AN X-BAND ELECTRICAL BALANCE DUPLEXER FOR IN BAND FULL DUPLEX COMMUNICATIONS

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ABSTRACT

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In Band Full Duplex systems are getting popular to meet the increasing demand of consumers and stringent requirements of developing 5G systems. In this type of communication, receiver and transmitter frequencies are at the same carrier frequency and occurs simultaneously, increasing both data rates and spectral efficiency. Its advantage over time division duplexing and frequency division duplexing have been theoretically proven and practically demonstrated in a number of recent studies. One major bottleneck of this type of duplexing is the echo created by the leakage from the transmitter to the receiver due to the same carrier frequency of the receiver and the transmitter. A typical design challenge is to suppress this leakage so that the transmitted signal does not appear as a blocker, reducing receiver's sensitivity. A novel method is to use an electrical balance duplexer which provides an isolation in a single antenna receiver if the antenna impedance is equal to a balancing impedance connected to the other side of the duplexer. However, antenna impedance varies considerably due to environmental factors, reducing the suppression. In order to achieve adequate suppression in practical implementations, a varying matching load, tuned to the varying antenna impedance is required. Typical way of creating a matching load is to construct a digitally configurable load which can be externally switched to desired impedance. However, discrete number of switches limit the performance and hence isolation in some cases. In the context of this thesis, a new balancing archi-

tecture for electrical balance duplexer is proposed and analyzed. Unlike other works in the literature, the proposed architecture has the capability to suppress in a continuous range of impedances rather than discrete steps. This system offers flexibility to the designers as the system can respond even to the slightest change in the antenna impedance maintaining maximum available isolation.

In order to evaluate the effectiveness of the proposed technique, it is implemented in a fully integrated system along with a power amplifier able to provide 1W of power and a differential LNA. The MMIC is tuned to work in the X-band and fabricated in a commercial 0.25 μm GaN on SiC technology. The measurement results show that the proposed system achieves a self interference cancellation level of more than 40 dB within a 100 MHz bandwidth for antenna impedance values up to 2.0:1 VSWR.

Keywords: Full Duplex, GaN, MMIC, Electrical Balance Duplexer, In Band Full Duplex, Balun

ÖZ

X-BANTTA ELEKTRİKSEL DENGE ÇİFT YÖNLEYİCİSİ İLE BANT İÇİ ÇİFT YÖNLÜ AKTARIM SİSTEMİ

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Bant içi tam çift yönlü aktarım sistemleri kullanıcılardan gelen yoğun talepler ve gelişmekte olan 5G sistemlerinde gerekli olan sıkı gereksinimleri sağlamak için popüler tasarımlar olmaya başlamıştır. Çift yönlü iletişimin aynı taşıyıcı frekans üzerinde gerçekleşmesi ve aynı anda aktarımın sağlanması bant verimliliğini ve veri iletim hızlarını artırmaktadır. Bu sebeplerden dolayı, zaman içerisinde bant içi tam çift yönlü aktarım sistemlerin frekans bölmeli çift yönlü sistemler ve zaman bölmeli çift yönlü sistemlere göre avantajları teorik olarak kanıtlanmış ve pratik ortamlarda da gösterilmiştir. Bu tip sistemlerin en büyük dezavantajı vericiden alıcıya doğru olan sızmaların yarattığı yankılardır. İletişim hem eş zamanlı hem de aynı taşıyıcı frekans üzerinden yapıldığı için bu tip sızmalar kaçınılmaz bir sonuçtur. Bu sızmaları asgari düzeye indirerek verici sinyalinin bir enegelleyici sinyal olarak alıcıda ortaya çıkmamasını sağlamak bu yapının getirdiği en büyük tasarım zorluğudur. Elektriksel denge çift yönleyici adı verilen bir sistem, tek antenli sistemlerde anten empedansı ile denge empedansı aynı olduğu zaman yüksek izolasyon sağladığı için önerilmiştir. Fakat anten empedansı çevresel faktörlerden dolayı değişebilmektedir. Değişken anten empedansı sebebiyle empedans uyumunu sağlamak için dışarıdan değiştirilmek üzere anahtarlanabilir bir ayarlanabilir empedans yapılması gerekir. Belirli sayılarda yapılan bu anahtarlar, empedans ayarlaması yaparken genellikle bazı empedanslar için maksimum izolasyon değerini sğlayamaz. Bu tezin içeriğinde, elektriksel denge

çift yönleyici için yeni bir empedans dengeleme methodu önerilip analiz edilecektir. Literatürde olan diğer örneklerinden ziyade önerilen yapı her empedans değerinde aralıksız olarak istenilen bastırma değerini verecektir. Sonuç olarak tasarlanan sistem tasarımcılara anten empedansı değişimi sırasında bu değişimi dengeleyerek azami izolasyonu elde etmeleri için büyük bir avantaj sağalayacaktır.

Tezde sunulan çözüm bir çip üstünde sistem olarak üretilmiş olup güç amfisi olan bir verici, düşük gürültülü amfisi olan bir alıcı, bir balun ve dengeleme yükünden oluşmaktadır. Sistem 0.25 um SiC üzerinde GaN MMIC teknolojisi ile üretilmiştir ve üretilen çip 100 MHz bandında 40 dB ve üzerinde bir izolasyonu 2.0:1 duran dalga voltaj oranında sağlamıştır. Tez, teorik analiz, şema ve serim tasarımı, elektromanyetik benzetimler ve sistemin tam verifikasyonunu içermektedir.

Anahtar Kelimeler: Tam Çift Yönlü Aktarım, GaN, MMIC, Electrical Balance Duplexer, Bant İçi Çift Yönlü Aktarım, Balun

To my family

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TABLE OF CONTENTS

LIST OF TABLES

TABLES

LIST OF FIGURES

FIGURES

LIST OF ABBREVIATIONS

BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
CMOS	Complementary Metal Oxide Semiconductor
EBD	Electrical Balance Duplexer
FDD	Frequency Division Duplexing
HEMT	High Electron Mobility Transistor
IBFD	In Band Full Duplex
IC	Integrated Circuit
ISV	Inside Source Via
LNA	Low Noise Amplifier
KCL	Kirchhoff's Current Loop
MMIC	Monolithic Microwave Integrated Circuit
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
OSV	Outside Source Via
PA	Power Amplifier
RF	Radio Frequency
SAW	Surface Acoustic Wave
SI	Self Interference
SIC	Self Interference Cancellation
SNR	Signal to Noise Ratio
SPDT	Single Pole Double Throw
TDD	Time Division Duplexing
VSWR	Voltage Standing Wave Ratio

CHAPTER 1

INTRODUCTION

Telecommunication is the process of transmitting signals or information by wired or wireless links between two or more objects. Modern telecommunication links are divided into three main groups. First type of the communication link is a simplex link which is only a single way communication link as depicted in Figure 1.1. There is only a transmitter in one system and the other system only receives. Since the receiving system cannot send signals to the transmitting system, the link is a single communication link which is referred as simplex. One common example to these kind of channels is the television broadcast system. Television systems receives information about the broadcast however cannot send data to the satellites.

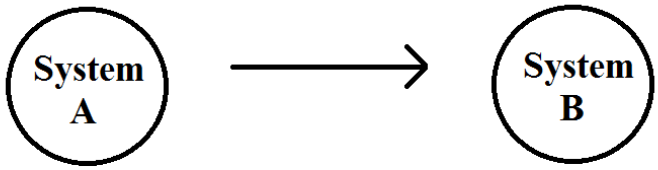


Figure 1.1: Simplex communication link

Second type of link is a duplex link where two way communication link can be established. Both of the systems now contains a transceiver which allows them to communicate back and forth. An example for a duplex link is a telephone communication where both sides can receive and transmit their voices throughout the link.

Third group of communication link is a multiplex link where multiple systems can communicate over a single channel simultaneously. Aim of the multiplexing systems

is to provide a communication link to a high number of users using limited amount of resources like bandwidth and channel. Typical multiplexing systems include a frequency division multiplexing where the channels are divided into different frequencies which allows simultaneous transmission but occupying a large bandwidth.

1.1 Duplex Systems

Duplex systems maintain two way communication link from both systems. Internet connection is an example of a duplex communication, which establishes a two way connection with the server. Users can send data to the server requesting a download and the server responds it by sending the data via the same channel. Figure 1.2 shows a duplex link between systems.

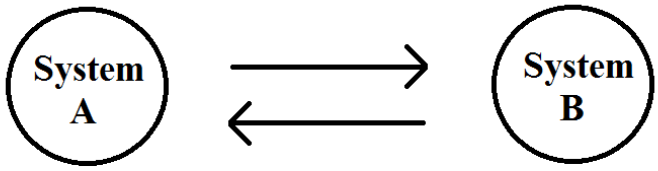


Figure 1.2: Duplex communication link

Duplex systems are further divided into two subgroups according to the simultaneous data transmission. These subgroups are:

- Half duplex which doesn't allow simultaneous communication
- Full duplex which allows simultaneous communication

1.1.1 Half Duplex

Half duplex is a type of duplex system which has a two way communication link. However during the communication only one way link can be active at a time instant.

A half duplex link can be established using time division duplexing (TDD). TDD systems use a single carrier frequency to transmit signals in the same channel however

divides the time slots for transmission for each end.

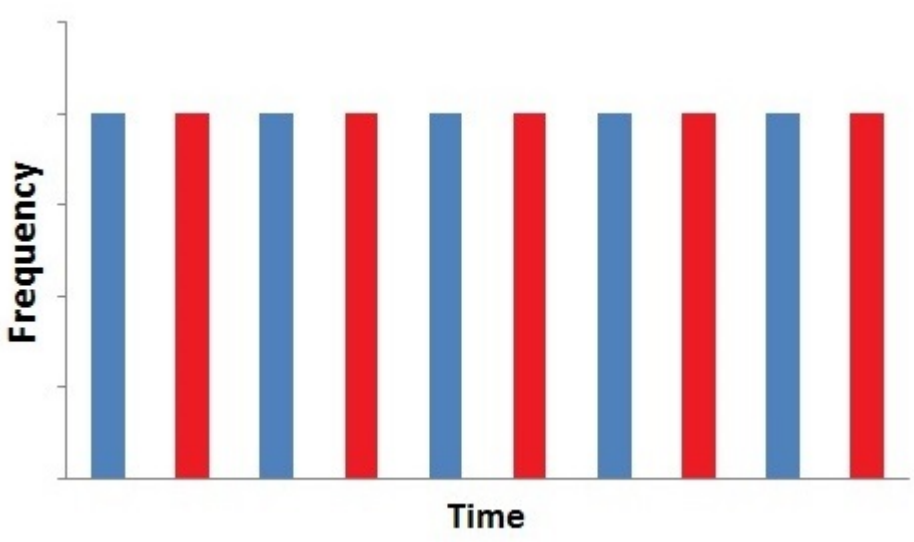


Figure 1.3: Time and frequency relation for a time division duplex system

Figure 1.3 depicts how a TDD system works. Blue lines indicate a transmission in one way and red lines indicate a transmission in the opposite direction. In order to avoid overlapping of signals, a guard time interval is used to separate the two link.

A simple and a common way to achieve TDD is the use of an RF switch [1]. A single pole single throw (SPDT) switch can be used to connect antenna to the receiver and the transmitter. A simplified RF schematic for TDD systems is given in Figure 1.4. A typical example of time division duplexing is walkie talkie systems. In normal operation, the radio stays in receiving mode where it only receives signals. However, when the user presses a button in the radio, radio immediately ends receiving signals and starts transmitting the user's voice. Therefore, it cannot receive or transmit signals at the same time.

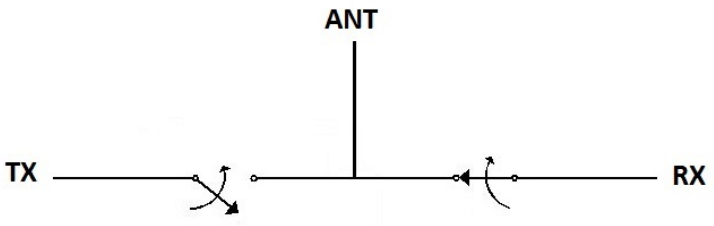


Figure 1.4: Connection of an SPDT switch of a TDD system

Typical examples of worldwide standardized TDD systems are:

- UMTS TDD mode [2]
- IEEE 802.16 WiMAX TDD mode [1]
- Half-duplex packet switched networks WLAN and Bluetooth

1.1.2 Full Duplex

A full duplex link allows two way communication simultaneously achieving transmission and reception to occur at the same time. A practical full duplex link can be achieved using frequency division duplexing. This method requires the transmission and the reception to be done at different carrier frequencies to prevent overlapping of the signals.

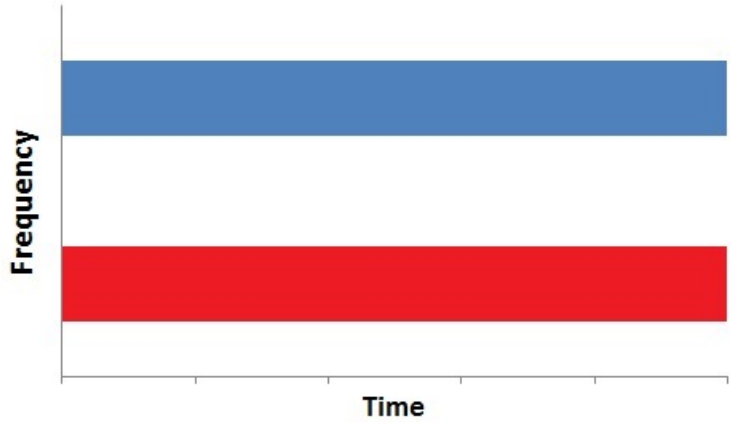


Figure 1.5: Time and frequency relation for a frequency division duplex system

As seen from Figure 1.5, separate bands are allocated for two way link and there is a spacing between the two bands. This interval is referred as a guard band [3] which ensures that the two frequency bands do not overlap.

A practical FDD system typically employs a diplexer to perform the correct operation. A diplexer consists of low loss filters such as surface acoustic wave (SAW) filters. These filters have sharp transitions and have low insertion losses making them ideal to be used to define frequencies of the transmitter and receiver.

A simplified RF schematic is given in Figure 1.6. Instead of an RF switch, there are two filters placed at different center frequencies and bands to allocate the bands and

suppress the leakages from transmitter to receiver or visa-versa.

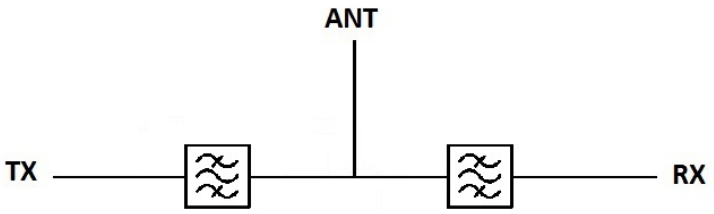


Figure 1.6: Diplexer connection in an FDD system

Typical examples of worldwide standardized FDD systems are:

- UMTS/WCDMA[2]
- IEEE 802.16 WiMAX FDD mode[1]
- ADSL and VDSL

1.1.3 Comparison Between TDD and FDD systems

Many worldwide telecommunication standards have relied on the TDD and the FDD operation. In addition to this, some of the standards have used both of the transmission types using their advantages at specific points.

In terms of bandwidth, TDD is more efficient since it uses a single carrier frequency whereas FDD uses two different carrier frequencies for communication. In order to serve same amount of customers, FDD communication uses double the amount of band compared to TDD. Especially, when the cost of the common communication bands such as GSM bands are considered, FDD can be a highly expensive way to adopt.

When the transmission is asymmetric (i.e. uplink and downlink rates are different from each other), TDD has certain advantages [5]. Consider a case when a user needs to download a large amount of data from the internet. User makes a request from the server, which usually requires small amount of data. Upon the receipt of the request, the download starts which constitutes of large amount of data and takes a long time to complete. If FDD is used instead of TDD, then the transmission channel must be

separated into two frequency channels which allocates large bandwidths and limits the download rate since the full bandwidth cannot be used. However, TDD maintains the allowable bandwidth throughout the link. In that case, user sends the download request for a short amount of time and the download starts after the request. The established link uses the maximum allowable bandwidth in TDD case.

If the communication link is symmetric, which means download and upload rates are the same, FDD is more advantageous than TDD. As two separate channels are allocated for transmission and reception, FDD allows continuous links between systems, which increases data rates.

One typical disadvantage of FDD systems is the requirement of electronics that are tuned at two different carrier frequencies. This makes the system design highly expensive as two separate transceivers must be designed to operate an FDD system. Furthermore, the antenna costs also rise in the case of FDD, where two separate antennas tuned to different frequency are used. In contrast; a TDD system operates at one carrier frequency which only requires one transceiver design and a single frequency antenna design which is a cheaper and simpler solution than FDD.

Table 1.1: Comparison of TDD and FDD

	TDD	FDD
Number of carrier frequencies	1	2
Spectral Efficiency	100%	<100%
Link Continuity	Not simultaneous	Simultaneous
Advantageous data link type	Asymmetric	Symmetric
Cost	Cheap	Expensive

Table 1.1 gives a comparison of FDD and TDD in different aspects. FDD systems consumes high bandwidth and therefore are costly, but allows simultaneous communication. TDD systems use a single frequency, therefore allocates less bandwidth and cheaper in terms of system construction and bandwidth. However, simultaneous operation is not possible. To sum up, each method compromises the spectral efficiency or the total throughput to achieve duplex communication.

1.2 In Band Full Duplex

As the development of new 5G systems is going underway, the requirements for the systems are getting tougher each day. Each base station must serve many users with highest available bandwidth and efficiency. The increasing demand of high performance pushed designers to develop new and alternative methods. One of these methods is called in band full duplex (IBFD). This kind of duplexing requires that the transmission and reception to be done at the same time and using the same carrier frequency. With this method, all spectral band can be used with the highest data rate available, since reception and transmission can be done at the same time.

In band full duplex combines the major advantages of TDD and FDD. It allows simultaneous operation with only single carrier operation. Cost of designed system is also cheaper since transceiver design is tuned to a single frequency. Symmetric or asymmetric data rates won't matter in this case as there is a single carrier frequency and a simultaneous operation. Moreover, IBFD communication doesn't require any guard band or guard time to operate correctly which furthermore increases efficiency and data rate.

In ideal operating conditions, if the receiver and the transmitter are totally isolated, communication can occur at the same frequency in a simultaneous manner. However, in practical operation, due to the finite isolation between the transmitter and receiver, transmitted signal directly appears (albeit with some loss) at the input of the receiver. This is called as a self-interference (SI) signal.

SI can occur in different ways [6], as illustrated in Figure 1.7. Path 1 shows the direct coupling from the transmitter PA to the receiver LNA, path 2 shows the direct coupling from the antennas and path 3 shows coupling from the reflectors in the environment.

SI can lead to serious problems in the transceiver design. Since the output power of the transmitter is high, any high amount of coupling from PA to LNA can lead to desensitization of the receiver LNA. If the receiver LNA is compressed due to the high input power, it will not provide any gain to the received low power signal which eventually causes no signal to be received.

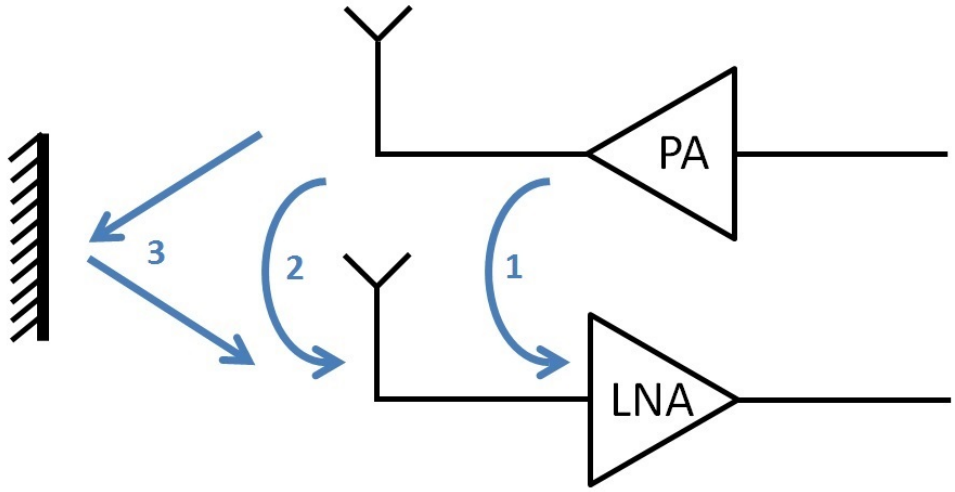


Figure 1.7: RF Self Interference paths

Low level couplings also pose a serious problem to these systems. For this case, the receiver LNA is not compressed, it provides all available gain to both the received signal and SI signal. However, since the output power is high and the received signal is at very low level, signal to noise ratio (SNR) degrades due to the presence of SI signal. The receiver, instead of processing the received signal, will process the delayed version of the transmitted signal. In terms of voice communication, the user will hear their own voice as a result of SI which is an undesired case. Therefore, these SI signals must be eliminated to ensure proper operation of the system.

1.3 Self-Interference Cancellation Techniques

In order to overcome the problem of self interference, several techniques have been proposed to achieve a cancellation of 100 dB or more [7]. In order to achieve this amount of suppression, different self interference cancellation (SIC) techniques are used at different layers of receivers. These layers are:

- RF self interference cancellation
- Analog self interference cancellation
- Digital self interference cancellation

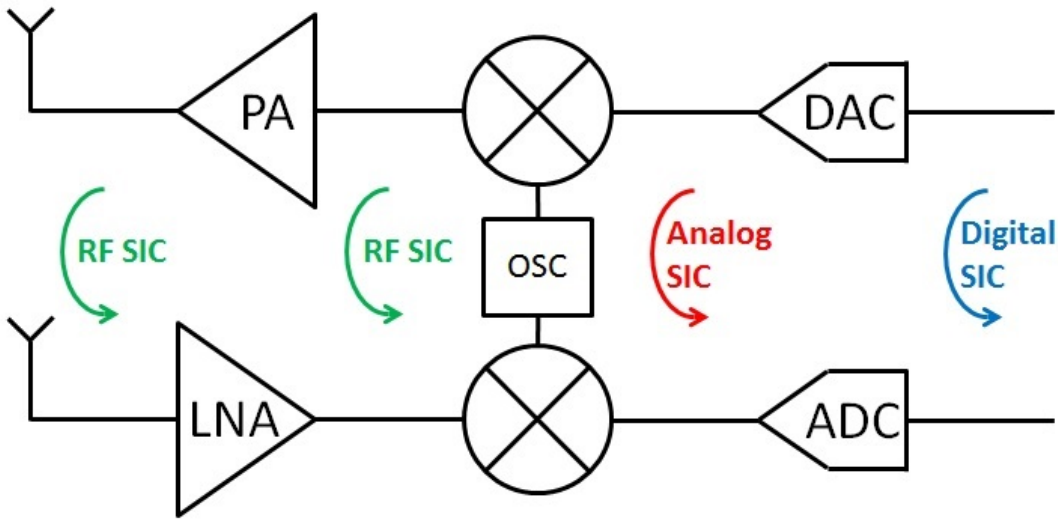


Figure 1.8: Self Interference Cancellation Paths

Figure 1.8 shows the SIC stages. RF SIC starts from the receiver antenna and ends at the first down-conversion stage. Analog SIC starts from the first down-conversion stage and ends at the receiver ADC. After the sampling is completed, digital SIC techniques starts to take effect.

Perfect cancellation can occur with the subtraction of perfectly reconstructed SI signal. Following effects must be taken account for perfect cancellation [8]:

- Phase Noise of the oscillator
- Quantization error of Analog to Digital Converter (ADC)
- Power amplifier nonlinearities
- Phase compensation
- Channel estimation

In three different domains, SIC techniques focus on matching these effects in order to achieve perfect cancellation. Some of these effects are deterministic, however many are random requiring adaptive cancellation techniques. Therefore achieving a suppression of 100 dB or higher requires a combination of different techniques in different domains. Practical systems employ a SIC stage in the RF, another SIC stage

in the analog domain and finally an SIC stage in the digital domain to fully cancel SI signals.

The main motivation of this thesis is to propose an effective RF SI cancellation method. The cancellation on other domains is beyond the scope of this thesis and will not be discussed.

1.4 RF Self Interference Cancellation Circuits

Most of the SIC can be performed at the RF stages of the receiver. RF cancellation adds a flexibility to the design and mitigates the linearity requirements for the following stages of the receiver chain due to the reduced transmitter power at the input of the receiver.

RF SIC relies on different mechanisms. The first method is to minimize the coupling from the transmitter and the receiver. Reduction of direct coupling from the PA to the LNA or between the transmitter and the receiver antennas is a SIC method and can be performed in the RF stage of the receiver.

Other method is to subtract a form of the output from the input. A perfect SIC requires that the subtracted signal must have an equal amplitude and a phase alignment with the received self interference signal.

1.4.1 RF Circulators

An RF circulator is a non-reciprocal three ports component that only transmits the RF signal from a port to the next port while isolating the signal from the remaining port. Circulators are typically constructed using ferromagnetic materials which provides them their unique transmission properties. In general, S-parameters of RF circulator mathematically can be expressed as [9]:

$$[S] = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 1 & 0 & 0 \end{bmatrix}$$

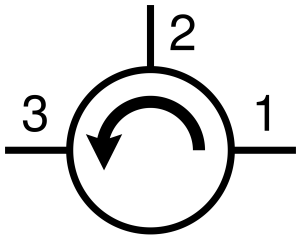


Figure 1.9: Symbol of RF Circulator

Form Figure 1.9, the transmission is defined in a counter clockwise fashion, meaning the first port transmits signal to second port only and signal entering from second port transmits energy to the third port and signal entering from third port is transmitted to first port.

As an SIC method, a circulator can be placed as a duplexing element in between the transmitter, receiver and antenna. Figure 1.10 shows a typical connection of a circulator in an IBFD system. The RF signal coming out of transmitter PA travels to the antenna while receiver is isolated by the circulator. The signal that enters from antenna travels to the receiver in ideal conditions.

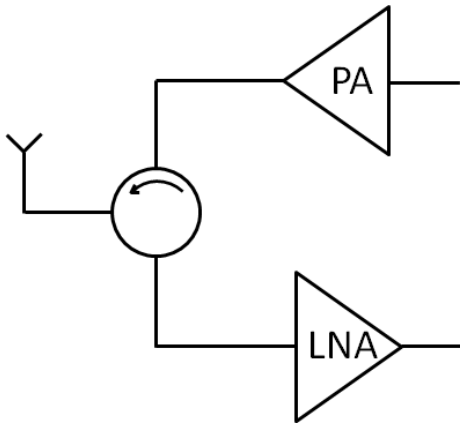


Figure 1.10: RF Circulator usage in IBFD system

The isolation amount in real circulators are finite. This limitation causes a circulator to provide a limited amount of SIC in an IBFD system. Examples of works in literature show 18 dB to 26 dB isolation by only using circulators [10] [11] [12].

Although, a circulator provides a simple way of cancellation, this insufficient cancellation around 20 dB forces extra SIC methods to be utilized at the RF stages. An RF circulator is most commonly employed with a feedforward canceler, that will be

explained in the following chapter, to provide sufficient SIC [10] [11] [12].

Ferromagnetic nature of the circulator makes it hard to be implemented on IC processes. Circulator, antenna, receiver and transmitter must be combined on a PCB which increases system area and cost.

One more disadvantage of circulator is that isolation amount is highly dependent on antenna and circulator impedance mismatch. Let's consider a case where all circulator ports are perfectly matched to 50 Ω and antenna has a reflection coefficient of -10 dB. RF signal entering from PA will travel to antenna and from antenna it will be reflected by an amount of 10 dB and again enter into the circulator. Even if circulator provides a perfect isolation, due to poor antenna match, SIC is limited to 10 dB. Antenna impedance must be controlled all the time to provide a high amount of SIC.

In conclusion, RF circulators provide a simple way providing SIC however due to finite amount of isolation additional cancellation stages are required. Moreover, antenna mismatch can significantly deteriorate SIC amount and incompatibility with IC technologies increases system cost and area.

1.4.2 RF Feedforward Cancellation

RF feedforward cancellation is a method of cancelling the SI using a feedforward path. This method directly aims to generate a phase and amplitude matched SI signal and at some point in the RF block, use this generated signal to eliminate the SI [13][14].

A general system approach is summarized in Figure 1.11. Output of the power amplifier is sampled using a coupler. The amplitude of the sampled signal is adjusted using a variable attenuator. Phase of the sampled signal is adjusted using a variable phase shifter.

The SI signal can be written in terms of transmitted signal, P(t), as

$$k.P(t-\tau)+n(t) \tag{1.1}$$

where, $P(t-\tau)$ is a delayed version of P(t) by an amount of τ, k is the coupling factor, $n(t)$ is the additive white noise.

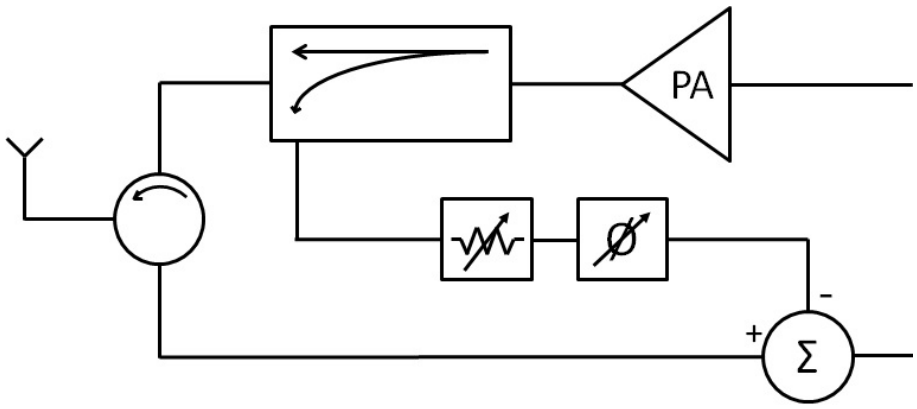


Figure 1.11: RF Feedforward cancellation schematic

In order to fully cancel the SI, coupling factor and the delay must be estimated. If there is a small error in the phase or in the amplitude, the resulting cancellation becomes ineffective and limits the system performance.

Let us assume, $P(t) = cos(\omega t)$ for the sake of simplicity.

Resulting self interference signal will be (with the noise term neglected):

$$P_{SI} = k.cos(\omega t - \omega\tau) \tag{1.2}$$

Since $\omega\tau$ is a constant term, it can be written as a single constant θ, which is in radians.

When there is an error in the amplitude of the reconstructed SI signal to be subtracted but there is perfect phase alignment then

$$P_{SIC} = P_{SI} - P_R \tag{1.3}$$

$$P_{SIC} = k.cos(\omega t - \theta) - k_1.cos(\omega t - \theta) \tag{1.4}$$

$$P_{SIC} = (k - k_1).cos(\omega t - \theta) \tag{1.5}$$

In dB scale, P_{SIC} can be written as:

$$P_{SIC,dB} = 20.log(k - k_1) \tag{1.6}$$

In order to achieve 40 dB SIC, amplitude difference must be less than 0.01.

When there is an error in phase alignment but perfect match in the amplitude, then

$$P_{SIC} = k.cos(\omega t - \theta) - k.cos(\omega t - \theta_1) \tag{1.7}$$

$$P_{SIC} = k[cos(\omega t - \theta) - cos(\omega t - \theta_1)] \tag{1.8}$$

$$P_{SIC} = -2k.sin(\omega t - \frac{\theta + \theta_1}{2}).sin(\frac{\theta - \theta_1}{2}) \tag{1.9}$$

If the phase error is small, (1.9) can be simplified to

$$P_{SIC} = k.(\theta - \theta_1).sin(\omega t - \frac{\theta + \theta_1}{2}) \tag{1.10}$$

In dB scale, the SIC due to mismatched phases becomes,

$$P_{SIC,dB} = 20.log[k(\theta - \theta_1)] \tag{1.11}$$

$$P_{SIC,dB} = 20.log(k) + 20.log(\theta - \theta_1) \tag{1.12}$$

From (1.12), the amount of cancellation is directly equal to the addition of phase difference between the two signals in dB scale and the coupling amount in dB. If the two signals have 1^o of phase difference with a coupling amount of 0 dB then the cancellation would be 35.2 dB. For 20 dB SIC from the angle component, a resolution of 5.72^o is required.

If there is both amplitude and phase differences, SIC is found to be

$$P_{SIC} = \sqrt{k^2 + k_1^2 - 2.k.k_1.cos(\theta - \theta_1)} \tag{1.13}$$

In dB scale total SIC becomes,

$$P_{SIC,dB} = 10.log[k^2 + k_1^2 - 2.k.k_1.cos(\theta - \theta_1)] \tag{1.14}$$

(1.14) suits to a more practical case as there is some amplitude and phase error in the cancellation signal.

These calculations are valid for small phase errors and narrow band signals. In general, the coupling is a function of frequency which changes with respect to the frequency. If a wideband SIC is required, these frequency dependent terms must also be taken into account. In narrow band systems, this varying coupling amount can be approximated as a constant term at the center frequency.

In wideband systems, the phase mismatch also starts to cause some problems as the calculations are done by assuming a single frequency of operation. However as stated before; θ is equal to $\omega\tau$ which is a function of frequency. As the bandwidth increases, different delays would cause different phase shifts. Assuming constant phase throughout the whole bandwidth would limit the performance of the SIC cancellation circuit.

In calculations, for the sake of simplicity; the RF system is considered as a perfect 50 Ω system. Also in practical cases, imperfect matching between systems would cause reflections. As these reflections would also create some new SI terms that is needed to be canceled, performance would be limited.

The last impractical case is that in the derivation above, only a single SI signal is considered. However as Figure 1.7 suggests there are multiple paths for SI, so at the input receiver there could be a multitude of SI signals. These SI signals would have different delays and different amplitudes which requires to generate multiple signals to cancel SI limiting the SIC amount.

In a general case, SI signal can be written as:

$$P_{SIC} = k_1(\omega).P(t-\tau_1) + k_2(\omega).P(t-\tau_2) + ... + k_n(\omega).P(t-\tau_n) + n(t) \quad (1.15)$$

where, $k_n(\omega)$ is the frequency dependent coupling, $P(t-\tau_n)$ is the delayed response of the transmitted signal by delay amount of τ_n and $n(t)$ is the random noise.

If a circulator as seen in Figure 1.11 is employed, then there would be two major SI signals present at the receiver. First SI contributor is direct leakage from PA to LNA over the circulator and second contributor is the reflection between antenna and circulator. In case of multiple SI signals, the cancellation circuit would be able to cancel the largest SI term which would yield the most suppression. Remaining SI signals would deteriorate the performance as they cannot be canceled by a single feedforward path cancellation. These errors would propagate to the next stages of the RF chain unless multiple feedforward paths are used.

Practical results indicate a SIC of 30 dB [13][14] at the RF stage by using RF feedforward cancellation. To further reduce SI levels, Venkatakrishnan et al.[13] added an additional feedforward circuit at the analog domain which provides an additional SIC

of 20 dB. Zhang et al. [15] designed another multiple feedforward paths achieving 55 dB SIC in total.

RF feedforward cancellation is an SIC method by directly generating and subtracting the SI components in the receiver from the transmitted components. Presence of multiple SI signals due to reflections and coupling, SIC levels are limited. In order to have a reasonable SIC, the transceivers must employ multiple feedforward cancellations in the receive chain. High resolution cancellation requires a tight control over amplitude and phase making complex circuit designs. In addition, every feedforward circuit injects noise to the receiver increasing the noise figure of the receiver. Due to all these imperfections, employing a feedforward technique is very hard.

1.4.3 Cross Polarized Antennas

Cross polarized antennas is another way of implementing SIC on RF domain. The idea is to use two differently polarized antennas to suppress the SI [16]. With receiver antenna at one polarization and transmit antenna at orthogonal polarization to receiver antenna, these antennas perform SIC at the frequency of interest.

Cross polarized antennas can provide high levels of SIC at a given frequency. One of the main reasons of SI is direct coupling from PA to LNA. As there are two antennas in the system, receiver and transceiver can be separated further to reduce coupling between parts. Furthermore, orthogonality between polarizations allow antennas to further reduce antenna to antenna coupling.

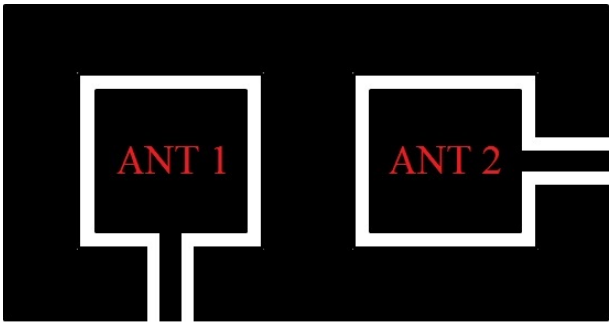


Figure 1.12: Two orthogonally polarized rectangular patch antennas

Figure 1.12 shows the layout of a two cross polarized rectangular patch antennas. By

changing the RF feeding direction to the patch antenna, orthogonal polarization is ensured in the system.

For two linearly polarized antennas, polarization loss factor [17], which is defined as the amount of polarization mismatch between two linearly polarized antennas, can be expressed as:

$$PLF = cos^2(\phi) \tag{1.16}$$

where ϕ is the angle difference between the polarization of the two antennas.
For two antennas that are placed together as shown in the figure 1.12, the SI power from the transmitter antenna to the receiver antenna can be written as:

$$P_{SI} = k.PLF \tag{1.17}$$

In order to achieve a perfect cancellation, (1.16) suggests that the two antennas must be polarized orthogonally. If there is a small angle offset from orthogonality:

$$P_{SIC,dB} = 20.log(k.cos(90 - \theta)) \tag{1.18}$$

$$P_{SIC,dB} = 20.log(k\theta) \tag{1.19}$$

$$P_{SIC,dB} = 20.log(k) + 20.log(\theta) \tag{1.20}$$

(1.20) suggests that the coupling is directly proportional to the SI signal level and the given polarization. As the coupling between the antennas are reduced, the SI levels would reduce with the amount of coupling. SIC furthermore increases with the orthogonality of the antennas.

A typical limitation for a cross polarized antenna design is due to the reflectors present in the area. A study by Everett et al. [18] clearly indicates that a cross polarized antenna pair provides an SIC level of 70 dB when the experiment is performed at anechoic chamber. However, when outside reflectors are present, SIC drops to 50 dB.

In literature, there are examples of works which maintained SIC greater than 50 dB with cross polarized antennas [18][19][20]. Unlike RF feedforward path method, cross polarized antennas offer an SIC greater than 50 dB in a single stage.

Cross polarized antennas offer a high SIC levels at RF level. More than 50 dB SIC is a mitigates SIC requirements of the preceding stages. However, employing two antenna instead of one causes a larger area consumption and increases system cost due to additional antenna. Performance degradation under the presence of reflectors can cause a variation is the SI levels during operation which is not a desired case. To conclude, cross polarized antennas can provide high amount of SIC with a cost of high area allocation.

1.4.4 Electrical Balance Duplexer

An electrical balance duplexer (EBD) is a type of duplexer which allows in band full duplex operation with the help of a hybrid transformer (a.k.a. balun). Figure 1.13 shows a simplified version of an EBD. The center tap of the hybrid transformer is connected to the output of the power amplifier. The primary coil is connected to an antenna and a load which is referred to as a balancing load. The secondary coil of the balun is directly connected to a differential LNA [21].

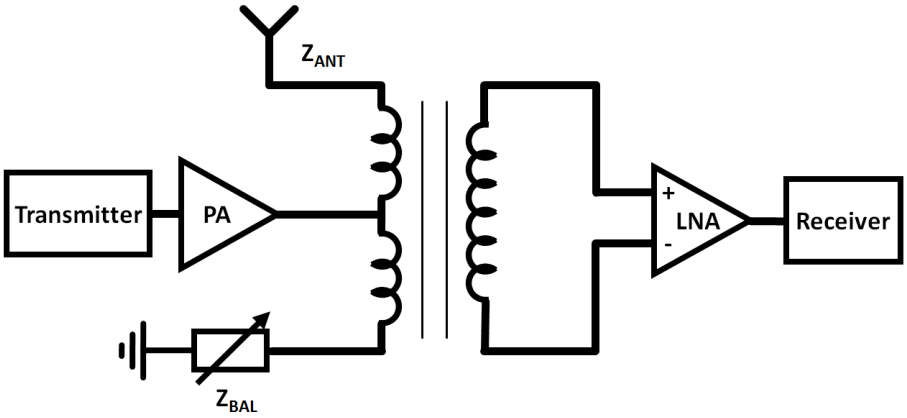


Figure 1.13: A simplified EBD system

The name of the electrical balance comes from the fact that when the balancing impedance which is referred to as Z_{BAL} in Figure 1.13 is equal to the antenna impedance, Z_{ANT}, the transmitted signal appears as a common mode signal to the input of the LNA. With the use of a differential LNA, the common mode signal, which is SI signal, is suppressed by the common mode rejection of the LNA. The signal entering from the antenna port appears as a differential signal to the input of the differential

LNA and amplified by the differential gain of the amplifier. The signal flow is depicted in Figure 1.14 [22].

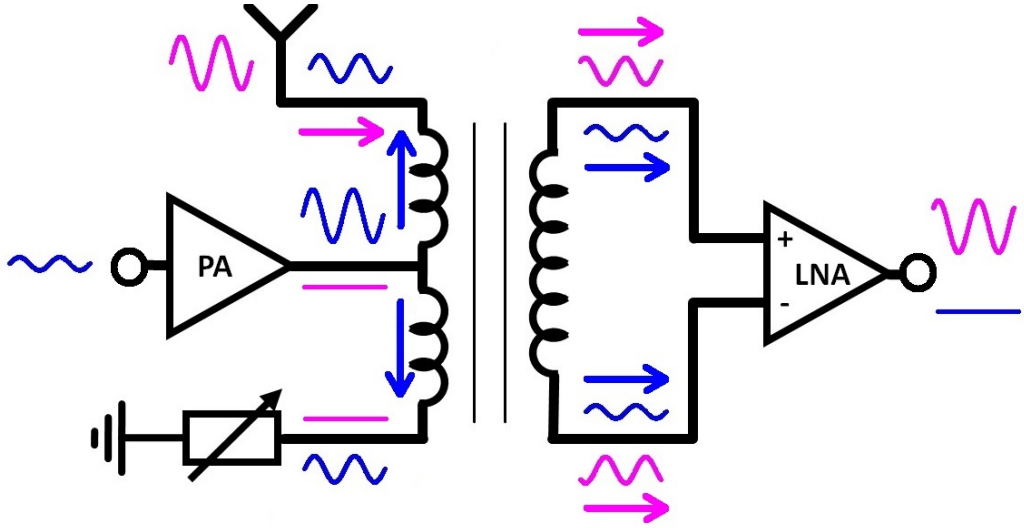


Figure 1.14: Transmitter and receiver signal flow in an EBD system. Blue lines show the transmitted signal, purple line shows received signal

It should be noted that, in order for an EBD to achieve full cancellation of the SI, the signal from the PA should appear as common mode at the input of the LNA. This is only achieved when the antenna impedance shown in Figure 1.13 perfectly matches with the balancing load impedance. However, in practical implementations the impedance equality between the antenna and the balancing load may not hold as the antenna impedance may change with the changing environment conditions. Therefore a balancing load that is capable of matching the antenna at every impedance point must be designed. Typical tunable load design includes a π matching section as seen in Figure 1.15 [23]. By making capacitors variable at the design of low pass π matching section, the electrical balance hence SIC can be obtained.

Examples in literature offer more complex balancing loads that can be tuned externally with a voltage source. A modified π [23][24][25][26] is shown in Figure 1.16. The output load and the capacitances are made tunable using MOSFET transistors parasitic capacitances and resistances. This structure can cover a large area of impedances with a cost of silicon area. In order to stack up two inductors and tunable capacitors would occupy a large area.

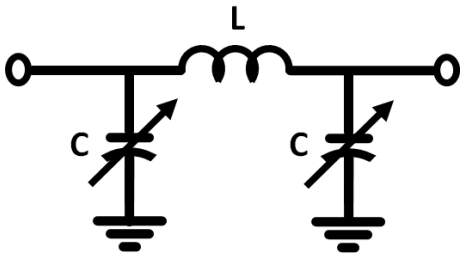


Figure 1.15: Low pass π matching section

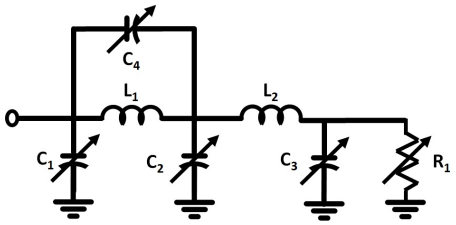


Figure 1.16: Modified π matching section

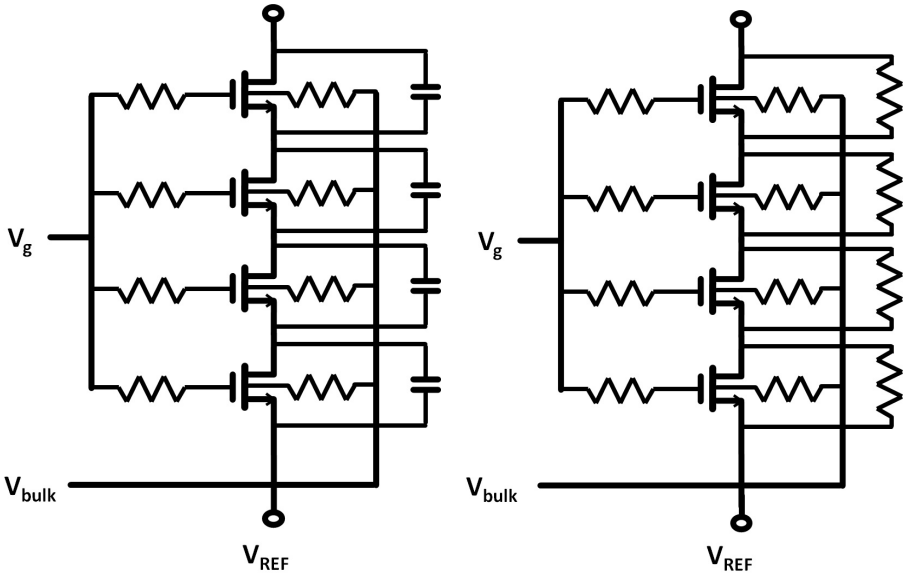


Figure 1.17: Tunable capacitor (left) and resistor (right) structures

Tunable capacitances and resistances can be implemented using same circuit topology as shown in Figure 1.17 [27]. A MOSFET transistor can act as a capacitance at its cut-off state and a resistance at its linear mode. By digitally adjusting V_g and V_{ref}, desired operation can be adjusted.

Some balancing load structures use only a parallel RC to emulate a balancing load [27]-[32]. This type of load only covers capacitive and resistive changes in the an-

tenna impedance. Although simple and area effective, these structures fail to provide isolation at every antenna impedance, impeding SIC at certain impedance points.

Generally designs only demonstrate the EBD operation without a transceiver solution. Some examples only present EBD structure and balancing load [23][25][33][34] where most of the examples only demonstrate EBD with LNA in a single chip [24][26] [27][28][30][31][32][35].

Moreover the examples in the literature are concentrated on the frequency regions between 0.5 GHz to 2.5 GHz [23]-[28], [30]-[34]. There are a few millimeter wave implementations of an EBD system at 30 GHz [35] and 120 GHz [29] that show promising results. In addition, all of the EBD designs found in the literature to date, were implemented in CMOS/BiCMOS technologies of various gate lengths.

1.5 Motivation of the Thesis

In the literature, there are various EBD designs that successfully demonstrate high isolation in a given bandwidth. Each design introduce a novel method to implement SIC at various scenarios.

These designs typically use same balancing load architecture to match the antenna impedance, with only difference in resolution and impedance coverage. The are also implemented as discrete impedances meaning the impedance change only covers discrete values [23]-[34].

A fully integrated solution is not presented in many of the EBD designs. To show functionality, most of the times only EBD and LNA are integrated into the same chip. PA is typically connected at outside of the IC [23]-[34].

Last but not least, many of the EBD solutions are implemented at frequencies lower than 3 GHz [23]-[28], [30]-[34]. As radio systems are being developed at higher frequencies like 60 GHz, it must be shown that this kind of topologies can work higher than 3 GHz.

Main motivation of this thesis is to address all of these missing parts in literature,

by forming an EBD system with a novel way of balancing which doesn't use any topology presented in the literature and implemented at 10 GHz with PA, EBD and LNA integrated into the same chip. Instead of traditional ways like π matching circuit, this thesis investigates the effect of matching impedances by varying the differential LNA branch currents. This proposed method is further supported by and increase an active balancing load to increase the tuning range. Rather than using discrete switching values, balancing is done continuously in this work providing SIC at every antenna impedance. In addition, unlike other implementations this IC is implemented in a commercial GaN on SiC process rather than typical CMOS/BiCMOS processes.

This work provides comparable performance in terms of SIC amount and SIC bandwidth. In terms of impedance range coverage and tuning, this unique way of balancing gives a state-of-the-art performance when compared to its counterparts.

This thesis is organized as follows; in chapter 2, an introduction to the EBD design is given along with theoretical calculations of balun. The same chapter will also introduce the novel balancing method. Chapter 3 introduces each of the circuits designed in the thesis and provides their simulation results. Chapter 4 provides details on the measurement methodology and measurement results of the fabricated ICs along with a conclusion and a discussion on the future work.

CHAPTER 2

ELECTRICAL BALANCE DUPLEXER DESIGN

In the introduction part, a basic description of the system is presented. In order to construct an electrical balance duplexer, four different types of circuits are required. These circuits are Power Amplifier (PA), balun, differential Low Noise Amplifier (LNA) and a balancing load to match the antenna impedance. Since the measurements were done on a wired setup (no antenna were used), a varying load impedance (Z_{LOAD}) is used to emulate an antenna with varying impedance. The whole designed system is given in Figure 2.1. In order to test the system in a single ended setup the differential output of the LNA is converted into a single ended output, with a balun at the output.

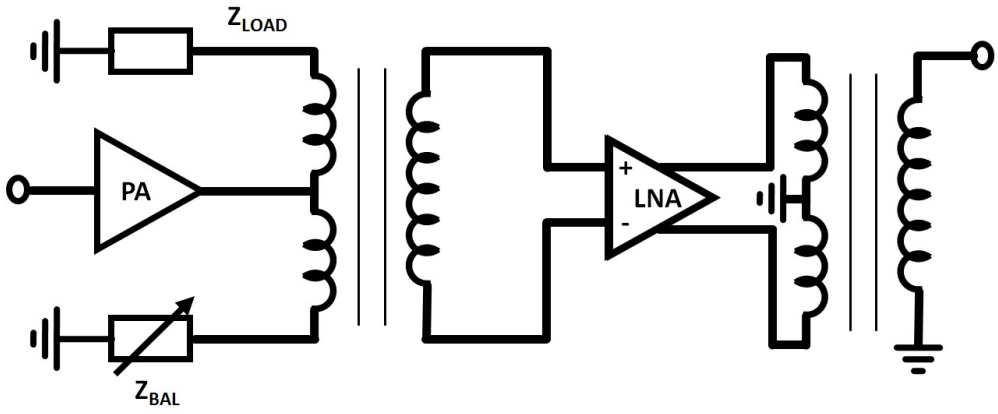


Figure 2.1: EBD system design

In this work all the system components as shown in the block diagram of Figure 2.1 was developed and implemented on a commercial GaN process.

In order to present a useful IBFD system, the system developed here was designed to

produce a transmitted power greater than 30 dBm while providing more than 40 dB of isolation in a 100 MHz band. The radio was designed to work in the X-band, to be used both for civilian and military applications. It was decided that the SIC to be performed for varying antenna impedances inside the Γ=0.3 circle.

The full system is integrated into a single chip using a commercial 0.25 μm GaN on SiC process. This chapter includes a theoretical analysis of the EBD system starting from the analysis of an ideal balun. By using ideal balun model, signals entering from PA and antenna are analyzed separately. Then a differential amplifier is analyzed in detail for the proposed method. Finally, a brief introduction for a balancing load is presented.

2.1 Novel Balancing Method

The concept of EBD depends on a balun structure which is the essential unit in providing isolation between the transmitter and the receiver.

2.1.1 Balun

A balun is a type of electronic component which converts a balanced signal into an unbalanced signal or vice versa. Balanced signal refers to a differential signal where the signals do not have a common ground. Unbalanced signal refers to a signal that is acting on a common ground. The name balun is also an acronym of "balanced to unbalanced".

In order to convert an unbalanced signal to a balanced signal, a hybrid transformer with a center tap can be used which is shown in Figure 2.2. The voltage and current on the transformer coils are also presented in Figure 2.2. If the voltage V_1 and current I_1 is on the primary coil, then due to the 1:1 transformer ratio, total voltage and current on the secondary coil must be the same with the primary coil. Then the voltage and the current equations for a hybrid transformer with center tap becomes:

$$V_1 = V_2 + V_3 \tag{2.1}$$

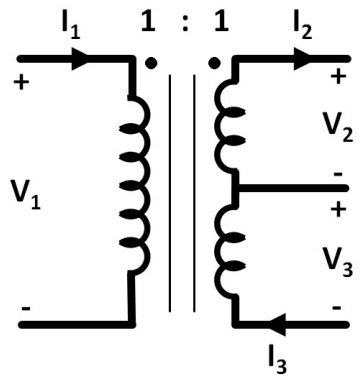


Figure 2.2: A hybrid transformer with a center tap which is a balun

$$I_1 = I_2 = I_3 \tag{2.2}$$

If the center tap is placed at the middle of the secondary coil, then the voltage equation become:

$$V_1 = 2V_2 = 2V_3 \tag{2.3}$$

Now the signal at the secondary coil becomes a balanced signal because it doesn't depend on any ground. Due to the equal values of I_2 and I_3, the center tap acts as a virtual ground.

If input impedance of Z is seen from the primary coil, then from voltage and current relations, input impedances at the secondary coil can be found as $Z/2$. This means that a balanced impedance of 50 Ω is converted into 100 Ω unbalanced impedance.

2.1.2 EBD Analysis with Signal from the PA

In an EBD, the balun is connected as shown in Figure 2.1. In this configuration, a power amplifier is connected to the center tap of the balun on the secondary coil and a differential LNA is connected on the primary coil to amplify the signal received by the antenna. In order to analyze the full operation, a linear balun is assumed which is necessary to apply superposition on the system. Each input source, which is transmitted signal from the PA and received signal from the antenna, are analyzed separately and the results are combined yielding full system operation.

A balun can be assumed a linear device because it is constructed using passive ele-

ments. Passive circuits also exhibit some nonlinearity at high power levels. However, at the power levels of this work, balun can be considered as a highly linear component. Therefore superposition can be applied to ease the analysis.

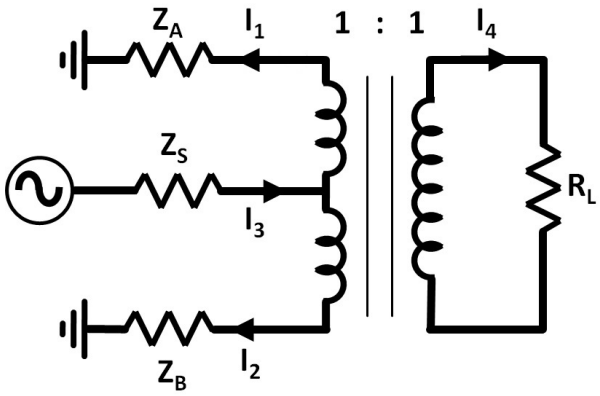


Figure 2.3: Port impedances in an ideal balun

As the first case of superposition, it is assumed that the transmitted signal is on and the antenna input source is off. If perfect match between antenna impedance Z_A and balancing impedance Z_B is achieved as in Figure 2.3, then the following voltage and current relations can be derived:

$$I_3 = I_1 + I_2 \tag{2.4}$$

Due to the impedance equality, the currents can be rewritten as:

$$I_3 = 2I_1 = 2I_2 \tag{2.5}$$

Z_S sees an impedance of two Z_A connected in parallel hence impedance match is achieved when:

$$2Z_S = Z_A \tag{2.6}$$

As the currents I_1 and I_2 are balanced, they induce currents of the same magnitude in opposite directions. Therefore, no net current is produced in the primary coil which results in no power transmission to the primary coil of the balun. No power at the primary coil means an isolation between the transmitter and receiver.

When the port impedances are concerned, if antenna impedance Z_A is equal to Z_O, then (2.6) states that Z_S must be equal to $0.5Z_0$ for a matched system. At the primary coil, the port impedance becomes $2Z_0$ to result in a matched system.

When the impedances are unbalanced, currents flowing to the antenna impedance and the balancing impedance are different. As a result, the secondary coil is unbalanced and generates a net current flowing at the primary coil. Figure 2.4 shows the analysis circuit, for the unbalanced case where $Z_A \neq Z_B$. In order to analyze the circuit, the source impedance is multiplied by two and secondary coil is separated into two coils where each coil has a turn ration of 1:2 with the primary coil.

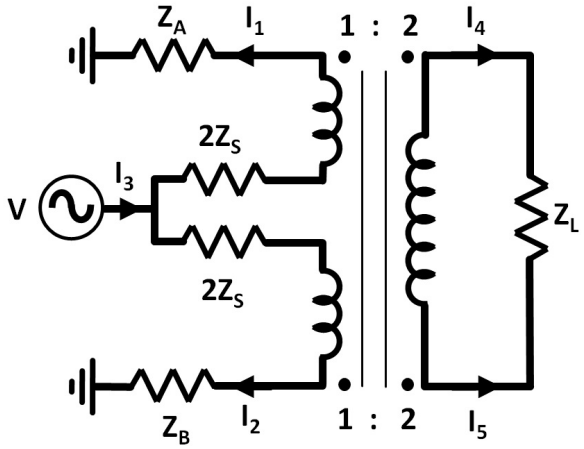


Figure 2.4: Analysis circuit for unbalanced case

Currents I_1 and I_2 can be written in terms of supply voltage as:

$$I_1 = \frac{V}{2Z_S + Z_A} \tag{2.7}$$

$$I_2 = \frac{V}{2Z_S + Z_B} \tag{2.8}$$

Two separate transformers that have a turn ratio of 1:2 results in the decrease in the excited current on the primary coil to half.

$$I_4 = \frac{V}{4Z_S + 2Z_A} \tag{2.9}$$

$$I_5 = \frac{V}{4Z_S + 2Z_B} \tag{2.10}$$

Net current on the impedance Z_L is equal to

$$I_T = I_4 - I_5 = \frac{V}{4Z_S + 2Z_A} - \frac{V}{4Z_S + 2Z_B} \tag{2.11}$$

$$I_T = I_4 - I_5 = \frac{V(Z_B - Z_A)}{2(2Z_S + Z_A)(2Z_S + Z_B)} \tag{2.12}$$

Total coupled power can be calculated using these current and impedance values.

$$|k^2| = \frac{|Z_B - Z_A|^2}{4|2Z_S + Z_B|^2} |\frac{Z_L}{Z_A}| \tag{2.13}$$

When a fully matched system is concerned, (2.13) is modified with port impedances in terms of Z_0, resulting in

$$|k^2| = \frac{|Z_B - Z_A|^2}{2|Z_0 + Z_B|^2} |\frac{Z_0}{Z_A}| \tag{2.14}$$

These calculations assume a matched condition between the source and load impedances. If load impedance deviates from the matched termination condition, then the currents on the balancing and antenna impedance is modified to accompany a proper operation in the balun structure.

(2.14) can be expressed with the reflection coefficients from the antenna and the balancing load. Defining impedances as reflection coefficients where the system impedance is Z_0:

$$Z_A = Z_0 \frac{1 + \Gamma_A}{1 - \Gamma_A} \tag{2.15}$$

$$Z_B = Z_0 \frac{1 + \Gamma_B}{1 - \Gamma_B} \tag{2.16}$$

Then (2.14) becomes,

$$|k^2| = \frac{|\Gamma_B - \Gamma_A|^2}{|1 - \Gamma_A^2|} \tag{2.17}$$

(2.17) shows that the difference in the reflection coefficients determines the coupling from the transmitter to the receiver. Moreover, the coupling further increases if antenna impedance deviates from Z_0 which is another deterioration of system performance.

2.1.3 EBD Analysis with Signal from the Antenna

At the antenna side, the analysis is pretty straightforward. By using superposition, the PA is replaced with a matched load which is Z_S and a source is connected to the antenna terminal. Then by writing KCL equations, the system is solved.

Figure 2.5 shows the connection of elements in the analysis of EBD from antenna side. If I_1 enters from antenna side, then current equations on the secondary coil can

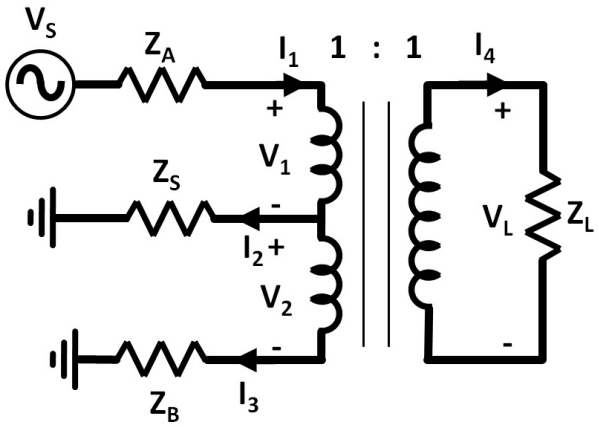


Figure 2.5: EBD analysis from antenna side

be written as:

$$I_1 = I_2 + I_3 \tag{2.18}$$

From Figure 2.5 upper half of the secondary coil is induced with the current I_1 and bottom half of the secondary coil is induced with current I_3. Due to 2:1 transformer ratio with each half coil and primary coil, the currents induced on the primary coil can be calculated as:

$$I_4 = \frac{I_1 + I_3}{2} \tag{2.19}$$

Voltage induced on the load V_L is:

$$V_L = I_4.Z_L = \frac{I_1 + I_3}{2} Z_L \tag{2.20}$$

Again due to 2:1 transformer ratio with each half coil and primary coil, this voltage can be rewritten at the secondary coil as half of the V_L. on the secondary coil can be written as:

$$V_1 = V_2 = \frac{V_L}{2} \tag{2.21}$$

With these defined voltages, KCL equations can be written to solve the system.

$$V_S - I_1 Z_A - I_2 Z_S = \frac{V_L}{2} = \frac{Z_L}{4}(I_1 + I_3) \tag{2.22}$$

$$I_2 Z_S - I_3 Z_B = \frac{V_L}{2} = \frac{Z_L}{4}(I_1 + I_3) \tag{2.23}$$

From these KCL equations, a relationship between currents I_1 and I_3 can be written as below which will be used in later parts.

$$I_3 = \frac{Z_S - \frac{Z_L}{4}}{\frac{Z_L}{4} + Z_S + Z_B} \tag{2.24}$$

Impedance seen by the antenna can be calculated using (2.22),(2.23) and given in (2.25):

$$Z_A = Z_S + \frac{Z_L}{4} - \frac{(\frac{Z_L}{4} - Z_S)^2}{Z_S + Z_B + \frac{Z_L}{4}} \tag{2.25}$$

If antenna impedance $Z_A = Z_0$ is chosen and $\frac{Z_L}{4} = Z_S$ is set then,

$$Z_A = Z_S + Z_S - \frac{(Z_S - Z_S)^2}{Z_S + Z_B + Z_S} = 2Z_S = Z_0 \tag{2.26}$$

$$Z_S = \frac{Z_0}{2}, Z_L = 2Z_0 \tag{2.27}$$

An important fact is that if the equality $\frac{Z_L}{4} = Z_S$ holds, then the input impedance seen from antenna doesn't depend on the balancing impedance Z_B. If the power from the input and on the load is computed, then the coupling can be calculated.

$$P_{in} = |I_1|^2[Z_S + \frac{Z_L}{4} - \frac{(\frac{Z_L}{4} - Z_S)^2}{Z_S + Z_B + \frac{Z_L}{4}}] \tag{2.28}$$

$$P_L = \frac{|I_1|^2(2Z_S + Z_B)^2}{4(Z_S + Z_B + \frac{Z_L}{4})^2} R_L \tag{2.29}$$

From (2.28) and (2.29) coupling can be calculated as:

$$|k^2| = \frac{(2Z_S + Z_B)^2.Z_L}{4(Z_S + Z_B + \frac{RZ_L}{4})[Z_B(Z_S + \frac{Z_L}{4}) + Z_S.Z_L]} \tag{2.30}$$

If $\frac{Z_L}{4} = Z_S$ and $Z_A = Z_B$ condition is satisfied, which is the desired condition to minimize the leakage from transmitter to receiver, then coupling function reduces to $|k^2| = 0.5$. This means that only half of the power incident on the antenna is coupled to the receiver at desired operation. This loss would increase the overall system noise figure by 3 dB because it is before the amplification stage.

2.2 Real Balun

Real baluns, due to finite physical lengths and material losses, have a degraded performance which are not considered in the calculations in the previous parts.

Although they are symmetrically designed and assumed, due to manufacturing defects, conductor distances, lengths and widths can vary inside the structure. These

defects affect the coupling between conductors and can result in a current imbalance between ports. Varying coupling over the conductors causes an amplitude imbalance, where the currents in each branch don't have equal magnitudes. This effect can be modeled simply by changing the turns ratio of the balun to generate the required imbalance. Unequal length of lines generates different delays in the currents on branches and results in a phase difference between lines, which is called as phase imbalance. Both of these effects are random in a symmetrically designed balun caused by manufacturing defects. However, as will be detailed in the following sections, this work presents a novel way to balance these manufacturing defects by introducing a small offset in the differential LNA biases.

Due to physical length of the lines in a balun, a phase shifted version appears at the terminals of the baluns which weren't considered in the calculations. This doesn't affect the calculations because balancing between the signals are preserved, although a phase shift occurs in the currents induced.

Real conductors like metal lines and dielectric substrate produces some loss in the transmission of the signals. Due to finite conductivity of the metal lines, there are some conductor losses which can be modeled as a series resistance in the balun structure. Dielectric loss on the other hand, produces a loss due to the imperfect dielectric material which can also be modelled as a series resistance.

All of these effects are linear effects, where they can be modelled with linear elements. For the sake of simplicity, these effects won't be considered in calculations here but worth mentioning in the design and analysis of an EBD system. However, in the final design of the system, electromagnetic analysis tools were employed, taking all these effects into account. By this way, a very accurate representation of the non ideal effects was created in the design phase increasing the confidence of the manufactured system.

2.3 Differential Amplifier Design

Referring back to Figure 2.1, the output of the primary coil is amplified by a differential amplifier. Moreover, as will be explained shortly, this differential amplifier is

used to balance the transmitter signal in order to provide a SIC for in band full duplex operation.

To begin, lets consider a single HEMT device. A HEMT transistor can be modelled as given in Figure 2.6, considering only intrinsic elements:

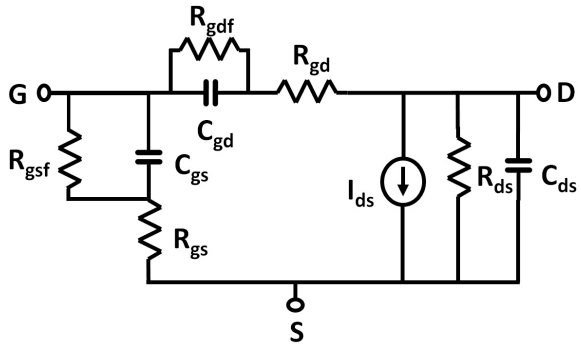


Figure 2.6: A small signal linearized model for HEMT devices [36]

In HEMT small signal model given in Figure 2.6, current I_{ds} depends on multiplication of the transconductance times the gate to source voltage. If the transistor provides a voltage gain from the gate to the drain, then the impedance from the gate to the drain can be divided as impedances from the gate to the source and the drain to the source according to the Miller Theorem [37].

Fig 2.7 shows a circuit representation of Miller theorem. The impedance Z is divided by approximately the voltage gain of the amplifier (considering the gain is much larger than 1) and placed between the gate and the source terminals. Assuming voltage gain is large, then impedance Z directly appears between the drain and the source terminals of the amplifier. With this way the impedance between the gate and the

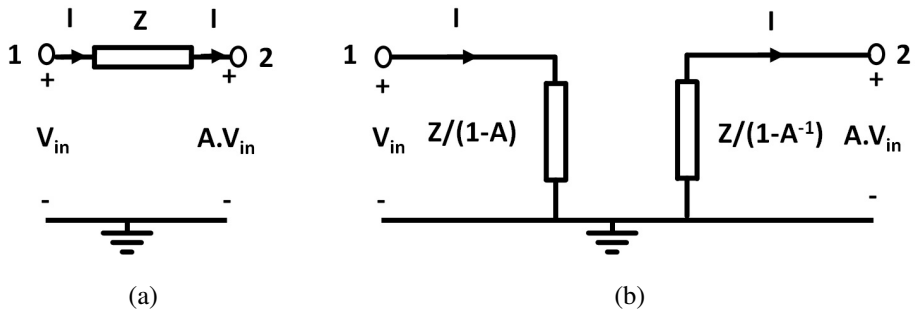


Figure 2.7: Miller theorem equivalent circuit[37]

drain is removed and distributed between the gate to source and the drain to source junctions.

By using HEMT transistors, a differential amplifier in Figure 2.8 can be formed.

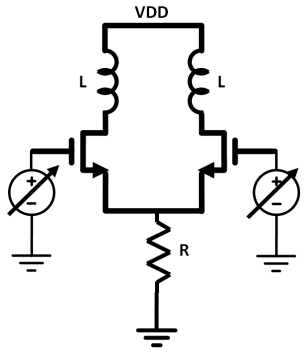


Figure 2.8: A simple differential amplifier

By using the small signal model for a HEMT device, a small signal model of the differential amplifier in Figure 2.8 is formed as shown in Figure 2.9. It is important to note that, the quiescent points of the amplifier branches are considered different and all related circuit elements are named distinctively. This is needed to explain how the novel SIC technique presented in this thesis is performed by tipping the balance of the quiescent point of the differential pair.

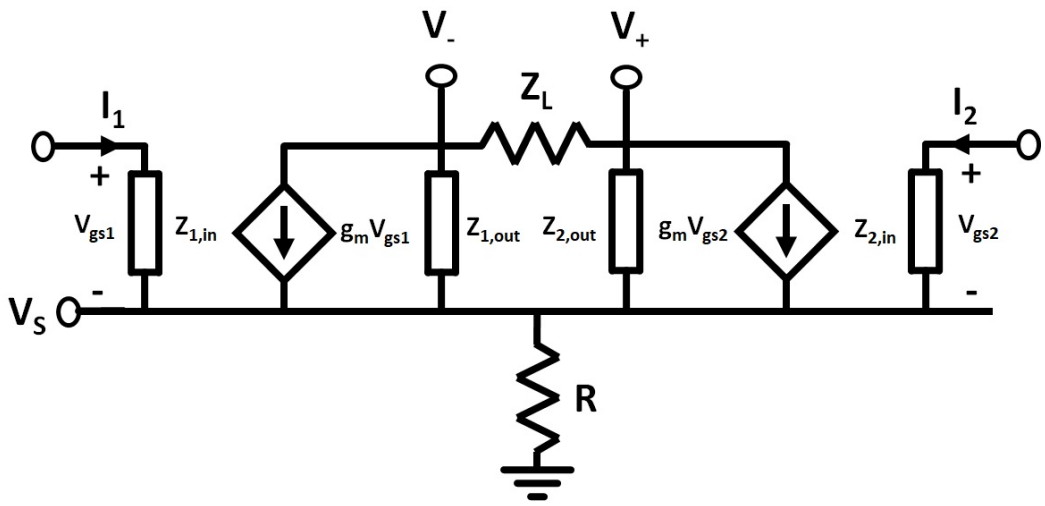


Figure 2.9: Small signal model for a differential amplifier

If we write node equations for the nodes V_S, V_+ and V_- assuming currents I_1 and I_2

entering into the opposite branches:

$$\frac{V_S - V_-}{Z_{1,out}} + \frac{V_S}{R} + \frac{V_S - V_+}{Z_{2,out}} = I_1 + I_2 + gm_1 V_{gs1} + gm_2 V_{gs2} \tag{2.31}$$

$$\frac{V_- - V_+}{Z_L} + \frac{V_- - V_S}{Z_{1,out}} + gm_1 V_{gs1} = 0 \tag{2.32}$$

$$\frac{V_+ - V_-}{Z_L} + \frac{V_+ - V_S}{Z_{2,out}} + gm_2 V_{gs2} = 0 \tag{2.33}$$

Rearranging (2.32) and (2.33),

$$\frac{Z_{1,out}(V_- - V_+)}{Z_L} + V_- + gm_1 Z_{1,in} Z_{1,out} I_1 = V_S \tag{2.34}$$

$$\frac{Z_{2,out}(V_+ - V_-)}{Z_L} + V_+ + gm_2 Z_{2,in} Z_{2,out} I_2 = V_S \tag{2.35}$$

V_S terms can be eliminated, leaving an equation dependent on input currents and output voltages.

$$\frac{(Z_{1,out} + Z_{2,out} + Z_L)(V_+ - V_-)}{Z_L} = gm_1 Z_{1,in} Z_{1,out} I_1 - gm_2 Z_{2,in} Z_{2,out} I_2 \tag{2.36}$$

(2.36) gives a general expression for the output voltage in terms of the input currents. Now the induced currents from the transmitter and the receiver can be replaced with I_1 and I_2 to determine the gain of the system. Using superposition theorem on different signals, both gains are calculated separately. For calculating these cases, $Z_A \neq Z_B$ is assumed.

For transmitted signal, (2.7) and (2.8) represent I_1 and I_2 respectively in (2.36). Substituting these values,

$$A(V_+ - V_-) = gm_1 Z_{1,in} Z_{1,out} \frac{V_{tr}}{8Z_S + 4Z_A} - gm_2 Z_{2,in} Z_{2,out} \frac{V_{tr}}{8Z_S + 4Z_B} \tag{2.37}$$

Setting right hand side of the (2.37) to zero, perfect SIC can be obtained. The condition is satisfied when,

$$gm_1 Z_{1,in} Z_{1,out}(2Z_S + Z_B) = gm_2 Z_{2,in} Z_{2,out}(2Z_S + Z_A) \tag{2.38}$$

Transconductances and impedances are all functions of the DC bias current of the transistors. Therefore manipulating the current in the branches, this equation can be equalized.

For received signal, (2.24) gives a relationship between I_1 and I_3 currents that forms the currents I_1 and I_2 respectively in (2.36). Substituting these values,

$$A(V_+ - V_-) = gm_1 Z_{1,in} Z_{1,out} \frac{I_1}{2} + gm_2 Z_{2,in} Z_{2,out} \frac{I_1(Z_S - \frac{Z_L}{4})}{\frac{Z_L}{4} + Z_S + Z_B} \tag{2.39}$$

Due to the current excitation in reverse direction, current entering from antenna side appears as a differential signal. In (2.39), current values are added and as a result forming a gain even though the antenna deviates from desired impedance.

2.4 Balancing Load Design

A transistor can only cover some set of impedances as stated in the previous part. (2.38) suggests that using balancing impedance has an effect on the cancellation. In order to increase the impedance coverage of the structure, a balancing load capable of only providing a tunable real impedance can be used.

In order to reach high levels of SIC at every impedance value, the resolution of π matching circuit must be very high. Thanks to the use of the technique introduced above the differential amplifier will reduce the resolution requirement of balancing load. In this thesis, an active transistor will be used as a balancing load to act as a tunable resistor which is also a novel way of constructing a balancing load, as it presents a nearly perfect resistive impedance. By this way impedance coverage of the EBD system will increase covering all loads at $\Gamma = 0.3$ circle with maintaining the highest available SIC.

A simplified schematic for the balancing load concept is provided in Figure 2.10. As will be shown in the next chapter, by adding some lumped components the transistor will yield a real impedance, controllable by the gate voltage.

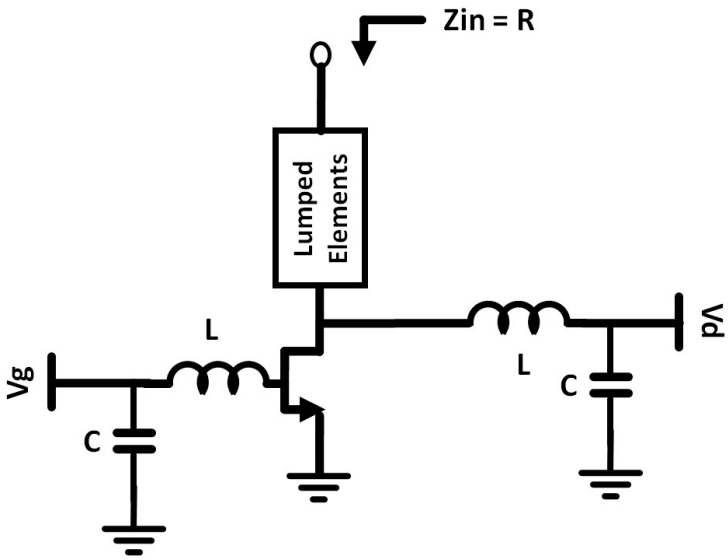


Figure 2.10: Simplified schematic of balancing load

CHAPTER 3

CIRCUIT DESIGN

In this chapter using the theory developed in the previous section, the circuits designed to achieve a fully integrated IBFD system is presented. The transceiver design includes a PA design, a balun design, a balancing load design and a differential amplifier design. All of these circuits are designed on a commercial 0.25 μm GaN on SiC process combined in a single IC.

This chapter begins with a description of the process that is used in the design and continues with the PA design, the differential LNA Design, the balun design and the balancing load design providing the simulation results associated with each circuit. At the end of the chapter, system level simulations are provided.

3.1 Process Evaluation

GaN high electron mobility transistors (HEMT) are suitable for high power amplifier designs as they can withstand higher powers when compared to their silicon and GaAs counterparts. Their high bandgap energy, which is around 3.2 eV[38], is almost three times that of GaAs and Si. Due to the high bandgap voltage, these transistors can withstand higher breakdown voltages and exhibits much larger power outputs.

In the design process, a commercial 0.25 μm GaN on SiC process from WIN Semiconductors is used. This process has transistors with cutoff frequencies up to 26 GHz. Due to the high cutoff frequency, this process is suitable for a design at 10 GHz where it can provide adequate gain and performance.

SiC substrate offers a high dielectric substrate ($\epsilon_r = 9.6$) which is a low loss dielectric material with thermal dissipation factor of 0.003. This low thermal dissipation factor and highly insulative substrate allows high quality passive devices to be constructed.

This process offers only depletion mode transistors with threshold voltages around -3 V. Negative threshold voltage requires a negative voltage source in order to bias the transistors in the saturation region with the highest transconductance.

28 V drain voltage operation allows high power output from a single transistor. In addition to the high power output, third point intercept and 1 dB compression levels of the transistors also increase which means the amplifiers can be more linear compared to the technologies with 5 V drain voltage.

Small signal parameters, when compared to GaAs technologies, provide higher noise figure and less gain. For a 4x100 μm transistor biased at 10 V and 100 mA/mm, the minimum noise figure is around 1.2 dB with the associated gain 10.82 dB. Although low noise amplifier can be designed with better specifications at different technologies, this process also offers a modest performance which is enough to show the performance of the proposed system.

At large signal operation, 2x125 μm transistor biased at 28 V and 100 mA/mm, provides saturated power at 31 dBm with the associated linear gain of 19.5 dB while 65% PAE.

These figure of merits suggest that this process can be used in the design of all circuits. For power amplifier, 250 μm width transistor can provide 31 dBm of power which eases the PA design of the system. Low loss substrate generates high quality factor balun which is essential for operation of EBD.

3.2 Power Amplifier Design

A power amplifier is an amplifier that provides a high power RF output that is generally placed before the antenna so that the antenna can transmit the signal.

A power amplifier can operate in different classes depending on their quiescent points.

The main four classes, which are A, B, AB and C are briefly discussed here. These classes are distinguished according to their conduction angle which can be defined as the angle of the output waveform that the transistor stays at the on state [39]. Figure 3.1 illustrates the conduction angle and corresponding output waveforms.

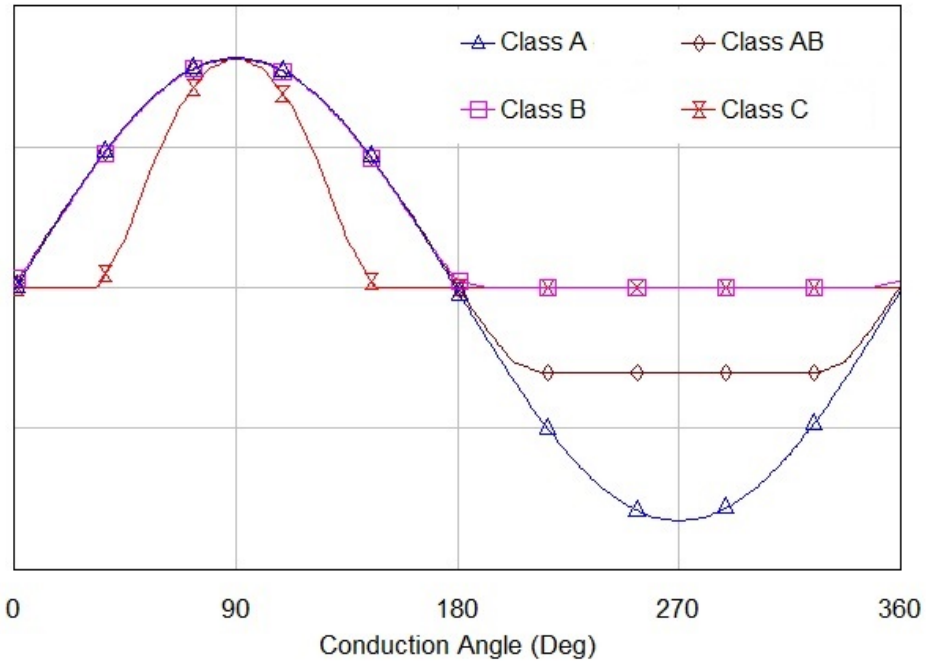


Figure 3.1: PA Classes at different conduction angles

A class A amplifier exhibits a full swing at the output waveform. Therefore the conduction angle can be stated as 360^{o} which is also shown in Figure 3.1. A simple common source amplifier that is biased in a way that allows full conduction acts as a class A amplifier. A simple schematic is given for a class A amplifier in Figure 3.2.

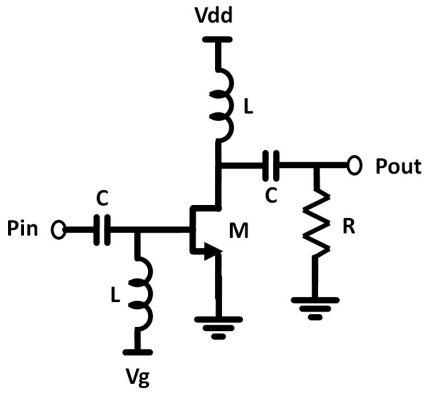


Figure 3.2: Class A PA schematic

Transistor's I-V characteristics can be assumed linear as in Figure 3.3. A linearized transistor provides a constant current for every drain voltage value and drain current is a linear function of the gate voltage. This assumption allows a simple analysis of a class A power amplifier and an estimation to its required output resistance.

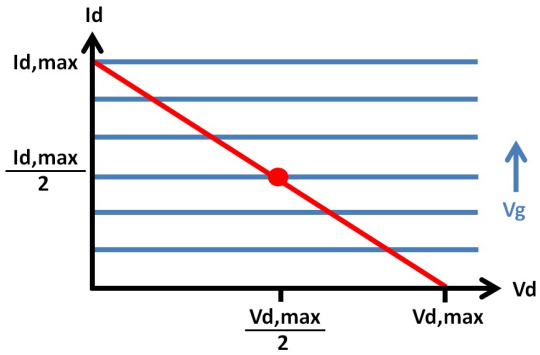


Figure 3.3: Linearized I-V characteristics

Maximum RF output power can be calculated as follows:

$$P_{RF,out} = \frac{V_{dd,max} I_{dd,max}}{8} \tag{3.1}$$

At the DC operating point, DC power is:

$$P_{DC} = \frac{V_{dd,max} I_{dd,max}}{4} \tag{3.2}$$

Hence, maximum drain efficiency can be calculated as 50%. Linearized transistor characteristic ensures maximum efficiency in the calculation however, practical transistors biased in class A operation yields 20% drain efficiency due to the their non-ideal characteristics.

Output load resistance can be found by using the load line in Figure 3.3. If the load resistance is selected as:

$$R_{opt} = \frac{V_{d,max}}{I_{d,max}} \tag{3.3}$$

then the maximum power output is obtained. Choosing another load resistance would decrease RF power output of the system however, efficiency would be constant if correct bias point is adjusted.

Class B amplifier is biased in a way that the amplifier only conducts half of the sine wave. This conduction results in a conduction angle of 180^o shown in Figure 3.1. In this mode of operation, the transistor is biased at a voltage where it is at the edge of

conduction. Therefore, it only conducts positive half of the sine wave and doesn't conduct anything at the negative half of the sine wave. Only DC power is spent at the conduction part therefore the efficiency increases. Theoretical maximum efficiency can be calculated as 78.5%.

Due to the half conduction, class B presents harmonic distortion at the output. For a half wave sine the fourier transform of the voltage waveform can be expressed as:

$$V(t) = \frac{A}{\pi} + \frac{A}{2}\, sin(\omega_0 t) - \frac{2A}{\pi} \sum_{n=1}^{\infty} \frac{cos(2n\omega_0 t)}{4n^2 - 1} \tag{3.4}$$

There is a trade-off between linearity and efficiency in the class B amplifier. By decreasing the conduction angle, nonlinear distortion increases.

Class AB amplifier is a middle state between class A and class B amplifier where the conduction angle is between 180^o and 360^o. This type of amplifier gives a compromise between efficiency and linearity where user can bias the amplifier to provide more efficient amplifier by sacrificing linearity or the other way around.

Class C amplifier considers the case where the conduction angle is reduced below 180^o. The theoretical efficiency can increase up to 100% at 0 conduction angle although it is not a practical state. However, decreasing the conduction angle would result in an increased harmonic distortion.

In the design of the power amplifier, a class AB topology is selected to provide an adequate efficiency with a low distortion. The design target is to reach 1 W of saturated power at the output of the power amplifier.

3.2.1 Transistor Choice and Load Impedance Selection

The commercial process used in the design of the MMIC offers two type of power transistors where the source is grounded with backvias. Inside Source Via (ISV) transistors have a backvia at each source connection of the transistor. Outside Source Via (OSV) transistors have two backvia connections at the outer side of the transistors. ISV and OSV transistor layout for a 6x125 μm is provided in Figure 3.4. The advantage of ISV over OSV is the reduction of source resistance to the ground and increased thermal conduction to the backside metal. However, due to the large size

(a) ISV transistor layout (b) OSV transistor layout

Figure 3.4: ISV and OSV transistor layouts

of the ISV transistors and a limited space available in the reticle imposed the use of OSV transistors.

In order to determine the load impedance where the transistor provides the best power output and efficiency, a series of load pull simulations are performed. Transistor size and biases are optimized to obtain the best output form a single transistor. As a result, a transistor size of 6x75 μm transistor with OSV is chosen.

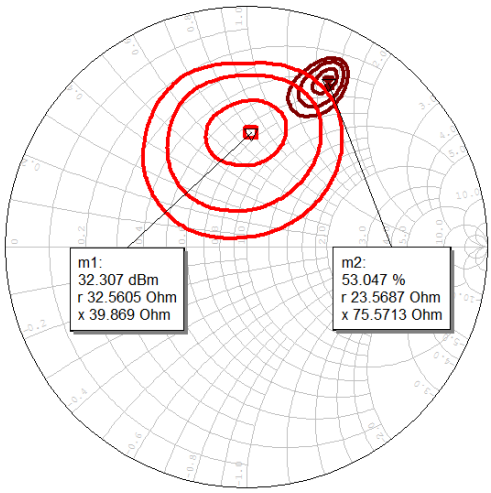


Figure 3.5: Load pull results for a 6x75 μm transistor

Figure 3.5 shows the load pull results of the transistor. At 10 GHz, 32.56+j39.87 Ω impedance yields the best output power which is 32.3 dBm This condition is obtained where the transistors are biased at a current of 25 mA.

According these figures, a two stage amplifier is formed with a single transistor for each stage. Single transistor can provide a saturated power output greater than

30 dBm. Therefore, the output stage contains only a single transistor. A small sized transistor is used to ease the matching conditions for the power amplifier.

3.2.2 Matching Circuit Design

Matching circuit is designed using a series L shunt C low-pass matching sections. For inductors, transmission lines are used to provide the required impedance shift. As the load impedance is close to the desired impedance condition of 25 Ω, a single stage matching is used for both stages of the amplifier.

In order to have a stable amplifier, some precautions are added in the matching circuit design. First precaution is to add a series resistance before the transistor to increase stability by decreasing the gain of the transistor. In this design, a series resistance of 5 Ω is used to ensure stability. Figure 3.6 shows the schematic of the PA with the stabilizing resistances.

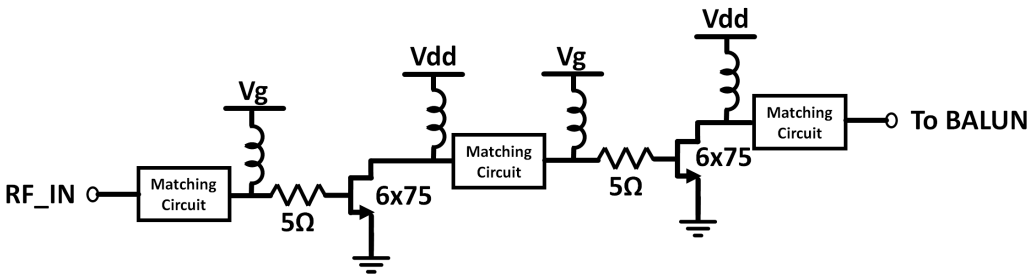


Figure 3.6: PA schematic view

Bias lines also act as matching elements of the system. Gate bias lines are composed of an input large decoupling capacitor at the input, a large valued choke inductor and a series resistance for gate biases. Drain bias voltages are supplied with lines that are composed of large decoupling capacitors and, large lines that act as a choke inductors. For drain biases, a resistance is not added due to the high current passing on the lines and preventing RF power dissipation at the output. Resistance addition on the input RF lines is the second precaution for the stability. This resistance dampens any resonance that can form between the supply rails hence decreasing feedback in the two stage amplifier.

As the stages are composed of single transistor, no power combining matching tech-

nique is required. Moreover, the problem of even odd mode oscillation is not a problem for this type of PA.

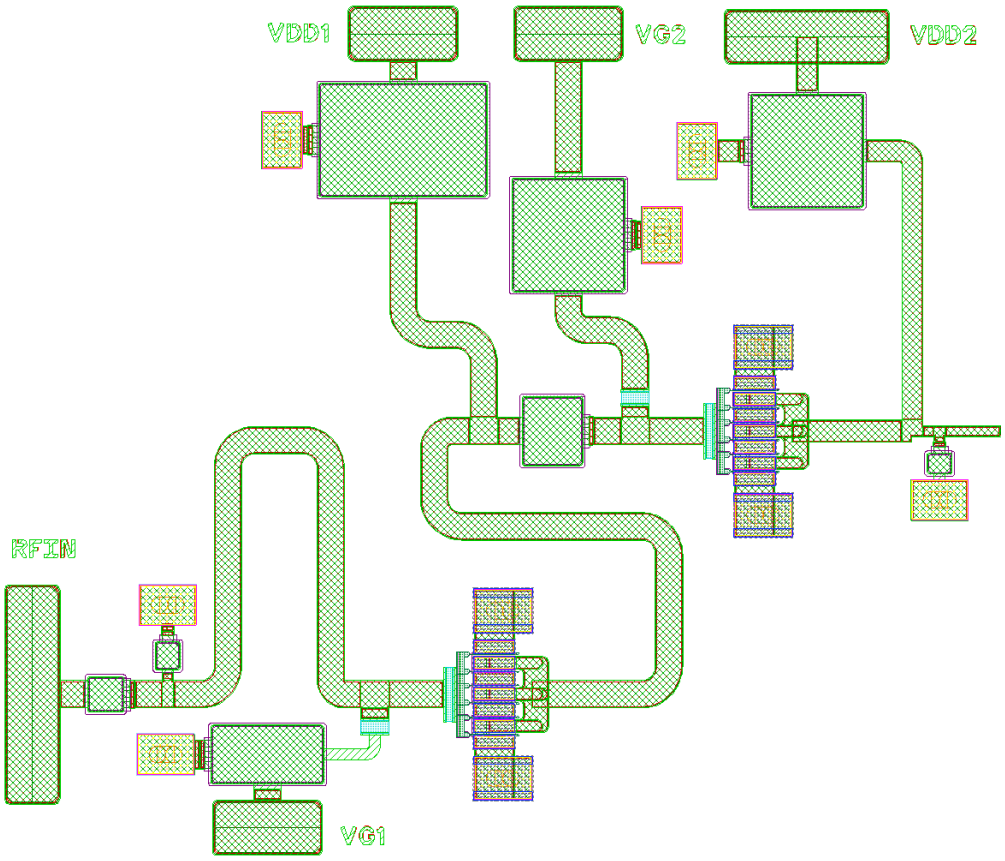


Figure 3.7: Layout of PA

Final layout of the power amplifier is given in Figure 3.7. Pad at the left side is the RF input of the system. RF input is DC blocked by a series capacitor at the input. Pad at the bottom side is the bias line for first transistor gate. Top pads are first stage drain bias, second stage gate bias, second stage drain bias from left to right respectively. At the right side, RF signals enters into the balun which is not shown in Figure 3.7.

3.2.3 Simulation Results

Simulations are performed using Microwave Office AWR software. The layout of the PA is simulated using 2D Electromagnetic solver AXIEM and parasitic and coupling effects in layout are included in the results. When simulating the PA, as there is high power, a harmonic balance simulator is used to model the PA.

Simulation results shows that PA can produce output power of more than 1 W at 10 GHz. Small size of the transistor and load impedance at close proximity to 25 Ω increased amplifier's bandwidth.

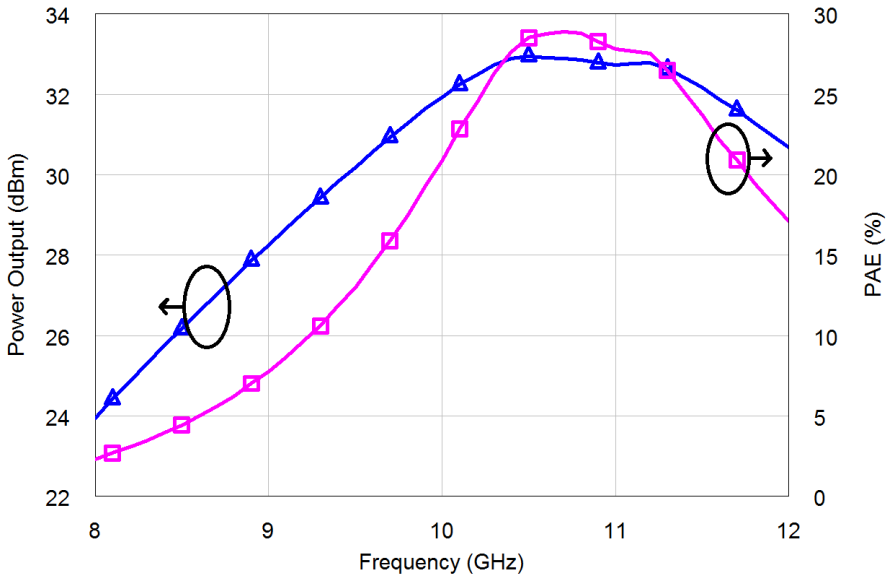


Figure 3.8: Saturated power output and PAE of PA

Fig 3.8 shows the power simulation results of the amplifier. At 10 GHz, the amplifier provides 32 dBm power at 20 % power added efficiency.

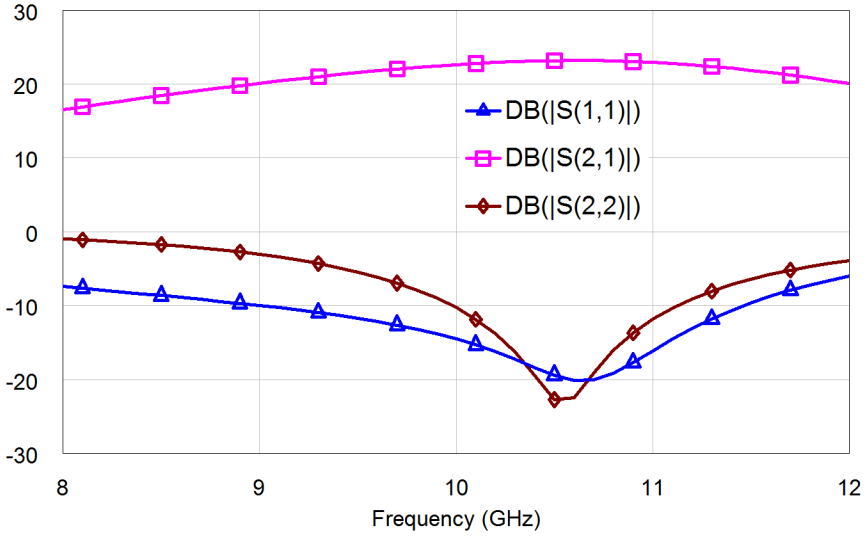


Figure 3.9: Small signal parameters of PA

Figure 3.9 shows small signal characteristics of the amplifier. Input matching is done

by considering the effect of wirebonds and transmission line at the input side of the amplifier. Output Matching is done considering the balun impedance which is 25 Ω. S_{11} and S_{22} are below -10 dB and S_{21} is above 20 dB for this power amplifier.

Figure 3.10 shows the small signal stability simulation of the amplifier. For stability, each stage is simulated on their own and results show that each stage of the amplifier is stable.

3.3 Differential Amplifier Design

Differential amplifier design is one of the most crucial circuit of the system. It must be a low noise amplifier where it can provide an amplification with the minimum noise figure. Since it is the second element in the receive chain, where the first one being the balun, its noise figure directly contributes to the overall noise of the system. When the losses of the balun are considered, the noise figure of the system must be kept as low as possible.

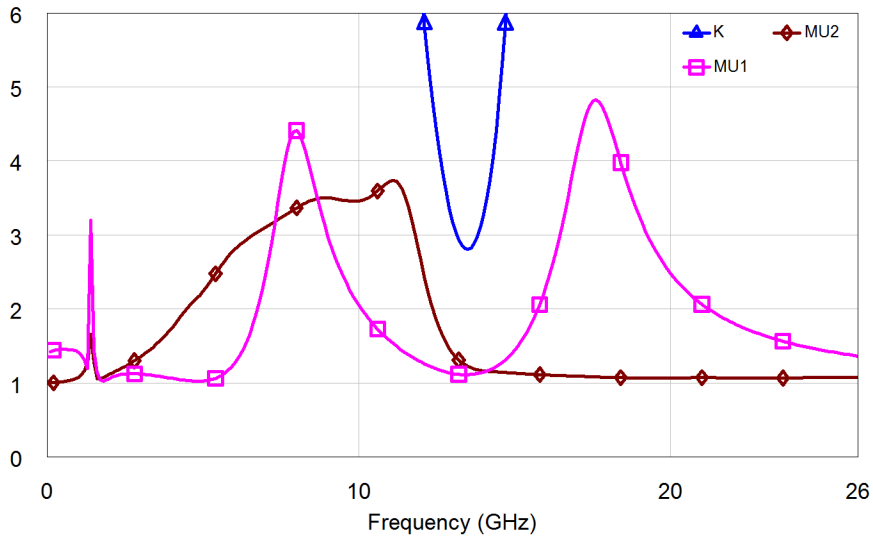
Factors affecting the design and things to be considered are explained in the following sub-sections.

3.3.1 Stability Concerns

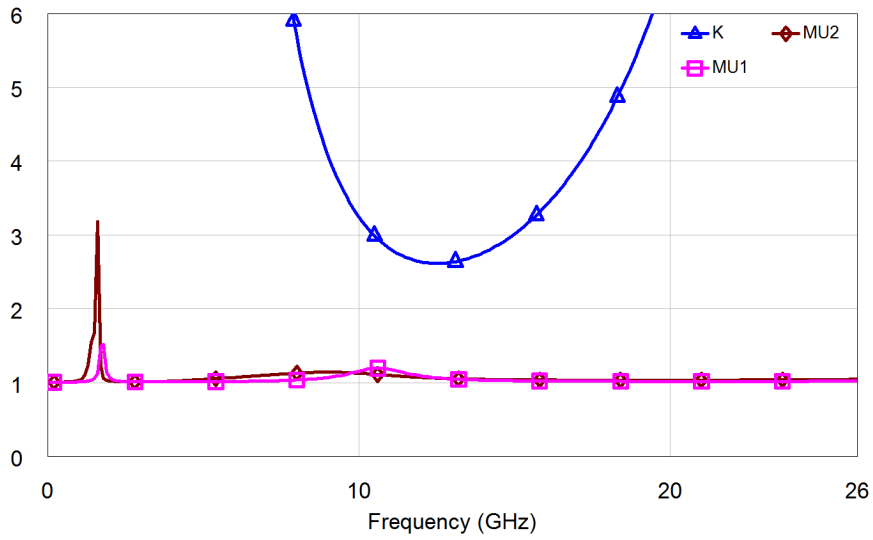
Stability is the key performance in the amplifier design. This amplifier must remain stable at all input impedances and biasing conditions. To ensure these tight system specifications, some precautions must be taken.

First case for the stability is the differential case where the input signal arrives differentially. If the amplifier branches are supplied with the same current, then the small signal model in Figure 3.11 can be obtained.

Due to differential action the source terminals appear as a ground. Current entering in the system forms V_{gs} potential and V_{gs} potential forms I_{ds} current. Some portion of this current goes to load impedance whereas, some of this current goes to the gate by traveling from gate to drain impedance. If conditions are right, then this feedback



(a) First stage stability results



(b) Second stage stability results

Figure 3.10: PA stability results

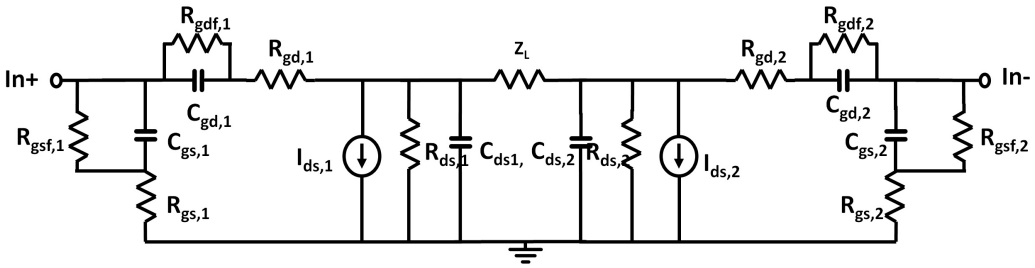


Figure 3.11: Small signal model for differential analysis of differential LNA

can cause oscillations in the transistor. Therefore this feedback must be compensated to ensure stable operation. This feedback loop can be compensated using a shunt feedback from drain to gate of by loading the output or the input of the amplifier.

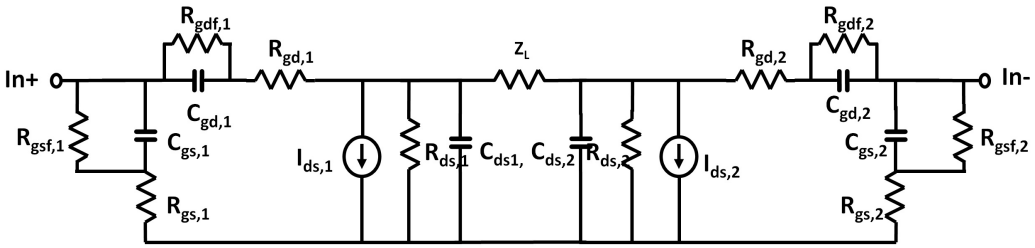


Figure 3.12: Small signal model for common mode analysis of differential LNA

For the common mode operation the source terminal becomes floating as shown in Figure 3.12. Current entering from the gate terminal creates V_{gs} potential and due to the floating source, this current completes the loop by traveling from drain to source impedance. Some part of this current flows to the load impedance and some part of it flows to the gate by the gate to drain impedance. If the feedback capacitance and resistance creates positive feedback conditions, the amplifier can oscillate. This type of stability is referred to as common mode stability [40]. In order to prevent this type of oscillation some type of current degeneration path must be added at the common source terminals. By this way, some of the entering current is dissipated by the degeneration and the current circulating in the amplifier decreases and reduce the chance of oscillation.

In this design, for common mode stabilization, a source resistance of 100 Ω is added with a shunt feedback from output to input is added. By this way unconditional stability with bias stability at every impedance point is ensured as will be shown later.

3.3.2 Effect of Source Degeneration Resistance

Apart from the stability, source degeneration resistance has additional benefits for the differential amplifier design.

DC operating point is mainly determined by the gate to source potential voltage. Source degeneration forms a series series feedback to the input. This creates a linearization effect on the DC characteristics in the transistor. A GaN HEMT's current in saturation regime can be expressed as [41]:

$$I_{d,sat} = \beta\mu F_s(\sqrt{(V_{gs} - V_{th})^2 + F_s^2L^2} - F_sL) \tag{3.5}$$

where β, μ are constants related to mobility and size of the transistor.
F_s is the velocity saturation in the HEMT device.
L is the channel length of the device.

This square-law characteristics linearizes if source degeneration resistance is used. With source degeneration resistance R, this equation becomes:

$$I_{d,sat} = \beta\mu F_s(\sqrt{(V_g - I_{d,sat}.R - V_{th})^2 + F_s^2L^2} - F_sL) \tag{3.6}$$

Resistance R creates a current feedback in the transistor, which means a squared current is also produced as the result of feedback. Cancellation of squared currents linearizes transistor characteristics.

Suppose without degeneration, 1 mV change in the gate potential causes 1 mA rise in the current. When a source degeneration added, at the same conditions 1 mV increase in gate potential causes a current change less than 1 mA depending on the amount of resistance. This allows a higher resolution in controlling the amplifier's current from gate voltage. Moreover, the resistance enables the total current to be a function of the DC gate biases of the transistor which decreases number of supplies that must be used in the design.

Figure 3.13 gives the schematic view of the LNA. For stability reasons a shunt feedback of 180 Ω and 6 pF is used. As for the source degeneration resistance, 100 Ω is used.

The layout of the differential amplifier is given in Figure 3.14. In the layout, "VGLNA1"

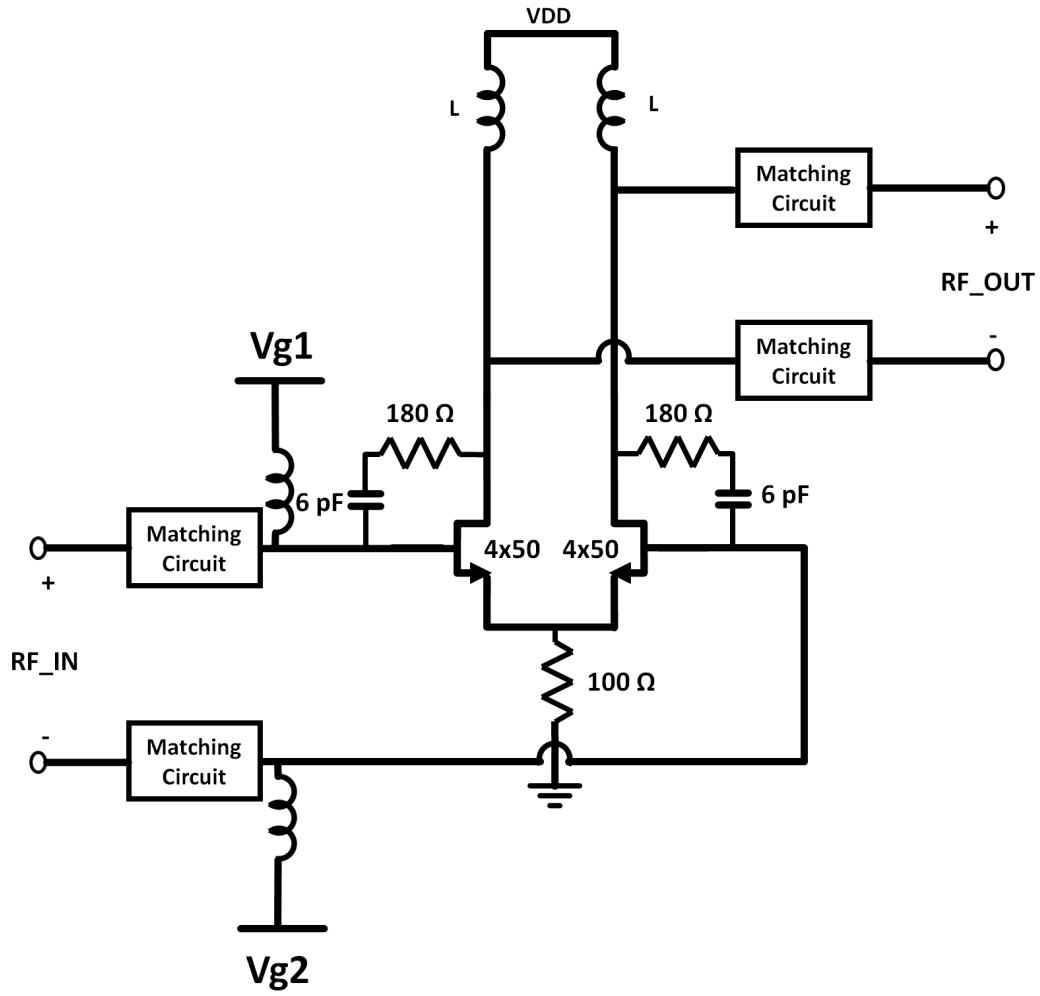


Figure 3.13: LNA schematic view

and "VGLNA2" represents gate connections of the transistor. "VDDLNA1" and "VDDLNA2" represents drain connections of the transistor. In order to avoid process variations at the source terminal, source resistors are divided into four parts and connected as seen in Figure 3.14.

3.3.3 Simulation Results

All simulations regarding the differential amplifier are performed using AWR software. Simulation results are divided into two cases. At the first case, the input signal is differential and second case considers where the input signal enters as common mode.

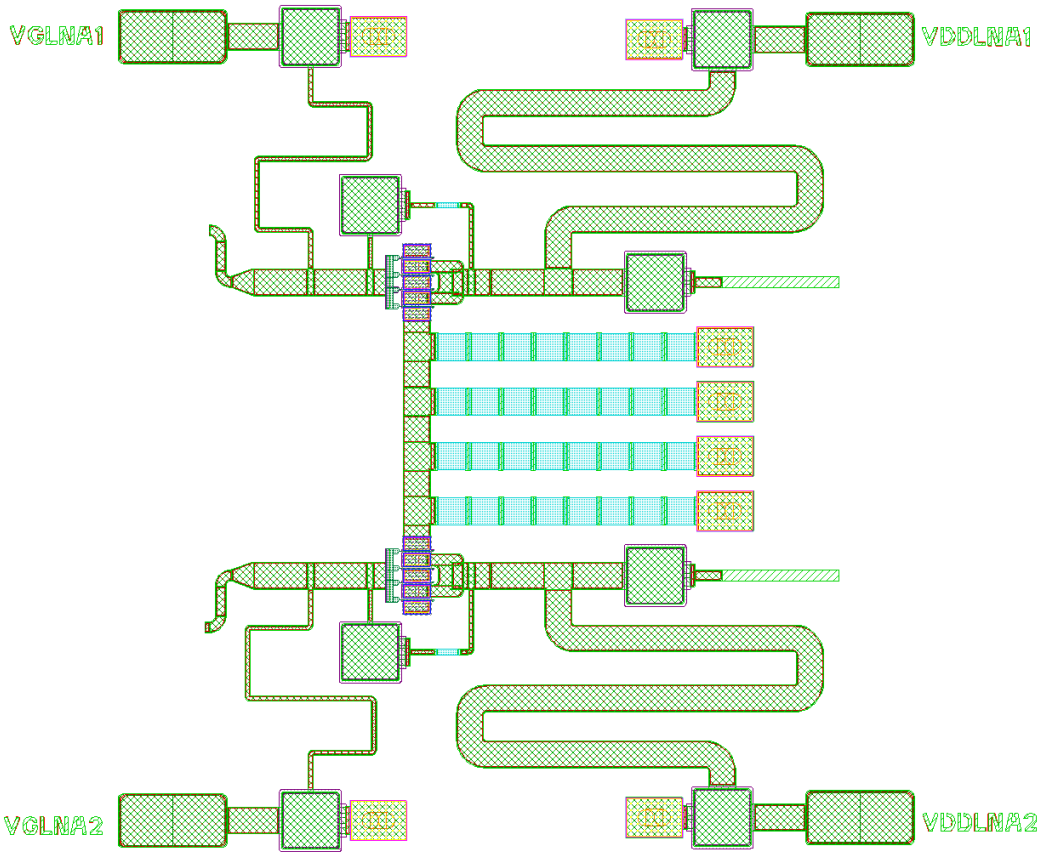


Figure 3.14: Differential LNA layout

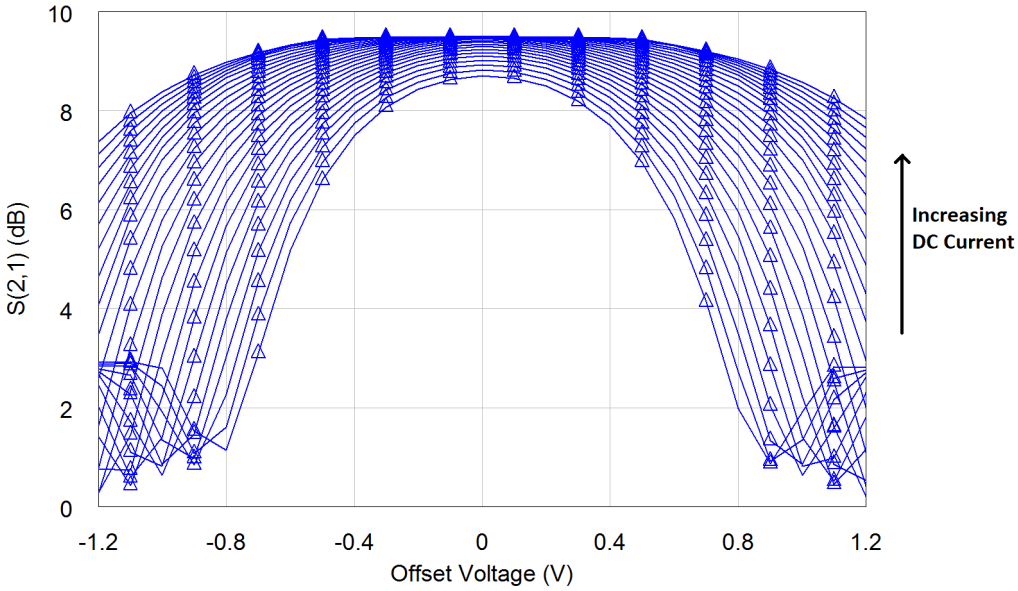


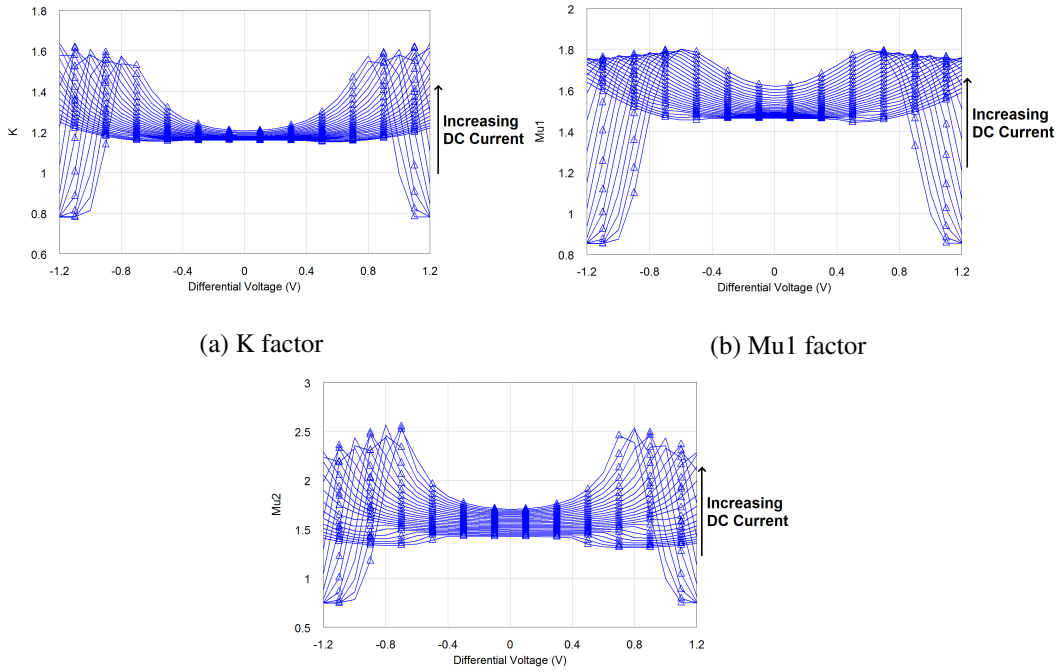
Figure 3.15: Differential amplifier gain with respect to offset voltage

Figure 3.15 shows the gain of the differential amplifier with respect to the voltage offset between bias points and varying common mode voltage values. Each blue lines

show different levels of common bias voltages. When there is no offset between bias points (both transistors have the same DC operating point) gain attains its maximum value of 9.6 dB. As the voltage offset increases gain starts to drop from its maximum value. As the common bias voltage increase, drop in the gain with respect to offset voltage decreases up to 6 dB.

For stability, differential stability parameters are given in Figure 3.16 at 10 GHz only and in Figure 3.17 as a 3D plot with respect to offset voltage and frequency. Both figures show that after the offset voltage goes beyond 0.9 V, the amplifier becomes unstable. Further compensation of the amplifier beyond this point would result in a degradation of the performance in terms of gain and noise figure.

Common mode stability for a single frequency is given in Figure 3.18 and Figure 3.19 gives stability results with respect to both frequency and offset voltage. All the stability parameters are well above 1 which means common mode PA signals wouldn't create any common mode oscillation in differential amplifier.

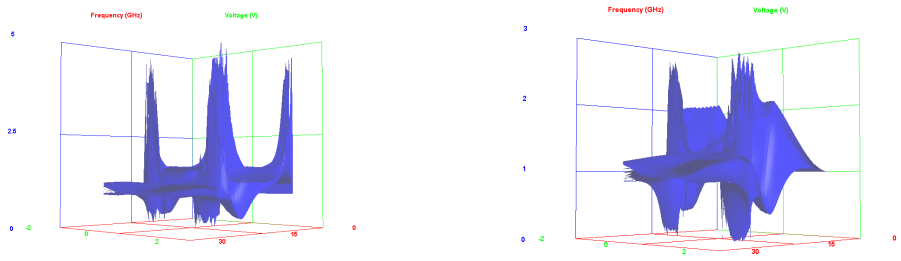


(a) K factor

(b) Mu1 factor

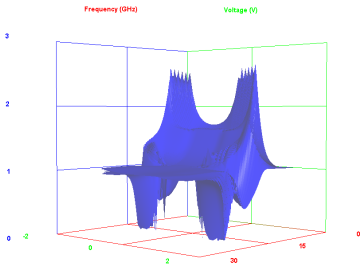
(c) Mu2 factor

Figure 3.16: Differential mode LNA stability at single frequency



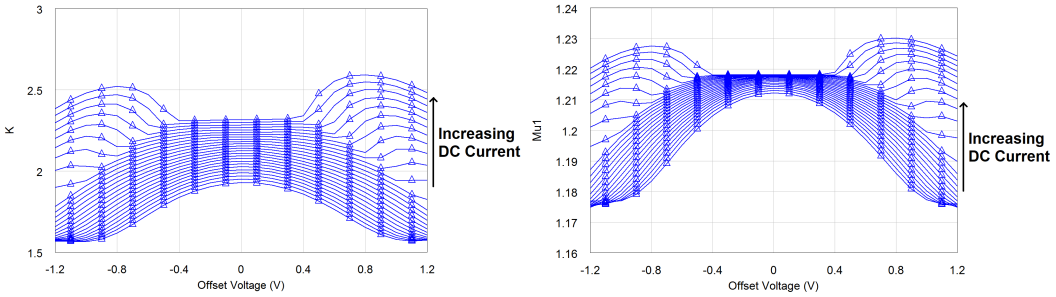
(a) K factor

(b) Mu1 factor



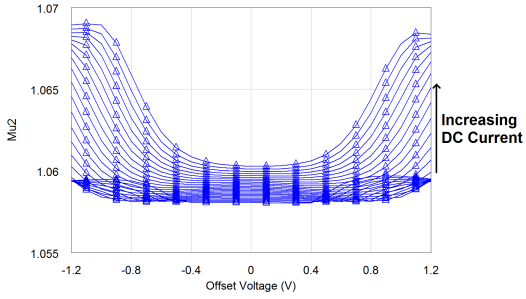
(c) Mu2 factor

Figure 3.17: Differential mode LNA stability with respect to offset voltage and frequency



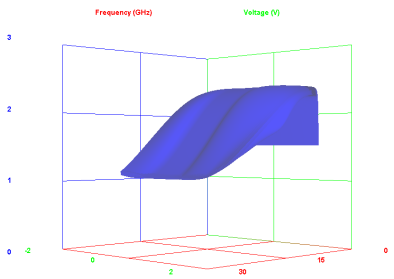
(a) K factor

(b) Mu1 factor

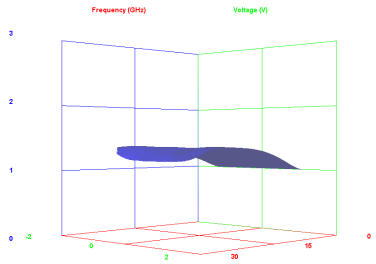


(c) Mu2 factor

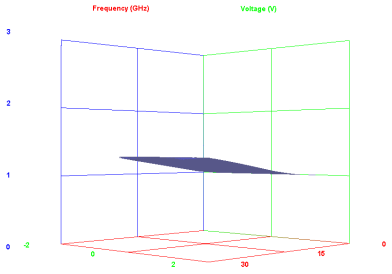
Figure 3.18: Common mode LNA stability at single frequency



(a) K factor



(b) Mu1 factor



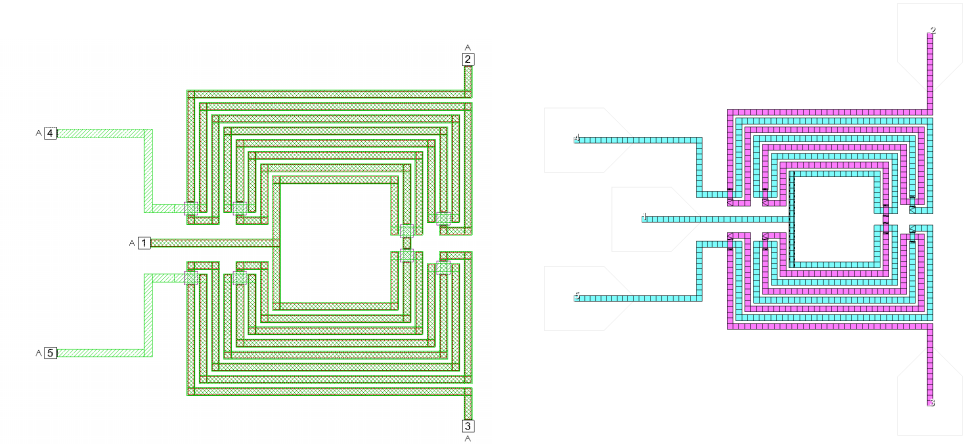
(c) Mu2 factor

Figure 3.19: Common mode LNA stability with respect to offset voltage and frequency

3.4 Balun Design

As discussed before, a balun is a hybrid transformer that has a 1:1 ratio between its primary and secondary coils. In order to implement it in MMIC technology, a wound up transformer layout is used. It consists of two parallel lines, where one for primary coil and the second one for secondary coil, are rounded in a way to maximize the coupling and minimize the area.

Formed balun layout is given in Figure 3.20a. Due to the two metal lines provided by the MMIC process, the balun cannot be realized in a traditional way where coils are formed in different metal layers and center tap is connected by using the third metal line. Therefore, center tap connection divides the connection between coil lines and forces them to rotate to the opposite direction. These rotations introduce extra loss due to impedance mismatches and edge effects. Signal flow can be seen in Figure 3.20b for easy analysis.



(a) Layout of balun

(b) EM Mesh and connection mapping for balun

Figure 3.20: Balun layout and connection

Both coil lines are formed with a thick line to minimize insertion loss. Crossings between coils are made with airbridge structure. Characteristics are obtained with a 2D EM analysis by AXIEM and optimized using EM simulation results.

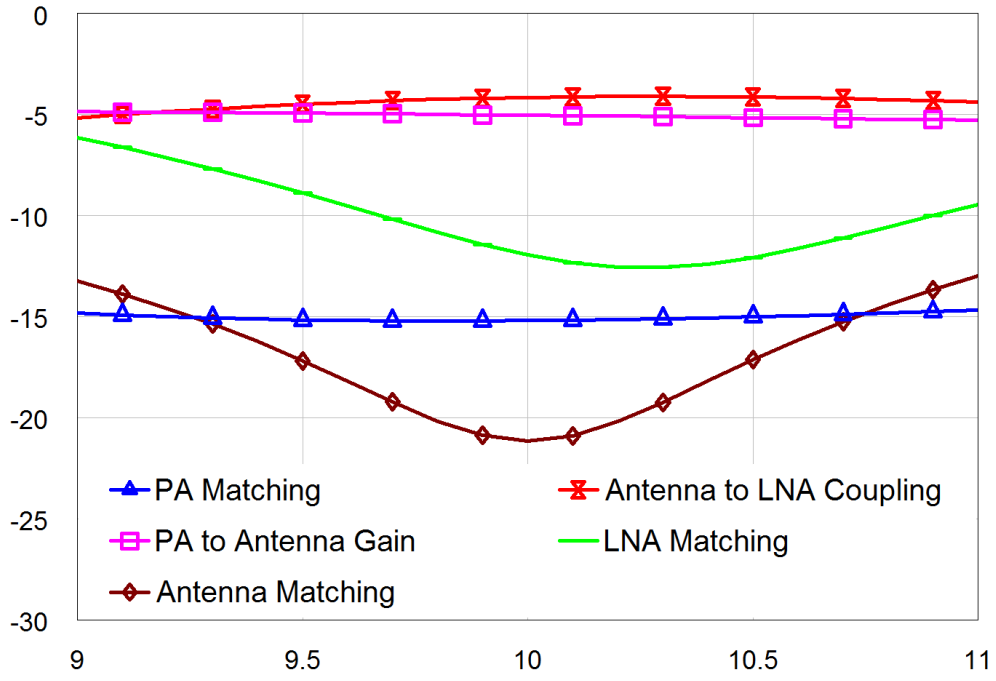


Figure 3.21: Balun S parameter results

Simulations are done assuming all ports are terminated with their respective ideal balun port impedances and given in Figure 3.21. Results indicate that loss from PA to

Antenna is 5 dB at 10 GHz. This 5 dB loss consists of the inherent 3 dB loss due to the power division of PA signal to balancing load and the antenna. Remaining loss is due to the conductor and dielectric material. From antenna to LNA, coupling is found to be 4.2 dB. Reflections from all ports are well below -10 dB which shows that all ports of the balun are matched.

3.5 Balancing Load Design

In order to increase the impedance range requirement, a tunable resistive load is constructed. This balancing load is formed by using a transistor and biased in a way to show only a real impedance.

When a transistor is biased in the saturation region, it presents an output impedance from its drain. However, this output impedance is a complex impedance. By adding lumped elements to the drain, imaginary part is cancelled and real part is furthermore increased by adding additional series resistance to the output. As this part won't be used for amplification, addition of resistance doesn't create any disturbance at the operation. Figure 3.22 shows a schematic view of the balancing load. Here L nad C denotes choke inductor and decoupling capacitor respectively. Other remaining capacitance and resistances are used to generate a real load at the frequency of interest.

One important factor is that, the transistor is still an active device and must be stabilized because it can still form an oscillation if the feedback is not suppressed. Stability is analyzed as if the balancing load is a two terminal device. In order to stabilize the structure, resistances are added to the gate and drain of the structure unlike the shunt feedback used in differential amplifier design. Layout of the design is given at Figure 3.23. "VG3" is the gate connection of the transistor and "VDD3" is the drain terminal of transistor. RF part is DC coupled to the balun. RF choke inductor is placed at the drain and gate terminals to eliminate the parasitic effects of the DC ports.

Simulation results in Figure 3.24 show that the balancing load has a real impedance range between 31 Ω to 68 Ω where imaginary part is changing between -j5 Ω to +j4 Ω. Balancing Load provides an 50 Ω impedance with -j2.5 Ω imaginary impedance

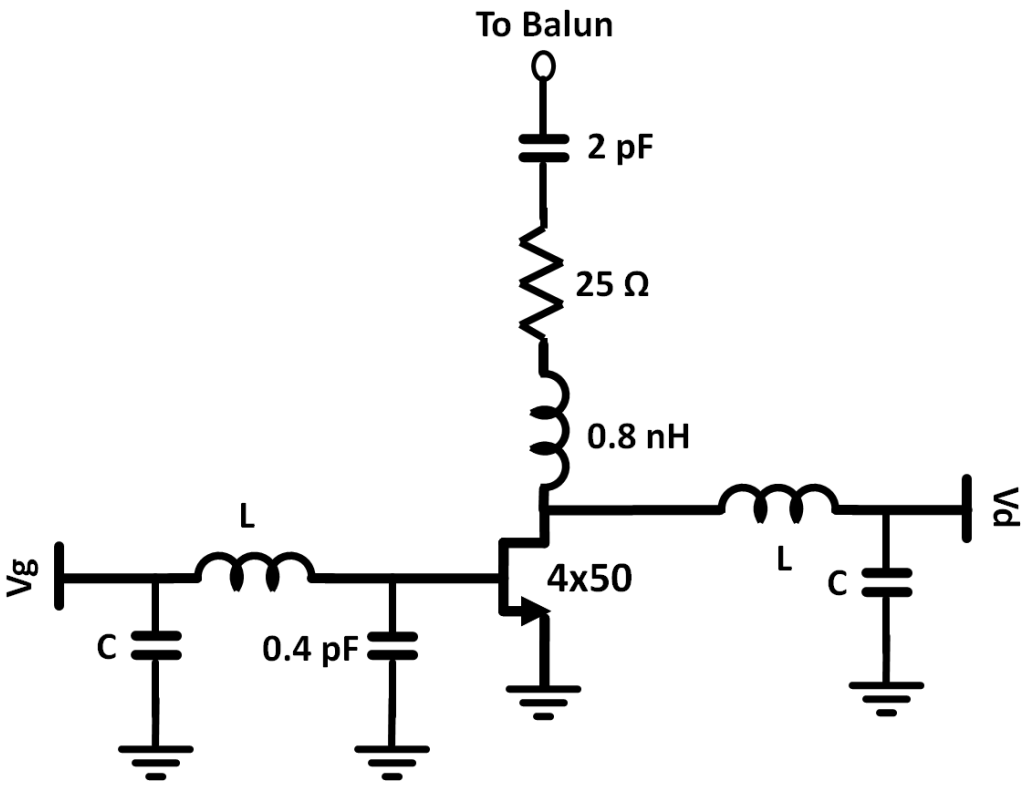


Figure 3.22: Balancing load schematic

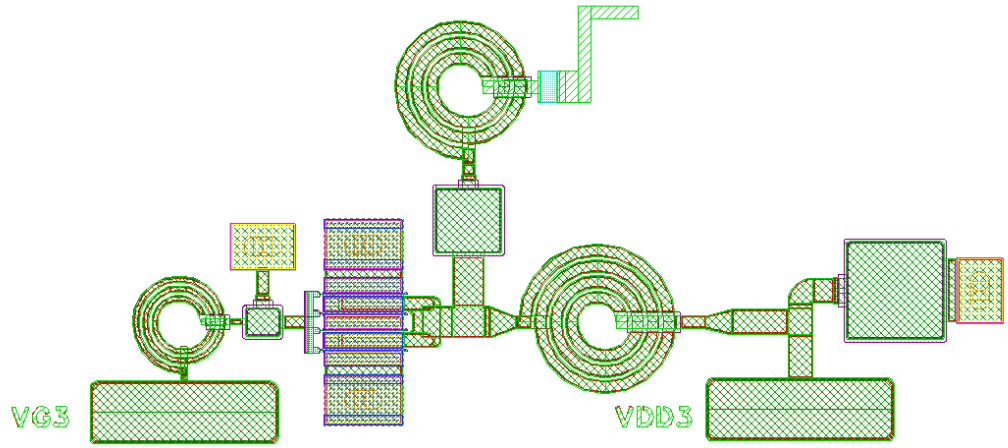


Figure 3.23: Balancing load layout

at gate bias voltage of -2.32 V.

Stability results are provided at Figure 3.25. Since stability indicators are larger than 1, it is safe to use this device as a balancing load.

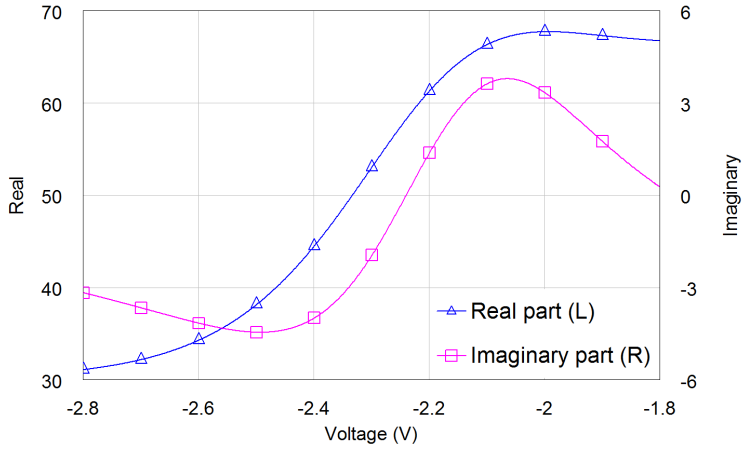


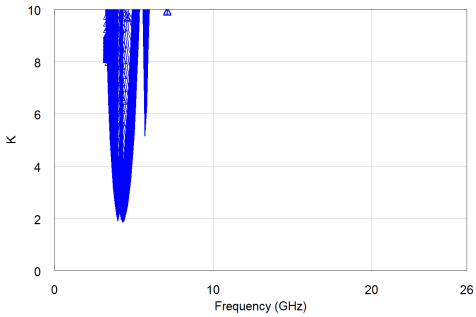
Figure 3.24: Balancing load impedance with respect to gate voltage

3.6 System Simulation

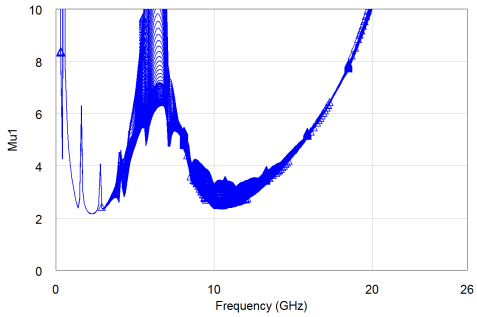
The complete system layout is given in Figure 3.26. As stated before this IC contains all of the necessary components required for in band full duplex transceiver with SIC. Differential LNA output is converted into balanced output with the help of the same balun designed for the EBD to ease measurements.

System simulations are done by using optimization algorithms provided in the AWR. Microwave simulations are performed using harmonic balance. As the transmitted power cannot be considered as small signal, harmonic balance is an ideal way to simulate the nonlinear effects of this system. For finding the maximum SIC level, the gate biases of balancing load and differential amplifier are adjusted manually up to 25 dB SIC by using tuning provided in AWR. After 25 dB of SIC level is reached, then gradient optimization is used to further increase SIC to 40 dB at 50 MHz bandwidth by adjusting same voltage sources. Since voltage biases are adjusted up to some point, gradient optimization finds the required solution in a few iterations. Therefore, it is fast and convenient way of optimization.

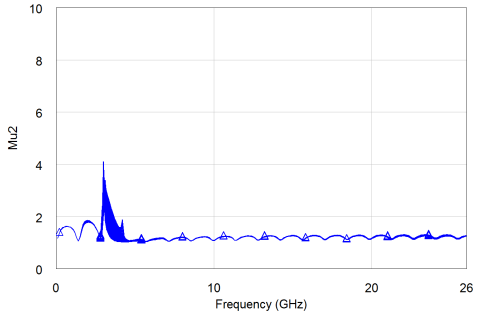
System simulation results showing antenna power and LNA output before and after tuning are given in Figure 3.27 - 3.31. The difference between the antenna power and output power of the LNA gives the SIC amount for the designed system. For impedances ranging from 50 Ω and points on Γ=0.3 circle are used to show that SIC



(a) K factor



(b) Mu1 factor



(c) Mu2 factor

Figure 3.25: Balancing load stability with respect frequency at different bias voltages

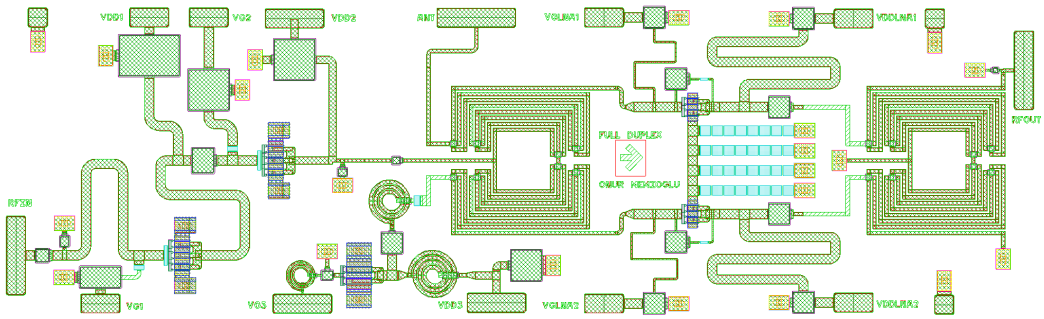


Figure 3.26: Fully integrated MMIC layout

occurs within these specified points. A table of the simulation results is also provided in table 3.1 providing LNA gain, branch currents and output power.

Antenna Imp. (Ω)	Transmitted Power (dBm)	Receiver Gain (dB)	SIC (dB)	LNA cur. 1 (mA)	LNA cur. 2 (mA)	Bal Load Bias (V)
50.0	24.87	9.08	51.31	23.5	43.5	-2.37
30.0-j14.0	26.04	8.25	40.58	12.6	68.0	-2.82
30.0+j14.0	24.57	9.40	45.03	39.3	52.5	-2.92
68.3+j31.9	24.10	9.13	58.55	41.3	25.2	-2.21
68.3-j31.9	26.49	9.28	44.24	51.4	111.0	-1.98

Table 3.1: Simulation results of EBD system

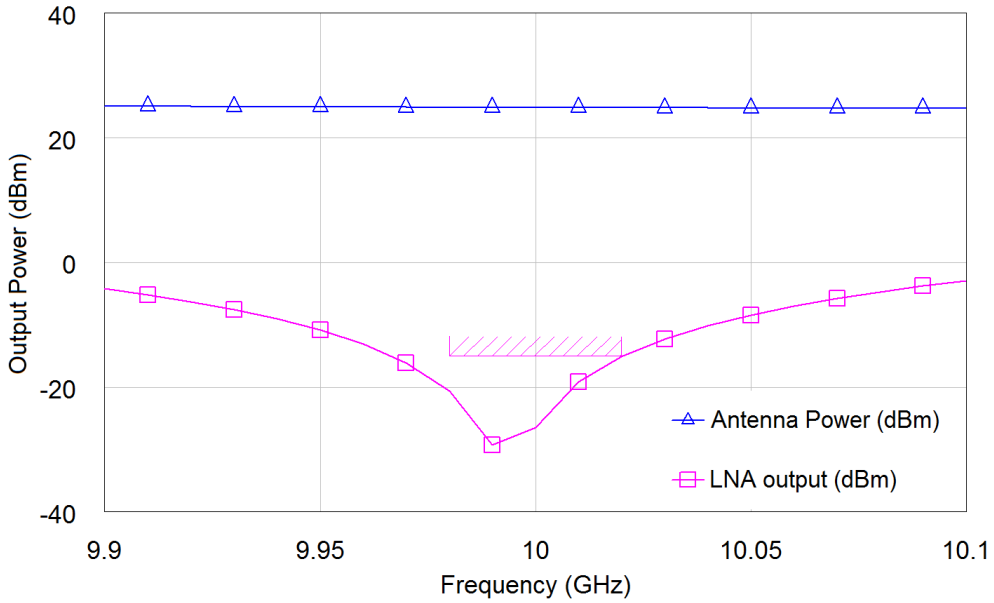
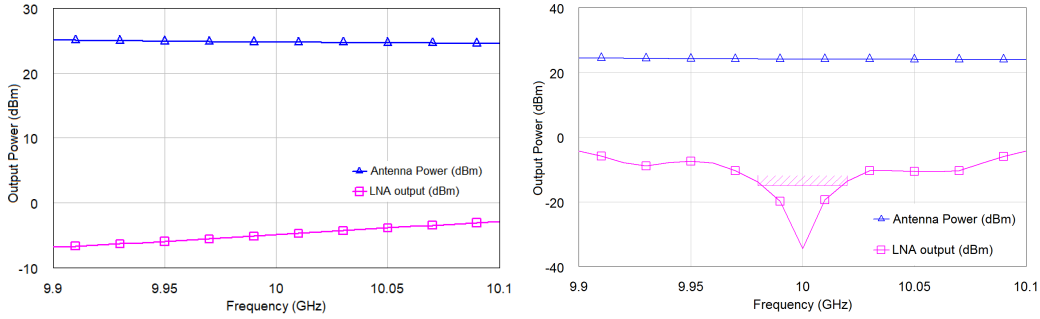
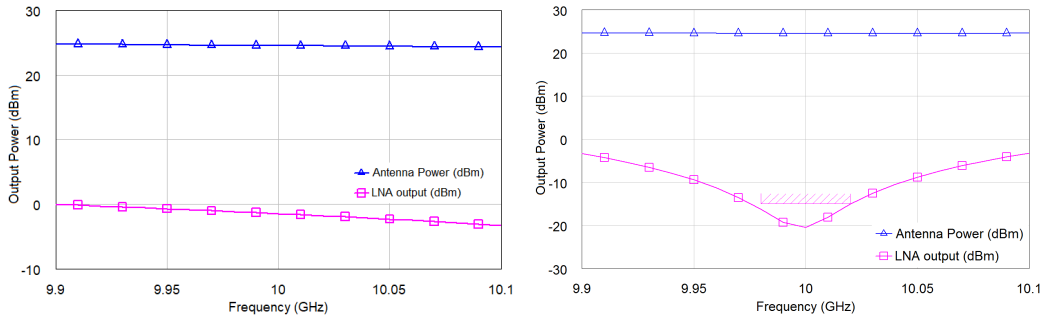


Figure 3.27: Antenna (blue) power and LNA output (purple) before and after tuning for 50 Ω load



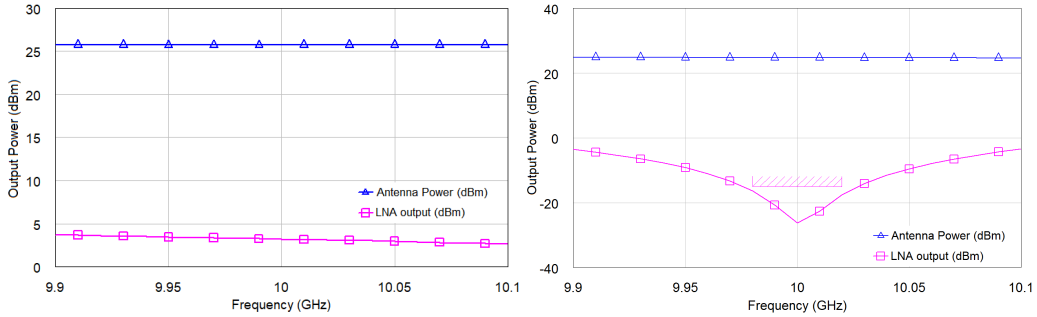
(a) Before tuning (b) After tuning

Figure 3.28: Antenna (blue) power and LNA output (purple) before and after tuning for Γ=(0.3,45^{o}) load impedance



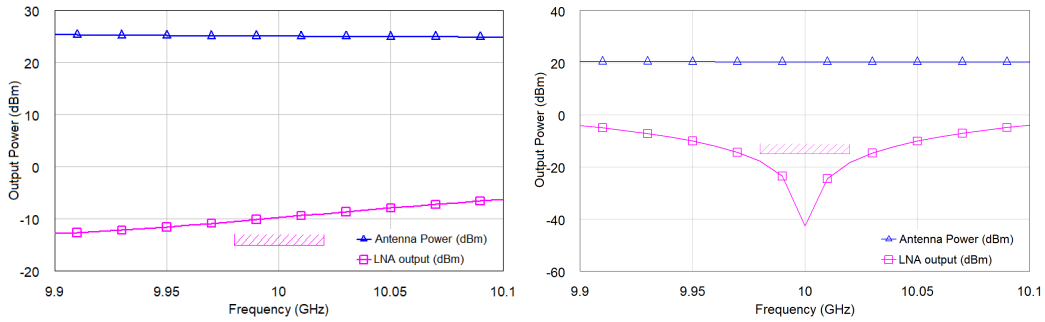
(a) Before tuning (b) After tuning

Figure 3.29: Antenna (blue) power and LNA output (purple) before and after tuning for Γ=(0.3,135°) load impedance



(a) Before tuning (b) After tuning

Figure 3.30: Antenna (blue) power and LNA output (purple) before and after tuning for Γ=(0.3,225°) load impedance



(a) Before tuning (b) After tuning

Figure 3.31: Antenna (blue) power and LNA output (purple) before and after tuning for Γ=(0.3,315°) load impedance

CHAPTER 4

MEASUREMENT AND EVALUATION

Previous chapters explain the theoretical background of operation. In the third chapter, the circuit design along with its simulation results are provided. System simulation results verify that the system is operational. However, in order to prove functionality, the designed IC is manufactured and tested. Figure 4.1 shows the photo of the manufactured IC.

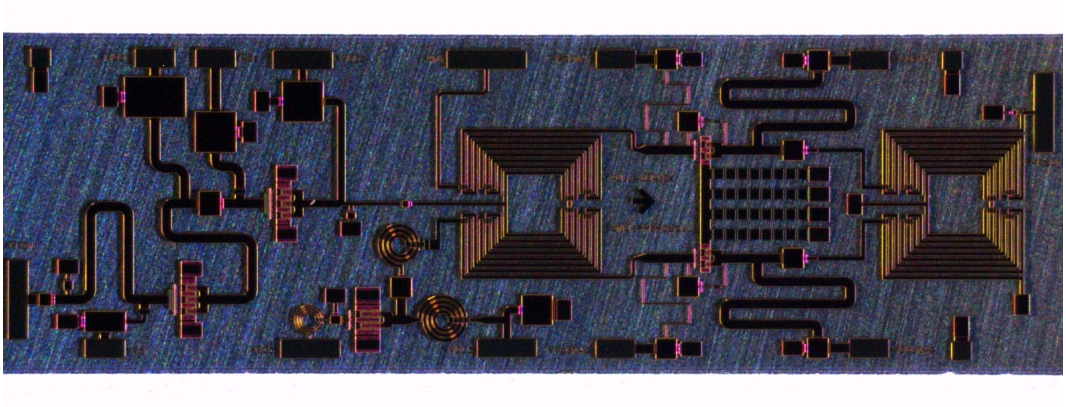


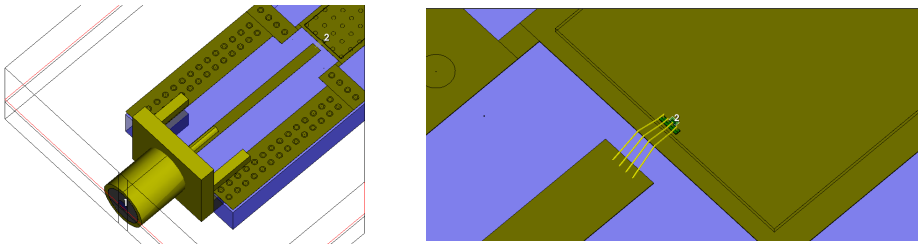
Figure 4.1: Die photo of the manufactured IC. Left side transmitter input, right side LNA output, middle side antenna output

In this chapter, test setup and test results are presented to show that the system operates and produces the required output. At first, a test PCB for testing is presented. Then general test setup for verification is discussed. Finally, test results are provided and discussion on the results is presented along with a future work to be done. This part also sums up all the work done in this thesis.

4.1 Test PCB

Test PCB is required to transfer IC's supply voltages, RF inputs and outputs to voltage supplies and measurement devices. As the RF frequency is at 10 GHz, the substrate and PCB thickness is chosen accordingly to ensure that the signal can be carried with a minimum attenuation. 20 mil thick ROGERS 4003C material is used, which has a dielectric constant of 3.38 and a loss tangent factor of 0.0027. With the given substrate thickness, a microstrip line with a width of 1.1 mm corresponds to a 50 Ω transmission line.

This IC is not placed inside a commercial package due to non standard size. A custom package could have been designed however to avoid costs of custom manufacturing, a chip on board scheme is used. In this scheme, MMIC are directly placed on the PCB with an electrically and thermally conductive epoxy. DC and RF signal connections from the IC to the PCB are done using 1 mil thick gold wirebonds.

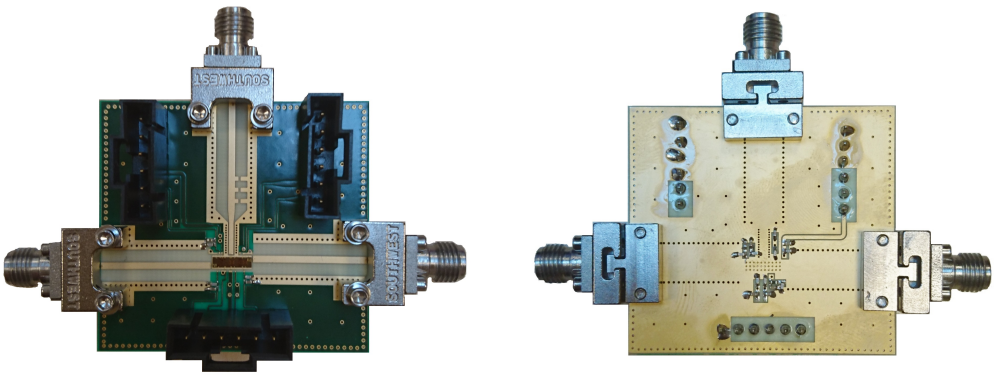


(a) EM view zoomed out (b) EM view zoomed in

Figure 4.2: 3D EM setup for the PCB and MMIC interface

Wirebonds cause degradation in the RF signal performance. These thin lines produce inductances rather than a transmission line which deviates input impedance from 50 Ω. To account for these effects, all the simulations are done with the test PCB to ensure the best performance from the system. Figure 4.2 shows the 3D view of the simulated PCB-MMIC interface. To minimize inductance on the RF lines, each RF connection uses 4 wirebonds in parallel to reduce the inductance. Moreover, the RF pads on the PCB are placed at the closest allowed proximity with the RF pads on the IC to minimize the length of these lines. Additional matching circuits are placed into the IC to take into the account of the wirebond effect.

Fig 4.3 shows the photo of the manufactured and assembled PCB. Antenna terminal



(a) PCB top side

(b) PCB bottom side

Figure 4.3: Photo of assembled pcb

begins as a coplanar line at the IC part and converted into a microstrip line at the end side of the PCB. This choice of transmission line is used in order to place decoupling capacitors of LNA and PA much closer to their respective pads. It is a two layered PCB with only top and bottom layers used for routing and component placement.

PA input and LNA output RF lines do not have any SMD components placed on them. Only transmission line for antenna has some space holders for component placement to create a matching circuit. This matching circuit is used to convert 50 Ω load into a desired antenna impedance. For each supply rails, two shunt capacitors with 1 nF and 100 nF capacitance are placed to serve as decoupling capacitors. These capacitors are placed at the closest place to the pads.

As RF connectors, Southwest 2.92 mm end launch connector is used for board to coaxial interconnection. This connection has a low VSWR less than 1.1 with loss at 0.8 dB at the frequency of interest.

4.2 Measurement Setup

System verification requires three types of measurement setups. First measurement is to measure the transmitted power at the antenna terminal. Second measurement is the verification of the SIC at the receiver. Final measurement is the verification of the receiver gain.

In order to generate different load impedances, three shunt place holders on the antenna transmission line are placed on the PCB. These place holders are replaced by different capacitances and inductances to generate a desired load impedance.

Firstly SIC is verified by forming the test setup in Figure 4.4. In this test setup, a signal generator is connected to the transmitter to provide RF input and a spectrum analyzer is connected at the output of the receiver to measure the output power. At this configuration, a tunable load is connected to emulate as an antenna of varying impedance. By subtracting the power at the antenna terminal with the power at the receiver, SIC can be calculated.

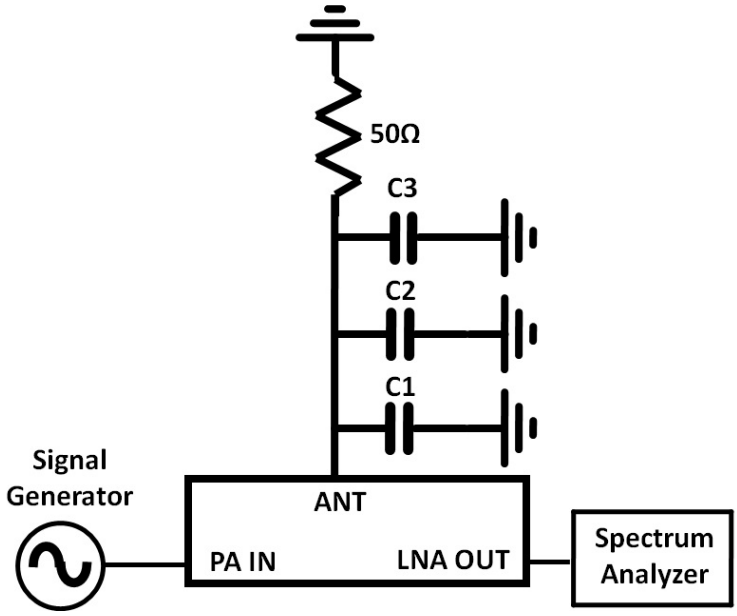


Figure 4.4: Test setup for measuring SIC

Controllable gate voltages allow tuning of the receiver to obtain the highest SIC possible. This search is done manually by adjusting the gate voltages. When the lowest receiver power is reached, the receiver would obtain its highest SIC amount. Bias currents of the LNA and balancing load gate voltage would be recorded to be used at the next verification setups.

Second measurement is to determine the power at the antenna terminal. This power is used to calculate SIC. In order to measure this power, a test setup in Figure 4.5 is formed. In this setup, spectrum analyzer is connected at the output of the antenna terminal and LNA is terminated with a fixed load. LNA bias currents and balancing

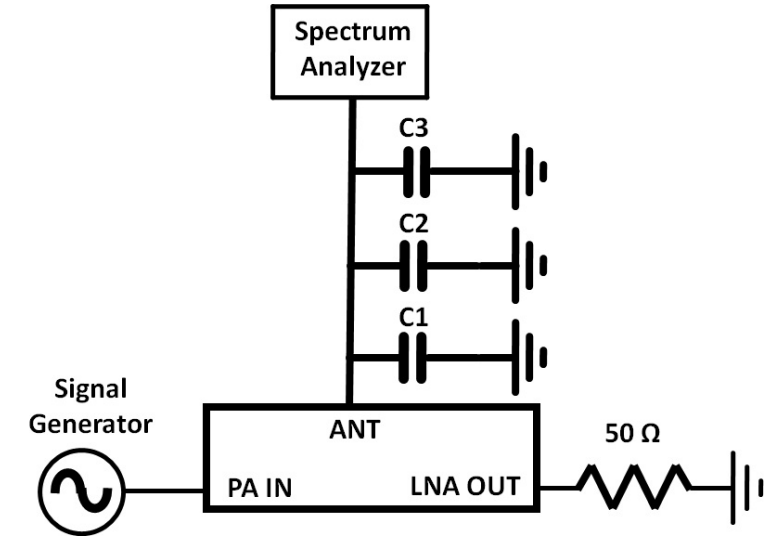


Figure 4.5: Test setup for measuring power output at antenna

load bias are set from the highest SIC conditions in the first test setup.

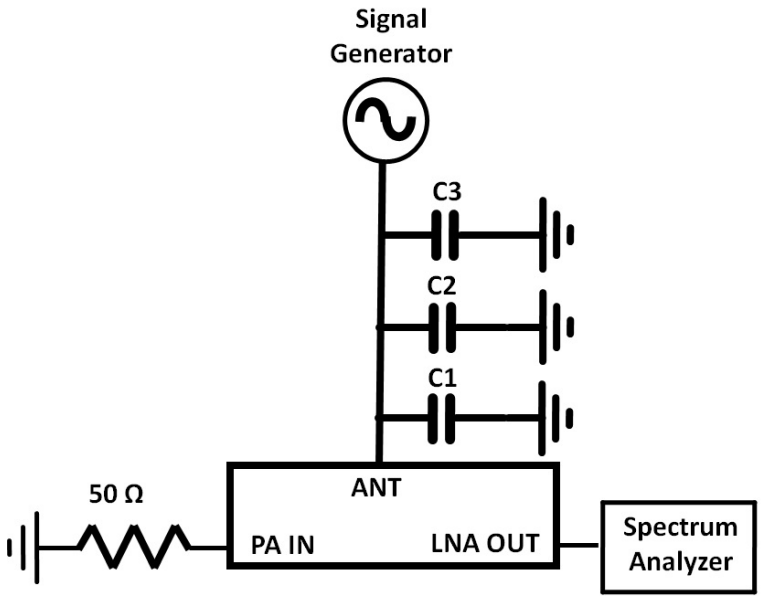


Figure 4.6: Test setup for measuring LNA gain

Third measurement setup is used to determine LNA gain where highest SIC is obtained. This measurement setup is formed by connecting the signal generator at the antenna terminal with the variable load and connecting the spectrum analyzer at the output of LNA terminal. This time the PA input is terminated with 50 Ω. By setting the LNA branch currents and balancing load voltages, we can obtain the condition where highest SIC is obtained and hence determine the LNA gain from antenna ter-

minal when SIC is at maximum.

4.3 Measurement Results

During initial power on sequence, when the PA and balancing load is biased with simulated DC bias point, an oscillation occurred in the PA side. When the balancing load and PA are turned on separately, there were no oscillations. However, when they are turned on at the same time a small signal oscillation starts up.

In order to quickly avoid this type of oscillation, PA bias conditions are changed. Drain voltage is reduced to 10 V while current density remains intact. At this bias voltage, PA remains stable for all balancing load bias conditions.

The reduction of drain voltage resulted in a power loss around 10 dB with power output at 22 dBm at 50 Ω antenna and LNA loads. PA simulation results with new bias points are given in Figure 4.7, which also suggests a power drop at the specified operation. However, with low power antenna power, still in band full duplex operation can be verified.

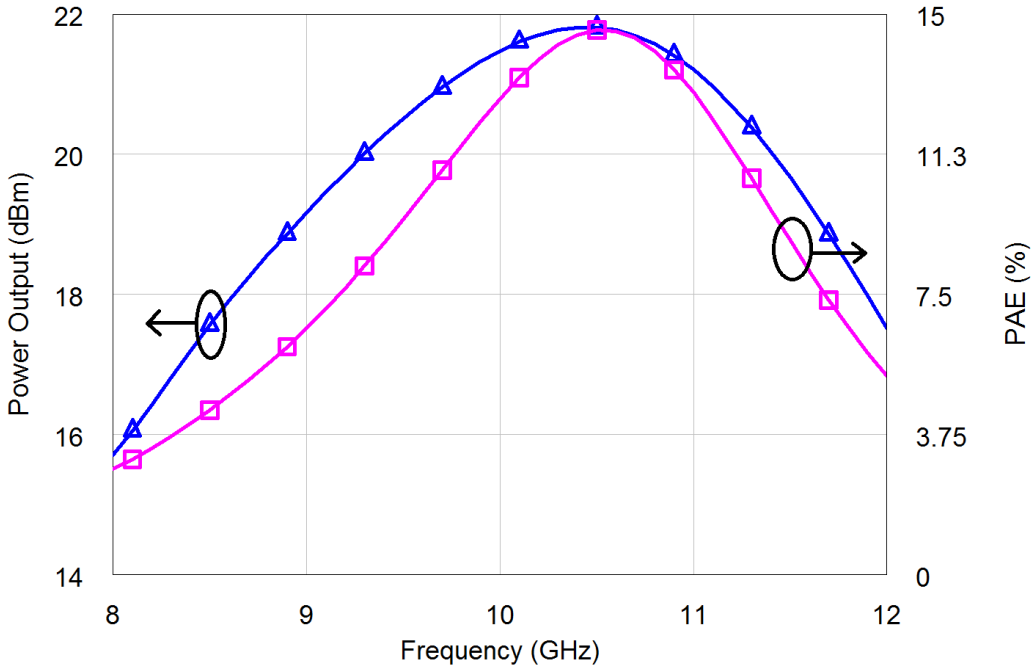


Figure 4.7: Power output and PAE of PA under 10V drain bias

System results with PA power, LNA gain, SIC levels and branch currents are provided in table 4.1. Moreover spectrum analyzer outputs of transmitter signal and self-interference signal are provided at different antenna impedances in Figure 4.8-4.12.

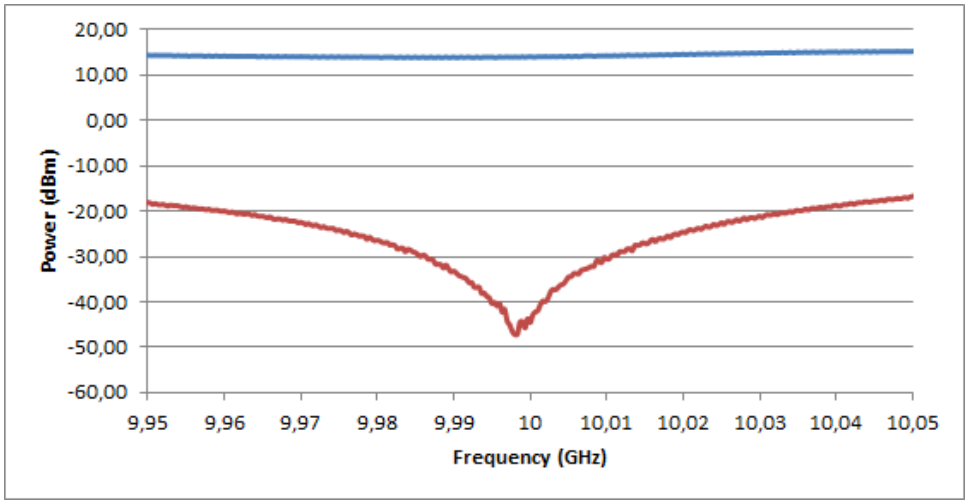


Figure 4.8: Transmitted (blue) and self-interference (red) power at 50 Ω load

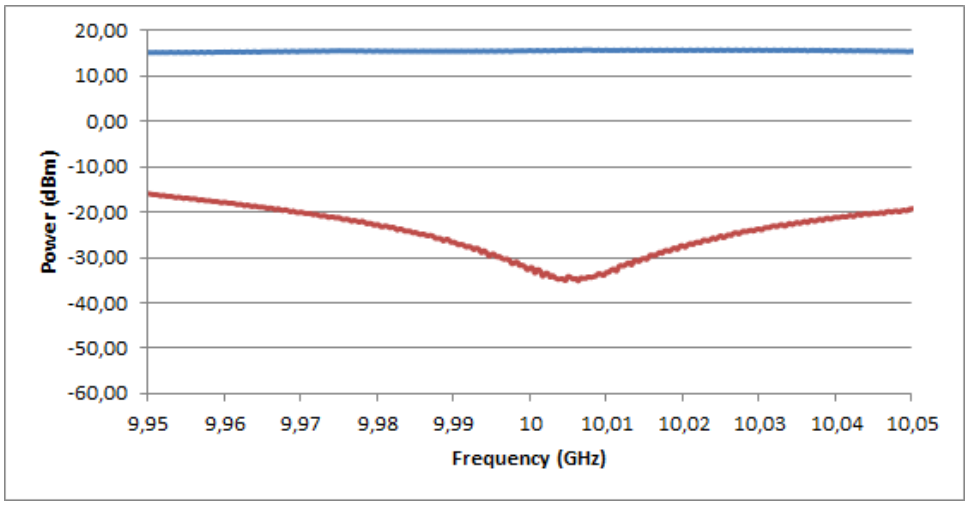


Figure 4.9: Transmitted (blue) and self-interference (red) power at 46-j29 Ω load

Results indicate that a maximum of 58 dB of SIC can be achieved with careful adjustment of biases. Branch currents are given in the table 4.1. Total current varies between 20 mA to 25 mA but providing more than 40 dB of SIC in many impedance points. In 100 MHz bandwidth at least 40 dB of SIC is obtained.

There are discrepencies between simulation results and measurement results. Especially, there are huge differences at LNA bias currents between simulation and measurement. At simulation level, total DC current go beyond 160 mA to provide 40 dB

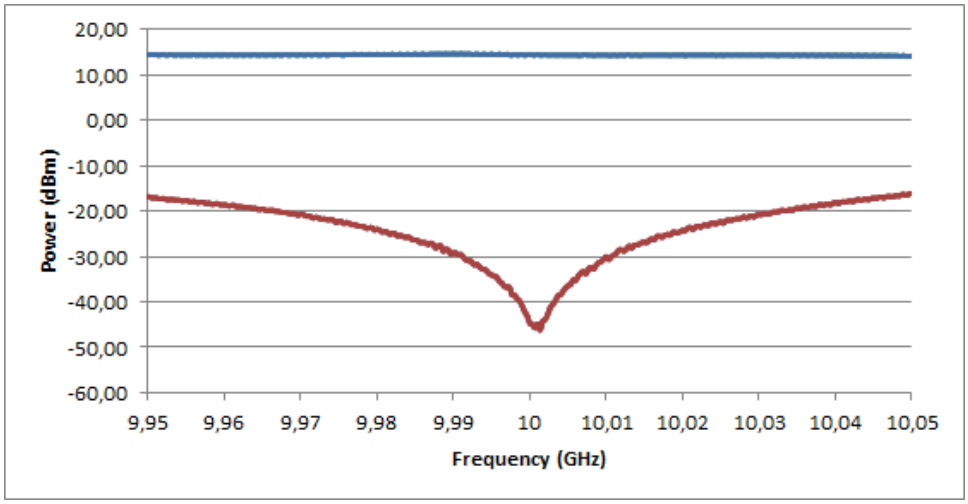


Figure 4.10: Transmitted (blue) and self-interference (red) power at 30.6-j10.5 Ω load

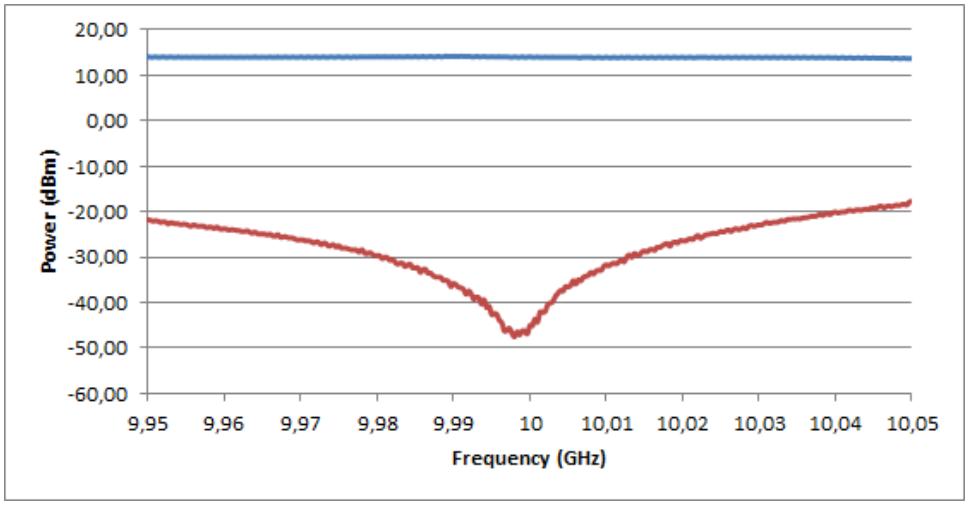


Figure 4.11: Transmitted (blue) and self-interference (red) power at 34.1+j9.4 Ω load

Table 4.1: Measurement results of EBD system at 10 GHz

Antenna Imp. (Ω)	Transmitted Power (dBm)	Receiver Gain (dB)	SIC (dB)	LNA cur. 1 (mA)	LNA cur. 2 (mA)	Bal Load Bias (V)
50.0	14.09	8.19	58.65	12.4	12.2	-2.35
46.0-j29.0	14.56	8.25	46.87	14.8	11.3	-2.33
30.6-j10.5	14.07	8.15	58.80	15.2	9.6	-2.65
34.1+j9.4	13.66	7.63	58.71	4.9	15.6	-2.53
54.5+j20.8	15.56	7.26	54.71	3.2	17.1	-2.48

SIC at some cases whereas in real domain total currents vary between 20 to 25 mA. The process used at the design is under development by WIN Semiconductors. Dur-

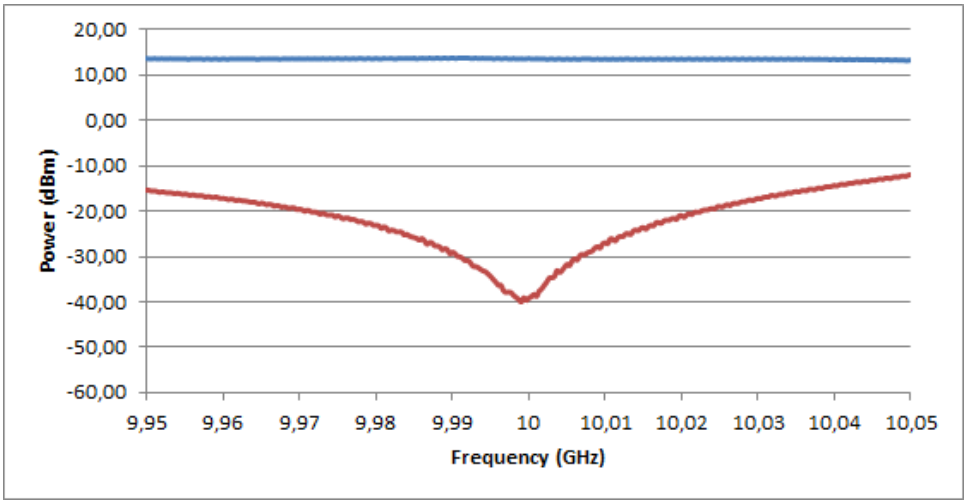


Figure 4.12: Transmitted (blue) and self-interference (red) power at 54.5+j20.8 Ω load

ing the design process, fab released new transistor structures and layouts along with their s-parameters. However non-linear model and DC characteristics are still under development. Therefore, poorly DC modeled transistors can cause the discrepancies in the large current differences in the simulation domain.

4.4 Comparision with Other State of Art

In literature there are a number examples of EBD systems that use a kind of balancing load to match the impedance at the matching terminal. However, the balancing method presented in this work is novel and achieves excellent control of the suppression achieving more than 40 dB of suppression in a large bandwidth.

All of the examples on the literature are implemented in CMOS/BiCMOS processes of various gate length. This thesis is implemented on a GaN process which is another novelty of the design.

Table 4.2 gives a comparison with other state of work. In terms of SIC and bandwidth, this work provides an adequate response when compared to others.

Table 4.2: Comparison with other state of work

	Center Frequency (GHz)	SI Suppression (dB)	SI bandwidth (GHz)	Ant. VSWR	Receiver Topology	Technology
[23]	2.15	50	0.3	1.5:1	Single Ended	0.18 μu SOI
[25]	1.875	40	0.036	N/A	Single Ended	0.18 μu SOI
[27]	2	45	0.1	N/A	Fully Diff	28 nm CMOS
[29]	120	30	14	N/A	Fully Diff.	40nm CMOS
[30]	1.8	45	0.2	N/A	Fully Diff.	65 nm CMOS
[31]	2	40	0.5	N/A	Fully Diff.	90 nm CMOS
[33]	1.9	40	0.16	N/A	Fully Diff.	0.18 μm CMOS
[34]	1.9	45	0.145	1.4:1	N/A	GaAs pHEMT
[35]	30	45	1	N/A	Single Ended	0.25μm SiGe BiCMOS
This Work	10	40	0.1	2.0:1	Fully Diff.	0.25μm GaN on SiC

CHAPTER 5

CONCLUSION AND FUTURE WORK

In this thesis, an MMIC enabling in band full duplex communication system is designed utilizing an EBD. This MMIC is designed in a commercial 0.25 μm GaN on SiC process. The main motivation of this thesis is to present a novel architecture in the balancing problem of an EBD structure. In the context of the research, it was shown that EBD systems can be balanced by modifying the DC operating conditions of a differential amplifier. By this method, a continuous way of balancing rather that discrete balancing methods presented in literature is achieved. Furthermore, a simple tunable much simpler balancing load is implemented in this design to further increase the balancing impedance range of the EBD system.

Main achievements in this thesis can be summarized as follows:

1. EBD balancing can be done by modifying differential amplifier branch currents.
2. 60 dB of SIC at the center frequency and 40 dB SIC at 100 MHz bandwidth can be obtained inside of the Γ=0.3.
3. In order to increase EBD system's balancing range, a variable resistance, which is a single active transistor, is implemented.
4. A PA is implemented on the same chip with the EBD and the LNA.

These four points are the main points that this thesis prove to be operational. In order to improve the design and functionality of this EBD system followings can be done in the future:

1. A self adapting loop can be formed to maintain balancing at all changing conditions. As SI power would be larger than the received signal in most of the cases, by sampling the output power of the LNA, SIC amount can be determined. A proposed schematic is given in Figure 5.1. By using a coupler, power at the output of LNA is sampled. Then this power is converted into a DC voltage with the help of a RF power detector. Detected power level is fed into a microcontroller. When the sampled power level is higher than the minimum level, microcontroller starts to tip off the DC bias voltages of LNA and balancing load to reach the minimum SI level. By this way, a continuous maximum SIC can be obtained by adapting all antenna and circuit conditions.

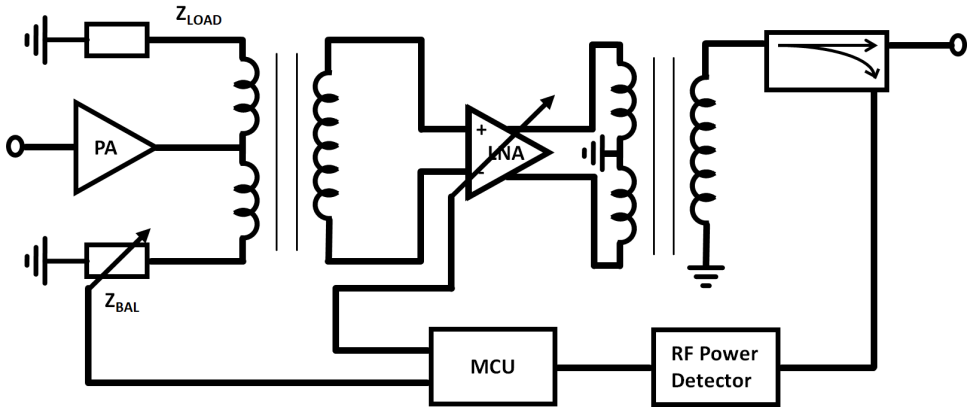


Figure 5.1: Proposed system diagram for self adapting loop

2. Further investigation on the stability issue between the active balancing load and the PA to obtain maximum power from PA.

3. Discrepancies between modeled and real transistor will be investigated and a model will be extracted for use in an EBD design.

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