SELECTIVE EMITTER FORMATION VIA SINGLE STEP DOPING THROUGH LASER PATTERNED MASK OXIDE LAYER FOR MONOCRYSTALLINE SILICON SOLAR CELLS

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
MIDDLE EAST TECHNICAL UNIVERSITY

BY

EMİNE HANDE ÇİFTPINAR

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF MASTER OF SCIENCE
IN
PHYSICS

SEPTEMBER 2014

Approval of the Thesis:

SELECTIVE EMITTER FORMATION VIA SINGLE STEP DOPING THROUGH LASER PATTERNED MASK OXIDE LAYER FOR MONOCRYSTALLINE SILICON SOLAR CELLS

submitted by **EMİNE HANDE ÇİFTPINAR** in partial fulfillment of the requirements for the degree of **Master of Science in Physics Department, Middle East Technical University** by,

Prof. Dr. Canan Özgen

Dean, Graduate School of **Natural and Applied Sciences** _____

Prof. Dr. Mehmet Zeyrek

Head of Department, **Physics** _____

Prof. Dr. Raşit Turan

Supervisor, **Physics Dept., METU** _____

Examining Committee Members:

Prof. Dr. Mehmet Parlak

Physics Department, METU _____

Prof. Dr. Raşit Turan

Physics Department, METU _____

Assoc. Prof. Dr. Emrah Ünalan

Metallurgical and Materials Engineering Department, METU _____

Assist. Prof. Dr. Alpan Bek

Physics Department, METU _____

Assoc. Prof. Dr. Ömer İlday

Electrical and Electronics Engineering Department, BU _____

Date:*02.09.2014*

I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

Name, Last Name: Emine Hande Çiftpınar

Signature :

ABSTRACT

SELECTIVE EMITTER FORMATION VIA SINGLE STEP DOPING THROUGH LASER PATTERNED MASK OXIDE LAYER FOR MONOCRYSTALLINE SILICON SOLAR CELLS

ÇİFTPINAR, Emine Hande

MS, Department of Physics

Supervisor: Prof. Dr. Raşit TURAN

September 2014, 152 pages

Selective emitter is one of the new approaches for higher efficiency solar cells. Although selective emitter cells could be processed by several different methods such as; etch back process, laser doping, ion implantation, doping paste, a different method based on diffusion through a laser patterned oxide layer was studied in this thesis. Utilization of pattern oxide layer as a diffusion barrier enables to obtain selective emitter profile via single step doping which reduces overall production cost and time significantly.

In this work, selective emitter solar cells were fabricated via single step doping through a laser patterned oxide. Oxide thickness, doping recipe, laser parameters and wet cleaning steps were optimized to reach the sheet resistance values needed for an efficient cell design. In addition, surface passivation studies were also conducted to further improve cell performance. A low temperature, dry oxidation step was also added to process sequence. Then, monocrystalline-Si selective emitter and reference solar cells were fabricated.

Both electrical and optical characterizations including reflection, lifetime, external quantum efficiency, Suns-Voc and current-voltage measurements were systematically carried out. It was observed that cells based on that new selective emitter structure could be used to reach higher conversion efficiency values compared to standard cell design with a proper finger design.

Key Words: *Selective Emitter Solar Cell, Surface Passivation, Laser Patterning, Single Step Doping.*

ÖZ

TEK KRİSTAL SİLİSYUM GÜNEŞ GÖZELERİ İÇİN LAZERLE DESENLENDİRİLMİŞ MASKE OKSİT KATMANI KULLANILARAK TEK AŞAMALI KATKILAMA İLE SEÇİCİ EMİTER OLUŞTURULMASI

ÇİFTPINAR, Emine Hande

Yüksek Lisans, Fizik Bölümü

Tez Yöneticisi: Prof. Dr. Raşit TURAN

Eylül 2014, 152 sayfa

Seçici emiter, daha yüksek verimli güneş gözeleri için kullanılan yeni göze tasarımlarından biridir. Seçici Emiter güneş gözeleri, tersine kimyasal aşındırma, lazer katkılama, iyon ekme gibi yöntemlerle üretilmesine rağmen, bu tez kapsamında lazerle desenlendirilmiş oksit tabaka kullanılarak tek aşamalı katkılama yöntemi çalışılmıştır. Desenlendirilmiş oksit tabakının difüzyon bariyeri olarak kullanılması üretimin tek aşamalı katkılama ile yapılmasına olanak sağlamakta, dolayısıyla, toplam üretim maaliyetini ve süresini düşürmektedir.

Bu tez kapsamındaki çalışmalarda, tek kristla silisyum güneş gözeleri için lazerle desenlendirilmiş oksit katman kullanırak tek aşamalı katkılama ile seçici emiter üretilmeye çalışılmıştır. Bu amaçla, oksit kalınlığı, katkılama reçesi, lazer parametreleri ve kimyasal temizlik aşamaları optimize edilmiştir. Buna ek olarak, hücre verimini daha iyi hale getirilebilmesi için yüzey pasivasyon çalışmaları da sürdürülmüştür. Bu amaçla, Düşük sıcaklıkta oksidasyon aşaması üretim akışına eklenmiştir.

Daha sonra, seçici emiter ve referens güneş gözeleri üretilmiştir. Yansıma, yarı ömür, Suns-Voc, E.Q.E ve akım-voltaj ölçümlerini içeren elektriksel ve optik karaterizasyonlar yapılmıştır. Bu çalışmaların sonucunda gözlendi ki; tasarlanan üretim yöntemi kullanılarak, uygun bir ön metalizasyon tasarımı ile seçici emiter güneş gözeleri referans gözelerden daha iyi sonuçlar elde edilebilir.

Anahtar Kelimeler: *Seçici Emiter Güneş Gözeleri, Yüzey Pasivasyonu, Lazer Desenlendirme, Tek Aşamalı Katkılama.*

To my dearest friends and family…

ACKNOWLEDGEMENTS

Firstly, I would like to thank Professor Raşit TURAN for giving me the opportunity of working with him and being a member of GUNAM family. I will be always grateful to him for his guidance, endless support and patience for all three years of my studies. I would like to thank Professor Mehmet PARLAK for all his help and kind attitude towards me since my undergraduate years.

I would also like to thank two special guys who mean more than friends for me; Fırat ES and Olgu DEMİRCİOĞLU. I don't know how I can pay for so many things they have done for me. I would like to start with Fırat from whom I've been learning so many things since the beginning of my studies, he has always been a great teacher, lab.partner, supporter and a real friend for me. Olgu has been another great friend and a brother pushing me to prepare weekly reports on time, to present myself in a better way and of course to write my thesis. He is the one who trusted in me about many different things and convinced me that I could do. Moreover, both Fırat and Olgu made a great effort to make me start writing this thesis and they didn't stop pushing me even if I gave up. I would like to continue with Zeynep DEMİRCİOĞLU. She is the one who has always been ready for help with a great smile on her pretty face. She gave me her hand when I was struggling with all these format adjustments and she has always been a great friend for me. I would also like to thank Selma ES for her care, nice friendship and her pretty saying: *"Naptın Handan, tez bitti mi?"*.

I would like to continue with Assist. Prof. Dr. Mustafa KULAKCI for his help at my first year in the group and for his friendship, too. I'm also grateful to Makbule TERLEMEZOĞLU for her priceless friendship and being my roommate with patience for three years. I would like to thank İsmail KABAÇELİK for his friendship and support.

I would like to thank Yasin ERGUNT for his friendship and kind help offers for anything I need especially during thesis writing period. I would like to thank Mete GÜNÖVEN for his effort on reflection and quantum efficiency measurements. I would also like to thank Ergi DÖNERÇARK for his nice friendship and reminding me that how many days left to my thesis presentation. I'm also grateful to Serra ALTINOLUK, my "*apla*" in her words, for her effort to make me continue writing and her effective e-mails that really pushed me even when she was abroad. I would like to thank Engin ÖZKOL for his friendship and also his help for a-Si depositions together with Zeynep. I would also like to thank all LAB 118 and basement staff starting at Dr.Tahir ÇOLAKOĞLU, Burcu ALTUNTAŞ, Salar HABIBPUR, Yusuf KASAP, Serim KAYACAN İLDAY, Burcu BARUTÇU, Mehmet KARAMAN, Mona ZOLFAGHARİ BORA, Fatih UZGUR, Gülsen BAYTEMİR, Hasan Hüseyin GÜLLÜ, Çiğdem DOĞRU, Özden Başar BALBAŞI, and Seda KAYRA GÜLLÜ for their friendship.

I would also like to thank my dearest friends Ceyda MISIRLIOĞLU, Nesrin AY, Oğuz AY and their lovely daughter Aypare AY for being in my life.

I also need to thank all GUNAM staff including Harun TANIK, Buket GÖKBAKAN and Tuncay GÜNGÖR for their kind attitude since I participated into the group. I would like to thank our technical staff Nevzat GÖRMEZ, Tayfun YILDIZ, Dursun ERDOĞAN, Mustafa YILDIRIM and especially Yücel EKE. I would like to continue with our pretty department secretaries Gülşen ÖZDEMİR PARLAK and Zeynep EKE for their endless help and positive attitude for all eight years that I spent in physics department.

Finally, I would like to thank my family for their patience and support along my studies.

TABLE OF CONTENTS

ABSTRACT v

ÖZ vii

ACKNOWLEDGEMENTS x

TABLE OF CONTENTS xii

LIST OF FIGURES xv

LIST OF TABLES xxi

CHAPTERS

1.INTRODUCTION 1

1.1. History and Current Status of Photovoltaic Technology 2

1.2. Classification of Solar Cell Technologies 5

1.2.1. 1st Generation Solar Cells 5

1.2.2. 2nd Generation Solar Cells 6

1.2.3. 3rd Generation Solar Cells 7

1.3. Relevant Concepts and Definitions 8

1.3.1. Solar Irradiation 8

1.3.2. Solar Cell Parameters and I-V Characteristics 10

2.FUNDAMENTALS OF CRYSTALLINE SILICON SOLAR CELL TECHNOLOGY 17

2.1. Silicon Wafer Production 17

2.2. Standard Single Crystalline Silicon Solar Cell Production 19

2.2.1. Surface Texturing 20

2.2.2. Doping 24

2.2.3. Anti Reflective Coating (ARC) 31
2.2.4. Metallization 34
2.2.5. Edge Isolation 38
3.A SINGLE STEP DOPING TECHIQUE FOR SELECTIVE EMITTER SOLAR CELLS AND PASSIVATION TECHIQUES FOR BETTER CELL PERFORMANCE 41
3.1. Selective Emitter Cell Concept 41
3.2. Fabrication Methods of Selective Emitter Cell 42
3.2.1. Emitter Etch Back 42
3.2.2. Laser Doping 44
3.2.3. Ion Implantation 47
3.2.4. Diffusion through a Barrier 49
3.3. Carrier Recombination and Related Passivation Techniques for Crystalline Silicon Solar Cells 55
3.3.1. Recombination Basics 55
3.3.2. Passivation Techniques 65
4.EXPERIMENTAL PROCEDURES 69
4.1. SINGLE DOPING STEP SELECTIVE EMITTER SOLAR CELL FABRICATION PROCESS FLOW 69
4.1.1. Texturing 69
4.1.2. Oxide Masking 70
4.1.3. Laser Patterning 71
4.1.4. Post Laser Cleaning 72
4.1.5. Doping 72
4.1.6. Anti Reflection Coating 74
4.1.7. Metallization and Co-Firing 76
4.1.8. Edge Isolation 76

4.2. PASSIVATION STUDIES 77
4.3. CHARACTERIZATION 77
4.3.1. Solar Cell Characterization 77
4.3.2. Characterization of Lifetime Samples 83
5.RESULTS and DISCUSSION 87
5.1. SELECTIVE EMITTER SOLAR CELL PROCESS OPTIMIZATIONS 87
5.1.1. First Run 87
5.1.2. Second Run 100
5.1.3. Third Run 115
5.2. SURFACE PASSIVATION STUDIES 129
6.CONCLUSIONS 143
BIBLIOGRAPHY 149

LIST OF FIGURES

FIGURES

Figure 1: NREL's best research cell efficiencies [49] 3
Figure 2: Country distribution of installed PV capacity by 2012 [4] 4
Figure 3: Market share of different PV technologies by 2010 [1] 4
Figure 4: Industrial mono and multi crystalline silicon solar cells [5] 5
Figure 5: CIGS solar cells on flexible substrate [6] 6
Figure 6: (a) Organic solar cell on flexible substrate [50] and (b) DSSC panel [51] .. 7
Figure 7: Solar spectrum reaching the Earth's surface [10]. Blue curve represents the spectrum on the surface of the Earth. Absorption bands of water vapor, O2, and CO2 are clearly seen 9
Figure 8: Schematic of A.M. 0, 1 and 1.5 conditions 9
Figure 9: I-V Characteristics of solar cell under dark and illuminated conditions [11] 11
Figure 10: I-V curve plotted in the 1st quadrant and representation of corresponding I_{sc} and V_{oc} values 13
Figure 11: External quantum efficiency of a silicon solar cell [13] 15
Figure 12: Cross-sectional view of a standard Si solar cell 17
Figure 13: Summary of Si purification process Process 18
Figure 14: Standard solar cell production Steps 20
Figure 15: Fraction of AM1.5 spectrum utilized by c-Si [16] 21
Figure 16: Absorption coefficient and depth of intrinsic Si at 300^{o}K 21
Figure 17: Etching process of (100) Si Surface 23
Figure 18: Reflection from a flat surface (a) and textured surface (b) 24
Figure 19: Crystal structure of intrinsic Si (a), phosphorous Si (b) and boron doped Si (c) 25
Figure 20: Cross-sectional view of a p-n junction 26
Figure 21: Band diagram of n-Si and p-Si before electrical contact 27
Figure 22: Band diagram of the system after p-n junction formation 27

Figure 23: Reflection spectrum of bare silicon 31
Figure 24: Band diagrams of metal and n-Semiconductor 35
Figure 25: Band diagram of metal-n-Semiconductor junction after 36
Figure 26: Band Diagram of metal and n-Semiconductor before physical contact ... 37
Figure 27: Band diagram of metal & n-Semiconductor after physical contact 37
Figure 29: Operation of a Si solar cell before edge isolation 39
Figure 30: Operation of a Si solar cell after edge isolation by laser ablation 39
Figure 31: Fabrication process of emitter etch back selective emitter solar cells 43
Figure 33: Fabrication process of laser doped selective emitter solar cells 46
Figure 34: Fabrication process of laser doped selective emitter solar cells with single step doping 47
Figure 35: Fabrication process of ion implanted selective emitter solar cells 48
Figure 36: Fabrication process of selective emitter solar cells using amorphous Si diffusion barrier 50
Figure 37: Fabrication process of selective emitter solar cells using silicon 52
Figure 38: Fabrication process of selective emitter solar cells using silicon 54
Figure 39: Schematic of radiative recombination process 57
Figure 40: Schematic of Auger recombination process 59
Figure 41: Schematic of Shockley Read Hall mechanism: (a) electron emission, (b) electron capture, (c) hole capture, (d) hole emission 62
Figure 42: Representation of Si dangling bonds 63
Figure 44: Schematic of oxidation furnace 70
Figure 45: Schematic of doping furnace 73
Figure 46: Schematic of PECVD chamber 74
Figure 47: Reflection set-up used in GUNAM Laboratories 78
Figure 48: Schematic of solar simulator 80
Figure 49: Schematic of external quantum efficiency set-up placed at GUNAM Laboratories 81
Figure 50: Schematic of contact resistance measurement system 83
Figure 51: Schematic of Lifetime measurement system 84
Figure 52: Effect of KOH dipping duration on groove depth 88
Figure 53: Oxidation duration, oxide thickness and sheet resistance relationship 89

Figure 54: Effect of 10% KOH dipping duration on sheet resistance of (a) standard doping, (b) high doping samples 90
Figure 55: Effect of mask oxide thickness on (a) cell efficiency, (b) fill factor 91
Figure 56: Effect of mask oxide thickness on (a) V_{OC}, (b) J_{SC} 92
Figure 57: Effect of mask oxide thickness on series resistance 92
Figure 58: Electroluminescence images of (a) reference cell, (b) selective emitter with 20 nm oxide mask, (c) selective emitter with 30 nm oxide mask for standard doping 93
Figure 59: Effect of sheet resistance and dead area on series resistance 94
Figure 60: Optical microscope images of (a) misaligned finger, (b) misaligned finger-busbar cross-section, (c) aligned finger under 20X magnification 95
Figure 61: Circuit representation of two diode model 96
Figure 62: Effect of mask oxide thickness on (a) pseudo efficiency, (b) pseudo fill factor 96
Figure 63: Effect of mask oxide thickness on Voc 97
Figure 65: Effect of mask oxide thickness on external quantum efficiency of high doping samples 99
Figure 66: J-V characteristics and corresponding efficiency and fill factors of high doping selective emitter and reference cells 100
Figure 67: Sheet resistance mapping on a full wafer with 4cm^2 laser scanned squares of different parameters 101
Figure 68: Effect of (a) 5sec., (b) 10sec., (c) 17 sec HF dipping on sheet resistance of both high and standard doping samples with 20,30 and 50 nm mask oxide layers for laser speed: 3mm/s with table (d) of symbol about corresponding doping recipe, oxide thickness and laser current. Lines are for visual aid 102
Figure 69: Effect of laser scan speed on sheet resistance. Lines are for visual aid . 104
Figure 70: Effect of mask oxide thickness on cell efficiency of fabricated cells (a) with oxide passivation, (b) without oxide passivation. 105
Figure 71: Effect of mask oxide thickness on fill factor of solar cells (a) with oxide passivation, (b) without oxide passivation. 105
Figure 72: Effect of mask oxide thickness on Voc (a) with oxide passivation, (b) without oxide passivation. Lines are for visual aid 106

Figure 73: Effect of mask oxide thickness on J_{SC} (a) with oxide passivation, (b) without oxide passivation. Lines are for visual aid 107
Figure 74: Effect of mask oxide thickness on Rseries (a) with oxide passivation, (b) without oxide passivation. Lines are for visual aid 107
Figure 75: Electroluminescence images of selective emitter cells with (a) 20, (b) 30, and (c) 50 nm mask oxide. Lines are for visual aid 108
Figure 76: Electroluminescence images of reference cells (a) without oxide passivation, (b) with oxide passivation. Lines are for visual aid 109
Figure 77: Electroluminescence images of oxide passivated selective emitter cells with (a) 20, (b) 30 and (c) 50 nm mask oxide. Lines are for visual aid 109
Figure 78: Effect of mask oxide thickness on pseudo efficiency (a) with (b) without oxide passivation. Lines are for visual aid 110
Figure 79: Effect of mask oxide thickness on pseudo fill factor (a) with 111
Figure 80: Effect of mask oxide thickness on Voc (a) with (b) without oxide passivation. Lines are for visual aid 111
Figure 81: Effect of mask oxide thickness on J_{01} (a) with (b) without oxide passivation. Lines are for visual aid 112
Figure 82: Effect on mask oxide thickness on J_{02} (a) with (b) without oxide passivation. Lines are for visual aid 112
Figure 83: External quantum efficiency comparison of fabricated solar cells 113
Figure 84: Resistance measurements by transferring line method. Lines are for visual aid 114
Figure 85: Effect of mask oxide thickness on contact resistance. Lines are for visual aid 115
Figure 86: Efficiency values of fabricated (a) Cz and (b) FZ cells. Lines are for visual aid 117
Figure 87: Fill factor values of fabricated (a) Cz and (b) FZ cells. Lines are for visual aid 118
Figure 88: Open circuit voltage values of fabricated (a) Cz and (b) FZ cells. Lines are for visual aid 118
Figure 89: Short circuit current density values of fabricated (a) Cz and (b) FZ cells. Lines are for visual aid 119

Figure 90: Series resistance values of fabricated (a) Cz and (b) FZ cells. Lines are for visual aid 120
Figure 91: Series resistance-fill factor-efficiency relationship of fabricated (a) Cz and (b) FZ cells. Lines are for visual aid 120
Figure 92: Pseudo efficiency values of fabricated (a) Cz and (b) FZ Cells. Lines are for visual aid..... 121
Figure 93: Pseudo fill factor values of fabricated (a) Cz and (b) FZ cells. Lines are for visual aid..... 122
Figure 94: Measured Voc values of fabricated (a) Cz and (b) FZ cells. Lines are for visual aid 122
Figure 95: Measured J_{01} values of fabricated (a) Cz and (b) FZ cells. Lines are for visual aid 123
Figure 96: Measured J_{02} values of fabricated (a) Cz and (b) FZ cells. Lines are for visual aid 124
Figure 97: EQE comparison of reference and selective emitter solar cells with corresponding short circuit current density enhancement..... 125
Figure 98: EQE comparison of oxide passivated reference and selective emitter solar cells with corresponding short circuit current density enhancement 126
Figure 99:Reflection spectra of bare , oxide, nitride and oxide/nitride stack existing textured silicon surfaces..... 127
Figure 100: Internal and external quantum efficiency and corresponding reflectance spectrum of a reference cell 128
Figure 101: Internal and external quantum efficiency and corresponding reflectance spectrum of an oxide passivated reference cell..... 128
Figure 102: Effect of process gas flow ratios on lifetime 130
Figure 103: Effect of process gas flow ratios on lifetime of SSP wafers 132
Figure 104: Effect of standard nitride deposition on effective lifetime 134
Figure 105: Effect of process gas flow ratio on refractive index at 632 nm. Lines are for visual aid..... 135
Figure 106: Effect of process gas flow ratio on lifetime of (a) n-type, (b) p-type DSP samples. Lines are for visual aid..... 136
Figure 107: Effect of sample shape on lifetime. Lines are for visual aid 137

Figure 108: Effect of process gas flow ratio on lifetime of full (a) n-type, (b) p-type DSP wafers. Lines are for visual aid 137
Figure 109: Effect of oxide passivation via dry oxidation on lifetime of full (a) n-type, (b) p-type DSP wafers. Lines are for visual aid 138
Figure 110: Effect of oxide passivation via pyrogenic oxidation on lifetime of full (a) n-type, (b) p-type DSP wafers. Lines are for visual aid 139
Figure 111: Effect of nitride deposition on oxide passivated full (a) n-type, (b) p-type DSP wafers. Lines are for visual aid 140
Figure 112: Performance of oxide / nitride stack structure. Lines are for visual aid141

LIST OF TABLES

TABLES

Table 1: SiH_4 & NH_3 flow rates of applied recipes on solar wafers and corresponding film thicknesses with refractive indices at 632nm 129

Table 2: Applied chamber pressures for standard nitride recipe and corresponding film thicknesses with refractive indices at 632 nm 131

Table 3: SiH_4 & NH_3 flow rates of applied Recipes on SSP wafers and corresponding film thickness with refractive indices at 632 nm 132

Table 4: Resistivity values of DSP wafers and corresponding names 133

CHAPTER 1

INTRODUCTION

With increasing energy demand of the world, utilization of alternative energy sources has become even more crucial within the last decades. Having advantages like abundancy and availability, the use of solar energy in electricity generation is becoming more and more popular compared to other alternative energy sources. Moreover with the increasing efforts in research and development, the efficiency of the energy conversion is steadily increasing. In particular, the efficiency of the most widely used solar cell technology, which is, wafer based Si solar cells has reached values exceeding 25% while this value drops to 22.9% at module level[1]. To increase the conversion efficiency even more, different cell designs have been developed. Selective Emitter (S.E.), Back Contact (B.C.), Passivated Emitter with Rear Collector (PERC) and Passivated Emitter with Rear Locally Diffused (PERL) cells are some of the promising cell concepts developed recently.

In the selective emitter approach, the idea is to have both low contact resistance and low emitter dopant concentration in the same device. Low contact resistance is required to reduce series resistance of the corresponding cell whereas decreased dopant concentration would reduce the front surface recombination. However, low resistance requires high doping level which inevitably increases front surface recombination. Thus, there exists a trade-off between emitter resistance and front side recombination. In order to solve this problem selective emitter approach has been developed. In this approach the emitter region lying under the front metal contact is heavily doped, while rest of the emitter is lightly doped. Thus, surface recombination is reduced without increasing series resistance of the cell. As a result, emitter saturation current is reduced, open circuit voltage of the cell increases and blue response is improved

1.1. History and Current Status of Photovoltaic Technology

The development of photovoltaic (PV) technology started with the Bequerel's discovery of photovoltaic effect when he observed electrical current production from a silver coated platinum electrode immersed into in electrolyte under light in 1839. Then, in 1876, Adams and Day found that photocurrent could be produced from a selenium sample contacted with platinum. In 1954, with the help of developing silicon technology, first solar cell was reported by Chapin, Fuller and Pearson with an efficiency of 6% in Bell Laboratories [2]. In addition to the production of first silicon solar cell, a 6 % efficient cadmium-sulphide p-n junction was also produced in 1954 [2].

In 1970's, as a result of crisis in the oil based energy supply, alternative energy sources drew interest among which photovoltaic energy was paid the greatest attention. Although the former studies focused mainly on space applications, the latter studies in the early 1980's resulted in decreased production cost and ensured continuous expansion of commercial applications for the utilization of the Sun's energy [3].

In 1990's, as a result of expanded interest towards photovoltaics, the awareness of need to find new energy sources alternative to fossil fuels also grew. Thus, in late 1990's the annual production of photovoltaics increased at a rate of 15-20% resulting in a further reduction in production costs [2]. Reduced cost made new application areas to be opened and new materials to be studied. So that, photovoltaic platform gained a great diversity ranging from high efficiency gallium arsenide, including wafer based silicon, thin film silicon to the younger dye sensitized and organic solar cell technologies. The development of photovoltaic technology could be seen in Figure 1.

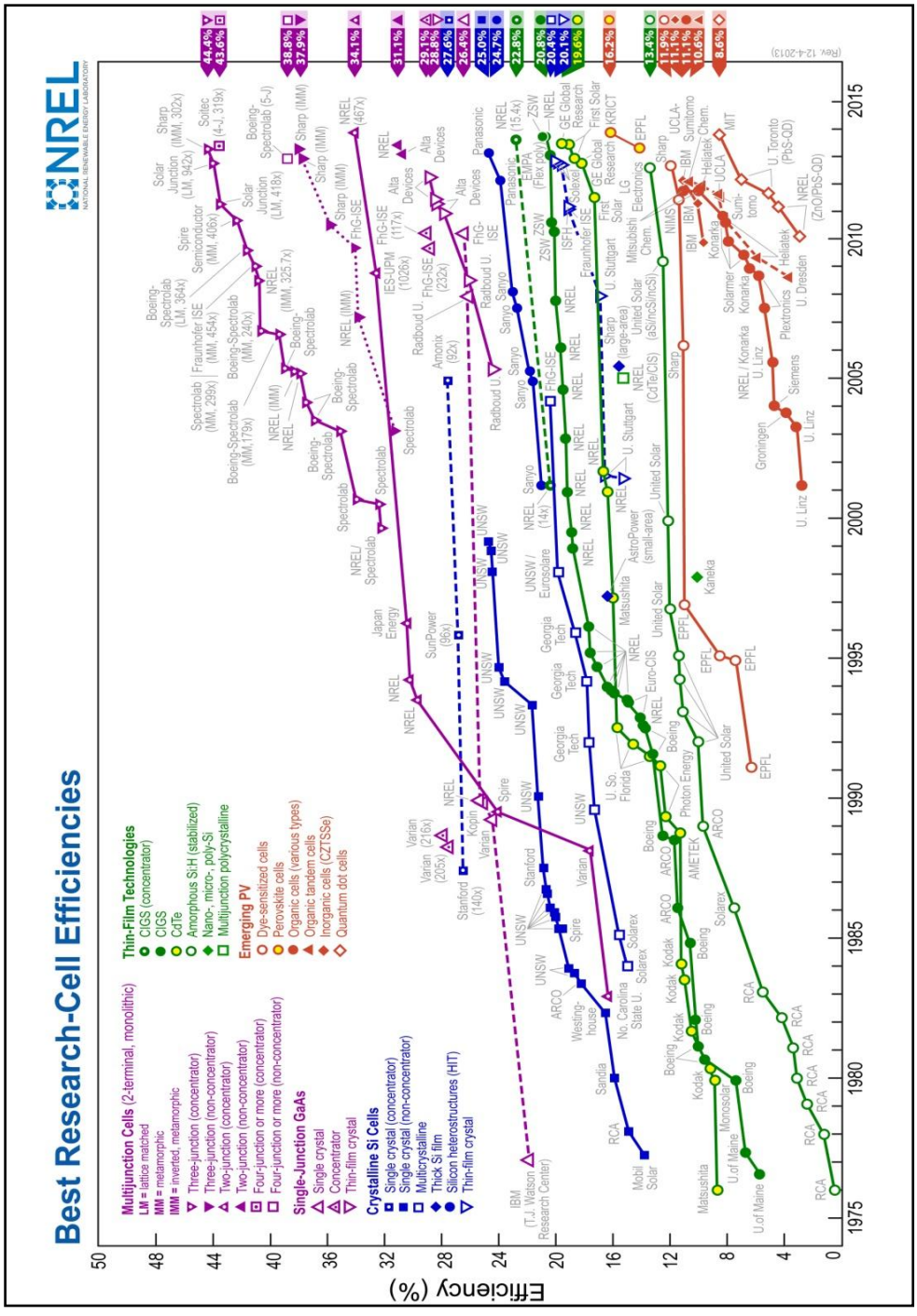


Figure 1: NREL's best research cell efficiencies [49]

By 2012, due to reduced production costs and due to some regulations considering CO_2 emission, installed PV capacity throughout the world has reached considerable values. Distribution of installed PV capacity by 2012 is shown in Figure 2. It is seen that EU countries, particularly Germany and Italy, have played a more important role in boosting the PV installation.

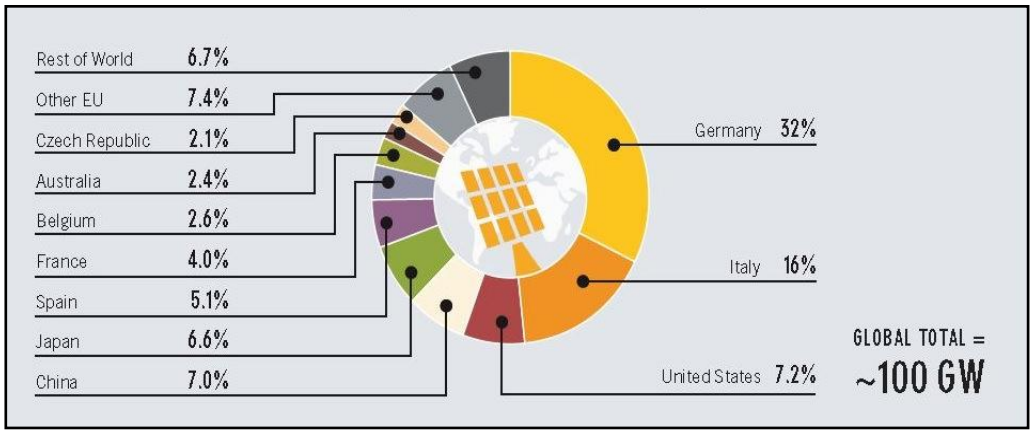


Figure 2: Country distribution of installed PV capacity by 2012 [4]

When market share of different PV technologies is analyzed, it is deduced that standard crystalline silicon technology is dominating the market.

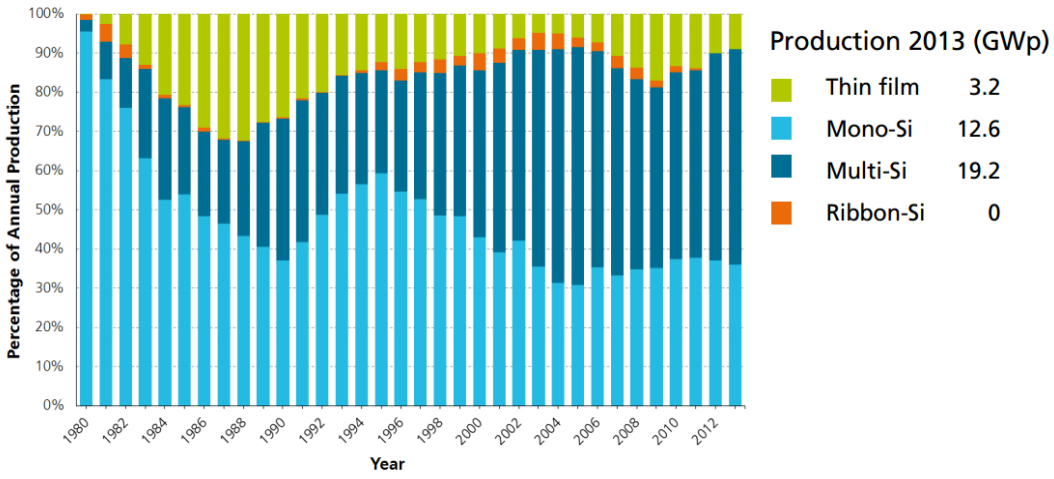


Figure 3: Market share of different PV technologies by 2010 [1]

Referring to Figure 3, it could be deduced that standard c-Si technology has reached a market share of 83% by 2010.

Silicon used in semiconductor technology is obtained from processed and purified form of sand which is the most abundant material forming the Earth's crust. Moreover, silicon is the material that has been studied for more than 30 years in semiconductor industry so that an extensive experience has been gained in processing of this material. Taking all these factors into account, it is reasonable for silicon technology to dominate the photovoltaic market today.

1.2. Classification of Solar Cell Technologies

1.2.1. 1st Generation Solar Cells

First generation solar cells are the wafer based type of solar cells still governing the solar market today. Although both mono and multi crystalline Si wafers could be used as base materials for that type of solar cells (Figure 4), multi crystalline cell production is holding a greater share of the world market. Mono crystalline wafers provide higher efficiency values with higher production cost values whereas multi crystalline wafers impose relatively lower efficiencies with lower production costs. In Figure 1, image of industrial mono and multi crystalline solar cells is shown.

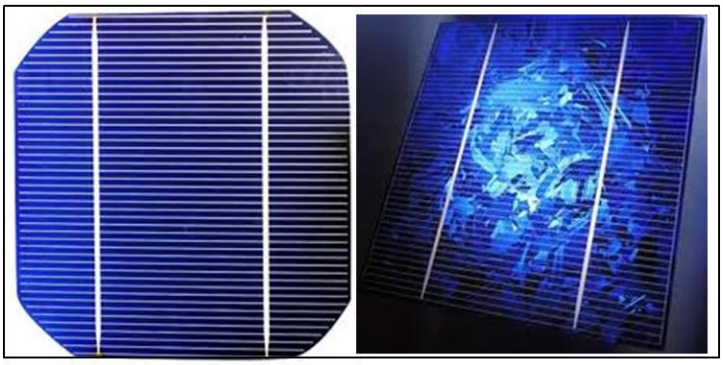


Figure 4: Industrial mono and multi crystalline silicon solar cells [5]

Considering the fact that wafer cost has a great effect on the overall production cost of solar cells, using multi crystalline Si wafers has been preferred by manufacturers despite relatively lower efficiency values. Mono c-Si solar cells reached efficiency values around 24% whereas multi c-Si solar cells are exceeding 21%. It can be argued that with the help of developing technology wafer based technology could dominate the PV industry for many years.

1.2.2. 2nd Generation Solar Cells

Contrary to the ordered structure of crystalline wafers, second generation solar cells are fabricated in the form of thin films. For this type of solar cells, active material is deposited on a glass or on a flexible substrate by a physical or chemical process depending on the type of the material to be deposited. Amorphous Si, CIGS (Cupper Indium Gallium (di)Selenide) and CdTe (Cadmium Telluride). are major thin film materials used as active layers today's commercialized thin film technologies (Figure 5).

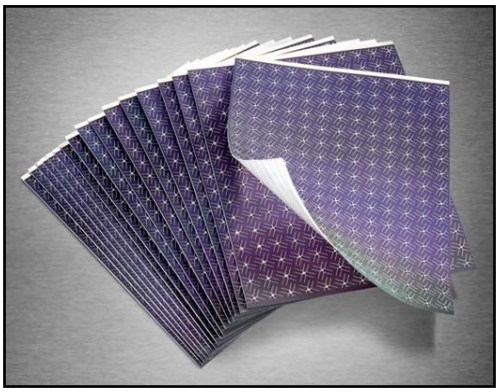


Figure 5: CIGS solar cells on flexible substrate [6]

As a result of high absorption coefficients of thin film materials, only a few micron thick active layers will be enough to absorb the incident light. Although less material consumption is an advantage of thin film solar cells, low efficiency values

couldn’t compete with their crystalline counterparts. Moreover, thin film solar cells suffer from instability problems resulted from sunlight exposure.

1.2.3. 3rd Generation Solar Cells

Third generation solar cells are made from a variety of novel materials including solar dye, multi-junction concepts (tandem solar cells), solar cells based on various quantum structure, conductive plastics, solar inks and also organic materials. In all these new approaches, high efficiency and low cost systems are targeted. Very cheap cells with moderate efficiency values (10-15%) and very high efficiency (>30%) and expensive systems are all considered to be third generation solar cells

Organic solar cells and Dye Sensitized Solar Cells (DSSC) are cheap but less efficient solar cells. For organic solar cells, shown in Figure 6-a, low cost polymers could be deposited on any substrate as active layer which makes roll-to-roll process possible. Besides being used as active layer, organic polymers could also be applied to tandem solar cell structures resulting in efficiency values 6.5 % [7]. DSSC’s, shown in Figure 6-b, could be taken as attractive low cost devices where a porous layer of titanium dioxide (TiO_2) nanoparticles is covered with light absorbing dye molecules.

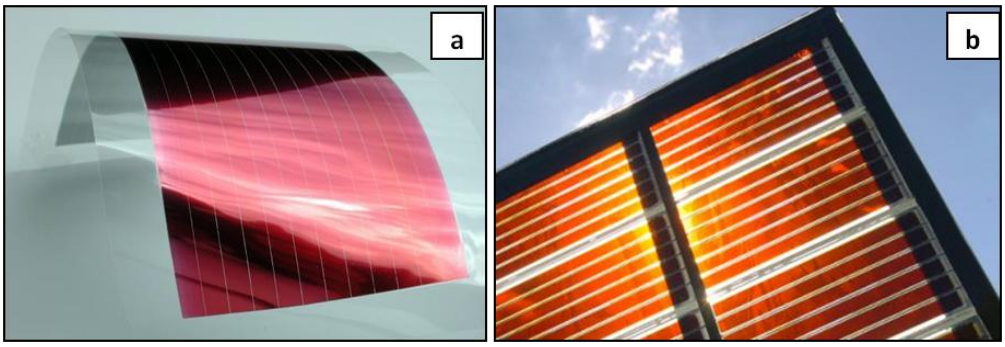


Figure 6: (a) Organic solar cell on flexible substrate [50] **and (b) DSSC panel** [51]

Absorption of incident light excites electrons which flow into the TiO_2. Then, those flowing electrons are collected at the corresponding electrodes. Efficiency values of 11.1 % have been reported for DSSC's [8].The greatest problem of those cheap devices is the degradation of the cell and high recombination rate of charge carriers [2]. Utilization of III-V semiconductors like GaAs, InP, InAs made in tandem configuration makes it possible to absorb different regions of solar radiation at different layers of solar cells. Bandgaps of these materials could be engineered for each layer independently resulting in attractive device performance. Efficiency values of 30.8 % could be reached under 1 sun illumination whereas that value reaches 44.7 % under concentration [1], [9].

1.3. Relevant Concepts and Definitions

1.3.1. Solar Irradiation

Solar irradiation is the energy of the light incident on Earth's surface coming from the Sun. Earth is at a distance 15 x 10^{10} meters away from the Sun which results in a mean solar irradiance of approximately 1360 W/m^2 at the Earth's surface outside the atmosphere. Solar irradiance is affected by the medium while passing through the atmosphere. Dust particles, water vapor (H_2O) and the other gas molecules especially carbon dioxide (CO_2), ozone (O_3) existing in the atmosphere will interact with the incident light causes absorption, reflection or scattering. As a result, a highly modified solar spectrum is obtained as shown in Figure 7.

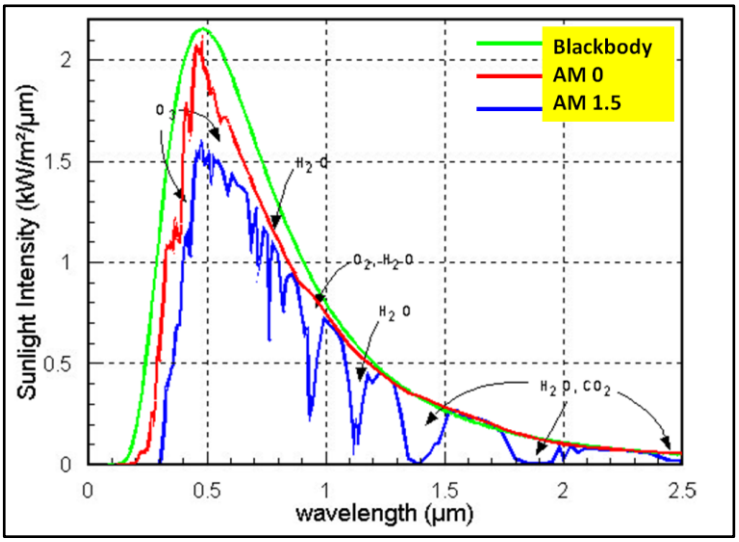


Figure 7: Solar spectrum reaching the Earth's surface [10]**. Blue curve represents the spectrum on the surface of the Earth. Absorption bands of water vapor, O_2, and CO_2 are clearly seen**

"AM" is an acronym standing for the term "air mass" which defines the ratio of path length that the light travels through the atmosphere at a specific condition to the path length that it travels when the sun is directly overhead.

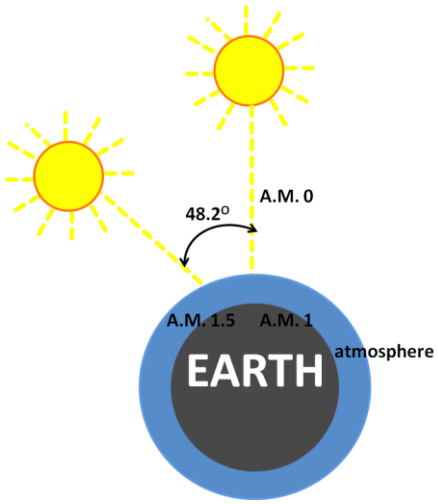


Figure 8: Schematic of A.M. 0, 1 and 1.5 conditions

"AM 0" defines the solar radiation just outside the atmosphere whereas "AM1" and "AM1.5" condition refers to the sun positioned along the vertical direction and at an angle of 48.2^{o} with the vertical axis respectively (Figure 8). Air Mass could be calculated by the following equation;

$$Air\ Mass\ (AM) = \frac{1}{\cos\theta} \qquad (Eq.1)$$ [2]

In above equation, "θ" is the angle that the sun is making with its vertical axis, also called as "*zenith angle"*.

Moreover, incident sun light could be divided into its components as "*diffuse*" and "*direct*" radiation. Direct radiation only takes the direct portion of the incident light which doesn't take the scattering effect into consideration whereas diffuse radiation only takes the scattered portion of the light into account while neglecting the direct radiation. Summation of direct and diffuse components results in "*global"* radiation. "AM1.5*D*" stands for the *direct* component of the AM1.5 condition while "AM1.5*G*" stands for the *global* radiation in conventional solar applications. At AM1.5 condition, irradiance outside the atmosphere is taken as 1000 W/m^2 and that constant value is also named as "*1 SUN*". Also AM1.5 condition, at T=25^{o}C is taken to be standard test conditions (STC) for solar cell measurements.

1.3.2. Solar Cell Parameters and I-V Characteristics

I-V Characteristics

Solar cell is simply a diode structure which is sensitive to the light impringing on it. Under dark conditions, a reverse saturation current – voltage characteristics of a solar cell is expressed as in the following equation;

$$I = I_0\left(e^{\frac{qV}{kT}} - 1\right) \qquad (Eq.2)$$ [2]

Incident light will generate current in the same direction as reverse saturation current which is expressed in Eq.3.

$$I = I_0 \left(e^{\frac{qV}{kT}} - 1\right) - I_L \qquad (Eq.3)$$ [2]

where I_0 is reverse saturation current determined by diode properties, q is electron charge, V is voltage applied between the terminals of the cell, k is Boltzmann constant, T is cell temperature in Kelvin, I_L is the light generated current and I is the net current flowing through the cell. Thus, current (I)- voltage (V) curve of solar cell will be superposition of I-V curve of the solar cell diode under dark and under light (Figure 9).

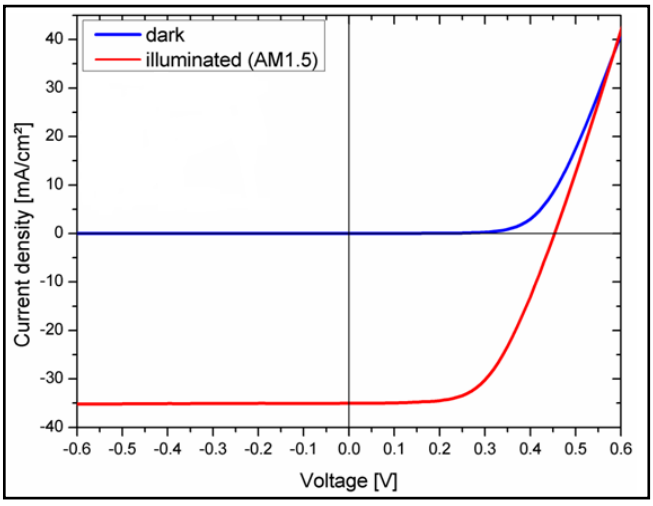


Figure 9: I-V Characteristics of solar cell under dark and illuminated conditions [11]

For the sake of conventional presentation, that curve is usually folded to the 1st quadrant.

Conversion Efficiency

Silicon solar cells with an ideal, single p-n junction have an upper efficiency value of around 30% due to both electronic and optical losses [12]. Optical losses could be attributed to reflection from the surface and absorption whereas electronic losses could be related to resistive effects and recombination losses where both optical and electronic losses posses an upper limit for the maximum efficiency of a solar cell.

In the most general sense, the conversion efficiency could be defined as the ratio of output of a device to the input optical power as in the following;

$$Cell\ Efficiecny\ (\eta) = \frac{P_{out}}{P_{in}} = \frac{P_{mpp}}{P_{light}} = \frac{V_{mpp} \times I_{mpp}}{P_{light}} \qquad (Eq.4)\ [2]$$

where P_{light} is the power of the light incident on the solar cell being measured and P_{mpp} is the power at the maximum power point (mpp) or the maximum power that could be obtained from the cell.

Solar cell efficiency measurement is carried out under standard test conditions consisting of a solar radiation of 1000W/m^2, AM1.5 and cell a cell temperature set to 25^{o}C.

Open Circuit Voltage

Open circuit voltage (V_{oc}) is the voltage output of the illuminated solar cell whereas no current flows through the device. V_{oc} is the maximum voltage output to be obtained from a solar cell (Figure 10) and determined by the properties of the semiconductor. Setting I to zero in Eq.3 will give V_{oc} equation as in the following equation:

$$V_{oc} = \frac{kT}{q} \ln\left(\frac{I_L}{I_0} + 1\right) \qquad (Eq.5)\ [2]$$

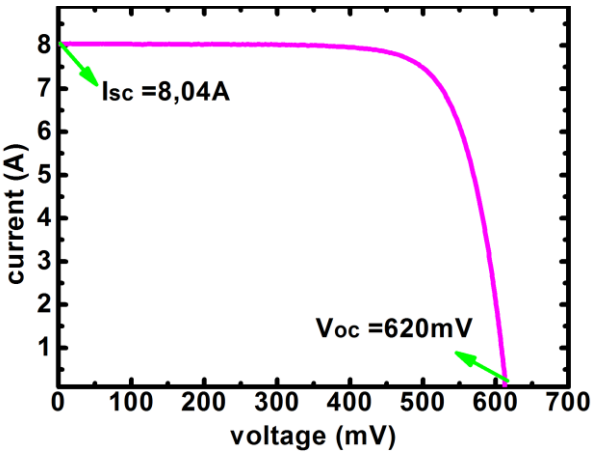


Figure 10: I-V curve plotted in the 1st quadrant and representation of corresponding I_{sc} and V_{oc} values

Short Circuit Current

Short circuit current (I_{sc}) is the current flowing through the cell under zero voltage between the terminals of the cell (Figure 10). I_{sc} is the maximum current value to be obtained Setting V to zero in Eq. 3 will give I_{sc} value which is equal to light generated current I_L.

Fill Factor

Fill factor (*FF*) is the parameter defining the squareness of the I-V curve. Since the area under I-V curve gives the power output of the cell, the more square-like curve will result in higher power output so higher efficiency values. For reasonable efficiency values, *FF* should lie in a range from 0.7 to 0.85. Mathematically, *FF* could be defined as;

$$FF = \frac{V_{mpp} \times I_{mpp}}{V_{oc} \times I_{sc}} \qquad (Eq.6)\ [2]$$

Series Resistance

Light generated current has to pass through the semiconductor which is the active layer of the solar cell, the metal-semiconductor interface and also metal contacts while being collected at an external load. Each of these segments will show a certain resistance towards the flow of generated current. Overall resistance of the structure is called as series resistance (R_s) and expressed as in the following;

$$Series\ Resistance\ (R_s) = \left(\frac{1}{\frac{dI}{dV}}\right)_{V=V_{oc}} \qquad (Eq.7)\ [2]$$

For a better cell performance, R_s should be minimized as possible. Rs can be easily determined from the derivative of the measured I-V at V_{oc} = 0.

Shunt Resistance

Shunt resistance (R_{sh}) could be mainly attributed to manufacturing imperfections rather than poor cell design. R_{sh} value could be used as an indicator for current leakages within the cell. Lower shunt resistance might indicate the presence of alternative paths for the light generated current passing through cell rather than being collected at an external load. The effect of low shunt resistance will be more severe at low illumination levels; since the less amount of current will be generated by light. Shunt resistance could be expressed as;

$$Shunt\ Resistance\ (R_{sh}) = \left(\frac{1}{\frac{dI}{dV}}\right)_{V=0} \qquad (Eq.8)\ [2]$$

For a better cell performance, R_{sh} should be as high as possible.

Quantum Efficiency

Quantum Efficiency (Q.E.) is the parameter defining the number of collected charge carriers for each photon absorbed by the solar cell. For the ideal case where all incident photons is absorbed and all generated charge carriers are collected, Q.E. will be unity as shown in Figure 11. Since Si will be transparent to light with energy below its band gap, 1.12 eV, Q.E. will drop to zero for the wavelengths beyond wavelength corresponding to 1.12 eV.

For the non-ideal case, there will be a reduction in the Q.E for shorter wavelengths due to front surface recombination. Also, for longer wavelengths, low absorption of the light and short diffusion length of the generated charge carriers will reduce Q.E. Moreover, reflection losses and poor collection of generated carriers will result in a decrease of the Q.E along the whole spectrum.

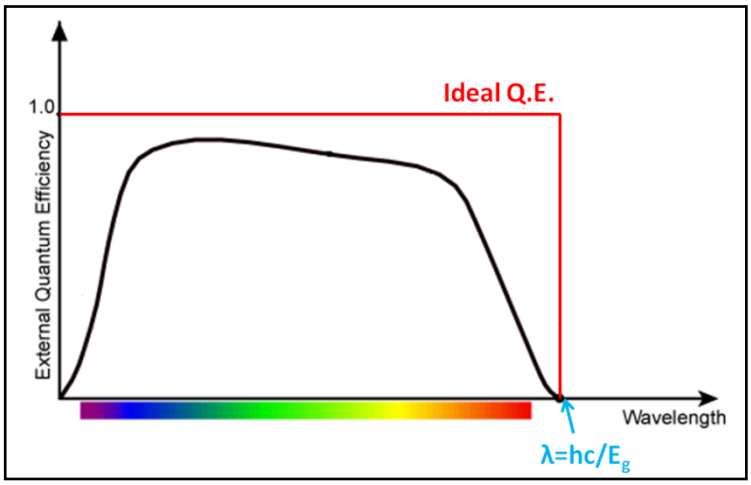


Figure 11: External quantum efficiency of a silicon solar cell [13]

For External Quantum Efficiency (E.Q.E.), optical losses like reflection and transmission are taken into consideration. For Internal Quantum Efficiency (I.Q.E.), on the other hand, optical losses are excluded from the calculation.

Spectral Response

Spectral response (S.R.) is another parameter similar to Q.E. defining the cell performance. S.R. whose mathematical form is given below could be expressed as the ratio of the current generated by the solar cell to the power incident on it.

$$Spectral\ Response\ \left(\frac{A}{W}\right) = \frac{q\lambda}{hc}\ QE = = \frac{QE}{\lambda(nm)} x1239.8 \qquad (Eq.9)\ [2]$$

CHAPTER 2

FUNDAMENTALS OF CRYSTALLINE SILICON SOLAR CELL TECHNOLOGY

2.1. Silicon Wafer Production

Standard crystalline Si solar cell is a device consisting of a single p-n junction as the active layer where generated electron-hole pairs and separated from each other with the help of the induced electric field at the junction region, anti reflection coating (ARC) on top to reduce reflection losses, top and bottom contacts to collect generated charge carriers as shown in Figure 12. Crystalline Si solar cells are fabricated on 180- 200 μm thick Si wafers with mono or multi-crystalline structures. The wafer quality plays an important role in the solar cell performance.

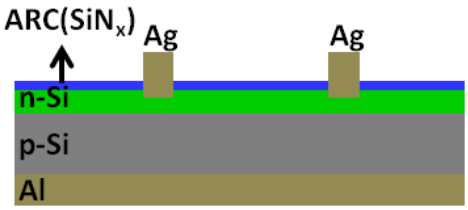


Figure 12: Cross-sectional view of a standard Si solar cell

In order to fabricate high quality crystalline wafers, Si existing as silica (impure SiO_2) and silicates (Si+oxygen+another element) in the Earth's crust has to be converted into its pure, device quality form. For this, high temperature purification steps shown in Figure 13 have to be followed.

Purification process starts with heating silica with Carbon (C) in a furnace. During this process, silica and carbon (in coal form) undergo a chemical reaction where Oxygen (O) which is already attached to Si in impure SiO_2 structure will be pulled away by C atoms leaving impure Si behind. This form of Si is known as "*Metallurgical Grade Silicon (MGS)"*.

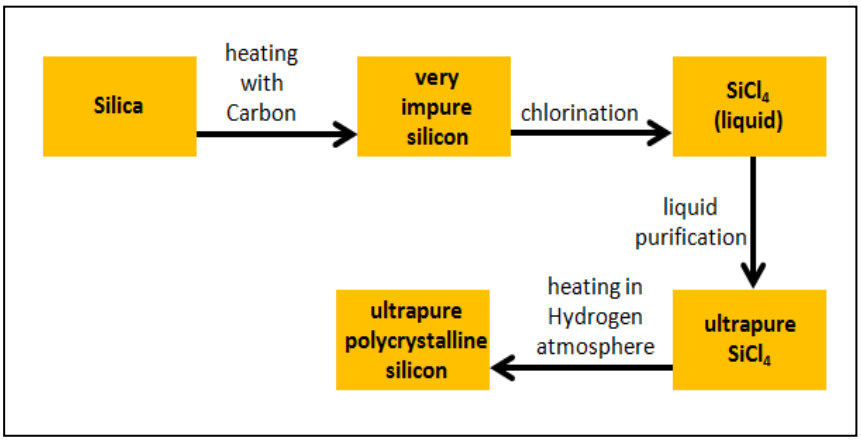


Figure 13: Summary of Si purification process Process

Next, MGS will be chlorinated to form $SiCl_4$ or $SiHCl_3$ both of which will be liquid at room temperature. After multiple distillation and liquid purification steps, ultrapure $SiCl_4$ will be obtained. Then, by heating the obtained ultrapure halide in Hydrogen (H_2) atmosphere, ultrapure polycrystalline Si will be reached. Once ultrapure form of Si is obtained, wafers of different properties could be fabricated by using different techniques.

"Czochralski (Cz)" is a crystal production technique commonly used in Si industry. In this technique, a single crystal seed is used to obtain single crystal ingot from already melted polySilicon being held at around 1417^oC in a quartz crucible. Pulling and rotating the seed material very slowly allows the existing melt to crystallize corresponding to the structure of the seed. During the growth, quartz crucible behaves as a sink of contaminants so that O and C amounts present in the pulled crystal will lie around 10^{18} and 10^{16} cm^{-3} respectively [14].

In order to avoid contamination coming from the crucible, *"Float Zone (FZ)"* method has been developed. In this method, an already produced single/multi crystal rod is held at its ends to be refined by an RF heating coil passing over the rod. As the coil passes, it melts the rod locally and that locally melted regime will recrystallize corresponding to the seed placed at the bottom of the rod. Since there exists no interaction between the rod and its surrounding, contaminant amount is reduced significantly for FZ-wafers. Typical O and C concentrations of FZ-wafers lie below $5x10^{15}$ cm^{-3} [14].

In addition, Si could also be produced in form of poly-crystalline chunks to be used as source material in thin film deposition processes. Si chunk production processes are less complicated compared to ingot growth and *"Siemens Method"* is a famous technique where $SiHCl_3$ gas is fed to the reaction chamber together with H_2 to obtain HCl and Si as reaction products. Within the reaction chamber, U-shaped Si rods are placed and heated up to 1000^oC. Si obtained as the product during the reaction will stick onto these heated Si rods. When the obtained U-shaped bars are pulverized, poly-Si chunks will be obtained [15].

Si ingot growth is followed by wafering process where obtained bulk crystal would be cut into small pieces of different thicknesses and different diameters with a diamond or a wire cutter.

2.2. Standard Single Crystalline Silicon Solar Cell Production

Si wafers which are produced by one of the production methods mentioned above are used for solar cell fabrication. Both Boron (B) doped p-type and Phosphorous (P) doped n-type Si wafers are commercially available. However, due to complicated nature of Boron diffusion process needed to form p-n junction on n-type wafers and difficulties in back contact formation, p-type wafers are preferentially used as the base material for standard solar cell production in industry. Typical fabrication steps could be summarized as shown below.

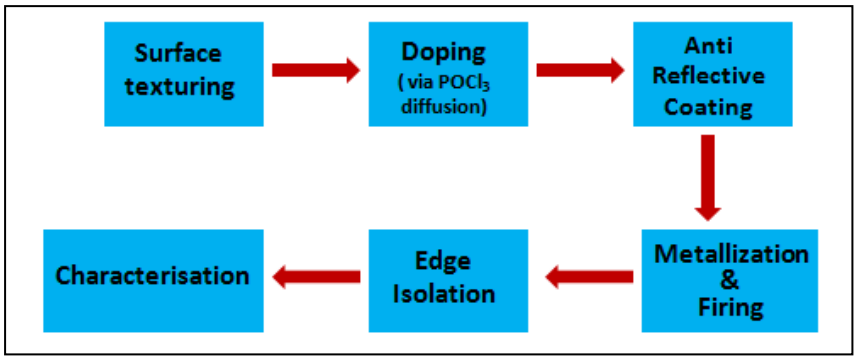


Figure 14: Standard solar cell production

2.2.1. Surface Texturing

Standard Si solar cell is a device with single p-n junction designed to absorb incident light and generate an electron-hole (e^--h^+) pair for each absorbed photon. Thus, as the number of absorbed photons increases, number of generated e^--h^+ pairs will also increase. Considering solar spectrum and absorption spectrum of Si at AM1.5 condition (Figure 12), almost 50% of the incident radiation cannot be utilized by Si [16]. Since Si has a band gap of 1.12 eV corresponding to the wavelength ~1100 nm, photons with less energy than 1.12eV will be insufficient to generate e^--h^+ pairs. So, the loss above 1100 nm shown in Figure 15 is due to un-absorbed photons of incident radiation.

Moreover, although 1.12eV of the photon energy is enough to generate e^--h^+ pairs, excess energy supplied by short wavelength photons, will not be utilized by Si. It will be given as heat to the crystal lattice, instead. Energy transfer to the lattice in form of heat is named as "*thermalization"* and responsible for the loss of energy in the high energy part of the spectrum as shown in Figure 15. Those losses resulting from thermalization and non-absorption of photons could be related to *"spectral mismatch"* of the Si band gap and energy distribution of photons [16].

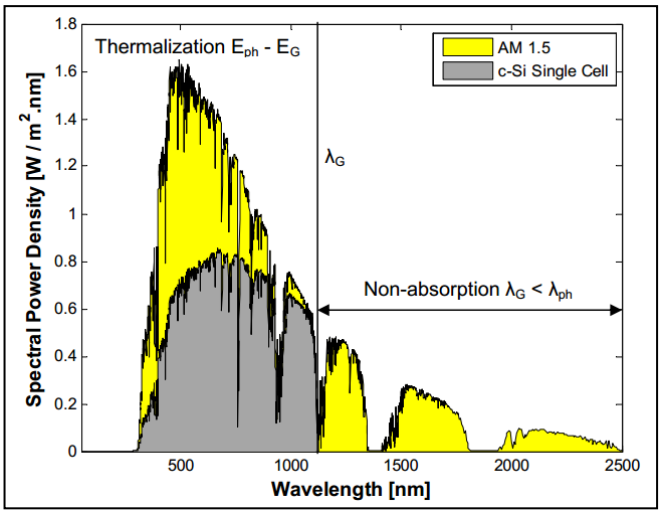


Figure 15: Fraction of AM1.5 spectrum utilized by c-Si [16]

As seen in Figure 15, most of the utilized photons belong to the visible region of the spectrum. However, to be able to absorb photons up to 1100-1200 nm, Si wafer thickness needs to be around 0.1-0.2 cm (Figure 16).

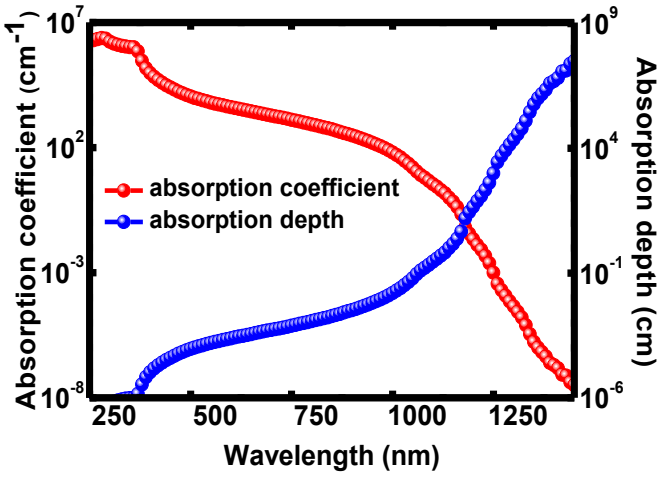


Figure 16: Absorption coefficient and depth of intrinsic Si at 300^{o}K

Although increasing wafer thickness enhances light absorption, it also means longer paths to be travelled by the generated charge carriers before being collected at

the metal contacts. As the path length to be travelled by the generated charge carrier increases, their recombination probability also increases. The distance travelled by the carriers until recombination is named as *"minority carrier diffusion length"*. Diffusion length in an n-doped emitter region is 14μm whereas that value reaches to 140μm in the p-doped base region for doping levels of $1x10^{19}cm^{-3}$ and $1x10^{16}cm^{-3}$ respectively [2, p. 189]. Hence, such short diffusion lengths impose an upper limit for the wafer thickness. Moreover, increased wafer thickness also increases production cost which is undesirable for the manufacturers. Thus, wafer should be thick enough to absorb as much light as possible and simultaneously thin enough to provide effective carrier collection and low cost. Light trapping approaches have been is developed as a solution for that tradeoff between absorption and carrier collection.

Optical path length is the distance travelled by an unabsorbed photon before escaping out of the device. Light trapping concept is applied to make this optical path several times longer than the actual device thickness. With the help of light trapping, a mechanically thin but optically thick device could be obtained. One of the most effective and practical light trapping methods is based on texturing the surface of Si wafer, which can be obtained by wet chemical etching.

Surface texturing can be easily obtained in a dilute alkaline solution which selectively etches Si surface at temperatures around 75-80^{o}C. Generally KOH or NaOH is used for alkaline solution and certain amount of isopropyl alcohol (IPA) is added to the solution to make chemical reaction more *selective* (surface orientation dependent). With this process, the wafer surface is ultimately transformed from a flat structure to a pyramidal surface. As the concentration of KOH or NaOH increases, selectivity of the reaction decreases and wafer's surface is isotropically etched resulting in a shiny surface, instead of random pyramid formation. The etch rate is determined by rate of two mechanisms. One is the rate of reaction taking place at the surface and the other is the diffusion rate of reactants into the surface [17]. IPA addition to the alkaline solution enhances the surface diffusion resulting in a rapid etching.

Different reaction mechanisms have been proposed to describe the texturing process.

According to one proposal, KOH/NaOH molecules react with Si atoms on the surface and a potassium/sodium (K/Na) including silicate which is soluble in water (H_2O) will be produced accompanied by H_2 gas emission [17]. Chemical reaction taking place in this process is given as;

$$Si + 2KOH + H_2O \rightarrow K_2SiO_3 + 2H_2 \qquad (Eq.10\ ^{[16]})$$

Since reaction rate will be different along different crystallographic directions due to different linear atomic densities, etched Si amount will be different for each direction. Etching is faster along (110) direction compared to (100) and slowest along (111) direction [17]. For instance, the ratio of etch rates of the KOH given as; (111): (110): (100) ~1:600:400 which means that etch process almost stops when (111) direction is reached.

Si surface texturing process starts with a wafer of (100) orientation. (100) planes are etched much faster than (111) planes and texturing process will be completed when all planes have (111) orientation as shown in Figure 17. At the end all surface will be covered by square based pyramids of 7-10µm height.

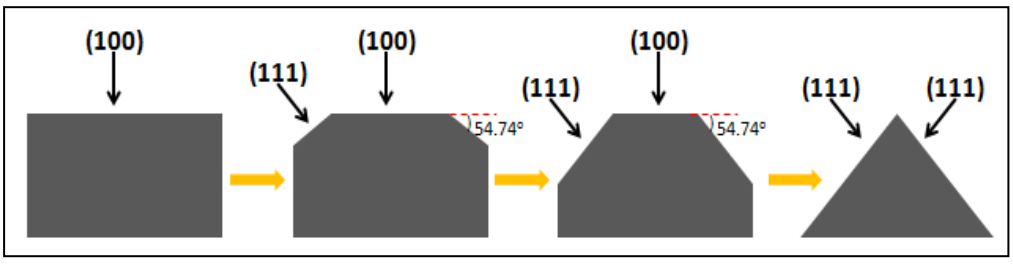


Figure 17: Etching process of (100) Si

Unlike flat surfaces, pyramid covered surfaces provide the incident light to interact with the surface more than once. More interaction with the surface increases the optical path length so postpones the escape of unabsorbed light outside the solar cell, thus, provides light trapping (Figure 18).

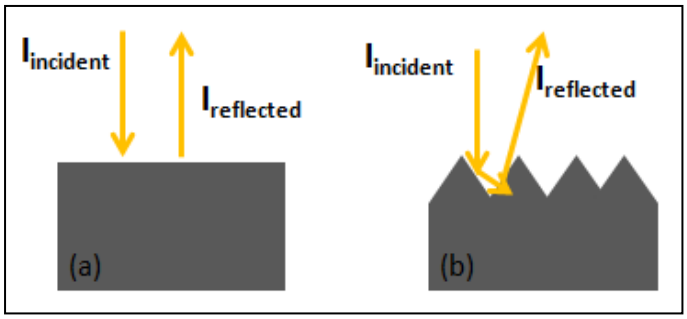


Figure 18: Reflection from a flat surface (a) and textured surface (b)

In the case of flat surface, if the incident light hits the surface with an intensity of $I_{incident}$, it will be reflected from the surface once and leave the surface with an intensity of R multiple of $I_{incident}$ as expressed in Eq.11. When the incident beam is reflected twice as in the case of pyramids shown in Figure 18-(b), the reflected beam intensity will be equal to R^2 times I as expressed in Eq.12. Since R is the surface reflectance and takes numerical values between 0 and 1, after successive reflections from the surface, reflected beam will leave the surface with a very small amount of intensity.

$$I_{reflected} = I_{incident} \times R \qquad (Eq. 11)$$

$$I_{reflected} = I_{incident} \times R^{2} \qquad (Eq. 12)$$

2.2.2. Doping

Doping is another critical step where active region of the solar cell is formed. In this step, p-n junction is created via solid state diffusion. Since the standard process of the solar industry is based on n-doping of the p-base wafers, Phosphorous (P) diffusion is worth of being discussed in details.

In the most general sense, doping is the way of changing electrical properties of a semiconductor material via intentional addition of impurity atoms into the crystalline lattice. Since the impurity atom has to replace a lattice atom, energy has to be supplied to the system in order to kick-off a lattice atom from its stable position via breaking its bonds and to reform bonds between the other lattice atoms and the impurity atom. This can be accomplished by a high process temperatures ~800-900^{o}C as in the case of solid state diffusion.

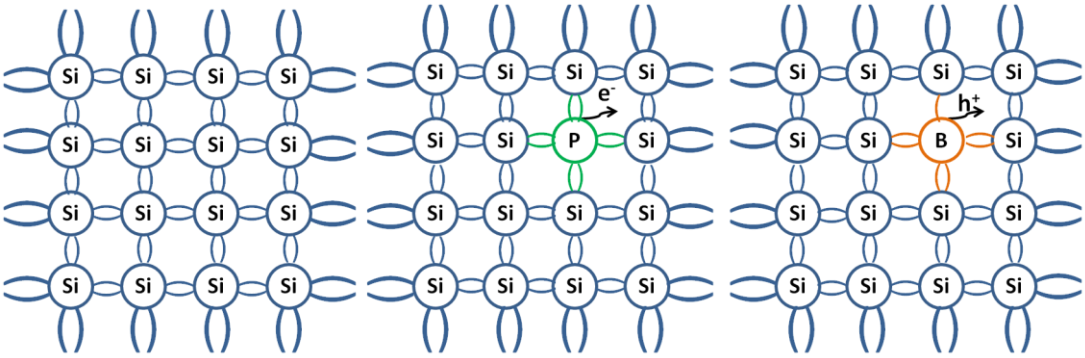


Figure 19: Crystal structure of intrinsic Si (a), phosphorous Si (b) and boron doped Si (c)

As being a member of Group IV-A of the periodic table, Si makes four covalent bonds in its intrinsic structure. It means that each Si atom will make bonds with its four nearest neighbors. When a Phosphorous atom is added to the system for n-type doping, as being a Group V-A element, P has five valence electrons four of which will be bonded to the nearest Si atoms and the fifth electron will be weakly bonded to P atom. That weakly bonded electron is easily freed to move throughout the lattice even at room temperature which consequently enhances the conductivity. Thus, more free electrons will result in higher conductivity.

On the other hand, Boron has three valence electrons as being a Group III-A element. Thus, Boron shares all its three electrons with the host atoms and there will be a missing electron which is equivalent to an additional hole, in the structure. Each

additional hole will also increase the conductivity of the material since holes are charge carriers.

In a standard solar cell structure n-doped layer is formed on the surface of a p-doped wafer via solid state diffusion. When p-doped and n-doped material is in physical contact with each other, electrons will flow from n-side towards p-side and recombines with holes there. Similarly, holes will flow from p-side for recombination with the electrons As a result of this diffusion-recombination process, electrons leave positively charged P^+ ions on the n-side whereas holes leave negatively charged B^- ions on the p-side of the junction as illustrated in Figure 20.

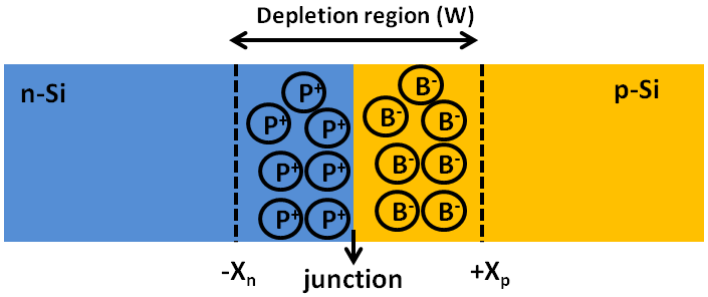


Figure 20: Cross-sectional view of a p-n junction

As a result, an electric field is induced at the junction region pointing from n-side to the p-side. This electric field makes minority carriers to drift across the junction rapidly to the other side they reach the edge of depletion region. In addition, all minority carriers created within a diffusion length distance to the depletion region can reach the junction and collected easily.

In order to understand the device properties, the energy band diagram of the materials should be clearly understood. Schematic band diagrams of p- and n-type Si before junction formation are shown in Figure 21. Fermi level (E_F) will lie close to the conduction band (C.B.) for n-type Si whereas it lies close to the valance band (V.B.) for the p-type.

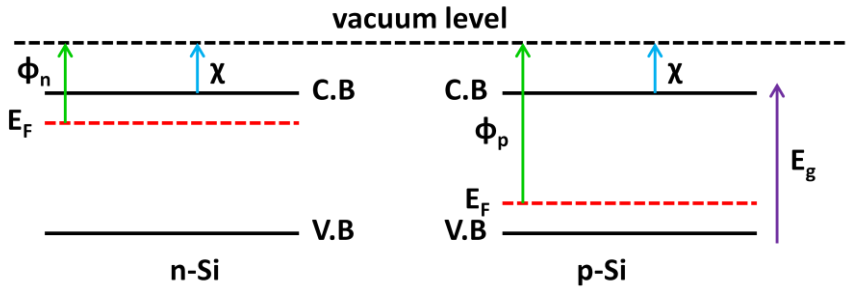


Figure 21: Band diagram of n-Si and p-Si before electrical contact

Here Φ_n and Φ_p are the *work functions*, the energy difference between the vacuum and Fermi level, of n-Si and p-Si respectively. χ stands for *electron affinity* which is the energy difference between bottom of the C.B. and vacuum level.

When p-Si and n-Si are brought into contact via junction formation, conduction and valence bands will bend due to the difference between in work functions. However, at thermo-dynamical equilibrium with no current flow across the junction, the Fermi level should be constant across the device. With this requirement, the difference in the work functions results in a potential barrier formation at the junction in shown in Figure 22.

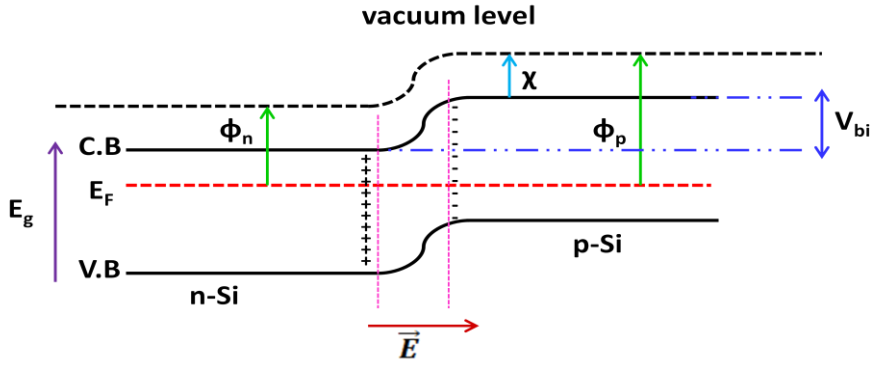


Figure 22: Band diagram of the system after p-n junction formation

In a standard solar cell structure, n-doped layer is formed on a p-doped Si wafer via solid state diffusion process. For this purpose, Phosphorous containing liquid $POCl_3$ is sent into a tube furnace at a temperature ~850^{o}C. $POCl_3$ is carried into the furnace by a carrier gas (N_2) and heated before entering into the tube. While P containing gas is fed in the system, O_2 gas is also supplied to form P_2O_5 according to following reaction;

$$4POCl_3(g) + 3O_2(g) \rightarrow 2P_2O_5(g) + 6Cl_2 \qquad (Eq.13)^{[18]}$$

This reaction takes place in the predeposition step of the diffusion process. After predeposition, the drive-in step is followed in which flow of $POCl_3$ is suppressed and deposited P_2O_5 reacts with Si to form SiO_2 on the surfaces of wafer. Formation of SiO_2 releases P atoms and allows them to diffuse into the Si via the following reaction;

$$2P_2O_5(g) + 5Si(s) \rightarrow 5SiO_2(s) + 4P(s) \qquad (Eq.14)^{[18]}$$

In addition to SiO_2 formation on the surface, P_2O_5 reacts with SiO_2 and phosphorous silicate glass (PSG) is formed as the product of the reaction by following the below equation

$$xSiO_2 + yP_2O_5 \rightarrow xSiO_2.yP_2O_5 \qquad (Eq.15)^{[18]}$$

During the drive-in step, freed P atoms have to penetrate both through PSG and SiO_2 layers formed on the surface in order to reach underlying Si wafer. Although P in Si will be redistributed near the growing SiO_2 on the surface, due to relatively low diffusivity of P in SiO_2 compared to that in Si, diffusion in SiO_2 will not affect the redistribution of P atoms in Si significantly [19]. Moreover, n-dopants like P and As are rejected by SiO_2 and pile up at the Si surface [20]. In drive-in step, changing O_2 flow rate will change Phosphorous content in PSG glass which in turn affects the

surface concentration in the emitter region. At the end of drive-in step, P atoms will replace Si atoms at the lattice sites so that initially p-type regions are converted into n-type.

Modeling

Solid state diffusion modeling is based upon one dimensional flow of the atoms in the absence of convection. Basic theory of diffusion was developed by Fick in 1885 [14] who assumed that in a dilute liquid or gaseous solution, solute atom transfer per unit area for one dimensional flow could be expressed as in the following equation.

$$J = -D\frac{\partial C(x,t)}{\partial X} \qquad (Eq.16)\ ^{[20]}$$

- *J* is the diffusion flux which is defined as the amount of solute transferred per unit area per unit time and has the units of $mol/cm^2.s$.
- *D* is diffusion coefficient or diffusivity of the material defining how easily an atom could move throughout a known medium. Diffusivity defined with the units of cm^2/s ,changes as a function of temperature and concentration.
- *C(x,t)* is the concentration of atoms per unit volume of the medium and defined with the units of mol/cm^3.
- $\frac{\partial C(x,t)}{\partial X}$ is known as the concentration gradient which is the driving force of the diffusion process.

Eq.16 is named as *Fick's 1st Law of Diffusion* in mass transfer. The negative sign in the equation states that the matter flows in the direction of decreasing solute concentration so that the defined concentration gradient is negative. Also, *continuity (i.e., conservation of matter)* imposes that within a very small volume of the system, spatial change in diffusion flux must be equal to the change in solute concentration per unit time as expressed in Eq. 17:

$$\frac{\partial J(x,t)}{\partial X} = -\frac{\partial C(x,t)}{\partial t} \qquad (Eq.17)^{[20]}$$

Inserting Eq. 17 into Fick's 1st Law results in *Fick's 2nd Law of Diffusion* for one dimensional flow as expressed in Eq.18 below.

$$\frac{\partial C(x,t)}{\partial t} = -\frac{\partial}{\partial X}\left[-D\ \frac{\partial C(x,t)}{\partial X}\right] = D\frac{\partial^2 C(x,t)}{\partial^2 X} \qquad (Eq.18)^{[20]}$$

Solving Eq. 18 for different initial and boundary conditions will correspond to different practical cases.

For example, constant source concentration at the surface corresponding to the initial condition *C(x,0)* = 0 and boundary conditions *C(0,t)*= C_s and C(∞,t) =0 leads to a solution in the form of *complementary error function* as expressed in Eq. 20 below where C_s is the surface concentration of dopant atoms.

$$C(x,t) = C_s erfc\left(\frac{x}{2\sqrt{Dt}}\right) \qquad (Eq.19)^{[20]}$$

Constant surface concentration corresponds to predeposition step of the diffusion process where dopant including process gas is fed to the system with a constant flow rate.

After predeposition step, the drive-in is followed where a thin layer of dopant atoms is already present on the wafer surface. A total Q_T amount of dopant per unit area will diffuse into the Si with the initial condition *C(x,0)* = 0 and the boundary conditions $\int_0^\infty C(x,t) = Q_T$ and C(∞,t) =0. The resultant solution satisfying the initial and boundary conditions will be in the form of *Gaussian distribution function* whose mathematical expression is given in Eq.20 on the next page.

$$C(x,t) = \frac{Q_T}{\sqrt{\pi D t}} exp\left(\frac{-x^2}{4Dt}\right) \qquad (Eq.20)$$ [20]

2.2.3. Anti Reflective Coating (ARC)

Anti Reflective Coating (ARC) is the thin layer of dielectric material applied onto the surface of a solar cell to reduce the reflection. The application of ARC on the solar cells increases the number of photons to be absorbed so as the number of generated carriers. Ultimately output current and efficiency of the cell increase. However, for an efficient AR action, ARC is properly applied to the surface.

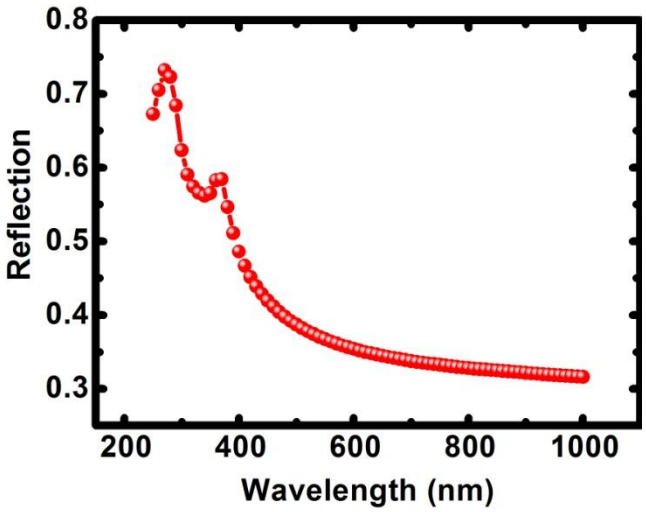


Figure 23: Reflection spectrum of bare silicon

Considering the reflection spectrum of bare Si shown in Figure 23, it could be deduced that almost 30 % of the visible regime of the incident light is reflected back from the surface. Reflection is due to difference between the refractive indices of different media that the light interacts with. If the incident and reflected light are in phase; then, they will interfere constructively and a certain amount of the incident light will be reflected back.

If the incident and reflected light are out of phase, they will interfere destructively so that reflection will be decreased. For wafer based Si solar cells, silicon nitride (Si_3N_4 and/or SiN_x) layers are used as anti reflective coating. For normal incidence condition, thickness of the nitride layer is adjusted in a way that, light reflected form the top of nitride layer will be separated from the light reflected from Si- Si nitride interface by a phase difference equal to π/2 [2, pp. 260–262]. Dielectric constant of a solid could be expressed as in the following equation:

$$\sqrt{\varepsilon_s} = n_s - i\kappa_s \qquad (Eq.21)\ [1]$$

Where,ε_s is the *dielectric constant* of the solid, n_s is the *real part* and κ_s is the *imaginary part* of the refractive index of the material [2, pp. 260–262]. Moreover, κ_s could be related to the absorption coefficient of the material as expressed in Eq.22 below.

$$\alpha = \frac{4\pi\kappa_s}{\lambda} \qquad (Eq.22)\ [1]$$

The reflection probability or *reflectance* of the surface for the light travelling form a medium of refractive index n_0 towards the medium of refractive index n_s at normal incidence could be expressed as shown in Eq. 23:

$$R = \left(\frac{n_0 - n_s}{n_0 + n_s}\right)^2 \qquad (Eq.23)\ [1]$$

When ARC is deposited as an additional layer between air and the Si surface, reflectivity of the film for the light of wavelength λ could be expressed as in the following equation;

$$R = \frac{(n_0 - n_s)^2 + \left(\left(\frac{n_0 n_s}{n_1}\right) - n_1\right)^2 tan^2\delta_1}{(n_0 + n_s)^2 + \left(\left(\frac{n_0 n_s}{n_1}\right) + n_1\right)^2 tan^2\delta_1} \qquad (Eq.24)\ [1]$$

where δ_1 is the phase shift in the film of the thickness d_1 and could be expressed as in Eq.25.

$$\delta_1 = \frac{2\pi n_1 d_1 cos\theta_1}{\lambda} \qquad (Eq.25)\ [1]$$

θ_1 is the angle between the light ray and the normal of the film surface.

Considering Eq.24, it could be clearly seen that *R* takes its minimum value when $\delta_1 = \pi/2$. In order for this condition to be satisfied, d_1 has to be equal to a quarter wavelength in the dielectric film [2]. Then, the light reflected from rear and front sides of the thin film will be out of phase so interfere destructively [2]. *R* could also be minimized when the following equation is satisfied.

$$n_1 = \sqrt{n_0 n_s} \qquad (Eq.26)\ [1]$$

Thus, for the light from air with n_0=1 towards Si with n_s=3.3 at 632nm optimum refractive index of ARC layer n_1=$\sqrt{3.3}$ ≅ 1.81 which can be provided by Si_3N_4. Since, thickness will minimize reflection at one specific wavelength, that wavelength will stay in red regime where solar radiation is maximum. Due to reflection in UV regime, standard Si solar cells appear blue or violet Moreover, the Sun has a surface temperature ~5760 K corresponding to ~500 nm as expressed in Eq. 27, known as Wien's Law, the thickness of the ARC film has to be chosen to minimize the reflection at this specific wavelength.

$$\lambda_p(\mu m) = \frac{2900}{T(K)} = \frac{2900}{5760} = 0.503 \mu m \qquad (Eq.27)$$ [1]

Then, applying Eq.25 for $\delta_1 = \pi/2$, $n_1 = 1.81$ and $\lambda_p = 503nm$, d_1 is calculated as ~70 nm for minimum reflection. Thus, ~70 nm of Si_3N_4 layer will reduce the reflection losses.

2.2.4. Metallization

Metallization is the process where metal contacts are patterned on both front and rear surface of the standard solar cells. This step starts with screen printing and successive drying of front Ag and rear Al contact. Then, a high temperature firing is necessary to obtain back surface field and to provide Ag diffusion through the Si_3N_4 layer for contact formation with the Si substrate. During the firing process, Ag diffusion takes place just after the front SiN_x layer is etched by the frit content of the paste.

When the p-n junction is exposed to light, minority carriers will be generated throughout the device. Charge carriers created in the depletion region and within the diffusion length distance from the depletion region will be collected with the help of electric field formed at the junction region. These carries are then fed to an external load as electrical current. In order to enhance carrier collection, electrical field at the metal- Si contacts is also needed in addition to the electrical field provided by the p-n junction.

When a metal and a semiconductor are brought into electrical contact, a Schottky or an Ohmic contact is formed at the junction region depending on the work functions of contacted materials. In case of Schottky contact formation, a potential barrier is built up at the junction region which will resist current flow in one direction while allowing in the other direction. For Ohmic contact formation, on the other hand, current flow is allowed in either direction. Although Schottky contacts could

be used as rectifying contacts under bias for some specific applications, Ohmic contacts are needed for many applications including solar cells.

Schottky Contact

When a metal with a work function of Φ_m is brought into an electrical contact with a semiconductor with a work function of Φ_s, charge transfer will take place until Fermi level (E_F) reaches its equilibrium position.

For an n-type semiconductor, Schottky contact will be obtained when $\Phi_m > \Phi_s$. Since the work function of the metal is greater than that of semiconductor, before the contact formation. E_F of semiconductor will lie above E_F of the metal as shown in Figure 24 where Φ_n is corresponding to the work function of n-type Si

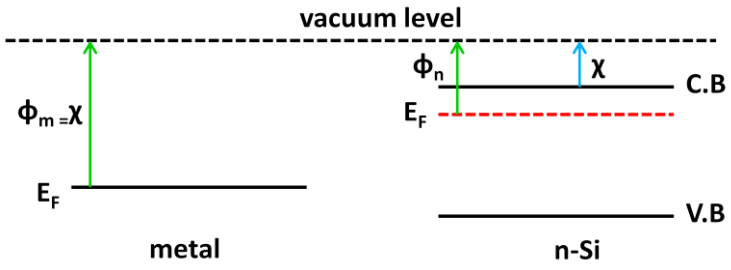


Figure 24: Band diagrams of metal and n-Semiconductor before physical contact

After physical contact is established, a charge transfer will occur and conduction /valance bands of semiconductor will bend downwards to prevent further electron diffusion from semiconductor to metal. A potential barrier called Schottky barrier (Φ_b) is formed at the junction to prevent electron flow as illustrated in Figure 25. Fermi level alignment is reached by raising the electrostatic potential at n-side, and negative charges will be induced at metal side due to uncompensated positively charged donor ions at n-side.

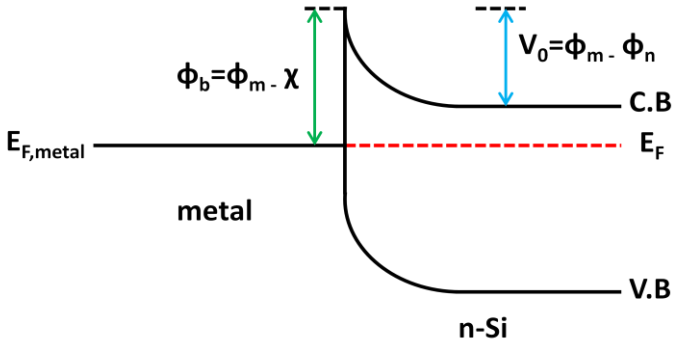


Figure 25: Band diagram of metal-n-Semiconductor junction after physical contact

For a p-type semiconductor, $\Phi_s > \Phi_m$ is the necessary condition to form a Schottky barrier. In this case, the band bending at the semiconductor side will be upwards and the potential barrier forming at the metal side will prevent hole movement between two sides.

Ohmic Contact

A metal-semiconductor junction with no or a negligible potential barrier is called Ohmic junction. In this case, *I-V* characteristic linear and independent from the polarity of the applied voltage [21].

For an n-type material to obtain Ohmic contact, $\Phi_s > \Phi_m$ condition should be satisfied whereas $\Phi_m > \Phi_s$ condition is needed for p-type material. Since $\Phi_s > \Phi_m$, initially E_F of n-material will lie above that of metal as shown in Figure 26.

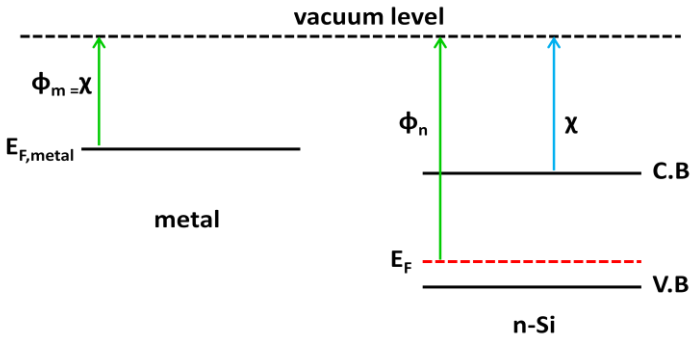


Figure 26: Band Diagram of metal and n-Semiconductor before physical contact

After the physical contact of the metal and n-type semiconductor, electron energies at n-side to be raised, so that, bands of the semiconductor will bend upwards as illustrated in Figure 27.

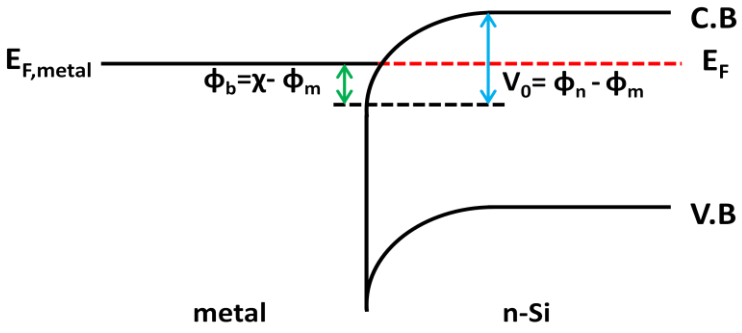


Figure 27: Band diagram of metal & n-Semiconductor after physical contact

If the Fermi level condition explained above cannot be maintained, Ohmic contacts can be formed by heavily doping the underlying Si surface. In this case, the current flows through the junction by tunneling mechanism easily because of narrow barrier and high electric field at the junction.

As mentioned before, solar cell is a device requiring top and bottom contacts to be Ohmic. For the standard p type based Si solar cells, Al is used as the back contact whereas Ag is used as the front contact to obtain Ohmic behavior.

2.2.5. Edge Isolation

After successive application of texturing, doping, anti-reflective coating and metallization steps as described in the flow chart shown in Figure 28, solar cell fabrication process will end up with the edge isolation which is another industrialized process step. It is applied to provide electrical isolation between the front side and rear side of the cell in order to avoid electrical shorts.

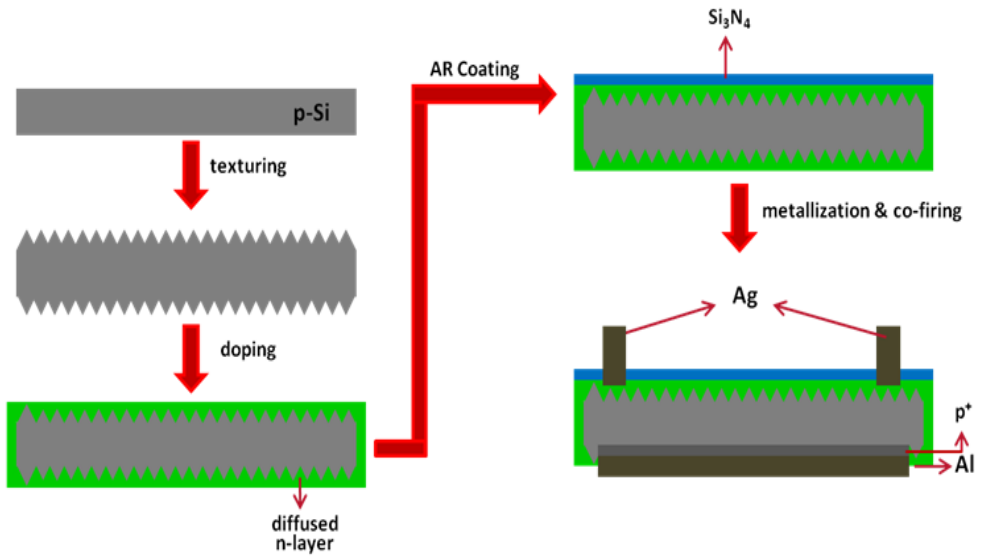


Figure 28: Fabrication process of standard Si solar cell

The electrical short is generated as a result of doping process of the base Si wafers. During $POCl_3$ diffusion, in addition to front surface of the wafer, its edges and rear side will also be phosphorous doped. Rear side of the wafer is converted to highly doped p-layer during the metallization step as a result of large amount of Al incorporation into the n-doped layer formed during POCl3 process. However, edges

of the rear side and rear side are not covered with Al remains as n-type and pose possible paths for generated minority carriers during operation. As shown in Figure 29, generated electrons could directly flow to the p-side at the edges of the wafer; instead of being collected at an external load.

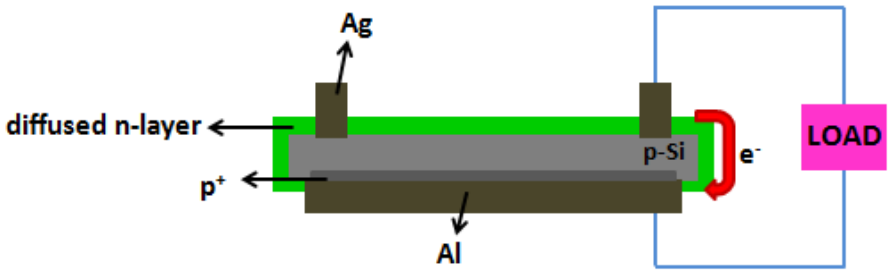


Figure 29: Operation of a Si solar cell before edge isolation

To be able to avoid electrical short problem, front side of the cell should be isolated from the rear side. That isolation could be obtained either via chemical/plasma etching or by laser ablation. At the end of chemical/plasma etching process, n-doped layer at the rear side and at the edges of the wafer will be completely removed. So that, there will be no contact possibility of n-layer to p-layer.

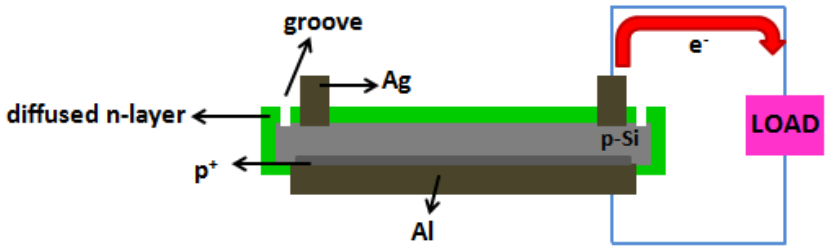


Figure 30: Operation of a Si solar cell after edge isolation by laser ablation

Alternatively, shallow grooves could be opened on the front surface of the wafer by using a laser, so that the only possible path for generated carriers will be the external load circuit as illustrated in Figure 30.

CHAPTER 3

A SINGLE STEP DOPING TECHIQUE FOR SELECTIVE EMITTER SOLAR CELLS AND PASSIVATION TECHIQUES FOR BETTER CELL PERFORMANCE

3.1. Selective Emitter Cell Concept

Standard Si solar cell technology based on screen printed contacts formed on homogenous emitter surface has an upper efficiency limit around 18.4% [22]. This limitation is related to contact resistances, reflection losses at the front side and recombination losses at both front and rear side of the cell. It will not be possible to reach higher efficiency values unless these losses are eliminated. For this, novel production techniques have been developed and started to be applied for industrial applications. *PERC (Passivated Emitter and Rear Cell), PERL (Passivated Emitter Rear Locally Diffused), IBC (Interdigitated Back Contact), Burried Contact* and *Selective Emitter* cell designs are the ones that have become popular recently. Among these new designs, selective emitter will be focused on throughout this thesis.

Selective Emitter is the concept of having a selectively doped, non-homogenous emitter where regions lying beneath metal contacts are highly doped while metal free regions are lightly doped. For a good emitter contact, dopant concentration must be 10^{19}-10^{20} cm^{-3} for n-type and $10^{17}cm^{-3}$ for p-type silicon with an emitter thickness of >300 nm [23]. Lower dopant concentrations will increase series resistance of the cell which will result in ineffective collection of generated charge carriers so as lower efficiency values. However, increasing dopant concentration will also increase the surface interface trap density, so increase surface recombination velocity thus, deteriorate minority carrier lifetime.

Besides, increasing dopant concentration will also increase the probability of carrier-dopant interaction which increases Auger recombination velocity. Thus, there exists a trade-off between minority carrier lifetime and series resistance of the emitter region. In order to provide low contact resistance while keeping the rest of the emitter region lightly doped selective emitter approach has been developed. In this approach, emitter surface could be selectively doped via several methods like, *emitter etch back, inline selective emitter concept, laser doping*, *doping via diffusion mask* and *ion implantation* [24].

Considering absorption spectrum of Si shown in Figure 16, it could be deduced that more energetic photons are absorbed at the front surface whereas less energetic ones could penetrate deeper along the Si. With the help of selective emitter, less dopant atoms will be present at the front surface between metal contacts, thus, not only surface but also Auger recombination velocity will be decreased. As a result, charge carriers associated with the shorter wavelengths could be more effectively collected which results in enhanced blue response of the solar cell. Consequently, 0.6-0.9% absolute increase in the conversion efficiency could be obtained [25].

3.2. Fabrication Methods of Selective Emitter Cell

3.2.1. Emitter Etch Back

Emitter etch back is a method used for selective emitter solar cell fabrication which makes it possible to fabricate selectively doped emitter via single step diffusion. For this method, as demonstrated in , fabrication starts with a heavy $POCl_3$ diffusion resulting in a homogenous emitter. Sheet resistance of obtained homogenous emitter will be around 45-60Ω/□ [26]. Then, without removing PSG formed on the surface, etching paste will be screen printed using a printing mask which is patterned as negative of the front Ag mask. After a short thermal treatment at temperatures around 200-250^{o}C, printed paste will be activated and start to etch the underlying PSG layer [26]. Although this short thermal treatment could be done by rapid thermal annealing, standard firing furnaces are preferred by the industry for

high production rates. Etch rate of the printed paste depends on thermal treatment duration.

The longer heating of the etching paste, the more etching of underlying PSG, so the higher sheet resistance values. After etching, cleaning is required to remove paste residues. Then, cleaning is followed by silicon nitride deposition, front and rear side metallization and co-firing of the printed contacts as in the case of standard solar cell fabrication. So that, etching paste printing and post cleaning steps will be added to standard solar cell fabrication. Moreover, since front Ag fingers will be printed over unetched regions, front side metallization needs alignment.

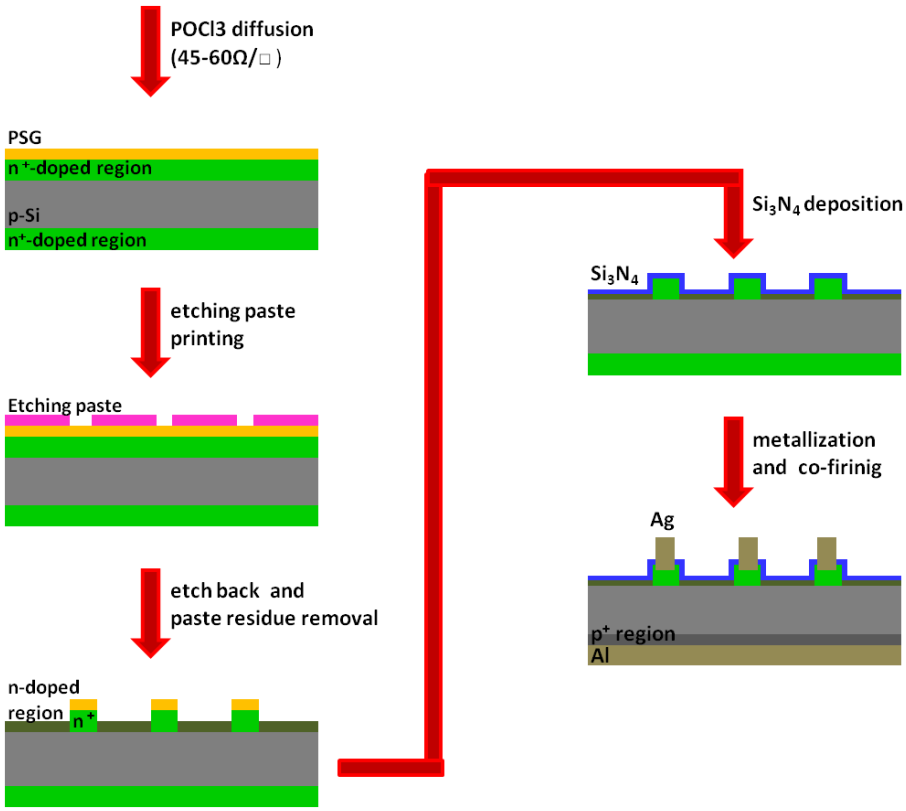


Figure 31: Fabrication process of emitter etch back selective emitter solar cells

Although etching paste could be used for selective etching, photoresist materials could also be used as etching barriers so that in a dilute etchant solution, resist covered regions of formed PSG will be protected whereas uncovered regions will be etched in a controlled manner.

3.2.2. Laser Doping

Selective profile of dopant concentration at emitter surface could also be obtained with the help of a laser beam. For this type of doping, laser pulse could be either applied onto PSG layer before HF dip or on coated Phosphorous source subsequent to a light solid state diffusion.

When PSG layer which is formed as a result of solid state diffusion process, only specific regions will be exposed to laser beam to be more heavily doped compared to the rest of the surface. This additional diffusion provided by laser beam could be attributed not only to the thermal energy induced by laser-matter interaction, but also to the damage given to the wafer surface. Thermal energy will lead to melting and evaporation of underlying Si atoms whereas induced damage will provide additional paths for P atoms standing on the surface so that their possibility to penetrate deeper away from the surface. As a result, without any additional doping step, required doping profile could be obtained.

As summarized in Figure 32, standard $POCl_3$ diffusion is to be adjusted in a way that the resulting sheet resistance will be around 70-90Ω/□. Then laser exposure will reduce this sheet resistance value to 40-50 Ω/□.

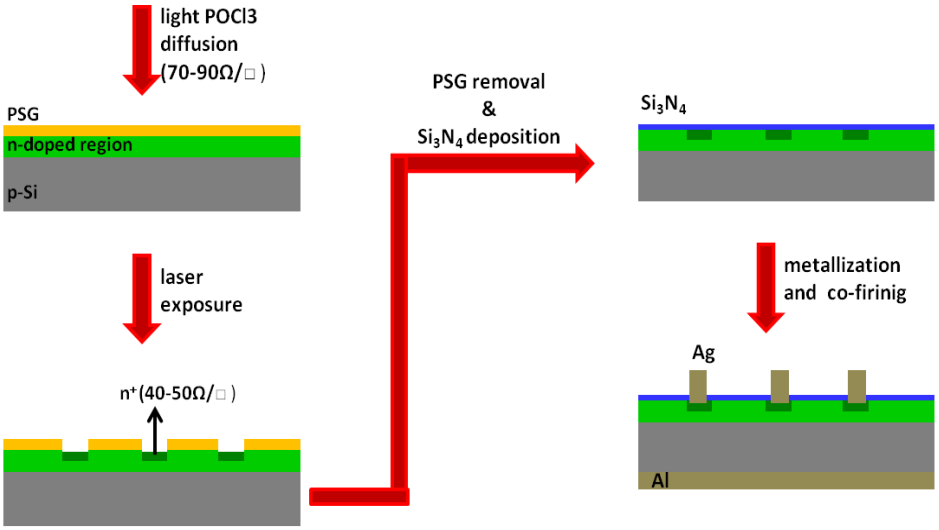


Figure 32: Fabrication process of laser doped selective emitter solar cells with single step doping

Lowered sheet resistance regions will lie beneath the front metal contacts so alignment will be needed for the front side metallization. Control of junction depth and suppression of generated laser damage on the surface could be counted as possible challenges about this process. Selective emitter solar cells fabricated using this technique have been reported to result in a 0.5% absolute increase in efficiency value [27].

On the other hand, the light $POCl_3$ diffusion resulting in 70-90 Ω/□ could be followed by spin coating of a thin layer of doping paste or Phosphorous containing ink. Before spin coating step, formed PSG layer has to be etched. After spin coating and drying of thin dopant layer, Phosphorous atoms will be activated with the help of laser beam resulting in 40-50 Ω/□. At the end of activation, residue of spin coated dopant should be removed. This method whose process flow shown in Figure 33, requires additional steps which makes fabrication process more complicated thus more expensive and time consuming.

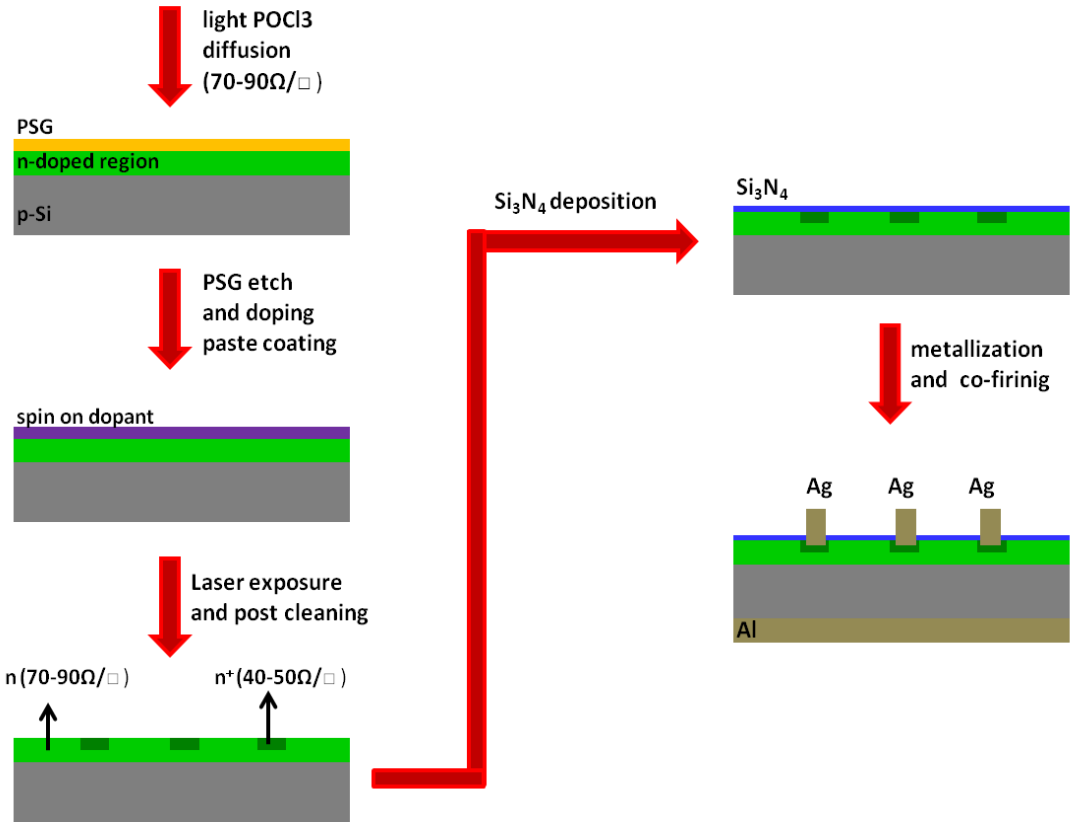


Figure 33: Fabrication process of laser doped selective emitter solar cells with two step doping

Thus, it is not suitable for industrial application. However, above mentioned doping paste and ink could also be screen printed instead of spin coating prior to solid state diffusion so that activation of both doping steps could be done simultaneously [28].

Moreover laser ablation could be carried out after PECVD nitride deposition step [27]. For this method of fabrication, after solid state diffusion, formed PSG is not etched opposing to standard fabrication process. Then, as summarized in Figure 34, PECVD nitride is deposited on top of underlying PSG layer. After that, both nitride and underlying PSG is exposed to laser beam so that nitride layer will be ablated whereas underlying Si region is highly doped.

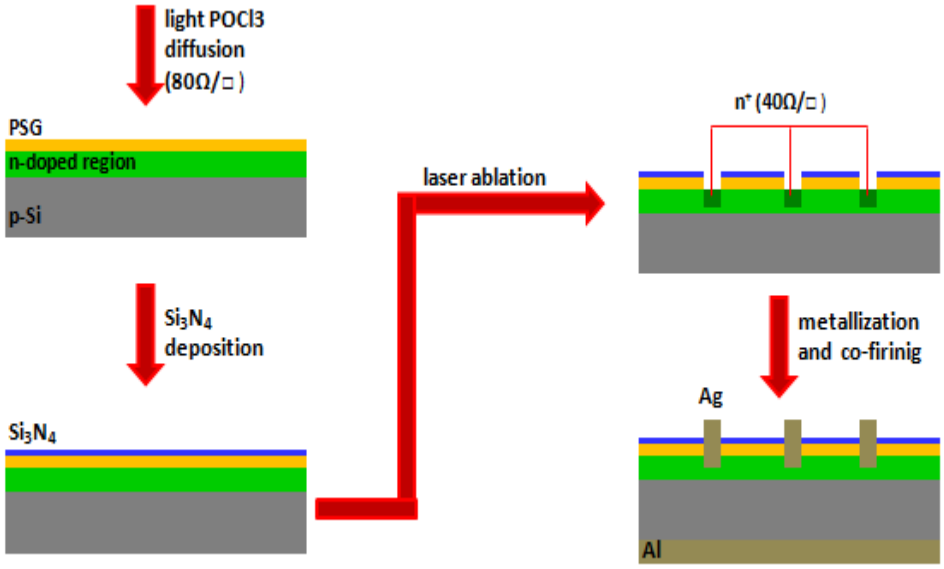


Figure 34: Fabrication process of laser doped selective emitter solar cells with single step doping

Although enhancement in the blue response of the solar cells fabricated by this method is observed, low V_{oc} values are attributed to recombination at the front surface [27]. High amount of P atoms kept in the PSG layer inevitably increases the front surface recombination velocity, thus, limits the efficiency output of the device.

3.2.3. Ion Implantation

Ion implantation is a well known method that has been widely used for microelectronic technology and recently adapted to solar industry. Although ion implantation is a complex doping method compared to solid state diffusion for standard solar cell structure, it provides better dose uniformity, better control of junction depth and profile. Thus, ion implantation could simplify the fabrication of advanced cell structures like PERC, IBC and SE [29]. The greatest disadvantages of these processes are their longer process time and high investment cost for industrial solar cell applications.

However, with the help of new designs improving wafer handling and increasing beam currents, high throughput values ~1000 wafers of 156x156mm^2 per hour have been reached [29].

For selective emitter solar cells, ion implantation could be either applied on lightly doped wafers to form highly doped regions or both high and light doping profiles could be obtained by two successive implantation steps without moving the wafers [29]. For the sake of high throughput, two successive implantation processes will be more favorable. As shown in Figure 35, the process is started with the implantation of whole surface resulting in a high sheet resistance ~100 Ω/□. Then, for the second implantation a proximity mask is placed between the ion beam and the wafer.

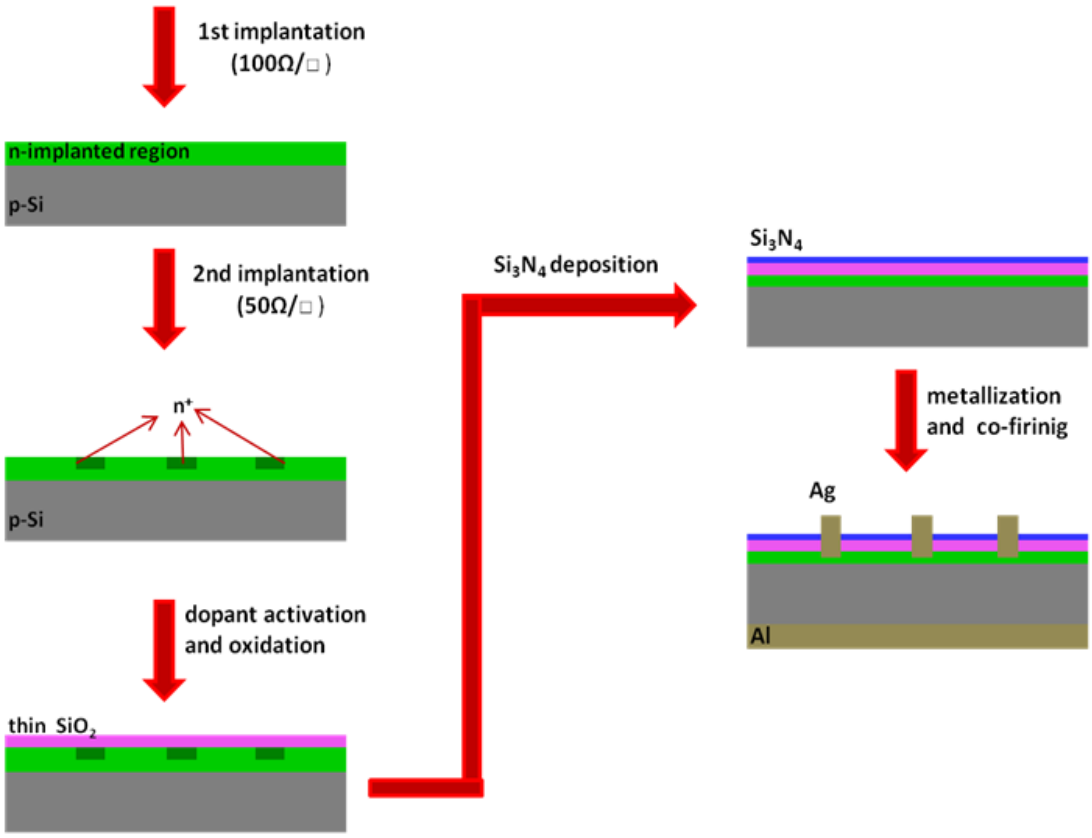


Figure 35: Fabrication process of ion implanted selective emitter solar cells

At the end of second implantation, beam exposed regions, that will lie under front contacts have sheet resistance value of ~50 Ω/□. Due to nature of implantation, an approximately 30 nm thick layer of the surface will be fully amorphized [30]. Thus, in order to activate implanted P atoms and repair the damage on the surface due to ion bombardment, a high temperature annealing step is needed which is carried out in a furnace, at a temperature above 810^{o}C and under N_2/O_2 flow [30]. Moreover, during annealing a very thin SiO_2 layer will be formed on the surface of Si which will provide high quality passivation. After annealing, PECVD nitride deposition, metallization and co-firing will be successively carried out as in the case of standard solar cell fabrication.

Although efficiency values of ion implanted p-base selective emitter solar cells have been reported as 19.6% [29], doping by ion implantation have some challenges. If the dopant atoms are not activated properly or the amorphization is incomplete during implantation, increased surface recombination velocities and higher reverse saturation current values can be observed. Moreover, unlike solid state diffusion, ion implantation does not provide an effective defect gettering which is an important advantage of the $POCl_3$ process. Thus, any contamination coming from base wafers or from other process prior to implantation could have detrimental effect on device performance [29]. As a result, high quality base material is needed, leading to increased production cost. So, despite improvements regarding to process throughput, ion implantation process has still some challenges to be overcome.

3.2.4. Diffusion through a Barrier

In addition to emitter etch back, laser doping and ion implantation processes, selective emitter solar cells could also be fabricated by using a diffusion barrier layer covering the emitter surface. Silicon dioxide (SiO_2), silicon nitride (SiN_x) or even amorphous silicon (a-Si) layers could be applied as diffusion barriers and the main idea for all these is the same. Diffusion barrier to be covered by a convenient process, which will then be patterned according to front side contact design prior to doping and selective doping profile will be obtained via solid state diffusion.

For a-Si case whose fabrication process is demonstrated in Figure 36, a thin layer of amorphous silicon is deposited at low temperature by plasma enhanced chemical vapor deposition (PECVD) or is evaporated by electron beam evaporation technique.

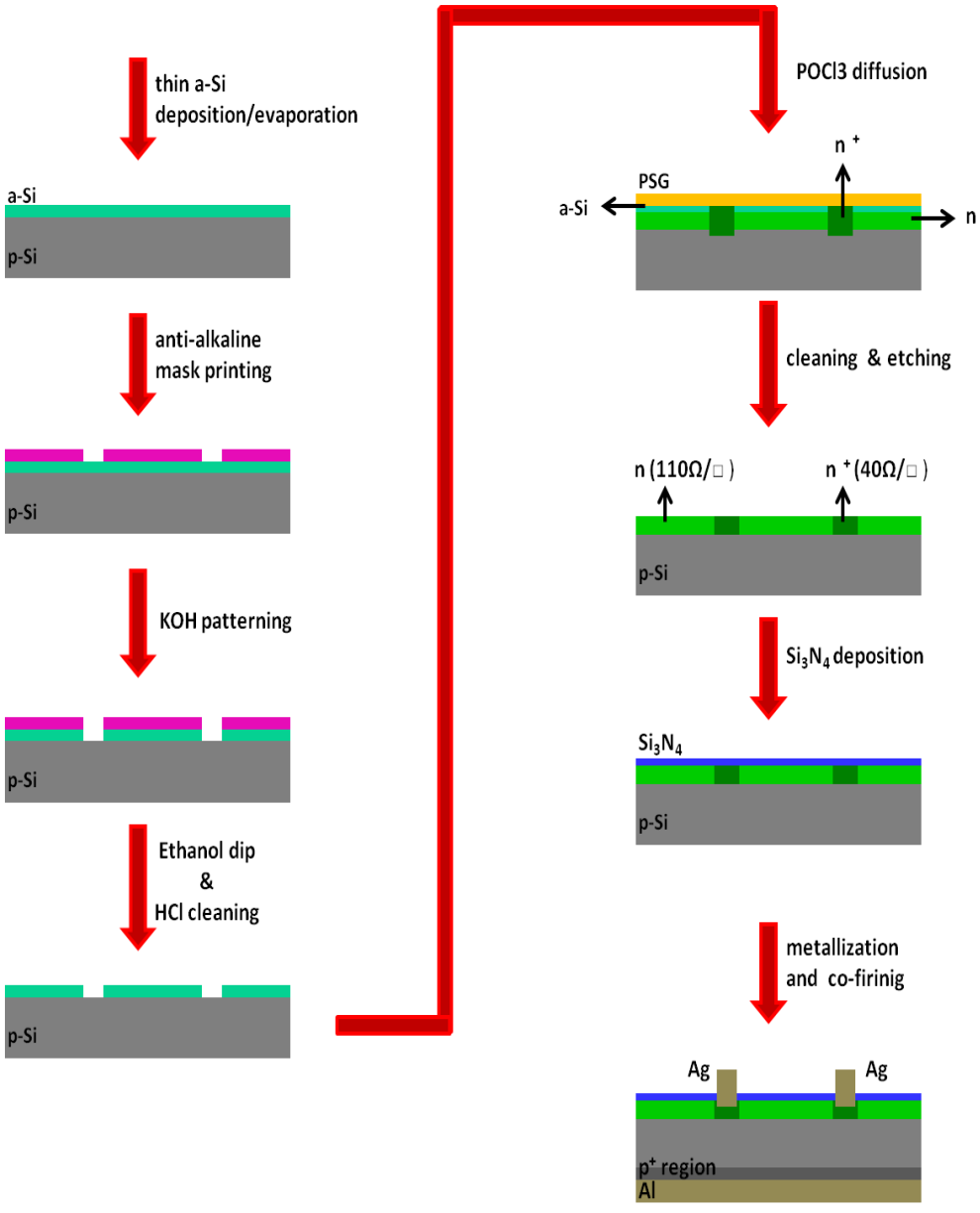


Figure 36: Fabrication process of selective emitter solar cells using amorphous Si diffusion barrier

Then, an anti-alkaline mask layer is screen printed at room temperature with the negative of front contact printing mask. After anti-alkaline mask printing, the wafer will be dipped into KOH solution for patterning, so that a-Si regions uncovered with the anti-alkaline mask will be etched away whereas mask covered regions will be protected against KOH. Then, anti etching mask will be cleaned off by absolute ethanol dip, so that there will be only a-Si layer above the wafer during doping process. In order to remove KOH residues from the surface, an HCl dip will also be required prior to doping. Since phosphorous atoms could penetrate a-Si layer more slowly, less dopant atoms could reach the underlying Si surface. As a result, regions lying beneath the a-Si layer will be lightly doped compared to a-Si etched regions of the emitter surface [31].

During $POCl_3$ diffusion process, a-Si layer will be oxidized, chemical reactions defined by equations 13, 14 and 15 will take place and free P atoms will migrate through underlying Si wafer at the same time. Moreover, a-Si will also crystallize during $POCl_3$ diffusion since it is known that a 30-40 nm thick a-Si would be crystallized within a few minutes at a temperature around 850^oC with a crystallinity of 65% [32]. However, as long as a-Si layer is completely oxidized and PSG layer could penetrate through underlying crystal Si substrate, crystallization of a-Si is not expected to pose a problem. Indeed, when a-Si layer is fully oxidized, it could be completely removed from the surface by HF dip. As a result, depending on the thickness and temperature of doping, high / low level doping concentrations resulting in sheet resistance values around 40 / 110 Ω/□ could be reached by using a-Si layer as diffusion barrier.

Silicon dioxide and silicon nitride are more commonly used as diffusion barrier layers. For both, local openings on the layers could be created by laser ablation or by the application of screen printed etching paste [25].

For silicon nitride (SiN_x) case, a two step doping could be necessary. As shown in Figure 37, a SiN_x layer is deposited on top of wafer prior to high doping which will result in a sheet resistance of 40Ω/□. After being deposited, nitride layer is patterned either by using a laser pulse for selective ablation of the layer or by screen printing of an etching paste. Etching paste requires heat treatment for

activation whose duration determines the etch rate. After selective etching of nitride layer, etching paste residues should be cleaned by water in ultrasonic bath [25]. Nitride patterning is followed by high doping step where only nitride free areas will be doped with a sheet resistance of 40Ω/□. Then, nitride barrier layer will be completely removed by HF dip and a second light $POCl_3$ diffusion resulting in a sheet resistance of 80Ω/□ over the whole emitter surface will be carried out. At the end of second doping, a high / low doping gradient could be reached at the surface so that selective emitter effect would be provided.

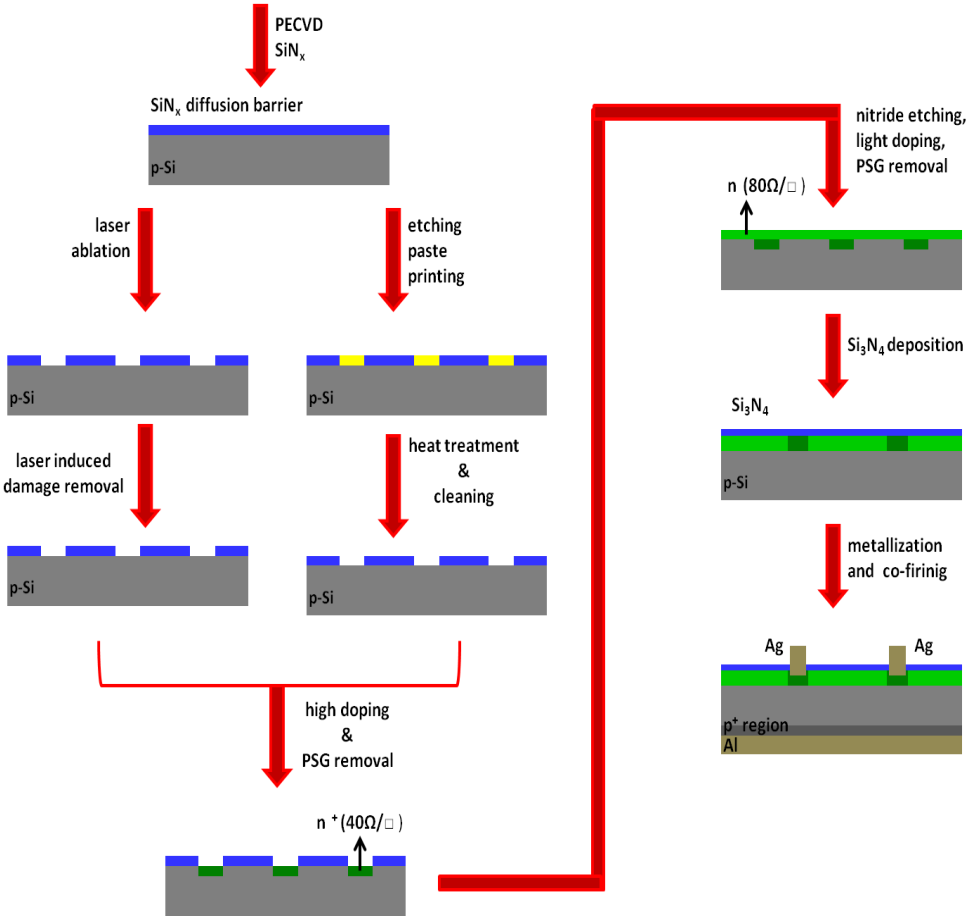


Figure 37: Fabrication process of selective emitter solar cells using silicon nitride diffusion barrier

Although silicon nitride is a commonly used material by the solar industry, patterning it is more difficult compared to that of silicon dioxide due to its resistance against etching [25]. Moreover, since silicon nitride layers are generally deposited at relatively lower temperatures around 350-400^{o}C, high temperatures around 800-850^{o}C reached during doping process would affect nitride's structure resulting in tensile stress generated on the wafer or even end up with decomposition of the layer during doping process resulting in possible contamination of the samples and doping furnace.

Unlike silicon nitride, silicon dioxide (SiO_2) could resist high process temperatures and also could be patterned more easily.

Moreover, phosphorous atoms could penetrate through thin SiO_2 layer and provides doping of underlying surface. Thus, for a proper thickness of SiO_2 and an optimized laser ablation process, selective emitter doping profile could be obtained even at a single step of doping. Although SiO_2 mask layers could be fabricated via dry/wet oxidation or deposition, special pastes with SiO_2 could also be applied via screen printing [33]. After being screen printed, the barrier layer needs to be sintered at 500^{o}C prior to spin on phosphorous dopant source coating [33]. After spin on coating, 900^{o}C diffusion will be applied to activate coated dopant atoms. As demonstrated in Figure 38 the rest of the fabrication process will be identical for oxide barriers both obtained via oxidation or screen printing.

Since the thickness of SiO_2 barrier paste determines the amount of SiO_2 deposited onto the surface, emitter sheet resistance will depend on the paste thickness. Although increasing barrier thickness will result in decreased doping concentration so decreased recombination velocity at the surface, crack formation within the barrier layer could become more probable with higher barrier thickness. Thus, beneficial effects of the selective emitter design could be reduced in the existence of cracks [33]. So, thickness of the barrier layer should be adjusted so as to obtain crack-free layers, so that the surface doping concentration would be reduced to a moderate level.

For barrier layers obtained via dry / wet oxidation, fabrication process requires high temperatures around 850-1000^{o}C, which could be counted as a disadvantage considering thermal budget of the fabrication process. After oxidation, oxide patterning could be either done by using etching paste [34] or by laser ablation. Etching paste would be screen printed and it needs thermal treatment to activate the etchants in the paste solution. However, after etching, paste residuals should be completely removed using phosphoric acid solution [34] prior to high temperature doping process to prevent possible contamination so worsening of cell performance. Despite acidic cleaning, etching paste residues could still be present on the surface. So that; in addition to high temperature oxidation step; screen printing, following heat treatment and post cleaning of etching paste steps need to be added to the standard fabrication process.

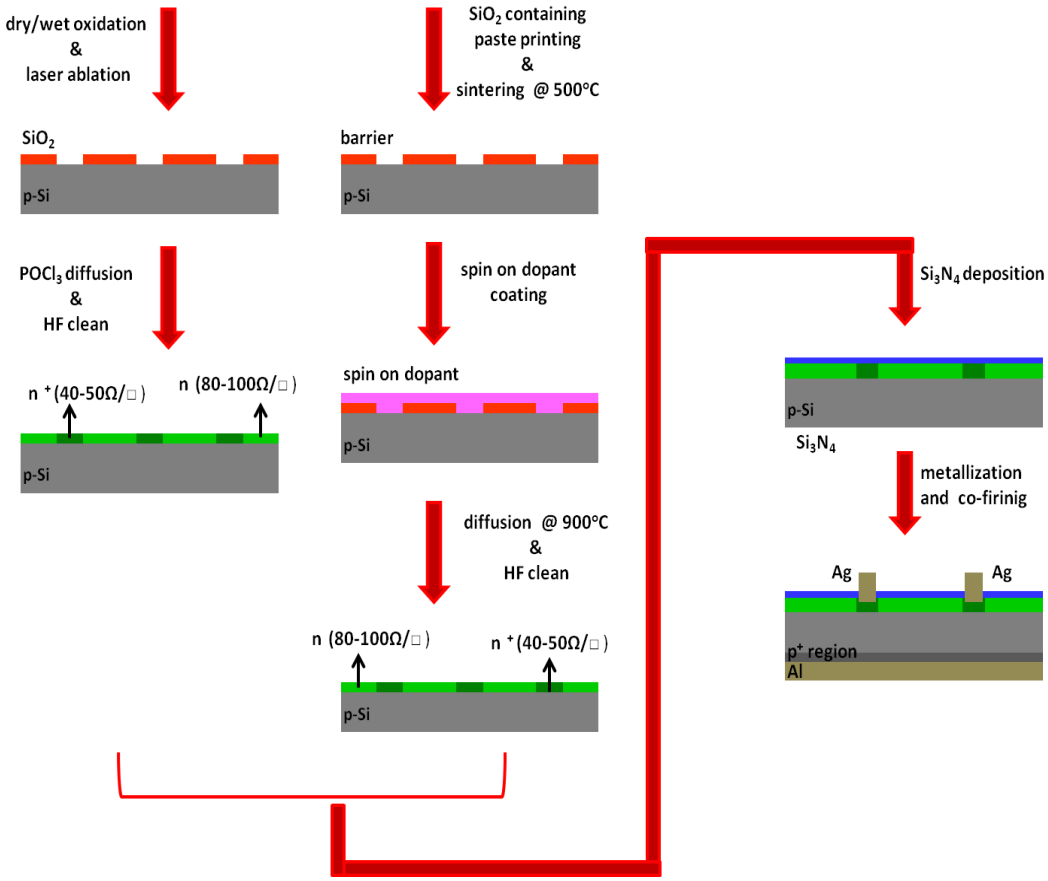


Figure 38: Fabrication process of selective emitter solar cells using silicon dioxide diffusion barrier

For the selective emitter approach studied in this thesis, a thin wet oxide mask was utilized as diffusion barrier. Patterning of the barrier was done via laser ablation which is suitable for the mass production. After a dilute KOH cleaning of laser induced damage, the standard fabrication process including doping, ARC coating and metallization processes were followed. Thus, without any additional screen printing, doping, thermal activation and harsh cleaning steps, selective emitter solar cell could be fabricated.

3.3. Carrier Recombination and Related Passivation Techniques for Crystalline Silicon Solar Cells

3.3.1. Recombination Basics

In order to improve cell performance, reflection, shading and contact losses are required to be minimized. For these purposes, surface texturing has been developed to improve the light trapping, anti reflection coatings such as silicon nitride have been developed to reduce reflection from the surface, and a proper contact design has been developed to reduce shading effect with lowered contact resistance. In addition to these developments, there exists one more critical factor limiting the efficiency output of solar cells which is known as *minority carrier recombination*.

After being generated, minority carriers will have a certain amount of time to move throughout the device before being collected at the corresponding metal contacts. And the time period starting from generation till recombination of minority carriers is known as *minority carrier lifetime* which could take values ranging from microseconds to milliseconds. If generated in the depletion region or within a diffusion length to depletion region, minority carriers will be swept away with the help of electrical field existing in the depletion region and collected at the corresponding contacts. Otherwise, if carriers are not in the vicinity of the depletion region electrical field; or if the material is containing a high concentration of defect states; or if the material is highly doped resulting in a too crowded lattice; then,

generated minority carriers will recombine, or will be captured by a defect state within the structure, or will be scattered by a host atom or a dopant atom staying within the crystal lattice during their motion throughout the device before being collected at the contacts. Each recombined carrier represents a loss in the current output of the cell.

Recombination process could take place both at the surfaces or within the bulk of semiconductor material both of which have adverse effect on cell conversion efficiency. .

Main recombination processes in silicon could be named as *radiative, trap assisted (Shockley- Read-Hall)* and *Auger recombination* [2].

3.3.1.1. Radiative Recombination

Radiative recombination which is also known as band-to-band recombination is simplest one among the other recombination processes [35]. For this type of recombination, an electron staying in an allowed state of conduction band directly falls into a vacant valence band state and recombine with the hole staying there. As a result, both electron and hole are annihilated and the resulting excess energy will be released as photons as demonstrated in Figure 39. Radiative recombination could be thought as the reverse of light induced carrier generation process. And since the top of valence band and bottom of conduction band of a direct band gap semiconductor have the same momentum values allowing direct transition of a conduction band electron to valence band, it could be said that direct band gap materials are more probable to suffer band-to-band recombination. Thus, this type of recombination is less probable to take place in indirect band gap materials, so that radiative recombination effect could be neglected for Si.

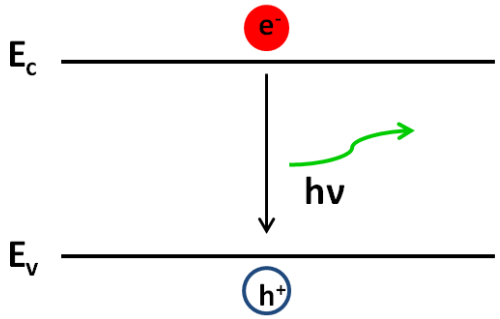


Figure 39: Schematic of radiative recombination process

Moreover, any type of recombination rate (U) is proportional to excess carrier concentration (Δn) and carrier lifetime (τ) [21]. For any semiconductor, difference between total recombination rate and equilibrium generation rate defines the net recombination rate as expressed in the following equation:

$$U = np - n_o p_o = np - n_i^2 \qquad (Eq.28)\ [21]$$

In Eq. 28, n and p defines steady state electron and hole concentration respectively whereas n_o and p_o stands for equilibrium carrier concentration for n and p type materials. Also n_i is conventional symbol of intrinsic carrier concentration. Knowing the fact that, radiative recombination will constitute some portion of the total recombination rate, it could be expressed as a multiple of total recombination rate as expressed in Eq.29 below.

$$U_{rad} = B(np - n_o p_o) = B(np - n_i^2) \qquad (Eq.29)\ [36]$$

In this equation, B is *radiative recombination coefficient* which is equal to 2.1×10^{-15} cm^{-3}/s for silicon [12]. Moreover recombination rate directly depends on excess carrier concentration and lifetime of the generated minority carriers and this relationship could be expressed as in the following equation.

$$U = \frac{\Delta n}{\tau} \qquad (Eq.30)$$ [21]

Combining Eq. 29 & 30, the following expression given as Eq.31 would be obtained to calculate lifetime for radiative recombination;

$$\tau_{rad} = \frac{1}{B(n_0 + p_0) + B\Delta n} \qquad (Eq.31)$$ [36]

For *low injection condition* where excess minority carrier concentration is less than dopant atom concentration, $\Delta n << N_d$, then, both Δn and p_o terms will be negligible compared to n_o term and under fully ionization assumption of dopant atoms, $n_o \approx N_d$. Thus, Eq. 31 takes the following form;

$$\tau_{rad}^{low} = \frac{1}{Bn_0} = \frac{1}{BN_d} \qquad (Eq.32)$$ [36]

For high injection condition where excess minority carrier concentration is equal to or higher than the dopant concentration, $\Delta n >> N_d$, Δn term will dominate Eq. 31 and the new form of the equation will be as in Eq. 33 below.

$$\tau_{rad}^{high} = \frac{1}{B\Delta n} \qquad (Eq.33)$$ [36]

Thus, considering Eq. 32 and Eq.33, it can be deduced that under low carrier injection radiative lifetime is constant whereas under high carrier injection, it starts to decrease as the number of injected carriers increases.

3.3.1.2. Auger Recombination

Unlike radiative recombination, Auger recombination stems from interaction of three charge carriers. Interacting carriers could be two electrons and a hole or two holes and an electron. During Auger recombination, excess energy resulting from recombination of a hole and an electron will either be transferred to a free electron in the conduction band or a free hole in the valence band. Then, the excess energy gained by the third carrier will be transferred to the lattice in form of phonons to bring the excited carrier back to its original energy state as demonstrated in Figure 40.

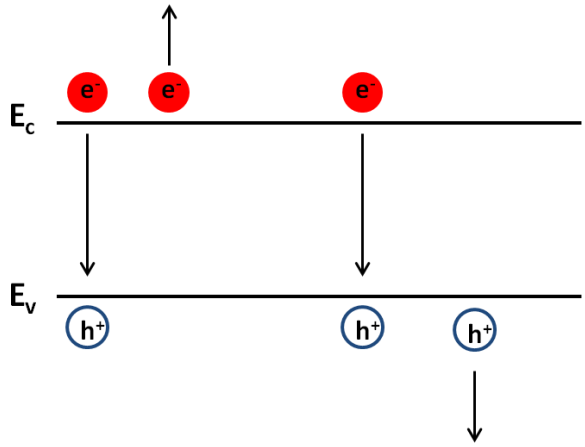


Figure 40: Schematic of Auger recombination process

If the excess energy is given to a conduction band electron, then Auger recombination rate would be expressed as in the following equation;

$$U_{eeh} = C_n n^2 p \qquad (Eq.34)$$ [36]

Else if the excess energy is given to a valance band hole, then Auger recombination rate would be expressed as in the following equation;

$$U_{ehh} = C_p p^2 n \qquad (Eq.35)^{[36]}$$

Summing the effect of eeh and ehh type Auger recombination and subtracting carrier generation, net Auger recombination rate would be expressed by the equation below.

$$U_{Au} = C_n(n^2 p - {n_o}^2 p_o) + C_p(np^2 - n_o {p_o}^2) \qquad (Eq.36)^{[36]}$$

Low injection Auger lifetime for p-type and n-type material could be expressed as,

$${\tau_{Au}}^{low,p} = \frac{1}{C_p N_a^2} \qquad (Eq.37)^{[36]}$$

$${\tau_{Au}}^{low,n} = \frac{1}{C_n N_d^2} \qquad (Eq.38)^{[36]}$$

On the other hand, high injection Auger lifetime for p-type and n-type material could be expressed as in the following equations.

$${\tau_{Au}}^{high,p} = \frac{1}{(C_n + C_p)\Delta p^2} = \frac{1}{C_a\, \Delta p^2} \qquad (Eq.39)^{[36]}$$

$${\tau_{Au}}^{high,n} = \frac{1}{(C_n + C_p)\Delta n^2} = \frac{1}{C_a\, \Delta n^2} \qquad (Eq.40)^{[36]}$$

C_n and C_p are *Auger coefficients* for n and p-type materials respectively where C_a stands for *ambipolar Auger coefficient*. Comparing Eq. 33 with Eq.40, it could be deduced that Auger lifetime more strongly depends on injection level than radiative lifetime does. Thus, under high injection conditions like concentrated illumination or for heavily doped materials, Auger recombination becomes more dominant.

3.3.1.3. Shockley Read Hall (SRH) Recombination

Bulk Recombination

Shockley Read Hall recombination which is also known as "*recombination through defects"* could take place both in the bulk Si or at the surfaces.

Crystallographic imperfections or impurities within the bulk Si results in SRH recombination and the recombination mechanism could be described by four dynamic processes [36]. Electron capture, electron emission, hole capture and hole emission processes make the recombination process up as demonstrated in Figure 41. And for a single recombination level SRH recombination rate could be described as in the following equation;

$$U_{SRH} = \frac{(np - n_i^2)v_{th}N_t}{\sigma_p^{-1}(n + n_1) + \sigma_n^{-1}(p + p_1)} \qquad (Eq.41)\ ^{[36]}$$

where v_{th} defines thermal velocity of generated charge carriers with a value of ~10^7 cm/s at room temperature, N_t stands for density of the recombination centers per unit volume, σ_p and σ_n are capture cross-section for holes and electrons respectively. Also n_1 and p_1 define electron and hole concentrations staying in the recombination level.

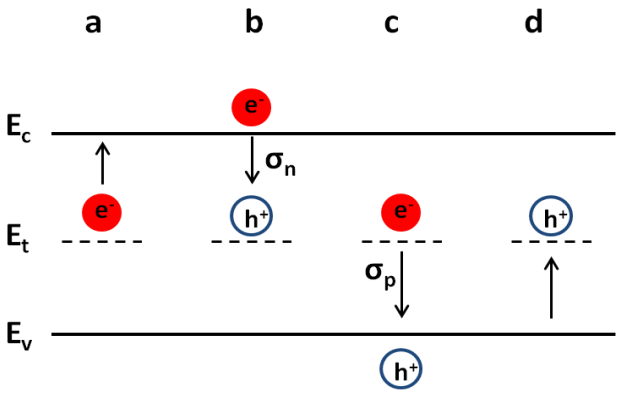


Figure 41: Schematic of Shockley Read Hall mechanism: (a) electron emission, (b) electron capture, (c) hole capture, (d) hole emission

Combining Eq. 30 and Eq. 41, SRH lifetime could be obtained as in the following equation;

$$\tau_{SRH} = \frac{\tau_{no}(p_o + p_1 + \Delta n) + \tau_{po}(n_o + n_1 + \Delta n)}{(p_o + n_o + \Delta n)} \qquad (Eq.42)$$ [36]

In above equation τ_{no} and τ_{po} stand for minority carrier lifetime of electrons and holes respectively and they could be defined as in the following;

$$\tau_{po} \equiv \frac{1}{N_t \sigma_p \nu_{th}} \quad , \quad \tau_{no} \equiv \frac{1}{N_t \sigma_n \nu_{th}} \qquad (Eq.43)$$ [36]

Surface Recombination

In addition to bulk recombination, like other materials Si also suffers from surface recombination. Unsaturated bonds at the bare surfaces of Si or interfaces between Si and dielectric materials or even metals, enhances recombination velocity at the surface which is the rate at which electron-hole pairs recombine.

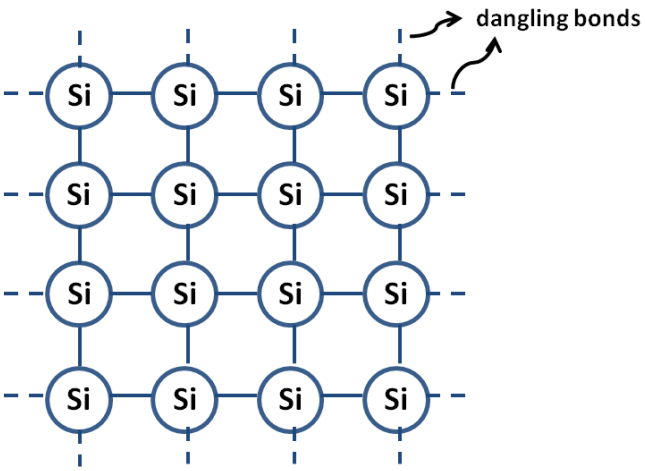


Figure 42: Representation of Si dangling bonds

Unsaturated bonds are also known as dangling bonds and result from the fact that Si atoms at the surface are unable to make four covalent bonds with their nearest neighbors. Instead, they make bonds with two or three neighboring Si atoms and one or two bonds remain open ended as shown in Figure 42. Since each Si atom with unsaturated bond needs to saturate its bonds to become more stable, these dangling bonds at the surface of Si will capture minority transporting carriers so becomes saturated. Same condition is also valid for the interface trap states. Captured minority carriers will not be held for a long time, after a while they will be freed and subsequent carriers will be held by the relaxed dangling bonds/trap states. This capture and freeing loop takes place continuously during the operation of Si solar cells and affects the cell performance adversely by decreasing minority carrier lifetime. Moreover, during holding period of an electron (or hole) if another hole (or electron) is captured by the same defect state, they will recombine at this defect site and the excess energy is given to the lattice as heat. Recombination at the surface or at the Si-insulator interface occurs the same as SRH mechanism in the bulk [36] and the rate of SRH surface recombination could be expressed as in the following equation.

$$U_s = \frac{n_s p_s - n_i^2}{\frac{n_s + n_1}{S_{po}} + \frac{p_s + p_1}{S_{no}}} \qquad (Eq.44)$$ [36]

Here, n_s and p_s are electron and surface concentrations respectively whereas S_{no} and S_{po} are surface recombination velocities of electrons and holes respectively. S_{no} and S_{po} could be defined as in the following equation.

$$S_n \equiv \sigma_n \nu_{th} N_{ts} \quad , \qquad S_p \equiv \sigma_p \nu_{th} N_{ts} \qquad (Eq.45)$$ [36]

where ν_{th} defines thermal velocity of generated charge carriers, N_{ts} stands for density of surface states per unit area, σ_p and σ_n are capture cross-section for holes and electrons respectively.

Among three recombination mechanisms, SRH recombination is the most dominant one for Si under doping concentrations of 10^{15} cm^{-3}. Above 10^{15} cm^{-3} Auger recombination starts to dominate the bulk lifetime of the sample [36].

Effective Lifetime

Effective lifetime is the measurable lifetime value of a sample including the effect of total bulk and surface recombination whereas total bulk lifetime includes the all effect of Radiative, Auger and SRH recombination velocities. Thus, effective lifetime of a wafer could be expressed as in the following equation,

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{1}{\tau_s} = \frac{1}{\tau_{rad}} + \frac{1}{\tau_{Auger}} + \frac{1}{\tau_{SRH}} + \frac{1}{\tau_s} \qquad (Eq.46)$$ [36]

Effective lifetime is generally measured by using Photoconductive Decay Method (PCD) where electron-hole pairs are generated by exposing the wafer to a short light pulse.

Since generated minority carriers change conductance of the sample, by monitoring the change in conductance, information about the decay of minority carriers could be deduced[36].

3.3.2. Passivation Techniques

Minority carrier recombination both within the bulk Si and at the surface poses an upper limit to cell efficiency values. Without a proper surface passivation, highest possible efficiency value of a solar cell couldn't be reached. Since bulk recombination mainly depends on material quality, it couldn't be controlled significantly after wafering process. However surface recombination velocity could be reduced by different *passivation* techniques regardless of wafer quality.

Surface passivation techniques can be mainly divided into three sub topics. The first way of reducing the surface recombination velocity is to apply a high-low junction to reduce the number of minority carrier present at the surface [36].
In this method, a p^+p or n^+n junction is formed at the rear side of the cell to induce an additional electric field pointing the same direction as the electric field at the depletion region of p-n junction as demonstrated in Figure 43.

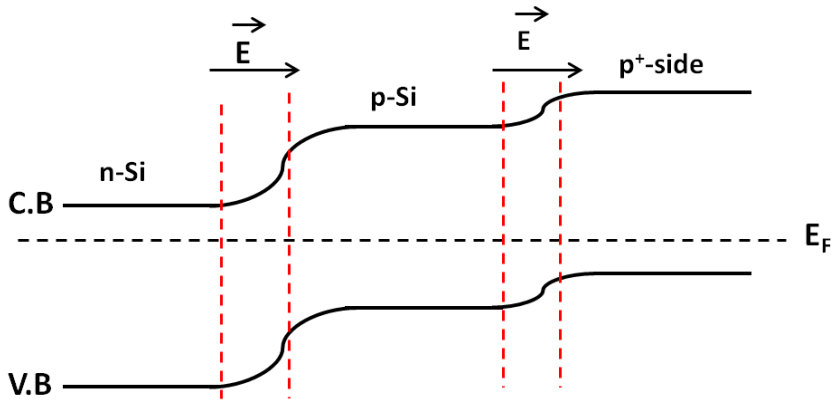


Figure 43: Energy band diagram of a p-n junction with a back surface field at p-Side

Although electric field of high-low junction will not be as strong as that of p-n junction, it will help to push minority carriers towards corresponding contacts so increase their collection probability. This method is widely utilized for Si solar cells and known as *Back Surface Field (BSF).* For standard Si solar cell lines, p-type wafers are utilized and for that reason, BSF is provided via Al rear contact. During co-firing of Ag front and Al rear contacts, temperature around 830-850^{o}C is reached. Al-Si binary system has a eutectic temperature of 577^{o}C with a composition of 11.7% Si in weight [37] whereas Ag-Si binary system has a eutectic temperature of 835^{o}C with a composition of 3.1% Si in weight [38]. Also, melting point of Al is 660^{o}C and of Ag is 962^{o}C. Thus, during co-firing of front and rear contacts, Al at the rear side will melt and form an Al-Si alloy which acts as a BSF whereas Ag will not melt within this temperature range thus no Ag-Si alloy will be formed at the front side.

Another way to reduce recombination velocity at the surfaces of the wafer is *field effect passivation* which is provided by a charged dielectric layer coated on the surface.

For this type of passivation, fixed charges stored in the passivation layer repel minority carriers towards corresponding contacts [36]. For the front surface applications, passivation layers should have refractive indices with minimum reflection at ~500 nm to match with the peak of solar spectrum for proper anti-reflection. Silicon nitride (SiN_x) layers are known to have positive fixed charges [39] so are able to properly passivate n-type surfaces whereas Al_2O_3 layer have negative fixed charges [40] thus good at passivation of p-type surfaces. Additionally, SiO_2 could be used both for n-type and p-type surfaces.

These three mentioned dielectric layers are widely used by the industry. In addition to their application as single layers, these dielectrics could be utilized in form of stack layers where a thin SiO_2 or Al_2O_3 layer is capped with SiN_x.

Surface passivation could also be provided via *chemical passivation*. For this type of passivation, dangling bonds at the surface are saturated by formation of new bonds between underlying c-Si and above deposited or coated layer of passivation material. Although amorphous Si (a-Si) itself is a highly defective material, it is

capable of providing excellent passivation of c-Si surface. It could be deposited at lower temperatures and this structure is known as hetero-junction [41].

In addition to application of a-Si, surface passivation could also be reached by solution immersion. In this case, sample is needed to be dipped into very dilute Iodine Methanol (IM) or Iodine Ethanol (IE) solutions where free I^- ions are ready to stick to Si surface. Thus, termination of dangling bonds will be saturated by I^- ions [42]. These techniques can also be used for bulk lifetime estimations. During such measurements, surface recombination can be almost reduced to zero, so measured effective lifetime will approximately be equal to bulk lifetime. However, solution based chemical passivation is unable to enhance device performance, because excellent passivation effect cannot be maintained during the high temperature fabrication steps solar cell. As soon as the sample is taken out of the solution, provided passivation effect will be lost. Moreover, iodine residues must be completely removed from the surface to avoid detrimental contamination effects. For these reasons solution based passivation is not used in the industrial production lines.

In addition to their surface passivation property, SiN_x and a-Si layers could also provide bulk passivation via *hydrogenation* [39].

In other words, during deposition of SiN_x layer, hydrogen (H) atoms are bonded to amorphous SiN_x molecules, also known as *hydrogenated silicon nitride (a-SiN_x:H)* and these H molecules diffuse into the bulk Si during contact firing process. With the help of heat energy, weak N: H bonds will be broken and new Si:H or $Si:H_2$ bonds will be formed where Si:H bonds are proven to provide more effective passivation than $Si:H_2$ does. Thus, in addition to field effect passivation at the surface, defect states within the bulk Si could also be saturated by SiN_x:H layer. Amorphous silicon is another material capable of providing simultaneous bulk and surface passivation of underlying crystal silicon. During the deposition of a-Si layer, if hydrogen gas is also fed to the system then, the deposited layer will be *hydrogenated amorphous Si (a-Si:H)* whose H atoms will be freed during post thermal treatment and freed H atoms will stick to defect states within the bulk of the wafer Thus, a-SiN_x:H and a-Si:H are capable of providing passivation by both field effect with the help of stored charge and chemical passivation respectively with the help of hydrogenation.

Passivation using SiN_x, SiO_2, a-Si:H and SiN_x:SiO_2 has been studied during this thesis work.

CHAPTER 4

EXPERIMENTAL PROCEDURES

4.1. SINGLE DOPING STEP SELECTIVE EMITTER SOLAR CELL FABRICATION PROCESS FLOW

Fabrication of selective emitter structure with single doping step using an oxide barrier layer has been studied in this thesis. The device structure and process flow is described in Section 3.2 in the previous chapter. In this chapter, details of each process step are described.

4.1.1. Texturing

Selective emitter solar cell fabrication process starts with alkali texturing of Si wafers as in standard cell fabrication. Texturing reaction is carried out in a custom designed, continuously stirred polypropylene tank, which is capable of processing 50 wafers per run. Stirring is done by means of nitrogen (N_2) bubbling, which provides uniform temperature distribution and solution homogeneity during reaction. Texturing solution has a weight distribution of 91.4% H_2O: 4.5% IPA: 4.1% KOH and the reaction is conducted at 75^{o}C for 40-45 minutes. This recipe is optimized at GUNAM Laboratories for the above described system.

After texturing, an HCl dip is necessary to neutralize KOH residues which is followed by HF dip to remove oxide layer formed on the surface and DI-H_2O rinse between each step. Finally, texturing step is completed with drying of wafer under nitrogen gas.

4.1.2. Oxide Masking

Oxide masking is an additional step which is not used in standard cell fabrication. For selective emitter cell fabrication with single step doping, a diffusion barrier is necessary which is chosen as thin SiO_2 for the studies within the scope of this thesis. Since mask layer is not supposed to have high quality, oxide masks were grown via pyrogenic oxidation instead of dry oxidation. Since the growth rate in pyrogenic oxidation is much faster compared to that of dry oxidation [14], using pyrogenic oxidation would decrease the total thermal budget and process time of the whole fabrication. All oxidation processes are carried out in *SEMCO Engineering Incorporation MINILAB Series* oxidation furnace. As demonstrated in Figure 44, oxidation furnace consists of a horizontal quartz tube with its gas inlets and corresponding controllers.

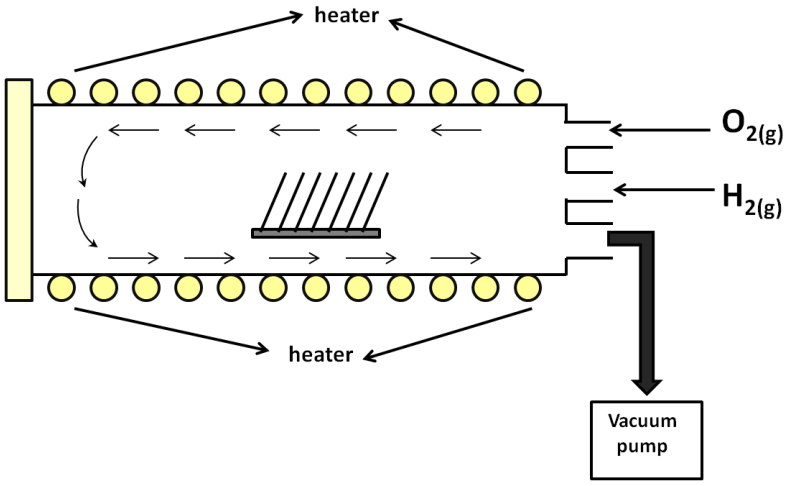


Figure 44: Schematic of oxidation furnace

Pyrogenic oxidation of Si is similar to wet oxidation and obeys the same reaction equation as wet oxidation does, which is expressed in Eq.47.

$$Si_{(s)} + 2H_2O_{(g)} \rightarrow SiO_{2(s)} + 2H_{2(g)} \qquad (Eq.47)$$ [14]

The difference between pyrogenic and wet oxidation is their reaction inlets. For pyrogenic oxidation, $H_{2(g)}$ and $O_{2(g)}$ will be fed to the system; whereas, for wet oxidation $H_2O_{(g)}$ will be the reaction input. As $H_{2(g)}$ and $O_{2(g)}$ gases come in contact within the furnace at high temperature, they form H_2O vapor that oxidizes the Si surface [14].

To be able to use SiO_2 as a diffusion barrier its thickness has to be optimized properly. If the oxide layer is not thick enough, then no barrier effect can be obtained. If the barrier is not thin enough dopant atoms cannot penetrate through. Thus, no doping can be obtained. For this reason, an extensive optimization study has been carried out to determine the optimum oxide thicknesses and different doping recipes to achieve a successful a selective emitter structure at the surface.

4.1.3. Laser Patterning

After formation of an oxide mask on the surface, fabrication process continued with laser scribing step. It was carried out by an IR marking laser with a maximum power of 30W and wavelength of 1064 nm. For patterning, grooves are opened on mask layer in such a way that front contact fingers will be printed over these grooves with the smallest misalignment as possible. In order to give a tolerance for finger alignment, under each finger; 6 grooves are opened with a separation of 25μm whereas spot size of the laser beam was 50μm. Thus, successively opened grooves overlap and final width of the groove becomes equal to 175μm. The final width of the groove exceeds that of finger which is equal to 125μm. Reducing groove thickness results in misalignment which adversely affects the device operation. Since misalignment is a serious problem resulting in an increased series resistance and *dead* regions which can easily be identified by electroluminescence, we have used a high tolerance value in this study. However, in principle, the difference between the grooves and the metal finger thickness can be minimized by special equipment so that better performance can be obtained.

In order to obtain optimum laser pattern, different laser parameters like power, speed and pass number have been studied in detail for different oxide thicknesses, different doping recipes and also for different post cleaning recipes. Changing laser parameters not only changes doping concentration at the surface but also affects laser induced damage given to the underlying Si surface which should be minimized as much as possible.

4.1.4. Post Laser Cleaning

After laser ablation, Si surface is damaged even at low laser power values and the damage has to be treated. For this purpose, laser ablated wafers are dipped into 10% wt KOH solution where Si surface is isotropically etched to remove damaged portion of Si away from the surface. Etching duration is optimized using optical microscope images and profilometer measurement results. After KOH dipping, wafers are rinsed in DI water which is followed by 10% HCl solution to remove KOH residues so that no K^+ contamination will be present prior to high temperature doping process. During successive KOH, DI water and HCl dips, a possible oxide layer is formed on oxide ablated regions of Si which could act as a potential barrier during following doping step. To get rid of this oxide layer, a short dilute HF step is introduced at the end of cleaning step. Solution concentration of 1% HF does not remove the oxide mask layer. The etch time periods of this process were studied and optimized for different oxide thicknesses. After HF dip, another DI water rinse step was applied and then samples are dried in hot N_2 environment prior to doping.

4.1.5. Doping

Following additional oxide masking, laser patterning and post cleaning steps, rest of the fabrication process will be the same as in standard cell fabrication, so that, post cleaning step will be followed by doping. In addition to standard doping recipe resulting in 50 Ω/□ sheet resistance, a high doping recipe was also applied for selective emitter solar cells which resulted in a sheet resistance of around 30 Ω/□.

Doping is carried out in *SEMCO Engineering Incorporation MINILAB Series* doping furnace where $POCl_{3(liquid)}$ is used as the dopant source. As shown in Figure 45, $POCl_3$ is carried through the furnace by N_2.

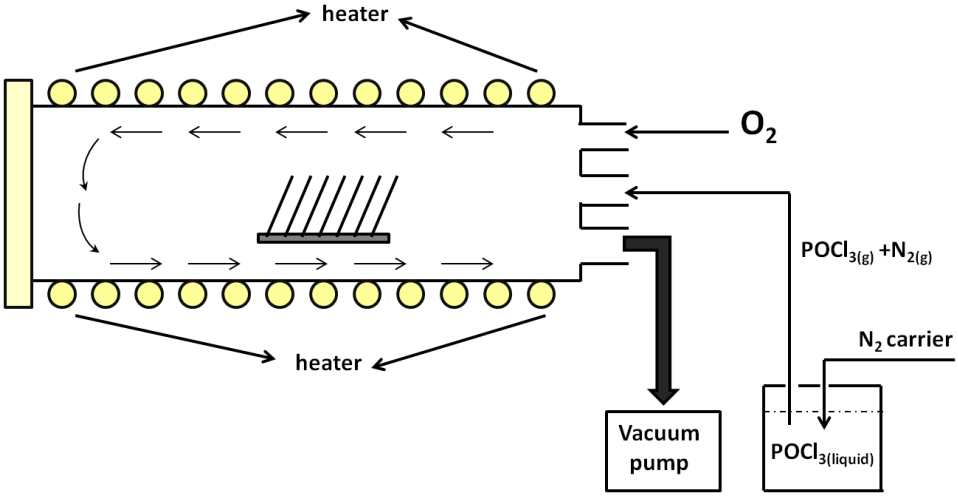


Figure 45: Schematic of doping furnace

In the predeposition step of doping, $O_{2(g)}$ and $POCl_3$ is simultaneously fed to the furnace to form $P_2O_{5(g)}$ as described by Eq.13. Then, in drive-in step, $POCl_3$ flow is suppressed and reactions expressed in Eq.14 and Eq.15 simultaneously take place to form PSG on the surface.

To ensure phosphorous diffusion through SiO_2 layer, full wafers with different oxide thicknesses are doped using both standard and high doping recipes, then corresponding sheet resistance values are measured after removing the oxide layer from the surface.

After doping, PSG and mask oxide layers are completely removed from the surface using 10% HF solution and samples are dried under hot nitrogen prior to the nitride deposition. However, a thin layer of oxide is grown on a group of samples by dry oxidation at low temperature for taking the advantage of SiO_2/SiN_x stack layer passivation over SiN_x single layer passivation [43].

4.1.6. Anti Reflection Coating

After doping and corresponding cleaning steps, anti reflection coating deposition is carried out where a-SiN_x is deposited by using PECVD chamber of *SEMCO Engineering Incorporation MINILAB Series* (Figure 46), which is capable of processing 10 wafers per run. For SiN_x deposition, SiH_4 and NH_3 gases are fed to the chamber at a temperature of 380^oC and pressure of 1Torr. Dissociation of inlet gases to their reactive radicals is provided by means of an RF generator operating at 375 W with a frequency of 50 kHz.

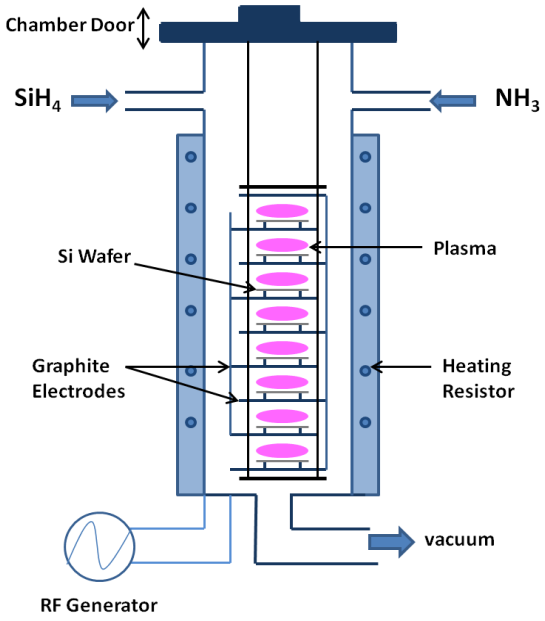


Figure 46: Schematic of PECVD chamber

Within the generated plasma, the chemical reaction expressed in Eq.48 takes place and the product molecules (Si_3N_4) move down and stick onto Si substrates. As soon as they stick onto substrate surface, Si_3N_4 molecules condense and cover the whole surface in the form of a thin film.

$$3SiH_{4(g)} + 4NH_{3(g)} \rightarrow Si_3N_{4(s)} + 12H_{2(g)} \qquad (Eq.48)$$ [3]

Depending on the inlet gas ratios, obtained film composition could be changed. Si_3N_4 which is known as stoichiometric silicon nitride needs 3 parts of SiH_4 gas for every 4 parts of NH_3 entering the system. Thus, the parameter *X* which is defined as [N]/[Si] ratio is equal to 1.33 for stoichiometric nitride layers [44]. Higher SiH_4 flows results in greater *X* values leading to formation of Si rich nitride layers, whereas, higher NH_3 flows result in nitrogen rich films with *X* values less than 1.33. Changing composition of nitride layer will also change optical properties, Depending on the film compositions, nitride layers can have refractive indices ranging from 1.8 to 2.3. It is known that stoichiometric silicon nitride has a refractive index of 2.01 at 632 nm and increasing Si content would increase this value up to 2.3[44].

Changing gas ratio would not only affect the optical properties; but also, temperature stability and passivation properties of the layer. Density of N is $1.251x10^{-3}$ g/cm^3; whereas, it is equal to 2.33 g/cm^3 for Si [45]. Hence, increasing nitrogen content decreases the density of the silicon nitride film and temperature stability of the film degrades. Silicon rich nitride layers are thought to release atomic hydrogen, whose diffusion through Si surface will be assisted via defects. Nitrogen rich films, on the other hand, are believed to induce molecular hydrogen release into the atmosphere [44]. Since atomic Hydrogen is believed to be responsible for the bulk and surface passivation, Si-rich SiN_x layers would provide superior passivation compared to N-rich layers. Also, N-H bonds, *also known as Hydrogen bonds*, are stronger compared to Si-H bonds; so N-H bonds are less likely to be broken and thus less Hydrogen will be available for passivation.

For passivation studies, different gas flow rates have been applied on both passivation samples and also selective emitter solar cells to determine nitride recipe resulting in a better cell performance. During deposition, total gas flow, chamber pressure and plasma temperature have been kept constant. Also, thickness of the layers has been kept constant within the range of 70-80 nm to provide the best anti reflection performance.

Passivation quality of different layers whose thicknesses and refractive indices have been obtained by ellipsometric measurements, have been examined via lifetime measurements whereas their reflection spectrum were obtained by reflection measurements.

4.1.7. Metallization and Co-Firing

Metallization of samples has been done by *ASYS EKRA-XL1* screen printing system. In the selective emitter process we develop here, front Ag fingers have to be aligned in a way that fingers will fall into already opened grooves where the dopant concentration is higher. Finger alignment is the most challenging part of the whole selective emitter cell fabrication process, which should be conducted carefully and properly. Even a small shift between the fingers and underlying grooves may result in dramatic performance losses. For the rear side of the cells, industrialized full Al contact design is used.

Screen printing and drying of front and rear contacts is followed by co-firing during which samples are exposed to high temperature on a conveyor belt with a speed of 90 mm/s under atmospheric conditions. Temperature profile of the firing furnace resembles a sharp Gaussian distribution function with a peak temperature around 835^{o}C. Such a sudden increase in temperature provides melting of back Al; thus, forming p^{+} back surface field at the rear side while front Ag contact diffuses through the nitride layer and touch emitter region without melting.

4.1.8. Edge Isolation

Cell fabrication sequence ends with edge isolation step. Edge isolation is carried out by an IR marking laser, which is also used for oxide mask patterning. For isolation, edges of the whole sample are scanned by laser beam without shorting the p-n junction. That is if the laser beam penetrates through the p-n junction, a new path combining p and n regions would be formed and the generated carries in the vicinity of the junction region would follow this new path instead of moving towards the corresponding contacts. During edge isolation, Si is ablated which results in 10-15

μm deep grooves opened on the surface. These grooves electrically disconnect front emitter from the rear collector.

4.2. PASSIVATION STUDIES

For passivation studies SiO_2, SiN_x and SiN_x/SiO_2 stack layers have been studied. SiN_x and SiO_2 layers are already utilized in standard solar cell production lines; thus, suitable for mass production.

For SiN_x optimization, flow rates of process gases were varied starting from N-rich towards Si-rich layers whose refractive indices and thicknesses were monitored by ellipsometric measurements. Lifetime measurements were conducted by *SINTON WTC-120_Photoconductance Lifetime Tester* which is a contactless measurement method that requires symmetrical samples. For this reason, SiN_x depositions were applied on both sides of all lifetime samples.

SiO_2 was also applied as a single layer and with SiN_x as capping layer on top. Different thicknesses of oxide layers were grown at different temperatures by both dry and pyrogenic oxidation methods.

4.3. CHARACTERIZATION

4.3.1. Solar Cell Characterization

4.3.1.1. Reflection Measurements

Solar cell characterization starts with reflection measurement just after the surface texturing step to observe the effect of alkali etching on surface reflection. With the help of light trapping provided by the pyramids, reflection of bare silicon reduces. Also after silicon nitride deposition, reflection would be measured one more time in order to observe anti reflection effect of the nitride layer.

Reflection measurements are carried out using the reflection set-up schematically shown in Figure 47.

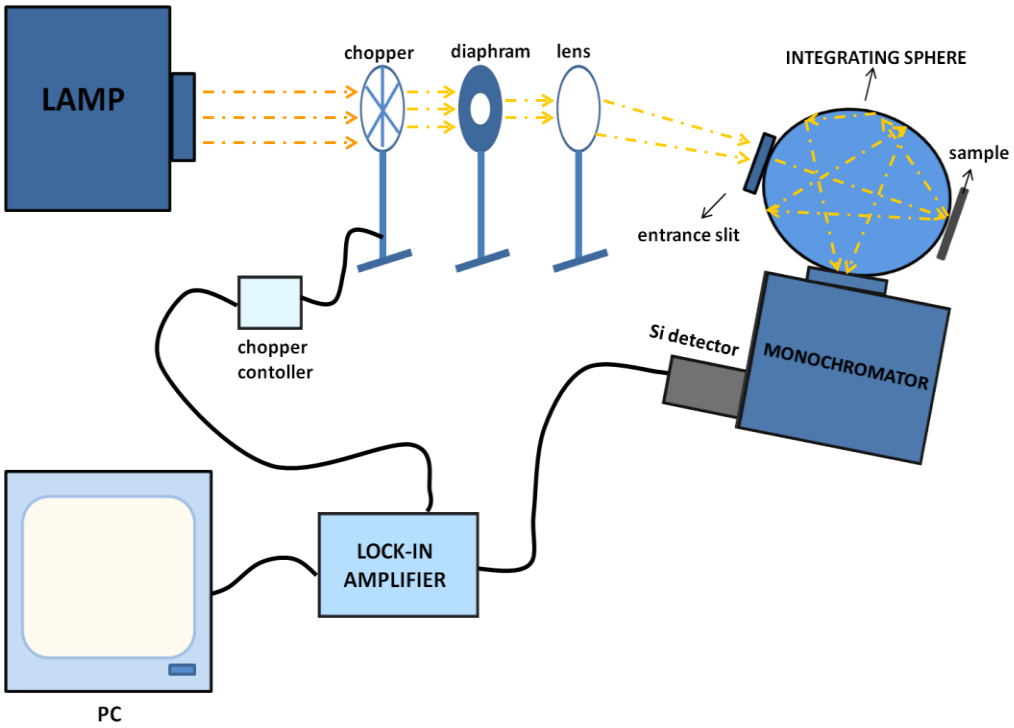


Figure 47: Reflection set-up used in GUNAM Laboratories

In this set up, a halogen lamp is used as the light source whose output signal is modulated by a chopper. Chopper rotates at a set frequency which is not an integer multiple of 50Hz to avoid from possible affects of network electricity. Then, with the help of chopper controller connected to lock-in amplifier, only signal with the set chopper frequency value could be detected, other frequency values were filtered. After passing through the chopper, spot size of the modulated light will be decreased at the diaphragm and smaller spot is then focused onto the entrance port of integrating sphere with the help of a condensing lens. Since pyramids are randomly oriented over the surface, incident light will be arbitrarily reflected. After many reflections within the integrating sphere, reflected light will be collected at the exit port of the sphere, which is connected to entrance slit of the monochromator. At the

exit of the monochromator, a Si detector is placed, which is connected to a computer via a lock-in amplifier. Using above described set-up, reflection measurements of the samples were carried out in 350-1100 nm range. In order to calculate reflection from the sample, a calibration measurement has to be carried out using a standard sample like a $BaSO_4$ disc with 100% reflectivity. Thus, reflection of the sample would be equal to ratio of sample's intensity spectrum to that of calibration disc.

4.3.1.2. Sheet Resistance Measurements

After doping, sheet resistance of the wafers are measured by a *JANDEL-RM3-AR* four point probe. Sheet resistance measurement became crucial for the optimization of high-low doping profile of selective emitter cells.

During the optimization studies, oxide masked wafers with varying oxide thicknesses were laser scanned as squares of $1x1cm^2$ for different laser parameters. And for each laser parameter and oxide thickness, sheet resistance was measured. Then, once optimum oxide thickness and laser parameters were obtained, uniformity of the whole wafers was checked by sheet resistance measurements.

4.3.1.3. *I-V* Measurements

I-V measurement is the most conventional way of analyzing solar cell performance. I-V measurements of fabricated solar cells were conducted by *QUICK SUN-120CA-XL Solar Simulator*, whose schematic is demonstrated in Figure 48. Solar cells are illuminated under 1 SUN AM 1.5 G and current output is measured as a function of applied bias voltage.

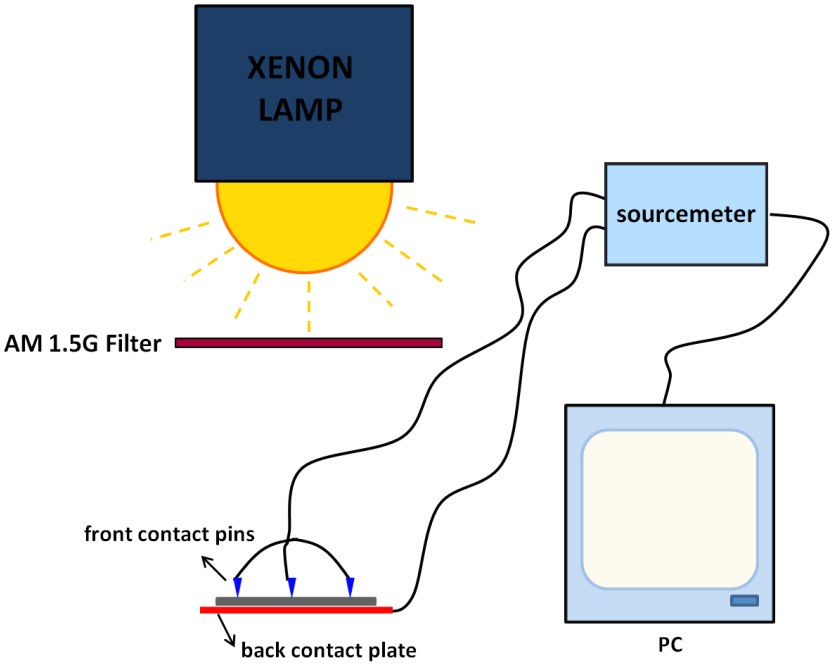


Figure 48: Schematic of solar simulator

Simulator's software provides cell efficiency, fill factor, series resistance, shunt resistance, open circuit voltage, short circuit current and maximum power point as output data.

4.3.1.4. Electroluminescence Measurements

Electroluminescence (EL) is a method, where cells are forced to radiate under an applied bias. For this purpose a *MBJ* closed box EL system is utilized. Measurement results provide information about the dead regions of a cell; because, no radiation could be generated from these regions. For the analysis of a fabricated selective emitter solar cell, front Ag contact misalignment problems, back Al adhesion problems or any possible cracks along the cell could be realized.

4.3.1.5. External Quantum Efficiency Measurements

External quantum efficiency (EQE) is another useful technique widely applied for solar cell characterization.

In this method, number of electrons generated per incident photon is determined as a function of wavelength. This method gives information about, the junction quality effects of contacts, recombination dynamics across the device.

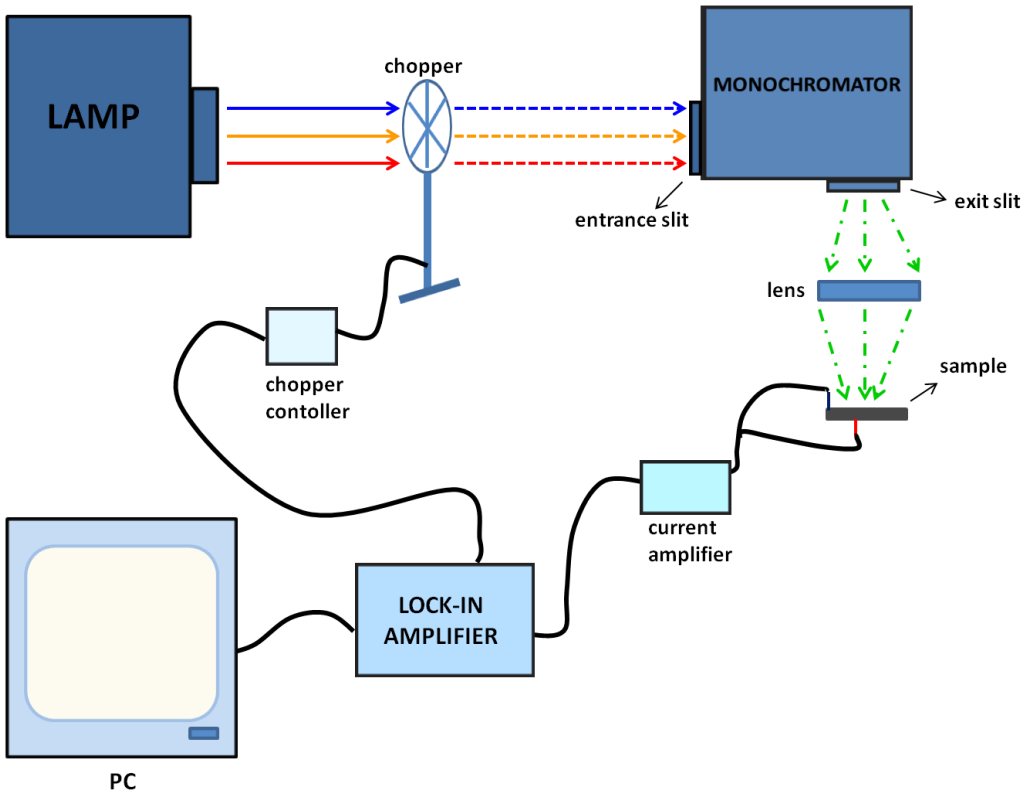


Figure 49: Schematic of external quantum efficiency set-up placed at GUNAM Laboratories

EQE measurements are carried out at the system shown in Figure 49. Unlike reflection set-up, modulated beam of light interacts with the sample after passing through the monochromator.

At the exit of the monochromator, light beam is focused on the sample and the corresponding response is collected by two probes, one of which is in contact with the front busbar while the other is touching rear Al of the cell. The collected signal is amplified prior to lock-in amplifier and the resultant response is monitored.

4.3.1.6. Suns-Voc Measurements

After whole fabrication sequence, open circuit voltages of the samples with contacts on both sides could be measured as a function of the incident light intensity with the help of Suns-Voc system. The measurement result gives information both about the base material and passivation quality.

Moreover, obtained data can be analyzed to predict the I-V behavior of the cell under zero series resistance assumption. By this assumption, some important cell parameters like *pseudo* efficiency, *pseudo* fill factor, etc could be estimated, since the effect of shunt and series resistance could have been separated from each other. And the difference between maximum power estimated by Suns-Voc and measured by solar simulator could be related to series resistance loses [46].

4.3.1.7. Contact Resistance Measurements

Contact resistance of the fabricated cells was calculated by taking I-V data from equally separated front fingers. For this measurement, full cell was separated into smaller, busbar-off pieces as demonstrated in Figure 50. Then, by keeping position of the first probe constant, second probe was placed on successive fingers respectively. Moving second finger changed the separation between two probes. Since front contacts are expected to be Ohmic, resistance to be calculated from taken I-V data would be linearly dependent on the separation between two probes. After plotting resistance v.s. separation graph, extrapolation of the plotted line to the *y*-axis would give resistance at zero contact separation which is value of *contact resistance*.

The above described method is known as *Transfer Line Method (TLM)* and the total measured resistance (R_T) will be summation of contact resistance coming

from two contacts (R_c) and resistance of the underlying semiconductor (R_{semi}) as expressed as in Eq. 49 [47].

$$R_T = 2R_c + R_{semi} \qquad (Eq. 49)\ ^{[47]}$$

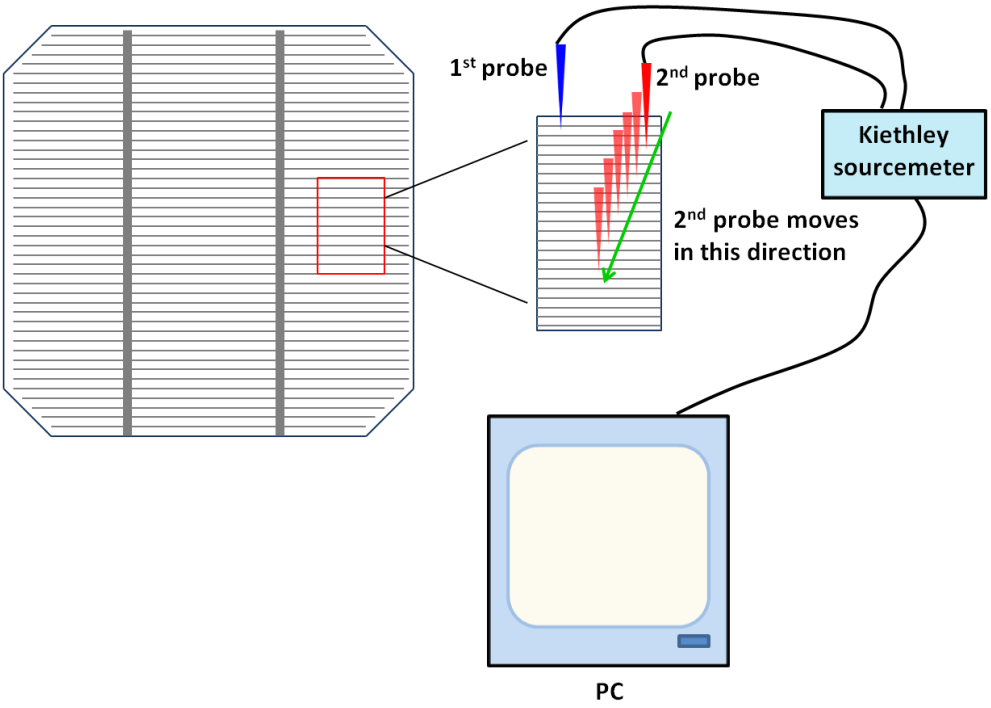


Figure 50: Schematic of contact resistance measurement system

As mentioned above, *y*-intercept of R_T vs. length plot gives $2R_c$ whereas its slope is equal to sheet resistance of the underlying Si wafer.

4.3.2. Characterization of Lifetime Samples

4.3.2.1. Lifetime Measurements

Lifetime measurement of the samples was carried out by *Sinton WTC-120 Lifetime Tester* where the method is based upon *Photoconductance Decay (PCD).* During

measurement, sample is exposed to light pulse with a decay constant ranging from 10-20 μs to 2 ms depending on the measurement mode. As the light decays, steady state injection assumption holds true; thus, each second of measurement could be described with a slightly different injection level [46]. Whereas the decaying light intensity is being measured with a calibrated light sensor positioned at the same level as the sample, the sheet conductivity of the sample is being measured by an inductively coupled RF coil as demonstrated in Figure 51 and this measured conductivity is then to be used for lifetime calculation.

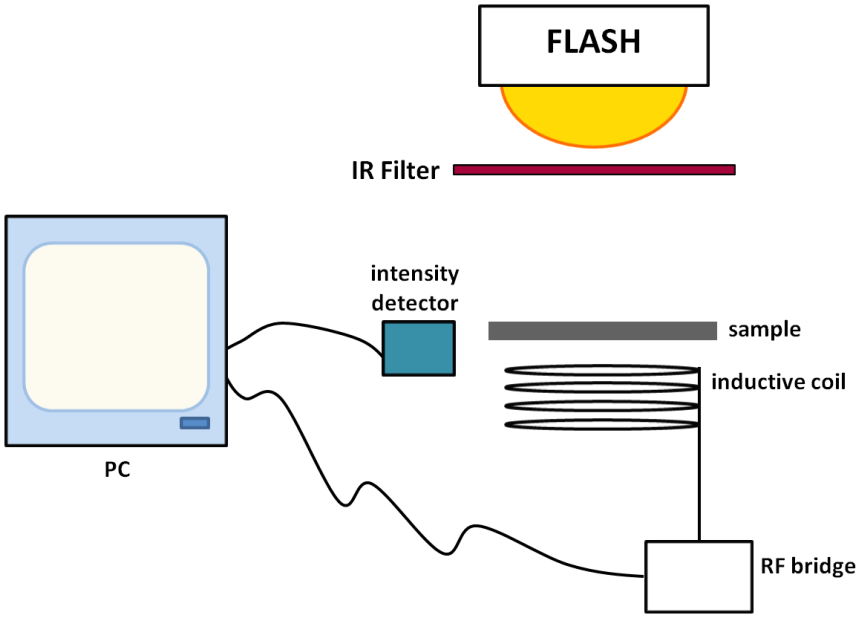


Figure 51: Schematic of Lifetime measurement system

Measured conductance of the sample is related to excess carrier density by the Eq. 50 expressed below.

$$\Delta n = \frac{\Delta\sigma(t)}{q(\mu_n + \mu_p)W} \qquad (Eq.50)$$ [46]

In this equation, $\Delta\sigma(t)$: measured conductance varying with time

q: elementary charge

W: sample thickness

μ_n,μ_p: electron and hole mobilities, respectively

Inserting sample thickness as an input to the software, excess carrier density could be calculated as a function of time. Also, under stead state assumption, generation rate measured with reference cell will be equal to the recombination rate. Then, by applying Eq. 30, effective lifetime is calculated.

CHAPTER 5

RESULTS and DISCUSSION

5.1. SELECTIVE EMITTER SOLAR CELL PROCESS OPTIMIZATIONS

Detailed description of the selective emitter process developed in this work is given in the previous chapters. In this chapter**,** we present the results and discussion of the studies we carried out to develop this technology.

5.1.1. First Run

As the first run of selective emitter cell fabrication, laser scribing was studied for different laser powers, different scribing speeds and different scribe numbers. Laser current was set to 30-32 A and 36-38 A whereas scribing speed was adjusted as 300 mm/s and 600 mm/s. For each laser parameter, either 1, 2, or 3 successive grooves were opened to provide some tolerance for the alignment of front side contact pattern. For all scribe parameters, laser wavelength was 532 nm; whereas, repetition rate was 50 kHz. Doping mask oxide layer was grown via pyrogenic oxidation at 950^{o}C for 3, 4, and 6 min to be able to properly control phosphorous concentration not only inside the opened grooves but also under oxide layer. At this point, KOH dipping duration was also required to be optimized in order to reduce laser induced damage at the surface. For this purpose, 10% KOH dipping was applied for 10, 20 and 35 min which was followed by 10% HCl dipping for 20 min to neutralize residual K^{+} ions. Moreover, in addition to "*standard doping"* recipe resulting in a sheet resistance of 50 Ω/□ with the estimated peak P concentration of $2.87x10^{20}cm^{-3}$.

Another recipe named as *"high doping"* was also used for selective emitter doping generating a sheet resistance of 35Ω/□ whose estimated peak concentration was $4.28x10^{20}cm^{-3}$. Deposition and drive-in duration of the standard doping recipe was 35 min and 30 min respectively; whereas, deposition duration was increased to 45 min and drive-in duration was kept constant at 30 min for high doping recipe. Process temperature was kept constant at 838°C for both standard and high doping recipes. A proper scribing parameter was aimed to be chosen as the starting point. Opened grooves were required to be wide enough to provide some tolerance for the subsequent metallization step and also shallow enough to ablate only mask layer giving as less damage as possible to the underlying silicon surface. Groove depth and width was measured just after scribing and after 10, 20 and 35 min KOH dipping to observe the effect of dipping duration.

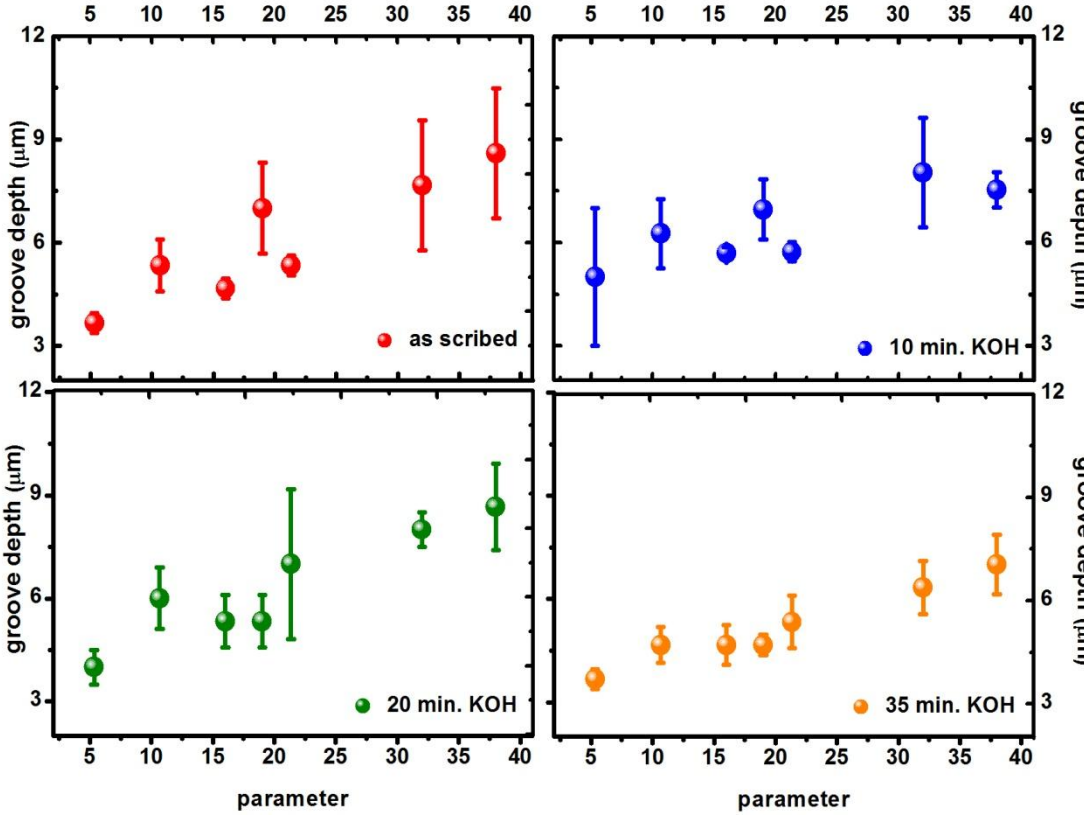


Figure 52: Effect of KOH dipping duration on groove depth

In order to express the effect of laser scribing in a compact way, we define a new parameter called "*Laser Impact Factor*" as $\frac{(laser\ current)x(scribe\ number)}{scribing\ speed}$. This factor express how strongly the material is exposed to the laser radiation. In Figure 52, the dependence of groove depth formed by laser scribing on this impact factor is given. We see that the depth of the opened groove increases with the impact factor as might be expected. Groove depth was proportional to laser current and scribe number whereas inversely proportional to scribing speed. However, as the KOH dipping duration increased, laser induced damage on the surface was reduced more, so opened grooves edges was smoothened more. Decreased roughness is reflected as reduced standard deviation in groove depth vs. laser impact factor plots. In order to decrease the groove depth and give less damage to silicon surface, laser current was chosen to be smallest which was 30-32A; whereas, scribing speed was set to its highest value which was 600 mm/s. These laser parameters correspond to "5" at laser impact factor axes in Figure 52. Prior to laser scribing, sheet resistance of the scribe-free regions had to be set at a value in 60-90 Ω/□ range. For each oxide thickness, both standard and high doping recipes were applied to determine the optimum doping recipe. After removing PSG by HF dipping, sheet resistance values were measured by four-point probe.

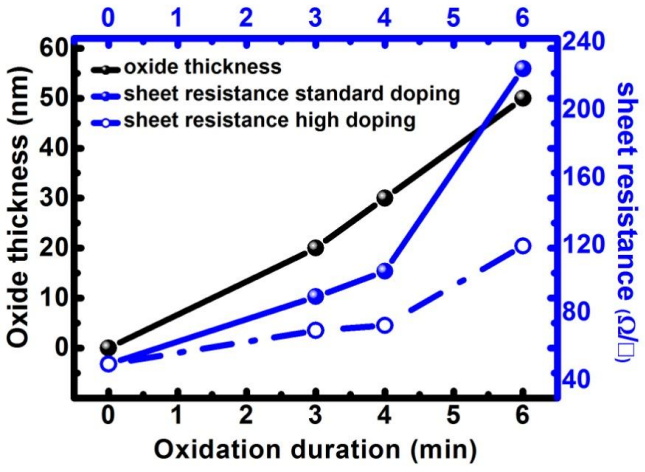


Figure 53: Oxidation duration, oxide thickness and sheet resistance relationship

As demonstrated in Figure 53, applied oxidation durations resulted in oxide thicknesses of 20, 30 and 50 nm respectively. Considering measured sheet resistance values; for 50 nm mask oxide, standard doping recipe resulted in sheet resistance greater than 120 Ω/□, which is not appropriate to be used as emitter layer of a solar cell. After observing the effect of KOH dipping duration on groove morphology and realizing oxide thickness-sheet resistance relationship, behavior of sheet resistance subsequent to KOH exposure had to be examined. In order to see upper and lower limits of sheet resistance, only 10min. and 35 min. KOH dipping was applied. As seen in Figure 54, KOH dipping duration didn't severely affect sheet resistance values of standard doping samples whereas longer KOH dipping resulted in relatively lower sheet resistance values for high doping samples with 30 nm and 50 nm mask oxide layers. This means that, 35min KOH dipping somehow affects diffusion barrier property of the mask oxide and results in higher phosphorous concentration on the surface. If the oxide mask layer is thinned too much, both scribed and un-scribed regimes of the surface would be almost equally doped, which creates a homogenous emitter instead of a selective one.

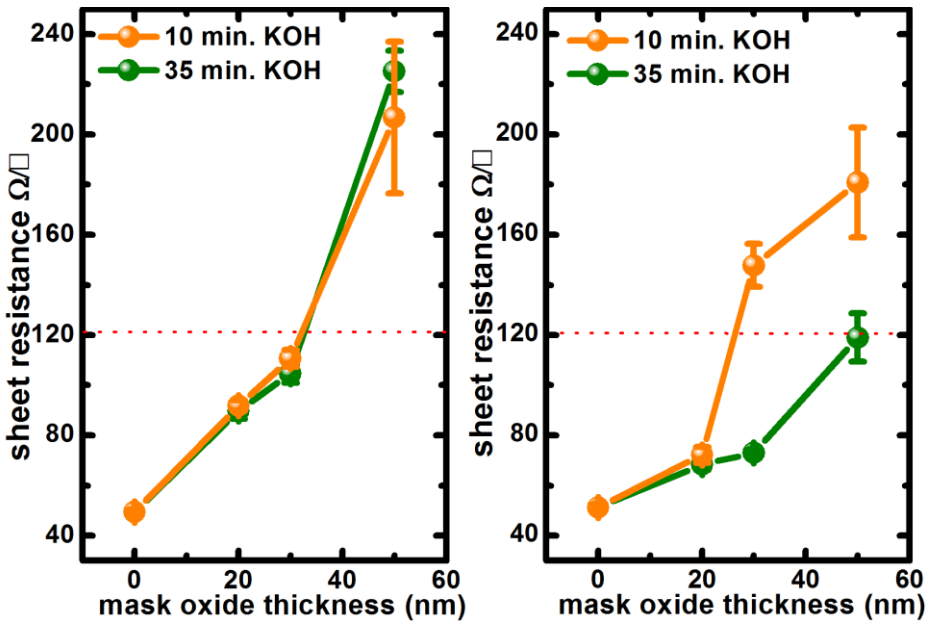
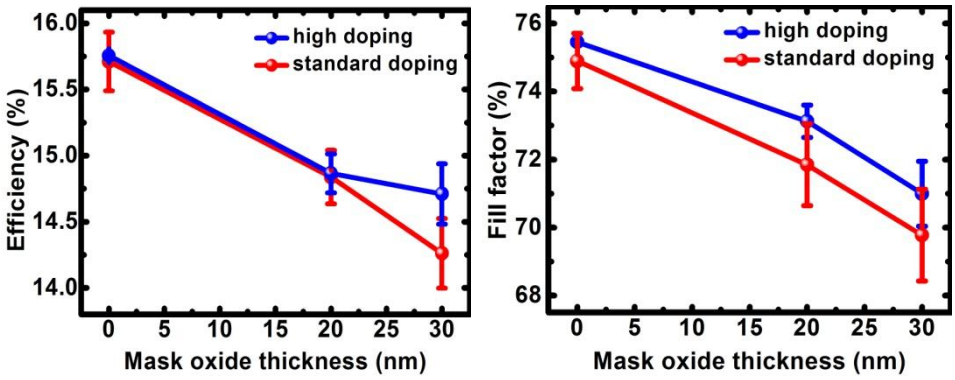


Figure 54: Effect of 10% KOH dipping duration on sheet resistance of (a) standard doping, (b) high doping samples

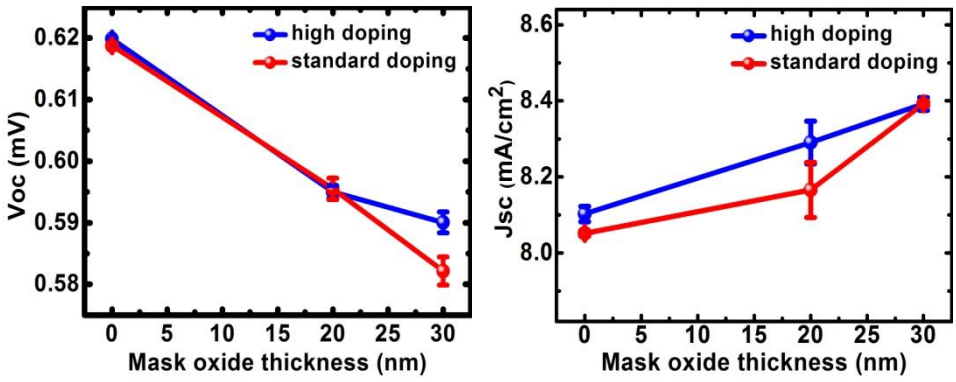
Considering Figure 52 and Figure 54 simultaneously, 20 min KOH dipping seems suitable for laser induced damage removal. After determining laser parameters and KOH dipping duration, to be able to see the effect of oxide mask thickness on cell performance, a set of 36 cells were fabricated half of which was standard doped and the other half was highly doped.



(a) **(b)**

Figure 55: Effect of mask oxide thickness on (a) cell efficiency, (b) fill factor

As seen in Figure 55, increasing oxide thickness decreased both efficiency and fill factor values of the fabricated solar cells. Zero oxide thickness, which is referring to reference set overcome selective emitter cells in performance. However, comparing selective emitter cell in terms of high and standard doping, high doping cells showed relatively better performance. For a selective emitter cell, blue response of the device is expected to improve which would result in enhanced short circuit current density and open circuit voltage. As demonstrated in Figure 56 (b), both high doping and low doping samples have higher J_{sc} values than reference ones, which means selective emitter design is working. However, considering V_{oc} values shown in Figure 56 (a), again selective emitter cells are inferior to reference cells.



(a) **(b)**

Figure 56: Effect of mask oxide thickness on (a) V_{OC}, (b) J_{SC}

At this point it could be deduced that selective emitter effect could be obtained at the first trial; but, some other problems were preventing selective emitter cells from higher performance.

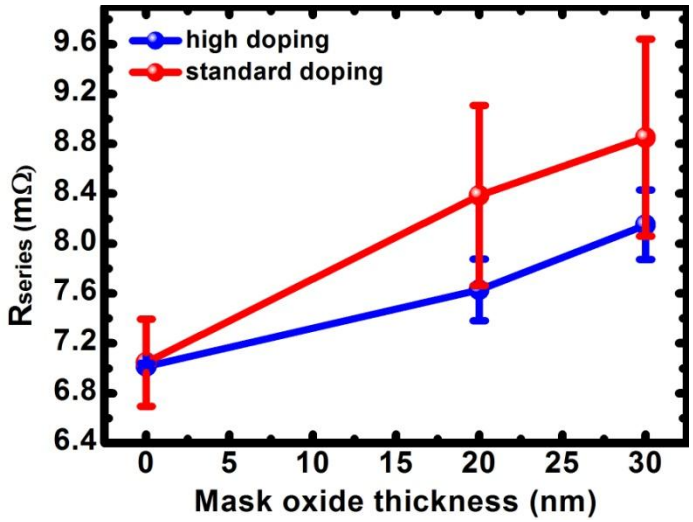
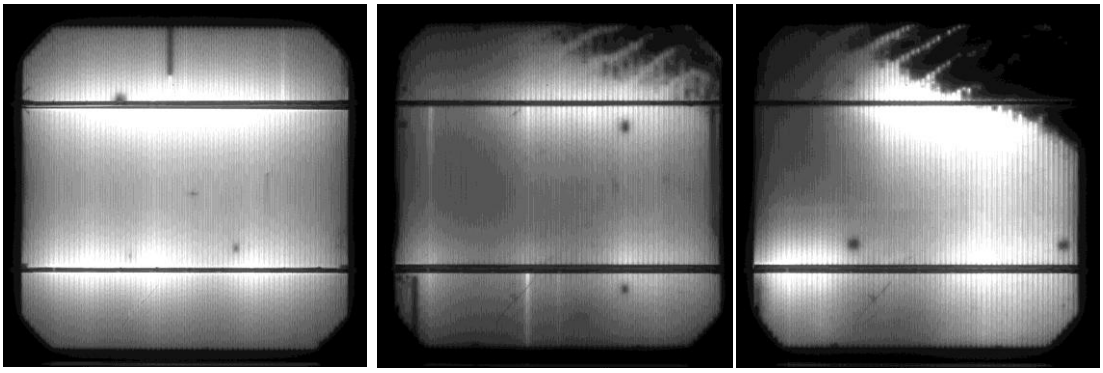


Figure 57: Effect of mask oxide thickness on series resistance

Taking Figure 57 into consideration, it can be deduced that selective emitter cells suffer from high series resistance, which explains lower efficiency values

compared to the reference cells. Moreover, relatively lower series resistance of high doping cells could be counted as the reason of their better performance compared to standard doping cells. In order to reveal the reason of high series resistance of the selective emitter cells, electroluminescence measurements were carried out.

Electroluminescence image of reference cells (Figure 58 (a)) reveals that there exist no dead regions despite single broken finger which results from the printing mask. As shown in Figure 58(b) and (c), there exist some dark areas in electroluminescence images of selective emitter cells, which means that these areas are not working properly (in other words they are *"dead"* regions).



(a) **(b)** **(c)**

Figure 58: Electroluminescence images of (a) reference cell, (b) selective emitter with 20 nm oxide mask, (c) selective emitter with 30 nm oxide mask for standard doping

These dead regions originate from contact misalignment problem and results in similar electroluminescence image for both standard doping and high doping conditions. In case of misaligned contacts, front side fingers would be in contact with the high sheet resistance emitter layer instead of lower sheet resistance grooves. However, standard Ag paste used for metallization is already optimized for 50-70 Ω/□ so when it is printed on higher sheet resistance emitters, it is possible to have high contact resistance, which will in turn increase the series resistance of the solar cell. In the case of high doping, sheet resistance of the emitter region takes a maximum value of 73 Ω/□ at 30 nm oxide which increases to 105 Ω/□ for standard

doping case. Thus, even if front Ag fingers are misaligned, they would contact with 73 Ω/□ instead of 105 Ω/□ emitter which will generate smaller contact resistance. This explains relatively lower series resistance, thus higher fill factor, higher open circuit voltage and higher efficiency outputs of high doping samples. Using Image-J software, dead area ratio to the whole cell area was calculated. Considering the effect of sheet resistance and dead area on series resistance, it is deduced that even at high dead area ratios, samples with the high doping level result in lower series resistances than standard ones as demonstrated in Figure 59 where series resistance values are labeled next to data points.

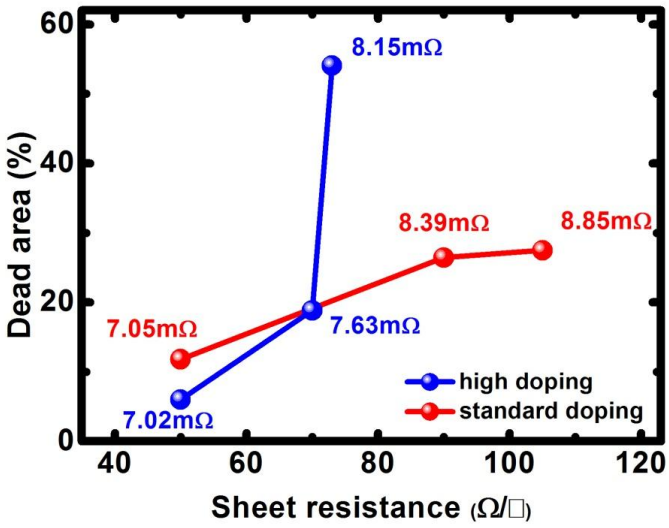


Figure 59: Effect of sheet resistance and dead area on series resistance

Upon understanding the misalignment problem and observing its effect on series resistance, optical microscope analysis was carried out to figure out at which points of the cell; printed fingers are out of contact with the opened grooves. As seen in Figure 60 (a) and (b), misaligned Ag fingers lie above opened grooves; whereas, for properly aligned contact printed Ag finger fills opened grooves (Figure 60 (c)).

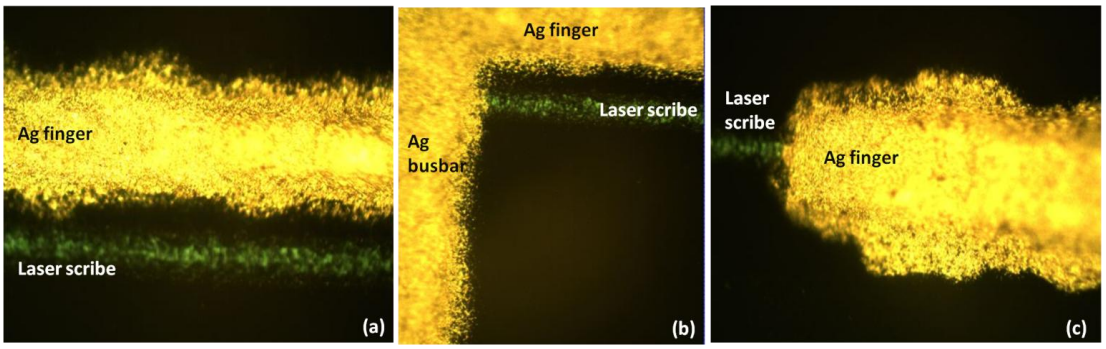


Figure 60: Optical microscope images of (a) misaligned finger, (b) misaligned finger-busbar cross-section, (c) aligned finger under 20X magnification

At this point another problem was realized that opened grooves were too narrow for overlying fingers which means even if there is no misalignment, still some part of the printed finger is in contact with the high sheet resistance emitter surface. Additionally, narrow grooves do not provide any tolerance for alignment. This condition was fixed in the latter trial.

In order to estimate the performance of fabricated cells under negligible series resistance assumption, Suns-Voc measurements were carried out. During this measurement, expected short circuit current density and wafer thickness are inserted as the input to the software, then V_{oc} of the cell is measured; efficiency and fill factor values are approximated by two diode model whose circuit representation is shown in Figure 61.

According to two diode model, the recombination in the solar cell is dominated by surface and bulk recombination at high voltages and this situation corresponds to a diode whose ideality factor is close to one. However, recombination in the junction region becomes dominant at low voltages and it corresponds to a diode whose ideality factor is close to two. So that, by adding the latter diode parallel to the former one, junction recombination is modeled.

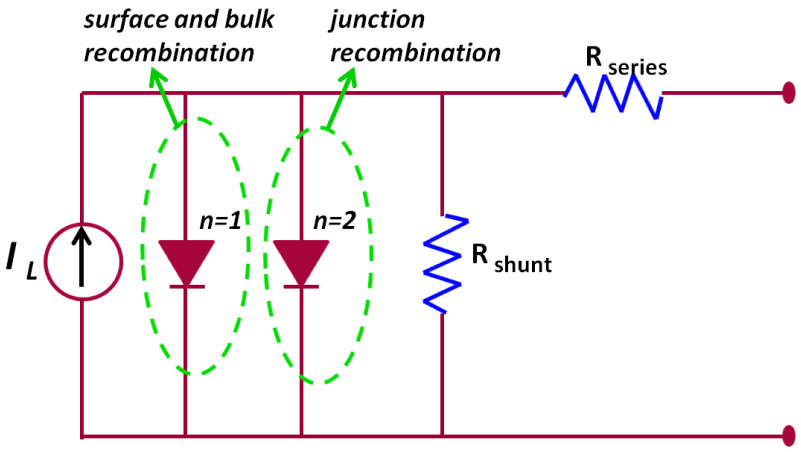


Figure 61: Circuit representation of two diode model

According to Figure 62 (a), reference cells of both high and standard doping sets have higher efficiency values compared to selective emitter cells, which means even if series resistance were decreased, there would still be some other factors preventing selective emitter cells having better performance.

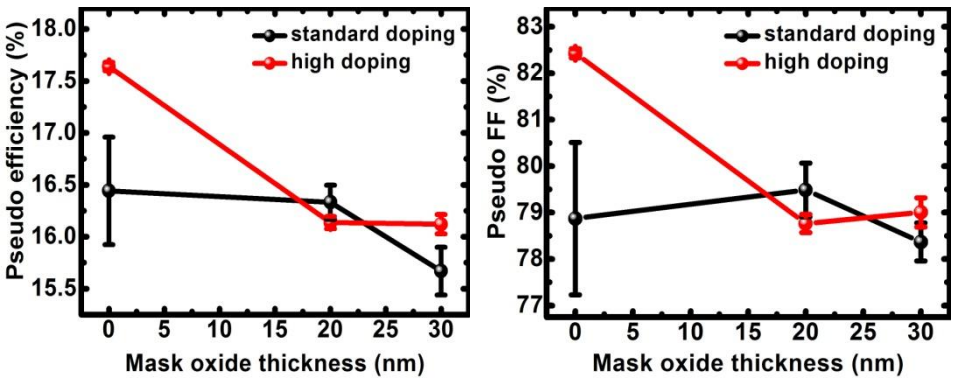


Figure 62: Effect of mask oxide thickness on (a) pseudo efficiency, (b) pseudo fill factor

For 20 nm mask oxide; pseudo efficiency of standard doping cells is greater than that of high doping cell which could be related to relatively lower phosphorous

concentration at the surface. Lower dopant concentration is expected to enhance V_{oc} and FF due to reduced surface recombination velocity while Figure 62 (b) and Figure 63 confirm this condition.

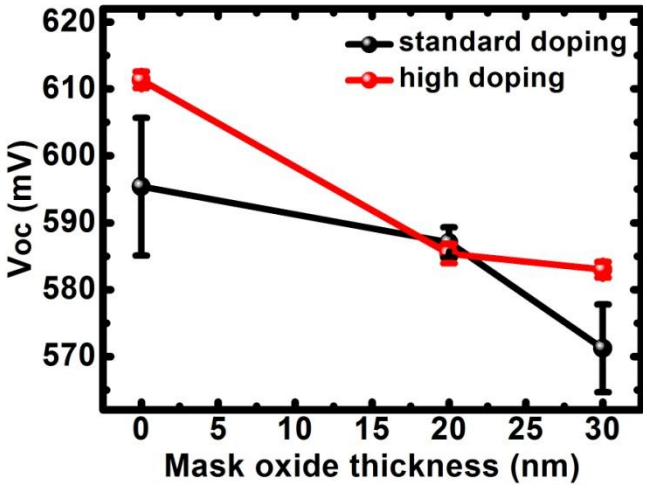


Figure 63: Effect of mask oxide thickness on V_{oc}

However, when mask oxide thickness is increased to 30 nm, dopant atom concentration significantly reduces which will in turn weakens electric field at the p-n junction thus both V_{oc} (Figure 63) and FF (Figure 62 (b)) is expected to reduce as a result of weak carrier separation. and collection properties of the cell. As a result, for standard doping cells, efficiency will inevitably decrease.

In addition to measurement of above mentioned cell parameters, two diode model reverse saturation current components J_{01} and J_{02} could also be extracted by Suns-Voc measurements. According to two diode model, J_{01} stands for minority carrier recombination in the base and emitter region whereas J_{02} accounts for the recombination in the depletion region which is expected to be in the order of 10^{-10} A/cm^2 [48]. As demonstrated in Figure 63 (a) reference cells have lower J_{01} values than selective emitter cells have. Although dopant concentration is decreasing, laser damage given to silicon surface could increase density of trap states in the emitter region which enhances surface recombination.

Relatively higher J_{01} values of standard doping cells could be attributed to higher contact resistance between lightly doped emitter region and front Ag fingers which results in reduced collection probability of carriers at the corresponding contacts thus increased recombination rate.

Moreover, since base wafers are of the same part of the ingot, all processed cell could be assumed to be of the same base material quality. However, since high doping samples were exposed to $POCl_{3(g)}$ for a longer time, more effective gettering could be attained compared to standard doping cells which would also explain lower J_{01} values of high doping samples

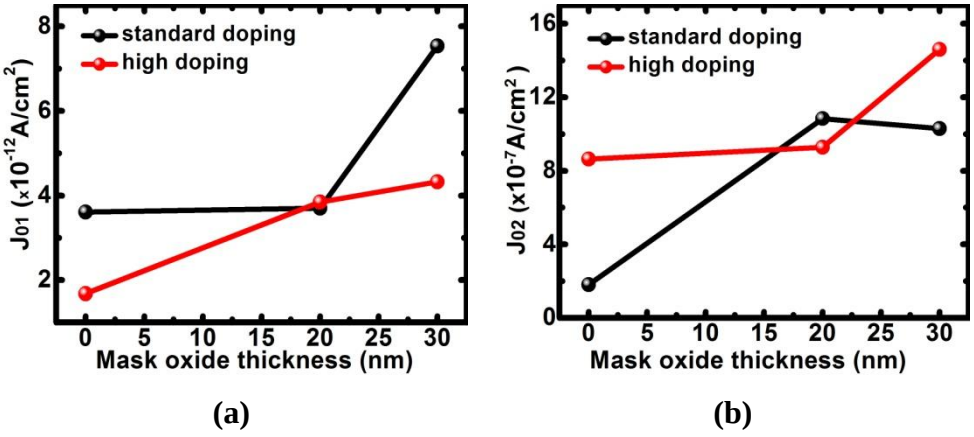


Figure 64: Effect of mask oxide thickness on (a) J_{01} and (b) J_{02}

Considering J_{02} (Figure 64(b)), reference samples have slightly lower values again which imply higher junction quality. When magnitude of J_{02} is taken into consideration, not only selective emitter cells but also reference cells are 1000 and 100 times greater than the optimum value which should be around 10^{-10} A/cm^2 [48].

As the last step of device characterization, external quantum efficiency (E.Q.E.) measurements were carried out. Both high doping and standard doping samples' results show an enhancement in the UV region which is expected as a natural result of reduced dopant concentration at selective emitter surface. It is known that reduced dopant concentration will decrease carrier recombination

velocity at the surface. Since high energy photons are absorbed at the surface, carriers corresponding to these photons will be created in the vicinity of surface so that these carriers are more likely to recombine with the dopant atoms whose concentration is very high at the surface of silicon. Thus, when dopant concentration at the the surface is reduced, their recombination probability with generated carriers will also decrease.

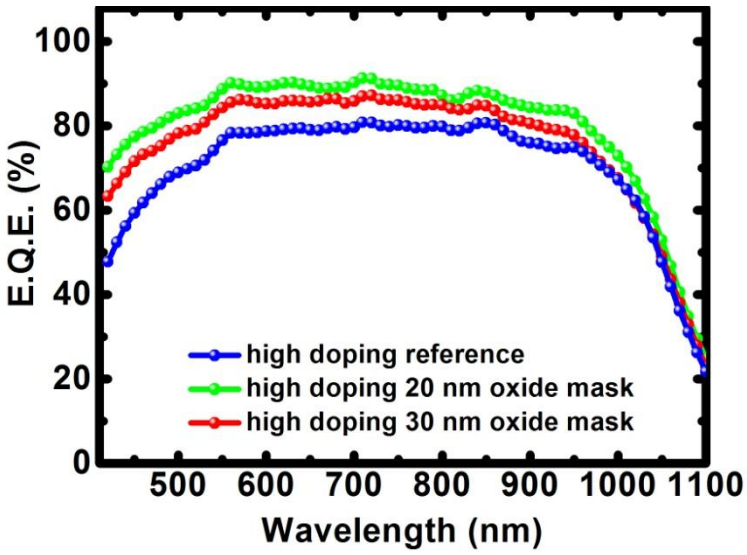


Figure 65: Effect of mask oxide thickness on external quantum efficiency of high doping samples

As seen in Figure 65, both 20 nm and 30 nm oxide mask have better blue response than reference sample whereas 30 nm oxide sample's response is relatively higher which could be related to further reduction of dopant concentration compared to 20 nm oxide samples. When current density-voltage characteristics of fabricated cells are plotted as shown in Figure 66, it is clearly seen that selective emitter cells suffer from lower fill factor and lower efficiency values compared to the reference cell. Moreover, open circuit voltages of the selective emitter cells are lower even if they have higher short circuit current densities. Also, 30 nm oxide sample has slightly higher short circuit current density than 20 nm oxide layer samples does whereas its open circuit voltage is slightly smaller than that of 20 nm oxide sample.

This improvement in J_{sc} is related to lower dopant atom concentration when mask oxide thickness is increased from 20 to 30 nm whereas the decrease in V_{oc} is due to increased series resistance between the emitter and metal contacts.

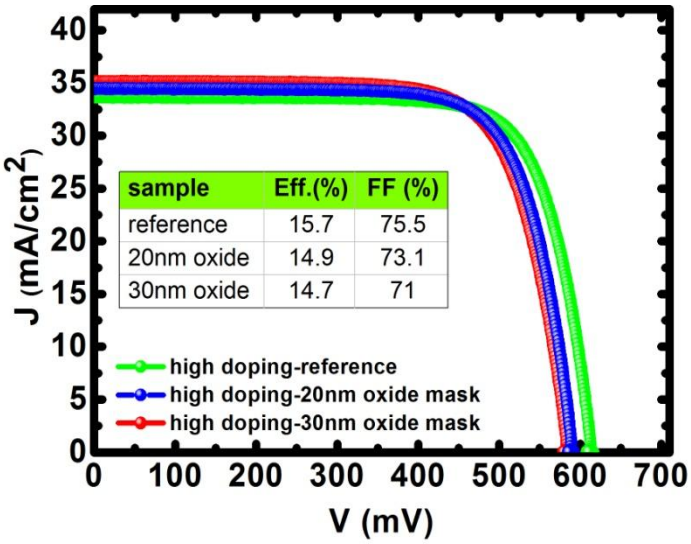


Figure 66: J-V characteristics and corresponding efficiency and fill factors of high doping selective emitter and reference cells

5.1.2. Second Run

As the second run for selective emitter fabrication, previously utilized laser has been replaced with a new marking one whose properties have been mentioned in the previous chapter. Lower scribing and corner turning speed of the previous laser were its main disadvantages that really decreased the process throughput. Prior to starting cell fabrication sequence, new laser parameters had to be optimized according to the process requirements. For this, solar grade, textured wafers with varying mask oxide thicknesses of 20, 30 and 50 nm was prepared. Taking first run's results into account; laser power was decreased as much as possible so that laser current was set 15%, 20% and 25% of its maximum value. KOH dipping duration

was already set to 20 min. But different than the first run, an additional HF dipping step was aimed to be optimized at this run.

During KOH dipping, post HCl dipping and DI-water rinses in between, laser damaged surface of Si is prone to be oxidized. This oxide layer between Si and Ag finger would generate a potential barrier which would resist against carrier transport during operation of the corresponding solar cell. In order to be sure about how formed oxide layer affects cell performance, 1%HF dipping step was studied for 5, 10 and 17 seconds.

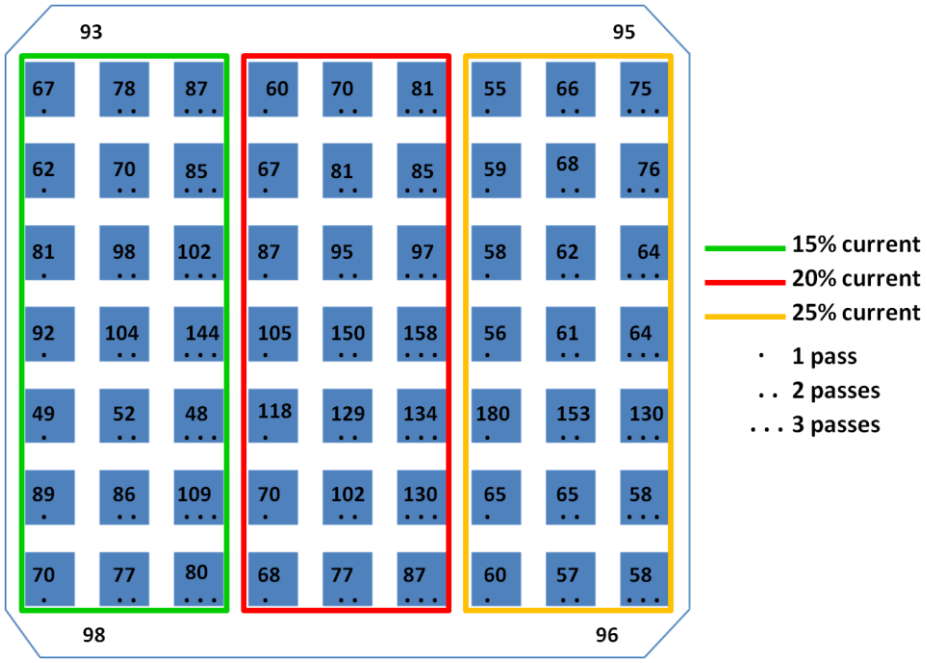


Figure 67: Sheet resistance mapping on a full wafer with 4cm^2 laser scanned squares of different parameters

In order to scan laser parameter-sheet resistance relation as detailed as possible, each wafer was patterned with different laser powers, different laser speeds and different pass numbers. As demonstrated in Figure 67, one third of the whole wafer was scanned with 15% laser current, one third was with 20% and the rest was scanned with 25% laser current and corresponding regions were shown within green,

red and yellow rectangles, respectively. Dots at the bottom of each square define how many times the laser beam scanned associated area and this quantity was named as *"pass number"* varying from 1 to 3. Numbers written in the small squares are sheet resistance values; whereas, the numbers written at square-free region of the wafers define sheet resistance under mask oxide layer, which will be equal to emitter resistance upon the fabrication of the corresponding cell.

For different laser scan rates, effect of HF dipping duration, doping recipe and mask oxide thickness was investigated.

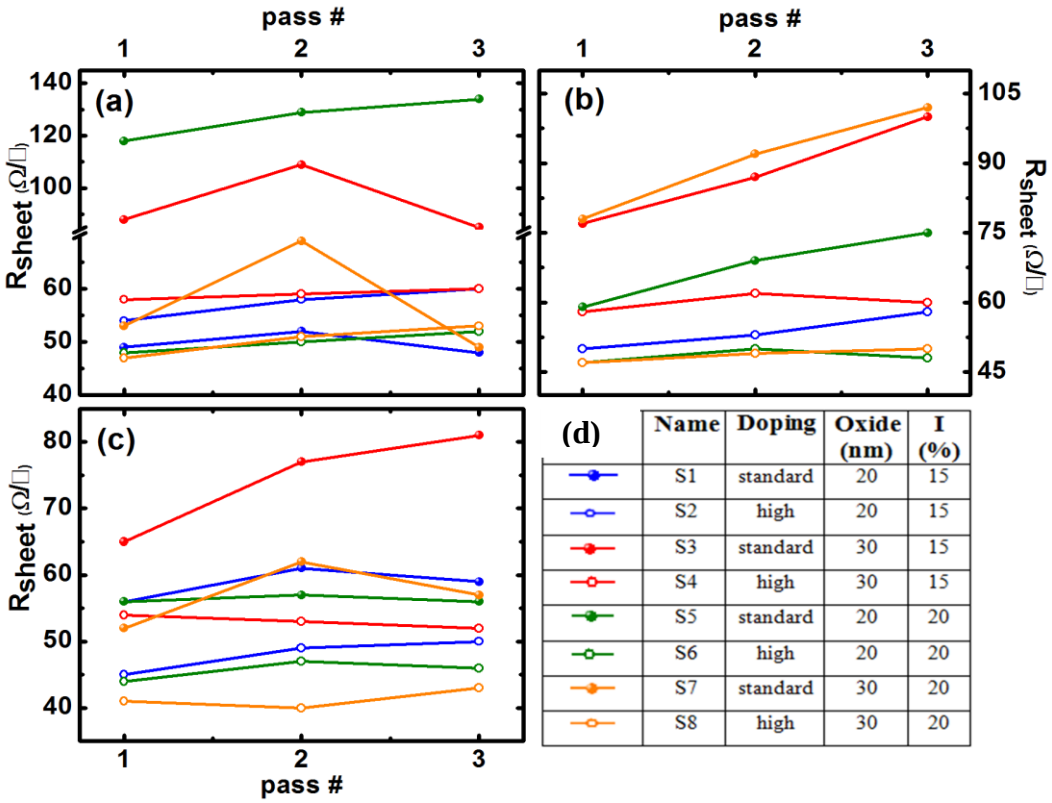


Figure 68: Effect of (a) 5sec., (b) 10sec., (c) 17 sec HF dipping on sheet resistance of both high and standard doping samples with 20,30 and 50 nm mask oxide layers for laser speed: 3mm/s with table (d) of symbol about corresponding doping recipe, oxide thickness and laser current. Lines are for visual aid

In Figure 68 (a), (b) and (c); sheet resistance values for a constant laser scan rate were plotted as a function of pass number for 5sec., 10sec. and 17 sec HF

dipping, respectively. In the plots, lines are used for visual aid. Also in the same figure (d); plot symbols corresponding to doping, mask oxide thickness and laser current values were tabulated.

Since 50 nm mask oxide resulted in sheet resistance values changing from 450 Ω/□ to 140 Ω/□ as HF dipping duration was increased from 5 to 17 sec, corresponding sheet resistance data wasn't demonstrated on the same plot. Although sheet resistance behavior was plotted for a constant value of laser speed, the same trend was followed for the other speed values.

As shown in Figure 68, increasing input current of the laser decreases sheet resistance since more SiO_2 can be ablated from the surface which facilitates phosphorous through oxide layer. Also, sheet resistance difference in-between high doping samples are much less compared to that of standard doped ones, which means doping profile is not significantly affected by mask oxide thickness for high doping recipe. Sheet resistance of the oxide ablated region is almost equal to that of oxide covered region and this reduces selectivity of the emitter significantly for the case of high doping. Considering high doping samples, sheet resistance and pass number dependence of samples with different mask oxide thickness was not conclusive. Low sheet resistance values were obtained even the thickest mask oxide was utilized. As a result, high doping recipe was determined to be inappropriate. Considering the effect of HF dipping, it is clear that increasing dip duration reduces sheet resistance since mask oxide thickness will be reduced thus more dopant atoms would penetrate through underlying silicon.

Moreover, in order to see laser scan speed-sheet resistance relation, sheet resistance vs. speed graph has been plotted for 20 nm oxide mask, standard doping, 5sec. HF dipped samples. As seen in Figure 69, for each different pass number, sample sheet resistance shows similar nonlinear behavior. Peak resistance value increases with increasing pass number, which could be related to increased surface damage. Scan speed was determined in a way that total process time and laser induced damage would be decreased simultaneously as the sheet resistance is kept within an appropriate range. As a result, scan speed of the laser was determined to be 2.86 for the following cell fabrication where corresponding data points are shown within a square in Figure 69.

For cell fabrication, laser current was chosen to be 25%, since 15% current was observed to be insufficient and 20% current could not generate enough contrast, which would make front Ag alignment difficult. After determining new laser parameters, three different mask oxide thicknesses were processed with standard doping recipe. Emitter doping profile was designed to have a sheet resistance of 50-60 Ω/□ under metal contacts and 80-90 Ω/□ over the contact free region. Based upon the experience from the first run, this time opened groove width was ~120-130μm to provide some tolerance towards possible contact misalignments. Also half of the processed cells were oxidized via dry oxidation at 850^{o}C to enhance surface passivation.

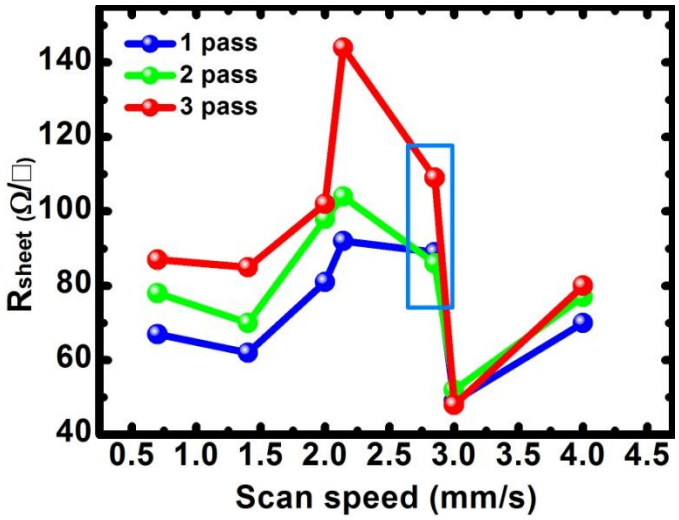
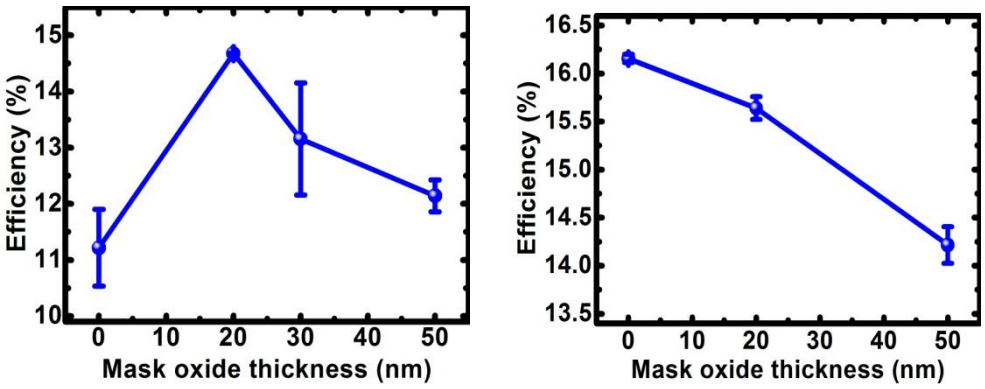


Figure 69: Effect of laser scan speed on sheet resistance. Lines are for visual aid

As could be deduced from Figure 69, while 5 sec HF dipping was enough for 20 nm or 30 nm which did not affect 50 nm mask oxide significantly. Even 17sec dipping resulted in very high sheet resistances under mask oxide whose graphs weren't plotted in the same figure. Comparing performance of the fabricated cells as shown in Figure 70, selective emitter ones with passivation oxide could outperform corresponding reference cells in efficiency. Also, increasing oxide mask thickness,

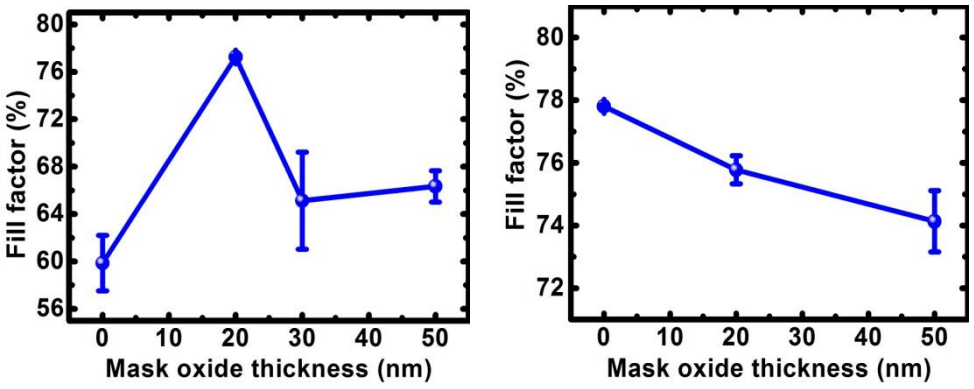
decreased efficiency of selective emitter cells; those both with and without passivation oxide.



(a) **(b)**

Figure 70: Effect of mask oxide thickness on cell efficiency of fabricated cells (a) with oxide passivation, (b) without oxide passivation. Lines are for visual aid

When fill factors are taken into consideration, a similar behavior with efficiency values was observed.



(a) **(b)**

Figure 71: Effect of mask oxide thickness on fill factor of solar cells (a) with oxide passivation, (b) without oxide passivation. Lines are for visual aid

On one hand; FF values of oxide passivated selective emitter cells are significantly greater than those of reference cells even though mask oxide thickness increases (Figure 71 (a)). On the other hand, reference cells without oxide passivation have greater FF values and increasing mask oxide thickness decreases FF values of the selective emitter cells (Figure 71(b)).

In case of V_{oc}, significantly lower values have been observed in oxide passivated cells (Figure 72 (a)). Although selective emitter cells have relatively higher V_{oc} values, such a decrease in V_{oc} of all oxide passivated wafers indicates a possible series resistance problem. Contrary to passivated samples, for the cells without oxide passivation, reference cells have the highest V_{oc} value (Figure 72 (b)); whereas, increasing mask oxide thickness decreased corresponding V_{oc} values of selective emitter cells

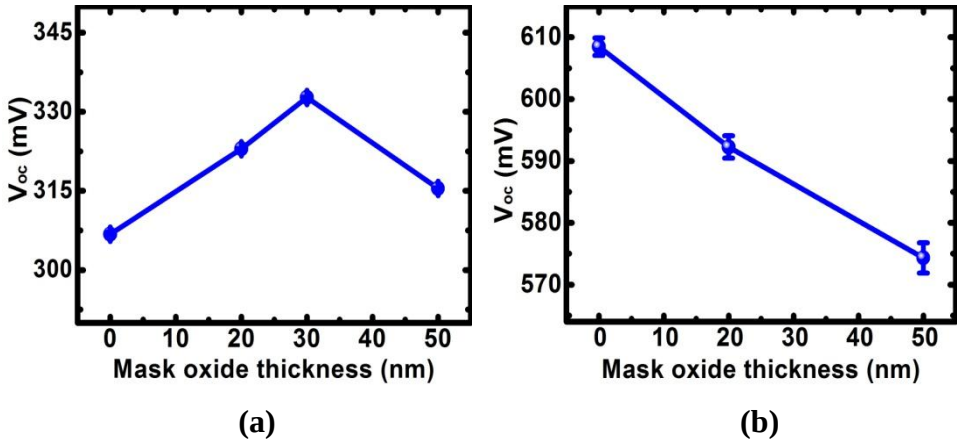
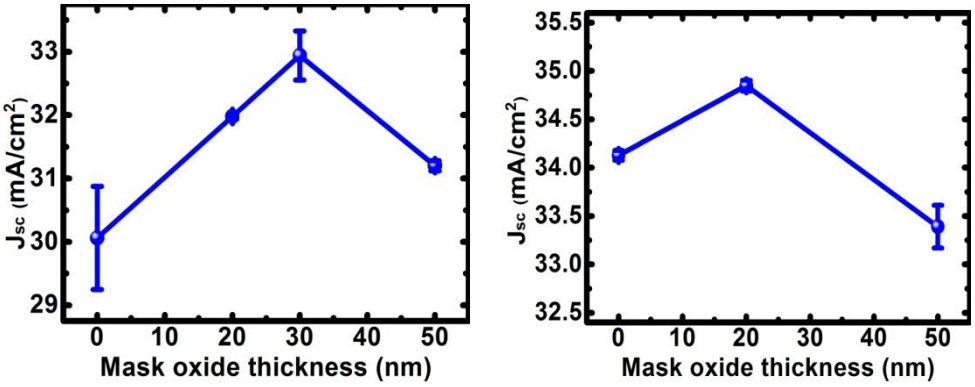


Figure 72: Effect of mask oxide thickness on Voc (a) with oxide passivation, (b) without oxide passivation. Lines are for visual aid

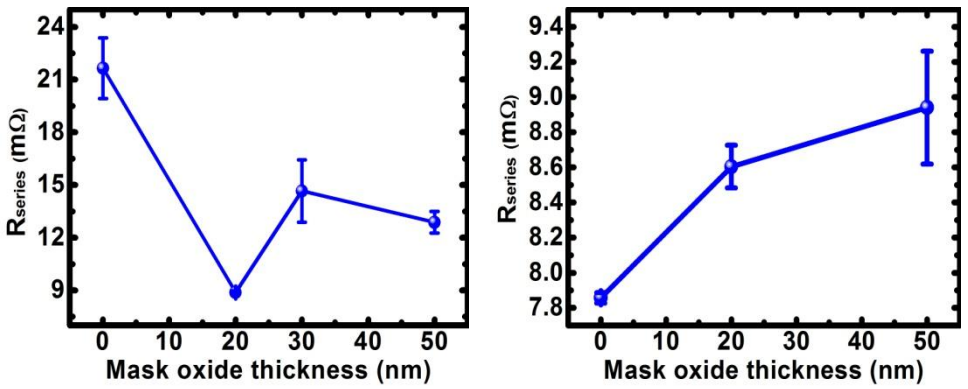
Despite relatively lower efficiency and fill factor values, selective emitter effect could apparently be observed in J_{sc} results (Figure 73). As expected, selective emitter cells both with and without oxide passivation, have higher J_{sc} values than reference cell which is apparently due to reduced front surface recombination velocity. Relatively lower J_{sc} values belonging to oxide passivated cells could be related to some contact problems.



(a) **(b)**

Figure 73: Effect of mask oxide thickness on J_{SC} (a) with oxide passivation, (b) without oxide passivation. Lines are for visual aid

Series resistance behavior of the fabricated cells was as expected. That is; oxide passivated selective emitter cells had lower series resistance compared to reference cells of the same set (Figure 74).



(a) **(b)**

Figure 74: Effect of mask oxide thickness on R_{series} (a) with oxide passivation, (b) without oxide passivation. Lines are for visual aid

Increasing mask oxide thickness increased corresponding series resistance with a similar manner as seen in FF behavior case.

Passivation of opened grooves by oxide layer could be counted as the reason for higher efficiency, FF, Voc and Jsc values of selective emitter cell compared to the reference ones. Comparing Figure 74(a) and Figure 74(b), it is clear that average series resistance of the oxide passivated cells are significantly greater than that of oxide free cells, which could be counted as the reason for inferior cell performance. For non-oxidized cells, on the other hand, increasing mask oxide thickness increases series resistance; thus, reference cells have the lowest series resistance explaining their better performance.

After I-V characterization of the fabricated cells, electroluminescence measurements were carried out to observe whether high series resistance of the cells are due to contact misalignment problem or not. Comparing 20, 30 and 50 nm of mask oxide samples for 5sec HF dipping; 30 nm mask oxide samples were observed to have more dead regions (Figure 75) explaining very low efficiency values of this set.

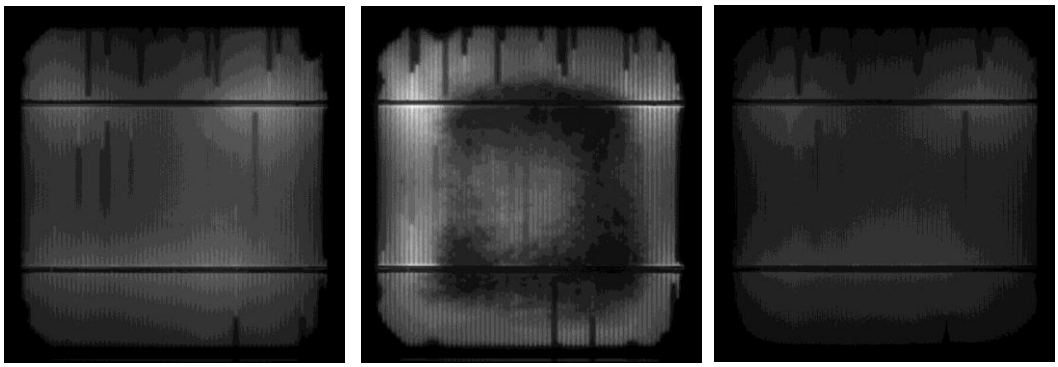
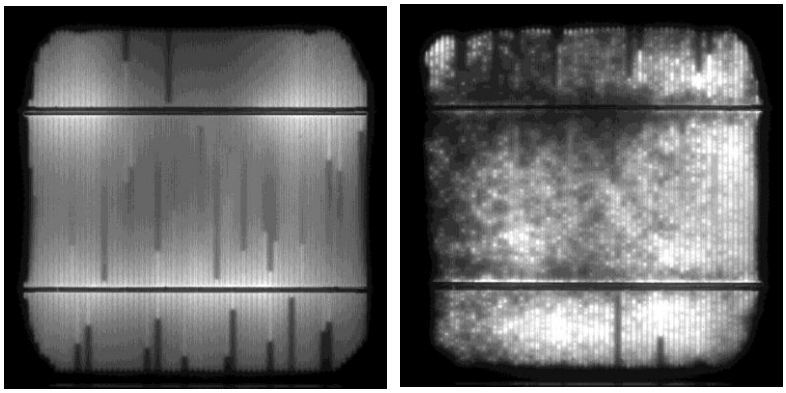


Figure 75: Electroluminescence images of selective emitter cells with (a) 20, (b) 30, and (c) 50 nm mask oxide. Lines are for visual aid

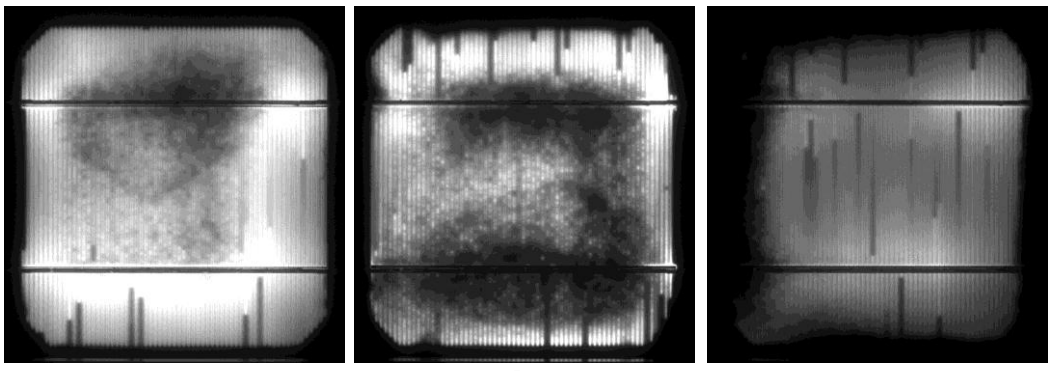
Also it stands out that regardless of mask oxide thickness, all selective emitter cells suffer from dead fingers. As seen in Figure 76, dead fingers are also seen on reference cells; which means that they're not due to alignment problem, instead; dead finger results from printing mask contamination.



(a) **(b)**

Figure 76: Electroluminescence images of reference cells (a) without oxide passivation, (b) with oxide passivation. Lines are for visual aid

Additionally, reference cells with oxide passivation suffer from far more serious problems because almost whole cell is not working properly (Figure 76(b)). The cell is not completely dead since there exist white points in-between black ones, corresponding to working parts of the cells. It is possible to observe such a result if front Ag and rear Al is not in good contact with the silicon wafer. That is, grown oxide layer acted as a barrier against diffusion of Ag and Al atoms which explains high series resistance of all oxide passivated samples.

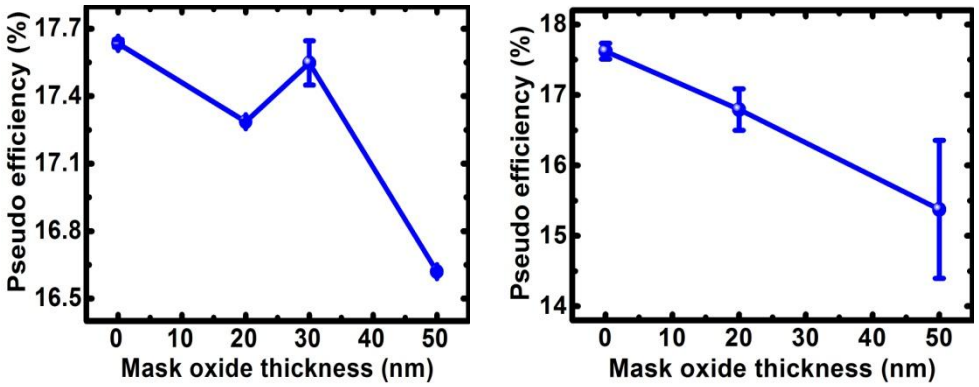


(a) **(b)** **(c)**

Figure 77: Electroluminescence images of oxide passivated selective emitter cells with (a) 20, (b) 30 and (c) 50 nm mask oxide. Lines are for visual aid

Not only reference samples but also selective emitter cells suffer from ineffective contact formation problem when they have passivation oxide layer. A similar pattern as Figure 76(b) can be seen in Figure 77 but dead area amount of selective emitter cells less than that of reference cells and this reduced dead area amount explains their better performance. 20 nm mask oxide cells have less dead layer amount compared to 50 nm oxide one which explains their relatively higher performance. Also, 30 nm oxide cells have the highest dead area amount which explains why they couldn't perform an acceptable level.

After electroluminescence, Suns-V_{oc} measurements were carried out to have an estimate of cell performance without the series resistance effect.

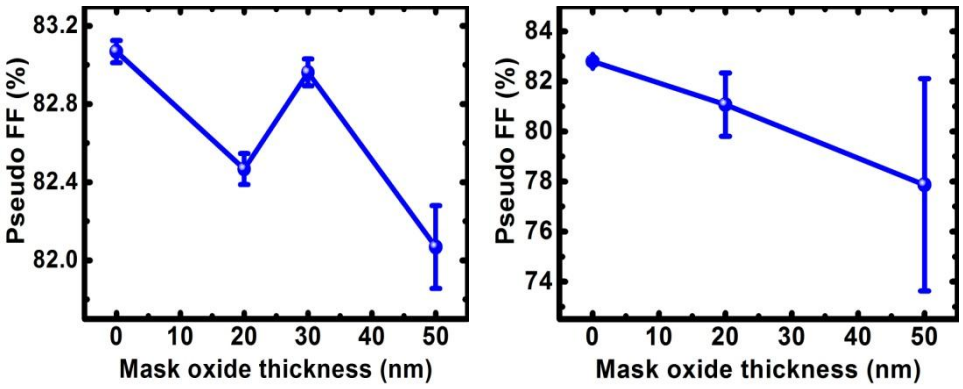


(a) **(b)**

Figure 78: Effect of mask oxide thickness on pseudo efficiency (a) with (b) without oxide passivation. Lines are for visual aid

As seen in Figure 78, pseudo efficiencies are significantly greater than real efficiency values for both reference and selective emitter cells, which means all fabricated cells suffer from series resistance problem. Not only for oxide passivated cells but also for un-passivated ones, increasing mask oxide thickness decreases pseudo efficiencies.

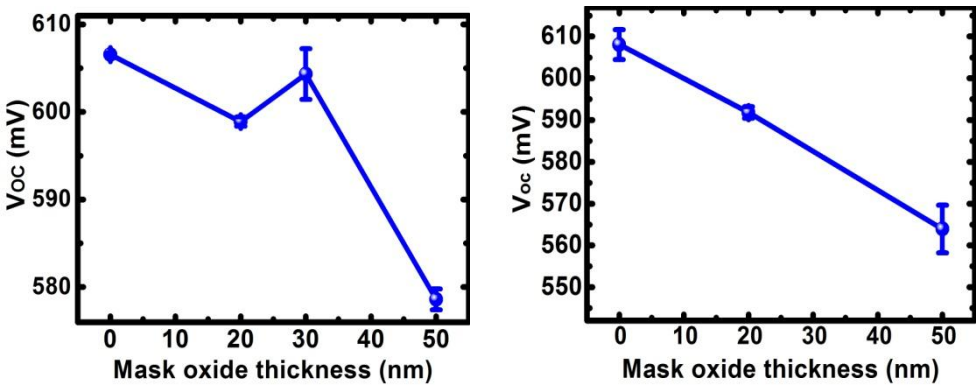
Pseudo FF shows a similar behavior as pseudo efficiencies that is increasing oxide mask thickness decreases pseudo FF and reference cells are superior to selective emitter ones (Figure 79).



(a) **(b)**

Figure 79: Effect of mask oxide thickness on pseudo fill factor (a) with (b) without oxide passivation. Lines are for visual aid

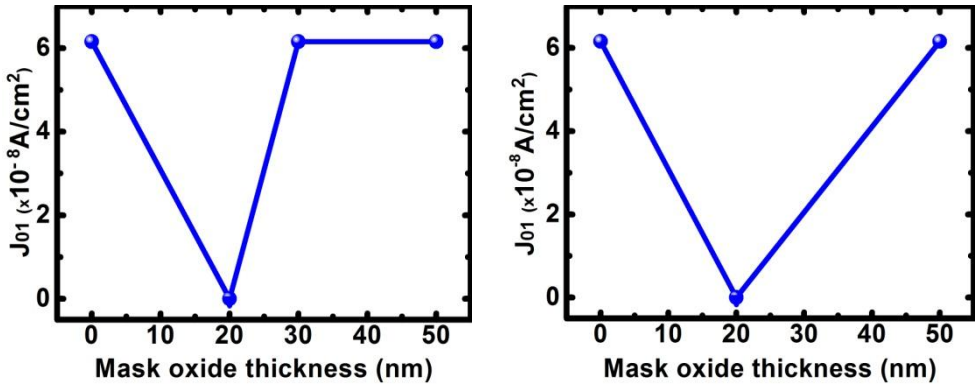
Measured V_{oc} values also follow the same trend as pseudo efficiency and pseudo FF. Cells with oxide passivation have slightly lower V_{oc} values compared to without oxide samples which could be related to increased series resistance due to existing oxide layer (Figure 80).



(a) **(b)**

Figure 80: Effect of mask oxide thickness on Voc (a) with (b) without oxide passivation. Lines are for visual aid

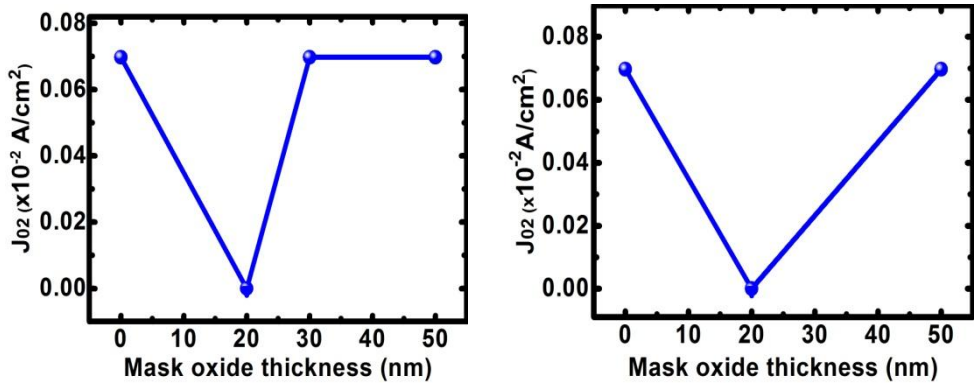
Emitter and bulk material related component of the reverse saturation current for both with and without oxide passivation cells is on the order of 10^{-8} A/cm^2, which is much higher than the value that it is supposed to be (Figure 81).



(a) **(b)**

Figure 81: Effect of mask oxide thickness on J_{01} (a) with (b) without oxide passivation. Lines are for visual aid

On the other hand, depletion region related component of reverse saturation current is on the order of 10^{-2} A/cm^2 (Figure 82); whereas, its ideal value is around 10^{-10}A/cm^2.



(a) **(b)**

Figure 82: Effect on mask oxide thickness on J_{02} (a) with (b) without oxide passivation. Lines are for visual aid

Samples either with or without oxide passivation have very high reverse saturation current values regardless of their emitter profile. If only selective emitter cells had such high values, the reason would be related to selective emitter fabrication process. However, reference cells also suffer from the same problem. The reason of such high saturation current could be associated with low junction quality. After realizing high reverse saturation current problem, EQE measurements were carried out to observe whether there is a selective emitter effect in blue response or not.

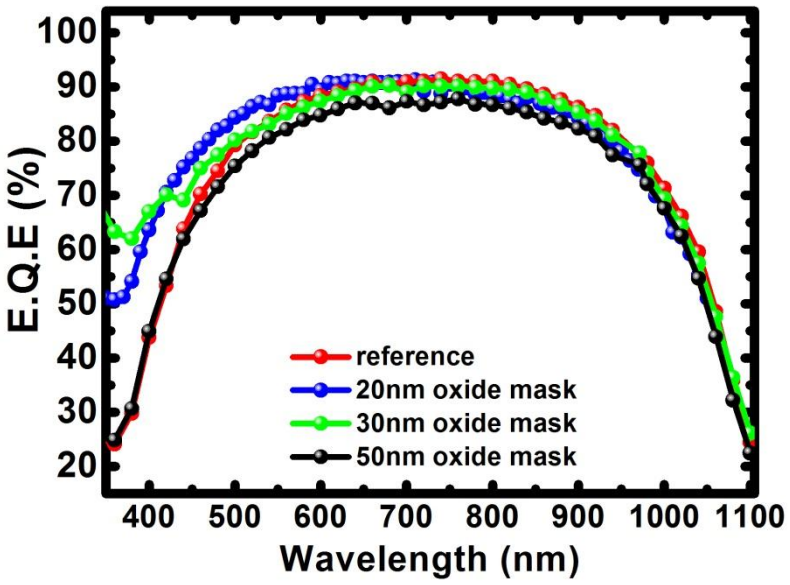


Figure 83: External quantum efficiency comparison of fabricated solar cells

As seen in Figure 83, selective emitter cells have better response in short wavelengths compared to the reference cell. Moreover, it could be deduced that increasing mask oxide thickness decreases EQE of the corresponding cells and oxide thickness of 20 nm seems to be the optimum mask oxide thickness for designed fabrication sequence.

As the final step of characterization, contact resistance measurements were carried out as described in Chapter 4.3.1.7.

As shown in Figure 84, measured resistance values were almost linearly dependent on the contact separation.

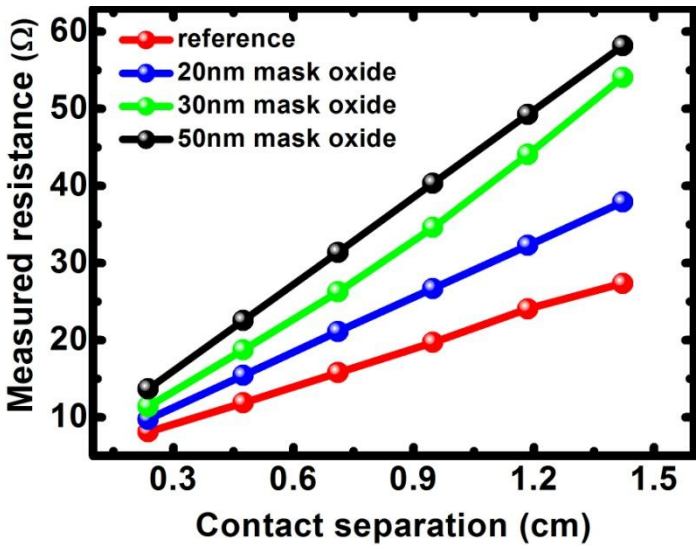


Figure 84: Resistance measurements by transferring line method. Lines are for visual aid

By extrapolating above plotted graphs to zero contact separation, contact resistances can be extracted. Through the application of the same procedure for at least two samples from each set, average contact resistance-mask oxide relationship can be plotted as shown in Figure 85. For without passivation oxide case, the contact resistance of reference samples are lower compared to that of selective emitter ones, which could be related to the damage given to silicon surface during laser scribing step. Since increasing oxide mask thickness increases sheet resistance, contact resistance between the metal and underlying Si will also increase (Figure 85).

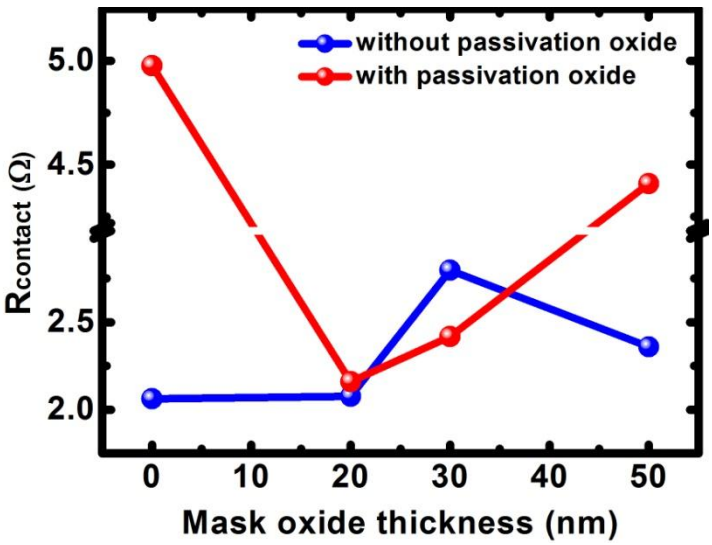


Figure 85: Effect of mask oxide thickness on contact resistance. Lines are for visual aid

The same condition holds true for samples with passivation oxide layer. However, this time selective emitter cells have relatively lower contact resistances than the reference cells. Considering series resistance values of samples with passivation oxide layer (Figure 74(a)) reference cells were observed to have higher resistance values. It could be deduced that the oxide passivation layer is not thin enough to generate required, low series resistance but still able to passivate laser damaged regions under metal contacts of selective emitter cells. Even 50 nm mask oxide samples have lower contact resistance values than the reference cells (Figure 85) which could be related to the reduced dangling bond concentration provided by oxide passivation.

5.1.3. Third Run

As the final fabrication run, all gained experience from previous sets of samples was brought together and a new set of samples was processed. Mask oxide thickness was set to 20 nm, doping recipe was set only to standard doping, laser parameters were chosen as 20% current with scan speed of 1.42 mm/s, HF dipping step was completely removed from process sequence to save mask oxide quality,

KOH dipping was reduced to 10 min. Different than the previous sets, gettering effect was tried to be comprehended. It was necessary to investigate this since existence of an oxide layer on wafer surface during doping could weaken gettering effect. For this, half of the samples were oxidized at 800^{o}C for 2 hours prior to the formation of mask oxide layer. Gettering oxidation was carried out via dry oxidation and formed oxide layer was etched before selective emitter process flow started. By this, at least some part of the impurities in bulk Si was aimed to be accumulated within the growing oxide layer which would be removed via HF etching afterwards. Also, in order to understand the effect of wafer quality on fabricated cells, a set of FZ samples was prepared with an equal number of samples as Cz set. After doping and cleaning steps, half of each set was oxidized at 850^{o}C to provide surface passivation. But this time, oxidation duration was 40 min which was 80 min in the previous run.

Front side finger alignment has been the most challenging step along all selective emitter fabrications. For the first run, where small squares were used as alignment marks, the fabricated cells suffered from serious contact misalignment problem. For the second run, where last finger of the front mask was scribed with higher laser power than scribing power to generate some contrast, but it didn't work properly. For the last run, plus symbols were added between two subsequent fingers at the top left and bottom right of the wafer as alignment marks and even though this method didn't make alignment less challenging, it helped us find a new way of proper alignment.

At the end of process sequence, 25 selective emitter cells were fabricated; 11 of which were passed through gettering oxidation whereas remaining 13 cells were kept as without gettering samples. 5 cells from with gettering set, 6 cells from without gettering set and 6 cells out of 12 reference samples were oxidized at 850^{o}C to form passivation layer. The same set of samples was also prepared for FZ wafers. After oxidation for passivation layer formation, standard cell fabrication protocol was followed for all wafers. Characterization of fabricated cells started with I-V measurements. As demonstrated in Figure 86, reference cells of both Cz and FZ wafers had higher efficiency values than corresponding selective emitter cells which were labeled as "*se*".

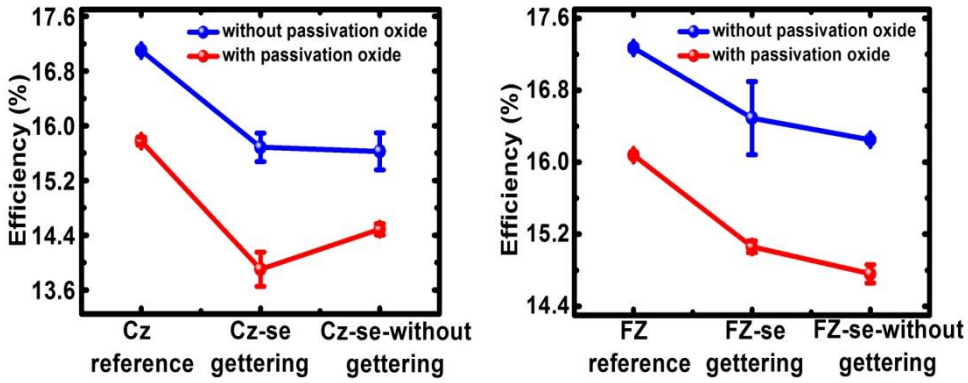
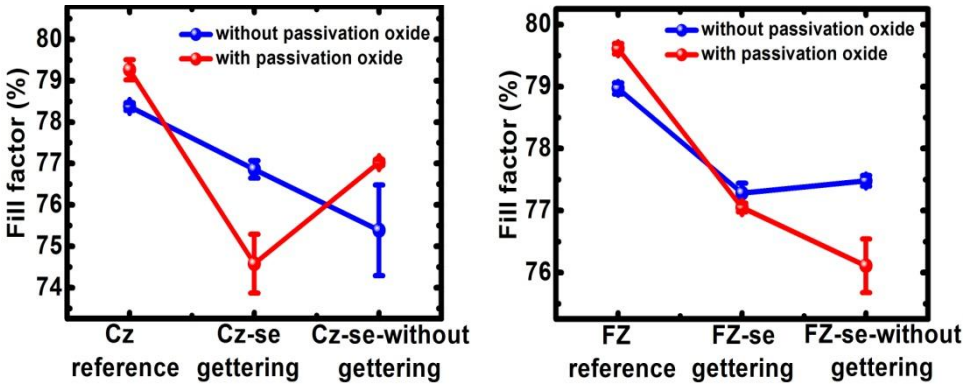


Figure 86: Efficiency values of fabricated (a) Cz and (b) FZ cells. Lines are for visual aid

Moreover, not only reference ones but also selective emitter cells of FZ set are superior to Cz set which could be related to higher wafer quality. It could be deduced that gettering affected performance of both with and without passivation oxide selective emitter cells of FZ set positively (Figure 86). On the contrary, gettering either provided little improvement on efficiency or didn't work out for without and with passivation oxide cells of Cz set. Since Cz wafers have higher impurity concentrations than FZ wafers, it seems that the foreseen gettering recipe was insufficient for Cz wafers.

Considering FF values, reference cells of both Cz and FZ sets are superior to selective emitter ones (Figure 87); although, FZ cells have relatively higher FF than Cz cells. For Cz set, samples without passivation oxide layer have higher FF values if gettering is applied whereas samples with passivation oxide layer have higher FF values if gettering is not applied.

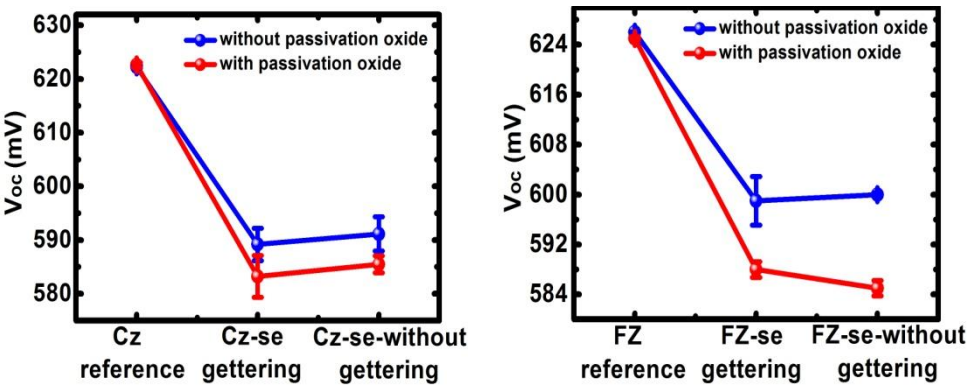


(a) **(b)**

Figure 87: Fill factor values of fabricated (a) Cz and (b) FZ cells. Lines are for visual aid

Although samples without passivation oxide layer have higher FF values for gettering and without gettering sets, difference between samples without and with oxide passivation layer gets bigger for without gettering case.

For the case of V_{oc}, behavior of Cz and FZ samples are similar except with oxide passivation samples of FZ set (Figure 88).



(a) **(b)**

Figure 88: Open circuit voltage values of fabricated (a) Cz and (b) FZ cells. Lines are for visual aid

Reference cells have the highest V_{oc} values and without gettering samples are superior to gettering samples; which means gettering effect didn't provide any enhancement in V_{oc}. The only change, as demonstrated in Figure 88, was observed for FZ with passivation oxide samples but not significant.

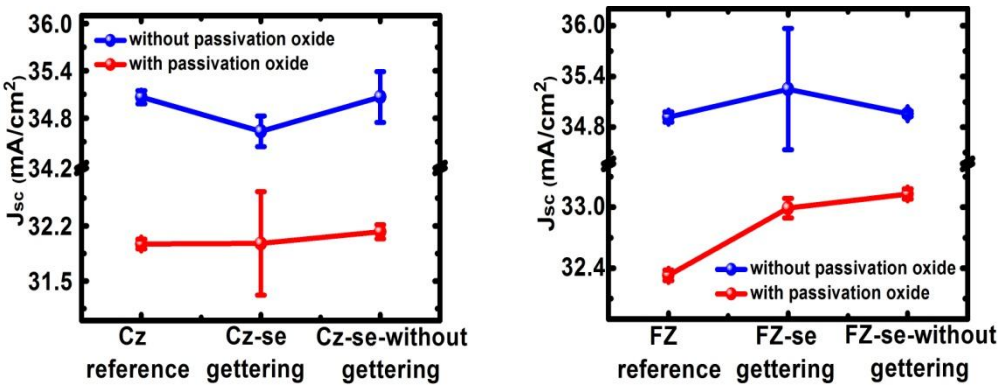
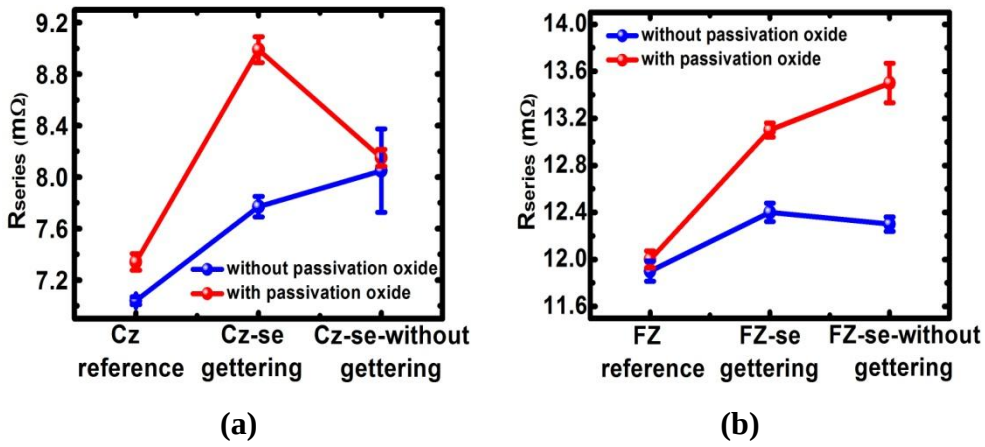


Figure 89: Short circuit current density values of fabricated (a) Cz and (b) FZ cells. Lines are for visual aid

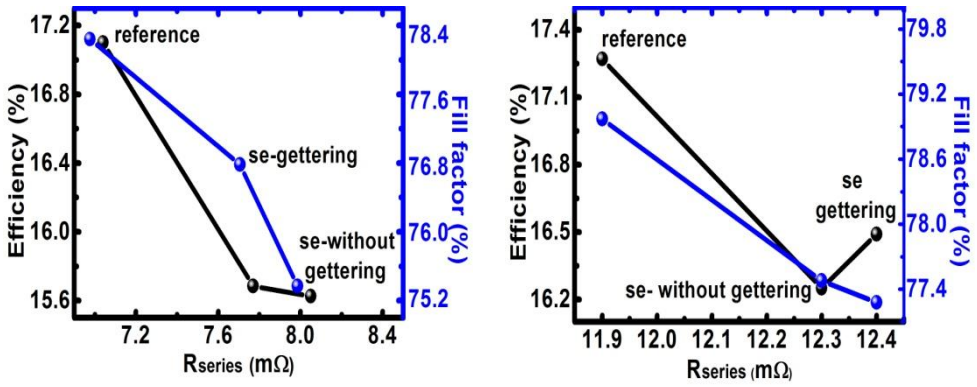
When J_{sc} values are taken into consideration, selective emitter cells overcome reference cells; which is an expected result and was also observed in the previous fabrication runs. Selective emitter effect is more distinguishable for FZ cells, which could be related to higher bulk material quality (Figure 89). Moreover, it could be deduced that gettering doesn't significantly affect J_{sc} values. J_{sc} of without oxide passivation cells approximately 3-4 mA/cm^2 greater than those of with oxide passivation cells which means oxide passivation layer is still thicker than required which could also be confirmed by their higher series resistance values as shown in Figure 90. Moreover, selective emitter cells of both Cz and FZ samples still suffer from high series resistance problem which stands as one possible reason of their lower efficiency values than the corresponding reference cells.



(a) **(b)**

Figure 90: Series resistance values of fabricated (a) Cz and (b) FZ cells. Lines are for visual aid

Although series resistance of selective emitter cells is not as much as they used to be in the first (Figure 57) and second run (Figure 73(b)), it is still high enough to significantly reduce cell performance. Even an increase of 0.7mΩ (Figure 90(a)) in series resistance results in a decrease of 1.5% in efficiency and of 1.6% in FF (Figure 91(a)).



(a) **(b)**

Figure 91: Series resistance-fill factor-efficiency relationship of fabricated (a) Cz and (b) FZ cells. Lines are for visual aid

In order to estimate pseudo efficiency and pseudo FF values of the fabricated solar cells, Suns-V_{oc} measurements were carried out.

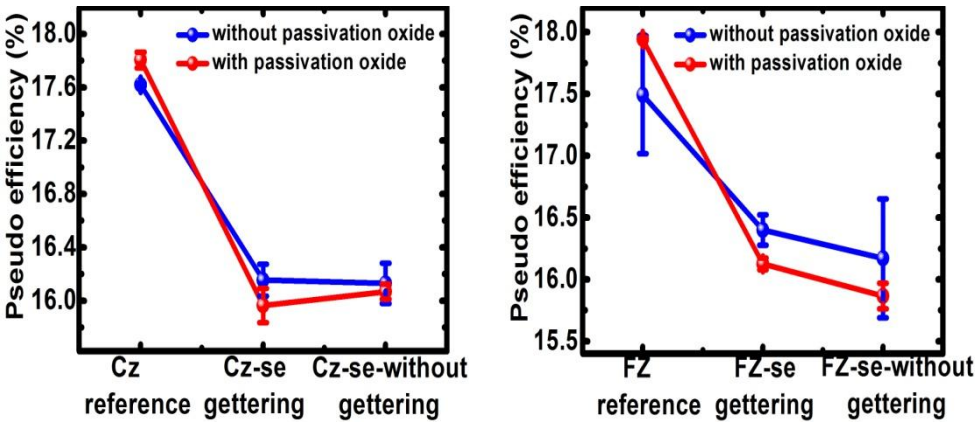


Figure 92: Pseudo efficiency values of fabricated (a) Cz and (b) FZ Cells. Lines are for visual aid

As demonstrated in Figure 92, even series resistance effect is eliminated; performance of selective emitter cells is still not better than reference cells in terms of efficiency, which means it is not only the series resistance that prevents selective emitter cells from better performance. However, it is clear that eliminating series resistance problem will make reference cells with oxide passivation to outperform reference cells without oxide passivation as expected. Thus, when passivation effect could be provided by a thinner oxide layer, expected performance improvement would become possible. Although eliminated series resistance effect enhances performance of selective emitter cells with oxide passivation, their efficiency values still lie slightly below those of without oxide passivation cells.

Pseudo fill factors of the fabricated cells are greater than their real values as expected since FF is a series resistance dependent cell parameter and both Cz and FZ cells show a similar behavior (Figure 93).

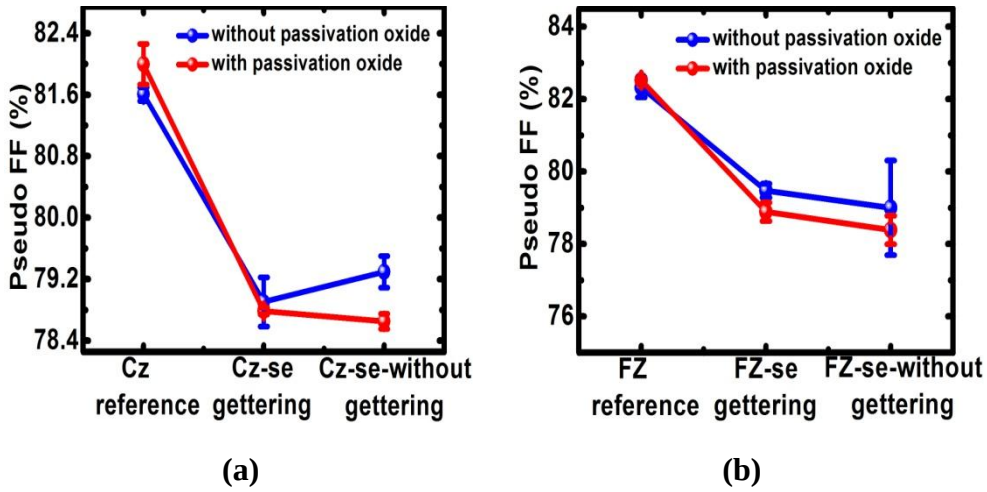


Figure 93: Pseudo fill factor values of fabricated (a) Cz and (b) FZ cells. Lines are for visual aid

V_{oc} values are close to those measured by solar simulator which implies that V_{oc} doesn't strongly depend on series resistance. Reference cells have significantly higher V_{oc} than selective emitter cells for both Cz and FZ wafers as plotted in Figure 94.

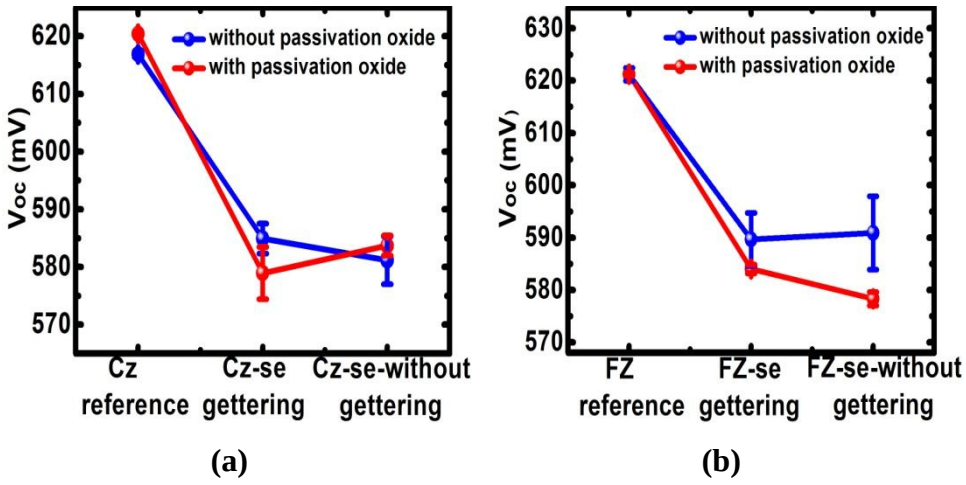
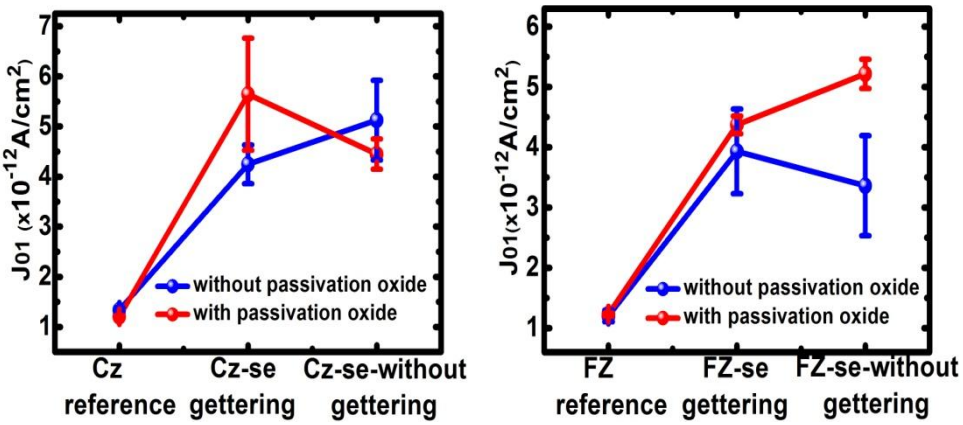


Figure 94: Measured Voc values of fabricated (a) Cz and (b) FZ cells. Lines are for visual aid

Such a decrease in V_{oc} under negligible series resistance assumption indicates possible recombination throughout the cell or junction related losses that would increase reverse saturation current components reducing V_{oc} of the fabricated cells. As plotted in Figure 95, selective emitter cells of both Cz and FZ wafers have higher J_{01} values compared to reference ones.



(a) **(b)**

Figure 95: Measured J_{01} values of fabricated (a) Cz and (b) FZ cells. Lines are for visual aid

Order of J_{01} is around 10^{-12} and 10^{-11} A/cm^2 for both reference and selective emitter cells of Cz and FZ wafers, respectively, which lies within an acceptable range. Thus, emitter and bulk recombination related component of reverse saturation current could be regarded as normal.

On the other hand, J_{02} is on the orders of 10^{-8} and 10^{-7} A/cm^2 for reference and selective emitter cells, respectively (Figure 96). It is known that J_{02} values that are greater than 10^{-10} A/cm^2 [48] is a sign of possible junction related problems which were also faced with in the previous fabrication runs.

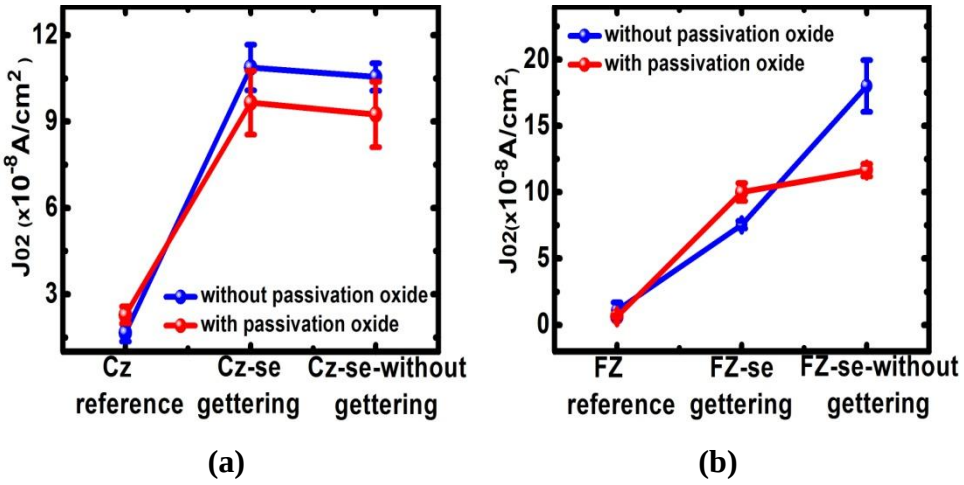


Figure 96: Measured J_{02} values of fabricated (a) Cz and (b) FZ cells. Lines are for visual aid

Although J_{02} value was reduced from the orders of 10^{-2} A/cm^2 (Figure 82) to 10^{-8} A/cm^2 with the help of proper process parameters, it is still higher than desired values for a decent cell performance.

After Suns-V_{oc}, EQE was the next measurement to be carried out to complete electrical characterization of the cells. As demonstrated in Figure 97, EQE of the selective emitter cells is better than the reference cells in short wavelength regime. E.Q.E is defined as; $\left[\frac{\#\ electrons}{\#\ incident\ photons}\right]$, Spectral Flux is; $\left[\frac{\#\ incident\ photons}{m^2 \times second \times nm}\right]$, q is unit charge in Coulombs, λ is wavelength in nm. Multiplying all these quantities with each other will give an estimate of short circuit current density in A/m^2. Since the spectral flux is almost constant for the measurements carried out with the same light source placed at a constant distance to all samples, area under E.Q.E. curve would be proportional to J_{sc}.

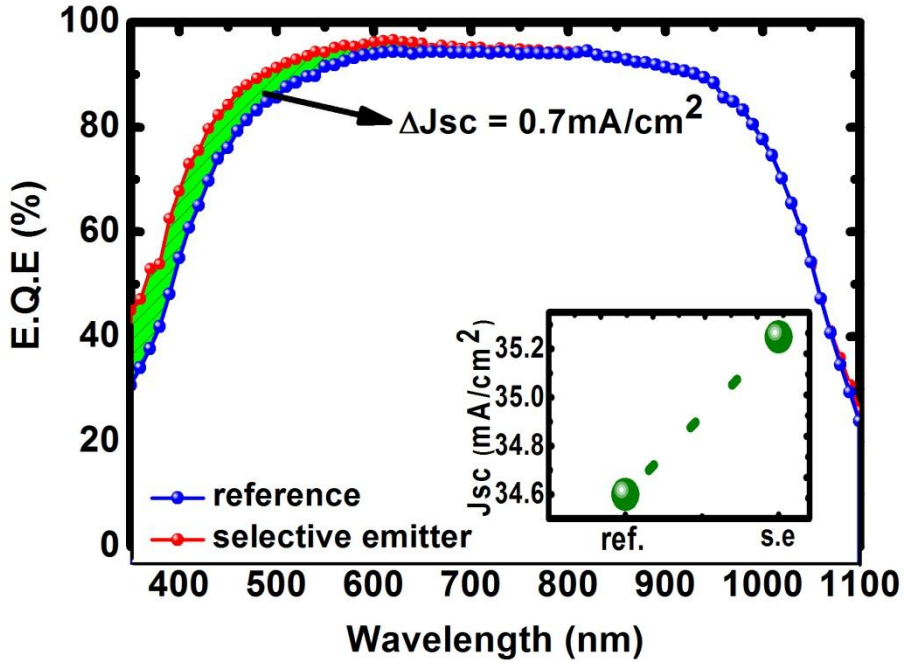


Figure 97: EQE comparison of reference and selective emitter solar cells with corresponding short circuit current density enhancement

As plotted in Figure 97, area between E.Q.E. curves of selective emitter and reference cell is corresponding to J_{sc} difference between them. Calculated J_{sc} difference was around 0.7mA/cm^2 whereas measured values was 34.6 and 35.25 mA/cm^2 for reference and selective emitter cell respectively. J_{sc} difference between measured values was 0.65 mA/cm^2, which is almost equal to the estimated value. The same procedure was applied for oxide passivated samples and it was observed that calculated J_{sc} difference was compatible with the value obtained from measurement. Although J_{sc} values of the oxide passivated samples were lower compared to those of without oxide samples, the difference between selective emitter and reference cells is greater. As shown in inset of Figure 98, J_{sc} of reference and selective emitter cell is 32.1 and 33.4 mA/cm^2 respectively with a difference of 1.2 mA/cm^2 , which is the same as the value estimated from E.Q.E results (Figure 98).

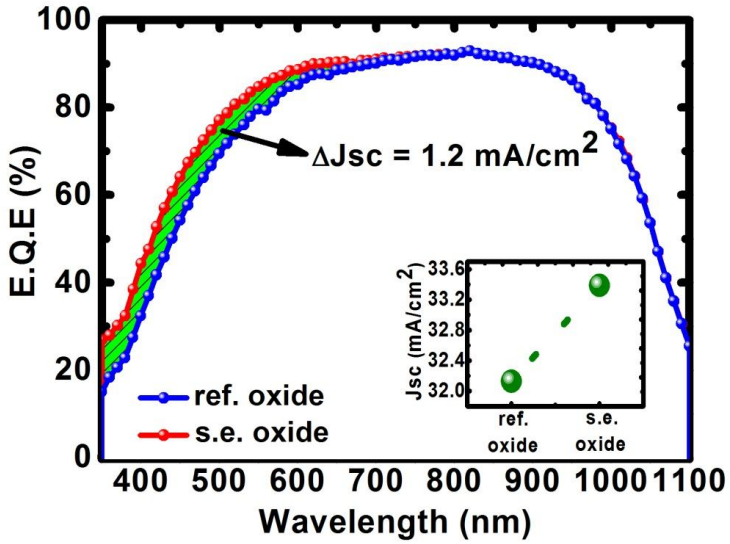


Figure 98: EQE comparison of oxide passivated reference and selective emitter solar cells with corresponding short circuit current density enhancement

Thus, despite series resistance problems, fabricated selective emitter cells have improved blue response. Also, enhancement observed in blue response of the oxide passivated cells which could be due to superior surface passivation provided by the additional oxide layer or due to optical enhancements resulting from different refractive index values of the oxide/nitride medium than the nitride layer. In order to understand the reason, reflection measurements and Internal Quantum Efficiency calculations (I.Q.E.) without reflection related losses, were carried out.

As plotted in Figure 99, textured bare Si surface has a reflectance of 12-14%, growth of oxide layer reduces the reflectance down to 9-10% whereas PECVD deposited nitride layer results in almost zero reflectance between 500 and 650 nm, which reaches at most 2-3% at around 900-950 nm. Application of oxide/nitride stack structure as anti-reflection coating results in almost zero reflectance between 650-900 nm, whereas reflectance between 500 and 650 nm is increased compared to that of the nitride deposited surface. Despite extended zero reflectance range, oxide/nitride stack structure increases surface reflectance in short wavelengths which would affect E.Q.E. adversely.

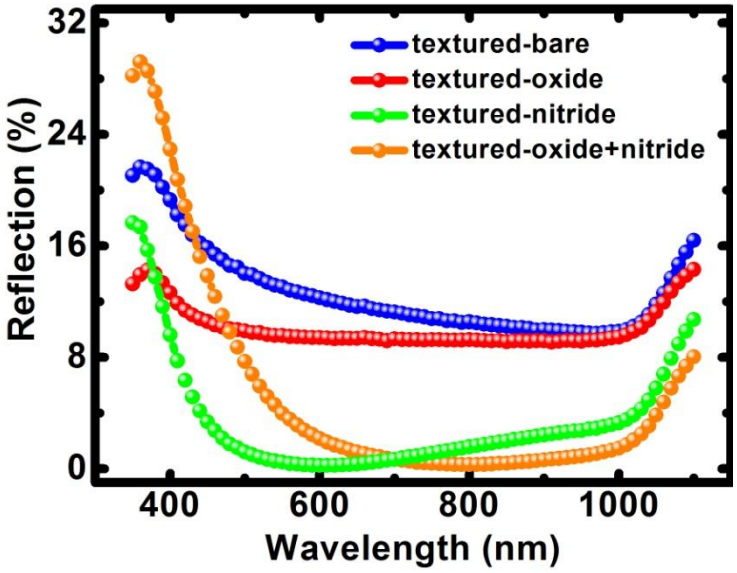


Figure 99:Reflection spectra of bare , oxide, nitride and oxide/nitride stack existing textured silicon surfaces

Considering greater improvement in blue response of oxide passivated selective emitter cells and increased reflection in corresponding region of spectrum simultaneously, it can deduced that observed improvement is due to better surface passivation provided by oxide/nitride structure.

When IQE and EQE of a reference cell is plotted on the same graph (Figure 100) it is observed that EQE lies below IQE at wavelengths shorter than 500 nm and longer than 700 nm since surface reflectance increases along these regions of the spectrum. IQE and EQE curves almost exactly coincide with each other as reflectance is very close to zero between 500 and 700 nm.

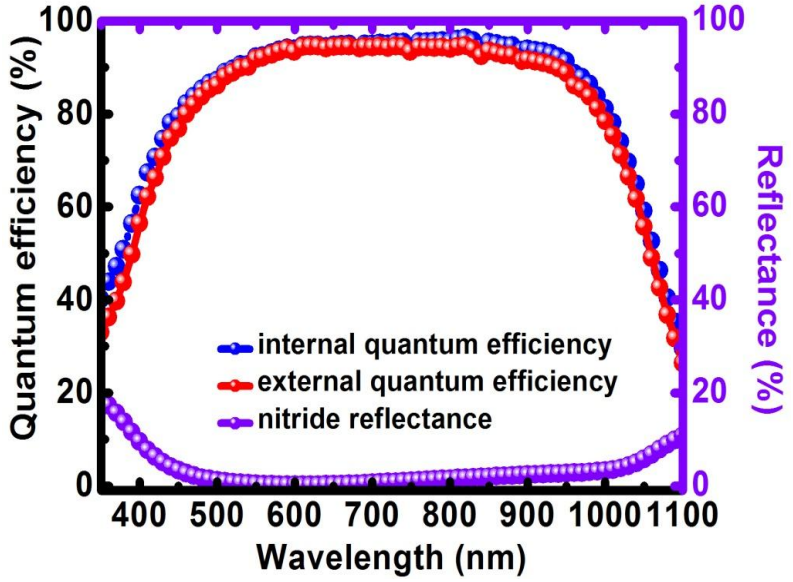


Figure 100: Internal and external quantum efficiency and corresponding reflectance spectrum of a reference cell

For the case of oxide passivated samples; IQE and EQE curves coincide with each other starting from 750 nm (Figure 101) till 1100 nm**.**

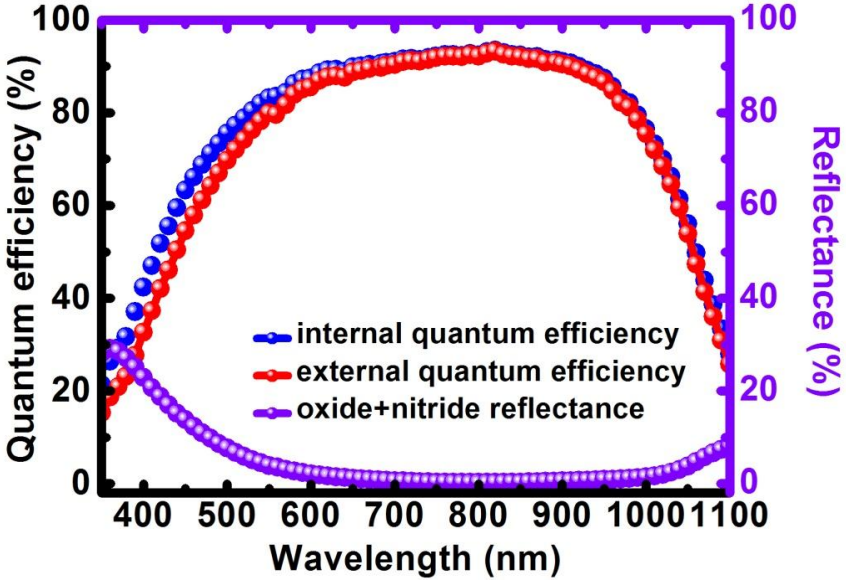


Figure 101: Internal and external quantum efficiency and corresponding reflectance spectrum of an oxide passivated reference cell

Since reflectance of oxide/nitride stack increases below 600 nm, deviation of EQE curve from IQE starts at the same wavelength. Hence, it is proven that despite inferior optical properties, oxide/nitride stack structure is capable of providing superior surface passivation which enhances short circuit current density of the fabricated cell.

5.2. SURFACE PASSIVATION STUDIES

First passivation study was carried out on solar grade, 180 μm thick, 0.1-1 ohm.cm, n-type textured wafers. Prior to nitride deposition, dilute HF dipping was applied for all samples to remove natural oxide from the surface. Then, different process gas ratios of SiH_4/NH_3, were applied to deposit silicon nitride films of different compositions. All deposition processes were carried out at 380^{o}C and 1Torr in the same PECVD chamber for equal deposition durations.

Table 1: SiH_4 & NH_3 flow rates of applied recipes on solar wafers and corresponding film thicknesses with refractive indices at 632nm

Recipe #	SiH_4(sccm)	NH_3(sccm)	thickness(nm)	n (at 632nm)
reference	x	x	x	3.87
1	200	450	105	1.927
2	200	350	101	1.939
3	200	250	101	1.941
4	200	200	108	1.938
5	200	150	111	1.929
6	150	450	102	1.905
7	250	150	124	1.937
8	300	150	95	1.976
9	350	150	60	1.987

Corresponding lifetime values were measured by SINTON lifetime tester whereas ellipsometric measurements were carried out to obtain corresponding film thicknesses and refractive indices whose results were tabulated in Table 1. Recipe #1 was the standard recipe that had been used in GUNAM Laboratories so far.

Nitride film deposited with standard nitride recipe has a refractive index of 1.927 at 632 nm. Increasing SiH_4 flow rate which corresponds to [3Si]>[4N] regime of the graph shown in Figure, resulted in higher refractive indices. On the other hand, increasing NH_3 flow rate generated lower refractive index films. Considering reaction equation of nitride deposition, stoichiometric nitride requires $[SiH_4]/[NH_3]$ ratio be 0.75 above which films became Si-rich whereas below that ratio obtained nitride film would be N-rich. Also, it could be deduced from Figure 102, Si-rich nitride layers provided better lifetime values till a certain value of refractive index was reached. When refractive index of the film was greater than 1.937, measured lifetime values started to decrease again. Moreover, $[SiH_4]/[NH_3]$= 350/150 and $[SiH_4]/[NH_3]$= 150/450 could be named as the limiting flow rates of our system, since film uniformity started to deteriorate at these flow rates.

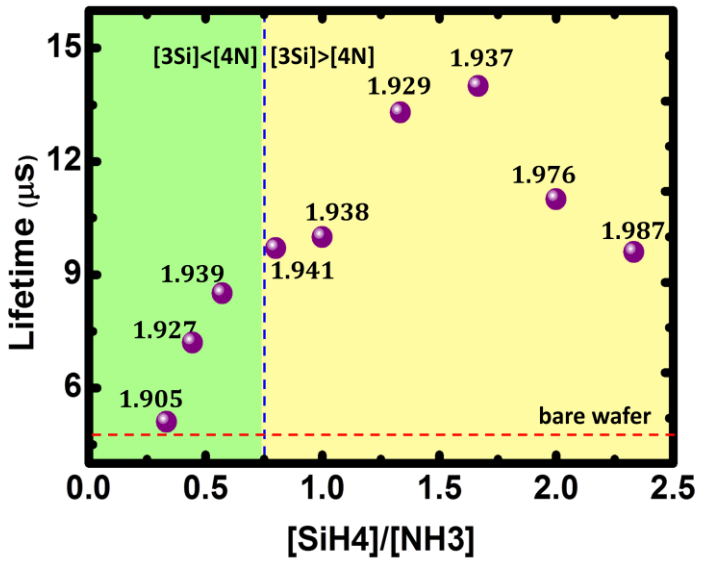


Figure 102: Effect of process gas flow ratios on lifetime

After studying effect of process gas ratios on passivation properties of the films deposited at constant temperature and pressure, standard nitride layers at various chamber pressures were deposited onto a new set of wafers. For this, $[SiH_4]/[NH_3]$= 200/450 was applied for chamber pressures of 900, 1000, 1200 and 1500 mTorr. For each pressure value, deposition time and chamber temperature were kept constant at 7.5 minutes and 380^oC, respectively.

Table 2: Applied chamber pressures for standard nitride recipe and corresponding film thicknesses with refractive indices at 632 nm

Pressure (mTorr)	thickness(nm)	n (at 632nm)	$\tau_{effective}$(μs)
900	107	1.90	9.5
1000	109	1.91	15
1200	114	1.96	11
1500	119	1.93	8

Considering the above results tabulated in Table 1 and Table 2, it could be deduced that, solar grade wafers had low bulk lifetimes. Low bulk lifetime reduces measured effective lifetime so even if applied nitride recipes decrease surface recombination velocity, these low bulk lifetime values would prevent us from detecting this enhancement. Thus, solar grade wafers were determined to be replaced with electronic grade wafers for surface passivation studies. At this step, test grade, single side polished (SSP), 525 μm thick, 10-20 ohm.cm, n-type wafers which were cut into small pieces of 2x2cm^2 were determined to be used. Before being processed, wafers were exposed to a 6 H_2O: 1 HCl: 1 HF solution for 15 minutes at room temperature. Then, as in the first study, effect of process gas flow was searched through. For this purpose, recipes whose gas flow rates are tabulated in Table 3 are utilized.

Table 3: SiH_4 & NH_3 flow rates of applied Recipes on SSP wafers and corresponding film thickness with refractive indices at 632 nm

Recipe #	SiH_4(sccm)	NH_3(sccm)	thickness(nm)	n (at 632nm)
reference	x	x	x	3.87
1	200	450	74	1.904
2	200	350	78	1.905
3	200	250	77	1.915
4	200	150	58	1.912
5	250	150	72	1.961
6	300	150	75	2.01

Except recipe #4, all recipes resulted in almost equal film thicknesses with increasing refractive indices as SiH_4 flow increases or NH_3 flow decreases. Reduced film thickness of recipe #4 could be related to the decreased total gas flow into the system.

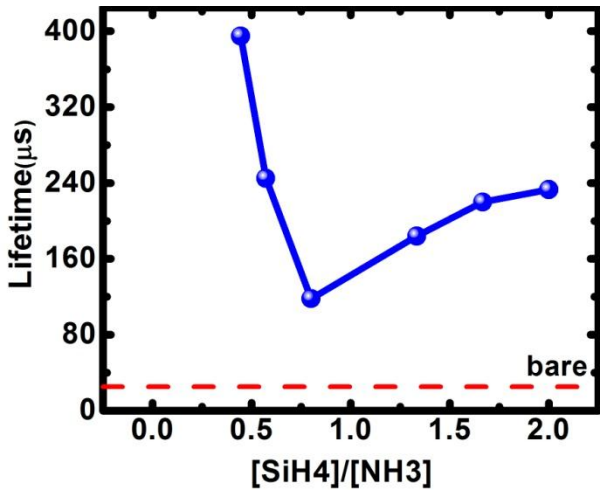


Figure 103: Effect of process gas flow ratios on lifetime of SSP wafers

As plotted in Figure 103, effective carrier lifetime takes its maximum value as 395μs for recipe #1 with SiH_4:200/NH_3:450 ratio. Decreasing NH_3 flow rate decreases effective lifetime until SiH_4/NH_3 ratio is 200/250 which makes Si/N ratio to be 0.8 close to that of stoichiometric silicon nitride which is equal to 0.75. After this point, increasing SiH_4 makes deposited nitride film silicon rich and enhances effective lifetime values. Then, the recipe resulting in the highest lifetime values was applied for a full n-type wafer to get rid of effect of damaged edges after cutting and the resulting effective lifetime value of it was 548 μs.

After obtaining remarkable results with SSP wafer it was determined to continue passivation studies with double side polished (DSP) wafers since SSP wafers are not physically symmetric. Front sides of SSP wafers are mirror polished whereas their rear sides are only lapped and etched as front side but not mirror polished. This makes the wafers unsymmetrical which makes it difficult to interpret lifetime measurements. Thus, DSP, electronic grade wafers were utilized for the latter passivation studies. In order to see the effect of resistance on lifetime, wafers of different resistance values of both n & p-type were processed. Resistance values of utilized wafers and their corresponding names given for clarity are tabulated in Table 4.

Table 4: Resistivity values of DSP wafers and corresponding names

N-TYPE WAFERS		**P-TYPE WAFERS**	
Resistance (Ωcm)	**Name**	**Resistance (Ωcm)**	**Name**
1-10	N1	1-10	P1
12-14	N2	5-10	P2
10-30	N3	10-20	P3
>3000	N4	>100	P4

As a starting point, different process gas flows were applied for silicon nitride deposition on small pieces of samples of 3-4 cm^2. Prior to deposition a short dilute HF dipping was applied to remove natural oxide layer from wafer surface.

Standard nitride recipe was utilized for the first run at 380°C and under 1000 mTorr chamber pressure. Average thickness of the samples was measured by ellipsometer as 93 nm with a refractive index of 1.88 at 632 nm.

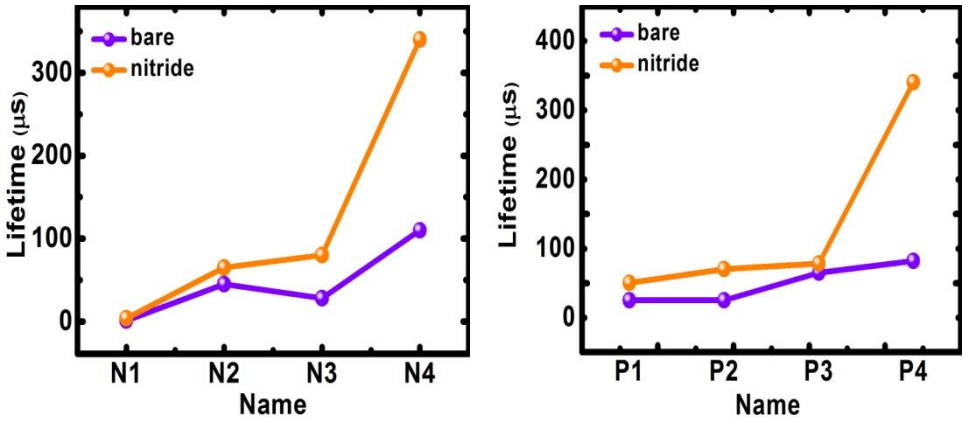


Figure 104: Effect of standard nitride deposition on effective lifetime of (a) n-type, (b) p-type DSP wafers. Lines are for visual aid

As shown in Figure 104, increasing base resistivity increases bulk lifetime of both n & p-type samples. Base resistivity depends on the doping level of the bulk material so that decreasing dopant concentration increases base resistivity, reduces Auger recombination and thus increases carrier bulk lifetime. Hence, bulk lifetime of high resistivity samples would be assumed to be high enough so that $1/\tau_{bulk}$ term in *Eq.46* could be neglected which means that measured effective lifetime values would be approximated to the remaining $1/\tau_{surface}$ term of the same equation.

After observing the effect of standard nitride recipe on effective lifetime, silicon nitride layer deposition onto a new set of samples was carried out with changing gas flow rates at constant process temperature. Based upon the previous passivation studies, it is known that silicon rich nitride layers provide better surface passivation compared to nitrogen rich ones. Thus, for this set of wafers, gas flows were adjusted in a way that SiH_4 flow rate will be greater than it is in the standard recipe.

SiH_4:200/NH_3:1400 ratio kept as reference recipe whereas SiH_4:500/NH_3:1100 ratio was the most silicon containing recipe for the total gas flow of 1600 sccm. SiH_4 flow rate cannot be set above 500 sccm due to safety interlocks of the system. For this, while keeping SiH_4 flow at its maximum value, NH_3 flow was set to its minimum possible value which was 100 sccm. Then, corresponding refractive indices, film thickness and lifetime values were measured via ellipsometer and lifetime tester respectively. Average thickness of the deposited nitride films was around 90 nm.

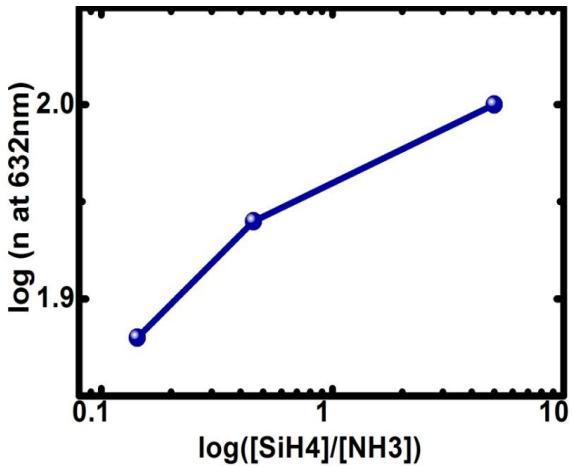


Figure 105: Effect of process gas flow ratio on refractive index at 632 nm. Lines are for visual aid

As plotted in Figure 105, increasing silicon content increased refractive index of the deposited film as expected. Refractive index of the standard nitride films was around 1.87 and takes its maximum value for SiH_4: 500/NH_3:100 as 2.01 at 632 nm.

Although lifetime values of the samples increase as the base resistivity of the material increases as a general trend, flow rate dependence of n and p-type samples slightly differ from each other. Considering Figure 106 (a), for relatively higher doping levels; silicon rich nitride provides better surface passivation than standard nitride does, whereas low doping levels, standard and Si-rich nitride layers result in similar lifetime values.

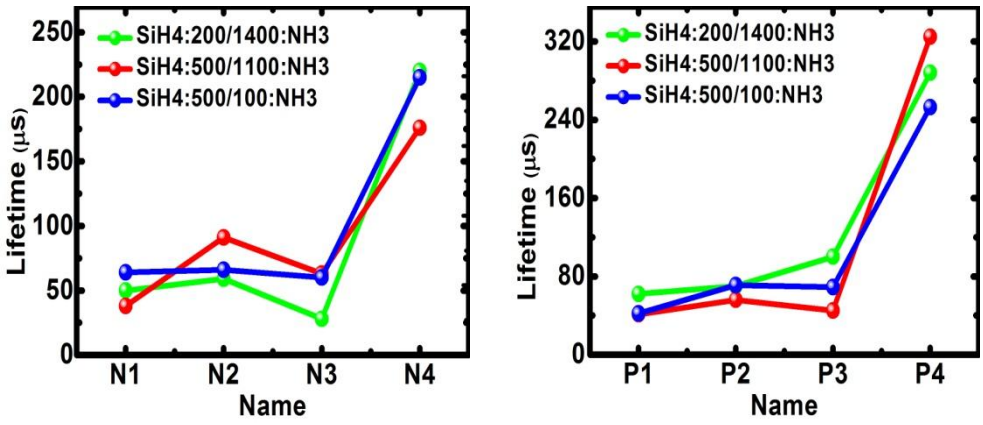


Figure 106: Effect of process gas flow ratio on lifetime of (a) n-type, (b) p-type DSP samples. Lines are for visual aid

On the other hand, for p-type samples, Si-rich nitride layers provided inferior passivation compared to standard nitride does especially for high doping levels (Figure 106 (b)). Moreover, for both n and p-type samples silicon rich nitride layers couldn't provide passivation as good as expected. At this point, it was argued that the number of damaged edges due to cutting really affected the lifetime of the sample. As the number of cut edges increases, corresponding lifetime decreases. In order to be sure of this argument, one full wafer, one fourth of a full wafer with two cut edges and one rectangular piece with four cut edges of the same resistivity were coated with nitride layer simultaneously. For this study only high resistance wafers were determined to be used due to their higher bulk lifetimes.

As shown in Figure 107, samples with four cut edges have 288 and 200 μs of lifetime for p and n-type respectively which increases to 373 and 340 μs for quarter samples and takes maximum values of 1950 and 1439 μs. As a result of this observation, previously applied nitride recipes were used on full wafers.

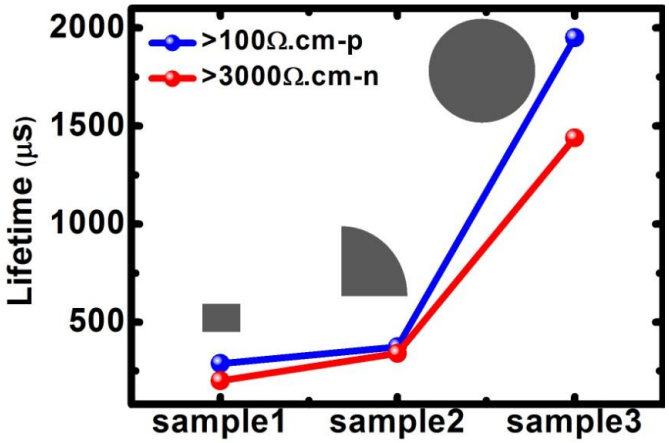


Figure 107: Effect of sample shape on lifetime. Lines are for visual aid

Considering Figure 108 it could be deduced that, both bare and nitride deposited samples' lifetime values of full wafers are greater than those of small pieces. Si-rich nitride layer with the ratio of SiH_4: 500 / 1100: NH_3, provides superior surface passivation compared to standard nitride layer for both n and p-type samples which is compatible with the literature.

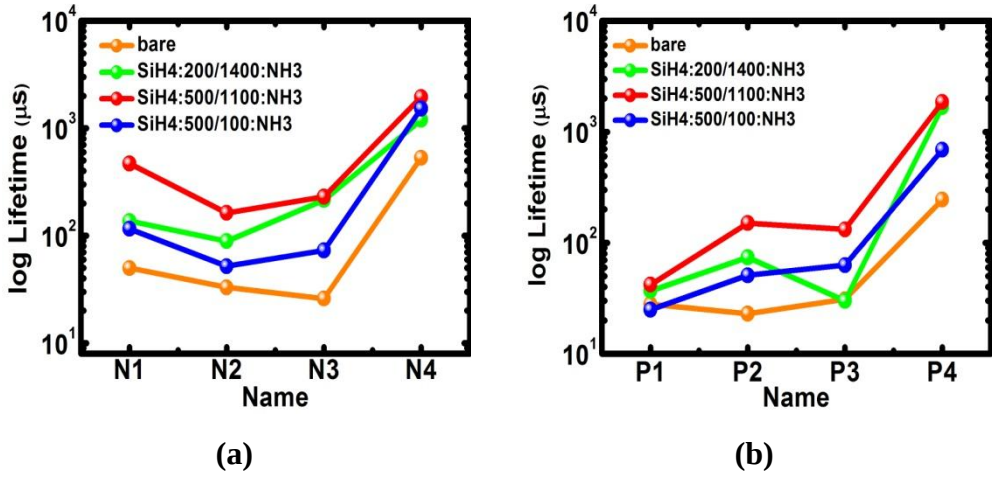


Figure 108: Effect of process gas flow ratio on lifetime of full (a) n-type, (b) p-type DSP wafers. Lines are for visual aid

On the other hand, SiH_4: 500 / 100: NH_3 recipe didn't work out properly since total gas flow rate is decreased from 1600 to 600 sccm which would significantly affect film uniformity. Moreover, for all recipes and almost samples, increasing bare resistivity increases measured effective lifetime as expected. Deposited film thicknesses were around 90-100 nm for all samples with changing refractive indices of 1.88, 1.92 and 2.1 as SiH_4 to NH_3 ratio increases. Taking this result into consideration, SiH_4: 500 / 1100: NH_3 was determined to be replaced with the standard recipe that had been used in cell fabrication so far.

After optimizing nitride recipe, a proper oxide passivation was aimed to be developed for further improvement of lifetime. For this purpose, both dry oxidation and wet oxidation samples were prepared at different temperatures for different oxidation durations.

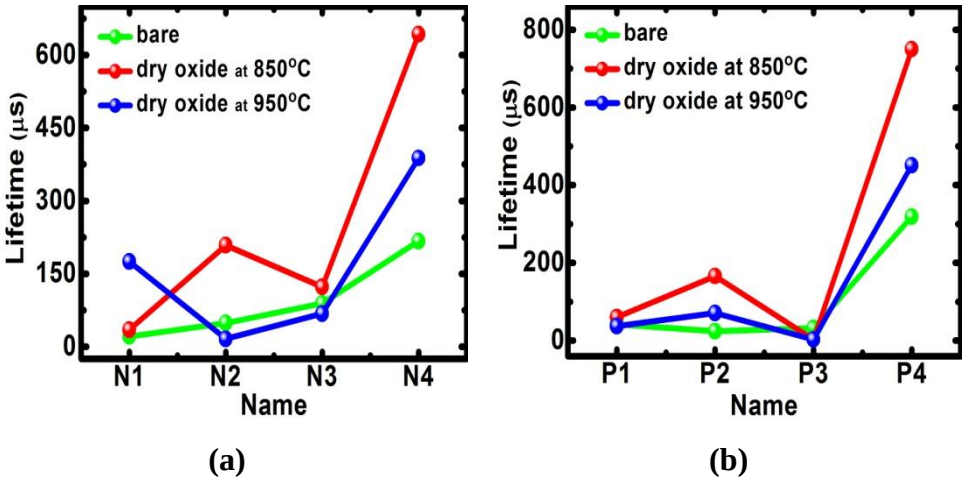


Figure 109: Effect of oxide passivation via dry oxidation on lifetime of full (a) n-type, (b) p-type DSP wafers. Lines are for visual aid

As plotted in Figure 109, oxide layer grown at 850°C results in higher lifetime values compared to that is grown at 950°C as expected since high temperature processes are known to degrade bulk lifetime due to increased number of trap associated states. Base resistivity dependence of the oxide passivation is similar to that of nitride however maximum lifetime value is 750 µs for p-type and

643 μs for n-type high resistivity samples which is significantly small compared to nitride passivation lifetime values. Oxide layer thickness was 20-25 nm for both of the applied temperatures. After dry oxidation, pyrogenic oxidation was also applied for passivation layer growth since it requires relatively lower process temperatures. For this purpose, 25 nm oxide layer was grown onto full wafers at 850^{o}C whose resultant lifetime values are plotted in Figure 110.

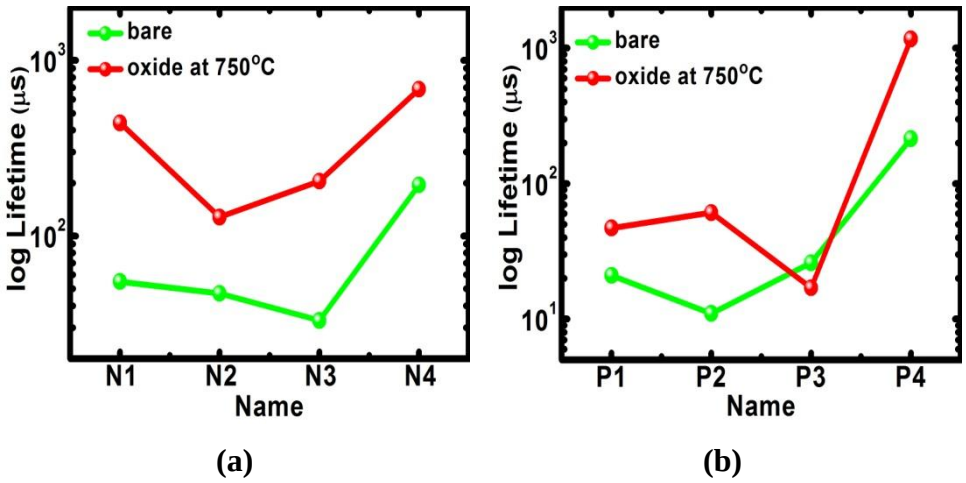


Figure 110: Effect of oxide passivation via pyrogenic oxidation on lifetime of full (a) n-type, (b) p-type DSP wafers. Lines are for visual aid

Considering Figure 109 and Figure 110 simultaneously, it is clear that pyrogenic oxidation provides higher lifetime values than dry oxidation does due to relatively lower process temperature.

After observing the effect different oxidation recipes on lifetime, performance of oxide/nitride stack structure was aimed to be observed. For this purpose, previously optimized silicon rich nitride layer was deposited onto all oxide passivated samples.

As demonstrated in Figure 111, samples passivated via pyrogenic oxide suffer from degraded passivation performance after nitride deposition. Despite lower process temperature which results in higher effective lifetime value, pyrogenic oxide layers are not as stable as dry oxide layers under thermal treatment.

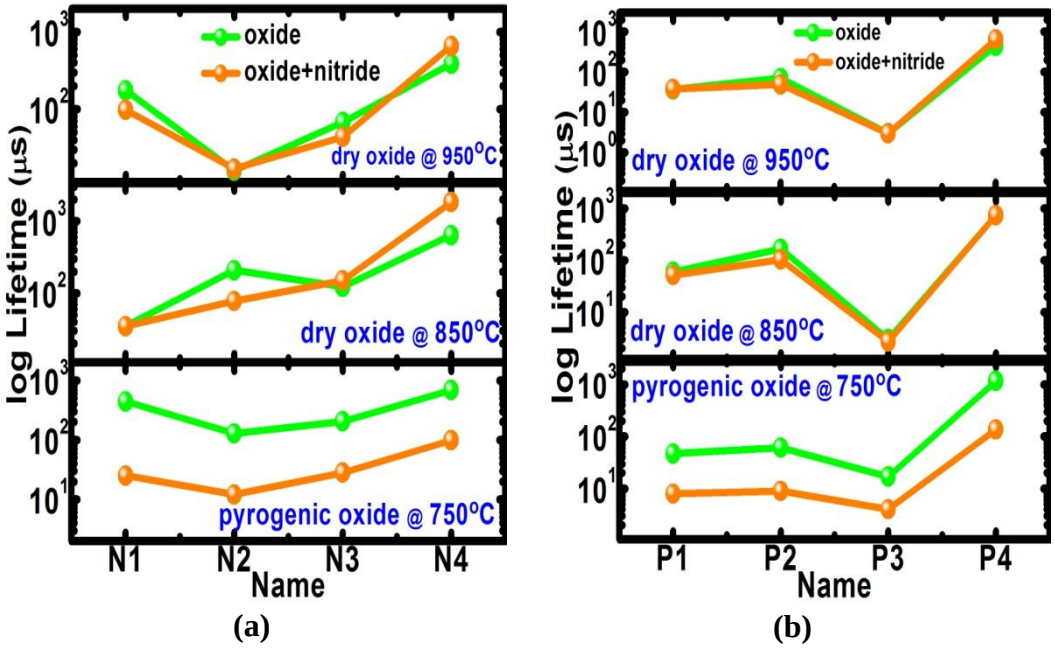


Figure 111: Effect of nitride deposition on oxide passivated full (a) n-type, (b) p-type DSP wafers. Lines are for visual aid

After first oxide passivation trial, a new set of samples were prepared only for high base resistivity wafers to eliminate the effect of Auger recombination on measured effective lifetime. For this >100 Ω.cm-p and >3000 Ω.cm-n type full wafers were exposed to dry oxidation at 950°C and pyrogenic oxidation at 850°C both for 10, 20, 40 and 80 min After oxidation and corresponding lifetime measurements, PECVD nitride deposition was applied for all oxidized samples.

As shown in Figure 112, all oxide and oxide/nitride provided lifetime values lie below those provided by predeposition HF dipping which is also known as a good way of temporary passivation. 40 min seems to be the optimum oxidation duration both dry and pyrogenic oxidation. Although deposition of nitride layer onto grown oxide decreases lifetime values, pyrogenic oxide provided passivation degrades more significantly compared to dry oxidation which could be related to lower quality of oxide layer grown via pyrogenic oxidation. Moreover, observed worsening of oxide provided passivation successive to nitride deposition could be related to the thickness of the applied nitride layer.

If the nitride thickness is kept constant 70-80 nm as utilized in standard cell fabrication, then the resulting surface will have a color of light blue instead of dark blue or violet which implies that the surface reflection increases

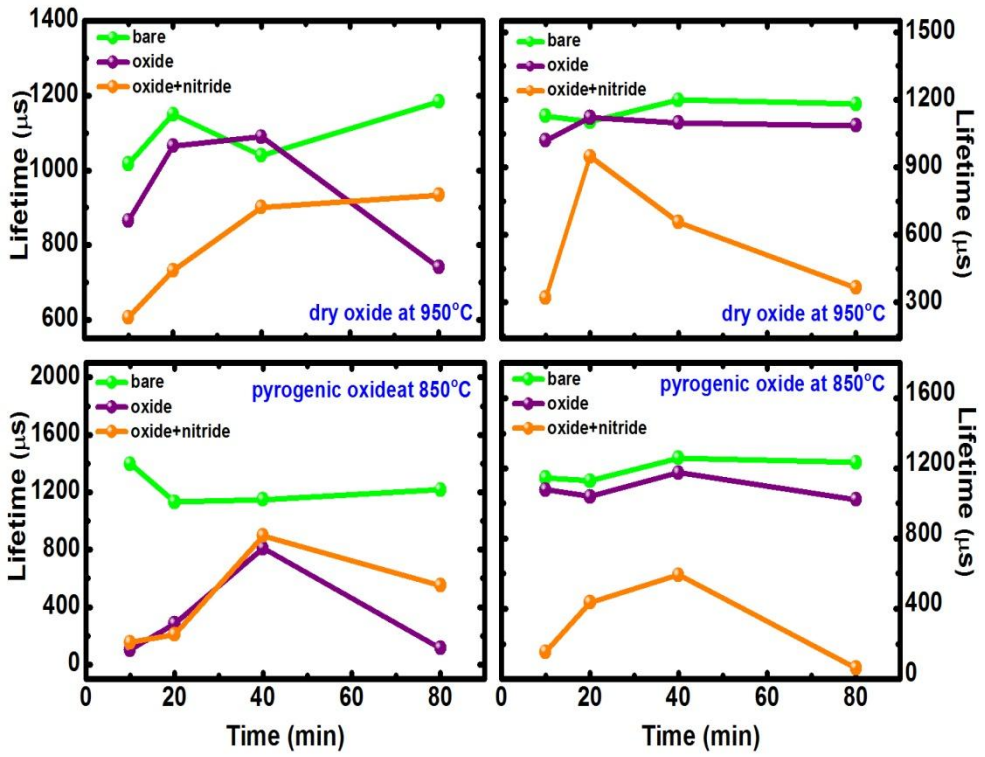


Figure 112: Performance of oxide / nitride stack structure. Lines are for visual aid

The same situation also generated problems in selective emitter cell fabrication with oxide passivation during second and the third run whose results were demonstrated in the previous section. Although, it hasn't been applied for passivation samples yet, reducing the deposited nitride thickness such that resulting surface will have a dark blue color was observed to improve cell performance. Thus, in order to benefit oxide/nitride stack structure deposited nitride thickness is required to be optimized.

CHAPTER 6

CONCLUSIONS

Utilization of alternative energy sources has become more crucial for the last decades due to increasing energy demand of the world. Application of solar cells providing direct conversion of solar energy into electricity has attracted greater interest due to relatively higher conversion efficiencies and cheaper fabrication methods compared to other alternative energy sources like wind, geothermal, biomass etc. Among other technologies, silicon wafer based solar cell technology, which is usually referred to as the first generation, is still dominating the market because of its high performance, reliability and well know production technologies.

In order to increase conversion efficiency of solar cells, different cell concepts like PERC, Back Contact, PERL and Selective Emitter have been developed and utilized by the industry in recent years. In this master thesis we studied a new selective emitter approach based on single step doping. Selective emitter concept takes the advantage of reduced emitter dopant concentration while keeping contact resistance low. Reduced emitter dopant concentration suppresses the minority carrier recombination at the front side of the cell, however, as the number of dopant atoms decreases, resistance of the emitter layer increases so that the contact resistance between the emitter and front fingers also increases. This trade-off between recombination velocity and contact resistance could be solved with the help of selective emitter design where emitter regions beneath the front fingers are highly doped to prevent from possible contact resistance problems while remaining regions would be lowly doped to reduce surface recombination velocity. Although selective emitter cells could be fabricated via several methods like lithography, spin on doping or laser doping, minimum number of additional steps was aimed for the method

studied throughout this thesis. For this purpose, a single step doping fabrication sequence was designed where phosphorous atoms diffuse through a diffusion mask layer some regions of which is ablated with the help of laser beam. These laser ablated regions so-called grooves would then be exposed to higher concentration of phosphorous atoms during doping compared to the rest of the surface.

Subsequently, highly doped grooves would be aligned to lie under front side fingers at metallization step. Although both silicon nitride and silicon dioxide layers could be used as mask layers, silicon dioxide was preferred for our studies since it is known to be more stable at high process temperatures.

As the starting point of the fabrication sequence, mask oxide thickness and emitter sheet resistance values had to be optimized. For this purpose, different thicknesses of 20, 30 and 50 nm oxide layers were utilized for two different doping recipes one of which was named as “high doping” resulting in a sheet resistance of 35Ω/□ whereas the other one was named as “standard doping” and resulted in 50Ω/□ sheet resistance on bare silicon without doping mask layer. In order to find optimum parameters; different laser powers, pass numbers and scan speeds were applied for different KOH dipping durations varying as 10, 20 and 35min. in 10% solution for each sample. Then, corresponding sheet resistance and dektak measurements were carried out. Considering obtained results, power value was chosen to be 30-32A and scan speed was determined to be 600mm/s due to less damage given to wafer surface with 20min. KOH dipping to fabricate the first set of selective emitter cells. When the performance of fabricated selective emitter and reference cells is compared, it was observed that selective emitter cells showed significantly inferior performance in terms of efficiency (eff.), fill factor (FF) and open circuit voltage (V_{oc}). The only enhancement we observed was in short circuit current density (J_{sc}) by an amount of approximately 1.5mA/cm^2 which is the result of improved blue response confirmed by external quantum efficiency measurements. All selective emitter cells were observed to suffer from contact misalignment problem with the help of electroluminescence measurements which explains increased series resistance and inferior cell performance. Also, depletion region related reverse saturation current

density components of the selective emitter cells were observed to be 10 times greater than those of reference samples.

As the second fabrication run, previously utilized laser was replaced with a new marking laser of 1064nm. Using this laser, all optimizations regarding laser power, scan speed and scribe number had to be re-optimized before the cell fabrication. Different than the first run, doping recipe number was decreased to one because high doping recipe resulting in low sheet resistance over the regions beneath oxide regardless of its thickness. Moreover, an additional dilute HF dipping step was included into fabrication sequence prior to nitride deposition in order to remove possible natural oxide layer exiting between metal contacts and laser opened grooves. Also, half of the samples were oxidized at $850^{o}C$ to provide surface passivation effect. Again fabricated cells suffer from contact misalignment problem which was not as much as in the first run but was still present causing high series resistance thus reduced cell performance. Moreover, oxide passivated samples had higher series resistance values compared to samples without oxide passivation cells which implies that the thickness of the growth oxide layers was much higher than it had to be and front side finger couldn't penetrate through thick oxide layer and form a proper contact. However, oxide passivated cells had higher efficiency, fill factor, open circuit voltage and short circuit current density values than reference cells which means that despite its being thick, oxide layer could provide passivation especially on the laser damaged surface of the selective emitter cells. On the other hand, for without oxide passivation cells, reference cells showed better performance than selective emitter cells as in the case of first run. Compared to the first run, maximum efficiency increased from 15.7% to 16.2%, maximum fill factor increased from 75% to 78% whereas maximum open circuit voltage decreased from 620mV to 610mV and maximum short circuit current density decreased from 34.8 to 33,6mA/cm^2 to. The increase in efficiency could be related to the enhanced fill factor despite reduced Voc and J_{sc} values. Increasing FF signs better metallization whereas decreased V_o and J_{sc} values are the results of significantly increased J_{02} value from the orders of 10^{-8}A/cm^2 to 10^{-2} A/cm^2.

As the final run for selective emitter cell fabrication, oxide thickness was set to 20 nm, laser power was kept constant, HF dipping step included in the previous run was removed from the fabrication sequence. For this set of samples, Fz wafers were also used to observe the effect of wafer quality on cell performance.

Cell performance of reference cells overcome that of selective emitter cells which could again be related to higher series resistance and J_{02} values.

To sum up, although fabricated selective emitter cells could result in improved blue response and short circuit current density values, there are other factors preventing them from reaching higher efficiency values than reference cells. First of all, J_{02} values are still significantly greater than they have to be which reduces both J_{sc} and V_{oc} of the corresponding cells. Second, although significantly reduced compared to the first fabrication run, contact misalignment still stands as a problem. Finally and most importantly, screen printing mask was designed for standard homogenous emitters. For proper carrier collection on selective emitters, fingers should be placed closer to eliminate the effect of high series resistance between successive fingers and should be narrower to decrease shading effects. Thus, by solving high J_{02} problem and using a properly designed mask for printing, one could reach better selective emitter cells developed in this thesis. Moreover, passivation oxide layer thickness should be reduced to get rid of series resistance problem.

As the second part of thesis studies, surface passivation properties of nitride and oxide layers were studied. Previously used standard silicon nitride recipe was replaced with a new silicon rich recipe with the flow ratio of SiH_4:500/NH_3:1100. For oxide layers, it was observed that although providing relatively higher lifetime values, passivation made by pyrogenic oxidation significantly deteriorates under thermal treatment. Thus, dry oxidation was determined to be more suitable to form a passivation oxide. Oxide layers grown at 850^{o}C resulted in higher lifetime values than those grown at 950^{o}C which confirmed that high temperature processes degraded bulk lifetime. Then, for oxide/nitride stack structure, a proper nitride thickness was to be determined since the thickness 75-80 nm which is the standard nitride thickness was observed to be thick for stack structure via reflection

measurements. Then, optimized stack structure was utilized for selective emitter cells and expected improvement in J_{sc} could be obtained.

In conclusion, selective emitter is a promising cell design to reach higher efficiency values. A more suitable laser with a shorter wavelength could be utilized to reduce the laser induced damage on the Si wafer. Also, front side metallization mask should be designed for selective emitter cells. In future, new selective emitter cells will be fabricated in accordance with these requirements.

BIBLIOGRAPHY

[1] "ISE Photovoltaics Report," 2014.

[2] Nelson Jenny, *The Physics of Solar Cells*. 2003.

[3] M. A. Green, *SOLAR CELLS (Operating Principles, Technology and System Applications)*. 1982.

[4] "Market Share of Installed PV Capacity by 2012." [Online]. Available: http://www.firstgreen.co/2013/08/graph-of-the-day-solar-pv-global-capacity-share-of-top-10-countries2012/ . [Accessed: 20-Jan-2014].

[5] "Solar Cells." [Online]. Available: http://alliedscientificpro.com/shop/solar-cells/ . [Accessed: 30-Jan-2014].

[6] "Nanosolar CIGS Solar Cells." [Online]. Available: http://www.solarfeeds.com/rip-nanosolar/. [Accessed: 01-Feb-2014].

[7] "Highest Efficiency Organic Solar Cell Created," *Sci. Dly.*, 2007.

[8] Y. Chiba, A. Islam, Y. Watanabe, R. Komiya, N. Koide, and L. Han, "Dye-Sensitized Solar Cells with Conversion Efficiency of 11.1%," *Jpn. J. Appl. Phys.*, vol. 45, no. No. 25, pp. L638–L640, Jun. 2006.

[9] C. B. Honsberg, "Paths to ultra-high efficiency (>50% efficient) photovoltaic devices," in *20th European Photovoltaic Solar Energy Conference,*, 2005.

[10] "Solar Spectrum." [Online]. Available: http://pveducation.org/pvcdrom/properties-of-sunlight/atmospheric-effects . [Accessed: 05-Feb-2014].

[11] B. Hoffmann, V. Sivakov, S. W. Schmitt, M. Y. Bashouti, M. Latzel, J. Dluhoš, and J. Jiruse, "Wet – Chemically Etched Silicon Nanowire Solar Cells : Fabrication and Advanced Characterization," 2012.

[12] T. O. M. Tiedje, E. L. I. Yablonovitch, G. D. Cody, and B. G. Brooks, "Limiting Efficiency of Silicon," no. 5, pp. 711–716, 1984.

[13] "Quantum Efficiency." [Online]. Available: http://pveducation.org/pvcdrom/solar-cell-operation/quantum-efficiency. [Accessed: 09-Feb-2014].

[14] S. . Sze, *VLSI Technology*, Second Edi. McGraw-Hill Book Company, 1988, pp. 277–299.

[15] "SiemensMethod." [Online]. Available: http://www.solarnenergy.com/eng/info/show.php?c_id=4977&pg=3&s_sort=&sub_cat=&s_type=&s_word=. [Accessed: 22-Feb-2014].

[16] C. Solar and C. C. Limits, "Solar cell conversion-efficiency limits 5.1," pp. 1–12.

[17] S. M. Iftiquar, Y. Lee, M. Ju, N. Balaji, and S. K. Dhungel, "Fabrication of Crystalline Silicon Solar Cell with Emitter Diffusion , SiNx Surface Passivation and Screen Printing of Electrode," 2005.

[18] R. . Ghoshtagore, "Phosphorous Diffusion in SiO2 Films," *Thin Solid Films*, vol. 25, no. 2, pp. 501–513, 1975.

[19] S. . Grove, *Physics and Technology of Semiconductors Devices*. John Wiley and Sons, 1967.

[20] K. Sakamoto, K. Nishi, F. Ichikawa, and S. Ushio, "Segregation and Transport Coefficients of Impurities at the Si/SiO2 Interface," *J. Appl. Phys.*, vol. 61, no. 15, 1987.

[21] B. Streetman, "Solid State Electronic Devices," 1995.

[22] M. Z. Rahman, "Status of Selective Emitters for p-Type c-Si Solar Cells," vol. 2012, no. June, pp. 129–134, 2012.

[23] M. Sciences, "Crystalline silicon solar cells with selective emitter and the self-doping contact."

[24] M. Z. Rahman, "Status of Selective Emitters for p-Type c-Si Solar Cells," *Opt. Photonics J.*, vol. 02, no. 02, pp. 129–134, 2012.

[25] M. Gauthier, M. Grau, O. Nichiporuk, F. Madon, V. Mong-The Yen, N. L. Quang, A. Zerga, and A. Slaoui, "INDUSTRIAL APPROACHES OF SELECTIVE EMITTER ON MULTICRYSTALLINE SILICON SOLAR CELLS," 2006.

[26] D. Rudolph, K. Peter, A. Meijer, O. Doll, and I. Köhler, "ETCH BACK SELECTIVE EMITTER PROCESS WITH SINGLE POCl3 DIFFUSION," pp. 2–5.

[27] G. Poulain, D. Blanc, a. Focsa, B. Bazer-Bachi, M. Gauthier, B. Semmache, Y. Pellegrin, N. Le Quang, and M. Lemiti, "Laser Process for Selective Emitter Silicon Solar Cells," *Int. J. Photoenergy*, vol. 2012, pp. 1–5, 2012.

[28] S. Liou, “Efficiency Improvement by Selective Emitter Technology through Silicon Ink Printing.”

[29] A. Rohatgi, D. L. Meier, B. McPherson, Y.-W. Ok, A. D. Upadhyaya, J.-H. Lai, and F. Zimbardi, “High-Throughput Ion-Implantation for Low-Cost High-Efficiency Silicon Solar Cells,” *Energy Procedia*, vol. 15, no. 2011, pp. 10–19, Jan. 2012.

[30] J. Wu, Y. Liu, X. Wang, and L. Zhang, “Application of ion Implantation Emitter in PERC Solar Cells,” vol. 4, no. 1, pp. 52–57, 2014.

[31] D. M. Chen, Z. C. Liang, L. Zhuang, Y. H. Lin, and H. Shen, “A novel method to achieve selective emitter for silicon solar cell using low cost pattern-able a-Si thin films as the semi-transparent phosphorus diffusion barrier,” *Appl. Energy*, vol. 92, pp. 315–321, Apr. 2012.

[32] A. Szekers and P. Danesh, “Structures formed by thermal oxidation of amorphous and crystalline silicon,” *Semicond. Sci. Technol.*, vol. 11, no. 1225, p. 30, 1996.

[33] J. H. Bultman, A. R. Burgers, J. Hoornstra, R. Kinderman, M. Koppes, W. J. Soppe, and A. W. Weeber, “IDEAL SINGLE DIFFUSION STEP SELECTIVE EMITTERS : A COMPARISON BETWEEN THEORY AND PRACTICE Barrier surface Silicon,” 2001.

[34] P. F. Mart, “Diffusion through Oxide Barriers for Solar Cell Applications.”

[35] R. Pierret, *Advanced Semiconductor Fundamentals*, Second Edi. Prentice Hall.

[36] E. Doktorgrades, “Rapid Thermal Processing of Silicon Solar Cells - Passivation and Diffusion,” 2003.

[37] M. M. Makhlouf and H. V. Guthy, “The Aluminum-Silicon Eutectic Reaction: Mechanisms and Crystallography,” *J. Light Met.*, 2002.

[38] R. W. Olesinski, A. B. Gokhale, and G. J. Abbaschian, “The Ag-Si(Silver-Silicon) System,” *Bull. Alloy Phase Diagrams*, vol. 10, no. 6, p. 635,636, 1989.

[39] W. Soppe, H. Rieffe, and A. Weeber, “Bulk and Surface Passivation of Silicon Solar Cells Accomplished by Silicon Nitride Deposited on Industrial Scale by Microwave PECVD,” *Prog. Photovoltaics Res. Appl.*, vol. 13, pp. 551–569, 2005.

[40] B. Hoex, J. J. H. Gielis, M. C. M. van de Sanden, and W. M. M. Kessels, “On the c-Si Surface Passivation Mechanism by Negative-Charge Dielectric Al2O3,” *J. Appl. Phys.*, 2008.

[41] M. Kondo, S. De Wolf, and H. Fujiwara, “Understanding of Passivation Mechanism in Heterojunction c-Si Solar Cells,” *Mater. Res. Soc.*, 2008.

[42] M. Ju, J. Y. Lee, K. Lee, C. Han, Y. Jo, and J. Yi, “Effectiveness of Iodine Termination for Ultrahigh Efficiency Solar Cells as a Means of Chemical Surface Passivation,” *Jpn. J. Appl. Phys.*, vol. 51, 2012.

[43] H. Li, S. R. Wenham, and Z. Shi, “High efficiency PERL cells on CZ P-type crystalline silicon using a thermally stable a-Si:H/SiNx rear surface passivation stack,” *Sol. Energy Mater. Sol. Cells*, vol. 117, pp. 41–47, Oct. 2013.

[44] J.-F. Lelièvre, E. Fourmond, a. Kaminski, O. Palais, D. Ballutaud, and M. Lemiti, “Study of the composition of hydrogenated silicon nitride SiNx:H for efficient surface and bulk passivation of silicon,” *Sol. Energy Mater. Sol. Cells*, vol. 93, no. 8, pp. 1281–1289, Aug. 2009.

[45] “Technical Data for Elements in Periodic Table.” [Online]. Available: http://periodictable.com/Elements/014/data.html. [Accessed: 26-Jun-2014].

[46] R. A. Sinton, A. Cuevas, and M. Stuckings, “Quasi-steady-state photoconductance, a new method for solar cell material device and characterization,” in *Proc. 25th Photovoltaic Specialists Conference*, 1996, pp. 457–460.

[47] S. Luan and W. Neudeck, “An Experimental Study of the Source/Drain Parasitic Resistance Effects in Amorphous Silicon Thin Film Transistors,” *J. Appl. Phys.*, vol. 72, no. 766, 1992.

[48] O. Breitenstein, J. Bauer, P. P. Altermatt, and K. Ramspeck, “Influence of Defects on Solar Cell Characteristics,” *Solid State Phenom.*, vol. 156–158, pp. 1–10, 2010.

[49] “NREL Best Researc Cell Efficiencies.” [Online]. Available: http://www.nrel.gov/ncpv/images/efficiency_chart.jpg. [Accessed: 20-Jan-2014].

[50] Fraunhofer, “Organic Solar Cells: Electricity From A Thin Film,” 2008. [Online]. Available: http://www.sciencedaily.com/releases/2008/02/080206154631.htm. [Accessed: 02-Feb-2014].

[51] S. Ver-Bruggen, “Building and automotive signify main opportunities for DSSCs,” *plastic electronics magazine*, 2010.