A NEW APPROACH FOR DISTRIBUTED AMPLIFIER DESIGN

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ABSTRACT

A NEW APPROACH FOR DISTRIBUTED AMPLIFIER DESIGN

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In this thesis work, a new distributed amplifier topology is discussed and applied to three different cases. The topology is based on dividing the frequency spectrum into channels and amplifying afterwards. The channelized and amplified signals are then combined at the output for broadband amplification. This topology is used in the design of a three channel 0.1-1 GHz amplifier with a gain of 14.5±0.6 dB. The design is fabricated, and then the measured and simulated results are compared. A second 0.1-1 GHz amplifier with 21±1 dB is designed in simulation environment with five channels. This five channel amplifier is fabricated and measured results are compared with the simulated ones. A 1-6 GHz three channel amplifier is also designed with a gain of 10.5±0.5 dB. Application of the proposed topology to three different designs shows promising results for future amplifier designs.

Keywords: Broadband Amplifier, Distributed Amplifier, Channelization, Tubular Filter, Manifold Multiplexer

ÖZ

DAĞITILMIŞ YÜKSELTEÇ TASARIMINDA YENİ BİR YAKLAŞIM

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Bu tez çalışmasında, yeni bir dağıtılmış yükselteç topolojisi geliştirilmiş ve üç farklı duruma uygulanmıştır. Topoloji frekans tayfının kanallara bölünmesi ve daha sonra da yükseltilmesi üzerine kuruludur. Kanallara ayrılmış ve yükseltilmiş sinyaller geniş bantlı yükseltme elde edebilmek için çıkışta birleştirilmektedir. Bu topoloji üç kanallı 0.1-1 GHz arasında 14.5±0.6 dB kazanç sağlayabilen bir yükseltecin tasarımında kullanılmıştır. Bu tasarım üretilmiş ve ölçüm sonuçları benzetim sonuçları ile karşılaştırılmıştır. Aynı topoloji 0.1-1 GHz arasında 21±1 dB kazanç sağlayabilen beş kanallı bir tasarım için de kullanılmıştır. Beş kanallı bu yükselteç üretilmiş ve ölçüm sonuçları benzetim sonuçları ile karşılaştırılmıştır. 1-6 GHz arasında çalışan üçüncü bir yükselteç 10.5±0.5 dB kazanç sağlayacak şekilde tasarlanmıştır. Bu topolojinin üç farklı tasarıma uygulanması sonucunda umut vaat eden sonuçlar elde edilmiştir.

Anahtar Kelimeler: Geniş Bantlı Yükselteç, Dağıtılmış Yükselteç, Kanallara Ayırma, Tubular Filtre, Manifold Çoğullayıcı

to my family

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CHAPTER 1

INTRODUCTION

1.1 RF and Microwave Amplifiers

An amplifier is employed to amplify input signals which may be received or generated inside a circuit. A signal is amplified before it is applied to the antenna or a received signal from an antenna is amplified for processing in a communication system.

As wireless technology proceeds, expectations from an amplifier increase with it. Today's wireless communication systems require wideband, efficient and high gain amplifiers. Depending on the application, requirements on an amplifier change. Obtaining high-gain and wideband systems has been one of the main areas of focus in wireless technologies. In RF and microwave amplifiers, transistors are employed as the main component; however physical constraints of transistors put an upper limit to the gain and bandwidth of a practical amplifier. This fact is observed as gain-bandwidth product which stays constant for an amplifier design.

Researchers have come up with some topologies to overcome the limitation on bandwidth. Compensating matching topology, feedback amplifier, balanced amplifier and distributed amplifier (DA) are some important topologies for broadband amplification.

The first three topologies listed earlier do not meet the high gain-bandwidth requirement. Distributed amplifier scheme has caught much attention since first broadband amplifiers; since problem of gain-bandwidth product is solved to an

extent. In theory, distributed amplifier has an infinite bandwidth. However due to physical limitations, bandwidth is limited.

1.2 Distributed Amplifiers

Distributed amplifier has been one of the main focus areas in microwave amplifiers area. W.S. Percival [1] showed that an amplifier's bandwidth is primarily set by the capacitance and transconductance of the valve used. Afterwards, Ginzton [2] explained the theory behind distributed amplifier which proves to be very useful in obtaining wide bandwidth amplifiers. By absorbing the capacitance in an artificial transmission line, distributed amplifier becomes a broadband amplifier. Since one of the main constraints on broadband amplification is eliminated, bandwidth of the amplifier is limited only to the band of the artificial transmission line.

In early days of DA, tube technology was employed [1-3]. In 60's and 70's FETs became the major component in distributed amplification. Researchers developed broadband amplifiers employing transistors [4,5]. With the introduction of MMIC technology, distributed amplifiers are designed covering a very wide range of frequencies [6,7].

Distributed amplifier is an ingenious way for broadband amplification; however it has some drawbacks that should be considered. Most important drawbacks are the limited gain as stages are cascaded and poor efficiency when distributed topology is employed in power amplifiers. A new topology is employed in this thesis that shows promising results to overcome these problems of DA.

1.3 Proposed Topology for Broadband Amplification

In section 1.1, some of the broadband amplification techniques are mentioned. Among these methods, only distributed amplifier comes up with a solution to overcome the gain-bandwidth product limitation. In this thesis work, a new topology is employed for enhancing the band of operation for an amplifier. The proposed topology achieves broadband operation by dividing the frequency spectrum of operation.

In DA, all of the amplifying elements work at the same frequency range, i.e. frequency selectivity is not observed. In the proposed scheme, frequency spectrum is divided into contiguous channels. These channels are amplified separately and combined at the output of the amplifier. Dividing an incoming signal and processing afterwards seems a relatively easy job. However combining the amplified signals may not be straightforward; since contiguous channels are of concern. This work contains designs of three separate amplifiers based on this topology.

First of all, a 3-channel 0.1-1 GHz amplifier, having a gain of 14.5±0.6 dB is designed. This amplifier is designed in the ADS simulation environment and fabricated on Hg-Tech FR4 substrate. After tuning manually, a broadband amplifier is achieved. Secondly, a 0.1-1 GHz amplifier is designed with five channels and in a different manner. The second amplifier is not manufactured, only the simulation results are given. This amplifier has a gain of 21±1 dB throughout the frequency band. Finally, a 1-6 GHz amplifier with three channels is designed. Again this amplifier is not fabricated, only the simulation results are provided. The simulated amplifier achieves a gain of 10.5±0.5 dB gain within the band of interest.

1.4 Outline of the Thesis

This thesis is organized as follows: Chapter 2 briefly discusses some of the broadband amplification techniques. Detailed formulation is only given for distributed amplifier topology which happens to be the basis for this thesis work.

In Chapter 3, proposed distributed amplifier topology is discussed in detail. First theory behind the topology is given and then simulation phases are described in detail. After simulation, fabrication and measurement processes are depicted. Results of the manufactured amplifier are given at the end of the chapter.

Chapter 4 contains the design of two amplifiers based on the proposed topology. First a 0.1-1 GHz amplifier is discussed on the simulation level. Then a 1-6 GHz amplifier is described in detail.

Finally conclusions about the design of the proposed topology are presented in chapter 5.

CHAPTER 2

BROADBAND AMPLIFIER THEORY

Aim of this Chapter is to give insight about broadband amplifier design topologies. As discussed in Chapter 1, broadband amplifiers have great importance in today's communications and electronic warfare systems; thus much effort has been spent on this topic. There are several ways to achieve broadband amplification.

Brief description for broadband amplifier topologies is given in this chapter. Emphasis is given on distributed amplification, since thesis work depends on distributed topology. It would be useful in comparing the proposed topology and distributed amplification.

2.1 Limitations on Broadband Amplification

In early days of amplifiers, tubes are used in order to amplify RF signals. Nowadays microwave amplification depends mainly on microwave transistors. Although transistor became the major element in amplifiers, it has limitations for broadband operation due to its inherent characteristics. These characteristics bring up frequency dependent behavior, some of which may be listed as [10]:

- Magnitude of S_{21} decreases with frequency at a rate of 6 dB/octave. Phase of S_{21} also changes with frequency.

- Both magnitude and phase of S_{12} changes with frequency. Together with the change of S_{21}, this variation can cause stability issues for broadband operation.
- S_{11} and S_{22} are also frequency dependent which makes impedance matching problematic.

In order to design a proper constant gain amplifier, the limitations mentioned above should be eliminated. Broadband amplification is merely a challenge to overcome these difficulties. This can be achieved by employing matching networks, feedback networks, balanced amplifier and distributed topology. These topologies are explained in the following sections.

2.2 Broadband Amplifier Topologies

In years researchers have developed several ways to achieve broadband amplification. However all of the topologies expanded bandwidth of operation in expense of either gain or design complexity. Some of the topologies are listed below:

- Compensating Matching Topology
- Feedback Amplifier
- Balanced Amplifier
- Distributed Amplifier (DA)

These topologies are discussed in the subsequent sections.

2.2.1 Compensating Matching Topology

Compensating matching topology is based on compensating the deviations of magnitude of S_{21} with frequency. Transistors are matched in order to get good input and output return loss values. Good input and output return loss values are necessary for a proper amplifier operation; however frequency dependant behavior of transistors can make traditional matching techniques useless in broadband amplifier design. This topology compensates the frequency behavior by mismatching the transistor in some part of the frequency band.

As mentioned previously, transistors have higher gain in lower frequencies. Thus for a flat gain response throughout a wide band, gain in lower frequencies should be decreased. In literature, compensating matching topology is also referred to as lossy matching technique [9]. An example is given for lossy matching network in Figure 2-1.

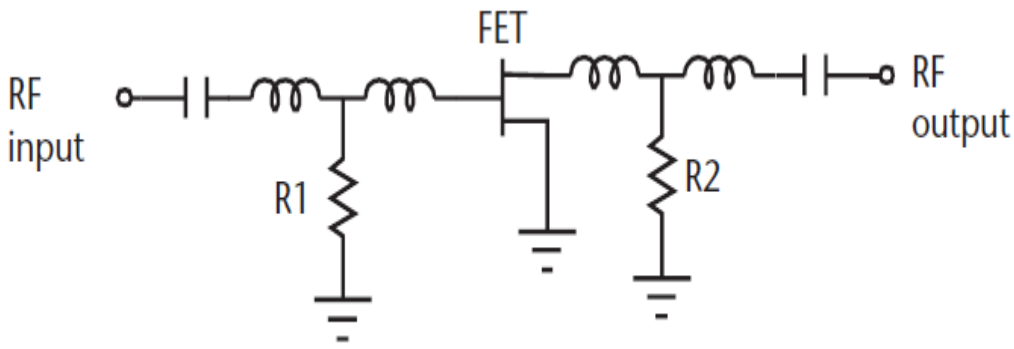


Figure 2-1 Lossy Matched Amplifier (given in [8])

This lossy matching technique uses two resistors at the input and output. For gain flatness these resistors attenuates the signal at low frequencies and introduces a lower attenuation at higher frequencies. This design also results in a good input and output return match. This amplifier has a broad band, however gain is reduced and efficiency is low as can be expected. Moreover noise figure is higher due to resistors used in the matching networks.

2.2.2 Feedback Amplifier

Feedback is used in several studies to extend the bandwidth of amplifiers [11-13]. Theory behind this extension is simple [14]. Block diagram for any feedback circuitry is given in Figure 2-2.

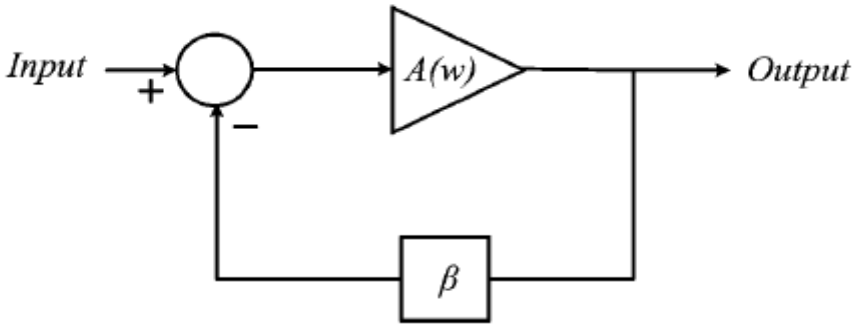


Figure 2-2 General diagram of a negative feedback amplifier (given in [14])

In this diagram amplifier gain without feedback is denoted by $A(w)$. Feedback constant is denoted by β. Then the circuit's transfer function can be expressed as:

$$A_{feedback}(w) = \frac{A(w)}{1+\beta A(w)} \ . \tag{2.1}$$

Assuming a single pole representation for the amplifier, its transfer function becomes

$$A(w) = \frac{A_0}{1+\frac{jw}{w_C}} . \tag{2.2}$$

Replacing $A(w)$ expression in equation (2.1) and simplifying further leads to the result

$$A_{feedback}(w) = \frac{\frac{A_0}{1+\beta A_0}}{1+\frac{jw}{w_C(1+\beta A_0)}} . \tag{2.3}$$

Looking at bandwidth w_C, an increase is observed at a rate of $(1+\beta A_0)$. On the other hand, gain expression at the nominator is reduced by the same factor. This leads to the conclusion that gain-bandwidth product does not change with feedback [14].

In microwave amplifiers feedback is located between gate and drain of the transistors. Feedback technique has some remarkable advantages [8]:

- Flat gain and unconditional stability is achieved over a wide band.

- Complexity is reduced compared to other topologies. Thus it leads to an easy and cost effective implementation
- Compared to distributed topology and lossy matched case, higher efficiencies can be obtained
- Lower distortion and sensitivity effect are observed on amplifier.

A general feedback amplifier circuitry is given in Figure 2-3. As can be seen from Figure 2-3, resistance R_{fb}, inductance L_{fb} and capacitance C_{fb} are feedback elements. Feedback inductance together with gate inductance L_g and drain inductance L_d can be used to extend the bandwidth. However it should be noted that L_{fb} acts a low-pass element and reduces feedback efficiency. Feedback capacitance C_{fb} is used as DC block. L1 and L2 are bias inductors. Bias inductors and DC block capacitor should be resonance free in the band of interest.

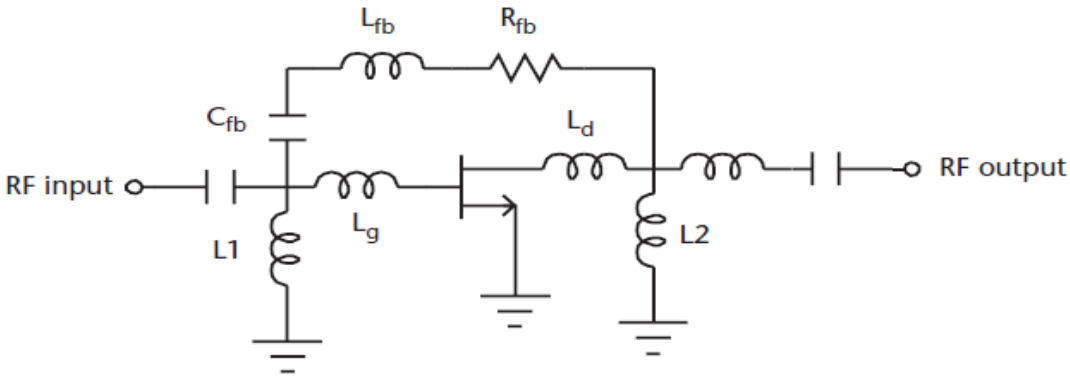


Figure 2-3 Generalized feedback schematic (given in [8])

2.2.3 Balanced Amplifier

As mentioned in compensating matching network section, a flat gain response can be obtained by mismatching the transistor for lower part of the frequency band. However for a proper amplifier operation, input and output match return losses should be as low as possible. A lower return loss is necessary when two stages are cascaded as is generally the case for a microwave amplifier. Balanced amplifier configuration overcomes this return loss problem.

Balanced amplifier employs two 90° hybrid couplers to cancel out input and output reflections from two identical amplifiers. The general circuitry is given in Figure 2-4.

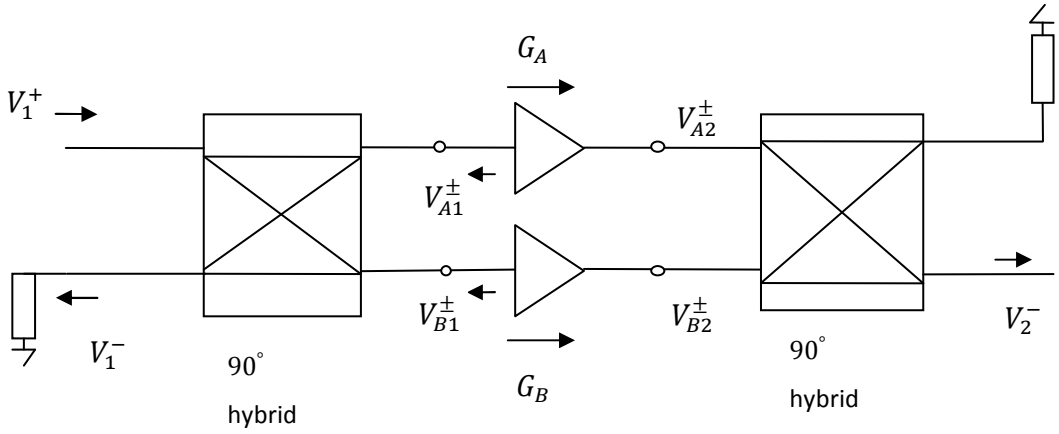


Figure 2-4 Balanced amplifier configuration (given in [15])

The coupler at the input divides the incoming signal into two signals with equal amplitude and 90° phase difference. These signals are amplified by identical amplifiers and then coupler at the output combines the amplified signals by again applying a 90° phase difference. Since identical amplifiers are used, reflections from these amplifiers should be of same magnitude but with 90° degree phase difference. Then couplers at the input and output combine these reflections with a 90° phase shift. The phase difference between reflections becomes 180° and they cancel out at the termination port [15].

Assuming ideal couplers, incident voltages can be represented as

$$V_{A1}^+ = \frac{1}{\sqrt{2}} V_1^+ \tag{2.5}$$

$$V_{B1}^+ = \frac{-j}{\sqrt{2}} V_1^+ \tag{2.6}$$

A gain of G_A and G_B are obtained from amplifiers A and B respectively. Output voltage can be written as

$$V_2^- = \frac{-j}{\sqrt{2}} V_{A2}^+ + \frac{1}{\sqrt{2}} V_{B2}^+ = \frac{-j}{\sqrt{2}} G_A V_{A1}^+ + \frac{1}{\sqrt{2}} G_B V_{B1}^+ = \frac{-j}{2} V_1^+ (G_A + G_B) \tag{2.7}$$

From the well known formula, S_{21} can be extracted as

$$S_{21} = \frac{V_2^-}{V_1^+} = \frac{-j}{2}(G_A + G_B) \tag{2.8}$$

The total reflected voltage can be written as

$$V_1^- = \frac{1}{\sqrt{2}}V_{A1}^- + \frac{-j}{\sqrt{2}}V_{B1}^- = \frac{1}{\sqrt{2}}\Gamma_A V_{A1}^+ + \frac{-j}{\sqrt{2}}\Gamma_B V_{B1}^+ = \frac{1}{2}V_1^+(\Gamma_A - \Gamma_B) \tag{2.9}$$

Using equation (2.9), S_{11} can be extracted as

$$S_{11} = \frac{V_1^-}{V_1^+} = \frac{1}{2}(\Gamma_A - \Gamma_B) \tag{2.10}$$

Identical amplifiers means G_A=G_B and Γ_A=Γ_B which leads S_{11}=0. These mathematical calculations clearly show a perfect theoretical match.

Balanced amplifier does not improve gain-bandwidth product of an amplifier. Moreover the circuit is more complex; since it uses two amplifying paths. Despite these disadvantages, balanced amplifier shows some remarkable advantages given in [15]:

- Very good input and output match which permits adjustments on amplifiers either for gain or noise Figure
- Good match at ports improves the amplifiers' stability
- An octave or more bandwidth can be achieved, primarily depending on the bandwidth of couplers.

2.2.4 Distributed Amplifier

Distributed amplifiers have been used in RF and microwave circuits for years. Since Ginzton [2] described the theory of distributed amplifiers in 1948, it has become one of the main focus areas of broadband amplification. As mentioned earlier, broadband amplification is limited with the gain-bandwidth product. Gain-bandwidth product is limited mainly by the characteristics of transistors (tubes). A transistor's gate and drain capacitance puts an upper limit to the gain-bandwidth

product that an amplifier can achieve. DA has the ability to overcome this problem by merging these capacitances in an artificial transmission line. This artificial line may either be of distributed nature or made of lumped elements. Since the input and output capacitances are absorbed in transmission lines, gain bandwidth product upper limit is defined with the bandwidth of these transmission lines only. Figure 2-5 (a) and (b) shows a generalized sketch for DAs. Input and output artificial transmission lines can be observed either with distributed elements or lumped elements.

With the advances in microwave technology, the importance of DAs is increased. In early days of distributed amplification, space allocated by a DA was very remarkable; however with recent advances, DAs are built in very small packages.

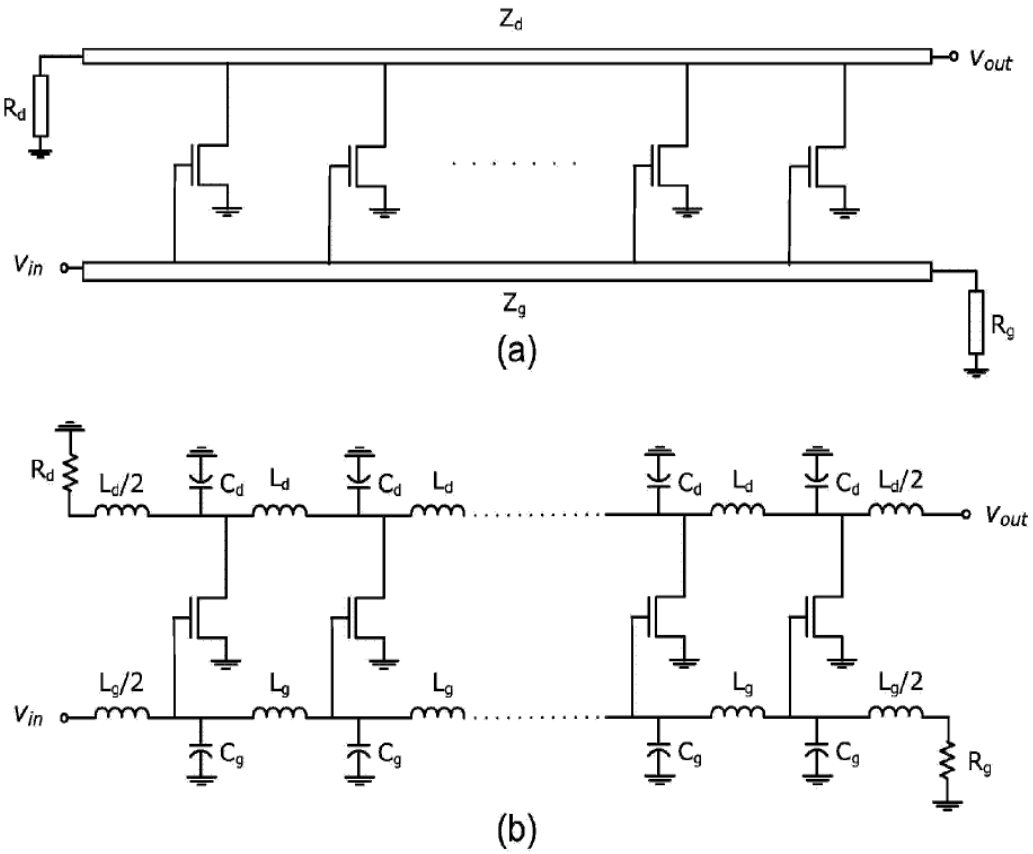


Figure 2-5 Distributed amplifier topology: (a) Distributed transmission line, (b) lumped transmission line (given in [14])

Figure 2-6 shows N identical FETs that are cascaded. Their gates are connected to a transmission line with characteristic impedance Z_g and spacing l_g. The drains of the transistors are connected to a transmission line with impedance Z_d and spacing between connections l_d. A signal applied to the input port of the DA propagates through the artificial gate line. During this propagation, power is coupled to the gate of each transistor and then these coupled signals are amplified through transistors. Amplified signals form a travelling wave at the output drain line. The propagation constants for the artificial gate and drain transmission lines are selected for additive phasing as well as the lines between the connections. Even though a Z_0 impedance transmission line is meant to be formed for gate and drain lines, there might be reflections which may disturb the travelling waves. Thus terminations are added to the other ends in order to absorb reflected waves.

Pozar explained the theory of operation for DA [15]. Pozar started the analysis by considering a unilateral FET equivalent where C_{gd} (capacitance between gate and drain) is zero. Using this model circuit in Figure 2-5 can be decomposed into two parts for gate and drain lines as shown in Figures 2-6 and 2-7.

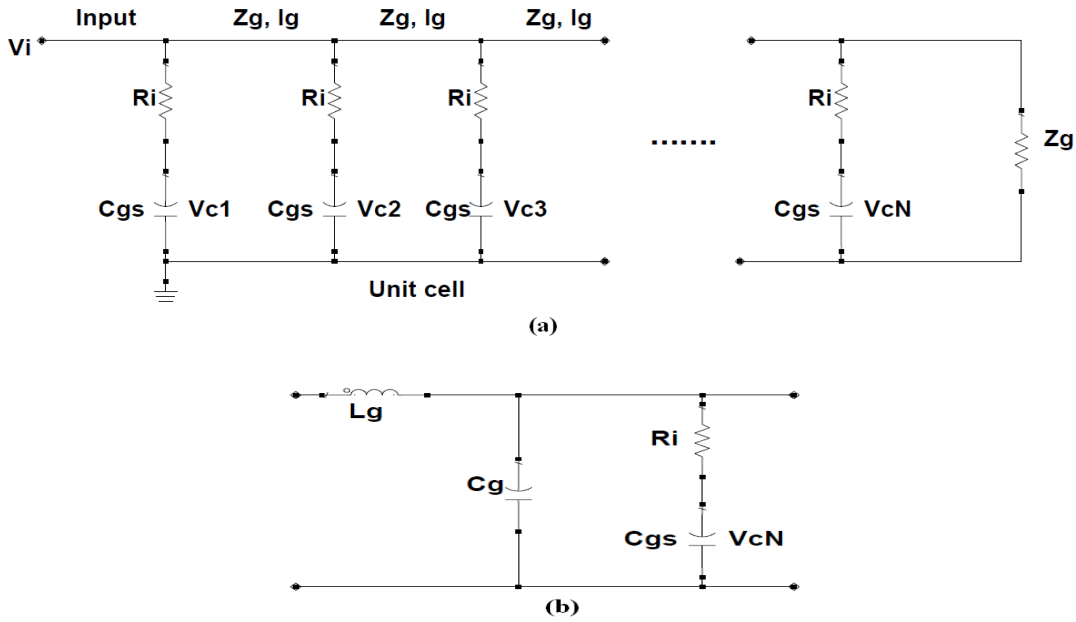


Figure 2-6 (a) Transmission line circuit for the gate line of DA, (b) equivalent circuit of a single unit cell of the gate line ([15])

Drain and gate lines are isolated except for the dependent current sources that are used to model the transistors between. These current sources are modeled as $I_d = g_m V_{cn}$. Equivalent circuits for unit cells of gate and drain transmission lines are given in Figures 2-6 and 2-7, respectively. In these equivalent circuits, L_g and C_g represent inductance and capacitance per unit length of gate line. Since C_{gs} is the gate to source capacitance and R_i is the FET input resistance, C_{gs}/L_g and $R_i L_g$ represent the equivalent per unit length loading of FET. Drain line unit cell has the same definitions for L_d, C_d, C_{ds}/L_d and $R_{ds}L_d$. These equivalent circuits use lumped element models of each FET and distributes these elements over the transmission lines.

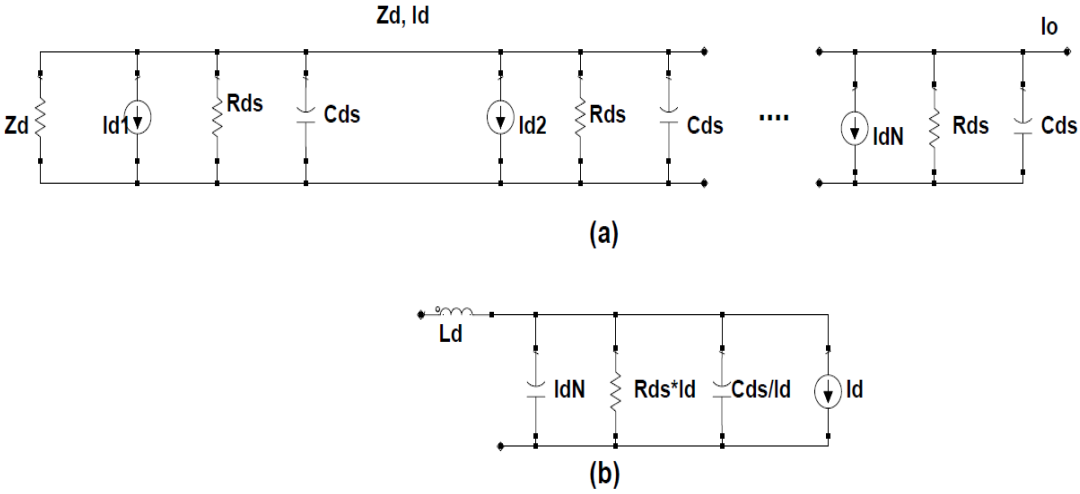


Figure 2-7 (a) Transmission line circuit for the drain line of DA, (b) equivalent circuit of a single unit cell of the drain line ([15])

Using these models, characteristic impedance and propagation constant for each line can be extracted. For gate line series impedance and shunt admittance can be written as

$$Z = jwL_g, \tag{2.11}$$

$$Y = jwC_g + \frac{jw\,C_{gs}/l_g}{1 + jwR_i C_{gs}}. \tag{2.12}$$

Neglecting the losses reduces the characteristic impedance.

$$Z_g = \sqrt{\frac{Z}{Y}} = \sqrt{\frac{L_g}{C_g + C_{gs}/l_g}}\,. \tag{2.13}$$

However for propagation constant formulation, lossy elements are kept. Thus we have

$$\gamma_g = \alpha_g + j\beta_g = \sqrt{ZY} = \sqrt{jwL_g\left[jwC_g + \frac{jw\,C_{gs}/l_g}{1 + jwR_iC_{gs}}\right]}. \tag{2.14}$$

Small loss approximation implies wR_iC_{gs} << 1, then propagation constant reduces to

$$\begin{aligned}\gamma_g = \alpha_g + j\beta_g &\cong \sqrt{-w^2L_g\left[C_g + C_{gs}\left(1 - jwR_iC_{gs}\right)/l_g\right]} \\ &\cong \frac{w^2R_iC_{gs}^2Z_g}{2l_g} + jw\sqrt{L_g\left(C_g + C_{gs}/l_g\right)}\end{aligned} \tag{2.15}$$

Drain line characteristic impedance can also be formulated after defining series impedance and shunt admittance of line as

$$Z = jwL_d, \tag{2.16}$$

$$Y = \frac{1}{R_{ds}l_d} + jw(C_d + C_{ds}/l_d). \tag{2.17}$$

Then the characteristic impedance of the drain line becomes

$$Z_d = \sqrt{\frac{Z}{Y}} = \sqrt{\frac{L_d}{C_d + C_{ds}/l_d}}\,. \tag{2.18}$$

Using small loss approximation as in the gate line, propagation constant can be represented as

$$\gamma_d = \alpha_d + j\beta_d = \sqrt{ZY} = \sqrt{jwL_d\left[\frac{1}{R_{ds}l_d} + jw(C_d + C_{ds}/l_d)\right]}$$

$$\cong \frac{Z_d}{2R_{ds}l_d} + jw\sqrt{L_d(C_d + C_{ds}/l_d)} \qquad (2.19)$$

Assuming an incident voltage of V_i is applied, then voltage on the gate capacitance can be written as

$$V_{cn} = V_i e^{-(n-1)\gamma_g l_g}\left(\frac{1}{1 + jwR_iC_{gs}}\right). \qquad (2.20)$$

The factor in the parentheses shows a voltage division between R_i and C_{gs}. As earlier for a FET, wR_iC_{gs} << 1 assumption can be used.

Transistors on each arm are defined as dependent current sources with $I_d = g_m V_{cn}$. The total output current on the drain line can be calculated if contribution from each arm is represented as

$$-\frac{1}{2} I_{dn} e^{\pm\gamma_d z}$$

propagating in each direction. Then the total output current can be written as

$$I_0 = -\tfrac{1}{2}\textstyle\sum_{n=1}^{n} I_{dn} e^{-(N-n)\gamma_d l_d}$$

$$= -\tfrac{g_m V_i}{2} e^{-N\gamma_d l_d} e^{\gamma_g l_g} \textstyle\sum_{n=1}^{N} e^{-n(\gamma_g l_g - \gamma_d l_d)} \qquad (2.21)$$

The summation terms in equation (2.21) add up in phase when $\beta_g l_g = \beta_d l_d$. This means that phase delays on each line are equalized. Backward waves for both lines are not considered since these terms are absorbed in terminations. Mathematical simplification leads to

$$I_0 = -\frac{g_m V_i}{2}\frac{e^{\gamma_d l_d}[e^{-N\gamma_g l_g} - e^{-N\gamma_d l_d}]}{e^{-(\gamma_g l_g - \gamma_d l_d)} - 1}$$

$$= -\frac{g_m V_i}{2}\frac{e^{-N\gamma_g l_g} - e^{-N\gamma_d l_d}}{e^{-\gamma_g l_g} - e^{-\gamma_d l_d}} \qquad (2.22)$$

Assuming matched input and output ports, gain of the amplifier can be written as

$$G = \frac{P_{out}}{P_{in}} = \frac{\frac{1}{2}|I_0|^2 Z_d}{\frac{1}{2}|V_i|^2/Z_g}$$

$$= \frac{g_m^2 Z_d Z_g}{4}\left[\frac{e^{-N\gamma_g l_g} - e^{-N\gamma_d l_d}}{e^{-\gamma_g l_g} - e^{-\gamma_d l_d}}\right]^2. \qquad (2.23)$$

Phase equalization condition reduces gain to

$$G = \frac{g_m^2 Z_d Z_g}{4}\frac{(e^{-N\alpha_g l_g} - e^{-N\alpha_d l_d})^2}{(e^{-\alpha_g l_g} - e^{-\alpha_d l_d})^2}. \qquad (2.24)$$

For small loss approximation, denominator in equation (2.24) can be reduced to $(\alpha_g l_g - \alpha_d l_d)$.

Equation (2.24) can also be reduced for lossless case as

$$G = \frac{g_m^2 Z_d Z_g N^2}{4}. \qquad (2.25)$$

Equation (2.25) shows that gain increases by N^2. For a cascaded stage gain increases as $(G_0)^N$. For a DA as stages go to infinity, gain approaches zero if loss is also considered. This fact is explained in a simple manner. As waves travel through gate line, amplitude of the wave decays exponentially such that no input signal achieves to the end of the amplifier (as N -> ∞). Same behavior on the drain line attenuates the amplified signals in earlier stages. Since attenuation is very high, the amplified signals never reach to the output.

This implies that there is an optimum value of N that maximizes the gain. By differentiating equation (2.23) and setting it to zero gives

$$N_{opt} = \frac{\ln(\alpha_g l_g/\alpha_d l_d)}{\alpha_g l_g - \alpha_d l_d} \qquad (2.25)$$

CHAPTER 3

PROPOSED TOPOLOGY FOR DISTRIBUTED AMPLIFICATION

3.1 Introduction

Different types of broadband amplification are discussed in Chapter 2. Among these methods distributed amplification seems to overcome the limitation of gain-bandwidth product which is the reason that distributed amplification has caught much attention for broadband amplifier design [16-18].

In this thesis distributed amplification is chosen as the basis for design. As discussed in Chapter 2, distributed amplification merges input and output capacitors in a virtual transmission line. Thus a theoretical bandwidth of infinity is achieved. Amplifying paths of a distributed amplifier operates in the same manner through the band of the whole amplifier which means that no frequency selectivity is applied.

Proposed topology can be considered as a kind of distributed amplifier; however it operates in a different manner. Power is distributed among different paths taking into account the frequency band. Input power is divided into frequency bands and amplified separately. Then these amplified signals are combined at the output. A single stage 0.1-1 GHz with a gain of 14.5+/-1dB is designed with this method.

This chapter discusses the details of the design. Parts of the design are explained with simulation and measurement results. Optimization procedure used in this design is also explained.

3.2 Proposed Topology for New DA

In this new distributed amplifier structure, a very simple method is used. Dividing an input signal into frequency bands and combining after amplification seems a relatively easy method. However in reality the situation is far away from an easy task. An input signal can be divided into frequency bands with de-multiplexer schemes; however combining these signals after amplification, limitation, etc is not straightforward. Since phases of the signals vary through these processes, the combining task is quite complicated. Despite its simple basis, there are only a few papers for this method [19]. In this work this difficulty is overcome by adjustments on the amplifying paths with help of an optimization procedure.

3.2.1 Principles of The Topology

As mentioned at the beginning of this chapter, topology of the new DA depends on dividing an input signal, then amplifying and combining afterwards. Generalized sketch for the proposed topology is provided in Figure 3-1

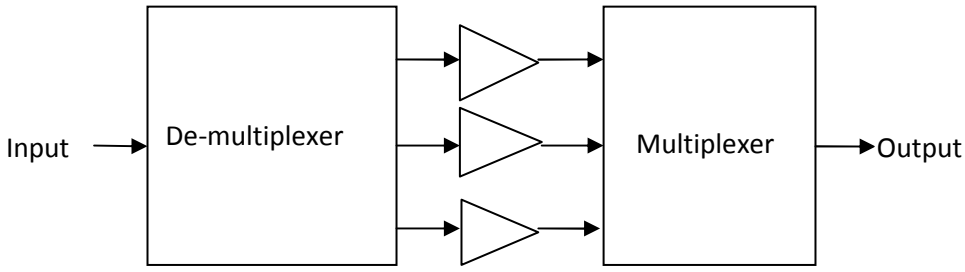


Figure 3-1 Generalized topology for the proposed amplifier

First input signal is divided into frequency bands by a de-multiplexer. But it is important to note that the frequency bands' -3 dB points meet. This means that at the corner frequencies two bands make contribution and add up at the output.

The number of frequency bands may change depending on the application. More channels may be used in a power amplifier where efficiency is one of the main concerns. However it should be mentioned that the more the number of channels

(frequency bands), the harder to design the de-multiplexer, and the harder to adjust the phases before combining. On the other hand lower number of frequency bands means that each amplification path should operate in a wider bandwidth which makes the design of the individual amplifier harder. Optimum number of channels should be chosen carefully. In this work, a 3-channel design is preferred. A 3-channel de-multiplexer is easy to design with simple filters. And this also gives an adequate freedom for design of amplifying paths. A reasonable approach for dividing the frequency band into sub-channels is to use equal length channels in logarithmic scale. This balances the task load required for matching individual channels. The related calculation for frequency bands' 3 dB corners is straightforward.

From logarithmic division of the band 0.1-1 GHz, the 3 dB corner frequencies for the channels are at 100 MHz, 215 MHz, 465 MHz and 1000 MHz. Then this channelized signal is amplified through amplifying paths where transistors are matched with different schemes and adequate gain is obtained. Finally the signals are combined with a multiplexer.

3.2.2 De-Multiplexer

As mentioned above, a 3-channel design is preferred which makes the de-multiplexer task easier. Considering the frequency band of designed amplifier, lumped element de-multiplexer should be sufficient.

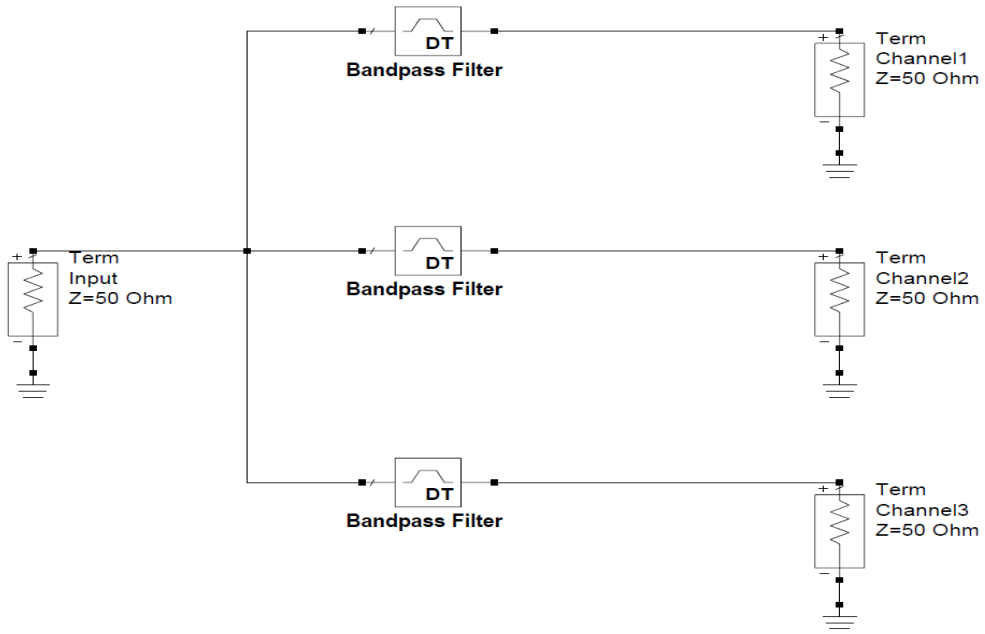


Figure 3-2 Sketch of De-multiplexer

There are different ways to design this de-multiplexer. A low pass-high pass filter followed by another low pass-high pass filter is one option. Band pass filters combined at a node, which is used in this design, is another option. Moreover combining filters along with a manifold can also be considered [20-22].

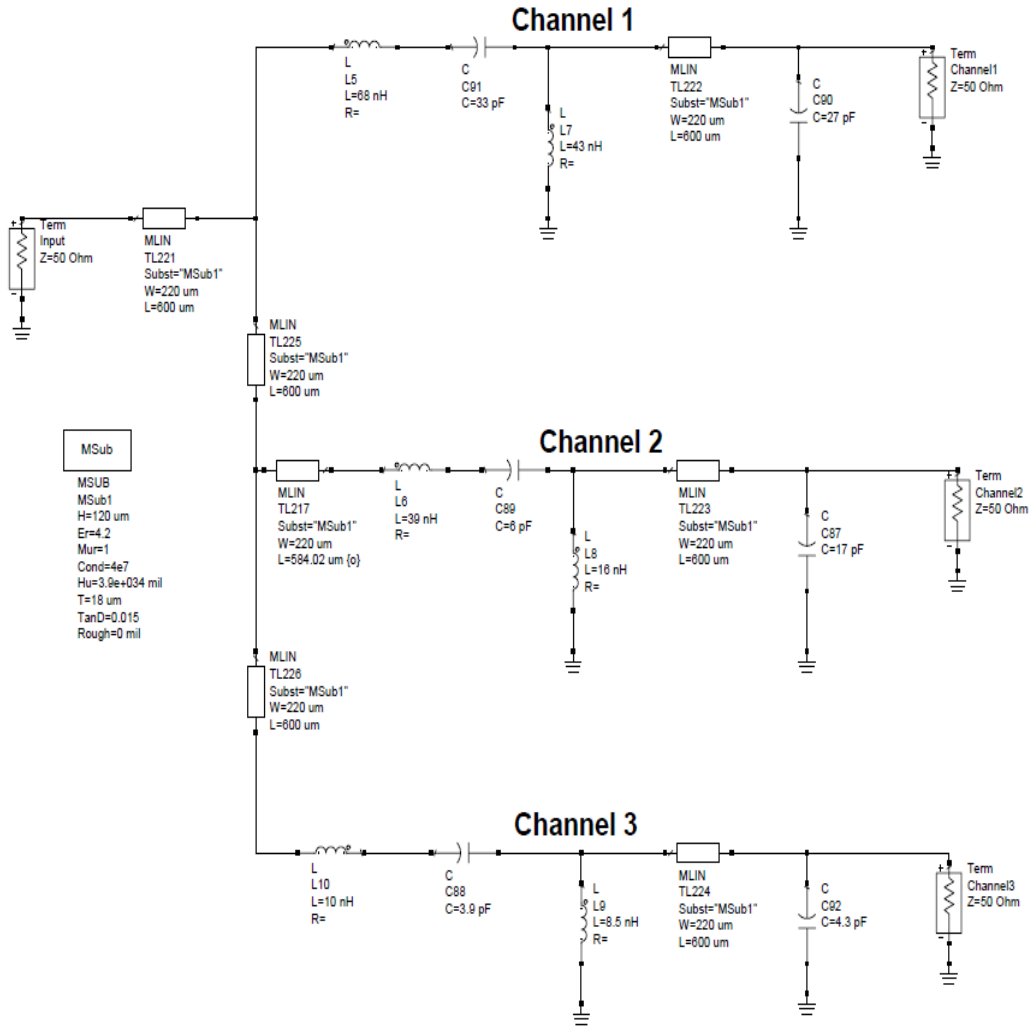


Figure 3-3 Schematic of De-multiplexer

Band-pass filters combined at a node is chosen since it provides more isolation between channels than lp-hp scheme, and it is easier to design than a manifold multiplexer.

An important reminder is that frequency bands meet at -3 dB corner points. This should also be considered as a design parameter. Butterworth filters are chosen for the task. On the other hand, Chebychev or elliptic filters can also be used. What is meant here would be clearer on transmission loss sketch for the filters. Figure 3-4 shows transmission losses for the de-multiplexer. S(2,1) depicts the first channel's insertion loss, S(3,1) shows the second channel's loss and S(4,1) indicates the third channel's insertion loss. As can be seen from Figure 3-4 channel 1 and 2 meet at

their -3 dB corners. The same is also true for channels 2 and 3 which indicates that channel 1 and 2 amplifies some portion of frequency spectrum together. Since it is the -3 dB corner for both of the filters, when they add up with the same phase, insertion loss is zero theoretically. Channels 2 and 3 have the same relationship as channel 1 and channel 2 have. As mentioned earlier corner frequencies are set to 215 MHz and 465 MHz. Figure 3-5 and 3-6 shows the related return loss graphs for all of the three filter outputs and for the input. Graph indicates that at the intersection points return loss for the output is around -6 dB.

These relationships between channels are important in the design process, since after de-multiplexing and amplifying, channels are added up at the output. The common points of frequency channels should have the same phase for a proper summation. This phase equalization is described in the later sections.

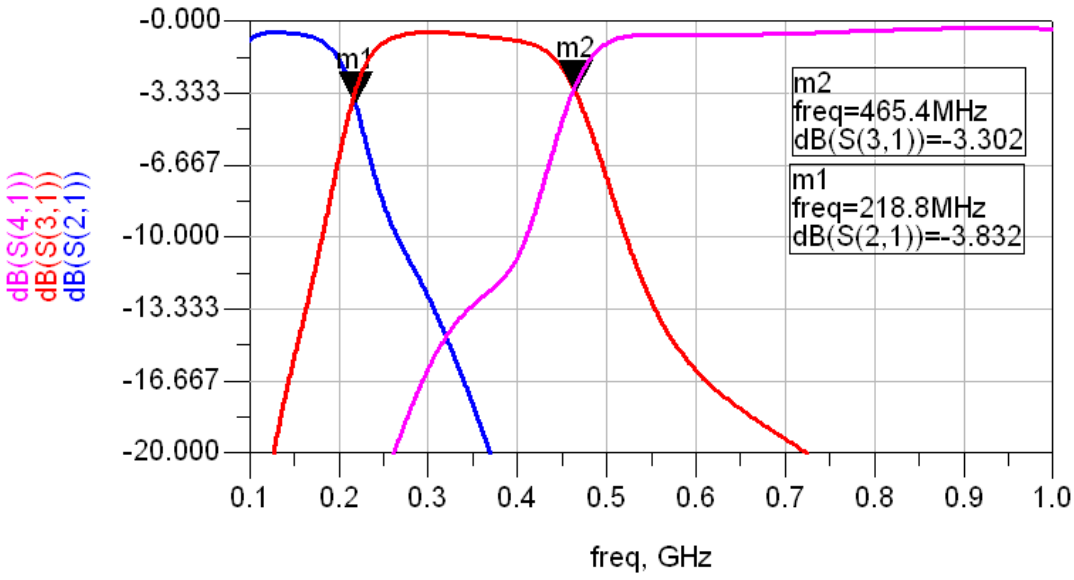


Figure 3-4 Insertion Losses for De-multiplexer Channels

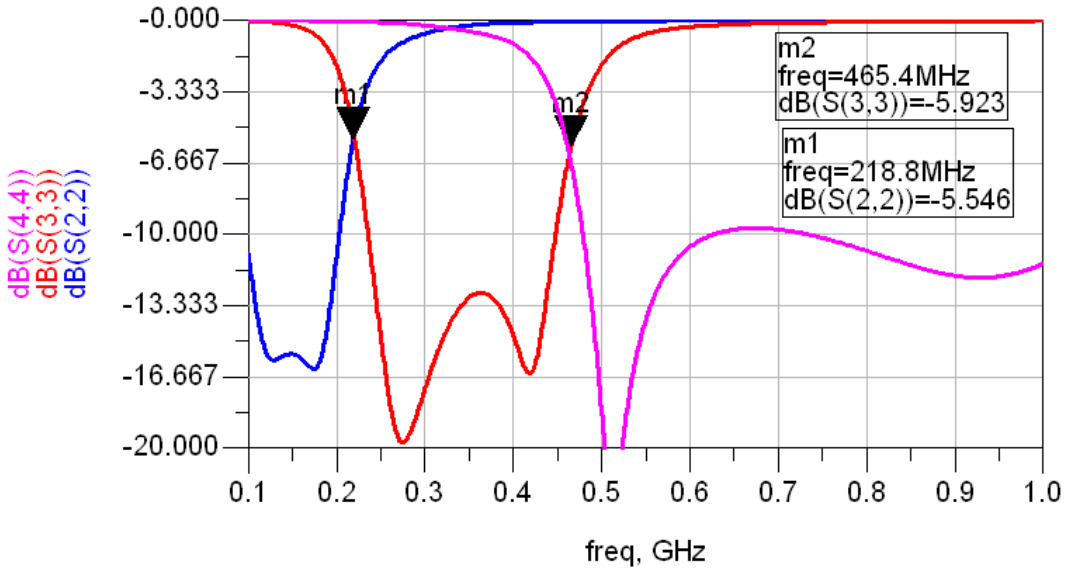


Figure 3-5 Return Losses at Channels' Output

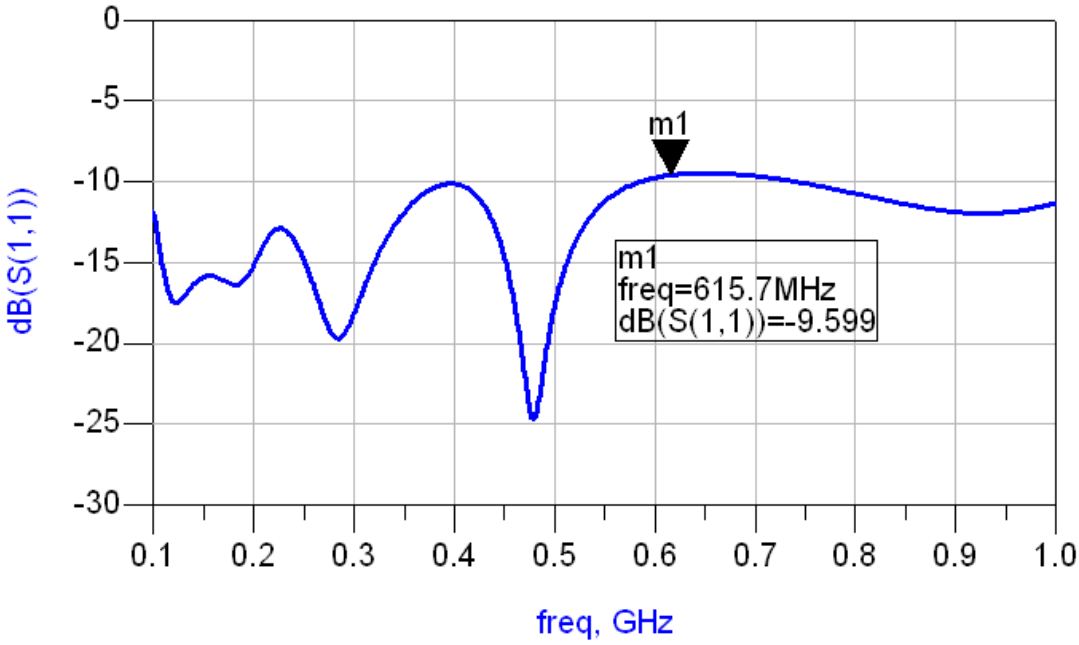


Figure 3-6 Return Losses at Input

3.2.3 Amplifying Paths

Amplifying paths of the amplifier provides gain over the specified bandwidth. There are three amplifying paths, which consist of single-stage matched transistor

amplifiers, associated with each channel. Low pass matching is selected for its simple design procedure and predictable phase characteristics which will be important during the combining process.

The procedure for the design is similar for a standard RF and microwave amplifier.

a) A transistor is selected for the desired gain and bandwidth. Achievable output power is also taken into account. As mentioned before, selected transistor should have a wide band of operation (low input and output capacitance) which is critical in order to have a flat gain throughout the band.

Considering these requirements, Avago Technologies' ATF52189 transistor is chosen whose operation frequency is from 50 MHz to 6 GHz with 16 dB gain at 2 GHz. Its associated output power is 27 dBm (at 4.5V and 200 mA). In this design operating voltage is selected to be 4.5V with a quiescent current of 120 mA. Small signal models and non-linear transistor model are provided by Avago. Figure 3-7 displays maximum available gain and $|S_{21}|^2$ graphs provided for ATF52189.

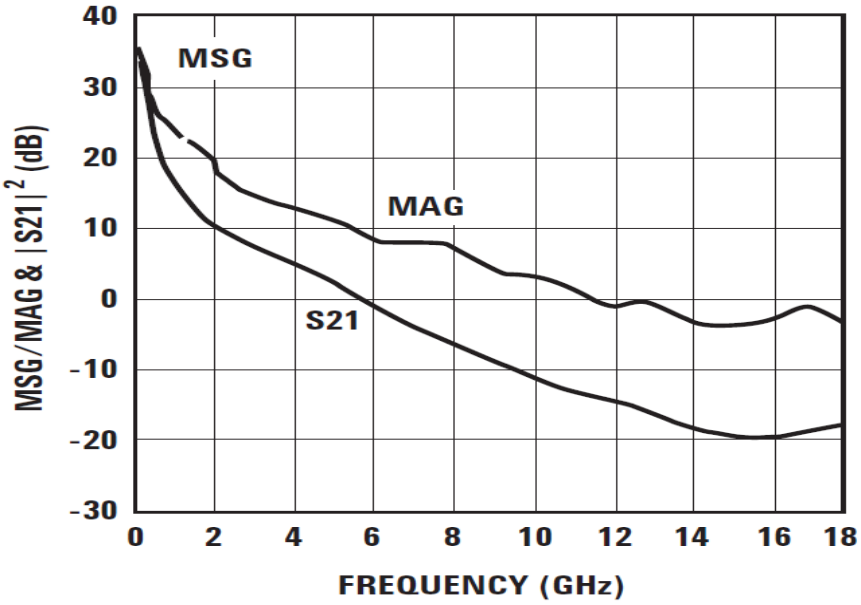


Figure 3-7 Maximum available gain and $|S_{21}|^2$ graphs provided for ATF52189 ([24])

b) Related RF chokes and DE blocks are selected for each frequency band.

For band-1 RF chokes are selected to be 330 nH. DC blocks are selected to be 270 pF. For band-2 RF chokes are selected to be 120 nH. DC blocks are selected to be 120 pF. For band-3 RF chokes are selected to be 68 nH. DC blocks are selected to be 82 pF.

Circuit schematic with RF chokes and DC blocks is given in Appendices C.

c) Topology for the amplifiers is selected. Even though whole frequency band of operation is divided into channels, each channel itself is wide enough to cause problems for matching. Thus a matching for wideband operation is necessary. In Chapter 2, when broadband amplifiers are discussed, feedback amplifiers are mentioned as a simple and good way of achieving broadband operation. The proposed design makes use of feedback topology in the amplifying paths. For this purpose a resistive feedback is used for all of the transistors.

A resistive feedback is very useful in obtaining a relatively wide band which also improves the stability of the amplifier. On the other hand, gain is reduced depending on the feedback element used; thus care should be taken in choosing the amount of feedback. Lower resistance value of feedback brings up higher feedback constant which also brings up lower gain and higher stability. Taking into account all these factors, a resistive feedback of 220 Ohms is selected for band-1. And a resistive feedback of 270 Ohms is selected for band-2 and band-3. Lower resistance value for band-1 is due to higher gain of transistors at lower frequencies. By this way gain of band-1 transistor is reduced more than the other two, giving a flat gain response for the whole band. It is observed that feedback element values below 220 ohms cause remarkable reduction in gain. On the other hand, element values above 270 ohms do not have much effect on the performance of transistor.

d) Input and output impedances are extracted. It should be kept in mind that amplifier is designed with a feedback. Any kind of feedback changes input and output impedance of the transistor. Feedback should be taken into account when matching is considered. Thus from now on when impedance is mentioned, transistor ATF52189 with a 270 Ohm resistance and DC block capacitance feedback should be

considered. Datasheet for ATF52189 provides related input and output loads for optimum OIP3 and output power separately. Optimum input and output loads are calculated using a load-pull system; thus impedance values can be directly used to design matching circuits. However since this transistor has a wide band, datasheet only provides optimum impedance at certain frequencies. It should be noted that impedance value can change from one frequency point to another very rapidly.

Datasheet provides optimum input and output load impedances for each of the specified quiescent points. Related optimum output impedance values for this transistor biased at 4.5V 120 mA are also provided by Avago Tech. Equation (3.1) can be used to convert these values to impedances easily; however it should be noted that magnitude and reflection of the transistor is given only at 0.5 GHz. In order to design amplifying paths including a range of 0.1 GHz to 1 GHz, impedances for this range should be extracted.

$$Z_L = Z_0 \frac{1 + \Gamma_0}{1 - \Gamma_0} \tag{3.1}$$

Avago Technologies use source-pull and load-pull techniques to extract impedance information. In load-pull and source-pull technique, impedance presented to a device is varied and some parameters are monitored during these changes of impedance. In load-pull, load presented to active device is varied. In source-pull, source impedance is varied during the process. Load and source pull measures a device's impedances under actual operating conditions at which device is biased and a signal of magnitude enough to obtain the required output power is applied. In general this process is not applied to linear devices that operate under small-signal conditions. It is more often used in determining large-signal, non-linear device impedances. The setup for load-pull analysis is very cumbersome and expensive. The impedance variation for input and output are provided with tuners. Input tuner is adjusted such that input power is always constant even when the output tuner is adjusted. By changing output and input tuner simultaneously, maximum output power is achieved. This occurs at only one point. Then impedance values corresponding to lower power levels are extracted. By this way a set of impedance values are obtained. These values correspond to contours on Smith chart. The same

process can be applied to obtain impedance values corresponding to maximum efficiency and minimum noise figure.

As mentioned, load-pull and source-pull are expensive techniques that may not be available in all laboratories. Instead of using traditional load-pull and source-pull, the proposed design topology features a simulation based impedance tune technique in order to obtain maximum gain available from the transistor.

Before moving on with simulation based load-pull technique, it would be necessary to recall some mathematical background for simultaneous conjugate matching. In his book Gonzales clearly explains the math behind simultaneous match [10]. Gonzales explained simultaneous match for bilateral case which corresponds to S_{12}≠0 for a device. S_{12}=0 is observed (unilateral case) when the isolation from output to input is infinite. When S_{12}=0, S_{11} value directly indicates input impedance and S_{22} value shows output impedance value to be matched. Reflection (matching) on input port does not affect output port reflection and vice versa. However in reality, transistors are always bilateral. For bilateral devices, as input match changes output match is also affected. Thus a simultaneous match for input and output is required.

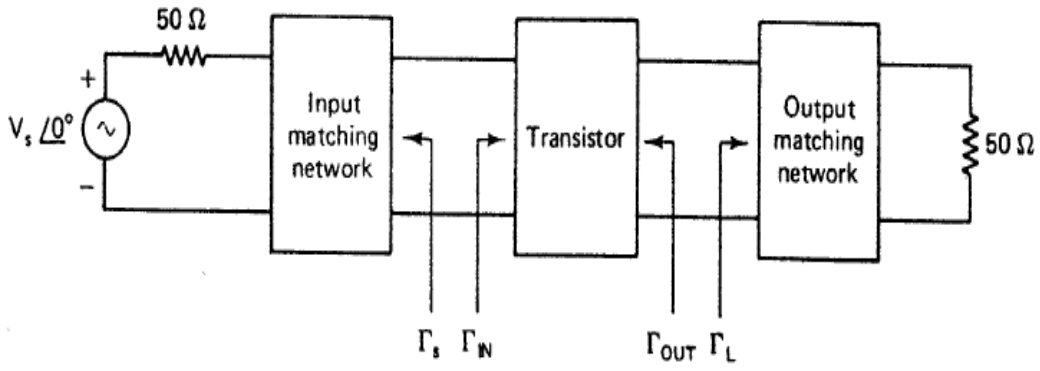


Figure 3-8 Generalized amplifier topology ([10])

Figure 3-8 shows a generalized amplifier circuit. Maximum transducer power from this kind of circuit is obtained when

$$\Gamma_{in} = \Gamma_S^* \tag{3.2}$$

and

$$\Gamma_{out} = \Gamma_L^* \quad . \tag{3.3}$$

The required source and load impedances are given as

$$\Gamma_S^* = S_{11} + \frac{S_{12}S_{21}\,\Gamma_L}{1 - S_{22}\Gamma_L} \tag{3.4}$$

and

$$\Gamma_L^* = S_{22} + \frac{S_{12}S_{21}\,\Gamma_S}{1 - S_{11}\Gamma_S} \quad . \tag{3.5}$$

As can be seen from equations (3.4) and (3.5), source and load reflection coefficients depend on each other. Solving these two equations simultaneously gives values for Γ_s and Γ_L. Calling these Γ_{Ms} and Γ_{ML}, and solving gives

$$\Gamma_{Ms} = \frac{B_1 \pm \sqrt{B_1^2 - 4|C_1|^2}}{2C_1} \tag{3.6}$$

$$\Gamma_{ML} = \frac{B_2 \pm \sqrt{B_2^2 - 4|C_2|^2}}{2C_2} \tag{3.7}$$

where

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 \tag{3.8}$$

$$B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |\Delta|^2 \tag{3.9}$$

$$C_1 = S_{11} - \Delta S_{22}^* \tag{3.10}$$

$$C_2 = S_{22} - \Delta S_{11}^* \tag{3.11}$$

In his book Gonzales proves that the only solution for unconditionally stable operation comes from the solutions with the minus sign. Then the corresponding Γ_s and Γ_L can be calculated from these equations.

Simultaneous conjugate match gives maximum transducer gain. If gain values other than the maximum are required, constant gain circles can be drawn.

Agilent's ADS simulation program draws source and load constant gain circles on Smith chart. Using these utilities of ADS, impedance values are easily determined for specific gains. An example circuitry for constant gain circle of ATF52189 (4V5 120 mA) at 100 MHz is given in Figure 3-10. Box in the middle of the circuit is a data item for S-parameter values of ATF52189 (4V5 120 mA). GaCircle item on the left of Figure 3-9 is placed for drawing constant gain circles for source mismatch. GpCircle item is used for drawing constant gain circles for load mismatch. Figure 3-10 shows gain circles drawn on Smith chart. By placing a marker on contours, impedance values required for each specific gain are determined.

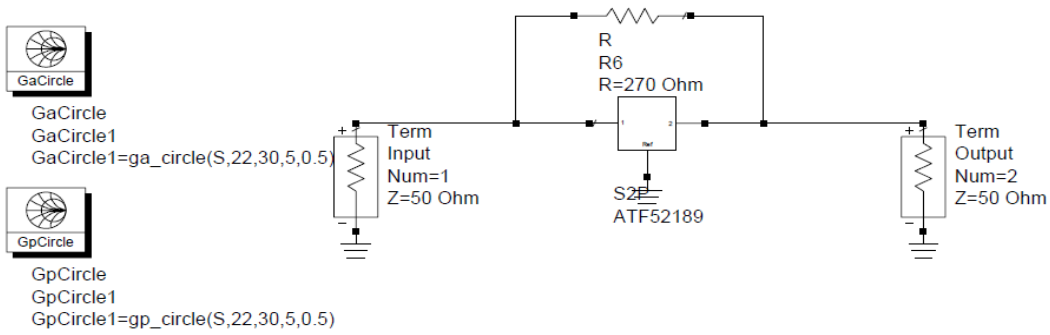


Figure 3-9 ADS circuit for gain circle extraction

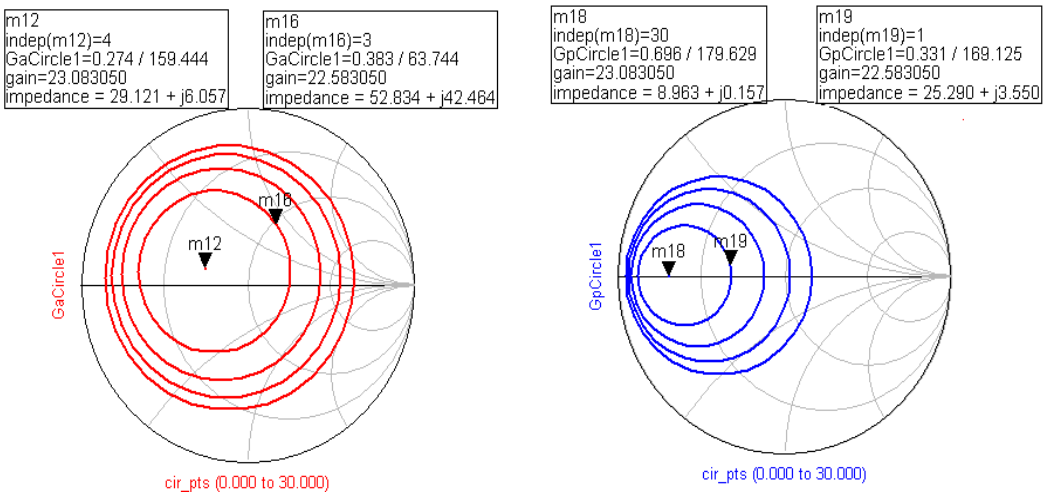


Figure 3-10 Constant gain circles for ATF52189

In Figure 3-10, left Smith chart shows constant gain contours for source mismatch. Smith chart on the right shows constant gain circles for load mismatch. As can be seen from Figure 3-10, maximum gain is achieved at only one point for both input and output. This point is the simultaneous conjugate match point. Contours around the center point are constant gain circles for gain values descending by 0.5 dB. Any number of points for any number of different gain values can be drawn and impedance values can be determined. Table 3-1 gives simultaneous conjugate match points extracted at different frequencies using ADS.

Simultaneous conjugate match and constant gain circles provide a neat way to find input and output impedances for matching. In this thesis, another way to find out the required input and output matching impedances is also carried out. This method makes use of ADS' optimization tool. The circuitry for impedance extraction is given in Figure 3-11.

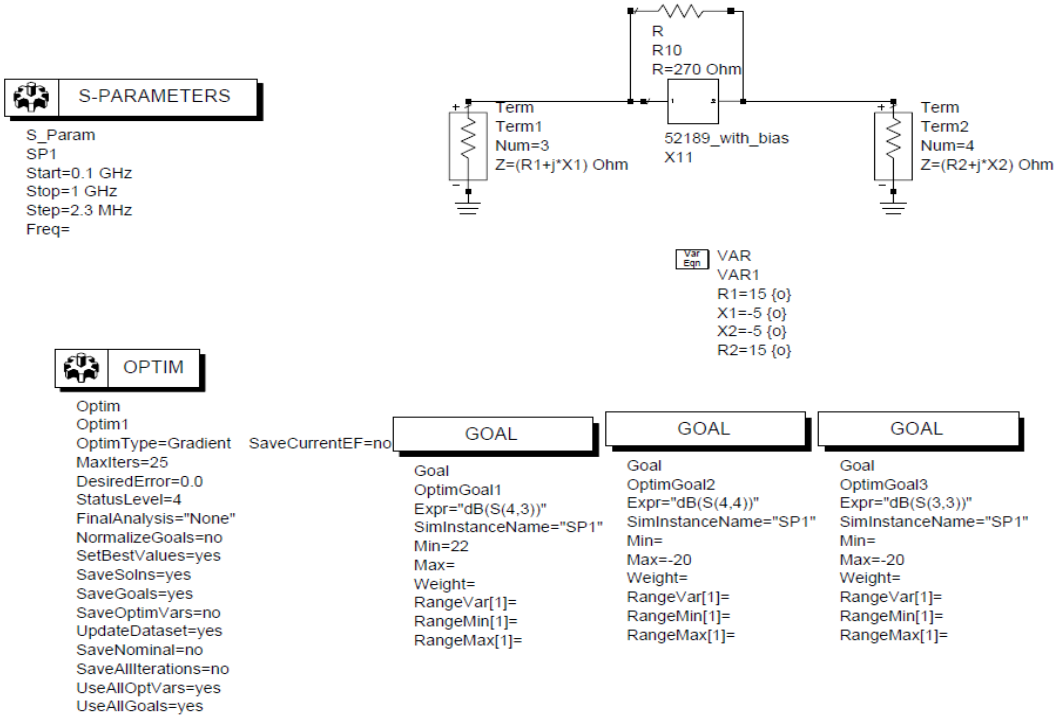


Figure 3-11 Proposed simultaneous conjugate match method

ADS' Optim tool enables a bunch of optimization methods. The suitable method for any desired application can be selected. As can be seen from the Figure Optim tool is

placed with some Goal definitions. These definitions specify the limits that Optim is trying to achieve. S-parameter tool is used since a small signal operation is performed.

Input and output terminations are specified as R1+j*X1 and R2+j*X2 Ohms respectively. R1 and R2 represent real parts of the impedances; whereas X1 and X2 represent imaginary parts of the impedances. These four parameter values are optimized during optimization process. The optimization for R1 and R2 is limited between 1 and 50; whereas the limit for X1 and X2 is set to -50 and +50, considering they represent imaginary parts and can also take negative values. Feedback resistance is also placed as mentioned in the beginning of the amplifying paths. There are 3 goals that can be set for impedance calculation. First one is gain that is to be maximized which is represented by S(4,3), gain from input termination to output termination. The other goals are reflection losses, S_{11} and S_{22}. As S_{21} is expected to be greater than 20 dB, return losses are expected to be lower than -15 dB. These values can be adjusted for different transistor types. As the optimization method, Gradient is selected. Although gradient may stuck in local minima, it happens to be a useful method for this kind of impedance pull operation.

The simulation is done within 100 MHz intervals. Figure 3-12 shows S(2,1), S(1,1) and S(2,2) in logarithmic diagram after optimization of impedance values between 100 MHz and 200 MHz.

It is very important to remind that these impedance values are for terminations at the input and output. Impedance of the transistor is complex conjugate of these values. For convenience termination impedance values are mentioned as impedances to be matched.

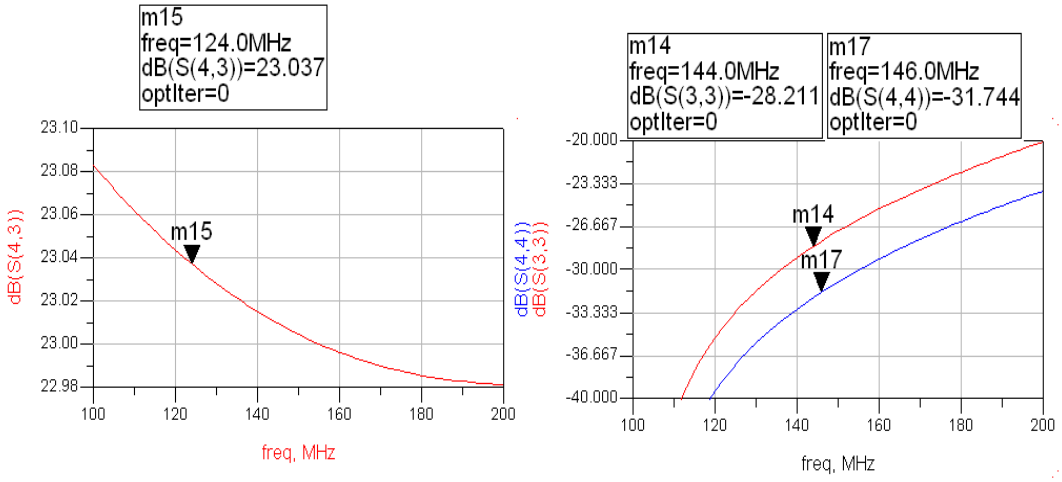


Figure 3-12 Obtained amplifier responses from simultaneous conjugate match

As can be seen from Figure 3-11, goals of optimization are achieved. The impedance values are given in Table 3-2.

Two methods can be used to determine input and output impedances of a transistor. These two methods can be compared using Table 3-1 and Table 3-2.

Table 3-1 ATF52189 impedance extracted from gain circles

	Constant Gain Circle Measurement	**Constant Gain Circle Measurement**
Frequency	**Input Impedance**	**Output Impedance**
150 MHz	26.5+j8.2 Ohms	9.4+j0.5 Ohms
250 MHz	20.38+j10.38 Ohms	10.27+j1.5 Ohms
350 MHz	13.11+j11.3 Ohms	11+j4.3 Ohms
450 MHz	5.6+j9 Ohms	9.76+j10.1 Ohms
550 MHz	5.2+j8.45 Ohms	10.1+j5.1 Ohms
650 MHz	4.8+j1.1 Ohms	17.3+j2.2 Ohms

Table 3.1 (continued)

750 MHz	7.1-j5 Ohms	19.5-j0.1 Ohms
850 MHz	9-j11 Ohms	15.1-j12 Ohms
950 MHz	10.2-j7.3 Ohms	14-j11.1 Ohms

Table 3-2 ATF52189 impedance extracted from proposed method

	Optimization Method	**Optimization Method**
Frequency	**Input Impedance**	**Output Impedance**
100-200 MHz	29.12+j6.05 Ohms	8.96+j0.15 Ohms
200-300 MHz	21.5+j14.2 Ohms	8.8+j1.2 Ohms
300-400 MHz	13.1+j11.2 Ohms	11.2+j4.3 Ohms
400-500 MHz	7.5+j7.8 Ohms	12.5+j7 Ohms
500-600 MHz	7+j5.1 Ohms	12.4+j4.17 Ohms
600-700 MHz	6.8+j0.2 Ohms	19.5+j1 Ohms
700-800 MHz	7.4-j1.78 Ohms	19.6-j6 Ohms
800-900 MHz	8.6-j2.6 Ohms	16.3-j7.5 Ohms
900-1000 MHz	9.23-j4.54 Ohms	14.8-j9.8 Ohms

Table 3-1 and Table 3-2 clearly display similar results for lower frequency parts. For higher frequency parts, there happens to be a difference in both imaginary part and real part of impedances. The difference here is caused by the definition of goals which is set to optimize impedances in the second method. For higher frequency optimization gain is set to be lower than the lower frequency parts due to convergence issues, whereas return loss limit is set to be -13 dB (-15 dB for lower frequencies). And also in the second method, optimization is performed in a 100 MHz interval. In constant loop extraction, a single frequency is set. This difference in frequency setting makes the second method an approximation for the band of

interest. The band used to optimize should be made smaller in order to get similar results. However this impedance data is enough to design matching circuits for all of the frequency range.

e) Now that the input and output impedances are extracted, matching circuits can be designed. Low-pass matching topology is selected for all three channels. As mentioned earlier, low-pass topology is selected due to its simple structure and predictable phase characteristics. Butterworth type matching is also preferred as channels add up at the output. Since Butterworth matching has maximally flat response, summation at the end would yield a flat gain response for the whole band.

The second method based on optimization seems to be a valid method to extract impedance data after comparing with constant gain circle data. Thus it would be advantageous to use the second method; however this time optimization is performed for all frequency points in each channel. That is to say, optimization on impedances is performed first on 100 MHz to 215 MHz interval (1st channel). Then impedances are optimized for 215 MHz to 465 MHz (2nd channel) and for 465 MHZ to 1 GHz (3rd channel). Table 3-3 shows impedance values for both input and output that are used in order to design matching circuits for each of the channels.

Table 3-3 Impedance values used for matching in each channel

Channel Number	Frequency Band	Input Impedance	Output Impedance
1	100-215 MHz	22+j9 Ohms	10+j1 Ohms
2	215-465 MHz	15.4+j9.4 Ohms	11+j3 Ohms
3	465-1000 MHz	9.64-j2.5 Ohms	15.1-j8 Ohms

Keeping in mind that these impedances represent terminations, matching circuitry can be designed by taking complex conjugate of these impedances. In order to design matching for input and output, ADS' Smith chart matching utility is used. This

tool enables the user to define two impedances to be matched. And user selects elements to be used in matching circuits. Both lumped and distributed elements may be placed in order to match these impedances. Smith chart in the utility visualizes the impedance change through matching elements. A frequency at which matching is performed is given which means that a single frequency point is specified for matching. For a broader band matching, impedance values obtained from Smith chart matching tool are optimized.

In Figures 3-13, 3-14 and 3-15, matching circuit topologies are given. As can be seen from figures, matchings are performed with parallel capacitors and series inductors. Order of matching may change depending on the impedance to be matched. For instance, for channels 1 and 2 matching is performed with one inductor and two capacitors. On the other hand, for channel 3 input matching is designed with one inductor and one capacitor, whereas output matching for channel 3 is performed with 2 inductors and 3 capacitors. Initial designs for all three channels were same. During the simulation and re-design process, it is observed that a lower order matching is enough for input matching of channel 3. On the other hand, observation on output matching of channel 3 yielded a higher order matching circuit.

ADS' 'Optim' tool has been used to extract impedances to be matched. For that method, goals are specified for gain and return losses. 'Optim' gives equal weight on each of these goals and varies impedance values of input and output terminations. This time goals are again specified as before (gain > 20-23 dB, return losses < -15dB); however elements to be optimized are lumped element values instead of impedance values themselves.

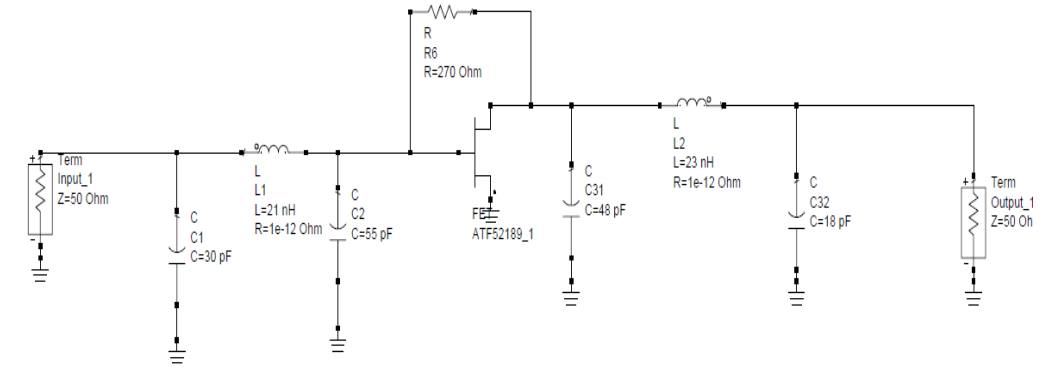


Figure 3-13 Channel 1 initial design

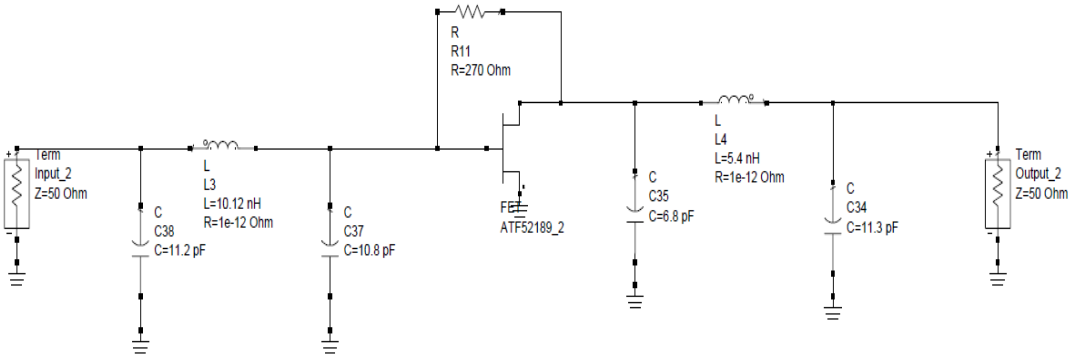


Figure 3-14 Channel 2 initial design

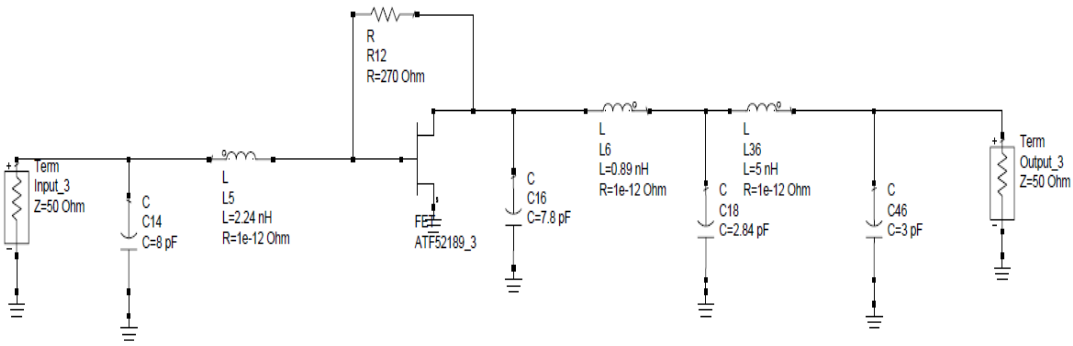


Figure 3-15 Channel 3 initial design

As mentioned earlier, matching elements are first extracted in Smith chart tool then these values are optimized for a broader operation.

After optimization, lumped element values are updated and then channels are simulated with these elements. Results are shown in Figures 3-16, 3-17 and 3-18.

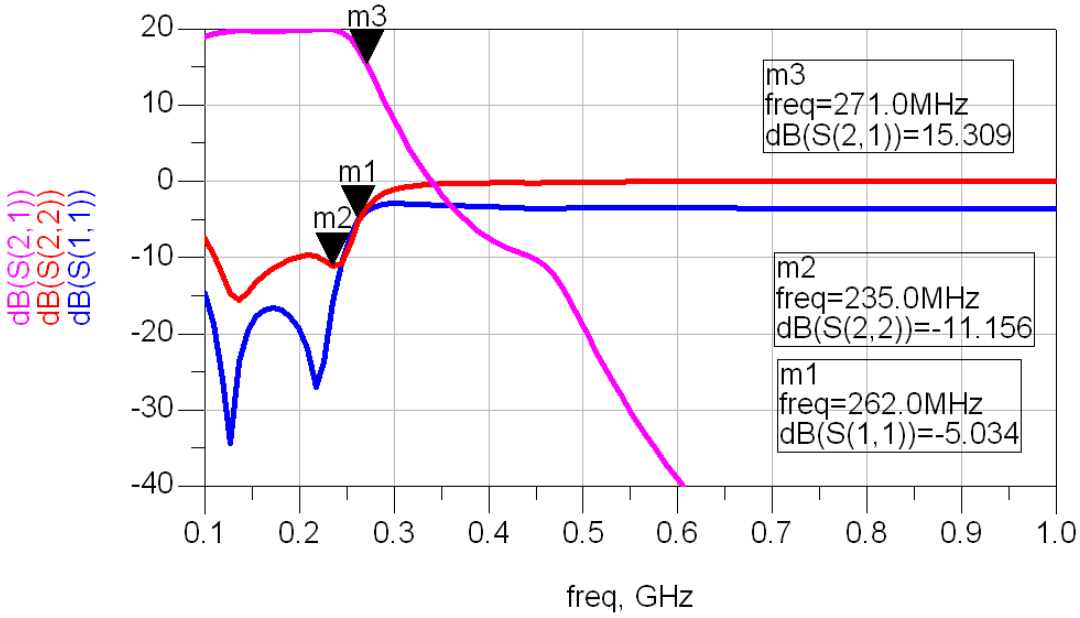


Figure 3-16 Channel 1 amplifying path result

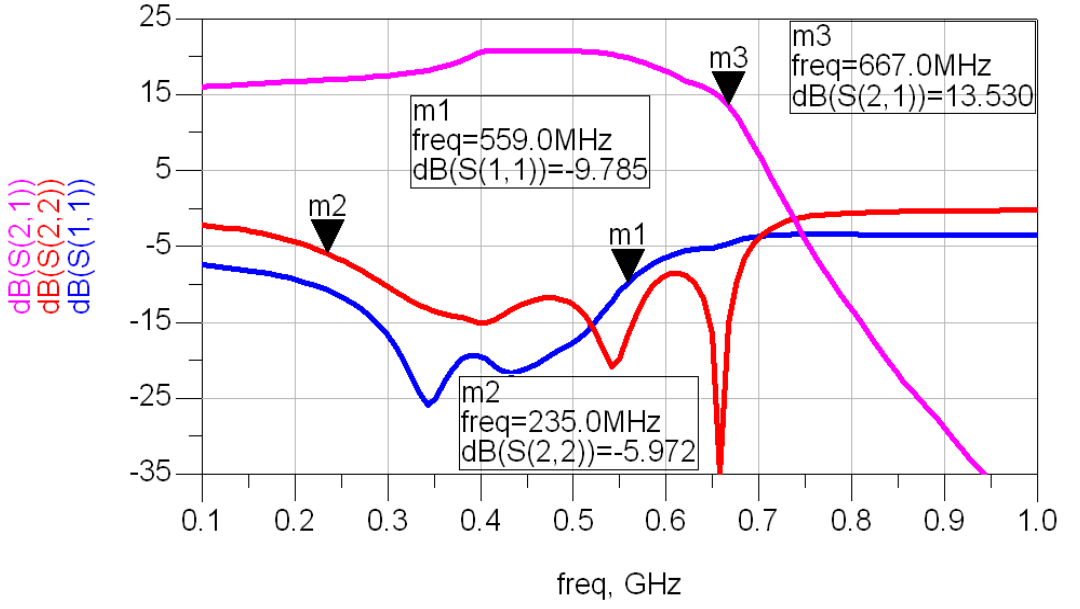


Figure 3-17 Channel 2 amplifying path result

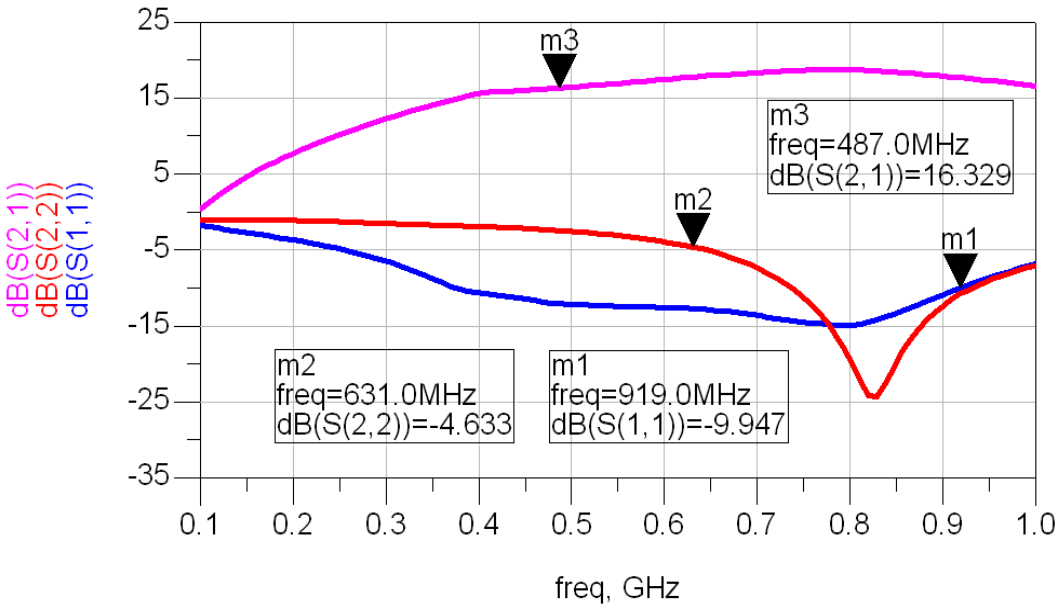


Figure 3-18 Channel 3 amplifying path result

Figure 3-16 shows gain and return losses for channel 1. As can be seen, in the band of interest gain is more than 20 dB and return losses for input and output are also as desired. Figure 3-17 shows gain and return losses for channel 2 as Figure 3-18 shows for channel 3. In the figures channel 1 input and output are represented with 1 and 2 respectively. Channel 2 is represented with port numbers 3 and 4 as input and output. Likewise, channel 3 is represented with 5 and 6. For instance S(6,5) depicts gain between input and output ports of channel 3.

3.2.4 Multiplexer

Up to now, de-multiplexer divided an input signal into frequency bands and these channelized signals are amplified through amplifying paths (each channel with different amplifying circuits). Multiplexer adds up these channelized signals. For simplicity multiplexer uses the same configuration as de-multiplexer which employs lumped elements defined in 3.2.2.

It should be reminded that signals from different channels add up at their -3 dB corner points. At these corners amplified signals from neighbor channels should

have the same phases at the output; otherwise signals would not add up. Since multiplexer uses the same structure of de-multiplexer, phase adjustments could not be done by adjusting element values. This would change the filtering properties of the multiplexer; thus phase should be equalized in amplifying paths section of the amplifier.

Optimizing elements of amplifying sections could change the properties defined for each channel. Also optimizing in one frequency point could change the phase properties at another frequency point. Computer based optimization tool can be used in order to match the phases of the channels. 'Optim' tool of the simulation program is used twice before in this project. However optimizing this many elements would require a different treatment.

3.3 Optimization of the Circuit

As mentioned earlier, phases of the amplified signals from channels should be equal at the intersection points of the channel bands. Since de-multiplexer and multiplexer remain unchanged, amplifying paths should be optimized in order to obtain phase synchronization. Elements used to match the transistors to 50 Ohms can be optimized for this purpose. However care should be taken on the overall response of each amplifier, since slight changes may cause undesirable amplitude response.

One way to optimize this kind of circuitry is to model every transistor and every element related to matching by mathematical equations. Then by using these equations, gain and return losses can be formulated. An optimization can be conducted to maximize the gain and minimize the return losses. However it would require a cumbersome programming and modeling which is out of the scope of this thesis.

ADS' optimization tool Optim was employed in this thesis before, for extracting impedance values and for matching element optimization. Optim can easily be used to optimize the amplifying paths for phase synchronization. However even with a good computer, optimization with this many elements can take too much time. Thus

an optimization procedure is necessary in this thesis work, to minimize the optimization time.

3.3.1 Optimizer Algorithm Selection

Optim tool has been discussed before in this work, i.e. goal definitions, schematic,…etc. One important prorperty of this tool is that it enables the user to select from different types of optimization topologies. In ADS2006, Optim tool has the following optimization topologies enabled.

- Random
- Gradient
- Random Minimax
- Gradient Minimax
- Quasi-Newton
- Least Pth
- Minimax
- Random Max
- Hybrid
- Discrete
- Genetic

Random, random minimax and random max algorithms use random optimization with different error function definitions. Random uses Least Squares error function as Random Minimax makes use of minimax L1 error function. On the other hand Random Max uses the Negated-Least Squares error function. The same difference exists between Gradient and Gradient Minimax and between Quasi-Newton and Least Pth. Hybrid optimizer uses random and Quasi-Newton optimizers together. Discrete optimizer uses Exhaustive Search Method where optimizer makes a comprehensive search for the combination of elements that gives the best performance. Genetic algorithms also provide a direct search method. Detailed information for optimizers is not provided in this work. Interested reader can find extensive study on [21].

For this work, all of the optimizer types are compared with the results obtained and optimization time. Optimizing the whole circuit with each type of optimizer would take too much time, thus one of the amplifying paths is used for comparison. It is observed that Gradient optimizer gives the best result in a reasonable time. For this work, Gradient optimizer is selected as the base optimizer for all of the optimization process.

3.3.2 Optimization Procedure

Elements of the amplifying paths would be a burden on the optimizer; thus in order to obtain an easier process, elements to be optimized is divided into groups. First channel one amplifying path elements are collected as a group, Group 1. Same as channel one, channel two elements are separated as Group 2, as channel three elements are grouped as Group 3. Flow chart shown in Figure 3-19 helps to explain the process in detail.

Firstly, goal definitions for the whole circuit are defined for transmission (S_{21}) and return losses (S_{11}, S_{22}). Gain (dB(S(2,1))) is set to be higher than 18 dB, whereas return losses are expected to be lower than -10 dB. For the whole optimization process, these definitions are chosen. After defining goals, Group 1 is optimized for 10 iterations maximum. Then Group 2 is optimized again with the same number of iterations. After Group 3 is optimized for the same number of iterations, loop starts from the beginning. Optimization process gets out of this cycle whenever it reaches the zero error for all of the goal definitions. At the end of the process, element values are updated.

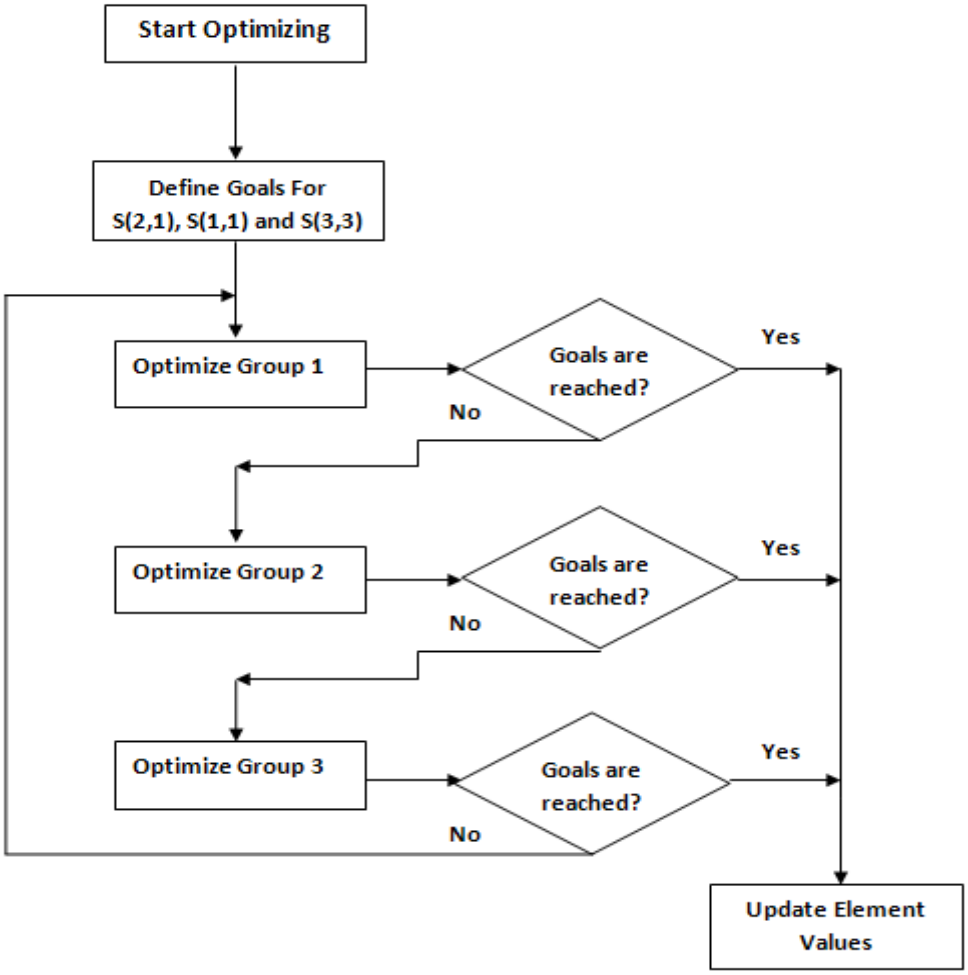


Figure 3-19 Optimization procedure

This process definition helps to minimize the optimization time. And also good results are obtained where brute force optimization (all elements are optimized at once) is not able to reach.

3.4 Schematic of the Proposed Amplifier

Figure 3-20 shows the whole circuit schematic of the proposed amplifier in detail. Input is applied to port 1, and then the de-multiplexer divides the signal into bands. Middle part is the amplifying path. Amplified signals are combined by the multiplexer at the end.

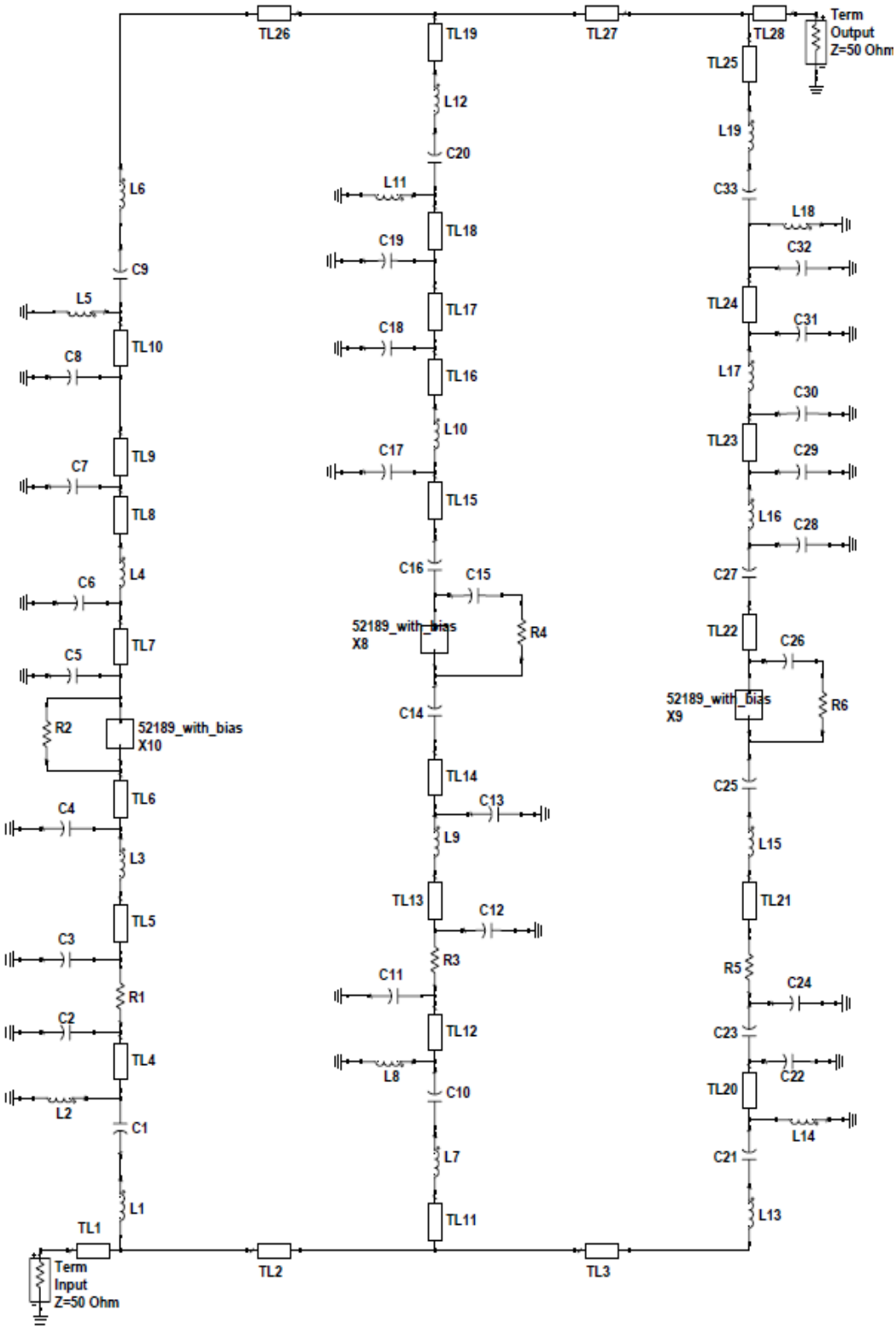


Figure 3-20 Schematic of three channel 0.1-1 GHz amplifier

The component values are given in Table 3-4 and Table 3-5. As can be realized from the circuit, there are transmission lines with different lengths. Obviously there should be a physical separation between channels and these transmission lines in the de-multiplexer and multiplexer provide this separation and corresponding lengths are not of optimization variables. On the other hand the transmission lines in the amplifying paths provide separation and play a role in the matching. As mentioned earlier, phase synchronization should be obtained for a proper constructive summation at the output. This phase synchronization is provided in the amplifying paths section where these transmission lines and lumped elements are optimized together to achieve the defined goals. The limit for the lengths of the transmission lines in optimization is kept at 2mm. A larger limit may cause complicated optimization, whereas a lower limit would not affect phase too much.

During measurement stage, it is observed that de-multiplexer and amplifying paths present mismatches to each other. This affects both the gain and the return losses for the whole amplifier. In order to have a better inter-stage match, small resistors are placed between de-multiplexer and amplifying paths.

Simulation results are given in Figures 3-21, 3-22 and 3-23. Figure 3-21 shows S(2,1) in dB where gain is around 17 dB. Return losses are less than 9 dB; however as can be observed a slight increase in the return loss is observed for S(2,2), which may be recovered with further optimization.

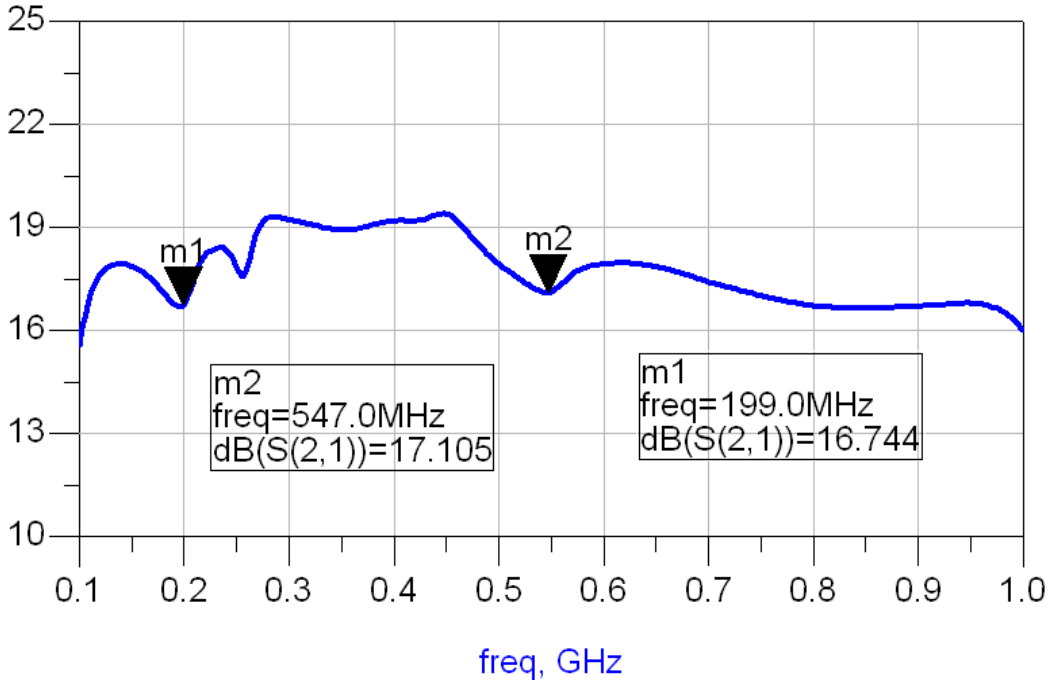


Figure 3-21 Simulated gain results for 0.1-1 GHz amplifier

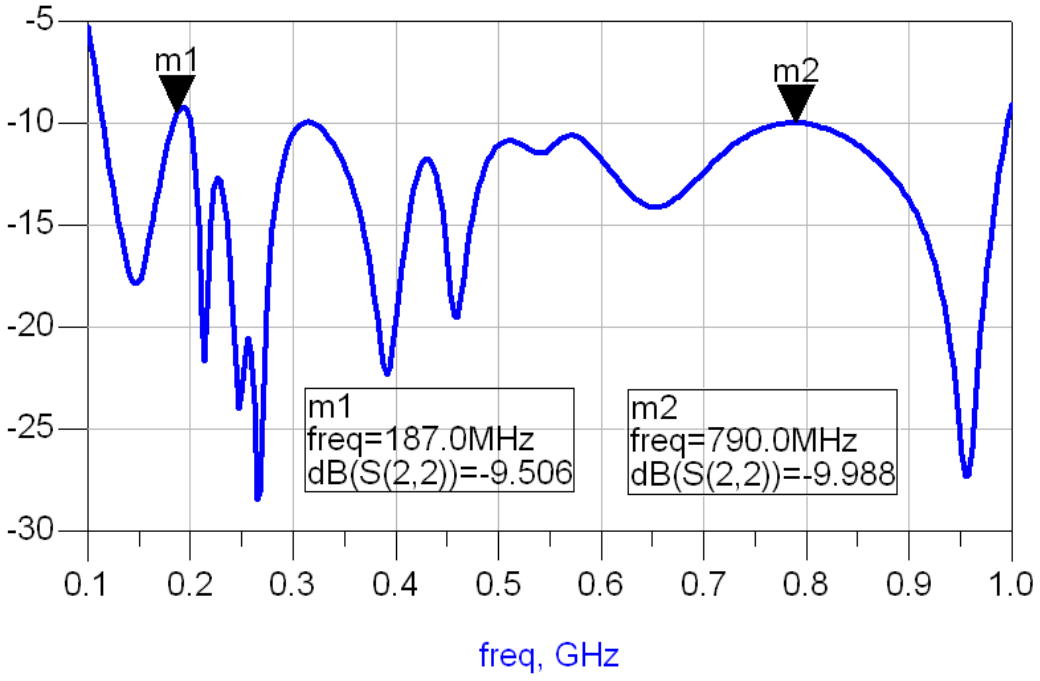


Figure 3-22 Simulated output return loss for 0.1-1 GHz amplifier

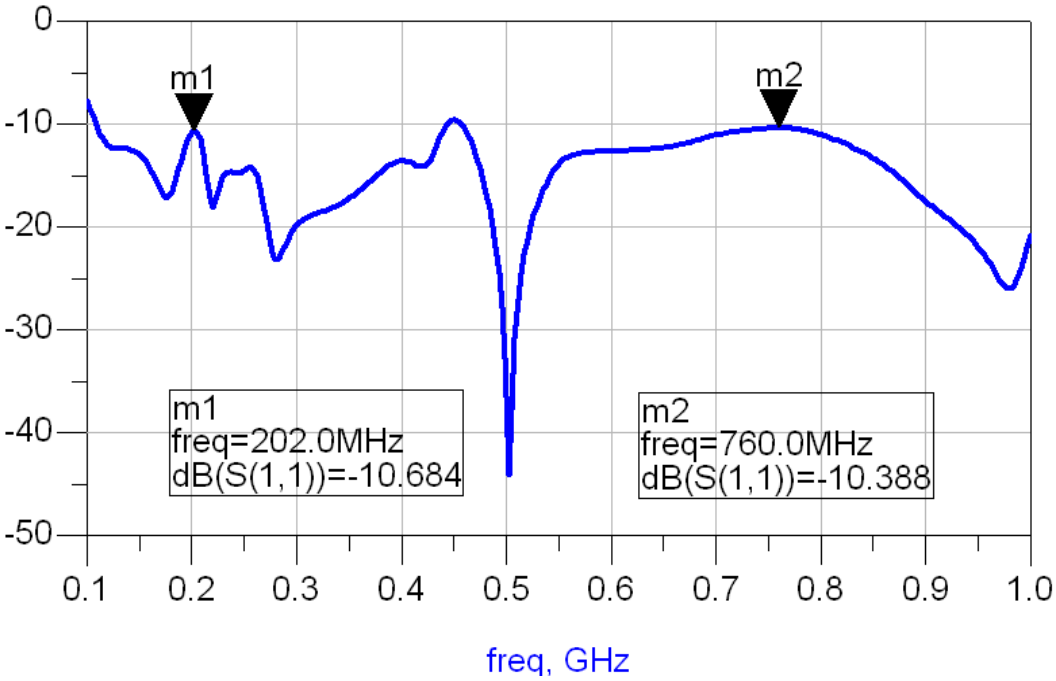


Figure 3-23 Simulated input return loss for 0.1-1 GHz amplifier

3.5 Layout Generation and Fabrication

The work in the simulation phase is enough for a layout generation and actual trials. Thus a layout is generated and a PCB is created. As the dielectric for PCB, Hi-Tg, FR4 which has a dielectric constant of 4.3, is selected. The transmission lines used in the simulations all have the property of this dielectric. Transmission lines in the simulation uses MSub1 element for characterization, which defines the dielectric coefficient, dielectric loss, substrate height, conductor loss and height. Thus the PCB layer heights are already known as well as the conductor heights. The generated layout is shown in Figure 3-24 which is fabricated in ASELSAN Inc.'s factory.

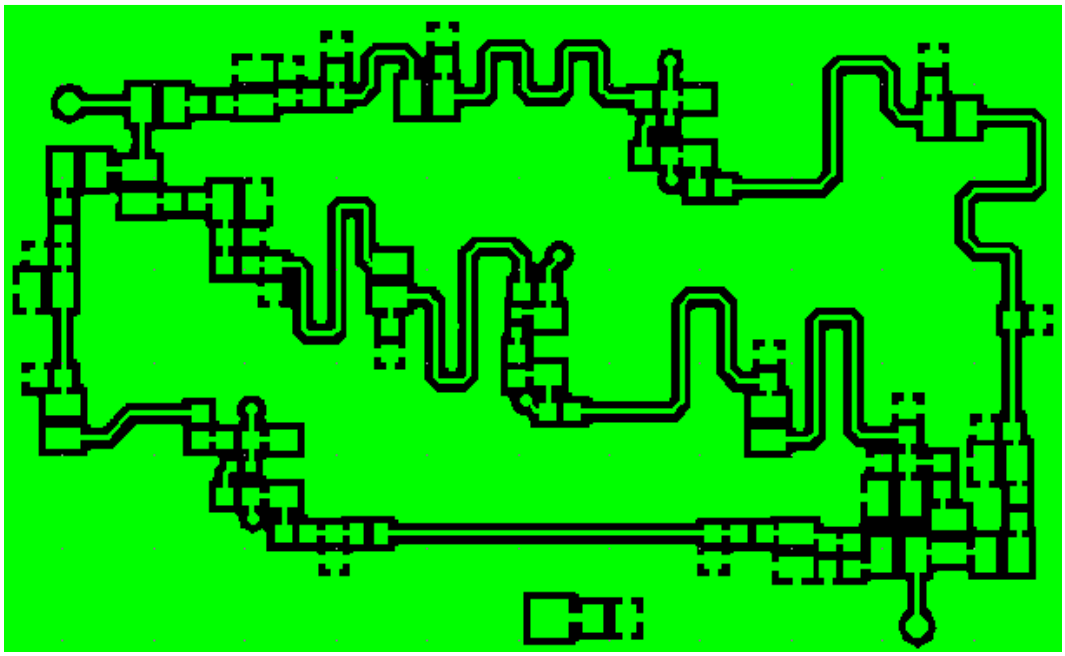


Figure 3-24 Layout for the 0.1-1 GHz amplifier

The resultant PCB is shown in Figure 3-25. As shown, the PCB board has dimensions 6.5x3.5 cm with a total board thickness of 0.5 cm.

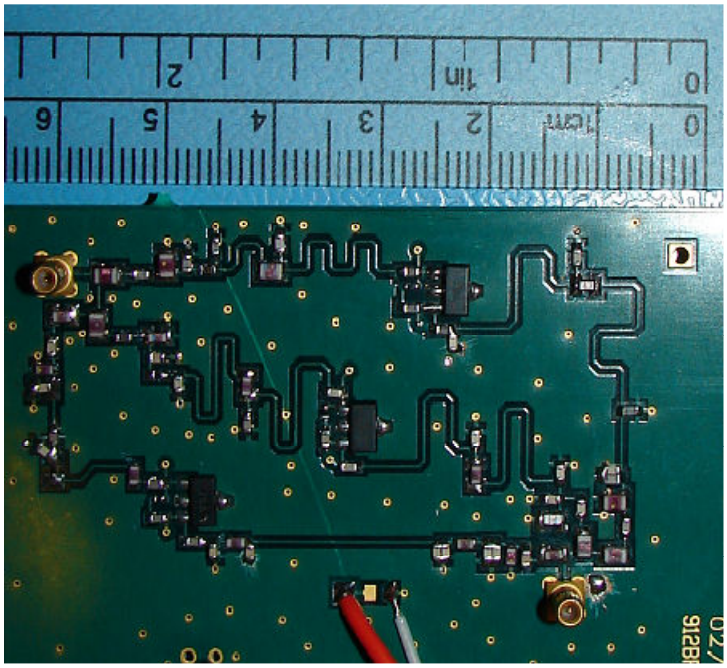


Figure 3-25 Fabricated 0.1-1 GHz amplifier

3.6 Test Set-Up

Figure 3-26 shows the test set-up used to measure S-parameters of the proposed design. Agilent's N5230A network analyzer is used to measure S-parameters. For the DC supply, Agilent's E3633A is preferred.

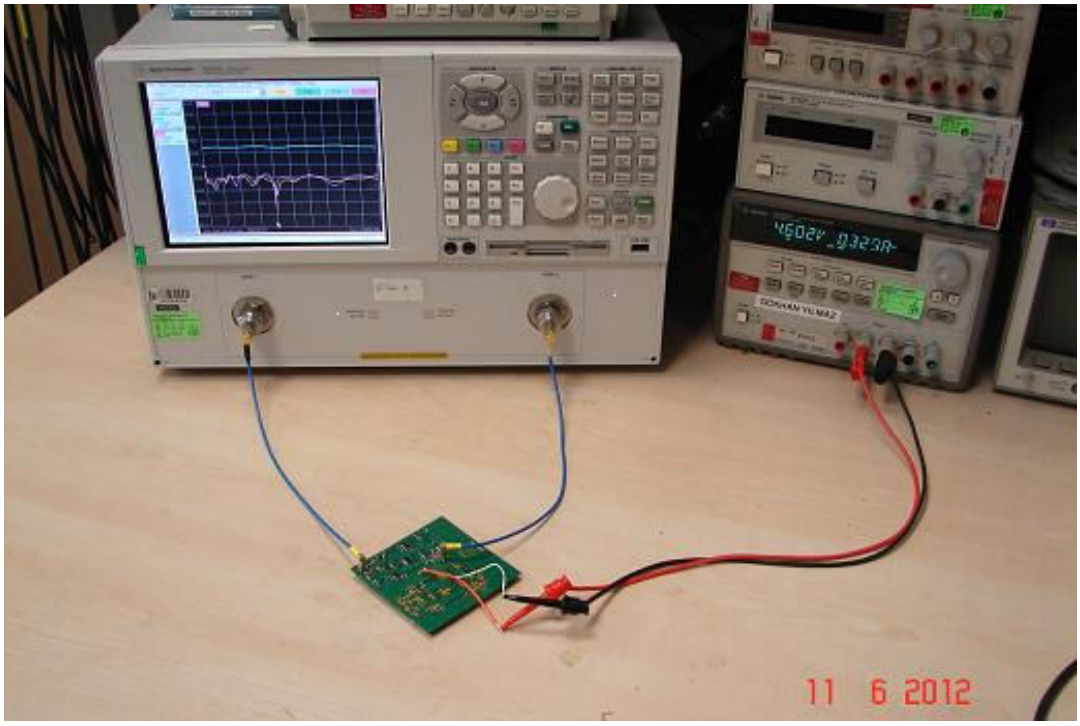


Figure 3-26 Measurement test set-up

After layout and PCB generation, components are placed on the board with a soldering process. The resultant circuit is shown in Figure 3-25. Two cables are required for the supply connections and RF ports are connected with SSMB connectors. Two SSMB-to-SMA cables are necessary in order to connect the circuit to network analyzer.

3.7 Measurement

Since there are cable losses for this set-up, a short-open-load-through (SOLT) calibration is performed for the whole frequency range (0.1 to 1 GHz). A calibration

for the 0.1 to 4 GHz measurement could not be performed since it is a very wide bandwidth that requires special calibration components. Since frequency band from 1 to 4 GHz is taken as out of band, un-calibrated 4 GHz measurements provide sufficient insight. Starting with de-multiplexer, results will be shown in this chapter with comparisons to the simulated versions.

3.7.1 De-multiplexer and Multiplexer Results

De-multiplexer consists of simple lumped elements with finite Q values. Even though scheme is simple, due to modeling errors and parasitic at higher frequencies cause a mismatch between the simulation and measured results. This mismatch is overcome by manually adjusting the component values on board. Table 3-4 highlights the change in element values after optimization.

Table 3-4 De-multiplexer and multiplexer element values

Component Value	Simulation	Optimized (on board)
L1	68 nH	68 nH
C1	33 pF	22 pF
L2	43 nH	43 nH
C2	27 pF	27 pF
L7	39.5 nH	33 nH
C10	5.9 pF	6.2 pF
L8	16 nH	18 nH
C11	17 pF	12 pF
L13	10.5 nH	11 nH
C21	3.9 pF	3 pF
L14	8 nH	12 nH
C22	4.3 pF	1 pF

After this manual optimization, simulated and measured results are compared. Figure 3-27 indicates the results for return loss at the input port.

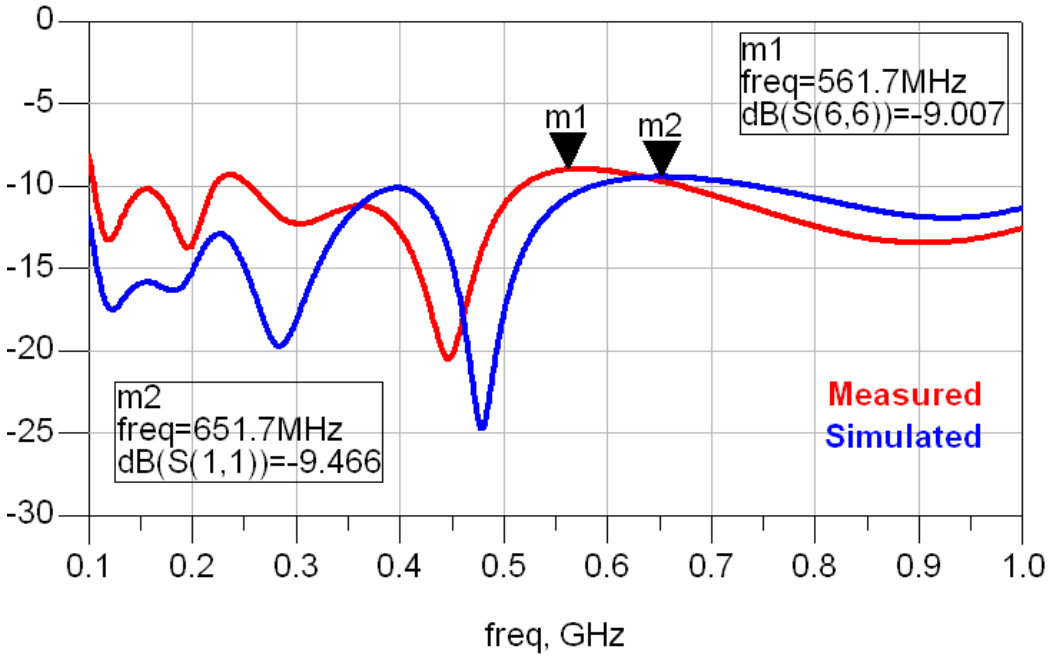


Figure 3-27 Measured and simulated input return losses for de-multiplexer

Result for input return loss shows good agreement except that the notch in the middle is shifted towards left. Then the results for first channel are presented in Figures 3-28 and 3-29.

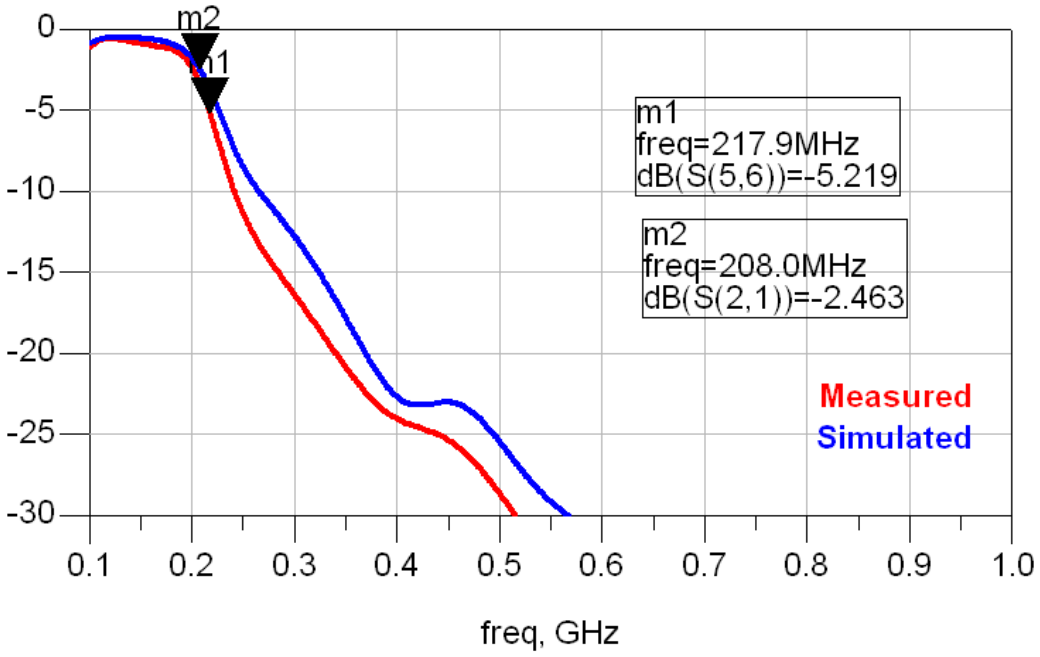


Figure 3-28 Measured and simulated insertion losses for channel 1

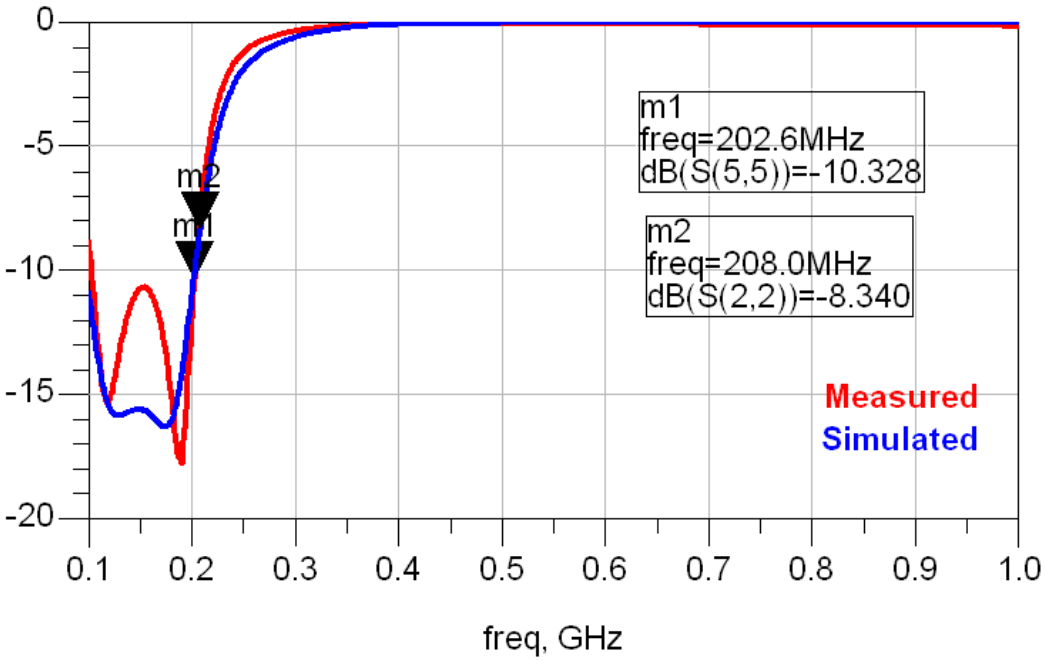


Figure 3-29 Measured and simulated output return losses for channel 1

Since first channel operates at the low frequency part of the amplifier, parasitics do not affect the results. Second channel measured results are also consistent with the simulated results as depicted in Figures 3-30 and 3-31.

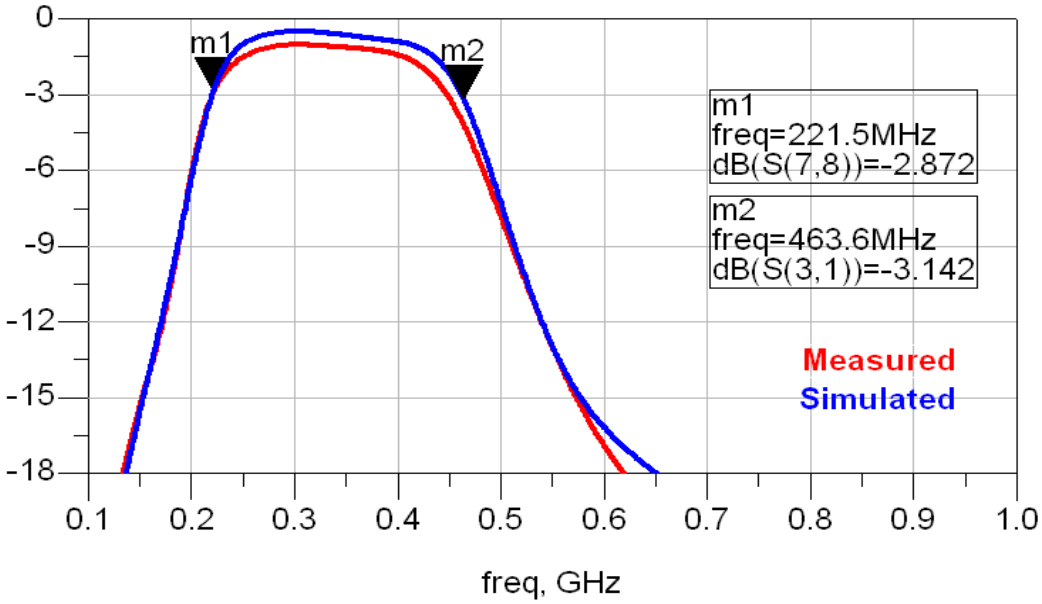


Figure 3-30 Measured and simulated insertion losses for channel 2

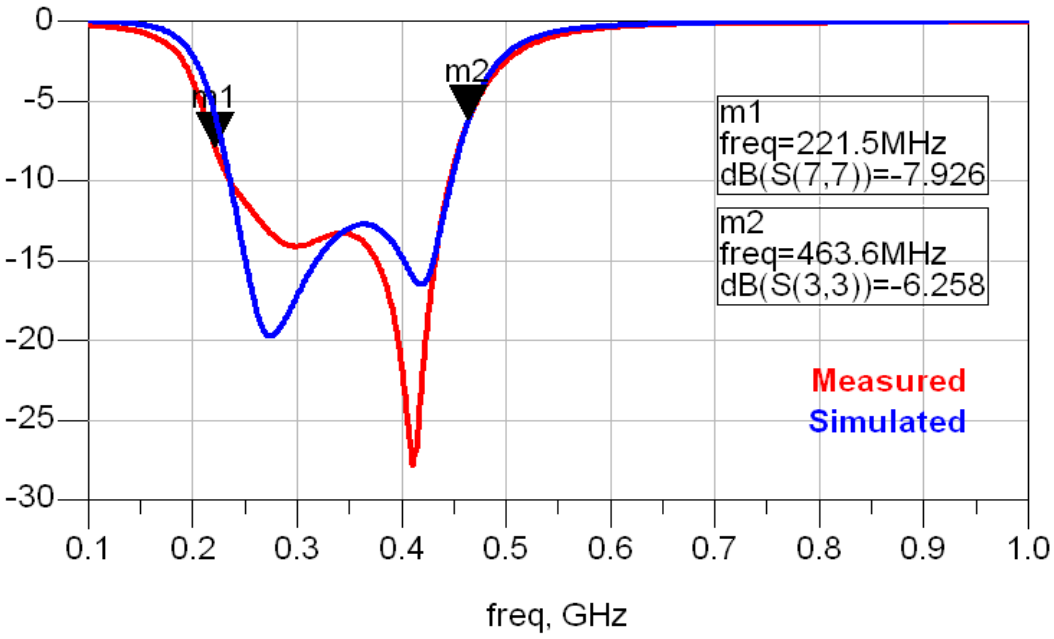


Figure 3-31 Measured and simulated output return losses for channel 2

Insertion loss graph for channel two indicates that more loss is associated with measured results than the simulated ones. However this loss is small and can be neglected. Third channel results are similar to the first and the second channels as can be observed from Figures 3-32 and 3-33.

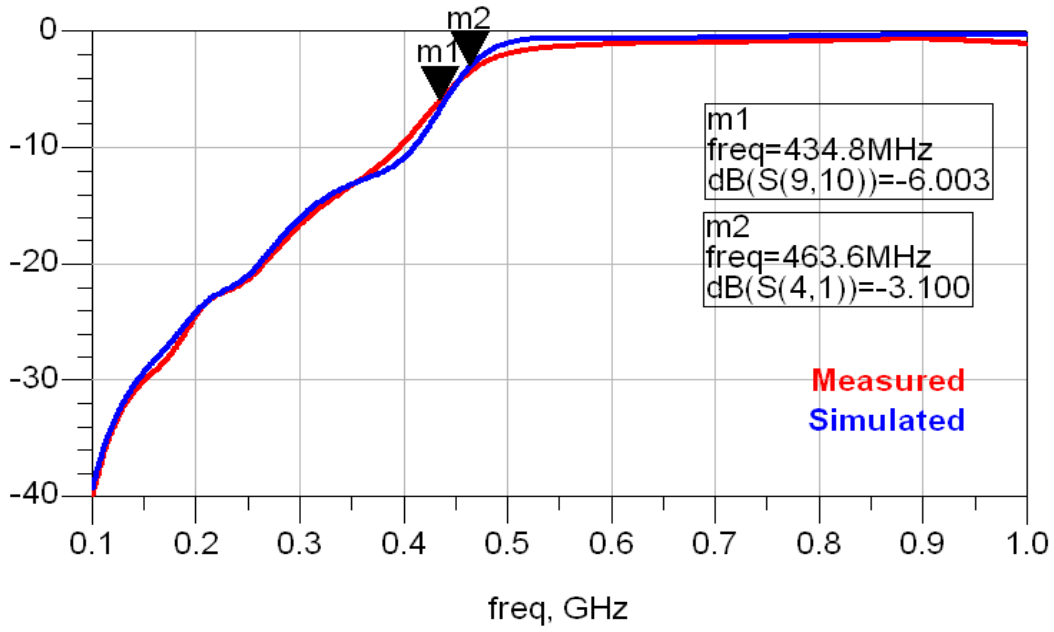


Figure 3-32 Measured and simulated insertion losses for channel 3

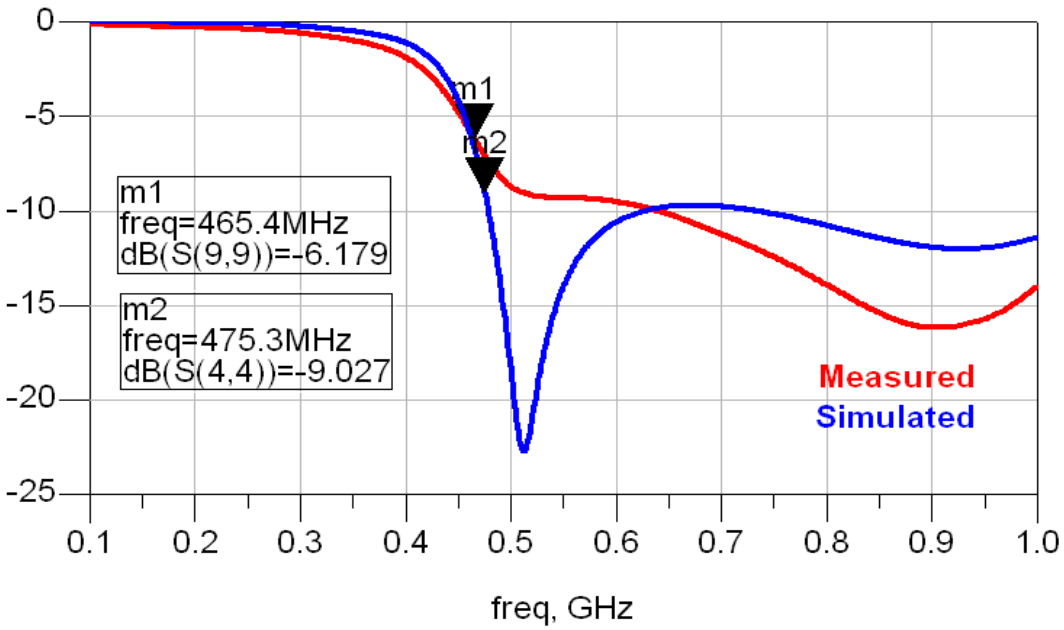


Figure 3-33 Measured and simulated output return losses for channel 3

Third channel return loss shows a little bit different characteristic than the simulated one. Notch in the simulated version is not observed at the same level for the measurements. As frequency gets higher, it becomes harder to fit simulation and measurement results. This statement can be based on parasitic contribution at high frequencies and modeling inaccuracies.

3.7.2 Amplifying Path Results

Figures 3-34 to 3-42 show the measured results and simulation results together of each amplifying path. Figure 3-34 depicts gain comparison for the first channel. As S(2,1) depicts simulated, S(4,3) indicates measured results.

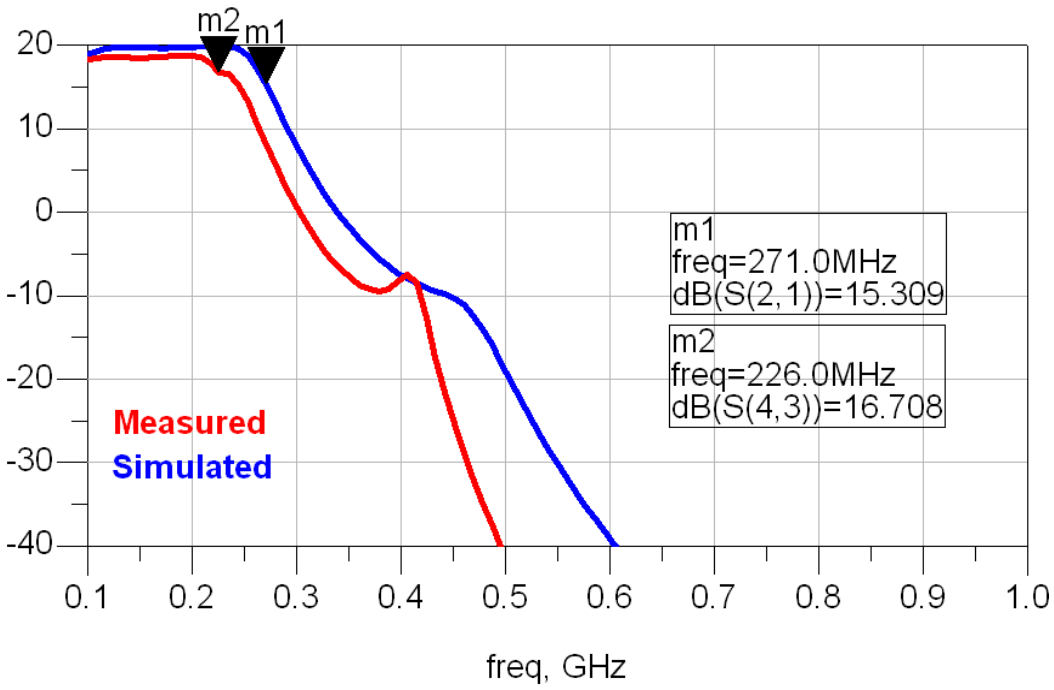


Figure 3-34 Measured and simulated amplifying path gain for channel 1

Comparison between simulated and measurement results shows very good agreement except the small slide of the frequency characteristics.

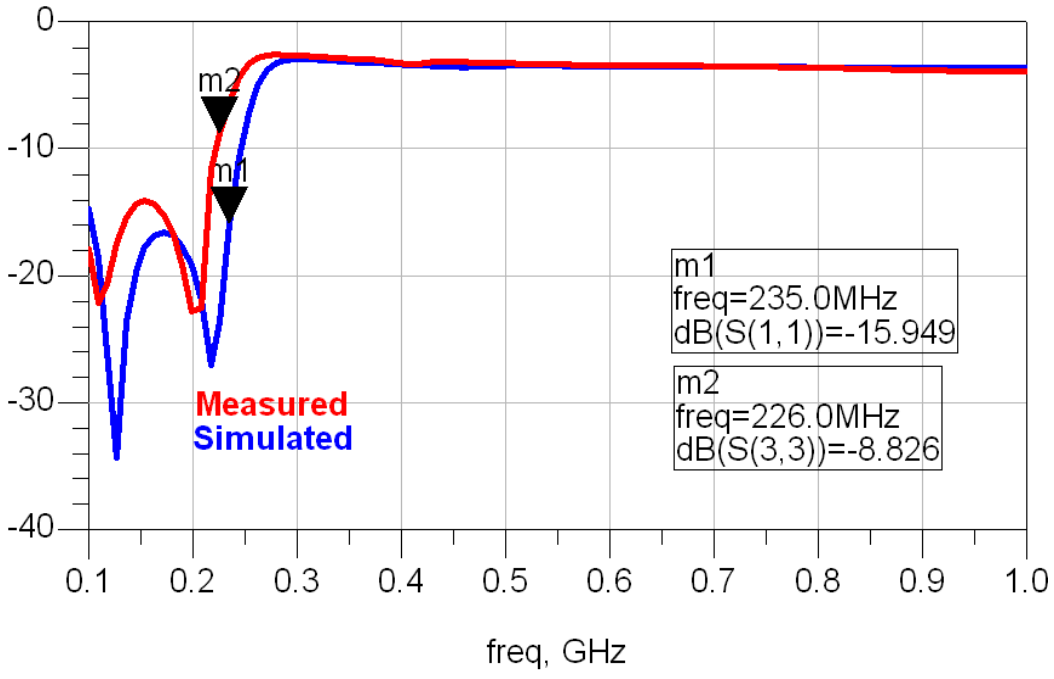


Figure 3-35 Measured and simulated amplifying path input return losses for channel 1

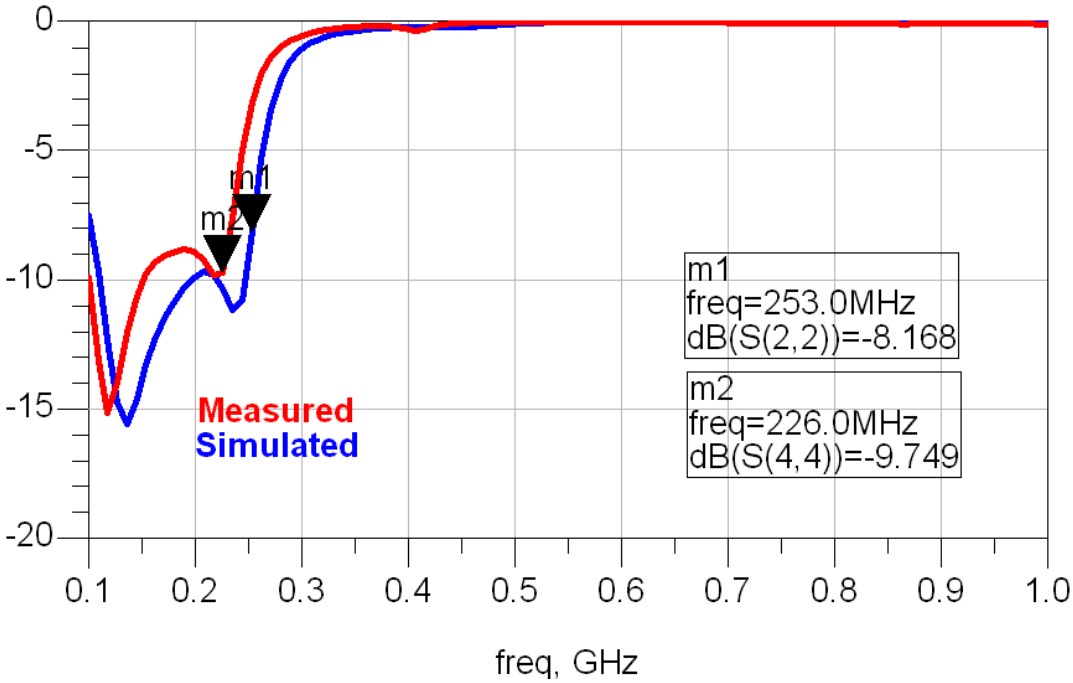


Figure 3-36 Measured and simulated amplifying path output return losses for channel 1

Second channel responses are given in Figures 3-37, 3-38 and 3-39. As graphs indicate, gain response fits very well. On the other hand there are some notches in the return loss graphs that are not similar to the simulated results. Overall performance is not affected by this fact, as will be seen in overall circuit design.

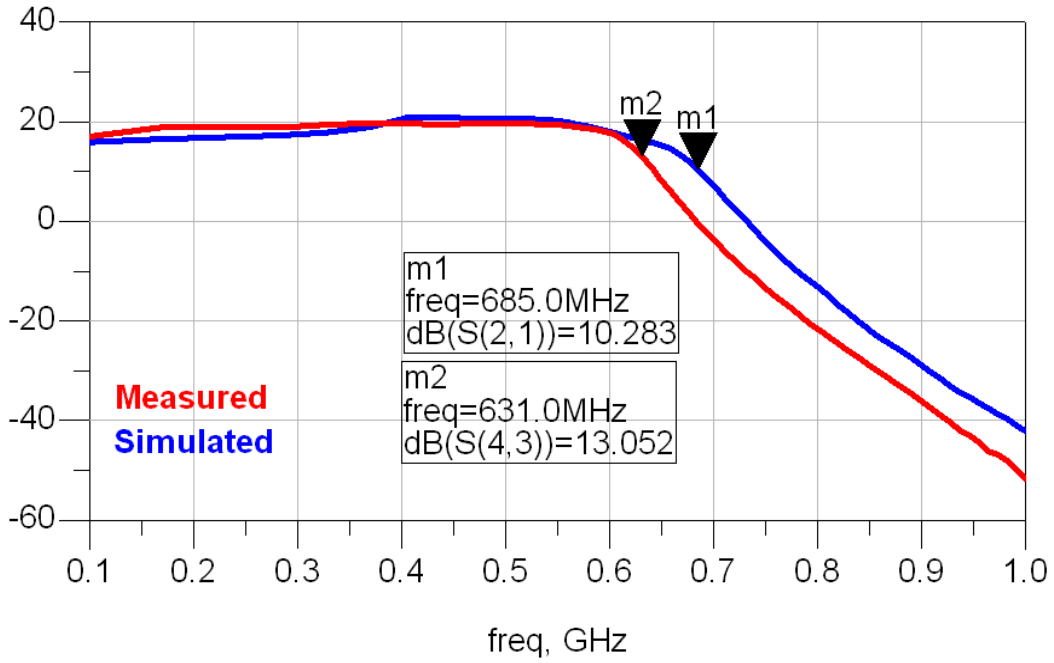


Figure 3-37 Measured and simulated amplifying path gain for channel 2

As input return loss graph shows, there is a notch at around 200 MHz where simulated version does not have. The same is also true for output return loss response.

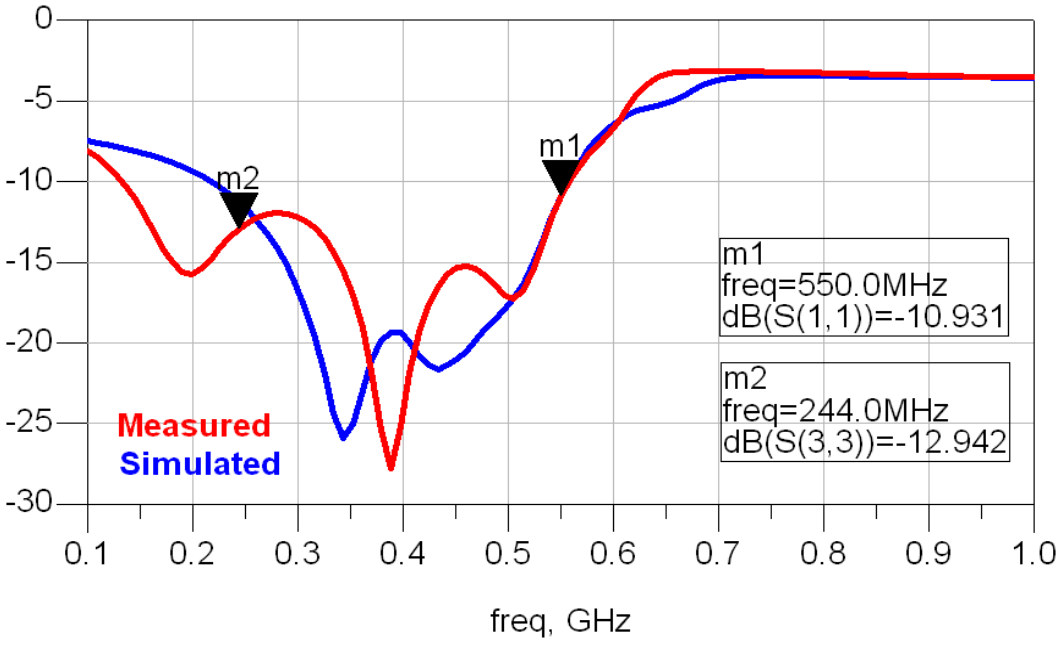


Figure 3-38 Measured and simulated amplifying path input return losses for channel 2

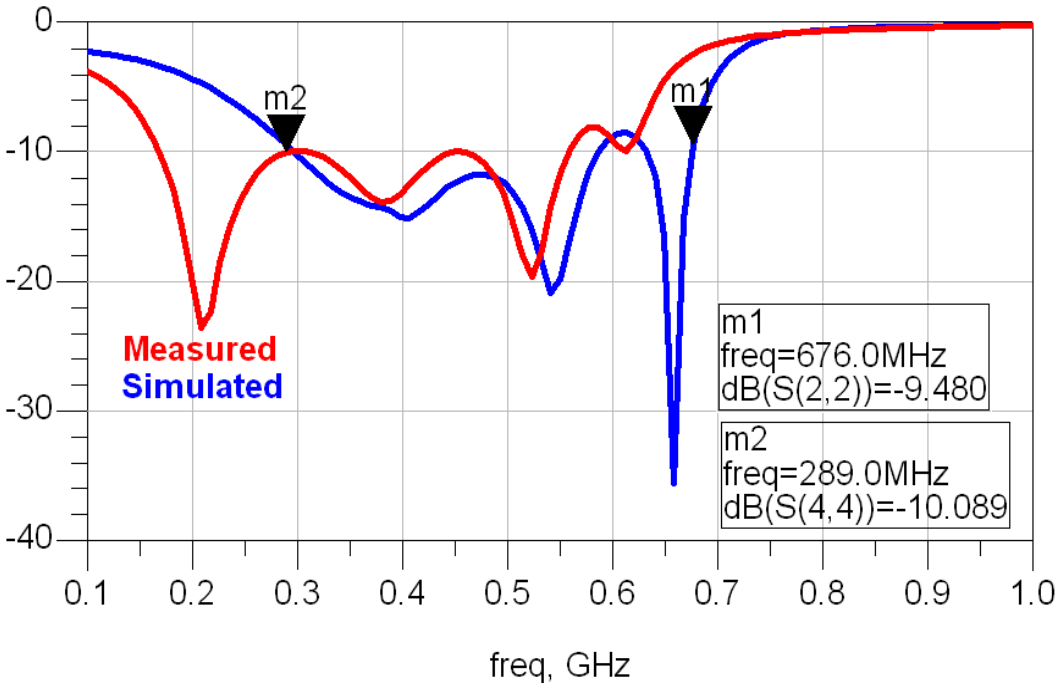


Figure 3-39 Measured and simulated amplifying path output return losses for channel 2

Third channel simulated and measured results are shown in Figures 3-40, 3-41 and 3-42.

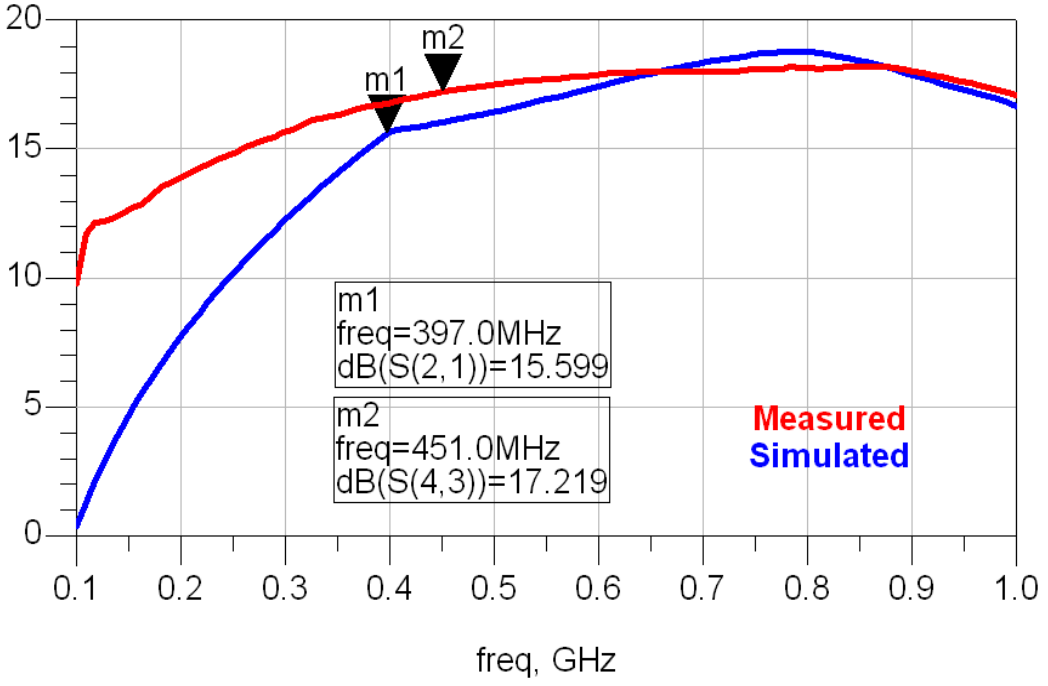


Figure 3-40 Measured and simulated amplifying path gain for channel 3

Extracted gain response again depicts similar results for measured and simulated third channel behavior. Gain graph is similar, whereas return loss results differ a little.

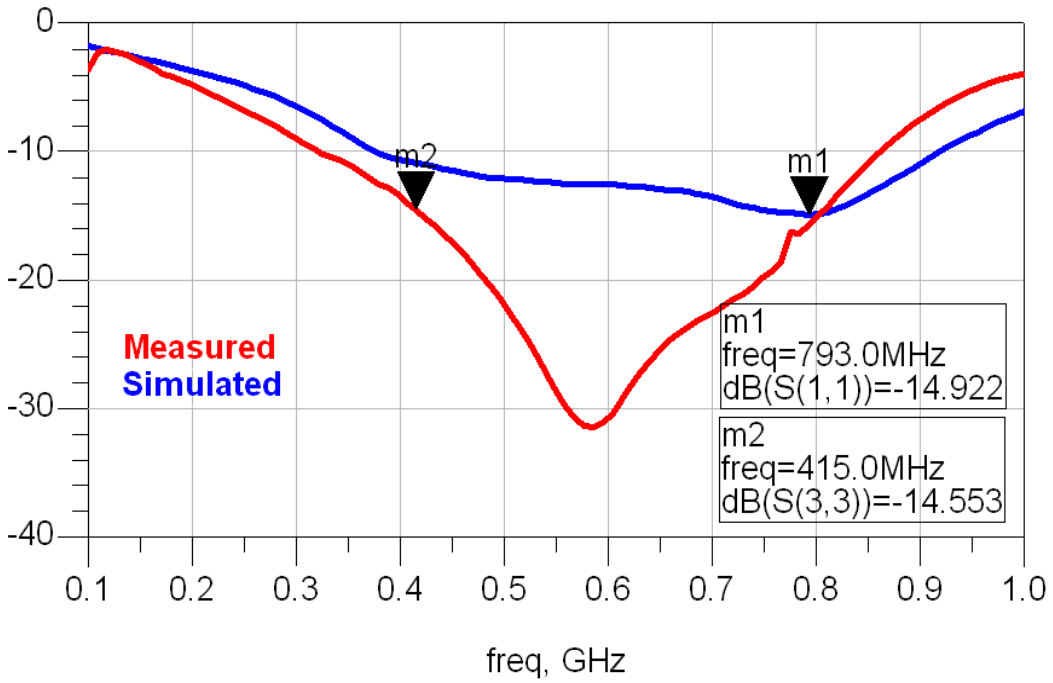


Figure 3-41 Measured and simulated amplifying path input return losses for channel 2

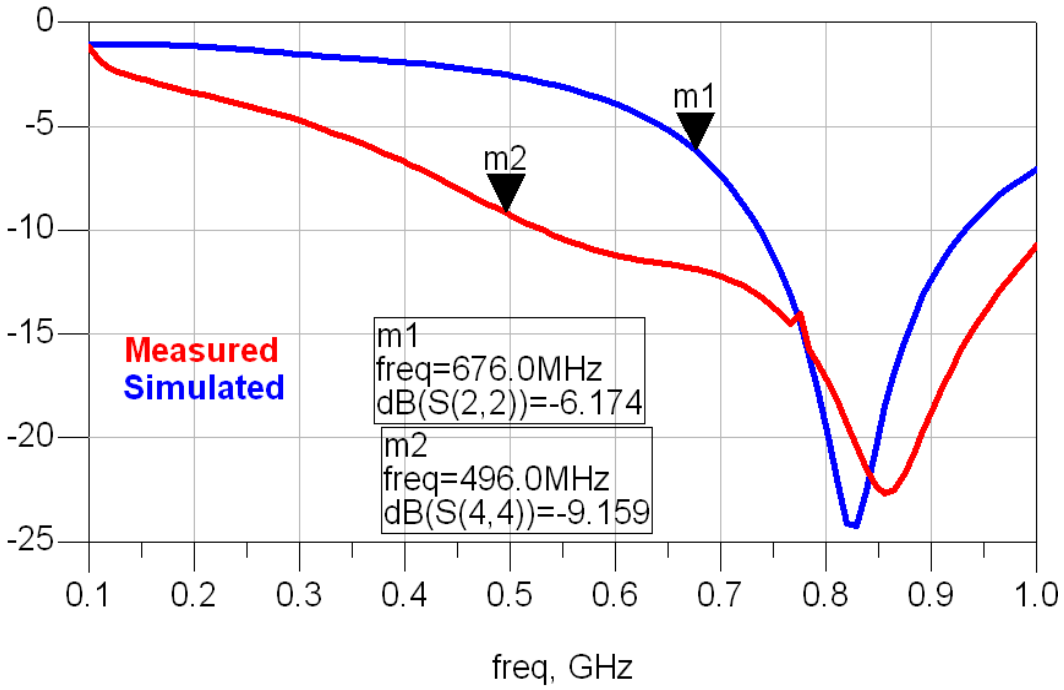


Figure 3-42 Measured and simulated amplifying path output return losses for channel 2

3.7.3 Overall Circuit Response

All of the results above show comparisons for the parts of the amplifier. After obtaining these results, sections are combined for the whole circuit response. After combining the sections, modifications are performed to obtain the desired result. Table 3-5 displays element values for simulated version and values for actual circuit. As can be seen from the table, circuit elements have a reasonable shift from the simulated values.

Table 3-5 Amplifying path element values (simulated and optimized versions)

Element	Simulation	Measurement	Element	Simulation	Measurement
1st Channel			TL15	20 mm	20 mm
R1	22 Ohm	22 Ohm	C17	18.5 pF	5.6 pF
C3	27 pF	27 pF	L10	7.5 nH	7.5 nH
TL5	7.5 mm	7.5 mm	TL16	20 mm	20 mm
L3	22 nH	22 nH	C18	10 pF	5.6 pF
C4	47 pF	47 pF	TL17	0.2 mm	0.2 mm
TL6	20 mm	20 mm	**3rd Channel**		
R2	220 Ohm	220 Ohm	C23	22 pF	22 pF
C5	2.2 pF	2.2 pF	C24	2.47 pF	0.75 pF
TL7	20 mm	20 mm	R5	22 Ohm	22 Ohm
C6	39 pF	56 pF	TL21	7.7 mm	7.7 mm
L4	27 nH	27 nH	L15	3.3 nH	3.9 nH
TL8	20 mm	20 mm	C25	82 pF	82 pF
C7	18 pF	18 pF	R6	270 Ohm	270 Ohm
TL9	5 mm	5 mm	C26	120 pF	120 pF
2nd Channel			TL22	0.1 mm	0.1 mm
R3	22 Ohm	22 Ohm	C27	82 pF	82 pF
C12	9.6 pF	10 pF	C28	17 pF	10 pF
TL13	20 mm	20 mm	L16	1.2 nH	3.3 nH
L9	0.5 nH	4.7 nH	C29	1.8 pF	1.8 pF
C13	13.2 pF	22 pF	TL23	17.5 mm	17.5 mm
TL14	20 mm	20 mm	C30	10.4 pF	4.3 pF
C14	200 pF	220 pF	L17	8.4 nH	11 nH
R4	270 Ohm	270 Ohm	C31	6.4 pF	3 pF
C15	220 pF	220 pF	TL24	0.1 mm	0.1 mm
C16	220 pF	220 pF			

Figures 3-43, 3-44 and 3-45 compare the simulated and measured results for the whole amplifier. As can be observed from these figures, a 0.1 to 1 GHz amplifier with 14-15 dB gain is obtained with this topology. Maximum return loss of -7.7 dB for output and maximum return loss of -8 dB for input is observed.

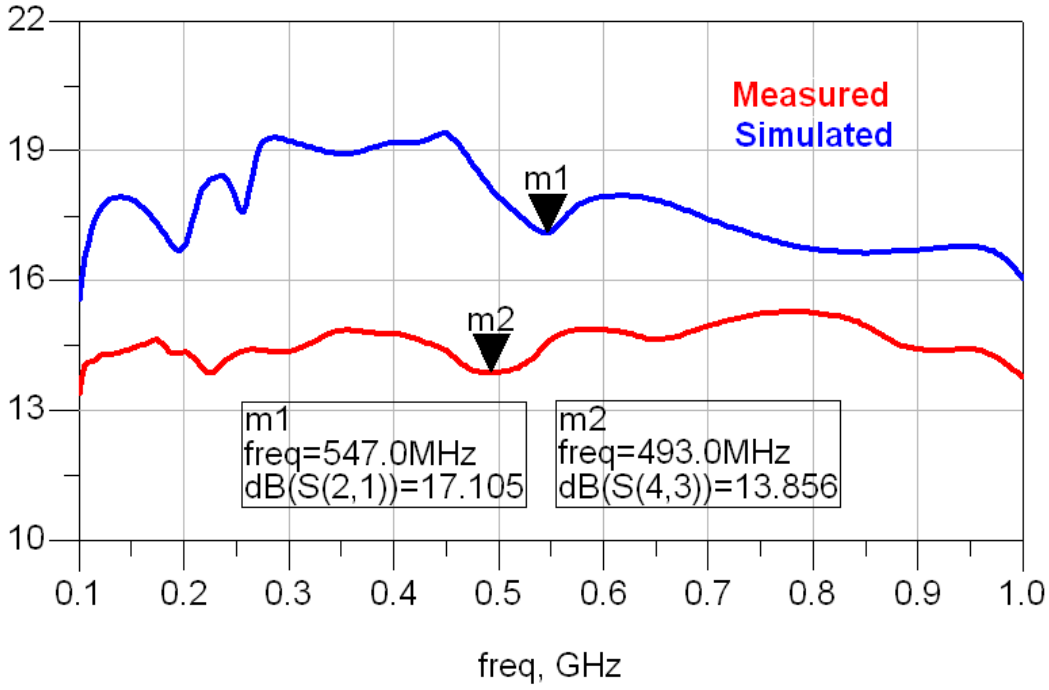


Figure 3-43 0.1-1 GHz whole circuit gain response

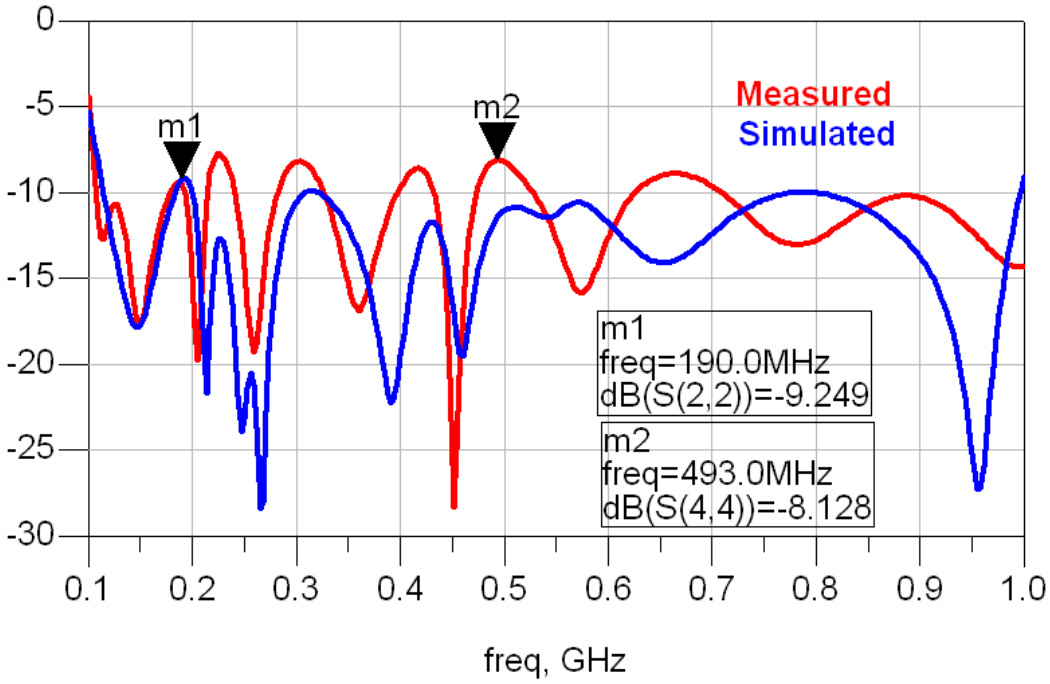


Figure 3-44 0.1-1 GHz whole circuit output return loss

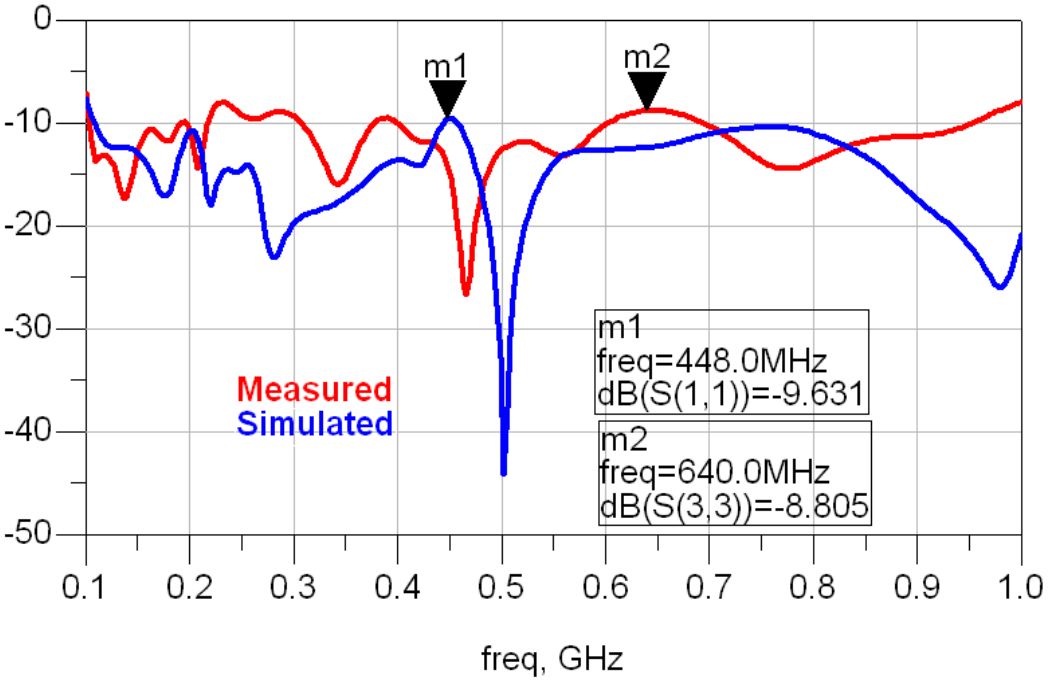


Figure 3-45 0.1-1 GHz whole circuit output return loss

Figure 3-43 depicts a decrease in gain which may be a result of the model inaccuracies and parasitics associated with the elements. Model accuracy becomes very important especially when a non-linear component is employed. An inaccurate model may lead to poor matching and thus poor efficiency and gain results. Parasitics at these frequency ranges may not have crucial impact; however they should be taken into account.

Whole circuit response is observed for 0.1 to 4 GHz. However due to the lack of the proper material for 4 GHz calibration, measurements are done without calibration. Figures 3-46, 3-47 and 3-48 display the results for 0.1 to 4 GHz.

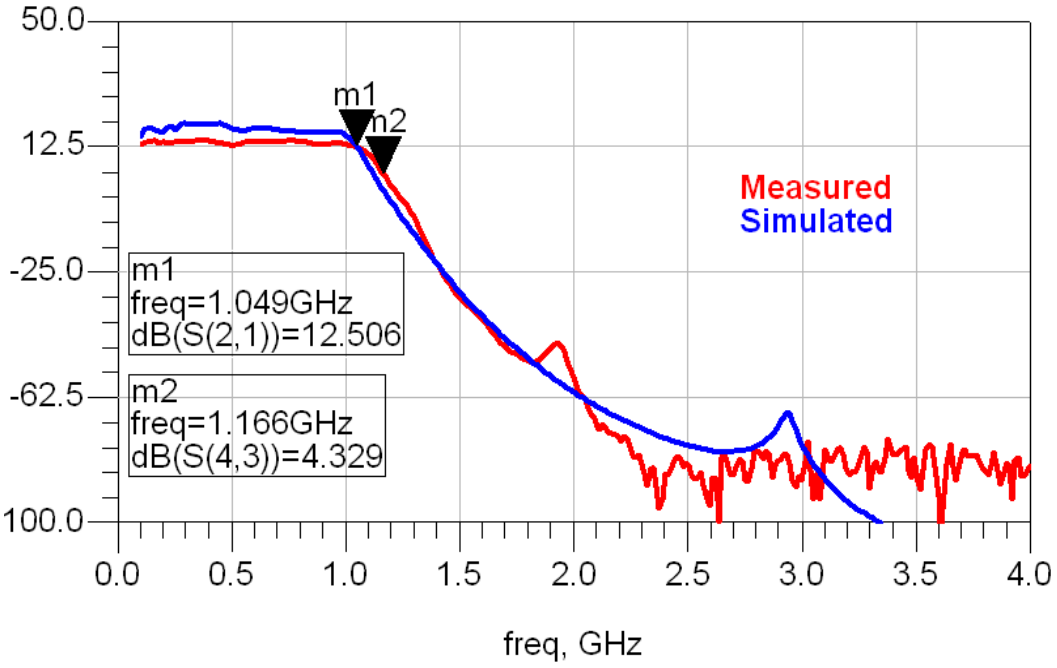


Figure 3-46 Gain response for 4 GHz

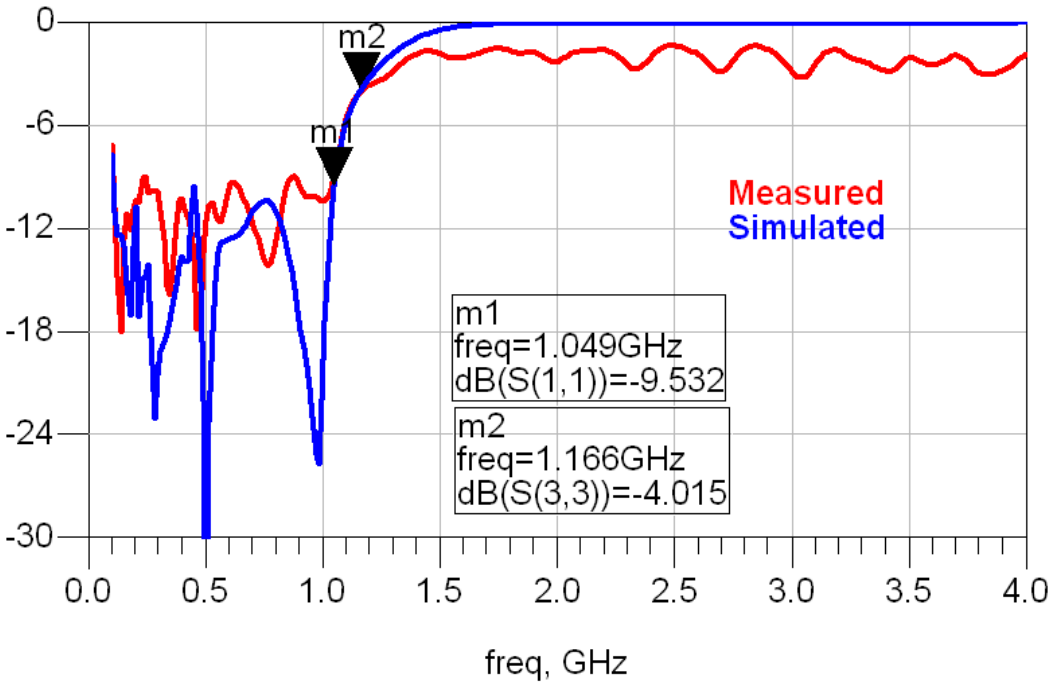


Figure 3-47 Input return loss for 4 GHz

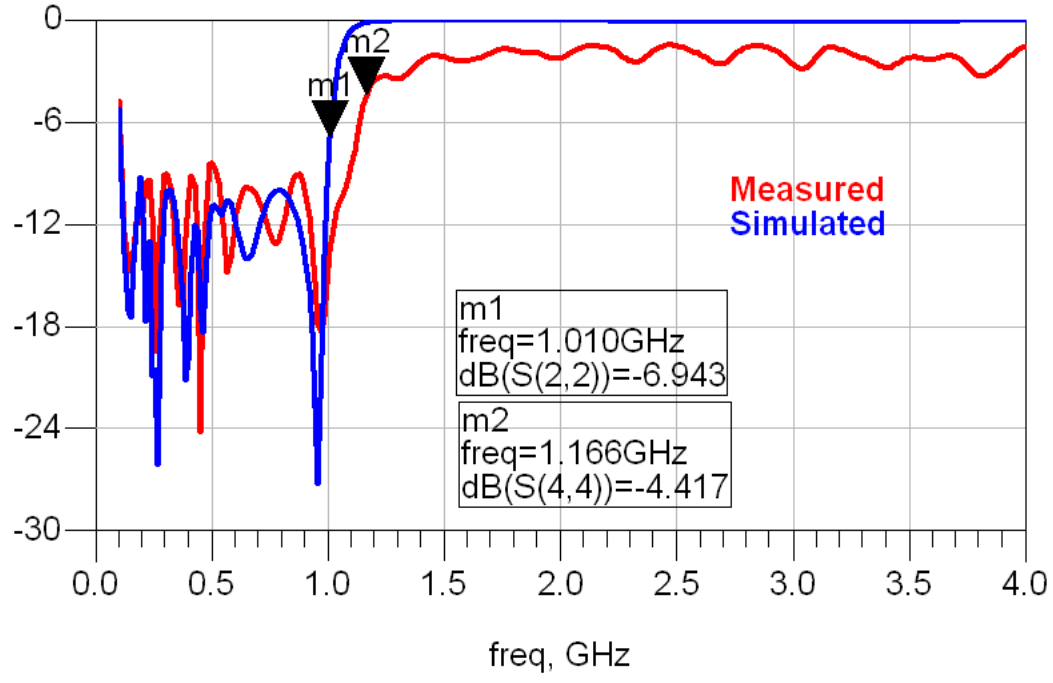


Figure 3-48 Output return loss for 4 GHz

Figure 3-49 displays output power versus input power graph. The fabricated amplifier has a saturated output power of 25 dBm.

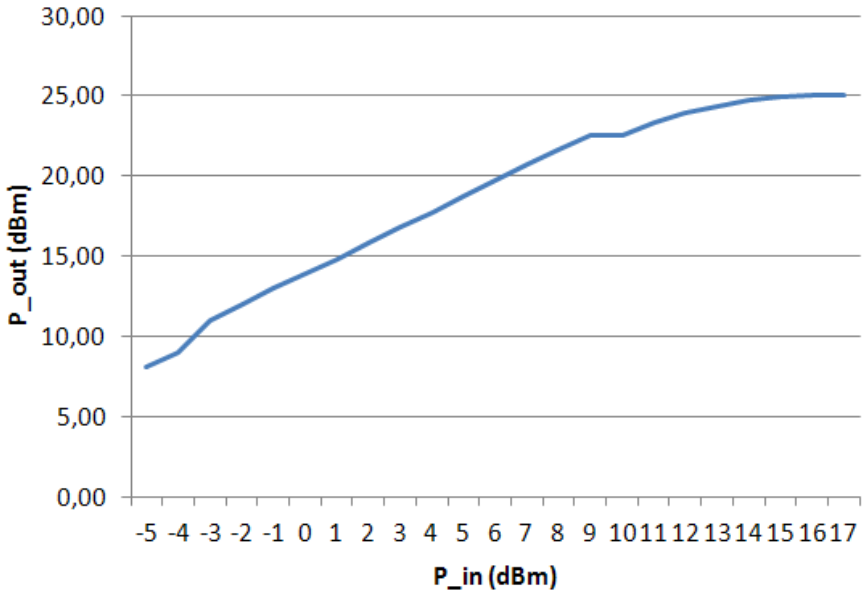


Figure 3-49 P_out vs P_in curve for three channel amplifier

Phase characteristic of an amplifier is important for application that requires linear amplification. Figure 3-50 displays phase response of the amplifier for the frequency spectrum of interest.

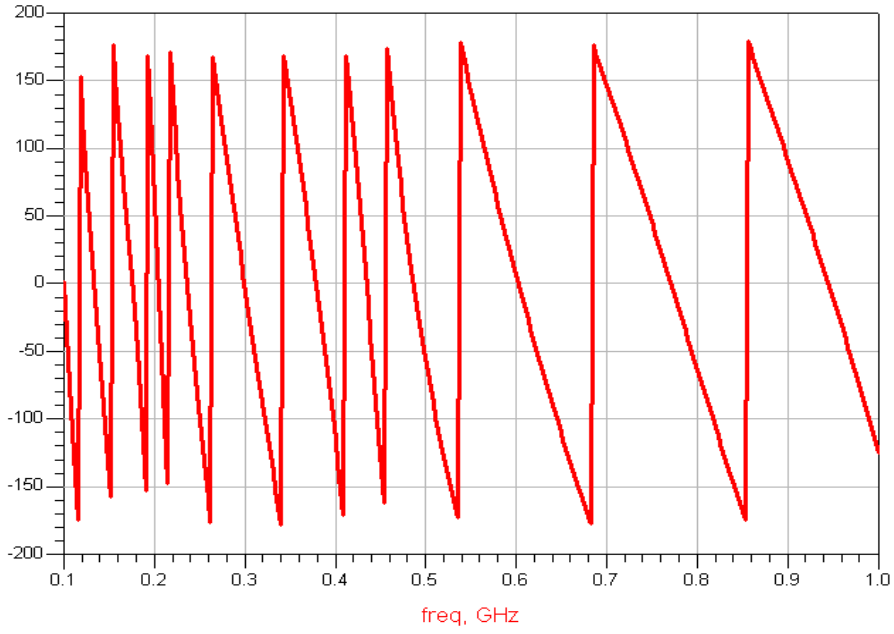


Figure 3- 50 Phase response of the three channel amplifier

After observing amplifier performance alone, another prototype is created based on the same elements. Then these amplifiers are cascaded and results are measured on the same set-up. Since transistor enters compression above 0 dB input power, a -15 dB input power is applied to the cascaded amplifier for non-compressed operation. Results are depicted in Figures 3-51, 3-52 and 3-53.

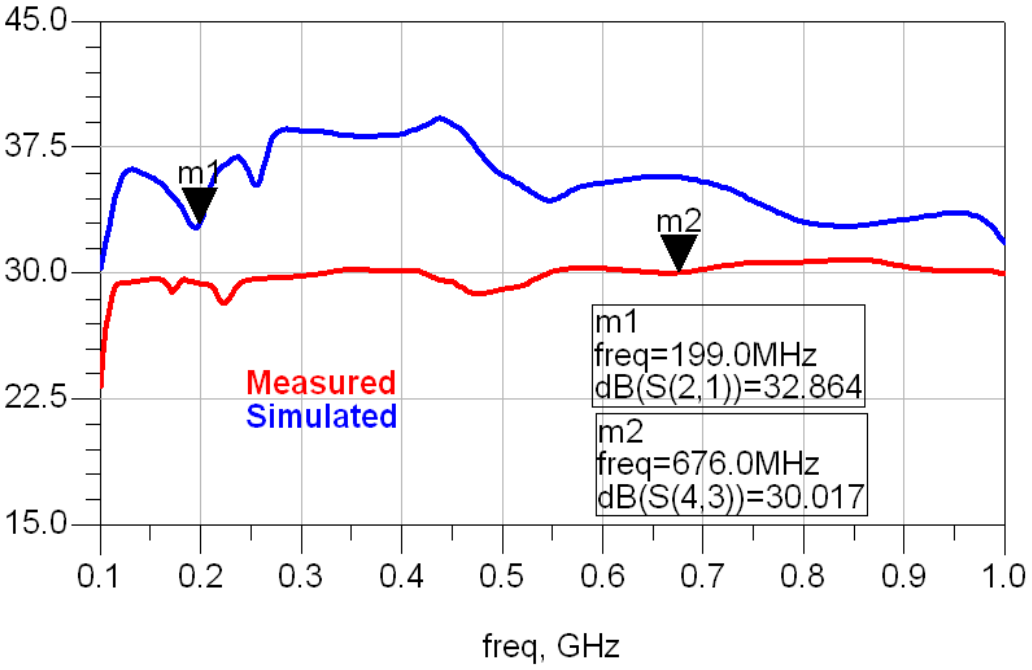


Figure 3-51 Two amplifiers cascaded gain

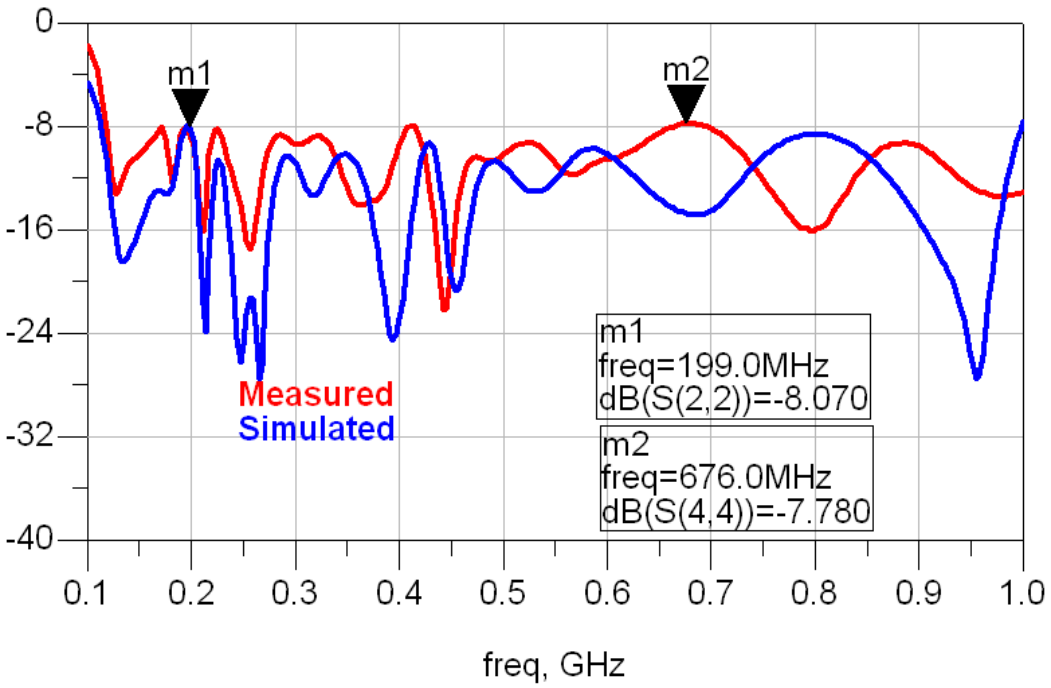


Figure 3-52 Two amplifiers cascaded output return loss

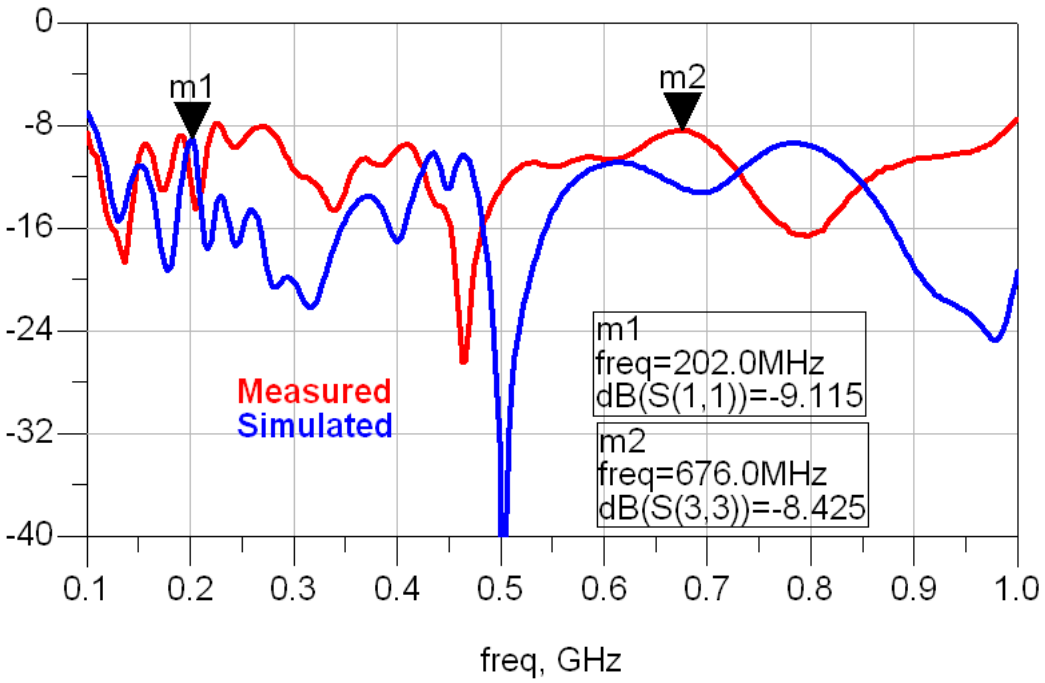


Figure 3-53 Two amplifiers cascaded input return loss

CHAPTER 4

DISTRIBUTED AMPLIFIER WITH MANIFOLD STRUCTURE

Previous chapter of this thesis is dedicated to the detailed design of a 0.1-1 GHz amplifier with the proposed topology. In this chapter, the same proposed topology is applied to two different amplifiers by changing some of the properties like number of channels and multiplexer schemes.

Proposed topology in Chapter 3 uses lumped Butterworth band-pass filters as de-multiplexer and multiplexer. Lumped matching is preferred for the amplifying paths. Moreover amplifier in Chapter 3 is a three channel amplifier.

First amplifier to be proposed in this chapter is a 0.1-1 GHz amplifier with five channels. Frequency spectrum is divided into five by applying the same procedure explained in Chapter 3. For de-multiplexer and multiplexer, tubular filter topology is preferred. For matching in the amplifying paths, high-pass matching is selected.

Proposed second amplifier in this chapter is a 1-6 GHz amplifier with three channels. Spectrum is divided into three as in other processes. As the de-multiplexer, tubular topology is selected for its superior characteristics for the frequency range. And simple lumped band-pass match is applied in the amplifying sections. The main difference is the manifold multiplexer employed in this topology.

This chapter first discusses a five channel amplifier for 0.1-1 GHz based on the proposed topology with the detailed description of the sections. This amplifier is fabricated and measured with the same set-up as in Chapter 3. Measurement results are compared to the simulated ones at the end of section. Then a three channel

amplifier for 1-6 GHz is discussed in detail. Only simulation results are given; since this amplifier is not fabricated in this thesis work.

4.1 Five Channel Amplifier for 0.1-1 GHz

This amplifier is based on the same procedure that is discussed in Chapter 3, however this time five channels are constructed for the same bandwidth. The reason behind the higher number of channels comes from the fact that the proposed topology may be used for different purposes. The proposed topology can be used to design power amplifiers and/or general amplifiers. For different applications, a higher number of channels may give better results in terms of circuit requirements.

Dividing the spectrum logarithmically into five, leads to the following corner frequencies:

- 1^{st} channel : 0.1 – 0.159 GHz
- 2^{nd} channel : 0.159 – 0.252 GHz
- 3^{rd} channel : 0.252 – 0.4 GHz
- 4^{th} channel : 0.4 – 0.635 GHz
- 5^{th} channel : 0.635 – 1 GHz

Logarithmically divided spectrum leads to almost equal effort on matching for all of the amplifying parts.

In the following sections, parts of the amplifier are discussed in detail.

4.1.1 De-multiplexer and Multiplexer Scheme

A five channel distributed amplifier requires different de-multiplexer and multiplexer schemes. Classical band-pass filter topology applied in Chapter 3 is cumbersome and not easy to implement. For this purpose, tubular type filters are selected. Tubular filters are easily connected to each other with the help of a manifold. They have lower inter-channel distortion and they are very easy to implement on PCB. In his paper, Galbraith [24, 25] employed tubular amplifiers in a channelizer. In that work, Galbraith makes use of the impedance shown by the tubular amplifier and obtains a

stepped impedance network to combine different channels. Tubular filter topology presents an inductive impedance for higher frequencies and a capacitive impedance for lower frequencies. By placing tubular filters along a manifold and employing inductors in the manifold, Galbraith successfully obtains a channelizer from 0.182 GHz to 1.13 GHz with ten channels. Galbraith explained the theory behind tubular filter. In this project, filter design program FILPRO is used to obtain the tubular filters.

Figure 4-1 shows the basic tubular schematic with two inductors and three capacitors. Degree of the filters can be increased depending on the type of the application. A higher order filter would yield a higher selectivity, thus less inter-channel distortion for this amplifier. However a higher order filter employs more elements which in turn enlarge the overall amplifier area. For these reasons, a tubular filter of second order is selected; since it provides sufficient selectivity with an easy implementation.

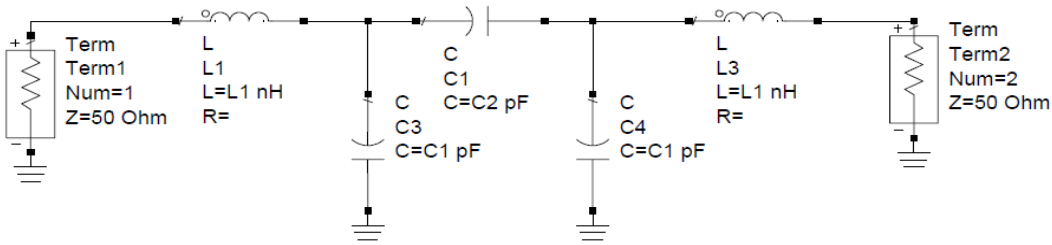


Figure 4-1 Tubular filter schematic

Table 4-1 provides lumped element values for all of the channels. As mentioned earlier, these values are obtained with FILPRO.

Table 4-1 Element values for tubular filters for five channel de-multiplexer

Channel #	L1 (nH)	C1 (pF)	C2 (pF)
1	190.4	5.75	2.6
2	120	3.6	1.6
3	76	2.28	1
4	47.8	1.44	0.65
5	30.7	0.9	0.4

Results for the tubular filters are given in Figure 4-2, which depicts that tubular filters provide sufficient selectivity for multiplexing operation. The most important property of tubular filter can be seen in Figure 4-2. Smith chart in Figure 4-2 displays the impedance characteristics (input and output both) which would be very useful for multiplexing. As can be seen from Figure 4-2, for higher frequencies tubular filter presents an inductive high impedance; whereas for lower frequencies it presents a capacitive high impedance. This fact will be useful when these filters are combined along a manifold.

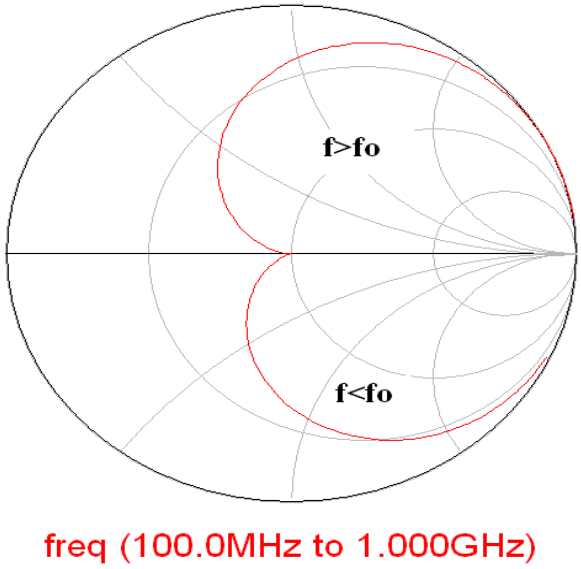


Figure 4-2 Tubular filter impedance characteristic

Figure 4-3 displays an five individual tubular filters with the element values calculated above. Figure 4-3 shows insertion losses for tubular filters built with ideal elements. With the use of more realistic component models, insertion losses are expected to be higher.

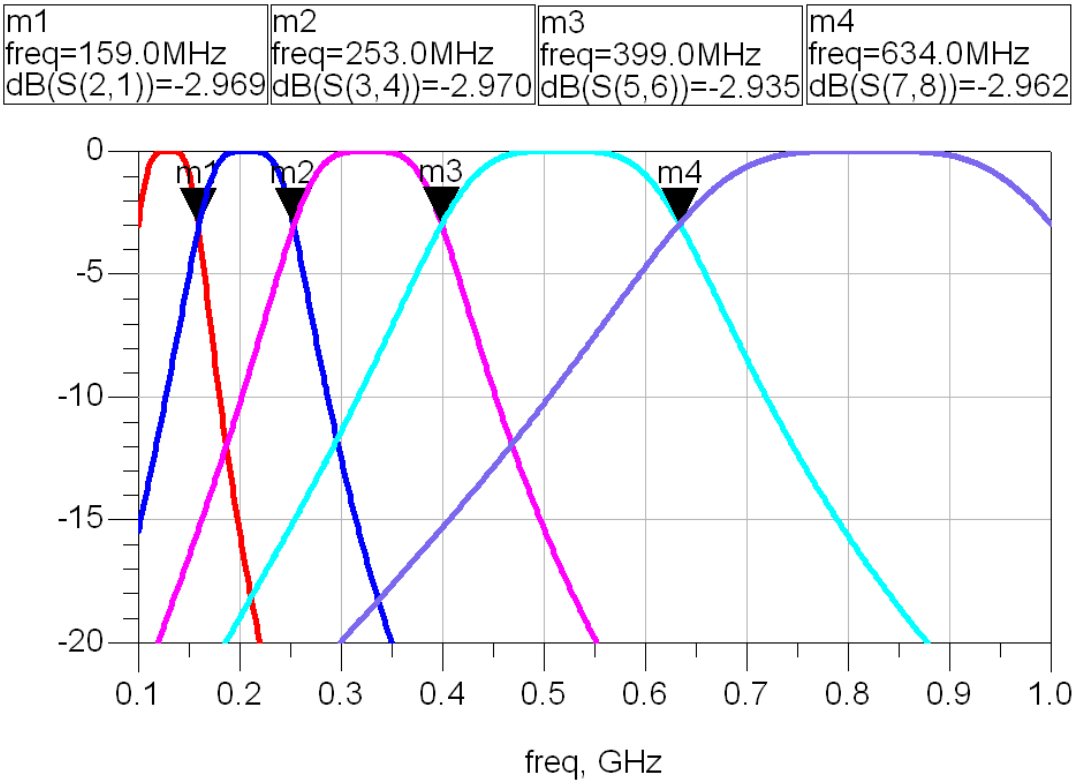


Figure 4-3 Tubular filter results for five channel de-multiplexer

A manifold is a structure, either a transmission line or waveguide, that filters are connected with spacings between them. These spacings provide necessary phase adjustments for proper multiplexing operation. A schematic of a basic manifold structure is given in Figure 4-4.

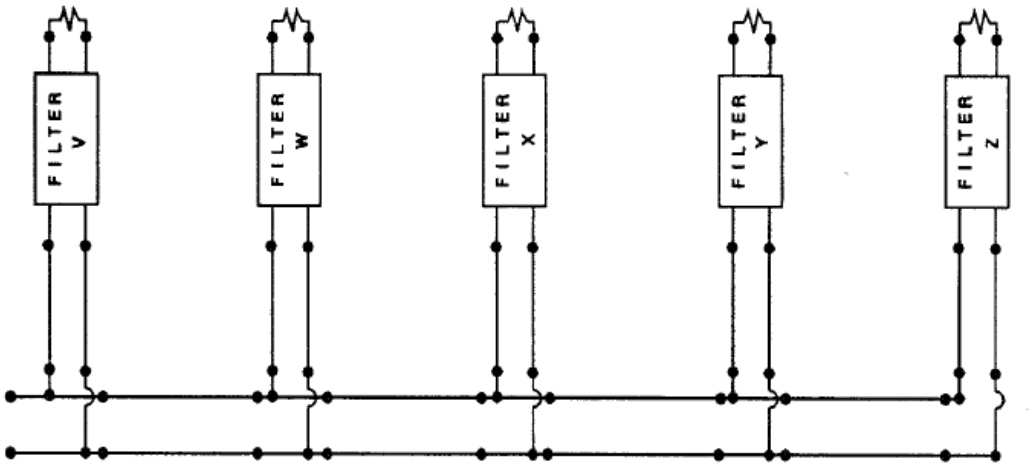


Figure 4-4 Basic manifold structure ([25])

Figure 4-4 displays five filter connected to a manifold with spacing between each channel. Filters may be contiguous or non-contiguous depending on the application. Rhodes [27] explained a generalized theory for multiplexer operation with mathematical calculations. In his paper [28], he further explained manifold multiplexer operation that can be applied to both contiguous and non-contiguous cases.

Now that tubular filters are designed, they can be connected on a manifold. Spacings between the filters can be optimized for the desired goal definitions. Transmission line manifold structure is employed in the design; however with a change in the structure. Surface mount inductors are also employed between channels, since transmission lines would be too long when frequency of operation is considered. Transmission lines and inductors are tuned manually to obtain a five channel multiplexer. For simpler optimization, transmission lines' lengths are kept constant at 4 mm which provides the space between amplifying paths. For phase synchronization lumped inductors are optimized; however this optimization is performed when all of the sections are connected together, since amplifying paths are not exactly 50 ohms. These non-ideal terminations of amplifying paths could alter the properties of filters, thus the properties of the de-multiplexer and multiplexer. Figure 4-5 displays the structure for the manifold and filters connected directly to it.

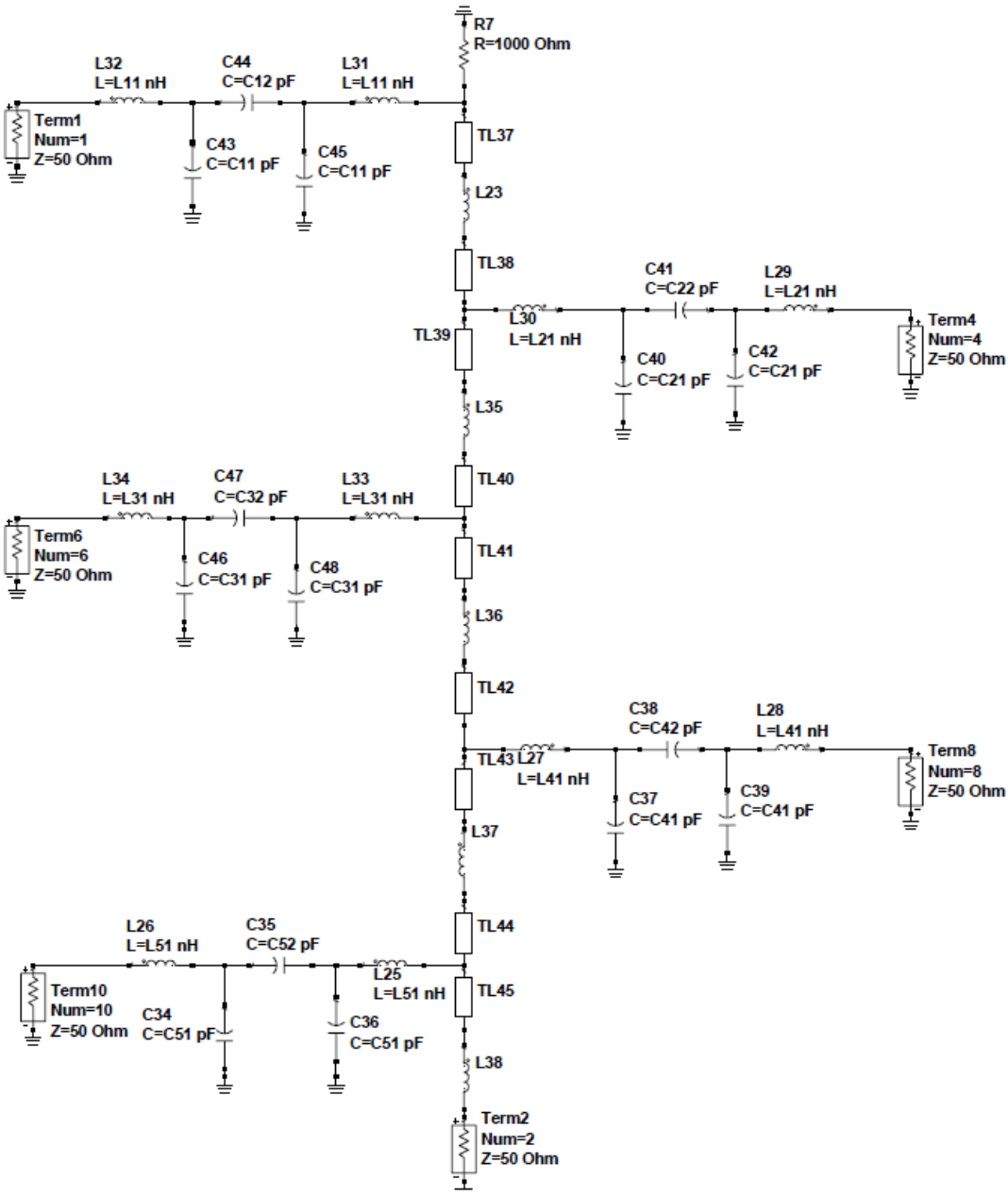


Figure 4-5 Manifold type de-multiplexer and multiplexer

Results of the filter can be observed from Figures 4-6 and 4-7. As depicted in these figures, manifold structure provides a neat multiplexer operation.

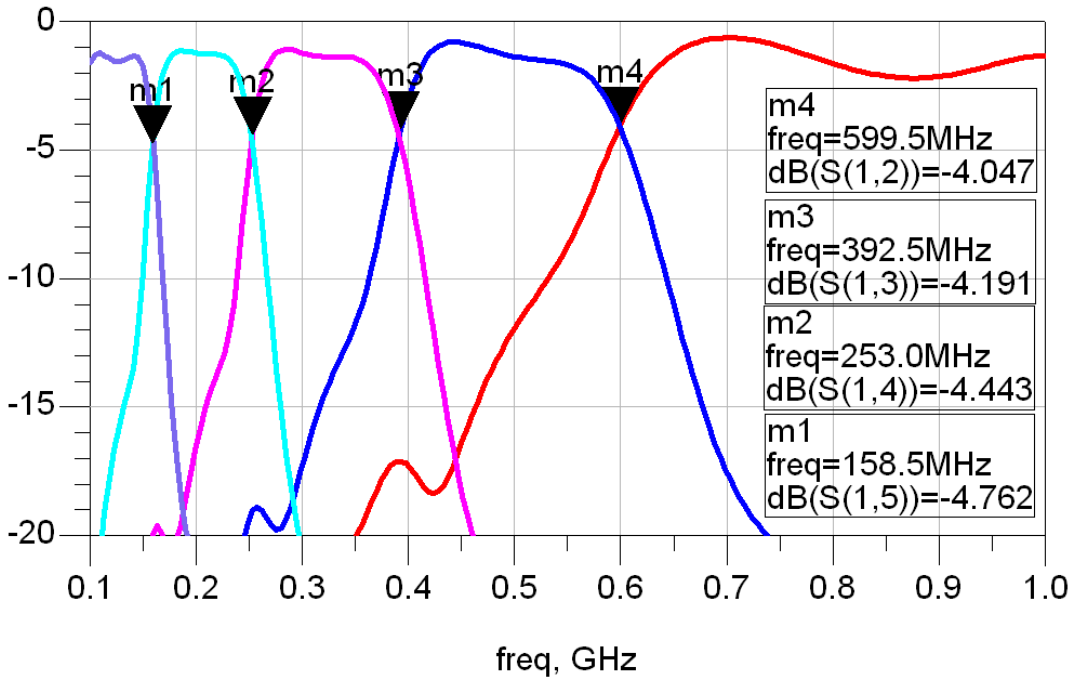


Figure 4-6 Manifold multiplexer insertion loss performance

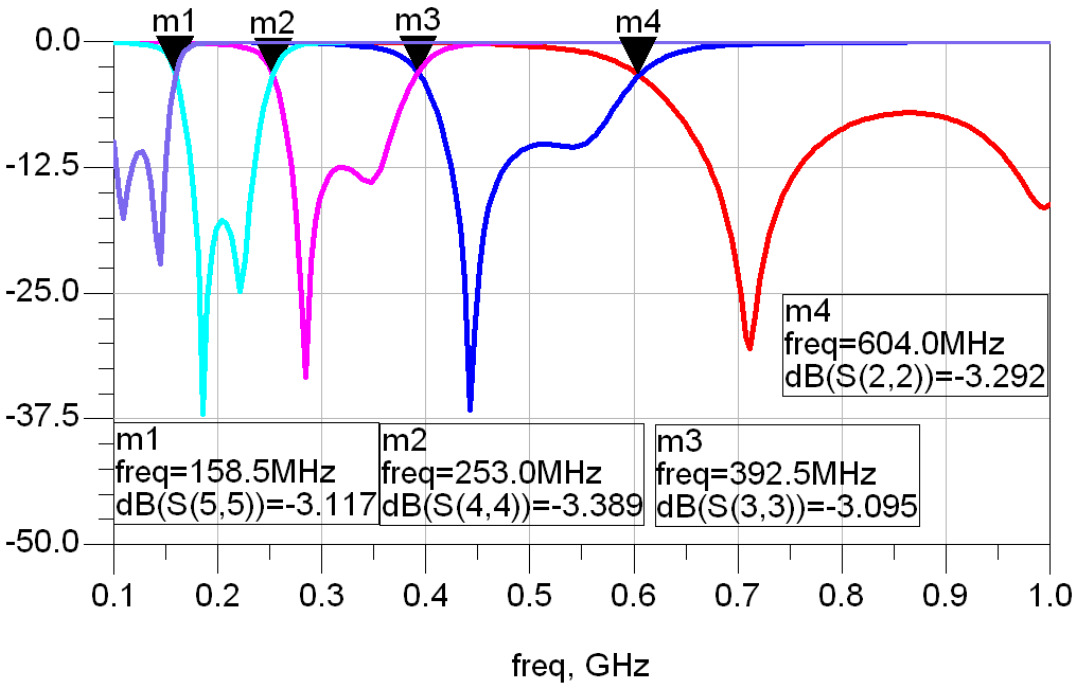


Figure 4-7 Return loss for channels connected to the manifold

4.1.2 Amplifying Parts

This section covers the amplifying parts of the proposed amplifier. As depicted in Chapter 3, amplifying parts play a crucial role in the phase alignment of the channels. The same procedure applied in Chapter 3 is also applied to five channel manifold amplifier, i.e. matching elements are optimized to provide phase synchronization without disturbing its matching duty.

For matching circuitry, lumped high-pass match is selected. Low-pass and band-pass match is also applied to the circuitry, however best performance is obtained with high-pass match scheme. For the low-pass and band-pass matching schemes, the impedance presented to the tubular filters result in mismatches. High-pass match is composed of two series capacitors and a parallel inductor between as shown in Figure 4-8. Same topology is applied both at input and output with different component values.

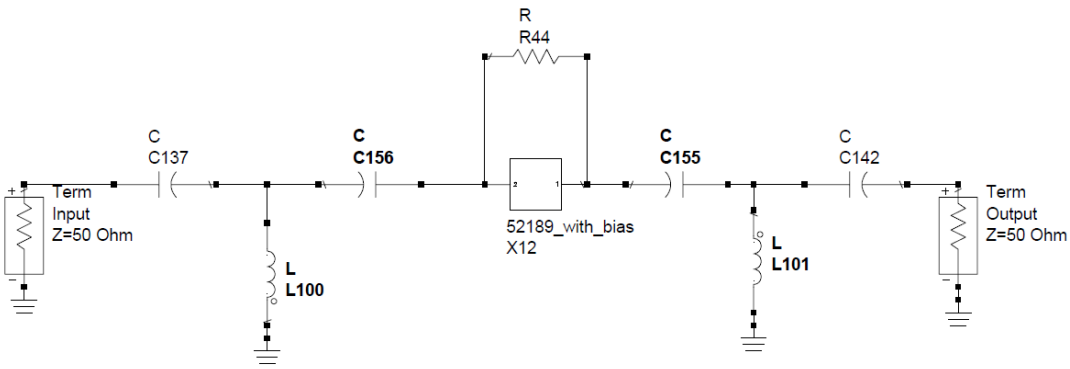


Figure 4-8 Amplifiers with high-pass matching schemes

Same structure for the transistor as in Chapter 3 is also employed in this amplifier. Avago Technologies' ATF52189 is selected as the transistor. A feedback of 270 ohm is used for wide band operation and for stability issues. Impedance values for input and output of ATF52189 with feedback is extracted in Chapter 3. Same values are used in this design for high-pass match scheme. Agilent's ADS is preferred for simulation program and matching elements are extracted using its matching tool.

Schematic for amplifying parts is given in Figure 4-8. Element values are not depicted in this section, which are given in whole circuit section after optimization. Results for the amplifying paths are depicted in Figures 4-9 to 4-13 for all of the channels.

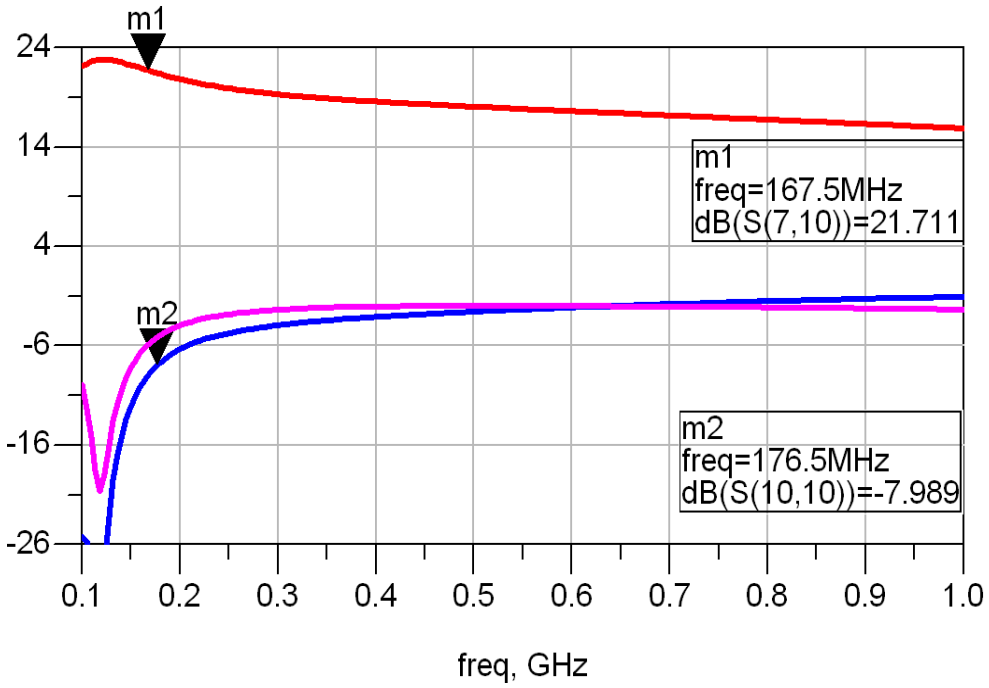


Figure 4-9 Channel 1 amplifying path results

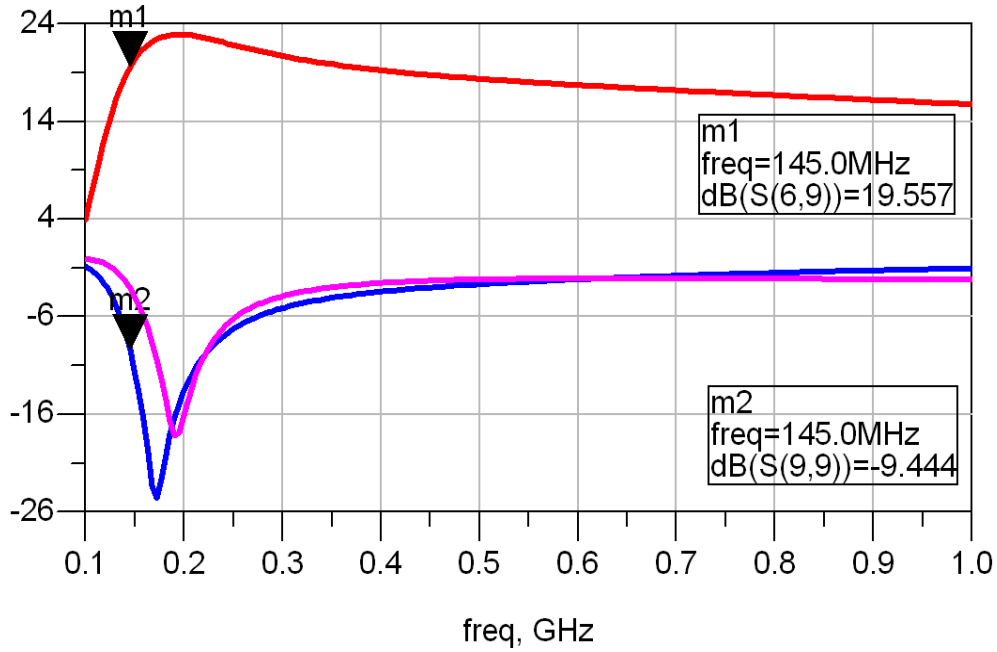


Figure 4-10 Channel 2 amplifying path results

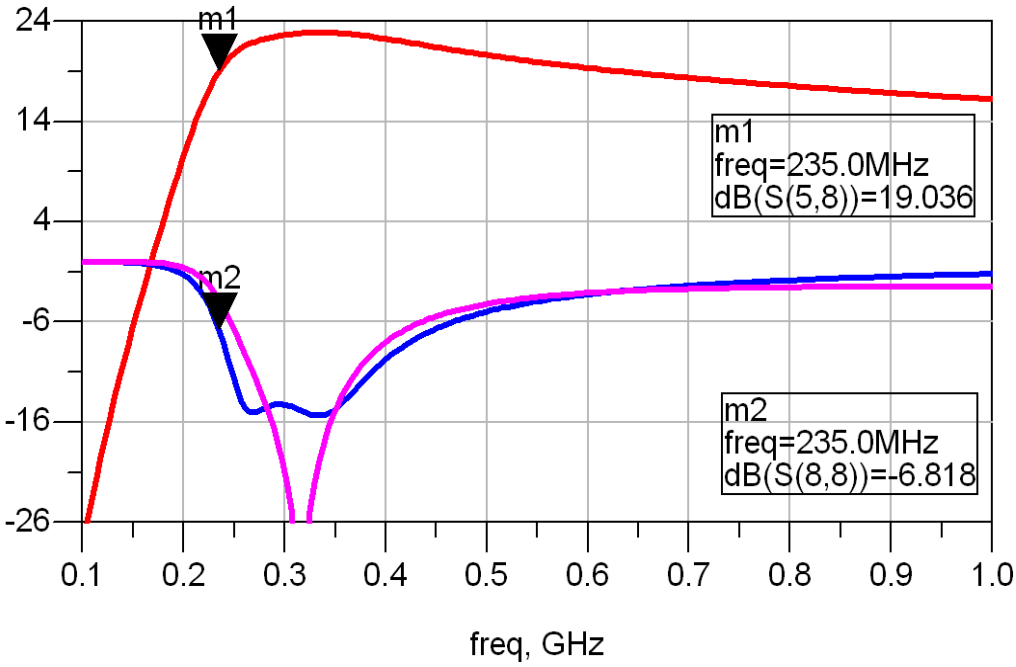


Figure 4-11 Channel 3 amplifying path results

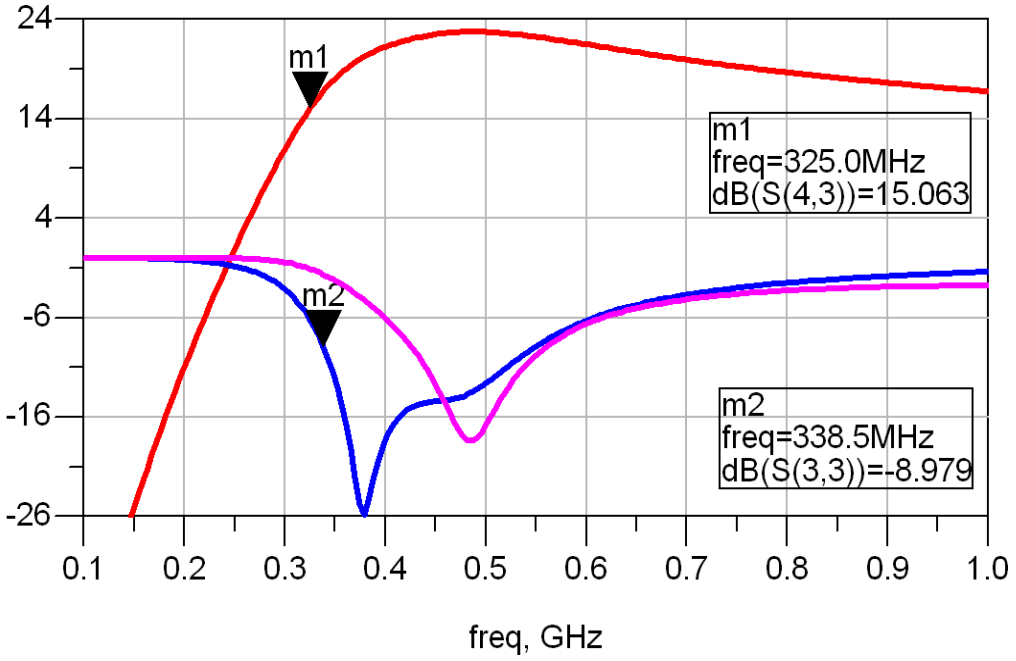


Figure 4-12 Channel 4 amplifying path results

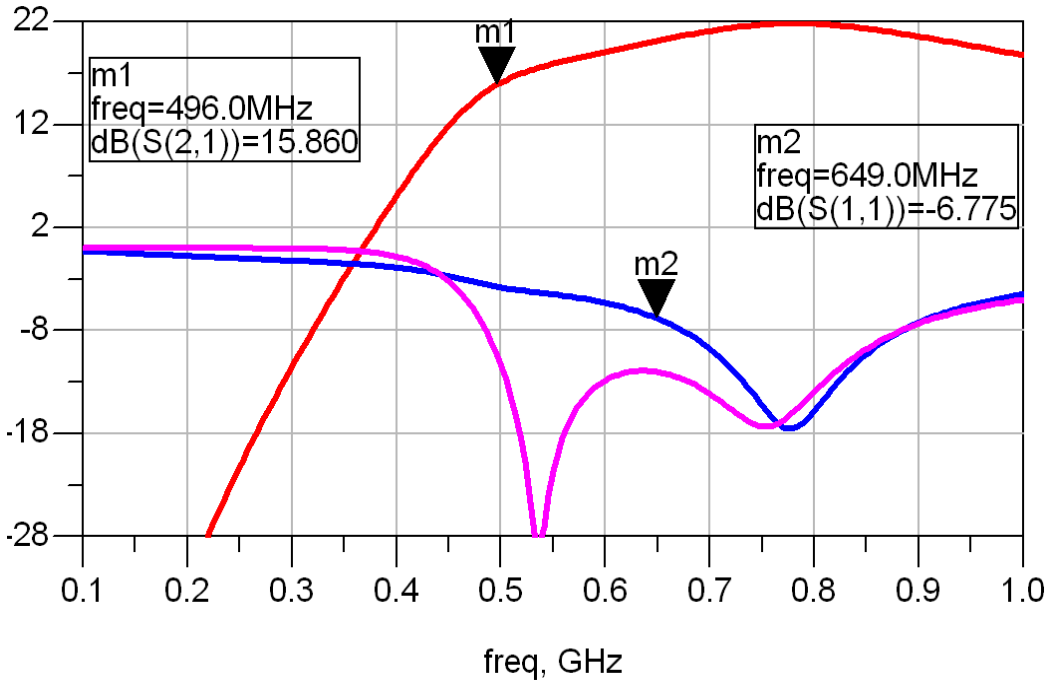


Figure 4-13 Channel 5 amplifying path results

4.1.3 Whole Circuit

Whole amplifier is obtained when de-multiplexer, amplifying paths and multiplexer are combined which is depicted in Figure 4-14. As mentioned earlier, de-multiplexer and multiplexer inductor values are optimized as well as the matching elements of the amplifying paths. Tubular filter elements are not optimized during the process. ADS' Optim tool is selected for optimization as in Chapter 3. Goals are specified for gain and return losses for both terminations. Gain is expected to be greater than 20 dB, whereas return losses are expected to be lower than -10 dB for the whole frequency range.

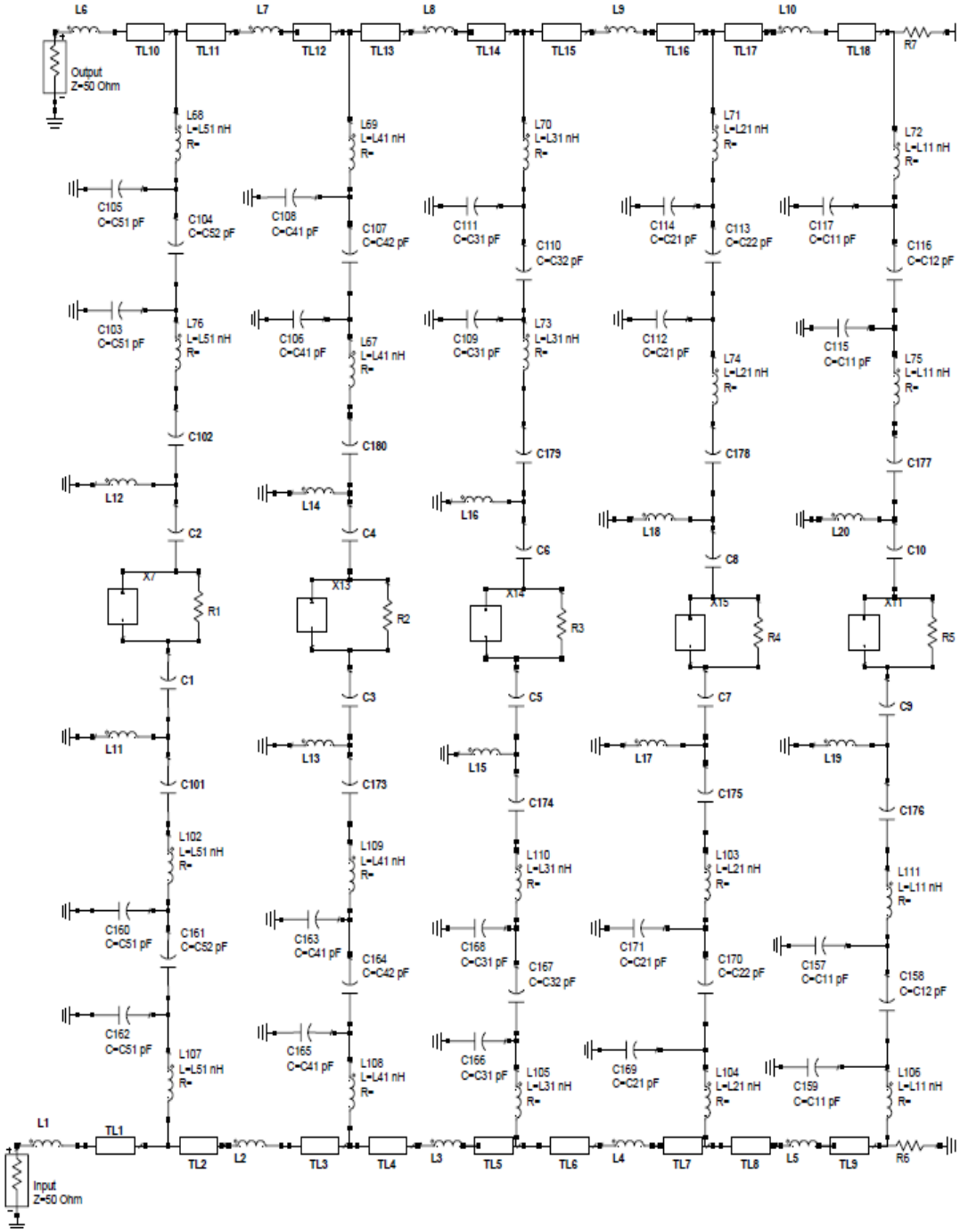


Figure 4-14 Five channel amplifier whole circuit

Optimized values are given in table 4-2. These values are also used in order to obtain the amplifying path results in section 4.1.2.

Table 4-2 Element values for the 0.1-1 GHz five channel amplifier

Component	Value	Component	Value	Component	Value
L1, L6	4.17 nH	C173	100 pF	L17	44 nH
L2, L7	0 nH	L13	13 nH	C7	24 pF
L3, L8	0.15 nH	C3	12 pF	C8	42 pF
L4, L9	2.14 nH	C4	12 pF	L18	14.2 nH
L5, L10	0.23 nH	L14	6.9 nH	C178	38 pF
R1,…,R5	270 Ohm	C180	9.1 pF	C176	150 pF
R6,R7	1 kOhm	C174	23 pF	L19	52 nH
C101	58 pF	L15	15.15 nH	C9	48 pF
L11	4.7 nH	C5	15 pF	C10	55 pF
C1	6.3 pF	C6	17.8 pF	L20	32 nH
C2	4.8 pF	L16	11.7 nH	C177	100 pF
L12	5.5 nH	C179	23 pF		
C102	5.3 pF	C175	180 pF		

Simulation results are given in Figures 4-15, 4-16 and 4-17. Results clearly display a gain of 19.4-22.2 dB and return losses below -10 dB. The circuit can easily be manufactured with surface mount elements. Simple tuning on the values may lead to the desired result.

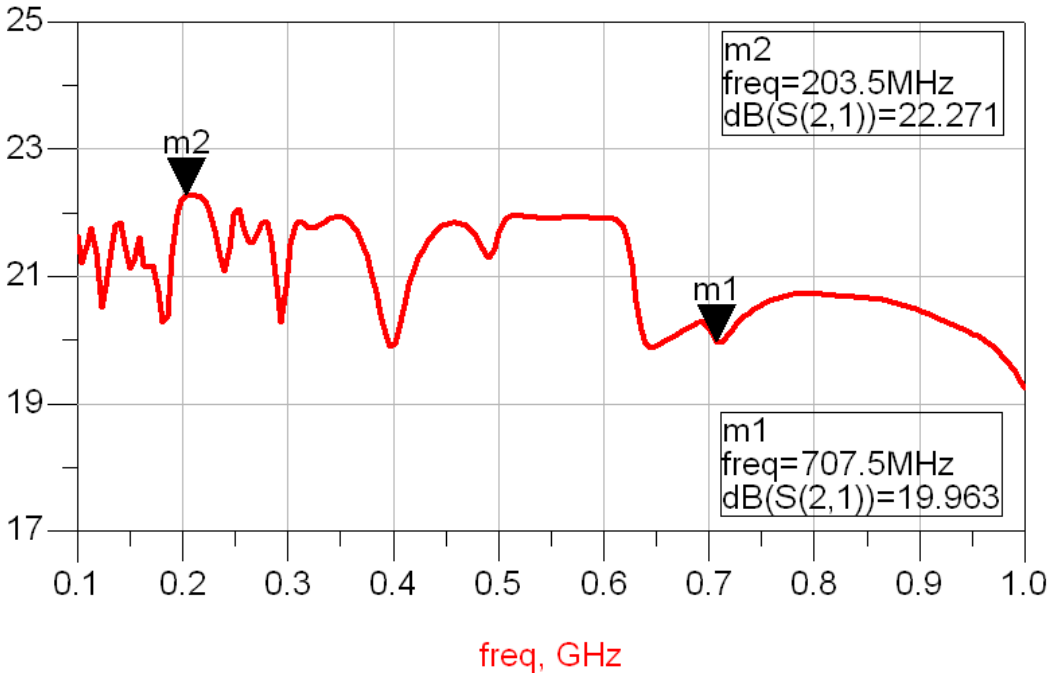


Figure 4-15 Gain response of five channel amplifier

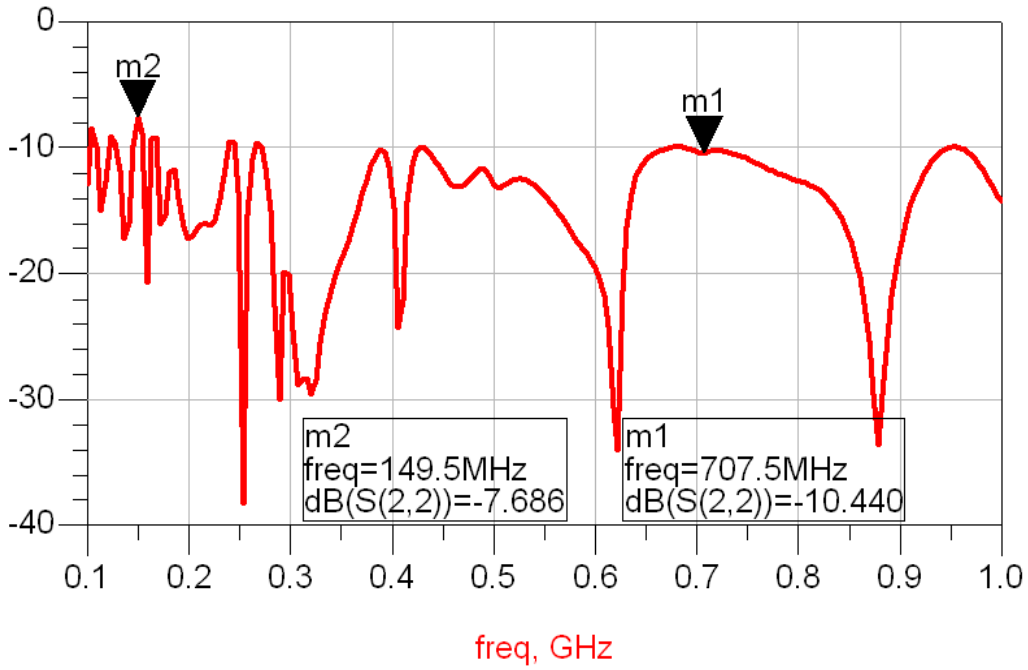


Figure 4-16 Return loss for output of five channel amplifier

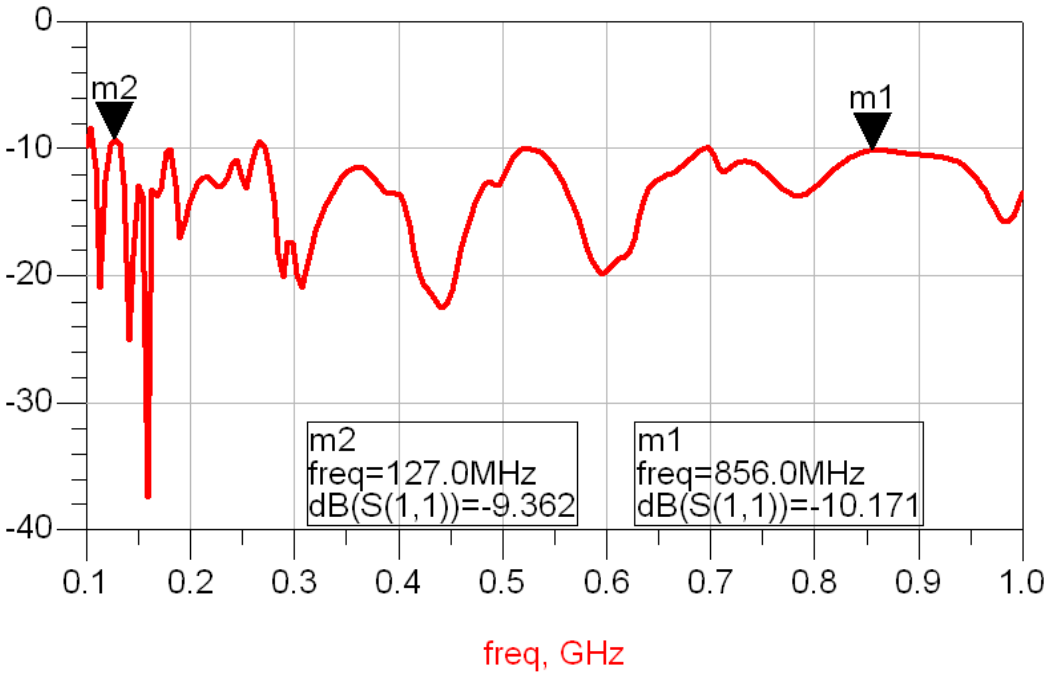
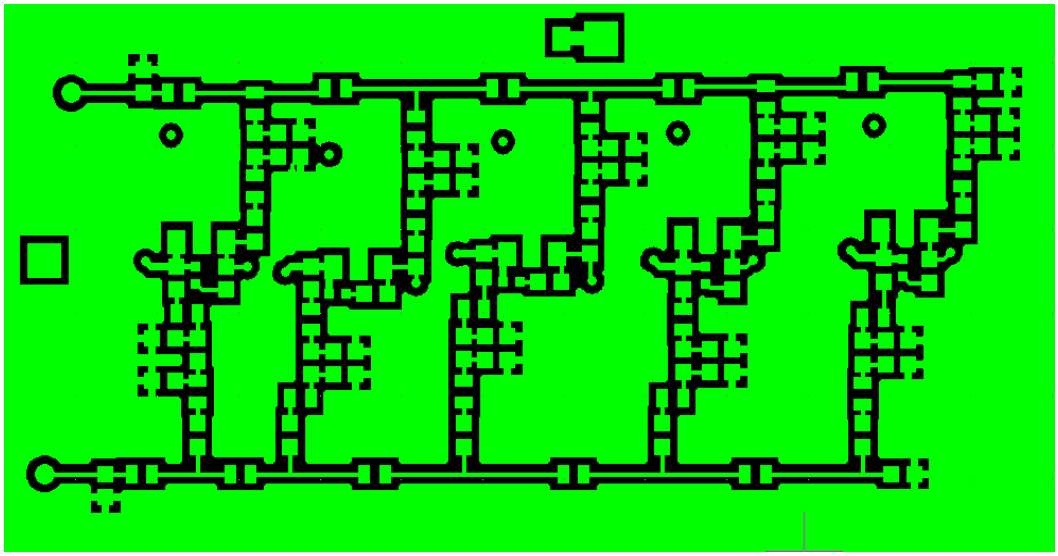


Figure 4-17 Return loss for output of five channel amplifier

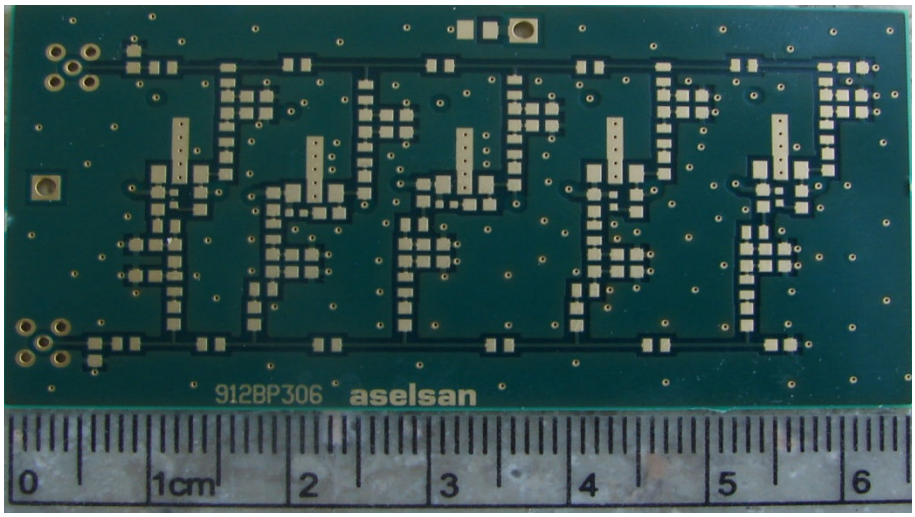
4.1.4 Layout Generation and Fabrication

Results indicate a promising amplifier for implementation for 0.1-1 GHz. Due to lower operational frequency, High-Tg FR4 is selected as the dielectric material with a thickness of 0.12 mm. Four layers are preferred in the design since RF lines do not cross each other. Top layer of the PCB is reserved for RF lines; whereas bottom layer is filled with DC lines. Two middle layers are ground layers for isolation and proper microstrip impedance.

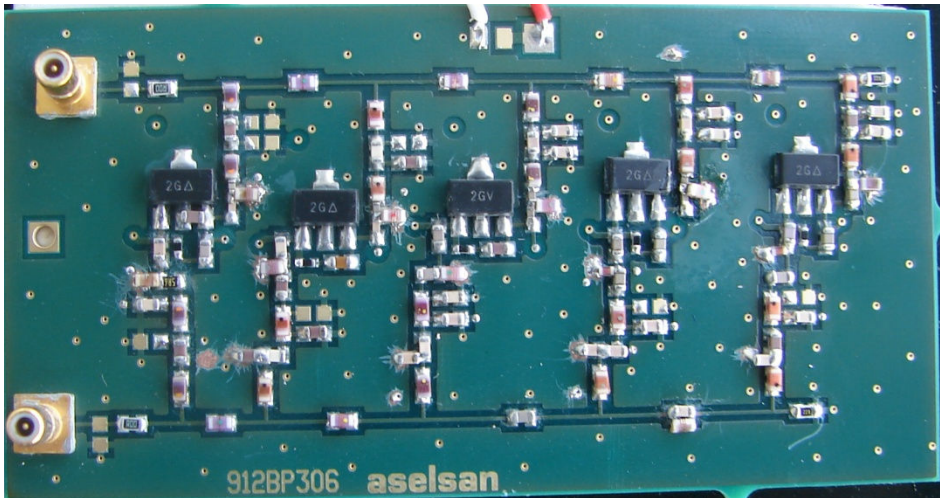
Generated layout's together with the fabricated PCB are shown in Figures 4-18 a-c.



a)



b)



c)

Figure 4-18 a) Layout for 0.1-1 GHz five channel amplifier b) Fabricated PCB c) PCB with components mounted on

4.1.5 Results for Five Channel 0.1-1 GHz amplifier

Element values given in Table 4-2 are placed on the layout shown. Adjustments on the values may be necessary due to the differences between simulation and implementation. Inherent capacitances associated with the layout bring up changes on the values especially for the capacitors. Tubular filter employed in this design makes use of capacitors connected to ground which provides an inherent immunity for parasitic capacitance. Even though the design has such an immunity, adjustments are necessary on the components.

The following results associated with the design are observed after these adjustments on the components are applied. Simulation and measurement results are compared for all of the parts of the amplifier. First of all, de-multiplexer (multiplexer as well) results are compared for five channels. Figures 4-19a-e indicates results for channels from the lowest frequency to highest, respectively.

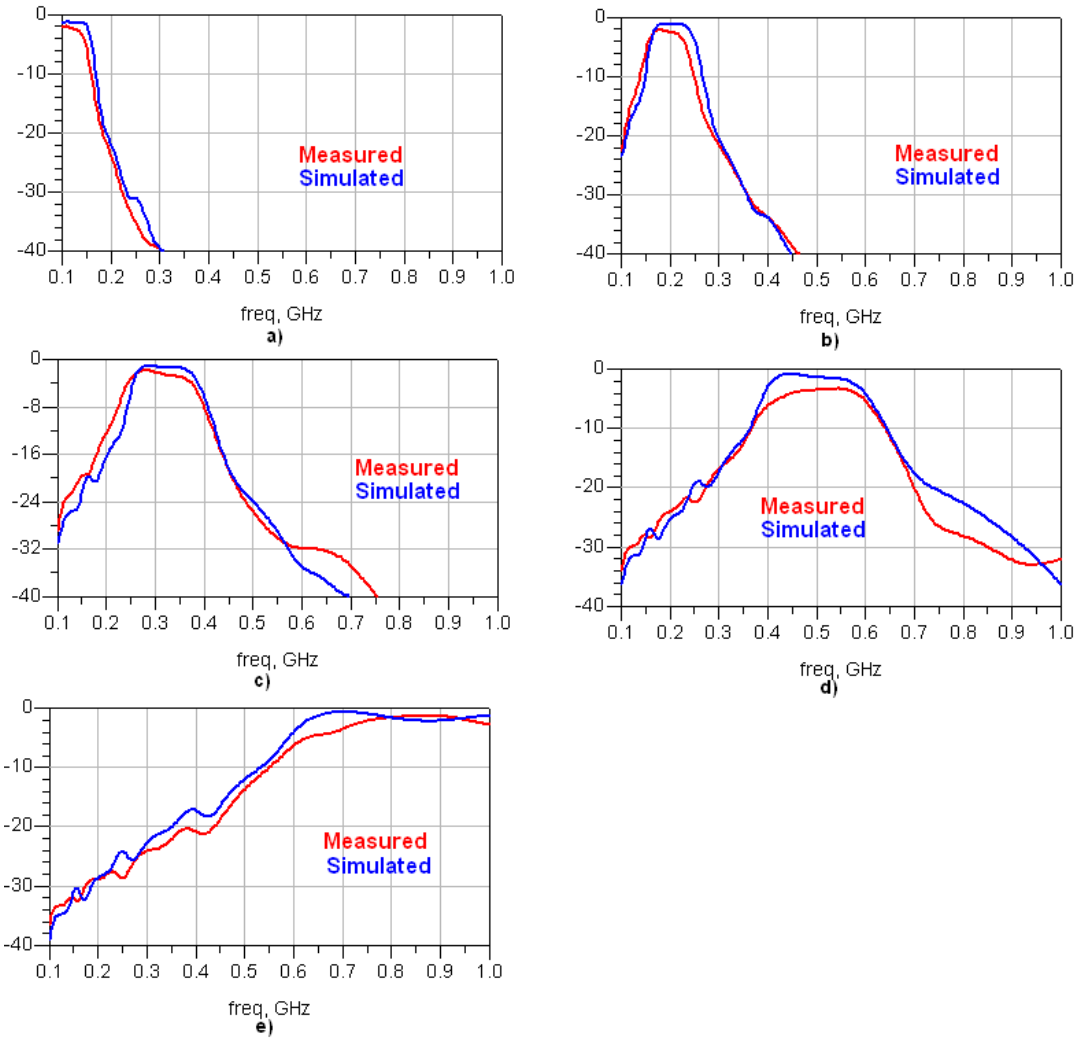


Figure 4-19 De-multiplexer (also multiplexer) Results a) 1st Channel, b) 2nd Channel, c) 3rd Channel, d) 4th Channel, d) 5th Channel

Results indicate similar cut-off regions for all of the channels; however insertion losses of the measured system seem to be 0.5-2 dB higher than the simulated ones. These higher insertion losses for de-multiplexer and multiplexer reduce the gain of the amplifier by up to 4 dB.

Second results belong to the amplifying path section where high-pass matching schemes are employed for all of the paths. Figure 4-20a-e displays the results for each channel, starting from the lowest frequency channel.

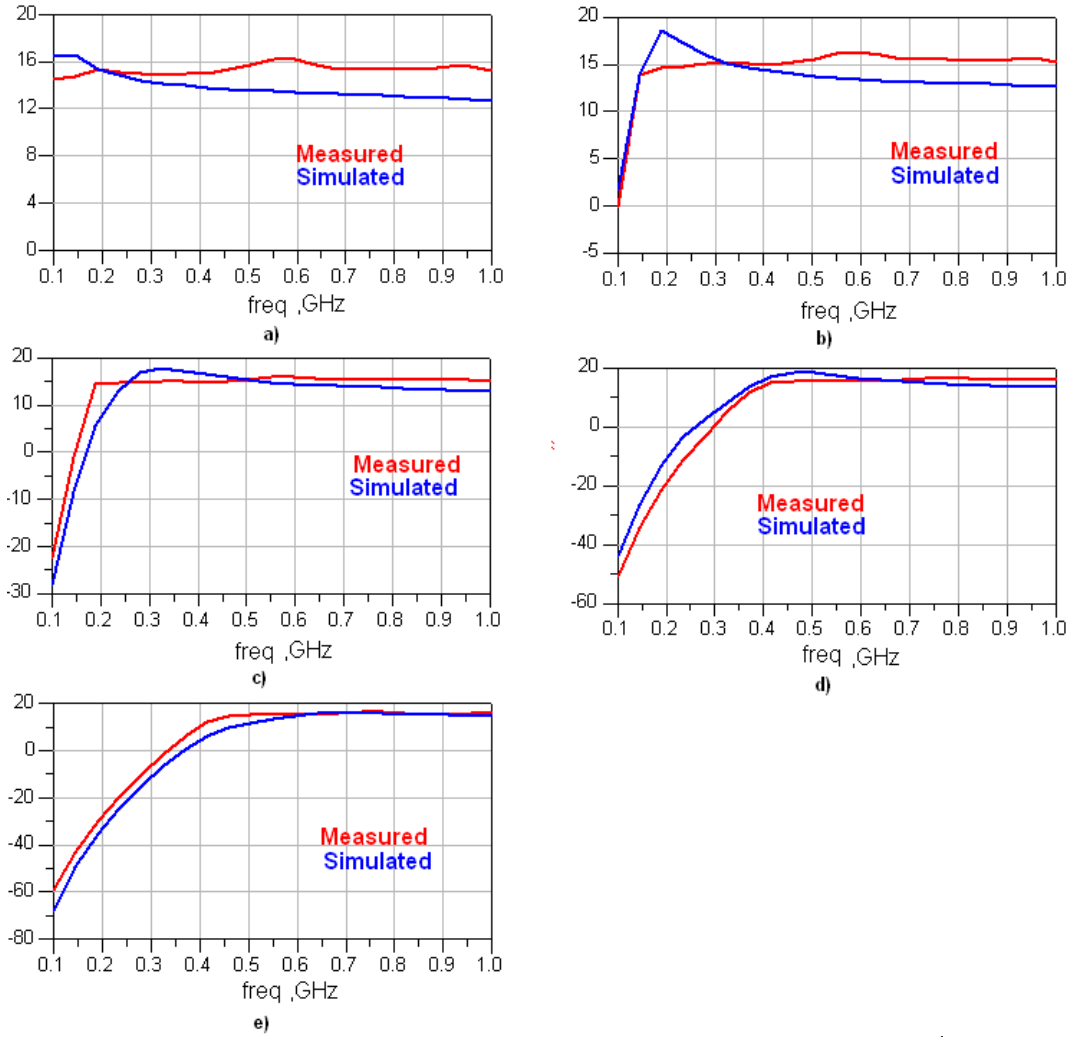


Figure 4-20 De-multiplexer (also multiplexer) Results a) 1st Channel, b) 2nd Channel, c) 3rd Channel, d) 4th Channel, d) 5th Channel

As can be observed from Figure 4-20, amplifying path results show similarities except the increase in gain at the cut-offs.

Finally the overall circuit response is given in Figure 4-21, 4-22 and 4-23 for 0.1-1 GHz. Results for 0.1-3 GHz is also given in Figure 4-24.

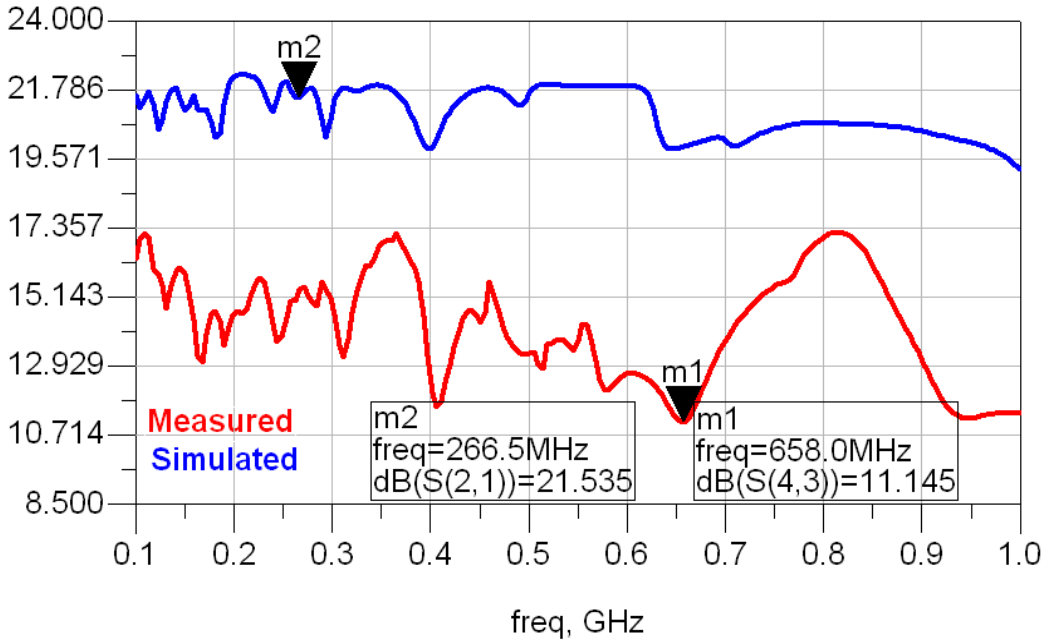


Figure 4-21 Gain response for 0.1-1 GHz five channel amplifier

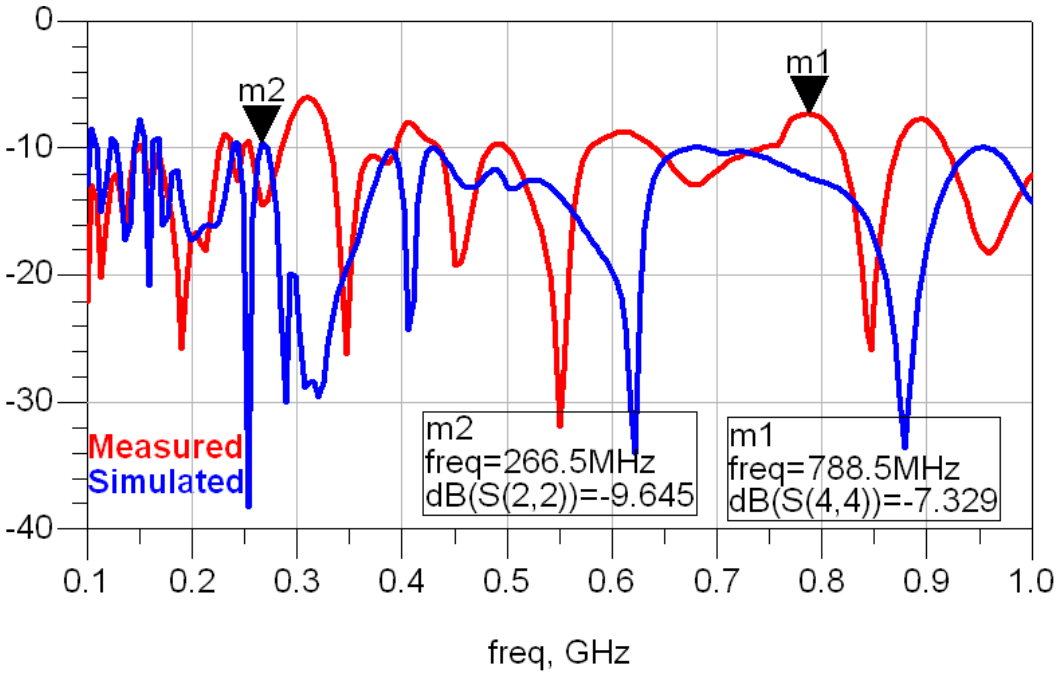


Figure 4-22 Output return loss for 0.1-1 GHz five channel amplifier

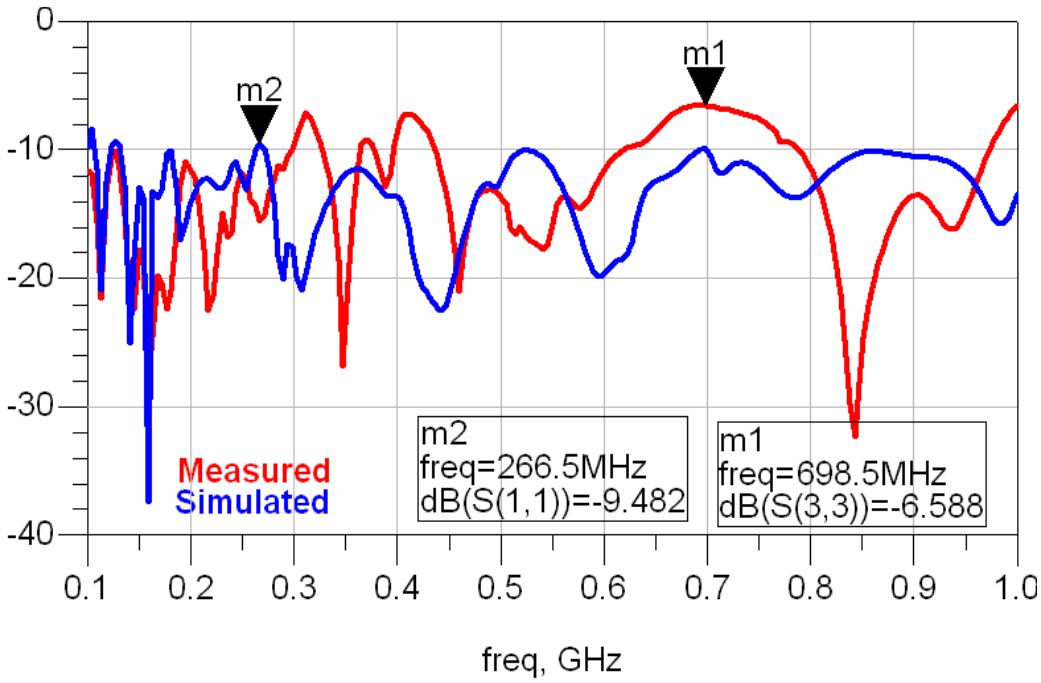


Figure 4-23 Input return loss for 0.1-1 GHz five channel amplifier

Figure 4-21, 4-22 and 4-23 shows that an amplifier with a gain of 14±2.5 dB and return losses lower than -6.5 dB is obtained. Gain response has a high deviation which may be the result of poor phase matching.

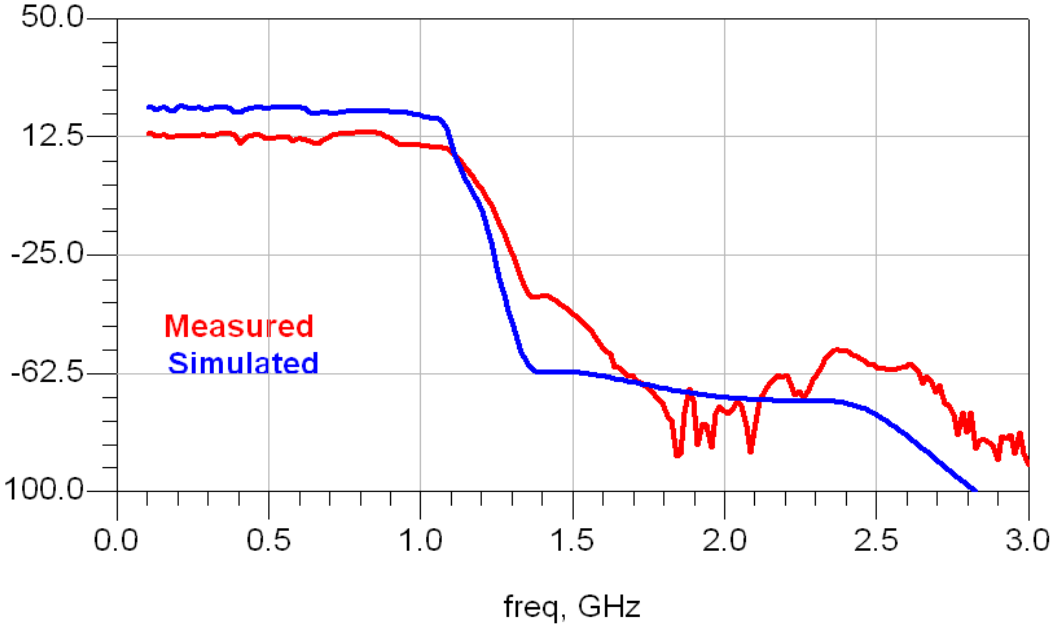


Figure 4-24 Gain response of five channel amplifier for 0.1-3 GHz

Results clearly indicate a decrease in gain which may be the result of poor matching and losses associated with the de-multiplexer and multiplexer. As mentioned earlier de-multiplexer and multiplexer bring up a loss of about 1 to 4 dB over the operational band. Moreover, simulated results are obtained by employing ideal components which results in an almost ideal gain response. One important factor contributing to the difference between measured and simulated results is the model of ATF52189 which is not suitable under large-signal conditions.

The results displayed for this amplifier indicates that designing a distributed amplifier with the new topology gets harder with increasing number of channels. Dividing the spectrum into more channels brings up complicated phase matching between channels. An optimum number for this new topology may be defined depending on the observations of these two amplifiers.

4.2 Three Channel 1-6 GHz Amplifier

Previous amplifiers are designed for 0.1-1 GHz range. For higher frequencies, the same procedure may also be applied. Lumped elements may be replaced by distributed counterparts. In order to apply the design topology for higher frequencies, a 1-6 GHz amplifier is designed. Three-channel design is preferred for simplicity; however number of channels may increase depending on the application.

Frequency spectrum 1-6 GHz is divided logarithmically into three which leads to corner frequencies:

- 1^{st} channel: 1-1.75 GHz
- 2^{nd} channel: 1.75-3.25 GHz
- 3^{rd} channel: 3.25-6 GHz

Logarithmic division leads similar effort on matching as depicted before.

The following sections cover the detailed description of de-multiplexer, amplifying parts and manifold multiplexer.

4.2.1 De-multiplexer and Amplifying Paths

In order to obtain a flat gain response throughout this frequency range, selected transistor should have a wide bandwidth; thus Avago's ATF35143 is preferred for this thesis work. ATF35143 has an operation range of 450 MHz to 10 GHz with an associated gain of 18 dB at 2GHz. Datasheet [29] provides the related information about the transistor.

For the sake of stability and matching, a resistive feedback is employed as in other amplifiers. 270 Ohm resistive feedbacks are used in order to provide a wide enough band. Applying the process described in Chapter 3 for determining the input and output impedances, the results in Table 4-3 are obtained. It should be reminded that impedance values are obtained with feedback connected between drain and gate of the transistor. These results have to be converted to their complex conjugates before applying in the matching process.

Table 4-3 Input and output impedance values for ATF35143

Channel	Input impedance (ohms)	Output impedance (ohms)
1	56.6+j25.6	32+j0.22
2	36+j14.2	49-j0.6
3	31-j6.36	59-j12.8

In this amplifier, de-multiplexer is designed with tubular filters as in the previous case. Tubular filters prove to be useful for high-frequency applications; however some of the element values are too small for surface mount technology. Distributed elements may be used in order to replace lumped elements. Another option for tubular filter is to employ end-coupled line filters which have the similar impedance characteristics with tubular topology. In this work, lumped element values are left as it is and further improvement is left as future work.

For the design of tubular filters, FILPRO is used to extract the element values. Tubular filters for this amplifier has the same configuration depicted in Figure 4-1. Table 4-4 displays the element values for all of the channels.

Table 4-4 Element values for tubular de-multiplexer for 1-6 GHz de-multiplexer

Channel	L1 (nH)	C1 (pF)	C2 (pF)
1	15	0.6	0.35
2	7.48	0.35	0.23
3	4.08	0.19	0.125

Results with the element values given in table 4-4 are depicted in Figures 4-18 and 4-19.

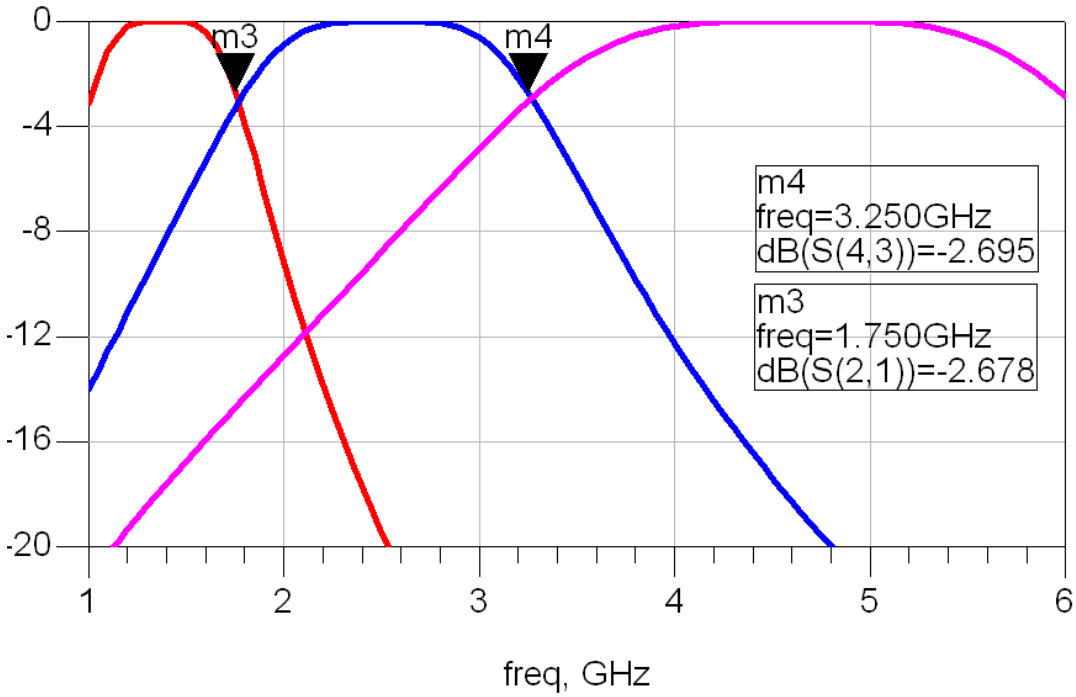


Figure 4-25 Insertion loss for tubular filters

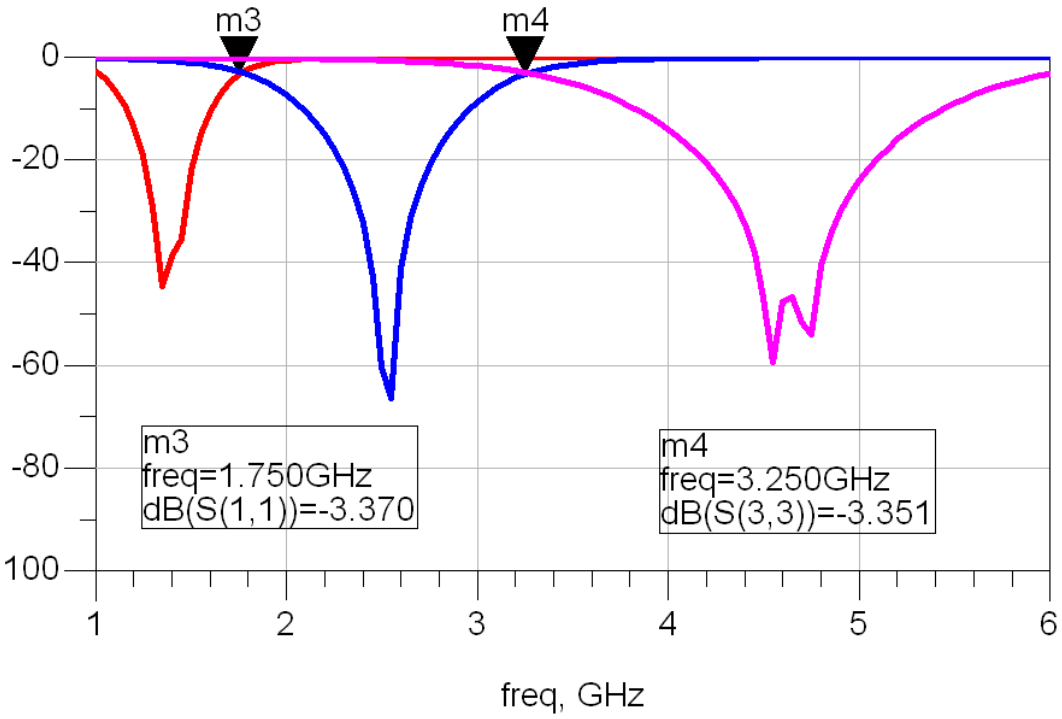


Figure 4-26 Return loss for tubular filters

These filters are terminated with 50 ohms, thus these results are expectable. In this proposed topology, Avago's ATF35143 transistor is preferred whose impedance values are calculated earlier. ATF35143 has fairly high impedance, thus a 50 ohm tubular filter may be directly connected to it without the need for matching elements. A tubular filter designed for 50 ohms may not work well when it is connected directly to the transistor with these impedance values. Thus values are tuned manually to obtain a good amplified multiplexer response. Optimized values are given in Table 4-5.

Table 4-5 Optimized values for de-multiplexer of 1-6 GHz amplifier

Channel	L1 (nH)	C1 (pF)	C2 (pF)
1	11.1	0.8	1.64
2	9.2	0.32	0.2
3	2.45	0.21	0.26

For output matching a simple band-pass structure is preferred contrary to the low-pass matching scheme employed for the three channel amplifier for 0.1-1 GHz

amplifier. A series inductor-capacitor is employed for matching which in turn proves to be very useful when connected to the multiplexer.

ATF35143 has fairly high impedance which makes impedance matching process easier. Manually tuning the values of the inductors and capacitors leads to a good output match for all of the channels. The values after tuning are given in Table 4-6.

Table 4-6 Band-pass match elements for channels of 1-6 GHz amplifier

Component	Value	Component	Value	Component	Value
L111	7.7 nH	L211	2.22 nH	L311	2.44 nH
C112	2.25 pF	C211	0.95 pF	C311	0.35 pF

4.2.2 Manifold multiplexer

The biggest difference between 1-6 GHz proposed amplifier and the other two 0.1-1 GHz amplifier lies in the phase synchronization. In 0.1-1 GHz amplifiers, phase synchronization is obtained in the amplifying paths part by optimizing the matching elements. On the other hand in 1-6 GHz amplifier, phase adjustment is applied in the multiplexer part. This gives the flexibility to design with different kinds of matching topologies; since these elements are kept fixed during final optimization.

For these purposes manifold type multiplexer is employed in the design. Manifold structure has been mentioned earlier in section 4.1.1. Here the same topology is used; however this time both lengths and widths of the transmission lines are optimized with the inductors between. Since frequency of operation is relatively high, inductors may be omitted. In this work inductors are also optimized. Schematic of the manifold multiplexer is given in Figure 4-20. As usual ADS' Optim tool is used for optimization.

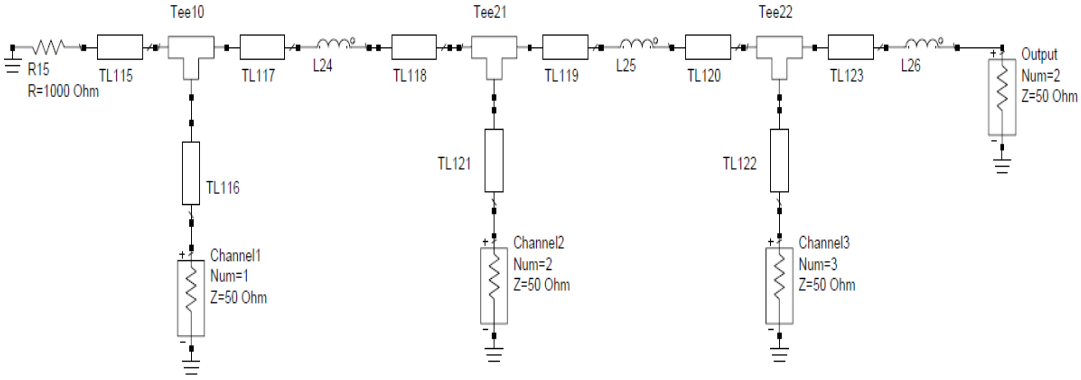


Figure 4-27 Manifold multiplexer schematic for 1-6 GHz amplifier

4.2.3 Whole 1-6 GHz amplifier

Now that de-multiplexer, amplifying paths and multiplexer are designed, they can be combined for the whole amplifier. As mentioned earlier de-multiplexer and amplifying paths are not optimized. Only manifold multiplexer elements are optimized with ADS' Optim tool whose goals are specified for gain and return losses. Gain is expected to be more than 10 dB; whereas return losses are expected to be lower than -10 dB. After optimization the element values in Table 4-7 are obtained for the multiplexer.

Table 4-7 Element values of manifold multiplexer in 1-6 GHz

Element	Value	Element	Value
TL115,width	0.16 mm	TL121,width	0.16 mm
TL115,length	0.1 mm	TL121,length	4.18 mm
TL116,width	0.16 mm	L25	0 nH
TL116,length	6 mm	TL120,width	0.16 mm
TL117,width	3.34 mm	TL120,length	0.85 mm
TL117,length	0.1 mm	TL123,width	0.48 mm
L24	0.12 nH	TL123,length	25 mm
TL118,width	3.95 mm	TL122,width	5.4 mm
TL118,length	0.4 mm	TL122,length	0.1 mm
TL119,width	3 mm	L26	0.2 nH
TL119,length	0.24 mm		

Circuit schematic for 1-6 GHz is given in Figure 4-21.

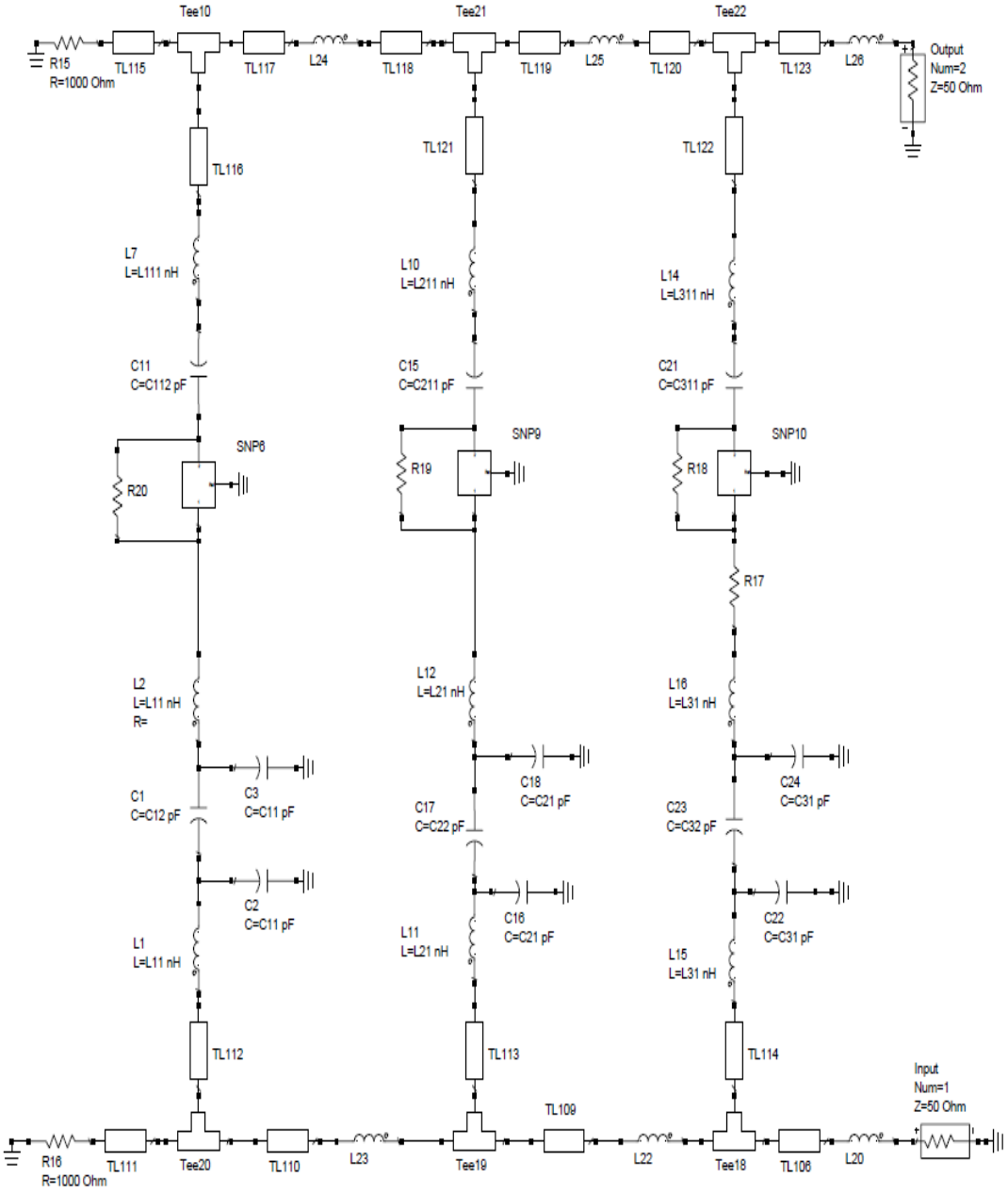


Figure 4-28 Circuit schematic for 1-6 GHz amplifier

4.2.4 1-6 GHz amplifier simulation results

Results in Figures 4-22, 4-23 and 4-24 indicate a gain of 9.7-11.6 dB and return losses below -9 dB.

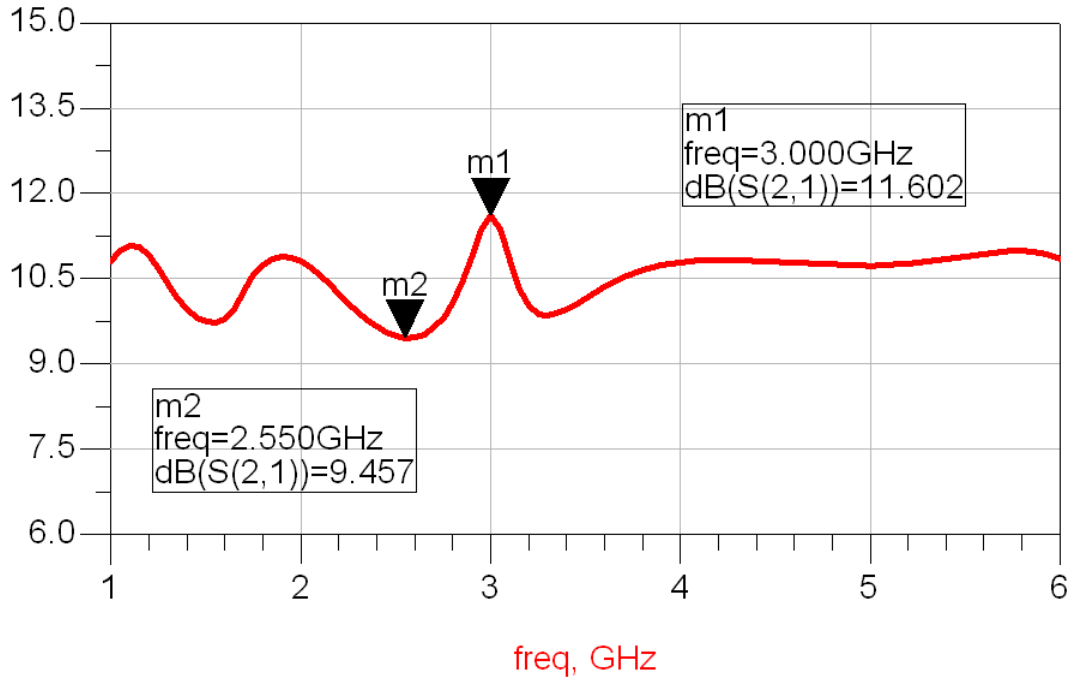


Figure 4-29 Gain response for 1-6 GHz amplifier

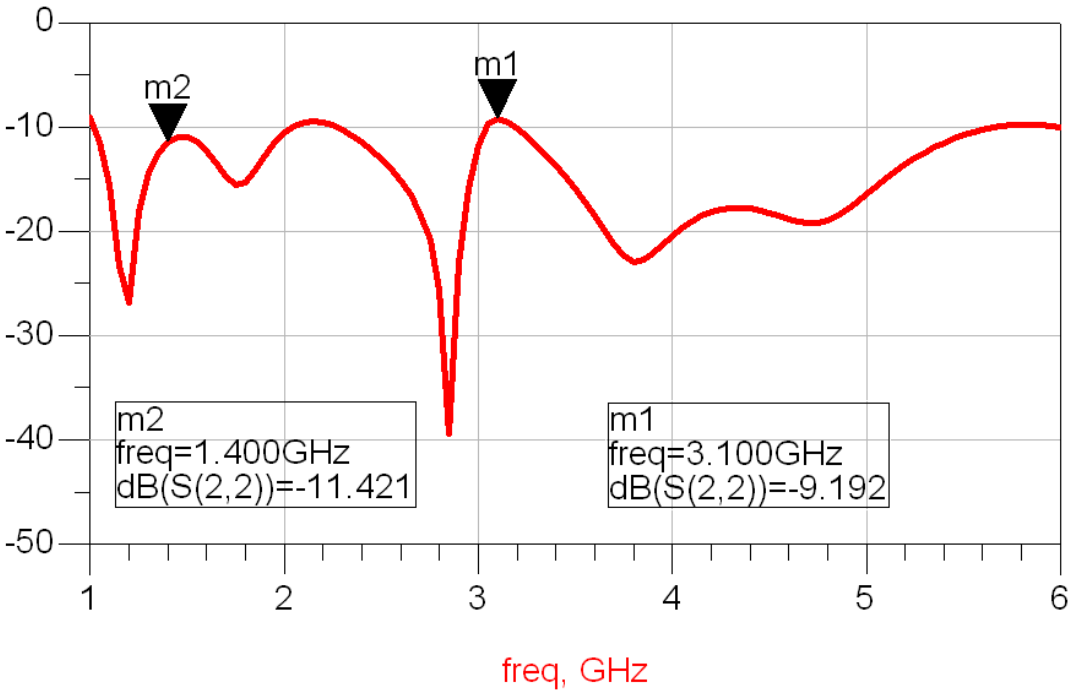


Figure 4-30 Output return loss for 1-6 GHz amplifier

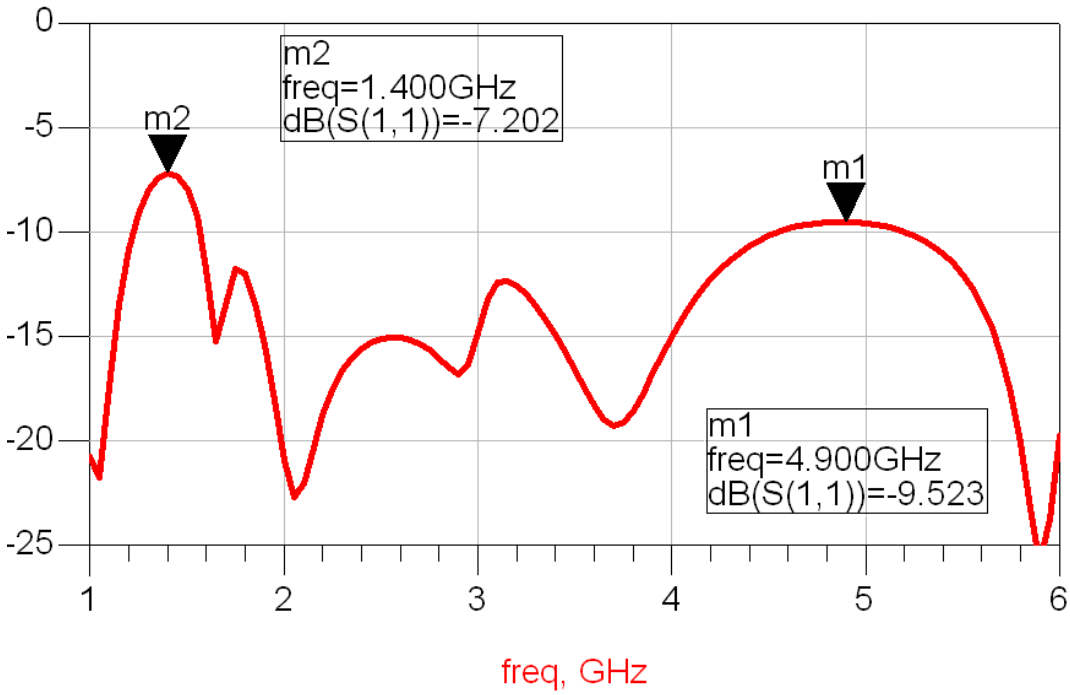


Figure 4-31 Input return loss for 1-6 GHz amplifier

Simulation results show a promising amplifier for implementation. Different techniques may be employed in order to observe these characteristics. However since the inductances are not too low, it would be better to employ inductors for simplicity. Using transmission lines instead of inductors may yield undesirable responses and may cause inter-channel interaction. Capacitances in the tubular filters and the high-pas match section may be converted to transmission lines; since the values are too low to be implemented in surface mount technology.

CHAPTER 5

CONCLUSIONS

In this thesis work, a new distributed amplifier topology is introduced and discussed. New DA topology depends on dividing the defined frequency spectrum into frequency channels and amplifying afterwards. The channelized and amplified signals are then combined at the output without switching any channel or turning off any part. Using this topology, a 0.1-1 GHz three channel amplifier with a gain of 14.5±0.6 dB is designed, fabricated and measured. The same topology is employed to design and implement a 0.1-1 GHz amplifier with five channels for 0.1-1 GHz. This five channel amplifier has a gain of 14±2.5 dB and return losses lower than -6.5 dB. The procedure is also applied to design a 1-6 GHz amplifier with a gain of 10.5±0.5 dB by employing three channels; however this three channel amplifier is not implemented.

Broadband amplification has been the focus of researchers for years. As wireless technology demands increase, wider bandwidth amplifiers with higher gains are required. In years, researchers have developed methods to design broadband amplifiers. Among these, compensating matching topology, feedback topology, balanced amplifier and distributed amplifiers has caught much of the attention. The first three methods among the mentioned above, achieves broadband operation by mismatching and/or reducing the gain in some way. These three methods do not increase the gain-bandwidth product. On the other hand, distributed amplifier enhances the operational bandwidth by employing a different scheme. The constraint for broadband operation comes from the input and output capacitances

of the transistors. DA topology merges these capacitors into artificial input and output transmission lines; thus limitation on bandwidth is eliminated.

DA is an ingenious method to enhance the bandwidth of an amplifier; however it has some disadvantages that should be considered. First of all, gain that can be extracted from a DA is limited due to the lossy characteristic of the transmission lines. Even though the number of transistors increases, gain does not increase after a certain point. One important drawback of the DAs is the low efficiency compared to other topologies. For a power amplifier efficiency is one of the main concerns; thus DA brings up efficiency problem for large signal applications.

Considering the disadvantages associated with DA, a new topology is employed for distributed amplification. The proposed topology distributes the signal according to its frequency and then amplifies it. For dividing the frequency spectrum into channels different de-multiplexer topologies are employed. Amplification is obtained with single-stage feedback transistor amplifiers and then combining the channelized and amplified signals are done via a multiplexer. Frequency spectrum is divided contiguously, i.e., channels' -3 dB corner frequencies meet; thus when channels are added up at the output, a flat response is obtained. The problem with this type of configuration comes from the phases at filter corners of each amplifier section. Since the signals are added up, phases should be synchronized for a flat response.

First amplifier with this topology employs three channels and lumped de-multiplexer and multiplexer. Lumped band-pass Butterworth filters are used and combined to obtain de-multiplexer and multiplexer. Amplifying paths are optimized for phase synchronization by tuning the element values of matching. The designed amplifier is fabricated in ASELSAN Inc. facilities in Hg-Tech FR4 PCB with surface mount components. Fabricated amplifier is measured in a calibrated set-up in ASELSAN Inc. A 0.1-1 GHz three channel amplifier with 14.5±0.6 dB amplifier is obtained.

Proposed topology is applied to a 0.1-1 GHz five channel amplifier whose results are obtained for simulation environment and then implemented. The frequency spectrum of interest is divided logarithmically into five. Tubular filter connected

manifold scheme is preferred for de-multiplexer and multiplexer; whereas high-pass lumped matching is selected for amplifying sections. Matching sections in the amplifying paths are optimized for phase synchronization. Simulation results indicate a gain of 21±1 dB with good return losses for input and output.

After simulation phases, resultant schematic is implemented on FR4 PCB at ASELSAN Inc.'s factory. Measurements show that an amplifier for 0.1-1 GHz with a gain of 14±2.5 dB and return losses lower than -6.5 dB is obtained. Gain fluctuations associated with this design is due to inevitable phase characteristics of the tubular filter. The difference between the simulated and measured results stems from the losses associated especially for the de-multiplexer and multiplexer.

Third amplifier based on this topology operates at 1-6 GHz with three channels. De-multiplexer is designed with tubular filters; whereas matching is designed on lumped band-pass basis. A distributed type manifold multiplexer, at which phase synchronization is achieved, is employed at the output. Phase synchronization is obtained by optimizing the widths and lengths of each section of the manifold. A gain of 10.5±0.5 dB is obtained in simulation environment.

Results indicate that this topology may include any number of stages and may operate at any desired frequency range. Gain acquired from this topology is directly related to the transistor gain at that frequency range; thus gain can be adjusted accordingly. Since each channel operates at specific frequency ranges, matching is neatly done. Therefore power amplifiers can easily be designed with this structure. One important aspect is the efficiency associated with this topology, since for low power amplifiers, efficiency is not improved. Since all of the transistors are biased (no switching), all of the amplifying paths draw current, which in turn decreases efficiency. For further improvement a switching mechanism can be designed.

To sum up, new topology is confidently employed in broadband amplifier design, showing good gain return loss results. The topology may be applied for different cases and different frequency ranges. Circuitry can be realized in either surface mount or distributed technology.

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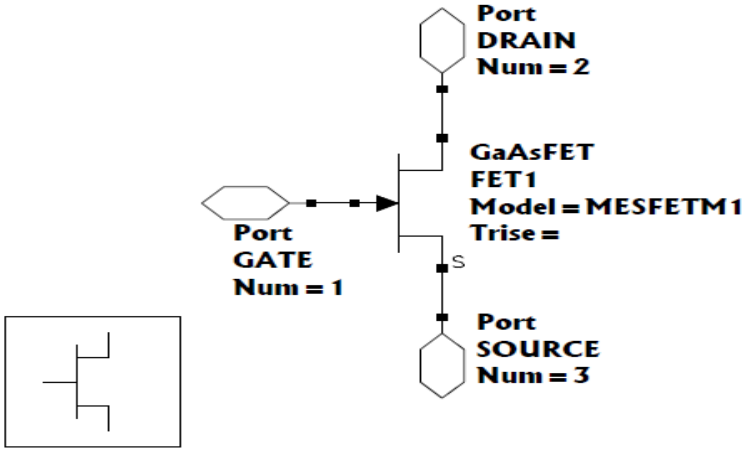
APPENDIX A

Avago Technologies ATF52189 Nonlinear Model

Avago provides S-parameter files and non-linear models for ATF52189. In the design phase, non-linear model is used in order to observe a more realistic response. Figure A-1 displays the die model provided by the company.



Advanced_Curtice2_Model
MESFETM1

NFET = yes	Rf =	Crf = 3.2 F	Eg =
PFET = no	Gscap = 2	Gsfwd =	N =
Vto = 0.318	Cgs = 6.82 pF	Gsrev =	Fnc = 1 MHz
Beta = 3.5	Cgd = 1.07 pF	Gdfwd =	R = 0.08
Lambda = 72e-3	Gdcap = 2	Gdrev =	P = 0.2
Alpha = 13.1	Fc = 0.65	R1 =	C = 0.1
Tau =	Rgd = 1 Ohm	R2 =	Taumdl = no
Tnom = 16.85	Rd = 0.263	Vbi = 0.95	wVgfwd =
Idstc =	Rg = 1.7 Ohm	Vbr =	wBvgs =
Ucrit = -0.72	Rs = 0.084	Vjr =	wBvgd =
Vgexp = 1.91	Ld = 1e-003 nH	Is = 32e-14	wBvds =
Gamds = 1e-4	Lg = 5.347e-002 nH	Ir =	wIdsmax =
Vtotc =	Ls =	Imax =	wPmax =
Betatce =	Cds = 0.912 pF	Imelt =	AllParams =
Rgs = 1 Ohm	Rc = 48.7 Ohm	Xti =	

Figure A-1 Die model of ATF52189

Figure A-2 shows the complete model of ATF52189. In this mode, die model mentioned above is embedded in the box at the middle. Figure A-2 displays the parasitic contributions associated with package of the transistor.

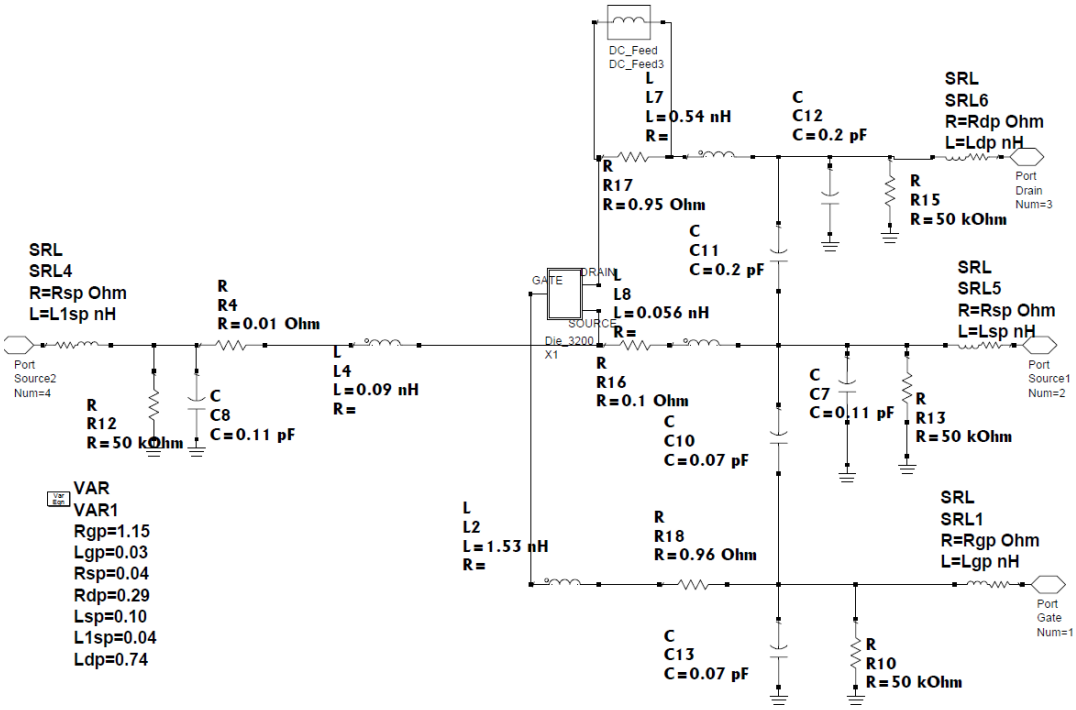


Figure A-2 Nonlinear model of ATF52189

APPENDIX B

Avago Technologies ATF35143 Nonlinear Model

Figure A-3 displays the die model employed for ATF35143. Figure A-4 shows the nonlinear model of ATF35143 when parasitic contributions are considered.

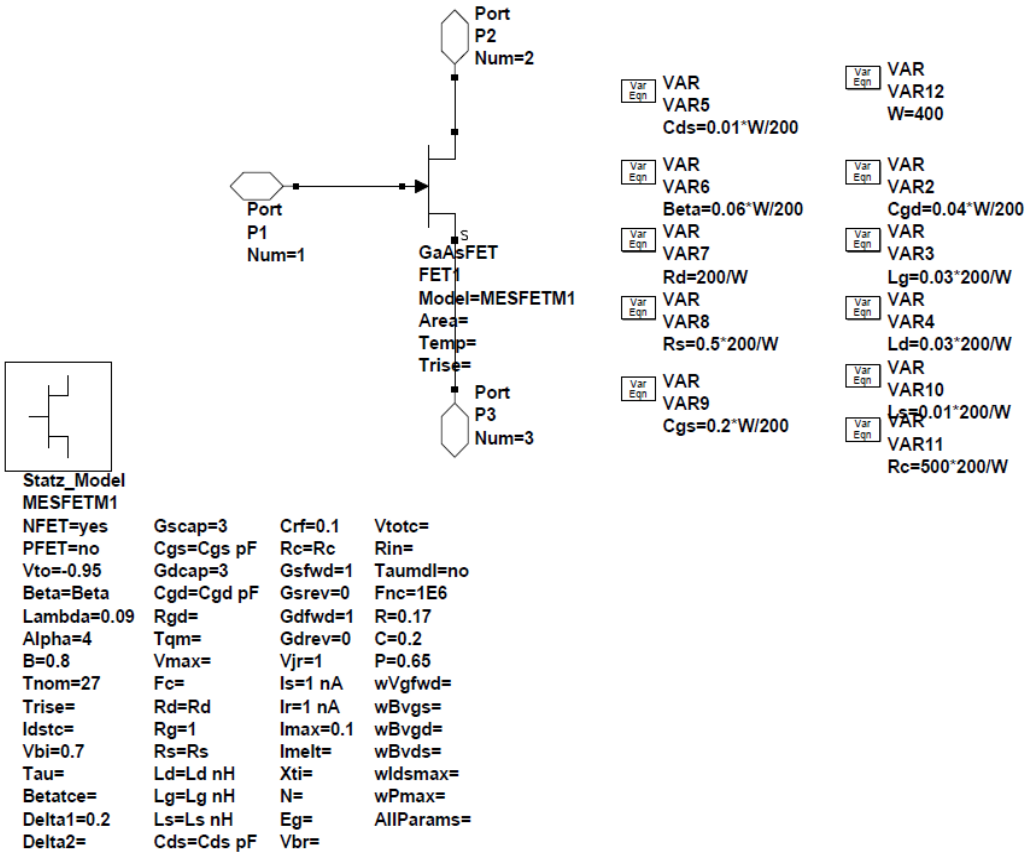


Figure B-1 Die model for ATF35143

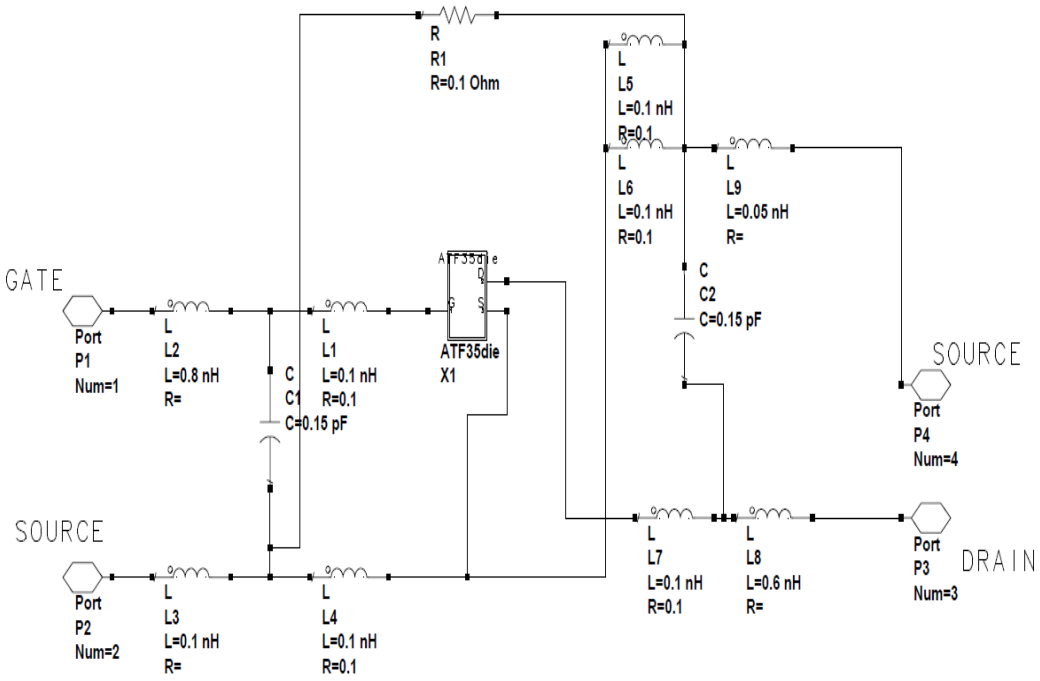


Figure B-2 Nonlinear model for ATF35143

APPENDIX C

Schematic for ATF52189 with RF chokes and DC blocks

For all three circuit configurations, transistors are employed as self-biased. Gate voltage and drain voltage is kept constant during the whole process. Figure C.1 displays a sample schematic from the three channel 0.1-1 GHz amplifier.

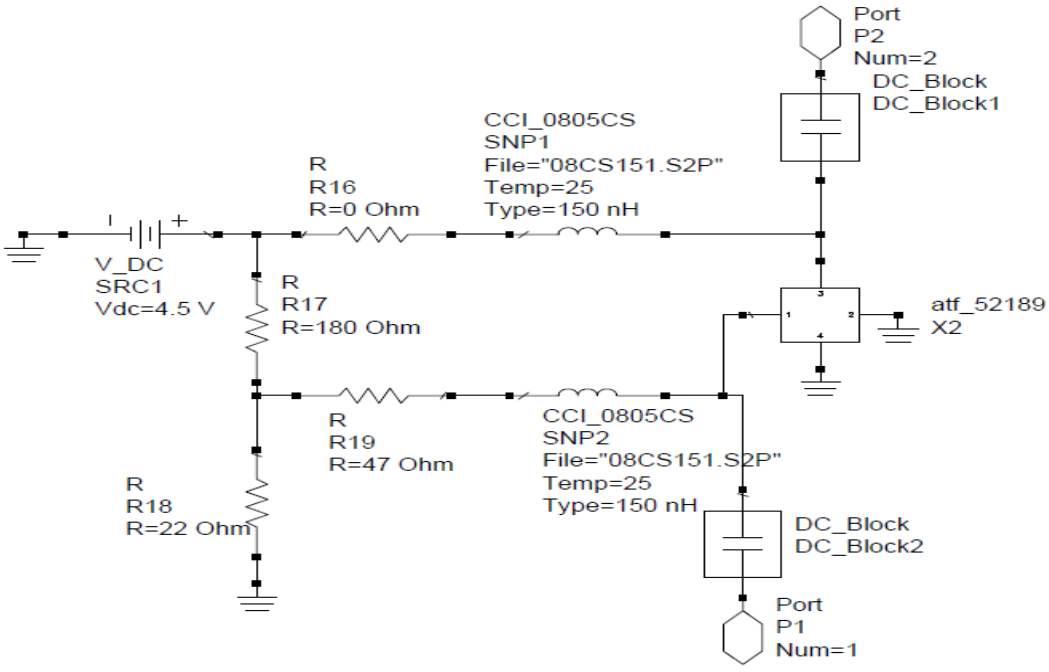


Figure C-1 Circuit schematic for ATF52189