BROADBAND PHASE SHIFTER REALIZATION WITH SURFACE MICROMACHINED LUMPED COMPONENTS

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ABSTRACT

BROADBAND PHASE SHIFTER REALIZATION WITH SURFACE MICROMACHINED LUMPED COMPONENTS

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Phase Shifters are one of the most important building cells of the applications in microwave and millimeter-wave range, especially for communications and radar applications; to steer the main beam for electronic scanning. This thesis includes all of the stages starting from the theoretical design stage to the measurements of the phase shifters. In detail, all-pass network phase shifter configuration is used to achieve broadband and ultra wide-band differential phase characteristics. For these reasons, 1 to 2 GHz, 2 to 4 GHz, and 3 to 6 GHz 4-bit, 22.5° phase resolution phase shifter realization with surface micromachined lumped components are designed, simulated, fabricated and measured. Basic building blocks of the phase shifters, i.e., surface micromachined lumped components, square planar spiral inductors and Metal-Insulator-Metal capacitors are designed with EM simulation and lumped equivalent model extractions. The validation of the designed square planar spiral inductors is done with fabrication and measurement steps, very low error, below 1%, between the designs and fabricated samples are observed. Using this knowledge on lumped elements finally phase shifters are designed with surface micromachined lumped components, fabricated using an in house technology provided by METU-MEMS facilities, RF MEMS group. Low phase rms error, good return and insertion loss considerations are aimed, and achieved.

In addition to the main work of this thesis, a generalized theoretical calculation method for 2^{n-1} number of stages all-pass network phase shifters is presented for the first time in literature. A different, new, broadband, and combined phase shifter topology using two-stage all-pass filters is presented. Moreover, the implementation of this idea is proved to be practical to 3 to 6 GHz 5.625° and 11.25° combined phase shifter.

A new approach for stage numbers other than power of 2 is indicated, which is different from what is already presented in the literature. An example practical implementation results are provided for the three-stage 4-bit 1 to 6 GHz phase shifter.

Also, a small improvement in SRF of the high inductance valued inductors is achieved with the mitering of the corners of square planar spiral inductors. Comparison of the measured data between the normal inductors and mitered versions shows that the first SRF of the inductors are increased about 80 MHz, and second SRF of the inductors are increased about 200 MHz.

KEYWORDS: Phase Shifters, All-Pass Network, Surface Micromachining, Broadband, Ultra Wide-Band, Square Planar Spiral Inductors, Metal-Insulator-Metal Capacitors, Mitered Corners

ÖZ

YÜZEY MİKRO İŞLENMİŞ TOPLU ELEMANLI

GENİŞ BANT FAZ KAYDIRICI GERÇEKLEŞTİRİLMESİ

Tokgöz, Korkut Kaan
Yüksek Lisans, Elektrik ve Elektronik Mühendisliği Bölümü
Tez Yöneticisi: Doç. Dr. Şimşek Demir

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Faz kaydırıcılar elektronik tarama için ana hüzmenin yönlendirimesinde mikrodalga ve milimetre dalga frekanslarında özellikle, iletişim ve radar uygulamalarında kullanılan önemli yapı taşlarındandır. Bu tez, faz kaydırıcıların kuramsal tasarım aşamasından başlayıp ölçümlerine kadar süren tüm aşamaları kapsamaktadır. Ayrıntılı olarak, tüm geçiren süzgeç ağları faz kaydırıcı düzenleşimini geniş bantlı ve engin frekans bantlı ayrımsal faz özelliklerini elde etmek için kullanılmıştır. Bu nedenle 1 GHz' den 2 GHz' e, 2 GHz' den 4 GHz' e, ve 3 GHz' den 6 GHz' e kadar 4-bitli, 22.5° faz çözünürlüklü, faz kaydırıcıların gerçekleştirilmesinde yüzey mikro işlenmiş toplu elemanlı tasarlanmış, bilgisayar programları yardımı ile benzetilmiş, üretilmiş ve ölçülmüştür. Faz kaydırıcıların temel yapı taşları yüzey mikro işlenmiş toplu elemanlar, düzlemsel kare sarmal endüktörler ve metal-yalıtkan-metal sığaçlar olup elektromanyetik benzetimleri ve toplu devre elemanlı eşdeğer modellerinin özütlenmeleri ile tasarlanmıştır. Tasarlanan düzlemsel kare sarmal endüktörlerin onaylanması üretim ve ölçüm aşamalarında yapılmış olup tasarım ile üretilen örnekler arasında % 1 'in altında çok düşük hata payı gözlemlenmştir. Bu bilgilerin toplu elemanlar üzerinde kullanılmasıyla nihayetinde yüzey mikro işleme ile şekillendirilen toplu elemanlı olan faz kaydırıcıları kendi imkanlarımızla, ODTÜ – MEMS tesislerindeki teknoloji ile RF MEMS grubu tarafından üretilmiştir. Düşük etkin değer faz hatası, düşük geri dönüş

kaybı ve düşük araya giriş kayıplarının göz önüne alınması hedeflenmiş ve bu hedefe ulaşılmıştır.

Bu tezin ana çalışmasına ilaveten, tüm geçiren süzgeç ağları faz kaydırıcılarının 2^{n-1} kat aşamaları için genelleştirilmiş teorik bir hesaplama yöntemi, bu tezde ilk kez literatüre kazandırılmıştır. Değişik yeni, geniş bantlı ve kombine faz kaydırıcısı topolojisi kullanılarak iki aşamalı tüm geçiren süzgeçler sunulmuştur. Dahası bu yeni fikrin 3 GHz'den 6 GHz'e kadar 5.625° ve 11.25° kombine faz kaydırıcının uygulanmasında çok kolaylık sağladığı kanıtlanmıştır. Mevcut literatürde var olandan farklı olarak aşama sayılarının 2'nin kuvvetlerinin dışında olmasına dair yeni bir yaklaşım belirtilmiştir. Pratik bir uygulama örneği üç-aşamalı 4-bitli 1 GHz' den 6 GHz'e kadar faz kaydırıcısıdır.

Düzlemsel kare sarmal endüktörler köşelerinin kesilmesiyle yüksek endüktans değeri olan endüktörlerin doğal rezonans frekanslarında küçük bir iyileştirme de elde edilmiştir. Ölçülmüş verilerin sıradan endükterlerle ve köşeleri kesilmiş indüktörlerin karşılaştırılması paralel rezonans frekansının yaklaşık 80 MHz ve seri rezonans frekansının yaklaşık 200 MHz arttığını göstermektedir.

ANAHTAR KELİMELER: Faz kaydırıcılar, Tüm Geçiren Süzgeç Ağları, Yüzey Mikro İşleme, Geniş Bantlı, Engin Frekans Bantlı, Düzlemsel Kare Sarmal Endüktör, Metal-Yalıtkan-Metal Sığaç, Kesilmiş Köşeli Düzlemsel Sarmal Endüktör

Dedicated to My Family

and

My Wife

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CHAPTER 1

INTRODUCTION

1.1 Preface

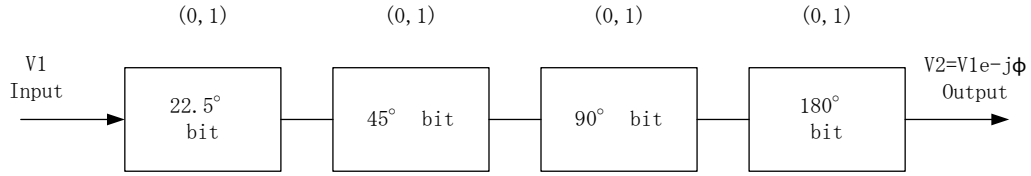
Phase shifters are key components in phased array antennas for telecommunications and radar systems, microwave instrumentation and measurement systems, and industrial applications. There, sure, are a few categorization methods of the phase shifters. For instance, in terms of design requirements, the phase shifters can be categorized as constant phase and linear phase versus frequency. The constant-phase design phase shifters are mainly used in radar applications where signal processing needed, wideband communications systems and components; such as, SSB mixers, vector modulators, balanced amplifiers, and etc. and high-precision instrumentation systems. On the other hand, the linear-phase designs are employed mostly in phased array applications as true-time-delay networks.

Another categorization of phase shifters is to classify them as mechanical and electronic depending on tuning. Before the advent of electronically variable phase shifters, almost all phase shifters were implemented as mechanical for both fixed and variable phase shifts. The mechanical phase shifters are generally constructed in coaxial line or metallic waveguides. The insertion phase of the device is varied by means of mechanical tuning, such as a variation in the physical length of the line or rotation-displacement of a dielectric slab inside a waveguide. As compared with the electronic phase shifters, mechanical phase shifters are rugged, simple to fabricate, and have very low loss (typically 0.5 dB for a 360°phase shift). The mechanical phase

shifters also offer an inexpensive option. On the other hand, electronic phase shifters have significant advantage on mechanical phase shifters in terms of volume requirements in phased array antenna systems for inertialess scanning [3].

1.2 Phase Shifters

Depending on the type of operation, phase shifters can be classified as analog or digital, having reciprocal or nonreciprocal characteristics. The analog phase shifters, as the name refers, are used to control the insertion phase within 0 to 360°. The digital phase shifters are used to produce discrete phase delays, which are selected by means of switches. A digital phase shifter generally consists of a cascade of several phase bits with phase shifts incremented in binary steps. For example, in an n-bit 360° phase shifter, the entire range of 0 to 360° is covered in 2^n steps. The smallest phase bit is $(360/2^n)$ degrees and that of the largest phase bit is 180°. As an example, a schematic of a 4-bit phase shifter and switching sequence are given in Figure 1-1. By switching the phase bits in suitable combinations, phase shift can be incremented in steps of 22.5° to cover the full range of 0 to 360° in sixteen steps.



Switching State	Output Phase, Φ (Degrees)	Differential Phase Shift, Δϕ (Degrees)
0 0 0 0	Φ_0 (Reference State)	0°
1 0 0 0	Φ_0+22.5°	22.5°
0 1 0 0	Φ_0+45°	45°
1 1 0 0	Φ_0+67.5°	67.5°
0 0 1 0	Φ_0+90°	90°
1 0 1 0	Φ_0+112.5°	112.5°
0 1 1 0	Φ_0+135°	135°
1 1 1 0	Φ_0+157.5°	157.5°
0 0 0 1	Φ_0+180°	180°
1 0 0 1	Φ_0+202.5°	202.5°
0 1 0 1	Φ_0+225°	225°
1 1 0 1	Φ_0+247.5°	247.5°
0 0 1 1	Φ_0+270°	270°
1 0 1 1	Φ_0+292.5°	292.5°
0 1 1 1	Φ_0+315°	315°
1 1 1 1	Φ_0+337.5°	337.5°

Figure 1-1. Schematic of 4-bit phase shifter and binary switching scheme.

An ideal reciprocal phase shifter (RPS) offers the same insertion phase for either direction of the RF signal. The scattering matrix of a reciprocal phase shifters is as follows,

$$[S]_{RPS}\begin{bmatrix} 0 & e^{-j\phi} \\ e^{-j\phi} & 0 \end{bmatrix}$$

A nonreciprocal phase shifter (NRPS) offers different insertion phases to waves traveling in opposite directions.

$$[S]_{NRPS}\begin{bmatrix} 0 & e^{-j\phi_1} \\ e^{-j\phi_2} & 0 \end{bmatrix}$$

The most commonly used NRPS is the ferrite phase shifter, in which the effect of reversing the direction of magnetization is the same as that of reversing the direction of propagation. Thus if the differential phase shift for a given direction of propagation is $\Delta\phi$, then with a reversal in the direction of propagation the differential phase shift is $-\Delta\phi$.

Depending on the type of electronic control medium or mechanism adopted, these phase shifters may be classified as ferrite, semiconductor device, active FET, or bulk semiconductor phase shifters. The surface acoustic wave and magneto-static-wave delay lines are true time-delay devices, and they are gaining increasing relevance for real-time signal processing at microwave frequencies. Ferrite based phase shifters are generally used in arrays where low insertion loss is required (about 1 dB) and slow-switching time (150 us) is permissible. However, these phase shifters are not suitable for the implementation of low profile and low weight phased arrays. FET based, PIN based and varactor diode based phase shifters are the semiconductor alternatives for phase shifter. They propose low cost, low weight and planar solutions to phased array systems.

The basis of operation of all ferrite devices is the interaction between the electromagnetic waves and the spinning electrons in a magnetized ferrite. In a magnetized ferrite, the magnetic dipole moment of the spinning electron precesses about the applied field, and its precession frequency is directly proportional to the magnitude of this dc magnetic field. The permeability of the ferrite takes the form of a tensor, the elements of which are a function of the applied magnetic field. When the magnitude or direction of the magnetic field is changed, the permeability of the ferrite changes, thereby, changing the propagation constant of the electromagnetic wave. Phase shift is a consequence of the change in the propagation constant brought about by electronically controlling the applied magnetic field.

Ferrite phase shifters have been realized mostly in waveguide geometry. Other geometries, such as the coaxial line, stripline, and microstrip line, have been employed as well but to a much lesser extent. These phase shifters can be designed

to operate either in analog or digital mode, having either reciprocal or nonreciprocal characteristics.

Semiconductor junction devices are used as electronic control elements. These phase shifters are all reciprocal in nature but can be classified as digital or analog, depending on whether the control element is used as an electronic switch or a continuously variable reactance. Examples of devices that can act as electronic switches are the PIN diode, GaAs FET, and the Schottky diodes. Of these, the first two are used most extensively, the PIN diode in planar hybrid phase shifters and the FET in monolithic phase shifters. For analog operation, the varactor diode is used most commonly. The PIN diode operates as an electronic on-off switch when switched between a fixed forward bias and a reverse bias. Under forward bias, the diode offers very low impedance thus approximating a short circuit (on-state), and under reverse bias, it offers very high reactive impedance approximating an open circuit (off-state).

The field effect transistor (FET) is a three terminal device which is used as a two-terminal switch (between source and drain) by applying a bias voltage to the gate. With a large negative bias (larger in magnitude than the pinch-off voltage) at the gate, the FET switch represents a high-impedance state (off state); and with zero gate bias, it represents a low-impedance state (on-state). Note that under the off-state, the PIN diode offers a high-capacitive reactance whereas a FET offers a high resistance in parallel with a capacitive reactance on the order of 50 Ω at X-band frequencies. Hence, to achieve the switching action, this capacitance is resonated with an external inductance or its effect is included in the impedance matching sections. Phase shifters that amplify the RF signal in addition to the phase shift are known as “active” phase shifters. The GaAs metal semiconductor FET (MESFET), in particular, the dual-gate MESFET, is the key control element that enables this dual function. Both analog and digital phase shifters have been realized.

Analog type semiconductor phase shifters in MIC configuration commonly make use of varactor diodes as control elements. The varactor diode provides a wide reactance range as a function of the negative-bias voltage. Varactor diode phase shifters have

been realized in the following two circuit forms: the hybrid coupled and the loaded line. A hybrid coupled circuit with planar varactor diodes also has been used to realize analog phase shifters in monolithic chip form.

The use of bulk semiconductor elements is reported to be an attractive practical alternative to the use of semiconductor junction devices in realizing phase shifters at millimeter-wave frequencies. It offers higher bandwidth and higher power handling capacity. In bulk semiconductor phase shifters, phase control is achieved by dynamically varying the conductive properties of electron-hole plasma in a semiconductor material. Plasma is created either through free carrier injection via contacts or optical illumination.

There are certain requirements for a phase shifter to provide a satisfactory operation. The electrical performance of a phase shifter generally is specified in terms of insertion loss, operating bandwidth, phase error, and power handling capability. In electronically variable phase shifters, two other parameters, switching time and drive power, are specified as well. For all applications, it is desirable to have the insertion loss, drive power, and phase error as low as possible. Regarding the bandwidth and power handling capability, it generally is more cost effective to design phase shifters separately for narrowband and broadband, and for low-power and high-power applications. The physical size and weight of the phase shifter should be minimized for use in mobile and airborne systems, whereas for ground based systems, the requirement can be relaxed [3].

The phase shifters are implemented in several different topologies, such as; switched line, reflection-type, loaded-line, high-pass/low-pass, and etc. The switched line and reflection types of phase shifters are most suitable for constant time delay, while all four types mentioned above can be modified into constant phase shift devices. The mentioned topologies will be investigated basically respectively.

As it can be seen in Figure 1-2, switched line phase shifter circuit needs two SPDT switches. The lower part of the circuit is the reference arm of the phase shifter and

with a length l, and the upper arm has a length of $l + \Delta l$. Accordingly the upper arm has a phase delay longer than the reference arm, i.e. the lower arm and the differential phase shift is given by $\Delta\phi = 2\pi\Delta l/\lambda$..

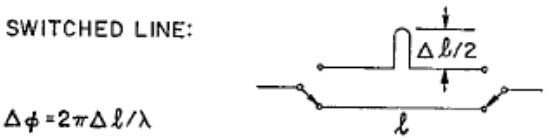


Figure 1-2. Switched Line Phase Shifter Circuit [2].

The reference length l must be carefully selected in order to avoid phase errors and high or unbalanced insertion losses. When the effective length is $\lambda/2$ or its multiples, large errors occur. The electrical length mentioned above is the electrical length plus the equivalent length of the switches. It is mentioned before that the switched line phase shifter is a time-delay device, so phase shift will be proportional to frequency. In order to achieve wide-band properties for this type phase shifter one can use Schiffman phase shifter in one of the arms.

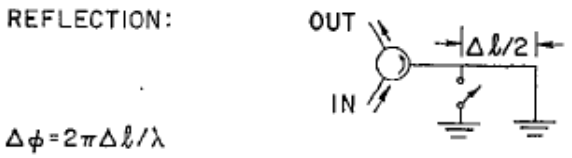


Figure 1-3. Reflection Type Phase Shifter Circuit [2].

A reflection type phase shifter can be made of a switch with a short circuit behind it, as shown in Figure 1-3, a series switch with an open circuit behind it, or a lumped circuit including switch parasitics terminating the line. The reflection type phase shifter can be very useful in phased-array radar applications with the switches backed up by lengths transmission line that they are time-delay devices. On the other hand, the reflection type phase shifters designed with lumped elements can be made to give constant phase shift. There should be problems according to the mismatches intervening between the terminating impedance and the perfect circulator as can be seen in Figure 1-3. Speaking of the circulator the internal reflections is also important when considering the phase errors occurred due to the imperfections of the circuit.

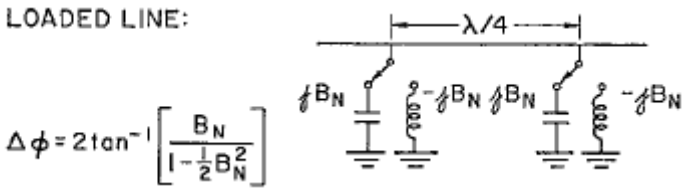


Figure 1-4. The Loaded Line Phase Shifter Circuit [2].

The loaded line phase shifter can be operated due to the capacitors or inductors periodically load the transmission line. One can find the differential phase shift with computing the normalized ABCD matrix of the overall circuit, then finding the S_{21} of the overall circuit. There certainly are a few ways to load the line. The followings may be some examples to them: switching with stubs, switching with lumped element diodes, etc.

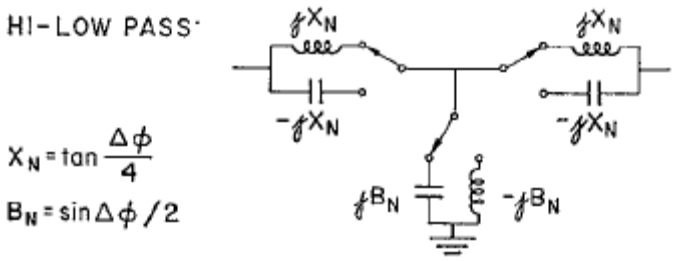


Figure 1-5. The High-Pass/Low-Pass Phase Shifter Circuit [2].

The last circuit topology mentioned is the high-pass/low-pass phase shifter circuit as can be seen in Figure 1-5. A low-pass filter comprised of series inductors and shunt capacitors provides phase delay to signals passing through it, and a high-pass filter comprised of series capacitors and shunt inductors provides phase advance. After some theoretical calculations one can find that $X_N = tan\left(\frac{\Delta\phi}{4}\right)$ and $B_N = sin\left(\frac{\Delta\phi}{2}\right)$ in order to match the circuit naturally. As frequency is increased, in the low-pass state, the series reactance increases proportional to frequency and the shunt reactance decreases inversely proportional to frequency. Therefore phase delay is increased. On the other hand, in the high-pass state, the series reactance decreases with increasing frequency and the shunt reactance increases, so the phase advance decreases. The

net effect is that the phase shifter tends to stay matched as frequency is increased, and phase delay increase in the low-pass state is compensated for by phase advance decrease in the high-pass state [2].

1.3 Objective of the Thesis

As already mentioned above, phase shifters are key components, and becoming more important with increased complexity in the systems. Recent cellular and mobile communication advancements prove the importance of the phase shifters. Moreover, constant phase broadband phase shifter usage is gaining acceleration from the beginning of their introduction [1], due to the extra features needed in Radar and communication systems.

The purpose of the thesis is to design, fabricate and measure broadband planar type phase shifter constructed with all-pass networks with characteristics of low cost, low circuit size, high performance. This work aims to achieve low loss, high return loss, and low phase error for the designed phase shift bits.

The designed, fabricated and measured components are 1 to 2 GHz, 2 to 4 GHz, and 3 to 6 GHz; 22.5°, 45°, 90°, and 180° phase shift bits with three different variations in the layout. For a successful all-pass network broadband phase shifters, studies on lumped elements in planar fabrications, i.e., surface micromachining, thin film, thick film, and etc. is a must to achieve high performance circuits. For that reason, square planar spiral inductors are in depth studied. The fabricated and designed inductor comparisons are provided to fully understand the performances of these components while achieving final phase shifter practical designs.

In addition to these, some improved ideas are applied for different topics. Namely; increasing the SRF of the inductors for ultra wide-band applications, improved theoretical approach to all-pass network phase shifter, and new combined phase shifter to achieve high resolution for the phase shifter.

1.4 Thesis Outline

Organization of the thesis can be summarized as follows;

In Chapter 2, a specific literature review on broadband planar type phase shifter is given in detail to understand the different circuit topologies, different fabrication methods related to the performances of the phase shifters.

Then in Chapter 3, the theoretical calculation method of lumped elements for one-stage, and two-stage all-pass network phase shifters is given, which is presented in literature before. In this work, only 4-bit designs are introduced. In addition to this, for the first time in literature the design parameters are optimally found considering the bandwidth of the phase shifters. Moreover, the design parameter values are extended to one-stage and two-stage all-pass network phase shifters bit-5 and bit-6, i.e., 11.25° and 5.625°. For these phase shift bits, also, the design parameters are optimally found, and presented in this thesis. A generalized formulation methodology for 2^{n-1} number of stages is presented for the first time in literature. In this methodology, briefly, from the known first inductor formulation all other inductors' formulations are found. After that the overall differential phase shift formula is found and the design parameters are optimally found for different bandwidth values. It is shown that for a sixteen-stage all-pass network phase shifter the bandwidth can be as large as 500:1. The phase shift bandwidth can be much larger than this case by increasing the stage numbers. At the end of third chapter, the ideal lumped element values are calculated and presented for different octave and multi-octave band phase shifters.

Chapter 4 covers the design, fabrication and measurements of the used lumped components; namely, square planar spiral inductors, and metal-insulator-metal capacitors. The design methodology of lumped square planar spiral inductors are described and validated with the measurements. The process variation cases are investigated for these components to ensure the tolerances of the fabricated inductors. An idea of mitering the corners of the square planar spiral inductors is

presented to increase the maximum quality factor value as well as the SRF values. The increased SRF values for the same geometry for mitered inductors and normal ones are proved with measurements. Note that the improvements a little bit low. The design, and lumped equivalent modeling of MIM capacitors are discussed at the end of this chapter.

Chapter 5 provides the practical design of two-stage 4-bit 1 to 2 GHz, 2 to 4 GHz, and 3 to 6 GHz phase shifters; and three-stage 4-bit 1 to 6 GHz phase shifter. The design methodology is described in detail for the sake of simplicity just for 1 to 2 GHz 180° phase shift bit. For the other three phase shift bits for 1 to 2 GHz phase shifter only the geometrical specifications of the used lumped elements are given together with lumped equivalent model parameters and quality factor related calculations. For the other phase shifter for two-stage design the details are provided in appendices, but the overall phase shifter design results for sixteen states are provided in terms of return loss, insertion loss, and differential phases together with the data of rms phase, rms phase error values, and maximum phase errors. For the 1 to 6 GHz 4-bit three-stage all-pass network phase shifter only the practical phase results are provided. Other needed specifications are provided numerically. A new circuit concept for combined phase shifter is explained. This new circuit provides an SPDT-less differential phase shift for two states for the low phase states; such as 5.625° and 11.25° phase shift bits. With this new method, the insertion loss is decreased about 4 dB from the conventional method, cost is decreased, and the circuit size is decreased compared with the conventional method.

In Chapter 6, the three variations for each phase shift bit, i.e. 1 to 2 GHz, 2 to 4 GHz, and 3 to 6 GHz 4 bit phase shifters are briefly described. The fabrication of the phase shift bits is summarized. For measurement purposes of these phase shift bits, post-production procedures are needed which are also described. The measured phase shift bits are presented in comparison with their related practical design results.

Finally, conclusions of the thesis, related future works, and some suggestions are given in Chapter 7.

CHAPTER 2

LITERATURE REVIEW ON BROADBAND PLANAR PHASE SHIFTERS

In this part of the thesis, a brief review of planar phase shifters will be given. There are lots of phase shifters designed and implemented up to date, such as ferrite phase shifters, mechanical phase shifters, semiconductor phase shifters and etc. [3]. However, in this part the investigated phase shifters are of planar type, in order to go deeper in to the specific subject of the thesis. The examined works are mainly concentrated on the switching elements as FETs or PIN diodes, those use couplers as a part of their designs [4]-[7], those use a new technique as artificial left- and right-handed transmission lines [17]-[19] –which will be touched later in details- and as a last work a phase shifter integrated with an LNA [20]. Significant works on this subject are presented in this part of the thesis, in terms of topology, technology, and main measurement results.

As the first example, a broadband phase shifter which employs a 180° digital bit and one or two analog phase shifter sections in order to obtain a full 360° phase shift in 4.5 to 18 GHz band [4] is given. The 180° bit exhibits satisfactory performance over the band, however the analog sections require some additional logic circuitry to achieve better phase shift characteristics. Below in Figure 2-1, one can find the basic building blocks of the wideband 180° phase shifter bit which are the shorted coupled lines and a simple π-network of transmission lines.

After some theoretical manipulations using ABCD parameters, it can be seen that the two networks are exactly equivalent for all frequencies except that the transmission phase difference between the two circuits is exactly 180°. Since the result is

independent of the electrical length, the insertion phase is independent of frequency thus, the wideband characteristics are reached. It is important to indicate that both networks behave like identical band-pass filters.

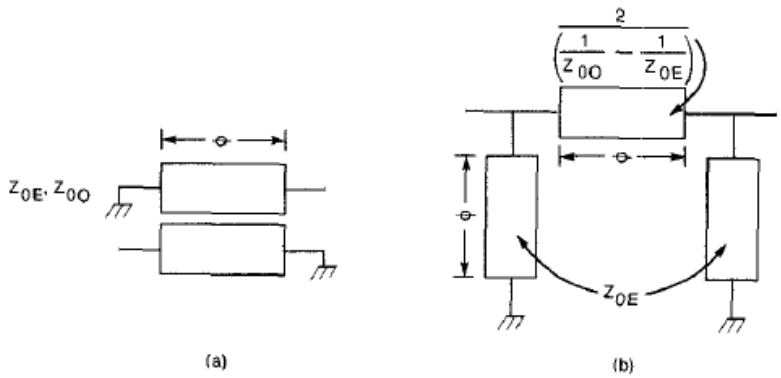


Figure 2-1. (a) Shorted Coupled Lines Sections (b) π Network Transmission Line Section [4].

In this work, the 180° phase shifter bit is constructed on 0.025" thick alumina, and FETs are used as switching elements. The phase shifter bit provided a measured phase shift of 177±7° from 2 to 17 GHz. Measured insertion loss is 2.3 dB±0.8 dB from 4 to 17.5 GHz. The insertion loss difference between the two states is not greater than 1.2 dB and generally less than 0.5 dB from 2 to 17.5 GHz. Return loss is greater than 10 dB from 6 to 18 GHz and greater than 8 dB from 4.5 to 18 GHz. The differential phase seems to be good in the band; however, the insertion loss is a little high, return loss is also acceptable. The analog part of this phase shifter section consists of a pair of varactor diode chips in series with a small bond wire inductance as the terminating elements of a 3dB 90° hybrid coupler. It is claimed that a four finger interdigitated coupler is utilized on a 0.025" in thick alumina. The two varactor diodes, GaAs hyperabrupt chip tuning varactors manufactured by MACOM, are mounted off the substrate on a padestal and connected to the coupler by short bond wires.

Voltage bias for the varactors is provided through chip resistors and DC blocking capacitors are employed at each end of the section. Moreover, at least 160° of phase shifting can be achieved from 4.5 to 18 GHz for a bias voltage range of +0.5 to -30V

with the help of the analog phase shift section. Insertion loss of the section is less than 4.5 dB over the band. Insertion loss variations versus applied voltage (phase shift) are less than 2.0 dB from 7 to 18 GHz and less than 3.5 dB from 4.5 to 18 GHz. The following comments can be given on the results: phase shift seems to be less at the beginning of the overall band, although it seems to be satisfactory for the rest of the band. Insertion loss is not good enough for the overall band and insertion loss variations are high. Some suggestions are mentioned in this work to overcome the improper phase characteristics of the analog phase shifter section; one of these suggestions is to operate only in the most linear portion of the characteristic and accepting less total phase shift per section; i.e. using two analog sections of 90° each, and another approach is to employ a "smart" silicon driver chip incorporating a "look up table" to determine the appropriate voltage to obtain the desired phase shift at any particular frequency. 180° phase shift characteristic is affected negligibly with the introduction of small "on" state FET resistance.

Another work is by Kwon, Lim, and Kang [5], which is a wideband phase shifter consisting of one Lange coupler, four radial stubs and four switching diodes and bias circuits. Below in Figure 2-2, there is a schematic diagram of a hybrid coupled phase shifter with capacitive reflective loads, in which two different pairs of radial stubs are used as the reflective loads of the Lange coupler in order to achieve wideband phase shifting. Four phase shift bits are implemented and tested in this work, 11.25°, 22.5°, 45°, and 90° with maximum measured phase errors of 2.2°, 2.2°, 3.6°, and 5.5° respectively, which are indeed admirable results.

The topology is of reflective type, using a 3 dB 90° hybrid coupler and terminations are capacitors as reflective loads. This typical phase shifter uses two different capacitors, C_1 and C_2. A relative phase change of the input signal is obtained by switching between C_1 and C_2. When C_1 is changed to C_2, the output phase changes by;

$$\phi = 2tan^{-1}\left\{\frac{wZ_0(C_2 - C_1)}{1 + w^2 Z_0^2 C_1 C_2}\right\}$$

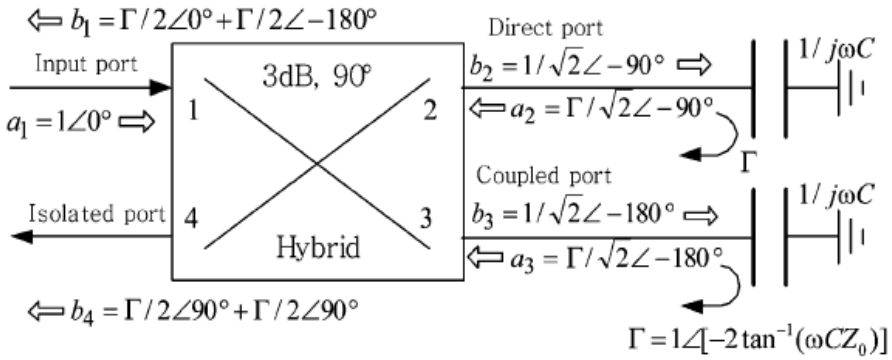


Figure 2-2. Schematic Diagram of a Hybrid Coupled Phase Shifter with Capacitive Reflective Loads [5].

Bandwidth limitations can be investigated from the above equation; the phase difference is proportional to $1/\omega$, for $\omega \gg 1/(Z_0\sqrt{C_1C_2})$ which limits the bandwidth. Radial stubs are the reflective elements, generally used to ground a wideband RF signal. The input impedance of a radial stub can be approximated by a series combination of a capacitor, C and an inductor, L. However, the detailed analysis of the radial stubs is not investigated in this thesis. A phase shifter is implemented on 200 um GaAs substrate. There are important points about the fabrication of the unfolded Lange coupler; such as, the coupling coefficient of the coupler decreases with decrease of the frequency because of the loss of the capacitive coupling between the fingers. Other than that, at a high frequency, this coupling coefficient also decreases because of the conductor loss on the coupler.

The length and the width of the conductors for the coupler are 1600 um and 14 um respectively. The spacing between the conductors is 6 um. For implementation of the radial stubs 3 um thick Au metal layers are electroplated. In order to switch between the radial stubs, HPND-4038 PIN diodes from Agilent are used. Spiral inductors are used to connect the outer arc of the stubs to the ground also providing a DC current path for the diodes. On state inductance of the PIN diode is assumed to be 0.25 nH, and the off state capacitance of PIN diode is assumed to be 0.06 pF. The inductance and the parasitics of the five turn spiral inductor 4.5 nH and 97 fF, respectively. Accounting all of the parasitics gives phase offsets of 0°, -3.5°, -2°, and +8° at the

center frequency and 9°, 10.5°, 16°, and 22° at the band edges, respectively for 11.25°, 22.5°, 45°, and 90° phase shifts. After that, phase shifters are tuned again to give the correct phase shift values. This phase shifter's photograph is given in Figure 2-3.

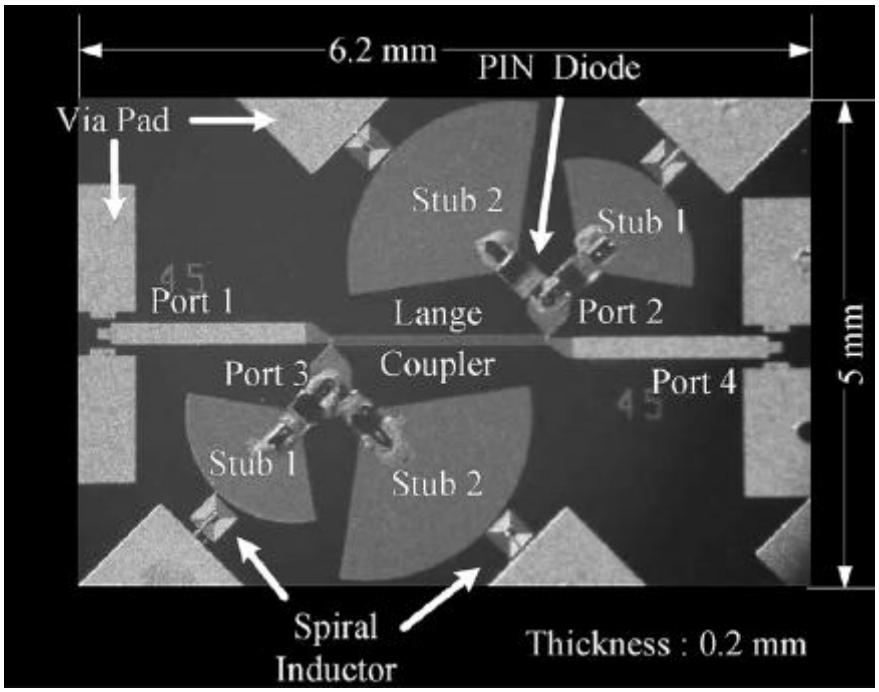


Figure 2-3. Photograph of fabricated 6–18 GHz 45° phase shifter [5].

Insertion loss of one PIN diode is given to be 0.7 dB, and the insertion loss of the phase shifter is not that high in the band. In fact the losses originated from the losses of the PIN diodes, the signal return loss and the conductor loss in the Lange coupler. The worst case return loss in the band is around 10 dB which is an acceptable value.

A significant property about the planar phase shifters (stripline or microstrip) is that they can achieve wideband performance. Coupled transmission lines are one of the basic building blocks to achieve wideband phase shifter performance, since couplers themselves are wideband components. A work by Amin M. Abbosh presents a specially implemented coupler (elliptically implemented), henceforth a different phase shifter [6]. In this phase shifter an elliptical shape for the coupled structure has been chosen because of its ability to achieve an almost constant coupling factor over

an ultra-wideband. In Figure 2-4 and Figure 2-5, the proposed phase shifter configurations are given.

Considering the given configuration, the coupling coefficient and the scattering parameter equations are obtained and then the differential phase shift is found. Phase difference of the output signal compared to the input signal, i.e. the differential phase shift, can be found as follows;

$$\phi_c = 90° - 2tan^{-1}\left\{\frac{\sin\beta_{ef}l}{\sqrt{1-C^2}\cos\beta_{ef}l}\right\}$$

where *C* is the coupling coefficient, and β_{ef} is the effective phase constant in the medium of the coupled structure, it is also shown that the effective phase constant can be found by averaging the even mode phase constant and the odd mode phase constant of the structure. To find the differential phase shift, which can be obtained using the proposed structure, a comparison is made with a reference line. The phase shift caused by a section of microstrip line of physical length l_m is;

$$\phi_m = -\beta_m l_m$$

where β_m is the phase constant of the microstrip transmission line and the microstrip transmission line is assumed to be 50Ω. Therefore the exact differential phase shift is:

$$\Delta\phi = 90° - 2tan^{-1}\left\{\frac{\sin\beta_{ef}l}{\sqrt{1-C^2}\cos\beta_{ef}l}\right\} + \beta_m l_m$$

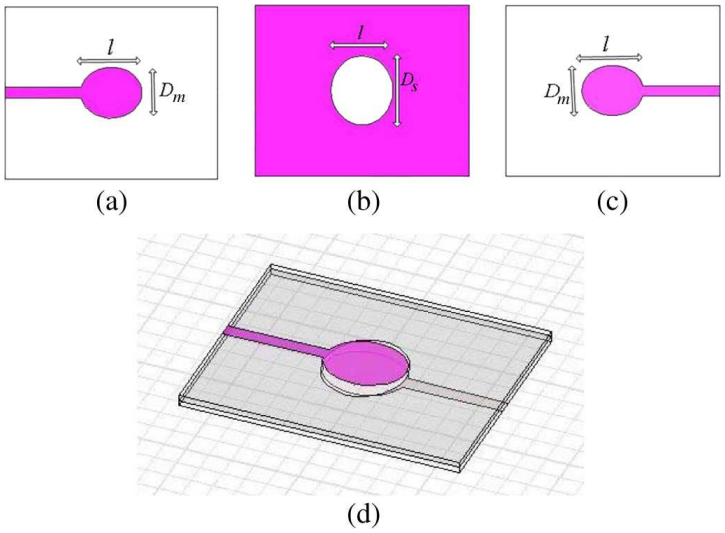


Figure 2-4. Configuration of the proposed phase shifter (a) Top layer (b) Mid layer (c) Bottom layer (d) Whole structure [6].

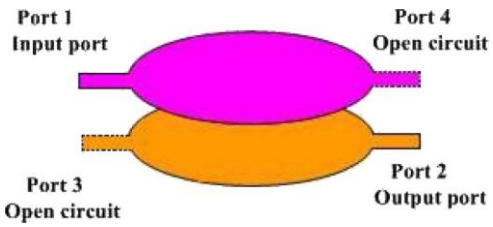


Figure 2-5. Proposed phase shifter as a four-port device with two of the ports open circuited [6].

The substrate is the RO4003C with 3.38 relative permittivity, 508 µm thickness, and 0.0023 loss tangent. In the design stage, elliptical equations are used since the patch is designed to be elliptical. Two phase shift bits are designed with values of 30°, and 45°. In Figure 2-6, one can find a photograph of a fabricated phase shifter.

According to the results, phase shift is measured as 30±2.5° and 45±2.3°, in 3.1 to 10.6 GHz band, return loss is better than almost 15 dB and insertion loss is better than 0.85 dB.

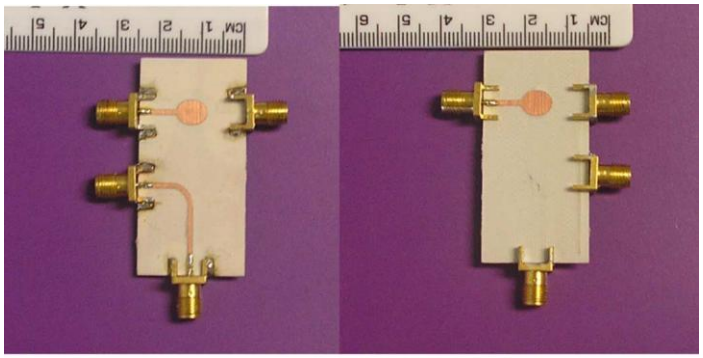


Figure 2-6. One of the manufactured phase shifters. (a) Top layer. (b) Bottom layer. The upper part of (a) and (b) is the phase shifter, where the reference transmission line is shown at the lower part of (a)[6].

Another example of a phase shifter implemented with a coupled line together with parallel stubs, is presented by Eom [7]. The proposed phase shifter consists of a $\lambda/2$ coupled line and parallel $\lambda/8$ open and short stubs which are shunted at the edge points of a coupled line, as it can be seen in Figure 2-7.

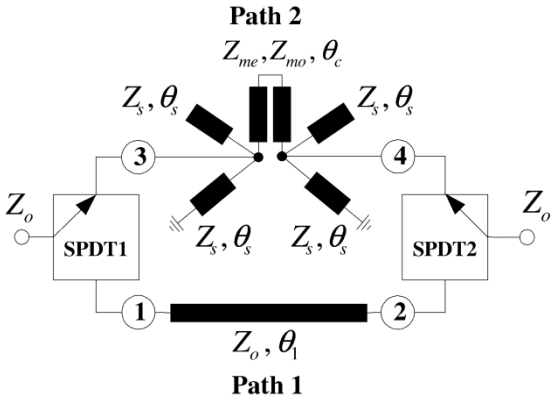


Figure 2-7. The proposed phase shifter consists of a $\lambda/2$ coupled line and parallel $\lambda/8$ open and short stubs [7].

The path 1 is designed using standard transmission line with characteristic impedance Z_0 and its length is $0.5\lambda_0$ plus and additional length that is required to obtain the desired phase shift. While upper branch is composed of a $\lambda/2$ coupled line and parallel $\lambda/8$ open and short stubs to the coupled line. Thus upper branch has a more dispersive phase property than a uniform transmission line in the lower branch. The phase slope can be controlled by the specific ratio of the main impedance of the

coupled line in the upper branch and the stub impedances which are connected in parallel. The device is fabricated using a soft Teflon substrate, the relative permittivity of the Teflon is 2.17 and the loss tangent is 0.0009 at 10 GHz. By fabricating using the proposed method, a satisfactory flat phase response is achieved with good return loss and insertion loss.

The planar type phase shifters could be implemented by distributed elements, lumped elements, or a combination of both. Although distributed elements have advantageous performances, lumped elements are, also, extensively used to decrease chip size, and cost. An example of use of lumped elements in phase shifters can be seen in Rizzi's work [8], which is a digital phase shifter utilizing three PIN diodes in a Tee configuration. One can see the proposed phase shifter circuit in Figure 2-8. Its operation is explained in terms of low-pass and high pass filter circuits.

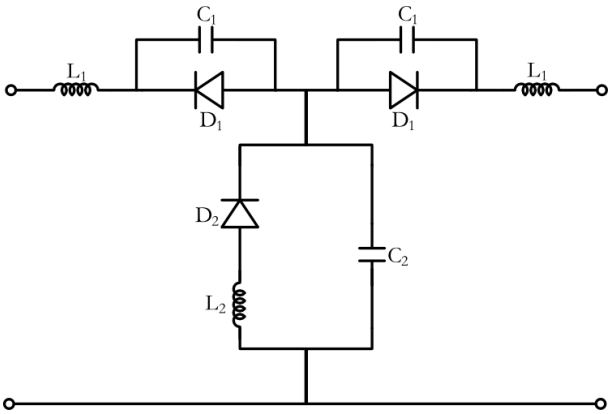


Figure 2-8. The proposed phase shifter circuit with three diodes.

In state A, diodes D1 are forward biased, diode D2 is reverse biased, the circuit behaves like a constant K low pass filter while in state B, diodes D1 are reverse biased and diode D2 is forward biased so that it approximates to a constant K high pass filter.

In order to decrease the losses due to the filter characteristics, the cutoff frequency of the low pass filter is chosen such that it is greater than the high-pass filter's cutoff frequency. Also the phase change occurs between the cutoff frequency of the high-pass and the cutoff frequency of the low-pass circuit. To investigate the parasitics and circuit analysis in-depth refer to Figure 2-9.

Forward biased diodes are modeled as a resistance, R_f (R_{f1} for D1, R_{f2} for D2). In the reverse bias state, the equivalent circuit of a diode is a resistance in series with a junction capacitance. Also, in the design it is assumed that any parasitic inductance due to diode packaging may be lumped in with inductances L1 and L2. The values of the lumped components are calculated according to some assumptions such as the diodes are lossless and the capacitance C_1 and C_2 are small.

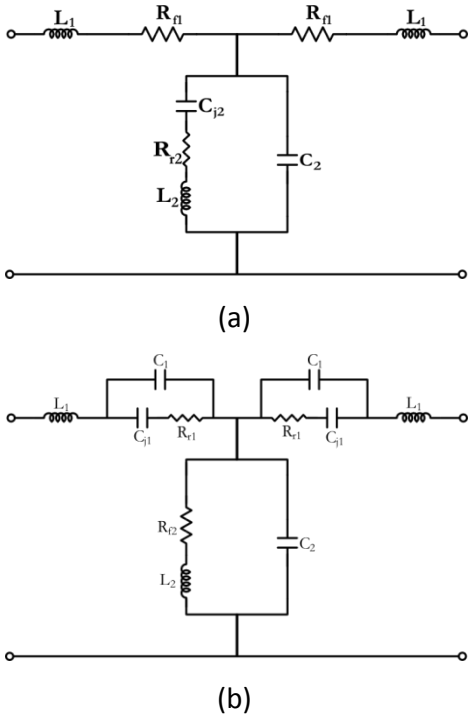


Figure 2-9. Bias States of the Proposed Phase Shifter (a) diodes-1 are forward biased and diode-2 is reverse biased (b) diodes-1 are reverse biased and diode-2 is forward biased.

Some meritorious works are done by Ayaslı [9],[10]. One of them is monolithic phase shifter operating in the 2-8 GHz frequency range, in which the phase shifter topology is high-pass/low-pass with the switching elements of six GaAs FETs per bit [9]. As known the FETs are modeled as a resistor in their low-impedance state and in the high-impedance state it is modeled as a combination of a resistor and a capacitor. In Figure 2-10 one can see the overall circuit of the proposed phase shifter by Ayaslı.

The parasitics of the FET switches are included in the design to achieve improved results. It is claimed that for monolithic circuit applications, the available switch elements are FETs. Unlike the PIN diodes, the total capacitor shunting the high-impedance switch state is large; to realize the switching action, this capacitance must either be resonated or its effect must somehow be included in the design of the impedance-matching sections. It is understood that for that kind of designs; i.e. not normally matched to system impedance, impedance-matching circuits must be used. For both cases the bandwidth is limited. Back to the schematic of the circuit; when the control voltage V_1 is equal to zero and V_2 is below the pinch-off voltage the circuit becomes like in Figure 2-11.

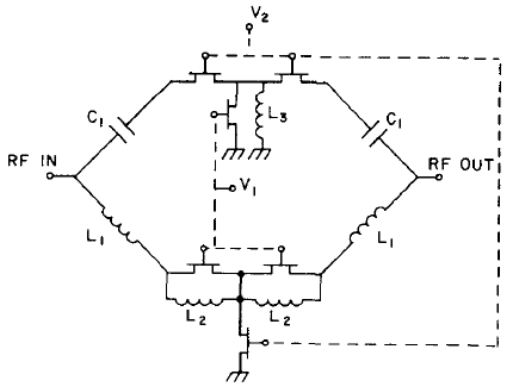


Figure 2-10. Schematic circuit diagram of one bit [9].

If a suitable design is prepared, the resistive components r_1 and r_2 are negligibly small compared with the resistive impedance in series or parallel with them, the circuit can be further simplified to the form as shown in Figure 2-12. The circuit shown in Figure 2-12 is the low-pass state of the phase shifter.

In the other state, that is, when V_2 is equal to zero and V_1 is below the pinch-off, the circuit is shown as in Figure 2-13. This is further simplified to as in Figure 2-14 as r_3 and r_4 are way too small from the reactive components. Figure 2-14 is like a five element high-pass state of the phase shifter as the capacitors C_4 and C_5 do not affect the shunt inductances.

Considering the implementation, the inductors are realized with high-impedance transmission lines since large inductor values are not needed; i.e. short line approximation is used. A two-bit phase shifter is designed and fabricated on 0.1 mm GaAs substrate in monolithic form. The phase shift bits are 90° and 180°.

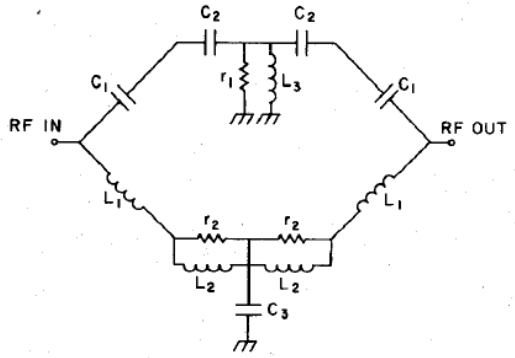


Figure 2-11. The circuit representation when state becomes V_1 is equal to zero and V_2 is below the pinch-off [9].

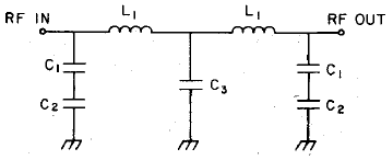


Figure 2-12. Simplified version of the circuit in state V_1 is equal to zero and V_2 is below the pinch-off [9].

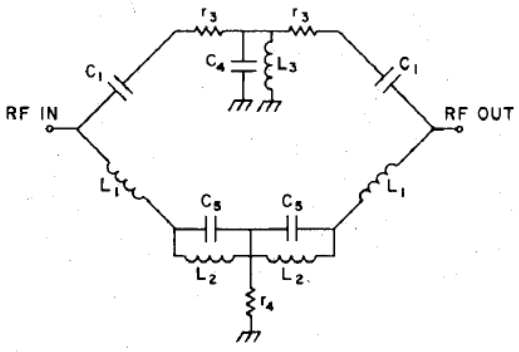


Figure 2-13. The circuit representation when state becomes V_2 is equal to zero and V_1 is below the pinch-off [9].

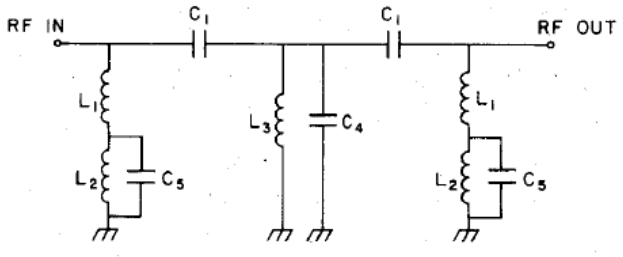


Figure 2-14. Simplified version of the circuit in state V_2 is equal to zero and V_1 is below the pinch-off [9].

There seems that a lot of experiments conducted for that phase shifter. Such as; the temperature variation of the insertion losses is checked for the two bits at 22°C, 58°C, and 88°C and it is seen from the results that the differential phase is varied less than 1° over the range, the sensitivity to the gate bias is checked by varying the gate voltage from -7 to -9 V and no change in phase or insertion loss is observed. These experiments are done because it guarantees that fluctuations in bias voltage as it switches back and forth between states are not translated in to phase or amplitude noise.

By using the same topology, as in Figure 2-10, in one of the phase shifter bits, Schindler presented a 3-bit MMIC phase shifter [11]. This phase shifter uses passive MESFET switching elements and it is bi-directional. High-pass/low-pass filter circuits are used in which MESFET off-state capacitances incorporated as filter elements. A high performance can be achieved with this broadband phase shifter. The MESFETs used in this phase shifter are the same as the MESFETs used in the amplifiers operating in the same band in order to ease the work to integrate the phase shifters with the amplifiers, 18 to 40 GHz. The phase shift bits 45° and 90° use a topology as shown in Figure 2-15 and the 180°phase shift bit uses the one in Figure 2-10 as described above.

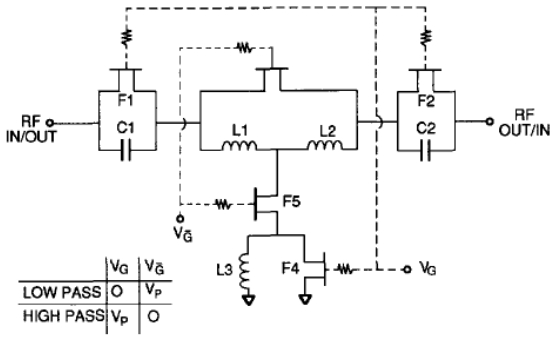


Figure 2-15. Schematic diagram of 45° and 90° bits [11].

The fabrication seems to be very similar as in [9]. Maximum rms phase error is 9.8° at 28 GHz. The rms phase error averaged over the 18-40 GHz band is 7.2°. The rms amplitude error has a maximum of 1.1 dB at 18 GHz and 1.2 dB at 40 GHz. The rms amplitude error averaged over the 18-40 GHz band is 0.97 dB. The differential phases are predicted well; however, the insertion losses are around 7 dB to 11 dB which are sure a little bit high compared to a practical phase shifter, but use of the phase shifter together with amplifiers decreases the importance of the losses at all. Return loss is generally better than 10 dB with occasional peaks at some frequencies in some states.

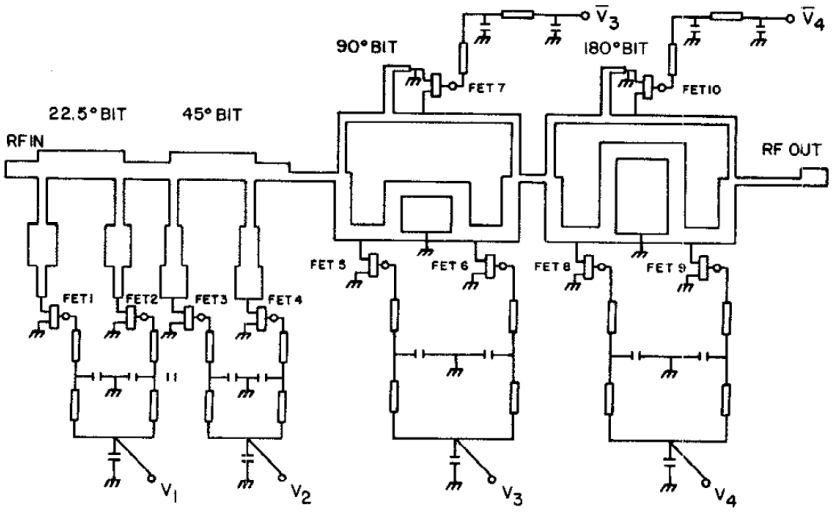


Figure 2-16. The schematic circuit diagram of the four-bit phase shifter [10].

The other work done by Ayasli is a four-bit digital phase shifter which works in X-band [10]. In this work, the properties of FET switches deeply investigated depending on

the geometry of the FETs, doping levels, etc. The schematic circuit diagram of the phase shifter is shown in Figure 2-16.

The 22.5° and 45° bits are designed to provide constant phase shifts over the frequency bandwidth using the loaded line technique. The loads are connected through proper matching networks with terminations as FET switches. The differential phase shift obtained by switching the loads in two states. When the main line is symmetrically loaded, the insertion loss variations and the input and output VSWR are low enough. Also nearly constant insertion phase is obtained. This circuit is reciprocal and passive. The dielectric used to form capacitors is a plasma-assisted CVD Si_3N_5 layer with a nominal thickness of 5000Å and its dielectric constant is 6.8. Insertion loss is around 6 dB and differential phase shift results seem to be satisfactory for phased-arrays.

There, also, are works done on true time-delay phase shifters. One of them is a 2-10 GHz phase shifter for ultra wideband phased-array systems by Kand and Hong [12]. For true time-delay phase shifters a linear phase change versus frequency is needed; in a wideband phased array antenna, a progressive phase shift between successive radiating elements must be a linear function of frequency in order to achieve a frequency insensitive scan over a wide signal bandwidth.

For implementing true time-delay, there exist some techniques, among them use of the switched delay lines is one of the easiest ways. Another one is the distributed analog phase shifter with diode-loaded transmission line. It is chosen because of low insertion loss and low power consumption. This technique has been demonstrated using Schottky junction varactors, MEMS bridges, or thin film ferroelectric barium strontium titanate (BST) varactors. A tunable delay line consists of a high-impedance transmission line periodically loaded with voltage variable capacitors. By applying a single bias voltage to varactors or MEMS bridges, the effective distributed capacitance of the synthetic transmission line can be changed, which in return changes the phase velocity, and the associated time delay through the line, as well.

There are limiting factors for this technique; one of them is the low quality of the varactors.

Figure 2-17 (a) shows a conventional varactor-loaded transmission line phase shifter. For this circuit the differential phase shift can be described as $\Delta\phi = 2\pi f_0 n\sqrt{L}\left(\sqrt{C_{max}} - \sqrt{C_{min}}\right)$ where maximum and minimum capacitances are the capacitance values that varactors could achieve. The phase control range is limited since varactor capacitance values are limited. Furthermore, the characteristic impedance changes as the capacitance of the varactor changes.

$$Z_{0-max} = \sqrt{\frac{L}{C_{min}}} \text{ and } Z_{0-min} = \sqrt{\frac{L}{C_{max}}}$$

This indicates that there is tradeoff between the matching performance and the amount of phase per section.

Unlike the above discussion, Figure 2-17 (b) is a digital distributed phase shifter in which the L and C values are fixed. Phase shift increases, by means of the steps of the single section phase shift, while maintaining a good matching performance as the input signal propagates along the artificial transmission line. Maximum possible differential phase shift of n T-sections can be written as

$$\Delta\phi = 2\pi f_0 (n-1)\sqrt{LC}.$$

For circuit implementation, phase selection in parallel is realized by distributed active switches using cascode MOSFETs like in Figure 2-18. One of these MOSFETs is used as the fixed capacitance and the other is used as the switching element. Advantages to use this structure are high gain, high output resistance, and high reverse isolation.

In order to increase the bandwidth of the phase shifter, a series inductor can be inserted between the shunt peaking inductor and the capacitive load. This is called shunt and series peaking load, seen in Figure 2-19 (a) (shown together with the simplified model Figure 2-19 (b)). In comparison with an ordinary shunt peaked topology, the combination of shunt and series peaking can provide three distinct resonance frequencies, thereby improving the bandwidth of the phase shifter. Also, it

is better to note that the shunt-series peaked load provides a relatively flat gain response over wideband frequency ranges which can be seen in the experimental results.

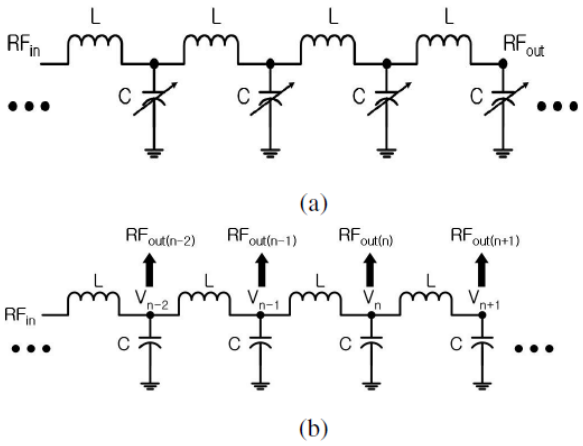


Figure 2-17. (a) The distributed analog phase shifter (b) The digital distributed phase shifter [12].

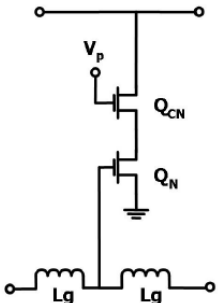


Figure 2-18. The schematic of a single T-section [12].

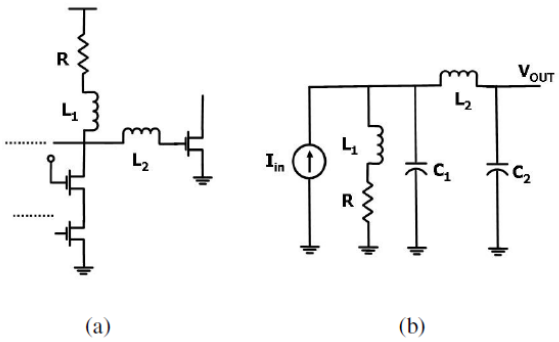


Figure 2-19. (a) Shunt and series peaking load (b) Simplified model [12].

The overall three-bit phase shifter circuit has been realized as in Figure 2-20, with the help of theoretical approaches described above. Note that a source follower is used

as an active buffer for wideband output matching. The phase response has nearly linear phase characteristic and the input return loss is better than 15 dB over the band. rms phase error is less than 4.5° and rms amplitude error is less than 0.42 dB.

The series-shunt configurations of the switches are used in several works. One of them is by Kang *et. al.* [13]. In this phase shifter, the FET switches are a part of phase shifting elements. Two types of a Ku-band 90° phase shifter are designed. The topology used is again high-pass/low-pass topology. In Figure 2-20 (a) the overall circuit schematic is presented, in Figure 2-20 (b) one of the states is shown where V1=0V, V2= -4V in which the circuit act like a high-pass filter as T-network, and in Figure 2-20 (c) the other state is presented where V1=-4V, V2= 0V in which the circuit act like a low-pass filter as π-network.

From the simulated isolation characteristics of the work by Kang *et. al.,* it is shown that the low-pass filter has better isolation compared to the high-pass filter since the series connected off-state capacitance of the FET to the lumped circuit capacitance improves this characteristic. It is a common fact that the size of the FET affect highly the phase shifter performance in terms of insertion loss, bandwidth, and amplitude balance, so the larger the FETs the better the performance but worse the bandwidth. In this work, the topology is the resonated FET circuit. In Figure 2-21 the topology of the resonated FET circuit can be seen as well as the equivalent circuit models for different states. At the high pass state, satisfying the impedance matching condition, the inductance and capacitance required to realize insertion phase ϕ_0 at frequency ω_0 are equal to the following;

$$L_1 = \frac{Z_0}{\omega_0 \tan(\phi_0/2)}$$

$$C_1 = \frac{1}{\omega_0 Z_0 \sin \phi_0}$$

At the other state of the circuit the circuit is simplified to a resonated circuit.

According to the experimental results, they seem to be inadequate. It is believed that the return loss of the reference state restricts the bandwidth.

One of the MMIC phase shifter examples is introduced by Boire *et. al.* [14]. Mentioning that a low-band version between the frequency band of 2-6 GHz of the phase shifter is done before and the new band were chosen as 4.5 to 18 GHz. In the low-band version, the phase shifter had a maximum phase error of less than 15° with less than ±0.6 dB insertion loss variation. In the high-band version the phase shifter had a maximum phase error of less than 20° and less than ±1.15 dB insertion loss variation with phase state.

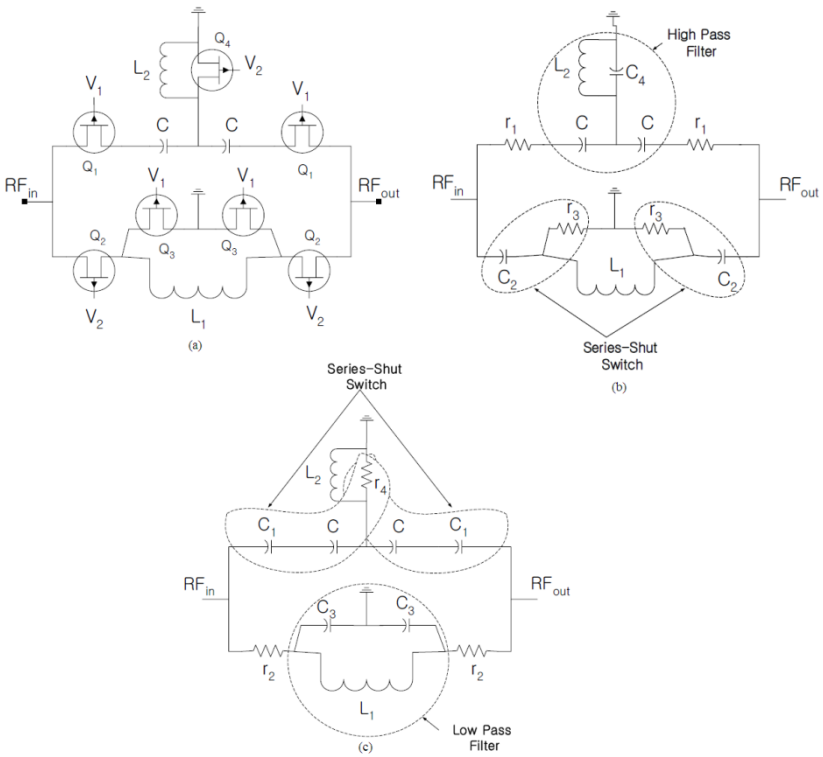
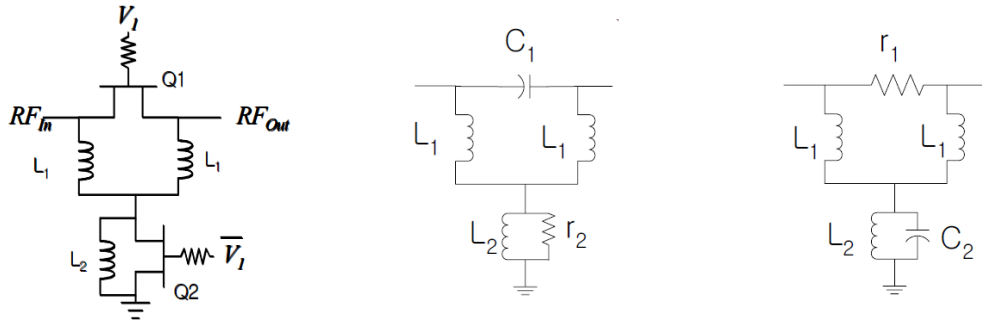


Figure 2-20. (a) The circuit schematic of the proposed phase shifter (b) The state where V1=0V, V2= -4V in which the circuit act like a high-pass filter (c) The state where V1=-4V, V2= 0V in which the circuit act like a low-pass filter [13].



(a) (b) (c)

Figure 2-21. (a) The schematic of the phase shifter using resonated FET circuit (b) The equivalent circuit of high-pass filter state (c) The equivalent circuit of the reference state [14].

The five-bit phase shifter composed of four separately optimized phase shifter sections consisting of 180°, 90°, 45°, and 22.5°/11.25° combined sections. The lowest two bits are combined to realize size and insertion loss savings over a separate bit approach. The topologies of the 90°, 45°, and 22.5°/11.25° sections utilize interdigitated quadrature couplers terminated with FET switched reflective loads. The 22.5°/11.25° section utilizes termination networks with two FET switches each.

In the operation, the input signal to the coupler splits and split parts are incident upon two identical terminations, signals reflected from the terminations added at the output port of the coupler. Changes in the impedance of the reflective terminations cause both phase and amplitude variations at the output port of the coupler. The insertion loss of the phase shifter sections is minimized by making the terminations as reflective as possible, and so as to reduce the incidental amplitude modulation of the phase shifter sections a small amount of loss is deliberately introduced in the termination networks to equalize magnitude of the reflection coefficient of the networks in each of their states. A 10-mil substrate is used to achieve low-loss from the interdigitated couplers over a two octave bandwidth. The authors tested for the yield of the phase shifter and the fabrication process. The insertion phases for all of the states are nearly in the desired range and the return losses are better than 10 dB, however, the insertion losses are not that promising.

Another MMIC phase shifter is introduced by Dai and Chen [15]. The introduced phase shifter works in the 5-20 GHz band, and it can work either in analogue or digital mode. The phase shift is 90° and the topology is specifically selected to minimize effect of process variations on performance. The basic topology is a reflection-type phase shift circuit as can be seen in Figure 2-22.

The phase shifter consists of a Lange bridge, switch FETs, resistors, capacitors, and microstrip lines. For analog phase shifter response, the gate bias voltages of the FETs are operated in the range of 0.1 to 0.9 pinch-off voltage to change the phase shift from 0° to 90°. The phase shifter is implemented with GaAs MMIC process. The thickness of air bridges, microstrip lines, and the bonding pads are increased to 5 um gold. Measured performances show a flat phase response, on the contrary, the insertion loss is not that good compared to the phase response.

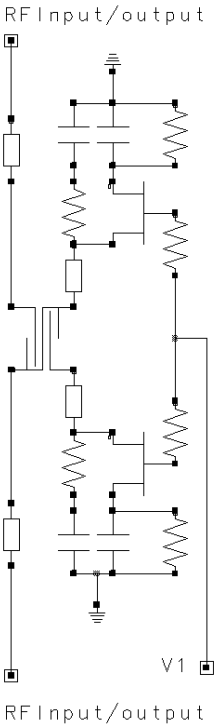


Figure 2-22. Schematic of the phase shifter proposed in [15].

Since the MMIC technology is preferred a lot, there are lots of works on that topic as described above and one of those works is a five-bit phase shifter with integrated

CMOS-compatible digital interface circuitry by Simon *et. al.* [16]. The differential phase shift is achieved using high-pass/low-pass topology, FETs are chosen as switch elements. The digital interface circuitry is composed of both active and passive elements formed using the standard microwave implant. A dual-implant microwave/digital process that produces high-performance digital circuits integrated with microwave circuits. The dual-implant process produces standard microwave devices alongside low-pinch-off (about 1 V) digital devices.

High-performance digital circuits can be obtained, with the low-pinch-off devices. The dual-implant process also yields reduced digital circuit area over the standard microwave process due to reduced digital device dimensions and metallization pitch. Using this digital circuitry and without changing the RF circuitry, the similar phase performance has been achieved with reduced DC power consumption by three times, total circuit area reduced by 25%. Switching time is reduced by a factor of 5. The phase shifter DC power consumption, completely in the digital interface circuitry, is 300 mW and the switching speed is 50 ns. The DC power consumption of the digital interface circuitry is high and the switching speed moderately slow due to the use of high-pinch-off, high-current, microwave FETs in the digital circuitry, result of using a standard foundry process. RMS phase error is <10° from 6.5 to 18 GHz and <15° from 6 to 6.5 GHz. The insertion loss ranges from 10 dB at 6 GHz to a maximum of 14 dB at 18 GHz. rms amplitude error is <0.8 dB, minimum input return loss is 7.5 dB, and minimum output return loss is 5 dB from 6 to 18 GHz. The slope in insertion loss is mainly due to the 90° bit which is formed by cascading two 45° bit. Measured performance of this bit shows excellent amplitude tracking but about 3 dB slope in insertion loss from 6 to 18 GHz.

One of the newest techniques in the design of a phase shifter is the design with artificial left-hand and right-hand transmission line, however this technique seems to be not promising enough as seen in some of the works present in the literature.

Starting with an example on artificial transmission lines, a paper written by Lee *et. al.* is investigated [17], to understand the theory behind the subject. A broadband

quadrature hybrid is designed with two power dividers to split the power and the phase difference elements as the meta-material delay lines are used. A conventional quadrature hybrid is built by four transmission lines with two different characteristic impedances. The transmission lines have 90° phase difference at a specific frequency, implying that the bandwidth is limited. Architecture of a broadband hybrid is given in Figure 2-23 together with the dispersion relation diagram of the meta-material transmission line. As can be observed from the architecture, two broadband hybrid power splitters are used to divide the power equally and two power combiners used to collect the orthogonal phase signals through a crossover circuit at the output. The artificial transmission line is a composite left-right hand transmission line which is like a band-pass filter. The zero value of the propagation constant can be controlled with the help of the artificial line's phase slope.

A left-handed line is composed of cascading unit cells where each unit cell consists of series capacitance, inductance and shunt capacitance and inductance. Propagation constant and the impedance of the transmission line are characterized by these four equivalent parameters and the number of unit cells used. Unlike the conventional transmission line where the zero propagation constant occurs at DC, the dispersion curve of the CRLH-TL (Composite Right-Left Handed-Transmission Line) will cross zero at a zero (DC) frequency as observed from Figure 2-23 (b). Therefore, the broadband phase difference between the two transmission lines can be realized, by designing two dispersion curves with the same slope but different offset frequency. Phase characteristics seem to be satisfactory in a limited band. In Figure 2-24 the complete structure of the quadrature hybrid can be observed.

Another artificial transmission line based phase shifter example is introduced by Kholodnyak *et. al.* [18]. This phase shifter topology is based on switching between a conventional transmission line with positive dispersion and an artificial meta-material transmission line having negative dispersion. The artificial transmission line used as the negative dispersion is implemented as a quasi-lumped-element structure using a

multilayer technology. Since the phase shift is linearly dependent on the frequency, this phase shifter is also a constant time-delay circuit.

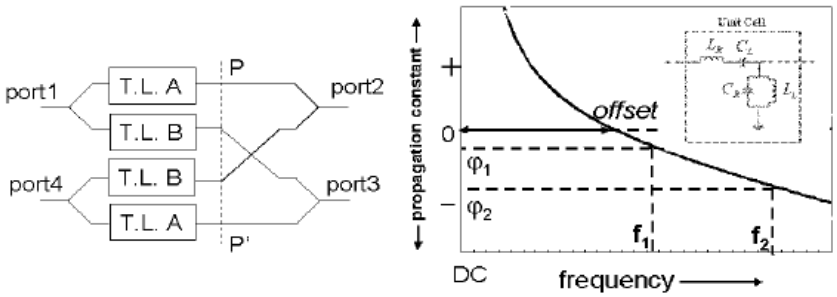


Figure 2-23. (a) Architecture of the broadband quadrature hybrid. (b) Dispersion diagram of the metamaterial transmission line, CRLH-TL. [17]

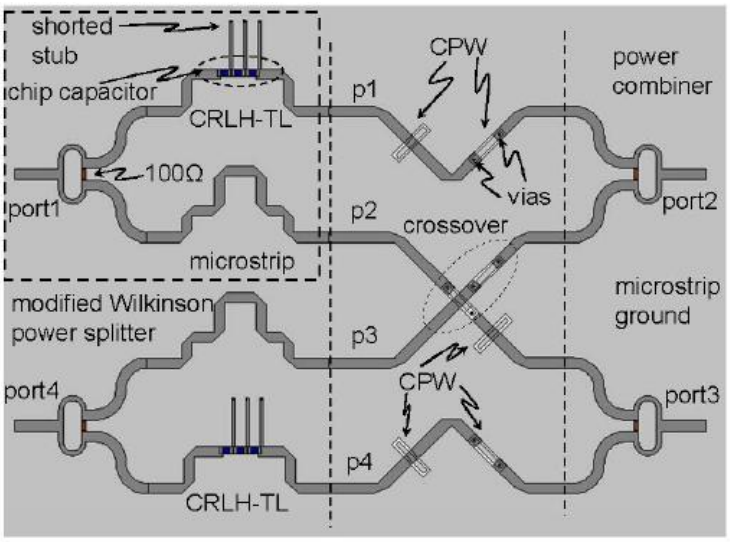


Figure 2-24. Complete structure of the proposed broadband four-port quadrature hybrid. [17]

The right-handed transmission line (RHTL), which is a conventional transmission line, in which the phase and group velocities are co-directional, has a positive dispersion; the insertion phase of the RHTL is negative and the artificial version of conventional transmission line can be formed by using a ladder network which is formed by connecting a series inductor with a shunt capacitor. According to the principle of duality, the transmission line with interchanged inductors and capacitors can be considered as a left-handed transmission line (LHTL) characterized by a negative dispersion with the opposite directions of phase and group velocities and the

insertion phase of LHTL is positive. LHTL is designed as a cascaded connection of two identical lumped-element T-networks with +45° phase incursion each. The simulation results prove the idea with good results; however the experimental results do not exist for this work.

The work about the artificial transmission line by Yongzhuo *et. al* . [19] is the last work to be examined in this section. Right-handed meta-materials are like the normal transmission lines but they have non-zero phase constants at DC. The circuit model of the artificial transmission line can be observed in Figure 2-25.

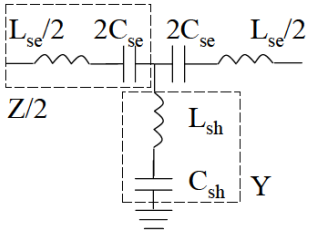


Figure 2-25. Equivalent circuit mode for the ideal TL unit cell of RH MMs [19]

By using standard Schiffman phase shifter topology and simple two transmission line topology two phase shifter circuits are proposed as shown in Figure 2-26.

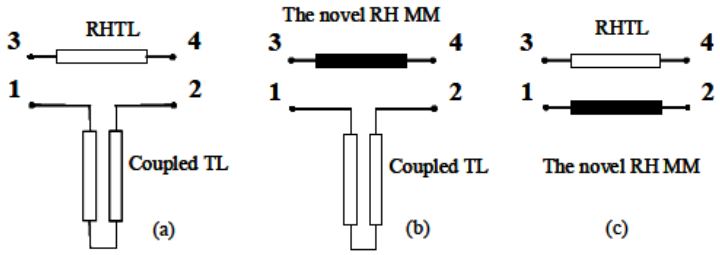


Figure 2-26. Three circuit schemes for (a) Standard Schiffman phase shifter, (b) Type-A: new differential phase shifter based on the coupled TL and RH MM TL, (c) Type-B: new differential phase shifter using the RH MM TL and conventional RHTL [19].

According to the simulation results, the return loss is better than -10 dB over the band, the insertion loss is promising enough and the phase responses' flatness is well.

As discussed before, phase shifters could also be implemented monolithically with amplifiers. For instance, a 12 GHz active phase shifter with an integrated LNA is implemented in SiGe (Silicon-Germanium) process [20].

CHAPTER 3

THE THEORY ON ALL-PASS NETWORK PHASE SHIFTER AND IDEAL PHASE RESPONSES FOR VARIOUS CASES

This part of the thesis is dedicated to the theory on the all-pass network phase shifter which is constructed with lumped inductors, capacitors, and SPDT switches, and ideal design results. Firstly, theory of an all-pass filter is given in detail with some additional analysis. Then, the design methodologies of one-stage, and two-stage all-pass network phase shifters, which are already introduced in the literature [21], are investigated. In [21], the design parameters are given for a four-bit phase shifter design, in addition to this four-bit design parameters, in this thesis bit-5 (11.25° phase shift bit), and bit-6 (5.625° phase shift bit) design parameters are found and presented. As it is already mentioned the related work [21] has given one-stage, and two-stage design parameters. Using this topology with increased number of stages, and introducing new design parameters, the differential phase bandwidth could be extended to infinity, and a generalized rule for this is introduced for the first time in the literature in this thesis. Three-stage version of this idea is introduced for an ultra-wideband (UWB), 1 to 6 GHz, four-bit phase shifter design and implementation in [22]. Finally, obtained lumped element values, and ideal phase responses for various cases are given at the end of this part of the thesis.

3.1 Theory of an All-Pass Filter Topology

Before starting the one-stage topology and its theory, a common knowledge for an all-pass filter might be important. The two types of all-pass networks are given in

Figure 3-1 and Figure 3-2. The network in Figure 3-1, can be named as all-pass network with series-L configuration, and the network in Figure 3-2, can be named as all-pass network with series-C configuration.

All-pass networks are said to be matched naturally, if the following condition is satisfied;

$$Z_0 = \sqrt{\frac{L}{C}} \tag{3.1}$$

where, L and C are the component values used in the all pass networks. The network is matched with Z_0 (system impedance) so that all-pass networks are matched naturally, no further effort needed to match the network to other networks. A very beneficial advantage of all-pass networks among the others such as high pass/low pass phase shifter networks is acquisition of wider bandwidths. Also, cascading all-pass networks increases the bandwidth compared to lesser stage ones.

It is shown that all-pass networks can have configurations of series-L or series-C. Both networks are unbalanced with a common ground which has an advantage over integration with different technologies such as stripline or microstrip. Both networks, i.e., the series-L and series-C configurations have equivalent phase responses. Even and odd mode analysis of the two networks leads the way to investigate the equivalency of the phase responses. In Figure 3-3, both series-L and series-C all-pass networks are shown in terms of just L and C values, in order to apply even and odd mode analysis.

For even mode analysis; both circuits are reduced to series L and C circuit. For odd mode; they all reduce to parallel L and C. So both have the same even mode reflection coefficient and odd mode reflection coefficient. Taking this into account and using unitary property for lossless, reciprocal and symmetric two ports, we can conclude that their S_{11} and S_{21} are the same since they have the same reflection coefficients. To find even mode reflection coefficient, odd mode reflection coefficient, S_{11} and S_{21} the procedure is as follows:

- The normalized impedance and normalized frequency are;

$$z = \frac{1}{Z_0}\sqrt{\frac{L}{C}} \tag{3.2a}$$

$$\Omega = \omega/\omega_0 \tag{3.2b}$$

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{3.2c}$$

- The inductance and capacitance can be written in terms of reactance and susceptance as;

$$x = \omega\, {}^{L}/_{Z_0},\ x = \Omega z \tag{3.3a}$$

$$b = \omega C Z_0\ ,\ b = \frac{\Omega}{z} \tag{3.3b}$$

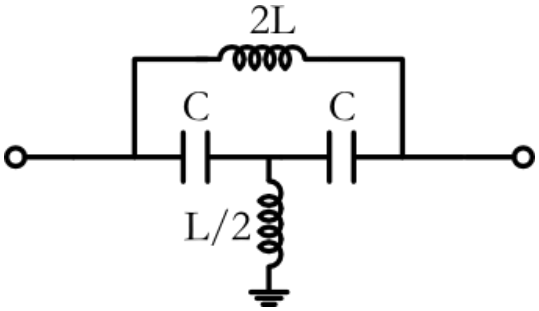


Figure 3-1. All pass network with series-L configuration

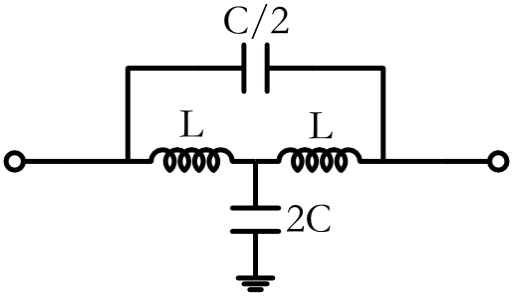


Figure 3-2. All pass network with series-C configuration

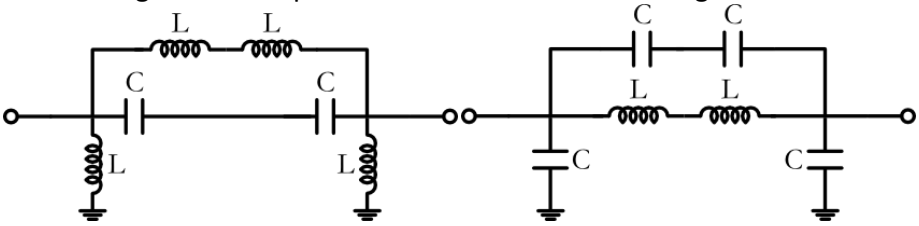


Figure 3-3. Series L and series C circuits respectively to analyze even and odd modes

- Then the even mode reflection coefficient is as follows;

$$\Gamma_e = \frac{j\omega L + \frac{1}{j\omega C} - Z_0}{j\omega L + \frac{1}{j\omega C} + Z_0} = \frac{\frac{j\omega L}{Z_0} - \frac{j}{\omega C Z_0} - 1}{\frac{j\omega L}{Z_0} - \frac{j}{\omega C Z_0} + 1} = \frac{j\left(x - {}^{1}/_{b}\right) - 1}{j\left(x - {}^{1}/_{b}\right) + 1} = \frac{jz\left(\Omega - {}^{1}/_{\Omega}\right) - 1}{j\left(\Omega - {}^{1}/_{\Omega}\right) + 1} = \frac{jWz - 1}{jWz + 1} \quad (3.4)$$

where;

$$W = \Omega - {}^{1}/_{\Omega} \quad (3.5)$$

- Odd mode reflection coefficient can be found with a similar procedure. The corresponding S_{11} and S_{21} are as follows;

$$S_{11} = \frac{1}{2}(\Gamma_e + \Gamma_o) \quad (3.6a)$$

$$S_{21} = \frac{1}{2}(\Gamma_e - \Gamma_o) \quad (3.6b)$$

- The corresponding phase response of that network is the phase of S_{21};

$$\Psi = \pi - 2tan^{-1}(W) \quad (3.7)$$

Note that throughout this work, series-C configuration is preferred because of several practical advantages on series-L configuration. Those advantages are;

- Eliminating the use of additional inductor elements (implemented inductors have electrical performance less close to that of ideal elements compared to capacitors). Hence the design time and variations are decreased.
- Inductance values are calculated to be smaller (2L inductance is needed in series-L configuration; on the other hand L inductance is needed for series-C configuration). Hence the circuit size is decreased.

3.2 Theory of One-Stage, and Two-Stage All-Pass Network Phase Shifter Topology

Below in Figure 3-4, an all-pass network phase shifter with one stage is presented. The two networks have their own transition frequencies according to their capacitance and inductance values as follows:

$$\omega_A = 1/\sqrt{L_A C_A}\,, \omega_B = 1/\sqrt{L_B C_B} \tag{3.8}$$

At this point, we can redefine Ω as ω/ω_m where $\omega_m = \sqrt{\omega_A \omega_B}$, which is the center frequency of the band of interest, and a new design parameter should be introduced; $a_1 = \sqrt{\omega_A/\omega_B}$ then the insertion phases of the two circuits are as follows;

$\Psi_A = \pi - 2tan^{-1}(\Omega a_1 - {}^{1}/_{\Omega a_1})$ and $\Psi_B = \pi - 2tan^{-1}({}^{\Omega}/_{a_1} - {}^{a_1}/_{\Omega})$ so that the differential phase is;

$$\phi = 2\left\{tan^{-1}\left(\Omega a_1 - {}^{1}/_{\Omega a_1}\right) - tan^{-1}\left({}^{\Omega}/_{a_1} - {}^{a_1}/_{\Omega}\right)\right\} \tag{3.9}$$

To find the design parameter p; equate ϕ to ϕ_m – which is the desired phase shift- when Ω=1 – the center frequency –, then a_1 is related as;

$$a_1 = \frac{1}{2}tan\left(\frac{\phi_m}{4}\right) + \sqrt{1 + \frac{1}{4}tan^2\left(\frac{\phi_m}{4}\right)} \tag{3.10}$$

Then we can calculate the lumped components values, i.e., inductance and capacitance, for both combinations of series-L, and series-C configurations as;

$$L_A = \frac{a_1 Z_0}{\omega_m} \quad (3.11a) \qquad C_A = \frac{a_1}{Z_0 \omega_m} \quad (3.11b)$$

$$L_B = \frac{Z_0}{a_1 \omega_m} \quad (3.11c) \qquad C_B = \frac{1}{a_1 Z_0 \omega_m} \quad (3.11d)$$

One can find the design parameter, a_1 values for different phase shifts in Table 3-1.

Table 3-1. Design parameter a_1 values for one-stage four-bit all-pass phase shifter.

Phase ϕ_m:	**22.5°**	**45°**	**90°**	**180°**
$\boldsymbol{a_1}$**:**	1.050	1.104	1.228	1.618

Following the exact steps, one could calculate the design parameter value for 11.25°, and 5.625° phase shift bits for a six-bit configuration. The calculated design parameter values for bit-5 and bit-6 are given in Table 3-2.

Table 3-2. Design parameter a_1 values for one-stage bit-5, and bit-6 all-pass phase shifter.

Phase ϕ_m:	**11.25°**	**5.625°**
$\boldsymbol{a_1}$**:**	1.025	1.012

The differential phase plots are given in Figure 3-5 for 5.625°, 11.25°, and 22.5° phase shift values, and Figure 3-6 for 45°, 90°, and 180° phase shift values.

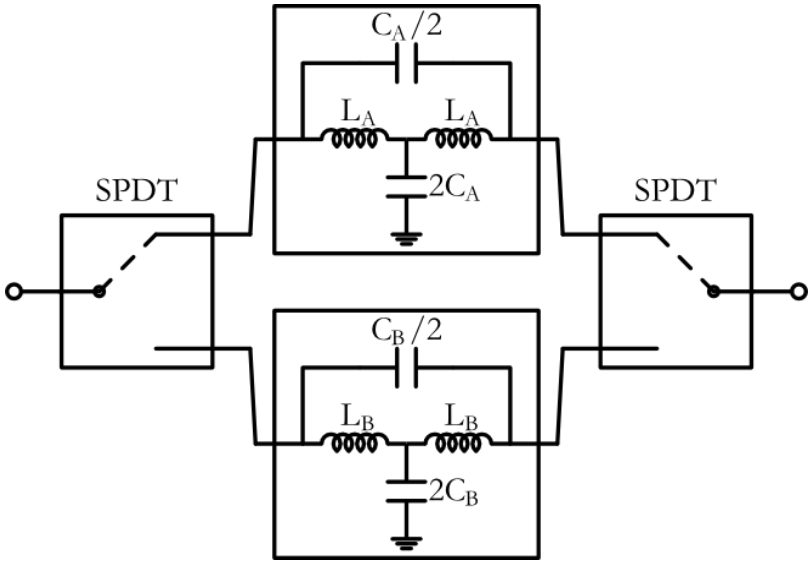


Figure 3-4. An illustration of One-Stage All-pass Phase Shift bit with series-C configuration.

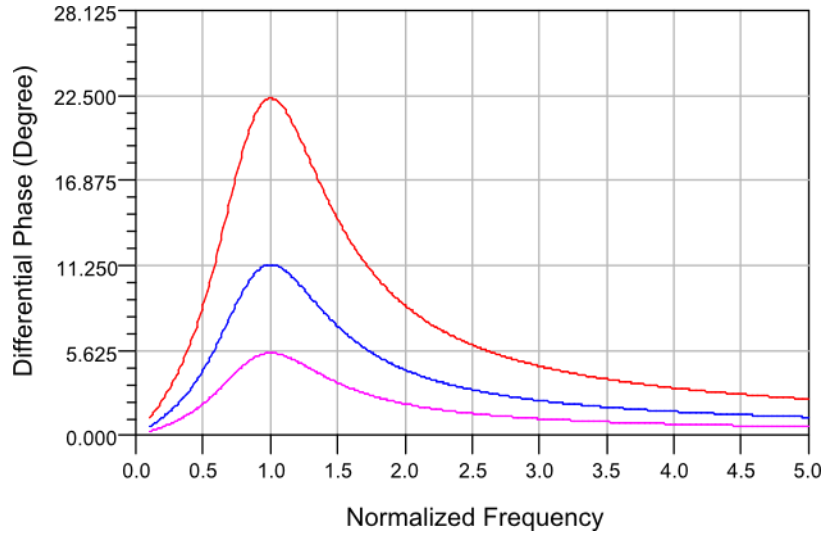


Figure 3-5. Differential phase shift plots for 5.625° (pink line), 11.25° (blue line), and 22.5° (red line).

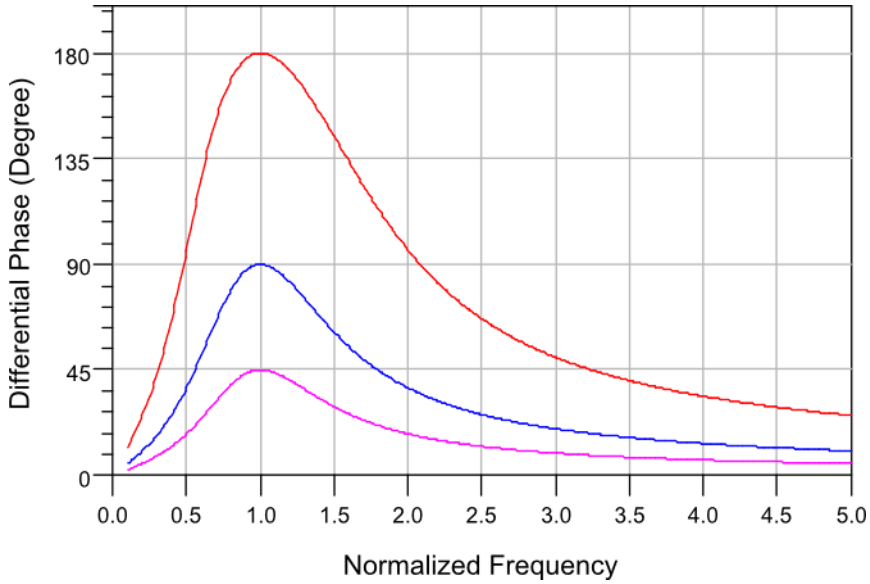


Figure 3-6. Differential phase shift plots for 45° (pink line), 90° (blue line), and 180° (red line).

Bandwidth considerations are also important for a phase shifter. Define bandwidth B as ω_2/ω_1 where ω_2 is the upper frequency for the bandwidth and ω_1 is the lower frequency for the bandwidth. Then the peak-to-peak flatness $\Delta\phi$ can be calculated from one of the following equations;

$$\Delta\phi = \phi\left(\Omega = \sqrt{B}\right) - \phi_0 \quad (3.12a)$$

$$\Delta\phi = \phi\left(\Omega = {}^{1}/_{\sqrt{B}}\right) - \phi_0 \quad (3.12b)$$

One can observe from Table 3-3 that for an octave bandwidth the peak-to-peak flatness values are high and it is not a desirable situation. A further examination on differential phase shifts could be of more help. The analysis is done for every phase shift bit for different bandwidth values in terms of rms phase, peak-to-peak flatness (P-P Flatness), and rms phase error. The results are given in Table 3-4. One can observe that the P-P flatness is increased for the increased bandwidth. This behavior can be foreseen because of the characteristics of the differential phase. Moreover, the rms phase is decreased for increasing bandwidth, and the rms phase error is increased at the same time. Taking into account the specifications of a desired phase shifter, one can achieve proper rms phase within the band, with proper choices of design parameter values. By doing that, the results are obtained as in Table 3-5. The 180° phase shift is improved in terms of rms phase, P-P flatness, and rms phase error. Other bits' rms phase values are improved; however, the P-P flatness and rms phase errors are degraded, slightly. These degradations are very small, and in overall one can say that the performance is improved. One can improve bandwidth characteristics by cascading one more stage of all-pass filter with the previous one. This brings to a new topic, which is the theory of two-stage all-pass network phase shifter.

Table 3-3. Peak-to-peak flatness values for one stage all pass phase shifter

Phase ϕ_m:	**22.5°**	**45°**	**90°**	**180°**
B=1.2:1	0.6°	1.2°	2.0°	1.9°
B=1.6:1	3.6°	6.9°	12.1°	12.5°
B=2.0:1	6.5°	12.8°	23.0°	26.5°

Table 3-4. Differential phase shift related data for each phase shift bit using design parameter (Table 3-1,Table 3-2), for one-stage phase shifter, and various bandwidths.

Bandwidth=1.2:1			
Bit	**rms Phase (°)**	**P-P Flatness (°)**	**rms Phase Error (°)**
5.625°	5.41	0.17	0.06
11.25°	11.18	0.35	0.11
22.5°	22.05	0.68	0.22
45°	44.36	1.31	0.43
90°	89.09	2.21	0.72
180°	179.24	2.08	0.68
Bandwidth=1.6:1			
Bit	**rms Phase (°)**	**P-P Flatness (°)**	**rms Phase Error (°)**
5.625°	5.15	0.88	0.28
11.25°	10.66	1.83	0.57
22.5°	21.03	3.57	1.11
45°	42.37	6.96	2.16
90°	85.62	12.16	3.76
180°	175.72	12.57	3.83
Bandwidth=2.0:1			
Bit	**rms Phase (°)**	**P-P Flatness (°)**	**rms Phase Error (°)**
5.625°	4.87	1.58	0.51
11.25°	10.07	3.27	1.04
22.5°	19.88	6.40	2.04
45°	40.12	12.57	4.00
90°	81.53	22.71	7.19
180°	170.97	26.10	8.07

Below in Figure 3-7; there is a two-stage all-pass phase shifter. For this network; the phase response should be as the following equation;

$$\phi = 2\left\{tan^{-1}\left(\frac{\Omega}{a_1 a_2} - \frac{a_1 a_2}{\Omega}\right) - tan^{-1}\left(\frac{a_1\Omega}{a_2} - \frac{a_2}{\Omega a_1}\right) + tan^{-1}\left(\frac{a_2\Omega}{a_1} - \frac{a_1}{a_2\Omega}\right) - tan^{-1}\left(\Omega a_1 a_2 - \frac{1}{\Omega a_1 a_2}\right)\right\} \quad (3.13)$$

In the above equations; for each all-pass filter there exist a transition frequency and those affect the phase response. A new design parameter can be introduced at that point named as a_2, and it can be defined as;

$$a_2 = \sqrt{\frac{\omega_{A2}}{\omega_{A1}}} = \sqrt{\frac{\omega_{B2}}{\omega_{B1}}} = \sqrt{\frac{\omega_A}{\omega_B}} \quad (3.14)$$

ω_A is the upper transition frequency of one of the two stages and ω_B is the lower transition frequency of one of the two stages. We defined ω_A as $\sqrt{\omega_{A1}\omega_{B1}}$ and ω_B as $\sqrt{\omega_{A2}\omega_{B2}}$ according to the designs of two-stage networks.

Table 3-5. Differential phase shift related data for each phase shift bit using different design parameter values for various bandwidths, for one-stage phase shifter.

Bandwidth=1.2:1				
a_1	**Bit**	**rms Phase (°)**	**P-P Flatness (°)**	**rms Phase Error (°)**
1.0125	**5.625°**	5.63	0.18	0.06
1.0252	**11.25°**	11.28	0.35	0.11
1.051	**22.5°**	22.44	0.69	0.22
1.106	**45°**	45.04	1.32	0.43
1.231	**90°**	89.96	2.22	0.72
1.623	**180°**	179.97	2.07	0.67
Bandwidth=1.6:1				
a_1	**Bit**	**rms Phase (°)**	**P-P Flatness (°)**	**rms Phase Error (°)**
1.0131	**5.625°**	5.62	0.97	0.30
1.0264	**11.25°**	11.23	1.92	0.60
1.054	**22.5°**	22.47	3.81	1.19
1.111	**45°**	44.94	7.34	2.28
1.242	**90°**	89.90	12.52	3.87
1.645	**180°**	180.02	12.27	3.74
Bandwidth=2.0:1				
a_1	**Bit**	**rms Phase (°)**	**P-P Flatness (°)**	**rms Phase Error (°)**
1.0138	**5.625°**	5.61	1.82	0.58
1.028	**11.25°**	11.22	3.64	1.16
1.057	**22.5°**	22.43	7.21	2.30
1.117	**45°**	44.89	13.94	4.44
1.256	**90°**	90.01	24.21	7.65
1.679	**180°**	180.56	24.91	7.69

The center frequency; i.e. ω_m, definition is the same as defined in one stage topology as $\omega_m = \sqrt{\omega_A \omega_B}$.

The other design parameter, a_1, should be; $a_1 = \sqrt{\omega_{B2}/\omega_{A2}} = \sqrt{\omega_{B1}/\omega_{A1}}$. The associated design parameters' values a_1 and a_2 for two stage network are as follows in Table 3-6.

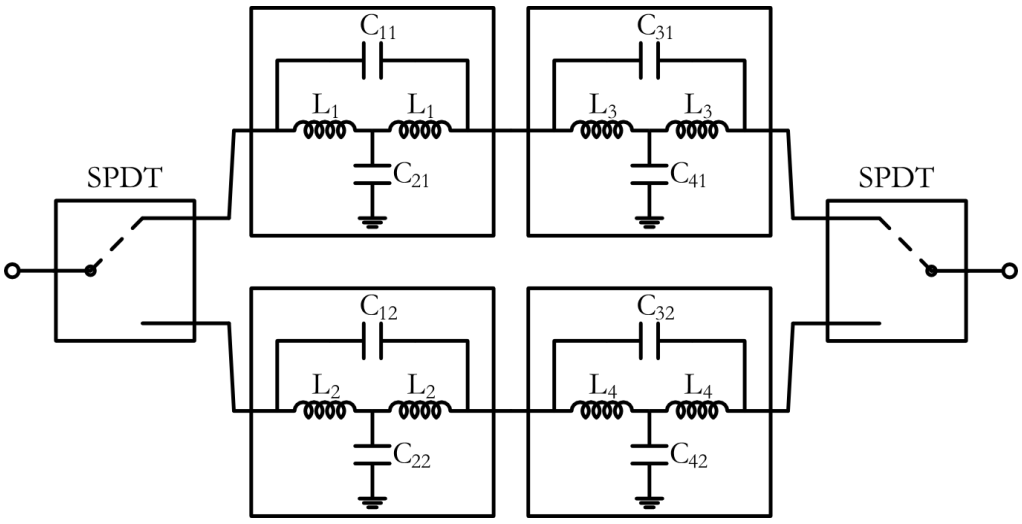


Figure 3-7. An illustration of a Two-Stage All-pass Phase Shift bit with series-C configuration.

Table 3-6. a_1 and a_2 values for two-stage, four-bit, all-pass phase shifter network.

Phase ϕ_m:	**22.5°**	**45°**	**90°**	**180°**
$\boldsymbol{a_1}$**:**	1.040	1.082	1.174	1.413
$\boldsymbol{a_2}$**:**	1.543	1.549	1.569	1.667

It is mentioned earlier that bandwidth is crucial for those types of devices, and for this reason, two-stage all-pass network phase shifter bandwidth considerations are examined. A similar analysis as in one-stage, is, also done here, for two-stage all-pass network phase shifter for given design parameter values in Table 3-6. The results are provided in Table 3-7. The P-P flatness and rms phase errors are increased, and at the same time the rms phase of the phase shift bits are decreased as the bandwidth is increased. A more improved phase shifter design could be made by considering the desired bandwidth, and the amount of allowed phase error. In Table 3-8, the design parameter values are written for a six-bit phase shifter design and for various bandwidths. Note that design parameter values are provided for the first time in the literature for various bandwidth values. Comparison of Table 3-8 with Table 3-7 shows that; 2:1 bandwidth could be designed almost as a constant phase with proper choice of design parameter values. In all of the cases the differential phases have rms

value at the desired value. For 3:1 bandwidth design, the rms phase values for the phase shift bits is very close to the desired values unlike using design parameter values given in Table 3-6, also, rms phase errors are improved. However, P-P flatness of the phase shift bits is a little degraded. For 4:1, and 6:1 bandwidth designs it is clear that the latter designs have superiority against the first one. The differential phase shifts for various bandwidth designs are provided in Figure 3-8 for 5.625° bit, Figure 3-9 for 11.25° bit, Figure 3-10 for 22.5° bit, Figure 3-11 for 45° bit, Figure 3-12 for 90° bit, Figure 3-13 for 180° bit for illustration purposes to give the relation between the bandwidth and differential phase shifts.

Table 3-7. Differential phase shift related data for each phase shift bit using design parameters (Table 3-6), for two-stage phase shifter, and various bandwidths.

Bandwidth=2.0:1			
Bit	**rms Phase (°)**	**P-P Flatness (°)**	**rms Phase Error (°)**
22.5°	22.65	1.58	0.55
45°	45.25	3.10	1.08
90°	90.44	5.52	1.92
180°	180.04	6.32	2.20
Bandwidth=3.0:1			
Bit	**rms Phase (°)**	**P-P Flatness (°)**	**rms Phase Error (°)**
22.5°	22.71	1.93	0.58
45°	45.40	3.67	1.12
90°	90.76	6.25	1.98
180°	180.50	6.59	2.22
Bandwidth=4.0:1			
Bit	**rms Phase (°)**	**P-P Flatness (°)**	**rms Phase Error (°)**
22.5°	22.08	5.34	1.41
45°	44.18	7.57	2.72
90°	88.60	18.43	4.80
180°	178.01	21.66	5.49
Bandwidth=6.0:1			
Bit	**rms Phase (°)**	**P-P Flatness (°)**	**rms Phase Error (°)**
22.5°	20.54	10.34	3.25
45°	41.17	20.39	6.36
90°	82.97	38.08	11.77
180°	170.10	53.87	15.85

Table 3-8. Differential phase shift related data for each phase shift bit using different design parameters' values for various bandwidths, for two-stage phase shifter.

Bandwidth=2.0:1					
a_1	a_2	**Bit**	**rms Phase (°)**	**P-P Flatness (°)**	**rms PE (°)**
1.009	1.442	**5.625°**	5.62	0.11	0.04
1.018	1.439	**11.25°**	11.26	0.20	0.07
1.036	1.434	**22.5°**	22.51	0.45	0.13
1.073	1.437	**45°**	45.01	0.90	0.25
1.155	1.455	**90°**	90.01	1.58	0.43
1.372	1.556	**180°**	180.01	1.69	0.46
Bandwidth=3.0:1					
a_1	a_2	**Bit**	**rms Phase (°)**	**P-P Flatness (°)**	**rms PE (°)**
1.010	1.538	**5.625°**	5.63	0.50	0.14
1.020	1.535	**11.25°**	11.25	1.02	0.29
1.039	1.534	**22.5°**	22.50	2.05	0.57
1.081	1.537	**45°**	45.00	4.00	1.09
1.171	1.554	**90°**	90.00	7.01	1.91
1.406	1.649	**180°**	180.04	7.79	2.10
Bandwidth=4.0:1					
a_1	a_2	**Bit**	**rms Phase (°)**	**P-P Flatness (°)**	**rms PE (°)**
1.011	1.630	**5.625°**	5.63	0.95	0.27
1.021	1.642	**11.25°**	11.27	1.79	0.56
1.042	1.628	**22.5°**	22.48	3.81	1.08
1.087	1.631	**45°**	44.97	7.41	2.10
1.184	1.647	**90°**	89.99	13.06	3.70
1.437	1.736	**180°**	180.12	14.98	4.18
Bandwidth=6.0:1					
a_1	a_2	**Bit**	**rms Phase (°)**	**P-P Flatness (°)**	**rms PE (°)**
1.012	1.791	**5.625°**	5.62	1.69	0.51
1.023	1.792	**11.25°**	11.25	3.36	1.02
1.047	1.793	**22.5°**	22.50	6.67	2.02
1.097	1.795	**45°**	45.01	13.01	3.92
1.206	1.805	**90°**	90.00	23.47	6.95
1.487	1.882	**180°**	180.30	28.32	8.13

Only the equations used to compute the component values are left and those are as follows in equation set (3.15) (please here note that the labeling of the components are the same for the labeling of the components used in the design).

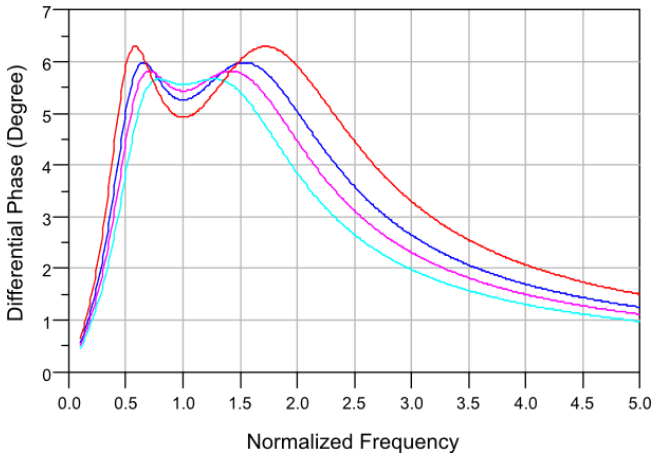


Figure 3-8. Differential phase shift plots for 5.625° bit two-stage for bandwidths of 2:1 (turquoise line), 3:1 (pink line), 4:1 (blue line), and 6:1 (red line).

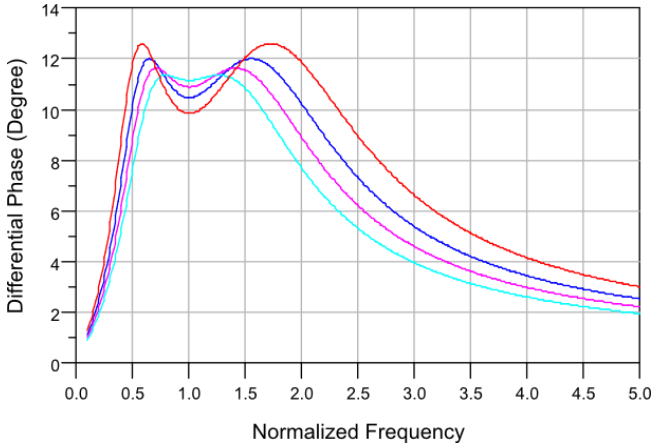


Figure 3-9. Differential phase shift plots for 11.25° bit two-stage for bandwidths of 2:1 (turquoise line), 3:1 (pink line), 4:1 (blue line), and 6:1 (red line).

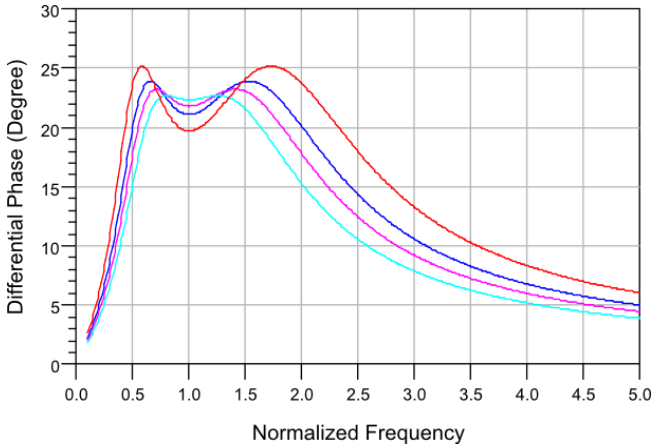


Figure 3-10. Differential phase shift plots for 22.5° bit two-stage for bandwidths of 2:1 (turquoise line), 3:1 (pink line), 4:1 (blue line), and 6:1 (red line).

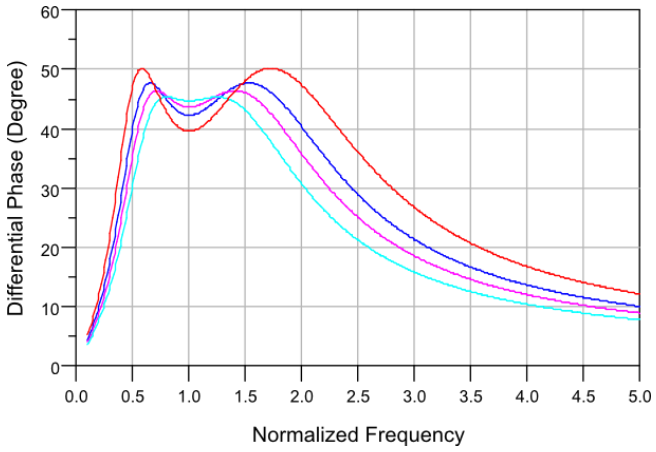


Figure 3-11. Differential phase shift plots for 45° bit two-stage for bandwidths of 2:1 (turquoise line), 3:1 (pink line), 4:1 (blue line), and 6:1 (red line).

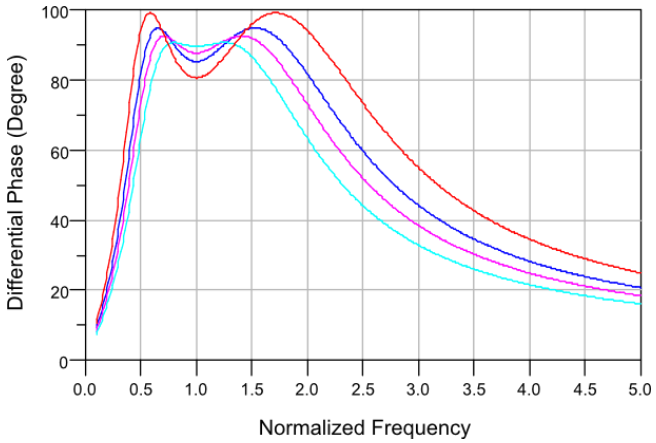


Figure 3-12. Differential phase shift plots for 90° bit two-stage for bandwidths of 2:1 (turquoise line), 3:1 (pink line), 4:1 (blue line), and 6:1 (red line).

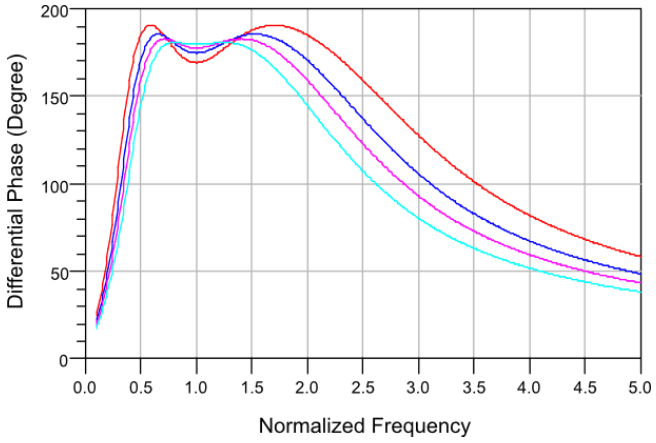


Figure 3-13. Differential phase shift plots for 180° bit two-stage for bandwidths of 2:1 (turquoise line), 3:1 (pink line), 4:1 (blue line), and 6:1 (red line).

$$L_1 = a_1 a_2 \frac{Z_0}{\omega_m} \quad (3.15a) \qquad C_{11} = \frac{a_1 a_2}{2 Z_0 \omega_m} \quad (3.15b) \qquad C_{21} = \frac{2 a_1 a_2}{Z_0 \omega_m} \quad (3.15c)$$

$$L_2 = \frac{Z_0}{a_1 a_2 \omega_m} \quad (3.15d) \qquad C_{12} = \frac{1}{2 a_1 a_2 Z_0 \omega_m} \quad (3.15e) \qquad C_{22} = \frac{2}{a_1 a_2 Z_0 \omega_m} \quad (3.15f)$$

$$L_3 = \frac{a_1}{a_2} \frac{Z_0}{\omega_m} \quad (3.15g) \qquad C_{31} = \frac{a_1}{a_2} \frac{1}{2 Z_0 \omega_m} \quad (3.15h) \qquad C_{41} = \frac{a_1}{a_2} \frac{2}{Z_0 \omega_m} \quad (3.15i)$$

$$L_4 = \frac{a_2}{a_1} \frac{Z_0}{\omega_m} \quad (3.15j) \qquad C_{32} = \frac{a_2}{a_1} \frac{1}{2 Z_0 \omega_m} \quad (3.15k) \qquad C_{42} = \frac{a_2}{a_1} \frac{2}{Z_0 \omega_m} \quad (3.15l)$$

3.3 Achieving constant differential phase shift for desired band of frequency

As mentioned above, one can characterize four-stage all-pass network phase shifter introducing a new design parameter, namely a_3. An illustration of a four-stage phase shifter is given in Figure 3-14. The differential phase shift equation is given in (3.16) for a four-stage all-pass network phase shifter. The design parameters; a_1, a_2, and a_3, are optimally found for various bandwidth values and listed in Table 3-9, for the first time in literature.

The ideal differential phase characteristics can be found in Figure 3-15, for 22.5° phase shift bit for bandwidth values of 6:1 (turquoise line), 8:1 (pink line), 12:1 (blue line), and 16:1 (red line); in Figure 3-16 for 45° phase shift bit for bandwidth values of 6:1 (turquoise line), 8:1 (pink line), 12:1 (blue line), and 16:1 (red line); in Figure 3-17 for 90° phase shift bit for bandwidth values of 6:1 (turquoise line), 8:1 (pink line), 12:1 (blue line), and 16:1 (red line); and finally in Figure 3-18 for 180° phase shift bit for bandwidth values of 6:1 (turquoise line), 8:1 (pink line), 12:1 (blue line), and 16:1 (red line). The y-axis is the differential phase shift in degrees; the x-axis is the normalized frequency in logarithmic scale. The arrows are the markers added to indicate the start and the stop frequency of the interested band.

Table 3-9. a_1, a_2, and a_3 values for four-stage, four-bit, all-pass network phase shifter for various bandwidth values.

Phase ϕ_m:	**22.5°**	**45°**	**90°**	**180°**
Bandwidth=6.0:1				
a_1:	1.027	1.055	1.116	1.255
a_2:	1.359	1.360	1.376	1.404
a_3:	2.028	2.028	2.072	2.144
Bandwidth=8.0:1				
a_1:	1.029	1.059	1.122	1.273
a_2:	1.401	1.403	1.408	1.445
a_3:	2.152	2.157	2.175	2.279
Bandwidth=12.0:1				
a_1:	1.032	1.064	1.134	1.299
a_2:	1.465	1.466	1.472	1.509
a_3:	2.349	2.354	2.378	2.494
Bandwidth=16.0:1				
a_1:	1.034	1.068	1.142	1.319
a_2:	1.515	1.515	1.522	1.558
a_3:	2.502	2.508	2.534	2.660

$$\phi = 2\left\{tan^{-1}\left(\frac{\Omega}{a_1a_2a_3} - \frac{a_1a_2a_3}{\Omega}\right) + tan^{-1}\left(\frac{a_2\Omega}{a_1a_3} - \frac{a_1a_3}{a_2\Omega}\right) + tan^{-1}\left(\frac{a_3\Omega}{a_1a_2} - \frac{a_1a_2}{a_3\Omega}\right) + tan^{-1}\left(\frac{a_1\Omega}{a_2a_3} - \frac{a_2a_3}{a_1\Omega}\right)\right.$$
$$- tan^{-1}\left(\frac{a_2a_3\Omega}{a_1} - \frac{a_1}{\Omega a_2a_3}\right) - tan^{-1}\left(\frac{a_1a_2\Omega}{a_3} - \frac{a_3}{\Omega a_1a_2}\right) - tan^{-1}\left(\frac{a_1a_3\Omega}{a_2} - \frac{a_2}{\Omega a_1a_3}\right) \quad (3.16)$$
$$\left. - tan^{-1}\left(\Omega a_1a_2a_3 - \frac{1}{\Omega a_1a_2a_3}\right)\right\}$$

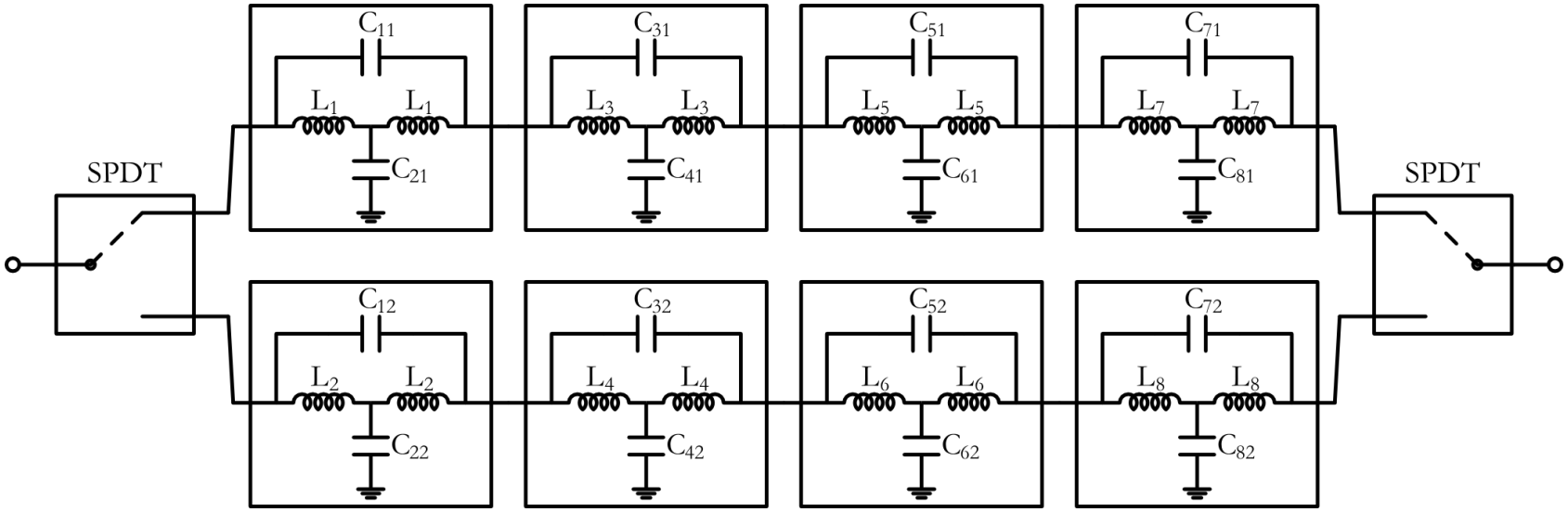


Figure 3-14. The four-stage all-pass network phase shifter with component names. Only one bit is illustrated.

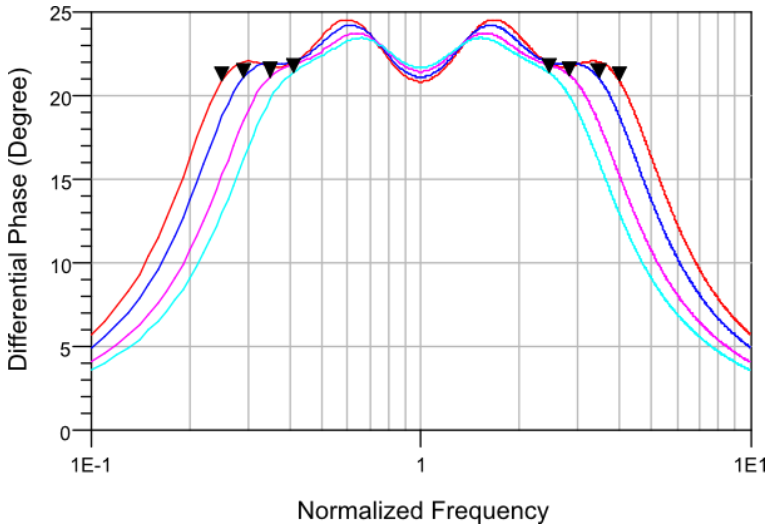


Figure 3-15. Differential phase shift plots for 22.5° bit four-stage for bandwidths of 6:1 (turquoise line), 8:1 (pink line), 12:1 (blue line), and 16:1 (red line).

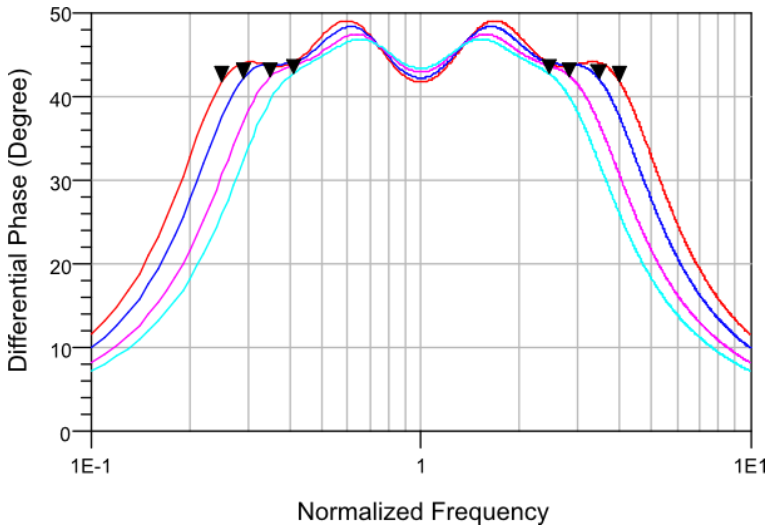


Figure 3-16. Differential phase shift plots for 45° bit four-stage for bandwidths of 6:1 (turquoise line), 8:1 (pink line), 12:1 (blue line), and 16:1 (red line).

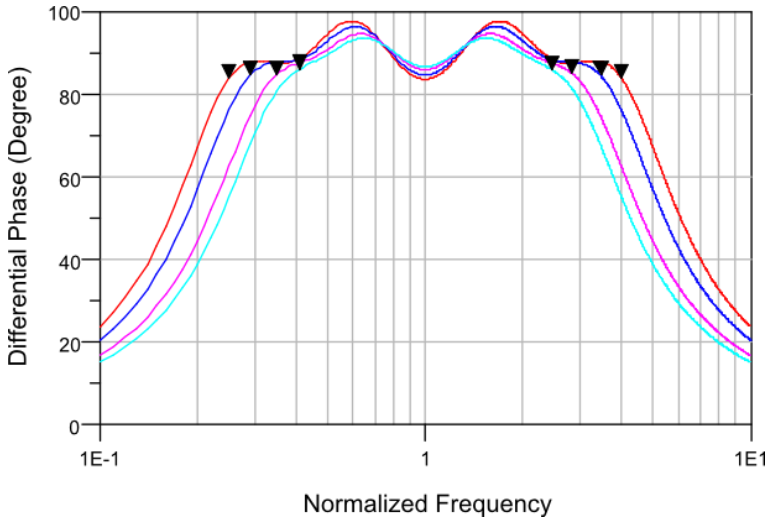


Figure 3-17. Differential phase shift plots for 90° bit four-stage for bandwidths of 6:1 (turquoise line), 8:1 (pink line), 12:1 (blue line), and 16:1 (red line).

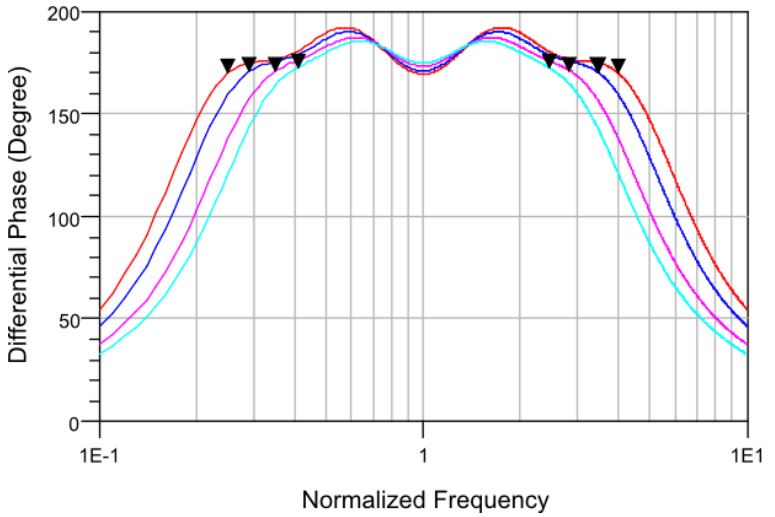


Figure 3-18. Differential phase shift plots for 180° bit four-stage for bandwidths of 6:1 (turquoise line), 8:1 (pink line), 12:1 (blue line), and 16:1 (red line).

Ideal differential phase related results are presented quantitatively in Table 3-10, for a four-bit, four-stage all-pass network phase shifter; for bandwidths of 6:1, 8:1, 12:1, and 16:1. The rms phases are close enough to the desired phase shift values, the rms phase errors are low enough to be considered as a success. However, the maximum phase errors are slightly high for 90°, and 180° phase shift bits, which are, actually, acceptable for high valued phase shift bits like 90°, and 180°.

Table 3-10. Differential phase shift related data for each phase shift bit, for four-stage phase shifter, and bandwidths of 6:1, 8:1, 12:1, and 16:1.

Bandwidth=6.0:1			
Bit	**rms Phase (°)**	**P-P Flatness (°)**	**rms PE (°)**
22.5°	22.49	2.07	0.64
45°	44.97	4.12	1.27
90°	90.01	7.63	2.44
180°	180.01	12.99	3.97
Bandwidth=8.0:1			
Bit	**rms Phase (°)**	**P-P Flatness (°)**	**rms PE (°)**
22.5°	22.46	2.59	0.78
45°	44.93	5.12	2.15
90°	89.92	9.90	3.00
180°	179.93	16.47	5.04
Bandwidth=12.0:1			
Bit	**rms Phase (°)**	**P-P Flatness (°)**	**rms PE (°)**
22.5°	22.46	3.12	0.95
45°	44.94	6.17	1.88
90°	89.92	11.80	3.63
180°	179.98	19.60	6.24
Bandwidth=16.0:1			
Bit	**rms Phase (°)**	**P-P Flatness (°)**	**rms PE (°)**
22.5°	22.42	3.70	1.06
45°	44.90	7.36	2.10
90°	89.88	14.05	4.06
180°	179.97	22.78	6.96

For a complete design procedure, one should know the lumped element formulations. The four-stage all-pass network phase shifter lumped element equations are given in the equation set of (3.17a-x);

$$L_1 = a_1 a_2 a_3 \frac{Z_0}{\omega_m} \quad (3.17a) \qquad C_{11} = \frac{a_1 a_2 a_3}{2 Z_0 \omega_m} \quad (3.17b) \qquad C_{21} = \frac{2 a_1 a_2 a_3}{Z_0 \omega_m} \quad (3.17c)$$

$$L_2 = \frac{Z_0}{a_1 a_2 a_3 \omega_m} \quad (3.17d) \qquad C_{12} = \frac{1}{2 a_1 a_2 a_3 Z_0 \omega_m} \quad (3.17e) \qquad C_{22} = \frac{2}{a_1 a_2 a_3 Z_0 \omega_m} \quad (3.17f)$$

$$L_3 = \frac{a_1 a_3}{a_2}\frac{Z_0}{\omega_m} \quad (3.17g) \qquad C_{31} = \frac{a_1 a_3}{a_2}\frac{1}{2Z_0\omega_m} \quad (3.17h) \qquad C_{41} = \frac{a_1 a_3}{a_2}\frac{2}{Z_0\omega_m} \quad (3.17i)$$

$$L_4 = \frac{a_2}{a_1 a_3}\frac{Z_0}{\omega_m} \quad (3.17j) \qquad C_{32} = \frac{a_2}{a_1 a_3}\frac{1}{2Z_0\omega_m} \quad (3.17k) \qquad C_{42} = \frac{a_2}{a_1 a_3}\frac{2}{Z_0\omega_m} \quad (3.17l)$$

$$L_5 = \frac{a_1 a_2}{a_3}\frac{Z_0}{\omega_m} \quad (3.17m) \qquad C_{51} = \frac{a_1 a_2}{2a_3 Z_0\omega_m} \quad (3.17n) \qquad C_{61} = \frac{2a_1 a_2}{a_3 Z_0\omega_m} \quad (3.17o)$$

$$L_6 = \frac{a_3 Z_0}{a_1 a_2 \omega_m} \quad (3.17p) \qquad C_{52} = \frac{a_3}{2a_1 a_2 Z_0\omega_m} \quad (3.17q) \qquad C_{62} = \frac{2a_3}{a_1 a_2 Z_0\omega_m} \quad (3.17r)$$

$$L_7 = \frac{a_1}{a_2 a_3}\frac{Z_0}{\omega_m} \quad (3.17s) \qquad C_{71} = \frac{a_1}{a_2 a_3}\frac{1}{2Z_0\omega_m} \quad (3.17t) \qquad C_{81} = \frac{a_1}{a_2 a_3}\frac{2}{Z_0\omega_m} \quad (3.17u)$$

$$L_8 = \frac{a_2 a_3}{a_1}\frac{Z_0}{\omega_m} \quad (3.17v) \qquad C_{72} = \frac{a_2 a_3}{a_1}\frac{1}{2Z_0\omega_m} \quad (3.17w) \qquad C_{82} = \frac{a_2 a_3}{a_1}\frac{2}{Z_0\omega_m} \quad (3.17x)$$

A general rule to obtain these lumped element formulations, and differential phase shift have been developed. The set of rules is as follows;

- One must have stage numbers as powers of 2; such as, 2^0, 2^1, 2^2, 2^3, and etc. In general, the number of stages is equated to 2^{n-1}.
- Such that, " n " is the number of design parameter. The design parameters are named as a_i. $i = 1, 2, \ldots n$.
- Let K_j be the coefficients of odd numbered inductors of half of the total number of inductors (it will be shown that one could obtain the other half by using the below calculated inductors)(Note that the odd numbered inductors are placed in one branch, and the even numbered inductors are placed in the other branch.), i.e. $j = 1, 3, \ldots 2^{n-1} - 1$;

$$L_j = \frac{Z_0}{\omega_m} K_j \tag{3.18}$$

- The even numbered inductors of the first half of the inductors can be calculated easily with using the odd numbered inductors as;

$$L_{j+1} = \frac{Z_0}{\omega_m} \frac{1}{K_j} \tag{3.19}$$

- The first inductor's coefficient's formula is always the same as;

$$K_1 = \prod_{i=1}^{n} a_i \tag{3.20}$$

- With the knowledge of the first inductor's coefficient one could obtain the other odd numbered inductors' coefficients of the first half easily. As it is already mentioned, from those odd numbered inductors the even numbered ones can be found. From the first inductors coefficient, one can use equation (3.22) to find K_3, K_5, K_9, K_{17}, and so, for large number of n;

$$K_{1+2^k} = K_1/(a_{1+k})^2, k = 1, \dots, n-2 \text{ for } n > 2 \tag{3.21}$$

- One can realize that coefficients like K_7, K_{11}, K_{13}, K_{15}, and so, could not be obtained directly from K_1. To obtain coefficients like these, one can use the coefficients obtained from K_1 like the following;

$$K_{1+2^k+2^l} = K_{1+2^k}/(a_{1+l})^2, l = 1, \dots, k-1 \text{ for } k > 1 \tag{3.22}$$

- Third version of this equation could achieve to obtain the further inductors coefficients as follows;

$$K_{1+2^k+2^l+2^m} = K_{1+2^k+2^l}/(a_{1+m})^2, m = 1, \dots, l-1 \text{ for } l > 1 \tag{3.23}$$

- This procedure continues as above for large number of stages. Once the odd numbered inductors' coefficients of the first half inductor set have been achieved, the inductor equations for these odd numbered inductors could be obtained from equation (3.18). Then, one should obtain the even numbered

inductor formulations from equation (3.19) should be obtained. Now, the first half of the inductor equations are obtained, the other half of the inductors' coefficients could be reached as in the following equation (3.24) using the first half set;

$$K_{t+2^{n-1}} = K_t(a_n)^{2(-1)^t}, t = 1,\ 2, \dots, 2^{n-1} \tag{3.24}$$

- The whole inductor equations are, now, complete. Using the inductors the capacitor equations can easily be obtained by dividing the inductors to ${Z_0}^2$, since the all-pass filter is assumed to be naturally matched to system impedance, as described in section 3.1 of this chapter of the thesis. For series-C configuration all-pass filter the series connected capacitor equation is given in (3.25a), and the shunt connected capacitor equation is given in (3.25b).

$$C_{series,i} = L_i/2{Z_0}^2, i = 1,\ 2, \dots, 2^n \tag{3.25a}$$

$$C_{sHunt,i} = 2L_i/{Z_0}^2, i = 1,\ 2, \dots, 2^n \tag{3.25b}$$

- Also, after obtaining the inductor equations, one can directly write the differential phase equation;

$$\phi = 2\left\{\sum_{j=1}^{2^n-1} tan^{-1}\left(\frac{\Omega}{K_j} - \frac{K_j}{\Omega}\right) - \sum_{j=1}^{2^n-1} tan^{-1}\left(\Omega K_j - \frac{1}{\Omega K_j}\right)\right\} \tag{3.26a}$$

$$j = 1, 3, \dots 2^n - 1 \tag{3.26b}$$

- The differential phase shift is obtained, and to finalize the overall ideal phase shifter design, the only item left is to optimize the design parameters a_i $i = 1, 2, \dots n$, to achieve the desired phase shift within the desired bandwidth.

To give an example we are going to derive the equations for sixteen-stage all-pass network phase shifter. The sequence and ability to derive the equations of inductors is simply shown in Figure 3-19.

1. The number of stages is equal to $16 = 2^n - 1$
2. Then the design parameter number is calculated to be 5. The design parameters are named as a_1, a_2, a_3, a_4, and a_5.
3. The coefficient of the first inductor can be found from equation (3.22). It is simply multiplying whole of the design parameters; $K_1 = a_1 a_2 a_3 a_4 a_5$.
4. From K_1, according to equation (3.21) K_3, K_5, and K_9 can be calculated (3.27a-c).

$$K_3 = K_1/{a_2}^2 = a_1 a_3 a_4 a_5/a_2 \quad (3.27a)$$

$$K_5 = K_1/{a_3}^2 = a_1 a_2 a_4 a_5/a_3 \quad (3.27b)$$

$$K_9 = K_1/{a_4}^2 = a_1 a_2 a_3 a_5/a_4 \quad (3.27c)$$

5. As one can observe from Figure 3-19, that K_7, K_{11}, and K_{13} is not found, yet. One could derive K_7 from K_5; and K_{11}, and K_{13} from K_9 as in equation (3.28a-c) with the help of equation (3.22).

$$K_7 = K_5/{a_2}^2 = a_1 a_4 a_5/a_2 a_3 \quad (3.28a)$$

$$K_{11} = K_9/{a_2}^2 = a_1 a_3 a_5/a_2 a_4 \quad (3.28b)$$

$$K_{13} = K_9/{a_3}^2 = a_1 a_2 a_5/a_3 a_4 \quad (3.28c)$$

6. There is, still, one inductor coefficient K_{15} not resolved, which can be found using equation (3.23) with using K_{13} as in (3.29).

$$K_{15} = K_{13}/{a_2}^2 = a_1 a_5/a_2 a_3 a_4 \quad (3.29)$$

7. Now that the all of left-half odd numbered inductors' coefficients are found, obtain the left-half even numbered inductors' coefficients using (3.19).
8. The right-half inductors are easy to obtain, using (3.24).
9. Since the inductance equations are ready, one can easily reach capacitors equations using (3.25a-b)
10. Obtain the differential phase shift expression using (3.26a-b).
11. Optimally find the design parameters a_1, a_2, a_3, a_4, and a_5, considering the permissible errors, and bandwidth.

Using these formulations, eight-stage and sixteen-stage, design parameters are found and presented in Table 3-11, and Table 3-12; respectively.

Table 3-11. a_1, a_2, a_3, and a_4 values for eight-stage, four-bit, all-pass network phase shifter for a bandwidth of 100:1.

Phase ϕ_m:	**22.5°**	**45°**	**90°**	**180°**
a_1:	1.028	1.058	1.119	1.258
a_2:	1.550	1.551	1.554	1.571
a_3:	2.321	2.310	2.330	2.376
a_4:	5.642	5.651	5.694	5.913

Table 3-12. a_1, a_2, a_3, a_4, and a_5 values for eight-stage, four-bit, all-pass network phase shifter for a bandwidth of 500:1.

Phase ϕ_m:	**22.5°**	**45°**	**90°**	**180°**
a_1:	1.023	1.046	1.097	1.203
a_2:	2.002	1.978	2.013	2.012
a_3:	4.039	4.034	4.214	4.221
a_4:	5.737	5.759	6.080	6.096
a_5:	16.580	16.368	17.714	17.764

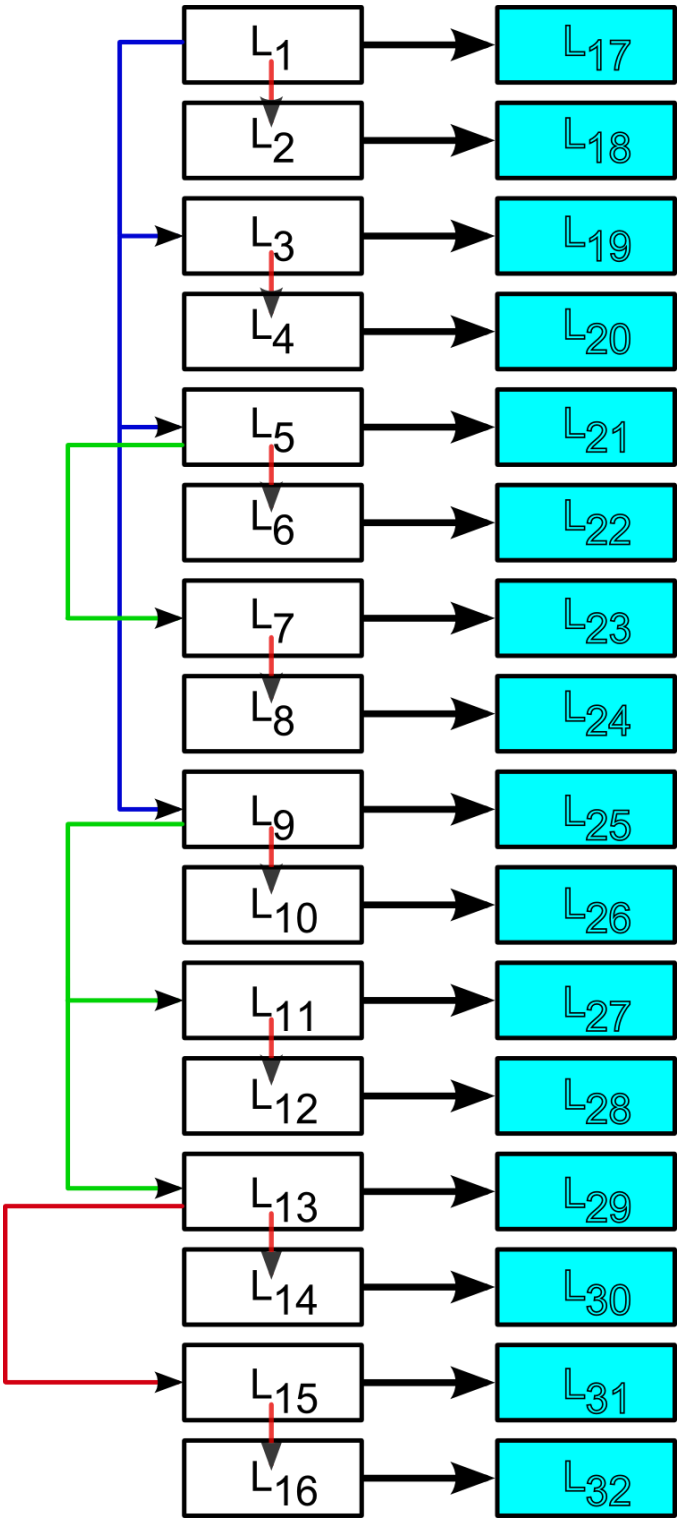


Figure 3-19. The sequence and ability to derive the inductor formulae diagram for sixteen-stage, all-pass network phase shifter.

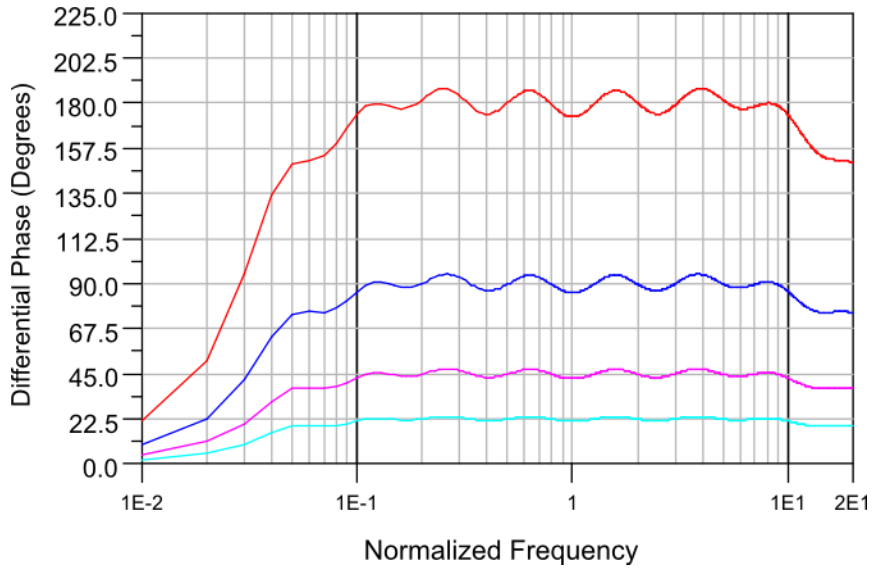


Figure 3-20. Ideal differential phase characteristics of eight-stage all-pass network phase shifter (Frequency is scaled to center frequency-normalized frequency in logarithmic scale) for a bandwidth of 100:1 (between the black vertical lines).

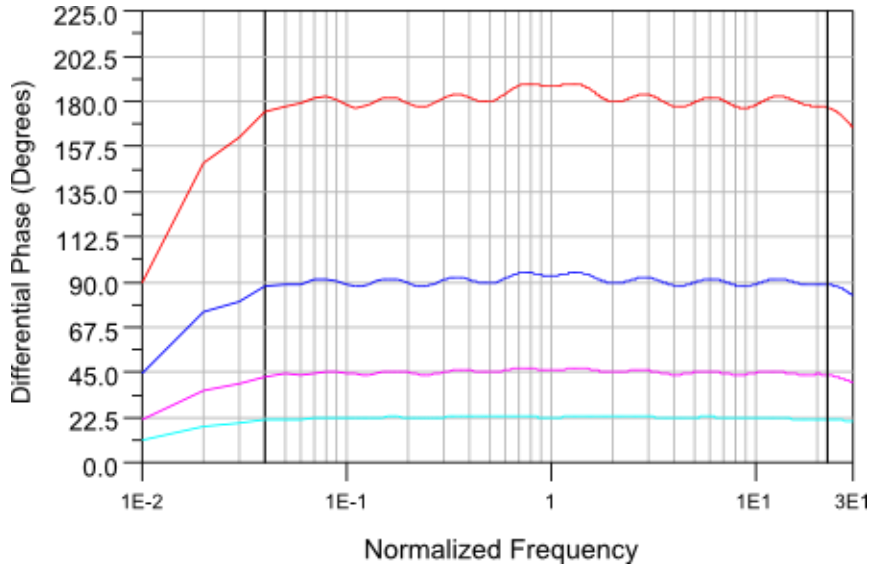


Figure 3-21. Ideal differential phase characteristics of sixteen-stage all-pass network phase shifter (Frequency is scaled to center frequency-normalized frequency in logarithmic scale) for a bandwidth of 500:1 (between the black vertical lines).

Using the above found design parameter values, and the formulas; the ideal phase shift results are presented in Figure 3-20, and Figure 3-21 for eight-stage, and sixteen-stage all-pass network phase shifters, respectively. The ideal differential phase shift

related data are provided in Table 3-13, and Table 3-14 for eight-, and sixteen-stage all-pass network phase shifters, respectively. It can be observed from the tables that the rms phases are very close to the desired phase shift values, the P-P phase flatness values are in good condition. Finally, the rms phase errors are less than 4° for each of the phase shift bits. A generalized formula set is introduced. An example calculation method is provided on sixteen-stage version. The whole equation set of lumped elements is not provided. The formulations can be applied to any number of stages, where the stage number is a power of 2. Three-stage can also be characterized with three design parameters. However, five-stage cannot achieve the desired phase characteristics with four design parameters. The decreased number of stages causes the circuit to be unbalanced in terms of phase performance. The reason that the three-stage can be characterized and achieve satisfactory performance is that there is only one-stage missing from four-stage and phase performances can be achieved with higher phase errors compared to four-stage version. In five-stage, six-stage, and etc. the phase performances are bad with using design parameters approach.

In the next section, various phase shifters ideal design's lumped element values and differential phase shift performances are provide

Table 3-13. Differential phase shift related data for each phase shift bit, for eight-stage phase shifter, and bandwidth of 100:1.

Bit	rms Phase (°)	P-P flatness(°)	rms PE (°)
22.5°	22.47	2.47	0.64
45°	44.97	4.91	1.26
90°	89.97	9.26	2.35
180°	179.94	14.18	3.64

Table 3-14. Differential phase shift related data for each phase shift bit, for sixteen-stage phase shifter, and bandwidth of 500:1.

Bit	rms Phase (°)	P-P flatness (°)	rms PE (°)
22.5°	22.18	1.99	0.50
45°	44.66	4.34	0.79
90°	89.86	6.88	1.54
180°	179.88	13.93	2.60

3.4 Achieving Satisfactory Phase Characteristics for Stage Numbers Other Than 2^{n-1}

Similar to the two-stage design procedure, three-stage all-pass network can also be designed. An illustration of one of the three-stage phase shift bit is given in Figure 3-22.

As it is already mentioned earlier in this chapter, while increasing number of stages, a third design parameter "a_3" must be introduced to characterize the three-stage differential phase response as;

$$\begin{aligned}\phi = 2\Big\{&\tan^{-1}\left(a_1a_2a_3\Omega - \frac{1}{a_1a_2a_3\Omega}\right) + \tan^{-1}\left(\frac{a_1a_2\Omega}{a_3} - \frac{a_3}{a_1a_2\Omega}\right)\\ &+ \tan^{-1}\left(\frac{a_1\Omega}{a_2a_3} - \frac{a_2a_3}{a_1\Omega}\right)\\ &- \tan^{-1}\left(\frac{\Omega}{a_1a_2a_3} - \frac{a_1a_2a_3}{\Omega}\right)\\ &- \tan^{-1}\left(\frac{a_2\Omega}{a_1a_3} - \frac{a_1a_3}{a_2\Omega}\right) - \tan^{-1}\left(\frac{a_2a_3\Omega}{a_1} - \frac{a_1}{a_2a_3\Omega}\right)\Big\}\end{aligned} \tag{3.30}$$

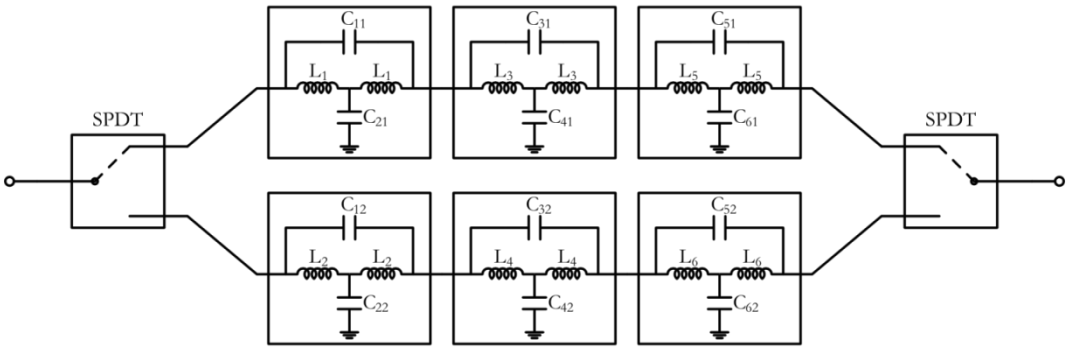


Figure 3-22. The three-stage all-pass network phase shifter with component names. Only one bit is illustrated.

The three design parameters a_1, a_2, and a_3 are optimized in order to give the desired phase shift with the smallest possible phase error for a bandwidth of 6:1, and for 22.5°, 45°, 90°, and 180°. The design parameter values are found as in Table 3-15. The related phase shifts are given in Figure 3-23 for 22.5° (turquoise line), 45° (pink line), 90° (blue line), and 180° (red line). The differential phase related data, and error analysis are given in Table 3-16. The desired phase shifts are achieved in rms term, and the rms phase errors are low enough to consider the design to be successful.

Table 3-15. a_1, a_2, and a_3 values for three-stage, four-bit, all-pass network phase shifter.

Phase ϕ_m:	22.5°	45°	90°	180°
a_1:	1.034	1.070	1.146	1.334
a_2:	1.513	1.515	1.526	1.579
a_3:	1.542	1.545	1.556	1.612

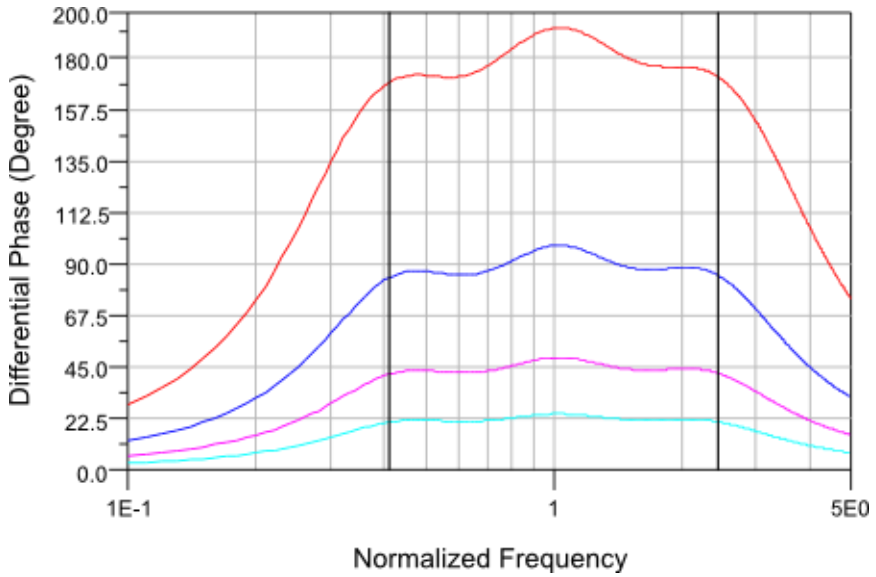


Figure 3-23. Differential phase shift plots for 22.5° (turquoise line), 45° (pink line), 90° (blue line), and 180° (red line), for three-stage 6:1 bandwidth.

Table 3-16. Differential phase shift related data for each phase shift bit, for three-stage phase shifter, and bandwidth of 6:1.

Bit	Mean Phase (°)	Maximum Phase Error (°)	Rms Phase Error (°)
22.5°	22.18	1.99	0.50
45°	44.66	4.34	0.79
90°	89.86	6.88	1.54
180°	179.88	13.93	2.60

Using the optimized design parameters, and proper choice of center frequency, the lumped element values can be calculated as given in Table 3-17.

Table 3-17. The equations of the lumped components for three-stage design. $\boldsymbol{Z_0}$ is the system impedance.

$L_1 = \frac{Z_0}{a_1 a_2 a_3 \omega_m}$	$C_{11} = \frac{1}{2Z_0 a_1 a_2 a_3 \omega_m}$	$C_{21} = \frac{2}{a_1 a_2 a_3 Z_0 \omega_m}$
$L_2 = \frac{a_1 Z_0}{a_2 a_3 \omega_m}$	$C_{12} = \frac{a_1}{2a_2 a_3 Z_0 \omega_m}$	$C_{22} = \frac{2a_1}{a_2 a_3 Z_0 \omega_m}$
$L_3 = \frac{a_2 Z_0}{a_1 a_3 \omega_m}$	$C_{31} = \frac{a_2}{a_1 a_3} \frac{1}{2Z_0 \omega_m}$	$C_{41} = \frac{a_2}{a_1 a_3} \frac{2}{Z_0 \omega_m}$
$L_4 = \frac{a_1 a_2}{a_3} \frac{Z_0}{\omega_m}$	$C_{32} = \frac{a_1 a_2}{a_3} \frac{1}{2Z_0 \omega_m}$	$C_{42} = \frac{a_1 a_2}{a_3} \frac{2}{Z_0 \omega_m}$
$L_5 = \frac{a_2 a_3}{a_1} \frac{Z_0}{\omega_m}$	$C_{51} = \frac{a_2 a_3}{a_1} \frac{1}{2Z_0 \omega_m}$	$C_{61} = \frac{a_2 a_3}{a_1} \frac{2}{Z_0 \omega_m}$
$L_6 = \frac{a_1 a_2 a_3 Z_0}{\omega_m}$	$C_{52} = \frac{a_1 a_2 a_3}{2Z_0 \omega_m}$	$C_{62} = \frac{2a_1 a_2 a_3}{Z_0 \omega_m}$

However, it is already mentioned early in this chapter, like the three-stage design, the stage numbers other than the power of 2 has an unbalanced phase response. Five-stage design cannot be achieved with this methodology. In order to achieve satisfactory results for such number of stages, one can increase the degree of freedom. Considering the center frequency of every all-pass filter as a degree of freedom, good phase performances can be achieved. There are examples of similar kind of design methodologies in the literature [23]-[26].

Unlike the design procedure described in [26], for three-stage the degree of freedom is assumed to be 6, since there are six all-pass filters for three-stage network. $\bar{\omega}_1$, $\bar{\omega}_2$, $\bar{\omega}_3$, $\bar{\omega}_4$, $\bar{\omega}_5$, and $\bar{\omega}_6$are the center frequencies of the all-pass filters, normalized to center frequency ω_m. These normalized center frequencies are found for 4-bit phase shifter and for a 6:1 bandwidth design, and they are summarized in Table 3-18. The differential phase responses of four bits are given in Figure 3-24. Phase related data are provided in

Table 3-19. Compared with the above presented design parameter methodology, the rms phases are closer to the desired phases, and the rms phase errors are improved. However, P-P flatness is increased for all bits, which is one of the disadvantages of this methodology. The other disadvantage can be seen in the practical design step. The unbalanced lumped element values between the upper and lower branch cause the circuit to have amplitude imbalance.

Table 3-18. $\bar{\omega}_1$, $\bar{\omega}_2$, $\bar{\omega}_3$, $\bar{\omega}_4$, $\bar{\omega}_5$, and $\bar{\omega}_6$ values for three-stage, four-bit, all-pass network phase shifter.

Phase ϕ_m:	**22.5°**	**45°**	**90°**	**180°**
$\bar{\omega}_1$:	0.456	0.471	0.502	0.567
$\bar{\omega}_2$:	0.424	0.407	0.374	0.298
$\bar{\omega}_3$:	0.976	0.999	1.050	1.159
$\bar{\omega}_4$:	0.926	0.900	0.854	0.777
$\bar{\omega}_5$:	2.215	2.300	2.510	3.166
$\bar{\omega}_6$:	2.053	1.975	1.841	1.619

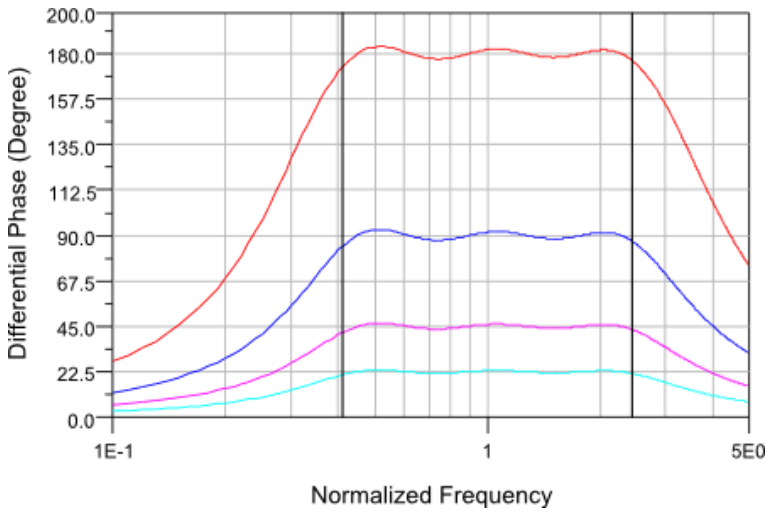


Figure 3-24. Differential phase shift plots for 22.5° (turquoise line), 45° (pink line), 90° (blue line), and 180° (red line) with achieving optimum center frequencies of all-pass filters, for three-stage 6:1 bandwidth.

Table 3-19. Differential phase shift related data for each phase shift bit, for three-stage phase shifter with optimum center frequencies of all-pass filters, and bandwidth of 6:1 .

Bit	rms Phase (°)	P-P flatness (°)	rms PE (°)
22.5°	22.50	2.35	0.43
45°	44.99	4.68	0.83
90°	89.99	8.40	1.48
180°	180.00	10.03	1.75

The calculation of lumped elements differs a little from the above discussed methodology. The inductors can be found as;

$$L_j = \frac{Z_0}{\omega_j} \tag{3.31}$$

$$\omega_j = \overline{\omega_j}\omega_m;\ \omega_m\text{: center frequency} \tag{3.32}$$

$$j = 1, 2, \ldots 2n;\ n\text{: stage number} \tag{3.33}$$

The capacitors can be calculated from equations (3.26a-b). Any other non-power-of-2 stages can be designed with this methodology. Three-stage is given in the following sub-section as an example of this methodology.

3.5 Calculated lumped element values for two-, and three-stage all-pass network phase shifters, and ideal phase shift characteristics

It is already mentioned in Chapter 1, that the main purpose of this thesis is to cover 1 to 6 GHz frequency band with a number of phase shifters. For that reason, the designed phase shifters are two-stage; 1 to 2 GHz, 2 to 4 GHz, 3 to 6 GHz, and three-stage; 1 to 6 GHz, 4-bit phase shifters.

To design these phase shifters, one must start with the ideal design of phase shifters. Following the two-stage design formulations, and with a proper choice of center frequency; the lumped element values for 1 to 2 GHz phase shifter are provided in Table 3-20. Similarly the lumped element values are calculated for 2 to 4 GHz and 3 to 6 GHz, they are presented in Table 3-21, and Table 3-22, respectively.

For 1 to 6 GHz design, one should follow the three-stage design equations and parameters as presented above in this section. A proper center frequency is chosen and the calculated lumped element values are presented in Table 3-23.

Table 3-20. The resultant lumped element values for 1 to 2 GHz phase shifter for 22.5°, 45°, 90°, and 180° phase shift bits (Inductance in nH, capacitance in pF).

22.5° Phase Shift Bit				**45° Phase Shift Bit**			
L_1=8.51	L_2=3.31	L_3=3.58	L_4=7.87	L_1=8.89	L_2=3.17	L_3=3.71	L_4=7.60
C_{11}=1.70	C_{12}=0.66	C_{31}=0.72	C_{32}=1.57	C_{11}=1.78	C_{12}=0.63	C_{31}=0.74	C_{32}=1.52
C_{21}=6.81	C_{22}=2.64	C_{41}=2.88	C_{42}=6.28	C_{21}=7.11	C_{22}=2.53	C_{41}=2.97	C_{42}=6.08
90° Phase Shift Bit				**180° Phase Shift Bit**			
L_1=9.71	L_2=2.88	L_3=3.97	L_4=7.09	L_1=12.50	L_2=2.25	L_3=4.50	L_4=6.26
C_{11}=1.95	C_{12}=0.58	C_{31}=0.79	C_{32}=1.42	C_{11}=2.50	C_{12}=0.45	C_{31}=0.90	C_{32}=1.25
C_{21}=7.82	C_{22}=2.30	C_{41}=3.16	C_{42}=5.67	C_{21}=10.00	C_{22}=1.80	C_{41}=3.60	C_{42}=5.00

Table 3-21. The resultant lumped element values for 2 to 4 GHz phase shifter for 22.5°, 45°, 90°, and 180° phase shift bits (Inductance in nH, capacitance in pF).

22.5° Phase Shift Bit				**45° Phase Shift Bit**			
L_1=4.26	L_2=1.66	L_3=1.79	L_4=3.94	L_1=4.46	L_2=1.58	L_3=1.85	L_4=3.80
C_{11}=0.85	C_{12}=0.33	C_{31}=0.36	C_{32}=0.79	C_{11}=0.89	C_{12}=0.32	C_{31}=0.37	C_{32}=0.76
C_{21}=3.40	C_{22}=1.32	C_{41}=1.44	C_{42}=3.15	C_{21}=3.56	C_{22}=1.28	C_{41}=1.48	C_{42}=3.04
90° Phase Shift Bit				**180° Phase Shift Bit**			
L_1=4.89	L_2=1.44	L_3=1.98	L_4=3.55	L_1=6.25	L_2=1.13	L_3=2.25	L_4=3.13
C_{11}=0.98	C_{12}=0.29	C_{31}=0.40	C_{32}=0.71	C_{11}=1.25	C_{12}=0.23	C_{31}=0.45	C_{32}=0.63
C_{21}=3.92	C_{22}=1.16	C_{41}=1.60	C_{42}=2.84	C_{21}=5.00	C_{22}=0.92	C_{41}=1.80	C_{42}=2.52

Table 3-22. The resultant lumped element values for 3 to 6 GHz phase shifter for 22.5°, 45°, 90°, and 180° phase shift bits (Inductance in nH, capacitance in pF).

22.5° Phase Shift Bit				**45° Phase Shift Bit**			
L_1=2.84	L_2=1.10	L_3=1.20	L_4=2.62	L_1=2.96	L_2=1.06	L_3=1.24	L_4=2.53
C_{11}=0.57	C_{12}=0.22	C_{31}=0.24	C_{32}=0.53	C_{11}=0.59	C_{12}=0.21	C_{31}=0.25	C_{32}=0.50
C_{21}=2.27	C_{22}=0.88	C_{41}=0.95	C_{42}=2.10	C_{21}=2.37	C_{22}=0.84	C_{41}=0.99	C_{42}=2.03
90° Phase Shift Bit				**180° Phase Shift Bit**			
L_1=3.26	L_2=0.96	L_3=1.32	L_4=2.36	L_1=4.17	L_2=0.75	L_3=1.50	L_4=2.09
C_{11}=0.65	C_{12}=0.19	C_{31}=0.26	C_{32}=0.47	C_{11}=0.83	C_{12}=0.15	C_{31}=0.30	C_{32}=0.42
C_{21}=2.61	C_{22}=0.77	C_{41}=1.06	C_{42}=1.89	C_{21}=3.33	C_{22}=0.60	C_{41}=1.20	C_{42}=1,67

After the calculation of the lumped element values in ideal, the circuit is constructed in ADS 2009. The switching elements are assumed to be ideal SPDTs, since the whole circuit, for now, is composed of ideal lumped elements. Following the construction of the circuit, the ideal simulation results are obtained. Note that the return loss, and insertion loss results are not provided in here, because of the fact that the all-pass filters are naturally matched to system impedance and there is no resistance is used

in the topology. The differential phase shifts for four phase shifters are given in Figure 3-25, Figure 3-26, Figure 3-27, and Figure 3-28; addition to those the differential phase related data and error analysis are given in Table 3-24, Table 3-25, Table 3-26, and Table 3-27; for 1 to 2 GHz, 2 to 4 GHz, 3 to 6 GHz, and 1 to 6 GHz, respectively. In all of the phase shifter designs, one can say that the designs are close to the desired phase shift values. Moreover, the phase flatness of the phase shifters is in good condition; proved by the fact that the rms phase errors are small.

Table 3-23. The resultant lumped element values for 1 to 6 GHz phase shifter for 22.5°, 45°, 90°, and 180° phase shift bits (Inductance in nH, capacitance in pF).

22.5° Phase Shift Bit					
L_1= 1.18	L_2= 1.27	L_3= 2.86	L_4= 3.03	L_5= 6.80	L_6= 7.35
C_{11}= 0.24	C_{12}= 0.25	C_{31}= 0.57	C_{32}= 0.61	C_{51}= 1.36	C_{52}= 1.47
C_{21}= 0.94	C_{22}= 1.02	C_{41}= 2.29	C_{42}= 2.42	C_{61}= 5.44	C_{62}= 5.88
45° Phase Shift Bit					
L_1=1.30	L_2=1.50	L_3=2.95	L_4=3.29	L_5=6.57	L_6=7.65
C_{11}=0.26	C_{12}=0.30	C_{31}=0.59	C_{32}=0.66	C_{51}=1.31	C_{52}=1.53
C_{21}=1.04	C_{22}=1.20	C_{41}=2.36	C_{42}=2.63	C_{61}=5.26	C_{62}=6.12
90° Phase Shift Bit					
L_1=1.22	L_2=1.64	L_3=2.82	L_4=3.47	L_5=6.08	L_6=8.27
C_{11}=0.24	C_{12}=0.33	C_{31}=0.56	C_{32}=0.69	C_{51}=1.22	C_{52}=1.65
C_{21}=0.98	C_{22}=1.31	C_{41}=2.26	C_{42}=2.78	C_{61}=4.86	C_{62}=6.62
180° Phase Shift Bit					
L_1=0.97	L_2=1.85	L_3=2.55	L_4=3.81	L_5=5.33	L_6=10.39
C_{11}=0.19	C_{12}=0.37	C_{31}=0.51	C_{32}=0.76	C_{51}=1.07	C_{52}=2.08
C_{21}=0.78	C_{22}=1.48	C_{41}=2.04	C_{42}=3.05	C_{61}=4.26	C_{62}=8.31

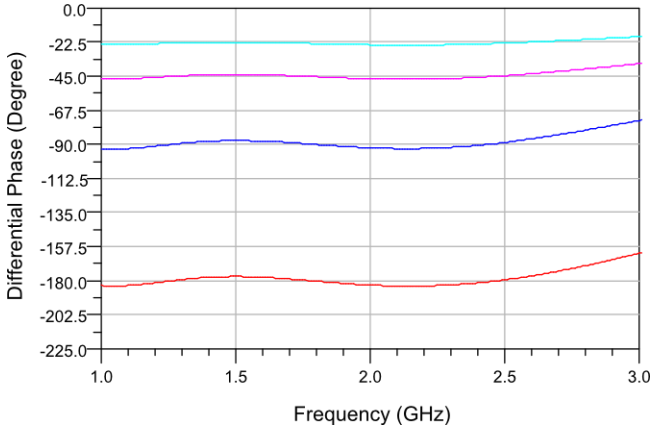


Figure 3-25. Ideal differential phase characteristics of two-stage, four-bit, 1 to 2 GHz phase shifter.

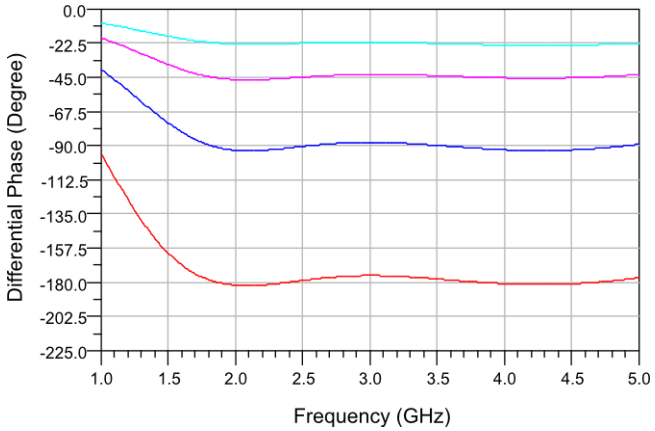


Figure 3-26. Ideal differential phase characteristics of two-stage, four-bit, 2 to 4 GHz phase shifter.

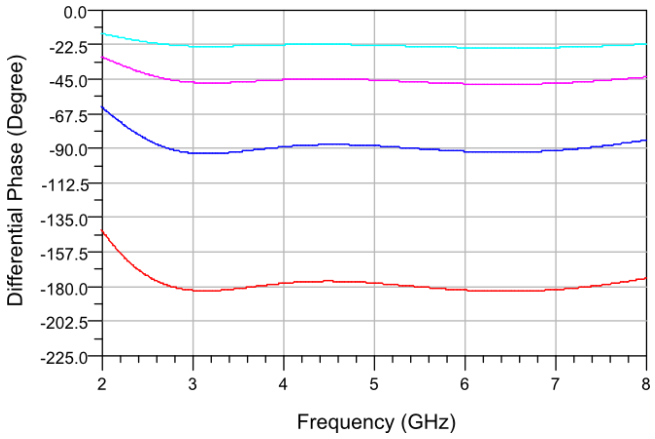


Figure 3-27. Ideal differential phase characteristics of two-stage, four-bit, 3 to 6 GHz phase shifter.

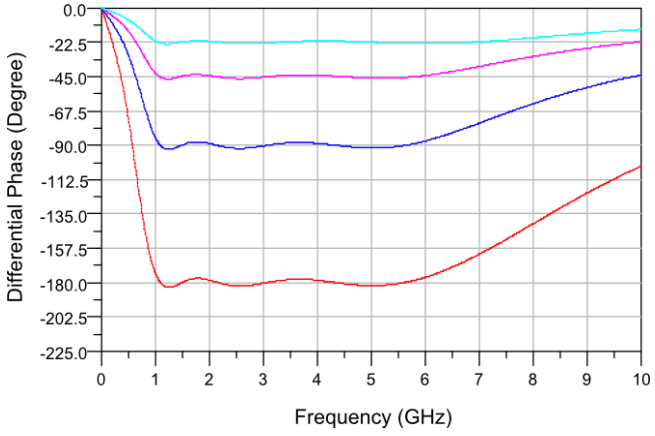


Figure 3-28. Ideal differential phase characteristics of three-stage, four-bit, 1 to 6 GHz phase shifter.

Table 3-24. Differential phase shift related data for each phase shift bit, for two-stage, 1to 2 GHz phase shifter.

Bit	Mean Phase (°)	Maximum Phase Error (°)	Rms Phase Error (°)
22.5°	23.35	0.96	0.53
45°	45.24	1.59	1.04
90°	90.01	4.72	2.35
180°	180.23	3.42	2.17

Table 3-25. Differential phase shift related data for each phase shift bit, for two-stage, 2 to 4 GHz phase shifter.

Bit	Mean Phase (°)	Maximum Phase Error (°)	Rms Phase Error (°)
22.5°	22.69	1.04	0.53
45°	44.50	2.22	1.16
90°	90.31	3.11	1.87
180°	178.50	3.79	2.19

Table 3-26. Differential phase shift related data for each phase shift bit, for two-stage, 3 to 6 GHz phase shifter.

Bit	Mean Phase (°)	Maximum Phase Error (°)	Rms Phase Error (°)
22.5°	23.17	1.23	0.59
45°	46.21	1.81	1.00
90°	90.01	3.54	1.95
180°	179.43	3.45	2.16

Table 3-27. Differential phase shift related data for each phase shift bit, for three-stage, 1 to 6 GHz phase shifter.

Bit	Mean Phase (°)	Maximum Phase Error (°)	Rms Phase Error (°)
22.5°	22.47	1.03	0.69
45°	45.06	2.44	0.90
90°	90.03	4.98	1.49
180°	180.05	6.23	1.75

Remember that, the theories of one-stage, two-stage, three-stage, and four-stage are provided, after introducing the theory of all-pass filter. The given design parameter values are extended for a 6-bit phase shifter design for one-stage and two-stage. Also, generalized theory of how to design ideal all-pass network phase shifter is given, together with the found design parameter values for three-stage, four-stage, eight-stage, and sixteen-stage, is also given for the first time in literature. The designed phase shifter component values are calculated and tabulated. The ideal phase shifts are given with additional data, and error analysis.

As already mentioned, the basic components of this topology are capacitors and inductors. Hence, a considerable amount of time has spent on the design, fabrication, and measurements of these components. For that reason, the next chapter is dedicated to lumped elements, which are the critical components completing the desired phase shifters.

CHAPTER 4

SURFACE MICROMACHINED LUMPED ELEMENTS: SQUARE PLANAR SPIRAL INDUCTORS (SPSIs) AND METAL-INSULATOR-METAL (MIM) CAPACITORS

In the previous chapter, characteristics of an all-pass filter are introduced. Based on this information, the theory of one-stage, and two-stage all-pass network phase shifters are introduced. Different than presented in [21], the 5.625°, and 11.25° phase shift design parameters are found for one-stage and two-stage phase shifters. Additional bandwidth, phase, and phase error analysis are done for various design parameter value cases. In addition to those, a generalized all-pass network formulization is introduced for increased number of stages with power of 2. Furthermore, design methodology for different number of stages is given. For all of these, bandwidth, phase, and phase error analysis are done. At the last part of the previous chapter, the desired lumped element values are calculated and tabulated.

Remember that the basic building elements for the phase shifters are the lumped inductors and capacitors. For the phase shifters to be designed with satisfactory performances, care should be taken for the lumped elements.

The technology has the most important role in design of the lumped elements. Our in-house (METU-MEMS) technology offers crucial technological opportunities; moreover with this technology we are able to realize surface micromachining components.

For these reasons, the phase shifters are realized with Square Planar Spiral Inductors (SPSIs), and Metal-Insulator-Metal (MIM) capacitors. All of these lumped elements are designed according to the technology parameters of surface micromachining.

The contents of this chapter can be summarized as follows;

- Inductors
  - Basics
  - Previous works from literature
  - Design method of SPSI, designed SPSI
  - Mitered SPSIs: a small change in the geometry, a small improvement in Q-factor and SRF
  - Fabrication and Measurement of SPSIs
- Capacitors
  - Basics
  - Previous works from literature
  - Design method of MIM capacitors

4.1 Introduction

A capacitor or an inductor is accepted as a lumped element based on the assumption that there should not be any significant phase shift between the input and output ports of the component, i.e., the maximum dimension of the component should not exceed $\lambda/20$. λ is the guided wavelength in the desired system.

Lumped elements are extensively used in many applications. Looking from a historical perspective, lumped elements are first used up to MHz frequency range. After technological improvements, such as in Microwave Integrated Circuits (MICs), lumped elements are extensively used for frequencies up to around 3 GHz. This usage decreased the size of the circuits compared to the use of distributed components [27]-[31], [33]; as in constructing microwave amplifiers. The use of lumped elements is increased with the improvements in film technology also [32]. With the

advancements in integrated circuits, i.e. Monolithic Microwave Integrated Circuits (MMICs), the RF components showed better performances for even higher frequencies [34],[35]. While advancements achieved in MICs, and MMICs, the production technologies have, also, improved, and so does the application range of the lumped components [27], [33], [36], [37]. As for today, lumped elements can be used up to 100 GHz due to improvements in production technologies; such as etching the substrate under the lumped components, patterning ground planes for microstrip implemented lumped components, etc.

Lumped elements are extensively preferred to distributed microwave components to decrease the size of the circuit. The main reason of this preference is the advancements in mobile, wireless communication technologies. The advantages of lumped elements roughly are; small size, low cost, well-known circuit topologies and wider band characteristics. Although lumped elements have many advantages, there are, certainly, disadvantages like; low Q-factor, higher insertion loss, etc.

In this work, lumped elements are designed to construct the overall phase shifter circuits, because of the following reasons;

- Octave-band and ultra wide-band (UWB) phase shifters are to be constructed.
- Well-known performances, and well-predicted parasitics of the lumped elements give us a chance to tune the circuit to a desired performance level [40] compared to COTS implementations [41].
- Since the lower frequency is as low as 1 GHz, use of distributed components requires a considerable amount of space. Hence cost would be increased.

In the next sub-section, inductors basics are presented, some previous works presented in literature are examined, design method of square planar spiral inductors is explained, and fabrication of the designed inductors and the measurements are presented.

4.2 Square Planar Spiral Inductors (SPSIs): Design, Fabrication and Measurements

It is already mentioned that basic building blocks of the designed phase shifters are square planar spiral inductors and metal-insulator-metal capacitors. Understanding and designing of MIM capacitors are easier than the SPSIs. For that reason, before fully fabricating the phase shifters, SPSIs with various diameters, turn numbers, trace widths, and spacings are designed, fabricated and measured.

In the following sub-sections basics of inductors, some previous works presented in literature, design procedure of SPSIs, fabrication, and measurements are presented.

4.2.1 Inductor Basics

Inductor is ideally defined as *"a conductor arranged in an appropriate shape to supply a certain amount of self-inductance"* [38]. Microwave and millimeter-wave inductors have several different geometrical shapes; such as, planar inductors, single-loop inductors, single or multiple wire bonds, chip inductors, etc. For all these forms of inductors a common inductance formula can be given for perfect conductors;

$$L = \mu_0 \frac{1}{\mathrm{I}} \oint H.dl \tag{4.1}$$

where I is the current through the conductor, H is the magnetic field. This inductance formula is also known as the self-inductance. The stored magnetic energy can be expressed using the inductance and the current through conductor;

$$W_m = \frac{L\mathrm{I}^2}{2} \tag{4.2}$$

The mutual inductance is one of the most important parameters for a system of at least two current carrying conductors in proximity. As a matter of fact, when the two currents flow in the same direction the mutual inductance has positive sign, i.e., additive, and when the two currents flow in the opposite direction the mutual inductance has negative sign, i.e., destructive. The mutual inductance formulae can be given as [27];

$$M = \frac{L_a - L_o}{2} \tag{4.3}$$

L_a is defined as the total inductance of the two conductors when the currents flow in the same direction. L_o is defined as the total inductance of the two conductors when the currents flow in the opposite direction.

Then the total inductance can be written as [27];

$$L_t = L + M; \textit{ currents in the same direction} \tag{4.4a}$$
$$L_t = L - M; \textit{ currents in the opposite direction} \tag{4.4b}$$

This formula is critical to understand the total inductance concept of a number of turns planar spiral inductors, since there are multiple conductors in the vicinity of each other form a system with currents flow in the same direction and at the same time in the opposite direction.

Another critical parameter about the inductors is the quality-factor, which gives an idea about the loss, series parasitic resistance, inductance, etc., about the component of the concern. The quality-factor affects many circuits; such as the phase noise of an oscillator (proportional to the relation $1/Q^2$), the power consumption of an oscillator or an amplifier, or the loss of a matching network, filter, and etc., or the noise figure of a system with the relation $1/Q$, and the gain of an amplifier with the proportion Q [39]. Hereby, one can understand the importance of the quality-factor of the passives like inductors. There are several Q-factor definitions for inductors in literature. The very basic one is like in the following equation;

$$Q = \frac{\omega W_s}{P_D} \tag{4.5}$$

where W_s is the stored energy in the inductor, and P_D is the dissipated power in the inductor [27]. On the other hand, the conventional definition of the Q-factor (effective Q-factor) is related to the impedance seen from port 1 [27], [39], [42] as in the following equations;

$$Q = \frac{Im[Z_{11}]}{Re[Z_{11}]} \tag{4.6a}$$

$$Q = -\frac{Im[Y_{11}]}{Re[Y_{11}]} \tag{4.6b}$$

The complex impedance representation can also be used. But for the sake of simplicity during the design procedure of the phase shifters, related to the employed computer aided programs, S-parameter representation is assumed. For that reason, the quality factor representation can be modified as in (4.7), assuming that the inductor's port 2 (output port) is short circuited to ground [39].

$$Q = \frac{2|Im[S_{11}]|}{1 - |S_{11}|^2} \tag{4.7}$$

As mentioned before, quality-factor is a measure of many things. From the quality-factor, one can also find the self-resonant frequency of an inductor. The frequency at which the quality-factor is zero according to (4.7) is the first self-resonant frequency of the inductor. The same self-resonant frequency can be obtained as the inductive reactance is equal to the capacitive reactance at a specific frequency, or the polarity of phase of S_{11} changes sign.

Self-resonant frequency is another critical parameter that a designer must be aware of. For instance, one cannot construct a wideband circuit with inductors which has self-resonance frequencies within the operational band. After the resonance frequency, the inductor behaves like a capacitor.

There are many properties of inductors other than the above mentioned ones. For example, maximum current rating, maximum power handling, temperature range of operation, and etc. Such properties may be crucial. However, these properties are not investigated deeply in here.

In the next chapter, a literature review on surface micromachined lumped components is given. The importance of high-Q lumped inductors is discussed for different applications.

4.2.2 Literature Review on Surface Micromachined Inductors

Microwave and RF inductors have been extensively studied over several decades; still there are improvements on surface micromachined inductors. The main objective of these works is to improve the quality-factor, and SRF.

There are plenty of methods to fulfill the duty of improvement of inductors [43]-[70]. In a general approach the methods can be summarized as follows;

- Using insulating substrates instead of semiconductor, or high resistivity substrates, to decrease the loss due to the substrate.
- Etching the substrate underneath the inductors to decrease the loss due to the substrate and to decrease the shunt parasitic capacitances of the inductors.
- Using thick metallization layer to decrease the metal losses.
- Using thick polyimide (around 10 μm), or any other low-K, low-loss dielectrics to form a substrate thinner than the commercially used substrates, and to decrease the shunt parasitics.
- Applying passivation under the structures, and above the high-resistivity silicon substrates [84], [85].

Some works use one of the above, or some works use a combination of two or three methods to increase the quality-factor and SRF of the inductors.

Quality-factor and SRF improvements by changing or adding a new step in the process must have the characteristics of compatibility with the existing most used processes, and not increasing the cost of fabrication. For that reason, passivation methodology is used. In [84], the passivation is formed between the high-resistivity silicon substrate and silicon dioxide layer with introducing Ar ions. This is done to reduce the accumulation of the charges in the substrate and in the layer between the substrate and oxide layer, which is caused by the conductivity of the substrate. Conductivity of the high-resistivity silicon substrate affects the performances of the inductors and capacitors. Implanting Ar ions between the oxide and substrate traps the charges in

the upper layer, and hence passives like capacitors and inductors have improved performances. Another passivation approach is introducing a polysilicon layer between the substrate and oxide [85].

In [43], a process compatible with standard silicon IC processes is done using thick polyimide and thick metallization. The main aim of this work is to achieve performances comparable with GaAs MMIC fabricated components. For the same reason, not only planar inductors are produced, but also transmission lines. The measured transmission lines have insertion losses around 0.2 dB for CPW, and 0.3 dB for microstrip at 4 GHz. The fabricated and measured sample inductor has an inductance of around 10 nH with SRF at 6 GHz, and quality-factor equal to 5.5 at 1.2 GHz. A passivation layer is formed onto a high resistivity substrate in [44]. Fabrication technology is a high-speed complementary bipolar process. The passivation layer is 1.2 µm SiON, 0.1 µm Si_3N_4, and 1.5 µm SiO_2 having the advantages of reducing the substrate losses and parasitic capacitance of the inductors. Also, thick metallization with gold is used. Achieved quality-factor of inductors is around 12. To prove the use of fabricated inductor, a high-pass filter and a single-balanced mixer are produced. As the technology improves, application frequencies approach to 100 GHz. In [45], planar and 3-D inductors are fabricated on silicon by shrinking the inductor areas as low as around 50 µm by 50 µm with narrow trace widths and spacings. Inductance values around pH levels are fabricated with this method and it is proven that the SRF of the inductors are beyond 100 GHz. To further prove the concept millimeter-wave mixer and VCO are produced and measured for 60 GHz and 77 GHz which are the WLAN and automotive radar frequency bands.

Another approach for the planar inductors is patterning the ground [46]. The parasitic resistances and capacitances are decreased with patterned ground of the microstrip inductors. Hence the quality-factor is improved with SRF. Using the patterned ground shield method and a new etching method of substrate, i.e., backside inductively coupled-plasma (ICP) deep-trench [47], four different inductor versions are compared. The versions of these inductors are the standard inductor, ICP etched

inductor, patterned ground shield inductor, and ICP etched patterned ground shield inductor. ICP etched inductor is chosen as an appropriate method, considering the compatibility to a standard RFIC process and the performance of the inductors. Using the same ICP process, millimeter-wave applications of inductors can also be accomplished [48].

All of the above mentioned works have novelties in fabrication processes. Improvement can also be done by optimizing the layout of the inductor [49]. In the mentioned work, inductors with constant trace widths, and variable width inductor are compared in term of quality-factor. It is seen that the optimized various width inductor have superiority to other constant value trace width inductors in term of quality-factor. The optimized layout can be seen in Figure 4-1.

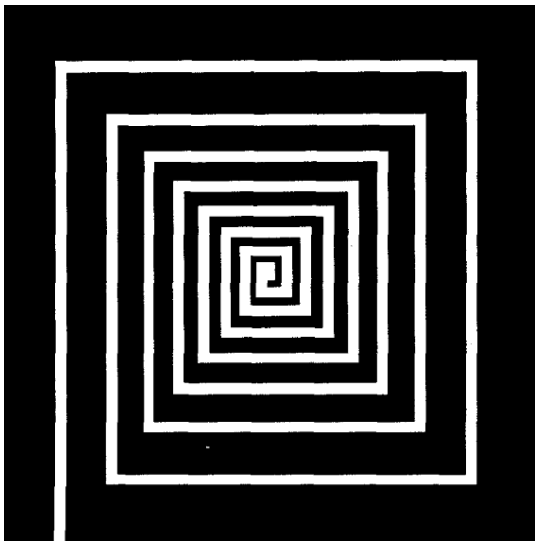


Figure 4-1. Optimized layout of a 20 nH inductor [49].

A common method in a general manner is to suspend the inductors to improve the Q-factor and SRF. However, the method of suspension differs for fabrication related parameters, design, etc. In [50], the traces of spiral inductors are first formed with polysilicon and cavity under inductors are formed with a height of 30 µm. Finally, in order to decrease the resistive loss Cu is plated. Inner surfaces of the cavity also Cu plated, thus, a good RF ground is formed underneath the inductor. This metallization of the cavity, also, helps to decrease the crosstalk between two adjacent inductors.

High-Q (around 30) is achieved with a SRF of higher than 10 GHz. A fabricated example is given in Figure 4-2. The suspended inductors can be formed with many techniques. As already mentioned the most common method is etching the substrate underneath the inductors. While doing this, one should care the fabrication costs, too. For example in [51], a maskless front side micromachining procedure is applied. This method ensures that all of the traces are separately suspended, which decreases the inter-turn capacitances and hence increase the Q-factor and SRF.

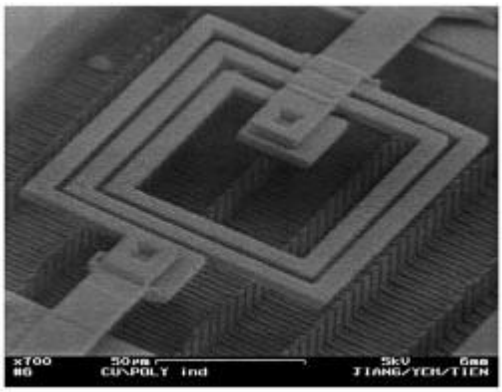


Figure 4-2. SEM image of a suspended inductor [50].

A different method for a suspended inductor is exemplified in [52]. In this work, the inductors are suspended with T-shape pillars with a height of 60 μm. MEMS technology is used to fabricate the inductors. The maximum quality-factor is measured to be 37 for a 4.2 nH inductance. The fabricated sample can be observed from Figure 4-3.

Another suspended inductor version is described in [53]; with a different integration technique named as glass micro bump bonding.

The suspended inductor method can be applied to different technologies, such as LTCC [54], [55]; the air-gap underneath the inductor is formed with use of several LTCC layers (actually LTCC technology allows multilayer combinations, so that, vias, packaging and etc. are easy to produce).

In [56], the inductors are suspended 100 μm above the substrate. CMOS micromachining is used. Proposed process helps to remove the sidewall oxides, and

hence the inter-turn capacitances are decreased. Moreover, etching the silicon underneath the inductor helps to decrease the shunt parasitic capacitances. As a fact, the quality-factor and SRF are improved.

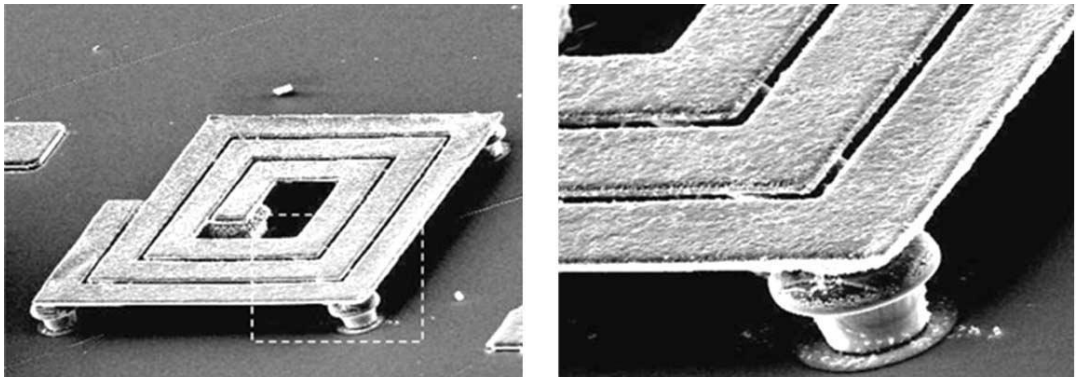
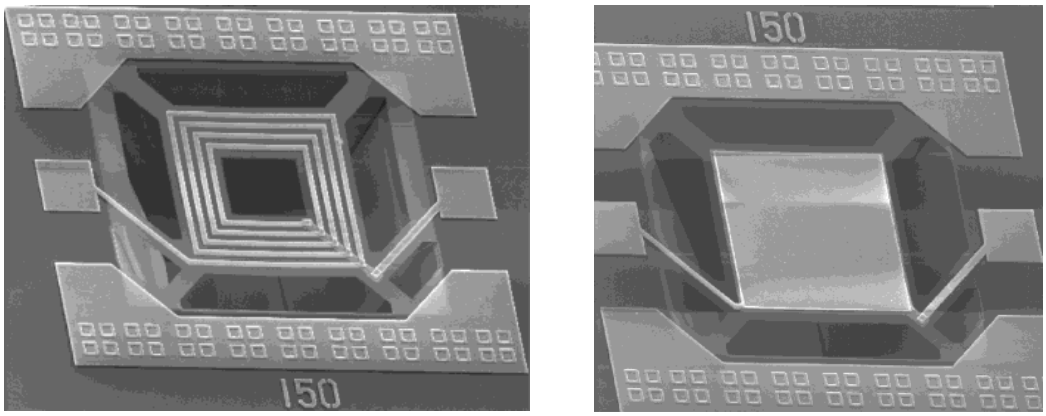


Figure 4-3. SEM image of a suspended inductor with T-shape pillar (zoomed in version on the right) [52].

To decrease the substrate losses and parasitic capacitances to the ground, not only the inductors but also the capacitors or the transmission lines can be suspended [57]. The examples of suspended inductor and capacitors from [57] are given in Figure 4-4. Large spiral inductors such as 100 nH can also be suspended. This is proved by Chang *et.al.*; the inductor is implemented in a CMOS RF amplifier [58].



(a) (b)

Figure 4-4. Photographs of (a) suspended inductor, and (b) capacitor [57].

In [59], it is shown that inductors are suspended on a thin dielectric membrane. Inductors with inductances 1.2 nH, and 1.7 nH had SRFs of 22 GHz and 17 GHz respectively. With the proposed method the SRFs are improved to 70 GHz, and 50 GHz, respectively. The membrane is formed with SiO_2, Si_3N_4, and again SiO_2.

The compatibility of the etching processes with the standard process flow is also an important fact. Nowadays, SiGe BiCMOS processes are extensively used. Thus, adaptation of the suspended inductors is also investigated in SiGe BiCMOS area. Back side etched high-Q inductors and etc. are investigated in [60], [61]. Quality-factor of in the order of 30 is achieved with this etching process in SiGe BiCMOS.

A different approach to increase the quality-factor of the inductors is the self-assembly [62], [63]. In [62], the metallization Cu is fabricated with solder pads. When the wafer is heated, the solder pads on metallization melts and the tension force on the Cu base metal rotates the structure as shown in Figure 4-5.

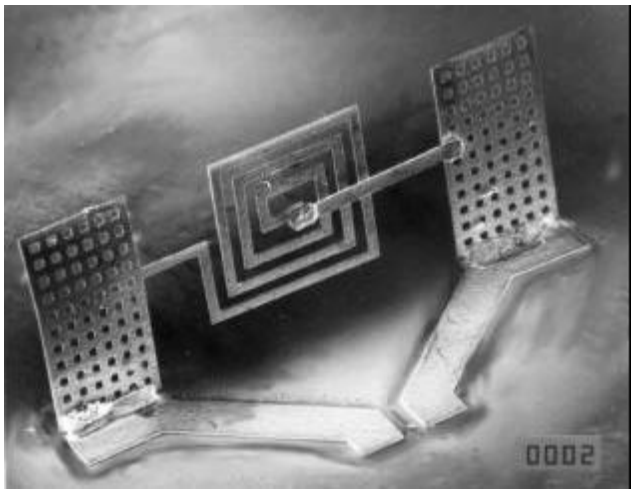
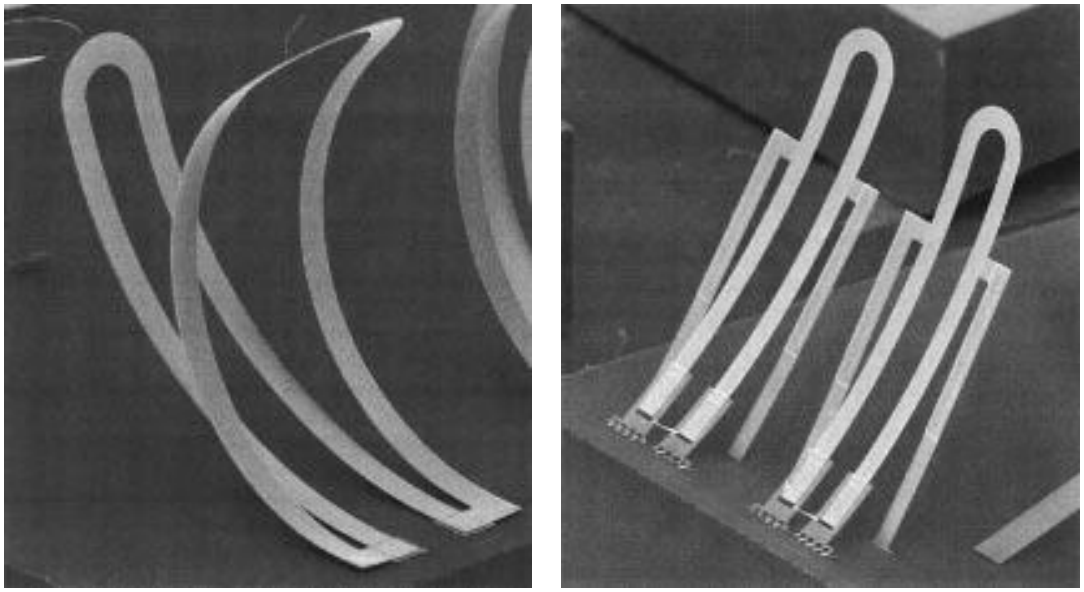


Figure 4-5. SEM image of a self-assembled inductor [62].

On the other hand, in [63], the inductors are designed and fabricated such that after releasing procedure the inductors self-assembled away from the substrate. Variable and fixed inductors are achieved. The examples are given in Figure 4-6. In [64], sacrificial layer differs from others, i.e., nickel is used as sacrificial layer to increase the height of the inductor from substrate. 30 μm air gap is reached, and the metal is thick 10 μm copper.

Other than planar spiral inductors, coil [65], and solenoid [66]-[69], inductors can also be fabricated with 3-D surface micromachining technology. Moreover, an application of a solenoid inductor can be examined in [70].



(a) (b)

Figure 4-6. Photographs of (a) self-assembled variable inductor, and (b) self-assembled fixed inductor [63].

4.2.3 Design Procedure for Square Planar Spiral Inductors

In-house MEMS process is used for implementation of the phase shifters, and hence for the square planar spiral inductors. Since there are no moving parts, the process is named as surface micromachining. In the design of these components, a thick electroplating is assumed to decrease the metal losses, as a result, the quality-factor of the inductors are increased (and at the same time SRF of the inductors). In the previous chapter, the phase shifters are designed with ideal lumped elements. However, in reality, the lumped elements are not ideal and they have parasitics related to the substrate losses, shunt capacitances to ground, metal losses, eddy current losses, and etc. These parasitics affect the performance of the phase shifters.

The designed inductors are modeled with an equivalent lumped circuit, to fully understand the behavior along the frequency band of interest, with the knowledge of the aforementioned parasitic effects and the achieved inductance values. This type of study is crucial to achieve a satisfactory performance of practical design of phase shifters.

For these reasons, the design of surface micromachined square planar spiral inductors is the most important step achieving the final phase shifter design.

Lumped inductor design has, also, its importance for the other applications. To predict the inductance of the specific inductor geometry before its manufacturing is a critical knowledge. The inductance formulas for circular and square coils are presented by Wheeler [71]. Planar spiral inductors have gained importance with the advancements in fabrication technologies such as GaAs MMIC, CMOS, and etc. Mutual inductance approach and several formulas are presented by Greenhouse for microelectronic inductors [72]. However, these formulations are not always valid for all type of the inductors. Moreover, when the formulas are given for the specific type of inductor the error is around 10% for the measured and predicted values. A most common way is the optimization of the inductors with some iterative analysis of with electromagnetic simulations. In [73], electromagnetic analysis for planar inductors (square or polygon) and transformers is done, and equivalent models are extracted. Moreover, a custom design tool done by the authors is described for these structures named as ASITIC [75].

A starting point to design planar spiral inductors is needed. In [74]; there are three approximating formulas about planar spiral inductances for four types of topologies namely square, circular, octagonal and hexagonal. From those four topologies the square planar spiral inductor (SPSI) topology has been picked up because of ease on computations, manufacturing and etc. One can see the square topology in the following Figure 4-7.

From the approximated formulas, the design started with modified Wheeler formula with the equation;

$$L_{mv} = K_1 \mu_0 \frac{n^2 d_{avg}}{1 + K_2 \rho} \quad (4.8)$$

where $d_{avg} = \frac{d_{out}+d_{in}}{2}$ and $\rho = \frac{d_{out}-d_{in}}{d_{out}+d_{in}}$. n is the turn number. $K_1 and\ K_2$ are the layout dependent parameters and they are 2.34, 2.75 respectively for square planar spiral inductor.

First of all, an example was chosen as 1.44 nH inductance, which belongs to 2 to 4 GHz phase shifter 90° phase shift bit (please refer to the last sub-section of the previous chapter). Before starting the design some parameters have been fixed, such as the turn number, the width of the trace of the inductor and the gap between the two inductor turn base metals. The turn number is fixed on 1.75. It is decided on that turn number value from previous works done by the group [78]-[79], since it is enough for 1.44 nH inductance values. In the beginning the trace width is fixed on 50 µm, and the gap between two base metals is fixed on 15 µm since it is enough to encounter the process variations on etching the gold. The gap and trace width variations are also investigated and presented later in this chapter.

First of all, a parametric model has been drawn in HFSS [76], for 1.75 turn square planar spiral inductor. It can be observed in Figure 4-8. Note that there is no air bridge and second metallization, so in order to connect the open ends of the inductor a torus used as wire bonding with a diameter of 25 µm. Wire bonding is assumed for the fabrication, because of the following reasons;

- To decrease the masks needed for the fabrication, to decrease the complexity of the fabrication, and to decrease the cost of the fabrication.
- To decrease the possible series parasitic resistance caused from under-, or air-bridges on the inductor. Hence the quality-factor of the inductors is increased and SRFs are increased.

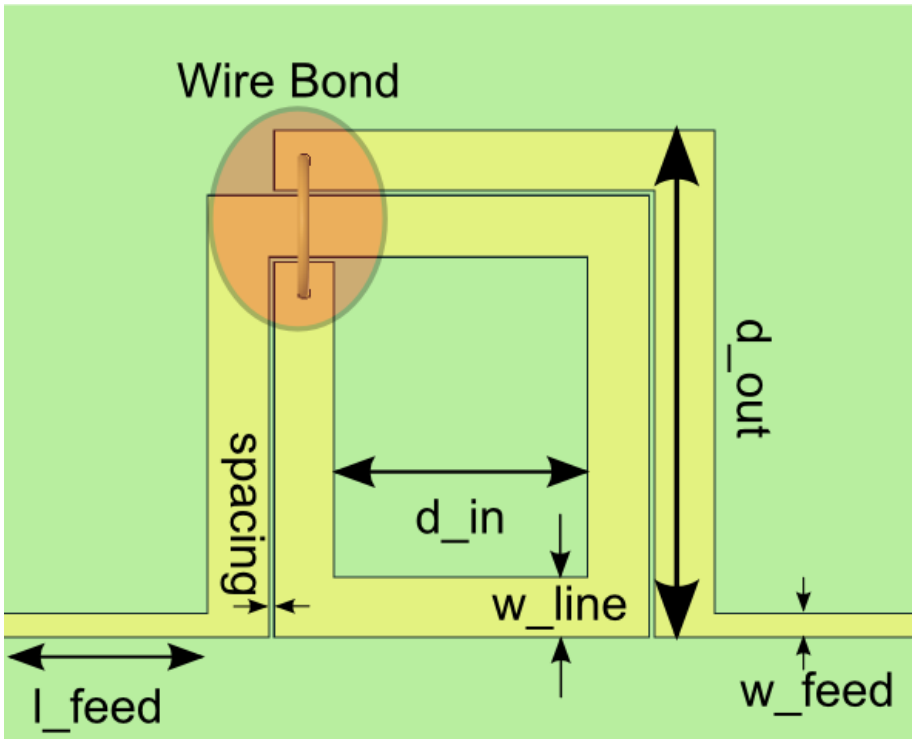


Figure 4-7. Illustration of square planar spiral inductor with geometrical parameters, and wire bond.

From the modified Wheeler formula with the fixed turn number, trace width, and gap; initially found d_{out} value was 434 µm. Simulation was done in HFSS. Note that the feed lines are a bit long, 400 µm. It is done in order to escape from the evanescent modes excited on microstrip line. After the simulations is done with the help of "de-embed" function of HFSS, the feed line reduced to 100 µm. All of the EM simulated inductors have common feed line lengths and widths as 100 µm, and 50 µm, respectively.

The substrate for this design procedure is assumed as alumina with $\varepsilon_r = 9.6$, and with dielectric loss equal to 0.001. The thickness of the substrate is 250 µm. For both ground plane and base metallization, gold is assumed with conductivity $\sigma = 3 \times 10^7$ S/m, and 1 µm thickness.

After the EM simulations are done, the matrix data of S-parameters has been exported as Touchstone file. This is done to extract lumped equivalent model parameters for the inductors. To decide on lumped equivalent circuit is a series

action. One must consider that the circuit shall not be too complex, for understanding and considerations on design time. On the other hand, the equivalent circuit should match the EM simulation data with a minimized error between the EM simulated S-parameters and extracted model S-parameters.

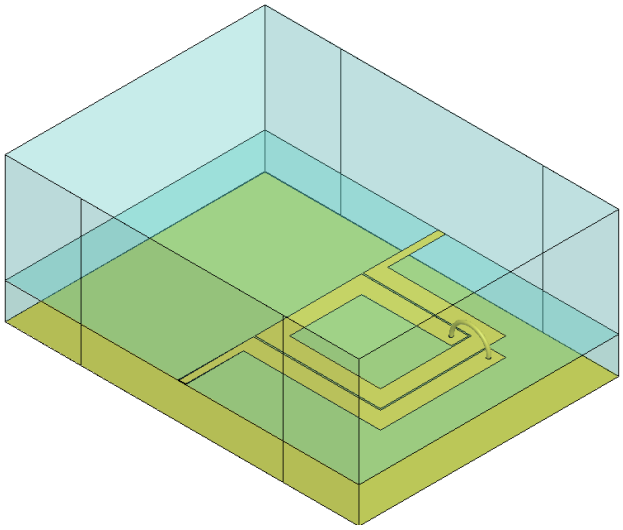


Figure 4-8. 1.75 turn square planar spiral inductor drawn parametrically in 3D EM simulator HFSS [76] (the substrate is chosen as alumina, and the metal is chosen as gold with a thickness 1 µm).

There are several equivalent models presented in the literature. In general, the equivalent circuit models are presented for silicon substrates [80]-[83]. A general equivalent circuit for planar spiral inductors on silicon is illustrated in Figure 4-9. L_s represents the total inductance of planar spiral inductors. R_s is the loss due to metals, or in some cases the radiation loss is included in here. C_s represents the inter-turn capacitance. C_{ox} is the capacitance due to the oxide layer underneath the inductor, and above the silicon substrate. C_{si} is the capacitance to the ground caused by the dielectric property of the silicon substrate. Finally, R_{si} is the substrate loss due to the low resistivity of the silicon. Since the used substrates for our cases are either alumina or quartz, one does not need;

- Oxide capacitance, since there is no oxide used underneath the inductors for alumina or quartz substrates.

- Substrate loss, since alumina or quartz are very low-loss substrates compared to silicon.

One can model the planar spiral inductors for low-frequency applications, such as 1 to 6 GHz, with L_s which is total inductance of the structure, R_s which is the losses due to metallization and/or radiation, C_p which is the inter-turn capacitance, and finally with C_{sh} which is the shunt capacitance to ground due to the substrate permittivity. According to this knowledge, the final lumped equivalent model used for this study is constructed as in Figure 4-10.

Using this circuit, optimization is done in ADS [77] to match the EM simulated S-parameters and lumped equivalent model S-parameters. EM simulation and lumped equivalent model S-parameters are given in Figure 4-11. Note that optimization is done within the band 1 to 6 GHz, since it is the band of interest. Red lines represent the EM simulation, and blue lines represent the lumped equivalent model results. The model matches well with the EM simulation, which means that the used circuit accurately models the square planar spiral inductors.

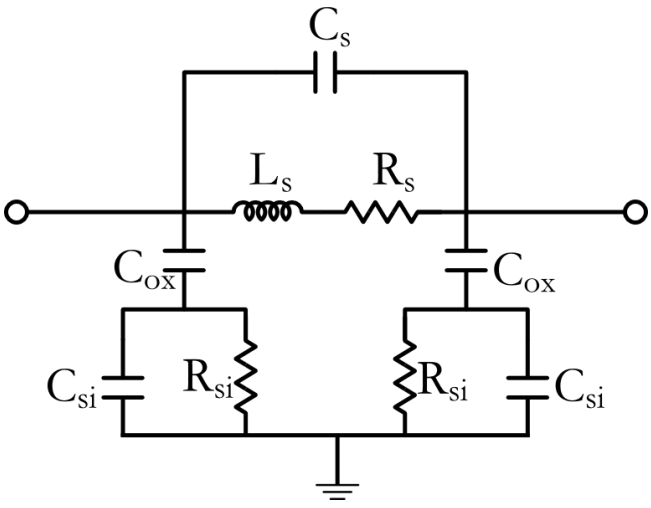


Figure 4-9. Lumped equivalent circuit for planar spiral inductors on silicon.

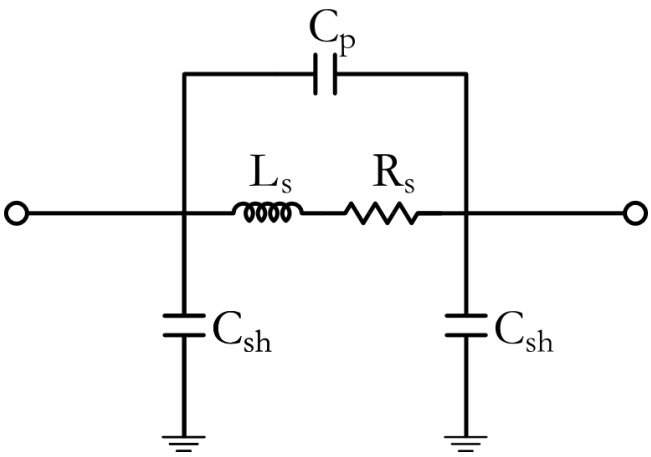


Figure 4-10. Lumped equivalent circuit for planar spiral inductors on alumina or quartz.

The extracted model parameters are; L_s=1.768 nH, C_p=9.22x10^{-6} pF, R_s=0.875 Ω, and C_{sh}=67.9 fF. It is obvious that the result does not match the desired inductance value, which is 1.44 nH. So that a modification on modified wheeler formulation is done, such that;

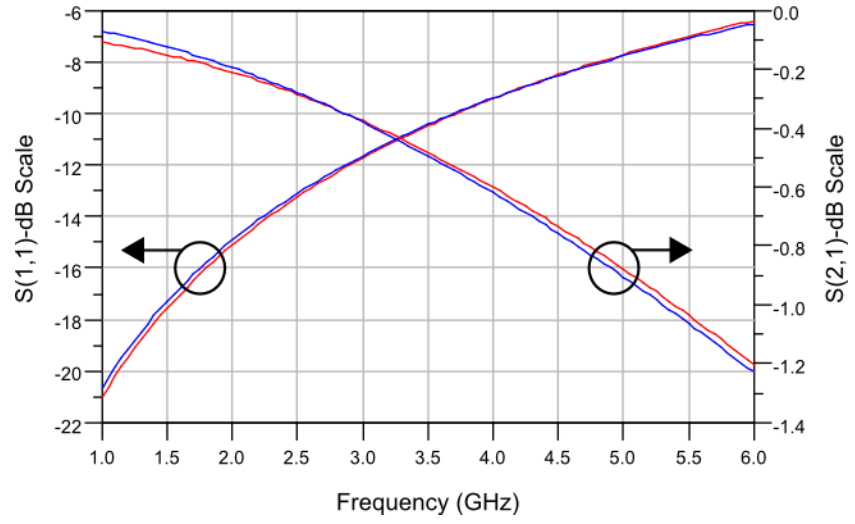
$$L_{mv} = K_1 \mu_0 \frac{n^2 d_{avg}}{1 + K_2 \rho} + K_3$$

From the results the included new parameter K_3 is found to be 0.32496x10^{-9}. Then a new iteration has done on the new modified wheeler formulation. The resultant outer diameter is found to be 385 µm. The same procedure is done as described above. The resultant lumped equivalent model parameters are; L_s=1.436 nH, C_p=2.3x10^{-12} pF, R_s=0.825 Ω, and C_{sh}=58 fF. The model and EM simulations seem to be fitted well enough and the desired inductance value has been reached very closely.

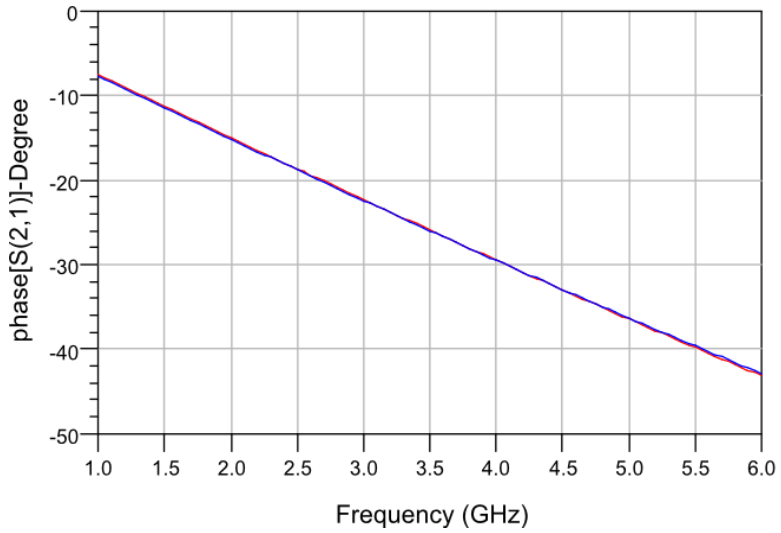
With the new obtained modified Wheeler formulation as mentioned above, an outer diameter value has been obtained for 1.98 nH planar spiral inductor, which is 465 µm. Replacing the new outer diameter value in HFSS to obtain EM simulation results has been done. After that the optimization is done in ADS and the resultant comparison graphs are given in Figure 4-12. The resultant lumped equivalent model parameters are; L_s=1.981 nH, C_p=8.9x10^{-13} pF, R_s=0.909 Ω, and C_{sh}=74 fF. The desired inductance value is achieved in the first trial after the design of previous inductor.

However, this could not be the case always. When the modified Wheeler formulation with the additional constant does not give the desired inductance value iteration on outer diameter value could achieve this, or a new iteration on K_3 with a basic calculation on modified Wheeler formulation.

On the other hand, the 1.75 turn planar spiral inductor could not achieve the desired inductance values when they are large, within an appropriate size, and without a self-resonant-frequency within the desired band. To achieve the desired inductance values for those inductors 2.75 turn, 3.75 turn, or even 4.75 turn planar spiral inductor could be used. The same design procedure was applied on 2.75 turn PSIs as for the above described inductors. An example geometrical illustration is given in Figure 4-13. Any further investigation is not needed here, since the 2.75 turn PSIs are desired to be avoided in terms of series parasitic resistance values. For the same inductance value the 1.75 turn PSI can achieve less series parasitic resistance. On the contrary, for some inductance values such as in the 1 to 2 GHz phase shifter (for the inductance values one can refer to previous chapter or the further chapter about the design of 1 to 2 GHz phase shifter in this report) 2.75 turn PSIs are needed.



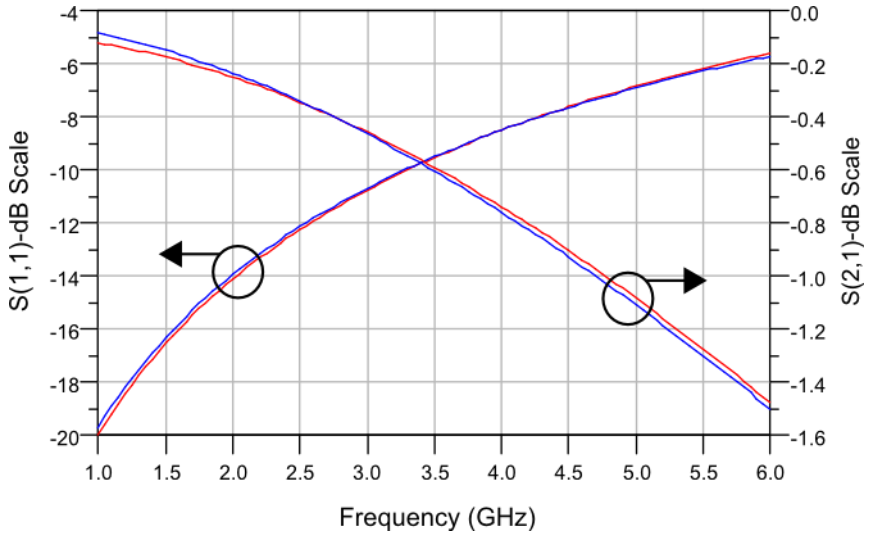
(a)



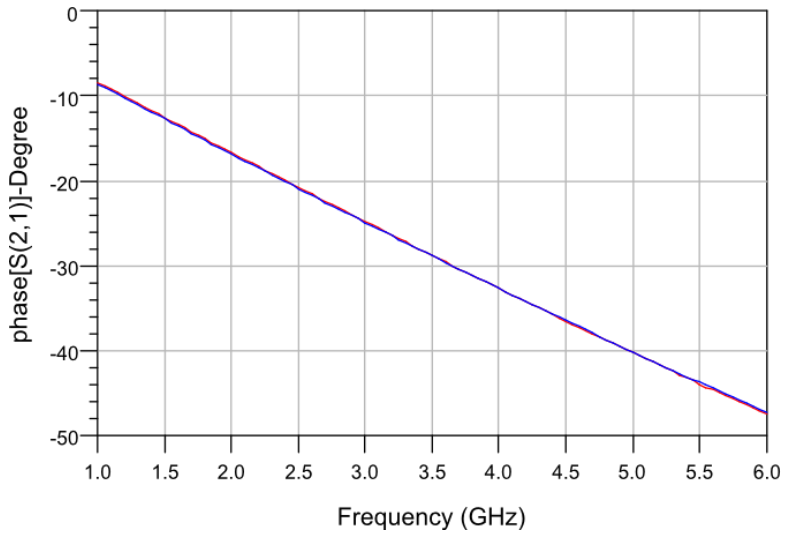
(b)

Figure 4-11. S-parameters comparison between the EM simulation (red lines) and lumped equivalent model (blue lines) for 1.44 nH inductance with outer diameter of 434 µm, (a) Return loss (y-left axis) and insertion loss (y-right axis), (b) Transmission phase

The effect of trace width and spacing values should be investigated for each inductors, since for each variation parasitics are different, and hence, the quality-factors of the inductors. Moreover, this will help to choose the appropriate variation for a specific inductor, for low-loss, and flat phase response phase shifters. In the next sub-section the trace width variation and spacing variation are investigated.



(a)



(b)

Figure 4-12. S-parameters comparison between the EM simulation (red lines) and lumped equivalent model (blue lines) for 1.98 nH inductance with outer diameter of 465 µm, (a) Return loss (y-left axis) and insertion loss (y-right axis), (b) Transmission phase.

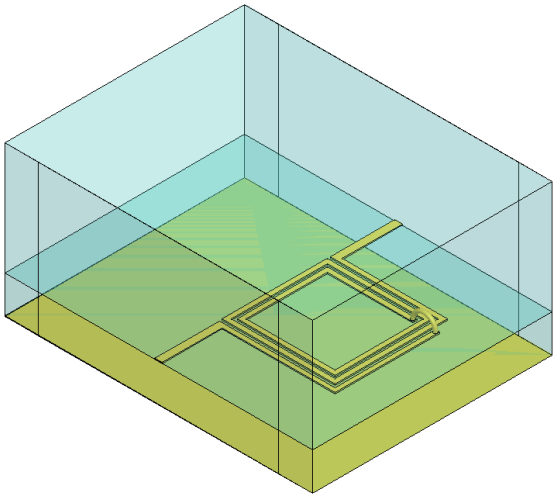


Figure 4-13. 2.75 turn square planar spiral inductor drawn parametrically in 3D EM simulator HFSS [76] (the substrate is chosen as alumina, and the metal is chosen as gold with a thickness 7 µm).

4.2.4 The Effect of Trace Width and Spacing Variations

In this work, various trace width values together with various spacing for 1.75 turn planar spiral inductor of 1.44 nH inductance values EM simulation and optimization for model fitting is done. The trace width values used are 40 µm, 50 µm, 60 µm, 80 µm, 100 µm, and 120 µm together with spacing values of 10 µm, 15 µm, and 20 µm. It is better to remember that the initial designs are established on 50 µm trace width with spacing of 15 µm, so that in this part of this document trace width of 50 µm together with spacing of 10 µm and 20 µm are given. The other trace width values will be given with spacing values of 10 µm, 15 µm, and 20 µm.

In Table 4-1, the parasitics values obtained for 1.44 nH planar spiral inductors for various width and spacing values after optimization are given. Corresponding comments will be given afterwards. The parallel connected parasitic capacitor values are not given in the table, since the values are very low. Addition to that, the S-parameters comparison graphs are not given, they were all well fitted.

As it can be observed from Table 4-1, obviously, the less the trace width values the higher the loss. Also, the optimum spacing value seems to be 15 µm for this inductance value. However, it may change for others. The other spacing values may

be due to eddy current losses and respectively increased line length conductor losses. For the desired inductance values it is possible to pick having less loss and nearly equal to the desired inductance values for a different trace width and spacing. It is better to note that the feed lines are not changed during this procedure they were fixed at 50 µm.

Among those variations the most appropriate one should be picked for a desired inductance value. The effect of the metallization thickness is another critical parameter that affects the metallization loss, and it can be more understood in the next sub-section, in which the process variations are concerned.

For a stable design, one should, also, consider the process variations. For example what will happen when the thickness of the metallization is not 1 µm but 0.9 or 0.8 µm, or the spacing variations; for example, the spacing is decided on 15 µm but after the process it could come out to be 17 µm or 13 µm, and etc. In the next sub-section, the possible process variations cases are examined and presented.

Table 4-1. The whole 1.44 nH inductance designs with trace width, spacing, outer diameter, found inductance, and found parasitics values.

W_{line} (µm)	Spacing (µm)	D_{out} (µm)	L_s (nH)	R_s (ohm)	C_{sh} (fF)
40	10	338	1.432	0.877	49
40	15	347	1.437	0.917	51
40	20	357	1.452	0.903	53
50	10	375	1.429	0.823	57
50	20	393	1.444	0.833	60
60	10	412	1.438	0.803	64
60	15	420	1.44	0.775	66
60	20	429	1.45	0.794	68
80	10	480	1.441	0.777	80
80	15	489	1.443	0.765	82
80	20	497	1.454	0.727	84
100	10	546	1.44	0.764	97
100	15	555	1.458	0.711	99
100	20	563	1.473	0.727	101
120	10	610	1.448	0.747	115
120	15	618	1.466	0.697	117
120	20	626	1.475	0.723	119

4.2.5 Process Variations Considerations

Process variation case is investigated for the designed planar spiral inductor of 1.44 nH inductance. The EM simulated inductors assumed to have line width of 50 µm and spacing of 15 µm. The process variation case gives a chance about the investigation of the conduction losses by solving inside the metallization of the inductors in HFSS, which shows us that, the real loss of the inductors. Remember that the thickness is selected as 1 µm. The thickness assumed to be changed by an amount of ±20% due to the process which is not the edge values, but it is simulated in order to give an idea

about the changes in the inductor due to metal thickness. The etching of the metallization case is assumed to be in two cases as 1 µm less etched as it leads us to 13 µm spacing value and 52 µm line width value, and the other case is the metallization is etched 1 µm more than the desired value which leads us to 48 µm line width and 17 µm spacing values. All possible variations for those values are considered.

The outer diameter is fixed for the 1.44 nH inductor, i.e., 384 µm. The thickness of the metallization layer is considered in three cases as 0.8 µm, 1.0 µm, and 1.2 µm. The spacing values are 13 µm, 15 µm, which is the desired spacing value, and 17 µm for over-etched case. For those spacing values the trace widths are considered as 52 µm, 50 µm, and 48 µm. The lumped equivalent model parameters are extracted for all these 9 cases, and they are presented in Table 4-2 together with the geometrical variation data.

Table 4-2. The whole process variation case for 1.44 nH inductance with trace width, spacing, thickness, found inductance, and found parasitics values.

W_{line} (µm)	Spacing (µm)	Thickness (µm)	L_s (nH)	R_s (ohm)	C_{sh} (fF)
48	17	0.8	1.449	2.576	58
48	17	1	1.446	2.22	58
48	17	1.2	1.449	1.932	58
50	15	0.8	1.428	2.416	58
50	15	1	1.42	2.124	58
50	15	1.2	1.422	1.868	58
52	13	0.8	1.395	2.35	58
52	13	1	1.393	2.122	59
52	13	1.2	1.418	1.696	57

From Table 4-2, it is seen that the 1.44 nH, 1.75 turn planar spiral inductor is not affected so much from the line width variations and spacing variations in the sense of shunt parasitic capacitance and series parasitic capacitance. However, the inductance value differs very little, which does not affect the responses much.

On the other hand, the series parasitic resistance differs much. In order to understand the changes one should refer to the skin depth issue which has a major role in the conductor loss mechanisms [88]. Skin and proximity effects have a huge impact on microwave circuits, and modeling them is another issue [86], [87], which is not examined in the scope of this thesis. At 1 GHz, the skin depth for gold is around 2.5 µm. For that reason even a slight change of thickness lower than skin depth significantly changes the series resistance values. It is better to note here that the thickness should be increased in order to get rid of the high values of series resistance, and hence the losses in the SPSIs.

The optimum metallization thickness should be around 2 times the skin depth value as stated in the literature which leads us around 5 µm gold thickness. On the other hand, it is stated from the previous researches that the metallization thickness should be around 7 µm of gold or if copper is used the thickness should be around 5 µm for low frequency level inductor designs [39]. As it can be observed, even when the thickness increases to 1.2 µm, the series resistance value changes significantly.

The inductance values are decreased from the over-etching case comparing with the under-etching case. However, the inductance variations are not that high compared to the series resistance variations.

From these process variation simulations, one can conclude that the shunt parasitic capacitance is not affected, even they did affected the fluctuations on those values are very small in the order of 1 fF, and have not considerable effects on the performance of the inductors.

The inductance values seem to have changed a little; which are believed to have negligible effects on the performance, since the changes are low enough (around 3%)

The main issue here is the metallization thickness, since the series parasitic resistance values are a bit high, which yields more losses on the planar spiral inductors, and decreasing the quality factor of the inductors.

The next design consideration focuses on increasing the metallization thickness. Related literature points out that the thickness for low frequency values should be around 2 times the skin depth of the used metallization material. However, it is also mentioned that this would not be enough. In order to decrease the losses and increase the quality factor of the inductors one should increase the thickness at least 5 μm for copper and 7 μm for gold [39]. It is decided to check the metallization thickness varying from 2 μm to 7 μm. It is possible to observe the influence of the thickness on model parameters with the changing metal thickness.

4.2.6 Obtaining the Proper Thickness Value for Low Series Parasitic Resistance

As it was discussed in the part above, the metallization thickness should be increased in order to decrease the series parasitic resistance of the planar spiral inductor and to increase the quality factor of the planar spiral inductor over the desired band of 1 to 6 GHz. For that reason, the thickness is increased to 2, 3, 4, 5, 6, and 7 μm with line width of 50 μm and spacing of 15 μm, for 1.44 nH inductor with outer diameter of 384 μm. The lumped equivalent model parameter results for these 6 cases are given in Table 4-3.

Table 4-3. The whole thickness variation case for 1.44 nH inductance with trace width of 50 μm, spacing of 15 μm, outer diameter of 384 μm, found inductance, and found parasitics values.

Thickness (μm)	L_s (nH)	R_s (ohm)	C_{sh} (fF)
2	1.405	1.442	58
3	1.399	1.203	58
4	1.387	1.138	58
5	1.374	1.041	58
6	1.37	0.919	58
7	1.352	0.974	58

The shunt capacitance values seem to be not affected from the thickness variations, as it is expected. The most important changes are observed in the series parasitic resistance value as the thickness increases, the parasitic resistance decreases with increasing thickness which is a good result, so it confirms the idea of decreasing the loss in the inductor by increasing the thickness. On the other hand, the obtained inductance values seem to decrease with increasing thickness, but not that much. This section is done to see the effects of thickness on planar spiral inductors. So, more accurate designs are done for further steps.

4.2.7 Q-Factors for Different Width and Spacing Values

Please remember the procedure about the different trace width values and spacing. For these inductors for different values of trace width and spacing there are the outer diameters calculated and the model fittings are done for all of them. The Q-factors for those simulations are extracted, assuming that port 2 of the inductors are short circuited to ground. Moreover, the related Q-factor formula is given in page-80.

The corresponding Q-factors are given in Figure 4-14. Note that the very best three Q-factors are obtained from the width and spacing values of 120 µm – 15 µm, 80 µm – 20 µm, and 120 µm – 20 µm respectively. It will be pointed out in the next chapter, but it is, also, appropriate to note that the inductors are chosen for the phase shifters with peak quality-factor values and less quality-factor ripples in the band.

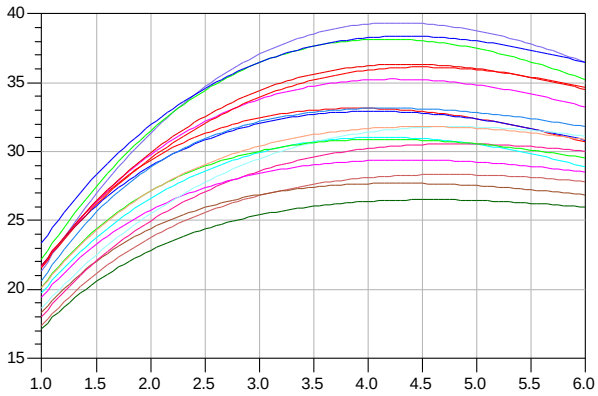


Figure 4-14. Q-factor calculations on 1.75 turn 1.44 nH planar spiral inductors for all of the trace width and spacing values.

4.2.8 Fabrication and Measurement of Square Planar Spiral Inductors

As it is already mentioned in the previous parts of this section, in the implementation phase of the phase shifter, the critical elements are the planar spiral inductors. Confinement of the magnetic field in a small area without increasing the dissipative insertion loss and without decreasing the series resonance frequency (SRF) is a serious task. There are numerous studies in the literature regarding to different production technologies such as RF CMOS, RF MEMS and MMIC. Most of these studies concentrate on improving the quality factor of the inductor without complicating the production process.

Modeling the inductor performance is another critical issue. An accurate model is necessary to be able to use in the design process. The ideal inductors which are used in the designs based on analytical derivations are not practically achievable; each parasitic effect changes the inductor performance and consequently changes the circuit, i.e. phase shifter, performance.

Electromagnetic (EM) simulations are, in most cases, reliable in predicting the inductor performance. The simulation results are then used for obtaining the circuit model. However, without getting the confirmation of the results by measurements, the design circle is not completed.

Before going thru the final production phase of the phase shifters, confirmation of the component performances by measurements is the last step. In this part, this step of the phase shifter implementation is explained in detail.

Following these arguments, inductor design by using EM simulation tools is recalled first for on quartz wafer designs. Comparisons with circuit simulations give clues about the simulation settings for getting a better accuracy.

After that, production and post-production processes of the sample inductors are given in detail. In brief, inductors with different line width and gaps and also inductors with different turns are included to the characterization process. In order to decrease the losses, increasing the thickness of the inductor turns by electroplating is also

considered. Comparison of the measurement results with the design predictions is also given.

The differences in the comparisons are also examined. The final conclusion is the verification of the design and the production processes.

Before the production of final prototype of the phase shifters, it is desired to validate the designs of the lumped elements with production and measurement phases. For that reason, a group of square planar spiral inductors are designed with quartz substrate with different turn numbers, trace widths, spacing, and outer diameters. The geometrical specifications of the designed square planar spiral inductors are given in Table 4-4, together with their names in the processes. The view of the mask could be observed in Figure 4-15. It is better to note that the inductors are varied in two as base metal and with electroplating. The electroplated version names are finished with "E", for instance inductor "1A" with electroplating named as "1AE". There are two masks for this mask set; one is the "Metal-1", which is related to the etching process of the base metal layer, and "Electroplating", which is the needed mask for the electroplating process.

The process is simple since there are two masks for the overall process. As a first step, 20 nm Ti is sputtered and then 1 um thick Au is sputtered on the substrates. Then electroplating mask is used to do the lithography in order to thicken the gold with electroplating process. After that the electroplating is done, and the wafers are ready for the last step, which is the etching process of the base metal layer. A final lithography is done for etching process, and then the etching is done.

Note that the measured conductivity of the sputtered base metal-gold is $4x10^7$ S/m. On the other hand, the relevant conductivities of electroplated gold are measured to be non-uniform ranging from 1.5 to 3.3 x 10^7 S/m. This conductivity variation studies are done on all phase shifters, and it is seen that there is no significant effect on the overall phase shifter performances; however it affects the insertion loss of the phase shifters.

For the inductors, to be measured, some post-production steps are needed. The reason behind this is the inductors are designed for microstrip and the measurement setup is for CPW measurements. For all of the inductors that are produced have a CPW to microstrip transition on port 1 and microstrip to CPW transition on port 2, which are same for all inductors, an example could be observed in Figure 4-16. There are two post-production steps after the dicing of the samples; those can be ordered as the bonding the inductor samples to a gold sputtered holder substrate with either silver-epoxy or Ultrasonic bonding machine, after the bonding procedure is done the wire bonding processes are done. The wire bonding is done via automated ball-bonder. Making reference to the previous parts of this chapter, remember that in the inductors, no air bridge or under-pass is used to get rid of the extra parasitics induced by those air-bridge or under-pass structures. Instead wire bonds are used to connect the internal arms of the inductors. Wire bonds are, also, used to connect the ground of CPW to the bonded holder substrate which is also connected to the ground of the microstrip inductors. Total of 9 (nine) wire bonds are done; one is for the internal connection of the inductors and the other 8 (eight) are for the ground connections of the CPW and microstrip structures. An example of an ultrasonically-bonded inductor could be observed in Figure 4-17. Because of the ultrasonic vibration, some part of the metal layers scratched a little; however, no considerable effect is observable, all of the bonded inductors are successfully measured.

Table 4-4. Designed square planar spiral inductors with their geometrical specifications.

Inductor Name	W_{line} (um)	Spacing (um)	D_{out} (um)	Turn Number
1A	60	10	458	1.75
1B	80	15	538	1.75
1C	100	10	602	1.75
1D	120	10	668	1.75
1E	50	20	456	1.75
1F	100	20	644	1.75
1G	120	20	716	1.75
1H	50	10	728	1.75
1J	60	20	820	1.75
1K	120	10	654	1.75
1L	120	15	664	1.75
1M	120	20	670	1.75
1N	60	15	780	1.75
1O	40	15	750	1.75
1P	60	20	531	1.75
1R	100	15	811	1.75
1S	40	20	599	2.75
1T	30	20	676	3.75
1U	30	15	600	4.75
1V	30	20	634	4.75

In order to get rid of the effects of additional fixture parts (CPW to microstrip transition on port 1 and microstrip to CPW transition on port 2) during measurements, multi-line TRL calibration kit is prepared on the same mask set. However, this TRL calibration method did not work properly, and the results were not even close being a passive component considering the inductors.

For that reason, the fixture parts are tried to be de-embedded via ADS, by introducing the CPW line and microstrip line; and also EM simulations of those parts are used for de-embedding. The SOLT calibration is used, for the measurement of the inductors. The measured inductors are listed as in Table 4-5. The measured inductor's magnitude of S_{11} in dB scale, magnitude of S_{21} in dB scale, and the phase of S_{21} in angle scale are given in Figure 4-18, Figure 4-19, and in Figure 4-20, respectively.

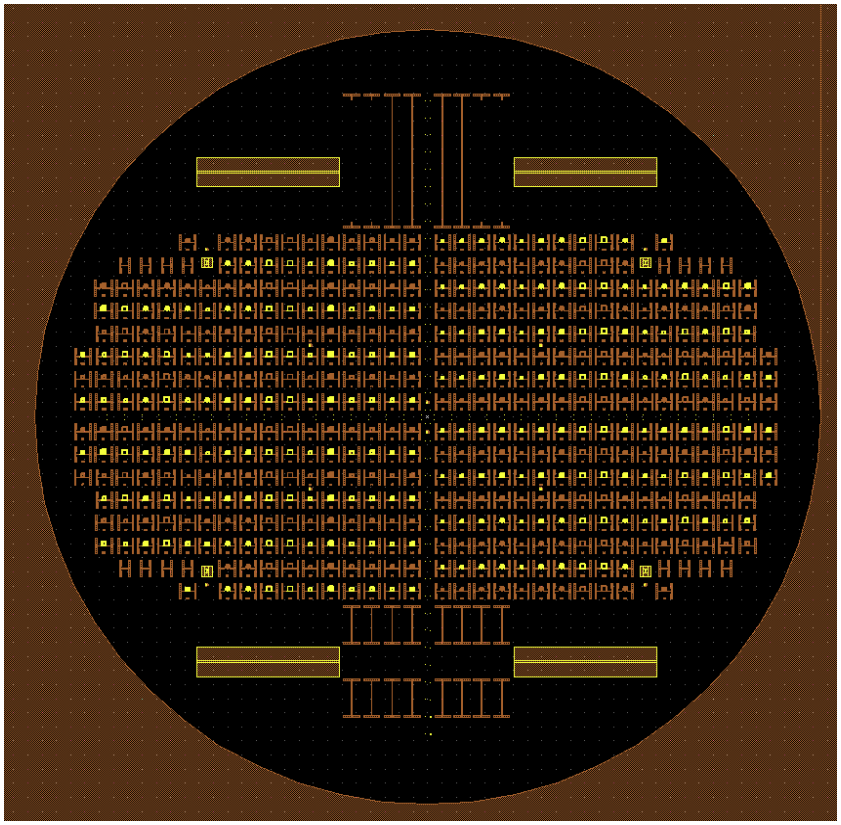


Figure 4-15. The mask layout of square planar spiral inductors.

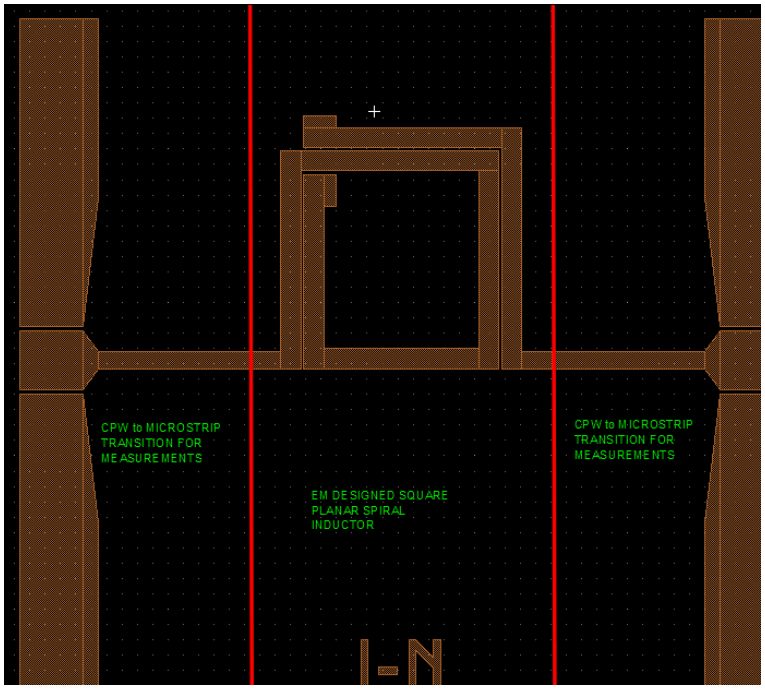
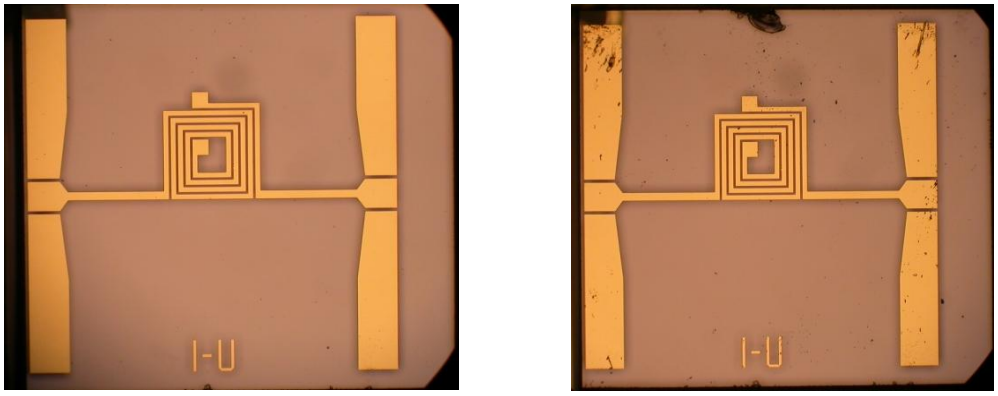


Figure 4-16. An example of the designed square planar spiral inductor, in which fixtures for measurements could be observed.



(a) (b)

Figure 4-17. An example of an ultrasonically-bonded inductor, 1U (a) Before bonding (b) After bonding.

Table 4-5. Geometrical and electroplating specifications of the Measured Inductors.

Inductor Name	W_{line} (um)	Spacing (um)	D_{out} (um)	Turn Number	Electroplated
1G	120	20	716	1.75	No
1M	120	20	670	1.75	No
1O	40	15	750	1.75	No
1S	40	20	599	2.75	No
1SE	40	20	599	2.75	Yes
1U	30	15	600	4.75	No
1V	30	20	634	4.75	No

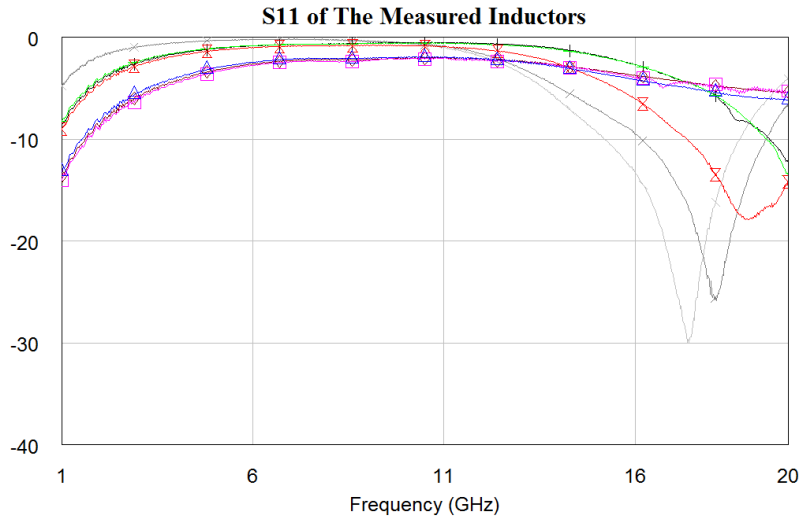


Figure 4-18. dB(S11) responses of the measured inductors with SOLT calibration and without de-embedding.

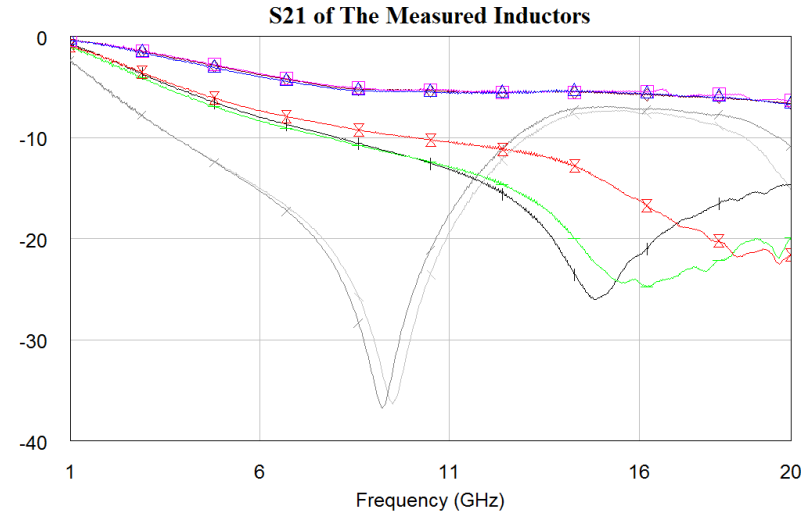


Figure 4-19. dB(S21) responses of the measured inductors with SOLT calibration and without de-embedding.

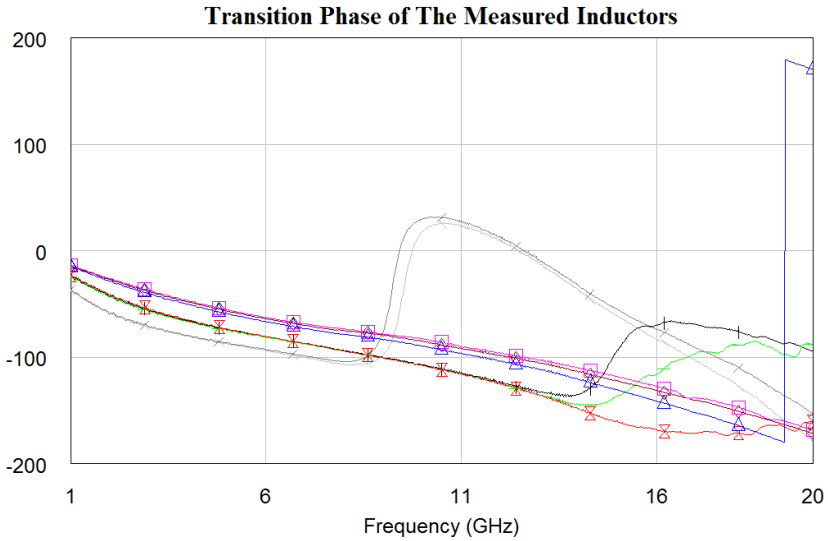


Figure 4-20. Phase angle(S21) responses of the measured inductors with SOLT calibration and without de-embedding.

In order to compare the measured data with the designed inductors, HFSS simulations of all measured inductors are done with quartz substrate and fabrication related data. The extracted lumped equivalent model parameters for those inductors are given in Table 4-6.

Table 4-6. Lumped equivalent model parameters for all measured inductors simulated in HFSS on quartz substrate and fabrication related data.

Inductor Name	L_s (nH)	R_s (ohm)	C_{sh} (fF)
1G	2.123	1.845	44
1M	1.867	1.601	40
1O	4.78	4.208	43
1S	5.409	4.803	37
1SE	5.326	4.096	37
1U	11.009	8.958	37
1V	11.084	8.917	40
1K	1.844	1.721	39

In order to extract the lumped equivalent model parameters for the measured inductors, one should get rid of the fixture effects on ports 1 and 2. Several de-embedding options are tried and, finally the microstrip equivalence of the fixtures are achieved proper de-embedding of the measured inductors, the same procedure is done via EM simulated microstrip lines and the best fitted microstrip line length is found to be 900 um with 50 um line width.

The extracted lumped equivalent model parameters of the measured inductors with additional microstrip lines are given in Table 4-7. The differences of the lumped equivalent model parameters are given in Table 4-8. Note that the designed inductor lumped equivalent model parameters are well matched. However, there is a significant difference for the electroplated inductor. In order to match the EM simulations and the measurements, a fully process related EM simulation is done in HFSS with 1 um thick gold with the sputtered gold conductivity of 4×10^7 S/m, and 6 um thick gold with the electroplated gold conductivity of 3×10^7 S/m for the inductor named as "1SE". The lumped equivalent model parameter results of the simulated inductor as follows: L (nH) = 5.122, R_s (ohm) = 1.98, and C_sh (fF) = 37, so that the differences are given in Table 4-8, with green background.

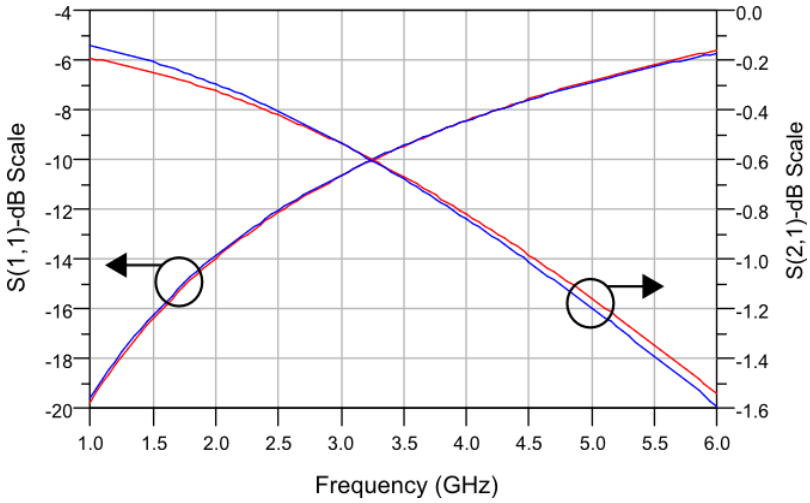
Table 4-7. Extracted Lumped equivalent model parameters for all measured inductors with additional microstrip lines with EM simulated in HFSS, 50 um line width and 900 um line length.

Inductor Name	L_s (nH)	R_s (ohm)	C_{sh} (fF)
1G	2.185	1.679	48
1M	1.957	1.693	43
1O	4.767	4.507	49
1S	5.418	5.132	41
1SE	5.022	2.127	41
1U	11.011	10.636	48
1V	11.146	10.12	52
1K	1.839	1.869	41

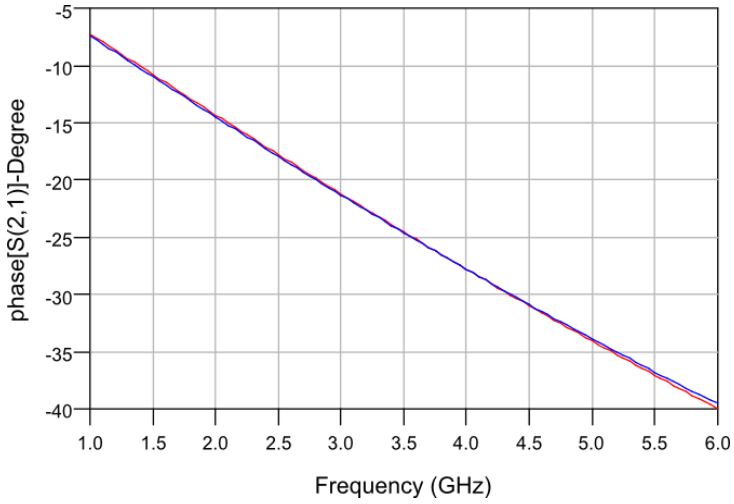
Table 4-8. Difference between the extracted Lumped equivalent model parameters for HFSS simulated and measurement results for all measured inductors with additional microstrip lines EM simulated in HFSS, 50 um line width and 900 um line length.

Inductor Name	ΔL_s (nH)	ΔR_s (ohm)	ΔC_{sh} (fF)
1G	0.062	0.166	4
1M	0.09	0.092	3
1O	0.013	0.299	6
1S	0.009	0.329	4
1SE	0.100	0.147	4
1U	0.002	1.697	11
1V	0.062	1.203	12
1K	0.005	0.148	2

In order to check the validity of the de-embedding with line length of 900 um of the microstrip line, a sample inductor "1K" is chosen with additional microstrip lines of 900 um simulated in HFSS. The comparison of the measured and simulated S-parameters is given in Figure 4-21. Note that there is a really good match between the two cases. So the de-embedding of the inductors can be trusted, and so the design of the inductors via HFSS is proven to be correct as compared to the measured data.



(a)



(b)

Figure 4-21. The S-parameters comparison graphs for the measured (red lines), and the simulated with additional 900 um length (blue lines) inductor named as "1K" (a) Return loss (y-left axis) and insertion loss (y-right axis), (b) Transmission phase.

4.2.9 Mitered SPSIs: A small change in the layout, a small improvement in Q-factor and SRF

Microstrip based transmission lines, passives, and etc. are the most exclusively used structures for microwave circuits for low-cost, satisfactory performances, and light weight applications [89]. In microstrip applications, even one small discontinuity has a

considerable effect on the performance of the circuits, and it is worthy to model these discontinuities to fully understand their behavior [92].

Some examples to these discontinuities are gaps, steps, double steps, open ended lines, crossings, slots, and etc. Microstrip bend is one such discontinuity, which has chances to be improved with mitering the corners [90], or using square cutouts from the corners [91].

By mitering the corners of the microstrip 45° bends, the parasitic capacitance to ground of the bend is decreased [90].

Remember that the designed, fabricated, and measured inductors in this work are microstrip square planar spiral inductors. Inspired from the same idea of decreasing capacitance from mitered microstrip 45° bends, the designed inductors are fabricated with 45° corners, and 50% mitering. An example illustration is provided in Figure 4-22.

The fabrication of these inductors is the same as the normal ones described above. The post-processes are also the same. The measurements and de-embedding procedure is also done to the mitered inductors. The measured mitered SPSIs' geometrical specifications together with electroplating information are provided in Table 4-9. Note that the mitered inductors are named beginning with "2". For example, "2U" is the mitered version of "1U".

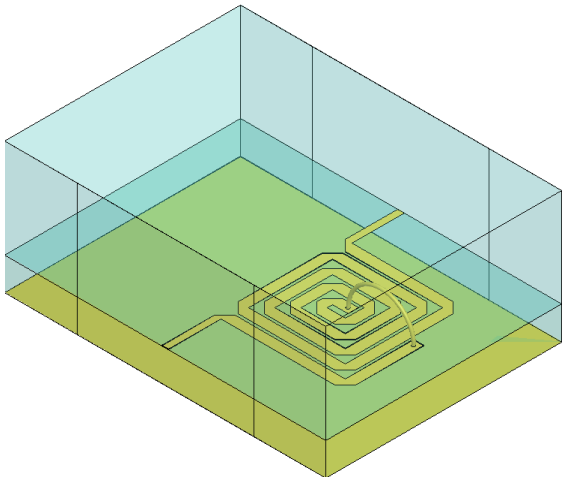


Figure 4-22. An illustration of a 4.75 turn mitered square planar spiral inductor on alumina substrate.

Table 4-9. The geometrical specifications of measured mitered square planar spiral inductors.

Name	W_{line} (um)	Spacing (um)	D_{out} (um)	Turn Number	Electroplated
2A	60	10	458	1.75	No
2D	120	10	668	1.75	No
2K	120	10	654	1.75	No
2KE	120	10	654	1.75	Yes
2OE	40	15	750	1.75	Yes
2R	100	15	811	2.75	No
2U	30	15	600	4.75	No
2V	30	20	634	4.75	No

These inductors are simulated on quartz substrate with process related data in HFSS. As described above, the lumped equivalent model parameters are extracted, and given in Table 4-10. The de-embedding is done as described in the above part, and from the de-embedded measurement results lumped equivalent model parameters are extracted. The extracted parameters are not given in here, instead the difference between the simulations and measurements are given in Table 4-11.

The difference between mitered SPSIs and normal SPSIs can be understood more smoothly by comparing the pairs. Such as pairs "1U" and "2U", "1V" and "2V". Before the measurements one should observe the comparison of S-parameters between these two pairs. Note that the geometrical specifications of the normal inductors are given in Table 4-5, and for mitered inductors in Table 4-9. The inductor pairs "1U" and "2U" EM simulated S-parameters comparison graph is given in Figure 4-23, together with quality-factor comparison graph. The blue lines represent the mitered inductor case and the red line represents the normal inductor case.

Table 4-10. Lumped equivalent model parameters for all measured mitered inductors simulated in HFSS on quartz substrate and fabrication related data.

Inductor Name	L_s (nH)	R_s (ohm)	C_{sh} (fF)
2A	1.983	2.800	25
2D	2.067	2.329	40
2K	1.994	2.304	39
2KE	1.795	1.157	37
2OE	4.561	1.654	44
2R	4.119	3.491	56
2U	10.917	9.052	37
2V	10.951	9.004	40

Table 4-11. Difference between the extracted Lumped equivalent model parameters for HFSS simulated and measurement results for all measured mitered inductors with additional microstrip lines 50 um line width and 900 um line length, EM simulated in HFSS.

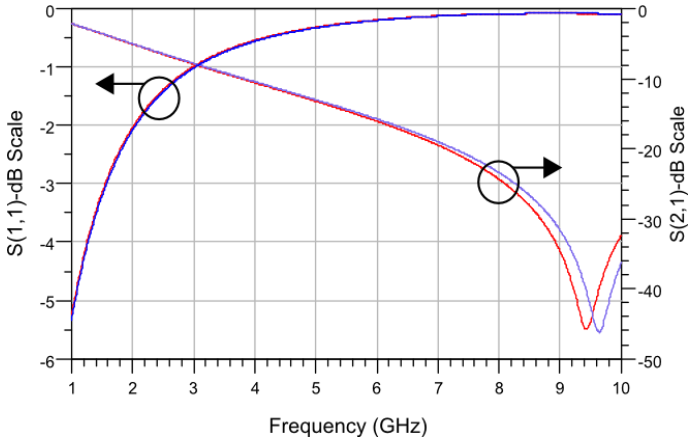
Inductor Name	ΔL_s (nH)	ΔR_s (ohm)	ΔC_{sh} (fF)
2A	0.101	0.671	2
2D	0.114	0.767	1
2K	0.05	0.694	2
2KE	0.036	0.112	2
2OE	0.067	0.062	5
2R	0.042	0.162	1
2U	0.072	1.277	11
2V	0.095	0.688	11

The first self-resonant frequency which is the parallel resonant frequency is shifted from 6.27 GHz to 6.35 GHz for the mitered case. An 80 MHz improvement has been achieved for the parallel resonant frequency. The second self-resonant frequency which is the series resonant frequency is improved from 9.45 GHz to 9.65 GHz, which is a 200 MHz improvement. The quality-factor maxima slightly decreased from the normal case; however the flatness of the quality-factor is increased for the mitered case.

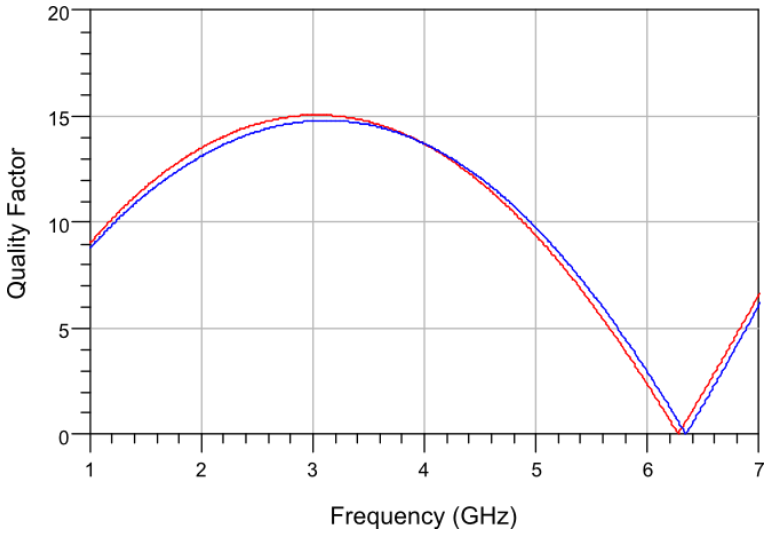
For the inductor pair of "1V" and "2V", the simulated S-parameters comparison and quality-factor comparison is provided in Figure 4-24. The line representations are the same as described above. One can observe that the parallel resonant frequency is shifted from 6.23 GHz to 6.27 GHz for the mitered case. This time the improvement is a bit low compared to the above one, i.e., a 40 MHz improvement is achieved. The

series resonant frequency improvement is about 200 MHz, in which the frequency shift is from 9.85 GHz to around 10.05 GHz. In this case, the quality-factor maxima and flatness are both improved.

An example comparison between the design and measured S-parameters are given in Figure 4-25 for the inductor named as "1U". Note that a good match between the design and measurements has been achieved.

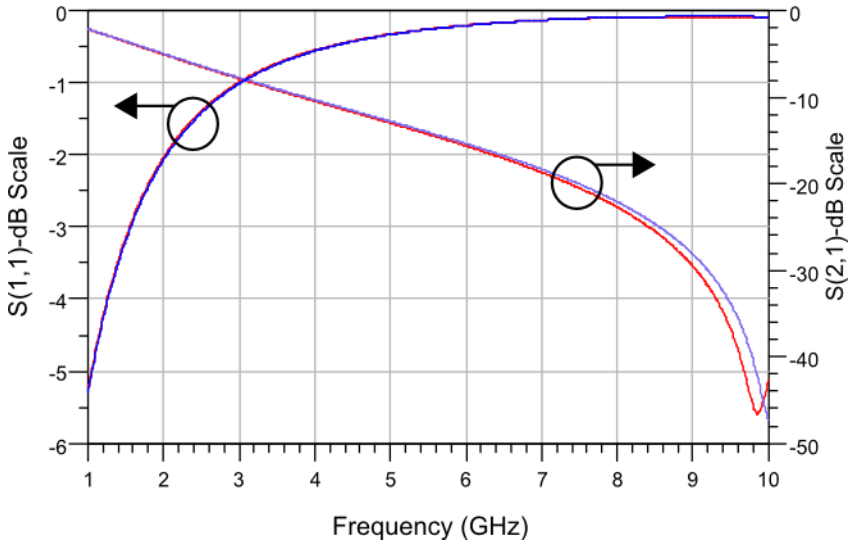


(a)

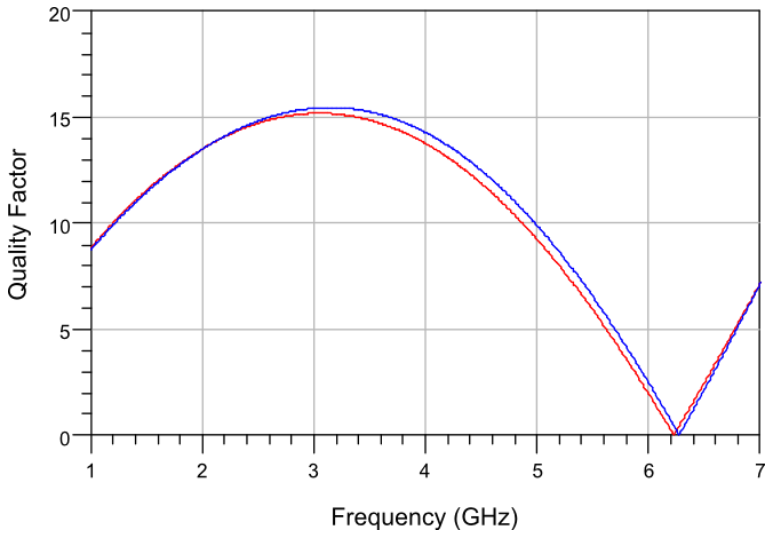


(b)

Figure 4-23. The simulated S-parameters comparison graphs for the normal inductor "1U" (red lines), and the mitered (blue lines) inductor named as "2U" (a) Return loss (y-left axis) and insertion loss (y-right axis), (b) Quality-factor.

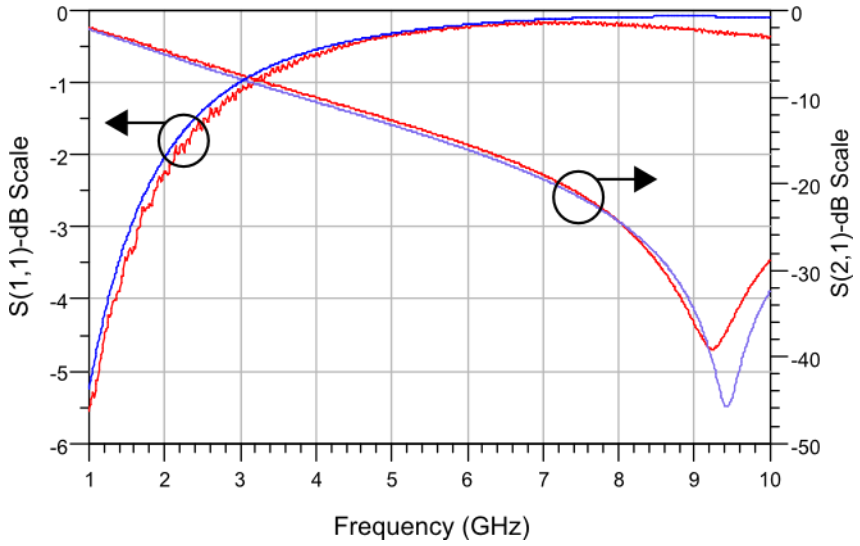


(a)

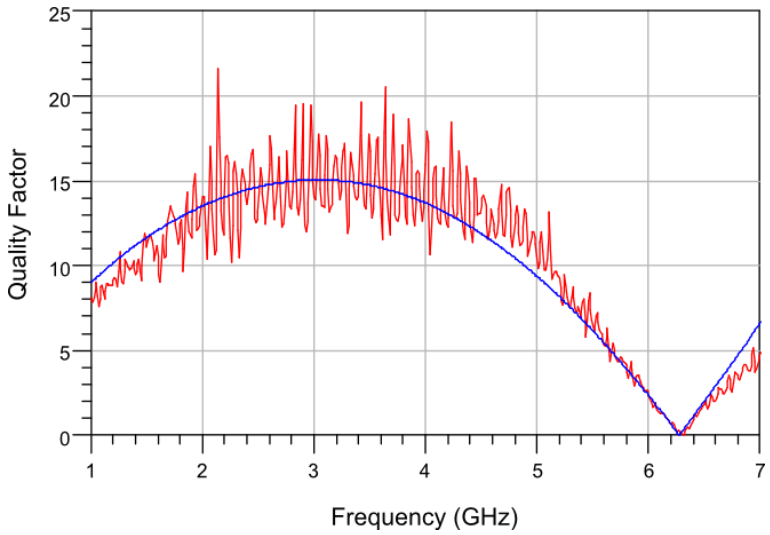


(b)

Figure 4-24. The simulated S-parameters comparison graphs for the normal inductor "1V" (red lines), and the mitered (blue lines) inductor named as "2V" (a) Return loss (y-left axis) and insertion loss (y-right axis), (b) Quality-factor.



(a)

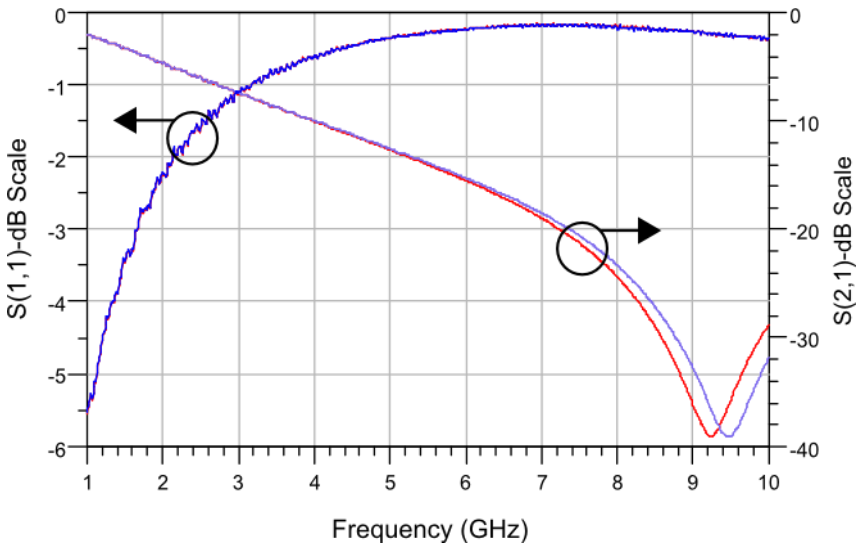


(b)

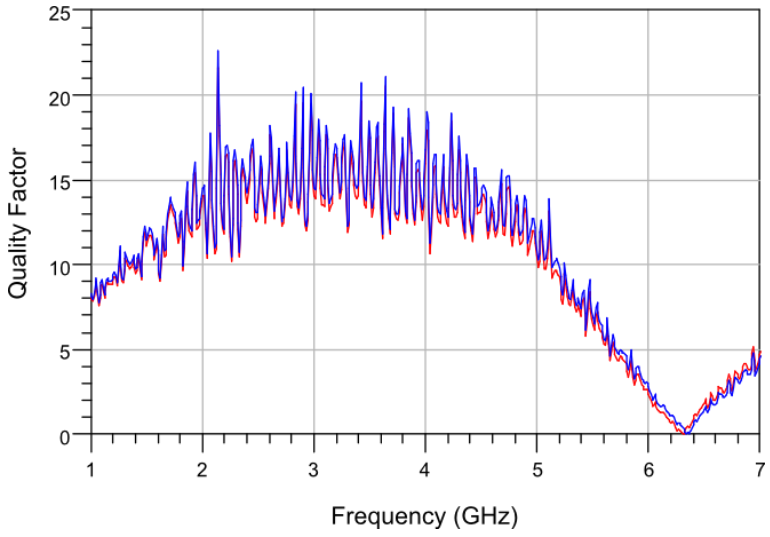
Figure 4-25. The simulated and measured S-parameters comparison graphs for the normal inductor "1U", red lines represent the measurement results and blue lines represent the EM simulation results (a) Return loss (y-left axis) and insertion loss (y-right axis), (b) Quality-factor.

In order to decide whether mitering has improved the inductor performance or not, could be understood from S-parameters and quality-factor comparisons for the measured inductor pairs. In Figure 4-26, the pair "1U" and "2U" is compared and S-parameters together with quality-factor are seen. The parallel resonant frequency is shifted from 6.31 GHz to 6.34 GHz, which means a 30 MHz improvement. From the

simulations the improvement is found to be 80 MHz (from 6.27 GHz to 6.35 GHz). The series resonant frequency, on the other hand, is improved from 9.22 GHz to 9.46 GHz, which is a 240 MHz improvement (larger than the simulated case-200 MHz).



(a)

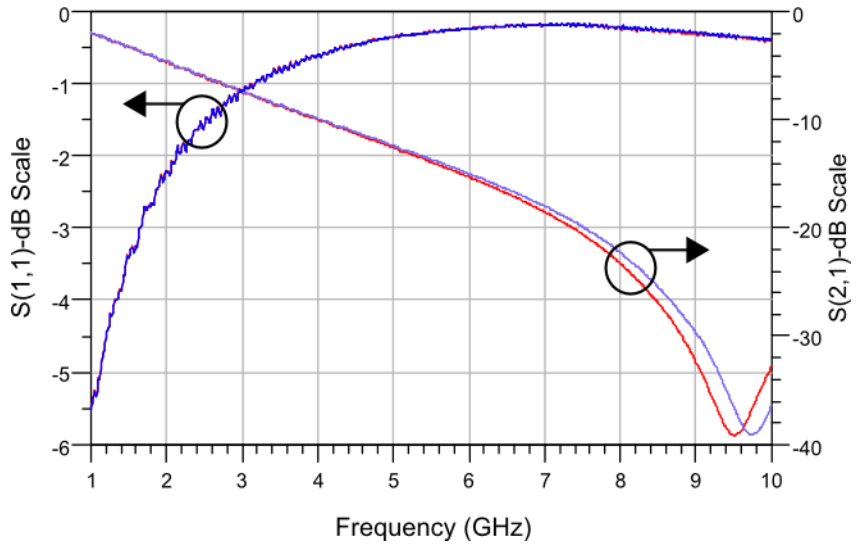


(b)

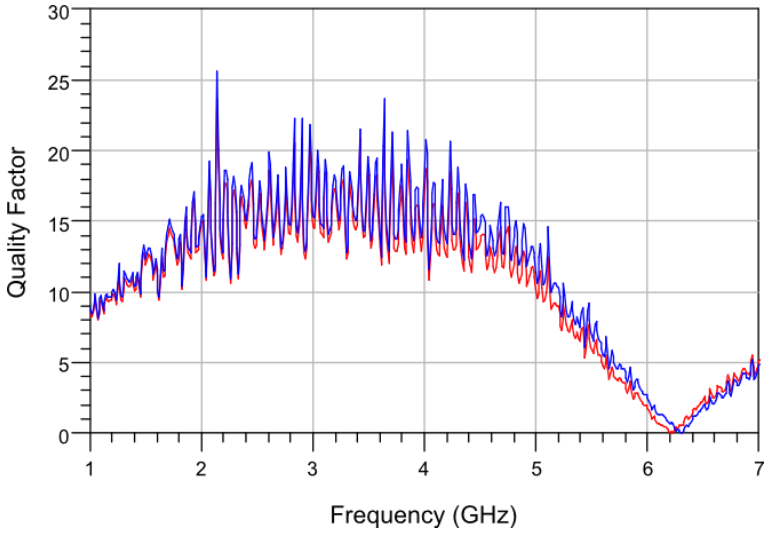
Figure 4-26. The measured S-parameters comparison graphs for the normal inductor "1U" (red lines), and the mitered (blue lines) inductor named as "2U" (a) Return loss (y-left axis) and insertion loss (y-right axis), (b) Quality-factor.

For the other pair, i.e., "1V" and "2V" pair, the comparison graphs are given in Figure 4-27. The improvement on parallel resonant frequency is 50 MHz, from 6.2 GHz to 6.25 GHz. The improvement on series resonant frequency is 230 MHz from 9.51 GHz

to 9.74 GHz. Both are higher improvements than the expected ones. The results are promising in a way that, these mitering percentages are same for every trace width which is 50%. A better approach could be made by finding the optimum mitering percentages for different trace widths, and then the mitered could be applied.



(a)



(b)

Figure 4-27. The measured S-parameters comparison graphs for the normal inductor "1V" (red lines), and the mitered (blue lines) inductor named as "2V" (a) Return loss (y-left axis) and insertion loss (y-right axis), (b) Quality-factor.

As one can observe the extracted lumped equivalent model parameters for measurements, mitering has effects on inductors; such as, the inductance is

decreased, as well as the series parasitic resistance. On the contrary, the shunt parasitic capacitances are not changed. The increase in parallel resonant frequency, and series resonant frequency could be explained as the decrease in inductance is lower than the decrease in resistance, and hence the SRFs increased, quality-factors are flattened.

Table 4-12. Extracted Lumped equivalent model parameters for all measured normal and mitered pair inductors with additional microstrip lines with EM simulated in HFSS, 50 um line width and 900 um line length.

Inductor Name	L_s (nH)	R_s (ohm)	C_{sh} (fF)
1U	11.011	10.636	48
1V	11.146	10.12	52
2U	10.989	10.329	48
2V	11.046	9.692	51

In the next sub-section, the design, process considerations, and etc. for the Metal-Insulator-Metal (MIM) capacitors are examined.

4.3 The design of Metal-Insulator-Metal (MIM) Capacitors.

Before going deep into the design of MIM capacitors, literature is discussed briefly below, to fully understand the importance of capacitors in use of lumped elements.

The lumped capacitors, like lumped inductors, have been used for over four decades for low-cost, and small size microwave integrated circuits [93], [94]. The first examples of lumped capacitors are the interdigitated capacitors [93], [94]. These type capacitors have well-known responses, at first, coming from the distributed approach [27]. However, with this topology one can achieve barely around 1 pF without degradation in the lumped element response. For that reason, a more complex fabrication but denser capacitance; Metal-Insulator-Metal (MIM) capacitors are extensively used. To increase the usefulness of the MIM capacitors; such as decreasing circuit size, the researchers have been focused on increasing the capacitance density over a unit area by either decreasing the dielectric thickness [95], or using different dielectrics [96], [97]. The most important property of surface

micromachined MIM capacitors is to become tunable using MEMS technology [98]. By using these tunable capacitors, one can construct tunable filters as in [99], and [100].

However, in the frame of this work, the capacitors are optimally designed using possible abilities in geometry.

When designing MIM (Metal-Insulator-Metal) capacitor the only formulation used was the parallel plate capacitance formulation. The thickness of the dielectric layer that is the nitrate was chosen as 0.3 µm according to the previously studied cases by the RF MEMS group in which the fabrication steps had already been considered. The dielectric permittivity was chosen as 6.9 according to the previously measured MIM capacitances. The designed MIM capacitance looks like in Figure 4-28. The width of the overlap changes in three values as 50 µm, 100 µm, and 200 µm. According to those three values three separate calculations were made in order to calculate the length of the overlap area. After a few iterations the formulations appear as;

$C = 0.01065 * l\_cap$ for 50 µm width case,

$C = 0.020963 * l\_cap$ for 100 µm width case,

$C = 0.0416875 * l\_cap$ for 200 µm width case.

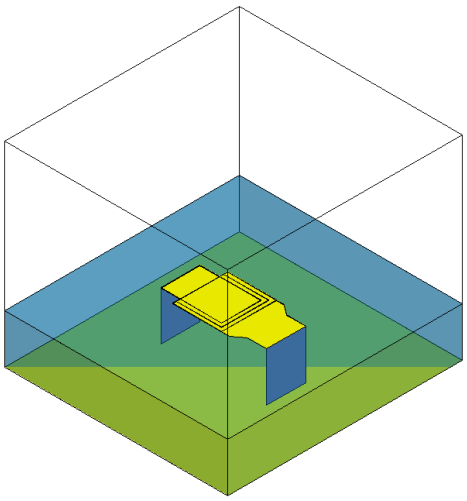


Figure 4-28. Illustration of the designed MIM capacitor in HFSS.

The model can be observed from Figure 4-29. Note that the parallel resistance is ignored since it has very little effect on model and it is very large (please refer to the

equivalent circuit of inductors on silicon). Parallel capacitance is not ignored yet it can be ignored in some cases. Also the shunt capacitances help the model fits to the EM simulation. The feed lines are 100 µm long and they are also included in the simulations results, no de-embedding has been done, since it is not necessary, because the capacitors are used with these additional lines. For the MIM capacitance case the quality factor is not investigated, since the quality factor values are very high for MIM capacitors.

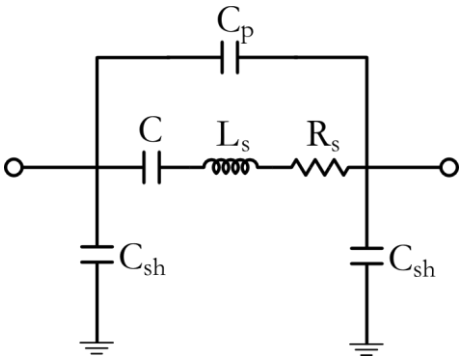
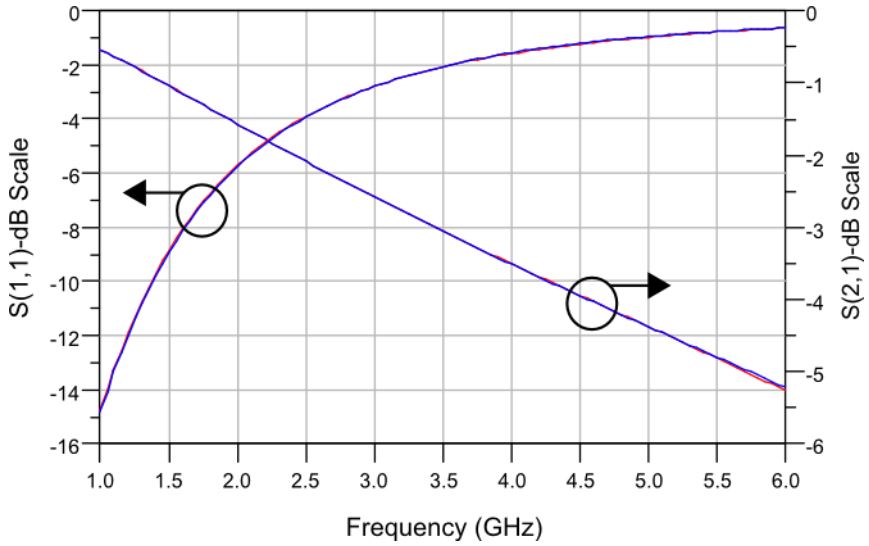


Figure 4-29. Illustration of lumped equivalent model of MIM capacitors, for alumina and/or quartz substrates.

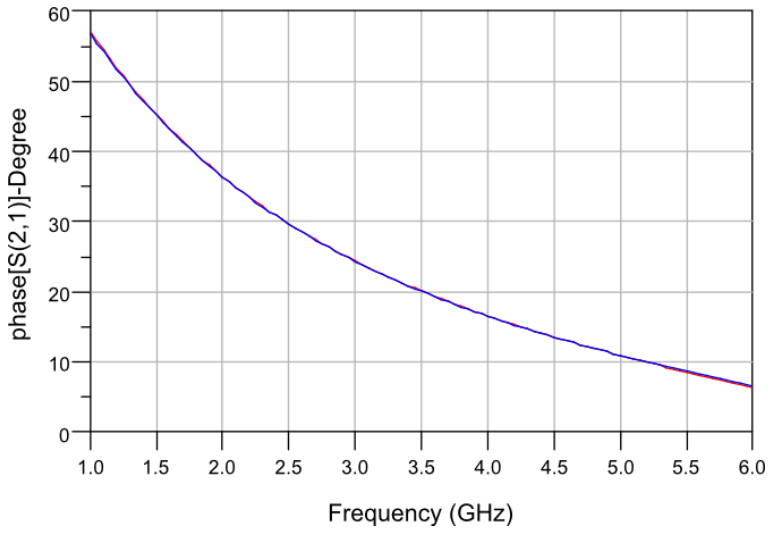
4.3.1 The Effect of Width on MIM Capacitors

In order to show the effects of width values of 50 µm and 100 µm of the overlap area of the MIM capacitor; two EM simulations and two model fitting are done and the comparison is done according to the model fitted values. The two simulations are predicted to give the exact capacitance value. The EM simulations are all done in HFSS 12, similar to the inductors. For 50 µm width of the overlap area the length of the overlap area is calculated to be 96 µm, and for 100 µm width of the overlap area of the capacitor the length of the overlap area is calculated to be 48 µm. The model fitted S-parameters results and the EM simulated S-parameters comparisons are given in the following two figures as Figure 4-30 for the overlap width of 100 µm and overlap length of 48 µm, and Figure 4-31 for the overlap width of 50 µm and the overlap length of 96 µm. The model fitted lumped equivalent values can be found in Table 4-13 for the two capacitors for different width and length values of overlap

area. As it can be observed from Table 4-13, with increasing width of the overlap area, the series parasitic resistance and the series parasitic inductance values are decreased with a very slight increase in the shunt parasitic capacitances.

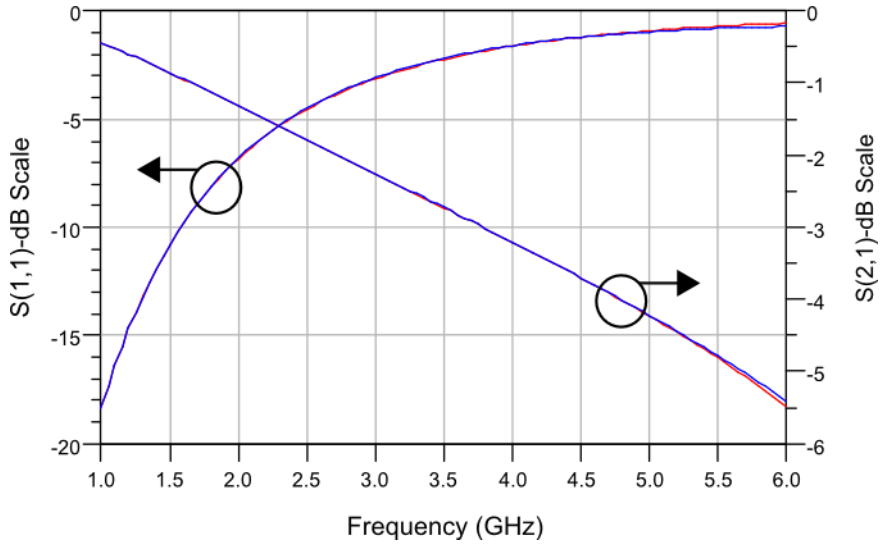


(a)

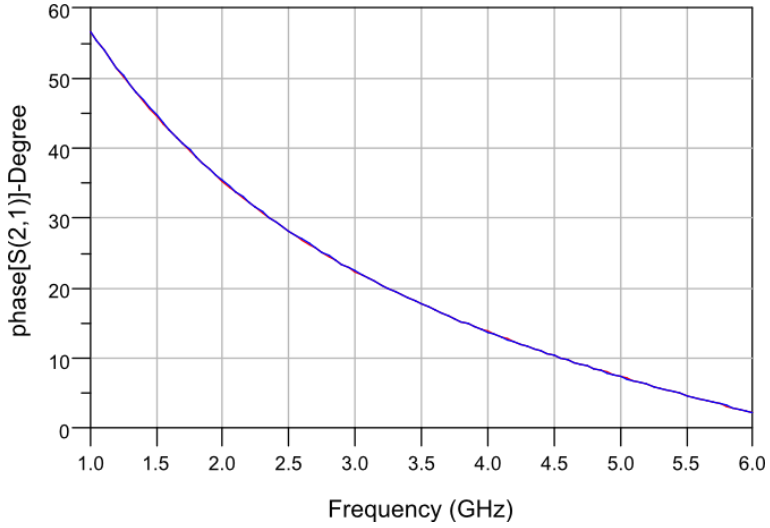


(b)

Figure 4-30. The S-parameters comparison of the model fitting (blue lines) and the EM simulation (red lines) of the overlap width of 100 µm and overlap length of 48 µm.



(a)



(b)

Figure 4-31. The S-parameters comparison of the model fitting (blue lines) and the EM simulation (red lines) of the overlap width of 50 µm and overlap length of 96 µm.

Table 4-13. The lumped equivalent model fitted MIM capacitors for different width and length values.

	Width (µm)	Length (µm)	C (pF)	C_{sh} (fF)	L_s (pH)	R_s (ohm)
C1	50	96	1.025	36	511	0.345
C2	100	48	1.024	40	366	0.168

4.3.2 The Effect of Metallization Thickness

Remember that when designing planar spiral inductors it is shown that thickness has a considerable effect on the performance of the inductor in terms of the series loss parasitic resistance, and a smaller effect on the inductance value of the planar spiral inductors.

However, in the case of MIM capacitor, the structure is smaller than the planar spiral inductors in comparison of the sizes. In that case, it is thought to investigate the metallization thickness effects on the lumped element model MIM capacitor.

Also the electroplating case is also considered. In the end, there are four case investigated for the effect of metallization thickness on the capacitor. The thicknesses are considered to be 0.8 µm, 1 µm, 2 µm, and the electroplating case of 7 µm. It is better to note that the metallization thickness of 2 µm is not simulated as electroplating, however; according to the fabrication this metallization thickness is a bit high to produce. It is examined to see how it would affect the capacitor.

Also it is better to note that the electroplating case is a bit different than the planar spiral inductor case, in a way that the overlap area is not electroplated in the simulations since the feed line and the overlap area could touch and forms a direct path.

The capacitor with changing thickness has the overlap dimensions of 50 µm in width and 92 µm in length. One can find the lumped element model parameters comparison in Table 4-14.

Table 4-14. The metallization thickness comparison of lumped element model parameters for an MIM capacitor.

	Width (μm)	Length (μm)	Thickness	C (pF)	C_{sh} (fF)	L_s (pH)	R_s (ohm)
C1	50	92	0.8 μm	0.988	36	504	0.396
C2	50	92	1 μm	0.985	36	507	0.358
C3	50	92	2 μm	0.98	36	506	0.262
C4	50	92	7 μm	0.976	35	507	0.236

As it can be observed from Table 4-14, the metallization thickness has a very little effect on the capacitance, series parasitic inductance, and the parallel parasitic capacitance values. It has nearly no effect on the shunt capacitance to the ground. Obviously, it has a considerable effect on the series parasitic resistance. But since the series parasitic resistance does not change so much it is decided to fix the metallization thickness on 1 μm. However, it is always possible to decrease the losses by increasing the metallization thickness whenever and wherever it is necessary.

4.3.3 Achieving the Desired Capacitance Values

The capacitances desired to be obtained are for the 2 to 4 GHz 90° phase shift bit capacitances. In Table 4-15, one can find the desired capacitances in the circuit topology. Note that the desired capacitances are designed for two different width values as 50 μm overlap width and 100 μm overlap width. For some capacitance values 50 μm width case more convenient than the 100 μm width case and for most of the cases 100 μm case has an advantage on 50 μm case. However, from the layout perspective it is better to design the capacitance with an overlap width of 100 μm or 200 μm according to the needs.

Note that the lumped element model S-parameters and EM simulation S-parameters comparison are not given in this case since they are very similar to the above ones. The comparison table for the 50 μm and 100 μm width cases are given in Table 4-15.

The next move is to use these models in the total phase shift bit model and see how those affect the performance of the phase shifter.

Table 4-15. The designed MIM capacitances for 50 µm and 100 µm overlap width cases together with lumped element model parameter values.

Desired (pF)	**Width (µm)**	**Length (µm)**	**C (pF)**	**C_{sh} (fF)**	**L_s (pH)**	**R_s (ohm)**
0.98	50	92	0.982	36	506	0.35
	100	46	0.978	39	369	0.182
3.92	50	368	3.918	53	687	0.547
	100	187	3.923	50	442	0.217
0.29	50	27	0.285	31	512	0.396
	100	14	0.291	37	415	0.251
1.16	50	109	1.16	37	519	0.37
	100	55	1.173	40	371	0.178
0.4	50	37	0.399	32	483	0.361
	100	19	0.414	37	363	0.194
1.6	50	150	1.599	39	546	0.396
	100	76	1.613	42	381	0.183
0.71	50	67	0.722	34	492	0.344
	100	33	0.708	38	362	0.183
2.84	50	267	2.833	47	623	0.475
	100	135	2.841	46	413	0.196

CHAPTER 5

DESIGN OF BROADBAND AND ULTRA WIDE-BAND (UWB) PHASE SHIFTERS USING SURFACE MICROMACHINED LUMPED COMPONENTS

Bear in mind that the ideal design procedure of phase shifters are given in Chapter 3. At the end of that chapter, ideal lumped element values are presented for phase shifters operating in various frequency bands. Afterwards, the theory and ideal design of phase shifters, the surface micromachined lumped components are examined. The design of these components, fabrication, and measurement results are provided in Chapter 4. These two chapters are important, for achieving a practical and final design of broadband and UWB (ultra wide-band) phase shifters implemented with surface micromachined lumped components.

In this chapter, the practical designs of 1 to 2 GHz, 2 to 4 GHz, 3 to 6 GHz, and 1 to 6 GHz; 22.5°, 45°, 90°, and 180° phase shift bits are presented. The practical design procedure of one phase shift bit is the only one explained in detail, because the procedure is exactly the same for the rest of the bits. The final results for the other phase shift bits are presented. For each bit, a comparison of the phase characteristics between the ideal and practical design is presented.

Remember that the ideal design of phase shifters are already presented, however, the return loss and insertion loss results are not presented, since the all-pass network phase shifters are inherently matched to system impedance, and the components have no loss at all. In this chapter, because the components are, now, not ideal, the return loss and insertion loss results are also of concern. Well matched (low return loss), and low-loss (low insertion loss) circuits are designed and presented.

5.1 Design of 4-bit 1 to 2 GHz Broadband Phase Shifter

In this part, 1 to 2 GHz phase shifter 22.5°, 45°, 90°, and 180° phase shift bit practical designs results are given. In order to give an example of the design procedure of all phase shift bits, the 1 to 2 GHz 180° phase shift bit is explained in detail, step by step.

One of the most important issues about the design of 1 to 2 GHz phase shifter is the high inductance and capacitance values. Nearly half of the inductors are designed with a turn number of 1.75 for relatively low inductance values. On the other hand, the other half is designed with 2.75 turn number, to decrease the size of the circuit, to achieve flat quality-factor, and high quality-factor values within the band of interest.

5.1.1 Design of 180° Phase Shift Bit

After designing a few phase shift bits with different design algorithms, an effective, proper, and relatively easy design procedure is determined. The design procedure can be ordered as follows;

- First of all, the series connected MIM capacitors should be designed according to the largest series MIM capacitor's length. Then the shunt connected MIM capacitors should be designed to their exact values and the lumped equivalent models should be extracted.
- From this point on, with the reference length of the largest series connected MIM capacitor, the extension length of the planar spiral inductors should be computed. With the computed value of the extension length of the inductors, various trace width and spacing values should be tried in order to decide on the most appropriate planar spiral inductors, the procedure for the appropriate planar spiral inductor selection must be done with EM simulation in HFSS and using ADS to achieve the lumped element equivalent models of the inductors.

- To decide the configurations of the inductors, one must implement them in ADS to check the phase shifter response together with the simulated and model extracted capacitors. Remember that this procedure could be done with the extracted lumped element equivalent models of planar spiral inductors and MIM capacitors.
- After deciding the most appropriate SPSIs (Square Planar Spiral Inductor), one should compensate the shunt parasitic capacitances belonging to the SPSIs with decreasing the capacitance of the shunt connected MIM capacitors.
- The next step can be summarized as layout issues, such as; the design of the Tee junctions, and the additional microstrip transmission lines. The additional microstrip line length is computed as the maximum of the total length of the neighboring SPSIs.
- As the last step, one should compensate further the parasitic shunt capacitances by decreasing the capacitances of the shunt connected MIM capacitors, sometimes increasing is the case.

1 to 2 GHz phase shifter 180° phase shift bit was the first one to be designed. First of all, the series connected MIM capacitors are designed in order to give the same length as 449 µm. The length is determined according to the design of the highest valued series connected MIM capacitor. The geometrical parameters together with the associated lumped equivalent model parameters are given in Table 5-1.

After the series connected MIM capacitor designs are finished the first design of shunt connected capacitors are held. Remember that these designs would be changed according to the compensation of shunt parasitic capacitances of both shunt connected MIM capacitors and the square planar spiral inductors. The first design related geometrical parameters, and lumped equivalent model parameters are given in Table 5-2.

Table 5-1. 1 to 2 GHz phase shifter 180° phase shift bit series connected MIM capacitor design related geometrical parameter values, and the lumped equivalent model parameter values.

Width (μm)	Length (μm)	L_{feed} (μm)	C (pF)	C_{sh} (fF)	L_s (pH)	R_s (ohm)
100	119	100	2.507	45	404	0.196
100	21	149	0.454	43	442	0.278
100	42	138.5	0.891	44	428	0.247
100	59	130	1.257	44	420	0.23

Table 5-2. The 1 to 2 GHz 180° phase shift bit original circuit's designed shunt MIM capacitors with lumped equivalent model parameters.

	(pF)	Width (μm)	Length (μm)	C (pF)	C_{sh} (fF)	L_s (pH)	R_s (ohm)
C2_1	10	200	240	10.005	70	355	0.132
C2_2	1.8	100	85	1.798	42	386	0.182
C4_1	3.6	100	172	3.613	49	432	0.209
C4_2	5	100	240	5.035	54	468	0.231

The 1 to 2 GHz phase shifter 180° phase shift bit design is continued with selecting the planar spiral inductors. The selected configuration SPSIs are given in Table 5-3 respectively for 2.25 nH, 4.5 nH, 6.26 nH, and 12.5 nH inductance values. Note that 2.25 nH and 4.5 nH inductances are designed as 1.75 turn PSIs, on the other hand 6.26 nH and 12.5 nH inductances are designed as 2.75 turn PSIs. The quality factor related data is calculated within the band of interest, which is in this case 1 to 2 GHz.

All of the inductors are EM simulated and model extracted with line widths of 40 μm, 50 μm, 60 μm, 80 μm, 100 μm, and 120 μm, with spacing values of 10 μm, 15 μm, and 20 μm, and hence with different outer diameter values. For every inductor, this procedure is done together with extraction of quality-factor related data. An important note should be pointed out here that the quality factor has a considerable effect on differential phase, insertion loss, insertion loss imbalance within the band of interest, and amplitude imbalance of the phase shifter. For flat phase within the band of interest, low insertion loss imbalance within the band of interest, and low amplitude imbalance of the phase shifter, one should minimize the ripple in quality factor results (quality factor ripple is calculated as the absolute maximum difference between mean quality factor and max or min quality factor). For low insertion loss

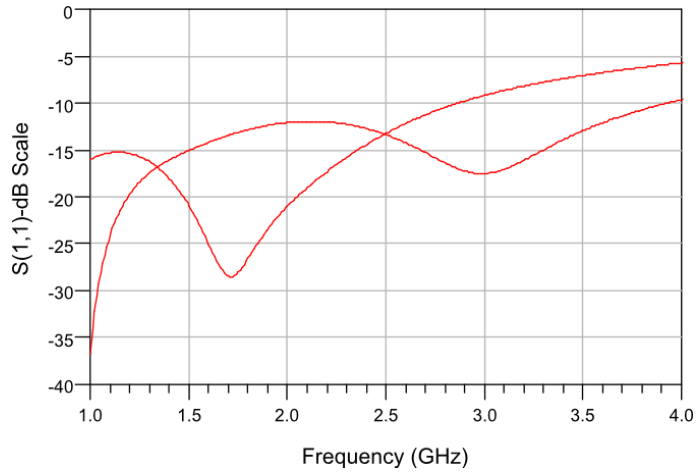
achievement, the chosen inductor must have a high quality factor (remember that quality factor is, also, a measure of the loss within the component).

One must also consider the extracted lumped equivalent model parameters for low return loss values, and flat phase response. The below given (Table 5-3) inductors are chosen based on the criteria explained above.

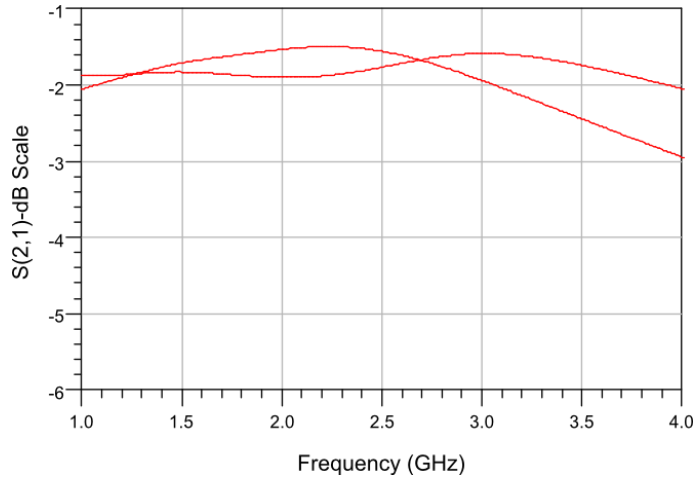
Table 5-3. 1 to 2 GHz phase shifter 180° phase shift bit configuration # 1 selection of SPSIs (first designs of PSIs).

W_{line} (μm)	Spacing (μm)	D_{out} (μm)	L_s (nH)	R_s (ohm)	C_{sh} (fF)	Q_{max}	Q_{ripple}	Q_{min}	Q_{mean}
100	15	712	2.242	0.632	143	52.055	9.491	34.525	44.016
120	20	1256	4.509	1.02	332	55.088	7.599	44.411	52.010
120	20	1200	6.235	1.480	376	43.887	4.612	37.403	42.015
40	20	1148	12.45	3.284	288	31.925	8.937	19.448	28.384

With these designs and the previously designed MIM capacitors, a whole phase shift bit simulation was done with lumped equivalent models of the components. The S-parameter results are given in Figure 5-1. Note that the ideal design's return loss and insertion loss plots are not provided for all cases. The differential phase shift response is given in Figure 5-2. The differential phase shift related calculation results are given in Table 5-4. Observing the results, the responses of both S-parameters and differential phase shift are not satisfactory. The iterations are done on shunt connected MIM capacitors.



(a)



(b)

Figure 5-1. The 1 to 2 GHz phase shifter 180° phase shift bit configuration # 1 S-parameters (a) return loss for the practical case, and (b) insertion loss for the practical case.

After that shunt connected MIM capacitors are redesigned according to some calculations that reduced to compensate the shunt parasitic capacitors of the SPSIs. The iterated shunt connected capacitors are given in Table 5-5. The results for this case are given in Figure 5-3 for S-parameters comparison, and Figure 5-4 for the differential phase shift characteristics. The differential phase shift related calculation results are given in Table 5-6. Observing the results, it is obvious that the differential phase shift response is a little bit improved in terms of phase ripple together with S-parameter results.

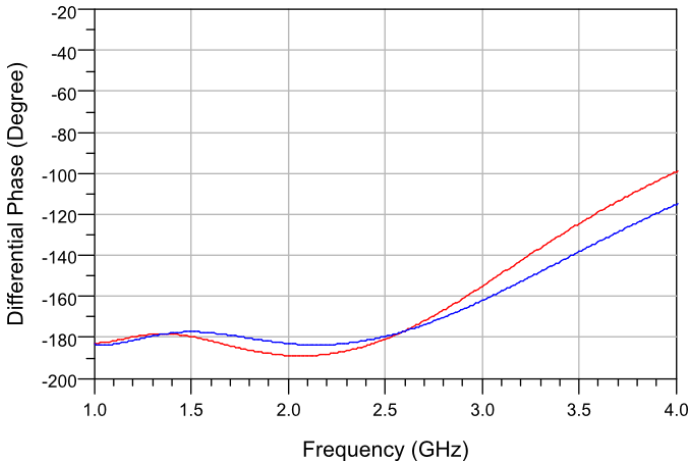


Figure 5-2. The differential phase shift response of 1 to 2 GHz phase shifter 180° phase shift bit configuration # 1 (red line represents the present case, and blue line represents the ideal case).

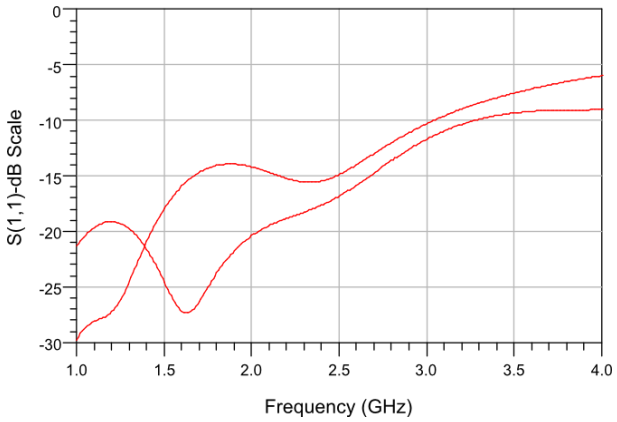
Table 5-4. Calculated mean phase, minimum phase, rms phase, maximum phase and phase ripple comparison between the ideal case and the configuration # 1 of 1 to 2 GHz phase shifter 180° phase shift bit.

	Min. Phase (°)	**Rms Phase (°)**	**Max. Phase (°)**	**Ripple (°)**
Ideal	177.357	180.230	183.636	3.419
Present case	178.330	182.463	188.821	6.389

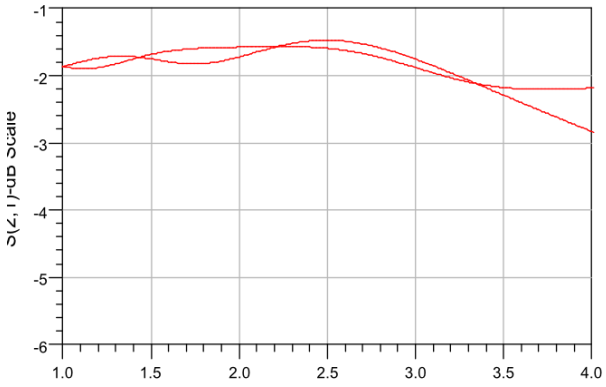
Table 5-5. The compensated shunt MIM capacitors with their lumped equivalent model parameter values, and the overlap area width and length for configuration # 1.

	(pF)	**Width (µm)**	**Length (µm)**	**C (pF)**	**C_{sh} (fF)**	**L_s (pH)**	**R_s (ohm)**
C2_1	10	200	224	9.346	69	352	0.142
C2_2	1.8	100	69	1.464	41	378	0.18
C4_1	3.6	100	137	2.888	46	413	0.196
C4_2	5	100	200	4.191	51	449	0.217

After this step, layout considerations are of concern. The suitable Tee junctions are added to the schematic and the results are obtained. The S-parameter comparison graphs are given in Figure 5-5, and differential phase shift related graphs are given in Figure 5-6, with some calculation results as in Table 5-7. The results are quite satisfactory.



(a)



(b)

Figure 5-3. The 1 to 2 GHz phase shifter 180° phase shift bit configuration # 1 with iterated shunt MIM capacitors S-parameters (a) return loss for the practical case, and (b) insertion loss for the practical case.

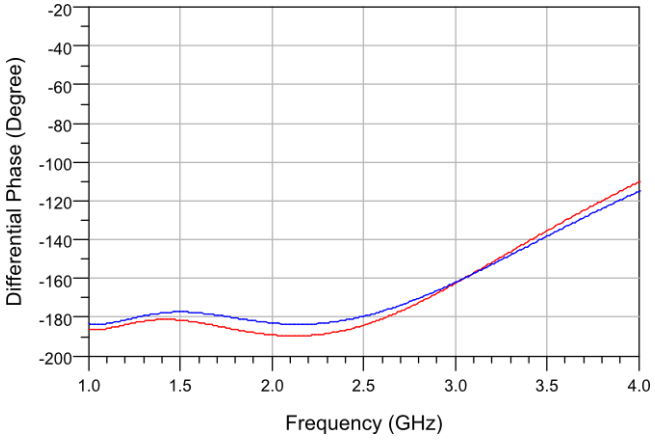
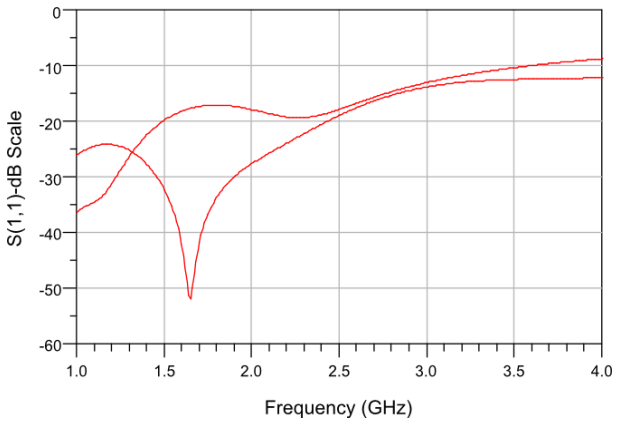


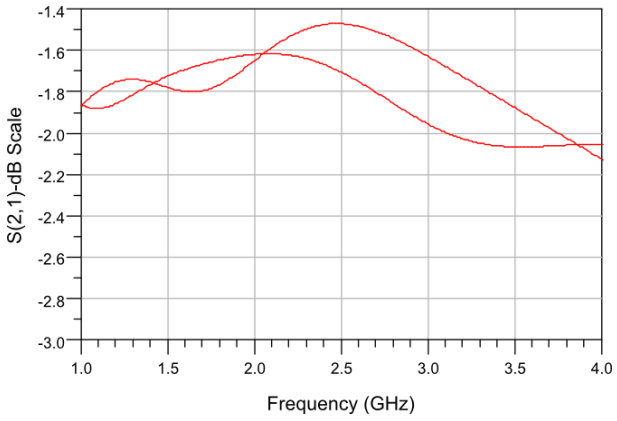
Figure 5-4. The differential phase shift response of 1 to 2 GHz phase shifter 180° phase shift bit configuration # 1 with iterated shunt MIM capacitors (red line represents the present case, and blue line represents the ideal case).

Table 5-6. Calculated mean phase, minimum phase, rms phase, maximum phase and phase ripple comparison between the ideal case and the configuration # 1 with iterated shunt MIM capacitors of 1 to 2 GHz phase shifter 180° phase shift bit.

	Min. Phase (°)	**Rms Phase (°)**	**Max. Phase (°)**	**Ripple (°)**
Ideal	177.357	180.230	183.636	3.419
Present case	181.199	184.486	189.151	4.681



(a)



(b)

Figure 5-5. The 1 to 2 GHz phase shifter 180° phase shift bit configuration # 1 with iterated shunt MIM capacitors and added Tee junctions to the circuit; S-parameters (a) return loss for the practical case, and (b) insertion loss for the practical case.

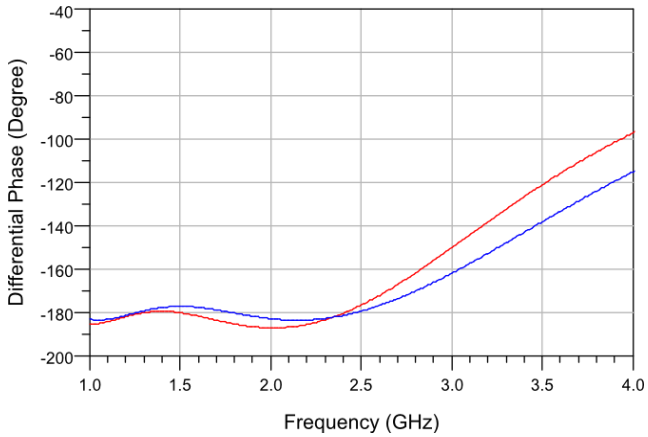


Figure 5-6. The differential phase shift response of 1 to 2 GHz phase shifter 180° phase shift bit configuration # 1 with iterated shunt MIM capacitors and added Tee junctions (red line represents the present case, and blue line represents the ideal case).

Table 5-7. Calculated mean phase, minimum phase, rms phase, maximum phase and phase ripple comparison between the ideal case and the configuration # 1 with iterated shunt MIM capacitors and added Tee junctions of 1 to 2 GHz phase shifter 180° phase shift bit.

	Min. Phase (°)	**Rms Phase (°)**	**Max. Phase (°)**	**Ripple (°)**
Ideal	177.357	180.230	183.636	3.419
Present case	179.668	183.146	187.267	4.139

Further increasing the layout concerns leads to redesigning the SPSIs with some extended lines. The extension lengths are found to be 174.5 µm for 2.25 nH, 4.5 nH, and 6.26 nH; and it was found to be 124.5 µm for 12.5 nH inductor since this inductor is connected to 200 µm width MIM capacitor, with considering the longest series connected MIM capacitor. The layout considered PSIs for 1.75 turn could be observed as an example in Figure 5-7, and for 2.75 turn as in Figure 5-8.

The resultant layout considered SPSI related geometrical data together with some quality-factor related calculation results and lumped equivalent model related parameter results are given in the following Table 5-8.

The additional microstrip line length between the stages was computed as 2260 µm. Only the EM simulation results are used in this layout consideration case. The S-parameters comparison graphs are given in Figure 5-9, and the differential phase shift

graph is given in Figure 5-10, together with some phase characteristic related calculation results as in Table 5-9.

The insertion and return loss results are quite satisfactory. On the other hand, the differential phase related results could be better than the present case, for that reason some iterations are done on layout considered schematic.

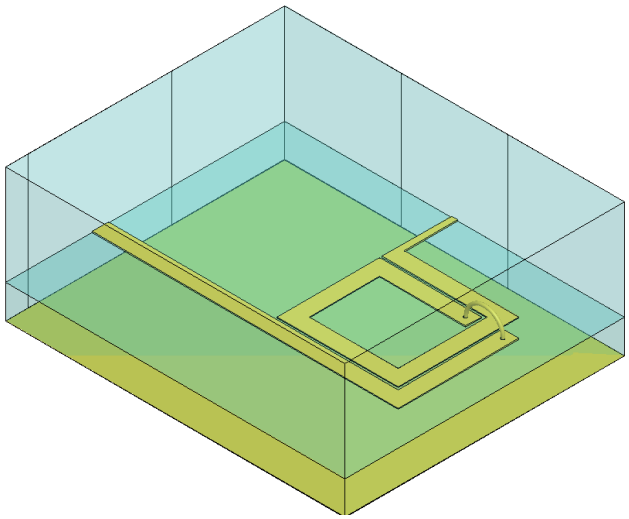


Figure 5-7. An example of layout considered 1.75 turn PSI.

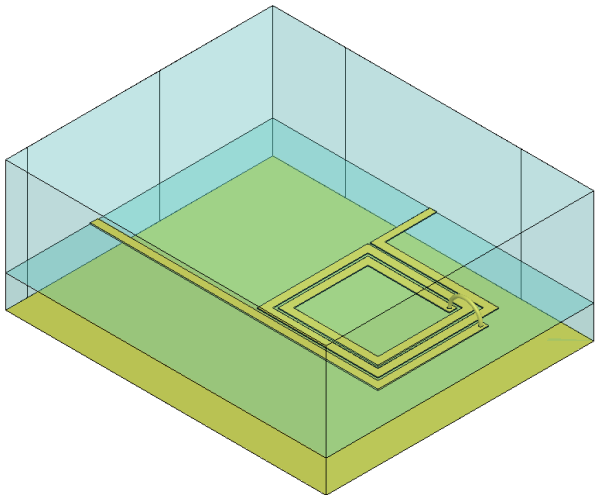
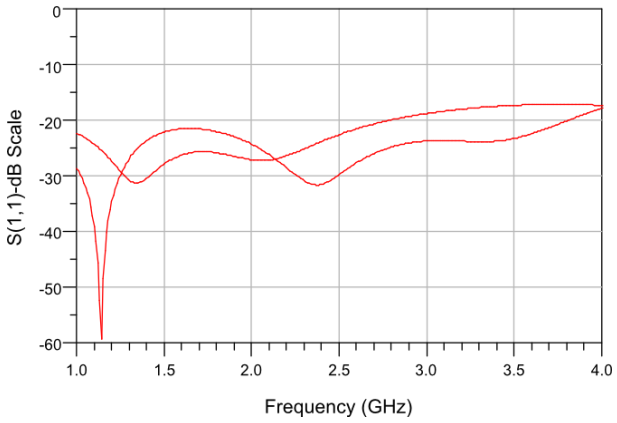


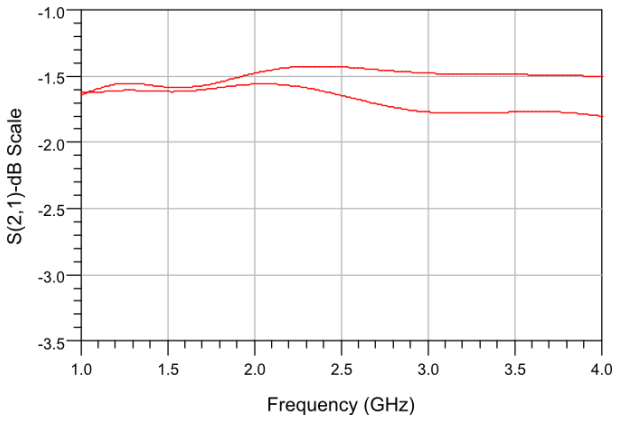
Figure 5-8. An example of layout considered 2.75 turn PSI.

Table 5-8. The layout designs of selected PSIs for configuration # 1 (with extension lengths of 174.5 µm for 2.25 nH, 4.5 nH, and 6.26 nH, and 124.5 µm for 12.5 nH).

W_{line} (µm)	Spacing (µm)	D_{out} (µm)	L_s (nH)	R_s (ohm)	C_{sh} (fF)	Q_{max}	Q_{ripple}	Q_{min}	Q_{mean}
100	15	694	2.277	0.713	142	51.062	9.817	33.167	42.984
120	20	1248	4.507	1.145	341	56.388	5.796	48.543	54.339
120	20	1170	6.34	1.445	368	47.274	4.793	40.515	45.308
40	20	1010	12.595	3.174	268	34.720	4.317	28.666	32.983



(a)



(b)

Figure 5-9. The 1 to 2 GHz phase shifter 180° phase shift bit configuration # 1 layout considered S-parameters graphs for practical case (a) return loss for the practical case, and (b) insertion loss for the practical case.

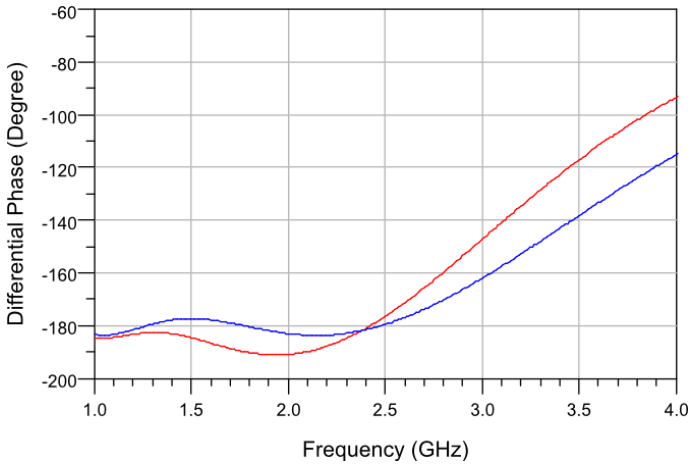


Figure 5-10. The differential phase shift response of 1 to 2 GHz phase shifter 180° phase shift bit configuration # layout considered (red line represents the present case, and blue line represents the ideal case).

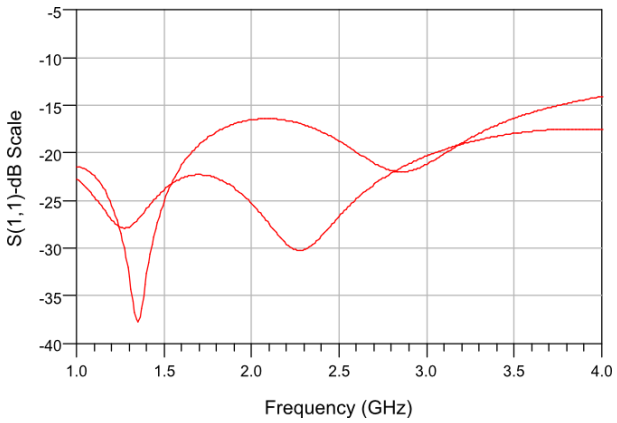
Table 5-9. Calculated mean phase, minimum phase, rms phase, maximum phase and phase ripple comparison between the ideal case and the configuration # 1 layout consideration of 1 to 2 GHz phase shifter 180° phase shift bit.

	Min. Phase (°)	**Rms Phase (°)**	**Max. Phase (°)**	**Ripple (°)**
Ideal	177.357	180.230	183.636	3.419
Present case	182.594	186.312	191.150	4.864

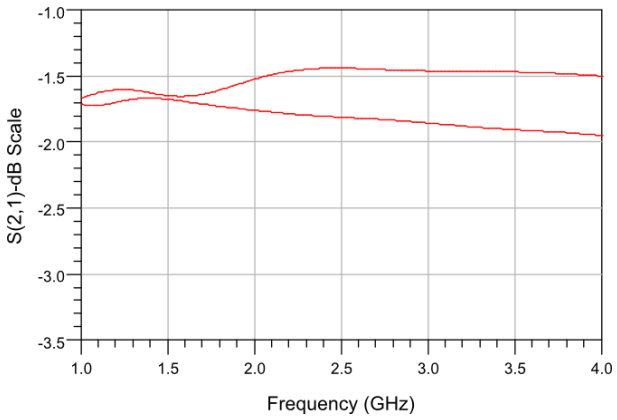
After the iterations, the desired phase shift response with satisfactory insertion and return loss results have been obtained. The present iterations are done only on the shunt connected MIM capacitors. The final designs of capacitors are given in Table 5-10. The obtained S-parameters comparison graphs and differential phase shift plot together with some phase shift related calculation results are given in Figure 5-11, Figure 5-12, and Table 5-11, respectively. The maximum return loss is around -16 dB, which corresponds to a considerably good result. The maximum insertion loss is around 1.7 dB, which is also a satisfactory result. The differential phase shift related results are in good shape as it can be observed in the figure and the related calculation results table. In fact, the ripple is found to be better than the design with ideal elements. The 1 to 2 GHz phase shifter 180° phase shift bit design is finished with this very last step.

Table 5-10. The final design of shunt connected MIM capacitors for configuration # 1 for 1 to 2 GHz phase shifter 180° phase shift bit.

	(pF)	Width (µm)	Length (µm)	C (pF)	C_{sh} (fF)	L_s (pH)	R_s (ohm)
C2_1	10	200	224	9.346	69	352	0.142
C2_2	1.8	100	82	1.734	42	385	0.183
C4_1	3.6	100	136	2.864	46	414	0.198
C4_2	5	100	200	4.191	51	449	0.217



(a)



(b)

Figure 5-11. The 1 to 2 GHz phase shifter 180° phase shift bit layout considered, and iterated shunt MIM capacitors; S-parameters graphs for practical case (a) return loss for the practical case, and (b) insertion loss for the practical case.

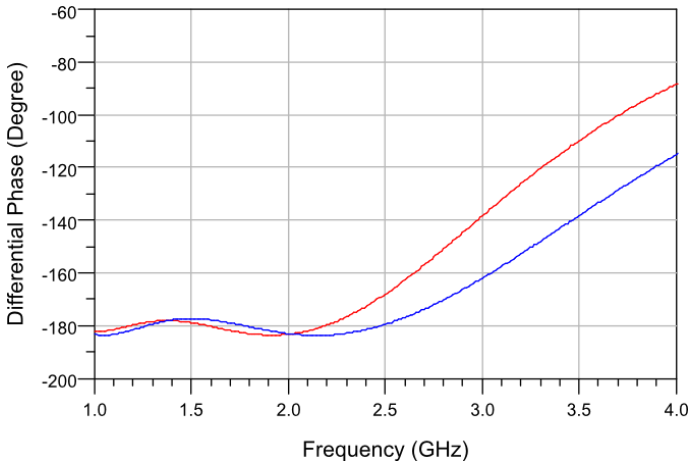


Figure 5-12. The differential phase shift response of 1 to 2 GHz phase shifter 180° phase shift bit layout considered, and iterated shunt MIM capacitors (red line represents the present case, and blue line represents the ideal case).

Table 5-11. Calculated mean phase, minimum phase, rms phase, maximum phase and phase ripple comparison between the ideal case and the finalized layout considerations of 1 to 2 GHz phase shifter 180° phase shift bit.

	Min. Phase (°)	**Rms Phase (°)**	**Max. Phase (°)**	**Ripple (°)**
Ideal	177.357	180.230	183.636	3.419
Present case	178.017	180.826	183.666	2.851

Considering the sizes and the layout view, one should refer to Figure 5-13 for the upper branch of 1 to 2 GHz phase shifter 180° phase shift bit, and for the lower branch refer to Figure 5-14.

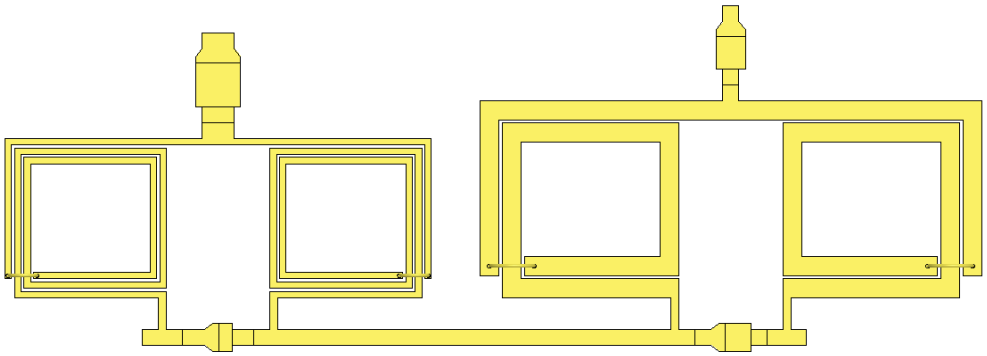


Figure 5-13. Upper branch of 1 to 2 GHz phase shifter 180° phase shift bit (Length: 6.116 mm, Width: 2.19 mm, Separation between inductors: 302 µm).

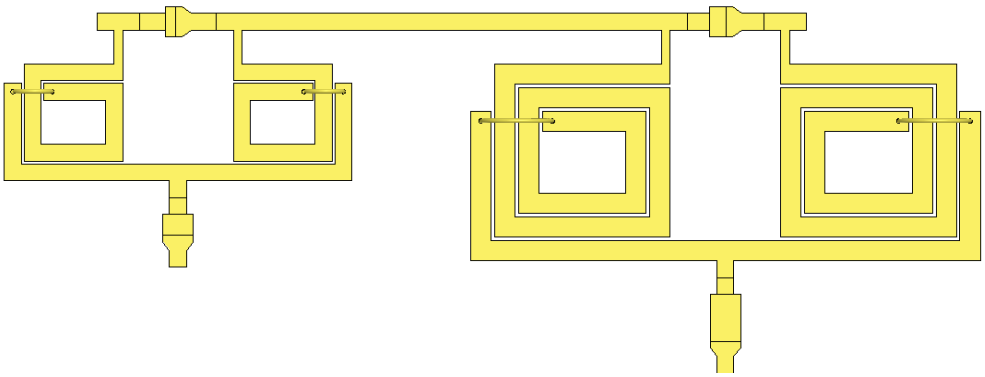


Figure 5-14. Lower branch of 1 to 2 GHz phase shifter 180° phase shift bit (Length: 5.722 mm, Width: 2.18 mm, Separation between inductors: 696 µm).

All other phase shift bits are designed according to the above described procedure. For the sake of simplicity, only the final design geometrical specifications of the phase shift bits for SPSIs, and MIM capacitors; and the finalized design return loss, insertion loss, and differential phase shift results are given.

5.1.2 Design of 90° Phase Shift Bit

The final series connected MIM capacitors design related data are given in Table 5-12, the layout considered SPSIs are given in Table 5-13, and the shunt connected MIM capacitors' final designs are given in Table 5-14. The S-parameters graphs of the final layout design are given in Figure 5-15, the differential phase shift related graph is given in Figure 5-16, with the phase shift related calculation results as in Table 5-15. It can be seen that these results have return loss around -19.6 dB, insertion loss around 1.7 dB at 1 GHz, in the worst case. The differential phase shift response is satisfactory.

Table 5-12. 1 to 2 GHz phase shifter 90° phase shift bit finalized series connected MIM capacitor design related geometrical parameter values, and the lumped equivalent model parameter values.

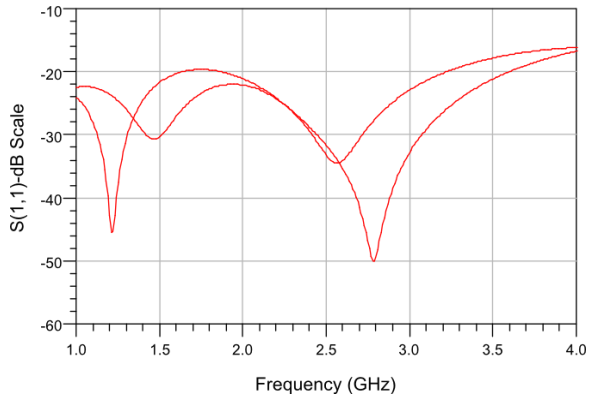
Width (µm)	Length (µm)	L_{feed} (µm)	C (pF)	C_{sh} (fF)	L_s (pH)	R_s (ohm)
100	92	100	1.943	43	389	0.183
100	27	132.5	0.581	42	410	0.228
100	37	127.5	0.797	42	402	0.219
100	67	112.5	1.426	43	393	0.205

Table 5-13. The finalized layout designs of selected SPSIs (with extension lengths of 161 µm and 111 µm).

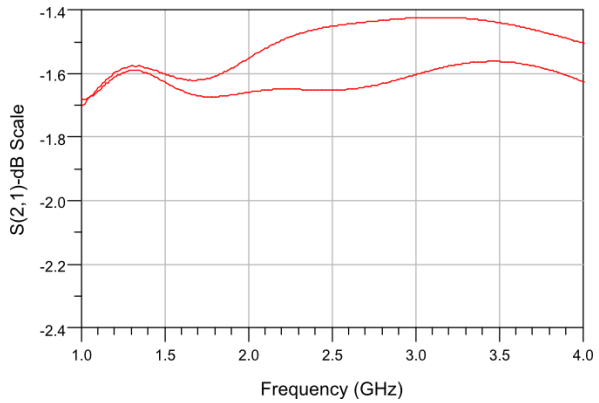
W_{line} (µm)	Spacing (µm)	D_{out} (µm)	L_s (nH)	R_s (ohm)	C_{sh} (fF)	Q_{max}	Q_{ripple}	Q_{min}	Q_{mean}
120	20	904	2.893	0.746	213	56.948	8.735	41.397	50.132
120	20	1136	3.979	1.001	298	55.247	8.084	43.264	51.347
100	20	1110	7.087	1.516	336	52.035	4.884	44.874	49.758
60	20	1016	9.769	2.217	282	39.156	2.966	34.677	37.643

Table 5-14. The final design of shunt connected MIM capacitors for 1 to 2 GHz phase shifter 90° phase shift bit.

	(pF)	Width (µm)	Length (µm)	C (pF)	C_{sh} (fF)	L_s (pH)	R_s (ohm)
C2_1	7.82	200	172	7.183	64	325	0.121
C2_2	2.3	100	97	2.048	43	392	0.184
C4_1	3.16	100	120	2.527	45	404	0.192
C4_2	5.67	200	118	4.953	59	299	0.109



(a)



(b)

Figure 5-15. The 1 to 2 GHz phase shifter 90° phase shift bit layout considered, and iterated shunt MIM capacitors; S-parameters graphs for practical case (a) return loss for the practical case, and (b) insertion loss for the practical case.

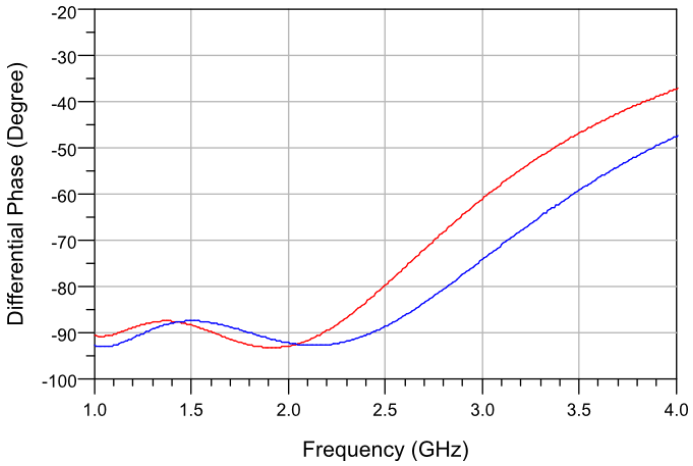


Figure 5-16. The differential phase shift response of 1 to 2 GHz phase shifter 90° phase shift bit layout considered, and iterated shunt MIM capacitors (red line represents the present case, and blue line represents the ideal case).

Table 5-15. Calculated mean phase, minimum phase, rms phase, maximum phase and phase ripple comparison between the ideal case and the finalized layout considerations of 1 to 2 GHz phase shifter 90° phase shift bit.

	Min. Phase (°)	**Rms Phase (°)**	**Max. Phase (°)**	**Ripple (°)**
Ideal	87.551	90.033	93.169	3.155
Present case	87.870	90.245	92.516	2.361

Considering the sizes and the layout view, one should refer to Figure 5-17 for the upper branch of 1 to 2 GHz phase shifter 90° phase shift bit, and for the lower branch refer to Figure 5-18.

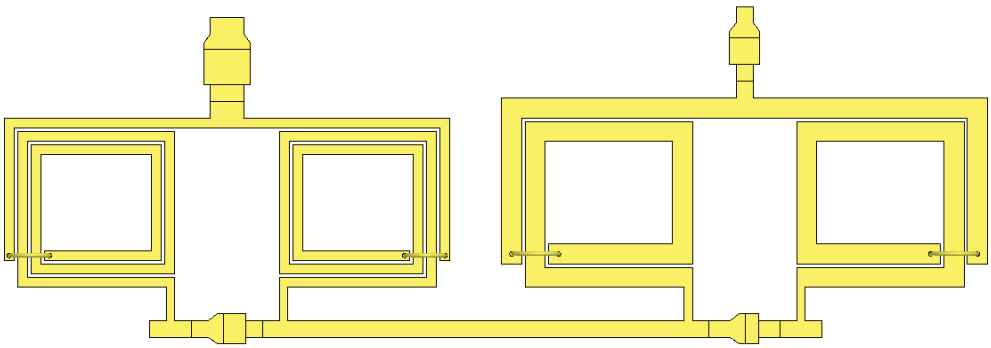


Figure 5-17. Upper branch of 1 to 2 GHz phase shifter 90° phase shift bit (Length: 5.856 mm, Width: 2.026 mm, Separation between inductors: 308 µm).

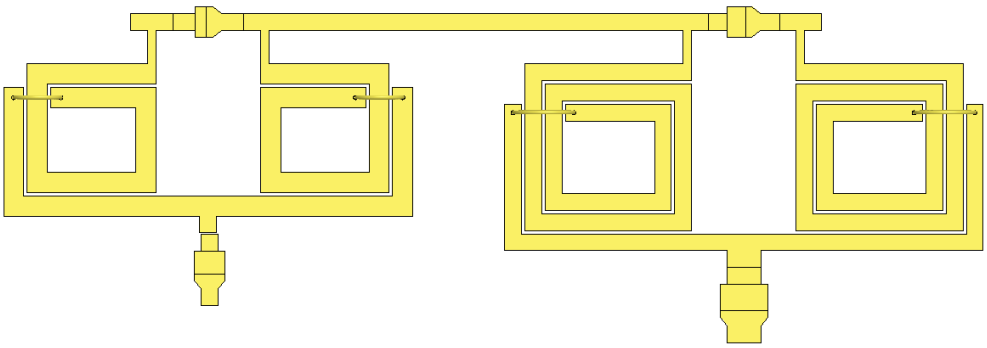


Figure 5-18. Lower branch of 1 to 2 GHz phase shifter 90° phase shift bit (Length: 5.818 mm, Width: 1.998 mm, Separation between inductors: 546 µm).

5.1.3 Design of 45° Phase Shift Bit

Considering the 1 to 2 GHz phase shifter 45° phase shift bit, the final series connected MIM capacitors design related data are given in Table 5-16, the layout considered SPSIs are given in Table 5-17, and the shunt connected MIM capacitors' final designs are given in Table 5-18. The S-parameters comparison graph of the final layout along with the ideal design is given in Figure 5-19; the differential phase shift related graph is given in Figure 5-20, with the phase shift related calculation results as in Table 5-19. It can be seen that these results have return loss around -25.1 dB, insertion loss around 1.64 dB at 1 GHz, in the worst case. The differential phase shift response is satisfactory.

Table 5-16. 1 to 2 GHz phase shifter 45° phase shift bit finalized series connected MIM capacitor design related geometrical parameter values, and the lumped equivalent model parameter values.

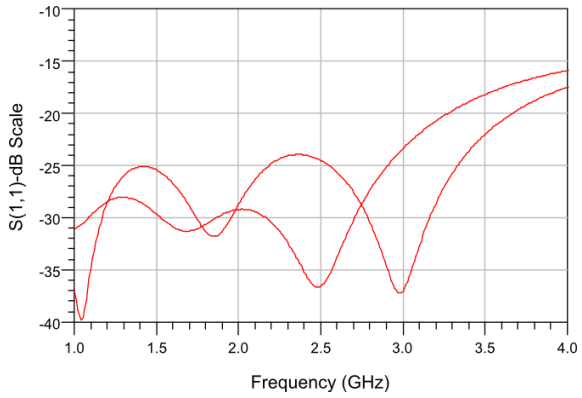
Width (µm)	Length (µm)	L_{feed} (µm)	C (pF)	C_{sh} (fF)	L_s (pH)	R_s (ohm)
100	84	100	1.78	42	384	0.181
100	29	127.5	0.621	42	415	0.255
100	34	125	0.725	42	412	0.258
100	72	106	1.526	42	400	0.222

Table 5-17. The layout designs of selected SPSIs (with extension lengths of 157 µm for 3.17 nH, and 3.71 nH; and 107 µm for 7.6 nH and 8.89 nH).

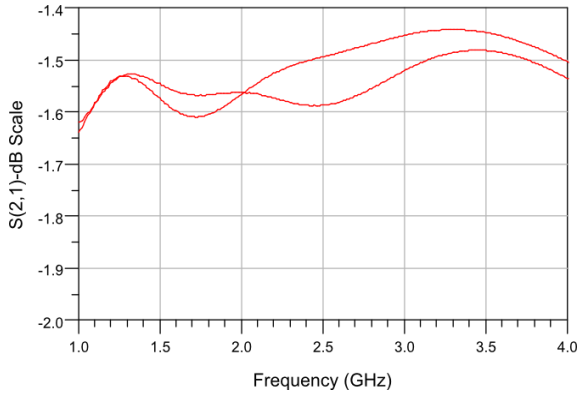
W_{line} (µm)	Spacing (µm)	D_{out} (µm)	L_s (nH)	R_s (ohm)	C_{sh} (fF)	Q_{max}	Q_{ripple}	Q_{min}	Q_{mean}
120	15	946	3.165	0.839	228	61.658	11.029	43.918	54.948
100	15	952	3.736	0.977	221	56.887	9.233	42.245	51.478
80	20	1040	7.611	1.600	277	46.682	3.466	41.627	45.093
60	20	1006	8.885	1.948	254	41.517	3.120	36.737	39.856

Table 5-18. The final design of shunt connected MIM capacitors for 1 to 2 GHz phase shifter 45° phase shift bit.

	(pF)	Width (µm)	Length (µm)	C (pF)	C_{sh} (fF)	L_s (pH)	R_s (ohm)
C2_1	7.11	200	156	6.518	62	317	0.116
C2_2	2.53	100	98	2.066	43	393	0.187
C4_1	2.97	100	118	2.482	45	405	0.189
C4_2	6.08	200	130	5.449	60	306	0.117



(a)



(b)

Figure 5-19. The 1 to 2 GHz phase shifter 45° phase shift bit configuration # 1 layout considered, and iterated shunt MIM capacitors; S-parameters graphs for practical case (a) return loss for the practical case, and (b) insertion loss for the practical case.

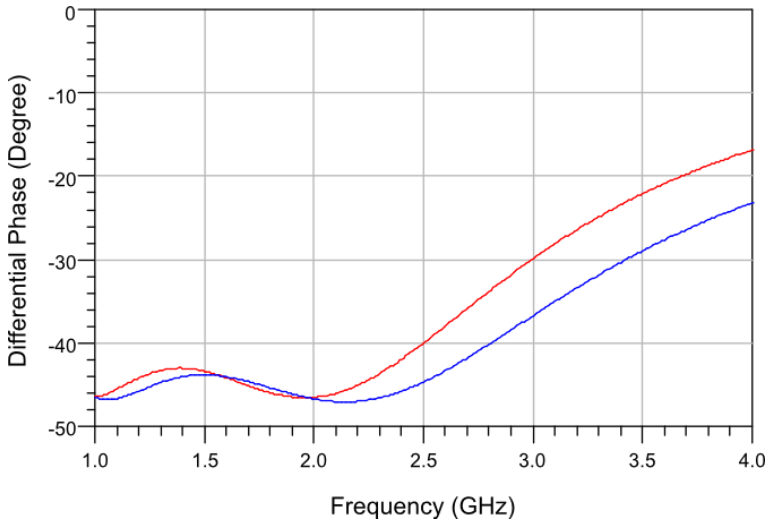


Figure 5-20. The differential phase shift response of 1 to 2 GHz phase shifter 45° phase shift bit configuration # layout considered, and iterated shunt MIM capacitors (red line represents the present case, and blue line represents the ideal case).

Table 5-19. Calculated mean phase, minimum phase, rms phase, maximum phase and phase ripple comparison between the ideal case and the finalized layout considerations of 1 to 2 GHz phase shifter 45° phase shift bit.

	Min. Phase (°)	**Rms Phase (°)**	**Max. Phase (°)**	**Ripple (°)**
Ideal	43.858	45.255	46.835	1.592
Present case	43.370	45.064	46.677	1.679

Considering the sizes and the layout view, one should refer to Figure 5-21 for the upper branch of 1 to 2 GHz phase shifter 45° phase shift bit, and for the lower branch refer to Figure 5-22.

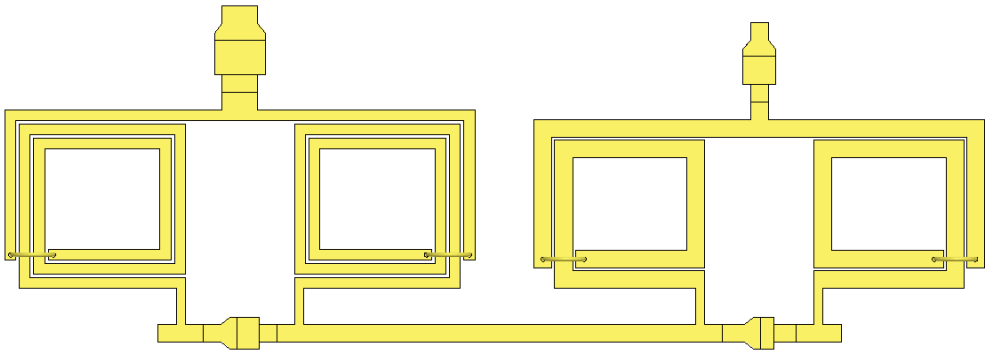


Figure 5-21. Upper branch of 1 to 2 GHz phase shifter 45° phase shift bit (Length: 5.476 mm, Width: 1.932 mm, Separation between inductors: 332 µm).

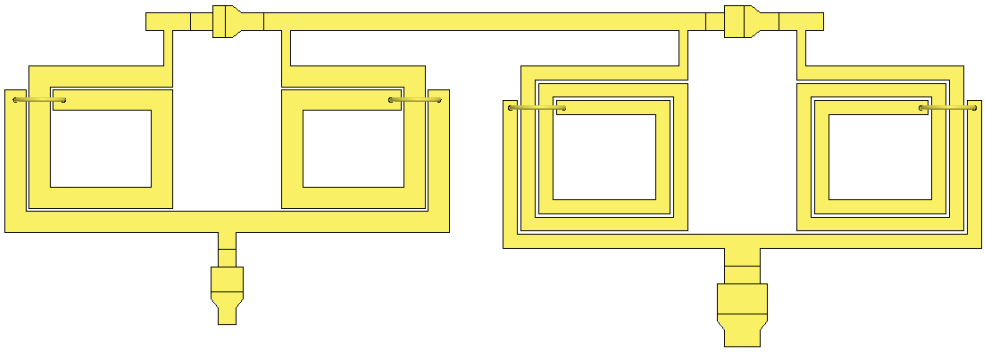


Figure 5-22. Lower branch of 1 to 2 GHz phase shifter 45° phase shift bit (Length: 5.504 mm, Width: 1.94 mm, Separation between inductors: 304 µm).

5.1.4 Design of 22.5° Phase Shift Bit

Considering the 1 to 2 GHz phase shifter 22.5° phase shift bit, the final series connected MIM capacitors design related data are given in Table 5-20, the layout considered SPSIs are given in Table 5-21, and the shunt connected MIM capacitors' final designs are given in Table 5-22. The S-parameters comparison graph of the final layout and the ideal design is given in Figure 5-23; the differential phase shift related graph is given in Figure 5-24, with the phase shift related calculation results as in Table 5-23. It can be observed from these results that return loss is around -18.1 dB; insertion loss is around 1.63 dB at around 1.5 GHz, in the worst case. The differential phase shift response is satisfactory.

Table 5-20. 1 to 2 GHz phase shifter 22.5° phase shift bit finalized series connected MIM capacitor design related geometrical parameter values, and the lumped equivalent model parameter values.

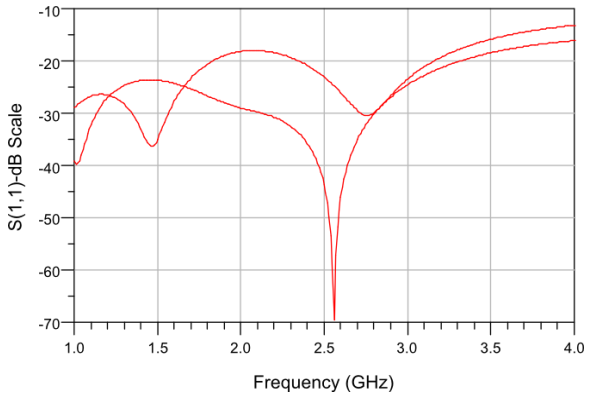
Width (µm)	Length (µm)	L_{feed} (µm)	C (pF)	C_{sh} (fF)	L_s (pH)	R_s (ohm)
100	80	100	1.694	42	383	0.19
100	31	124.5	0.664	41	411	0.259
100	34	123	0.725	41	410	0.25
100	74	103	1.574	42	395	0.221

Table 5-21. The layout designs of selected SPSIs (with extension lengths of 155 µm for 3.31 nH, and 3.58 nH; and 105 µm for 7.87 nH and 8.51 nH).

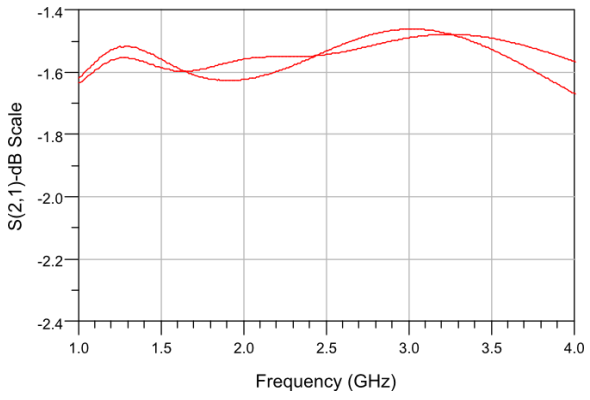
W_{line} (µm)	Spacing (µm)	D_{out} (µm)	L_s (nH)	R_s (ohm)	C_{sh} (fF)	Q_{max}	Q_{ripple}	Q_{min}	Q_{mean}
120	20	990	3.312	0.737	244	64.454	10.761	46.206	56.967
120	20	1048	3.595	0.911	263	58.093	9.142	43.601	52.743
80	20	1068	7.925	1.765	290	43.037	2.632	38.960	41.592
80	20	1136	8.524	1.936	330	42.981	6.340	34.236	40.576

Table 5-22. The final design of shunt connected MIM capacitors for 1 to 2 GHz phase shifter 22.5° phase shift bit.

	(pF)	Width (µm)	Length (µm)	C (pF)	C_{sh} (fF)	L_s (pH)	R_s (ohm)
C2_1	6.81	200	145	6.063	61	314	0.119
C2_2	2.64	100	110	2.323	44	400	0.189
C4_1	2.88	100	109	2.297	44	400	0.191
C4_2	6.28	200	134	5.621	60	307	0.116



(a)



(b)

Figure 5-23. The 1 to 2 GHz phase shifter 22.5° phase shift bit configuration # 1 layout considered, and iterated shunt MIM capacitors; S-parameters graphs for practical case (a) return loss for the practical case, and (b) insertion loss for the practical case.

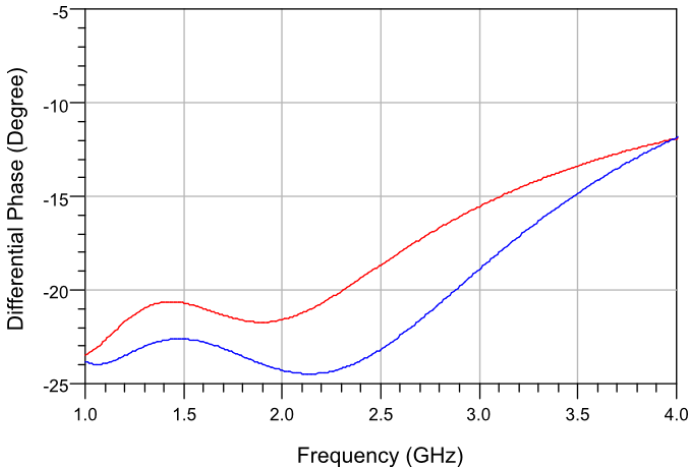


Figure 5-24. The differential phase shift response of 1 to 2 GHz phase shifter 22.5° phase shift bit configuration # layout considered, and iterated shunt MIM capacitors (red line represents the present case, and blue line represents the ideal case).

Table 5-23. Calculated mean phase, minimum phase, rms phase, maximum phase and phase ripple comparison between the ideal case and the finalized layout considerations of 1 to 2 GHz phase shifter 22.5° phase shift bit.

	Min. Phase (°)	**Rms Phase (°)**	**Max. Phase (°)**	**Ripple (°)**
Ideal	22.624	23.351	24.306	0.961
Present case	21.510	22.453	23.810	1.367

Considering the sizes and the layout view, one should refer to Figure 5-21 for the upper branch of 1 to 2 GHz phase shifter 22.5° phase shift bit, and for the lower branch refer to Figure 5-22.

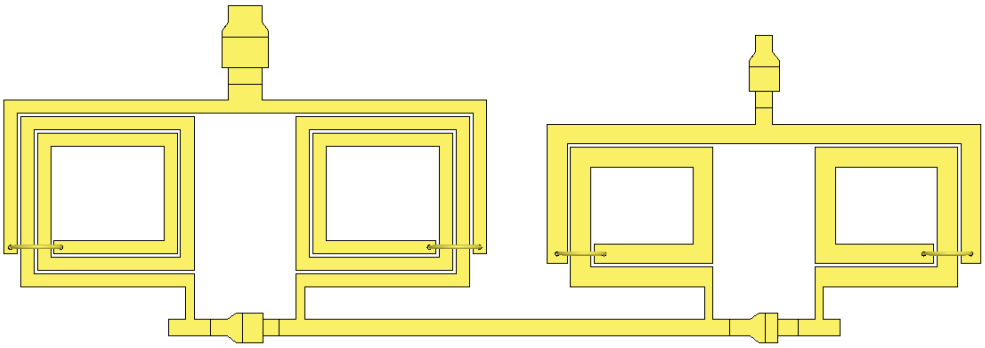


Figure 5-25. Upper branch of 1 to 2 GHz phase shifter 22.5° phase shift bit (Length: 5.836 mm, Width: 2.051 mm, Separation between inductors: 364 µm).

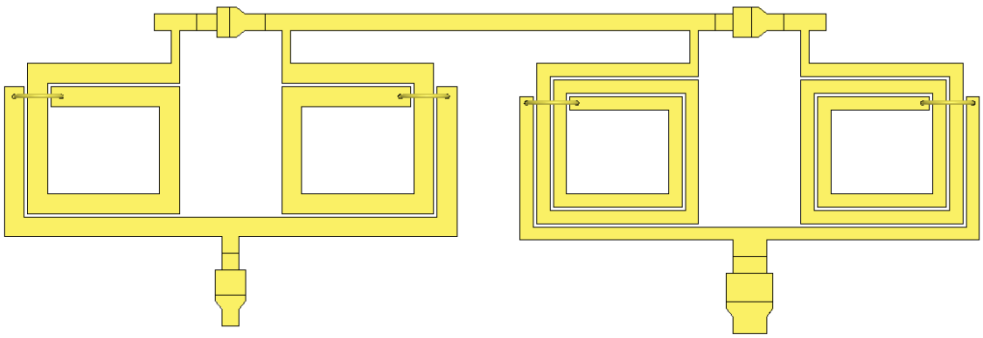


Figure 5-26. Lower branch of 1 to 2 GHz phase shifter 22.5° phase shift bit (Length: 5.826 mm, Width: 1.972 mm, Separation between inductors: 374 µm).

5.1.5 All Phase Bit States of 1 to 2 GHz Phase Shifter

Since the 1 to 2 GHz phase shifter 180°, 90°, 45°, and 22.5° phase shift bit designs are completed the overall phase shifter performance is simulated based on the EM simulations of the components. The SPDT switches are assumed to be static, and the switches are assumed to have 0.5 dB insertion loss (that is total of 4 dB insertion loss of the phase shifters are coming from switches since there are total of 8 switches are needed), 25 dB isolation. The return loss plots for all phase shift bits are given in Figure 5-27. The maximum return loss is around -13 dB. The insertion loss plots for all phase shift states are given in Figure 5-28. The maximum insertion loss is around -7 dB at 1 GHz (4 dB from the switches).

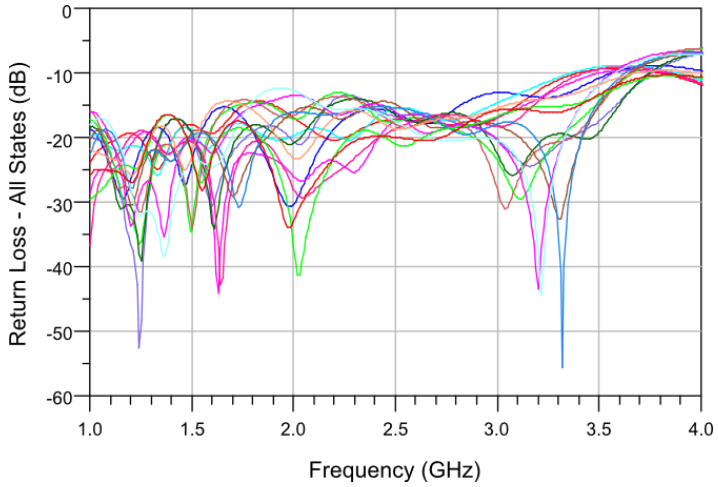


Figure 5-27. The overall performance of 1 to 2 GHz for all 16 phase shift states and the reference state S_{11} plots (Return losses).

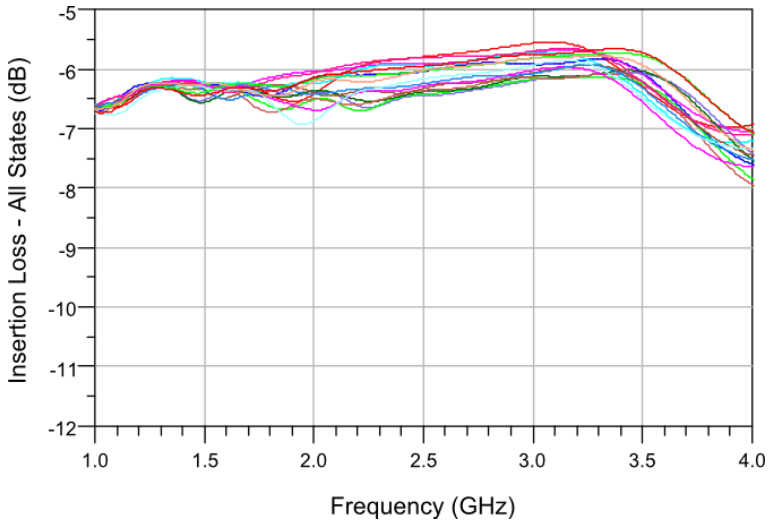


Figure 5-28. The overall performance of 1 to 2 GHz for all 16 phase shift states and the reference state S_{21} plots (Insertion losses).

The overall differential phase shift performance for all phase shift states are given in Figure 5-29. The results are, indeed, satisfactory, as it can be observed from Table 5-24, which is about phase shift related calculations. The design of 1 to 2 GHz phase shifter is complete. The maximum rms phase error could be observed from Figure 5-30, as around 5.8°.

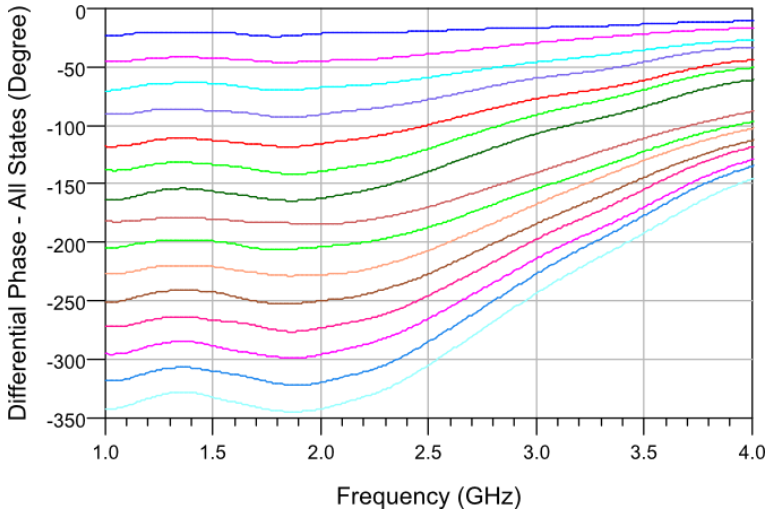


Figure 5-29. The overall differential phase shift performance of 1 to 2 GHz phase shifter for all 15 phase shift states with respect to reference phase shift state.

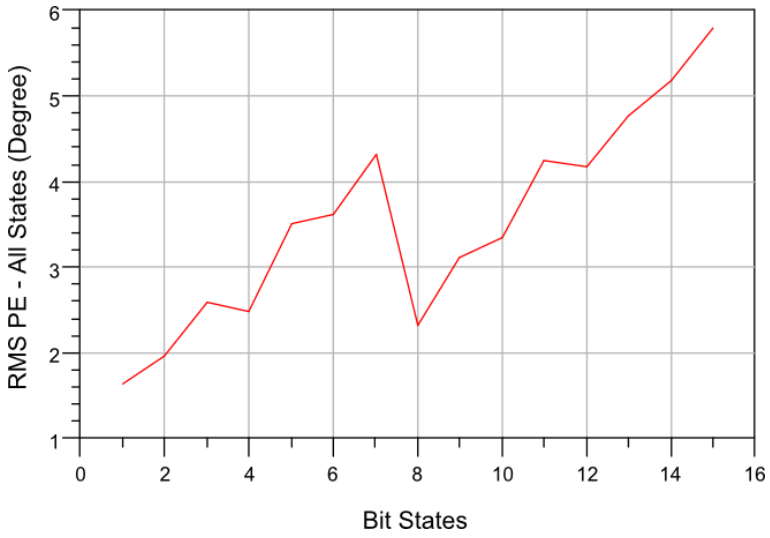


Figure 5-30. Phase rms error graph for bit states of 1 to 2 GHz 4-bit phase shifter.

Table 5-24. Calculated mean phase, minimum phase, rms phase, maximum phase and phase ripple of 1 to 2 GHz phase shifter for all phase shift states.

	Mean Phase	**Min. Phase**	**rms Phase**	**Max. Phase**	**Ripple**
22.50	22.873	21.672	22.895	24.834	1.961
45.00	45.091	43.366	45.108	46.681	1.725
67.50	67.958	65.127	67.991	71.661	3.703
90.00	90.519	87.686	90.542	93.826	3.306
112.50	113.237	108.999	113.266	116.456	4.238
135.00	135.515	131.083	135.549	139.879	4.433
157.50	158.240	152.374	158.282	162.612	5.867
180.00	180.568	178.072	180.577	183.408	2.840
202.50	203.465	199.680	203.483	207.074	3.785
225.00	225.655	221.456	225.675	229.607	4.199
247.50	248.552	243.044	248.583	253.438	5.508
270.00	271.124	265.440	271.151	277.294	6.170
292.50	293.887	286.602	293.920	299.891	7.285
315.00	316.123	308.811	316.160	323.429	7.312
337.50	338.886	329.958	338.931	345.927	8.928

5.2 Design of 4-bit 2 to 4 GHz Broadband Phase Shifter

In the above sub-section, the design procedure of a phase shift bit is detailed for 1 to 2 GHz 180° phase shift bit. Following this design, the brief design of other phase shift bits for 1 to 2 GHz is presented with the geometrical specifications of the used lumped components and necessary dimensions. After that the complete design of phase shifter is presented.

For the sake of simplicity, only the overall design results for 2 to 4 GHz phase shifter are presented. For detailed designs of phase shift bits, please refer to "Appendix A". The used SPDT switches are assumed to have an insertion loss of 0.5 dB over the whole band with an isolation of 25 dB. The return loss plots for all phase shift bits are given in Figure 5-31. The maximum return loss is around -15 dB. The insertion loss plots for all phase shift states are given in Figure 5-32. The maximum insertion loss is around -7.9 dB at 4 GHz.

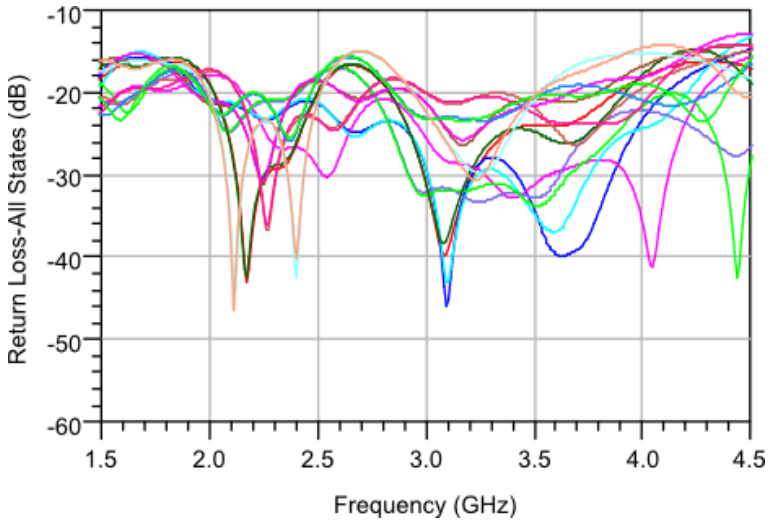


Figure 5-31. The overall performance of 2 to 4 GHz for all 16 phase shift states and the reference state S_{11} plots (Return losses).

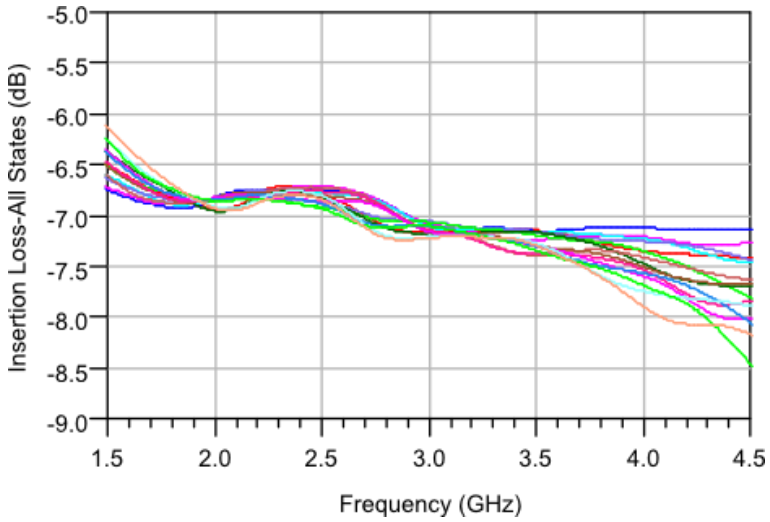


Figure 5-32. The overall performance of 2 to 4 GHz for all 16 phase shift states and the reference state S_{21} plots (Insertion losses).

The overall differential phase shift performance for all phase shift states are given in Figure 5-33. The results are, indeed, satisfactory, as it can be observed from

Table 5-25, which is about phase shift related calculations. The design of 2 to 4 GHz phase shifter is complete. The maximum rms phase error could be observed from Figure 5-34, as around 7.35°.

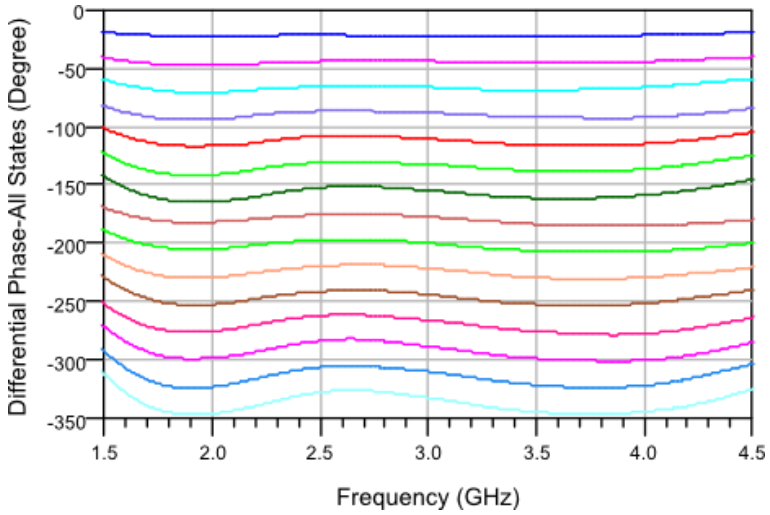


Figure 5-33. The overall differential phase shift performance of 2 to 4 GHz phase shifter for all 15 phase shift states with respect to reference phase shift state.

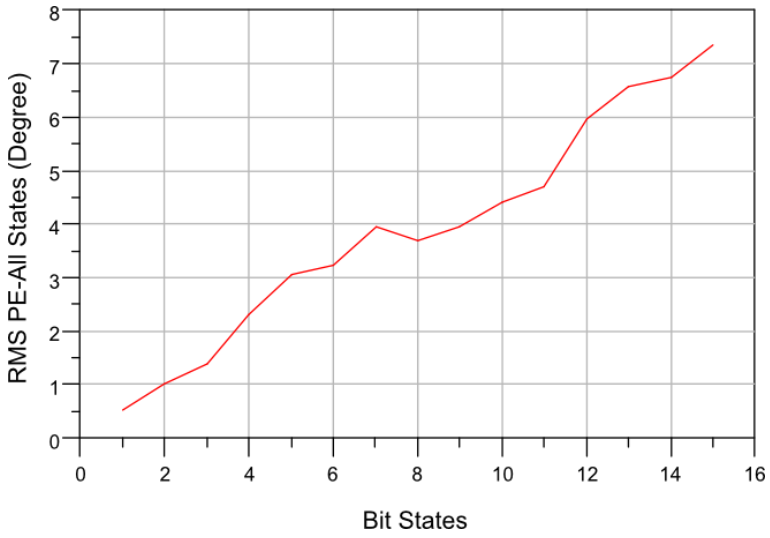


Figure 5-34. Phase rms error graph for bit states of 2 to 4 GHz 4-bit phase shifter.

Table 5-25. Calculated mean phase, minimum phase, rms phase, maximum phase and phase ripple of 2 to 4 GHz phase shifter for all phase shift states.

	Mean Phase	**Min. Phase**	**rms Phase**	**Max. Phase**	**Ripple**
22.50	22.581	21.408	22.588	23.789	1.209
45.00	44.784	43.459	44.797	47.732	2.948
67.50	67.373	65.238	67.387	71.364	3.991
90.00	89.973	86.854	89.998	94.076	4.103
112.50	112.620	108.107	112.651	117.345	4.725
135.00	134.779	130.656	134.810	141.794	7.015
157.50	157.419	151.997	157.458	165.180	7.761
180.00	180.104	174.545	180.152	186.135	6.032
202.50	202.659	196.813	202.704	208.304	5.846
225.00	224.888	218.010	224.936	230.956	6.877
247.50	247.457	240.259	247.503	253.465	7.198
270.00	270.083	261.324	270.153	278.522	8.760
292.50	292.702	282.533	292.775	301.168	10.169
315.00	314.889	305.326	314.960	323.671	9.563
337.50	337.496	326.532	337.570	346.331	10.964

5.3 Design of 4-bit 3 to 6 GHz Broadband Phase Shifter

Like the same for 2 to 4 GHz phase shifter section, for the sake of simplicity, only the overall design results for 3 to 6 GHz phase shifter are presented. For detailed designs

of phase shift bits, please refer to "Appendix B". The SPDT switches are assumed to have an insertion loss of 0.5 dB over the whole band with an isolation of 25 dB.

The return loss plots for all phase shift bits are given in Figure 5-35. The maximum return loss is around -12 dB. The insertion loss plots for all phase shift states are given in Figure 5-36. The maximum insertion loss is around -10.4 dB at 6 GHz.

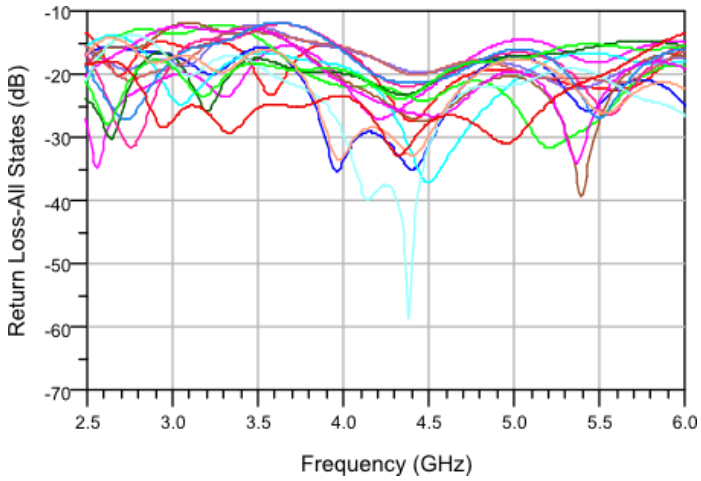


Figure 5-35. The overall performance of 3 to 6 GHz for all 16 phase shift states and the reference state S_{11} plots (Return losses).

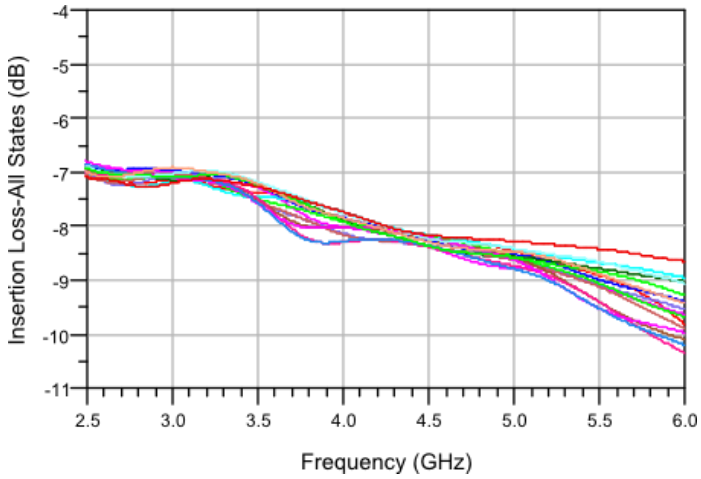


Figure 5-36. The overall performance of 3 to 6 GHz for all 16 phase shift states and the reference state S_{21} plots (Insertion losses).

The overall differential phase shift performance for all phase shift states of 3 to 6 GHz phase shifter are given in Figure 5-37. The results are, indeed, satisfactory, as it can be observed from Table 5-26, which is about phase shift related calculations. Maximum rms phase error could be observed from Figure 5-38, as around 7°.

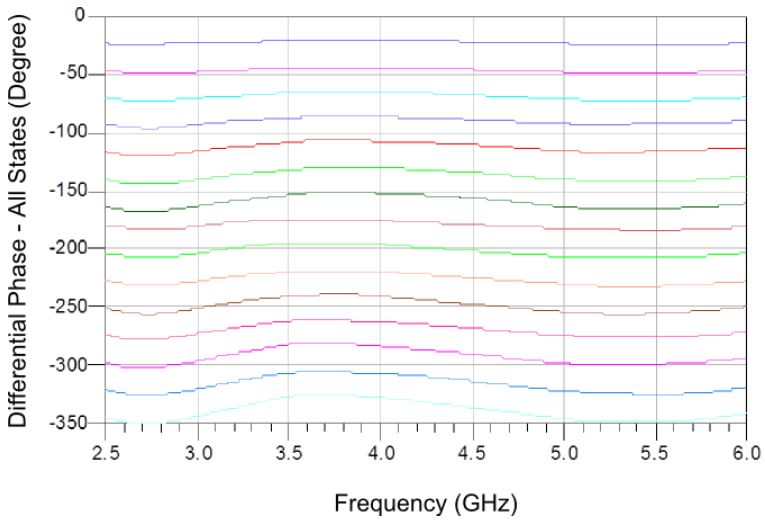


Figure 5-37. The overall differential phase shift performance of 3 to 6 GHz phase shifter for all 15 phase shift states with respect to reference phase shift state.

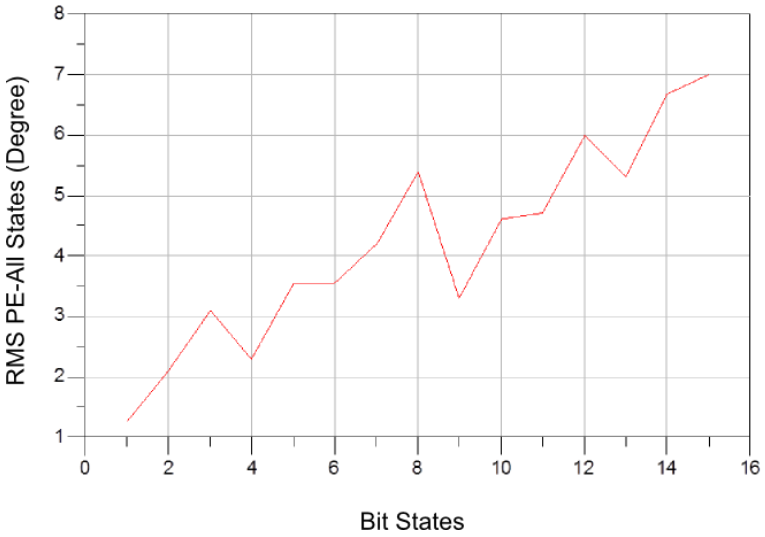


Figure 5-38. Phase rms error graph for bit states of 3 to 6 GHz 4-bit phase shifter.

Table 5-26. Calculated mean phase, minimum phase, rms phase, maximum phase and phase ripple of 3 to 6 GHz phase shifter for all phase shift states.

	Mean Phase	**Min. Phase**	**rms Phase**	**Max. Phase**	**Ripple**
22.50	22.381	20.524	22.416	23.970	1.857
45.00	46.376	44.024	46.403	48.693	2.351
67.50	68.748	64.492	68.806	72.780	4.256
90.00	89.673	86.104	89.702	92.989	3.569
112.50	112.034	106.273	112.089	116.925	5.761
135.00	136.328	130.470	136.386	141.522	5.858
157.50	158.695	150.655	158.782	165.784	8.041
180.00	179.233	174.860	179.262	183.652	4.418
202.50	201.594	194.882	201.644	207.353	6.712
225.00	225.586	218.795	225.634	232.046	6.790
247.50	247.939	238.835	248.012	255.991	9.104
270.00	268.836	260.365	268.886	275.140	8.471
292.50	291.182	280.055	291.255	299.539	11.127
315.00	315.515	304.985	315.593	324.840	10.530
337.50	337.865	324.639	337.967	348.567	13.226

5.4 Design of 11.25° and 5.625° phase shift bits for 3 to 6 GHz Phase Shifter

Higher resolution for digital phase shifters is always desired. For that reason, 5.625° and 11.25° phase shift bits for 3 to 6 GHz band are designed with a novel approach to broadband all-pass network phase shifters.

If one desires to implement the 5.625° and 11.25° phase shift bits with the method as described above; one must use twice the two-stage all-pass network components for this case in addition to 4 SPDT switches. In total 12 SPDT switches must be used, and this results in 6 dB additional insertion loss to the circuit. Using the results described above for 3 to 6 GHz 4-bit phase shifter, with a rough calculation, 15 dB insertion loss is presented by 6-bit design. The cost of the circuit, the design time, and size are also increased with the conventional method.

The new method proposes an SPDT-less phase shifter. Using only two stages, one could implement 5.625° and 11.25° bits. The schematic of the circuit is given in Figure

5-39. Series connected capacitors and inductors have fixed values. In addition to that, shunt connected capacitors are realized in three states to achieve phase shifting of 5.625° and 11.25° just with one circuit. One of these three capacitors is used for the reference state, while the other two are employed to achieve the phase shifts.

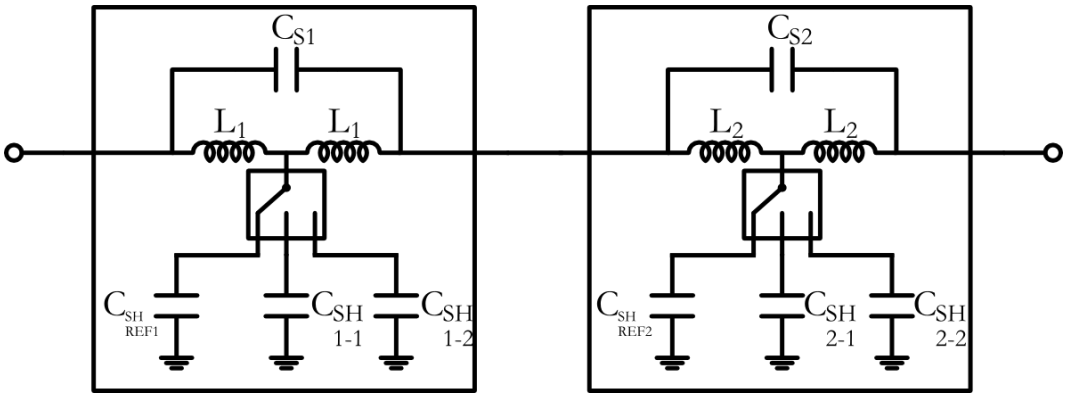


Figure 5-39. Novel 2 bit SPDT-less all-pass network phase shifter.

Before going into details of this method, the ideal design results of conventional method for the two bits are presented.

Using the two design parameters found in Chapter 3 for bit-5 and bit-6, and choosing a proper center frequency, ideal lumped element values for 3 to 6 GHz frequency band are calculated as listed in Table 5-27.

Table 5-27. The resultant lumped element values for 3 to 6 GHz phase shifter for 5.625° and 11.25° phase shift bits (Inductance in nH, capacitance in pF).

5.625° Phase Shift Bit				**11.25° Phase Shift Bit**			
L_1= 2.73	L_2= 1.29	L_3= 1.31	L_4= 2.68	L_1= 2.78	L_2= 1.13	L_3= 1.17	L_4= 2.67
C_{11}= 0.546	C_{12}= 0.258	C_{31}= 0.263	C_{32}= 0.537	C_{11}= 0.555	C_{12}= 0.225	C_{31}= 0.234	C_{32}= 0.534
C_{21}= 2.185	C_{22}= 1.032	C_{41}= 1.051	C_{42}= 2.146	C_{21}= 2.221	C_{22}= 0.901	C_{41}= 0.937	C_{42}= 2.137

The ideal phase shift responses of the two phase shift bits are given in Figure 5-40. The phase responses have satisfactory performance. Phase related calculations are given in Table 5-28. The return loss and insertion loss plots are not given since the all-pass networks are inherently matched with this method, and the components are ideal.

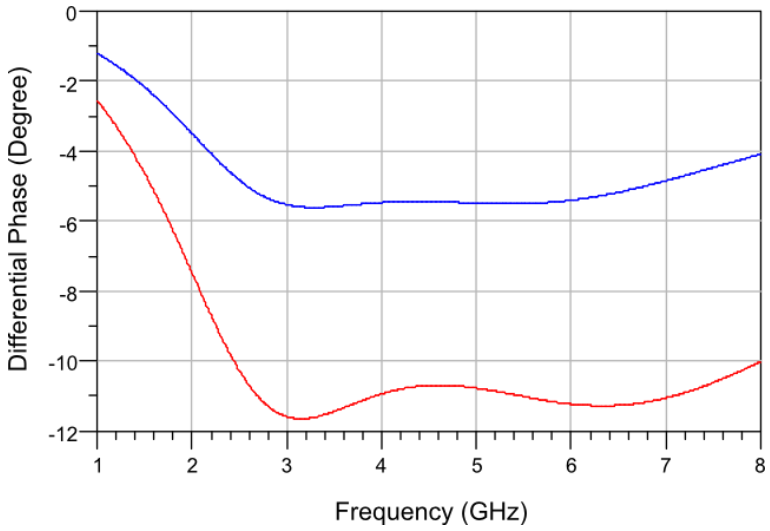


Figure 5-40. Ideal phase responses of 5.625° (blue line), and 11.25° (red line) phase shift bits constructed with ideal lumped elements for 3 to 6 GHz phase shifter.

Table 5-28. Differential phase shift related data bit-5 and bit-6, for 3 to 6 GHz phase shifter.

Bit	Mean Phase (°)	Maximum Phase Error (°)	Rms Phase Error (°)
5.625°	5.50	0.11	0.06
11.25°	11.05	0.60	0.31

The above results are given in order to compare the new circuit with the conventional one. From now on, the new circuit is described. Referring to Figure 5-39, $C_{SH\text{-}REF1}$, and $C_{SH\text{-}REF2}$ are the one state of the shunt capacitors, which are related to the reference state. $C_{SH1\text{-}1}$ is the shunt capacitor for the first all-pass filter for the state of 5.625° phase shift bit, and $C_{SH2\text{-}1}$ is the shunt capacitor for the second all-pass filter for the state of 5.625° phase shift bit. Similarly, $C_{SH1\text{-}2}$ is the shunt capacitor for the first all-pass filter for the state of 11.25° phase shift bit, and $C_{SH2\text{-}2}$ is the shunt capacitor for the second all-pass filter for the state of 11.25° phase shift bit. All other components are fixed at a proper value. L_1 is equated to 2.78 nH, L_2 is equated 1.13 nH, C_{S1} =0.555 pF, and C_{S2} =0.225 pF. Since these values are fixed, the only switched elements are the shunt capacitors. The values of the above mentioned capacitor values are found as $C_{SH\text{-}REF1}$=2.084 pF, $C_{SH\text{-}REF2}$=0.872 pF, $C_{SH\text{-}11}$=2.214 pF, $C_{SH\text{-}21}$=0.951 pF, $C_{SH\text{-}12}$=2.329 pF, and finally $C_{SH\text{-}22}$=1.043 pF. The ideal lumped element simulations are done and the results are obtained.

Note that since the inherently matched nature of the structure is not valid in this case, the return loss and insertion loss graphs are also given. Return loss graphs are given in Figure 5-41. Maximum return losses for the reference state is 25 dB at around 2.7 GHz, 25 dB at around 6 GHz for 5.625° phase shift bit, and around 17 dB at 5.8 GHz for 11.25° phase shift bit, respectively. Insertion loss graphs are given in Figure 5-42. Note that the insertion loss values are low; however they are not "0 dB", a behavior caused by the non-ideal filter characteristics. Differential phase shift performance for two states given in Figure 5-43 is noted to be satisfactory.

The phase related calculations are given in Table 5-29. One can observe a little degradation in maximum phase error and rms phase error up on comparing the resultant values with the conventional method's results (Table 5-28).

To completely design this phase shifter, EM simulations and model extractions are done for all lumped element values presented for this combined phase shifter.

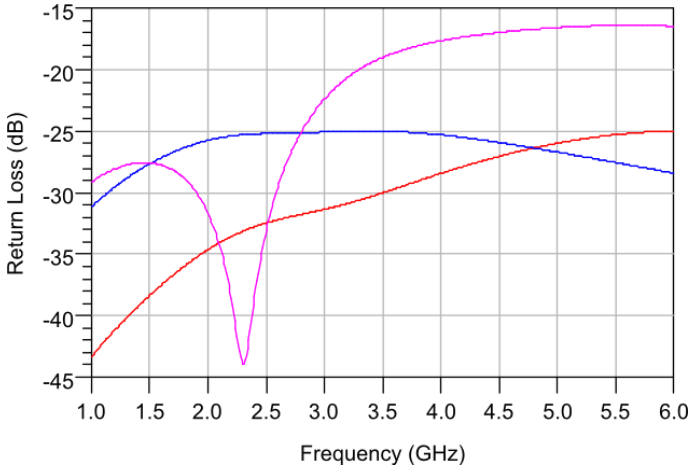


Figure 5-41. Return loss graphs of 5.625° and 11.25° phase shifter constructed with ideal elements; reference state (blue line), 5.625° phase shift state (red line), and 11.25° phase shift state (pink line).

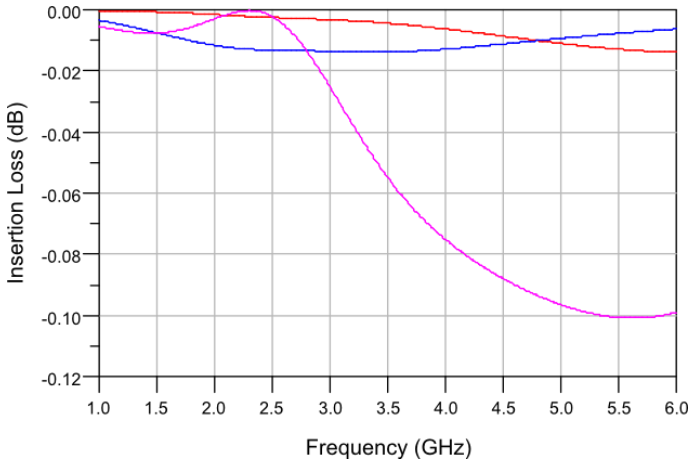


Figure 5-42. Insertion loss graphs of 5.625° and 11.25° phase shifter constructed with ideal elements; reference state (blue line), 5.625° phase shift state (red line), and 11.25° phase shift state (pink line).

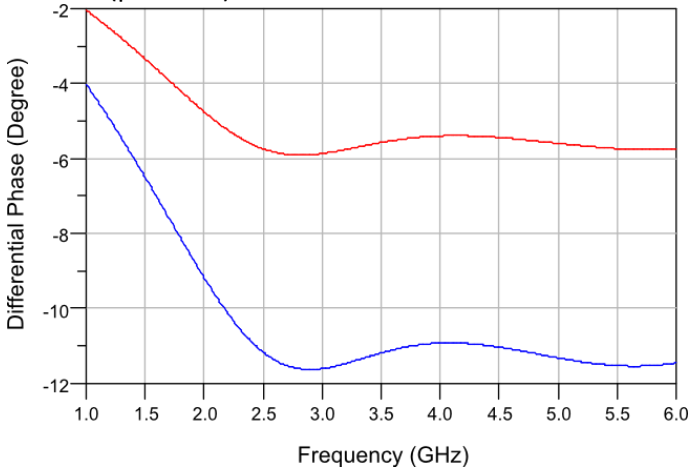


Figure 5-43. Differential phase graphs of 5.625° phase shift state (red line), and 11.25° phase shift state (blue line) constructed with ideal elements.

Table 5-29. Differential phase shift related data for combined phase shift bits, for 3 to 6 GHz phase shifter.

Bit	Mean Phase (°)	Maximum Phase Error (°)	Rms Phase Error (°)
5.625°	5.60	0.28	0.14
11.25°	11.27	0.35	0.23

The resultant geometrical specifications for the employed lumped components are given as follows; the series connected fixed capacitors are given with their lumped equivalent model parameters in Table 5-30, the layout considered SPSIs are given with their lumped equivalent model parameters in Table 5-31, and the switched

shunt connected capacitors are given with their lumped equivalent model parameters in Table 5-32.

Note that the branches, i.e., the reference branch, 5.625° phase shift branch, and 11.25° phase shift branch are practically designed considering the capacitors as frozen. No varactors, or tunable MEMS capacitors are assumed, this overall practical implementation is done to prove the concept.

The finalized layouts of this combined phase shifter are EM simulated and the results are obtained.

Table 5-30. 3 to 6 GHz phase shifter 5.625° and 11.25° combined phase shifter finalized series connected MIM capacitor design related geometrical parameter values, and the lumped equivalent model parameter values.

Width (μm)	**Length (μm)**	**L_{feed} (μm)**	**C (pF)**	**C_{sh} (fF)**	**L_s (pH)**	**R_s (ohm)**
100	26	100	0.559	38	363	0.190
100	10	108	0.227	38	392	0.291

Table 5-31. The layout designs of selected SPSIs for the combined phase shifter (with extension lengths of 128 μm).

W_{line} (μm)	**Spacing (μm)**	**D_{out} (μm)**	**L_s (nH)**	**R_s (ohm)**	**C_{sh} (fF)**	**Q_{max}**	**Q_{ripple}**	**Q_{min}**	**Q_{mean}**
80	20	718	2.773	0.954	143	46.89	13.46	26.27	39.73
120	20	568	1.136	0.692	104	36.64	2.17	33.71	35.88

Table 5-32. The final design of shunt connected MIM capacitors for 3 to 6 GHz combined phase shifter of 5.625° and 11.25° phase shift bits.

	(pF)	**Width (μm)**	**Length (μm)**	**C (pF)**	**C_{sh} (fF)**	**L_s (pH)**	**R_s (ohm)**
$C_{SH\text{-}REF1}$	2.084	100	99	2.087	43	394	0.190
$C_{SH\text{-}REF2}$	0.872	100	40	0.850	39	368	0.182
$C_{SH\text{-}11}$	2.214	100	104	2.193	44	396	0.184
$C_{SH\text{-}21}$	0.951	100	44	0.943	39	366	0.179
$C_{SH\text{-}12}$	2.329	100	107	2.253	44	399	0.191
$C_{SH\text{-}22}$	1.043	100	49	1.044	40	369	0.173

Return loss for the practical implementation can be observed from Figure 5-44. Insertion loss graphs for the practical implementation can be found in Figure 5-45. The reference state has a maximum return loss value of 12.1 dB and maximum insertion loss value of 1.55 dB. The 5.625° phase shift state has a maximum return

loss value of 10 dB and maximum insertion loss value of 1.79 dB. The 11.25° phase shift state has a maximum return loss value of 8.2 dB and maximum insertion loss value of 2.15 dB. Note that the return loss values are low compared to the above designs, however these values can still be considered as satisfactory values according to the needs. On the other hand, insertion losses are comparable to that of the conventional design. In return, it is the most important advantage of this combined phase shifter method, since there are no SPDTs and phase shifter bit number is decreased by one. With a rough calculation, the insertion loss caused by these two phase shift bits is decreased from around 5 dB to 2.15 dB max.

The differential phase graphs are presented in Figure 5-46, and the differential phase related data are provided in Table 5-33. The maximum phase errors and rms phase errors are low; there is no high degradation in the phase response. However, they are higher than the ideal implementation of the new method (Table 5-29), and the ideal implementation of the conventional method (Table 5-28).

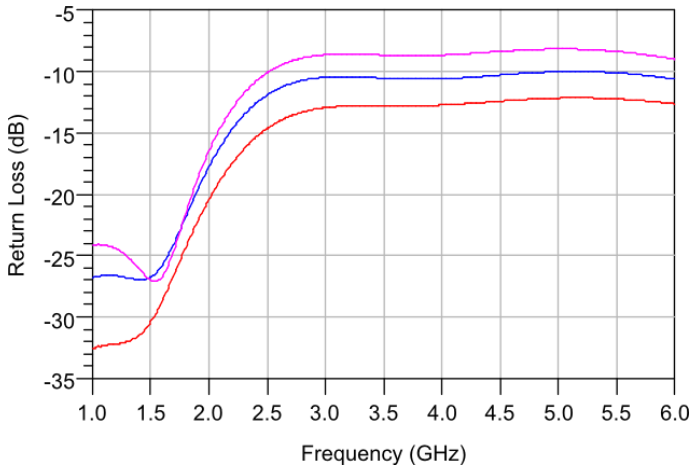


Figure 5-44. Return loss graphs of 5.625° and 11.25° practically constructed phase shifter; reference state (blue line), 5.625° phase shift state (red line), and 11.25° phase shift state (pink line).

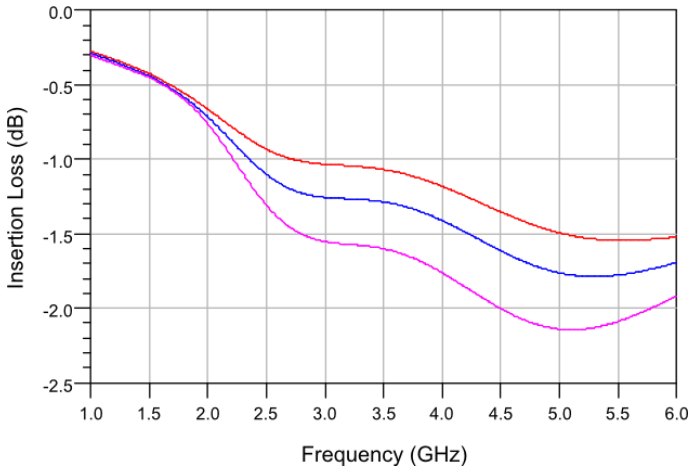


Figure 5-45. Insertion loss graphs of 5.625° and 11.25° practically constructed phase shifter; reference state (blue line), 5.625° phase shift state (red line), and 11.25° phase shift state (pink line).

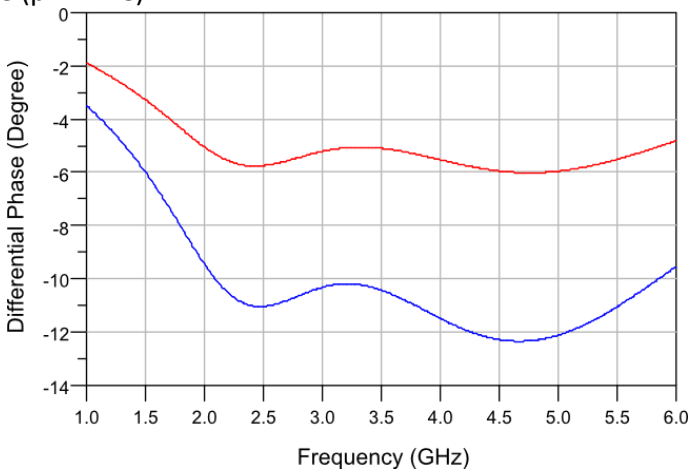


Figure 5-46. Differential phase graphs of 5.625° phase shift state (red line), and 11.25° phase shift state (blue line) of the practically constructed phase shifter.

Table 5-33. Differential phase shift related data for combined phase shift bits, for 3 to 6 GHz phase shifter.

Bit	Mean Phase (°)	Maximum Phase Error (°)	Rms Phase Error (°)
5.625°	5.83	0.88	0.36
11.25°	11.26	1.68	0.83

This new implementation method has several advantages and disadvantages. The advantages of this method can be listed as;

- The design is SPDT-less, hence the insertion loss is decreased by 2 dB, circuit size is decreased, and cost is decreased.

- The employed two-stage all-pass network phase shift bit is decreased by one, which means the total branch number is decreased by three, and hence, the circuit size is decreased, total insertion loss is decreased, design time of lumped elements is considerably decreased, and fabrication cost is decreased.
- Resolution of the phase shifter is increased.

The disadvantages can be listed as;

- The inherently matched nature of the all-pass network is not valid anymore. The return loss may be a problem for some applications.
- The differential phase performance is slightly degraded. This may be a problem for desired precise phase shifters and some applications.

The switched shunt MIM capacitors can be realized with varactors, tunable MEMS capacitors, or with MEMS bridge arrays with proper design.

5.5 Design of Three-Stage 4-bit UWB 1 to 6 GHz Phase Shifter

The ideal design procedure of this phase shifter is already described in Chapter 3 Section 4. Moreover, the calculated ideal lumped element values are presented in the same chapter last section.

To achieve a practical design of this phase shifter, same procedure as described above, is done. For the sake of simplicity, the details of the design procedure are not given in here. A comparison between the phase characteristics of ideal design and the practical design is given in Figure 5-47, and the overall phase shifter performance of all bit states is given in Figure 5-48. A detailed error analysis is done for this phase shifter, and provided in Figure 5-49.

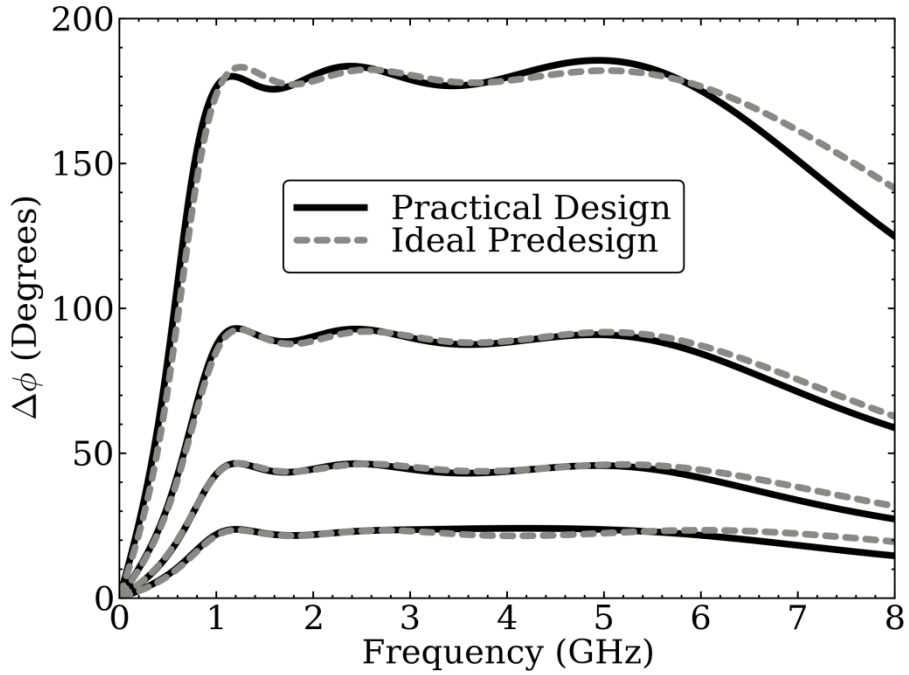


Figure 5-47. A comparison of the single-bit differential phase responses between the ideal UWB phase shifter design (using ideal elements) and the practical design (using surface micromachined lumped elements).

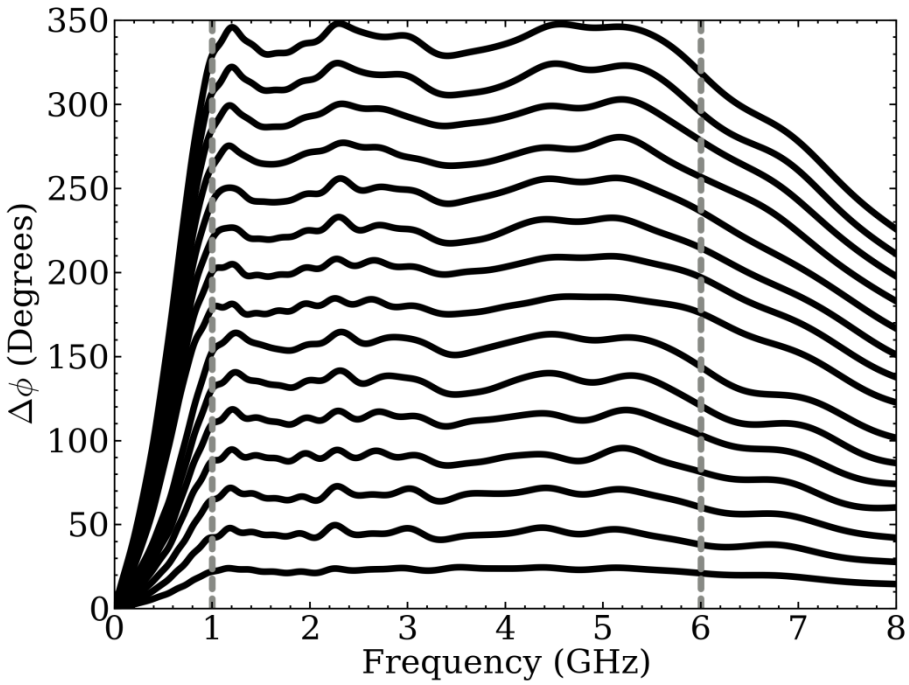


Figure 5-48. Simulated phase performance of the practical UWB phase shifter for all bit states.

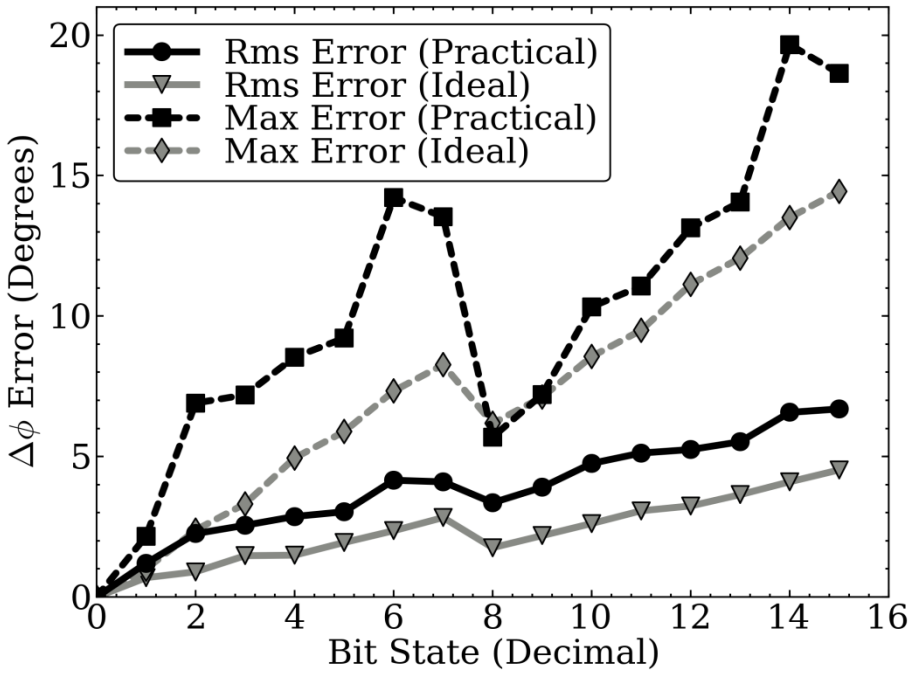


Figure 5-49. rms phase error, and maximum phase error analysis of all bit states for 1 to 6 GHz phase shifter.

The results of the practical phase shifter are promising in terms of its UWB phase shift performance, with a worst case rms phase error of 6.9° for 315° phase shift state. The return loss is nominally -10 dB over the 1-6 GHz band with the worst case value of -8 dB for all possible bit states. In addition, the insertion loss is found to be nominally 5.5 dB with a worst case value of 7.4 dB (with ideal SPDT switches).

In the next chapter, the fabrication and measurements of the designed phase shifters are presented.

CHAPTER 6

FABRICATION AND MEASUREMENTS OF BROADBAND PHASE SHIFTERS

Remember that the practical designs of phase shifters are introduced in the previous chapter. The last step of the realization procedure is the fabrication of the designed structures and measurements.

For this reason, in order to check the validity of the phase shifter designs, 1 to 2 GHz, 2 to 4 GHz, and 3 to 6 GHz; 22.5°, 45°, 90°, and 180° phase shift bits are fabricated in three different layouts:

1. The designed layouts given in Chapter-5, in addition with a ground plane connected to shunt connected MIM capacitors. For measurement purposes additional microstrip lines are added to input and output ports, and CPW-to-microstrip transitions are added at the end of these additional microstrip lines. These additional lines are then de-embedded after measurements. The details are given in the next sub-section.
2. Remember that the overall phase shifter design is a hybrid one, i.e., the SPDT semiconductor switches are added after the surface micromachining fabrication. Since the SPDTs are semiconductor and commercial ones, in general, do not have DC protection, DC blocking capacitors are needed at the common RF port, and the output ports of these switches.

   A simple idea as adding a DC blocking capacitor between the two all-pass filters for each upper and lower branches, not only decreases the needed DC

blocking capacitors by half, it also helps to decrease the return loss. Moreover, the cost is also decreased.

For measurement purposes, additional microstrip lines are added, and CPW-to-microstrip transitions are also added, as in case 1. These additional lines and transitions are de-embedded after measurements are done. The details are given in the next sub-section.

3. The last layout version is the microstrip ended ports of case 2, for hybrid integration with SPDT switches.

After the layouts are briefly discussed, a simple discussion about the fabrication is given. Finally, the measurement results are provided in comparison with practical design results.

6.1 Layout Considerations and Fabrication of Phase Shifters

The three fabricated layouts are briefly discussed above. An example of the second case is given in Figure 6-1. In this case a DC blocking capacitor is added between the two all-pass filters in the same branch, i.e., upper or lower branches. The advantages of adding the DC blocking capacitor in the surface micromachining fabrication are;

- Decreasing the cost of the overall implementation
- Decreasing the implementation time, when combining the SPDT switches and phase shifter structures.
- Decreasing the return loss of the upper and lower branches.
- In some cases the differential phase characteristics are better compared to the without DC blocking capacitor cases.

Note that case 1 can be understood from Figure 6-1 considering the layout without the DC blocking capacitors. Instead a microstrip line can be assumed. The third case is the microstrip ended structures in Figure 6-1.

The designed DC blocking capacitors are constructed with the same idea of the capacitors used in the phase shifters. However, they have larger capacitance values,

with a minimum value of around 24 pF. The designed DC blocking capacitors have; overlap width of 300 μm, overlap length of 400 μm (24 pF), overlap width of 300 μm, overlap length 500 μm (30.5 pF), and overlap width of 300 μm, overlap length of 600 μm (37 pF). These DC blocking capacitors are connected in series between the two all-pass filters of the upper and lower branches of the phase shift bits.

According to these three different layouts of each phase shift bit, i.e., total of 36 different layouts, are formed as a mask set. The mask set of the phase shifters are given in Figure 6-2.

The overall fabrication process consists of generally four steps:

At first, the wafers are Ti/Au (20 nm/1 μm) sputtered from both sides. One of the sides is the ground plane, the other one is then etched as a second step to obtain the base metal in which the inductors, transmission lines and base of MIM capacitors are formed. As a third step, polyimide is coated to protect the base metal and then UV photolithography step is done to form the second metallization openings. Then 1.2 μm gold is sputtered and etched for the second metallization. Finally polyimide is released, and the wafer is diced.

After the dicing is completed, the dies must be prepared for measurements. Note that the measurements cannot be done on wafer, since the phase shifters are formed as microstrip based structures. For that reason, post-processing is required to measure on a CPW probe station.

To measure the devices, dies are silver-epoxy bonded to a holder wafer with gold sputtered as ground plane. This must be done to prepare the devices for CPW probe station measurements. Finally wire-bonds are done for two specific reasons as; to connect the inner and outer traces of the inductors and to connect the ground of the CPW and ground sections below the shunt connected capacitances of the base metallization to the global ground which is the holder wafer metallization. Figure 6-3 represents the fabricated and post-processed 2 to 4 GHz 22.5° phase shift bit.

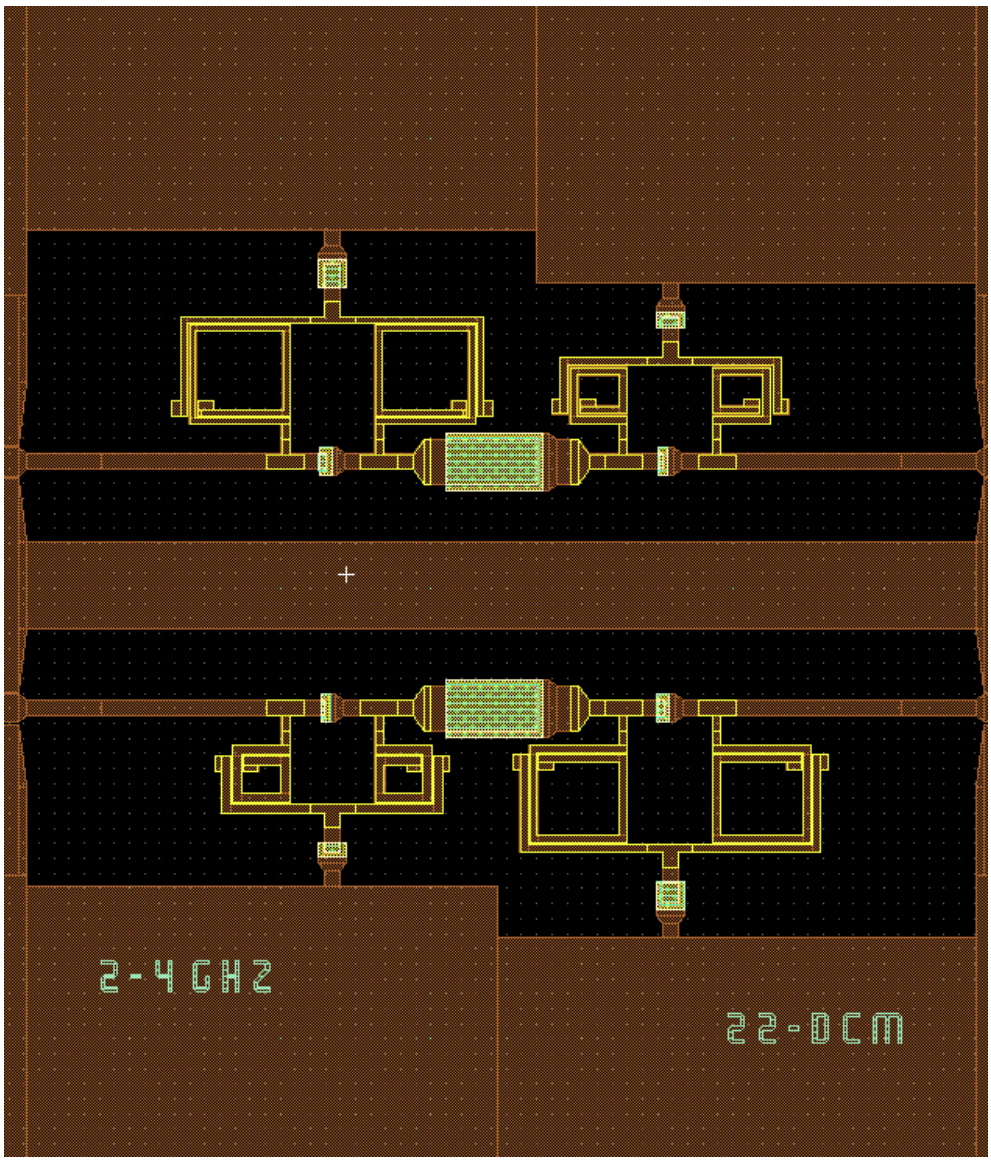


Figure 6-1. An example phase shift bit layout with DC blocking capacitor between the two all-pass filters for each upper and lower branches.

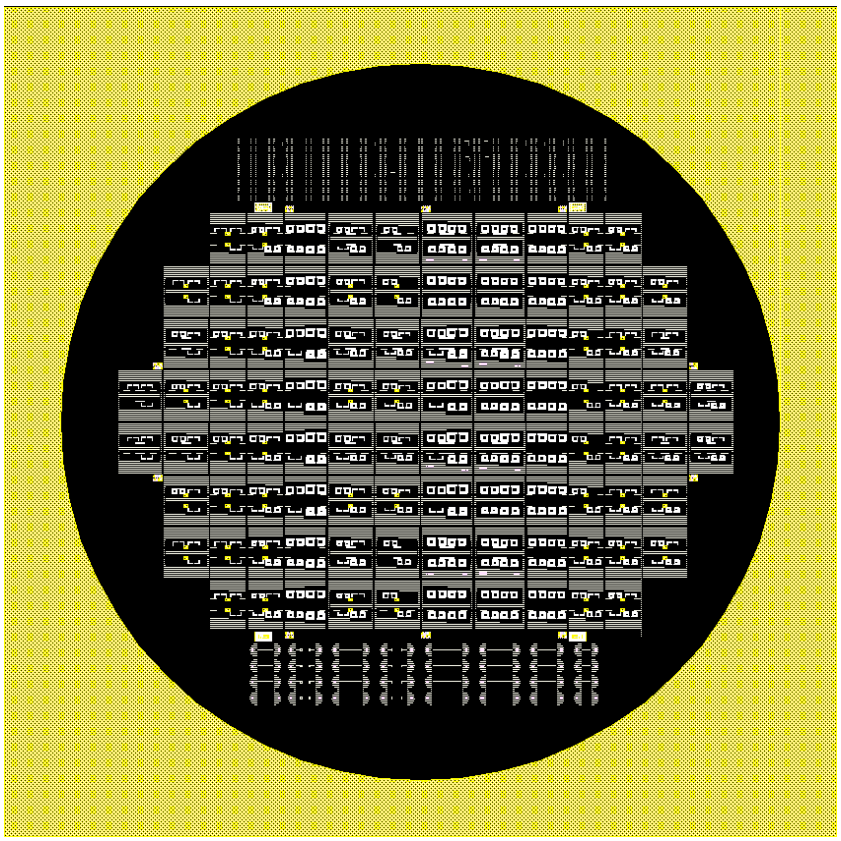


Figure 6-2. Mask Set of Phase Shifters.

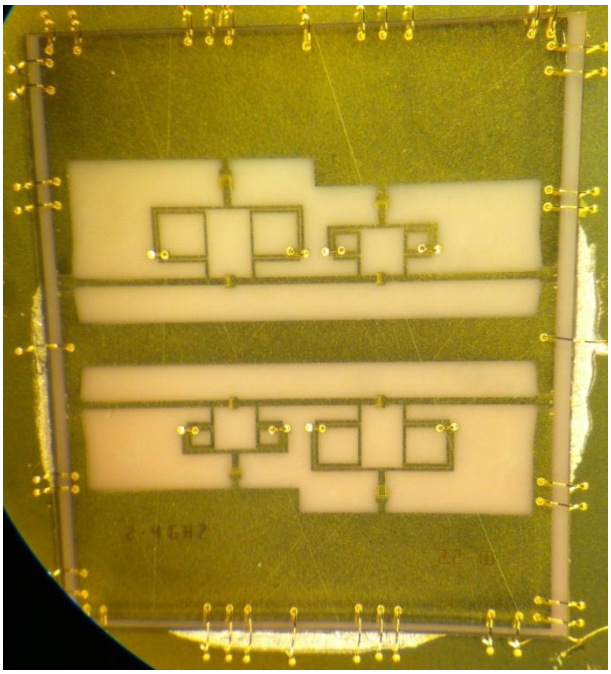


Figure 6-3. An example: Realized 2 to 4 GHz 22.5° Phase shift bit ready for measurement after post-processing.

6.2 Measurement Results of Phase Shift Bits

Measurements are done on Cascade Summit9000 Analytical probe station with CPW probes, and Agilent E8361A PNA. Remember that there are three layouts for each phase shift bits. Some of the variations could not be measured due to certain reasons; such as, fabrication related problems, post-process related problems, and etc. The measured variations are given in this sub-section.

The variations are named as "M" for the case 1 of the original design, "DCM" for the DC blocking capacitor added version of the original design, and "DCF" for the hybrid connection assumed case. For example "180° M" is the 180° phase shift bit constructed with original design and additional transitions for measurement purposes, "90° DCM" is the 90° phase shift bit constructed with DC blocking capacitors, additional lines, and transitions for measurement purposes in addition to the original designed phase shifter. Finally, "45° DCF" is a 45° phase shift bit with DC blocking capacitors and Microstrip ended structures for hybrid integration of the originally designed phase shift bit.

For the sake of simplicity, only the differential phase plots of the measured responses are given. Other than differential phase, minimum return loss and maximum insertion loss are given comparison with the practical design.

6.2.1 Measurement Results of 1 to 2 GHz Phase Shift Bits

The measured variations of 1 to 2 GHz phase shifter 180° phase shift bit are "180° DCM", and "180° DCF". Again, please note that the return loss and insertion loss plots are not given for the sake of simplicity. Instead maximum value of insertion loss and minimum value of return loss are given in the tables together with differential phase related calculations.

In Figure 6-4, the differential phase plots of measurement and practical design are given for 180° DCM. The design and measurement have well agreement. In Table 6-1, differential phase related data, i.e., rms phase, rms phase error, and maximum phase

error; together with maximum insertion loss and minimum return loss values for the ideal design, practical design, and fabrication are presented. rms phase error is worse than the practical case. However, it is still very low compared to a 180° phase shift within an octave band. The insertion loss values presented are the total switch losses and circuit loss. Insertion loss is higher than the expected, which is a normal result because no electroplating is done for this fabrication. Insertion loss can be better by electroplating the base metals. Return loss is around 15 dB.

For 1 to 2 GHz 180° DCF phase shift bit, the differential phase is presented in Figure 6-5 having a well agreement with the practical design; differential phase related data are presented along with the minimum return loss and maximum insertion loss in Table 6-2. rms phase error is measured for this case as 2.81° lower than the previous one. The reason why insertion loss is high is explained above.

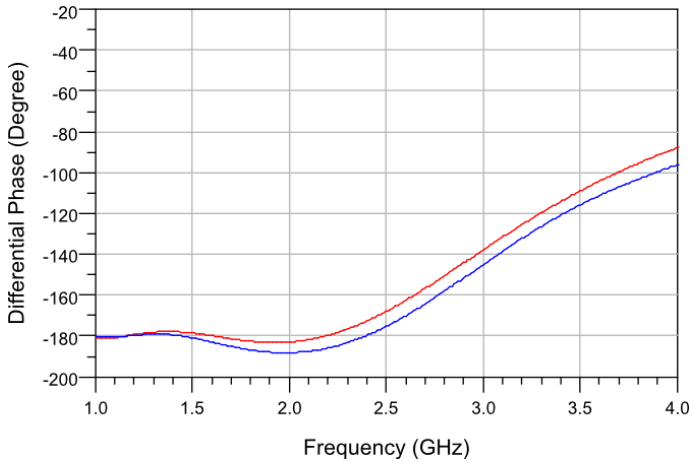


Figure 6-4. Differential phase response of 1-2 GHz 180° DCM phase shift bit measurement in comparison with practical design (red line represents the practical design and blue line represents the measurement result).

Table 6-1. Calculated rms phase, rms Phase Error (PE), and maximum phase error, maximum insertion loss and minimum return loss comparison between the ideal case, practical design, and measurement results of 1 to 2 GHz 180° DCM phase shift bit.

	rms Phase (°)	rms PE (°)	Max. PE (°)	Max IL (dB)	Min RL (dB)
Ideal	180.23	2.17	3.42	-	-
Practical	180.45	1.85	2.80	1.83	16.64
Measurement	182.80	3.31	5.53	3.32	14.86

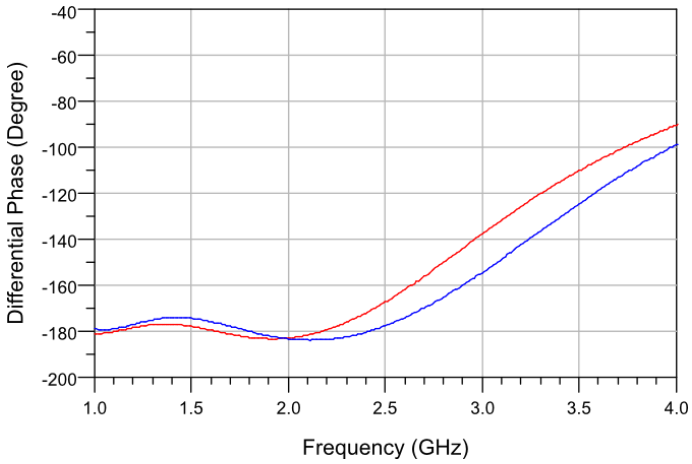


Figure 6-5. Differential phase response of 1-2 GHz 180° DCF phase shift bit measurement in comparison with practical design (red line represents the practical design and blue line represents the measurement result).

Table 6-2. Calculated rms phase, rms Phase Error (PE), and maximum phase error, maximum insertion loss and minimum return loss comparison between the ideal case, practical design, and measurement results of 1 to 2 GHz 180° DCF phase shift bit.

	rms Phase (°)	**rms PE (°)**	**Max. PE (°)**	**Max IL (dB)**	**Min RL (dB)**
Ideal	180.23	2.17	3.42	-	-
Practical	180.20	2.21	3.30	1.8	18
Measurement	177.90	2.81	5.61	5.19	14.65

All of the variations of 1 to 2 GHz phase shifter 90° phase shift bit are measured. Those are "90° M", "90° DCM", and "90° DCF".

The differential phase of 1 to 2 GHz 90° M variation is given in Figure 6-6. The measured response is degraded from the practical design. The phase related calculations, maximum insertion loss and minimum return loss data are given in Table 6-3. The degradation in phase can also be observed in that table. Maximum insertion loss is around 7 dB, which is actually not acceptable. The minimum return loss is around 12 dB, which is much lower than the expected design case. In fact, these values both belong to lower branch, telling that there might be a problem with fabrication or post-processing for that branch. The maximum insertion loss is around 3.37 dB, and the minimum return loss is around 16 dB for the upper branch. The degradation in phase can be explained with this explanation. If the lower branch is

fabricated properly the results would be much better than the present case. Observing other two variations support this explanation.

The differential phase of 1 to 2 GHz 90° DCM variation is given in Figure 6-7. The practical design and fabricated and measured results well agreed. In Table 6-4, the phase related data can be observed. The minimum return loss is around 13 dB. This value is still an acceptable one.

1 to 2 GHz 90° DCF variation's differential phase plot is given in Figure 6-8. The practical design and measurement agreed well. The data; i.e., rms phase, rms phase error, maximum phase error, maximum insertion loss, and minimum return loss are given in Table 6-5. The measured differential phase is the best for this case compared with the ideal and practical designs. The minimum return loss is around 14 dB, and the maximum insertion loss is 3.45 dB.

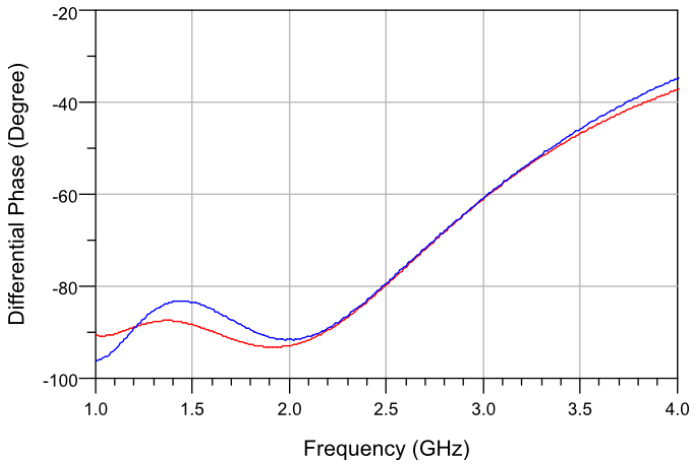


Figure 6-6. Differential phase response of 1-2 GHz 90° M phase shift bit measurement in comparison with practical design (red line represents the practical design and blue line represents the measurement result).

Table 6-3. Calculated rms phase, rms Phase Error (PE), and maximum phase error , maximum insertion loss and minimum return loss comparison between the ideal case, practical design, and measurement results of 1 to 2 GHz 90° M phase shift bit.

	rms Phase (°)	rms PE (°)	Max. PE (°)	Max IL (dB)	Min RL (dB)
Ideal	90.01	2.35	4.72	-	-
Practical	90.32	1.98	3.02	1.70	19.60
Measurement	88.42	3.83	7.95	7.14	11.87

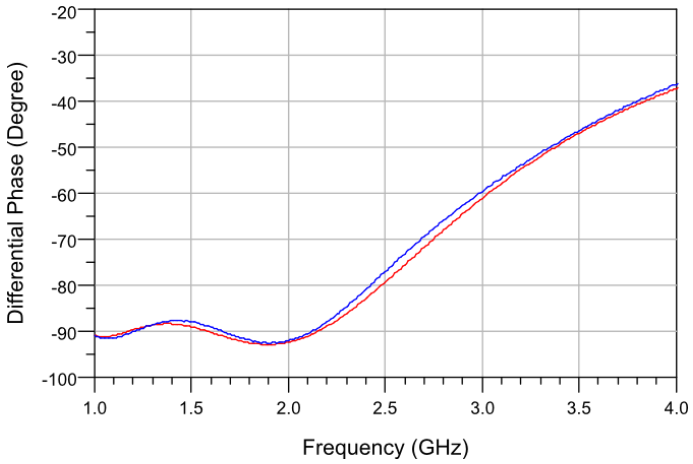


Figure 6-7. Differential phase response of 1-2 GHz 90° DCM phase shift bit measurement in comparison with practical design (red line represents the practical design and blue line represents the measurement result).

Table 6-4. Calculated rms phase, rms Phase Error (PE), and maximum phase error , maximum insertion loss and minimum return loss comparison between the ideal case, practical design, and measurement results of 1 to 2 GHz 90° DCM phase shift bit.

	rms Phase (°)	**rms PE (°)**	**Max. PE (°)**	**Max IL (dB)**	**Min RL (dB)**
Ideal	90.01	2.35	4.72	-	-
Practical	90.70	1.54	2.28	1.78	16.74
Measurement	90.31	1.67	2.54	4.68	12.82

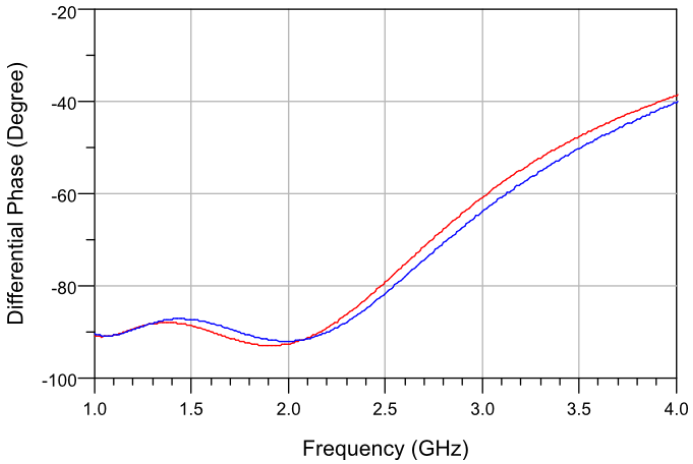


Figure 6-8. Differential phase response of 1-2 GHz 90° DCF phase shift bit measurement in comparison with practical design (red line represents the practical design and blue line represents the measurement result).

Table 6-5. Calculated rms phase, rms Phase Error (PE), and maximum phase error , maximum insertion loss and minimum return loss comparison between the ideal case, practical design, and measurement results of 1 to 2 GHz 90° DCF phase shift bit.

	rms Phase (°)	rms PE (°)	Max. PE (°)	Max IL (dB)	Min RL (dB)
Ideal	90.01	2.35	4.72	-	-
Practical	90.48	1.73	2.61	1.77	18.61
Measurement	89.55	1.60	2.59	3.45	13.94

The measured variations of 1 to 2 GHz phase shifter 45° phase shift bit are "45° M", and "45° DCF".

The measured differential phase of 1 to 2 GHz 45° M phase shift bit variation in comparison with practical design is given in Figure 6-9. The measured response and practical design behaves similar in terms of trace figure, however, the measured response has around 1° high rms phase value. This can be observed in Table 6-6. The rms phase error values are very close to each other, as well as the maximum phase errors. The minimum return loss value is close to the practical design. The insertion loss is a little bit higher than the practical case, which is because of only base metal is fabricated in the process, the electroplating is not done.

The comparison of the differential phase shifts of the practical design and measurement result is presented in Figure 6-10 for 1 to 2 GHz 45° DCF phase shift bit variation. The difference in rms phase, rms phase error, and maximum phase error between the practical case and the fabricated phase shift bit is very low, and can be observed in Table 6-7. The return loss for the fabrication is around 15 dB. The insertion loss is around 3.3 dB. The design and fabrication of the phase shift bits agree with a little error, which is usual.

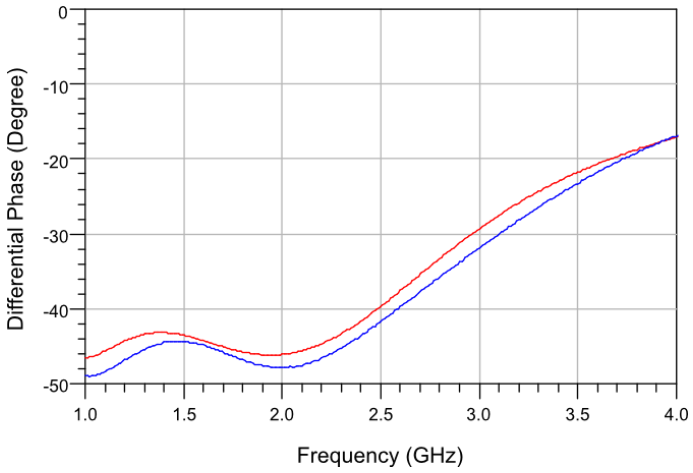


Figure 6-9. Differential phase response of 1-2 GHz 45° M phase shift bit measurement in comparison with practical design (red line represents the practical design and blue line represents the measurement result).

Table 6-6. Calculated rms phase, rms Phase Error (PE), and maximum phase error, maximum insertion loss and minimum return loss comparison between the ideal case, practical design, and measurement results of 1 to 2 GHz 45° M phase shift bit.

	rms Phase (°)	**rms PE (°)**	**Max. PE (°)**	**Max IL (dB)**	**Min RL (dB)**
Ideal	45.24	1.04	1.59	-	-
Practical	44.82	1.13	1.81	1.78	19.83
Measurement	46.38	1.47	2.70	3.29	19.68

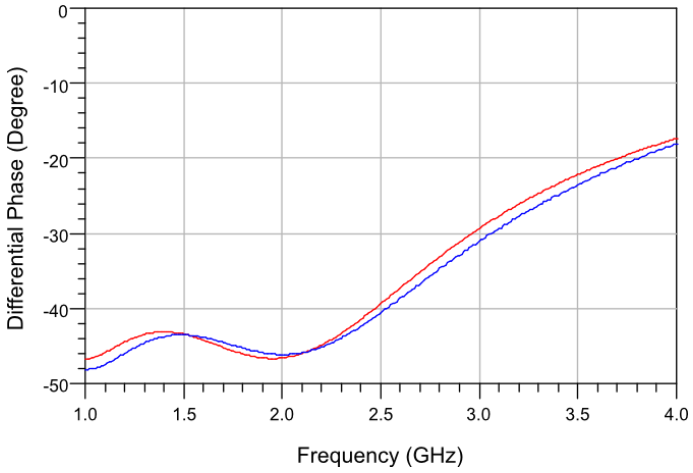


Figure 6-10. Differential phase response of 1-2 GHz 45° DCF phase shift bit measurement in comparison with practical design (red line represents the practical design and blue line represents the measurement result).

Table 6-7. Calculated rms phase, rms Phase Error (PE), and maximum phase error, maximum insertion loss and minimum return loss comparison between the ideal case, practical design, and measurement results of 1 to 2 GHz 45° DCF phase shift bit.

	rms Phase (°)	rms PE (°)	Max. PE (°)	Max IL (dB)	Min RL (dB)
Ideal	45.24	1.04	1.59	-	-
Practical	44.98	1.30	1.86	1.71	20.84
Measurement	45.27	1.37	2.97	3.55	14.95

1 to 2 GHz 22.5° phase shift bit measured variations are "22.5° M" and "22.5° DCF". The measured differential phase shift can be observed in Figure 6-11 for 1 to 2 GHz 22.5° M phase shift bit. The fabricated phase shift bit has a shift in rms phase around 2°. rms phase error of the practical design and the fabricated phase shifter has a little difference. The return loss of the fabricated phase shifter and the practical design are nearly at the same value. These can also be observed in Table 6-8.

The measured differential phase shift in comparison with practical design is presented in Figure 6-12. The difference between the practical design and fabricated one may seem to be high. However, since the phase shift value is low, the difference actually is not that high. One can observe this issue in Table 6-9. The rms phase of the practical design result and the measured one have just 0.2° difference, in rms phase error this value is very low; such that it is equal to 0.1°. The return loss of the fabricated phase shift bit is around 14 dB. Overall, the fabricated phase shifter is successful.

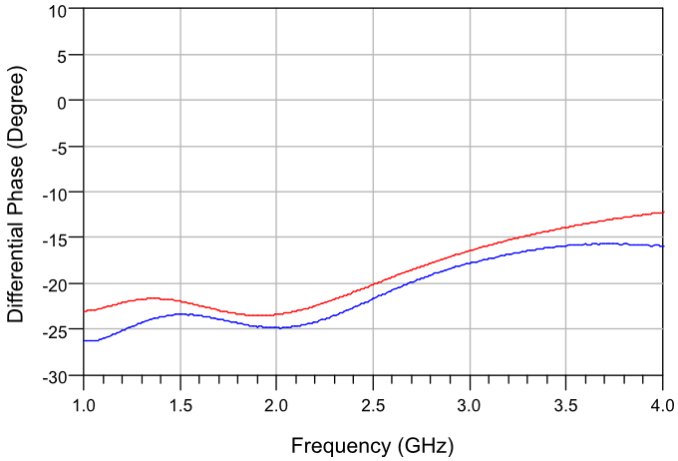


Figure 6-11. Differential phase response of 1-2 GHz 22.5° M phase shift bit measurement in comparison with practical design (red line represents the practical design and blue line represents the measurement result).

Table 6-8. Calculated rms phase, rms Phase Error (PE), and maximum phase error, maximum insertion loss and minimum return loss comparison between the ideal case, practical design, and measurement results of 1 to 2 GHz 22.5° M phase shift bit.

	rms Phase (°)	rms PE (°)	Max. PE (°)	Max IL (dB)	Min RL (dB)
Ideal	23.35	0.53	0.96	-	-
Practical	22.57	0.64	0.93	1.64	20.57
Measurement	24.48	0.89	1.86	3.36	20.47

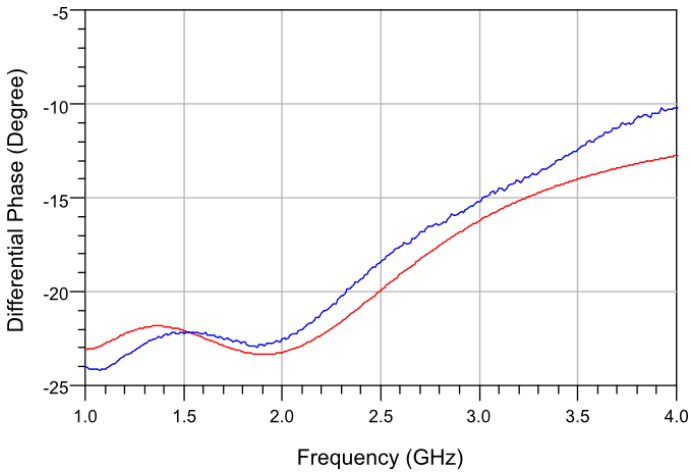


Figure 6-12. Differential phase response of 1-2 GHz 22.5° DCF phase shift bit measurement in comparison with practical design (red line represents the practical design and blue line represents the measurement result).

Table 6-9. Calculated rms phase, rms Phase Error (PE), and maximum phase error, maximum insertion loss and minimum return loss comparison between the ideal case, practical design, and measurement results of 1 to 2 GHz 22.5° DCF phase shift bit.

	rms Phase (°)	rms PE (°)	Max. PE (°)	Max IL (dB)	Min RL (dB)
Ideal	23.35	0.53	0.96	-	-
Practical	22.62	0.53	0.76	1.71	20.84
Measurement	22.87	0.63	1.37	3.65	13.79

6.2.2 Measurement Results of 2 to 4 GHz Phase Shift Bits

Better to note that some of the variations could not be measured due to fabrication, post-processing, and layout mistakes. The results of the measured variations are given in detail; the differential phase comparison graphs are given, and then the

phase related calculations together with minimum return loss and maximum insertion loss values are given in tables. For the sake of simplicity, the return loss and insertion loss plots are not included in here.

For 2 to 4 GHz 180° phase shift bit, only "180° DCF" variation could be measured. The differential phase plots are given in Figure 6-13. There is a high difference between the measured result and practical design result. Note that the maximum insertion loss is 6.66 dB, which is a high insertion loss value. This value is not normal compared to the above presented results. In addition to that, the return loss is measured to be at minimum around 10 dB. These two values are from the same branch, i.e., the upper branch. On the other hand, the maximum insertion loss in the lower branch is around 2.8 dB, and the minimum return loss is around 19 dB in the same branch. These unbalanced results caused an unbalanced differential phase shift.

The phase related calculations are presented in Table 6-10. One can observe that there is a 7° difference in rms phase between the measured results and practical design results.

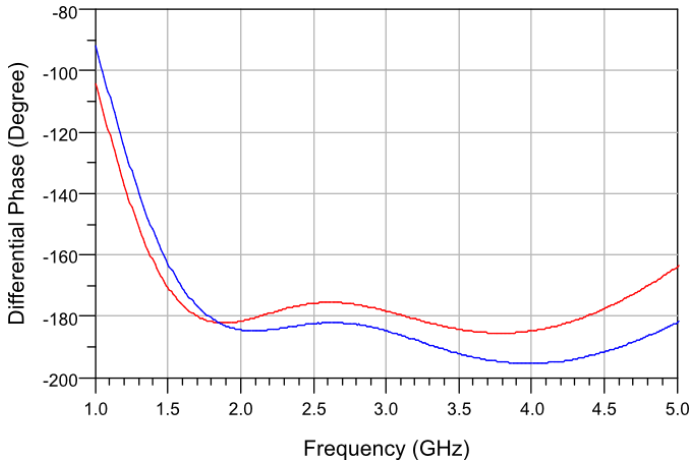


Figure 6-13. Differential phase response of 2-4 GHz 180° DCF phase shift bit measurement in comparison with practical design (red line represents the practical design and blue line represents the measurement result).

Table 6-10. Calculated rms phase, rms Phase Error (PE), and maximum phase error, maximum insertion loss and minimum return loss comparison between the ideal case, practical design, and measurement results of 2 to 4 GHz 180° DCF phase shift bit.

	rms Phase (°)	rms PE (°)	Max. PE (°)	Max IL (dB)	Min RL (dB)
Ideal	178.50	2.19	3.79	-	-
Practical	180.43	3.59	5.12	2.02	18.95
Measurement	187.50	4.75	8.03	6.66	10.20

For 2 to 4 GHz 90° phase shift bit, only "90° DCM" variation could be measured. The differential phase plots are given in Figure 6-14. A considerable difference can be observed between the measured result and practical design result at the end of the band of interest. The phase related calculations together with minimum return loss and maximum insertion loss data is presented in Table 6-11.

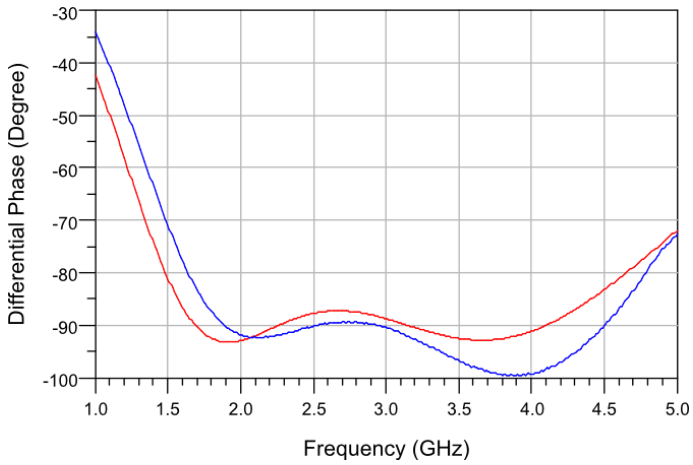


Figure 6-14. Differential phase response of 2-4 GHz 90° DCM phase shift bit measurement in comparison with practical design (red line represents the practical design and blue line represents the measurement result).

Table 6-11. Calculated rms phase, rms Phase Error (PE), and maximum phase error , maximum insertion loss and minimum return loss comparison between the ideal case, practical design, and measurement results of 2 to 4 GHz 90° DCM phase shift bit.

	rms Phase (°)	rms PE (°)	Max. PE (°)	Max IL (dB)	Min RL (dB)
Ideal	90.31	1.87	3.11	-	-
Practical	90.31	2.00	3.04	2.03	18.13
Measurement	93.47	3.55	6.30	3.46	14.39

"45° M" and "45° DCF" are the two variations that can be measured properly for 2 to 4 GHz 45° phase shift bit. The comparison of differential phase shift between the measured result and practical design result is presented in Figure 6-15 for "45° M"

case. There is around 2° shift can be observed from this plot. It can also be observed from Table 6-12, together with other phase shift related data. There is a little difference in terms of rms phase error and maximum phase error. The return loss and insertion loss values are satisfactory.

For "45° DCF" variation of 2 to 4 GHz phase shifter, the differential phase shift result is given in Figure 6-16, and the phase related data together with minimum return loss and maximum insertion loss values can be observed from Table 6-13. As it can be observed from the differential phase plots, the degradation increases with the frequency within the band of interest. Hence the maximum phase error is increased compared to the practical design results, as well as the rms phase error.

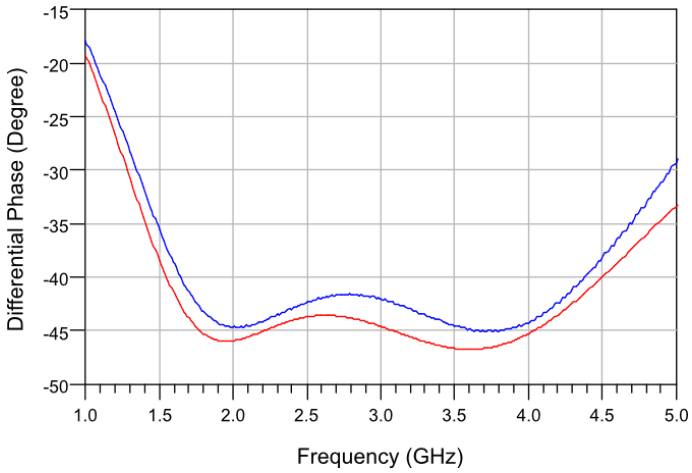


Figure 6-15. Differential phase response of 2-4 GHz 45° M phase shift bit measurement in comparison with practical design (red line represents the practical design and blue line represents the measurement result).

Table 6-12. Calculated rms phase, rms Phase Error (PE), and maximum phase error, maximum insertion loss and minimum return loss comparison between the ideal case, practical design, and measurement results of 2 to 4 GHz 45° M phase shift bit.

	rms Phase (°)	rms PE (°)	Max. PE (°)	Max IL (dB)	Min RL (dB)
Ideal	44.50	1.16	2.22	-	-
Practical	45.21	1.09	1.63	1.90	20.66
Measurement	43.43	1.21	1.86	2.91	15.00

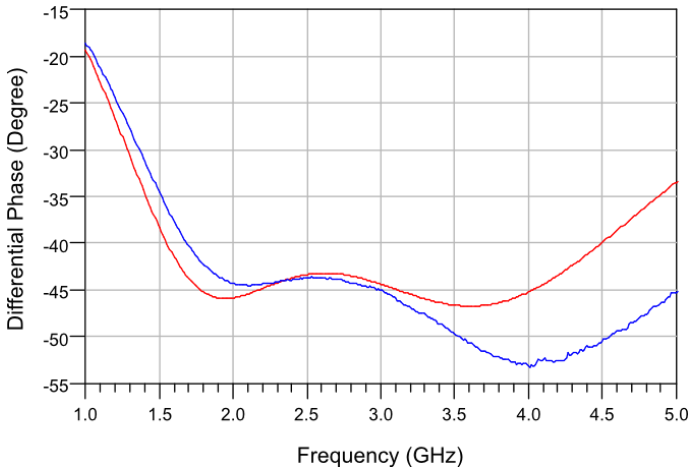


Figure 6-16. Differential phase response of 2-4 GHz 45° DCF phase shift bit measurement in comparison with practical design (red line represents the practical design and blue line represents the measurement result).

Table 6-13. Calculated rms phase, rms Phase Error (PE), and maximum phase error, maximum insertion loss and minimum return loss comparison between the ideal case, practical design, and measurement results of 2 to 4 GHz 45° DCF phase shift bit.

	rms Phase (°)	**rms PE (°)**	**Max. PE (°)**	**Max IL (dB)**	**Min RL (dB)**
Ideal	44.50	1.16	2.22	-	-
Practical	45.04	1.22	1.81	1.98	22.63
Measurement	46.96	3.23	6.31	5.28	17.49

For 2 to 4 GHz 22.5° phase shift bit, only the "22.5° M" variation can be measured properly. Differential phase plots can be observed from Figure 6-17, and it can be seen that there is around 2° rms phase difference between the measured result and practical design result.

The phase related calculations are given in Table 6-14, together with return loss and insertion loss related data.

The measured variations for 2 to 4 GHz phase shift bits are presented, and in the next-subsection 3 to 6 GHz phase shift bits are discussed.

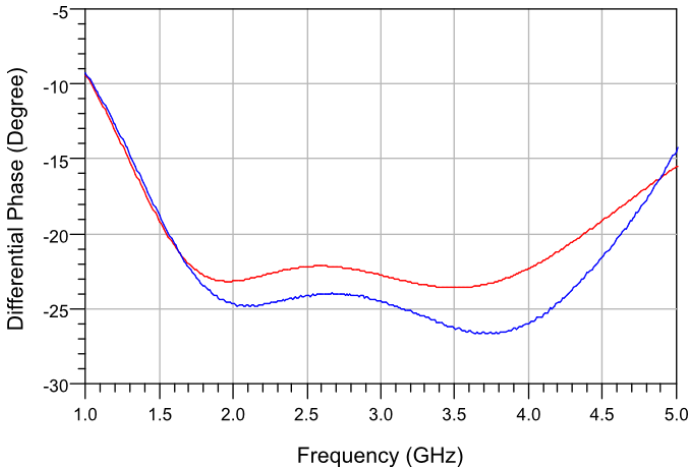


Figure 6-17. Differential phase response of 2-4 GHz 22.5° M phase shift bit measurement in comparison with practical design (red line represents the practical design and blue line represents the measurement result).

Table 6-14. Calculated rms phase, rms Phase Error (PE), and maximum phase error, maximum insertion loss and minimum return loss comparison between the ideal case, practical design, and measurement results of 2 to 4 GHz 22.5° M phase shift bit.

	rms Phase (°)	rms PE (°)	Max. PE (°)	Max IL (dB)	Min RL (dB)
Ideal	22.69	0.53	1.04	-	-
Practical	22.88	0.48	0.73	1.91	20.63
Measurement	25.16	0.94	1.54	3.64	14.26

6.2.3 Measurement Results of 3 to 6 GHz Phase Shift Bits

The measured phase shift variations for 3 to 6 GHz phase shifter are very low. In fact, there are two measured phase shift variations, which are "45° DCM", and "22.5° DCF".

3 to 6 GHz "45° DCM" variation related differential phase in comparison with the practical design is given in Figure 6-18. Note that the practical design result and measured result have good agreement up to around 4.5 GHz. After this frequency a little degradation can be observed. The phase related calculations, minimum return loss and maximum insertion loss information are provided in Table 6-15.

3 to 6 GHz "22.5° DCF" variation related results can be observed in Figure 6-19, and Table 6-16. There is a little difference between the rms phase values between the

practical design result and the measured results. However, the results are still satisfactory. There is little difference in terms of rms phase error values and maximum phase error values.

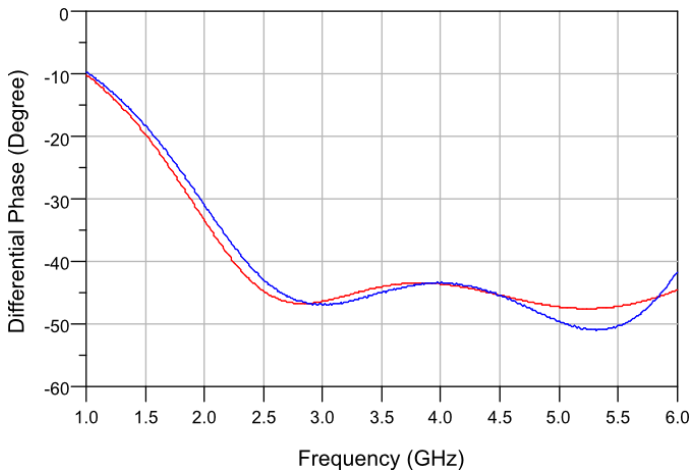


Figure 6-18. Differential phase response of 3-6 GHz 45° DCM phase shift bit measurement in comparison with practical design (red line represents the practical design and blue line represents the measurement result).

Table 6-15. Calculated rms phase, rms Phase Error (PE), and maximum phase error, maximum insertion loss and minimum return loss comparison between the ideal case, practical design, and measurement results of 3 to 6 GHz 45° DCM phase shift bit.

	rms Phase (°)	rms PE (°)	Max. PE (°)	Max IL (dB)	Min RL (dB)
Ideal	46.21	1.00	1.81	-	-
Practical	45.56	1.39	2.08	2.50	21.94
Measurement	46.63	2.55	4.91	4.91	10.21

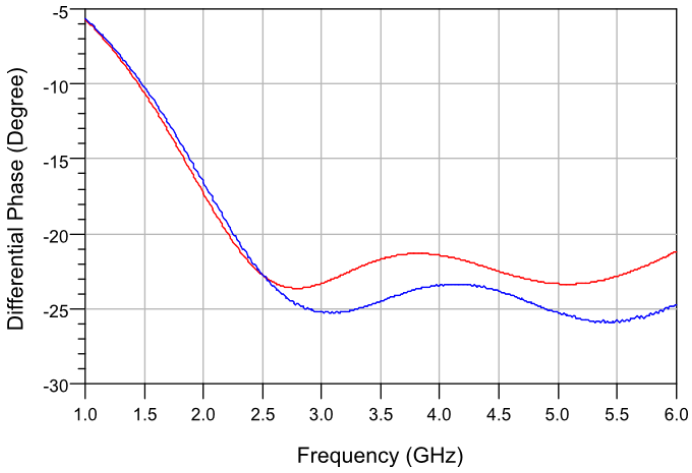


Figure 6-19. Differential phase response of 3-6 GHz 22.5° DCF phase shift bit measurement in comparison with practical design (red line represents the practical design and blue line represents the measurement result).

Table 6-16. Calculated rms phase, rms Phase Error (PE), and maximum phase error, maximum insertion loss and minimum return loss comparison between the ideal case, practical design, and measurement results of 3 to 6 GHz 22.5° DCF phase shift bit.

	rms Phase (°)	**rms PE (°)**	**Max. PE (°)**	**Max IL (dB)**	**Min RL (dB)**
Ideal	23.17	0.59	1.23	-	-
Practical	22.37	0.71	1.18	2.54	21.27
Measurement	24.70	0.84	1.33	4.96	13.92

Almost all of the phase shift values are reached with different phase shift variations. The results can be accounted as satisfactory. Moreover, for some cases the practical design results are almost obtained from the measurement results. The last measured performances of the phase shift bits are presented in Appendix C

The next chapter is the conclusion of the thesis. A brief summary is given, and possible future works are discussed.

CHAPTER 7

CONCLUSIONS AND FUTURE WORKS

In this study all of the stages of broadband phase shifter realization are presented. These stages can be named as theoretical design, practical design, surface micromachining fabrication, post-processing, and measurements.

In this thesis, literature survey on broadband phase shifters is discussed in detail. In general, the ideal design of 1 to 2 GHz, 2 to 4 GHz, and 3 to 6 GHz 4-bit phase shifters are done, and the ideal value of lumped components are calculated. After the ideal design of phase shifters are completed, square planar spiral inductors and metal-insulator-metal capacitors are EM simulated, then lumped equivalent model parameters are obtained for the non-ideal components. When the desired values of the lumped components are achieved, the practical designs of phase shifters are completed. Surface micromachining is used to fabricate the phase shift bits. Post-processing is done for the phase shift bits for measurement purposes, and measurements are done. From the measured phase shift bit variations it can be observed that the designs are accurate enough.

Achievements of the presented work in this thesis can be ordered as follows;

1. Theoretical approach to one-stage, and two-stage 4-bit, all-pass network phase shifters are given, which is already given in literature. In addition to this, for the first time in literature, design parameters for 5.625°, and 11.25° are found for one-stage, and two-stage all-pass network phase shifter for different bandwidths.

2. An extended theoretical calculation method for multi-stage all-pass network phase shifters is presented for the first time in literature, for 2^{n-1} number of stages. An example of this new theoretical approach is given for eight-stage all-pass network phase shifter. Obtaining the equations for the ideal inductors starting from the first inductor up to 2^{n}th inductor, generating the differential phase equations, and equations for capacitors are provided. The ideal phase shift results are also given. It is pointed out that with this method, ideally, infinite phase shift band can be achieved.
3. For stage numbers other than power of 2, a different approach, i.e., adjusting the center frequencies of the all-pass filters, is presented. An example is given regarding to this approach, which is three-stage all-pass network phase shifter.
4. The calculated ideal lumped element values are given for two-stage 4-bit all-pass network phase shifters of 1 to 2 GHz, 2 to 4 GHz, and 3 to 6 GHz. Also, the calculated ideal lumped element values for three-stage 4-bit 1 to 6 GHz phase shifter are provided. Ideal phase responses are investigated in terms of rms phase, rms phase errors, and maximum phase errors within the band of interest.
5. Square planar spiral inductor basics, surface micromachined inductor literature review, design of the SPSIs using in-house technology, fabrication and measurement results are provided. It is seen that the results of practical design and fabrication of these SPSIs are well matched.
6. Mitered corner square planar spiral inductor idea is discussed. In practical design results and measurement results it is observed that for the same geometry of a square planar spiral inductor, both self-resonance frequencies, i.e., parallel resonance frequency and series resonance frequency, are shifted to the right in frequency.
7. Design methodology of metal-insulator-metal capacitors is examined. Since the group has considerable experience on that topic, dedicated fabrication to

MIM capacitors are not done. They have been used directly in the phase shifter fabrication.

8. Practical design of two-stage 4-bit 1 to 2 GHz, 2 to 4 GHz, and 3 to 6 GHz phase shifters are discussed with geometrical specifications of lumped components, equivalent model parameters of lumped components. The results are presented in terms of return loss, insertion loss, and differential phase shift together with rms phase, rms phase error, and maximum phase error calculations. Also, practical design results of three-stage 4-bit 1 to 6 GHz phase shifter are given.
9. A novel approach for increased phase resolution phase shifter other than conventional method is discussed. An example practical design is provided for 3 to 6 GHz 5.625°, and 11.25°. The results are provided in terms of return loss, insertion loss, and differential phase together with phase related calculations.
10. Fabrication, post-processing, and measurement of 1 to 2 GHz, 2 to 4 GHz, and 3 to 6 GHz phase shift bit variations are discussed. According to the measurement results, in general, the designed phase shift bits well agreed with the practical designs. In most cases, low rms phase error, high return loss values are achieved. Although insertion loss values seem to be high, it can be avoided by electroplating the base metals of the inductors, lines, tee-junctions and etc.

Although the fabrication of the phase shift bits can be accounted as successful, there is still much to do. Moreover this topic can further be improved, or the all-pass network topology can be used in different topics. For a brief summary of the future work and possible improvements, refer to below ordered topics;

1. The hybrid connection of phase shift bits together with proper SPDT switches can be done. A proper substrate, microstrip connections, and RF and DC grounding must be considered to completely achieve this work.

2. Mitering of the corners of inductors can be studied to achieve the optimum miter with less parasitics. Inductors may then have higher quality-factor values, and higher SRF values.
3. High resistive silicon substrates with backside etch can be assumed, for cost effective fabrications. However, further study on decreasing the parasitics of lumped components is needed.
4. Fabrication of three-stage phase shifters for ultra wide-band applications can be done. It is better to note that the insertion loss would be high.
5. A monolithic fabrication with SPDT switches would further increase the performance of the phase shifters. MMIC, SiGe BiCMOS, or RF CMOS fabrications may be used for monolithic fabrication of the phase shifters.
6. For higher resolution phase shifters, the new method described for 5.625°, and 11.25° phase shift bits can be fabricated. For this fabrication, one might need tunable MEMS capacitors, or MEMS bridge arrays (as used in DMTL phase shifters). Varactors might be another candidate for achieving the tunable capacitor, in which only three voltages used.
7. The inherently matched nature of all-pass filters can be an important advantage in many applications. For example, ultra wide-band impedance matching networks may be studied or ultra-wide-band equal and unequal Wilkinson power dividers may be achieved with decreased circuit size.

APPENDIX A

DESIGN DETAILS OF 2 TO 4 GHz PHASE SHIFT BITS

A.1 Design of 180° Phase Shift Bit

The final series connected MIM capacitors design related data are given in Table A-1, the layout considered SPSIs are given in Table A-2, and the shunt connected MIM capacitors' final designs are given in Table A-3. The S-parameters graphs of the final layout design are given in Figure A-1, the differential phase shift related graph is given in Figure A-2, with the phase shift related calculation results as in Table A-4. As it can be observed from these results that return loss is around -16 dB, insertion loss is around 1.95 dB at 4 GHz, at worst.

Table A-1. 2 to 4 GHz phase shifter 180° phase shift bit finalized series connected MIM capacitor design related geometrical parameter values, and the lumped equivalent model parameter values.

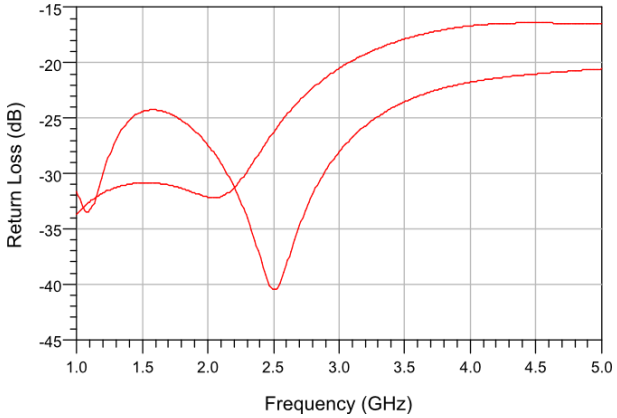
Width (µm)	Length (µm)	L_{feed} (µm)	C (pF)	C_{sh} (fF)	L_s (pH)	R_s (ohm)
100	59	100	1.257	40	373	0.177
100	9	125	0.2	39	436	0.317
100	21	119	0.455	39	390	0.212
100	29	115	0.622	39	384	0.203

Table A-2. The finalized layout designs of selected SPSIs (extension of 144.5 µm).

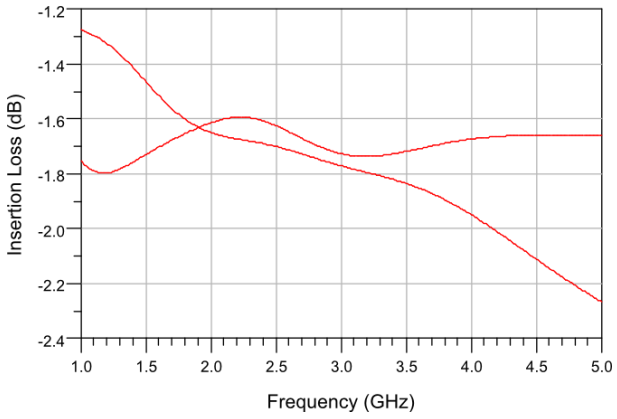
W_{line} (µm)	Spacing (µm)	D_{out} (µm)	L_s (nH)	R_s (ohm)	C_{sh} (fF)	Q_{max}	Q_{ripple}	Q_{min}	Q_{mean}
100	20	504	1.14	0.764	88	32.659	3.86	26.42	30.28
100	15	698	2.263	0.776	142	53.019	5.326	45.83	51.156
100	15	850	3.13	0.961	188	50.102	6.612	41.022	47.634
40	20	672	6.235	1.866	131	37.445	9.506	24.198	33.705

Table A-3. The final design of shunt connected MIM capacitors for 2 to 4 GHz phase shifter 180° phase shift bit.

	(pF)	Width (µm)	Length (µm)	C (pF)	C_{sh} (fF)	L_s (pH)	R_s (ohm)
C2_1	5	100	222	4.654	52	459	0.226
C2_2	0.92	100	34	0.725	38	365	0.187
C4_1	1.8	100	67	1.424	41	377	0.174
C4_2	2.52	100	99	2.087	43	394	0.19



(a)



(b)

Figure A-1. The 2 to 4 GHz phase shifter 180° phase shift bit layout considered, and iterated shunt MIM capacitors; S-parameters graphs for practical case (a) return loss for the practical case, and (b) insertion loss for the practical case.

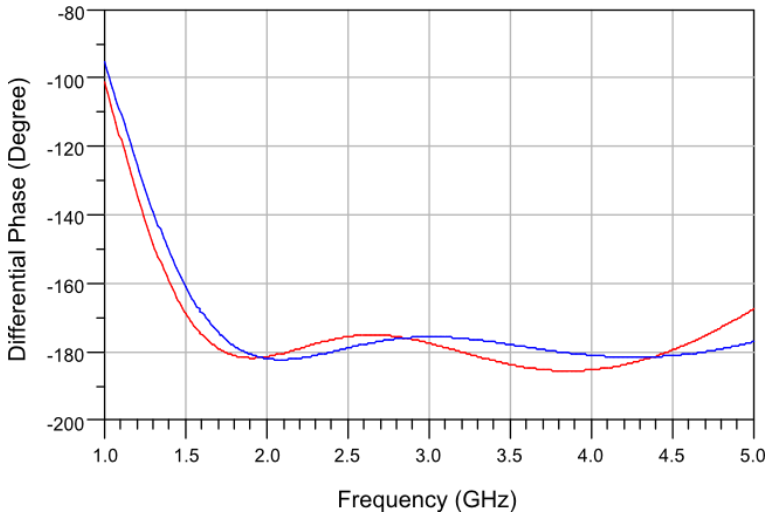


Figure A-2. The differential phase shift response of 2 to 4 GHz phase shifter 180° phase shift bit layout considered, and iterated shunt MIM capacitors (red line represents the present case, and blue line represents the ideal case).

Table A-4. Calculated mean phase, minimum phase, rms phase, maximum phase and phase ripple comparison between the ideal case and the finalized layout considerations of 2 to 4 GHz phase shifter 180° phase shift bit.

	Min. Phase (°)	**Rms Phase (°)**	**Max. Phase (°)**	**Ripple (°)**
Ideal	175.627	178.515	182.294	3.792
Present case	175.071	180.034	185.573	5.578

Considering the sizes and layout view, one should refer to the following Figure A-3, for the upper branch of 2 to 4 GHz phase shifter 180° phase shift bit, and for the lower branch refer to Figure A-4.

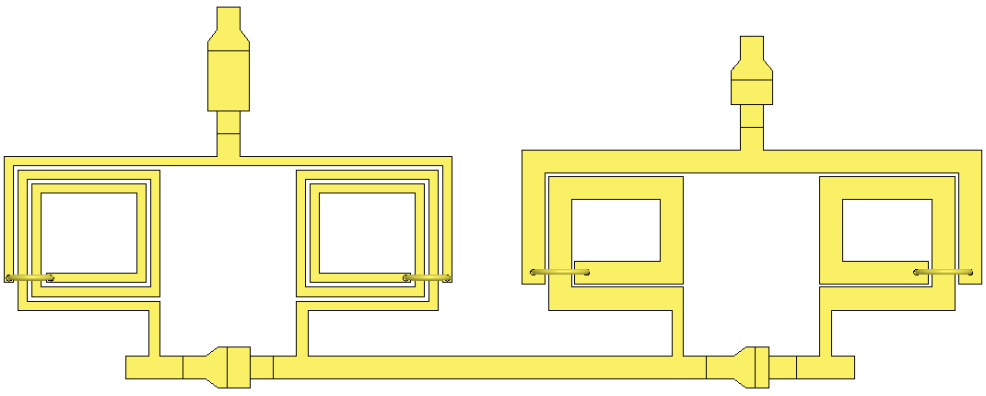


Figure A-3. Upper branch of 2 to 4 GHz phase shifter 180° phase shift bit (Length: 4.218 mm, Width: 1.664 mm, Separation between inductors: 300 µm).

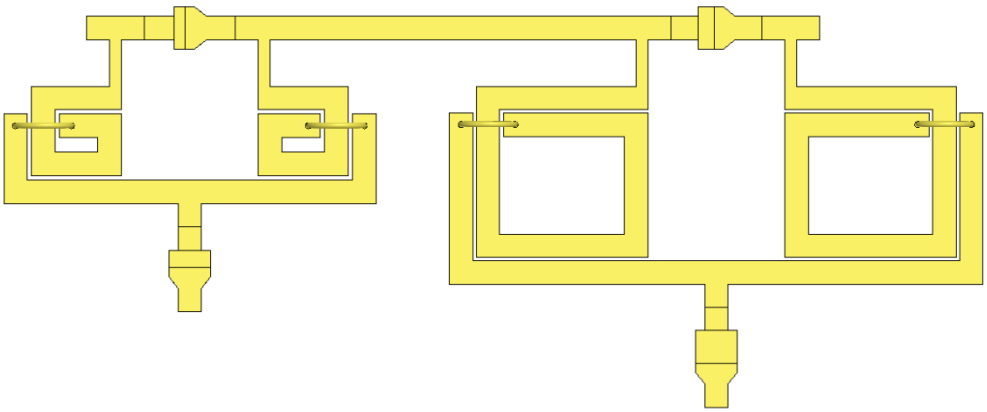


Figure A-4. Lower branch of 2 to 4 GHz phase shifter 180° phase shift bit (Length: 4.202 mm, Width: 1.719 mm, Separation between inductors: 316 µm).

A.2 Design of 90° Phase Shift Bit

The final series connected MIM capacitors design related data are given in Table A-5, the layout considered SPSIs are given in Table A-6, and the shunt connected MIM capacitors' final designs are given in Table A-7. The S-parameters graphs of the final layout design are given in Figure A-5, the differential phase shift related graph is given in Figure A-6, with the phase shift related calculation results as in Table A-8. As it can be observed from these results that return loss is around -17.5 dB, insertion loss is around 1.9 dB at 4 GHz, at worst.

Table A-5. 2 to 4 GHz phase shifter 90° phase shift bit finalized series connected MIM capacitor design related geometrical parameter values, and the lumped equivalent model parameter values.

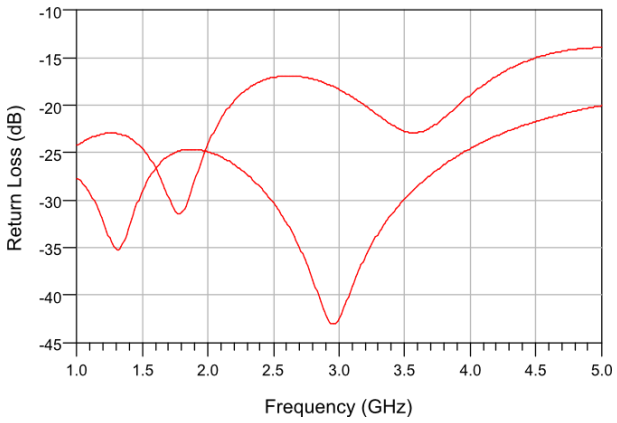
Width (µm)	Length (µm)	L_{feed} (µm)	C (pF)	C_{sh} (fF)	L_s (pH)	R_s (ohm)
100	46	100	0.978	39	369	0.182
100	14	116	0.292	38	434	0.259
100	18	114	0.387	39	393	0.221
100	34	106	0.729	39	372	0.182

Table A-6. The finalized layout designs of selected SPSIs (extension of 138 µm).

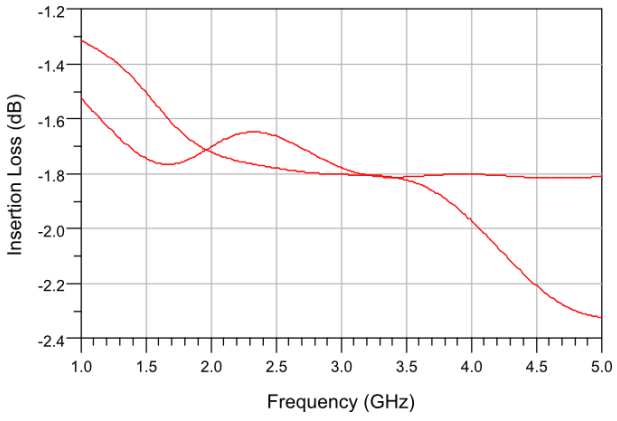
W_{line} (µm)	Spacing (µm)	D_{out} (µm)	L_s (nH)	R_s (ohm)	C_{sh} (fF)	Q_{max}	Q_{ripple}	Q_{min}	Q_{mean}
40	20	805	4.87	1.584	146	39.069	7.102	29.098	36.201
80	15	831	3.565	1.042	175	49.626	8.015	38.376	46.391
100	20	665	1.978	0.842	133	44.452	4.476	38.273	42.749
120	15	621	1.436	0.834	121	34.664	3.827	28.793	32.62

Table A-7. The final design of shunt connected MIM capacitors for 2 to 4 GHz phase shifter 90° phase shift bit.

	(pF)	Width (µm)	Length (µm)	C (pF)	C_{sh} (fF)	L_s (pH)	R_s (ohm)
C2_1	3.92	100	166	3.486	48	431	0.209
C2_2	1.16	100	37	0.788	38	366	0.176
C4_1	1.6	100	58	1.234	40	372	0.18
C4_2	2.84	100	108	2.265	44	400	0.191



(a)



(b)

Figure A-5. The 2 to 4 GHz phase shifter 90° phase shift bit layout considered, and iterated shunt MIM capacitors; S-parameters graphs for practical case (a) return loss for the practical case, and (b) insertion loss for the practical case.

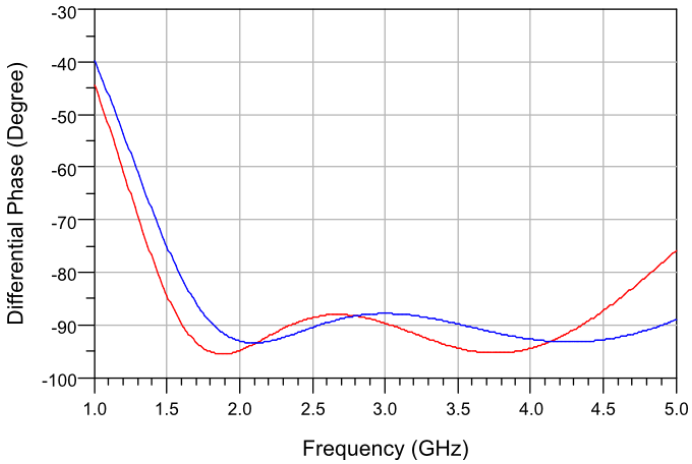


Figure A-6. The differential phase shift response of 2 to 4 GHz phase shifter 90° phase shift bit layout considered, and iterated shunt MIM capacitors (red line represents the present case, and blue line represents the ideal case).

Table A-8. Calculated mean phase, minimum phase, rms phase, maximum phase and phase ripple comparison between the ideal case and the finalized layout considerations of 2 to 4 GHz phase shifter 90° phase shift bit.

	Min. Phase (°)	**Rms Phase (°)**	**Max. Phase (°)**	**Ripple (°)**
Ideal	87.846	90.325	93.416	3.110
Present case	86.451	90.038	93.434	3.553

Considering the sizes and layout view, one should refer to the following Figure A-7, for the upper branch of 2 to 4 GHz phase shifter 90° phase shift bit, and for the lower branch refer to Figure A-8.

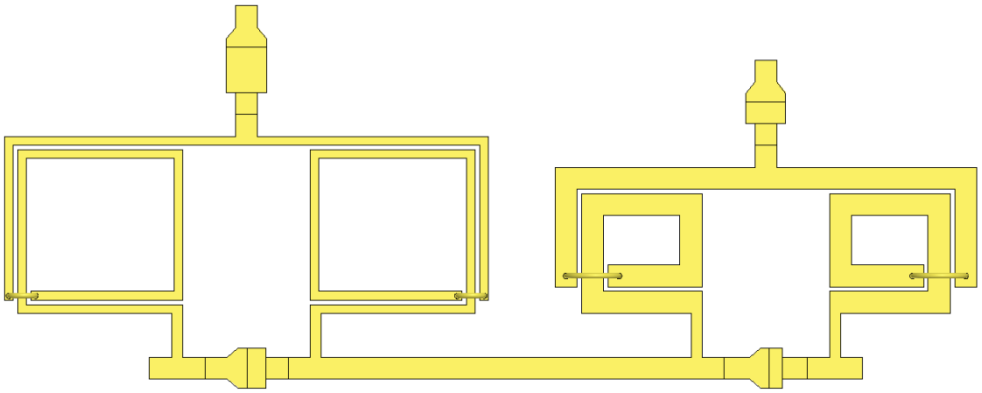


Figure A-7. Upper branch of 2 to 4 GHz phase shifter 90° phase shift bit (Length: 4.351 mm, Width: 1.741 mm, Separation between inductors: 300 µm).

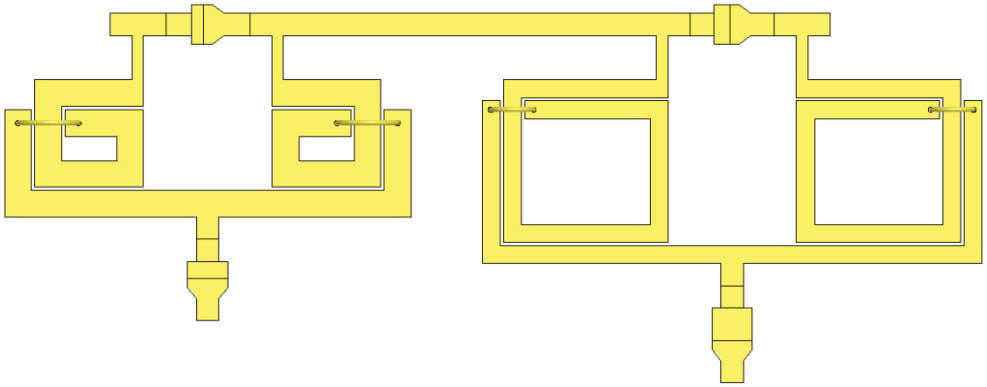


Figure A-8. Lower branch of 2 to 4 GHz phase shifter 90° phase shift bit (Length: 4.374 mm, Width: 1.709 mm, Separation between inductors: 318 µm).

A.3 Design of 45° Phase Shift Bit

The final series connected MIM capacitors design related data are given in Table A-9, the layout considered SPSIs are given in Table A-10, and the shunt connected MIM capacitors' final designs are given in Table A-11. The S-parameters graphs of the final layout design are given in Figure A-9, the differential phase shift related graph is given in Figure A-10, with the phase shift related calculation results as in Table A-12. As it can be observed from these results that return loss is around -23 dB, insertion loss is around 1.9 dB at 4 GHz, at worst.

Table A-9. 2 to 4 GHz phase shifter 45° phase shift bit finalized series connected MIM capacitor design related geometrical parameter values, and the lumped equivalent model parameter values.

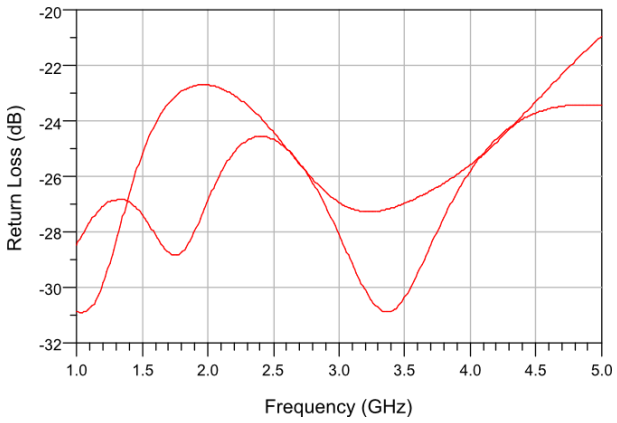
Width (µm)	Length (µm)	L_{feed} (µm)	C (pF)	C_{sh} (fF)	L_s (pH)	R_s (ohm)
100	41	100	0.881	39	365	0.176
100	15	113	0.316	38	417	0.245
100	17	112	0.365	38	396	0.229
100	35	103	0.751	39	368	0.182

Table A-10. The finalized layout designs of selected SPSIs (extension of 135.5 µm).

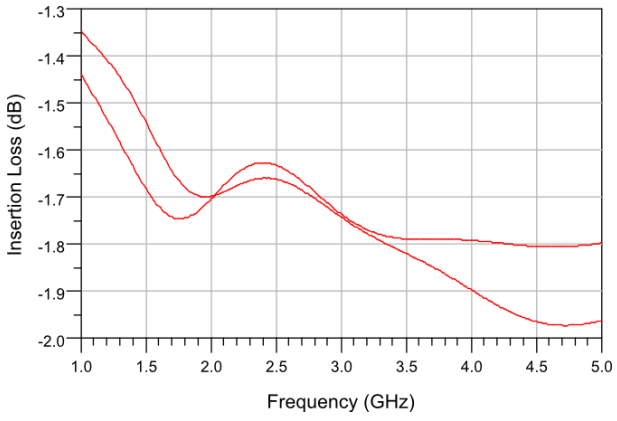
W_{line} (µm)	Spacing (µm)	D_{out} (µm)	L_s (nH)	R_s (ohm)	C_{sh} (fF)	Q_{max}	Q_{ripple}	Q_{min}	Q_{mean}
80	15	512	1.599	0.806	89	40.964	3.769	35.780	39.548
80	15	554	1.856	0.754	100	49.122	6.01	40.512	46.521
60	15	762	3.792	1.105	149	48.214	5.118	41.178	46.296
40	15	728	4.458	1.409	128	44.207	5.624	36.469	42.093

Table A-11. The final design of shunt connected MIM capacitors for 2 to 4 GHz phase shifter 45° phase shift bit.

	(pF)	Width (µm)	Length (µm)	C (pF)	C_{sh} (fF)	L_s (pH)	R_s (ohm)
C2_1	3.56	100	154	3.235	47	424	0.205
C2_2	1.28	100	47	1.002	40	369	0.173
C4_1	1.48	100	57	1.234	40	372	0.18
C4_2	3.04	100	124	2.621	45	409	0.198



(a)



(b)

Figure A-9. The 2 to 4 GHz phase shifter 45° phase shift bit layout considered, and iterated shunt MIM capacitors; S-parameters graphs for practical case (a) return loss for the practical case, and (b) insertion loss for the practical case.

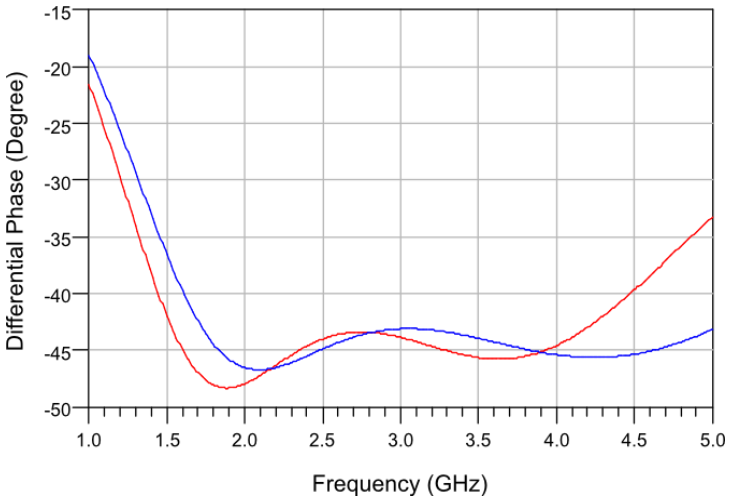


Figure A-10. The differential phase shift response of 2 to 4 GHz phase shifter 45° phase shift bit layout considered, and iterated shunt MIM capacitors (red line represents the present case, and blue line represents the ideal case).

Table A-12. Calculated mean phase, minimum phase, rms phase, maximum phase and phase ripple comparison between the ideal case and the finalized layout considerations of 2 to 4 GHz phase shifter 45° phase shift bit.

	Min. Phase (°)	**Rms Phase (°)**	**Max. Phase (°)**	**Ripple (°)**
Ideal	43.091	44.512	46.719	2.221
Present case	43.542	45.062	47.545	2.495

Considering the sizes and layout view, one should refer to the following Figure A-11, for the upper branch of 2 to 4 GHz phase shifter 45° phase shift bit, and for the lower branch refer to Figure A-12.

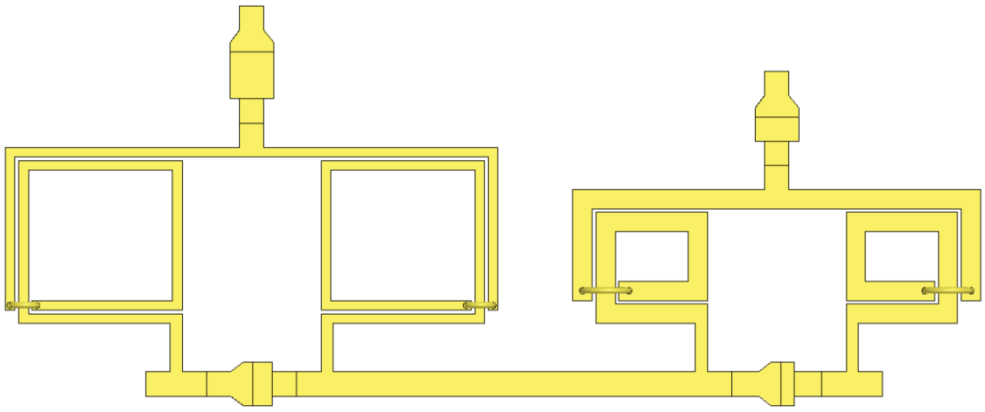


Figure A-11. Upper branch of 2 to 4 GHz phase shifter 45° phase shift bit (Length: 4.014 mm, Width: 1.652 mm, Separation between inductors: 308 µm).

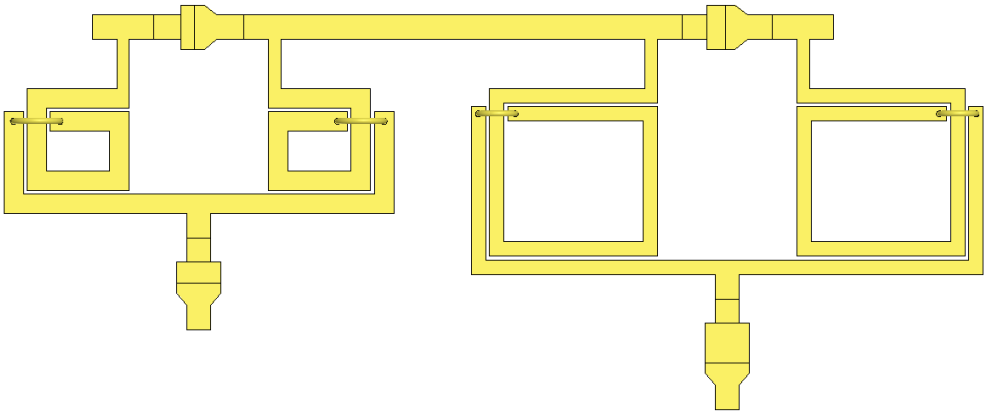


Figure A-12. Lower branch of 2 to 4 GHz phase shifter 45° phase shift bit (Length: 4.006 mm, Width: 1.656 mm, Separation between inductors: 316 µm).

A.4 Design of 22.5° Phase Shift Bit

The final series connected MIM capacitors design related data are given in Table A-13, the layout considered SPSIs are given in Table A-14, and the shunt connected MIM capacitors' final designs are given in Table A-15. The S-parameters graphs of the final layout design are given in Figure A-13, the differential phase shift related graph is given in Figure A-14, with the phase shift related calculation results as in Table A-16. As it can be observed from these results that return loss is around -21 dB, insertion loss is around 1.9 dB at 4 GHz, at worst.

Table A-13. 2 to 4 GHz phase shifter 22.5° phase shift bit finalized series connected MIM capacitor design related geometrical parameter values, and the lumped equivalent model parameter values.

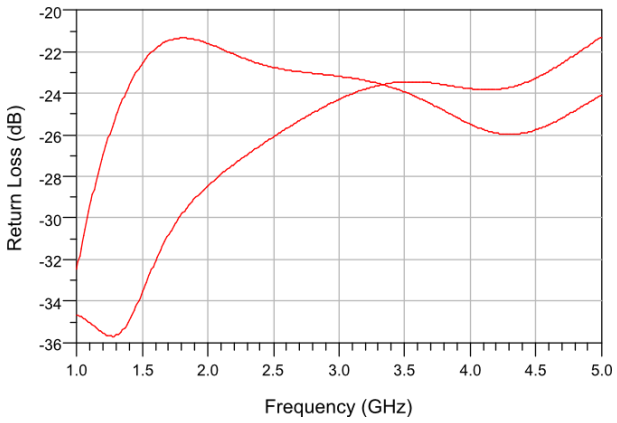
Width (µm)	Length (µm)	L_{feed} (µm)	C (pF)	C_{sh} (fF)	L_s (pH)	R_s (ohm)
100	40	100	0.85	39	368	0.182
100	16	112	0.344	38	397	0.232
100	17	111.5	0.364	38	396	0.227
100	37	101.5	0.788	39	368	0.182

Table A-14. The finalized layout designs of selected SPSIs (extension of 135 µm).

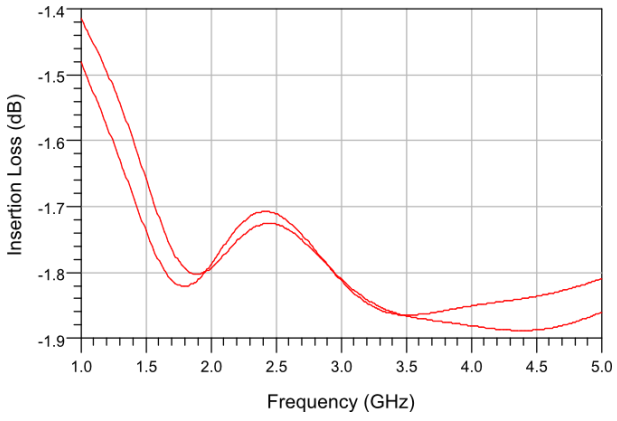
W_{line} (µm)	Spacing (µm)	D_{out} (µm)	L_s (nH)	R_s (ohm)	C_{sh} (fF)	Q_{max}	Q_{ripple}	Q_{min}	Q_{mean}
40	15	716	4.267	1.547	128	39.639	3.524	34.751	38.275
50	10	708	3.938	1.328	131	41.828	3.72	36.699	40.419
50	20	448	1.786	0.822	74	43.603	6.543	32.781	39.324
60	10	448	1.656	0.83	75	39.688	5.492	30.808	36.301

Table A-15. The final design of shunt connected MIM capacitors for 2 to 4 GHz phase shifter 22.5° phase shift bit.

	(pF)	Width (µm)	Length (µm)	C (pF)	C_{sh} (fF)	L_s (pH)	R_s (ohm)
C2_1	3.4	100	147	3.087	47	418	0.199
C2_2	1.32	100	54	1.142	40	372	0.185
C4_1	1.44	100	59	1.257	40	373	0.177
C4_2	3.15	100	139	2.923	46	416	0.199



(a)



(b)

Figure A-13. The 2 to 4 GHz phase shifter 22.5° phase shift bit layout considered, and iterated shunt MIM capacitors; S-parameters graphs for practical case (a) return loss for the practical case, and (b) insertion loss for the practical case.

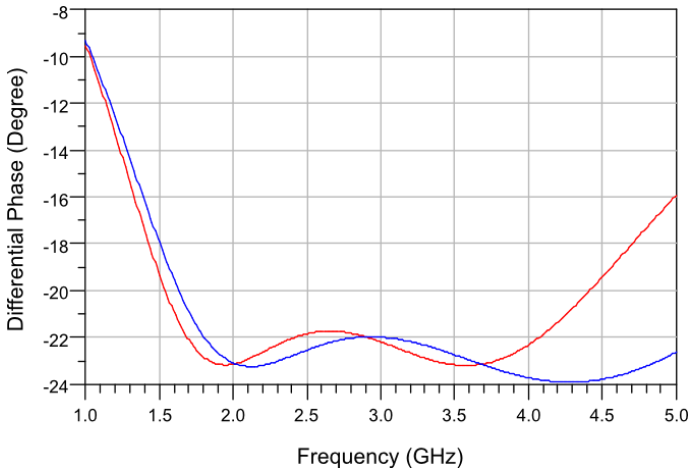


Figure A-14. The differential phase shift response of 2 to 4 GHz phase shifter 22.5° phase shift bit layout considered, and iterated shunt MIM capacitors (red line represents the present case, and blue line represents the ideal case).

Table A-16. Calculated mean phase, minimum phase, rms phase, maximum phase and phase ripple comparison between the ideal case and the finalized layout considerations of 2 to 4 GHz phase shifter 22.5° phase shift bit.

	Min. Phase (°)	**Rms Phase (°)**	**Max. Phase (°)**	**Ripple (°)**
Ideal	21.975	22.691	23.720	1.035
Present case	21.733	22.518	23.199	0.779

Considering the sizes and layout view, one should refer to the following Figure A-15, for the upper branch of 2 to 4 GHz phase shifter 22.5° phase shift bit, and for the lower branch refer to Figure A-16.

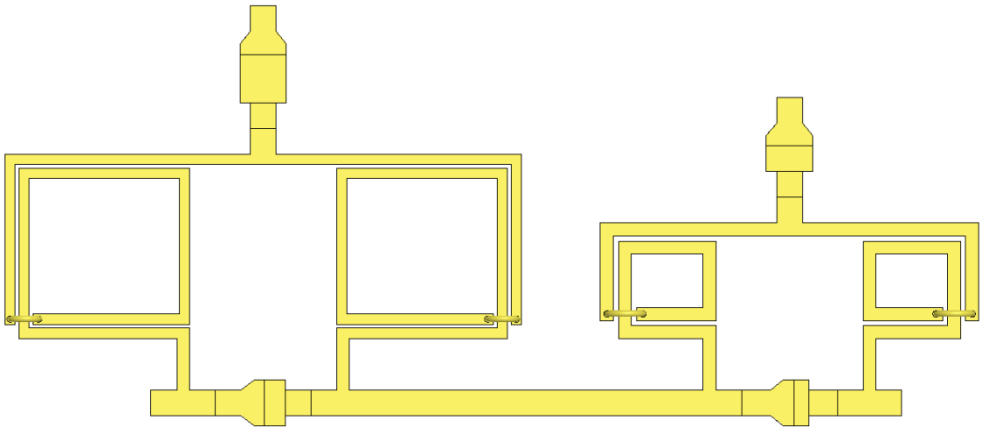


Figure A-15. Upper branch of 2 to 4 GHz phase shifter 22.5° phase shift bit (Length: 3.774 mm, Width: 1.633 mm, Separation between inductors: 306 µm).

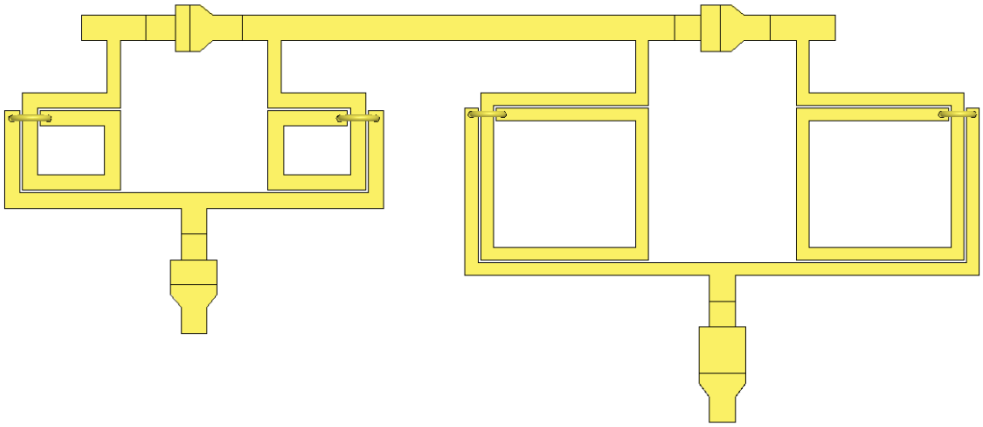


Figure A-16. Lower branch of 2 to 4 GHz phase shifter 22.5° phase shift bit (Length: 3.766 mm, Width: 1.617 mm, Separation between inductors: 314 µm).

APPENDIX B

DESIGN DETAILS OF 3 to 6 GHz PHASE SHIFT BITS

B.1 Design of 180° Phase Shift Bit

The final series connected MIM capacitors design related data are given in Table B-1, the layout considered SPSIs are given in Table B-2, and the shunt connected MIM capacitors' final designs are given in Table B-3. The S-parameters graphs of the final layout design are given in Figure B-1, the differential phase shift related graph is given in Figure B-2, with the phase shift related calculation results as in Table B-4. As it can be observed from these results that return loss is around -16.5 dB, insertion loss is around 2.48 dB at 6 GHz, at worst.

Table B-1. 3 to 6 GHz phase shifter 180° phase shift bit finalized series connected MIM capacitor design related geometrical parameter values, and the lumped equivalent model parameter values.

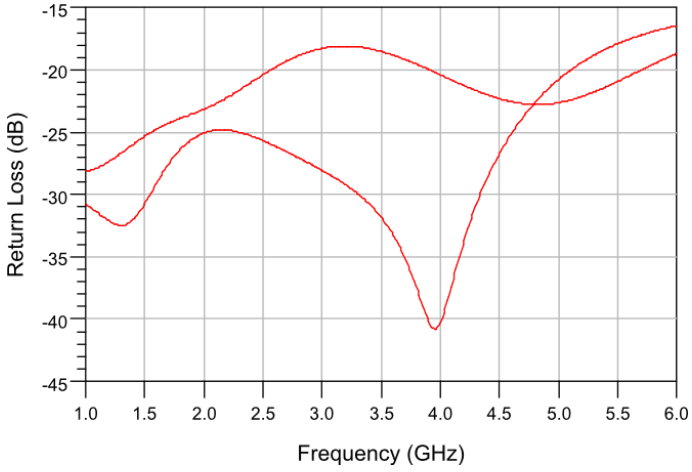
Width (µm)	Length (µm)	L_{feed} (µm)	C (pF)	C_{sh} (fF)	L_s (pH)	R_s (ohm)
100	39	100	0.842	39	363	0.175
100	6	116.5	0.143	38	422	0.408
100	14	112.5	0.31	38	385	0.231
100	19	110	0.414	38	379	0.212

Table B-2. The finalized layout designs of selected SPSIs (extension of 134.5 µm).

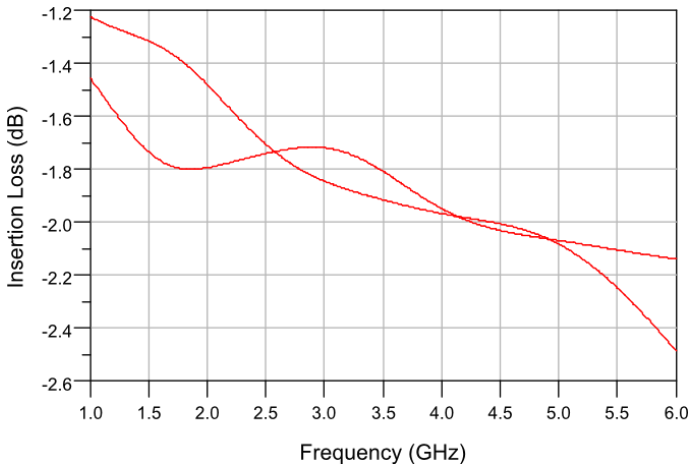
W_{line} (µm)	Spacing (µm)	D_{out} (µm)	L_s (nH)	R_s (ohm)	C_{sh} (fF)	Q_{max}	Q_{ripple}	Q_{min}	Q_{mean}
60	20	330	0.86	0.785	50	24.167	1.212	22.587	23.799
80	20	614	2.149	0.745	116	54.596	8.057	43.239	51.295
120	15	632	1.504	0.72	123	43.692	3.833	38.330	42.164
40	20	714	4.162	1.187	127	51.792	21.959	15.680	37.638

Table B-3. The final design of shunt connected MIM capacitors for 3 to 6 GHz phase shifter 180° phase shift bit.

	(pF)	Width (µm)	Length (µm)	C (pF)	C_{sh} (fF)	L_s (pH)	R_s (ohm)
C2_1	3.33	100	144	3.023	46	420	0.2
C2_2	0.6	100	22	0.478	37	363	0.194
C4_1	1.2	100	42	0.906	40	361	0.183
C4_2	1.67	100	66	1.407	41	373	0.169



(a)



(b)

Figure B-1. The 3 to 6 GHz phase shifter 180° phase shift bit layout considered, and iterated shunt MIM capacitors; S-parameters graphs for practical case (a) return loss for the practical case, and (b) insertion loss for the practical case.

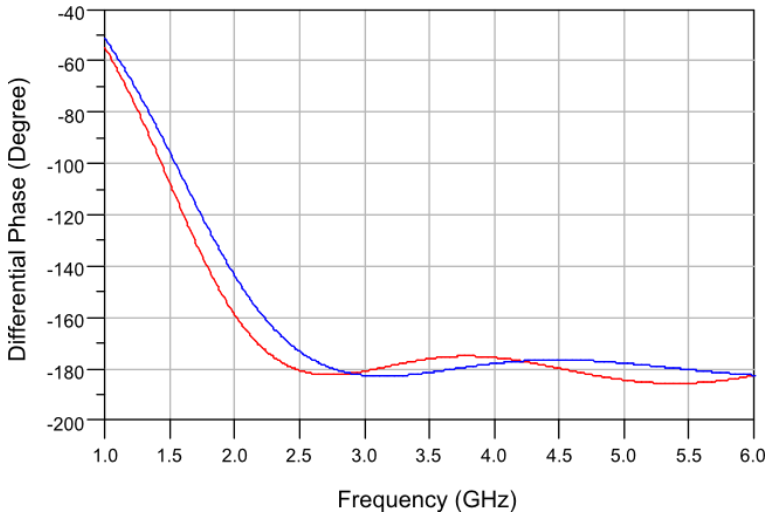


Figure B-2. The differential phase shift response of 3 to 6 GHz phase shifter 180° phase shift bit layout considered, and iterated shunt MIM capacitors (red line represents the present case, and blue line represents the ideal case).

Table B-4. Calculated mean phase, minimum phase, rms phase, maximum phase and phase ripple comparison between the ideal case and the finalized layout considerations of 3 to 6 GHz phase shifter 180° phase shift bit.

	Min. Phase (°)	**Rms Phase (°)**	**Max. Phase (°)**	**Ripple (°)**
Ideal	176.524	179.438	182.876	3.451
Present case	174.807	179.489	183.743	4.656

Considering the sizes and layout view, one should refer to the following Figure B-3, for the upper branch of 3 to 6 GHz phase shifter 180° phase shift bit, and for the lower branch refer to Figure B-4.

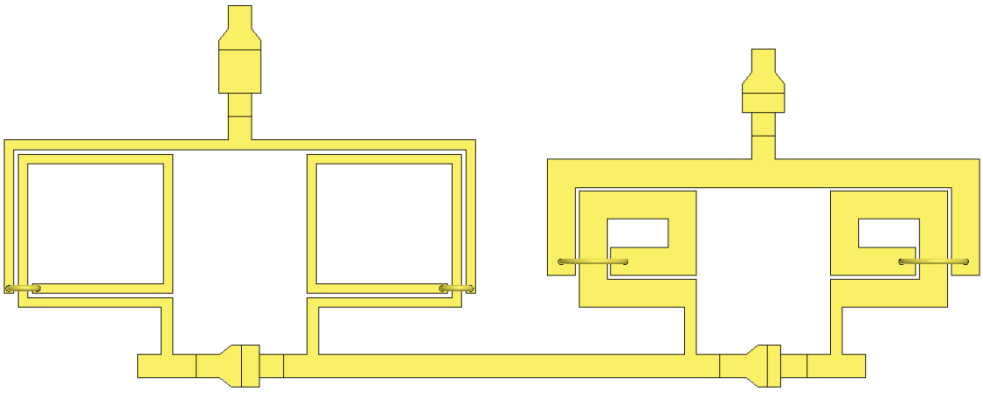


Figure B-3. Upper branch of 3 to 6 GHz phase shifter 180° phase shift bit (Length: 4.134 mm, Width: 1.628 mm, Separation between inductors: 304 µm).

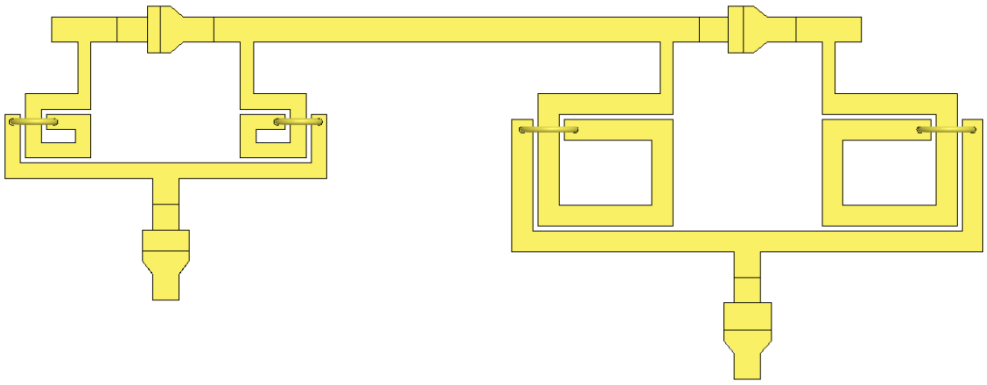


Figure B-4. Lower branch of 3 to 6 GHz phase shifter 180° phase shift bit (Length: 3.732 mm, Width: 1.45 mm, Separation between inductors: 706 µm).

B.2 Design of 90° Phase Shift Bit

The final series connected MIM capacitors design related data are given in Table B-5, the layout considered SPSIs are given in Table B-6 and the shunt connected MIM capacitors' final designs are given in Table B-7. The S-parameters graphs of the final layout design are given in Figure B-5, the differential phase shift related graph is given in Figure B-6, with the phase shift related calculation results as in Table B-8. As it can be observed from these results that return loss is around -15.4 dB, insertion loss is around 2.71 dB at 6 GHz, at worst.

Table B-5. 3 to 6 GHz phase shifter 90° phase shift bit finalized series connected MIM capacitor design related geometrical parameter values, and the lumped equivalent model parameter values.

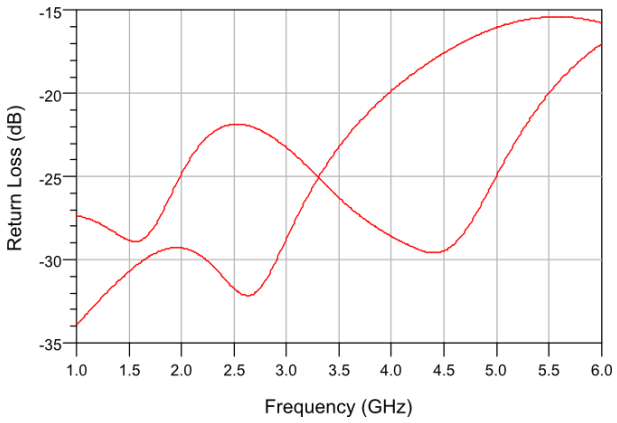
Width (µm)	Length (µm)	L_{feed} (µm)	C (pF)	C_{sh} (fF)	L_s (pH)	R_s (ohm)
100	30	100	0.643	38	364	0.185
100	8	111	0.185	37	405	0.342
100	12	109	0.268	38	388	0.264
100	22	104	0.476	38	373	0.212

Table B-6. The finalized layout designs of selected SPSIs (extension of 130 µm).

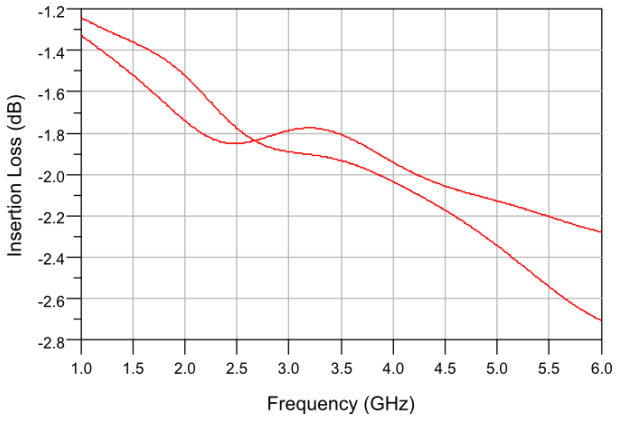
W_{line} (µm)	Spacing (µm)	D_{out} (µm)	L_s (nH)	R_s (ohm)	C_{sh} (fF)	Q_{max}	Q_{ripple}	Q_{min}	Q_{mean}
40	15	586	3.277	1.091	98	49.557	10.653	34.517	45.171
60	20	570	2.376	0.764	100	55.656	6.368	46.82	53.189
120	20	606	1.329	0.753	118	36.39	1.769	33.794	35.563
100	20	466	0.962	0.781	77	27.815	0.828	26.54	27.369

Table B-7. The final design of shunt connected MIM capacitors for 3 to 6 GHz phase shifter 90° phase shift bit.

	(pF)	Width (µm)	Length (µm)	C (pF)	C_{sh} (fF)	L_s (pH)	R_s (ohm)
C2_1	2.61	100	110	2.323	44	400	0.189
C2_2	0.77	100	28	0.604	38	362	0.184
C4_1	1.06	100	37	0.788	38	366	0.176
C4_2	1.89	100	74	1.575	42	378	0.184



(a)



(b)

Figure B-5. The 3 to 6 GHz phase shifter 90° phase shift bit layout considered, and iterated shunt MIM capacitors; S-parameters graphs for practical case (a) return loss for the practical case, and (b) insertion loss for the practical case.

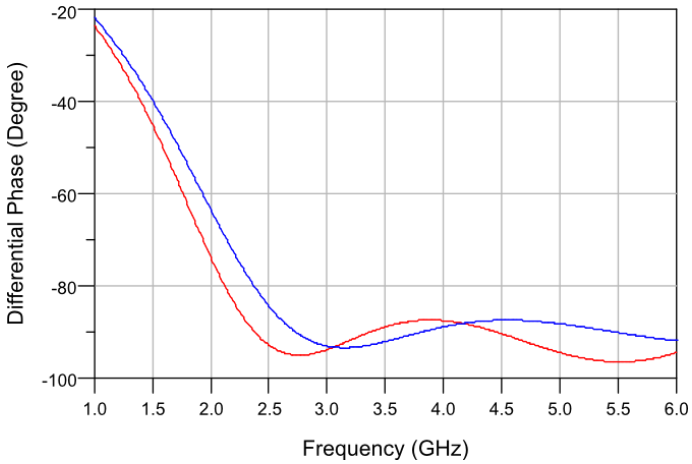


Figure B-6. The differential phase shift response of 3 to 6 GHz phase shifter 90° phase shift bit layout considered, and iterated shunt MIM capacitors (red line represents the present case, and blue line represents the ideal case).

Table B-8. Calculated mean phase, minimum phase, rms phase, maximum phase and phase ripple comparison between the ideal case and the finalized layout considerations of 3 to 6 GHz phase shifter 90° phase shift bit.

	Min. Phase (°)	**Rms Phase (°)**	**Max. Phase (°)**	**Ripple (°)**
Ideal	87.543	90.031	93.546	3.536
Present case	86.056	89.936	93.291	3.844

Considering the sizes and layout view, one should refer to the following Figure B-7, for the upper branch of 3 to 6 GHz phase shifter 90° phase shift bit, and for the lower branch refer to Figure B-8.

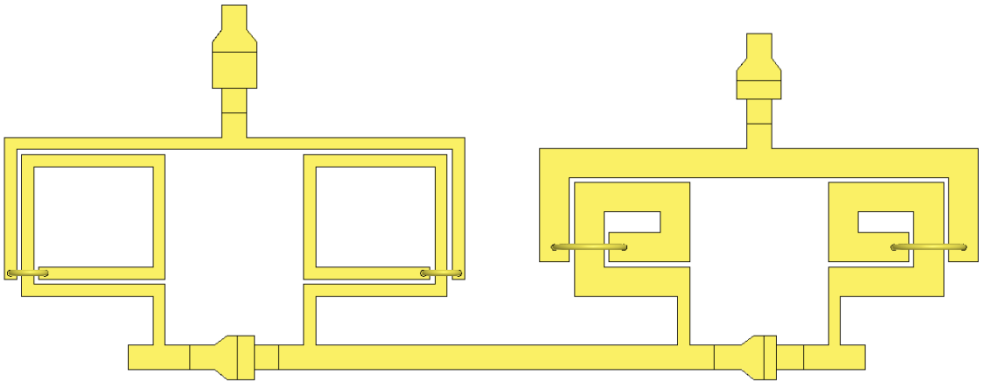


Figure B-7. Upper branch of 3 to 6 GHz phase shifter 90° phase shift bit (Length: 3.936 mm, Width: 1.53 mm, Separation between inductors: 304 µm).

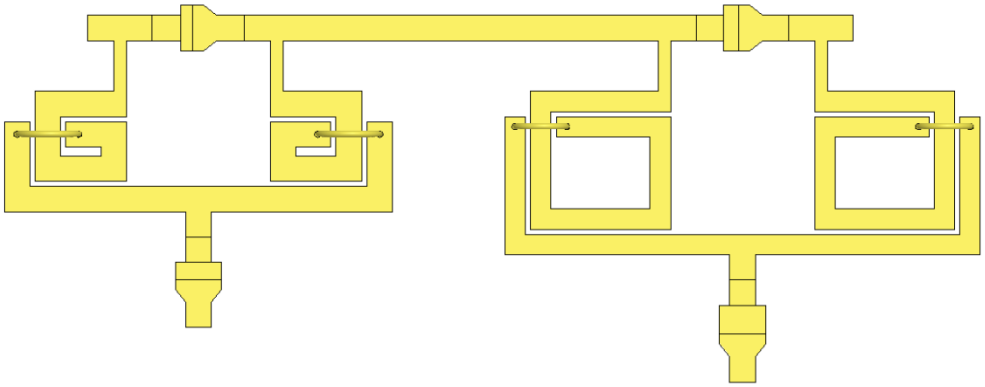


Figure B-8. Lower branch of 3 to 6 GHz phase shifter 90° phase shift bit (Length: 3.802 mm, Width: 1.49 mm, Separation between inductors: 438 µm).

B.3 Design of 45° Phase Shift Bit

The final series connected MIM capacitors design related data are given in Table B-9, the layout considered SPSIs are given in Table B-10, and the shunt connected MIM capacitors' final designs are given in Table B-11. The S-parameters graphs of the final layout design are given in Figure B-9, the differential phase shift related graph is given in Figure B-10, with the phase shift related calculation results as in Table B-12. As it can be observed from these results that return loss is around -18.9 dB, insertion loss is around 2.41 dB at 6 GHz, at worst.

Table B-9. 3 to 6 GHz phase shifter 45° phase shift bit finalized series connected MIM capacitor design related geometrical parameter values, and the lumped equivalent model parameter values.

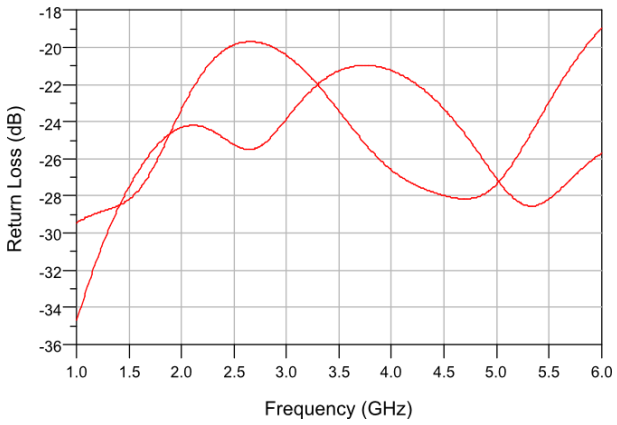
Width (µm)	Length (µm)	L_{feed} (µm)	C (pF)	C_{sh} (fF)	L_s (pH)	R_s (ohm)
100	27	100	0.582	38	363	0.183
100	9	109	0.205	37	398	0.315
100	11	108	0.247	37	391	0.277
100	23	102	0.496	38	371	0.213

Table B-10. The finalized layout designs of selected SPSIs (extension of 128.5 µm).

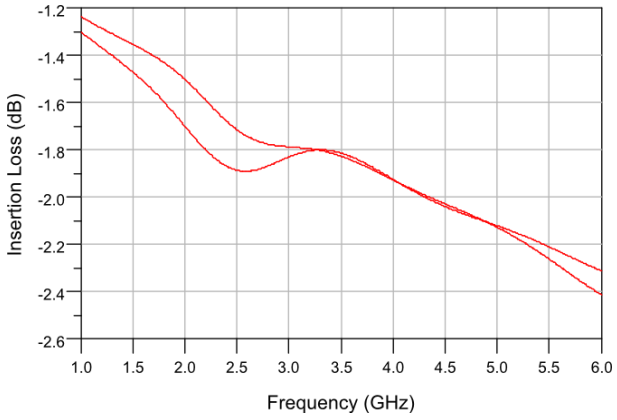
W_{line} (µm)	Spacing (µm)	D_{out} (µm)	L_s (nH)	R_s (ohm)	C_{sh} (fF)	Q_{max}	Q_{ripple}	Q_{min}	Q_{mean}
50	20	610	2.986	0.868	106	55.454	11.363	39.510	50.872
100	15	746	2.531	0.908	159	46.272	13.896	24.694	38.590
120	15	584	1.241	0.798	110	33.101	1.394	31.015	32.409
120	20	548	1.073	0.775	96	31.277	1.851	28.651	30.502

Table B-11. The final design of shunt connected MIM capacitors for 3 to 6 GHz phase shifter 45° phase shift bit.

	(pF)	Width (µm)	Length (µm)	C (pF)	C_{sh} (fF)	L_s (pH)	R_s (ohm)
C2_1	2.37	100	100	2.11	44	392	0.19
C2_2	0.84	100	27	0.582	38	363	0.183
C4_1	0.99	100	34	0.725	38	365	0.187
C4_2	2.03	100	79	1.672	42	383	0.189



(a)



(b)

Figure B-9. The 3 to 6 GHz phase shifter 45° phase shift bit layout considered, and iterated shunt MIM capacitors; S-parameters graphs for practical case (a) return loss for the practical case, and (b) insertion loss for the practical case.

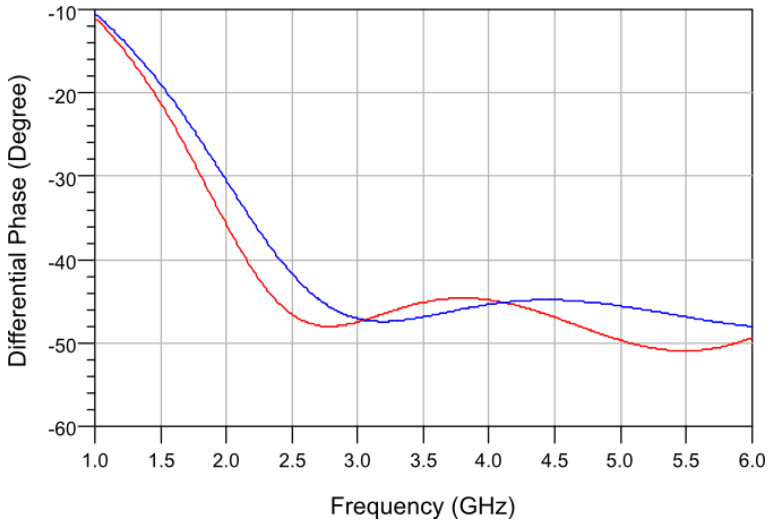


Figure B-10. The differential phase shift response of 3 to 6 GHz phase shifter 45° phase shift bit layout considered, and iterated shunt MIM capacitors (red line represents the present case, and blue line represents the ideal case).

Table B-12. Calculated mean phase, minimum phase, rms phase, maximum phase and phase ripple comparison between the ideal case and the finalized layout considerations of 3 to 6 GHz phase shifter 45° phase shift bit.

	Min. Phase (°)	**Rms Phase (°)**	**Max. Phase (°)**	**Ripple (°)**
Ideal	44.857	46.223	48.026	1.814
Present case	44.074	46.484	48.778	2.381

Considering the sizes and layout view, one should refer to the following Figure B-11, for the upper branch of 3 to 6 GHz phase shifter 45° phase shift bit, and for the lower branch refer to Figure B-12.

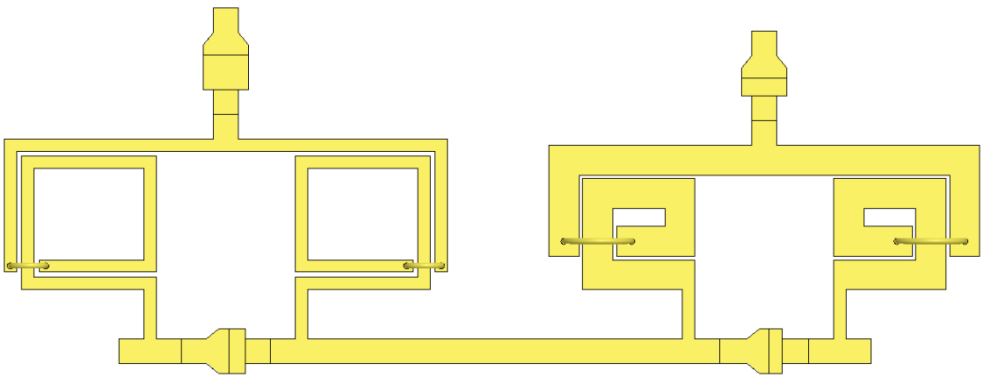


Figure B-11. Upper branch of 3 to 6 GHz phase shifter 45° phase shift bit (Length: 3.908 mm, Width: 1.48 mm, Separation between inductors: 406 µm).

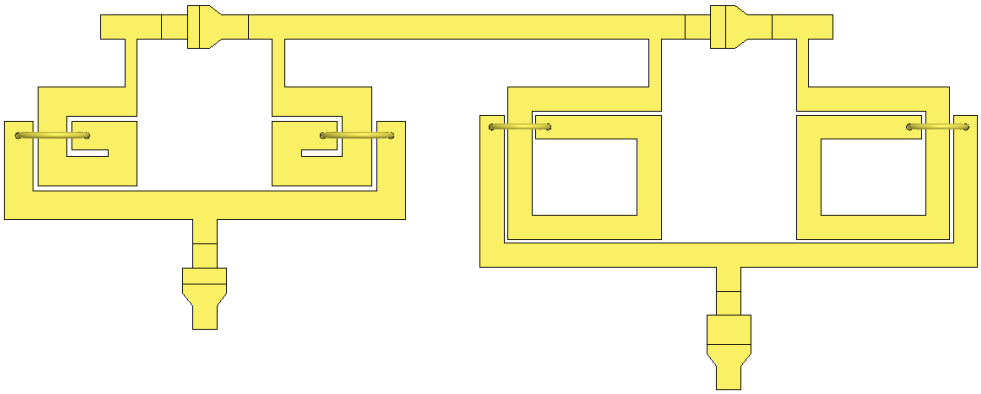


Figure B-12. Lower branch of 3 to 6 GHz phase shifter 45° phase shift bit (Length: 4.008 mm, Width: 1.595 mm, Separation between inductors: 306 µm).

B.4 Design of 22.5° Phase Shift Bit

The final series connected MIM capacitors design related data are given in Table B-13, the layout considered SPSIs are given in Table B-14, and the shunt connected MIM capacitors' final designs are given in Table B-15. The S-parameters graphs of the final layout design are given in Figure B-13, the differential phase shift related graph is given in Figure B-14, with the phase shift related calculation results as in Table B-16. As it can be observed from these results that return loss is around -18.3 dB, insertion loss is around 2.42 dB at 6 GHz, at worst.

Table B-13. 3 to 6 GHz phase shifter 22.5° phase shift bit finalized series connected MIM capacitor design related geometrical parameter values, and the lumped equivalent model parameter values.

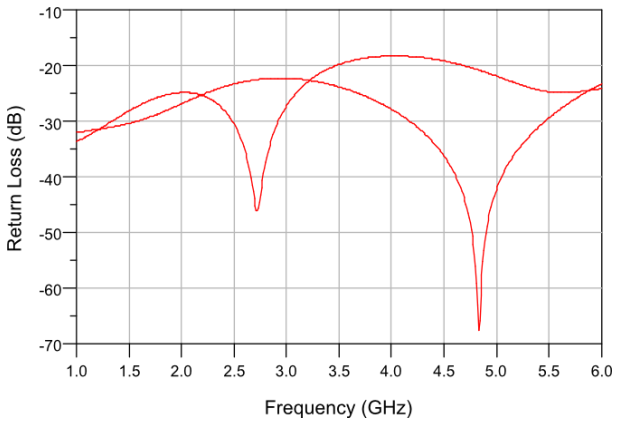
Width (µm)	Length (µm)	L_{feed} (µm)	C (pF)	C_{sh} (fF)	L_s (pH)	R_s (ohm)
100	26	100	0.559	38	363	0.19
100	10	108	0.227	38	392	0.291
100	11	107.5	0.247	37	388	0.28
100	25	100.5	0.539	38	368	0.208

Table B-14. The finalized layout designs of selected SPSIs (extension of 128 µm).

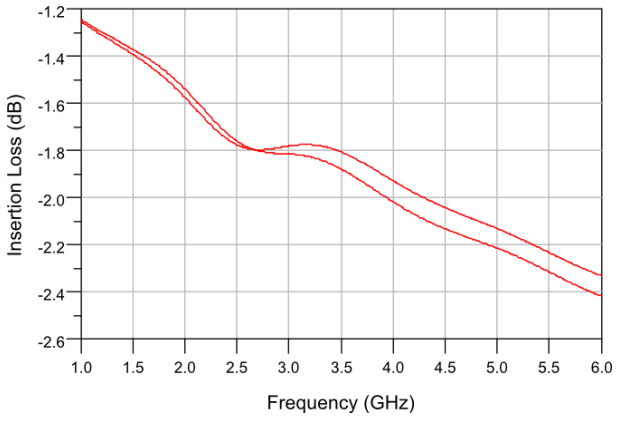
W_{line} (µm)	Spacing (µm)	D_{out} (µm)	L_s (nH)	R_s (ohm)	C_{sh} (fF)	Q_{max}	Q_{ripple}	Q_{min}	Q_{mean}
80	20	724	2.823	0.790	149	58.298	19.376	27.115	46.491
100	15	754	2.611	0.826	163	53.337	18.000	24.799	42.799
120	20	580	1.203	0.723	108	36.635	2.480	33.140	35.620
120	20	556	1.092	0.777	101	30.070	1.176	28.355	29.532

Table B-15. The final design of shunt connected MIM capacitors for 3 to 6 GHz phase shifter 22.5° phase shift bit.

	(pF)	Width (µm)	Length (µm)	C (pF)	C_{sh} (fF)	L_s (pH)	R_s (ohm)
C2_1	2.27	100	92	1.943	43	389	0.183
C2_2	0.88	100	31	0.665	38	364	0.187
C4_1	0.95	100	33	0.708	38	363	0.183
C4_2	2.1	100	80	1.694	42	383	0.19



(a)



(b)

Figure B-13. The 3 to 6 GHz phase shifter 22.5° phase shift bit layout considered, and iterated shunt MIM capacitors; S-parameters graphs for practical case (a) return loss for the practical case, and (b) insertion loss for the practical case.

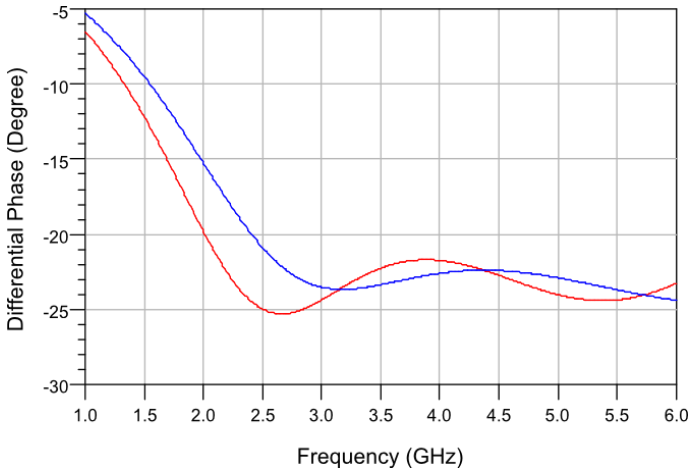


Figure B-14. The differential phase shift response of 3 to 6 GHz phase shifter 22.5° phase shift bit layout considered, and iterated shunt MIM capacitors (red line represents the present case, and blue line represents the ideal case).

Table B-16. Calculated mean phase, minimum phase, rms phase, maximum phase and phase ripple comparison between the ideal case and the finalized layout considerations of 3 to 6 GHz phase shifter 22.5° phase shift bit.

	Min. Phase (°)	**Rms Phase (°)**	**Max. Phase (°)**	**Ripple (°)**
Ideal	22.404	23.178	24.403	1.233
Present case	20.779	22.454	23.985	1.645

Considering the sizes and layout view, one should refer to the following Figure B-15, for the upper branch of 3 to 6 GHz phase shifter 22.5° phase shift bit, and for the lower branch refer to Figure B-16.

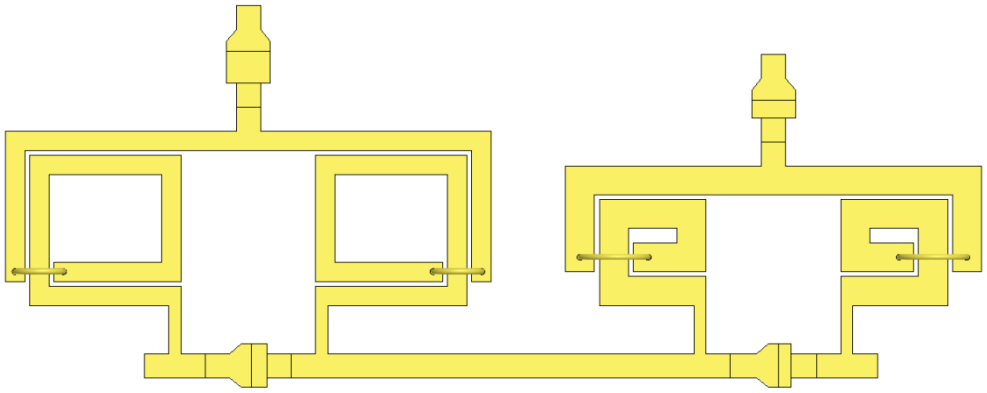


Figure B-15. Upper branch of 3 to 6 GHz phase shifter 22.5° phase shift bit (Length: 4.026 mm, Width: 1.546 mm, Separation between inductors: 306 µm).

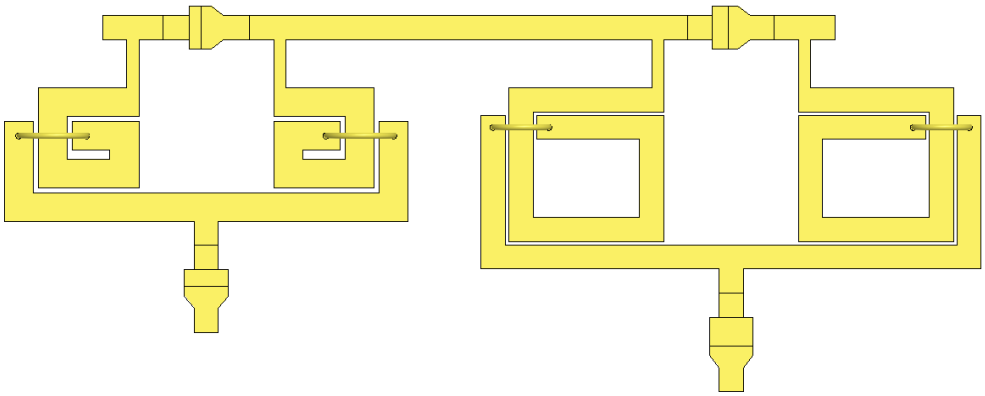


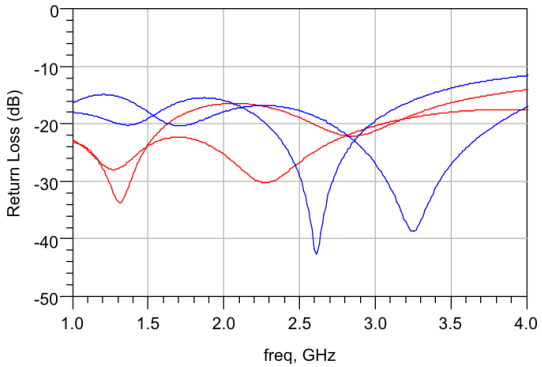
Figure B-16. Lower branch of 3 to 6 GHz phase shifter 22.5° phase shift bit (Length: 4.032 mm, Width: 1.604 mm, Separation between inductors: 300 µm).

APPENDIX C

LAST FABRICATED AND MEASURED SAMPLES

In this section, the last fabricated and measured phase shift bit variations are presented. From 36 variations, 32 variations are measured.

1 to 2 GHz Phase Shifter 180° M



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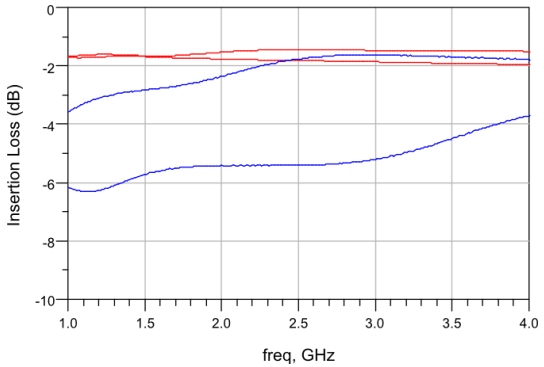

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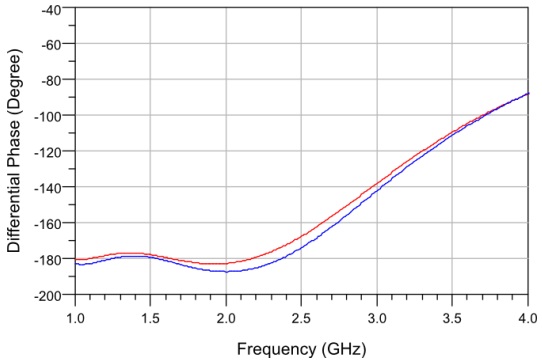
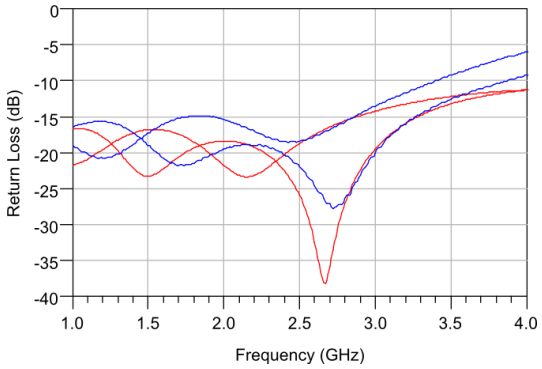


Differential Phase

Differential Phase Related Calculations

	RMS Phase (°)	RMS PE (°)	Max. PE (°)	Max IL (dB)	Min RL (dB)
Ideal	180.23	2.17	3.42	-	-
Practical	180.05	2.12	3.18	1.76	16.49
Measurement	182.59	2.85	5.01	6.31	14.89

1 to 2 GHz Phase Shifter 180° DCM



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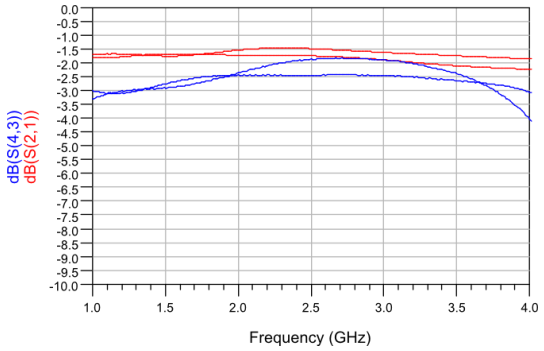

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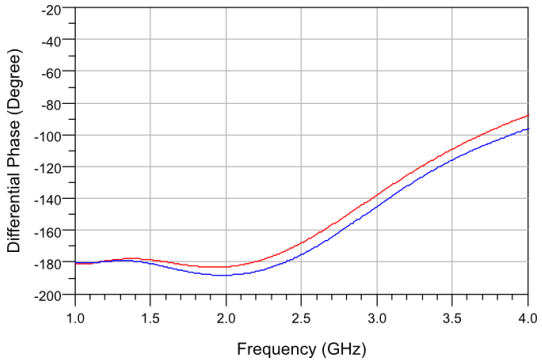
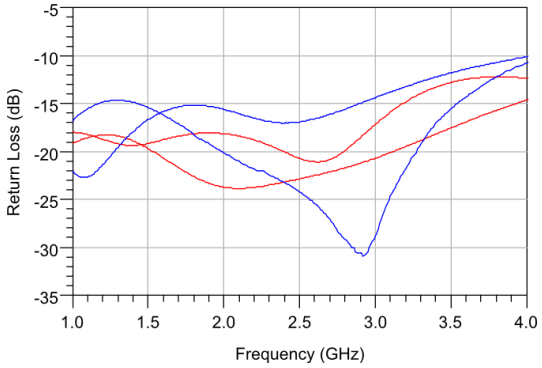


Differential Phase

Differential Phase Related Calculations

	RMS Phase (°)	RMS PE (°)	Max. PE (°)	Max IL (dB)	Min RL (dB)
Ideal	180.23	2.17	3.42	-	-
Practical	180.45	1.85	2.80	1.83	16.64
Measurement	182.80	3.31	5.53	3.32	14.86

1 to 2 GHz Phase Shifter 180° DCF



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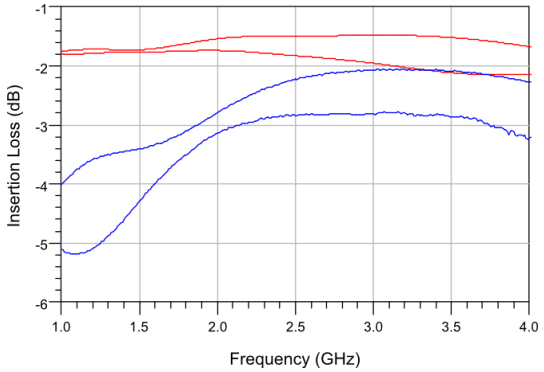

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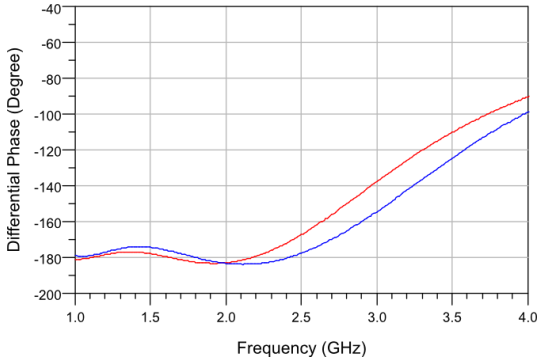
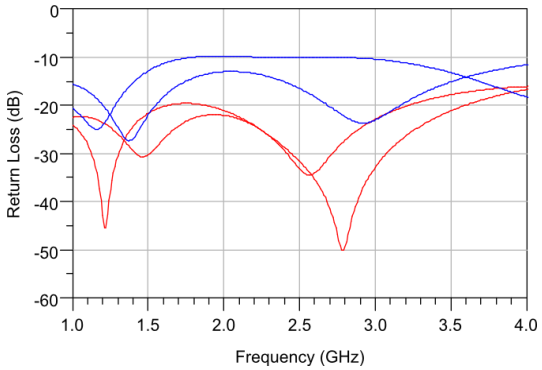


Differential Phase

Differential Phase Related Calculations

	RMS Phase (°)	RMS PE (°)	Max. PE (°)	Max IL (dB)	Min RL (dB)
Ideal	180.23	2.17	3.42	-	-
Practical	180.20	2.21	3.30	1.8	18
Measurement	177.90	2.81	5.61	5.19	14.65

1 to 2 GHz Phase Shifter 90° M



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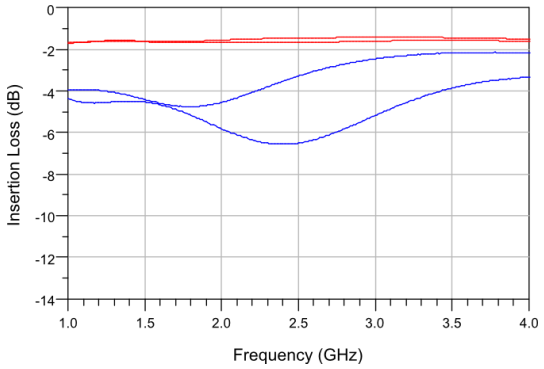

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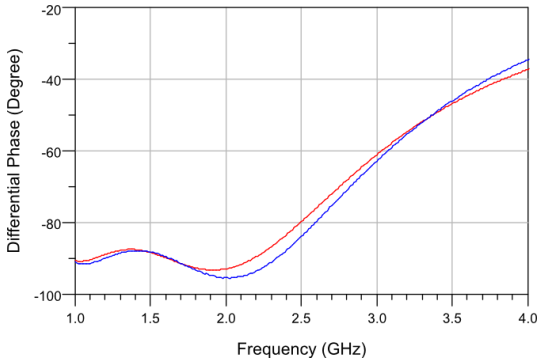
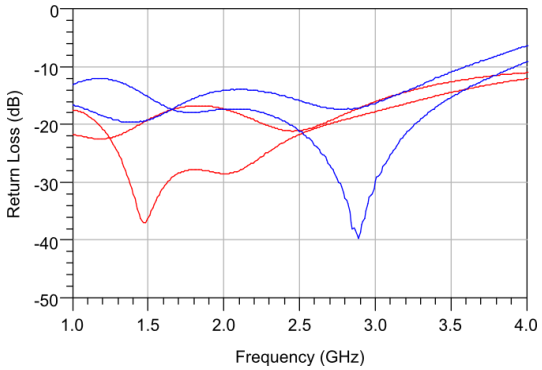


Differential Phase

Differential Phase Related Calculations

	RMS Phase (°)	RMS PE (°)	Max. PE (°)	Max IL (dB)	Min RL (dB)
Ideal	90.01	2.35	4.72	-	-
Practical	90.32	1.98	3.02	1.70	19.60
Measurement	90.96	2.38	4.66	5.81	9.81

1 to 2 GHz Phase Shifter 90° DCM



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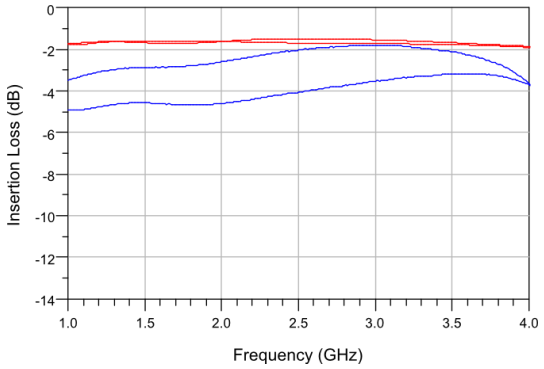

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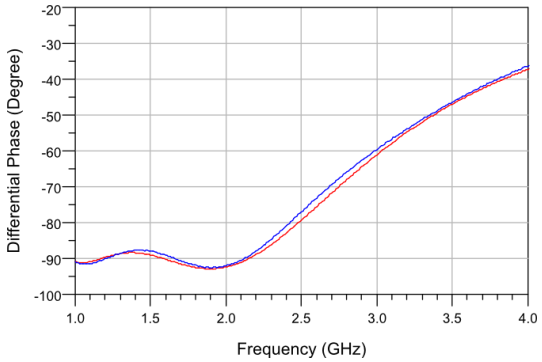
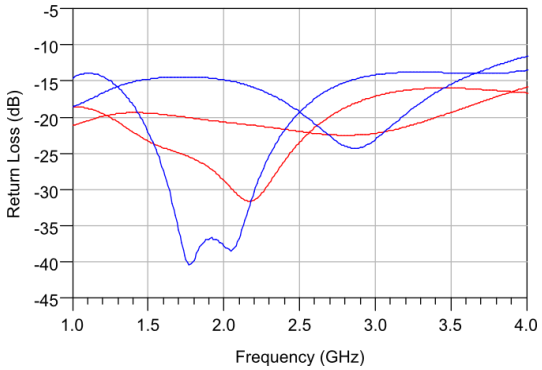


Differential Phase

Differential Phase Related Calculations

	RMS Phase (°)	RMS PE (°)	Max. PE (°)	Max IL (dB)	Min RL (dB)
Ideal	90.01	2.35	4.72	-	-
Practical	90.70	1.54	2.28	1.78	16.74
Measurement	90.31	1.67	2.54	4.68	12.82

1 to 2 GHz Phase Shifter 90° DCF



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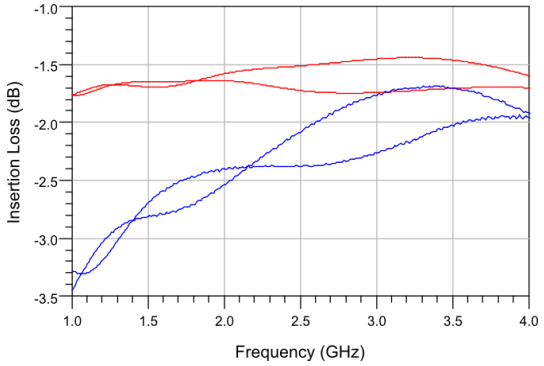

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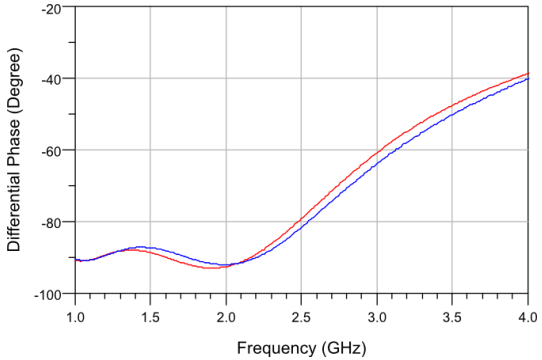
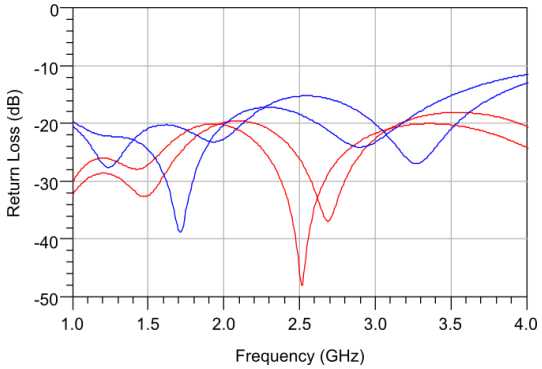


Differential Phase

Differential Phase Related Calculations

	RMS Phase (°)	RMS PE (°)	Max. PE (°)	Max IL (dB)	Min RL (dB)
Ideal	90.01	2.35	4.72	-	-
Practical	90.48	1.73	2.61	1.77	18.61
Measurement	89.55	1.60	2.59	3.45	13.94

1 to 2 GHz Phase Shifter 45° M



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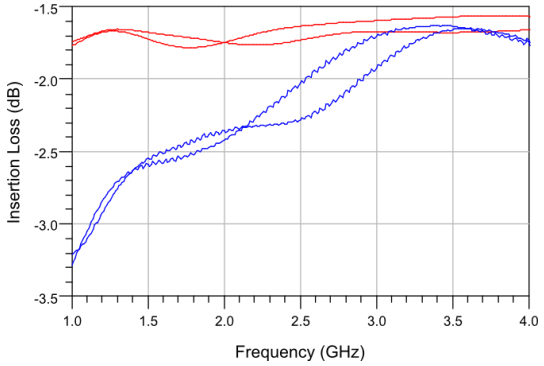

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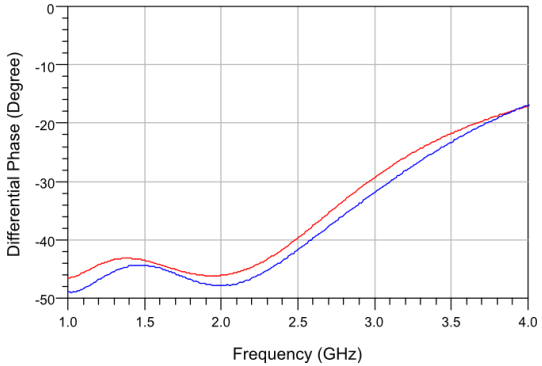
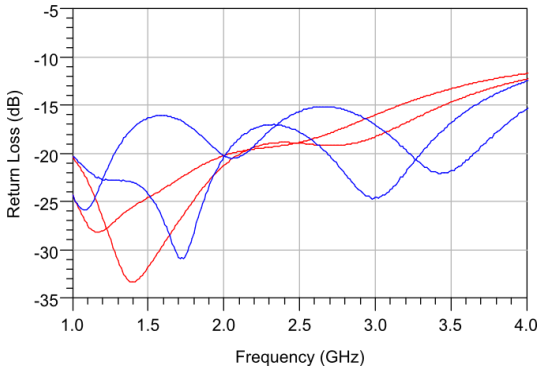


Differential Phase

Differential Phase Related Calculations

	RMS Phase (°)	RMS PE (°)	Max. PE (°)	Max IL (dB)	Min RL (dB)
Ideal	45.24	1.04	1.59	-	-
Practical	44.82	1.13	1.81	1.78	19.83
Measurement	46.38	1.47	2.70	3.29	19.68

1 to 2 GHz Phase Shifter 45° DCM



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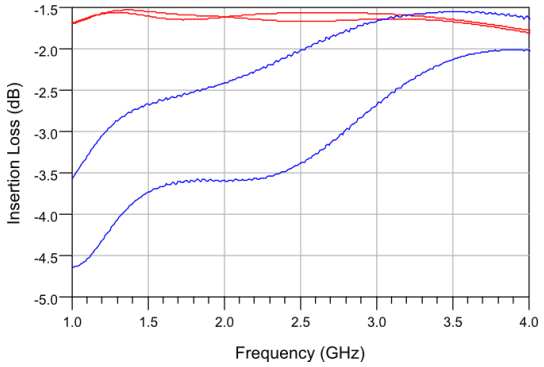

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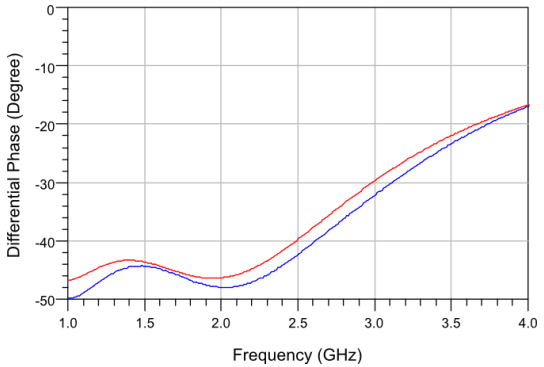
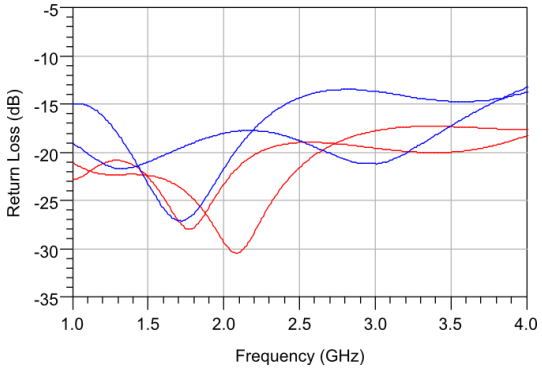


Differential Phase

Differential Phase Related Calculations

	RMS Phase (°)	RMS PE (°)	Max. PE (°)	Max IL (dB)	Min RL (dB)
Ideal	45.24	1.04	1.59	-	-
Practical	45.02	1.16	1.79	1.69	20.25
Measurement	46.51	1.68	3.46	4.64	16.08

1 to 2 GHz Phase Shifter 45° DCF



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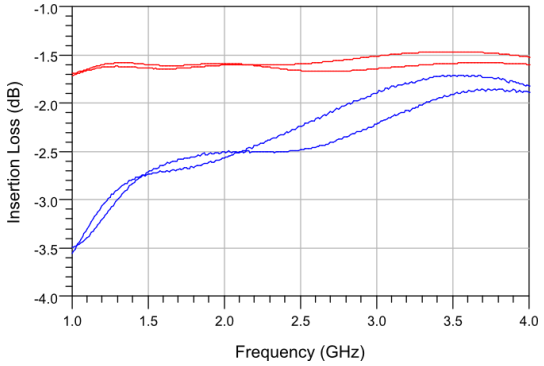

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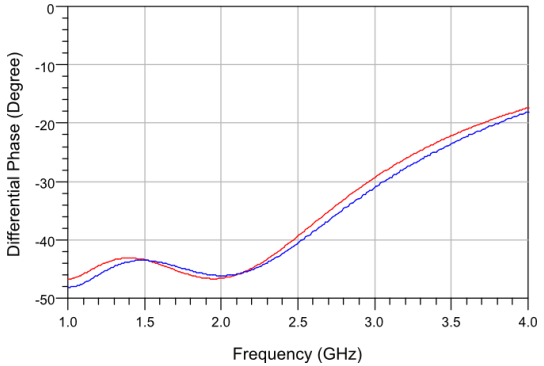
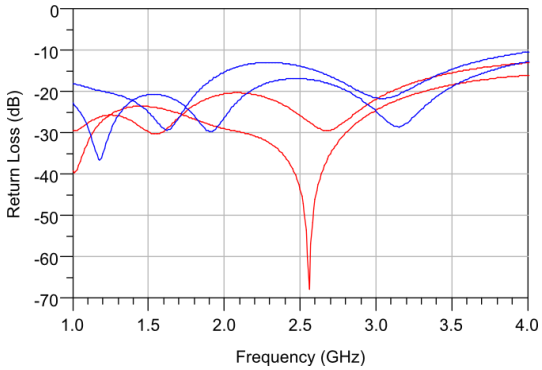


Differential Phase

Differential Phase Related Calculations

	RMS Phase (°)	RMS PE (°)	Max. PE (°)	Max IL (dB)	Min RL (dB)
Ideal	45.24	1.04	1.59	-	-
Practical	44.98	1.30	1.86	1.71	20.84
Measurement	45.27	1.37	2.97	3.55	14.95

1 to 2 GHz Phase Shifter 22.5° M



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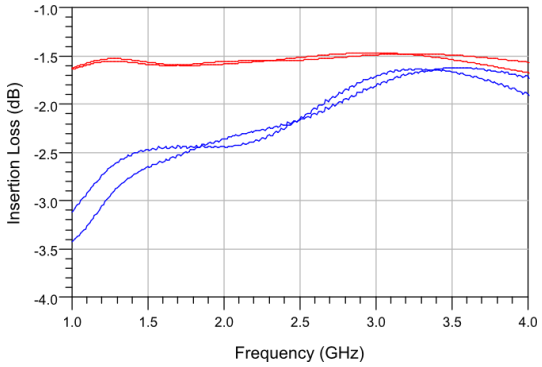

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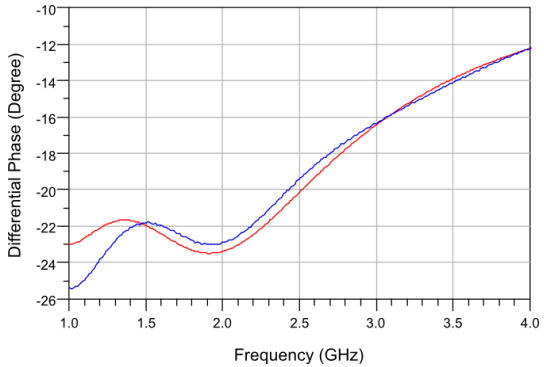
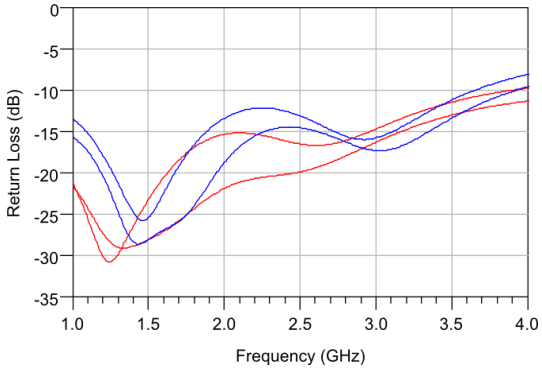


Differential Phase

Differential Phase Related Calculations

	RMS Phase (°)	RMS PE (°)	Max. PE (°)	Max IL (dB)	Min RL (dB)
Ideal	23.35	0.53	0.96	-	-
Practical	22.57	0.64	0.93	1.64	20.57
Measurement	23.02	1.07	2.44	3.42	15.31

1 to 2 GHz Phase Shifter 22.5° DCM



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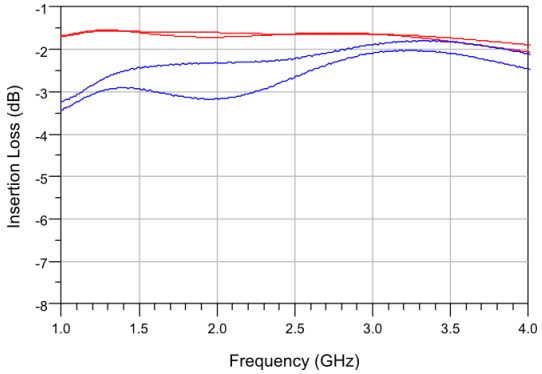

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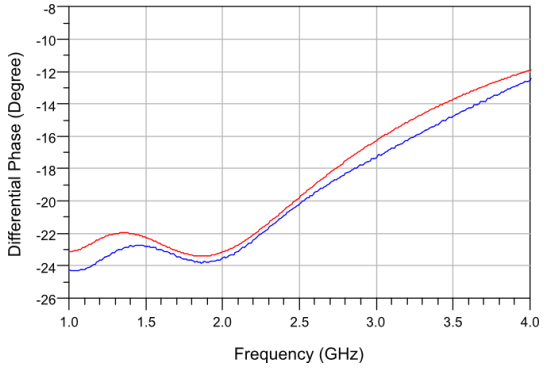
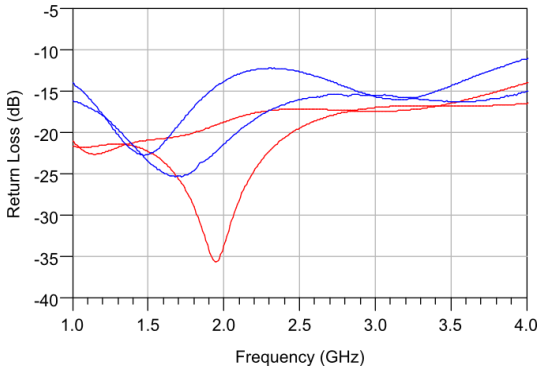


Differential Phase

Differential Phase Related Calculations

	RMS Phase (°)	RMS PE (°)	Max. PE (°)	Max IL (dB)	Min RL (dB)
Ideal	23.35	0.53	0.96	-	-
Practical	22.73	0.50	0.75	1.71	15.31
Measurement	23.47	0.48	0.88	3.43	13.38

1 to 2 GHz Phase Shifter 22.5° DCF



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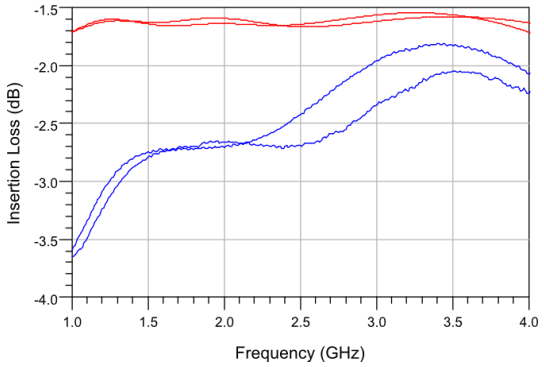

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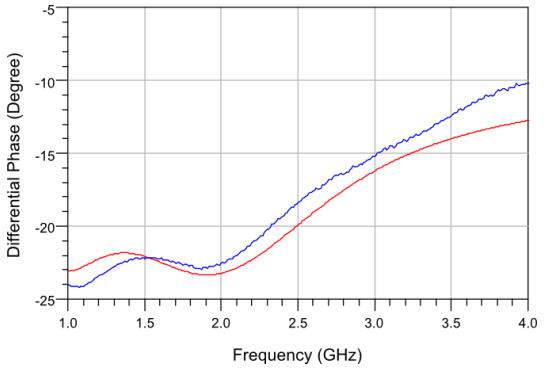
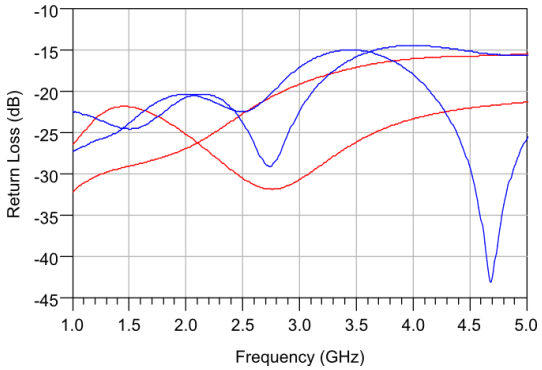


Differential Phase

Differential Phase Related Calculations

	RMS Phase (°)	RMS PE (°)	Max. PE (°)	Max IL (dB)	Min RL (dB)
Ideal	23.35	0.53	0.96	-	-
Practical	22.62	0.53	0.76	1.71	20.84
Measurement	22.87	0.63	1.37	3.65	13.79

2 to 4 GHz Phase Shifter 180° M



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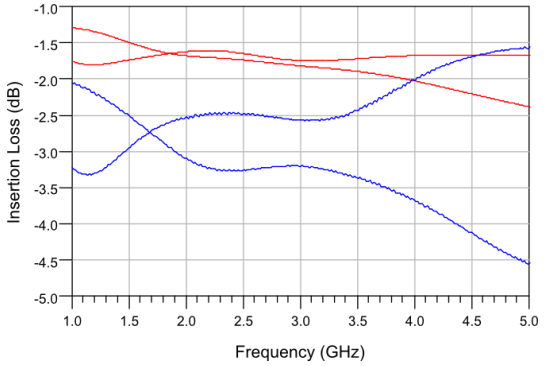

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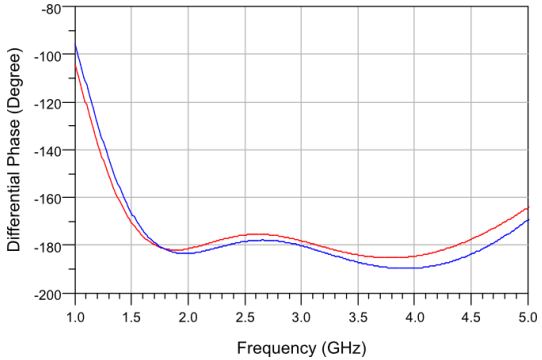
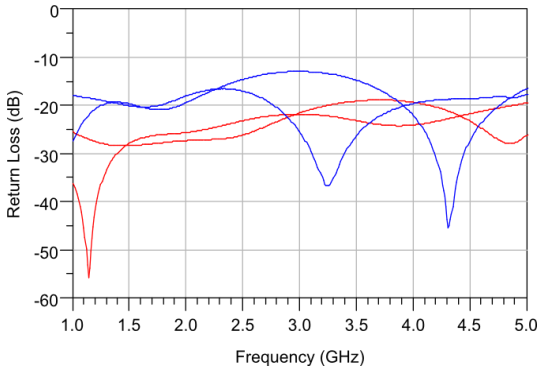


Differential Phase

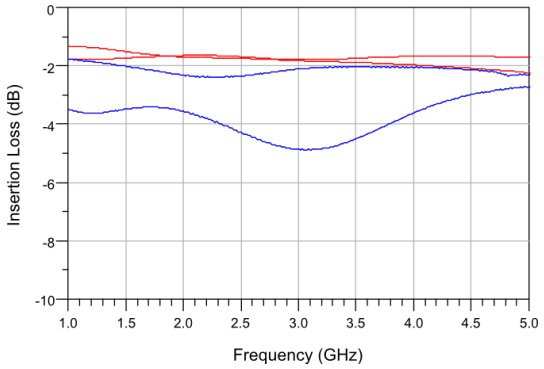
Differential Phase Related Calculations

	RMS Phase (°)	RMS PE (°)	Max. PE (°)	Max IL (dB)	Min RL (dB)
Ideal	178.50	2.19	3.79	-	-
Practical	180.30	3.55	5.08	2.03	16.03
Measurement	183.17	4.13	6.65	3.69	14.41

2 to 4 GHz Phase Shifter 180° DCM



Return Loss



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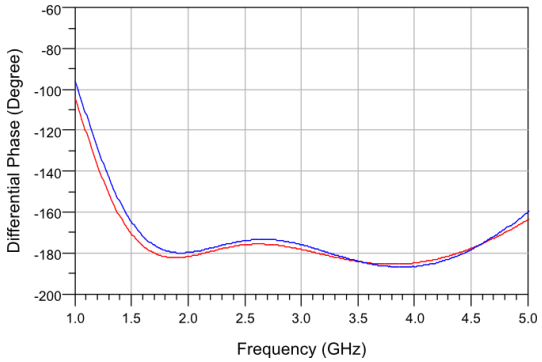
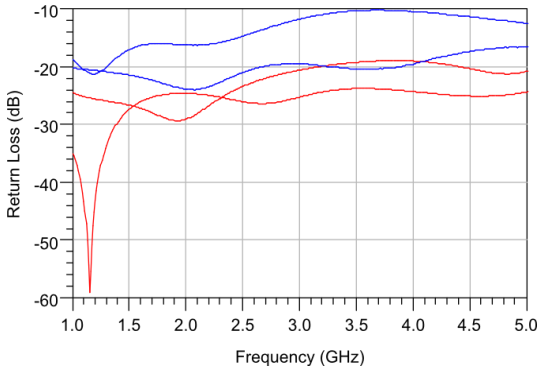


Differential Phase

Differential Phase Related Calculations

	RMS Phase (°)	RMS PE (°)	Max. PE (°)	Max IL (dB)	Min RL (dB)
Ideal	178.50	2.19	3.79	-	-
Practical	180.46	3.52	5.09	1.96	18.92
Measurement	179.37	4.74	7.59	4.88	12.94

2 to 4 GHz Phase Shifter 180° DCF



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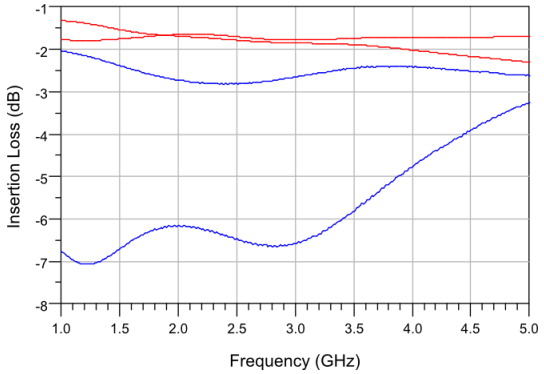

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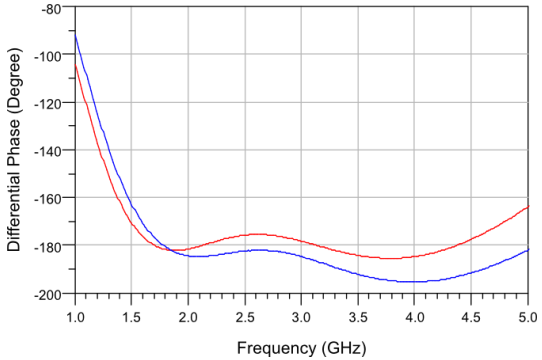
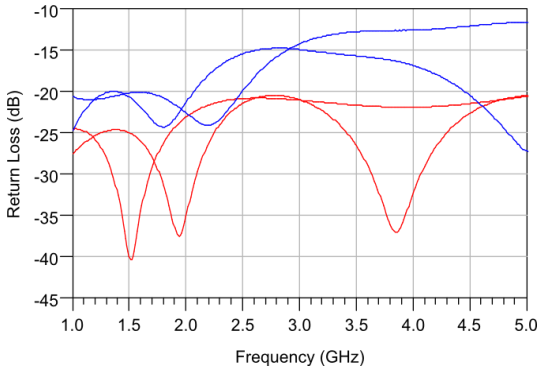


Differential Phase

Differential Phase Related Calculations

	RMS Phase (°)	RMS PE (°)	Max. PE (°)	Max IL (dB)	Min RL (dB)
Ideal	178.50	2.19	3.79	-	-
Practical	180.43	3.59	5.12	2.02	18.95
Measurement	187.50	4.75	8.03	6.66	10.20

2 to 4 GHz Phase Shifter 90° M



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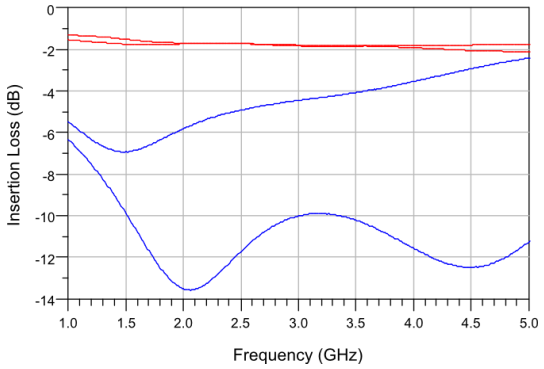

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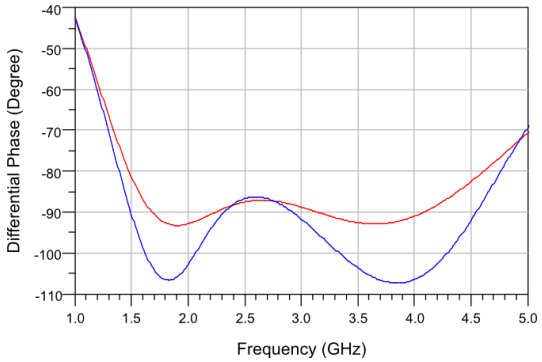
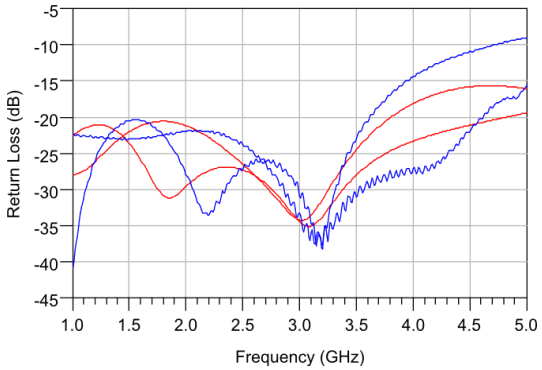


Differential Phase

Differential Phase Related Calculations

	RMS Phase (°)	RMS PE (°)	Max. PE (°)	Max IL (dB)	Min RL (dB)
Ideal	90.31	1.87	3.11	-	-
Practical	90.26	2.06	3.12	1.92	20.48
Measurement	96.66	7.52	11.03	13.58	12.56

2 to 4 GHz Phase Shifter 90° DCM



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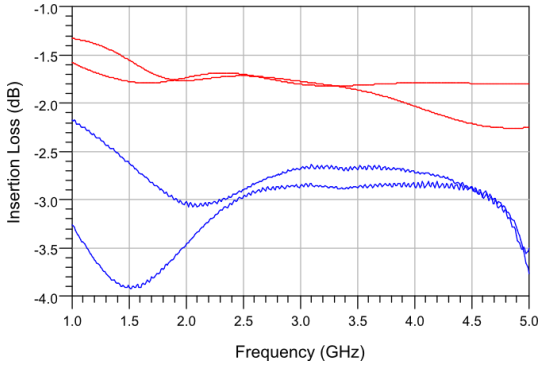

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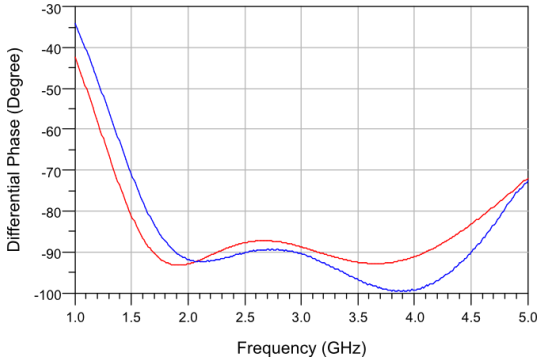
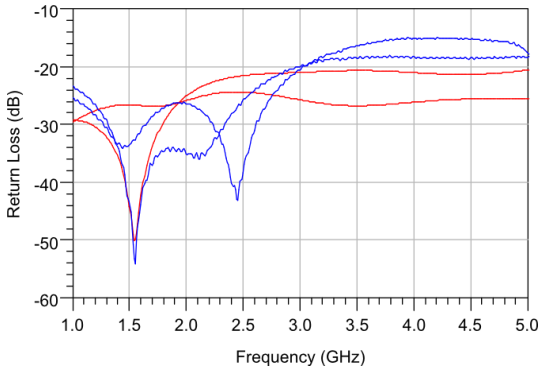


Differential Phase

Differential Phase Related Calculations

	RMS Phase (°)	RMS PE (°)	Max. PE (°)	Max IL (dB)	Min RL (dB)
Ideal	90.31	1.87	3.11	-	-
Practical	90.31	2.00	3.04	2.03	18.13
Measurement	93.47	3.55	6.30	3.46	14.39

2 to 4 GHz Phase Shifter 45° M



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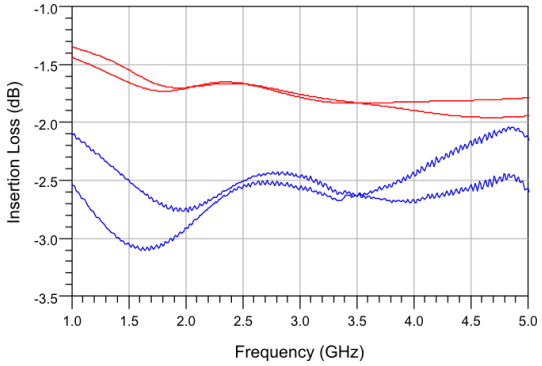

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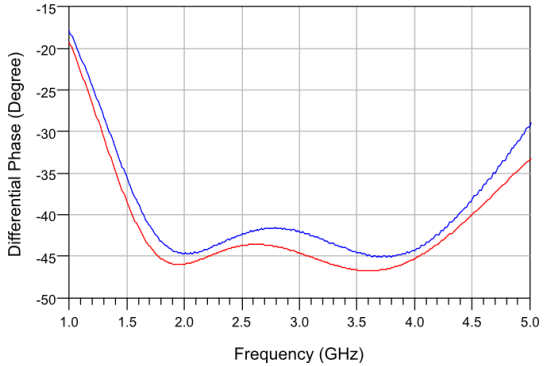
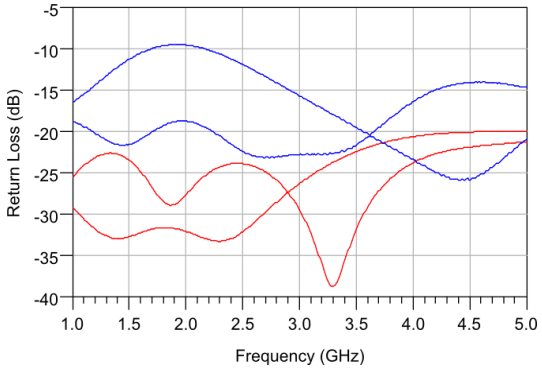


Differential Phase

Differential Phase Related Calculations

	RMS Phase (°)	RMS PE (°)	Max. PE (°)	Max IL (dB)	Min RL (dB)
Ideal	44.50	1.16	2.22	-	-
Practical	45.21	1.09	1.63	1.90	20.66
Measurement	43.43	1.21	1.86	2.91	14.99

2 to 4 GHz Phase Shifter 45° DCM



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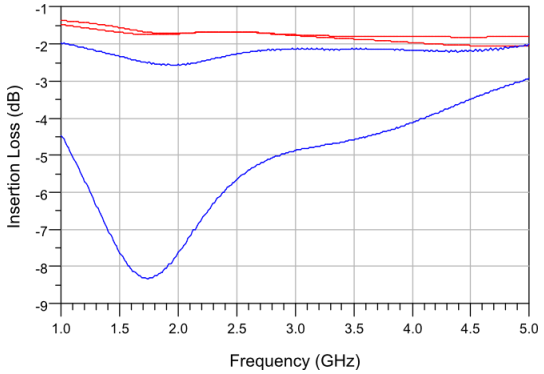

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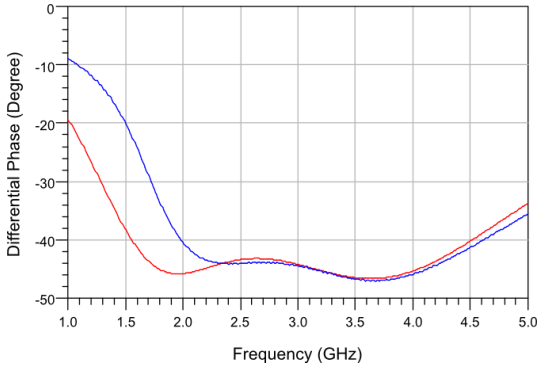
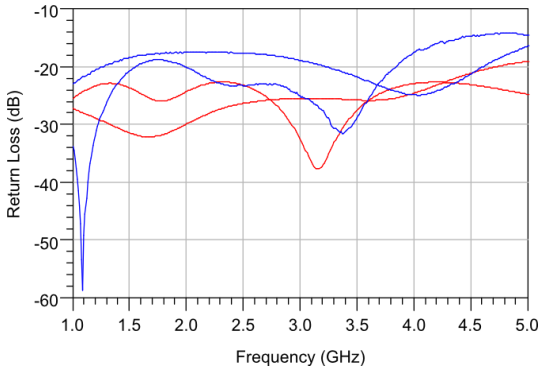


Differential Phase

Differential Phase Related Calculations

	RMS Phase (°)	RMS PE (°)	Max. PE (°)	Max IL (dB)	Min RL (dB)
Ideal	44.50	1.16	2.22	-	-
Practical	45.01	1.20	1.77	1.96	20.61
Measurement	44.97	1.50	4.44	7.61	9.53

2 to 4 GHz Phase Shifter 45° DCF



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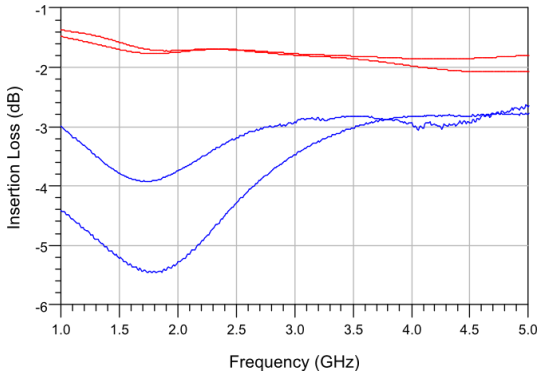

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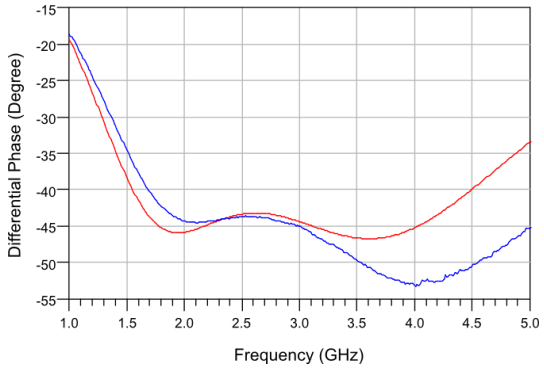
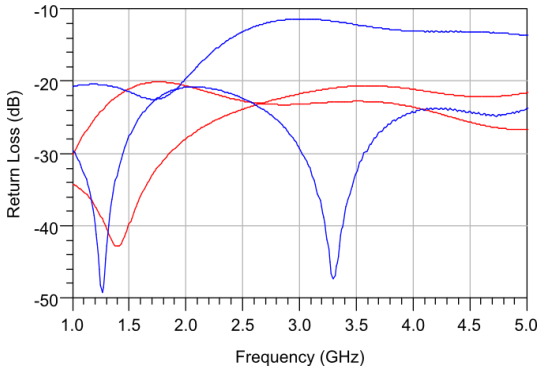


Differential Phase

Differential Phase Related Calculations

	RMS Phase (°)	RMS PE (°)	Max. PE (°)	Max IL (dB)	Min RL (dB)
Ideal	44.50	1.16	2.22	-	-
Practical	45.02	1.22	1.81	1.98	22.63
Measurement	46.96	3.23	6.31	5.28	17.49

2 to 4 GHz Phase Shifter 22.5° M



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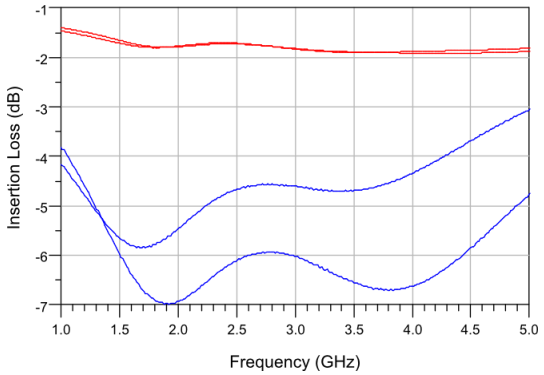

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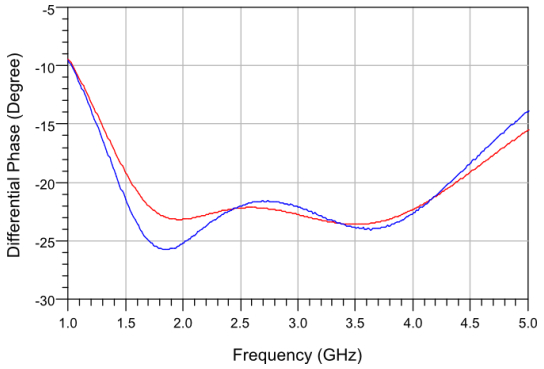
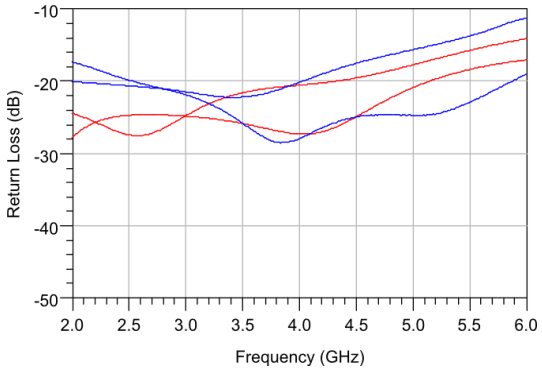


Differential Phase

Differential Phase Related Calculations

	RMS Phase (°)	RMS PE (°)	Max. PE (°)	Max IL (dB)	Min RL (dB)
Ideal	22.69	0.53	1.04	-	-
Practical	22.87	0.48	0.73	1.91	20.63
Measurement	23.01	0.943	2.25	6.93	11.38

3 to 6 GHz Phase Shifter 180° M



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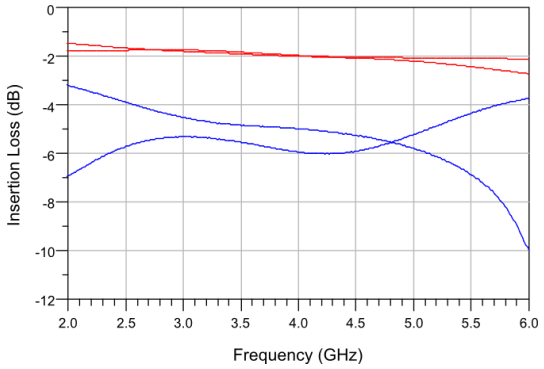

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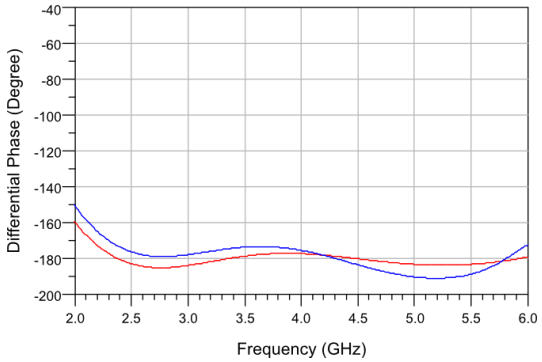
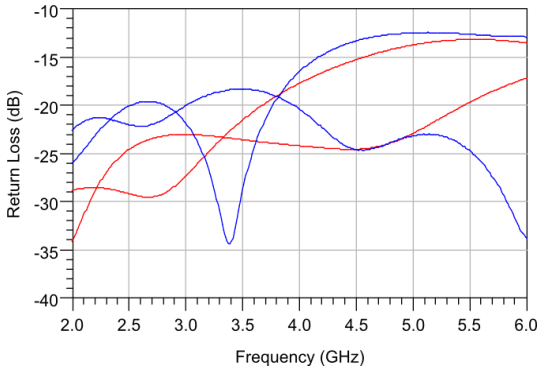


Differential Phase

Differential Phase Related Calculations

	RMS Phase (°)	RMS PE (°)	Max. PE (°)	Max IL (dB)	Min RL (dB)
Ideal	179.43	2.16	3.45	-	-
Practical	180.96	2.28	3.61	2.72	14.10
Measurement	181.70	6.46	9.72	10.00	11.31

3 to 6 GHz Phase Shifter 90° M



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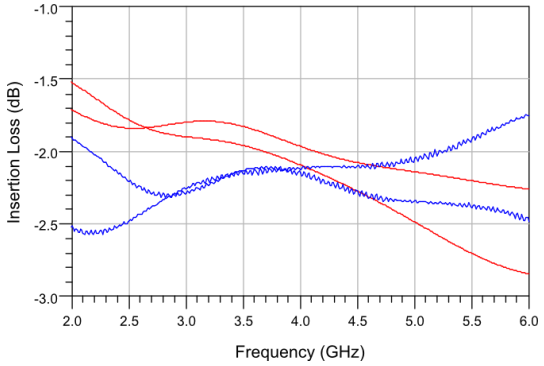

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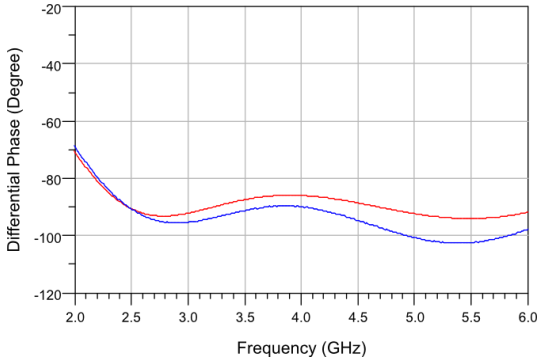
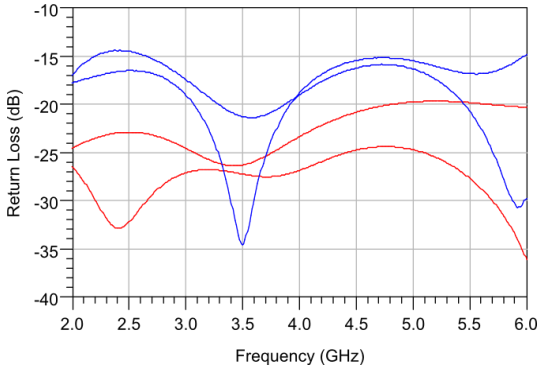


Differential Phase

Differential Phase Related Calculations

	RMS Phase (°)	RMS PE (°)	Max. PE (°)	Max IL (dB)	Min RL (dB)
Ideal	90.01	1.95	3.54	-	-
Practical	90.11	2.89	4.17	2.85	13.15
Measurement	96.11	4.63	6.66	2.49	12.44

3 to 6 GHz Phase Shifter 90° DCM



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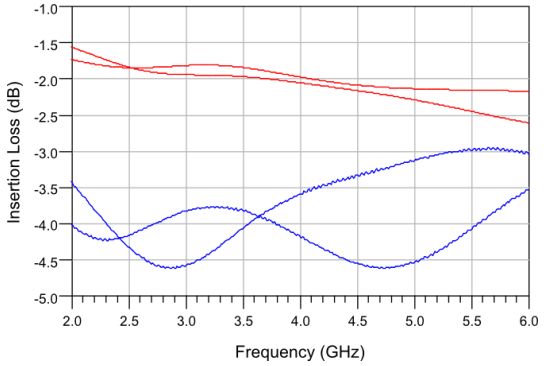

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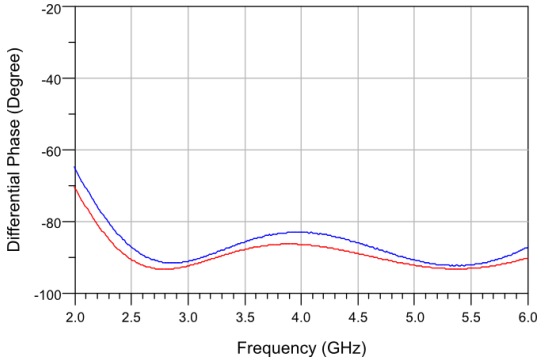
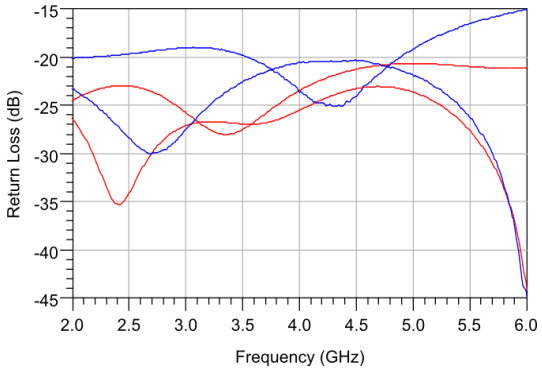


Differential Phase

Differential Phase Related Calculations

	RMS Phase (°)	RMS PE (°)	Max. PE (°)	Max IL (dB)	Min RL (dB)
Ideal	90.01	1.95	3.54	-	-
Practical	90.07	2.39	3.64	2.61	19.68
Measurement	87.96	3.19	4.90	4.61	14.85

3 to 6 GHz Phase Shifter 90° DCF



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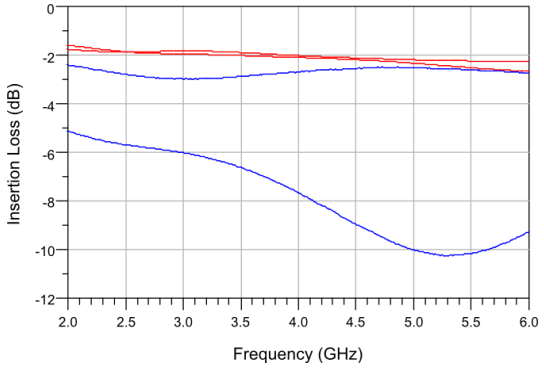

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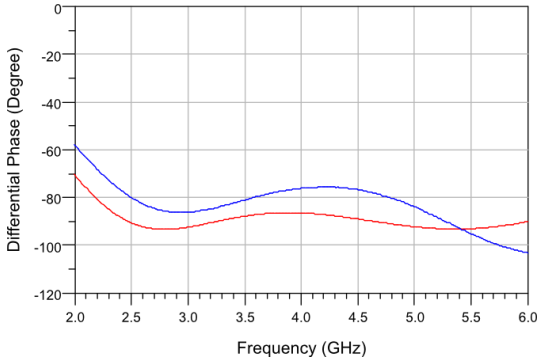
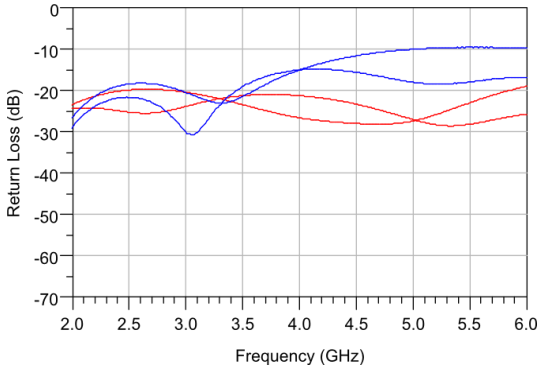


Differential Phase

Differential Phase Related Calculations

	RMS Phase (°)	RMS PE (°)	Max. PE (°)	Max IL (dB)	Min RL (dB)
Ideal	90.01	1.95	3.54	-	-
Practical	90.06	2.38	3.63	2.67	20.68
Measurement	84.99	8.38	18.64	10.25	15.06

3 to 6 GHz Phase Shifter 45° M



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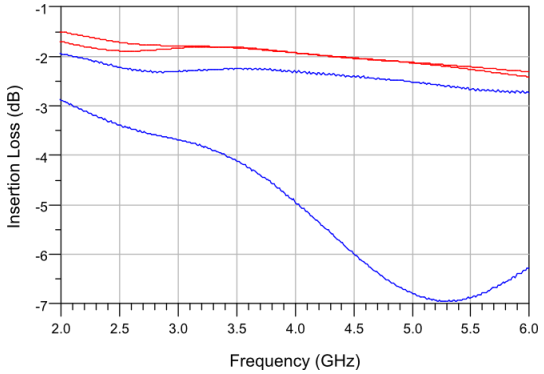

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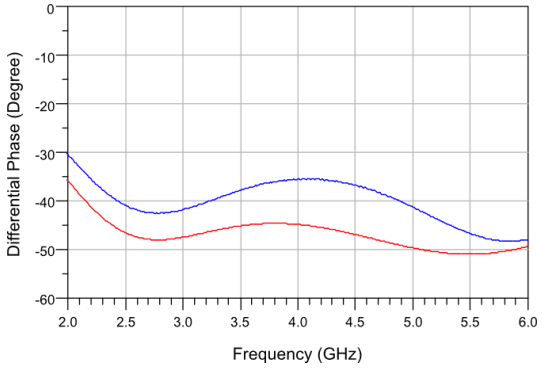
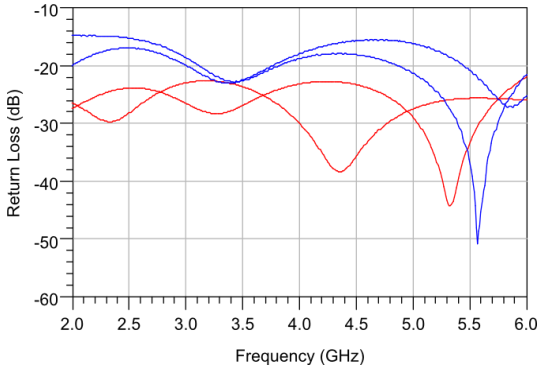


Differential Phase

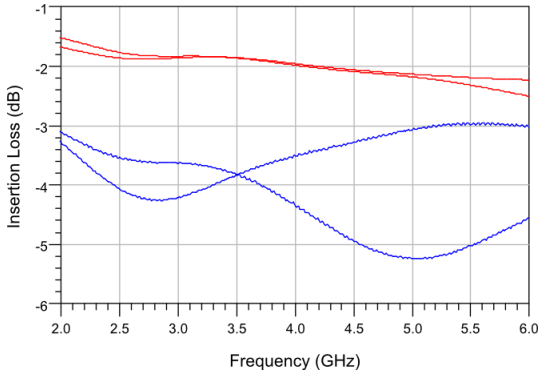
Differential Phase Related Calculations

	RMS Phase (°)	RMS PE (°)	Max. PE (°)	Max IL (dB)	Min RL (dB)
Ideal	46.21	1.00	1.81	-	-
Practical	47.75	2.32	3.30	2.41	18.94
Measurement	40.75	4.41	7.85	6.96	9.54

3 to 6 GHz Phase Shifter 45° DCM



Return Loss



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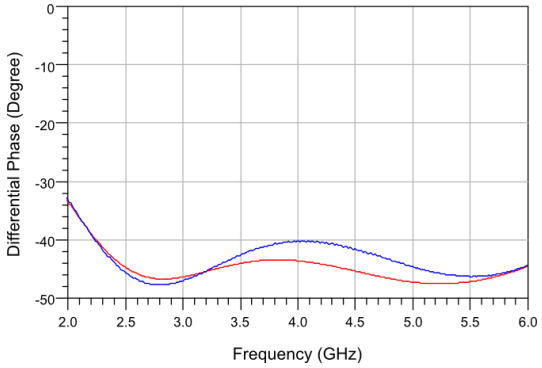
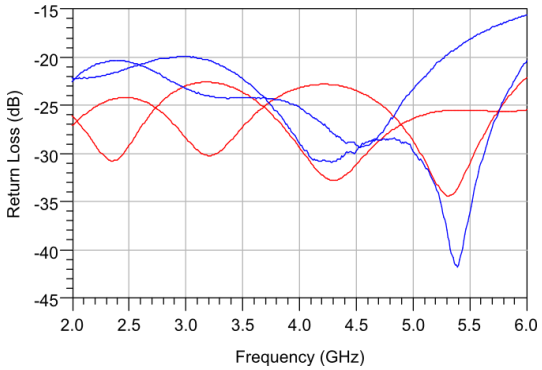


Differential Phase

Differential Phase Related Calculations

	RMS Phase (°)	RMS PE (°)	Max. PE (°)	Max IL (dB)	Min RL (dB)
Ideal	46.21	1.00	1.81	-	-
Practical	45.56	1.39	2.08	2.50	21.94
Measurement	43.61	2.20	3.52	5.25	15.43

3 to 6 GHz Phase Shifter 45° DCF



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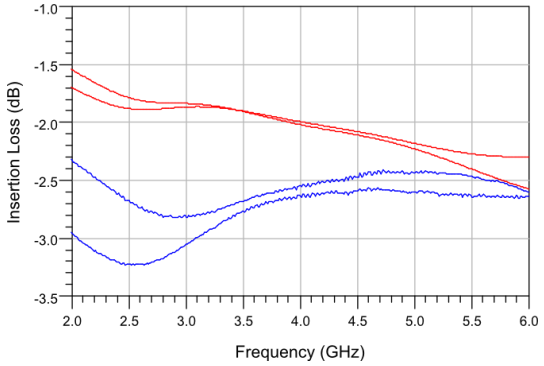

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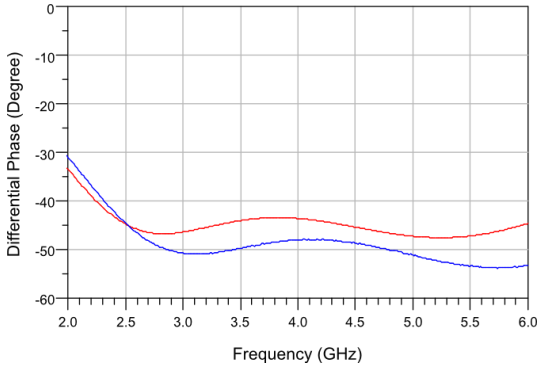
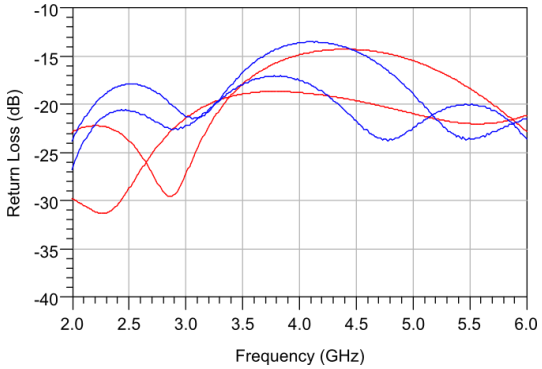


Differential Phase

Differential Phase Related Calculations

	RMS Phase (°)	RMS PE (°)	Max. PE (°)	Max IL (dB)	Min RL (dB)
Ideal	46.21	1.00	1.81	-	-
Practical	45.58	1.39	2.09	2.57	22.08
Measurement	50.62	2.00	3.28	3.05	15.65

3 to 6 GHz Phase Shifter 22.5° M



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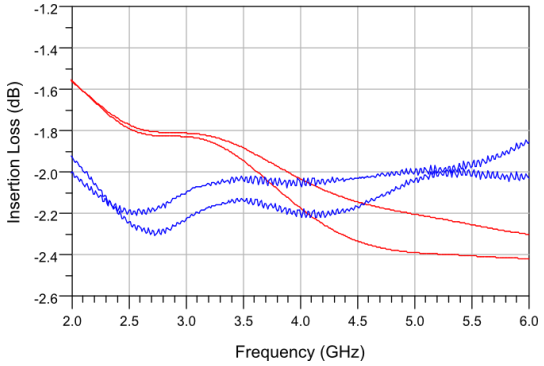

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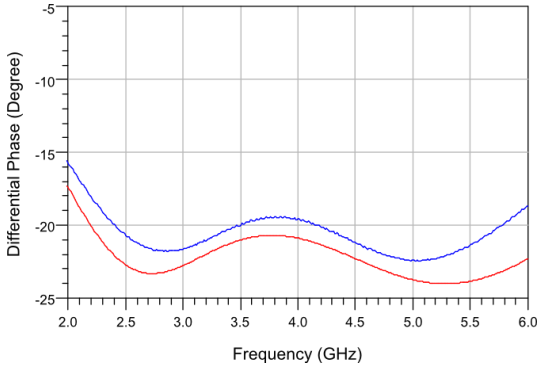
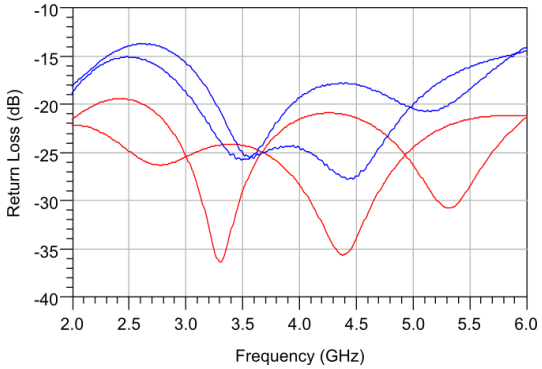


Differential Phase

Differential Phase Related Calculations

	RMS Phase (°)	RMS PE (°)	Max. PE (°)	Max IL (dB)	Min RL (dB)
Ideal	23.17	0.59	1.23	-	-
Practical	22.44	1.16	1.70	2.42	14.28
Measurement	20.84	1.05	2.14	2.23	13.51

3 to 6 GHz Phase Shifter 22.5° DCM



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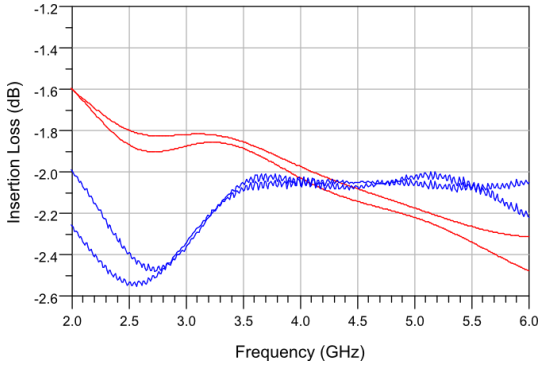

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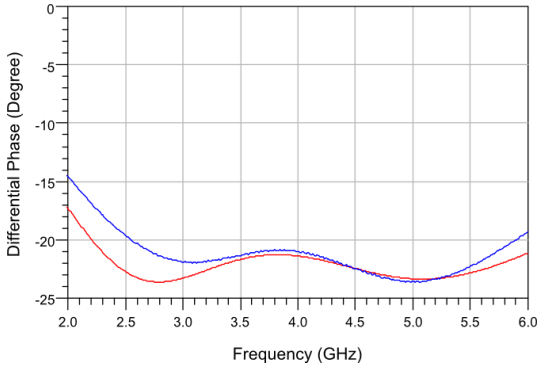
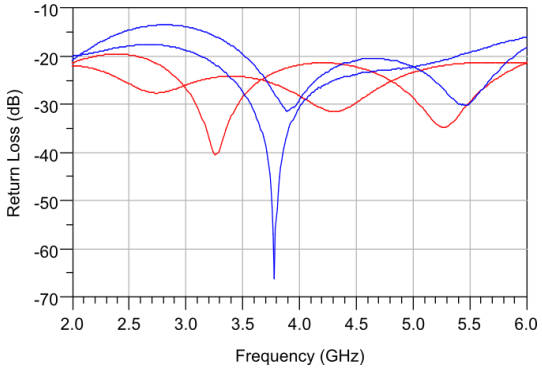


Differential Phase

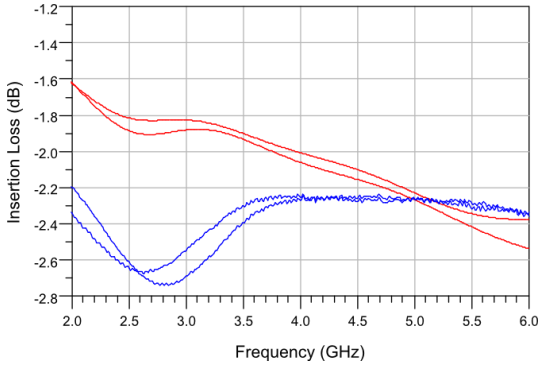
Differential Phase Related Calculations

	RMS Phase (°)	RMS PE (°)	Max. PE (°)	Max IL (dB)	Min RL (dB)
Ideal	23.17	0.59	1.23	-	-
Practical	22.36	0.72	1.18	2.48	20.90
Measurement	21.97	1.04	2.59	2.36	14.03

3 to 6 GHz Phase Shifter 22.5° DCF



Return Loss



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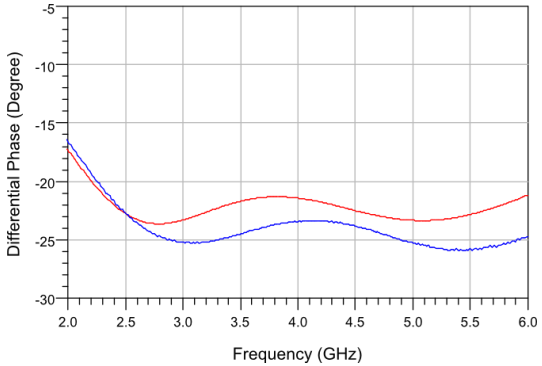

Differential Phase

Differential Phase Related Calculations

	RMS Phase (°)	RMS PE (°)	Max. PE (°)	Max IL (dB)	Min RL (dB)
Ideal	23.17	0.59	1.23	-	-
Practical	22.37	0.71	1.18	2.54	21.27
Measurement	24.70	0.84	1.33	4.96	13.92

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