UNCOOLED INFRARED FOCAL PLANE ARRAYS WITH INTEGRATED READOUT CIRCUITRY USING MEMS AND STANDARD CMOS TECHNOLOGIES

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Approval of Graduate School of Natural and Applied Sciences

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ABSTRACT

UNCOOLED INFRARED FOCAL PLANE ARRAYS WITH INTEGRATED READOUT CIRCUITRY USING MEMS AND STANDARD CMOS TECHNOLOGIES

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This thesis reports the development of low-cost uncooled microbolometer focal plane arrays (FPAs) together with their integrated readout circuitry for infrared night vision applications. Infrared microbolometer detectors are based on suspended and thermally isolated p^+-active/n-well diodes fabricated using a standard 0.35 μm CMOS process followed by a simple post-CMOS bulk-micromachining process. The post-CMOS process does not require any critical lithography or complicated deposition steps; and therefore, the FPA cost is reduced considerably. The integrated readout circuitry is developed specially for the p^+-active/n-well diode

microbolometers that provides lower input referred noise voltage than the previously developed microbolometer readout circuits suitable for the diode type microbolometers. Two FPAs with 64 × 64 and 128 × 128 array formats have been implemented together with their low-noise integrated readout circuitry. These FPAs are first of their kinds where such large format uncooled infrared FPAs are designed and fabricated using a standard CMOS process.

The fabricated detectors have a temperature coefficient of -2 mV/K, a thermal conductance value of 1.55×10^{-7} W/K, and a thermal time constant value of 36 ms, providing a measured DC responsivity ($\Re$) of 4970 V/W under continuous bias. The measured detector noise is 0.69 μV in 8 kHz bandwidth, resulting a measured detectivity (D^*) of 9.7×10^8 cm√Hz/W. The 64 × 64 FPA chip has 4096 pixels scanned by an integrated 16-channel parallel readout circuit composed of low-noise differential transconductance amplifiers, switched capacitor integrators, and sample-and-hold circuits. It measures 4.1 mm × 5.4 mm, dissipates 25 mW power, and provides an estimated NETD value of 0.8 K at 30 frames/sec (fps) for an f/1 optics. The measured uncorrected voltage non-uniformity for the 64 × 64 array after the CMOS fabrication is 0.8 %, which is reduced further down to 0.2 % for the 128 × 128 array using an improved FPA structure that can compensate for the fixed pattern noise due to the FPA routing. The 128 × 128 FPA chip has 16384 microbolometer pixels scanned by a 32-channel parallel readout circuitry. The 128 × 128 FPA measures 6.6 mm × 7.9 mm, includes a PTAT temperature sensor and a vacuum sensor, dissipates 25 mW power, and provides an estimated NETD value of 1 K at 30 fps for an f/1 optics. These NETD values can be decreased below 350 mK with further optimization of the readout circuit and post-CMOS etching steps. Hence, the proposed method is very cost-effective to fabricate large format focal plane arrays for very low-cost infrared imaging applications.

Keywords: Uncooled infrared detectors, microbolometers, low-cost microbolometer detectors, uncooled infrared focal plane arrays, readout circuits for microbolometers.

ÖZ

MEMS VE STANDART CMOS TEKNOLOJİLERİ İLE ENTEGRE OKUMA DEVRELİ SOĞUTMASIZ KIZILÖTESİ ODAK DÜZLEM MATRİSLERİ

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Temmuz 2003, 276 sayfa

Bu tezde kızıl ötesi gece görüş uygulamaları için MEMS ve standart CMOS teknolojileri kullanılarak düşük maliyetli, okuma devreleri ile entegre edilmiş soğutmasız kızıl ötesi dedektör odak düzlem matrisleri (ODMler) anlatılmaktadır. Geliştirilen kızıl ötesi mikrobolometre dedektörleri, 0.35 μm CMOS üretim süreci ve sonrasında basit bir gövde aşındırma işlemi kullanılarak üretilen, gövdeden ısıl olarak izole edilmiş p^+-aktif/n-kuyu diyot yapılarına dayanmaktadır. CMOS üretim sonrasında yapılan işlemler ne kritik bir pozlama ne de karmaşık bir malzeme serim işlemi içermektedir; bu nedenle, odak düzlem matrisinin maliyeti oldukça düşürülmüştür. Entegre okuma devresi özel olarak p^+-aktif/n-kuyu diyot tipi mikrobolometreler için geliştirilmiş olup, daha önceden geliştirilen diyot tipi

mikrobolometrelere uygun okuma devrelerinden daha düşük giriş gürültüsüne sahiptir. Düşük gürültülü entegre okuma devreleri içeren 64 × 64 ve 128 × 128 dizin formatlı iki adet odak düzlem matrisi üretilmiştir. Üretilen bu odak düzlem matrisleri bu boyutlarda CMOS teknolojisinde üretilmiş olan ilk odak düzlem matrisleri olma özelliğine sahiptirler.

Üretilen dedektörlerin sıcaklık sabitleri -2 mV/K, ısıl iletileri 1.55×10^{-7} W/K, ısıl zaman sabitleri 36 ms'dir ve ölçülmüş kızılötesi DC cevaplılıkları sürekli kutuplama altında 4970 V/W'dır. Ölçülen dedektör gürültüsü 8 kHz elektriksel band aralığında 0.69 μV'dur ve 9.7×10^8 cm√Hz/W'lık bir dedektivite değerine karşılık gelmektedir. 64 × 64 odak düzlem matrisindeki 4096 adet piksel, düşük gürültülü fark-geçiş-ileti yükselticisi, anahtarlamalı kapasitör entegratörü ve örnekle-ve-tut devreleri içeren 16 kanallı paralel bir okuma devresi tarafından taranmaktadır. Üretilen 64 × 64 odak düzlem matrisinin boyutu 4.1 mm × 5.4 mm, güç tüketimi 25 mW olup, 30 fps tarama hızında f/1 optik ile 0.8 K'lik bir gürültüye eş sıcaklık farkı (GESF) sağlaması beklenmektedir. CMOS üretim sonunda 64 × 64 odak düzlem matrisinin ölçülmüş eşdeğersizlik değeri % 0.8'dir ve bu değer 128 × 128 odak düzlem matrisinde geliştirilmiş odak düzlem yapısı sayesinde % 0.2'ye kadar indirilmiştir. 128 × 128 odak düzlem matrisindeki 16384 adet piksel 32 kanallı bir okuma devresi tarafından okunmaktadır. 128 × 128 odak düzlem matrisinin boyutu 6.6 mm × 7.9 mm, güç tüketimi 25 mW olup, 30 fps hızında f/1 optik ile 1 K GESF değeri sağlaması beklenmektedir. Okuma devrelerinin ve CMOS sonrası aşındırma işlemlerinin optimizasyonu ile verilen GESF değerlerinin 350 mK'in altına indirilmesi mümkündür. Yukarıda belirtilen nedenlerden dolayı öne sürülen bu yeni yöntem, düşük maliyetli kızıl ötesi görüntüleme uygulamaları için büyük dizin yapılarının düşük maliyet ile üretimini mümkün kılmaktadır.

Anahtar Kelimeler: Soğutmasız kızıl ötesi dedektörler, mikrobolometreler, düşük maliyetli mikrobolometre dedektörleri, soğutmasız kızılötesi odak düzlem matrisleri, mikrobolometreler için okuma devreleri.

To My Parents

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CHAPTER I

1 INTRODUCTION

Infrared radiation is part of the electromagnetic spectrum with wavelengths above visible spectrum ranging from 1 μm to several tens of μm. Detectors that can sense the infrared radiation are called infrared detectors, and ensembles of the infrared detectors in (one or) two dimensional arrays are called focal plane arrays (FPAs). Infrared detectors are used in many military and commercial applications such as night vision, mine detection, reconnaissance, fire fighting, medical imaging, and industrial control.

There are basically two types of infrared detectors used in the FPAs for infrared imaging applications: photon and thermal detectors. In photon detectors, the absorbed infrared photons generate free electron-and-hole (E-H) pairs, which are collected by an applied electric field for electronic processing. For proper operation, the photon detectors need to be cooled down to cryogenic temperatures, such as 77 K or lower, hence they are also called cooled infrared detectors. There are very high performance photon detector FPAs in the market, however their costs are very high for many commercial and even for some military applications. In order to achieve lower cost infrared FPAs, a different technology has been developed known as the thermal infrared detector technology. In thermal detectors, the energy of the absorbed infrared photon rises the temperature of the detector, and the change in one of the electrical parameter due to the temperature change is measured with the help

of proper electronic circuitry. Thermal detectors can operate at room temperature without the need for cryogenic coolers; therefore they are also called uncooled infrared detectors. Despite their lower detectivity values, these detectors have recently gained wide attention due to their advantages such as low cost, small size, and low power.

For some applications, the cost of the current state-of-the art uncooled infrared detector arrays are still very high due to the required complicated deposition and patterning steps of the sensitive detector materials. There is still need for a very low-cost approach to implement uncooled FPAs. This thesis reports the development of such low-cost uncooled infrared detectors and arrays together with their integrated readout circuitry using MEMS and standard CMOS technologies.

The rest of the chapter is organized as follows: Section 1.1 gives the theory of infrared radiation. Section 1.2 explains the types of infrared detectors, Section 1.3 explains the principles of thermal detectors and their history of development, and Section 1.4 describes the types of thermal detectors, including resistive microbolometers, pyroelectric and ferroelectric detectors, thermoelectric detectors, and diode microbolometers. Finally, Section 1.5 gives the research objectives and organization of the thesis.

1.1 Infrared Spectrum

Infrared radiation is part of the electromagnetic spectrum with wavelengths above visible spectrum ranging approximately from 1 μm to 1000 μm [1], which is called the infrared spectrum discovered first in 1800 by William Hershel. Figure 1.1 shows the complete electromagnetic spectrum of light with important spectral regions. Infrared spectrum is divided into sub-regions called short-wave infrared (SWIR: 1 μm - 3 μm), mid-wave infrared (MWIR: 3 μm - 6 μm), long-wave infrared (LWIR: 6 μm – 16 μm), and far infrared (FIR: > 16 μm) [1].

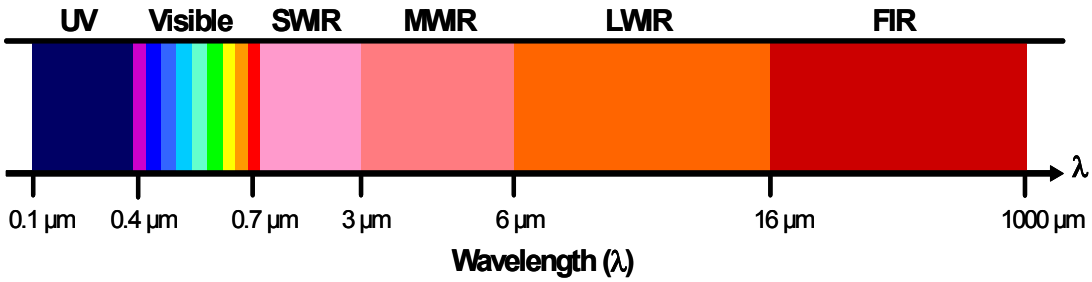


Figure 1.1: Complete electromagnetic spectrum of light with important spectral regions [1].

Infrared detectors are sensitive to a specific wavelength range in the electromagnetic spectrum. Selection of the detector type, and hence the wavelength range, is determined by the atmospheric transmission characteristics and the temperature range of the targets. Figure 1.2 shows the atmospheric transmittance over 2 km at sea level [2]. It can be seen that there are spectral windows where the infrared radiation is absorbed heavily, making infrared imaging impossible. The commonly used spectral windows are 3 µm - 5 µm band in MWIR and 8 µm - 12 µm band in LWIR, where the loss due to the atmospheric absorption is at negligible levels. The infrared detectors are designed such that their spectral responsivity covers at least one of these bands.

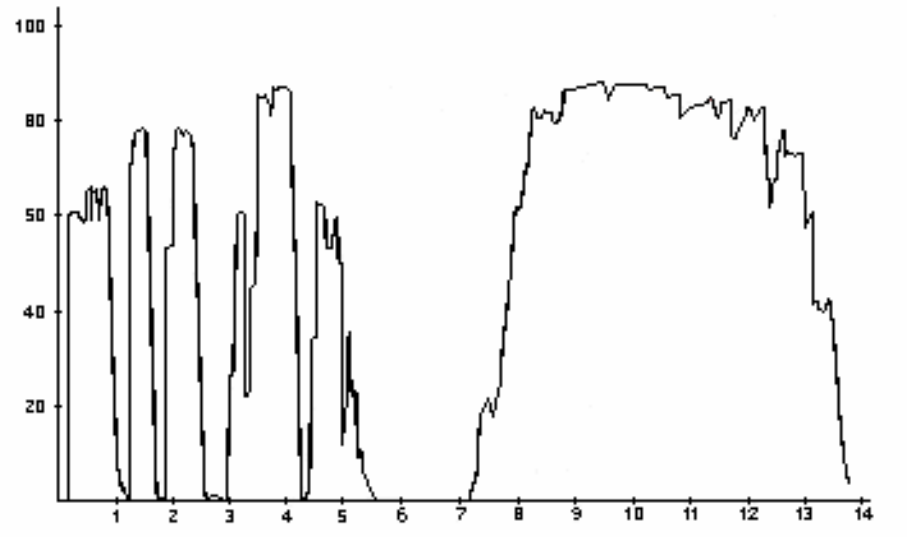


Figure 1.2: Atmospheric transmittance over 2 km at sea level [2].

Selection of the spectral window for imaging application also depends on the temperature range of the target, since the spectral content of the infrared radiation emitted from the objects changes with temperature, and it is given in terms of spectral radiant exitance. For a blackbody object, the spectral radiant exitance ($M_e(\lambda, T)$) is given as [3]

$$M_e(\lambda,T) = \frac{2\pi hc^2}{\lambda^5\left(e^{hc/\lambda kT}-1\right)} \tag{1.1}$$

where, h is the Plank's constant, c is the speed of light, λ is the wavelength of infrared radiation, k is the Boltzmann constant, and T is temperature of the blackbody in Kelvin. Figure 1.3 shows the variation of the blackbody spectral exitance with wavelength for different blackbody temperatures from 100 K to 1000 K [4]. As the temperature of the blackbody increases, the wavelength of maximum exitance (λ_{max}) shifts to smaller wavelengths, which is known as Wien Displacement Law. The wavelength at which the spectral exitance becomes maximum at a given temperature is given as [3]

$$\lambda_{\max} = \frac{2898\mu mK}{T} \tag{1.2}$$

where, T is the temperature in Kelvin.

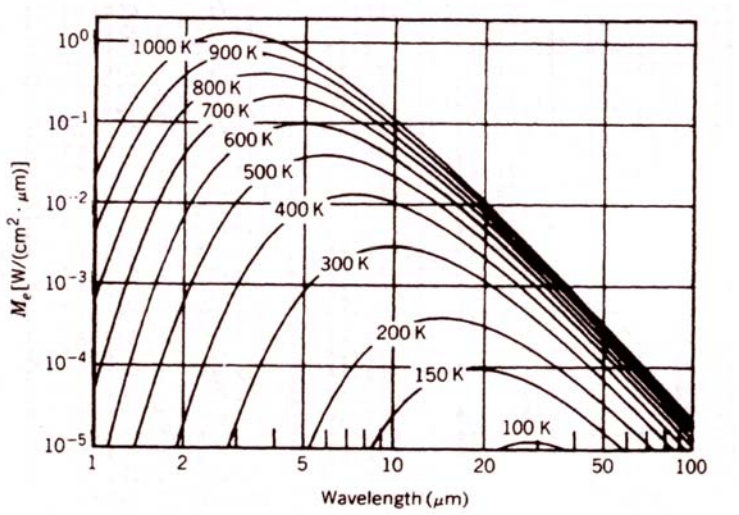


Figure 1.3: Variation of the blackbody spectral exitance with wavelength for different blackbody temperatures from 100 K to 1000 K [4].

For a blackbody at 300 K, maximum exitance occurs at 9.7 μm, close to the midpoint of the atmospheric transmission window of 8 μm – 12 μm (LWIR). Therefore, LWIR detectors are used in the infrared imaging applications for objects at around 300 K, such as night vision applications. MWIR detectors are preferred when the target temperature increases, as in the case of tracking of hot objects such as air planes or missiles. The imaging in 3 μm – 5 μm and 8 μm – 12 μm spectral windows can be performed with different types of infrared detectors, as explained in the next section.

1.2 Types of Infrared Detectors

There are basically two types of detectors that can sense the infrared radiation. The first type is the photon detectors, where the absorbed infrared photons generate free electron-and-hole (E-H) pairs, which are then collected by the application of electric field for electronic processing. The second type of infrared detectors are known as thermal detectors, where the energy of the absorbed infrared photon rises the temperature of the detector, and the temperature induced change in one of the electrical parameters is measured with the help of a proper electronic circuit.

Photon infrared detectors are fast, and their sensitivities are much higher as compared to thermal detectors. However, the number of thermally generated E-H pairs are much higher than the infrared induced E-H pairs at room temperature, which makes their use for infrared imaging impossible especially in the LWIR range unless they are cooled down to cryogenic temperatures such as 77 K or below. For this purpose, special and expensive coolers are used, increasing the size, cost, and operating power of the detector systems or cameras. Commonly used cooled detectors are fabricated using Indium Antimonide (InSb) [5], Mercury Cadmium Telluride (HgCdTe or MCT) [6, 7], or Quantum Well Infrared Photodetector (QWIP) [8-10] technologies. The fabrication of these detectors involve complicated processing steps due the known difficulties of handling low-bandgap materials required for the detection of low energy infrared photons. Therefore, the cost of the

photonic detectors and infrared cameras using photonic detectors are very high, finding application areas only in expensive weapon platforms, in astronomical observation instruments, or special medical instruments, where the performance is the primary issue. On the other hand, the infrared cameras using thermal detectors are small in size, consume less power, and are low-cost, making them ideal choice for applications which require high unit numbers with relatively lower performance. The next section explains the principles of thermal detectors and their history of development.

1.3 Thermal (Uncooled) Infrared Detectors

Thermal or uncooled infrared detectors sense the change in an electrical parameter upon the change in the device temperature related with the amount of absorbed infrared energy. Therefore, thermal detection mechanism is an indirect way of infrared detection, and the response time of these detectors are longer as compared to the photon detectors. In most of the cases, signal-to-noise ratio and detectivity of the uncooled thermal detectors are lower than that of the cooled photon detectors. Therefore, the performance of the thermal detectors is lower then the cooled photon detectors. Since the electrical bandwidth of the staring arrays is much lower than the scanned arrays, it is possible to improve the signal-to-noise ratio of the thermal detectors when operated in staring arrays. Furthermore, it is relatively easier to fabricate staring array using thermal detectors as compared to the arrays that use cooled photon detectors. Furthermore, at scanning speeds close to the TV frame rate (30 frames/sec), the performance degradation of the thermal detectors due to their relatively longer thermal time constants can be minimized by proper detector design. Considering these factors, although the cooled detector arrays still provide better performances, the performance difference between the thermal and cooled photonic detectors becomes smaller than what is expected by just comparing them on pixel basis [11].

The most important advantage of the thermal detectors is that they can operate at room temperature without requiring any complex and expensive cooling

equipment. The resulting infrared imaging systems utilizing the uncooled detector technology have much smaller size, lower cost, lower power consumption, and extended operation durations. Due to these advantages uncooled detectors are used in many military and commercial applications, such as night vision, mine detection, driver night vision enhancement, fire fighting, and industrial control applications. Figure 1.4 shows the technological development of uncooled infrared FPAs [12], and Figure 1.5 shows the system application roadmap of the uncooled infrared FPAs [12]. As can be seen, the uncooled technology has already demonstrated detectors with 50 μm × 50 μm size and with a noise equivalent temperature difference (NETD) better than 100 mK. Currently, there are uncooled FPAs with 640 × 480 array format with 28 μm × 28 μm pixel sizes and NETD values lower than 50 mK [13]. The target of the uncooled technology is to fabricate detectors with less than 25 μm × 25 μm pixel size and with NETD values better than 10 mK. Therefore, as the uncooled technology develops, many other infrared imaging systems that currently use cooled infrared detector arrays may start using uncooled detector arrays. Considering the developments in the cooled technology, the cooled photonic detectors may find application areas in more sophisticated and expensive infrared imaging platforms requiring relatively higher performance possibly with new features such as multi-spectral infrared radiation sensing capability possible to achieve using the rapidly developing QWIP technology.

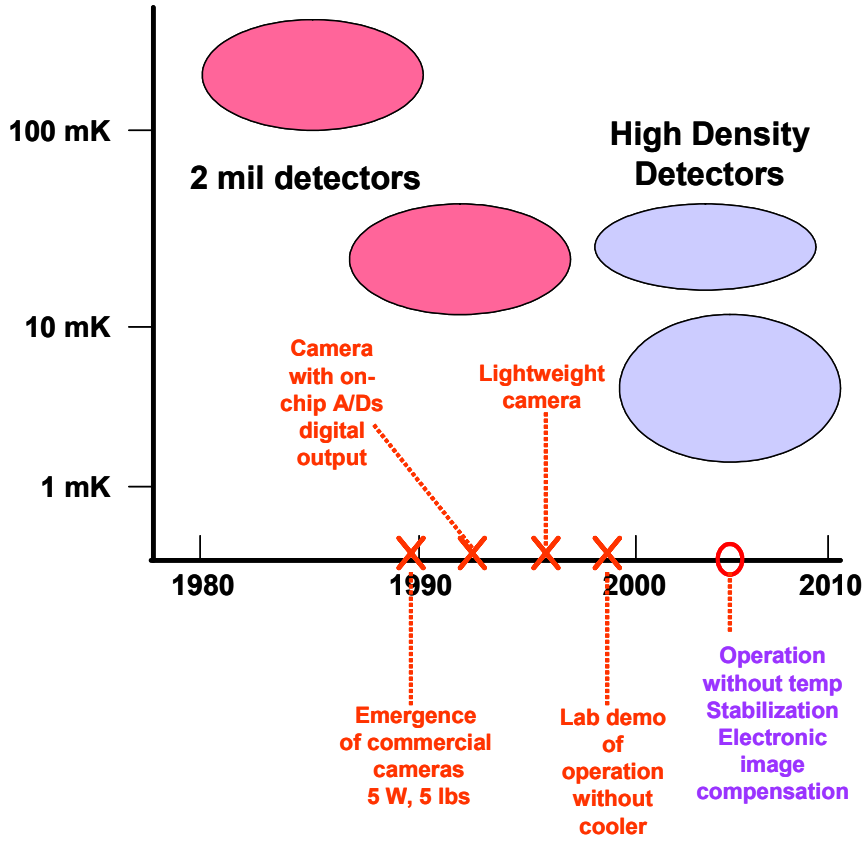


Figure 1.4: Technological development of uncooled infrared FPAs [12].

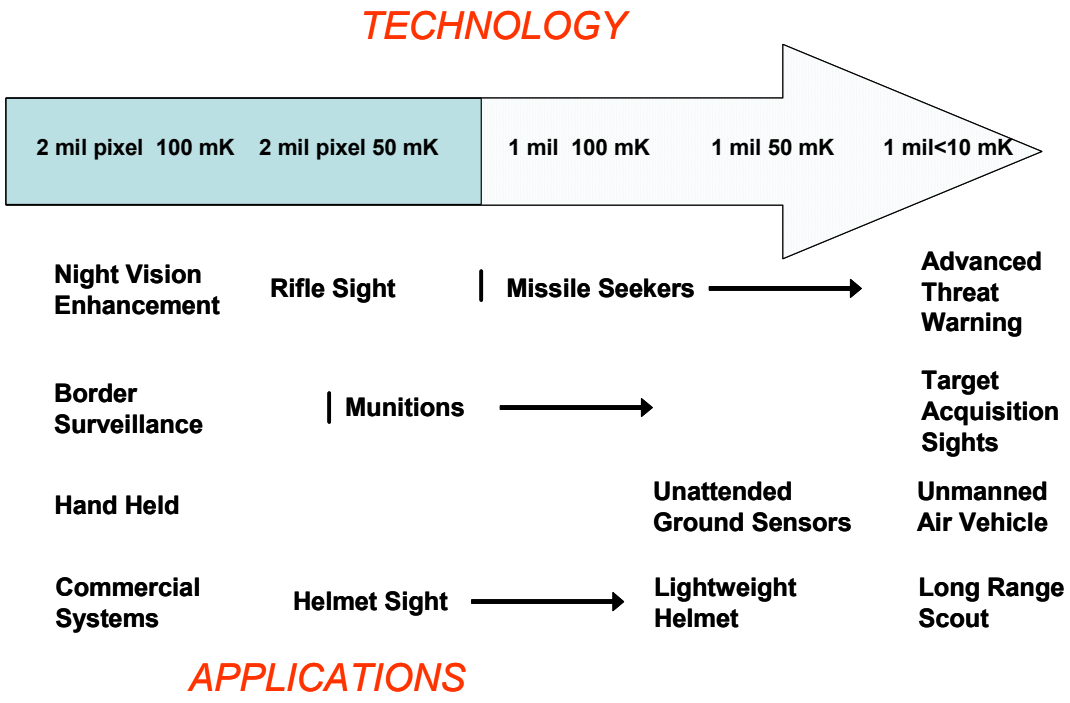


Figure 1.5: System application roadmap for the uncooled infrared FPAs [12].

1.3.1 History of Thermal Detectors

The first practical demonstration of thermal infrared detection dates back to 1880, when Langley constructed the first thermal detector, more specifically the first bolometer, whose resistance changes upon absorbed infrared radiation. In 1901, he successfully demonstrated that he could detect a cow at a distance about a quarter mile away from his detector, by just monitoring the deflections in a meter [14].

At the beginning of the 1980, after 100 years since the first demonstration, the idea of bolometric thermal infrared imaging attracted interest of researchers, and a group of researchers under the direction of R. Andrew Wood started working on thermal imaging at the Honeywell Technology Center, targeting the development of resistive bolometer arrays for uncooled infrared imaging applications. This project was supported by several funding agencies such as the U.S. Department of Defense, Defense Advanced Research Projects Agency (DARPA), and U.S. Army Night Vision and Electronic Sensor Directorate (NVESD). As result of this project, Honeywell successfully developed uncooled microbolometer arrays with 336 × 240 format with 50 μm × 50 μm pixels with an NETD value better than 100 mK at a scanning speed of U.S. TV frame rate of 30 frames-per-second (fps) [11]. Currently, there are 640 × 480 uncooled microbolometer FPAs utilizing 25 μm × 25 μm pixels with an NETD value better than 50 mK [13].

An alternative thermal infrared detection mechanism, which is based on the pyroelectric effect, is proposed by Chynoweth in 1956 [14]. The first thermal imaging camera based on pyroelectric effect was built by Tompsett using a pyroelectric photo tube [15]. Uncooled arrays based on pyroelectric detectors are implemented by several research groups in different companies such as Texas Instruments in the U.S., Royal Signals and Radar Establishment, and GEC Marcony in the U.K. [14, 16, 17]. The above listed companies used hybrid technologies, making it difficult to improve the sensitivity due to the thermal isolation problems [14]. After a long development time, only Texas Instruments and GEC Marconi have managed to fabricate hybrid pyroelectric detector arrays. At the time of writing

this thesis, there are 320×240 uncooled pyroelectric detector arrays using 48.5 μm × 48.5 μm pixels with 100 % fill factor bump bonded to the readout circuit, resulting an NETD value of 60 mK [18]. There are also efforts to fabricate these detectors monolithically [19]; however, fabrication of a monolithic array has not been demonstrated yet.

The research on uncooled infrared detector arrays was conducted under classified projects until 1992 [11]. Since that time, the information on the uncooled technology has been made available to the public, resulting more companies to enter into this new infrared imaging area such as Raytheon [20], DRS (formerly Boeing) [21], BAE (formerly Honeywell) [13], Sarcon [22], and Indigo [23] in the U.S., INO in Canada [24], ULIS in France [25, 26], NEC [27] and Mitsubishi [28, 29] in Japan. There are also many research institutions working on the uncooled infrared detectors and arrays, such as LETI LIR in France [25, 26], IMEC in Belgium [30], ETH [1, 2, 31-33] in Switzerland, The University of Texas Arlington [34] and the University of Michigan [35-37] in the U.S., KAIST in Korea [38], and METU in Turkey [39-45]. Some of them have fabricated thermal detector arrays and cameras based on different thermal detectors both for commercial and military applications. The next section describes the types of thermal infrared detectors.

1.4 Types of Thermal Infrared Detectors

There are basically four types of thermal infrared detectors: 1) resistive microbolometers, 2) pyroelectric and ferroelectric detectors, 3) thermoelectric detectors, and 4) diode microbolometers. Although, there are some other thermal infrared detection mechanisms, such as heat-balancing [36, 37] and microcantilever thermal detectors [22], only the above four detector types have been widely used in the practical uncooled thermal imaging applications, and they will be explained in the next sections.

1.4.1 Resistive Microbolometers

One of the most famous approaches for uncooled infrared imaging is to use resistive microbolometers implemented using surface micromachined bridges on CMOS processed wafers [13, 20-26, 30]. Figure 1.6 shows the simplified perspective view of a microbolometer structure obtained using surface micromachining techniques [11]. Infrared radiation increases the temperature of a material on the thermally isolated and suspended bridge, causing a change in its resistance related with its TCR value. The performance of the resistive microbolometers depends both on the temperature sensitive layer along with its thermal isolation and the quality of the readout circuit.

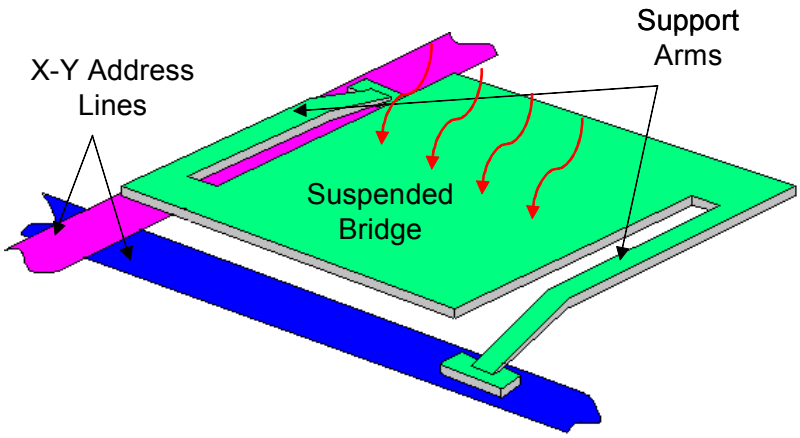
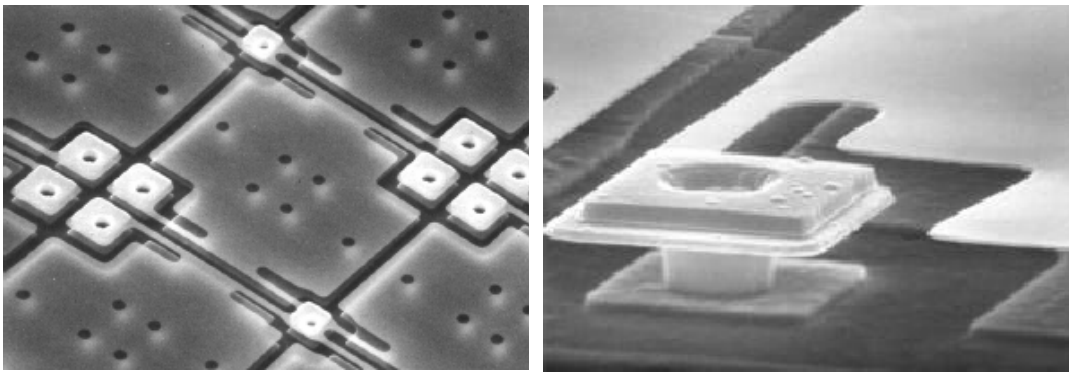


Figure 1.6: Simplified perspective view of a microbolometer structure obtained using surface micromachining techniques [11].

Surface micromachining technique allows deposition of temperature sensitive layers with very small thickness, very small mass, and very good thermal isolation on top of bridges over the readout circuit chips. With the removal of the sacrificial layers between the bridge structures and readout circuit chip, suspended and thermally isolated detector structures are obtained. Figure 1.7 (a) shows the SEM photographs of a surface micromachined microbolometer detector array from top, and Figure 1.7 (b) shows the zoomed view of the pixel support arm structure [25].



(a) (b)

Figure 1.7: SEM photographs of the a-Si surface micromachined microbolometer detectors: (a) top view and (b) zoomed view of the pixel support arm structure [25].

There are efforts to implement microbolometers using many different materials, such as vanadium oxide (VO_x) [13, 20-21, 23, 46], amorphous silicon (a-Si) [25, 26], polycrystalline silicon–germanium (poly SiGe) [30], Yttrium Barium Copper Oxide (YBaCuO) [29, 34], and metal films [47, 48]. The main drawback of VO_x is that it is not compatible with a CMOS line, and requires a separate fabrication line after CMOS process to prevent the contamination of the CMOS line. In addition, VO_x exhibits large 1/*f* noise due to its non-crystalline structure, limiting its performance. Although a-Si and poly SiGe are CMOS compatible, they require high temperature annealing to achieve stability of microstructures, making the monolithic CMOS integration difficult. In addition, both a-Si and poly SiGe have high 1/*f* noise due to their non-crystalline structures, as VO_x. Deposition of YBaCuO is performed at room temperature, however, fabrication of these detectors still require complicated post-CMOS surface micromachining processes as the above materials. On the other hand, metals are both CMOS compatible, and their fabrication does not require any high temperature process steps. However, metal microbolometers have low performance due to low TCR value of metal films. In summary, in all of the surface micromachined microbolometers, there is a need for critical deposition and post-CMOS lithography steps, limiting their cost reduction.

In uncooled microbolometers, special care should be given to the readout electronics, as it can determine the final overall performance of the detector. The change in the detector resistance, hence the incident infrared radiation, can be

measured using a simple bridge circuit. Figure 1.8 shows the schematic of a half-bridge circuit used to measure microbolometer resistance. There are more advanced readout circuits developed for the resistive microbolometers, which are explained in detail in Chapter V.

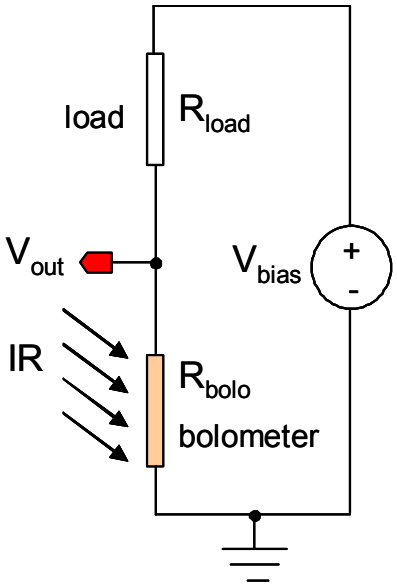


Figure 1.8: Simple half-bridge circuit used to measure microbolometer resistance.

The resistance of the microbolometer changes related with its TCR value and the temperature change due to the absorbed infrared radiation. The change in the detector resistance will cause a change in the output voltage of the half bridge, from which the incident infrared radiation can be measured. The output voltage of the half-bridge circuit is given as

$$V_{out} = V_{bias}\left(1 - \frac{R_{load}}{R_{bolo}\left(1+\alpha\Delta T\right) + R_{load}}\right) \tag{1.3}$$

where, V_{bias} is the bias voltage, R_{bolo} and R_{load} are the microbolometer and load resistance at a given operating temperature, α is the TCR of the microbolometer resistor, and ΔT is the temperature rise in the microbolometer pixel due to the absorbed infrared radiation.

1.4.2 Pyroelectric and Ferroelectric Detectors

There are some materials which exhibit transient electric polarization upon a rapid change in their temperatures. This effect is called pyroelectric effect, and detectors that make use of this feature are called pyroelectric detectors [11]. The temperature induced polarization causes formation of surface charges on opposite plates of the material generating a detector current given as [36]

$$i_d = pA\frac{dT}{dt} \tag{1.4}$$

where, p is the pyroelectric coefficient, A is area of the electrode, T is the detector temperature, and t is time. The above equation states that generated detector current is zero when the detector is excited at DC, since the induced polarization vanishes in time due to the internal charge flow through the material. Therefore, pyroelectric detectors can not be used in staring mode, and the incoming infrared energy should be modulated before detection. After modulation, there will be an alternating current whose amplitude can be measured and used to determine the incident infrared radiation level. Figure 1.9 shows the electrical model of the pyroelectric uncooled detector and its load [36].

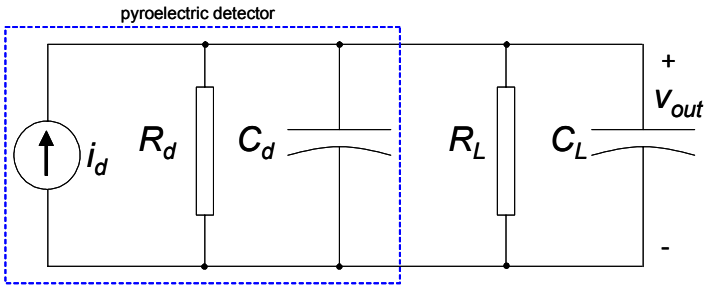


Figure 1.9: Electrical model of the pyroelectric uncooled detector and its load [36].

Pyroelectric effect vanishes above a certain temperature unique for each material, which is known as the Curie temperature. Furthermore, it is advantageous to operate the pyroelectric detectors just below their Curie temperatures due to the improved responsivity. The Curie temperature can be adjusted to be around room

temperature by adjusting the material compositions, at least for the composite materials, such as barium strontium titanate ($Ba_{1-x}Sr_x\ TiO_3$ or BSTO). When the Curie temperature is set as room temperature, the detector is operated just below it with the help of a thermo-electric temperature stabilizer [11].

Ferroelectric effect is the electric field-enhanced version of the pyroelectric effect, where a bias voltage is used to set up an internal electric field inside the detector material, which in turn boosts the device responsivity. Unlike the pyroelectric materials, the Curie temperature of these materials is well above the room temperature, and they do not require any temperature stabilizer. Monolithically integrated FPAs use ferroelectric materials and therefore, they do not require any temperature stabilizers [11]. Except the required bias circuitry, the same readout circuit used for the pyroelectric microbolometers can be used for the ferroelectric microbolometers.

Currently, there are 320 × 240 uncooled pyroelectric detector arrays using 48.5 μm × 48.5 μm pixels with about 100 % fill factor which are bump bonded to the readout circuit, providing an NETD value of 60 mK [18]. There are also efforts to fabricate these detectors monolithically [19]. However, fabrication of a monolithic array has not been demonstrated yet.

1.4.3 Thermoelectric Detectors

Thermoelectric detectors are formed using thermocouples, whose operation principle is based on the Seebeck effect. Figure 1.10 shows the schematic of a thermocouple. When two pieces of different materials A and B are joined and heated at one end, then there will be a potential difference between the two other ends of the structures depending on the difference of their Seebeck coefficients and the temperature difference between the hot and cold end points. The generated voltage is quite stable without a need for a bias.

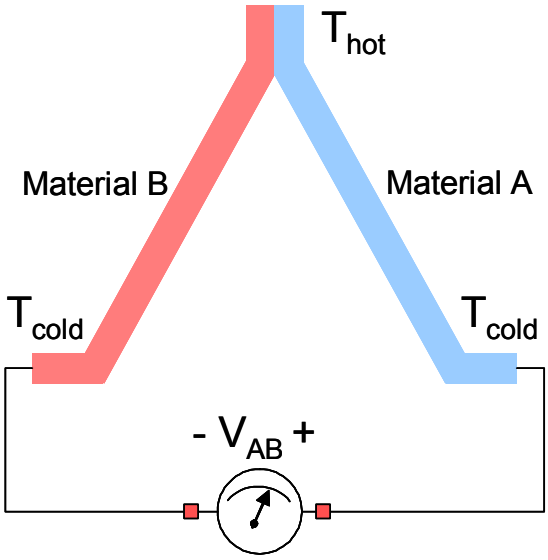


Figure 1.10: Schematic of a thermocouple.

The output voltage of a thermocouple (V_{AB}) is given as [2]

$$V_{AB} = (\alpha_A - \alpha_B)\Delta T_{hot-cold} \tag{1.5}$$

where, α_A and α_B are the Seebeck coefficients of the two different materials, and $\Delta T_{hot\text{-}cold}$ is the temperature difference between hot and cold junctions. The output voltage of a single thermocouple is usually not sufficient; therefore, a number of series connected thermocouples are used in infrared detection. This new structure is called thermopile, which can be constructed using metals or semiconductors. Since the Seebeck coefficients of the semiconductors are larger as compared to that of the metals, semiconductor thermopiles [1, 2, 31-33, 35, 50] are more responsive as compared to the metal counterparts [49]. For the semiconductor thermopiles, the magnitude and the sign of the Seebeck coefficient can be adjusted by adjusting the doping type and doping level. As any thermal detector, thermopiles are implemented on thermally isolated structures. Due to the requirement of many series connected thermocouple structures, the detector size can not be decreased below a certain size, and therefore pixel number in a possible focal plane array can not be increased as in the case of microbolometer FPAs. Figure 1.11 shows the SEM photograph of a semiconductor thermopile structure implemented using 20 n-poly/p^+ active

thermocouples in a standard n-well CMOS process developed at METU [50]. The structure measures 325 μm × 180 μm in a 1.2 μm CMOS process.

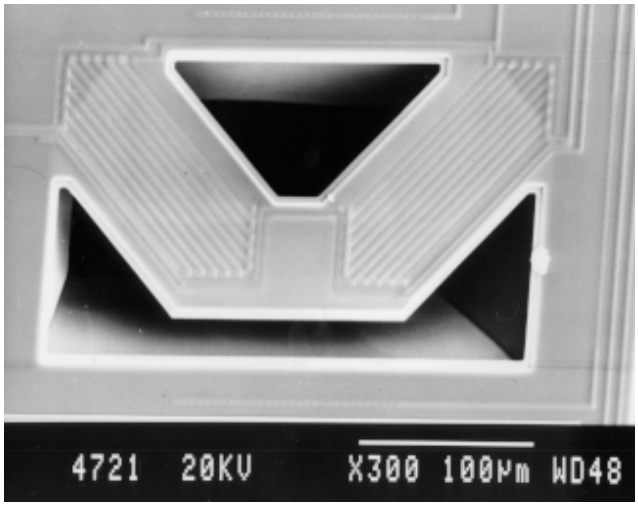


Figure 1.11: SEM photograph of a semiconductor thermopile structure implemented using 20 n-poly/p^+ active thermocouples in a standard n-well CMOS process developed at METU [50]. The structure measures 325 μm × 180 μm in a 1.2 μm CMOS process.

The uncooled infrared detectors implemented with thermopiles do not require temperature stabilizers due to their inherent differential operation between hot and cold junctions [2]. However, the temperature gradient in the thermopile array may cause significant offsets; therefore spatial variation in the array temperature should be minimized by careful array design. In one application it has been reported that the heat generated by the on-chip preamplifiers causes noticeable offset in the thermopile outputs [1]. Furthermore, the responsivity of the thermopiles are very low, in the order of 5 – 15 V/W, and the pixel sizes in these devices are large, such as 250 μm × 250 μm, limiting their use for large format detector arrays. Furthermore, these detectors require extra processing for thermal isolation between pixels, such as processing steps to obtain silicon islands [35] or electroplated gold lines [2]. Although there are successful implementations of thermopile arrays, their low responsivity values and large pixel sizes limit their performance and application areas.

1.4.4 Diode Type Microbolometers

Diode type microbolometer detectors use the variation in the diode current or diode voltage with the pixel temperature, depending on their biasing methods. Figure 1.12 shows a simple readout circuit used for the diode type microbolometers. The diode microbolometer is biased at constant current (I_{bias}), and the change in the detector voltage due to the incident infrared radiation is measured with respect to a reference voltage (V_{ref}). The output voltage (V_{out}) is given as

$$V_{out} = V_{ref} - \left(V_{D0} + \alpha_D \Delta T\right) \tag{1.6}$$

where V_{ref} is the reference voltage, V_{D0} is the detector voltage at the given bias current, α_D is the temperature coefficient of the diode forward voltage at the given bias level, and ΔT is the detector temperature change due to the absorbed infrared radiation.

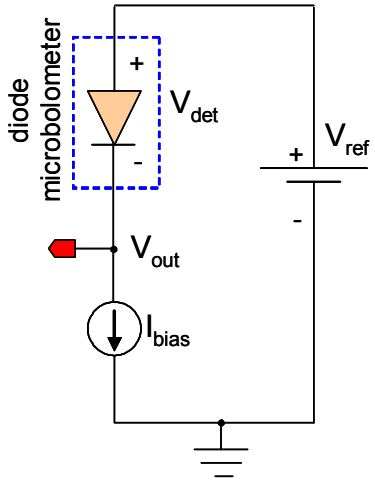
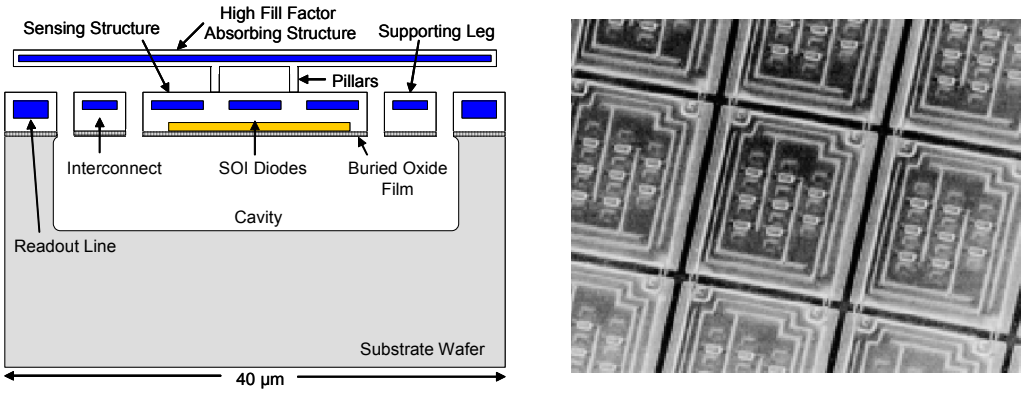


Figure 1.12: Simple readout circuit used for the diode type microbolometers.

The diode forward voltage changes related with the temperature coefficient of the pixel and the increase in the detector temperature due to the absorbed infrared radiation. Therefore, incident infrared radiation can be measured easily using the above circuit. There are other advanced readout circuits for the diode type microbolometers that are explained in detail in Chapter V.

In the literature, successful implementation of an uncooled 320 × 240 FPA based on suspended multiple series diodes with 40 μm × 40 μm pixel sizes fabricated on SOI wafers has been reported [28]. The reported NETD value is 120 mK for an f/1 optics at 30 fps scanning rate. Figure 1.13 (a) and (b) show the schematic of the detector cross section and SEM photograph of the fabricated SOI diode array pixels, respectively.



(a) (b)

Figure 1.13: SOI diode microbolometer: (a) schematic of the detector cross section and (b) SEM photograph of the fabricated SOI diode array pixels [28].

Although the SOI diode approach provides very uniform arrays with very good potential for low-cost high performance uncooled detectors, its fabrication is based on a dedicated in-house SOI process. Since these detectors can not be implemented in a standard CMOS process, it would be difficult to reduce their costs down to limits that ultra low-cost applications require. For ultra low-cost applications, the best approach would be to implement the detector arrays together with their readout circuitry fully in standard CMOS, using some simple post-CMOS etching steps where neither lithography nor detector material deposition steps are needed.

1.5 Low-cost Uncooled Infrared Detectors at METU

The research on uncooled infrared detectors started at METU in 1997. The goal of this work is to achieve very low-cost uncooled infrared detector array based

on bulk silicon micromachining etching on CMOS processed dies. Initial work started with resistive microbolometers, where n-well resistance is used as the sensitive detector material. Successful implementation of various 16 × 16 CMOS n-well microbolometer array prototypes using a commercial 0.8 μm CMOS process have also been demonstrated [36-38]. In these low-cost arrays, the pixel size and fill factor are 80 μm × 80 μm and 13 %, respectively. Figure 1.14 shows the SEM photographs of the fabricated and post processed 16 × 16 n-well microbolometer array. Although single pixel n-well microbolometer has much better performance parameters as compared to other CMOS compatible approaches, such as metal microbolometers or thermopiles, their performance decreases when an array is formed, due to the negative effect of the built-in pixel diode used to simplify the scanning of the arrays. Furthermore, their pixel size needs to be reduced to be able to implement large format FPAs such as 64 × 64 or 128 × 128. Hence, a different approach and fabrication technique is required to achieve small pixel size with reasonable performance.

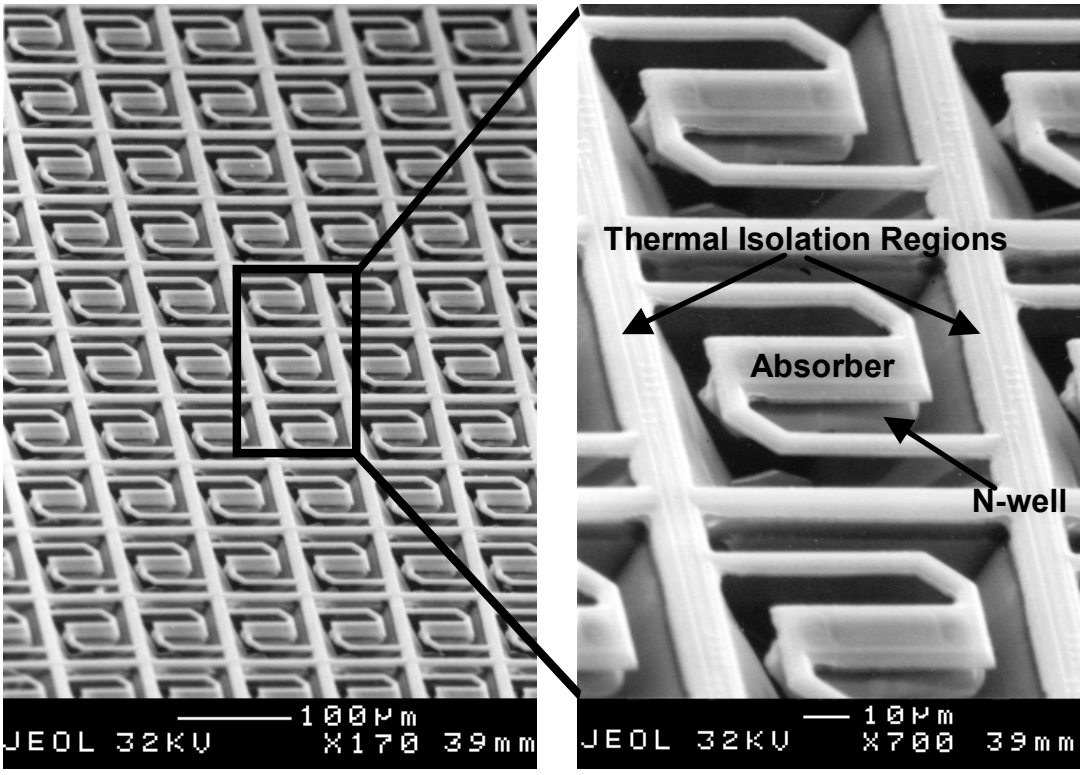


Figure 1.14: SEM photograph of the fabricated and post processed 16 × 16 n-well microbolometer array [36-38].

The work presented in this thesis reports the development of a new low-cost uncooled microbolometer FPA together with the monolithic readout circuitry implemented using a standard CMOS process. The developed detector pixel is based on the p^+-active /n-well diode that can be implemented in any standard n-well CMOS process [39, 40]. The size of the fabricated p^+-active /n-well diode microbolometer detectors are 40 µm × 40 µm with a fill factor of 44 % suitable for very low cost large format FPAs. Within the framework of this thesis, a 64 × 64 [41] and a 128 × 128 [42] FPA have been designed and fabricated together with their on-chip readout circuitry providing estimated NETD values of 0.8 K and 1 K, respectively for f/1 optics at 30 fps scanning rate. Figure 1.15 shows the perspective view of the p^+-active/n-well diode microbolometer that can be obtained in a standard n-well CMOS process [39].

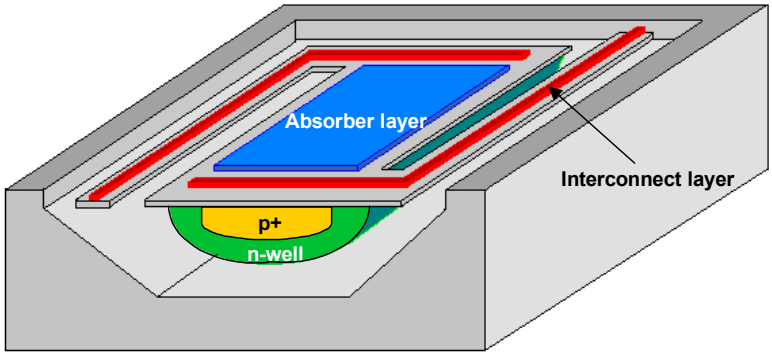


Figure 1.15: Perspective view of the p^+-active/n-well diode microbolometer that can be obtained in a standard n-well CMOS process [39].

Figure 1.16 shows the layout of the fabricated uncooled infrared imager chips with low-noise on-chip readout circuitry. The 64 × 64 FPA chip has 16-channel parallel readout circuitry, and it measures 4.1 mm × 5.4 mm in a 0.35 µm CMOS process. The 128 × 128 FPA has 32-channel parallel readout circuits, and it measures 6.6 mm × 7.9 mm in the same process [42]. The FPAs are fabricated using a standard 0.35 µm CMOS process followed by simple post-CMOS bulk micromachining that does not require any critical lithography or complicated deposition steps; and therefore, the cost of the uncooled FPA is reduced considerably. The post-CMOS fabrication steps include an RIE etching to reach the

bulk silicon and an anisotropic silicon etching to obtain thermally isolated pixels. During the RIE etching, CMOS metal layers are used as masking layers, and therefore, narrow openings such as 2 μm can be defined between the support arms. This approach allows achieving small pixel size of 40 μm × 40 μm with a fill factor of 44 %. The details of the post-processing steps are studied within another thesis work [51].

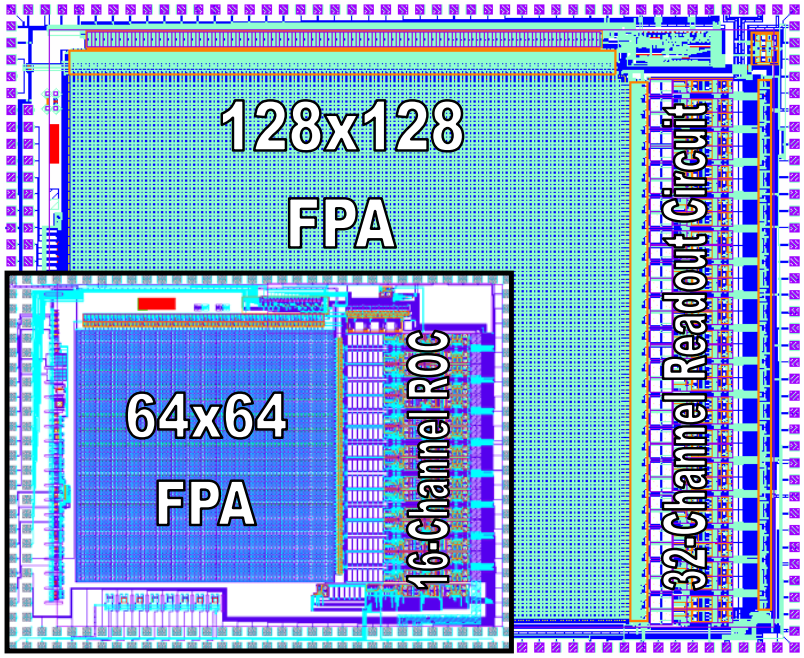


Figure 1.16: Layout of the fabricated uncooled infrared imager chips with on-chip readout circuitry. The 64 × 64 FPA chip has 16-channel parallel readout circuitry, and it measures 4.1 mm × 5.4 mm in a 0.35 μm CMOS process. The 128 × 128 FPA has 32-channel parallel readout circuitry, and it measures 6.6 mm × 7.9 mm in the same process [42].

1.6 Research Objectives and Thesis Organization

The goal of this research is to develop new low-cost uncooled infrared detector arrays together with integrated readout circuitry using MEMS and standard CMOS technologies. The specific objectives can be listed as follows:

1. Design of an optimized uncooled detector pixel. The detector should be CMOS compatible and its size should be small enough to allow fabrication of

low-cost uncooled FPAs. The detector should provide still acceptable performance at reduced pixel dimensions and at reduced biasing levels. For pixel size reduction, submicron fabrication technologies should be considered together with improved post-CMOS fabrication techniques, and the pixel optimization tasks should be carried out in accordance with these fabrication technologies. The effect of pixel size, interconnect material type, and biasing conditions on the detector performance should be analyzed, and optimum device dimension and biasing conditions should be determined.

2. Development of a 64 × 64 FPA using the optimized detector structure with monolithically integrated readout circuitry. The pixels in the array should be read out by an integrated readout circuitry which contains a multiplexer for pixel selection, a preamplifier circuit for signal conditioning, and a digital scanning control circuitry that generates all the required timing signals for proper operation of the FPA at scanning rates up to 30 fps. Possibility of parallel readout architectures should be investigated in order to decrease the electrical bandwidth and total electrical noise. The designed readout circuit should be able to apply bias potentials to the array pixels by a special etching circuitry without affecting normal FPA operation. Furthermore, the design of the scanning circuits should enable accessing the FPA pixels for uniformity tests. The design of the readout circuit should be performed in such a way that uniformity errors can be compensated during normal operation, at least at some lower scanning rates. The designed FPA should have individual detector pixels and standalone circuit modules for electrical and optical tests.

3. Development of an improved 128 × 128 FPA using the optimized pixel design. The new FPA should be tolerant to the effects of routing resistance in the enlarged FPA. The readout circuit should use differential low-noise preamplifiers and sufficient number of reference detectors to minimize the effect of temperature variations and self-heating.

4. Development of the required test setups for single pixel characterization and electrical tests of the fabricated arrays. Discrete low-noise preamplifiers

should be designed and implemented that can be used in the noise and infrared responsivity measurement of the single pixels. The uniformity of the fabricated arrays should be measured using a computer based data acquisition setup. In this test, the fabricated FPA should be interfaced to the data acquisition system properly using a multi-layer printed circuit board that can integrate all the required external electronics to minimize noise coupling.

The organization of this thesis and the contents of the following chapters can be summarized as follows:

Chapter II discusses the figures of merits used to compare the various infrared detectors. It gives the definition of basic parameters such as NETD and D^*, and the detector parameters that effect the detector performance. The maximum obtainable performance limits of the detectors are also given in this chapter.

Chapter III introduces the structure of the n-well microbolometer, which has also been used in the resistive detector arrays. It gives the structure and proposed fabrication procedure of the diode type n-well microbolometer together with its advantages. This chapter also includes detailed simulation results performed to determine the optimum detector structure, which are used to estimate the performance of the n-well microbolometer.

Chapter IV presents the test results of the fabricated and successfully post-processed single pixel n-well diode type microbolometer detectors. The performed tests include the temperature sensitivity, infrared responsivity, spectral absorption, and electrical noise measurements.

Chapter V explains different preamplifiers circuits used in the uncooled infrared detector arrays. Noise calculations of the different preamplifier circuits are presented, and the preamplifier circuit developed for the n-well diode type FPAs is introduced.

Chapter VI and VII explain the design details of the fabricated 64 × 64 and 128 × 128 FPAs based on the n-well diode type microbolometer. The FPA architecture and the operation principles of the readout circuit blocks are given in detail.

Chapter VIII gives the electrical test results of the fabricated FPAs. Array uniformity tests and electrical tests that verify the proper operation of the analog and digital readout circuit modules are presented.

Finally, Chapter IX summarizes this research work and gives conclusions together with the list of possible future work related to this study.

CHAPTER II

2 FIGURE OF MERITS FOR THERMAL DETECTORS

This chapter explains the common figure of merits to evaluate performance of different kinds of infrared detectors including photonic and thermal detectors. The most important figures of merits are the responsivity ($\Re$), thermal time constant (τ), noise equivalent power (NEP), noise equivalent temperature difference (NETD), and detectivity (D^*). In the following sections, each of these parameters is explained in detail, and their measured results are given in the Chapter V. Section 2.1 defines responsivity, and explains detector parameters that affect the responsivity. This section also gives responsivity expression for both resistive and diode type microbolometer detectors. Section 2.2, 2.3, and 2.4 give the definitions of NEP, NETD, and D^*, respectively. Section 2.5 explains the fundamental performance limitations of the thermal infrared detectors such as background and temperature fluctuation noise limitations. Finally, Section 2.6 gives the summary of the important parameters used in the comparison of different detector types.

2.1 Responsivity

Responsivity of a detector is defined to be the ratio of the detector output signal to the infrared power incident on the active part of the detector. It applies both to the single pixels and pixels of an array. The output of a detector may either be

voltage or current; therefore, $\Re$ is expressed in Volts/Watt (V/W) or Amps/Watt (A/W), which actually depends on the biasing circuit used.

In order to have high detector responsivity in thermal detectors, the temperature sensitivity of the detector material should be high, and the detector should be well isolated from its ambient so that it can easily be heated up with the absorbed infrared radiation. The temperature sensitivity of the detector is given in terms of temperature coefficient of resistance (TCR) for the resistive microbolometers, and as temperature coefficient of some electrical variable (current or voltage) for the microbolometers that use active devices, such as transistors or diodes. The thermal isolation level is represented by the thermal conductance value (G_{th}). For a good detector, the starting point should be to place a high TCR material or a device with high temperature sensitivity on a thermally isolated structure with the minimum possible G_{th} value. Furthermore, the thermal mass or thermal capacity (C_{th}) of the detector should also be minimized in order for the detector to follow rapid changes in the incoming infrared radiation.

Figure 2.1 shows the thermal equivalent circuit for a microbolometer detector with thermal conductance of G_{th} and thermal capacitance of C_{th}. The incident infrared radiation has a power level of P_0 modulated at ω_0, and only a portion of the incident power related to the absorption coefficient (η) is absorbed and converted into heat. One terminal of the detector is at the thermal ground, and the temperature difference between the terminals is taken as output denoted as ΔT.

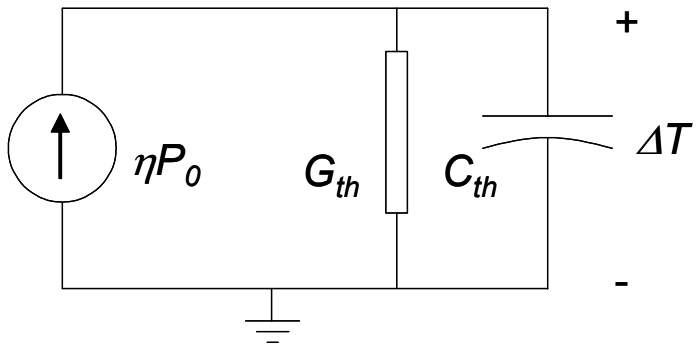


Figure 2.1: Thermal equivalent circuit of the microbolometer detector.

The magnitude of the steady state temperature variation due to the applied modulated infrared radiation is given as [11]

$$| \Delta T | = \frac{\eta P_0}{G_{th}\sqrt{1+(\omega_0 \tau)^2}} \tag{2.1}$$

where, η is the absorption coefficient of the detector, P_0 is the magnitude of the incident infrared radiation modulated at ω_0, and G_{th} is the thermal conductance of the detector with a thermal time constant of τ, which is given by

$$\tau = \frac{C_{th}}{G_{th}} \tag{2.2}$$

where, C_{th} is the thermal capacitance, and G_{th} is the thermal conductance. The magnitude of temperature rise improves as the thermal isolation improves with reduced G_{th} value. The thermal capacitance and conductance forms a pole with a 3 dB frequency (f_{3dB}) given as

$$f_{3dB} = \frac{1}{2\pi\tau} \tag{2.3}$$

where, τ is the thermal time constant of the detector. As the thermal time constant (τ) is decreased, the 3 dB frequency is shifted to higher frequencies so that the detector output can follow more frequent changes in the incident infrared radiation.

The rise in pixel temperature causes a proportional change in the detector voltage related with its temperature coefficient of that particular detector type. For a resistive microbolometer biased at constant current, the magnitude of the output variation due to the modulated radiation is given as [11]

$$| \Delta V_b | = \alpha I_b R_b | \Delta T | = \frac{\alpha I_b R_b \eta P_0}{G_{th}\sqrt{1+(\omega_0 \tau)^2}} \tag{2.4}$$

where, α is the TCR value of the resistive microbolometer, I_b is the bias current value, R_b is the microbolometer resistance, η is the absorption coefficient, P_0 is the

incident infrared power, G_{th} is the thermal conductance, ω_0 is the infrared modulation frequency, and τ is the thermal time constant. If the detector is a diode type microbolometer, then the output voltage is given as

$$|\Delta V_b| = TC_D |\Delta T| = \frac{TC_D \eta P_0}{G_{th}\sqrt{1+(\omega_0 \tau)^2}} \tag{2.5}$$

where, TC_D is the temperature coefficient of the diode forward voltage, η is the absorption coefficient, P_0 is the incident infrared power, G_{th} is the thermal conductance, ω_0 is the infrared modulation frequency, and τ is the thermal time constant. Responsivity ($\Re$) can be calculated by dividing the output voltage to the incident power level. The responsivity value for the resistive and diode type detectors are given as

$$\Re_{res} = \frac{\alpha I_b R_b \eta}{G_{th}\sqrt{1+(\omega_0 \tau)^2}} \tag{2.6}$$

$$\Re_{diode} = \frac{TC_D \eta}{G_{th}\sqrt{1+(\omega_0 \tau)^2}} \tag{2.7}$$

where, $\Re_{res}$ [11] and $\Re_{diode}$ are responsivity values for the resistive and diode type detectors biased at a constant current, respectively.

2.2 Noise Equivalent Power (NEP)

Noise equivalent power (NEP) is defined as the input power level that would generate a detector output voltage (or current) equal to the root-mean-square (rms) noise voltage (or current) of the detector. NEP of a detector with voltage output is given as [11]

$$NEP = \frac{V_n}{\Re} \tag{2.8}$$

where, V_n is the detector root-mean-square (rms) noise voltage, and $\Re$ is detector voltage responsivity. While giving the NEP value, it is necessary to mention the

corresponding electrical bandwidth and the scanning rate. When a detector is scanned at higher rates, its responsivity will decrease due to the finite thermal time constant. Furthermore, the electrical bandwidth will increase, which results an increase in the rms noise voltage affecting the NEP value.

2.3 Noise Equivalent Temperature Difference (NETD)

NETD value of the uncooled detectors can be defined as the change in the temperature of a blackbody that results in the signal to noise ratio of unity in the detector output signal [11]. The same definition also applies when the detector is integrated with a readout circuit; therefore, it is important to specify which definition is used while giving the NETD value. A small NETD value indicates that the detector can resolve very small temperature changes in the scene, and such a small NETD value can be obtained using high performance detector with a small noise level and high responsivity. The NETD expression involves the detector parameters, such as electrical noise, active detector area, and NEP, as well as parameters related to the optics used, and some fundamental parameters, such as the variation of spectral power density of a blackbody with respect to temperature. Figure 2.2 shows the simplified optical setup used in thermal detection.

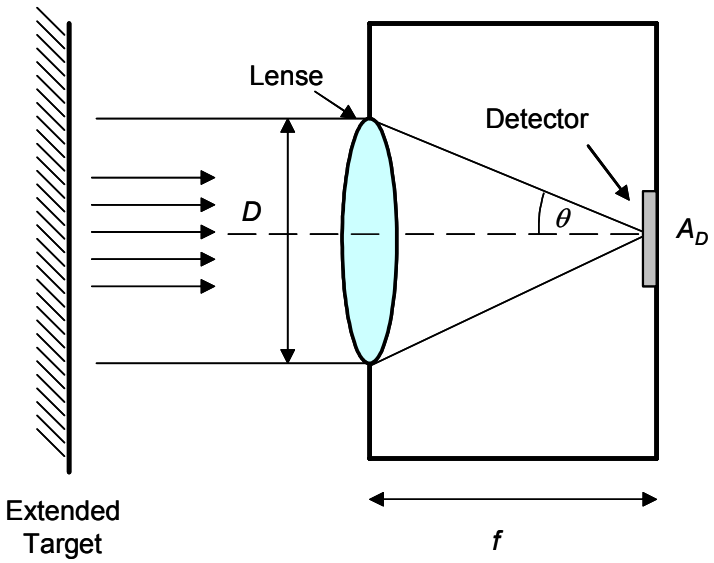


Figure 2.2: Simplified optical setup used in thermal detection [14].

For a lossless optical setup, the change in incident power onto the detector upon one Kelvin change in the extended target is given as [14]

$$\Delta P_{\text{det}} / dT_{target} = (\Delta p_{target} / \Delta T_{target})_{\lambda_1 - \lambda_2} A_D \sin^2 \theta \tag{2.9}$$

where, θ is the half angle shown in the above figure, A_D is the active detector area, and the term in the parenthesis ($\Delta p_{target} / \Delta T_{target}$) gives the change in the radiated power at the target side per Kelvin and per unit area for π steri-radians. This term depends on the wavelength of incident radiation. For the 3-5 μm and 8-12 μm bands, the value of this term is 2.1×10^{-5} W(cm^{2}K)$^{-1}$ and 2.62×10^{-4} W(cm^{2}K)$^{-1}$ at 300 K, respectively [14]. By using the geometrical dimensions of the imaging setup, such as the diameter (D) and focal length (f) of the optics, $\sin\theta$ can be expressed as [14]

$$\sin^2(\theta) = \frac{(D/2)^2}{f^2 + (D/2)^2} = \frac{1}{4(f/D)^2 + 1} \tag{2.10}$$

where, D is diameter, and f is the focal length of the optics. There is also another optical parameter called F-number (F), which is defined as [14]

$$F = \frac{1}{2\sin\theta} \tag{2.11}$$

where, θ is the half angle shown in Figure 2.2. Equation 2.9 can be expressed in terms of F as

$$\Delta P_{\text{det}} / dT_{target} = \frac{\Delta p_{target} / \Delta T_{target} A_D}{4F^2} \tag{2.12}$$

which gives the change in power incident to the detector active area (A_D) upon one Kelvin change in the target temperature. Using this relation, it is possible to determine the minimum temperature variation on the target limited by the noise equivalent power of the detector (NEP). This parameter is called noise equivalent temperature difference (NETD), and NETD is given as [14]

$$NETD = \frac{NEP}{\Delta P_{\det} / dT_{target}} = \frac{4F^2 NEP}{A_D \Delta p_{target} / \Delta T_{target}} = \frac{4F^2 V_n}{A_D \Re(\Delta p_{target} / \Delta T_{target})_{\lambda_1 - \lambda_2}} \quad (2.13)$$

where, F is the F-number of the optics, V_n is the electrical noise, A_D is the active detector area, $\Re$ is the responsivity, and the term in the parenthesis ($\Delta p_{target} / \Delta T_{target}$) is a constant defined previously. In order to be able to resolve small temperature variation on the targets, the NETD value of the detector should be as small as possible. To reduce the NETD value, NEP of the detector should be decreased as much as possible. At the initial design phase, a suitable detector size should be selected, and the pixel should be designed with the maximum possible responsivity value. Note that, NETD is inversely proportional with the detector active area. Therefore, is difficult to reduce the NETD value for smaller pixels, and for a given pixel size, the detector should be designed with maximum achievable fill factor. Noise of the detector should also be reduced by limiting the electrical bandwidth of the detector. Infrared optics also affects the NETD value, and smaller focal ratio (*f/D*) should be used to decrease the NETD value; however, optics with smaller focal ratio is usually expensive. Modern thermal cameras use focal ratios ranging from 0.8 [28] to 1.8 [23].

2.4 Detectivity (D^*)

Detectivity (D^*) is a normalized parameter that is used to compare the performance of different detector types with different pixel size and operating at different scanning rates, and detectivity is given as [14]

$$D^* = \Re \frac{\sqrt{A_D \Delta f}}{V_n} = \frac{\sqrt{A_D \Delta f}}{NEP} \quad (2.14)$$

where, A_D is the active area of the pixel, Δf is the electrical bandwidth, $\Re$ is the detector responsivity, and V_n is total rms noise voltage measured in the specified bandwidth. A high performance detector should have a high D^* value, which indicates a high responsivity and a low noise spectral density. Since the detector

noise voltage increases with the square roof of the electrical bandwidth, detectors that have different electrical bandwidths due to their readout architectures can be compared using their D^* values, provided that the scene is scanned at the same rate. In most of the detectors the signal-to-noise ratio of the detectors depends on the square root of the active detector area, and it improves as the detector area increases. Therefore, normalizing the noise voltage with the square root of the active detector area allows us to compare detectors with different active areas.

For the photon detectors, responsivity varies very much with the wavelengths, and for those detectors it is necessary to indicate the wavelength at which the D^* value is given, and to denote the wavelength dependency D^*_λ is used. It is also possible to give the detectivity as blackbody detectivity, whose symbol is $D^*(T)$, where T is blackbody temperature. For most of the thermal detectors, the responsivity has a relatively flat response, and only $D^*(T)$ is specified for the thermal detectors. However, there is still some dependency of the responsivity on the wavelength due to the absorption characteristics of the absorber material or due to the different geometries of the resonant optical cavity structures used to improve the absorption level.

2.5 Fundamental Limits

There are fundamental limitations for the maximum performance that a detector can achieve. These limitations arise due to the statistical nature of the energy exchange between the ambient and the detector body either through conduction or radiation. There are basically two kinds of limits that are encountered for the thermal detectors: 1) background fluctuation noise limit and 2) temperature fluctuation noise limits. The first one is due to the statistical emission of the photons from the radiating background. Random emission of photons causes fluctuations in the absorbed power acting as a noise source which is also called photon noise. The latter occurs due to the energy exchange between the detector body and substrate through conduction or convection, which results in random fluctuations in the

detector temperature, and this noise source is called thermal fluctuation noise. These two noise sources will be explained in detail in the coming sections.

2.5.1 Background (Photon) Noise Limit

The analysis of the background (photon) noise in the thermal detectors is different as compared to the photon detectors, in that the detection mechanism is based on absorption of the incoming radiation rather than the rate of photon absorption. The power spectral density of the sum of the photon noise that is radiated and absorbed by the detector, and radiated by the detector and absorbed by the background is given as [14]

$$p_{photon}^2 = 4kT^2 G_{rad} \tag{2.15}$$

where, k is the Boltzmann constant, T is temperature of both the detector and ambient, and G_{rad} is thermal conductance of the radiation losses, and G_{rad} is defined as

$$G_{rad} = 4A_D \eta \sigma T^3 \tag{2.16}$$

where, A_D is the active detector area, η is the absorption coefficient (equivalently emissivity), and σ is the Stefan's constant. The Stefan's constant is defined as [11]

$$\sigma = \frac{2\pi^5 k^4}{15c^2 h^3} \tag{2.17}$$

where, k is the Boltzmann constant, c the speed of light, and h is Plank's constant. Here, it is assumed that η is independent of temperature and wavelength. However, this assumption is not true for most of the thermal detectors in that they exhibit some spectral selectivity, therefore corrections is required for the above simplified equation [11].

It should be noted that p_{photon} is equal to the spectral density of the noise equivalent power, therefore, using Equation 2.11, maximum achievable detectivity in background (photon) fluctuation noise limiting case (D^*_{BF}) is given as [14]

$$D^*_{BF} = \sqrt{\frac{\eta}{16\sigma k T^5}} \tag{2.18}$$

Note that background (photon) noise limited detectivity, $D^*_{BF,}$ is independent of active detector area, which is an expected result for a limiting value that should be valid for each and every kind of detectors for which the above mentioned assumptions hold. For a detector with unity absorption coefficient, background noise limited detectivity is equal to 1.8×10^{10} cmHz$^{1/2}$/W when both the detector and ambient is at 300 K, which is a theoretical limit for the thermal detectors. If the modified version of the p_{photon} is used, then the photon noise limited D* will also be changed accordingly [14].

2.5.2 Temperature Fluctuation Noise Limit

Each thermal detector is subject to random variations in its temperature due to the statistical nature of heat transfer through conduction and radiation. The power spectral density of a hypothetical detector with zero thermal mass and finite thermal conductance is given as [14]

$$p^2_{thermal} = 4kT^2G \tag{2.19}$$

where, k is the Boltzmann constant, T is the temperature of the detector and its surrounding in Kelvin, and G is the thermal conductance of the detector which is equal to the sum of the thermal conductance of the support arms (G_{arm}) and thermal conductance of the radiation losses (G_{rad}). It should be noted that, temperature fluctuation still exists even though the detector and the surrounding are at the same temperature. This can be considered to be analogous to the thermal noise current of a resistor, which flows even if there is no net electric field inside the resistor. The

finite thermal mass of the detector will limit the bandwidth of thermal fluctuation noise by introducing a pole related with its thermal time constant. The frequency dependent power spectral density is given as [14]

$$p_{thermal}^2 = \frac{4kT^2G}{1+(\omega\tau)^2} \tag{2.20}$$

where, k is the Boltzmann constant, T is the temperature, G is the thermal conductance, ω is the natural frequency, and τ is thermal time constant of the detector. The damping introduced by the finite time constant (τ) results in an effective bandwidth given as [14]

$$\Delta f_{eff} = \frac{1}{4\tau} \tag{2.21}$$

where, τ is thermal time constant of the detector. If the electrical bandwidth extends beyond the pole introduced by the reciprocal of τ, then the total integrated noise power will be given as [14]

$$P_{thermal}^2 = 4kT^2G\Delta f_{eff} = \frac{kT^2G}{\tau} = \frac{kT^2G^2}{C} \tag{2.22}$$

where, C is the thermal mass of the detector. The total integrated temperature fluctuations is given as [14]

$$\Delta T_{thermal}^2 = \frac{kT^2}{C} \tag{2.23}$$

where, k is the Boltzmann constant, T is the temperature, and C is the thermal capacitance of the detector. For staring detectors that operate at DC (zero natural frequency), the thermal capacitance of the detector has no affect on the temperature fluctuation noise, and the thermal fluctuation noise limited detectivity (D^*_{TF}) is given as [14]

$$D^*_{TF} = \sqrt{\frac{\eta^2 A_D}{4kT^2 G}} \tag{2.24}$$

where, η is the absorption coefficient, A_D is the active detector area, k is the Boltzmann constant, T is temperature, and G is the thermal conductance. For the scanned detectors for which the bandwidth extends well beyond the pole introduced by the thermal time constant, the thermal noise limited D^* is given as

$$D^*_{TF} = \sqrt{\frac{\eta^2 A_D \Delta f \tau}{kT^2 G}} \tag{2.25}$$

where, η is the absorption coefficient, A_D is the active detector area, Δf is the electrical bandwidth, τ is the thermal time constant, k is the Boltzmann constant, T is temperature, and G is the thermal conductance. It is interesting to note that the D^*_{TF} can be larger for the scanned detectors, since most of the time the product, $\Delta f \tau$, is larger than 1/4, which is due to the fact that the electrical bandwidth involved in these scanned detectors is much larger than the effective thermal bandwidth ($1/4\tau$). This in turn results in a much smaller noise density as compared to the detectors operated at DC [14].

It should also be noted that thermal fluctuation noise limit also includes the photon noise limit, and the two limits become identical when the thermal conduction becomes negligible. For this to happen, thermal conductance of the support arms should be below the radiation thermal conductance value, which is equal to 3.8×10^{-9} W/K for a 50 μm × 50 μm detector with an absorption coefficient of 0.5 and a fill factor of 50 %. Typical support arm thermal conductance for most of the modern thermal detectors is about 20 times larger than the radiation thermal conductance value, and their noise level is much above the background noise level; therefore the thermal detectors are limited by the thermal fluctuation noise. At the time of writing this thesis, there are photonic cooled infrared detectors that are background noise limited, and all of the thermal detectors are thermal fluctuation noise limited. As the technology develops, it is expected that the performance of the uncooled scanned arrays become close to that of cooled detectors.

2.6 Conclusions

This chapter explained the figure of merits used in the performance comparison of different type infrared detectors. These parameters include responsivity ($\Re$), noise equivalent power (NEP), noise equivalent temperature difference (NETD), and normalized detectivity (D^*). Section 2.1, 2.2, 2.3, and 2.4 explained responsivity, NEP, NETD, and D^*, respectively. Finally, Section 2.5 discussed fundamental performance limits of the thermal infrared detectors. These limits are the background noise limit and temperature fluctuation limit, where it has been indicated that the thermal detectors are limited by the temperature fluctuation noise.

CHAPTER III

3 N-WELL DIODE TYPE MICROBOLOMETER DETECTOR

This chapter presents the details on the design and optimization of a new small size low-cost uncooled microbolometer detector. The detector is based on suspended and thermally isolated p^+-active/n-well diodes fabricated in a standard 0.35 μm CMOS process. After CMOS fabrication a simple post-processing method is used, which does not require any critical lithography or complicated deposition steps. Using this approach, it is possible to reduce the pixel size and increase the fill factor suitable for large format arrays with 64 × 64 and 128 × 128 pixel resolutions.

In the following sections, the pixel structure and its corresponding post-processing method are explained. Effect of various pixel parameters on the detector performance are presented with MATLAB simulations. Section 3.1 gives the pixel structure of the p^+-active/n-well diode type microbolometer. Section 3.2 gives the pixel optimization simulation results and gives the performance estimates. Using the simulation results, optimum pixel size and optimum pixel bias are determined, and temperature sensitivity, responsivity, NETD, and D^* values are estimated. Section 3.3 explains the self-heating effect and compares the self-heating of the p^+-active/n-well diode microbolometer with that of the resistive n-well microbolometer. Finally, Section 3.4 summarizes the pixel design and optimization.

3.1 Pixel Structure

Figure 3.1 shows a perspective view of the p^+-active/n-well diode microbolometer that can be obtained in a standard n-well CMOS process [39-42]. Infrared radiation heats the absorbing layer on the thermally isolated n-well, increasing its temperature, which in turn results in a change in the diode forward voltage related to its temperature coefficient. Bulk silicon under the n-well is etched away to reduce the thermal conductance and to increase the responsivity of the detector. To obtain high thermal isolation the interconnect material on support arms are fabricated using polysilicon. This thermally isolated suspended structure is obtained by front-end bulk etching of the fabricated CMOS dies, where the electrochemical etch-stop technique is used to prevent the etching of the n-well [39-45].

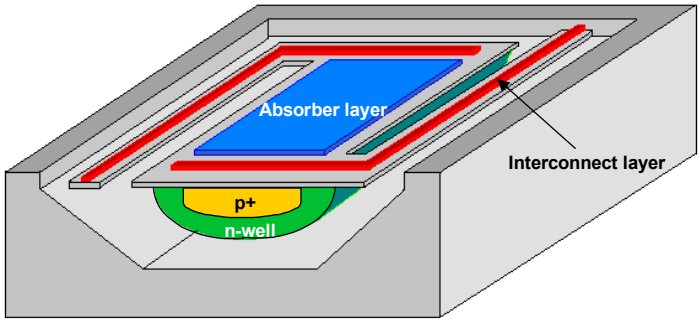


Figure 3.1: Perspective view of the n-well diode microbolometer that can be obtained in a standard n-well CMOS process [39-42].

The pixel size and fill factor are determined by process limitations, such as the minimum interconnect width and opening between the arms that allow silicon to be exposed to the solution during etching. To improve the fill factor, etch openings are drawn at their minimum possible dimensions, and no initial oxide openings are created on the CMOS fabricated devices. The required etch openings are created in a simple dry etch process using metal layers in the process as protection mask [52]. After the necessary openings are created on the surface to reach the silicon substrate, the silicon underneath the pixel is removed in an anisotropic silicon etchant called tetramethyl ammonium hydroxide (TMAH), while the electrochemical etch-stop

process is used to prevent the etching of the n-well layer. Figure 3.2 shows the post-CMOS fabrication steps and the cross-section of the pixel structure after (a) CMOS process, (b) dry-etch, and (c) anisotropic silicon etch [39-42, 51]. At the beginning, the surface of the pixel is covered with oxide. After dry-etching, all the oxide not protected by metal layers is etched down to silicon substrate, and the protected regions are stopped at that particular metallization level. Silicon underneath the pixel is removed by using front-end bulk silicon micromachining technique. Finally, the metal mask layers are removed by a simple metal etch process.

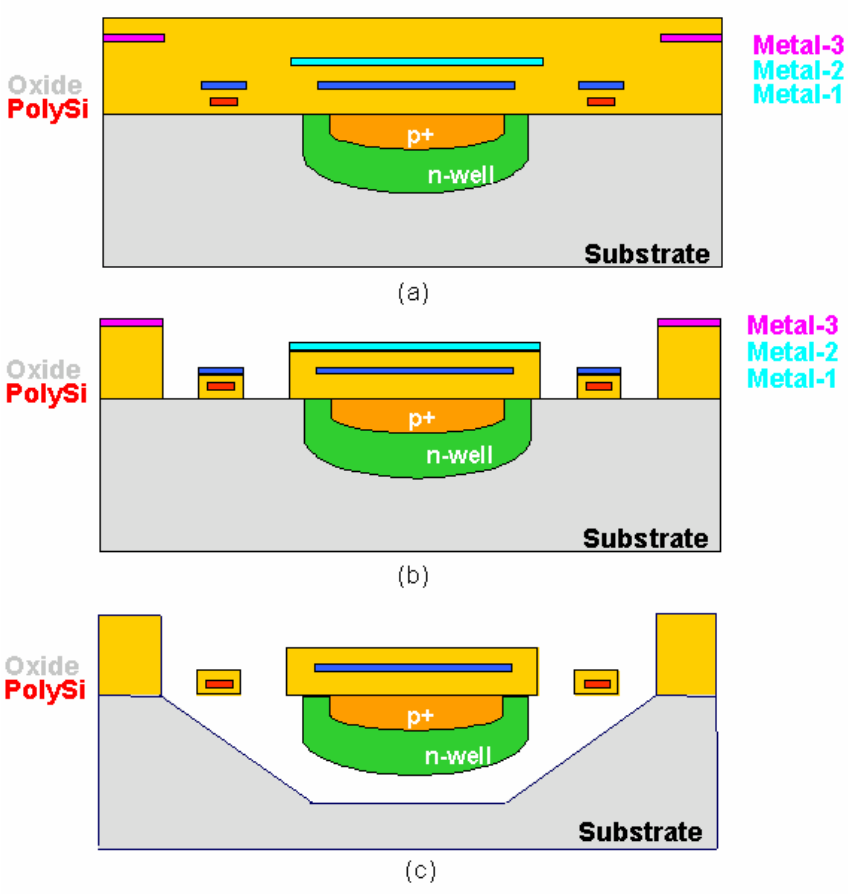


Figure 3.2: The post-CMOS fabrication steps and the cross-section of the diode pixel structure (a) after CMOS process, (b) after dry etch, and (c) anisotropic silicon etch [39-42, 51].

This approach has a number of advantages. First of all, it does not require any critical lithography step after the CMOS process, reducing the cost of the

detectors. In addition, the gaps between the support arms can be reduced as the CMOS technology allows, making it possible to reduce the pixel size while increasing the fill factor. Also, there is no need for any complicated post-CMOS deposition or surface micromachining steps. Therefore, the detector cost is almost equal to the cost of the CMOS chip.

Since the detectors are implemented using diodes on single crystal silicon, their 1/*f* noise contribution is negligibly small especially at low bias levels, where low bias level also helps decreasing the 1/*f* noise contribution of the polysilicon interconnects.

3.2 Pixel Optimization and Performance Analysis

The performance of the p^+-active/n-well microbolometer pixel is affected by a number of design parameters and material characteristics, including absorber layer on the pixel, interconnect layer on the support arms, pixel size, opening and support arm widths, and fill factor. As absorber layer, a sandwich layer composed of oxide and metal is used, which can be formed in any CMOS process. These layers produce an absorptance of 30-80 % in the 8-14 μm bands, depending on composition of the sandwich layer [2, 45]. The interconnects of the pixel are implemented using polysilicon layer to improve the thermal isolation. The thermal isolation is further improved with the use of L-shaped supporting structures. The diode is implemented in the middle of the pixel and occupies most of the n-well area in order to avoid performance degradation due to the n-well resistance.

3.2.1 Optimum Pixel Size

Table 3.1 gives the material [53] and process [54] properties used in the determination of the optimum pixel size for the diode type microbolometer detector. Among them the thermal conductivity value is very important in that it directly affects the NETD and D^* values. Sheet resistance of the material determines the electrical resistance of the interconnects and their electrical noise contributions.

Table 3.1: Material [53] and process [54] properties used in the determination of the optimum pixel size for the diode type microbolometer detector.

Layer	**Thickness** (nm)	**Sheet Resistance** (Ω/ □)	**Thermal Conductivity** (W/mK)
Polysilicon	275	7	18
Metal	670	0.08	180
Oxide	930	∞	1.16

In order to determine G_{th} as precisely as possible, thermal conductance of the oxide layer (G_{th_oxide}) in the support arms and the radiation losses ($G_{th\_radiation}$) [14] are included in addition to the dominant part coming from the thermal conductance of the polysilicon interconnects (G_{th_poly}), which are calculated as

$$G_{th} = G_{th\_poly} + G_{th\_oxide} + G_{th\_radiation} \tag{3.1}$$

$$G_{th\_poly} = 2\frac{\sigma_{poly} t_{poly} w_{poly}}{L_{arm}} \tag{3.2}$$

$$G_{th\_oxide} = 2\frac{\sigma_{oxide} t_{oxide} w_{oxide}}{L_{arm}} \tag{3.3}$$

$$G_{th\_radiation} = [8\eta(\frac{2\pi^5 k^4}{15c^2 h^3})T^3]A_D \tag{3.4}$$

where σ is thermal conductivity, t and w are the thickness and width of the cross-section of the layers, L_{arm} is the mean length of a single support arm, η is the absorption coefficient, k is the Boltzmann constant, c the speed of light, and h is Plank's constant, T is the temperature, and A_D is the detector area. The factor of two in the thermal conductance of polysilicon and oxide layers are used since the detector is connected to the substrate via two support arms. Radiation thermal conductance value is calculated assuming that both of the detector surfaces are radiating, and the value in brackets is equal to 5.5×10^{-4} W/(Kcm^2) for a detector with 0.45 absorption coefficient operating 300 K.

To determine the optimum pixel size, a parametric pixel layout has been drawn and simulated in MATLAB [55] in terms of thermal conductance (G_{th}), NETD, and D^*. Figure 3.3 shows the simulated variation of the NETD and D^* values with pixel pitch including the required routing in a possible array [39].

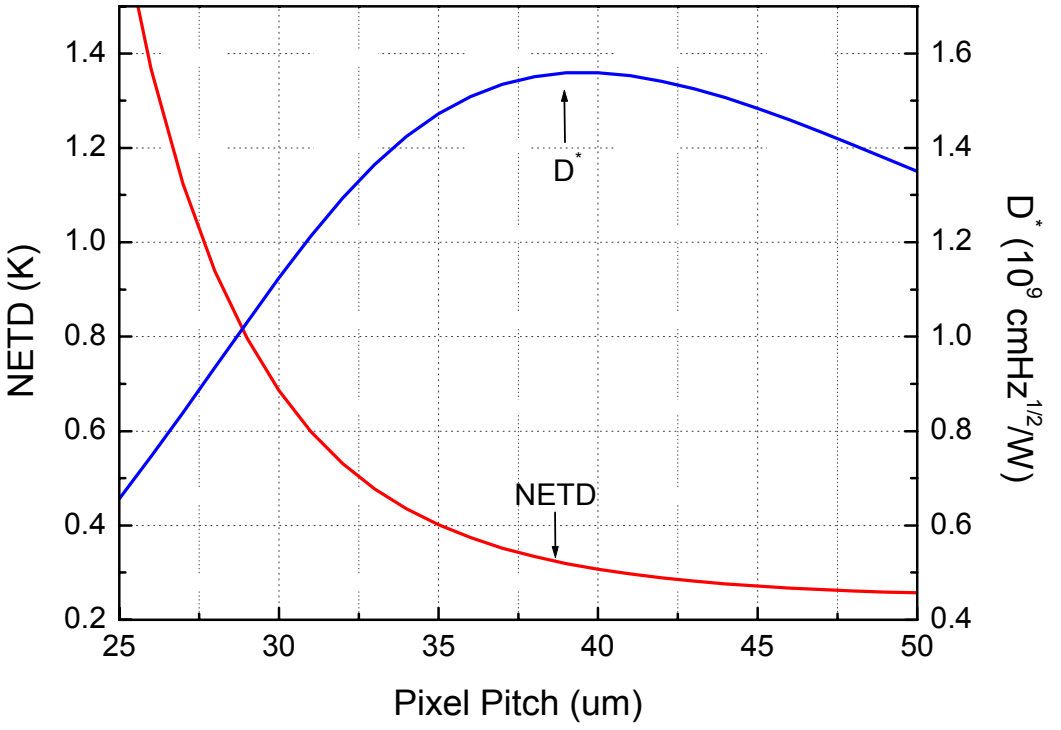


Figure 3.3: Simulated variation of the NETD and D^* values with pixel pitch including the required routing in a possible array [39].

As expected, NETD value decreases monotonically when the pixel size is increased. On the other hand, D^* has peak value of 1.56×10^9 cm√Hz/W at 40 µm pixel pitch where the pixel has a fill factor of 44 %. At this point corresponding NETD value is 307 mK. The reason for lower D^* values at higher pixel sizes is that the excessively increased thermal time constant decreases the responsivity of the pixel, canceling the improvement in the thermal conductance coming from longer support arms [39]. Furthermore, temperature sensitivity of the detector decreases while its electrical noise increases due to the increased interconnect resistance at larger pixels, which cancels the improvement coming from longer interconnect length. At optimum pixel size, the pixel has a thermal conductance of

1.3×10^{-7} W/K with a thermal time constant of 31 ms. At this pixel size, radiation thermal conductance value is as small as 3.9×10^{-9} W/K, which can easily be neglected. The thermal time constant of the pixel is about two times large as compared to the surface micromachined microbolometer detectors, where the detector is deposited as thin film on a thermally suspended bridge, resulting in a relatively small thermal mass at the expense of complicated fabrication process and increased detector cost. When the detector is scanned at 30 fps with a period of 33 ms, the detector temperature rises to the 67 % of the maximum achievable temperature rise, which causes a proportional loss in the responsivity and detectivity values. Finally, it should be mentioned that the pixel bias level is selected as its optimum level, which will be explained later.

Having determined the optimum detector structure, the thermal conductance of the detector is simulated in detail using finite element analysis methods in CoventorWare software [56]. Figure 3.4 shows the thermal simulation result obtained using CoventorWare simulation program.

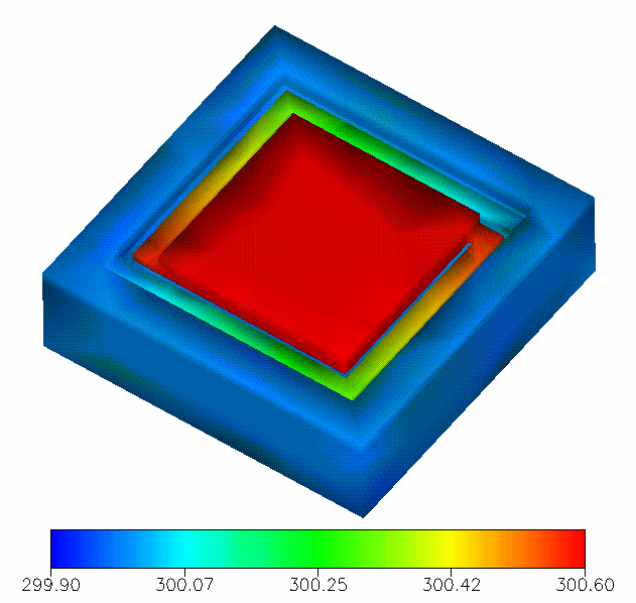


Figure 3.4: Thermal simulation result obtained using CoventorWare simulation program.*

* This simulation has been performed by M. Yusuf Tanrıkulu.

In the simulation given in Figure 3.4, constant power is applied to the suspended structure, while the substrate temperature is kept at a fixed temperature. In this simulation, the detector is assumed to be in vacuum. During the simulation, temperature rise with respect to substrate is simulated. The simulation duration is adjusted so as to allow the detector to reach its steady state value, which depends only on the applied power and the thermal conductance of the detector. The ratio of the applied power to the steady state temperature rise is equal to the thermal conductance of the detector. From the recorded transient response, time constant of the detector is extracted. The thermal conductance and thermal time constant for the diode type pixel are simulated as 1.6×10^{-7} W/K and 27 ms, respectively. The thermal conductance value obtained through finite element simulations are larger than the results obtained with MATLAB simulations. However, it should be mentioned that the actual measured thermal conductance value is close to the results obtained by finite element simulations. The measurement technique of the thermal conductance value will be given in Chapter V.

3.2.2 Temperature Sensitivity

The temperature sensitivity of the pixel voltage is one of the key parameters in determining the performance of the pixel. The p^+-active/n-well diode pixel includes a temperature sensitive built-in diode and resistors coming from polysilicon interconnects, which affect the temperature coefficient of the pixel voltage (dV_{out}/dT). Figure 3.5 shows the model of the p^+-active/n-well diode pixel used in analyzing the temperature coefficient of the pixel voltage when biased at a constant current.

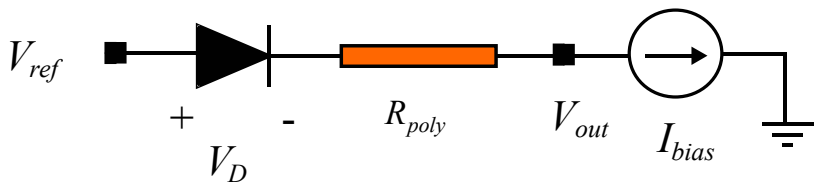


Figure 3.5: Model of the p^+-active/n-well diode pixel used in analyzing the temperature coefficient of the pixel voltage when biased at a constant current.

Temperature coefficient (TC_{out}) of the output voltage of the suspended detector structure is given as

$$TC_{out} = dV_{out}/\mathrm{dT} = -\frac{dV_D}{dT} - \frac{R_{poly} I_{bias} \alpha_{poly}}{2} \tag{3.5}$$

$$dV_D/\mathrm{dT} = -\frac{1.21\mathrm{V} - \mathrm{V_D}}{T} \tag{3.6}$$

$$V_D = \frac{\mathrm{kT}}{\mathrm{q}} \ln\left(\frac{I_{bias}}{I_s} + 1\right) \tag{3.7}$$

where dV_D/dT [28] is the temperature sensitivity of diode forward voltage (V_D), R_{poly} is the resistance of the polysilicon interconnects, I_{bias} is the detector bias current, α_{poly} is the TCR of the polysilicon layer, and k is the Boltzmann constant, T is temperature in Kelvin, q is the electron charge in Coulomb, and I_s is the reverse saturation current of diode. The factor of two in the denominator of the last term in Equation 3.5 accounts for the temperature gradient across the polysilicon interconnects along the support arms. It should be noted that the two terms in Equation 3.5 have canceling effects. However, this effect is not so critical, since the pixel is biased at a low level between 10-20 μA, and the TCR of the polysilicon layer is less than 0.1 %/K. The term 1.21V in Equation 3.6 is a constant with the unit of Volt [28].

Figure 3.6 shows the variation in the magnitude of the detector voltage temperature sensitivity ($|dV_{out}/dT|$) with bias current (I_{bias}). In these simulations updated device parameters based on actual measurements are used. The decrease in the sensitivity at low bias levels is due to the increase of V_D with increasing bias current, and the effect of poly silicon TCR is negligible at low bias levels. As the bias current is increased further, effect of polysilicon TCR is not negligible anymore, and the sensitivity drops further. The sensitivity of pixel output voltage decreases from 2.35 mV/K to 1.65 mV/K when the bias current is increased from 1 μA to 100 μA. Therefore, it is advantageous to use lower bias current values to have both higher sensitivity and lower self-heating.

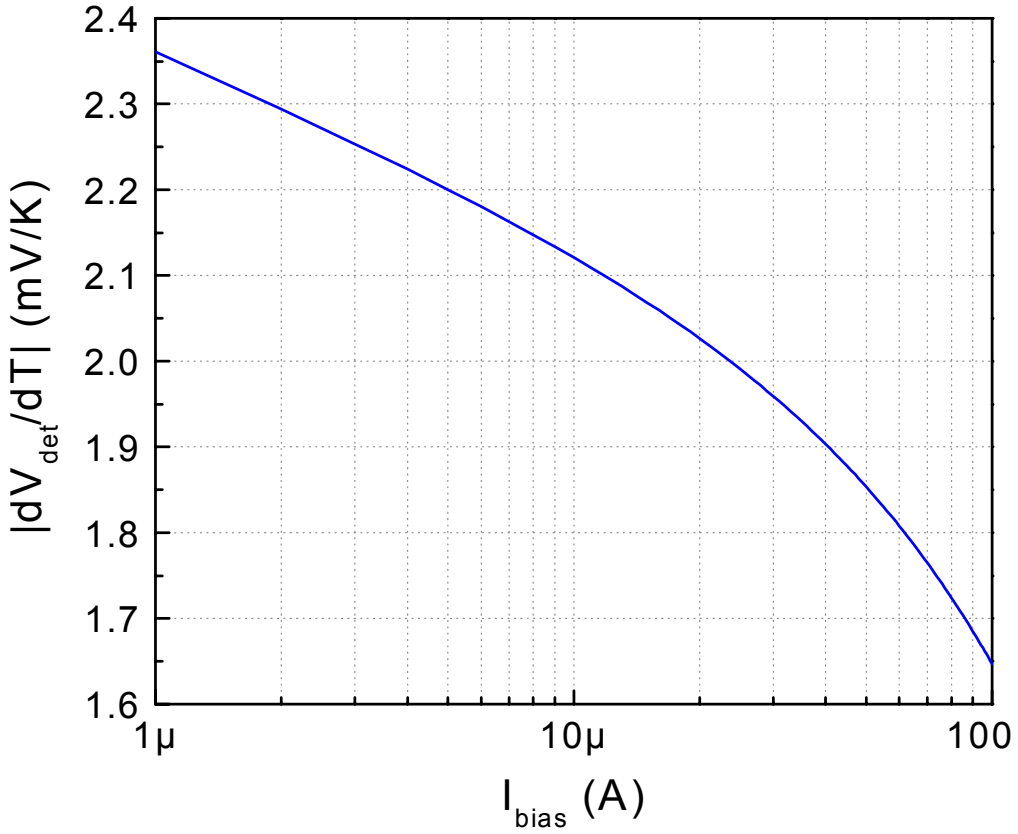


Figure 3.6: Simulated variation in the magnitude of detector voltage temperature sensitivity ($|dV_{det}/dT|$) with pixel bias current (I_{bias}). The magnitude of temperature sensitivity decreases from 2.35 mV/K to 1.65 mV/K when the bias current is increased from 1 µA to 100 µA.

Using a lower bias levels decreases V_D, which in turn results in a higher TC_{out}, hence higher responsivity whose low frequency value is given as

$$\Re_{DC} = \frac{TC_{out}\eta}{G_{th}} \tag{3.8}$$

where TC_{out} is the temperature sensitivity of the pixel output, η is the absorption coefficient, and G_{th} is the thermal conductance value of the detector. Furthermore, reducing the pixel current also helps in keeping the self-heating effect at minimum level, which is the key advantage of diode like pixels as compared to the resistive ones [39, 40].

3.2.3 Electrical Noise

Electrical noise is another important parameter that determines the ultimate performance of the detectors. Figure 3.7 shows the electrical noise model of the pixel used in the performance analysis [39].

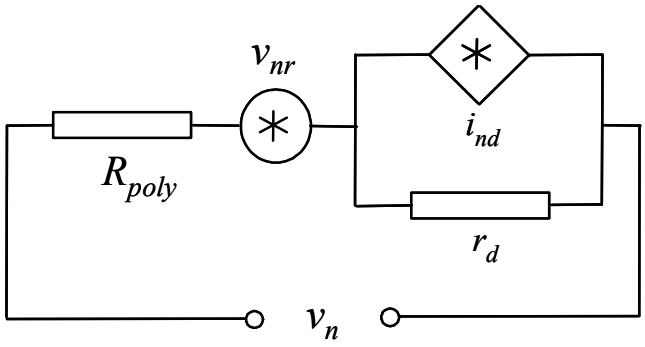


Figure 3.7: Electrical noise model of the pixel used in the performance analysis [39].

The noise voltage of the pixel is composed of two noise sources coming from the interconnect resistor (v_{nr}) and p^+-active/n-well diode (i_{nd}). Since the flicker ($1/f$) noise of the p^+-active/n-well diode is small at low bias levels, it is neglected in the above model, and only shot noise of the diode is considered. In fact, in actual measurements the corner frequency of the 1/f noise of the fabricated detectors is measured to be below 100 Hz at 20 μA bias level, which is sufficiently low for detectors operating with an electrical bandwidth of 4 kHz - 8 kHz. Diode shot noise current (i_{nd}) and the dynamic resistance (r_d) at the given bias current is given as [57]

$$i_{nd} = \sqrt{2qI_{bias}\Delta f} \tag{3.9}$$

$$r_d = \frac{kT}{qI_{bias}} \tag{3.10}$$

where, q is the electron charge, I_{bias} is the detector bias current, Δf is the electrical bandwidth, k is the Boltzmann constant and T is the temperature in Kelvin. Thermal (Johnson) noise (v_{nr}) of the polysilicon support arms is given as [57]

$$v_{nr} = \sqrt{4\mathrm{kTR}_{\mathrm{poly}}\Delta f} \tag{3.11}$$

where, k is the Boltzmann constant, T is the temperature, R_{poly} is the polysilicon interconnect resistance, and Δf is the electrical bandwidth.

The excess $1/f$ noise of the polysilicon interconnect can be neglected due to its low value at low bias levels, which has been verified by the noise measurement results where the $1/f$ corner frequency is measured to be below 100 Hz for detectors having a bandwidth larger than 4 kHz. To calculate the pixel noise voltage, diode noise current is converted to voltage and added to the resistor thermal noise. Total pixel noise voltage (v_n) can be expressed in a similar form used for the thermal noise of a resistor, and v_n is given as [39]

$$v_n = \sqrt{(\mathrm{i}_{\mathrm{nd}} r_d)^2 + v_{nr}^{\ 2}} = \sqrt{4(R_{poly} + \frac{r_d}{2})kT\Delta f} \tag{3.12}$$

where i_{nd} is the shot noise current of the diode, r_d is the dynamic resistance of the diode, v_{nr} is the thermal noise of the interconnect, R_{poly} is the interconnect resistance, k is the Boltzmann constant, T is the temperature, and Δf is the electrical bandwidth. In the above noise expression, the effect of diode shot noise is included in the diode small signal resistance (r_d), which is inversely proportional to I_{bias}. Therefore, to decrease the overall noise voltage, the diode bias current should be increased. However, the pixel voltage temperature sensitivity (dV_{out}/dT) also decreases with increasing bias current, and there is an optimum bias current value for the diode pixel, as explained later in this section.

Figure 3.8 shows the simulated variation of noise components for the p^+-active/n-well diode microbolometer for 4 kHz bandwidth at different bias levels [39]. Noise contribution of the interconnect resistor and p^+-active /n-well diode are also plotted separately. As detector bias current is increased, the dynamic resistance of the diode (r_d) decreases, therefore the voltage noise of the diode ($i_{nd}\, r_d$) decreases even though its shot noise current (i_{nd}) increases. The thermal noise of the resistor is

independent of bias current, and it is constant. Although, at high bias current levels total noise approaches to the thermal noise of the resistor, at low bias levels the diode noise can not be neglected. As bias current increases, contribution of diode noise decreases. For example, at 20 μA bias level, total noise is 0.51 μV, and noise power contributions of the resistor and diode are 85 % and 15 %, respectively. Note that, using a bias level higher than a certain value does not decrease the detector noise much, since total noise approaches to that of the thermal noise of the support arms. However, 1/*f* noise is no more negligible at such high bias levels, and the self-heating effect becomes unacceptably high.

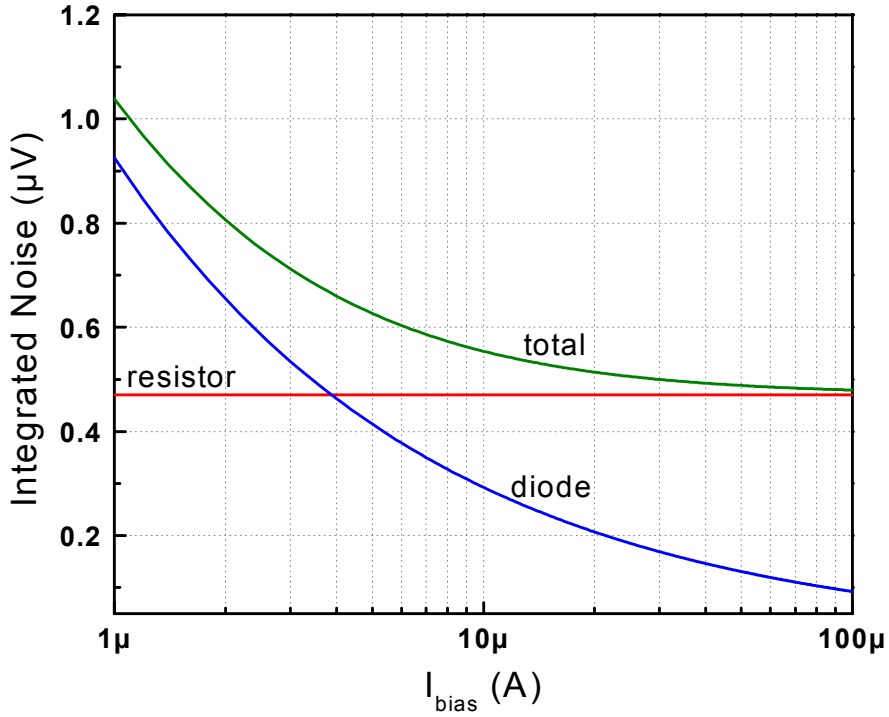


Figure 3.8: Simulated variation of noise components for the p^+-active /n-well diode microbolometer for 4 kHz bandwidth at different bias levels. Noise contribution of the interconnect resistor and p^+-active/n-well diode are also plotted separately [39].

3.2.4 Optimum Pixel Bias

Figure 3.9 shows the simulated variations of the NETD and D^* values of the p^+-active/n-well diode type microbolometer for different bias levels (I_{bias}) for 4 kHz bandwidth. In this simulation the detector parameters are taken from the actual

measurement results of the fabricated 40 µm × 40 µm detectors, which will be given in Chapter IV. At lower bias levels, the diode small signal resistance increases, hence the total pixel noise voltage. Therefore, NETD value increases. On the other hand, at higher bias levels responsivity ($\Re$) decreases due to the decrease in the temperature sensitivity of the pixel voltage. In addition, the self-heating also increases at high bias levels. Therefore, there is an optimum bias level for the detector. Optimum performance is achieved at 20 µA with NETD and D^* values of 470 mK and 9.7×10^8 cm√Hz/W, respectively. At this point, it should be mentioned that, the same optimum bias value was also calculated at the design phase, with only a scaling in the NETD and D^* values as previously given in Figure 3.3.

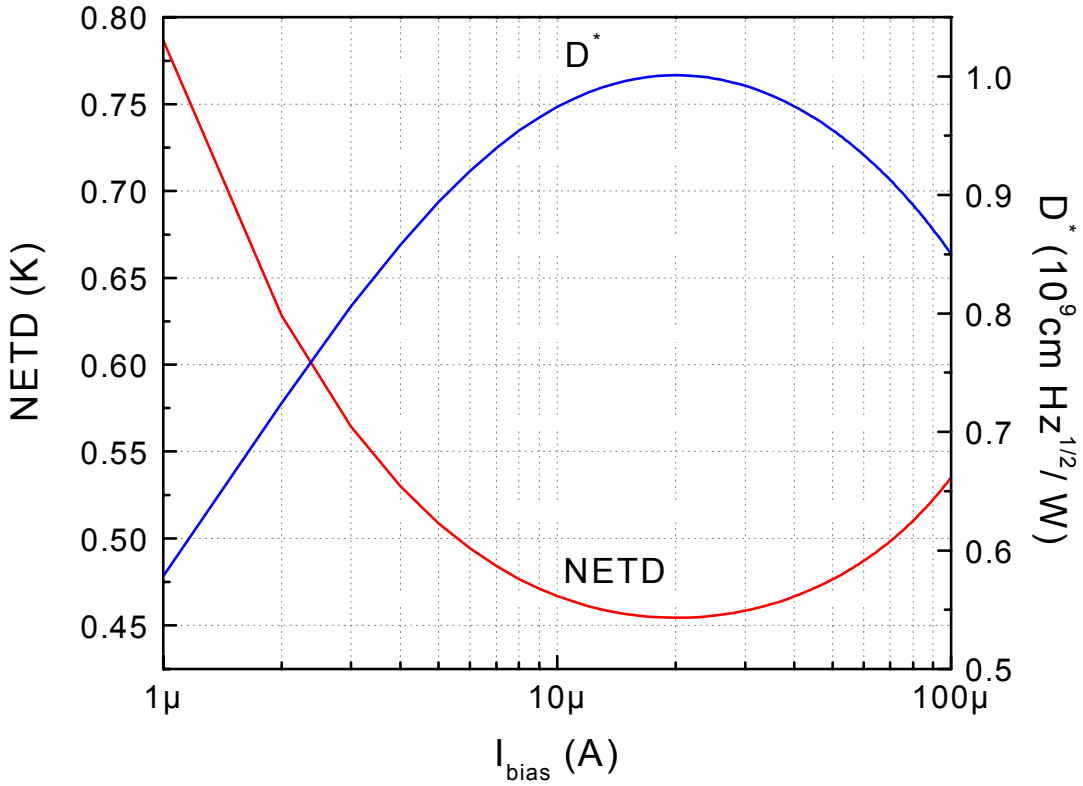


Figure 3.9: Simulated variation of the NETD and D^* values of the p^+-active/n-well diode type microbolometer for different bias levels (I_{bias}) for 4 kHz bandwidth. Optimum performance is achieved at 20 µA with NETD and D^* values of 470 mK and 9.7×10^8 cm√Hz/W, respectively. In this simulation the detector parameters are taken from the actual measurement results of the fabricated 40 µm × 40 µm detectors, which will be given in Chapter IV.

3.3 Self-Heating

Self-heating of the uncooled detectors is an important parameter affecting the operation of the readout circuit. For most of the microbolometer detectors, the detector performance parameters, such as NETD and D^*, improve with the increasing detector bias voltage or current. However, high voltage or current bias levels causes excessive self-heating which may be difficult or impossible to compensate for. Therefore, self-heating and bias levels of the detectors should be considered while comparing the NETD values of different detectors. Figure 3.10 shows the simulated variation of self-heating and NETD of n-well resistive and p^+-active/n-well diode type microbolometers [40]. The NETD value for the resistive microbolometer decreases as the bias level is increased. However, this results in an excessive self-heating problem that may be difficult to compensate for. Whereas, diode type microbolometer can provide same NETD values at much lower bias levels with much less self heating. At the optimum bias point of 20 µA, self-heating for the p^+/n-well diode type microbolometer is only 0.27 K, which is about 10 times smaller as compared to that of the resistive microbolometer.

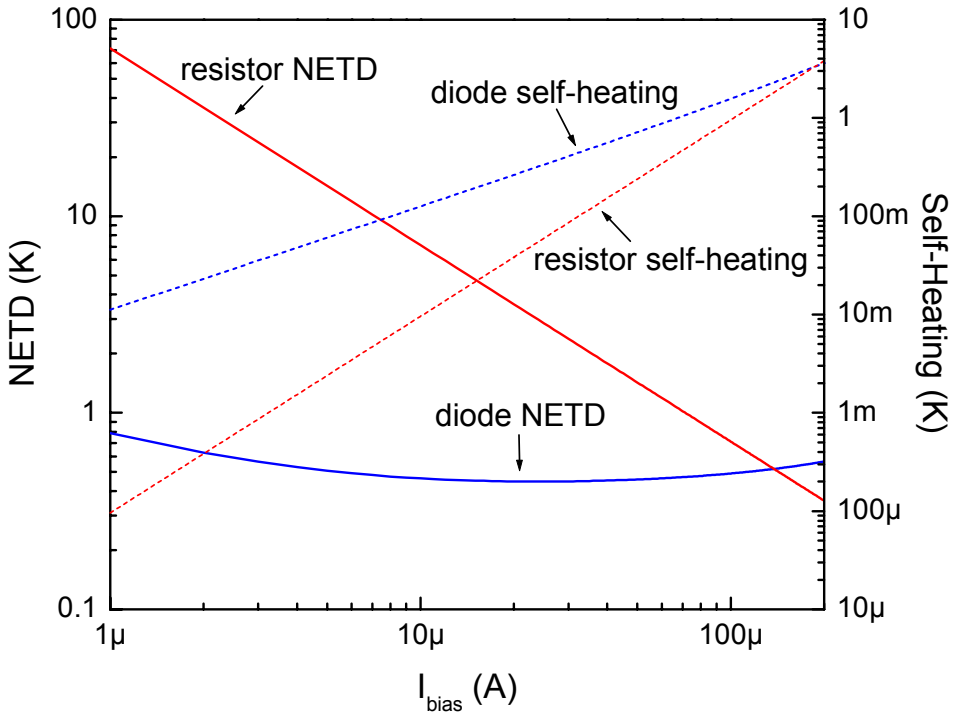


Figure 3.10: Simulated variation of self-heating and NETD of n-well resistive and p^+-active/n-well diode type microbolometers [40].

3.4 Conclusions

This chapter gives the details on the design and optimization of a new small size n-well microbolometer detector based on a suspended and thermally isolated p^+-active/n-well diodes fabricated in a standard 0.35 μm CMOS process. A new post-processing method is proposed that do not require any critical lithography or complicated deposition steps. The required etch openings are created in a simple dry etch process using metal layers in the process as protection mask. After the necessary openings are created on the surface to reach the silicon substrate, the silicon underneath the pixel is removed in an anisotropic silicon etchant, while the electrochemical etch-stop process is used to prevent the etching of the n-well layer.

This approach has a number of advantages. First of all, it does not require any critical lithography step after the CMOS process, reducing the cost of the detectors almost equal to the CMOS chip cost. In addition, the gaps between the arms can be reduced as the CMOS technology allows, making it possible to reduce the pixel size while increasing the fill factor suitable for large format arrays with 64 × 64 or 128 × 128 pixel resolutions. Since the detectors are implemented using diodes in single crystal silicon, their 1/*f* noise contribution is negligibly small especially at low bias levels. At optimum bias level, noise contribution of the diode is very small as compared to the noise coming from polysilicon interconnect resistors. At low bias levels, 1/*f* noise contribution of the polysilicon interconnects are also low, therefore, total detector noise approaches to the thermal noise of the interconnect resistors.

MATLAB simulation performed at the design stage showed that the optimum performance is achieved with a pixel size of 40 μm × 40 μm and a corresponding fill factor of 44 %. This detector structure can theoretically achieve NETD and D^* values of about 300 mK and 1.56×10^9 $cmHz^{1/2}/W$, respectively, when biased at the optimum level of 20 μA. In these simulations, absorption coefficient is taken as 0.45, which is updated according to the measurement results given in Chapter IV. The thermal conductance and time constant of the optimized detector are calculated in MATLAB as 1.3×10^{-7} W/K and 31 ms, respectively. After the pixel structure is

determined, the thermal conductance value is simulated using finite element analysis in CoventorWare software, and a slightly larger value of 1.6×10^{-7} W/K is obtained, which is close to the measured results of 1.55×10^{-7} W/K, which will be presented in detail in Chapter IV. Based on the measured detector parameters, the new n-well diode type microbolometer achieves a detectivity of 9.7×10^{8} cmHz$^{1/2}$/W at 20 μA bias level. For 4 kHz electrical bandwidth the detector is expected to have an NETD value of 470 mK for an f/1 optics. Considering its simple fabrication method and its moderate performance, this new uncooled infrared detector together with its simple post-processing method is very suitable for the fabrication of low-cost large format uncooled FPAs required in many commercial infrared imaging applications.

CHAPTER IV

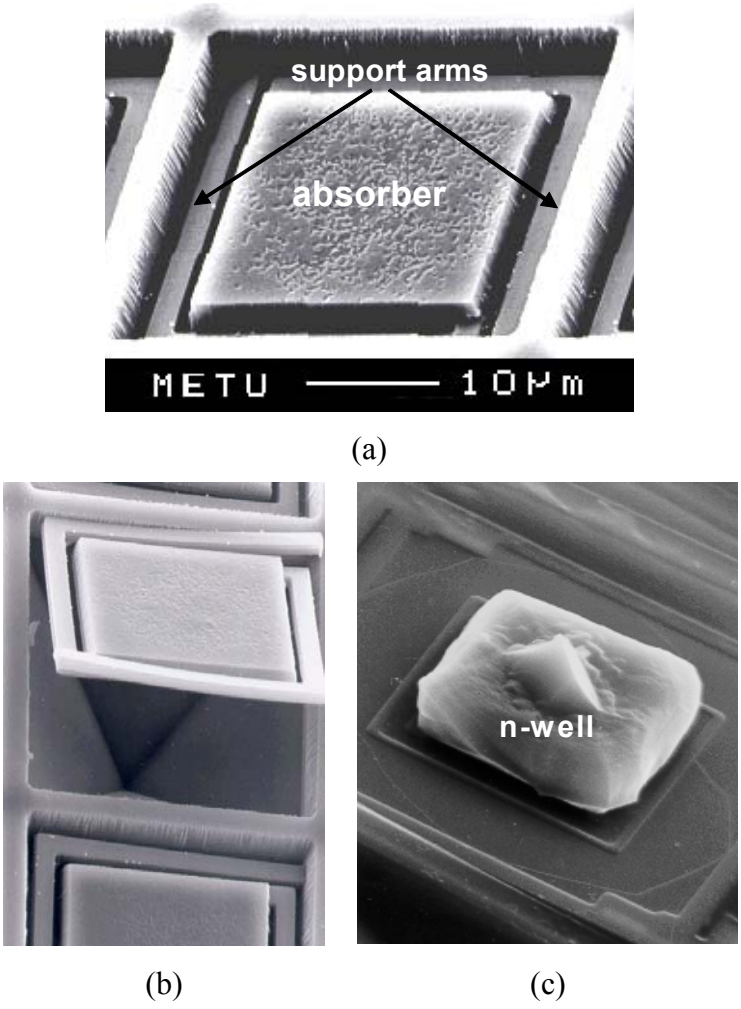
4 TEST RESULTS OF THE SINGLE PIXEL DETECTORS

This chapter gives the details of the electrical and optical tests performed to determine the performance of the single pixel p^+-active/n-well diode type microbolometer detector. These tests include the measurements of the temperature sensitivity measurement, I-V characteristics, infrared responsivity, spectral absorption, and electrical noise of the detector.

Section 4.1 gives the post-processing results of the single pixel detectors, which has been developed within the framework of another thesis [51]. Section 4.2 gives the measurement setup and test results of the temperature sensitivity tests. Section 4.3 gives the I-V and V-I characteristics of the suspended detector, and it presents a method to extract the thermal conductance value of the detector from the measured device characteristics. Section 4.4 presents the responsivity measurement result, and Section 4.5 gives test results of the spectral absorption measurement. Section 4.6 explains in detail the noise measurement setup with the emphasis on the low-noise preamplifiers used for the detector noise measurement, and measured noise spectral densities are presented. Finally, Section 4.7 summarizes the electrical and optical tests to determine the performance of the p^+-active/n-well diode type microbolometer detector.

4.1 Post-CMOS Fabrication

Figure 4.1 (a) shows the SEM photograph of the post-processed single pixel p^+-active/n-well diode microbolometer using a dry-etch step followed by an electro-chemical etch stop in TMAH solution. The pixel measures 40 μm × 40 μm with a fill-factor of 44 % [39]. Figure 4.1 (b) shows the SEM photograph of the etched v-groove underneath a single pixel p^+-active/n-well diode microbolometer broken on purpose, and Figure 4.1 (c) shows the SEM photograph of the suspended n-well structure obtained by removing the pixel from the substrate using a sticky-tape [51].



(a)

(b) (c)

Figure 4.1: SEM photographs of the post-processed single pixel p^+-active/n-well diode microbolometer using a dry-etch step followed by an electro-chemical etch stop in TMAH solution: (a) top view measuring 40 μm × 40 μm with a fill-factor of 44 % [43], (b) etched v-groove underneath the pixel, and (c) suspended n-well structure obtained by removing the pixel from the substrate using a sticky-tape [51].

4.2 Temperature Sensitivity Measurement

Figure 4.2 shows the temperature sensitivity measurement setup using a thermo-electric cooler (TEC) together with a heat-sink and a temperature sensor (AD590). Temperature sensitivity of the detectors are measured by heating the chip substrate using the TEC whose cold plate is mounted on top of a metal heat sink in order to avoid damage of the TEC. First, the detector is placed on an alumina substrate which has gold plated metal pads on it. Wires are soldered on these pads, and then detector pads are wirebonded on the extensions of these metal pads on the alumina substrate. The alumina substrate is placed on the hot side of the TEC, and temperature difference between the hot and cold plates of the TEC is controlled by changing the applied TEC voltage. Thermal compound is deposited between the surfaces placed on the hot plate to decrease the thermal resistance and to minimize temperature difference between the surfaces. The temperature of the hot plate is measured using an absolute temperature sensor (AD590) whose output current in μA corresponds to absolute temperature in Kelvin. A flat ceramic sensors package (AD590-KF) whose bottom plate is plated with gold is used so that it can properly measure the surface temperatures.

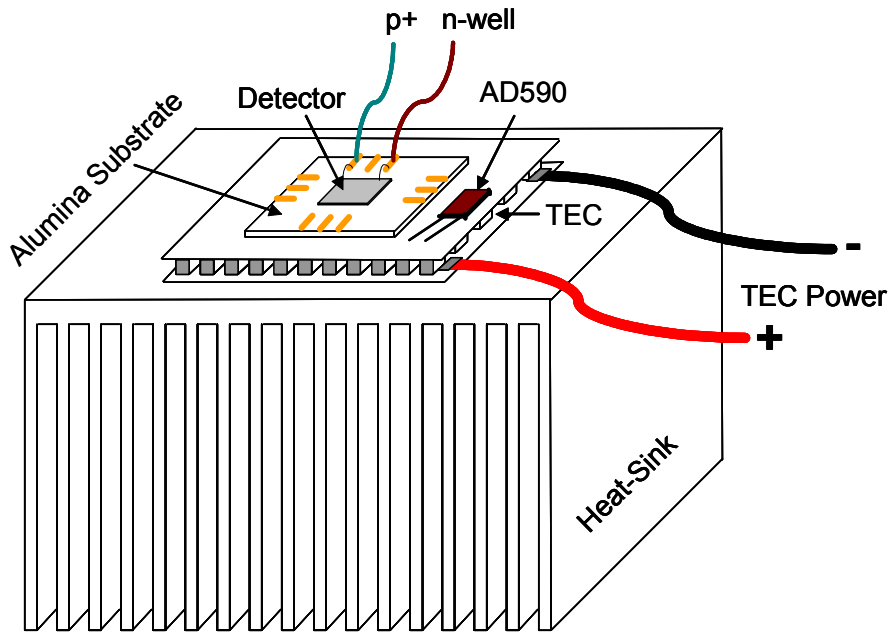


Figure 4.2: Temperature sensitivity measurement setup using a thermo-electric cooler (TEC) together with a heat-sink and a temperature sensor (AD590).

Figure 4.2 shows the measured variation of the detector voltage with temperature at different detector bias levels. The detector temperature sensitivity is measured as -2 mV/K at 20 µA [39]. As expected, the temperature sensitivity decreases (in magnitude) with increased bias levels. At 100 µA detector bias level the temperature sensitivity is measured as -1.7 mV/K. These results are in accordance with the simulation results presented in Chapter III. In fact, the simulated temperature sensitivity values are -2.03 mV/K and -1.65 mV/K at 20 µA and 100 µA bias levels, respectively. At this point it should be noted that the tests are performed using the unsuspended dies that come from the CMOS fabrication. The reason is that, it is not easy to control the detector temperature by changing the substrate temperature since the sensitive suspended part will be in thermal interaction with the surrounding air.

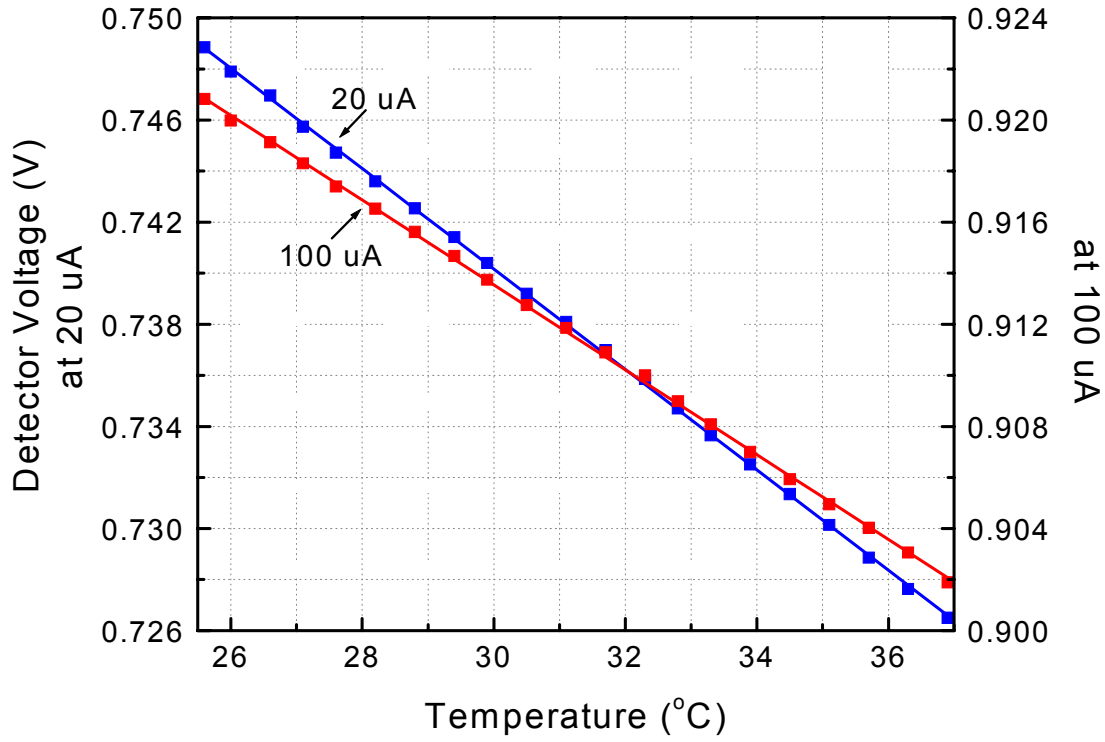


Figure 4.3: Measured variation of detector voltage with temperature at different detector bias levels. The detector temperature sensitivity is measured as -2 mV/K at 20 µA, and sensitivity decreases in magnitude to -1.7 mV/K at 100 µA, which is in accordance with the simulation results given in Chapter III [39].

4.3 I-V Measurements

I-V measurements are performed to determine the detector voltage at different detector bias current levels. Figure 4.3 shows the measured I-V characteristics of the suspended diode type detector operated at room temperature (298 K) and at atmospheric pressure (1 atm) [42]. For the sake of simplicity, the data points are not shown, since the bias voltage is applied in small steps of 10 mV. Since the detector does not operate in vacuum, not much self-heating is observed, and therefore, the I-V characteristics of the detector is the same as what is expected for a diode with a series resistor. The measured I-V characteristics is mapped to the device current equation given as [58]

$$I_{\text{det}} = I_s(\text{e}^{\frac{q(V_{\text{det}} - I_{\text{det}}R)}{nkT}} - 1) \tag{4.1}$$

where, I_{det} is the detector current, I_s is the reverse saturation current of the diode, R is the series interconnect resistance, V_{det} is the detector voltage, n is the diode ideality factor, k is the Boltzmann constant, and T is the temperature in Kelvin.

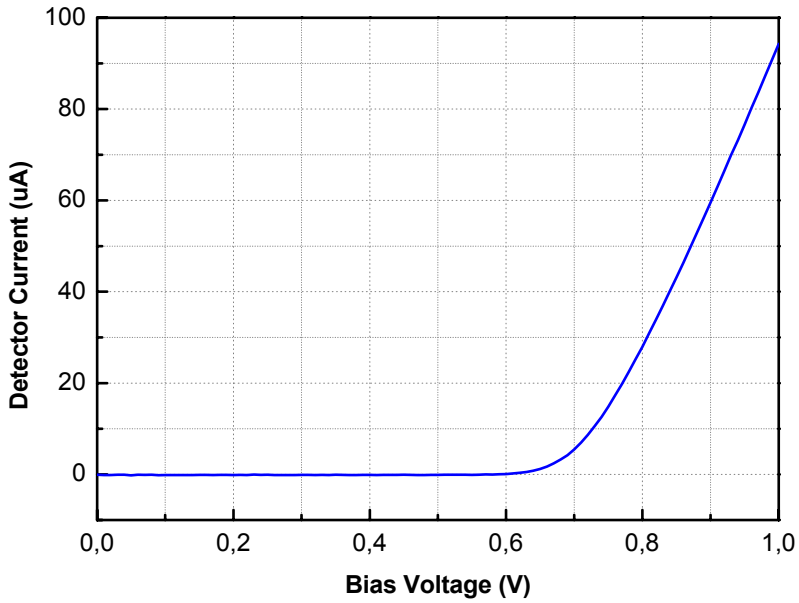


Figure 4.4: Measured I-V characteristics of the suspended diode type detector operated at room temperature (298 K) and under room pressure level (1 atm). For the sake of simplicity, the data points are not shown, since the bias voltage is applied in small steps of 10 mV [42].

From the measurement result, in the low bias region (I_{det} < 50 μA), I_s, n, and R are extracted as 1.02 fA, 1.08, and 2.63 kΩ, respectively. At high bias level, the measured diode current deviates from the Equation 4.1 due the high-level injection effects [58]. Another reason for this deviation is the fact that applied large bias increases the diode temperature even though the detector is not in vacuum. Therefore, large bias portion is omitted during curve fitting operation. As expected, at high bias levels, the slope of the I-V curve becomes almost constant due to the fact that diode voltage changes very little due to its exponential I-V characteristics. The slope of the curve in this region can be used to extract the actual interconnect resistance, since the dynamic resistance of the diode is very small in this region. In this region, the interconnect resistance is extracted as 3.05 kΩ, which is close to the designed value of 3.2 kΩ. The difference in the extracted R values for both low level and high level bias is due to the difficulties in calculating the voltage drop across the series resistor in the low bias level; therefore, R value found at high bias level is more reliable.

Figure 4.5 shows the measured I-V characteristic of the suspended diode type detector at 50 mTorr vacuum level biased by a variable current source. When the suspended detector operates under vacuum condition, it heats up easily with the applied value of the DC bias, causing a bending in the V-I characteristics [42]. If the detector is biased by a constant voltage source, the detector current will increase with the increase in the detector temperature, due to the decreasing diode forward voltage drop related to its negative temperature coefficient (TC) value. Since the applied bias voltage is constant, increase in the detector current will increase the applied power, and eventually the device will burn-out due to the thermal runaway. However, in the case of constant current bias, the detector power decreases as the device is heated up allowing a stable operation.

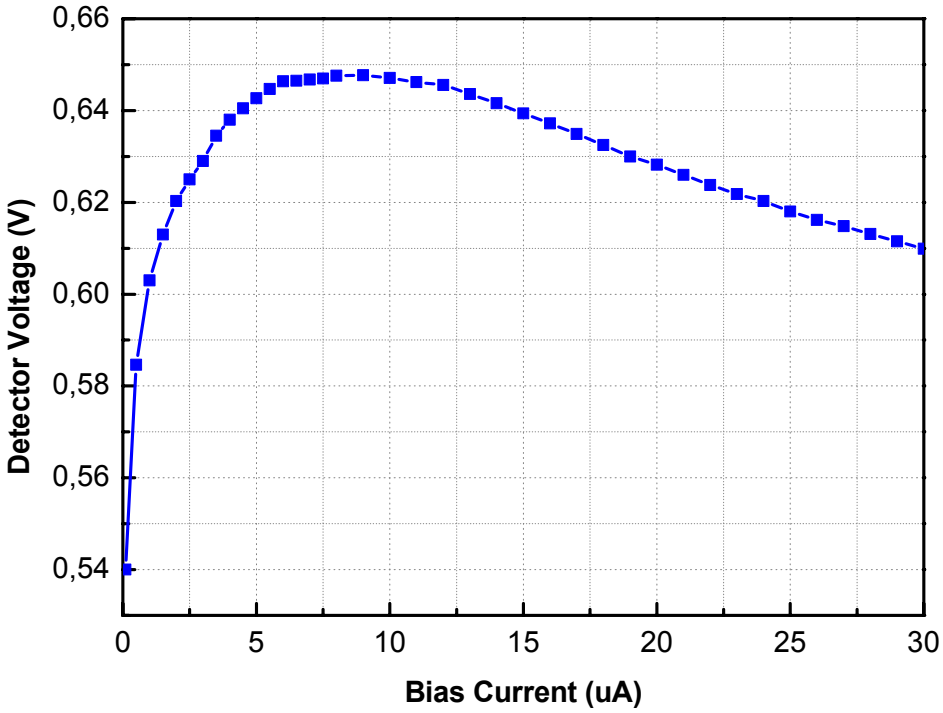


Figure 4.5: Measured I-V characteristic of the suspended p^+/n-well active diode type microbolometer detector at 50 mTorr vacuum level biased by a variable current source [42].

At low bias levels, the self-heating effect is negligible due to the low value of the applied electrical power. Therefore, the detector voltage increases with the increasing bias current related to the interconnect resistance along the support arms and dynamic resistance of the diode. However, when the bias is increased further, the slope of the voltage curve decreases. After a certain bias level, the slope turns out to be negative, and the detector voltage decreases with the increasing bias current due to the excessive self-heating. Self-heating makes the slope of the V-I curve negative forcing the detector voltage to decrease related with its negative TC value despite an expected increase in detector voltage due to the series interconnect resistance and the dynamic resistance of the diode as in the case of low-level bias. Neglecting the power dissipation along the interconnects, the slope of the V-I curve is given as [42]

$$\frac{dV}{dI} = \frac{R_{connect} + r_d + TC_{eff} V / G_{th}}{1 - TC_{eff} I / G_{th}} \tag{4.2}$$

$$TC_{eff} = \frac{IR_{connect}\alpha_{connect}}{2} - n\frac{1.21 - V_d / n}{T} \tag{4.3}$$

where, $R_{connect}$ is the interconnect resistance, r_d is the dynamic resistance of the diode, TC_{eff} is the effective temperature coefficient of the detector voltage, V is the detector voltage, n is the diode ideality factor extracted as 1.08 for the suspended n-well diodes, G_{th} is thermal conductance, I is the detector bias current, $\alpha_{connect}$ is the temperature coefficient of resistance of the interconnect material (0.09 %/K), V_d is the diode voltage, and T is the detector temperature.

By calculating the slope of the measured V-I curve and TC_{eff} at each bias point, G_{th} of the detector is extracted as 1.55×10^{-7} W/K. This G_{th} value is larger than the expected value of 1.2×10^{-7} W/K according to simulations performed using the CoventorWare program [56]. One possible reason for the increase in the G_{th} value is the fact that there remains a thin residual metal layer on the interconnects of the detector after post processing, and this problem can be solved by extending the etching periods during post processing steps. In fact, the simulated thermal time constant value is close to measured value of 36 ms, which suggests that there is some extra material left on the pixel, resulting in the same thermal time constant value despite the increase in the thermal conductance value. With process optimization, it is possible to decrease the G_{th} down to its simulated value without much increase in the thermal time constant value [41].

4.4 Infrared Responsivity Measurement

Figure 4.6 shows the test setup used for the infrared responsivity measurement. The setup is constructed using a light source, a light chopper, an infrared bandpass filter, reference detector or microbolometer detector, and a lock-in amplifier.

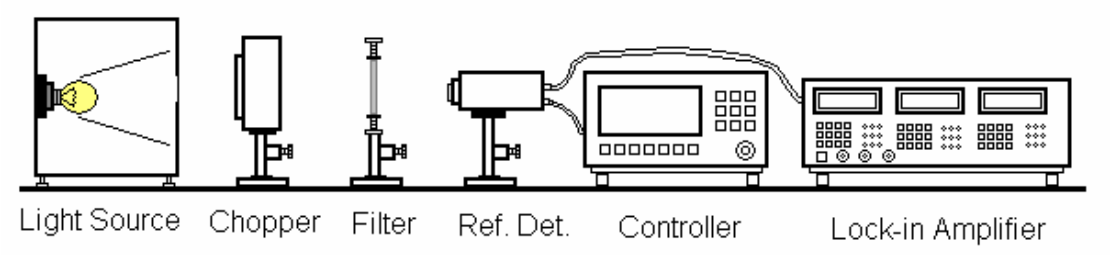


Figure 4.6: Test setup used for the infrared responsivity measurement.

The light source is constructed using an incandescent bulb whose radiation is modulated using a light chopper. Visible portion of the incoming radiation is filtered out using a Germanium (Ge) infrared bandpass filter whose transmission is given in the next section. A small piece of Ge filter is also used as the IR window in the vacuum chamber where the n-well microbolometer is placed during the tests. The incident power to the detector at a fixed location is measured by a pyro-electric reference detector with its special readout unit which also controls the chopper frequency. Then, the reference detector is replaced with the p^+-active /n-well diode type microbolometer detector which is put in a vacuum chamber and placed at the same position as the reference detector. The rms value of the modulated detector voltage is measured using a lock-in amplifier.

In the calculation of responsivity, normalization is performed by dividing the measured detector voltage to the measured power level read out by the reference detector. In this calculation, effect of the chopper on the signal shape should be considered. For example, the readout unit of the reference detector is adjusted such that it gives the DC level of the unmodulated infrared radiation. However, a standard lock-in amplifier gives the rms value of the incoming signal at the given chopping frequency. Therefore, a conversion factor is required to convert the DC radiation level displayed by the readout unit of the reference detector to the actual rms level, which can be found using the specifications of the light chopper, which is 0.4 for the particular chopper used in the measurements. Figure 4.7 shows the measured responsivity of the p^+-active/n-well diode type microbolometer detector with respect to infrared modulation frequency from 8.5 Hz to 85 Hz at 80 mTorr vacuum level. In this test the detector is biased continuously by a constant current source to avoid

thermal run-away. The measurement data fits into a single-pole frequency response, and the DC responsivity and the thermal time constant values of the detector are extracted as 4970 V/W and 36 ms, respectively [40, 41].

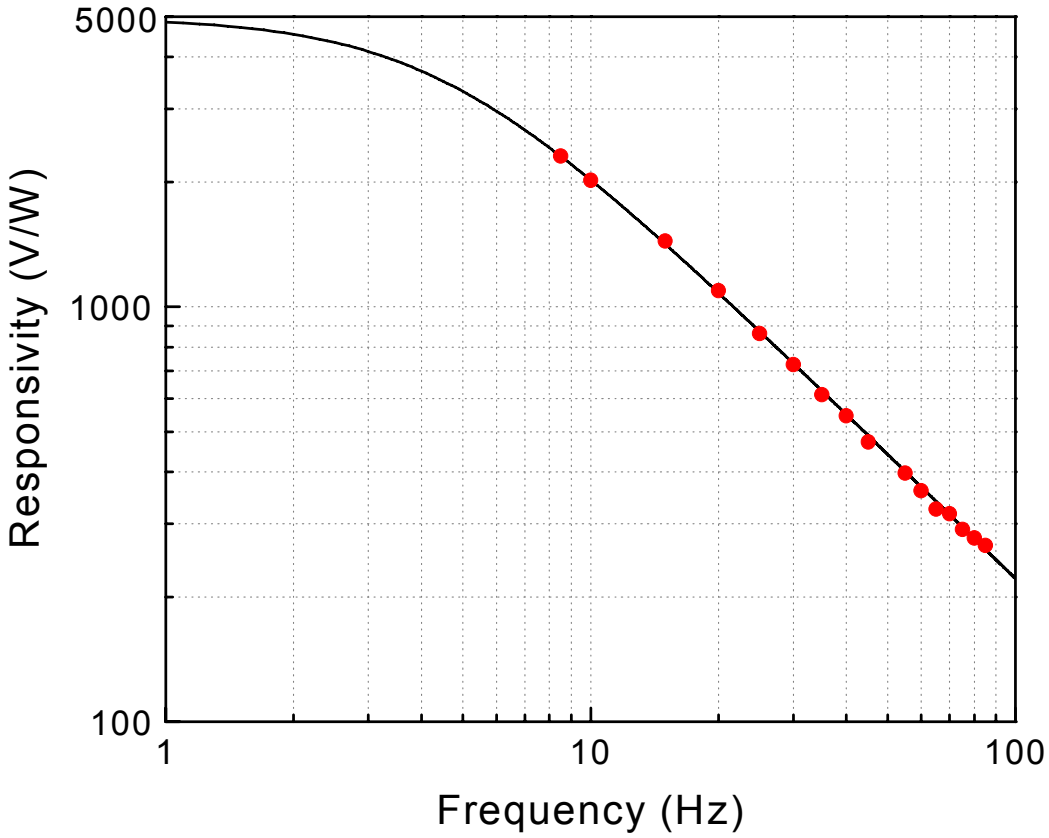


Figure 4.7: Measured responsivity of the p^+/n-well active diode type microbolometer detector with respect to infrared modulation frequency from 8.5 Hz to 85 Hz at 80 mTorr vacuum level. The measurement data fits into a single-pole frequency response, and the DC responsivity and the thermal time constant values of the detector are extracted as 4970 V/W and 36 ms, respectively [40, 41].

Due to the negative temperature coefficient, self-heating has a negative effect on the DC responsivity of the detector. This is called electrothermal effect, which is observed especially for the continuously biased detectors [14]. When the infrared radiation heats up the detector, there is a decrease in the detector voltage related with its negative TC value. Since it is biased by a constant current source, applied electrical power also decreases, which in turn decreases the expected change in the detector temperature due to the reduced self-heating. The DC responsivity of the continuously biased diode type microbolometers ($\Re_{DC\_cont}$) is given as [42]

$$\Re_{DC\_cont} = \eta TC_{eff} / G_{th\_eff} \tag{4.4}$$

$$\Re_{DC\_cont} = \frac{\eta TC_{eff}}{G_{th}(1 - TC_{eff} I / G_{th})} \cong \frac{\eta TC_{eff}}{G_{th}(1 - TC_{eff} \Delta T_{self-heating} / V)} \tag{4.5}$$

where, η is the absorption coefficient, TC_{eff} is the effective temperature coefficient of the detector, G_{th_eff} is the effective thermal conductance value that accounts for the electrothermal feedback effect, I is DC bias current, V is the detector voltage, and $\Delta T_{self\_heating}$ the temperature rise due to self-heating. For continuous bias case, G_{th_eff} of the detector becomes as large as 1.8×10^{-7} W/K, and using this G_{th_eff} value and measured DC responsivity of the detector, absorption coefficient (η) is extracted as 0.45. It should be noted that in the pulsed bias case $\Delta T_{self\_heating}$ is negligible; therefore, an improvement in thermal conductance value is expected for the array detectors operating in the pulsed bias mode. In the pulsed bias mode, self-heating will be negligible, and therefore, G_{th_eff} of the detector will decrease from 1.8×10^{-7} W/K to its measured physical value of 1.55×10^{-7} W/K, providing an improvement of about 16 % in the overall DC responsivity.

4.5 Spectral Absorption Measurement

Spectral absorption of the p^+-active/n-well diode microbolometer detector is measured at a fixed modulation frequency by repeating the responsivity measurement at discrete wavelengths of the infrared radiation. Figure 4.8 shows the spectral absorption test setup including a black body, a light chopper, a monochromator, a Zinc Selenide (ZnSe) lens for focusing, a Germanium (Ge) optical filter, and reference detector or p^+-active/n-well diode type microbolometer detector for testing, and the control unit of the reference detector or a lock-in amplifier.

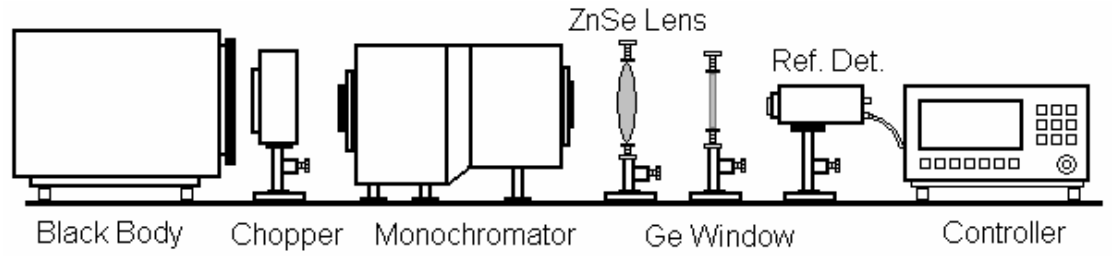


Figure 4.8: The spectral absorption test setup including a black body, a light chopper, a monochromator, a Zinc Selenide (ZnSe) lens for focusing, a Germanium (Ge) optical filter, and reference detector or p^+-active/n-well diode type microbolometer detector for testing, and the control unit of the reference detector or a lock-in amplifier.

In the spectral absorption test spectral content of the emitted radiation is limited to a very narrow band using a monochromator; therefore the power level is reduced considerably as compared to the wide band responsivity test explained previously. To keep the detector voltage above the noise floor of the measurement system, incoming radiation is increased by setting the blackbody temperature to higher temperatures such as 1000 K. The power level of the band limited infrared radiation is measured by the reference detector at each wavelength setting of the monochromator. Then, the detector output voltage is measured using the same procedure as explained for the wide band responsivity measurement. Then, measured responsivity values at different wavelengths are normalized with respect to the maximum value. Figure 4.9 shows the measured optical transmission of the Ge optical filter and relative spectral absorption of the p^+-active/n-well diode type microbolometer detector recorded in the 5 μm - 14.5 μm spectral window.

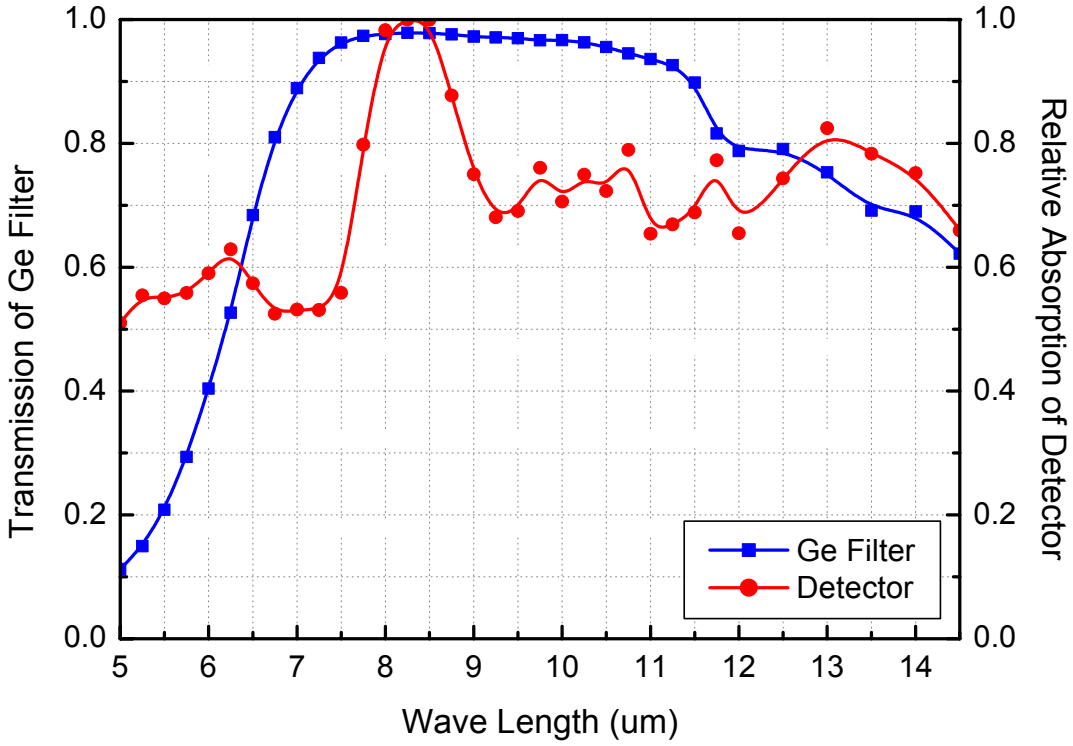
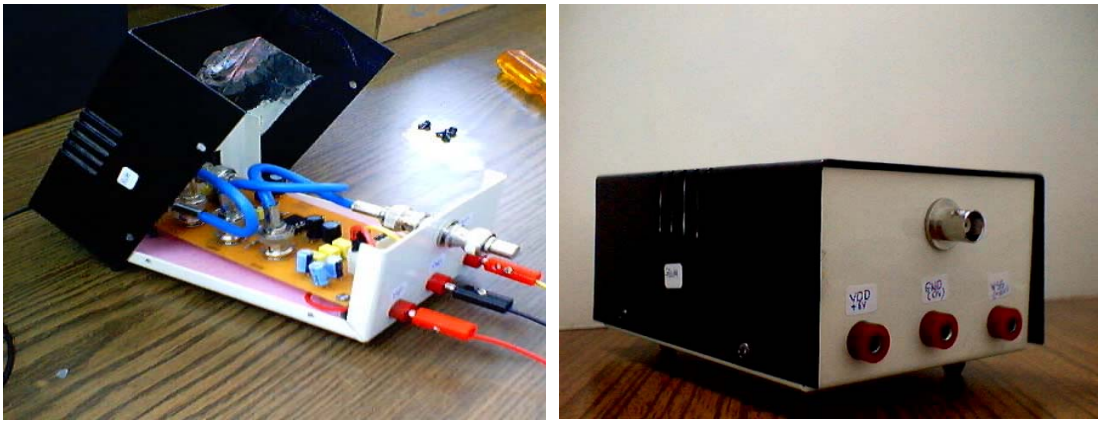


Figure 4.9: Measured optical transmission of the Ge optical filter and relative spectral absorption of the p^+-active/n-well diode type microbolometer detector recorded in the 5 µm - 14.5 µm spectral window.

The optical transmission of the Ge filter is above 90 % in the 8-12 µm bandwidth. In this region, the relative absorption coefficient of the n-well microbolometer is better than 65 % having the maximum absorption at the wavelength of 8.5 µm. At this point it should also be noted that outside the 7-12 µm bandwidth, the incoming IR radiation power is attenuated considerably by the Ge optical window of the vacuum chamber, which makes the recorded data unreliable outside the specified range. The electro-optical test results presented up to this point verify that the p^+-active/n-well diode type microbolometer detector can de used for the uncooled infrared imaging applications in the commonly used 8-12 µm spectral window. The next section presents the noise measurement results together with the test setups which include custom made low-noise preamplifiers. Gain and noise characteristics of the designed preamplifiers are given together with the measured noise spectrum of the p^+-active/n-well diode type microbolometer detector.

4.6 Noise Measurement

Noise of the detector is measured using a custom made low-noise preamplifier circuit implemented with discrete components and commercially available operational amplifier integrated circuits. Figure 4.10 (a) and (b) show the prepared preamplifier circuit board placed in a metal box to minimize possible electromagnetic interference.



(a) (b)

Figure 4.10: Prepared preamplifier circuit board (a) placed in a metal box (b) to minimize any possible electromagnetic interference.

Figure 4.11 shows the schematic of the implemented low-noise preamplifier circuit together with the detector bias circuit designed to be used both for the resistive and diode type n-well microbolometers. The amplifier is composed of a buffer stage, and two gain stages, where the cascaded stages are AC coupled to avoid any saturation due to the large DC value of the detector voltage. To minimize the noise level of the amplifier, bipolar opamps (NE5532P) with low-input noise is selected. Furthermore, small resistance values are used to limit the thermal noise coming from these resistors.

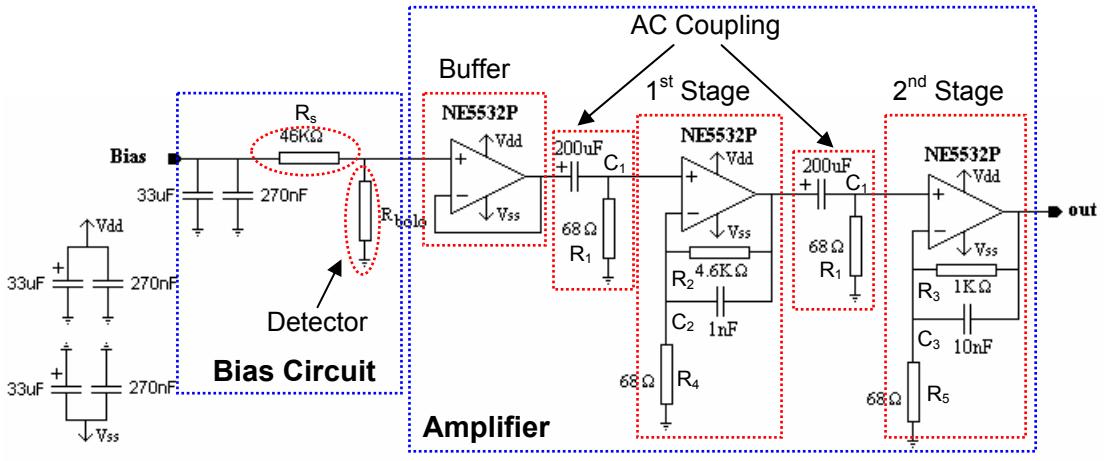


Figure 4.11: Schematic of the implemented low-noise preamplifier circuit together with the detector bias circuit designed to be used both for the resistive and diode type n-well microbolometers.

AC coupling of the cascaded amplifier stages are achieved using first order high pass passive filters implemented with discrete capacitors (C_1) and resistors (R_1) with a zero at DC and pole at 11.7 Hz. The gain of the first and second stages are designed as 67.6 V/V and 14.7 V/V, respectively, which gives an overall gain of 995 V/V very close to 60 dB. The gain of these stages are limited at high frequencies by the addition of bypass capacitors (C_2 and C_3) across the feedback resistances (R_2 and R_3), which introduce poles at 34.6 kHz and 15.9 kHz. The frequency response of the designed amplifier is given as

$$A(\omega) = \left(\frac{j\omega R_1 C_1}{1 + j\omega R_1 C_1} \right)^2 \left(1 + \frac{R_2}{R_4} \frac{1}{1 + j\omega R_2 C_2} \right) \left(1 + \frac{R_3}{R_5} \frac{1}{1 + j\omega R_3 C_3} \right) \tag{4.6}$$

where, the first term in the parentheses is the transfer function of the AC coupling circuits which is squared due to the two such cascaded blocks in the circuit, and the second and third terms in the parentheses are the transfer functions for the first and second gain stages.

The bias circuit is integrated on the same circuit board placed in the metal box, which minimized electromagnetic interference at the sensitive detector bias input during noise measurements especially when the detector is also placed in the same box for electromagnetic shielding purposes. The resistance of the diode type

microbolometers is an order of magnitude smaller than the source resistance (R_s) used in the bias circuit designed to be used with a 1.5 V battery to achieve low noise operation. The bias circuit generates a bias current of about 17 μA, which is close to the optimum bias point of 20 μA for the p^+-active/n-well diode microbolometer detector.

Figure 4.12 shows the measured frequency response of the designed preamplifier obtained using HP 4395A. The amplifier has 3 dB points at 10 Hz and 13.7 kHz with a mid-band gain of 60 dB. To measure the frequency response of the preamplifier, the detector is disconnected from the circuit, and a sine wave is applied to the detector input of the amplifier. The frequency of the sine wave is swept from 10 Hz to 1 MHz, and preamplifier output voltage is recorded together with the applied input voltage. The ratio of amplitudes of these two signals gives the magnitude of the frequency response of the implemented preamplifier.

Figure 4.13 shows the measured noise spectral density of the preamplifier output when the detector is replaced with a 50 Ω resistor. This test is performed using HP 4395A in the noise spectrum measurement mode. Detector bias is applied using a 1.5 V battery. The measured spectrum has both 1/f and thermal noise components. The decay in 1/f noise component with increasing frequency is an expected result. The gradual decrease in the thermal noise floor with increasing frequency is due to the decrease in the amplifier gain at higher frequencies.

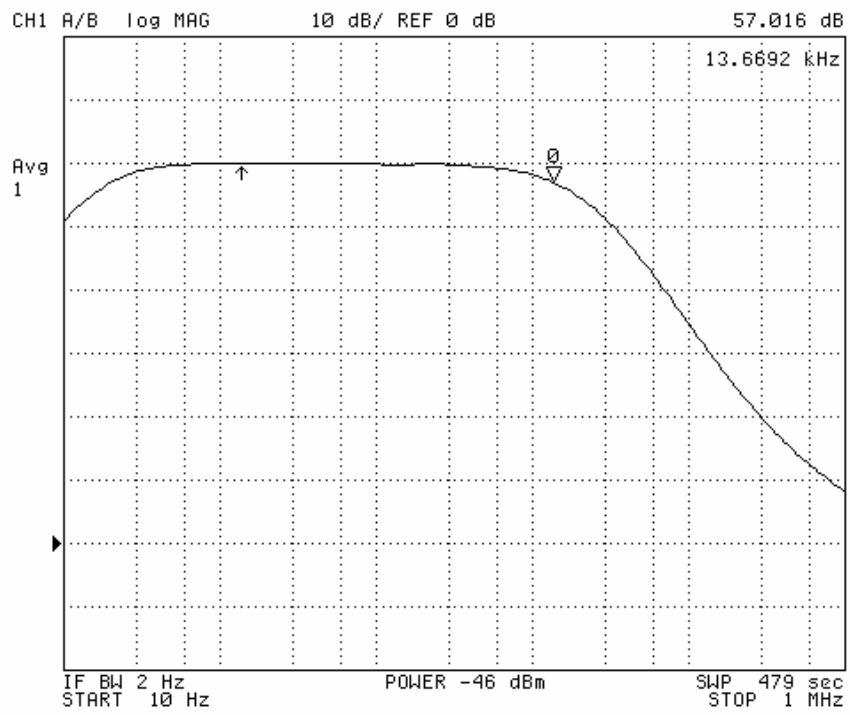


Figure 4.12: Measured frequency response of the designed preamplifier obtained using HP 4395A. The amplifier has 3 dB points at 10 Hz and 13.7 kHz with a mid-band gain of 60 dB gain.

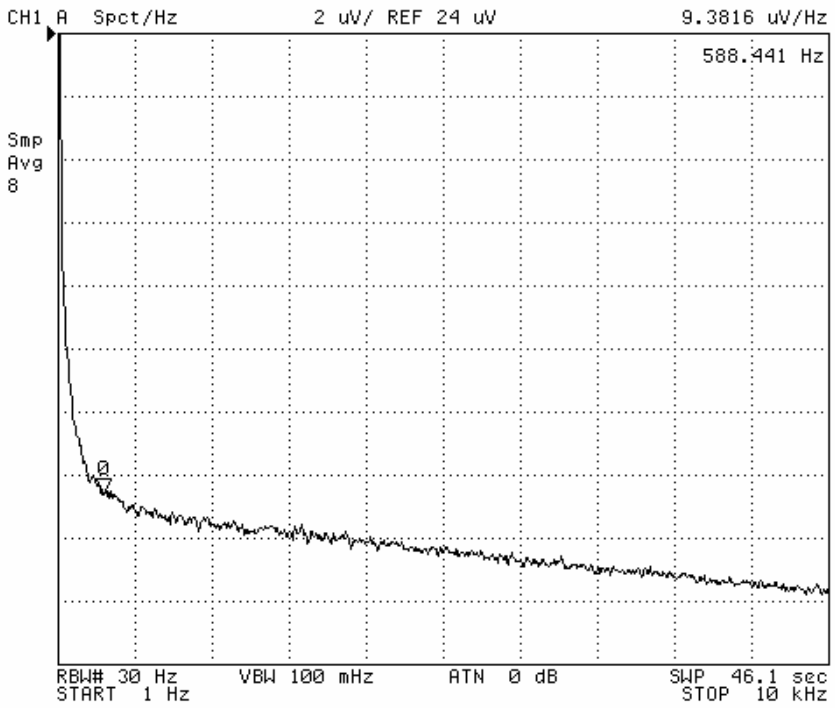


Figure 4.13: Measured noise spectral density of the preamplifier output when the detector is replaced with a 50 Ω resistor.

The measured noise spectral density of the amplifier is subtracted from the measurement result obtained with the addition of a detector, which gives the incremental noise spectral density at the output of the amplifier associated with the detector. To find the detector noise at the input side, the incremental noise spectral density is divided by the amplifier gain at each measurement frequency. Figure 4.13 shows the measured noise spectral density of the p^+-active/n-well diode type microbolometer detector from 0.1 Hz to 4 kHz at 17 μA bias level. The part of the spectrum from 0.1 Hz to 10 Hz is measured using the lock-in amplifier (SRS 830), and the rest of the given spectrum is measured using HP 4395A. The measurement results are combined together and fitted into an expression with 1/*f* and thermal noise components. Total rms noise voltage from 0.1 Hz to 4 kHz is measured as 0.51 μV with a corner frequency of 4.4 Hz. Low corner frequency shows that the 1/*f* noise contribution of the n-well microbolometer is low, which is due to the single crystal nature of the n-well and low 1/*f* noise value at low biasing levels.

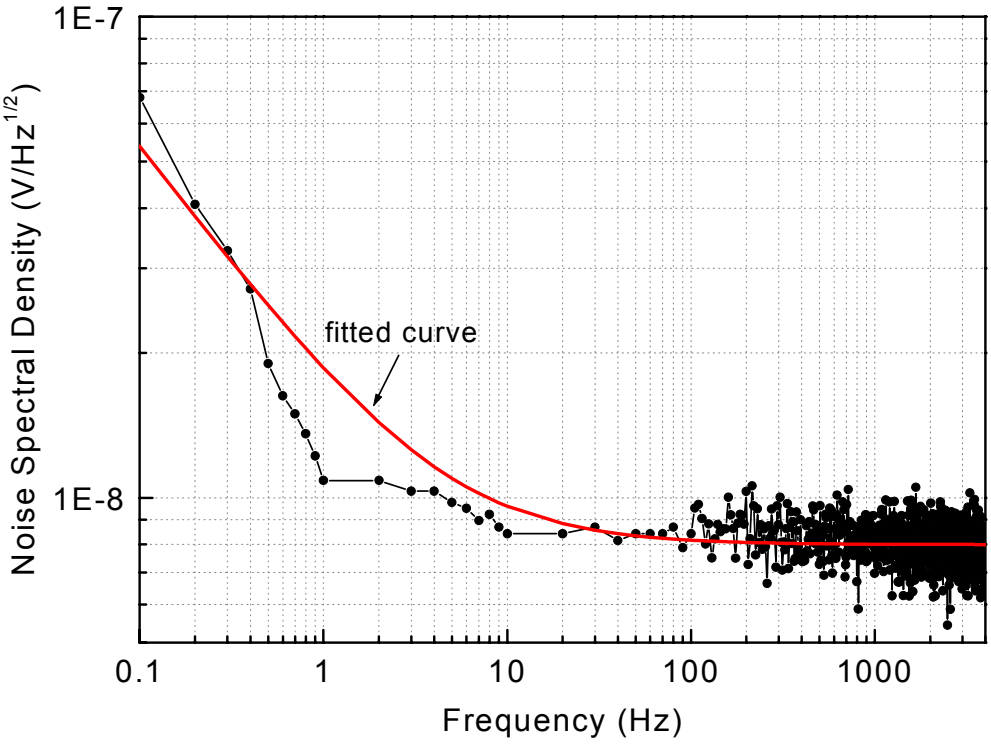


Figure 4.14: Measured noise spectral density of the p^+-active/n-well diode type microbolometer detector from 0.1 Hz to 4 kHz at 17 μA bias level. Total rms noise voltage from 0.1 Hz to 4 kHz is measured as 0.51 μV with a corner frequency of 4.4 Hz.

The noise measurement setup is improved by using a dynamic signal analyzer (Agilent 35670A) which is capable of measuring noise spectrum down to several tens of mHz. To be able to properly measure 1/f noise component, a new low-noise preamplifier is designed with a low frequency corner frequency lower than 100 mHz. Figure 4.15 shows the schematic of the new low-noise preamplifier circuit composed of a bias circuit and two gain stages.

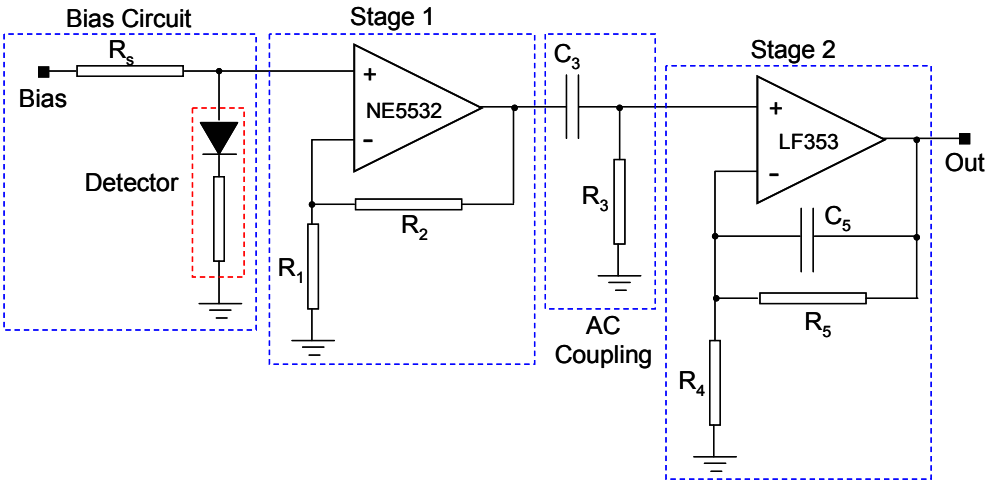


Figure 4.15: Schematic of the new low-noise preamplifier circuit composed of a bias circuit and two gain stages.

The first gain stage is DC coupled, and the second stage is AC coupled. The designed overall gain is close to 50 dB with 3 dB frequencies at 70 mHz and 18.5 kHz. The first gain stage is implemented using a bipolar opamp, which provides low noise at the expense of increased input bias current. Due to its high input bias current, detector is DC coupled. If the AC coupling were used at the input, corresponding input bias of the bipolar opamp would create a DC voltage across the large coupling resistance, which would require another AC coupling between the two gain stages to avoid any possible saturation at the output. The addition of another coupling stage causes sharper roll-over at low frequencies, which is not desired especially for 1/*f* noise measurements. Furthermore, large input resistance associated with AC coupling circuit increases the noise contribution of the bipolar opamps. Therefore, DC coupling is used with a relatively low detector resistance placed in series in the bias circuit. To prevent saturation due to DC coupling, the gain of the

first stage is set as low as 4.3 V/V. The output of the first stage is fed to the next stage using an AC coupling circuit with a 3 dB point set as 70 mHz. The gain of the second stage is set as 72.6 V/V, and its 3 dB point is designed as 18.5 kHz, resulting in a measured mid-band gain of 49.9 dB (312.6 V/V). To avoid saturation due to input bias current, a FET opamp is used in the second stage. Although, the FET opamps have much higher input referred noise voltages, its use is not so critical in this case due to the fact that its input noise is divided by the gain of the first stage while calculating the overall input noise voltage of the preamplifier. Figure 4.16 shows the amplifier placed in a metal box for electromagnetic shielding. To achieve low noise, power is applied using with two 6 V batteries. Bias for the detector is applied using a 1.5 V battery placed inside the box together with the detector to prevent any external interference. Figure 4.17 shows the measured noise spectral density of the diode type microbolometers measured from 0.15 Hz to 6.5 kHz at 17 μA bias level. The measurement is performed using a dynamic signal analyzer (Agilent 35670A). To be able to see the 1/*f* noise component of the detector, the spectrum is divided into three parts from 100 mHz – 12.5 Hz, 12.5 Hz – 110 Hz, and 110 Hz – 6.5 kHz. The two low frequency region is scanned in 400 points, and the last region is scanned in 1600 points.

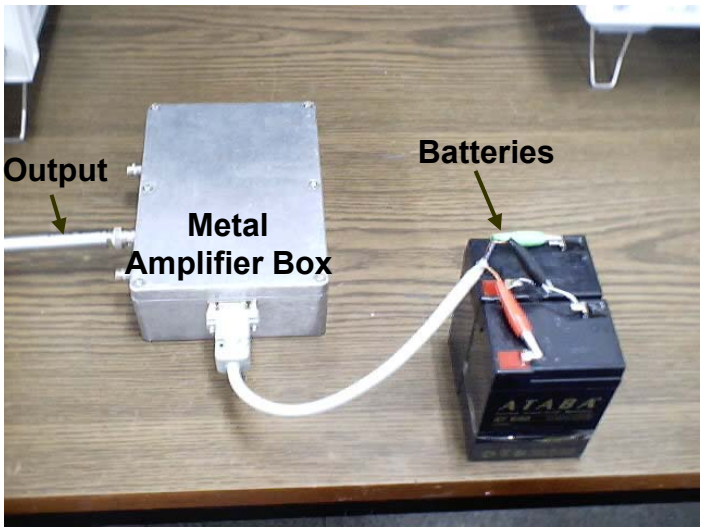


Figure 4.16: Amplifier placed in a metal box for electromagnetic shielding. To achieve low noise, amplifier is powered with 6 V batteries. Bias for the detector is applied using a 1.5 V battery placed inside the box together with the detector to prevent any external interference.

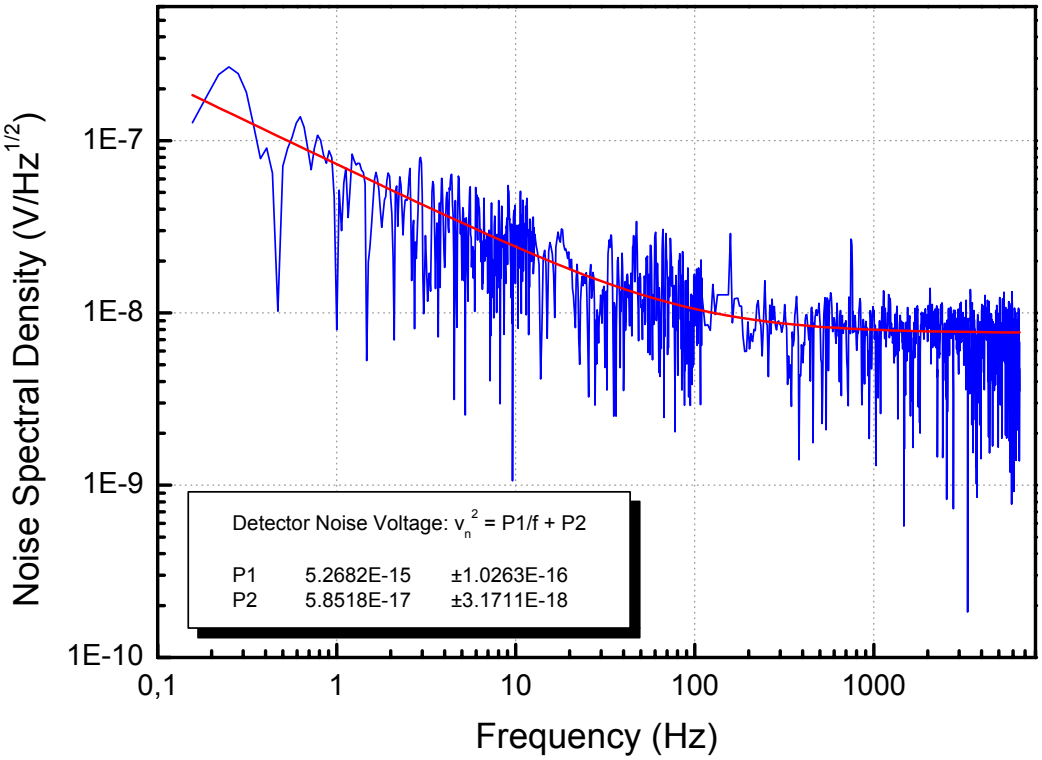


Figure 4.17: Measured noise spectral density of the diode type microbolometers measured from 0.15 Hz to 6.5 kHz at 17 μA bias level. Total rms noise voltage is found as 0.69 μV with a corner frequency of 90 Hz.

The measurement result is fitted into a curve with *1/f* and thermal noise components given as

$$v^2(f) = \frac{K_f}{f} + v_{th}^2 \tag{4.7}$$

where, K_f is the scaling factor of the *1/f* noise, f is the frequency, and v_{th} is the thermal noise spectral density of the detector noise voltage. Using the recorded noise spectrum, K_f and v_{th} are found as 5.27×10^{-15} V^2Hz, and 7.6 nV, respectively. Total rms noise voltage in the above given bandwidth is found as 0.69 μV with *1/f* a corner frequency of 90 Hz. For 8 kHz bandwidth, total noise is measured as 0.74 μV.

4.7 Conclusions

The electrical and optical tests verify that the p^+-active/n-well diode microbolometer detector is capable to detect infrared radiation within a wavelength band of 8 μm – 12 μm. The diode microbolometer has a measured temperature sensitivity of -2 mV/K. Using self-heating method, the physical thermal conductance of the suspended detector is measured as 1.55×10^{-7} W/K. The suspended detector has a measured DC responsivity of 4970 V/W with a thermal time constant of 36 ms. Absorption coefficient of the detector is extracted as 0.45. The electrical bandwidth of the detector is assumed to be 4 kHz, and in this bandwidth total rms detector noise is measured as 0.51 μV. When the detector is scanned at 30 fps, the detector can output only to the 60 % of the maximum available signal level within 33 ms due to its comparably large time constant value. Considering this decrease in the responsivity in the scanned case and the measured electrical noise of the detector, the detectivity (D^*) value of the detector is determined as 9.7×10^8 cmHz$^{1/2}$/W. When the detector is biased with pulsed bias, a slight improvement is also expected due to the negative effect of self-heating on responsivity in continuously biased case. Considering only the detector noise, it is expected that the NETD value of a possible array will be 470 mK when the array is scanned at 30 fps with an electrical bandwidth of 4 kHz using an f/1 optics. It is possible to decrease this NETD value further by decreasing the electrical bandwidth. For example, it is possible to decrease the electrical bandwidth down to 1 kHz for a typical 64 × 64 FPA by using separate channels for each detector column, which will decrease the NETD value down to 250 mK.

Table 4.1 gives the comparison summary for the resistive and diode type n-well microbolometer detectors. At the optimum bias level of 20 μA, the diode type microbolometer detector has a DC responsivity ($\Re$) value of 4970 V/W. Corresponding NETD and detectivity (D*) values are 470 mK and 9.7×10^8 cmHz$^{1/2}$/W, respectively. At 20 μA bias with 125 μsec pulse duration, the diode type microbolometer has a self-heating of 0.27 K. The resistive type microbolometer requires about 8 times higher bias current and 4 times larger pixel

area to obtain the same NETD value as the diode type detector, resulting in an excessive self heating of 2.7 K, which is 10 times larger as compared to that of the diode type detector.

Table 4.1: Comparison of resistive and diode type n-well microbolometer detectors.

Detector Type	Resistor	Diode
Process	AMS 0.8 μm	AMS 0.35 μm
Post-CMOS	Wet etch	RIE + Wet etch
Pixel size (μm^2)	80×80	40×40
Fill factor (%)	13	44
G_{th} (W/K)	6.2×10^{-7}	1.55×10^{-7}
Absorption coefficient	0.6	0.45
Time constant (msec)	21	36
I_{bias} (μA)	170	20
Self-heating (K)	2.7	0.27
Electrical noise (μV)	0.81	0.51
Sensitivity	0.34 %/K	-2.0 mV/K
DC Responsivity (V/W)	4970	4970
D* ($cmHz^{1/2}/W$)	8.9×10^8	9.7×10^8
Expected NETD (mK) (f/1)	470	470

CHAPTER V

5 READOUT CIRCUITS FOR UNCOOLED INFRARED DETECTOR ARRAYS

The readout circuits used for the uncooled infrared detector arrays perform two basic operations: 1) pixel addressing in the detector array and 2) low noise amplification and signal conditioning of the detector signal before any signal processing stages. The addressing circuitry can be common for different detector types, however preamplifier structure differs for different detector types to able to read out different detectors with minimum signal loss and minimum noise contribution.

In the literature, there are basically two types of uncooled microbolometer detectors: resistive microbolometers and diode type microbolometers. The continuous improvement in the uncooled infrared detectors and their readout circuits improved the performance of the uncooled imaging arrays at reduced device size, power consumption, and overall cost.

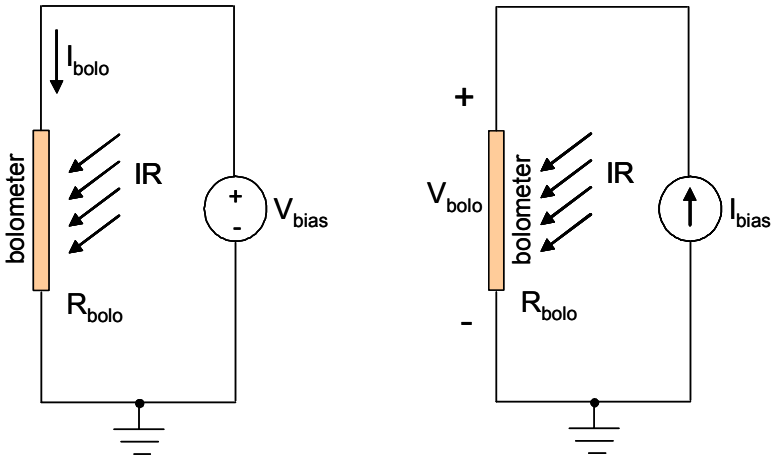
This chapter is organized as follows: Section 5.1 gives the biasing circuits used for most of the uncooled detectors. Effects of process variation and fluctuation in the operating temperature are discussed in detail. Section 5.2 explains the self-heating effect and gives methods to compensate for the self-heating effect. Section 5.3 presents the low-noise preamplifiers reported in the literature for the resistive

microbolometer detectors. Section 5.4 introduces the diode type microbolometers and the preamplifiers used for the diode type microbolometers. Section 5.4 also introduces the low noise readout circuit developed for the p^+-active/n-well diode microbolometer detector arrays developed within this study. Section 5.5 explains the general readout architecture of the uncooled infrared detector arrays. Section 5.6 discusses the non-uniformity issue in the uncooled detector arrays and proposes methods to compensate for this problem. Finally, Section 5.7 gives the summary of the different preamplifiers presented in this chapter.

5.1 Biasing Circuits for the Uncooled Detectors

Biasing circuitry is required for all of the uncooled detector types except for the thermoelectric and pyroelectric detectors. Resistive and diode type microbolometers need to be biased by a voltage or current source in order to sense the changes in the detector parameter upon absorbed infrared radiation. This section first explains the biasing circuits and very simple readout circuits used for the resistive and diode type microbolometers.

The simplest and most direct method of reading out a resistive microbolometer is to apply a voltage or current bias and to measure the pixel current or voltage for resistance measurement. Figure 5.1 (a) and (b) show the two basic methods to measure the resistance value of the resistive microbolometer detectors, which use constant voltage biasing with current reading and constant current biasing with voltage reading methods, respectively.



(a) (b)

Figure 5.1: Two basic methods to measure the resistance value of the resistive microbolometer detectors: (a) constant voltage bias-current reading and (b) constant current bias-voltage reading methods.

Among these methods, constant voltage bias can be implemented easily with minimum additional electronic noise, since the implementation of stable and low-noise current sources is not an easy task [58]. Although constant voltage or constant current biasing methods are very simple, they have some major disadvantages. First of all, the resistance readings obtained with these simple circuits are absolute and are affected by process variations as well as by the fluctuations in the operating temperature. Secondly, the detector temperature starts rising with the application of bias pulse, known as self-heating effect. The detector voltage changes related with the changes in the detector resistance due this self-heating effect, and usually the self-heating induced change in the detector voltage is much larger than what can be achieved with infrared radiation.

The effects of process and operating temperature variations can be reduced by performing a ratio based measurement which can be obtained using resistive divider circuits operating in half bridge or full bride modes. These bridge circuits can also be used to compensate for the self-heating effect. Figure 5.2 shows the half bridge and full bridge circuits used for the resistive microbolometers, where R_{bolo} and R_{load} are the resistance of the microbolometer detector and the resistive load, respectively. Load resistances are implemented on the substrate without any thermal isolation; therefore, they are insensitive to infrared radiation. Optically shielded

microbolometer is electrically identical to the bolometer pixel, and it is suspended and made insensitive to infrared radiation by increased thermal conductance value. This optically shielded detector is mainly used to cancel the variation in the detector voltage due to the self-heating effect. Being suspended and being identical to the actual bolometer detector, the temperature of the optically shielded detector rises similarly as the actual bolometer detector, and self-heating generated signal component at the detector output is canceled by using a differential readout circuit. Since the optically shielded bolometer can not respond to the infrared radiation, there is no loss in the actual infrared induced voltage at the detector output. Section 5.3 explains the details of the self-heating.

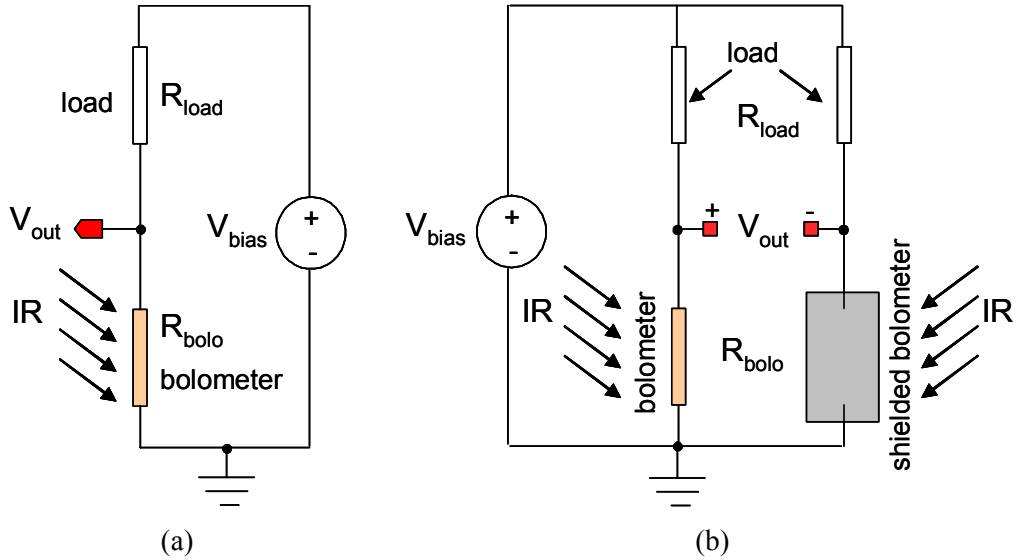


Figure 5.2: Bridge circuits for the resistive microbolometers: (a) half bridge and (b) full bridge circuits, where R_{bolo} and R_{load} are the resistance of the microbolometer detector and the resistive load, respectively.

Responsivity value ($\Re$) for the half bridge and full bridge circuits are given as

$$\Re = \frac{R_{bolo}R_{load}}{\left(R_{bolo}+R_{load}\right)^2}\frac{\eta\alpha V_{bias}}{G_{th}} \tag{5.1}$$

where, R_{bolo} and R_{load} the resistance of the load and bolometer resistors, η is the absorption coefficient, α is the TCR of the bolometer resistor, V_{bias} is the applied constant DC bias voltage, and G_{th} is the thermal conductance of the detector..

In order to achieve maximum responsivity, load resistance and bolometer resistance values should match [43], and in that case responsivity expression is simplified to

$$\Re = \frac{\eta \alpha V_{bias}}{4G_{th}} \tag{5.2}$$

where, η is the absorption coefficient, α is the TCR of the bolometer resistor, V_{bias} is the applied constant DC bias voltage for the bridge structures, and G_{th} is the thermal conductance. To calculate the NETD value, electrical noise voltages of the half bridge and full bridge structures are required, which are given as

$$V_{n\_half} = \sqrt{4kT\left(\frac{R_{bolo}R_{load}}{R_{bolo}+R_{load}}\right)\Delta f} \tag{5.3}$$

$$V_{n\_full} = \sqrt{8kT\left(\frac{R_{bolo}R_{load}}{R_{bolo}+R_{load}}\right)\Delta f} \tag{5.4}$$

respectively, where k is the Boltzmann constant, T is the temperature, R_{bolo} and R_{load} are resistance values of the bolometer and the load resistors, and Δf is the electrical bandwidth. When the load resistance is adjusted to be the same as bolometer resistance for maximum responsivity, then the noise voltages for the half and full bridge configurations reduce to

$$V_{n\_half} = \sqrt{2kTR_{bolo}\Delta f} \tag{5.5}$$

$$V_{n\_full} = \sqrt{4kTR_{bolo}\Delta f} \tag{5.6}$$

respectively, where k is the Boltzmann constant, T is the temperature, R_{bolo} and R_{load} are resistance values of the bolometer and the load resistors, and Δf is the electrical bandwidth. Although the responsivity values are the same, the noise voltage of the full bridge structure is √2 times higher due to the fact that the part implemented with

the optically shielded bolometer does not contribute to the signal level but to the circuit noise. However, the full bridge structure is still used to cancel the DC signal that occurs at the half bridge output and to make the signal output insensitive to small variations in the bridge bias voltage. The NETD values for half bridge ($NETD_{half}$) and full bridge ($NETD_{full}$) structures are given as

$$NETD_{half} = \frac{4F^2\sqrt{4kTR_{bolo}R_{load}/\left(R_{bolo}+R_{load}\right)\Delta f}}{A_{\det}R_{bolo}R_{load}\alpha V_{bias}/\left(R_{bolo}+R_{load}\right)^2\left(dP/dT\right)_{\lambda}} \tag{5.7}$$

$$NETD_{full} = \sqrt{2}\ \ NETD_{half} \tag{5.8}$$

where, F is the f-number of the optics, k is the Boltzmann constant, T is the temperature, R_{bolo} and R_{load} are the resistance values for the bolometer and the load resistors, Δf is the electrical bandwidth, A_{det} is the active detector area, α is the TCR of the bolometer detector, V_{bias} is the bridge bias voltage, and $(dP/dT)_{\lambda}$ is a constant equal to 2.62×10^{-4} $WK^{-1}cm^{-2}$ for the 8 μm – 12 μm spectral window. Maximum detector performance is achieved with minimum possible NETD value, and maximum responsivity does not necessarily result in the minimum NETD value. Minimum NETD value depends on the load resistance value, detector structure, bias voltage, and electrical bandwidth. The condition for load resistance to achieve minimum possible NETD value is found by differentiating the NETD expression for the half bridge case with respect to load resistance (R_{load}). The condition for the minimum NETD value is given as

$$R_{load} = R_{bolo}/2 \tag{5.9}$$

where, R_{bolo} is the given bolometer resistance, and this result is different than the condition for the maximum responsivity condition. This result suggests that the NETD value becomes minimum when the load resistance is selected to be equal to the half of the bolometer resistance. In fact, when the load resistance is adjusted for maximum responsivity, then there is only about 9 % increase in the NETD value as compared to its minimum value.

5.2 Self-Heating Compensation

Self-heating is an unavoidable effect observed in the resistive and diode type microbolometers with the application of bias pulses. The electrical power dissipated in the suspended detector rises its temperature even though the bias duration is much shorter than the associated thermal time constants of the detectors. This is mainly due to the fact that the applied electrical bias power is about three orders of magnitude higher than typical absorbed infrared radiation power levels. Therefore, before reaching the steady state, the temperature of the pixel rises well above a few degrees of its rest temperature before the application of the bias pulse. When the self-heating effect is uncompensated, then the readout circuits are required to have very high dynamic range, complicating the circuit design and increasing the overall chip area.

There are three approaches reported so far to compensate for the self-heating effects. One method uses an external circuitry which emulates the change in the detector voltage for compensation purposes [59]. This method is simple since it uses external electronics, but causes noise coupling at the very beginning of the signal processing line, reducing the overall performance. The second method is based on the design of a matched reference detector to generate the same self-heating effect to be subtracted from the output voltage of the actual detector with the help of a full bridge structure followed by a differential readout [60]. Although this method solves the self-heating problem on the chip-level without requiring any complex circuitry, the complete cancellation of self-heating is not possible due to the matching problems of the actual pixel and the optically shielded reference pixel. The main problem arises when an imaging array is formed, where the reference pixels are designed with increased thermal conductance values so that they can cool down much faster and can be addressed more frequently serving a group of actual array pixels. Therefore, the change in the detector structure causes mismatches in their heating cycles, making complete compensation not possible. The third method considers self-heating similar to other effects that cause non-uniformity, and corrects it by applying an equivalent correction signal to the detector output before the signal

is amplified or integrated [61]. In the design of the 64 × 64 FPA the second method is used, and in the design of the 128 × 128 the combination of the last two methods are used.

The full bridge structure is also useful in the compensation of the self-heating effect. The optically shielded reference detector in the full bridge configuration is used to cancel the voltage change in the bolometer detector due to the self-heating. Since the optically shielded detector is identical to the actual bolometer detector, its voltage is affected in the same way as the actual bolometer detector. Therefore, this acts as a common signal which is canceled with the help of a differential readout circuit using a Wheatstone bridge configuration [21]. After the biasing circuits the detector signals are amplified with low noise preamplifiers. The next section explains in detail the preamplifier circuits.

5.3 Preamplifiers for the Resistive Microbolometers

The preamplifiers used for the resistive microbolometers have usually a simple biasing circuit followed by an integrator. The preamplifiers sense and amplify the detector current or detector voltage with minimum noise contribution. This section will give four preamplifier examples to sense current or voltage of the resistive microbolometers: 1) Bolometer current direct injection (BCDI) [61], 2) capacitive transimpedance amplifier (CTIA) [23, 25], 3) Wheatstone bridge differential amplifier (WBDA) [21], and 4) constant current buffered direct injection (CCBDI) [58] circuits. The first two preamplifiers convert the detector current to voltage through an integration process which limits the bandwidth and provides gain. The last two preamplifiers convert the detector voltage to current with a low noise differential preamplifier whose output is integrated providing bandwidth limitation and gain.

5.3.1 BCDI Preamplifier Circuit

Bolometer current direct injection (BCDI) preamplifier is used for the resistive microbolometers, and they are fabricated using bipolar technology due to the fact that the circuit noise can be decreased considerably as compared to MOS technology. Figure 5.3 shows the schematic of the BCDI preamplifier circuit used for a 320 × 240 resistive microbolometer detector array [61].

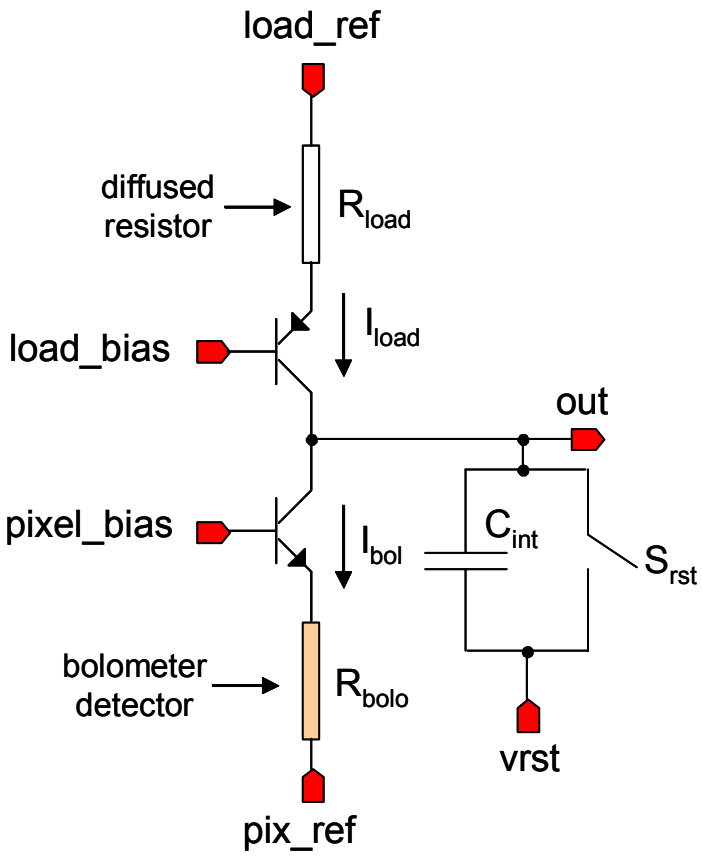


Figure 5.3: Schematic of the BCDI preamplifier circuit used for a 320 × 240 resistive microbolometer detector array [61].

In the BCDI preamplifier circuit, the detector is biased by constant voltage, and the detector current is integrated across an integration capacitor. The preamplifier is composed of common base NPN and PNP type bipolar transistors. The bolometer resistor is connected to the emitter of the NPN type transistor, and it is biased by applying a bias potential to the base of the transistor. The bolometer

bias potential is the difference of the pixel bias (*pixel_bias*) voltage and pixel reference (*pix_ref*) potentials, and it is lower than this difference by a base-emitter voltage drop of the NPN transistor. The current flowing through the bolometer detector has a large DC component, which is cancelled by using a current sink circuit implemented with a symmetric circuit structure constructed using a PNP bias transistor and a load resistor. The load resistor is not a bolometer, and it is implemented with diffused resistors on the substrate. Similarly, the required bias voltage for the load resistor is applied by the reference bias voltage applied to the base of the PNP transistor. Using a load resistor different than the detector resistance complicates compensation of temperature effects in the bias circuitry. In fact, the pixel and reference bias voltages are generated by a temperature stabilized bias generator so as to keep the bias of the bolometer detector and load resistor constant for a given temperature range, simplifying the required temperature stabilizers. The self-heating effect is not compensated at the biasing level of the detectors, but it is solved in circuit level which will be explained later in this section. The difference of the bolometer and load currents is integrated across the integration capacitor (C_{int}).

Figure 5.4 shows the variation of integration capacitor voltage ($V_c(t)$) in time neglecting the self-heating effect. One plate of the integration capacitor is at a reference potential (V_{rst}), and the capacitor is periodically reset for a fixed reset duration of time (t_{rst}) before an integration period (t_{int}) starts. In this analysis, it is assumed that the detector is unaffected by the infrared radiation and self-heating during the short integration period. The assumption for the effect of infrared radiation is realistic; however, the latter is not. Effect of self-heating on the integration curve will be explained in the following paragraph.

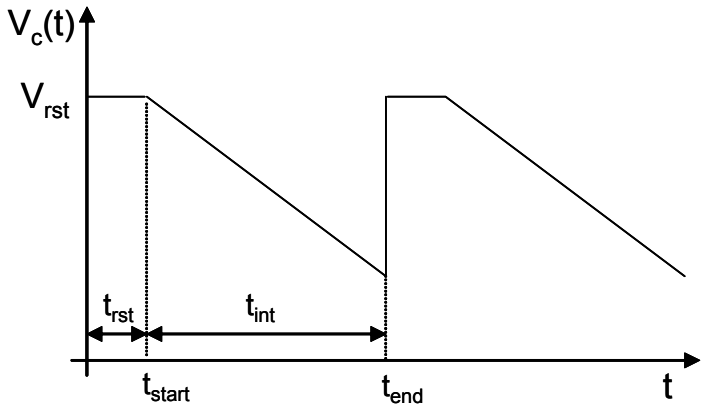


Figure 5.4: Variation of integration capacitor voltage ($V_c(t)$) in time neglecting self-heating effect. One plate of the integration capacitor is at a reference potential (V_{rst}), and the capacitor is periodically reset for a fixed reset duration of time (t_{rst}) before an integration period (t_{int}) starts.

The main advantage of the integration is that it limits the electrical bandwidth, and it amplifies the signal with a certain gain. The electrical bandwidth (BW) [62] and gain of the preamplifier (A_{preamp}) are given as [61]

$$BW = \frac{1}{2t_{\text{int}}} \tag{5.10}$$

$$A_{preamp} = \frac{t_{\text{int}}}{R_{bolo}C_{\text{int}}} \tag{5.11}$$

where t_{init} is the integration period, R_{bolo} is the bolometer resistance, and C_{int} is the integration capacitance. The integration time is kept as 30 μs, which results an electrical bandwidth of about 17 kHz for the 320 × 240 FPA. If we assume that bolometer resistance is 20 kΩ, and integration capacitance is 10 pF, then the preamplifier gain is found as 150 V / V, which is sufficient to suppress the noise contributions of the next stages to the detector input. The measured input referred noise of the readout circuit is reported as 6.2 μV for 17 kHz bandwidth, where the contribution of the preamplifier noise is extracted as 4.4 μV. It is estimated that the designed readout circuit provides an NETD value of between 34 mK and 67 mK when integrated with a detector where the pixels have a TCR value between 1 % / K and 2 % / K [61].

Since the load resistor is implemented using a diffused resistor on the substrate, it will be heated negligibly upon the application of bias pulse. However, the detector temperature will be heated up with the applied bias, because it is thermally isolated from the substrate, and power dissipated or absorbed by the detector rises its temperature. Although the bias duration is very short, and the detector does not reach a steady state, the rise in the temperature is in the order of a few degrees centigrade, which is an order of magnitude larger than what would be achieved by a typical infrared radiation level. The difference in the heating cycles of the detectors causes mismatches in the detector and load resistance values, which in turn results an offset current at the output of the BCDI output even at the absence of infrared radiation. Therefore, it is necessary to compensate for the variations in the detector current in order to prevent any saturation at the following integrator stage due to the limited dynamic range of the integrator circuit specially designed to integrate weak current signals for long periods for signal amplification and bandwidth limitation. Figure 5.5 (a) and (b) show the variation of bolometer current and integrator capacitance voltage in the BCDI circuit with respect to time including the effect of self-heating and absorbed infrared radiation, respectively [61]. The load current is adjusted to be the average of the detector current which changes during integration period due to the self-heating even in the absence of infrared radiation. In the absence of infrared radiation, the integrated current is positive in the first half of the integration period, and it becomes negative in the second half of the integration time. Therefore, capacitor voltage first rises from its reset level (V_{rst}) and makes a peak at the mid point of the integration time where integration current is zero, and becomes negative from this point on. At the end of the integration period, the capacitor voltage returns back to its reset value with zero difference voltage indicating zero infrared radiation. The detector current increases, when the detector is illuminated with infrared radiation. This results a net voltage difference in the integrator output, which is related with the infrared radiation only and does not contain any terms related with the self-heating effect. The adjustment of load current is performed by changing the bias voltage of the load resistor, which is controlled by an external circuitry [61].

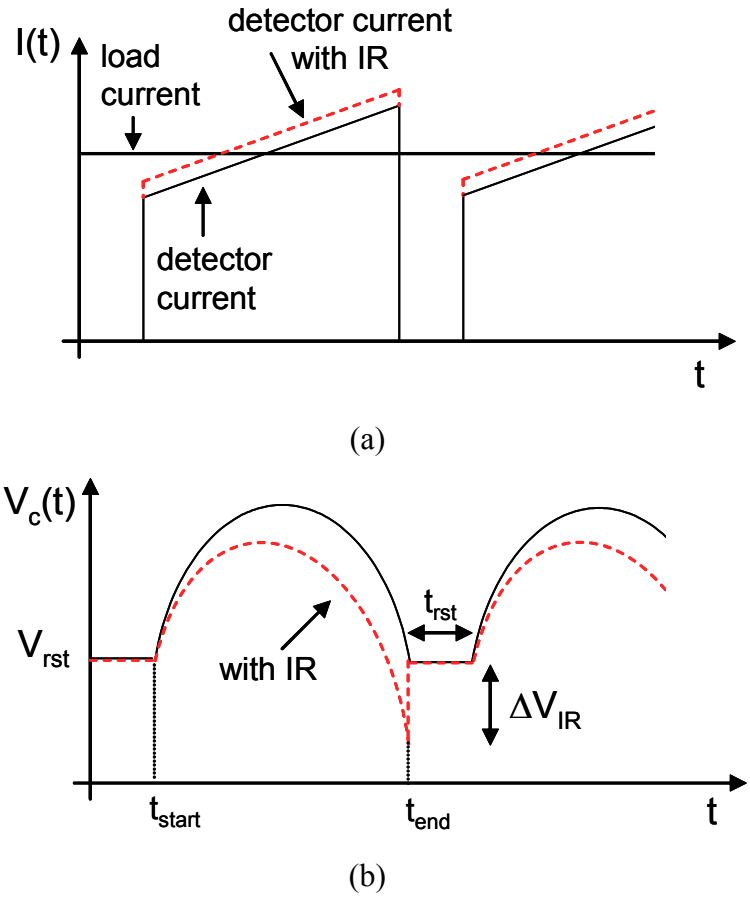


Figure 5.5: Operation of the BCDI circuit with respect to time including the effect of self-heating and absorbed infrared radiation: (a) variation of bolometer current and (b) integration capacitance voltage [61].

One of the main disadvantages of the BCDI circuit is that the integration capacitance is connected directly to the output node of the biasing circuit. Although the output resistance of the biasing circuit is improved using direct injection transistors, it is still not sufficient to keep the integrated current independent of the integrated output voltage. Figure 5.6 shows the small signal model of the output stage.

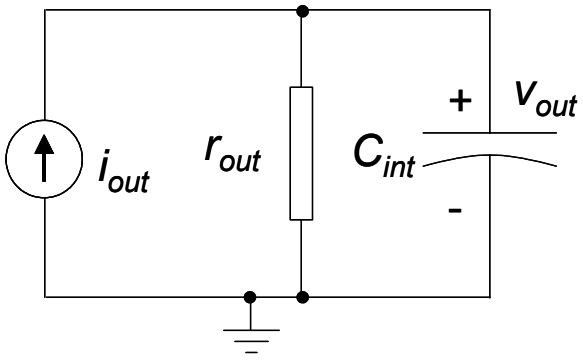


Figure 5.6: Small signal model of the of the output stage.

When the integration period starts, the capacitor acts as a short circuit, and integrates all the current (i_{out}) available at the output. After a certain period of time, voltage across the integration capacitor (C_{int}) is high enough to induce current through the output resistance (r_{out}), decreasing the current being integrated. The decrease in the integrated current decreases gradually the slope at the output, making it deviate from the ideal integrator operation. Assuming that the above small signal model holds for a wide range of output voltage swing, then the output voltage (v_{out}) can be expressed as

$$v_{out} = i_{out} r_{out} \left(1 - e^{-t/\tau}\right) \tag{5.12}$$

$$\tau = r_{out} C_{\text{int}} \tag{5.13}$$

where, i_{out} is the small signal output current, r_{out} is the output resistance of the direct injection biasing circuit, C_{int} is the integration capacitance, t is the time, and τ is the time constant of the output stage given above.

As the output voltage decreases due to the incident infrared radiation, a current will be induced flowing into the capacitor so as to cancel the decrease in the output voltage. When the integration time is much shorter than the time constant, then the exponential variation of the output voltage can be approximated as

$$v_{out} = i_{out} r_{out} \left(1 - \left(1 - \frac{t}{r_{out} C_{\text{int}}} \right) \right) = \frac{i_{out} t}{C_{\text{int}}} \tag{5.14}$$

where, i_{out} is the small signal output current, t is time, and C_{int} is the integration response.

Typical values for the time constant value range between a few micro seconds to a few tens of micro seconds, which is not negligible as compared to the typical integration times ranging from 10 μs to 100 μs; therefore, the output signal is distorted. To avoid distortion, either integration capacitance is increased, or the integration period is kept shorter. Increasing the integration capacitance decreases the gain and increases the implementation area, especially when variable integration capacitors are used to improve the dynamic range of the circuit. Decreasing the integration time increases the electrical bandwidth resulting in excessive circuit noise. When the integration period is kept shorter, the scanning rate can be increased above 30 fps. In this case, the additional frames can be averaged to reduce the increased noise level.

The problem of the output loading can be solved by using an actual integrator circuit with nearly zero input resistance. Integrator circuits are mostly used in switched capacitor circuit applications mainly developed in CMOS technology due to the possibility of implementing high quality switches and capacitors. Furthermore, in CMOS the integration density is higher, and the overall chip cost is lower, making CMOS technology and ideal for readout circuits applications.

5.3.2 CTIA Preamplifier

Figure 5.7 shows the simplified schematic of a preamplifier circuit called capacitive transimpedance amplifier (CTIA), where the detector is biased by a constant voltage, and the detector current is integrated using a switched capacitor reset integrator [25]. This preamplifier structure is commonly used in the readout circuits of the resistive uncooled detector arrays [23, 25].

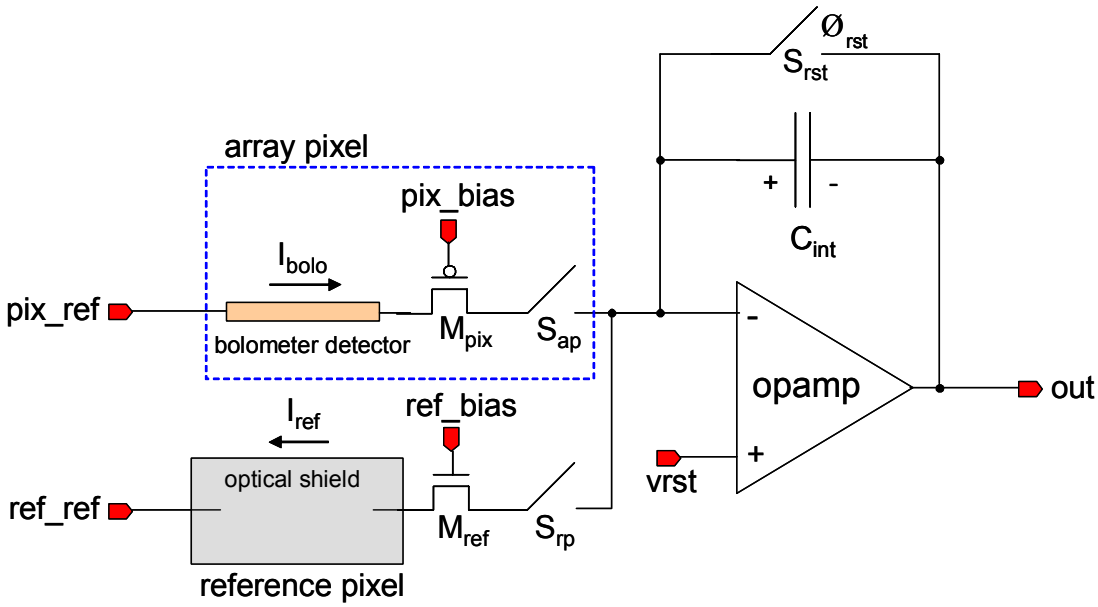


Figure 5.7: Simplified schematic of a preamplifier circuit called capacitive transimpedance amplifier (CTIA), which is commonly used in the readout circuits of the resistive uncooled detector arrays [25].

The detector bias in the CTIA preamplifier is performed using a p-channel MOS transistor (M_{pix}) acting as a direct injection transistor. One terminal of the array pixel is at the pixel reference potential (*pix_ref*), and the other terminal of the array pixel is at a potential which is one source-to-gate potential higher than the applied pixel bias voltage (*pix_bias*). Since the change in the detector current is negligibly small as compared to its DC level, the change in the source-to-gate potential of the direct injection transistor is negligible providing a stable bias voltage to the array pixel. The DC portion of the detector current is cancelled by using a reference pixel, which is biased similar to the array pixel, but in reverse polarity. To bias the reference pixel in reverse polarity, an n-channel MOS transistor is used as a direct injection transistor. The reference bias potential (*ref_bias*) and reference potential (*ref_ref*) for the reference pixel are adjusted so as to sink the DC current of the array pixel before entering the CTIA circuit. The negative input of the opamp follows the DC potential at the positive opamp input terminal making the input stay at the signal ground with zero input impedance. Therefore, theoretically the entire infrared induced detector current is integrated in the integrator without any loss in the

gain. The output impedance of the biasing circuit of the detector and load resistances implemented using direct injection transistors is given as

$$r_{out} = \frac{1+(g_m + g_d)R_{bolo}}{2g_d} \cong \frac{g_m R_{bolo}}{2g_d} \tag{5.15}$$

where, g_m and g_d is the input and output transconductance value of the n-channel and p-channel biasing transistors which are assumed to have same values, and R_{bolo} is the resistance of the bolometer detector and the identical reference detector. In the above expression it is assumed that g_m is much larger than g_d, and the term $g_m R_{bolo}$ is much larger than unity. Furthermore, the effect of bulk-to-source transconductance is neglected. The factor of two in the denominator is due to the parallel combination of the detector and reference bias circuits. As expected the output resistance of the direct injection biasing circuit is much higher than the detector resistance and output resistance of the transistor, a well known feature of the common gate or cascode connection [63]. The advantage of high output resistance is that it reduces the contribution of the opamp input noise to the detector input, making the CTIA circuit very suitable for the readout circuits of the resistive uncooled detectors, especially attractive for detectors with relatively large resistance values.

The current responsivity of the detectors biased with the direct injection transistors is reduced due to the inherent negative feedback that exists in the biasing circuit. For negative TCR materials, the detector resistance decreases upon absorbed infrared radiation, causing an increase in the detector current. This in turn increases the required gate overdrive voltage causing a drop in the actual detector bias voltage. The decrease in detector bias voltage tends to decrease the detector current due to the negative feedback effect. The negative feedback tends to decrease the current responsivity of the detector ($\Re_I$), and $\Re_I$ is given as

$$\Re_I = \frac{g_m R_{bolo}}{1+g_m R} \frac{I_0 \alpha \eta}{G_{th}} \tag{5.16}$$

where, g_m is the transconductance of the direct injection MOS biasing transistor, R_{bolo} is the detector resistance, I_0 is the detector bias current under no infrared radiation, α is the TCR of the detector resistance, η is the infrared absorption coefficient of the detector, and G_{th} is the thermal conductance of the detector. In the above expression, the effect of the output resistance and bulk-to-source transconductance of the transistor are neglected. In order to maximize the current responsivity for a given bias current, the $g_m R_{bolo}$ product term should be maximized. This is possible for selecting a large detector resistance and a large W/L ratio for the MOS transistor. Figure 5.8 shows the noise sources in the CTIA circuit with direct injection biasing circuits composed of a MOS transistor, detector resistance, and an opamp integrator circuit.

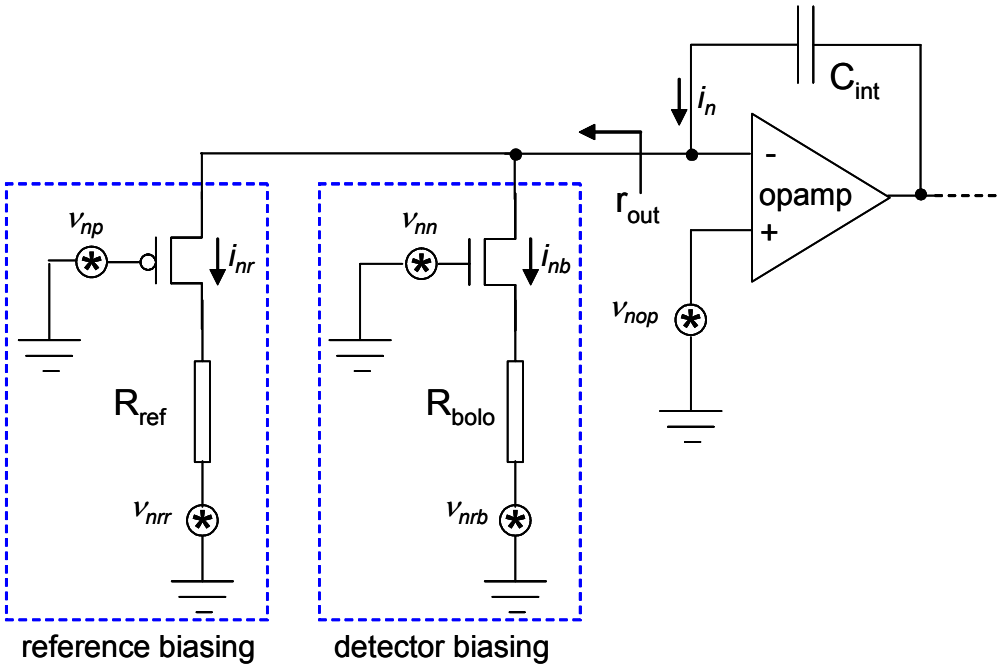


Figure 5.8: Noise sources in the CTIA circuit with direct injection biasing circuits composed of a MOS transistor, detector resistance, and an opamp integrator circuit.

The noise power spectral density of the CTIA input current is the sum of the noise currents in the detector and reference bias circuits, and the noise current generated by the opamp input referred noise. The noise current power spectral density for the bias circuit includes both the thermal noise component and the flicker

noise component. Neglecting the effect of the output resistance of the transistor, the noise power spectral density of the detector biasing circuit (i_{nb}^2) and reference biasing circuit (i_{nr}^2) are given as

$$i_{nb}^2 = \frac{g_{mn}^2}{\left(1+g_{mn}R_{bolo}\right)^2}\left(\frac{8kT}{3g_{mn}} + \frac{K_{fn}}{C_{ox}(WL)_n f} + 4kTR_{bolo} + \frac{I_{bolo\_bias}^2 R_{bolo}^2 K_{fbolo}}{f}\right) \quad (5.17)$$

$$i_{nr}^2 = \frac{g_{mp}^2}{\left(1+g_{mp}R_{ref}\right)^2}\left(\frac{8kT}{3g_{mp}} + \frac{K_{fp}}{C_{ox}(WL)_p f} + 4kTR_{ref} + \frac{I_{ref\_bias}^2 R_{ref}^2 K_{fref}}{f}\right) \quad (5.18)$$

where, g_{mn} and g_{mp} are the transconductance values of the direct injection n-channel and p-channel MOS biasing transistor, R_{bolo} and R_{ref} are the resistance values for the detector and reference, K_{fn} and K_{fp} are the scaling factors of the gate referred flicker noise components of the n-channel and p-channel transistors, C_{ox} is the unit gate oxide capacitance value of the transistors, W and L are width and length of the n-channel and p-channel MOS transistors, f is the frequency, k is the Boltzmann constant, T is the temperature, I_{bolo_bias} and I_{ref_bias} are the bias current values for the bolometer and reference detectors, and K_{fbolo} and K_{fref} are scaling factors for the flicker noise components of the bolometer and reference detectors. The total noise power spectral density of the CTIA input current is given as

$$i_n^2 = i_{nb}^2 + i_{nr}^2 + \frac{v_{nop}^2}{r_{out}^2} \quad (5.19)$$

where, v_{nop} is the opamp input referred noise voltage, and r_{out} is the output resistance of the biasing circuits operating in parallel. If the transconductance and output conductance parameters for the n-channel and p-channel transistor match, if the bolometer and reference detectors are identical to each other and biased at the same level, and if the $g_m R_{bolo}$ term is much larger then unity, then the CTIA input current noise power spectral density is simplified to

$$i_n^2 = \underbrace{\frac{8kT}{R_{bolo}} + \frac{2I_{bias}^2 K_{fbolo}}{f}}_{DETECTOR\ and\ LOAD} + \underbrace{\frac{16kT}{3g_m R_{bolo}^2} + \frac{1}{R_{bolo}^2 C_{ox} f}\left(\frac{K_{fn}}{(WL)_n} + \frac{K_{fp}}{(WL)_p}\right)}_{BIAS\ TRANSISTORS} + \underbrace{\frac{4g_d^2 v_{nop}^2}{g_m^2 R_{bolo}^2}}_{OPAMP} \qquad (5.20)$$

where g_m and g_d are the transconductance and output conductance values of the direct injection MOS transistors, R_{bolo} is the resistance for the detector and reference, K_{fn} and K_{fp} are the scaling factors of the gate referred flicker noise components of the n-channel and p-channel transistors, C_{ox} is the unit gate oxide capacitance value of the transistors, W and L are width and length dimensions of the n-channel and p-channel MOS transistors, f is the frequency, k is the Boltzmann constant, T is the temperature, I_{bias} is the bias current for the detector and reference, K_{fbolo} is the scaling factor for the voltage flicker noise component of the bolometer detector and reference, and v_{nop} is the input referred noise of the opamp. The contribution of noise sources for each term is given in the above equation, which states that the $g_m R_{bolo}$ term should be maximized in order to decrease the noise contribution of the biasing circuitry and opamp used in the CTIA circuit. Using large detector resistances helps reducing the input noise of the readout circuitry. Furthermore, for a given detector bias current, the g_m value can be increased by using large W/L ratios. Based on the above noise analysis, the noise performance of the direct injection biasing technique with the CTIA circuit is better for the high resistance detectors, where the noise terms associated with the bias transistors and opamp in the noise expression can be neglected. As mentioned previously, the noise contribution of the detector and load are assumed to be same. In practice, the resistance of the load resistor is selected to be larger than that of the detector, reducing the noise contribution of the load. On the other hand, for the low resistance detectors, the noise contribution of the direct injection transistors and opamp are not negligible, limiting the performance of the low resistance detectors such as the n-well microbolometers. One of the uncooled arrays using CTIA circuit has 160 × 128 pixels scanned by an 8-channel parallel readout circuit. The reported NETD value is 80 mK for an f/1.8 optics, which is achieved for a detector bias of 4.25 V for a detector with a TCR value of 2.74 % [23]. The other uncooled array that uses CTIA circuit has 320 × 240 pixels with 45 μm pitch with an NETD value of 70 mK for f/1 optics, and it has been reported that 36 mK NETD has been achieved using a pixel pitch of 35 μm [25].

5.3.3 WBDA Preamplifier

WBDA preamplifier structure uses a Wheatstone bridge type differential detector biasing circuit followed by a low noise differential preamplifier and an integrator circuit. Figure 5.9 shows the schematic of the Wheatstone bridge type differential readout circuit used in a modern 640×480 uncooled microbolometer FPA [21]. The detector voltage is sensed by a low noise differential transconductance amplifier with respect to the reference detector voltage, which is identical to the actual detector and is optically shielded. Since the reference detector is biased in the same way as the infrared detector, most of the errors coming from process variations, self-heating, and fluctuations in the operating temperature are cancelled to a great extend. The output of the differential transconductance amplifier is then integrated to achieve filtering operation and additional gain.

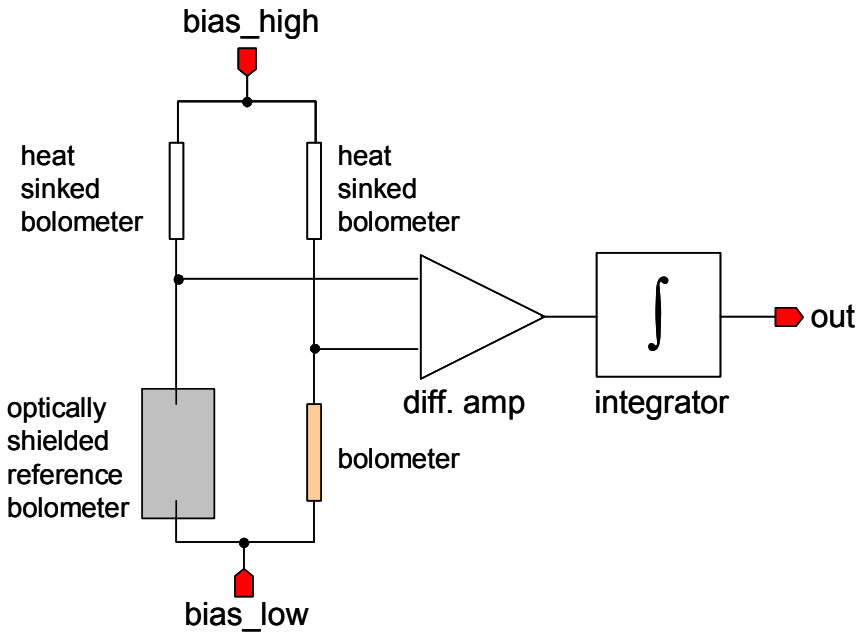


Figure 5.9: Schematic of the Wheatstone type differential readout circuit used in a modern 640×480 uncooled microbolometer FPA [21].

The output resistance of the full bridge circuit is lower than that of the direct injection bias circuits explained before. Therefore, for proper voltage measurement, the differential preamplifier should have high input impedance with minimum input

referred noise voltage. The required impedance level is achieved easily using MOS preamplifiers with relatively large input device dimensions to minimize the circuit input referred noise level, which directly adds up to the detector noise and limits the overall performance. The input noise power of the full bridge circuit and the differential amplifier can be calculated by adding the individual noise powers. The noise analysis of the full bridge circuit has been given at the beginning of this section. The noise power of the differential amplifier can be incorporated into this result by adding the power sources since they are independent.

The bridge type readout circuits are suitable for resistive detectors. When the detectors have high resistance values, then the detector noise level will be at a level that is affected negligibly by low noise preamplifiers that can easily be implemented in CMOS technology. For the low resistance detectors such as n-well resistive detectors, the required preamplifier noise level is so low that it is quite difficult to achieve in CMOS technology.

5.3.4 CCBDI Preamplifier

Figure 5.10 shows the simplified schematic of the preamplifier using a constant current bias circuit with a differential transconductance amplifier [58]. This preamplifier circuit is the core of a new circuit called constant current buffered direct injection (CCBDI) structure. Although most of the preamplifier structures used for the resistive detectors use voltage biasing, this new preamplifier structure uses constant current biasing. Constant current biasing is preferred due to its increased responsivity and linearity; however the design of low noise and stable current sources is a difficult task. Since the biasing circuit gives a voltage output, it is necessary to use a transconductance amplifier to convert the detector voltage to current prior to an integrator circuit, which is implemented by connecting an integration capacitance (C_{int}) at the output of the transconductance amplifier. The detector voltage is readout with respect to a reference voltage, which is used to suppress the large amount of DC current at the output to prevent saturation. The residual offset current in the transconductance amplifier output is cancelled by a

constant current source, which improves the dynamic range of the circuit. The integration capacitor is reset to a reference potential periodically before a new integration period starts. The actual implemented capacitor reset circuit is different than a simple reset transistor, and it is designed so as to minimize transient effects of the differential circuit and the offset removal circuit [58].

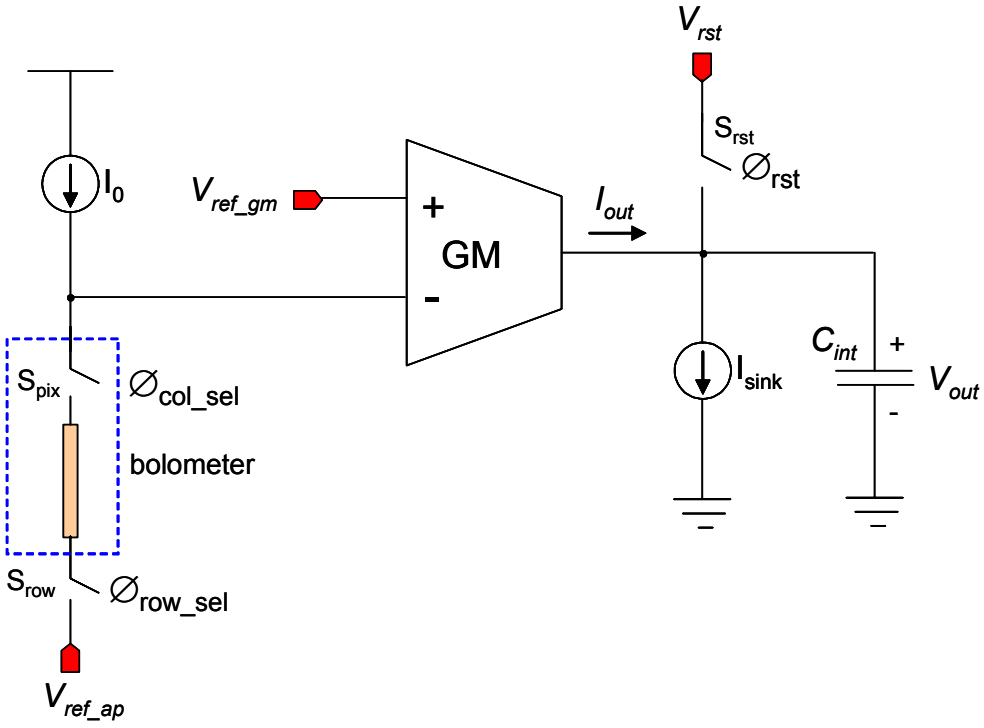


Figure 5.10: Simplified schematic of the preamplifier using a constant current bias circuit with a differential transconductance amplifier [58].

Figure 5.11 shows the schematic of the differential transconductance amplifier used in the constant current preamplifier circuit [58]. The differential transconductance amplifier is composed of five transistors, and three of them are integrated within the pixel electronics implemented in the readout circuit chip under each pixel of the FPA. The differential pair is formed using p-channel MOS transistors (P_1 and P_2), which helps reducing the flicker noise of the circuit.

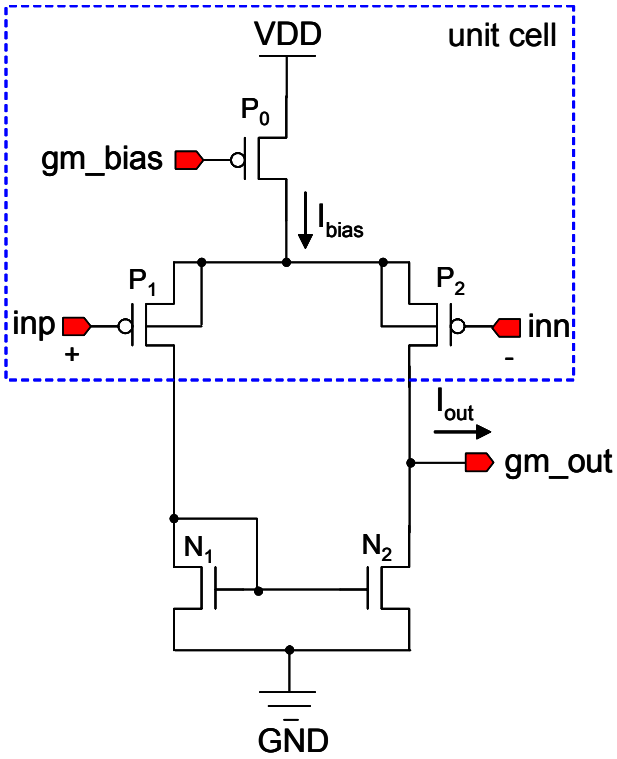


Figure 5.11: Schematic of the differential transconductance amplifier used in the constant current preamplifier circuit [58].

Since the differential circuit in Figure 5.11 is not fully symmetric, there is a mismatch in the drain voltages of the differential pair and n-channel current mirrors (N_1 and N_2), causing a mismatch in the drain currents and mismatch in the transconductance values of the transistors of the differential pair (P_1 and P_2). Figure 5.12 shows the schematic of the improved differential transconductance amplifier used in the CCBDI preamplifier structure. The transconductance mismatch is minimized by using a negative feedback circuit implemented with buffered direct injection circuit, which matches the drain voltages of the transistors in the differential transconductance amplifier; hence the transconductance parameters of the transistors, resulting in a reduced input referred offset voltage. The new circuit is called constant current buffered direct injection (CCBDI) circuit [58]. Figure 5.13 shows the noise model of the CCBDI amplifier circuit.

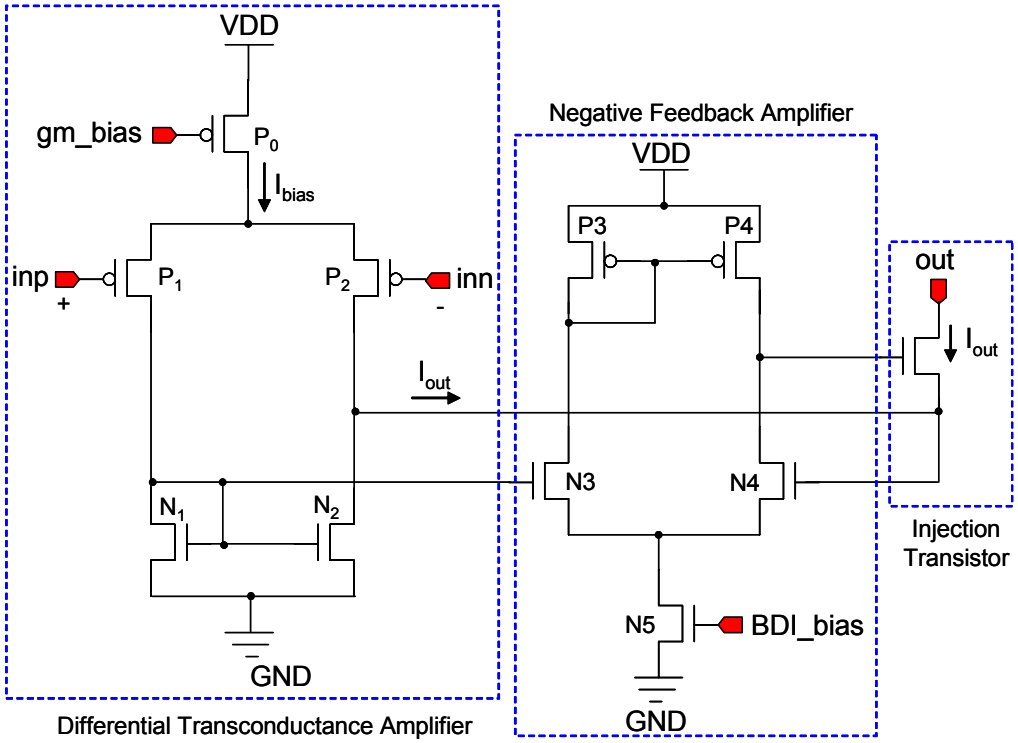


Figure 5.12: Schematic of the improved differential transconductance amplifier used in the CCBDI preamplifier structure [58].

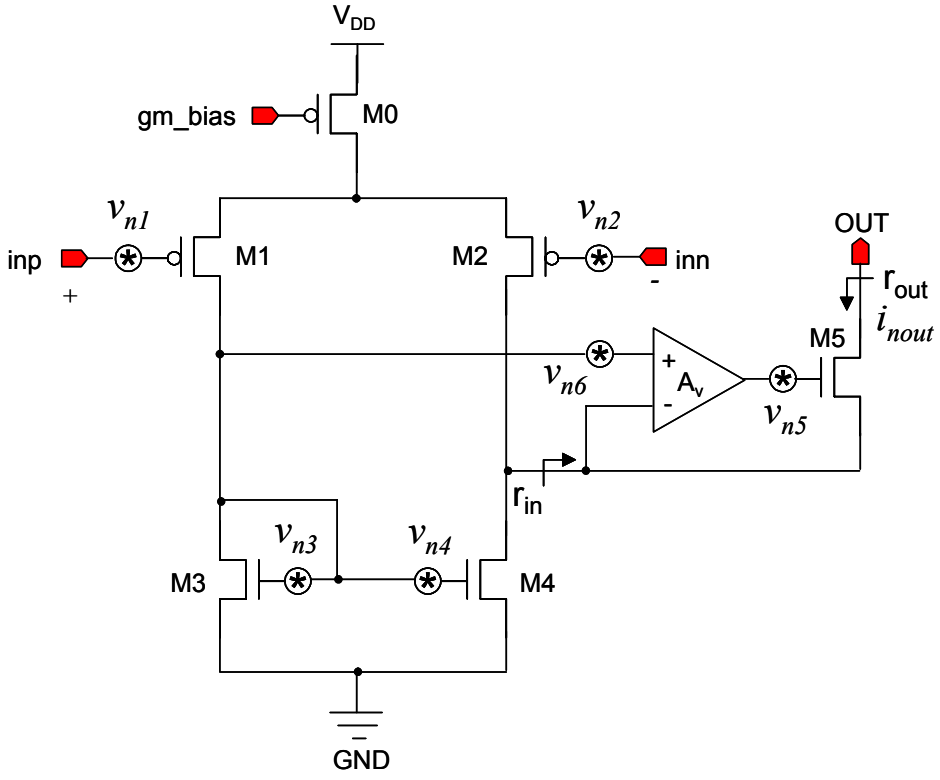


Figure 5.13: Noise model of the CCBDI amplifier circuit.

The output noise current spectral density is approximately given as

$$i_{nout}^2 = g_{mi}^2 \left[v_{n1}^2 + v_{n2}^2 + \left(\frac{g_{m3}}{g_{mi}} \right)^2 \left(v_{n3}^2 + v_{n4}^2 \right) + \left(\frac{g_{d3} + g_{d1}}{g_{mi} A_v} \right)^2 v_{n5}^2 + \left(\frac{g_{d3} + g_{d1}}{g_{mi}} \right)^2 v_{n6}^2 \right] \quad (5.21)$$

where, g_{mi} is the transconductance value of the transistors in the differential pair (*M1* and *M2*), g_{d1} is the output conductance value of the *M1*, g_{m3} is the transconductance value of the transistors in the current mirrors (*M3* and *M4*), g_{d3} is the output conductance value of *M3*, A_v is the voltage gain of the differential amplifier used in the feedback path, v_{n1}-v_{n5} are the gate referred noise voltages of the transistors *M1*-*M5*, and v_{n6} is the input noise of the feedback amplifier. The gate referred noise voltage power spectral density of the transistors is given as [63]

$$v_n^2 = \frac{8kT}{3g_m} + \frac{K}{C_{ox}WL}\frac{1}{f} \quad (5.22)$$

where, k is the Boltzmann constant, T is the temperature in Kelvin, g_m is the transconductance of the transistor, K is the 1/f noise scaling factor for the transistors and is different for n-channel and p-channel transistors, W and L are the width and length of the transistors, and f is the frequency in Hz. The expression in the square brackets in Equation 5.18 is equal to the input referred squared noise voltage spectral density, and it is dominated mainly by the gate referred noise voltages of the input differential pair. The gate referred noise voltage of the input transistors is minimized by increasing the device transconductance (g_{mi}) and by increasing the gate area (WL). To decrease the noise contribution of the current mirror transistors, their transconductance value should be adjusted to be much lower than that of the differential pair. Increasing the transconductance of the input differential pair also helps to reduce the noise contribution of the feedback amplifier and the injection transistor (*M5*). Increasing the gain of the feedback amplifier (A_v) decreases the noise contribution of the injection transistor. Since the opamp noise contribution minimized by the high output resistance of the differential transconductance circuit, the device dimensions in the feedback transistor can be selected much smaller as

compared to the differential transconductance circuit. Decreasing the preamplifier noise is only possible when the gate referred noise voltages of the differential pair are minimized. The thermal noise component is minimized by selecting large W/L values for a given bias level. Furthermore, the 1/*f* noise components can be minimized by selecting the gate area as large as possible. Since these two conditions require large device area, it is not possible to integrate the preamplifier or the differential pair within the pixel area when low-noise operation is required. However, in the previously reported preamplifier [58], the differential pair and the bias transistor are integrated in a 50 μm × 50 μm area under the pixels in the detector area of the designed readout chip, and only the feedback amplifier and other support electronics are moved outside the pixel area. Furthermore, p-channel transistors are used as input differential pair, which would generate higher thermal input noise at a given bias current level as compared to the n-channel transistors. Since the available device area is very small, the reduction in the 1/*f* noise due to the p-channel devices may not be so advantageous. Based on the noise analysis, it is clear that integrating the preamplifier or the critical transistors, such as that of differential pair, within the pixel area increases the input referred noise well above acceptable levels.

There are four main short comings of the CCBDI circuit: 1) The constant current bias of the detector introduces high noise due to the high detector resistance and large detector bias level. The resistive detectors have generally high resistance values above 10 kΩ, which increases the noise contribution of the biasing circuit. When the detector has high resistance, its voltage noise will also be higher, increasing the noise level at the preamplifier input terminal. 2) The input transistors of the preamplifier are p-channel MOS transistors, whose input referred noise increases as the device area and transconductance value are reduced. Since the differential pair and the biasing transistor are implemented in the unit cell, the device area is reduced considerably; therefore both the input referred thermal noise and flicker noise components increase dramatically. Furthermore, since the preamplifiers are used in each unit cell, the power requirement may increase drastically unless they are turned off when the corresponding pixels are not addressed. The turning on and off the preamplifier may cause transients effects which may cause saturation at the

integrator. To prevent this, integration period can be shortened to allow sufficient time for the transient signals to decay. The disadvantage of long transients is that bandwidth and noise level increases as the integration time is reduced. 3) The integration capacitance is directly connected to a high impedance node. The reset operation may cause large transients in the output current. Although, a special circuit is designed to minimize these transients, it is not possible to cancel nonlinearities induced by the finite output resistance, since the output voltage is not kept constant through out the complete operation. 4) The operation is not a true differential operation in that the input reference voltage is not generated using a reference detector, and this complicates the uniformity correction issues. Although the noise levels of the proposed preamplifier is not mentioned at all, considering these side effects it seems very difficult to construct a readout circuit with sufficiently low noise level, especially for the resistive microbolometer detector arrays, which was given to be the application area of the fabricated 64 × 64 test circuit [58]. The proposed CCBDI preamplifier can be used for low resistance detectors, such as the diode type microbolometers, provided that design is optimized in terms of noise. The next section first gives the details on the preamplifier used in the 320 × 240 SOI diode FPA. Then, it introduces the readout circuit used in the 64 × 64 and 128 × 128 n-well diode FPAs.

5.4 Preamplifiers for the Diode Type Microbolometers

Diode type uncooled microbolometers use forward biased p-n junction diodes instead of high TCR resistors as temperature sensitive elements. Since the I-V characteristics of the diode type detectors are exponential, readout circuits that read the detector current upon voltage bias are not suitable [38]. In the constant voltage biasing, a small variation in the bias voltage may cause a large variation in the detector current, increasing the non-uniformity of the array. The bridge type circuits are also not practical due to the non-linear I-V characteristics of the diode type detectors. Furthermore, the diode type detectors have both less temperature sensitivity and reduced impedance compared to the resistive and capacitive devices. Therefore, the noise level of the corresponding preamplifier should be very low,

which is quite difficult to achieve in CMOS technology. There are two diode FPAs reported in the literature: SOI diode and n-well diode FPAs. The first FPA uses gate modulation integration (GMI) [32] circuit, and second FPA uses differential buffered injection-capacitance transimpedance-amplifier (DBI-CTIA) circuit [39-42].

5.4.1 GMI Preamplifier

Figure 5.14 shows the schematic of the preamplifier circuit used for the 320 × 240 SOI diode FPA [28]. This preamplifier structure is called gate modulation integration (GMI) circuit [64]. The preamplifier circuit is composed of a constant current source (M_1), one amplifier transistor (M_2), one reset transistor (M_3), and an integration capacitor (C_{int}), which is simple enough to be implemented separately for each column in the FPA. In fact, the 320 × 240 FPA has 240 parallel readout channels [28].

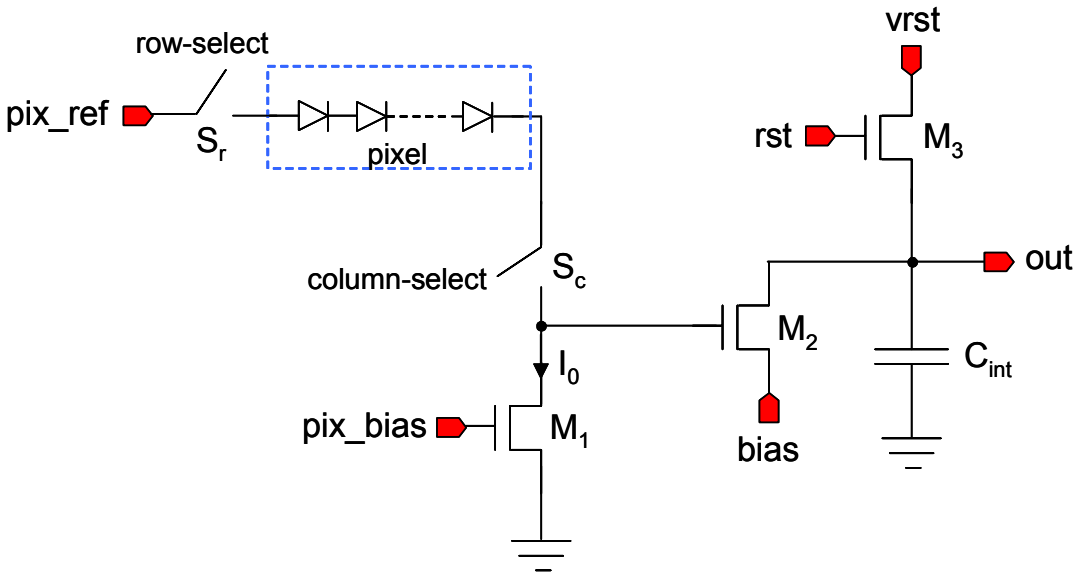


Figure 5.14: Schematic view of the preamplifier used in the 320 × 240 SOI diode FPA [28]. This preamplifier structure is called gate modulation integration (GMI) circuit.

The operation of the gate modulation integration circuit can be explained as follows: The absorbed infrared radiation increases the temperature of the pixel, causing a decrease in the forward voltage of the diode pixel, which is biased by a

constant current source. The anode of the diode is connected to a reference potential, and the potential of the cathode increases with the decrease in the diode forward voltage due to the increase in the pixel temperature. The cathode potential is connected to the gate of M_2, which converts the voltage variation at its gate to current integrated across an integration capacitor (C_{int}). The integration capacitor is reset periodically by M_3 to a reset voltage, and the capacitor is discharged by the drain current of the M_2.

Figure 5.15 shows the noise model of the series diodes. In this model, r_d is the dynamic resistance of the diode at the given bias current, and i_d is the noise current of the diode. The output resistance of the series diodes (r_d) increases linearly with the number of series diodes (n) in the pixel. On the other hand, the noise voltage of each diode is added in terms of power since they are uncorrelated, and the total noise voltage increases by a factor of √n; therefore, the noise current is scaled by the reciprocal of √n.

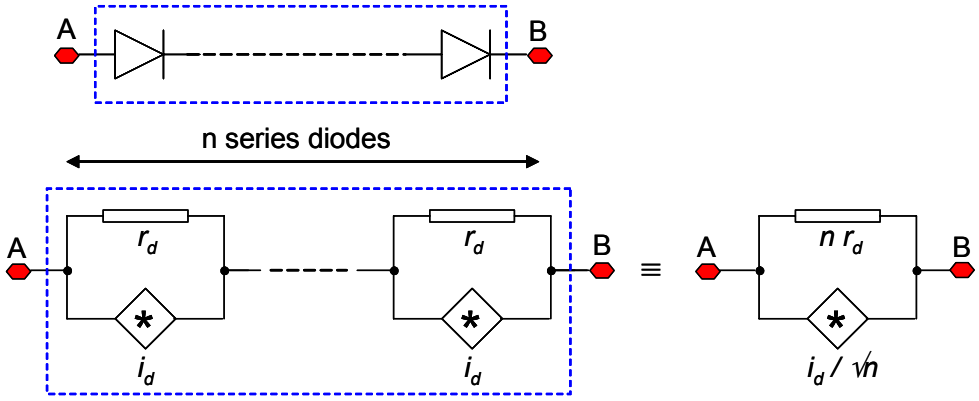


Figure 5.15: Noise model of the series diodes.

The temperature sensitivity of the pixel increases linearly with the number of series diodes (n) in the pixel. For the pixels in the 320 × 240 SOI FPA, the temperature sensitivity of the pixel is reported as -9.7 mV/K at 10 µA bias current [28]. This sensitivity value is about 5 times larger than what is achieved using a single diode in the pixel at a bias level of 20 µA [39]. In the actual implementation, the increase in the number of series diodes limits the junction area available for a

single pixel. Based on the given data, it is calculated that the number of series diodes in the 320 × 240 SOI diode FPA pixels is 8; therefore, the diode area is reduced considerably to be able to fit into a 40 μm × 40 μm diode area. The decrease in the junction area decreases the reverse saturation current of the diode, which increases the required forward voltage for a given bias current. As explained in Chapter 4, the increase in the diode forward voltage decreases the temperature sensitivity of the pixel. Furthermore, as the diode size decreases, the contribution of the flicker noise will be more important, and it can not be neglected as compared to the shot noise component [65]. In fact, the flicker noise component of the SOI diodes is reported to be higher than their shot noise component [28], mainly due to the reduced device area, and possibly due to reduced junction depth in SOI process.

Since the infrared induced signal level improves linearly with the number of series diodes (n), and the noise voltage adds in quadrature, the signal-to-noise ratio of the pixel (SNR_{pixel}) improves by a factor of √n, which is the major advantage of using multiples series diodes in the pixel. Assuming the pixel thermal time constant is small enough to cause negligible loss in the detector signal, and assuming that the flicker noise component in the diode noise current is negligible, the pixel SNR value (SNR_{pixel}) is given as

$$SNR_{pixel} = \sqrt{n}\,\frac{|dV_d / dT|\,\eta / G_{th}}{i_d r_d \sqrt{\Delta f}} \tag{5.23}$$

where, n is the number of series diodes in the pixel, the $|dV_d/dT|$ is the temperature sensitivity of the diode forward voltage, η is the absorption coefficient, G_{th} is the thermal conductance of the pixel, i_d is the pixel noise current spectral density, r_d is the dynamic resistance of a single diode, and Δf is the electrical bandwidth.

The total input noise power spectral density of the buffered gate modulation readout circuit is composed of the detector noise, noise of the constant current bias transistor, and gate referred noise of the modulation transistor. The total input noise power spectral density of the buffered gate modulation readout circuit is given as

$$v_n^2 = \left(\underbrace{\frac{1}{n}\left(2qI_0 + \frac{K_{fd} I_0^a}{f}\right)}_{DIODE} + \underbrace{g_{m1}^2 \left(\frac{8kT}{3g_{m1}} + \frac{K_f}{C_{ox}(WL)_1 f}\right)}_{BIAS\ TRANSISTOR} \right) \left(\underbrace{g_{d1} + \frac{qI_0}{nkT}}_{\substack{BIAS\ CIRCUIT \\ OUTPUT\ CONDUCTANCE}} \right)^{-2} + \underbrace{\frac{8kT}{3g_{m2}} + \frac{K_f}{C_{ox}(WL)_2 f}}_{MODULATION\ TRANSISTOR} \quad (5.24)$$

where, q is the electron charge, I_0 is the pixel bias current, n is the number of the series diodes in the pixel, K_{fd} is the flicker noise scaling factor for the diode, a is the exponent related with the bias dependence of the flicker noise in the diode ($1 \le a \le 2$), f is the frequency, k is the Boltzmann constant, T is the temperature, g_{m1} and g_{m2} are the transconductance of the constant current bias transistor (M_1) and modulation transistor (M_2), K_f is the flicker noise scaling factor of the transistors, C_{ox} is the unit gate capacitance, $(WL)_1$ and $(WL)_2$ are the gate area of M_1 and M_2, f is the frequency, and g_{d1} is the output conductance of M_1.

To achieve low-noise operation, an optimization is necessary both for the detector bias condition, transistor dimensions, and transistor biasing. High detector bias increases the shot noise current related with the square root of the bias current. However, the corresponding noise voltage decreases inversely proportional to the square root of the detector bias current; therefore, detector noise voltage decreases as the detector bias is increased. At high bias levels flicker noise also contributes to the overall noise voltage. In order to reduce the noise contribution of the bias transistor, its transconductance value (g_{m1}) should be decreased. The g_{m1} value can be decreased by increasing the channel length, which decreases both the thermal and flicker noise components of the biasing transistor. Since the flicker noise component of the output noise current of the bias transistor inversely proportional to the square of its channel length, decreasing the channel length is an effective way to decrease the noise of the bias circuit [63]. Since the detector has a lower output resistance as compared to the bias transistor, the overall noise voltage will be small. To minimize the noise contribution of the modulation transistor at the detector input, its transconductance should be maximized. This is achieved by biasing the modulation transistor at a relatively high level, and the W/L ratio should be increased, while preserving a large gate area (WL) to keep its flicker noise at a low level. When the SNR level of the detector is low, then the modulation transistor would require large

implementation area, making it impractical assigning separate readout channels or each column in the FPA. In the SOI diode the series connection of the diodes improves the SNR and relaxes the noise requirements for the gate modulation circuit, making it possible to assign one readout channel per FPA column. The detector noise voltage in the 320 × 240 SOI FPA is 6.2 μV, and the input referred noise voltage of the readout circuit is 4.7 μV at 60 fps scanning rate. The measured NETD value of the fabricated FPA is reported to be 120 mK for an f/1 optics [28].

5.4.2 DBI-CTIA Preamplifier

The p^+-active/n-well diode type detectors has a single diode in the pixel. Therefore, the temperature sensitivity of the detectors is about 3 times lower as compared to the SOI diode type pixels with multiple series diodes in it. Assuming that all the other parameters are the same, the input referred noise of the preamplifier of the n-well diodes should have about 3 times lower noise voltage as compared to the buffered gate modulation preamplifier designed for the SOI diodes. This requires higher bias levels and larger transistor dimensions for the input transistors to reduce the thermal and flicker noise components, making it impractical to assign separate readout channels for each column of the n-well diode FPAs. Figure 5.16 shows the simplified schematic of the preamplifier used in the 64 × 64 and 128 × 128 n-well diode type FPAs [41-42]. The preamplifier is composed of a detector biasing stage, a low noise differential transconductance amplifier, an offset current removal circuitry, and a capacitive transimpedance amplifier. This preamplifier is the combination of the CCBDI and CTIA structures, and it is called differential buffered injection-capacitance transimpedance amplifier (DBI-CTIA).

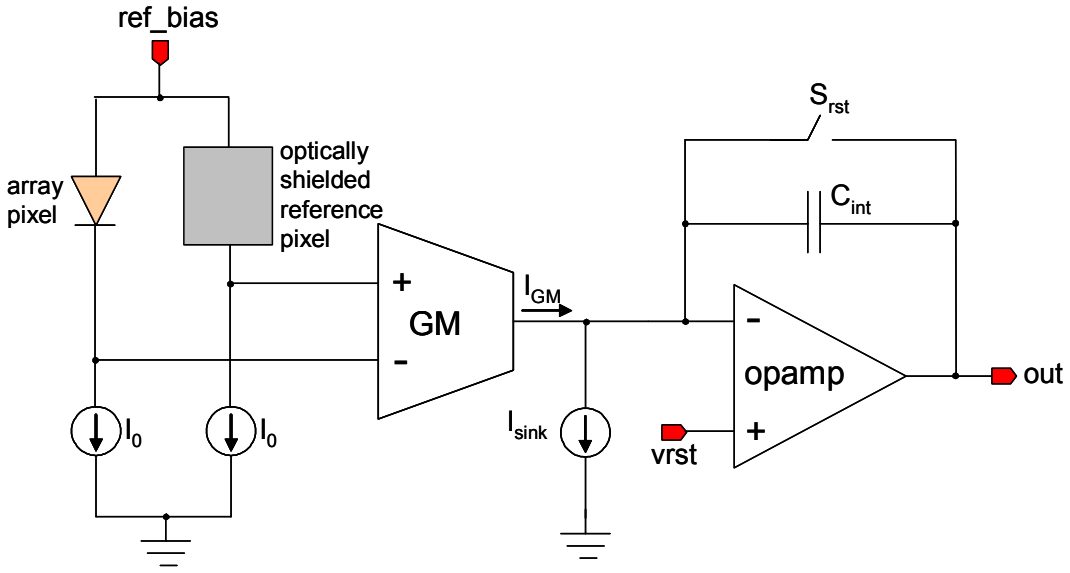


Figure 5.16: Simplified schematic of the preamplifier used in the 64 × 64 and 128 × 128 n-well diode type FPAs [41-42]. This preamplifier is the combination of the CCBDI and CTIA structures, and it is called differential buffered injection-capacitance transimpedance amplifier (DBI-CTIA).

The n-well microbolometer is biased using a constant current source. The change in the detector voltage is read out differentially with respect to an identical but optically shielded reference pixel biased in the same manner. The use of an optically shielded reference detector cancels the effects of process variations and makes the reading insensitive to changes in the operating temperature. The low-noise differential transconductance amplifier converts the differential detector voltage to a current signal, suppressing the common signal considerably. The residual offsets are cancelled by adjusting the current level subtracted from the transconductance amplifier output prior to integration. The reset integrator limits the bandwidth of the signal and provides sufficient gain enabling further post processing of the signal with negligible increase in the input referred noise level.

Since the resistance of the n-well microbolometer is very small as compared to the output resistance of the current sources, the noise of the differential detector output is dominated by the noise voltage of the array and reference pixels. The low-noise differential transconductance amplifier is implemented using MOS transistors providing almost zero loading within the designed bandwidth. The output

resistance of the differential transconductance amplifier is high enough to achieve high current injection efficiency into the integration capacitance. In fact, injection efficiency is further improved by the use of a CTIA circuit, which provides zero input resistance, relaxing the requirement on the output impedance of the transconductance amplifier. In a typical design, the output resistance of the transconductance amplifier is high enough to suppress the noise contribution to the detector input terminals due to the opamp input noise used in the CTIA circuit. Therefore, the input noise level of the preamplifier is minimized by tuning other circuit parameters, especially for the input transistors in the differential transconductance amplifier. To achieve low input noise, the input noise of the transistors is minimized by using high transconductance values and large device areas for the input transistors. The design details of the preamplifier structure are given in Chapter VI and VII. The designed readout circuit for the 64 × 64 n-well diode FPA has a measured input referred noise of 0.48 μV for a 4 kHz bandwidth at 30 fps resulting an expected NETD value of 0.8 K for an f/1 optics. The readout circuit for the 128 × 128 n-well diode FPA has a measured input referred noise of 0.76 μV for an 8 kHz bandwidth at 30 fps resulting an expected NETD value of 1 K for an f/1 optics. Both readout circuits achieved input referred noise levels about an order of magnitude lower as previously designed preamplifiers. The design details of the preamplifier circuits used in the 64 × 64 and 128 × 128 FPAs are given in Chapter VI and VII, respectively. The following section explains the readout circuits used for the pyroelectric uncooled infrared detectors.

5.5 Readout Architecture for the Uncooled Detector Arrays

Figure 5.17 shows the block diagram of the readout architecture used for most of the uncooled infrared detector arrays. The readout circuit is composed of a row and column multiplexers controlled by a digital timing circuit. The detector signals are amplified and band limited by the analog readout circuit.

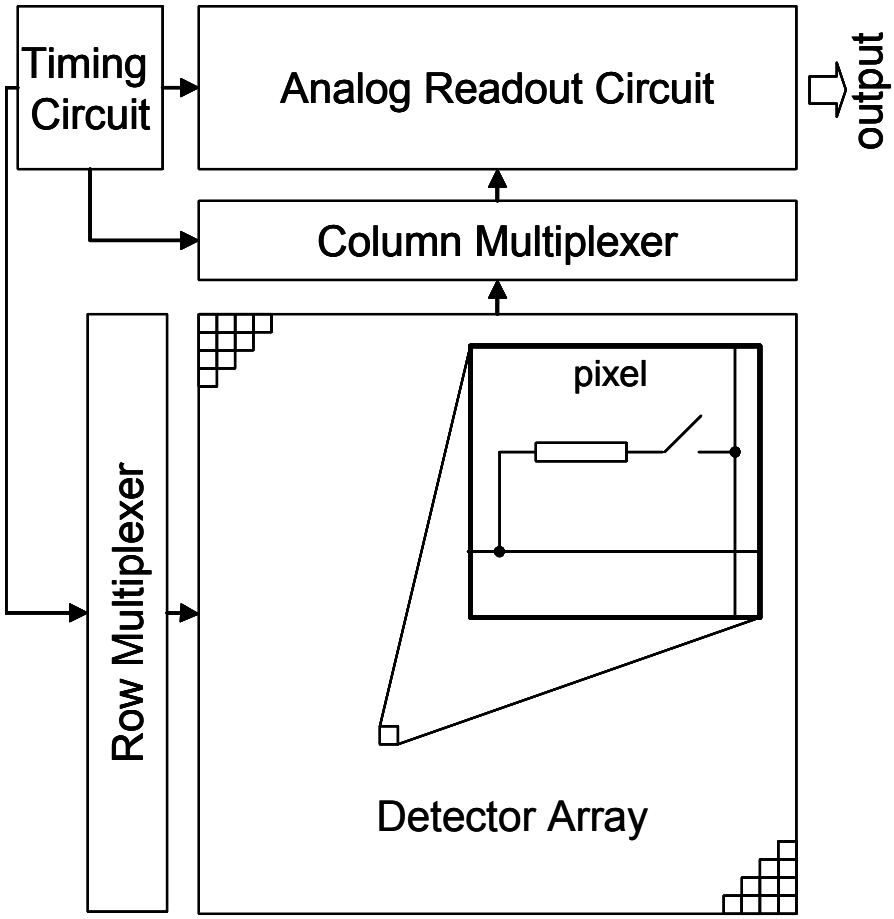


Figure 5.17: Block diagram of the readout circuit used for most of the uncooled infrared detector arrays.

The pixels in the detector array are addressed sequentially by the row and column multiplexers controlled by the digital timing circuit. The selection of an array pixel is achieved by turning on the corresponding switch integrated in the pixel or under the pixel. The position of the pixel switch depends very much on the selected detector fabrication technology. A common approach is to implement the detector array on top a separately fabricated CMOS readout circuit. In this case, the pixel switches and the required routing lines are integrated under the detector array. Other required circuitry, such as the row and column multiplexers and the analog readout circuits, are integrated outside the detector area. In the readout circuit of uncooled detector arrays, the detector bias is applied during a short period of time. This biasing scheme is called pulsed-biasing, and it prevents any possible damage to the pixels due to excessive joule heating effect that occurs in the continuously biased

case. The initial transient during pixel selection and bias application introduce considerable noise, therefore not all the portion of the pixel selection time is used to process the detector signals. To avoid noisy operation, it is necessary to wait for a sufficient time so that noisy transient signals decay down to an acceptable level [14].

The readout circuit can be designed using fully-serial or parallel readout architecture. In the fully-serial readout architecture, only a single pixel is selected at a given time. In this case, one readout circuit is sufficient for the complete array, occupying less silicon area. Furthermore, compensation for the offset and gain errors of the circuit is simple due to reduced number of circuit blocks. However, the pixel selection time for a given scanning rate decreases in the fully serial readout architecture as the array format increases. Furthermore, the readout will be noisy due to the excessively wide electrical bandwidth. However, in the parallel readout architecture, more than one pixel can be selected for much longer time; therefore, the electrical bandwidth decreases reducing the noise level of the readout circuit. On the other hand, the use of parallel operating readout circuits causes fixed pattern noise in the final image output due to the offset and gain errors in the analog readout channels. Since the number of error sources is increased with increased number of parallel readout channels, the correction of these errors becomes more difficult as compared to the fully-serial readout architecture [14].

The readout circuits were implemented initially using bipolar transistors in BiCMOS technologies due for improved noise performances [66]. However, the readout circuits of modern detector arrays are implemented using CMOS technology due to the higher integration density of the CMOS technology at lower fabrication cost. The main disadvantage of CMOS circuits is its increased noise level compared to bipolar technologies, since the transconductance value of MOS transistors are lower than that of bipolar transistors, and $1/f$ noise is higher for the MOS transistors [63]. To achieve low noise preamplifiers in the CMOS, the device dimensions are increased to suppress the $1/f$ noise, which increases the required silicon area for a single readout channel. Depending on the noise density of the detector, it may not be feasible to assign a separate readout channels for each array column, since the

increase in the 1/f noise component may suppress the expected decrease in the overall noise due to reduced bandwidth. Furthermore, it may be difficult to integrate the channel readout circuitry within a base width equal to that of the pixel pitch, which is less than 50 μm for modern detector arrays [11].

5.6 Uniformity Correction

As the array size increases, the variations of pixel voltage due to process variations or fluctuations in the operating temperature becomes so high that they limit the array performance, causing loss in the dynamic range or saturation at the preamplifier output. To avoid these problems, uniformity correction is applied where the bias points of the array detectors are adjusted so as to cancel the above mentioned variations. After the array fabrication, the pixel non-uniformity is measured for each fabricated FPA. Using the data required bias voltages are calculated to cancel the non-uniformity errors. Furthermore, the pixels with very low responsivity or very high responsivity are marked as defective pixels, and during scanning the defective pixels are replaced with the properly operating neighboring pixels. The FPA uniformity measurement is repeated for different temperatures, so that variation in the operating temperature can be compensated effectively [23, 67]. Performing the uniformity correction at more than one temperature point relaxes the requirements for temperature stabilization. To be able to perform uniformity correction on pixel level, on-chip digital-to-analog data converters are required. These on-chip data converters are used for bias adjustment prior to preamplifiers and integrators. If they are not used, the preamplifiers should be designed with very high dynamic range which is impractical and consumes large silicon area. There are commercial uncooled FPAs which have on-chip 6-bit [21] and 14-bit [23] digital-to-analog converters which are integrated in each readout channel performing real-time uniformity correction.

As compared to the resistive microbolometer FPAs, the uniformity of the p^+-active/n-well diode FPAs are very good due to the mature CMOS fabrication technology. However, overall pixel uniformity is affected by the resistive voltage

drops along the FPA routing lines. Compensation of the resistive voltage drop by pixel level bias adjustment is not practical since it would require very high resolution parallel digital-to-analog data converters. The use of external data digital-to-analog converters is not preferred since the input voltage range of external converters are much higher than the allowed bias range, unnecessarily increasing the required converter resolution. Therefore, on-chip digital-to-analog data converters are required. However, the design and integration of digital-to-analog data converters into narrow pitch allowed for the analog channel electronics is a difficult task which requires many prototype fabrications that would cause deviation from the scope of this study.

The uniformity problem of the p^+-active/n-well diode FPAs are solved in detector and preamplifier level by using an identical reference row and improved FPA routing [41, 42]. By reading the pixel voltages in the array differentially with respect to the pixel voltages in the reference row, the effect of the resistive voltage drops along the routing lines in the FPA and the effect of operating temperature variations are minimized considerably, decreasing the peak-to-peak pixel variation by an order of magnitude. The self-heating effect is also compensated partially by the reference detectors, and the residual offsets are canceled by an analog on-chip offset removal circuitry. The design details of the fabricated p^+-active/n-well diode microbolometer FPAs are given in the following chapters together with their on-chip integrated readout circuitry.

5.7 Summary and Conclusions

This chapter gives the examples of various preamplifiers that are used for the resistive and diode type microbolometer detectors and arrays. The preamplifiers circuits used for the resistive microbolometers are listed as follows: current direct injection (BCDI) circuit, capacitance transimpedance amplifier (CTIA), Wheatstone bridge based preamplifier, and constant current buffered direct injection (CCBDI) circuit. The preamplifiers used for the diode type microbolometers are as follows:

gate modulation integration (GMI) and differential buffered injection-capacitance transimpedance amplifier (DBI-CTIA) circuits.

The BCDI circuit is implemented in a bipolar technology using npn and pnp bipolar transistors and a simple integration capacitance, providing very low noise operation. The preamplifier removes large portion of the DC bias current prior to integration using a load resistor biased in the same way as the detector. Furthermore, the effect of self-heating is cancelled by adjusting the bias level of the load resistor. The preamplifier is designed for a 320 × 240 FPA, and since the preamplifier is simple enough, it is integrated on each column of the array. The input referred readout noise voltage is 4.4 μV, providing an estimated NETD value is 34 mK with f/1 optics for resistive detectors having a TCR value of 2 % / K [61].

The CTIA preamplifier is commonly used CMOS based readout circuitry together with direct injection biasing transistors with an identical and optically shielded reference detector biasing circuitry to cancel the DC portion of the detector current. The reported NETD value for the FPAs that use CTIA circuit are 80 mK for an 160 × 128 FPA [23] and 70 mK for a 320 × 240 FPA [25], where both of them use detectors with TCR values above 2 % / K.

Wheatstone bridge based readout circuits are implemented using a full-bridge detector biasing circuit followed by a differential preamplifier, which cancels large DC portion of the detector voltage, and compensates for the process variations and fluctuations in the operating temperature [21]. Furthermore, the use optically shielded reference detector is used to cancel the effect of self-heating.

The CCBDI preamplifier uses a constant current biasing followed by a differential transconductance amplifier and simple capacitor integration circuit [58]. The preamplifiers are implemented in pixel level, making low noise operation impossible. Furthermore, constant current biasing is used, which will introduce relatively higher noise as compared to the constant voltage biasing case. Finally, the preamplifier does not provide a true differential operation since there is no identical

and optically shielded reference detector integrated in the FPA. However, it should be mentioned the differential transconductance amplifiers can be used for other type of uncooled microbolometers that have low resistance and requires constant current biasing, such as the diode type microbolometers.

The readout circuits of the diode type microbolometers use constant current biasing where the detector output is in the form of voltage. The detector voltage is converted to current by a transconductance amplifier followed by an integrator circuit. There are two different readouts developed for the uncooled diode type detectors: gate modulation integration (GMI) and differential buffered injection-capacitance transimpedance amplifier (DBI-CTIA) circuits. The GMI circuit uses gate modulation transistor followed by a simple capacitor integrator, and it is used for the 320 × 240 SOI diode FPA where the array pixels include multiple series diodes to improve SNR of the detector [28]. Since the proposed GMI readout circuit is relatively simple, it is possible to assign a separate readout channel for each column in the FPA. The input referred noise voltage of the designed readout circuit is reported as 4.7 μV, providing an NETD value of 120 mK with f/1 optics using a pixel with multiple series diodes with an overall pixel temperature sensitivity of -9.8 mV/K at 10 μA bias [28]. Since the GMI circuit does not operate differentially, it is affected from process variations and temperature fluctuations. In addition, the integrated current level also includes the DC current of the modulation transistor, requiring either large integration capacitors or short integration periods. The former requires large implementation area, whereas the latter increases the electrical bandwidth and overall noise. Furthermore, the use of simple integrator causes deviations from the ideal integrator characteristics for longer integration periods.

A new preamplifier circuit is designed for the p^+-active/n-well diode microbolometers, and this new circuit combines GMI and CCBDI with CTIA preamplifiers. The constant current biasing of the GMI and CCBDI circuit is used to bias the p^+-active/n-well diode type microbolometers. Since there is a single diode in the pixel, the SNR of the pixel is lower as compared to multiple SOI diodes, therefore, it is necessary to minimize the input referred noise of the preamplifier.

Different than the CCBDI structure, the preamplifier is taken out of the pixels and placed outside the FPA, where the device sizes can be increased to provide lower input noise. In addition, true differential operation is performed using identical and optically shielded reference pixels. The use of differential circuit cancels the effects of process variations and fluctuations in the operating temperature relaxing the requirements for the temperature stabilizers. Finally, the residual offsets are canceled by an analog on-chip offset removal circuit prior to integration. The required integration is performed using CTIA circuit, which has zero input impedance, and provides stable operating point for the output stage of the transconductance amplifier minimizing the transients during scanning. Longer integration periods can be used by changing the integration capacitance using a set of digitally controlled capacitors. The designed readout circuit for the 64 × 64 n-well diode FPA has a measured input referred noise of 0.48 μV for a 4 kHz bandwidth at 30 fps resulting an expected NETD value of 0.8 K for an f/1 optics. The readout circuit for the 128 × 128 n-well diode FPA has a measured input referred noise of 0.76 μV for an 8 kHz bandwidth at 30 fps resulting an expected NETD value of 1 K for an f/1 optics. Both readout circuits achieved input referred noise levels about an order of magnitude lower than that of the previously designed preamplifiers. The design details of the preamplifier circuits used in the p^+-active/n-well diode FPAs are presented in the following chapters.

CHAPTER VI

6 THE 64 × 64 UNCOOLED INFRARED FPA

This chapter presents the design details of the 64 × 64 uncooled infrared FPA chip. The 64 × 64 FPA is based on the p^+-active/n-well diode microbolometer detectors. The 64 × 64 FPA has 4096 diode microbolometer pixels scanned by a monolithically integrated readout circuit. Pixel selection in the FPA is performed using row and column multiplexers controlled by an on-chip digital scanning control circuit. The selected pixels are biased and their signals are band-limited and amplified by on-chip low-noise preamplifier circuits. The FPA chip has a 16-channel parallel readout circuitry, and each readout channel is composed of a detector biasing circuit, a low-noise differential transconductance amplifier, a switched capacitor integrator (SCI), a correlated double sampling (CDS) circuit, a sample-and-hold (S/H) circuit, and a channel output multiplexer. The 64 × 64 FPA chip is fabricated using a standard 0.35 μm CMOS process followed by simple post-CMOS bulk micromachining that does not require any critical lithography or complicated deposition steps; therefore, the cost of the uncooled FPA chips is almost equal to the CMOS chip cost.

This chapter is organized as follows: Section 6.1 introduces the detector array structure of the 64 × 64 FPA, and analyzes the effect of the FPA routing on the array uniformity. Section 6.2 demonstrates the effect of FPA routing on infrared image with the help of MATLAB simulations. Section 6.3 gives the reference array

used in the 64 × 64 FPA. Section 6.4 explains the parallel readout architecture of the 64 × 64 FPA chip. Section 6.5 presents the design details of the analog circuit blocks, including the low-noise differential transconductance circuit, SCI, CDS, and S/H circuits. Section 6.6 explains the digital scanning circuitry composed of a digital timing circuit and several shift registers to address the rows, columns, and analog readout channels in the FPA. Section 6.7 presents the integration of circuit modules and gives the floor plan and overall layout of the 64 × 64 FPA chip. Finally, Section 6.8 summarizes the design of the 64 × 64 FPA chip.

6.1 Array Structure

Figure 6.1 shows the simplified schematics of the 64 × 64 FPA. For simplicity it is assumed that the FPA is scanned using a 64 channel readout circuit, and at a given time, all the row pixels in a row selected by the row switches (S_0 - S_{63}) are biased and read out in parallel.

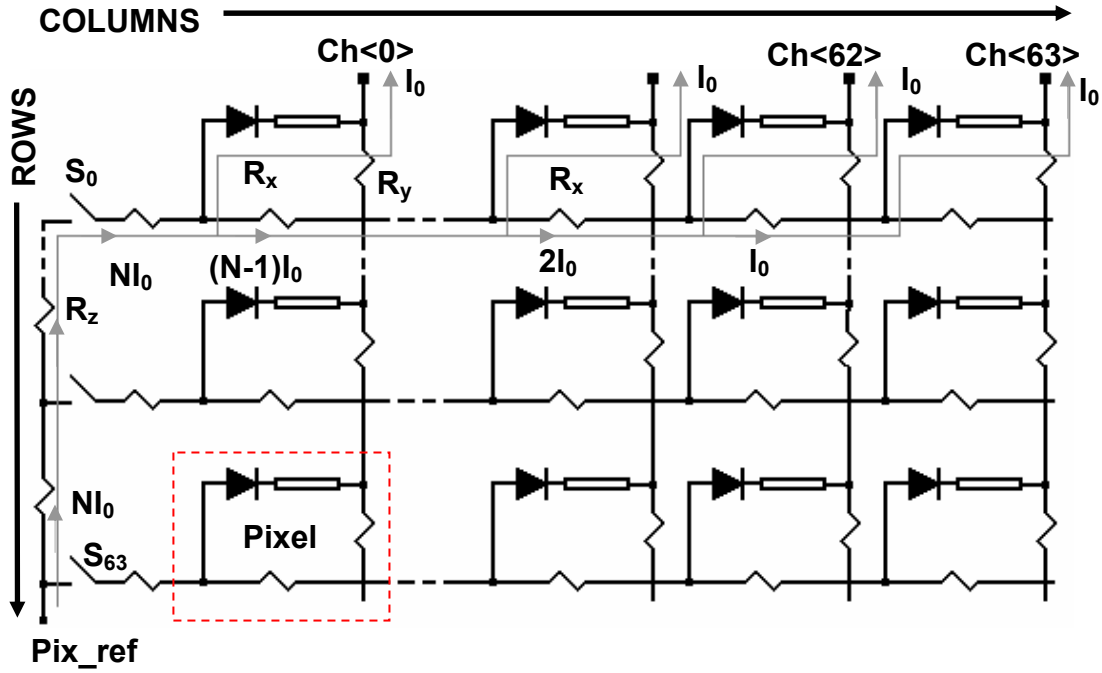


Figure 6.1: Simplified schematics of the 64 × 64 FPA.

In Figure 6.1, R_x and R_y are the horizontal and vertical routing resistances in the FPA associated for a single pixel. R_z is the vertical routing resistance value of the routing line associated with a single row implemented, which is implemented outside the pixel area. Corresponding resistive voltage drops cause a gradient in the multiplexed pixel voltages. The R_x, R_y, and R_z values for the 64 × 64 FPA are 1.60 Ω, 2.13 Ω, and 1.06 Ω, respectively. The array pixels are biased at 10 μA; therefore, the vertical voltage drop along R_y is 21.3 μV. Since the current level is changing along a row, corresponding voltage drops also vary being maximum at the left most pixel (1024 μV), and being minimum at the right most pixel (16 μV) assuming that all the pixels in a selected row are biased in parallel. The FPA output voltage (V_{FPA}) for a pixel at the m^{th} row and n^{th} column in the array is given as

$$V_{FPA}(m,n) = V_{pix\_ref} - V_{pix}(m,n) - NI_0(N-1-m)R_z - mI_0R_y - I_0R_x\sum_{k=0}^{n}(N-k) \quad (6.1)$$

where, V_{pix_ref} is the array reference bias voltage, $V_{pix}(m,n)$ is the selected pixel voltage, N is the number of rows and columns of the array, R_x and R_y are horizontal and vertical routing resistance associated with each pixel, R_z is the routing resistance associated for each row outside the pixel area. The last summation term represents the accumulated voltage drop across the horizontal routing line in a row due to the varying branch current values due to the multiple bias sources associated for each column in the simplified array schematic.

Since the row switches are placed outside the FPA, corresponding routing resistance (R_z) can be made smaller by increasing the width of the corresponding metal routing layer. Furthermore, it is also possible to minimize variations along the vertical direction if increase in the current magnitude flowing through R_z is compensated by a proportional decrease in the routing resistance with the help of identical multiple parallel routing lines. In that case, vertical voltage drop can be made constant, and it can be made independent of the selected row position in the array. However, compensation for the horizontal voltage drops is not so easy due to the parallel readout architecture requiring multiple bias sources, which creates a varying current level in the horizontal routing lines of the FPA. Since there are very

limited space between the pixels, complex routing schemes are not possible, which requires other means of compensation. This problem is solved with the help of reference pixels in the 128 × 128 FPA as explained in Chapter VII.

The variation in the FPA output voltages due to the resistive voltage drops is slightly more complicated in the actual fabricated array, since in the 64 × 64 FPA the readout circuit is composed of 16 channels shared by the 4 pixel columns, causing a position dependent R_x and R_y values in the array. The FPA output voltage (V_{FPA}) for a pixel at the m^{th} row and n^{th} column in the actual array is given as

$$V_{FPA}(m,n) = V_{row}(m) - V_{pix}(m,n) - mI_0R_y - \frac{N}{K}(K-1-p)I_0R_x - KI_0R_x\sum_{k=0}^{c}(\frac{N}{K}-k) \quad (6.2)$$

$$V_{row}(m) = V_{pix\_ref} - NI_0(N-1-m)R_z \quad (6.3)$$

$$p = \mathrm{mod}(n,K) \quad (6.4)$$

$$c = (n-p)/K \quad (6.5)$$

where, m and n the row and column of the pixel, V_{row} is the bias voltage for the selected row, V_{pix} is the voltage of the selected pixel, I_0 is the pixel bias current, R_x and R_y are horizontal and vertical routing resistance values for a single pixel, N is the number of columns and rows in the FPA (N = 64), K is the number of the parallel readout channels (K = 16), p is the position index of the pixel in a selected column group ($0 \le p \le 3$), and c is the position index of the corresponding readout channel ($0 \le c \le 15$). As the array size increases, the resistive voltage drops become very critical in that they waste large portion of the input dynamic range of the designed preamplifiers. The variation in the vertical direction is less as compared to the variations in the horizontal direction due to two reasons. The first reason is that the resistance of the vertical routing lines outside the pixel area can be decreased easily, since there is no space limitation. The second reason is that the current level that flows vertically inside the FPA is low, reducing the voltage drops in the vertical direction. However, this is not the case for the horizontal lines, since they are

implemented within the pixel area, and associated current levels are very high, especially for the pixels close to the row select switches. The next section explains the effect of the FPA routing resistance on the infrared image with the help of MATLAB simulations.

6.2 Effect of the FPA Routing Resistance on the Infrared Image

The previous section shows that the routing resistances in the FPA cause some resistive voltage drops in the output signal, and the effects of these voltage drops need be evaluated. Figure 6.2 shows the simulated effect of FPA routing resistance on the infrared image.

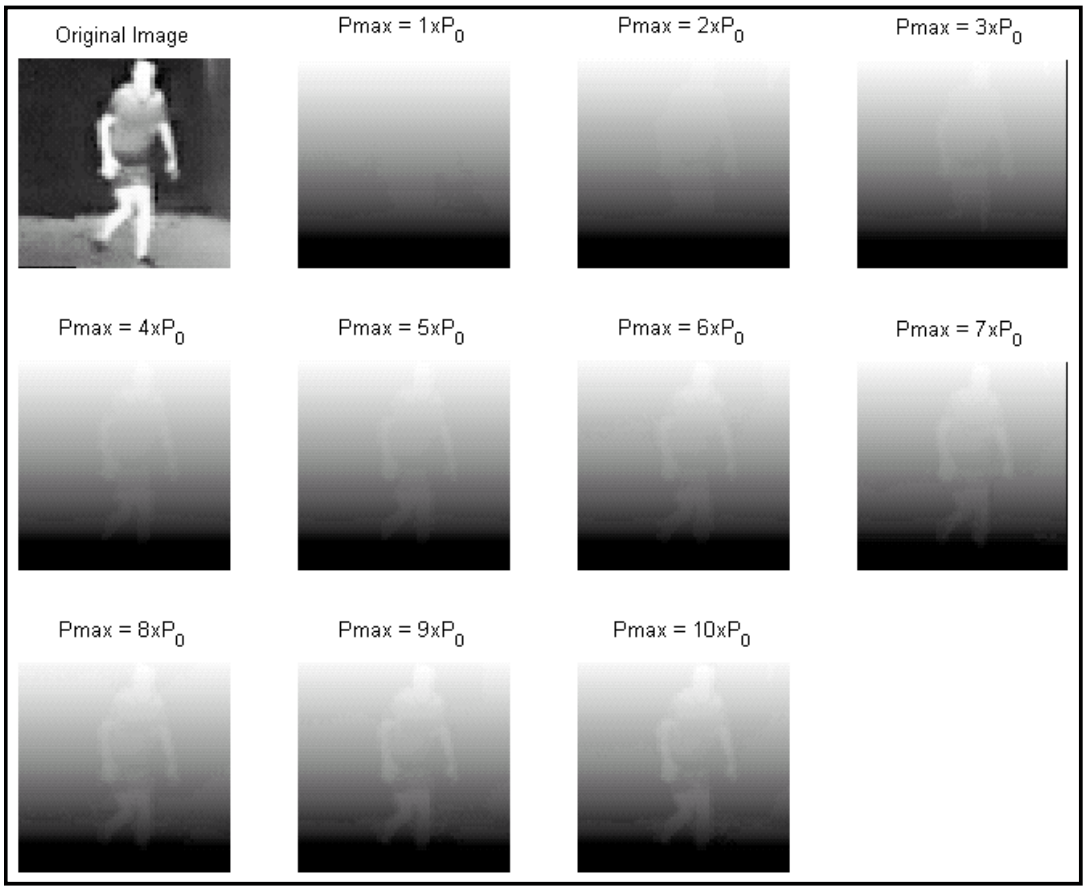


Figure 6.2: Simulated effect of FPA routing resistance on the infrared image.

The simulation given in Figure 6.2 is performed in MATLAB using a sample infrared image input, which models the infrared power incident to the FPA pixels. Incident pixel power is converted to a pixel voltage related with the pixel parameters, where the voltage variation due to the resistive drops in the FPA is also incorporated while calculating the multiplexed pixel voltages. Maximum pixel power in the array is P_{max}, and it is increased in steps of P_0 set as 1 nW for this simulation. In these simulations, it has been assumed that the readout circuit has sufficiently large dynamic range to accommodate the variations in the multiplexed pixel voltages. For simplicity, only the effect of vertical routing is considered in these simulations. These simulations shows that the voltage drops on the routing resistances severely affect the image quality, and therefore these voltage drops should be minimized or compensated to obtain a good quality image from the FPA. As expected, the resistive voltage drops in the FPA consumes most of the allowed dynamic range, and infrared induced voltage variation can not be understood, unless power of incident radiation is increased substantially. In the actual FPAs, the voltage gradient in the horizontal direction is more severe; therefore, solving this problem is the primary issue in designing of the diode FPAs. To compensate for the horizontal voltage variation, generation of exact replica of resistive voltages is required, which can be implemented using a number of parallel working active circuits with digital-to-analog data converters or identical reference pixels. The first method is complex and requires large number of components both when implemented on-chip of outside the chip. The second method can be implemented easily by using a number of reference pixels to compensate for the horizontal voltage drops and by designing the vertical interconnect routing to compensate for the vertical voltage drops. Considering all these factors, an improved array structure is developed, and the new array structure can compensate for all these resistive voltage drops in the array without using any active circuitry. This new array structure is used in the 128 × 128 FPA as explained in Chapter VII.

6.3 Reference Detector Array

The reference detectors in the 64 × 64 FPA compensate for the variation in the operating temperature, and partially for the self-heating effect. Figure 6.3 shows the layout of the reference detector array with its biasing circuitry, which measures 680 µm × 300 µm in a 3-metal 2-poly 0.35 µm CMOS process. The reference detectors are arranged in groups of 4 to serve for 64 × 4 array pixels. There are 4 reference pixel groups, and each of them is shared by 4 of the 64 × 4 array pixels. The reference detectors are electrically identical to the array pixels; however, they have different thermal properties. The thermal conductance of the reference detectors is very high as compared to that of the array pixels. Due to the high thermal conductance value of the reference detectors, they can be addressed more frequently with less self-heating. The thermal mass of the reference detector and array pixels are the same, which results in similar self-heating, at least for short integration periods [68, 69]. For longer integration periods, reference detector reaches the steady state much before the array pixels. Therefore, self-heating effect can not be compensated in detector level, and circuit level solutions should be provided. These methods are explained in Chapter VII.

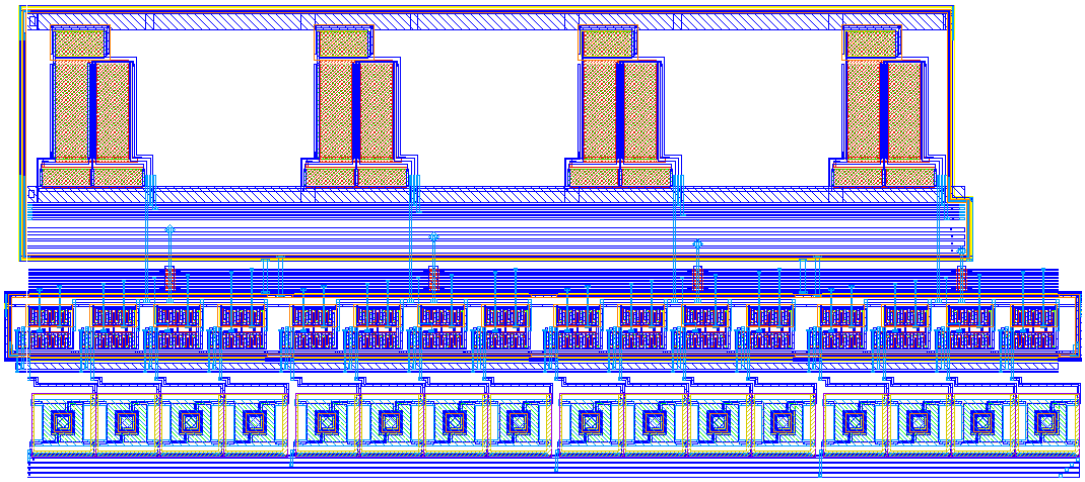


Figure 6.3: Layout of the reference detector array with its biasing circuitry, which measures 680 µm × 300 µm in a 3-metal 2-poly 0.35 µm CMOS process.

6.4 Readout Architecture of the 64 × 64 FPA Chip

Figure 6.4 shows the readout architecture of the 64 × 64 FPA chip. The FPA chip is composed of three main blocks: 1) analog circuits, 2) digital circuits, and 3) detector array. Analog circuits include the row and column multiplexers, channel readout circuit, and output multiplexers. The digital circuits include the vertical shift register (VSR), horizontal shift register (HSR), serial output shift registers (OSR), and a timing circuit that generates the control signals for the shift registers and for the analog channel readout circuit (ROC).

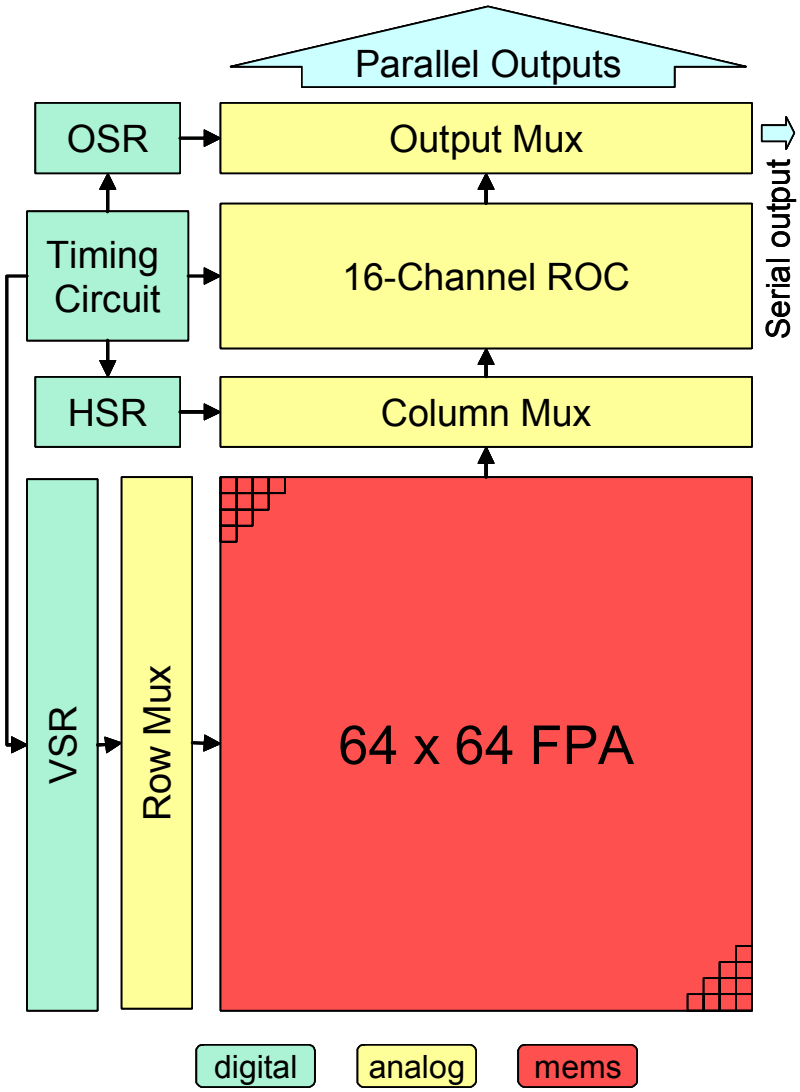


Figure 6.4: Readout architecture of the 64 × 64 FPA.

To limit the circuit noise, the electrical bandwidth of the readout circuitry is limited by using the parallel readout architecture. Due to the fact that the input transistors should be implemented with large aspect ratios, the required silicon area for the readout circuitry becomes quite large to fit into a single channel pitch of 40 μm. Therefore, a single readout channel is shared by a group of pixel columns in the detector array. In the 64 × 64 FPA chip, there are 16 parallel readout channels, each of which scans 4 FPA columns (512 pixels). This corresponds to an electrical bandwidth of about 4 kHz when the FPA is scanned at 30 fps. At a given time, 16 pixels are biased in a selected row, and they are read out in parallel by the corresponding readout channels. Row selection is performed by the analog row switches controlled by the vertical shift register, which stores a 64-bit data with a single bit being at logic high level whose position indicates the selected row of the FPA. Similarly, there is also horizontal shift register, which selects the pixels within each sub-array with 64 × 4 pixels. There are 16 such sub-arrays in the FPA, and a 4-bit shift register is used to address the pixels in these sub-arrays in parallel. The required timing signals for these shift registers and for the analog readout circuitry is generated by a scanning control unit. The next section explains the analog channel readout circuit and its building blocks.

6.5 Analog Channel Readout Circuit

Figure 6.5 shows the block diagram of the analog channel readout circuit in the 64 × 64 FPA. The channel readout circuit is composed of a differential transconductance amplifier whose output is integrated by a switched-capacitor integrator. The offset and low frequency correlated noise in the integrator is cancelled by a correlated double sampling (CDS) circuit followed by a sample-and-hold amplifier. The processed signal is buffered before the serial output multiplexers and parallel output pins. For testing purposes, there is also a 4-to-1 analog multiplexer which selects the outputs of the integrator, CDS, S/H circuits, or the array pixel. In addition to that, CDS can be by-passed, and the integrator output can be directly connected to the S/H amplifier for testing purposes.

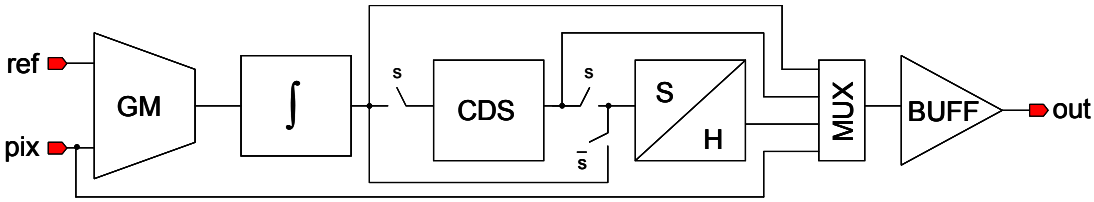


Figure 6.5: Block diagram of the analog channel readout circuit in the 64 × 64 FPA.

6.5.1 Low-Noise Preamplifier

The low-noise preamplifier constitutes the core of the analog channel readout circuit. The preamplifier is a differential transconductance amplifier specially designed to achieve very low noise operation. Figure 6.6 shows the schematic of the low-noise differential transconductance amplifier used in the 64 × 64 FPA chip. The n-channel transistors *N1* and *N2* form the differential input pair, and the n-channel transistor *N3* generates the bias current for the differential stage. The p-channel transistors *P1* and *P2* form the active loads working as a current mirror, while the p-channel transistors *P3* and *P4* are used to improve the current mirror operation by forming a high-swing current mirror with improved output resistance [63]. Following sections present the analysis and simulation results of this amplifier structure. The noise analysis of the circuit is performed in order to determine the effect of various transistor parameters on the overall circuit noise. Then, the noise simulation of the design is performed to compare the simulation results with the hand calculated values. In addition, a number of circuit parameters are simulated using Affirma Analog Design Environment in Cadence [70], including the frequency response and output resistance, the temperature sensitivity of the transconductance value, input referred offset and its temperature sensitivity, simulation of common mode range, the input capacitance, and settling time of the circuit.

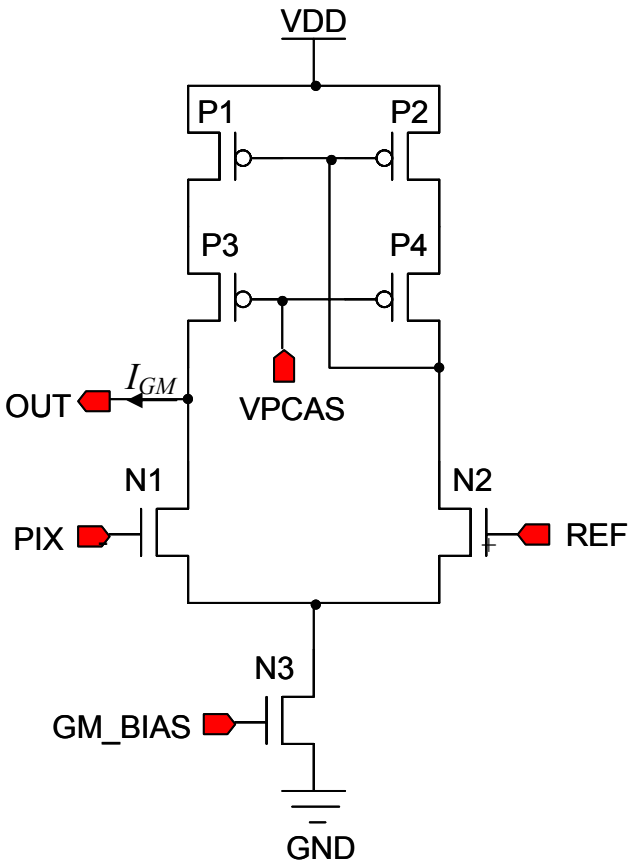


Figure 6.6: Schematic of the low-noise differential transconductance amplifier used in the 64 × 64 FPA chip.

6.5.1.1 Noise Analysis

Figure 6.7 shows the simplified schematic of the differential transconductance amplifier with important noise sources. The transistor noise is modeled as an equivalent voltage connected to their gate inputs. Among them, the noise voltage of *N3* is not shown due to the fact that its noise contribution acts as a common source signal which is negligible due to sufficiently high common mode signal suppression capability of the given differential circuit [71].

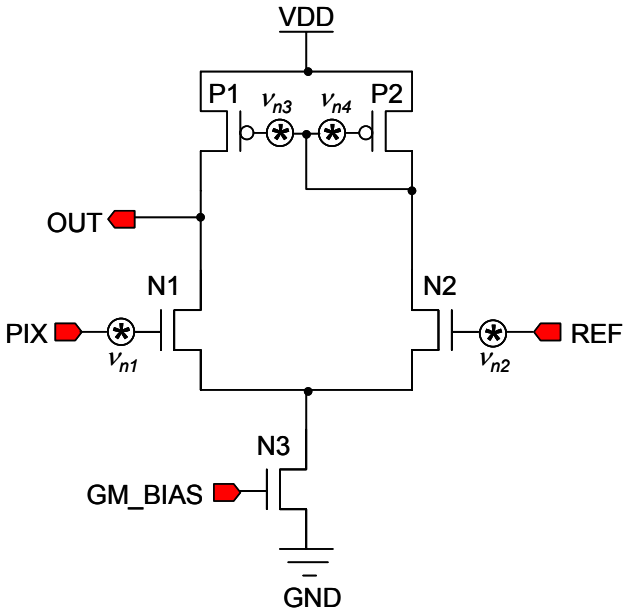


Figure 6.7: Simplified schematic of the differential transconductance amplifier with important noise sources.

The output noise current and input referred noise of the differential circuit is given as [71]

$$i_{out}^2 = \left(v_{n1}^2 + v_{n2}^2\right) g_{mi}^2 + \left(v_{n3}^2 + v_{n4}^2\right) g_{ml}^2 \tag{6.6}$$

$$v_{in}^2 = v_{n1}^2 + v_{n2}^2 + \left(\frac{g_{ml}}{g_{mi}}\right)^2 \left(v_{n3}^2 + v_{n4}^2\right) \tag{6.7}$$

where, v_{n1} and v_{n2} are gate referred noise voltages of the differential input pair *N1* and *N2*, g_{mi} is the transconductance of the input pair transistors, v_{n3} and v_{n4} are the gate referred noise voltages of the active load transistors *P1* and *P2* with their transconductance values of g_{ml}. The above noise equations suggests that the squared input referred noise of the differential transconductance amplifier is the sum of the noise powers of the input pair and the scaled sum of the noise powers of the load pair. Therefore, to minimize overall noise, noise contribution of the input pair should be minimized as the primary task. Since the transconductance of the load transistors are much lower than that of the input pair, their noise contribution will be suppressed by a factor related with the ratio of their transconductance values.

The power spectral density of the gate referred noise voltage for a MOS transistor has two components: 1) thermal noise and 2) flicker (1/*f*) noise. These noise components originate from two independent noise mechanisms, and their power spectral density values can be added to determine the total noise power spectral density. The gate referred noise power spectral density of a MOS transistor is given as [63]

$$v_n^2 = \frac{8kT}{3g_m} + \frac{K}{C_{ox}WLf} \tag{6.8}$$

where, k is the Boltzmann constant, T is the temperature in Kelvin, g_m is the transconductance of the MOS transistor, K is the flicker noise coefficient, C_{ox} is unit gate capacitance, W and L are device width and length values, and f is the frequency in Hz. According to the above noise expression, g_m of the transistor should be increased to minimize the thermal noise component. This can be achieved by increasing the bias current level as much as the allowed power dissipation. To improve the g_m value, the device can be designed with higher W/L ratios. Considering the fact that flicker noise component decreases as the gate area decreases, L of the transistor should be kept above a certain level. This requires quite large device widths when the transistor's lower operating frequency is below 1 Hz, which is the case for most of the microbolometer detectors. Table 6.1 gives the device geometries for the circuit given in Figure 6.6.

Table 6.1: Device geometries for the circuit given in Figure 6.6.

Transistor	W (μm)	L (μm)	Number of Gates
N1, N2	4725	3.5	35
N3	20	15	2
P1, P2	90	15	3
P3, P4	90	3	3

Figure 6.8 shows the simulated input referred noise power spectral density of the differential transconductance amplifier from 100 mHz to 4 kHz. Total rms noise voltage is extracted as 0.57 μV in 4 kHz bandwidth. It should be noted this noise level is close to that of the single detector. Due to the large device geometries used

in the preamplifier circuit, 1/*f* noise of the MOS transistor is kept at a low level; the knee frequency (*1/f* corner frequency) is found to be less than 600 Hz for the preamplifier circuit, which is in the order of several kHz for MOS circuits with small device sizes.

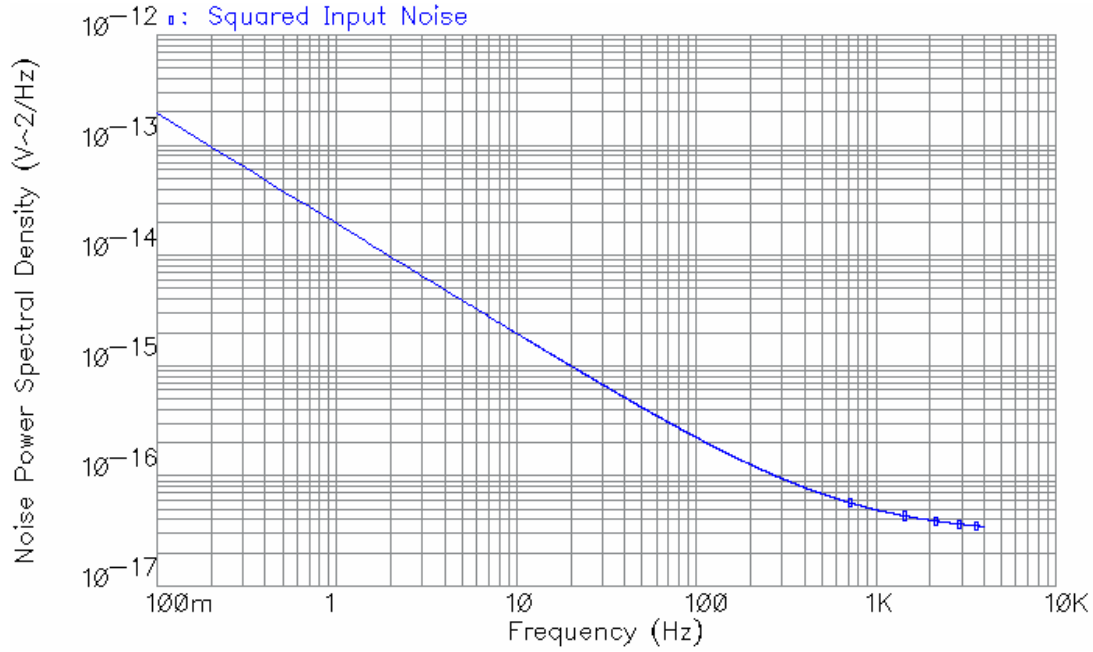


Figure 6.8: Simulated input referred noise power spectral density of the differential transconductance amplifier from 100 mHz to 4 kHz. Total rms noise voltage is extracted as 0.57 μV in 4 kHz bandwidth.

6.5.1.2 AC Analysis

Figure 6.9 shows the simulated transconductance value of the differential transconductance amplifier designed for the 64 × 64 FPA. The simulated transconductance value is 1004 μA/V with a 3 dB corner frequency of 2.45 MHz, well above the 4 kHz bandwidth of the 64 × 64 FPA. Figure 6.10 shows the simulated small signal output resistance of the differential transconductance amplifier. Output resistance is larger than 1 MΩ for frequencies less than 20 kHz. This output resistance is sufficiently high, since the output of the differential transconductance amplifier is connected to an integrator with almost zero input impedance as will be explained later.

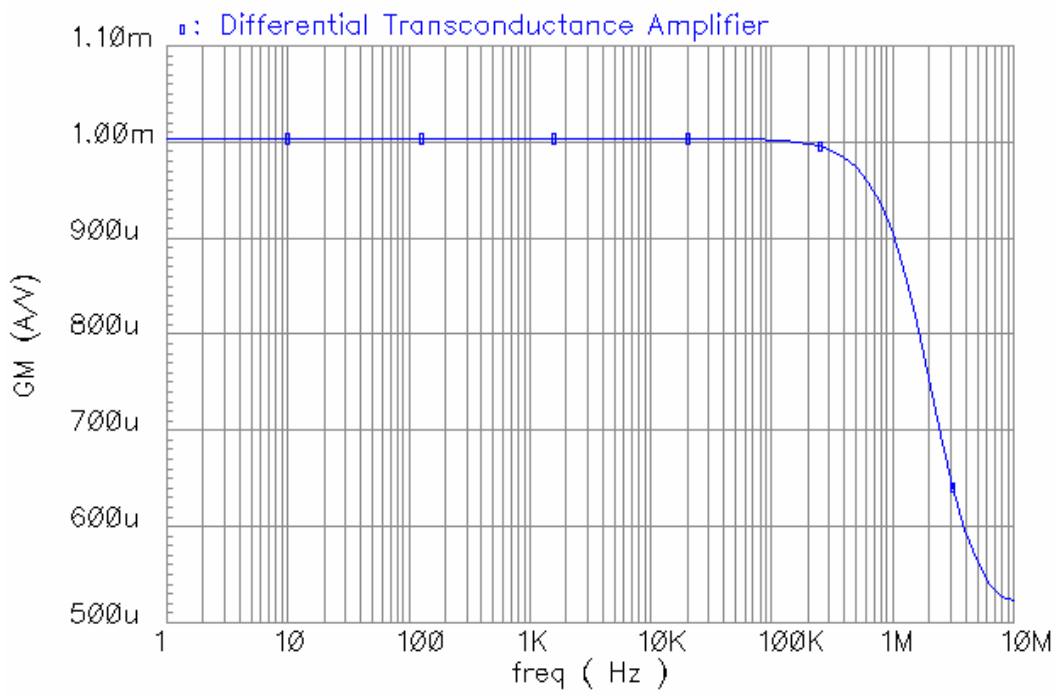


Figure 6.9: Simulated transconductance value of the differential transconductance amplifier designed for the 64 × 64 FPA. The simulated transconductance value is 1004 µA/V with a 3 dB corner frequency of 2.45 MHz well above the 4 kHz bandwidth of the 64 × 64 FPA.

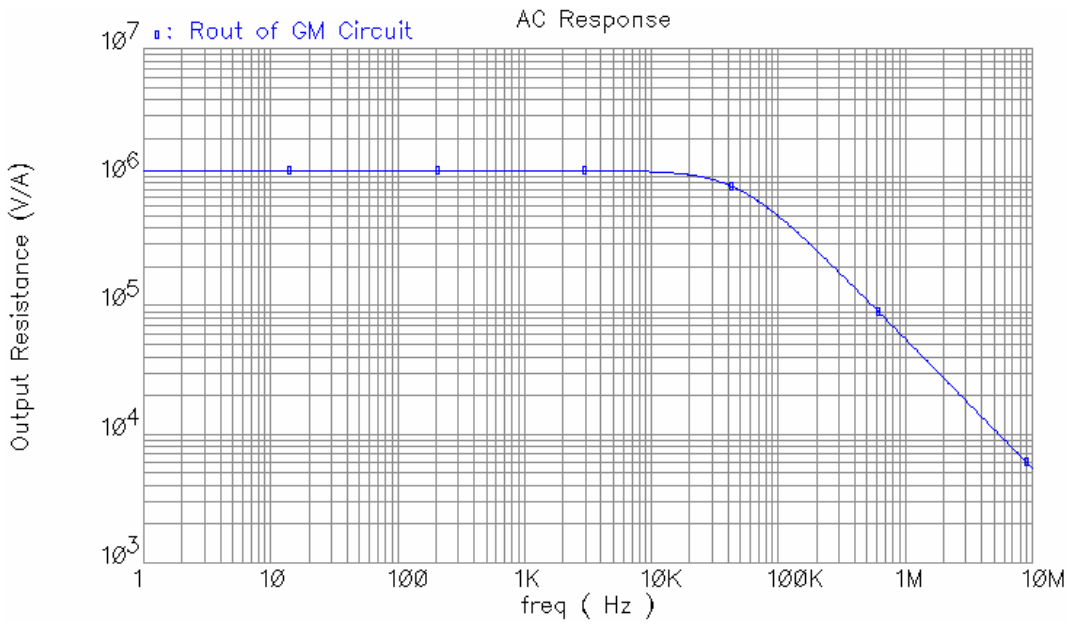


Figure 6.10: Simulated small signal output resistance of the differential transconductance amplifier. Output resistance is larger than 1 MΩ for frequencies less than 20 kHz.

Figure 6.11 shows the simulated variation of transconductance value with operating temperature. The result is obtained using AC analysis at different temperatures from 0 °C to 50 °C. The temperature sensitivity of the transconductance value is extracted as -4.6 µA/V/K, which corresponds to a temperature coefficient of 0.46 %/K. It should be noted that the differential readout reduces the temperature dependency of the output signal to great extend; therefore, the dynamic range is preserved avoiding any possible saturation problems. The performed simulation indicates that the transconductance of the input stage has a temperature coefficient of 0.46 %/K. Secondly, the change in the transconductance value only modifies slightly the infrared induced current output, which in turn alters the gain slightly. If it is desired to make the gain independent of temperature, then the input stage should be designed so as to provide constant transconductance at the expense of increased circuit complexity and noise [71]. The problem can also be solved by generating the required bias voltage for the differential transconductance amplifier using a D/A based circuitry with a proper lookup table.

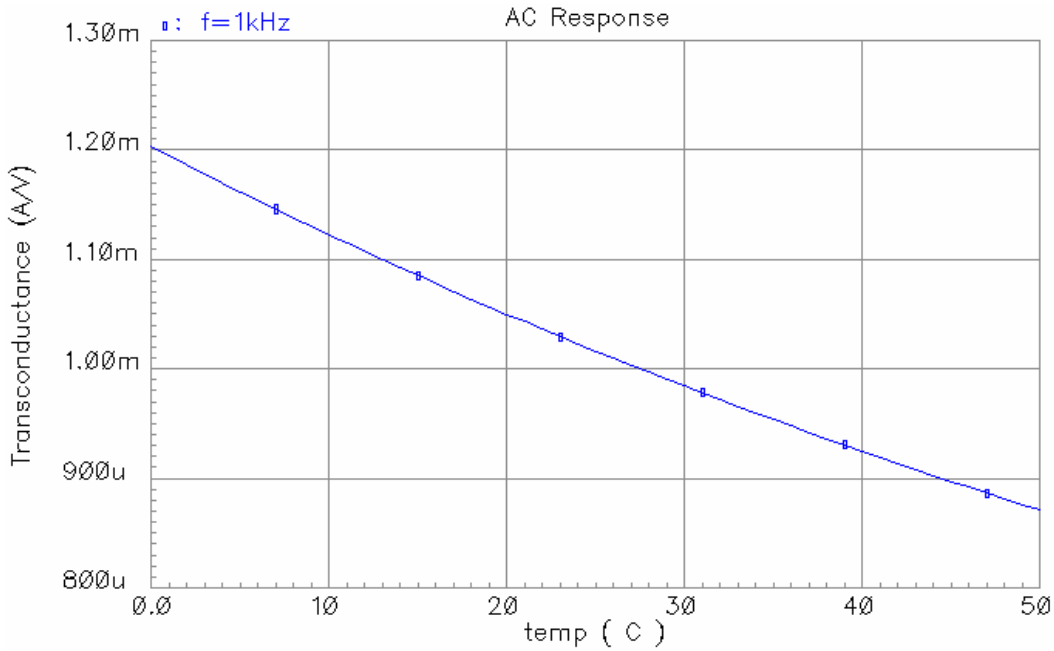


Figure 6.11: Simulated variation of transconductance value with operating temperature. The result is obtained using AC analysis at different temperatures from 0 °C to 50 °C. The temperature sensitivity of the transconductance value is extracted as -4.6 µA/V/K, which corresponds to a temperature coefficient of 0.46 %/K.

6.5.1.3 DC Analysis

Figure 6.12 shows the DC simulation result of the output current (I_{GM}) with respect to the differential input voltage (V_{rp}-V_{ap}). The offset current is simulated to be about 530 nA, which corresponds to 0.53 mV input referred offset voltage.

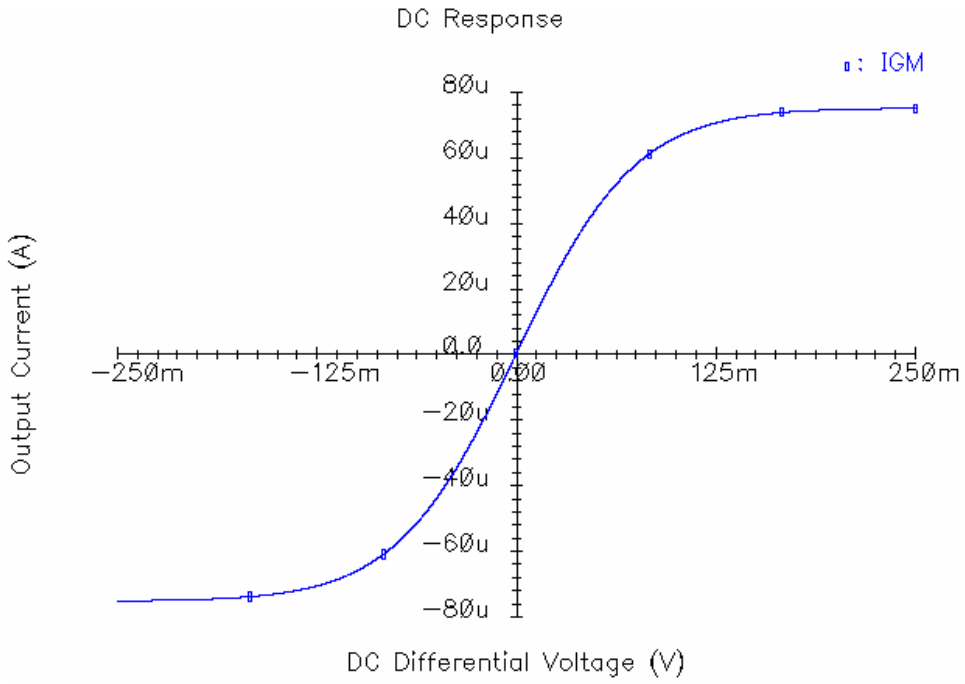


Figure 6.12: DC simulation result of the output current (I_{GM}) with respect to differential input voltage (V_{rp}-V_{ap}).

Figure 6.13 shows the simulated variation of the offset current of the differential transconductance amplifier with respect to operating temperature from 0 °C to 50 °C. The differential voltage is set to 0 V, and the offset at room temperature (27 °C) is found to be about 530 nA. It should be noted that the variation of the offset voltage is less than 30 nA for a 50 °C temperature change, and the sensitivity becomes less as the temperature is increased above the room temperature. To compensate for the 530 nA offset current, the bias voltage of the reference pixel should be adjusted to pull the offset level below 200 nA. The residual offset current can be cancelled by the offset current removal circuit placed in front of the switched capacitor circuit explained in Section 6.5.2.

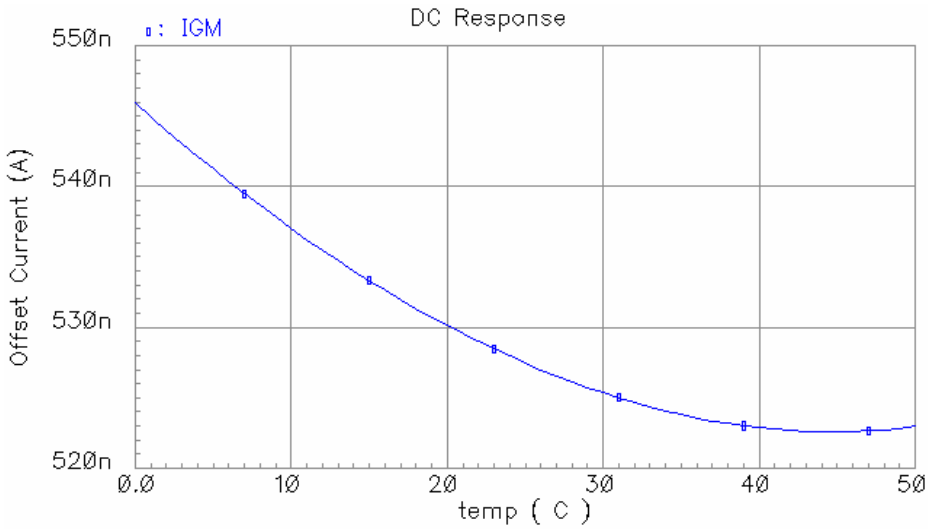


Figure 6.13: Simulated variation of the offset current of the differential transconductance amplifier with respect to operating temperature from 0 °C to 50 °C. Differential voltage is set to 0 V, and offset at room temperature (27 °C) is about 530 nA.

6.5.1.4 Input and Output Dynamic Range

Figure 6.14 shows the simulated variation of the transconductance value with respect to the input common mode voltage swept for different output common mode voltage values. This data is obtained by performing AC analysis at 1 kHz for different input and output DC voltage levels. The input common mode voltage is swept rail-to-rail, while the output common mode voltage is simulated at discrete points from 0.5 V to 3.0 V in six linear steps. To operate the differential stage for wide input common mode range, the output voltage should be selected somewhere close to the analog signal ground ($V_{DD}/2$ = 1.65 V). At this point, the input common mode voltage can also be selected as $V_{DD}/2$, which will also help to reduce the required number of analog bias voltages for the overall readout circuit. In the actual circuit, the detectors are biased such that the input common mode voltage remains at half of the supply voltage. The output voltage of the transconductance amplifier is determined by the input common mode voltage of the switched capacitor integrator, which is also the reset voltage of the integrator. For proper operation, it is also selected to be at half of the supply voltage. The offset current of the

transconductance amplifier is adjusted to make use of the maximum available output swing at the integrator circuit.

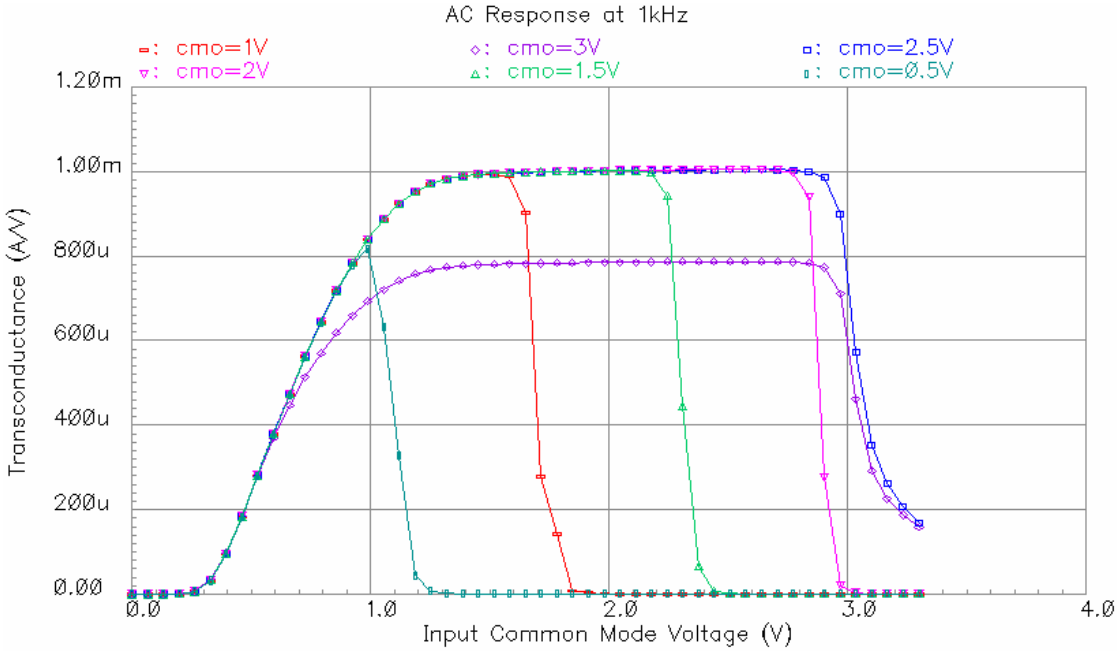


Figure 6.14: Simulated variation of the transconductance value with respect to input common mode voltage swept for different output common mode voltage values. This data is obtained by performing AC analysis at 1 kHz for different input and output DC voltage levels. Input common mode is swept rail-to-rail, while output common mode voltage is simulated at discrete points from 0.5 V to 3.0 V in six linear steps.

6.5.1.5 Input Capacitance and Settling Time

The use of large devices in the differential input stage reduces the input referred noise of the preamplifier. However, large devices have high input capacitance values, increasing the settling time of the preamplifier when the input is switched during scanning between different pixels in the FPA. Figure 6.15 shows the simulated circuit schematic to determine the input capacitance (C_{in}) of the transconductance (GM) circuit. The value of C_s at which the transconductance from source to the output decreases to half of the designed transconductance value of the GM circuit is equal to the input capacitance of the GM circuit at a single input terminal. To solve the problem of DC biasing at the input pins, dual supply voltages (V_{DD} and V_{SS}) are used, where the input DC level reduces to 0 V.

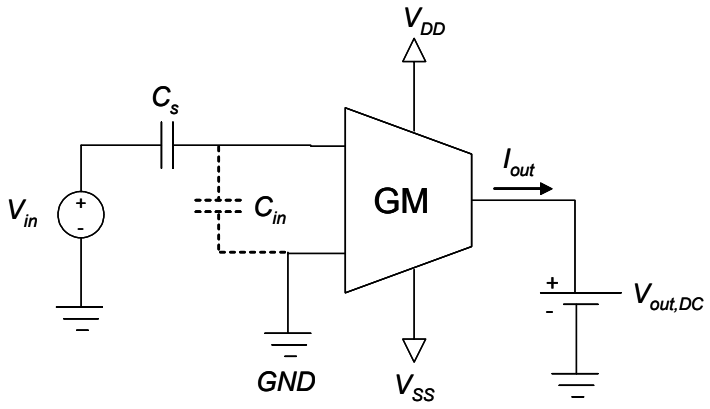


Figure 6.15: Simulated circuit schematic used to determine the input capacitance (C_{in}) of the GM circuit.

Figure 6.16 shows the simulated variation of the overall transconductance with varying source capacitance (C_s). The value of C_s at which the gain drops to half of the original value is equal to the value of the input capacitance value (C_{in}). When Cs becomes 20.3 pF, overall transconductance value reduces to 500 µA/V, which is half of the original transconductance of the GM circuit (1000 µA/V). The input capacitance for a single input is determined as 20.3 pF, which is large due to the large geometry of the input transistors necessary for noise reduction.

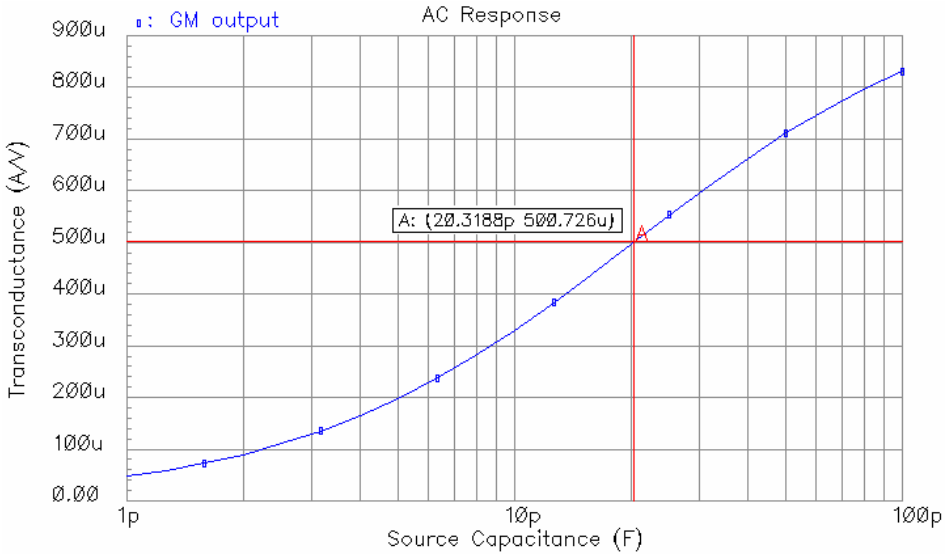


Figure 6.16: Simulated variation of overall transconductance with varying source capacitance. The value of C_s at which the gain drops to half of the original value is equal to the value of the input capacitance value (C_{in}). The input capacitance for a single input is determined as 20.3 pF.

In fact, the 20 pF input capacitance is a high value and may impact the readout performance severely, if the turn-on resistance of the FPA multiplexer circuit is not minimized to keep the resulting time constant at an acceptable level. Figure 6.17 shows the simplified schematic of the input stage showing the pixel select circuitry with the row and column select switches, the constant current source, and the GM circuit. The array reference bias voltage (V_{ref_ap}) is adjusted to bias the inverting input of the GM circuit at half of the supply voltage ($V_{DD}/2$), and non-inverting input of the GM circuit is biased by a DC voltage so as to decrease the output steady state current below 50 nA, typical for most of the applications. A transient simulation is performed to measure the settling time from the application of the pixel select pulse to the time at which the output current reaches its steady state value.

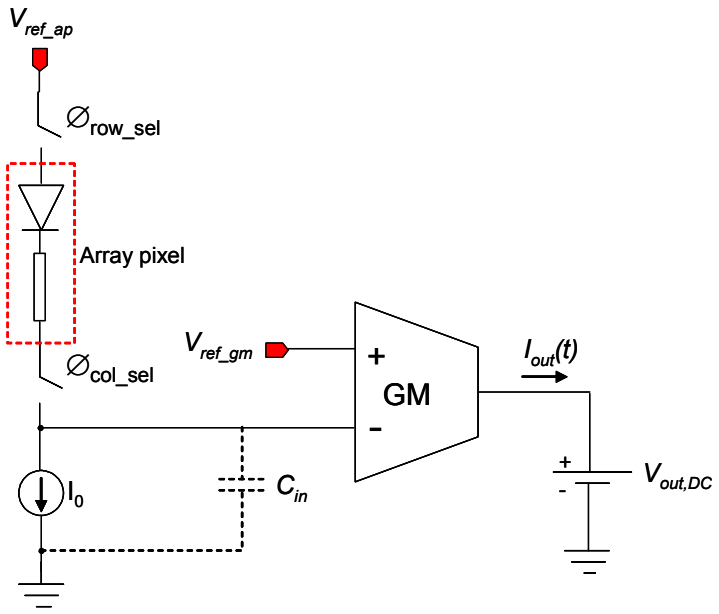


Figure 6.17: Simplified schematic of the input stage showing the pixel select circuitry with the row and column select switches, the constant current source, and the GM circuit.

The settling time is determined by the time constant of the input node, which depends on the input capacitance and the output resistance of the pixel biasing circuit including the pixel, select switches, and the current source. Since the current source have much higher output resistance as compared to the others, the output resistance

of the node driving the GM input terminal is determined by the resistance of the pixel and the small signal resistances of the pixel select switches. The pixel itself has a small resistance coming from the resistive interconnects and the small signal resistance of the diode. The interconnect resistance is 3 kΩ, and the diode small signal resistance is 2.5 kΩ at the designed bias level of 10 µA, making the overall pixel resistance 5.5 kΩ. The row and column switches are implemented with CMOS transmission gates with sufficiently large W/L values (120 µm / 0.3 µm) to keep the turn-on resistance and the associated thermal noise at relatively low level. The designed CMOS transmission gate has small signal resistance value of 51 Ω at 10 µA pixel bias level, whose contribution to the settling time is negligible. The output resistance of the pixel bias current reduces to that of the pixel, which results a time constant value of 114 ns. Figure 6.18 shows the simulated transient response of the bias and pixel select circuitry when driving a 20.3 pF load, equivalent to that of the input capacitance of the GM circuit. The time required for the transient to decay is recorded as 0.75 µs, which is sufficiently low as compared to pixel select time allowing enough integration time with moderate scanning rates where the pixel time is usually well above 20 µs.

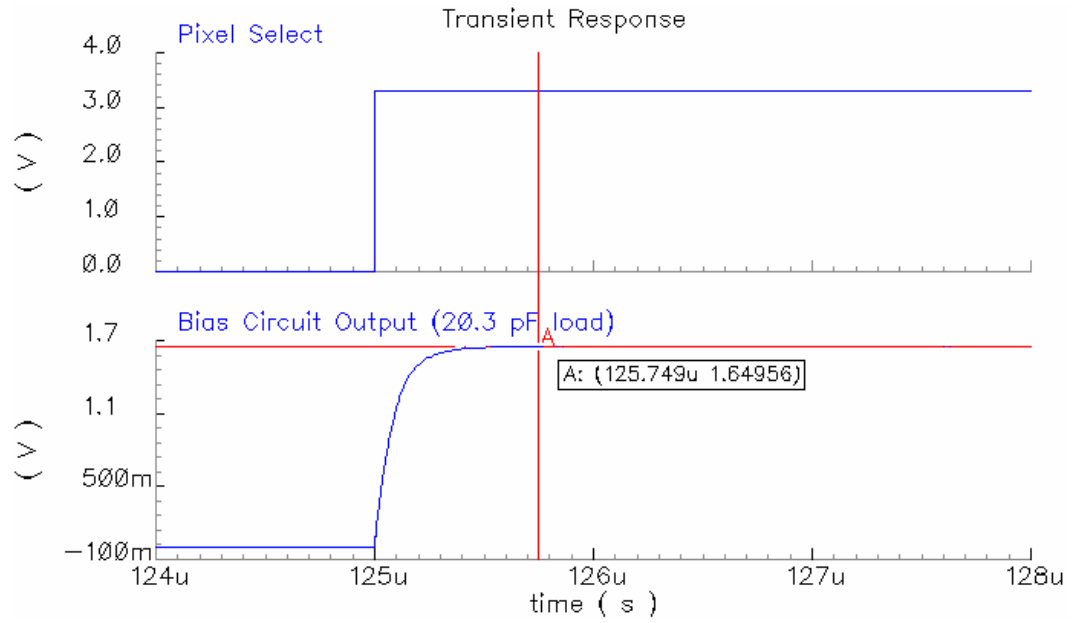


Figure 6.18: Simulated transient response of the bias and pixel select circuitry when driving a 20.3 pF load equivalent to that of the input capacitance of the GM circuit. The time required for the transient to decay is recorded as 0.75 µs.

The transient response of the GM circuit also contributes to the settling time in that it faces a large signal swing at its inputs. This happens because there is a short period lasting for a few micro seconds during which the pixel is disconnected from the GM circuit, and the input of the GM circuit is discharged by the current source. When the reference potential is kept same, a large current will flow out of the device due to a large differential input voltage. To avoid any saturation at the following integrator stages, integration should be disabled before the row and column select switches are turned off. Considering the fact that the output resistance of the bias circuit is high on the average during this period, the associated time constant is higher resulting longer transient in this case. When the next pixel is selected, the inverting input voltage of the GM circuit starts to increase, causing the output current to decrease from its large levels in the order of a few tens of µA to much lower levels in the order of a few tens of nA. Figure 6.19 shows the simulated settling time of the differential transconductance (GM) output current upon the applied pixel select pulse (at t=125 µs). All the transient effects decay within the first 2 µs, and the output reaches its steady state value within 2 µs.

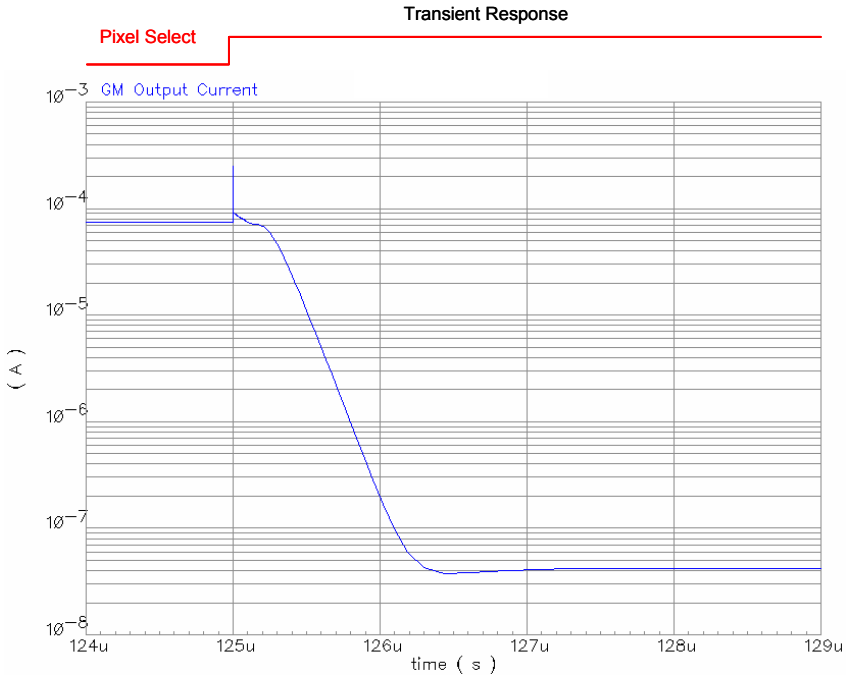


Figure 6.19: Simulated settling time of the differential transconductance (GM) output current upon an applied pixel select pulse (at t=125 µs), and output reaches its steady state value within 2 µs.

The settling time is longer, mainly due to the effects of internal dynamics of the GM circuit subject to a large signal swing at its inputs during the switching period. In order to be able to resolve small variations in the pixel voltages due to infrared radiation, integration should only be started after waiting for sufficiently long time so that all of the transient signals decay. In fact, for 30 fps scanning rate, the pixel access time is 125 μs for the 64 × 64 FPA, and only 110 μs of this period is used for integration, which is found to be sufficient to avoid any transient effects.

6.5.1.6 Power Dissipation

The supply voltage of the differential transconductance amplifier is 3.3 V, and it is biased at 80 μA, causing a power dissipation of 264 μW. By increasing the bias level and device sizes, it is possible to decrease circuit noise level at the expense of increased power consumption and increased silicon area. However, neither of these methods can be applied easily, since the overall chip power consumption will increase due to the large number of readout circuits running in parallel. The device dimensions cannot be increased beyond certain levels, since the readout circuits should be able to fit into narrow regions limited by the narrow pixel pitches.

6.5.1.7 Layout

Figure 6.20 shows the layout of the input differential pair used in the low-noise differential transconductance amplifier in the 64 × 64 FPA. The transistors have W/L values of 4250 μm / 3.5 μm implemented using 35 identical gates laid out in an interdigitated manner for improved matching purposes [72]. It measures 155 μm × 387 μm in a 3-metal 2-poly 0.35 μm CMOS process. Figure 6.21 shows the layout of the load and bias transistors of the differential transconductance amplifier used in the 64 × 64 FPA. It also includes the offset removal circuitry together with integration enable switches. For matching purposes, the transistor pairs are laid out symmetrically in an interdigitated manner. The layout measures 140 μm × 158 μm in a 3-metal 2-poly 0.35 μm CMOS process.

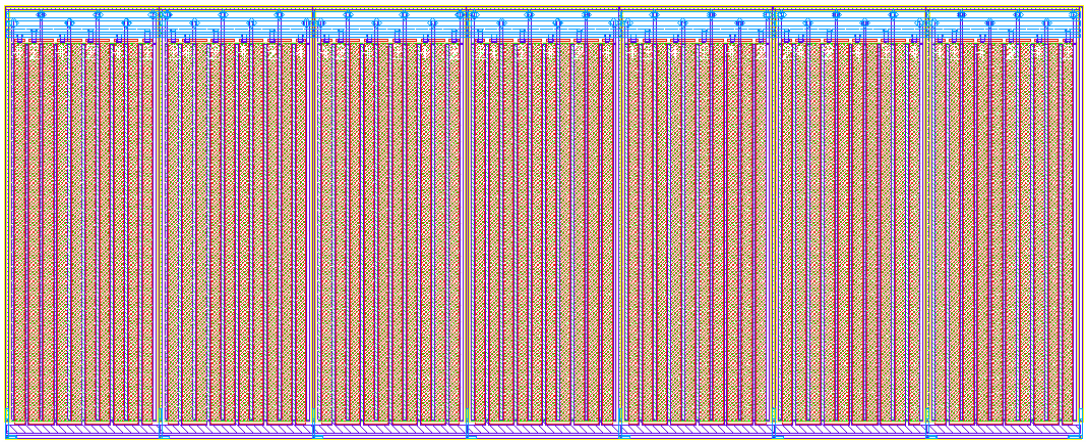


Figure 6.20: Layout of the input differential pair used in the low-noise differential transconductance amplifier in the 64 × 64 FPA. The transistors have *W*/*L* values of 4250 µm / 3.5 µm implemented using 35 identical gates laid out in an interdigitated manner for improved matching purposes [72]. It measures 155 µm × 387 µm in a 3-metal 2-poly 0.35 µm CMOS process.

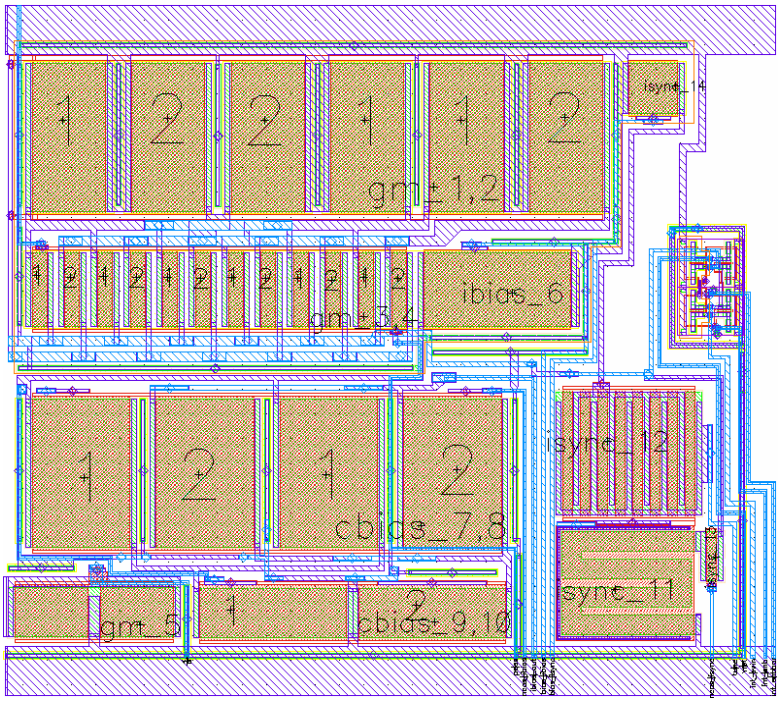


Figure 6.21: Layout of the load and bias transistors of the differential transconductance amplifier used in the 64 × 64 FPA. It also includes the offset removal circuitry together with integration enable switches. For matching purposes transistor pairs are laid out symmetrically in an interdigitated manner. The layout measures 140 µm × 158 µm in a 3-metal 2-poly 0.35 µm CMOS process.

6.5.2 Switched-Capacitor Integrator (SCI)

Figure 6.22 shows simplified block diagram of the switched capacitor integrator circuit (SCI) together with the offset current sink circuit, differential transconductance amplifier, and detector bias circuit. The array detector and the reference detector are represented by forward biased diodes biased at identical DC bias currents (I_0). The anodes of these diodes are connected to a common bias voltage (*vref*), and their cathode voltages are read out by the differential transconductance amplifier (*GM*). The polarity of the input terminals is chosen to indicate that the output current (I_{GM}) direction is out of the transconductance stage. The offset current sink circuitry [58] subtracts the DC portion of the I_{GM} to increase the dynamic range of the integrator by eliminating the DC component of the integrated current. Therefore, the integrated current, hence the integrator output voltage (*int_out*) measured with respect to the reset voltage (*vrst*) will be linearly proportional with the absorbed infrared radiation.

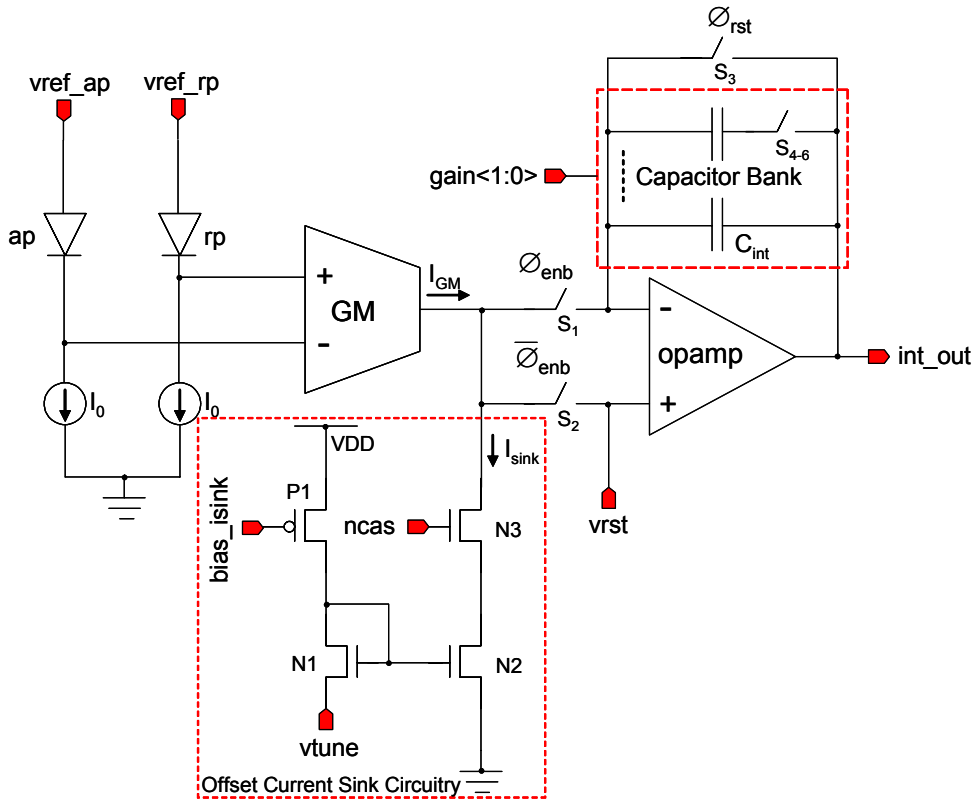


Figure 6.22: Simplified block diagram of the switched capacitor integrator (SCI) circuit together with the offset current sink circuitry, differential transconductance amplifier, and detector bias circuit.

Upon absorbed infrared radiation, the temperature of the array pixel (*ap*) rises, and the detector forward bias voltage decreases increasing its cathode voltage. As a result of this, there is a non-zero current flowing into the transconductance amplifier output. This infrared induced current output is integrated by the switched capacitor integrator after it is reset. Therefore, the integrator output rises from its reset voltage.

In the switched capacitor circuits, there is a problem known as charge injection, where the charge stored in the parasitic capacitances of the transistors are injected into the periodically switched capacitors during switching instants, causing errors in the capacitor voltages [73]. The effect of charge injection can be minimized by using dummy transistors in series with the actual switching transistor. By selecting properly sized dummy transistors operated at the opposite phase of the clock signal as compared to that of the actual reset transistor, the charge injection problem can be minimized considerably [73]. In order to suppress the voltages induced by charge injection, the integration capacitance value should be much larger than the parasitic capacitance values. Using larger capacitance values also decreases the voltage noise across the integration capacitance due to the thermal noise of channel resistance of the reset transistor. The square of the total integrated thermal noise voltage across a capacitor with a parallel resistance over an infinite bandwidth is given as [73]

$$v_n^2 = \frac{kT}{C} \tag{6.9}$$

where, k is the Boltzmann constant, T is the temperature, and C is the capacitance. Since an infinite bandwidth is used in the derivation, it is expected that actual noise voltage will be smaller than the value predicted by Equation 6.9. Although, the above noise voltage is only due to the thermal noise of the parallel resistance, the resistance value does not enter directly in the above expression. When the resistance increases, the noise power spectral density of the associated thermal noise increases; however, total integrated noise in the infinite bandwidth remains the same due to the narrower bandwidth associated with the capacitance and increased resistance. The

total current noise at the integrator input can be calculated by dividing this value by the integrator gain expression, and the total current noise at the input of the switched capacitor integrator is approximately given as

$$v_n^2 = \frac{kT}{C}\left(\frac{C}{t_{\text{int}}}\right)^2 = \frac{kTC}{t_{\text{int}}^2} \tag{6.10}$$

where, k is the Boltzmann constant, T is the temperature, C is the integration capacitance, and t_{int} is the integration period. According to this result, integration capacitance (C) should be decreased in order to decrease the input referred noise. Decreasing the integration capacitance helps also to increase the gain; however, there is a limit on the minimum value of the C set by the charge injection effects. In fact, since a differential transconductance amplifier is used prior to the switched capacitor integrator, the effect of kTC noise is negligible, and sufficiently large capacitances in the order of pF can be used without increasing much the input noise at the detector side.

Another problem is saturation of the integrator circuit due to the large offset in the integrated current. The offset in the integrated current can be eliminated in two ways: 1) by adjusting the reference bias voltages of the array pixel (*vref_ap*) or reference pixel (*vref_rp*), and 2) by adjusting the current that is sunk (I_{sink}) prior to integration. The former method is suitable to perform coarse offset adjustment, while the latter method is suitable for fine offset adjustment. It should also be mentioned that the offset removal circuit has a uni-polar nature due to the NMOS current mirrors, which may require use of both methods when the offset current turns out to be negative. Due to the large transconductance value, high resolution D/A converters should be used for offset cancellation when the first method is used. The transconductance value is 1000 µA/V, which corresponds to 1 µA change in the output current per 1 mV change in the reference bias voltage. For a 3.3 V supply, a 14-bit D/A converter can be used to adjust the reference voltages with a resolution of 0.2 mV, corresponding to 200 nA offset current correction capability. The values less than 200 nA can be compensated by using the offset current sink circuitry.

6.5.2.1 Offset Current Sink Circuitry

The offset current sink circuitry is composed of a bias transistor *P1*, a modified current mirror formed by *N1* and *N2*, and a cascode transistor *N3*. The bias transistor (*P1*) generates a bias current, which generates the V_{GS} potential of the diode connected NMOS transistor (*N1*). This V_{GS} voltage is in series with the applied tune voltage (*vtune*). Since the gates of the modified current sources are connected and its source is grounded, the current through *N2* is determined by the gate voltage of *N1*. By choosing the *W*/*L* ratio of *N1* large, its gate overdrive voltage can be decreased considerably. Therefore, the gate voltage of *N1* is mainly determined by its threshold voltage and the applied *vtune* voltage. Since gates of the *N1* and *N2* are tied to a common potential, the gate overdrive potential for *N2* will be mainly determined by the externally applied *vtune* voltage, making the output current insensitive to the threshold variations through out the FPA and the variations in the bias current through *P1* [74]. On the other hand, the *W*/*L* ratio of *N2* is made considerably small, which reduces the device current through *N2* as much as possible, making it possible to cancel very small offset currents with the help of relatively large voltage steps. Table 6.2 gives the device geometries for the offset current sink circuitry.

Table 6.2: Device geometries for the offset current sink circuitry.

	W (µm)	**L (µm)**
P1	10	10
N1	200	2
N2	4	100
N3	10	2

The output current of the offset current cancellation circuitry is given as [74]

$$I_{D1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS1} - V_{tn})^2 \tag{6.11}$$

$$V_{GS1} = \sqrt{\frac{2I_{D1}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_1}} + V_{tn} \tag{6.12}$$

$$I_{sink} = I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 \left(\sqrt{\frac{2I_{D1}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_1}} + V_{tune}\right)^2 \tag{6.13}$$

where, I_{D1} is the drain current of *N1* determined by the bias transistor *P1*, μ_n is the electron mobility, C_{ox} is the unit gate capacitance, W and L are device width and length, V_{GS1} is the gate-to-source potential for *N1*, V_{tn} is the threshold voltage for the NMOS transistors, and V_{tune} is the tune voltage used to adjust the output current (I_{sink}) of the offset current cancellation circuitry. It should be noted that the I_{sink} is almost independent of the threshold parameter, which is both temperature dependent and varies within and between the FPAs. By choosing the bias current of *N1* (I_{D1}) low and making its device geometry,$(W/L)_1$, small, output current (I_{sink}) will be mainly determined by the applied tune voltage (V_{tune}), which also decreases the temperature sensitivity considerably [74].

Figure 6.23 shows the simulated variation of the output current of the offset current sink circuitry with respect to the tune voltage (V_{tune}) at different operating temperatures ranging from 0 °C to 50 °C. It is designed to cancel the offset current values as low as 1 nA. The only disadvantage of this method is that the current-voltage expression is not linear, which can easily be handled by a moderate resolution digital-to-analog converter and a look-up table.

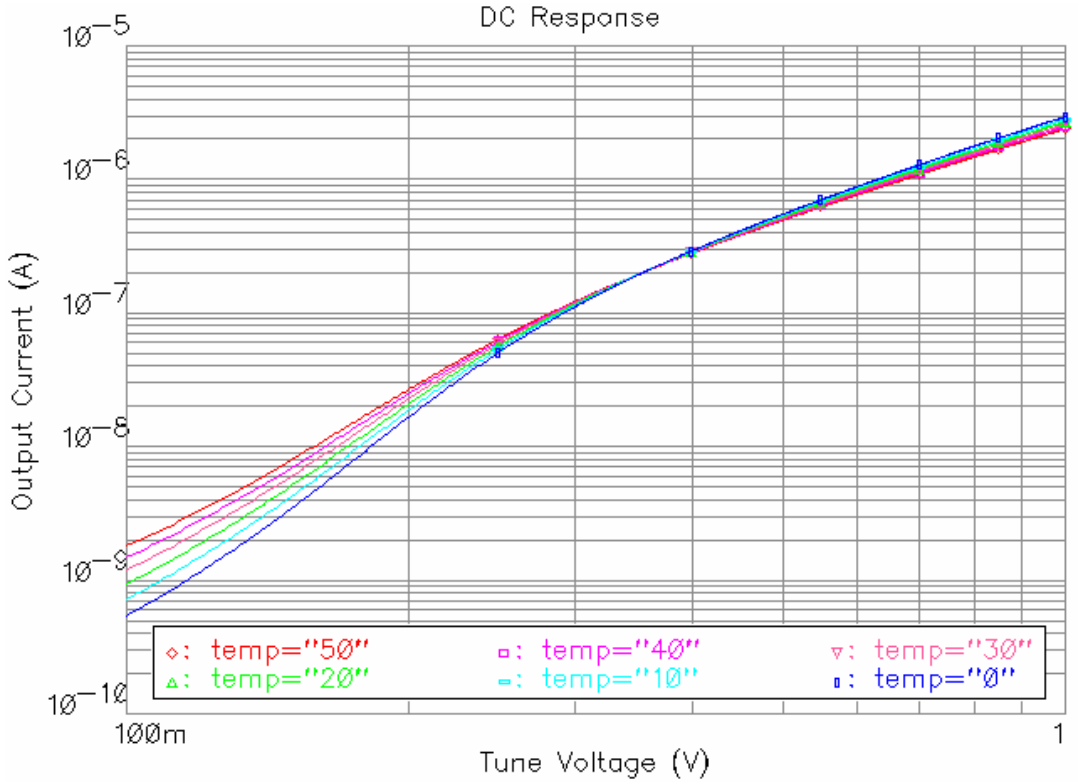


Figure 6.23: Simulated variation of the output current of the offset current sink circuitry with respect to the tune voltage (V_{tune}) at different operating temperatures ranging from 0 °C to 50 °C. The circuit is designed to cancel the offset current values as low as 1 nA.

6.5.2.2 Variable Gain Adjustment

The gain of the switched capacitor integrator is adjusted by varying the integration capacitance and by changing the integration time. Integration capacitance can be changed from 1.17 pF to 9.36 pF, which is controlled by a 2-bit digital control word (*gain<1:0>*). The integration time has two modes: short and long, where short and long integration time values correspond to 55 µs and 110 µs, respectively. The selection of short or long integration time is performed via a 1-bit digital control input (*int_time_select*). Table 6.3 gives the gain adjustment of the SCI and corresponding dynamic ranges of the readout circuit for a 2.8 V output swing. When the integration time is selected as 55 µs (*int_time_sel* = 0) and the integration capacitance is set as 9.36 pF, then the readout can integrate currents up to 480 nA without saturation. With a transconductance value of 1000 µA/V, this corresponds to

480 μV infrared induced voltage change on the detector. Since the detector has a temperature sensitivity of -2 mV/K, this corresponds to an infrared induced temperature change of 240 mK on the detector in the FPA. Finally, this corresponds to about 376 K temperature variation in the scene. By using long integration time of 110 μs (*int_time_sel* = 1) and lowest integration capacitance (1.17 pF), the total output swing of the integrator can be assigned to a much narrower scene temperature range of 23.5 K. Using the variable gain integrator, maximum level of incident infrared radiation level can be increased about 16 times without causing any saturation. Figure 6.24 shows the transient simulation result of the SCI at different input current levels ranging from 0 nA to 100 nA. Integration gain is set to its maximum value by selecting long integration (110 μs) and by selecting the minimum integration capacitance (1.25 pF when *gain<1:0>* = 00). In this simulation, integrator reset voltage is set as 0.5 V. When the integration is disabled, the output preserves its previous value until the integration capacitor is reset. Due to the finite slew rate of the opamp used in the SCI, the output can not return to its reset voltage immediately, and a certain time is required for this process. Therefore, the next integration starts after allowing sufficient time for the transients to decay. When the integration is enabled, the integration starts, raising the output again from its reset value.

Table 6.3: Gain adjustment of the SCI and corresponding dynamic ranges of the readout circuit for a 2.8 V output swing.

Int_time_sel	**gain<1:0>**	**C_{int} (pF)**	**Gain (mV/nA)**	**I_{int_max} (nA)**	**ΔT_{det_max} (mK)**	**ΔT_{scene_max} (K)**
0	00	1.17	47	60	30	47
0	01	2.34	23.5	120	60	94
0	10	4.68	11.8	240	120	188
0	11	9.36	5.9	480	240	376
1	00	1.17	94	30	15	23.5
1	01	2.34	47	60	30	47
1	10	4.68	23.5	120	60	94
1	11	9.36	11.8	240	120	188

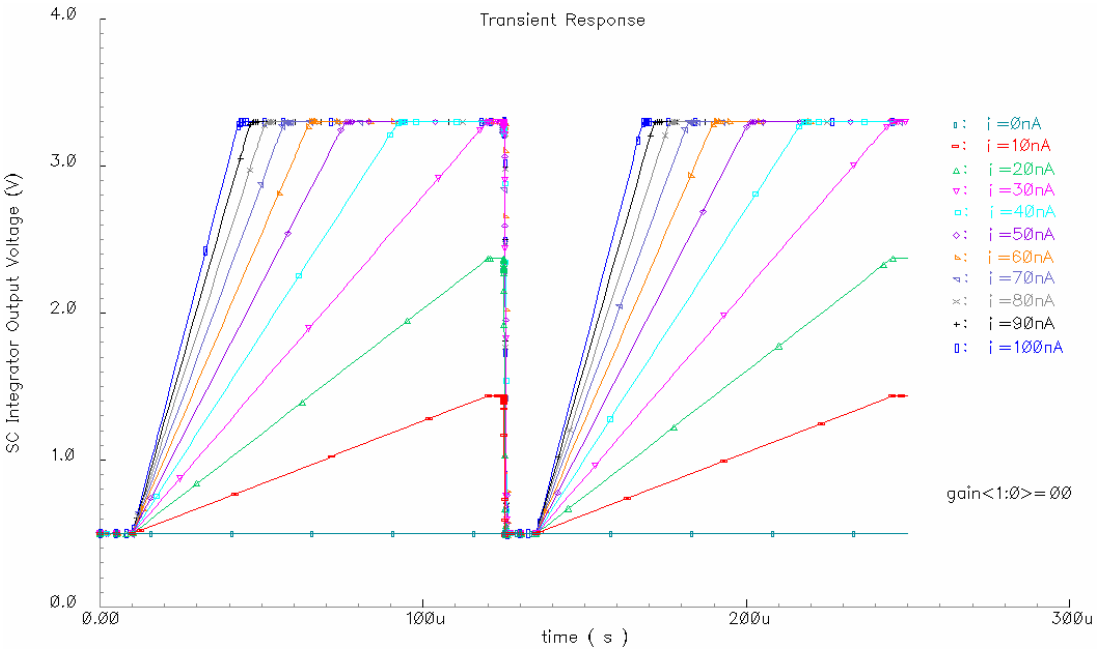


Figure 6.24: Transient simulation result of the SCI at different input current levels ranging from 0 nA to 100 nA. Integration gain is set to its maximum value by selecting long integration (110 µs) and the minimum integration capacitance (1.25 pF when *gain<1:0>* = 00).

Figure 6.25 shows the transient simulation result of the SCI at different input current levels ranging from 0 nA to 200 nA. Integration capacitance is set to its maximum value (10 pF when gain<1:0> = 11), and long integration is used.

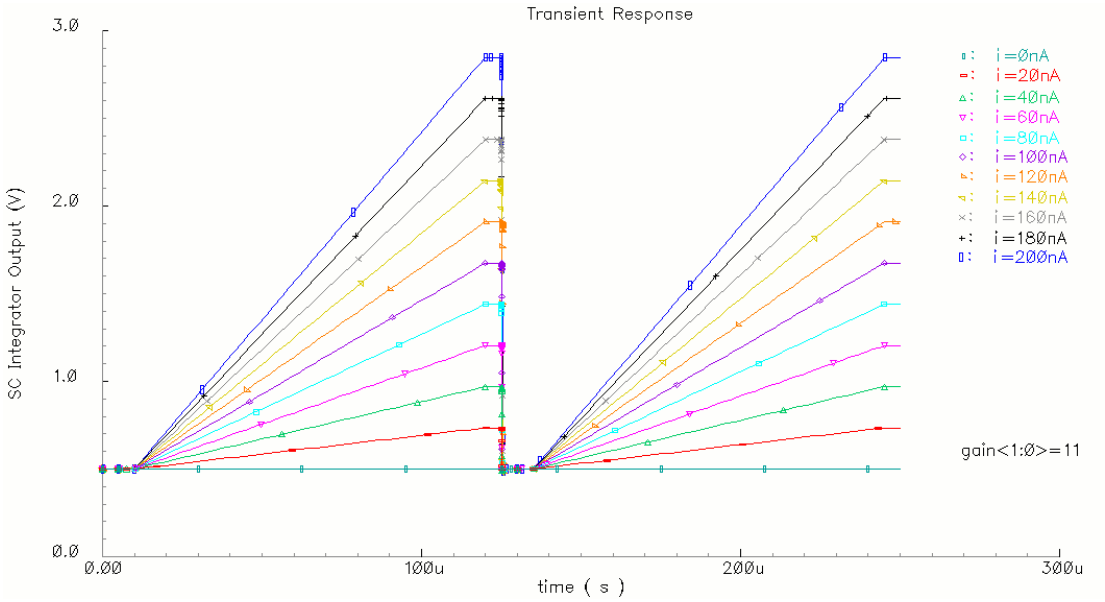


Figure 6.25: Transient simulation result of the SCI at different input current levels ranging from 0 nA to 200 nA. Integration capacitance is set to its maximum value (10 pF when *gain<1:0>* = 11), and long integration is used.

Figure 6.26 shows the layout of the variable gain SCI circuit. It is composed of an opamp, a capacitor bank, switches, and digital circuitry for gain control. The layout measures 140 µm × 300 µm in a 3-metal 2-poly 0.35 µm CMOS process. The opamp used in the integrator circuit is also used in other circuit blocks, and the design details of this opamp are given in the next section. Figure 6.27 shows the layout of the input stage of the channel readout circuit. It is composed of the differential pair of the GM stage, the load and bias transistors of the GM stage placed in the middle together with the offset removal circuitry, and the variable gain switched capacitor integrator circuit. The height of the latter blocks is smaller as compared to the bulky input differential pair in order to leave space to signal and bias routing between the blocks and adjacent channel readout circuits.

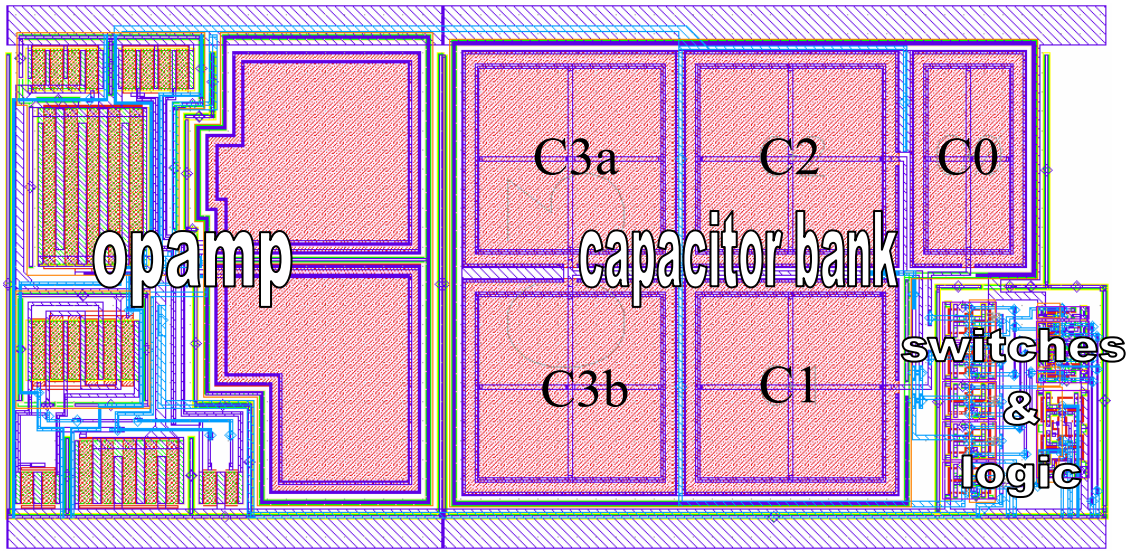


Figure 6.26: Layout of the variable gain switched capacitor integrator circuit. It is composed of an opamp, a capacitor bank, switches, and digital circuitry for gain control.

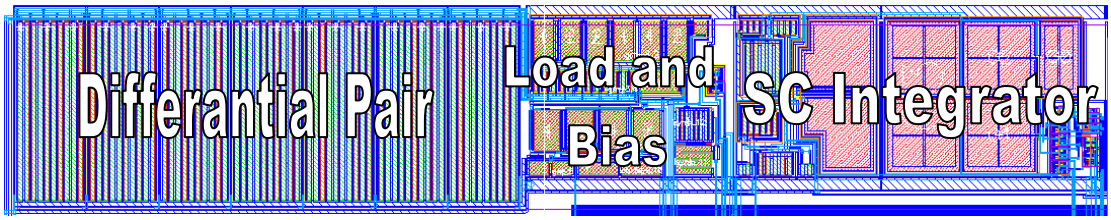


Figure 6.27: Layout of the input stage of the channel readout circuit. It is composed of the differential pair of the GM stage, the load and bias transistors of the GM stage placed in the middle together with the offset removal circuitry, and the variable gain switched capacitor integrator circuit.

6.5.3 Opamp

Figure 6.28 shows the schematic of the opamp used in various places in the FPA readout [73]. The opamp has a single ended class-AB output stage implemented with a common-source stage. The common source stage is preferred due to its large swing property as compared to the source-follower stages which are widely used in bipolar opamps due to their wide bandwidth high buffering capabilities. However, source-follower stages are difficult to use due their limited output voltage swings [73]. Since the designed opamp should operate at a single 3.3 V supply, source-follower stages are not considered, and common-source stages are used at the expense of reduced bandwidth and complicated design task. Compensation of this particular opamp has been carried out using Miller capacitances (C_1 and C_2). Table 6.4 gives the transistor device geometries used in the opamp circuit.

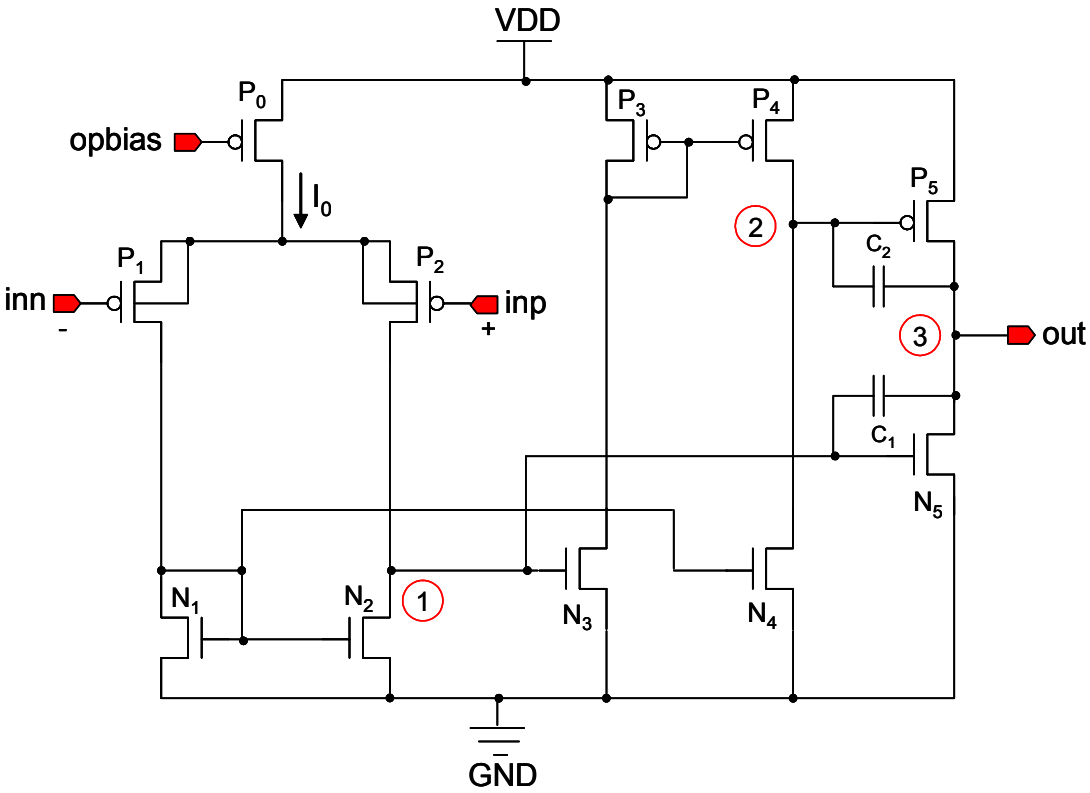


Figure 6.28: Schematic of the opamp used in various places in the FPA readout [73].

Table 6.4: Transistor device dimensions used in the opamp circuit.

MOS Transistors	W (µm)	L (µm)	# of Gates
$\mathbf{P_0}$	40	3	4
$\mathbf{P_1, P_2}$	45	3	3
$\mathbf{P_3, P_4}$	20	3	2
$\mathbf{P_5}$	200	3	5
$\mathbf{N_1, N_2, N_3, N_4}$	8	3	1
$\mathbf{N_5}$	80	3	5

The designed opamp circuit is composed of three stages: 1) differential input stage, 2) first gain stage, and 3) second gain stage, which also acts as an output stage. The output nodes of these stages are marked in Figure 6.28. Due to the common-source structure, the output resistance is not as low as that of the buffered opamps. However, it can still provide load current sufficient to drive resistive loads, provided that the load current does not exceed the quiescent current of the output stage. The input differential pair is realized using p-channel transistors (P_1 and P_2) implemented in a separate n-well region whose bulk terminal is connected to the source terminals, which eliminates any threshold variations and improves the power supply rejection ratio [73]. The input stage is biased by a p-channel transistor (P_0). The active load of the differential pair is a simple current mirror implemented with n-channel transistors (N_1 and N_2).

The differential input voltage is amplified related with the transconductance (g_{mi}) of the input transistors (P_1 and P_2) and the output conductance (g_{dP2} and g_{dN2}) of the P_2 and N_2 transistors. Neglecting the capacitive effects, the low frequency output voltage of the first stage (v_1) is given as

$$v_1 = \frac{g_{mi} v_i}{g_{dP2} + g_{dN2}} \tag{6.14}$$

where, g_{mi} is the transconductance of the input transistors (*P1* and *P2*), v_i is the differential input voltage, and g_{dP2} and g_{dN2} are the output conductance values of the *P2* and *N2* transistors, respectively.

The output of the differential input stage (v_1) is connected to the gate of the N_3, which converts the voltage signal to current signal copied by the P_3 to P_4, where the current signal is converted back to a voltage signal with an amplification factor related with the transconductance value of N_3 and output conductance values of P_4 and N_4. The low frequency voltage at the output of the second stage (v_2) is given as

$$v_2 = \frac{g_{mN3} v_1}{g_{dP4} + g_{dN4}} \tag{6.15}$$

where, g_{mN3} is the transconductance of *N3*, v_1 is the output voltage of the first stage, and g_{dP4} and g_{dN4} are the output conductance values of the *P4* and *N4* transistors, respectively.

It should be noted that N_4 is biased by the same gate voltage as N_1 and N_2, which implies that the bias current of these transistors can be adjusted depending on the ratio of *W/L* values. The bias current is mirrored back to N_3 via P_2 and P_3 pairs; therefore, the gate-to-source voltage of N_3 can be made same as N_1, provided that N_1, N_2, N_3, and N_4 have the same device dimensions. In fact, all the n-channel transistors except the N_5 have the same device dimensions. Matching the gate-to-source voltages also makes the drain-to-source voltages of N_1 and N_2 equal, improving the performance of the current mirror formed by N_1 and N_2.

The output stage is formed using common-source transistors *P5* and *N5*, which are biased at relatively high level as compared to the other transistors. This is necessary to decrease the output resistance and to widen the bandwidth of the opamp. The device dimensions of the output transistors are also selected large to decrease the gate overdrive voltage, and hence to improve the output swing. By increasing the device size and the bias level, their transconductance values are increased considerably, shifting the zero associated with the compensation capacitances C_1 and C_2 [71]. As a result of these, the gain of this stage is about an order of magnitude smaller as compared to the other stages. The low frequency output voltage of the last stage, which is also the opamp's output voltage, is given as

$$v_3 = v_{out} = \frac{g_{mP5} v_2 + g_{mN5} v_1}{g_{dP5} + g_{dN5}} \tag{6.16}$$

where, g_{mP5} and g_{mN5} are the transconductance values of *P5* and *N5*, v_1 and v_2 and are the output voltages for the first and second stages, and g_{dP5} and g_{dN5} are the output conductance values of the transistors *P5* and *N5*, respectively. Combining these three equations the overall low frequency gain (A_v) of the opamp is found as

$$A_v = \frac{g_{mi}}{g_{dP5} + g_{dN5}} \left(\frac{g_{mP5} g_{mN3}}{(g_{dP2} + g_{dN2})(g_{dP4} + g_{dN4})} + \frac{g_{mN5}}{g_{dP2} + g_{dN2}} \right) \tag{6.17}$$

where, the last term in the parenthesis can be neglected. The low frequency gain expression is simplified to

$$A_v \cong \frac{g_{mi} g_{mN3} g_{mP5}}{(g_{dP2} + g_{dN2})(g_{dP4} + g_{dN4})(g_{dP5} + g_{dN5})} \tag{6.18}$$

If the gain of each stage is designed as high as 40 dB, then the overall open loop gain of the opamp can be as high as 120 dB, which is more than enough for most of the applications. In fact, the gains of the stages are not equal, and the gain of the output stage is the least among them. Table 6.5 gives the simulated electrical parameters of the transistors involved in the low frequency open loop gain expression of the opamp circuit. In this simulation, the opamp bias voltage is set as 2.5 V, and the inputs are connected to 1.65 V, half the supply voltage. Using these parameters the gain of the first, second, and third stages are found as 476 V/V, 344 V/V, and 32 V/V, respectively. The product of these terms results an overall gain of 5.25×10^6 V/V (about 134 dB), which is sufficiently large for most of the applications.

Table 6.5: Simulated electrical parameters of the transistors involved in the low frequency open loop gain expression of the opamp circuit.

Transistors	g_m (µA/V)	g_d (nA/V)	I (µA)
P_1, P_2	63.9	51.1	4.65
P_4	46.9	94.4	4.65
P_5	460	13200	46.7
N_2, N_3, N_4	54.9	65.2	4.65
N_5	552	1098	46.7

For stable operation, the phase characteristics should be designed such that phase margin becomes larger than 45°, preferably above 60° [63, 71]. The required frequency compensation is performed by using Miller capacitances (C_1 and C_2). The addition of these capacitors pulls the low frequency pole closer to the origin and pushes the high frequency pole to much higher frequencies; hence, these capacitors are called pole-splitting capacitors [71]. In this particular design, C_1 and C_2 are selected as 2 pF. Figure 6.29 shows the simulated gain and phase plot of the compensated opamp. Low frequency open loop gain of the opamp when driving a 1 pF load is recorded as 131 dB with a unity gain frequency of 4.1 MHz and phase margin of 67°. Markers show the data points where the gain is about unity (0 dB).

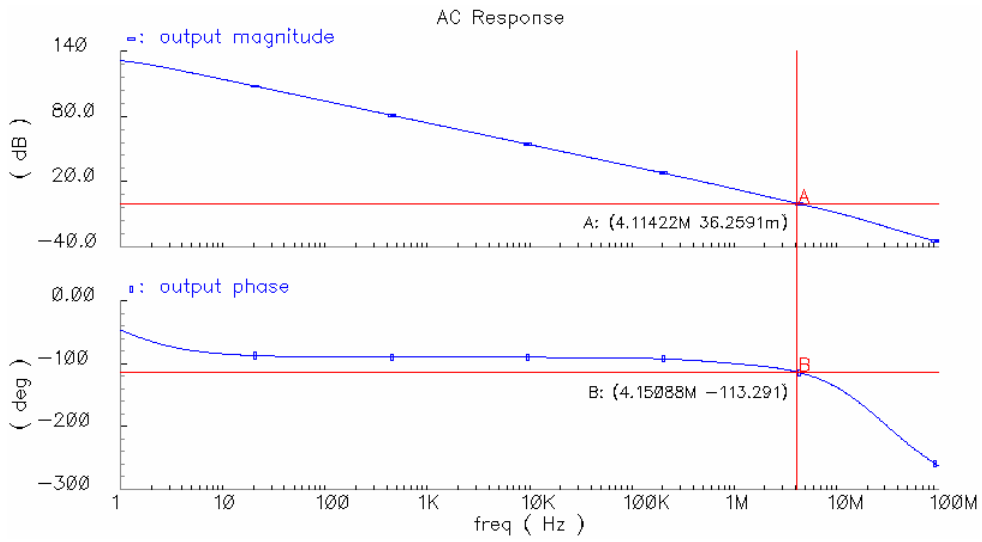


Figure 6.29: Simulated gain and phase plot of the compensated opamp. Low frequency open loop gain of the opamp when driving a 1 pF load is recorded as 131 dB with a unity gain frequency of 4.1 MHz with a phase margin of 67 °. Markers show the data points where the gain is about unity (0 dB).

The noise analysis of the opamp can be performed in a similar manner as have been given for the differential transconductance amplifier (GM circuit) in Section 6.5.1. Both of the circuits have basically same differential stage, with the only difference being that the p-channel and n-channel devices are swapped in the opamp circuit. In other words, the differential stage is implemented with p-channel devices biased by a p-channel device, and the active loads are implemented with n-channel devices. Based on the results of the noise analysis performed for the GM circuit, input referred noise can be minimized by increasing the transconductance of the input transistors, and by decreasing the transconductance of the load transistors. The input referred noise of the opamp calculated at the detector terminals is considerably small due to the high transconductance and high output resistance of the differential transconductance amplifier. Any noise voltage referred to the non-inverting terminal of the opamp causes a noise current inversely proportional with the output resistance of the GM circuit, which was found to be larger than 1 MΩ. Therefore, the generated noise current is negligibly small, and the input referred noise voltage to the detector terminals will be lower due to the high transconductance value of the GM circuit.

The output noise voltage of the opamp can be expressed as the superposition of the associated gate referred noise powers of each transistor in the opamp schematic given in Figure 6.28 [63, 71]. Among them, the noise contribution of the bias transistor is neglected since it acts as a common mode signal as mentioned previously for the low-noise differential transconductance amplifier. The total output noise voltage of the opamp is given as

$$v_{out}^2 = A_v^2 \left(\begin{array}{l} \frac{1}{\beta_1^2}(v_{P1}^2 + v_{P2}^2) + \frac{1}{\beta_2^2}(v_{N1}^2 + v_{N2}^2) + \frac{1}{\beta_3^2} v_{N3}^2 + \frac{1}{\beta_4^2}(v_{P3}^2 + v_{P4}^2) + \frac{1}{\beta_5^2} v_{N4}^2 \\ + \frac{1}{\beta_6^2} v_{P5}^2 + \frac{1}{\beta_7^2} v_{N5}^2 \end{array} \right) \quad (6.19)$$

$$\begin{bmatrix}\beta_1\\ \beta_2\\ \beta_3\\ \beta_4\\ \beta_5\\ \beta_6\\ \beta_7\end{bmatrix} = \begin{bmatrix} 1 \\ g_{mi}/g_{mN2} \\ g_{mi}/(g_{dP2}+g_{dN2}) \\ g_{mi}g_{mN3}/\left(g_{mP4}(g_{dP2}+g_{dN2})\right) \\ g_{mi}g_{mN3}/\left(g_{mN4}(g_{dP2}+g_{dN2})\right) \\ g_{mi}g_{mN3}/\left((g_{dP2}+g_{dN2})(g_{dP4}+g_{dN4})\right) \\ g_{mi}g_{mN3}g_{mP5}/\left(g_{mN5}(g_{dP2}+g_{dN2})(g_{dP4}+g_{dN4})\right) \end{bmatrix} \tag{6.20}$$

where, A_v is the open loop gain of the opamp, v_P and v_N are gate referred noise voltages of the indicated transistors, β is the ratio of the gain for the noise voltage of the transistors measured at the output with respect to the open loop gain. Input referred noise of the opamp can be found by dividing the total output noise voltage to the open loop gain of the opamp, and it is given as

$$v_{in}^2 = \left(\begin{array}{l} \frac{1}{\beta_1^2}(v_{P1}^2+v_{P2}^2)+\frac{1}{\beta_2^2}(v_{N1}^2+v_{N2}^2)+\frac{1}{\beta_3^2}v_{N3}^2+\frac{1}{\beta_4^2}(v_{P3}^2+v_{P4}^2)+\frac{1}{\beta_5^2}v_{N4}^2 \\ +\frac{1}{\beta_6^2}v_{P5}^2+\frac{1}{\beta_7^2}v_{N5}^2 \end{array} \right) \tag{6.21}$$

which is equal to the term given in the parenthesis of Equation 6.19. As expected, the transistors that are far away from the input stage (N_3, P_3, P_4, N_4, P_5, and P_6) contribute less to the input referred noise voltage, which can be given approximately as

$$v_i^2 \cong v_{P1}^2 + v_{P2}^2 + \left(\frac{g_{mN2}}{g_{mi}}\right)^2 (v_{N1}^2+v_{N2}^2) \tag{6.22}$$

where, v_P and v_N are gate referred noise voltages of the p-channel and n-channel MOS transistors given previously in Equation 6.8. Figure 6.30 shows the simulated opamp input noise power spectral density from 0.1 Hz to 100 kHz. Total rms noise in 4 kHz bandwidth is simulated as 5.16 μV, which has an average noise spectral density of 81 nV/√Hz. For 8 kHz bandwidth, total integrated noise is found as

5.6 µV with a density of 63 nV/√Hz. For wide bandwidth applications noise spectral density becomes less than 30 nV/√Hz. In addition to that, the low frequency output noise of the opamp is cancelled by the use of a correlated double sampling circuit (CDS), which will also help to decrease the actual opamp noise to lower levels suggested by the simulation results performed without the CDS circuit [76]. Table 6.6 gives the simulated parameter summary of the opamp circuit.

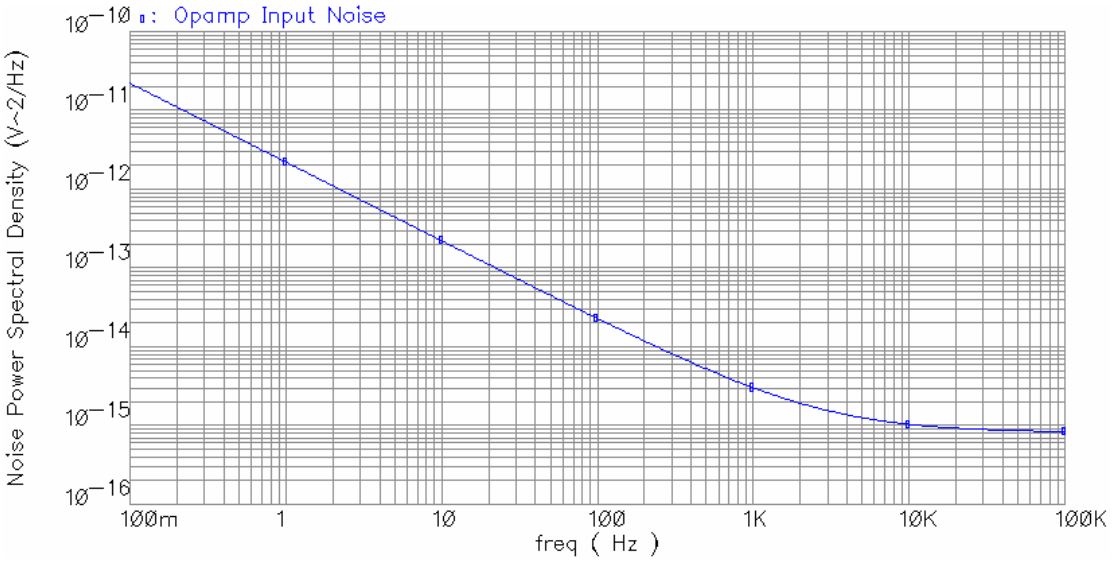


Figure 6.30: Simulated opamp input noise power spectral density from 0.1 Hz to 100 kHz. Total rms noise in 4 kHz bandwidth is simulated as 5.16 µV, which has an average noise spectral density of 81 nV/√Hz. For 8 kHz bandwidth, total integrated noise is found as 5.6 µV with a density of 63 nV/√Hz. For wide bandwidth applications noise spectral density becomes less than 30 nV/√Hz.

Other important parameters of the opamp are the slew rate, input common mode voltage, output voltage swing, power supply rejection ratio (PSRR), common mode rejection ratio (CMRR), and power dissipation. The slew rate of the opamp is simulated to be better than 3.3 V/µs, which indicates that the output can swing rail-to-rail within less than 1 µs sufficient for the 64 × 64 FPA readout circuits where the pixel processing time is larger than 50 µs in the fastest operation mode. The input common mode of the opamp is found by simulation to be starting from about 0 V and reaching up to 2.8 V for a single 3.3 V supply, being limited at the positive supply side. Output voltage swing is simulated to be 40 mV above the negative supply (0 V) and 100 mV below the positive supply (3.3 V). The designed opamp

has a simulated PSRR value of 129 dB at low frequencies, indicating about unity gain from supply to the output [75]. The CMRR of the designed opamp is simulated as 162 dB at low frequencies [75]. The designed opamp draws 65 μA from a single 3.3 V power supply, and most of the power dissipation occurs at the output stage since its quiescent bias current is 47 μA, which is about 72 % of total supply current. Total DC power dissipation of the opamp is 0.21 mW, which can be minimized considerably at the expense of increased output resistance and decreased load driving capability. At this bias level the output resistance of the opamp is simulated as 47 kΩ in the open loop configuration, which is better than the typical values that of the unbuffered opamps. This value decreases down to 13 mΩ when the opamp is operated in the unity gain buffer mode, which is an expected result based on the feedback theory [57, 63]. Table 6.6 gives the simulated parameter summary for the opamp circuit.

Table 6.6: Simulated parameter summary for the opamp circuit.

Process	AMS 0.35 μm 3M2P CMOS
Size	140 μm × 113 μm
Power Supply	Single 3.3 V
Power Dissipation	210 μW
Open Loop Gain	131 dB
Phase Margin	67°
Unity Gain Frequency	4.1 MHz (1 pF load)
Slew Rate	3.30 V/μs (low-to-high) -3.45 V/μs (high-to-low)
PSRR	129 dB at DC
CMRR	162 dB at DC
Input Common Mode Voltage	$0 < V_{in} <$ VDD – 0.5 V
Output Voltage Swing	40 mV $< V_{out} < V_{DD} -$ 100 mV
Output Resistance	47.5 kΩ (open loop DC) 13 mΩ (buffer connected)
Input Referred Noise	81 nV/√Hz (0.1 Hz-4 kHz) 30 nV/√Hz (0.1 Hz-1 MHz)

Figure 6.31 shows the layout of the designed opamp. It measures 140 µm × 113 µm in a 0.35 µm 3M2P CMOS process. The transistors are drawn in stacked manner to minimize the implementation area [72, 73].

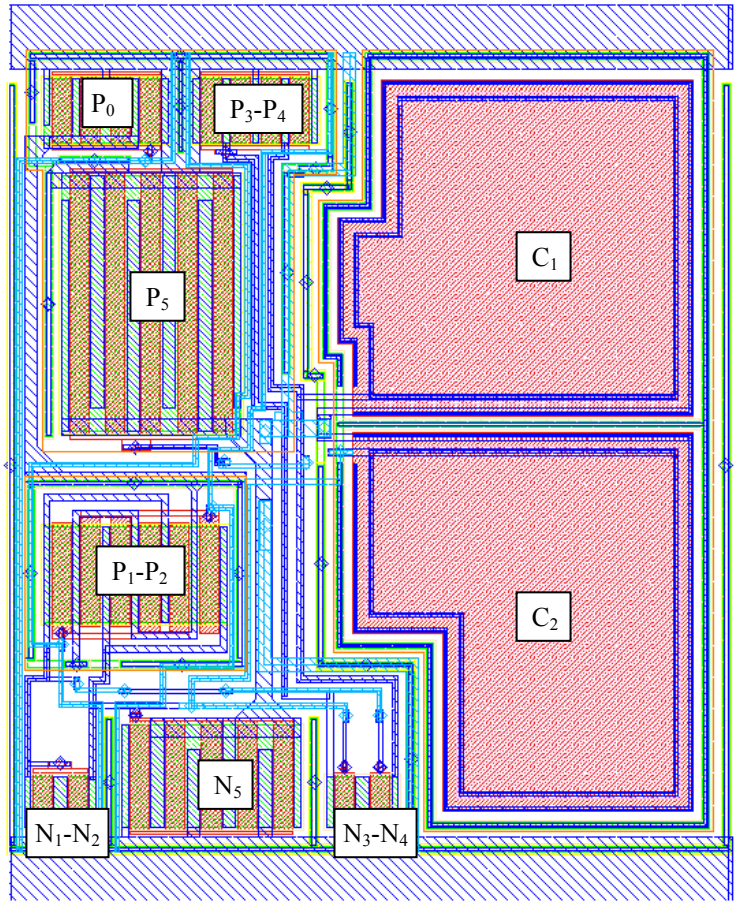


Figure 6.31: Layout of the designed opamp. It measures 140 µm × 113 µm in a 3-metal 2-poly 0.35 µm CMOS process.

6.5.4 Correlated Double Sampling (CDS) Circuit

Correlated double sampling (CDS) circuit is used to remove the offset and low frequency correlated noise in the input signals by performing two successive measurements and eliminating the above mentioned undesired components from the input signal. In the 64 × 64 FPA readout, it is used to filter out the low frequency noise and offset in the switched capacitor integrator circuit, which does not have any auto-zero features. Figure 6.32 shows the simplified schematic view of the switched

capacitor correlated double sampling (CDS) circuit designed to be used in the 64 × 64 FPA readout circuit. It is implemented using an opamp, two sampling capacitors, and four CMOS switches with dummy transistors. To reduce the switch induced noise, the capacitors are selected as 1.5 pF, and the minimum sized transistors are used in the switches.

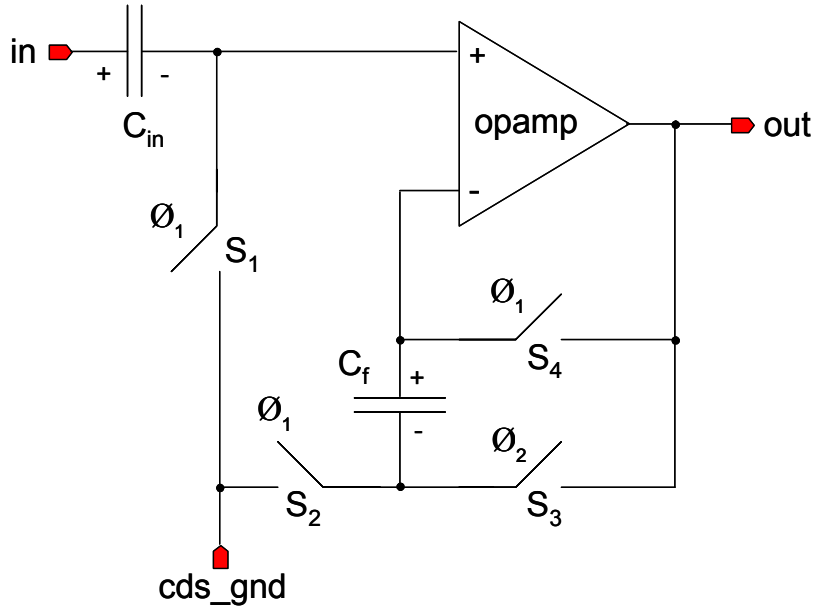


Figure 6.32: Simplified schematic view of the switched capacitor correlated double sampling (CDS) circuit used in the 64 × 64 FPA readout circuit.

The timing of the designed switched capacitor circuit is performed by using a non-overlapping two phase clocking scheme indicated as $Ø_1$ and $Ø_2$ in the schematic given below. During $Ø_1$, S_1, S_2, and S_4 are turned on. At $Ø_1$, C_{in} is samples the input voltage with respect to a reference voltage (*cds_gnd*), and at the same time C_f samples the input noise of the opamp, which is connected in the unity gain buffer mode at $Ø_1$. At $Ø_2$, only S_3 is turned on, which passes the signal at its non-inverting terminal by removing the offset at this terminal with the help of offset stored across C_f during previous period of $Ø_1$. Similarly, the input signal is passed to the non-inverting terminal of the opamp after its offset voltage is cancelled by the value stored across C_{in} at $Ø_1$. This verifies that the output of the CDS circuit is free of the offset voltages and correlated noise voltages coming from the input signal and from

the opamp used in the CDS circuit. Table 6.7 gives the capacitor and output voltages at different clock phases in the CDS circuit. It should be mentioned that the gain of the CDS circuit is unity independent of the capacitance ratios for Cin and Cf, which are selected as 1.5 pF.

Table 6.7: Capacitor and output voltages at different clock phases in the CDS circuit.

	$Ø_1$	$Ø_2$
V_{in}	V_{in_off}	$V_{in\_off} + V_{in\_signal}$
C_{in}	$V_{in\_off} - V_{cds\_gnd}$	$V_{in\_off} - V_{cds\_gnd}$
C_f	V_{op_off}	V_{op_off}
V_{out}	$V_{cds\_gnd} + V_{op\_off}$	$V_{in\_signal} + V_{cds\_gnd}$

Figure 6.33 shows the simulation result of the CDS circuit where the output of the integrator is connected to the input of the CDS circuit. The circuit is capable to cancel the offset at the input and at the integrator output.

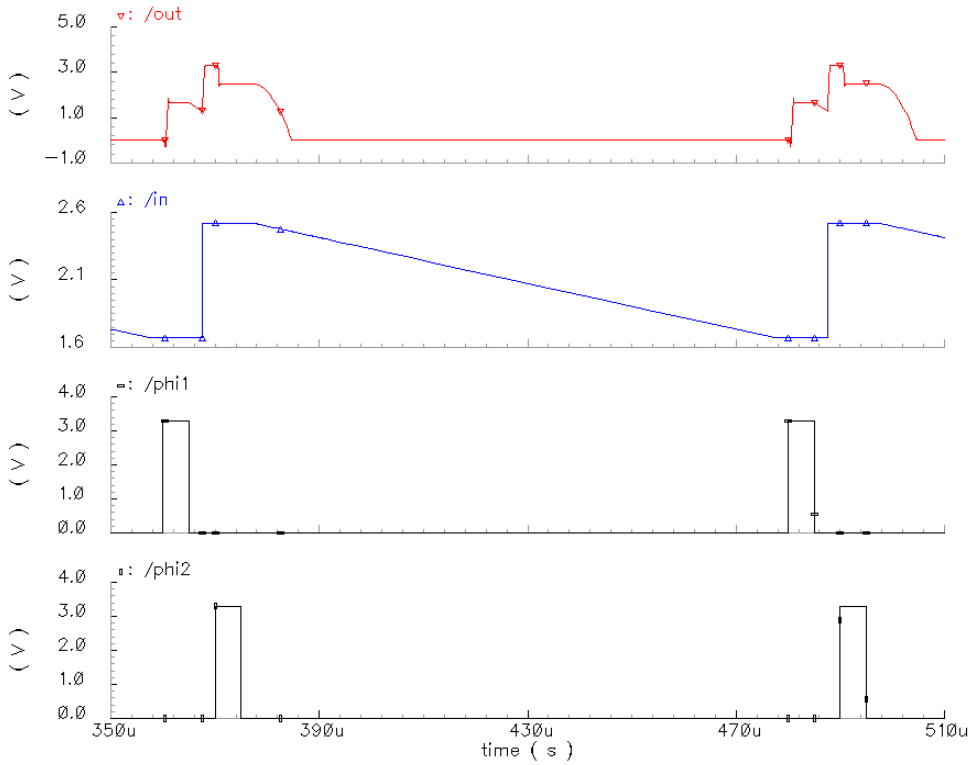


Figure 6.33: Simulation result of the CDS circuit. The output of the integrator is connected to the input of the CDS circuit. The circuit is capable to cancel the offset at the input and at the integrator output.

Figure 6.34 shows the layout of the CDS circuit. It is composed of an opamp, two sampling capacitors (C_{in} and C_f), and four analog CMOS switches with dummy transistors. The layout measures 140 µm × 190 µm in a 3-metal 2-poly 0.35 µm CMOS process. The empty area on top of the CMOS switches on the left of the layout is used by the sample and hold amplifier which is not included here.

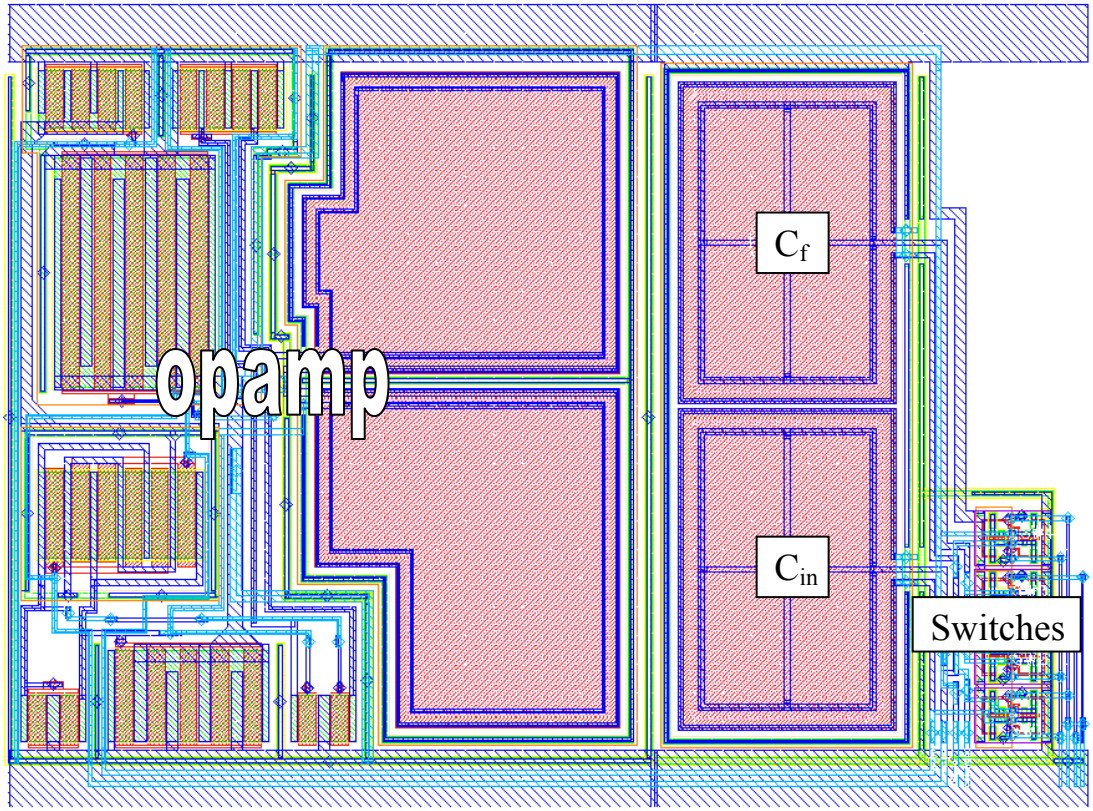


Figure 6.34: Layout of the CDS circuit. It is composed of an opamp, two sampling capacitors (C_{in} and C_f), and four analog CMOS switches with dummy transistors. The layout measures 140 µm × 190 µm in a 3-metal 2-poly 0.35 µm CMOS process.

6.5.5 Sample-and-Hold (S/H) Amplifier

The sample-and-Hold (S/H) amplifier is used to sample the output of the integrator so that it can be stored for output multiplexing, while integrator starts to process the next pixel upon a reset operation. In the 64 × 64 FPA, the CDS output remains the same during 125 µs neglecting the reset time of the S/H circuit necessary for offset removal. During this period, output multiplexer scans the 16 column outputs from left to the right of the FPA. Therefore, if S/H were not used, the

sampled integrator outputs should be frozen for about the same period, which will slow down the scanning operation. Figure 6.35 shows the simplified schematic of the switched capacitor sample-and-hold (S/H) circuit with offset cancellation feature used in the 64 × 64 FPA [63]. The circuit is composed of an opamp, a sampling capacitor (C_{SH}), and three CMOS switches with dummy transistors. The CMOS switches are controlled by three different timing signals ($Ø$, $Ø_d$, and complement of $Ø$), which are generated from a single clock signal by a simple inverter circuit.

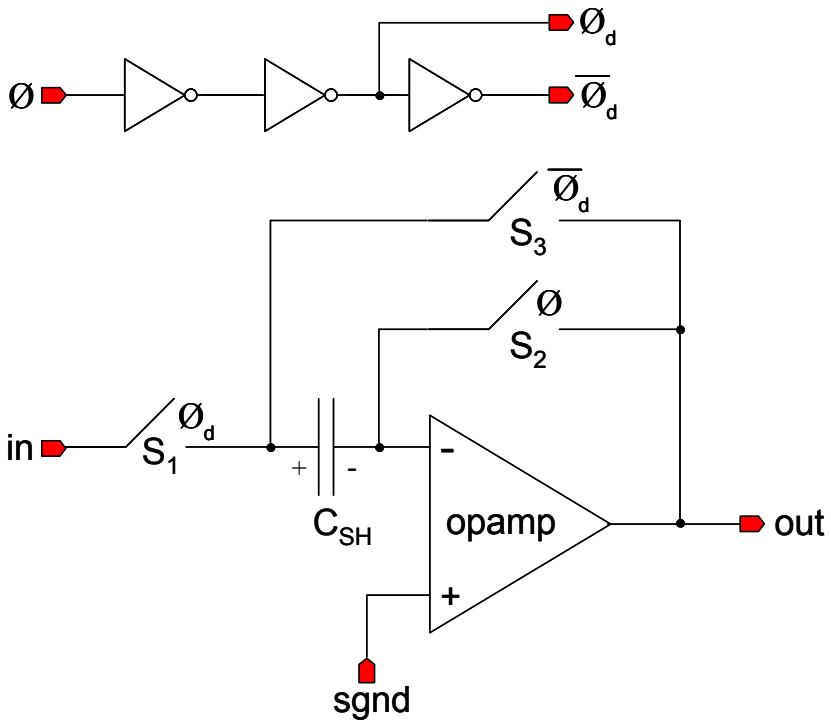


Figure 6.35: Simplified schematic of the switched capacitor sample-and-hold (S/H) circuit with offset cancellation feature used in the 64 × 64 FPA readout circuit [63]. The CMOS switches are controlled by three different timing signals ($Ø$, $Ø_d$, and its complement $\overline{\Phi}_d$), which are generated from a single clock signal by a simple inverter circuit.

The operation of the circuit is best understood when we assume that $Ø$ and the delayed version of it ($Ø_d$) are identical signals. During $Ø$, S_1 and S_2 are turned on, and the C_{SH} samples the difference of the input voltage and reference potential including the offset voltage of the opamp. During the complementary phase ($\overline{\Phi}_d$), C_{SH} is connected in the negative feedback loop so that the opamp offset is cancelled

by the previously sampled opamp offset voltage. Hence, the output follows the input without any offset and low frequency noise of the opamp used. Table 6.8 gives the capacitor and output voltages of the S/H circuit at different clock phases. Figure 6.36 shows the simulation result of the S/H amplifier. The input (*in*) is a 1 V peak-to-peak sine wave at 1 kHz with DC value of 1.65 V. The circuit samples the input signal and holds it at the output at the positive and negative edges of the applied clock signal (*Ø* = *phi2*), respectively. The circuit is reset, when the clock signal is high, which starts at the same time that the input is sampled. During reset operation, S/H output is equal to the reference signal used (V_{SH_gnd}), which is selected to be equal to 1.65 V, half of the supply voltage in this simulation.

Table 6.8: Capacitor and output voltages of the S/H circuit at different clock phases.

	$Ø_1$	$\overline{\Phi}$
C_{SH}	$V_{in} - V_{SH\_gnd} - V_{op\_off}$	$V_{in} - V_{SH\_gnd} - V_{op\_off}$
V_{out}	$V_{SH\_gnd} + V_{op\_off}$	V_{in}

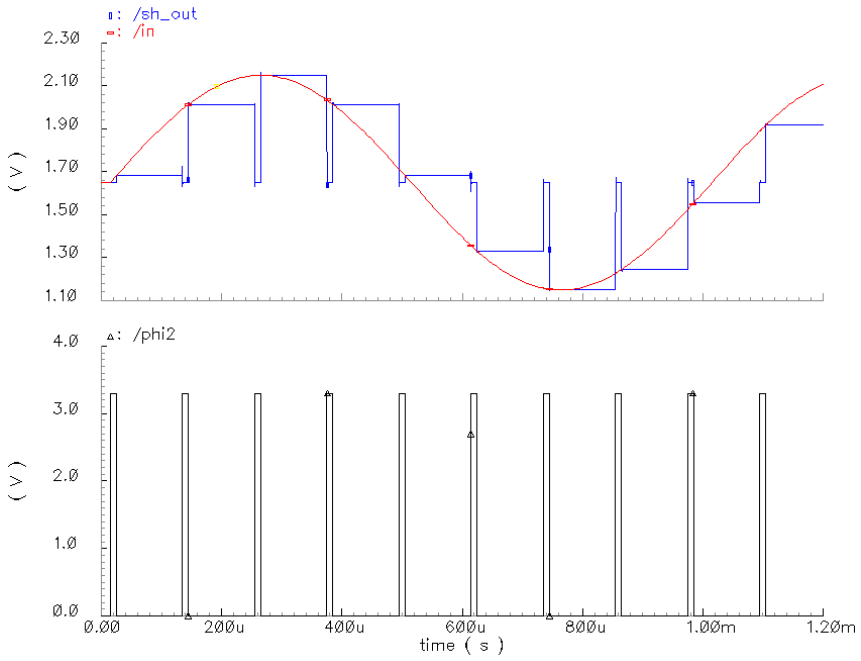


Figure 6.36: Simulation result of the S/H amplifier. The input (*in*) is a 1 V peak-to-peak sine wave at 1 kHz with DC value of 1.65 V. The circuit samples the input signal and holds it at the output at the positive and negative edges of the applied clock signal (*Ø* = *phi2*), respectively.

Figure 6.37 shows the layout of the S/H circuit. It is composed of an opamp, a sampling capacitor (C_{SH}), and three analog CMOS switches with dummy transistors. The layout measures 140 µm × 170 µm in a 3-metal 2-poly 0.35 µm CMOS process. The layout has been flipped vertically in order to utilize the unused area on top of the CDS switches when the two blocks are placed next to each other.

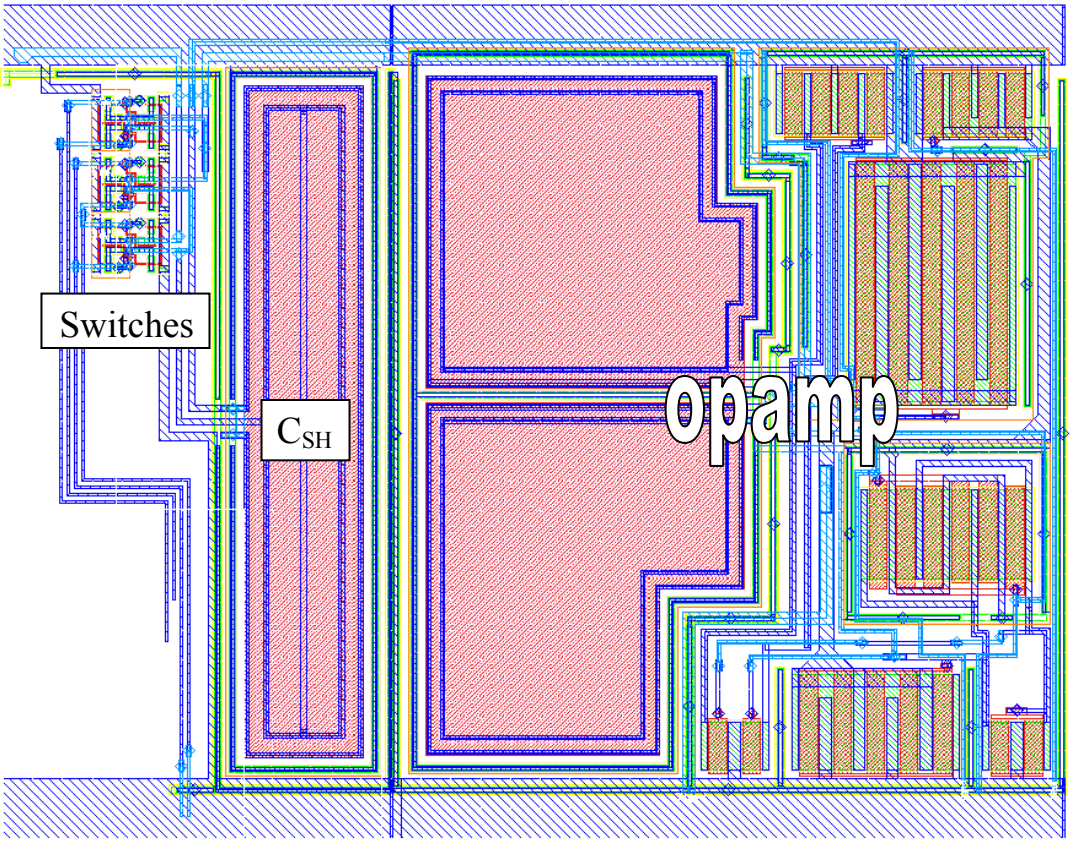
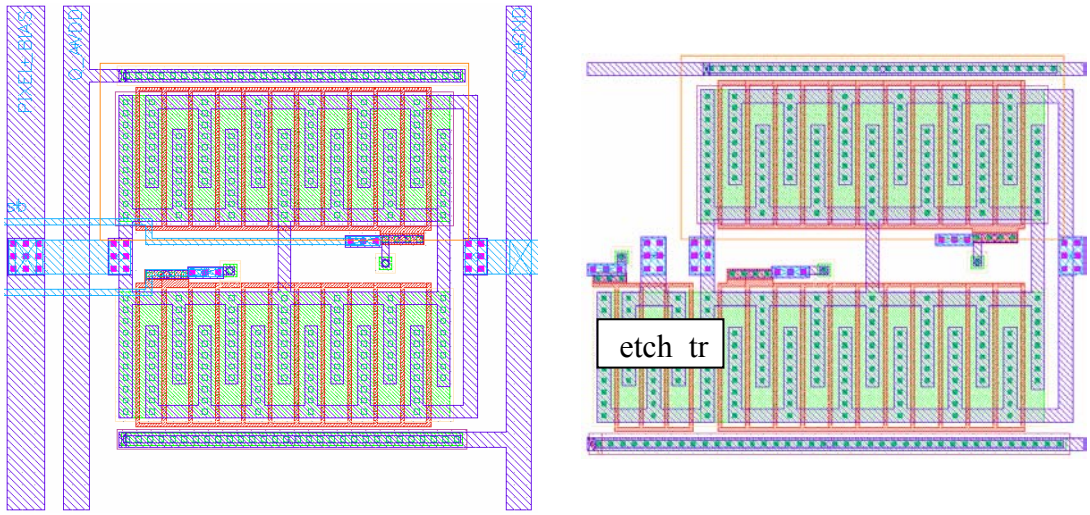


Figure 6.38: Layout of the S/H circuit. It is composed of an opamp, a sampling capacitor (CSH), and three analog CMOS switches with dummy transistors. The layout measures 140 µm × 170 µm in a 3-metal 2-poly 0.35 µm CMOS process.

6.5.6 Analog Multiplexers and Etch Transistors

Analog multiplexers are transmission gates with sufficient device dimensions to handle all the array bias currents without much voltage drop and with negligible electrical noise [47]. These switches are used in the row and column addressing circuitry on the left and on the top of the 64 × 64 FPA. The switches used in the row

select circuitry carry all the FPA bias current for the 16 channels that are scanned in parallel. Therefore, the horizontal switches should be capable of carrying as much as 160 µA current with negligible voltage drop and electrical noise contribution. Figure 6.39 shows the layout of the analog CMOS switches used in the (a) row and (b) column multiplexer circuitry. Column select switches have also an additional n-cannel transistor used to bias the n-wells of the array pixels during electro-chemical etching process. The designed *W*/*L* ratio of the p-channel and n-channel transistors in the analog switches is 120 µm / 0.3 µm. The simulated small signal resistance of the CMOS switches are 51 Ω, which is sufficiently small for the required analog multiplexing operations.



(a) (b)

Figure 6.39: Layout of the analog CMOS switches used in the (a) row and (b) column multiplexer circuitry. Column select switches have also an additional n-cannel transistor used to bias the n-wells of the array pixels during electro-chemical etching. The designed *W*/*L* ratio of the p-channel and n-channel transistors in the analog switches is 120 µm / 0.3 µm.

Figure 6.40 shows the simplified schematic of the FPA addressing circuit together with the etch transistors. During etching the *etch_enb* signal is high, and all the cathodes (n-well connections) of the array pixels are shorted to a common bias potential (*etch_bias*) that prevents etching of the n-well. During normal operation I_0 and mI_0 flow through the column switch and row switches, if there are *m* pixels read out in parallel. The etch transistor is implemented with an n-channel transistor which

can easily be operated by applying *etch_enb* and *etch_bias* potentials, whose absolute value depend on the potential applied to the chip substrate. The etching transistor can not be implemented using complementary transistors in parallel, because this will require an extra potential to be applied during etching. This complicates the preparation of the fabricated die for etching since every bias connections should be isolated from the etching solution by covering the bonding pads and the bonding wires.

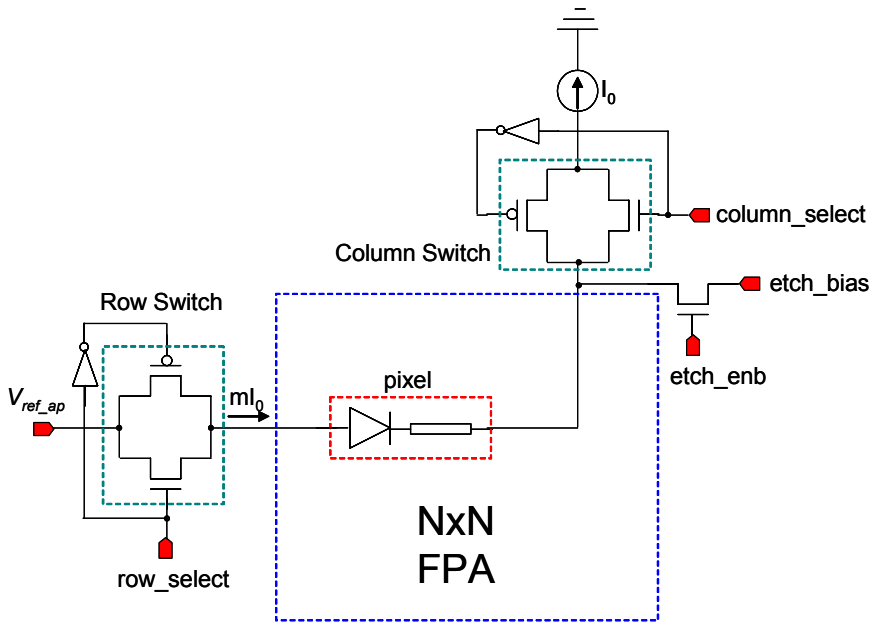


Figure 6.40: Simplified schematic of the FPA addressing circuit together with the etch transistors. During etching the *etch_enb* signal is high, and all the cathodes (n-well connections) of the array pixels are shorted to a common bias potential (*etch_bias*) that prevents etching of the n-well.

In the 64 × 64 FPA, there are 64 row switches and 64 column switches, where each of them is connected to one of the rows and columns of the FPA. The etch transistors are placed in each column switch. The row switch is tied to a common reference potential, and each pixel in the FPA is biased at a constant current level of 10 µA. Considering the fact that *m* is 16 for this FPA, the current flowing through the row switch becomes 160 µA. The next section explains the designed and integrated digital circuitry, which generates all the required control signals for the pixel selection, and timing signals for the switched capacitor circuits and multiplexers in the analog channel readout circuits.

6.6 Digital Scanning Circuitry

Figure 6.41 shows the block diagram of the 64 × 64 FPA readout circuit including the FPA, row and column multiplexers, the 16-channel parallel analog readout circuit, and the output multiplexer, which are controlled by the digital circuit. The digital circuit is composed of a synchronous counter, a combinational timing circuit, a synchronous sampler, and a number of shift registers to control the row and column selection in the FPA, and to control the serial output multiplexing operation. The digital circuitry is implemented using semi-custom design technique by using the required logic gates from the digital standard cell library of the AMS 0.35 µm CMOS process [77].

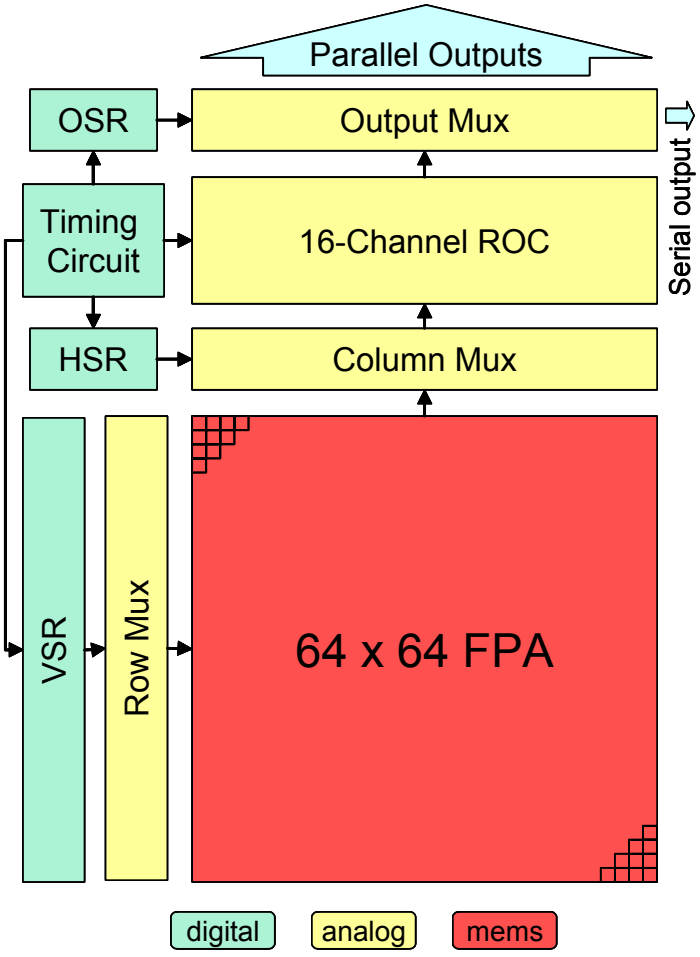


Figure 6.41: Block diagram of the 64 × 64 FPA readout circuit including the array pixels, row and column multiplexers, the 16-channel parallel analog readout circuit, and the output multiplexer, which all are controlled by the digital circuit.

The digital control and timing signals are generated by a synchronous binary counter, followed by a combinational circuitry that generates the required digital signals. These combinational signals are sampled by a synchronous sampler to avoid any problems that may arise due to the delays in between the blocks. The FPA rows are selected by the row multiplexers controlled by the vertical shift register (VSR). Similarly, columns are controlled by the analog column multiplexers controlled by the horizontal shift register (HSR). The serial multiplexed output is generated by the analog output multiplexer controlled by the output shift register (OSR). The details of the timing circuits and the shift registers will be described next.

6.6.1 Digital Timing Circuit

Figure 6.42 shows the block diagram of the digital timing circuit composed of a synchronous counter, a combinational circuit that generates the required timing signals using the counter outputs, and a sampling circuit operating at the negative clock edge. The use of a two phase clocking scheme improves the system immunity to propagation delays between the digital blocks. The sampled timing signals are used to control the operation of the shift registers and analog readout circuit blocks.

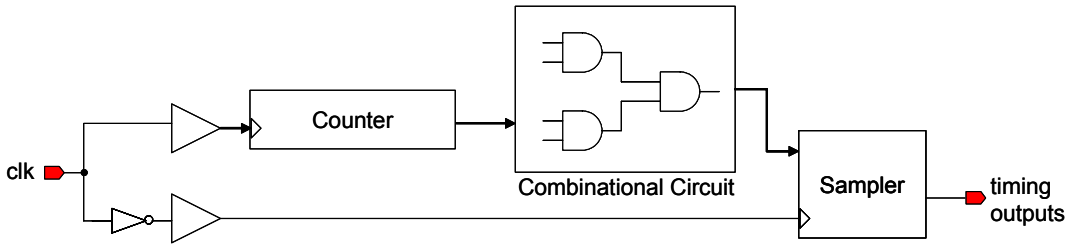


Figure 6.42: Block diagram of the digital timing circuit composed of a synchronous counter, a combinational circuit that generates the required timing signals using the counter outputs, and a sampling circuit which is operating at the negative clock edge.

In the 64 × 64 FPA, one frame time is divided into 64 × 4 sub time intervals equal to the pixel select time. Furthermore, 8 clock cycles are assigned for each individual pixel multiplexed to the output, which will simplify the required interfacing to external data acquisition systems. Since there are 16 pixels to be

scanned by the serial output registers when a single pixel is biased and integrated, the actual pixel time is 128 clock cycle long. Since there are 4 pixels assigned for each readout channel, 512 clock cycles are required for a single row, which corresponds to 32768 clock cycles for a single frame. To be able to generate all these timings a 15-bit counter is required. Figure 6.43 shows the internal register content of the 15-bit counter. The first 6 bits are for the addressing of 64 rows, 2 bits are for the addressing of 4 columns, 4 bits are for the addressing one of the 16 output channels, and the last 3 bits are for the precision timing allowing 8 clock cycles per a single pixel multiplexed to the serial output. For 30 fps scanning rate the required system clock frequency is 983040 Hz (about 1 MHz).

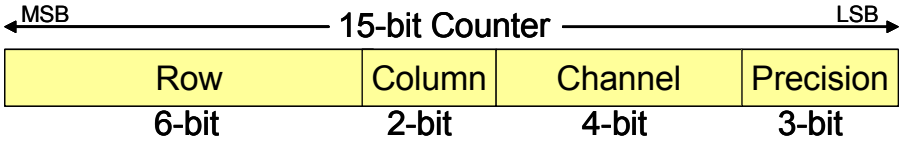


Figure 6.43: Internal register content of the 15-bit counter.

6.6.2 Shift Registers (VSR, HSR, and OSR)

There are three shift registers in the digital scanning circuit: 1) the vertical shift register (VSR) used for row selection, 2) the horizontal shift register (HSR) used for column selection, and 3) the output shift register (OSR) used for channel selection. The structures of these shift registers are same, and they only differ in word length. Among them, VSR is the largest whose resisters are 64-bit wide allowing addressing of the FPA rows. The HSR is only 4-bit wide, allowing addressing of the columns in the 64 × 4 sub arrays. The OSR is 16-bit wide allowing addressing of the readout channels. The content of these shift registers are zero for all the bits except for the bit location used a address a particular position. For example to select the first pixel in a row in a given readout channel is selected by loading a binary data of “1000” to the HSR. As this data is shifted to the right by one bit at each time, other pixels in the selected row of a particular sub-array are selected. The same operation is valid for other registers as well.

To control each of these registers two control signals are required: enable and load. When the enable signal is high, the content of the register shifts one bit to the right. When the load signal is high, binary one is loaded into the least significant bit of the registers. It should also be mentioned that both enabling and loading operations are synchronous and take place at the proper edge of the clock input. Since there are three shift registers in the digital scanning circuitry, the required number of the control signals would be at most six. Considering the fact that some of them may be used in common, the number of control signals can be reduced.

The required signal patterns for the registers vary depending on the word length of the register and the operation frequency. Among these registers, the OSR register is the one whose content is shifted and rotated at the fastest rate. It holds its content for 8 clock cycles at each positions of the shift register, and completes its full cycle operation in 128 clock cycles and returns to the initial position. The content of the HSR is updated whenever the OSR completes its full cycle, reducing its operation rate by a factor of 16 as compared to the OSR. The HSR completes its full cycle in 4 shift operations, lasting 512 clock cycles where the HSR stays at each state for 128 clock cycles equal to the full period of OSR. The VSR has the slowest operation rate, and its content is updated whenever the HSR completes a full cycle operation; therefore, it holds its states for 512 clock cycles. The VSR completes its full cycle in 64 shift operations, which also corresponds to the frame period lasting for 32768 clock cycles. At 30 fps scanning rate, the above operations are repeated 30 times in a second, requiring a 983040 Hz (about 1 MHz) system clock. Figure 6.44 shows the block diagram of the shift registers of OSR, HSR, and VSR together with their common control signals of *sme*, *hse*, *hsl*, and *vls*. In the actual design, the load signal of a faster register, i.e. the one whose content is updated faster, can be used as an enable signal of a slower register. Therefore, the required number of the control signals is less than six for the three shift registers. In fact, only four signals are enough to control all of the shift registers. These are the enable signal for the serial OSR (*sme*), enable and load signals for the HSR (*hse* and *hsl*), and finally the load signal of the VSR (*vsl*). The *hse* and *hsl* signals for the HSR are in common with the OSR's load (*Load*) signal and VSR's enable (*Enb*) signal, respectively.

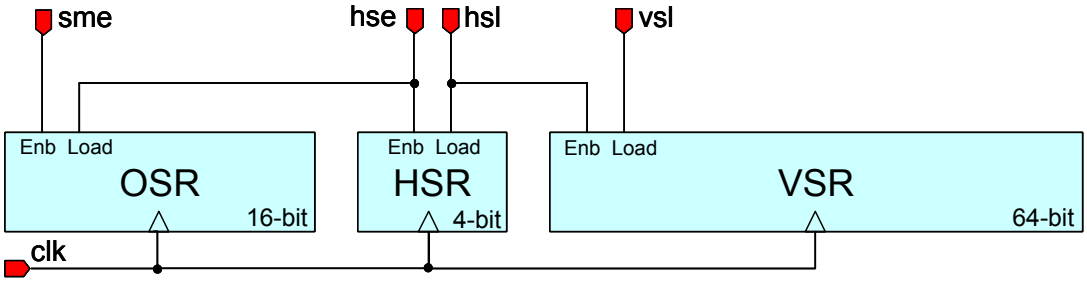


Figure 6.44: Block diagram of the shift registers of OSR, HSR, and VSR together with their common control signals of *sme*, *hse*, *hsl*, and *vls*. The *hse* and *hsl* signals for the HSR are in common with the OSR's load (*Load*) signal and VSR's (*Enb*) enable signal, respectively.

6.6.2.1 Vertical Shift Register (VSR)

The vertical shift register is a 64-bit register, which performs row selection in the FPA. Selection of a particular row means that one of the pixel terminals of all the pixels in that particular row is connected to a common potential via an analog switch whose gate is driven by the corresponding shift register outputs. When the corresponding shift register holds logic-one (1) at a particular position, then that particular row is selected. Under normal conditions only one row can be selected at a given time, therefore all the other shift registers should store logic-zero (0). If this is not obeyed, then the signal read out by the readout circuit will be corrupted, and the power dissipation of the chip will increase.

To be on the safe side, the rotating one (1) in the 64-bit shift register is updated whenever the scanning of all the 64 lines in the FPA is completed. In this way, even if there is an error, it will be recovered at least in the next frame period. Restoring the "10000…0000000" 64-bit pattern in the VSR and rotation is performed as follows. The control circuit waits 128 clock pulses for each pixel in a row. Considering the fact there are 4 pixels in a column, it waits 512 clock cycles for a row. When the scanning of the 4 pixels in a row is completed, vertical shift enable identical to the horizontal shift load signal (*hsl*) is raised high at the falling edge of clock (↓). Then, the internally stored data in the VSR is shifted to the left by one position at the next rising edge of the clock pulse (↑). When all the rows are

scanned, the *vsl* input of the VSR shift register is raised high at the falling edge of the clock pulse (↓) so that at the next rising edge of the clock pulse (↑), the 64-bit data "10000….000000" is loaded again into the register, and the first row in the FPA is selected again. According to this explanation, the frequency of the *hsl* should be 64 times faster as compared to *vsl*. Figure 6.45 shows the Verilog-XL simulation result showing the generation of *hsl* and *vsl* pulses.

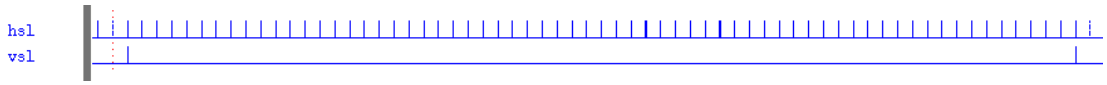


Figure 6.45: Verilog-XL simulation result showing the generation of the *hsl* and *vsl* pulses.

6.6.2.2 Horizontal Shift Register (HSR)

The horizontal shift register (HSR) is a 4-bit register, which controls the pixel selection in the 64 × 4 sub arrays. Selection of a particular pixel means that one of the pixel terminals out of 4 pixels in that particular pixel column group is connected to a constant current circuit via an analog switch whose gate is driven by the corresponding shift register outputs. When the corresponding shift register holds logic-one (1), then that particular pixel is selected. Under normal operating conditions, only one pixel is selected, therefore all the other 3 shift register outputs store logic-zero. The operation principle of the HSR is very similar to that of the VSR. The pixel select time 128 clock cycles, and there are 4 pixel in each column group. Therefore, the horizontal shift enable (*hse*) signal is raised 4 times for a single row, and within 128 clock cycles the HSR completes its one cycle. At the end of each cycle, the horizontal shift load (*hsl*) signal is raised. The control signals *hse* and *hsl* are raised high at the negative edge (↓) of the clock, and the shift operation takes place at the positive edge (↑) of clock. Figure 6.46 shows Verilog-XL simulation showing the generation of *hse* and *hsl* signals. The frequency of *hsl* is $1/4^{th}$ of the frequency of *hse*.

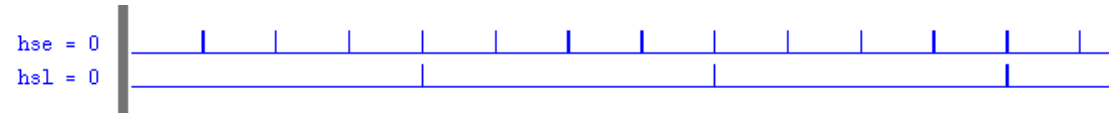


Figure 6.46: Verilog-XL simulation result showing the generation of the *hse* and *hsl* signals. The frequency of *hsl* is 1/4th of the frequency of *hse*.

6.6.2.3 Output Shift Register (OSR)

The Output shift register (OSR) is a 16-bit register, which controls the channel selection. Basically, the OSR rotates the 16-bit pattern (1000000…0000) 4 times during a row select period, so that all the pixels in the selected row are multiplexed to the serial output. Figure 6.47 shows the timing diagram of the serial output multiplexer. Within a pixel select time, S/H outputs of 16 channels are multiplexed to the serial output. The duration of the multiplexing operation is less than that of the pixel select time due to the fact that the S/H amplifier wastes some time during reset operation, making their valid output-hold time less than pixel select time. To prevent any loss in the channel outputs, the OSR waits only for 7 clock cycles for each channel output, and completes its operation within 112 clock cycles, where the pixel select time is 128 clock cycles.

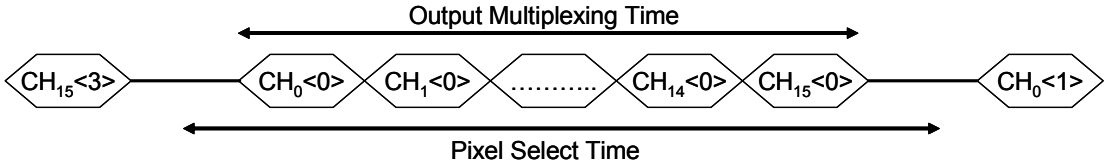


Figure 6.47: Timing diagram of the serial output multiplexer. Within a pixel select time, S/H outputs of 16 channels are multiplexed to the serial output.

In this sequence $CH_n<m>$ corresponds the output of m^{th} pixel in the n^{th} readout channel, where *m* takes values from 0 to 3, and *n* takes values from 0 to 15. The enable signal of this register is serial multiplexer enable (*sme*), and its load signal is equivalent to horizontal shift enable (*hse*). With the above timing, the first samples of the multiplexed output are wrong, because the sampled outputs of the readout channels may belong to some other pixels of the previous row. To solve this

timing problem, the load signal of the OSR is differentiated from *hse*, it is named as *hse_ext*, and taken from one of the digital input pins. In this way, the operation of this shift register becomes much more flexible simplifying interfacing of the FPA to data acquisition systems. Figure 6.48 shows the Verilog-XL simulation showing the generation of timing signals for the OSR. In this figure, *CLK* is the system clock, *sme* is the enable signal, and *hse* is the load signals for this register. *Mcol* is the content of the OSR, *scol* is the content of the HSR, and row is the content of the VSR. Note that, *sme* and *hse* changes at the negative edge of the clock, while the register contents are changes at the positive edge of the clock signal. *Sme* changes 16 times faster than *hse* as explained before. Whenever an *sme* pulse occurs at the negative edge (↓) of *CLK*, at the following positive edge (↑) the content of the OSR changes. Note that the column select register content remains unchanged until all the outputs of the 16 channels are scanned by the serial output shift register. In fact, when the *hse* rises, the next column is selected and 0001Hex is loaded into the OSR, where LSB is represents the first channel output.

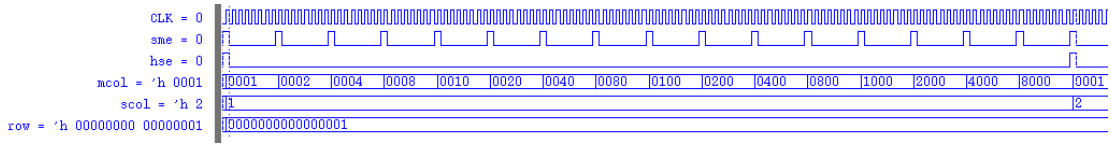


Figure 6.48: Verilog-XL simulation result showing the generation of timing signals for the OSR. *CLK* is the system clock, *sme* is the enable signal and *hse* is the load signals for this register. *Mcol* is the content of the OSR, *scol* is the content of the 4-bit HSR, and row is the content of the VSR.

6.6.2.4 Generation of Timing Signals for the Analog Circuits

The analog readout circuit requires timing signals to control the integration period and to trigger the output transfer from one block to another in the analog readout channels. They are generated at the same frequency as the horizontal shift enable signal (*hse*), since *hse* indicates that a new pixel is addressed. The required timing signals are integration enable (*intenb*), and two phase clock signals (*phi1* and *phi2*) are used for the switched capacitor circuits. As the name implies, *intenb* signal is used to define the integration period. The *phi1* and *phi2* signals are used to define

the correct timing for the CDS and S/H circuits. The operation principles of these circuits are explained in detail in the previous sections. Figure 6.49 shows the Verilog-XL simulation result showing the generation of the *intenb*, *phi1*, and *phi2* with respect to pixel select control signals such as *hse*, *hsl*, and *vsl*. In order to be able to see the clock edges, the zoomed simulation view of the timing signals for the analog circuits is given in Figure 6.50. In this simulation, the total time allocated for a pixel is 128 clock cycles. Within this time, the integration takes place for 112 clock cycles leaving 8 clock cycles from the start and end points of the *hse* pulses. The total integration time corresponds to 87.5 % of the total pixel time. It should also be mentioned that the detector bias will be applied for 128 clock cycles and the pixel signal will be integrated only for 112 clock cycles.

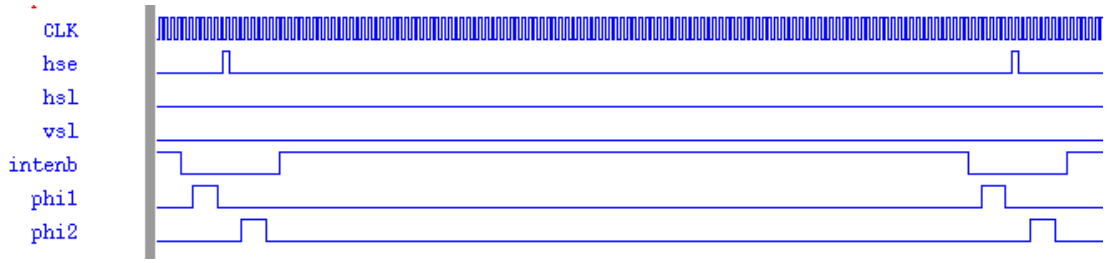


Figure 6.49: Verilog-XL simulation result showing the generation of the *intenb*, *phi1*, and *phi2* with respect to pixel select control signals such as *hse*, *hsl*, and *vsl*.

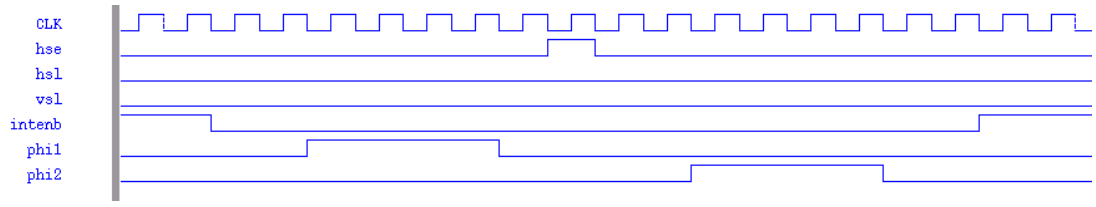


Figure 6.50: Zoomed simulation view showing the generation of timing signals for analog circuits.

In order to improve the NETD of the FPA, it may be required to scan the array at a reduced clock rate. Then, the signal levels at the output of the integrator may require a higher supply voltage provided that the integration time is also extended according to the applied clock rates. Since the maximum supply voltage is limited, increase of the supply voltage is not possible. Therefore, the control circuit

should be designed such that the integration time can be shortened. In fact, the control circuit is capable to use both long (112 clock cycles) and short periods (56 clock cycles). Figure 6.51 shows the Verilog-XL simulation result showing generation of *intenb* signal when the integration time is reduced. The *intenb* pulse is reduced from 112 clock cycles to 56 clock cycles.

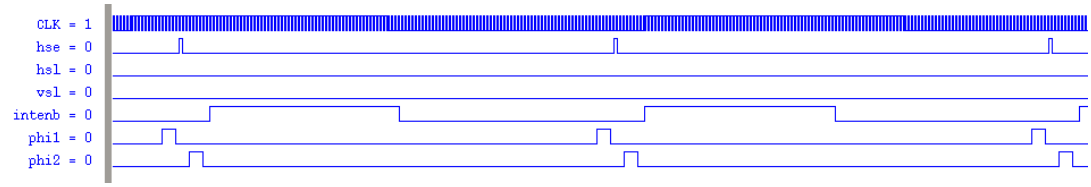


Figure 6.51: Verilog-XL simulation result showing generation of the *intenb* signal when the integration time is reduced. The *intenb* pulse is reduced from 112 clock cycles to 56 clock cycles. 56 clock cycles.

6.7 Layout Integration of Modules

The layout integration of the modules is performed in three steps: First, the analog channel readout circuit is integrated. Then, the integration of the 16-channel analog readout circuit is completed. Similarly, the integration of the digital timing circuit and shift registers is completed. Finally, these modules are brought together to form the 64 × 64 FPA chip.

The layout of the analog channel readout circuit is drawn by placing the layout of the designed circuit blocks next to each other. Since the layout of these individual blocks have been designed considering the required routing, it was relatively easy to perform the input and output connections. To save silicon area and to increase the width of this routing channel, the adjacent channels are placed with mirror symmetry. Since all the channel readout circuits operate in parallel, the digital control signals are the same for all the readout channels, therefore they are used in common, minimizing the required signal routing between the adjacent readout channels. The required external bias voltages and internally generated timing signals are routed within a routing channel left between two adjacent readout channels.

The 64 ×64 FPA is designed so that the non-uniformities in the array can be corrected by using adjustable bias voltages. These external bias voltages are used to control the transconductance of the GM circuit, the array and reference pixel reference voltages, the pixel bias current, and the reset voltage used in the switched capacitor integrator and S/H stages. Among them, the reference voltages for the array and reference pixels are used in common for all the pixels in a selected row. However, others voltages can be applied specifically for each channel. This is not practical due to the large number of required adjustable inputs and complicated external circuitry. Instead, the readout channels are grouped, and some of the bias voltages are shared by a group of readout channels so that the number of adjustable inputs decreases, and the required external circuitry becomes simpler. The only disadvantage of the common bias potential is that it is not possible to compensate for the non-uniformities in the channels with commonly used adjustable voltages when the readout is scanned at normal scanning rate. However, it is possible to perform these corrections for some part of the FPA at a given time, which reduces the overall frame rate. In the 64 × 64 FPA, there are four sets of adjustable voltages shared by a group of four channels, which reduces the uniformity corrected frame rate to 7.5 fps even though the array is scanned at 30 fps. Figure 6.52 shows the combined layout of the two identical readout channels (*Channel-1* and *Channel-2*). The layout measures 340 μm × 1320 μm in a 0.35 μm 3M2P CMOS process. It should be noted that there is a 20 μm increase in the allowed base width as compared to the 320 μm width of the 8 pixels in the column readout by two adjacent readout channels. The increase in the base width is utilized by the dummy pixels used to improve the uniformity and yield of the FPA, and the 64 × 64 array pixels are surrounded by two rows of dummy pixels.

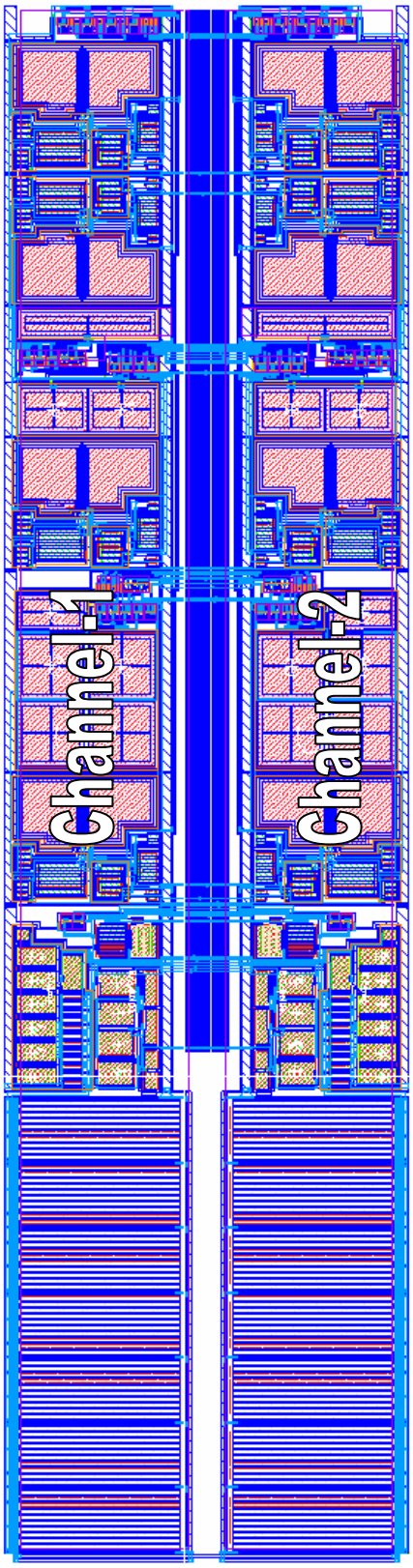


Figure 6.52: Combined layout of the two identical readout channels (*Channel-1* and *Channel-2*). The layout measures 340 µm × 1320 µm in a 3-metal 2-poly 0.35 µm CMOS process.

The 16 channel readout circuit is formed by placing eight of the combined channel layouts side by side. Figure 6.53 shows the layout of the complete 16-channel analog readout circuit. It is composed of 16 identical readout channels, a reference array and its bias circuit, and analog multiplexer switches for column selection. The layout measures 3025 µm × 1700 µm in a 3-metal 2-poly 0.35 µm CMOS process. The top level routing of the parallel channel outputs is performed on top of the channel layouts, and the channel outputs are routed to the corresponding bonding pads. Between the readout circuit and the FPA, there is a switch array, which is used to select corresponding columns during the scanning. In addition to that, the reference pixel array is also placed on the left of the channel readout.

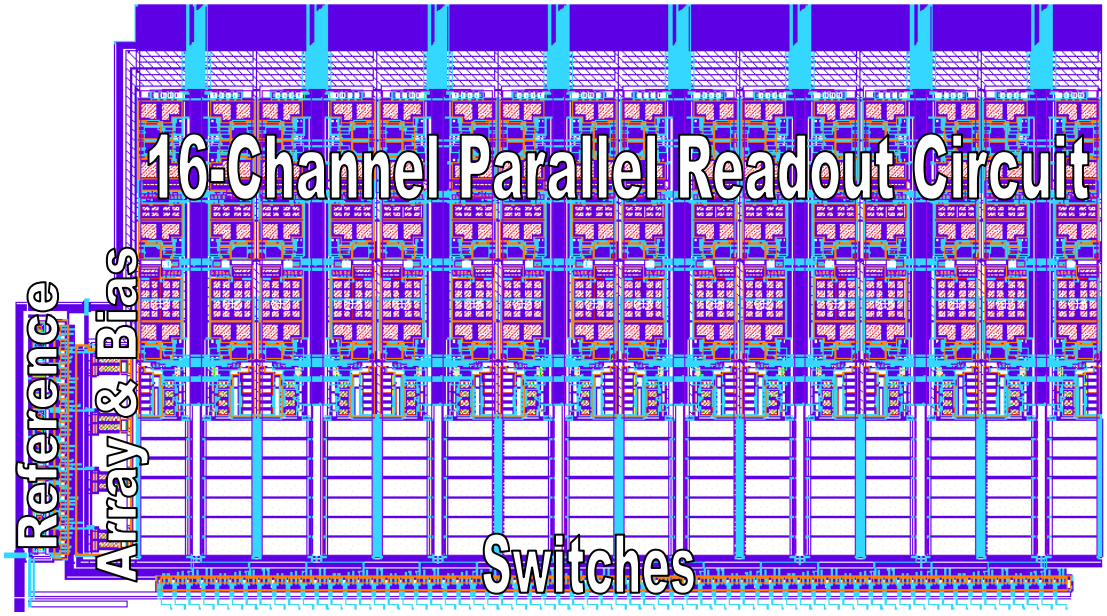


Figure 6.53: Layout of the complete 16-channel analog readout circuit. It is composed of 16 identical readout channels, a reference array and its bias circuit, and analog multiplexer switches for column selection. The layout measures 3025 µm × 1700 µm in a 3-metal 2-poly 0.35 µm CMOS process.

The digital blocks are implemented using semi-custom design techniques. The required gates are used from a digital standard cell library that is provided by the CMOS foundry. The layout view of these library cells contain only the metallization layers, and they are replaced with the original layout views by the foundry before fabrication.

Figure 6.54 shows the floor plan of the chip including the pad frame, and There are basically 11 structures in the chip: 1) 16–channel readout circuit, 2) 64 × 64 FPA, 3) analog test circuits, 4) reference array and its bias circuit, 5) analog serial output multiplexer, 6) scanning control circuit, 7) vertical shift register, 8) test pixels, 9) thermal test structures, 10) etch monitor openings, and 11) surface profile measurement structures. Figure 6.55 shows the layout of the fabricated 64 × 64 microbolometer FPA chip. The chip measures 4095 μm × 5375 μm (22mm^2) in a 3-metal 2-poly 0.35 μm CMOS process.

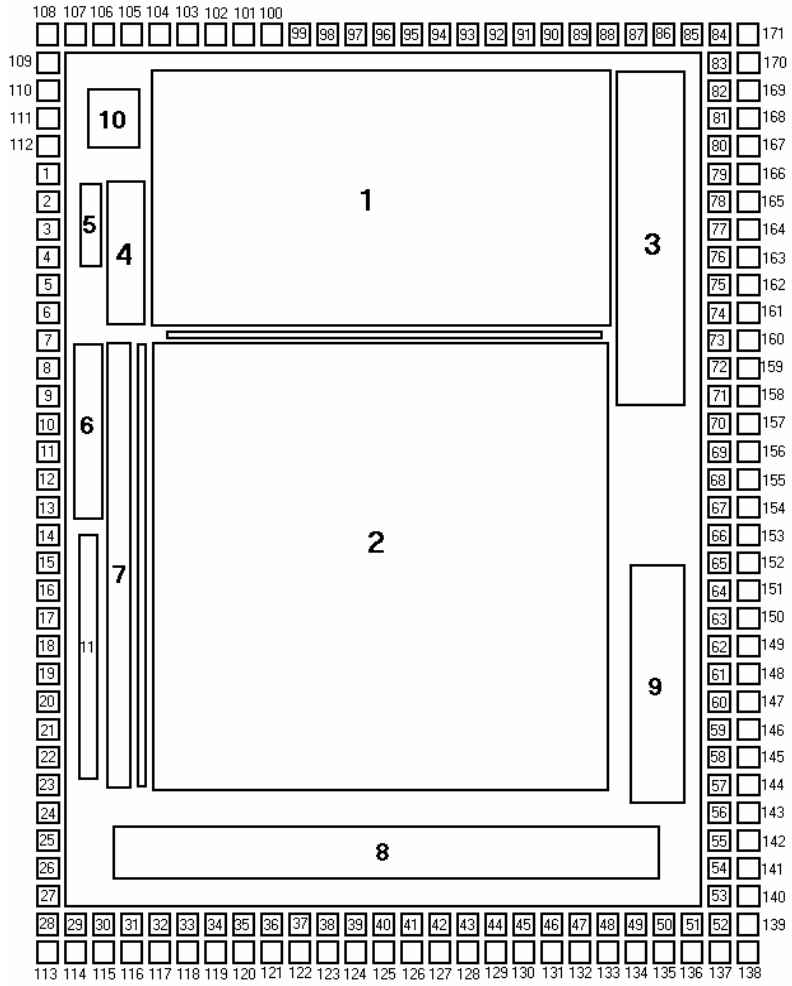


Figure 6.54: Floor plan and pad frame of the 64 × 64 microbolometer FPA. There are basically 11 structures in the FPA: 1) 16–channel readout circuit, 2) 64 × 64 FPA, 3) analog test circuits, 4) reference array and its bias circuit, 5) analog serial output multiplexer, 6) scanning control circuit, 7) vertical shift register, 8) test pixels, 9) thermal test structures, 10) etch monitor openings, 11) surface profile measurement structures.

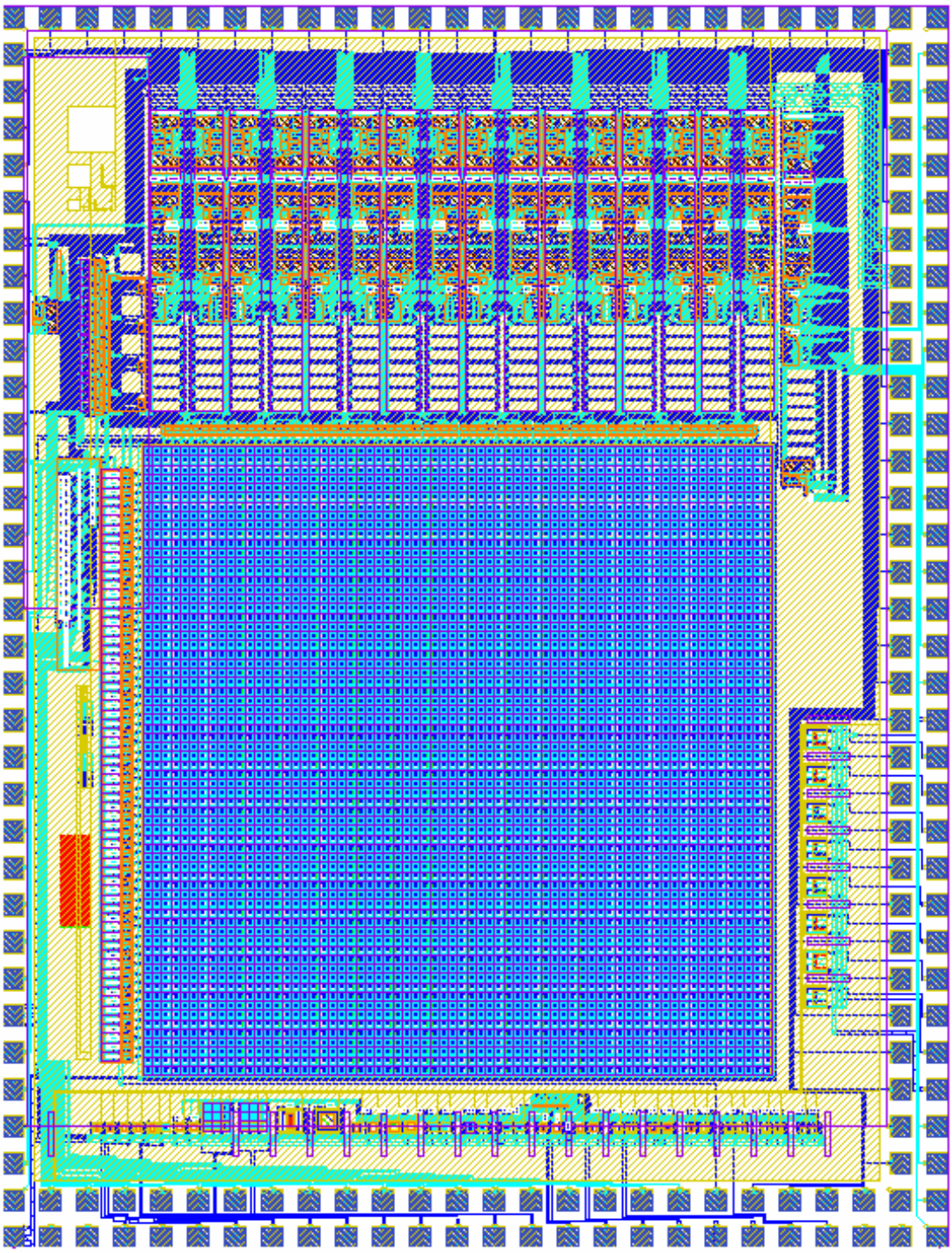


Figure 6.55: Layout of the 64 × 64 infrared imager chip. It measures 4095 µm × 5375 µm (22mm^2) in a 3-metal 2-poly 0.35 µm CMOS process.

6.8 Summary and Conclusions

This chapter presents the design details of the new 64 × 64 microbolometer FPA together with its integrated readout circuit. The designed 64 × 64 FPA is first of its kind where such a large format uncooled infrared detector array is implemented together with its integrated readout fully in CMOS process. The detectors used in the 64 × 64 FPA are based on the p^+-active/n-well diode microbolometer with 40 μm × 40 μm pixel size and 44 % fill factor, which has been explained in detail in Chapter 3. The fabricated p^+-active/n-well diode microbolometer has an estimated NETD value of 470 mK for a 4 kHz bandwidth, which sets the limit that can be achieved with any kind of readout circuits.

The readout circuit given in this chapter is specifically designed using full-custom design techniques. The parallel readout architecture is developed to minimize the electrical bandwidth which in turn improves the NETD of the overall array. To be able to keep the NETD as low as possible, 16-channel parallel readout circuit is designed. The preamplifiers and other circuit blocks used in the readout channels are optimized in terms of noise and silicon area. Careful design of the layout of the individual blocks makes integration of the 16-channel readout possible on top of the array pixels. Calculations show that the new 64 × 64 FPA provides an estimated NETD value of 800 mK for f/1 optics at 30 fps. This NETD value can be improved down to 350 mK by optimizing the post-processing steps and by decreasing the electrical bandwidth with increased number of readout channels.

CHAPTER VII

7 THE 128 × 128 UNCOOLED INFRARED FPA

This chapter presents the design details of the 128 × 128 uncooled infrared FPA chip. Like the 64 × 64 FPA described in Chapter VI, the 128 × 128 FPA is also based on the p^+-active/n-well diode microbolometers, which can be fabricated using a standard n-well CMOS process together with its monolithic readout circuitry without the need for any deposition and critical lithography steps. The 128 × 128 FPA has many similarities compared to the 64 × 64 FPA, but there are also a number of new features. The differences and similarities are shortly summarized below, and more detailed explanations are given in the following sections.

The 128 × 128 FPA has 16384 array pixels and 128 reference pixels, where the reference pixels are arranged in an identical single row above the array pixels. The use of a row of reference pixels together with a differential readout circuit makes differential FPA voltages independent of pixel positions in the FPA, reducing the fixed pattern noise and improving the array uniformity [42]. Furthermore, the dependence of the differential pixel output on the operating temperature is reduced dramatically, which relaxes the requirement for temperature stabilization. The 128 × 128 FPA chip has an integrated readout circuit with 32-channel parallel readout circuit, which is improved in terms of individual circuit block performance, implementation area, and overall block count and power consumption. The input referred offset voltage and matching of the input transconductance values are

improved in the differential transconductance amplifier. The switched capacitor integrator (SCI) circuit is modified so that it can cancel its own offset voltage without the need for a correlated double sampling (CDS) circuit afterwards. Furthermore, a common buffer circuit is used at the multiplexed channel outputs. With these modifications, the power consumption of the 128 × 128 FPA is kept same as that of the 64 × 64 FPA despite the increase in the number of parallel readout channels. The digital scanning and timing circuit of the 128 × 128 FPA has the same architecture as the one used in the 64 × 64 FPA. However, it has a new feature that makes external control of the FPA possible, where all the on-chip generated address and timing signals can also be applied externally to simplify electronic interfacing. The 128 × 128 FPA has also some on-chip sensors to monitor the chip temperature and package vacuum level. The 128 × 128 FPA chip has an expected NETD value of 1 K at 30 fps for f/1 optics. This NETD value can be decreased below 350 mK by optimizing the post-processing steps and by decreasing the electrical bandwidth with the help of increased number of readout channels. Considering its simple fabrication process and moderate FPA performance, the proposed FPA together with its readout circuit can be used in many low-cost uncooled infrared imaging applications.

This chapter is organized as follows: Section 7.1 presents the architecture of the 128 × 128 FPA chip. Section 7.2 described in detail the improved array structure of the 128 × 128 FPA that can compensate for the effect of FPA routing resistances and variations in the operating temperature. Section 7.3 explains the analog readout circuitry used in the parallel readout channels of the 128 × 128 FPA, and major modifications and improvements as compared to the previous designs. Section 7.4 briefly explains the digital scanning circuitry. Section 7.5 presents the integration of the modules and gives the overall layout of the 32-channel analog readout circuit. Section 7.6 explains the on-chip temperature and vacuum sensors. Section 7.7 gives the floor plan and layout of the 128 × 128 FPA chip. Finally, Section 7.8 summarizes the 128 × 128 FPA design with its performance parameters and improvements as compared to the previous 64 × 64 FPA.

7.1 FPA Architecture

Figure 7.1 shows the block diagram of the 128 × 128 uncooled infrared imager chip. The chip is controlled by a digital scanning circuitry similar to the one used in the 64 × 64 FPA chip. It has 32-channel parallel readout circuitry that scans the 128 × 128 FPA differentially with respect to a 1 × 128 reference pixels at 30 fps with an electrical bandwidth of 8 kHz. There are 2 output multiplexers that route the channel outputs to 2 serial outputs. At 30 fps scanning rate, the output multiplexers operate at a sped of 250 Ksamp/s.

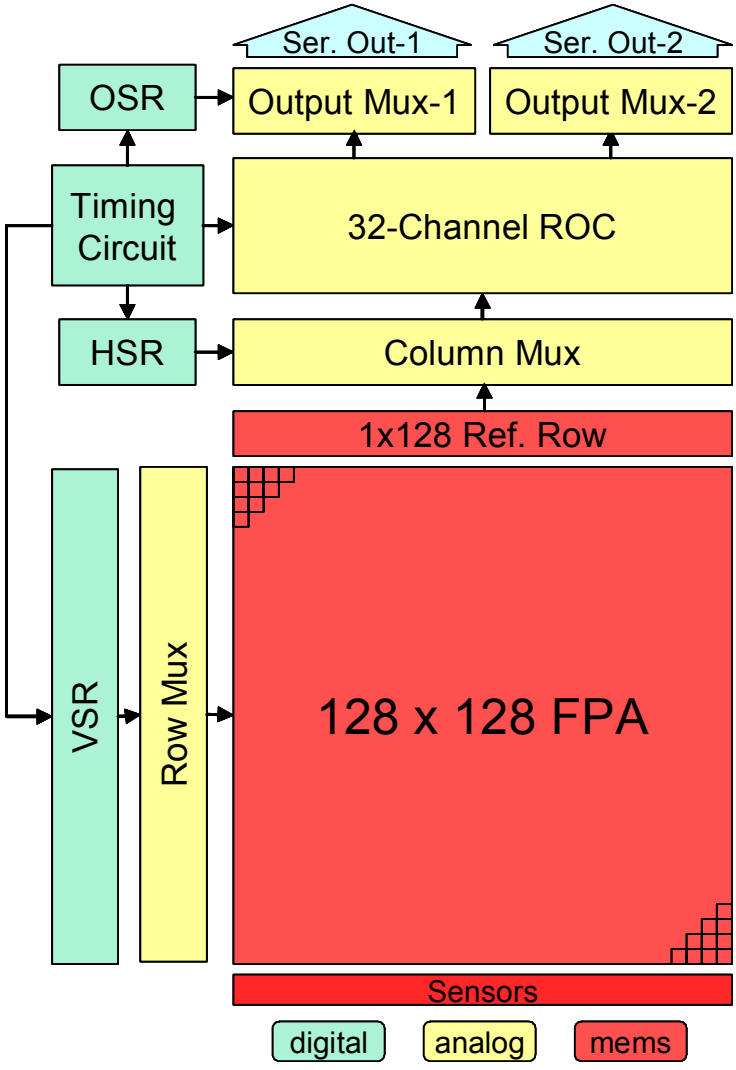


Figure 7.1: Block diagram of the 128 × 128 uncooled infrared imager chip.

The details of each block in the 128 × 128 FPA are explained in detail in the coming sections, with the emphasis on the improvements as compared to the previous 64 × 64 FPA. The major improvements are in the array structure and in the preamplifier of the analog readout channels. The array structure is improved in such a way that the effect of the fixed pattern noise due to the FPA routing resistance is minimized. The input matching of the input differential pair is improved with the help of a feedback structure, which matches the transconductance value of the input pair reducing the input offset and simplifying the uniformity correction. The number of opamp circuits is decreased by eliminating the standalone CDS block and integrating it in the switched capacitor integrator circuit. Furthermore, a common buffer is used for the channel outputs, and it is placed after the analog channel multiplexers. Despite the increase in the analog readout channels, the power consumption of the chip is kept about 25 mW, which is almost the same as the power consumption of the 64 × 64 FPA. The next section explains the improved architecture of the 128 × 128 FPA.

7.2 Improved Array Structure

Figure 7.2 shows the simplified schematics of the 128 × 128 array with the improved array structure [42]. The improvement is achieved by using an exact replica of the array row as a reference row of pixels just above the array pixels, and improving the vertical routing structure external to the detector area. To compensate for the horizontal voltage variation, the reference pixels are placed in a single row above the array pixels. The electrical property of the reference pixels is identical to that of the array pixels, with the only difference being in their thermal conductance values. To reduce any possible self-heating due to excessively fast addressing of these pixels, they are connected with metal support arms on wider oxide support arms. The corresponding electrical resistance of the reference pixels is matched by using the same interconnect structure outside the pixel area on the substrate. Due to the poor thermal isolation of the reference pixels, they can be considered to be infrared-blind due to their reduced responsivity by about three orders of magnitude. The high thermal-conductance associated with the reference pixels reduces also their

thermal time constant to a very low level, and they can respond to the self-heating almost immediately. However, due to the increased thermal conductance value, the self-heating of these detectors is not as high as the actual detectors, even if they can reach the steady state very quickly. The disadvantage of having short thermal time constant for the reference pixels is that they can not be used to compensate for the self-heating occurring unavoidably for the array pixels. However, this can be solved by adjusting the current level just prior to the integration as will be explained in detail in the coming sections.

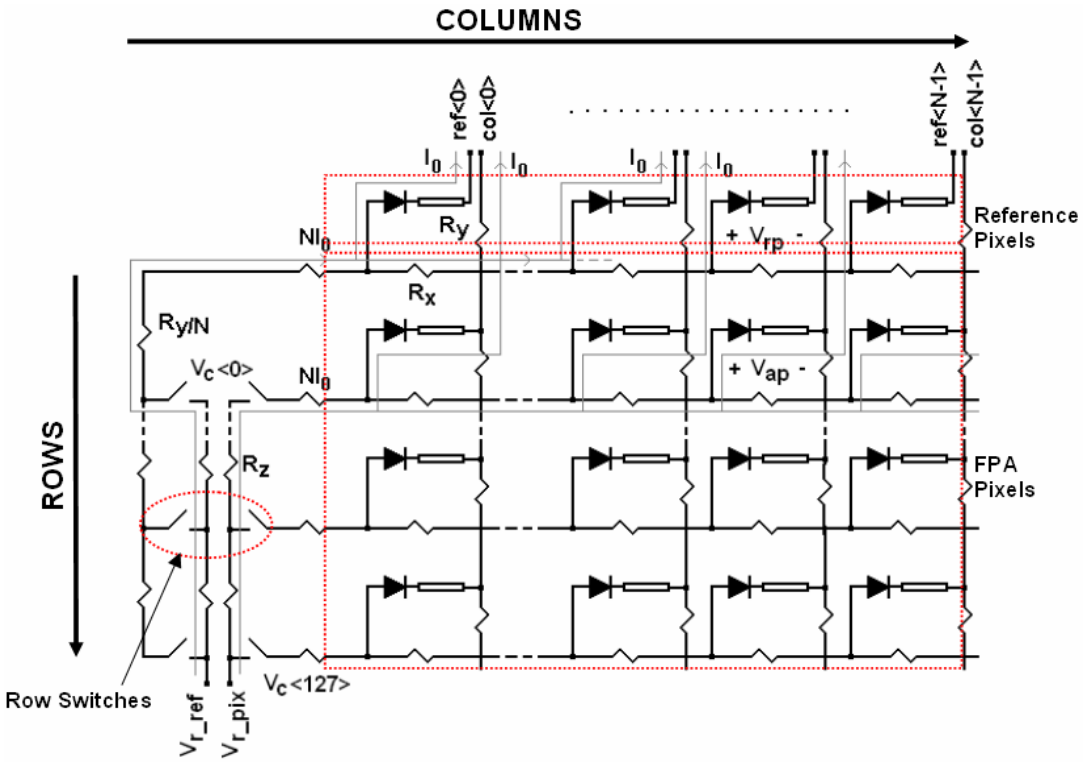


Figure 7.2: Simplified schematics of the 128 × 128 array with the improved array structure [42].

To compensate for the vertical voltage variations, the metal lines in the external vertical routing structure is implemented in such a way that the vertical voltage drop measured from a selected row bias voltages are same both for the reference and array pixels, which is cancelled by a differential readout circuit. Although it is also possible to make the FPA insensitive to vertical pixel selection, the last designed FPA is designed so that the differential reading is compensated both

for the horizontal and vertical voltage variations. The resulting array pixel voltage ($V_{FPA}(m,n)$) and reference pixel voltage ($V_{REF}(m,n)$) in the FPA are given as [42]

$$V_{FPA}(m,n) = V_{row}(m) - V_{pix}(m,n) - mI_0R_y - \frac{N}{K}(K-1-p)I_0R_x - KI_0R_x\sum_{k=0}^{c}(\frac{N}{K}-k) \quad (7.1)$$

$$V_{REF}(m,n) = V_{row}(m) - V_{ref}(n) - mNI_0\frac{R_y}{N} - \frac{N}{K}(K-1-p)I_0R_x - KI_0R_x\sum_{k=0}^{c}(\frac{N}{K}-k) \quad (7.2)$$

$$V_{row}(m) = V_{ref\_ref} - NI_0(N-1-m)R_z \quad (7.3)$$

$$p = \mathrm{mod}(n,K) \quad (7.4)$$

$$c = (n-p)/K \quad (7.5)$$

where, m and n the row and column of the pixel, V_{row} is the bias voltage for the selected row, V_{pix} and V_{ref} are the voltage of the selected array and reference pixels, I_0 is the pixel bias current, R_x and R_y are horizontal and vertical routing resistance values for a single pixel, N is the number of columns and rows in the FPA (N = 64), K is the number of the parallel readout channels (K = 16), p is the position index of the pixel in a selected column group ($0 \le p \le 3$), c is the position index of the corresponding readout channel ($0 \le c \le 15$), and V_{pix_ref} and V_{ref_ref} are the reference bias voltage of the array rows and reference row. Assuming that the line resistance values match well between the array routing lines and reference lines, the differential FPA output voltage ($\Delta V(m,n)$) is given as [42]

$$\Delta V(m,n) = V_{REF}(m,n) - V_{FPA}(m,n) = V_{pix}(m,n) - V_{ref}(n) \quad (7.6)$$

As it can be seen, the differential FPA output voltage does not include any voltage drop term related with the pixel position in the array. This result verifies that the differential FPA output voltage is fully compensated in terms resistive voltage drops in the array. In addition to that, the differential voltage also helps compensating for the effect of operating temperature variations, relaxing the requirements for the temperature stabilization, and hence, making low-power operation possible. It

should be noted that the 128 × 128 reference voltages are generated by a 1 × 128 reference row and a dummy routing structure outside the pixel area. The only disadvantage of the differential structure is that it introduces extra noise coming from the reference pixels and extra circuitry in the differential readout. However, considering its inherent non-uniformity (fixed-pattern noise) correction capability, it is still preferred to the single ended structure. In the single ended case, external compensation would be required, which would also increase the input noise level even at the expense of increased circuit complexity.

In the 128 × 128 FPA, the reference pixels are placed in a single row with 40 µm pixel pitch on top of the microbolometer pixel array with 136 × 136 pixels with 4 dummy pixels on each side. Figure 7.3 shows the zoomed layout of the 136 × 136 array pixels with reference pixels placed in a 1 × 136 format above the array pixels. There is a separate reference pixel for each column of array pixels, and none of the reference pixels is shared with any other column. In this way, the mismatch due to the self-heating effect resulting due to frequent addressing of the reference pixels is minimized considerably.

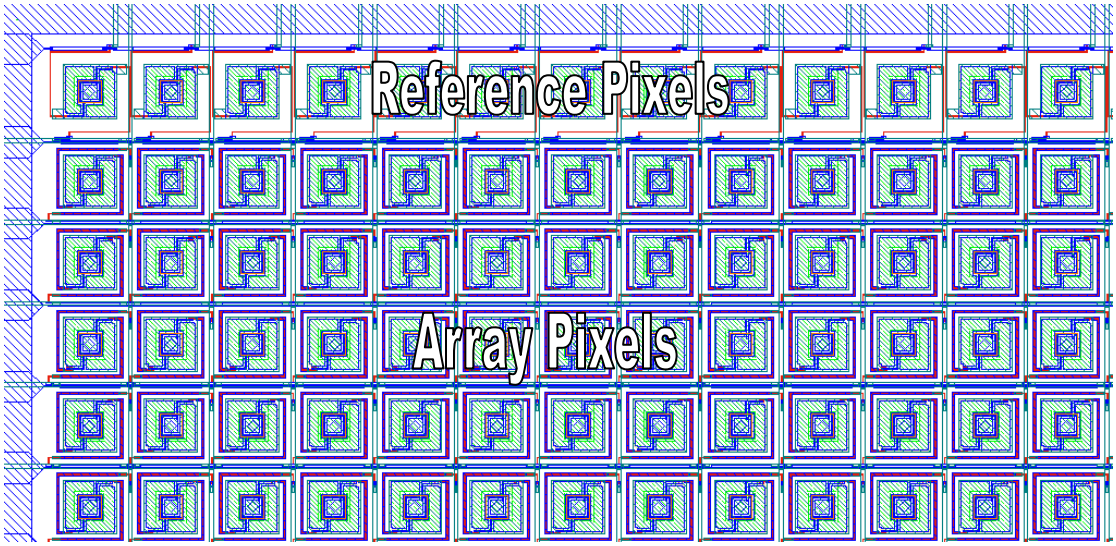


Figure 7.3: Zoomed layout of the 136 × 136 array pixels with reference pixels placed in a 1 × 136 format above the array pixels.

Since there is only one row of reference pixels, there is a need for some additional circuitry to compensate for the vertical voltage drops (nR_yI_0) in the array. Therefore, a dummy routing structure is used to compensate for this vertical voltage drop in the FPA. Then, all of the reference pixel currents add up to NI_0. To compensate for this increased current level flowing vertically outside the pixel area, identical parallel lines are used to reduce the line resistance to $1/N^{th}$ of that of the resistance of the vertical array routing lines, so that both vertical terms become equal to nR_yI_0. Figure 7.4 shows the zoomed layout of the dummy routing structures used to compensate for the vertical voltage drops in the FPA.

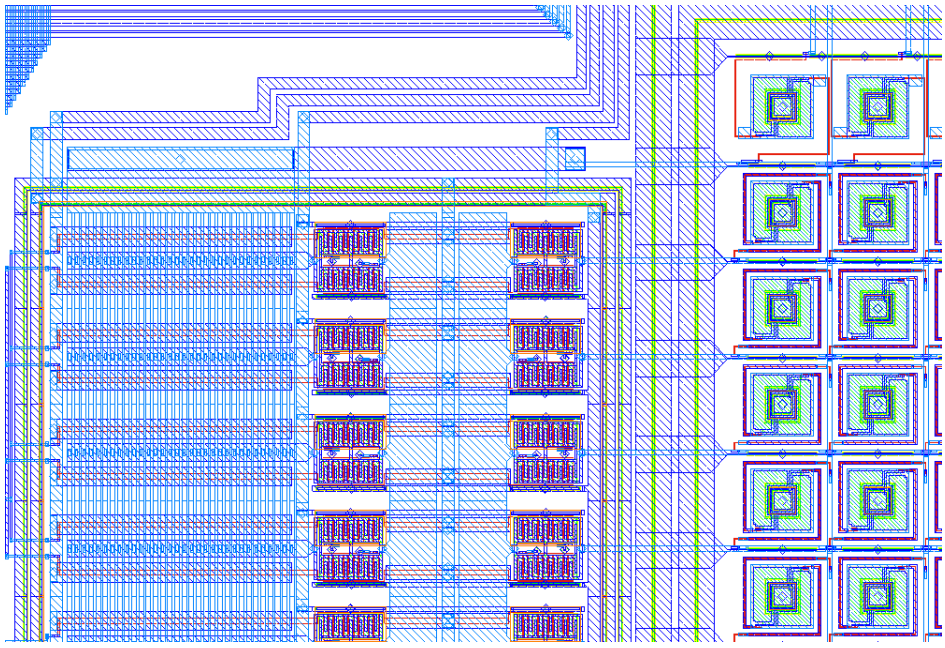


Figure 7.4: Zoomed layout of the dummy routing structures used to compensate for the vertical voltage drops in the FPA.

If the resistive voltage drops are not compensated, the variation of pixel voltage will be about 2 mV between the top and bottom pixels in the same column, and it will be 33 mV between the left-most pixel and right-most pixel in the same row. If no bias corrections is applied during the scanning, at least 35 mV input dynamic range will be required just for the voltage drops along the line resistances, where the infrared induced voltages will be at most 50 µV - 100 µV. Therefore, the above mentioned compensation procedure solves these problems. In addition, most

of the input dynamic range can be used for the infrared induced signals, and large gains or long integration periods can be used.

Figure 7.5 shows the layout of the reference pixel. The reference pixel is thermally shorted to the substrate with wide metal-oxide layer to increase the thermal conductance value. The thermal conductance (G_{th}) and capacitance (C_{th}) values of the reference pixels are 4.7×10^{-4} W/K and 3.4×10^{-9} J/K, respectively. The resulting time constant value (τ) is only 7.2 μs, therefore the reference pixel can cool down easily until it is addressed for the next pixel in the next row. The low time constant value of the reference pixels complicates the compensation of the self-heating effect with the differential readout architecture. However, this problem is solved at circuit level as explained in the next section. A polysilicon interconnect placed on the substrate is used to match the electrical resistance of the pixel to that of the array pixel.

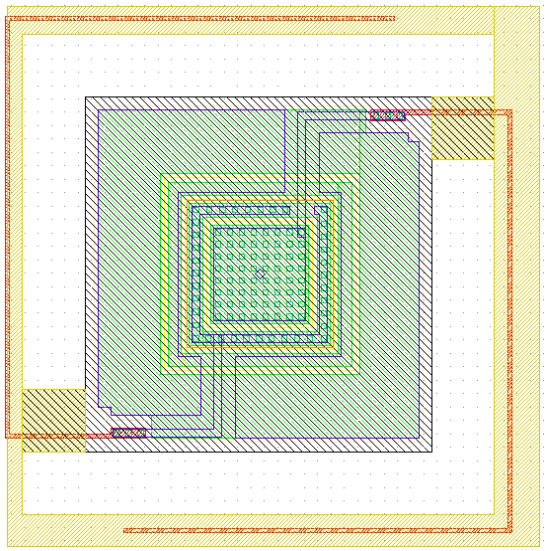


Figure 7.5: Layout of the reference pixel. The reference pixel is thermally shorted to the substrate with wide metal-oxide layer to increase the thermal conductance value. A polysilicon interconnect placed on the substrate is used to match the electrical resistance of the pixel to that of the array pixel.

7.3 Analog Readout Circuitry

Figure 7.6 shows the block diagram of the analog readout circuitry used in the parallel readout channels in the 128 × 128 FPA chip. The analog readout channel circuit contains the following blocks: a differential transconductance amplifier, a switched capacitor integrator (SCI), and a sample-and-hold (S/H) circuit. In the previous implementation, there was also a CDS circuit to remove the integrator offset voltage. In this version, this feature is integrated in the integrator itself, and the channel layout is compacted considerably. Bias currents required by the blocks are generated by a bias block. This block also sinks the desired amount of DC current from the output of the transconductance amplifier at the input of the integrator to avoid saturation. For simplicity, this block is not shown in the block diagram.

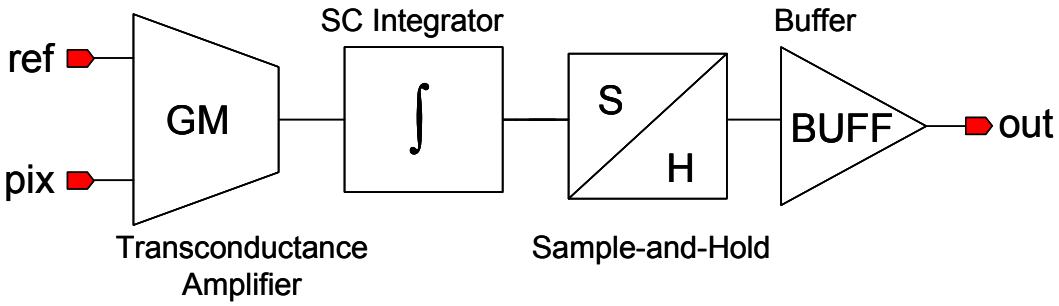


Figure 7.6: Block diagram of the analog readout circuitry used in the parallel readout channels in the 128 × 128 FPA.

There are three major improvements in the analog readout circuitry of the 128 ×128 FPA, which are given as follows: 1) the differential transconductance amplifier is improved in terms of transconductance matching and input offset voltage, 2) the SCI circuit is improved with the integrated offset removal circuitry, and 3) an improved self-heating compensation method is used. These improvements will be explained in detail in the following sections.

7.3.1 Improved Differential Transconductance Amplifier

Figure 7.7 shows the schematic of the improved differential transconductance amplifier used in the readout circuitry of the 128 × 128 FPA. Matching and offset reduction is achieved with the help of a negative feedback structure [58]. In the absence of the negative feedback, the drain-source voltages would not be equal for the input transistors N_1 and N_2. Due to finite output resistance values of these input transistors and due to the unsymmetrical structure of the current mirror, there will be a mismatch in the drain current values of the transistors, causing a mismatch in their transconductance values and an offset current at the output. One way to solve this mismatch and offset problem is to force the two drain voltages to be equal using negative feedback [58] as shown in Figure 7.7. The amplifier used in the feedback structure is implemented using basically the same circuit as the differential transconductance amplifier with different device dimensions to save power and silicon area.

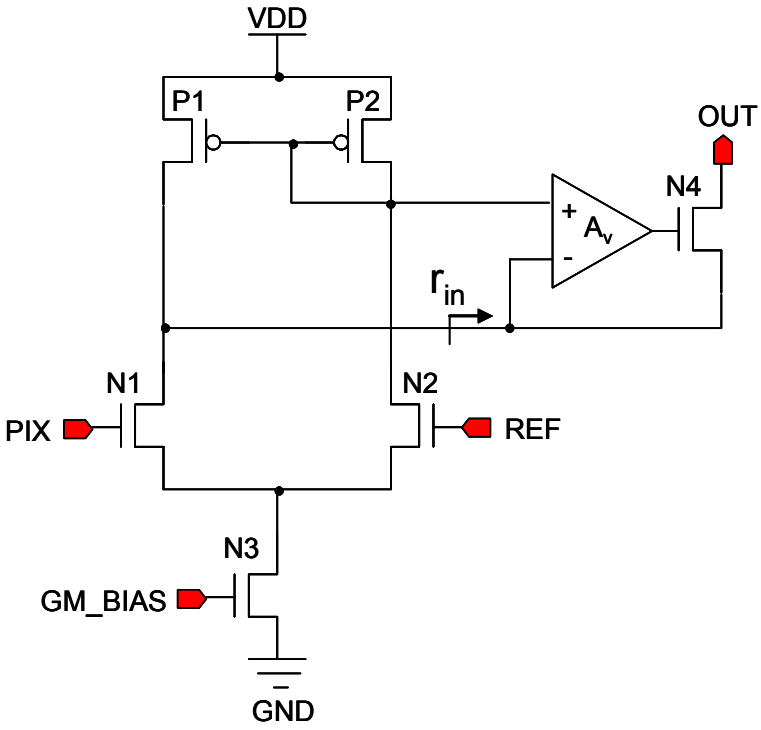


Figure 7.7: Schematic of the improved differential transconductance amplifier used in the readout circuitry of the 128 × 128 FPA. Matching and offset reduction is achieved with the help of a negative feedback structure [58].

Due to the negative feedback, the resistance seen by the transconductance stage is reduced considerably mainly due to the large open loop gain of the amplifier (A_v) in the feedback path given as

$$r_{in} = \frac{r_o}{1 + g_m r_o (1 + \eta + A_v)} \cong \frac{1}{g_m A_v} \tag{7.7}$$

where, g_m and r_o are the transconductance and output resistance of the feedback transistor (*N4*), η is the ratio of the bulk-to-source transconductance of transistor to g_m, and A_v is the open loop gain of the feedback amplifier. Since the input resistance value (r_{in}) is very small, the required output resistance of the transconductance circuit is not so high, and a simple current mirror can be used as the active load. In fact, a simple current mirror implemented with *P1* and *P2* transistors is used, which reduces the layout area and the number of required bias voltages.

Figure 7.8 shows the noise model of the improved differential transconductance amplifier. The noise analysis is similar to the result presented in Chapter V, and the output noise current spectral density is approximately given as

$$i_{nout}^2 = g_{mi}^2 \left[v_{n1}^2 + v_{n2}^2 + \left(\frac{g_{m3}}{g_{mi}} \right)^2 \left(v_{n3}^2 + v_{n4}^2 \right) + \left(\frac{g_{d3} + g_{d1}}{g_{mi} A_v} \right)^2 v_{n5}^2 + \left(\frac{g_{d3} + g_{d1}}{g_{mi}} \right)^2 v_{n6}^2 \right] \tag{7.8}$$

where, g_{mi} is the transconductance value of the transistors in the differential pair (*M1* and *M2*), g_{d1} is the output conductance value of the *M1*, g_{m3} is the transconductance value of the transistors in the current mirrors (*M3* and *M4*), g_{d3} is the output conductance value of *M3*, A_v is the voltage gain of the differential amplifier used in the feedback path, v_{n1}-v_{n5} are the gate referred noise voltages of the transistors *M1*-*M5*, and v_{n6} is the input noise of the feedback amplifier.

In the preamplifier design it is advantageous to have a large transconductance (g_m) value to decrease the thermal noise and large device area to reduce the flicker (1/*f*) noise components of the input referred noise voltage [63, 71]. Usually, the

device sizes are chosen such that *W/L* value gives a sufficient g_m value at a certain bias level and the gate area (*WL*) is sufficiently large to suppress the 1/*f* noise. The bias level should also be kept as small as possible to keep the power dissipation at a reasonable level.

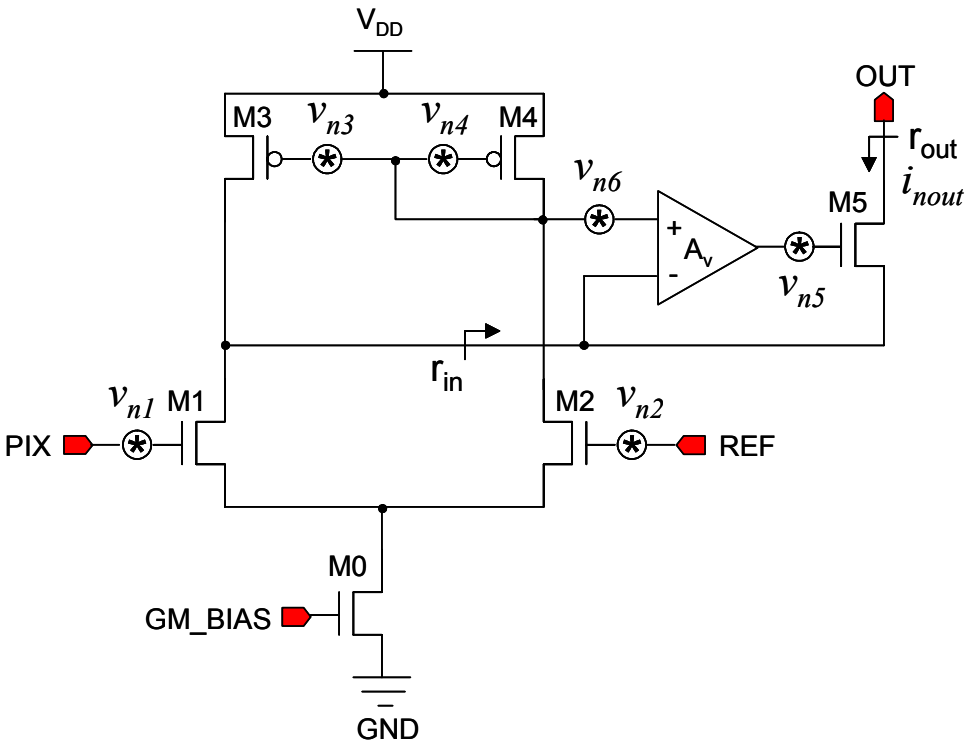


Figure 7.8: Noise model of the improved differential transconductance amplifier.

To keep the electrical bandwidth at 4 kHz as in the previous design, 64 parallel readout channels are required. The required readout channel needs to be implemented within 80 μm base width (2 pixel wide), which is not practical due to the requirement of large transistors to achieve low noise. Therefore, there are 32 parallel readout channels in the 128 × 128 FPA, each of which is used to scan 4 pixel columns at 30 fps. The electrical bandwidth is doubled to about 8 kHz (7.7 kHz) and pixel noise level increased by a factor of √2. Therefore, the requirement for low *1/f* noise for the preamplifier is relaxed, since due to the extended bandwidth the contribution of *1/f* noise is not as critical as it was for the 64 × 64 FPA. This is also valid for the thermal noise, since the detector noise is also increased due to the

extended bandwidth. Hence, it is possible to use lower g_m values, which is possible with smaller *W/L* ratios. However, to keep *1/f* noise at an acceptable level, *L* values should be chosen larger. In the 128 × 128 FPA design, *W/L* ratios was chosen as 1215 μm / 10 μm. With these values g_m is found about 700 μA/V when the differential stage is biased at 60 μA.

The input referred noise of the improved preamplifier circuit is simulated to be 0.72 μV from 0.1 Hz to 8 kHz. The detector noise is calculated to be 0.72 μV for 8 kHz bandwidth. Total input noise voltage is calculated to be 1.26 μV, where the noise of the reference pixel has also been included. With a G_{th} value of 1.8×10^{-7} W/K, and thermal time constant of 27 ms, this corresponds to an estimated NETD value of 1 K when the FPA is scanned at 30 fps using an f/1 optics. This NETD value can be decreased below 350 mK provided that the electrical bandwidth is reduced further by using increased number of readout channels. Increasing the number of readout channels will result larger chip area and increased cost, if the readout circuitry is not simplified. The readout can be simplified by using simpler integrator circuits without any opamps at the expense of reduced voltage swing. However, the use of simpler circuit structures allows assignment of separate readout channels for each pixel column in the FPA [28].

7.3.2 Improved Switched Capacitor Integrator (SCI)

There are two improvements in the switched capacitor integrator (SCI) as compared to the previous design: 1) opamp offset is removed, and 2) effect of switching transients is reduced. Figure 7.9 shows the schematic of the improved SCI circuit used in the readout circuitry of the 128 × 128 FPA. The offset and low frequency correlated noise of the opamp are cancelled by resetting and sampling the residual offset voltage prior to the actual integration operation [76]. The gain of the integrator can be adjusted by varying the integration capacitance (C_{int}).

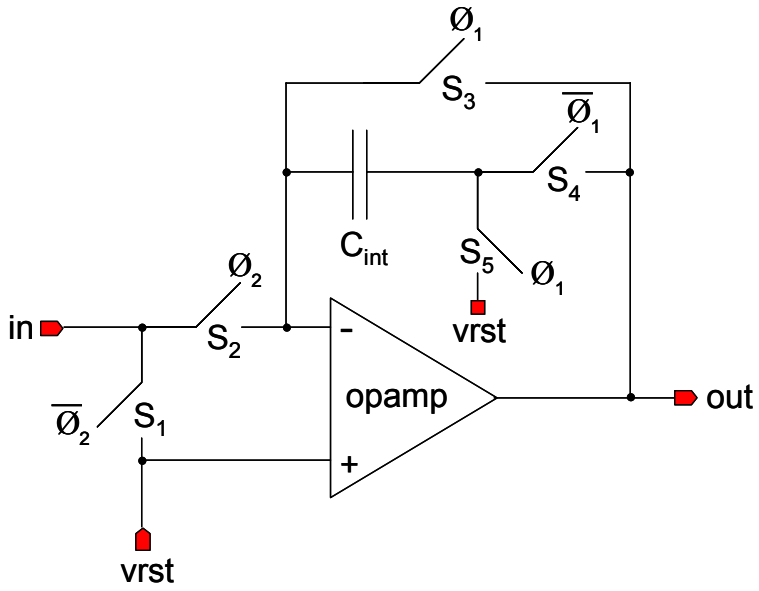


Figure 7.9: Schematic of the improved SCI circuit used in the readout circuitry of the 128 × 128 FPA. The offset and low frequency correlated noise of the opamp are cancelled by resetting and sampling the residual offset voltage prior to the actual integration operation [76]. The gain of the integrator can be adjusted by varying the integration capacitance (C_{int}).

The SCI circuit operates in two phases as follows: At $\varnothing_1$, S_1, S_3, and S_5 switches are closed. With this configuration, the opamp is in the unity gain buffer mode. The integration capacitor is isolated from the output and connected between negative input and reset potential (*vrst*), and the capacitor is discharged or reset. In this configuration, the opamp offset voltage is stored in the integration capacitor (C_{int}). The S_1 switch is used to keep the output terminal of the transconductance amplifier at a fixed potential equal to the reset potential of the SCI circuit. In this way, the transient spikes in the integrated current are minimized considerably.

At $\varnothing_2$, S_1, S_3, and S_5 are opened, and S_2 and S_4 are closed. By the time when $\varnothing_2$ becomes high, the switching transient in the scanning circuit has passed away, and the detector current, $i_{in}(t)$, is integrated during the integration period (T_{int}) across the integration capacitor (C_{int}), whose initial voltage is the opamp input referred offset voltage ($V_{op\text{-}offset}$). Therefore, the output voltage (V_{out}) is independent of the opamp offset, which is given as

$$V_{out} = V_{rst} + V_{op-offset} - V_{op-offset} - \frac{1}{C_{\text{int}}}\int_0^{T_{\text{int}}} i_{in}(t)dt = V_{rst} - \frac{1}{C_{\text{int}}}\int_0^{T_{\text{int}}} i_{in}(t)dt \qquad (7.9)$$

where, V_{rst} is the reset voltage of the switched capacitor integrator circuit, $V_{op\text{-}offset}$ is the offset voltage of the opamp, C_{int} is the integration capacitance, and T_{int} is the integration period, and $i_{in}(t)$ is the input current of the SCI circuit.

7.3.3 Improved Self-Heating Compensation

The self-heating compensation in the previous 64 × 64 design relies on the matching of thermal capacitance values of the reference and array pixels. In case of matched thermal capacitances, the applied electrical bias would heat both the pixel and the reference by the same amount, and there will be a ramp of equal slope for both pixel voltages. With a differential readout, this common mode signal is rejected and only the differential signal will be amplified or integrated. If the reference and array pixels match, then the output contains only the infrared induced voltage change. However, any mismatch in the thermal capacitances will affect the output voltage due to the self-heating effect.

In the new design, a fixed DC signal which is equal to the average of the uncompensated self-heating current is subtracted from the output current of the differential transconductance amplifier before the SCI circuit. If there is no infrared induced current signal, then the integrator output will make a peak and return to its initial value, and the shift from its initial value corresponds to the infrared induced signal. Figure 7.10 shows the cancellation of self-heating effect by using current sink method [61]. $I_{in}(t)$ is the output current of the differential transconductance amplifier, which changes to the self-heating effect, reaching a maximum value of I_{max}. I_o is the average of $I_{in}(t)$ over the integration period of T_{int}. $V_{out}(t)$ is the output voltage of the SCI circuit with a reset voltage of V_{rst}.

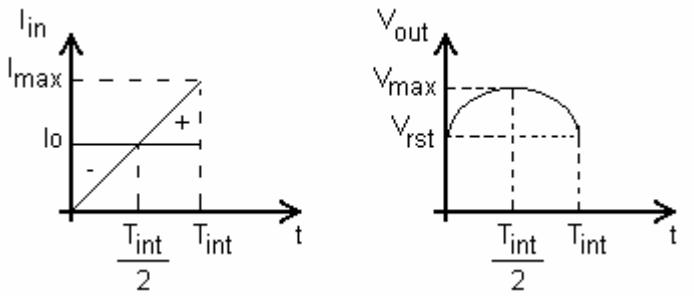


Figure 7.10: Cancellation of self-heating by using current sink method [61]. $I_{in}(t)$ is the output current of the differential transconductance amplifier, which changes to the self-heating effect, reaching a maximum value of I_{max}. I_o is the average of $I_{in}(t)$ over the integration period of T_{int}. $V_{out}(t)$ is the output voltage of the SCI circuit with a reset voltage of V_{rst}.

In Figure 7.10, I_0 is the average value of self-heating induced current waveform equal to $I_{max}/2$. At the beginning of integration cycle, I_{in} is negative and output voltage rises and reaches a maximum value of V_{max} at $T_{int}/2$. Starting from that point on, I_{in} becomes positive and V_{out} starts to decrease. Finally, when it reaches its initial value at T_{int}, output voltage is sampled by the sample and hold amplifier, and the self-heating effect is cancelled. If there is an infrared induced output current, then the output at sampling time is going to be lower than the initial reset value, and that difference will be the actual signal carrying the information about incident infrared radiation level.

7.4 Digital Scanning Circuitry

The digital scanning circuitry used in the new 128 × 128 FPA has the same architecture as that of the 64 × 64 FPA. Since the 128 × 128 FPA is divided into two parallel scanned 128 × 64 sub arrays, the multiplexers requires twice as much as address locations as compared to the 64 × 64 FPA. Therefore, a 16-bit counter is used in the digital scanning circuit of the 128 × 128 FPA, which is 1-bit longer as compared to the previously explained counter. As a new feature, the shift registers used to address the rows and columns of the 128 × 4 sub arrays can be controlled by a 7-bit row address and a 2-bit column address, which are applied externally together with the required timing signals for the analog readout circuitry. In this way, the

scanning of the circuit becomes compatible ideally for any data acquisition system, making the required interfacing more flexible and tolerant to design errors. Since the digital circuit architecture is very similar to the one used in the 64 × 64 FPA, the design details are not given here*.

7.5 Integration of Modules

The integration of the modules is performed in three steps: 1) integration of analog channel readout circuitry, 2) integration of parallel readout channels, and 3) overall chip integration. The integration of the analog circuitry starts with the integration of analog channel readout circuitry, which has been performed in the same way as described previously for the 64 × 64 FPA. Considering the fact that each pixel is 40 µm wide, the pitch for the layout becomes 160 µm including the routing. The allowed base width for the readout channels increases with the use of dummy pixels and the use of mirror symmetric placement of the channels. With this method, the width of a single channel becomes 155 µm without routing, and the pitch for the combined mirror symmetric channels becomes 335 µm, which is wide enough for the required routing for the channel signals. Figure 7.11 shows the layout of the analog channel readout circuitry. It measures 155 µm × 820 µm in a 3-metal 2-poly 0.35 µm CMOS process. Different than the 64 × 64 FPA, the CDS and output buffers in the channel readout circuit are replaced with a common output buffers placed after the channel multiplexers in the 128 × 128 FPA.

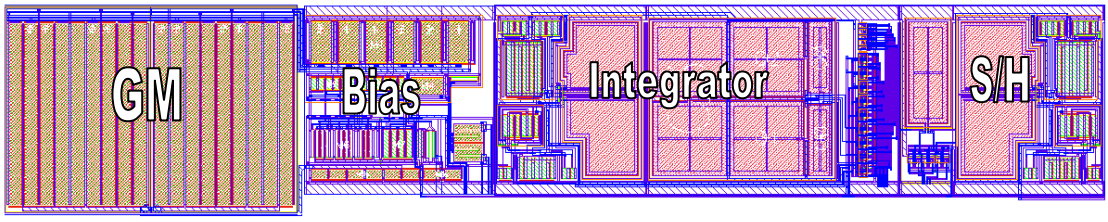


Figure 7.11: Layout of the analog channel readout circuitry. It measures 155 µm × 820 µm in a 3-metal 2-poly 0.35 µm CMOS process.

* The modification of the digital scanning circuit for the new 128 × 128 FPA with the external addressing capability has been performed by Murat Tepegöz.

Two of the channel readout circuits are placed next to each other in mirror symmetry, and 16 of these double channel readout circuits are repeated with a pitch of 335 μm to form the 32 channel parallel readout circuit. The required power, analog bias, and digital control signals are routed on top of the readout circuit area using a horizontal bus structure. During drawing the layout, crossing of sensitive analog and digital lines are avoided as much as possible. When this is inevitable, shielding is applied using the metal-1 layer as shielding layer, and metal-2 and polysilicon as interconnect layer. Figure 7.12 shows a zoomed layout view of the 32-channel readout circuit, where only 12 of the readout channels are shown. The zoomed layout clearly shows the layout of the output multiplexers, power and signal bus, analog channel readout circuits, pixel multiplexers, and FPA pixels. Figure 7.13 shows the complete layout of the 32-channel analog readout circuit. It is composed of parallel readout channels, power and signal bus, channel output multiplexers (mux-0, mux-1), and pixel column multiplexers. There is also test channel placed at the left end of the channels. By integrating the test channel in the readout area considerable area is saved, since the dimensions of the chip is quite large and any extra area brings unacceptable empty spaces in the layout

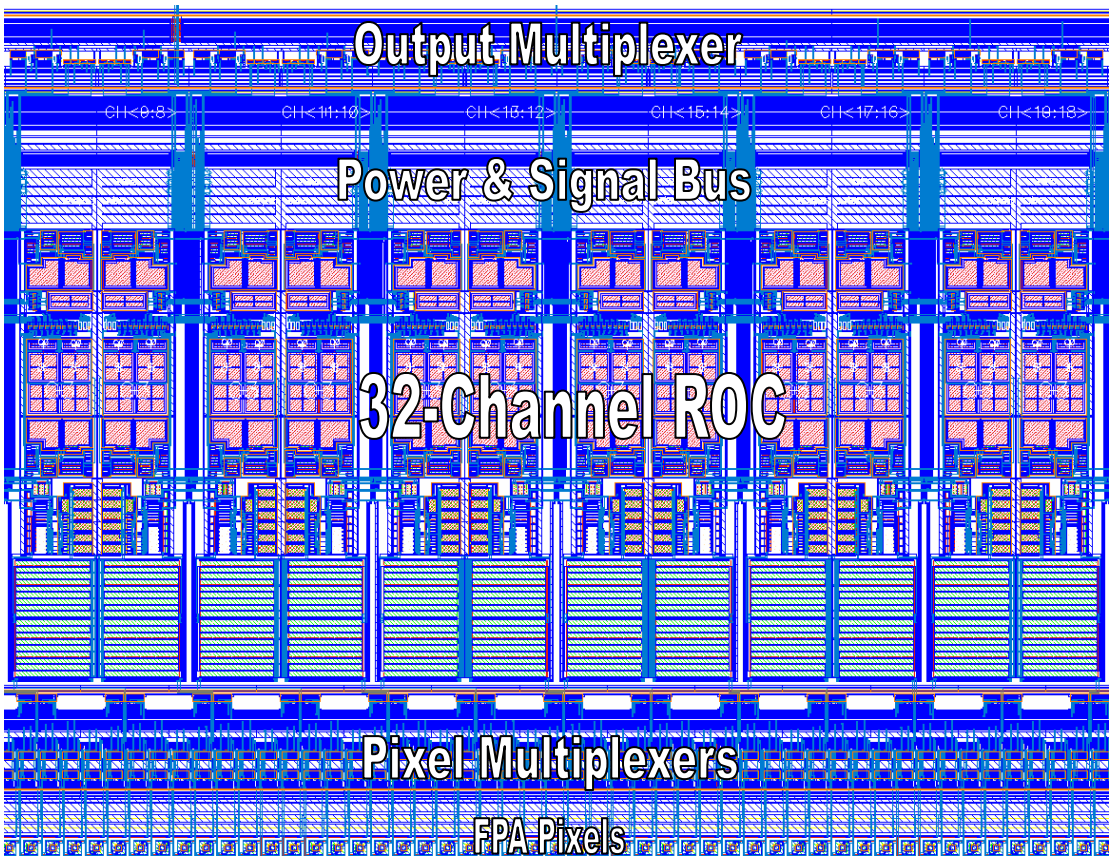


Figure 7.12: Zoomed layout view of the 32-channel readout circuit, where only 12 of the readout channels are shown.

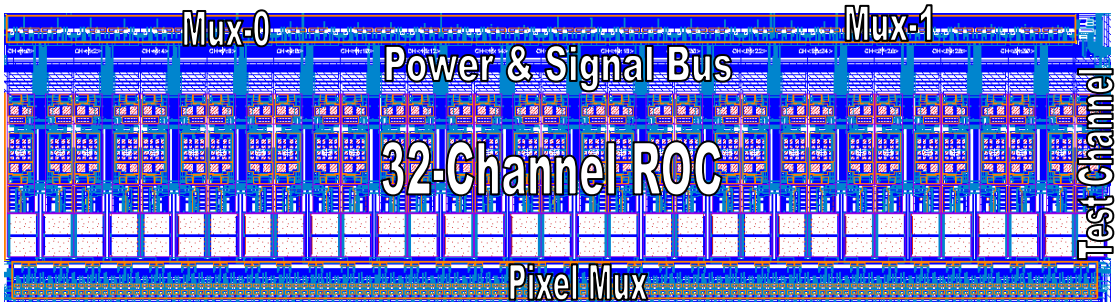


Figure 7.13: Complete layout of the 32-channel analog readout circuit.

7.6 On-chip Temperature and Vacuum Sensors

There are on-chip temperature and vacuum sensors in the 128 × 128 FPA. On-chip temperature sensors are used for temperature stabilization, and on-chip vacuum sensors are used to monitor the vacuum level of the package for the uncooled FPAs. In the 128 × 128 FPA, on-chip temperature sensors are

implemented using diodes and temperature sensitive resistors. On-chip vacuum sensors are implemented using suspended diodes and polysilicon resistors.

7.6.1 Temperature Sensors

On-chip temperature sensors in the 128 × 128 FPA are implemented using two methods: diodes and resistors. The diode type temperature sensors are implemented using diode connected vertical bipolar transistors readily available in the CMOS process and suspended p^+-active/n-well diodes obtained after a post-CMOS fabrication. The temperature sensors implemented with resistors use n-well layer of the CMOS process.

Figure 7.14 shows the schematic of a simple temperature sensor based on diode connected vertical bipolar transistors available in CMOS [63, 78]. The diodes are biased by a constant current source (I_o), and they have a ratio of 1:N. Therefore, their saturation currents carry also have the same 1:N ratio. The differential output voltage is given as

$$V_{out} = \frac{kT}{q}\ln\frac{I_o}{I_s} - \frac{kT}{q}\ln\frac{I_o}{NI_s} = \frac{kT}{q}\ln N \tag{7.10}$$

where, k is the Boltzmann constant, T is the absolute temperature in Kelvin, q is the electron charge, and N is the ratio of reverse saturation current values for the Q_1 and Q_2 [63, 78].

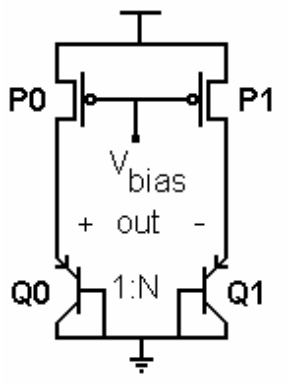


Figure 7.14: Schematic of a simple temperature sensor based on diode connected vertical bipolar transistors available in CMOS [63, 78].

Since the differential output is proportional to the absolute temperature (PTAT), and this type of sensors are called PTAT sensors. The dependence of bias current on temperature is cancelled out due the logarithmic difference to great extend. The designed PTAT sensor has an *N* value of 7, and provides a simulated temperature sensitivity of 165 μV/K (about 50 mK at 300 K). The temperature sensitivity of a single diode with larger area is simulated as –1.96 mV/K. Note that, the sensitivity of a single diode is larger, but it does not provide a PTAT output.

The noise performance of the designed PTAT sensor with vertical bipolar devices has been simulated, and integrated noise voltage of the single ended output from 0.1 Hz to 100 Hz is determined as 70 nV. Considering the fact that the temperature sensitivity of the single-ended output is 2 mV/K, minimum resolvable (substrate) temperature difference becomes 35 μK, which is small enough for many temperature stabilization tasks. For the differential output case, the noise increases by a factor of √2, and it becomes 100 nV, which corresponds to a minimum resolvable (substrate) temperature difference of 0.6 mK. It is possible to improve the noise performance of the PTAT circuit provided that a lower bandwidth is used. For the uncooled detectors, it is necessary to control the temperature of the substrate within range of ± 10 mK. This requirement is relaxed considerably for the case where the array pixels are read out with respect to a reference pixel, canceling out the dependence of the detector output to operating temperature. Considering these, it is clear that the designed PTAT temperature sensors provide much better performance than actually required. In the chip, there are three PTAT sensors to monitor the chip temperature. Two of them are constructed using vertical bipolar transistors, while the other is constructed using the reference pixels used in the FPA. One of the bipolar based PTAT sensors is placed on top of the chip, and the other one is placed on the bottom of the chip together with the sensor constructed using reference pixels. Figure 7.15 shows the layout of two PTAT sensors. The upper one uses diode type reference pixels, while the lower one uses bipolar transistors with integrated current sources.

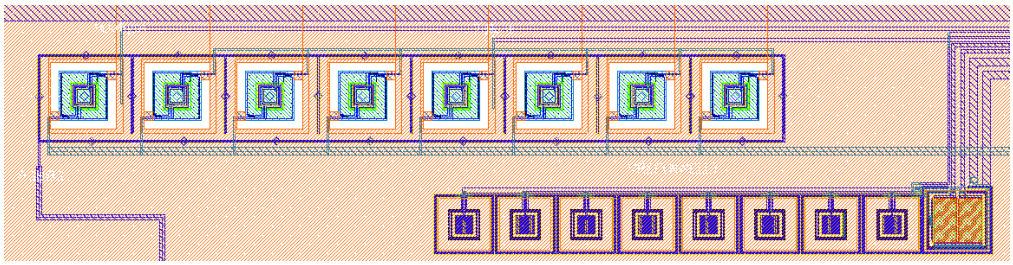
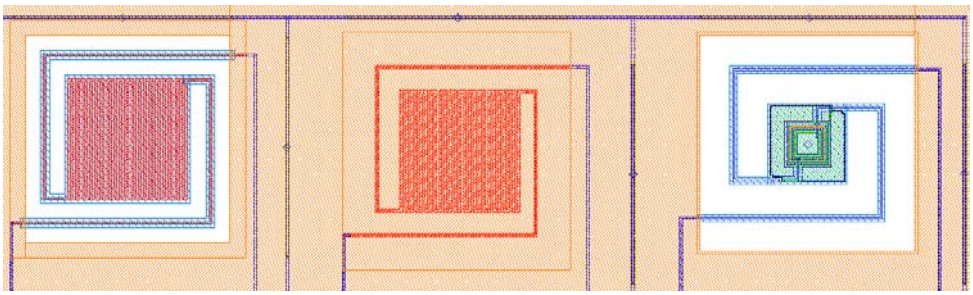


Figure 7.15: Layout of two PTAT sensors. The upper one uses diode type reference pixels, while the lower one uses bipolar transistors with integrated current sources.

On the chip there is also a resistive temperature sensor implemented using n-well layer. The implemented resistance value is 10.5 kΩ with a TCR value of 0.65 %/K. If the sensor is biased at 30 μA, the sensor resistor would provide a temperature sensitivity of 2.05 mV/K, which is close to that of a single diode. The thermal noise of the resistor will be 0.132 μV in 100 Hz bandwidth, which corresponds to 66 μK of minimum resolvable temperature change. Note that this is comparable to that of the single ended diode output, but does not give the absolute temperature. It is also possible to use such devices in temperature stabilization circuits.

7.6.2 Vacuum Sensors

The microbolometer chips need to be operated under vacuum condition. Once the sensor is packaged, and the package is vacuum-sealed, it is very difficult to identify the inside vacuum level. Therefore, some vacuum sensors are integrated in the chip, and pads are assigned to them so that continuous monitoring of package vacuum level is possible. Microbolometer structures can be used to detect the vacuum level indirectly based on the variation of their thermal conductance value with the change in the vacuum level. In the chip, there are two types of vacuum sensors: resistive and diode type. Figure 7.16 shows the layout of the resistive and diode type vacuum sensors. Resistive vacuum sensor has a bridge circuit constructed with a variable and reference vacuum sensors using polysilicon resistors. Diode type vacuum sensor is implemented using a suspended n-well diode thermally shorted to the substrate using metal interconnects.



(a) (b) (c)

Figure 7.16: Layout view resistive and diode type vacuum sensors. Resistive vacuum sensor has a bridge circuit constructed with (a) a variable and (b) reference vacuum sensors using polysilicon resistors. (c) Diode type vacuum sensor is implemented using a suspended n-well diode thermally shorted to the substrate using metal interconnects.

7.7 Floor Plan and Chip Layout

Figure 7.17 shows the floor plan of the 128 × 128 uncooled IR imager chip. The chip is composed of 10 basic blocks: 1) pixel area with 128 × 128 array pixels and 1 × 128 reference pixels, 2) vertical shift register and row decoder circuits, 3) row select switches, 4) column select switches, 5) 32-channel analog readout circuit, 6) serial output multiplexers, 7) analog output buffers, and 7) digital timing control circuit. Figure 7.18 shows the layout of the 128 × 128 FPA chip. It measures 6555 µm × 7915 µm (52 mm^2) in a 3-metal 2-poly 0.35 µm CMOS process. Due to the fabrication requirements, regions outside the pixels are protected with a mask constructed using metal-3 mask.

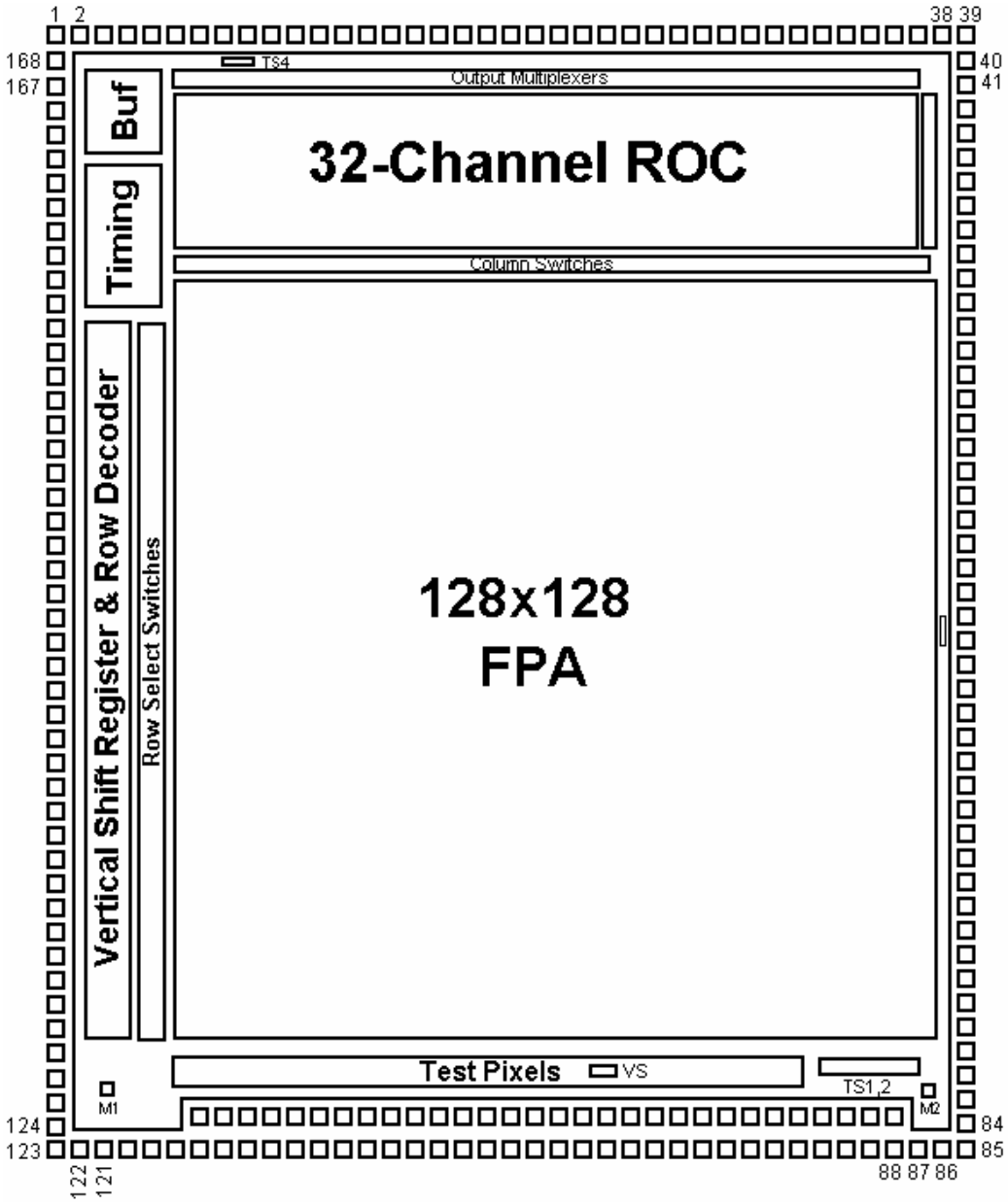


Figure 7.17: Floor plan and pad frame of the 128×128 FPA.

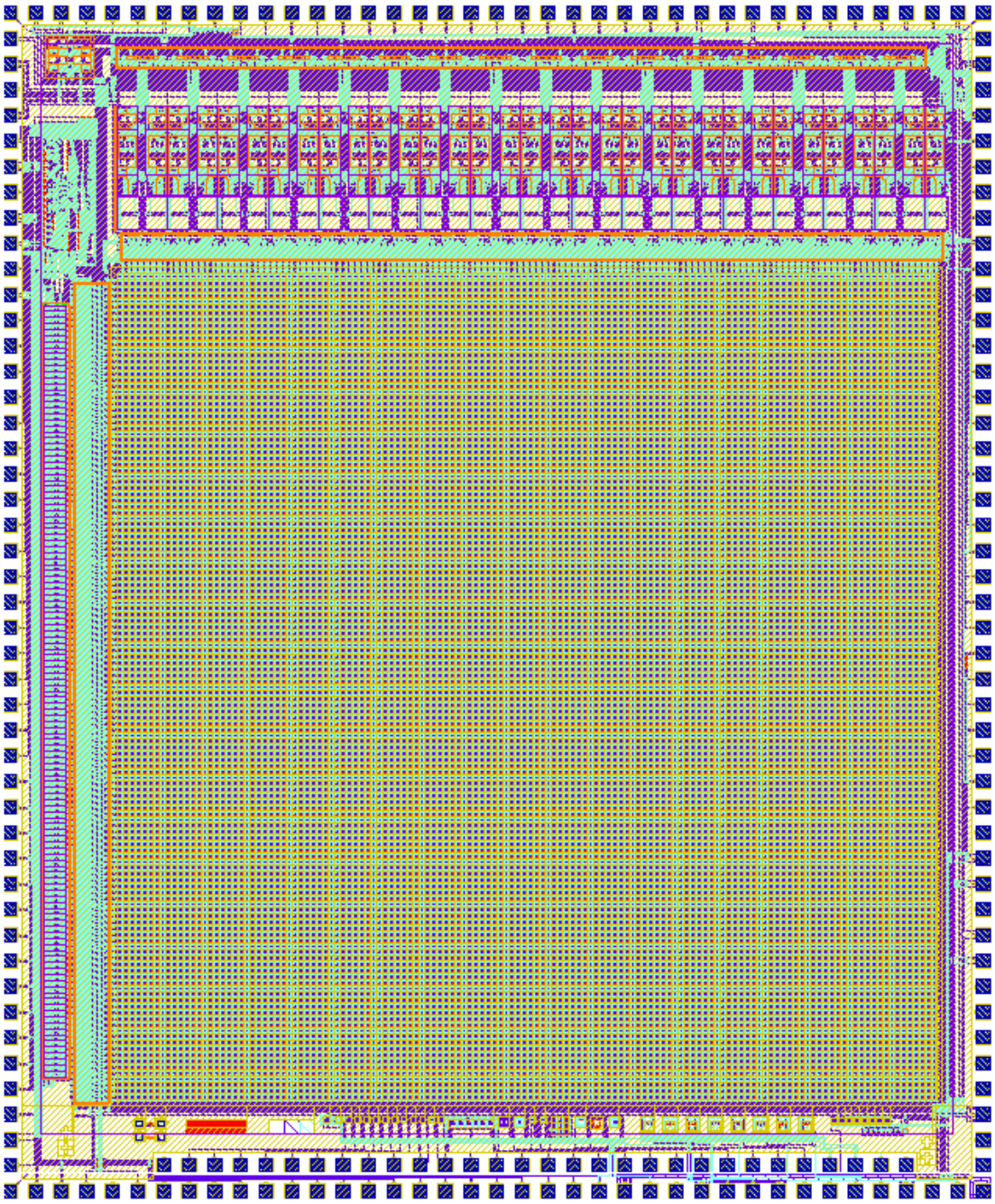


Figure 7.18: Layout view of the 128 × 128 imager chip. It measures 6555 µm × 7915 µm (52 mm^2) in a 0.35 µm 3M2P CMOS process.

7.8 Summary and Conclusions

This chapter presented the 128 × 128 uncooled infrared FPA chip. The 128 × 128 FPA is based on the p^+/n-well active diode microbolometers, which can be fabricated using a standard n-well CMOS process together with its monolithic readout circuitry without the need for any deposition and critical lithography steps. The new FPA has 16384 array pixels and 128 reference pixels, where the reference pixels are arranged in an identical single row above the 128 × 128 array pixels. The use of a row of reference pixels together with a differential readout circuit makes differential FPA voltages independent of pixel positions in the FPA, reducing the fixed pattern noise and improving the array uniformity. Furthermore, the dependence of the differential pixel output on the operating temperature is reduced dramatically, which relaxes the requirement for temperature stabilization. The 128 × 128 FPA chip has an integrated readout circuit with 32-channel parallel readout circuit, which is improved in terms of individual circuit block performance, implementation area, and overall block count and power consumption. The input referred offset voltage and matching of the input transconductance values are improved in the differential transconductance amplifier. The switched capacitor integrator (SCI) circuit is modified so that it can cancel its own offset voltage without the need for a correlated double sampling (CDS) circuit afterwards. Furthermore, a common buffer circuit is used at the multiplexed channel outputs. With these modifications, the power consumption of the 128 × 128 FPA is kept same as that of the 64 × 64 FPA despite the increase in the number of parallel readout channels. The 128 × 128 has also some on-chip sensors to monitor the chip temperature and package vacuum level.

The 128 × 128 FPA chip has an expected NETD value of 1 K at 30 fps for f/1 optics. This NETD value can be decreased below 350 mK by optimizing the post-processing steps and by decreasing the electrical bandwidth with the help of increased number of readout channels. Considering its simple fabrication process and moderate FPA performance, the proposed FPA together with its readout circuit can be used in many low-cost uncooled infrared imaging applications.

CHAPTER VIII

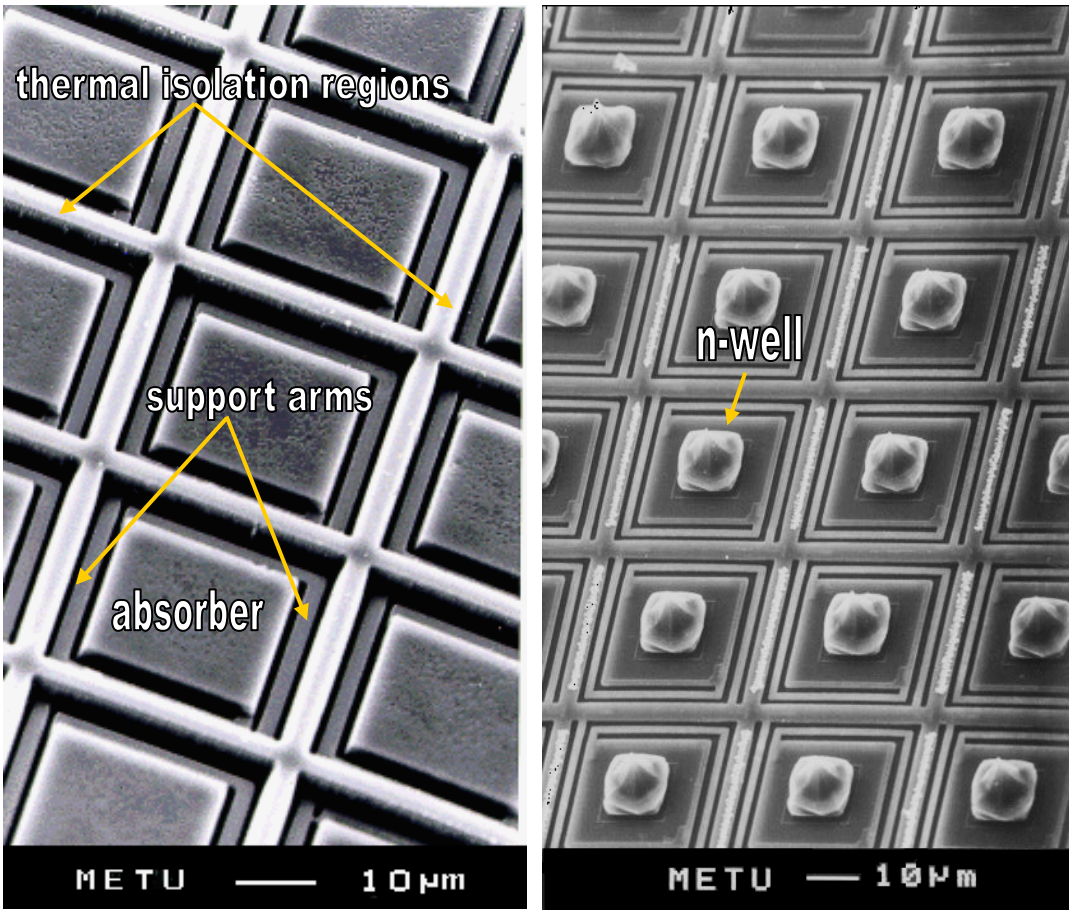
8 TEST RESULTS OF THE FABRICATED FPAS

This chapter gives the test results for the fabricated 64 × 64 and 128 × 128 FPAs developed within the framework of this thesis. Various electrical tests have been performed to verify the functionality of the fabricated 64 × 64 and 128 × 128 FPAs. These tests include verification of circuit operation for the digital and analog circuit blocks, as well as the uniformity measurement results of the array pixels voltages and their temperature sensitivities.

This chapter is organized as follows: Section 8.1 presents briefly the post-CMOS fabrication results of the 64 × 64 and 128 × 128 FPA, which is performed within the framework of another thesis [51]. Problems encountered during post-processing steps are summarized. Section 8.2 explains the test results of the 64 × 64 FPA. Test results of the digital and analog circuit modules are presented. The uniformity measurement results of the 64 × 64 FPA are presented, and the effect of fixed pattern noise due to the FPA routing resistances is discussed. Section 8.3 presents the test results of the 128 × 128 FPA, including the functional verification of the digital and analog readout circuit modules and uniformity measurement results of the array pixels and their temperature sensitivities of the CMOS fabricated FPAs. Finally, Section 8.4 summarizes the fabrication and test results of the 64 × 64 and 128 × 128 FPAs.

8.1 Post-CMOS Fabrication Results

Figure 8.1 shows the SEM photographs of the fabricated detector array pixels after post-CMOS processing showing (a) the top view and (b) the bottom view after removing pixels from the substrate using a sticky-tape [41, 42]. The post-CMOS processing steps start with a dry-etch step optimized specifically for the selected CMOS fabrication process. After dry-etch step, the detectors are suspended using the electro-chemical etch-stop technique using tetramethyl ammonium hydroxide (TMAH) solution where the silicon underneath the pixels is removed while preserving the n-well without being etched [43, 45]. These two steps are developed within the framework of another thesis [51].



(a) (b)

Figure 8.1: SEM photographs of the fabricated detector array pixels after post-CMOS processing: (a) top view and (b) bottom view after removing pixels from the substrate using a sticky-tape [41, 42].

There are two main problems that occur during the post-processing of the CMOS fabricated FPAs. These are the under-cut effect and damaging of the bonding pads, both of which occur during the electro-chemical etching process. In the under-cut effect, the solution etches also the side walls of the supporting silicon island between the pixels. The under-cut problem is more evident when the etching duration is kept long. The etching duration is kept longer, since the etch rate of the TMAH solution is lower at high concentration levels, which is required to minimize the surface roughness for improved etching success [79]. When the amount of under-cut increases, the silicon underneath the silicon islands are removed at some locations in the array, which causes the array to collapse and prevents proper operation of the array. Another problem is the loss of the bonding pads during etching. Although, the bonding pads are protected by manually deposited photoresist layer, some of the bonding pads are destroyed by the electro-chemical etching solution due to the fact that these pads are initially etched during dry etching process owing to the imperfections in the manually deposited photoresist layer. These two problems prevent the fabrication of fully functional thermally suspended uncooled IR imager chips. Currently, optimizations of the etching solution and post-CMOS fabrication steps are under development. The problems faced during etching can be eliminated considerably by performing the post-CMOS etching in wafer level, instead of chip level etching. The following sections present the test results of the readout circuit blocks in the 64 × 64 and 128 × 128 FPAs, including the FPA uniformity results performed using CMOS fabricated unsuspended chips.

8.2 Test Results of the 64 × 64 FPA

Figure 8.2 shows the CMOS fabricated 64 × 64 FPA placed in a 120-pin pin grid array (PGA-120) package, which is used for the electrical tests of the 64 × 64 FPA. Figure 8.3 shows the two-layer PCB designed for the electrical tests of the 64 × 64 FPA placed in a PGA-120 package. All the input, output, and power pins of the PGA-120 package are routed to the sides of the PCB and connected to the connectors for testing purposes. There is a switch circuitry on the PCB to apply digital control inputs to set some FPA features such as gain and integration time.

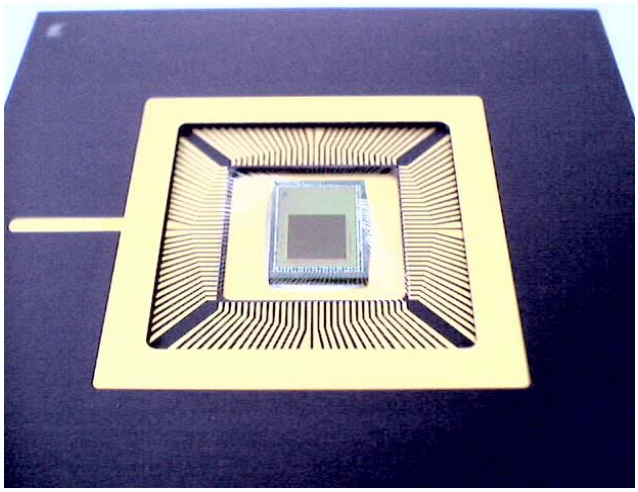


Figure 8.2: CMOS fabricated 64 × 64 FPA placed in a 120-pin pin grid array (PGA-120) package, which is used for the electrical tests of the 64 × 64 FPA.

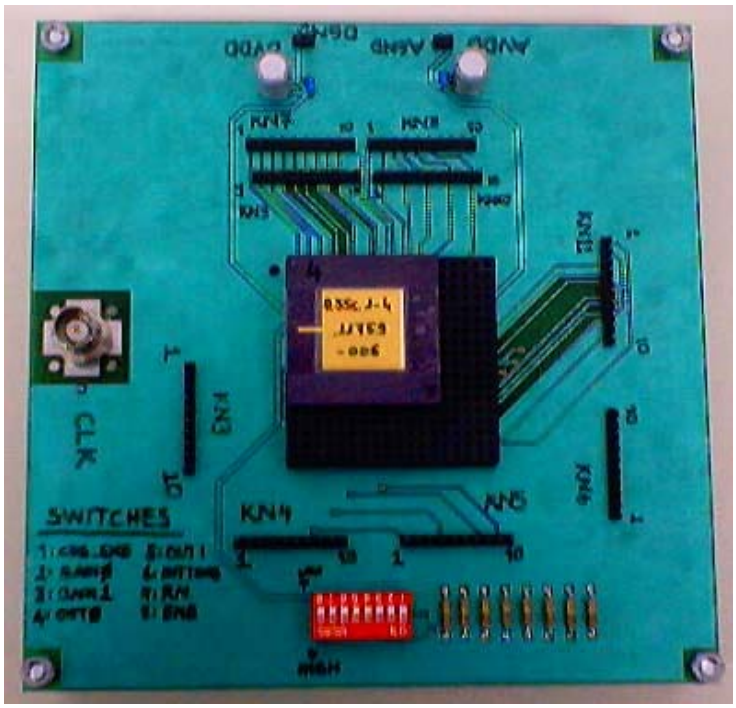


Figure 8.3: Two-layer PCB designed for the electrical tests of the 64 × 64 FPA placed in a PGA-120 package*. All the input, output, and power pins of the PGA-120 package are routed to the sides of the PCB and connected to the connectors for testing purposes. There is a switch circuitry on the PCB to apply digital control inputs to set some FPA features such as gain and integration time.

* This PCB has been fabricated by ASELSAN Inc.

The following sections give the details of the test results of the 64 × 64 FPA. First, the functionality of the digital scanning circuit is presented. Then, the test results of the analog readout circuit blocks are given. Finally, measured uniformity result of the CMOS fabricated unsuspended 64 × 64 array is presented, and possible effects of post-processing on the FPA uniformity is discussed.

8.2.1 Test Results of the Digital Scanning Circuitry

The test of the digital circuitry includes the verification of the on-chip generated digital signals for addressing the rows and columns in the FPA, and for timing of analog readout circuits. Figure 8.4 shows the block diagram of the digital scanning circuit used for addressing the FPA pixels and timing the analog readout circuit.

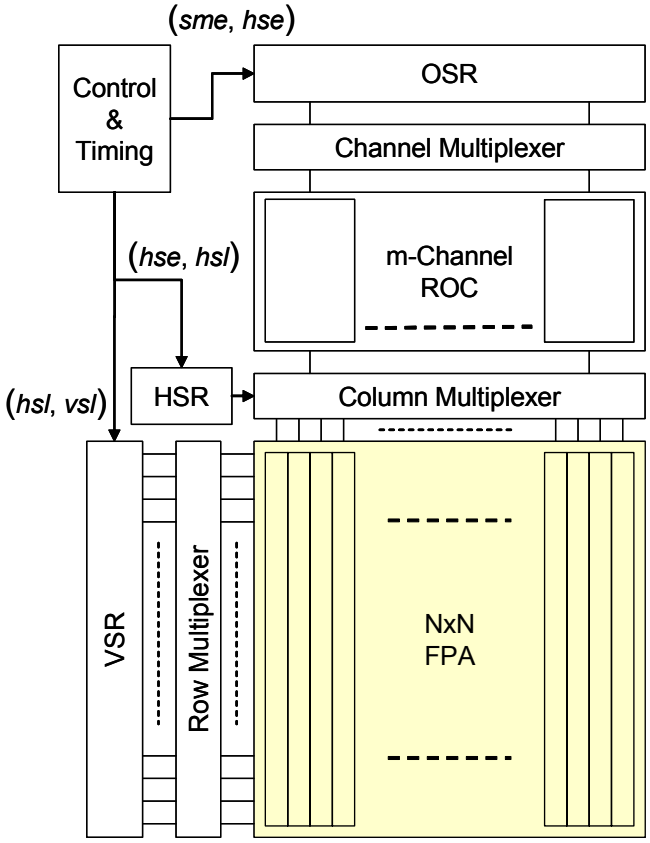


Figure 8.4: Block diagram of the digital scanning circuit used for addressing the FPA pixels and timing the analog readout circuit.

The 64 × 64 FPA pixels are addressed by a 64-bit vertical shift register (VSR) and 4-bit horizontal shift register (HSR). The FPA pixels are grouped in 16 columns readout by 16-channel parallel readout circuit. The channel outputs are scanned by a 16-bit output shift register (OSR). The control and timing circuit generates the required control signals for the HSR, VSR, and OSR. Each of the registers is controlled by an enable and load signal, which are indicated in the block diagram. Control signals for the shift registers are serial multiplexer enable (*sme*), horizontal shift enable (*hse*), horizontal shift load (*hsl*), and vertical; shift load (*vsl*). The functions of these signals are explained in detail in Chapter VI.

Figure 8.5 shows the scope view showing generation of *sme*, *hse*, and *hsl* signals from top to bottom, respectively. There are 16 pixels selected in a single row at a given time. Each pixel voltage is converted to current and integrated. After the integration, the pixel signal is sampled and hold for a sufficient time so that a top-most multiplexer can multiplex these signals to a serial output with an output rate of about 123 kpixel/s (122880 pixel/s), which corresponds to 30 fps for a 64 × 64 FPA. To perform this multiplexing operation, the channel outputs are scanned 16 times faster than the addressing frequency of a single pixel. Addressing of the channel outputs are performed by the channel multiplexer whose select signals are applied by the OSR. The content of the OSR has a single high bit shifted synchronously. After completing the scanning of the channels, a new high bit is loaded into OSR. The shift operation of the OSR is controlled by the serial multiplexer enable signal (*sme*), and the load operation is controlled by the enable signal of the horizontal shift enable (*hse*). When the 4-bit horizontal shift register is enabled and shifted, there are 16 successive *sme* signals, with a frequency ratio of 16:1. Horizontal shift register also has a load control input, called horizontal shift load (*hsl*), which has a frequency equal to the $1/4^{th}$ of the *hse* signal.

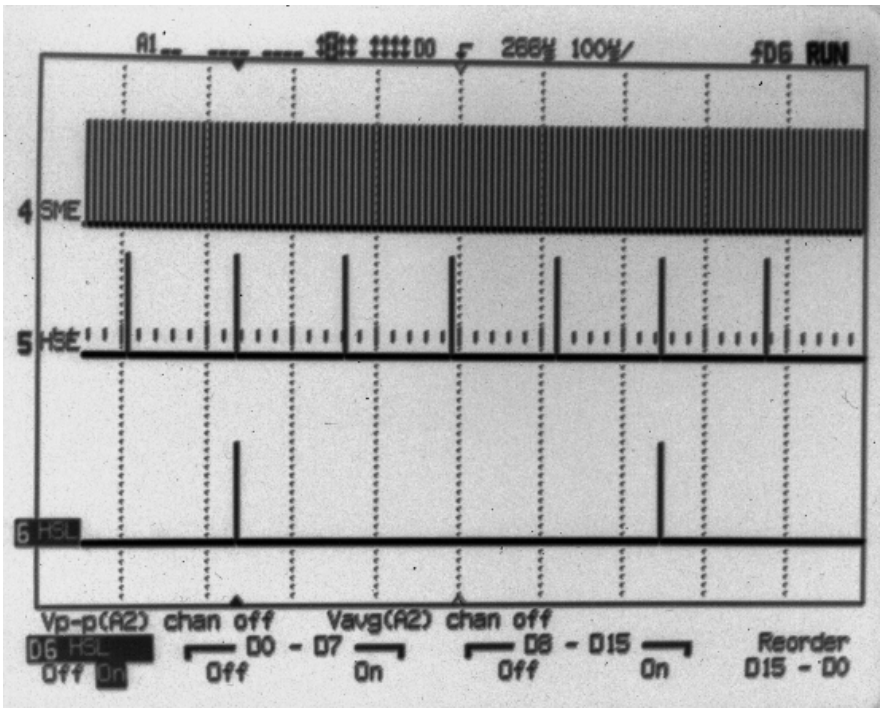


Figure 8.5: Scope view showing generation of *sme*, *hse*, and *hsl* signals from top to bottom, respectively.

Figure 8.6 shows the generation of *hsl* and *vsl* signals, which are the enable and load control signals for the VSR. There is a ratio of 64:1 in pulse densities. In order to have a clear snapshot, the system frequency is decreased to 400 kHz. When *hsl* is high, it indicates that the scanning of a row is completed, and the scanning of next row is started. Therefore, this signal is used as shift enable signal for the vertical shift register. The frequency of the load control signal for the vertical shift register is $1/64^{th}$ of the *hse* signal since there are 64 rows in the FPA. Each time *vsl* is high, a new frame is started; therefore, the frequency of *vsl* is equal to the frame rate. The 64 × 64 FPA is scanned at 30 fps by using a 1 MHz (983040 Hz) system clock signal.

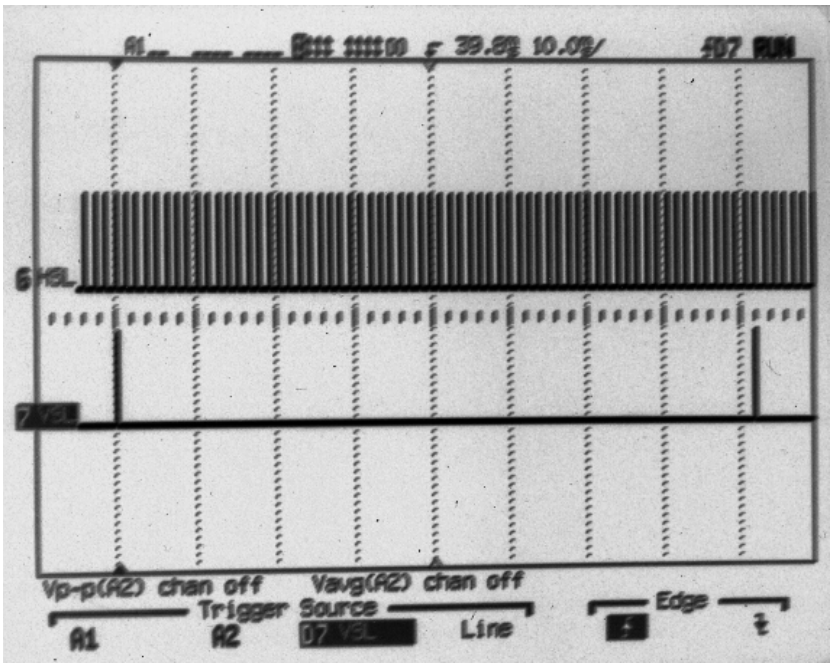
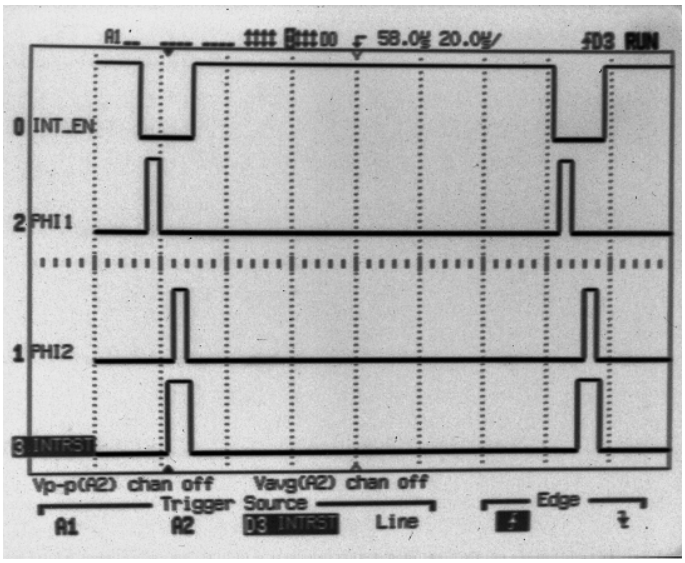
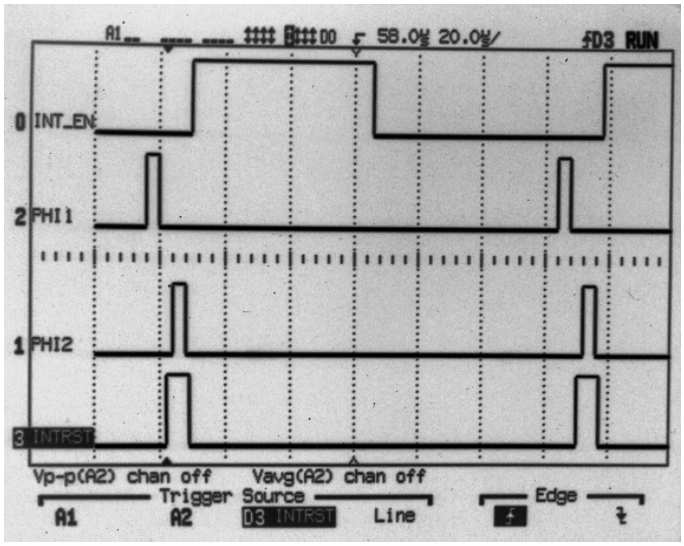


Figure 8.6: Scope view showing generation of *hsl* and *vsl* signals, which are the enable and load control signals for the VSR. There is a ratio of 64:1 in pulse densities.

Figure 8.7 (a) and (b) show the generation of integration enable signal (*int_enb*), two clock phases (*phi1* and *phi2*), and integration reset (*intrst*) signals when long (110 μs) and short integration time (55 μs) is selected, respectively. The *int_enb* signal determines the starting and ending points for integration by turning on and of a CMOS switch at the output of the differential transconductance amplifier. The *intrst* signal is used to rest the switched capacitor (SC) integrator. The output of the integrator is sampled first by a correlated double sampling circuit fallowed by a sample-and-hold circuit. The operation of these circuits is controlled by two phase clocking using *phi1* and *phi2*. The operation principles of these circuits are described in detail in Chapter VI. These tests verify that the on-chip digital circuitry generates the required signals properly. To operate the 64 × 64 FPA at 30 fps, the chip clock frequency should be 1 MHz (983040 Hz).



(a)



(b)

Figure 8.7: Scope view showing the generation of *int_enb*, *phi1*, *phi2*, and *int_rst* signals from top to bottom, respectively: (a) when long integration time (110 μs) is selected, and (b) when short integration time (55 μs) is selected.

8.2.2 Test Results for the Analog Test Channel

The tests of the analog circuit blocks in the readout channel are performed using the identical circuits placed in the test channel integrated next to the actual readout circuit. The use of the test channel allowed access to the input and output of each circuit module, which is not possible in the actual array. The modules in the test

channel includes the differential transconductance amplifier, offset removal circuit, switched capacitor integrator circuit, correlated double sampling (CDS) circuit, sample-and-hold (S/H) circuit, and output multiplexer with buffer. During testing the rest voltage of the switched capacitor integrator and sample-and-hold circuit is set to be at 1.65 V. The digital timing signals required by the SC integrator, CDS, and S/H circuit can be applied externally using separate test pads. During testing, on-chip generated timing signals are fed back to these pins to simplify testing. In the coming sections, test results of these blocks will be given starting from the differential transconductance amplifier circuit.

8.2.2.1 Differential Transconductance Amplifier

Figure 8.8 shows the variation of output current of the transconductance (GM) circuit with respect to differential voltage. Positive output current indicates that current flows out of the GM circuit, which happened when the reference input is at higher potential. In this test, input common mode voltage is set as 1.65 V. The output current varies linearly between –0.01 V and 0.01 V, with a peak-to-peak variation of 20.4 μA. Corresponding transconductance value is 1050 μA/V at 70 μA bias current, which is very close to the designed value verifying that the transconductance stage operates as designed.

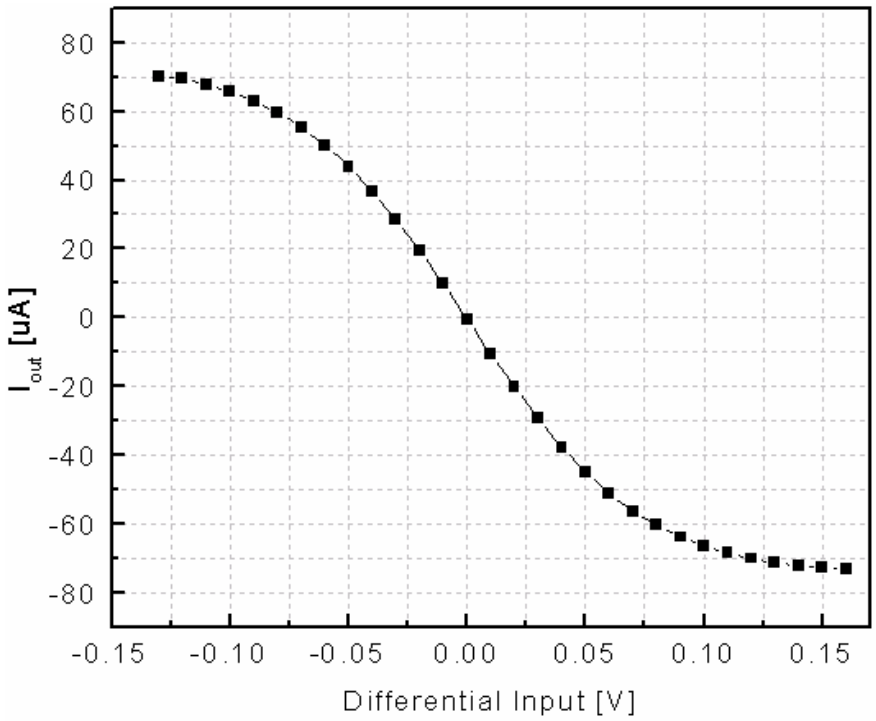


Figure 8.8: Measured variation of output current with differential input voltage. Total bias current is 70 μA. Transconductance value at the origin is recorded as 1050 μA/V.

A PCB is prepared for the noise test with all the required circuitry, including a 3.3 V supply and an adjustable bias voltage generators. The reference and pixel bias voltages are given by a 1.5 V (1.495V) battery placed also under the PCB. Then the PCB is placed in a metal box acting as a faraday cage. The output is taken via a BNC connector, and the power of the chip is taken from a ± 6 V batteries via a 9-pin connector. For the 9-pin connector a shielded cable is prepared. Figure 8.9 shows the prepared PCB placed in the faraday cage. Figure 8.10 shows the noise measurement setup where the test circuit is placed in a faraday cage powered by an external battery.

Figure 8.9: Prepared PCB and faraday cage for noise measurement. The test chip and all the required bias circuitry is on the PCB. The critical bias voltages are applied by a 1.5 V battery placed at the bottom of the PCB (not seen here). Output is taken via one of the BNC connectors, and power is applied by a 9-pin connector.

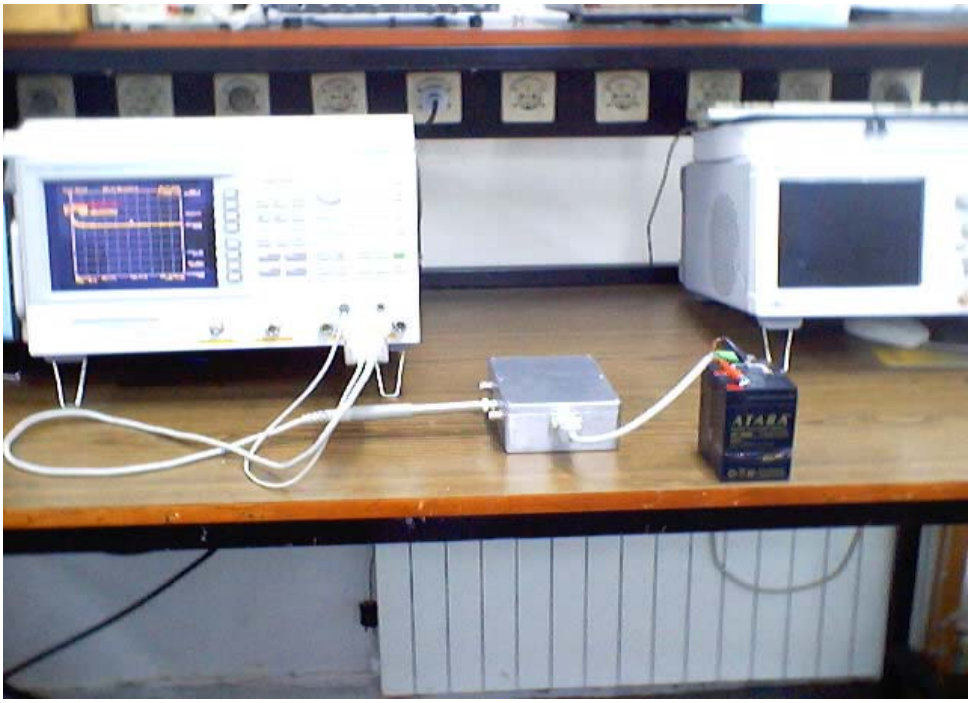


Figure 8.10: Noise measurement setup where the test circuit is placed in a faraday cage powered by an external battery.

Figure 8.11 shows the total measured noise spectral density of the preamplifier from 10 Hz to 4 kHz using a transimpedance amplifier with 39.2 kΩ feedback resistance. The measurement is performed using HP 4395A. The current output of the preamplifier is converted to voltage by a transimpedance amplifier. It is observed that the spectrum is free of the 50 Hz line components, which is due to the shielding of the faraday cage. The spectrum is close to the expected results.

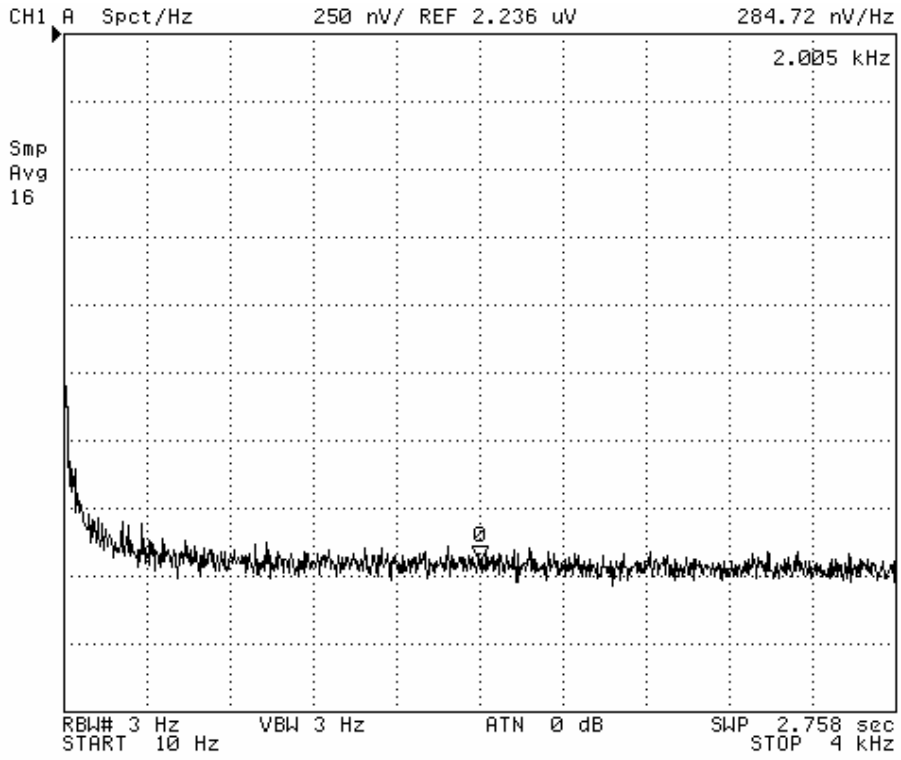


Figure 8.11: Total measured noise spectral density of the preamplifier from 10 Hz to 4 kHz using a transimpedance amplifier with 39.2 kΩ feedback resistance.

In order to minimize the errors in the calculations of the input referred noise of the transconductance amplifier, the gain of the complete circuit (GM stage and the transimpedance amplifier) is measured. This gain measurement is performed by applying a small signal voltage to the pixel input while keeping the DC value the same by using an AC coupling circuit formed with a 2.2 μF capacitor and 1 kΩ resistor. This is necessary since HP 4395A can not apply AC signals with DC offsets. Therefore, coupling is necessary, which causes a drop in gain at low

frequencies. Since this test is performed to verify the gain of the circuit, the drop in the low frequency is not considered, since this coupling stage is not used during noise measurement. In the actual noise test, both inputs are shorted to battery voltage without any coupling. This is achieved with a jumper on the PCB. With this setup, total gain is measured 31.875 dB at 2 kHz, which is the middle of the 4 kHz band, which is far away from the 3 dB point of the coupling circuit. Taking 39.2 kΩ resistance into account, transconductance of the GM stage is found as 1001 µA/V, which is very close to the design value as shown previously with the DC measurements. Figure 8.12 shows the measured transconductance values at varying frequencies. Reference input is kept at DC and AC signal is coupled to the Pixel input. The low values close around DC is due to AC coupling. Common mode input voltage is set as 1.65 V. From this measurement, it is understood that transconductance value is very close to the design value of 1000 µA/V.

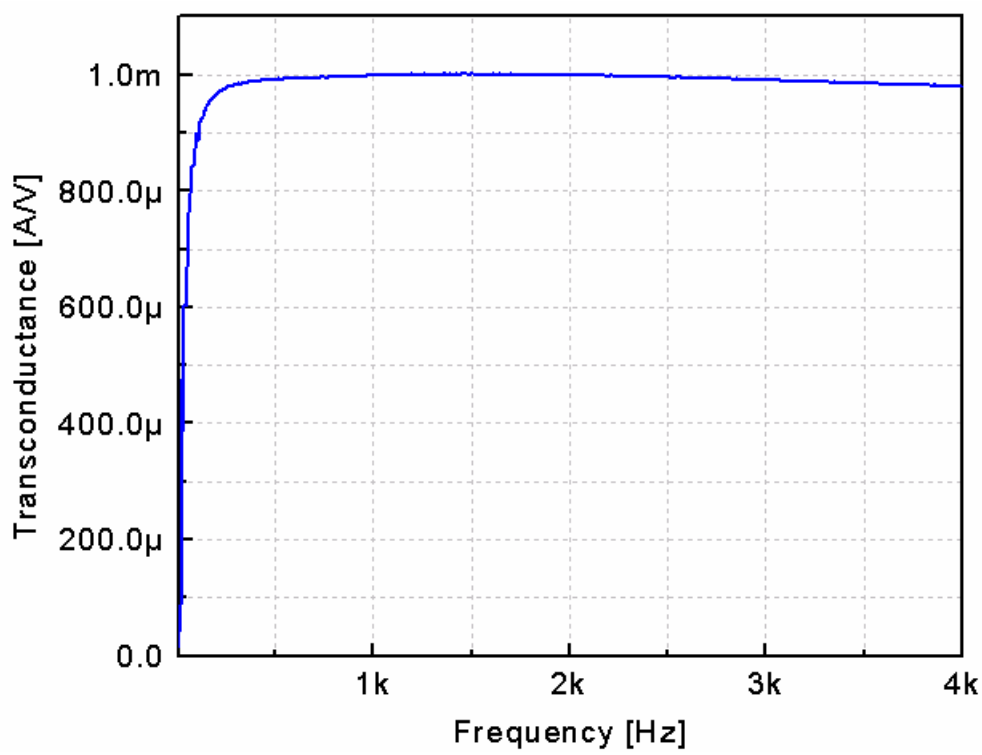


Figure 8.12: Measured transconductance values at varying frequencies. Reference input is kept at DC and AC signal is coupled to the Pixel input. The low values close around DC is due to AC coupling. Common mode input voltage is set as 1.65 V. From this measurement, it is understood that transconductance value is very close to the design value of 1000 µA/V.

Figure 8.13 shows the measured input referred noise spectral density of the differential transconductance amplifier. The recorded noise spectrum is analyzed in MATLAB. The transimpedance gain (39.2 K), and differential stage gain (1 mA/V) is used to calculate the input referred noise of the GM stage. By dividing the total result to the total gain, input referred noise is calculated. With this method average input noise of the GM stage is measured as 7.6 nV/√Hz, where total integrated noise is found as 0.48 µV rms in 10 Hz -4 kHz bandwidth. During the design, average input noise was simulated as 7.3 nV/√Hz in the same bandwidth. At this point it seems that the simulated and measured data match very well.

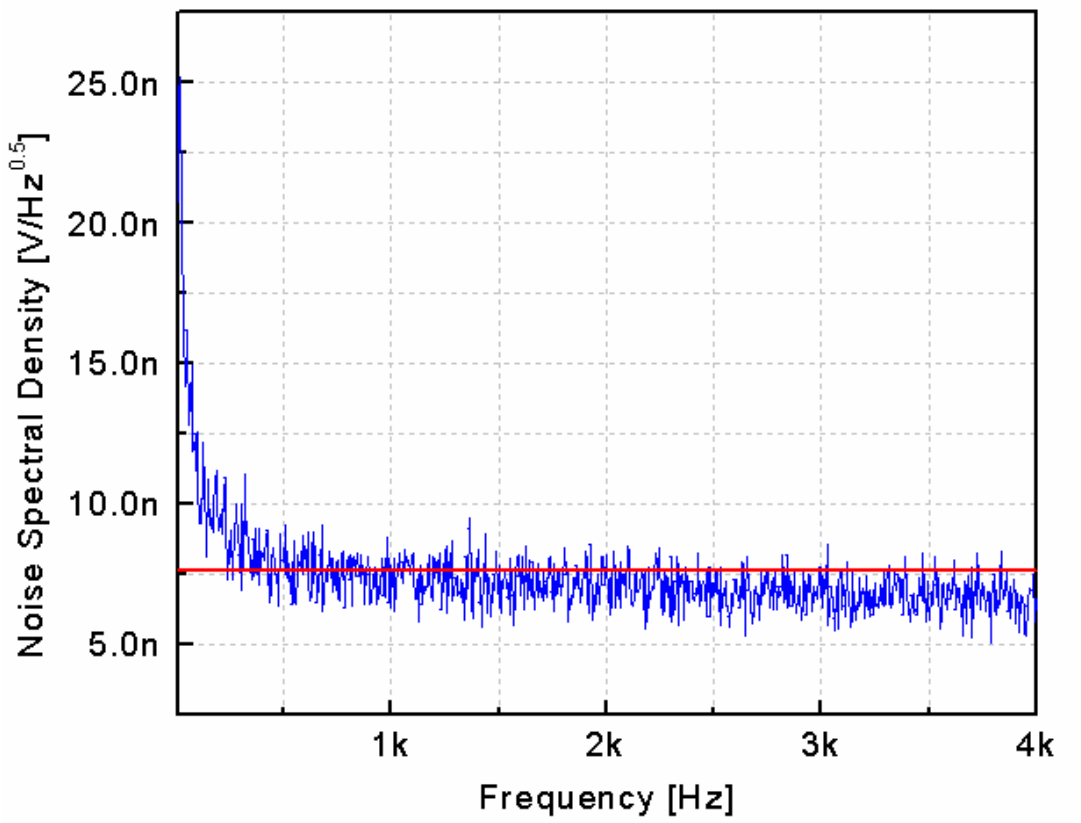


Figure 8.13: Measured input referred noise spectral density of the differential transconductance amplifier. Average density is 7.6 nV/√Hz, and is indicated by the horizontal line. Total integrated input noise over 4 kHz bandwidth is 0.48 µV rms.

8.2.2.2 Switched Capacitor Integrator

In the test of the SC integrator, both the differential transconductance amplifier and the offset current removal circuits are used. For proper timing, on-chip generated timing signals of *int_enb* and *int_rst* are fed from digital scanning circuit to the test circuits. Considering the fact that 1 mV change at the input of the transconductance amplifier causes about 1 μA change in the integrated current value, it is very difficult to test the integrator circuit with the normal settings. In other words, the gain of the differential transconductance amplifier should be decreased by decreasing its bias current. To do this, bias voltage of the differential stage is decreased from 1.7 V to 700 mV. The gate voltage (*bias_isink*) of the p-channel transistor in the offset current removal stage is biased so as to obtain maximum bias current in that stage. Tune voltage is changed between 0 – 200 mV, and it is observed that output current varies from negative to positive values. The channel multiplexer is programmed so as to pass the integrator signal to the output pin.

There are two variables that can be changed during the test of SC integrator: 1) integration time, and 2) integration capacitors. Both of these variables are digitally controlled. Integration time has two modes: short and long, which is controlled by the *intime_sel* input. When it is low, integration stops before at the middle of pixel select time, and when it is high, integration continues close to the end of pixel select time. Value of the integration capacitance is selected digitally by a 2-bit digital control signal *int_gain<1:0>*. Integration capacitance can take values of 1.25 pF, 2.5 pF, 5 pF, and 10 pF when the int_gain<1:0> increases from binary "00" to "11". Figure 8.14 shows the scope view of the SC integrator output with reset and integration enable control signals. Integrator outputs are recorded for integration capacitance values of 1.25 pF (lower trace), 2.5 pF, 5 pF, and 10 pF (upper trace). In this test integration time is kept long (110 μs), and input current is set to be about 180 nA. Figure 8.15 shows scope view of the integrator output when the integration capacitance is kept at 10 pF and integration time is short (55 μs). In this test, the input current is kept same at 180 nA, however, the output can not fall to the value reached in the previous scope view due to the shortened integration time.

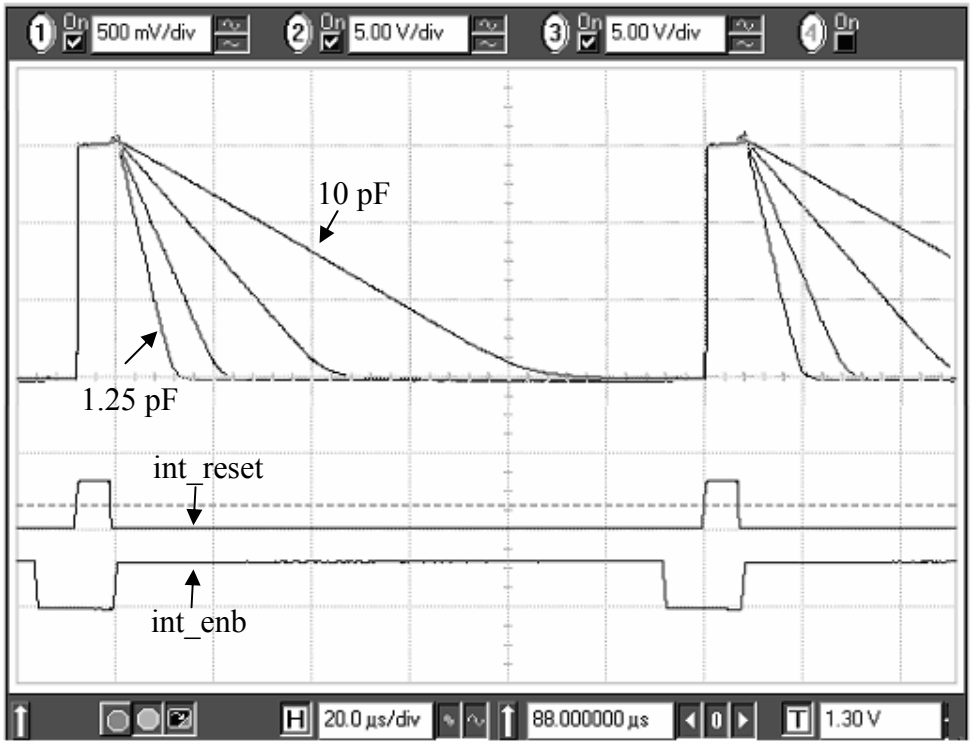


Figure 8.14: Scope view of the SC integrator output with reset and integration enable control signals. Integrator outputs are recorded for integration capacitance values of 1.25 pF (lower trace), 2.5 pF, 5 pF, and 10 pF (upper trace).

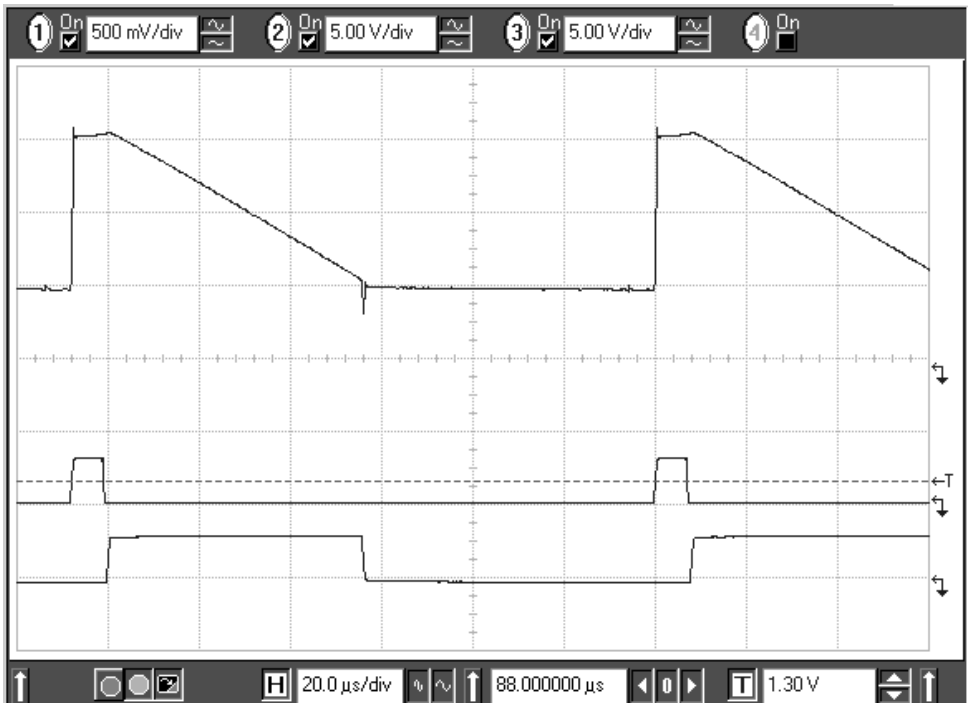


Figure 8.15: Scope view of the SC integrator output with 10pF capacitance and short integration time.

8.2.2.3 Sample-and-Hold Amplifier

In the 16-channel readout circuit, the input of the sample-and-hold (S/H) circuit is connected both to the integrator output and CDS output with a multiplexer, whose control input is *cds_enb* signal. When *cds_enb* is high, CDS output is sampled, and when it is low, integrator output is processed. In the test channel this is changed in order to be able to test each block individually. For this, the integrator input of the S/H circuit is connected to an external pad. In this way, by applying an external input, such as a sine wave, operation of the S/H circuit can be tested much more easily. Figure 8.16 shows the scope view of the S/H circuit output, where the input is a 500 Hz, 2 V peak-to-peak sine wave with 1.65 V DC offset. With a 1 Mhz system clock (30 fps scanning rate), sampling rate of the S/H circuit is about 7.8 K, which corresponds to about 16 samples in a period of a 500 Hz sine wave.

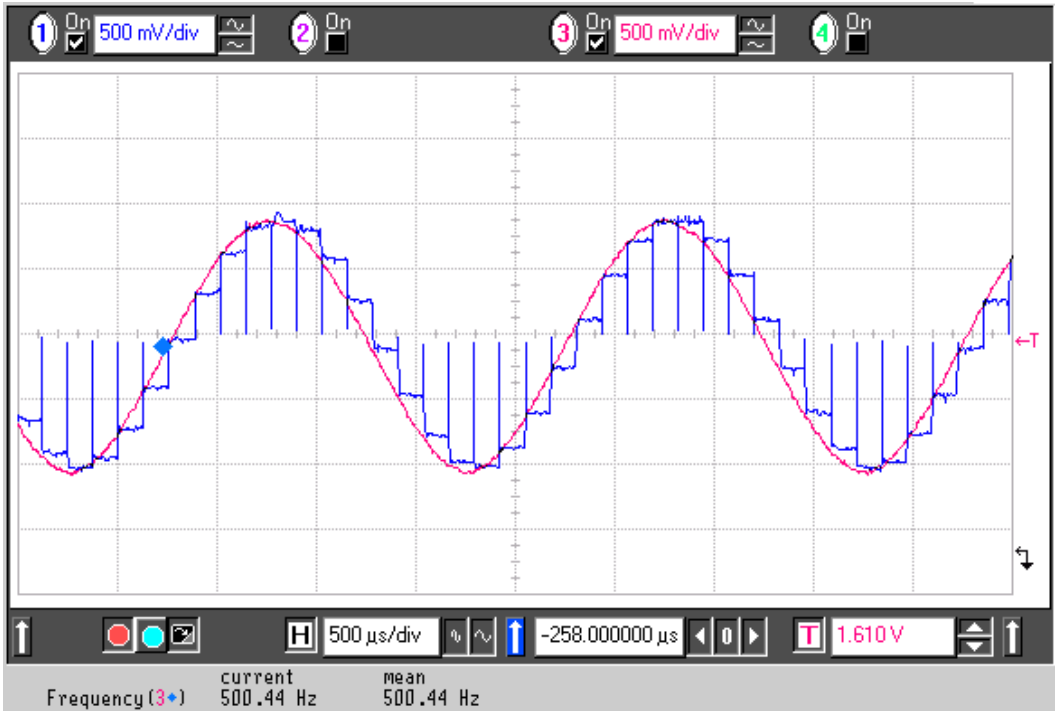


Figure 8.16: Scope view of the sample-and-hold (S/H) circuit output. Input is a 500 Hz, 2 V peak-to-peak sine wave with 1.65 V DC offset.

8.2.3 Uniformity Tests

Uniformity of the 64 × 64 FPA has been measured by recording the pixel voltages in the CMOS fabricated unsuspended FPA. The pixel voltages are amplified with a gain of 100 so that very small voltage variations can be resolved. To avoid saturation, only the signal above a known reference voltage is amplified. Figure 8.17 shows the schematic of the non-inverting amplifier used to measure the pixel voltages in the 64 × 64 FPA. A FET operational amplifier is used (LF353) to prevent loading of the FPA pixels. In the amplifier, the input resistance (R_1) is 68 Ω, and feedback resistance (R_2) is 6.81 kΩ, which results in a measured gain of about 101 V/V. With this high gain value, voltages as low as 20 μV have been successfully measured, which is easy to measure even with laboratory multimeters with 1 mV resolution or better.

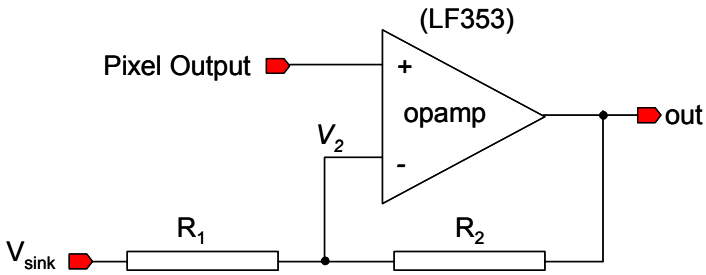


Figure 8.17: Schematic of the non-inverting amplifier used to measure the pixel voltages in the 64 × 64 FPA. R_1 is 68 Ω and R_2 is 6.81 kΩ. V_{sink} (1.45V) is used to prevent amplification of the DC part of the input signal. Gain is close to 101 V/V.

The pixel voltages are recorded using HP 34401A multimeter and the above given amplifier circuit. In the 64 × 64 FPA, 128 clock pulses is required to address the next pixel in the FPA. The required clock pulses are applied using the HP 33120A function generator adjusted in burst mode of operation with 128 clock pulses for a single trigger operation. The triggering of the function generator and multimeter reading are synchronized using a personal computer with a general purpose interface bus (GPIB) and running HP VEE program [84]. During the test, the FPA is programmed in such a way that the channel output multiplexers passes the

pixel voltages to the parallel channel output pins. The measurement is performed separately for each of the 16 readout channels each of them scans sub-arrays with 64 × 4 pixels, and the test is completed in 16 steps. Figure 8.18 shows the measured amplified output voltages for the 0^{th} channel of the 64 × 64 FPA. As the rows are scanned the pixel output voltage increases as the pixels get closer to the bias point, which is bottom of the FPA. That means output voltage increases as the pixel row number increases. Due to this effect, output voltages tend to increase as the rows are scanned from top to the bottom of the FPA, which corresponds to increasing the sample number in Figure 8.18. On the other hand, when a row is selected, output voltage decreases as the pixel is scanned from left to the right. In each row channel there are 4 pixels in a row, and they exhibit decreasing staircase signals for each row, with the increasing average as the row number increases. The recorded channel data are transferred into MATLAB and analyzed. Analysis was started by calculating the actual channel output values using the gain (101 V/V), and V_{sink} (1.45V) values. After that, each 64 × 4 channel values are combined and re-sampled to form the 64 × 64 array. Figure 8.19 shows the 3-D map of the measured pixel voltages in the 64 × 64 FPA [41]. Figure 8.20 shows the 2-D gray scale map of the measured pixel voltages in the 64×64 FPA. In order to understand the voltage variation better, lowest pixel voltage is mapped to black, and highest pixel voltage is mapped to white. The 2-D gray scale image have 16 strips with different average values, which is due to different offset voltages of each parallel readout channel.

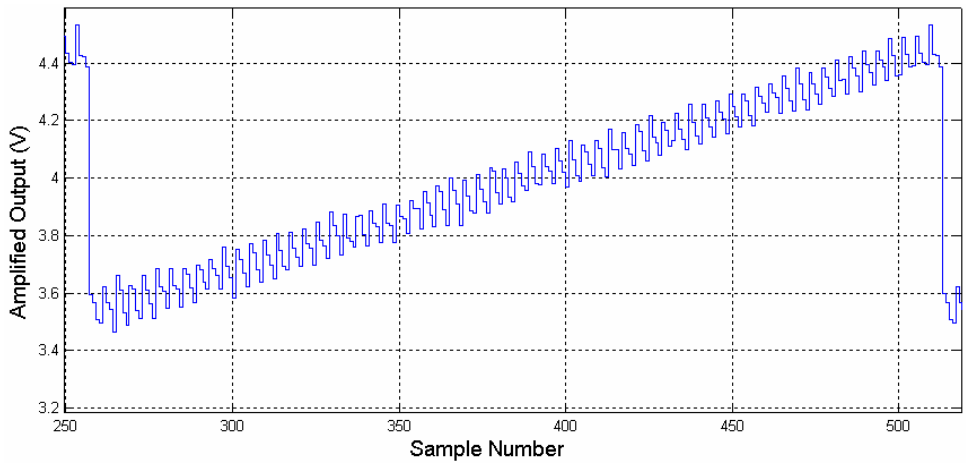


Figure 8.18: Measured amplified output voltages for the 0^{th} channel of the 64 × 64 FPA.

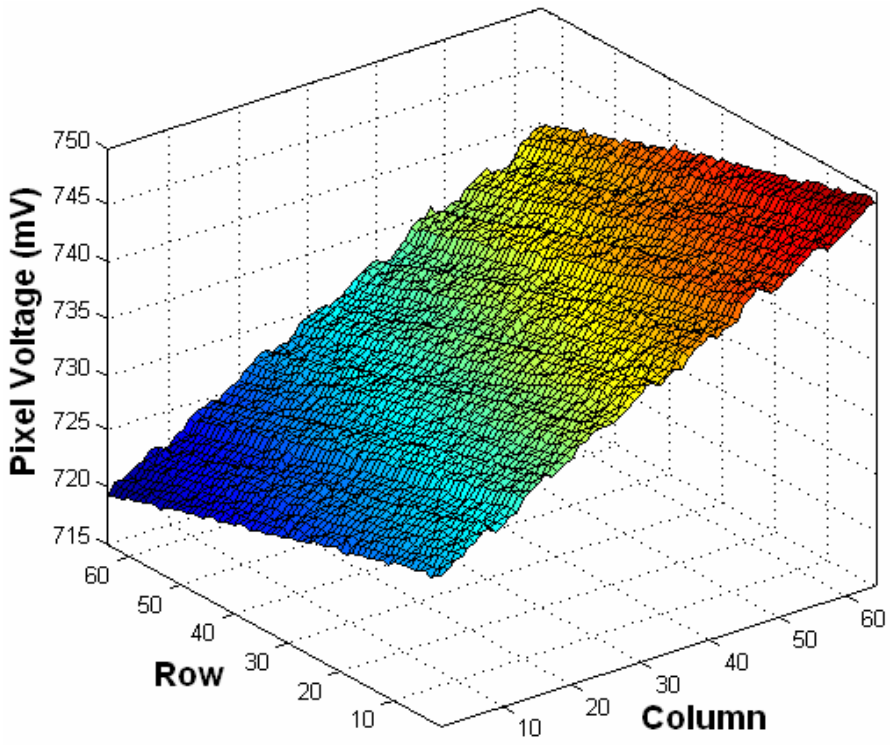


Figure 8.19: 3-D map of the measured pixel voltages in the 64 × 64 FPA [41].

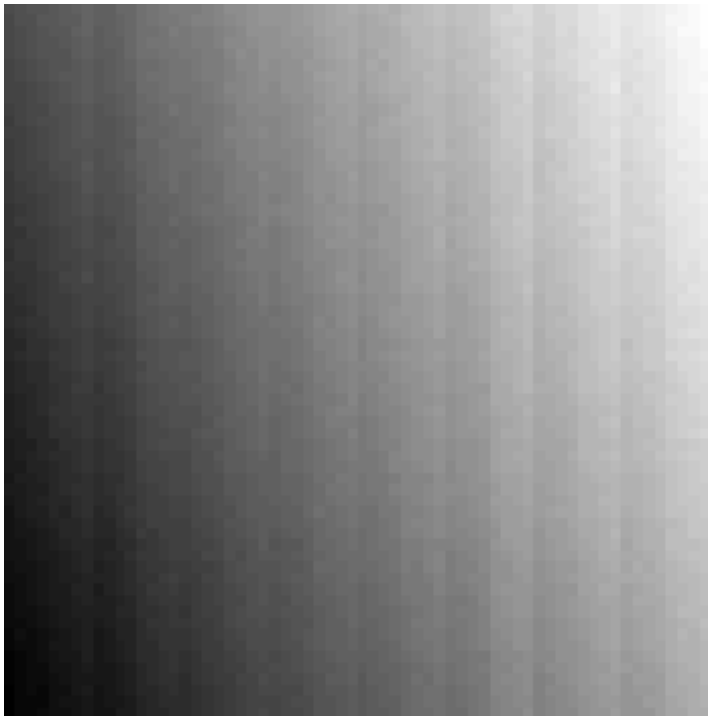


Figure 8.20: 2-D gray scale map of the measured pixel voltages in the 64×64 FPA. Top-left-most pixel is in the 0^{th} row and 0^{th} column. Therefore, lowest pixel voltage is observed towards to the bottom-left-most pixel, and they marked as black.

Figure 8.21 shows the measured histogram of the 4096 pixel voltages in the 64 × 64 without any non-uniformity corrections [41]. Pixel voltages have a mean value (μ) of 734.6 mV and standard deviation (σ) of 6 mV, which corresponds to a non-uniformity value of 0.82 %. Note that this very initial result includes both the routing resistance effects, and different offset values for different channels. There is a wide span in the measured data also results in an increased standard deviation value of 6 mV, including all the resistive voltage drops in the FPA.

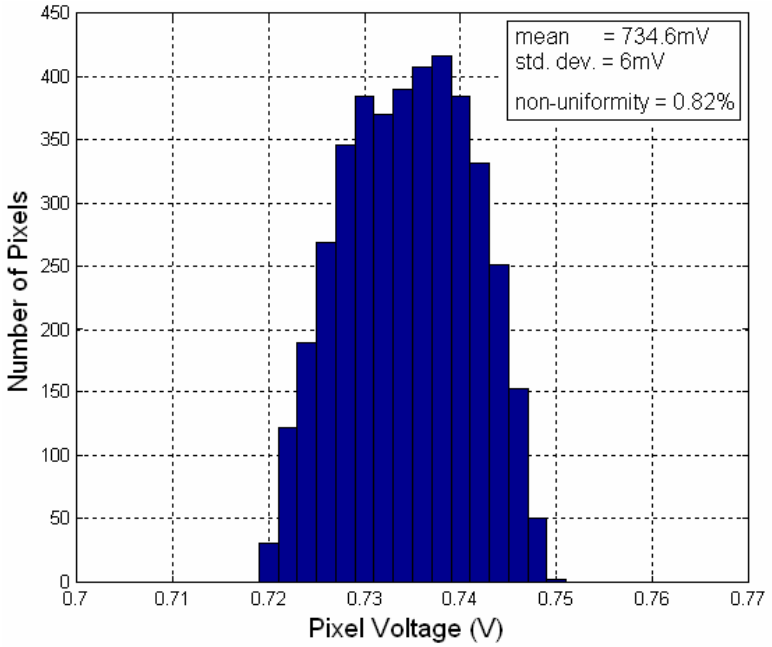


Figure 8.21: Measured histogram of the 4096 pixel voltages in the 64 × 64 without any non-uniformity corrections. Pixel voltages have a mean value (μ) of 734.6 mV and standard deviation (σ) of 6 mV, which corresponds to a non-uniformity value of 0.82 % [41].

Figure 8.22 shows the calculated resistive voltage drops due to the metal interconnects in the 64 × 64 FPA. The calculations and measurement results are in accordance. As expected the drop is the lowest at the lowest left most pixel in the array. Since the resistive voltage drop is easily calculated by a set of simple formulas, it can easily be compensated at least in MATLAB. Figure 8.24 shows the 3-D plot of the variation of the pixel voltages after compensating for resistive voltage drops along the routing lines and offset variations in the readout channels. Figure 8.24 shows the 2-D gray scale map of the pixel voltages given in Figure 8.23.

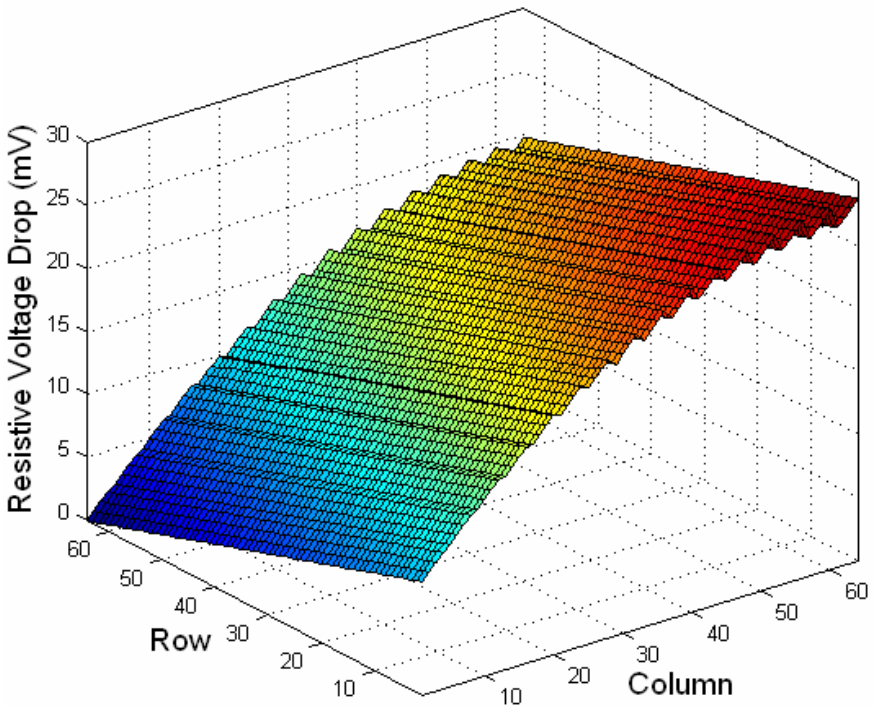


Figure 8.22: Calculated resistive voltage drops due to the metal interconnects in the 64 × 64 FPA. Peak-to-peak variation is 30 mV at 10 µA pixel bias current.

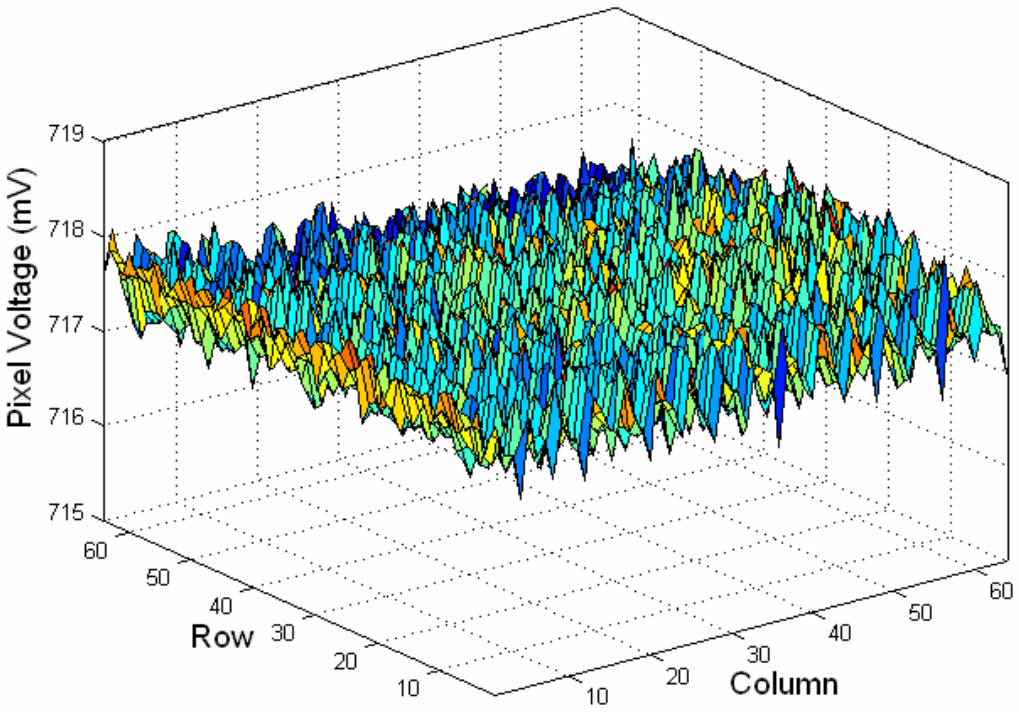


Figure 8.23: 3-D plot of the variation of the pixel voltages after compensating for resistive voltage drops along the routing lines and offset variations in the readout channels.

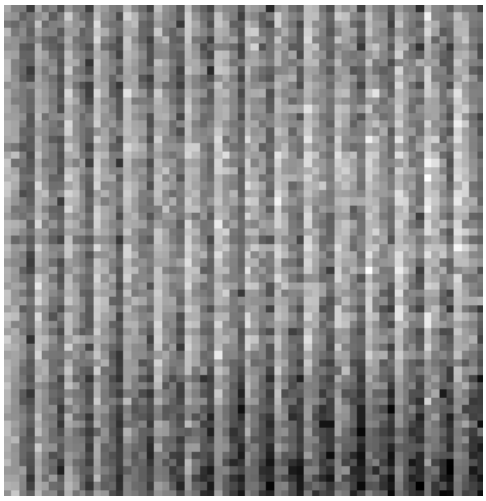


Figure 8.24: 2-D gray scale map of the pixel voltages given in Figure 8.23.

Figure 8.25 shows the histogram of the 4096 pixels after compensating for the resistive voltage drops and offsets in the readout channels. Mean value is 717.6mV, and the standard deviation is reduced to 0.33 mV with a non-uniformity value of 0.046 %. This histogram is plotted in the same interval as the previous case, and its spread is reduced. This result indicates that a great portion of the non-uniformity is due to the offsets in the channel readout and FPA routing.

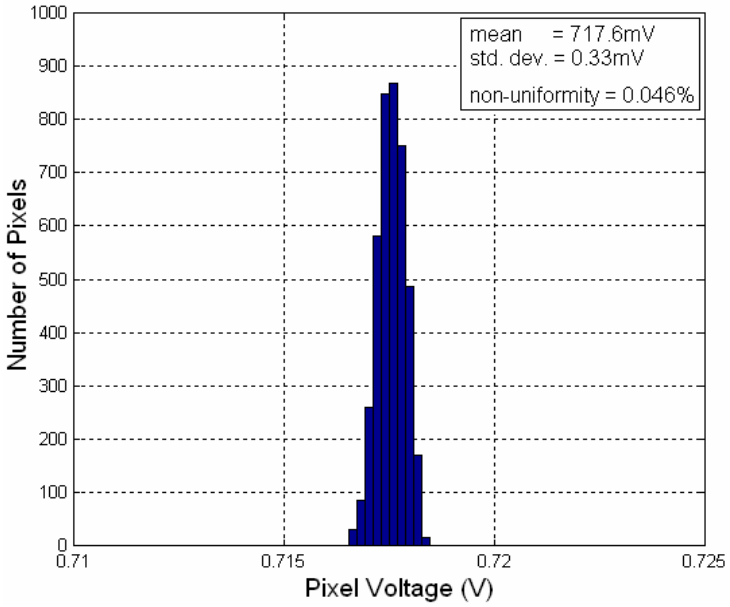


Figure 8.25: Histogram of the pixel voltages after compensating for the resistive voltage drops and offsets in the readout channels. Mean value is 717.6 mV, and the standard deviation is reduced to 0.33 mV with a non-uniformity value of 0.046 %.

8.3 Test Results of the 128 × 128 FPA

Figure 8.26 shows the multi-layer printed circuit board (PCB) prepared for the testing of the 128 × 128 uncooled imager chip placed in a PGA-144 package. The required bias generation circuitry and a 3.3 V power regulator is integrated on the PCB.

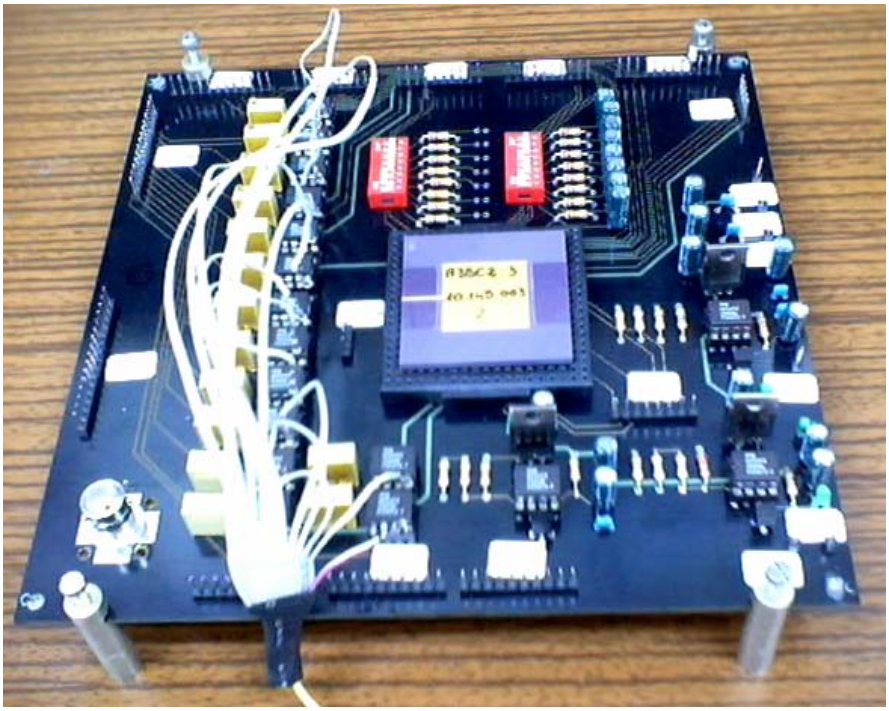


Figure 8.26: Multi-layer printed circuit board (PCB) prepared for the testing of the 128 × 128 uncooled imager chip placed in a PGA-144 package. The required bias generation circuitry and a 3.3 V power regulator is integrated on the PCB.

To verify the functionality of the 128 × 128 FPA, several electrical tests have been performed. These include the verification of the analog readout circuitry and the digital scanning circuitry. In addition to these, uniformity of all the 16384 pixel voltages in the array is measured together with their temperature sensitivities. As mentioned in the design section, the use of matched reference row helped to reduce the voltage non-uniformity about by a factor of 10. Due to the mature CMOS fabrication process, the uniformity of the temperature sensitivity of the array pixels is measured to be better than 3 %. The details of these tests will be given in the coming sections, starting with the test results of the digital scanning circuit.

8.3.1 Test Results of the Digital Scanning Circuit

The test of the digital circuits include the verification of the timing signals for the row and column selection, and generation of timing signals for the analog readout circuits, as given previously for the 64 × 64 FPA. Figure 8.27 shows the scope view of the decoded column select signals (*col<3:0>*) and the load (*col_ld*) and enable (*col_en*) control signals for the horizontal shift register (*HSR*) that controls the column multiplexers. System clock frequency is set as about 2.1 MHz (2097152 Hz) for 32 fps scanning rate. 32 fps is selected to be able to obtain a stable scope view. The scanning circuit completes the scanning of a row in four steps lasting 244.2 μs.

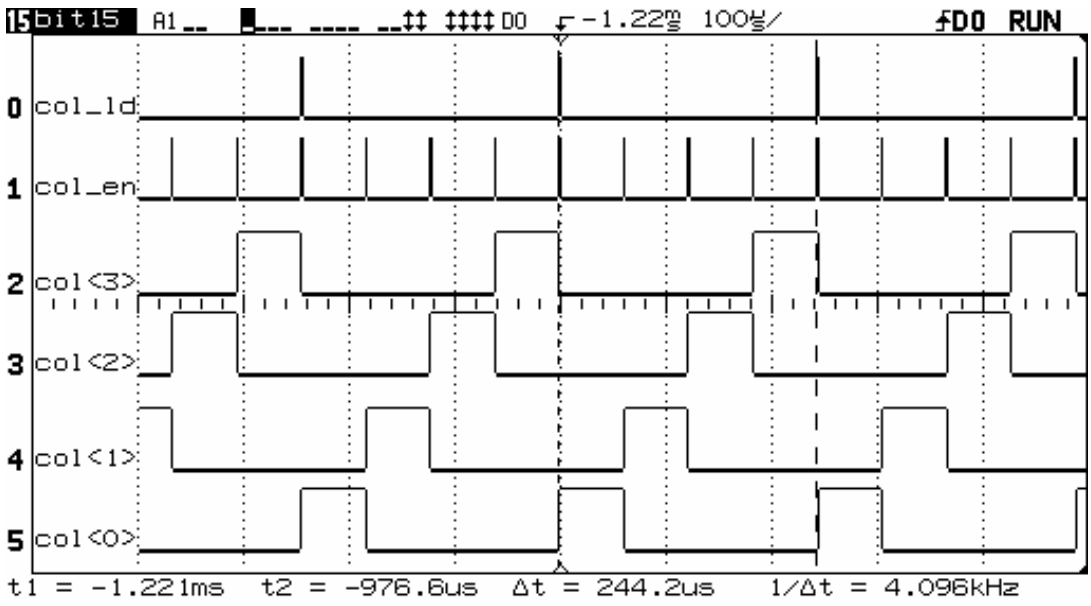


Figure 8.27: Scope view of the decoded column select signals (*col<3:0>*) and the load (*col_ld*) and enable (*col_en*) control signals for the horizontal shift register (*HSR*) that controls the column multiplexers. System clock frequency is set as about 2.1 MHz (2097152 Hz) for 32 fps scanning rate.

Figure 8.28 gives the scope view showing for the generation of row select signals verifying the correct operation of the vertical shift register (VSR). Row<0> and row<127> are select signals for the row multiplexer, which follow each other, indicating proper generation of the load and enable signals for the VSR. For proper demonstration, "delayed sweep" feature of the scopes used, enabling to zoom into a

particular window in the actual scope view given in the upper part of the scope window.

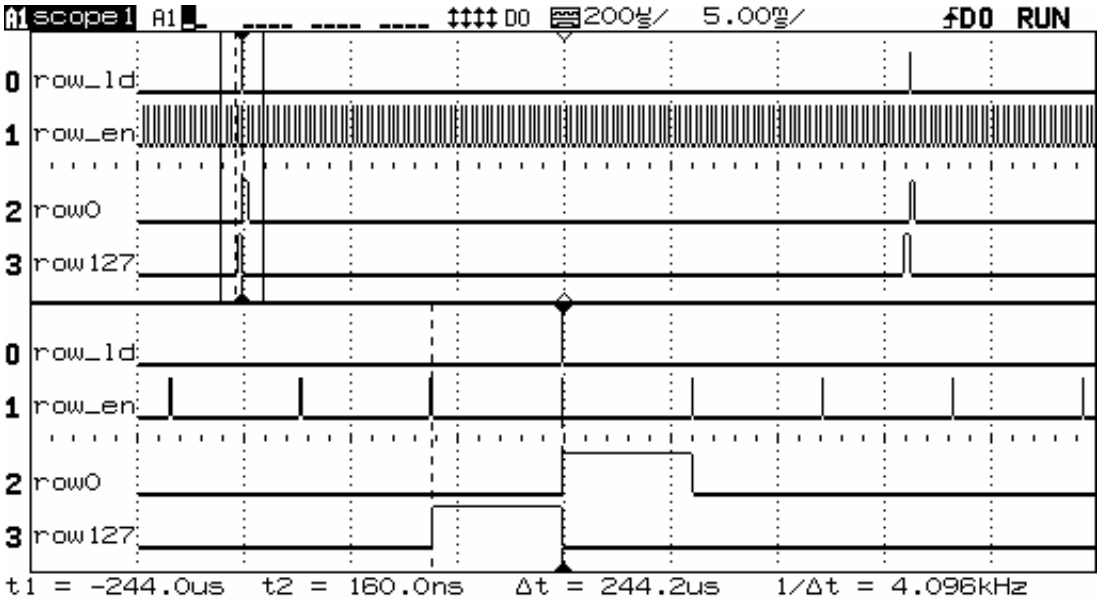


Figure 8.28: Scope view showing for the generation of row select signals verifying the correct operation of the vertical shift register (VSR). Row<0> and row<127> are select signals for the row multiplexer, which follow each other, indicating proper generation of the load and enable signals for the VSR. For proper demonstration "delayed sweep" feature of the scope is used, enabling to zoom into a particular window in the actual scope view given in the upper part of the scope window.

Figure 8.29 gives the scope view showing generation of integration enable signal (*int_enb*), sample-and-hold control signal (*phi2*) together with the pixel select signal (*col<3>*). In addition to that, most significant (*colm<15>*) and least significant (*colm<0>*) bits of the serial output multiplexer control signals are given. Integration starts after a certain time when the pixel is selected. When integration is stopped, integrator output is sampled at *phi2*, and serial output multiplexer passes the sampled channel outputs starting from the 0^{th} channel to the 15^{th} channel within one pixel select time with a certain offset in time as compared with the pixel select time to accommodate the required delays for resetting operation of the switched capacitor integrator.

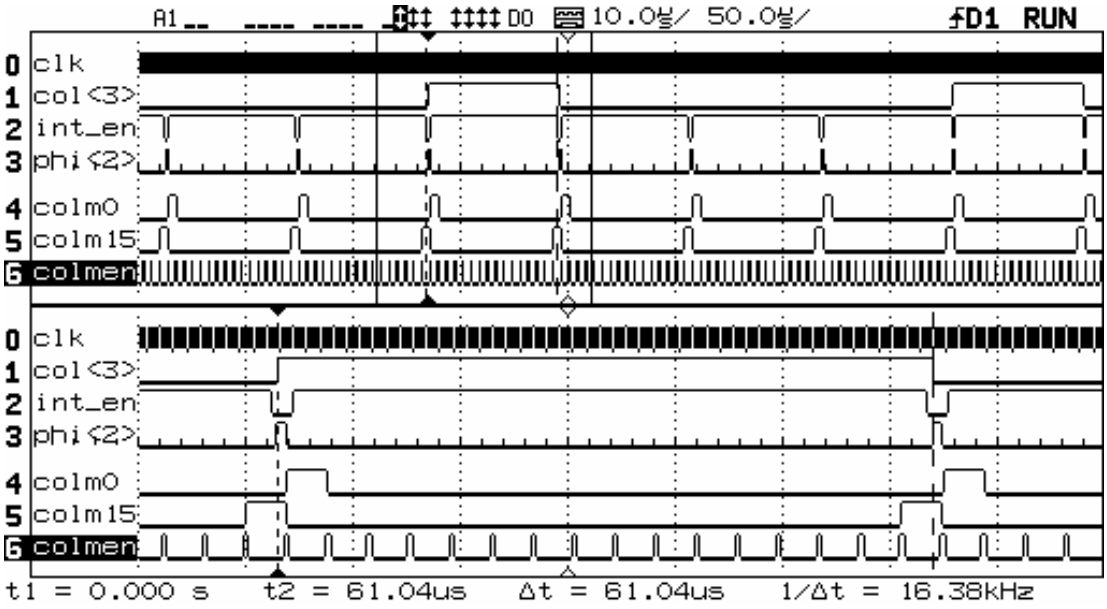


Figure 8.29: Scope view showing generation of integration enable signal (*int_enb*), sample-and-hold control signal (phi2) together with the pixel select signal (*col<3>*). In addition to that, MSB (*colm<15>*) and LSB (*colm<0>*) bits of the serial output multiplexer control signals are given.

8.3.2 Test Results of the Analog Circuits

The test of the analog circuit blocks have been carried out using an identical test channel integrated in the 128 × 128 FPA. The tests include the transconductance and noise measurement of the differential transconductance amplifier. The functionality of the on-chip scanning circuitry is verified. In addition, the array pixel voltage uniformity test results of the unsuspended 128 × 128 FPA have been presented. Furthermore, the uniformity of the temperature sensitivity of the array pixels has been measured and presented.

Figure 8.30 shows the variation of the output current of the differential transconductance amplifier in the 128 × 128 FPA with the differential input voltage measured with respect to a reference voltage at 1.65 V. The differential transconductance amplifier is biased at 74 µA and uses 3.3 V supply voltage. The circuit provides a transconductance value of 700 µA/V for a differential input voltage less than 50 mV. Figure 8.31 shows the measured variation of the voltage gain of the differential transconductance followed by a transimpedance amplifier with 100 kΩ

feedback resistance. The measured gain is 36.9 dB within 8 kHz bandwidth, corresponding to a transconductance value of 700 µA/V.

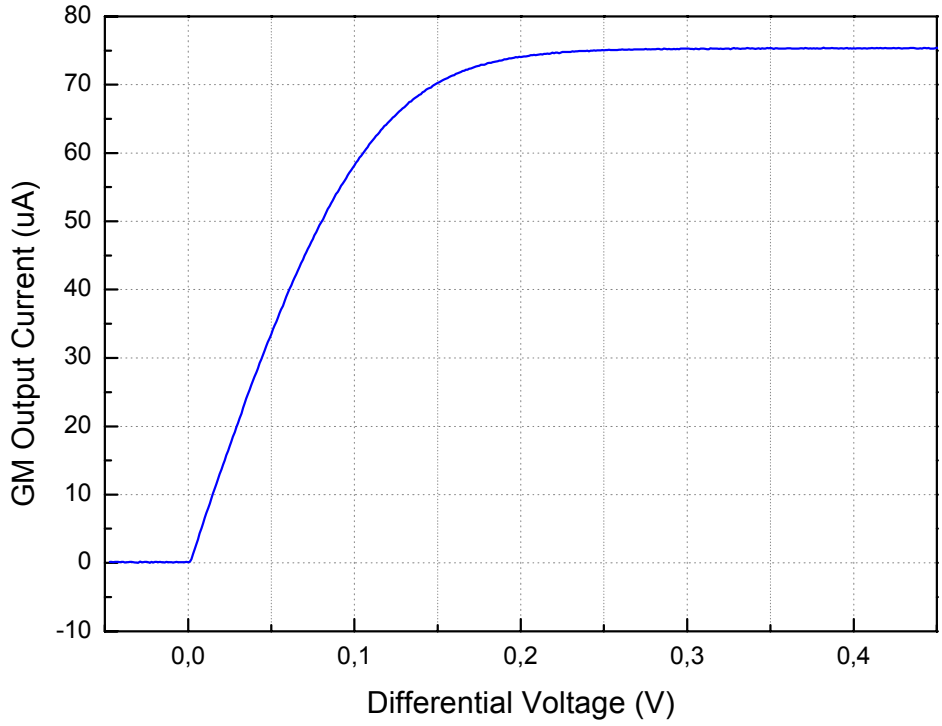


Figure 8.30: Variation of the output current of the differential transconductance amplifier in the 128 × 128 FPA with the differential input voltage measured with respect to a reference voltage at 1.65 V. The differential transconductance amplifier is biased at 74 µA and uses 3.3 V supply voltage. The circuit provides a transconductance value of 700 µA/V for a differential input voltage less than 50 mV.

Figure 8.31 shows the measured variation of the voltage gain of the differential transconductance followed by a transimpedance amplifier with 100 kΩ feedback resistance. The measured gain is 36.9 dB within 8 kHz bandwidth, corresponding to a transconductance value of 700 µA/V. Figure 8.32 shows the Measured input referred noise spectral density of the differential transconductance amplifier. The average noise spectral density in the 10 Hz – 8 kHz bandwidth is 8.3 nV/√Hz, which corresponds to 0.74 µV rms noise in the same bandwidth. The measured average noise spectral density is very close to the simulated result of 8.1 nV/√Hz.

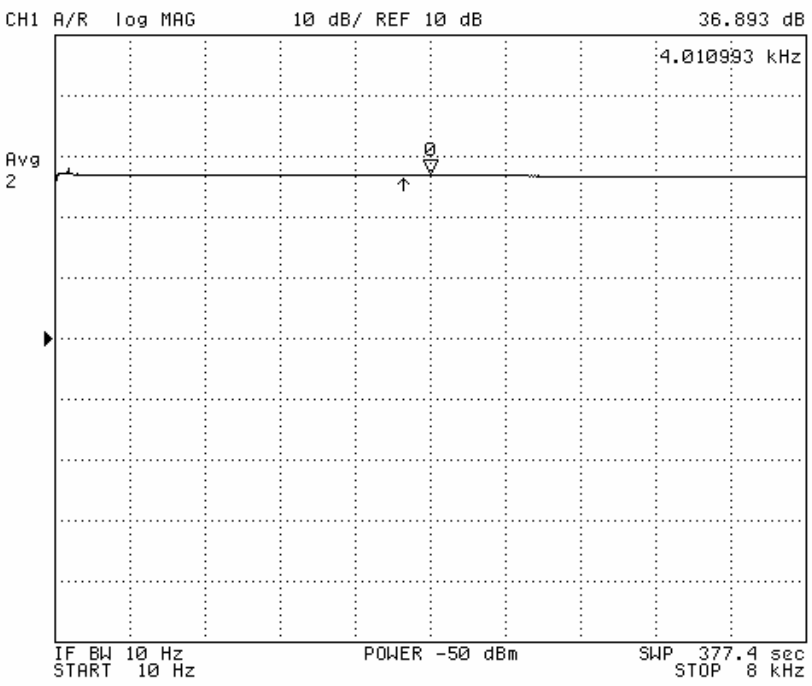


Figure 8.31: Measured variation of the voltage gain of the differential transconductance followed by a transimpedance amplifier with 100 kΩ feedback resistance. The measured gain is 36.9 dB within 8 kHz bandwidth, corresponding to a transconductance value of 700 µA/V.

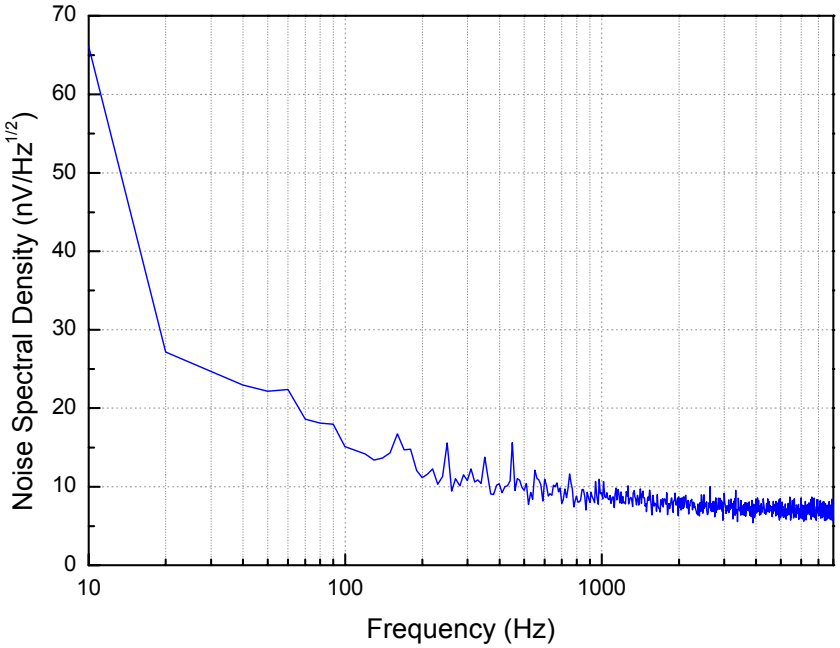


Figure 8.32: Measured input referred noise spectral density of the differential transconductance amplifier. The average noise spectral density in the 10 Hz – 8 kHz bandwidth is 8.3 nV/√Hz, which corresponds to 0.74 µV rms noise in the same bandwidth.

Figure 8.33 shows the scope view showing the CTIA amplifier output for different input current levels of 2 nA, 4 nA, 6 nA, 8 nA, and 20 nA. In this test, integration capacitance of the CTIA amplifier is set as 1.25 pF, and system clock signal is applied as 300 kHz to be able to see the integration of low current values. Figure 8.34 (a) and (b) show the measured variation of the output current of the offset current sink circuitry with respect to coarse and fine bias adjustment voltages, respectively. With the coarse bias adjustment, the circuit can cancel output offset current values starting from 0.1 µA up to 35 µA. With the fine bias adjustment, the circuit can cancel output offset current values starting from 1 nA up to 140 nA.

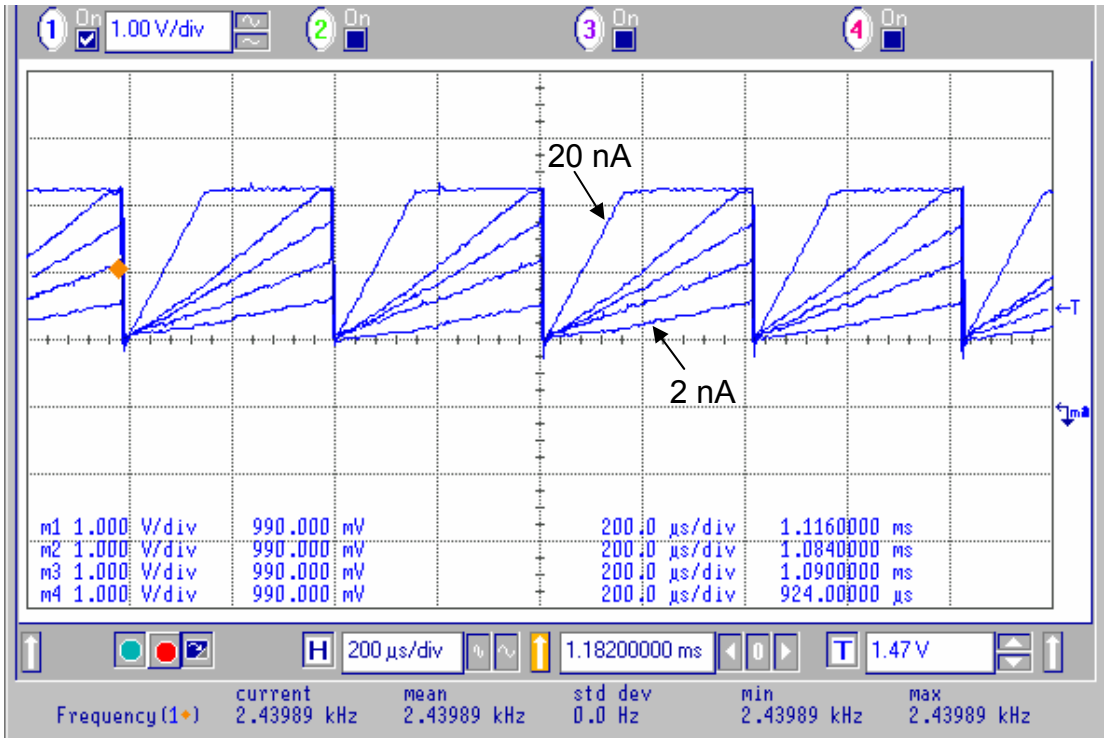
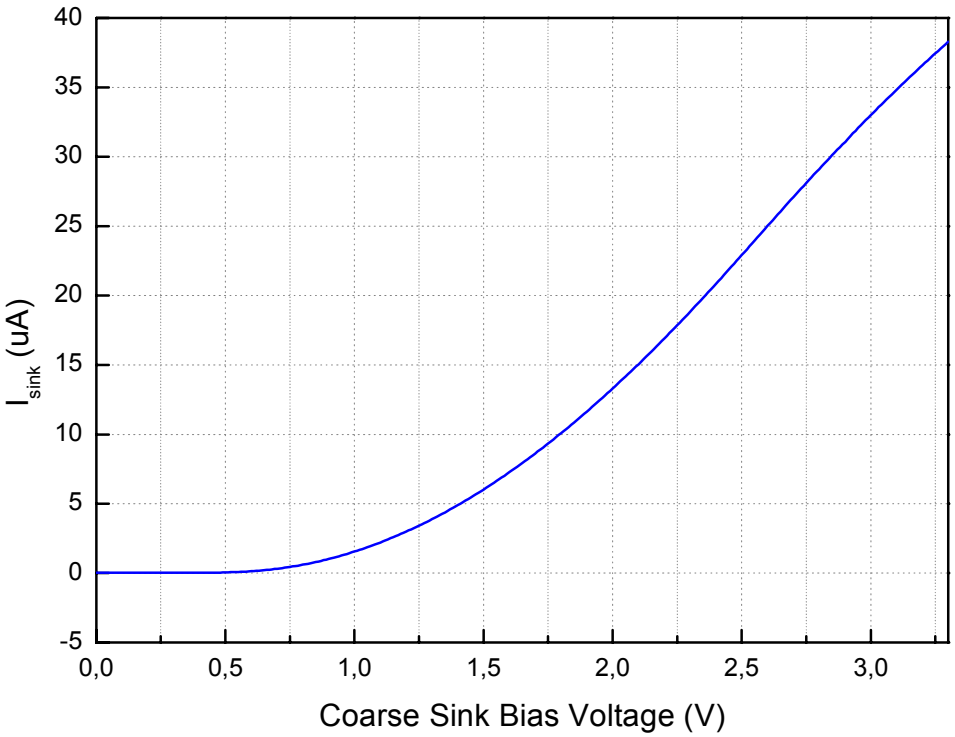
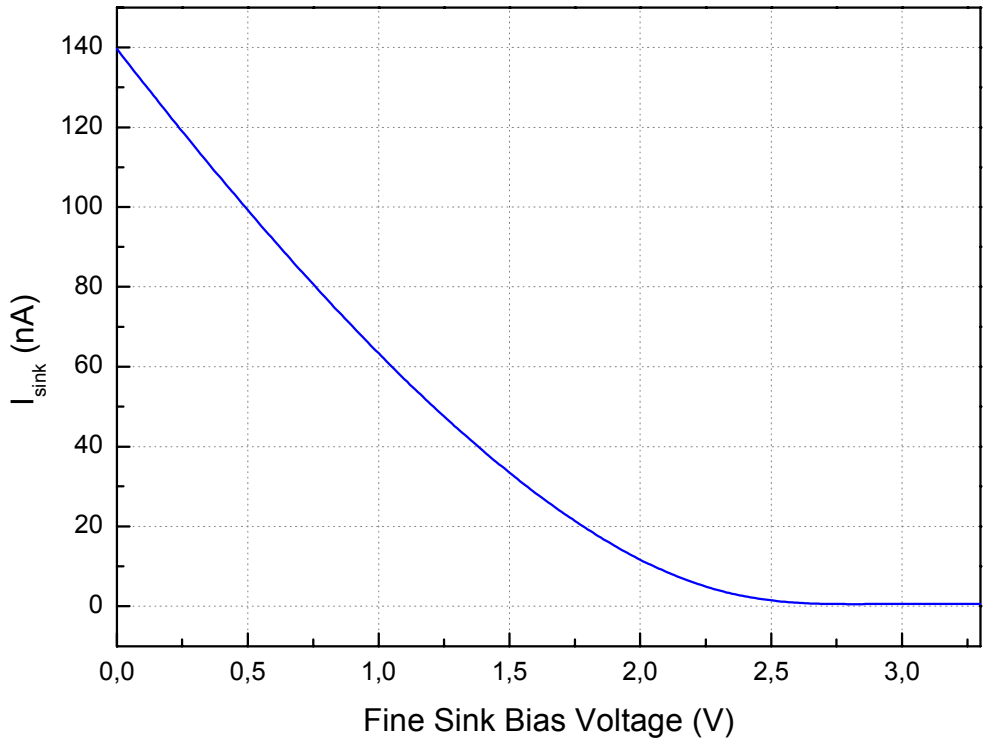


Figure 8.33: Scope view showing the CTIA amplifier output for different input current levels of 2 nA, 4 nA, 6 nA, 8 nA, and 20 nA. In this test, integration capacitance of the CTIA amplifier is set as 1.25 pF, and system clock signal is applied as 300 kHz to be able to see the integration of low current values.



(a)



(b)

Figure 8.34: Measured variation of the output current of the offset current sink circuitry with respect to bias adjustment voltages: (a) coarse adjustment from 0.1 µA up to 35 µA and (b) fine adjustment from 1 nA up to 140 nA.

Figure 8.35 shows the scope view showing the output of the capacitive transimpedance amplifier (CTIA) and sample-and-hold (S/H) circuits in the 128 × 128 FPA. The circuit is operated at a clock speed equivalent to 15 fps scanning of the 128 × 128 FPA with about 125 µs of integration time.

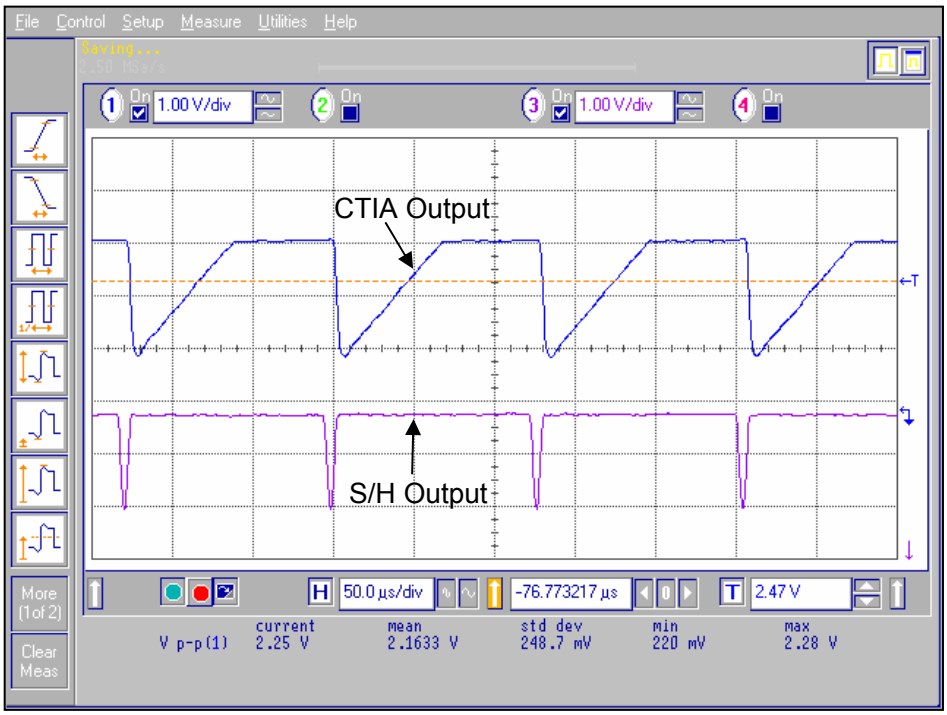
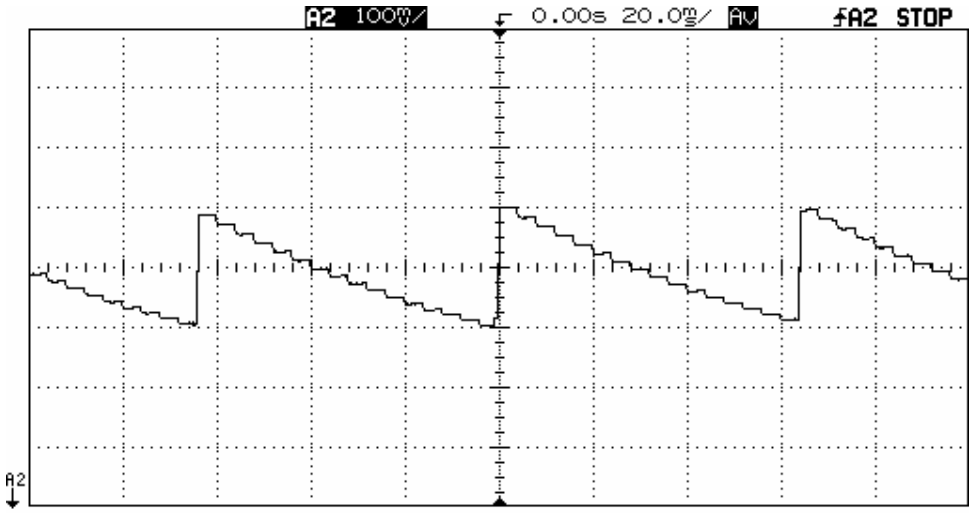


Figure 8.35: Scope view showing the output of the capacitive transimpedance amplifier (CTIA) and sample-and-hold (S/H) circuits in the 128 × 128 FPA.

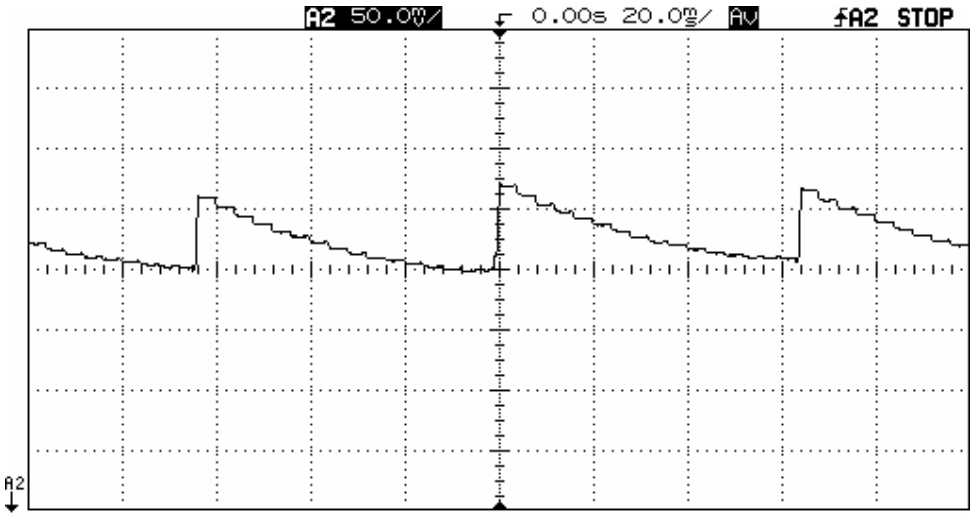
8.3.3 FPA Uniformity Test Result

Figure 8.36 (a) and (b) give the scope view showing the multiplexed array pixel outputs of the 128 × 128 FPA to the 0^{th} and 1^{st} serial outputs, respectively. Array pixels are biased at 10 µA with respect to a reference voltage of 2.0 V. To improve the signal quality, the system clock frequencyis reduced to 4 kHz. There are 16 steps in each scope view, which makes 32, equal to the number of readout channels in the 128 × 128 FPA. The decrease in the pixel voltages is more at for the pixels for the pixels at the beginning in the 0^{th} serial channel due to the fact that the horizontal voltage drop is large due to the larger integrated bias current. As the

channel number increases, current flowing along the horizontal direction decreases, resulting smaller voltage drop steps in the multiplexed output. In the design part, it has been mentioned that there is a 1 × 128 row of reference pixels integrated on top of the 128 × 128 array to compensate for the resistive voltage drops with the help of a differential readout circuit.



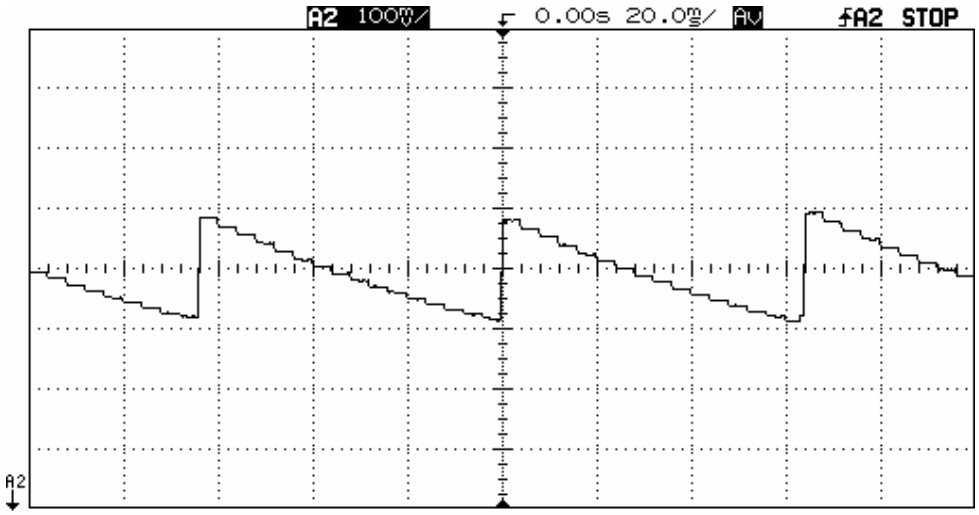
(a)



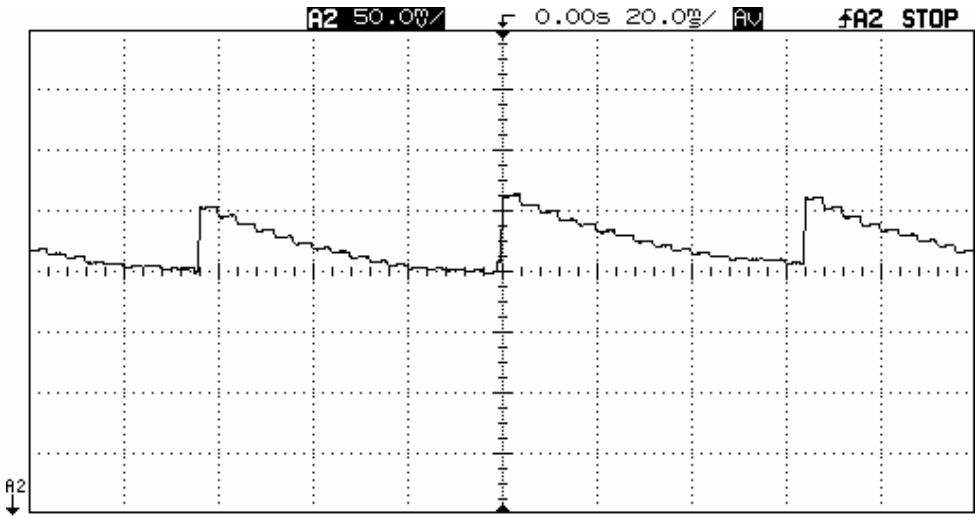
(b)

Figure 8.36: Scope view showing the multiplexed array pixel outputs of the 128 × 128 FPA to the 0^{th} (a) and 1^{st} (b) serial outputs. Array pixels are biased at 10 µA with respect to a reference voltage of 2.0 V. To improve the signal quality, the system clock frequencyis reduced to 4 kHz. There are 16 steps in each scope view, which makes 32, equal to the number of readout channels in the 128 × 128 FPA.

Figure 8.37 (a) and (b) show the scope view showing the multiplexed reference row pixel outputs of the 128 × 128 FPA to the 0th and 1stserial outputs, respectively. This scope view is almost identical to the one given for the array pixels in Figure 8.36, verifying that use of reference row can be useful in canceling the resistive voltage drops with the help of a differential readout circuit.



(a)



(b)

Figure 8.37: Scope view showing the multiplexed reference row pixel outputs of the 128 × 128 FPA to the 0th (a) and 1st (b) serial outputs. Similar to the array pixels, reference pixels are biased at 10 μA with respect to a reference voltage of 2.0 V. To improve the signal quality, the system clock frequencyis reduced to 4 kHz. There are 16 steps in each scope view, which makes 32, equal to the number of readout channels in the 128 × 128 FPA.

Figure 8.38 shows the block diagram of the computer based data acquisition system used in the measurement and recording of the array and reference pixel voltages in the CMOS fabricated 128 × 128 FPA. The FPA chip is driven using external timing signals generated by a XILINX circuit board, which also generates the required control signals for the data acquisition board in the computer.

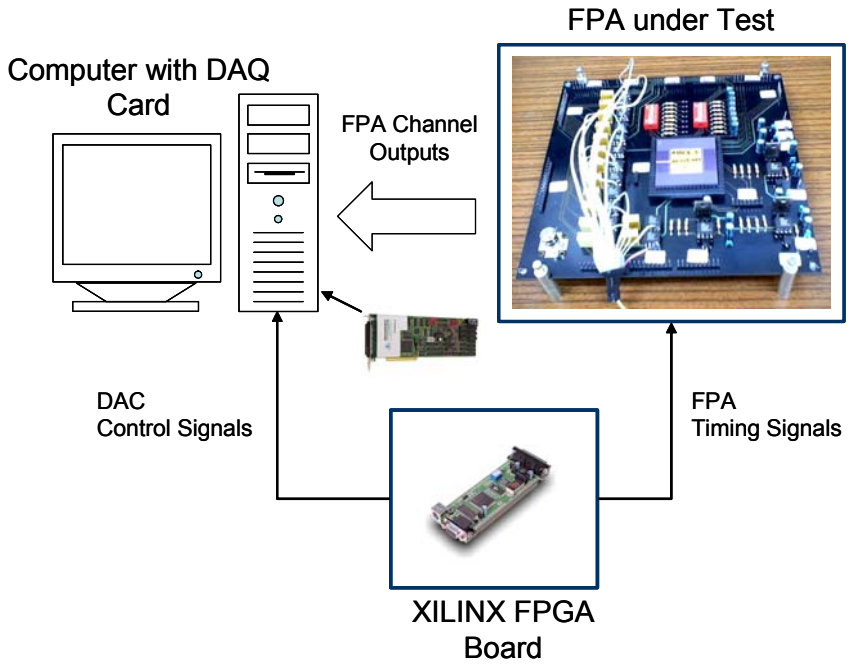
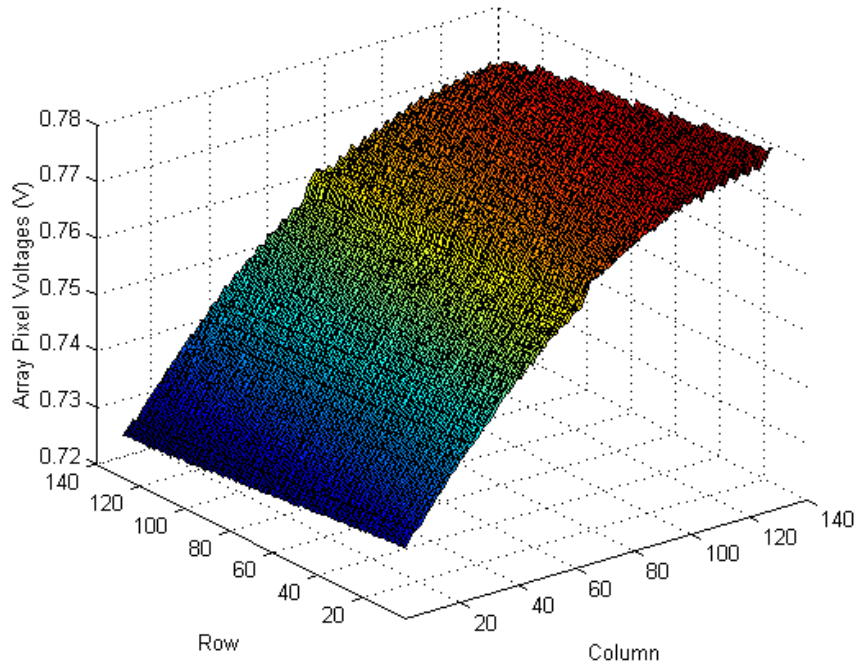
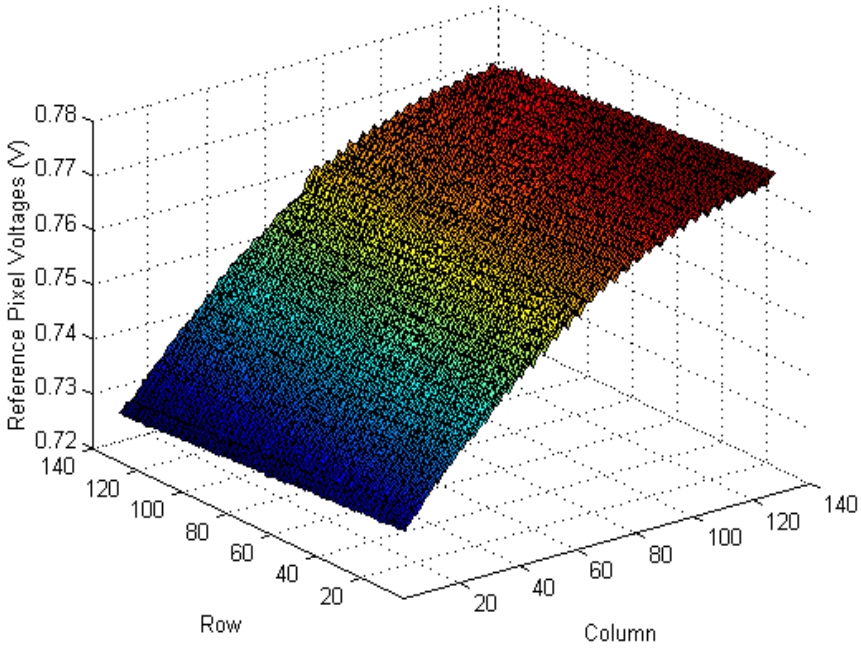


Figure 8.38: Block diagram of the computer based data acquisition system used in the measurement and recording of the array and reference pixel voltages in the CMOS fabricated 128 × 128 FPA.

Figure 8.39 (a) shows the measured voltages of the array pixels in the 128 × 128 FPA, and Figure 8.39 (b) shows the measured reference pixel voltages at each position of the row select switch [42]. In these figures, voltage variation along the rows is much higher as compared to the voltage variation along the columns. This is due to the low resistance of the routing lines outside the pixel area. This result also shows that it is very important to compensate for the effect of voltage gradient along the rows. Standard deviation (σ) of the array and reference pixel voltages are measured as 14.9 mV and 13.6 mV, respectively.



(a)



(b)

Figure 8.39: Measured detector voltages in the 128 × 128 FPA (a) array pixels and (b) reference pixel voltages at each position of the row select switch. Standard deviation (σ) of the array and reference pixel voltages are measured as 14.9 mV and 13.6 mV, respectively [42].

It should be noted that the reference pixel voltages change in the same way as the array pixel voltages, and they can be used for the compensation purposes. Standard deviation of the differential pixel voltages is reduced down to 1.5 mV, which is equivalent to a non-uniformity value of 0.2 % when calculated for the single-ended array pixel voltages. It should be noted that the proposed differential array structure with compensated routing provides about 10 times improvement in the non-uniformity compared to the uncompensated single-ended case [42].

Figure 8.40 shows the schematic of the package used in the uniformity measurement of the temperature sensitivities for the 128 × 128 FPA pixels. The FPA chip is placed on top of a thermo-electric cooler (TEC) placed in a PGA-144 package. To reduce the thermal resistance between the cold TEC plate-PGA package interface and hot TEC plate-FPA chip interface, thermal compound is deposited. The hot TEC plate, on which the FPA chip resides, is heated by applying electrical power to the TEC power pins, and the chip temperature is monitored and controlled using on-chip temperature sensors. The pixel voltages are recorded at different temperatures, from which the temperature sensitivity of each pixel in the 128 × 128 FPA is extracted.

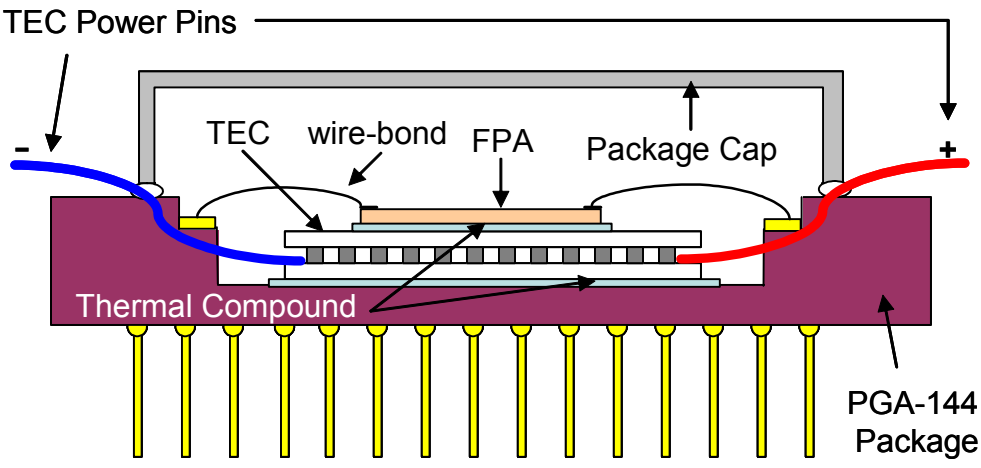


Figure 8.40: Schematic of the package used in the uniformity measurement of the temperature sensitivities for the 128 × 128 FPA pixels.

Figure 8.41 shows the measured histogram of the temperature sensitivity of the array pixels in the 128 × 128 FPA [42]. The mean value of temperature sensitivity is measured as -2.05 mV/K for both array and reference pixels. Standard deviation is calculated as 61 μV/K with a non-uniformity value of 2.96 %. Mean value of the temperature sensitivity of the differential voltage between the array and reference pixels is measured as 2.3 μV/K, which shows that differential readout structure can compensate for the variations in the ambient temperature, eliminating the need for high precision temperature stabilization.

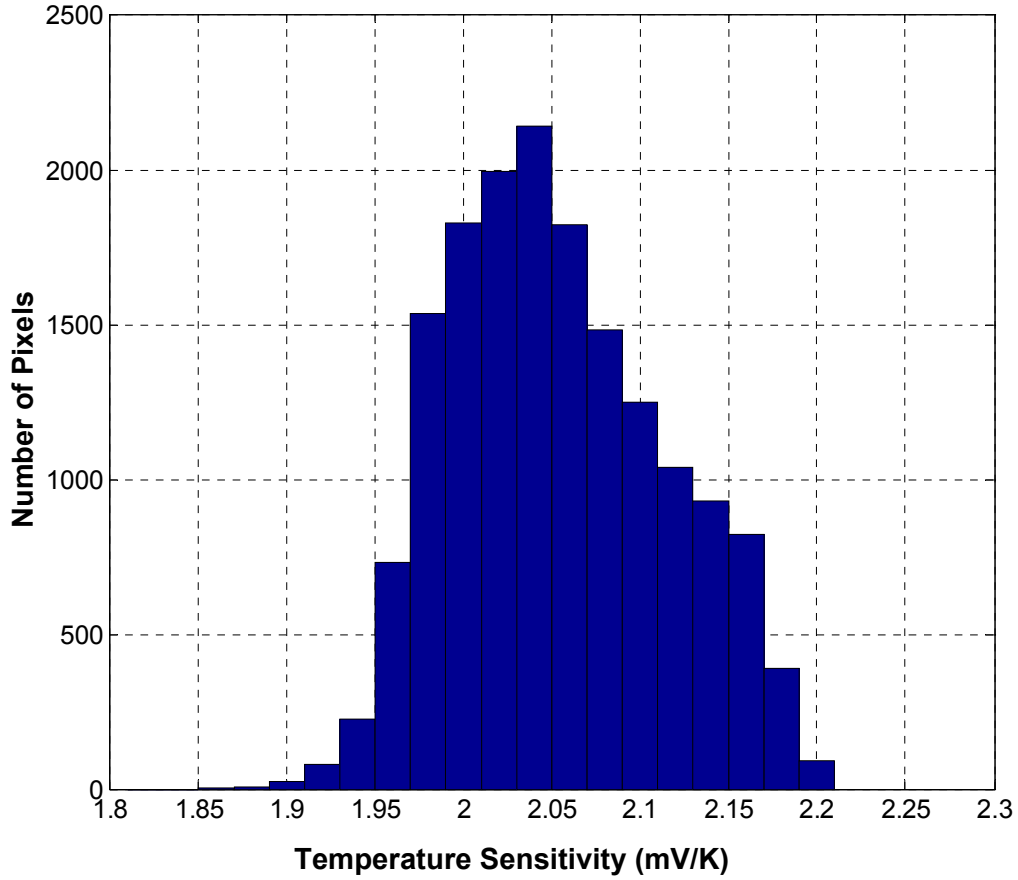


Figure 8.41: Measured histogram of the temperature sensitivity of the array pixels in the 128 × 128 FPA. Mean value is -2.05 mV/K, and the standard deviation is 61 μV/K with a non-uniformity of 2.96 % [42].

8.4 Effect of Post-CMOS Processing on FPA Uniformity

An important source of the non-uniformity in the uncooled FPAs is the variation of the pixel thermal conductance value. Thermal conductance values of the FPA pixels may decrease due to the reduction in the interconnect cross-section owing to over-etching in some pixels, or the thermal conductance of the pixels may increase due to the metal residues left on the interconnects. Another source of the non-uniformity is the variation of the oxide thickness over the FPA; however, due to the mature CMOS process the effect of this is expected to be less than the non-uniformity induced by the variations in the pixel thermal conductance values. These two sources together with the variations in the temperature sensitivity of the array pixels modulate the responsivity of the array pixels, and in the literature it has been reported that the non-uniformity of the responsivity value for a 320 × 240 SOI diode FPA is better than 1.5 % [28]. It should be mentioned that the SOI diodes are implemented using an in-house SOI process on 8-inch wafers, and the pixels are released from the substrate using a dry-etch method. On the other hand, p^+-active/n-well diode FPA is fabricated in a standard CMOS process, and the pixels are released from the substrate using a dry-etch step followed by a wet-etch step. Therefore, it is expected that the non-uniformity in the array pixels will be slightly higher as compared to that of the SOI diodes, mainly due to the difficulties encountered in wet-etch steps. The non-uniformity measurement of the p^+-active/n-well diode FPA could not be performed due to the problems in the post-processing steps performed using dies fabricated in multi-project wafer runs [81, 82], which prevented fabrication of fully functional suspended FPAs. Currently, the optimization of the post-CMOS fabrication steps is under development.

The problems associated in die level post-processing can mostly be overcome when a wafer level fabrication is used, where the yield will improve considerably. The next section presents the yield calculation results of the p^+-active/n-well diode FPAs assuming that they are fabricated wafer level on 6-inch wafers using a standard CMOS process.

8.5 Expected Yield for Wafer Level Fabrication

The yield calculation of the p^+-active/n-well diode FPAs is performed for a standard CMOS fabrication using 6-inch wafers for FPAs with 64 × 64, 128 × 128, and 320 × 240 array formats. The number of dies that can be fabricated on a 6-inch wafer for the fabricated 64 × 64 and 128 × 128 FPAs, and a possible 320 × 240 FPA are 570, 260, and 70, respectively. It is assumed that the yield of the CMOS fabricated chips is 99 % for the 64 × 64 FPA, and yield values (Y) for the other FPAs are calculated by scaling this assumed yield according to the silicon chip areas using an exponential yield formula given as [83]

$$Y = e^{-D_0 A} \tag{8.1}$$

where, D_0 is the defect density, and A is the chip area. The 64 × 64 FPA measures 22 mm^2, 128 × 128 FPA measures 52 mm^2, and a possible 320 × 240 FPA measures 170 mm^2. Corresponding CMOS fabrication yields for the 128 × 128 and 320 × 240 FPAs are calculated as 74 % and 22 %, respectively. The yield of the post-processing steps is assumed to be 90 % for all the p^+-active/n-well diode FPAs. CMOS fabrication cost is assumed to be 1000 U.S. dollars ($) per wafer. The cost of the post-CMOS processing steps for the p^+-active/n-well diode FPAs is assumed to be 50 U.S. dollars per wafer. The costs of the different FPAs can be compared by a common figure of merit equal to the FPA cost in U.S. cent (¢) for a given NETD value (in Kelvin) per 1000 pixels. In the calculation, targeted NETD value of 350 mK is used for the 64 × 64 and 128 × 128 FPAs, and a projected value for the 320 × 240 FPA is used. Table 8.1 gives the comparison of the expected yield and cost of the p^+-active/n-well FPAs developed at METU with different arrays in the literature [23]. The vacuum packaging cost is assumed to be 50, 75, and 100 U.S. dollars for the 64 × 64, 128 × 128 (160 × 128), and 320 × 240 (320 × 256) FPAs, respectively. The FPA cost increases rapidly with increased array formats due to the decreased yield with the increased CMOS chip size. For example, it may be advantageous to use a 128 × 128 FPA instead of a 320 × 240 FPA in some applications limited by size, weight, and cost [23]. Based on the above yield and cost calculations, it seems that p^+-active/n-well diode FPAs provides better figure of

merits as compared to the state of the art detectors at much lower overall detector cost, making them ideal solutions for low-cost infrared imaging applications.

Table 8.1: Comparison of the expected yield and cost of the p^+-active/n-well FPAs developed at METU with different uncooled arrays in the literature [23].

	METU			**INDIGO** [23]	
FPA Format	64×64	128×128	320×240*	160×128	320 ×256
Dies / Wafer (6-inch wafer)	570	260	70	76	30
Yield (%)	90	67	20	73	16
NETD (K) f/1 optics	0.35**	0.35**	0.5**	0.025	0.035
Unpackaged FPA Cost (U.S. $)	2	6	75	280***	3000***
Normalized Unpackaged FPA Cost (¢ × K / 1000 Pixels)	17	13	49	34	128
Vacuum Packaged FPA Cost (U.S. $)	52	81	175	355	3100

Uncooled detectors need vacuum packaging for improved performance. If the vacuum packaging is performed on die level, the overall detector cost is increased due to relatively higher cost of the hermetic metal or ceramic packages as compared to the CMOS chip cost [84]. Wafer-level vacuum packaging can be used to decrease the overall detector cost considerably [84], especially when the chip cost low. Furthermore, the cost of the detector can be reduced down to the CMOS chip cost, when the etching yield is improved, since the post-processing cost can be neglected.

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* Not fabricated.

** Targeted NETD value

*** Currently, there are 320 × 240 FPAs that are sold at about 3000 U.S. dollars. The cost of the 160 × 128 FPA is calculated using the improved yield with decreased chip size.

8.6 Conclusions

In this chapter, the electrical test results of the fabricated 64 × 64 and 128 × 128 FPAs have been presented. The measurement and test results verify that the on-chip digital circuitry generates the FPA address signals and timing signals for the analog readout circuitry properly as designed. Furthermore, it has been verified that the designed differential transconductance amplifier provides low noise suitable for the readout of the p^+-active/n-well diode microbolometers. The preamplifier noise is measured as 0.48 μV in a 4 kHz bandwidth for the 64 × 64 FPA, and as 0.74 μV in an 8 kHz bandwidth for the 128 × 128 FPA. These results correspond to expected NETD values of 0.8 K and 1 K for the 64 × 64 and 128 × 128 FPAs using f/1 optics, respectively. These NETD values can be decreased below 350 mK with further optimization of the readout circuit and post-CMOS etching steps for improved responsivity. Due to the problems faced in the post-processing steps, the uniformity measurements have been carried out on the CMOS fabricated unsuspended FPAs. The uniformity measurement of the pixel voltages in the 64 × 64 FPAs verify that the FPA routing resistances causes large fixed pattern noise in the FPA pixel voltages. The uncorrected non-uniformity of the array pixel voltages is measured as 0.82 %, and it has been theoretically shown that the fixed pattern noise can be compensated such that the non-uniformity value improves down to 0.05 %. In the 128 × 128 there is a reference row identical to the rows in the array, which is used to compensate for the fixed pattern noise and effect of operating temperature with the help of a differential readout circuitry. It has been verified that the standard deviation is reduced from 15 mV down to 1.5 mV when the FPA pixel voltages are read out differentially with respect to reference row pixels in the 128 × 128 FPA, providing 10 times improvement. The uniformity of the pixel temperature sensitivities of the 128 × 128 FPA is measured to be -2.0 mV/K, with a non-uniformity better than 3 %, which is good due to the mature CMOS fabrication technology. Using a differential readout and identical reference pixels, the mean of the temperature sensitivity of the differential FPA voltage is measured as 2.3 μV/K, relaxing the requirements for temperature stabilization.

CHAPTER IX

9 CONCLUSIONS AND FUTURE WORK

The research presented in this dissertation involves the development of a new low-cost uncooled microbolometer FPA together with monolithic readout circuitry implemented using a standard CMOS process. The FPAs are based on the p^+-active/n-well diode microbolometer detector that can be implemented in any standard n-well CMOS process without the need for any material deposition or critical lithography steps. Within the framework of this thesis, two low-cost FPAs with 64 × 64 and 128 × 128 array formats have been designed and fabricated together with their on-chip readout circuitry specially developed for the n-well diode type microbolometers.

Based on the achievements and results of this study, following conclusions can be drawn:

1. The limitations of the previously developed resistive n-well microbolometer detector are investigated. The detector size of the resistive n-well microbolometer detectors is relatively large, making fabrication of low-cost large format FPAs difficult. Although single pixel performance of the resistive n-well microbolometers is much better as compared to other CMOS compatible uncooled detectors, there is a reduction in its responsivity due to the built-in diodes incorporated in each pixel to simplify the array scanning.

Furthermore, when the size of the n-well resistive microbolometer is decreased using advanced post-processing steps, the pixel performance decreases due to the reduction in the effective pixel TCR value. To compensate for the performance reduction, higher detector bias can be used at the expense of increased self-heating.

2. A new uncooled microbolometer detector structure has been proposed, which is based on the p^+-active/n-well diode that can be implemented using a standard CMOS process. The optimum detector size and pixel biasing conditions have been analyzed using MATLAB simulations. The optimum pixel size is determined as 40 μm × 40 μm. Below 40 μm pixel pitch, the detector area becomes so small that the NETD becomes unacceptably high. Above 40 μm pixel pitch, the detector becomes so large that the improvement in thermal isolation is cancelled by the increase in the time constant. Furthermore, the use of longer support arms in the lager pixels requires using longer polysilicon interconnects, which decreases the responsivity and results additional noise.

3. The p^+-active/n-well diode microbolometers have been fabricated using a standard 0.35 μm CMOS process followed by simple post-CMOS bulk micromachining that does not require any critical lithography or complicated deposition steps making fabrication of very low-cost uncooled detector arrays possible. The post-CMOS fabrication steps include an RIE etching to reach the bulk silicon and an anisotropic silicon etching to obtain thermally isolated pixels. During the RIE etching, CMOS metal layers are used as masking layers, and therefore, narrow openings can be defined between the support arms. The post-processing steps of the CMOS fabricated detectors have been investigated in detail within another study. This approach allows achieving small pixel size of 40 μm × 40 μm with a fill factor of 44 %.

4. Several electrical and optical measurements have been performed for the fabricated p^+- active/n-well diode microbolometer detectors. The dependence of the sensitivity on detector bias has been simulated together with the

associated detector noise. The optimum detector bias level has been found as 20 μA at which the temperature sensitivity has been measured as -2 mV/K.

It is observed that the detector noise is dominated by the noise coming from the polysilicon interconnects used to improve the detectivity of the pixels. The flicker noise of the detector is found to be low which is due to its low value at low current bias levels. The detector noise voltage has been measured as 0.52 μV and 0.69 μV for a 4 kHz and 8 kHz bandwidths, respectively. The corner frequency of the detector noise voltage is measured as 90 Hz, which is an order of magnitude smaller than that of the commonly used microbolometer detectors mainly due to the single crystal nature of the silicon n-well diode and low value of 1/*f* noise at low bias levels.

5. The thermal conductance value of the fabricated diode microbolometers has been measured based on the self-heating effect. The thermal conductance of the detector is measured as 1.8×10^{-7} W/K under continuous bias at 50 mTorr vacuum level. The responsivity and spectral absorption of the diode type microbolometer are tested using an electro-optical test setup. The responsivity of the n-well diode microbolometer detector is measured at different infrared modulation frequencies, from which the DC responsivity is extracted as 4970 V/W with a thermal time constant of 36 ms. The measured detectivity (D^*) is of 9.7×10^8 cm√Hz/W. These performance values are sufficiently good to form many low-cost infrared imaging applications.

6. Within the framework of this thesis, two low-cost FPAs with 64 × 64 and 128 × 128 array formats have been designed and fabricated together with their on-chip readout circuitry specially developed for the n-well diode type detectors. The FPAs are fabricated using a standard 0.35 μm CMOS process followed by simple post-CMOS bulk micromachining that does not require any critical lithography or complicated deposition steps. The 64 × 64 FPA chip has 4096 n-well diode microbolometer pixels scanned at 30 fps by an integrated low-noise 16-channel parallel readout circuit, and it measures 4.1 mm × 5.4 mm in a 0.35 μm CMOS process. The 128 × 128 FPA chip has

16384 n-well diode microbolometer pixels scanned at 30 fps by an integrated 32-channel parallel readout circuit, and it measures 6.6 mm × 7.9 mm in the same process. The designed multi-channel parallel readout circuits include low-noise differential preamplifiers, switched capacitor integrators, sample-and-hold circuits, and various other circuit blocks for reducing the effects of variations in detector voltage and operating temperature.

For the n-well diode type microbolometers a new preamplifier circuit is designed, that combines GMI and CCBDI circuits with CTIA amplifier. The constant current biasing of the GMI and CCBDI circuit is used to bias the n-well diode microbolometers. Since there is a single diode in the pixel, the SNR of the pixel is lower as compared to SOI diodes, therefore, it is necessary to minimize the input referred noise of the preamplifier. Different than the CCBI structure, the preamplifier is taken out of the pixels and placed outside the FPA, where the device sizes can be increased to provide lower input noise. In addition, true differential operation is performed using identical and optically shielded reference pixels. The use of differential circuit cancels the effects of process variations and fluctuations in the operating temperature, relaxing the requirements for the temperature stabilizers. Finally, the residual offsets are canceled by an analog on-chip offset removal circuit prior to integration. The required integration for bandwidth limitation is performed using CTIA circuit, which has zero input impedance, and provides stable operating point for the output stage of the transconductance amplifier minimizing the transients during scanning. Unlike other simple capacitor integrators of GMI and CCBDI, longer integration periods can be used possibly with a set of digitally controlled capacitors with relatively smaller unit capacitances reducing the implementation area.

7. The functionality of the designed FPA readout circuits have been verified by detailed electrical tests. First, the noise and transconductance of the differential transconductance amplifier are measured using a custom prepared circuit boards and using in-house packaged CMOS dies. The measured

transconductance values for the preamplifiers for the 64 × 64 and 128 × 128 FPAs are 1000 μA/V and 700 μA/V respectively, which are very close to their designed values. The designed preamplifier circuit for the 64 × 64 n-well diode FPA has a measured input referred noise of 0.48 μV for a 4 kHz bandwidth at 30 fps providing an expected NETD value of 0.8 K for an f/1 optics. The preamplifier circuit for the 128 × 128 n-well diode FPA has a measured input referred noise of 0.76 μV for an 8 kHz bandwidth at 30fps providing an expected NETD value of 1 K for an f/1 optics. Both readout circuits achieved input referred noise levels much lower than the previously designed preamplifiers. These NETD values can be decreased below 350 mK by decreasing the electrical bandwidth with the help of increased number of parallel readout channels and by optimizing the post-CMOS etching steps.

8. The uniformity of the fabricated FPAs is very good due to the mature CMOS fabrication technology. The measured uncorrected differential voltage non-uniformity for the 128 × 128 array pixels after the CMOS fabrication is 0.2 % with a standard deviation of only 1.5 mV, which is low due to the improved array structure that can compensate for the voltage drops along the routing resistances in the array. Non-uniformity of temperature sensitivity of the array pixels is measured to be less than 3 % with a mean and standard deviation of -2.05 mV/K and 61 μV/K, respectively. The temperature sensitivity of the differential pixel voltages has a measured mean value of 2.3 μV/K. The use of differential readout with respect to identical reference pixels relaxes the requirements on the temperature stabilization resulting lower cost and lower power dissipation. Table 9.1 gives the performance parameter summary for the CMOS fabricated FPAs.

Table 9.1: Performance parameter summary for the CMOS fabricated FPAs.

Process	AMS 0.35 μm CMOS 3M2P	
Detector	Diode	
Pixel Size	40 μm × 40 μm	
Fill Factor	44 %	
Detector Responsivity	4970 V/W	
Detector Noise	0.51 μV rms (4 kHz BW)	0.69 μV rms (8 kHz BW)
Array Format	**64 × 64** array pixels **1 × 16** reference pixels	**128 × 128** array pixels **1 × 128** reference pixels
On-Chip ROC	• 16-column parallel architecture • 4 kHz BW @ 30 fps • Differential readout • Less sensitive to ambient temp • On-chip timing • Variable gain • Variable integration time • 16 Parallel + 1 serial outputs	• 32-column parallel architecture • 8 kHz BW @ 30 fps • Differential readout • Less sensitive to ambient temp • Reduced fixed pattern noise • On-chip sensors • On-chip / external timing • Variable gain • Variable integration time • 32 Parallel + 2 serial outputs
Power Dissipation	25 mW	25 mW (minimized circuitry)
FPA Responsivity	5mV/Kscene->95mV/Kscene	2 mV/Kscene-> 35 mV/Kscene
ROIC Input Noise	0.48 μV rms	0.76 μV rms
FPA NETD	0.8 K	1 K

Although all of the major research objectives have been achieved within this research, there are various points that need further study. These points are related with the readout circuitry and device fabrication, which are explained as follows:

1. The 128 × 128 FPA has been designed to improve the non-uniformity; however, bias adjustment is still required in order to avid saturation in the integrator circuits. Bias adjustment can be implemented externally or internally using parallel working digital-to-analog (D/A) converters. In order to be able to apply bias voltages with better than 0.5 mV precision, a 14-bit resolution is required for a D/A with 5 V output swing. Since there are more than one readout channel in large FPAs, large number of D/As will be needed with increased power consumption, increased circuit complexity, and possible external noise coupling at the sensitive bias nodes. Since there will be large offset variation between the external A/Ds, overall FPA calibration will also be difficult. On the other hand, the bias adjustment can be performed at the same quality with lower resolution D/As when they are integrated as part of the on-chip readout circuitry. In fact, simpler architectures with reduced circuit complexity and improved device matching can be used for each readout channels. Since the devices will be implemented in chip level, the problem of matching and noise coupling can be minimized considerably.

   Based on the similar arguments, on-chip analog-to-digital data converters can also be integrated. However, this is not as critical as the D/As, since there are sufficiently fast and high resolution A/Ds developed for the video applications. On the other hand, it is desired to provide complete infrared imaging systems on a single chip with minimum number of external components; therefore, there are efforts to integrate the A/Ds monolithically within the FPA. On-chip A/Ds can be implemented in parallel form in each readout channel with a moderate speed and high resolution at the expense of increased silicon area and power consumption, or a single high speed A/D with moderate resolution can be used for the multiplexed analog FPA output.

There are very simple A/D architectures that can be used in the column level, and such a design is under development.

2. For CMOS fabrication, multi-project-wafer (MPW) production services are used provided by chip brokers such a Europractice [81] and CMP [82], where a single silicon wafer is shared by different designs, and the users receive their designs only packaged or unpackaged in die form. Since the post-processing of the samples in die level is very difficult as compared to wafer level processing, the fabrication yield of the n-well FPAs drops considerably making it very difficult to achieve fully functional thermally suspended FPAs. Up to know, the main problem was the protection of the metal bonding pads during the dry etch. Defects on manually deposited protective layers are destroyed first during RIE and then during following wet etch processes that include a short hydrofluoric acid (HF) and long TMAH etching steps. At the end of TMAH etching, it is possible that some of the bonding pads are destroyed so that electrical connection is not possible to those pads. Therefore, it is necessary to work in wafer level where all kind of deposition and etching steps are much simpler using conventional fabrication techniques. Furthermore, it is also possible to use wafer level vacuum packaging in when wafer level FPA fabrication is used. Figure 9.1 shows the schematic of the wafer level vacuum packaging. An IR transparent cap is placed and patterned on top of the FPA. The cap and FPA wafer is sealed in vacuum and diced later.

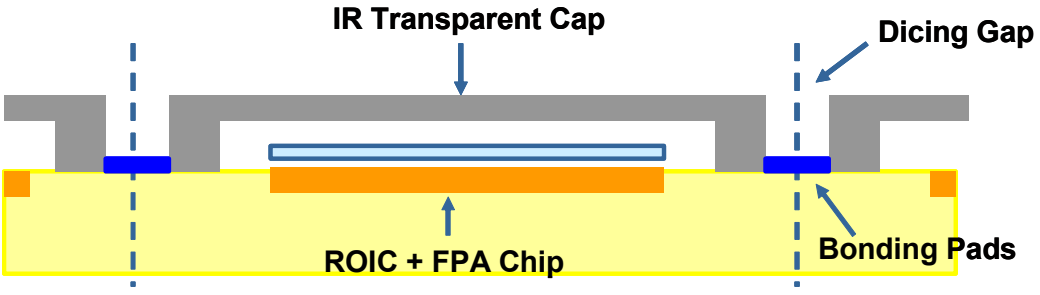

Figure 9.1: Schematic of the wafer level vacuum packaging. An IR transparent cap is placed and patterned on top of the FPA. The cap and FPA wafer is sealed in vacuum and diced later.

To conclude, the major achievement of this research is the development of low-cost uncooled infrared FPAs with integrated readout circuitry that can be fabricated using standard CMOS and MEMS technologies. Considering the performance of the fabricated FPAs and the involved fabrication steps, the proposed method is very cost-effective to fabricate large format focal plane arrays for low-cost infrared imaging applications. It is hoped that, the result of this research will enable the use of infrared imaging for many other commercial applications which is currently not possible due to the high system costs of the current infrared imaging systems.

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The publication list of the author is given below:

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