CMOS READOUT ELECTRONICS FOR MICROBOLOMETER TYPE INFRARED DETECTOR ARRAYS

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submitted by **ALPEREN TOPRAK** in partial fulfillment of the requirements for the degree of **Master of Science in Electrical and Electronics Engineering Department, Middle East Technical University** by,

Prof. Dr. Canan Özgen _____
Dean, Graduate School of **Natural and Applied Sciences**

Prof. Dr. İsmet Erkmen _____
Head of Department, **Electrical and Electronics Engineering**

Prof. Dr. Tayfun Akın _____
Supervisor, **Electrical and Electronics Eng. Dept., METU**

Examining Committee Members:

Prof. Dr. Murat Aşkar _____
Electrical and Electronics Engineering Dept., METU

Prof. Dr. Tayfun Akın _____
Electrical and Electronics Engineering Dept., METU

Prof. Dr. Cengiz Beşikçi _____
Electrical and Electronics Engineering Dept., METU

Assoc. Prof. Dr. Haluk Külah _____
Electrical and Electronics Engineering Dept., METU

Dr. Selim Eminoğlu _____
Micro and Nanotechnology Program, METU

Date: **13.02.2009**

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ABSTRACT

CMOS READOUT ELECTRONICS FOR MICROBOLOMETER TYPE INFRARED DETECTOR ARRAYS

Toprak, Alperen

M.Sc., Department of Electrical and Electronics Engineering

Supervisor: Prof. Dr. Tayfun Akın

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This thesis presents the development of CMOS readout electronics for microbolometer type infrared detector arrays. A low power output buffering architecture and a new bias correction digital-to-analog converter (DAC) structure for resistive microbolometer readouts is developed; and a 384x288 resistive microbolometer FPA readout for 35 µm pixel pitch is designed and fabricated in a standard 0.6 µm CMOS process. A 4-layer PCB is also prepared in order to form an imaging system together with the FPA after detector fabrication.

The low power output buffering architecture employs a new buffering scheme that reduces the capacitive load and hence, the power dissipation of the readout channels. Furthermore, a special type operational amplifier with digitally controllable output current capability is designed in order to use the power more efficiently. With the combination of these two methods, the power dissipation of the output buffering structure of a 384x288 microbolometer FPA with 35 µm pixel pitch operating at 50 fps with two output channels can be decreased to 8.96% of its initial value.

The new bias correction DAC structure is designed to overcome the power dissipation and noise problems of the previous designs at METU. The structure is composed of two resistive ladder DAC stages, which are capable of providing multiple outputs. This feature of the resistive ladders reduces the overall area and power dissipation of the structure and enables the implementation of a dedicated DAC for each readout channel. As a result, the need for the sampling operation required in the previous designs is eliminated. Elimination of sampling prevents the concentration of the noise into the baseband, and therefore, allows most of the noise to be filtered out by integration.

A 384x288 resistive microbolometer FPA readout with 35 µm pixel pitch is designed and fabricated in a standard 0.6 µm CMOS process. The fabricated chip occupies an area of 17.84 mm x 16.23 mm, and needs 32 pads for normal operation. The readout employs the low power output buffering architecture and the new bias correction DAC structure; therefore, it has significantly low power dissipation when compared to the previous designs at METU. A 4-layer imaging PCB is also designed for the FPA, and initial tests are performed with the same PCB. Results of the performed tests verify the proper operation of the readout. The rms output noise of the imaging system and the power dissipation of the readout when operating at a speed of 50 fps is measured as 1.76 mV and 236.9 mW, respectively.

Key words: Readout circuits for large format microbolometer arrays, low power readout circuits for microbolometers, uncooled infrared focal plane arrays.

ÖZ

MİKROBOLOMETRE TİPİ KIZILÖTESİ DETEKTÖR DİZİNLERİ İÇİN CMOS OKUMA ELEKTRONİĞİ

Toprak, Alperen

Yüksek Lisans, Elektrik ve Elektronik Mühendisliği Bölümü

Tez Yöneticisi: Prof. Dr. Tayfun Akın

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Bu tezde mikrobolometre tipi kızılötesi detektör dizinleri için CMOS okuma devresi geliştirilmesi sunulmuştur. Direnç tipi mikrobolometreler için düşük güç tüketimli bir çıkış tamponlama mimarisi ve yeni bir eğilimleme düzeltme sayısal – analog çevirici (SAÇ) yapısı geliştirilmiş; ve 35 µm pixel boyutuna sahip bir 384x288 direnç tipi mikrobolometre odak düzlem matrisi için standart 0.6 µm CMOS teknolojisinde okuma devresi tasarlanmış ve ürettirilmiştir. Detektör üretiminden sonra odak düzlem matrisi ile beraber bir görüntüleme sistemi oluşturmak üzere 4 katlı bir baskılı devre levhası da hazırlanmıştır.

Düşük güç tüketimli çıkış tamponlama mimarisi okuma kanallarının kapasitif yükünü ve bu sayede güç tüketimini azaltan yeni bir tamponlama şeması kullanmaktadır. Buna ek olarak, gücü daha verimli kullanmak amacıyla çıkış akım kapasitesi sayısal olarak kontrol edilebilen özel bir işlevsel yükseltici tasarlanmıştır. Bu iki metodun birleşimiyle, saniyede 50 kare gösteren 35 µm piksel boyutuna ve iki çıkış kanalına sahip bir 384x288 odak düzlem dizininin çıkış tamponlama yapısının güç tüketimi ilk değerinin %8.96'sına düşürülebilmektedir.

Yeni eğilimleme düzeltme SAÇ yapısı, daha önce ODTÜ'de tasarlanmış yapıların gürültü ve güç tüketimi sorunlarının üstesinden gelmek için tasarlanmıştır. Bu yapı, iki adet çoklu çıkış verebilen direnç merdiveni tipi SAÇ aşamasından oluşmaktadır. Direnç merdiveni tipi SAÇ'ların bu özelliği yapının toplam alanını ve güç tüketimini düşürmekte ve her okuma kanalına tahsis edilmiş ayrı bir SAÇ yapılmasına olanak tanımaktadır. Bunun sonucunda, daha önceki tasarımlarda gerekli olan örnekleme işlemine olan ihtiyaç ortadan kaldırılmıştır. Örneklemenin ortadan kaldırılması, gürültünün düşük frekans bandında yoğunlaşmasını önlemekte; dolayısıyla, gürültünün büyük kısmının integrasyon işlemiyle süzülmesine imkan vermektedir.

35 µm piksel boyutuna sahip bir 384x288 odak düzlem dizini okuma devresi standart bir 0.6 µm CMOS teknolojisinde tasarlanmış ve ürettirilmiştir. Üretilen yonga 17.84mm x 16.23 mm boyutunda olup normal çalışma için 32 bağlantıya ihtiyaç duymaktadır. Bu okuma devresi, düşük güç tüketimli çıkış tamponlama mimarisini ve yeni eğilimleme düzeltme SAÇ yapısını kullanmaktadır; dolayısıyla, ODTÜ'deki eski tasarımlarla karşılaştırıldığında kayda değer şekilde düşük güç tüketimine sahiptir. Bu odak düzlem dizini için bir görüntü baskılı devre levhası da tasarlanmış ve ilk testler aynı baskılı devre levhasında yapılmıştır. Yapılan testlerin sonuçları okuma devresinin doğru çalıştığını göstermektedir. Görüntü sisteminin çıkış gürültüsünün etkin değeri ve okuma devresinin güç tüketimi, sistem saniyede 50 kare gösterebilen bir hızda çalıştığında sırasıyla 1.76 mV ve 236.9 mW olarak ölçülmüştür.

Anahtar kelimeler: Büyük biçimli mikrobolometre dizinleri için okuma devreleri, mikrobolometreler için düşük güçlü okuma devreleri, soğutmasız kızılötesi odak düzlem dizinleri.

To my family,

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CHAPTER 1

INTRODUCTION

The electromagnetic (EM) spectrum is divided into several regions according to the wavelength of the EM radiation, and each region has specific application areas. Infrared (IR) radiation term refers to the EM wave region between the microwaves (1 m to 1 mm) and visible light (760 nm to 380 nm). One of the most notable applications involving IR radiation is thermal imaging, which has several military [1-3] and civilian [2, 4-6] applications. Thermal imaging is based on the fact that all objects above 0 K emit EM waves with a spectrum depending on the absolute temperature of the object. For the objects at typical ambient temperatures, the peak of this spectrum falls into the IR region; therefore, thermal imagers use IR detectors. There are two main types of infrared detectors: Photon detectors and thermal detectors.

Photon detectors use low energy bandgap semiconductor materials or quantum well structures with low energy barriers such as QWIPs in order to detect the IR radiation. Incoming photons with sufficient energy create electron-hole pairs by transferring the electrons from the valence band to the conduction band, and the transferred electrons are collected by applying an electric field. However, at room temperature, thermally generated electron-hole pairs are much more than the IR induced pairs due to the low energy bandgap. In order to decrease thermal excitation, these detectors should be cooled down to cryogenic temperatures; therefore, photon detectors are also called cooled detectors.

Photon detectors have better performance compared to the thermal detectors; however, cooling operation requires heavy and expensive systems with high power dissipation.

Thermal detectors do not directly detect the IR photons, instead, they detect the rise in the temperature of a material due to absorbed IR radiation. For this purpose, materials having measurable temperature dependent parameters are used. Thermal detectors can operate at room temperature; therefore, they are also called uncooled IR detectors. Although there are many different thermal detection mechanisms, the most commonly used ones are pyroelectric effect, thermoelectric effect, and bolometric effect [7]. The pyroelectric effect is the spontaneous electric polarization observed in some crystals caused by rapid temperature changes [8]. Pyroelectric detectors do not have DC response; therefore, the IR radiation should be modulated by using choppers, which is the main disadvantage of these detectors. Another drawback of the pyroelectric detectors is that their monolithic implementation with CMOS is difficult. Thermoelectric detectors are built using thermocouples, which is formed by connecting two conductive materials at two junction points. If there is a temperature difference between the two junctions, a voltage will be generated, which is called thermoelectric or Seebeck effect. Thermoelectric detectors can operate at DC excitation; however, their low responsivity and large detector size limit their usage.

Bolometric effect mainly refers to the resistance change caused by increasing temperature [8]. Bolometers have significant advantages over the other thermal IR detector types: they have high responsivity, it is possible to fabricate small sized bolometric detectors, and no IR modulation is required. Monolithic microbolometer arrays fabricated using standard CMOS and MEMS technologies currently dominate the thermal IR detection market, and extensive research is

still going on to fabricate larger arrays with high responsivity, high speed, and low power.

The readout circuits are critical for the performance of bolometers. Besides detecting IR radiation with a high responsivity, the readout circuit should have high signal-to-noise ratio (SNR) and wide dynamic range in order to increase the overall quality of the system. Furthermore, low power dissipation, low number of I/O pads, and small silicon area are the key parameters for the microbolometers to be used in mobile applications.

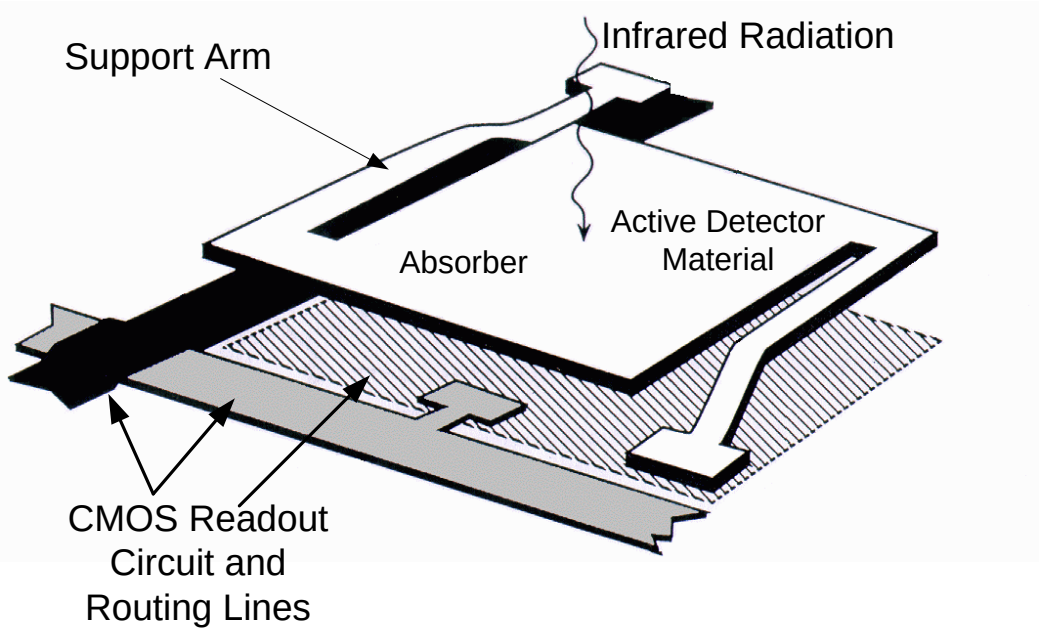
METU has been working on large format microbolometer array readouts in order to develop 320x240 focal plane arrays (FPAs) with 50 µm pixel pitch. Two generations of 320x240 FPA readouts have been designed and fabricated since the research has begun, and room temperature IR scenes have been obtained using the fabricated microbolometers. However, these designs had a number of shortcomings such as high power dissipation and high number of I/O pads, which makes them unsuitable for mobile applications. Moreover, 50 µm pixel pitch limits the maximum array size due to the limitations in the CMOS technology.

This study presents the development of a new ROIC for large format microbolometer arrays, which is mainly focused on overcoming the drawbacks of the previous designs at METU. The ROIC is designed for a 384x288 FPA with 35 µm pixel pitch. It employs a new readout architecture that provides very low power operation. The readout has two differential output channels, and single output channel mode is also available. The FPA is designed to operate at 50 fps when two output channels are used, and 32 pads are necessary in this mode. The designed ROIC has been fabricated in a standard 0.6 µm CMOS process, and occupies an area of 17.84 mm x 16.23 mm. The initial tests verify the proper operation of the fabricated chip.

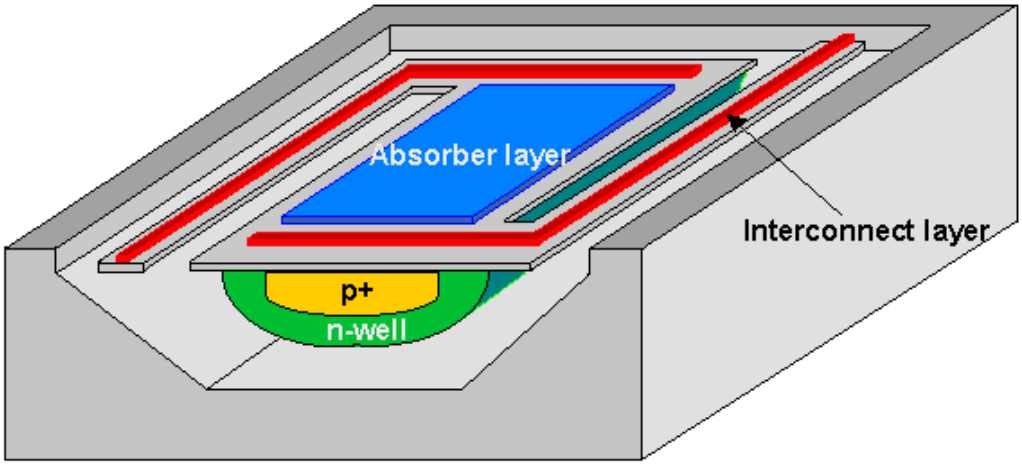
1.1 Microbolometers

Microbolometers detect the IR radiation by measuring the change in a temperature dependent electrical parameter of a sensitive material. The most common microbolometer types are resistive and diode types. However, there are also capacitive [9] and transistor type [10] microbolometers reported in literature. Resistive type microbolometers measure the change in the resistance of the sensitive material. In diode type microbolometers, the measured electrical parameter is the forward bias voltage of a diode under constant current bias. In both types, the cause of the electrical parameter change is the temperature change in the sensitive material due to the absorbed infrared power.

The IR radiation power that can be absorbed from an object at room temperature by a microbolometer pixel is in the order of nanowatts. In order to obtain a detectable temperature change from such small amounts of power, the microbolometer pixels should have excellent thermal isolation. The most common method to achieve the necessary thermal isolation in microbolometer pixels is to use suspended bridge structures. Suspended bridge structures can be implemented on silicon wafers using surface [11-14] or bulk [15, 16] micromachining techniques. In surface micromachining, thin layers of temperature sensitive materials are deposited on top of a sacrificial layer and suspended by removing the sacrificial layer. In bulk micromachining, pixels are suspended by etching the silicon substrate underneath the bridge. Figure 1.1 shows perspective views of microbolometer pixel structures fabricated using (a) surface [11], and (b) bulk [15] micromachining techniques.



(a)



(b)

Figure 1.1: Perspective view of microbolometer structures fabricated using (a) surface [11], and (b) bulk [15] micromachining techniques.

Surface micromachining allows the utilization of highly temperature sensitive materials in the form of thin layers, which provides high responsivity and speed. Therefore, it is the most common technique in the fabrication of high

performance microbolometers. There are different temperature sensitive materials used in surface micromachined microbolometers such as VO_x [17, 18], a-Si [19, 20], PolySiGe [21], YBaCuO [22, 23].

The history of the bolometers goes as far as 1880 [24]; however, the development of IR imaging arrays waited for mature microfabrication technologies, which took place in the 1980s. The first thin film microbolometers were proposed by R. Hartmann and K. Liddiard in 1982 and 1984, respectively [25]. Honeywell Inc. began to develop the first microbolometer arrays in USA in 1983, and completed a 336x240 array with 50 µm pixel pitch in 1991 [8]. After the public release of the technology in 1992, several companies such as Raytheon, BAE Systems, DRS Technologies, SCD, Indigo Systems, ULIS started to work on this subject [24], and 1024x768 arrays with 17 µm pixel pitch have been recently reported [20]. Furthermore, there are a number of research institutes studying microbolometers such as IMEC in Belgium, ETH Zurich in Switzerland, University of Texas at Arlington and University of Michigan in the USA, KAIST in Korea, and METU in Turkey [26].

1.2 Preamplifiers Used in Resistive and Diode Type Microbolometer Readouts

Microbolometers convert the IR radiation energy into electrical signals in order to obtain an infrared image. The conversion is performed in two steps: The first step is the conversion of the IR radiation energy into heat energy, which takes place in the pixels. The heat energy increases the temperature of the sensitive material in the pixels, causing changes in its electrical parameters. The second step is the conversion of the temperature change in the pixels into an electrical signal, which is performed by the readout circuit. The readout circuit measures the amount of the change in the electrical parameters of the sensitive material, which is a measure of the absorbed infrared radiation.

As mentioned in Section 1.1, the two most common type microbolometers are resistive and diode type. Therefore, the electrical parameter to be measured by the microbolometer readouts is either resistance or diode forward bias voltage, depending on the type of the microbolometer. Both measurements require electrical biasing of the pixels. The pixel biasing and initial amplification of the resultant signal is performed by preamplifiers in microbolometer readouts. The following sections describe different preamplifier types used in resistive and diode type microbolometers.

1.2.1 Preamplifiers Used in Resistive Microbolometers

In resistive microbolometers, the absorbed infrared power increases the pixel temperature and consequently, the pixel resistance changes. The amount of the resistance change depends on the temperature coefficient of resistance (TCR) of the sensitive material in the pixel. The resistance of the sensitive material is given as

$$R = R_0 + \alpha \cdot R_0 \cdot \Delta T \qquad 1.1$$

where R_0 is the resistance at the reference temperature, α is the TCR and ΔT is the temperature change due to absorbed infrared power. If the pixel resistance is measured by a readout circuit, the amount of the absorbed infrared power can be extracted using the resistance data.

The pixel resistance can be measured by either applying voltage and measuring the current, or applying current and measuring the voltage. There are a number of preamplifier types for resistive microbolometers, each employing either one of these methods. In the following sections, four of these preamplifier types will be described: (1) buffered current direct injection, (2) capacitive

transimpedance amplifier, (3) Wheatstone bridge differential amplifier, and (4) constant current buffered direct injection. In all of these preamplifiers, the signal is amplified by current integration. As well as amplifying the signal, the integration operation limits the bandwidth to

$$BW = \frac{1}{2 \cdot t_{int}} \tag{1.2}$$

where t_{int} is the integration period [27]. Limited bandwidth decreases the noise interference, which is critical especially at the early stages of the readout.

1.2.1.1 Buffered Current Direct Injection (BCDI)

Figure 1.2 shows the simplified schematic of a bolometer current direct injection preamplifier [28]. In this preamplifier type, the detector is biased by constant voltage through an injection transistor and the resultant current is integrated on a capacitor. A symmetrical counterpart is implemented using an infrared blind reference resistor, in order to cancel the DC portion of the current. The bipolar transistors provide constant bias on the resistors, and they have considerably low current noise when compared to MOS transistors.

The most important drawback of the BCDI preamplifier is that the integrator output is directly connected to the output node of the biasing circuit [29]. In this structure, the change in the capacitor voltage affects the detector and reference currents due to the finite output resistance of the transistors. This feedback effect causes nonlinearity in the integrator output. In order to overcome this problem, either the voltage change in the capacitor should be decreased or the output resistance of the biasing circuit should be increased. The change in the capacitor voltage can be decreased by increasing the capacitance or decreasing the integration period. However, both methods

result in reduced responsivity. On the other hand, the output resistance can be increased by either increasing the resistance values of the detector and reference pixels, or increasing the forward gain of the injection transistors. However, increasing the resistances decreases the responsivity due to reduced bias current, and the forward gain of the transistors is determined by the process. As a result, the nonlinearity can be reduced by only decreasing the responsivity, which is not desirable.

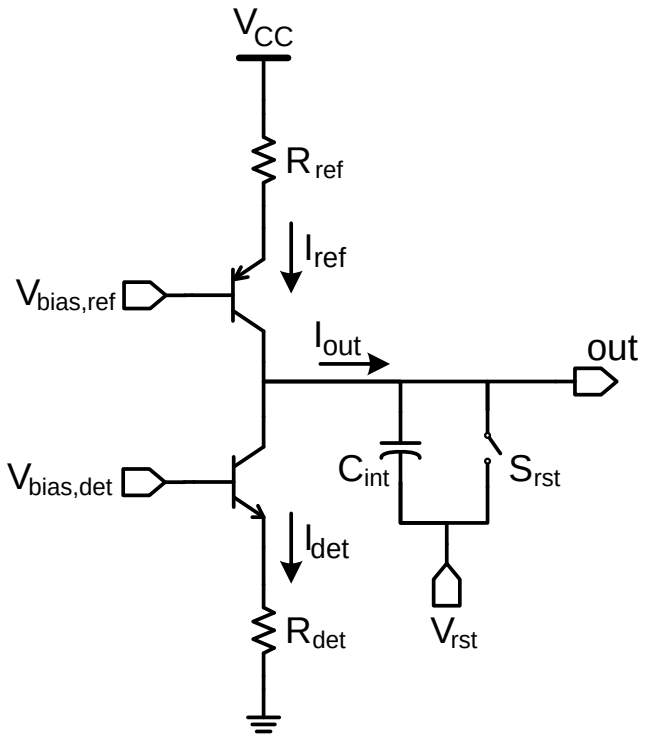


Figure 1.2: Simplified schematic of a buffered current direct injection preamplifier [28]. The detector is biased through a BJT, which provides almost constant voltage over the detector. The symmetrical counterpart cancels the DC portion of the detector current; therefore, only the current due to absorbed IR radiation is integrated over the capacitor.

1.2.1.2 Capacitive Transimpedance Amplifier (CTIA)

CTIA type preamplifiers are commonly used in resistive microbolometer readouts [30-33]. Figure 1.3 shows the simplified schematic of a capacitive transimpedance amplifier [31]. Similar to the BCDI circuit, the detector and reference resistors are biased with constant voltage; however, MOS transistors are generally used in CTIA instead of bipolar transistors.

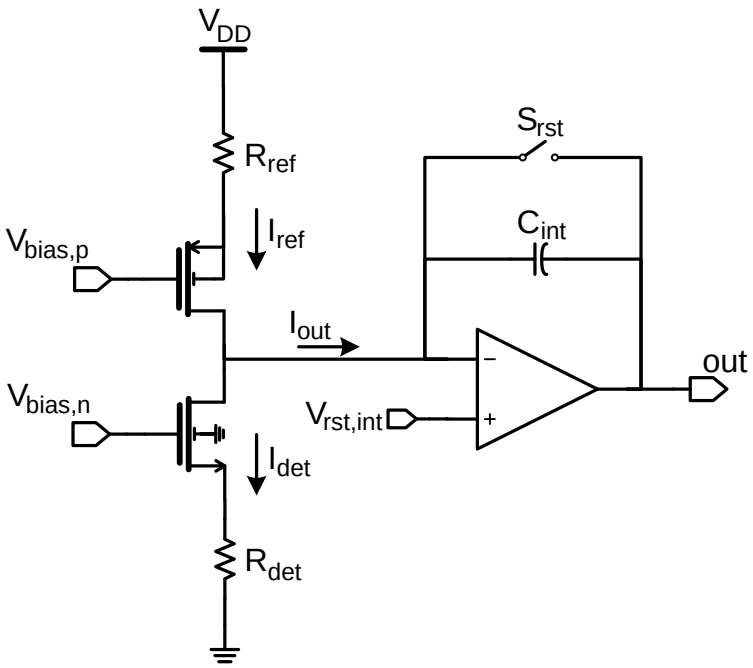


Figure 1.3: Simplified schematic of a capacitive transimpedance amplifier, which is commonly used in resistive microbolometer FPAs [31].

In this structure, a different integrator structure is used in order to solve the nonlinear integration problem of the BCDI circuit caused by the direct coupling of the integrator output to the bias circuit output. The operational amplifier in the switched capacitor integrator keeps the output node of the bias circuit at constant voltage during integration. As a result, the output current will be

independent of the integrator output as long as the opamp stays in its linear region.

The noise contribution of the CTIA is higher compared to the BCDI, due to higher flicker noise of the MOS transistors and addition of an operational amplifier. The biasing transistors directly contribute to the current noise since they are on the current path. The noise contribution of the operational amplifier is mostly due to the voltage noise at the inverting input terminal. The negative input terminal is directly connected to the output of the bias circuit, and the voltage fluctuations at that node affect the bias current through the finite output resistance of the biasing transistors. The flicker noise of the MOS transistors can be reduced by simply increasing the transistor area. In order to decrease the noise contribution of the opamp, the output resistance of the bias circuit should be increased. Actually, the output resistance is typically high enough due to source degeneration, and can be further increased by increasing the transconductance of the injection transistors. Consequently, low noise CTIA preamplifiers can be implemented using proper design techniques, and the CTIA is the most preferred preamplifier type for resistive microbolometers.

1.2.1.3 Wheatstone Bridge Differential Amplifier (WBDA)

Wheatstone bridge differential amplifier uses a Wheatstone bridge followed by a low noise differential transconductance amplifier and an integrator. Figure 1.4 shows the simplified schematic of a WBDA preamplifier [34]. The differential operation of the preamplifier reduces the errors caused by process and temperature variations.

The output resistance of the bridge is considerably low when compared to the previous bias circuits since there are no injection transistors [29]. Therefore, the differential amplifier should have a high input impedance. The input referred voltage noise of the amplifier is also critical since it directly adds up to

detector noise. The achievable noise level of the WBDA in the CMOS technology makes it suitable only for detectors with high resistance, and therefore, it is not suitable for detectors with low resistance such as n-well detectors [29].

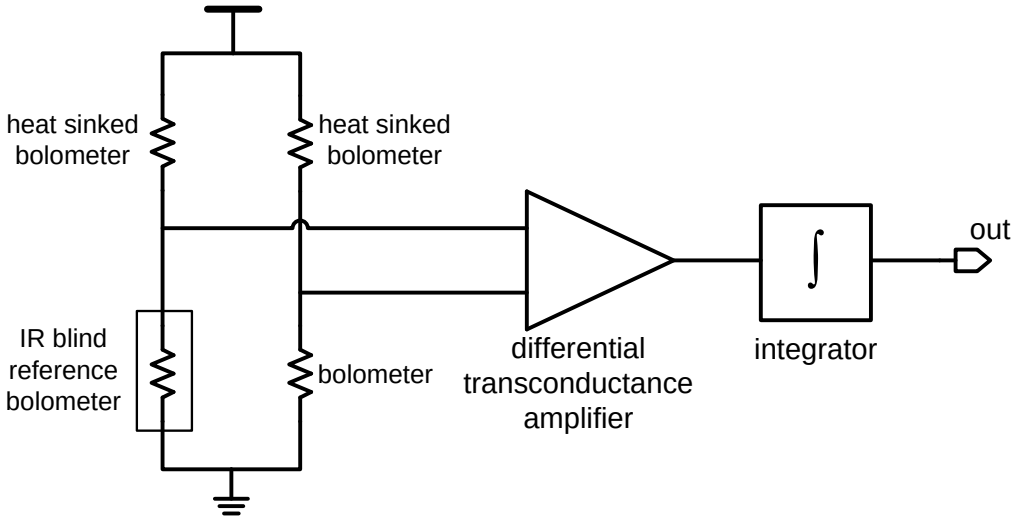


Figure 1.4: Simplified schematic of the Wheatstone bridge differential amplifier used in a 640x480 microbolometer FPA [34].

1.2.1.4 Constant Current Buffered Direct Injection (CCBDI)

The constant current buffered direct injection preamplifier uses constant current biasing, unlike the preamplifiers described in the previous sections. The constant current biasing provides improved responsivity and linearity; however, it is not easy to implement low noise and stable current sources [35]. Figure 1.5 shows the simplified schematic of a CCBDI preamplifier [35]. In this circuit, the detector voltage is compared to a reference voltage by a transconductance amplifier, and the resultant current is integrated on a capacitor. The current source at the output of the transconductance amplifier is used to sink the offset current, and therefore, increase the dynamic range.

The CCBDI preamplifier has some important drawbacks in terms of noise, which limits its usage especially in resistive microbolometers with high detector resistance [29].

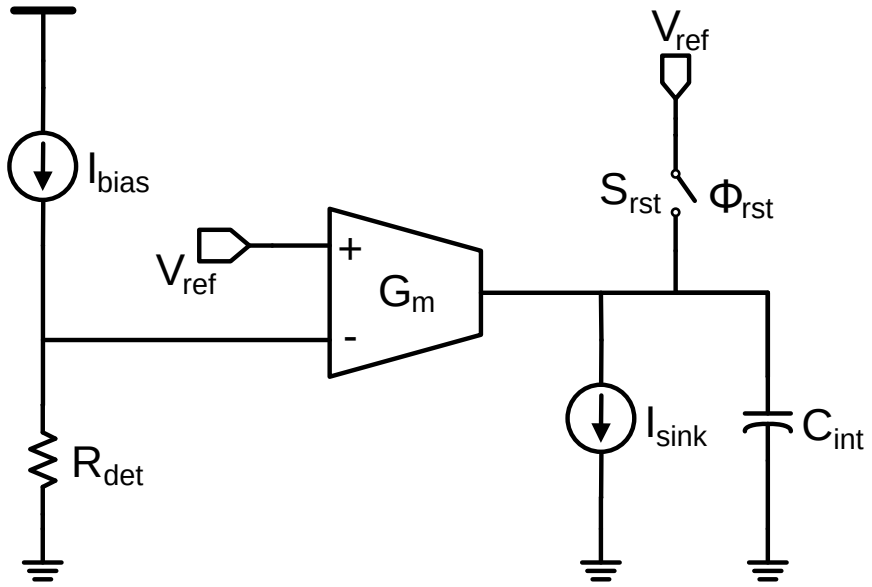


Figure 1.5: Simplified schematic of a constant current buffered direct injection preamplifier [35].

1.2.2 Preamplifiers Used in Diode Type Microbolometers

Diode type microbolometers use forward biased diodes in order to measure the temperature change caused by the infrared radiation. The forward bias voltage of a diode can be calculated using the formula

$$V_D = V_{D0} + \alpha_D \cdot \Delta T \qquad 1.3$$

where V_{D0} is the forward bias voltage at a reference temperature, α_D is the temperature coefficient of diode forward voltage, and ΔT is the temperature change due to the absorbed infrared radiation. Typically, the diode microbolometers have less temperature sensitivity when compared to resistive ones due to their low temperature coefficients. Therefore, the preamplifiers used in diode microbolometers should have very low noise levels in order to obtain a reasonable signal-to-noise ratio [29].

Due to the exponential I-V characteristics of the diodes, applying constant voltage and measuring the current is not suitable for diode type microbolometers [36]. Instead, the applying current and measuring voltage method is used in the readouts. There are two types of diode microbolometers reported in the literature: SOI diode and n-well diode microbolometers. The first one uses gate modulation integration (GMI) preamplifier [37] while the second one uses differential buffered injection-capacitive transimpedance amplifier (DBI-CTIA) [11, 34, 35]. The following sections describe these preamplifiers.

1.2.2.1 Gate Modulation Integration

Figure 1.6 shows the schematic of the gate modulation integration circuit used in the SOI diode type 320x240 FPA [37], where the diodes in the pixel are biased with constant current. The absorbed infrared radiation increases the diode temperature, and consequently, decreases the forward bias voltage of the diodes. This voltage change is converted to current by a second transistor and integrated on a capacitor in order to amplify and band-limit the signal [29].

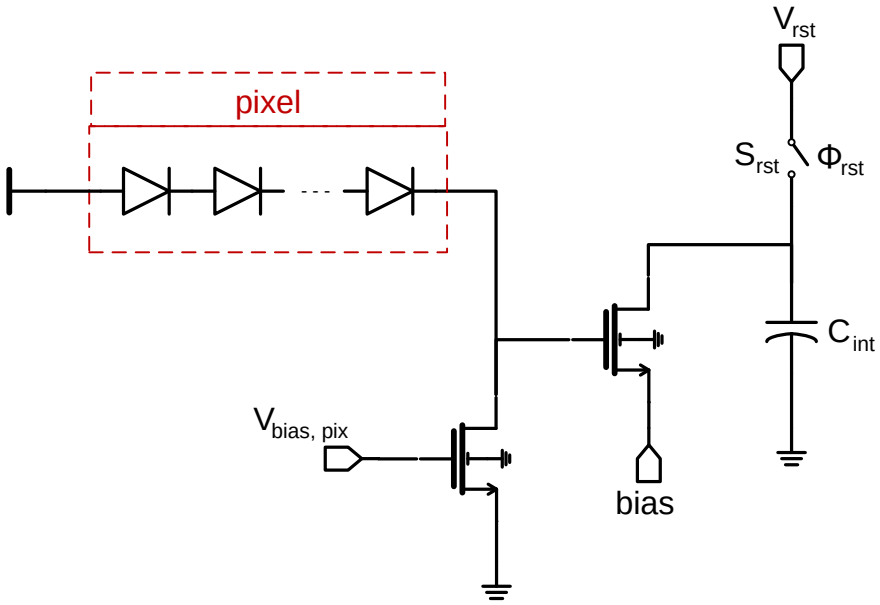


Figure 1.6: Simplified schematic of the gate modulation integration circuit used in the SOI diode type 320x240 FPA [37].

1.2.2.2 Differential Buffered Injection – Capacitive Transimpedance Amplifier

Figure 1.7 shows the simplified schematic of the DBI-CTIA type preamplifier used in the 64x64 and 128x128 n-well type diode microbolometer FPAs developed at METU [15, 38, 39].

The DBI-CTIA type preamplifier consists of a biasing stage, a differential transconductance amplifier, and an integrator. The biasing stage is used to bias the detector and the IR-blind reference diodes with a constant current. The voltage difference between the cathodes of the diodes are converted to current by the differential transconductance amplifier, and the resultant current is amplified and band limited by the integrator [29].

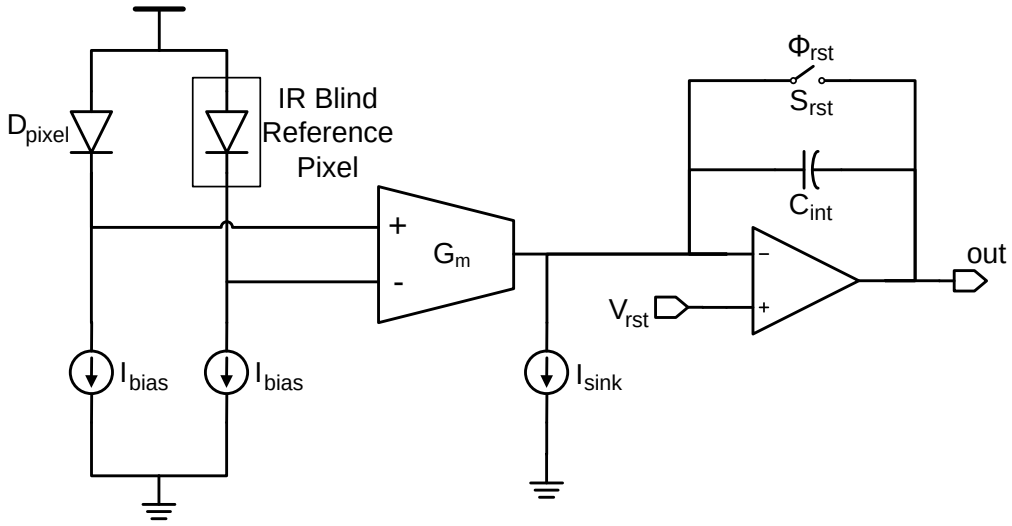


Figure 1.7: Simplified schematic of the differential buffered injection - capacitive transimpedance amplifier preamplifier circuit [15, 38, 39].

The pixels of the n-well type diode microbolometers consist of only one pixel; therefore, the responsivity is lower compared to SOI diode type microbolometers. In order to compensate for the low pixel responsivity, the preamplifier should contribute low noise. This can be achieved by using higher bias levels and larger transistor dimensions. However, large area reduces the number of preamplifiers that can be fit into the limited chip area, which causes shorter integration times, and hence, larger noise bandwidth [15, 38, 39].

1.3 Readout Architecture of the Microbolometer FPAs

The preamplifier circuits described in Section 1.2 are the most basic units of the readout circuits; however, a microbolometer FPA readout circuit includes several other blocks in order to function properly. Figure 1.8 shows the block diagram of the typical readout architecture used in the microbolometer FPAs [29]. The analog readout block is the main unit, which performs the measurement and feeds the data to the chip output. The analog readout block needs digital timing signals for operations such as integrator reset, integration

duration and output multiplexing. These digital signals are generated by the digital timing block. The digital timing block also generates the inputs of the row and column multiplexers, which are used to address the pixels to be processed at a given time [29].

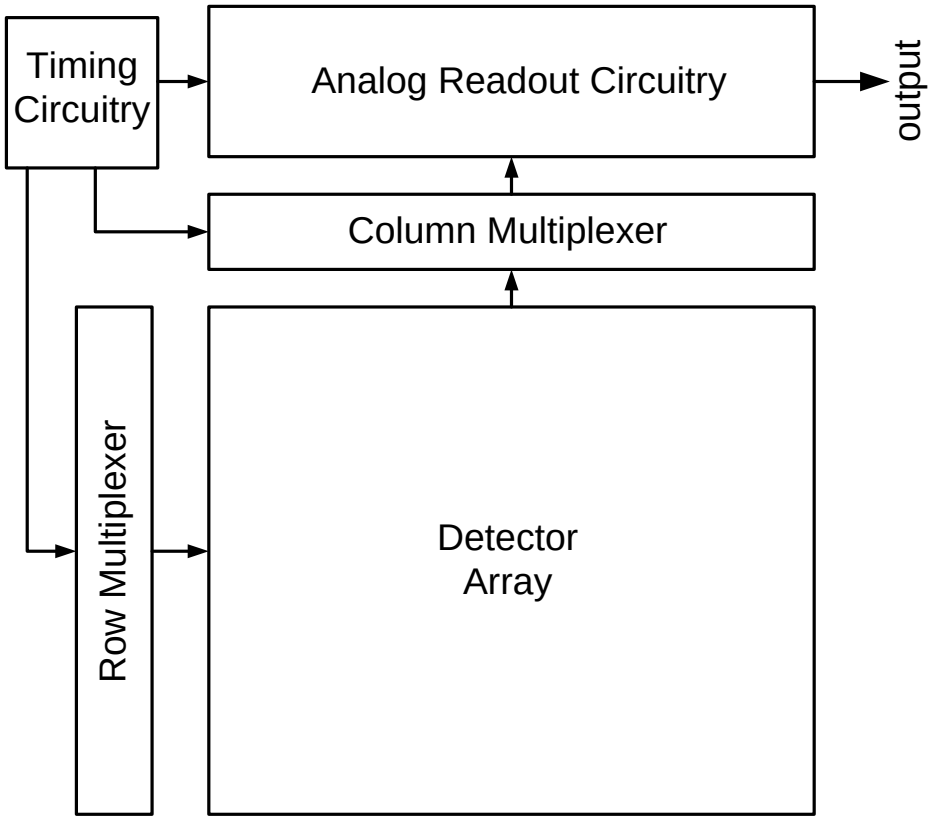


Figure 1.8: Block diagram of the typical readout architecture used in microbolometer FPAs [29]. The pixels addressed by row and column multiplexers are connected to the analog readout circuitry for the readout operation. The timing block generates the timing signals required by the multiplexers and the analog readout circuitry.

During the readout operation, the pixels in the detector array are addressed sequentially by the row and column multiplexers. The addressed pixels are biased by the preamplifier circuits while the other pixels remain unbiased. As a

result, each pixel is biased by short pulses during the readout operation. The purpose of this bias procedure, which is called pulse biasing, is saving power as well as preventing overheating of the pixels. However, the initial transients during the pixel selection introduce considerable noise; therefore, the current integration should not be enabled before the transients decay [8].

The readout architecture can be designed either fully-serial or parallel. In the fully serial operation, the readout processes a single pixel at a given time; therefore, one readout unit is sufficient for the whole array. Using a single readout unit consumes small silicon area and reduces the errors caused by process variations. However, the pixel selection time for a given frame rate decreases as the FPA size increases in the fully serial readout architecture. A short pixel selection duration means a short integration period, which necessitates wide bandwidth, and therefore, increases the noise. In a parallel readout architecture, there are several identical readout units, enabling more than one pixel to be processed at a given time. Parallel processing increases the allowable pixel selection time and allows longer integration periods. On the other hand, the fixed pattern noise caused by process variations is higher in the parallel readout architecture [8]. In large format microbolometer FPAs, fully serial architectures are not suitable due to the excessively short pixel selection durations; and therefore, parallel readout architectures are preferred.

1.4 Nonuniformity Correction in Microbolometer FPAs

In microbolometers, the process variations cause nonuniformity in the detectors and in the readout circuitry. The nonuniformity causes a fixed pattern noise (FPN) and can even saturate the readout, especially in the large format arrays. The FPN problem can be solved with a technique called the nonuniformity correction (NUC), which is an essential part of the microbolometer FPAs.

Nonuniformity correction has two main steps: (i) preventing the saturation of the readout, and (ii) mapping the readout output to the absorbed IR radiation. The first step is performed by on-chip bias correction structures while the second step generally requires external processors.

The first step of NUC is applied to the detector bias voltages, and it is called bias correction [40]. In order to perform the bias correction, the detector resistance nonuniformity is measured for the whole array, and appropriate bias voltages are determined for each detector. The calculated bias data is stored digitally in an external memory and sent to on-chip digital to analog converters (DACs) during the readout operation, which are used to generate the detector bias voltages. The bias correction method minimizes the DC part of the integration current and prevents the saturation of the readout as well as increasing the dynamic range.

Performance of the bias correction method is limited with the resolution of the DACs; therefore the DC current cannot be cancelled perfectly. Furthermore, this method does not correct the FPN caused by the readout circuit and non-uniform detector responsivity values. As a result, even after bias correction, each pixel will have a specific input-output characteristic. Therefore, a mapping operation between the outputs and the incident IR radiation, which is the second step of NUC, is necessary to remove the FPN completely. There are a number of methods in the literature for this operation, such as two-point [41, 42], multi-point [43], and scene-based [44, 45] nonuniformity correction algorithms.

1.5 Performance Parameters of the Microbolometer Readout Circuits

The main performance parameters of a microbolometer readout circuit are responsivity, signal-to-noise ratio (SNR), and dynamic range. The power

dissipation and occupied silicon area are also important constraints for microbolometer readouts.

Responsivity of a system is defined as the ratio of its output to the measured quantity. The readout circuit of a resistive microbolometer is supposed to measure the resistance change in the detector. Therefore, the readout responsivity can be defined as the ratio of the output voltage or current to the resistance change. For a CTIA type preamplifier, the voltage responsivity can be approximated as

$$\Re = I_B \cdot \frac{t_{int}}{R_{det} \cdot C_{int}} \quad 1.4$$

where I_B is the detector bias current, R_{det} is the detector resistance, t_{int} is the integration period, and C_{int} is the integration capacitance. Equation 1.4 states that increasing the bias current or integration time, or decreasing the detector resistance or integration capacitance increases responsivity. However, detector resistance is not a readout related parameter, the integration period is limited with the available pixel selection time, and self-heating of the detector limits the detector bias current. Therefore, the most convenient method for increasing the voltage responsivity of a CTIA is using smaller integration capacitance.

SNR is the ratio of the meaningful signal power to the noise power corrupting the signal, and it is equal to

$$SNR = \frac{S_{in}}{n_{in,rms}} \quad 1.5$$

where S_{in} is the input signal amplitude and $n_{in,rms}$ is the rms value of the input referred noise voltage. In order to have a better SNR, either responsivity should

be increased while keeping the noise constant, or the readout noise should be reduced. Preamplifier is the most critical part of the readout in terms of noise since the noise of the latter stages are divided by preamplifier gain while calculating the input referred noise. Therefore, a low noise preamplifier design is essential for high performance readout circuits.

The dynamic range is defined as the ratio of the operation range to the minimum detectable signal. A readout circuit with a high dynamic range can provide high detail level in a high contrast scene without being saturated. In order to have a high dynamic range, the readout circuit should have a high operation range and responsivity. The operation range of the readout circuit is generally determined by the opamps on the signal path; and therefore, can be maximized by using appropriate opamp topologies. However, extra voltage headroom necessitated by the currents due to array nonuniformity and self heating prevents the effective usage of the operation range. The offset current caused by the nonuniformity can be cancelled to some extent by applying bias correction as explained in Section 1.4. The self heating current is caused by the asymmetry in the thermal conductance values of the detector and reference pixels. In large format microbolometer arrays, the number of reference pixels is much less than the detectors due to limited area; and therefore, reference pixels are addressed more frequently. In order to prevent overheating due to frequent addressing, the reference pixels are designed to have higher thermal conductance compared to the detector pixels. Figure 1.9 shows (a) the currents of reference and detector pixels and (b) the corresponding integration curve during an integration period [28]. As seen in the figure, the unbalanced current due to different heating curves causes extra voltage headroom usage in the integrator. Therefore, a careful design of the reference pixels and effective bias correction are essential for obtaining a high dynamic range.

In most modern applications, microbolometers are implemented on mobile devices with battery powered modules, increasing the importance of the power dissipation. Not only the power dissipated by the microbolometer itself, but also the power dissipated by the thermo-electric coolers (TECs), which are used to stabilize the temperature of the microbolometer chips, affect the battery lifetime [46]. As the Joulean heating on the microbolometers increase, the TEC needs more power to stabilize the temperature. Consequently, low power dissipation is a very important performance parameter in modern microbolometer readout circuits.

The final performance parameter to be mentioned in this section is the size of the readout circuit. Smaller readouts reduce the unit cost of the bolometers by increasing the number of FPAs fabricated on a single wafer. Not only the FPA cost, but also the cost of packaging and external electronics are decreased as the readout circuit gets smaller.

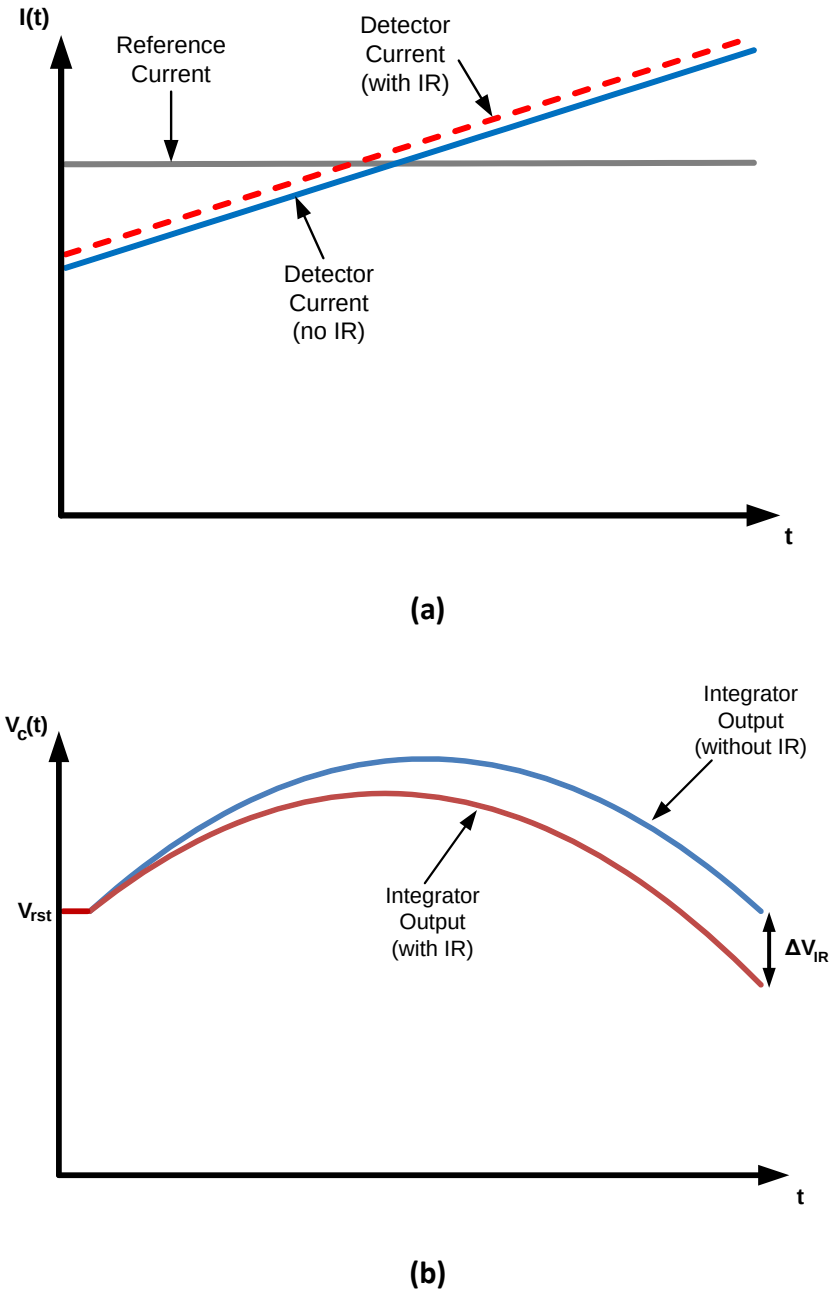


Figure 1.9: Currents of reference and detector pixels (a) and the corresponding integration curve (b) during an integration period [28].

1.6 Previous Work on Microbolometers at METU

The research on microbolometers at METU started in 1997, in order to develop low cost IR detector arrays using very simple post-CMOS processes. Most of the research had been based on n-well [15, 38, 39, 47, 48] and SOI [49, 50] diode type microbolometers. However, the large pixel dimensions of these bolometers limit the array size. Furthermore, low temperature sensitivity of the silicon diodes reduces the maximum available responsivity of the FPAs. Therefore, in order to develop large format FPAs with high performance, resistive microbolometer research is also being conducted.

The work on large format resistive microbolometer FPAs at METU has started in 2003. The first goal was designing a monolithic 320x240 resistive microbolometer FPA with 50 µm pixel pitch. Since the research has begun on this work, two readout generations are designed and fabricated in a standard 0.6 µm CMOS process. The detector pixels are also fabricated on the CMOS readouts in METU-MEMS facilities using surface micromachining techniques, and Figure 1.10 shows the SEM photographs of the 50 µm x 50 µm pixels from the 320x240 resistive microbolometer FPA fabricated at METU [51]. IR images of room temperature scenes are taken using these FPAs, and Figure 1.11 shows two sample IR images obtained using the fabricated arrays [51]. The first and second generation FPAs have a power dissipation of 900 mW and 700 mW, respectively, when operating at 30 fps with single output channel.

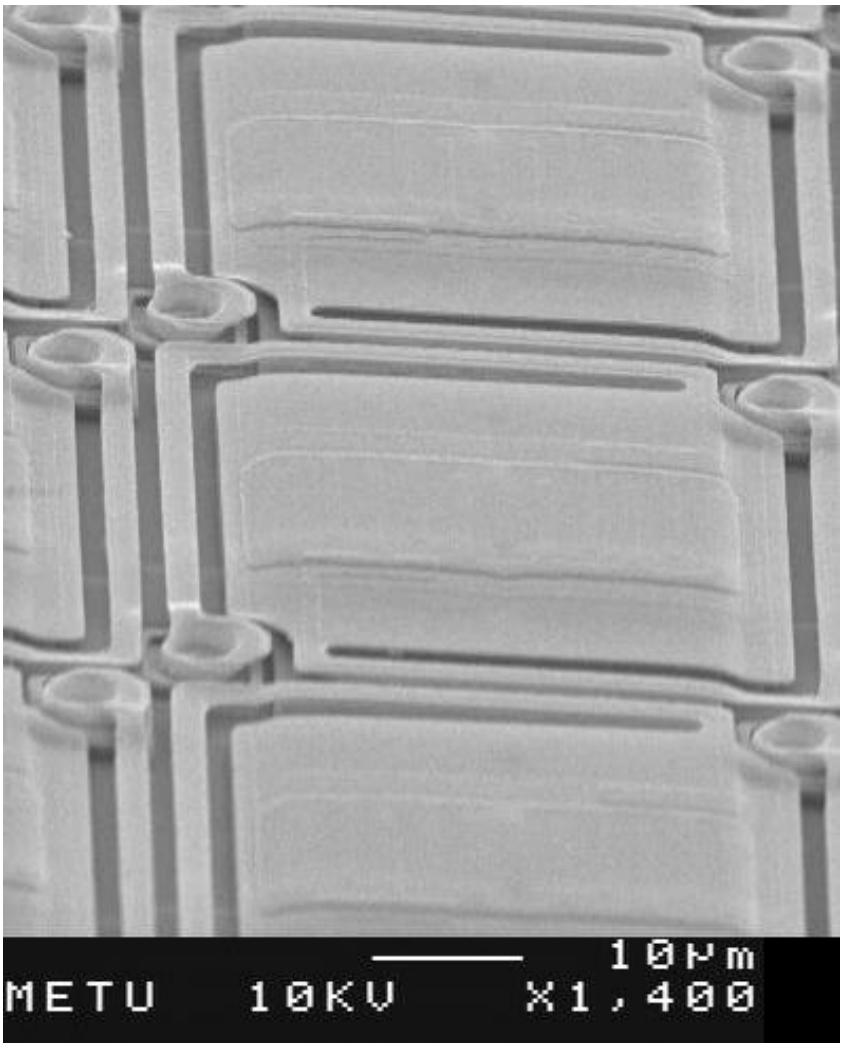


Figure 1.10: SEM photographs of the 50 µm x 50 µm pixels from the 320x240 microbolometer FPA fabricated at METU [51].

(a)

(b)

Figure 1.11: Sample IR images of room temperature scenes obtained using the 320x240 resistive microbolometer FPA developed at METU [51].

The main focus of this thesis is to implement a readout circuit for large format resistive microbolometer arrays, where the array size is 384x288 and the pixel size is 35 µm. The research is focused on reducing the power dissipation and the number of I/O pins in order to allow easy commercialization of the final FPA. The research objectives and organization of the thesis are described in the following section in more detail.

1.7 Research Objectives and Thesis Organization

The objective of this research is to develop high performance CMOS readout electronics for large format resistive microbolometer arrays. The specific objectives can be listed as follows:

1. Designing a resistive microbolometer FPA readout for 35 µm pixel pitch. The readout dimensions should allow sufficient readout units to be placed on the FPA in order to provide high performance.
2. Development of a readout architecture for a 384x288 resistive microbolometer FPA. The readout should be suitable for real camera systems; low number of I/O pads, an output system compatible with standard video systems, and operational controllability are the key parameters.
3. Reducing the power dissipation of the readout circuits previously developed for large format resistive microbolometer FPAs at METU. As well as dissipating low power, the readout should occupy small area and provide reasonable performance together with the detectors fabricated at METU-MEMS facilities.
4. Designing a complete imaging system to be used for IR imaging after detector fabrication. The system should be able to provide digital outputs in order to eliminate the need for complex external data acquisition equipments.

5. Preparing the necessary setups to test the designed readout. The testing procedure includes the design of test circuits and PCBs.

The thesis is organized as follows:

Chapter 2 presents a new readout architecture that greatly reduces the power dissipation when compared to conventional architectures. The low power architecture includes a new output buffering scheme, a digitally controllable opamp, and an improved bias correction structure. The test results of the fabricated low power preamplifiers and bias correction DACs are also given in this chapter.

Chapter 3 gives the details of the designed 384x288 resistive microbolometer FPA readout. The chapter presents the general readout architecture, analog and digital blocks of the readout circuit, and floor plan of the FPA, together with the planned pixel placement. As well as the design and operation principles; the block diagrams, schematics, layouts, and simulation results of the designed blocks are also given in this chapter.

Chapter 4 presents the fabricated 384x288 resistive microbolometer FPA readout, the 4-layer imaging PCB, and the results of the tests performed on the FPA readout and the imaging system.

Finally, Chapter 5 concludes the presented work and gives a list of possible future work on this research subject.

CHAPTER 2

ADVANCED LOW POWER READOUT ARCHITECTURE

This chapter presents the advanced readout architecture that is designed to decrease the power dissipation in large format microbolometer FPAs. The proposed low power architecture is designed for parallel readout operation, which is the preferred method in large format arrays. The overall power dissipation is reduced by employing an output buffering scheme, a special opamp whose output current capability is digitally controllable and a new bias correction DAC structure. The first two of these individual blocks had been implemented in a standard 0.6 μm CMOS process through a multi project wafer (MPW) run. After verifying the proper operation of these blocks, the design of the ROIC has been started, which is described in Chapter 3. The new bias correction DAC is developed during the design of the ROIC. Individual test circuits for all of these blocks are placed on the same wafer with the fabricated ROIC, and the test results of these latest circuits are also included in this chapter.

Section 2.1 gives the general description of the CTIA type readout channel, which is the basic unit of the designed architecture. Section 2.2 explains the advanced sampling and buffering structure used in the advanced architecture. Section 2.3 presents the low power digital to analog converter (DAC) structure used for the bias correction. Finally, Section 2.4 gives the test results of the proposed readout architecture.

2.1 CTIA Type Readout Channel

Large format microbolometer arrays employ parallel readout architectures due to the reasons stated in Section 1.3. The parallel readout architectures consist of several identical readout units, which typically consist of a preamplifier and a sample-and-hold circuit. In this work, these units are referred as readout channels. Readout channels can be classified according to the type of their preamplifiers.

Figure 2.1 shows the simplified schematic of a CTIA type readout channel. The CTIA type preamplifier in the readout channel biases the detector, amplifies the signal and limits the noise bandwidth by integration. The output of the preamplifier is sampled by the sample-and-hold (S&H) block at the end of the integration period and stored until the next sampling operation. Since the data is stored in the S&H blocks, the preamplifier can immediately start processing another pixel. In the meantime, the stored data is multiplexed and sent to chip output through buffers.

Readout channels are the basic units that process the signal obtained from the detectors. Therefore, selecting an appropriate readout channel type is the most critical step of a microbolometer readout design. In the large format resistive microbolometer FPAs previously designed at METU, CTIA type readout channels have been implemented due to their high linearity, low noise and ease of implementation in CMOS technology. The test results of these FPAs indicate that the CTIA type readout channels provide excellent performance; and therefore, the same type readout channels are also used in this work.

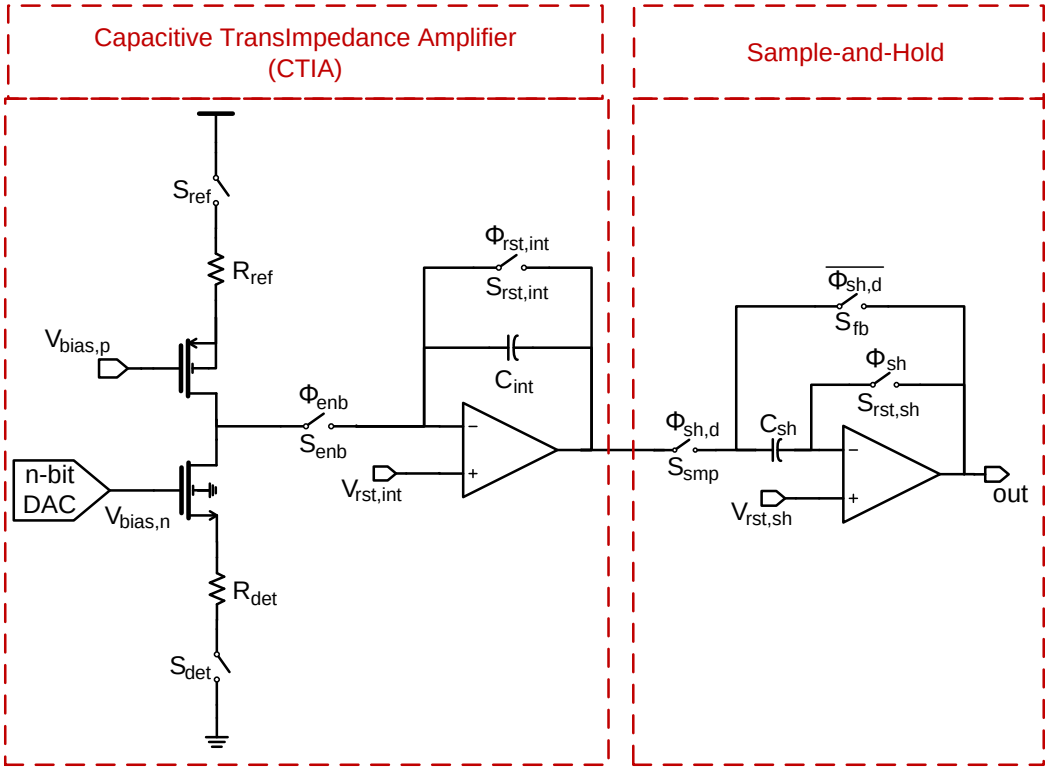


Figure 2.1: Simplified schematic of a CTIA type readout channel, which consists of a CTIA type preamplifier followed by a sample-and-hold (S&H) circuit.

2.2 Low Power Sampling and Buffering Scheme

The power dissipation of the readout channels in a large format microbolometer FPA is mostly due to high S&H output currents, which are necessary for output multiplexing. This section introduces the new output buffering scheme and the digitally controllable opamp to be used in S&H block to reduce the power dissipation of the readout channels. The output buffering scheme reduces the load capacitance of the S&H blocks, and hence, the required output current. The digitally controllable opamp further decreases the power dissipation by increasing the power efficiency of the S&H circuit.

Section 2.2.1 describes the conventional buffering structure and gives its power calculations. Then Section 2.2.2 and Section 2.2.3 present the new buffering scheme and the digitally controllable opamp, respectively. The improvement in the power dissipation provided by each method is also examined in the related section.

2.2.1 Conventional Sampling and Buffering Scheme

In the parallel readout architectures, the pixels are processed simultaneously; however, the outputs cannot be given in a parallel manner due to the large number of readout channels. Instead, they are multiplexed and routed to a certain number of output channels. The number of output channels generally depends on the array size and the frame rate; however, minimum number of output channels is always preferred in order to simplify the external signal processing circuitry. State-of-the art microbolometers generally use only one or two output channels [12, 52].

In conventional microbolometer readout circuits, the readout channels that will be routed to the same output channel are connected to a common bus through digitally controlled switches. The common bus is connected to the input of an output buffer, which drives the output channel. The readout channel outputs are multiplexed consecutively to the output buffer in order to form the serial output signal. Figure 2.2 shows the simplified block diagram of a conventional readout circuit with a single output channel [46].

The most important challenge of the conventional buffering scheme in large format and high frame rate FPAs is to drive the large bus capacitance within a short output multiplexing time. The output multiplexing time is defined as the duration allocated for the output of each pixel and can be calculated using the formula

$$t_{mux} = \frac{K}{f_{frame} \times M \times N} \quad 2.1$$

where K is the number of output channels, f_{frame} is the frame rate, and M and N denote the array dimensions.

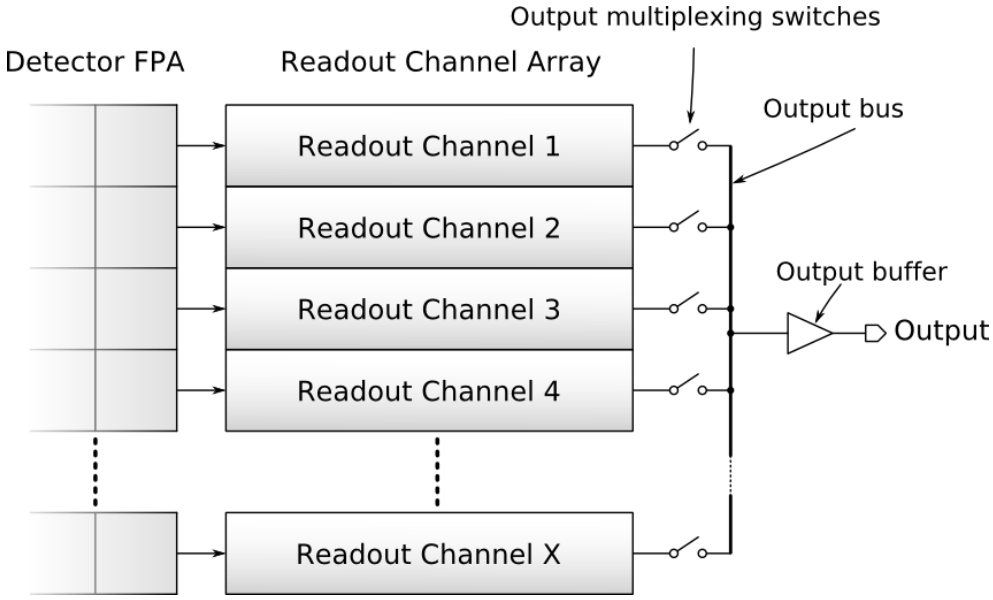


Figure 2.2: Simplified block diagram of a conventional readout circuit with single output channel [46].

Table 2.1 shows the output multiplexing times for various array dimensions, frame rates, and number of outputs which are calculated using Equation 2.1 [46]. The bus capacitance consists of the routing capacitances, off-switch capacitances, and the input capacitance of the output buffer, and it can be expressed as

$$C_{bus} = \underbrace{C_a \cdot W \cdot L + C_p \cdot 2 \cdot (W + L)}_{Routing\ \ cap.} + \underbrace{(X - 1) \cdot C_{sw}}_{Off-switch\ cap.} + \underbrace{C_{buf}}_{\substack{Output\ \ buffer \\ input\ \ cap.}} \quad 2.2$$

where C_a and C_p are the unit area and perimeter capacitances between the used metal lines and the substrate, respectively; W and L are width and length of the bus, respectively; X is the number of the readout channels connected to the bus; C_{sw} is the capacitance of a single switch between the readout channel and the bus when it is off; and C_{buf} is the input capacitance of the output buffer. Table 2.2 shows the capacitance values for various FPA readouts and detector sizes implemented in a standard 0.6 µm CMOS process, which are calculated using the typical parasitic capacitance values given in the process specification file of the standard 0.6 µm CMOS process [46].

Table 2.1: Output multiplexing times for various array dimensions, frame rates, and number of outputs [46].

FPA	f_{frame}	***K***	T_{settle}
384x288	25	1	362 ns
	50		180 ns
640x480	30	1	109 ns
		2	217 ns
	60	1	54.3 ns
		2	109 ns
		4	217 ns
1024x768	30	1	42.4 ns
		2	84.8 ns

Table 2.2: Calculated capacitance values for various FPA readouts and detector sizes implemented in a standard 0.6 µm CMOS process [46].

FPA Size	W_{det} *(µm)*	*X*	$C_{rc,out}$ *(pF)*	*Output Buffers*
384x288	50	384	8.3	Single output buffer
	35	192	4.8	Two output buffers
	25		4.5	
640x480	25	320	7.0	Two output buffers
	17		6.5	
1024x768	17	512	10.1	Two output buffers

In order to be able to read the data correctly, the voltage at the output channel should settle within the output multiplexing duration. If the output buffer delay is neglected and constant current charging is assumed for the bus capacitance, the required readout channel output current can be approximated as

$$I_{out} = \frac{\Delta V_{out} \cdot C_{bus}}{t_{mux}} \qquad 2.3$$

where ΔV_{out} is the change in the output voltage, C_{bus} is the bus capacitance, and t_{mux} is the output multiplexing time as given in Equation 2.1. Table 2.3 shows the approximate values of the readout channel output currents that are required to provide 2.5 V voltage swing at the output for various FPAs in a standard 0.6 µm CMOS process [46]. These values are calculated assuming that the bus capacitances given in Table 2.2 are driven by constant current within the corresponding output multiplexing times, which are calculated using Equation 2.1. In practice, the necessary currents are higher than the approximate values

given in the table due to the output buffer delay and non-zero small signal settling time.

Table 2.3: The approximate values of the readout channel output currents that are required to provide 2.5 V voltage swing at the output for various FPAs implemented in a standard 0.6 µm CMOS process [46].

FPA Size	*Pixel Pitch (µm)*	*Frame Rate*	*Number of Outputs*	*RC Output Current (µA)*
384x288	35	25	1	33.1
		50	1	66.2
640x480	25	30	1	160.5
		60	2	160.5
	17	60	1	298.2
1024x768	17	30	2	297.8

The power dissipation of the readout channels can be decreased by either decreasing the common bus capacitance or increasing the output multiplexing time. For a specific array size and frame rate, the only method to increase the output multiplexing time is adding extra output channels. Increasing the number of output channels also reduce the routing and off-switch capacitances by decreasing the number of readout channels connected to a single bus. On the other hand, as mentioned earlier, the number of output channels is minimized in state-of-the-art microbolometers in order to simplify the external electronics, and hence, reduce the device volume. Other methods to decrease the common bus capacitance are to use minimum size routing lines and

switches. However, thin routing lines and small size switches increase the resistance, and therefore, can increase the settling time.

2.2.2 Readout Channel Group Concept

The readout channel group (RCG) concept is developed to reduce the common bus capacitance without increasing the number of output channels [46]. For this purpose, the readout channels are divided into groups, each one having its own buffer. The outputs of these buffers are then multiplexed to the output buffers. As a result, the bus capacitance to be driven by the readout channels is reduced at the cost of one more stage on the signal path. Figure 2.3 shows the simplified diagram of a readout circuit with Q different RCGs and a single output channel [46].

The RCG bus capacitance of a readout circuit with Q RCGs can be calculated using the formula

$$C_{bus,rcg} = \underbrace{C_a \cdot W \cdot \frac{L}{Q} + C_p \cdot 2 \cdot (W + \frac{L}{Q})}_{Routing\ \ cap.} + \underbrace{(X-1) \cdot C_{sw}}_{Off-switch\ cap.} + \underbrace{C_{buf,rcg}}_{\substack{RCG\ buffer \\ input\ \ cap.}} \quad 2.4$$

where Q is the number of RCGs, $C_{buf,rcg}$ is the input capacitance of the RCG buffer, and all other parameters are the same as in Equation 2.2. Equation 2.4 states that the routing and off-switch components of the bus capacitance are decreased with the use of RCGs due to the reduced number of readout channels connected to the same bus.

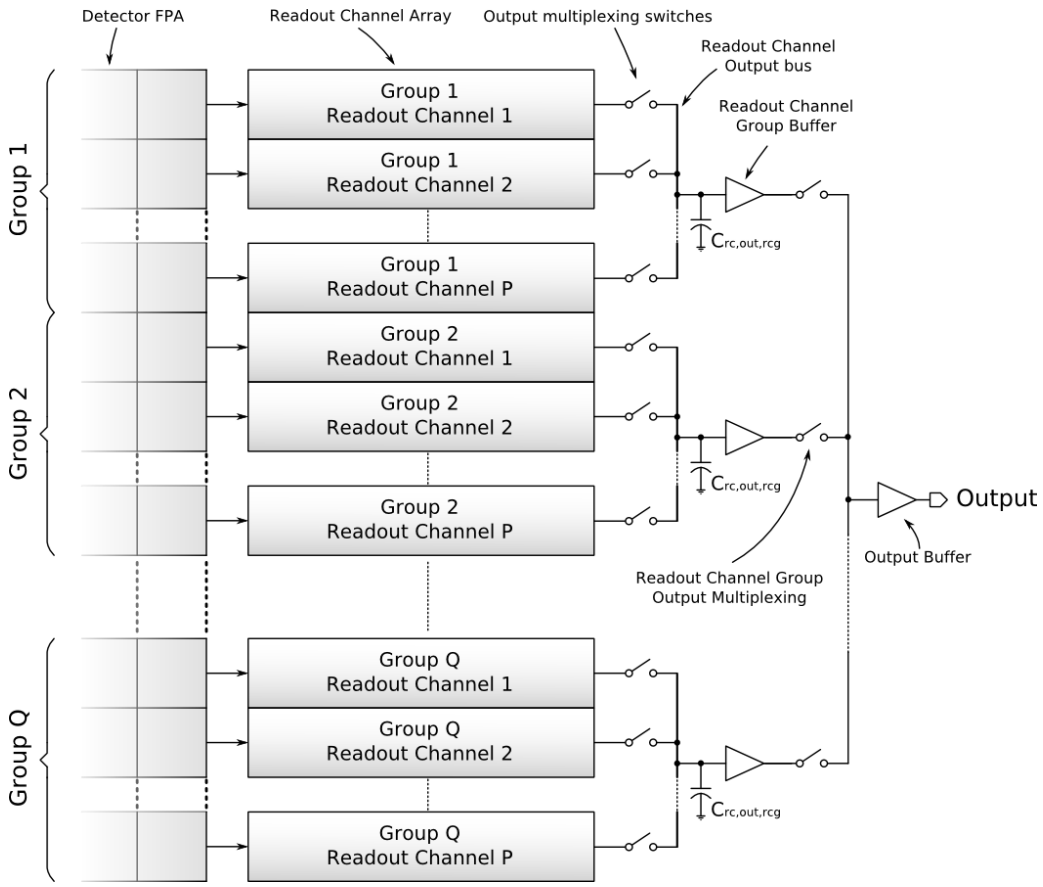


Figure 2.3: Simplified block diagram of a readout circuit with Q different RCGs and single output channel [46].

Figure 2.4 shows the approximate common bus capacitance for different number of RCGs in a 384x288 FPA with 35 µm pixel pitch, a 640x480 FPA with 25 µm pixel pitch, and a 1024x768 FPA with 17µm pixel pitch fabricated in a standard 0.6 µm CMOS process. These values are calculated using the typical parasitic capacitance values given in the process specification file of the process.

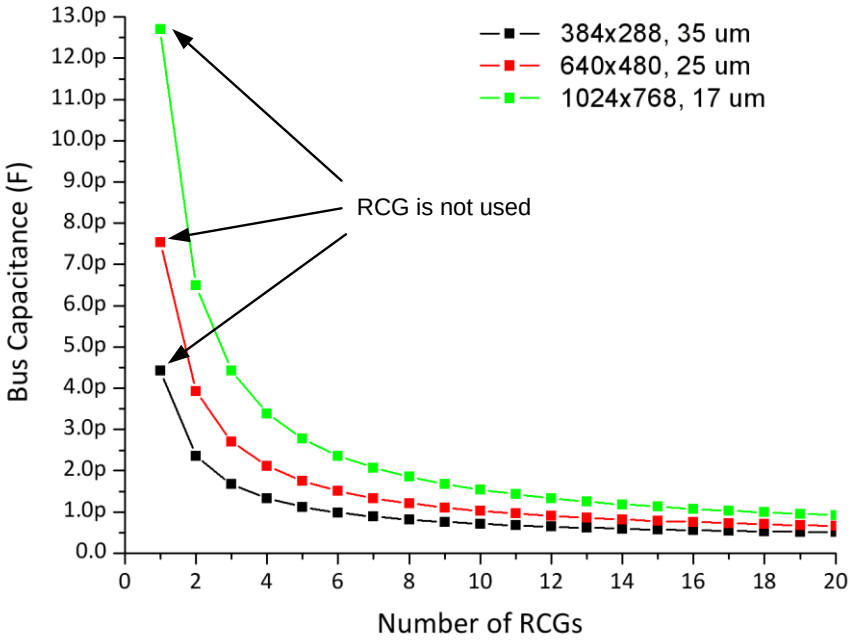


Figure 2.4: Approximate common bus capacitance for different number of RCGs in a 384x288 FPA with 35 µm pixel pitch, a 640x480 FPA with 25 µm pixel pitch, and a 1024x768 FPA with 17µm pixel pitch fabricated in a standard 0.6 µm CMOS process. All arrays are assumed to have readout channels at both sides of the detector array and number of RCGs is given for each readout channel array.

As the common bus capacitance decreases, the necessary readout channel output current, and consequently the power dissipation, is reduced. Nevertheless, adding an extra stage to the signal path causes an increase in the overall delay; and therefore, the reduction in the necessary output current is not directly proportional to the reduction in the bus capacitance. In order to maximize the available signal settling time, opamps with high output current capability should be used as RCG buffers. As a result, the buffers can have significant contribution to the total power dissipation of the output buffering structure, which can be expressed as

$$P_{buf,t} = Y \cdot P_{rc} + Q \cdot P_{buf,rcg} \quad (2.5)$$

where Y and P_{rc} are the number and the power dissipation of the readout channels, respectively; Q is the number of RCGs, and $P_{buf,rcg}$ is the power dissipated by each RCG buffer. The number of RCGs should be chosen such that the total power dissipation of the output buffering structure is minimized.

2.2.3 Sample and Hold Opamp with Digitally Programmable Output Current Capability

The sample-and-hold (S&H) block of the readout channels perform two main tasks. The first one is sampling and storing the integrator output, and the second one is driving the output buffer in order to send the data outside of the chip. Simple S&H circuits consisting of a CMOS switch and a capacitor can do the first task; however, the signal would be corrupted during output multiplexing due to capacitive charge sharing between the sampling and bus capacitances. In order to prevent the corruption of the signal, more advanced S&H circuits that employ opamps are used in the readout channels. Figure 2.5 shows the schematic of a well known S&H structure which can perform both tasks without corrupting the sampled signal [53]. The circuit samples the voltage at the input during phase ϕ, and stores the sampled voltage after ϕ goes low. Any current drawn from the output of S&H is provided by the opamp; and therefore, the sampled voltage remains unchanged.

As stated in Section 2.2.1, the output multiplexing duration is very short in large format FPAs, necessitating a high output current for the S&H opamp. On the other hand, sampling operation can be performed with much lower output current since the sampling duration is typically much longer than the output multiplexing time. Besides, the sampled voltage can be stored as long as the

opamp provides sufficient open loop gain, which can also be achieved by a low quiescent current. As a result, using a standard opamp with constant supply current causes inefficiency in the power dissipation. Instead, an opamp with digitally controllable current sources can be used in order to increase the power efficiency. Such an opamp can be implemented by adding controllable current sources to the standard opamp topologies. In this study, the folded cascode topology is chosen since it is very suitable for switched capacitor applications [53]. Figure 2.6 shows the schematic of the designed folded cascode opamp structure with digitally programmable current modes developed at METU [46]. The opamp stays in its low current mode during sampling and storing operations, and switched to its high current mode during output multiplexing.

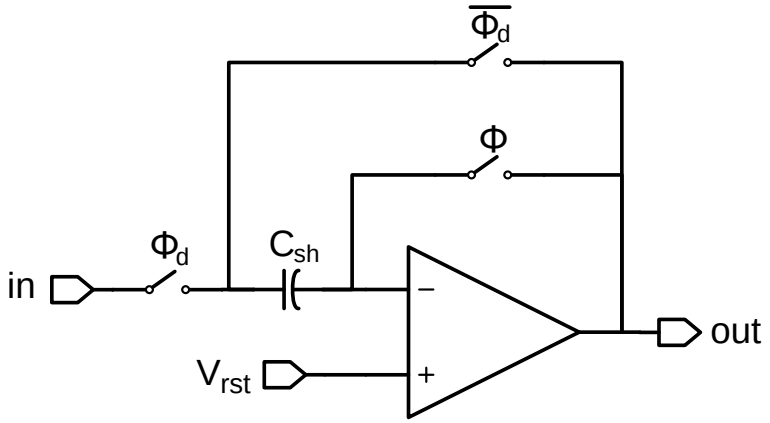


Figure 2.5: Schematic of a well known S&H structure which can perform both sampling and driving loads without corrupting the sampled signal [53].

The average power dissipation of the proposed opamp structure can be expressed as

$$P_{avg} = (V_{DD} - V_{SS}) \cdot \frac{t_{low} \cdot I_{low} + t_{high} \cdot I_{high}}{t_{low} + t_{high}} \quad 2.6$$

where t_{low} and t_{high} are the durations of the low and high current modes, respectively; and I_{low} and I_{high} are the currents drawn from the supply during the low and high current modes, respectively. In typical applications, t_{high} is much lower than t_{low}; therefore, the average supply current will be close to I_{low}, which can be very small.

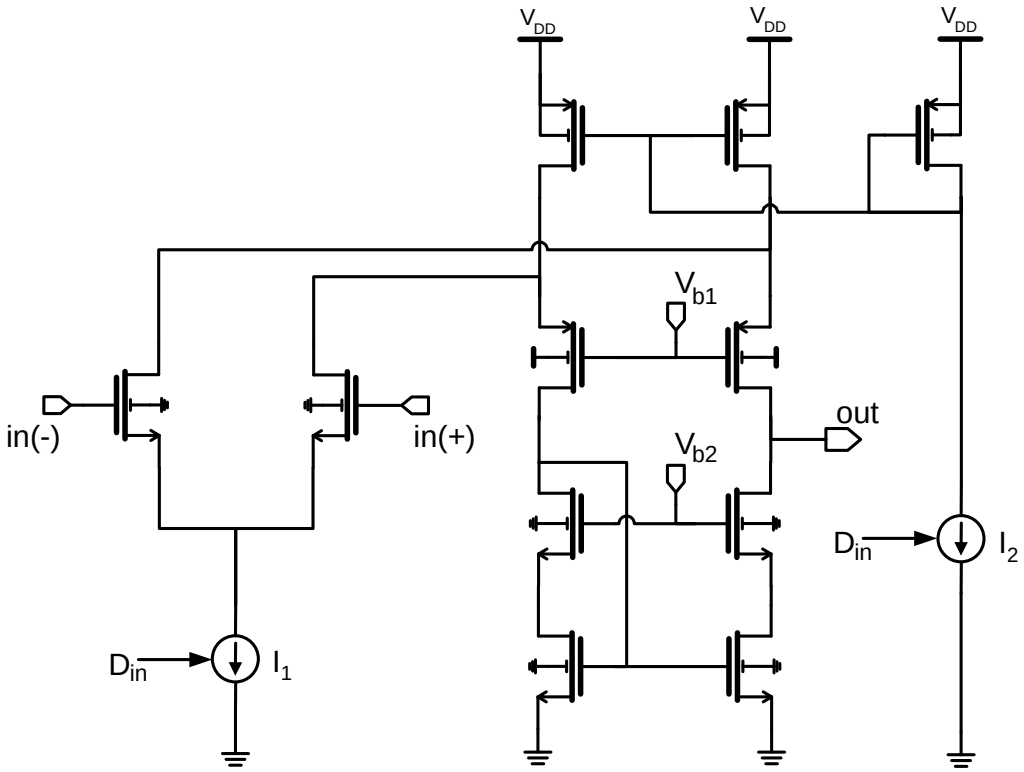


Figure 2.6: Schematic of the designed folded cascode opamp structure with digitally programmable current modes. The low and high current modes are selected by applying digital input bit D_{in} to the programmable current sources [46].

The proposed two-mode opamp structure has some issues related to the changing DC operation point. The most important issue is the offset voltage at the output when the opamp mode switches from low to high during output multiplexing. This offset is caused by the change in the overdrive voltages of the input transistors. Figure 2.7 shows the input terminals of the two mode sample and hold opamp during the hold mode. During sampling, the opamp is in the unity gain buffer mode, which implies $V_a = V_b = V_{rst}$ if the gain error is neglected. After the sampling is completed, the node a remains floating; and therefore, the charge amount at that node is frozen. When the opamp switches to the high current mode, V_c drops in order to increase the currents of the input transistors. As a result, the voltage stored at the gate-source capacitances of the input pair increases. The necessary charge is provided by the low impedance voltage source at the node b; however, since the node a is floating, the charge is taken from the sampling capacitance, reducing its voltage. The amount of the offset can be expressed as

$$V_{offset} = (V_{GS,a,high} - V_{GS,a,low}) \cdot \frac{C_{GS,a}}{C_s} \qquad 2.7$$

where $V_{GS,a,high}$ and $V_{GS,a,low}$ are the gate-to-source voltages, and $C_{GS,a}$ is the gate-to-source capacitance of the input transistor at the inverting terminal of the opamp, and C_s is the sampling capacitance.

There are two methods to cancel the output offset caused by the change of the overdrive voltage. The first one is switching the opamp to high current mode during the sampling operation. In this case, the DC voltages at the terminals of the input transistors would be same during the sampling and output multiplexing; and therefore, the offset is completely removed. However, this method increases the duration of the high current mode, causing a higher

power dissipation. The other method is correcting the voltage after reading the data from the chip. Since the opamp is always switched between the two same modes, the value of the offset voltage is independent of the input. Therefore, it can be considered as a part of fixed pattern noise (FPN) of the chip, which is removed by nonuniformity correction methods. As a result, the second method is more preferable since it does not require any extra operations.

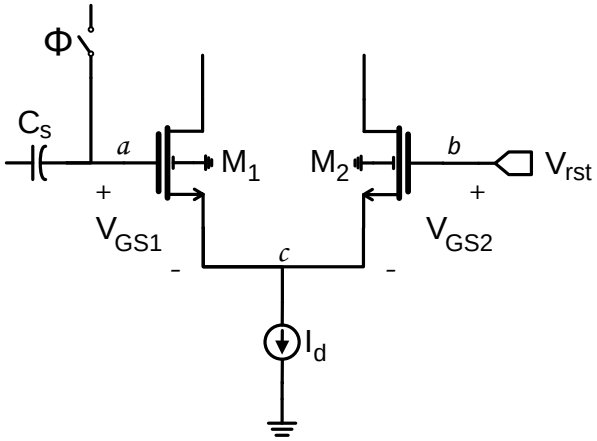


Figure 2.7: Input terminals of the S&H opamp during the hold mode. The labels ***a***, ***b***, and ***c*** show the gates and the common source node of the input transistors, respectively.

Another point is the changing opamp parameters like gain or phase margin when the current mode is switched. It must be ensured that the opamp has sufficient gain to suppress the gain error, and its phase margin provides a stable operation for both high and low current modes. Finally, the mode transition should be performed earlier than the output multiplexing time in order to allow the transients decay to an acceptable level.

2.3 Improved Bias Correction DAC

As explained in Section 1.4 and Section 1.5, bias correction is necessary for large format microbolometer FPAs in order to prevent the saturation of the readout and increase the dynamic range. The on-chip DACs used for bias correction have significant contribution to the power dissipation and the area of the readout, which are important performance parameters [26]. Therefore, reducing the area and the power of the bias correction DACs significantly improves the overall performance of the readout.

This section presents an improved bias correction DAC with low power dissipation and small area. First, Section 2.3.1 gives the DAC structure previously used in large format FPAs designed at METU to explain its drawbacks and its difference compared to the new DAC. Then, Section 2.3.2 introduces the improved bias correction DAC, while its power dissipation and noise performance is examined in Section 2.3.3.

2.3.1 Previously Used Bias Correction DAC Structure in the Large Format FPAs Designed at METU

In the 320x240 resistive microbolometer previously designed at METU, 9-bit, R-2R type on-chip bias correction DACs have been used. Figure 2.8 shows the simplified schematic of the bias correction structure of this chip. In this structure, four readout channels share a single DAC due to the area and power limitations. The bias data of each readout channel is stored in a separate RAM, and transferred to the DAC sequentially. After the data is transferred, the injection transistor in the corresponding readout channel is connected to the DAC output, and the voltage is sampled at the gate of the transistor. The same procedure applies to all four readout channels.

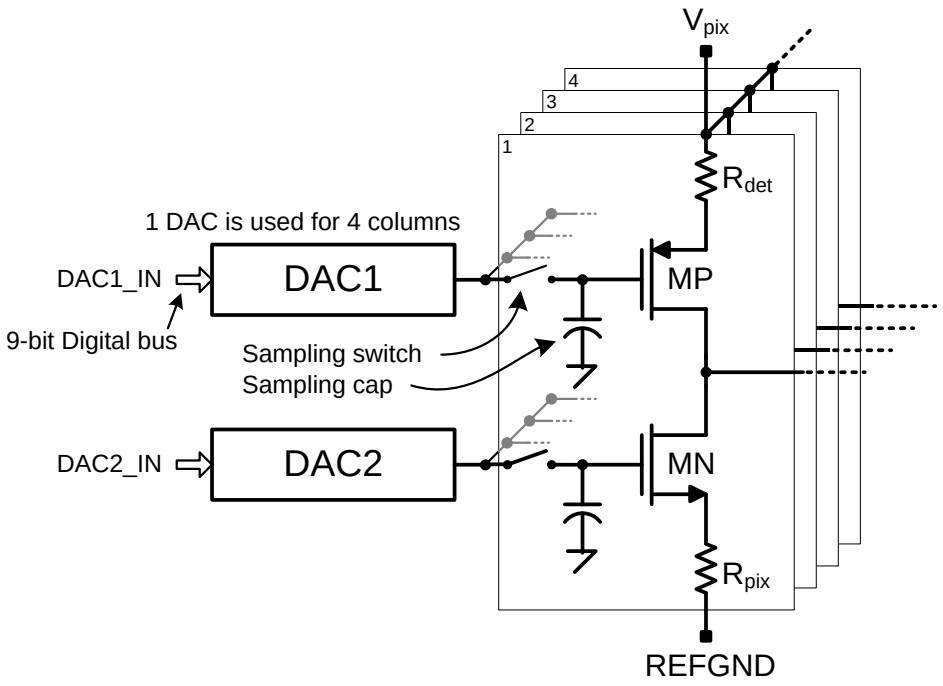


Figure 2.8: Simplified schematic of the bias correction structure used in the 320x240 resistive microbolometer FPA previously designed at METU.

This structure has some certain drawbacks. First of all, the noise in the bias voltage within the integration bandwidth is increased due to the noise shaping of the sampling operation. The circuit configuration at the gate of the injection transistor can be modeled with a simple RC circuit where R represents the equivalent resistance of the DAC, and C represents the gate capacitance. Figure 2.9 shows the noise power spectral density (PSD) of an RC circuit with and without the sampling operation. The total noise power of the circuit is equal to kT/C regardless of the sampling operation, where k is the Boltzmann constant, T is the absolute temperature, and C is the capacitance value. However, the sampling operation concentrates the noise into a bandwidth of $f_s/2$, where f_s is the sampling frequency [54]. Since the bias voltage is sampled before each integration operation, the sampling and integration periods are close to each other. Therefore, the noise bandwidth of the sampled voltage is approximately

equal to the integrator bandwidth. As a result, the entire noise power remains in the signal bandwidth. The only method to decrease the noise in the bias voltage is increasing the capacitance at the gate of the injection transistor. This method is used in previous designs by adding an extra capacitor to the DAC output node; however, this approach increases the time constant, and hence, the required time for the biasing operation.

Another problem is the power dissipation of this structure. Figure 2.10 shows the schematic of an n-bit R-2R type DAC operating between the voltages V_H and V_L. In this structure, any high state input connects the corresponding switch to V_H and creates a resistive path between the two supplies. The equivalent resistance seen from each bit is different; therefore, the power dissipation depends on the number and significance of the bits that are in high state.

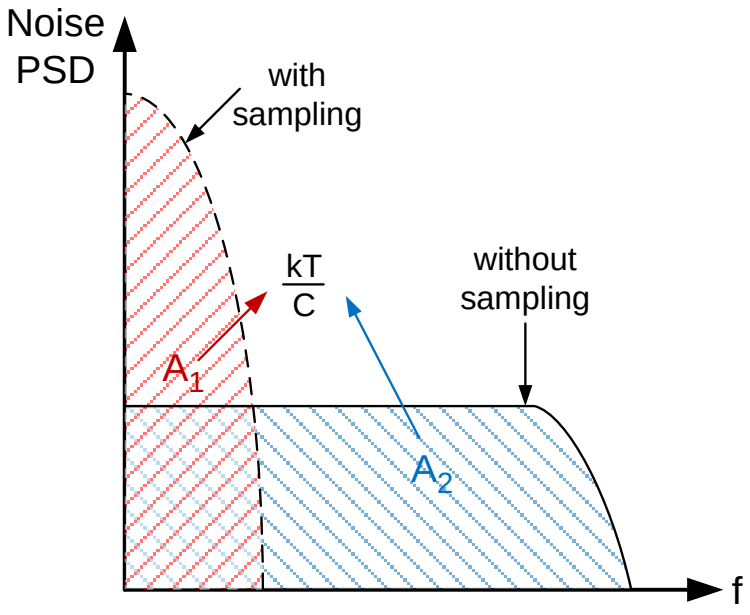


Figure 2.9: Noise power spectral density (PSD) of an RC circuit with and without the sampling operation. The total noise power is equal to $\boldsymbol{kT/C}$ for both cases; however, the noise bandwidths are different.

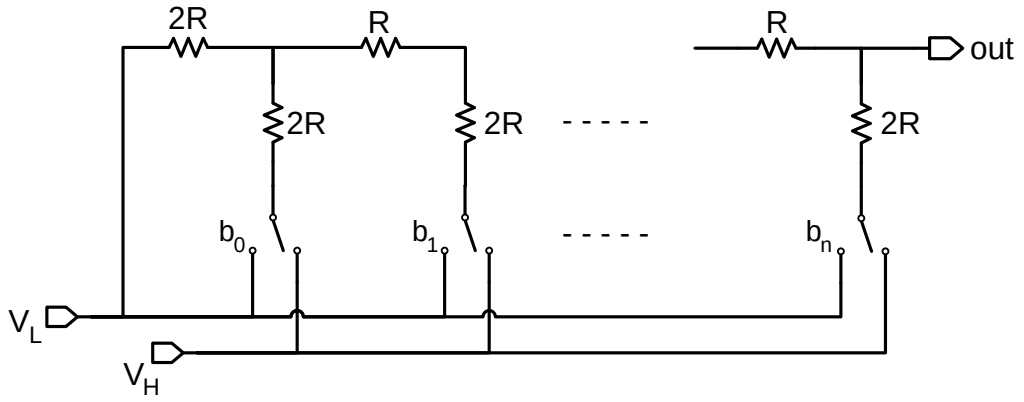


Figure 2.10: Schematic view of an n-bit R-2R type DAC operating between the voltages V_H and V_L. Here b_n is the most significant bit and b_0 is the least significant one.

Table 2.4 shows the variation of the equivalent resistance seen from the input nodes of a 9 bit R-2R DAC. As the table indicates, the power dissipation is minimum for the most significant bit (MSB), and it increases towards the least significant bit (LSB). The maximum power dissipation of a 9-bit R-2R DAC is approximately equal to

$$P_{max} = \frac{2.89 \cdot (V_H - V_L)^2}{R} \qquad 2.8$$

where R is the unit resistance. The maximum total power can be calculated by multiplying this value with the number of the implemented DACs. The previously designed 320x240 FPA readout used one readout channel for each column, and one bias correction DAC for four readout channels. Consequently, the total number of the bias correction DACs was 80, resulting in very high power dissipation values. In this structure, the power dissipation can be reduced by either decreasing the operation range or increasing the unit

resistance. However, both methods have limitations. The operation range must include the maximum and minimum possible bias voltages for the injection transistors. Besides, even if the operation range is decreased, V_H and V_L should still be obtained from the supply voltage. Therefore, this method just transfers the power dissipation from DACs to voltage reference blocks. The DAC resistance forms a time constant with the equivalent capacitance at the transistor gate; therefore, its value should be small enough to enable the settling of the voltage during the sampling operation. It has already been mentioned that extra capacitances are added to injection transistor gates in order to decrease the noise, which necessitates the use of smaller unit resistance.

Table 2.4: Equivalent resistance seen from the input nodes of a 9-bit R-2R DAC. The resistance is given in terms of unit resistance R.

Bit Number	***Equivalent Resistance (R)***
MSB - 1	4.00
2	3.20
3	3.05
4	3.01
5	3.00
6	3.00
7	3.00
8	3.00
LSB - 9	3.00

The third problem of the previously used bias correction DAC structure is the non-guaranteed monotonicity. The non-zero switch resistances and resistor

nonuniformity due to process variations may cause non-monotonic output characteristic in R-2R DACs. To give an example, in a 9-bit R-2R DAC, if the resistor connected to the MSB switch does not have a resistance of exactly 2R and all the other parameters are ideal, the deviation at the output voltage for an input of $(100000000)_2$ is equal to

$$\Delta V = V_{ideal} \cdot \left(\frac{-\Delta R}{\Delta R + 4R}\right) \quad 2.9$$

where V_{ideal} is the ideal output voltage, and ΔR is the resistance difference between the actual and ideal values of the resistor connected to the MSB switch. If ΔR is greater than $0.0156R$, which corresponds to 0.78% mismatch, the output voltage will decrease although the input increases from $(011111111)_2$ to $(100000000)_2$. The possibility for such small mismatch values is quite high unless special layout techniques are applied; therefore, it is hard to avoid non-monotonic output characteristic in this structure.

2.3.2 Improved Bias Correction DAC Structure*

The improved bias correction DAC structure implemented in this thesis has low noise, low power dissipation, and naturally monotonic output characteristic; therefore, it provides solutions to the problems of the previous structure discussed in the previous section. The improved structure uses resistive ladder type DACs which are naturally monotonic, providing a direct solution for the non-monotonic output problem. Besides, it is possible to obtain multiple outputs from a single resistive ladder, which enables multiple readout channels to share the same resistive ladder, reducing the overall area and the total power

* This structure is developed together with Murat Tepegöz.

dissipation of the structure [55]. With reduced area and power dissipation, it is possible to implement a dedicated DAC for each readout channel, and hence to eliminate the need for sampling operation. Elimination of the sampling is crucial in terms of noise since this operation concentrates the noise into the integrator bandwidth as explained in the previous section. Without sampling, the noise bandwidth will be much larger than the integrator bandwidth for typical applications; and therefore, most of the noise will be filtered out by the integrator.

Figure 2.11 shows the block diagram of the improved bias correction DAC structure. The structure is composed of two stages; the first stage is common for the entire readout channel array and the second stage generates distinct bias values for each readout channel. The second stage has also two parts; first one generates the bias voltages and it is shared by all readout channels within the same RCG, while the second part is used to select the appropriate voltage for a particular readout channel. The following sections describe the parts of the bias correction structure.

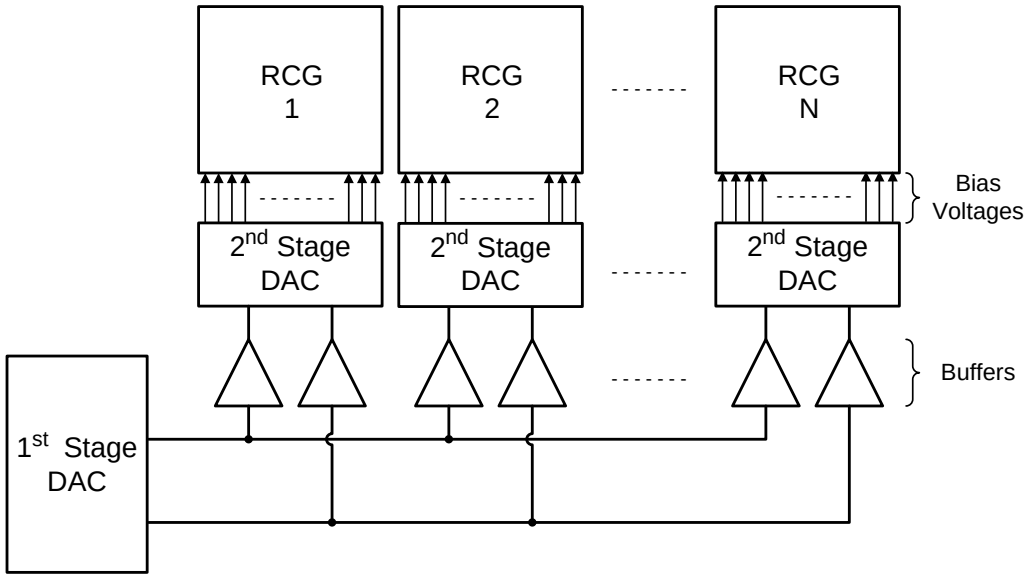


Figure 2.11: Block diagram of the improved bias correction DAC structure, which is composed of two stages. The first stage is common for the entire readout channel array, and the second stage generates distinct bias values for each channel.

2.3.2.1 First Stage of the Bias Correction Structure

Figure 2.12 shows the simplified schematic of the first stage DAC, which is an n-bit resistive ladder DAC with two outputs that are used to determine the output range of the DACs in the second stage.

The two outputs of the first stage DAC are adjusted according to the minimum and maximum values of the required pixel bias voltages, and they are connected to the high and low bias voltages of the second stage DACs through buffers. It is also possible to connect the outputs directly to the resistive ladders since the capacitive load of the injection transistor gates do not draw DC current; however, it is not practical due to the very large time constants. The static output values and capacitive-only load greatly reduces the current capability requirements; therefore, only one or two DACs are sufficient for the first stage.

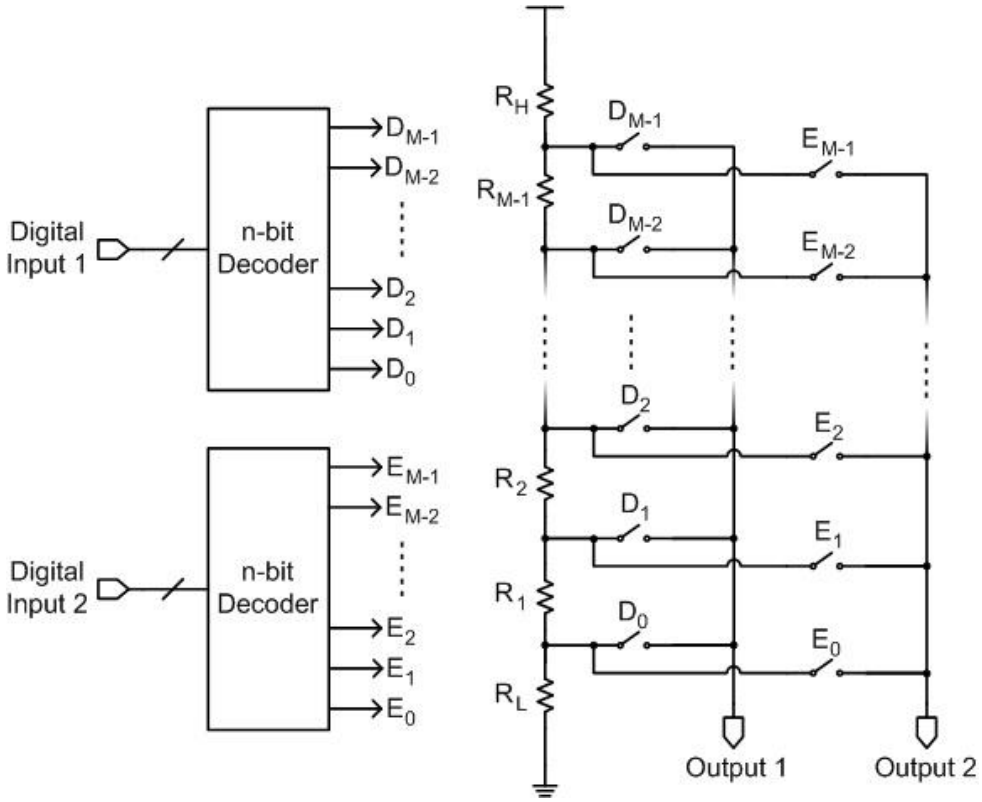


Figure 2.12: Simplified schematic of the first stage DAC, which is an n-bit resistive ladder DAC with two outputs that is used to determine the output range of the DACs in the second stage. There are (M-1) unit resistors in the resistive ladder, where $M = 2^n$. The other two resistors, R_L and R_H are used to adjust the output range.

2.3.2.2 Second Stage of the Bias Correction DAC

The second stage of the bias correction structure is a resistive ladder DAC with multiple outputs, and it is composed of two parts: The voltage generation block and in-channel decoder-switch networks (DSN). The voltage generation block generates the bias voltages to be applied to the gates of the injection transistors. The generated voltages are routed into the readout channels, and in-channel DSNs are used to connect the desired voltage to the gate of the injection transistors.

Figure 2.13 shows the schematic of the voltage generation block of the second stage, which is a resistive ladder connected between the outputs of two buffer connected opamps. The voltage generation block can be shared by multiple readout channels by implementing a separate DSN for each output. With this method, the total area and power dissipation of the bias correction structure can be greatly reduced [55]. The number of readout channels that can be connected to the same voltage generation block is limited by the settling time at the output. Unlike the first stage, the second stage DACs have rapidly changing outputs, and it should be ensured that the bias voltages are settled before the integration period. The output current capability of the buffers, the unit resistance value of the resistive ladder, and the total capacitance at the output are the parameters that affect the settling time. Grouping the readout channels and using a separate resistive ladder for each group reduce the capacitance at the output node, and consequently, reduce the time constant. This is the same idea leading to the RCG concept described in Section 2.2.2; therefore, the RCGs can be used as the units that will share the same voltage generation block.

Figure 2.14 shows the simplified schematic of a DSN, which is composed of an n-bit decoder and 2^n switches and implemented into each readout channel. The switches are connected between the outputs of the voltage generation block and the gate of the injection transistor. According to the n-bit input applied to the decoders, the corresponding switch is closed, connecting the gate of the injection transistor to the desired voltage. The DSNs dissipate power only during the change of the decoder inputs; therefore, they do not have significant contribution to the power dissipation of the overall structure. The power dissipation and the noise performance of this improved bias correction structure are addressed in the next section.

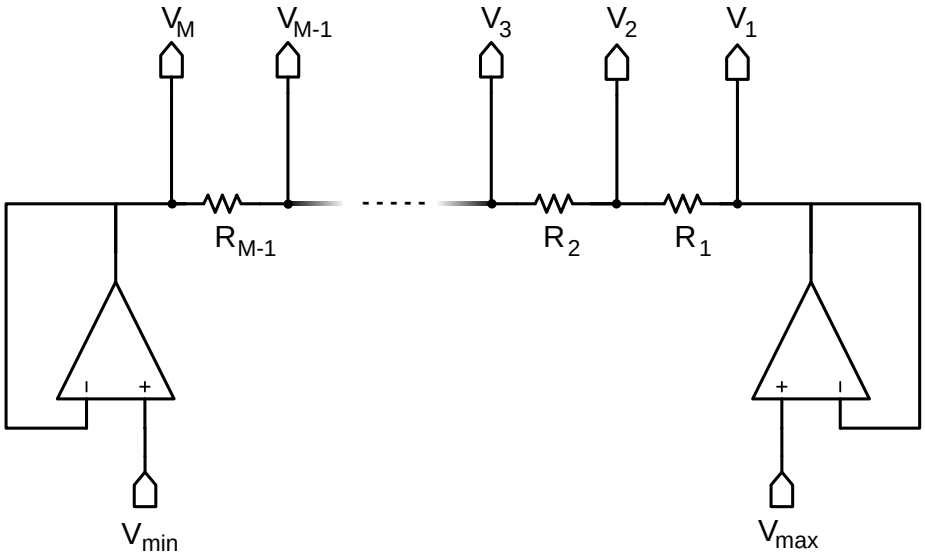


Figure 2.13: Schematic of the voltage generation part of the second stage of the bias correction structure.

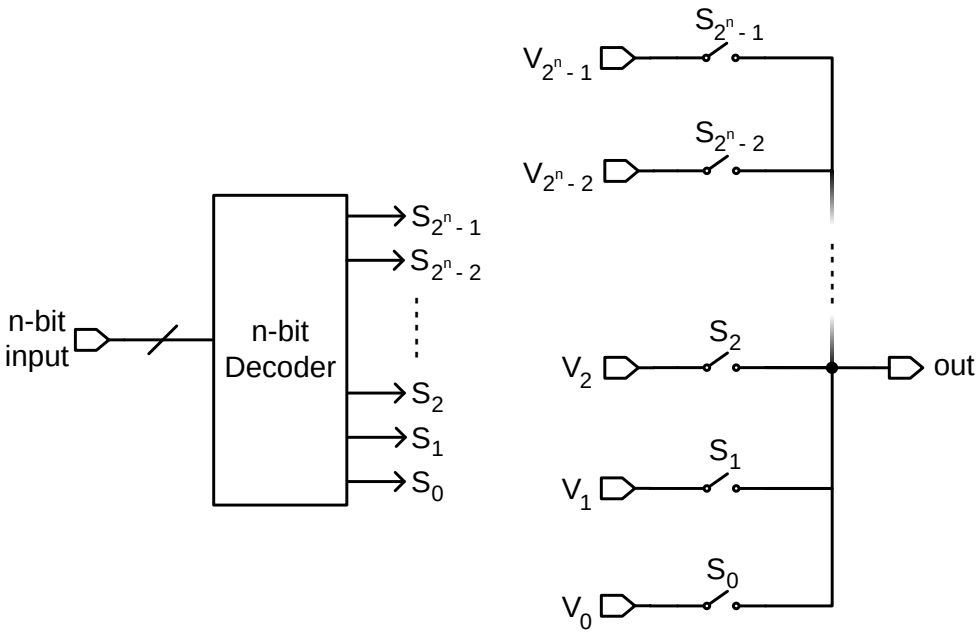


Figure 2.14: Simplified schematic of a DSN, which is composed of an n-bit decoder and $\mathbf{2^n}$ switches, and implemented into each readout channel. According to the decoder input, the corresponding switch connects the desired voltage to the output node, which is connected to the gate of the injection transistor.

2.3.3 Power Dissipation and Noise Performance of the Improved Bias Structure

The power dissipation of the improved bias correction structure can be expressed as

$$P_{total} = Y \cdot \frac{{V_{DD}}^2}{R_{fs}} + 2 \cdot Q \cdot P_{buf} \quad (2.10)$$

where Y is the number of the readout channel arrays (typically 1 or 2), V_{DD} is the supply voltage, R_{fs} is the total resistance of the first stage DAC, Q is the number of RCGs, and P_{buf} is the average power dissipated by a single buffer that is used to bias the resistive ladders in the second stage. P_{buf} depends on the opamp topology and the required output current to bias the resistive ladder and to drive the capacitance at the DAC output. Therefore, the power dissipation can be reduced by increasing the unit resistance used in the resistive ladders. However, increasing the resistance also increases the settling time and the noise; therefore, an optimization between the power dissipation, speed, and noise is necessary during the design of the second stage DACs.

The noise of the bias correction structure is very critical since it directly adds up to the detector current through the transconductance of the injection transistor. The total voltage noise power at the output of the bias correction structure can be expressed as

$${v_{n,BCS}}^2 = \int_0^{BW_{int}} ({v_{n,FS}}^2 + {v_{buf}}^2 + {v_{n,SS}}^2 + {v_{n,DSN}}^2) \quad (2.11)$$

where BW_{int} is the integrator bandwidth, ${v_{n,FS}}^2$ is the noise power due to the resistive ladder of the first stage DAC, ${v_{buf}}^2$ is the noise power of a single buffer, ${v_{n,SS}}^2$ is the noise power due to the resistive ladder of the second stage DAC, and ${v_{n,DSN}}^2$ is the noise power due to the decoder-switch network. The last term may be ignored since the switch resistance is typically very low compared to the resistance of the DACs. ${v_{n,FS}}^2$ and ${v_{n,SS}}^2$ depend on the equivalent resistance seen from the buffer input and transistor gate, respectively; therefore, these values are input-dependent. In order to decrease the noise contribution of the bias correction structure, the unit resistance values of the resistive ladders should be chosen as low as possible, and the buffer opamps should have a low noise.

2.4 Test Results of the Advanced Low Power Readout Architecture

The proper operation of the output buffering architecture and digitally controllable opamp had been verified by the test circuits fabricated in an MPW run before the design of the ROIC for the 384x288 array, which is described in Chapter 3. However, the improved bias correction DAC structure is developed during the design of the ROIC. Nevertheless, test circuits for both structures are placed on the same wafer with the 384x288 FPA ROIC, and this section presents the test results of these latest circuits.

The main aim of the performed tests is to verify the proper operation of the readout channel and to observe the improvement in the power dissipation. In order to perform the tests, three 4-layer PCBs have been used; two for the low power readout and the improved DAC, and one for generating the analog bias voltages. Required digital signals are generated using a Xilinx FPGA card.

2.4.1 Test Results of the Low Power Sampling and Buffering Structure

Figure 2.15 shows the simplified schematic of the low power sampling and buffering structure test circuit, which includes the whole signal path of a single readout channel output. The circuit includes a CTIA type preamplifier followed by a RCG and an output buffer. Using the switches, it is possible to test different parts separately or change the output load of the blocks. The integrator and S&H outputs are normally internal signals; therefore, internally placed buffer opamps (*aopac07*, IP of X-FAB Semiconductor Foundries) are used to observe the outputs of these blocks. On the other hand, the outputs of the RCG and output buffers are directly connected to bond pads, since they have high output driving capability when compared to the preceding blocks. Nevertheless, the RCG and output buffers are designed to drive only capacitive loads; and consequently, their outputs should be buffered by an external opamp with sufficient speed.

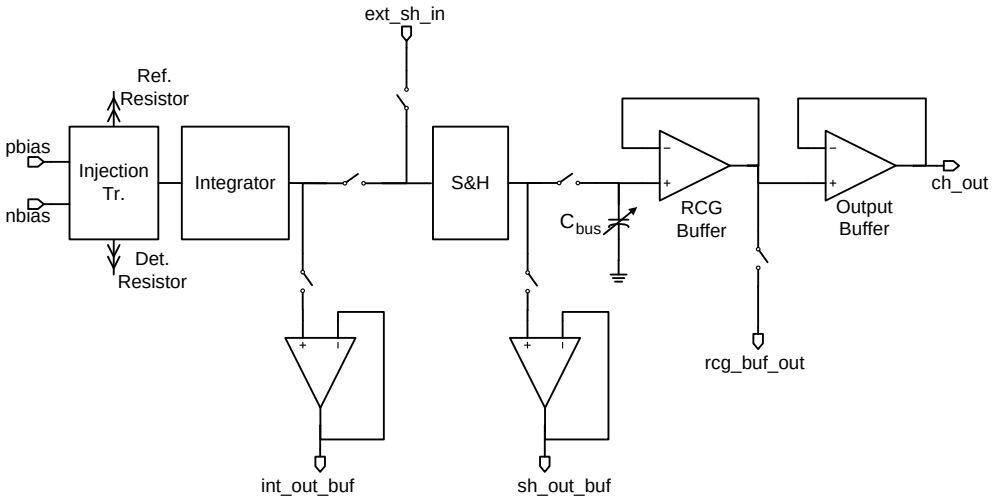


Figure 2.15: Simplified schematic of the low power sampling and buffering structure test circuit, which includes the whole signal path of a single readout channel output.

The test circuit for low power sampling and buffering architecture is fabricated in a standard 0.6 µm process, and occupies an area of 4.5 mm x 0.9 mm. Figure 2.16 shows the layout and Figure 2.17 shows the photograph of the fabricated test circuit, which occupies an area of 4.5 mm x 0.9 mm in a standard 0.6 µm CMOS process and has 51 I/O pads.

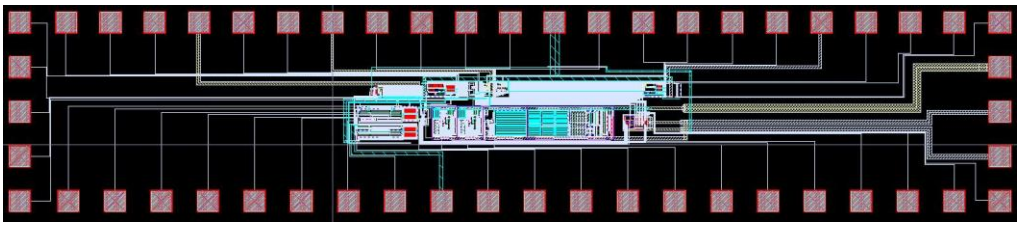


Figure 2.16: Layout of the test circuit designed to test the low power sampling and buffering architecture, which occupies an area of 4.5 mm x 0.9 mm in a standard 0.6 µm CMOS process and has 51 I/O pads.

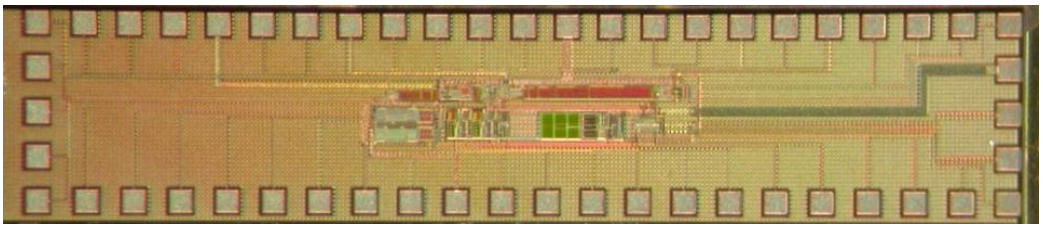


Figure 2.17: Photograph of the fabricated test circuit designed to test the low power sampling and buffering architecture, which occupies an area of 4.5 mm x 0.9 mm in a standard 0.6 µm CMOS process and has 51 I/O pads.

Figure 2.18 shows the photograph of the prepared test setup, which includes three PCBs and a breadboard. The leftmost PCB carries the Xilinx XSA-3000 FPGA, which is used to generate the digital signals. The breadboard is used to place the two 74HC541 octal digital buffers, which are used to convert the 3.3 V outputs of the FPGA to 5 V, which is the digital supply voltage of the circuit. The

test circuit is placed on the PCB next to the breadboard together with the control switches. The test PCB also includes an AD8062 dual video buffer opamp in order to buffer the outputs of the RCG and output buffers, which has high slew rate (650 V) and fast small signal settling time (35 ns for 0.1% settling) [56]. Finally, the rightmost PCB is used to generate the required analog bias voltages.

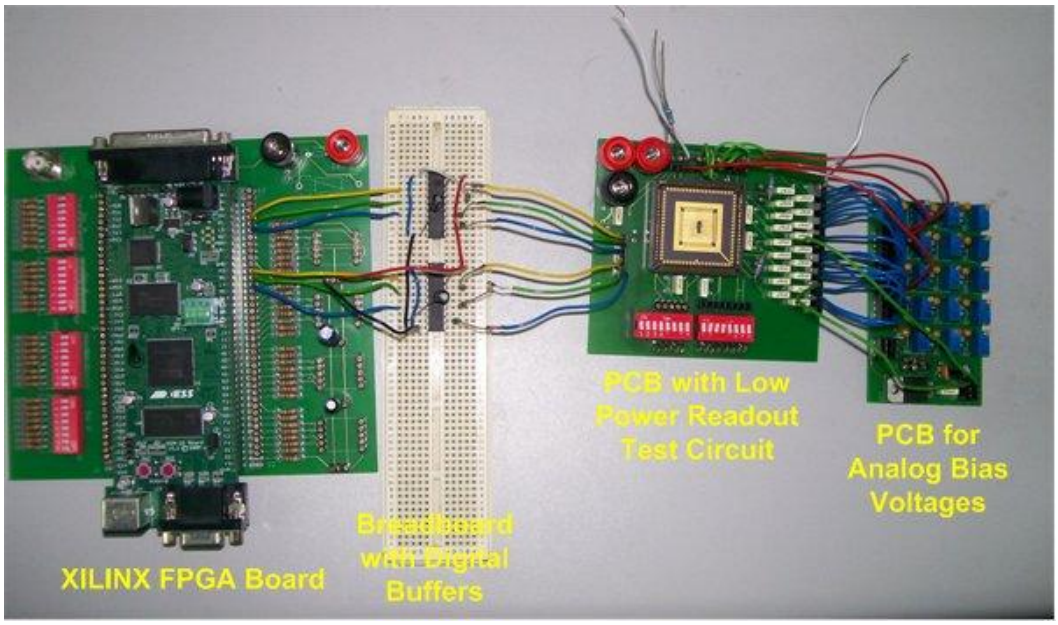


Figure 2.18: Photograph of the prepared test setup for the low power readout circuit, which includes three PCBs and a breadboard.

2.4.1.1 Verifying the Proper Operation of the Blocks

The first test is performed to verify proper operation of all circuits on the signal path. For this purpose, two 60.4 kΩ metal film resistors are connected to the injection transistors as detector and reference resistors; and the resultant current is processed by the readout channel. Figure 2.19 shows the outputs of the integrator, S&H block, RCG buffer, and the output buffer, indicating that all blocks in the test circuit are working properly.

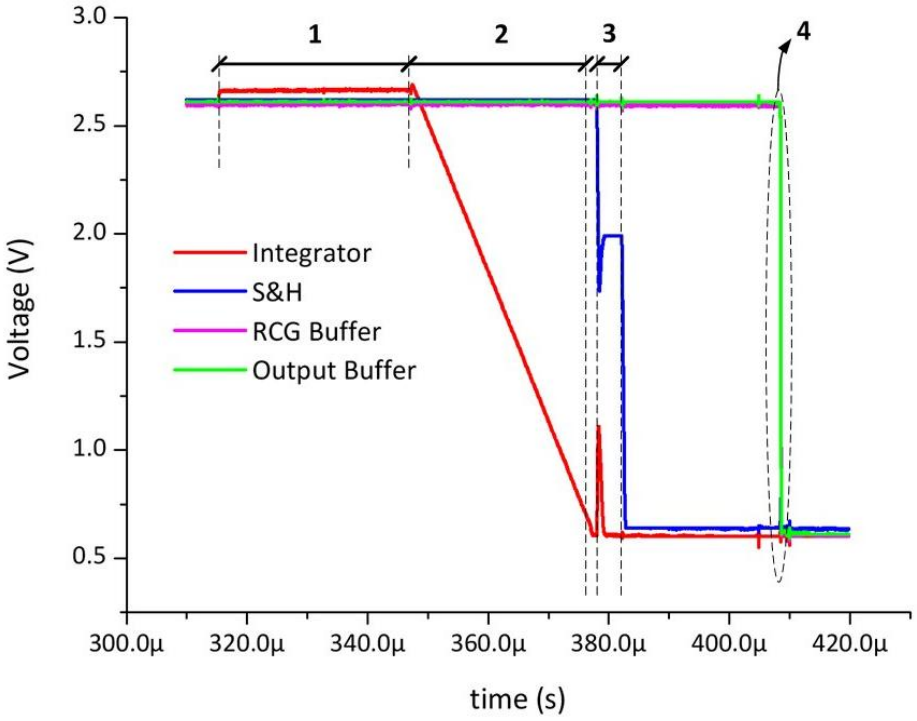


Figure 2.19: Outputs of the integrator, S&H, RCG and output buffers of the low power readout test circuit. The different phases of the readout are shown by labels as: 1. Integration reset, 2. Integration enable, 3. Sampling, and 4. Output multiplexing.

2.4.1.2 Effect of RCG Concept on Power Dissipation

After verifying that all blocks are working as expected, the effect of the readout channel group concept on the power dissipation is examined. In order to see the effect, the integrator output is sent to the output through two different paths, which are shown in Figure 2.20. The first path resembles the conventional buffering scheme; it has high S&H output load capacitance and the output is taken from the RCG buffer, whose output current capability is adjusted to drive the video buffer. The second path on the other hand, has a lower S&H output load; however, the output is taken from the output buffer, adding one extra stage as in the RCG case.

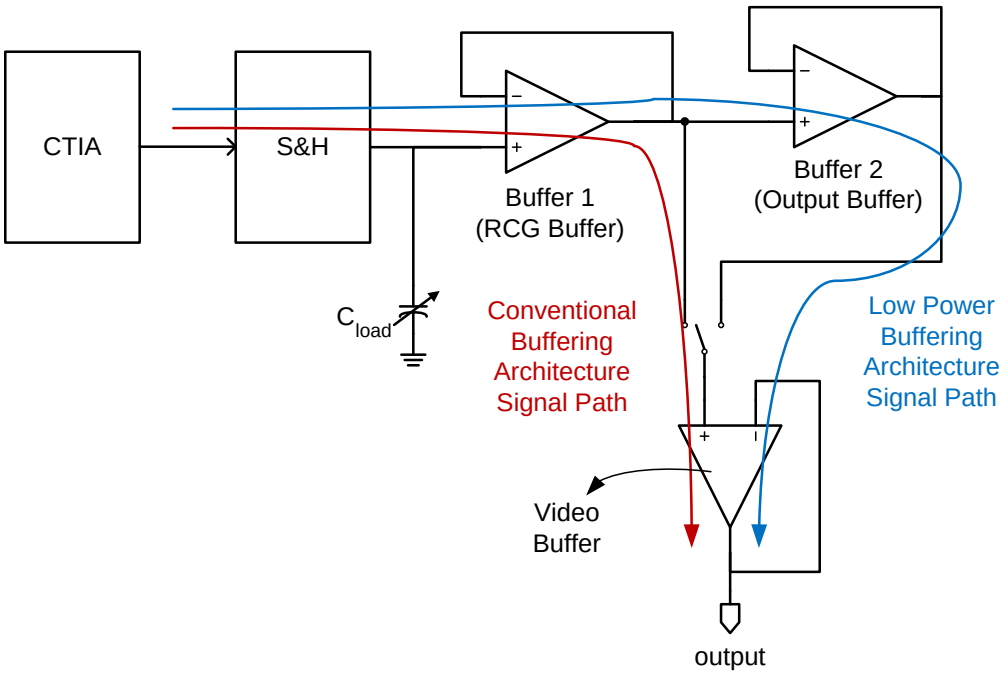


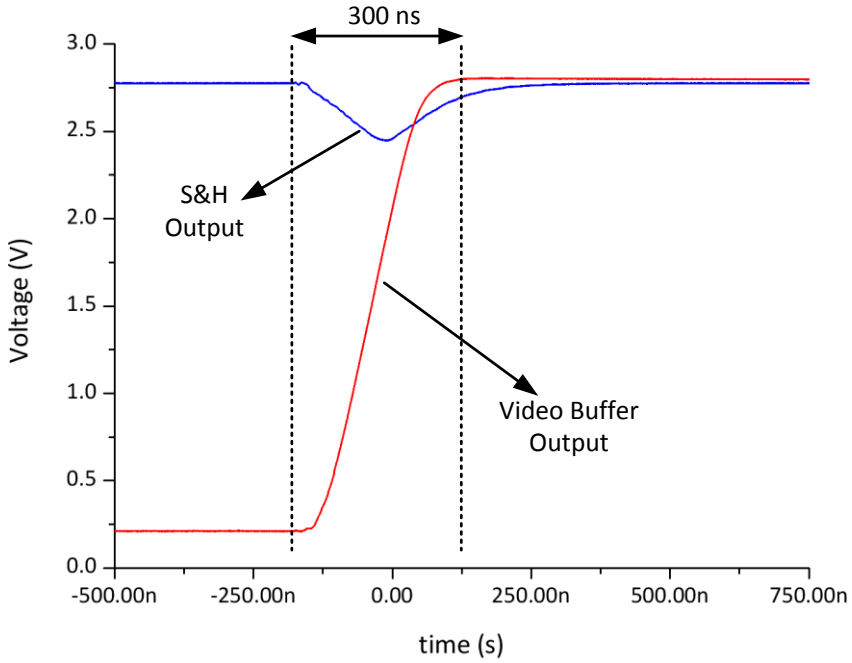
Figure 2.20: Signal paths used during the low power readout test in order to resemble the conventional and low power buffering architectures.

In an FPA readout, consecutive readout channels may have very different outputs, which is the worst case in terms of output settling. In order to resemble this case, two different integration durations are used. The bias voltages of the opamps are adjusted such that the output voltage settles within the same duration for both cases, and the corresponding currents are measured to calculate the power dissipation.

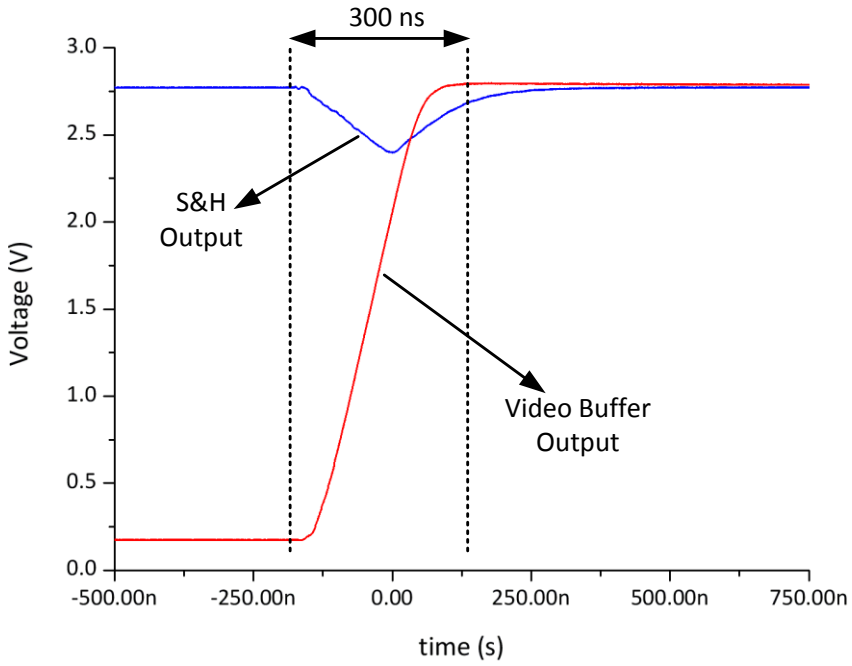
The bus capacitance values are chosen from Figure 2.4 for a 384x288 FPA with 35 µm pixel pitch. The S&H output loads are approximately equal to 4.5 pF and 0.8 pF for 0 and 8 RCGs, respectively. During the test, the loads are applied as 5.0 pF and 1.0 pF, which are sufficiently close to the calculated values. The output multiplexing time of a 384x288 FPA with two output channels operating at 50 fps is 360 ns, and the opamp bias voltages are adjusted such that the

output settles within 300 ns in both cases, in order to make sure that the small signal settling is completed with sufficient accuracy within the output multiplexing duration.

Figure 2.21 shows the transient outputs of the S&H and video buffer resembling a 384x288 FPA with 35 µm pixel pitch for (a) with conventional buffering scheme, and (b) with low power architecture with 8 RCGs. As clearly seen in the figure, the outputs are settled within approximately same duration, indicating that the conventional and low power readout architectures are working at the same speed. The currents of the S&H opamps, RCG buffers, and output buffers are measured separately in this case in order to calculate the approximate power dissipation of the two output buffering architectures in a 384x288 FPA. The power dissipations are calculated assuming that the readout has 384 readout channels, and the supply voltages of the S&H opamps and the buffers are 3.3 V and 5 V, respectively. The measured currents and calculated total power dissipations for the two cases are listed in Table 2.5. As the table indicates, test results show that the power dissipation of the buffering structure of a 384x288 FPA with 35 µm pixel pitch can be reduced from 281 mW to 66.5 mW, which corresponds to a 76% improvement, by applying the RCG concept.



(a)



(b)

Figure 2.21: The transient outputs of the S&H and video buffer resembling a 384x288 FPA with 35 µm pixel pitch for (a) with conventional buffering scheme, and (b) with low power architecture with 8 RCGs. It is seen that the outputs are settled within the same duration, indicating that the conventional and low power output buffering architectures are working at the same speed with the adjusted currents.

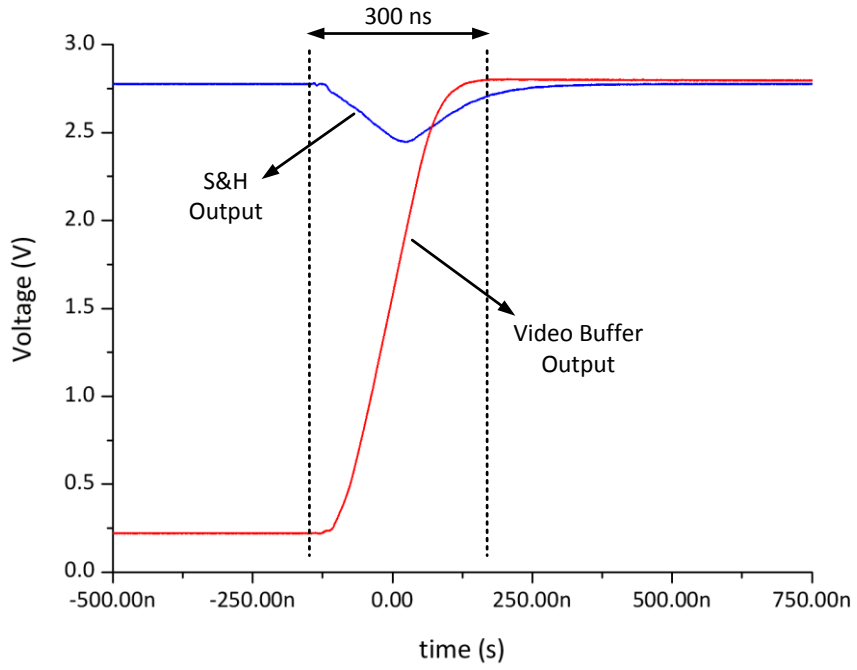
Table 2.5: Measured currents and calculated total power dissipation of the buffering structure of a 384x288 FPA for conventional buffering scheme and low power architecture with 8 RCGs. The total power dissipations are calculated assuming that the readout has 384 readout channels, and the supply voltages of the S&H opamps and the buffers are 3.3 V and 5 V, respectively.

	Conventional	***With 8 RCGs***
S&H Opamp Current	(384) x 221 µA	(384) x 47.5 µA
RCG Buffer Current	-	(8) x 120 µA
Output Buffer Current	(2) x 137 µA	(2) x 151 µA
Total Power Dissipation of the Output Buffering Architecture	281 mW	66.5 mW

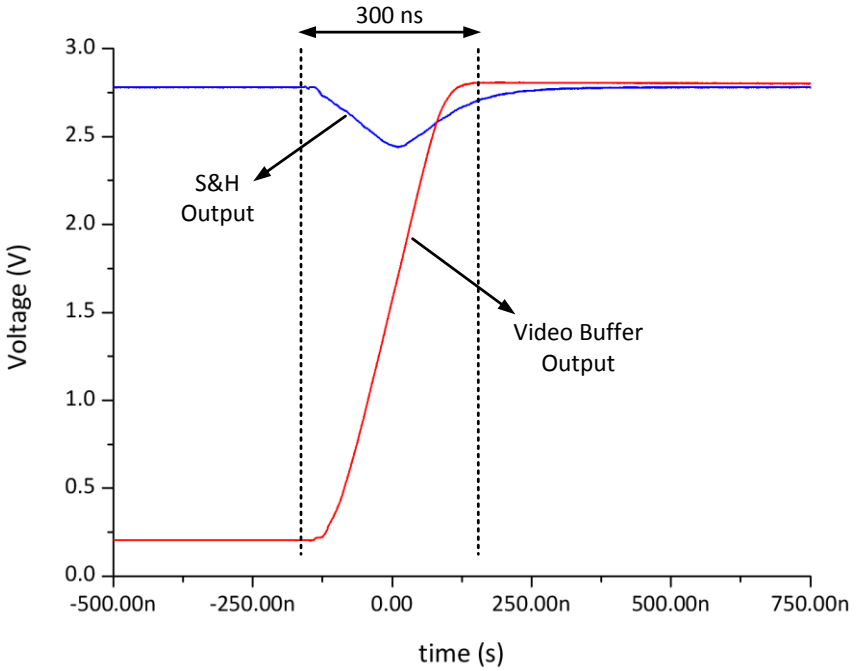
2.4.1.3 Effect of Digitally Controllable S&H Opamp on Power Dissipation

After the RCG concept, the effect of the digitally controllable S&H opamp on the power dissipation of the buffering structure has also been tested. For this purpose, the same configuration for the 8 RCG case in the previous tests are conserved except the S&H block. Then, digital control signals are applied to the S&H opamp, and the analog bias voltages are adjusted such that the output settles within again 300 ns.

Figure 2.22 shows the transient outputs of the S&H and video buffer for the 8 RCG configuration used in the previous test, when the high current mode of the S&H opamp is activated during (a) both sampling and output multiplexing and (b) only output multiplexing. The test is performed for these two modes since the changing DC points may necessitate the activation of high current mode during both sampling and output multiplexing. The figure shows that the output voltages are settled within 300 ns, which verifies that the current of the S&H opamp is adjusted properly.



(a)



(b)

Figure 2.22: The transient outputs of the S&H and video buffer for the 8 RCG configuration used in the previous test, when high current mode of the S&H opamp is activated during (a) both sampling and output multiplexing, and (b) only output multiplexing. The output voltages are settled within 300 ns, showing that the S&H opamp currents are adjusted properly.

Table 2.6 lists the measured DC current of the S&H opamp for two different activation modes. The measurements show that the power dissipation can be further decreased up to 62% for the 384x288 FPA described in the previous section by using the digitally controllable opamp described in Section 2.2.3.

Table 2.6: Measured DC current of the S&H opamp and corresponding power dissipation of a 384x288 FPA with 35 µm pixel pitch and two output channels operating at 60 fps for two different activation modes. Mode 1 denotes the activation of high current mode during both sampling and output multiplexing, and Mode 2 denotes the activation during only output multiplexing.

	Not Activated	***Mode 1***	***Mode 2***
S&H Current	47.5 µA	17.5 µA	15.5 µA
Total Power Dissipation	65.7 mW	27.7 mW	25.2 mW

2.4.1.4 DC Offset Caused by High Current Mode Activation

Another test is performed in order to verify that the DC offset at the S&H output due to the activation of high current mode is independent of the input voltage as explained in Section 2.2.3. For this purpose, the S&H input is connected to an external voltage, and digital signals are adjusted such that the sampling is done in the low current mode. After the sampling, the opamp is switched to the high current mode, and the S&H output is observed. Figure 2.23 shows the transient output of the S&H block when the opamp is switched to high current mode after an external voltage is sampled. The figure shows that switching between the current modes adds an offset to the output voltage, which is approximately equal to 6 mV for this specific test.

This operation is repeated for various input voltages within the operation range of the S&H block, and the corresponding output voltages are measured using an oscilloscope. Figure 2.24 shows the measured S&H output offset for different input voltages. As the figure indicates, the measurements show that the offset is almost constant through the entire operation range as expected. Therefore, this offset can be treated as a part of the FPN and can be corrected easily.

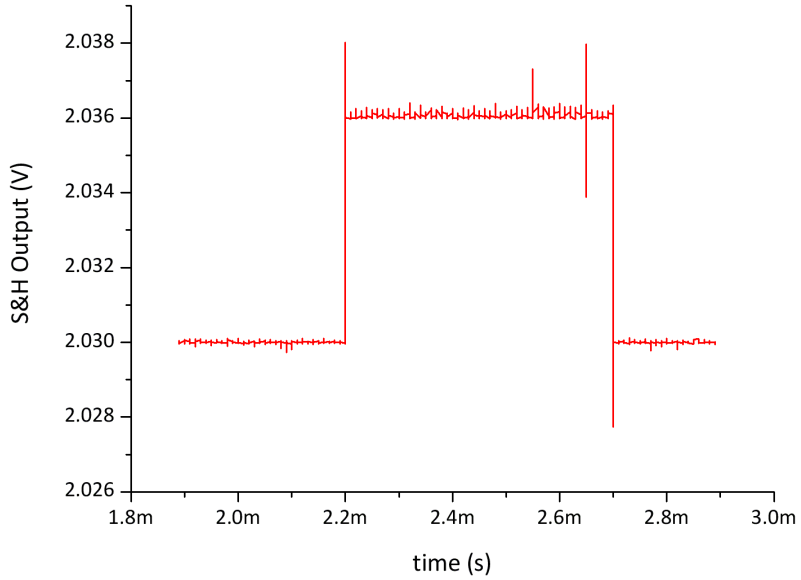


Figure 2.23: Transient output voltage of the S&H block when the opamp is switched to high current mode after an external voltage is sampled. This figure shows that switching between the current modes adds an offset to the output voltage, which is approximately equal to 6 mV for this specific test.

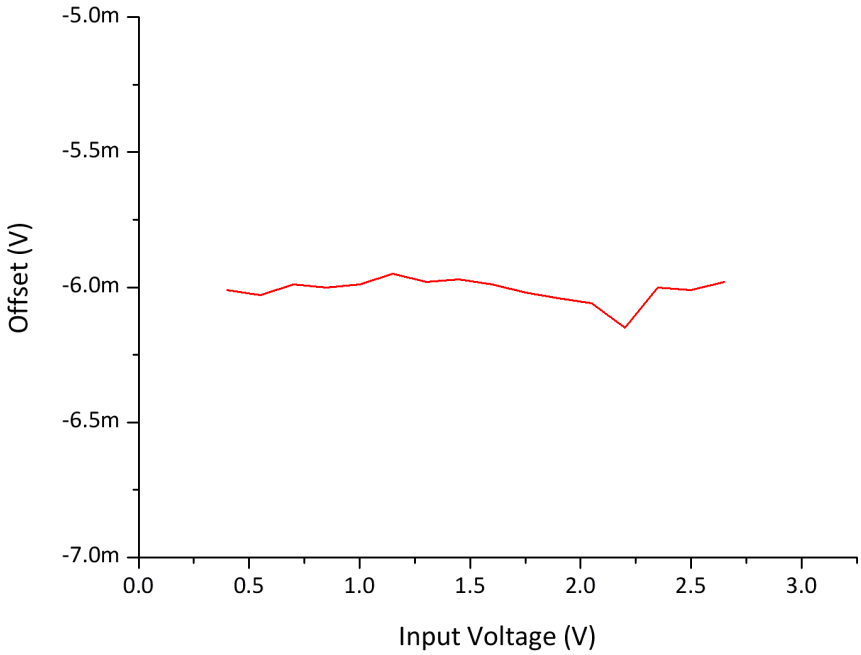


Figure 2.24: Measured offset values at the S&H output for different input voltages. The opamp bias voltages were constant during all measurements.

2.4.2 Test Results of the Improved Bias Correction DAC

Figure 2.25 shows the improved bias correction DAC test circuit, which is fabricated in a standard 0.6 µm CMOS process. The circuit has all the necessary parts to be used in an actual FPA readout; besides the DAC itself, there are also digital circuitries used for storing and transferring the digital bias correction data. Moreover, there are 4 configuration switches which enable testing the two stages of the structure independently. Figure 2.26 shows the layout of the circuit, while Figure 2.27 shows the photograph of the fabricated chip, which occupies an area of 2.9 mm x 0.9 mm and has 36 I/O pads. The fabricated chip is tested in order to verify the proper operation of the blocks and determine their performance in terms of linearity and power dissipation.

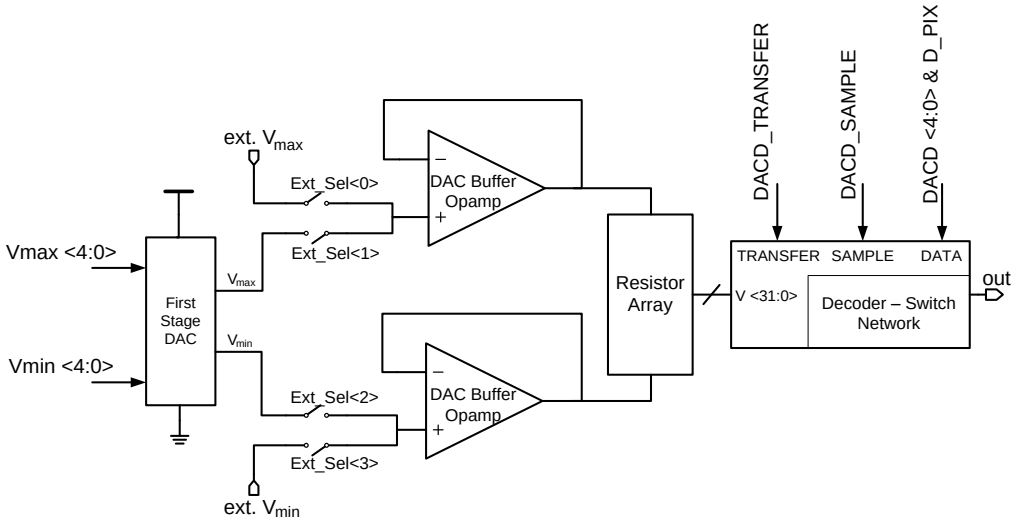


Figure 2.25: Simplified schematic of the improved bias correction DAC circuit, which is fabricated in a standard 0.6 µm CMOS process.

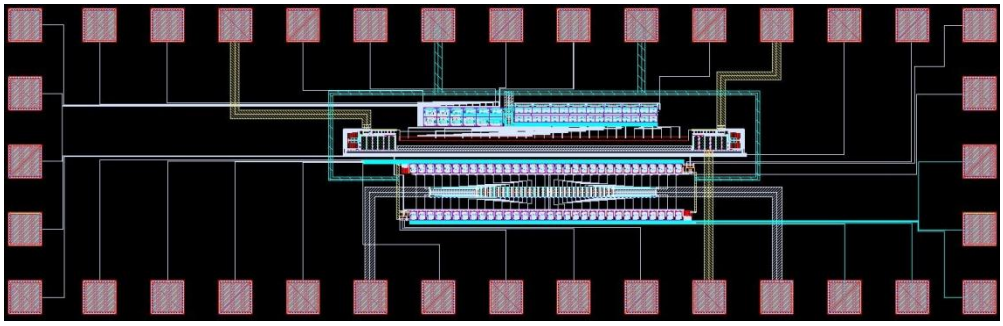


Figure 2.26: Layout of the test circuit designed to test the improved DAC structure, which occupies an area of 2.9 mm x 0.9 mm in a standard 0.6 µm CMOS process and has 36 I/O pads.

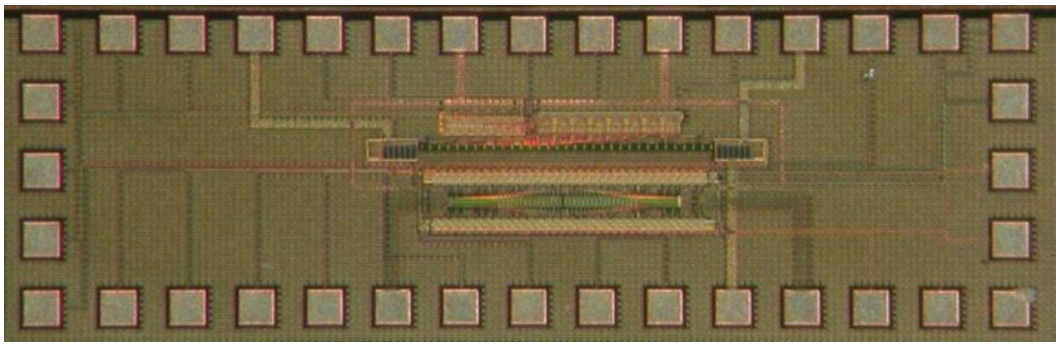


Figure 2.27: Photograph of the fabricated test circuit designed to test the improved DAC structure, which occupies an area of 2.9 mm x 0.9 mm in a standard 0.6 µm CMOS process and has 36 I/O pads.

2.4.2.1 Test Results of the First Stage

The first test conducted is the input-output relationship of the first stage. For this purpose, *Ext_Sel<2>* and *Ext_Sel<3>* are set to high, and consequently, the output of the first stage DAC is connected to a bond pad. Then, the output voltage is measured by a multimeter and recorded for each digital input. Figure 2.28 shows the measured input-output relationship of the first stage of the bias correction DAC for a supply voltage of 5 V. As the figure indicates, the first stage DAC has a highly linear output. The measured power dissipation of the first stage is approximately 2 mW, which is a relatively high value as expected. As stated in Section 2.3.3, the first stage resistance should be low in order to decrease the noise, which results in a relatively high power dissipation. Nevertheless, only one or two first stage DACs are sufficient for an entire readout channel array, and therefore, the overall power dissipation of this block will be only a small part of the overall power dissipation of the readout.

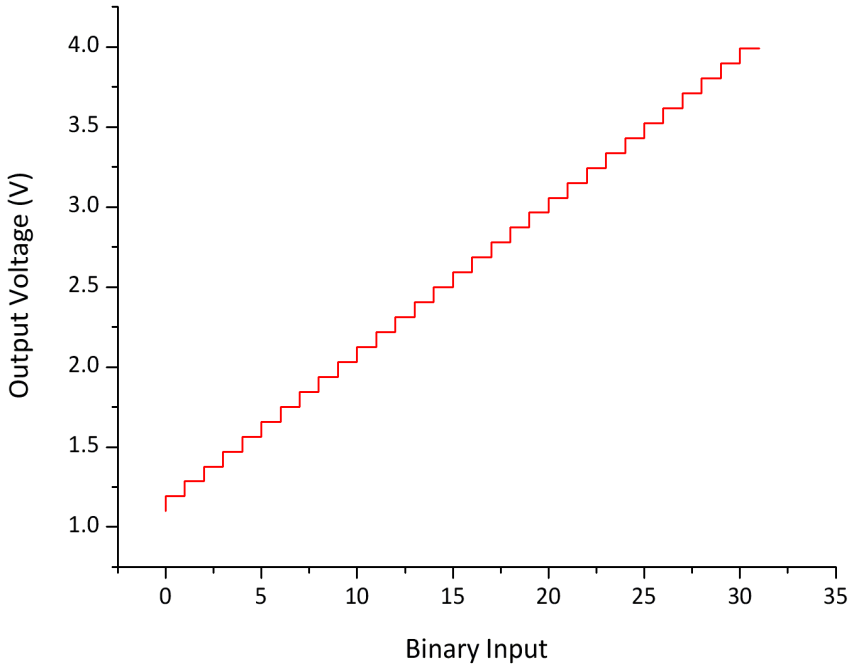


Figure 2.28: Measured input-output relationship of the first stage of the bias correction DAC for a supply voltage of 5 V.

2.4.2.2 Test Results of the Second Stage

After the test of the first stage is completed, another test is performed in order to verify the proper operation of the second stage. For this purpose, the inputs of both buffers are connected to external voltages. Then, the digital input is incremented continuously, and the corresponding output is observed through a buffer connected LF353 opamp using an oscilloscope. The bias correction data and timing signals of the digital blocks are generated using an FPGA chip. Figure 2.29 shows the transient output voltage of the second stage of the bias correction DAC. For this test, the external voltages are adjusted as V_{max} = 3.5 V and V_{min} = 1.9 V; however, the outputs change in a slightly different range due to the gain error of the buffers. The results verify that the second stage of the bias correction DAC also operates properly.

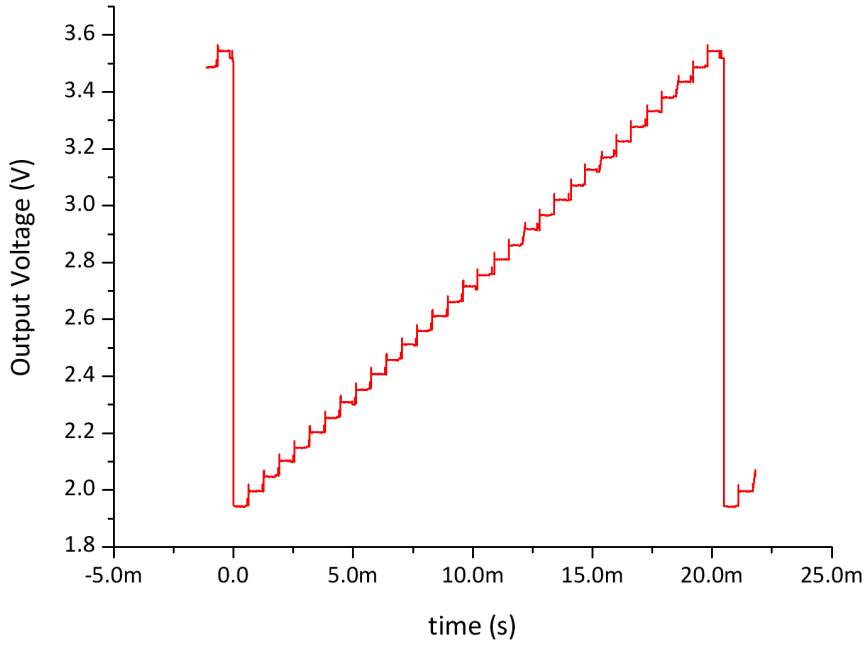


Figure 2.29: Transient output of the second stage of the bias correction DAC. The data is obtained by continuously incrementing the digital input.

The power dissipation of the second stage during this test is measured to be 0.21 mW, which provides a slew rate of 0.37 V/µs with 15 pF capacitive load at the output. However, the power dissipation of the second stage strongly depends on the injection transistor dimensions, bias voltage range, and available bias voltage settling duration. Therefore, the actual power dissipation of this structure can only be determined after the FPA is fabricated and the pixels are characterized.

2.5 Summary and Conclusions

This chapter presented the development of a low power readout architecture which will be used for the development of a low power ROIC for a 384x288 FPA. The new architecture consists of a low power sampling and buffering scheme, and an improved bias correction DAC structure. The low power sampling and

buffering scheme has two main parts: a new output buffering scheme and a special opamp with digitally controllable current modes. The improved bias correction DAC is composed of two stages: one for determining the overall bias voltage range and the other for generating the distinct bias values for each readout channel.

The new output buffering structure used in the low power architecture decreases the capacitive load at the output of the readout channels. Although it adds one extra stage on the signal path, the overall power dissipation is greatly reduced due to the reduced current capability requirement for the S&H opamps. The power dissipation of the output buffering architecture is further decreased by using a special opamp with digitally controllable current modes in the S&H block. The opamp is switched to the high power dissipation mode only during output multiplexing, which is very short when compared to integration time. Therefore, the average power dissipation of the readout channels becomes very low.

In the improved bias correction DAC structure, both stages use resistive ladder type DACs, which are capable of giving multiple outputs. As a result, the number of the DACs, and hence, the total power dissipation of the bias correction structure is decreased. Furthermore, reduced area and power dissipation allows implementing a dedicated DAC for each readout channel, unlike the previous designs at METU, which reduces the noise caused by sampling of the bias voltages.

The first test circuits of the low power sampling and buffering architecture were fabricated through an MPW run, and its proper operation has been verified before the design of the ROIC. Then, the improved DAC has been developed during the design of the ROIC of the 384x288 array. Test circuits designed for both structures are fabricated together with this ROIC, and the results of the

tests performed on these circuits are presented in this chapter. The test results include the results of both the low power sampling and buffering architecture and the improved DAC. The obtained results show that the low power sampling and buffering architecture can decrease the power dissipation of the output buffering architecture of a 384x288 FPA with a 35 µm pixel pitch and two output channels operating at 50 fps from 281 mW to 25.2 mW, which corresponds to an reduction of 91% in power dissipation. The test results of the improved bias correction DAC structure verify the proper operation of the circuit. The total power dissipation of this structure depends on several FPA parameters such as required noise level, injection transistor dimensions, bias voltage range, and available bias voltage settling time. However, the test results show that the power dissipation of the bias correction DAC is reduced to a great extent in any case when compared to the previously used structure.

CHAPTER 3

DESIGN OF A 384x288 RESISTIVE MICROBOLOMETER FPA READOUT

This chapter includes the details of the readout circuit designed for a 384x288 resistive microbolometer FPA with 35 µm pixel pitch. The readout is designed for parallel operation, and one CTIA type readout channel is implemented for each detector column. Therefore, all pixels in a single row are processed simultaneously, and the image is formed by addressing all rows sequentially within a frame period. The readout channel outputs are multiplexed to the chip output using the low power sampling and buffering architecture described in Chapter 2. The chip has two output buffers, but it can be operated in single and dual output modes. The improved bias correction structure presented in Chapter 2 is used in order to apply specific bias voltages to each pixel, and even completely turn off the bias of the defective pixels. A digital timing circuitry generates the necessary digital signals for pixel addressing, output multiplexing and switched capacitor operations in the readout channels. The digital blocks also include a control interface, which is used to configure several parameters of the readout.

The 384x288 FPA readout is implemented in a standard 0.6 µm CMOS process, and it can be tested using the poly-Si resistors implemented on the chip without the need of any suspended pixels.

The chapter is organized as follows: Section 3.1 gives the general architecture of the readout. Section 3.2 presents the pixel placement and in-pixel CMOS circuitries for different types of pixels. Then, Section 3.3 and Section 3.4 explain the design and operation principles of the analog and digital blocks of the readout circuit, respectively. Section 3.5 gives the floor plan and layout of the designed FPA readout. Finally, Section 3.6 presents the expected performance parameters of the designed readout.

3.1 Readout Architecture

Figure 3.1 shows the simplified block diagram of the readout architecture of the 384x288 FPA. The 384x288 FPA consists of three main parts: (i) the pixel array, (ii) the analog readout blocks, and (iii) the digital readout blocks. The analog blocks include the readout channels, analog bias voltage generation blocks, buffers, and analog multiplexers used for selecting the bias sources for the analog voltages. The digital blocks include the timing signals block, row and output multiplexers, and the control interface.

In the readout, there is one CTIA type readout channel implemented for each column with a width of 70 μm. Since the readout channel width is twice the pixel width, two readout channel arrays (RCAs) are implemented; odd numbered columns are connected to the RCA at the top and even numbered columns are connected to the one at the bottom. During readout operation, one row is selected at a time and all columns in the selected row are processed simultaneously. The outputs of the readout channels are then multiplexed and sent to the output channels while the next row is being processed. The output multiplexing is done using the low power sampling and buffering architecture described in Section 2.2, with 8 RCGs in total. In order to decrease the sensitivity to common mode fluctuations, outputs are designed differential.

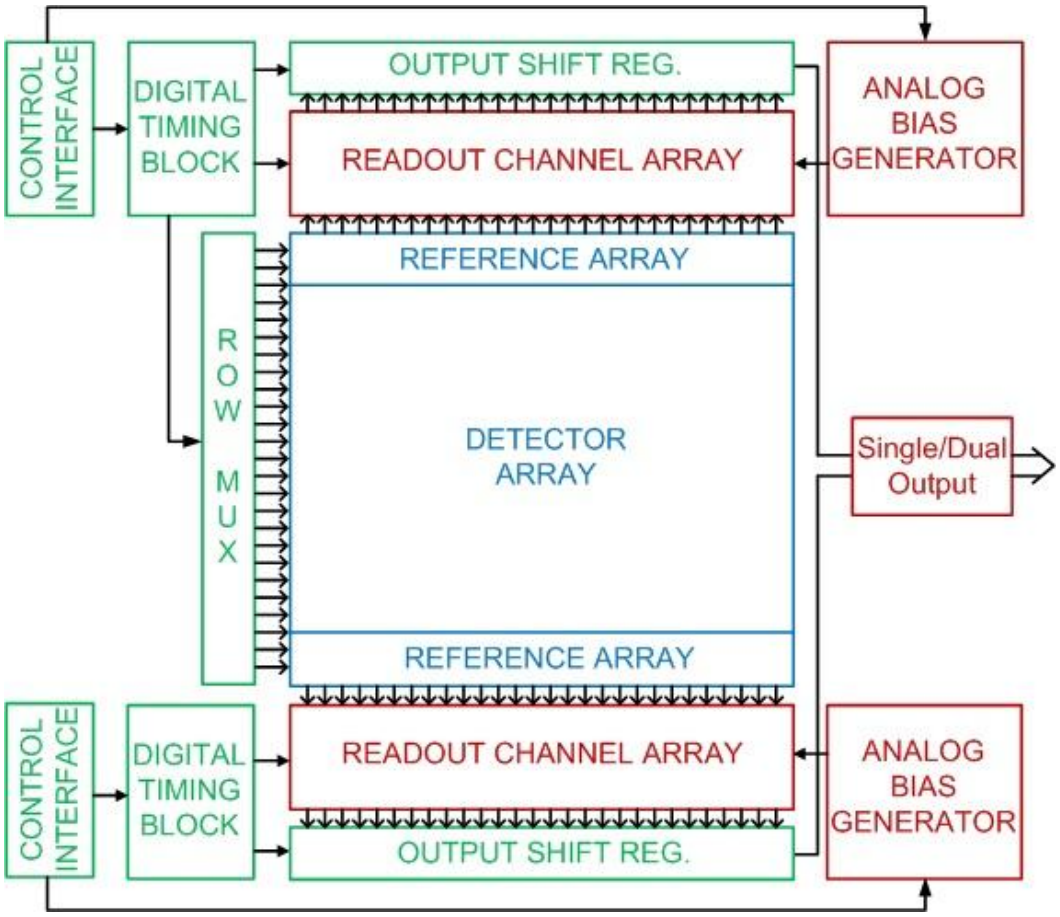


Figure 3.1: Simplified block diagram of the readout architecture of the 384x288 FPA.

Each output channel includes two output buffers: one gives the readout output and the other one gives a reference voltage, which is taken from the first stage of the bias correction structure. The actual output will be the difference of these two voltages, which will provide a pseudo-differential operation and hence reduce the sensitivity of the output voltage to the fluctuations in the supply voltages.

The analog voltages required to bias the pixels and the opamps in the readout channels are generated by the analog bias generation blocks. The required voltages are generated using resistive ladder type DACs and bandgap reference

circuits. Bandgap reference circuits are normally preferred for critical voltages; however, all bias voltages have the option to be generated by a DAC in order increase the controllability.

Besides the bias voltages, the analog readout channel array also requires digital timing signals in order to perform the switched-capacitor operations like integration and sampling. Not only the readout channels, but also the row and output multiplexers require timing signals. The digital timing block generates the timing signals required by these blocks.

There are several controllable parameters in the readout like the operational array size, number of active output channels, integration capacitance value, analog bias voltage values, etc. These parameters are controlled by the control interface block, which is a serially programmable on-chip RAM. Details of the various blocks of the chip are explained in the following sections.

3.2 Pixels

The detector and reference pixels of the 384x288 resistive microbolometer FPA will be fabricated by a post-CMOS process which is out of the scope of this thesis. However, the bias lines and readout connections of these pixels should be fabricated during the CMOS process. Besides the connections of the actual pixels, the 384x288 FPA also includes poly-Si resistors, which are called self-test pixels. These resistors are IR blind since they are not suspended; and therefore, they cannot be used for IR imaging. However, it is possible to test the basic functions of the readout without any post-CMOS process by connecting these self-test pixels to the preamplifiers.

Section 3.2.1 gives the placement of the pixels, and then, the following three sections describe the circuitry implemented for detector, reference and self-test pixels.

3.2.1 Placement of the Pixels

The placement plan of the detector and reference pixels are done during the readout design, and the readout connections are implemented accordingly. Figure 3.2 shows the pixel placement of the 384x288 resistive microbolometer FPA. The dummy row and columns are placed in order to increase the uniformity of the actual pixels.

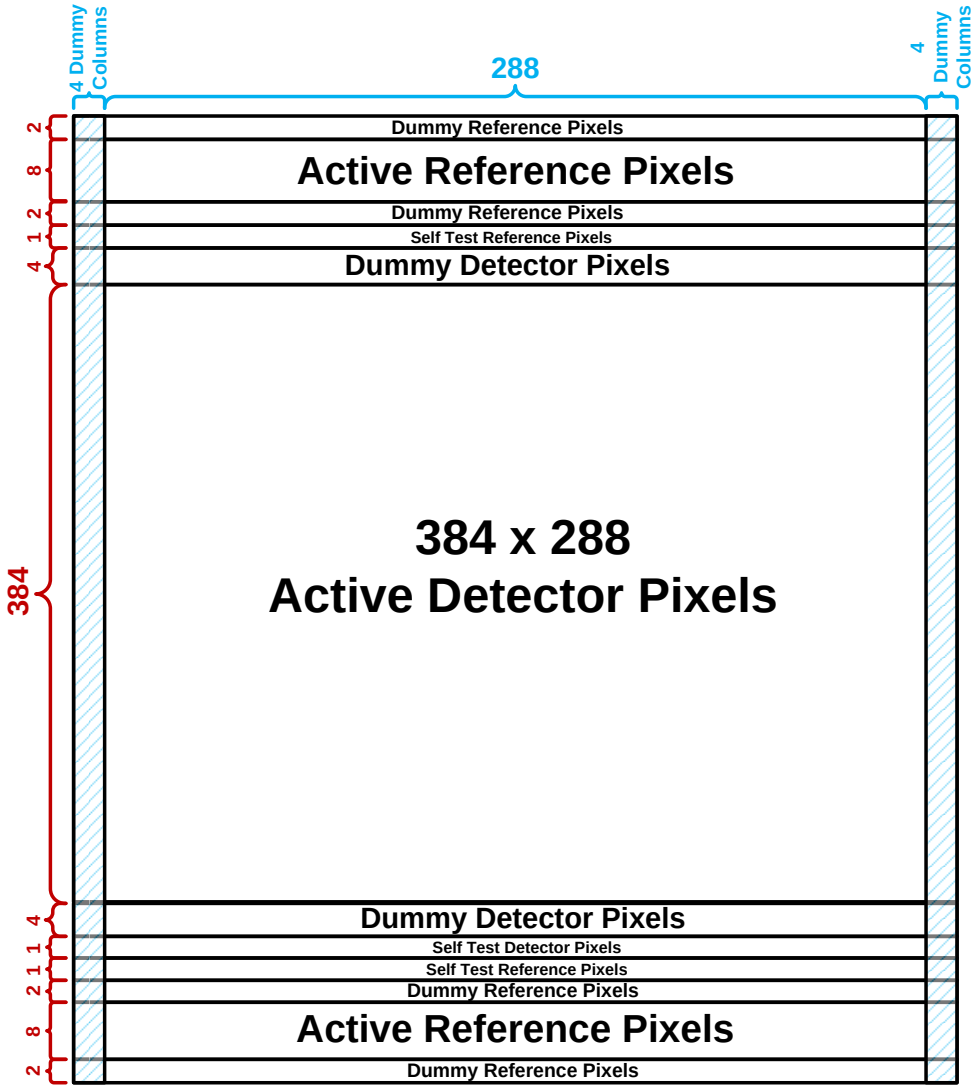


Figure 3.2: The pixel placement of the 384x288 resistive microbolometer FPA. The numbers of the rows and columns for each pixel type are shown on the figure.

3.2.2 Detector Pixel Circuitry

Figure 3.3 shows the layout of the circuitry implemented on the detector pixel area, which consists of an NMOS switch, two metal lines, and two pad openings.

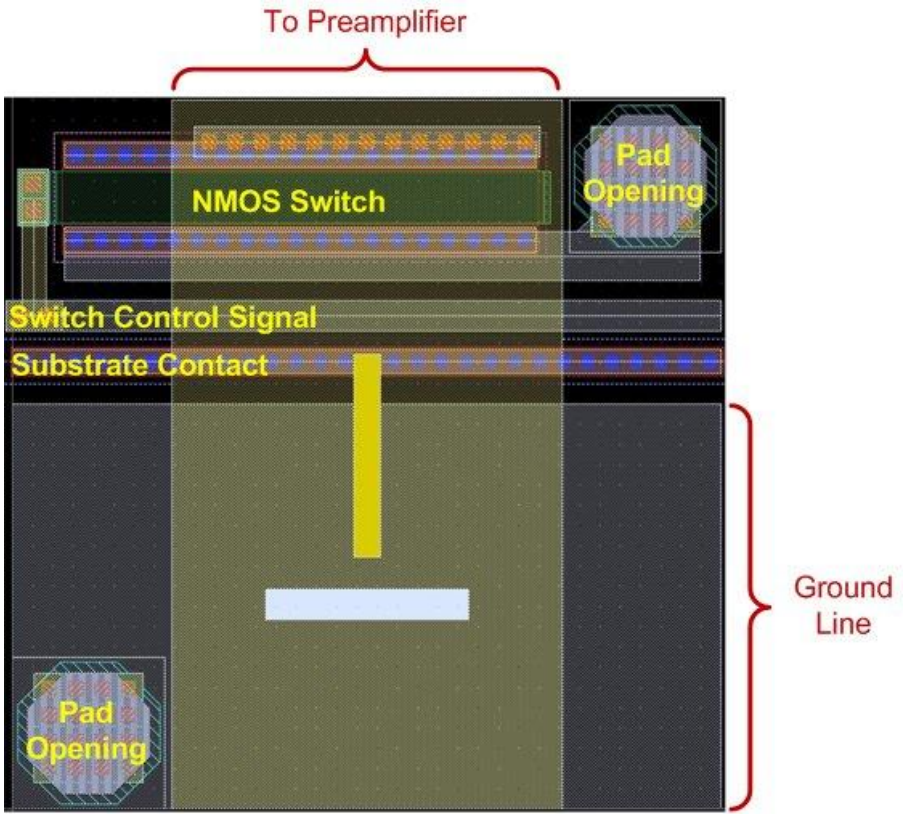


Figure 3.3: Layout of the detector pixel circuitry implemented on the detector pixel area, which consists of an NMOS switch, two metal lines, and two pad openings.

The pad openings are necessary to provide contact between the fabricated detector and the CMOS circuitry. One terminal of the detector will be connected to the switch, and the other will be connected to the ground rail via the pad openings. The switch is used for addressing, and its control signal is

common with the other detector pixels on the same row. A single NMOS transistor provides sufficiently low switch resistance since the detector will be connected to the lower half of the CTIA, where the voltage levels will be low. When high voltage is applied to the gate of the switch transistor, the detector will be connected to the preamplifier through the vertical metal line. Figure 3.4 shows the corresponding schematic view of the detector pixel circuitry.

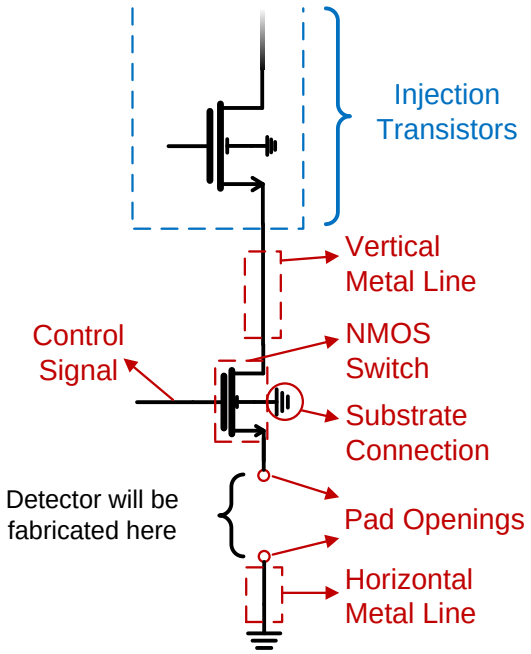


Figure 3.4: Schematic view of the detector pixel circuitry corresponding to the layout given in Figure 3.3.

3.2.3 Reference Pixel Circuitry

Figure 3.5 shows the layout of the reference pixel circuitry implemented on the reference pixel area. Similar to the detector pixel circuitry, it consists of a switch, metal routing lines, and two pad openings. The reference pixels are

placed between the detector pixels and the readout; therefore, the routings between these two blocks pass over the reference pixel area as seen in the figure. As a result, there are three routing lines on the reference pixel circuitry.

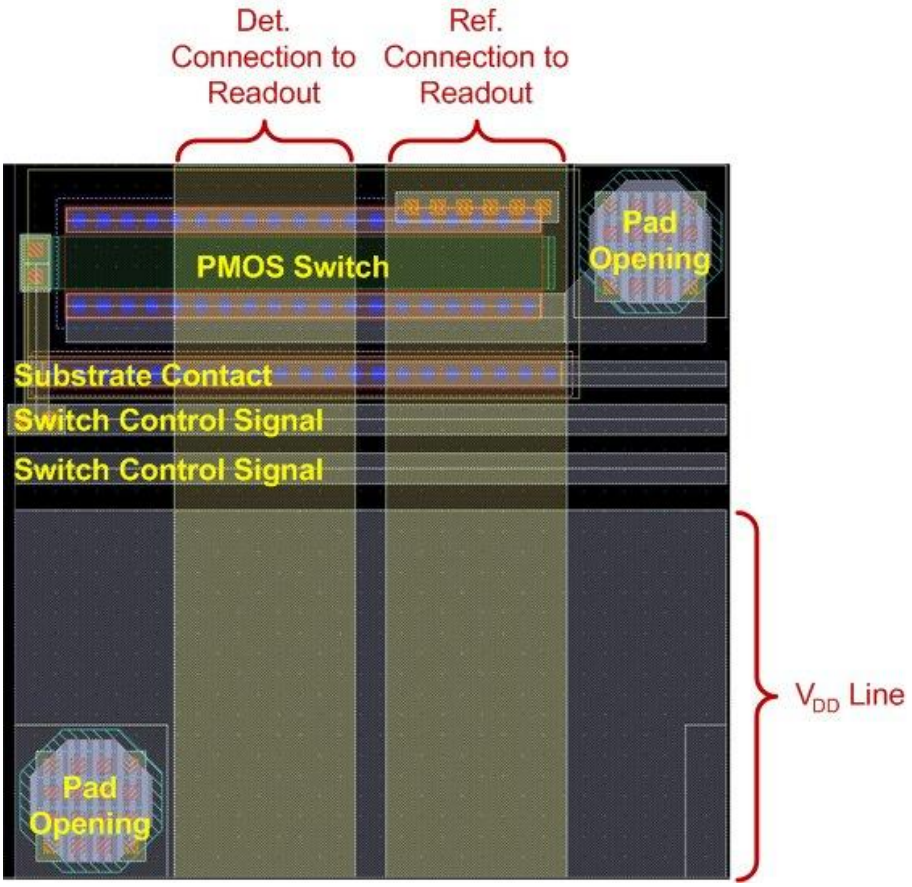


Figure 3.5: Layout of the reference pixel circuitry implemented on the reference pixel area, which consists of a PMOS switch, three metal routing lines, and two pad openings. Since the reference pixels are placed between the detector pixels and the readout, the routings between these two blocks pass over the reference pixel circuitry.

The switch in the reference pixel circuitry is implemented with a PMOS transistor since the reference pixels are connected to the upper half of the biasing circuit and PMOS transistors are more suitable for transferring high voltages.

The reference pixels are placed at the top and the bottom of the detector arrays, next to the RCAs. Therefore, unlike the detectors, both odd and even numbered reference columns are connected to the same RCA. Consequently, there are two reference pixels within the area of a single readout channel. In order to be able to control these two pixels independently, two different switch control lines are implemented in the reference pixel circuitry as shown in Figure 3.5. One of the reference pixels within the area of the same readout channel is connected to one control signal line, and the other reference pixel is connected to the other one. As a result, although they are physically on the same row, these two reference pixels can be used as they are in two different rows.

3.2.4 Self Test Pixels

Figure 3.6 and Figure 3.7 show the layouts of the self test detector and reference pixels, respectively. Although the self test pixels are named as detector and reference, these names only refer to the connection of the pixels to the readout. There is no IR detection or self heating effect in the self test pixels since there are no suspended structures with sufficiently low thermal conductance.

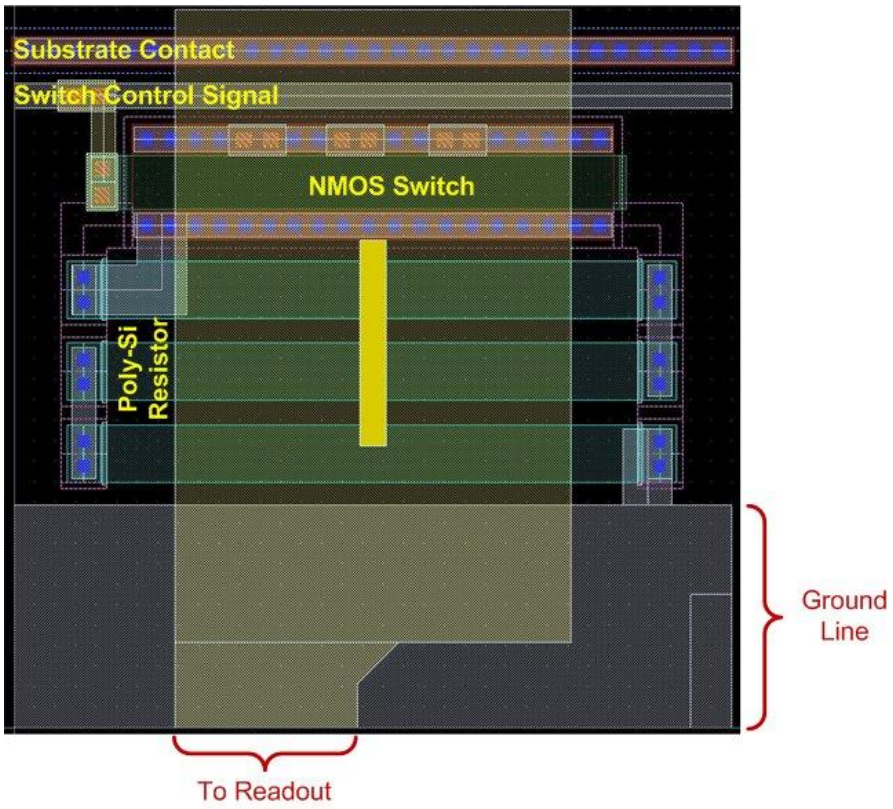


Figure 3.6: Layout of the self test detector pixel. The name 'detector' refers only to the connection of the resistor to the layout; the pixel cannot detect IR radiation since there are no suspended structures with sufficiently low thermal conductance.

The self-test pixels are used to test the basic functions of the readout circuit without any post-CMOS detector fabrication. When the self-test mode is activated, the actual detector and reference pixels are disconnected, and self test pixels are connected to the readout instead. As a result, it will be possible to operate the preamplifiers and the following stages of the readout. The self-test mode can be activated using the control interface, which will be described in Section 3.4.7.

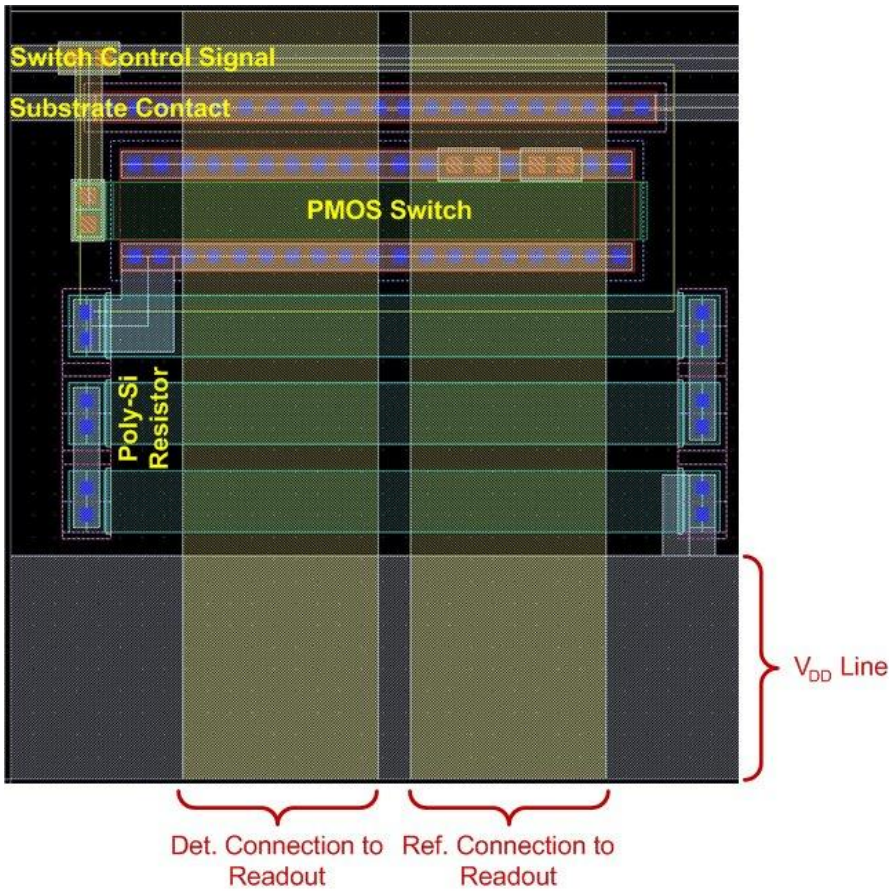


Figure 3.7: Layout of the self test reference pixel. The name 'reference' refers only to the connection of the pixel to the readout.

3.3 Analog Blocks

Analog blocks of the 384x288 resistive microbolometer FPA can be examined in four main parts: (i) the readout channels, (ii) the buffers, (iii) the analog bias generation blocks, and (iv) the analog multiplexers. The readout channels are the basic signal processing units as mentioned previously, and they form the main part of the analog readout. Buffers are necessary in output multiplexing and the bias correction structure; each buffer is designed according to the calculated output load and time constraints. The analog bias generation blocks are used to generate and control the bias voltages of the readout channels and

buffers. Finally, the analog multiplexers are used to connect the bias nodes to either internal blocks or to the bond pads, which increases the controllability and the observability of the bias voltages.

3.3.1 Readout Channel

The readout channel of the 384x288 FPA, which consists of a CTIA type preamplifier and a S&H block, is designed according to the advanced low power sampling and buffering scheme described in Section 2.2. In order to further decrease the power dissipation, the integrator and the S&H blocks are designed to work with a 3.3 V power supply. Nevertheless, the readout channel will work without any problems with 5 V supply as well.

The readout channel is the basic analog signal processing unit of the readout; the resistance data of the pixels, which is a measure of the absorbed radiation, is processed by these units. Then, the data processed by all readout channels are multiplexed and sent to the chip output. Figure 3.8 shows the block diagram of the readout channel array (RCA), which is implemented in both sides of the pixel array. The readout channel array consists of 4 RCGs, each containing 48 readout channels.

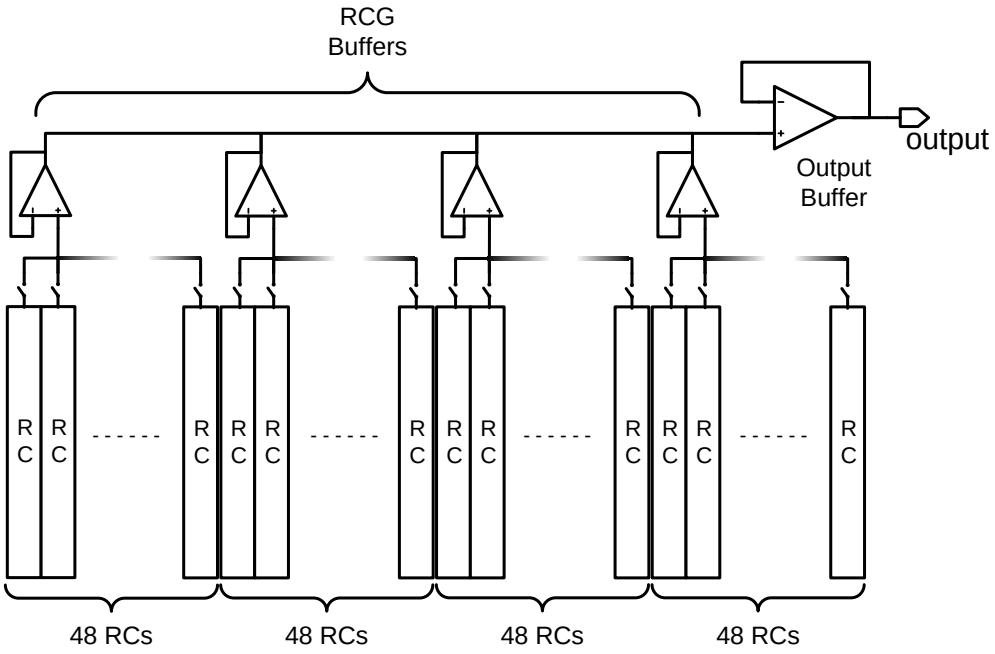


Figure 3.8: Block diagram of the readout channel array, which is implemented on both sides of the FPA. The readout channel array consists of 4 RCGs, each containing 48 readout channels. As a result, two readout channel arrays include 384 readout channels, and each column has its own readout channel.

3.3.1.1 CTIA Type Preamplifier

Figure 3.9 shows the schematic view of the CTIA type preamplifier used in the readout channel block. The block biases the pixels using the injection transistors, and the output current is integrated by the switched capacitor integrator in order to amplify and band-limit the signal.

The first step of the microbolometer readout operation is biasing the detectors. The biasing circuit is designed to operate with a 5 V supply; and the integrator reset voltage is set to 2.5 V in order to provide symmetry. The reference and detector pixels are connected such that the voltage headroom consumed by self heating is below the integrator reset voltage, since the integrator supply voltage

is only 3.3 V. Figure 3.10 shows the integration curve characteristic of the designed biasing circuitry.

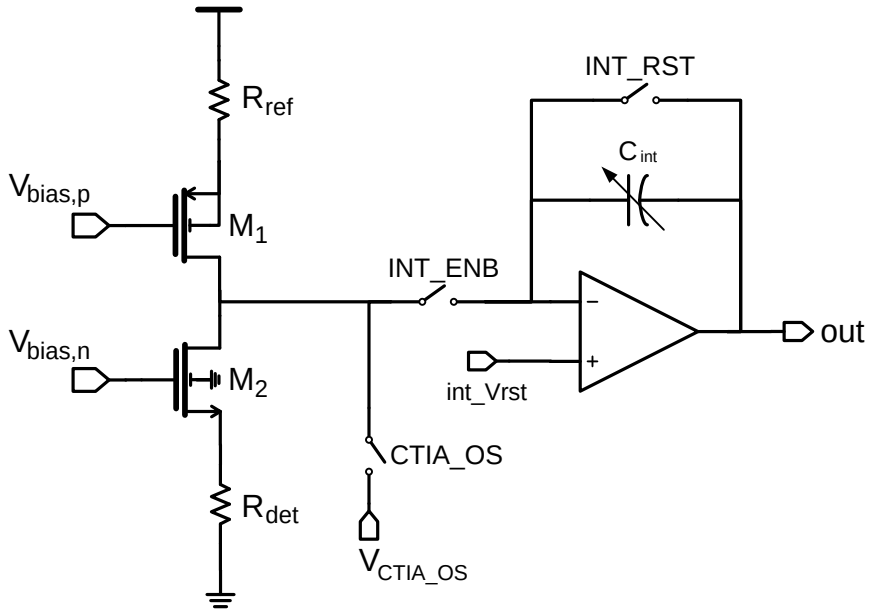


Figure 3.9: Schematic view of the CTIA type preamplifier used in the readout channel block.

If the transistors are in saturation and channel length modulation is neglected, the voltage on the detector pixel can be expressed as

$$V_{det} = \left(V_{b,n} - V_{t,n}\right) - \frac{1}{K_n R_{det}} \cdot \left(\sqrt{1 + 2K_n R_{det}\left(V_{b,n} - V_{t,n}\right)} - 1\right) \qquad 3.1$$

where $V_{b,n}$ is the gate voltage, $V_{t,n}$ is the threshold voltage, K_n is the gain factor of M_2; and R_{det} is the resistance of the detector pixel. The reference pixel bias can be calculated using the same formula for the PMOS transistor. The gate

voltages of the injection transistors should be adjusted so that the detector and reference pixel currents cancel each other when no IR is present. In the 384x288 FPA readout, the $V_{bias,p}$ voltage is common for the entire readout channel array, while the $V_{bias,n}$ voltage is adjusted for each pixel using the bias correction structure.

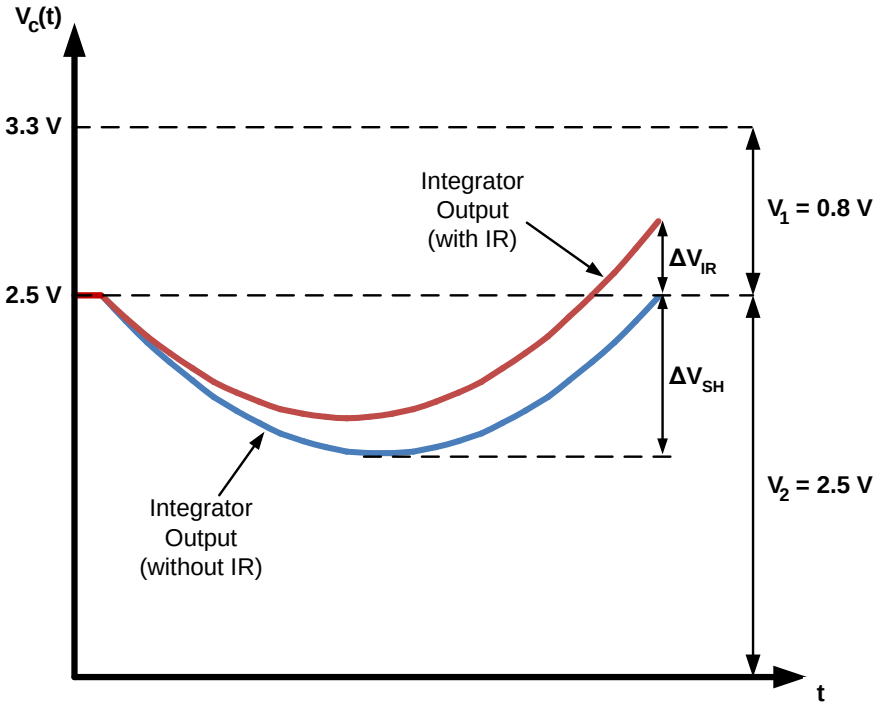


Figure 3.10: Expected integration curve of the implemented CTIA. The reference and detector pixels are connected such that the voltage headroom consumed by self heating, which is denoted as ΔV_{SH}, is in the region between ground and integrator reset voltage since the available headroom is larger than the upper region labeled as V_1.

Equation 3.1 states that the voltage on the detector depends on the detector resistance as well as the gate voltage of the injection transistor and the transistor parameters. This effect is due to the negative feedback structure formed by source degeneration, and it affects the responsivity of the

preamplifier. The change in the bias voltage with changing resistance can be expressed as

$$\frac{\partial V_{det}}{\partial R_{det}} = \frac{I_{det}}{1 + g_m R_{det}} \tag{3.2}$$

where I_{det} is the detector current, g_m is the transconductance of the injection transistor at that specific bias, and R_{det} is the detector resistance. For a detector material with negative TCR, absorbed IR radiation decreases the detector resistance. Equation 3.2 states that the bias voltage also decreases when the resistance is decreased; and consequently, the current induced due to absorbed IR radiation decreases. In order to reduce the effect of the negative feedback, g_m of the transistor should be kept high.

The noise of the injection transistors directly add up to the integrated current; and therefore, should be kept as low as possible. The overall current noise power of a MOS transistor is given as

$$i_{n,d}{}^2 = \left(\underbrace{4kT\gamma g_m}_{Thermal} + \underbrace{2qI_{DS}}_{Shot} + \underbrace{\frac{K}{f} \cdot \frac{g_m{}^2}{WLC_{ox}}}_{Flicker} \right) \cdot \Delta f \tag{3.3}$$

where γ is a parameter changing from $2/3$ in long channel devices to 2.5 in short channel devices; q is the charge of a single electron; I_{DS} is the DC current flowing through the transistor; W and L are the device width and length, respectively; and C_{ox} is the gate capacitance per unit length [53]. In the frequency band of interest, the flicker noise component is generally dominant;

and therefore, increasing the device area effectively decreases the overall noise contribution of the injection transistors.

Table 3.1 shows the aspect ratios of the injection transistors, which are selected considering the transconductance and noise issues discussed in the above paragraphs. Figure 3.11 shows the simulated change in the bias voltage with changing detector resistance for a 15 µA bias current and a 60 kΩ detector resistance. In this case, about 4.7% of the current induced by the absorbed IR radiation will be cancelled by the negative feedback mechanism. Figure 3.12 shows the simulation result for the noise PSD of the implemented injection transistors at the same current bias. The rms value of the injection transistor current noise over a bandwidth from 0.1 Hz to 10 kHz is equal to 19.87 pA, which is almost negligible when compared to other noise sources like the detector or the injection transistor bias circuitry.

Table 3.1: Dimensions of the injection transistors in the CTIA preamplifier.

	W (µm)	***L (µm)***
M_1	180	2.5
M_2	120	2.5

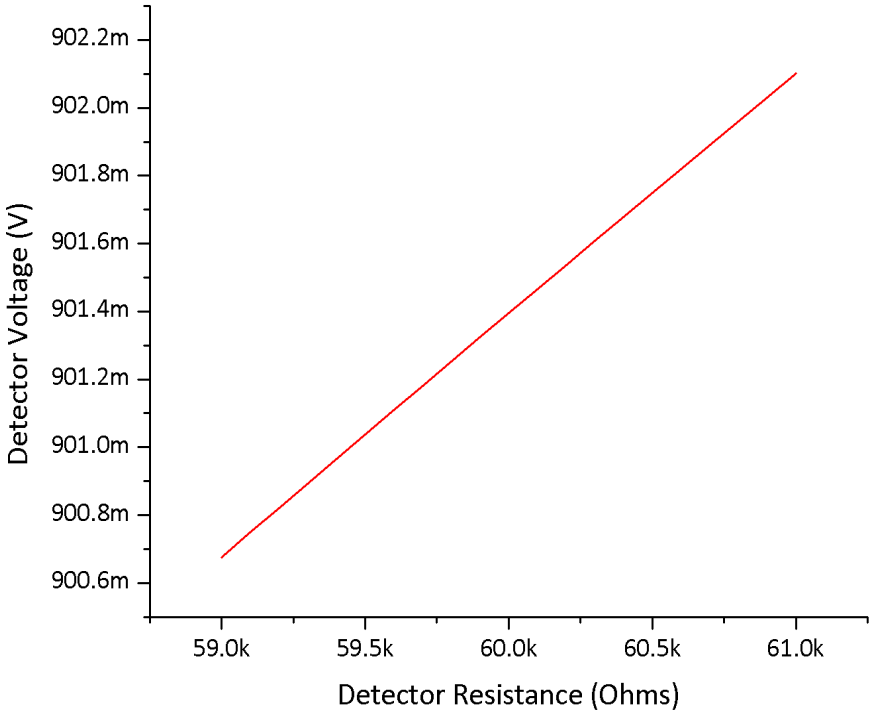


Figure 3.11: Simulated detector bias voltage with changing detector resistance for a 15 µA bias current and a 60 kΩ detector resistance. The bias voltage on the detector changes due to the negative feedback effect although the gate voltage of the injection transistor stays constant.

Before the integration is enabled, the voltage at the output node of the biasing circuit settles at a value such that the detector and reference currents are equal to each other. When the integration enable switch is closed, the negative feedback of the opamp sets the voltage at this node to $V_{rst,int}$, which is typically selected as $V_{DD}/2$, and the output current is integrated on the integration capacitance. The voltage change requires charge transfer from the drain capacitances of the injection transistors; and this charge may be injected into the integration capacitor. In order to prevent the corruption of the signal by the injected charge, the voltage at the output node of the biasing circuit is set to $V_{rst,int}$ by a low impedance voltage source before the integration. This operation is called 'CTIA output stabilization' in this work. Figure 3.13 shows the

simulated outputs of the integrator for different amounts of resistance change (a) with and (b) without CTIA output stabilization. As seen in the figure, output stabilization greatly increases the linearity of the integrator.

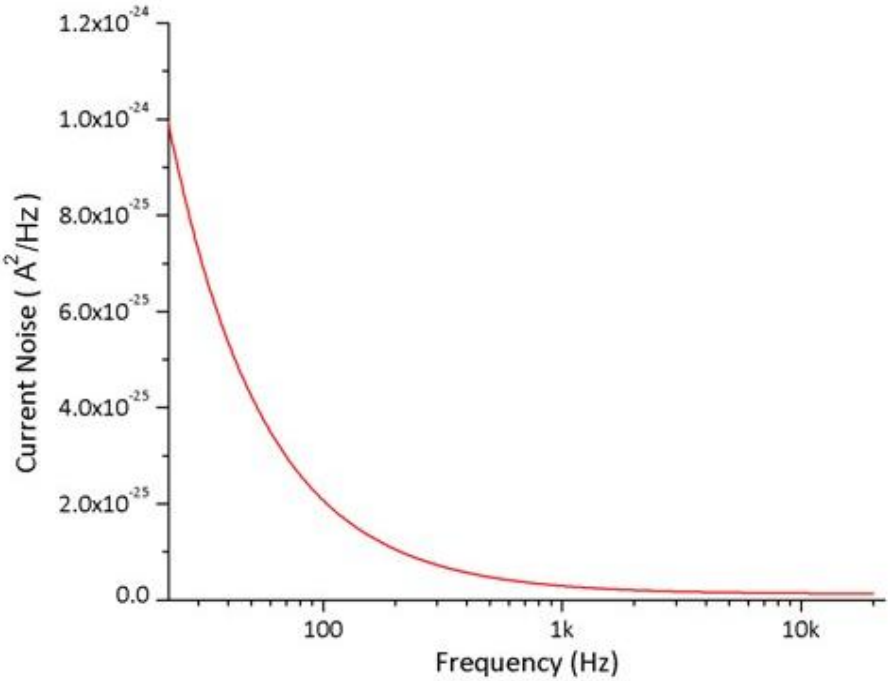
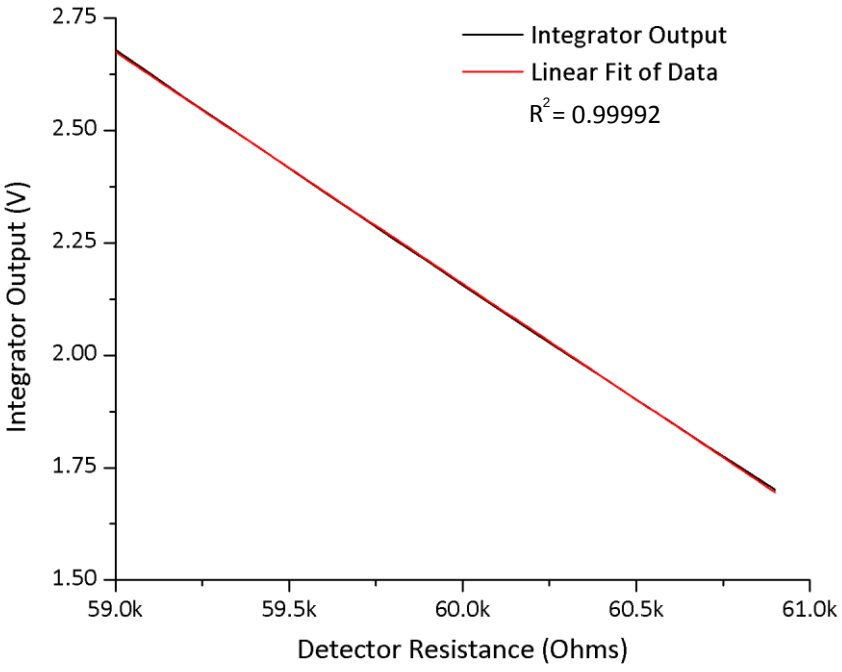
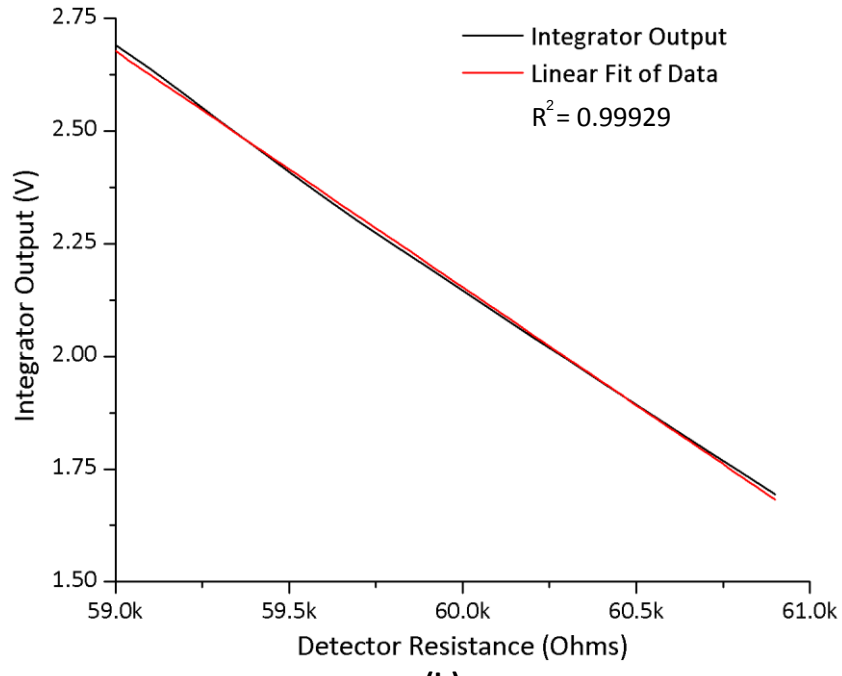


Figure 3.12: Simulation result for the noise PSD of the implemented injection transistors at 15 µA current bias. The integrated noise over the bandwidth (0.1 Hz – 10 kHz) is equal to 19.87 pA.



(a)



(b)

Figure 3.13: Simulated outputs of the integrator for different detector resistance values (a) with and (b) without CTIA output stabilization. The reference resistor and bias voltages are held constant while the detector resistance is being changed, and the output current is integrated for 50 µs to obtain the outputs. The R^2 values of the fitting curves show that the CTIA output stabilization greatly increases the linearity of the integrator.

The output current of the biasing circuit starts being integrated on the integration capacitance when the integration enable switch is closed. The integrator includes a capacitor bank controlled by a 5-bit digital data, which allows the adjustment of the integration capacitance value. Figure 3.14 shows the schematic of the capacitor bank implemented in the integrator block. Each bit controls a 2^n pF capacitor, where n denotes the significance of the bit. As a result, the integration capacitance value will be equal to the number shown by the control bits, in picofarads. Smaller capacitance values provide higher voltage gain; however, too small integration capacitance may cause saturation as explained in Section 1.5.

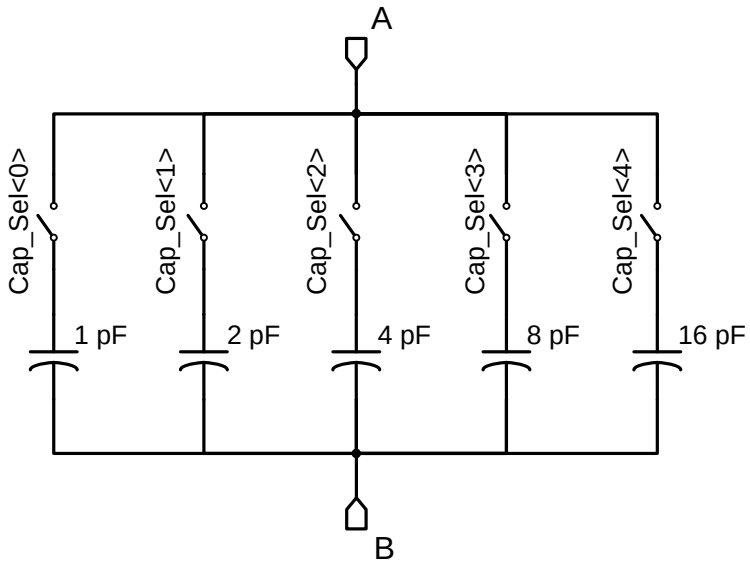


Figure 3.14: Schematic of the capacitor bank implemented in the integrator block. The *Cap_Sel* bits control the switches and hence, the total capacitance between the nodes A and B.

Figure 3.15 shows the layout of the CTIA type preamplifier, which occupies an area of 840 µm x 70 µm in a standard 0.6 µm CMOS process. As seen in the

figure, the switch transistors are covered by a guard ring in order to protect the nearby analog signals.

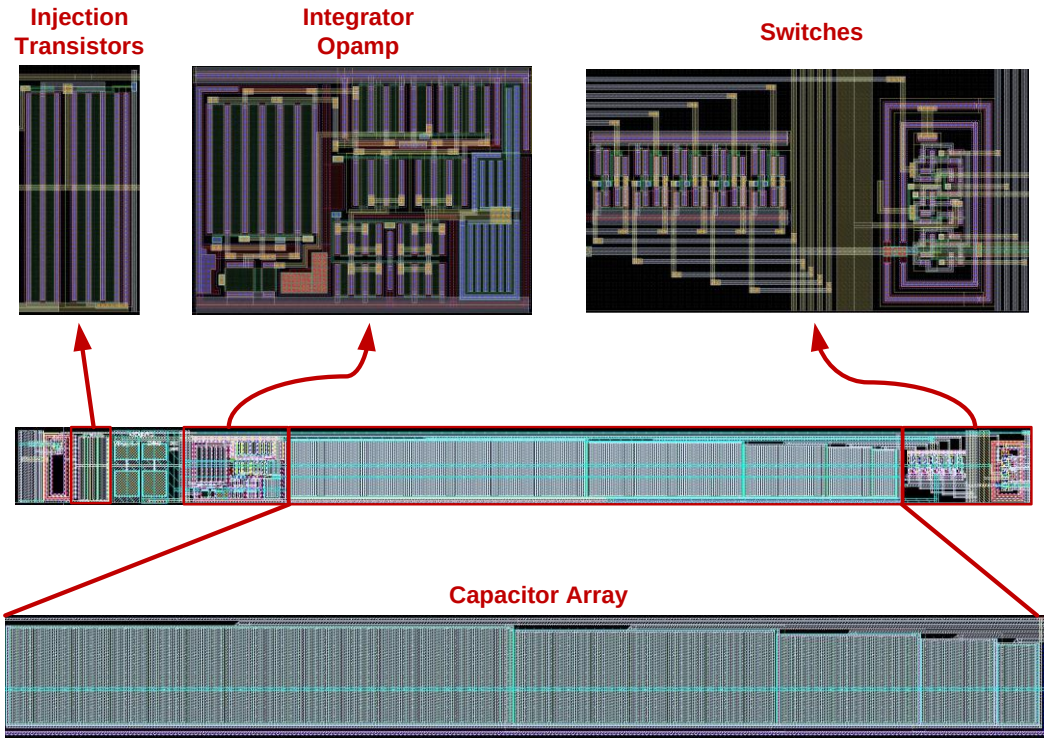


Figure 3.15: Layout of the CTIA type preamplifier, which occupies an area of 840 µm x 70 µm.

3.3.1.1.1 Integrator Opamp

The integrator opamp needs only high gain to minimize the gain error and low noise to minimize the noise contribution from the output node of the biasing circuit. Its load is capacitive only and does not require high output currents; therefore, a single stage opamp will be sufficient. Figure 3.16 shows the schematic of the folded cascode opamp used in the integrator block. Table 3.2 shows the nominal bias voltages, and Table 3.3 lists the parameters of the opamp obtained from simulations using the nominal bias values.

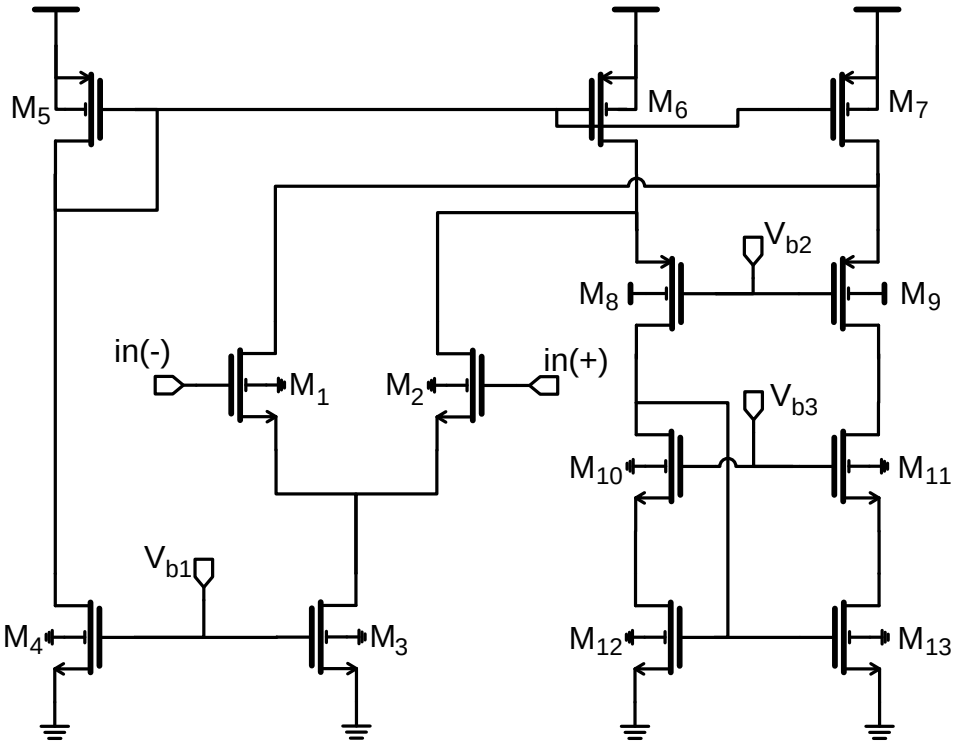


Figure 3.16: Schematic of the folded cascode opamp used in the integrator block.

Table 3.2: Nominal bias voltages and transistor dimensions of the folded cascode opamp used in the integrator block.

Bias Voltages (V)	
$\mathbf{V_{DD}}$	3.30
$\mathbf{V_{b1}}$	1.27
$\mathbf{V_{b2}}$	1.85
$\mathbf{V_{b3}}$	1.40

	W/L (µm / µm)
$\mathbf{M_1, M_2}$	100.5 / 3.0
$\mathbf{M_3}$	7 / 6.0
$\mathbf{M_4}$	3 / 6.0
$\mathbf{M_5}$	12 / 2.4
$\mathbf{M_6, M_7}$	36 / 2.4
$\mathbf{M_8, M_9}$	36 / 2.4
$\mathbf{M_{10}, M_{11}}$	24 / 2.0
$\mathbf{M_{12}, M_{13}}$	24 / 2.0

Table 3.3: Simulated parameters of the integrator opamp. The results are obtained using the nominal bias voltages.

DC Gain	95.46 dB
Noise in Unity Gain Buffer Connection	5.46 µV (0.1 Hz – 10 kHz)
Output Range (For Integrator Configuration)	0.33 V - 2.90 V
Phase Margin	58.6°
Gain Margin	16.52 dB
Total DC power	48.9 µW
Input capacitance (at one terminal)	0.41 pF @ V_{in} = 0 V (maximum) 0.23 pF @ V_{in} = 2.5 V
Reset Time to 2.5V (From Pos. SAT)	352 ns
Reset Time to 2.5V (From Neg. SAT)	510 ns

3.3.1.2 Sample-and-Hold Circuit

The sample-and-hold structure implemented in the 384x288 FPA readout has been given in Figure 2.5. The structure provides offset cancellation and suppresses the flicker noise of the opamp. Furthermore, its output is insensitive to the charges injected by S_s and S_3, and charge injected by S_2 causes only a constant offset, which can be cancelled by the nonuniformity correction algorithms applied to the output signal [53].

Figure 3.17 shows the layout of the S&H circuit, which consists of three CMOS switches, a sampling capacitor, and an opamp. The circuit occupies an area of 223.5 µm x 70 µm in a standard 0.6 µm CMOS process. A guard ring is placed around the switches in order to absorb the charges injected into the substrate during transitions so that the analog blocks are not disturbed.

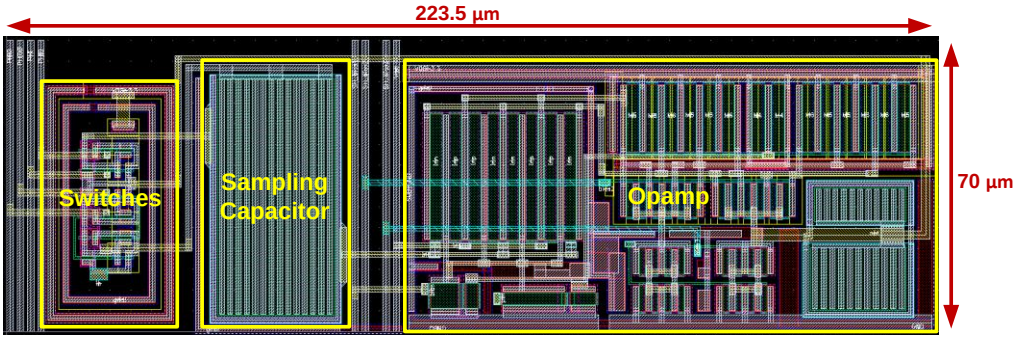


Figure 3.17: Layout of the sample-and-hold circuit, which consists of three CMOS switches, a sampling capacitor and an opamp.

3.3.1.2.1 Sample and Hold Opamp

The 384x288 FPA readout is designed with the low power sampling and buffering architecture described in Section 2.2. Therefore, the opamp used in the S&H block is the special type opamp with digitally controllable current modes, as explained in Section 2.2.3, and its schematic is given in Figure 3.18. The nominal bias voltages and transistor dimensions are listed in Table 3.4, and the opamp parameters obtained from simulations are given in Table 3.5.

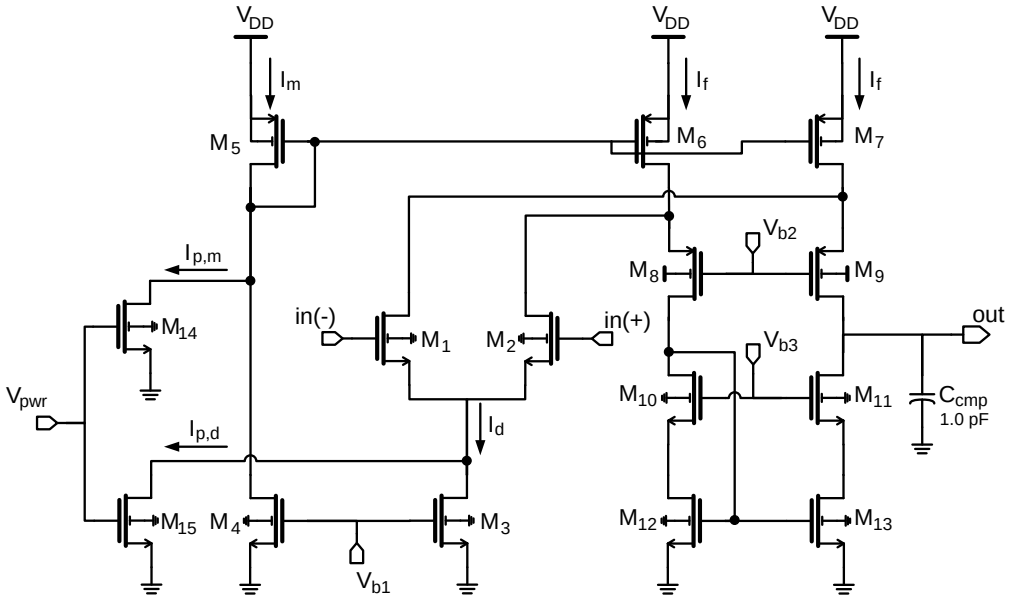


Figure 3.18: Schematic of the special type opamp with digitally controllable current modes, which is used in the sample and hold block. The current capability is controlled by adjusting the currents I_m and I_d using M_{14} and M_{15}. The opamp is in low power mode when V_{pwr} is not high enough to turn the transistors on. When higher V_{pwr} is applied to the opamp, M_{14} and M_{15} have non-zero currents $I_{p,m}$ and $I_{p,d}$, respectively; and consequently, I_m and I_d are increased.

Table 3.4: Nominal bias voltages and transistor dimensions of the S&H opamp.

Bias Voltages (V)	
$\mathbf{V_{DD}}$	3.30
$\mathbf{V_{b1}}$	1.27
$\mathbf{V_{b2}}$	1.85
$\mathbf{V_{b3}}$	1.40
$\mathbf{V_{pwr}}$	0 / 1.27

	W/L (µm / µm)
$\mathbf{M_1, M_2}$	120 / 3.0
$\mathbf{M_3}$	7.0 / 6.0
$\mathbf{M_4}$	3.0 / 6.0
$\mathbf{M_5}$	32 / 3.0
$\mathbf{M_6, M_7}$	96 / 3.0
$\mathbf{M_8, M_9}$	48 / 1.5
$\mathbf{M_{10}, M_{11}}$	24 / 1.5
$\mathbf{M_{12}, M_{13}}$	24 / 1.5
$\mathbf{M_{14}}$	6.0 / 3.0
$\mathbf{M_{15}}$	15 / 3.0

Table 3.5: Simulated parameters of the S&H opamp. The results are obtained using the nominal bias voltages.

	Low Current Mode	***High Current Mode***
DC Gain	91.41 dB	82.49 dB
Noise in Unity Gain Buffer Connection (0.1 Hz – 10 MHz)	68.1 µV	45.7 µV
Output Range	N/A	0.40 V - 2.80 V
Phase Margin	66.45°	58.79°
Gain Margin	19.23 dB	18.82 dB
Total DC power	47.6 µW	295.4 µW
0.02% Bus Settling (From 3.3 V to 0.4 V)	N/A	125 ns
0.02% Bus Settling (From 0 V to 2.8 V)	N/A	135 ns
Output Load	1.0 pF (Including RCG buffer)	

The difference of the S&H opamp from a simple folded cascode opamp is the addition of two extra transistors, which are labeled as M_{14} and M_{15} in the figure. These transistors are connected in parallel with the current source branches of the opamp; and therefore, it is possible to change the branch currents by turning the transistors on and off. In low power mode, V_{pwr} is lower than the threshold voltage, and M_{14} and M_{15} are in off state. When V_{pwr} is set to a value higher than the threshold, the transistors go into saturation; and consequently, the branch currents I_d, I_m, and hence I_f are increased. The output slew current of the opamp can be expressed as

$$I_{out} = \begin{cases} I_f - (I_f - I_d) = +I_d, & Positive\ Slew \\ (I_f - I_d) - I_f = -I_d, & Negative\ Slew \end{cases} \quad 3.4$$

provided that $(I_f - I_d)$ is not negative. Therefore, the output slew current is increased when the opamp is switched to the high current mode.

It is possible to activate the high current mode during both sampling and output multiplexing in order to cancel the offset caused due to changing DC operating points by using the control interface as described in Section 2.2.3. However, the default mode activates the high current mode only during the output multiplexing. Figure 3.19 shows the simulated difference between the input and output voltages of the sample and hold circuit for both operation modes. As seen in the figure, the offset due to shifting of the DC operation point is constant and can be cancelled by the nonuniformity correction algorithms.

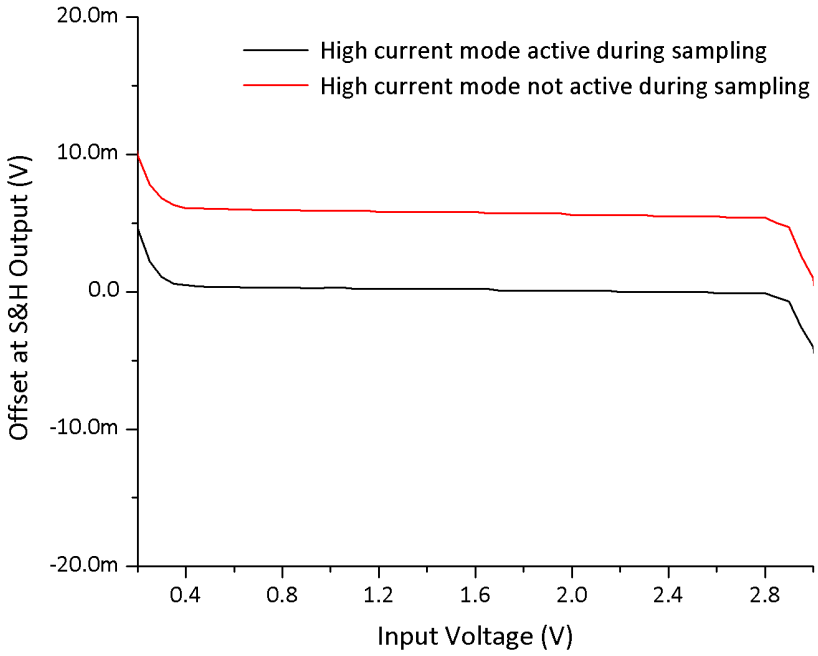


Figure 3.19: Simulated difference between the input and output voltages of the S&H block. The output value is taken while the opamp is at high current mode and sampling operation is performed with low and high current modes, in order to observe the offset caused by shifting of the DC operation points.

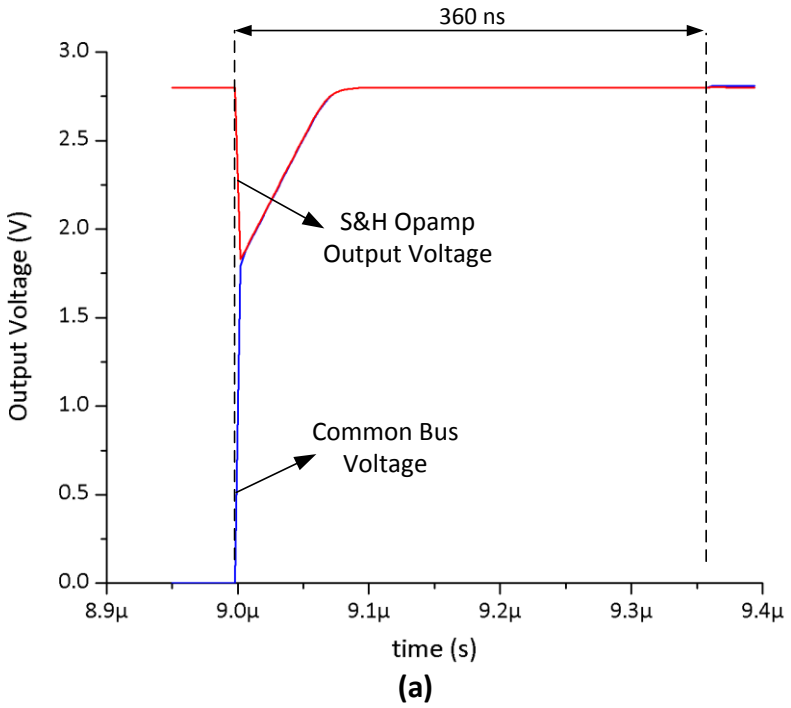


Figure 3.20: The transient simulation results showing the S&H output and common bus voltages during output multiplexing. The common bus voltage is driven by the S&H opamp (a) from 0 V to 2.8 V, and (b) 3.3 V to 0.4 V within a time much less than 360 ns, which is the output multiplexing time of a 384x288 FPA operating at 50 fps with two output channels.

Sample and hold block should be able to drive the RCG bus within the allowed output multiplexing time. Figure 3.20 shows the transient simulation results showing the S&H output and common bus voltages during output multiplexing, when the bus is driven by the S&H opamp (a) from 3.2 V to 0.4 V, and (b) from 0.1 V to 2.8 V. The simulation results in these figures show that the current capability of the opamp is sufficient for driving the bus. In case of insufficient settling time due to unexpected high load or low output current, it is still possible to further increase the output current of the opamp by adjusting the bias voltages using the control interface.

3.3.2 Buffers

There are four types of buffers used in the 384x288 FPA readout: (i) RCG buffers, (ii) output buffers, (iii) the bias correction DAC buffers, and (iv) the CTIA output stabilization buffer. Each buffer is designed considering the necessary design requirements like gain and output driving capability. The RCG buffers and output buffers have only capacitive loads; therefore, the folded cascode topology is chosen. On the other hand, bias correction DAC buffers are required to drive resistive loads, and the CTIA output stabilization buffer should be able to handle relatively large currents since the output stabilization line is common for all the readout channels within the same array. Therefore, a simple two stage topology is used in the bias correction DAC buffer, and another two stage opamp, which is an IP of the X-FAB Semiconductor Foundries, is used for the CTIA output stabilization line.

The following sections describe the RCG buffer, output buffer, bias correction DAC buffer, and CTIA output stabilization line buffer.

3.3.2.1 RCG Buffer

Figure 3.21 shows the schematic of the RCG buffer opamp, which is used to buffer the outputs of the readout channels within the same RCG. Its output is connected to the output buffer; and therefore, the load is only capacitive. However, due to the large capacitive load and limited output multiplexing time, the necessary output current is much higher than the sample and hold opamps. Increased current reduces the maximum gain of the MOS transistors, which increases the gain error. In order to reduce the gain error to acceptable levels, three cascode stages are used in the RCG buffer opamp. The nominal bias voltages and transistor dimensions of the RCG buffer opamp is given in Table 3.6, and its parameters obtained from simulations are listed in Table 3.7.

The RCG buffers should be able to drive the capacitive load at the output with a delay time that will not prevent the settling of the output within the output multiplexing time. Figure 3.22 shows the transient simulation result of the RCG buffer with the calculated capacitive load of 1.8 pF at the output and S&H block at the input: (a) from 0.1 V to 2.8 V, and (b) from 3.2 V to 0.4 V. The simulation results show that the RCG output can be settled for the given voltage swings within 170 ns.

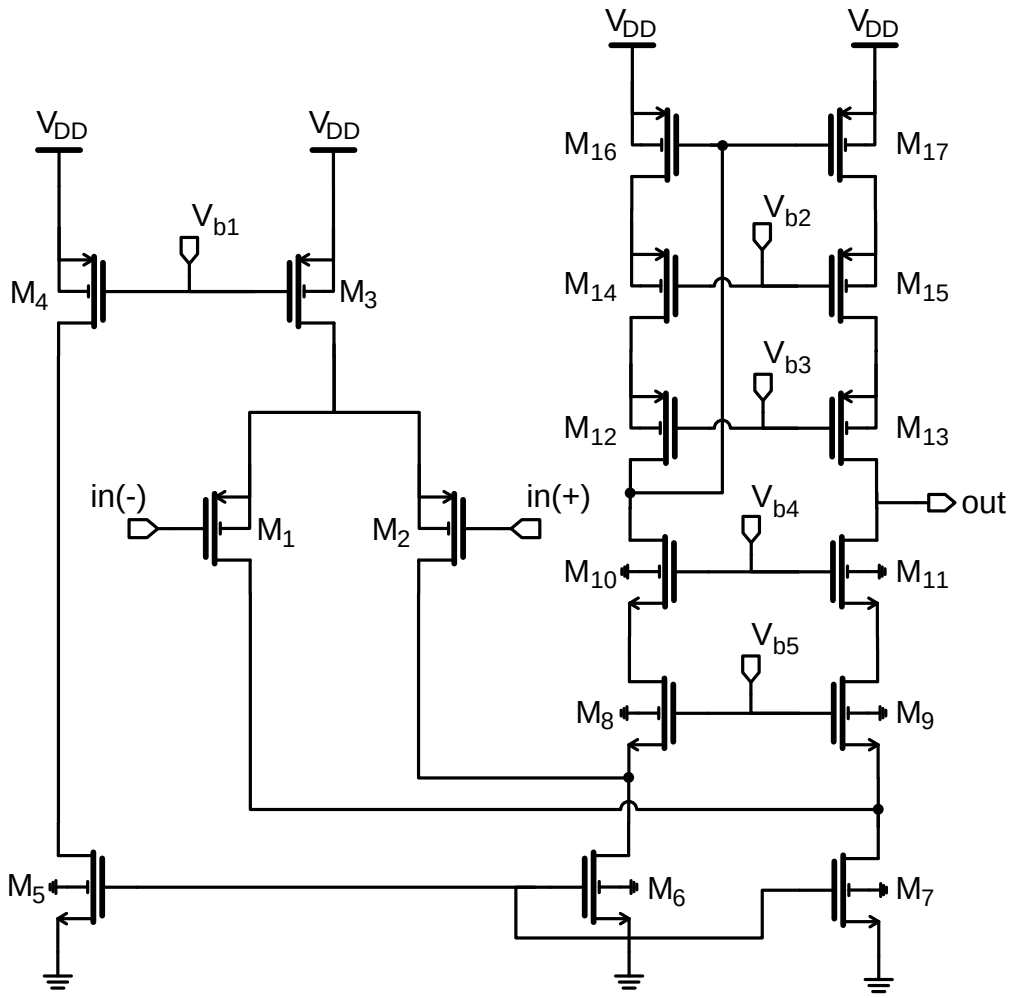


Figure 3.21: Schematic of the RCG buffer opamp, which is used to buffer the outputs of the readout channels within the same RCG.

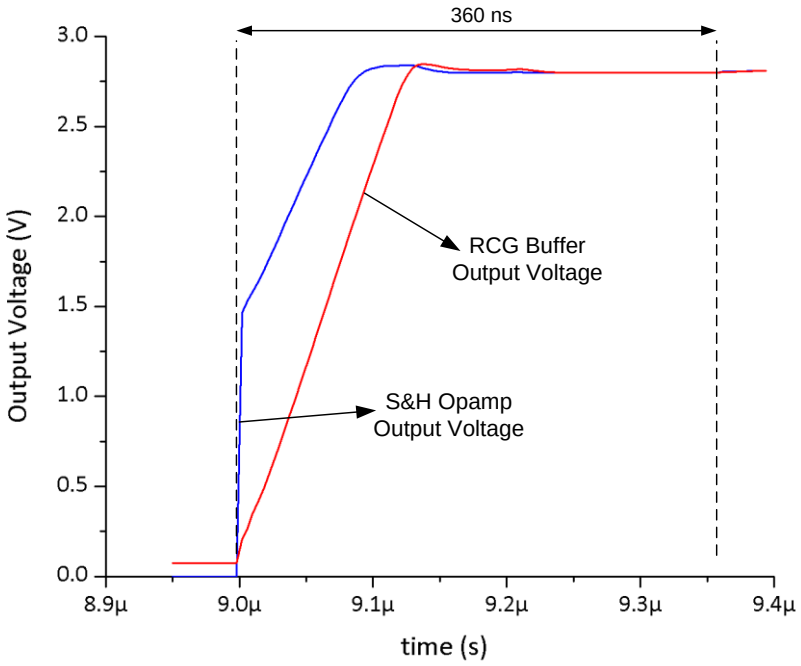
Table 3.6: Nominal bias voltages and transistor dimensions of the RCG buffer opamp.

Bias Voltages (V)	
V_{DD}	5.00
V_{b1}	3.508
V_{b2}	3.50
V_{b3}	3.00
V_{b4}	1.70
V_{b5}	1.45

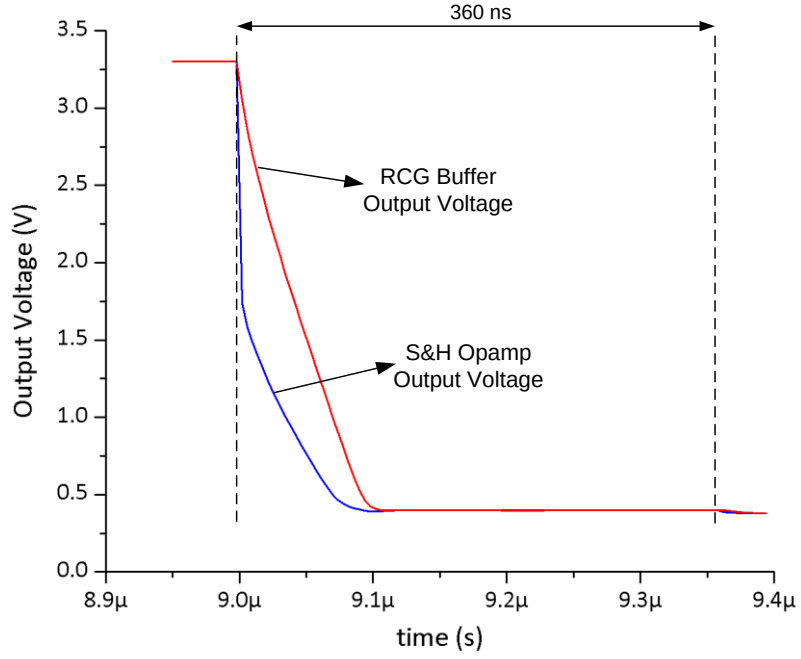
	W/L (µm / µm)
M_1, M_2	240 / 3.0
M_3	55.8 / 6.0
M_4	2.5 / 6.0
M_5	4.2 / 6.0
M_6, M_7	70 / 4.0
M_8, M_9	149.8 / 1.2
M_{10}, M_{11}	149.8 / 1.2
M_{12}, M_{13}	120.4 / 1.2
M_{14}, M_{15}	120.4 / 1.2
M_{16}, M_{17}	30 / 1.2

Table 3.7: Simulated parameters of the RCG buffer opamp. The results are obtained using the nominal bias voltages.

DC Gain	77.71 dB
Noise in Unity Gain Buffer Connection (0.1 Hz – 10 MHz)	38.7 µV
Output Range	0.45 V – 3.95 V
Phase Margin (with load capacitance)	71.84°
Gain Margin	13.45 dB
Total DC power	520 µW
0.02% Bus Settling (From 3.3 V to 0.4 V)	160 ns
0.02% Bus Settling (From 0 V to 2.8 V)	170 ns
Output Load	1.8 pF (including output buffer)



(a)



(b)

Figure 3.22: Transient simulation result of the RCG buffer with the calculated capacitive load of 1.8 pF at the output and S&H block at the input: (a) from 0.1 V to 2.8 V, and (b) from 3.2 V to 0.4 V.

Figure 3.23 shows the layout of the RCG buffer, which occupies an area of 269 µm x 66 µm in a standard 0.6 µm CMOS process. The transistor layouts are drawn interdigitated in order to minimize the offsets caused by mismatches.

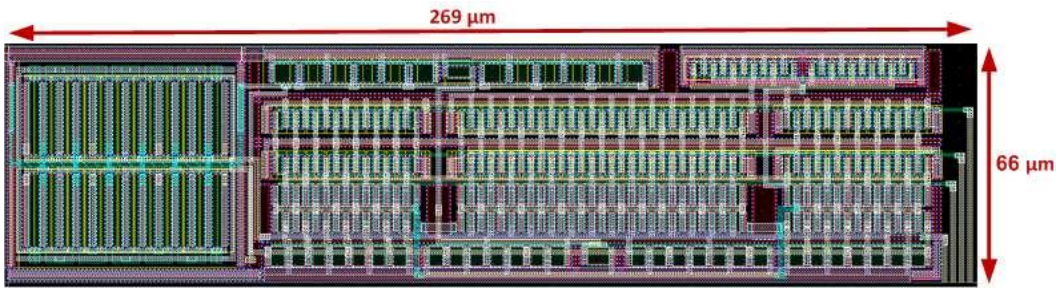


Figure 3.23: Layout of the RCG buffer opamp, which occupies an area of 269 µm x 66 µm in a standard 0.6 µm CMOS process.

3.3.2.2 Output Buffer

The output buffers are used to drive the chip output directly, and therefore, its expected load is much higher when compared to S&H blocks and RCG buffers. Like the RCG buffer, a folded cascode opamp with three cascode stages is used as the output buffer in order to provide sufficient gain and output current at the same time. The schematic of the output buffer is the same as the RCG buffer, which is shown in Figure 3.21. However, the nominal bias voltages, transistor dimensions, and consequently, the opamp parameters are different than the RCG buffer opamp. Table 3.8 gives the nominal bias voltages and transistor dimensions of the output buffer, and Table 3.9 lists the opamp parameters obtained from simulations.

The output buffer is designed to be able to drive 5 pF capacitive load within the output multiplexing time. Figure 3.24 shows the transient simulation results of the output buffer with a 5 pF output load, with its input changing from (a) 0 V to

2.8 V, and (b) 3.3 V to 0.4 V. The simulation results show that the output is easily settled within the output multiplexing time.

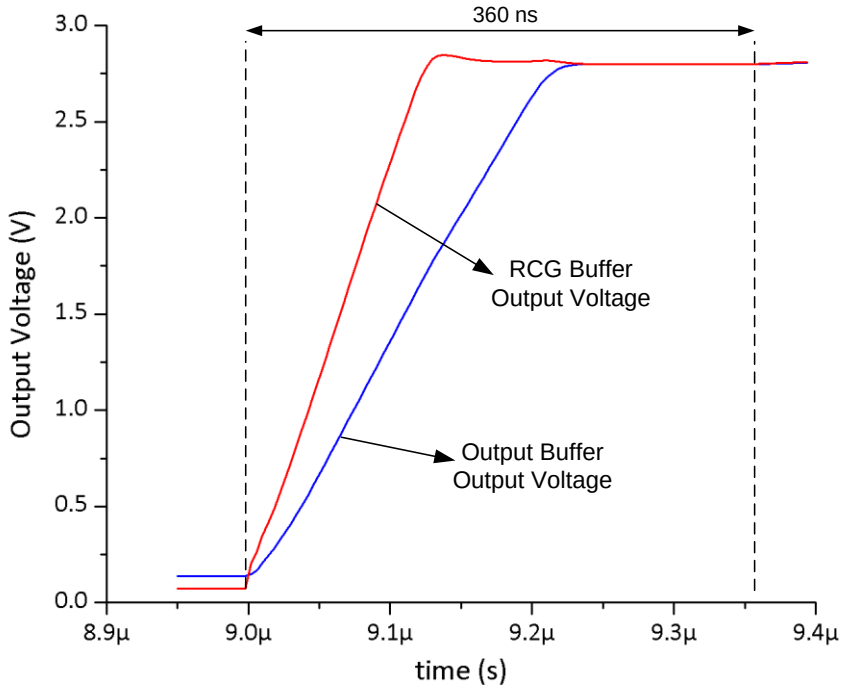
Table 3.8: Nominal bias voltages and transistor dimensions of the output buffer.

Bias Voltages (V)	
V_{DD}	5.00
V_{b1}	3.508
V_{b2}	3.50
V_{b3}	3.00
V_{b4}	1.70
V_{b5}	1.45

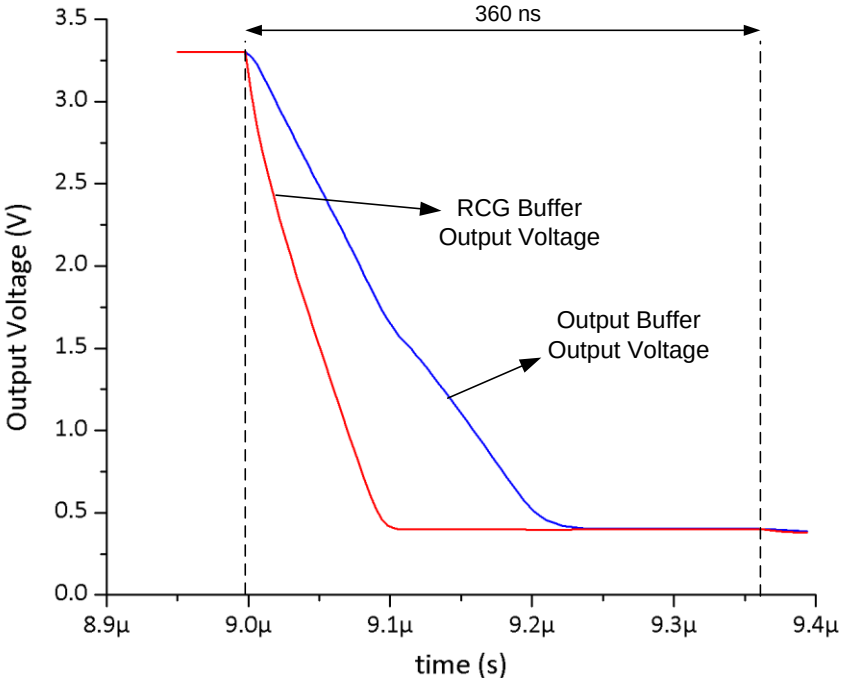
	W/L (µm / µm)
M_1, M_2	240 / 3.0
M_3	80 / 5.8
M_4	2.5 / 6.0
M_5	2.8 / 6.0
M_6, M_7	67.5 / 4.0
M_8, M_9	120 / 1.8
M_{10}, M_{11}	120 / 1.8
M_{12}, M_{13}	80.4 / 1.8
M_{14}, M_{15}	80.4 / 1.8
M_{16}, M_{17}	40 / 1.2

Table 3.9: Simulated parameters of the output buffer opamp. The results are obtained using the nominal bias voltages.

DC Gain	76.17 dB
Noise in Unity Gain Buffer Connection (0.1 Hz – 10 MHz)	36.1 µV
Output Range	0.5 V – 3.9 V
Phase Margin (with 5 pF load capacitance)	80.10°
Gain Margin	17.76 dB
Total DC power	841.9 µW
0.02% Output Settling (From 3.3 V to 0.4 V)	270 ns
0.02% Output Settling (From 0 V to 2.8 V)	265 ns



(a)



(b)

Figure 3.24: Transient simulation results of the output buffer with a 5 pF output load, with its input changing from (a) 0 V to 2.8 V, and (b) 3.3 V to 0.4 V.

Figure 3.25 shows the layout of the output buffer opamp, which occupies an area of 271 µm x 66 µm in a standard CMOS process. Similar to the RCG buffer opamp, the transistor layouts are drawn interdigitated in order to minimize the effect of mismatches.

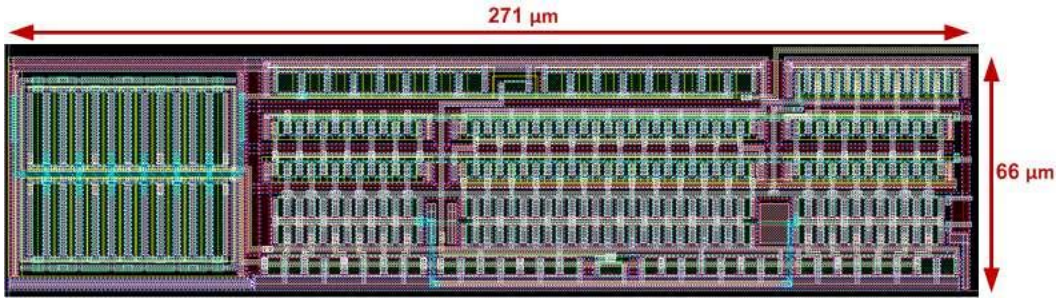


Figure 3.25: Layout of the output buffer opamp, which occupies an area of 271 µm x 66 µm in a standard CMOS process.

3.3.2.3 Bias Correction DAC Buffer

The buffers in the bias correction DAC structure are used to buffer the outputs of the first stage DAC. The load at the output of these buffers is a resistive ladder as described in Section 2.3.2; therefore, single stage opamps are not suitable to be used as DAC buffers due to their high output resistance. Two stage opamps have low output resistance, and therefore, they are suitable for driving resistive loads. Another important aspect of the DAC buffer is the output noise, since it directly adds up to the voltage noise at the gate of the injection transistor. A simple topology with minimum number of transistors is chosen in order to provide low noise operation. Figure 3.26 shows the schematic of the bias correction DAC buffer, which is a simple two-stage opamp. Table 3.10 gives the nominal bias voltages and transistor dimensions of the bias correction DAC buffer, and Table 3.11 lists the parameters obtained from simulations.

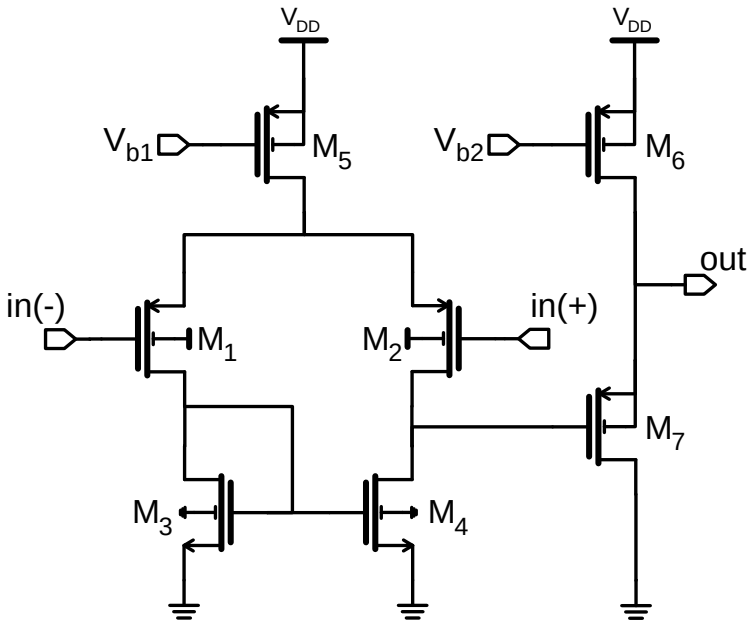


Figure 3.26: Schematic of the bias correction DAC buffer opamp.

Table 3.10: Nominal bias voltages and transistor dimensions of the bias correction DAC buffer opamp.

Bias Voltages (V)	
$\mathbf{V_{DD}}$	5.00
$\mathbf{V_{b1}}$	3.508
$\mathbf{V_{b2}}$	3.508 for V_{max} 3.80 for V_{min}

	W/L (µm / µm)	***# of Gates***
$\mathbf{M_1, M_2}$	120 / 3.0	6
$\mathbf{M_3, M_4}$	120 / 15	3
$\mathbf{M_5}$	7.0 / 6.0	1
$\mathbf{M_6}$	16 / 6.0	1
$\mathbf{M_7}$	120 / 3.0	15

Table 3.11: Simulated parameters of the DAC buffer opamp. The results are obtained using the nominal bias voltages.

DC Gain (with maximum load)	57.53 dB
Noise in Unity Gain Buffer Connection (0.1 Hz – 10 kHz)	1.82 µV
Output Range	1.2 V – 4.1 V
Phase Margin	79.20°
Gain Margin	Phase does not reach -180°
Total DC power	111.7 µW for V_{max} buffer 51.7 µW for V_{min} buffer
Settling Time (V_{min} to V_{max}, ΔV = 310 mV)	330 ns
Settling Time (V_{max} to V_{min}, ΔV = 310 mV)	300 ns

The buffer that provides the minimum voltage draws current from the resistive ladder while the other one supplies this current. In order to compensate for the current difference in the output stages, the minimum voltage buffer is designed with a lower output stage current. The amount of the current difference depends on the output range of the second stage, and the nominal values are chosen assuming a 280 mV output range. Nevertheless, the currents can be adjusted for different output range values such that the output stage currents of the buffers are equal to each other.

Figure 3.27 shows the layout of the bias correction DAC buffer opamp, which occupies an area of 155 µm x 64 µm in a standard 0.6 µm CMOS process. The transistors M_3 and M_4 have large dimensions in order to minimize the flicker noise of the opamp.

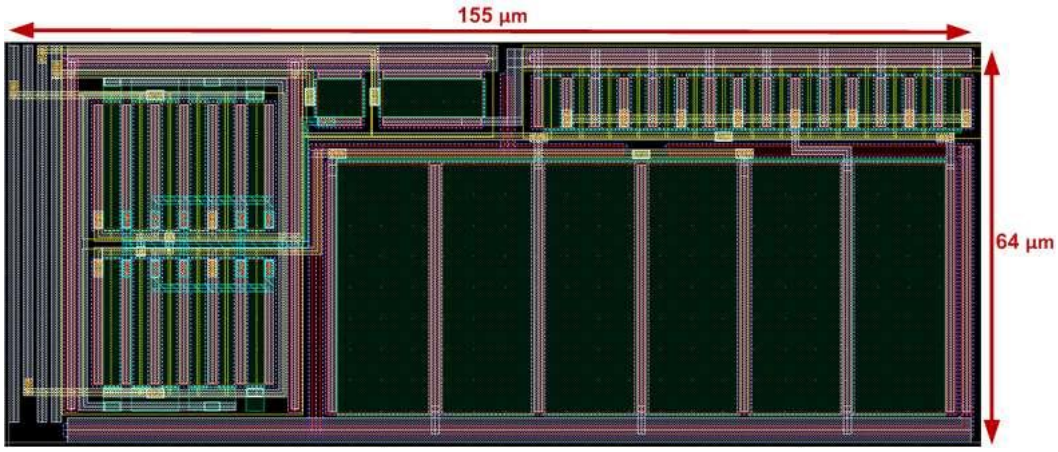


Figure 3.27: Layout of the bias correction DAC buffer opamp, which occupies an area of 155 µm x 64 µm in a standard 0.6 µm CMOS process.

3.3.2.4 CTIA Output Stabilization Buffer

The CTIA output stabilization is a technique that is used to increase the linearity of the integrator, as explained in Section 3.3.1.1. Setting the output voltage of the biasing circuits to a predetermined value requires that the necessary current is supplied to the biasing circuit. In order to provide the necessary current, the CTIA output stabilization line should be driven by a buffer. For this purpose, the *aopac01* model opamp, which is an IP of XFAB Company, is used. Figure 3.28 shows the connection schematic of the CTIA output stabilization buffer. As seen in the figure, the buffer input is connected to the integrator reset voltage line since the CTIA output voltage should be set to this value.

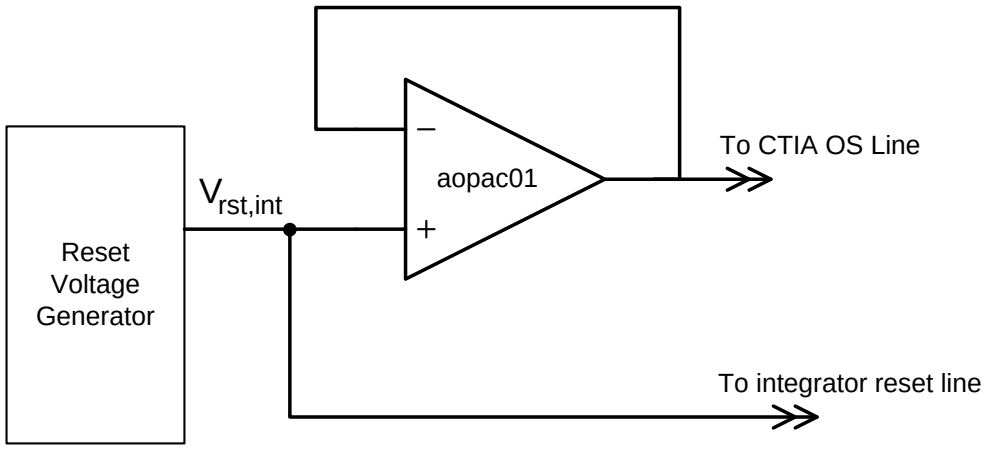


Figure 3.28: Connection schematic of the CTIA output stabilization buffer. The CTIA output stabilization is used to set the CTIA output voltage equal to the integrator reset voltage; therefore, the buffer input is connected to the integrator reset voltage line.

3.3.3 Analog Bias Generation Blocks

The bias voltages required by the injection transistors and the opamps in the readout are generated by the on-chip bias generation blocks. There are four different bias generation blocks: (i) Injection transistor bias generator, (ii) Opamp bias generator, (iii) Reset voltage generator, and (iv) Bandgap reference circuits. The first three of these circuits are resistive ladder DACs, and their outputs can be controlled using the control interface. The output voltages of the bandgap reference circuits are constant, and they are used to generate the critical bias voltages since they provide a supply and temperature independent output.

3.3.3.1 Injection Transistor Bias Generator

The gate voltages of the injection transistors in the preamplifier circuit are used to bias the detector and reference pixels. The bias voltages of the PMOS

injection transistors are common and generated only by the injection transistor bias generator block. On the other hand, NMOS injection transistors are normally biased by the bias correction structure; however, the 384x288 FPA readout has the option to bias these transistors with a common voltage, which is also generated by this block.

The injection transistor bias generator consists of two resistive ladder DACs, which provide control over the detector and reference pixel bias voltages. The important parameters of the block that are obtained from simulations are listed in Table 3.12.

Table 3.12: The important parameters of the injection transistor bias generator block obtained from simulations.

	Resolution	***Range***	***Unit Res.***	***Power***	***Max. rms Noise (0.1 Hz – 10 kHz)***
$\mathbf{V_{bias,p}}$	17.6 mV	2.60 V – 3.15 V	100 Ω	0.89 mW	1.08 μV
$\mathbf{V_{bias,n}}$	20.5 mV	2.18 V – 2.82 V	100 Ω	1.02 mW	1.00 μV

The injection transistor bias circuit has relatively high power dissipation due to relatively low resistance values. Low resistance values are preferred in order to reduce the thermal noise, which is critical for the injection transistor gates as stated in Section 2.3.3.

3.3.3.2 Opamp Bias Generator

The opamp bias generator is used to generate the bias voltages required by the opamps in the readout channels, output buffering structure, and bias correction DAC structure. It is possible to generate these voltages locally within each

opamp; however, this method is not preferred for two main reasons. First of all, same type opamps are biased with same voltages in the FPA readout; therefore, a single block is sufficient to bias a specific node of all same type opamps. The other reason is the lack of controllability when the voltages are generated locally. Biasing the opamps using a separate DAC block provides control over the bias voltages, and hence some important parameters such as the output slew current.

Figure 3.29 shows the simplified schematic of the opamp bias generator block, which consists of 6 resistive ladder DACs connected in series together with some resistors. Table 3.13 summarizes the range, resolution, and resistance data together with the bias voltages generated by each DAC within the opamp bias generation block. The noise and the time constant of this block are not critical; therefore, high resistance values are used in the resistive ladder. As a result, the total power dissipation is very low as seen in Table 3.13.

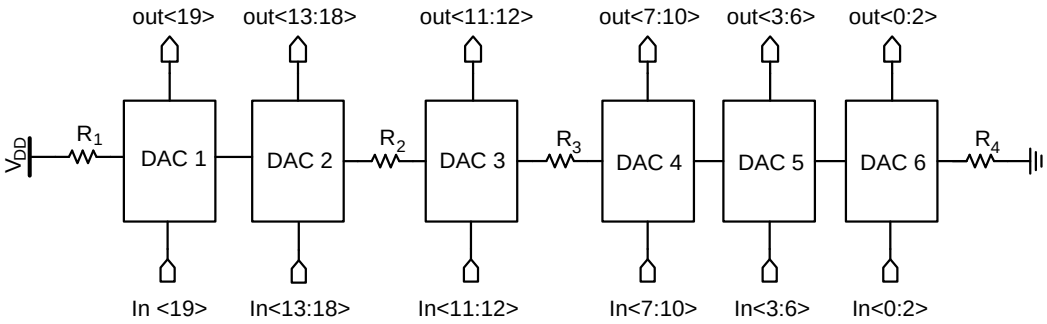


Figure 3.29: Simplified schematic of the opamp bias generator block, which consists of 6 resistive ladder DACs connected in series together with some resistors. The extra resistors are used to adjust the output ranges of the DACs.

Table 3.13: The range, resolution and power dissipation of the DACs in the opamp bias generator block together with the list of generated bias voltages by each DAC.

DAC Number	*Range (V)*	*Resolution*	*Generated Voltages*
1	1.19 - 1.33	3 bits - 20 mV	- Integrator V_{b1} - S&H V_{b1} - S&H V_{pwr}
2	1.35 - 1.50	2 bits - 50 mV	- Integrator V_{b3} - S&H V_{b3} - RCG buffer V_{b5} - Output buffer V_{b5}
3	1.55 - 1.90	3 bits - 50 mV	- Integrator V_{b2} - S&H V_{b2} - RCG buffer V_{b4} - Output buffer V_{b4}
4	2.95 - 3.10	2 bits - 50 mV	- RCG buffer V_{b3} - Output buffer V_{b3}
5	3.45 - 3.59	3 bits - 20 mV	- RCG buffer V_{b1} - RCG buffer V_{b2} - Output buffer V_{b1} - Output buffer V_{b2} - DAC buffers V_{b1}; - DAC V_{max} buffer V_{b2}
6	3.61 - 3.91	4 bits - 20 mV	- DAC_V_{min} buffer V_{b2}

3.3.3.3 Reset Voltage Generator

The non-inverting terminals of the integrator and S&H opamps are connected to a predetermined DC voltage, which is called the reset voltage. During the integration reset and sampling phases, these opamps are in unity gain configuration, and the inverting terminal is also set to the same voltage. By this method, the opamps are switched to their linear region, which is then preserved by the negative feedback for a proper operation. The absolute values of the

reset voltages are not important; however, it should be ensured that they are within the input common mode range of the opamp.

The reset voltage generator is a resistive ladder DAC with two outputs, one for the integrator and the other for the S&H reset voltages. The range and resolution of the block are equal to 0.3 V and (1.9 V - 2.8 V), respectively.

3.3.3.4 Bandgap Reference Circuits

Bandgap reference circuits are used to generate stable voltages that are almost independent of supply voltage and temperature. Therefore, the voltages that determine the quiescent currents of the opamps have the option to be biased by bandgap references as well as the opamp bias generation block. The reference circuit used in the 384x288 FPA readout is the combination of *abgpc01* and *abiac03* cells, which are IPs of the X-FAB Semiconductor Foundries. Besides, *abiac05* cell is used to bias the CTIA OS line buffer, which is also an IP of the same company.

The output voltages of the *abgpc01* – *abiac03* combination are 1.27 V and 3.508 V, and the nominal values of the bias voltages are chosen accordingly during the design.

3.3.4 Bias Correction DAC Structure

In the 384x288 FPA readout, the improved bias correction DAC structure described in Section 2.3 is implemented for each RCA. The structure includes both analog and digital blocks. This section presents the analog blocks, and the digital parts will be described in Section 3.4.4.

3.3.4.1 First Stage of the Bias Correction DAC

The first stage of the bias correction DAC is a 5-bit resistive ladder connected in series with two extra resistors that adjust the output range. Table 3.14 lists the important parameters of the first stage.

Table 3.14: Important parameters of the first stage of the bias correction DAC structure.

Range	1.1 V – 4 V
Resolution	94 mV
Power Dissipation	1.99 mW
Maximum Noise (0.1 Hz – 20 kHz)	0.71 μV

The outputs of the first stage DAC are buffered using the opamp given in Section 3.3.2.3, and they are used to bias the resistive ladders in the second stage.

3.3.4.2 Second Stage of the Bias Correction DAC

The second stage of the bias correction structure includes a 5-bit resistive ladder and in-channel DSNs as described in Section 2.3.2. There is also an extra bit that is used to turn off the bias voltages of the defective pixels with very low resistance, which may draw large currents and affect the other readout channels. Figure 3.30 shows the simplified schematic of the second stage of the bias correction DAC structure, and Table 3.15 lists its important parameters.

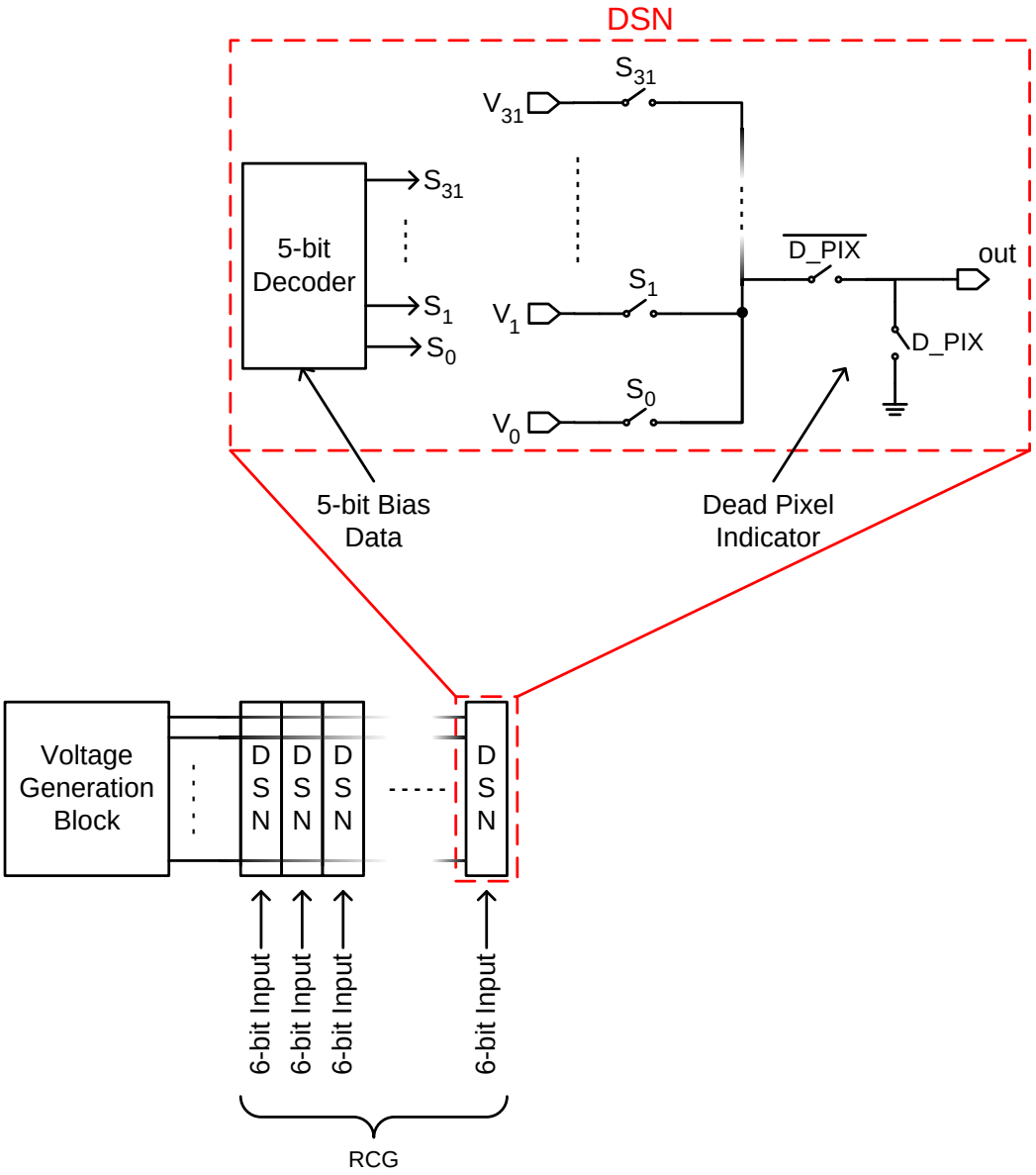


Figure 3.30: Simplified schematic of the second stage of the bias correction DAC structure. The generated voltages are routed to all readout channels within the same RCG, and the DSNs select the appropriate voltage. There is also a dead pixel indicator, which is used to turn off the bias in case of an excessively low pixel resistance.

Table 3.15: The important parameters of the second stage of the bias correction structure. The results are obtained from simulations for nominal output range of 280 mV. The rms noise depends on the output voltage, and its maximum value is given in the table.

Minimum Resolution	2.94 mV
Power Dissipation for each RCG	163 µW
Total Power Dissipation	1.30 mW
Maximum rms Noise including the first stage (0.1 Hz – 10 kHz)	2.40 µV

3.3.5 Analog Multiplexers

In order to increase the controllability and observability of the bias voltages, an analog multiplexing circuitry is implemented in the 384x288 FPA readout. Figure 3.31 shows the simplified structure of an analog multiplexer. Each analog bias voltage in the readout is taken from the output of an analog multiplexer, which connects the node either to an internal bias generation circuit or a bonding pad. With this method, the bias voltages can be controlled directly from outside of the chip when it is necessary. The switches in the multiplexer can be controlled independently; therefore, it is also possible to observe the internally generated voltages by connecting its output to a bonding pad.

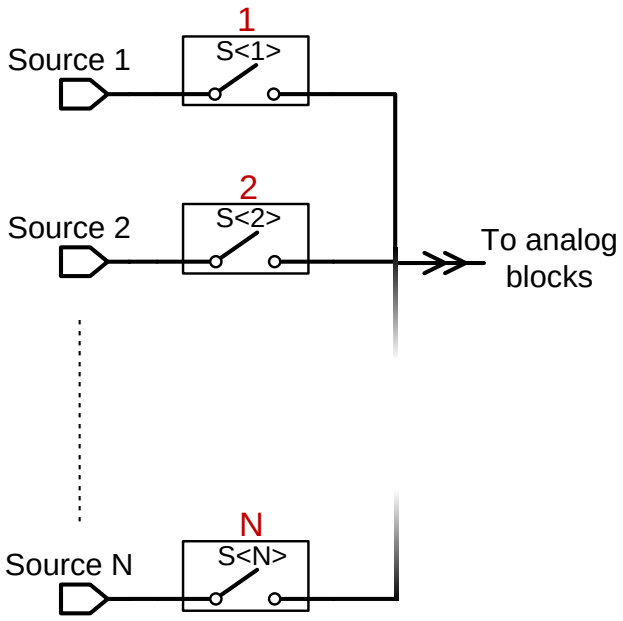


Figure 3.31: Schematic of an analog multiplexer with N inputs. The switches can be controlled independently; therefore, it is possible to connect the two inputs to each other.

3.4 Digital Blocks

The digital blocks in the 384x288 FPA readout are used to generate the timing signals, to operate the bias correction DACs, and to configure the chip. There are seven main digital blocks that will be described in this section: (i) readout channel control signal block, (ii) row signals block, (iii) row select decoder, (iv) bias correction DAC input module, (v) output multiplexer block, (vi) reference row selection block, and (vii) control interface block*. Besides these blocks, the readout channels also include small digital circuitry for the high current mode control and bias correction data storing, which is also presented in this section. All digital blocks are implemented using the digital gates that are IPs of X-FAB Semiconductor Foundries.

* Gate level design and layout of the first five of these blocks are completed by Alp Oğuz.

3.4.1 Readout Channel Control Signal Block

The readout channel control signal block generates the digital signals that control the operation of the readout channels. Table 3.16 lists the digital signals generated by this block together with their functions.

Table 3.16: Digital signals generated by the readout channel control signal block together with their functions.

Signal	***Explanation***	***Connected to***
INT_RST	Resets the integrator.	Integrator
INT_ENB	Enables the integration.	Integrator
SH	Starts sampling of the integrator output.	Sample and Hold
SH_PW_1	Switches all S&H opamps in the same RCA to high current mode.	Sample and Hold
DACD_TRANSFER	Transfers the data in storing RAMs to the active RAMs of bias correction DAC.	Bias correction DAC RAM
DACD_NBIAS_LOAD	Connects the bias correction DAC output to the gate of the NMOS injection transistor.	Bias correction DAC RAM
DACD_LOAD	Starts the operation of bias correction data shift register.	Bias correction data shift register
ROW_ENB	Enables the pixel bias.	Row selection circuitry
CTIA_OS	Enables CTIA output stabilization.	Integrator

The readout channel control signal block has four external inputs that determine the timing of the output signals. Besides these inputs, the outputs of the readout channel control signal block can be configured for different operation modes using the configuration data stored in the control interface block. Table

3.17 and Table 3.18 list the timing and configuration inputs, respectively; and Table 3.19 gives the timing information of the readout channel control signals. The timing of the readout channel control signals are also visualized in Figure 3.32.

Table 3.17: External inputs of the readout channel control signal block that determine the timing of the outputs.

Timing Inputs	***Explanation***
CLK	External clock of the chip. Its frequency determines the frame rate; 50 fps operation needs 5.53 MHz clock frequency.
FSYNC	The frame synchronization signal. Every frame starts with an FSYNC signal. Rises at the positive edge of CLK.
LSYNC	The line synchronization signal. Every row begins with an LSYNC signal. Rises at the positive edge of CLK.
RN	Global reset signal of the chip. (Active low)

Table 3.18: Configuration inputs of the readout channel block that determine the operation modes of the readout channels.

Configuration Inputs	***Explanation***
Int_Rst_Drtn<4:0>	Defines the negative edge of the **INT_RST** output.
Sh_Wait<7:0>	Defines the positive edge the **SH** output
Sh_End<7:0>	Defines the negative edge of the **SH** output
Pw_ Diff<3:0>	Defines the differences between the rising and falling edges of the **SH_PW1** and **SH** outputs in terms of clock pulses.
Sh_Pw_Req	Determines if the high current mode will be activated during sampling. (Active high)
Ctia_Os<1:0>	Defines the duration of the **CTIA_OS** signal in terms of clock pulses. When it is zero, CTIA O. S. is disabled.

Table 3.19: Timing information of the outputs of the readout channel control signals block. The columns Rise Ref. and Fall Ref. indicate the reference points for the rise and fall of the output, respectively; and Rise Delay and Fall Delay columns indicate the delay of the rising and falling edges of the output after the reference point in terms of clock pulses, respectively.

Output	***Rise Ref.***	***Rise Delay (CP)***	***Fall Ref.***	***Fall Delay (CP)***
INT_RST	LSYNC Rising	1	LSYNC Rising	1 + Int_ Rst_Drtn
INT_ENB	INT_RST Rising	2 x Ctia_Os	LSYNC Falling	0.5
SH	INT_RST Rising	2 x Sh_Wait	INT_RST Falling	2 x Sh_End
SH_PW_1	INT_RST Falling	2 x (Sh_Wait–Pw_Diff)	INT_RST Falling	2 x (Sh_End+Pw _Diff)
DACD_TRANSFER	LSYNC Rising	0.5	LSYNC Falling	0.5
DACD_NBIAS_LOAD	LSYNC Rising	1.5	LSYNC Falling	2.5
DACD_LOAD	LSYNC Rising	0.5	LSYNC Rising	2.5
ROW_ENB	INT_RST Rising	0	LSYNC Falling	2.5
CTIA_OS	INT_RST Rising	0	INT_RST Falling	2 x Ctia_Os

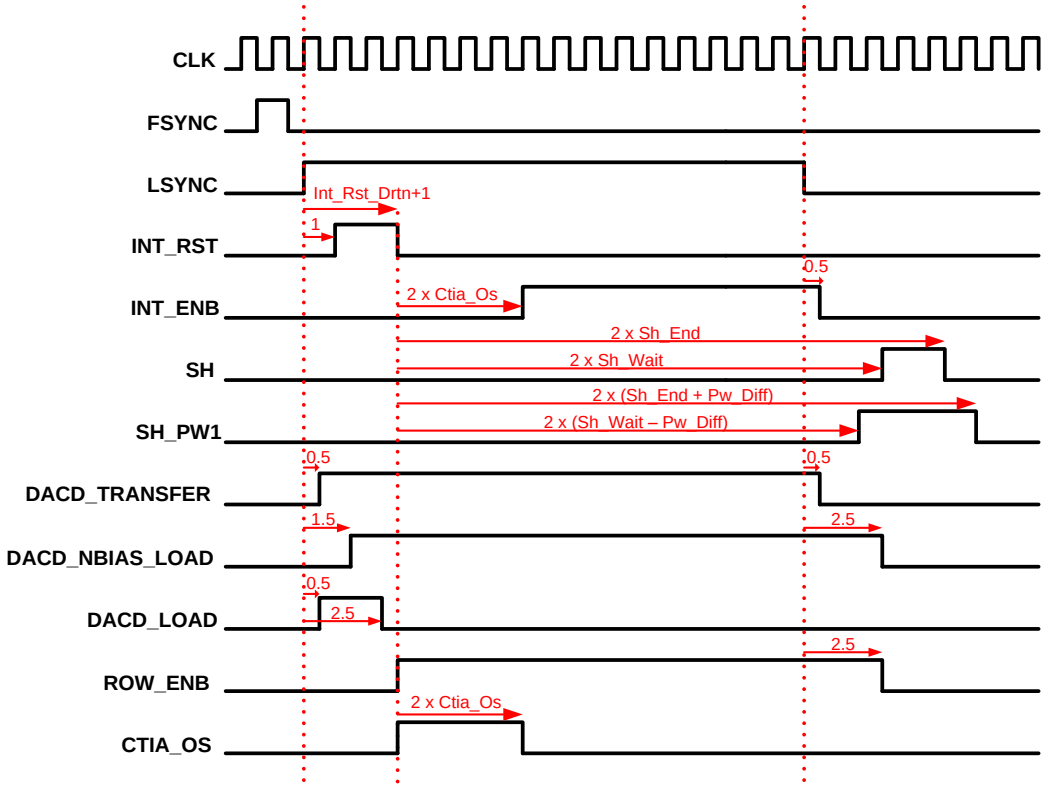


Figure 3.32: Inputs and corresponding outputs of the readout channel control signals block. The reference points, delay times and durations of the outputs are labeled on the figure.

3.4.2 Row Signals Block

Row signals block generates the inputs of the row select decoder, which is used to connect the pixels in a specific row to the readout channels. The output of the row signals block indicates the binary representation of the number of the row to be processed. The rows are numbered from 1 to 288, where 1 is the top and 288 is the bottom row. Figure 3.33 shows the block diagram, and Table 3.20 lists the inputs and the outputs of the row signals block.

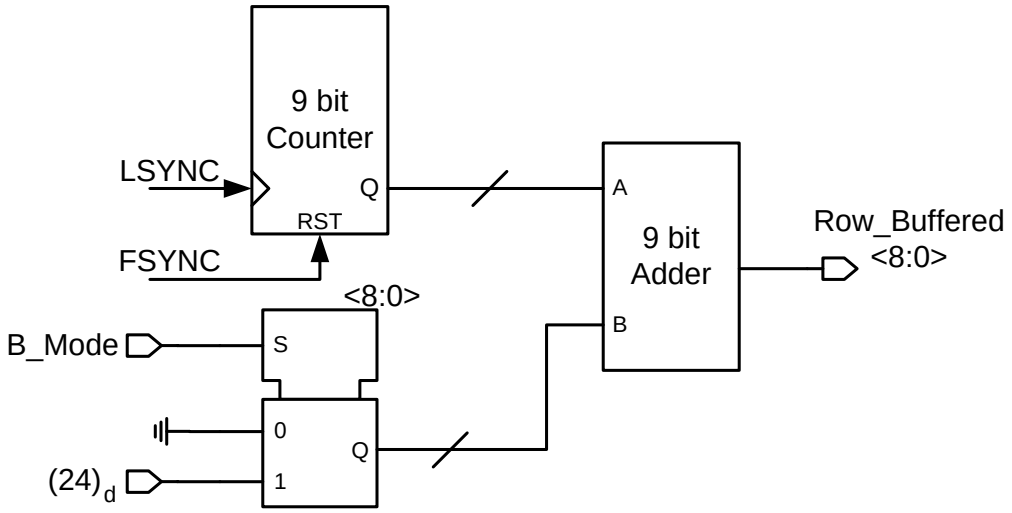


Figure 3.33: Simplified block diagram of the row signals block, which is used to generate the inputs of the row select decoder block.

Table 3.20: List of the inputs and outputs of the row signals block.

Signal	***Explanation***
CLK	External clock of the chip.
CLK_BAR	Complement of the CLK signal.
FSYNC	Frame synchronization signal.
LSYNC	Line (row) synchronization signal.
RN	Global reset signal (Active low).
B_Mode	Single bit configuration signal. When it is low, the chip operates in 384x288 mode. Otherwise, operation mode is 320x240.
ROW_BUFFERED<8:0>	The 9 bit output signal, which indicates the number of the row to be selected.

3.4.3 Row Select Decoder

Row select decoder is simply a 9-bit decoder that controls the switches of the detector pixels. According to the output of the row signals block, only one of the outputs of this block becomes high; and the detector pixels in the corresponding row are connected to the pixel biasing circuitries in the readout channels. Table 3.21 lists the inputs and the outputs of the row select decoder.

Table 3.21: Inputs and outputs of the row select decoder block.

Signal	***Explanation***
D<8:0>	9-bit input of the row select decoder, comes from row signals block and indicates the number of the row to be selected.
DB<8:0>	Complement of D<8:0>.
ROW_ENB	Output enable signal of row select decoder.
B_Mode	Control bit used to select the active FPA size.
OUT<288:1>	Output of the row select decoder block.

3.4.4 Bias Correction DAC Input Module

Bias correction DAC input module is used to generate the signals that enable the storing of the bias correction data into the RAMs implemented in the readout channels. The module consists of a shift register and digital timing circuitry that generates the starting bit, which is called coin in this work. At the beginning of the row time, all bits of the shift register are reset; and the timing circuitry generates the coin of the shift register. The coin shifts left at every clock pulse, loading the data into the next readout channel.

Normally, it is sufficient to use a single shift register to load the bias correction data. However, in this case, a long routing line from the top RCA to the bottom RCA is necessary, which would decrease the reliability of the circuit. Instead, two independent bias correction DAC input modules are implemented for the two RCAs. The clock of the module and digital timing circuitry is designed to provide that the bias correction data is loaded into the two modules successively at each clock pulse. Figure 3.34 shows the clocking sequence of the shift registers of the two modules.

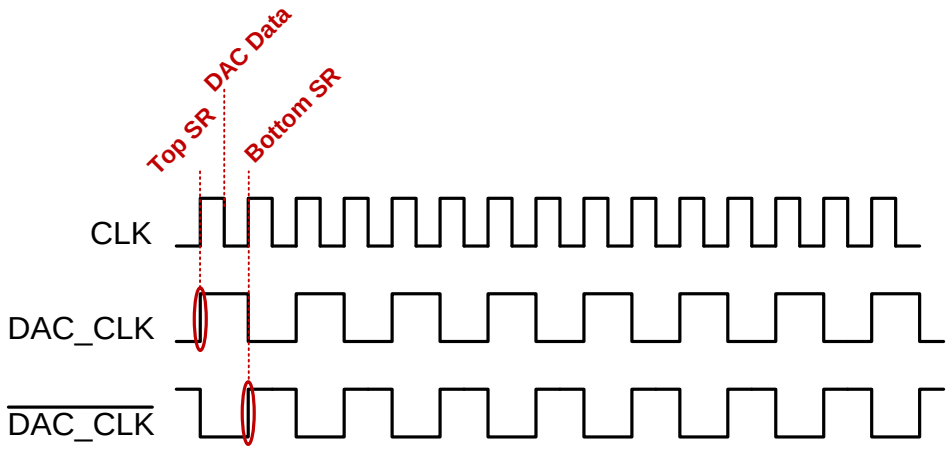


Figure 3.34: Clocking sequence of the DAC input modules. The modules use complementary clocks at half frequency of the external chip clock. Bias correction data are loaded into the bus at the falling edges of the clock; and at each rising edge, one of the modules load the data into the RAM of the corresponding readout channel.

3.4.5 Output Multiplexer

The outputs of the readout channels should be multiplexed to the output channels as explained in the previous sections. The output multiplexing

operation includes the multiplexing of the outputs of the readout channels, the RCGs, and if the chip is operated in single output mode, the output buffers. Not only the multiplexing signals, but also the high current mode control signals required during the output multiplexing are generated by the output multiplexer.

A single output multiplexer block consists of a 192-bit shift register, 4 registers for RCGs, 1 register for output buffers, and digital timing circuitry. Similar to the DAC input modules, there are two independent output multiplexer blocks in the readout. The timing signals of these modules are adjusted according to the active FPA size and number of output channels. Figure 3.35 and Figure 3.36 show the timing of the signals generated by the output multiplexer block at 384x288 active FPA size for single and dual output channel modes, respectively.

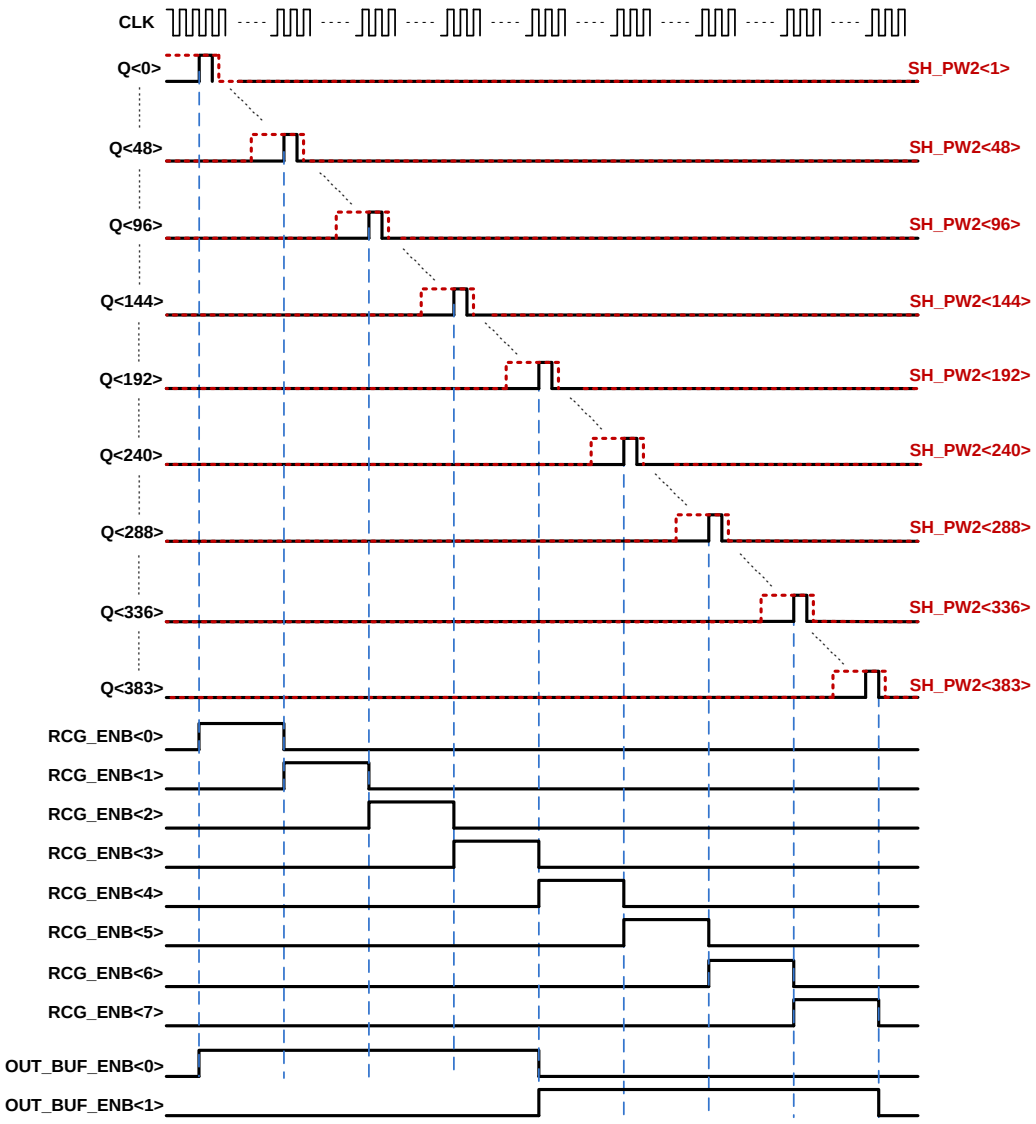


Figure 3.35: Outputs of the output multiplexer for 384x288 active FPA size and single output channel. In the figure, *Q*, *RCG_ENB* and *OUT_BUF_ENB* signals denote the output enable signals of the readout channels, RCGs and output buffers, respectively. Besides the output enabling signals, the high current mode control signal of the S&H opamps are also generated by this block during output multiplexing. The high current mode control signals are shown by red lines and denoted as *SH_PW2*.

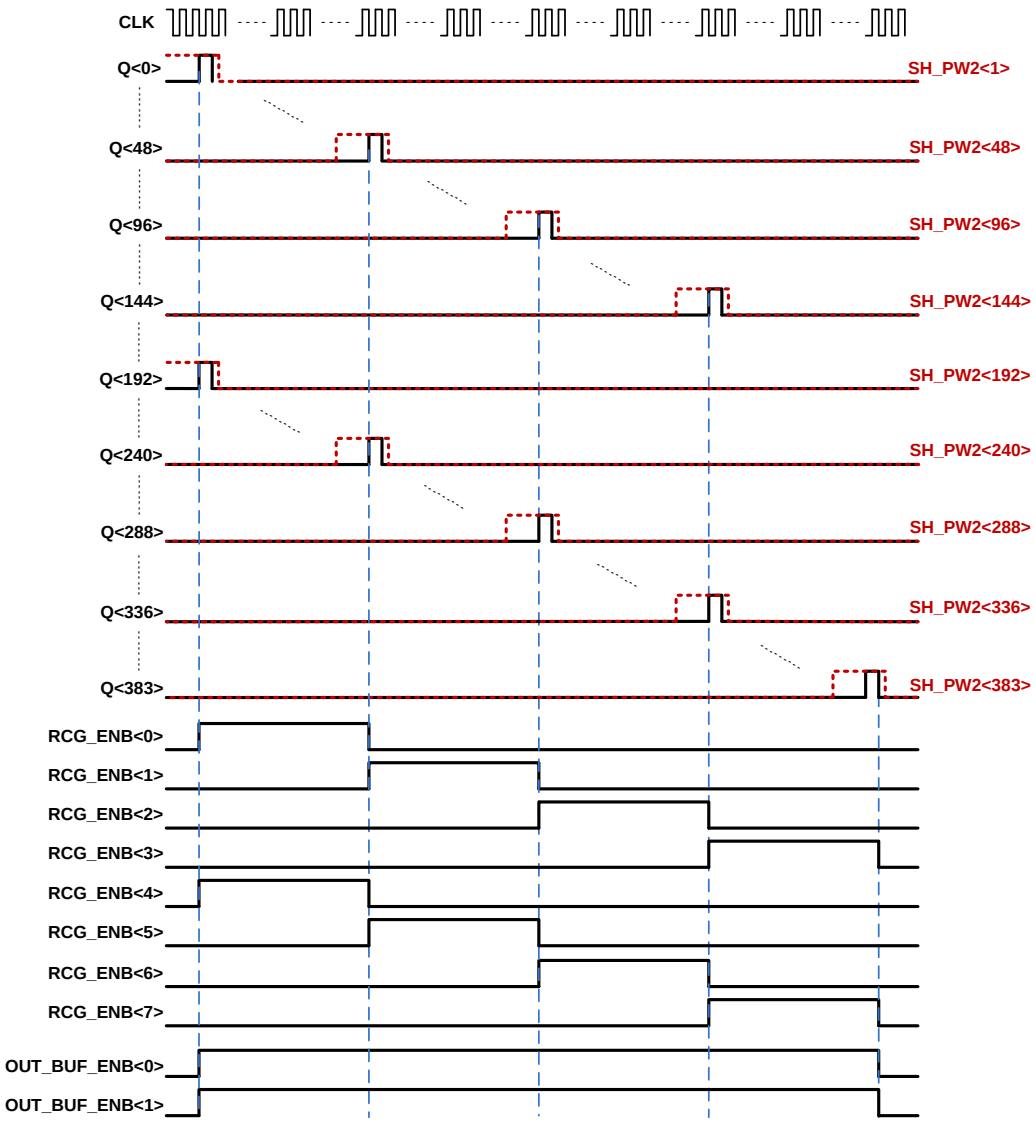


Figure 3.36: Outputs of the output multiplexer for 384x288 active FPA size and dual output channels.

3.4.6 Reference Pixel Selection Circuit

The reference pixels are used to cancel the DC portion of the detector current. The number of reference pixels used in the readout affects the addressing frequency, and hence the heating curves of the reference pixels. In order to

obtain better control on the self heating, a reference pixel selection circuit is implemented in the 384x288 FPA readout. Table 3.22 lists the inputs and the outputs, and Figure 3.37 shows the simplified block diagram of the reference pixel selection circuit, which consists of a 16-bit controllable shift register, and digital circuitry that generates the timing signals according to the selected reference rows.

Table 3.22: List of the inputs and the outputs of the reference pixel selection circuit.

Signal	***Explanation***
FSYNC	Frame synchronization signal.
LSYNC	Line synchronization signal.
RN	Active low global reset.
Selected_Rows<15:0>	A 16 bit sequence showing the reference pixels to be operated by 1 and the others with 0.
Self_Test_Enb_Bar	Complement of the Self_Test_Enb signal, which enables self test mode.
ROW_ENB	Output enable of this block.
REF_ENB_BAR<15:0>	The outputs of the reference pixel selection circuit. When an output bit is low, the corresponding reference row is connected to biasing circuitry.

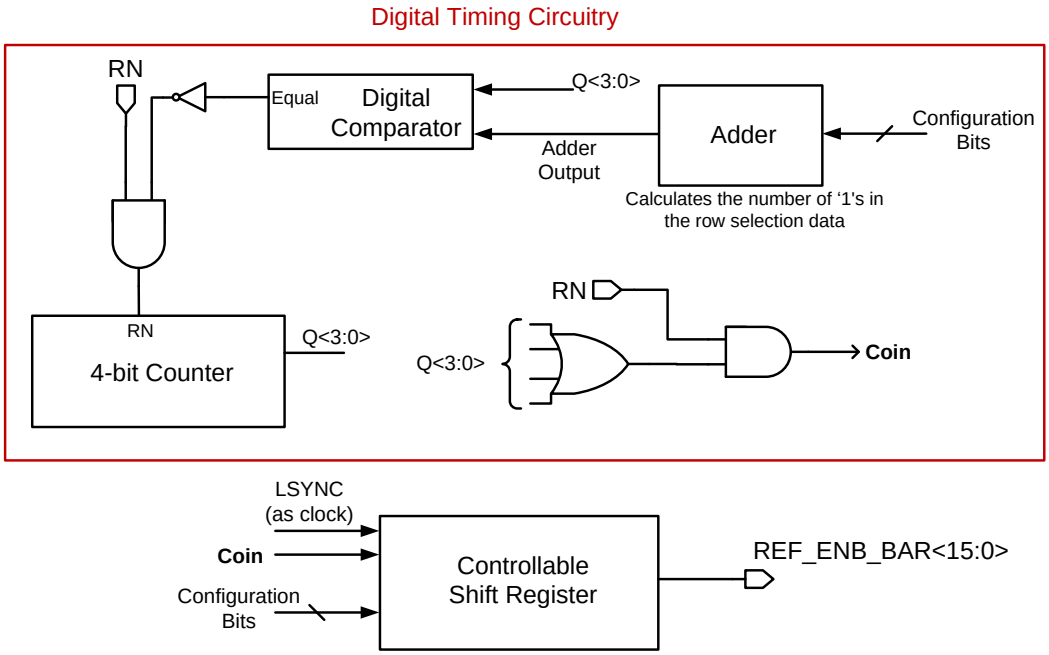


Figure 3.37: Simplified block diagram of the reference pixel selection circuit. The timing circuitry determines the starting time of the controllable shift register, which enables the selected rows sequentially.

The controllable shift register directly disables the unselected reference pixels and provides a circular operation sequence between the selected ones. Instead of directly shifting the coin, this circuit has a bypassing structure that enables the transfer of the coin from one selected row to the next one even if there are unselected rows between the two. Figure 3.38 shows the basic unit of the controllable shift register, and a sample operation sequence for a specific configuration is presented in Figure 3.39.

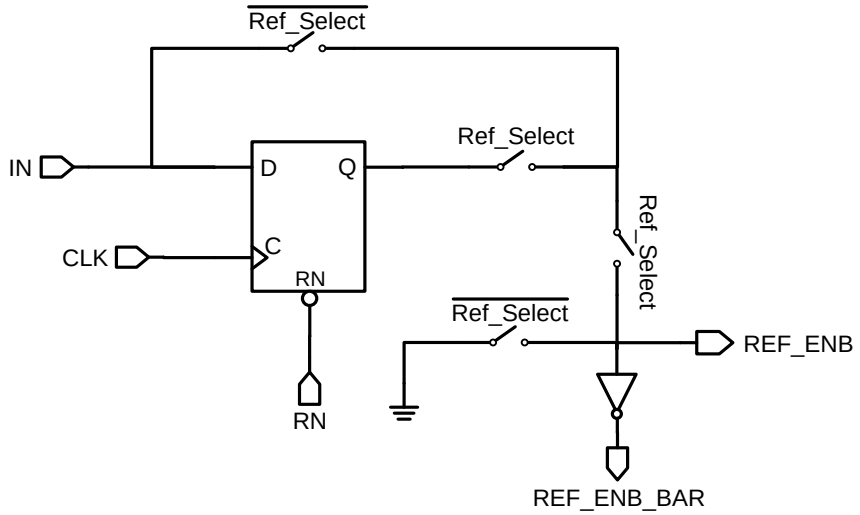


Figure 3.38: Schematic of the basic unit of the controllable shift register block of the reference pixel selection circuit. The switches are used to disable the unselected reference rows, and bypass the D flip-flop so that the coin moves to control register of the next selected row.

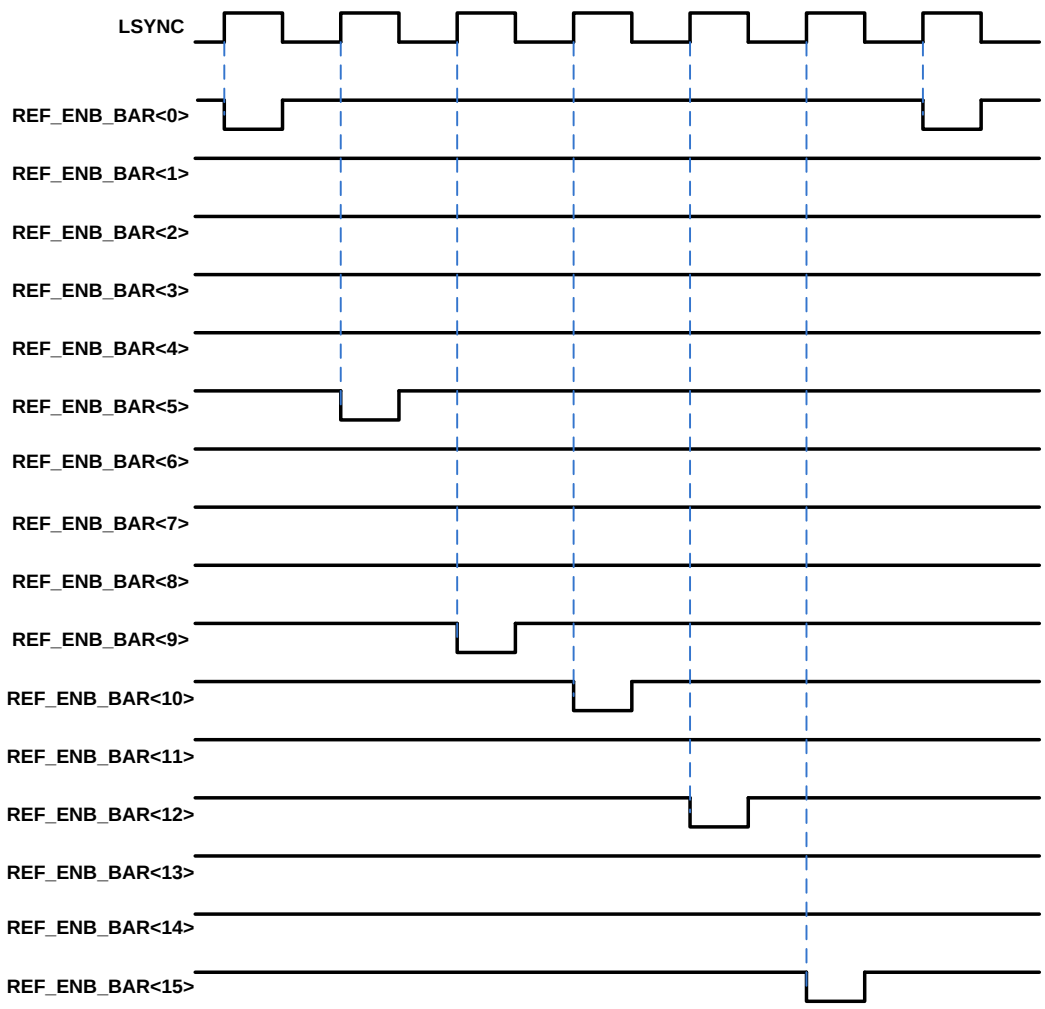


Figure 3.39: Outputs of the reference row selection circuit for a configuration where the rows 0, 5, 9, 10, 12, and 15 are selected. The corresponding 16-bit configuration input is $_0(1000010001101001)_{16}$, with 1's for selected rows and 0's for the others.

3.4.7 Control Interface Block

There are several control parameters in the 384x288 FPA readout such as the active pixel size, number of output channels, bias voltages, and test modes. It is not feasible to control every parameter directly from dedicated bond pads since it requires lots of pads, and hence, extra silicon area. Instead, a serially

programmable 31-byte RAM, which is named as the control interface, is implemented in order to store the configuration data. Table 3.23 lists the inputs and outputs of the control interface block, and Figure 3.40 shows its block diagram, which consists of a 31-byte RAM, an address decoder, and latching circuitry.

Table 3.23: List of the inputs and the outputs of the control interface block.

Signal	***Explanation***
SI_ENABLE	Enables the programming operation.
S_DATA_IN	Single bit serial data input.
Addr_In<4:0>	5 bit address data. Used to select the memory address to be programmed.
CLK	System clock.
RN	Active low global reset.
SI_OUT	Single bit serial data output. Used for testing the shift register operation.

The serial input bit of the control block is routed to the inputs of each byte in the RAM, and the addressing circuitry provides that only the byte at the selected address takes the given input. Each byte consists of a shift register for taking the serial input and an 8-bit register with parallel load for storing the data. Figure 3.41 shows the simplified schematic of a byte in the serial control interface RAM. The two-stage structure shown in the figure ensures that the configuration bits become active only after the whole word is completed. This precaution prevents any unwanted states during the shifting operation. There is also a multiplexing circuitry that is used to load the default values to the RAM at every reset operation.

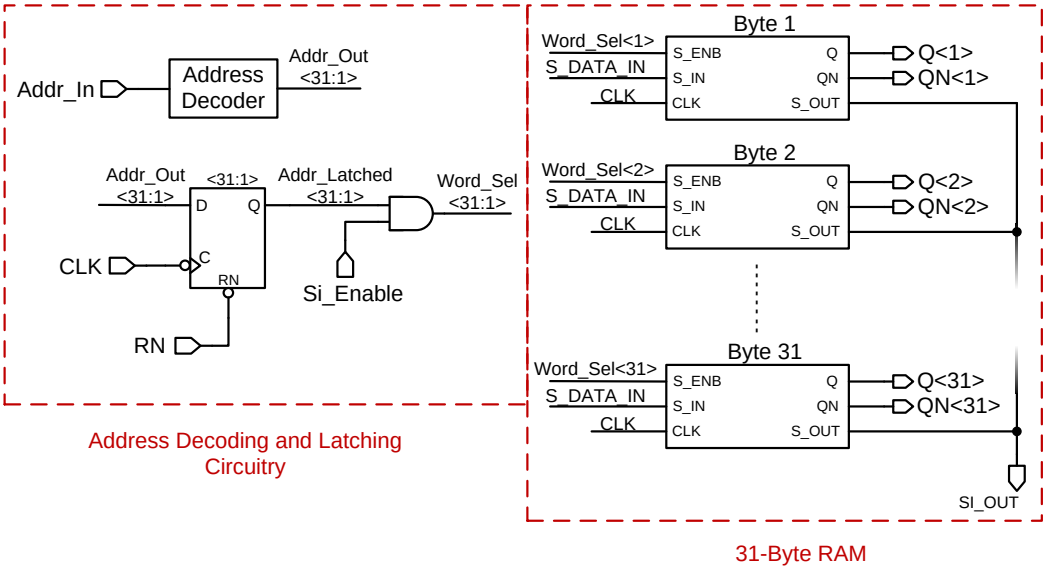


Figure 3.40: Block diagram of the control interface block, which consists of a RAM, and an address decoder and latching circuitry.

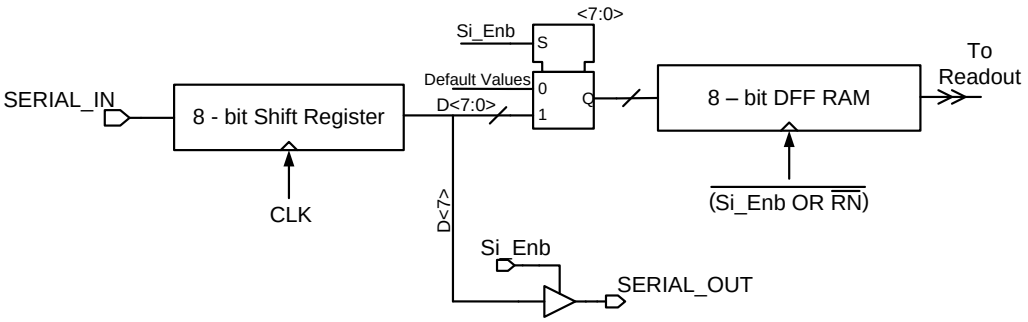


Figure 3.41: Simplified schematic of a byte in the control interface block RAM. The multiplexer is used to load the default values to the RAM when the chip is reset.

The control interface can be programmed serially when the enable bit is set to high. The data is transferred into the addressed RAM when the address data

changes or the enable bit go low. Figure 3.42 shows a sample programming sequence with labels showing the critical timing information.

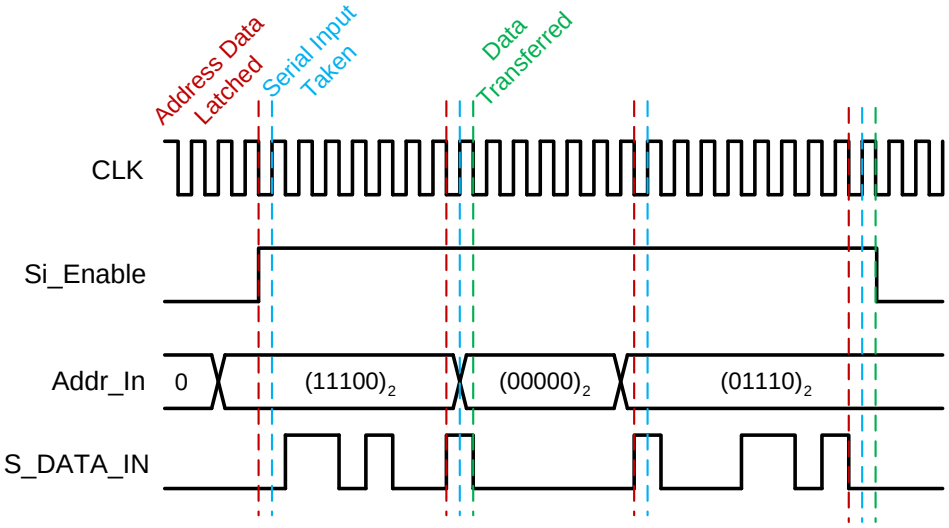


Figure 3.42: Sample programming sequence of the control interface with labels showing the critical timing information.

3.4.8 In-Channel Digital Circuitry

As well as the separate digital blocks presented in the preceding sections, there are also two digital blocks within the readout channels: the bias correction RAMs and high current mode control circuit. The bias correction RAM is a two-stage structure that is used to sample and store the bias correction data for each readout channel. The high current mode control circuit is used to activate the high current mode for the S&H opamp within the readout channel.

Figure 3.43 shows the block diagram of the bias correction RAM, which consists of two 5-bit D flip-flop type RAMs with parallel load, one named as the storage

RAM and the other as the active RAM. The operation sequence of this block is as follows: The storage RAM reads the bias correction data of the next row pixels during the readout of a row. The sampling signals of the storage RAM are generated by the bias correction DAC input modules as described in Section 3.4.4. The stored data is transferred to the active RAMs at the beginning of the row readout time. The outputs of the active RAMs are directly connected to the in-channel DSN, which connects the desired bias voltage to the gate of the NMOS injection transistor. By using a two-stage structure, it is possible to use a full row time for loading the bias correction data, which is similar to the purpose of using S&H blocks.

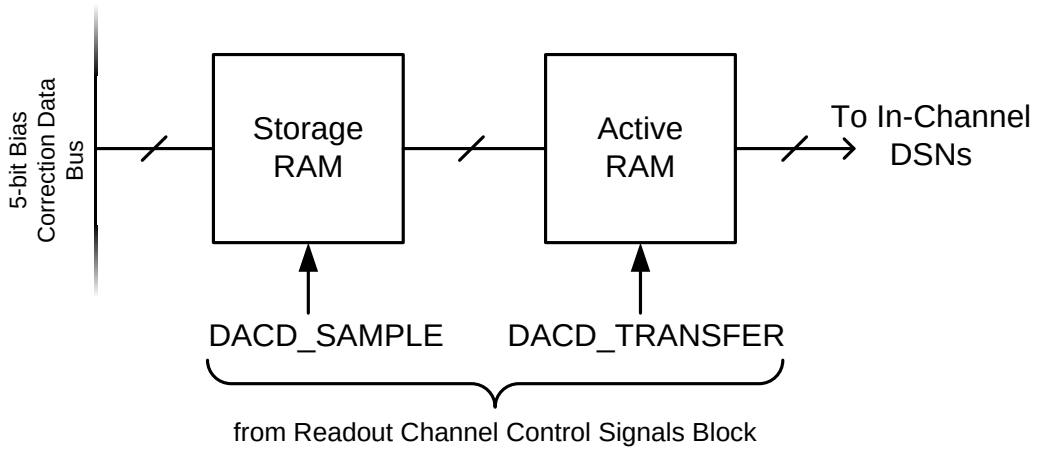


Figure 3.43: Block diagram of the in-channel bias correction DAC RAM structure.

The other digital block within the readout channels is the high current mode control circuit, which is used to activate the high current mode of the S&H opamp within the readout channel. Figure 3.44 shows the schematic of this block. As stated in Section 2.2.3, the high current mode is activated during the output multiplexing, and optionally during the sampling operation, in order to remove the offset caused by the shifting in the DC operation points of the

opamp. The high current mode activation circuit generates two non-overlapping signals using the control signals generated by the readout channel control signals block (*SH_PW1*) and the output multiplexer (*SH_PW2*). These signals control two switches, which connect the V_{pwr} input of the S&H opamp to either V_{pwr} voltage generated by analog bias generators or to ground. The signals are designed to be non-overlapping in order to prevent any short circuit between the V_{pwr} and ground during mode transitions.

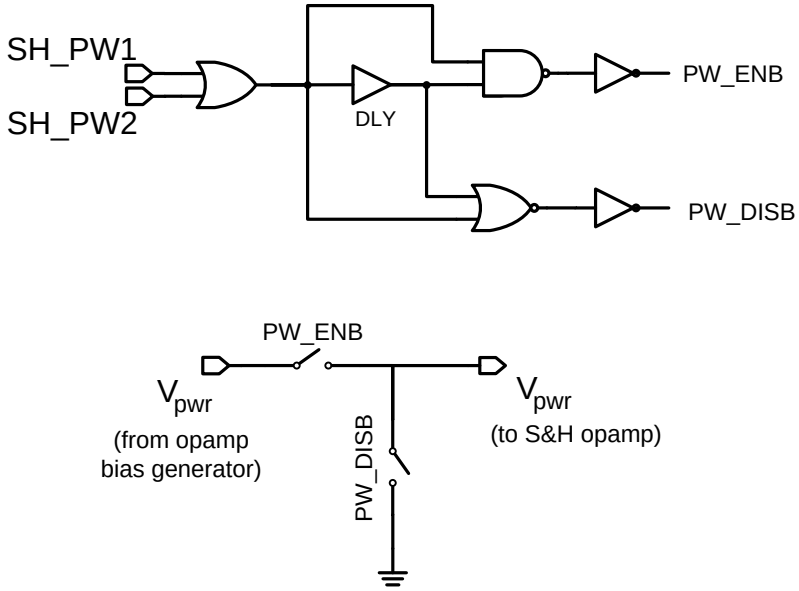


Figure 3.44: Schematic of the high current mode control circuit.

3.5 Floor Planning and Layout of the FPA Readout

Figure 3.45 shows the floor plan, and Figure 3.46 shows the final layout of the 384x288 resistive microbolometer FPA. The FPA is fabricated in a 0.6 µm standard CMOS process and occupies an area of 17.84 mm x 16.23 mm.

The readout has total 89 bond pads; however, most of these pads are for testing purposes. The number of the pads required during the operation of the FPA is 32: 10 of these pads are for digital timing signals, 2 for programming the control interface, 4 for two differential outputs, and remaining 16 pads are for supply voltages. The pad frame also includes an ESD protection scheme, which is implemented using the I/O cells that are IPs of XFAB.

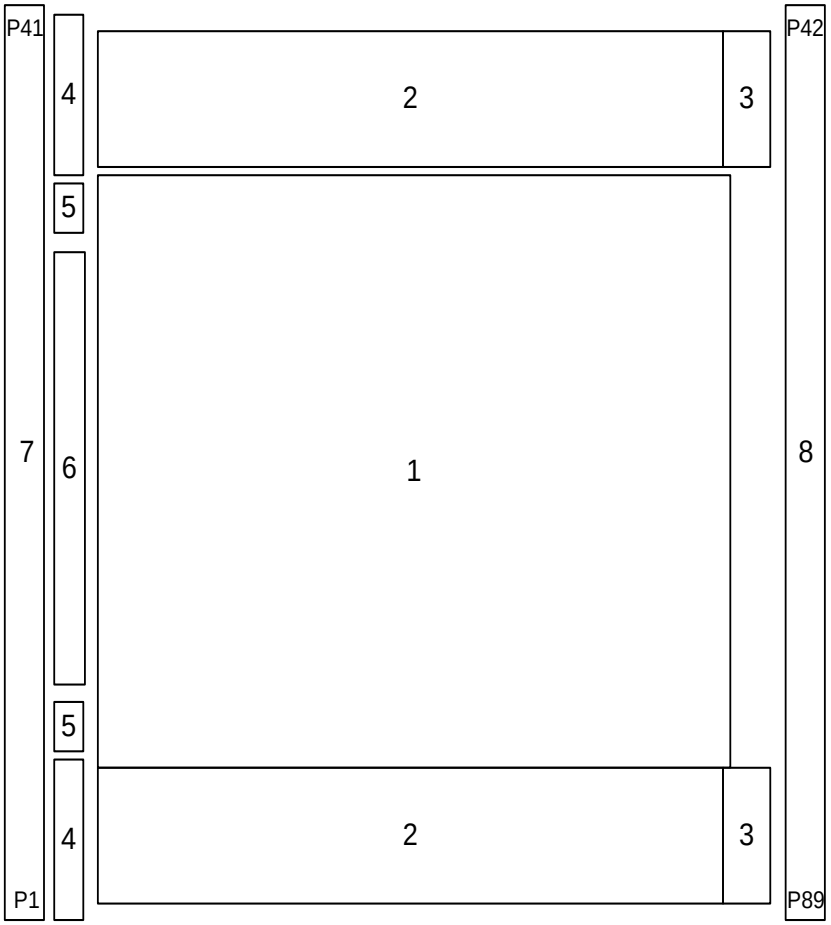


Figure 3.45: Floor plan of the fabricated 384x288 resistive microbolometer FPA readout. The parts are labeled as follows: 1. Detector and reference pixels, 2. Readout channel arrays, 3. Analog bias generation blocks, 4. Control interface blocks, 5. Reference pixel selection circuits, 6. Readout channel control signals and row signals blocks and row decoder, 7. Digital I/O pads, and 8. Analog I/O pads.

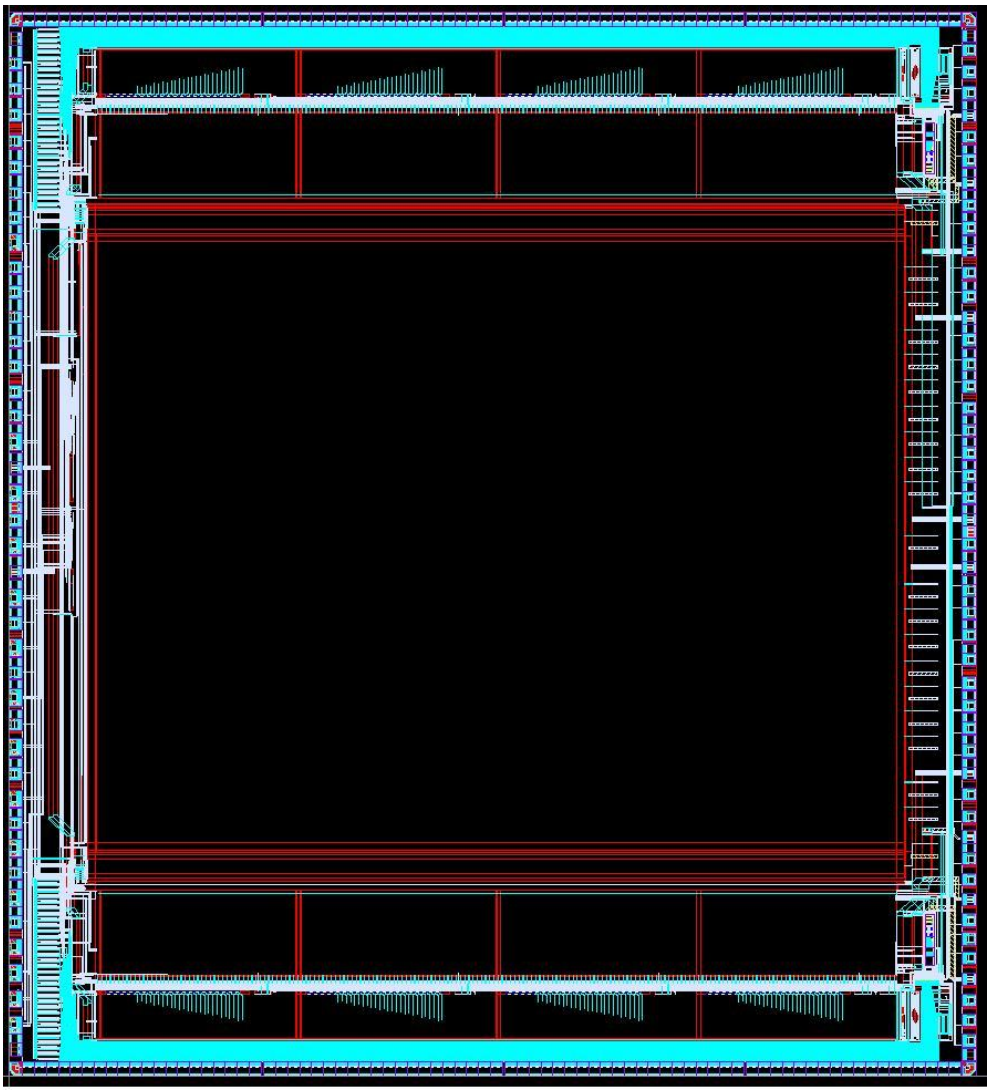


Figure 3.46: Layout of the fabricated 384x288 resistive microbolometer FPA, which occupies an area of 17.84 mm x 16.23 mm in a standard 0.6 µm CMOS process.

3.6 Expected Array Performance

The performance parameters of a microbolometer readout circuit are listed in Section 1.5 as follows: (i) responsivity, (ii) dynamic range, (iii) signal-to-noise ratio (SNR), (iv) power dissipation, and (v) area. Some of these parameters depend on the characteristics of the detectors even if only the readout

performance is concerned. To give an example, dynamic range and responsivity depend on the integration capacitance, which should be determined according to the self heating curves of the detector and reference pixels. Therefore, only noise and power dissipation of the designed readout will be examined in this section.

The total input referred noise of the readout is the combination of the noise contribution of all stages involved in the signal path. Each stage has a noise bandwidth, which is determined by the integrator for pixel biasing circuitry and by the output load for the stages after the integrator. After the total noise of all stages within their corresponding bandwidths, this value should be referred to input by dividing it to the gain of the previous stages. Table 3.24 lists the important parameters that are used to calculate the input referred noise of the readout, and Table 3.25 lists the noise contributions by each stage on the signal path. The bandwidths of the first four stages are determined by integration time, which is nominally 60 µs. However, the noise values are calculated for 50 µs integration time in order to take shorter integration times into account. The kT/C noise is concentrated into 10 kHz bandwidth by the sampling operation, which corresponds to the sampling frequency of each readout channel. The bandwidths of the remaining three stages are determined by the output speed requirements. In 50 fps operation, 5.53 million pixel outputs should be sent to output in 1 second; therefore, the bandwidth should be larger than 5.53 MHz. The nominal bandwidths of the opamps in these stages are very wide, therefore, an RC filter should be placed at the output in order to limit the noise, which has a time constant low enough to allow settling of the output voltage within the output multiplexing time. The noise contributions of the last three stages are calculated for an RC filter with a bandwidth of 10 MHz, which would have a time constant of 15.9 ns. The output multiplexing time is approximately 180 ns in 50 fps operation; therefore, such a filter would provide sufficient speed. Total

input referred noise of the readout is calculated as 53.1 pA using the parameters given in Table 3.24.

Table 3.24: List of the important parameters that are used to calculate the input referred noise of the readout.

Detector Resistance	60 kΩ
Reference Resistance	60 kΩ
Integration Capacitance	20 pF
Integration Time	50 μs
Output Filter BW	10 MHz

Table 3.25: List of the noise contributions by each stage on the signal path. Total current noise referred to the detector branch is equal to 53.1 pA.

	Noise BW	***Total in-band Noise***	***Input Referred Noise***
Injection Transistors	10 kHz	19.9 pA	19.9 pA
PMOS Biasing Circuitry	10 kHz	1.08 μV	16.8 pA
NMOS Biasing Circuitry	10 kHz	2.40 μV	38.0 pA
Integrator Opamp	10 kHz	5.46 μV	1.83 pA
Sampling Noise (kT/C)	10 kHz	37.1 μV	12.4 pA
S&H Opamp	10 MHz	45.7 μV	15.2 pA
RCG Buffer	10 MHz	38.7 μV	12.9 pA
Output Buffer	10 MHz	36.1 μV	12.0 pA
Total Noise			53.1 pA

The overall noise of a microbolometer has two main components: the readout noise and the detector noise. The detector noise also has two components: the thermal noise and the flicker noise. Thermal noise of the detector depends

solely on the resistance value and it can be calculated easily for a given resistance. However, the flicker noise strongly depends on the process. Currently, there is an ongoing research to optimize the fabrication process of the detectors to be implemented on this readout circuit. Table 3.26 lists the expected detector pixel parameters for the 384x288 resistive microbolometer FPA with 35 µm pixel pitch. The flicker noise coefficient is not known yet, which affects the overall performance to a great extent. Figure 3.47 shows the expected noise equivalent temperature difference (NETD) of the designed 384x288 resistive microbolometer FPA for different flicker noise corner frequencies. The other detector parameters that are used to obtain the graph are as listed in Table 3.26. The NETD that can be obtained by using a noiseless readout for the given detectors are also shown in the figure in order to show the effect of the readout noise on the NETD value. This figure shows that the expected NETD value of the designed FPA is 93.9 mK and 151.8 mK for 3 kHz and 10 kHz corner frequencies, respectively. The values that can be obtained by using a noiseless readout for the same frequencies are 87.5 mK and 147.9 mK, showing that the noise contribution of the readout is very small when compared to the detectors.

Table 3.26: Expected detector pixel parameters for the 384x288 resistive microbolometer FPA with 35 µm pixel pitch.

Resistance	60 kΩ
Bias Current	15 µA
Thermal Conductance	$1x10^{-7}$ W/K
Thermal Time Constant	7 ms
Fill Factor	50%
Absorption Coefficient	50%
TCR	3.10%

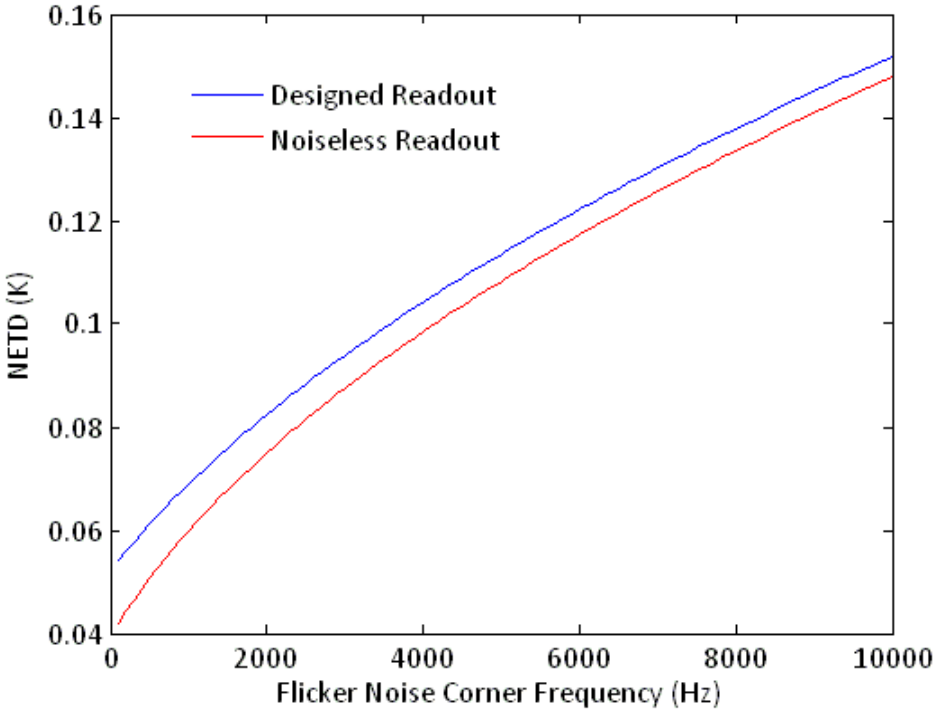


Figure 3.47: Expected noise equivalent temperature difference (NETD) of the designed 384x288 resistive microbolometer FPA for different flicker noise corner frequencies. The other detector parameters that are used to obtain this graph are as listed in Table 3.26. The NETD that can be obtained by using a noiseless readout for the given detectors are also shown in the figure in order to show the effect of the readout noise on the NETD value.

The power dissipation of the 384x288 microbolometer FPA readout can be examined in four main groups: (i) analog readout blocks, (ii) digital readout blocks, (iii) digital I/O pads, and (iv) pixels. The simulated power dissipation values of the analog readout blocks are listed in Table 3.27, which add up to 57 mW. The power dissipation of the digital blocks depends on the operating frequency and the load capacitance, and it is given as

$$P_{dig} = {V_{DD}}^2 \cdot f \cdot \sum C_{load} \quad 3.5$$

where f denotes the operating frequency and C_{load} is the capacitive load at the output of each digital cell. The operating frequency and the output load are different for each block; therefore, the exact power dissipation of the digital cells are not easily predictable. The digital I/O cells in the pad frame have digital input and output buffers, and pull up or pull down circuits. Therefore, the power dissipation of the digital I/O cells can be calculated using the same formula for the digital blocks. Finally, the pixels should be biased from an external voltage source during the readout operation, and the total power dissipated by the pixels directly depends on the bias current value.

Table 3.27: Simulated power dissipations of the analog blocks. The total power dissipation of these blocks is equal to 57 mW.

	Power Dissipation of a Single Block	***Total Power Dissipation***
Integrator opamp	48.9 µW	18.8 mW
S&H opamp	53.0 µW	20.4 mW
RCG buffers	0.52 mW	4.16 mW
Output buffers	0.84 mW	3.37 mW
Bias correction DAC buffers	81.7 µW	1.31 mW
Bandgap references	0.33 mW	0.66 mW
Bias generation blocks	2.20 mW	4.40 mW
First stage of bias correction DAC	2.00 mW	4.00 mW

3.7 Summary and Conclusions

This chapter presented the design of a 384x288 resistive microbolometer FPA readout. The FPA can be roughly divided into three parts: (i) pixels, (ii) analog blocks, and (iii) digital blocks.

The FPA has 288 detector and 16 reference pixel rows, each consisting of 384 columns. Although the actual pixels are to be fabricated by post-CMOS processes, the circuitries that will be used to connect the fabricated pixels to the readout are included in the readout. The pixel circuitry consists of metal routing lines and multiplexing switches, which are used to connect the selected pixel to the readout for biasing.

The main functions of the analog blocks are processing IR radiation data obtained from the pixels and forming the serial output signal. For this purpose, a single dedicated CTIA type readout channel is implemented for each pixel column, and the outputs of the readout channels are multiplexed to the output channels using the low power sampling and buffering architecture described in Chapter 2. Besides these main analog blocks, there are also analog bias generation blocks that are used to generate the analog bias voltages. Another analog block is the bias correction DAC structure, which is used to generate distinct bias voltages for each pixel in order to decrease the effect of nonuniformity and increase the dynamic range. In the 384x288 FPA readout, the improved bias correction DAC structure described in Chapter 2 is implemented.

Digital blocks are necessary to generate the timing signals of the switched-capacitor operations in the analog readout such as integration, sampling, and output multiplexing. Besides generating the timing signals, various configurations of the readout are also performed by the digital blocks. For this purpose, a control interface block is implemented, which consists of a 31-byte D

flip-flop type RAM for storing the data and shift registers for serial programming. Serially programmable control interface structure considerably reduces the number of bond pads required for configuration and testing purposes.

The readout has several configurable parameters that can be controlled using the control interface. These parameters include the number of output channels, active array size (either 384x288 or 320x240), the reference rows, digital timing signal durations, and analog bias voltages. It is also possible to observe the internally generated digital and analog signals, and even apply these signals externally in case of any unexpected problem.

The 384x288 resistive microbolometer FPA is fabricated in a standard 0.6 µm CMOS process, and it occupies an area of 17.84 mm x 16.23 mm. The expected power dissipation of the analog readout blocks and total input referred current noise are approximately 57 mW and 53.1 pA, respectively.

Prepared test setup and obtained test results are given in the next chapter.

CHAPTER 4

PERFORMANCE OF THE FABRICATED 384x288 RESISTIVE MICROBOLOMETER FPA READOUT

This chapter presents the test setup and the initial test results of the fabricated 384x288 resistive microbolometer FPA readout. The circuit is fabricated in a standard 0.6 μm CMOS process, and it occupies an area of 17.84 mm x 16.23 mm. A dedicated run is used for the fabrication of the circuit on 6" wafers, so that microbolometer detector pixels can be implemented on these wafers using the surface micromachining process developed at METU. Besides the design and implementation of the readout, a 4-layer imaging PCB is prepared in order to take images from the FPA after the detectors are implemented. The initial tests of the fabricated readout are also performed on this PCB by activating the self-test mode of the circuit.

This chapter first presents the fabricated chip, the designed imaging PCB, and the prepared test setup in Section 4.1. Then, Section 4.2 gives the test results of the digital blocks and Section 4.3 gives the test results of the analog blocks. Section 4.4 presents the measured noise performance of the imaging system. Finally, Section 4.5 gives the results of the power dissipation measurements of the FPA.

4.1 Fabricated Chip and the Imaging PCB

Figure 4.1 shows the photograph of the 6” CMOS wafer and zoomed view of the 384x288 resistive microbolometer FPA readout with 35 µm pixel pitch, which occupies an area of 17.84 mm x 16.23 mm. The chip is wire bonded to a 180 pin PGA type package to perform the tests, and Figure 4.2 shows the photograph of the chip together with the package.

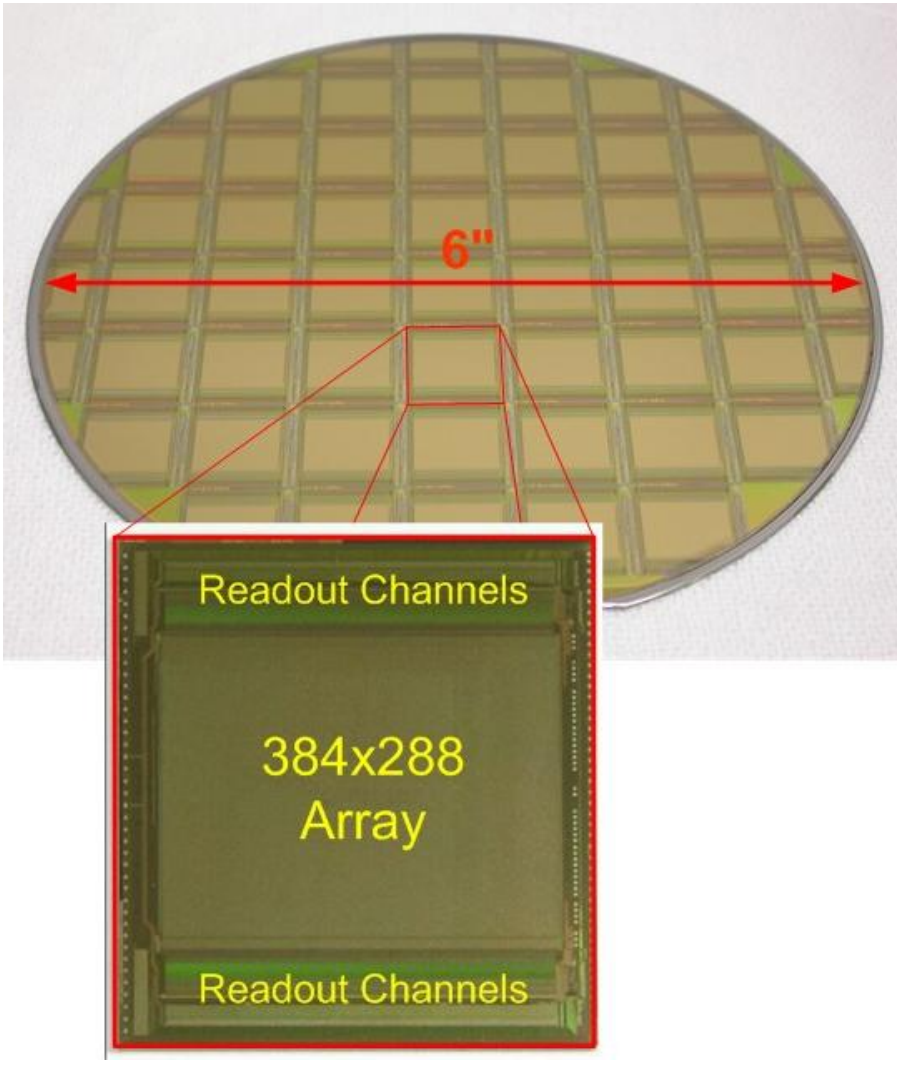


Figure 4.1: Photograph of the 6” CMOS wafer and zoomed view of the 384x288 resistive microbolometer FPA readout with 35 µm pixel pitch, which occupies an area of 17.84 mm x 16.23 mm.

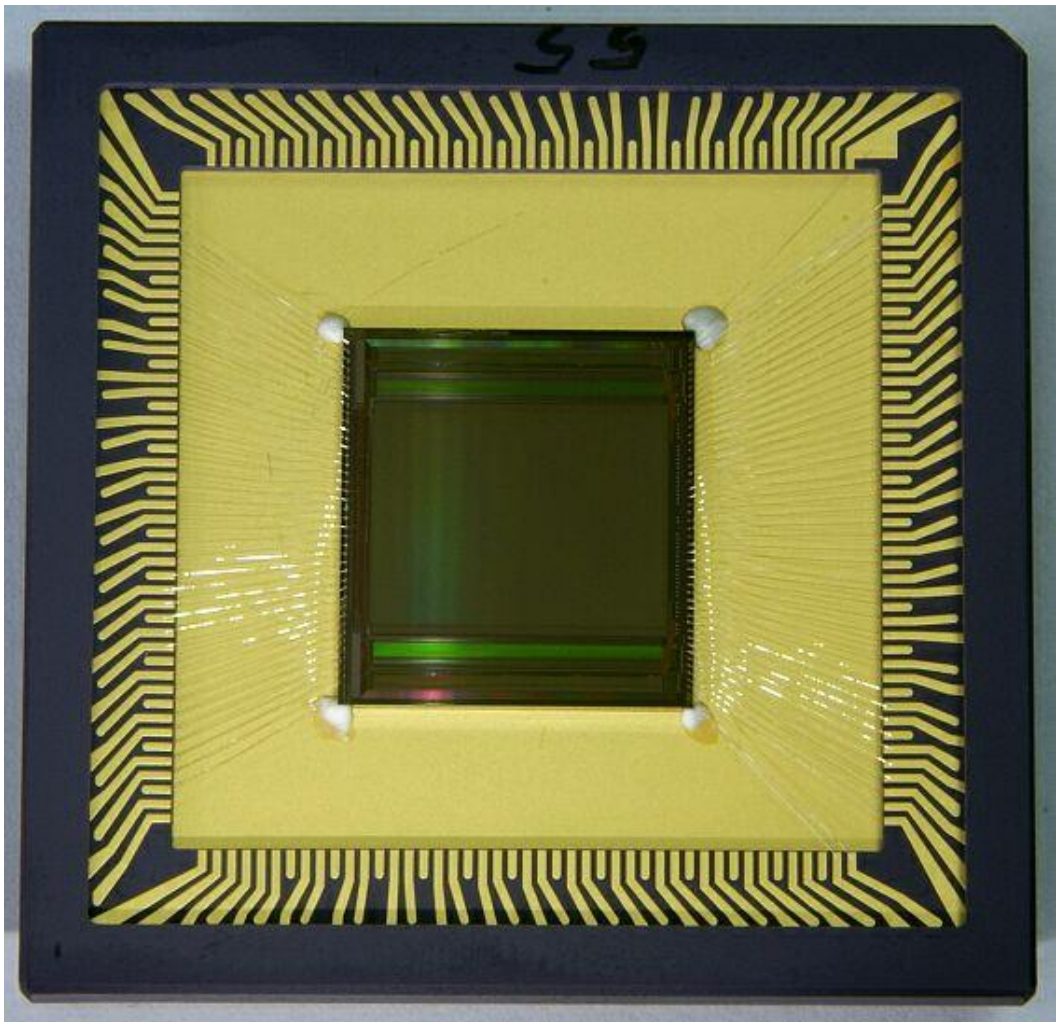


Figure 4.2: Photograph of the 384x288 microbolometer FPA together with the 180 pin PGA type package.

A 4-layer imaging PCB is also designed in order to take images from the FPA after the detectors are fabricated, which can also be used to test the readout. Figure 4.3 shows the simplified block diagram, and Figure 4.4 shows the photograph of the imaging PCB. As seen in these figures, The PCB includes two dual video buffer opamps (AD8062) to buffer the readout outputs, two 14-bit A/D converters (AD9240) to provide digital video output, three octal digital buffers (MM74HC541) to buffer the important digital inputs and A/D converter

outputs, three triple CMOS switches (ADG733) to select different configurations, and five voltage regulators (three MIC5205BM5s and two MC7805s) to generate the supply voltages of these ICs. The PCB needs only supply voltages and digital timing signals in order to operate the readout, and therefore, greatly simplifies the required test setup.

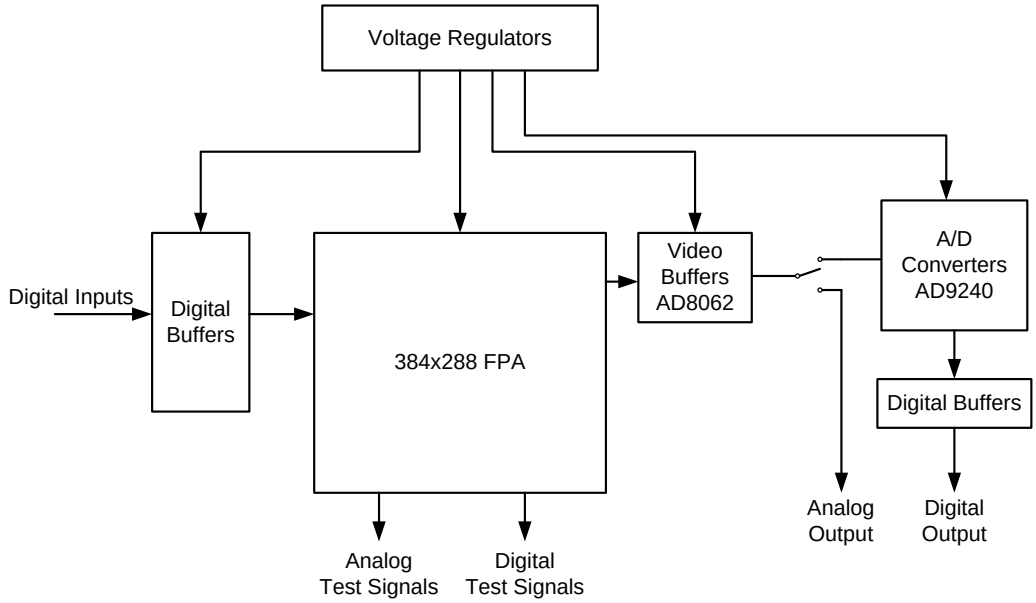


Figure 4.3: Simplified block diagram of the 4-layer imaging PCB.

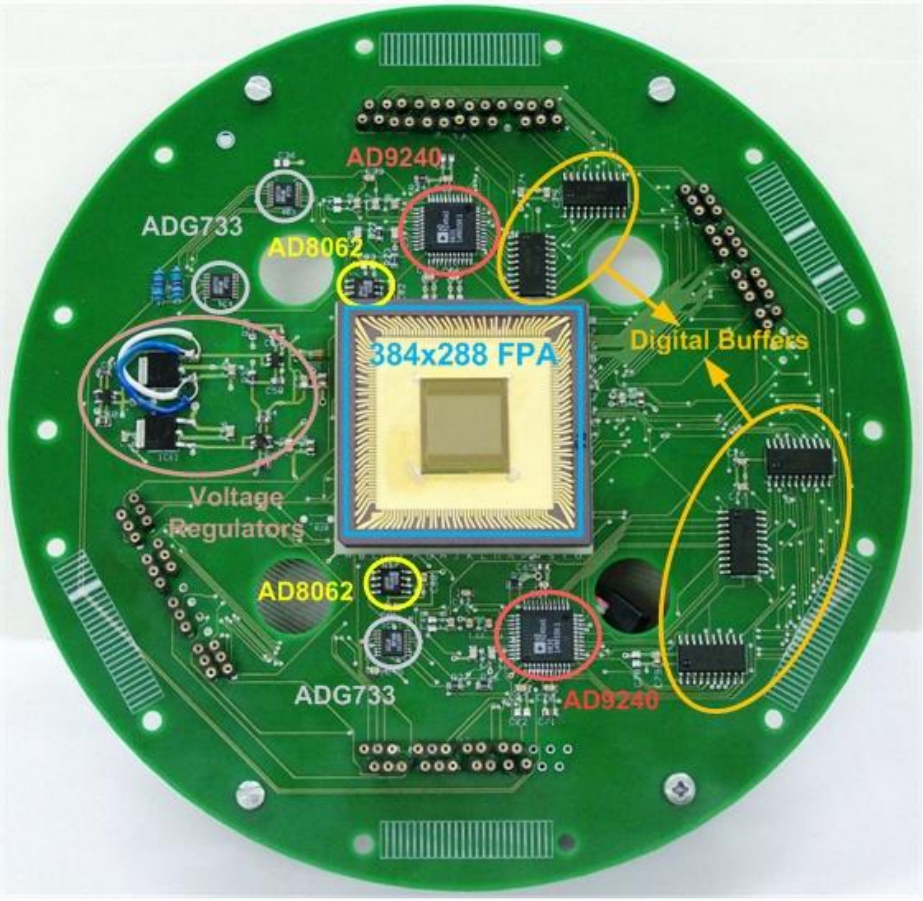


Figure 4.4: Photograph of the 4-layer PCB designed for 384x288 microbolometer FPA.

Figure 4.5 shows the simplified block diagram, and Figure 4.6 shows the photograph of the setup prepared to test the fabricated 384x288 FPA readout. The test setup includes the imaging PCB, an FPGA board programmed by a computer using its relevant software, an analog bias PCB to control the internal analog bias voltages, and other necessary testing equipments.

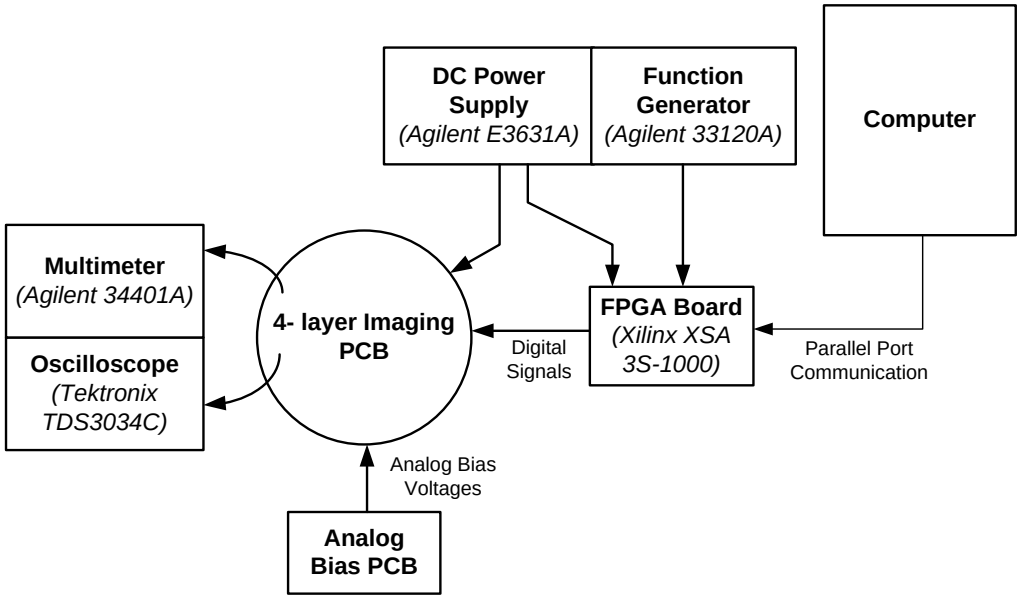


Figure 4.5: Simplified block diagram of the setup prepared to test the fabricated 384x288 FPA readout.

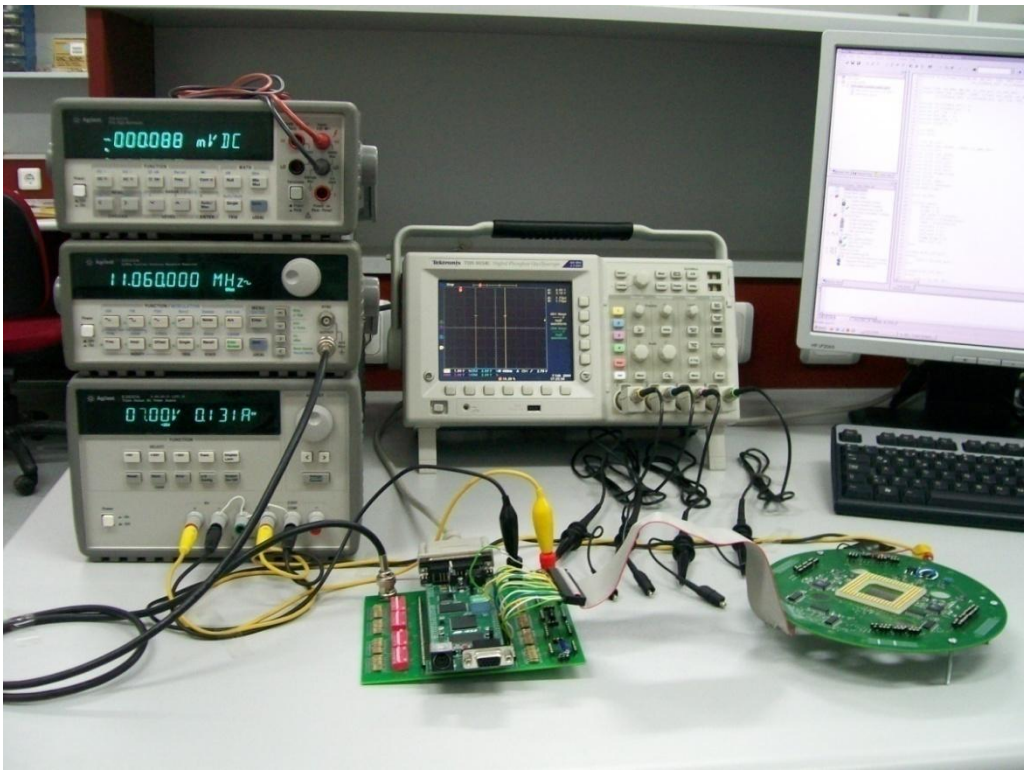


Figure 4.6: Photograph of the test setup prepared for the 384x288 FPA readout.

4.2 Test Results of the Digital Blocks

This section presents the test results of the two digital blocks of the 384x288 FPA readout: the readout channel control signals block and the output multiplexer blocks. The important digital signals of the 384x288 FPA readout are connected to the bidirectional I/O cells in the pad frame, which are IPs of the X-FAB Semiconductor Foundries, in order to increase the controllability and the observability of these signals. Figure 4.7 shows the simplified schematic of a bidirectional I/O cell, which can be used either to observe or to drive the connected digital signal. The control signals of these I/O cells are stored in the control interface of the chip. When the test mode is activated, all bidirectional pads switch to output mode, and consequently, all the digital signals that are connected to the bidirectional I/O cells can be observed.

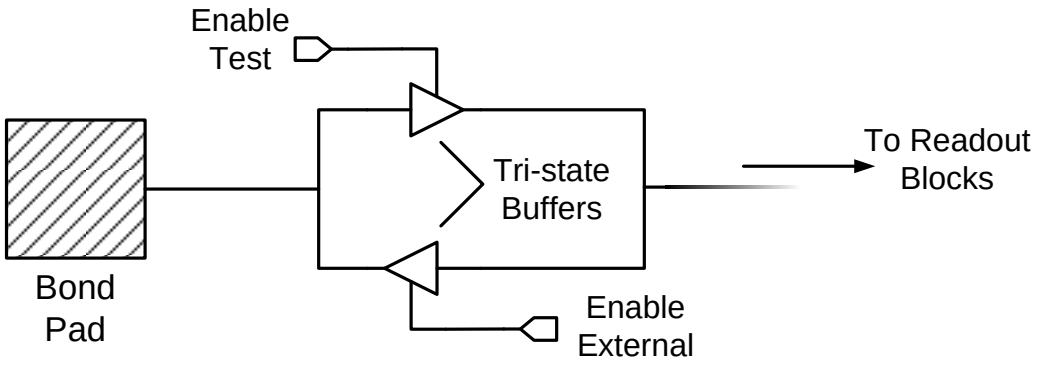


Figure 4.7: Simplified schematic of the bidirectional I/O cells, which can be used either to observe or to drive the digital signals externally. The control signals of these cells are stored in the control interface.

There are 13 observable digital signals in the 384x288 FPA readout. 9 of these signals are the outputs of the readout channel control signals block, and 4 of them are the coins of the output multiplexer block. The bidirectional pads are

switched to output mode using the control interface in order to observe these signals. The required clock (*CLK*) and line synchronization (*LSYNC*) signals are generated on the FPGA board. Figure 4.8 shows the clock and line synchronization (*LSYNC*) signals that are applied to the chip during the tests of the digital blocks. The clock frequency is chosen as 5.53 MHz, which is the nominal clock frequency for 50 fps operation of a 384x288 array.

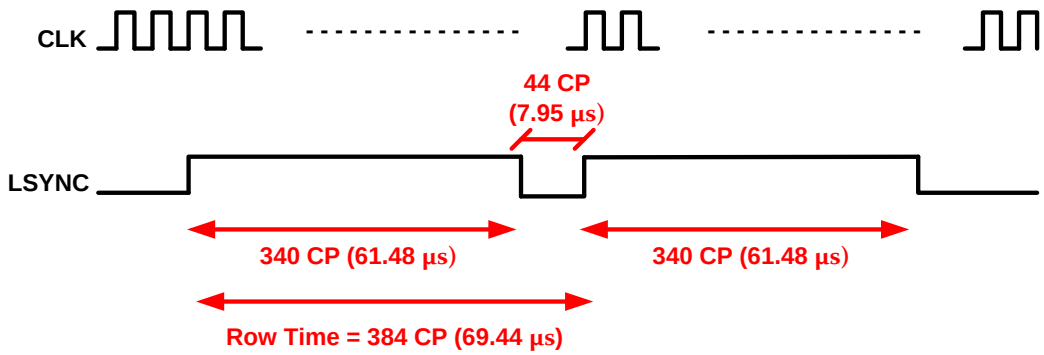


Figure 4.8: Clock (*CLK*) and line synchronization (*LSYNC*) signals that are applied to the chip during the tests of the digital blocks. The clock frequency is chosen as 5.53 MHz, which is the nominal clock frequency required to operate a 384x288 array at 50 fps.

The following two sections present the test results of the readout channel control signals block and the output multiplexer block. The obtained results verify the proper operation of both blocks.

4.2.1 Operation of the Readout Channel Control Signals Block

The control signals block generates the timing signals for the readout channels, and it controls two main groups of operations: (i) switched capacitor readout channel operations such as integration and sampling, and (ii) application of the

bias correction voltages to the gates of the NMOS injection transistors in the CTIA preamplifiers.

First, the integration and sampling signals are observed. Figure 4.9 shows the following four digital signals: integration reset (*INT_RST*), CTIA output stabilization (*CTIA_OS*), integration enable (*INT_ENB*), and sampling (*SH*) signals. For this test, the durations of the *INT_RST*, *CTIA_OS*, and *SH* signals are configured as 10, 2, and 8 clock pulses, respectively. The duration of the *INT_ENB* signal is determined by *LSYNC*, which is applied for 340 clock pulses. This figure verifies that these signals are generated inside the chip as configured.

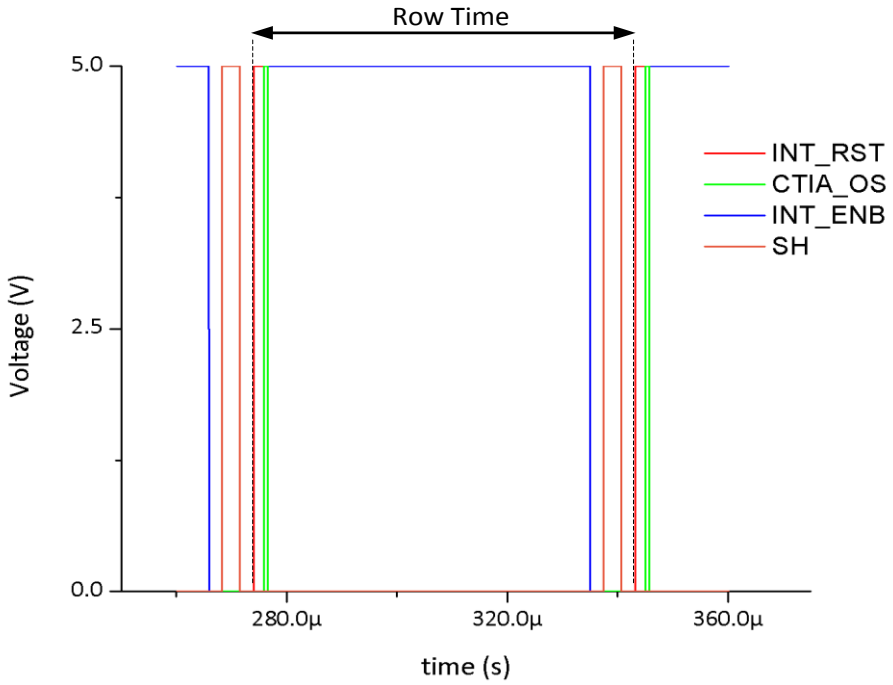


Figure 4.9: Digital signals that determine the timing of the main readout channel operations: integration reset, CTIA output stabilization, integration enable, and sampling signals. The results are obtained using a 5.53 MHz clock.

Then, the second group signals, which determine the timing of the application the bias correction voltages to the gates of the NMOs injection transistors are

observed. Figure 4.10 shows the following three digital signals: bias correction data transfer (*DACD_TRANSFER*), bias correction voltage loading (*DACD_NBIAS_LOAD*), and bias correction data transfer (*DACD_LOAD*) signals. The timings of these signals are not configurable, and they are always generated automatically in accordance with the timing information given in Table 3.19. The figure verifies that these signals are generated inside the chip properly.

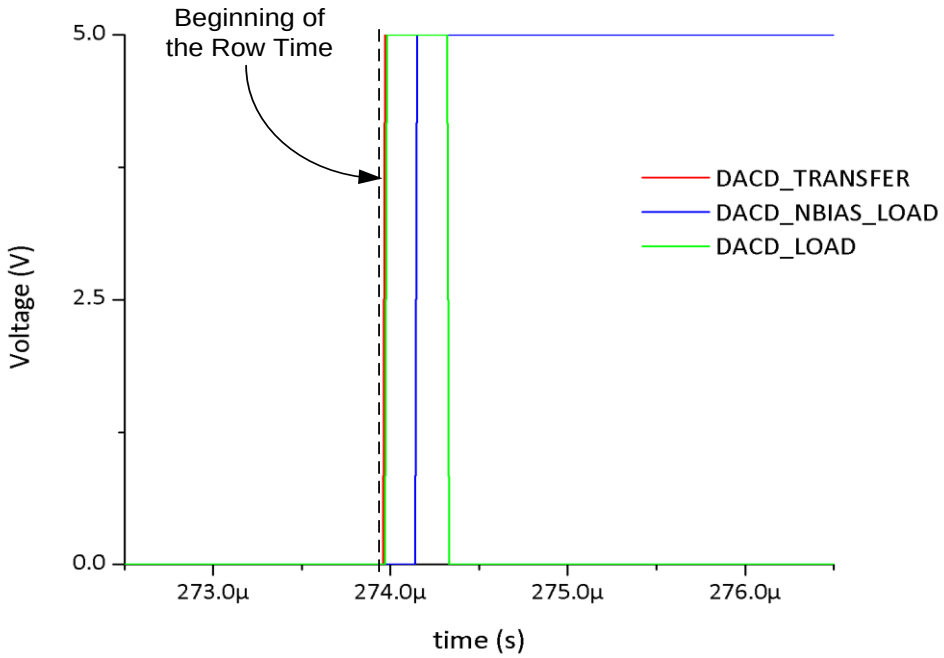


Figure 4.10: Digital signals that determine the timing of the application the bias correction voltages: bias correction data transfer (*DACD_TRANSFER*), bias correction voltage loading (*DACD_NBIAS_LOAD*), and bias correction data transfer (*DACD_LOAD*) signals. The results are obtained using a 5.53 MHz clock.

4.2.2 Operation of the Output Multiplexer

After verifying the proper operation of the readout channel control signals block, the outputs of the output multiplexer block is observed to check the operation of this block. Figure 4.11 shows the simplified schematic of the

192-bit shift register in a single output multiplexer block, where *Coin1* and *Coin2* denote the bits that are shifted in the shift register for output multiplexing. At the beginning of output multiplexing, the digital timing circuitry inside the output multiplexer block sets *Coin1* to high for the 384x288 mdoe, while Coin2 is set to high for the 320x240 mode. Both signals are connected to the bidirectional I/O cells in the pad frame, and consequently, they are both observable and controllable. The proper operation of the output multiplexer block can be verified by observing only these coin bits. First of all, the timing of the generated coin bits can be directly observed. The shifting operation can also be checked by observing the time difference between the two coins in the 384x288 mode of the FPA. If the shift register is working as designed, there must be 16 and 32 clock pulses between *Coin1* and *Coin2* for single and dual output modes, respectively. As a result, both the shifting operation and the correct timing of the output multiplexing can be verified.

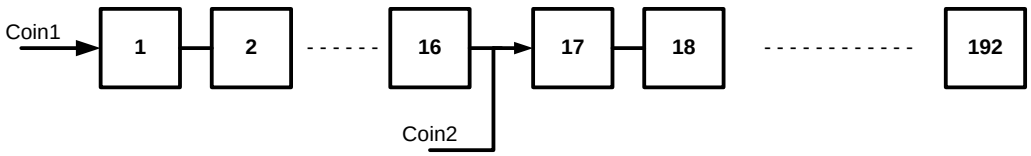
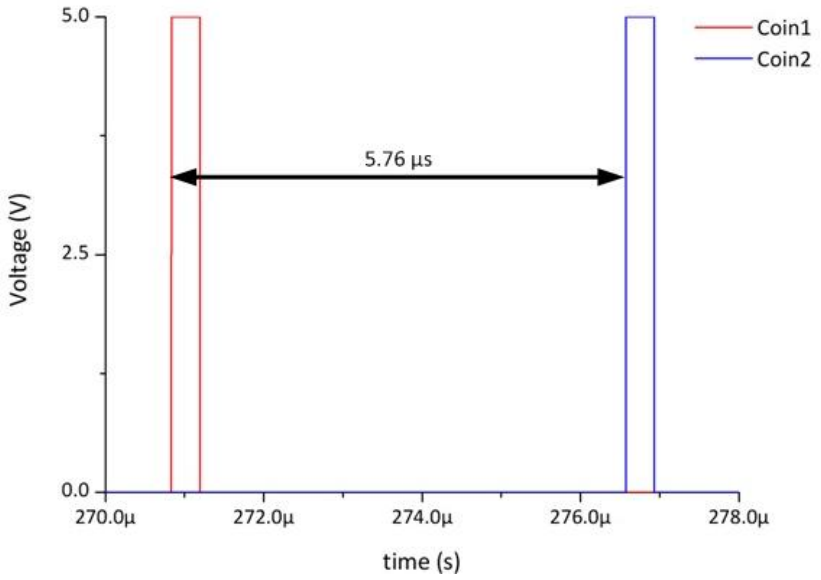
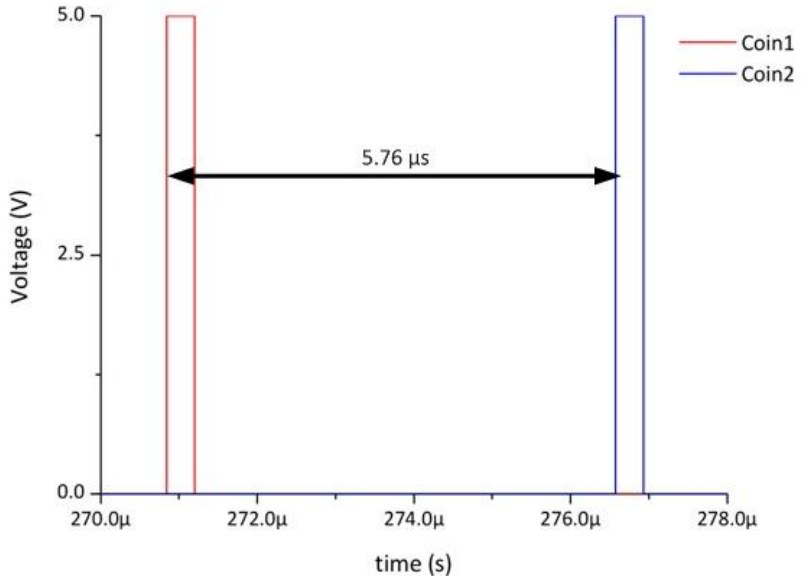


Figure 4.11: Simplified schematic of the 192-bit shift register in a single output multiplexer block, where *Coin1* and *Coin2* denote the bits that are shifted in the shift register for output multiplexing. At the beginning of output multiplexing, *Coin1* is set to high for 384x288 mode, while *Coin2* is set to high for 320x240 mode.

Figure 4.12 and Figure 4.13 show the coin bits of the output multiplexers of the top and the bottom readout channel arrays for dual and single output modes, respectively. These figures verify that the coins are generated with a correct timing and the shift registers in the output multiplexer blocks operate properly.



(a)



(b)

Figure 4.12: Coin bits of the shift registers in the output multiplexers of (a) the top readout channel array, and (b) the bottom readout channel array for dual output channel mode. In dual output channel mode, the main system clock is divided into two in the output multiplexer block, therefore, there must be 32 clock pulses between the two coin bits, which corresponds to 5.76 µs for a clock frequency of 5.53 MHz.

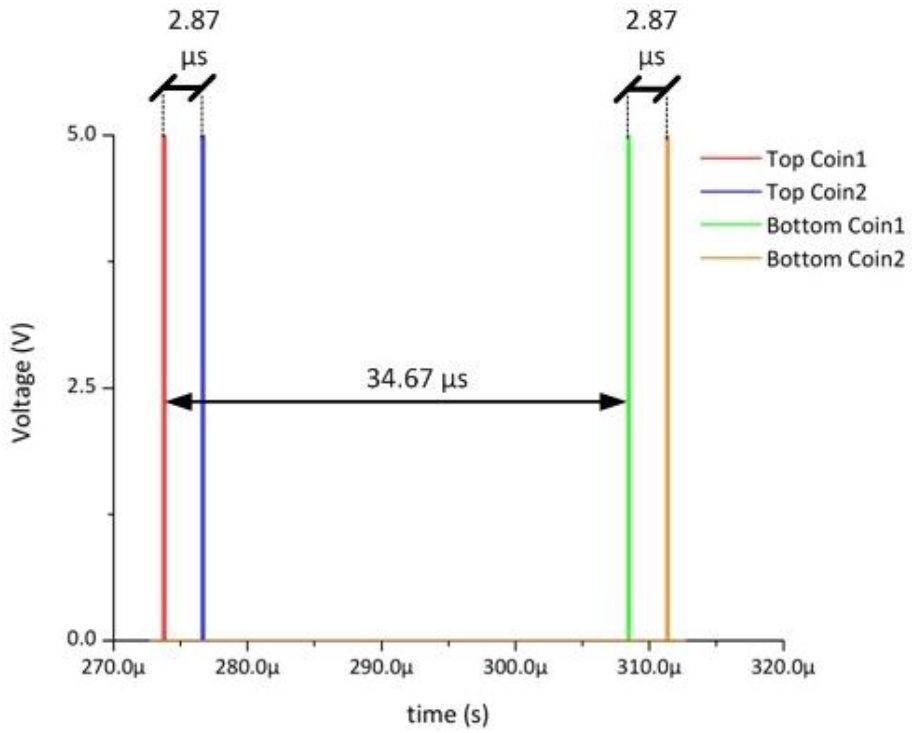


Figure 4.13: Coin bits of the shift registers in the output multiplexers of the top and the bottom readout channel array for single output channel mode. In single output channel mode, the main system clock is directly used in the output multiplexer block, and therefore, there must be 16 clock pulses between the two coin bits of the same output multiplexer, and 192 clock pulses between the coins of the two output multiplexers, which correspond to 2.87 µs and 24.67 µs, respectively.

4.3 Test Results of the Analog Blocks

This section presents the results of the tests that are performed to verify the operation of the analog blocks in the 384x288 FPA readout. These tests are performed by observing the outputs of three different blocks: (i) the bias generator blocks, (ii) individual readout channels at the right side of the FPA, and (iii) the output channels of the FPA.

The bias generator blocks are tested by changing their digital inputs and measuring the corresponding output voltage. The outputs of these blocks can

be observed using the analog multiplexers by connecting the internally generated voltages to the bond pads as explained in Section 3.3.5. On the other hand, the individual readout channels and the output channels of the FPA are tested using the self-test pixels, which are poly-Si resistors implemented in the CMOS process. For this purpose, the chip is switched to the self-test mode by configuring the control interface. Besides switching to the self-test mode, NMOS bias voltages are connected to a common bus, which is then connected to a bond pad. As a result, the bias voltages of the self-test detector pixels, and hence the integration curves, could be easily controlled using a potentiometer.

Section 4.3.1 gives the measurement results of the bias generation blocks. Section 4.3.2 presents the test results of a single readout channel in the 384x288 FPA readout, and Section 4.3.3 presents the test results of the entire readout, which is observed through the output channels of the chip.

4.3.1 Operation of the Bias Generation Blocks

This section presents the test results of the on-chip resistive ladder DACs that are used to generate the bias voltages for the analog blocks of the readout. These DACs include: (i) Injection transistor bias generator, (ii) opamp bias generator, (iii) reset voltage generator, and (iv) first stage of the bias correction DAC structure. All of these blocks are tested using the same method: The analog multiplexers are configured to connect the internally generated voltages to bond pads, and the outputs for each digital input are measured using a multimeter.

Table 4.1 summarizes the measured range and resolution of the bias generation blocks together with the design parameters. The results show that the DACs are operating as expected.

Table 4.1: Summary of the measured range and resolution of the bias generation blocks together with the design parameters. The results show that the DACs are operating as expected.

	Range (V)		***Resolution (mV)***	
	Measured	***Designed***	***Measured***	***Designed***
PMOS Bias Gen.	2.62 - 3.15	2.60 - 3.15	17.2	17.6
NMOS Bias Gen.	2.20 - 2.82	2.18- 2.82	20.1	20.5
Reset Voltage Gen.	1.93 - 2.79	1.90 - 2.80	286.8	300
First Stage of Bias Corr.	1.12 - 4.00	1.10 - 4.01	93.1	94
Op. DAC1	1.20 - 1.32	1.19 - 1.33	17.5	20
Op. DAC2	1.38 - 1.53	1.35 - 1.50	48.3	50
Op. DAC3	1.58 - 1.93	1.55 - 1.90	50.6	50
Op. DAC4	2.95 - 3.10	2.95 - 3.10	49.5	50
Op. DAC5	3.44 - 3.57	3.45 - 3.59	18.9	20
Op. DAC6	3.59 - 3.91	3.61 - 3.91	21.5	20

4.3.2 Operation of a Single Readout Channel

The first test conducted on the readout channels of the fabricated 384x288 FPA readout is observing the integrator and S&H outputs of a single readout channel. The integrator and S&H outputs of the rightmost readout channels in the top and the bottom readout channel arrays are connected to bond pads through switches that are controlled by the control interface. Therefore, it is possible to observe the operation of a single readout channel by configuring the corresponding bit in the control interface.

Figure 4.14 shows the integrator and S&H outputs of the rightmost readout channel in the top readout channel array. The digital signals *INT_ENB* and *SH* are also shown in the figure in order to show the timing information. This figure

shows that the integration and sampling operations are performed as expected in the readout channels.

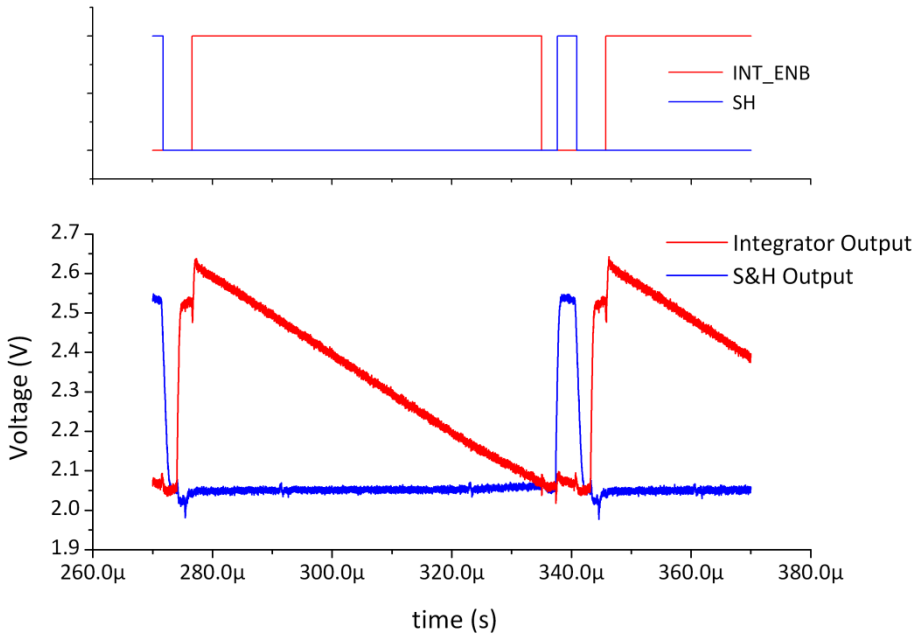
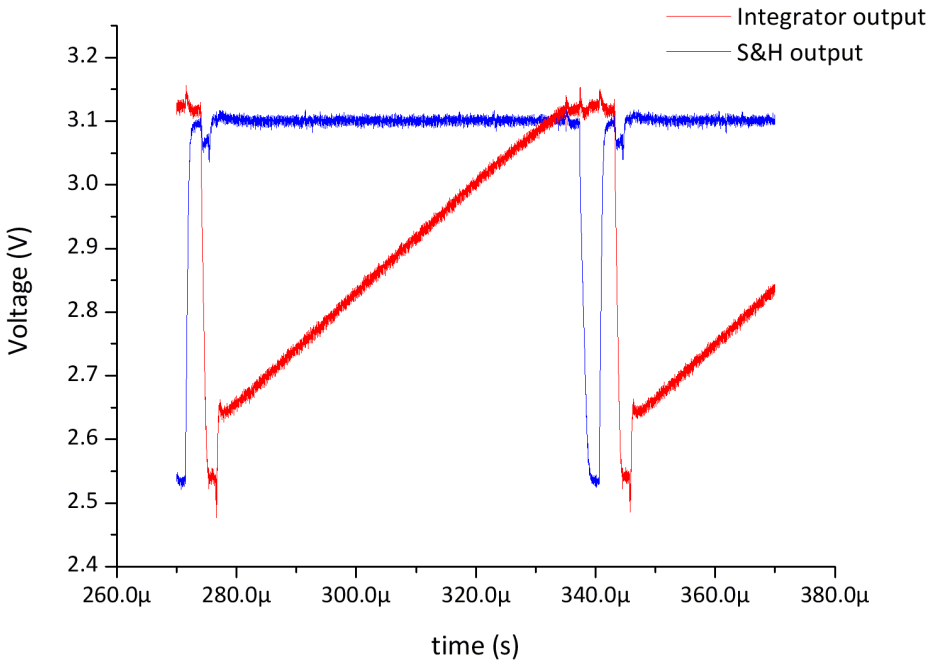
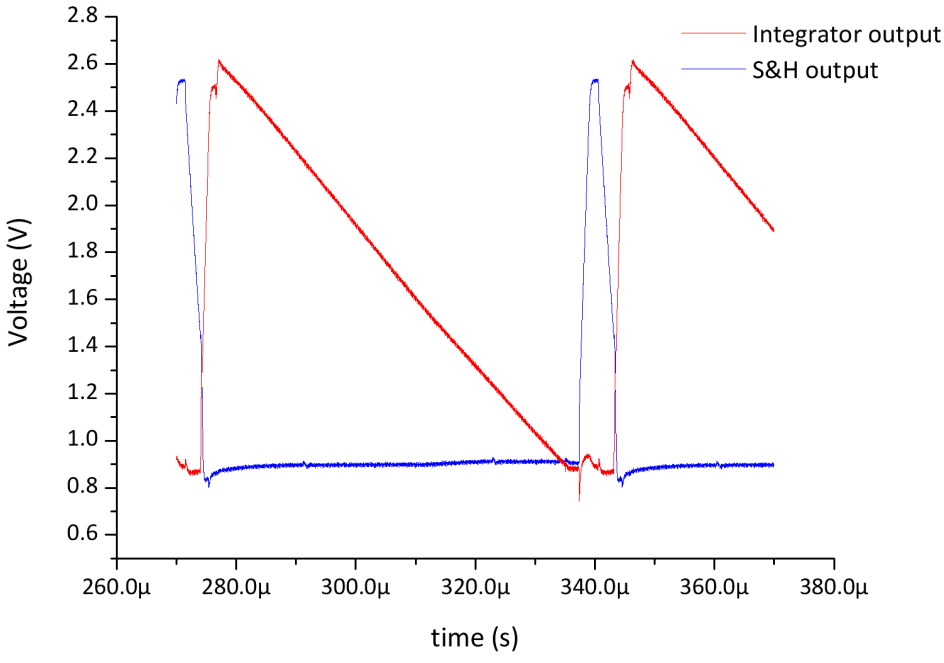


Figure 4.14: Integrator and S&H outputs of the rightmost readout channel in the top readout channel array. The digital signals *INT_ENB* and *SH* are also shown in order to show the timing information.

The same procedure is repeated by changing the bias voltages of the NMOS injection transistors in order to observe if the S&H output follows the integrator output. Figure 4.15 shows the transient output voltages of the integrator and S&H outputs of a single readout channel for different NMOS injection transistor bias voltages. This figure shows that the S&H output follows the integrator output between approximately 3.1 V and 0.9 V.



(a)



(b)

Figure 4.15: Transient output voltages of the integrator and S&H outputs of a single readout channel for different NMOS injection transistor bias voltages.

4.3.3 Operation of the Output Channels

After verifying the operation of a single readout channel, the operation of the entire readout is observed through the output channels. For this purpose, the PCB is configured for analog output mode, and the analog outputs are observed using an oscilloscope in both single and dual output modes. This procedure is repeated for different integrator output voltages by changing the bias voltage of the NMOS injection transistors in order to check if the analog output changes accordingly.

Figure 4.16 shows the analog channel output of the 384x288 FPA together with the integrator outputs of the test channels and the integration enable signal in single output mode. The output data becomes valid at the falling edge of the 5^{th} clock after LSYNC signal and stays valid for 384 clock pulses. The FPA output is interdigitated in the single output mode; therefore, the first half of the output belongs to the top RCA, while the second half belongs to the bottom RCA. Figure 4.17 shows the outputs of FPA with the same bias values in dual output mode. As seen in this figure, the FPA output in the single output mode is the combination of the two outputs in the dual output mode, verifying that the output channel multiplexing is working properly.

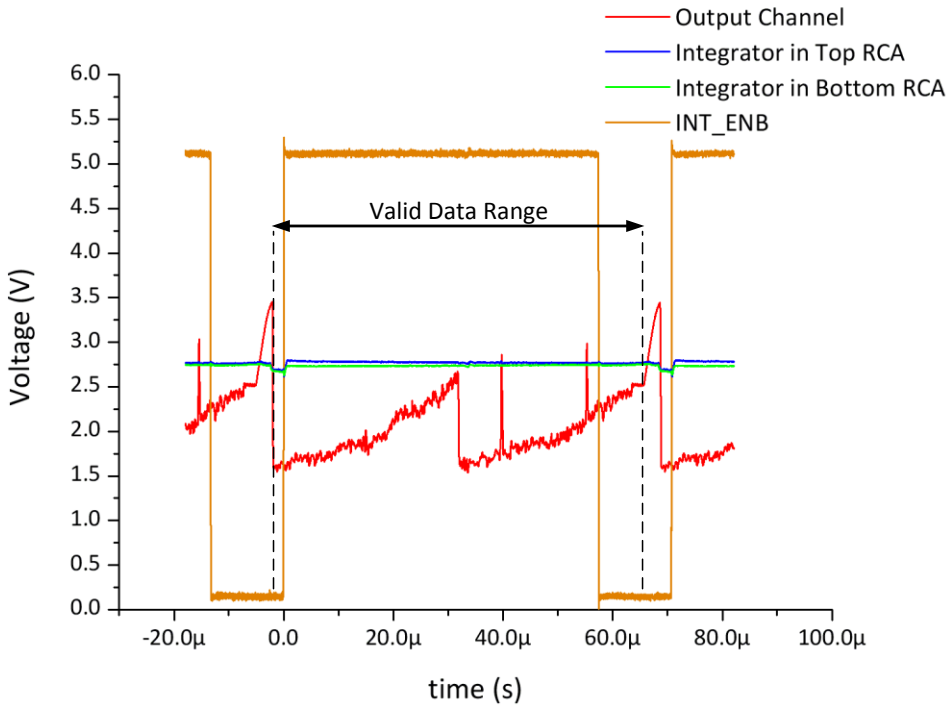
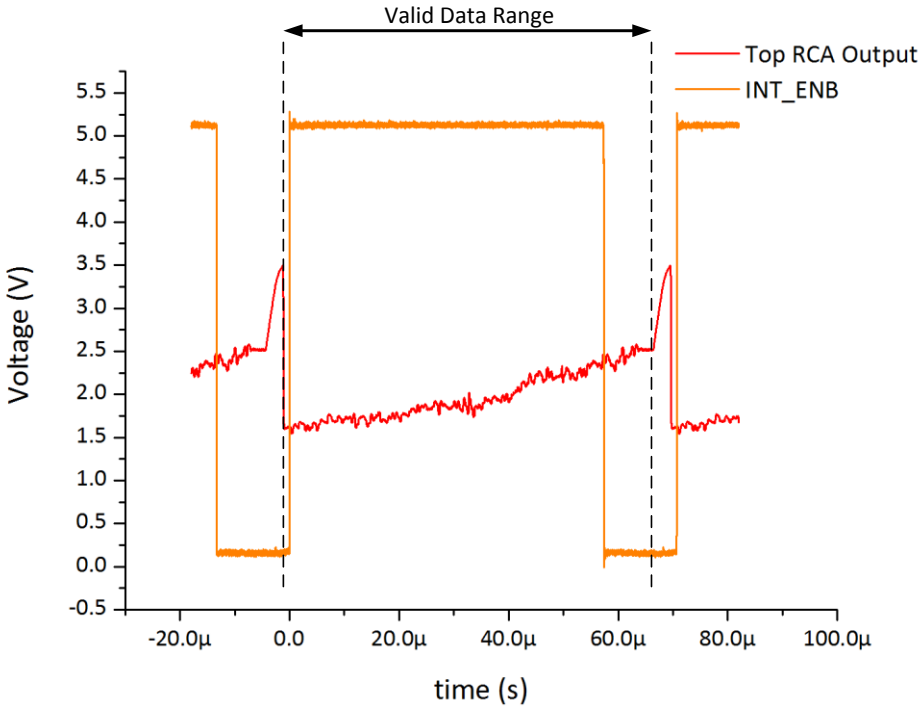
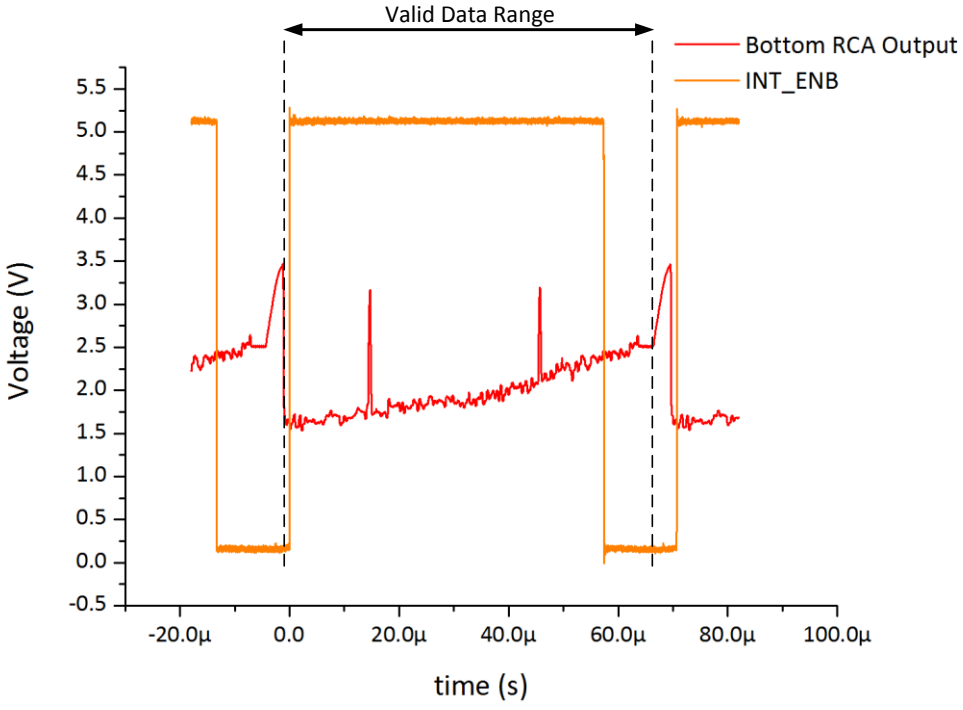


Figure 4.16: Analog channel output of the 384x288 FPA together with the integrator outputs of the test channels at the top and the bottom RCAs and the integration enable signal. The output data becomes valid at the falling edge of the 5th clock after LSYNC signal and stays valid for 384 clock pulses.

During this test, the injection transistor bias voltages are adjusted to provide minimum integration current at the test channels. Although the outputs of the rightmost channels are consistent with this configuration, there is a gradient at the output, which means that the integration current is increasing towards the left of the array. This is an expected result due to the routing resistance of the supply lines. Figure 4.18 shows the calculated voltage gradient in the supply lines of the self-test pixels for 10 µA average bias current. As seen in this figure, the supply voltage values deviate from ideal through the array. Since the gate bias voltages of the injection transistors are constant, the effective bias voltages of the pixels have a gradient, resulting in the output pattern shown in Figure 4.16 and Figure 4.17.



(a)



(b)

Figure 4.17: Outputs of the (a) top RCA, and (b) bottom RCA of the 384x288 FPA readout in dual output mode.

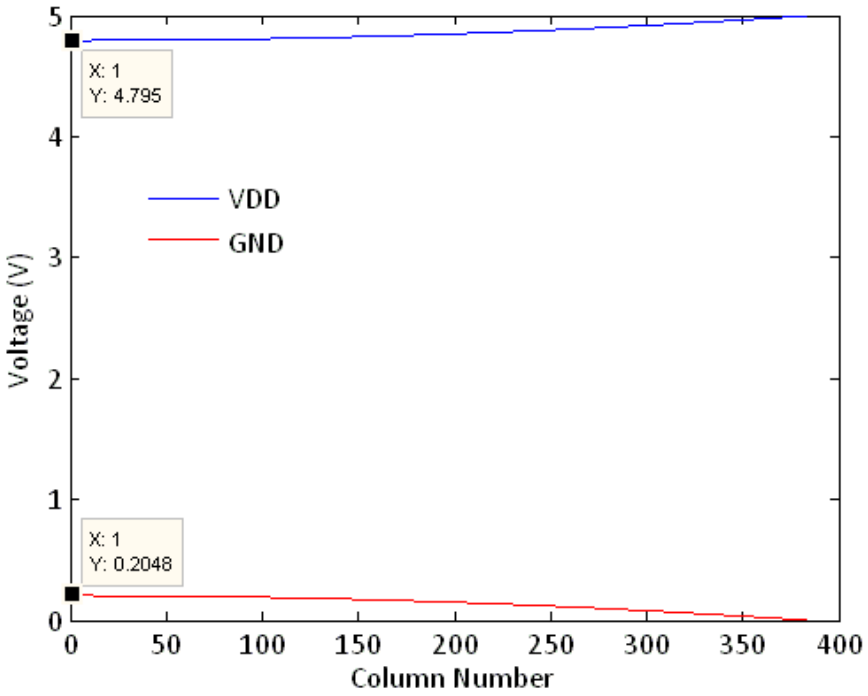
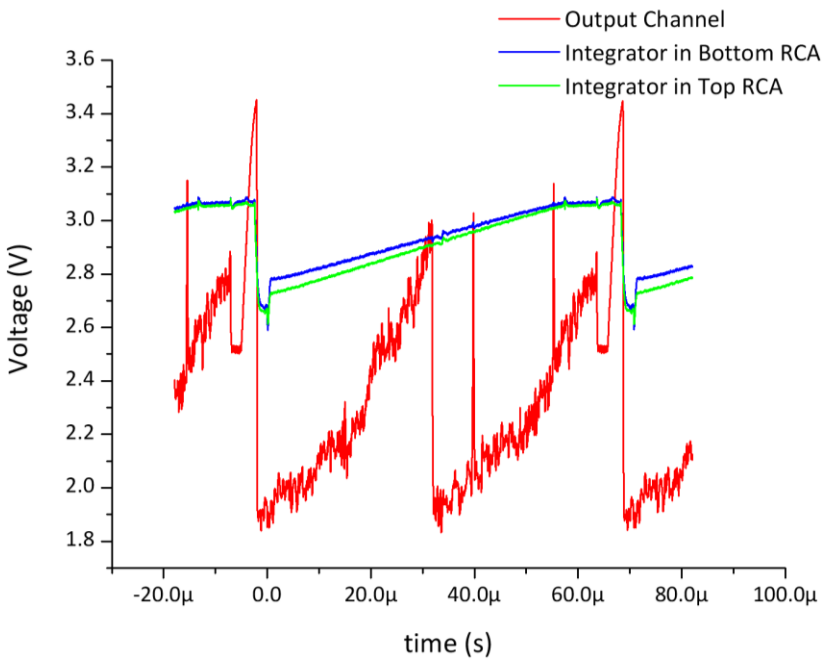
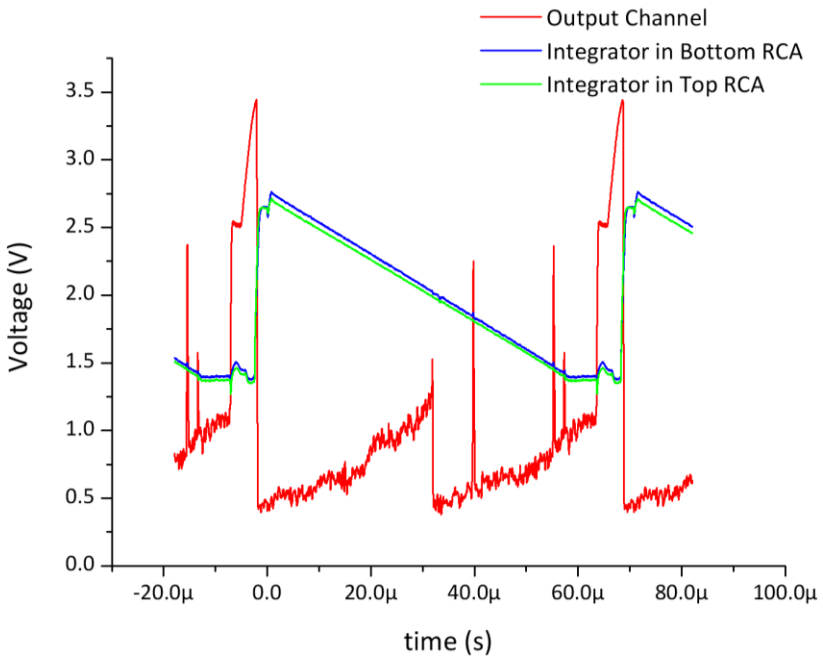


Figure 4.18: Calculated voltage gradient in the supply lines of the self-test pixels for 10 µA average bias current. The values are calculated according to the process specification file of the used 0.6 µm CMOS process.

This test is repeated for different detector bias voltage values in order to check if the array outputs follow the integrator outputs. Figure 4.19 shows the output of the 384x288 FPA readout in single output mode for (a) 3.0 V, and (b) 1.5 V integration output voltages. The indicated integration voltages are for the test channels, which are the rightmost readout channels of the array. The gradient throughout the array is still observed at the output as expected. This figure verifies that the array output follows the integrator outputs, which means that the output sampling and buffering circuitries are working properly.



(a)



(b)

Figure 4.19: Output of the 384x288 FPA readout in single output mode for (a) 3.0 V, and (b) 1.5 V integration output voltages. The indicated integration voltages are for the test channels, which are the rightmost readout channels of the array. The gradient throughout the array is still observed at the output as expected.

4.4 Noise Performance of the Imaging System

After the proper operation of the 384x288 FPA readout is verified, the noise performance of the imaging system is examined. During the tests presented in the previous sections, the PCB was configured for analog output mode. As stated in Section 4.1, there are two 14-bit analog-to-digital converters (ADCs) on the imaging PCB, which can provide digital outputs with a resolution of 305 µV in a 5 V operation range. The digital output mode of the imaging PCB is very suitable for measuring the noise of the system since it is possible to record large amounts of samples with high accuracy using this mode. Therefore, the digital output mode of the PCB is used during the noise measurements.

As stated in Section 3.1, there are two outputs at each channel of the FPA: the first one is the output of the readout channels, and the second one is a reference voltage taken from the first stage of the bias correction DAC structure. The actual channel output is considered as the difference of these two voltages in order to provide a pseudo-differential output, which reduces the sensitivity of the output to the supply voltage variations. The subtraction operation can be directly performed by the AD9240 ADCs on the imaging PCB. Figure 4.20 shows the block diagram of the equivalent functional circuit of AD9240 [57]. As seen in the figure, the AD9240 converts the difference between its two inputs. Therefore, it is possible to get a pseudo-differential output by connecting a readout output and its corresponding reference voltage to the same ADC. Figure 4.21 shows the simplified schematic of the connections between one of the FPA output channels and its corresponding AD9240 converter. The signal paths of the readout output and the reference voltage are identical in order to preserve the differential operation throughout the entire signal bandwidth. Two identical RC filters with a single pole at 11.98 MHz are placed at the inputs of the AD9240 in order to limit the noise bandwidth. The time constant of the filter is

equal to 13.29 ns, which is sufficiently small when compared to 180 ns, which is the output multiplexing time for 50 fps operation with single output channel.

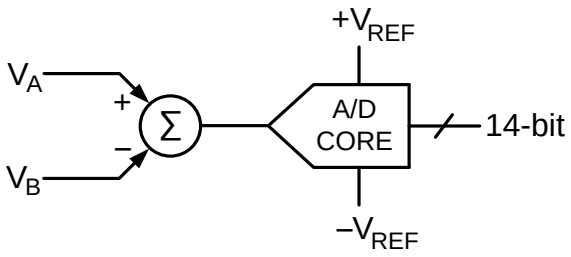


Figure 4.20: Block diagram of the equivalent functional circuit of AD9240 A/D converter [57].

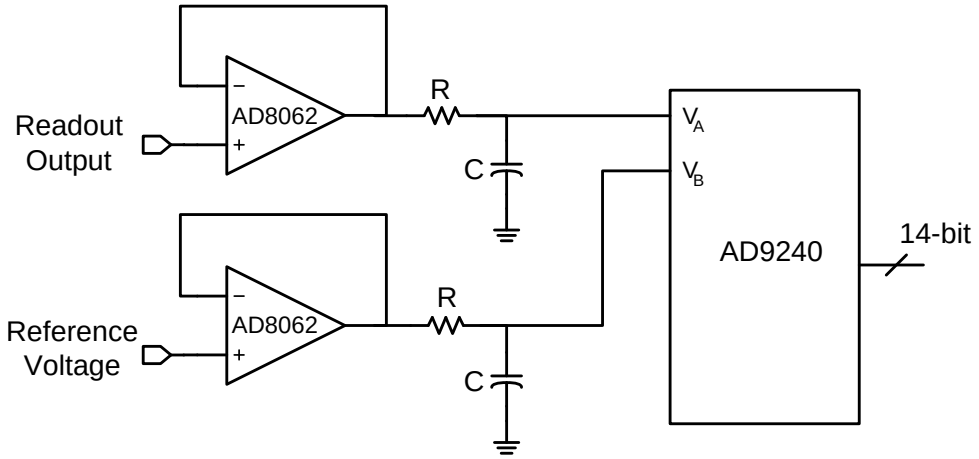


Figure 4.21: Simplified schematic of the connections between an FPA readout output and the corresponding AD9240 A/D converter. The signal paths of the readout output and the reference voltage are identical in order to preserve the differential operation throughout the entire signal bandwidth. Two identical RC filters with a single pole at 11.98 MHz are placed at the inputs of the AD9240 in order to limit the noise bandwidth.

The first test is performed without the FPA readout chip, in order to verify the operation of the ADCs and measure the noise of the test setup. For this purpose, an external voltage is connected to the inputs of the AD8062 buffers instead of FPA outputs. Since the input voltages are shorted and the signal paths are identical, the effective input of the ADC may be considered almost noiseless, and the measured noise is approximately equal to the noise of the test setup and the ADC itself. A/D conversion is performed at the clock frequencies of 5.668 MHz and 2.834 MHz, which correspond to the output multiplexing frequencies at 50 fps operation in single and dual output modes, respectively. Figure 4.22 shows the measured rms noise of the test setup in terms of LSB counts when the ADC is operated at 2.834 MHz and 5.668 MHz. The rms noise values at these frequencies are measured as 0.4293 LSB and 0.4375 LSB, respectively, which correspond to 131.0 µV and 133.5 µV in a 14-bit ADC operating at 5 V range. This result shows that the test setup has an excellent noise performance, and it can be used to measure the noise of the FPA readout.

After the proper operation of the A/D converters are verified and the noise of the test setup is measured, the FPA readout is placed on the PCB and its outputs under different configurations are recorded. Before measuring the output noise, the FPA outputs are recorded for single and dual output modes in order to check if the digitized outputs match the pattern that is observed in the analog output mode. Figure 4.23 shows the reconstruction of the digitized output of the 384x288 FPA readout when operated at 50 fps in single output mode. Similarly, Figure 4.24 shows the reconstruction of the digitized outputs of the (a) top, and (b) bottom RCAs when the readout is operated at 50 fps in dual output mode. These two figures show that the digitized output pattern match with the analog outputs, which means that the A/D conversion operation is performed properly by the imaging system.

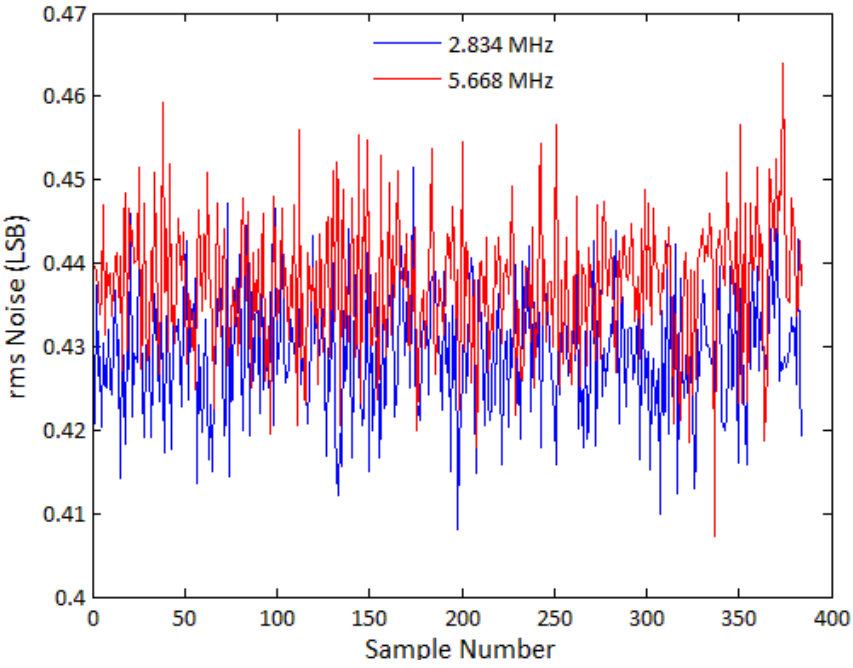


Figure 4.22: Measured rms noise of the test setup in terms of LSB counts when the ADC is operated at 2.834 MHz and 5.668 MHz conversion rates.

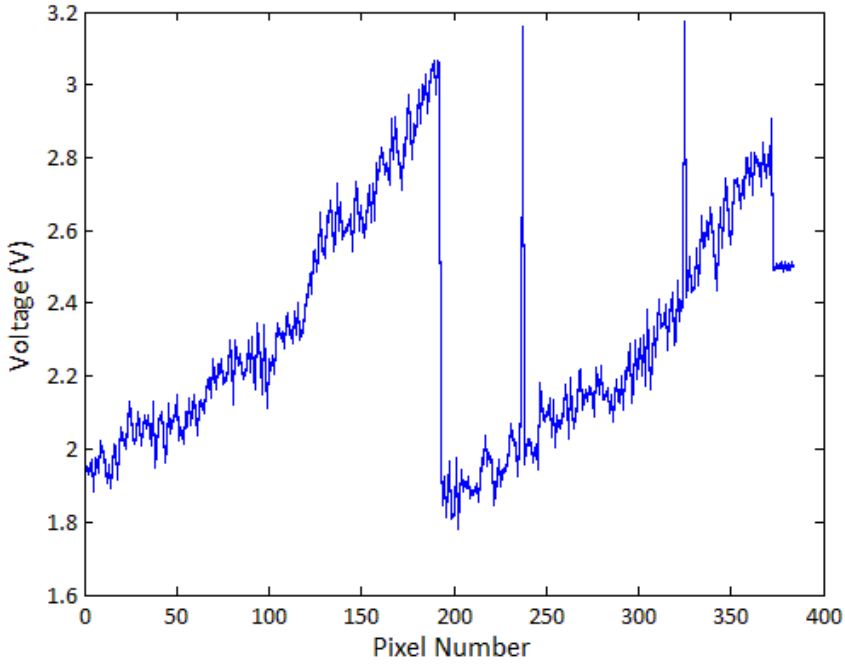
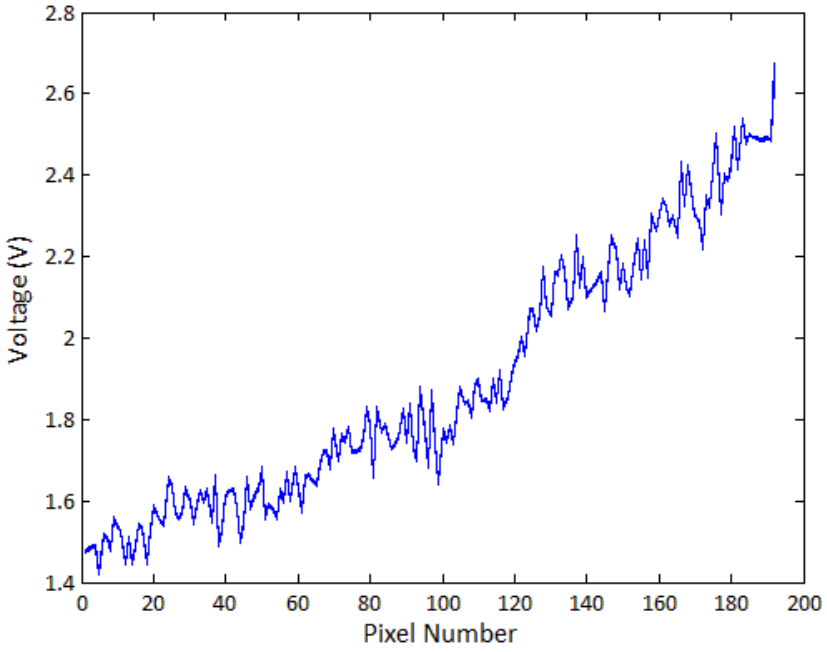
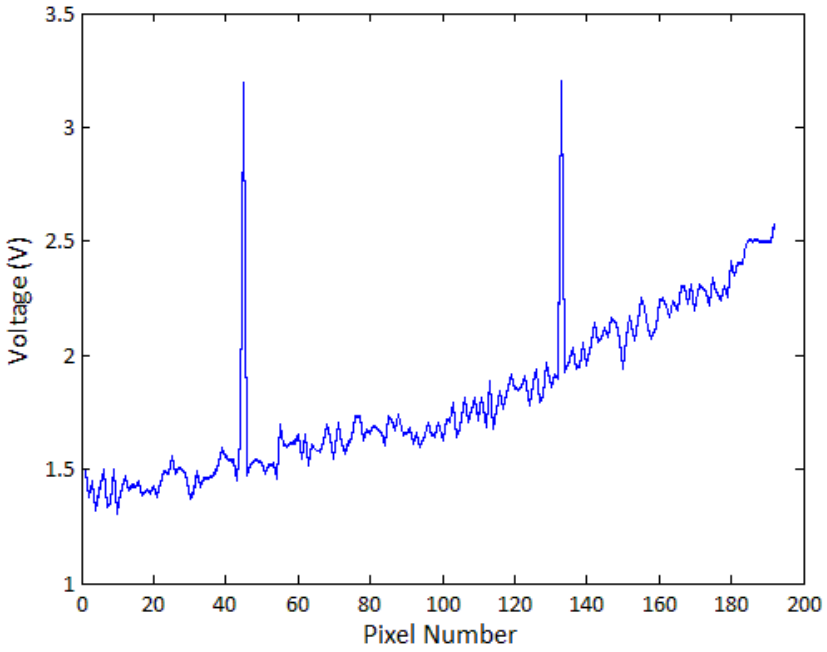


Figure 4.23: Reconstruction of the digitized output of the 384x288 FPA readout operated at 50 fps in single output mode.



(a)



(b)

Figure 4.24: Reconstruction of the digitized outputs of the (a) top, and (b) bottom RCAs when the readout is operated at 50 fps in dual output mode.

After the digital output mode of the imaging system is tested and verified, the noise at the outputs of the 384x288 FPA readout is examined for different configurations. Figure 4.25 shows the measured rms noise of the 384x288 FPA readout for different integration capacitance values when the chip is operated at 50 fps in single output mode. As seen in the figure, the rms noise decreases as the integration capacitance increases, which is an expected result since smaller integration capacitances provide higher gain and hence cause higher output noise. The same procedure is applied for the dual output mode of the chip. Figure 4.26 shows the measured rms noise of the (a) top RCA, and (b) bottom RCA of the 384x288 FPA readout for different integration capacitance values when operated at 50 fps in dual output mode. Similar to the single output case, the rms noise decreases with increasing integration capacitance as expected. Table 4.2 summarizes the measured average rms noise voltages at the output of the designed imaging system for different integration capacitance values when the chip is operated in the self-test mode.

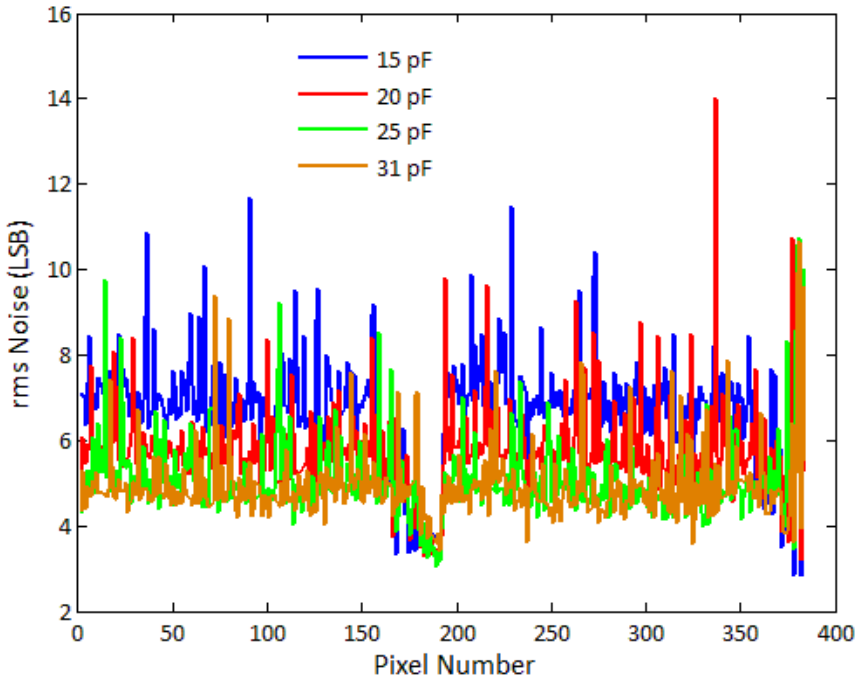
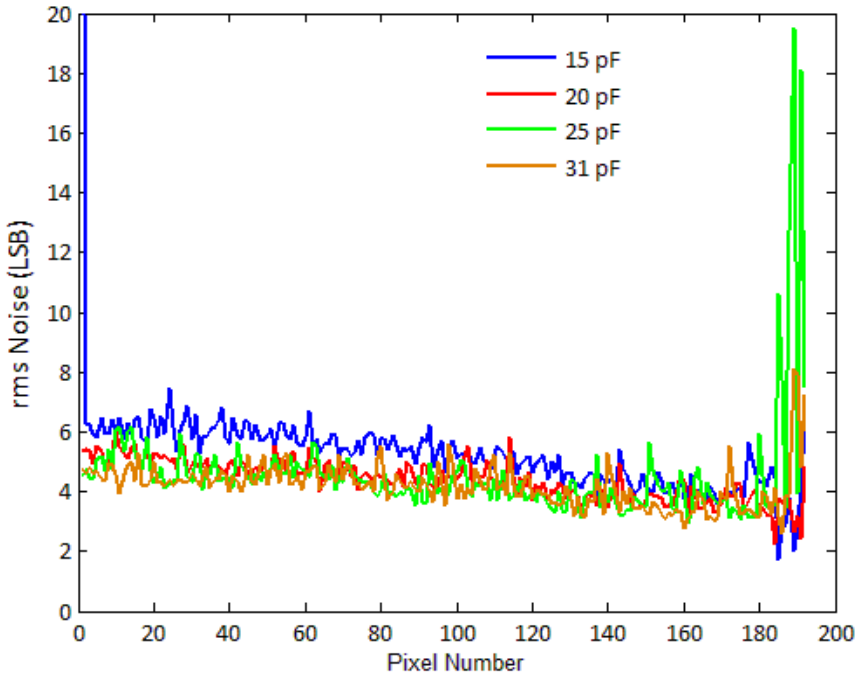
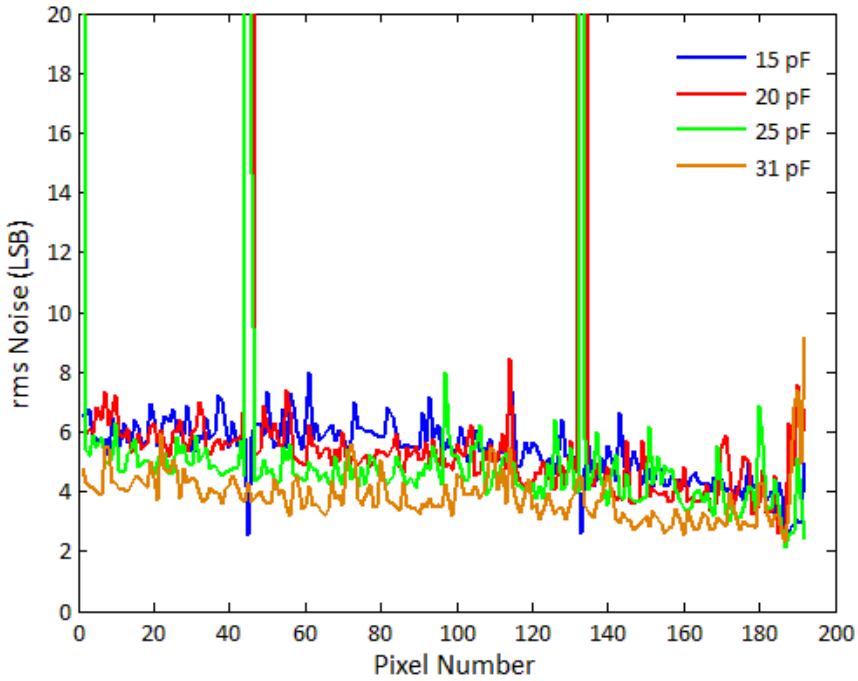


Figure 4.25: Measured rms noise of the 384x288 FPA readout for different integration capacitance values when operated at 50 fps in single output mode. The noise decreases as the integration capacitance increases, which is an expected result since smaller integration capacitances provide higher gain and hence cause higher output noise.



(a)



(b)

Figure 4.26: Measured rms noise of the (a) top RCA, and (b) bottom RCA of the 384x288 FPA readout for different integration capacitance values when operated at 50 fps in dual output mode.

Table 4.2: Measured average rms noise voltages at the output of the designed imaging system for different integration capacitance values when the chip is operated in the self-test mode.

	Single Output	***Dual Output - Top***	***Dual Output - Bottom***
15 pF	2.05 mV	1.58 mV	1.64 mV
20 pF	1.76 mV	1.35 mV	1.63 mV
25 pF	1.55 mV	1.31 mV	1.40 mV
31 pF	1.51 mV	1.28 mV	1.18 mV

The input referred rms noise of the readout is expected to be 53.1 pA for a 20 pF integration capacitance and 50 fps operation frequency. This value corresponds to an output noise of 0.16 mV, which is much smaller than the measured value of 1.76 mV in single output. Although there are some extra noise sources in the measurement such as the poly-Si resistors in the self-test pixels, the noise contribution of these sources are not sufficient to cause such a difference between the theoretical and the measured values. Besides, there are some peaks in the measured noise pattern, which occur near the pixels that cause large output slews. Consequently, the main reason of the output noise may be the fluctuations in the supply voltages during large signal transitions. Figure 4.27 shows the reference voltage, the readout output, and the effective output, which is the difference of these two voltages, taken from the same output channel. The regions where the output is sampled by the ADCs are also labeled in the figure. As seen in the figure, there are fluctuations in the readout output between the output multiplexing instants. The same pattern is observed in the reference voltage, showing that the fluctuations are caused by the variations in the supply voltages during clock transitions. In the ideal case, these fluctuations are completely cancelled by differential operation, and the effective output stays noiseless. However, in the designed readout, there is an asymmetry

between the dependencies of the reference voltage and the readout output to the supply voltage variations. The readout output is referenced to the ground, and it has a relatively high power supply rejection ratio (PSRR). On the other hand, the reference voltage is taken from a resistive ladder connected between the 5 V supply and the ground of the readout, which results in a low PSRR. As a result, the effective output is affected to some extent by supply voltage variations as seen in Figure 4.27. Since the effective output is not completely settled within the sampling regions, the jitters in the ADC clock also cause a noise at the output, which is probably the dominant noise source of the system.

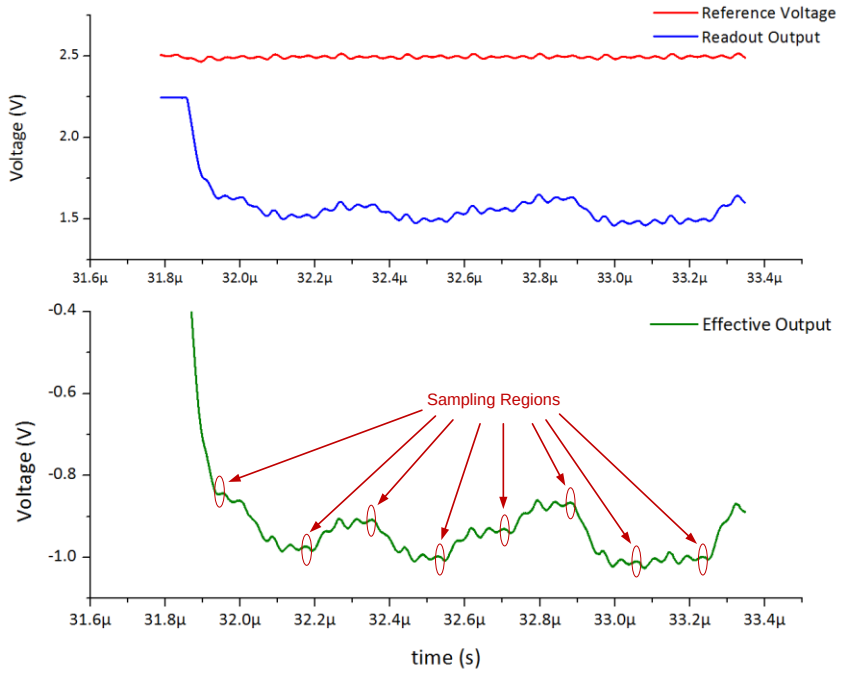


Figure 4.27: Outputs of the top output channel when the readout is operated at 50 fps in single output mode. The regions where the output is sampled by the ADCs are also labeled in the figure. Since the effective output is not completely settled within the sampling regions, the jitters in the ADC clock also cause a noise at the output.

4.5 Power Dissipation of the FPA

The final test conducted on the fabricated 384x288 resistive microbolometer FPA readout is the power measurement. The imaging PCB has a number of regulators for the different supply voltages required by the FPA readout and the other ICs on the PCB. Since there is no direct connection of an external supply voltage to the FPA, there are two alternatives to measure its power dissipation: (i) modifying the PCB by breaking the supply lines to insert a multimeter in series, and (ii) measuring the power dissipation of the readout blocks separately by turning off the blocks using the adjustable bias voltages. The first method is more accurate; however, it may cause permanent damage on the imaging PCB. Furthermore, the PCB consists of four layers, and it is not easy to reach to the intermediate layers, which are used mainly for power distribution. The second method gives only an approximate value for the power dissipation; however, it does not require any modification on the PCB. Therefore, the second method is chosen to measure the power dissipation of the fabricated 384x288 FPA readout.

In order to measure the power dissipation of the circuit, a multimeter is connected to the main power supply of the PCB. First of all, the current drawn by the PCB is measured when the FPA readout is not connected. Then, the FPA readout is connected to the PCB, and the total current is measured again. The difference between the two currents can be considered as the total current drawn by the readout. The total currents drawn by the PCB are 191 mA and 145 mA with and without the FPA readout, respectively.

After measuring the total current drawn by the readout, the power dissipation of the digital blocks is examined. The power dissipation of CMOS type digital gates is directly proportional to the operating frequency, and it can be expressed as

$$P = f \cdot C_{load} \cdot {V_{DD}}^2 \qquad 4.1$$

where f is the operating frequency, C_{load} is the capacitive load at the output, and V_{DD} is the supply voltage. The clock frequency of the readout is changed and the total current is recorded for each frequency in order to approximate the current drawn by the digital gates. Figure 4.28 shows the change in the total current with changing clock frequency and the linear fit curve of the measured data. The total power dissipation of the digital blocks in the readout is approximated as 32 mW by extrapolating the obtained data.

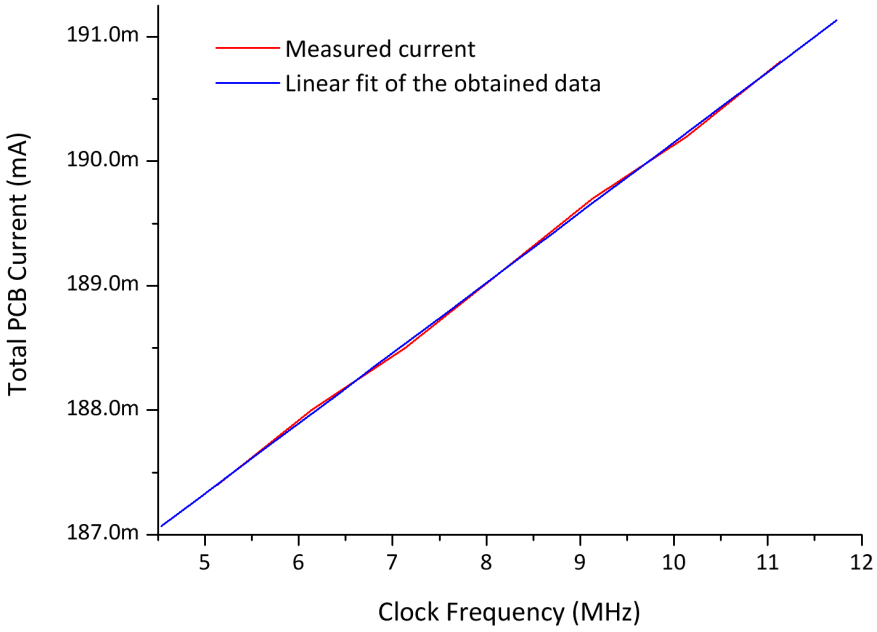


Figure 4.28: Change in the total current with changing clock frequency and the linear fit curve of the measured data. The total power dissipation of the digital blocks in the readout is approximated as 32 mW by extrapolating the obtained data.

After the total power dissipation of the digital blocks is approximated, the currents drawn by the integrator and S&H blocks are measured. In order to measure the power dissipations of these blocks, the bias voltages of the integrator and S&H opamps are connected to external sources by configuring the control interface, and the bias voltages are reduced until the total current is stays constant. The measured power dissipations of the integrator and S&H blocks are 27.1 mW and 30.3 mW, respectively. The same procedure is applied for the RCG and output buffers, and the total power dissipations of these blocks are measured as 11 mW and 10 mW, respectively.

The total current drawn by the aforementioned blocks add up to 20.7 mA. As stated above, the total current drawn by the FPA readout is approximately 46 mA, which means that the remaining currents are drawn by the other blocks. Since all blocks in the readout except the integrator and S&H use 5 V supply, the total power dissipation of the readout can be approximated as 236.9 mW. Table 4.3 summarizes the measured and expected power dissipations of different blocks of the 384x288 FPA readout.

Table 4.3: Summary of the measured and expected power dissipations of different blocks of the 384x288 FPA readout.

	Measured	***Expected***
Integrators	27.1 mW	18.8 mW
S&H Blocks	30.3 mW	20.4 mW
RCG Buffers	11.0 mW	4.16 mW
Output Buffers	10.0 mW	3.37 mW
Digital Blocks	32.0 mW	-
Other	126.5 mW	-
Total	236.9 mW	-

The measured power dissipation of the fabricated readout is higher than its expected value, which may be due to a number of reasons. First of all, the measurement method is not accurate and the results may contain errors to some extent. It is possible that the power dissipations of the ICs on the PCB change when the readout is connected, which means that the increase in the PCB current may not be completely due to the readout. Another possible reason is the underestimation of the capacitive loads of the readout channels and the RCG buffers, which is verified by the difference between the measured and expected currents of the integrator, S&H, and the buffers. Nevertheless, the total power dissipation of the readout is much lower when compared to the 320x240 microbolometer FPA readouts previously designed at METU, which is measured as 900 mW and 700 mW for the first and second generation readouts, respectively. This result shows that the low power readout architecture successfully reduces the power dissipation of the readout.

4.6 Summary and Conclusions

This chapter presented the fabricated 384x288 resistive microbolometer FPA, the imaging system designed for this FPA, the test setup prepared for this system, and the results of the performed tests.

The 384x288 resistive microbolometer FPA readout is fabricated in a standard 0.6 µm CMOS process and occupies an area of 17. 84 mm x 16.23 mm. The chips are fabricated on 6” wafers, which will be processed in METU-MEMS facilities for detector fabrication. One of these wafers is diced for the readout tests, which are described in this chapter.

A 4-layer imaging PCB is prepared for the fabricated readout, which is mainly designed for IR imaging operation. However, it may be used for the tests as well. A test setup is prepared for this PCB, which includes an FPGA board to

generate the digital inputs of the system, a computer to program the FPGA board, and other necessary testing equipment such as a DC power supply and an oscilloscope.

The performed tests are presented in four groups: (i) operation of digital blocks, (ii) operation of analog blocks, (iii) noise performance of the imaging system, and (iv) power dissipation of the readout. The operations of digital and analog blocks are observed directly by using an oscilloscope or a multimeter. Noise measurement is also directly performed using the digital output mode of the imaging PCB. However, the power dissipation is measured using indirect methods due to the compact connections on the imaging PCB.

The digital blocks are tested using the bidirectional I/O cells in the pad frame, which can be used either to observe or to drive the connected digital signals. The output mode of these bidirectional pads are activated by configuring the control interface, and the internally generated digital signals are observed. There are two digital blocks that can be tested by this method: the readout channel control signals block and the output multiplexer, which are both tested for different configuration modes. The test results show that both digital blocks are operating as expected.

The tests of the analog blocks are performed by observing the outputs of three different blocks: (i) bias generation blocks, (ii) individual readout channels, and (iii) FPA output channels. The bias generation blocks are tested by connecting their outputs to bond pads using the analog multiplexers. On the other hand, the readout channels and the FPA output channels require resistors in order to operate. Since the detector and reference pixels are not fabricated yet, these blocks are tested using the self-test pixels.

Self-test pixels, which are poly-Si resistors implemented in the CMOS process, are used for the tests of the readout channels and array outputs. These pixels

are connected to the readout channels instead of the actual detector and reference pixels by configuring the control interface. Besides, important bias voltages are connected to bond pads to be able to control them easily using potentiometers.

The tests of readout blocks are performed in two steps: First, the integrator and S&H outputs of a single readout channel are observed. Then, the analog outputs of both output channels are examined. The single readout channel tests are performed by connecting the integrator and S&H outputs of the rightmost readout channels to bond pads using the control interface. The outputs of these blocks are observed for different integration current values. The output channel tests are performed by observing the outputs of the AD8062 video buffer opamps on the PCB for different integration currents. The obtained results show that the readout channels and output buffering structure are operational as expected.

After the operation of the readout is verified, the noise performance of the imaging system is evaluated. For this purpose, the digital output mode of the imaging PCB is activated. First, the operation of the AD9240 ADCs on the PCB is tested by connecting external voltages to the inputs. The rms noise of the test setup is measured as approximately 0.44 LSB, which is sufficiently low to use this setup for noise measurement of the readout. Then, the correct operation of the digital output mode is verified by comparing the reconstruction of the digital outputs to the analog outputs. Finally, the noise at the outputs of the FPA readout is measured for single and dual output modes. The measured rms noise of the system is approximately 1.76 mV when the chip is operated at 50 fps in single output mode with an integration capacitance of 20 pF. This value is much higher than expected. However, most of the measured noise is probably caused by the asymmetrical dependencies of the reference voltages and the readout

outputs on the supply variations rather than the fundamental electrical noise sources.

Finally, the power dissipation of the readout is measured. There are no external supply connections to the FPA on the PCB, therefore, the measurements are performed using indirect methods. The approximate power dissipation of the 384x288 FPA is measured as 236.9 mW for the same configuration used throughout the tests of the digital and analog blocks. This value is higher than the expected value, which may be due to a number of reasons such as the inaccuracy in the measurement method or underestimation of capacitive loads at the outputs of readout channels. Nevertheless, the measured power dissipation is much smaller when compared to the 320x240 resistive microbolometer readouts previously designed at METU, verifying that the designed low power readout architecture has the intended effect on the power dissipation.

CHAPTER 5

CONCLUSIONS AND FUTURE WORK

The research presented in this thesis covers the development of a high performance and low power CMOS readout circuit for resistive microbolometer focal plane arrays. A new sampling and buffering architecture is developed, which has considerably low power dissipation when compared to conventional architectures. The low power architecture employs an output buffering scheme and a digitally controllable opamp. The output buffering scheme reduces the necessary output current for the readout channels by decreasing the capacitive load at the output; and the digitally controllable opamp further decreases the power dissipation by increasing the power efficiency. Besides the low power sampling and buffering architecture, a new bias correction DAC is designed in order to overcome the drawbacks of the structure used in the previously designed resistive microbolometer FPAs at METU. The new bias correction structure consists of two resistive ladder DACs, which are capable of providing multiple outputs. By taking multiple outputs from a single resistive ladder, the area and power dissipation of the DACs in an FPA readout can be considerably reduced. After the development of the low power readout architecture, a 384x288 resistive microbolometer FPA readout with 35 µm pixel pitch which employs the designed low power architectures is designed and fabricated in a standard 0.6 µm process. Finally, a 4-layer imaging PCB is prepared in order to form a complete imaging system together with the microbolometer FPA. The

tests of the fabricated chip are also performed using this PCB. The results of the performed tests show that the fabricated readout is operating properly. The rms output noise of the imaging system and the power dissipation of the readout at 50 fps operation frequency are measured as 1.76 mV and 236.9 mW, respectively.

The achievements during the research presented in this thesis can be summarized as follows:

1. Resistive microbolometer FPA readouts previously designed at METU are investigated and the drawbacks of these circuits are studied. As a result, the research is focused on reducing the power dissipation. In order to overcome this disadvantage, a low power sampling and buffering architecture is developed. According to the test results, the low power architecture is expected to have a power dissipation of 25.2 mW when implemented in a 384x288 FPA with 35 µm pixel pitch operating at 50 fps with two output channels. This value corresponds to an improvement of 91.6% when compared to the 281 mW power dissipation of the conventional structure, which is calculated according to the same test results. Another improvement on the previous FPA readouts is provided by designing a new bias correction DAC structure. The improved structure uses resistive ladder type DACs, which are capable of giving multiple outputs from a single ladder. By using a single ladder to bias multiple transistors, the area and power dissipation of the DACs can be greatly reduced. As a result, it would be possible to implement a dedicated DAC for each readout channel, which eliminates the need for the sampling operation performed in the previous designs. Elimination of sampling improves the noise performance since the noise bandwidth is shifted towards the baseband during sampling.

2. A readout channel suitable for large format microbolometer FPAs with 35 µm pixel pitch is designed for the first time at METU. The readout channel is designed in a standard 0.6 µm CMOS process, and it has 70 µm width. By placing the designed readout channels to both upper and lower sides of the FPA, it is possible to implement a single readout channel for each column; which increases the available integration time, and consequently, increases the responsivity and decreases the noise bandwidth.

3. A 384x288 resistive microbolometer FPA readout that is suitable for real camera applications is designed and fabricated. In real camera applications, the key parameters are low power dissipation, low number of bond pads and output channels, an output system compatible with standard video systems, and operational controllability. Low power dissipation is achieved by using the low power sampling and buffering architecture and the new bias correction structure. In order to decrease the number of required bond pads while keeping the controllability on the FPA parameters, a serially programmable control interface is implemented in the readout. The FPA has single and dual output channel modes, and the analog readout is capable of settling the output within the time duration required by PAL video standard.

4. A 4-layer imaging PCB is designed in order to form a camera system using the 384x288 FPA after the fabrication of the detectors. The PCB can also be used to test the readout. The digital and analog blocks are tested, and the output noise of the system and the power dissipation of the readout are measured using this PCB. The results show that the readout is operating properly at 50 fps, the rms output noise is 1.76 mV, and the power dissipation of the readout is 236.9 mW. Although the power dissipation is higher than expected, it is much smaller when compared to the 700 mW

power dissipation of the second generation readout previously designed at METU, verifying that the low power architecture is functional.

Despite the extensive effort to reach the important achievements listed above, there are some future works to be performed on this study:

1. After the detectors are implemented using post-CMOS MEMS processes, IR images should be taken using the fabricated readout. The imaging PCB is compatible with dewars; therefore, it is possible to obtain IR images using the current setup. The pixel resistances should be measured after the fabrication in order to be able to apply bias correction to the detectors.

2. Output driving capability of the FPA should be improved in order to be able to drive different type of loads. Currently, the output channels of the FPA is capable of driving only capacitive loads up to 10 pF, which mandates the use of external buffers with low input capacitance.

3. The pseudo-differential output operation of the readout should be improved by using a reference voltage with a PSRR characteristic which is similar to that of the readout outputs in order to decrease the overall system noise.

4. On-chip analog-to-digital converters should be designed in order to be able to obtain the digital outputs directly from the FPA. This approach reduces the corruption of the analog output by external noise sources, and simplifies the required external imaging circuitry.

REFERENCES

[1] C. Bigwood, L. Eccles, A. Jones, B. Jones, D. Meakin, S. Rickard, and R. Robinson, "Thermal imager for dismounted infantry," *Electro-Optical and Infrared Systems: Technology and Applications,* SPIE Vol. 5612, pp. 160-171, 2004.

[2] T. Breen, M. Kohin, C. A. Marshall, R. Murphy, T. White, A. Leary, and T. Parker, "Even more applications of uncooled microbolometer sensors," *Infrared Technology and Applications XXV*, SPIE Vol. 3698, pp. 308-319, 1999.

[3] C. Hornberger, "Application of military uncooled infrared sensors to homeland defense," *Sensors, and Command, Control, Communications, and Intelligence (C3I) Technologies for Homeland Defense and Law Enforcement*, SPIE Vol. 4708, pp. 201-211, 2002.

[4] F. Amon, N. Bryner, and A. Hamins, "Evaluation of thermal imaging cameras used in fire fighting applications," *Infrared Imaging Systems: Design, Analysis, Modeling, and Testing XV,* SPIE Vol. 5407, pp. 44-53, 2004.

[5] C. Vieider, S. Wissmar, P. Ericsson, U. Halldin, F. Niklaus, G. Stemme, J.-E. Källhammer, H. Pettersson, D. Eriksson, H. Jakobsen, T. Kvisterøy, J. Franks, J. VanNylen, H. Vercammen, and A. VanHulsel, "Low-cost far infrared bolometer camera for automotive use," *Infrared Technology and Applications XXXIII,* SPIE Vol. 6542, pp. 65421L, 2004.

[6] C. H. Jones, "Medical thermography," *Physical Science, Measurement and Instrumentation, Management and Education, Reviews, IEE Proceedings A,* Vol. 134, pp. 225-236, 1987.

[7] P. W. Kruse, *Uncooled Thermal Imaging Arrays, Systems and Applications*: SPIE Press, 2001.

[8] P. W. Kruse and D. D. Skatrud, "Uncooled Infrared Imaging Systems and Arrays," *Semiconductor and Semimetals*, Vol. 47: Academic Press, 1997.

[9] H. Lakdawala and G. K. Fedder, "CMOS micromachined infrared imager pixel," *Technical Digest of the IEEE 11th Int. Conf. on Solid-State Sensors and Actuators*, Vol. pp. 1548-1551, 2001.

[10] C.-C. Liu and C. H. Mastrangelo, "A CMOS uncooled heat-balancing infrared imager," *IEEE Journal of Solid-State Circuits,* Vol. 35, pp. 527-535, 2000.

[11] R. A. Wood, "Uncooled thermal imaging with monolithic silicon focal arrays," *Infrared Technology XIX*, SPIE Vol. 2020, pp. 322-329, 1993.

[12] D. Murphy, M. Ray, A. Kennedy, J. Wyles, C. Hewitt, R. Wyles, E. Gordon, T. Sessler, S. Baur, and D. V. Lue, "High sensitivity 640 × 512 (20 µm pitch) microbolometer FPAs," *Infrared Technology and Applications XXXII*, SPIE Vol. 6206, pp. 62061A, 2006.

[13] H. Wada, M. Nagashima, M. Kanzaki, T. Sasaki, A. Kawahara, Y. Tsuruta, N. Oda, and S. Matsumoto, "Fabrication process for 256 x 256 bolometer-type uncooled infrared detector," *Micromachined Devices and Components III*, SPIE Vol. 3224, pp. 40-51, 1997.

[14] J. J. Yon, L. Biancardini, E. Mottin, J. L. Tissot, and L. Letellier, "Infrared microbolometer sensors and their application in automotive safety," *7th International Conference on Advanced Microsystems for Automotive Applications*, pp. 137-157, 2003.

[15] S. Eminoğlu, D. S. Tezcan, M. Y. Tanrıkulu, and T. Akın, "Low-cost uncooled infrared detectors in CMOS process," *Sensors and Actuators A,* Vol. 109, pp. 102-113, 2003.

[16] X. He and G. Karunasiri, "Performance of microbolometer focal plane arrays under varying pressure," *IEEE Electron Device Letters,* Vol. 21, pp. 233-235, 2000.

[17] A. Fraenkel, U. Mizrahi, L. Bikov, A. Adin, E. Malkinson, A. Giladi, D. Seter, and Z. Kopolovich, "VOx - based uncooled microbolometric detectors: recent developments at SCD," *Infrared Technology and Applications XXXII,* SPIE Vol. 6206, pp. 62061C, 2006.

[18] K. A. Hay, "Large format VOx microbolometer UFPA development at ITC," *Infrared Detectors and Focal Plane Arrays VII*, SPIE Vol. 6295, pp. 629505, 2006.

[19] M. Almasri and J. Castracane, "Amorphous silicon two-color microbolometer for uncooled IR detection," *IEEE Sensors Journal,* Vol. 6, pp. 293-300, 2006.

[20] B. Fièque, P. Robert, C. Minassian, M. Vilain, J. L. Tissot, A. Crastes, O. Legras, and J. Yon, "Uncooled amorphous silicon XGA IRFPA with 17µm pixel-pitch for high end applications," *Infrared Technology and Applications XXXIV,* SPIE Vol. 6940, pp. 69401X/1-5, 2008.

[21] S. Kavadias, P. D. Moor, M. Gastal, N. Hendrikx, F. Wirix, and C. A. V. Hoof, "Hybrid long-wavelength IR sensor based on a linear array of poly Si-Ge uncooled microbolometers with a CMOS readout " *Sensors, Systems, and Next-Generation Satellites IV,* SPIE Vol. 4169, pp. 348-355, 2003.

[22] Z. Celik-Butler, D. P. Butler, and A. Yildiz, "Room temperature YBaCuO infrared detectors on a flexible substrate," *Infrared Detectors and Focal Plane Arrays VII*, SPIE Vol. 4721, pp. 260-268, 2003.

[23] C. M. Travers, A. Jahanzeb, D. P. Butler, and Z. Celik-Butler, "Fabrication of Semiconducting YBaCuO Surface-Micromachined Bolometer Arrays," *Journal of Microelectromechanical Systems,* Vol. 6, pp. 271-276, 1997.

[24] A. Rogalski, "Infrared detectors: status and trends," *Progress in Quantum Electronics,* Vol. 27, pp. 59-210, 2003.

[25] F. Niklaus, C. Vieider, and H. Jakobsen, "MEMS-Based uncooled infrared bolometer arrays – a review," *MEMS/MOEMS Technologies and Applications III*, SPIE Vol. 6836, pp. 6836D/1-15, 2007.

[26] Ö. Ö. Yıldırım, "High Performance Readout Electronics for Uncooled Infrared Detector Arrays," M. S. Thesis, Middle East Technical University, 2006.

[27] R. W. Boyd, *Radiometry and the Detection of Optical Radiation*: John Wiley and Sons, 1984.

[28] A. Tanaka, K. Chibaa, T. Endoha, Kuniyuki Okuyamaa, A. Kawaharab, K. lidab, and N. Tsukamotoc, "Low-noise readout circuit for uncooled infrared FPA," *Infrared Technology and Applications XXVI*, SPIE Vol. 4130, pp. 160-167, 2000.

[29] S. Eminoğlu, "Uncooled Infrared Focal Plane Arrays With Integrated Readout Circuitry Using MEMS and Standard CMOS Technologies," Ph. D. Dissertation, Middle East Technical University, 2003.

[30] C. H. Hwang, D. H. Woo, Y. S. Lee, and H. C. Lee, "Readout integrated circuit for microbolometer with an analog non-uniformity correction," *Infrared Components and Their Applications,* SPIE Vol. 5987, pp. 59870P, 2005.

[31] E. Mottin, A. Bain, J. Martin, J. Ouvrier-Buffet, S. Bissotto, J. J. Yon, and J. L. Tissot, "Uncooled amorphous silicon technology enhancement for 25 µ pixel pitch achievement," *Infrared Technology and Applications XXVIII,* SPIE Vol. 4820, pp. 200-207, 2003.

[32] J. L. Tissot, J. P. Chatard, S. Tinnes, and B. Fieque, "320x240 uncooled microbolometer 2D array for radiometric and process control applications," *Detectors and Associated Signal Processing,* SPIE Vol. 5251, pp. 114-120, 2004.

[33] C. H. Hwang, C. B. Kim, Y. S. Lee, and H. C. Lee, "Pixelwise readout circuit with current mirroring injection for microbolometer FPAs," *IEEE Electronic Letters,* Vol. 44, pp. 732-733, 2008.

[34] P. E. Howard, J. E. Clarke, A. C. Ionescu, C. C. Li, and J. C. Stevens, "DRS U6000 640x480 VOx uncooled IR focal plane," *Infrared Detectors and Focal Plane Arrays VII*, SPIE Vol. 4721, pp. 48-55, 2002.

[35] T.-H. Yu, C.-Y. Wu, Y.-C. Chin, P.-Y. Chen, F.-W. Chi, J.-J. Luo, C. D. Chiang, and Y.-T. Cherng, "A new CMOS readout circuit for uncooled bolometeric infrared focal plane arrays," *ISCAS 2000*, Vol. 2, pp. 493-496, 2000.

[36] J.-K. Kim and C.-H. Han, "A new uncooled thermal IR detector using silicon diode," *Sensors and Actuators A,* Vol. 89, pp. 22-27, 2000.

[37] T. Ishikawa, M. Ueno, K. Endo, Y. Nakaki, H. Hata, T. Sone, M. Kimata, and T. Ozeki, "Low-cost 320x240 uncooled IRFPA using a conventional silicon IC process," *Infrared Technology and Applications XXV*, SPIE Vol. 3698, pp. 556-564, 1999.

[38] S. Eminoğlu, M. Y. Tanrikulu, and T. Akın, "Low-cost uncooled infrared detector arrays in standard CMOS," *Infrared Technology and Applications XXIX,* SPIE Vol. 5074, pp. 425-436, 2003.

[39] S. Eminoğlu, M. Y. Tanrıkulu, and T. Akın, "A low-cost 64x64 uncooled infrared detector arrays in standard CMOS," *The 12th Int. Conf. on Solid-State Sensors and Actuators (TRANSDUCERS'03, Eurosensors XV),* Boston, USA, pp. 316-319, 2003.

[40] W. J. Parrish and J. T. Woolaway, "Methods and circuitry for correcting temperature-induced errors in microbolometer focal plane array," U. S. Patent 6028309, Feb. 22, 2000.

[41] S.-x. Xing, J. Zhang, L. Sun, B.-k. Chang, and Y.-s. Qian, "Two-point nonuniformity correction based on LMS," *Infrared Components and Their Applications,* SPIE Vol. 5640, pp. 130-136, 2005.

[42] H.-x. Zhou, R. Lai, S.-q. Liu, and G. Jiang, "New improved nonuniformity correction for infrared focal plane arrays," *Optics Communications,* Vol. 245, pp. 49-53, 2005.

[43] B. Zhou, Y. Wanga, Y. Yeb, X. Wuc, and J. Yinga, "Realized multi-point method for real-time correction of nonuniformity of uncooled IRFPA," *Infrared Components and Their Applications,* SPIE Vol. 5640, pp. 368-375, 2005.

[44] D. R. Droege, "Scene-based nonuniformity correction using texture-based adaptive filtering," *Infrared Technology and Applications XXXIII*, SPIE Vol. 6542, pp. 65423R/1-12, 2007.

[45] B. M. Ratliff and M. M. Hayat, "An algebraic algorithm for nonuniformity correction in focal-plane arrays," *Journal of the Optical Society of America A,* Vol. 19, pp. 1737-1747, 2002.

[46] M. Tepegöz, A. Toprak, and T. Akın, "A low power readout circuit approach for uncooled resistive microbolometer FPAs," *Infrared Technology and Applications XXXIV*, SPIE Vol. 6940, pp. 694026/1-8, 2008.

[47] E. Alpman, "Development of Low-Cost Uncooled Infrared Detector Arrays in Standard CMOS and SOI-CMOS Processes," M.S. Thesis, Middle East Technical University, 2005.

[48] K. S. Demirci, "A Low-Cost 16x16 Uncooled Infrared Detector FPA Using Standard CMOS and Wafer Level MEMS Processes," M.S. Thesis, Middle East Technical University, 2005.

[49] M. B. Dayanık, "Low-Cost High Performance Infrared Detectors in SOI-CMOS Technology," M.S. Thesis, Middle East Technical University, 2007.

[50] E. İncetürkmen, "A Low-Cost 128x128 Uncooled Infrared Detector Array in a Standard SOI-CMOS Technology," M.S. Thesis, Middle East Technical University, 2008.

[51] M. Y. Tanrıkulu, "An Uncooled Infrared Microbolometer Detector Array Using Surface Micromachined MEMS Technology," Ph. D. Dissertation, Middle East Technical University, 2007.

[52] A. Fraenkel, U. Mizrahi, L. Bikov, A. Giladi, A. Adin, N. Shiloah, E. Malkinson, T. Czyzewski, A. Amsterdam, and Y. Sinai, "BIRD640: SCD's High Sensitivity VGA VOx μ-Bolometer Detector," *Electro-Optical and Infrared Systems: Technology and Applications IV*, SPIE Vol. 6737, pp. 67370U, 2007.

[53] B. Razavi, *Design of Analog CMOS Integrated Circuits*: McGraw-Hill, 2001.

[54] K. S. Kundert, "Simulating Switched-Capacitor Filters with SpectreRF," The Designer's Guide, 2003. [Online]. Available: http://www.designers-guide.org/Analysis/sc-filters.pdf. [Accessed: 27.12.2008].

[55] A. Tanaka, Y. Tanka, T. Endoh, K. Okuyama, and K. Kawano, "A non-uniformity correction scheme using multiple analog buses for an uncooled infrared sensor," *IEEE Symposium on VLSI Circuits*, Vol. pp. 161-164, 2003.

[56] Analog Devices, "Low Cost, 300 MHz Rail-to-Rail Amplifiers," AD8061/AD8062/AD8063 datasheet, Nov. 1999, [Revised Oct. 2007].

[57] Analog Devices, "Complete 14-Bit, 10 MSPS Monolithic A/D Converter," AD9240 datasheet, Nov. 1998.