DESIGN AND DIGITAL IMPLEMENTATION OF THYRISTOR CONTROLLED REACTOR CONTROL

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DESIGN AND DIGITAL IMPLEMENTATION OF THYRISTOR CONTROLLED REACTOR CONTROL

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ABSTRACT

DESIGN AND DIGITAL IMPLEMENTATION OF THYRISTOR CONTROLLED REACTOR CONTROL

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In this research work, the control system of 16 MVAr, 13.8 kV TCR will be designed and digitally implemented. A Real-Time Control System (NI CompactRIO™ Reconfigurable I/O) and a Digital Platform (NI LabVIEW™ G-code) are used in the digital implementation of TCR control system. The digital control system is composed of reactive power calculation, firing angle determination and triggering pulse generation blocks. The performance of control system will be tested in the field. The simulation results will also be compared with test data.

Keywords: Reactive Power Compensation, Thyristor Controlled Reactor (TCR), Real-Time controller, LabVIEW, CompactRIO.

ÖZ

TRİSTÖR KONTROLLÜ REAKTÖR KONTROLÜ TASARIMI VE SAYISAL GERÇEKLEŞTİRMESİ

Genç, Murat
Yüksek Lisans, Elektrik ve Elektronik Mühendisliği Bölümü
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Aralık 2007, 116 sayfa

Bu araştırma çalışmasında, 16 MVAr, 13,8 kV TKR'nin kontrol sistemi tasarlanacak ve sayısal olarak gerçekleştirilecektir. TKR Kontrol sisteminin sayısal gerçekleştirilmesinde Gerçek Zamanlı Kontrol Sistemi (NI CompactRIO Reconfigurable I/O) ve Sayısal Platform (NI LabVIEW G-code) kullanılacaktır. Kontrol sistemi reaktif güç hesabı, ateşleme açısı belirlemesi ve tetikleme sinyali üretimi bloklarını içermektedir. Kontrol sisteminin performansı sahada test edilecektir. Ayrıca, benzetim sonuçları test verisi ile karşılaştırılacaktır.

Anahtar Kelimeler: Reaktif Güç Kompanzasyonu, Tristör Kontrollü Reaktör (TKR), Gerçek zamanlı kontrollör, LabVIEW, CompactRIO.

to my grandmother Ayşe

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This industrial system developed within the scope of this research work is a part of the turn-key project (Project No: 7050503) carried out by TÜBİTAK-UZAY for ERDEMİR Iron & Steel Inc. I would like to acknowledge TÜBİTAK-UZAYfor allowing this reseach work.

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INTRODUCTION

1.1 OVERVIEW

With the advance in modern industrial plants, consuming electrical energy, significant problems arise. These are;

- Reactive power consumption of industrial loads from the supply
- Harmonic currents injected by the loads to the supply
- Unbalanced loading of the supply because of unbalance operation of some industrial loads
- Light flicker arising from voltage fluctuations
- Further power quality problems arise from nonlinear industrial loads such as electric arc furnaces, ladle furnaces, rolling mils, excavating machines, transportation systems, etc.

These problems are solved by the use of FACTS to a great extent these are ranging from TCR based SVC to STATCOM [1] [2] [3][4][5][6][7].

This research work deals with the design and implementation of a real-time digital controller for TCR based SVC systems.

TCR based SVCs should follow the rapidly changing reactive power demand of loads closely. In general, since rapidly changing loads are also unbalanced loads, each SVC phase must be controlled separately [1] [8][9].

For the accurate and redundant operation of SVC, digital implementation is selected for the controller of SVC. Noise immunity, accuracy of arithmetic operations, ability for modularity structure, and improved sensitivity to parameter variations in digital electronics made the choice of digital option for implementation of TCR controller more advantageous as compared to the analog counter part.

Further than this, the digital controller provides more flexibility. Modification in the field and development is easier because the implementation is markedly based on software. Most of the modifications are done by changing the code installed into the digital components as ICs, compact devices. Moreover, due to the ability of complex arithmetic calculations of digital implementation, performance of the controller is increased as compared to the analog controller.

Since, digital electronics do not require calibration and maintenance as much as analog electronics, changing the application does not require major changes in hardware but only minor modifications in software.

For the implementation platform NI cRIO 9004 Real-Time Controller and NI cRIO 9104 Reconfigurable Embedded Chassis are used for the TCR controller. More information about NI cRIO is available in Appendix (A). The software of the controller is built on NI LabVIEW program compatible with NI cRIO RT controller. The software is available in Appendix (B).

The implemented controller has been tested on the reactive power compensation system of ladle furnace of Ereğli Iron & Steel Works. PI based feedback, feedforward, hybrid and adaptive control strategies have been tried out theoretically and experimentally.

1.2 SCOPE OF THE STUDY

In this study, the control system of TCR has been designed and digitally implemented on NI CompactRIO Real-Time controller platform. This controller is used in the TCR type compensation system of ERDEMİR Iron and Steel Co., Turkey. The compensation system includes 32 MVAr TCR, 14.2 MVAr C-type 2^{nd} harmonic filter and 16 MVAr 2^{nd} order 3^{rd} harmonic filter and it is connected to the low voltage side of 154/13.8 kV transformer at TEİAŞ switchyard within the ERDEMİR campus. This system is designed to compensate the reactive power of ladle furnaces of the factory.

The control system is tested in the field with different type of control algorithms feedback (PI), feedforward (FF), hybrid (PI+FF) and adaptive control. The results are discussed according to the resultant reactive power measurements acquired by the field measurements carried out by DAQ systems.

The outline of the thesis is as follows;

In Chapter 2, description and operating principles of TCR based SVC is described. After explaining the basic definitions of SVC and TCR, operation principles and reactive power control by TCR are described. The ladle furnace, its operation and its electrical characteristic are also described in this chapter. Passive filtering method for harmonic filtering is described and the damping factor is examined. Lastly, SVC design procedure is explained to have the optimum system.

In Chapter 3, power system of the SVC is described. The connections of the elements to the power system are explained. The control of TCR based SVC is examined and the control algorithm of an SVC is explained mathematically for positive and negative sequence compensation. The structure of control stage and closed loop control diagram are given. The parts of electronic TCR controller are identified and their functions and operating principles are explained. Also the real-time controller's codes are explained.

In Chapter 4, the simulations of the SVC system are carried out. For feedback control, the effects of PI parameters are examined and the optimum parameter values are obtained by trial and error method. The contribution of feedforward loop to the response time of the system is examined. An adaptive control method is simulated and its operation is explained.

In Chapter 5, the field measurement results are given. The resultant incoming busbar reactive powers for different control strategies are examined and the results are compared with the theoretical ones given in Chapter 4.

In Chapter 6, general conclusions are given.

CHAPTER 2

TCR BASED SVC

2.1 GENERAL

In an AC electrical system, *active power (P)* is the power consumed by the resistive loads in an electrical circuit. *Reactive power (Q)* is the power generated in an AC circuit because of the expansion and the collapse of magnetic (inductive) and electrostatic (capacitive) fields. Reactive power is expressed in Volt-Amperes-reactive (VAr) (Figure 2.1). These are given in Equations 2.4-2.6 for purely sinusoidal voltages and currents. In a single phase AC circuit;

$$V = \frac{\hat{V}}{\sqrt{2}}\cos(\omega t) \qquad 2.1$$

$$I = \frac{\hat{I}}{\sqrt{2}}\cos(\omega t + \theta) \qquad 2.2$$

$$\omega = 2\pi f \qquad 2.3$$

$$P = V_{rms} I_{rms} \cos(\theta) \qquad 2.4$$

$$Q = V_{rms} I_{rms} \sin(\theta) \qquad 2.5$$

$$S = \sqrt{P^2 + Q^2} \qquad 2.6$$

$$pf = \frac{P}{S} \qquad 2.7$$

Unlike active power, reactive power is not a useful power. Reactive energy is stored by inductors since they expand and collapse their magnetic fields in an attempt to keep their current constant and it is also stored by capacitors since they charge and discharge in an attempt to keep their voltage constant. Circuit inductance and capacitance consume and give back the reactive energy. The power delivered to the inductance is stored in the magnetic field when the field is expanding and it is returned to the source when the field collapses. The power delivered to the capacitance is stored in the electrostatic field when the capacitor is charging and returned to the source when the capacitor discharges. The active power, which is the power consumed is consumed over one cycle, is thus zero for inductive and capacitive elements.

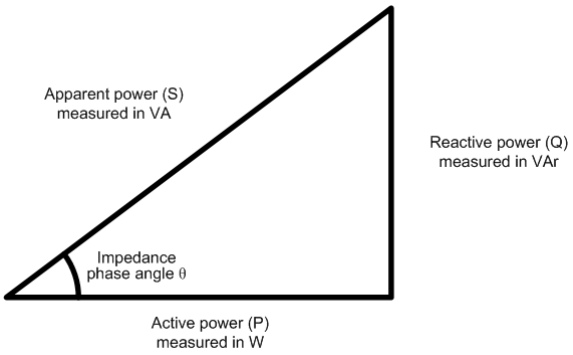


Figure 2.1. Power triangle

2.2 STATIC VAr COMPENSATOR

Static VAr compensator (SVC) is a fast acting reactive power compensator device connected to a high or medium voltage power network to supply the required reactive power by electrical loads. It contains some of the compensation devices such as TCR, thyristor switched capacitor (TSC), thyristor switched reactor (TSR), fixed capacitor (FC), fixed filter (FF) as illustrated in Figure 2.2.

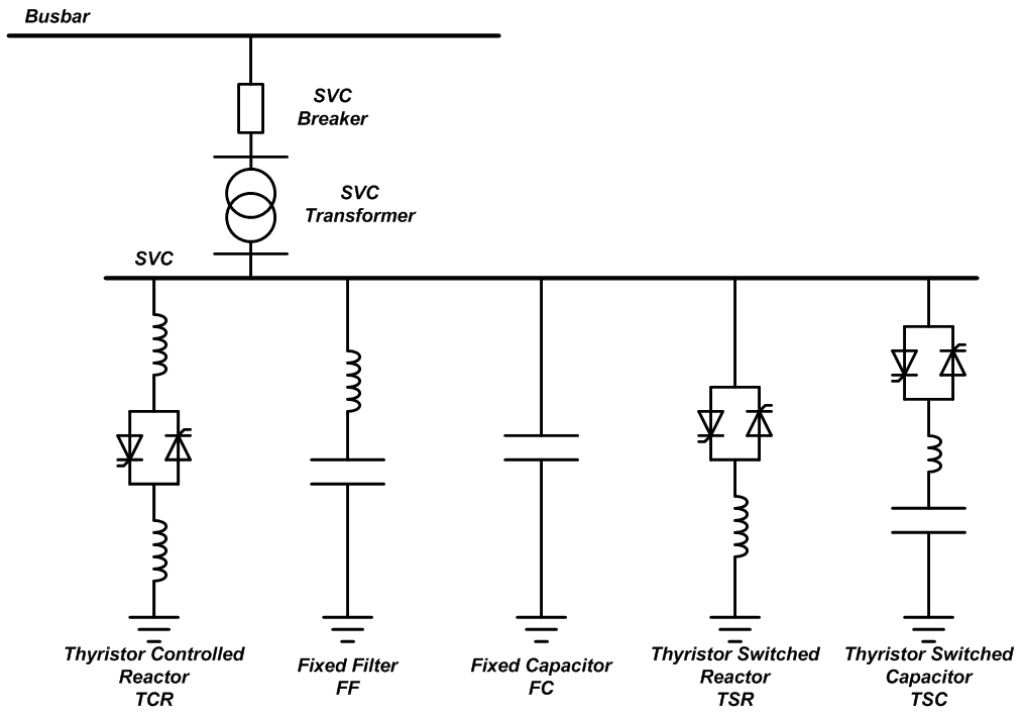


Figure 2.2. Basic scheme of SVC

The SVC is an automated impedance matching device. It measures the reactive power of the power system and calculates the required reactive power for compensation. The required reactive power is generated by phase angle modulation of thyristor switches. Since the reactive power adjustment is made by thyristor switches and there is no mechanical switching action, it is called *static*.

An SVC can continuously supply reactive power to the bus to which it is connected. Whenever the load power varies, SVC responds quickly, and continues to operate with a new reactive power value.

TCR based SVC is the most common topology used in SVC type compensators. The main idea is to compensate the load with capacitors and make the total reactive power capacitive. The TCR is controlled to compensate the capacitive reactive power. TCR type SVC has a compensation capacity between the power of capacitors for capacitive reactive power and the reactive power difference between

reactors and capacitors for inductive reactive power. Figure 2.3 shows the compensation limits for a TCR based SVC.

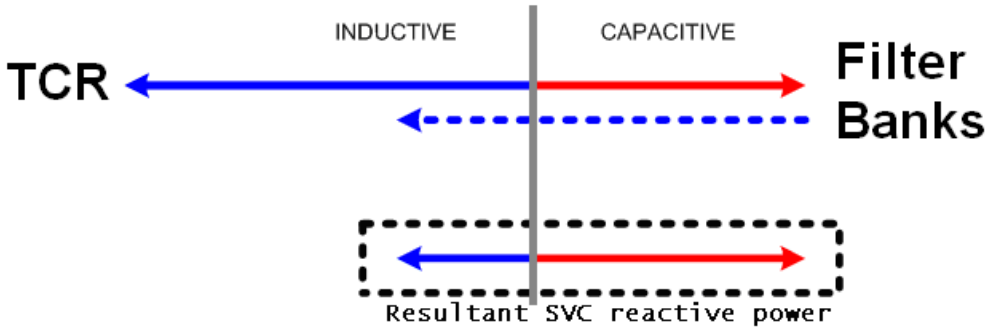


Figure 2.3. SVC compensation capability according to the capacitor and inductor reactive powers

Because of the resonance and inrush problem between the line impedance and capacitance, generally capacitors are not to be connected to the bus directly. Instead of direct connection, a small tuning or detuning reactor is used to eliminate the inrush currents of the capacitor, and by the resonance frequency between the reactor and capacitor, the load harmonic at this frequency can be eliminated. Two problems, inrush and harmonic filtering, are solved by reactor addition.

2.3 THYRISTOR CONTROLLED REACTOR

Thyristor controlled reactor (TCR) is a dynamic passive element whose admittance is controlled by a thyristor stack connected in anti-parallel form and it conducts on half cycles of the power supply voltage period. The circuit diagram of each phase of a TCR is shown in Figure 2.4.

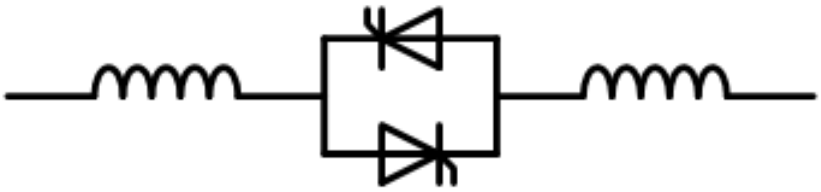


Figure 2.4. Thyristor Controlled Reactor

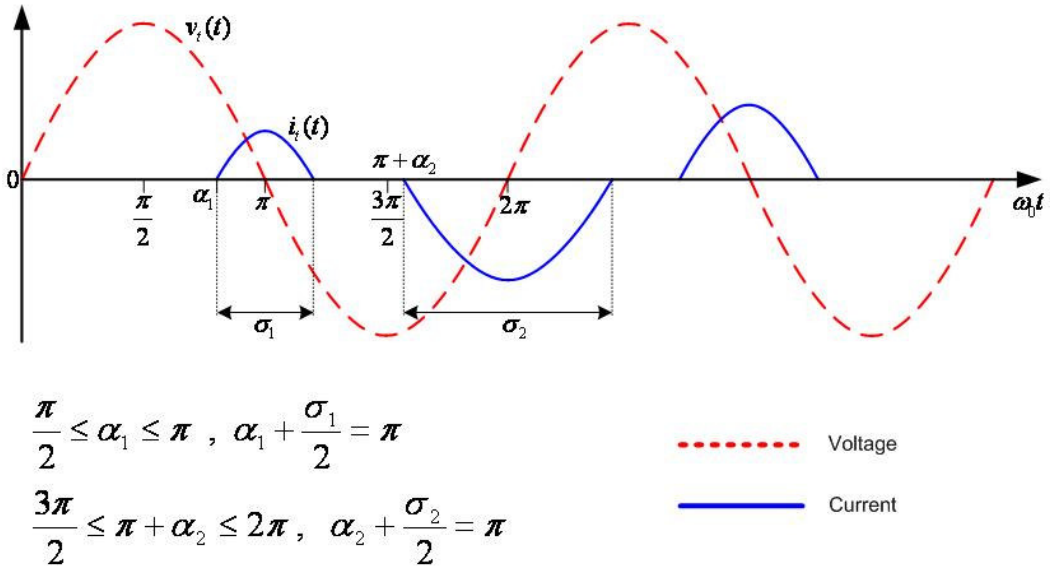


Figure 2.5. TCR voltage and current waveforms

The admittance of reactor depends on the triggering angle of the thyristors. Each thyristors is triggered into conduction in the second quadrant of its anode-cathode voltage signal (Figure 2.5).

The current on the reactor is controlled by changing the firing angle of the thyristors (α). The fundamental component of the TCR current depends on the firing angle which makes the impedance of the reactor controllable. The ability to control the impedance of the reactor makes TCR a controllable inductive load which is suitable for reactive power compensation.

The relation between firing angle and TCR current is acquired by solving the following equation 2.8 for the fundamental component which gives equation 2.10.

$$I_{TCR} = \begin{cases} \frac{\sqrt{2}V}{X_L}(\cos(\alpha) - \cos(\omega t)), & \alpha < \omega t < \alpha + \sigma \\ 0, & \alpha + \sigma < \omega t < \alpha + \pi \end{cases} \text{ A} \quad (2.8)$$

$$\sigma = \frac{\pi - \alpha}{2} \quad (2.9)$$

$$I_{TCR,n} = \frac{4}{\pi}\frac{V}{X_L}\left[\frac{\sin(n+1)\alpha}{2(n+1)} + \frac{\sin(n-1)\alpha}{2(n-1)} - \cos\alpha\frac{\sin(n\alpha)}{n}\right] \quad (2.10)$$

$n = 3,5,7,...$

$$I_{TCR,1} = \frac{\sigma - \sin(\sigma)}{\pi \times X_L} V_{rms} \text{ A}_{\text{rms}} \quad (2.11)$$

$$B_L(\sigma) = \frac{\sigma - \sin(\sigma)}{\pi} \times \frac{1}{X_L} \quad (2.12)$$

Since the current of TCR is non-sinusoidal, there occurs harmonics in the power system to which TCR is connected. The harmonic values are shown in Table 2.1.

Harmonic	Ratio to the fundamental (%)
1	100
3	(13,78)
5	5,05
7	2,59
9	(1,57)
11	1,05
13	0,75
15	(0,57)
17	0,44
19	0,35
21	(0,29)
23	0,24
25	0,20

Table 2.1 Maximum harmonic current ratios of TCR current

If the firing angle is same for positive and negative half-cycles of voltage signal then the current has odd symmetry and there is no harmonics with even index number. From Equation 2.10, the 3rd harmonic and the other harmonics with index number odd multiplies of 3 are in zero sequence and if TCR branches are connected in delta form, these harmonics do not flow through the power system and they circulate among TCR branches. When TCR branches are connected in Δ form, only harmonics with index number 6k±1 (k=1,2,3,…) will flow through the system (Figure 2.6, 2.7, 2.8).

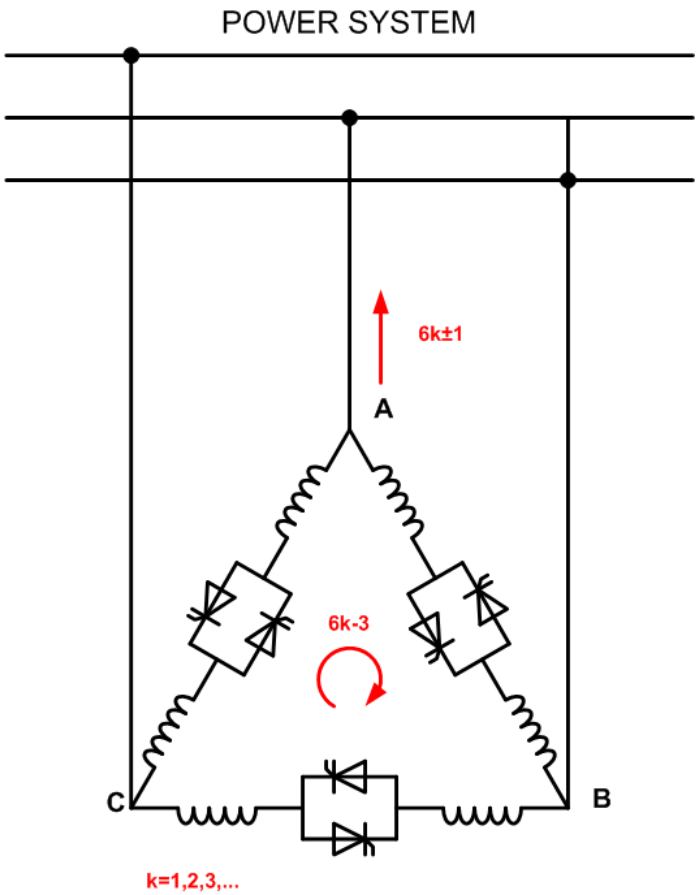


Figure 2.6. TCR harmonic currents flow

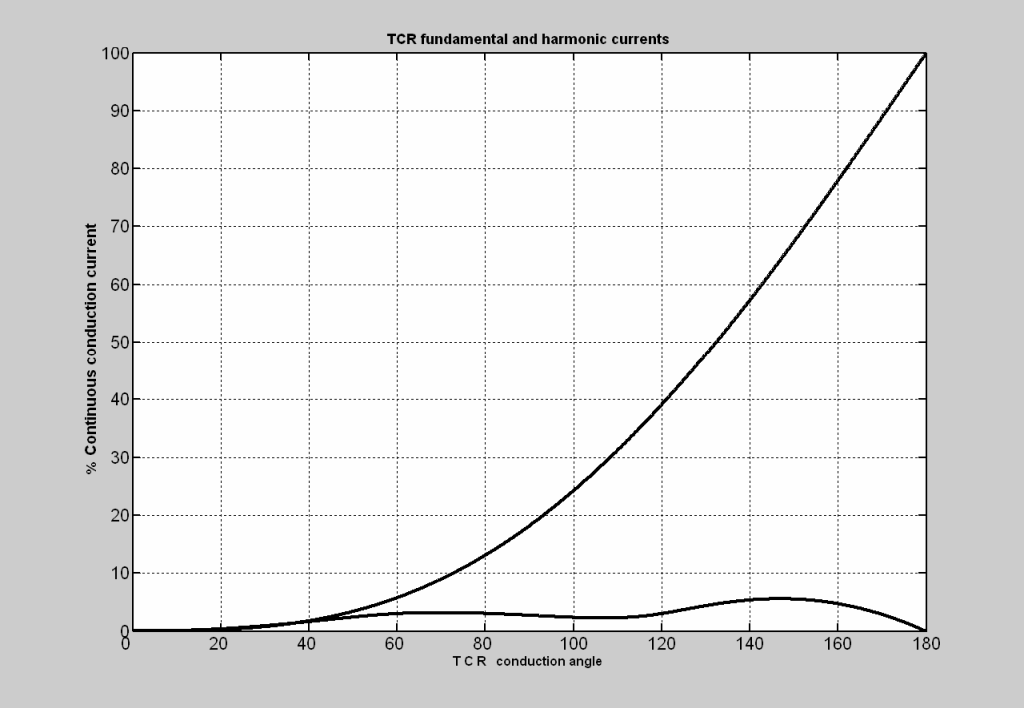


Figure 2.7. TCR current values according to conduction angle

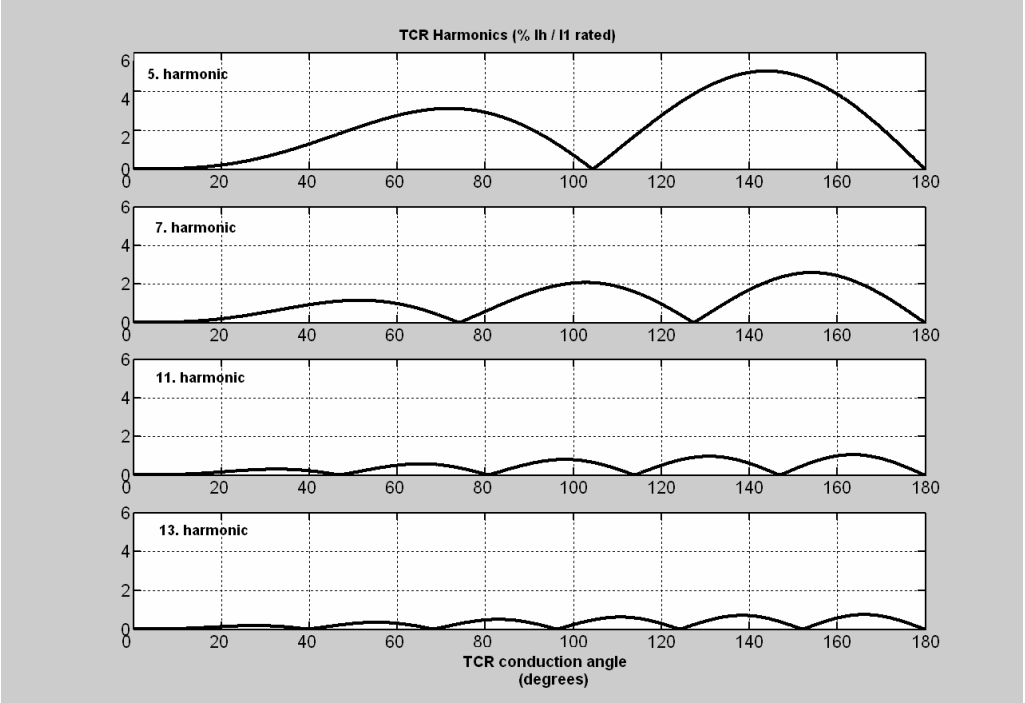


Figure 2.8. TCR harmonic current values according to conduction angle

2.4 LADLE FURNACE

The *steelmaking* is one of the process steps in steel production in which the impurities such as carbon and sulfur are removed from steel and some materials are added such as manganese, nickel, chromium to produce the steel with required characteristics. This operation is done via *ladle furnace* by adjusting the temperature of molten iron ore (Figure 2.9).

Temperature adjusting (heating) of the material is the main function of ladle furnace (LF). There is a power transformer that converts high voltage low- current electric power into low voltage high current electric arc in order to heat the molten steel in the LF.

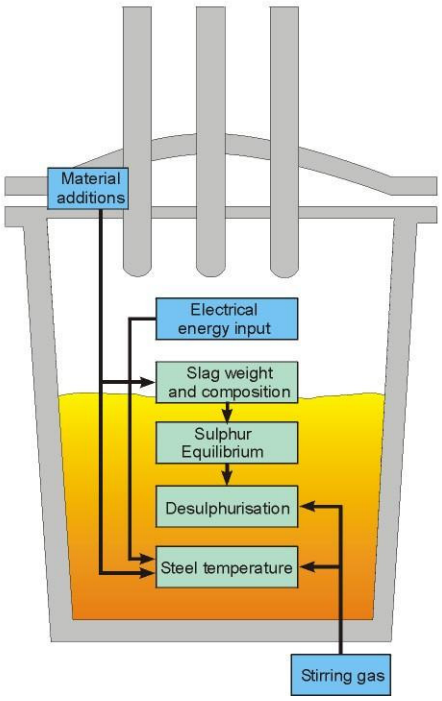


Figure 2.9. Ladle Furnace

The electrodes at the low voltage side of the LF are connected to the phases of the power system respectively. When the heating treatment process starts, the electrodes come close to the slag at the top of the molten material and an electric

arc occurs between the electrode pairs crossing through the slag surface. The current between the electrodes and the slag heats the molten material in the LF. By this way, the electric energy is transformed into thermal energy and the heat of the material is increased to the desired processing temperature (Figure 2.10, 2.11).

Since the ladle furnace generates electric arc and the arc has a nonlinear V-I characteristics (Figure 2.12, 2.13, 2.14) it generates inductive reactive power and harmonics at the power system. The power factor and harmonic content of power system exceed the standard permissible values. The reactive power and harmonic currents of the LF make it the second worst electric load after the arc furnace. In fact, ladle furnace electrical model is the same as the arc furnace electrical model at the refining stage of arc furnace operation.

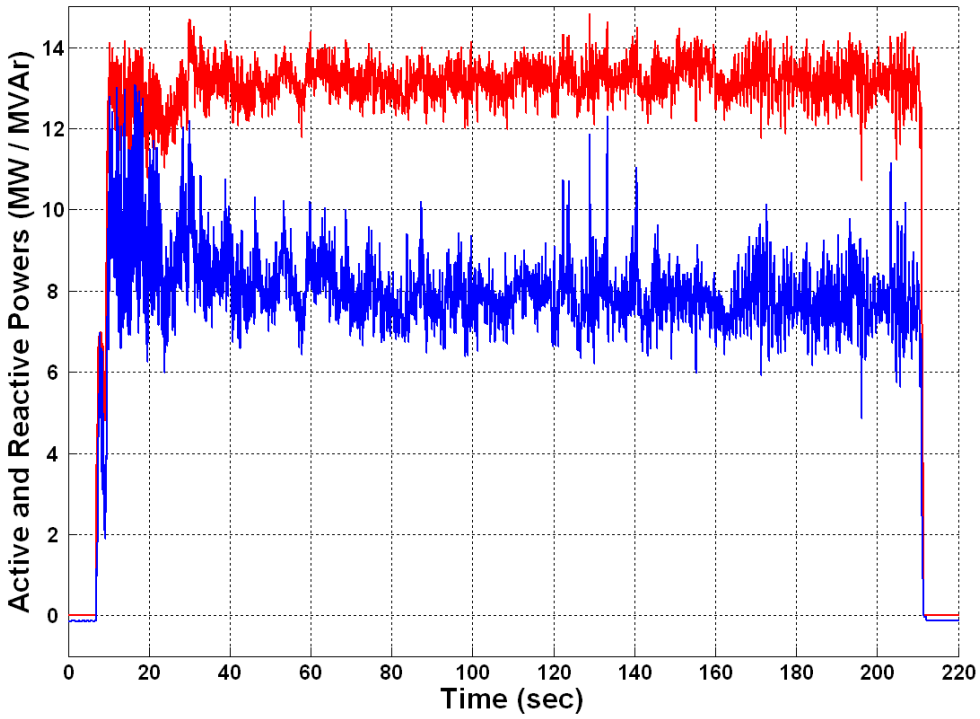


Figure 2.10. Active (red) and Reactive (blue) powers of ladle furnace for one heating process

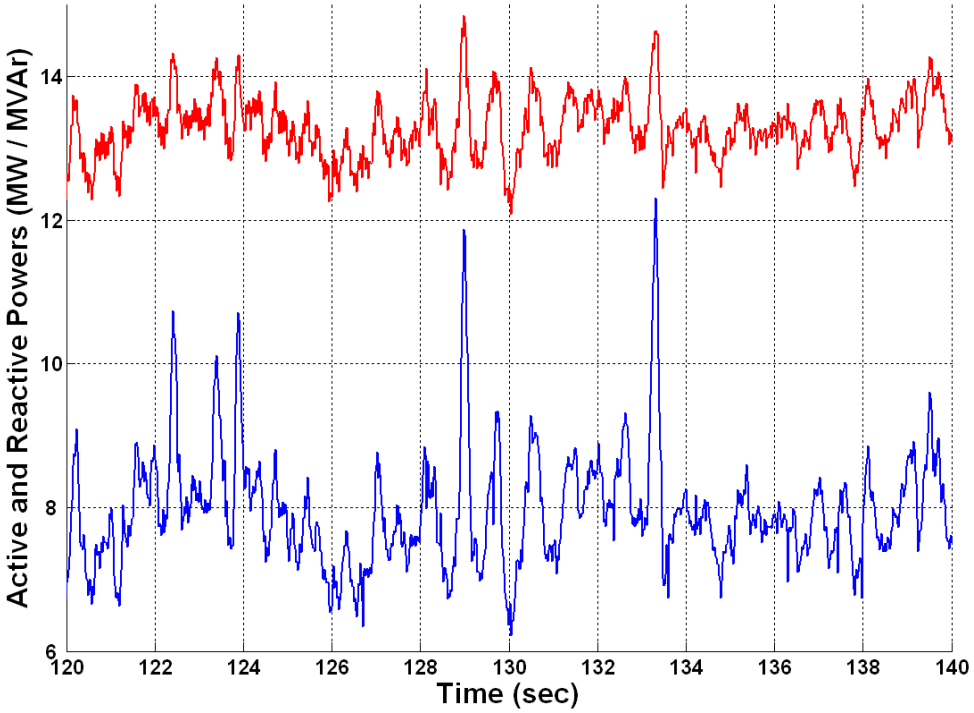


Figure 2.11. Active (red) and Reactive (blue) powers of ladle furnace for one heating process (zoomed)

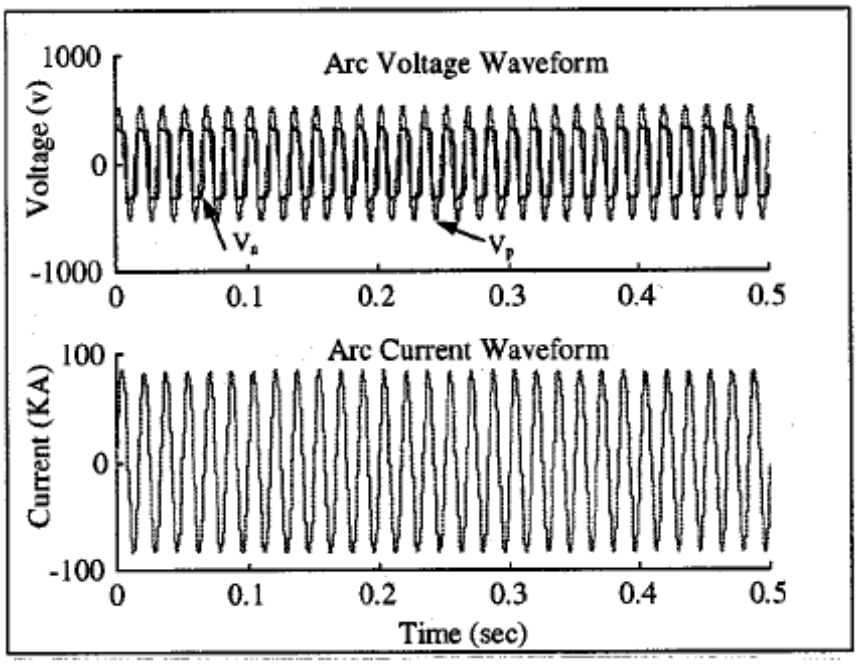


Figure 2.12. Voltage and current waveforms of an electric arc

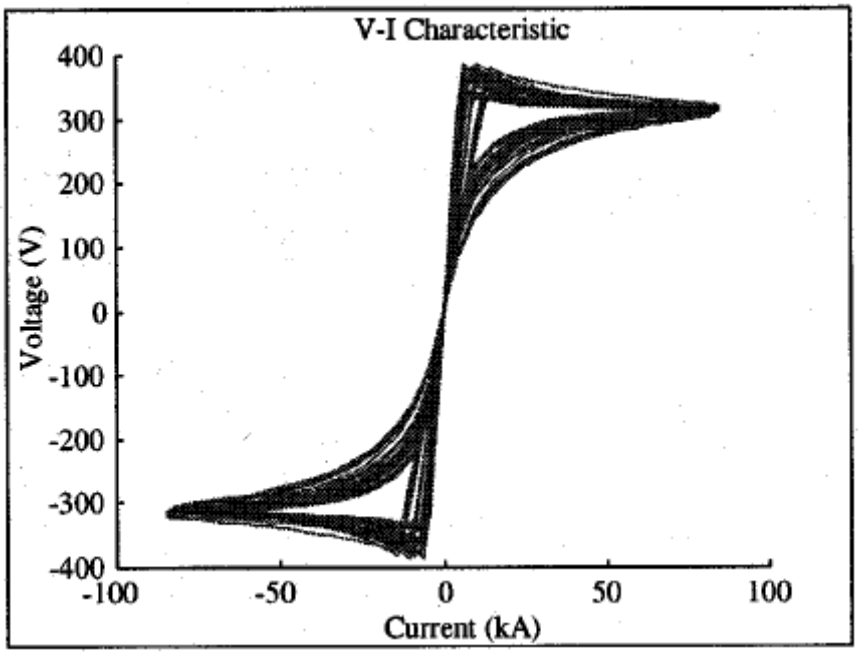


Figure 2.13. Nonlinear Voltage-Current characteristic of electric arc

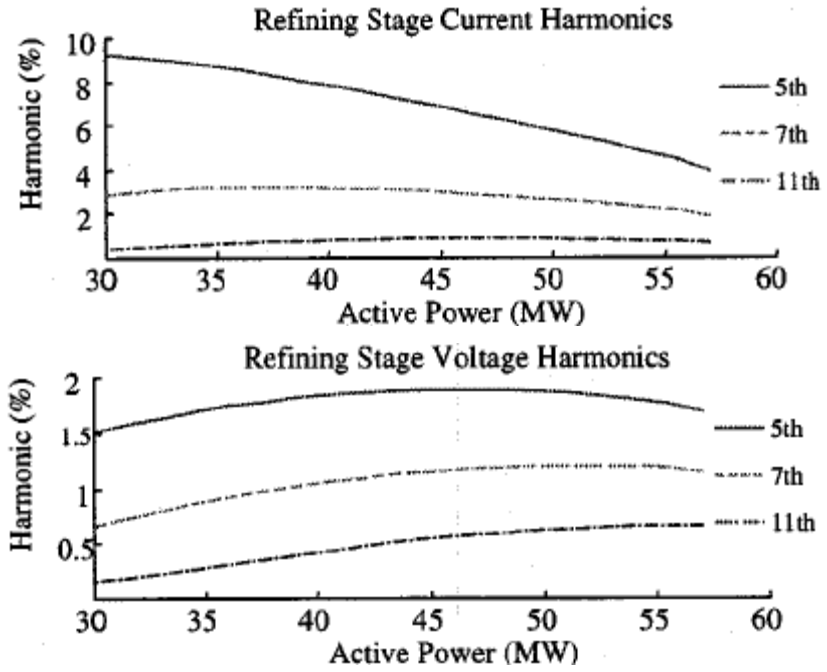


Figure 2.14. Harmonics of an electric arc furnace at refining stage

2.5 HARMONIC FILTERING

With the development of electric technologies, modern power systems require power quality more than before. The efficiency of transmission and distribution systems is proportional to the power quality of the loads connected to the system. When the power quality increases, the infrastructure capacity can be used more efficiently that makes the investment costs lower. The economic point of view and customer satisfaction are the main reasons imposing power quality.

In a DC system, the system has only two parameters as bus voltage and line resistance; however, an AC system has bus voltage, frequency, voltage harmonic content and line impedance as power source. The effect of a load to an AC system is more complex than a DC system. When an electrical load is linear -that can be modeled by resistor, capacitor, inductor or dependent sources- then the load current is proportional to bus voltage in magnitude and phase. For a pure sine voltage signal, a linear load draws pure sine current at the same frequency. On the other hand, for a nonlinear load, the drawn current has harmonics which cause voltage harmonics at the bus voltage. Another load or customer connected to the same bus with the nonlinear load is affected by the harmonics in a bad manner.

In a power system, harmonics bring about overheating of electric devices (motors, transformers, etc.), resonance problems between the inductive and the capacitive parts (i.e. transmission line and shunt capacitors) and malfunctioning of the electronic devices which are designed and manufactured to be supplied at voltage with fundamental frequency and high currents in neutral conductors. A simple solution for these problems is to increase the electrical ratings of the devices and more lasting devices due to disturbances.

However, this solution is not economical from engineering perspective. More material, more cost and bulky designs are not appropriate when the optimum solution is considered. Instead of protection against harmonics at the load side, eliminating the harmonics is more feasible and reasonable.

There are two types of harmonic filtering methods. The first one is connecting a passive filter that has a high impedance at fundamental frequency and low impedance at the harmonic frequency that is chosen to be eliminated. The second way is to use a DC/AC converter topology connected to the power system that inserts inverse of the harmonic current to eliminate.

In a TCR type SVC, passive filters are commonly used. An LC resonant circuit (Figuree 2.15) tuned to any harmonic frequency supplies capacitive reactive power at fundamental frequency and filters out the harmonic current that it is tuned. Adding a reactor in series with the capacitor makes it a harmonic filter and reduces the transient current component at the switching instant.

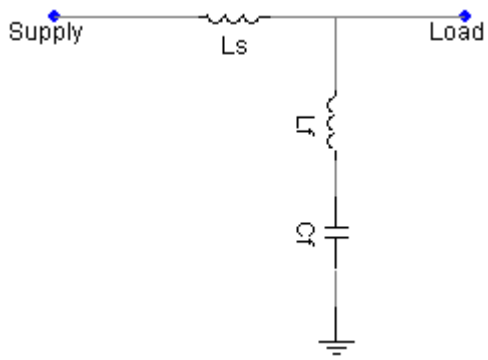


Figure 2.15. Passive filter connection to a power system

For a passive filter connected to a power system, the impedance from the supply side is a capacitance at the fundamental frequency and if the supply side has no voltage harmonics, there are no current harmonics from the supply side through the load side. From the load side, the impedance of the bus is $L_s||(L_f+C_f)$ which results in theoretically zero Ohm impedance at L_f and C_f resonance frequency. So, when the load generates harmonic near this resonance frequency, then this harmonic component will flow through the filter instead of the line.

Even if passive filters can be a better solution for harmonic elimination, there are resonance problems for harmonic currents. When the circuit topology is

investigated for the load side, it is easy to see that there is a parallel resonance circuit in $L_s||(L_f+C_f)$ form which has a resonance frequency at $(L_f+L_s||C_f)$. This parallel resonance circuit acts like an open circuit. If there is a current harmonic near this frequency, the voltage harmonic on the filter with this frequency will be amplified and more than the load harmonic current would flow both through the system and the filter.

To eliminate this resonance problem, a resistance can be used at the filter side to make the impedance at parallel resonance frequency a real value instead of infinity. The damping resistor (Figure 2.16) eliminates the resonant problem, protects the filter capacitors against overvoltage and the new topology, and also filters other harmonics at higher frequencies to some extent.

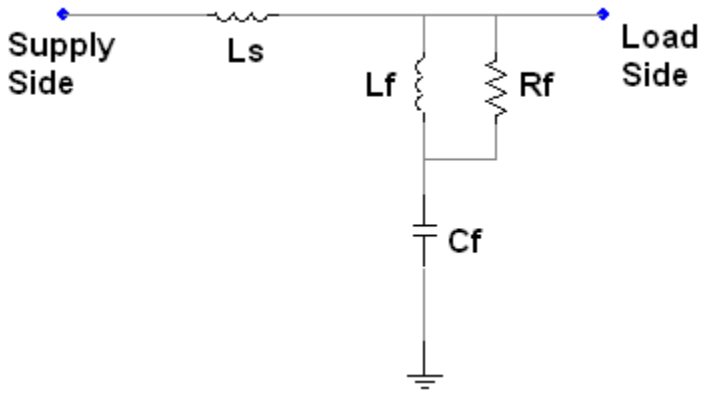
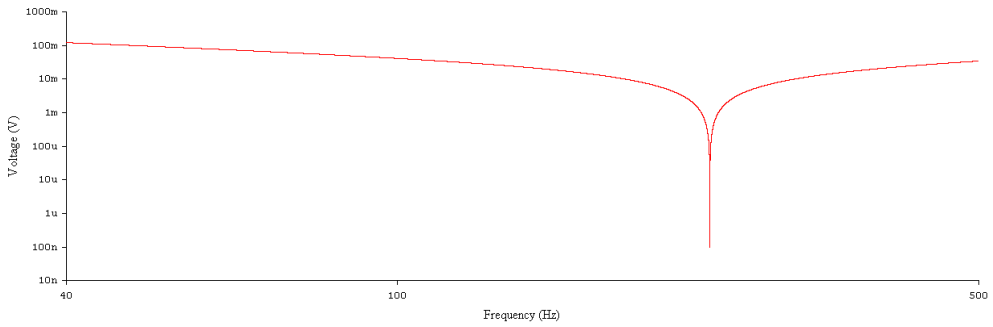
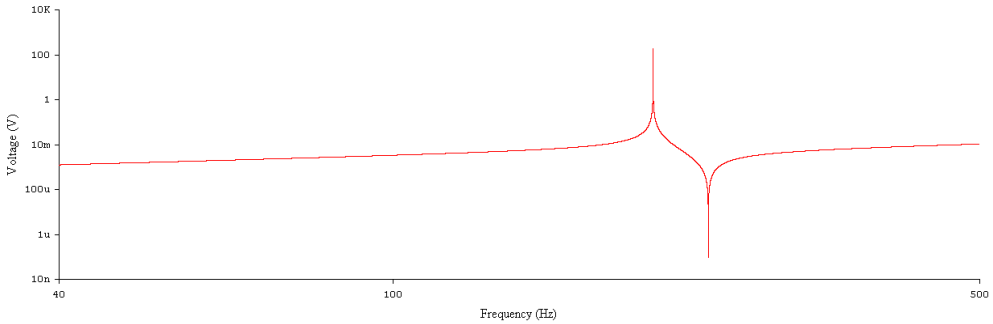


Figure 2.16. Damped passive filter connection to a power system

For a 100 kVAr 5th harmonic filter at 1 kV bus with 5 uH line impedance, when the tuned frequency is 95% of the harmonic frequency, then the frequency-impedance characteristic of the filter and the impedance seen from the load side are as shown in Figure 2.17.



(a)



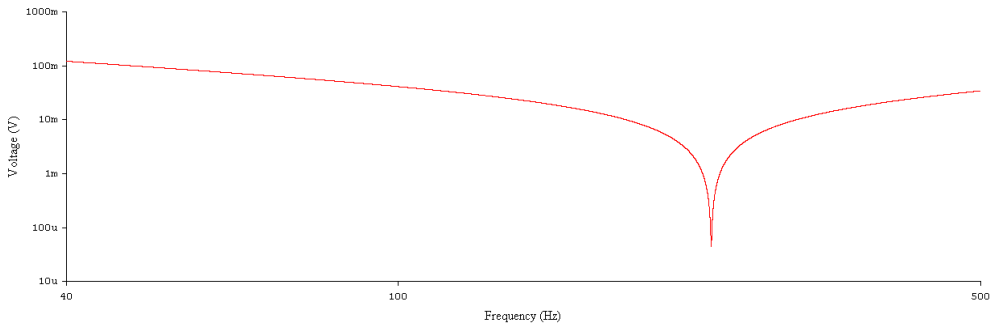
(b)

Figure 2.17. Frequency-impedance characteristics of filter

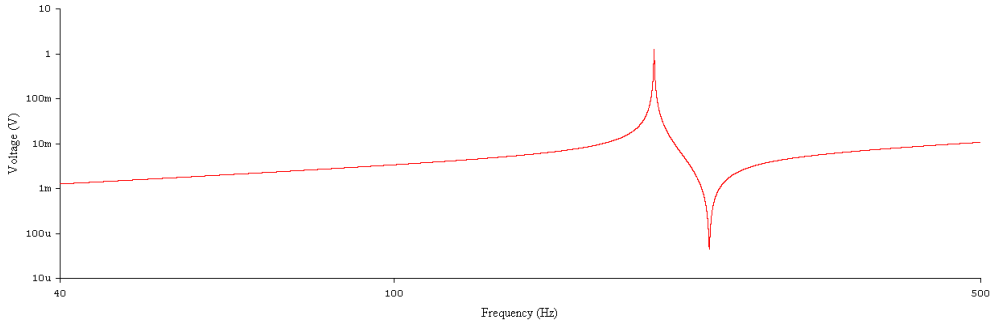
(a) LC branch impedance (b) Impedance seen from the load side

When the impedance graphs are investigated, the filter has zero impedance near 238 Hz, and from the load side, the supply impedance is infinity near 204 Hz. If the load has any 4th harmonic, then this harmonic will be amplified. Because of this problem, 4th harmonic of the load may exceed the limit value specified in the associated standard.

When a resistor is connected in parallel with the filter reactor, then the filter impedance and supply impedance change. The resultant impedances are not zero and infinity. The resultant frequency- impedance characteristics are shown in Figure 2.18.



(a)



(b)

Figure 2.18. Frequency-impedance characteristics of the damped filter
(a) LC branch impedance (b) Impedance seen from the load side

The new impedance characteristics show that the resistor makes the frequency response of the filter smoother and the resonance problems are solved. Furthermore, the higher frequency harmonics are filtered with the new topology. The resistance value is calculated due to the optimization of filtering characteristic and active loss cost of the filter.

Another solution for parallel resonance problem for passive filters is to add another passive filter tuned to the previous harmonic frequency. If the load does not have dominant harmonic at this frequency, the second passive filter filters out the amplified harmonic and prevents it from penetrating into the through the power system.

Light flicker stands for the fluctuations at the fundamental component of the power system voltage between 8-100 Hz where the human eye is disturbed. The main reason of flicker is powerful loads changing rapidly. When the reactive

power of the load changes rapidly in large amounts, then the voltage drop on the transmission line becomes considerable. As a result of this voltage drop, the voltage value at the load bus decreases. If the reactive power of the load fluctuates, then the bus voltage fluctuates. The main reason of flicker is rapidly changing loads such as arc furnaces, ladle furnaces, welding machines, etc.

However, when there is a passive filter at the SVC stage, the harmonic component of fluctuating load current at the flicker frequency may be amplified because of the parallel resonance. For instance, when a 2nd harmonic filter is used, the parallel resonance frequency of the filter and line impedance may occur at 90 Hz neighborhood. A dirty load -like arc furnace or ladle furnace- generates interharmonic at this frequency neighborhood, the harmonic problem becomes more complicated. The second harmonic filter which is designed to filter the harmonics at 100 Hz neighborhood amplifies the interharmonics near this neighborhood. To avoid this problem, the harmonic filter is used in damped form which means that the damping resistor of the filter is small enough to filter a large frequency band but when the resistor gets smaller, filtering capability at the tuned frequency is reduced. The effect of damping resistor to filtering characteristic of a C-type second harmonic filter is shown in figure 2.19 and 2.20.

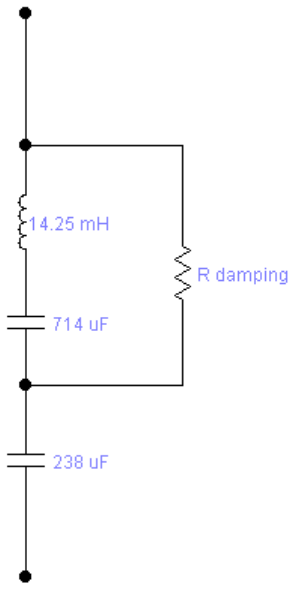


Figure 2.19. One phase of 13.8 kV/14.2 MVAr C-type 2nd Harmonic Filter

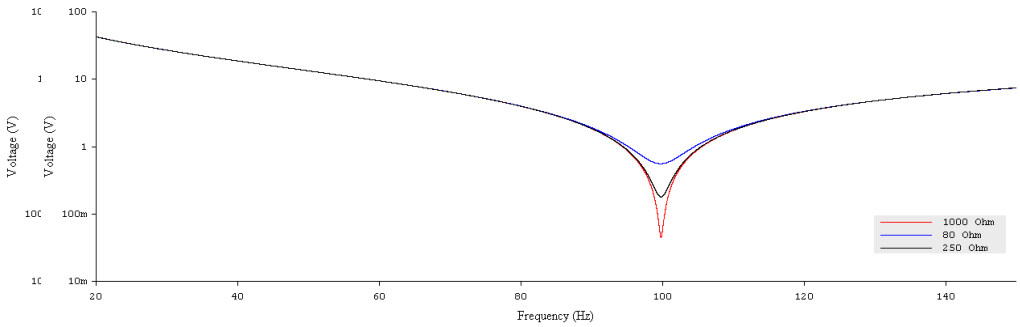


Figure 2.20. Filter characteristic of the C-type filter

2.6 SVC DESIGN PROCEDURE

An SVC system is designed and constructed in 5 steps. These parts are power stage design, controller design, simulation, optimization and construction. The main idea of the procedure is to find the optimum point between power capacity + controller performance and financial cost + installation cost of system. For an SVC system, the producer and the customer negotiate and agree upon capacity, cost, and installation and operation type. After the agreement the producer should find the optimum design to have positive profit and the desired operation performance.

The power capacity of the SVC is defined by the field measurements of the load aimed to be compensated. Before the measurements, the load characteristic is defined by the help of customer. The power characteristic, operation duty cycle, load changes, etc. are to be defined and measurement technique and its duration are to be defined. At this stage, the previous information available in literature and guidance of the customer are very important to obtain the exact load characteristics.

After characterization of load, the measurement technique (full-cycle, 1 second average, 3 second average, energy meter, …) and measurement time period (hour, day, week, …) are defined. If the load cannot be characterized, then the most accurate measurement technique and the longest measurement time should be chosen. Since the power stage units are custom designed for the load, voltage and

environment parameters, and then the design error at this stage should be minimum for safe operation of SVC.

After the measurements, power quality parameters of the load such as active and reactive powers, power factor, harmonics, unbalance and flicker are to be calculated. The next step is the decision of load balancing. Since SVC can balance the unbalanced active power of load, the power capacity of SVC can be chosen for both reactive power compensation and load balancing.

If the load balancing option is chosen then the design of SVC power capacity should be done for compensator's delta branch impedances. By the help of Steinmetz equations the maximum inductive and capacitive powers for delta branches of SVC are calculated. Only if the reactive power compensation option is selected, then the capacitive and inductive power capacity of SVC can be chosen by using the maximum reactive power of the load as reference.

After capacity calculation, the structure of SVC is defined. By the help of load's power characteristic the SVC elements are chosen for compensation. All or some of TCR, FF, FC, TSC and TSR can be selected as SVC components to have the minimum cost and adequate performance. After structure design, the basic simulation of the system is done. At this stage, the correctness of capacity and structure design is controlled. For example, by the load's power characteristic the designer selects TSC as a component and load balancing option for operation type. At the basic simulation step, if he founds that the compensator cannot balance the active load when TSC is out of operation; as mentioned before, at this stage the design should be carried out with high attention to have zero error since modifying the power stage is very expensive after installation.

After basic simulation; if the results are not adequate for performance, then the error should be defined. If the error comes from capacity or structure stage, then the component parameters are modified due to the error. The other error source is simulation error that can be corrected by editing the simulation parameters. The flowchart of power stage design is shown in Figure 2.21.

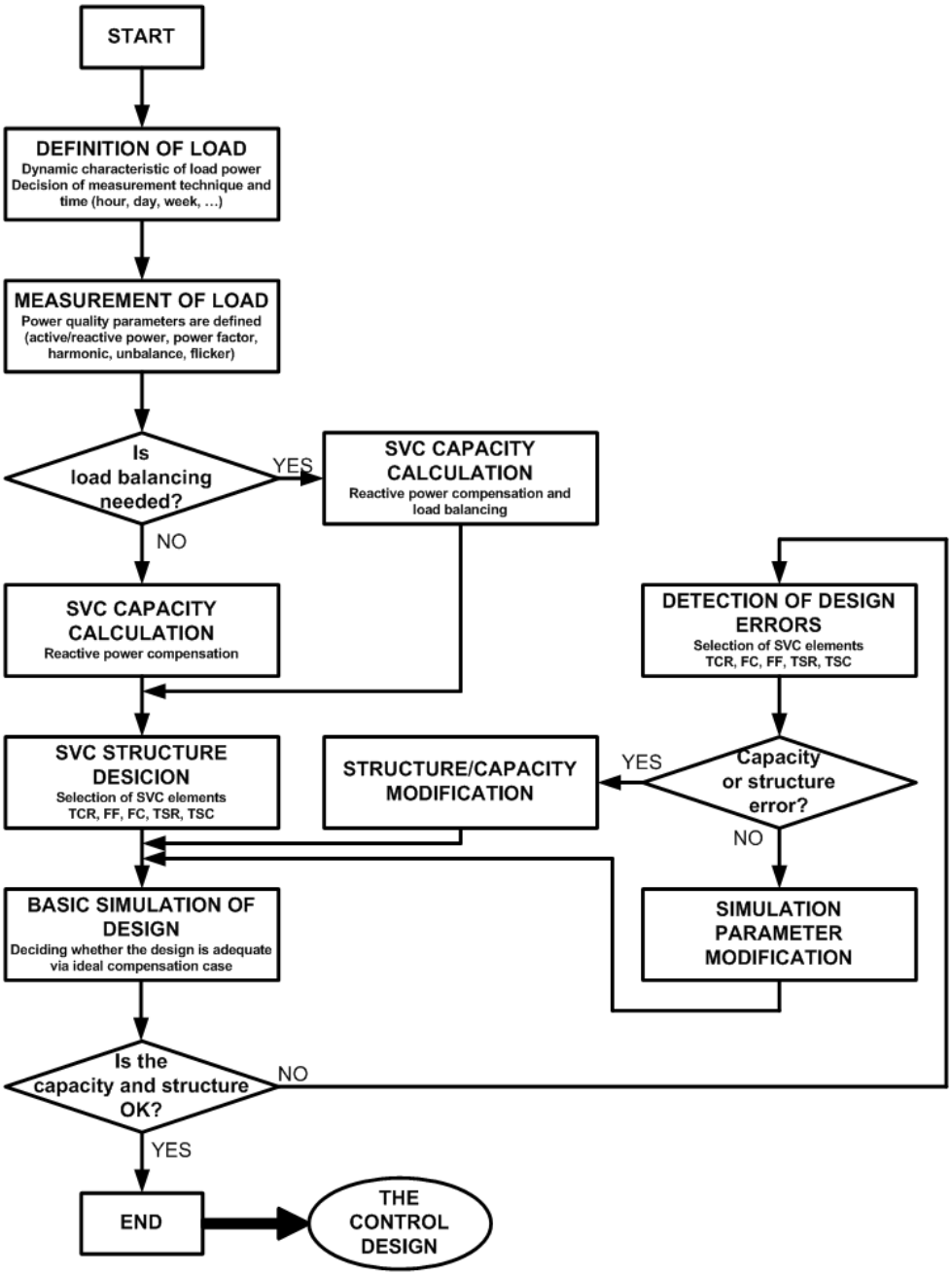


Figure 2.21. Power Stage design

Power stage design is followed by the controller design of the SVC. The reference data for the controller are measurement data, performance goals, predefined controller budget, signal measurement techniques (voltage/current transformers, capacitive divider, lems, etc.), human machine interface (HMI), system monitoring.

Controller design procedure starts with control technique (PI, PID, feedforward) selection step. The dynamic characteristic of load power and performance goal is the main guides for control technique selection. If the rate of change of load's power is high and the reactive power error limits are small, then the response time of the controller must be small enough to meet the desired performance. The control technique can be selected by the guidance of literature and experience of previous applications.

For an electronic controller, the most important decision is choosing the implementation platform of the controller. If the control technique requires fast and complex calculations and controller budget is large enough, then digital platforms should be chosen. In opposition, if the control technique is simple (basic PID controller) and controller budget is limited, and then analog platform should be chosen. For selection of analog or digital controller, the following criteria are the guide for the designer. The advantages and disadvantages of digital implementation are listed in Table 2.2 and 2.3. When it is considered that analog electronics is the native solution, the following rules make the designer switch to digital electronics or not. The design procedure for the control is shown in Figure 2.22.

Advantages of Digital Control
• System upgrade in the field is easier than that of solution. • Arithmetic calculations are more flexible and accurate. • The data processing is noise free. Once the data is transferred into digital platform (0s and 1s), the data have noise immunity. • Suitable for modular design and implementation. • Digital devices have more reliability. MTBF parameter is very large for digital than it that of the case. • Communications between other elements and data logging is easier. • Changing the structure controller does not require an alternation in the hardware. • Digital systems provide improved sensitivity to parameter variations.

Table 2.2. Advantages of Digital Controller

Disadvantages of Digital Control
• Limited cycles due to the finite wordlength of the digital processor or ADCs and DACs. • Platform has limited capability. After reaching the maximum capacity, another digital device is required for expansion. • Production costs are higher for digital systems. There is a trade off between cost and performance and this should be taken into account at hardware decision stage before system design. • Reduced signal resolution due to the finite wordlength of the digital processor.

Table 2.3. Disadvantages of Digital Control

For analog controller, the first step is designing the flow chart of control and analog circuit design of the flow chart components. These steps can be done by designing an analog mainboard as base for the controller and analog PCBs for control elements (power measurement, triggering, etc.). In an ideal system, accuracy of analog circuits is 100%, but when the parameter characteristic of

components for temperature changes is considered with an analog circuitry, calculation errors can be much higher than it is expected. This handicap should be taken into account and analog controller type should be chosen with considering the operation area of the SVC. If there is harsh environment, the PCBs should be well protected by coolers, heaters, air filters, which means more maintenance and small *mean time between failures* (MTBF) and more malfunctioning.

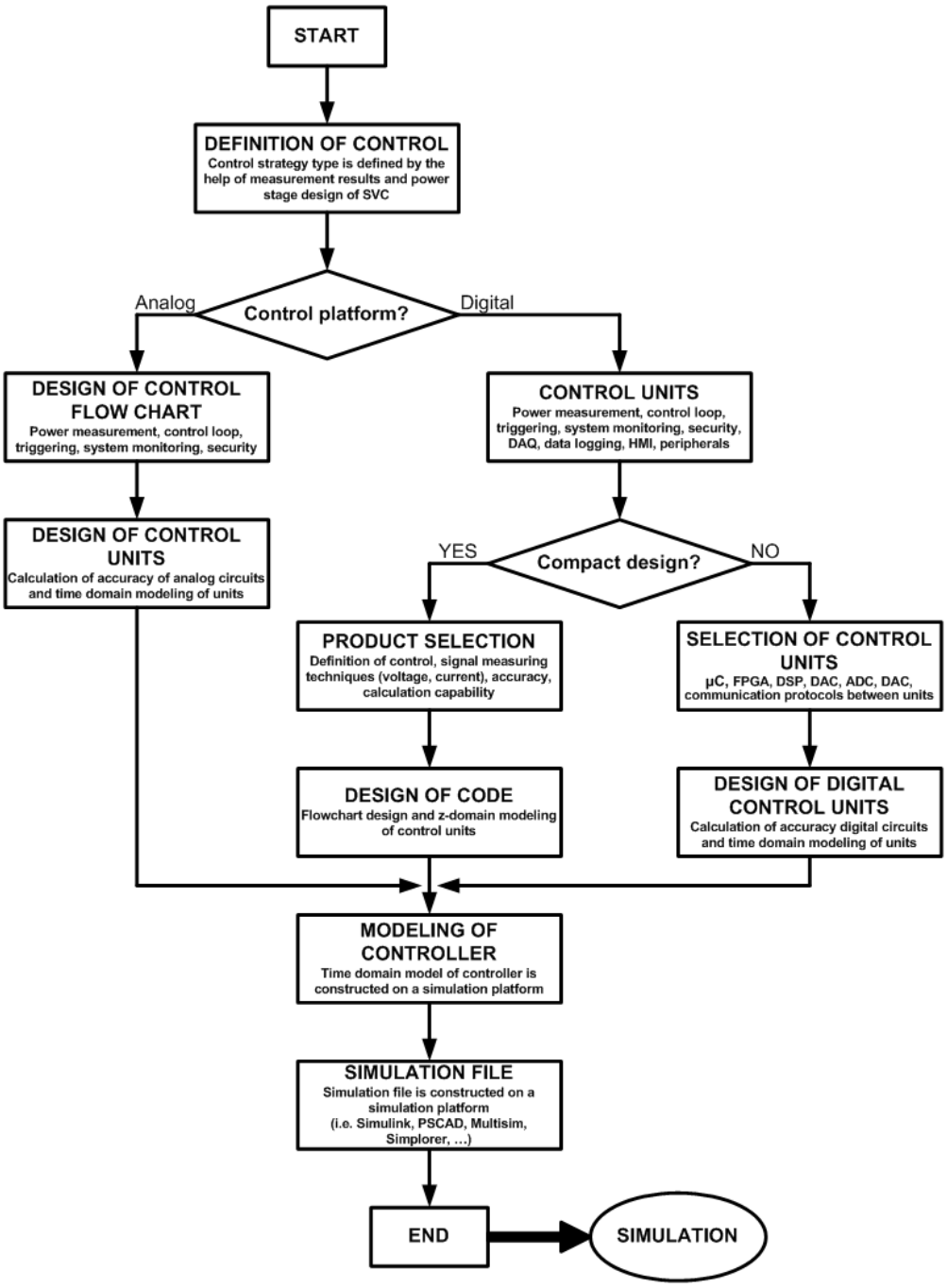


Figure 2.22. Controller design

When digital control is selected, the first step is choosing the digital platform for the controller. In digital electronics world, an electronic system can be designed and built by implementing each flowchart element by ICs and additionally a compact platform can be used with integrated embedded control, ICs, sensors, peripherals. The advantage of compact platforms is reducing the design and implementation job to software level that the designer only works on software. For discrete design with ICs, each part should be designed separately and the communications between parts should also be implemented. In opposition, with discrete designs each variable transmitted between parts can be monitored and custom designs can be done. For a compact platform, all of the operations take place inside the box and there is no possibility to intervene in the system for modification. The design engineer is restricted by the abilities of the product and if there is an upgrade need in the future a new or additional platform will be needed.

Using a compact platform makes the job easier but the ability of the system is restricted and expansion is stepwise. When there is a need for extra control job in discrete analog/digital design, adding a new PCB solves the problem. For compact platform case; if the used capacity is near 100%, new additions require an additional platform or a new platform with more capability.

After selecting the controller type, the preparation of simulation stage starts. The designed controller's units are mathematically modeled for simulations. The simulation platform is selected due to the accuracy required. If it is needed, a powerful simulation platform (high speed CPU, large RAM, etc.) is built. Then the simulation file is constructed on the simulation platform.

For the controller design stage, the important rule is that the designer can modify the controller and control strategy whenever he wants before controller implementation. Once the implementation gets started, then any modification means extra time, cost and effort. The critical point is the decision of the structure of the controller. If the deadline of the SVC construction limits research and development studies a basic and previously implemented control technique and controller platform are more suitable to reduce the risks. If the practice is a

research and development job, a powerful compact controller platform makes the job easier by eliminating the electronics studies such as PCB design, implementation, and noise immunity.

After the controller design stage, the system is fully designed for simulation stage. The simulation file is run on the simulation platform selected in the previous stage. The first step is selecting the *simulation time step* for the accuracy of the results. The simulation time step should be small enough for measuring and calculation accuracy for analog case and it should be smaller than the operation time step of the controller for digital case.

The next step for simulation stage is testing the constructed blocks of simulation file. The SVC units and control units are tested basically to guarantee right operation of simulation. Currents, voltages, active/reactive powers, delay times of SVC units are tested for ideal cases. The response times, measurement and calculation accuracy, right operation, correctness of algorithms of control units are controlled by using constant values and basic signals like sine, square, triangle, sawtooth waves. Running the simulation to take constant power from TCR connected to an ideal source can be an example for this step. Morover, the simulation time step value is verified for accurate operation of simulations at this step.

If the simulation of units is completed successfully, then the whole system simulation of the complete system takes place. In the simulation stage the designer builds the controller structure. The design procedure is shown in Figure 2.23.

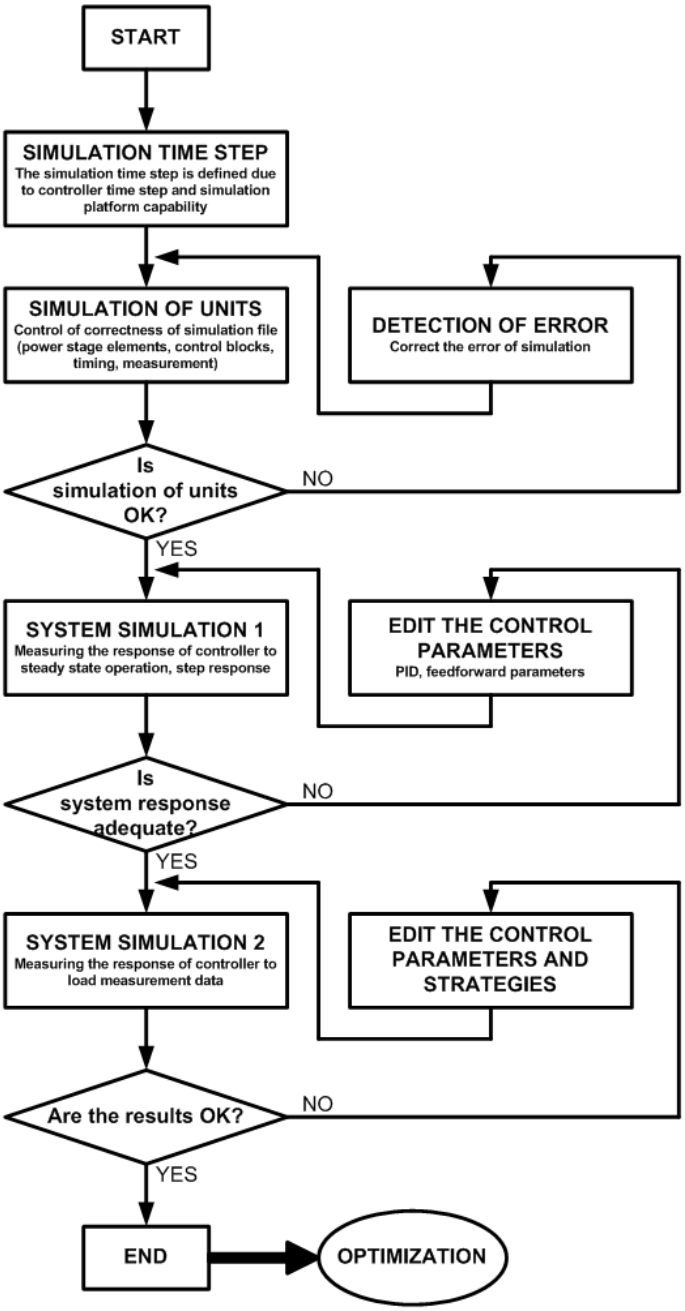


Figure 2.23. Simulation

In the first step of system simulation, the control parameters are defined. These parameters can be found by trial and error method or by solving the system transfer function. The method depends on the accuracy goal of the system.

If the desired system response is found, then the second system simulation takes place. At this step the measured data are integrated to the simulation to obtain the

response of the design to the load to be compensated. At this step the important point is modeling the load by using the measured data. When the field data is simulated with the designed SVC in parallel the resultant voltage drop, harmonic content and loading of transmission and distribution elements will be improved. The effect of these improvements to the load should also be modeled in the simulations to have more accurate results. Instead of the conventional modeling techniques like component based modeling, more accurate techniques like adaptive back-propagation, improved composite load modeling may be used [15].

At the second system simulation step the response of the system is optimized to have the minimum errors as a result. The optimization is done by changing the control parameters and control strategy. If the results show that the control strategy should be improved and if the controller design is not capable for this improvement, the controller should be changed in the next step of design. Furthermore, the basic simulation step results in the phase of power stage design are verified at the second simulation step.

The following stage is the optimization of the system design (Figure 2.24). Up to this stage, the system is designed for full compensation in ideal by selecting the capacity and performance for the worst case of load and zero error in ideal. When the result is considered in engineering philosophy, the goal should not be the case nearest to ideal. Optimum solution is to have the best solution with the lowest price. In optimization stage the system's parameters are modified due to the system error result of simulation stage. If the results are not within the error limits, then the designer has two choices. The first one is modifying the power capacity of the system by increasing the capacity by the redundant error value. This option is the expensive one but gives the designer the chance to be more flexible while choosing new parameters and structure for the power stage in the next design loop iteration. The second option is modifying the controller of the system. From the simulation results, if it is seen that a better control technique (adding a second control loop or adaptive control) decreases the error under the limit values, then the designer can select this step. Besides selecting one of the modification options, both of them can be selected for optimization iteration. At this step, the choice and

modification strategy can be selected by the guidance of literature and previous experience.

When the prices of increasing the capacities of power stage and controller are compared, modifying the controller at this step is more reasonable. By this way, the designer may found an optimum point with smaller price.

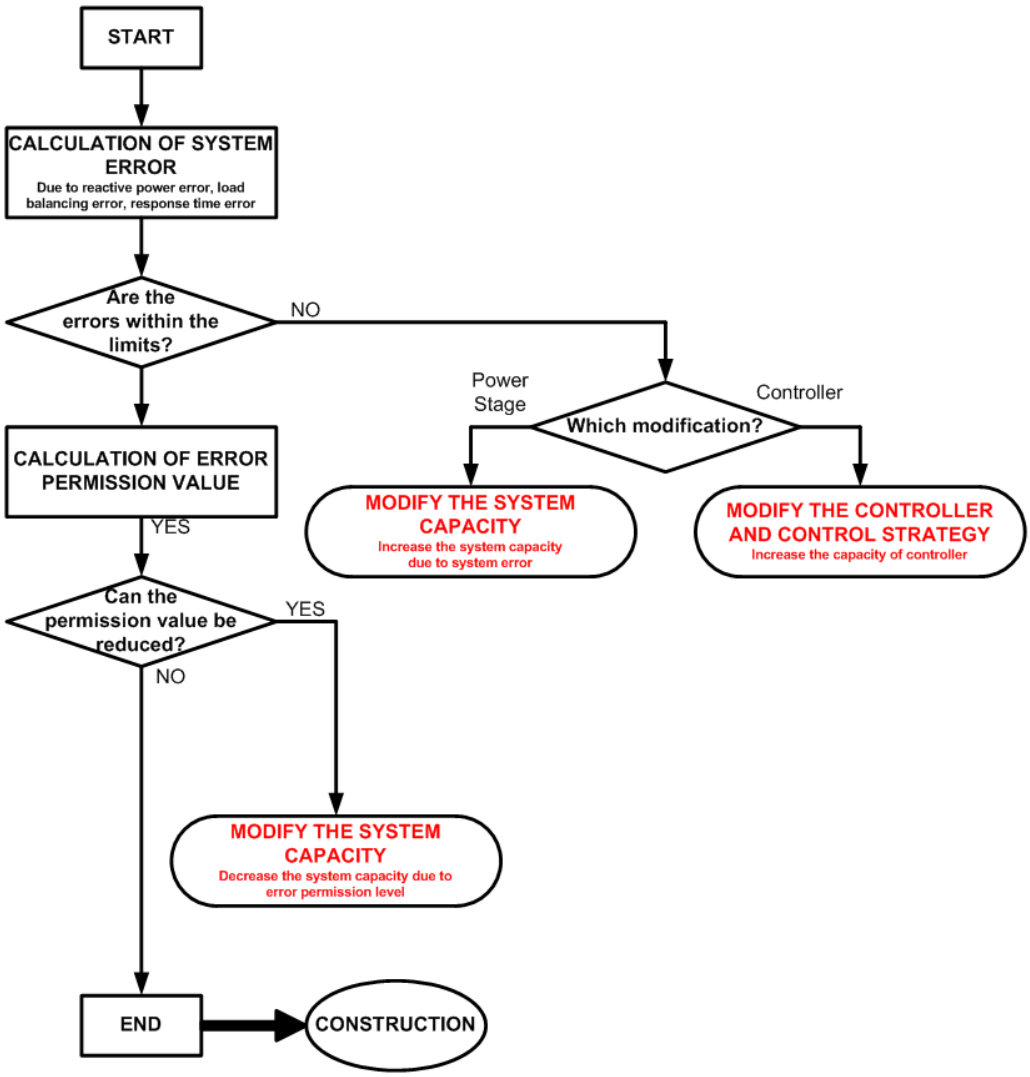


Figure 2.24. Optimization

If the resultant error values are within the limits, then the next step is calculating the *error permission value* of the design. *Error permission value* is the difference

between the predefined error limits and the resultant error values. If the ratio of error permission value is comparable to ratio of error level, then the design is modified to decrease the error permission value. To do this decrement, the system capacity is reduced. When the price of power stage capacity cost is compared with the controller cost, reducing the expensive one, power capacity, is more reasonable. In the next optimization stage of iteration loop, the designer could decrease the controller capacity to reduce the cost of the system. The key point of this modification is reducing only one type of parameter. When the both capacity of power stage and controller capacity are reduced; then in the next iteration loop the result may diverge such that the simulation results are above the limits. This step is a controlled experiment and the optimization is done for power stage only.

If the error permission value is near 0, then the design procedure finishes and implementation and construction stages start. The optimization of the design is based on optimizing the power stage firstly and the controller secondly. The reason of designing the controller parallel with the power stage instead of sequential independent design procedures is to start with an closer point to the optimum case. When the design procedure finishes, the designer may optimize the controller again to reduce the controller's budget content in the project.

After the design procedure, the construction procedure takes place (Figure 2.25). The components of the SVC system are ordered, the time plan for the project is defined and the implementation and construction of the system is started. After the installation of the system, the SVC is tested in the field. The tests consists isolation tests of power stage components, operation tests of components (controller, voltage/current transformers, thyristors, etc.) and control parameter tests for no load, full load, step responses of the system. The test procedure is defined by the conditions and characteristics of the components and depends on the system design.

The next step is occupied by the performance tests, which means running the SVC system with load connected. If the results of the performance tests are within the

limits as planned in the design steps, then the job is done and the designer deserves a greeting.

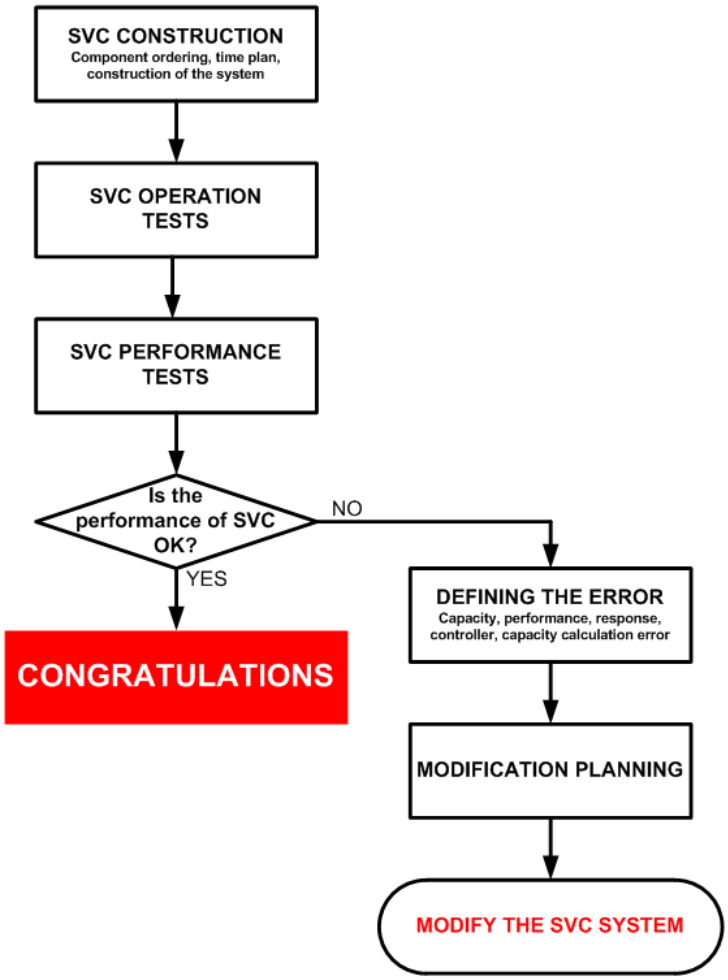


Figure 2.25. Construction

If the performance tests' results do not meet the planned values, then the source of the error is defined. A modification plan is done and the required changes are applied to the system and the test procedure is run again.

CHAPTER 3

STRUCTURE OF PROTOTYPE SVC SYSTEM

3.1 POWER SYSTEM

The power system to which the SVC is connected is the secondary side of 154/13.8 kV power transformer that supplies power to the two ladle furnaces of ERDEMİR Iron & Steel Factories Co. The transformer is wye connected at the primary side and delta connected at the secondary side; it is located at the TEİAŞ switchyard within the factory campus. Power is delivered to the factory by a 154 kV overhead line with a SCMVA 4500 MVA (Figure 3.1). The earth connection is maintained via a grounding transformer. There is no ground connection other than this one which means no zero sequence at the 13.8 kV bus.

The SVC system is connected to the secondary of the transformer and the ladle furnaces are connected through power cables with a length about 1 km. The ladle furnaces have step-down transformers with 13.8/0.4 kV voltage ratio shown in Figure 3.1. These step-down transformers are energized by circuit breakers at each heating process and this operation causes high inrush currents with a markedly 2^{nd} harmonic current content.

The power stage of the SVC has 3 reactor pairs with 16 MVAr connected in delta form and a C-type 2^{nd} harmonic filter with 14.2 MVAr connected in wye connection without grounding (Figure 3.2 and 3.3). Three thyristor stacks with 9

thyristors in series are connected between the reactors for control of reactive power (Figure 3.3 - 3.6)

When the ladle furnace's step down transformer is energized, there occurs an inrush current which has a high amount of 2^{nd} harmonic current. The amount of the 2^{nd} harmonic current of inrush current is harmful for the filter capacitors. To eliminate the risk of failure, the damping status of 2^{nd} harmonic filter is controlled by controlled resistors connected in parallel with damping resistors. These controllable resistors are taken into operation with LTTs when the current of any damping resistor passes predefined threshold level [24] (Figure 3.4).

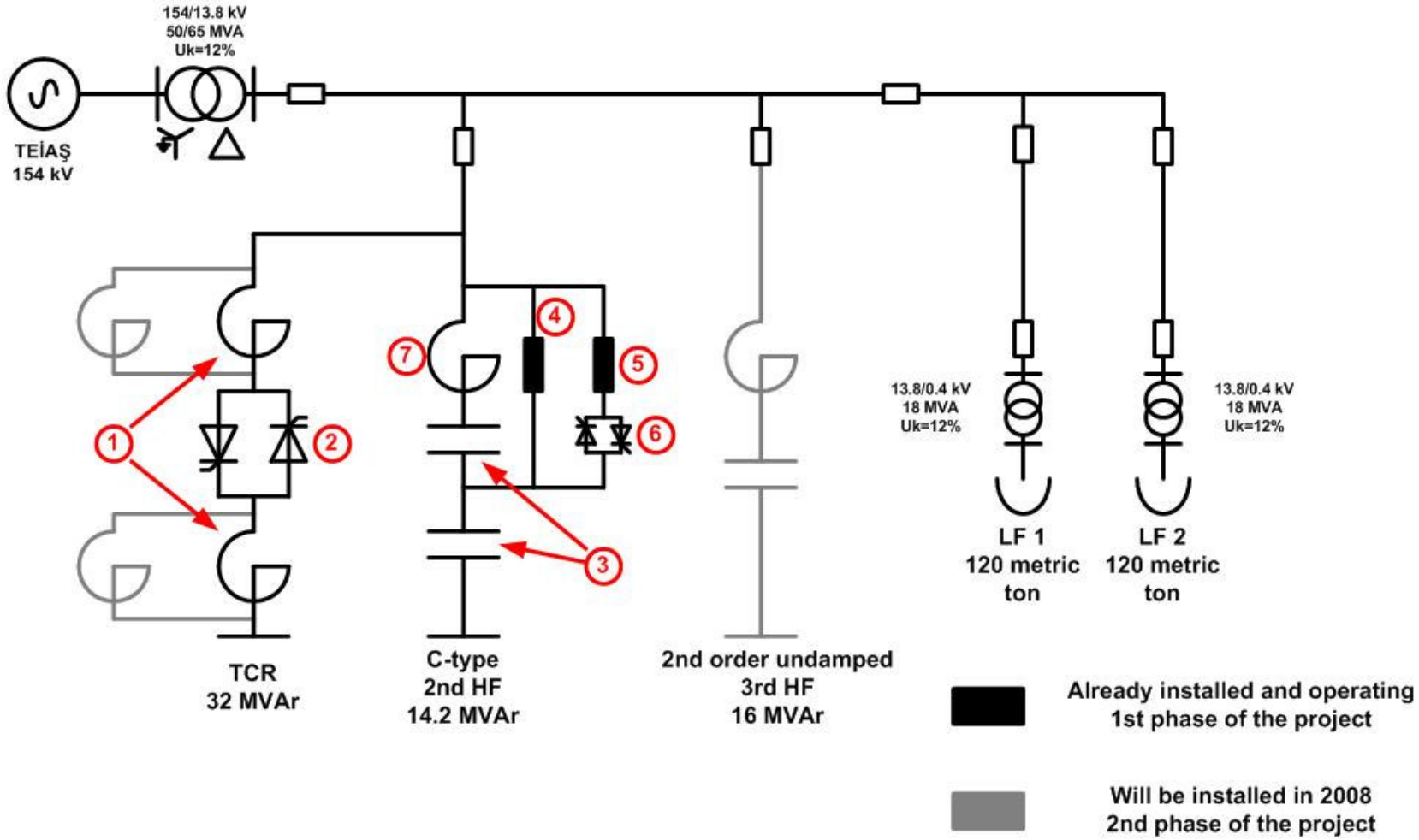


Figure 3.1. Connection diagram of power system of SVC

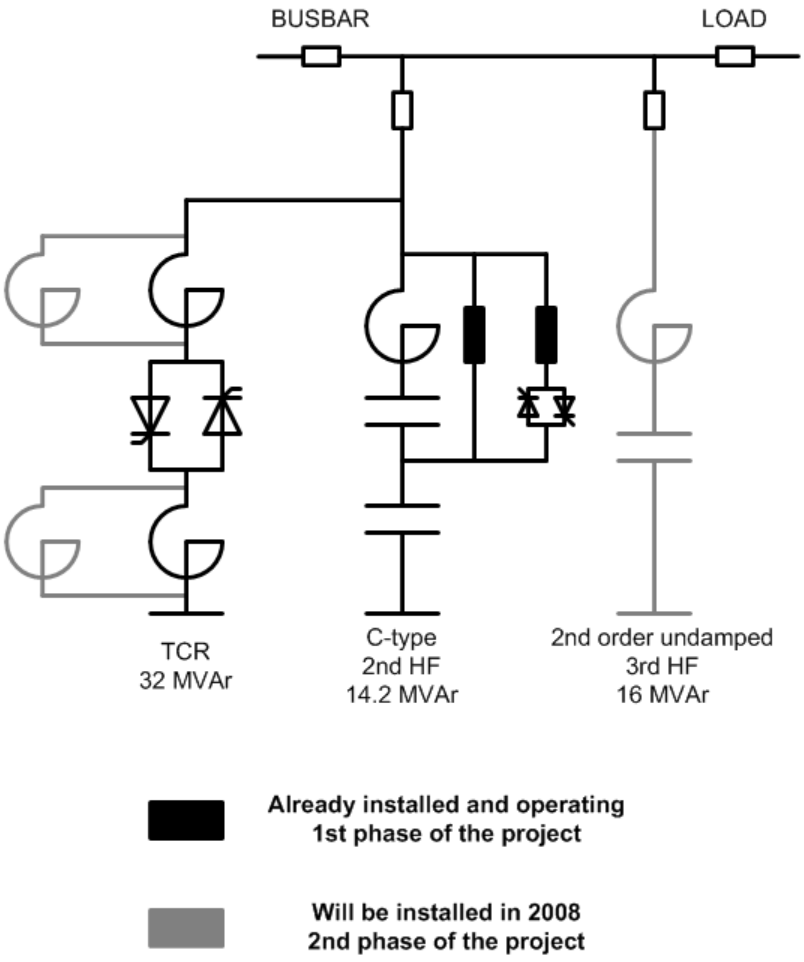
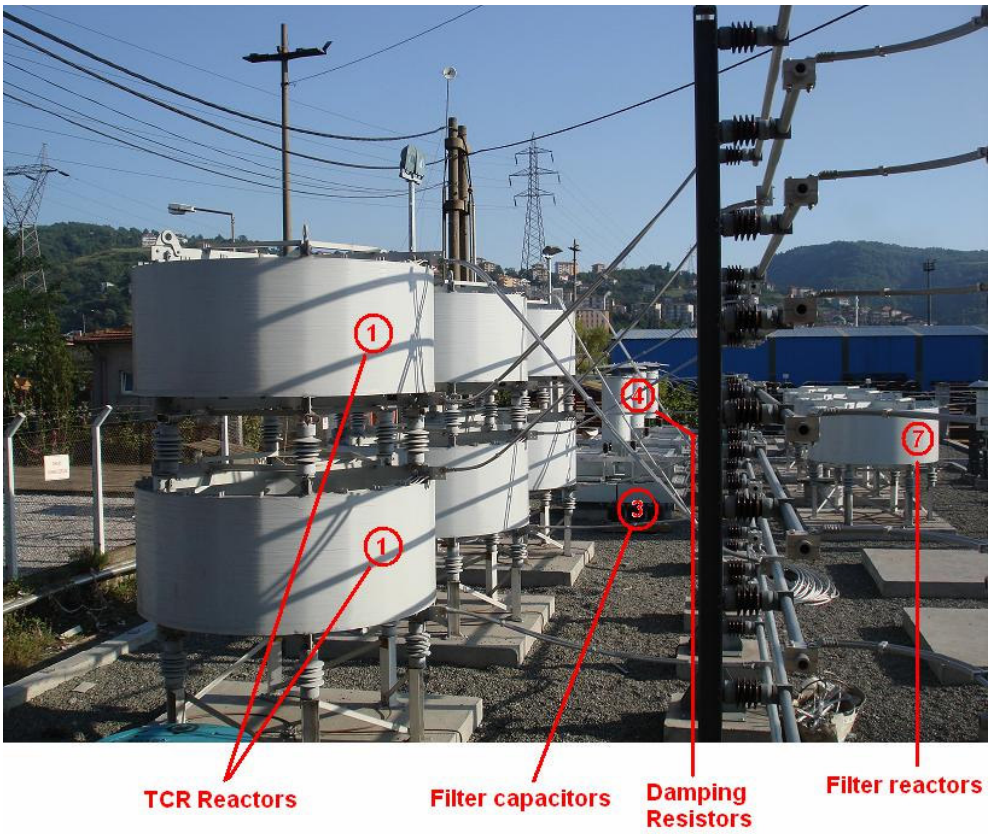


Figure 3.2. Power stage of SVC system



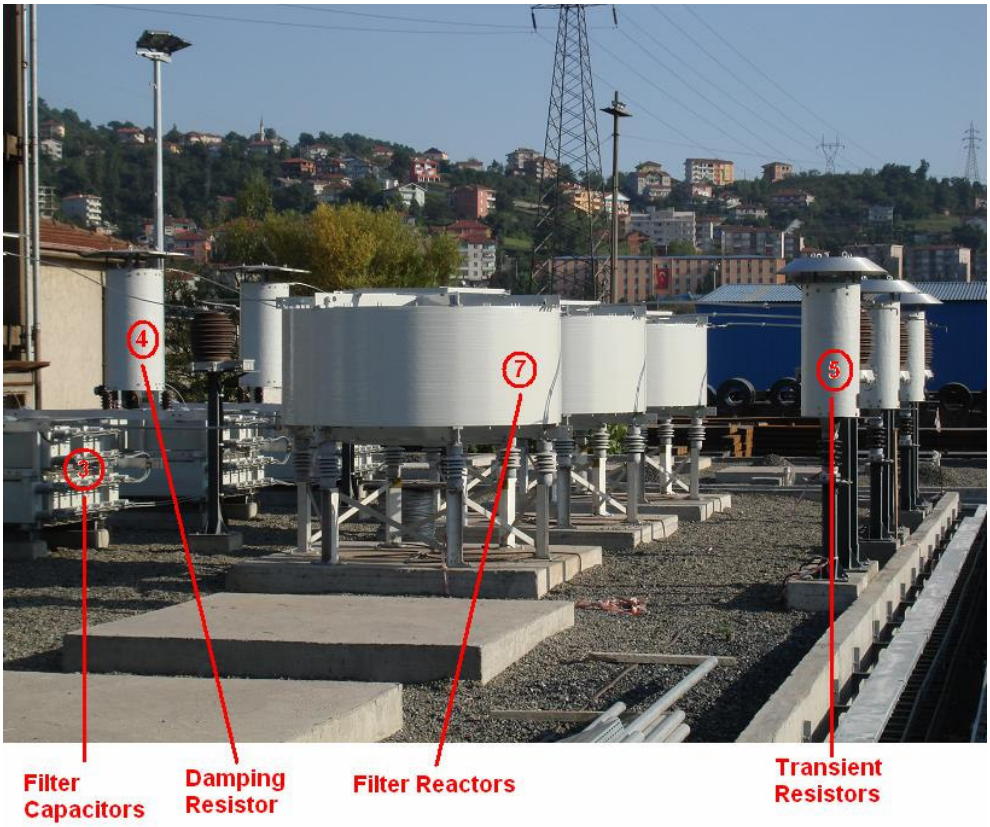


Figure 3.3. Views of power system elements of SVC (outside)

Figure 3.4. View of power system elements of SVC (inside)

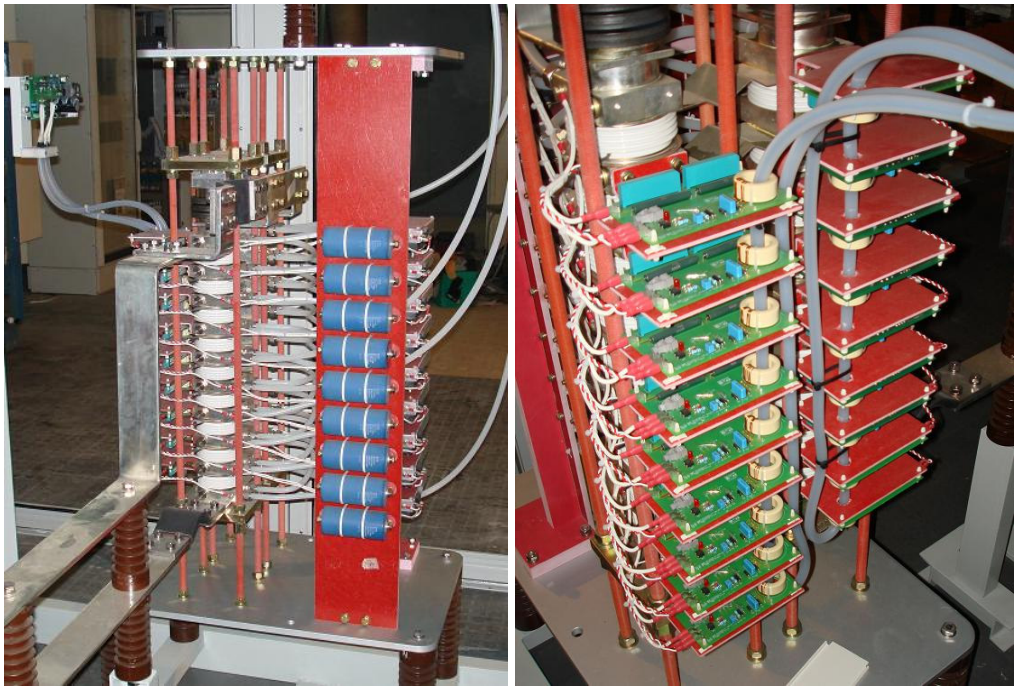


Figure 3.5 Thyristor stack

Figure 3.6 General view of indoor stage

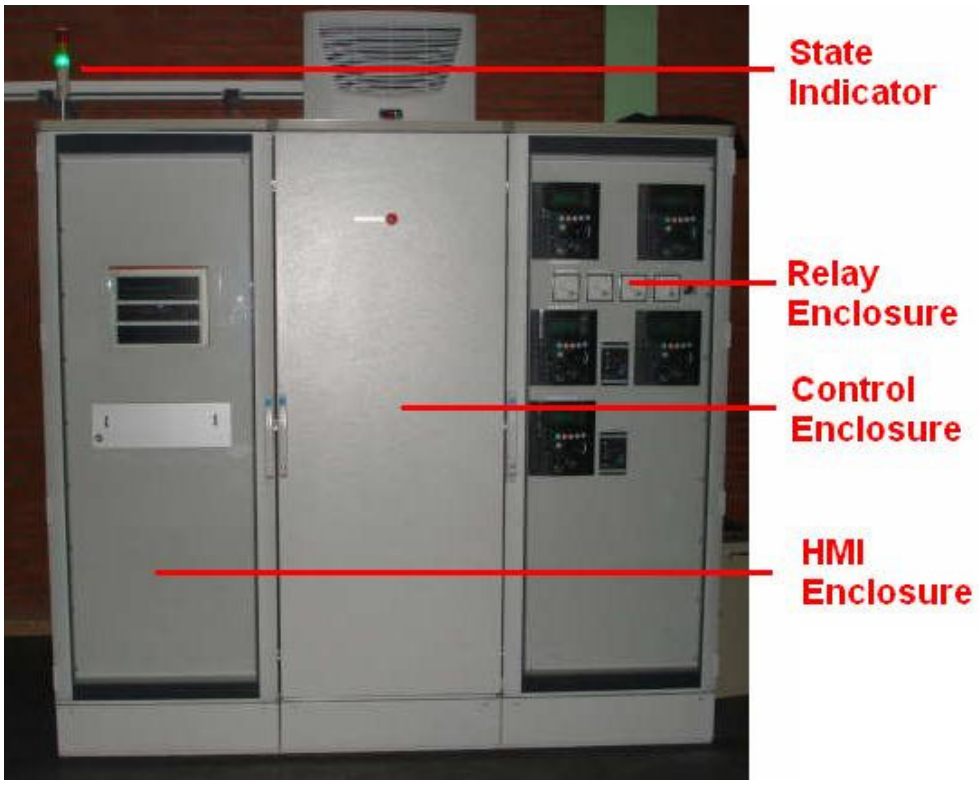


Figure 3.7 Control system enclosures

3.2 CONTROL STAGE

The control stage contains two main and three supplementary parts. The main parts are analog circuitry and NI CompactRIO Real-Time Controller. The supplementary parts are GE Fanuc PLC, GE F650 Bay controllers and PC based HMI.

3.2.1 SVC Control

The control of the SVC is a closed loop PI with a feedforward gain. The job of the control loop is calculating the firing angles of thyristors. The calculation is done with incoming and load reactive powers. SVC compensates the reactive power of incoming bus to the set value and balance the active power of the load at each phase at incoming bus. SVC is given the compensation job for both positive and negative sequences.

In the control scheme shown in Figure 3.3, the PI regulator calculates the required inductive reactive power for the system for compensation at each phase. The feedforward part makes the response of closed loop controller faster and improves the system stability. The basic control of SVC is calculating the load reactive power and with the known reactive power of capacitive filters firing the thyristors of TCR branches such that the incoming reactive powers are zero. This type of control, feedforward control, is inherently stable and fast. The PI element makes the incoming reactive powers accurate and eliminates the errors due to voltage changes, firing errors, measurement errors etc. For rapidly changing loads such as ladle furnaces, feedforward part makes the control robust and decreases reactive power error. This decrement makes the bus voltage oscillations [15] [18].

The control diagram and control system structure are shown in Figures 3.8 and 3.9.

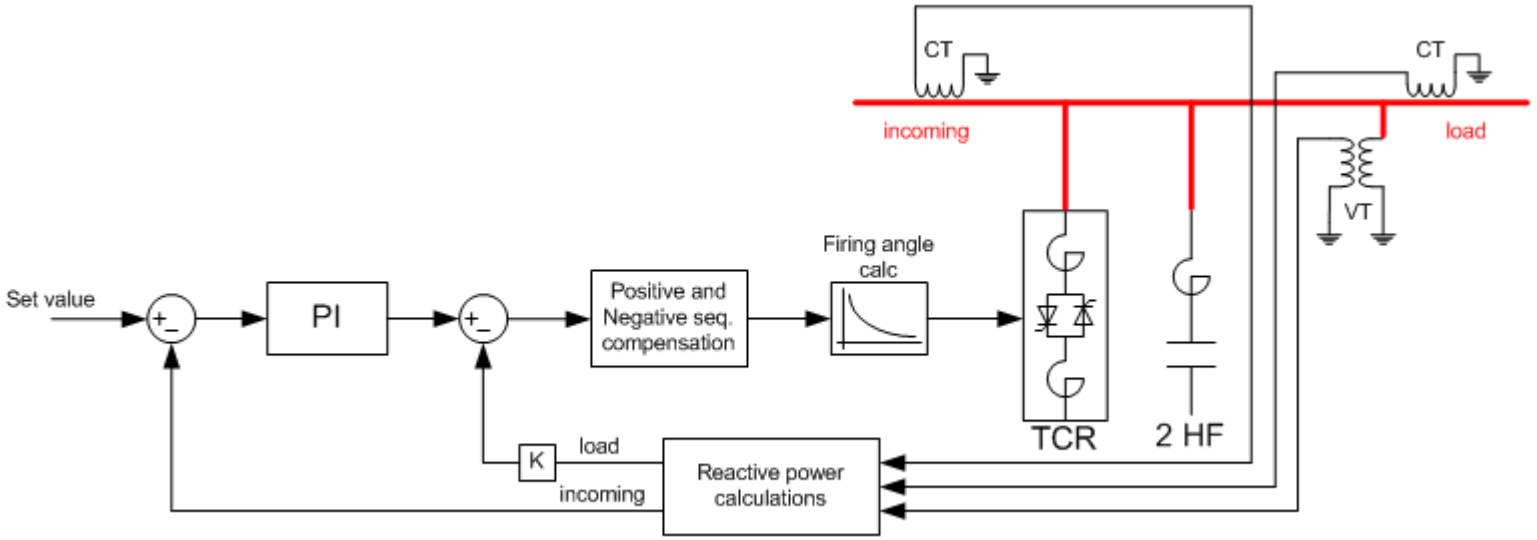


Figure 3.8. Control diagram of SVC

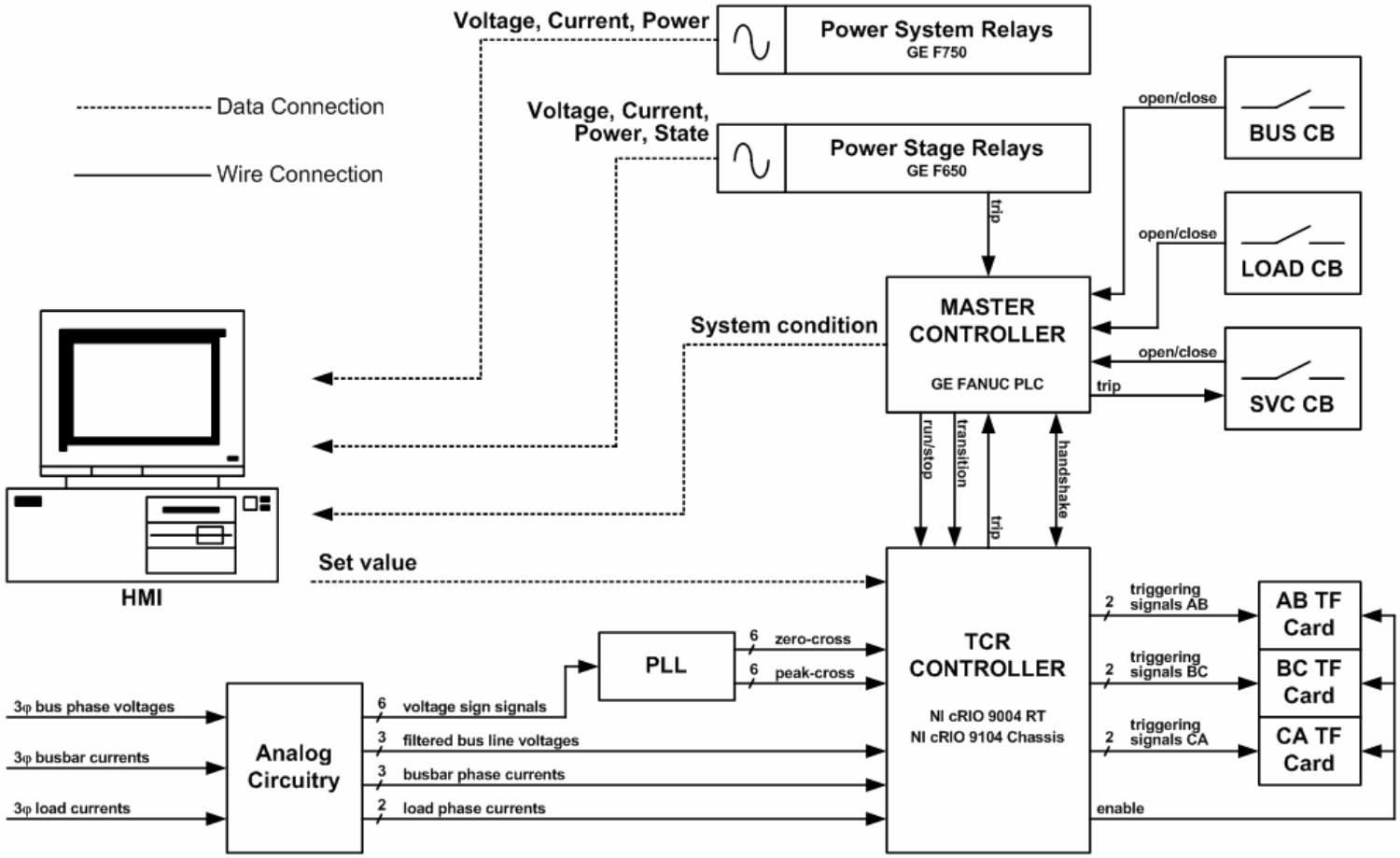


Figure 3.9. Control stage of SVC

The weights of its and feedforward controllers depend on reactive power measurement accuracy and speed, load variations, utility voltage fluctuations. If the load's current harmonic content has a big THD, then load reactive power measurement is not accurate to make the controller feedforward dominant. Since the incoming currents are total of load, TCR and harmonic filters then the THD of incoming busbar currents are decreased when compared to the load currents. If the power measurement is not capable of filtering current signals rapidly, then instead of using feedforward dominant control technique, it is more reasonable to use a feedback dominant control technique.

For reactive power calculation, the definition is that at each phase the phase current and phase voltage signal at 90° lagging are multiplied and the mean of this calculation for one period gives reactive power. For a 1ϕ voltage signal, the power calculation is done by delaying the voltage signal 90° (5 ms for 50 Hz power system). In a 3ϕ voltage signal instead of the delayed voltage signal, the other two phases' line-to-line voltage signal may be used.

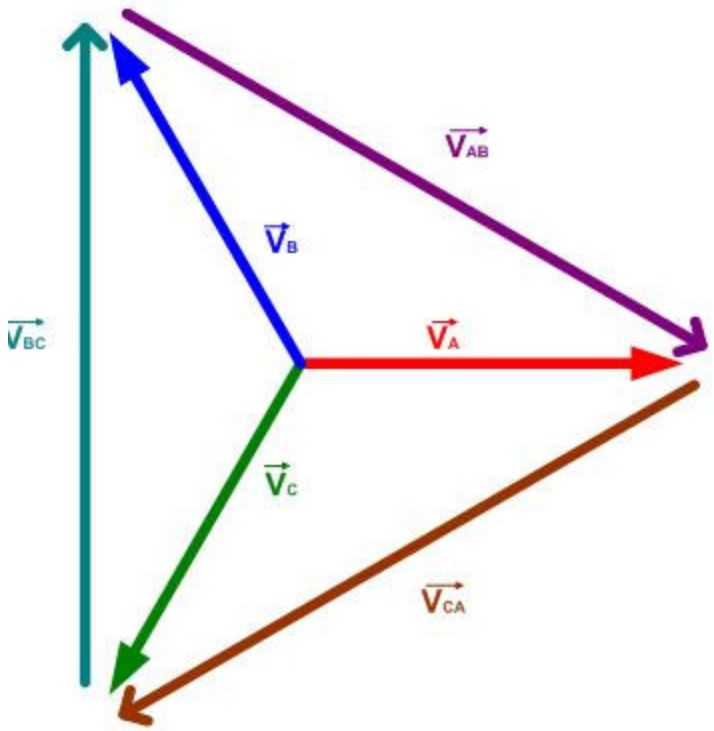


Figure 3.10. Voltage phasors for a 3ϕ system

The phase voltage phasors shown in Figure 3.10 are expressed in Equations 3.1 and 3.2.

$$\begin{aligned} V_A &= V\angle 0° \\ V_B &= V\angle -120° \\ V_C &= V\angle -240° \end{aligned} \tag{3.1}$$

$$\begin{aligned} V_{AB} &= V_A - V_B = \sqrt{3}V\angle -330° \\ V_{BC} &= V_B - V_C = \sqrt{3}V\angle -90° \\ V_{CA} &= V_C - V_A = \sqrt{3}V\angle -210° \end{aligned} \tag{3.2}$$

Instead of generating delayed signals, it is easier to use line-to-line voltages for reactive power calculation. In this case, the results are √3 times the reactive powers.

$$\begin{aligned} Q_A &= \frac{1}{T}\int_0^T V_A \cos(\omega t - 90°) \times I_A \cos(\omega t - \beta) dt \\ Q_A &= \frac{1}{\sqrt{3}}\frac{1}{T}\int_0^T V_{BC} \cos(\omega t) \times I_A \cos(\omega t - \beta) dt \end{aligned} \tag{3.3}$$

For line-to-line voltage calculation, the magnitudes of voltages are assumed the same for each line-to-line and the phases are assumed 120° far from the previous one. It means that there is no negative and zero sequence components for the supply voltage signals. Since SVC is connected without neutral and it has no capability to compensate the zero sequence component of the load, then only the line-to-line voltages are read by the controller.

If the load current has a negative sequence component, the voltage at the load bus has also a negative sequence component. When the SVC starts to the compensation of load, the incoming currents become balanced and the voltage drop on the line impedance becomes balanced. At the steady state operation, the bus voltages have no negative sequence component. For this part of operation, line

impedance has an important effect on load balancing. When the line impedance is large, load balancing operation takes more time which means longer settling time.

For reactive power compensation and load balancing, SVC compensates both negative and positive sequence currents of the load. The positive sequence compensation is done by injecting the inverse of one third of total reactive power to each phase.

Negative sequence compensation is the load balancing operation. For a 3ϕ balanced voltage system without neutral connection, when the reactive power of all phases are zero, then the load and SVC total is seen as three equal resistances connected to the bus. The main idea of compensation with load balancing is modeling the load as a delta connected circuit and controlling the SVC to eliminate the negative sequence and reactive components of the load currents.

$$\begin{aligned} V_a &= V \\ V_b &= V \text{ x } h^2 \\ V_c &= V \text{ x } h \\ h &= e^{j2\pi/3} = -1/2 + j\sqrt{3}/2 \end{aligned} \qquad (3.4)$$

The phase voltages are defined as shown in equation 3.7 and the line-to-line voltages becomes as follows.

$$\begin{aligned} V_{ab} &= V_a - V_b = (1 - h^2)\ V \\ V_{bc} &= V_b - V_c = (h^2 - h)\ V \\ V_{ca} &= V_c - V_a = (h - 1)\ V \end{aligned} \qquad (3.5)$$

Assuming that the load is delta connected then the delta branch currents of the load becomes;

$$\begin{aligned} I_{ab} &= Y_l^{ab} \text{ x } V_{ab} = Y_l^{ab} \text{ x } (1 - h^2)\ V \\ I_{bc} &= Y_l^{bc} \text{ x } V_{bc} = Y_l^{bc} \text{ x } (h^2 - h)\ V \\ I_{ca} &= Y_l^{ca} \text{ x } V_{ca} = Y_l^{ca} \text{ x } (h - 1)\ V \end{aligned} \qquad (3.6)$$

From the delta branch currents, the phase currents can be acquired

$$\begin{aligned} I_a &= I_{ab} - I_{ca} = (Y_l^{ab} \text{ x } (1 - h^2) - Y_l^{ca} \text{ x } (h - 1))\ V \\ I_b &= I_{bc} - I_{ab} = (Y_l^{bc} \text{ x } (h^2 - h) - Y_l^{ab} \text{ x } (1 - h^2))\ V \\ I_c &= I_{ca} - I_{bc} = (Y_l^{ca} \text{ x } (h - 1) - Y_l^{bc} \text{ x } (h^2 - h))\ V \end{aligned} \qquad (3.7)$$

Instead of calculating the phase impedances from phase currents, using symmetrical components of the currents makes the solution easier since one of the goals is eliminating the negative sequence currents (one of the symmetrical components). Then the symmetrical components of the line currents become as follows. To make the transformation orthogonal, $1/\sqrt{3}$ is used instead of 1/3.

$$\begin{aligned} I_0 &= (\ I_a + I_b + I_c\ ) / \sqrt{3} = 0 \\ I_1 &= (\ I_a + h \text{ x } I_b + h^2 \text{ x } I_c\ ) / \sqrt{3} = (Y_l^{ab} + Y_l^{bc} + Y_l^{ca}\ )\ V\sqrt{3} \\ I_2 &= (\ I_a + h^2 \text{ x } I_b + h \text{ x } I_c\ ) / \sqrt{3} \\ &= -\ (h^2 \text{ x } Y_l^{ab} + h \text{ x } Y_l^{bc} + Y_l^{ca}\ )\ \ V\sqrt{3} \end{aligned} \qquad (3.8)$$

With analogy the compensator currents will be

$$\begin{aligned} I_{0\gamma} &= 0 \\ I_{1\gamma} &= j\ (B_\gamma^{ab} + B_\gamma^{bc} + B_\gamma^{ca}\ )\ V\sqrt{3} \\ I_{2\gamma} &= -j\ (h^2 \text{ x } B_\gamma^{ab} + h \text{ x } B_\gamma^{ba} + B_\gamma^{ca}\ )\ \ V\sqrt{3} \end{aligned} \qquad (3.9)$$

For negative sequence compensation the equation (3.10) and for reactive power compensation in positive sequence equation (3.11) should be satisfied.

$$I_{2l} + I_{2\gamma} = 0 \qquad (3.10)$$

$$Im\ (I_{1l}\ ) + Im\ (\ I_{1\gamma}\ ) = 0 \qquad (3.11)$$

Using equations 3.10 and 3.11 with 3.9, the delta branch impedances of compensator become as follows

$$
\begin{aligned}
B_\gamma^{ab} &= -1/(3\sqrt{3}V)\,(\,\mathrm{Im}\,(\,I_{1l}\,) + \mathrm{Im}\,(\,I_{2l}\,) - \sqrt{3}\,\mathrm{Re}\,(\,I_{2l}\,)\,) \\
B_\gamma^{bc} &= -1/(3\sqrt{3}V)\,(\,\mathrm{Im}\,(\,I_{1l}\,) - 2\,\mathrm{Im}\,(\,I_{2l}\,)\,) \\
B_\gamma^{ca} &= -1/(3\sqrt{3}V)\,(\,\mathrm{Im}\,(\,I_{1l}\,) + \mathrm{Im}\,(\,I_{2l}\,) + \sqrt{3}\,\mathrm{Re}\,(\,I_{2l}\,)\,)
\end{aligned}
\qquad (3.12)
$$

Converting the symmetrical component impedances in equation (3.9) to delta branch impedances, the result becomes as

$$
\begin{aligned}
B_\gamma^{ab} &= -1/(3V)\,(\,+\,\mathrm{Im}\,(\,I_{al}\,) + \mathrm{Im}\,(\,hI_{bl}\,) - \mathrm{Im}\,(\,h^2I_{cl}\,)\,) \\
B_\gamma^{bc} &= -1/(3V)\,(\,-\,\mathrm{Im}\,(\,I_{al}\,) + \mathrm{Im}\,(\,hI_{bl}\,) + \mathrm{Im}\,(\,h^2I_{cl}\,)\,) \\
B_\gamma^{ca} &= -1/(3V)\,(\,+\,\mathrm{Im}\,(\,I_{al}\,) - \mathrm{Im}\,(\,hI_{bl}\,) + \mathrm{Im}\,(\,h^2I_{cl}\,)\,)
\end{aligned}
\qquad (3.13)
$$

By this formula, the branch impedances of SVC can be calculated due to wye impedances of load. For AB branch

$$
\begin{aligned}
B_\gamma^{ab} &= -1/3\,(\,+\,\mathrm{Im}\,(\,I_{al}/V) + \mathrm{Im}\,(\,hI_{bl}/V) - \mathrm{Im}\,(\,h^2I_{cl}/V)\,) \\
B_\gamma^{ab} &= -1/3\,(\,+\,\mathrm{Im}\,(\,I_{al}/V_a\,) + \mathrm{Im}\,(\,I_{bl}/V_b\,) - \mathrm{Im}\,(\,I_{cl}/V_c)\,) \\
B_\gamma^{ab} &= -1/3\,(\,+\,\mathrm{Im}\,(\,Y_l^{\,a}\,) + \mathrm{Im}\,(\,Y_l^{\,b}\,) - \mathrm{Im}\,(\,Y_l^{\,c})\,) \\
B_\gamma^{ab} &= -1/3\,(\,+\,B_l^{\,a} + B_l^{\,b} - B_l^{\,c}\,)
\end{aligned}
\qquad (3.14)
$$

When both sides are multiplied by V^2 then the equation becomes for AB branch as follows

$$
\begin{aligned}
V^2\,B_\gamma^{ab} &= -1/3\,(\,+\,B_l^{\,a} + B_l^{\,b} - B_l^{\,c}\,)\,V^2 \\
(\sqrt{3}V)^2\,B_\gamma^{ab} &= -\,(\,+\,V^2\,B_l^{\,a} + V^2\,B_l^{\,b} - V^2\,B_l^{\,c}\,) \\
V_{l\text{-}l}^{\,2}\,B_\gamma^{ab} &= -\,(\,+\,V^2\,B_l^{\,a} + V^2\,B_l^{\,b} - V^2\,B_l^{\,c}\,) \\
Q_\gamma^{ab} &= -\,(\,Q_l^{\,a} + Q_l^{\,b} - Q_l^{\,c}\,)
\end{aligned}
\qquad (3.15)
$$

$$
\begin{aligned}
Q_\gamma^{ab} &= -\,(\,+\,Q_l^{\,a} + Q_l^{\,b} - Q_l^{\,c}\,) \\
Q_\gamma^{bc} &= -\,(\,-\,Q_l^{\,a} + Q_l^{\,b} + Q_l^{\,c}\,) \\
Q_\gamma^{ca} &= -\,(\,+\,Q_l^{\,a} - Q_l^{\,b} + Q_l^{\,c}\,)
\end{aligned}
\qquad (3.16)
$$

3.2.2 Analog Circuitry

The power system data acquired by voltage and current transformers are converted to electronic signals by an analog circuitry (Figure 3.11). The signals for reactive power calculation and thyristor firing are built at this part. The electric signals from voltage and current transformers are converted to small voltage signals via lems.

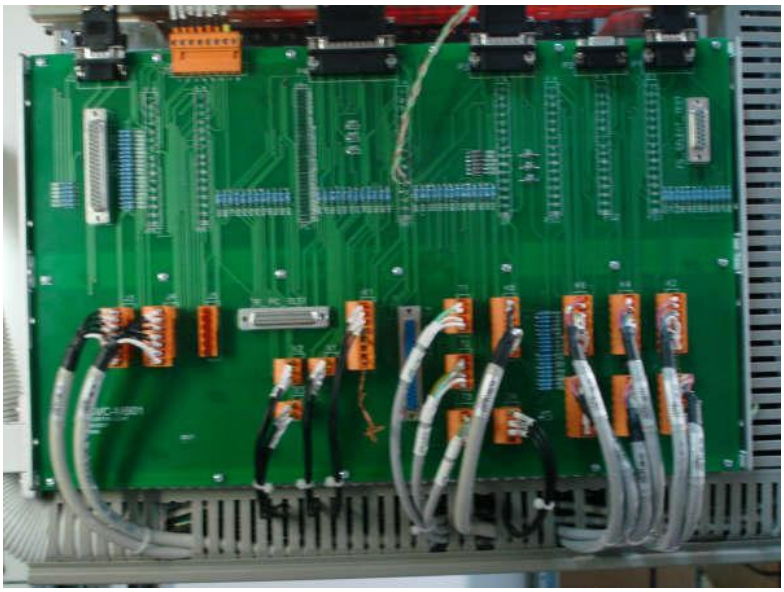


Figure 3.11. Analog circuitry

Since the SVC system can compensate the reactive power at the fundamental frequency, then the reactive power calculation for compensation should include only the fundamental components of the voltage and current signals. For this purpose, the voltage signals are filtered by a bandpass filter tuned to fundamental frequency, 50 Hz. Reactive power calculations are done by multiplying voltage and current signals. Since the integral of two signals at different frequencies and in product form is zero over one cycle, then filtering only voltage signals is enough to calculate the reactive power at fundamental frequency. Reactive power calculation with fundamental components of voltage and current signals gives the same result

with reactive power calculation with the filtered voltage and the unfiltered current signals.

$$V = \sum_n V_n \cos(n\omega t + \alpha_n) \tag{3.17}$$

$$I = \sum_n I_n \cos(n\omega t + \beta_n) \tag{3.18}$$

$$\frac{1}{T}\int (V \times I)dt = \frac{1}{T}\int (V_1 \times I)dt = \frac{1}{T}\int (V_1 \times I_1)dt \tag{3.19}$$

Thyristors of TCR are phase controlled and the phase reference is acquired by the zero-crosses of line voltages. To avoid multiple zero-crosses, filtered voltage signals are used for the phase reference. To avoid misfiring which cause flow of DC current, the thyristors should be triggered after the peaks of voltage signals. The peaks of voltage signals are detected by a PLL circuit. The input of the PLL circuit is a square wave generated by voltage signals, and output is the sign of voltage signals. The filtered voltage signals are compared to ground by a comparator and the output of the comparator is used as voltage sign signal. The peak of line voltage is the middle of the sign signal that is the second most significant bit of PLL counter. Using PLL guarantees that firing pulses to the thyristor stacks are always after the voltage peak and the risk of DC firing vanishes. Here, the important criterion for the PLL stage is the response time of the circuitry to the frequency changes at the bus voltage. When there is a frequency change, the PLL should settle down rapidly and generate the new peak signals at new position. The PI controller inside the PLL should not oscillate in a large scale. Since the triggering reference is the output of PLL, then the firing angle of TCR oscillates and the reactive power generated by the TCR also oscillates due to PLL PI oscillations. The PI parameter setting of PLL is carried out assuming that the bus frequency changes are 0.1 Hz for a cycle. Since the PLL input square wave is generated from the filtered voltage signal, the minor changes occurring the transients are eliminated and only the major frequency changes of utility frequency are effective. For PLL stage, CD4046BE (Figure 3.12) is used and the error of the peak signal is set to 5 us.

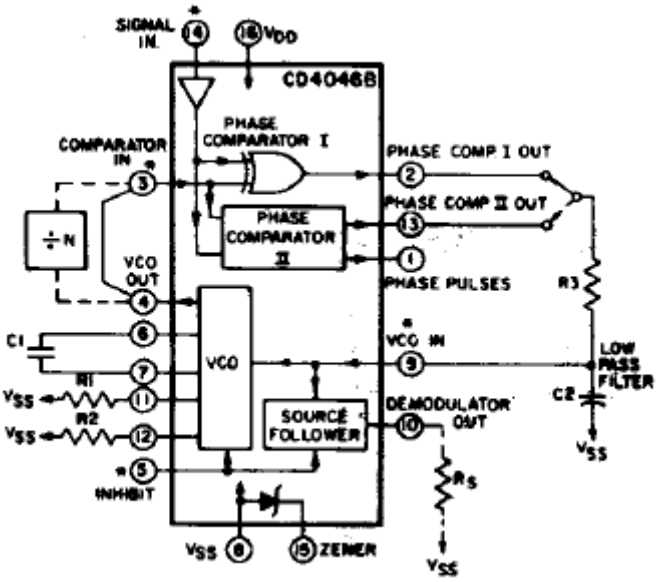


Figure 3.12. Inside of CD4046BE PLL

3.2.3 Real-Time Computing

The term *real-time* refers to an application that receives information and the corresponding output is immediately responded without any delay. In real-time world, input information and output response are synchronous with no time period.

In a *real-time system*, the deadlines between inputs and outputs are predefined and the execution time between the input event and the system response is always constant (Figure 3.13). By contrast, a non-real-time system has no deadlines for outputs and even if its responses to input events are very fast [10][11][12][13][14].

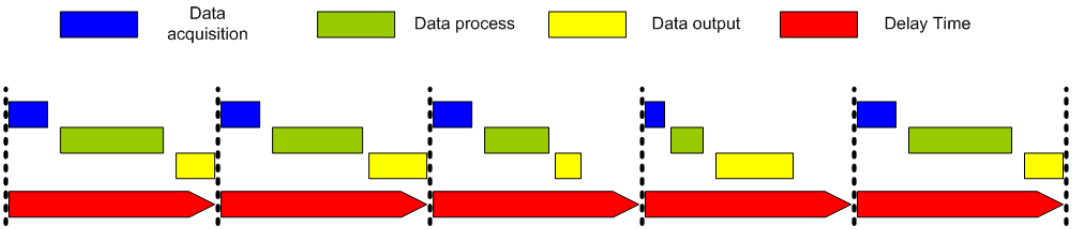


Figure 3.13. Real-Time system operation

In electrical manner, fully analog electronic systems are real-time systems. The time delay between any input and its corresponding output is always constant. In ideal case there is no delay and in practical case the delays due to internal impedances of ICs are constant. A dedicated digital electronic system is also a real-time system. For example, a flip-flop circuit triggered with a clock signal and changing its state at each clock pulse is a real-time system. The output state of the flip-flop is defined by the present state and the input signal. Computer based real-time systems are the result of the developments of microcomputer (μC) technologies. For a μC based real-time system, the μC program has deadlines for the responses to the input events.

In a real-time system correctness of operation depends not only upon the right outputs but also upon the time delays. If the corresponding output is not responded for an input event before deadline, it is called as a *real-time system failure* (Figure 3.14).

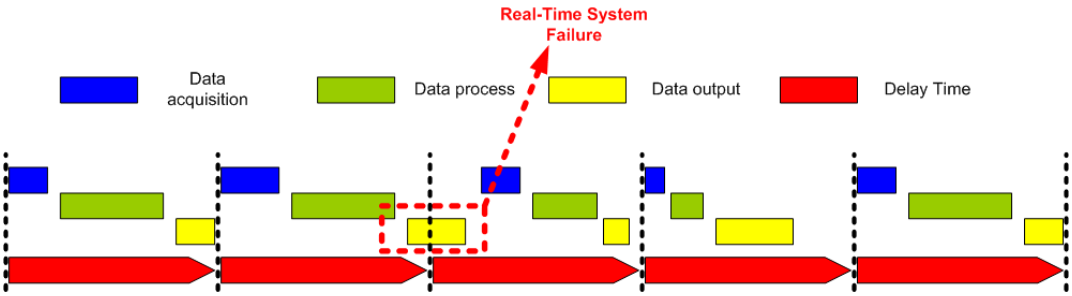


Figure 3.14. Real-Time system failure

3.2.4 LabVIEW and NI CompactRIO Real-Time Controller

LabVIEW (abbr. of **Lab**oratory **V**irtual **I**nstrumentation **E**ngineering **W**orkbench) is a virtual programming language (VPL) of National Instruments (NI). LabVIEW development environment provides data acquisition, instrument control, industrial control and measurement, and embedded design abilities to user. It is available on various platforms such as Windows, UNIX, Linux and Mac OS.

The NI CompactRIO (**R**econfigurable **I/O**) programmable automation controller (PAC) is a reconfigurable control and acquisition system that includes a real-time processor and a reconfigurable chassis with FPGA connected analog and digital I/O modules. NI cRIO RT Controller 9004 has 195 MHz processor, 64 MB DRAM and 512 MB CompactFlash. NI cRIO 9104 Reconfigurable Embedded Chassis has 3 MGate Xilinx FPGA chip (XC2V3000-4FG676I) and 8 reconfigurable slots.

The main part of SVC control stage is NI CompactRIO controller (Figure 3.15). Reactive power calculations, PI controller and firing pulse generation take place inside the chassis FPGA of cRIO. The chassis structure is configured for the requirements of reactive power calculation and firing pulses. There are also digital I/Os for system control.

The reactive power calculations are made by using the equation 3.3. The current and voltage signals are sampled periodically in 16 bit form with a sampling rate 25 kHz simultaneously, and for each phase reactive power is calculated by its using current and the other phases by line-to-line voltage signal. At each sampling, the current and voltage signals are multiplied. The analog input channels have noise. Moreover, the integrator has 32 bit register and the sum of 500 data at each cycle may overflow this register. To eliminate the noise of input signals and the risk of overflow, the result of the multiplication is divided with a constant. The division is done by a shift register which is faster than the standard divider element and occupies less memory in the FPGA.

The result of division is put in to an integrator. This operation is the integral part of Equation 3.3. The output of this integrator is sampled at each zero cross of voltage signal and later in the next sampling step, the integrator is reset. In the next step, the multiplication result is taken as initial value to the integrator not to lose the sampled data.

Figure 3.15. NI cRIO mounted inside the control enclosure

The following code part of LabVIEW FPGA calculates the reactive power of phase A for incoming and load busses. The sampled signal data are multiplied by a 32 bit multiplier. The zero cross detector generates a TRUE signal if the voltage crosses 0 V to sample the integrator data and reset the integrator in the next step. The signal is delayed for a sampling step time, 40 us. When a zero cross occurs for voltage signal, the integral output is written to a local variable. If the zero-cross type is selected “either”, then the calculations are done for every half cycle; if the direction is selected “minus-plus” or “plus-minus”, then the calculations are done for full cycle.

For the reactive power formula in Equation 3.3, the 1/T constant is ignored in calculation operation because of the sampling rate. If the sampling rate is low and the number of sampled data at each cycle is small, then the right way to measure the reactive power is to synchronize the sampling frequency to line frequency, which means constant sampling at each cycle. If the sampling frequency is high enough, the output of integral gets nearer to (50 Hz / Line frequency) x Actual Reactive Power. For a constant sampling rate, the variations in reactive power calculation vary only with line frequency changes. Since the line frequency varies in a narrow range and the rate of change of line frequency is small, then eliminating 1/T part of Equation 3.3 changes the calculated reactive power in a small range which can be corrected by the PI controller easily.

The code shown for reactive power calculation (Figure 3.16) for incoming and load bus at phase B. For the other phases, the code is the same with other analog channels.

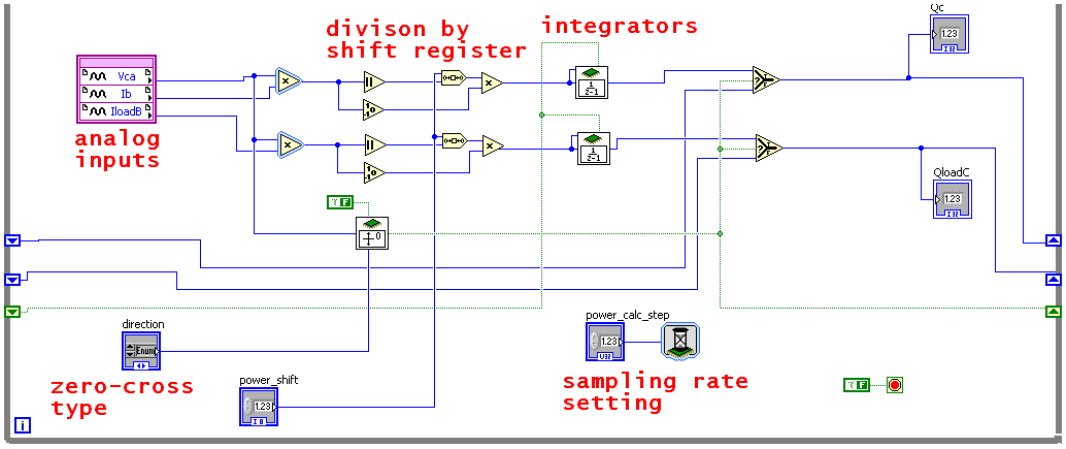


Figure 3.16. Reactive power calculation loop for phase B

The reactive power calculation loop is an infinite loop. It samples the analog inputs continuously and calculates the reactive power of the input signals.

The second part of the code is PI loop that takes the set values and the calculated values of reactive power as input and runs 3 parallel PI controllers one for each phase. The feedforward part takes place at the output of PI component and the reactive power of the load is multiplied with a constant between 0 and 1 and it is subtracted from PI output.

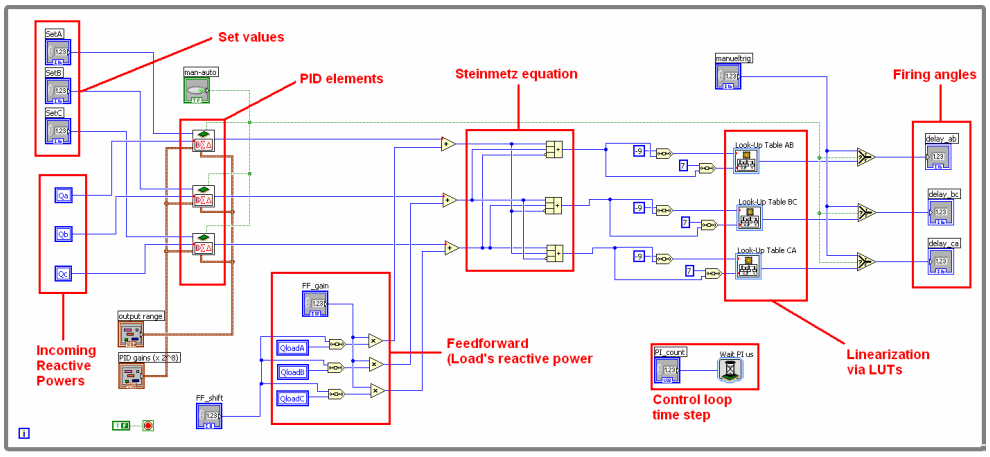


Figure 3.17. Control loop

In the control loop (Figure 3.17 and 3.18), the discrete time PID components of LabVIEW FPGA are used as PI controller. The definition and formulas for the P,I and D constants are as follows.

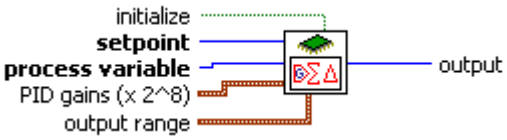


Figure 3.18. Discrete PID component of LabVIEW FPGA

$$output(n+1) = Pe(n) + I\sum_{i=0}^{n} e(i) - D\Delta PV(n) \qquad (3.20)$$

$\Delta PV(n) = PV(n) - PV(n-1)$

$e(n) =$ **setpoint**$(n) - PV(n)$

T_s = sampling interval, T_i integral time (both in minutes)

$$P = K_c$$

$$I = K_i * T_s$$

$$D = K_d / T_s$$

$$K_i = K_c / T_i$$

$$K_d = K_c * T_d$$

When these discrete time constants are converted to time domain constants, then the P, I and D becomes as

$$P = Kc / 2^8$$

$$I = Kc \times (Ts / Ti) / 2^8 \qquad (3.21)$$

$$D = Kc \times (Td / Ts) / 2^8$$

Here, the P, I and D constants are 16 bit integers and the first 8-bit is the integer part. The second 8-bit part is the floating part of PID constants.

The firing angles are calculated in μs resolution via look-up tables at the output of PI+FF stage. The output of control loop is mapped to triggering angle with the TCR power equation. To eliminate the risk of firing after 180° degree, the upper limit of firing angle is set to 9.7 ms from zero cross which is equal to 174.6°. The firing angle values in us are stored in local variables at each PI cycle.

If manual triggering option is selected, then the PI elements are reset, the outputs and the integrator inside is set to zero, and the firing angles are set to the manual trig angle. This operation is built for test procedures of SVC system. After returning to auto running mode, the PI elements start to run. At the beginning of auto control, the outputs of PI elements are limited to the upper value and this

limitation increases to its normal state step by step. This kind of control provides soft start to the SVC operation.

The triggering pulses are generated by using the peak signals as reference. The zero-cross and peak signals of each line-to-line voltage signal from the PLL are taken as digital inputs for triggering pulses. Each thyristor stack has two triggering pulse for both positive and negative half cycles. For each side, the zero cross signal starts the triggering operation. To eliminate the risk of multiple PLL pulse error, after zero-cross signal is read, the operation waits 3 ms and starts to wait the peak cross signal. For every firing pulse, the corresponding zero-cross and peak-cross signals become retrieved in right order. This operation, reading two pulses, guarantees safe operation of triggering loop (Figure 3.19 and 3.20).

After the peak-cross signal is read from the PLL, the triggering loop waits for the corresponding delay time calculated for the thyristor stack side of the loop. The wait time has no normalization for frequency changes and the reactive power error from firing angle error is assumed to be corrected by the PI controller. Here, since the PLL is driven by the filtered voltage signals, the firing angle error for one cycle comes from major frequency changes at the utility and this error is corrected in the PI loop in the next cycles.

The angle output at the PI loop is sampled when the peak-cross signal is retrieved. Since the PI loop runs in time domain and asynchronous to line frequency, then it is better to take the latest delay angle to give the best response. The firing pulse pattern has 4 pulses with 50 us period and 50% duty cycle. This pulse train is sent to triggering cards if the triggering operation is enabled.

At each firing loop, the period of the zero-cross signal is calculated to monitor the operation of PLL and utility frequency. These period values are monitored by the CompactRIO RT and if these values exceed the frequency limits, then a trip signal is generated to stop the operation. Since these period values belongs to zero-cross signals, by this operation the correct operation of analog cards is verified.

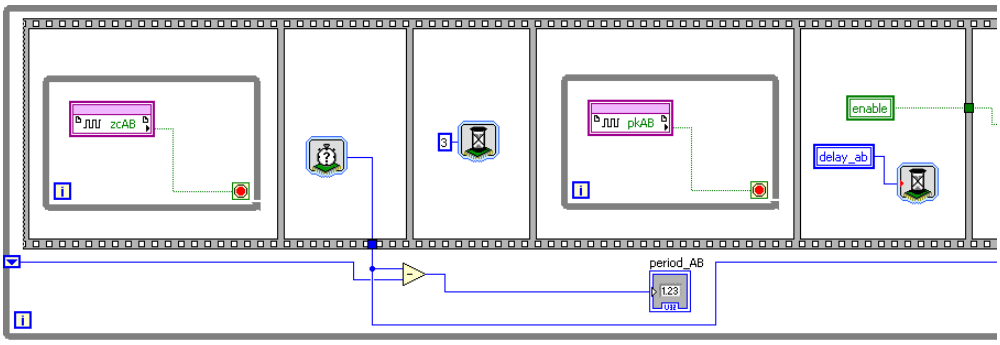


Figure 3.19. Detection of ZC and PC signals

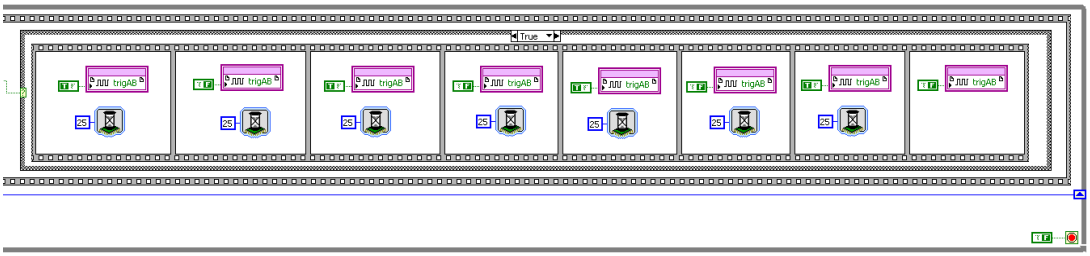


Figure 3.20. The pulse train generation

After the triggering pulse generation, the loop restarts and waits for the next zero-cross pulse. There are 6 triggering loops for each side of thyristor stacks. Each triggering loop is an infinite loop as reactive power calculation and PI loops. This pulse train is applied to the firing PCBs near the stacks through fiber optic cables by thyristor firing cards. Thyristor firing cards monitor voltage on thyristor stacks and decides whether or not the pulse train is to be applied by considering the states of thyristors.

3.2.5 Supplementary Elements

The supplementary elements of control system are GE Fanuc PLC, GE F650 Bay controllers and PC based HMI. The PLC and other control units can be seen in Figure 3.19.

The PLC is located inside the control enclosure (Figure 3.21), and it controls the whole electric and electronic equipment inside and outside the cabinets. In addition the PLC permits the circuit breaker for closing. CompactRIO's operation is controlled by a handshaking method by the PLC. A square wave is generated by the PLC and it is sent to CompactRIO and then the FPGA part generates the inverse of the square wave and sends back it to PLC immediately.

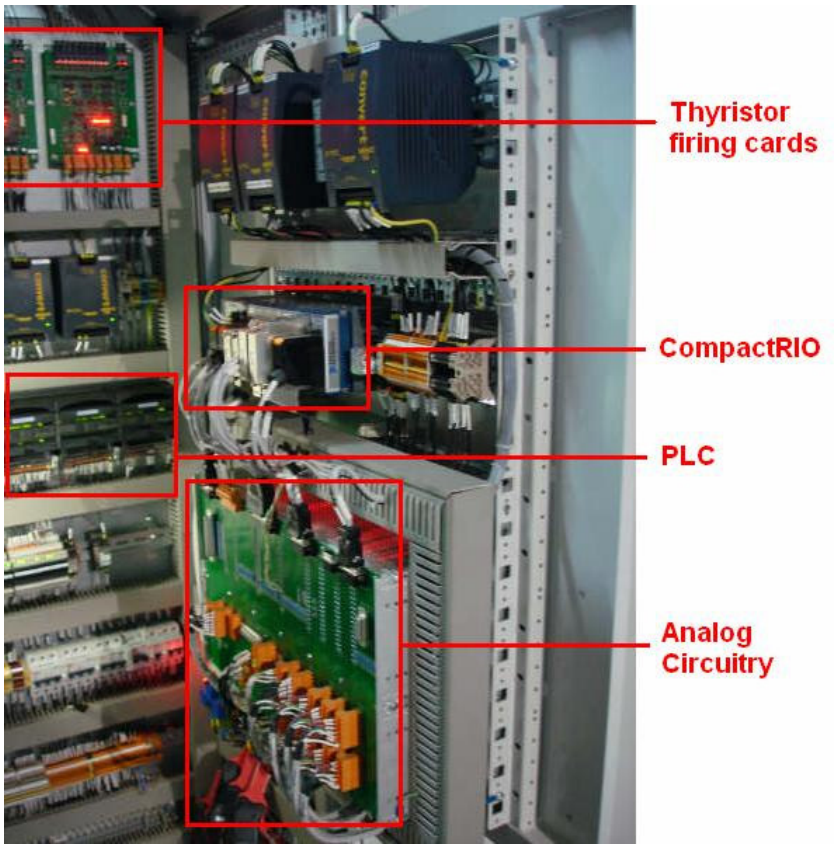


Figure 3.21. Inside of control enclosure

The bay controllers are protection relays for TCR, HF and HF resistors. The phase currents are monitored in case of a short circuit fault or malfunction, then a trip signal is sent to the PLC to stop the operation.

The HMI is PC based interface for the operators that is programmed with GE Cimplicity and gives the user the ability of watching the system status, voltage, current and power values and controlling the reactive power set value of the SVC system.

CHAPTER 4

SIMULATION WORK

4.1 SIMULATION PLATFORM

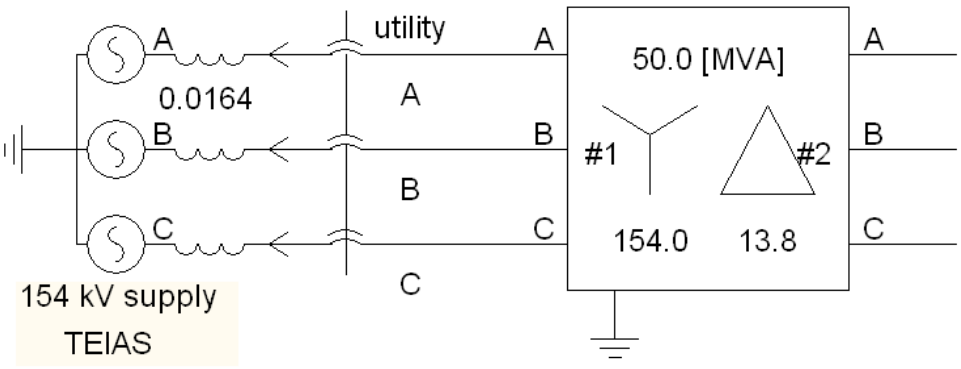
The system simulations are carried out by using PSCAD/EMTDC 3.0.8 program running on a PC with Intel Pentium 4 3.2 GHz CPU and 2GB RAM. The simulation time step is selected as 5 μs to give accurate results.

In the simulations, instead of PSCAD original blocks such as reactive power, RMS, SVC, all the elements are rebuilt to meet the same results inside the controller. The power calculations are done at each halfcycle of line-to-line voltages. Moreover the power system side of the SVC is built with the table parameters of reactors and capacitors.

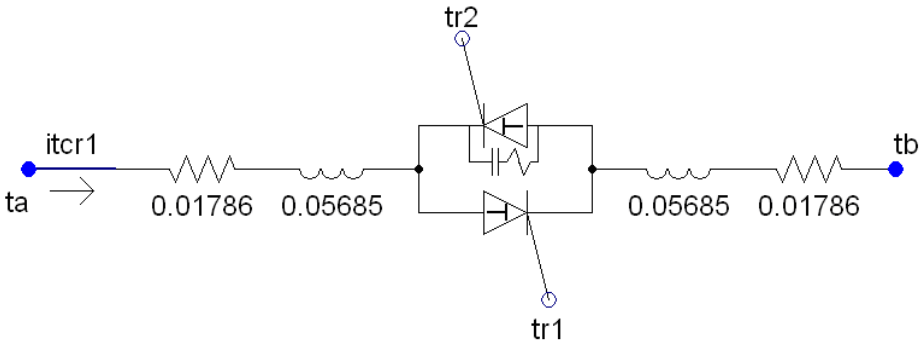
For the power stage simulations, the TCR and HF reactors are modeled with internal resistance. Instead of using a 13.8 kV supply, the power transformer is also modeled in the switchyard.

In the simulations, step response of PI+FF is calculated for different control parameters. An adaptive control technique is tested for total compensation of the load even if load balancing operation is not available due to the lack of power capacity of the SVC.

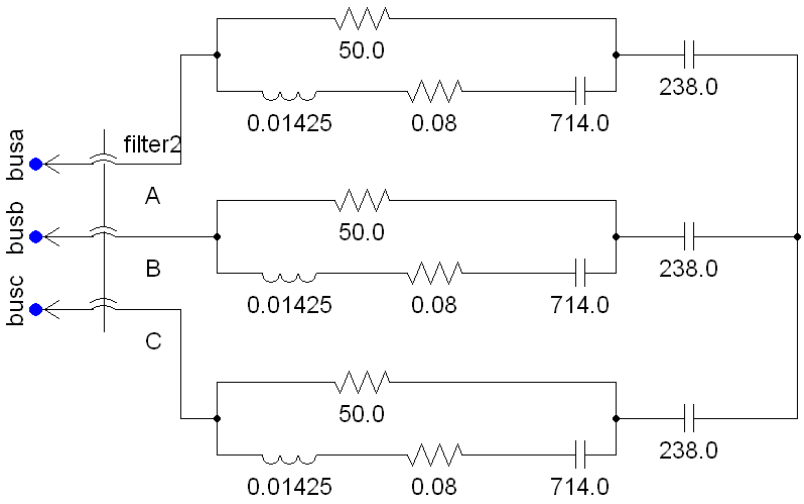
The elements used in simulations are shown in Figure 4.1.



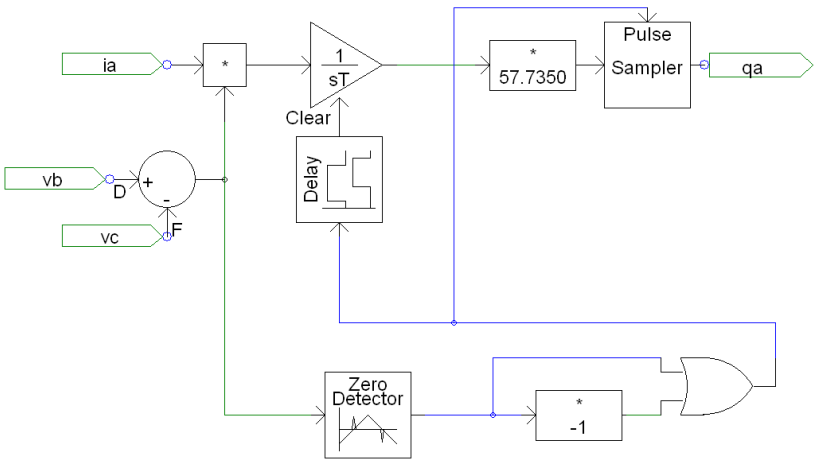
(a)



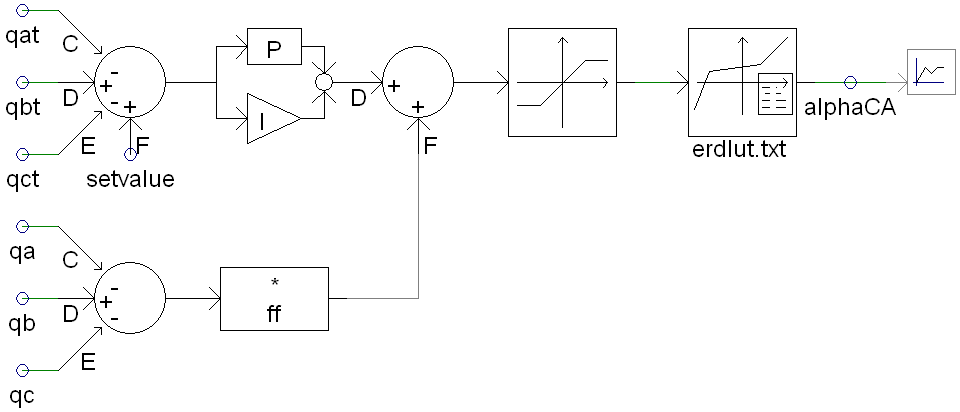
(b)



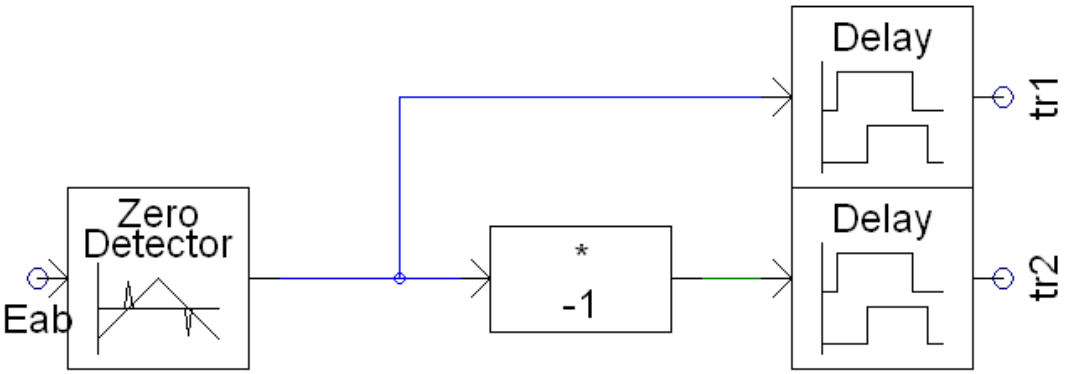
(c)



(d)



(e)



(f)

Figure 4.1. Simulation elements

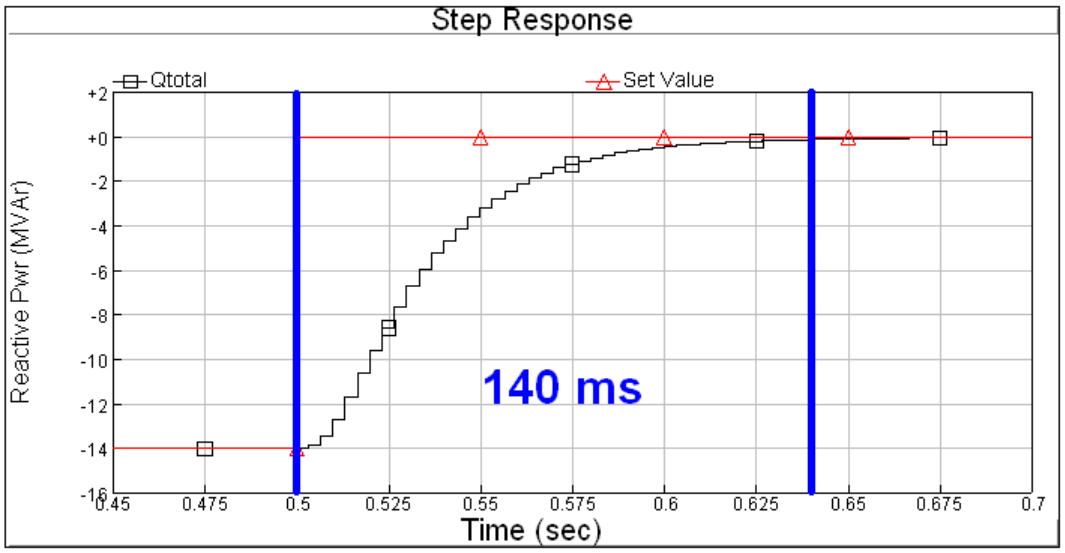
(a) supply and power transformer (b) TCR branch and thyristor

(c) 2nd harmonic filter (d) reactive power calculation

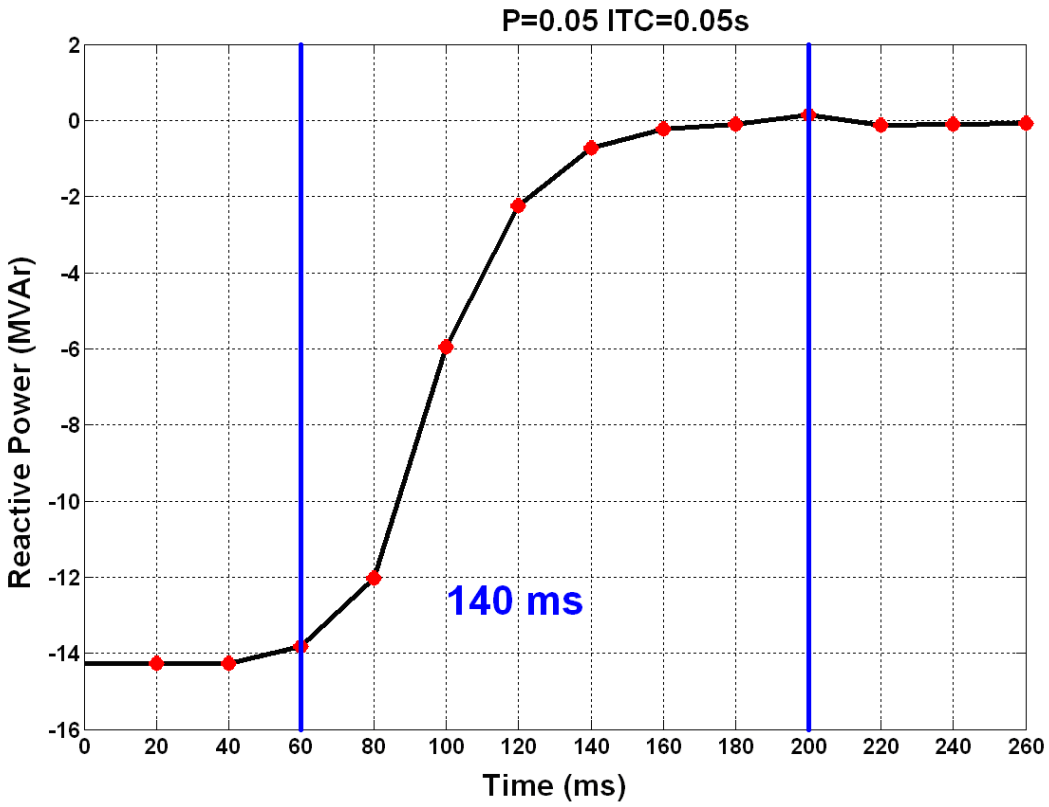
(e) PI+FF control (f) thyristor triggering

4.2 STEP RESPONSE

The step response of SVC is obtained by varying set value of reactive power demand from nominal value to zero. The following Figures 4.2-4.7 show the step responses of some PI parameters (proportional gain and integral time constant) from 14 MVAr capacitive to 0 MVAr. The response time is measured from the reactive power of incoming busbar. The set value is changed from 14 MVAr capacitive to 0 MVAr. For this transition, the TCR's reactive power changes from 200 kVAr to 14.2 kVAr that is a step change from 1.25% to 88.75% of reactive power capacity of TCR reactors. The response of the system is calculated for balanced operating condition and for these simulations the power supply and the transformer is used as supply.



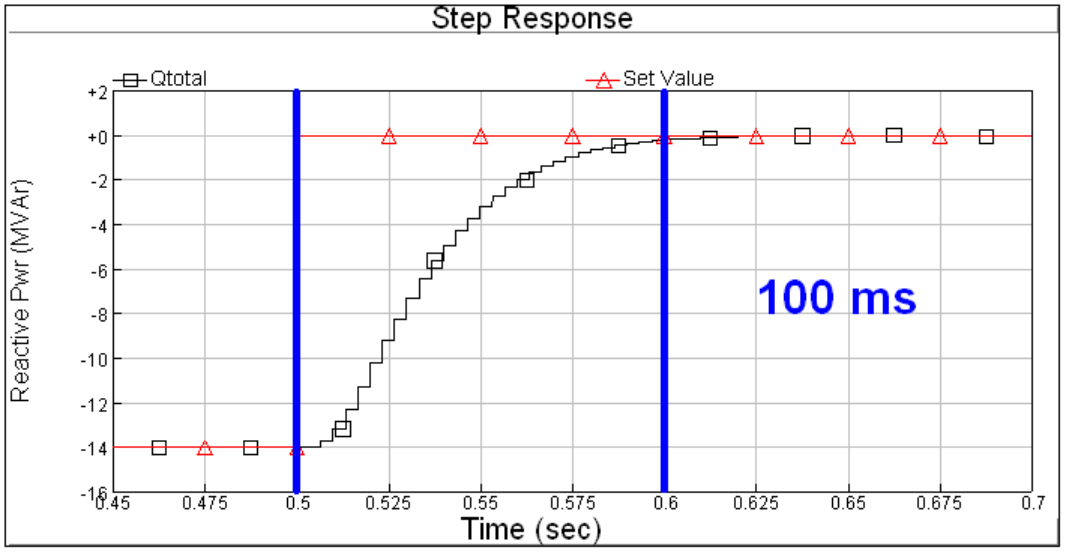
(a)



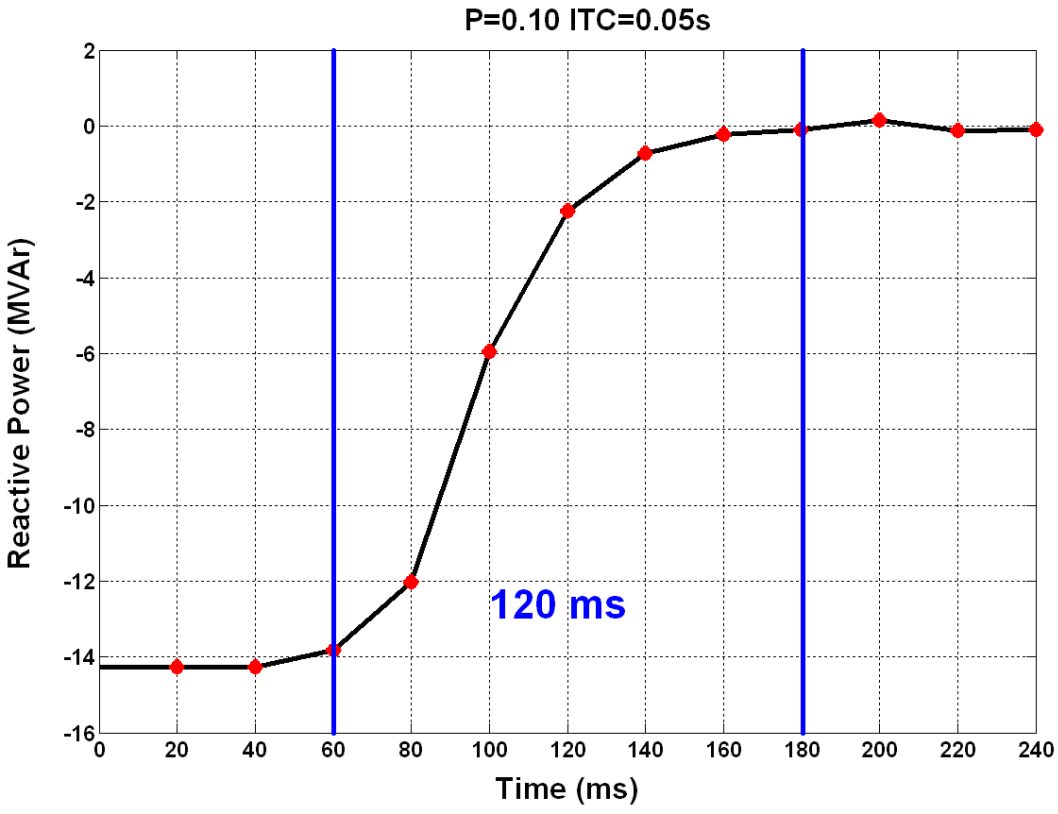
(b)

Figure 4.2. P=0.05, ITC=0.05 sec.

(a) Simulation (b) Field result



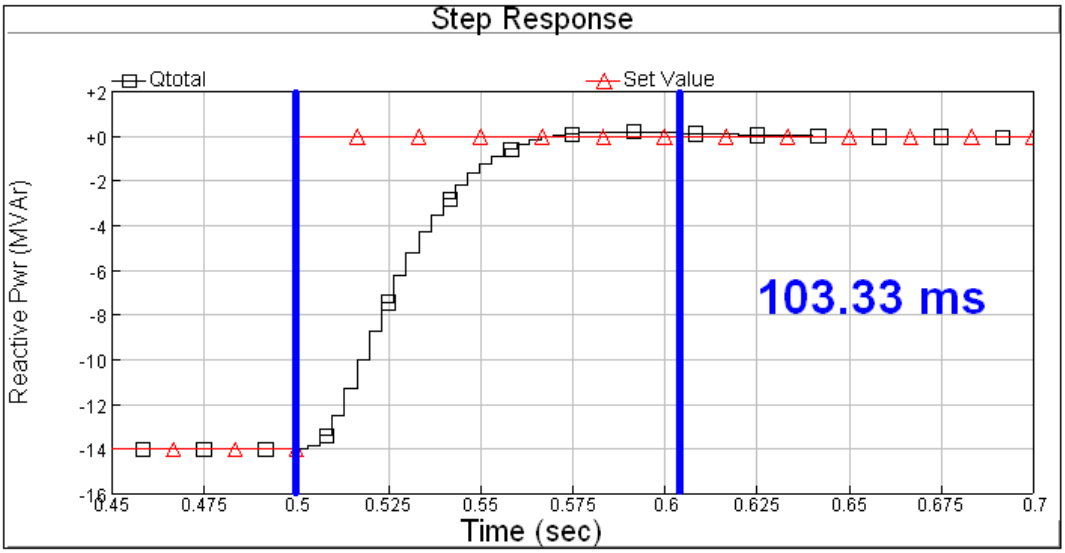
(a)



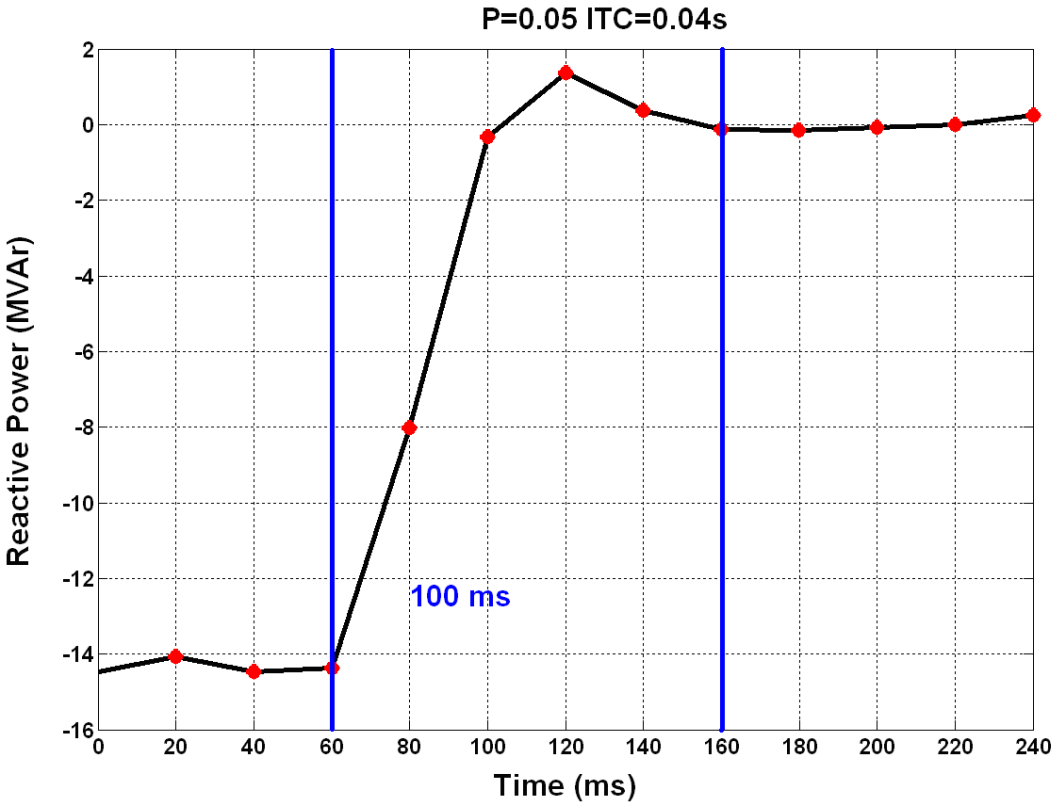
(b)

Figure 4.3. P=0.1, ITC=0.05 sec.

(a) Simulation (b) Field result



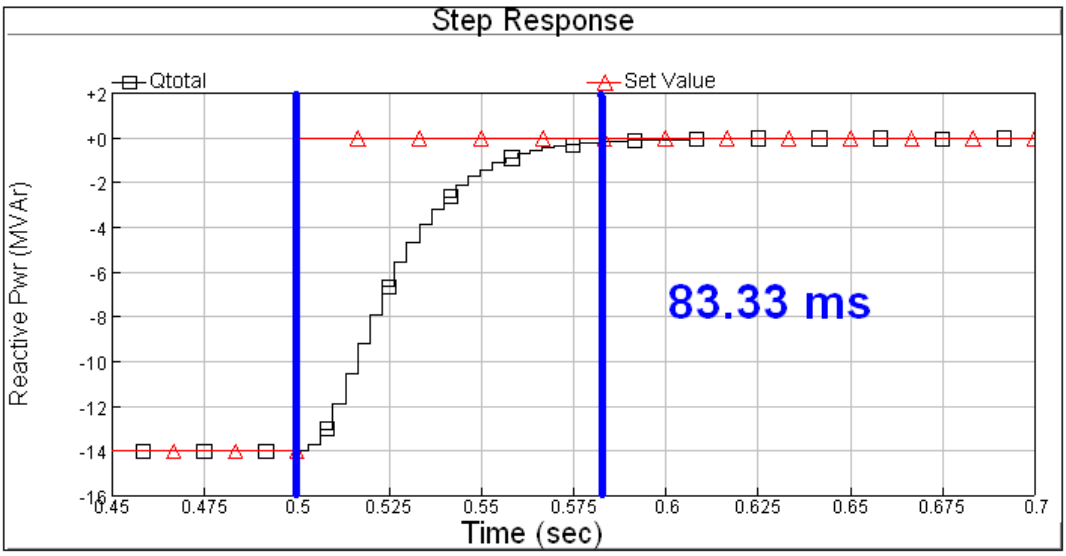
(a)



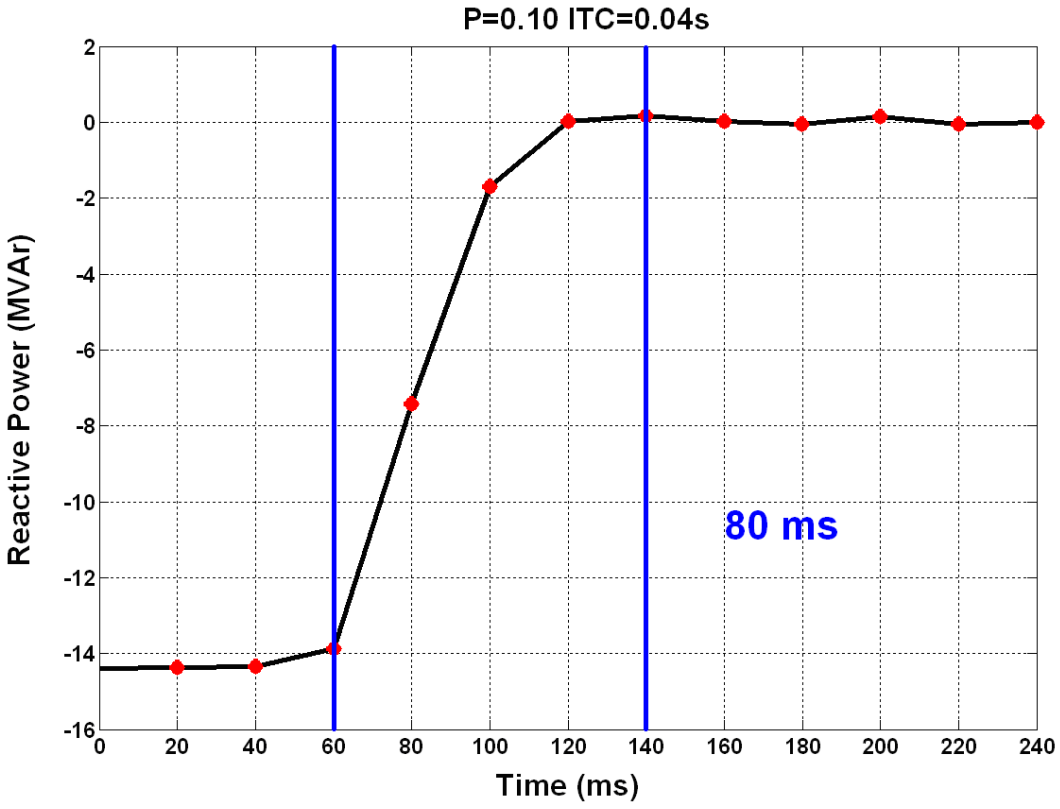
(b)

Figure 4.4. P=0.05, ITC=0.04 sec.

(a) Simulation (b) Field result



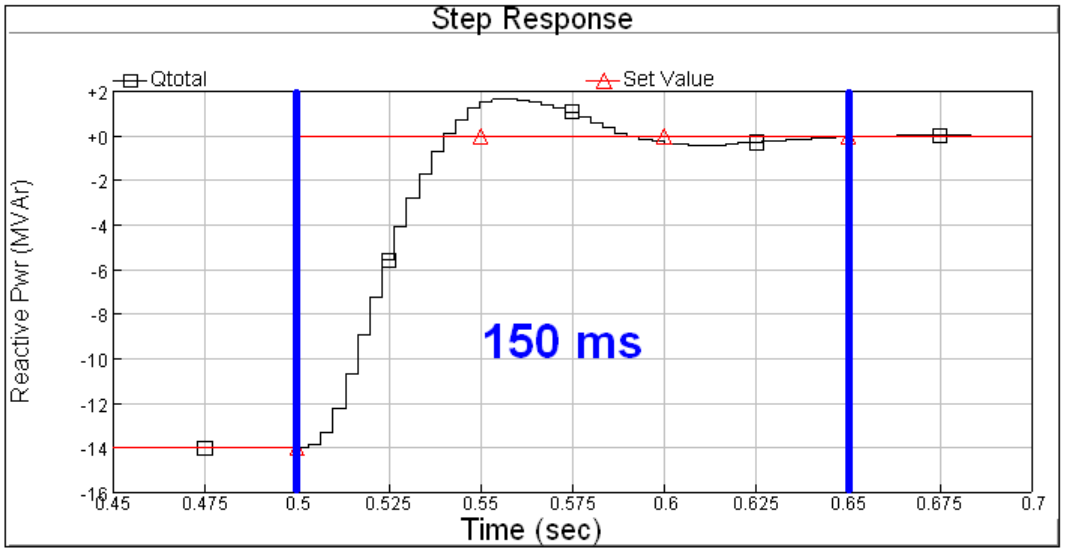
(a)



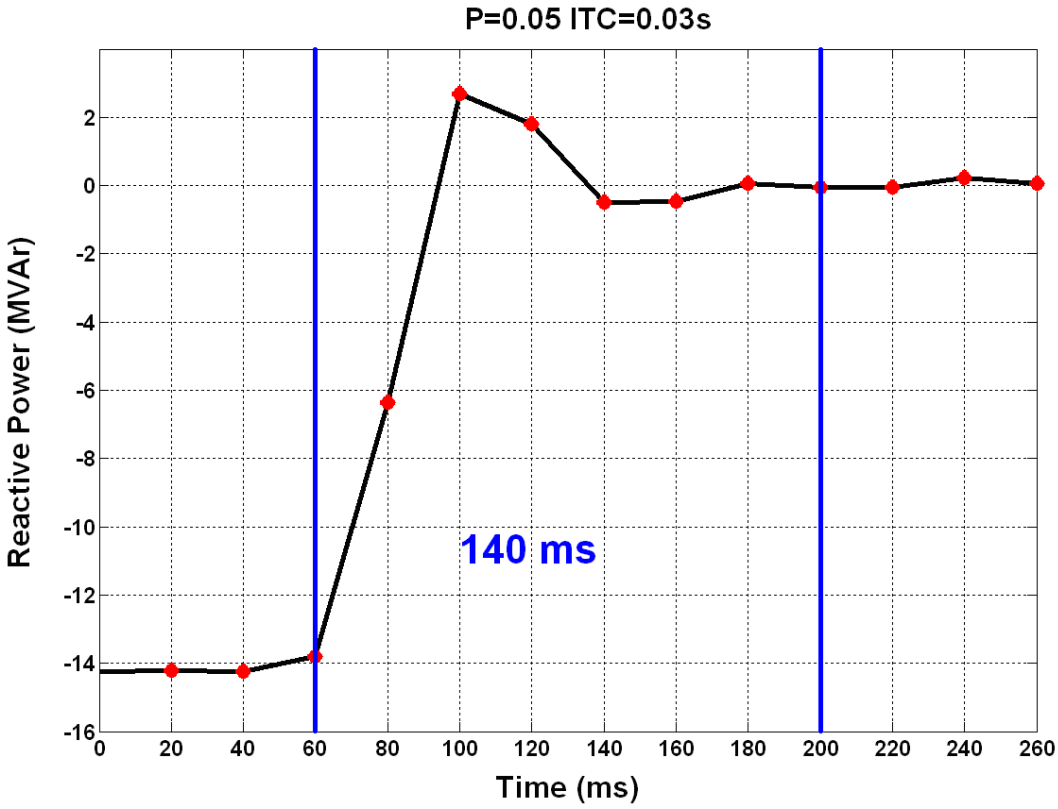
(b)

Figure 4.5. P=0.1, ITC=0.04 sec.

(a) Simulation (b) Field result



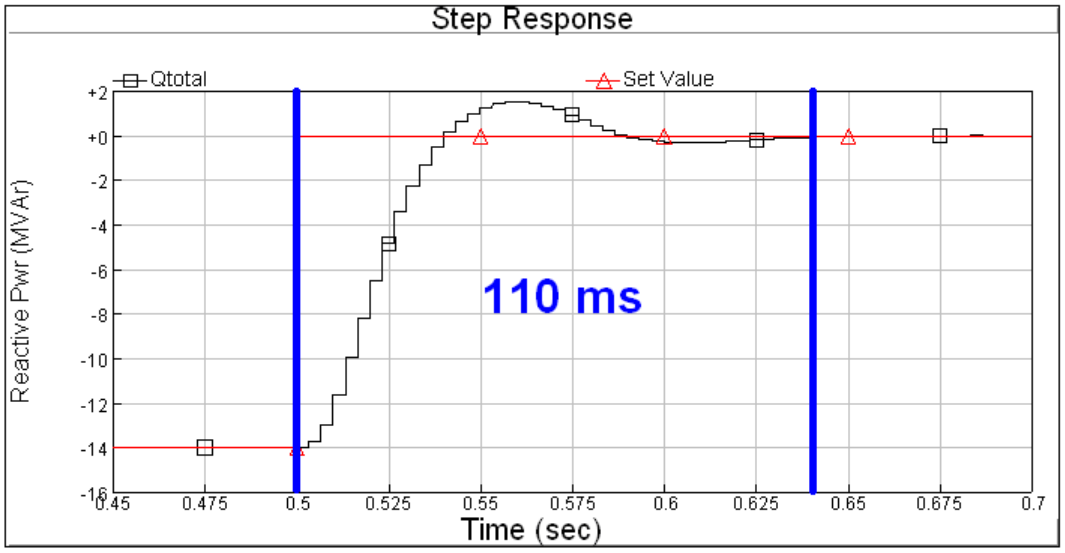
(a)



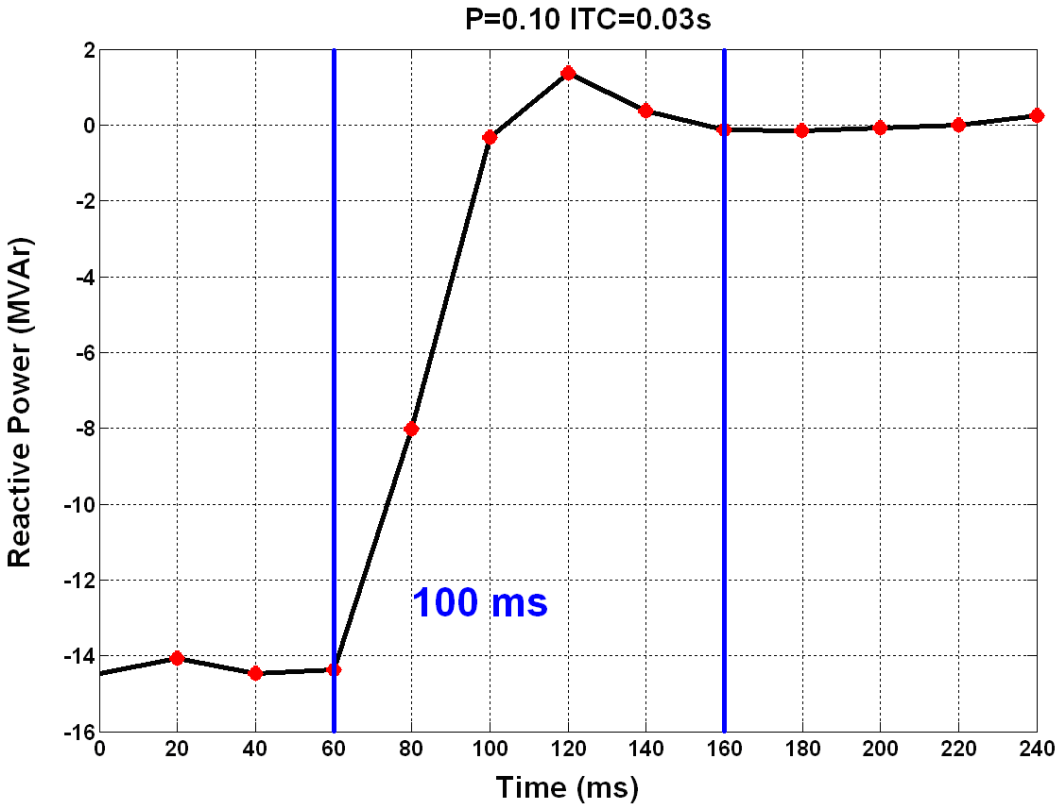
(b)

Figure 4.6. P=0.5, ITC=0.03 sec.

(a) Simulation (b) Field result



(a)



(b)

Figure 4.7. P=0.1, ITC=0.03 sec.

(a) Simulation (b) Field result

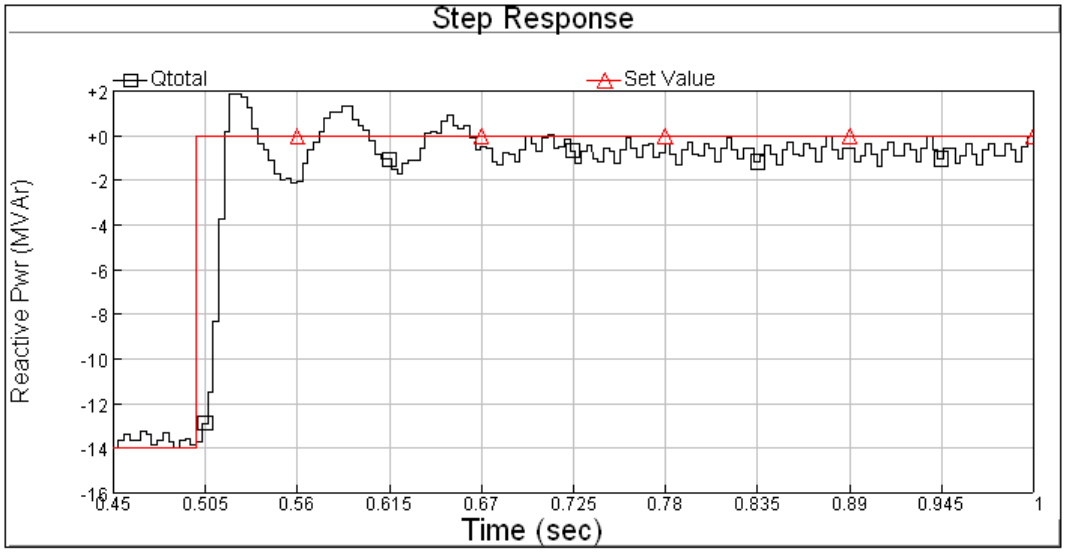


Figure 4.8. P=0.2, ITC=0.01 sec. (oscillatory)

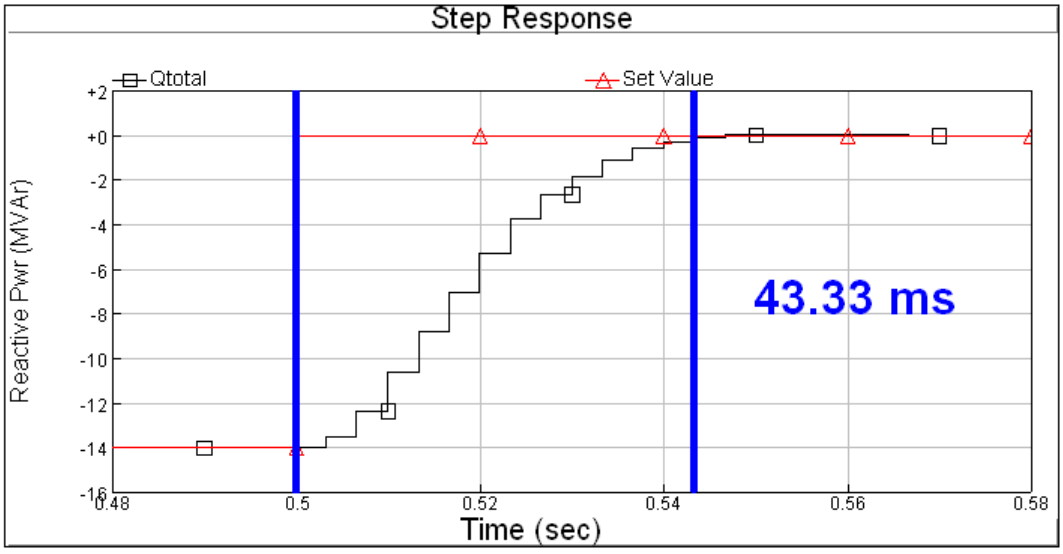
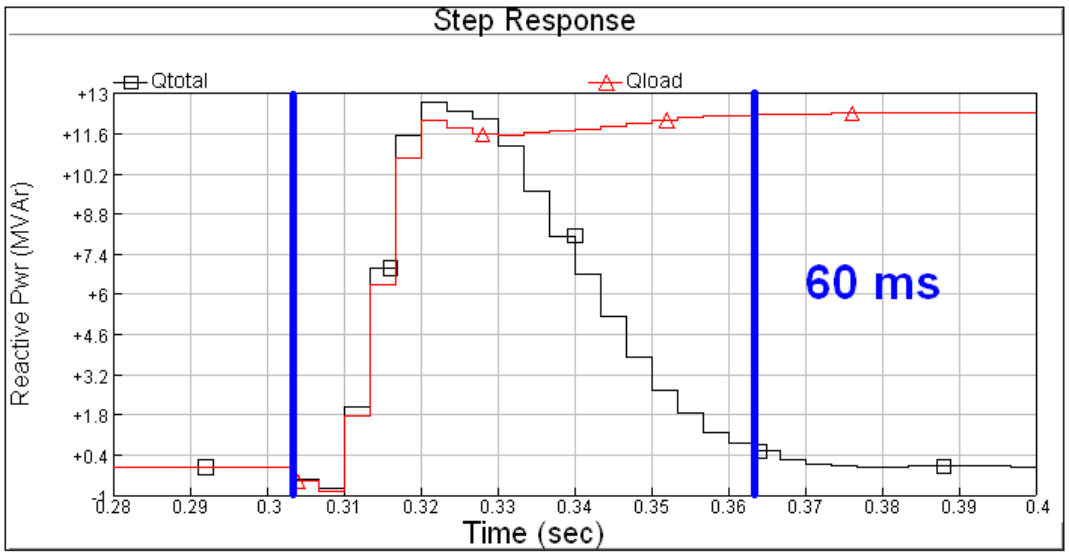


Figure 4.9. P=0.18, ITC=0.029 sec. (optimum response)

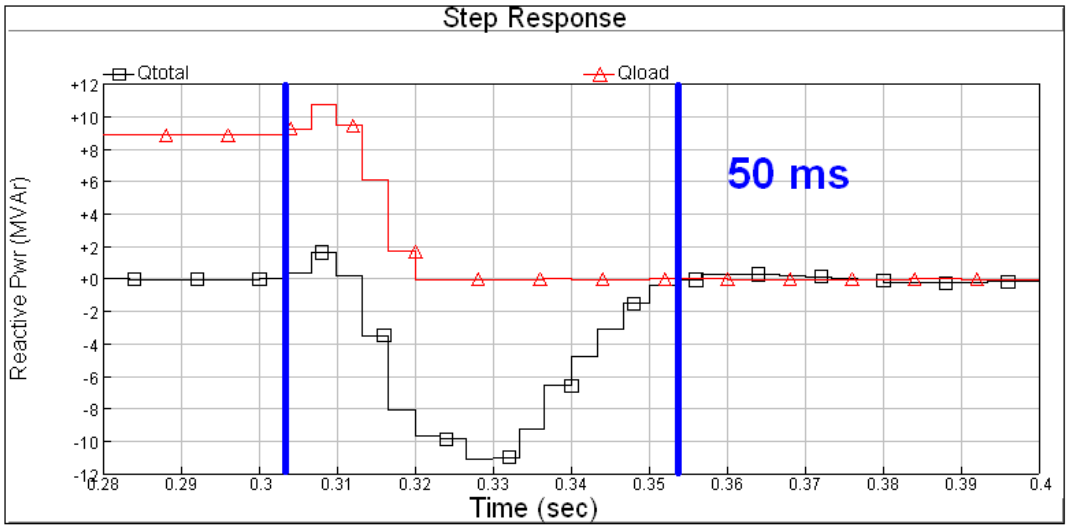
The step response time of TCR gets shorter when the integral gain is increased. The overshoot of the response increases when the proportional gain increases. If the relationship between reactive power error and response time is considered, when the response time of SVC decreases, the ability of compensating fast changing loads like arc or ladle furnaces increases. The best parameters are found as P=0.18 and ITC=0.029 sec. for fastest response of SVC.

4.3 SVC RESPONSE AGAINST LOAD VARIATIONS

For the simulation of SVC response against load variations a step change at the load is applied to the SVC system. The response of SVC is calculated for step changes from no load full load and from full load to no load. The full load is a 12 MW 0.8 pf lagging (10.16 + j7.6 Ω Y connected) balanced load and is energized and deenergized at the SVC bus. The results are shown in Figures 4.10 and 4.11.

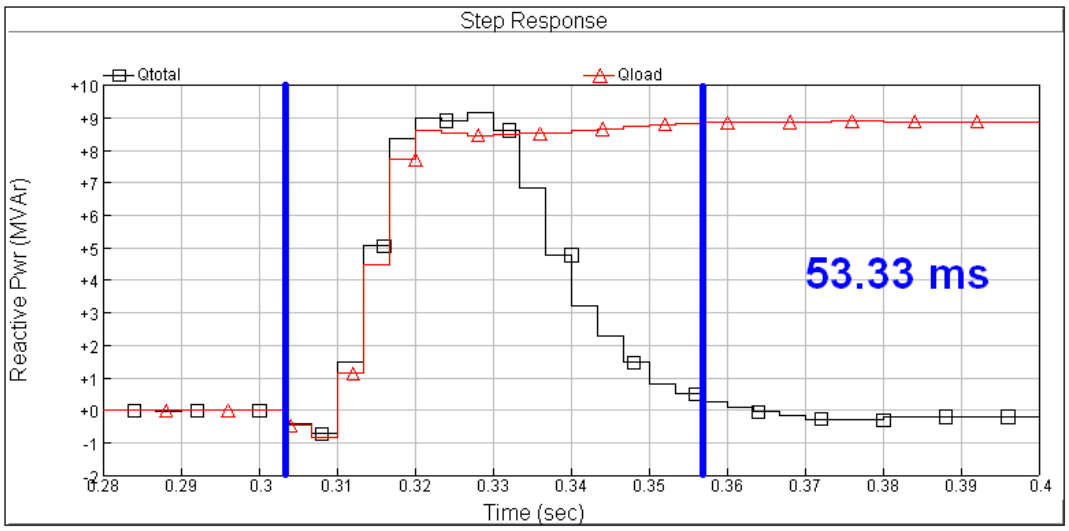


(a)

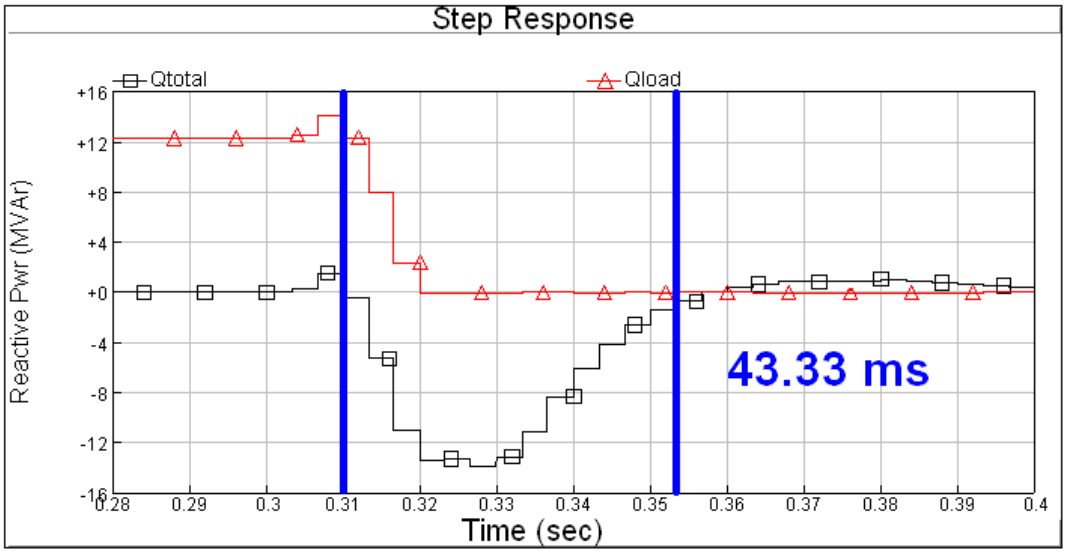


(b)

Figure 4.10. The response of SVC to load for FB
Load is (a) energized (b) deenergized



(a)



(b)

Figure 4.11. The response of SVC to load for FB+FF
Load is (a) energized (b) deenergized

It can be seen that the response time is 53.3 ms minimum for TCR from no load to full load. Response of SVC is delayed with 10 ms because of reactive power measurement of the control system. When the load is energized or deenergized, the response of the SVC comes with 10 ms delay. Furthermore, the response of SVC changes due to the transient current of the load. Since the load's current is not

constant, the response will oscillates and the response time may be longer than the set value change response time. The incoming bus' and load's reactive powers are as shown in figure 4.10 for feedback case. The reactive powers for hybrid control (feedback + feedforward) condition are shown in figure 4.11.

4.4 LOAD BALANCING

As mentioned in the SVC control part, if the negative sequence of the load current is compensated by the SVC, the incoming busbar currents becomes balanced.

For an unbalanced load, Y connected, with unbalanced active and reactive powers, the SVC compensation and load balancing operation the result is shown in Figures 4.12-4.15.

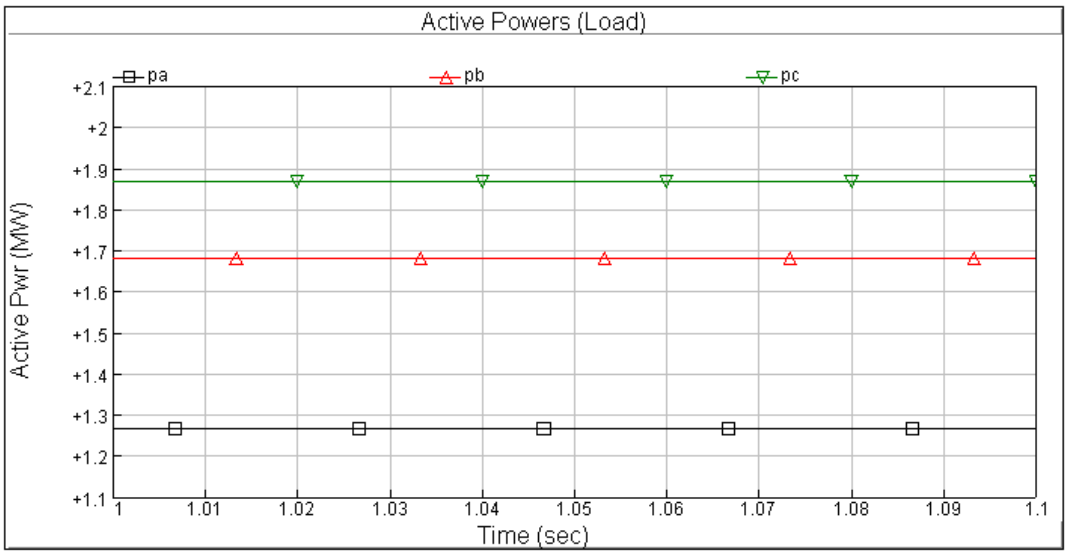


Figure 4.12. Unbalanced load's active powers (MW)

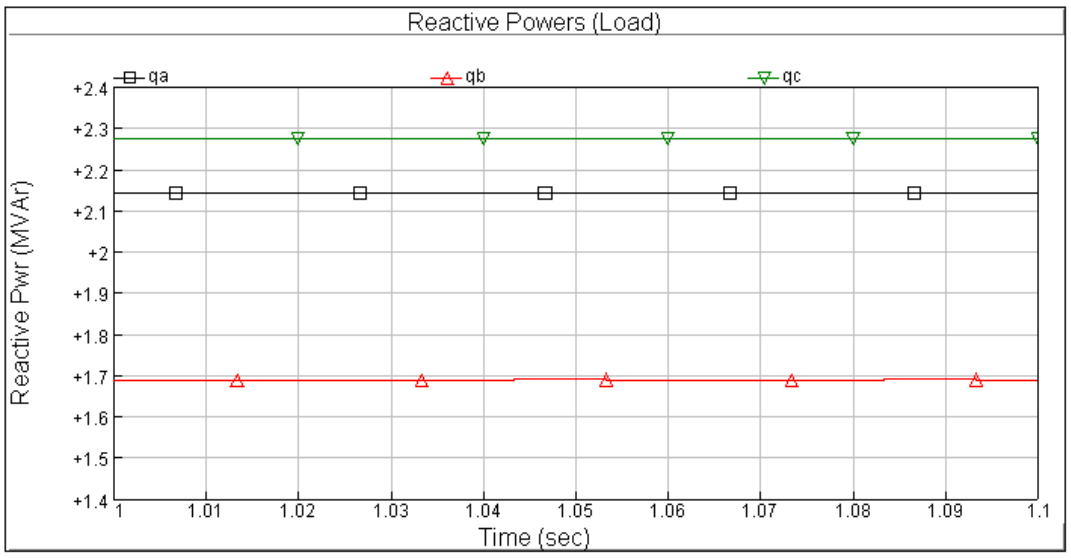


Figure 4.13. Unbalanced load's reactive powers (MVAr)

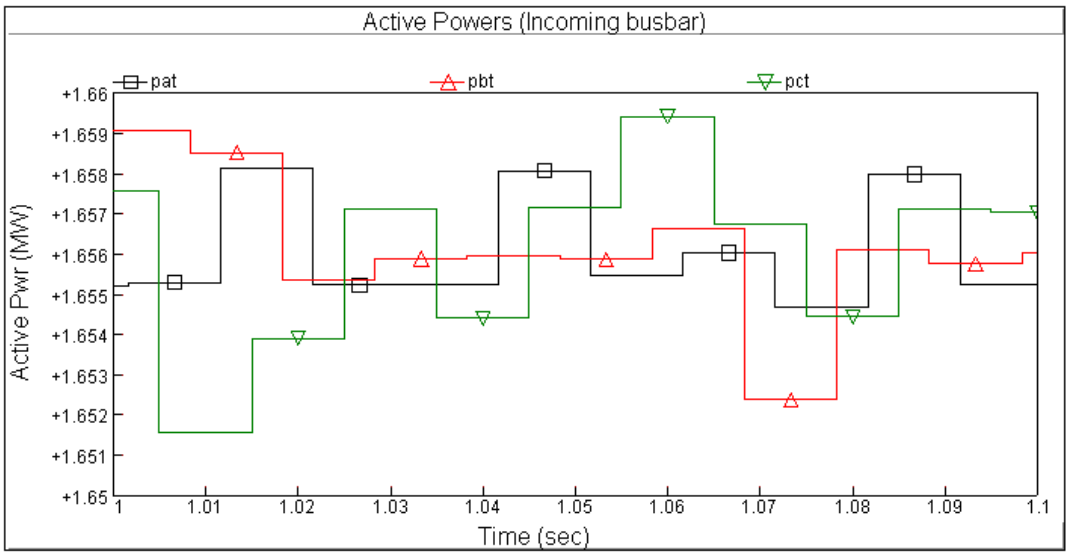


Figure 4.14. Balanced incoming busbar active powers

Note that, the variations in power take place in a narrow range (±1.5% of mean power).

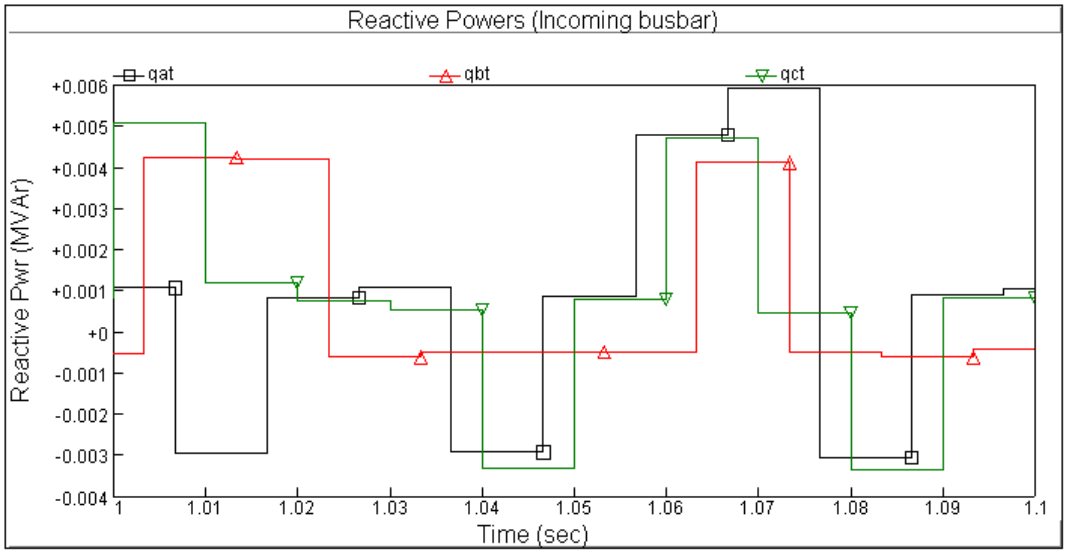


Figure 4.15. Compensated incoming busbar active powers

As a result of negative sequence compensation, both the reactive power and the negative sequence of load currents are compensated. Any unbalanced load can be reflected a balanced load to the source side of power system.

These simulations are carried out for partial loads. The simulated system can not balance full load satisfactorily because of lack enough installed TCR and HF capacities.

4.5 ADAPTIVE CONTROL

When the SVC operates for load balancing option selected, the installed capacity of the SVC should be enough for reactive power compensation and load balancing at the same time. When the required reactive power of compensator for compensating and load balancing for the load exceeds the installed capacity, neither compensation nor load balancing operations can be achieved successfully. Since the installed capacity may not be modified easily another solution for this problem should be implemented inside the controller.

The major job of SVC is reactive power compensation and the minor job is load balancing. When the phase powers of the load exceeds the limits of installed TCR and HF capacities both of the jobs cannot be achieved successfully at the same time. In such a case the major job, reactive power compensation, should be done. For this type of operation, only the positive sequence compensation part of the controller should operate while the negative sequence part is bypassed.

The system returns to normal operation when the load's powers are within the installed capacity limits. Adaptive control block diagram is shown in figure 4.16.

For this control strategy, the controller changes its operation mode from positive sequence + negative sequence compensation to positive sequence compensation and back to positive sequence + negative sequence compensation. The operation mode of controller varies due to power of the load and this *adaptation* is done by the controller itself. Since this adaptation is done by the controller automatically it is called *adaptive control*.

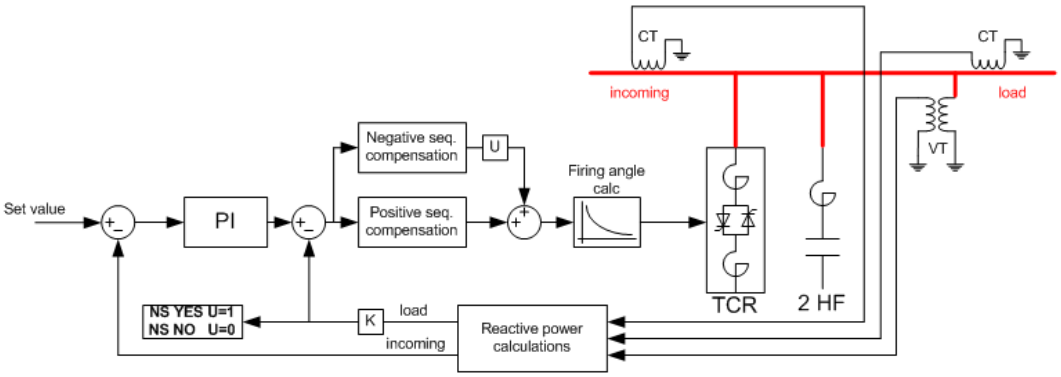


Figure 4.16. Adaptive control

An unbalanced load with powers 2MW + 5.9 MVAr inductive in phase A, 0.42 MW + 3.6 MVAr inductive in phase B , 3.3 MW + 3.3 MVAr inductive in phase C is energized during the SVC operation. The SVC controls the compensation capability and switches to *only positive sequence compensation mode* when it recognize that load balancing cannot be achieved.

The active and reactive powers of an unbalanced load are shown in Figures 4.17 and 4.18 respectively.

Figure 4.17. Active powers of the unbalanced load

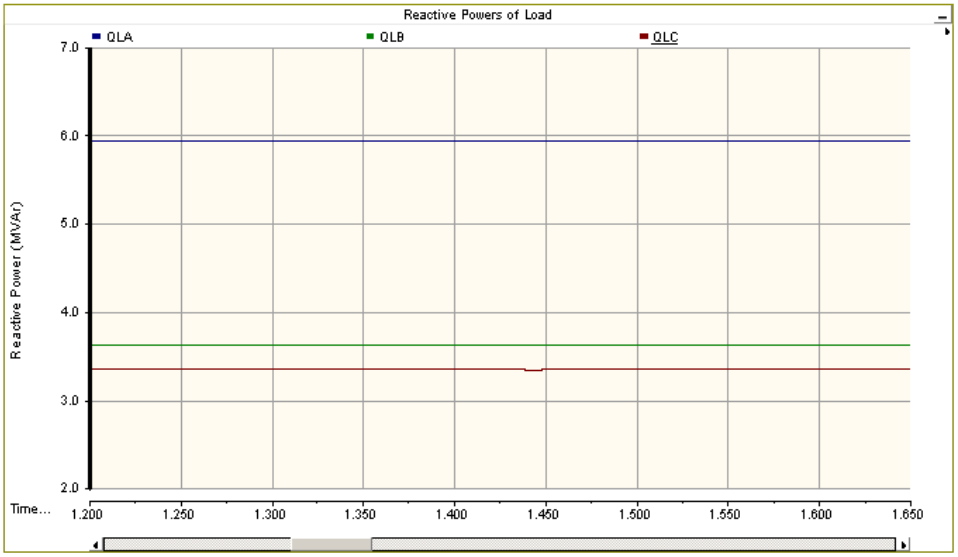


Figure 4.18. Reactive powers of the unbalanced load

The inductive reactive power of the load at phase A is 5.9 MVAr inductive which is higher than the maximum capacitive reactive power of phase of SVC. Because

of this problem the SVC cannot compensate total reactive power of the load and balance the active powers.

When this unbalanced load is connected to the busbar of SVC at steady state operation the resultant reactive powers are as follows.

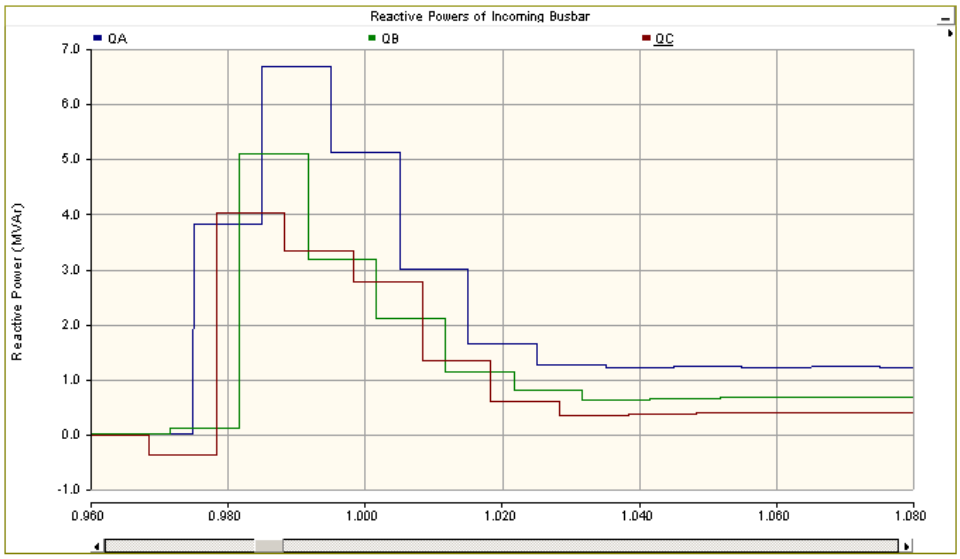


Figure 4.19. Reactive powers of the unbalanced load

In figure 4.18, the transient and the steady state reactive powers of the load can be seen. The resultant incoming busbar reactive powers are 1.21 MVAr inductive in phase A, 0.66 MVAr inductive in phase B and 0.39 MVAr inductive in phase C. Total reactive power of the load is 12.8 MVAr and this value is below the harmonic filter's reactive power, 14.2 MVAr. However total reactive power is under the limit value, the resultant error is 2.26 MVAr inductive. For such a case, the performance of SVC is 2.26 / 12.8 = 17.66% which is not acceptable.

After the load is energized, the SVC monitors its operation and decides whether to switch into only positive compensation mode.

The phase reactive powers are 1.63 MVAr inductive in phase A, 0.69 MVAr capacitive in phase B, 0.95 MVAr capacitive in phase C. Total reactive power is set to 0 about 40 ms and the SVC operation continues with only positive sequence compensation.

When the mode changes the resultant reactive power values are shown in Figures 4.20 and 4.21.

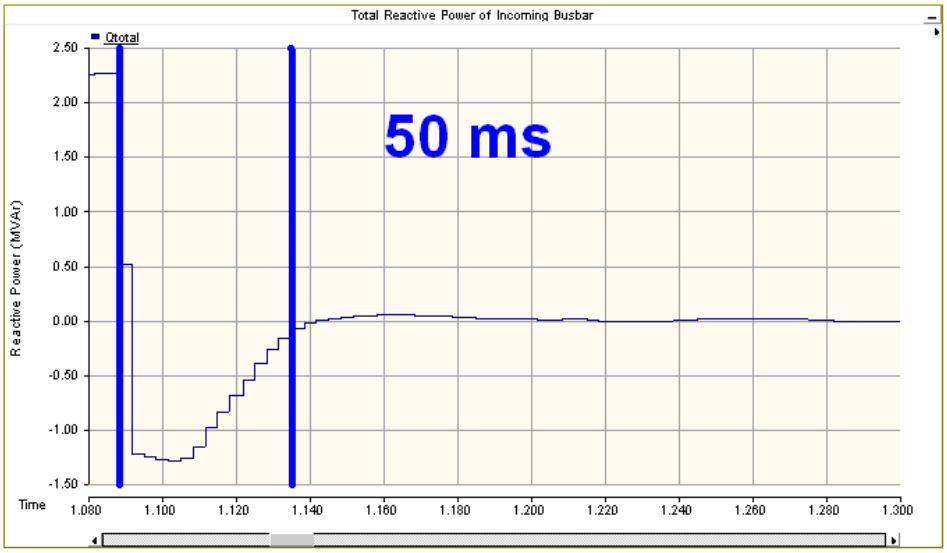


Figure 4.20. Total reactive power of incoming busbar for adaptive control

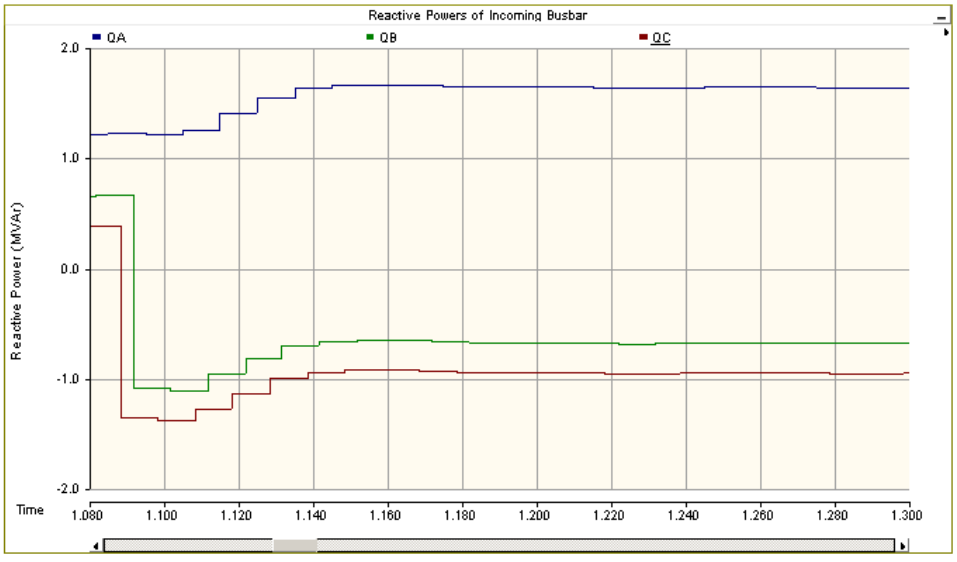


Figure 4.21. Phase reactive powers of incoming busbar for adaptive control

4.6 SUMMARY OF SIMULATION WORK RESULTS

When the simulation results are investigated, a basic PI controller's performance is adequate for SVC operation. For compensation of fast changing loads, the response of SVC can be improved by addition of feedforward control. The optimum PI parameters for the SVC is found as P=0.18 and ITC=0.029 s.

The control variable of the SVC is reactive powers of incoming busbar phases which are measured with a time step of 10 ms. Using small integral time constants for PI controller makes the response of SVC oscillative.

With use of an SVC, active power of an unbalanced load can be balanced at the incoming busbar. The capability of load balancing of SVC depends on installed capacity of TCR and HF and reactive power of the load. If operating in reactive power compensation + load balancing mode is unavailable then the control method of SVC should switch into only reactive power compensation mode to achieve at least one job instead failing in both two jobs. After the mode changes, it takes 50 ms for the system to settle down.

CHAPTER 5

FIELD TESTS

5.1 FEEDBACK CONTROL

The feedback control method (Figure 5.1) is a native closed loop PI controller that takes incoming busbar reactive powers as control variable and tries to hold incoming busbar's reactive power at set value. The block diagram of feedback control is show in figure 5.1.

The performance of feedback control can be seen in Figures 5.2 and 5.3. The SVC tries to keep the reactive power of the compensated load at zero and hence the reactive power oscillations decrease at the incoming busbar.

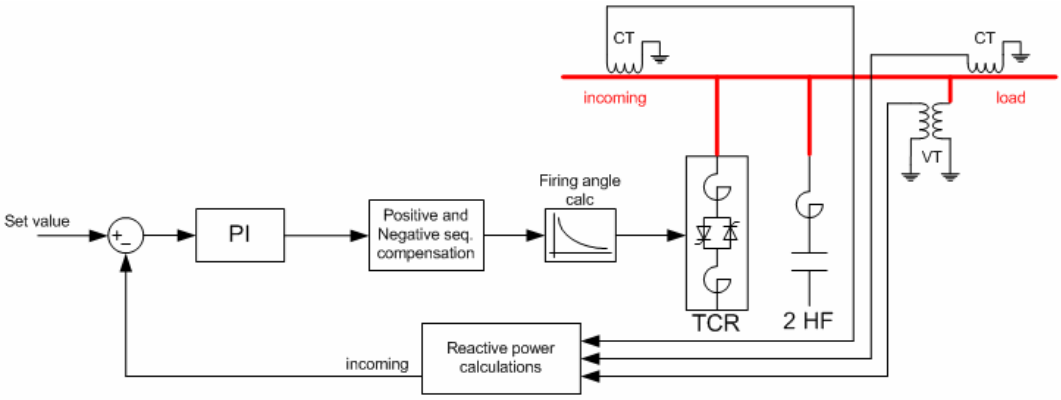


Figure 5.1. Feedback control

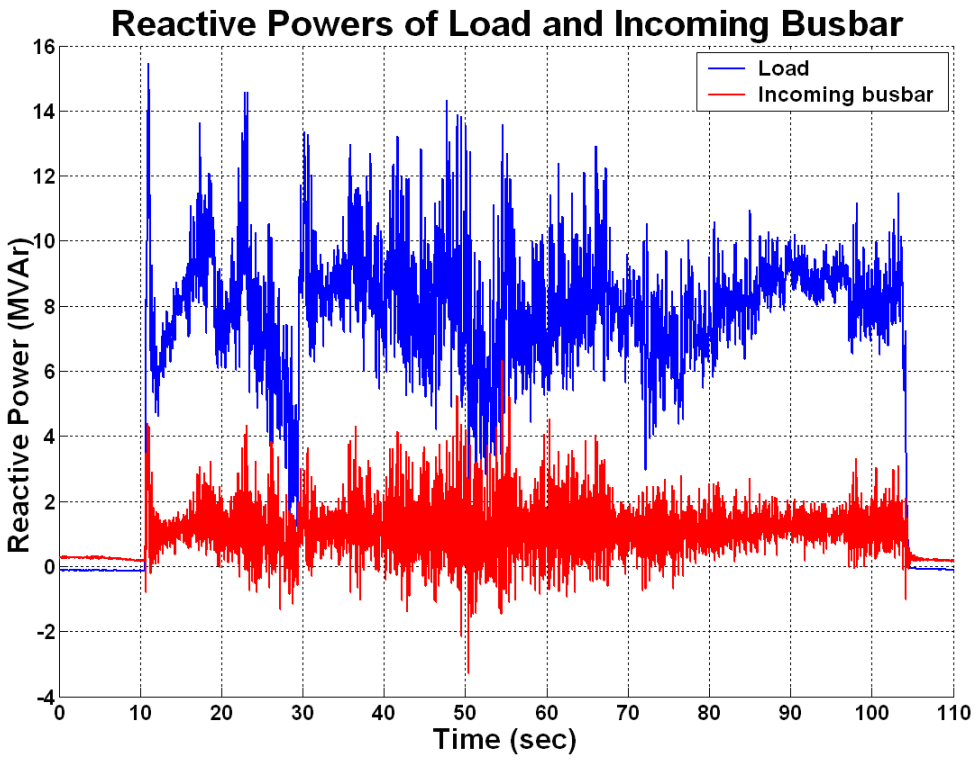


Figure 5.2. Reactive powers for feedback control

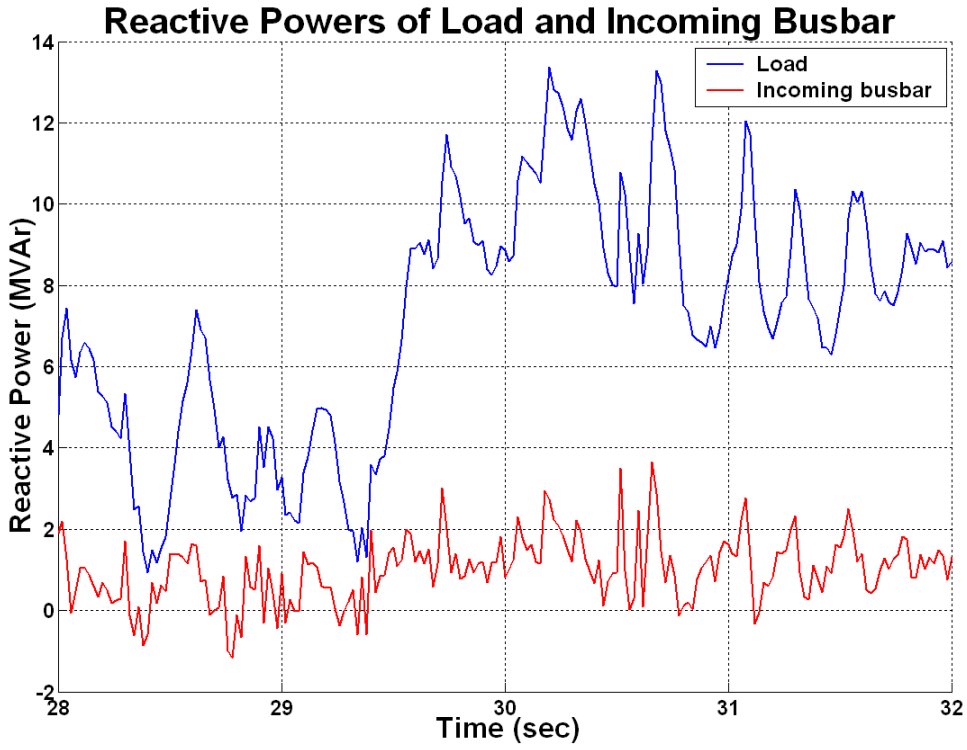


Figure 5.3. Reactive powers for feedback control (zoomed)

When there is a large change at the load's reactive power, PI regulator's output changes and settles down with a time delay. From the figures it is inferred that transient response of feedback is slower for rapidly changing loads as ladle furnaces.

5.2 FEEDFORWARD CONTROL

When the load's reactive power is calculated and the thyristors' firing angles are calculated with load's and filter's reactive powers, the resultant reactive power at the incoming bus is expected to be zero VAr. With this method, the reactive power of the capacitive element, harmonic filter, is assumed to be constant and the TCR injects the difference of reactive powers of the filter and the load. Feedforward method (Figure 5.4) is inherently stable. The error of the response comes from the variation of reactive powers of capacitive elements due to the voltage changes.

Load balancing can also be done in feedforward control. For the control algorithm, the measured phase reactive powers are subtracted from the harmonic filter's reactive power. From the resultant reactive powers, the firing angles for compensation and load balancing are calculated. The following figure shows block diagram of feedforward control. K constant for feedforward loop is 1 when pure feedforward control is used. The results are shown in Figures 5.6-5.7.

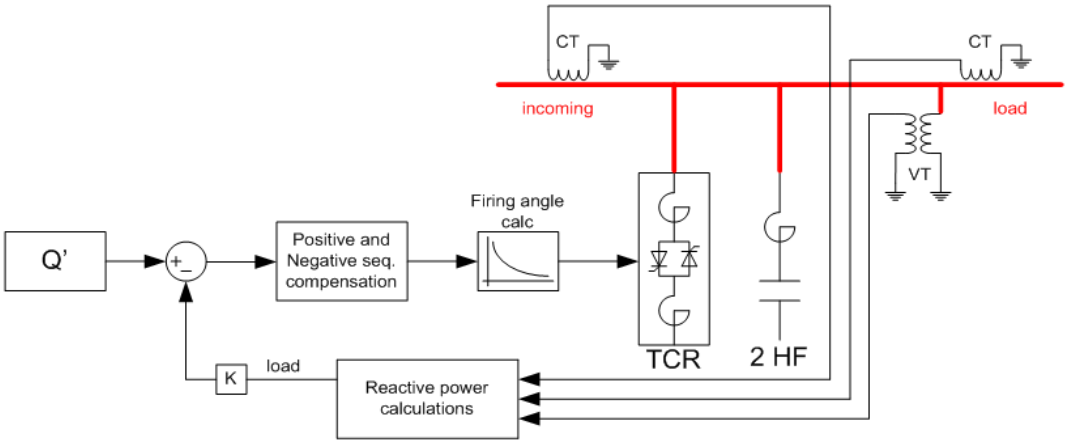


Figure 5.4. Feedforward control

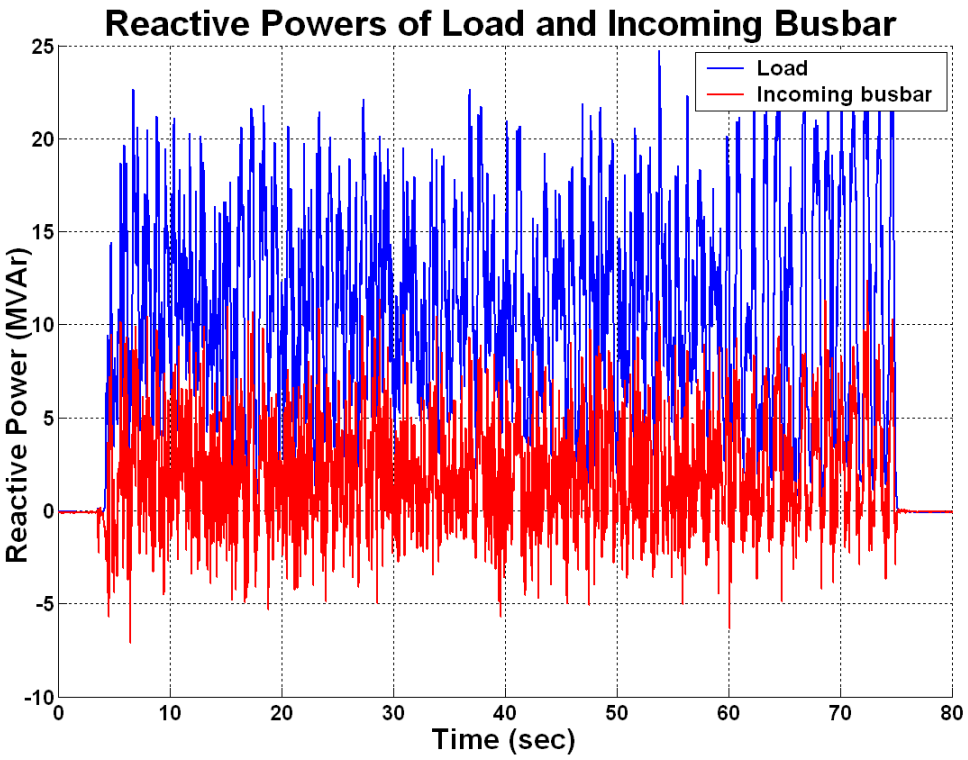


Figure 5.5. Reactive powers for feedforward control

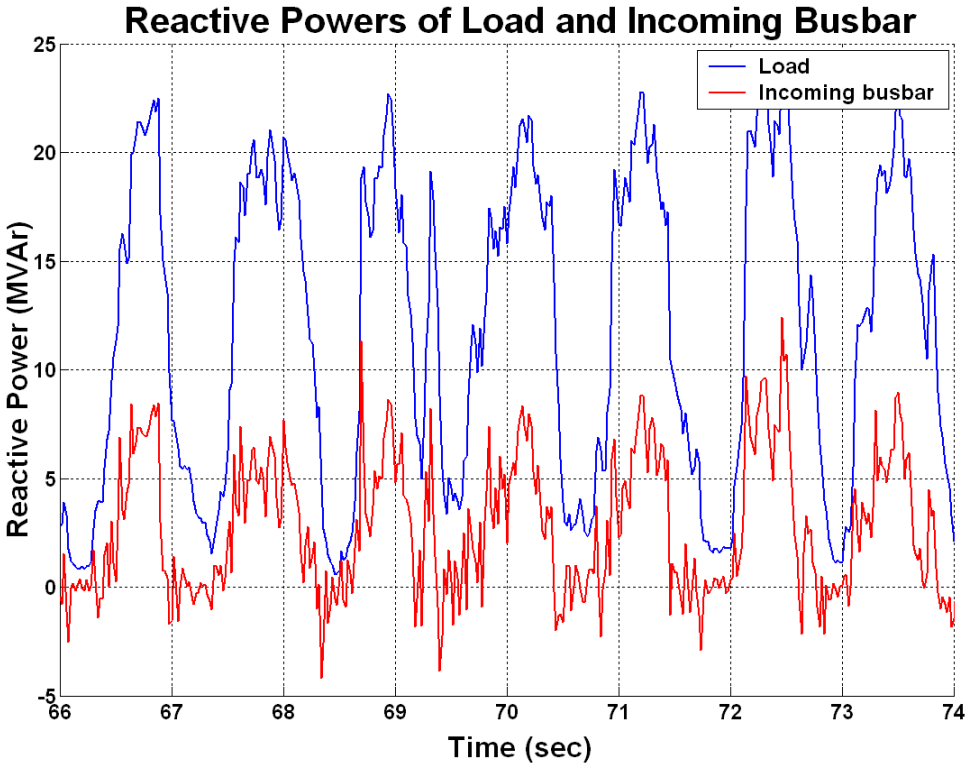


Figure 5.6. Reactive powers for feedforward control (zoomed)

The control system holds incoming reactive power at low level, near zero when the load's reactive power is changing slowly and within the installed compensation capacity. When there is a large change at the load's reactive power, the resultant incoming reactive power cannot be compensated quickly. The response of SVC is well when the load's reactive power is under filter's reactive power. When the load's reactive power exceeds the installed capacitive reactive power, the system increases firing angles to maximum to give minimum inductive reactive power.

5.3 HYBRID CONTROL

The rapid response property of feedforward is combined with the zero error at steady state compensation capability of feedback. The ratios of FB and FF depend on the rate of change of load's reactive power. The following figures show the response of control system with hybrid control.

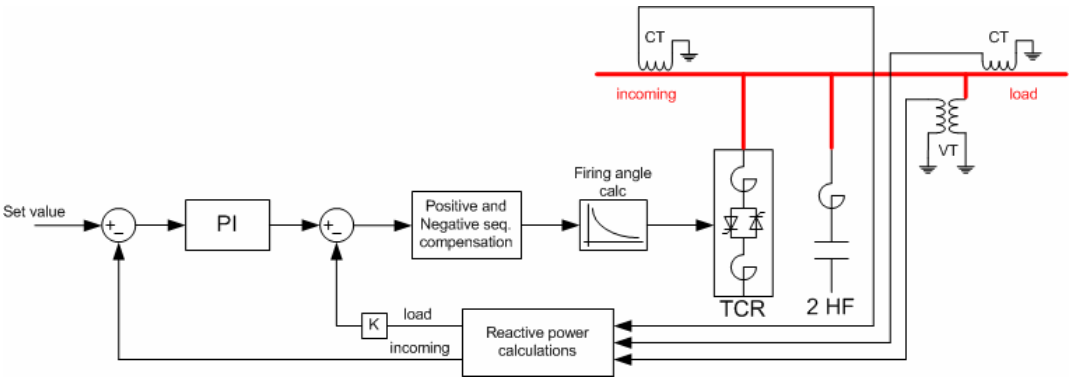


Figure 5.7. Hybrid (FB+FF) control

When the resultant incoming busbar reactive power is examined, it can be seen that the best control technique is the hybrid control. The small error capability of feedback controller and fast response characteristic of feedforward controller is combined and the resultant reactive power is the smallest one as found in the simulation chapter.

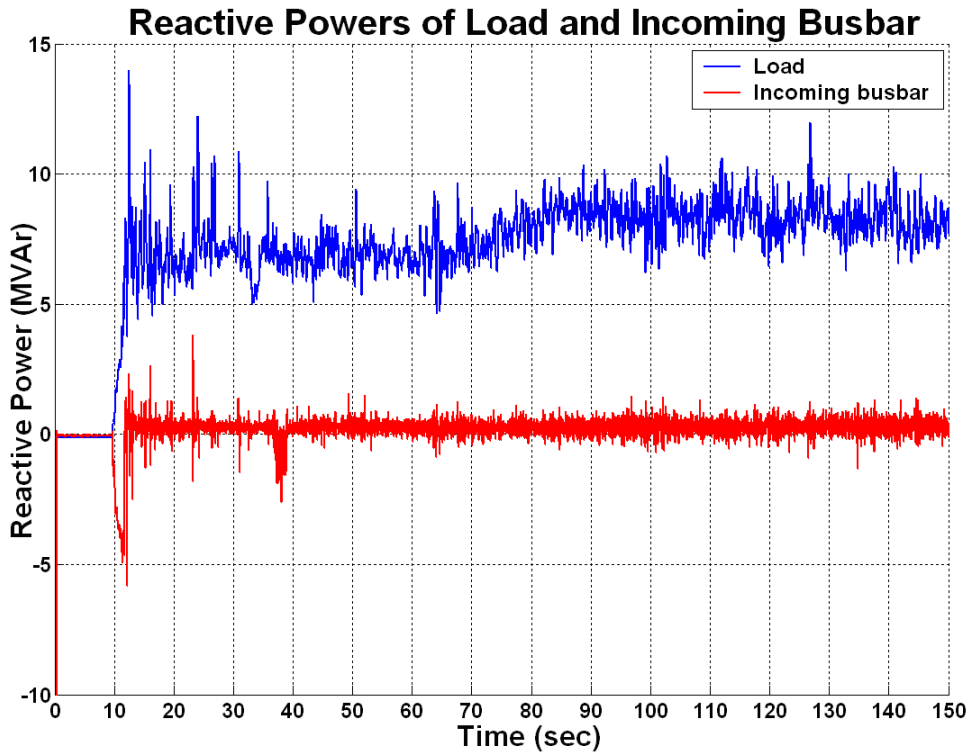


Figure 5.8. Reactive powers for hybrid control

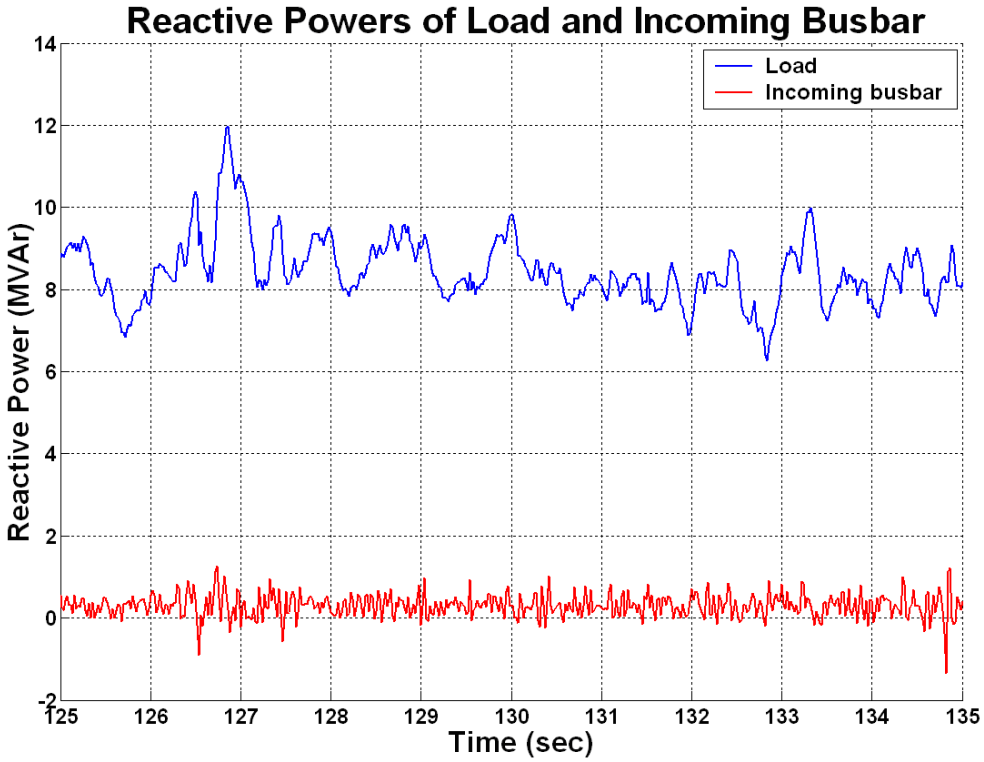


Figure 5.9. Reactive powers for hybrid control (zoomed)

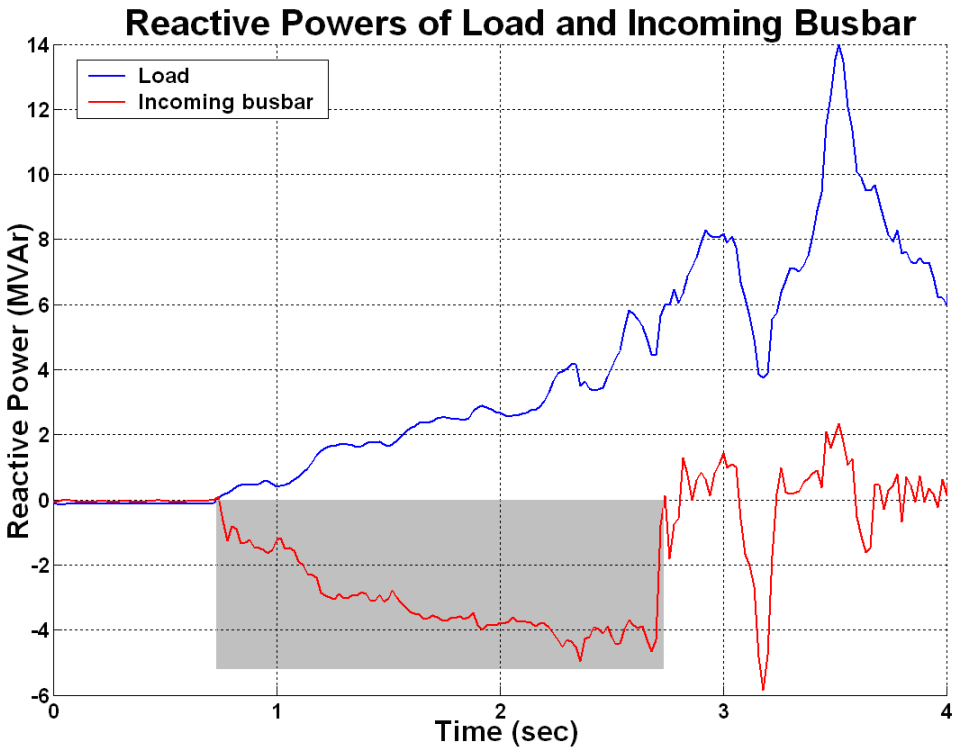


Figure 5.10. Malfunction of SVC (shaded area)

The control algorithm contains load balancing option and the control system has been built also for this purpose. When the active and reactive power consumptions of the load in each phase are not within the limits of SVC compensation and load balancing capability, the calculated firing angles cannot give the inverse of total reactive power of the load. For such a case, the resultant incoming busbar reactive power is not the set value (0 for figure 5.10).

At such cases, the controller should run only for reactive power compensation (positive sequence compensation). Since the first goal is reactive power compensation and reactive power measurement for performance test is done for 3 phase total reactive power, changing the control strategy for this case is reasonable.

By considering the design procedure, after the installation of system, if such a case is met, then modifying the control strategy is required. For this purpose the adaptive control technique can be used instead of capacity increment.

5.4 SUMMARY

The ladle furnace has a rapidly changing reactive power characteristic and the compensator should response the exact reactive power immediately. The feedback part of the controller makes reactive power error small enough for the limits but the transient response is slow. Since the ladle furnace has a fast varying reactive power characteristic, the step response of the regulator to load changes should be faster. This fast acting characteristic is acquired by the feedforward part. When there is a change at the load's reactive power the compensator responses to the load change immediately and regulate the remaining error by the feedback regulator.

Load current is measured with current harmonics. For fast changing loads, the power measurement must be as fast as rate of change of load's power. For this purpose, in reactive power measurements, load's currents are not filtered to avoid the delay of filtering stage which slows SVC response. When the effect and portion of feedforward control technique is considered, increasing the feedforward constant K improves the SVC response, but when the harmonic error of power measurement for load side is considered, increasing K may also increase the system's error.

If the reactive power measurement errors are decreased, the feedforward part's contribution to the control system can be increased that increases reactive power compensation quality. Instead of analog filtering with time delay, a digital filtering and reactive power measurement technique based on a DSP improves the system's performance. For future works, when harder load cases like arc furnaces and more complex control options like reactive power management with voltage regulation are considered, a DSP module integration is required.

CHAPTER 6

CONCLUSION

5.1 CONCLUSION

In this research work a digital controller has been designed and implemented for TCR based SVCs. The digital controller employs a commercially available device which is composed of NI cRIO 9004 RT Controller and NI cRIO 9104 Reconfigurable Chassis. The control system computes bıth reactive power consumption of the load before compensation and reactive power drawn from or injected into supply after compensation. Reactive power calculation technique is based on averaging the integral of the product of required current and voltage signals over a half-cycle. Reactive powers, error signals and control signal are generated independently one set for each phase. The resulting controller is suitable for unbalanced industrial loads with rapid variations in their reactive power demands such as arc and ladle furnaces, rolling mill drives, etc.

The digital control system has been designed by using EMTDC/PSCAD simulations of the overall system including SVC, digital controller, nonlinear load and the power system to which SVC is connected. In the design several control strategies have been exercised such as feedback control, feedforward control, hybrid (feedback + feedforward) control and adaptive control. These results show that;

1. Feedback control strategy can provide us a fast response (in the range from 43.33 ms to 60 ms) against step variations in reactive power demand of loads.
2. Optimum performance for feedback control strategy has been obtained for P and ITC parameters for 0.18 and 0.029 s respectively.
3. Feedback controller gives theoretically zero steady state error for its optimized settings.
4. Faster response can be obtained at the expense of periodic reactive power oscillations at the supply side in the steady state.
5. Feedforward controller yields shorter settling time than feedback controller at the expense of considerable steady state error.
6. The hybrid controller (a dominant feedback + weak feedforward gain) gives the best results almost all operating conditions.
7. In the cases where the installed SVC capacity is insufficient for perfect reactive power compensation and perfect load balancing adaptive control strategy gives better result then other control strategies exercised and mentioned above.

An SVC system (16 MVAr TCR + 14.2 MVAr 2^{nd} harmonic filter) including the digital controller described in this thesis has been designed, manufactured and applied to Erdemir Iron&Steel Inc. to solve reactive power compensation and load balancing problems of two ladle furnaces. Real-time data have been collected o the prototype system in the field. By this way field performance of feedback, feedforward and hybrid control strategies have been investigated for actual load variation during longer time periods. These results shoe that;

1. Field performance of the digital controller is in good agreement with theoretical results.
2. The digital controller described in this thesis can keep inductive reactive energy / active energy and capacitive reactive energy / active energy ratios on monthly bases at values less then 4.47%, 1.35% respectively. This performance is quite satisfactory because the penalty

limits are respectively 5% and 5% percent of monthly active energy according current regulator.

These deviations from ideal full compensation state (zero MVAr demand the supply after compensation for both inductive and capacitive regions) may be attributed to the facts that the SVC has a limited installed capacity and SVC responds against rapid fluctuations in the load always with a delay. For better performance against rapid load fluctuations a faster response needed. One way of achieving this is to measure reactive powers in a time shorter then 10 ms. For this purpose instantaneous reactive power theory may be used as a further study this may save 10 ms at most in response time of SVC.

REFERENCES

[1] L. Gyugyi, R. A. Otto, and T. H. Putman, "Principles and Application of Static Thyristor-Controlled Shunt Compensators," Trans. IEEE, Power Appar. Syst. 97, 1935-1945. (September/October 1978)

[2] T. J. E. Miller, "Reactive Power Control in Electric Systems" 1982

[3] N. Köse, B. Mutluer, M. Ermis, et. al., "Two-folded Implementation of a 12-Pulse TCR with Dissimiliar Transformers for a Ladle Furnace: Reactive Power Compensation and Power System Redundancy", Industry Applications Conference, 2004. 39th IAS Annual Meeting, Conference Record of the 2004 IEEE Vol. 1, 3-7, October 2004.

[4] IEEE Std 519-1992, IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems.

[5] Bilgin, Faruk H, "Design and Implementation of a current Source Converter Based STATCOM for Reactive Power Compensation", 2007

[6] Ö. Salor, B. Gültekin, S.Buhan, et. al., "Electrical Power Quality of Iron and Steel Industry in Turkey", IEEE IAS 2007 Annual Meeting (Accepted).

[7] J. Arrillaga, D. A. Bradley, P. S. Bodger, "Power system harmonics" 1985

[8] J.M. Cano, G.A. Orcajo, M.F. Cabanas, M.G. Melero," TCR Based Reactive Power Compensator With Low Harmonıc Injection", EPE'99 Lausanne

[9] Garcia-Cerrada, A.; Garcia-Gonzalez, P.; Collantes, R.; Gomez, T.; Anzola, J.; "Comparison of thyristor-controlled reactors and voltage-source inverters for compensation of flicker caused by arc furnaces", Power Delivery, IEEE Transactions on Volume 15, Issue 4, Oct. 2000 Page(s):1225 – 1231

[10] A. L. Freedman, R. A. Lees, “Real-time Computer Systems”, 1977

[11] Qing Li ; with Caroline Yao, “Real-Time concepts For Embedded Systems”, 2003

[12] Alexander Kusko, Marc T. Thompson, “Power Quality In Electrical Systems”, 2007

[13] Richard J. Vaccaro, “Digital Control : a State-Space Approach”, 1995

[14] Phillips, Charles L., “Digital control system Analysis and Design”, 1995

[15] Ai, Q.; Gu, D.; Chen, C.; "New Load Modeling Approaches Based on Field Tests for Fast Transient Stability Calculations", Power Systems, IEEE Transactions on Volume 21, Issue 4, Nov. 2006 Page(s):1864 – 1873

[16] Renjie Ding; Jun Zhang; Yong Min; Zhiqiang Shi; Haitao Song; Yuwei Zhao; "Design and implementation of a new kind of FC-TCR controller based on multiprocessor and digital phase shift triggers" ,Advances in Power System Control, Operation and Management, 1993. APSCOM-93., 2nd International Conference on 7-10 Dec 1993 Page(s):142 - 146 vol.1

[17] Gutierrez, J.; Montano, J.C.; Castilla, M.; Lopez, A.; "Power-quality improvement in reactive power control using FC-TCR circuits", IECON 02 [Industrial Electronics Society, IEEE 2002 28th Annual Conference of the] Volume 2, 5-8 Nov. 2002 Page(s):880 - 885 vol.2

[18] Hugelschafer, L.; Vempel, G.; "Digital Firing Control For Line-commutated High Power Converters"; AC and DC Power Transmission, Sixth International Conference on (Conf. Publ. No. 423)29 Apr-3 May 1996 Page(s):157 – 162

[19] McKenna, S.M.; Hamai, D.; Kezunovic, M.; Galijasevic, Z.; "The Choice of a Simulation Time Step In The Real-Time Simulator Applications", Digital Power System Simulators, 1995, ICDS '95., First International Conference on 5-7 Apr 1995 Page(s):75

[20] Montano, J.-C.; Gutierrez, B.J.; Lopez, O.A.; Castilla, I.M.; "Effects of Voltage-Waveform Distortion in TCR-type compensators", IEEE Transactions on Industrial Electronics, Vol. 40, No. 3, June 1993 Page(s):373-383

[21] Farias, V.J.; De Oliveira, J.C.; Silveira, J.C.P.; Miskulin, M.S.; "Performance analysis of static TCR compensators for load balancing under asymmetrical voltages", Transmission and Distribution Conference, 1991., Proceedings of the 1991 IEEE Power Engineering Society 22-27 Sept. 1991 Page(s):953 – 958

[22] IEEE Guide for Static VAr Compensator Field Tests

[23] Narain J. Hingorani, Laszlo Gyugyi, “Understanding FACTS” 2000

[24] Optimizing Transient And Filtering Performance Of A C-type 2^{nd} Harmonic Power Filter By The Use Of Solid-State Switches

[25] ERDEMİR [Online], “http://www.erdemir.com.tr”, 29/11/2007.

[26] LabVIEW 8.0 Help

APPENDIX A

LabVIEW CODE OF

NI CompactRIO RT CONTROLLER

Reactive Power Measurement

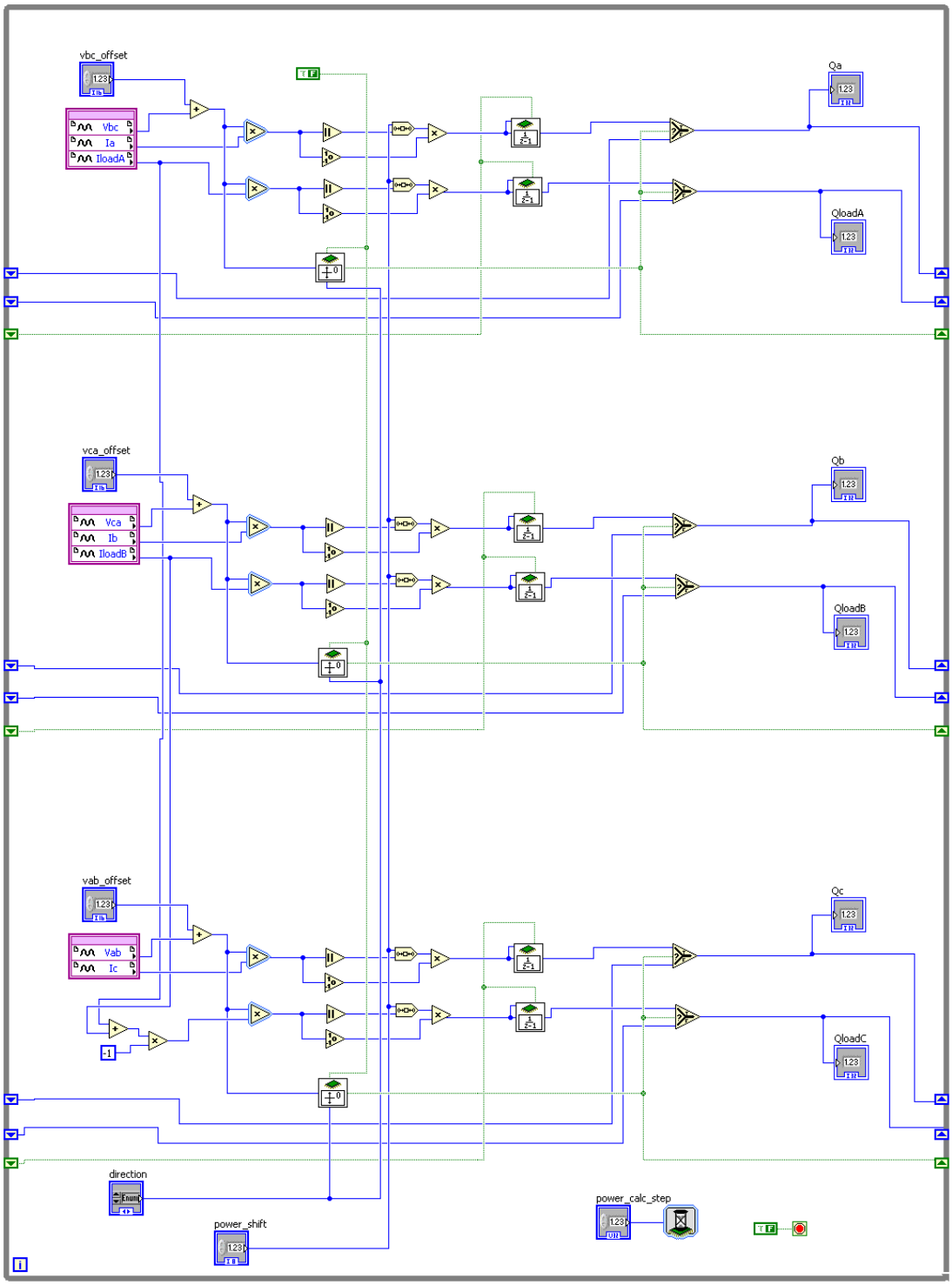


Figure A.1. Reactive Power Measurement code

Digital I/O

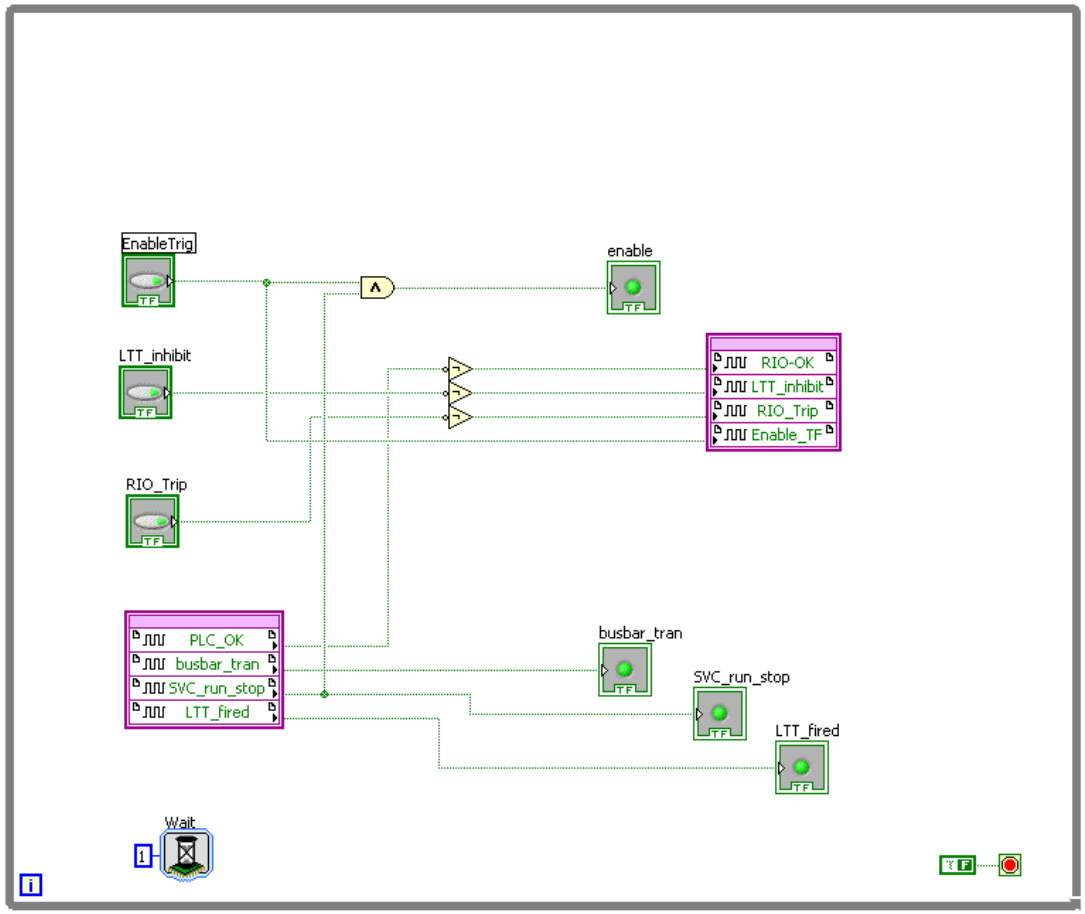


Figure A.4. Digital I/O code

Initializing

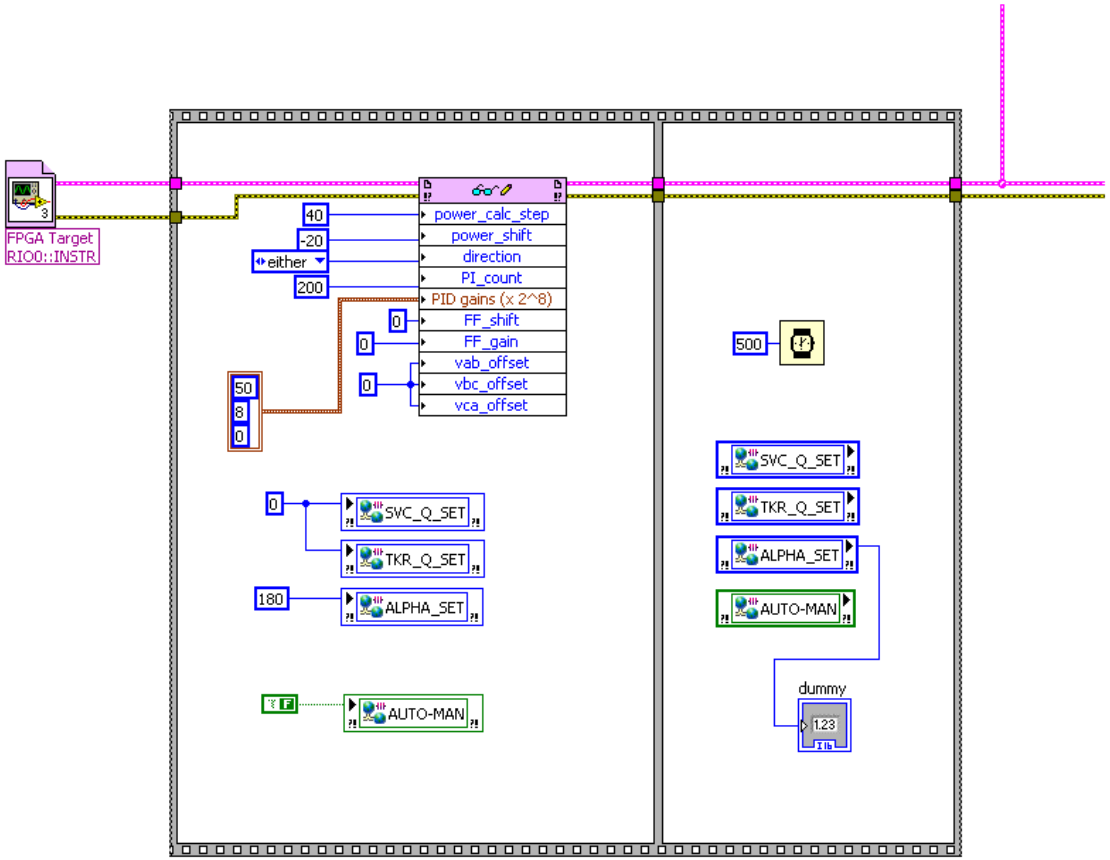


Figure A.5. Initialing Code

FPGA Control

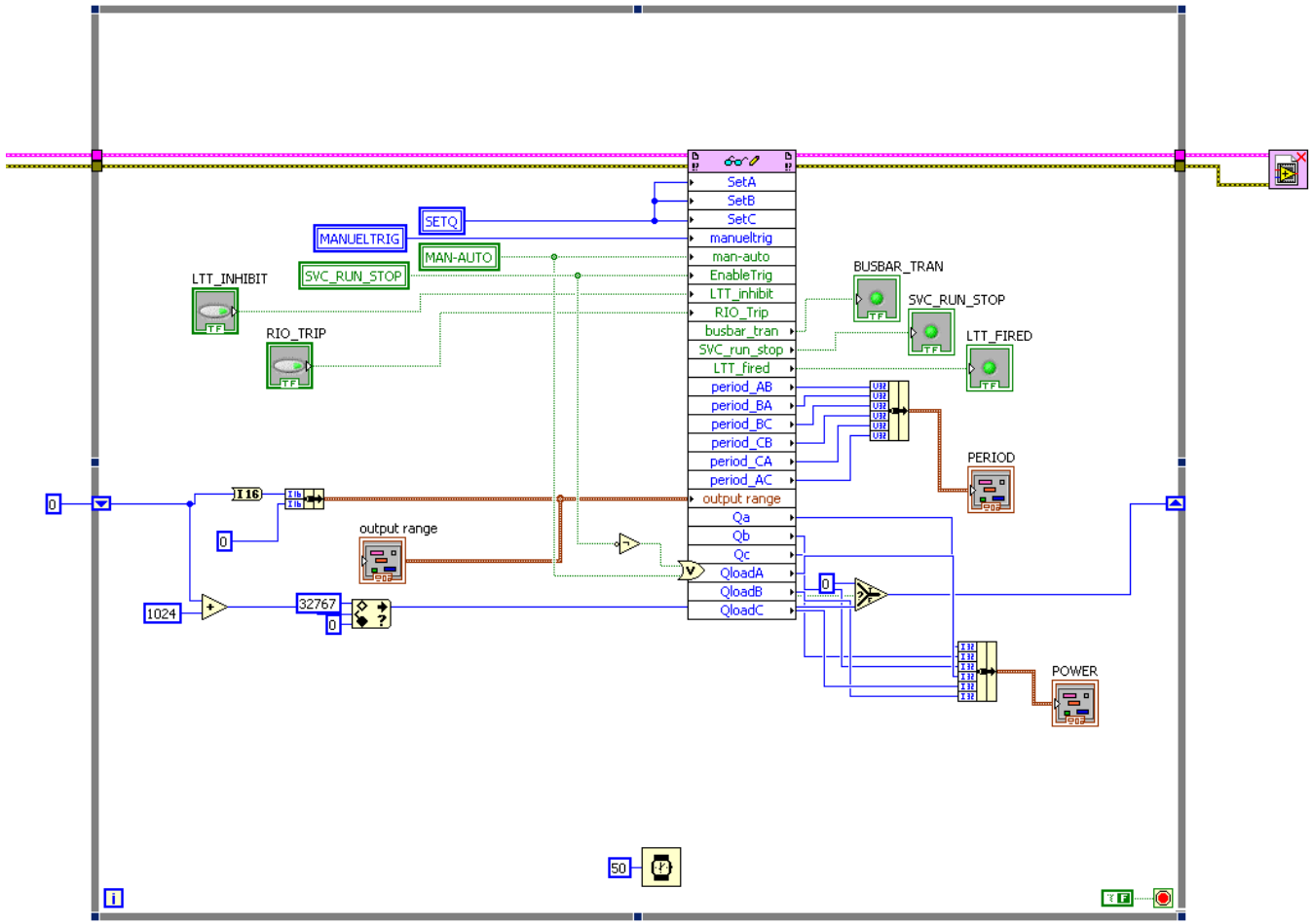


Figure A.6. FPGA Control

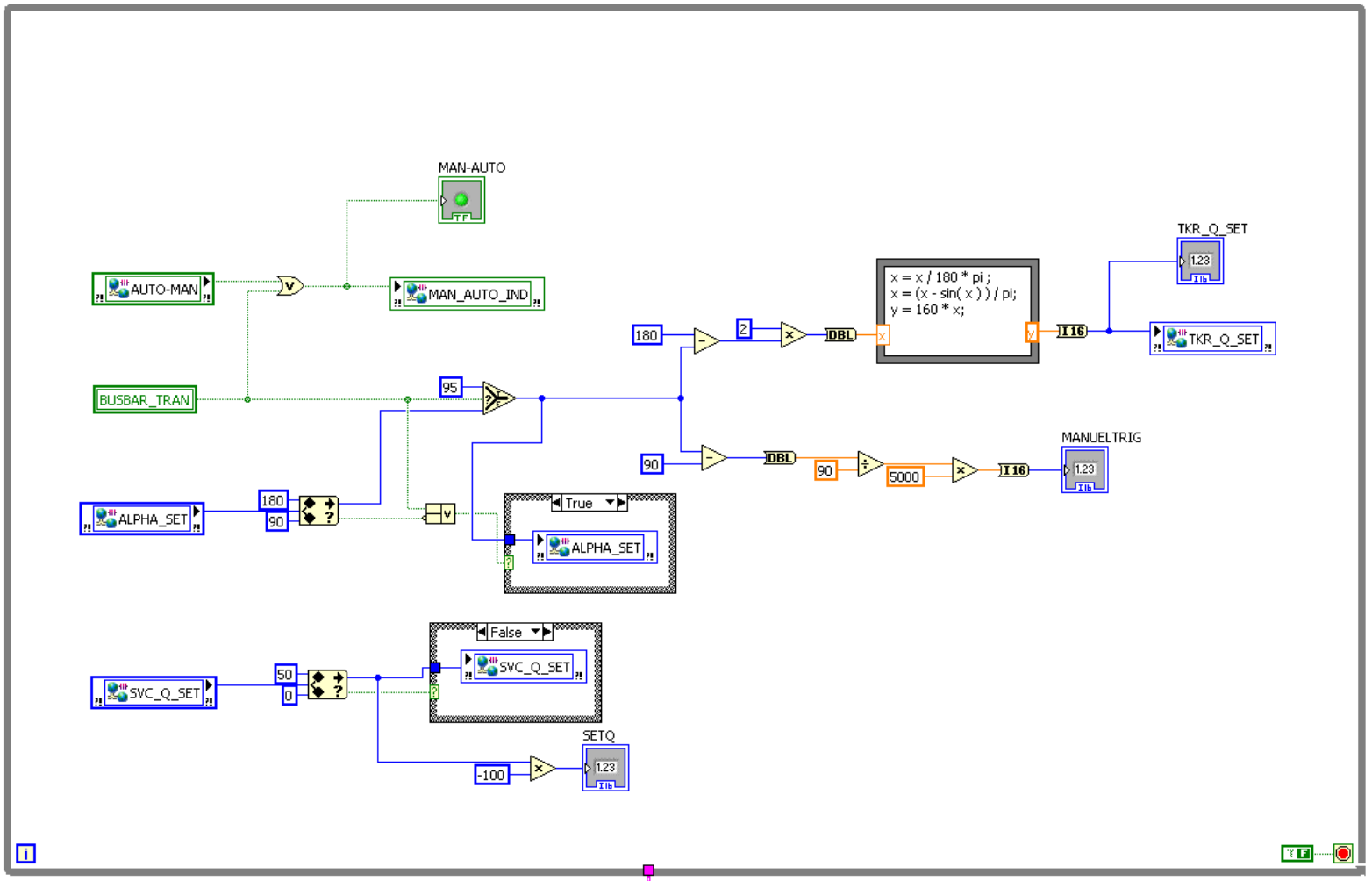
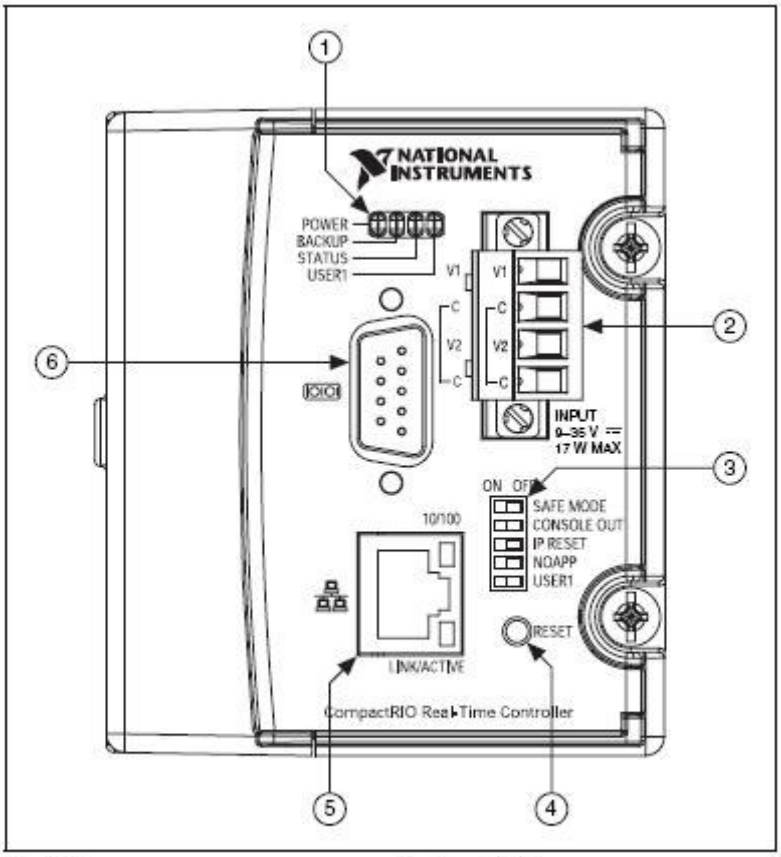


Figure A.7. Communication code

APPENDIX B

NI CompactRIO RT CONTROLLER



1	LEDs	4	Reset Button
2	Power Connector	5	RJ-45 Ethernet Port
3	DIP Switches	6	RS-232 Serial Port

Figure B.1. NI CompactRIO 9002/9004 RT Controller

CompactRIO Real-Time Embedded Controllers

NI cRIO-900x

- Small, rugged, high-reliability embedded real-time processor for intelligent stand-alone operation
- Executes powerful floating-point algorithms with deterministic real-time performance
- Low power consumption with dual DC supply inputs for redundancy
- 10/100BaseT Ethernet port with built-in LabVIEW remote panel Web server and FTP file sharing server
- RS232 serial port for peripheral devices

Operating System
- LabVIEW Real-Time (ETS)

Development Environment
- LabVIEW Full or Professional Development System for Windows
- LabVIEW Reconfigurable I/O Software Development Kit (includes LabVIEW Real-Time and LabVIEW FPGA modules and developer toolkits)

Driver Software
- NI-RIO for reconfigurable embedded systems

Product	DRAM Memory (MB)	Internal Nonvolatile Storage (MB)	10/100BaseTX Ethernet Port	RS232 Serial Port	LEDs	DIP Switches	Power Supply Input Range	Power Consumption	Backup Power Input	Remote Panel Web Server	FTP Server
cRIO-9002	32	64	✓	✓	4	5	9 to 35 VDC	7 W max	✓	✓	✓
cRIO-9004	64	512	✓	✓	4	5	9 to 35 VDC	7 W max	✓	✓	✓

Table 1. cRIO-900x Selection Guide

Overview and Applications

National Instruments cRIO-900x real-time embedded controllers offer powerful stand-alone embedded execution for deterministic LabVIEW Real-Time applications. The NI cRIO-9002 includes 32 MB of DRAM memory and 64 MB of nonvolatile flash storage for file storage. The cRIO-9004 includes 64 MB of DRAM memory and 512 MB of nonvolatile flash storage for data-logging applications. Both controllers are designed for extreme ruggedness, reliability, and low power consumption with dual 9 to 35 VDC supply inputs that deliver isolated power to the CompactRIO chassis/modules and a -40 to 70 °C temperature range. A 195 MHz industrial processor balances low power consumption with powerful real-time floating-point signal processing and analysis capabilities for deterministic control loops exceeding 1 kHz.

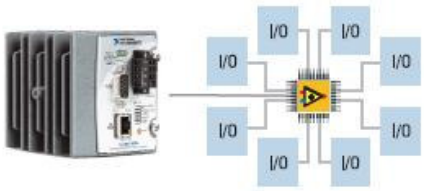


Figure 1. CompactRIO Hardware Architecture

System Configuration

The CompactRIO real-time controller connects to any 4- or 8-slot CompactRIO reconfigurable chassis. The user-defined FPGA circuitry in the chassis controls each I/O module and passes data to the controller through a local PCI bus, using built-in communication functions.

Embedded Software

You can synchronize embedded code execution to an FPGA-generated interrupt request (IRQ) or an internal millisecond real-time clock source. The LabVIEW Real-Time ETS OS provides reliability and simplifies the development of complete embedded applications that include time-critical control and acquisition loops in addition to lower-priority loops for postprocessing, data logging, and Ethernet/serial communication. Built-in elemental I/O functions such as the FPGA Read/Write function provide a communication interface to the highly optimized reconfigurable FPGA circuitry. Data values are read from the FPGA in integer format, and then converted to scaled engineering units in the controller.

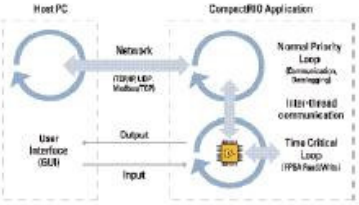


Figure 2. CompactRIO Software Architecture

NATIONAL INSTRUMENTS

NI 9201/9221 Circuitry

The NI 9201/9221 channels are isolated from other modules in the system. The module protects each channel from overvoltages. The input signals are scanned, buffered, conditioned, and then sampled by a single 12-bit ADC. For more information about overvoltage protection, refer to the *Specifications* section.

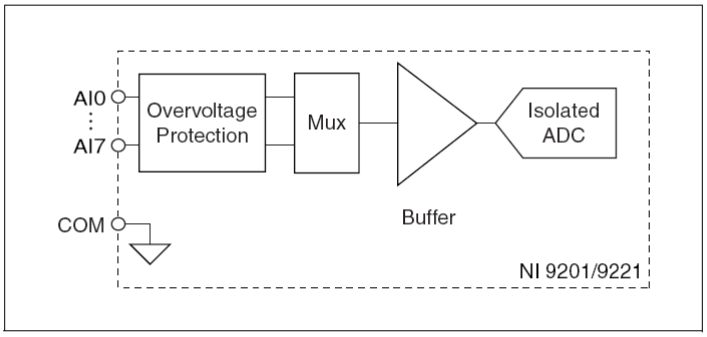


Figure 5. Input Circuitry for One Channel

Specifications

The following specifications are typical for the range –40 to 70 °C unless otherwise noted. All voltages are relative to COM unless otherwise noted.

Input Characteristics

Number of channels 8

ADC resolution ..... 12 bits

Type of ADC ..... Successive approximation register (SAR)

Sample rate (aggregate):

Module	Maximum Sample Rate (R Series Expansion Chassis)	Maximum Sample Rate (All other chassis)
NI 9201, single channel	475 KS/s	800 KS/s
NI 9201, scanning	475 KS/s	500 KS/s
NI 9221	475 KS/s	800 KS/s

NI 9201 8ch 12 bit ± 10V Analog Input Specifications cont.

Input range

NI 9201 ..... ±10 V

NI 9221 ..... ±60 V

Operating voltage ranges[1]

	Measurement Voltage, AI to COM			Maximum Voltage, AI or COM to Earth Ground	
	Min (V)	Typ (V)	Max (V)	Screw Terminal	DSUB
NI 9201	±10.3	±10.53	±10.8	250 V_{rms}	±60 VDC
NI 9221	±61.4	±62.50	±63.8		

Isolation voltage (AI or COM to earth ground, verified by a 5 s dielectric withstand test)[1]

Screw terminal..... 2,300 V_{rms}

DSUB ..... 1,000 V_{rms}

[1] Refer to the *Safety Guidelines* section for more information about safe operating voltages.

Overvoltage protection

(AI to COM) ..... ±100 V

Accuracy[1]

Error	Percent of Reading	Percent of Range*
NI 9201		
Calibrated typ (25 °C, ±5 °C)	±0.04%	±0.07%
Calibrated max (–40 to 70 °C)	±0.25%	±0.25%
Uncalibrated typ (25 °C, ±5 °C)	±0.26%	±0.46%
Uncalibrated max (–40 to 70 °C)	±0.67%	±1.25%
NI 9221		
Calibrated typ (25 °C, ±5 °C)	±0.04%	±0.07%
Calibrated max (–40 to 70 °C)	±0.25%	±0.25%
Uncalibrated typ (25 °C, ±5 °C)	±0.26%	±0.43%

[1] Excludes noise.

NI 9201 8ch 12 bit ± 10V Analog Input Specifications cont.

Error	Percent of Reading	Percent of Range*
Uncalibrated max (–40 to 70 °C)	±0.67%	±1.06%
* Range equals 10.53 V for the NI 9201, 62.50 V for the NI 9221		

Stability
- Offset drift
  - NI 9201 ..... ±100 µV/°C
  - NI 9221 ..... ±580 µV/°C
- Gain drift ..... ±34 ppm/°C

Input bandwidth (–3 dB)
- NI 9201 ..... 690 kHz min
- NI 9221 ..... 950 kHz min

Input impedance
- Resistance ..... 1 MΩ
- Capacitance ..... 5 pF

Input noise (code-centered)
- RMS ..... 0.7 LSB_{rms}
- Peak-to-peak ..... 5 LSB

No missing codes ..... 12 bits

DNL ..... –0.9 to 1.5 LSB

INL ..... ±1.5 LSB

Crosstalk ..... –75 dB, 10 kHz

Settling time (to 1 LSB)
- NI 9201 ..... 2 µs
- NI 9221 ..... 1.25 µs

MTBF ..... 1,485,465 hours at 25 °C; Bellcore Issue 6, Method 1, Case 3, Limited Part Stress Method

Note Contact NI for Bellcore MTBF specifications at other temperatures or for MIL-HDBK-217F specifications. Go to `ni.com/certification` and search by module number or product line for more information about MTBF and other product certifications.

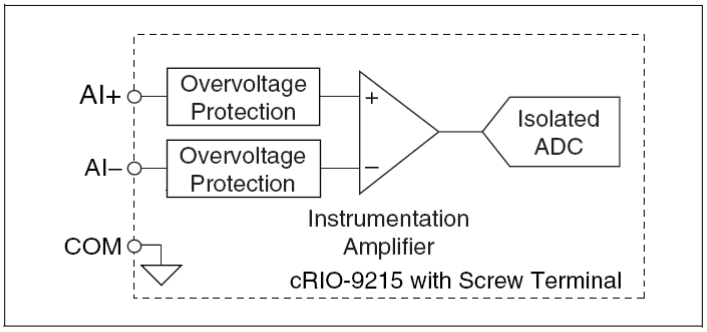


Figure 5. Input Circuitry for One Channel on the cRIO-9215 with Screw Terminal

The cRIO-9215 with BNC has a resistor that ensures the input voltage does not drift outside of the common-mode range.

NI-RIO Software

For information about determining which software you need for the modules you are using, go to `ni.com/info` and enter `rdniriosoftware`.

Specifications

The following specifications are typical for the range –40 to 70 °C unless otherwise noted.

Input Characteristics

Number of channels ..... 4 analog input channels

ADC resolution ..... 16 bits

Type of ADC ..... Successive approximation register (SAR)

NI 9215 4ch 16 bit ± 10V Analog Diff. Input Specifications cont.

Operating voltage range (AI+ to AI–)
- Typical ..... ±10.4 V
- Minimum[1] ..... ±10.2 V
- Maximum ..... ±10.6 V

Maximum working voltage (signal +common mode)
- cRIO-9215 with screw terminal ..... Each channel must remain within ±10.2 V of common
- cRIO-9215 with BNC ..... All inputs must remain within ±10.2 V of the average AI– inputs

Overvoltage protection ..... ±30 V

Conversion time
- One channel ..... 4.4 µs
- Two channels ..... 6 µs
- Three channels ..... 8 µs
- Four channels ..... 10 µs

[1] The *minimum operating voltage range* is the largest voltage the cRIO-9215 can accurately measure.

Accuracy

Error	Percent of Reading	Percent of Range*
Calibrated max (–40 to 70 °C)	0.2%	0.082%
Calibrated typ (25 °C, ±5 °C)	0.02%	0.014%
Uncalibrated max (–40 to 70 °C)	1.05%	0.82%
Uncalibrated typ (25 °C, ±5 °C)	0.6%	0.38%
* Range equals 10.4 V		

Stability
- Offset drift ..... 60 µV/ºC
- Gain drift ..... 10 ppm/ºC

CMRR (at 60 Hz) ..... –73 dB min

Input bandwidth (–3 dB) ..... 420 kHz min

Input impedance
- Resistance
  - cRIO-9215 ..... 1 GΩ

cRIO-9215 with BNC
(Between any two
AI– terminals) ..... 200 kΩ
Capacitance ..... 25 pF
Input bias current ..... 10 nA
Input noise
RMS ..... 1.2 LSB_{rms}
Peak-to-peak ..... 7 LSB
Crosstalk ..... –80 dB
Settling time (to 2 LSBs)
cRIO-9215 with screw terminal
10 V step ..... 10 µs
20 V step ..... 15 µs
cRIO-9215 with BNC
10 V step ..... 25 µs
20 V step ..... 35 µs
No missing codes ..... 15 bits guaranteed
DNL ..... –1.9 to 2 LSB max
INL ..... ±6 LSB max

MTBF ..... 1,167,174 hours at 25 °C; Bellcore Issue 6, Method 1, Case 3, Limited Part Stress Method

Note Contact NI for Bellcore MTBF specifications at other temperatures or for MIL-HDBK-217F specifications. Go to `ni.com/certification` and search by model number or product line for more information about MTBF and other product certifications.

Power Requirements

Power consumption from chassis (full-scale input, 100 kS/s)
Active mode ..... 560 mW max
Sleep mode ..... 25 µW max
Thermal dissipation (at 70 °C)
Active mode ..... 560 mW max
Sleep mode ..... 25 µW max

The DIO channels of the NI 9401 are grouped in two ports, one containing channels 0, 1, 2, and 3, and one containing channels 4, 5, 6, and 7. You can configure each port in software for input or output. Note that all four channels in a port must be configured for the same direction.

Connecting an SPI Device to the NI 9401

Figure 2 shows an SPI device connected to the NI 9401. In this example, the three channels assigned to output signals are on one port and the channel assigned to an input signal is on the other port.

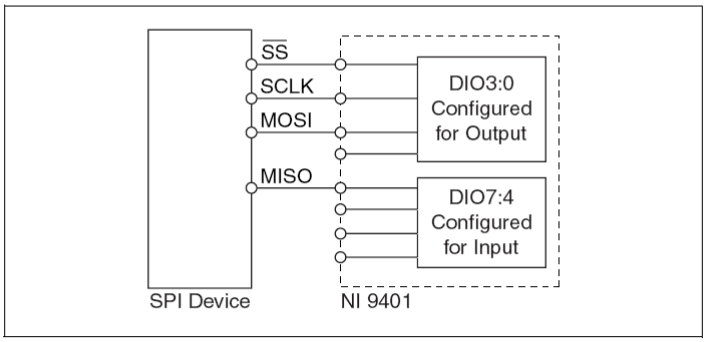


Figure 2. Connecting an SPI Device to the NI 9401

Input type ..... TTL, single-ended

Output type ..... TTL, single-ended

Digital logic levels

- Maximum input voltage ..... 5.25 V
- Input high, V_{IH} ..... 2 V min
- Input low, V_{IL} ..... 0.8 V max
- Output high, V_{OH} ..... 5.25 V max
  - Sourcing 100 µA ..... 4.7 V min
  - Sourcing 2 mA ..... 4.3 V min
- Output low, V_{OL}
  - Sinking 100 µA ..... 0.1 V max
  - Sinking 2 mA ..... 0.4 V max

Maximum input-signal switching frequency by number of input channels

- 8 input channels ..... 9 MHz
- 4 input channels ..... 16 MHz
- 2 input channels ..... 30 MHz

NI 9401 8ch TTL Digital I/O cont.

Maximum switching frequency by number of output channels, with 1 mA, 50 pF load

- 8 output channels ..... 5 MHz
- 4 output channels ..... 10 MHz
- 2 output channels ..... 20 MHz

Propagation delay

- Input ..... 100 ns max
- Output ..... 100 ns max

Pulse width distortion

- Input ..... 10 ns typ
- Output ..... 10 ns typ

I/O leakage current ..... 20 µA typ

Input impedance

- Input capacitance ..... 40 pF max
- Input resistance ..... 45 kΩ min

Input rise/fall time ..... 500 ns max

Input protection ..... ±30 V max on one channel at a time

Isolation barrier (channel to earth ground)[1]

- Continuous ..... 60 VDC, Measurement Category I
- Withstand ..... 1,000 V_{rms}, verified by a 5 s dielectric withstand test

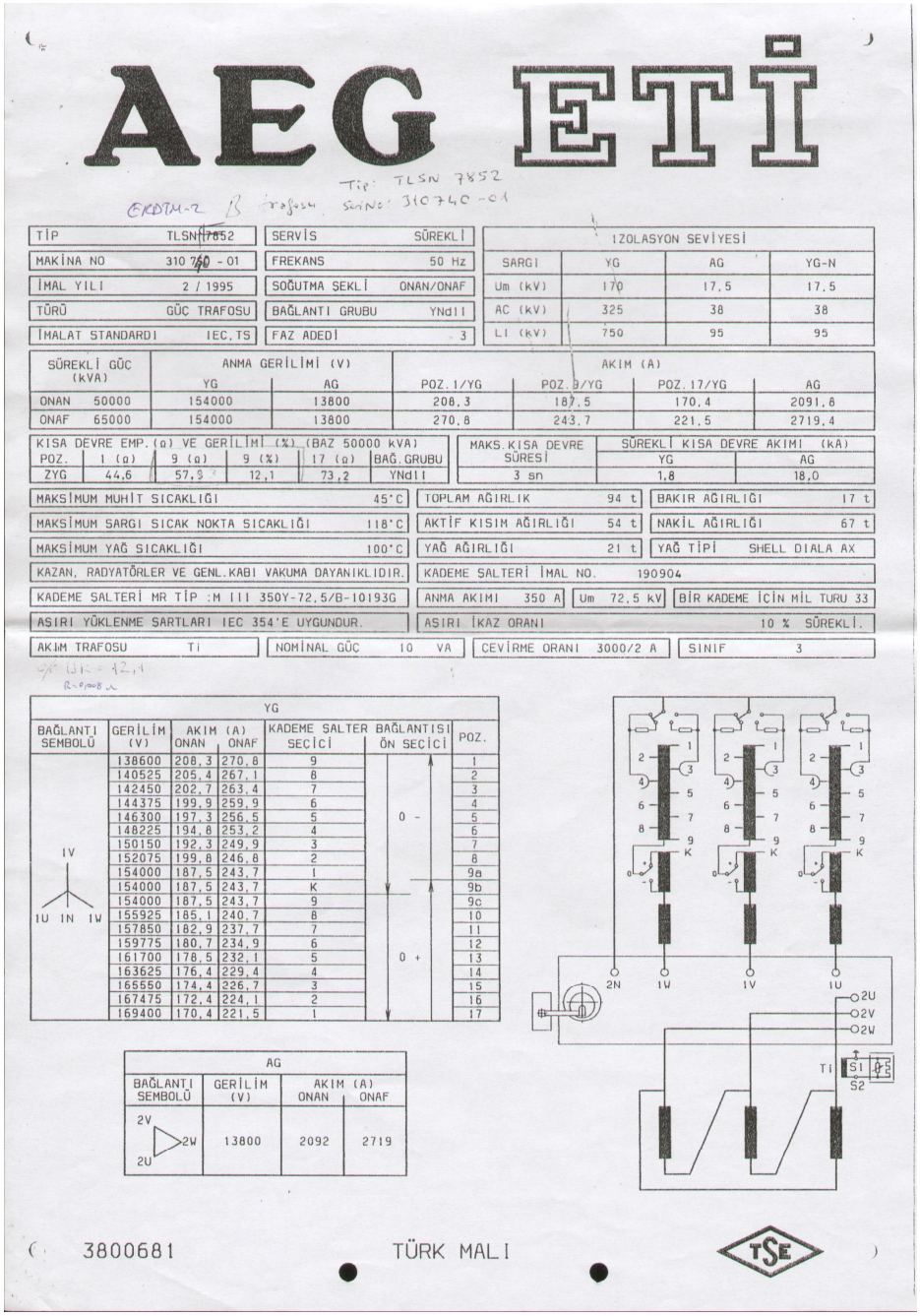
MTBF ..... 1,244,763 hours at 25 °C; Bellcore Issue 6, Method 1, Case 3, Parts Count Method

Note Contact NI for Bellcore MTBF specifications at other temperatures or for MIL-HDBK-217F specifications. Go to `ni.com/certification` and search by module number or product line for more information about MTBF and other product certifications.

[1] Refer to the *Safety* section for more information about safety and isolation voltages.

APPENDIX C

POWER TRANSFORMER DATASHEET



AEG ETİ

Tip: TLSN 7852
ERDTM-2 B trafosu Sıra No: 310740-01

TİP	TLSN 7852	SERVİS	SÜREKLİ
MAKİNA NO	310740 - 01	FREKANS	50 Hz
İMAL YILI	2 / 1995	SOĞUTMA SEKLİ	ONAN/ONAF
TÜRÜ	GÜÇ TRAFOSU	BAĞLANTI GRUBU	YNd11
İMALAT STANDARDI	IEC,TS	FAZ ADEDİ	3

İZOLASYON SEVİYESİ			
SARGI	YG	AG	YG-N
Um (kV)	170	17,5	17,5
AC (kV)	325	38	38
LI (kV)	750	95	95

SÜREKLİ GÜÇ (kVA)	ANMA GERİLİMİ (V)		AKIM (A)			
	YG	AG	POZ.1/YG	POZ.9/YG	POZ.17/YG	AG
ONAN 50000	154000	13800	208,3	187,5	170,4	2091,8
ONAF 65000	154000	13800	270,8	243,7	221,5	2719,4

KISA DEVRE EMP. (a) VE GERİLİMİ (%) (BAZ 50000 kVA)					MAKS.KISA DEVRE SÜRESİ	SÜREKLİ KISA DEVRE AKIMI (kA)	
POZ.	1 (a)	9 (a)	9 (%)	17 (a)	BAĞ.GRUBU		YG / AG
ZYG	44,6	57,9	12,1	73,2	YNd11	3 sn	1,8 / 18,0

MAKSİMUM MUHİT SICAKLIĞI 45°C	TOPLAM AĞIRLIK 94 t	BAKIR AĞIRLIĞI 17 t
MAKSİMUM SARGI SICAK NOKTA SICAKLIĞI 118°C	AKTİF KISIM AĞIRLIĞI 54 t	NAKİL AĞIRLIĞI 67 t
MAKSİMUM YAĞ SICAKLIĞI 100°C	YAĞ AĞIRLIĞI 21 t	YAĞ TİPİ SHELL DIALA AX
KAZAN, RADYATÖRLER VE GENL.KABI VAKUMA DAYANIKLIDIR.	KADEME SALTERİ İMAL NO. 190904	
KADEME SALTERİ MR TİP :M III 350Y-72,5/B-10193G	ANMA AKIMI 350 A	Um 72,5 kV / BİR KADEME İÇİN MİL TURU 33
AŞIRI YÜKLENME SARTLARI IEC 354'E UYGUNDUR.	AŞIRI İKAZ ORANI 10 % SÜREKLİ.	
AKIM TRAFOSU Ti	NOMİNAL GÜÇ 10 VA	ÇEVİRME ORANI 3000/2 A / SINIF 3

YG

BAĞLANTI SEMBOLÜ	GERİLİM (V)	AKIM (A) ONAN	AKIM (A) ONAF	KADEME SALTER BAĞLANTISI SEÇİCİ	ÖN SEÇİCİ	POZ.
1V / 1U 1N 1W	138600	208,3	270,8	9	0 -	1
	140525	205,4	267,1	8		2
	142450	202,7	263,4	7		3
	144375	199,9	259,9	6		4
	146300	197,3	256,5	5		5
	148225	194,8	253,2	4		6
	150150	192,3	249,9	3		7
	152075	199,8	246,8	2		8
	154000	187,5	243,7	1		9a
	154000	187,5	243,7	K		9b
	154000	187,5	243,7	9		9c
	155925	185,1	240,7	8		10
	157850	182,9	237,7	7		11
	159775	180,7	234,9	6		12
	161700	178,5	232,1	5	0 +	13
	163625	176,4	229,4	4		14
	165550	174,4	226,7	3		15
	167475	172,4	224,1	2		16
	169400	170,4	221,5	1		17

AG

BAĞLANTI SEMBOLÜ	GERİLİM (V)	AKIM (A) ONAN	AKIM (A) ONAF
2V / 2U 2W	13800	2092	2719

3800681 TÜRK MALI TSE

APPENDIX D

GROUNDING TRANSFORMER DATASHEET

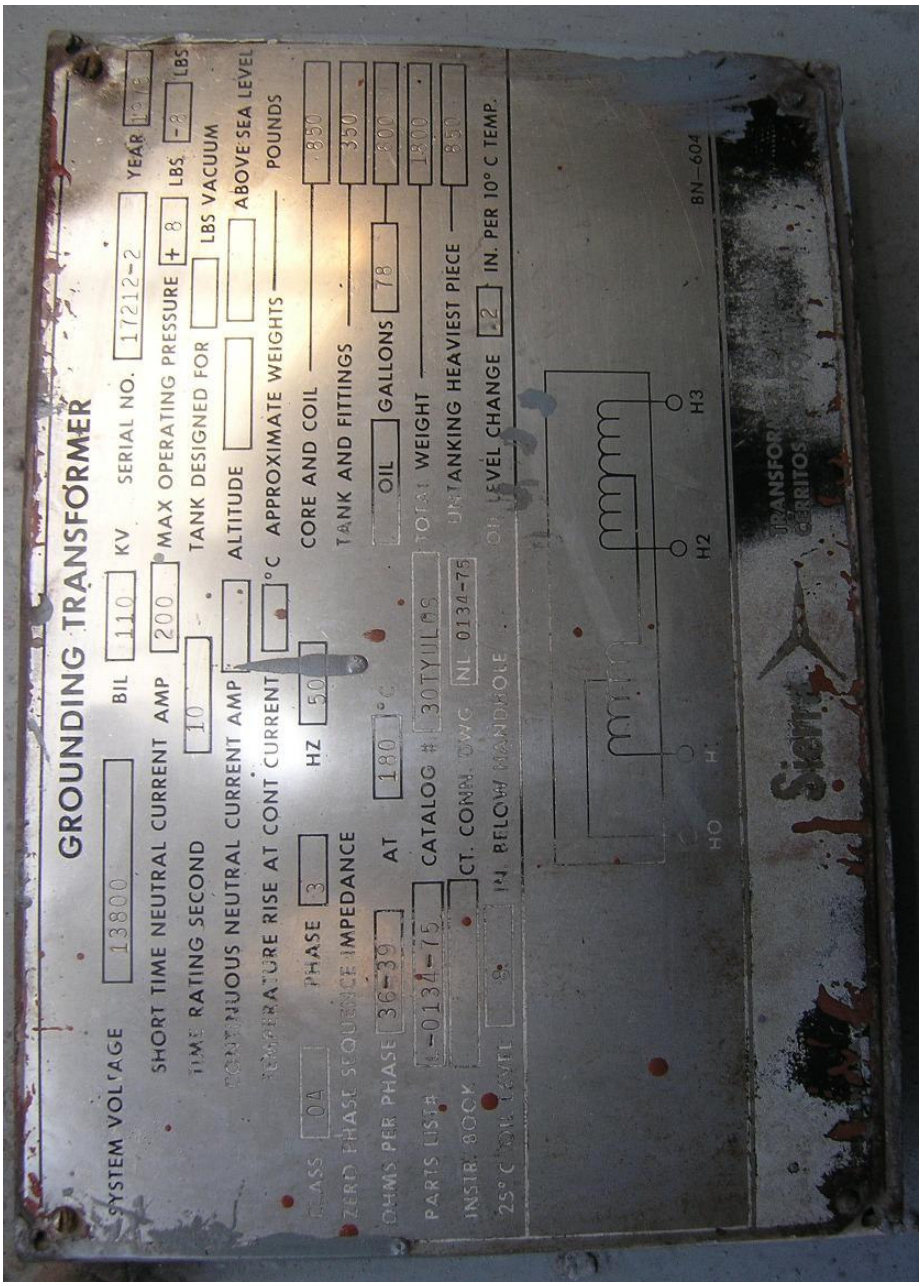


Figure D1. Grounding Transformer Data