MECHANICAL FATIGUE AND LIFE ESTIMATION ANALYSIS OF PRINTED CIRCUIT BOARD COMPONENTS

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
MIDDLE EAST TECHNICAL UNIVERSITY

BY

CEM GENÇ

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF MASTER OF SCIENCE
IN
MECHANICAL ENGINEERING

AUGUST 2006

Approval of the Graduate School of Natural and Applied Sciences

Prof. Dr. Canan ÖZGEN
Director

I certify that this thesis satisfies all the requirements as a thesis for the degree of Master of Science.

Prof. Dr. Kemal İDER
Head of Department

This is to certify that I have read this thesis and that in our opinion it is fully adequate, in scope and quality, as a thesis for the degree of Master of Science.

Prof. Dr. Y. Samim ÜNLÜSOY
Supervisor

Examining Committee Members

Prof. Dr. Cahit ERALP (Chairperson)	(METU, ME)	
Prof. Dr. Y. Samim ÜNLÜSOY	(METU, ME)	
Prof. Dr. Mehmet ÇALIŞKAN	(METU, ME)	
Asst. Prof. Dr. İlhan KONUKSEVEN	(METU, ME)	
Assoc. Prof. Dr. Mehmet ÇELİK	(ASELSAN)	

I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

Name, Last Name: Cem GENÇ

Signature:

ABSTRACT

MECHANICAL FATIGUE AND LIFE ESTIMATION ANALYSIS OF PRINTED CIRCUIT BOARD COMPONENTS

GENÇ, Cem
M.Sc., Department of Mechanical Engineering
Supervisor: Prof. Dr. Y. Samim ÜNLÜSOY
August 2006, 190 Pages

In this thesis, vibration induced fatigue life analysis of axial leaded Tantalum & Aluminum capacitors, PDIP and SM capacitors mounted on the printed circuit boards are performed. This approach requires the finite element model, material properties and dynamic characteristics of the PCB. The young modulus of the PCB material is obtained from 3 point bending tests, resonance frequencies are obtained from modal tests and transmissibility's of the PCB are obtained from transmissibility tests which are used as fatigue analysis inputs.

Step Stress Tests are performed to obtain failure times of the tested electronic components which are also used as the numerical fatigue analysis inputs. Consecutively, fatigue analysis of a sample PCB used in military systems is aimed since it is important to compare the calculated fatigue damage to estimated life limits in order to determine which component(s), if necessary, must be moved to positions of lower damage . For this purpose, power PCB of the power distribution unit used in Leopard 1 battle tank is examined. Numerical fatigue analysis coupled with accelerated life test whose profile is convenient to military platforms is performed.

Furthermore, the effects of "eccobond" and silicone on the fatigue life of the components are also surveyed since these techniques are common in electronic

packaging. In addition, mean-time-to-failure values are obtained for the tested components by using Weibull distribution.

Finally, sensitivity analysis is performed to indicate the effect of certain parameters on the fatigue life of a sample axial leaded capacitor.

Keywords: Vibration Fatigue, Failure, Printed Circuit Boards, Finite Element Method, Accelerated Life Testing.

ÖZ

BASKI DEVRE KART ELEMANLARININ MEKANİK YORULMASI VE YORULMA ÖMÜRLERİNİN TAHMİNİNE AİT ANALİZLER

GENÇ, Cem

Yüksek Lisans, Makine Mühendisliği Ana Bilim Dalı

Tez Yöneticisi: Prof. Dr. Y. Samim ÜNLÜSOY

Ağustos 2006, 190 Sayfa

Bu tez çalışmasında; baskı devre kartlar üzerine monte edilen eksenel bacaklı Tantal ve Aluminyum kapasitörler, plastik çift sıralı paketler ve yüzey monte kapasitörlerde titreşim kaynaklı yorulmaya bağlı oluşan hasarlar analiz edilmiştir. Bu metotta baskı devre kartın sonlu elemanlar modeli kullanılmaktadır. Baskı devre kart malzemesinin 3 nokta bükme testleri vasıtasıyla elde edilen elastisite modülüsü, modal testler ile elde edilen rezonans frekansları ve geçirgenlik testleri ile elde edilen rezonans geçirgenlikleri analizlerde girdi olarak kullanılmıştır.

Basamaklandırılmış Gerilme Test Yöntemi kullanılarak malzemelerin hızlandırılmış ömür testlerindeki dayanımları elde edilmiş ve bu değerler de analizlerde girdi olarak kullanılmıştır. Ardından, örnek olarak askeri sistemlerde kullanılacak bir baskı devre kartın analizi hedeflenmiştir. Bu çalışmada, Leopard 1 tankının güç dağıtım biriminin güç baskı devre kartı incelenmiştir. Baskı devre karta askeri platformlara uygun olan bir yük uygulanarak kartın hızlandırılmış ömür testleri ve sayısal yorulma analizleri yapılmıştır.

Bunun yanı sıra, elektronik paketlemede “eccobond” ve silikon ile sağlamlaştırma yaygın bir yöntem olduğu için bu yöntemlerin elektronik malzemelerin yorulma

ömrü üzerine olan etkileri de incelenmiştir. Ayrıca test edilen malzemeler için ortalama hasar süreleri de Weibull dağılımı kullanılarak elde edilmiştir.

Son olarak baskı devre kartlara ait çeşitli özelliklerin değiştirilmesi ile yorulma ömrünün nasıl etkilendiğini görmek için örnek bir eksenel bacaklı kapasitör için hassasiyet analizleri yapılmıştır.

Anahtar Kelimeler: Titreşim Kaynaklı Yorulma, Hasar, Baskı Devre Kart, Sonlu Elemanlar Yöntemi, Hızlandırılmış Ömür Testi

To My Family

ACKNOWLEDGEMENTS

I express my sincere appreciation to my thesis supervisor Prof. Dr. Y. Samim ÜNLÜSOY and Assoc. Prof. Dr. Mehmet ÇELİK for their supervision, support and helpful critics throughout the progress of my thesis study.

I would like to thank to Murat AYKAN and also to Mr. Mehmet BAYHAN, Mr. Hakan AKGÜN, Emin İlker ÇETİNBAŞ, Tuğba ŞİLTU, Murat ERTEK and Mrs. Arzu KONUKSEVEN for their great support.

The cooperation and friendly support of my colleagues in ASELSAN during my thesis study also deserves to be acknowledged.

Finally, many thanks to my parents and my elder sister for their continuous help and understanding during my thesis study.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF SYMBOLS & ABBREVIATIONS

A: Amplitude ratio, S_a / S_m

A_s : Shear area

$A_{leadwire}$: Area of the lead wire

a_{in}: Input vibration acceleration

a_w : Weibull scale parameter

AC: Alternative current

ALT: Accelerated life test

ASTM: American Society for Testing of Materials

b: Basquin exponent

b_w : Weibull shape parameter

$b_{specimen}$: Width of the 3 point bending test specimen

BGA: Ball grid array

C: Constant in Basquin exponent

d: Relative damage number

d^*: Accumulated damage for the test step in which failure is detected.

d_{actual}: Accumulated damage at failure for the DIP which fails first.

d_{cap} : Lead wire diameter

d_h : Diameter of the plated through hole

d_s : Shear tearout diameter induced by bending of the lead wire

d_w : Lead wire diameter

d_{step}: Incremental damage accumulated for the fail-free step(or when the failure occurs at the end of the step)

d_{step1}: Accumulated damage at the end of the step 1

d_{test}: Accumulated damage for the most critical DIP on the PCB in the SST.

d_{tot}: Total accumulated damage number for the failed component

D: Total damage number

D_i : Damage fraction

D_{cap}: Component body diameter

DC: Direct current

DIP: Dual Inline Package

DOE: Design of experiments

DOF: Degree of freedom

δ : Resultant vertical deflection at point 3

δ_3^P : Vertical deflection at point 3 due to force P.

δ_3^θ : Vertical deflection at point 3 due to θ.

ε : Strain

ε_s : Maximum strain in the solder joint

ε_w : Lead wire strain

E_s : Modulus of elasticity of the solder

E_w : Modulus of elasticity of the lead wire

E_x : Modulus of elasticity of the PCB in X direction

E_y : Modulus of elasticity of the PCB in Y direction

ESS: Environmental Stress Screen

f_n : Damped Natural frequency

f_s : Sampling frequency of the recorded signal

FEA: Finite Element Analysis

FEM: Finite Element Model

FR-4: Epoxy glass laminate

FFT: Fast Fourier Transform

FRF: Frequency response function

$G_{in}(f)$: PSD of the input acceleration

$G_{out}(f)$: PSD of the response acceleration

G_{RMS} : Output RMS acceleration in g's.

h : Vertical portion of the leadwire

h_{board} : Board thickness

I_1 : Area moment of inertia for M_1 (XZ plane)

I_2 : Area moment of inertia for M_2 (YZ plane)

I_h : Area moment of inertia of the horizontal portion of the leadwire

I_v : Area moment of inertia of the vertical portion of the leadwire

I_w : Area moment of inertia of the lead wire

ICP: Integrated circuit piezoelectric

IEST: Institute of Environmental Sciences and Technology

K: Stress concentration factor

K_0 : Stress concentration factor for axial stress

K_1 : Stress concentration factor for the bending stress due to M_1

K_2 : Stress concentration factor for the bending stress due to M_2

l : Horizontal portion of the leadwire

L: Length of the PCB

L_{cap}: Component body length

$L_{specimen}$: Span of the 3 point bending test specimen

m: S-N curve slope

m_{comp} : Mass of the axial leaded component

M_1 : Resultant bending moment at the buit-in end

M_1^P : Reaction moment at the buit-in end (critical point 1)

M_2^P : Reaction moment at the crtical location 2

M_3^P : Reaction moment at the crtical location 3

M_1^θ : Reaction moment at the buit-in end due to θ

M_2^θ : Reaction moment at the crtical location 2 due to θ

M_X : Bending moment in YZ plane (about x axis of the PCB)

M_Y : Bending moment in XZ plane (about y axis of the PCB)

MDTF: Mean damage index to failure

MTTF: Mean time to failure

N: Number of cycles to failure

N_i : Number of cycleas to failure at stress level S_i

n: Number of cycles experienced in the response range

n_i : Number of applied cycleas at stress level S_i

P: Force acting on the component normal to the surface of the board

$P_{leadwire}$: Axial force on the leadwire

P (sigma$_1$, sigma$_2$): Probability that a peak will be between (sigma$_1$.RMS) & (sigma$_2$.RMS)

PBGA: Plastic ball grid array

PBT: Polybutylene Terephthalete

PCB: Printed Circuit Board

pdf: Probability density function

PLCC: Plastic leadless chip carrier

PSD: Power spectral density

PSD_{input} : Input acceleration spectral density in units of g^2/Hz at f_n

PQFP: Plastic Quad Flat Package

PWA: Printed Wiring Assembly

PWB: Printed Wiring Board

Q : Resultant shear force

Q_n: Transmissibility at resonance

$Q(f)$: Transmissibility as a function of frequency.

Q^P : Shear force at the buit-in end (critical point 1)

Q^θ : Shear force at the buit-in end due to θ

R: Stress ratio, $S_{\min} / S_{\max}$

RMS: Root mean square

RSS: Root Sum Square

S: Stress

S_a : Alternating stress amplitude

S_f : Endurance strength

S_m : Mean stress

$S_{\max}$: Maximum alternating stress

$S_{\min}$: Minimum alternating stress

S_r : Stress range

SEM: Scanning electron microscopy

SM: Surface Mount

SMT: Surface Mount Technology

SMOBC: Solder mask over bare copper

SSC: Selective solder coating

SST: Step stress test

σ : RMS value of the stress or acceleration

σ_{bend} : Bending stress

σ_s : Solder joint stress

$\sigma_{\max}$: Maximum principal stress

σ_{tot} : Total bending stress

σ_w : Bending stress in the leadwire

$\tau_{\max}$: Maximum shear stress

τ_s : Average shear stress

t^*: Time passed from the beginning of the step to the instant of failure

$t_{specimen}$: Thickness of the 3 point bending test specimen

T: Sample Period

Δt: Constant step duration

T_{life}: Actual fatigue life time

T_r: Transmissibility ratio

θ : Relative rotation of leads

θ_A : Curvature of the PCB at point A

θ_B : Curvature of the PCB at point B

θ_{cap} : Angle between horizontal and the axial leaded capacitor

ω : Vertical displacement of the circuit board

W: Width of the PCB

CHAPTER 1

INTRODUCTION

1.1 Fatigue

Fatigue is one of the most persistent problems in engineering design, ranging from failure of rotating shafts and reciprocating components to failure in aircraft, ships, and large civil engineering structures like bridges and buildings. In electronic packages, fatigue problems are commonly encountered in solder joints, bond wires, copper plated vias, etc.

In real life, machine parts, mechanical systems etc. are rarely under static loading. Most of the time dynamic loadings are encountered and these kinds of loading occurring in machine members produce stresses which are called *repeated, alternating* or *fluctuating* stresses. Materials can fracture when they are subjected to repeated stresses that are considerably less than the ultimate static strength of the material, and quite frequently even below the yield strength. It is usually relatively easy to design products and processes so that the margin between static strength and the static stress is adequate. However, cyclic mechanical stresses well below the yield or fracture stress can cause progressive weakening, so that the resisting strength is reduced, eventually resulting in failure. This mechanism is called as *fatigue.*

Failure definitions in fatigue are subjective. It could be a predetermined crack length, fracture of the component or malfunction of a system. With this definition two categories of fatigue can be considered: low cycle and high cycle fatigue.Low cycle fatigue corresponds to the largest stresses, higher than the yield stress of a material, where number of cycles, N, of the S-N curve varies from a quarter of

cycle with approximately 10^4 to 10^5 cycles (for mild steels). In this zone there are large strain amplitudes hence one can very quickly observe significant plastic deformation followed by failure of the material.

High cycle fatigue gets its name from the number of cycles required for failure, which are relatively higher than low cycle fatigue. It refers to failures due to low stress amplitudes without appearance of measurable plastic deformation. Approximately $10^4 - 10^5$ cycles [1] or more are required for high cycle fatigue. The reason for this is that, if the loading to the component is such that the yield strength is not exceeded and the stress state is much below, than the component will remain mostly in the elastic region and will require higher number of cycles to failure. But if the loading is such that the yield strength is exceeded by little amount, and then since the component is forced plastically, lesser cycles will be enough for failure and thus a low cycle fatigue failure will occur.

Three methods were developed to investigate the fatigue phenomenon. The first one is the *Stress-Life* method. In this method no crack initiation or propagation effects are considered. Stress versus Cycle (S-N) curve of the material is used for the analysis. The failure criterion is that when the damage index is, e.g. for Palmgren-Miner's damage rule, reaches one the specimen or component fails.

The second method is the *Strain-Life* method. This theory is by some the best theory to explain the nature of the fatigue failure. However it appears to be of little use to the designers because the question of how to determine the total strain at the bottom of a notch or discontinuity has not been answered. There are no sufficient tables or charts of strain concentration factors in the literature.

The final method is the *Crack Propagation* method, which assumes that the nominal stress and the crack size control the fatigue life. This is the only method directly dealing with the cracks. The theory needs the accurate determination of the initial crack size. From these definitions it is evident that for high cycle fatigue analysis the *Stress-Life* method (S-N curve) and for low cycle fatigue analysis *Strain-Life* (ε-N curve) method should be used.

Finally, there are two domains for fatigue analysis. First one is the time domain (rain flow cycle counting) and the second one is the frequency domain methods. In this study frequency domain fatigue life prediction method using the Miner-Palmgren linear damage accumulation theory will be used.

1.2 Vibration of Electronic Components Mounted On the Circuit Boards

Many different types of printed circuit boards are manufactured by the electronics industry. FR-4 (epoxy glass laminate) is the most commonly employed composite material used with laminated copper layers for PCB production. The rectangular printed-circuit board is the most common geometry used by the electronics industry, since this shape is easily adapted to the plug-in type of assembly.

When a printed circuit board is deflected during exposure to vibration, the magnitude of the stresses produced depends on the deflected shape of the circuit board.This deflection is strongly dependent upon the boundary conditions imposed in constraining the board. However it can be concluded that epoxy-glass circuit boards can be designed to be fatigue resistant. Indeed structural failure of the board itself is rarely observed [2]. However, during vibration in an axis perpendicular to the plane of the printed circuit board the circuit board bends back and forth so bending stresses are developed in the electrical lead wires of the components which fasten the components to the printed circuit boards (Figure 1.1).

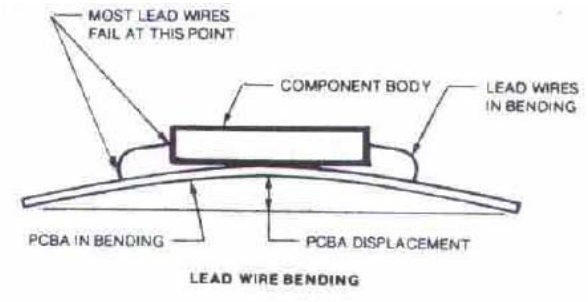


Figure 1.1: Bending in the component lead wires on a vibrating circuit board [3]

The ability of the electronic components to survive vibration depends upon many different factors such as component size, component location & orientation on the board, resonant frequency of the PCB, method of mounting of the component, duration and amplitude of the vibration requirement etc. Some basic characteristics of commonly used electronics components are shown in Figure 1.2.

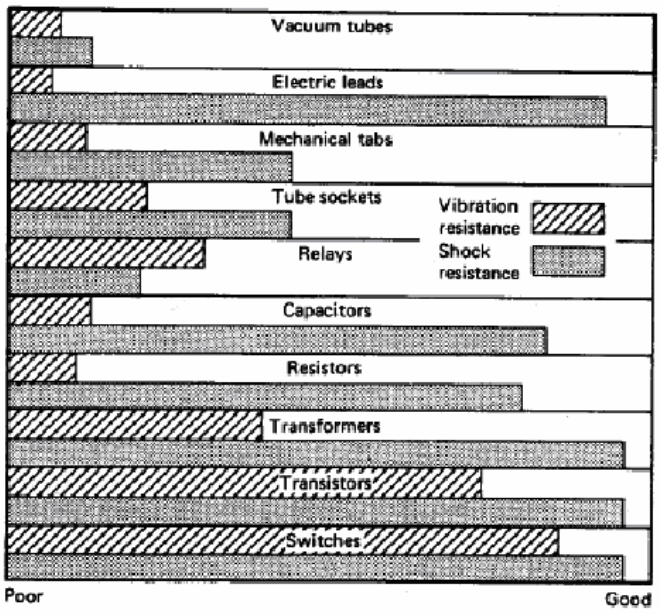


Figure 1.2: Relative dynamic resistance of common electronics components [4]

Most component failures in vibration will be due to the flexure (capacitors and resistors usually fail from flexure of the component leads or cracked solder joints [4]). These failures are caused by relative motion between the electronic component body, the electrical lead wires and the printed-circuit board (Figure 1.3).

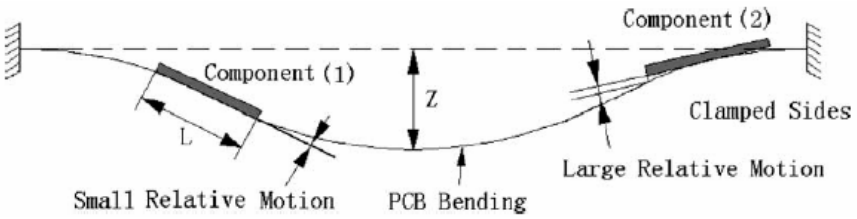


Figure 1.3: More rapid change of curvature results in more relative motion between the PCB and the components, which increases the stresses in the solder joints and reduces the fatigue life [5]

The relative motion is most severe during resonance. If the stress levels are high enough and the number of fatigue cycles is great enough then fatigue failures can be expected in the solder joints and/or lead wires of the electronic components.But if the component is cemented to the board the relative motion is reduced and the fatigue life in the solder joints and in the lead wires will be improved.

CHAPTER 2

LITERATURE SURVEY

Modern electronic equipment used in military applications must be able to survive vibration environment. The reliability of such equipment is defined by the ability of internal electronic components to survive vibration without developing mechanical fatigue. Therefore, scientists have been interested in developing methods of examining the mechanical fatigue of printed circuit boards.Below some of these studies are summarized.

Roberts and Stillo [6] used finite element modeling to analyze the vibration fatigue of ceramic capacitor's leads under random vibration. Barker et al. [7], Sidharth and Barker [8] proposed some analytical methods to estimate the vibration fatigue life of leaded surface mount components. Liguore et al. [9] and Fields et al. [10] studied vibration fatigue problems in leadless chip carrier. Ham and Lee [11] developed a fatigue-testing system to study the integrity of electronic packaging subjected to vibration. Jih and Jung [12] used finite element modeling to study the crack propagation in surface mount solder joints under vibration. Wong et al. [13] developed a model to estimate the vibration fatigue life of BGA solder joints.

W.W.Lee et al. [14] presented a review of fourteen solder joint fatigue models with an emphasis on summarizing the applications of each fatigue model. The models are classified into five categories: stress based, plastic strain-based, creep strain-based energy-based and damage-based. Each model is presented under one category with the applicable electronic packages. Following each category, common issues such as solder joint geometry and coverage are mentioned. Furthermore, two fatigue model application scenarios are discussed. In the first scenario, a set of existing fatigue test data is given to the engineer to determine how best to interpret the data and which fatigue model(s) best apply.

In the second one, a test scheme must be devised for a new product in order to determine the number of cycles to failure.

Q.J. Yang et al. [15] reported some work on characterization of plastic ball grid array (PBGA) assembly's dynamic properties. In this study, natural frequency and mode shapes of the BGA assembly of plastic ball grid array assemblies were identified by using experimental modal analysis and finite element analysis. In FE analysis, in order to overcome the difficulties caused by the complexity of PCB assemblies and limitation in computer resources, some techniques were developed. The bare PCB and PCB assembly with PBGA modules were tested and analyzed separately, so that the influence of PBGA modules on the PCB's dynamic properties could be identified. Furthermore, in order to assess the reliability of the PBGA assembly against vibration fatigue, constant-amplitude vibration fatigue testing (sine sweep tests around resonance) of the PBGA assembly with four PBGA modules were conducted and mean-time-to-failure (MTTF) of the PBGA assemblies were estimated. It was observed by using scanning electron microscopy (SEM) that the PBGA assembly was vulnerable to vibration, and fatigue failure always occurred at the corner solder balls of the PBGA module.

Thomas E. Renner [16] outlined a procedure where a finite element model of a circuit board was created incorporating laboratory test data. Force/deflection testing coupled with simple finite element models and static analysis were used to obtain the material properties and boundary conditions. Swept sine vibration testing along with modal and harmonic analyses were performed and the model was changed to match test data.

The information obtained consists of natural frequencies, stress contours and damping information. Finally set of trend (sensitivity) curves were presented that indicate how the natural frequencies change when parts of the circuit board are modified. To accomplish the tasks outlined above engineering analysis program ANYS Rev 4.1 was used.

R.Toroslu et.al [17] carried on to guide the design of the mechanical packaging which will protect the electronic components of a telemetry unit mounted in a 155 mm artillery projectile from high accelerations (shocks) reaching 1800g's.In this work, in order to simulate electronic components behavior under extremely high longitudinal and centrifugal accelerations, finite element models of the critical electronic components (diodes, transistors and capacitors) were created. Their natural frequencies and mode shapes were obtained by modal analysis. By linear transient dynamic analyses, the time varying stresses in the electronic components were investigated. The results of the dynamic analyses have shown that the stresses in the electronic components resulting from launching accelerations could well be investigated by static analyses. Besides the electronic components orientations in the mechanical packaging were decided.

H.Lau et.al [18] studied the mechanical integrity of surface mount technology (SMT) plastic leaded chip carrier (68-pin PLCC with copper J-leads) solder joints. The effects of printed circuit board (PCB) pad surface composition and testing temperature on solder joint reliability were pointed out. The failure of a solder joint was defined as 10% increase in the measured electrical resistance. In the present study, three sets of FR-4 epoxy/glass PCBs (a total of 90 boards) were tested, one with Cu-Ni- Sn pad surface metallurgy, one with Cu-Ni-Au, and one with SMOBC/SSC (Solder Mask Over Bare Copper/Selective Solder Coating, or simply, SMOBC). The solder composition was the 63wt%Sn/37wt%Pb. In this study, reliability of the solder joints was modeled by the Weibull distribution. The joints formed on Cu-Ni-Au and SMOBC boards were considerably more reliable than those formed on Cu-Ni-Sn board due to organic brighteners used in Sn plating. The gold was not anticipated to degrade the solder joint because it was below the 4 weight-percent level at which brittle fracture occurs

Some specific remarks were obtained:

- The solder joint fatigue crack starts near the tip of the outer solder fillet and propagates along the interface between J-lead and the solder joint.
- The mean lives at different temperatures of solder joints attached to Cu-Ni-Au PCB and SMOBC PCB were longer than those attached to Cu-Ni-Sn

PCB.The mean lives of solder joints attached to Cu-Ni-Au board and SMOBC board were almost the same.

- Higher temperatures reduce the fatigue life of the solder joints particularly above 60 C^{o}.

G.Mesmacque et.al [19] needed to propose a representative damage indicator model in return for the well known Miner's damage accumulation rule since Miner's rule does not take into account the loading history. For the same loading level the experimental results are higher than the Miner expectations for increasing loading and are lower than the Miner expectations for decreasing loading. In this new damage parameter model, damage is reported from one level of stress to the other and the damage stress which is taken as the stress corresponding to the residual life goes to the ultimate stress at the last cycle before failure. The model proposed in this work needs only the S-N curve .The stress field is considered in terms of equivalent Von Misses stress or in terms of maximum shear stress.In this way, the proposed model may be used in multi-axial loading conditions. In order to estimate the significance of the proposed model in life prediction, this new approach was confronted with the experimental results. Experimental results in the literature indicate that the proposed model takes into account the loading history and correctly assesses the fatigue life under different loading conditions.

Jingshu Wu et.al [20] studied the vibration analysis of medical devices by a finite element analysis (FEA) model calibrated with test data. The test structure is a plastic case that contains a printed circuit board with various attached electronic components such as capacitors, resistors and integrated circuits. In this study, an FEA model of the automatic external defibrillator is established with the use of ANSYS based on design specifications and static tests. The model is first calibrated with various static and dynamic tests in order to verify that the static displacements at selected locations of the PCB and first three natural frequencies predicted by the FEA model are consistent with those obtained by the tests. The model is then used to examine the vibration transmissibility of the PCB within both rigid and flexible medical device cases.

Finally; random vibration analysis ofthe PCB is presented. This study shows that the predicted frequency data favorably agrees with test data (within 7% error range), while predicted vibration amplitudes are in a reasonable range at major PCB locations when compared with the test data, but do not always agree well at the locations where the PCB has more complicated structural features and boundary conditions. The established FEA model predicts the reliability of the design of the AED from a vibration viewpoint. It can also help engineers improve the PCB mechanical design and product reliability when used in harsh vibration environments.

H.Wang et.al [5] studied high cycle fatigue induced by vibration. In this study series of fatigue experiments including PBGA256 and FCBGA1521 assembly were conducted. Firstly, proper mounting method of the test vehicles on the vibration shaker was determined based on the curvature of the circuit board defined by finite element analysis. Secondly, experimental modal analysis was used to identify the fundamental resonance frequency of the test vehicles. After that vibration fatigue tests were performed with a narrow band random excitation signal. During the tests the fatigue failure of each solder joint loop in the BGA assembly was recorded using a specially designed monitoring device.Moreover, after the fatigue tests solder joints were investigated using an optical microscope. After the analysis, some concluding remarks were achieved:

- Solder joints fatigue is related to the BGA location (curvature of the PCB) in PCB. Generally solder joints in the inside loop of the BGA assembly are not sensitive to vibration fatigue.
- Solder joints fatigue in the same loop of the BGA assembly are different due to different locations. Generally solder joints in the corner position are easier to be in failure condition than the other joints in the loop that is, the outside loop has larger relative displacement than the inside loop.
- Solder joints have different damage even if they are symmetric within the BGA assembly.
- Finally, although the boundary conditions of the PCB and the input loading were the same, the maximum displacement of the both assemblies (PBGA

& FCBGA1521 assembly) wasn't same since the mass, stiffness shape and the numbers of solder joints were different.

Q.Guo et.al [21] performed a series of vibration fatigue experiments including plastic ball grid array assembly in order to obtain a random fatigue semi-experimental model of surface mount technology (SMT) solder joint using random vibration theory. According to linear Miner fatigue damage accumulation theory, damage estimation formula was obtained considering the narrow band random process without taking the plastic deformation of the solder joint into account. In order to obtain the material constants in this formula, tests results were also used. By rearranging this formula semi experimental model for estimating solder joints fatigue lifetime was obtained. Compared with random vibration test results, the semi experimental model results were good enough to predict solder joints fatigue.

D.Barker & Y.Chen [22] studied the determination of natural frequency of the printed wiring board (PWB) in its working environment. The importance of accurate identification of the natural frequency in determining the vibration fatigue damage is stressed. It is also pointed out that the most important variable in determining the natural frequency of PWB's is the type of support provided by the edge guides of the PWB. The classical types of support (free, simple, or clamped) are assumed to exist at the edges of the PWB. However, in reality, edge guides limit translation and rotation but can not completely eliminate either. Therefore, it is stated that the actual natural frequency of a PWB falls somewhere between the values obtained for simply supported boundary condition and clamped (fixed) support boundary condition.

This study focuses on how commonly used wedge-lock edge guide's affect the natural frequency of a PWB. The wedge-lock edge guides were modeled as being rigid in translation but elastic in rotation. Since the edge guides are assumed to be elastic in rotation, they were modeled as rotational springs. Vibration tests were conducted on a variety of edge guides. The analyses of the edge guide test data with finite element analysis allowed the calculation of corresponding rotational spring constants.Values for rotational spring constants were then integrated into

plots to establish look-up tables to determine the spring constant in any environment. This research is critical to the accurate modeling and design of PWB natural frequency.

D. Barker, Y. Chen and A. Dasgupta [23] developed an algorithm for predicting the vibration fatigue lives of electronic components mounted on a printed wiring board (PWB) during the system design stage. The algorithm is based on accurately modeling the PWB's boundary supports so that the natural frequencies and mode shapes can be determined. The PWB's deflection and it's radius of curvature can then be calculated for the prescribed random vibration loading condition. The solder joint stresses are then obtained by applying force equilibrium on a component mounted on the PWB. Basquins high cycle fatigue relation is then used to determine the fatigue life of the components. The method can be implemented on computer as a design tool. In order to more accurately model a PWB's boundary conditions, an experimental program was conducted to evaluate the restraint offered by commonly used wedge lock card guides. A simple analytical solution to approximate the attach deflection from the local radius of curvature of the PWB was derived. For simplifying the definition of the deformed PWB geometry, some assumptions were made. The effects of these assumptions were studied by comparing the analytical results with the finite element analysis solutions. After comparing the results with FEM results, the algorithm was improved.

J. Starr [24] has been working out the vibration life capabilities of electronic components. He describes the vibration testing as an important part of producing quality electronics through accelerated life testing.It is also underlined that for modern electronic systems, vibration life capabilities are dominated by flexure cycles of the components.The stresses occurring at critical points within the components, leads solder, etc., determine the life capabilities of the system.

In this work, it is also emphasized that the most commonly used formulation which defines the limitations on displacement for a circuit card exposed to vibration has bad form for extrapolation across design generations of electronics.

It is noted that as companies found the empirical formula failed in many systems, detailed finite element analysis (FEA) have been used extensively. Finally it is recommended to use of analysis to quantify and extrapolate test results since analysis is subject to high error (due to unknowns and modeling approximations) while test results accurately defining life.

I. Sharif [25] has been working on the interconnection reliability of surface mount leaded components. In this study methodology for computation of lead stiffness and prediction of fatigue life of the leaded surface mount components were developed. Finite element analyses was used to obtain stiffness matrices for both the plastic quad flat package (PQFP) gull wing and plastic leadless chip carrier (PLCC) J leads and solder joints. This stiffness was then used in fatigue life prediction equations to estimate the fatigue life. Moreover, variability's in lead and package dimensions provided by different vendors, were identified and their effects on solder joint fatigue life were studied with the help of finite element analyses. The effect of change in lead length, height, width and thickness on the lead stiffness and solder joint fatigue life for both the PQFP and PLCC components were studied. Finally recommendations were made in order to obtain a better control on component fatigue life.

Bishop [26] has been involved in developing new fatigue analysis theories and structural analysis techniques in the frequency domain. He performed some design applications in finite element environment by using time domain and frequency domain fatigue methods. It is pointed out that, time domain approach lacked the dynamics of the structure if the analysis is performed by assuming that the loading is statically applied. Furthermore in order to include the dynamics of the structure in the time domain, a transient dynamic analysis has to be performed which is very time consuming and sometimes practically impossible. Instead of the time domain methods, a more computationally efficient spectral method using the random vibration theory can be used. The benchmarks represented showed that spectral methods and transient dynamics method results were consistent and accurate enough for numerical analysis.

W.F. Wu et al. [27] investigated the applicability of methods proposed for the estimation of fatigue damage and life of components under random loading. Palmgren-Miner and Morrow's plastic work interaction rule which take into account the stress sequence effect were investigated and verified by strain controlled low cycle fatigue tests of 7075-T651 aluminum alloy. From the test results it was shown that Morrow's plastic work interaction damage rule works much better than the widely used Palmgren-Miner's linear damage rule. The fatigue damage estimated based on the Morrow's plastic work interaction damage rule was found to be more conservative. It can also be concluded from the test results that fatigue lives of test specimens can be fitted by normal (Gaussian) probability density function.

H.Y. Liou et al. [28] studied damage accumulation rules and fatigue life estimation methods for components subjected to random vibration loading. In this study, random vibration theory was used to estimate the fatigue life and fatigue damage with Morrow's plastic work interaction damage rule. Experimental work was carried out to verify the derived formulas. From fatigue tests the damage results were compared with the traditional cycle by cycle counting method. The results showed that the prediction of Morrow's plastic work interaction damage is even more accurate as compared with cycle-by-cycle calculation. The degree of accuracy of Morrow's method depends strongly on the selection of an appropriate plastic work interaction exponent. But the iterative process required to find out the plastic work exponent which accounts for the material's sensitivity to the variable amplitude loading is one of the reasons why Palmgren-Miner's damage rule is more preferred.

Nathan J. Blattau [29] has proposed an approach in which the "stiffness method" will be used in conjunction with Calce PWA software and commercial finite element analysis software to generate more capable stress analysis models for rapidly assessing the durability of surface mount components during circuit board bending. The durability of the component will be determined by finding the various overstress limits for the materials used in its construction through experimental data and finite element analysis.

Calce PWA will be used to attain the printed wiring board curvatures for the applied loading conditions. These curvatures will then be converted into the moments applied to the component.Then, the stiffness method or analytical models will be used to convert the applied moment into the forces and moments seen in the various parts of the component. Converting these loads into stresses and comparing them to the previously attained overstress limits will determine whether the component has failed and where the failure is located.

D.Haller et al. [30] mentioned the capabilities of the software PCB-FEA sponsored by Bayern Innovative and Siemens. It represents a link between board station (Mentor Graphics) and ANSYS. It is noted that all ANSYS capabilities for solution and post processing are available and the program can be started within ANSYS. Layout data are transferred automatically into a finite element model in ANSYS by means of a database, containing a component library, material data and other information for further mechanical and thermal analyses of the PCB's. Furthermore it is stated that FEM models of numerous types of frequently used packages are stored in the program.

R.E.Colyer [31] worked on the practical techniques of reliability assurance of high technology equipments. In this study it is pointed out that the evidence of reliability should be obtained either from data accumulated from use in real life or from extensive tests under representative operating conditions. In addition, accelerated-life testing as used in step-stress testing (SST) which involves the application of gradually increasing the stresses applied to components to levels above those experienced during normal operating conditions was pointed out.

Consequently, it can be concluded that finite element modeling is widely used to analyze vibration fatigue failures of electronic components mounted on the PCBs. Furthermore, there are limited numbers of commercial finite element analysis software for analyzing PCB fatigue failure. Moreover finite element analysis must be calibrated with test data since the analysis alone is subject to error.

Besides, frequency domain approach is computationally more efficient and requires less time than the traditional time domain approach. In addition, although PBGA components are expensive they have been tested frequently therefore this component class can be considered as a vulnerable component to vibration and should be tested in the future. Finally, there isn't any database comprising fatigue lives of electronic components in the market. Therefore firms in electronic industry should build up their own database.

CHAPTER 3

FATIGUE ANALYSIS THEORY

Fatigue damage is a process which causes premature failure of a component subjected to repeated loading. It is a complicated process which is difficult to accurately describe and model. Despite these complexities, fatigue damage assessment for design of structures must be made. Therefore fatigue analysis methods have been developed.

In this chapter the application of the stress-life method used in the thesis will be explained. As mentioned before, fatigue can be approached in several ways and in particular by three main methods: These are stress- life approach, strain-life approach and the fracture mechanics (study of the crack propagation rate) approach.

3.1 Stress Life Approach

The S-N approach is still the most widely used in design applications where the applied stress is primarily within the elastic range of the material and the resultant lives (number of cycles to failure) are long.The basis of the stress-life method is the Wöhler or S-N diagram, which is a plot of alternating stress, S, versus cycles to failure N. The most common procedure for generating the S-N data is the rotating-bending test. Tests are also frequently conducted using alternating uniaxial tension- compression stress cycles. A large number of tests are run at each stress level of interest, and the results are statistically massaged to determine the expected number of cycles to failure at that stress level. Taking into account the great variations of N with S; data are plotted as stress S versus the logarithm of the number N of cycles to failure. The values of S are taken as alternating stress

amplitudes; S_a sometimes $S_{\max}$ values can also be used. Curves can be derived for smooth specimens, individual components, sub-assemblies or complete structures. Figure 3.1 is an example of a typical fatigue life curve.

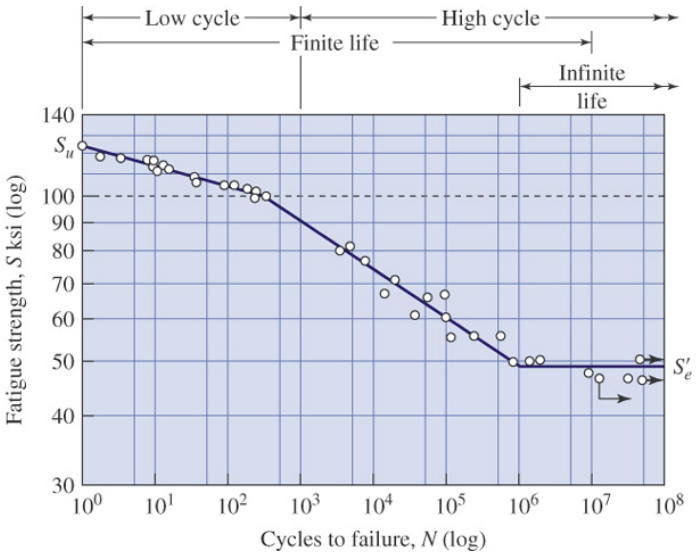


Figure 3.1: S-N diagram for UNS G41300 steel [32]

For some ferrous (iron base) alloys, the S-N curve becomes horizontal at higher N values; or, there is a limiting stress level, called the *fatigue limit* (also called *endurance limit*), below which there is never failure by fatigue whatever the number of cycles is applied. Below this stress level material has an "infinite" life. For engineering purposes, this infinite life is usually considered to be 1 million cycles [33]. Furthermore, for many steels, fatigue limits range between 35-60% of the tensile strength [34]. In the case of nonferrous alloys (aluminum, copper, magnesium, etc.) however the true endurance limit is not clearly defined and the S-N curve has a continuous slope. Thus fatigue will certainly occur regardless of the magnitude of the stress. In such cases it is common practice to define a" pseudo-endurance limit" for these materials which is taken as the stress value corresponding to life of 5×10^8 cycles for aluminum alloys [33] (Figure 3.2).

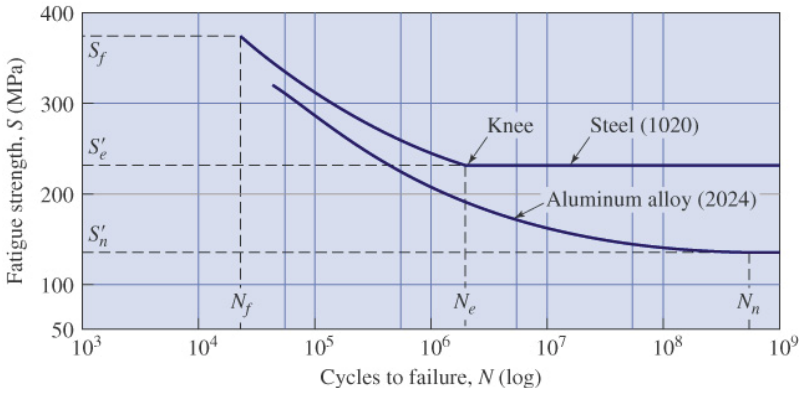


Figure 3.2: S-N data of steel and aluminum [35]

In actual operation the shape of the stress-time pattern takes many forms. Perhaps the simplest fatigue stress spectrum to which a structure may be subjected is a zero mean sinusoidal stress-time pattern of constant amplitude and fixed frequency, applied for a specific number of cycles, often referred to as a completely reversed cyclic stress, illustrated in Figure 3.3a**.** A second type of stress-time pattern often encountered is the nonzero mean spectrum shown in Figure 3.3b.

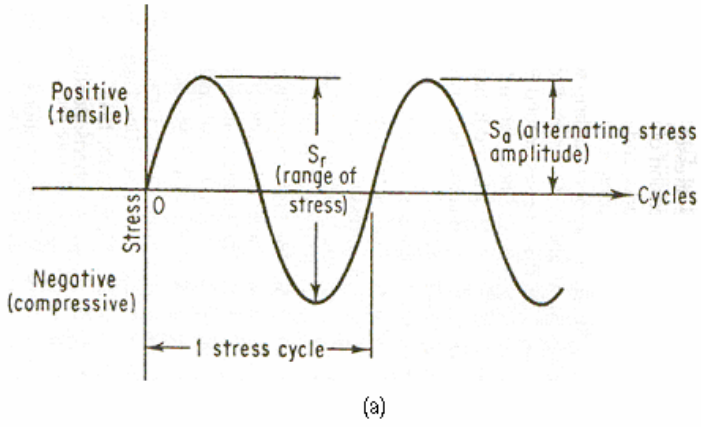


Figure 3.3: Sinusoidal fluctuating stresses, a) with zero mean (fully reversed) [36]

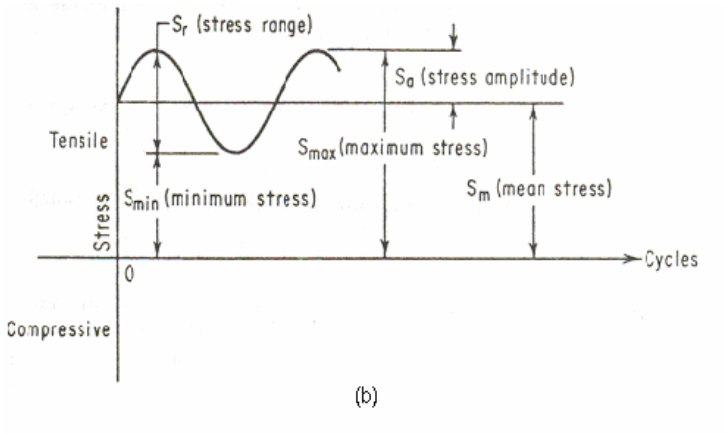


Figure3.3 (continued): Sinusoidal fluctuating stresses, b) with nonzero mean [36]

$S_a, S_r, S_m, S_{\max}$ and $S_{\min}$ are defined in Figure 3.3a and Figure 3.3b.The following relationships and definitions are defined when discussing cyclic loading:

R : Stress ratio, $S_{\min} / S_{\max}$ (3.1)

A : Amplitude ratio, S_a / S_m (3.2)

Although stress components have been defined by using a sinusoidal stress, the exact shape of the stress versus time curve does not appear to be of particular significance. Most of the time, random type loading is present in mechanical systems.

In place of the graphical approach a power relationship can be used to estimate the S-N curves. The relation suggested by Basquin in 1910 is in the form

$$N.S^b = C \tag{3.3}$$

Where;

N : The number of cycles to failure at stress level, S

S : Stress amplitude

b : Stress (Basquin) exponent

C : Constant

In the above expression the stress tends towards zero when N tends towards the infinite. This relation is thus representative of the *S-N* curve only in intermediate zone (high cycle region) between infinite life and low cycle.

The range of variation of b is between 3 and 25 for the metals. However the most common values are between 3 and 10 [33]. M.Gertel and C.E.Crede, E.J.Lunney proposed a value of 9 to be representative of the most materials. This led to the choice of 9 by such standards as MIL-STD-810, etc. This value is satisfactory for copper and most light alloys but it may be unsuitable for other materials. For example, for steels, the value of b varies between 10 and 14 depending on the alloy. Therefore it is necessary to be very careful in choosing the value of this parameter (average value) especially when reducing test times for constant fatigue damage testing (qualification tests) [33] [37].

The relation between the stress exponent b is related to the slope of the S-N curve by

$$b = 1/\log_{10}(slope) \tag{3.4}$$

Due to the exponential nature of the *S-N* relationship, slight change in stress can cause considerable change in fatigue life. For example if b is taken as 10, which is an approximate value for the soft solder (63-37 Tin-Lead), then if the stress level is increased by a factor of 2, fatigue life will be reduced by a factor of 10^3.

Fatigue life depends primarily on the amplitude of stress or strain but this is modified by the mean value of stress existing in the component.Many components carry some form of "*dead load*" before the working stresses are applied, and some way of allowing for this is then needed. The magnitude of the mean stress has an important influence on the fatigue behavior of the specimen particularly when the mean stress is relatively large compared to alternating stress. The influence of mean stress on fatigue failure is different for compressive mean stress values than for tensile mean stress values.

In the tensile mean stress region, the allowable amplitude of alternating fatigue stress gets smaller as the mean stress becomes more tensile whereas in the compressive mean stress region, failure is rather insensitive to the magnitude of the mean stress and fatigue life increases to a lesser extent.

Moreover the influence of mean stress in the compressive region is greater for shorter lives than for longer lives [38] such that if the stresses are enough large to produce significant repeated plastic strains as in the low cycle fatigue, the mean stress is quickly released and its effect can be weak [39][40].

S-N curves of material when there is nonzero mean stress can be represented by plotting S_a versus N for various values of S_m. Empirical relations are then derived in accordance with S_m for the constants "C" and "b" of the Basquin's relation $N.S^b = C$. Tensile mean stress existing in the structure reduces the endurance limit of the system as shown in Figure 3.4.

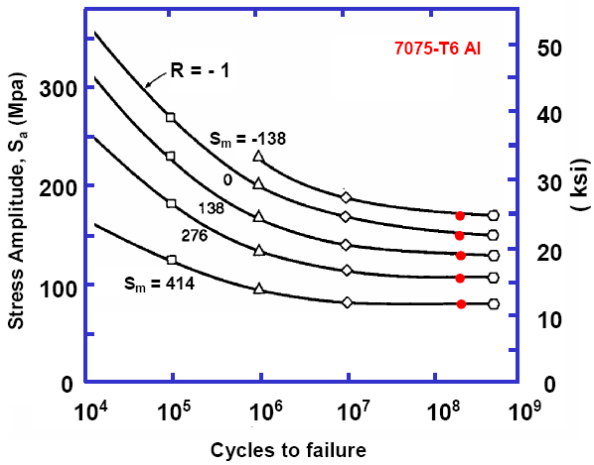


Figure 3.4: Example of S-N curve with non zero mean stress [41]

The application of static stress led to a reduction in S_a as stated above. It is thus interesting to know the variations of S_a with S_m.

Several empirical relationships that relate failure at a given life under nonzero mean conditions to failure at the same life under zero mean cyclic stresses have been developed.

These methods use various curves to connect the fatigue limit on the alternating stress axis to either the yield strength, ultimate strength, or the true fracture stress on the mean stress axis. By using these methods, for finite-life calculations, the endurance limit can be replaced with purely alternating stress (zero mean stress) level corresponding to the same life as that obtained with the stress condition S_a and S_m .The value for this fully reversed alternating stress can then be entered on the S-N diagram to obtain the life of the component.

However in order to be able to use these emprical approaches it is required that stress versus time information must be known so that one can analyze the data using rainflow cycle counting method.This is practically subtle for structures like PCB's because in order to get stress history one must use strain gages. However using strain gages is almost impractical because it can not be posted to leadwires or the solders of the electronic components on the PCB. Therefore frequency domain method will be used instead of time domain approach to analyze the PCB fatigue failures.

3.2 Printed Circuit Board Frequency Domain Fatigue Approach

In the frequency domain vibration fatigue analysis of the printed circuit boards, CirVibe software, specially built package, for the electronic circuit card assembly fatigue analysis is used. The details of the vibration fatigue life prediction approach are outlined in Figure 3.5 below:

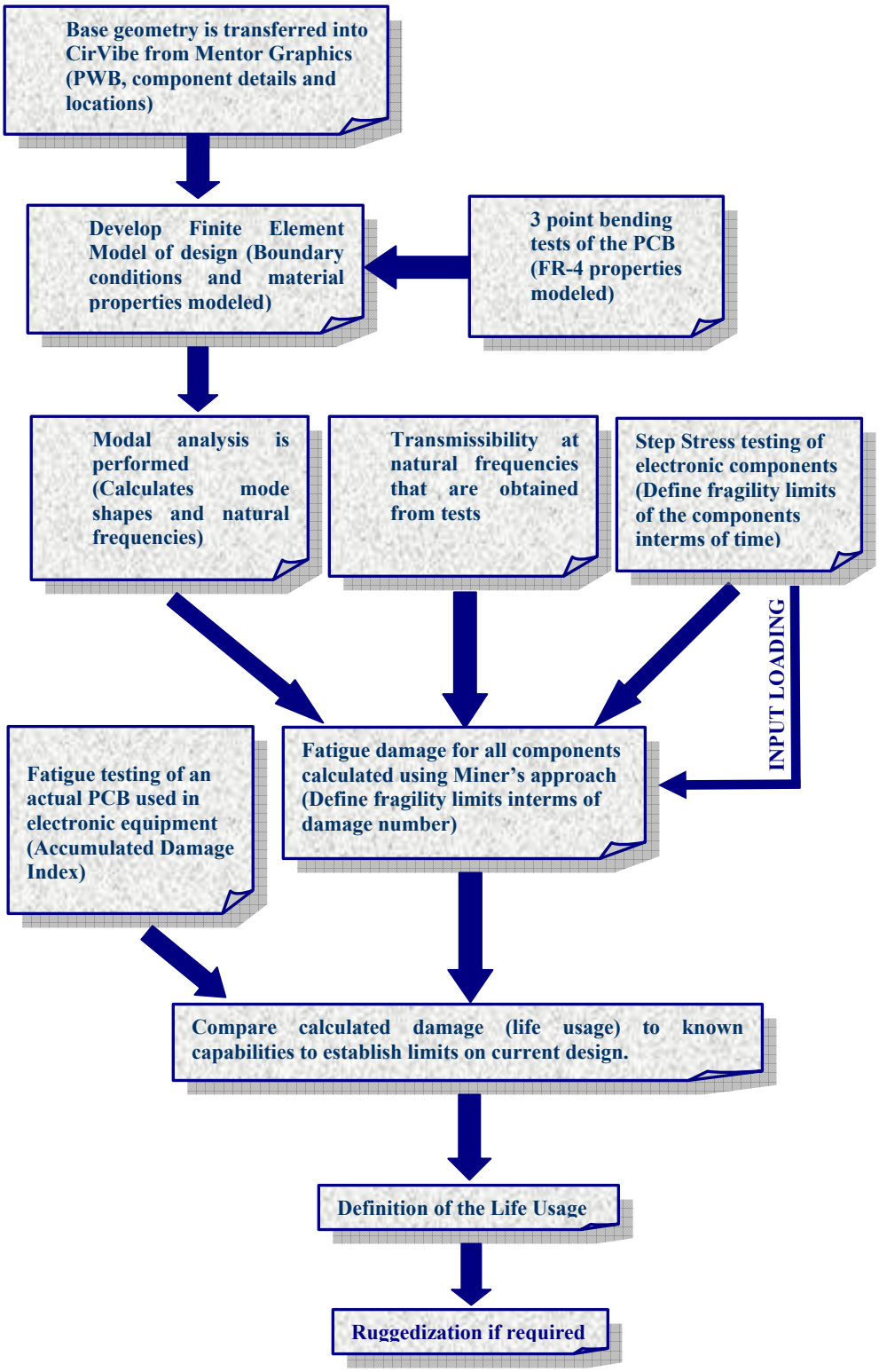


Figure 3.5: Schematic representation of analysis process used in the thesis work

Finite Element based tools for fatigue life prediction are now widely available. It is necessary to define vibration induced fatigue as the estimation of fatigue life when the stress histories obtained from the structure or components are random in nature.

There are several alternative ways of specifying the same random process. Fourier analysis allows any random loading history of finite length to be represented using a set of sine wave functions, each having a unique set of values for amplitude, frequency and phase. It is still time based and therefore specified in the time domain. As an extension of Fourier analysis, Fourier transforms allow any process to be represented using a spectral formulation such as a *Power Spectral Density* (PSD**)** functions. It is described as a function of frequency and is therefore said to be in the *frequency domain* (Figure 3.6). It is still a random specification of the function. In a frequency domain representation, it is possible to see trends that would be impossible to identify in the time domain.For example natural frequencies of vibration are easily detected.

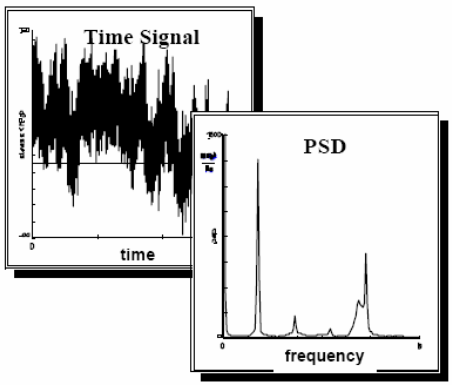


Figure 3.6: Random processes [42]

Random vibrations are generally represented by power spectral density functions in frequency domain. Many design standards give data on random processes in the form of power spectral density functions (PSD). In order to obtain the PSD of the input loading, first of all it is necessary to transform the loading input in the time

domain in to the frequency domain. This is achieved by Fourier series representation. In practice however, time histories will be recorded digitally by a computer in a discrete format .Therefore what is really needed is a discrete version of the Fourier transform pair which can be applied to real, digitally recorded data. The discrete transform pair does the same job as the Fourier transform pair but operates on digitally recorded data. A very rapid discrete Fourier transform algorithm was developed in 1965, by Cooley and Tukey, known as the 'Fast Fourier Transform' (or FFT) [42] (Figure 3.7).

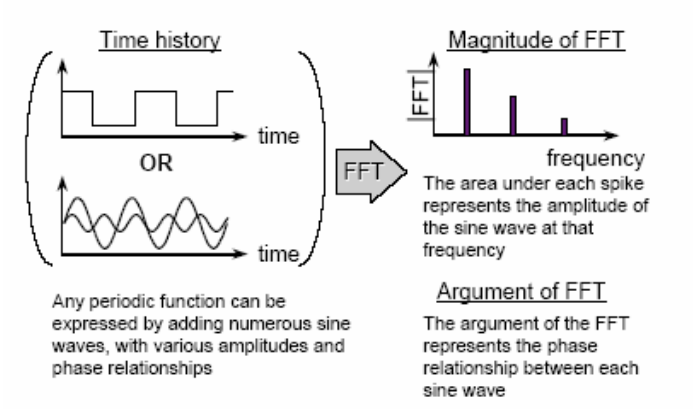


Figure 3.7: Using an FFT to characterize a time signal [42]

PSDs are obtained by taking the modulus squared of the Fast Fourier Transform (FFT). The PSD is a statistical way of representing the amplitude content of a signal. The FFT outputs a complex number given with respect to frequency but in a PSD only the amplitude of each sine wave is retained (Figure 3.8). In the definition of the PSD given in Figure 3.8 T stands for the sample period which can also be defined as $1/f_s$, f_s being the sampling frequency of the recorded signal. All phase information is discarded. In most engineering situations it is only the amplitude of the various sine waves that is of interest. In fact, in many cases it is found that the initial phase angle is totally random, and so it is unnecessary to show it.

For this reason the PSD function alone is usually used. In CirVibe the input loading is also defined in the form of PSD.The user enters random loading point to point. One very useful characteristic can be calculated directly from the PSD is the so-called *root mean square (rms)* value of the input loading. It is defined as the square root of the area under the PSD curve.

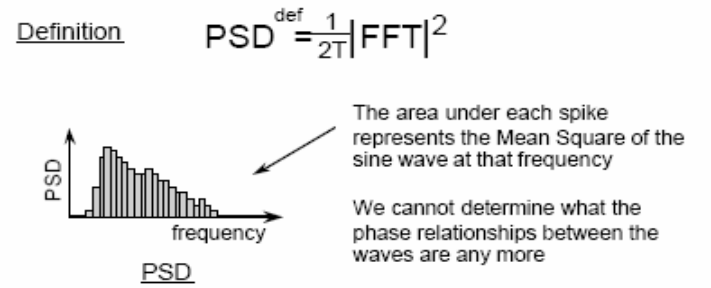


Figure 3.8: Definition of PSD [42]

In order to predict the probable stress (or acceleration levels) the equipment will see in the random vibration environment, it is necessary to understand the probability density functions (pdf). Calculation of damage under random vibration performed in the CirVibe is based on a Rayleigh probability density function [26] (Figure 3.9)

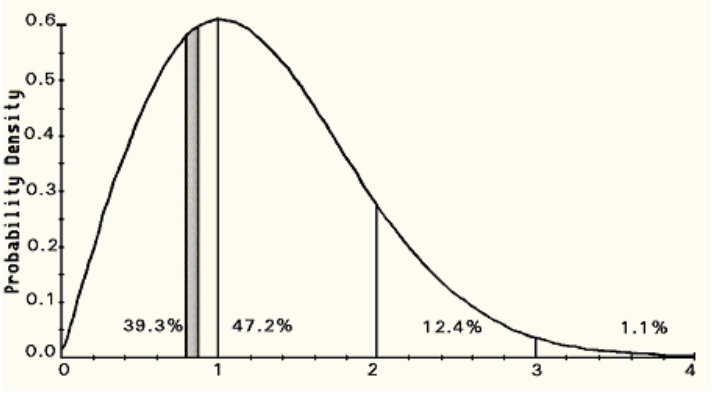


Figure 3.9: Rayleigh Probability Distribution of Cycled Peak Stresses [43]

It is the true peak response (random response) distribution. The total area under the curve is equal to unity. The area under the curve between any two points represents the probability that peak stress (acceleration) amplitude will be between these two points.

The Rayleigh distribution shows the following relations:

- Peak stresses (accelerations) will exceed the 1σ level 60.7% of the time.
- Peak stresses (accelerations) will exceed the 2σ level 13.5% of the time.
- Peak stresses (accelerations) will exceed the 3σ level 1.2% of the time.
- Peak stresses (accelerations) will exceed the 4σ level 0.03% of the time where σ represents the root mean square (rms) value of the stress (or acceleration)

Every structural member has a useful fatigue life and that every stress cycle uses up a part of this life. When enough stress cycles have been accumulated, the effective life is used up and the component will fail. Component damage calculation in CirVibe uses Miner's rule. Miner [34] suggested the use of a damage fraction D to determine the fraction of the life that is used up. This ratio compares the actual number of stress cycles, n, at a specific stress level, to the number of cycles, N, required to produce a failure at the same stress level, using an alternating stress. The linear damage rule states that the damage fraction, D_i at stress level S_i is equal to the cycle ratio n_i / N_i.

The failure criterion for variable amplitude loading can now be predicted when

$$\frac{n_1}{N_1}+\frac{n_2}{N_2}+\frac{n_3}{N_4}+...+\frac{n_k}{N_k}\geq 1 \quad \text{or} \quad \sum_{i=1}^{i=k}\frac{n_i}{N_i}\geq 1 \tag{3.5}$$

Considerable test data have been generated in an attempt to verify Miner's rule. The results of Miner's original tests showed that the cycle ratio corresponding to failure often ranged from 0.25 to about 4. In most cases the average value is close to Miner's proposed value of 1.

Tests using random histories with several stress levels show very good correlation with Miner's rule [34]. An alternative form of Miner's rule has been proposed which is represented by

$$\sum \frac{n_i}{N_i} \geq X \tag{3.6}$$

where X is selected on a desired factory of safety. A value less than 1 is usually used. For example fatigue-cycle ratios of 0.7 (for typical electronic structures) have been proposed to determine the useful life of a structure when weight is important [3].The linear damage rule has two main shortcomings:

- It does not consider load sequence effects. The theory predicts that the damage caused by a stress cycle is independent of where it occurs in the load history.
- The linear damage rule is amplitude independent. It predicts that the rate of damage accumulation is independent of stress level. However this last trend does not correspond to observed behavior.

Based on a survey of experimental results, many nonlinear damage theories have been proposed to overcome the shortcomings of Miner's rule. However, there are some practical problems involved when trying to use these methods: Firstly, they require material and shaping constants which must be determined from series of tests. Secondly, in some cases this requires considerable amount of time.

Thirdly, some of the methods take into account the load sequence effects, the number of calculations can become a problem in complicated load histories.

These theories do not give significantly more reliable life predictions and require also material and shaping constants which may not be available. Therefore, for most situations, Miner's rule is still considered to be simplest, most general and the most widely used by far [34] and often sufficiently accurate in predicting the fatigue life of a structure. The error associated with the precision of the fatigue life

estimates by Miner's rule depends on the rule itself, but also on the precision of the S-N curve used [44].

CirVibe uses the maximum lead wire stress for each component to define the damage for that component.

Lead wire stress is the sum of the axial stress plus the bending stresses from each of two bending moments. This stress is usually the highest in end or corner lead wires. CirVibe allows the user to include stress concentration factors for each of the contributions to the stress. The stress used in the calculation is determined by [43]:

$$\sigma_{tot} = K_0 P_{leadwire} / A_{leadwire} + K_1 M_X c_1 / I_1 + K_2 M_Y c_2 \tag{3.7}$$

The default stress concentration factors K_0 to K_2 are 1.0 (all stress contributions to failure are equal). *K* is usually taken between 1.5 and 2 but there is little data available to justify these choices.Therefore stress concentration factors effects are implicitly included into the fatigue analysis by the failure time observed in the step stress tests.

CirVibe generates shell mesh automatically in FEM and evaluates the modified modulus to account for the added stiffness of the components [43].

Under random vibration, all vibration modes will be excited simultaneously. Stresses from multiple modes superimpose, enhancing the damage rate that would be experienced if driven by individual mode stresses. The one sigma level response can be approximated using Miles equation [45] which estimates the RMS response of the mass to a broad band vibration. Miles' Equation used by CirVibe calculates the square root of the area under the response curve, providing the G_{RMS} value for the first 7 modes of the circuit board.

$$G_{rms} = \sqrt{\frac{\pi}{2} . PSD_{input} . f_n . Q_n} \tag{3.8}$$

Where;

G_{rms} : Output RMS acceleration in G's.

f_n : Natural frequency

Q_n : Transmissibility at resonance

PSD_{input} : Input acceleration spectral density in units of G^2 / Hz at f_n .

There are some important points about the uses of Miles' equation which should be pointed out:

- Mile's equation is based on the response of a SDOF system subjected to a flat random input (white noise input). However it can be used to describe stresses for a multi-degree of freedom systems if the natural frequencies are well separated
- Mile's equation is valid when the random vibration PSD input is flat in the area of resonance. This demonstrates that Miles' Equation is best used when the input PSD is flat or nearly so [46]. Yet the amount of error is small even when the slope of the random-vibration input curve is 6 dB/octave (in other words slope value of 2, which is represented by an angle of 63.4°).Therefore it can be used to obtain good results under most conditions [3].

CirVibe damage calculation includes 0 to 7 sigma stress levels.It is performed for each mode of the circuit board. The damage calculation post processor sums incremental damage over the distribution of the response peaks (Rayleigh distribution) by dividing experienced cycles by normalized allowable cycles. The integration of damage of a continuous distribution is performed over 0.001 sigma increments. The root mean square (RMS) stress equals 1 sigma stress. The area under the Rayleigh pdf between points $sigma_1$ and $sigma_2$ represents the probability that a peak amplitude will be between these two points.The number of cycles experienced at each stress level is calculated from the total test time multiplied by the natural frequency and the probability factor. Consequently, the number of cycles experienced in the response range is given by [43]:

$$n = (total \quad test \quad time) \times \mathrm{P}(sigma_1, sigma_2) \times f_n \tag{3.9}$$

Where;

$\mathrm{P}(sigma_1, sigma_2)$: Probability that a peak will be between [$sigma_1.RMS$] and [$sigma_2.RMS$].

Using the normalized fatigue curve, response level at each integration increment determines "*N*", the allowable number of cycles which can be determined from the following relationship [43]:

Response level (peak acceleration) = $G_{rms} \times (sigma_1 + sigma_2)/2$ (3.10)

Damage is summed over the distribution to determine the total damage for the random input loading. CirVibe always calculates the factored individual mode damage as well as root-sum-square (RSS) damage. RSS is a statistical method of combining distributions. For multiple mode damage contributions, RSS stress which is the means of adding a stress from multiple modes is used [43].

$$RSS = \sqrt{\sum_{i=1}^{n} (RMS_i)^2} \tag{3.11}$$

Where;

RMS_i: 1.0 sigma RMS stress for the i.th mode and

n: the number of modes driven by the input excitation

The damage calculation for the multiple mode contributions (RSS damage) uses a single damage integration using the RSS stress as the "1 sigma" response level combined with the natural frequency of the dominate mode (frequency of the highest stress contributor) for count of applied number of cycles because the stress in the most critical component is usually dominated by one mode of the PCB [43]. The RSS damage calculation assumes that the stresses are occurring at the same instant in time. Therefore, the RSS includes stresses for all modes of a requirement

and calculates the damage for that RSS combination of stresses. It does this for each input loading and sums the damage of all the input loadings.The summation of damage, calculated from each individual mode would underestimate the damage experienced. For the most of the components, the damage tends to be dominated by one mode. In addition, the damage numbers from different modes aren't likely to be the highest at the same point so they are not truly additive. Therefore damage can be considered to be at least as great as the damage from the dominate mode, but not quite as great as the RSS damage value. The RSS value is however the best estimate for defining the component capability.

3.3 Lead Wire Stresses on Vibrating Printed Circuit Boards

When the circuit board vibrates, the components mounted on the circuit board are subjected to the stresses from two different sources: First, the mass of the component is subjected to an acceleration that produces a force P ($P(t) = T_r * m_{comp} * a_{in}(t)$) normal to the plane of the board (Figure 3.10a) where m_{comp} is the mass of the component, $a_{in}(t)$ represents the input vibration acceleration and T_r is the transmissibility ratio. The transmissibility ratio can be obtained from vibration testing for each mode of the PCB.

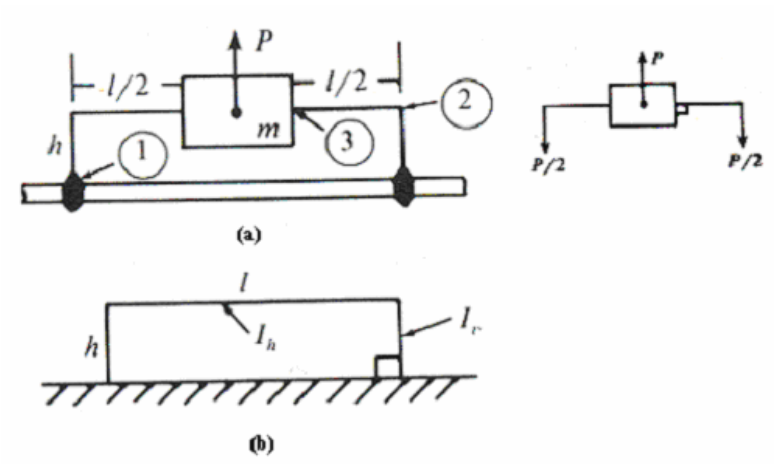


Figure 3.10: Modeling an axial leaded component with a wire frame. (a) Load *P* due to input acceleration. (b) The wire frame representation [2].

The body of the component is kept in equilibrium with reaction forces developed in the lead wires. Secondly, the surface of the circuit board flexes which causes the leads bend back and forth at their junctions with the board.

Components with lead wires such as capacitors or DIPs can be modeled as frames. The body of the component is very rigid compared to the lead wire so that it can be assumed that deflection of the component is due entirely to the deformation of the lead wires. Leads are soldered to the PCB and reinforced with solder fillet hence the leads can be assumed to be built-in when defining the boundary conditions for the frame. Loads are produced by both input acceleration and circuit board flexure. Therefore problem can be considered to be superposition of two cases as shown in Figure 3.11.

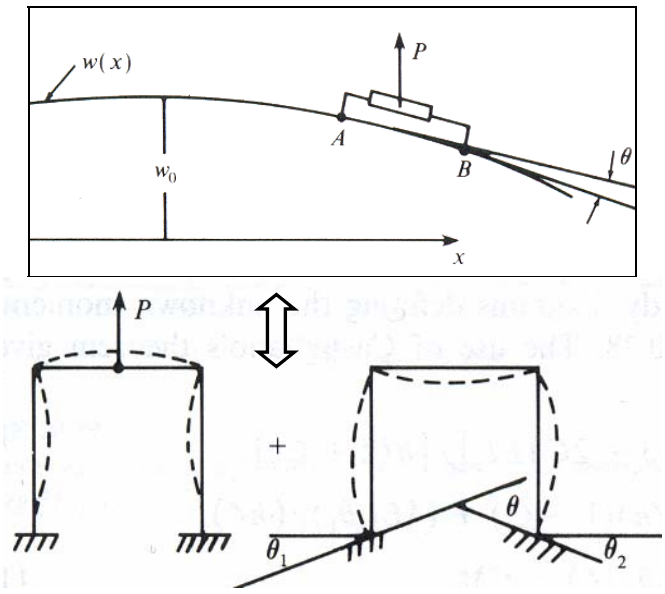


Figure 3.11: Circuit board component interaction and superposition of the lead wire stress [2]

In the above figure the relative rotation of the leads (depends on the boundary conditions of the PCB) θ is given by;

$$\theta = \theta_B - \theta_A = \left(\partial\omega/\partial x\right)_B - \left(\partial\omega/\partial x\right)_A \tag{3.12}$$

Considering the wire frame with the central load P unknown reactions and moments can be evaluated by using Castigliano's theorem. The free-body diagrams presented in Figure 3.12 define the unknown reactions.

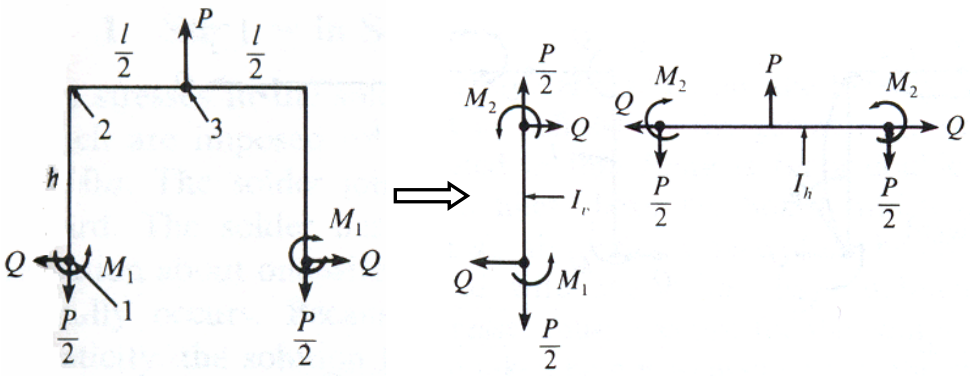


Figure 3.12: Free-body diagram of a wire frame with the load P [2].

The results for the frame subjected to the load P defined in Figure 3.12 are

$$Q^P = \left(3Pl\right)/\left[8h\left(C+2\right)\right] \tag{3.13}$$

$$M_1^P = \left(Pl/8\right)\left(C+2\right) \tag{3.14}$$

$$M_2^P = \left(Pl/4\right)\left(C+2\right) \tag{3.15}$$

$$M_3^P = \left(Pl/2\right)\left(C+1\right)/\left(C+2\right) \tag{3.16}$$

$$\delta_3^P = \left[Pl^3/(96EI_h)\right]\left[\left(C+1\right)/\left(C+2\right)\right] \tag{3.17}$$

Where;

$$C = \left(h/l\right)\left(I_h/I_v\right) \tag{3.18}$$

I_h: is the area moment of inertia of the horizontal portion including the lead and the component body

I_v : is the area moment of inertia of the vertical lead portion

In the above equations, Q^P denotes the shear force at the built-in end (critical point 1), M_1^P represents the reaction moment at the built-in end (critical point 1), M_2^P and M_3^P represent the reaction moments at the critical locations 2 & 3 respectively. In addition, δ_3^P is the vertical deflection (component deflection) at point 3 due to the force *P*. All the moments, forces and displacements are time dependent (have random characteristics if $a(t)$ has random nature). The worst case situation for the leads rotation θ (Figure 3.13) (relative rotation of the leads) occurs when the component is placed at the center line of the PCB.

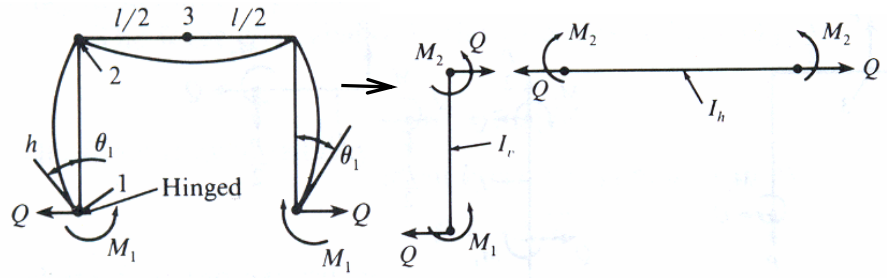


Figure 3.13: Free-body diagrams of a lead wire frame with moments M_1 applied to give rotation of θ at the support points [2]

In this case;

$$\theta = \theta_B - \theta_A = (\partial\omega/\partial x)_B - (\partial\omega/\partial x)_A = (\partial\omega/\partial x)_B - \left[-(\partial\omega/\partial x)_B\right] = 2(\partial\omega/\partial x)_B \tag{3.19}$$

$$M_1^\theta = \left[2\theta_1(3+2C)EI_v\right] / \left[h(2+C)\right] \tag{3.20}$$

$$Q^\theta = (M_1/h)(1-C) + (4EI_h\theta_1)/(hl) \tag{3.21}$$

$$M_2^\theta = (4EI_h\theta_1/l) - CM_1^\theta \tag{3.22}$$

$$\delta_3^\theta = (\theta_1 l/4)(1/2C) \tag{3.23}$$

Superposition gives the combined moments, forces and deflections associated with force P and rotation θ.

$$M_1 = M_1^P + M_1^\theta \tag{3.24}$$

$$Q = Q^P + Q^\theta \tag{3.25}$$

$$\delta = \delta_3^P + \delta_3^\theta \tag{3.26}$$

The stresses are determined by using the bending stress equation $\sigma_{bend} = Mc / I$. These stresses are then compared to the endurance strength S_f of the lead wire (or solder) material for the accumulated fatigue cycles. If $S_f \geq K\sigma$ then lead wire (or solder) will not fail from fatigue. Here K is the stress concentration factor associated with the geometric discontinuity at the lead wire/solder joint or lead wire/component body interface.

3.4 Solder Joint Stresses in Printed Circuit Boards

Solder joints are crucial for the reliability of the electronic packages. The stress in the solder joint is determined from moment caused by force P and circuit board flexure. Printed-circuit boards may have printed circuits on only one side of the board or on both sides (Figure 3.14)

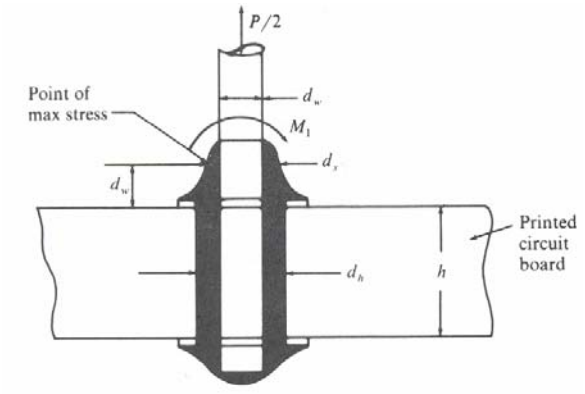


Figure 3.14: Solder joints on double sided circuit boards [2]

The solder forms a fillet above the circuit board, which has a critical location (at the knee of the solder fillet where there is a rapid change of fillet radius) about one lead wire diameter d_w above the surface of the PCB (about halfway up the height of the solder joint) where failure usually occurs [2]. The bending stress in the leadwire is given by;

$$\sigma_w = M_1 c / I_w = 32M_1 / \pi d_w^3 \tag{3.27}$$

M_1 is the net bending moment acting on the lead wire and I_w (or I_v) is the area moment of inertia for the lead wire. The strain the lead wire is given by

$$\varepsilon_w = \frac{\sigma_w}{E_w} = 32M_1 / \left(E_w \pi d_w^3 \right) \tag{3.28}$$

Where;

E_w: Modulus of elasticity of the leadwire.

The strain across the composite (solder and lead wire section) section is linearly distributed since in bending plane sections remain plane. Therefore maximum strain in the solder is calculated as;

$$\varepsilon_s = \left(d_s / d_w \right) \varepsilon_w \tag{3.29}$$

Where;

d_s: is the "*shear tearout*" diameter induced by bending of the lead wire.

The solder stress is calculated as

$$\sigma_s = E_s \varepsilon_s = \left(d_s / d_w \right) \left(E_s / E_w \right) \left(32M_1 \right) / \left(\pi d_w^3 \right) \tag{3.30}$$

Where;

E_s: Modulus of elasticity of the solder.

The failure initiation on a solder joint is usually starts at a position where $d_s = 1.5 d_w$ [2] [3].

Then solder joint stress becomes;

$$\sigma_s = E_s \varepsilon_s = \left(E_s / E_w\right)\left(48M_1\right) / \left(\pi d_w^3\right) \tag{3.31}$$

In addition to bending stress, shear stress will also occur due to the axial forces ($P/2$) developed. The average shear stress is given by

$$\tau_s = \left(P/2\right) / A_s \tag{3.32}$$

Where shear area A_s is given by

$$A_s = \pi d_h (h_{board} + 2d_w) \tag{3.33}$$

and d_h is the diameter of the plated through hole of the PCB and h_{board} is the circuit board thickness. Therefore shear stress τ_s is given by

$$\tau_s = P/[2\pi d_h (h_{board} + 2d_w)] \tag{3.34}$$

The maximum principal and shear stresss are given by

$$\sigma_{max} = \sigma_s / 2 + \left[\left(\sigma_s / 2\right)^2 + \tau_s^2\right]^{1/2} \tag{3.35}$$

$$\tau_{max} = \left[\left(\sigma_s / 2\right)^2 + \tau_s^2\right]^{1/2} \tag{3.36}$$

The maximum stress is an alternating stress due to vibratory exposure of the printed circuit board. The stress in the solder joint has to be below 1500 psi (≈ 10.34 MPa) (considering the *S-N* curve of the 37 % lead-63 % tin solder which is a typical solder arrangement in electronic assemblies) in order to prevent early vibration fatigue failures.

CHAPTER 4

EXPERIMENTAL ANALYSIS OF PCB's

Resonance transmissibility and resonance frequencies of printed circuit boards are the main required inputs for the numerical analysis performed in CirVibe. Furthermore, the young moduli of the composite PCB material are also required for numerical fatigue analysis.Glass laminates are widely used material for PCB fabrication. Bending moduli of the PCB material are very important in numerical modal analysis in order to get correct natural frequencies. Moreover, bending modulus value can be highly dependent on the manufacturer. The range for the bending modulus of FR-4 is min to max: 12 to 25 GPa [47]. Therefore exact value for the bending moduli should be obtained experimentally by the application of 3 bending test and put into the analysis.

4.1 Printed Circuit Board Transmissibility

One critical part of the analysis relates to the dynamic loads developed in the printed circuit boards at their resonant frequencies. These loads are closely associated with the transmissibility's developed by the circuit boards. In steady state vibration, transmissibility is the ratio of the measured acceleration amplitude at a point of interest in the product to the measured input acceleration amplitude of the test surface of the apparatus [48]. At structural resonance, transmissibility, Q_n , is high and it reachs its peak value. The most important data point in the transmissibility curve is the one where transmissibility is maximum since vibration damage is most likely to occur at product resonance frequencies, these resonances might be thought of as potential product fragility points.

The transmissibility of a printed-circuit board during resonance depends upon many factors such as the board material, number and type of the laminations in a multilayer board, natural frequency, type of mounting (boundary conditions), type of electronic components mounted on the circuit board, acceleration G levels, and shape of the board. Q_n must be used as "value that can be expected" since Q_n is not likely to be a fixed value that is exact for all tests - how it is fixtured for real life support is likely to have different values from test to test.

Extensive vibration test data has shown that the transmissibility Q_n for many types of PCB with various edge restraints can be approximated as being equal to the square root of the damped natural frequency. However the general range of the transmissibility normally varies from about 0.5 to about 2.0 times the square root of the damped natural frequency depending upon board size [3][49].

$$0.5\sqrt{f_n} \le Q_n \le 2\sqrt{f_n} \tag{4.1}$$

According to the data obtained by Gilbert J.Bastien [50] the resonance transmissibility of printed-circuit boards can be evaluated based on the empirical formula which is also used by CirVibe.

$$Q_n = \left(0.0053 f_n + 0.3\right)\sqrt{f_n} \qquad 50 < f_n < 400 \quad Hz \tag{4.2}$$

Obviously, test data are the best sources for information on the transmissibility characteristics for various types of circuit boards. If there are no test data available on the particular type of printed circuit board being analyzed, then the approximations outlined above can be suggested as a good starting point.Most specifications call for running transmissibility tests at a specified input drive level [51].

4.1.1 Printed Circuit Board Transmissibility Test Procedure

Before proceeding with transmissibility tests performed for the test PCB's it is necessary to determine some basic points regarding the test procedure outlined in ASTMD3580 [48]:

- According to ASTMD3580, acceleration levels sufficient to excite resonance normally range from 0.25 to 0.5g [48].
- There are two alternate test methods available in order to conduct transmissibility tests: Test Method A-Resonance Search Using Sinusoidal Vibration, and Test Method B- Resonance Search Using Random Vibration. Random vibration test can be conducted more quickly than the sine tests therefore in this study it will be used for the PCB transmissibility tests.
- For the input loading profile a flat broadband spectrum (band limited white noise input), shall be used. In addition the overall amplitude of the spectrum is recommended to be not less than 0.25grms as mentioned above. In the transmissibility tests 0.5grms white noise input with frequency range of 20-1000 Hz was used
- For the determination of resonances, any resonances with transmissibility's of 2 or greater may be considered significant.

4.1.2 PCB Transmissibility Tests

The set up used for the transmissibility tests is shown below (Figure 4.1).

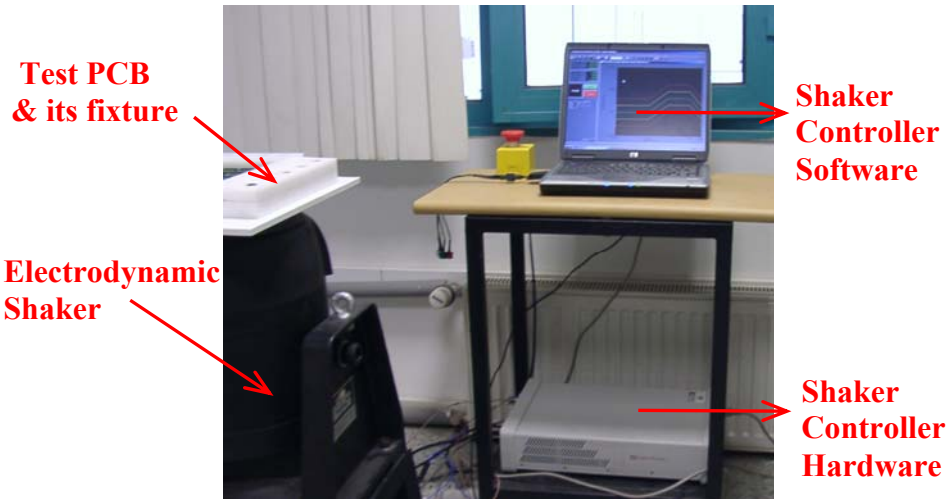


Figure 4.1: Printed Circuit Board Transmissibility Test Setup

Dataphysics Vector 1 Closed Loop Shaker Controller is used to drive the Ling Dynamics electrodynamic shaker. The closed loop control hardware consists of 1 drive channel together with two output (measurements) channels. In the tests, two accelerometers are used; one for the control accelerometer, one for the response measurements.

Control accelerometer is 3-axis ICP type accelerometer (PCB Model 35616) which is mounted on the moving head of the shaker and connected to the input of the drive channel of the shaker controller. For the response measurements, one miniature single axis (0.7 grams) ICP type accelerometer (PCB Model 352A24) is used (Figure 4.2).

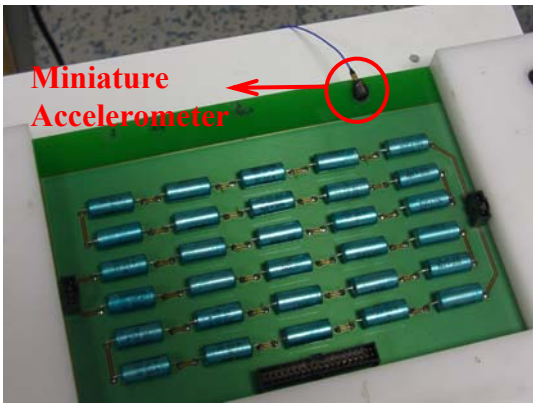


Figure 4.2: Miniature lightweight response accelerometer for response measurements

Transmissibility values are obtained for the first 7 modes of each of the printed circuit boards (PCB populated with Tantalum Capacitor, PCB populated with DIP, PCB populated with Surface Mount Ceramic capacitor and PCB populated with Aluminum capacitor).

First of all, based on the numerical modal analysis performed in CirVibe maximum deformation points of the PCB's for each mode are determined. Then the response accelerometer is roved at these points for each of the test PCB in order to determine the resonance transmissibility's for each mode. However for some of the modes, the maximum deformation points are identical hence number of roving points is actually less than 7.

Table 4.1 shows the maximum deformation points of PCB populated with Tantalum Capacitor, PCB populated with DIP, PCB populated with Aluminum capacitor and PCB populated with Surface Mount Ceramic capacitor respectively.

Table 4.1: Maximum Deformation Points of Test PCB's together with resonance transmissibility's

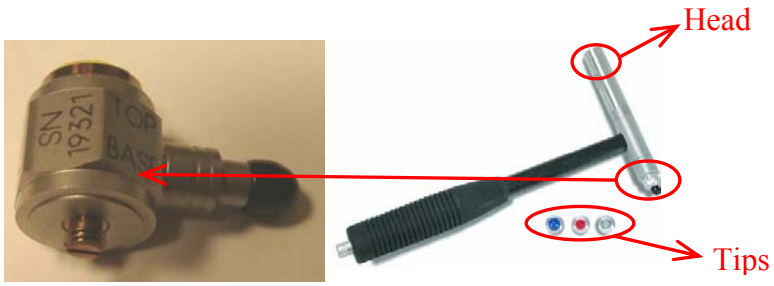
1-Axial Leaded Tantalum Capacitor Test PCB			
Mod No	X [mm]	Y [mm]	Q
1	116,89	160,02	7.66
2	116,89	160,02	20.4
3	76,84	160,02	24.75
4	73,66	160,02	2.28
5	174,12	160,02	1.59
6	116,89	160,02	4.55
7	57,35	160,02	3.87
2-Dual Inline Package (DIP) Test PCB			
Mod No	X [mm]	Y [mm]	Q
1	116,84	160,02	16.08
2	116,84	160,02	10.04
3	157,48	160,02	46.41
4	73,66	160,02	14.59
5	172,72	160,02	2.76
6	119,38	160,02	2
7	58,42	160,02	2.30
3-Axial Leaded Aluminum Capacitor Test PCB			
Mod No	X [mm]	Y [mm]	Q
1	118,11	160,02	16.38
2	118,11	160,02	9.69
3	76,2	160,02	12.92
4	160,02	160,02	30.61
5	175,26	160,02	24.11
6	118,11	160,02	3.02
7	57,89	160,02	3
4-Surface Mount Ceramic Capacitor Test PCB			
Mod No	X [mm]	Y [mm]	Q
1	115,57	160,02	7.59
2	115,57	160,02	36.19
3	76,124	160,02	22.84
4	157,33	160,02	3.39
5	171,93	160,02	1.69
6	115,57	160,02	1.83
7	58,04	160,02	4.69

From the test results it is apparent that resonance transmissibility doesn't increase permanently with increasing natural frequency. In addition, components mounted on the PCB's play an important part in defining the resonance frequency & transmissibility.

4.2 Experimental Modal Analysis of PCB's

Experimental modal analysis is used to validate finite element analysis models, Once an FEA model has been validated, it can be used for a variety of load simulations. This is called model verification [52].

In this method, the structure is excited with a force and the responses from various locations of the structure are measured. In most cases, the force value is measured by a force transducer (Figure 4.3a) and the responses are measured by accelerometers (Figure 4.3b). By determining the relationship between the forces imparted to a structure and the structure's response to those forces, the modes of a structure can be defined. The two most popular methods of imparting forces to the test structure are a shaker when the structure is big and massive so that it cannot be exited with a hammer whereas for lightweight structures like printed circuit boards, hard disks an impact hammer can be used. The impact hammer testing has become the most popular modal testing method used today [53].Different sized hammers are required to provide the appropriate impact force, depending on the size of the structure; small hammers for small structures, large hammers for large structures.



(a) (b)

Figure 4.3: a) Force transducer (load cell), b) Modal Hammer (impactor)

The boundary condition of the PCB's was selected as cantilever boundary condition (Figure 4.4).The miniature ±50 g accelerometers (PCB 352A24) were placed at points 2, 4 and 5 of the sample PCB as shown in Figure 4.4. At point 1 miniature ±500g accelerometer (Dytran 3023A) and at point 3 (PCB 356B21) where the impact force was applied (excitation point) again miniature ±500g accelerometer (PCB 356B21) was used in order to avoid saturation of the accelerometer signal due to improper force level. The boundary condition of the PCB fixture is simulated by "fixed line supports" for the purpose of FE model validation (Figure 4.5).

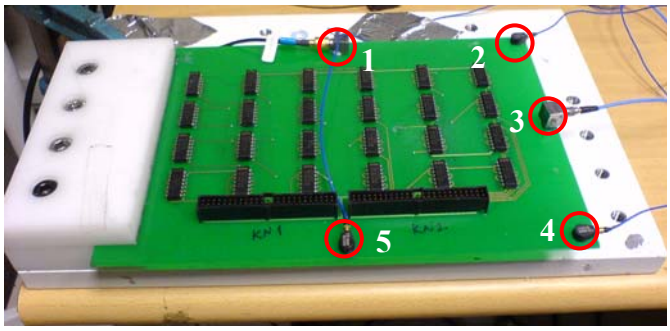


Figure 4.4: Boundary condition of the PCB and accelerometers used in modal test

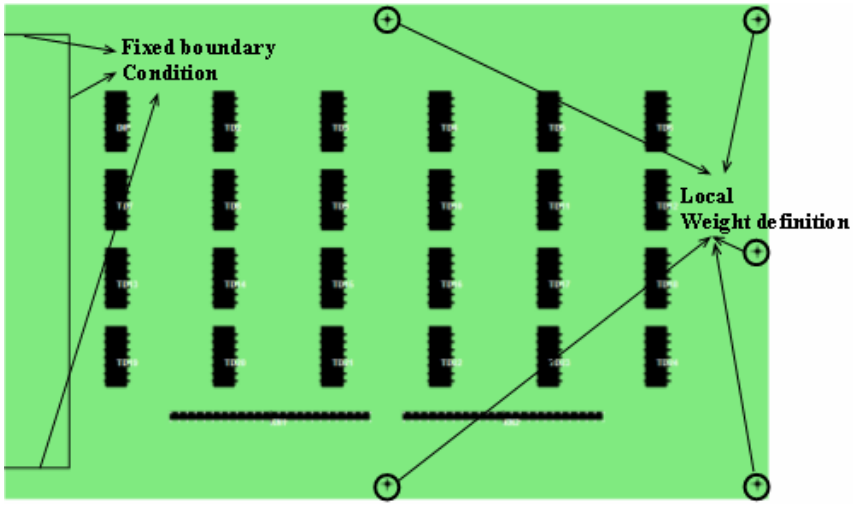
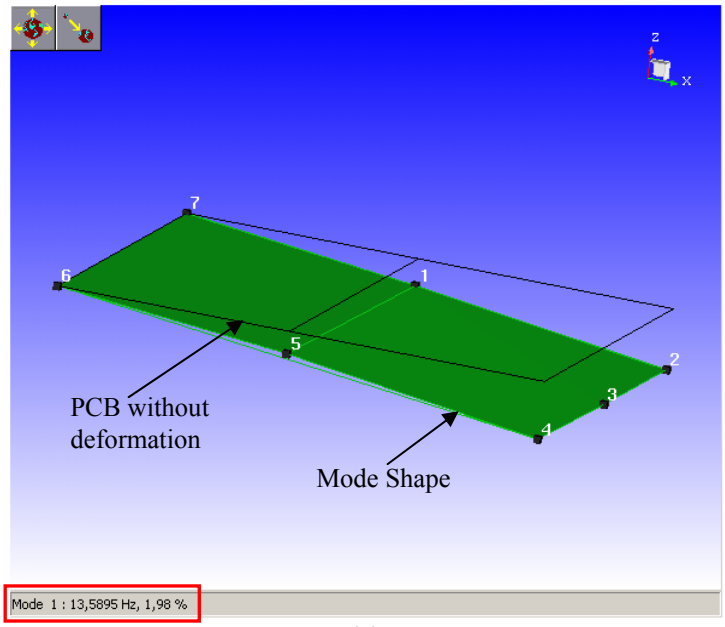


Figure 4.5: FEA Model of the PCB showing the boundary condition and local weights

After exciting the PCB with modal hammer (PCB 086C01/440 N range), the input loading and response accelerations are stored and analyzed to give the Frequency Response Functions (the ratio of the output response of a structure to an applied force). FRF calculations for all of the accelerometers are performed and curves are fitted to these functions in order to obtain the resonant frequency, damping and the mode shape of the structure. In this analysis Least Squares Complex Exponential method in LMS Test Lab was used for curve fitting [54].

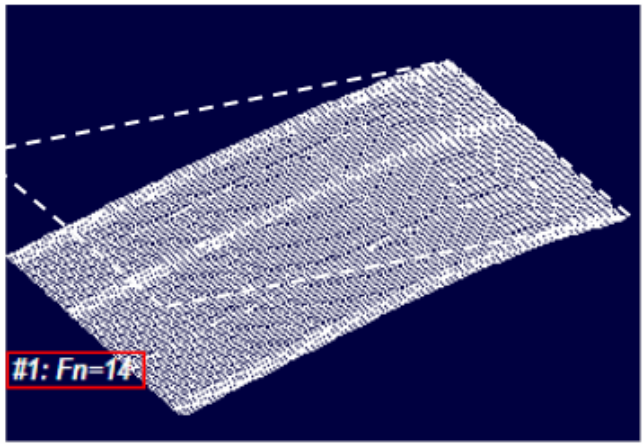
Moreover the masses of the accelerometers on the PCB were also included into the analysis by defining "local weight" in CirVibe. By evaluating the results, the following sample comparison is performed for the first three natural frequencies (only the first mode shapes are shown) of the PCB populated with Plastic Dual Inline Packages (Figure 4.6).



(a)

Figure 4.6: a) Experimental modal Analysis for the first mode (13.59 Hz) of the PCB with actual boundary conditions,

Comparisons of the FEA and test results for the test PCBs are summarized in Table 4.2 below:



(b)

Figure 4.6 (continued) b) Finite element Modal Analysis for the first mode (14 Hz) of the PCB with Clamped-Free Free -Free boundary conditions

Table 4.2: Comparison of the numerical and experimental modal analysis of the test PCB's for their first three natural frequencies

PCB with Plastic Dual Inline Package			
Mode	Frequency by FEA model (Hz)	Frequency by Test (Hz)	(FEA-test)/test (%)
1	13.59	14	-2.93
2	40.89	43	-4.9
3	87.17	91	-4.21
PCB with Axial Leaded Tantalum Capacitor			
Mode	Frequency by FEA model (Hz)	Frequency by Test (Hz)	(FEA-test)/test (%)
1	15.18	12	26.49
2	38.54	43	-10.38
3	87.09	72	20.96
PCB with Axial Leaded Aluminum Capacitors			
Mode	Frequency by FEA model (Hz)	Frequency by Test (Hz)	(FEA-test)/test (%)
1	11.15	11	1.35
2	32.17	39	-17.51
3	58.7	68	-13.68

Table 4.2 (continued): Comparison of the numerical and experimental modal analysis of the test PCB's for their first three natural frequencies

PCB with Ceramic Surface Mount Capacitors			
Mode	Frequency by FEA model (Hz)	Frequency by Test (Hz)	(FEA-test)/test (%)
1	13.9	14	-0.75
2	53.4	47	13.62
3	87.34	93	-6.09

It can be seen from the results that the natural frequency values and mode shapes are consistent.The natural frequency of the printed circuit boards is strongly dependent on the young modulus of the composite PCB material. The young modulus is dependent on the ply structure (fiber directions) of the composite. In the numerical analysis of the test PCBs the mean values of the young modules for lengthwise (x) and crosswise (y) directions obtained from three-point bending tests were used. In order to achieve better accuracy the number of test specimens in three point bending test could be increased .Here the accuracy level is found to be sufficient therefore the dynamic behavior of the structure can be simulated using the finite element model.

4.3 PCB 3 Point Bending Test

The bending test method measures the behavior of materials subjected to simple beam loading. A flexure test produces tensile stress in the convex side of the specimen and compression stress in the concave side. In this test, a composite beam specimen of rectangular cross-section is loaded in either a three-point bending mode or a four-point bending mode. In a 3- point test (Figure 4.7) a concentrated load is applied at the span centre. This method is used most often on account of it simplicity and has received wide acceptance in the composite material industry.

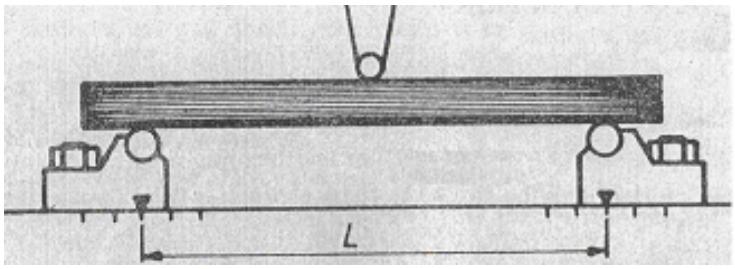


Figure 4.7: 3- point bending test [1].

Flexural properties, such as flexural strength and modulus, are determined by ASTM test method D790 [55]. This test method covers the determination of flexural properties of unreinforced and reinforced plastics, including high-modulus composites in the form of rectangular bars molded directly or cut from sheets, plates [56] .In this study bending stiffness (modulus) will be determined by using 3-point bending test procedure A.

4.3.1 Summary of the Test Method

- A bar of rectangular cross-section rests on two supports and is loaded by means of a loading nose midway between the supports (Figure 4.7). Unless otherwise stated by an applicable standard or code, large span-thickness ($L_{specimen}/t_{specimen}$) ratio is recommended [55].For most materials support span-to-depth ratio of 16:1 is acceptable.
- The strain rate of 0.01mm/mm/min is used for this test method. Bending tests are conducted for each of 5 specimens in "lengthwise" and "crosswise" directions. A span-to-depth ratio of 60 is used in the tests. Span length, $L_{specimen}$, is selected to be 96mm.Printed Circuit Board thickness (depth of beam tested), $t_{specimen}$, is 1.6mm.In addition, width of the beam tested, $b_{specimen}$, is selected as 20mm. Rate of crosshead motion is calculated as 10mm/min.

4.3.2 FR-4 Bending Tests

Flexural modulus of highly anisotropic laminates is a strong function of ply-stacking sequence and it may vary with specimen depth and rate of straining. Bending tests are performed by using INSTRON 1175 test machine (Figure 4.8)

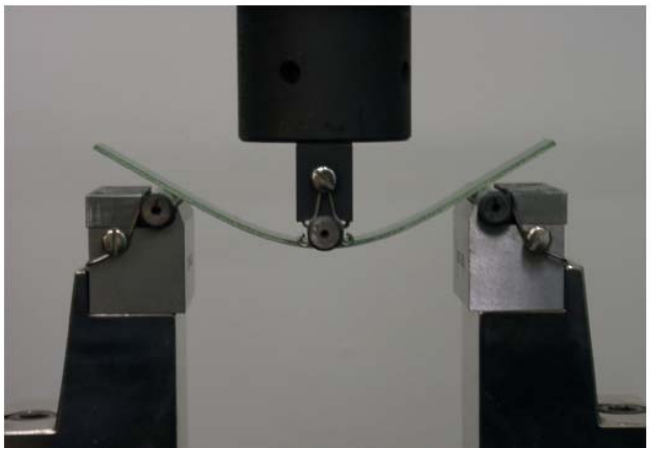


Figure 4.8: 3 point bending test set up (Printed Circuit Board Specimen, Loading Nose and Supports)

After the application of the load to the specimen at the specified crosshead rate load-deflection data's are collected intermittently.

The tangent modulus of elasticity, often called the "modulus of elasticity" which is the ratio within the elastic limit is calculated by drawing tangent to the steepest initial straight-line portion of the load- deflection curve. In Figure 4.9 below, load-deflection diagram and in Table 4.3 the results obtained from the 3 point bending tests of specimens tested in lengthwise direction are shown.

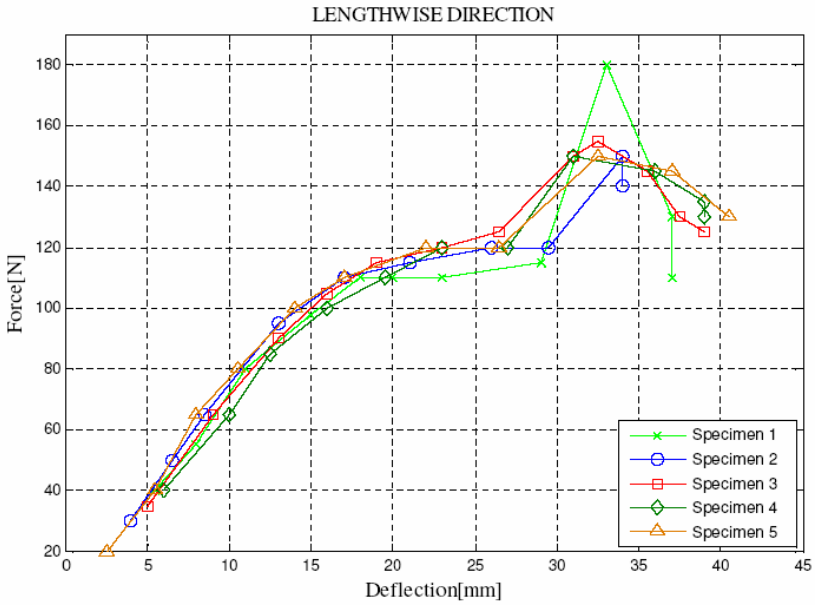


Figure 4.9: Load deflection diagrams for test specimens (lengthwise direction) in three –point flexural tests.

Table 4.3: Bending Modulus, Lengthwise Direction

FR-4 (Epoxy Glass)	Modulus, GPa
Specimen 1	16.071
Specimen 2	17.560
Specimen 3	18.043
Specimen 4	17.670
Specimen 5	18.830
Mean	**17.634**
Standard Deviation	1.763

Similarly, in Figure 4.10 below, load-deflection diagram obtained from the 3 point bending tests of specimens tested in crosswise direction is shown. In Table 4.4 the bending modulus values of the each specimen in crosswise direction are shown.

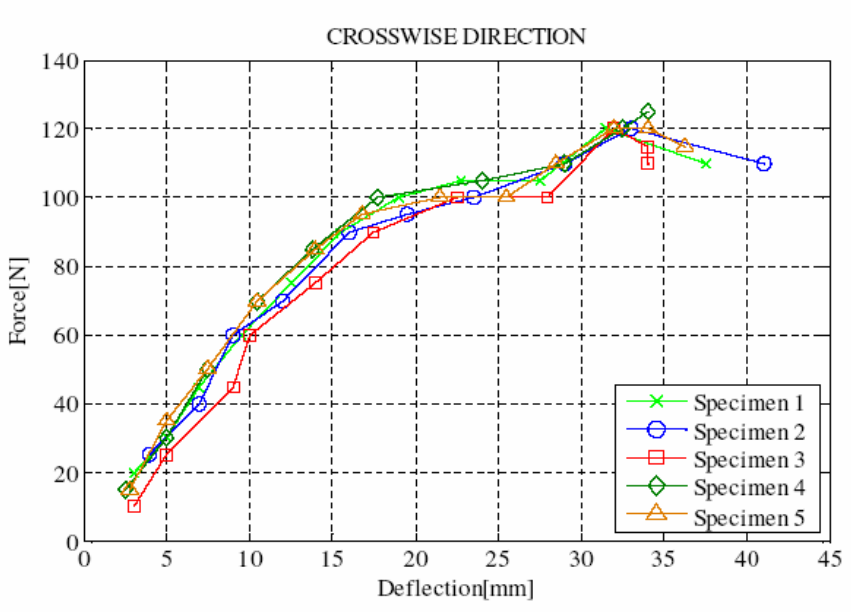


Figure 4.10: Load deflection diagrams for test specimens (crosswise direction) in three –point flexural tests

Table 4.4: Bending Modulus, Crosswise Direction

FR-4 (Epoxy Glass)	Modulus, GPa
Specimen 1	16.073
Specimen 2	15.397
Specimen 3	16.153
Specimen 4	17.489
Specimen 5	16.156
Mean	**16.254**
Standard Deviation	0.760

CHAPTER 5

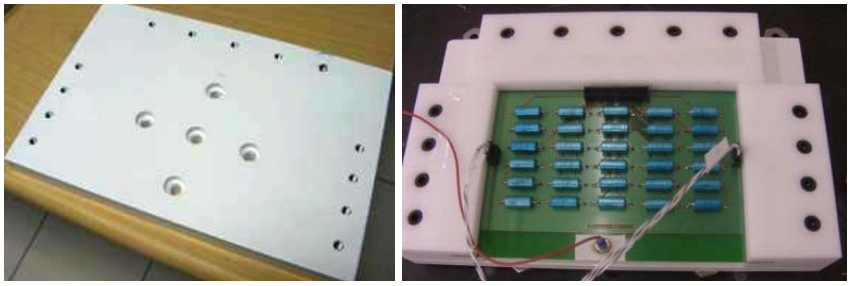
FATIGUE TESTING & ANALYSIS OF PCB

The rapid advancement of electronic technologies has placed increasing demands on electronic packaging and its material structures in terms of the reliability requirements.Quality of electronics could be measured by its ability to meet its expected product life.Vibration testing is an important part of producing quality electronics through accelerated life testing.In addition to the thermally induced stresses, electronic packages often experience dynamic external loads during shipping, handling, and/or operation. This is especially important for automotive, military, and commercial avionics operating environments. These dynamic loads give rise to large dynamic stresses in the leads causing fatigue failures.Component failure can occur in solder joint, lead wire, body and internals.Dimensions, material properties, stress concentrations and expected variations affect life capability of components. Furthermore, component capability variations are expected across component types and within component types. Therefore in this thesis work electronic components which are critical in terms of vibration induced fatigue will be investigated. The aim is to numerically describe the vibration in terms meaningful to failure: Vibration Damage. The tested components have been chosen based on the discussions with electronic engineers in ASELSAN. The solution is achieved by using integrated Finite Element Analysis (FEA) and Design of Experiments (DOE).

5.1 PCB Test Setup

Before proceeding with the fatigue analysis of the PCBs tooling must be developed to interface the PCB to stress testing equipment. Fixturing is used to

provide mechanical coupling of the test item to the vibration table. For this purpose PCB fixture was designed and manufactured (Figure 5.1).



(a) Aluminum part (lower) (b) Polyoxymethylene parts (upper)

Figure 5.1: PCB fixture used in the SST

Accelerated life testing of the PCBs has been conducted by using electrodynamic vibration shaker to generate multiple random frequency vibration (Figure 5.2**)**.

Figure 5.2: Vibration test equipment [57]

5.2 Purpose of Accelerated Life Testing

Traditional life data analysis involves analyzing times-to-failure data (of a product, system or component) obtained under normal operating conditions in order to quantify the life characteristics of the product, system or component.

In many situations, and for many reasons, such life data (or times-to-failure data) is very difficult to obtain. The reasons for this difficulty can include the long life times of today's products, the small time period between design and release. Given this difficulty, in order to better understand their failure mechanisms and their life characteristics, reliability practitioners have attempted to devise methods to force these products to fail more quickly than they would under normal use conditions. In other words, they have attempted to accelerate their failures. Over the years, the term accelerated life testing has been used to describe all such practices.

There are different types of accelerated tests. Traditional accelerated life test methods have involved the application of single stresses (for example only vibration or only temperature cycle). However, it is increasingly felt many potential failure mechanisms result from, or are accelerated by, combinations of environmental conditions (e.g. random vibration + high temperature). However in this study, only vibration induced failures are of interest therefore step stress tests of PCBs were conducted using only random vibration stress. Accelerated life testing of electronic systems uses rules of equivalent damage to define vibration spectra for use in compressed time capable of representing a full life of service use [43].

5.3 Step Stress Testing

Traditionally, accelerated tests using a time-varying stress application have been used to assure failures quickly. The most basic type of time-varying stress test is a step-stress test. A great advantage of the SST procedure is that it is possible to quickly gain information on the stress level where product failure is significant. Another advantage is that reasonable time period can be established to complete the tests.The step stress approach determines the design limit (fragility limits) of the products [58].What step-stress test (SST) properly means is exposing a sample to a series of successively higher “steps” of stress, with measurement of the cumulative failures after each step (Figure 5.3) [59].

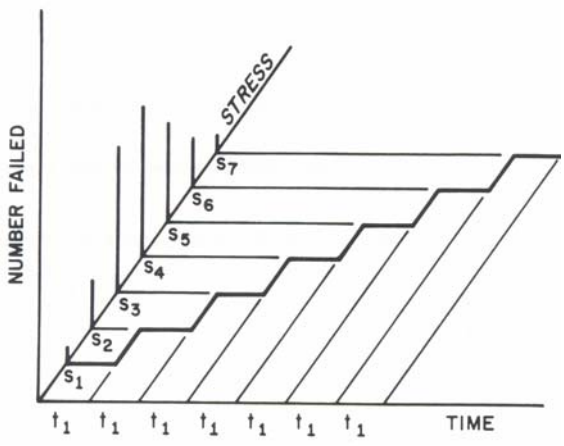


Figure 5.3: Step Stress Testing Procedure [59]

The step stress test can shorten test time, because a unit is placed on test at an initial low stress, and if it does not fail in a predetermined time the stress is increased [60]. The test is terminated when all units have failed or when a certain number of failures are observed or until a certain time (till the test hardware doesn't allow to continue tests) has elapsed.

According to IEST it is recommended that a broad band spectrum with adequate energy in 20-2000 Hz can be chosen, and a broadband vibration input level of 2 or 3g (rms) can be used for the starting level of the testing. The overall vibration input level is then increased in predetermined steps (typically 3 g (rms) steps) holding at each level for some prescribed length of time which is usually selected as 10 minutes [58]. However, overall vibration g (rms) input level is best defined by experience through analysis of similar systems. Furthermore steps in the SST test are best set at a constant factor (best tied to slope*)* on the previous level, so that the life factor is also constant. Therefore in the SST of the test PCBs, at each test step, the input has been incremented by the fatigue curve slope of 1.25 (factor on stress for an order of magnitude reduction in allowable cycles) which is an expected value for lead wire and solder materials used in electronic systems [3][61]. Finally, duration of the test steps should be set to assure failure defined by high cycle fatigue so that 1 hour step duration has been selected [62].

5.4 Fatigue Testing & Analysis of PCB Populated with Axial Leaded Tantalum Capacitor

In Figure 5.4 below, test PCB which is populated with Tantalum type capacitors (Sprague 100 μF capacitors) is shown. In addition there are two 1x4 pin type and one 2x19 type connectors used for the purpose of automatic damage detection infrastructure (APPENDIX-A).

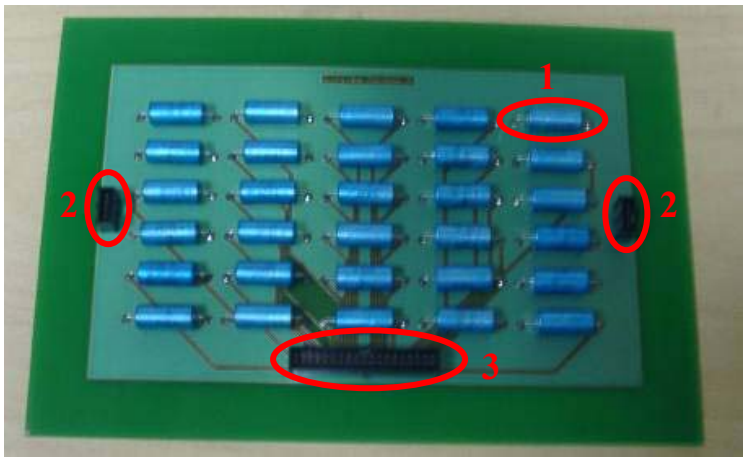


Figure 5.4: Test PCB populated with axial leaded Tantalum capacitors 1: Tantalum Capacitor (vendor: Sprague), 2: Molex Connector (1x4 pin type), 3: Molex Connector (2x19 pin type)

Step Stress Accelerated Life Tests (SST) of the 3 PCBs were performed. The starting level (1.step) of the loading was 20-2000 Hz 2grms (2.02×10^{-3} g^2/Hz) random vibration. Test duration for each step was chosen to be 1 hour in order to provide high cycle fatigue occurrence. In the SST of the test PCBs, at each test step, the input has been incremented by the fatigue curve slope of 1.25 (factor on stress that results in a 10 times reduction in the number of cycles to failure) which is an expected value for lead wire and solder materials used in electronic systems [3][61]. SST was conducted up to the 5.step for the 1.PCB and up to 6.step for the 2. & 3.PCB's.

During this test period 9 failures (the 9 failures define numerical values useful in understanding distributions as well as differences in component types**)** were detected for the 1. and 3.PCB and 11 failures were detected for the 2.PCB.The number of failures were adequate so that tests were not carried on after 6.step. Some failures were observed at the solder joints and some were observed at the junctions where component body is attached to the lead wire.In vibration testing of the PCB in order to detect the damage automatically, an electrical test set-up was formed (Figure 5.5). Table 5.1 shows laboratory test results (vibration life testing) of the SST for the PCB's populated with Tantalum capacitors.

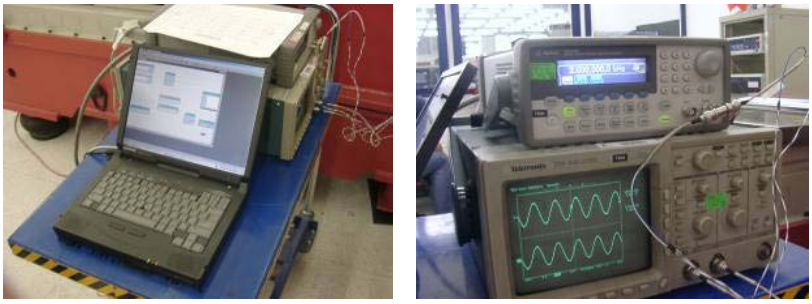


Figure 5.5: Automatic damage detection system components (HP 33120A arbitrary wave form generator (signal generator), test software (Agilent Vee 6.2) and 2 channel digitizing oscilloscope)

Table 5.1: Capacitor Failure Times in SST (Accelerated Lives)

	Failure Time [min]				
Failure Sequence	PCB 1	PCB 2	PCB 3	Standard Deviation	Arithmetic Mean
1.failure	152	155	204	22.44	170.33
2.failure	175	187	216	15.56	192.67
3.failure	178	224	238	23.56	213.33
4.failure	184	245	249	28	226
5.failure	243	305	257	24.44	268.33
6.failure	257	314	319	26.44	296.66
7.failure	260	316	331	28.22	302.33
8.failure	270	330	331	26.89	310.33
9.failure	277	339	359	32	325
10.failure	X	344	X	X	344
11.failure	X	346	X	X	346

Table 5.1 brings out the similar fatigue behavior of the capacitors on the PCB 2 and PCB 3 according to the failure times. In addition, fatigue lives of the capacitors on the PCB 1 are always less than the ones for PCB 2 and PCB 3.

In the calculation of the fatigue lives of the capacitors, a relative damage number, *d*, which is based on the test data, will be computed for each of the failed capacitors. It is named as "relative damage index "since incremental damage accumulated for the 1.step of the SST is taken as 1 unit. This damage number represents the total accumulated damage up to the instant of failure of the capacitor and it uses the failure time (accelerated life) obtained from the SST. Since $Damage \propto \frac{1}{N}$ (*N* being the fatigue life of the component), at each step, fatigue cycles will be 10 times as damaging as the previous step. Therefore if the incremental damage for the 1.step is taken as 1 unit, then step 2 will be 10 times as damaging as step 1 and step 3 will be 100 times as damaging as step 1 and soon.When failure occurs during the step, using Miner's linear fatigue damage theory, relative incremental damage number for this test step can be evaluated by using equation 5.1 as follows :

$$d^* = \left(\frac{t^*}{\Delta t}\right) d_{step} \qquad d^* \le d_{step} \tag{5.1}$$

Where;

t^* : Time passed from the beginning of the step to the instant of failure

Δt : Constant step duration which is taken as 1 hour in the SST in order to achieve high cycle fatigue cycles.

d^* : Accumulated damage for the test step in which failure is detected.

d_{step} : Incremental damage accumulated for the fail-free (or when the failure occurs at the end of the step) test step

Finally relative damage numbers (*d*) of the capacitors can be evaluated by summing up the relative incremental damage numbers (d^*) of each step.

Table 5.2 below demonstrates the relative damage numbers for the 1. failed capacitors mounted on the 1. test PCB.The relative damage number for the 1.failed capacitor on the 2.PCB (damage at 35.min of the 3.step) and on the 3.PCB (damage at 24.min of the 4.step) were evaluated as 69.33 and 511 respectively.

Finally actual accumulated damage numbers for the failed capacitors can be evaluated by modifying the damage accumulated at the 1.step of the SST by the relative damage numbers

$$d_{tot} = d * d_{step1} \tag{5.2}$$

Where;

d_{tot} : Total (final) accumulated damage number for the failed component

d_{step1} : Accumulated damage at the end of the 1.step of the SST

Table 5.2: Relative damage number *d* for the 1.failed capacitor on the 1.PCB

PCB-1						
slope	1.25					
			damage			
	step ratio	accumulated	factor			
excitation	i / (i-1)	life total (d)	i / (i-1)			
1		1		Damage index at the end of 1.step		
1.25	1.25	11	10	Damage index at the end of 2.step		
1.5625	1.25	64.333	10	**Damage at 32.min of the 3.step**		
1.5625	1.25	111	10	Damage index at the end of 3.step		

Material properties of the capacitors and connectors are obtained from the material database of Matweb [63]. Figure 5.6 shows material and geometrical properties list of the axial leaded Tantalum capacitor ($100\,\mu F$) analyzed. Capacitor body (Tantalum) elastic modulus and component body density are 186 GPa and 5.0073 gr/cm^3 respectively. The lead wire of the capacitor is Nickel with elastic modulus of 207 GPa.Material and geometrical properties list of the 1x4 pin type connector is listed in Figure 5.7.

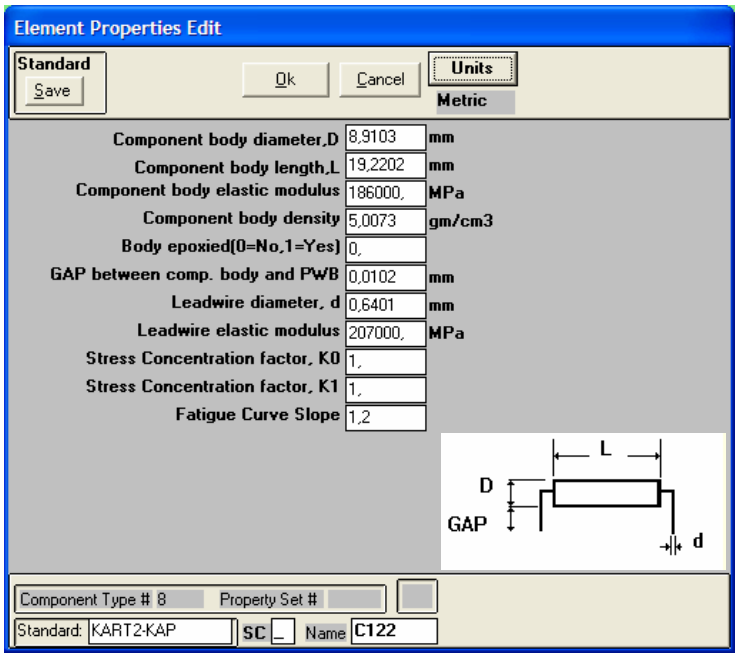


Figure 5.6: Axial leaded Solid Tantalum Capacitor material and geometrical properties (vendor: Sprague)

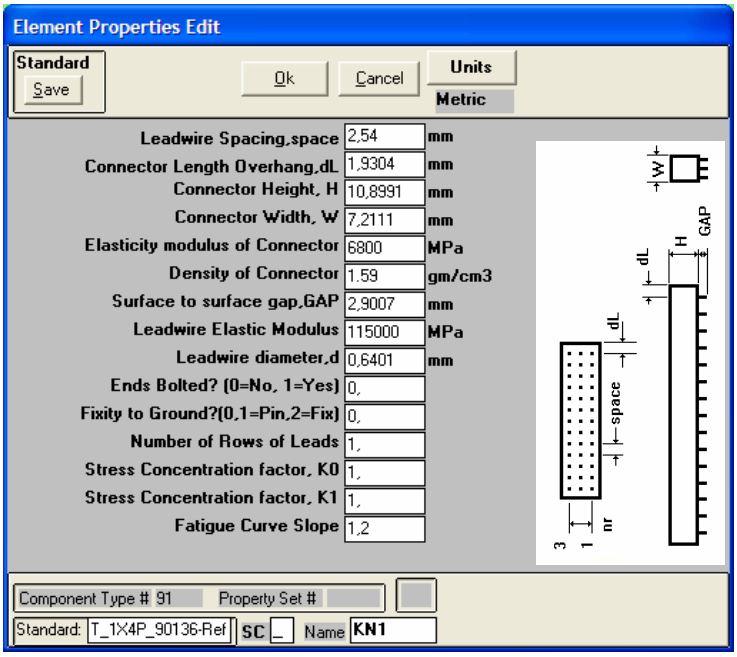


Figure 5.7: Connector (1x4 pin type) material and geometrical properties (vendor: Molex)

The overhang length and width for the 2x19 pin type connector are different than the ones for the 1X4 pin type connector.These values are 1.42 and 9.75 respectively.

Connector body (Glass-Filled Polyester (Polybutylene Terephthalete (PBT))) elastic modulus and component body density are 6.8GPa (average) and 1.59gr/cm^3 (average) respectively.

The lead wires of the connectors are made from a Copper alloy called Phosphor Bronze with elastic modulus of 115 GPa. In Figure 5.8. PWA total weight, PWB thickness, PWB elastic bending modulus in X and Y directions are entered. Bending modules in X & Y direction are obtained from three-point bending test of the PWB material.

Definition of the boundary condition is important because it affects the natural frequency consequently fatigue damage of the PCB. Figure 5.9 represents the edge and corner support definitions of the PCB.

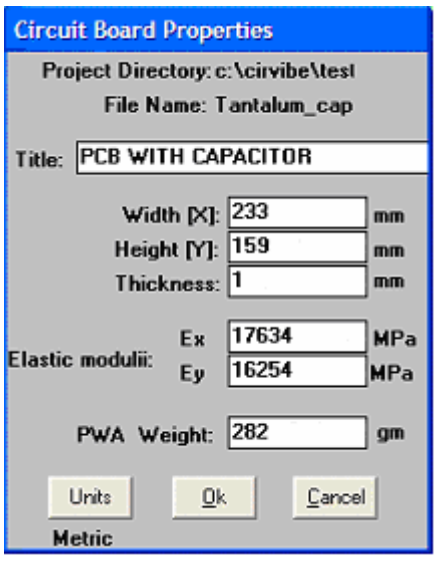


Figure 5.8: Circuit Board Properties Edit Window

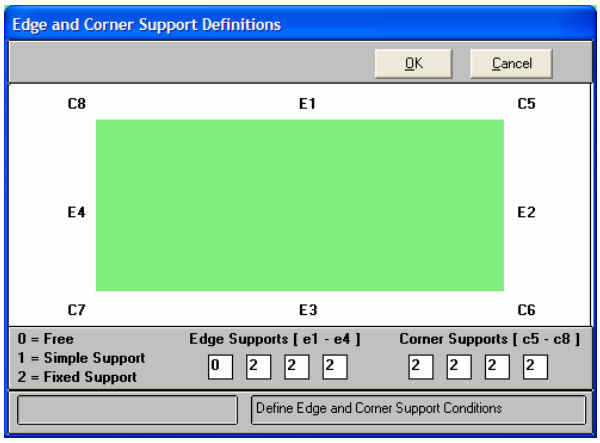
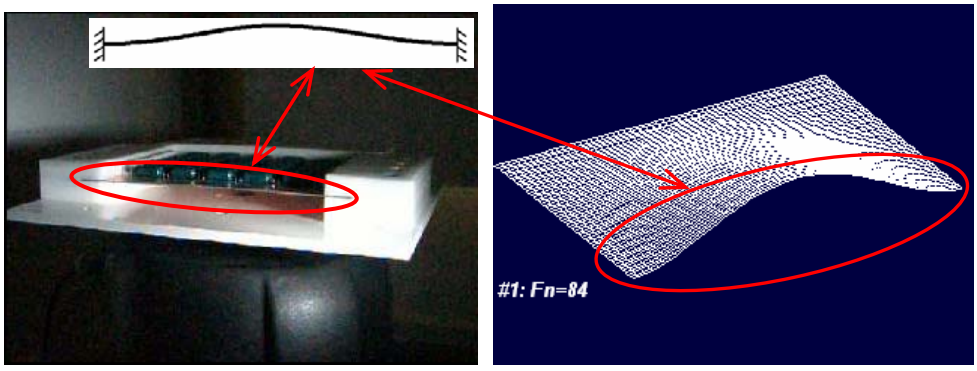


Figure 5.9: Edge and corner support definitions window

In order to give greater confidence in the boundary condition definition stroboscope verification of the lowest mode shape was done. Verification of the higher frequency mode shapes was not done since the displacement amplitude would be so small that distinct mode shapes could not be distinguished.

Figure 5.10 represents the image from the mode shape verification test done by using stroboscope and the 1.mode shape of the PCB obtained by numerical modal analysis. The board was deformed similar to the Figure 5.10b.



(a) (b)

Figure 5.10: a) 1.Mode shape verification of the PCB using a stroboscope (fundamental natural frequency defined by vibration test=91.6 Hz, vibration frequency = 90.6Hz) b) 1.mode shape of the PCB obtained by numerical modal analysis (fundamental natural frequency =84 Hz)

A stroboscope is a light source such that when the flashing frequency of the stroboscope is tuned to be the same as the vibration frequency (1.natural frequency), the vibrating surface of the PCB becomes in the same position each time it is illuminated. Therefore, the vibrating surface appears motionless due to persistence of vision.

Vibration loading is defined as the Power Spectral Density (PSD).The first step of the SST was previously defined as 20-2000 Hz 2grms white noise broadband random vibration as shown in Figure 5.11.

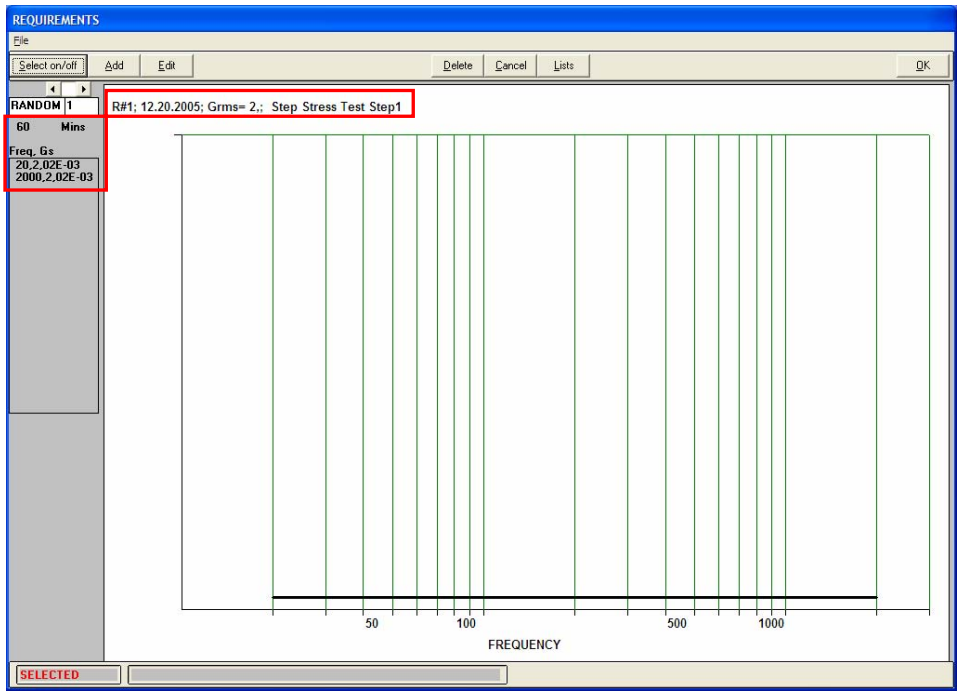


Figure 5.11: Vibration requirement definition (SST 1.step)

Virtual accelerometers are defined (Figure 5.12) at the peak response locations (Table 4.1) in CirVibe in order to input the measured peak transmissibility's at these peak accelerometer locations. Resonance transmissibility's which are obtained from transmissibility tests are defined at these accelerometer positions (Table 5.3).

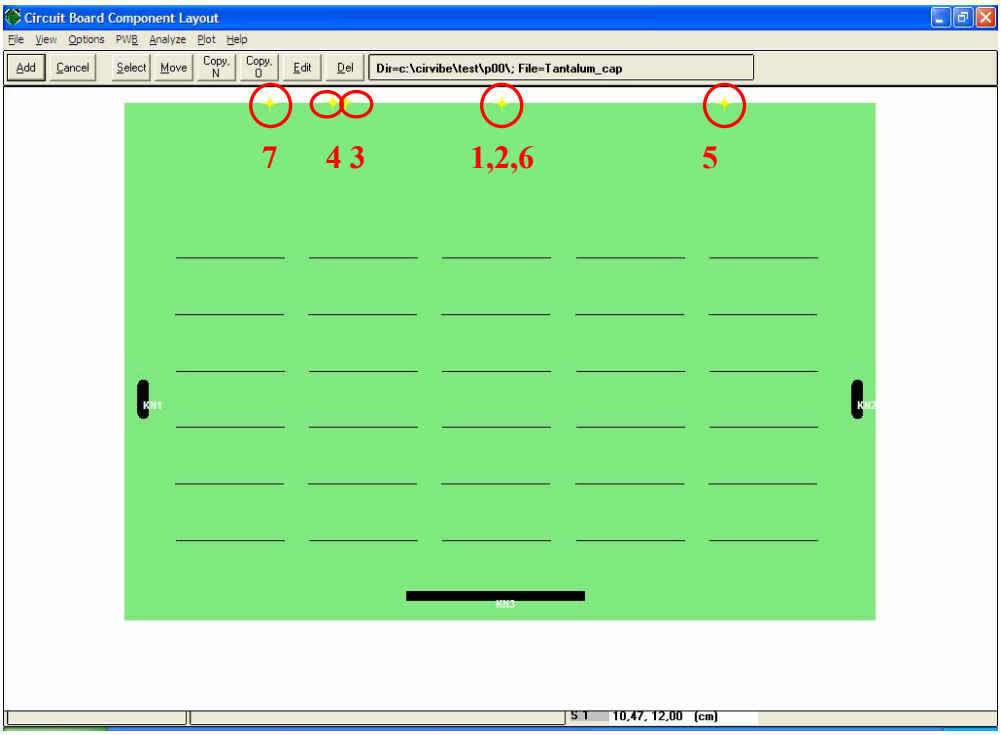


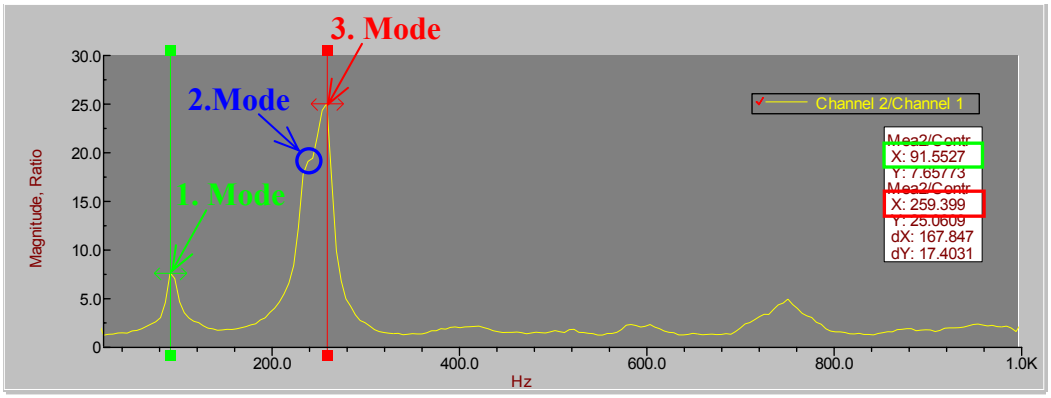
Figure 5.12: Accelerometers at the peak response locations in order to use the test data in the analysis

Table 5.3: Comparison of resonance frequencies and transmissibility's obtained by transmissibility tests & CirVibe numerical analysis for the PCB populated with Tantalum capacitors.

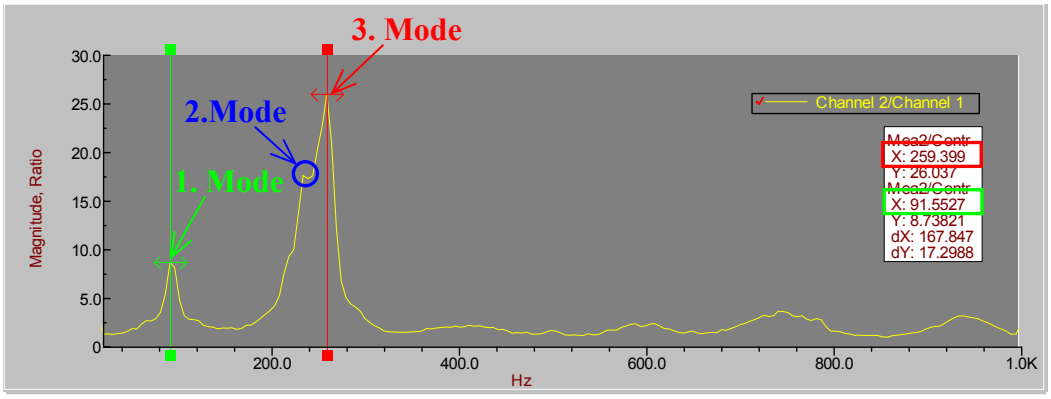
MODE #	NATURAL FREQUENCY [Hz]		
	TEST	SIMULATION	% DEVIATION
1.	91,55	83,73	8.55
2.	244,1	180,59	26.02
3.	259,4	211,47	18.48
4.	417,1	308,96	25.93
5.	493,4	403,16	18.29
6.	584,9	404,21	30.89
7.	768	497,2	35.26
MODE #	TRANSMISSIBILITY		
	TEST	SIMULATION	% DEVIATION
1.	7,66	6,81	11.07
2.	20.4	16,89	17.21
3.	24,75	20,66	16.53
4.	2,28	34,06	93.32
5.	1,59	48,93	96.75
6.	4,55	49,1	90.73
7.	3,87	65,45	94.09

If Table 5.3 is investigated, it can be seen that there is a large diversity between test and simulation results for the 4.,5.,6. and 7.modes. Accuracy can be expected to decrease with higher modes since these modes are higher modes and higher modes are harder to excite with single axis shaker.

Namely, if there is a good agreement on other natural modes, but not on one it is likely that it is a mode that is hard to excite. Natural modes and corresponding transmissibility's are obtained by observing the transmissibility plots which were attained experimentally from the accelerometer locations shown in Figure 5.12.In Figure 5.13 first three modes of the PCB were shown for the test points 1, 2, 3 and 5 respectively.

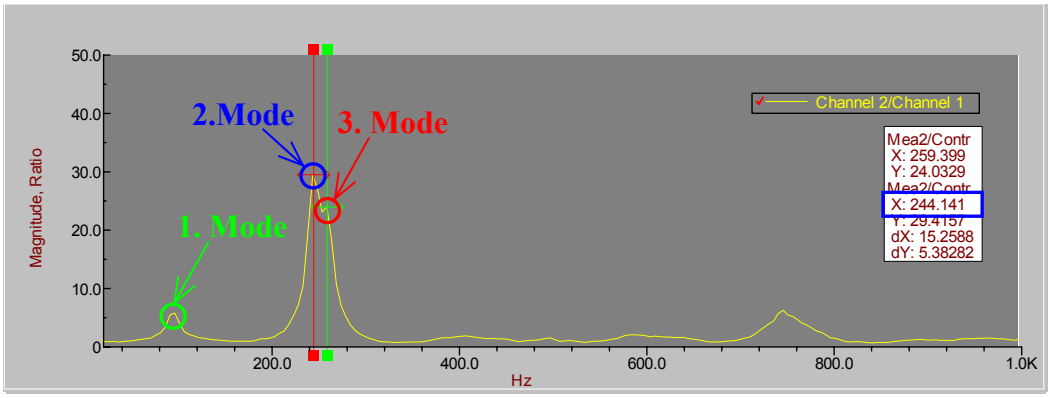


(a)



(b)

Figure 5.13: Transmissibility (Q) tests (random vibration 0.5grms white noise input freq range: 20-1000 Hz) a) - Q versus frequency plot for point 1 & 2 b) - Q versus frequency plot for point 3



(c)

Figire 5.13 (cont'd): Transmissibility (Q) tests (random vibration 0.5grms white noise input freq range: 20-1000 Hz) c) - Q versus frequency plot for point 5

The capacitors on the PCB are named as shown in Figure 5.14.

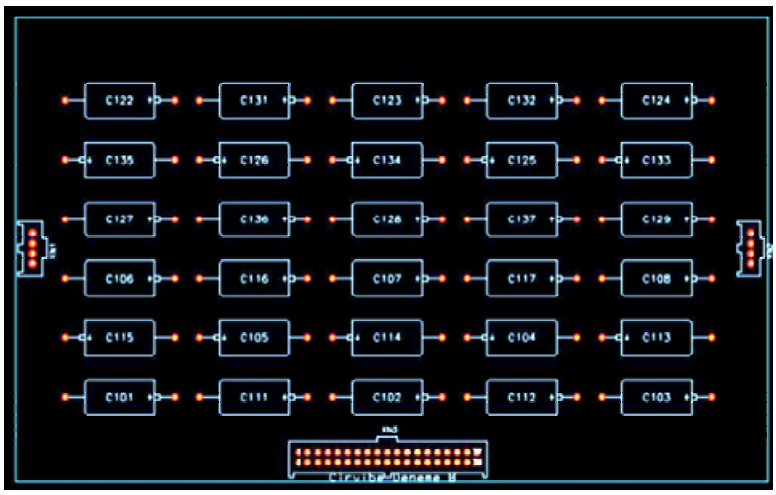


Figure 5.14: Designation of Tantalum capacitors on the test PCB (Mentor V8.9)

Energy losses are greatest when deflections are greatest and smallest when deflections are smallest. Since higher frequencies have smaller deflections (due to high stiffness at higher modes), damping will be less.

This means that higher natural frequencies will have higher transmissibility's. This is compatible with the transmissibility's obtained by simulation. However vibration tests confirm this phenomenon up to 3.mode of the PCB.

In APPENDIX-E the relative damage numbers and total accumulated damage numbers for the failed capacitors on the 1.PCB, 2.PCB and 3.PCB are listed respectively**.**

Figure 5.15, Figure 5.16 and Figure 5.17 demonstrate the locations and sequence of the failed capacitors obtained at the end of the Step Stress Tests. First of all, when the test PCB's are examined it is seen that positions of the capacitors which fail in the very first place are different for each PCB's. This is due to the fact that the scatter range in failures which affects life capability of components is very large for electronic components because of the material property variations (fatigue curve scatter), solder quality (solder process control is critical), variations in local stress concentrations and dimensions (geometric tolerances) which can not be accurately embedded into the fatigue analysis.

Furthermore there are also some other factors like response amplification (transmissibility) variations, loading variations although reference loading profile is same for all the test PCB's (variation in tests due to test equipment (shaker)). In addition, any component with 2 leads like capacitors, resistors, diodes might be dominated by their own modes (local modes of the components). Therefore natural frequency of such components should be isolated from the circuit board load spectrum. Moreover it might not be possible to predict accurately which capacitor is most likely to fail for the circuit board since "slight assembly differences" can result in a different order of failure. That is, the alignment of the component with the Z-axis can affect the life of the component. A capacitor initially tilted to the side can be expected to have a higher average response than one perfectly centered (for the same excitation). Variations in assembly procedures for circuit cards can result in differences in response (Q_n - transmissibility, f_n - natural Frequency) from one test to another.

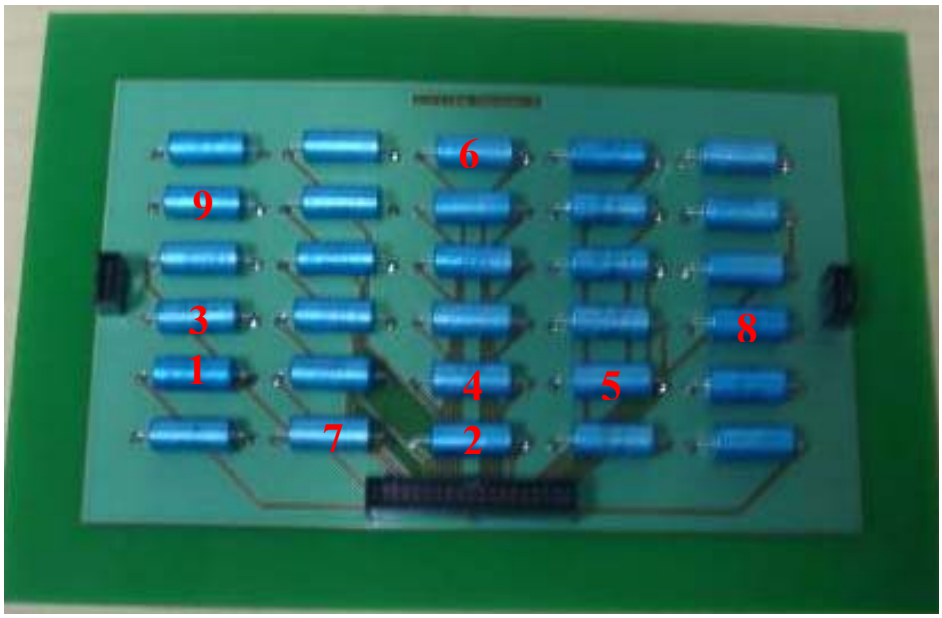


Figure 5.15: Area damage plot for the PCB 1 obtained from SST

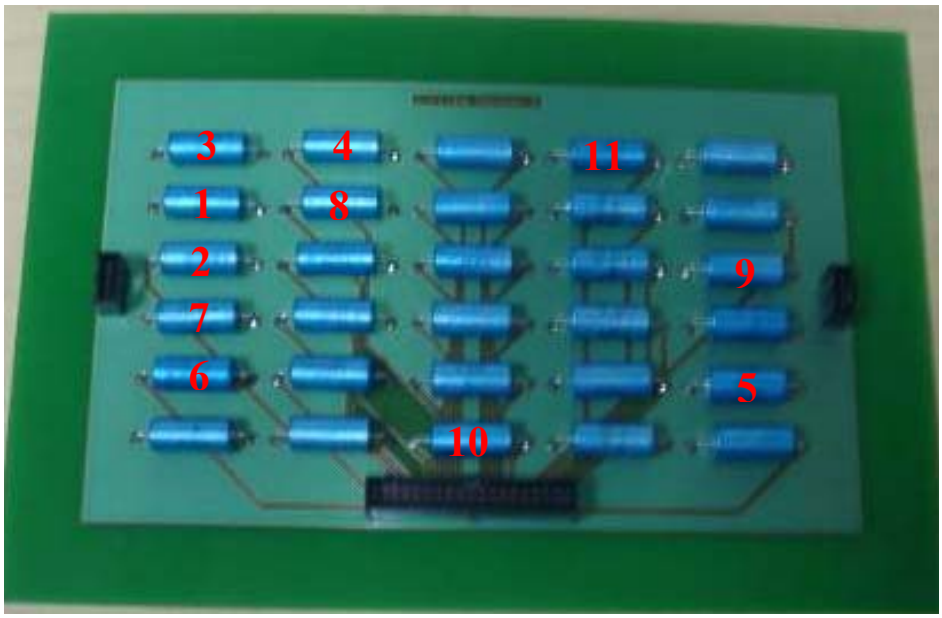


Figure 5.16: Area damage plot for the PCB 2 obtained from SST

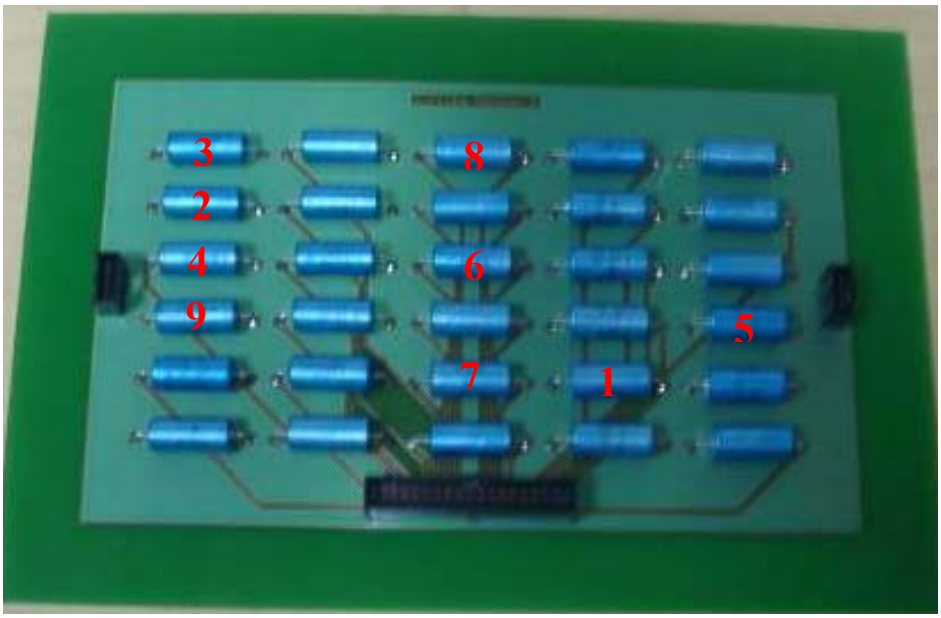


Figure 5.17: Area damage plot for the PCB 3 obtained from SST

The test results and simulation results are compared in Table 5.4 as follows:

Table 5.4: Comparison of the failure rank for test and simulation results

Failure Rank for the Damaged Capacitors					
PCB1		**PCB 2**		**PCB 3**	
Test	**Analysis**	**Test**	**Analysis**	**Test**	**Analysis**
1.	**3.**	**1.**	**1.**	**1.**	**1.**
2.	**1.**	2.	10.	2.	3.
3.	5.	3.	4.	3.	2.
4.	4.	4.	7.	4.	4.
5.	6.	5.	5.	5.	5.
6.	5.	6.	6.	6.	8.
7.	2.	7.	8.	7.	7.
8.	9.	8.	9.	8.	9.
9.	8.	9.	10.	9.	6.
		10.	2.		
		11.	11.		

Namely, test results are complicated by data scatter .There must be significant test sample for each test configuration [43].The level of testing should be performed considering cost versus value of knowledge. From Table 5.4 the most important deduction is that simulation results could be able to determine the capacitors which failed first in the tests.

The reliability of a product or component constitutes an important aspect of product quality. Of particular interest quantification of a product's reliability, so that people can derive estimates of the product's expected useful life.

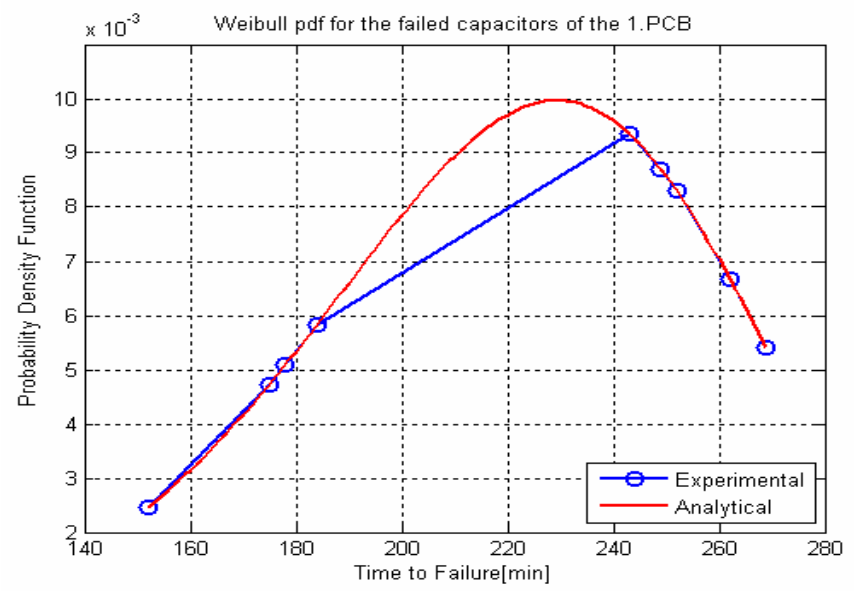
5.5 The Weibull Model in Life Testing of Tantalum Capacitors

The Weibull distribution is widely used in reliability and life data analysis. This distribution is appropriate for modeling a wide variety of different data sets (electronic components, relays, ball bearings etc.) particularly as a model for product life [64][65].For much life data, the Weibull distribution is more suitable than the exponential and normal distributions [64].When the failure probability varies over time, then the Weibull distribution is appropriate[66]. The Weibull probability density function (pdf) is

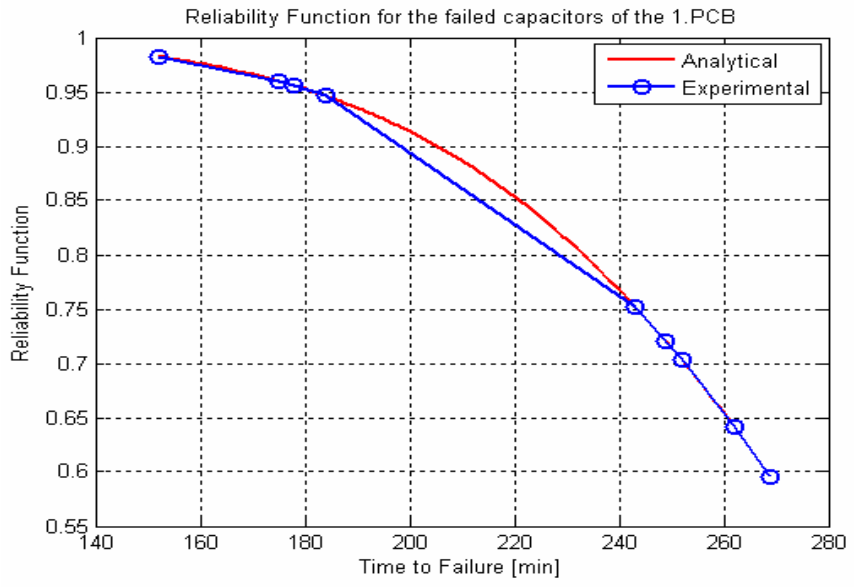
$$f(x)=\begin{cases} 0 & if \quad x<0 \\ \dfrac{b_w}{a_w}x^{b_w-1}e^{-\left(\frac{x}{a_w}\right)^{b_w}} & if \quad x>0 \end{cases} \tag{5.3}$$

The parameter b_w is called the shape parameter and the parameter a_w is called the scale parameter which determines the spread (scale) of the distribution [64][65]. The probability density functions, reliability functions and hazard rate functions for the fatigue life of the failed capacitors of the 1.PCB, 2.PCB and the 3.PCB could also be estimated. Figure 5.18, Figure 5.19 and Figure 5.20 show the estimated probability density functions together with the reliability functions for the 1. , 2. and 3. PCB respectively.

In addition, Figure 5.21 and Figure 5.22 show the hazard rate functions of the failed capacitors of the 1. , 2, & 3.PCB.

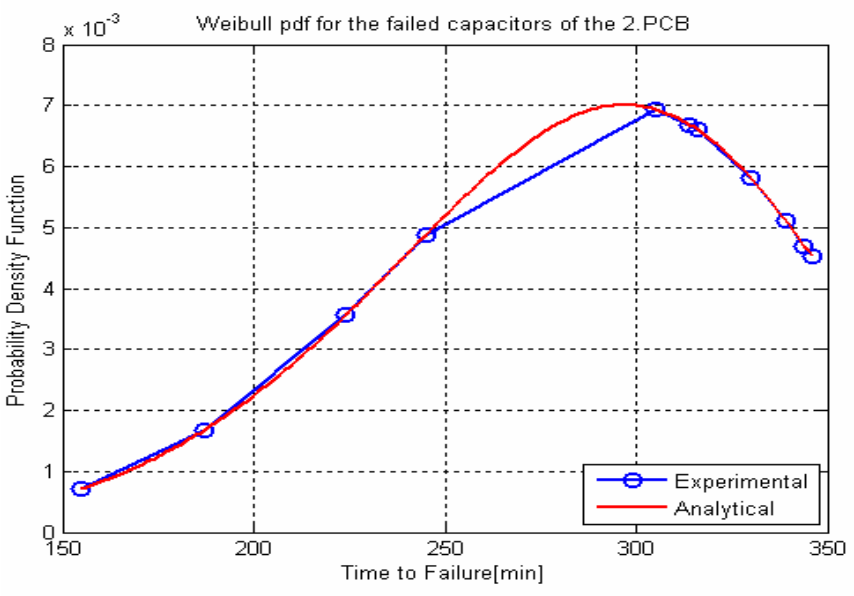


(a)

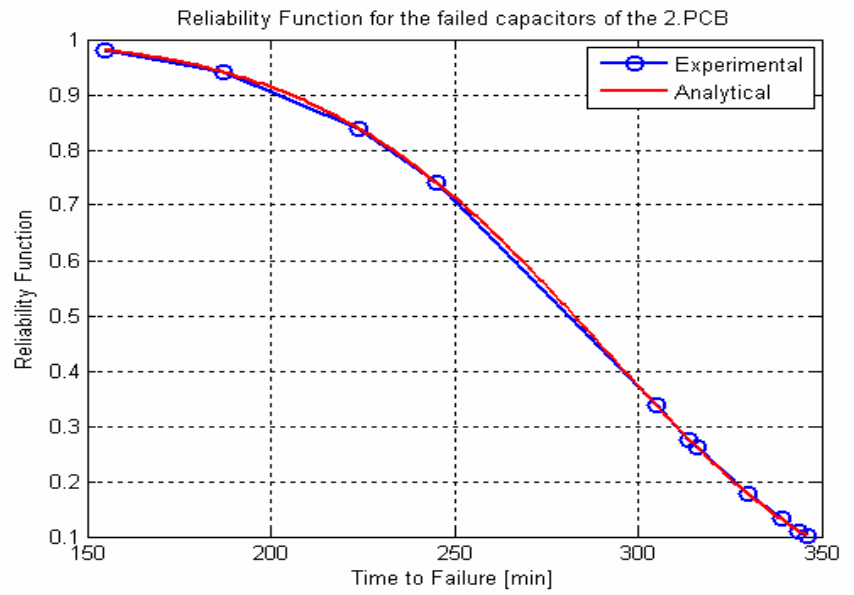


(b)

Figure 5.18: a) - Probability density function of the 1.PCB b) - Reliability function of the 1.PCB

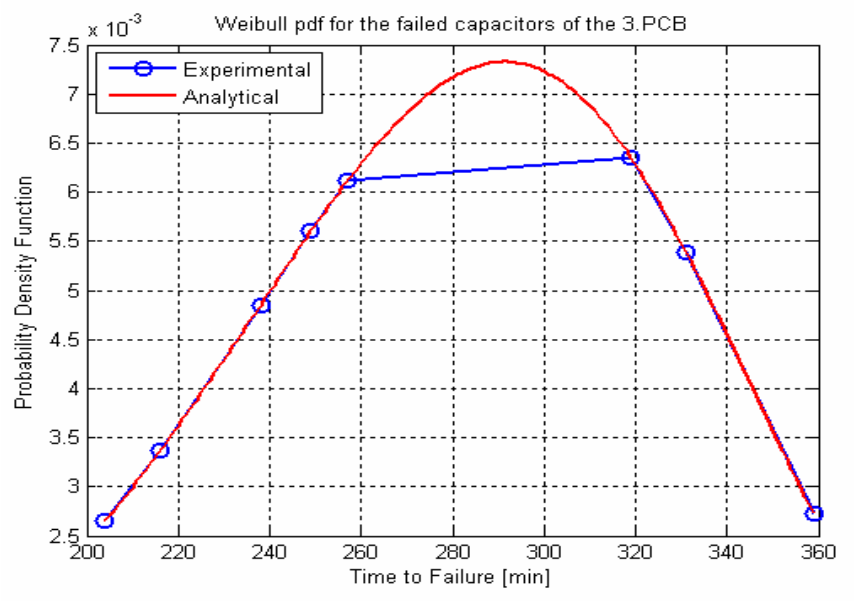


(a)

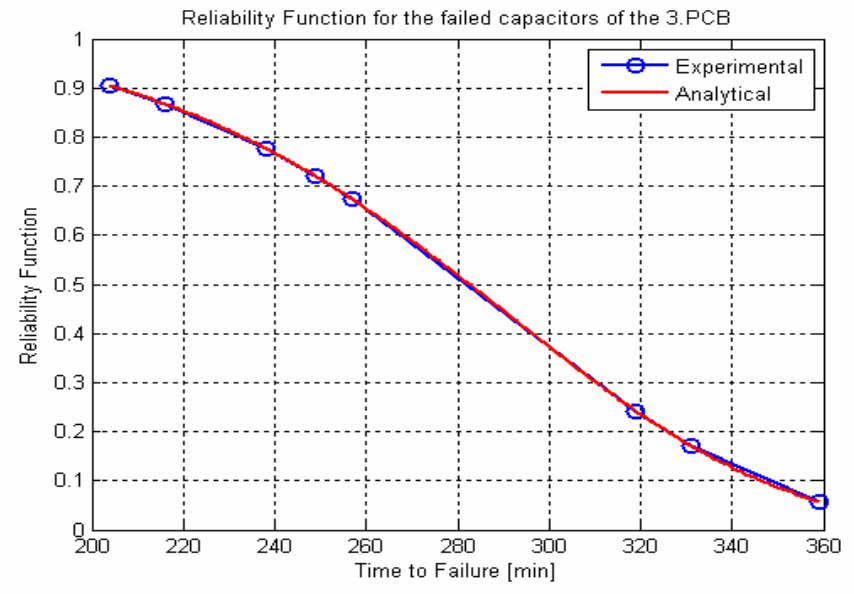


(b)

Figure 5.19: a) - Probability density function of the 2.PCB b) - Reliability function of the 2.PCB

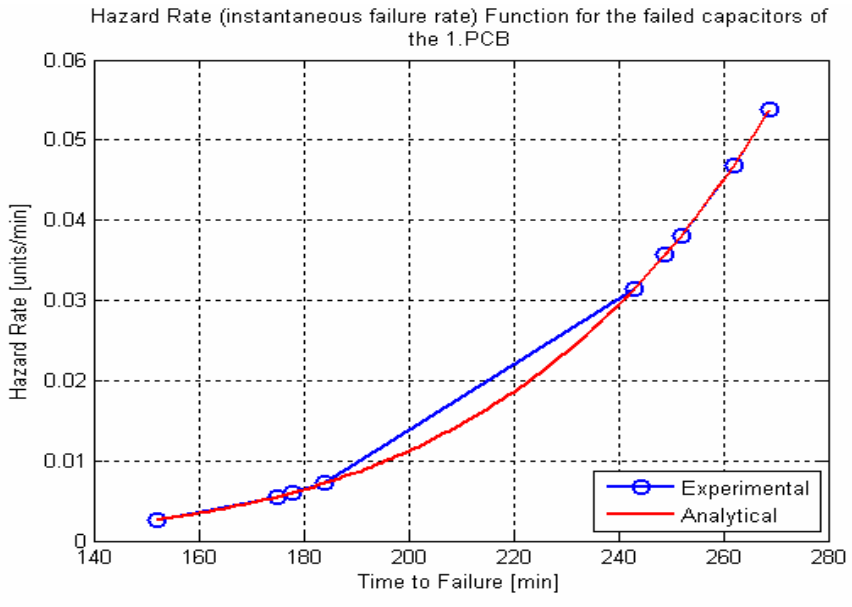


(a)

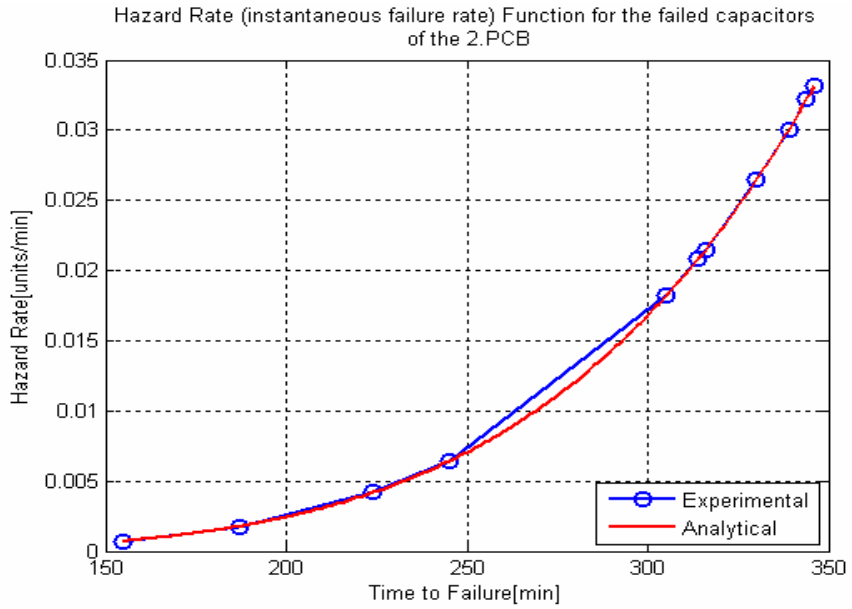


(b)

Figure 5.20: a) - Probability density function of the 3.PCB b) - Reliability function of the 3.PCB



(a)



(b)

Figure 5.21: a) Hazard Rate Function of the 1.PCB b) - Hazard Rate Function of the 2.PCB

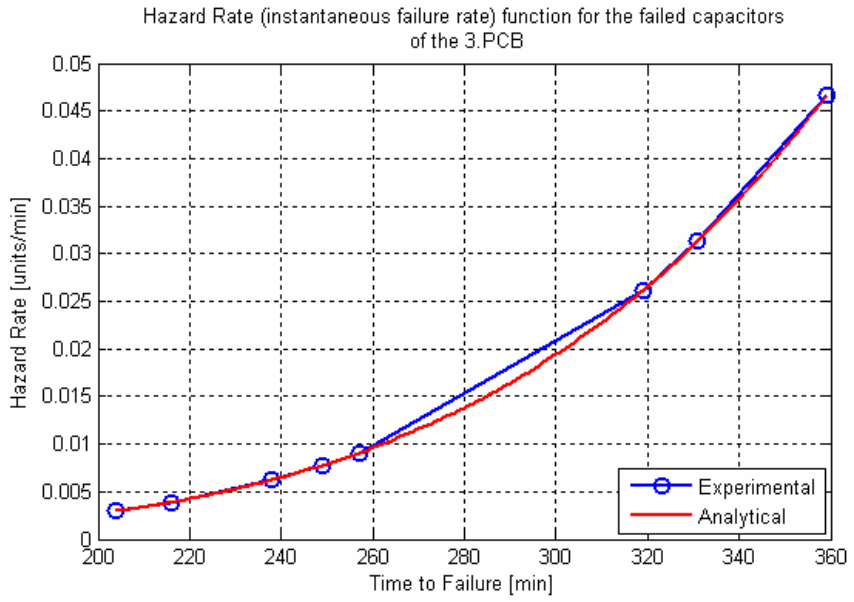


Figure 5.22: Hazard Rate Function of the 3.PCB

Fitting the test results (time to failure for the capacitors) to the Weibull distribution model, the values of a_w and b_w can be estimated. Table 5.5 shows the maximum likelihood estimates of these parameters.

Table 5.5: Weibull parameters and MTTF

Weibull Parameters	PCB 1	PCB 2	PCB 3
a_w**[min]**	2.357e+02	3.07e+02	3.007e+02
b_w	6.3e+00	5.8e+00	5.9e+00
MTTF[min]	2.192e+02	2.841e+02	2.787e+02

Since $b_w > 1$ the failure rate is increasing with time for the capacitors.In APPENDIX B there is a sample MATLAB m.file used to obtain the results presented in Figure 5.18, Figure 5.19, Figure 5.20, Figure 5.21, Figure 5.22 and Table 5.5.

5.6 Fatigue Testing & Analysis of PCB Populated with Plastic Dual Inline Package (PDIP)

In Figure 5.23 below, test PCB which is populated with 14 –Lead Plastic Dual-In-Line Packages (Fairchild MM74HC04 Hex Inverter) is shown. DIP is a package with two rows of leads extending at right angles from the base with standard spacing between the leads and row. This package is intended for through hole mounting.

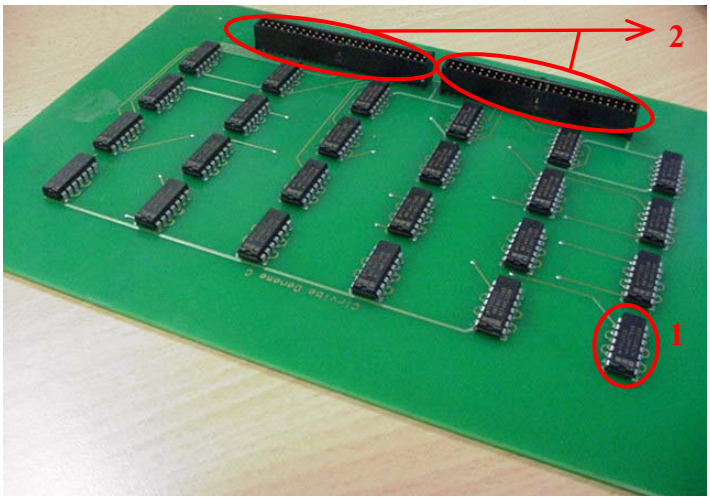


Figure 5.23: Test PCB populated with 14 lead PDIP, 1: Dual Inline Package, 2: Molex 2x25 pin type connector

There are two 2x25 type connectors used for the purpose of automatic damage detection infrastructure. Step Stress Accelerated Life Test (SST) was used again to create failure(s).

Previously, initial test level of 2 grms was used for the Tantalum capacitors/ However 2grms is likely to be mild for DIP component. Therefore the starting level (1.step for the DIP component) of the loading was selected to be 20-2000 Hz 3.13 grms (4.93×10^{-3} g^2/Hz) random vibration. Test (Figure 5.24) duration for

each step was chosen again to be 1 hour in order to provide high cycle fatigue occurrence.

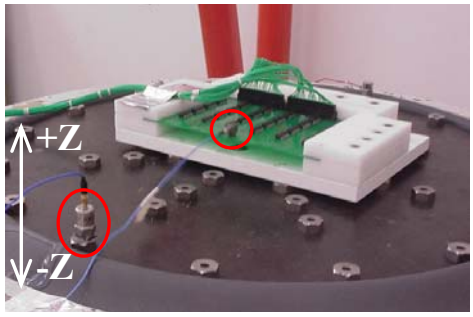
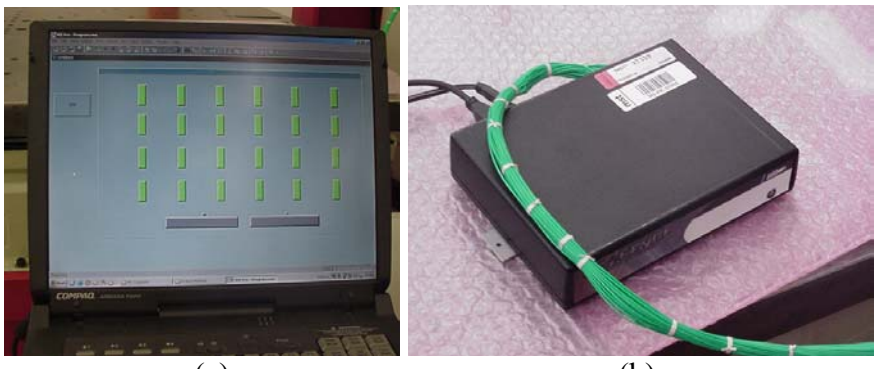


Figure 5.24: Step Stress Testing of PCB populated with PDIP (PCB 338B34 ±500g range accelerometer on the shaker table, PCB 356B21±500g range accelerometer on the PCB) [67])

In vibration testing of the PDIP in order to detect the damage automatically, an electrical test set-up was formed (Figure 5.25).Also in order to record accelerometer signals; IOTECH Data Acquisition System (Figure 5.26) was used.



(a) (b)

Figure 5.25: Automatic damage detection system components a)-Software built in Agilent Vee 6.2 for the visualization of the failed DIP(s) b) - C Port P10-96 (C level) 96 channel signal I/O test equipment

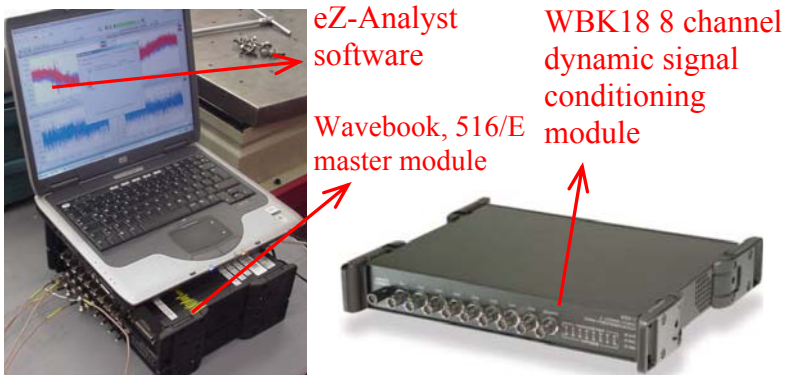


Figure 5.26: IOTECH 16 bit-1MHz Data Acquisition System with Ethernet Interface, WBK18 8 channel dynamic signal conditioning module and eZ-Analyst software 3.3.0.74 for the Wavebook, 516/E master module [68] used in order to examine and record accelerometer signals

Damage Detection System for the PCB populated with PDIP is explained in APPENDIX-B.

DIP construction is usually made of plastic or ceramics [69]. When there isn't any data available for the lead wire of dips, copper (for ceramic DIP) or nickel properties (for PDIP) could be used [47]. The tested DIPs are made of plastic. The lead wires of the package are made of a copper alloy (CDA194).The body of the package is a plastic epoxy material (epoxy resin) which is injection-molded to encapsulate the device/lead frame configuration [70]. Material properties of the PDIP (Figure 5.27) and connectors are obtained from the material database of Matweb [63].

Connector (Molex 2x25 pin type) properties are exactly the same as the properties listed in Figure 5.27 The overhang length and width for the 2x19 pin type connector are different than the ones for the 1X4 pin type connector.These values are 1.42 and 9.75 respectively. The PCB properties are the same as the one listed in Figure 5.8 except the effective weight of the PCB. The effective weight of the PCB populated with PDIP package is 120.77 grams. Furthemore; the

boundaryconditions of the PCB are the same as the boundary conditions shown in Figure 5.9.

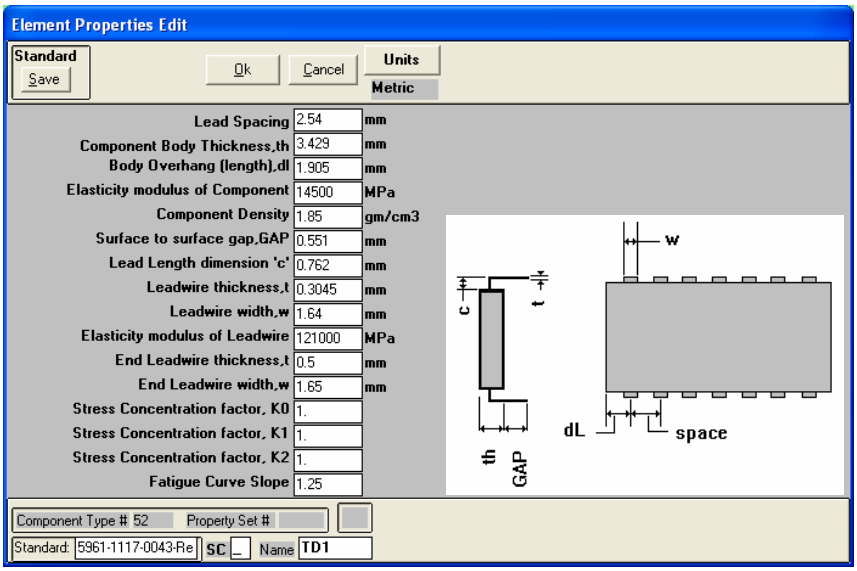


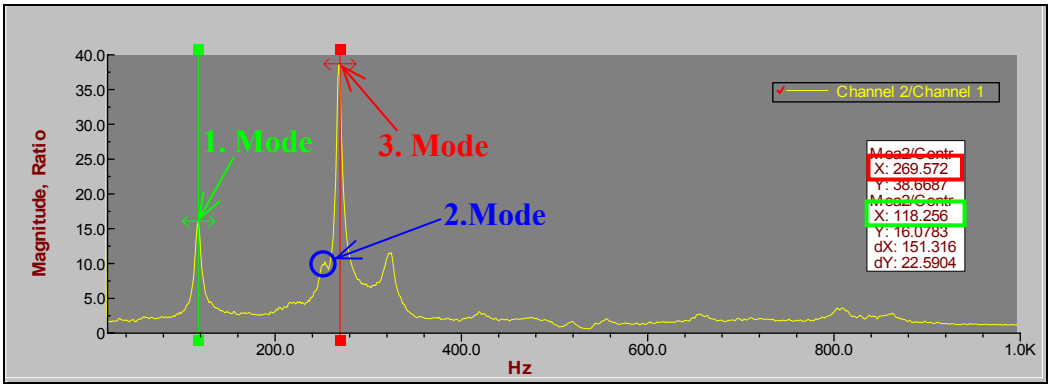
Figure 5.27: Plastic Dual Inline Package (PDIP) material and geometrical properties (vendor: Fairchild)

Step Stress Test vibration profiles which have been applied to the tested PCBs are listed in APPENDIX-D. The Step Stress Test of the PCB populated with PDIP was conducted up to the 14.step. But at the beginning section of the 14.step of the test (after 2.5 min passed) vibration shaker was interlocked (abort status) hence test was stopped.At the 14.step of the test, the input excitation was 36.44 grms (max instantaneous acceleration was around 150g) and the vibration shaker wasn't able to apply this vibration energy therefore this level was set to be the limit for the vibration shaker.Virtual accelerometers are again defined at the peak response locations (Table 4.1) in CirVibe in order to input the measured peak transmissibility's at these peak accelerometer locations.Resonance transmissibility's are defined at these accelerometer positions based on the data obtained from the transmissibility tests (Table 5.6).

According to the results represented in Table 5.6 it seems again that accuracy decreases with higher modes. In Figure 5.28 first three modes of the PCB were shown for the test points 1&2 (Figure 5.28a), test point 3 (Figure 5.28b) and test point 4 (Figure 5.28c) respectively.

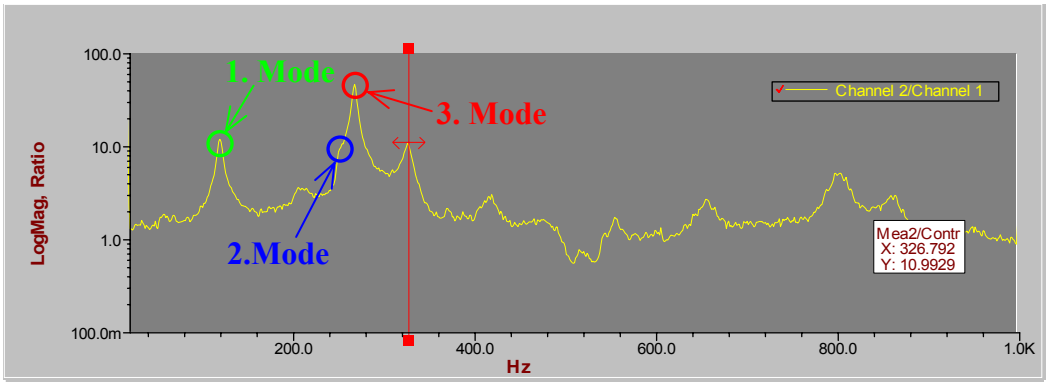
Table 5.6: Comparison of resonance frequencies and transmissibility's obtained by transmissibility tests & numerical analysis for the PCB populated with PDIP.

MODE #	NATURAL FREQUENCY [Hz]		
	TEST	SIMULATION	%DEVIATION
1	118.26	119.1	0.71
2	245.41	250.9	2.24
3	269.57	302.1	12.07
4	330.6	432.2	30.73
5	417.1	555.9	24.97
6	557	575.5	3.32
7	639.6	712.4	11.38
MODE #	TRANSMISSIBILITY		
	TEST	SIMULATION	%DEVIATION
1	16.08	10.16	36.81
2	22.27	25.81	15.92
3	38.67	33.04	14.56
4	14.59	53.86	72.91
5	2.76	76.55	96.4
6	2	80.37	97.51
7	2.3	108.79	97.88

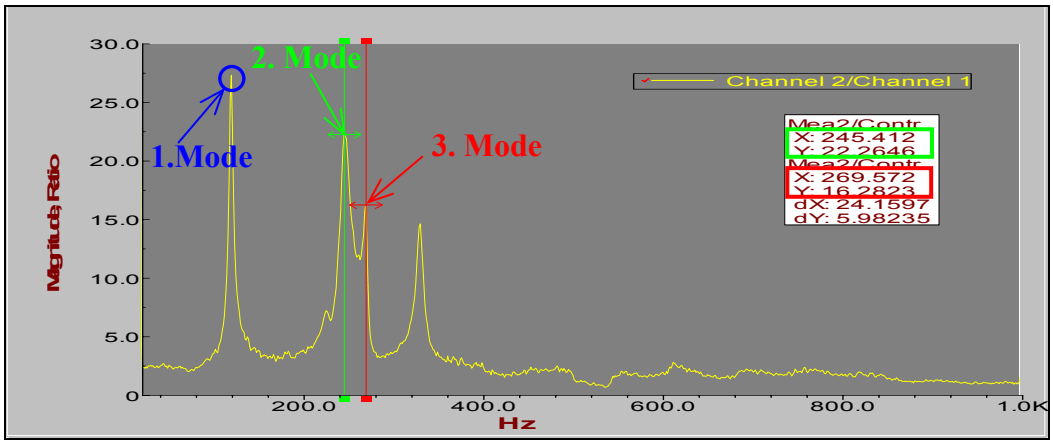


(a)

Figure 5.28: Transmissibility (Q) tests (random vibration 0.5grms white noise input freq range: 20-1000 Hz) a) - Q versus frequency plot for point 1 & 2



(b)



(c)

Figure 5.28 (continued): Transmissibility (Q) tests (random vibration 0.5grms white noise input freq range: 20-1000 Hz) b)- Q versus frequency plot for point 3 c) - Q versus frequency plot for point 4

If the transmissibility plot obtained from point 3 (Figure 5.28b) is investigated, it can be seen that 2.natural frequency is not seen clearly. This is most probably due to heavy modal coupling between 2. and 3.modes of the PCB .

There are a number of reasons why experimental and numerical (Finite Element Analysis) natural frequencies don't match. A significant one is that the boundary conditions might be different between the experimental and Finite Element Analysis (FEA). It is often difficult to reproduce in experimental tests (transmissibility tests or modal testing) the same boundary conditions that were used during the construction of the Finite Element Model (FEM).

Conversely, the flexibility of floors, platforms, mounts and all types of boundaries that could be assumed as rigid in an FEM may significantly affect the natural frequencies and mode shapes of the real structure [52].

At the end of the test there wasn't any apparent failure for the lead wires of the PDIP. As a matter of fact the pins are short and relatively large in cross-sectional dimension which makes them stiff and robust.

However analysis of the circuit board defines the damage values for all the components. The highest of these values defines a "lower limit of possible failure". Therefore it can be concluded that

$$d_{actual} \geq d_{test} \tag{5.4}$$

Where;

d_{test}: accumulated damage (maximum accumulated damage or lower limit of possible failure) for the most critical DIP on the PCB in the SST.

d_{actual}: accumulated damage at failure for the DIP which fails first.

Although d_{actual} was not defined by the SST it can be stated that without reaching this threshold fatigue damage index d_{test} there won't be any vibration induced fatigue failure for the tested PDIP.

Damage numbers accumulated at the end of the SST are listed for the PDIPs and connectors in APPENDIX-F. It can be concluded that the accelerated fatigue life of the most critical Plastic Dual-Inline Packages is at least equal to 782.53 minutes.

In terms of damage, the accumulated damage number for the PDIP named as TD3 (Figure 5.29) at the end of the Step Stress Test is $d_{actual} \geq d_{test} = 0.752E+04$.

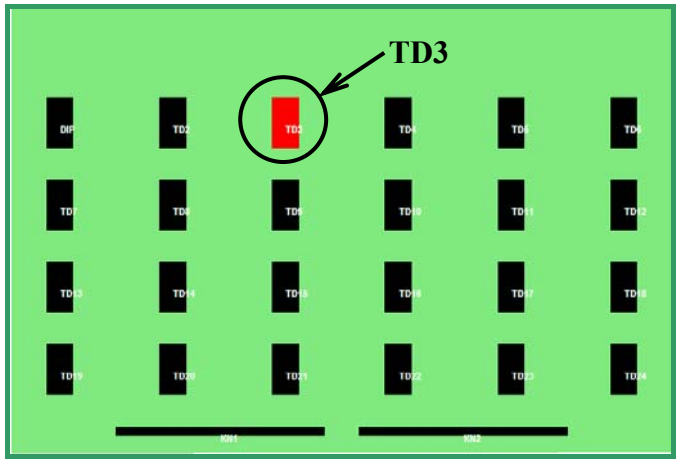


Figure 5.29: Most critical PDIP in terms of fatigue life on the PCB in the SST

5.7 Fatigue Testing & Analysis of PCB Populated with Aluminum Electrolytic Capacitors

Capacitors are generally divided into three categories, namely, tantalum, film and electrolytic capacitors.In Figure 5.30 test PCB which is populated with Aluminum electrolytic type capacitors is shown.

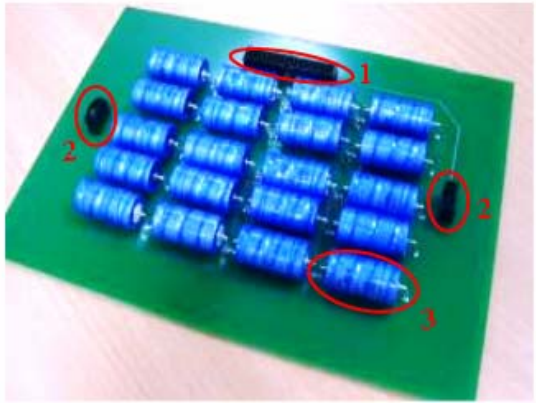


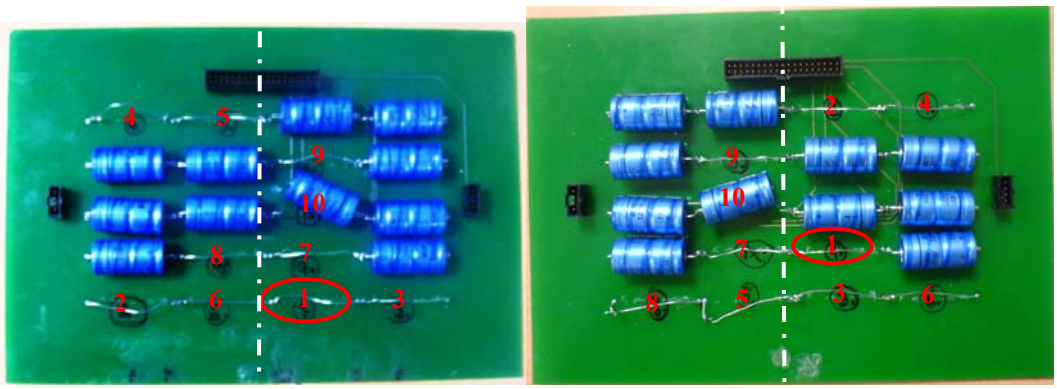
Figure 5.30: Test PCB populated with axial leaded Aluminum electrolytic capacitors (vendor: Philips) 1: Molex Connector (2x19 pin type), 2: Molex Connector (1x4 pin type), 3: Aluminum Electrolytic Capacitor (100 μF)

Similarly, Step Stress Accelerated Life Tests (SST) of the 2 circuit boards were performed. Tests were both conducted up to the 8.step for the 1.PCB and the 2.PCB's. During these tests 10 failures were detected for the 1. and 2.PCB.The number of failures were adequate so that tests were not carried on after 8.step. For the first tested PCB all the failures were due to flexure stress developed at the junction of the lead and component body but for the 2.tested PCB some of the failures were observed at the solder joints.

In vibration testing of the PCB in order to detect the damage, an electrical test set-up was again formed which was used before in the testing of Tantalum capacitors. Damage Detection System for the PCB populated with axial leaded aluminum electrolytic capacitors is same as the one explained in APPENDIX-A. In addition, accelerometers were also used on the PCB. Vibration signals from these accelerometers were recorded by IOTECH 16 bit-1MHz Data Acquisition System.

Figure 5.31 shows the test PCBs (PCB 1 & PCB2) at the end of the SST with the failed capacitors are also shown (capacitors failed at first are shown in the red oval) for each of the printed circuit boards.

Table 5.7 shows laboratory test results (accelerated life tests) of the SST for the PCB's populated with Aluminum electrolytic capacitors.



(a) (b)

Figure 5.31: Test PCB after Step Stress Tests a)-1.PCB b)-2.PCB

The gap between the component body and the PCB affects the lead length and as a result the stiffness of the lead wire. Aluminum electrolytic capacitors are larger than the Tantalum capacitors. The gap between the component body and the PCB is smaller for the Aluminum electrolytic capacitors causing a shorter lead length which increases the stiffness of the aluminum electrolytic capacitor. This might be emphasized as one of the reasons that the Aluminum electrolytic capacitors failed afterwards.

Table 5.7: Capacitor Failure Times in SST (Accelerated Lives)

	Failure Time [min]			
Failure Sequence	PCB 1	PCB 2	Standard Deviation	Arithmetic Mean
1.failure	363.6	334.2	14.7	348.9
2.failure	402.9	355.3	23.8	379
3.failure	425.5	390.3	17.6	407.9
4.failure	440.3	427	6.6	433.6
5.failure	442.8	437	2.8	440
6.failure	449	437	5.9	443
7.failure	449	441.3	3.9	445.2
8.failure	455.9	462	3	459
9.failure	457.8	467.4	4.8	462.6
10.failure	466.3	469	1.4	467.7

Table 5.7 indicates the similar fatigue behavior of the capacitors (especially from 4.failure to 10.failure) on the PCB 1 and PCB 2 according to the failure times (life capabilities). Standard deviation in Table 5.7 represents the measure of fatigue life scatter. The relative damage numbers for the 1. failed aluminum electrolytic capacitors mounted on the 1. and 2.tested PCB were calculated as 170555.444 (damage at 3.567 min of the 7.step) and 68056 (damage at 34.167 min of the 6.step) respectively.

Material and geometrical properties list of the 1x4 pin type connector is identical to the properties listed in Figure 5.7.

The overhang length and width for the 2x19 pin type connector are different than the ones for the 1X4 pin type connector.These values are 1.42 and 9.75 respectively.

Figure 5.32 shows material and geometrical properties list of the axial leaded Aluminum electrolytic capacitor (100 μF) analyzed. Capacitor body (Aluminum) elastic modulus and component body density are 68GPa and 2.6989 gr/cm^3 respectively. The lead wire of the capacitor is copper-based alloy with average elastic modulus of 122.5 GPa.

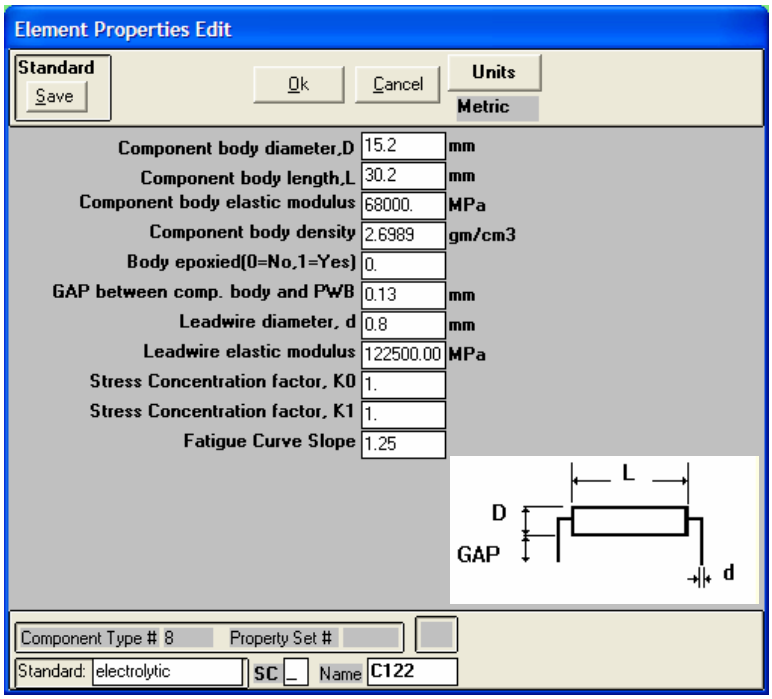


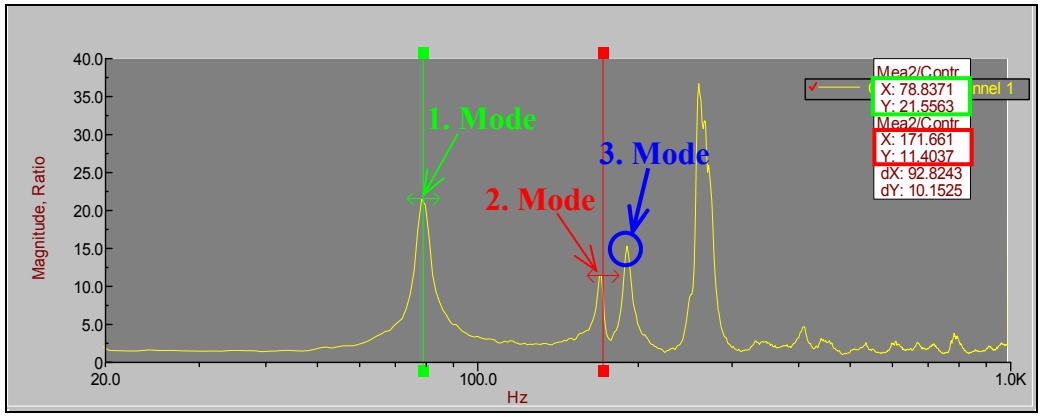
Figure 5.32: Axial leaded Aluminum Electrolyte Capacitor material and geometrical properties

PCB properties are the same as the one listed in Figure 5.8 except the effective weight of the PCB. The effective weight (weight of the PCB bordered by the fixture or in other words the weight of the visible portion of the PCB in its fixture) of the PCB populated with Aluminum electrolytic capacitors is 243.23 grams.

In addition; the boundary conditions of the PCB are the same as the boundary conditions shown in Figure 5.9. Virtual accelerometers are again defined at the peak response locations (Table 4.1) in order to input the measured peak transmissibility's at these peak accelerometer locations. Resonance transmissibility's are obtained from transmissibility tests (Table 5.8). Natural modes and corresponding transmissibility's are obtained by observing the transmissibility plots (Figure 5.33) which were attained experimentally from the accelerometer locations given in Table 4.1. The capacitors on the PCB are named as shown in Figure 5.34.

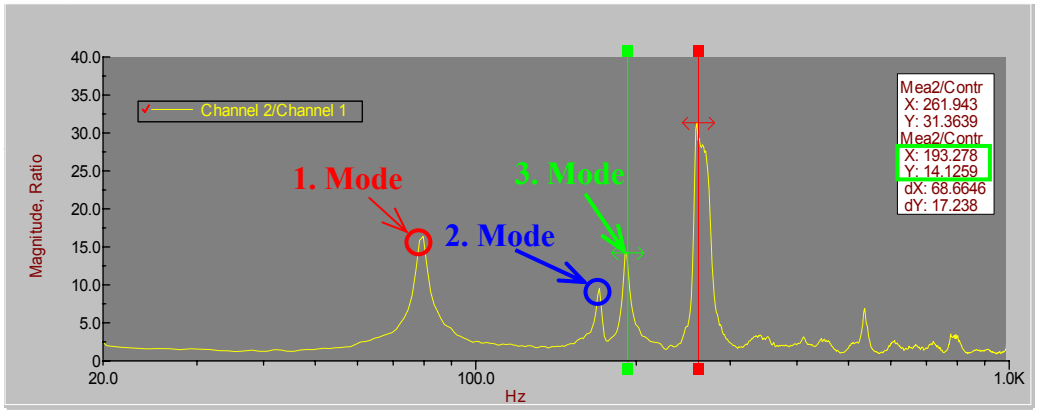
Table 5.8: Comparison of resonance frequencies and transmissibility's obtained by transmissibility tests & numerical analysis for the PCB populated with aluminum electrolytic capacitors.

MODE #	NATURAL FREQUENCY			TRANSMISSIBILITY		
	TEST	SIMULATION	%DEVIATION	TEST	SIMULATION	%DEVIATION
1	78.84	90.16	14.36	21.56	7.39	65.86
2	171.66	194.53	13.32	11.4	18.56	38.56
3	193.28	227.81	17.87	14.13	22.75	37.9
4	264.49	333.15	25.96	31.36	37.7	16.83
5	272.11	434.1	59.53	24.11	54.19	55.51
6	339.5	435.46	28.27	3	54.42	94.46
7	399.3	535.58	34.13	3	72.63	95.8



(a)

Figure 5.33: Transmissibility (Q) tests (random vibration 0.5grms white noise input freq range: 20-1000 Hz) a) - Q versus frequency plot for point 1 & 2



(b)

Figure 5.33 (continued): Transmissibility (Q) tests (random vibration 0.5grms white noise input freq range: 20-1000 Hz) b) - Q versus frequency plot for point 3

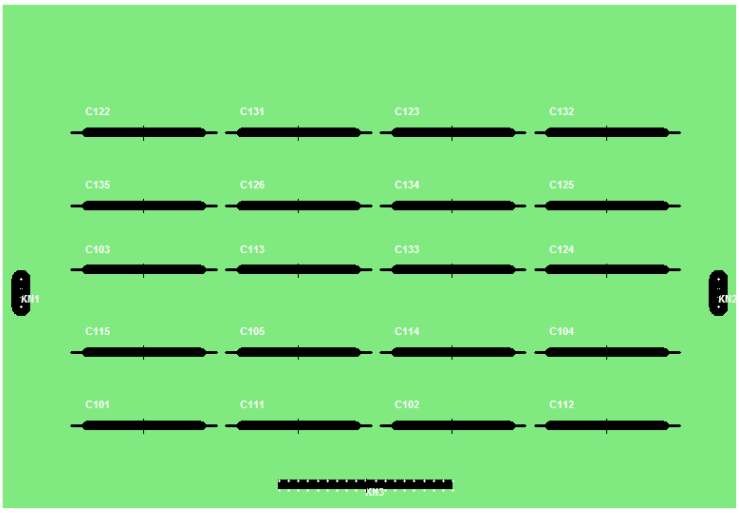


Figure 5.34: Designation of Aluminum electrolytic capacitors on the test PCB

The relative damage numbers and the total accumulated damage numbers for the failed capacitors on the test PCB's are listed in APPENDIX-G. If the test failure distribution of the printed circuit boards are compared it can be realized that the failures are symmetrical with respect to the axis passing from the middle of the PCB (Figure 5.31).This implies the consistency of failure locations observed in the vibration tests of the PCBs. For both of the test PCBs the capacitor which failed first in the tests is found to fail in the third place.

This level of accuracy is found to be sufficient enough for systems involving electronic components for which the scatter range is very large. Also, the simulation and test results obtained for the 2.PCB agree better than for the 1.PCB (Table 5.9).The inconsistencies encountered can be due to the large variations in acceptable dimensions for these components whose effects on fatigue life can be reflected into the simulation up to a certain extent.

Table 5.9: Comparison of the failure rank for test and simulation results

PCB1		**PCB 2**	
Test	**Simulation**	**Test**	**Simulation**
1.	**3.**	**1.**	**3.**
2.	4.	**2.**	**1.**
3.	5.	3.	4.
4.	2.	4.	2.
5.	**1.**	5.	7.
6.	8.	6.	5.
7.	7.	7.	8.
8.	9.	8.	9.
9.	6.	9.	6.
10.	10.	10.	10.

5.8 The Weibull Model in Life Testing of Aluminum Electrolytic Capacitors

The probability density functions, reliability functions and hazard rate functions for the fatigue life (in terms of time) of the failed aluminum electrolytic capacitors of the 1.PCB and the 2.PCB have been evaluated. Figure 5.35, Figure 5.36, Figure 5.37 and Figure 5.38 show the estimated probability density functions together with the reliability functions for the 1. & 2. PCB respectively.

Moreover, Figure 5.39 & Figure 5.40 show the hazard rate functions of the failed capacitors of the 1. & 2.PCB.

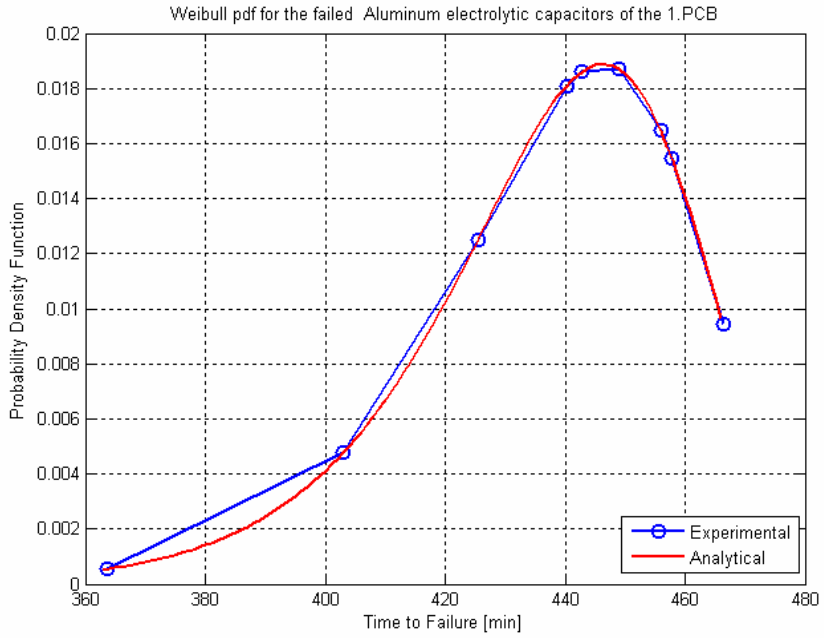


Figure 5.35: Probability density function of the 1.PCB

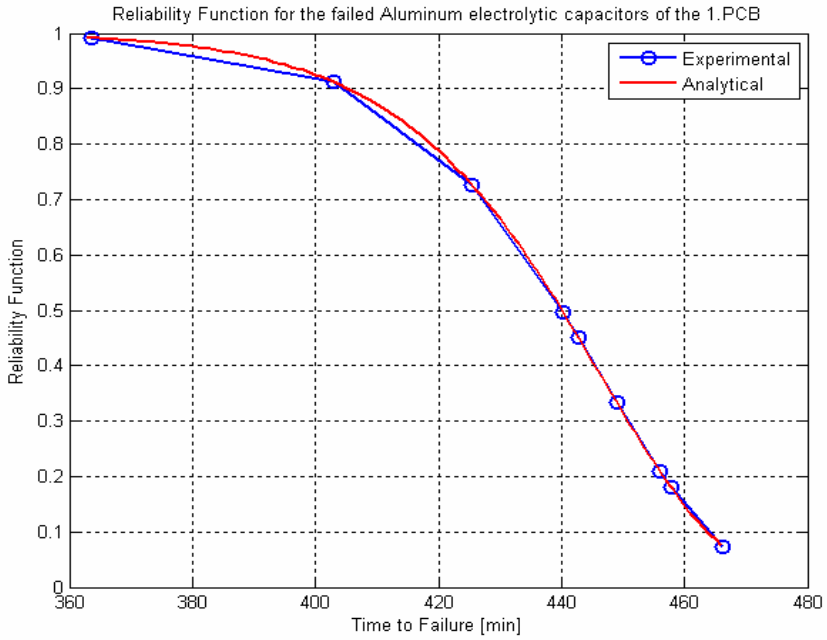


Figure 5.36: Reliability function of the 1.PCB

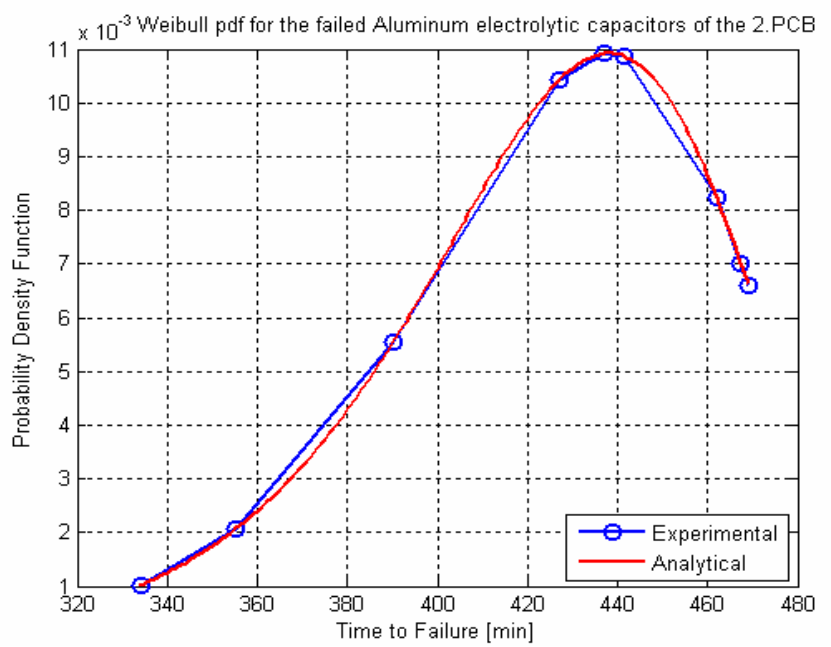


Figure 5.37: Probability density function of the 2.PCB

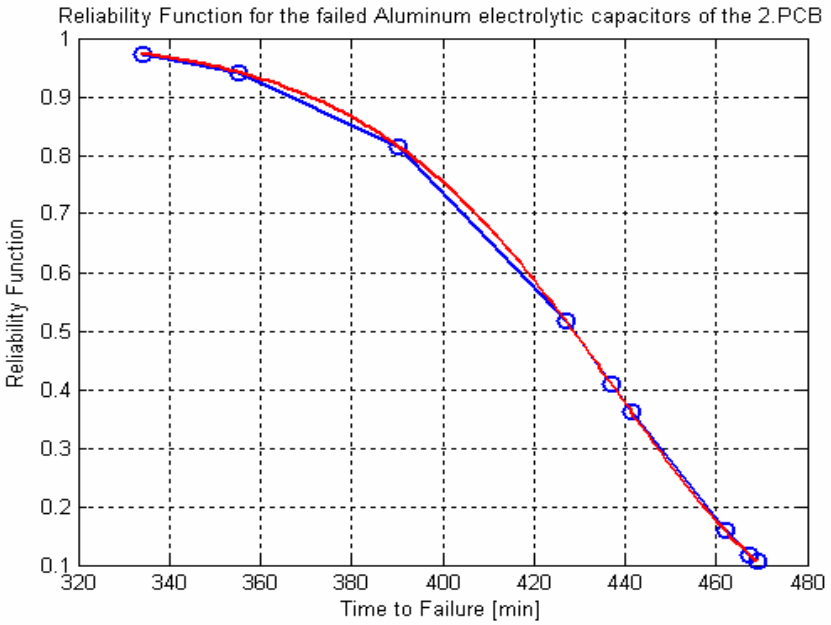


Figure 5.38: Reliability function of the 2.PCB

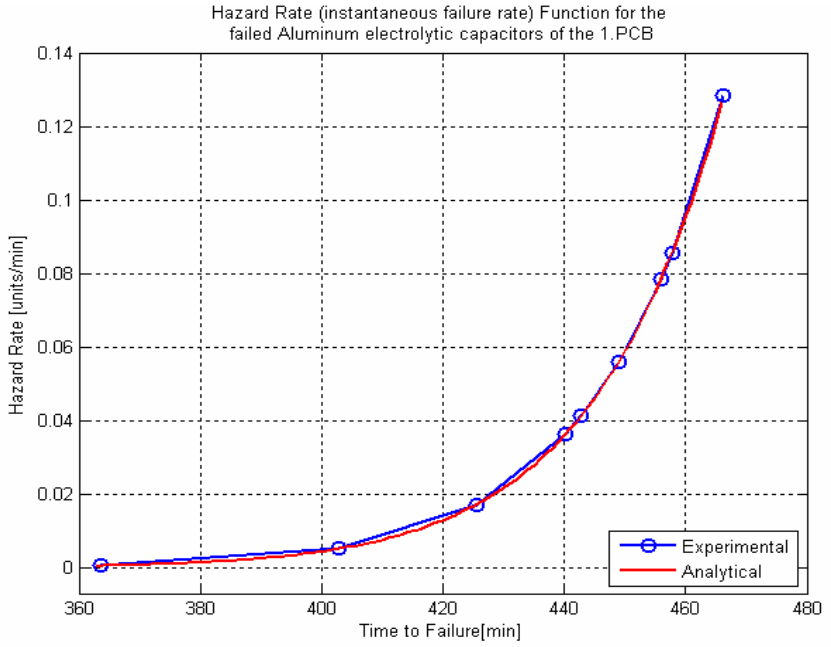


Figure 5.39: Hazard Rate Function of the 1.PCB

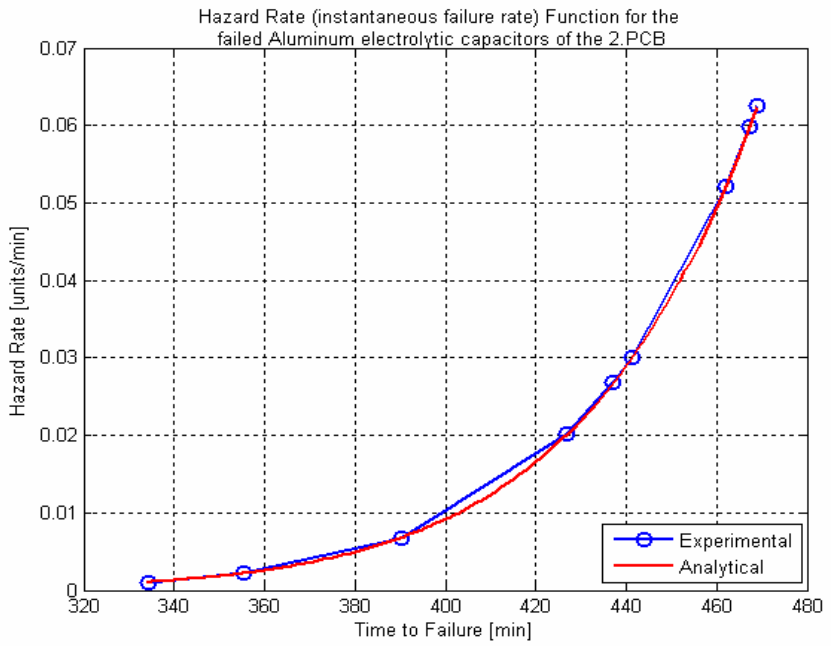


Figure 5.40: Hazard Rate Function of the 2.PCB

Again by fitting the test results (time to failure for the capacitors) to the Weibull distribution model, the Weibull parameters can be estimated. Table 5.10 shows the maximum likelihood estimates of these parameters.Since $b_w > 1$ the failure rate is increasing with time for the aluminum capacitors.

Table 5.10: Weibull parameters and MTTF for the aluminum capacitors

Weibull Parameters	PCB 1	PCB 2
a_w**[min]**	4.472e+002	4.408e+002
b_w	2.29e+001	1.3e+001
MTTF[min]	**4.367e+002**	**4.237e+002**

Sample MATLAB m.file used to obtain the results presented in Figure 5.35-Figure 5.40 and Table 5.10 is given in APPENDIX-C.

5.9 Fatigue Testing & Analysis of PCB Populated with Aluminum Electrolytic Capacitors with Epoxy (Eccobond 55) Reinforcement

In electronic industry most of the time components like axial leaded capacitors or resistors are secured to the circuit boards using epoxy (eccobond) or silicone. Epoxy is an adhesive, especially an epoxy resin which is technically and economically attractive alternative to mechanical fasteners and becoming more and more accepted as a cost-effective production method in the aerospace, automotive, marine, construction, mechanical and electrical/electronic industries.

The components are fixed with epoxy resin onto printed circuit boards over their surface to enable them to withstand vibration or impact. Therefore it is desired to see the effects of adhesive bonding (epoxy reinforcement) on the fatigue lives of the electronic components. Printed Circuit Board populated with axial leaded aluminum capacitors are reinforced with epoxy resin (eccobond 55) as shown in Figure 5.41.

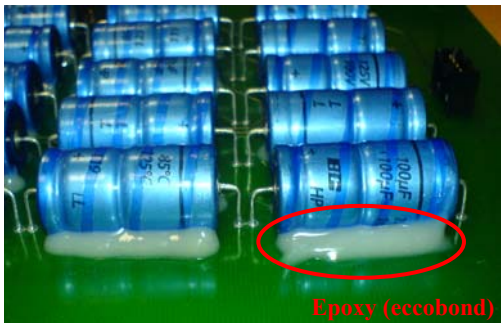


Figure 5.41: Epoxy (supplier: Emmerson & Cuming Inc.) bonding with eccobond 55 applied to PCB populated with axial leaded aluminum capacitor

Soldered connections were kept free from free of epoxy for further wiring which may be required for damage detection system.In vibration testing of the PCB, an electrical test set-up was again used in order to detect the damage which was used before. Furthermore, accelerometers were again used on the PCB and vibration signals from these accelerometers were recorded by IOTECH 16 bit-1MHz Data Acquisition System.Step Stress Accelerated Life Test (SST) was done again to create failure(s). Step duration and starting test level were chosen to be the same as the SST of the PCBs populated with aluminum electrolytic capacitors. SST was performed up to the 12.step. During the test 10 failures were detected for the PCB. The number of failures were adequate so that tests were not carried on after 11.step.All of the failures were observed at the junction of the lead and component body (Figure 5.42).

(a) (b)

Figure 5.42: a) - Sample failure for the capacitor reinforced with epoxy resin b) - Damage detection

Figure 5.43 represents the test PCB at the end of the SST with the failed capacitors bonded with epoxy resin onto printed circuit board (capacitor failed at first is shown in the red oval).

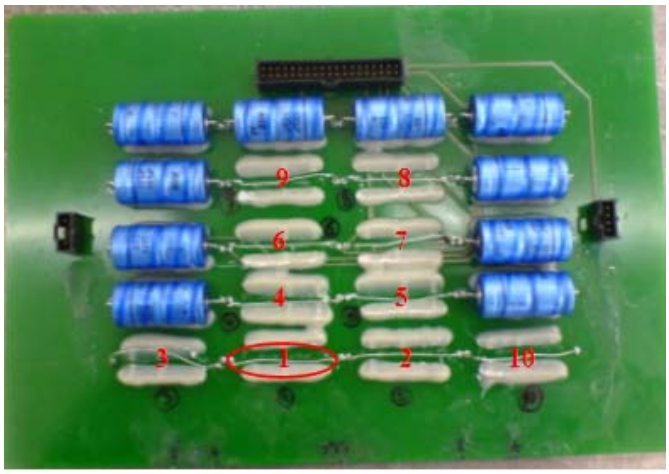


Figure 5.43: Epoxy reinforced PCB populated with aluminum capacitors at the end of the SST

Table 5.11 lists the laboratory test results (vibration life testing) of the SST for the PCB's populated with Aluminum electrolytic capacitors which were reinforced by eccobond 55.

Table 5.11: Capacitor Failure Times in SST (Accelerated Lives)

Failure Sequence	Failure Time [min]
1.failure	416.8
2.failure	495.6
3.failure	504.5
4.failure	504.5
5.failure	522.2
6.failure	550.1
7.failure	564.9
8.failure	637.7
9.failure	660
10.failure	660

In this situation, the body of the axial leaded Aluminum capacitor should be selected as epoxied in the element properties list (Figure 5.44).

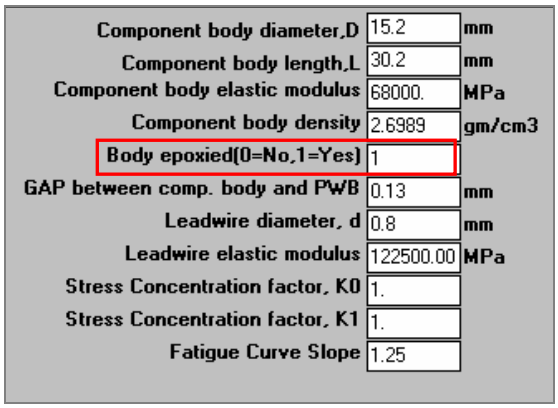


Figure 5.44: Epoxy reinforced axial leaded aluminum electrolyte capacitor material and geometrical properties

PCB properties into Circuit Board Properties are the same as the one listed in Figure 5.8 except the effective weight of the PCB. The effective weight of the PCB populated with epoxy reinforced Aluminum electrolytic capacitors is 261.23 grams. In addition; the boundary conditions of the PCB are the same as the boundary conditions shown in Figure 5.9. Moreover, when the body of the component is epoxied, it removes the inertial components of stress. Therefore the only lead wire stress calculated in CirVibe are those associated with modal displacement forced on the lead wires.

The relative damage number for the 1. failed aluminum electrolytic capacitor secured to the circuit board using eccobond 55 is calculated as 1058333.2 (damage at 56.8 min of the 7.step of the SST).

In order to obtain the resonance transmissibility's of the PCB for each modes accelerometers are placed at the peak response locations as shown in Figure 5.45.Three PCB model 356B21 ±500g tri-axis miniature [67] and 1 Endevco model 2226C ± 1000 g single axis miniature accelerometers [71] were placed on

the PCB. 1 PCB 356A16 ±50g tri-axis accelerometer [67] was placed on the shaker table in order to record the input acceleration.

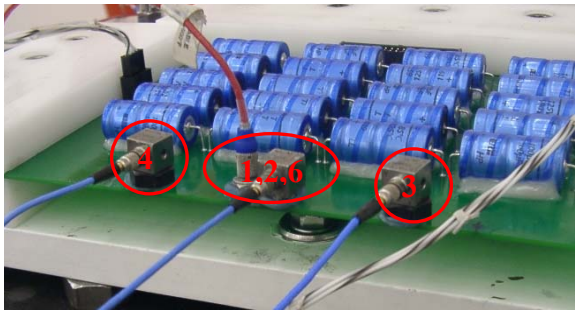


Figure 5.45: Peak response locations for mode 1, 2, 3 and 4 on the PCB

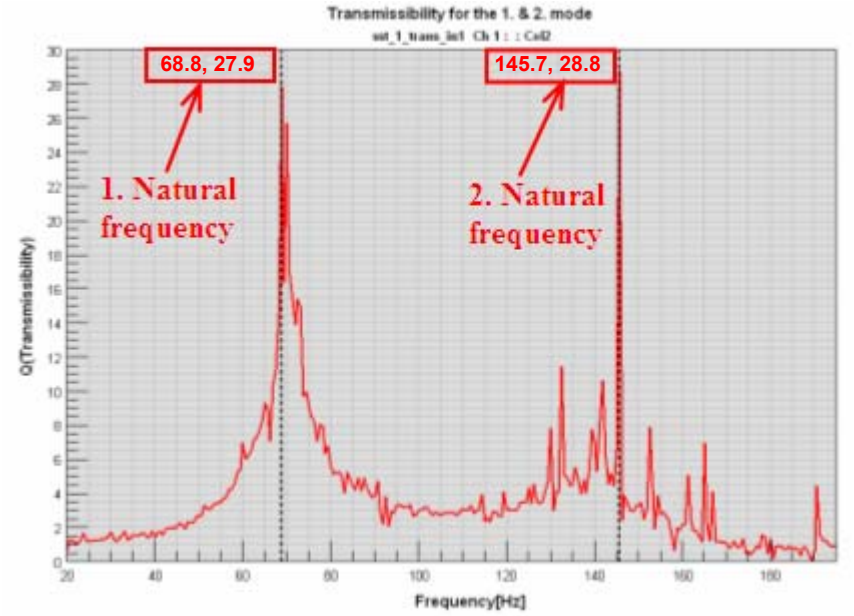
Transmissibility of the circuit board under random vibration can be found from the PSD (power spectral density) of the input and PSD of the response points. If the PSD of the input acceleration is represented with $G_{in}(f)$ and PSD of the response acceleration points are represented by $G_{out}(f)$ then transmissibility is given by;

$$Q(f) = \sqrt{\frac{G_{out}(f)}{G_{in}(f)}} \tag{5.5}$$

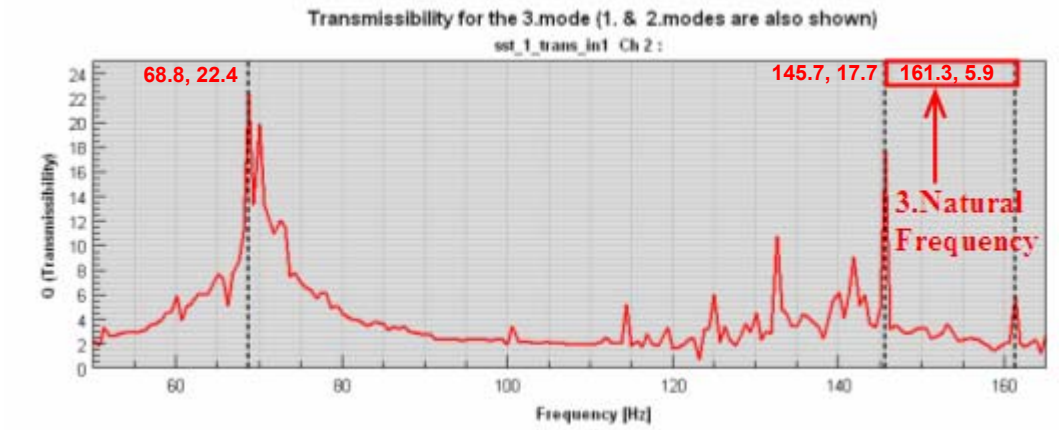
Printed circuit boards are very complex structures with characteristics that make accurate predictive analysis nearly impossible. For electronic systems material properties have huge variations, dimensional tolerances are large. Besides, the boundary conditions in test conditions can not be fully described in simulation.

Furthermore, higher modes of the PCB's are difficult to excite with single axis excitation. As a matter of fact the strains hence the stresses will be lower at higher modes so that the contribution of fatigue damage due to stresses at higher modes of the PCB will not be as significant as the contribution of the lower modes. Due to all these reasons, only first three modes will be considered in fatigue analysis of the PCB.

Hence resonance transmissibility's for the 1. , 2. , 3. & 4. modes (additional) of the PCB which were obtained from the data collected during SST are represented in Figure 5.46a, Figure 5.46b and Figure 5.46c, respectively.

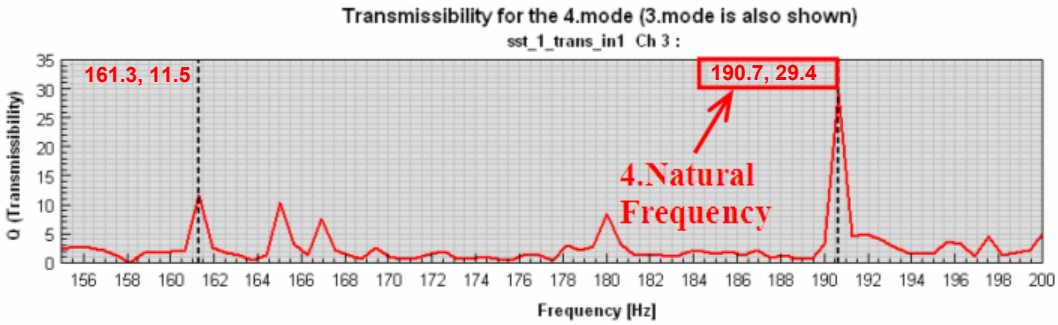


(a)



(b)

Figure 5.46: Transmissibility (Q) versus frequency obtained from SST test (random vibration 2grms white noise input freq range: 20-2000 Hz) a) - Q versus frequency plot for 1. & 2.mode at point 1, 2 & 6 a) 1.mode (68.8 Hz, Q=27.9) & 2.mode (145.7 Hz, Q=28.8) b)- 3.mode (161.3 Hz, Q=5.9) (1. & 2. modes are also shown)



c)

Figure 5.46 (continued): Transmissibility (Q) versus frequency obtained from SST test (random vibration 2grms white noise input freq range: 20-2000 Hz) c) - Q versus frequency plot for 4.mode at point 4 (190.7 Hz, Q=29.4) (3.mode is also shown)

In Table 5.12 resonance frequencies and transmissibility's obtained from simulation and test are compared for the PCB with eccobond reinforcement.

Table 5.12: Comparison of resonance frequencies and transmissibility's obtained by transmissibility tests & numerical analysis for the aluminum electrolytic capacitors with eccobond coating

MODE #	NATURAL FREQUENCY [Hz]			TRANSMISSIBILITY		
	TEST	SIMULATION	%DEVIATION	TEST	SIMULATION	%DEVIATION
1.	68.8	69.3	0.6	27.9	5.5	80.1
2.	145.7	131.6	9.6	28.8	11.4	60.3
3.	161.3	165.6	2.6	11.5	15.2	31.2
4.	190.7	243.2	27.6	29.4	24.8	15.8
5.	201.3	283.9	41	19.9	30.4	52.9
6.	206.9	289.4	39.9	11	31.2	>100
7.	254.4	338.2	32.9	10.3	38.5	>100

Virtual accelerometers are again defined on the PCB (Figure 5.45 is the actual configuration) at the peak response locations (Table 4.1) in CirVibe in order to enter the measured peak transmissibility's as input test data which will be used in the fatigue analysis.

In CirVibe local weights are defined at the center of gravity of the components and at locations where accelerometers are placed. The purpose of the local weight is to cover a case where distributed weight is not representative of the average weight distribution by a significant amount. Therefore, the local mass loading effects of eccobond coating and accelerometers are incorporated into the analysis.

The relative damage numbers and lists of total accumulated damage numbers for the failed epoxy coated capacitors. on the test PCB's are given in APPENDIX-H. Attaching the capacitors to the PCB with epoxy changes the dynamic characteristics of the PCB (compared to the case where there is no epoxy reinforcement) hence it considerably affects the failure distribution due to its mass and stiffness effects. The simulation and test results obtained are compared in Table 5.13 below:

Table 5.13: Comparison of the failure rank for test and simulation results

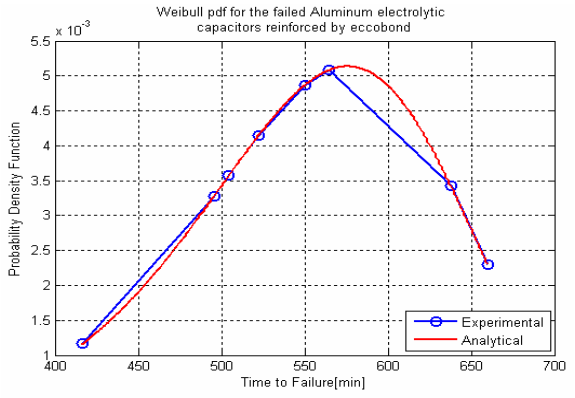
PCB with epoxy coating	
Test	**Simulation**
1.	**1.**
2.	7.
3.	**3.**
4.	2.
5.	8.
6.	**6.**
7.	9.
8.	5.
9.	4.
10.	**10.**

The inconsistencies encountered can be again due to the large variations in component material and geometrical properties whose effects on fatigue life can be reflected into the simulation to a certain extent.

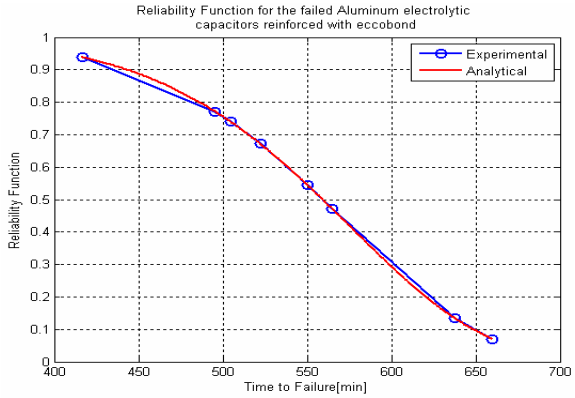
Nevertheless in order to increase the accuracy the number of circuit boards tested can be increased. However in this study, the capacitor which failed first in the test (capacitor C123) is found to fail also first in the simulation. Hence the level of accuracy is found taken be again sufficient for such a structure for which the scatter range is very large.

5.10 The Weibull Model in Life Testing of Aluminum Electrolytic Capacitors reinforced with epoxy coating (eccobond 55)

The pdf, reliability and hazard rate functions for the fatigue life of the failed aluminum electrolytic capacitors are evaluated (Figure 5.47**)**.



(a)



(b)

Figure 5.47: a)-Probability density function of the capacitors reinforced with epoxy b)- Reliability function of the capacitors reinforced with epoxy

Hazard rate function of the failed capacitors is also given in Figure 5.48.

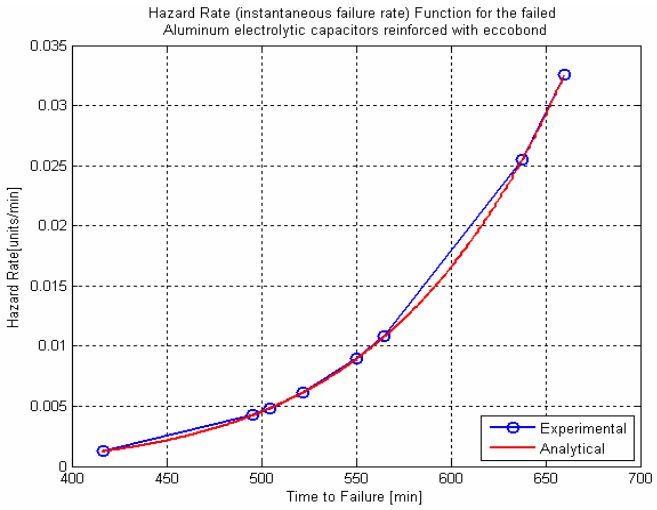


Figure 5.48: Hazard Rate Function of the capacitors reinforced with epoxy

Again by fitting the test results (time to failure for the capacitors) to the Weibull distribution model, the Weibull parameters are estimated. Table 5.14 shows the maximum likelihood estimates of these parameters. Since $b_w > 1$ the failure rate is increasing with time for the capacitors

Table 5.14: Weibull parameters and MTTF for the epoxied aluminum capacitors

Weibull Parameters	PCB with epoxy
a_w**[min]**	5.85e+02
b_w	8.1e+00
MTTF[min]	**5.514e+02**

It is put forward that the epoxy coating under the capacitor body has a positive effect on the fatigue life. If the mean-time-to-failure of the capacitor with epoxy coating and the capacitor without epoxy coating are compared it can be seen that epoxy coating increases the fatigue life.

In accelerated life testing of the capacitors it was determined that the MTTF for the capacitor without epoxy coating were found to be 436.719 min and 423.714 min for the 1. test PCB and 2. test PCB respectively.

On the other hand MTTF for the capacitor with epoxy reinforcement was determined as 551.4 min as shown in Table 5.14.Therefore the epoxy coating increases the fatigue life of the capacitor about 30%. However the disadvantage of the eccobond coating is such that it can be removed from the component with difficulty. Therefore sometimes component can be sacrificed.

5.11 Fatigue Testing & Analysis of PCB Populated with Aluminum Electrolytic Capacitors with Silicone Reinforcement

One alternative method of fixing the components onto printed circuit boards over their surface to enable them to withstand vibration or impact is by silicone reinforcement (Figure 5.49).

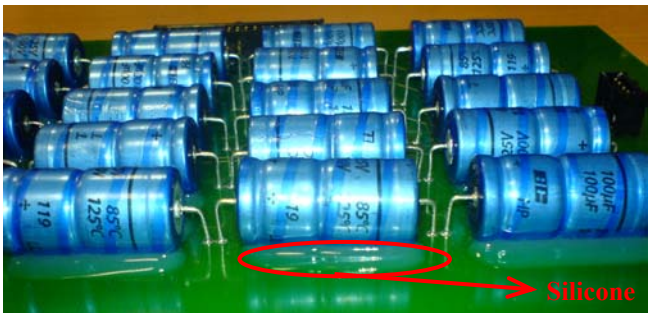


Figure 5.49: Adhesive (supplier: Omni Technic GmbH) bonding with silicone (OMNIVISC 1050) applied to PCB populated with axial leaded aluminum capacitor

Silicone and epoxy resin are two common methods of electronic component reinforcement techniques used in ASELSAN. However there isn't any concrete information about these techniques on the fatigue lives of the electronic components.

Therefore it is also worth seeking for the effects of silicone reinforcement on the fatigue lives of the electronic components.The testing equipments used in vibration testing of the PCB reinforced with silicone is identical to one used for the epoxy reinforced PCB (Figure 5.42). Step Stress Accelerated Life Test (SST) was done again to create failure(s). Based on the information gathered from the step stress testing of the PCB with epoxy coating, the damage accumulated in the first 4 step duration (4 hours testing) is converted to an equivalent test time which will create the same amount of damage in the 5.step. The damage accumulated at the end of the first 4 step is 1111 units. In 5.step incremental damage of 10000 units will be accumulated. Therefore in order to create 1111 units of damage in the 5.step, $(1111/10000)\times 60\,\text{min} = 6.666\,\text{min} \equiv 6\,\text{min}\,40\,\text{sec}$ extra testing is required for the 5.step. This equivalent test duration is added to the 5.step and the test was started from the 5.step.The reason for the starting level to be 5.step is such that because if it were selected as the following steps (6.step, 7.step etc.) there would be possibility of having failure in that step.However the general procedure is that at least the first step of testing is proposed to be completed without failure. Therefore 5.step test duration was 66 min 40 seconds. SST was stopped at the 43.6 min of the 9.step when the 10.failure was detected. During the test 10 failures were detected for the PCB. The failures were most of the time observed at the junction of the lead and component body (Figure 5.50a).However failure due to fatigue crack also occurred at the lead wire twist as shown in Figure 5.50b.

(a) (b)

Figure 5.50: Fatigue failures occurring at the lead wires of the axial leaded aluminum capacitor with silicone reinforcement a)-Mostly seen failure type b)-Failure at the lead wire twist

Figure 5.51 represents the test PCB at the end of the SST with the failed capacitors bonded with silicone onto printed circuit board. Table 5.15 lists the laboratory test results of the SST for the PCB's populated with Aluminum electrolytic capacitors reinforced by silicone.

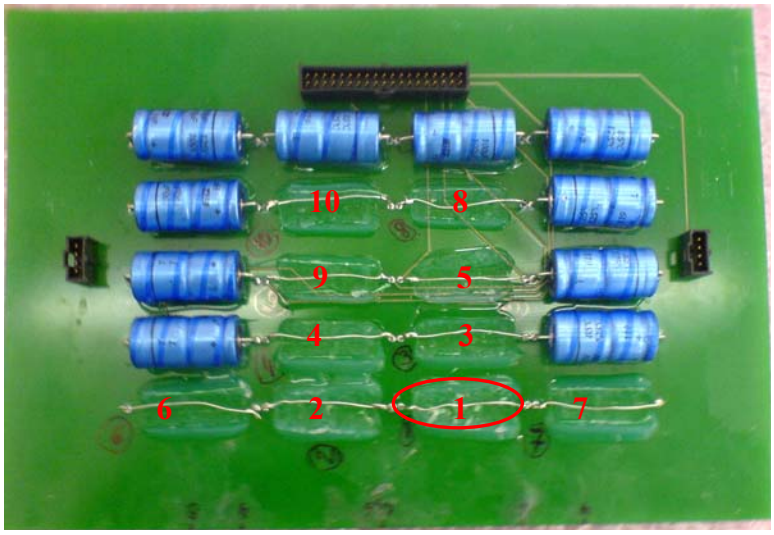
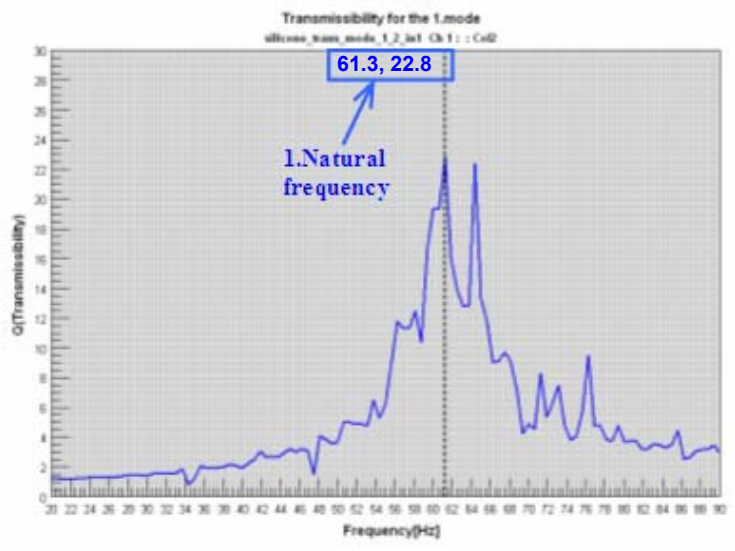


Figure 5.51: Silicone reinforced PCB populated with aluminum capacitors at the end of the SST

Table 5.15: Capacitor Failure Times in SST (Accelerated Lives)

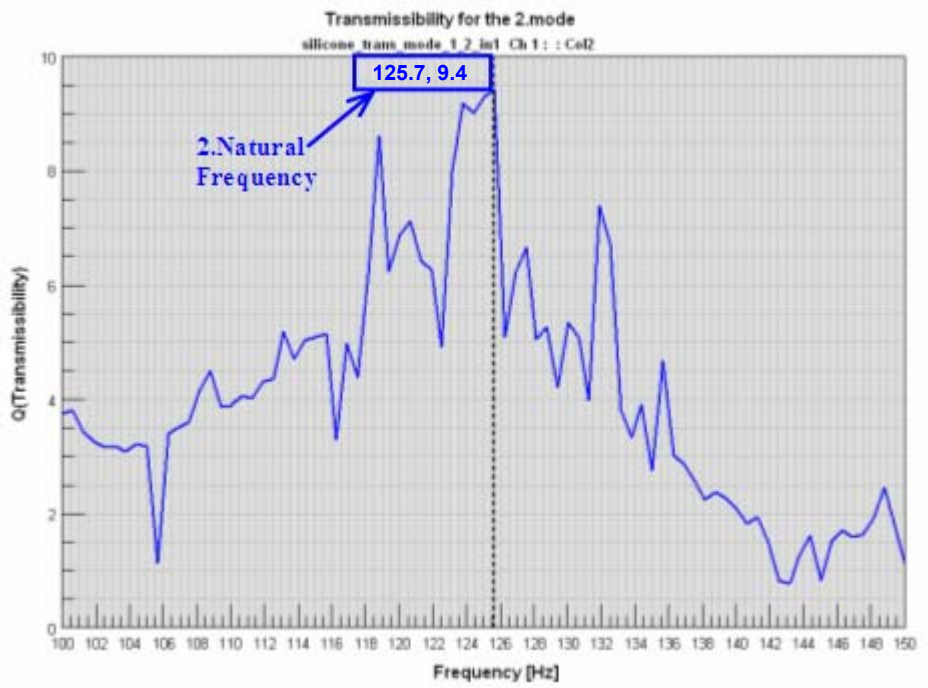
Failure Sequence	Lab. Test Failure Time[min]	Actual Failure Time[min]
1.failure	100.2	333.5
2.failure	135.6	368.9
3.failure	162	295.3
4.failure	193.2	426.5
5.failure	215.2	448.5
6.failure	237	470.3
7.failure	246.7	480
8.failure	252.9	486.3
9.failure	255.8	489.2
10.failure	289.4	522.8

These failure times are rearranged so that they represent the failure times which would occur if the SST was started from the 1.step.This re-arrangement is necessary in order to compare the failure times of the silicone reinforced capacitors with the failure times of the epoxy reinforced capacitors. Therefore these re-arranged failure times are the actual failure times of the capacitors which will be used in comparison. Any time the component is secured (epoxy or silicone) to the board, it is equivalent to "epoxied" for purposes of analysis in CirVibe (Figure 5.44) [47]. PCB properties are the same as the one listed in Figure 5.8 except the effective weight of the PCB. The effective weight of the PCB populated with epoxy reinforced Aluminum capacitors is 255.2 grams. In addition; the boundary conditions of the PCB are the same as the boundary conditions shown in Figure 5.9. The relative damage number for the 1. failed silicone reinforced aluminum electrolytic capacitor is evaluated as 66944.33 (damage at 33.5 min of the 6.step of the SST). Transmissibility plots for the 1. mode (Figure 5.52a), 2.mode (Figure 5.52b) and 3.mode (Figure 5.52c) of the PCB were obtained from the vibration data collected during SST using n-Code Glyphworks 3.0 post processing software [72].

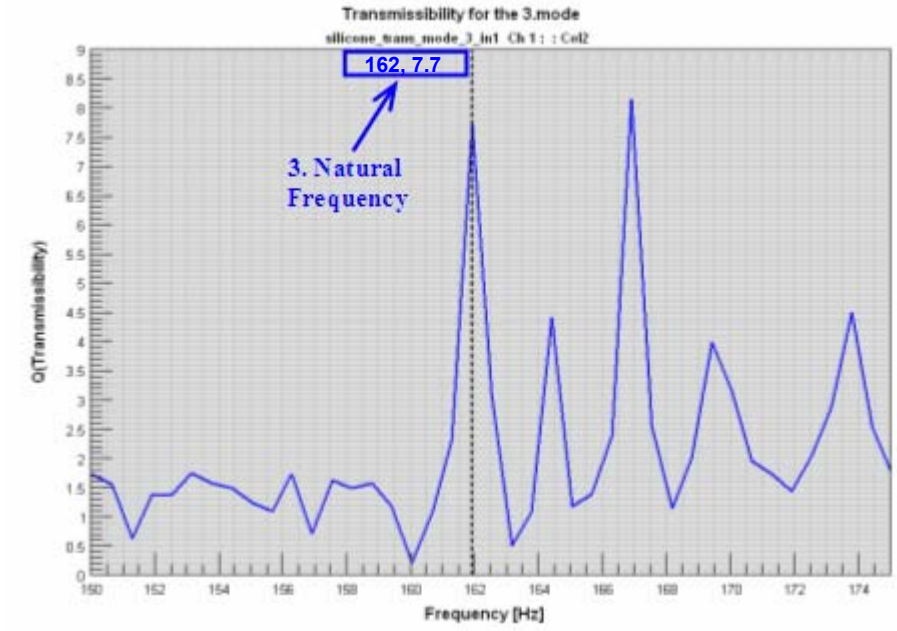


(a)

Figure 5.52: Transmissibility (Q) versus frequency (random vibration 6.1 grms white noise input freq range: 20-2000 Hz) a) - Q versus frequency plot for 1.mode at point 1,2 & 6 (61.3 Hz, Q=22.8)



(b)



(c)

Figure 5.52 (continued): Transmissibility (Q) versus frequency (random vibration 6.1 grms white noise input freq range: 20-2000 Hz) b) - Q versus frequency plot for mode 2 at point 1,2,6 (125.7 Hz, Q=9.4) c)- Q versus frequency plot for 3.mode at point 3 (162 Hz, Q=7.7)

In Table 5.16 below resonance frequencies and transmissibility's obtained from simulation and test are compared for the PCB with silicone reinforcement.

Table 5.16: Comparison of resonance frequencies and transmissibility's obtained by transmissibility tests & numerical analysis for the aluminum electrolytic capacitors with silicone coating

MODE #	NATURAL FREQUENCY [Hz]			TRANSMISSIBILITY		
	TEST	SIMULATION	%DEVIATION	TEST	SIMULATION	%DEVIATION
1.	61.3	60.3	1.6	22.8	4.8	>100
2.	125.7	137.5	9.4	9.4	12	27.9
3.	161.9	153.5	5.2	7.7	13.8	78.8
4.	190	239.7	26.1	14.8	24.3	63.7
5.	200.7	253.8	26.5	25.3	26.2	3.5
6.	265	318.1	20	19.6	35.4	80.8
7.	330	388.6	17.7	5.3	46.5	>100

Virtual accelerometers are similarly defined on the PCB at the peak response locations (Table 4.1) in CirVibe in order to enter the measured peak transmissibility's as input test data .However this time since the silicone reinforced PCB is lighter than the eccobond reinforced PCB, only accelerometer placed on the PCB are modeled as local weights.

Furthermore only first three modes of the PCB is included into the fatigue analysis since the reliability of higher mode natural frequencies is lower and contribution of the higher frequencies will be negligible.

The relative damage numbers and total accumulated damage numbers for the failed capacitors (silicone coated) on the test PCB's are listed in APPENDIX-H. Since damage is inversely proportional to the fatigue life, it can then be interpreted that the capacitor for which the accumulated damage number is found to be maximum in the analysis will fail first in the accelerated life test (SST). The simulation and test results obtained are compared in Table 5.17 below:

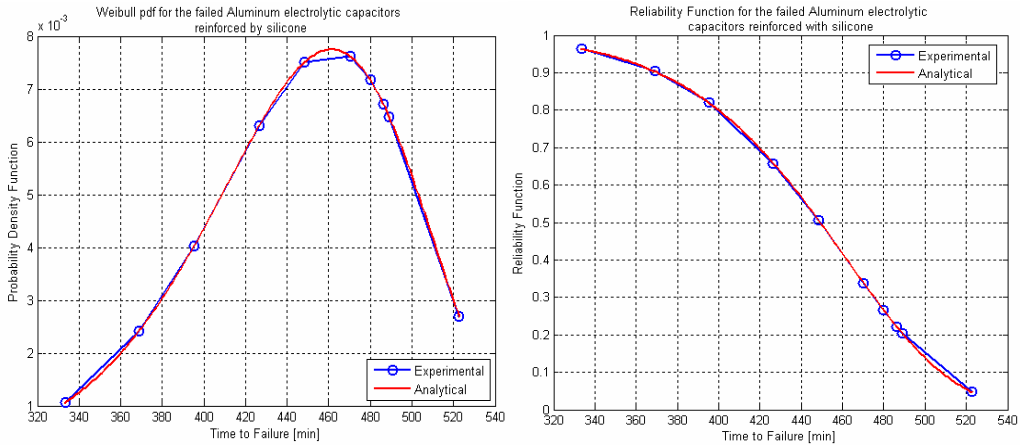
Table 5.17: Comparison of the failure rank for test and simulation results

PCB with silicone coating	
Test	**Simulation**
1.	4.
2.	**1.**
3.	8.
4.	**5.**
5.	**7.**
6.	3.
7.	2.
8.	**10.**
9.	6.
10.	**9.**

When test results and semi-experimental analysis are compared it can be seen that there exists discrepancy. However the capacitor which failed secondly in the step stress testing is found to be damaged first according to simulation results. This can be taken as a sufficient estimate because most of the time the first failed component is of interest. It should again be mentioned that the number of test circuit boards have to be increased in order to increase the accuracy level of the comparison between test and simulation.

5.12 The Weibull Model in Life Testing of Aluminum Electrolytic Capacitors reinforced with silicone

The probability density functions, reliability functions and hazard rate functions for the fatigue life (in terms of time) of the failed aluminum electrolytic capacitors are evaluated. Figure 5.53 shows the estimated probability density functions together with the reliability functions for the sample PCB respectively. Hazard rate function of the failed capacitors is also given in Figure 5.54.



(a) (b)

Figure 5.53: a) - Probability density function of the capacitors reinforced with epoxy b) - Reliability function of the capacitors reinforced with epoxy

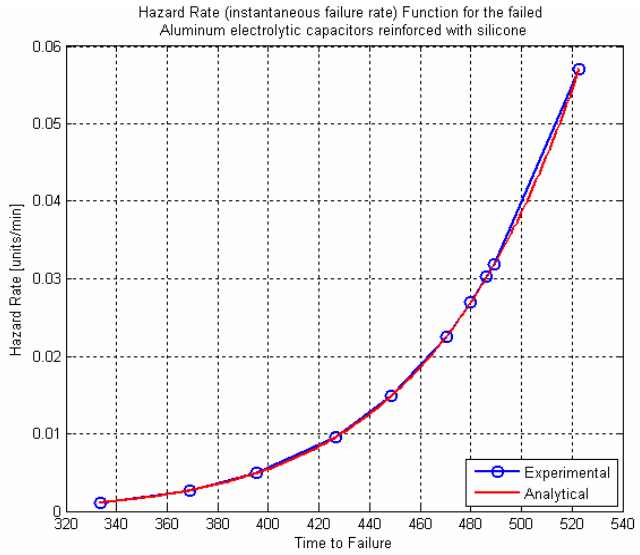


Figure 5.54: Hazard Rate Function of the capacitors reinforced with epoxy

Table 5.18 shows the maximum likelihood estimates of these parameters. Since $b_w > 1$ the failure rate is increasing with time for the capacitors

Table 5.18: Weibull parameters and MTTF for the aluminum capacitors with silicone reinforcement

Weibull Parameters	PCB with silicone
a_w**[min]**	4.6640e+02
b_w	9.77e+00
MTTF[min]	**4.432e+02**

The silicone coating under the capacitor body has a positive effect on the fatigue life. If the mean-time-to-failure of the capacitor with silicone coating and the capacitor without any reinforcement are compared it can be seen that silicone coating increases the fatigue life.

However its contribution to the fatigue life is not as significant as the eccobond. That is, MTTF for the capacitor with silicone reinforcement was determined as 443.23 min as shown in Table 5.18. Furthermore in accelerated life testing of the capacitors it was determined that the MTTF for the capacitor without any reinforcement were found to be 436.72 min and 423.71 min for the 1. test PCB and 2. test PCB respectively. Therefore it is obtained that it increased the fatigue life 4.61% for the 1.PCB and 1.49 % for the 2.PCB.

Moreover the disadvantage of the silicone coating is such that in order to remove it from the component it is necessary to cut it in slices so that the component might be damaged during this operation. Finally it should be noted that because of the large variation in conformal coating material properties, thickness applied, methods of application, etc., effect of conformal coating, in general, needs to be evaluated empirically for each application [73].

5.13 Fatigue Testing & Analysis of PCB Populated with Surface Mount Ceramic Chip Capacitors

The reliability of the solder joint attachment of electronic components surface mounted to printed circuit boards requires explicit attention in the design phase, as

well as during manufacturing. During use, surface mount (SM) solder joints can be subjected to a variety of loading conditions which can lead to premature failure. The surface mount ceramic capacitor shown in Figure 5.55 is observed to be problematic during vibration tests performed in ASELSAN and it is decided to be worth investing the potential vibration induced fatigue damage. Therefore accelerated life tests of the PCBs populated with ceramic multilayer chip capacitors were done. In addition there are two 1x4 pin type and one 2x19 type connectors used for the purpose of automatic damage detection infrastructure (for AC voltage signal feeding) which was used also for testing of Tantalum and Aluminum capacitors.

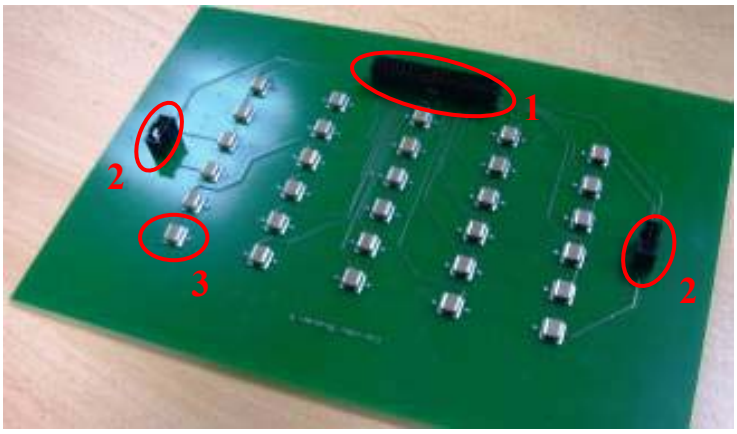


Figure 5.55: Test PCB populated with Chip Ceramic Capacitors (vendor: AVX & KYOCERA), 1: Molex Connector (2x19 pin type), 2: Molex Connector (1x4 pin type), 3: 2.2 µF Ceramic SM Capacitor

Step Stress Accelerated Life Tests (SST) of the 3 PCBs were performed. Since this type of component is very rugged for vibration, the starting level selected is likely to be large. In order to reduce the testing time, it is therefore decided to start the SST from the 12.step in which 20-2000 Hz wideband 2,740E-01 g^2/Hz (23.3grms) white noise excitation is applied to the PCB. Damage that would accumulate in the first 11 step duration (11 hours testing) is converted to an equivalent test time which will create the same amount of damage in the 12.step.

The damage accumulated at the end of the first 11 step is 1.1111E+10 units. In 12.step incremental damage of 1.00E+11 units will be accumulated. Therefore in order to create 1.1111E+10 units of damage in the 12.step, $(1.1111\times10^{10}/1\times10^{11})\times60\,\text{min} = 6.666\,\text{min} \equiv 6\,\text{min}\,40\,\text{sec}$ extra testing is required for the 12.step. Therefore 12.step test duration was 66 min 40 seconds. The shaker was capable of applying vibration up to the 13.level therefore it was planned to stop at the end of the 13.step.If there were no failure at the end of the 13.step it would be concluded that the surface mount capacitors have a fatigue life of at least 780 min in the accelerated life tests however failures were detected for all the PCBs tested therefore MTTF for the surface mount capacitors was actually found to be 725 min in the SST of the PCBs. During the accelerated life tests of the PCBs 3 failures (Figure 5.56a) were detected for the 1.PCB, 1.failure (Figure 5.56b) was detected for the 2.PCB and 6 failures (Figure 5.56c) were detected for the 3.PCB in the SST.

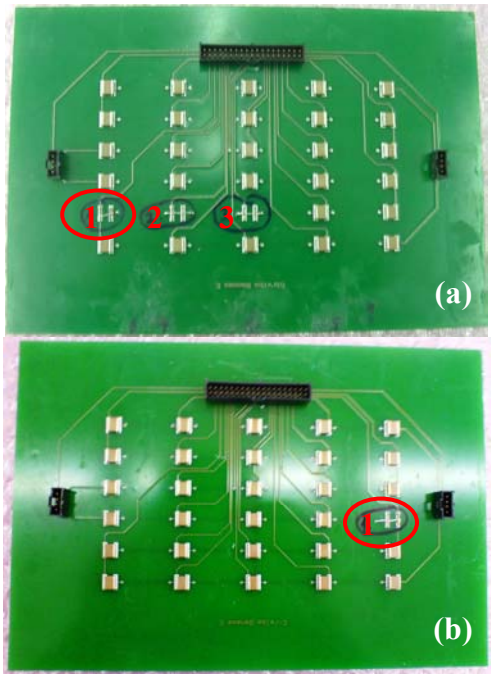
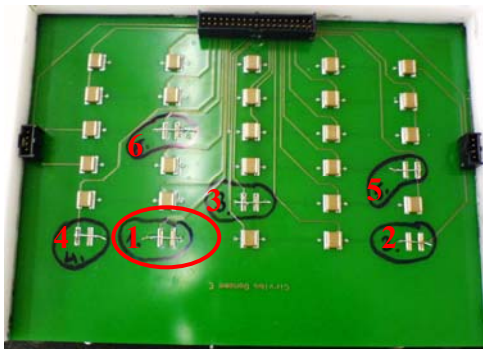


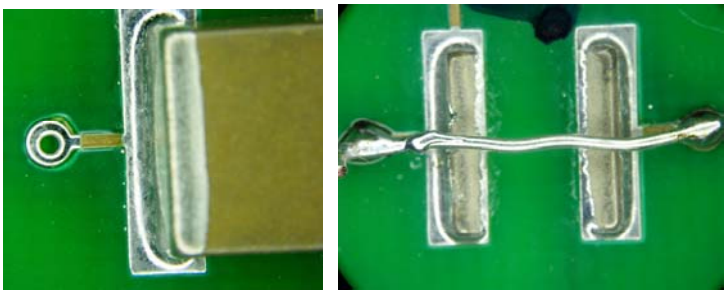
Figure 5.56: PCBs populated with SM ceramic capacitors at the end of the Step Stress Tests a) -1.Test PCB b)-2.Test PCB



(c)

Figure 5.56 (continued) :PCBs populated with SM ceramic capacitors at the end of the Step Stress Tests c)-3.Test PCB

The type of fatigue failures observed on three of the test PCBs were all similar. Due to cyclic loading fatigue crack starts and quickly propagates from end to end at the upper portion of the solder and eventually causes the SM capacitor to be skinned from the solder (Figure 5.57b).



(a) (b)

Figure 5.57: a)-Healthy solder joint b)-Failed solder joint

Table 5.19 lists the laboratory test results of the SST for the PCB's populated with surface mount ceramic capacitors. These failure times are rearranged so that they represent the fatigue lives of the capacitors which would occur if the SST was started from the 1.step.These re-arranged failure times are the actual failure times of the capacitors which will be used in comparison.

If Table 5.19 are observed it can be realized that the strength of the solder joints of the three PCB are different although the solders of the SM capacitors on the PCBs are formed by using the same vapor (Freon FC-70) phase reflow soldering process in the reflow oven.

Table 5.19: SM Capacitor Failure Times in SST (Accelerated Lives)

PCB 1		
Failure Sequence	**Lab. Test Failure Time [min]**	**Actual Failure Time [min]**
1.Failure	56.2	709.6
2.Failure	75.3	729.3
3.Failure	78.1	731.4
PCB 2		
Failure Sequence	**Lab. Test Failure Time [min]**	**Actual Failure Time [min]**
1.Failure	124	777.3
PCB 3		
Failure Sequence	**Lab. Test Failure Time [min]**	**Actual Failure Time [min]**
1.Failure	9.2	662.5
2.Failure	38.8	692.1
3.Failure	70	723.3
4.Failure	89.3	742.6
5.Failure	90.6	744
6.Failure	91.1	744.4

It was observed before the SST that the solder joints of the SM capacitors on 3 different PCBs were not all the same. Therefore this led to the different failure distribution for each PCB in the fatigue life tests. According to the engineers in Electronics Manufacturing Department, it is difficult for this SM capacitor to achieve identical quality solders because of its size. However looking at the boundary conditions of the PCB it could be commented before the SST that the first failures (first three failures) will most probably be seen at the capacitors located nearby the free edge of the PCB where larger deflection occurs compared

to capacitors at the other isolated sides of the PCB. The failure distribution of the 3 test PCB confirmed this.

PCB properties are the same as the one listed in Figure 5.8 except the effective weight of the PCB. The effective weight of the PCB populated with chip multilayer ceramic capacitors is 103.81grams. In addition; the boundary conditions of the PCB are the same as the boundary conditions shown in Figure 5.9. The relative damage numbers for the failed ceramic SM capacitors of the 3 test PCBs are shown in APPENDIX-I.

Material properties of the SM capacitor and connectors are obtained from the material database of Matweb [63] . Material and geometrical properties list of the 1x4 pin type connectors are identical to the properties listed in Figure 5.7. The overhang length and width for the 2x19 pin type connector are different than the ones for the 1X4 pin type connector.These values are 1.42 and 9.75 respectively. Figure 5.58 shows material and geometrical properties list of the SM capacitor (2.2 μF) analyzed.

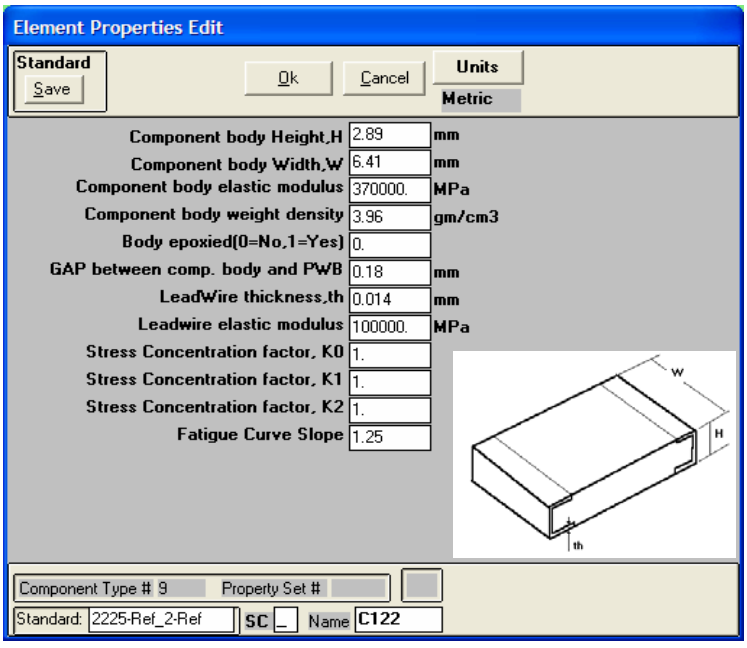
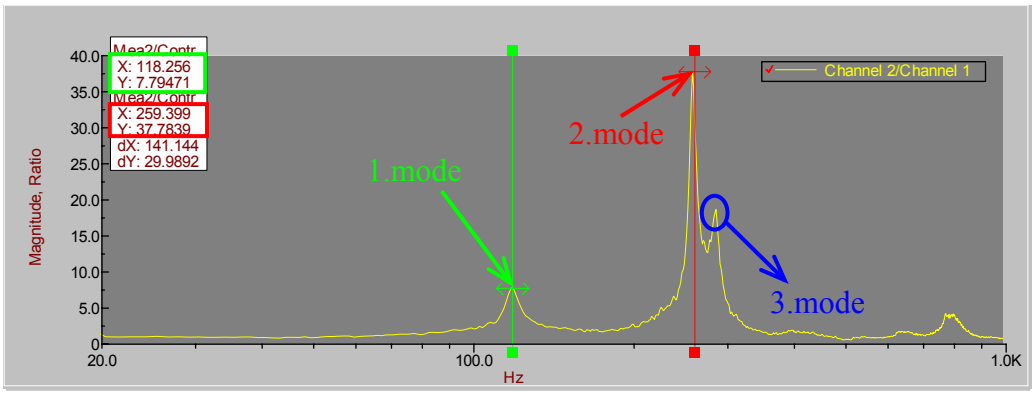


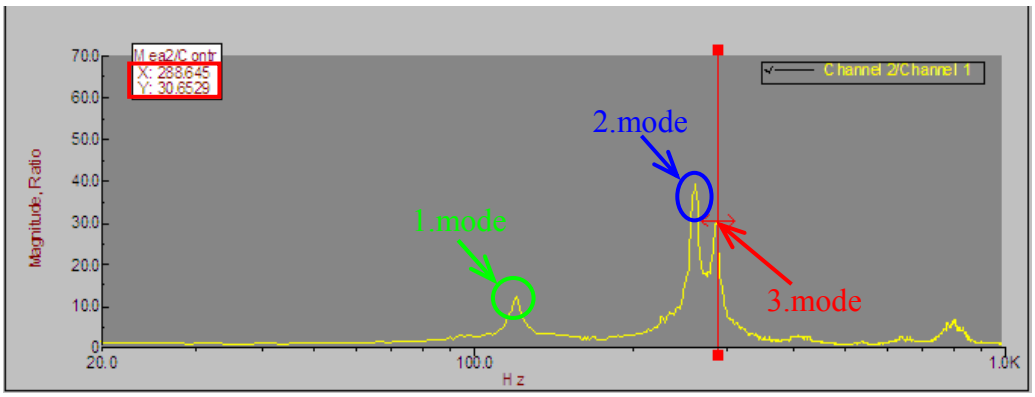
Figure 5.58: Ceramic SM Capacitor material and geometrical properties

Capacitor body (Alumina) elastic modulus and component body density are 370GPa and 3.96gr/cm^3 respectively. The lead wire (termination material) of the of the capacitor include palladium-silver alloy with average elastic modulus of 100 GPa.

In order to obtain resonance transmissibility's of the PCB populated with ceramic SM capacitor, accelerometers are placed at the peak response locations (Table 4.1) which are obtained from numerical modal analysis of the PCB in CirVibe. Figure 5.59a shows the transmissibility values for the 1. and 2.mode of the PCB. Figure 5.59b shows the transmissibility (Q) value for the 3.mode of the PCB.



(a)



(b)

Figure 5.59: Transmissibility (Q) versus frequency Q versus frequency plots a)-1. & 2.mode b)-3.mode

Virtual accelerometers are again defined at the peak response locations (Table 4.1) in CirVibe in order to input the resonance transmissibility's at these peak accelerometer locations. Miniature lightweight PCB 352A24 accelerometer [67] was used in order to record output signal. The reference signal (input) was recorded by using PCB 356A16 accelerometer on the vibration shaker under the PCB fixture. Model-based and testing results in Table 5.20 below are consistent with each other, except a poor match of transmissibility values at higher modes.Total accumulated damage numbers of the damaged SM (shown in red) and non damaged surface mount capacitors are given in APPENDIX-I.

Table 5.20: Comparison of resonance frequencies and transmissibility's obtained by transmissibility tests & numerical analysis for the ceramic surface mount capacitors

MODE #	NATURAL FREQUENCY [Hz]			TRANSMISSIBILITY		
	TEST	SIMULATION	%DEVIATION	TEST	SIMULATION	%DEVIATION
1.	118.3	122	3.2	7.8	10.5	34.2
2.	259.4	269.6	3.9	37.8	28.4	24.9
3.	288.645	306.6	6.2	30.7	33.7	9.9
4.	403.1	457	13.4	3.4	58.2	N/A
5.	545.5	582.8	6.8	1.7	81.8	N/A
6.	663.8	606.6	8.6	1.8	86.6	N/A
7.	810	728.6	10	4.7	112.3	N/A

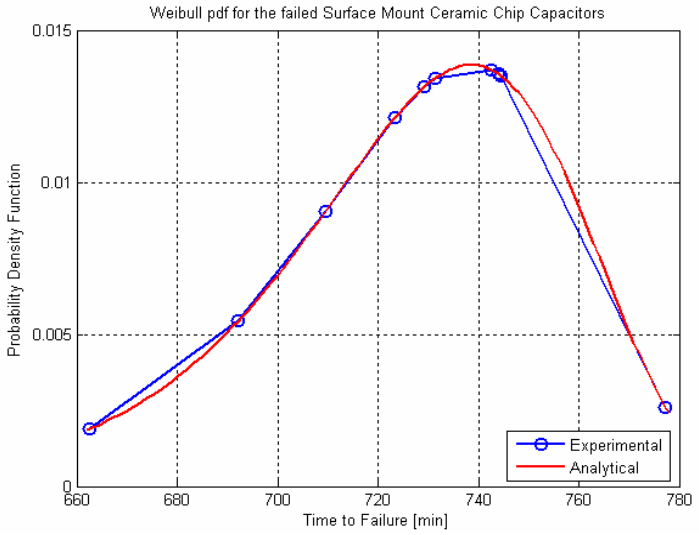
The capacitors which aren't damaged withstand to damage numbers shown in the above tables and have a fatigue life of at least 780 min since the SST can not be continued after 13.step because of the shaker capability.

5.14 The Weibull Model in Life Testing of Ceramic SM Capacitors

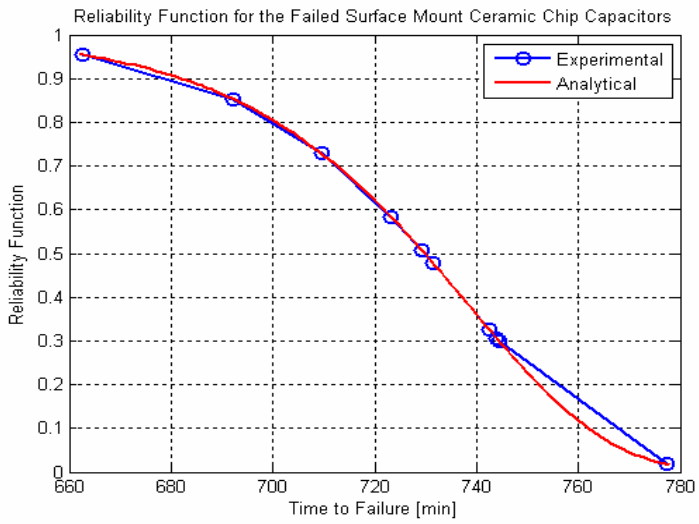
In this case since the numbers of failures observed for the components on each of the test PCBs are small the fatigue lives of the components on different PCBs are processed together when evaluating the MTTF for the SM capacitor.

This is possible since the important thing here is that failures are all observed for the same type of the component.

Figure 5.60 shows the estimated probability density functions together with the reliability functions for the sample PCB respectively. Hazard rate function of the failed capacitors is also given in Figure 5.61.



(a)



(b)

Figure 5.60: a) - Probability density function of the capacitors reinforced with epoxy b) - Reliability function of the capacitors reinforced with epoxy

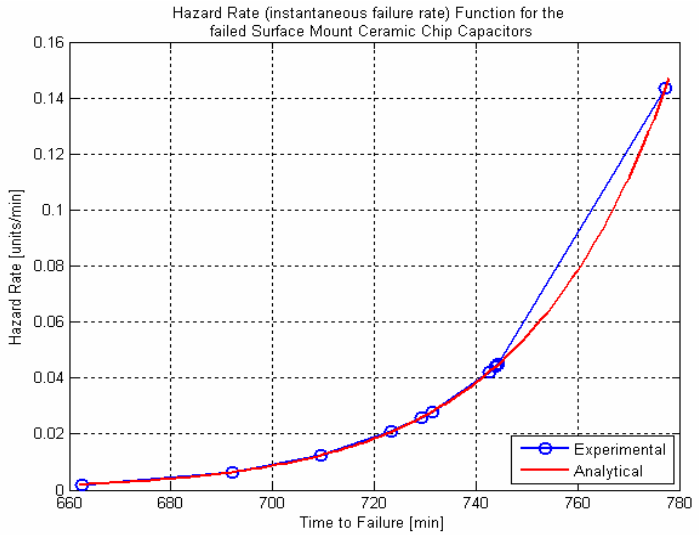


Figure 5.61: Hazard Rate Function of the capacitors reinforced with epoxy

Table 5.21 shows the maximum likelihood estimates of these parameters. Since $b_w > 1$ the failure rate is increasing with time for the capacitors. The MTTF for the SM capacitor is calculated as 725 minutes in accelerated life tests. This is expected since this type of component is very rugged for vibration as mentioned before.

Table 5.21: Weibull parameters and MTTF for the SM capacitors

Weibull Parameters	PCB with SM Ceramic Chip Capacitors
a_w[min]	7.395e+02
b_w	2.78e+01
MTTF[min]	**7.25e+02**

At this stage the accelerated fatigue life database for the four different components is obtained. The results are summed up in Table 5.22 below together with the corresponding mean damage index to failure (MDTF) values.

MDTF values correspond to the accumulated damage numbers for the MTTF of the tested components. Multiple test circuit boards populated with electronic

components must be used to gain a better statistical confidence in the accelerated fatigue life. From Table 5.22 it can be concluded that surface mount capacitors and PDIP components are more rugged than axial leaded capacitors.

Moreover designers have been trying to use SM components rather than using axial leaded components since using SM components give the designers more flexibility when designing the circuit board. SM components are smaller and occupy less space than the axial leaded components.

Table 5.22: Electronic Component Accelerated Fatigue Life Database for vibration induced cyclic stresses

Electronic Component Type	**Mean-Time-To-Failure (MTTF) [min]**	**Mean-Damage-Index-To-Failure (MDTF)**
Axial Leaded Tantalum Capacitor	263	4.592E+01
Plastic Dual-Inline Package	≥ 782.5	≥ 0.752E+04
Axial Leaded Aluminum Electrolytic Capacitor	430.4	1.4241E+05
Axial Leaded Aluminum Electrolytic Capacitor with epoxy bonding	551.4	5.033E+01
Axial Leaded Aluminum Electrolytic Capacitor with silicone bonding	443.2	3.238E-07
Surface Mount Ceramic Multilayer Chip Capacitor	725	3.109E-05

CHAPTER 6

FATIGUE ANALYSIS OF THE POWER CIRCUIT BOARD OF THE POWER DISTRIBUTION UNIT USED IN LEOPARD 1A1 BATTLE TANK

6.1 Purpose of the Study

Every design project has the task of defining the environmental capability of the new product. Therefore it is aimed in this study to compare the calculated vibration damage for the electronic components (Axial leaded Tantalum & Aluminum electrolytic capacitors) with known capabilities defined in Step Stress Tests in order to establish limits on design. For this purpose the circuit board used in the power distribution unit (Figure 6.1) of the Leopard 1 battle tank was chosen**.** It is possible to define the life usage for these components provided that the power distribution unit vibration specification (vibration input loading in the form of power spectral density) is available.

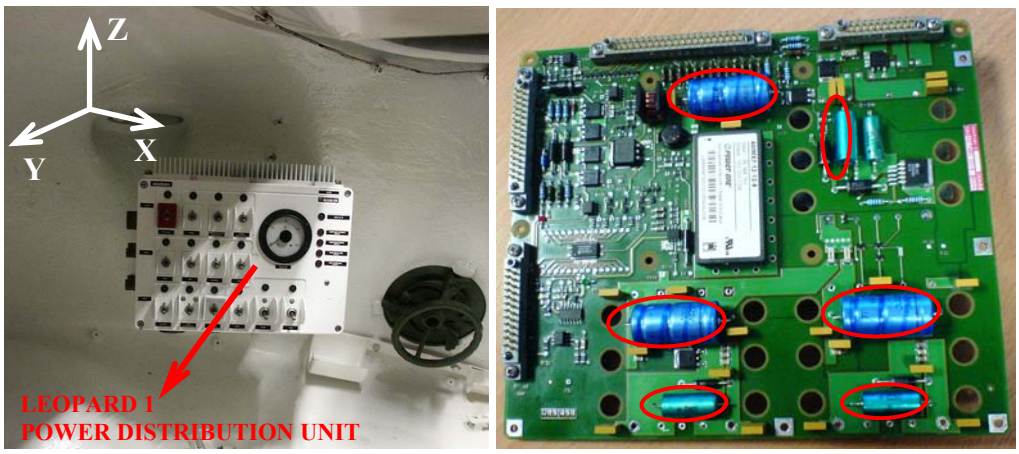


Figure 6.1: Power Distribution PCB

The power circuit board is oriented parallel to the z axis (Figure 6.1).Before going into the fatigue analysis of the power distribution PCB it is aimed first to verify the

modal frequencies obtained by CirVibe with the experimental modal analysis results. After that numerical fatigue analysis will be compared with the accelerated life test results.

6.2 Verification of the Natural Frequencies obtained by CirVibe with Modal Test

In order to verify the modal frequencies of the power PCB obtained by CirVibe experimental modal analysis using impact hammer method was used for. For this purpose one edge of the power PCB was clamped and the other edges were chosen as free (Figure 6.2).

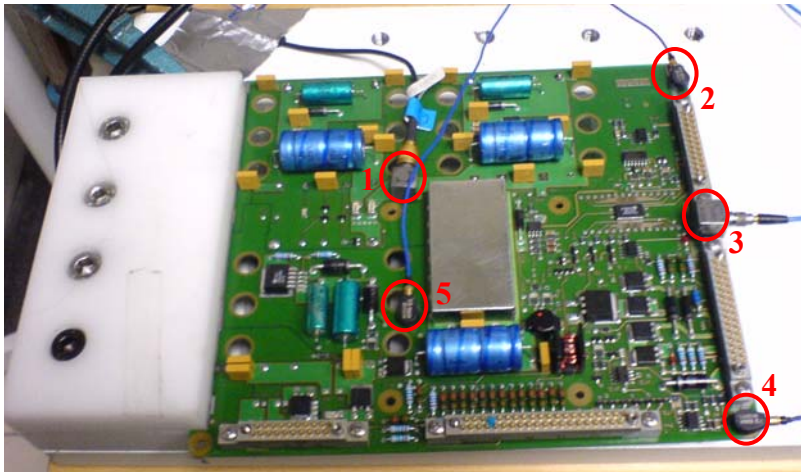
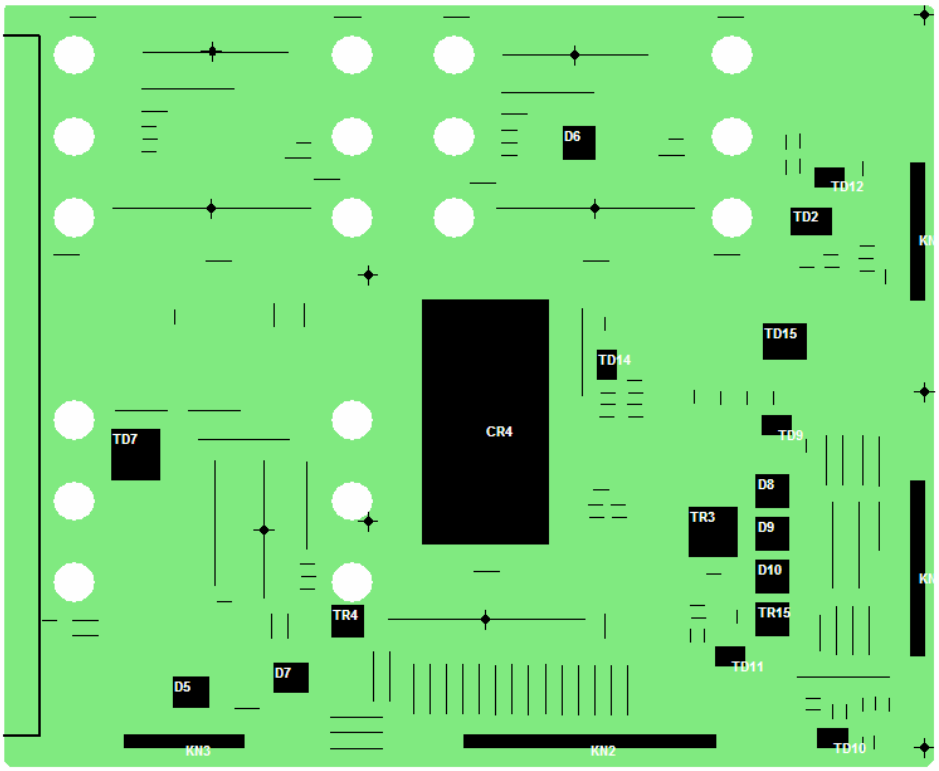
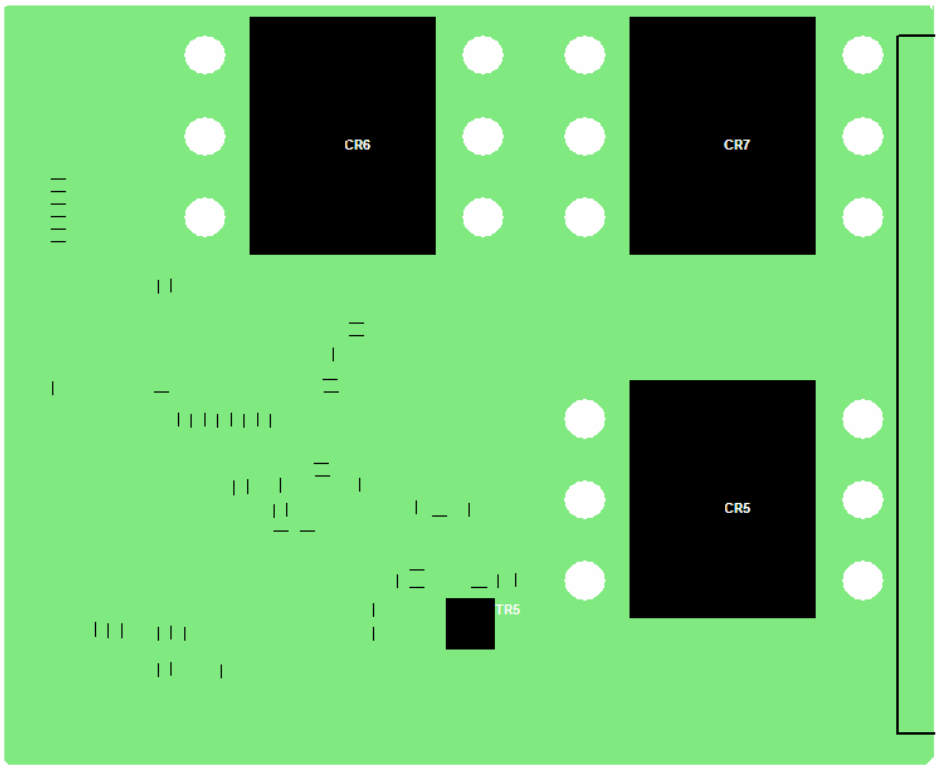


Figure 6.2: Modal Test of the Power PCB (fixed-free-free-free boundary condition)

Figure 6.3 shows the PCB model used in CirVibe. Local weights are defined for the massive components in the model. Boundary condition on the left side of the PCB where it is mounted to the fixture is modeled as cantilevered boundary by using “fixed line support” element in CirVibe.



(a)



(b)

Figure 6.3: Model of the Power PCB in CirVibe a)-Side 1 (upper side) of the PCB b)-Side 2 (lower side) of the PCB.

Comparison of finite element analysis and modal test results for the first three natural frequencies of the power PCB are done. Figure 6.4 and Figure 6.5 show the experimental and numerical analysis for the fundamental natural frequency of the power PCB respectively.Table 6.1 compares the FEA results with the results obtained by modal testing. In this analysis Least Squares Complex Exponential method in LMS Test Lab [54] was used for curve fitting.

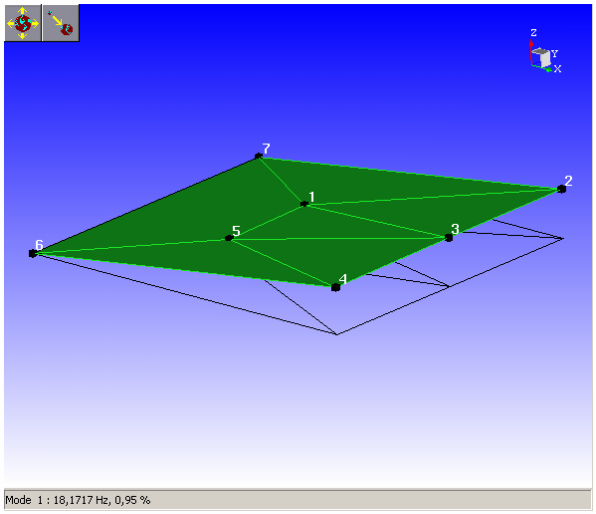


Figure 6.4: First natural frequency of the Power PCB obtained from experimental modal analysis ($f_1 = 18.2$ Hz, damping ratio, $\zeta = 0.95$ %)

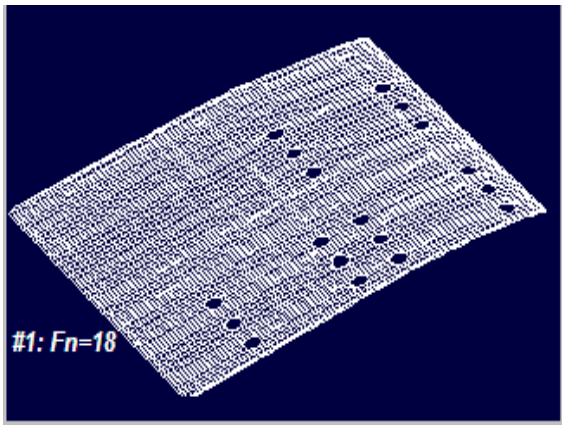


Figure 6.5: First natural frequency of the Power PCB obtained from CirVibe simulation ($f_1 = 17.5$ Hz)

Table 6.1: First three natural frequencies of Power PCB of the Power Distribution Unit

Mode	Frequency by FEA model (Hz)	Frequency by Test (Hz)	(FEA-test)/test (%)
1	17.5	18.2	-3.7
2	67.4	69.6	-3.2
3	108.8	104.3	4.4

Looking at the results summarized in Table 6.1 it can be concluded that the dynamic behaviour of the Power PCB can be represented by the model used in CirVibe. Mode shapes obtained from FEA are also consistent with the experimental modal analysis results. Therefore the circuit board model can now be used in the numerical fatigue analysis of the components.

6.3 Fatigue Analysis of the Power PCB integrated with Transmissibility and Accelerated Life Tests

In Figure 6.6 the 3-D model of the power circuit board is shown. In its operating conditions, the power PCB (Figure 6.6) is mounted to the support plate (5) using M2.5X8 screws (1) .There exists another PCB over the power PCB (4) which is also mounted to the support plate using the same 6 M2.5X8 screws together with M2.5X23 spacer screws (2).The weight of the PCB above the power PCB is supported only by the support plate but since the spacer screws are mounted to the support plate through the power PCB, these screws also build up a support boundary for the power PCB, therefore there are 12 mounting points on the upper side of the power PCB. Furthermore, the power PCB is two-sided and on the lower side there are 3 DC-DC inverters which are mounted to the support plate by 18 M3X8 screws and to the PCB from the solder joints.Therefore the power PCB is mounted to the support plate from these 18 screws also by means of inverters. This forms totally 30 mounting points which leads to a very rigid structure for vibration. Finally, the support plate is mounted to the chassis of the power distribution unit (not shown in the figure) via 6 M6X12 screws (3).

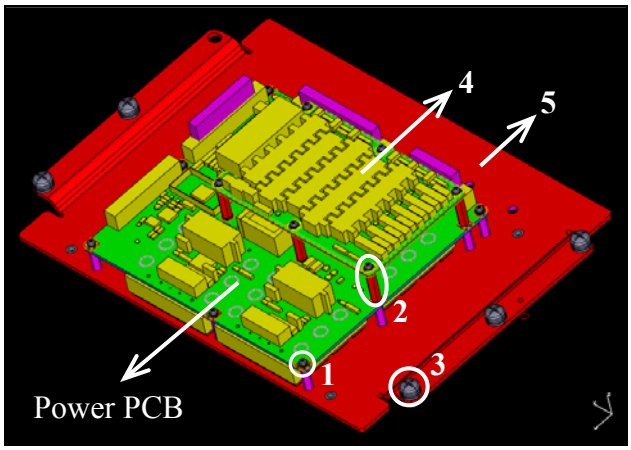


Figure 6.6: 3-D model of the Power PCB

Since in this configuration (normal operating conditions) it is difficult to obtain a failure for the mounted components, the boundary conditions of the power PCB was changed so that the numerical analysis results can be compared to test failures which could possibly be induced in the laboratory environment. Therefore the PCB located above the power PCB is dismounted and the inverters are lifted up by using spacers so that they aren't connected to the support plate anymore. Besides, the mounting points on the power PCB is reduced to 4 points shown in Figure 6.7.

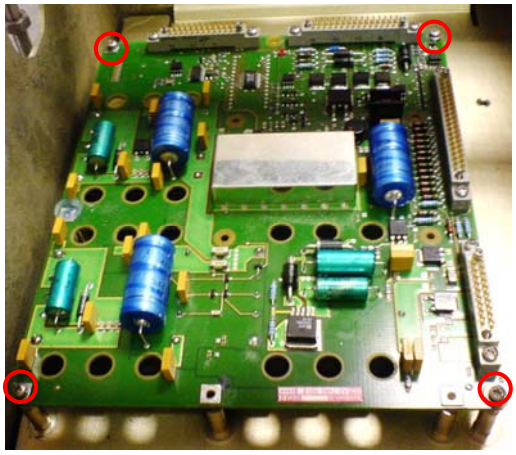


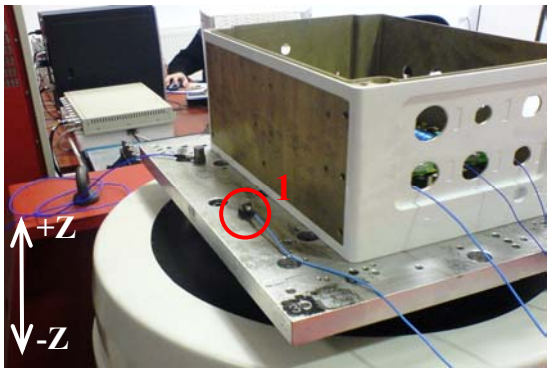
Figure 6.7: Boundary conditions of the power PCB used in the laboratory tests

6.3.1 Resonance Transmissibility Search Test of the PCB

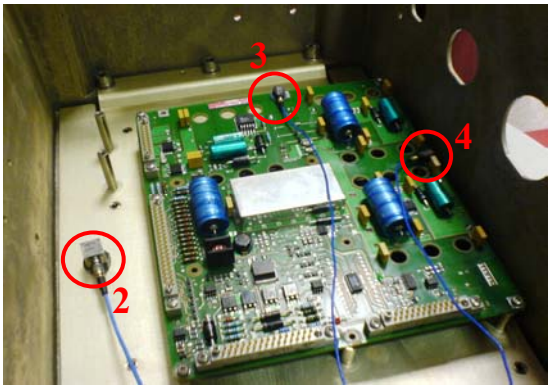
In order to obtain the transmissibility's at resonance frequencies miniature lightweight accelerometers are placed on the PCB where the displacement response is maximum.4 accelerometers are used.

One accelerometer (1) was placed on the fixture mounted to the shaker table. Another accelerometer (2) was mounted on the support plate and the other 2 accelerometers (accelerometer 3 & 4) were placed on the PCB (Figure 6.8).

In Figure 6.9 red identifiers represent the standoff supports at the edges and blue identifiers represent the miniature accelerometers placed on the PCB used to input the test data into the simulation.



(a)



(b)

Figure 6.8: Accelerometer positions used in the transmissibility test a)- fixture b)- PCB

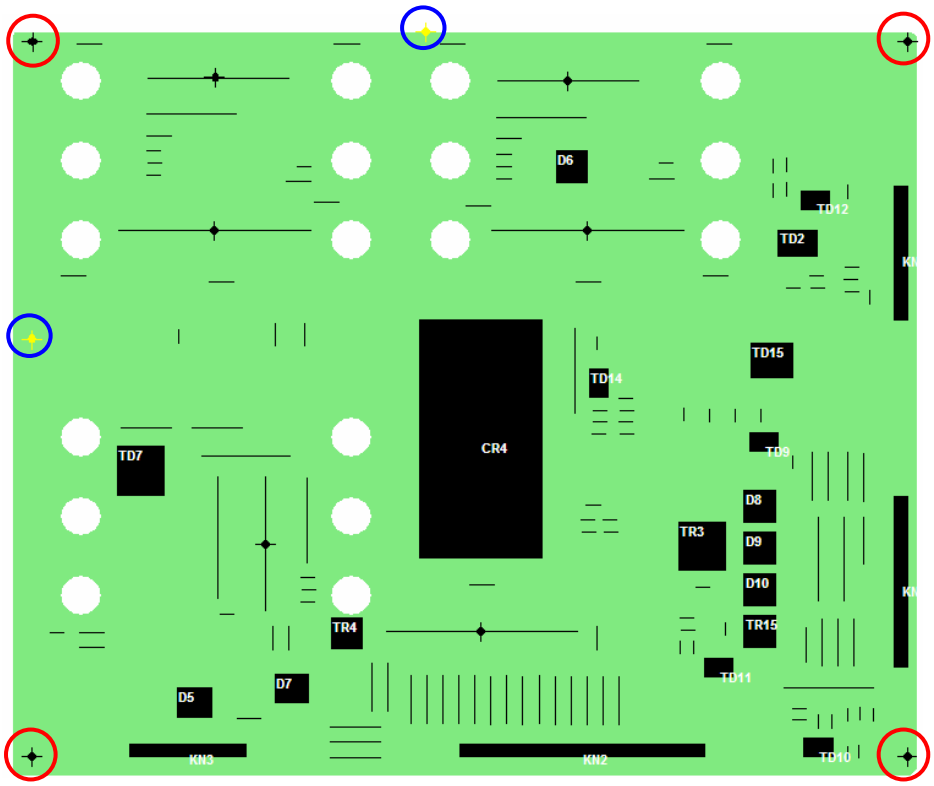


Figure 6.9: Simulation model of the Power PCB used in CirVibe for the transmissibility and accelerated life (minimum integrity tests)

The resonance transmissibility for the first three modes are obtained from the transmissibility test because for the higher frequencies displacements and the resulting stresses will be small so that the damage contribution will be small for the higher modes. Besides, for the higher modes it is rather very difficult to obtain reliable resonance frequency and transmissibility results since the higher mode shapes will be much more complex.Transmissibility together with the resonance frequency obtained from the test for the 1.mode of the power PCB of the Power Distribution unit is represented in Figure 6.10. Figure 6.11 represents the mode shape plot for the 1.mode of the Power PCB. Figure 6.12 demonstrates the resonance frequency obtained from the test for the 2.mode of the power PCB together with the resonance transmissibility. Figure 6.13 represents the mode shape for the 2.mode of the Power PCB.

Figure 6.14 demonstrates the resonance frequency obtained from the test for the 3.mode of the power PCB together with the resonance transmissibility**.** Figure 6.15 represents the mode shape for the 3.mode of the Power PCB.

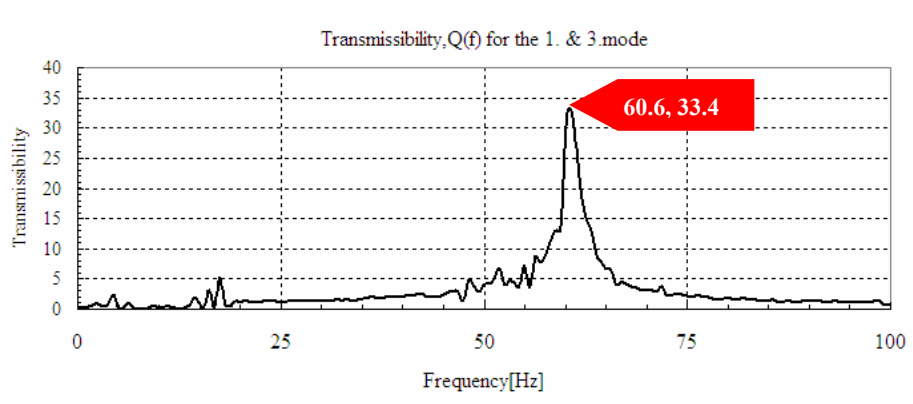


Figure 6.10: Expected 1.mode resonance frequency, $f_1 = 60.6\,\text{Hz}$ & transmissibility, $Q_1 = 33.4$

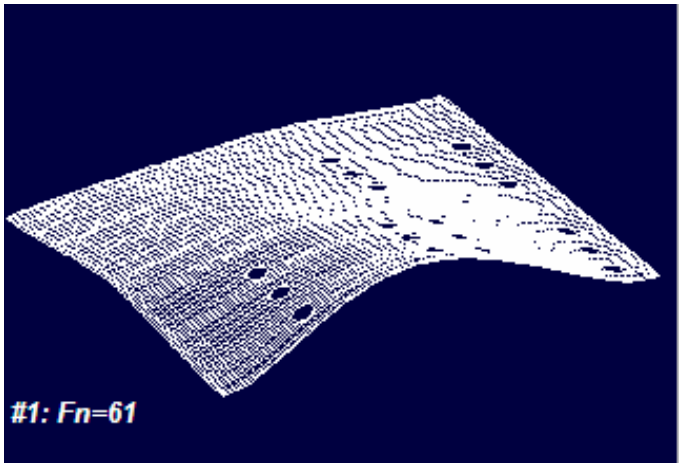


Figure 6.11: 1.mode shape and resonance frequency obtained in CirVibe $f_1 = 61.2\,\text{Hz}$

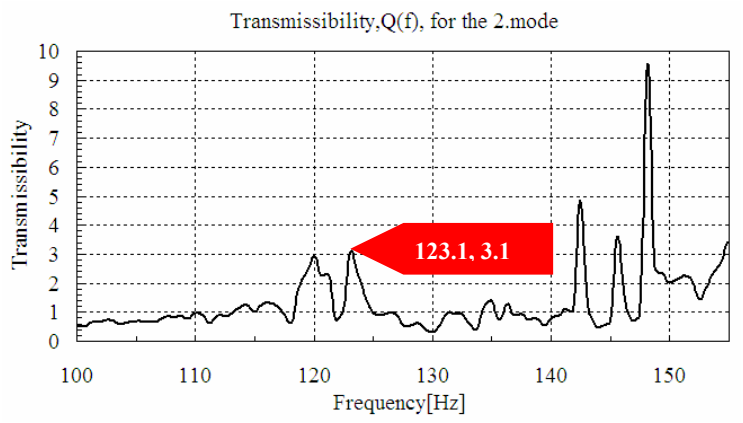


Figure 6.12: Expected 2.mode resonance frequency, $f_2 = 123.1\,\text{Hz}$ & transmissibility, $Q_2 = 3.1$

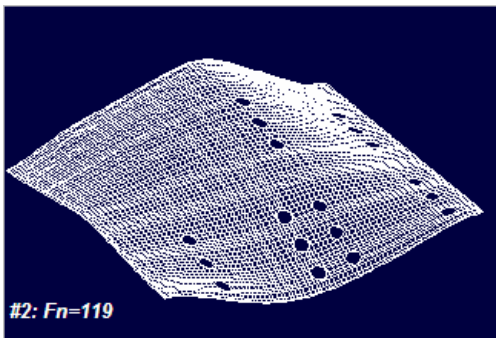


Figure 6.13: 2.mode shape and resonance frequency obtained in CirVibe $f_2 = 118.6\,\text{Hz}$

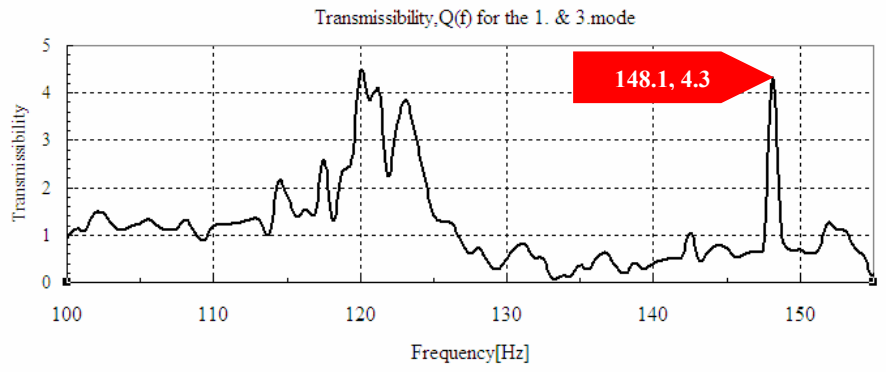


Figure 6.14: Expected 3.mode resonance frequency, $f_3 = 148.1\,\text{Hz}$ & transmissibility, $Q_1 = 4.3$

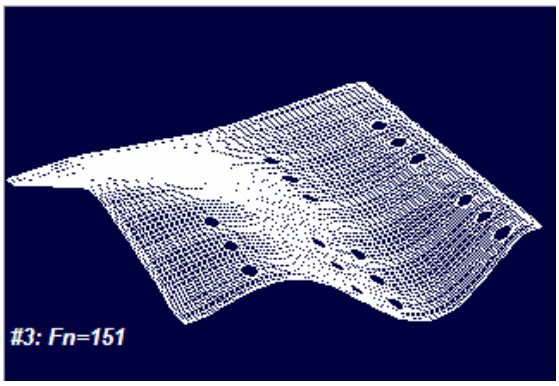
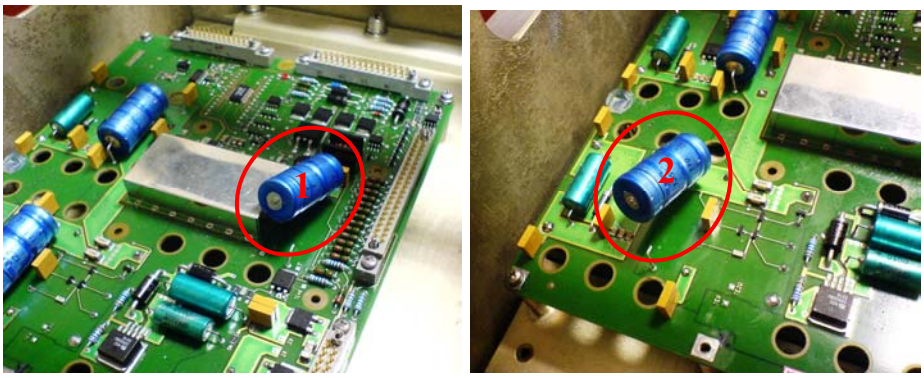


Figure 6.15: 3.mode shape and resonance frequency obtained in CirVibe $f_3 = 150.5\,\text{Hz}$

6.3.2 Accelerated Life Test of the Power PCB

After the transmissibility test of the power PCB, accelerated life testing of the PCB was performed in order to justify the failure-potential components expostulated by CirVibe fatigue analysis results. The minimum integrity test [74] (endurance test) vibration profile (broadband (20-2000 Hz) random vibration profile (7.69 G_{rms}) was used in the laboratory test. This vibration profile was selected in order to expose failures in a reasonable testing time so that the simulation results and test results can be compared. Minimum integrity test (endurance test) vibration profile was also defined in CirVibe and applied as a vibration loading applied normal to the plane of the PCB. Modal Analysis, Component Stress Analysis and Fatigue Analysis were performed for the power PCB**.** The fatigue analysis results for the components mounted on the power PCB is given in APPENDIX-J. Duration of the minimum integrity test is 60 minutes.

First capacitor failure (capacitor C-103) occurred at 32 minutes 52 seconds (32.9 min) of the test. Second capacitor failure (capacitor C-102) was observed after 38 minutes 44 seconds (38.7 min).There wasn't any more component failure after the capacitor C-102 had failed. Figure 6.16 represents the failures observed at capacitors C-103 & C-102.



(a) (b)

Figure 6.16: Failure of the Aluminum electrolytic capacitors during Minimum Integrity Tests a)- 1.fatigue failure at capacitor C-103 b)- 2.fatigue failure at capacitor C-102

Fatigue failure of structural systems has wide variations in life capabilities because there are orders of magnitude differences in rates of life usage that a component might experience depending on its location. Therefore it is important to compare the calculated fatigue damage to defined life limits (obtained by SST) in order to determine which components, if necessary, must be moved to positions of lower damage. Moreover, numerical values of component capability can be used across design configurations. Therefore the accumulated damage numbers obtained from SST for the Aluminum electrolytic capacitors will be used in the life usage calculations. Life usage of the components with known capabilities can be given by;

$$Total \quad Life \quad Usage = \left(Accumulated \quad Damage / Component \quad Capability \right) \qquad (6.1)$$

The lower limit of the failures within a component type can be defined as the component type life limit or component capability. Based on the results represented in Table G.2, Table G.3 and life usage distribution for the failed capacitors C-103 and C-102 are given below in Table 6.2 and Table 6.3 respectively.

Table 6.2: Life Usage for the failed capacitor C-103

CAPACITOR C-103 ON THE POWER PCB (**ACCUMULATED DAMAGE=1.626E+01**)			
TEST PCB	COMPONENT NAME	COMPONENT CAPABILITY	LIFE USAGE (%)
1	C113	3.9572E+05	0.004
2	C133	3.0458E+05	0.005
2	C132	2.9380E+05	0.006
1	C134	2.5608E+05	0.006
1	C123	2.3450E+05	0.007
2	C134	1.6351E+05	0.010
2	C123	1.5125E+05	0.011
1	C126	1.4575E+05	0.011
2	C114	9.0652E+04	0.018
2	C122	8.7418E+04	0.019
1	C105	5.9315E+04	0.027
1	C122	4.7993E+04	0.034
1	C132	3.0270E+04	0.054
2	C131	2.4802E+04	0.066
1	C131	6.8751E+03	0.237
2	C126	1.6129E+03	1.008
1	C112	5.0171E+02	3.241
1	C102	4.6107E+02	3.527
2	C101	1.9107E+02	8.510
2	**C111**	**6.7745E+00**	**240.018**

Table 6.3: Life Usage distribution for the failed capacitor C-102

CAPACITOR C-102 ON THE POWER PCB (**ACCUMULATED DAMAGE=1.7770E+02**)			
TEST PCB	COMPONENT NAME	COMPONENT CAPABILITY	LIFE USAGE (%)
1	C113	3.9572E+05	0.045
2	C133	3.0458E+05	0.058
2	C132	2.9380E+05	0.060
1	C134	2.5608E+05	0.069
1	C123	2.3450E+05	0.076
2	C134	1.6351E+05	0.109
2	C123	1.5125E+05	0.117
1	C126	1.4575E+05	0.122
2	C114	9.0652E+04	0.196
2	C122	8.7418E+04	0.203
1	C105	5.9315E+04	0.300
1	C122	4.7993E+04	0.370

Table 6.3 (continued): Life Usage distribution for the failed capacitor C-102

CAPACITOR C-102 ON THE POWER PCB(**ACCUMULATED DAMAGE=1.7770E+02**)			
TEST PCB	COMPONENT NAME	COMPONENT CAPABILITY	LIFE USAGE (%)
2	C131	2.4802E+04	0.716
1	C131	6.8751E+03	2.585
2	C126	1.6129E+03	11.017
1	C112	5.0171E+02	35.419
1	C102	4.6107E+02	38.541
2	**C101**	**1.9107E+02**	**93.003**
2	**C111**	**6.7745E+00**	**2623.072**

In order to have failure, accumulated damage should be at least equal to the component capability. It can be observed that accumulated damage numbers (1.62E+01 for C-103 & 1.777E+02 for C-102) obtained by the application of the minimum integrity test are higher than the lower limits obtained by SST , that is, the total life usage is greater than 100 % which confirms the minimum integrity test results.That is, in the minimum integrity test, failures were observed for the capacitors C-103 & C-102 like the simulation results indicate.

In Table 6.3 life usage of 93 % (0.93) is also highlighted because according to Palmgren-Miner cumulative fatigue damage theory, failure is assumed to occur usually when the summation of damage fraction lies in the $0.7-2.2$ range [32] therefore this life usage value also indicates a possible failure.

Another viewpoint is that the fatigue life of the capacitors can be given in terms of time. Table 6.4 compares the life times observed in the tests and derived from the simulations (semi-experimental approach).

Table 6.4: Fatigue Life comparison of the failed capacitors in Minimum Integrity Test normalized to lower limit of the capacitor

Failed Component	Experimental [min]	Simulation (Semi-experimental) [min]
C-103	32.9	13.7
***C-102**	38.7	*1.5
****C-102**	38.7	**41.6

*: with respect to minimum component capability (6.7745E+00)
**: with respect to component capability corresponding to 93% life usage (1.9107E+02)

The results indicate that simulation results are more conservative than the test results except for case of the capacitor **C-102. However due to the nature of the fatigue phenomenon, in these tests,it can be observed that the actual life-time (test failure time) is likely to be in a range of values of the order $0.3T_{life}$ to $3T_{life}$ where T_{life} is the value obtained from the simulation results [75].

The life usage of the capacitors C-104, C-63, C-64 and C-65 are also represented in APPENDIX-J.

According to the simulation results it was obtained that the probability of failure in the minimum integrity test for the capacitor C-104 is 10%. Simultaneously, capacitor C-104 did not fail in the vibration test (minimum integrity test) so this shows that the life capability for this capacitor is greater than the accumulated damage in minimum integrity test for this capacitor. Similarly,according to the simulation results the probability of failure for the capacitor C-65 is 31.034 %.The capacitor C-65 did not fail in the minimum integrity test as capacitor C-104 so this shows again that the life capability for this capacitor is also greater than the accumulated damage.

The capacitors C-63 & C-64 should fail according to the simulation results however they did not fail in the test.

This is most probably related to the number of capacitors tested to failure in the step stress tests for this component type.In this study, for this capacitor 3 PCB were tested and 29 capacitor failures were detected. So the greater the number of failures the broader will be the fatigue life distribution. Hence if some more PCBs were tested then it could be possible to obtain more precise results..

CHAPTER 7

SENSITIVITY STUDY FOR SOME OF THE PARAMETERS AFFECTING THE ELECTRONIC COMPONENT FATIGUE LIFE

In order to understand certain parameters affecting the fatigue life of the electronic components sensitivity (parametric) analysis should be performed. Figure 7.1 represents the general overview of the parameters which have direct effect on the fatigue lives of the electronic components mounted on the PCBs.

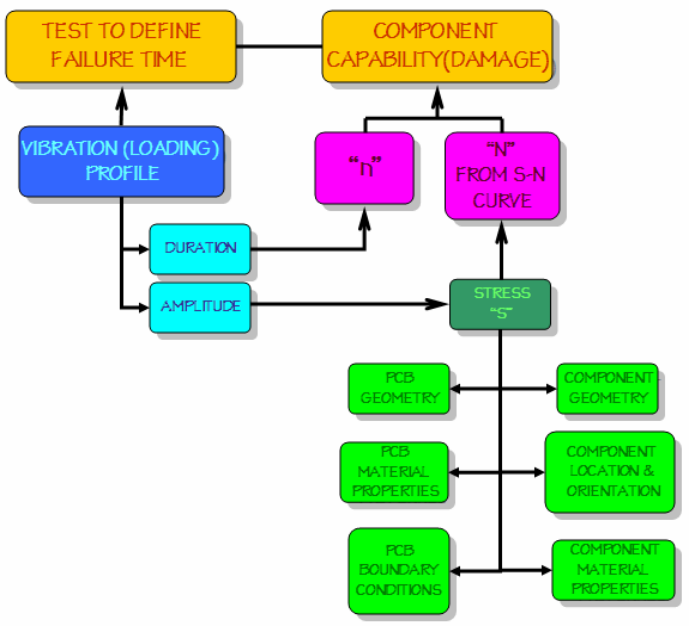


Figure 7.1: Diagram showing the factors influencing the component life capability

In Figure 7.1 “n” stands for the applied number of stress cycles and “N” is the number of cycles to failure at the stress level “S” in the S-N curve.

In this chapter, some of the parameters which are represented in Figure 7.1 affecting the component fatigue life will be investigated separately for axial leaded capacitor [76].

7.1 Sensitivity with respect to PCB Geometry

In order to obtain the effect of PCB geometry on the fatigue life, width and length of the PCB were changed. The variation of damage with respect to width and length of the PCB alone are given successively in Figure 7.2 and Figure 7.3 below. Moreover Figure 7.4 is shown in which the variation of damage is plotted with respect to PCB geometry when width & length of the PCB both changing.

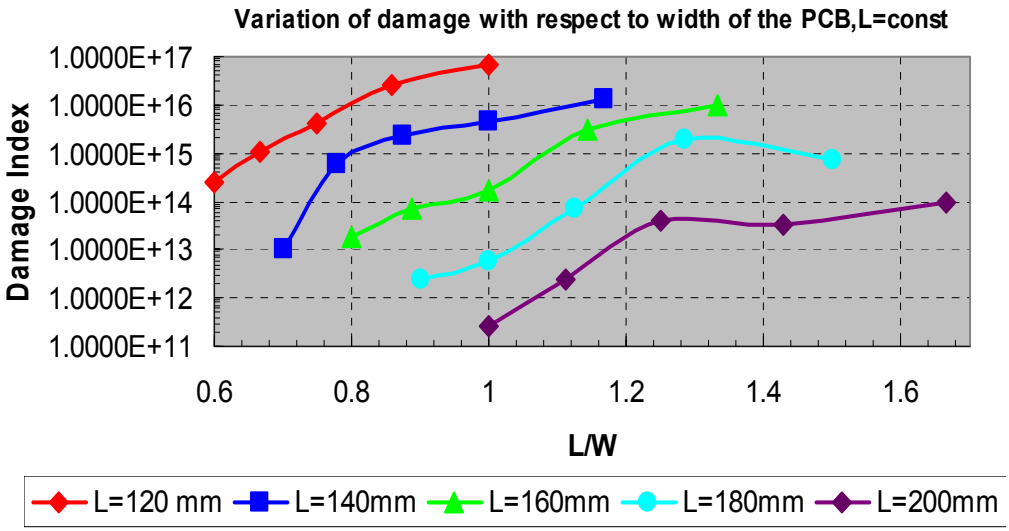


Figure 7.2: Variation of damage with respect to width of the PCB while length of the PCB is constant

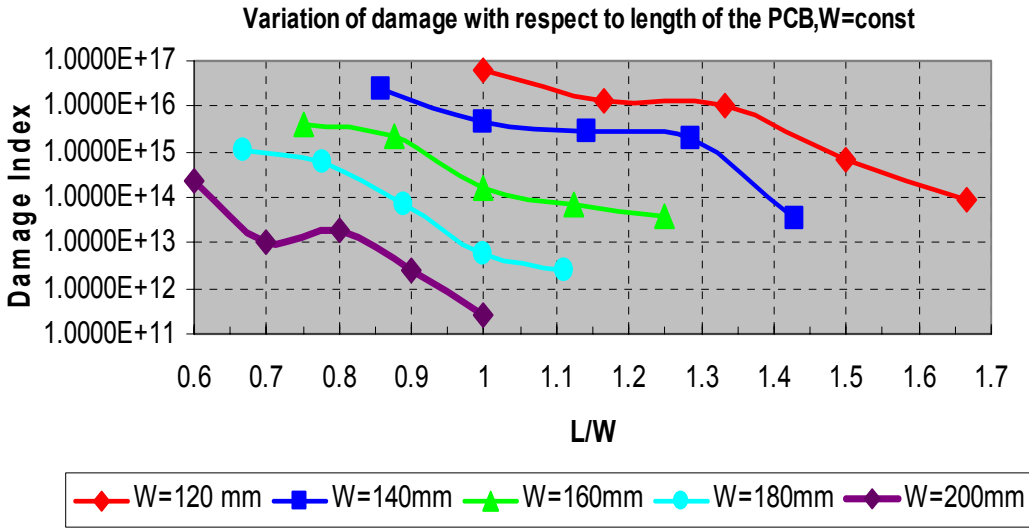


Figure 7.3: Variation of damage with respect to length of the PCB while width of the PCB is constant

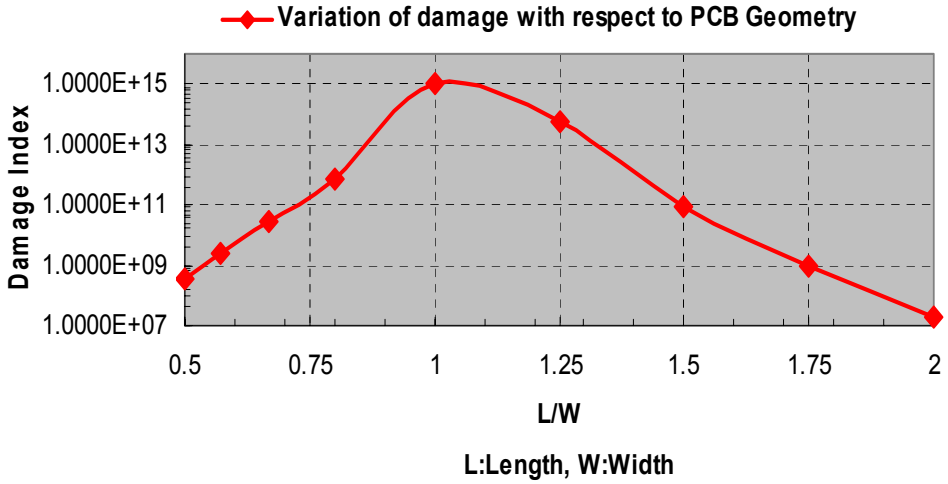


Figure 7.4: Variation of damage with respect to PCB geometry when width & length of the PCB both changing

According to the simulation results the conclusions are listed as follows:

1. When L=constant increasing L/W increases damage for the component.
2. Damage values are highest for the case where L is constant and has the smallest value (L=120mm case).

3. When W=constant increasing L/W decreases damage for the component.
4. Damage values are smallest for the case where W is constant and has the highest value (W=200mm case).
5. Based on the conclusion 1 & conclusion 3 it can be commented that fatigue damage will be maximum when $L = W$ and decreases for the cases where $L/W \neq 1$ (Figure 7.4).

7.2 Sensitivity with respect to PCB Young Modulus

In order to obtain the effect of PCB material properties on the fatigue life, first of all PCB modulus of elasticity in x and y direction were changed. E_x is the young modulus in x (lengthwise) direction E_y is the young modulus in y (crosswise) direction.

The variation of damage with respect to E_x and E_y of the PCB alone are given successively in Figure 7.5 and Figure 7.6 below.

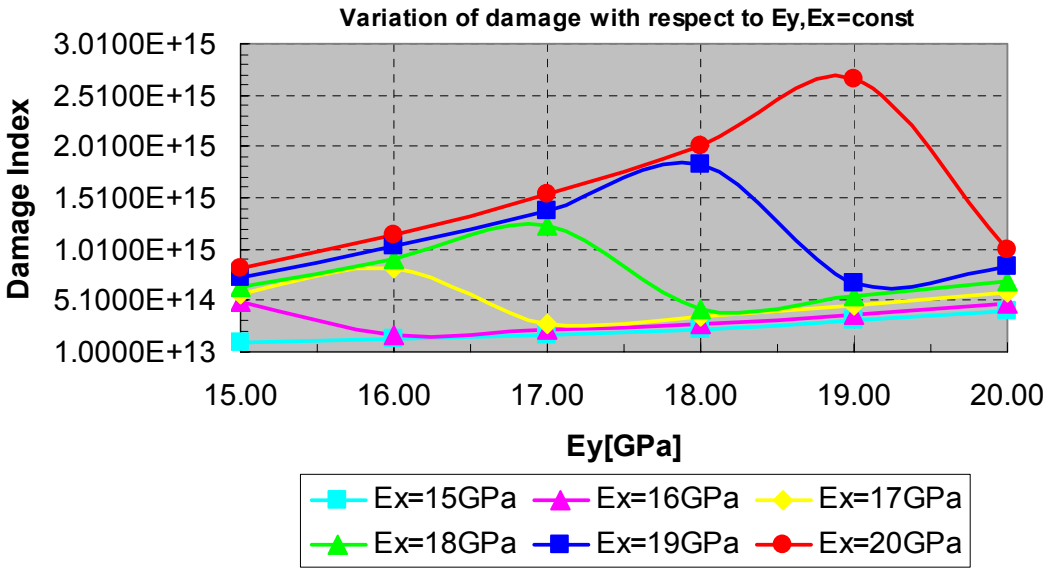


Figure 7.5: Variation of damage with respect to E_y of the PCB while E_x of the PCB is held constant

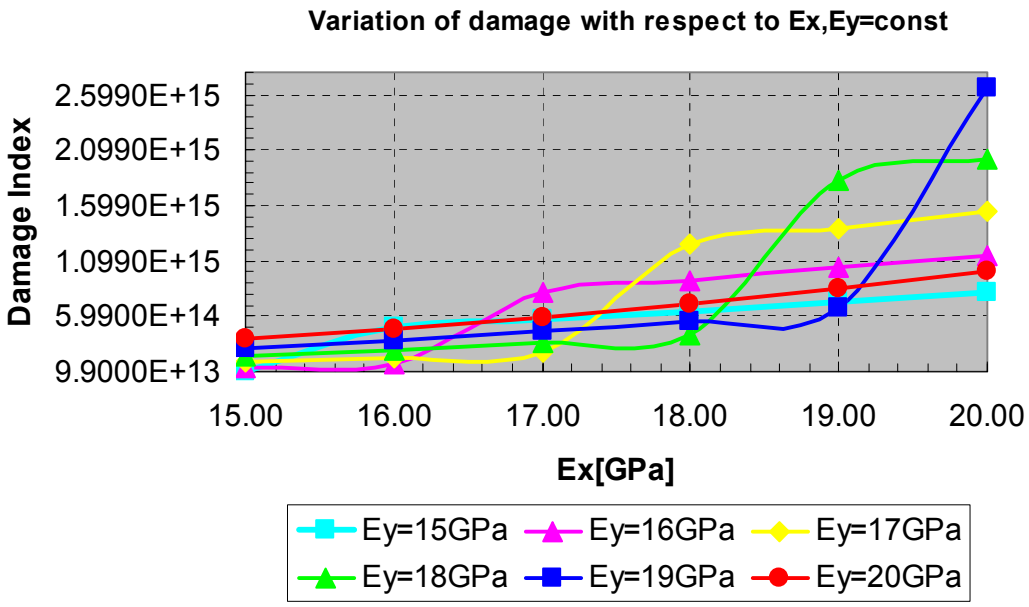


Figure 7.6: Variation of damage with respect to E_x of the PCB while E_y of the PCB is held constant

According to the simulation results the following conclusions are obtained:

1. When $E_y = E_x$ for the E_x=constant case then the fatigue damage will be smallest. Besides the fatigue damage will be maximum for the case where $E_y = (E_x - 1)$.Namely; fatigue damage will increase up to certain point then decreases and then starts to increase again with increasing E_y.
2. The fatigue damage trend is different for E_x compared to E_y.It increases with E_x.The rate of change of damage will increase considerably at the point where $E_x = E_y$.

7.3 Sensitivity with respect to Material S-N curve slope

The first investigated parameter of the component that has direct effect on the fatigue life is the material *S-N* curve slope. This slope can belong to solder material or the lead wire material. Considering the applied number of cycles, *n*, to be constant in order to have less damage, *N* should increase. In Figure 7.7 *S-N* curve for different slopes is shown.

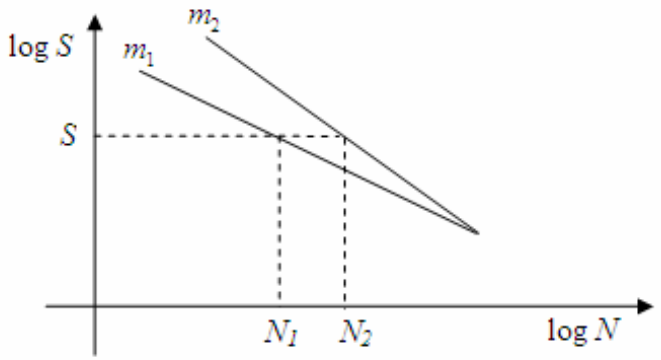


Figure 7.7: S-N curve for different fatigue curve slope

When slope increases ($m_2 > m_1$) number of cycles to failure at the stress level increases ($N_2 > N_1$) therefore fatigue damage will be less. According to Figure 7.8 fatigue damage decreases with increasing fatigue curve slope which is consistent with Figure 7.7.

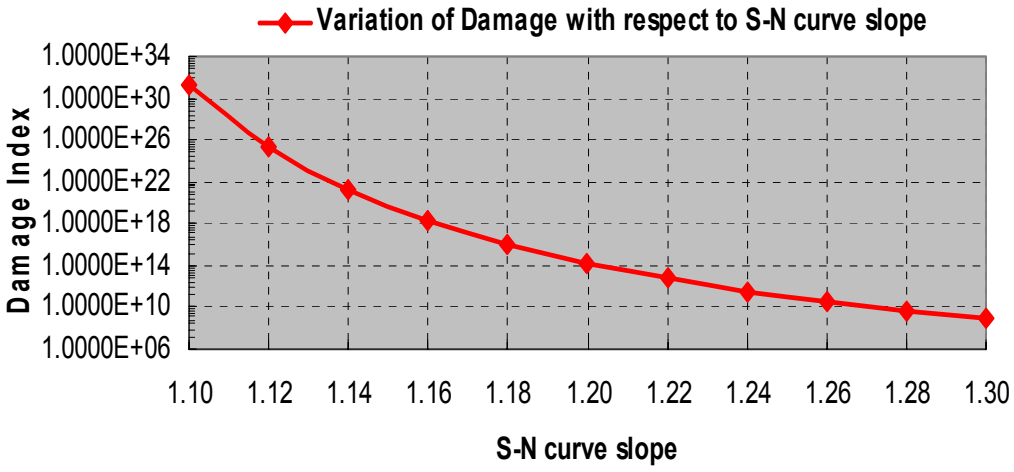


Figure 7.8: Variation of damage with respect to *S-N* curve slope

7.4 Sensitivity with respect to Component Orientation

Orientation has also direct effect on the fatigue life of the component. Figure 7.9 shows the angle θ_{cap} between horizontal and the component. In this study, this angle is varied and the change in the damage number is noted. In Figure 7.10 the variation of damage with respect to angle θ_{cap} is represented.

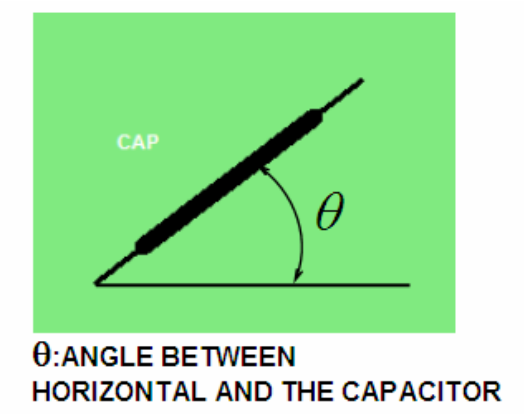


Figure 7.9: Orientation of the component

According to the simulation results the following conclusions can be obtained for the simply supported boundary conditions:

1. Fatigue damage starts to increase first, reaches maximum and then starts to decrease and reaches minimum at 45^{o}.Therefore, the optimum orientation (minimum fatigue damage) of the axial leaded capacitor on the PCB having all the edges simply supported is 45^{o} orientation
2. The fatigue damage is maximum for 30^{o} & 60^{o} orientations. In addition damage is equal for the parallel (0^{o}) and perpendicular (90^{o}) orientations
3. The variation of damage is almost symmetrical around $\theta_{cap} = 45^{o}$.
4. Although the optimum configuration is $\theta_{cap} = 45^{o}$ configuration it is rarely used for this type of component orientation. However $\theta_{cap} = 0^{o}$ or $\theta_{cap} = 90^{o}$ are more common configurations

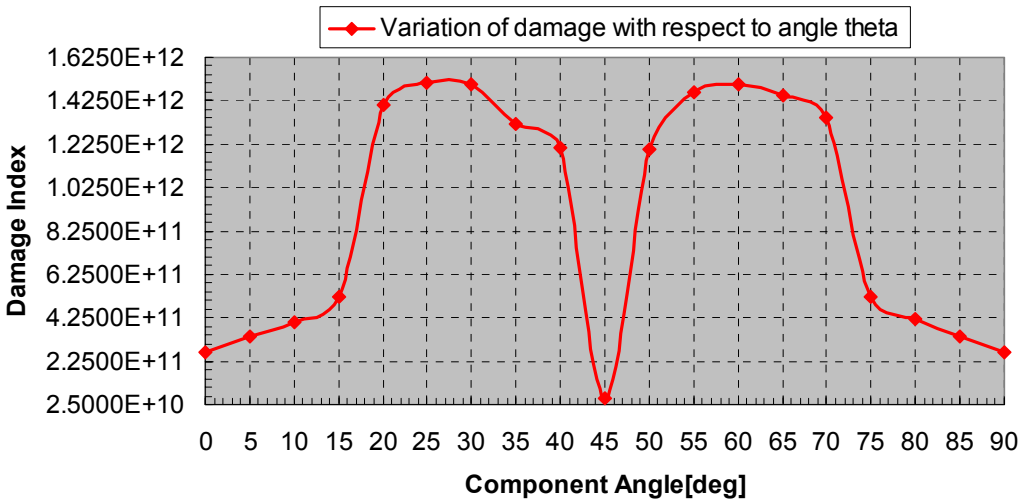


Figure 7.10: Fatigue Damage versus orientation angle θ

7.5 Sensitivity with respect to Component Lead-wire Diameter

When the lead-wire diameter increases the stiffness of the lead increases hence fatigue damage will be less. Figure 7.11 represents the variation of damage with respect to lead-wire diameter.

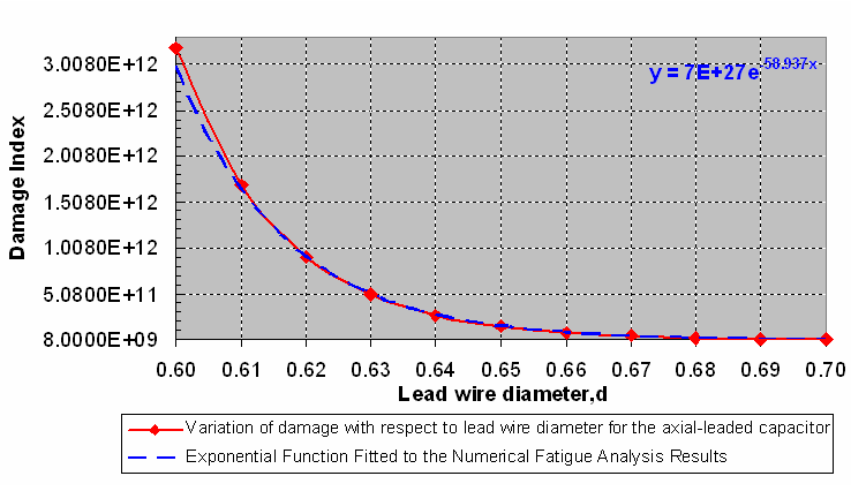
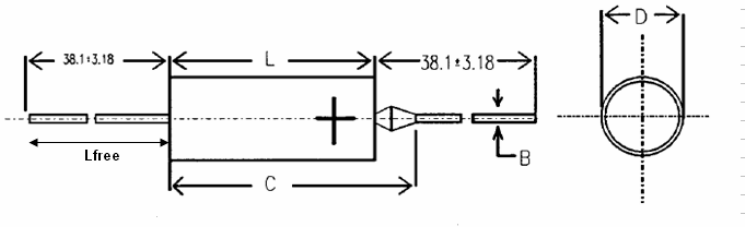


Figure 7.11: Graph representing the variation between damage and the lead-wire diameter

Exponential equation like $D = \alpha e^{\beta d_{cap}}$ can be used to find relation between lead-wire diameter and the fatigue damage. In this equation D represents the damage number and d_{cap} is the lead-wire diameter. Here it should be noted that α & β will be different for different PCB boundary condition, geometry, thickness and young modulus.

7.6 Sensitivity with respect to Component Body Length & Diameter

Component body length and diameter are another two important parameters which again directly influences the fatigue life of the electronic component. Figure 7.12 shows the axial leaded capacitor geometry used in this case study.



Dimensions (millimeters)

Case Size	Uninsulated D ±0.13	Uninsulated L ±0.79	Insulated D ±0.25	Insulated L ±0.79	B ±0.3	C max.
C/R	7.09	16.51	7.34	17.42	0.64	20.88
D/S	8.66	19.05	8.92	19.96	0.64	23.42

Figure 7.12: Dimensions of the axial leaded capacitor used in the analysis [76]

There can be 3 possible cases that can be considered:

1. L_{cap}=constant and D_{cap} is changing
2. D_{cap}=constant and L_{cap} is changing
3. L_{cap} & D_{cap} are both changing

D_{cap} is the component body diameter and L_{cap} is the component body length. Figure 7.13 & Figure 7.14 show the variation of damage with respect to component body diameter when body length is held constant and the variation of

damage with respect to component body length when body diameter is held constant respectively.

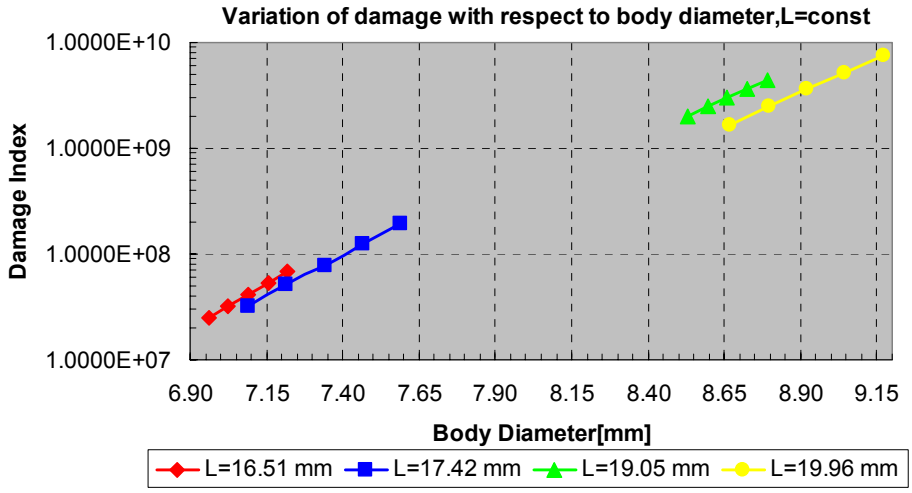


Figure 7.13: Variation of damage with respect to component body diameter when body length is held constant

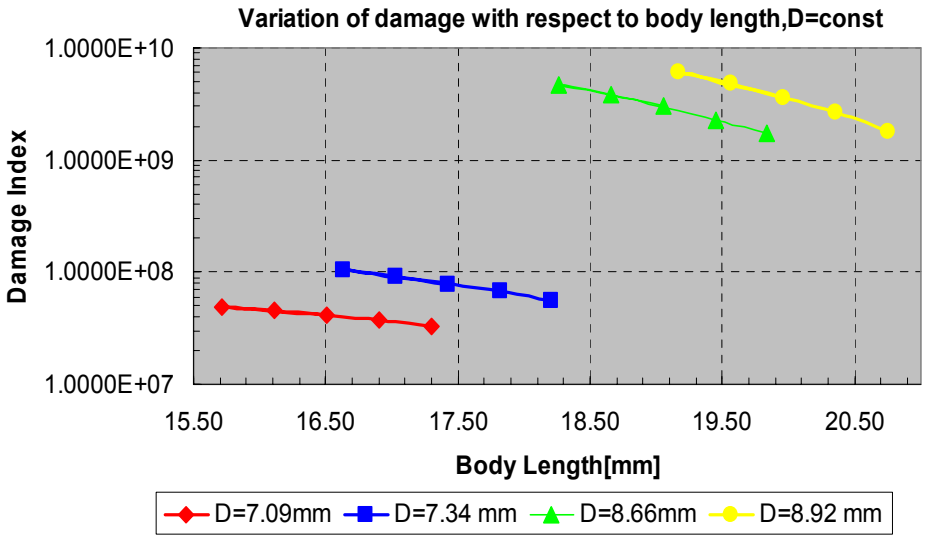


Figure 7.14: Variation of damage with respect to component body length when body diameter is held constant

According to the simulation results the following conclusions can be obtained:

1. When body length is held constant increasing the body diameter increases the fatigue damage.
2. When body diameter is held constant increasing the body length decreases the fatigue damage.
3. When body diameter and length both increases the fatigue damage increases therefore the body diameter is more dominant than the body length in terms of fatigue damage

CHAPTER 8

DISCUSSION AND CONCLUSIONS

Circuit card assembly failures from exposure to vibration are mostly from accumulated fatigue damage. Since most modern components are stress dominated by resonances of the assembly, only those components in high stress positions are likely to be at risk. In this study, vibration induced fatigue analysis has been performed for different types of electronic components used on printed circuit boards. CirVibe software, a purpose built package for electronic circuit card assembly fatigue analysis, is used to illustrate component risk for damage.The design cycle, consisting of testing the test PCB's populated with electronic components, building the finite element models for the PCBs, verification of the models by transmissibility & modal tests and finally numerical fatigue analysis has been applied.

It has been shown how the mechanical design for dynamic loading of circuit boards can be performed using finite element analysis. A close coupling between test and analysis can be used to create a finite element model and to verify its correctness. Then the models are used to determine areas where failure would most likely to occur.

The exact modeling of dynamic behavior of the circuit board is not feasible since the manufacturers do not supply the complete material properties of the components in their data sheets. In addition sometimes designer has to perform extra tests like 3-point bending test of FR-4. FR-4 (epoxy glass laminate) is the most commonly employed composite material used for PCB production. Most of the time FR-4 manufacturers can not give the precise information for the bending modulus or they can only give range for the bending modulus.

However, in order to simulate the actual response of the circuit board this bending modulus must be obtained by 3-point or 4-point bending tests because PCB resonant frequency is very much dependent upon the bending modulus. Besides this test should be performed in crosswise and lengthwise direction since FR-4 is usually an orthotropic material.

It is important to compare the calculated fatigue damage to defined life limits in order to determine which components, if necessary, must be moved to positions of lower damage.Therefore fatigue life usage analysis of components (C63, C64, C65, C102, C103, C104) on the power PCB of the power distribution unit which is used in Leopard 1 battle tank was performed. In the minimum integrity tests, failures were observed for capacitors C102 & C103.Test and simulation results were compatible for C65, C102, C103 & C104. However, for capacitors C63 & C64 test and simulation results were contradictory.This is most probably due to the fact that limited number of tests were performed. That is, if more PCB's were tested to failure then it would be possible to obtain broader life distribution.

Moreover, in order to obtain consistency between simulation and fatigue test results it is very important to obtain standard solder quality. If the same quality for solders is not assured solder joint fatigue failure distribution within the PCB and among the similar PCBs will lead to faulty results.

Fatigue tests performed with the axial leaded Tantalum capacitor reinforced with "eccobond" and silicone showed that by using eccobond and silicone the fatigue lives of the axial leaded capacitors are improved. Furthermore eccobond improves the fatigue life better than the silicone.

Namely, for the life usage analysis of the electronic components it can be argued that only probability of failure can be estimated because the probability of failure depends on the sampling that is used when defining the component capabilities. However this requires excessive testing time and money. And it should always be remembered that there is a large scatter for fatigue live of electronic components.

Stress values used in the fatigue analysis would be better obtained using strain gages. However for structures like printed circuit boards this method can not be used because it is almost impossible to agglutinate the strain gage onto lead wires of the components.

Sensitivity analysis performed for the axial leaded capacitor showed that fatigue damage is maximum for the square shaped PCBs. In addition, fatigue damage trend is different for the young modulus in crosswise and lengthwise directions of the circuit board. Moreover, damage for the axial leaded capacitor is minimum at 45^{o} orientation and maximum for 30^{o} & 60^{o} orientations. Moreover exponential equation can be used to find relation between lead-wire diameter and the accumulated fatigue damage. Finally, it is better to use test based methodology coupled with numerical fatigue analysis rather than using empirical based failure rate prediction tools outlined in reliability handbooks like MIL-HDBK-217.

The fatigue database obtained for the tested component by the application of SST can be used to determine the random vibration profile and duration that will be used as Environmental Stress Screen (ESS) based on the limits identified in ALT.

ESS exposes hardware to environmental loads (like vibration, temp etc.) in order to prevent infant mortality of the product. Vibration screens could be very efficient in finding manufacturing-related problems before shipment. However, detailed understanding is required to determine what level of stress can be applied without damaging the product and lowering its life expectancy. If the vibration screen is effective the reliability of the product will be higher because with an effective screen it is easy to stimulate production related problems and these faults can be corrected before shipment.

Experimental modal analysis has been performed to verify the finite element model of the PCBs such that the finite element models simulate the dynamic characteristics of the actual test circuit boards. It is important here to mention that for printed circuit boards miniature lightweight accelerometers shall be used in order not to affect the dynamic characteristics of the circuit boards.

However if this is not possible the mass of the transducers can also be modeled as local weight in the finite element models and these models should be verified with the test results.

The fatigue tests performed to obtain component capabilities contain some assumptions. First of all the loading is applied in Z axis only. X and Y axis are not considered since it is assumed that the dominant vibration is in Z axis that is perpendicular to the circuit board layout. Actually, the best way is to have 6-DOF vibration test equipment and apply all loadings at the same time with cross correlations. Multi-axis testing is done routinely by the automotive industry as well as seismic simulation systems but the electronics industry is still slow to catch up with simultaneous multi-axis testing. Low-cost single axis electrodynamic shakers are the norm in the electronics industry. However with these shakers it is possible to excite only first few modes of the PCBs in random vibration.

REFERENCES

[1] Esin, A., "Properties of Materials for Mechanical Design", Middle East Technical University, Gaziantep, 1981.

[2] Dally, J.W., "Packaging of Electronic Systems", A Mechanical Engineering Approach, Mc-Graw Hill Series in Mechanical Engineering, 1990.

[3] Steinberg, D.S., "Vibration Analysis for Electronic Equipment", Second edition, John Wiley&Sons, USA, 1988.

[4] Matisoff, B.S., "Handbook of Electronics Manufacturing Engineering", Van Nostrand Reinhold Comp.Inc., 1978.

[5] Wang,H., Zhao, M., Guo,G., "Vibration fatigue experiments of SMT solder joint", The State Key Laboratory of Vibration, Shock and Noise, Shanghai Jiatong University, Shanghai, PR China,2003.

[6] J.C.Roberts, D.M.Stillo,"Random Vibration analysis of a Printed Wiring Board with electronic components", Journal of IES, January/February, pp 25-31, 1991.

[7] D.B.Barker, A.Dasgupta, M.G.Pecht,"PWB Solder Joint Life Calculation under Thermal and Vibration Loading, "Journal of IES, January/February, pp 17-25,1992.

[8] Sidharth, and D.B.Barker,"Vibration Induced Fatigue Life Estimation of Corner Leads of Peripheral Leaded Components,"Journal of Electronic Packaging, Vol. 118, pp 244-249, 1996.

[9] Liguore, and D. Folllowell,"Vibration Fatigue of Surface Mount Technology (SMT) Solder Joints", Proceedings of Annual Reliability and Maintainability Symposium, pp 18-26, 1995.

[10] S.Fields, S.Liguore, D.Followell, R.Perez, R.,"High and Low-Cycle Fatigue Characteristics of Leadless Chip Carrier Solder Joints", ASME paper, 92-WA/EEP-26, 1992.

[11] S.J.Ham, S.B.Lee,"Experimental Study for Reliability of Electronic Packaging under Vibration", Experimental Mechanics, Vol.36, No.4, pp 339-344, 1996.

[12] E.Jih, W.Jung,"Vibrational Fatigue of Surface Mount Solder Joints", Proceedings of InterSociety Conference on Thermal Phenomena, pp 246-250, 1998.

[13] T.E.Wong, B.A.Reed, H.M.Cohen, D.W.Chu,"Development of BGA Solder Joint Vibration Fatigue Life Prediction Model", Proceedings of 1999 Electronic Components and Technology Conference, pp 149-154, 1999.

[14] W.W.Lee, L.T.Nguyen, G.S.Selvaduray, "Solder joint fatigue models:review and applicability to chip scale packages",Microelectronics Reliability,Vol.40,pp231-244,2000.

[15] Qianjin,Y.,"Test and Reliability Analysis of PBGA Assemblies Under Random Vibration, Singapore Institute of Manufacturing Technology, Joining Technology Group,Process Technology Divison,2001.

[16] Renner, T., "Mechanical Design of Circuit Boards Using Finite Element Analysis", ANSYS Proceedings, Pittsburgh, Pennsylvania, April 23-25,1985.

[17] Kucuk, A., Toroslu, R., Carkoglu,N.,"Static and Dynamic Analyses of Electronic Components Subjected to High Accelerations",ANSYS Fifth International Conference and Exhibition ,Volume II,May 20-24,1991.

[18] Lau,J.,Harkins,G.,Rice,D.,Kral,J.,Wells,B.,"Experimental & Statistical Analyses of Surface-Mount Technology PLCC Solder- Joint Reliability",IEEE Transactions on Reliability,Vol.37,No.5, December,1988.

[19] Mesmacque,G.,Garcia,S.,Amrouche,A.,Gonzalez,C.,"Sequential law in multiaxial fatigue, a new damage indicator",International Journal of Fatigue,2005,Vol.27,pp.461-467.

[20] Wu, J., Zhang, R.R, Radons, S., Long, X., "Vibration analysis of medical devices with a calibrated FEA model", Computer & Structures", March 2002.

[21] Guo,G.,Zhao,M.,Wang,H.,F.,"SMT solder joint's semi-experimental fatigue model",Mechanics Research Communication,May,2004.

[22] D. Barker, Y. Chen, "Modeling the Vibrational Restraint of Wedge Lock Card Guides", ASME Winter Annual Meeting, paper number 92-WA/EEP-16, Anaheim, CA, November 9-13, 1992.

[23] D. Barker, Y. Chen, A.Dasgupta,"Vibration Fatigue Life Calculations for Components Mounted on PWBs", Journal of Electronic Packaging, Vol. 115, No. 2, pp. 195-200, June 1993.

[24] Starr, J., "Understanding electronic system vibration life capabilities", Proceedings Military/Aerospace COTS Conference, August 25-27, 1999.

[25] D. Barker, I. Sharif, A. Dasgupta ,"Effect of SMC Lead Dimensional Variabilities on Lead Compliance and Solder Joint Fatigue Life", Journal of Electronic Packaging, Transactions of the ASME, Vol. 144, pp. 177-184, June 1992.

[26] Bishop, NWM, "Vibration Fatigue Analysis in the Finite Element Environment" XVI Encuentro Del Grupo Español De Fractura, Spain, 1999.

[27] Wu, W. F., Liou, H. Y., Tse, H. C., "Estimation of Fatigue Damage and Fatigue Life of Components Under Random Loading", International Journal of Pressure Vessels and Piping, 1997, Vol.72, pp.243-249.

[28] Liou, H.Y., Wu, W.F., Shin, C.S., "A Modified Model for The Estimation of Fatigue Life Derived from Random Vibration Theory", Probabilistic Engineering Mechanics, 1999, Vol.14, pp.281-288.

[29] Blattau,N.,"Models For Rapid Assessment of Surface Mount Component Failures During Printed Wiring Board Bending", CALCE Electronic Packaging Research Centre, University of Maryland, 2004.

[30] Haller, D., Neumaier, K., Schelzig, U., "A Tool for the Thermal and Mechanical Simulation of Printed Circuit Boards", ANSYS Conference Proc., 1991.

[31] Colyer, R. E., McGuigan, S.J., "Reliability Assurance In Low Volume High Technology Equipment", Royal Military College of Science (Cranfield), Shrivenham, Swindon, Wilts, UK, 1993.

[32] Shigley J.E., Mischke, C.R., "Mechanical Engineering Design",Fifth Edition,McGraw-Hill International Editions,1989.

[33] Lalanne, C., "Mechanical Vibration & Shock, Fatigue Damage Volume IV", Hermes Penton Ltd, 2002.

[34] Bannantine, J.A., Comer J.J., Handrock, J.L.,"Fundamentals of Metal Fatigue Analysis", Prentice-Hall Inc., 1990.

[35] Candan, B., "Yorulma Teorisine Giriş, Eğitim Notları", Figes, 2003.

[36] "Rothbart H.A.,"Mechanical Design and System Handbook", 2 nd. Edition, McGraw Hill International Editions, Mechanical Engineering Series, 1986.

[37] Hieber, G., 2005, *Use and Abuse of Test Time Exaggeration Factors*, http:\\www.ttiedu.com, visited on August 2006.

[38] Collins, J.A.,"Failure of Materials in Mechanical Design", "Analysis, Prediction, Prevention",Second Edition, John Wiley & Sons,1993.

[39] Topper T.H.,Sandor B.I.,Morrow,J.D.,"Cumulative fatigue damage under cylic strain control",Journal of Materials,Vol.4,March 1969,p.189/199.

[40] Yang, J.N.,"Simulation of random envelope processes", Journal of Sound and Vibrations, Vol 21.,1972,p.73/85.

[41] nCode Training Notes, "Integrated Durability Management", December 2004.

[42] NWM Bishop, F. Sherratt, "Finite Element Based Fatigue Calculations", NAFEMS, 2000.

[43] CirVibe Inc, "CirVibe Version 2003 User's Manual", USA, 2003.

[44] Schijve, J.,"The accumulation of fatigue damage in aircraft materials and structures, AGARDograph, AG.157, January, 1972.

[45] Miles, J. W., "On Structural Fatigue Under Random Loading", Aeronautical Sciences, pg 753, November, 1954.

[46] Simmons, R.," Miles Equation", NASA Goddard Space Flight Center, May, 2001.

[47] Starr, J., CirVibe Support Service, CirVibe Inc., POB 47394; Plymouth, MN 55447; (612) 559-5166, http://www.cirvibe.com ,2005.

[48] ASTM D3580 Standard Test Methods for Vibration (Vertical Linear Motion) Test of Products, 2004.

[49] Nikkhoo, M,"Vibration Analysis for Electronic Equipment", Electronics Cooling, Volume 11, No: 3, Celestica Corporation, August, 2005.

[50] Gilbert, J.B., "Random Vibration of Printed Wiring Assemblies", Hughes Aircraft CO., Fullerton, CA.1989 Proceedings-Institute of Environmental Sciences.

[51] Tustin, W., "Environmental Vibration and Shock Testing, Measurement, Analysis and Calibration", Tustin Institute of Technology, Santa Barbara, California, 1977.

[52] Richardson, M.H., "Modal Analysis versus Finite-Element Analysis", Sound and Vibration, September, 2005.

[53] Schwarz B.J., Richardson, M. H., "Experimental Modal Analysis", CSI Reliability Week, Orlando, October, 1999.

[54] LMS Test Lab Release 4A Software Manual and Training Notes, LMS International, Belgium, 2003.

[55] Mallick, P.K.,"Fiber-Reinforced Composites Materials, Manufacturing, And Design", Marcel Dekker Inc., 1988.

[56] ASTMD790–99 Standard Test Methods for Flexural Properties of Unreinforced and Reinforced Plastics and Electrical Insulating Materials, 1999.

[57] Ling Dynamics Inc.,"LDS V895-440 HBT 900C Model Vibration Shaker User Manual", England, 2004.

[58] IEST-RP-PR001.1 Appendix A, Vibration Stress Screening Characteristics Development, Institute of Environmental Sciences and Technology, 1999.

[59] Peck, D.S., & Trapp, O.D. "Accelerated Testing Handbook", Technology Associates & D.S. Peck Consulting Corp., 1987.

[60] Khamis, I. H., Higgins, J.J.,"A new model for step stress testing", IEEE Transactions on Reliability, 1998, Volume 47(2), p.131-134.

[61] Hobbs, G.K., "Highly Accelerated Life Tests", Proceedings of Institute of Environmental Sciences, 1992.

[62] Starr, J., "Optimizing HALT, ESS and HASS of Electronic Circuit Cards", CirVibe Inc., Plymouth, USA, 2003.

[63] *MatWeb Online Materials Information Resource*, http:\\www.matweb.com, visited on August 2006.

[64] Nelson, W. "Applied Life Data Analysis, Wiley series in probability and mathematical statistics", ISSN O271–6356, USA, 1982.

[65] Vardeman, S.B., "Statistics for Engineering Problem Solving", ISBN 0-534-92871-4, PWS Foundations in Engineering Series, IEEE Press, Boston, 1994.

[66] Miller, Irwin, Freud, J. E., "Probability and Statistics for Engineers", 2nd Edition, 1977.

[67] PCB Product Catalog, Shock and Vibration Sensors Division, USA, 1999.

[68] IOTECH 16 bit-1MHz Data Acquisition System with Ethernet Interface and eZ-Analyst software 3.3.0.74 User Manual, 2005.

[69] IPC-SM–782 Surface Mount Design and Land Pattern Standard, Association Connecting Electronics Industries, Northbrook, Illinois, 2004.

[70] Packages and Packaging Methodologies Handbook, Spansion, August, 2005.

[71] Endevco Product Catalog, Shock and Vibration Sensors Division, USA, 2005.

[72] nCode Glyphworks Version 3.0 User Manual, 2005.

[73] IPC-SM 785 Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments, November, 1992.

[74] MIL-STD-810F, "Environmental Engineering Considerations and Laboratory Tests", Department of Defense Test Method Standard, USA, 2000.

[75] Newland, D.E., "An Introduction to Random Vibrations, Spectral and Wavelet Analysis", Third Edition, Pearson Education Limited, 1993.

[76] Gökçen M.,"Axial Leaded Tantalum Capacitor Material Specification", MST-ETM/ASELSAN, 1992.

[77] *Fairchild MM74HC04 Hex Inverter Datasheet*, http:\\www.fairchildsemi.com , visited on August 2006.

[78] Matlab 7.0 R14 User Manual, Mathworks Corp., USA, 2005.

APPENDIX-A

DAMAGE DETECTION SYSTEM FOR THE PCB POPULATED WITH AXIAL LEADED TANTALUM CAPACITORS

In order to detect failures of the capacitors remotely; alternative current (AC at 2 kHz) was used because under AC capacitors behave like a wire without resistance which makes up a suitable path for the current flow. However, under direct current (DC) capacitors do not let the current flow therefore they act as if there were an open circuit. Figure A.1 indicates the schematic representation of the damage detection circuit designed. In addition, the capacitors were divided into two groups in order to facilitate the procedure used to find out the damaged capacitor(s).

When there is no damage (Figure A.2a) for the capacitors potential difference ΔV (potential difference read from the oscilloscope) is 2V peak-to-peak (or $\sqrt{2}/2$ V rms). However when there is damage potential difference drops (Figure A.2b) suddenly because at that time capacitor(s) will cause an open circuit so that potential difference drops to 0.

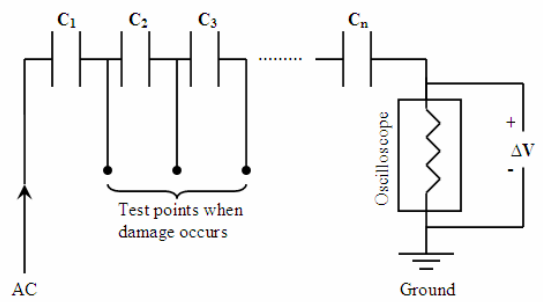
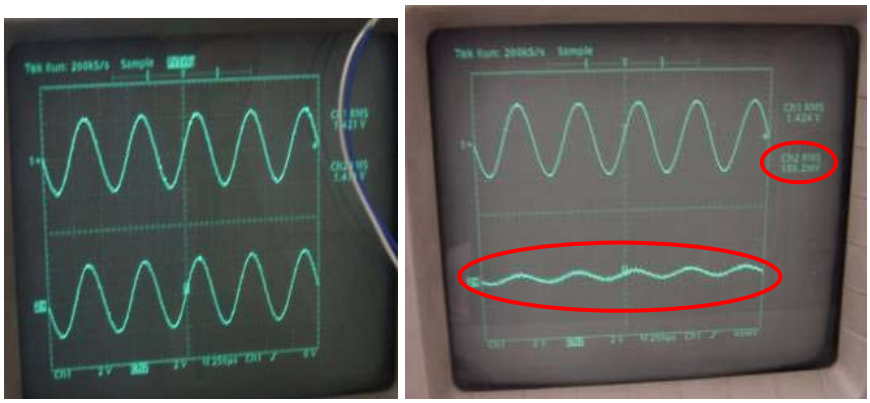


Figure A.1: Schematic representation of the damage detection circuit for the capacitors

The test set up does not directly indicate which capacitor is damaged but it can understand the group of the damaged capacitor. However by using a control probe which is shown in Figure A.3 the damaged capacitor can be detected correctly.



(a) (b)

Figure A.2: a) normal operating condition b) voltage drop when there is failure

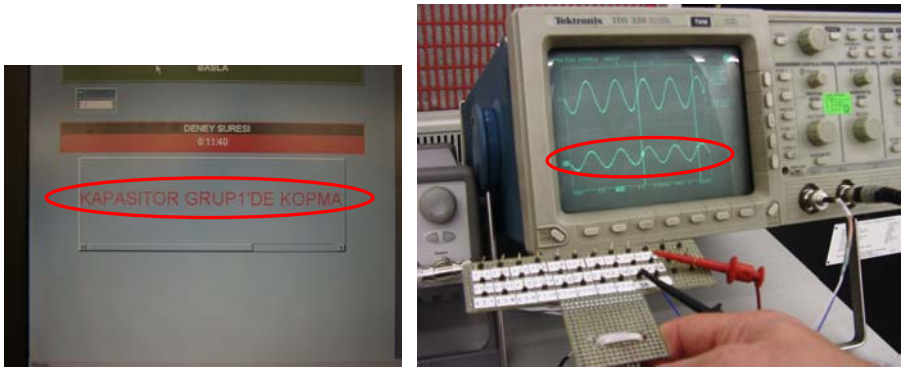


Figure A.3: Control Probe used to detect damaged capacitor(s)

APPENDIX-B

DAMAGE DETECTION SYSTEM FOR THE PCB POPULATED WITH PDIP COMPONENT

In order to detect damaged PDIP (Figure B.1) C PORT P10-96 (C level) 96 channel signal I/O test equipment is used. In the tests 6 ports (3 ports for the input channels (24 input channels) and 3 ports for the output channels (24 output channels)) of the test equipment were used.Each port involves 8 PDIP.

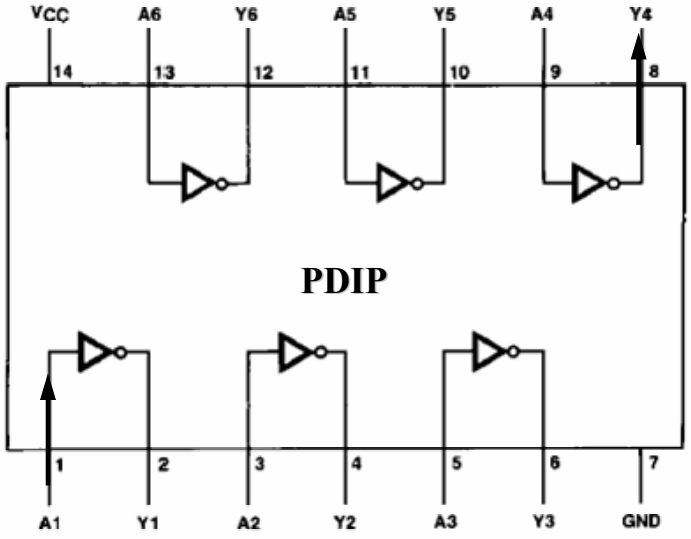


Figure B.1: Pin Assignments for PDIP [77]

Pin A1 is connected to the signal input (0 or 5V). Pin Y4 is connected to the signal output (0 or 5V).Pin 14 is connected to the supply voltage (V_{CC} :5V). Pin Y1 is connected to pin A2. Pin Y2 is connected to pin A3. Pin Y3 is connected to pin A6. Pin Y6 is connected to pin A5. Pin Y5 is connected to pin A4.

Logic used in the plastic dual inline package can be divided into two categories:

1. Positive Logic (PL): 5V input represents 1. 0V input represents 0.
2. Negative Logic (NL): 5V input represents 0. 0V input represents 1.

The numbers 1 and 0 are binary numbers and have meanings in logic circuits.They are used to quantize the analog inputs. Under normal operating conditions (Figure B.2), no matter how the logic is selected the given input should be obtained at the output port.

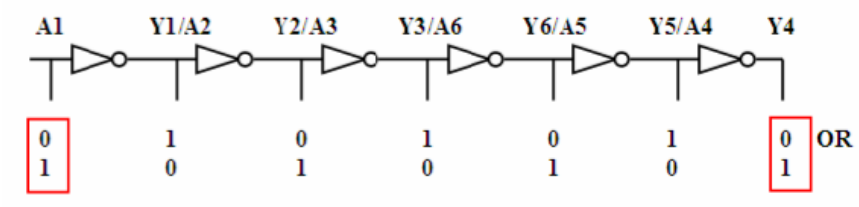


Figure B.2: Logic Diagram for normal operating condition

When there is failure the given input (5V DC input) can not be obtained in the same way (input: 1→output:0 or input: 0→output:1) at the pin (at the relevant lead wire) where failure has occurred.

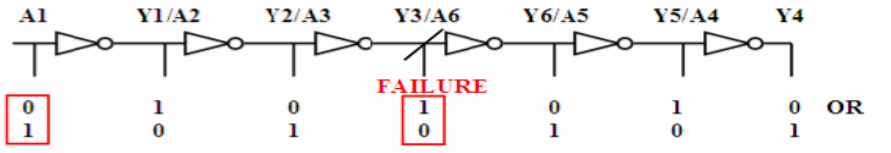


Figure B.3: Logic Diagram when failure occurs

APPENDIX-C

SAMPLE MATLAB® M.FILE FOR THE WEIBULL DISTRIBUTION

The probability density function, reliability function, hazard (failure) rate function, the shape and scale parameter of the Weibull life-time model and MTTF values are all calculated using Matlab [78] built-in functions. Below the sample Matlab m.fie is shown which is related to 1.test PCB populated with Tantalum Capacitors.The Weibull functions and parameters for the other test PCB's can be calculated with the same code just by changing the failure time values used as the inputs.

```
Failure_time_Tantalum_PCB_1=[152;175;178;184;243;257;260;270;277];
                    % fatigue lives of the capacitors obtained in SST
```

INPUT

```
t=Failure_time_Tantalum_PCB_1;

parmhat=wblfit(t); % returns the maximum likelihood estimates of the Weibull parameters

a=parmhat(1);       % scale parameter

b=parmhat(2);       % shape parameter

y=wblpdf(t,a,b);    % computes the Weibull pdf at each of the values in t using the
corresponding parameters a and b

plot(t,y)

p=wblcdf(t,a,b);    % computes the Weibull cdf at each of the values in t using the
corresponding parameters a and b

r=1-p;              % reliability function for the Weibull distribution

plot(t,r)

[m,v]=wblstat(a,b) % returns the mean(MTTF)and variance for the Weibull distribution with
parameters specified by a and b

h=wblpdf(t,a,b)./(1-wblcdf(t,a,b));
                    % hazard rate function for the Weibull distribution

plot(t,h)
```

Figure C.1: Matlab m file used to find out the Weibull parameters for the failed axial leaded Tantalum capacitors

APPENDIX-D

STEP STRESS TEST (SST) VIBRATION PROFILES (INPUTS) FOR THE TESTED PCB

Table D.1 shows the step stress test vibration profiles used in the accelerated life tests of the electronic components.Note that the amplification factor between two successive steps is the slope of the S-N curve of the leadwire/solder material of the component.

Table D.1: SST Bandlimited Whitenoise Vibration Test Profiles

STEP	Bandwidth [Hz]	Amplitude [g^2/Hz]	RMS [g]	Duration [min]
1	20-2000	2,020E-03	2	60
2	20-2000	3,160E-03	2,5	60
3	20-2000	4,930E-03	3,13	60
4	20-2000	7,710E-03	3,91	60
5	20-2000	1,200E-02	4,88	60
6	20-2000	1,880E-02	6,1	60
7	20-2000	2,940E-02	7,63	60
8	20-2000	4,600E-02	9,54	60
9	20-2000	7,180E-02	11,93	60
10	20-2000	1,120E-01	14,91	60
11	20-2000	1,750E-01	18,63	60
12	20-2000	2,740E-01	23,3	60
13	20-2000	4,300E-01	29,13	60
14	20-2000	6,694E+02	36,41	60

APPENDIX-E

RELATIVE & TOTAL DAMAGE NUMBERS OF THE FAILED AXIAL LEADED TANTALUM CAPACITORS

Table E.1: Relative damage numbers *d* for the failed capacitors on the test PCB's

DAMAGE SEQUENCE	PCB 1	SST DAMAGE FACTOR
1.	C115	64.333
2.	C102	102.667
3.	C106	114.333
4.	C114	214.333
5.	C104	1944.333
6.	C123	4277.667
7.	C111	4777.667
8.	C108	6444.333
9.	C135	7611.000

DAMAGE SEQUENCE	PCB 2	SST DAMAGE FACTOR
1.	C135	69.333
2.	C127	211.000
3.	C122	827.667
4.	C131	2111.000
5.	C113	21111.000
6.	C115	36111.000
7.	C106	39444.333
8.	C126	62777.667
9.	C129	77777.667
10.	C102	86111.000
11.	C132	89444.333

DAMAGE SEQUENCE	PCB 3	SST DAMAGE FACTOR
1.	C104	511.000
2.	C127	711.000
3.	C135	1077.667
4.	C106	2611.000
5.	C108	3944.333
6.	C128	42777.667
7.	C114	62777.667
8.	C123	62777.667
9.	C115	109444.333

Table E.2: Total accumulated damage numbers for the failed capacitors on the 1.PCB

COMPONENTS SORTED BY DAMAGE LEVEL (PCB 1):

COMPONENT_MODE NAME	DAMAGE FILE	Damage SST_1	DamageTot
KN3	CON033_	0.1762E-21	
KN2	CON032_	0.4222E-33	
KN1	CON031_	0.2377E-39	
C127	R-C021_	0.7889E-03	
C132	R-C025_	0.6268E-03	
C108	R-C008_	0.4797E-03	3,0913E+00
C131	R-C024_	0.4563E-03	
C124	R-C018_	0.4228E-03	
C129	R-C023_	0.3687E-03	
C106	R-C006_	0.3432E-03	3,9239E-02
C107	R-C007_	0.3309E-03	
C137	R-C030_	0.2744E-03	
C125	R-C019_	0.2647E-03	
C122	R-C016_	0.2555E-03	
C136	R-C029_	0.2541E-03	
C126	R-C020_	0.2359E-03	
C117	R-C015_	0.1789E-03	
C133	R-C026_	0.1724E-03	
C116	R-C014_	0.1518E-03	
C128	R-C022_	0.1487E-03	
C135	R-C028_	0.1273E-03	9,6888E-01
C123	R-C017_	0.1108E-03	4,7397E-01
C134	R-C027_	0.1033E-03	
C114	R-C012_	0.9783E-04	2,0968E-02
C104	R-C004_	0.3533E-04	6,8693E-02
C105	R-C005_	0.2741E-04	
C113	R-C011_	0.2652E-04	
C115	R-C013_	0.1866E-04	1,2005E-03
C102	R-C002_	0.7306E-06	7,5009E-05
C112	R-C010_	0.2926E-06	
C111	R-C009_	0.2339E-06	1,1175E-03
C103	R-C003_	0.8823E-07	
C101	R-C001_	0.5429E-07	

Table E.3: Total accumulated damage numbers for the failed capacitors on the 2.PCB

COMPONENTS SORTED BY DAMAGE LEVEL (PCB 2):

COMPONENT_NAME	MODE FILE	DAMAGE Damage SST_1	DamageTot
KN3	CON033_	0.1762E-21	
KN2	CON032_	0.4222E-33	
KN1	CON031_	0.2377E-39	
C127	R-C021_	0.7889E-03	1,6646E-01
C132	R-C025_	0.6268E-03	5,6064E+01
C108	R-C008_	0.4797E-03	
C131	R-C024_	0.4563E-03	9,6325E-01
C124	R-C018_	0.4228E-03	
C129	R-C023_	0.3687E-03	2,8677E+01
C106	R-C006_	0.3432E-03	1,3537E+01
C107	R-C007_	0.3309E-03	
C137	R-C030_	0.2744E-03	
C125	R-C019_	0.2647E-03	
C122	R-C016_	0.2555E-03	2,1147E-01
C136	R-C029_	0.2541E-03	
C126	R-C020_	0.2359E-03	1,4809E+01
C117	R-C015_	0.1789E-03	
C133	R-C026_	0.1724E-03	
C116	R-C014_	0.1518E-03	
C128	R-C022_	0.1487E-03	
C135	R-C028_	0.1273E-03	8,8261E-03
C123	R-C017_	0.1108E-03	
C134	R-C027_	0.1033E-03	
C114	R-C012_	0.9783E-04	
C104	R-C004_	0.3533E-04	
C105	R-C005_	0.2741E-04	
C113	R-C011_	0.2652E-04	5,5986E-01
C115	R-C013_	0.1866E-04	6,7383E-01
C102	R-C002_	0.7306E-06	6,2913E-02
C112	R-C010_	0.2926E-06	
C111	R-C009_	0.2339E-06	
C103	R-C003_	0.8823E-07	
C101	R-C001_	0.5429E-07	

Table E.4: Total accumulated damage numbers for the failed capacitors on the 3.PCB

COMPONENTS SORTED BY DAMAGE LEVEL (PCB 3):

COMPONENT_NAME	MODE DAMAGE FILE	Damage SST_1	DamageTot
KN3	CON033_	0.1762E-21	
KN2	CON032_	0.4222E-33	
KN1	CON031_	0.2377E-39	
C127	R-C021_	0.7889E-03	5,6091E-01
C132	R-C025_	0.6268E-03	
C108	R-C008_	0.4797E-03	1,8921E+00
C131	R-C024_	0.4563E-03	
C124	R-C018_	0.4228E-03	
C129	R-C023_	0.3687E-03	
C106	R-C006_	0.3432E-03	8,9610E-01
C107	R-C007_	0.3309E-03	
C137	R-C030_	0.2744E-03	
C125	R-C019_	0.2647E-03	
C122	R-C016_	0.2555E-03	
C136	R-C029_	0.2541E-03	
C126	R-C020_	0.2359E-03	
C117	R-C015_	0.1789E-03	
C133	R-C026_	0.1724E-03	
C116	R-C014_	0.1518E-03	
C128	R-C022_	0.1487E-03	6,3610E+00
C135	R-C028_	0.1273E-03	1,3719E-01
C123	R-C017_	0.1108E-03	6,9558E+00
C134	R-C027_	0.1033E-03	
C114	R-C012_	0.9783E-04	6,1415E+00
C104	R-C004_	0.3533E-04	1,0181E-01
C105	R-C005_	0.2741E-04	
C113	R-C011_	0.2652E-04	
C115	R-C013_	0.1866E-04	2,0422E+00
C102	R-C002_	0.7306E-06	
C112	R-C010_	0.2926E-06	
C111	R-C009_	0.2339E-06	
C103	R-C003_	0.8823E-07	
C101	R-C001_	0.5429E-07	

APPENDIX-F

TOTAL DAMAGE NUMBERS OF PDIP

Table F.1: Total accumulated damage numbers for the PCB populated with Plastic Dual Inline Packages (PDIP) & connectors

COMPONENTS SORTED BY DAMAGE LEVEL:
COMPONENT_MODE DAMAGE

NAME	FILE	DAMAGE
KN2	CON002_	0.1890E-03
KN1	CON001_	0.9082E-06
TD3	DIP020_	0.7522E+04
TD4	DIP021_	0.7241E+04
TD5	DIP022_	0.6895E+04
TD2	DIP014_	0.6600E+04
TD1	DIP003_	0.2432E+04
TD6	DIP023_	0.2160E+04
TD11	DIP005_	0.1874E+04
TD8	DIP025_	0.1828E+04
TD10	DIP004_	0.1402E+04
TD9	DIP026_	0.1343E+04
TD21	DIP016_	0.6495E+03
TD22	DIP017_	0.5520E+03
TD15	DIP009_	0.5019E+03
TD16	DIP010_	0.4854E+03
TD23	DIP018_	0.1450E+03
TD20	DIP015_	0.1381E+03
TD14	DIP008_	0.1110E+03
TD17	DIP011_	0.1087E+03
TD7	DIP024_	0.9050E+02
TD12	DIP006_	0.7878E+02
TD24	DIP019_	0.2470E+02
TD19	DIP013_	0.2407E+02
TD13	DIP007_	0.1515E+02
TD18	DIP012_	0.1370E+02

APPENDIX-G

RELATIVE & TOTAL DAMAGE NUMBERS OF THE FAILED AXIAL LEADED ALUMINIUM CAPACITORS

Table G.1: Relative damage numbers *d* for the failed aluminum electrolytic capacitors on the test PCB's

DAMAGE SEQUENCE	PCB 1	SST DAMAGE FACTOR
1.	C131	170555.444
2.	C132	835944.333
3.	C122	2224999.889
4.	C112	4688888.778
5.	C102	5111111.000
6.	C123	6149999.888
7.	C126	6149999.888
8.	C134	7299999.888
9.	C105	7608333.222
10.	C113	9030555.445

DAMAGE SEQUENCE	PCB 2	SST DAMAGE FACTOR
1.	C126	68055.444
2.	C111	103333.222
3.	C131	615277.667
4.	C101	2272222.111
5.	C123	3966666.555
6.	C122	4052777.667
7.	C134	4661111.000
8.	C132	8113888.778
9.	C114	9011111.000
10.	C133	9288888.778

Table G.2: Total accumulated damage numbers for the failed capacitors on the 1.PCB

COMPONENTS SORTED BY DAMAGE LEVEL (PCB 1):
COMPONENT_MODE DAMAGE

NAME	FILE	Damage SST_1	DamageTot
KN3	CON023_	0.2506E-13	
KN2	CON022_	0.6784E-25	
KN1	CON021_	0.3543E-30	
C103	R-C003_	0.6069E-01	
C113	R-C008_	0.4382E-01	3.9572E+05
C125	R-C014_	0.4372E-01	
C131	R-C016_	0.4031E-01	6.8751E+03
C124	R-C013_	0.4029E-01	
C123	R-C012_	0.3813E-01	2.3450E+05
C132	R-C017_	0.3621E-01	3.0270E+04
C134	R-C019_	0.3508E-01	2.5608E+05
C133	R-C018_	0.3279E-01	
C135	R-C020_	0.2933E-01	
C126	R-C015_	0.2370E-01	1.4575E+05
C122	R-C011_	0.2157E-01	4.7993E+04
C104	R-C004_	0.1193E-01	
C114	R-C009_	0.1006E-01	
C115	R-C010_	0.9408E-02	
C105	R-C005_	0.7796E-02	5.9315E+04
C112	R-C007_	0.1070E-03	5.0171E+02
C102	R-C002_	0.9021E-04	4.6107E+02
C101	R-C001_	0.8409E-04	
C111	R-C006_	0.6556E-04	

Table G.3: Total accumulated damage numbers for the failed capacitors on the 2.PCB

COMPONENTS SORTED BY DAMAGE LEVEL (PCB 2):
COMPONENT_MODE DAMAGE

NAME	FILE	Damage SST_1	DamageTot
KN3	CON023_	0.2506E-13	
KN2	CON022_	0.6784E-25	
KN1	CON021_	0.3543E-30	
C103	R-C003_	0.6069E-01	
C113	R-C008_	0.4382E-01	
C125	R-C014_	0.4372E-01	
C131	R-C016_	0.4031E-01	2.4802E+04
C124	R-C013_	0.4029E-01	
C123	R-C012_	0.3813E-01	1.5125E+05
C132	R-C017_	0.3621E-01	2.9380E+05
C134	R-C019_	0.3508E-01	1.6351E+05
C133	R-C018_	0.3279E-01	3.0458E+05
C135	R-C020_	0.2933E-01	
C126	R-C015_	0.2370E-01	1.6129E+03
C122	R-C011_	0.2157E-01	8.7418E+04
C104	R-C004_	0.1193E-01	
C114	R-C009_	0.1006E-01	9.0652E+04
C115	R-C010_	0.9408E-02	
C105	R-C005_	0.7796E-02	
C112	R-C007_	0.1070E-03	
C102	R-C002_	0.9021E-04	
C101	R-C001_	0.8409E-04	1.9107E+02
C111	R-C006_	0.6556E-04	6.7745E+00

APPENDIX-H

RELATIVE & TOTAL DAMAGE NUMBERS OF THE FAILED AXIAL LEADED ALUMINIUM CAPACITORS REINFORCED WITH ECCOBOND & SILICONE

Table H.1: Relative damage numbers *d* for the failed aluminum electrolytic capacitors bonded to the PCB with epoxy (eccobond 55) coating

DAMAGE SEQUENCE	PCB_WITH_EPOXY_COATING	SST DAMAGE FACTOR
1.	C123	1058333.222
2.	C131	37055555.450
3.	C132	51916666.550
4.	C134	51916666.550
5.	C126	81444444.330
6.	C133	279999999.800
7.	C113	525833333.200
8.	C105	7391666666.000
9.	C114	11111111111.000
10.	C122	11111111111.000

Table H.2: Total accumulated damage numbers for the failed capacitors bonded to PCB with epoxy

COMPONENTS SORTED BY DAMAGE LEVEL (PCB_WITH_EPOXY_COATING):

COMPONENT_MODE NAME	DAMAGE FILE	Damage_SST_1	DamageTot
KN3	CON023_	0.2336E-12	
KN2	CON022_	0.1805E-22	
KN1	CON021_	0.1822E-29	
C123	R-C012_	0.5415E-06	5.7309E-01
C131	R-C016_	0.4907E-06	1.8183E+01
C113	R-C008_	0.2967E-06	1.5601E+02
C126	R-C015_	0.2418E-06	1.9693E+01
C132	R-C017_	0.6125E-07	3.1799E+00
C134	R-C019_	0.4588E-07	2.3819E+00
C133	R-C018_	0.3632E-07	1.0170E+01
C122	R-C011_	0.3030E-07	3.3667E+02
C103	R-C003_	0.1296E-08	
C105	R-C005_	0.1037E-08	7.6652E+00
C114	R-C009_	0.4206E-09	4.6733E+00
C125	R-C014_	0.3292E-09	
C124	R-C013_	0.2477E-09	
C135	R-C020_	0.1963E-10	
C104	R-C004_	0.8017E-11	
C115	R-C010_	0.4158E-12	
C102	R-C002_	0.1233E-12	
C111	R-C006_	0.1233E-12	
C112	R-C007_	0.1336E-13	
C101	R-C001_	0.6091E-14	

Table H.3: Relative damage numbers *d* for the failed aluminum electrolytic capacitors bonded to the PCB with silicone (OMNIVISC 1050) coating

DAMAGE SEQUENCE	PCB_WITH_SILICONE_COATING	SST DAMAGE FACTOR
1.	C131	66944.333
2.	C123	259999.889
3.	C126	699166.556
4.	C134	2199999.889
5.	C113	5861111.000
6.	C132	9502777.667
7.	C122	11111111.000
8.	C105	21555555.440
9.	C133	26388888.770
10.	C114	82388888.780

Table H.4: Total accumulated damage numbers for the failed capacitors bonded to PCB with silicone

COMPONENTS SORTED BY DAMAGE LEVEL (PCB WITH SILICONE COATING):

COMPONENT_MODE NAME	DAMAGE FILE	Damage_SST_1	DamageTot
KN3	CON023_	0.9642E-22	
KN2	CON022_	0.1835E-30	
KN1	CON021_	0.4463E-36	
C123	R-C012_	0.3860E-11	1.0040E-06
C131	R-C016_	0.2208E-11	1.4800E-07
C122	R-C011_	0.3563E-13	3.9600E-07
C132	R-C017_	0.3094E-13	2.9400E-07
C134	R-C019_	0.1534E-13	3.4000E-08
C113	R-C008_	0.2283E-14	1.3000E-08
C126	R-C015_	0.1141E-14	1.0000E-09
C133	R-C018_	0.1093E-14	2.9000E-08
C135	R-C020_	0.1111E-15	
C103	R-C003_	0.1938E-16	
C125	R-C014_	0.1702E-16	
C114	R-C009_	0.3357E-17	2.7658E-10
C124	R-C013_	0.5115E-18	
C105	R-C005_	0.1422E-19	3.0652E-13
C115	R-C010_	0.7274E-20	
C104	R-C004_	0.2084E-20	
C102	R-C002_	0.2167E-21	
C112	R-C007_	0.1611E-21	
C111	R-C006_	0.4488E-22	
C101	R-C001_	0.2057E-24	

APPENDIX-I

RELATIVE & TOTAL DAMAGE NUMBERS OF THE FAILED SM CERAMIC CAPACITORS

Table I.1: Relative damage numbers *d* for the failed ceramic SM capacitors

DAMAGE SEQUENCE	PCB_1	SST DAMAGE FACTOR
1.	C133	9.36944E+10
2.	C125	2.66111E+11
3.	C134	3.01389E+11

DAMAGE SEQUENCE	PCB_2	SST DAMAGE FACTOR
1.	C127	1.06611E+12

DAMAGE SEQUENCE	PCB_3	SST DAMAGE FACTOR
1.	C132	1.53333E+10
2.	C122	6.46389E+10
3.	C134	1.65833E+11
4.	C124	4.87778E+11
5.	C127	5.10278E+11
6.	C117	5.18333E+11

Table I.2: Total accumulated damage numbers of the damaged and non damaged SM capacitors on the 1.PCB

COMPONENTS SORTED BY DAMAGE LEVEL (PCB 1):
COMPONENT_MODE DAMAGE

NAME	FILE	Damage SST_1	DamageTot
KN3	CON033_	0.2195E-18	0.2459E-06
KN1	CON031_	0.5220E-34	0.7937E-22
KN2	CON032_	0.5220E-34	0.1122E-21
C122	SRC016_	0.6869E-15	0.7876E-03
C124	SRC018_	0.6869E-15	0.7773E-03
C131	SRC024_	0.5630E-16	0.6478E-04
C132	SRC025_	0.5630E-16	0.6492E-04
C135	SRC028_	0.4400E-16	0.4944E-04
C133	**SRC026_**	**0.4133E-16**	**3.8720E-06**
C115	SRC013_	0.2391E-16	0.2741E-04
C113	SRC011_	0.2313E-16	0.2673E-04
C106	SRC006_	0.1391E-16	0.1565E-04
C108	SRC008_	0.1343E-16	0.1543E-04
C107	SRC007_	0.1165E-16	0.1323E-04
C101	SRC001_	0.1047E-16	0.1198E-04
C103	SRC003_	0.1047E-16	0.1187E-04
C127	SRC021_	0.1008E-16	0.1146E-04
C129	SRC023_	0.1008E-16	0.1135E-04
C128	SRC022_	0.8708E-17	0.1004E-04
C114	SRC012_	0.7792E-17	0.8865E-05
C125	**SRC019_**	**0.4792E-17**	**1.2750E-06**
C126	SRC020_	0.4792E-17	0.5465E-05
C123	SRC017_	0.4053E-17	0.4686E-05
C134	**SRC027_**	**0.2388E-17**	**7.2000E-07**
C104	SRC004_	0.1528E-17	0.1745E-05
C105	SRC005_	0.1463E-17	0.1679E-05
C102	SRC002_	0.1308E-17	0.1464E-05
C112	SRC010_	0.8979E-18	0.1001E-05
C111	SRC009_	0.7827E-18	0.8853E-06
C116	SRC014_	0.1926E-18	0.2139E-06
C117	SRC015_	0.1834E-18	0.2125E-06
C136	SRC029_	0.1746E-18	0.1972E-06
C137	SRC030_	0.1746E-18	0.1953E-06

Table I.3: Total accumulated damage numbers of the damaged and non damaged SM capacitors on the 2.PCB

COMPONENTS SORTED BY DAMAGE LEVEL (PCB 2):
COMPONENT_MODE DAMAGE

NAME	FILE	Damage SST_1	DamageTot
KN3	CON033_	0.2195E-18	0.2459E-06
KN1	CON031_	0.5220E-34	0.7937E-22
KN2	CON032_	0.5220E-34	0.1122E-21
C122	SRC016_	0.6869E-15	0.7876E-03
C124	SRC018_	0.6869E-15	0.7773E-03
C132	SRC025_	0.5630E-16	0.6492E-04
C131	SRC024_	0.5630E-16	0.6478E-04
C135	SRC028_	0.4400E-16	0.4944E-04
C133	SRC026_	0.4133E-16	0.4777E-04
C115	SRC013_	0.2391E-16	0.2741E-04
C113	SRC011_	0.2313E-16	0.2673E-04
C106	SRC006_	0.1391E-16	0.1565E-04
C108	SRC008_	0.1343E-16	0.1543E-04
C107	SRC007_	0.1165E-16	0.1323E-04
C101	SRC001_	0.1047E-16	0.1198E-04
C103	SRC003_	0.1047E-16	0.1187E-04
C127	**SRC021_**	**0.1008E-16**	**1.0746E-05**
C129	SRC023_	0.1008E-16	0.1135E-04
C128	SRC022_	0.8708E-17	0.1004E-04
C114	SRC012_	0.7792E-17	0.8865E-05
C125	SRC019_	0.4792E-17	0.5537E-05
C126	SRC020_	0.4792E-17	0.5465E-05
C123	SRC017_	0.4053E-17	0.4686E-05
C134	SRC027_	0.2388E-17	0.2721E-05
C104	SRC004_	0.1528E-17	0.1745E-05
C105	SRC005_	0.1463E-17	0.1679E-05
C102	SRC002_	0.1308E-17	0.1464E-05
C112	SRC010_	0.8979E-18	0.1001E-05
C111	SRC009_	0.7827E-18	0.8853E-06
C116	SRC014_	0.1926E-18	0.2139E-06
C117	SRC015_	0.1834E-18	0.2125E-06
C136	SRC029_	0.1746E-18	0.1972E-06
C137	SRC030_	0.1746E-18	0.1953E-06

Table I.4: Total accumulated damage numbers of the damaged and non damaged SM capacitors on the 3.PCB

COMPONENTS SORTED BY DAMAGE LEVEL (PCB 3):
COMPONENT_MODE DAMAGE

NAME	FILE	Damage SST_1	DamageTot
KN3	CON033_	0.2195E-18	0.2459E-06
KN1	CON031_	0.5220E-34	0.7937E-22
KN2	CON032_	0.5220E-34	0.1122E-21
C122	**SRC016_**	**0.6869E-15**	**4.4400E-05**
C124	**SRC018_**	**0.6869E-15**	**3.3506E-04**
C132	**SRC025_**	**0.5630E-16**	**8.6300E-07**
C131	SRC024_	0.5630E-16	0.6478E-04
C135	SRC028_	0.4400E-16	0.4944E-04
C133	SRC026_	0.4133E-16	0.4777E-04
C115	SRC013_	0.2391E-16	0.2741E-04
C113	SRC011_	0.2313E-16	0.2673E-04
C106	SRC006_	0.1391E-16	0.1565E-04
C108	SRC008_	0.1343E-16	0.1543E-04
C107	SRC007_	0.1165E-16	0.1323E-04
C101	SRC001_	0.1047E-16	0.1198E-04
C103	SRC003_	0.1047E-16	0.1187E-04
C127	**SRC021_**	**0.1008E-16**	**5.1440E-06**
C129	SRC023_	0.1008E-16	0.1135E-04
C128	SRC022_	0.8708E-17	0.1004E-04
C114	SRC012_	0.7792E-17	0.8865E-05
C125	SRC019_	0.4792E-17	0.5537E-05
C126	SRC020_	0.4792E-17	0.5465E-05
C123	SRC017_	0.4053E-17	0.4686E-05
C134	**SRC027_**	**0.2388E-17**	**3.9600E-07**
C104	SRC004_	0.1528E-17	0.1745E-05
C105	SRC005_	0.1463E-17	0.1679E-05
C102	SRC002_	0.1308E-17	0.1464E-05
C112	SRC010_	0.8979E-18	0.1001E-05
C111	SRC009_	0.7827E-18	0.8853E-06
C116	SRC014_	0.1926E-18	0.2139E-06
C117	**SRC015_**	**0.1834E-18**	**9.5000E-08**
C136	SRC029_	0.1746E-18	0.1972E-06
C137	SRC030_	0.1746E-18	0.1953E-06

APPENDIX-J

TOTAL DAMAGE NUMBERS OF THE COMPONENTS MOUNTED ON THE POWER PCB

Table J.1: Accumulated Fatigue Damage for the Electronic Components Mounted on the Power PCB

COMPONENTS SORTED BY DAMAGE LEVEL (POWER_PCB):

COMPONENT_MODE NAME	DAMAGE FILE	DAMAGE
KN3	CON086_	0.1263E-03
KN2	CON085_	0.9707E-05
KN1	CON084_	0.1599E-05
KN4	CON087_	0.3112E-06
CR7	DCC073_	0.1091E+08
CR6	DCC072_	0.8342E+06
CR5	DCC071_	0.1003E+03
CR4	DCC217_	0.2329E+02
TD12	DIP188_	0.3680E-03
TD9	DIP193_	0.3031E-03
TD10	DIP186_	0.1223E-03
TD11	DIP187_	0.4551E-05

****

COMPONENTS SORTED BY DAMAGE LEVEL (POWER_PCB):

COMPONENT_MODE NAME	DAMAGE FILE	DAMAGE
C63	R-C034_	0.1603E+05
C64	R-C035_	0.6224E+04
ZD9	R-C200_	0.3797E+04
C102	R-C003_	0.1777E+03
C104	R-C005_	0.1926E+03
D13	R-C075_	0.7638E+02
C103	R-C004_	0.1626E+02
R24	R-C103_	0.8964E+01
R22	R-C101_	0.5936E+01
ZD8	R-C199	0.5188E+01

Table J.1 (continued): Accumulated Fatigue Damage for the Electronic Components Mounted on the Power PCB

R36	R-C117_	0.4956E+01
R82	R-C166_	0.1280E+01
R66	R-C148_	0.7850E+00
R65	R-C147_	0.5109E+00
D15	R-C077_	0.4130E+00
R81	R-C165_	0.3931E+00
ZD2	R-C197_	0.7757E-01
C65	R-C036_	0.7618E-01
R25	R-C104_	0.1678E-02
C105	R-C006_	0.1293E-03
R33	R-C114_	0.2951E-05
R41	R-C122_	0.2470E-05
R39	R-C120_	0.1527E-05
R40	R-C121_	0.4307E-06
ZD7	R-C198_	0.8605E-07
R34	R-C115_	0.6277E-07
R38	R-C119_	0.2367E-07
R26	R-C105_	0.5424E-08
R21	R-C100_	0.3044E-08
ZD12	R-C196_	0.2448E-08
R23	R-C102_	0.1760E-08
R69	R-C151_	0.1408E-08
R70	R-C153_	0.1408E-08
R35	R-C116_	0.1080E-08
R30	R-C109_	0.9099E-09
R71	R-C154	0.4649E-09
R37	R-C118_	0.4361E-10
R29	R-C108_	0.4451E-11
R32	R-C113_	0.2217E-11
R28	R-C107_	0.1806E-11
R31	R-C112_	0.1806E-11
R27	R-C106_	0.9099E-12
ZD10	R-C222_	0.5516E-12
D14	R-C076_	0.2521E-12
D43	R-C078_	0.1040E-12

****

COMPONENTS SORTED BY DAMAGE LEVEL (POWER_PCB):

COMPONENT_MODE	DAMAGE	
NAME	FILE	DAMAGE
C203	RC1019_	0.3672E+26
C210	RC1026_	0.1437E+26
C208	RC1024_	0.2308E+24
C99	RC1070_	0.1478E+24
C209	RC1025_	0.4374E+23
C100	RC1001_	0.3071E+23
C96	RC1067_	0.2438E+23
C101	RC1002_	0.4376E+20
C204	RC1020_	0.1911E+18
C202	RC1018_	0.5537E+17
C97	RC1068_	0.8726E+15

Table J.1 (continued): Accumulated Fatigue Damage for the Electronic Components Mounted on the Power PCB

C211	RC1027_	0.3944E+07
C98	RC1069_	0.5350E+05
C205	RC1021_	0.1439E+04
C94	RC1065_	0.1122E+04
C201	RC1017_	0.1988E+01
C200	RC1016_	0.1913E+01
C206	RC1022_	0.9470E-02
C207	RC1023_	0.3603E-02
C95	RC1066_	0.7038E-05

****

COMPONENTS SORTED BY DAMAGE LEVEL (POWER_PCB):

COMPONENT_MODE		DAMAGE
NAME	FILE	DAMAGE
TD14	SMD226_	0.5078E+25
D8	SMD252_	0.1158E+02
D9	SMD251_	0.6220E+01
TD15	SMD190_	0.4276E+01
D10	SMD250_	0.3874E+01
D6	SMD232_	0.3560E+01
TD2	SMD191_	0.4620E+00
TR15	SMD245_	0.7394E-01
TR4	SMD264_	0.4166E-01
TR3	SMD237_	0.8074E-03
D7	SMD231_	0.5650E-03
TD7	SMD243_	0.2550E-03
TR5	SMD238_	0.9297E-06
D5	SMD228_	0.3132E-07

****

COMPONENTS SORTED BY DAMAGE LEVEL (POWER_PCB):

COMPONENT_MODE		DAMAGE
NAME	FILE	DAMAGE
R90	SRC175_	0.2466E-04
R56	SRC137_	0.1142E-04
R58	SRC139_	0.4254E-05
C55	SRC030_	0.1072E-05
R301	SRC111_	0.5671E-07
R68	SRC150_	0.5188E-07
R83	SRC167_	0.2315E-07
R51	SRC132_	0.1555E-07
R47	SRC128_	0.1463E-07
R300	SRC110_	0.1188E-07
R89	SRC173_	0.1174E-07
R42	SRC123_	0.1145E-07
R91	SRC176_	0.9406E-08
R46	SRC127_	0.7665E-08
R45	SRC126_	0.6586E-08
R13	SRC092_	0.5328E-08
R97	SRC182_	0.3331E-08

Table J.1 (continued): Accumulated Fatigue Damage for the Electronic Components Mounted on the Power PCB

R63	SRC145_	0.1910E-08
C90	SRC061_	0.1305E-08
R18	SRC097_	0.1305E-08
C80	SRC051_	0.1220E-08
R80	SRC164_	0.1106E-08
C91	SRC062_	0.9307E-09
R96	SRC181_	0.5176E-09
R94	SRC179_	0.4129E-09
R59	SRC140_	0.3681E-09
R61	SRC143_	0.2948E-09
R60	SRC142_	0.2779E-09
R54	SRC135_	0.2681E-09
R7	SRC152_	0.2602E-09
R86	SRC170_	0.2006E-09
R12	SRC091_	0.1970E-09
C89	SRC060_	0.1774E-09
R11	SRC090_	0.1362E-09
C83	SRC054_	0.1337E-09
R84	SRC168_	0.1191E-09
R9	SRC174_	0.1081E-09
R14	SRC093_	0.8584E-10
R6	SRC141_	0.8030E-10
R55	SRC136_	0.7407E-10
R85	SRC169_	0.5367E-10
R75	SRC158_	0.4408E-10
R10	SRC089_	0.3581E-10
C114	SRC015_	0.3187E-10
C109	SRC010_	0.2195E-10
R79	SRC162_	0.1757E-10
S3	SRC185_	0.1074E-10
R77	SRC160_	0.1047E-10
R95	SRC180_	0.9837E-11
R72	SRC155_	0.9733E-11
C54	SRC029_	0.8742E-11
R44	SRC125_	0.8179E-11
R87	SRC171_	0.6970E-11
R19	SRC098_	0.6132E-11
R43	SRC124_	0.4061E-11
R49	SRC130_	0.3884E-11
S2	SRC184_	0.3581E-11
R50	SRC131_	0.3549E-11
R88	SRC172_	0.3210E-11
R17	SRC096_	0.3067E-11
C108	SRC009_	0.2956E-11
R78	SRC161_	0.2254E-11
R92	SRC177_	0.1898E-11
C93	SRC064_	0.1862E-11
C107	SRC008_	0.1503E-11
S1	SRC183_	0.1459E-11
R48	SRC129_	0.1423E-11

Table J.1 (continued): Accumulated Fatigue Damage for the Electronic Components Mounted on the Power PCB

R64	SRC146_	0.1249E-11
R8	SRC163_	0.1132E-11
R57	SRC138_	0.9653E-12
R52	SRC133_	0.9264E-12
R67	SRC149_	0.7926E-12
C82	SRC053_	0.7364E-12
C87	SRC058_	0.4946E-12
C78	SRC049_	0.3789E-12
R74	SRC157_	0.2419E-12
C106	SRC007_	0.1027E-12
R15	SRC094_	0.9264E-13
R76	SRC159_	0.5607E-13
C77	SRC048_	0.4760E-13
C86	SRC057_	0.2907E-13
C74	SRC045_	0.2301E-13
C85	SRC056_	0.2264E-13
R20	SRC099_	0.2244E-13
R16	SRC095_	0.1943E-13
C75	SRC046_	0.1158E-13
C84	SRC055_	0.8958E-14
C81	SRC052_	0.8801E-14
C70	SRC041_	0.4291E-14
C56	SRC031_	0.4072E-14
C69	SRC040_	0.4002E-14
R73	SRC156_	0.2636E-14
C66	SRC037_	0.2423E-14
C112	SRC013_	0.9644E-15
C113	SRC014_	0.9157E-15
C79	SRC050_	0.8719E-15
C72	SRC043_	0.8544E-15
TK_EB2	SRC195_	0.5096E-15
C71	SRC042_	0.2679E-15
C111	SRC012_	0.1985E-15
C92	SRC063_	0.1850E-15
C57	SRC032_	0.1329E-15
C68	SRC039_	0.1230E-15
C76	SRC047_	0.1142E-15
C88	SRC059_	0.9125E-16
C67	SRC038_	0.6370E-16
TK_EB1	SRC194_	0.4932E-16
C73	SRC044_	0.4880E-16
C58	SRC033_	0.3336E-16
C53	SRC028_	0.1775E-16
R53	SRC134_	0.5305E-17
C110	SRC011_	0.4060E-17
R1	SRC088_	0.5379E-34
R93	SRC178_	0.1096E-34
R62	SRC144_	0.1670E-35

Table J.2: Life Usage distribution for the capacitor C-104

CAPACITOR C-104 ON THE POWER PCB (ACCUMULATED DAMAGE=1.9260E+02)			
TEST PCB	COMPONENT NAME	COMPONENT CAPABILITY	LIFE USAGE (%)
1	C113	3.9572E+05	0.049
2	C133	3.0458E+05	0.063
2	C132	2.9380E+05	0.066
1	C134	2.5608E+05	0.075
1	C123	2.3450E+05	0.082
2	C134	1.6351E+05	0.12
2	C123	1.5125E+05	0.13
1	C126	1.4575E+05	0.13
2	C114	9.0652E+04	0.21
2	C122	8.7418E+04	0.22
1	C105	5.9315E+04	0.33
1	C122	4.7993E+04	0.4
1	C132	3.0270E+04	0.64
2	C131	2.4802E+04	0.78
1	C131	6.8751E+03	2.8
2	C126	1.6129E+03	11.94
1	C112	5.0171E+02	38.4
1	C102	4.6107E+02	41.8
2	**C101**	**1.9107E+02**	**100.8**
2	**C111**	**6.7745E+00**	**2843**

Table J.3: Life Usage distribution for the capacitor C-63

CAPACITOR C-63 ON THE POWER PCB (ACCUMULATED DAMAGE=1.6030E+04)			
TEST PCB	COMPONENT NAME	COMPONENT CAPABILITY	LIFE USAGE (%)
2	C132	5.6064E+01	2.86E+04
2	C129	2.8677E+01	5.59E+04
2	C126	1.4809E+01	1.08E+05
2	C106	1.3537E+01	1.18E+05
3	C123	6.9558E+00	2.30E+05
3	C128	6.3610E+00	2.52E+05
3	C114	6.1415E+00	2.61E+05
1	C108	3.0913E+00	5.19E+05
3	C115	2.0422E+00	7.85E+05
3	C108	1.8921E+00	8.47E+05
1	C135	9.6888E-01	1.65E+06

Table J.3 (continued): Life Usage distribution for the capacitor C-63

CAPACITOR C-63 ON THE POWER PCB(ACC.DAMAGE=1.6030E+04)			
TEST PCB	COMPONENT NAME	COMPONENT CAPABILITY	LIFE USAGE (%)
3	C106	0.8961	1788862.9
2	C115	0.67383	2378938.31
3	C127	0.56091	2857855.98
2	C113	0.55986	2863215.8
1	C123	0.47397	3382070.6
2	C122	0.21147	7580271.43
2	C127	0.16646	9629941.13
3	C135	0.13719	11684525.11
3	C104	0.10181	15745015.22
1	C104	0.068693	23335711.06
2	C102	0.062913	25479630.6
1	C106	0.039239	40852213.36
1	C114	0.020968	76449828.31
2	C135	0.0088261	181620421.3
1	C115	0.0012005	1335276968
1	C111	0.0011175	1434451902
1	C102	0.000075009	21370768841

Table J.4: Life Usage distribution for the capacitor C-64

CAPACITOR C-64 ON THE POWER PCB (ACCUMULATED DAMAGE=6.2240E+03)			
TEST PCB	COMPONENT NAME	COMPONENT CAPABILITY	LIFE USAGE (%)
2	C132	5.6064E+01	1.11E+04
2	C129	2.8677E+01	2.17E+04
2	C126	1.4809E+01	4.20E+04
2	C106	1.3537E+01	4.60E+04
3	C123	6.9558E+00	8.95E+04
3	C128	6.3610E+00	9.78E+04
3	C114	6.1415E+00	1.01E+05
1	C108	3.0913E+00	2.01E+05
3	C115	2.0422E+00	3.05E+05
3	C108	1.8921E+00	3.29E+05
1	C135	9.6888E-01	6.42E+05
2	C131	9.6325E-01	6.46E+05
3	C106	8.9610E-01	6.95E+05

Table J.4 (continued): Life Usage distribution for the capacitor C-64

CAPACITOR C-64 ON THE POWER PCB (ACCUMULATED DAMAGE=6.2240E+03)			
TEST PCB	COMPONENT NAME	COMPONENT CAPABILITY	LIFE USAGE (%)
3	C127	0.56091	1109625.43
2	C113	0.55986	1111706.5
1	C123	0.47397	1313163.3
2	C122	0.21147	2943207
2	C127	0.16646	3739036.4
3	C135	0.13719	4536773.8
3	C104	0.10181	6113348.4
1	C104	0.068693	9060603
2	C102	0.062913	9893026.9
1	C106	0.039239	15861770.2
1	C114	0.020968	29683327
2	C135	0.0088261	70518122.4
1	C115	0.0012005	518450645.6
1	C111	0.0011175	556957494.4
1	C102	0.000075009	8297670946

Table J.5: Life Usage distribution for the capacitor C-65

CAPACITOR C-65 ON THE POWER PCB (**ACCUMULATED DAMAGE=7.6180E-02**)			
TEST PCB	COMPONENT NAME	COMPONENT CAPABILITY	LIFE USAGE (%)
2	C132	5.6064E+01	1.36E-01
2	C129	2.8677E+01	2.66E-01
2	C126	1.4809E+01	5.14E-01
2	C106	1.3537E+01	5.63E-01
3	C123	6.9558E+00	1.10E+00
3	C128	6.3610E+00	1.20E+00
3	C114	6.1415E+00	1.24E+00
1	C108	3.0913E+00	2.46E+00
3	C115	2.0422E+00	3.73E+00
3	C108	1.8921E+00	4.03E+00
1	C135	9.6888E-01	7.86E+00
2	C131	9.6325E-01	7.91E+00
3	C106	8.9610E-01	8.50E+00
2	C115	6.7383E-01	1.13E+01
3	C127	5.6091E-01	1.36E+01

Table J.5 (continued): Life Usage distribution for the capacitor C-65

CAPACITOR C-65 ON THE POWER PCB (**ACCUMULATED DAMAGE=7.6180E-02**)			
TEST PCB	COMPONENT NAME	COMPONENT CAPABILITY	LIFE USAGE (%)
1	C123	0.47397	16.07
2	C122	0.21147	36.02
2	C127	0.16646	45.76
3	C135	0.13719	55.53
3	**C104**	**0.10181**	**74.83**
1	**C104**	**0.068693**	**110.9**
2	**C102**	**0.062913**	**121.1**
1	**C106**	**0.039239**	**194.1**
1	**C114**	**0.020968**	**363.32**
2	**C135**	**0.0088261**	**863.12**
1	**C115**	**0.0012005**	**6345.69**
1	**C111**	**0.0011175**	**6817**
1	**C102**	**0.000075009**	**101561.15**