IMPLEMENTATION OF A DIGITAL SIGNAL SYNTHESIZER WITH HIGH SPURIOUS FREE DYNAMIC RANGE

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ABSTRACT

IMPLEMENTATION OF A DIGITAL SIGNAL SYNTHESIZER WITH HIGH SPURIOUS FREE DYNAMIC RANGE

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Today's analog modulators and upconverters are inadequate to synthesize and modulate signals with high 'Spurious Free Dynamic Range' (SFDR). Thus, the main objective of this thesis is to design and implement a 'Digital Signal Synthesizer' (DSS) that is capable of synthesizing signals between 50-100 MHz with 60dB SFDR and to modulate them variable symbol rates and modulation techniques with very high phase/frequency resolution and switching speed while keeping the amplitude modulation occurring during a modulated symbol duration as small as possible.

In this thesis, digital words of the desired signals are first synthesized in a 'Field Programmable Gate Array' (FPGA) using 'Direct Digital Synthesizer' (DDS) fundamentals and then converted to analog signals with a high speed 'Digital to Analog Converter' (DAC). In order to attain the analog requirements, the system variables such as DAC analog performance, nonlinearities, sample and hold affects, DDS parameters, system clock, bandwidth requirements of analog filters and how they effect the output performance are studied. FPGA blocks that are capable of

modulating and synthesizing desired signals are designed and programmed on a FPGA. Finally, single tone and modulated signals are synthesized with this DSS implementation and measured in order to verify this system's performance and capabilities.

Keywords: Digital Signal Synthesizer, Direct Digital Synthesizer, Digital to Analog Converter, Spurious Free Dynamic Range, AD9777, FPGA.

ÖZ

YÜKSEK PARAZİTSİZ DİNAMİK ALANLI SAYISAL SİNYAL SENTEZÖRÜNÜN GERÇEKLEMESİ

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Temmuz 2006, 112 Sayfa

Günümüzde analog modülatörler ve yükselteçler yüksek 'Parazitten Arınmış Dinamik Alanlı' (SFDR) sinyalleri sentezleyip, modüle etmekte yeterli olmamaktadır. Bu nedenle bu tezde 50-100MHz arasında bir frekansta 60dB dinamik alana sahip sinyal sentezleyebilen, bu sinyali değişken sembol hızlarında, yüksek faz/frekans çözünürlüğünde ve anahtarlama hızlarında değişik tekniklerle modüle edebilen, modüle edilmiş semboller süresince oluşabilecek genlik bozulmalarını en aza indiren bir sayısal sinyal üretecinin tasarımı ve gerçeklemesi açıklanmaktadır.

Bu tezde, sayısal kelimeler 'Dolaysız Sayısal Sentezleme' (DDS) teknolojisi temel alınarak 'Alanı Programlanabilen Geçit Dizilimleri' (FPGA) içinde üretilmiş ve bir yüksek hızlı 'Sayısal-Analog Dönüştürücü'(DAC) ile analog sinyallere dönüştürülmüştür. Analog performans gereksinimlerini karşılayabilmek amacıyla, DAC analog performansları, doğrusal olmayan bozunumları, örnekle ve tut etkileri, DDS parametreleri, sistem saat işaretinin etkileri, genlik bozulmaları için gerekli bant genişlikleri ve bunların sistem performansı üzerine etkileri incelenmiştir. Gereksinim duyulan

sinyalleri modüle edip sentezleyebilen FPGA blokları tasarlanış ve bir FPGA üzerinde uygulanmıştır. Son olarak bu sistemin performansını ve yeteneklerini doğrulamak için tek ton ve modüle edilmiş sinyaller sentezlenip ölçümleri yapılmıştır.

Anahtar Kelimeler: Sayısal Sinyal Sentezörü, Dolaysız Sayısal Sentezleyiciler, Sayısal-Analog Dönüştürücüler, Parazitten Arınmış Dinamik Alan, AD9777, FPGA.

Dedicated to My Parents and to My Brother

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I want to express sincere thanks to my supervisor, Asst. Prof. Dr. Ali Özgür YILMAZ for his guidance, insight, and patience throughout this study. I shall also state my deepest appreciation and admiration about his exceptional brilliance and enthusiasm.

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SYMBOLS

f_{CLK}	Clock frequency
f_{out}	Output frequency
V_{PP}	Voltage peak to peak
$x_{lp}(t)$	Baseband signal
$x(t)$	Passband signal
$X_{lp}(f)$	Fourier transform of $x_{lp}(t)$
$X(f)$	Fourier transform of $x(t)$
$a_I(t)$	Inphase component
$a_Q(t)$	Quadrature component
$a(t)$	Amplitude function
$\theta(t)$	Phase function
f_C	Carrier frequency
$\delta(n)$	Impulse function
$X_{SH}(t)$	Signal after sample and hold
$X_{SH}(f)$	Fourier transform of $X_{SH}(t)$
q	Weight of the least significant bit in digital word
$e(t)$	Error function

f_S	Sampling frequency
f_O	Output frequency
f_P	Frequency of periodicity
$v(t)$	Full scale output
$X_P[k]$	Fourier series coefficients
A_C	Amplitude
θ	Phase
B	Boltzmann constant
I	Inphase codes
Q	Quadrature codes

LIST OF ABBREVIATIONS

ABBREVIATIONS

AC	Alternating Current
ACPR	Adjacent Channel Power Ratio
AM	Amplitude Modulation
CDMA	Code Division Multiple Access
CPM	Continuous Phase Modulation
cos	Cosine
DAC	Digital to Analog Converter
DDS	Direct Digital Synthesizer
DSS	Digital Signal Synthesizer
EB	Evaluation Board
EMI	Electro Magnetic Interference
FM	Frequency Modulation
FPGA	Field Programmable Gate Array
ISE	Integrated Software Environment
LSB	Least Significant Bit
LUT	Look Up Table
LVTTL	Low Voltage Transistor Transistor Logic
MSB	Most Significant Bit
MSK	Minimum Shift Keying
PLL	Phase Locked Loop
PM	Phase Modulation
RAM	Read Access Memory
rect	Rectangular function
rms	Root Mean Square
QPSK	Quadrature Phase Shift Keying

SFDR	Spurious Free Dynamic Range
sin	Sine
sinc	Function of sin(x)/x
SNR	Signal to Noise Ratio
THD	Total Harmonic Distortion
THDN	Total Harmonic Distortion plus Noise
VHDL	Very High scale integrated circuit Description Language

CHAPTER 1

INTRODUCTION

The general aim of this thesis is the analysis and implementation of a 'Digital Signal Synthesizer' (DSS) that is capable of synthesizing signals between 50-100 MHz with 60dB 'Spurious Free Dynamic Range' SFDR. This DSS is expected to adapt to different modulation techniques, have very high phase/frequency resolution and switching speed, be flexible to adapt to different symbol rates, be externally controllable, and create as small amplitude modulation as much as possible.

Analog synthesizers and modulators are inadequate to meet requirements of such a complicated synthesizer since usually carrier signals and other harmonics of the carrier signal couple to the output of the analog synthesizers and modulators deteriorating the SFDR performance of the output signal. Besides, these analog components have limited modulating capabilities with very low phase and frequency resolution at very low switching speeds. Finally it is impossible to shift between different modulations and control the system parameters like modulation rate, hopping speed, carrier frequency without making any hardware modification.

The basic principles of digital synthesizers which are very popular in today's architectures were introduced in [1]. The architecture of a basic digital synthesizer consists of a digital block producing digital samples characterizing the desired analog signal, a 'Digital to Analog Converter' (DAC) and an analog filter as seen in Figure 1.1.

Figure 1.1 Main Blocks of a Digital Signal Synthesizer

There are various digital synthesizer implementations built over these principles in the literature. These synthesizers are mostly integrated circuit (IC) solutions integrating a direct digital synthesizer (DDS) and a DAC inside a chip. DDS is the method of producing digital words of a discrete sinusoidal signal. These IC solutions can be separated into three groups from the point of view of the desired synthesizer in this thesis. In the first group, synthesizers that are operating at relatively low sampling frequencies such as [2-6] are present. The sampling frequencies of these synthesizers can not even get closer to the sampling rates that are going to be desired in our system to produce 50-100MHz signal. The second group [7-8] consists of high speed synthesizers. However these synthesizers do not meet our 60dB SFDR requirement. Finally the last group [9-10] consists of high speed and high SFDR synthesizers. Even though these synthesizers have modulation capabilities, these systems lack controllability and flexibility to control all parameters of a DDS plus DAC system and thus limits designers within the capabilities of these ICs.

Today's transmitter systems are expected to be controllable in a wide range of frequencies, flexible enough to change signal processing chains rapidly, and support very high data rates. To serve this purpose, we decided to use a Field Programmable Gate Array (FPGA) and integrate it with a high speed DAC in this thesis. FPGAs enable designer to service multiple communication standards,

implement very important signal processing blocks such as filters, and control each block easily at high frequencies. DDS, modulator, control and signal processing blocks can be implemented on a FPGA.

The implementation of the desired synthesizer introduces a non-trivial design problem. Firstly, such a system requires integration of complex digital blocks that are capable of controlling the system, interfacing with the outer digital world, and processing signals. Secondly, 60dB SFDR requirement for a frequency range of 50-100MHz is also a challenging problem since producing signals at these frequencies requires high sampling frequencies. At these high frequencies high speed DACs create harmonic signals and distort the output performance. On the other hand, the sampling frequency defines where the harmonics and images due to sampling are placed in the signal spectrum. These unwanted signals are highly related to the bandwidth and dynamic range of the output. Hence, the choices for the DAC and the sampling rate are very critical for the desired synthesizer.

Moreover, it is mentioned that amplitude modulation (AM) should be kept at a minimum. This amplitude modulation is related to the band limitation effect of the analog filter seen in Figure 1.1. Such an AM is undesired since AM is converted to a phase modulation by some non-linear amplifiers which are usually present in transmitters of interest in this work. In order to create small AM., all system parameters such as DDS parameters, DAC parameters, and filter parameters must be considered altogether to widen the filter band while holding the SFDR level at 60dB.

Finally, design of mixed signal systems (systems in which digital and analog signals are mixed) is another problem since coupling of digital

circuits distorts the clarity of the analog outputs and consequently degrades the SFDR performance. Therefore in this thesis, solutions for these problems are investigated and a digital signal synthesizer is designed and implemented.

Since the problem is a design problem, a thorough understanding of the DDS and DAC architectures and analog filter characteristics are very important. Therefore, architectures and parameters of DDS, DAC, and analog filters are explored in Chapter 2. In Chapter 3 the effects of these parameters and other parameters such as the system clock over the output signal are assessed.

In Chapter 4, digital systems that are designed to be utilized on FPGAs which can control, modulate, and synthesize signals are explained. The phase/frequency switching times and angle resolution of these digital systems are discussed.

In Chapter 5, the DSS implementation is explained. The comparison and evaluation of high speed DACs in the market are discussed with respect to the parameters mentioned in Chapter 3. The FPGA board used in the system is introduced. Moreover, important points about system implementation are mentioned.

Chapter 6 is devoted to the verification of the system. In order to test the board, a QPSK modulator is utilized on the FPGA. As an example, a QPSK modulated signal at 67.5MHz signal is synthesized and examined in this chapter. The outputs of this system are investigated and compared with theoretical expectations. Moreover, how AM level is affected according to the amount of energy filtered by the analog filter is inspected.

CHAPTER 2

BACKGROUND

2.1 FUNDAMENTALS OF DDS

Simply, DDS is a digital block which outputs samples of a sinusoidal signal. DDS architecture consists of a memory and a counter for that memory. Each time the clock triggers the counter points to the next address of the memory to form a continuous pattern of a sinusoidal as seen in Figure 2.1.

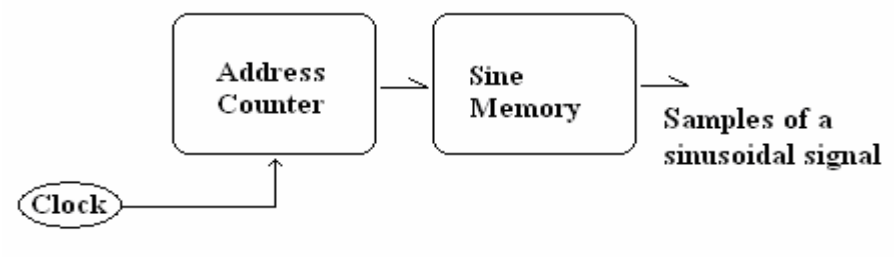


Figure 2.1 Block diagram of a simple DDS model

This simplistic model lacks of frequency tuning flexibility. There are two ways of changing output frequency in this model. Either the frequency of input clock should be changed or the contents of the memory should be changed which are both very impractical.

In order to overcome this problem, phase accumulator is introduced to the DDS architecture [11]. The phase accumulator is an interface

to change output frequency while keeping the same input clock. Basically, phase accumulator adjusts the steps of the counter pointing to the memory in order to tune the output frequency. The step size is called the 'Tuning Word'. The latter DDS architecture is as seen on Figure 2.2.

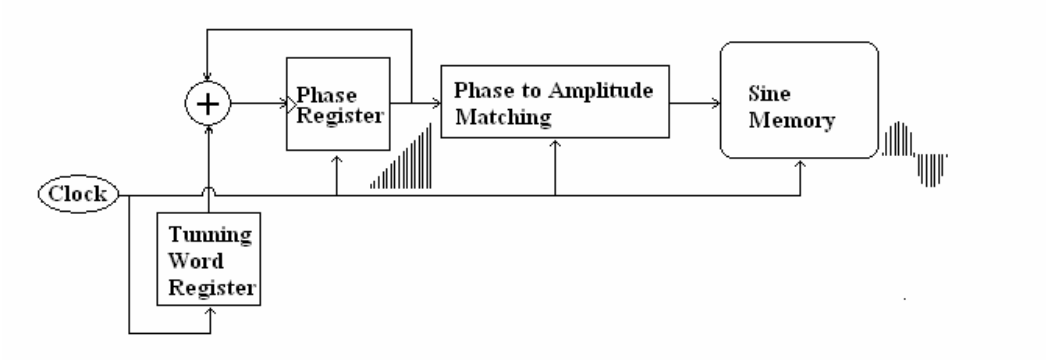


Figure 2.2 DDS architecture employing phase accumulator

The number of samples for one cycle of a sinusoidal is determined by the number of address bits in the memory. If the number of address bits of a memory is 'N', then there are 2^N samples of a sinusoidal. This number of address bits identifies the depth of the memory.

Assuming N is five, and tuning word is one then a complete cycle of a sinusoidal stored in the memory will be completed in 32 clock cycles, resulting in a output signal period of 32 times the clock period. To generalize, the frequency of the output signal has a relation with the clock frequency and the memory depth as

$$f_{out} = \frac{M * f_{clock}}{2^N}, \qquad (2.1)$$

where M denotes the tuning word. The phase accumulator mainly adjusts the jump size of the counter according to the tuning word. Steps taken by the counter are equal to each other, however since sinusoidal functions are not linear functions, phase wheel functions are introduced. If the beginning of one cycle of a sinusoidal is taken as phase zero, the end of the cycle is denoted as phase $2*\pi$. This results in correspondence of each point of a sinusoidal to a phase. As counter increases linearly with equal step sizes, the phase equivalent of the sinusoidal signal also increases linearly and phase to amplitude converter tries to estimate the amplitude value of that angle [12]. Since counter has a limited number of bits, when the limits of this digital word is reached, the counter turns back to the beginning of the memory completing one full phase cycle. This one complete phase cycle is called a phase wheel [11].

The number of points on the phase wheel is determined by the depth of the memory. Besides, the size of the jump on the phase wheel is determined by the tuning word. The bigger the memory depth, the higher the phase resolution of the sinusoidal memory is. Number of points presented in Figure 2.3 could be thought as the number of points dividing $2*\pi$.

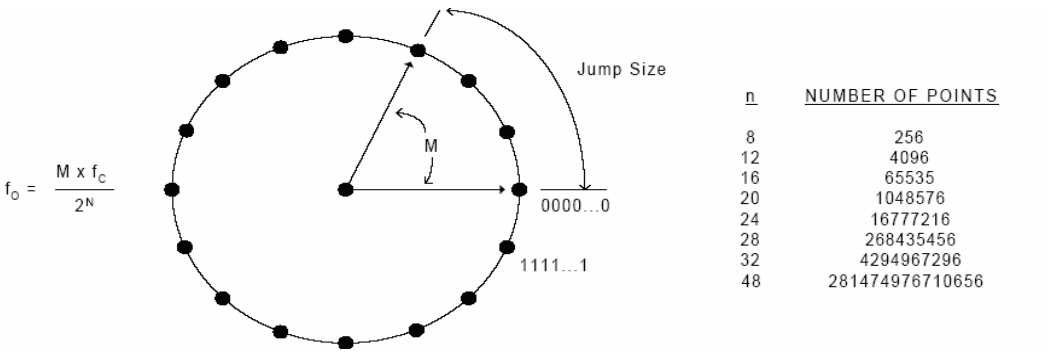


Figure 2.3 Digital Phase Wheel [11]

Although the depth of the memory is an important factor for the phase resolution, the width of the memory is another parameter affecting phase resolution. The width of the memory is the number of bits stored in the memory for each sample. The number of bits stored for each sample is also an identifier for the number of quantized levels dividing the normalized amplitude of a sinusoidal. Indeed the difference between two consecutive quantized levels is the amplitude resolution of the samples of a sinusoidal signal and it is determined by width of the memory and DAC input resolution.

At this point, it is important to emphasize that the smallest of the depth and width of the memory is the limiting factor for phase resolution. Usually phase resolution is kept high and amplitude resolution is kept low so that the size of the memory could be kept under a certain design level. Conversion between resolution levels of phase accumulator and memory takes place in between the phase accumulator and the memory blocks of DDS as seen in Figure 2.4.

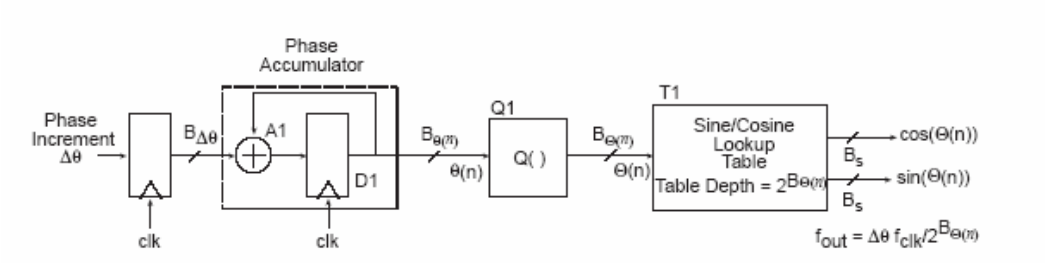


Figure 2.4 Phase Truncation DDS [13]

Finally in order to convert digital words to analog signals like voltage or current, Digital to Analog Converters follows Direct Digital Synthesizers which are going to be explained in next section.

2.2 FUNDAMENTALS OF DAC

DACs are mixed signal components transforming digital words to analog counterparts such as voltage or current. DAC inner structure consists of converter and sample-hold blocks. Converter blocks are composed of R-C circuitry which is used to convert each digital word to an analog signal like current or voltage. The outputs of these R-C circuits can not be controlled regularly because of capacitive coupling of digital transitions and the effects of some switches in the DAC operating quicker than others [14]. In order to stabilize the outputs these R-C circuits are followed by sample and hold circuits. Sample and hold circuits are used to hold the previous analog signal at the output until next analog output stabilizes as seen in Figure 2.5.

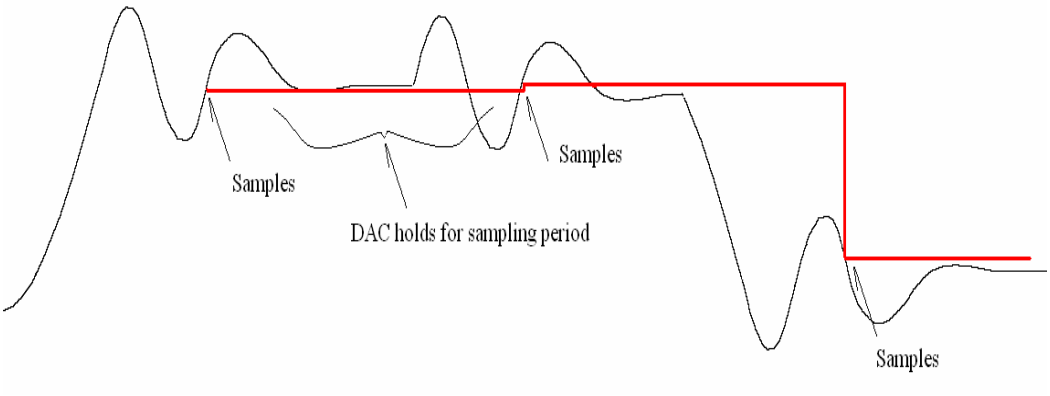


Figure 2.5 Realization of Sample and Hold function

DAC are grouped mostly according to their resolution and sampling rate. These two parameters designate the border of the group of DAC that are suitable for a specific system.

In addition to the aforementioned parameters, each DAC in the market also have important specific performance characteristics. These characteristics are mainly shaped with DAC inner blocks that can not be controlled regularly and result in nonlinear transfer characteristics. These characteristics could be grouped as DAC DC and AC performance specifications.

The DC performance specifications of DACs are

- Offset error
- Gain error
- Integral linearity error
- Differential linearity error

Whereas, AC performance specifications of DACs are

- Output settling time
- Glitch impulse area
- Distortions and Spurious Free Dynamic Range
- Signal to Noise Ratio

The detailed requirements of a system play a key role in determining the suitable DAC for the system. In order to find a suitable DAC for the system, a careful understanding of these specifications is needed. For our case, since we have a SFDR criterion, mostly AC performance of DAC will be considered. Besides most of the DAC in the market today have almost similar DC performance characteristics, but differentiate according to their AC performance characteristics.

Now, in the following sections these characteristics will be explained to come with a better understanding of DAC in order to appreciate the DAC selection procedure that will be explained in Chapter 5.

2.2.1 Parameters of DAC

The number of input bits determines the amplitude resolution and consequently quantization noise floor at the output of a DAC [14]. The number of input bits of a DAC, similar to DDS memory depth, defines the number of steps the analog output is divided into. If a DAC has 12 input bits and 1 V_{pp} output full voltage range, then there are 2^{12} steps dividing $1V_{pp}$. Therefore for the DAC mentioned, the resolution of the DAC could be taken as 0.244 mV. Since the real analog output is quantized to these steps, noise arises according to the misrepresentation which is called quantization noise [15].

Secondly, the update rate which is the limiting factor for the sampling frequency of a digital synthesizer is the second important parameter of a DAC. In other words, DAC update rate is the number of samples a DAC can convert to analog signal in one second.

According to sampling theorem [16], a real signal, for example a sinusoidal with a center frequency f_O and sampled with a sampling frequency f_S has imaginary and real parts shifted as much as Kf_S in the spectrum where K is 1, 2, 3, 4.... The resulting spectra will have signals placed at $|\pm Kf_S \pm f_O|$ as seen in Figure 2.6. These signals are called aliases or images of the original signal.

Moreover, Nyquist Theorem states that a signal which has frequency components between f_a and f_b must be sampled at a rate $f_s \geq 2(f_b - f_a)$ in order to prevent alias components from interfering to the main signal [16].

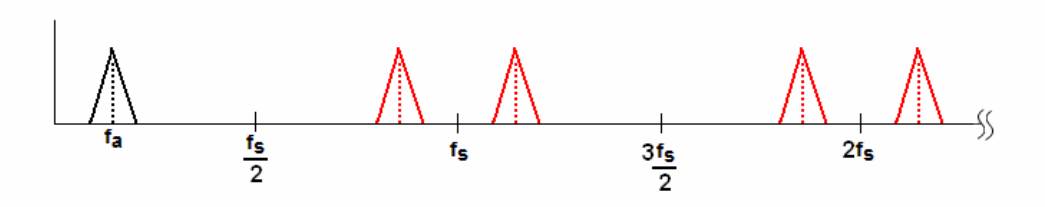


Figure 2.6 A sampled signal

Thus the sampling frequency, bandwidth and carrier frequency of a modulated signal are highly related with each other and in order to avoid aliasing a careful analysis is needed. At this point, the update rate of DAC is a very critical parameter in a system design. A detailed mathematical analysis of sampling, aliases and power spectrum of output signal will be done in Chapter (2.4).

2.2.2 Characteristics of DAC

2.2.2.1 DC Specifications

DC specifications of DAC are mostly related with the transfer function of DAC. Simply the transfer function of a DAC could be characterized with the formula:

$$A = G(D).D + O \tag{2.2}$$

where D is the digital input, A is analog output, O is offset and $G(x)$ is nonlinear gain function.

Gain error, integral linearity error and differential nonlinearity error are consequences of nonlinear transfer functions of DAC. Simply the

deviation of the gain function from the ideal linear gain function is called the gain error. The deviation of actual transfer function from the linear transfer function is called the integral linearity error. Finally for one bit increase in the digital word, a constant increase is expected at the analog output. The deviation from this constant analog increase for each smallest increase in the digital word is called the differential linearity error. Moreover, the constant shift in the amplitude of the output of the DAC is called offset error.

Most of the DAC show similar DC performance characteristics. However, the SFDR performances of different DAC do not show that much similarity. Besides, since AC characteristics of DAC are rather important for our case, AC characteristics of DAC are analyzed in a more detailed way.

2.2.2.2 AC Specifications

2.2.2.2.1 Output Settling Time and Glitch

The output settling time is defined as the time for analog output of the DAC to remain in some error band after digital word is latched. There are four regions of settling time. These regions are dead time, slew time, recovery time and linear settling time which are shown in Figure 2.7. Dead time is the period for the digital input switching. Slew time is the increase or decrease time to the desired output. Recovery time is the recovery time of the output from fast slew and overshoot. Finally linear settling time is the time for DAC to approximate its output in an exponential or near exponential manner.

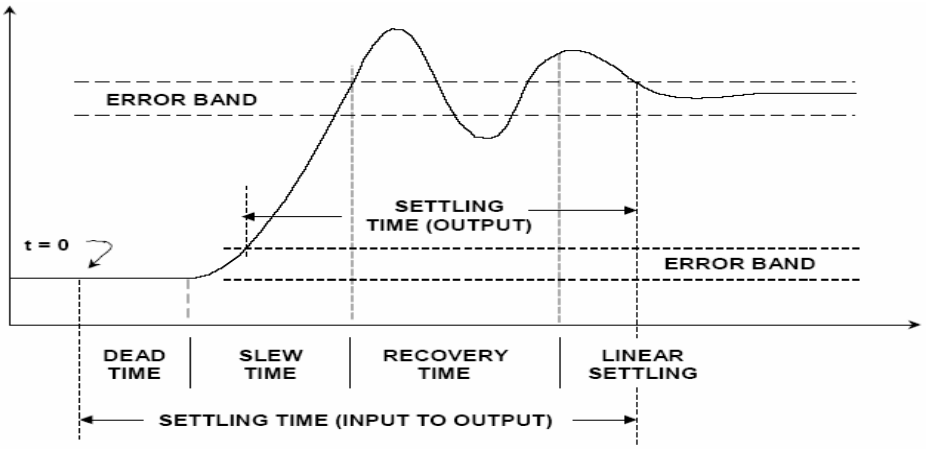


Figure 2.7 DAC settling time [14]

The overshoot of analog output as seen in Figure 2.7 is called the glitch. Main reasons of glitches are capacitive coupling of digital to analog transitions and unsynchronized converter switches [14]. The largest of the negative or positive glitch areas is called peak glitch area.

2.2.2.2.2 Distortions and Spurious Free Dynamic Range

Transfer functions of data converters are not linear functions as transfer functions of linear devices such as op-amps. These nonlinearities produce distortions that could be observed in the spectrum of analog output. The most important causes of these distortions are

1) Resolution,
2) Integral non-linearity,
3) Differential non-linearity,
4) Code dependent glitches,
5) Ratio of sampling frequency to output frequency.

These distortions called the harmonic distortions can be observed at various points in spectrum. Some of these harmonics are located at frequencies equal to $|\pm K.f_S \pm n.f_O|$ [17], where n is the harmonic order and K is the multiples of sampling frequency as seen in Figure 2.8. Mostly second or the third harmonic is the strongest harmonic which may degrade a DAC's performance the most. The harmonics are measured relatively to the carrier frequency. Therefore they are usually specified with dBc (decibels below carrier).

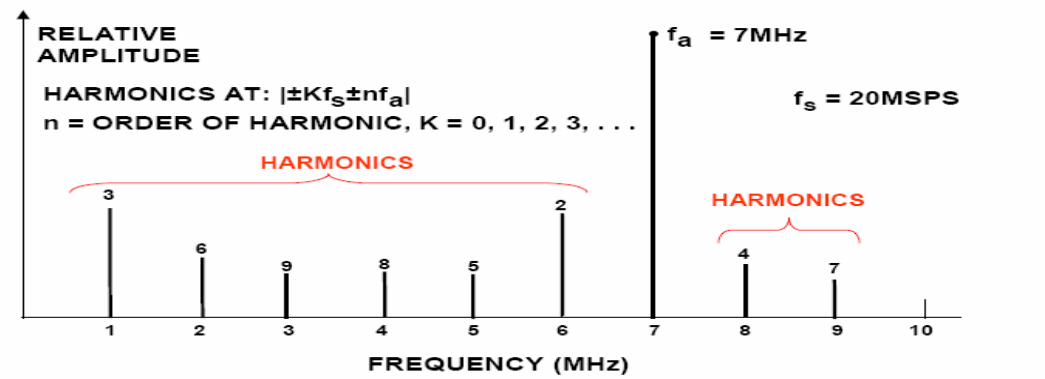


Figure 2.8 Locations of harmonics. Output signal is centered at 7MHz and sampling rate is 20MHz [14]

The ratio of the root-mean-square (rms) of the fundamental signal to the rms of its harmonics (generally, only the first five of the harmonics are significant) is called the total harmonic distortion (THD) and the ratio of the rms of the fundamental signal to the rms of the harmonics plus noise inside the signal's band is called total harmonic distortion plus noise (THDN). Moreover, spurious free dynamic range (SFDR) is the ratio of the carrier signal to the worst spurious signal in a defined band. Mostly Nyquist Band is taken as reference to measure SFDR.

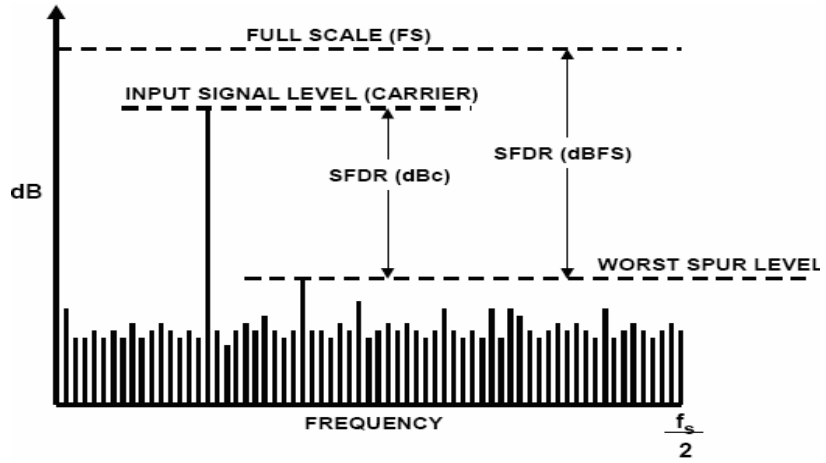


Figure 2.9 Spurious Free Dynamic Range [14]

The total glitch area or nonlinearity measurements of DAC are not sufficient to calculate possible frequencies of spurs since there are infinite number of combinations. Therefore, manufacturers mostly define test vectors to inform the customer about SFDR performance of DAC. A test vector is a combination of amplitudes, output frequencies, and update rates covering the sampling limits of DAC as seen in Figure 2.10.

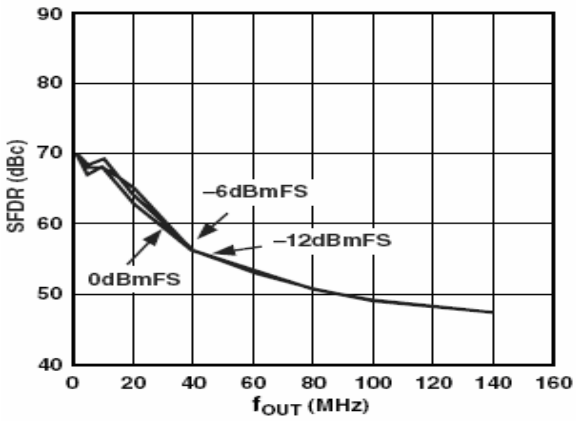


Figure 2.10 SFDR measurements of the DAC AD9755 [18]

Besides, in some DAC datasheets, specifications like adjacent channel power ratio (ACPR) and adjacent channel leakage ratio are defined. These specifications are useful mostly for the systems that are using multi frequency channels like CDMA channels. The ratio of the measured power within a channel to the measured power within its adjacent channel is defined as ACPR.

2.2.2.2.3 Signal to Noise Ratio

Beyond the quantization noise, there is another noise source which is called resistor noise that is additive to the total output noise level. Resistor noise is the noise coupled by the circuit components, board grounding and fast transition buses surrounding the DAC. The power of the resistor noise could be calculated as:

Resistor Noise Power: $4kTRB$ (2.3)

where k is Boltzman constant, T is temperature in Kelvin and B is the bandwidth of the output signal. Signal to Noise ratio (SNR) is the ratio of the rms power of output signal to the power of the noise inside the band of the signal. The bandwidth of the signal and its filtering is extremely important in determining SNR value of a DAC output.

2.3 ANALOG FILTERS IN DIGITAL SYNTHESIZERS

As mentioned previously, because of sampling and nonlinearities of DAC, image and harmonic signals appears in the spectrum of the analog output. These signals may interfere with the band of the fundamental signal. In other words, since DAC basically produce a staircase realization of the desired analog signal, there are sharp transitions in the signal observed in time domain. These sharp

transitions produce higher frequency components of the signal in the spectrum. Therefore, in order to remove aliased images and to smooth the output signal, lowpass or bandpass filtering is required.

Also analog filters have important parameters like passband width, stopband width, stopband attenuation, transition band, group delay, and passband amplitude response that are critical for digital signal synthesizers. These parameters and their effects will be explored in Chapter 3.

2.4 MATHEMATICAL BACKGROUND

The flowchart for generation of a modulated signal is provided in Figure 2.11. In this section, the mathematical representation of each output signal after each block would be derived. For the sake of consistency, all of the derivations are taken from [16].

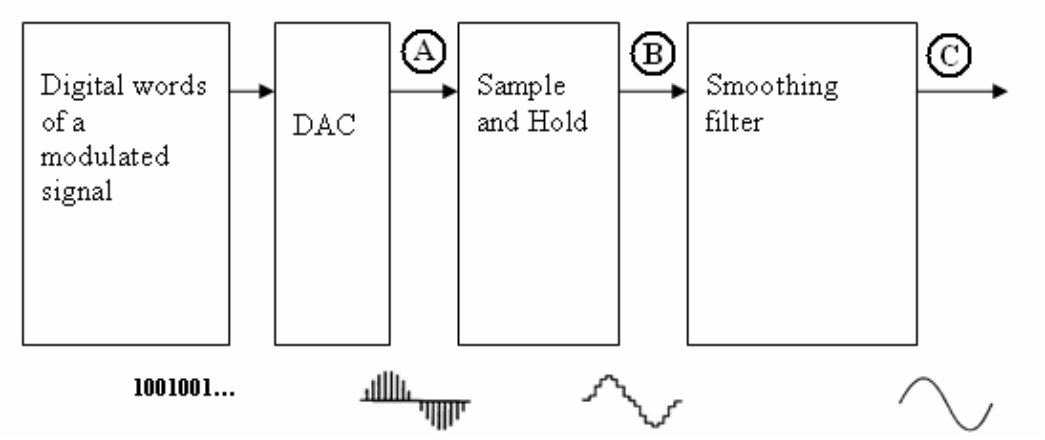


Figure 2.11 Functional blocks of a DSS

Firstly let us show the mathematical representation of a real bandpass signal *x(t),* in terms of a base band signal $x_{lp}(t)$.

$$x_{lp}(t) = a_I(t) + ja_Q(t) \tag{2.4}$$

$$x_{lp}(t) = a(t)e^{j\theta(t)} \tag{2.5}$$

where $a(t) = \sqrt{a_I(t)^2 + ja_Q(t)^2}$, $\theta(t) = \tan^{-1}\dfrac{a_Q(t)}{a_I(t)}$

$$x(t) = \mathrm{Re}(x_{lp}(t)e^{j2\pi f_c t}) \tag{2.6}$$

where f_c *is* center frequency of the bandpass signal.

$$x(t) = \left[x_{lp}(t)e^{j2\pi f_c t} + x_{lp}^{*}(t)e^{-j2\pi f_c t}\right]/2 \tag{2.7}$$

In frequency domain,

$$X(f) = \frac{1}{2}\left[X_{lp}(f - f_c) + X_{lp}^{*}(-f - f_c)\right] \tag{2.8}$$

where *X(f)* is Fourier transform of *x(t)* and $X_{lp}(f)$ is Fourier transform of $x_{lp}(t)$.

Now let us leave the representation of the signal in terms of a baseband signal for a while and analyze the effect of the blocks on the signal *x(t)* and *X(f).* In time domain, the signal is discrete at step A in Figure 2.11 and can be represented as:

$$x_s(n) = \sum_k x(kT)\delta(n - kT) \tag{2.9}$$

where T is the sampling period

The sample and hold function is used to avoid glitches of digital to analog converters. It could be represented as the convolution of a rectangular function with the signal. So, at step B

$$x_{SH}(t) = \sum_k x(kT)\delta(n - kT) * rect\ (\frac{t}{T}) \tag{2.10}$$

$$x_{SH}(t) = \sum_k x(kT)rect\ (\frac{t - kT}{T}) . \tag{2.11}$$

Finally, the signal should be filtered with a low pass filter to avoid images and to smooth the signal so the output of the signal at step C could be ideally represented as,

$$x_{LP}(t) = \sum_k x(kT)rect\ (\frac{t - kT}{T}) * \frac{1}{T} sinc\ (\frac{t}{T}) \quad . \tag{2.12}$$

In time domain the discrete signal is represented by summation of pulses. The representation of this summation of pulses in frequency domain is as follows,

$$\sum_k \delta(t - kT) \xrightarrow{F} \frac{1}{T} \sum_{m=-\infty}^{\infty} \delta(f - mf_s) \tag{2.13}$$

where f_s is sampling frequency.

The signal at A could be represented as follows

$$x_s(n) = \sum_k x(kT)\delta(n - kT) \xrightarrow{F}$$
$$X_s(f) = \frac{1}{T} \sum_{m=-\infty}^{\infty} X(f - mf_s) . \tag{2.14}$$

The effect of the sample and hold operation in the frequency domain is multiplication of the folded spectrum with a sinc function.

The signal at B is

$$X_{SH}(f) = \frac{1}{T}\sum_{m=-\infty}^{\infty} X(f - mf_S) \,.\, Tsinc\left(\frac{f}{fs}\right) \tag{2.15}$$

$$X_{SH}(f) = \sum_{m=-\infty}^{\infty} X(f - mf_S)\, sinc\left(\frac{f}{fs}\right) . \tag{2.16}$$

After that, the signal will be lowpass filtered, possibly by multiplying with a rect function in frequency domain. At C we have

$$X_{LP}(f) = \sum_{m=-\infty}^{\infty} X(f - mf_S)\, sinc\left(\frac{f}{fs}\right) rect\left(\frac{f}{f_S}\right) . \tag{2.17}$$

If we replace *X(f)* with its baseband representation

$$X(f) = \frac{1}{2}\left[X_{lp}(f - f_c) + X_{lp}^{*}(-f - f_c)\right] \tag{2.18}$$

$$X_{LP}(f) = \frac{1}{2}\sum_{m=-\infty}^{\infty}[X_{lp}(f - f_c - mf_s) + X_{lp}^{*}(-f - f_c + mf_s)]$$

$$sinc\left(\frac{f_s}{fs}\right) rect\left(\frac{f}{f_S}\right) \tag{2.19}$$

Using MATLAB, $X_{SH}(f)$ is plotted in Figure 2.12. $X_{lp}(f)$ is chosen as a baseband rectangular function so that the image and the sinc effect could be easily observed.

In Figure 2.12, the first rectangular region seen on the left is the upconverted lowpass signal. The second approximate rectangular portion is the image of this upconverted signal at frequency $(-f_c + f_S)$. The reason of the approximately triangular decay on these spectral plots is the sinc effect.

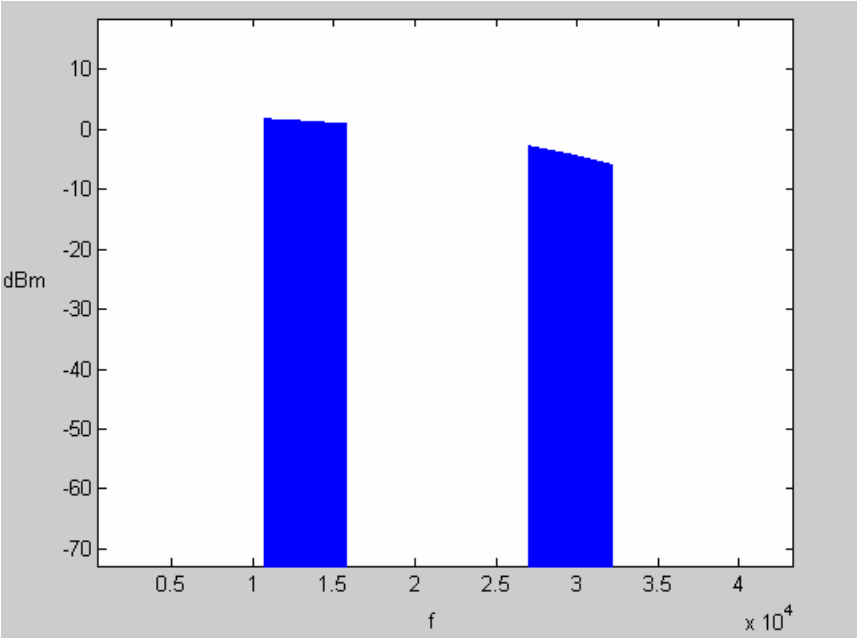


Figure 2.12 Theoretically expected spectrum. The signal is centered at 13kHz whereas the sampling frequency is 42 kHz

The last equation, eqn. 2.19, clearly shows the images placed just after half the sampling frequency which is also seen in Figure 2.12. The higher the sampling frequency is, the further away the image signal will be placed from the original signal.

CHAPTER 3

ASSESSMENT OF CRITICAL PARAMETERS

3.1 GENERAL

In Chapter 2 parameters of DSS blocks are explained. However, effects of these blocks over the analog output performance will be explained in this chapter.

The spectrum of the digital signal synthesizers' output consists of various spurs and images located at various frequencies. It is very complicated to investigate reasons for these spurs; however the analysis of synthesizer blocks will give a hint about most of them. Therefore the parameters of these three blocks will be considered as system parameters and relations of those that are critically affecting the output will be analyzed in this chapter.

Considering a complete DSS system, the spurious content of the analog output is affected by

1) DAC input resolution
2) Clock frequency and over sampling
3) DDS lookup table width and depth (Consequently the phase truncation.)
4) Harmonics caused by nonlinearities of DAC
5) Jitter and phase noise of system clock
6) Sin(x)/x effect of DAC
7) Filter characteristics.

These effects are critical for a DSS system and will be analyzed in detail.

3.2 ANALYSIS OF SYSTEM PARAMETERS

3.2.1 DAC Input Resolution

The quantization noise which is defined in Chapter 2 is determined by the DAC input resolution. For a system which has a resolution of q, the rms quantization noise inside the Nyquist Band for any AC signal can be approximated as:

$$\text{rms quantization noise} = \sqrt{\overline{e^2(t)}} = \frac{q}{\sqrt{12}} \qquad (3.1)$$

where *e(t)* is the mean square value of the error function. This noise is Gaussian and spread over Nyquist Band, under the assumption that noise is uncorrelated to the input signal. However, if the sampling clock's frequency is a multiple of the signal frequency, then this quantization noise is concentrated at the harmonics of the signal and its rms power is still $q/\sqrt{12}$ [14].

Moreover, SNR of a digitally produced sinusoidal signal can be calculated with the rms value of the signal and the rms value of the quantization noise inside the Nyquist Band. If the sinusoidal signal is taken as

$$v(t) = \frac{q.2^N}{2}\sin(2.\pi.f_O.t) \qquad (3.2)$$

where N is the number of input bits, then rms of this signal is

$$rms(v(t)) = \frac{q.2^N}{2\sqrt{2}} \tag{3.3}$$

So, SNR can be calculated as using the rms quantization noise value given in eqn 3.1

$$\text{SNR} = 20\log_{10}\left[\frac{\frac{q.2^N}{2\sqrt{2}}}{\frac{q}{\sqrt{12}}}\right] , \tag{3.4}$$

resulting in

$$\text{SNR} = 6.02.\text{N} + 1.76 \text{ dB} . \tag{3.5}$$

It is important to emphasize that the SNR value calculated above is for the noise measured in the whole Nyquist Band. If a filter is used, noise in the band of the filter should be considered in SNR calculations. Obviously, the noise in the band of the filter will be smaller than the whole noise distributed in the Nyquist Band as seen in Figure 3.1. This reduction in noise will bring a processing gain to the output which is

$$\text{SNR} = 6.02.\text{N} + 1.76 \text{ dB} + 10\log_{10}\left[\frac{f_S/2}{BW}\right] \tag{3.6}$$

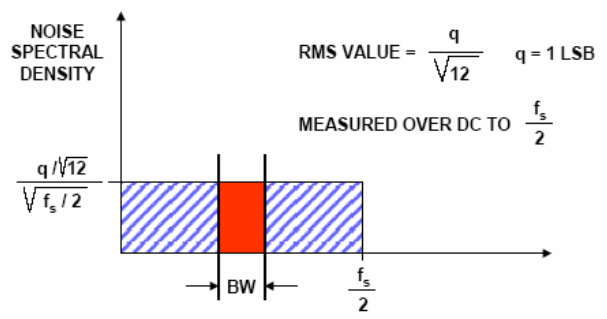


Figure 3.1 Quantization noise spectrum [14]

Although this mathematical model is an approximation for Bennett's work [19], this model holds for many systems.

3.2.2 Clock Frequency and Over Sampling

The quantization noise mentioned in previous section is inversely proportional to the number of input bits. Therefore using the same DAC at different clock frequencies will not change total rms value of quantization noise.

However, if the same DAC is used in different sampling frequencies and the output noise is filtered with similar filters then oversampling brings a gain to the SNR calculations.

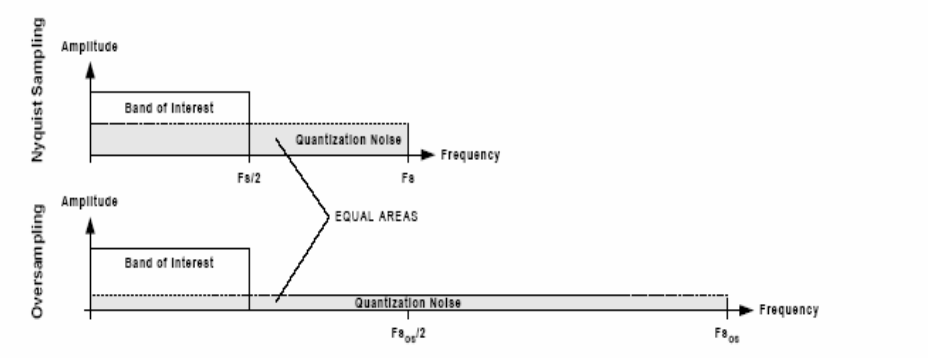


Figure 3.2 The effect of oversampling on SNR [15]

As seen in Figure 3.2, the higher the sampling clock frequency is, the wider the band the fixed amount of quantization noise is distributed into. Therefore average amount of noise per unit band decreases. This result in less amount of noise measured in the filtered band which means a higher SNR.
The gain caused by over sampling is

$$\text{SNR} = 6.02.\text{N} + 1.76\ \text{dB} + 10\log_{10}\left[\frac{f_s/2}{BW}\right] + 10\log_{10}\left[\frac{f_{oversampling}}{f_s}\right] \quad (3.7)$$

At this point, it is important to mention measurement errors that may be caused by digital spectrum analyzers. These analyzers filter a portion of the spectrum of a signal and plot it. The amount of band that is filtered and plotted each time is called the resolution bandwidth. As seen in eqn. 3.7 if the measurement bandwidth is smaller than the Nyquist Band, SNR increases. Similarly since resolution bandwidth is much smaller than Nyquist Bandwidth, noise floor level measured by the analyzers will decrease. SNR calculation of a digitally produced sinusoidal is made with rms quantization noise inside the Nyquist Band, therefore directly using the

quantization noise floor value measured by spectrum analyzer will cause a wrong SNR calculation. Instead using the noise value measured by an analyzer, the total noise placed in the whole Nyquist Band should be calculated and used in SNR calculations.

3.2.3 Phase Truncation

Memory requirements of a DDS are important. The accumulator width identifies the phase resolution; however, the look up table, table of discrete amplitude levels, (LUT) following the phase accumulator has memory limitations limiting the phase resolution also. As mentioned in Chapter 2, if width and depth of a LUT is chosen to be 32 bit and 2^{32} addresses respectively, then 16 gigabytes of memory is needed which is infeasible. To overcome this memory requirement, DDS systems usually take the most significant P bits of an accumulator and disregard the rest. By this way, it is also possible to decrease the width of the LUT.

Accumulators usually have much higher resolution compared to phase resolution of LUTs. For example, a system with an accumulator width of 8 bits and LUT depth of 2^5 and width of 6 bits has an accumulator phase resolution of 1.41 degree, whereas 11.25 degree LUT phase resolution [11]. The resolution could be seen in the phase wheel drawn for this system in Figure 3.3. Dots on the outer circle represent phase resolution of the accumulator whereas the dots on the inner circle represent the phase resolution of the LUT.

LUT memory allocation directly disregards 7 least significant bits of the accumulator. Thus LUT approximates the phase pointed by the

accumulator causing a phase truncation. This phase truncation can be seen also in Figure 3.3 [15]. Phase accumulator jumps equal amount of phases according to tuning word. Phases pointed by the accumulator do not find a corresponding phase pointed by the LUT. The phase difference in between the accumulator and the LUT is the error function of phase truncation. Since accumulator is periodic, error function is also a periodic function.

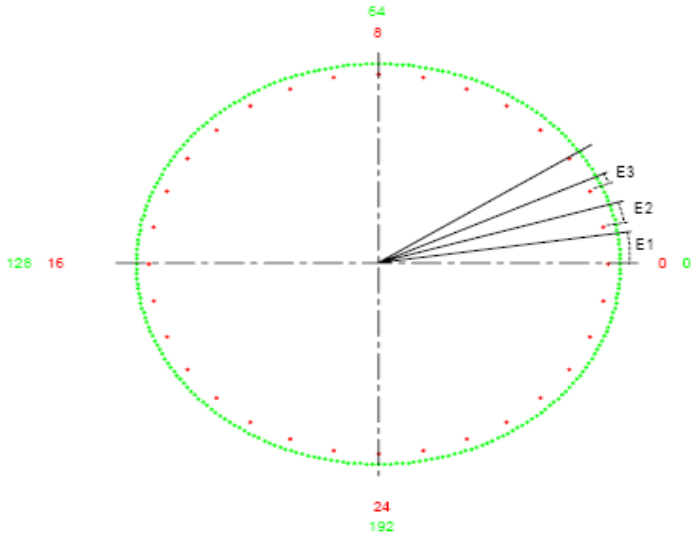


Figure 3.3 The Phase Wheel [15]

This periodicity of this error function causes spurs in the spectrum of the analog output. If A is the accumulator width, P is the phase word received by the LUT and T is the tuning word, then maximum spur level for a system which has at least 4 bits truncated ($A-P \geq 4$), the maximum spur level can be approximated by -6.02*P [15]. For example, if A is 32 and P is 12, then for that DDS system maximum phase truncation spur is -72dBc.

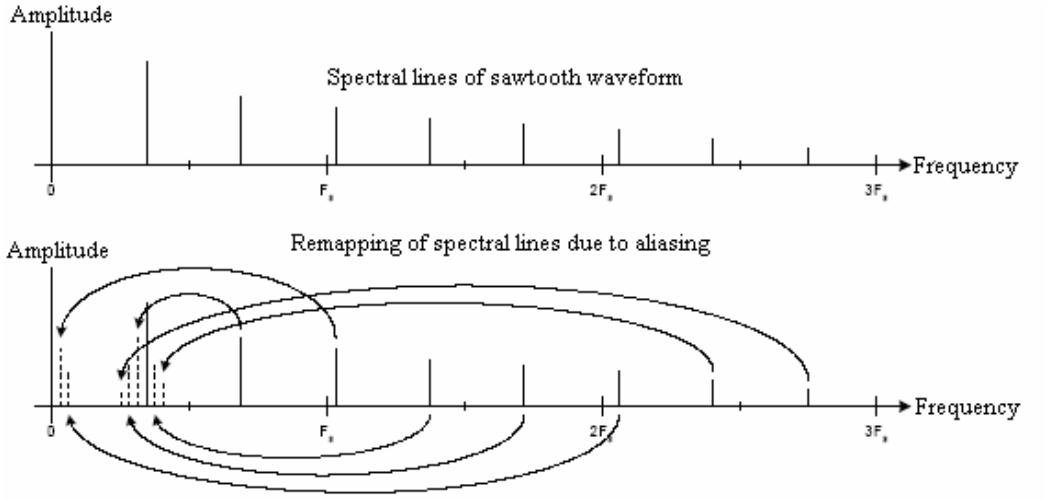


Figure 3.4 Spurs caused by phase truncation [15]

Remembering that frequency components higher that $f_S/2$ alias into the Nyquist Band due to the sampling theorem, the higher harmonics of truncation spurs alias into the Nyquist Band as seen in lower trace of Figure 3.4. Usually in order to filter the images of a digitally produced signal, the signal is lowpass filtered. This filtering is also beneficial to filter spurs located outside the Nyquist Band. However, since higher harmonics of truncation spurs alias into the Nyquist Band, the aliased spurs can not be filtered by lowpass filtering. Therefore these aliased spurs are the most important spurs that should be taken into consideration for SFDR requirements.

3.2.4 Nonlinearity Harmonics

Nonlinear characteristics of DAC are introduced in Chapter 2.2. These nonlinearities cause harmonics to appear in the spectrum even for perfectly sampled sinusoidal signals. The harmonics are located at multiple frequencies of output signal's frequency f_O.

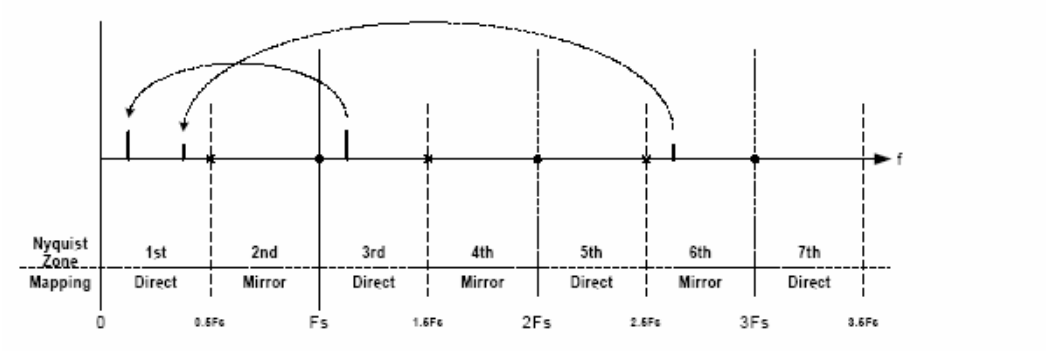


Figure 3.5 Nonlinearity harmonics [15]

In Figure 3.5 harmonics of a digitally produced sinusoidal signal are seen. At this point it is important to notice that again because of sampling, these harmonics alias into Nyquist Band. These harmonics can not be filtered and again very important with regard to SFDR performance.

Designers have to choose output frequency and sampling frequency very carefully in order to place these harmonics far away as much as possible from the carrier signal. Designers must be aware that aliased signals are placed in Nyquist Band according to this formula:

$$R = remainder(\frac{n.f_O}{f_S}) \tag{3.8}$$

$$f_{alias,n} = R \text{ if } R \leq f_S/2 \tag{3.9}$$

$$f_{alias,n} = f_S - R \text{ if } R \geq f_S/2 \tag{3.10}$$

Locations of harmonics at the spectrum are predictable; however their magnitudes are not. The magnitudes of harmonics change from DAC to DAC and usually manufacturers inform customers about harmonic performance of their products in their datasheets.

Designers must carefully analyze DAC datasheets before deciding on a DAC for a system.

3.2.5 Jitter and Phase Noise of the System Clock

Digital signal synthesizer's analog performance is closely related with the analog performance of the input clock. While analog performance of output signal is evaluated by its SNR and SFDR values, the analog performance of a system clock is evaluated by its phase noise (in dBc/Hz) and jitter (in ns or ps). The jitter and phase noise causes a digital synthesizer to give output at unequal sampling intervals resulting in noise and spurs. Effects of jitter and phase noise could be seen in Figure3.6.

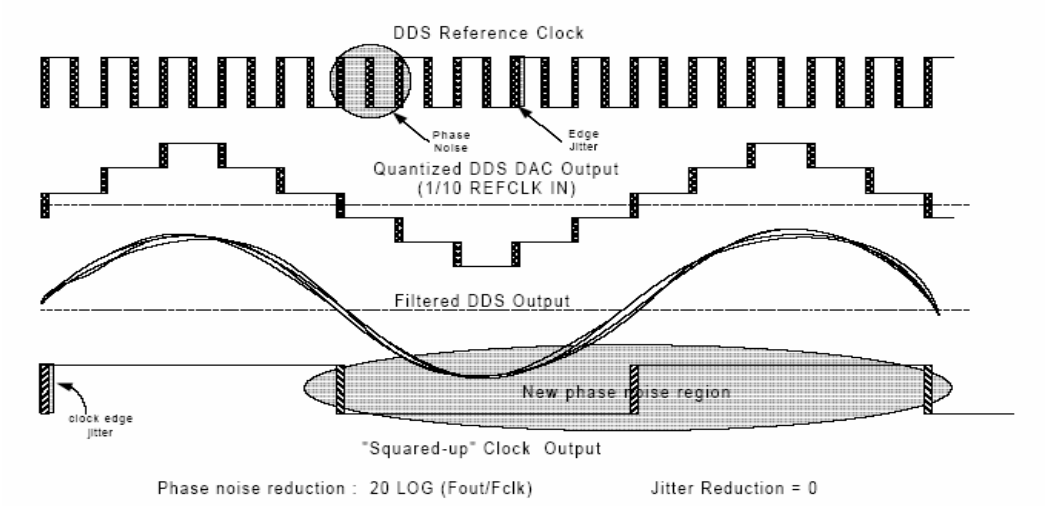


Figure 3.6 Jitter and phase noise [19]

Jitter occurs basically due to thermal noise and coupling noise [19]. Thermal noise is produced by random movement of electrons in

circuits where thermal noise power is expressed as eqn 2.3. Secondly coupling noise is the noise caused by crosstalk and/or group loops within or adjacent to the immediate area of the circuit. Moreover there could be coupling from surrounding environment which is called the electromagnetic interference (EMI).

The phase noise of clock is added to the output noise with a reduction according to the ratio of output frequency to the clock frequency [19]. The reduction could be shown as

$$\text{Noise Reduction} = 20\log\left(\frac{f_o}{fclk}\right). \qquad (3.11)$$

For instance, for a 100 MHz system clock, an output signal of 10 MHz will have 20dB less phase noise than the phase noise of the clock. The net phase noise caused by the clock will be added to the phase noise of DDS plus DAC system. Since the phase noise of DDS plus DAC system is also a contributor to total noise, it is a limiting factor for system performance. Therefore, it is not necessary for the phase noise of the clock to be better than this system's phase noise minus reduction level. For the example mentioned above, if the desired phase noise of DDS plus DAC system is 130dB, the phase noise of the clock need not to be better than 110dB. With a reduction of 20dB over the phase noise of the clock, the two 130dB phase noise will be added resulting in a total of 127dB system phase noise.

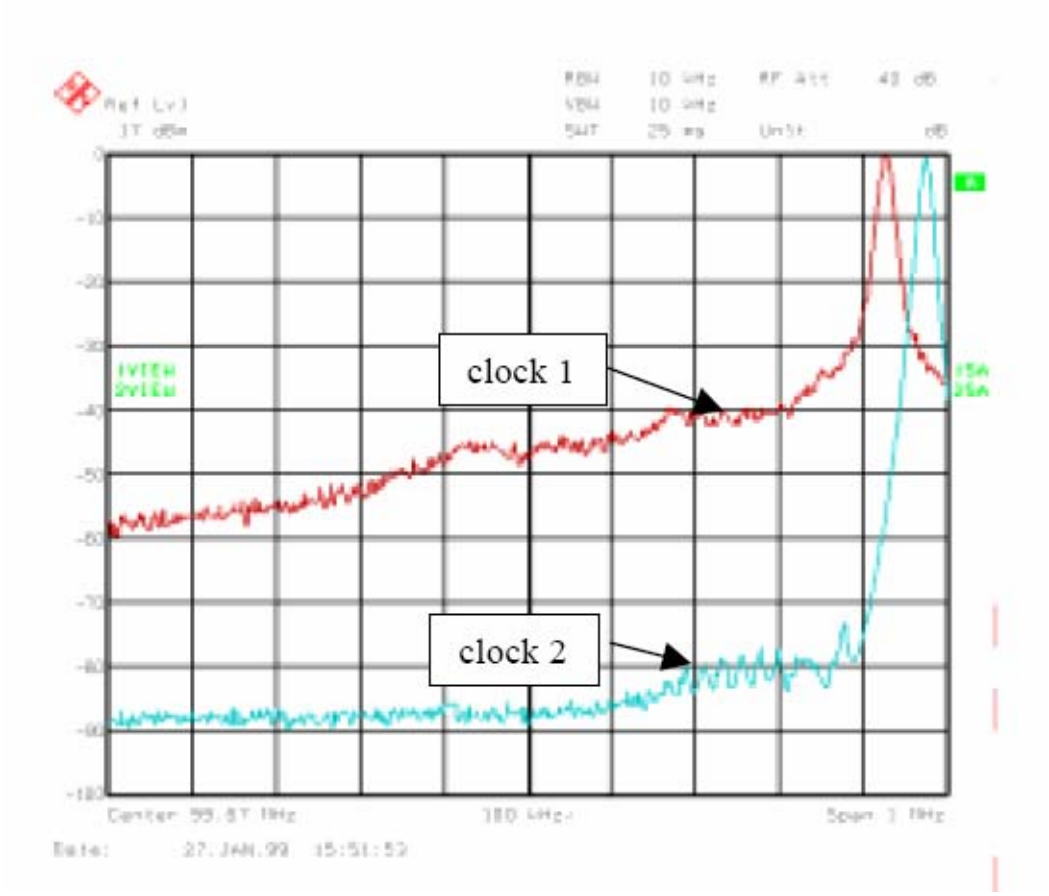


Figure 3.7 Phase noises of poor (clock 1) and good (clock 2) clocks [19]

In Figure 3.7, analog performance of a system derived with different clocks is shown. The improvement in clock phase noise improves the output phase noise level as well which will be seen in Figure 3.8.

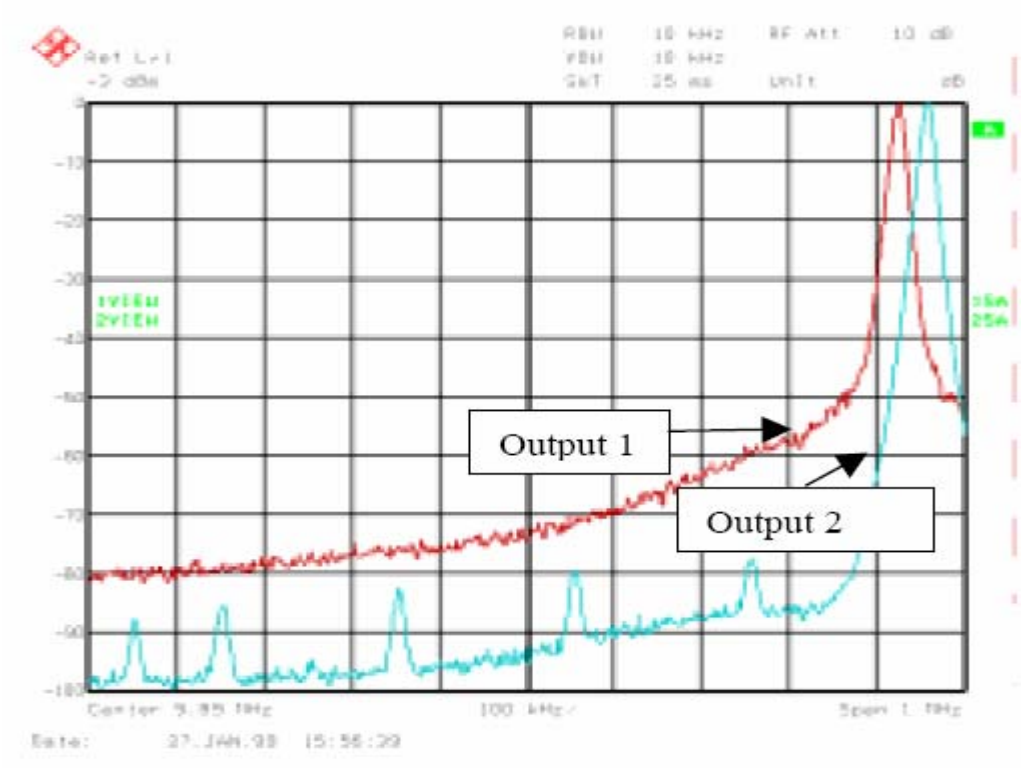


Figure 3.8 Phase noise of a DDS driven by good and poor clock [19]

In Figure 3.8 the phase noise performances of similar DDS systems which are driven with two different clocks are seen. Since the phase noise of the second clock is lower than the first one, the noise floor of the output 2 is lower than that of output1. At this point it is important to emphasize that the spurs seen in the second figure are due to phase truncation. As the output phase noise improves by 20 dB, the spurs hidden under the noise appear.

Moreover, some of the DAC have internal clock multipliers. Their main purpose is to soften the system clock requirements by giving the flexibility of using lower frequency clocks. Since these multipliers increase the frequency, they bring phase noise distortion. The distortion calculations are similar to phase noise improvement

calculations made in Eqn 3.10. However, the difference is that now the result is subtracted form the input system clock.

For example, a 4 times multiplier degrade the phase noise performance by 12dB (20log (4)) resulting in 88dB phase noise for a clock of 100dB phase noise.

In addition to phase noise, clock phase noise also degrades the SFDR performance of a digital signal synthesizer. Figure 3.9 shows spur levels of a system derived with two clocks with different phase noise performances which are -68dBc and -78dBc respectively.

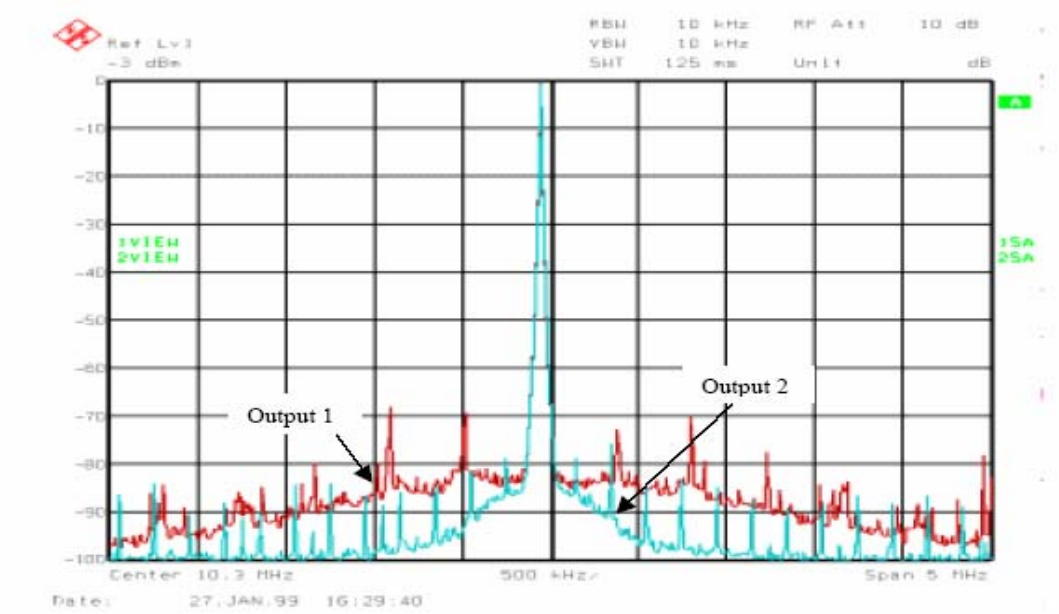


Figure 3.9 Output SFDR performance according to input clock phase noise [19]

As seen in Figure 3.9, SFDR performance of the second system is improved by 15dB approximately.

To conclude, for the best SFDR and SNR performance, it is critical to use a good clock source, and moreover it is beneficial not to use a clock multiplier.

3.2.6 Sin(x)/x Effect of DAC

Sample and hold blocks present in the inner architecture of DAC are mentioned in Chapter 2. These blocks are used to hold the previous analog output till next analog output stabilizes. In order to mathematically model the transfer function of these blocks, holding the sampled data could be thought of a convolution of sampled data with a square of unit height and width of $1/f_s$. Since convolution in time domain means multiplication in frequency domain, the spectrum of output signal will be multiplied with sin(x)/x function where x is $\pi f / f_s$. The mathematical derivations about sinc effect are made in Chapter 2.4.

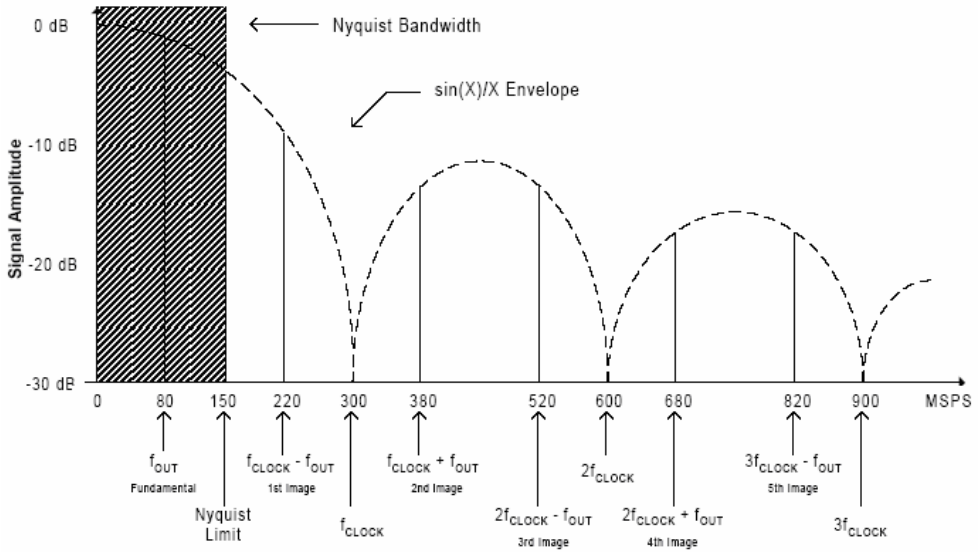


Figure 3.9 Sinc Effect [11]

As seen in Figure 3.10, sinc function brings different amplitude attenuations at different frequencies. For a wideband modulated signal, if the amplitude attenuations for the beginning and end of the band are quite different, an amplitude modulation will be produced in time domain. However it should also be noted that the magnitude response of sinc functions has approximately constant magnitude response in certain frequency ranges.

Firstly in the Nyquist Band magnitude response of sinc function makes sharp changes at frequencies after $0.4\,f_s$ Hz. If the designer could place the band of the modulated signal in frequencies below $0.4\,f_s$ the band of the output will not be affected from sharp changes [14]. Also the attenuation level of a sinc function up to $f_s/2$ is analyzed in MATLAB. Sampling rate is taken as 270MHz. Figure 3.11 shows its attenuation level in Nyquist Band. At 108MHz (0.4*270) sinc function causes only 2.35dB attenuation. This attenuation is under the limit of 3dB attenuation which is taken as reference limit attenuation in all analog filter designs for the passband region. Moreover the analog filter's passband transfer characteristics can also be simply modified to compensate for this 1-2dB sinc effect.

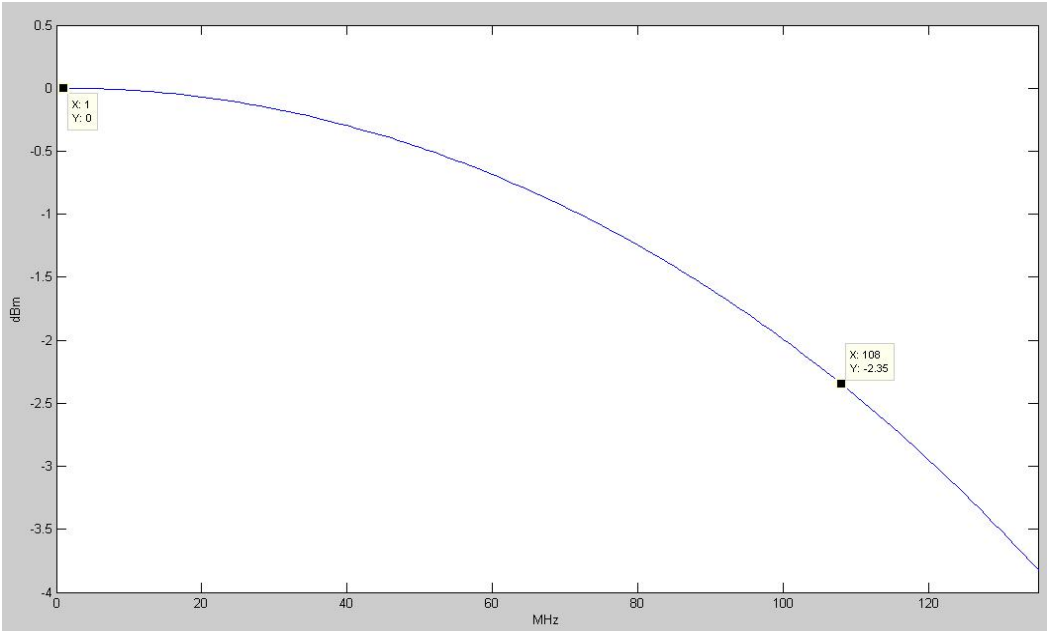


Figure 3.11 Sinc effect in Nyquist Band

A second method to compensate for the sinc effect is using an inverse sinc function. An inverse sinc function, which is x/sin(x), multiplied with the sinc function yield in constant magnitude response. In order to correct the spectrum of the output signal, the inverse Fourier transform of the inverse sinc function could be taken as digital filter coefficients so that the digital words are filtered with this filtered before passing these words to converters.

Moreover, some designers may prefer to bandpass filter sampling replicas of the signal placed at $|f_O + Kf_S|$, where $K \geq 2$. Although, by this method a signal could be upconverted digitally, this method is not generally preferred since the behavior of harmonics at higher frequencies are more unpredictable and may significantly degrade the SFDR performance of the signal. However, if a designer decides to upconvert signal digitally, the designer must compensate for the sinc

effect by using an inverse sinc filter since the sinc effect is more apparent at higher frequencies. For example, the replica of the signal placed at 380MHz in Figure 3.10 is attenuated by 15dB.

3.2.7 Filter Response

The requirement for an analog filter and filter parameters are mentioned in Chapter 2.3. Group delay, magnitude response and bandwidth of the filter are critically important parameters of filters and in order to be able to filter the required signal from spurs and images, designer has to choose sampling frequency, output frequency and the bandwidth carefully. For instance, SFDR requirement of a system is a key parameter in defining the stopband attenuation value of the filter. Besides, sampling frequency relative to the frequency of the output signal defines the location of images and hence identifies the transition band requirements of the filter.

In Figure 3.12, the relation between the transition bandwidth and the sampling frequency is discussed. In the left portion of the signal the transition band required to suppress DR dB which is much smaller than the transition band shown in right portion. In the right portion the sampling frequency is increased, so the image is carried further away from the fundamental signal in the spectrum, allowing higher transition band for the filter. This relaxation in transition bandwidth also decreases the complexity of the filter.

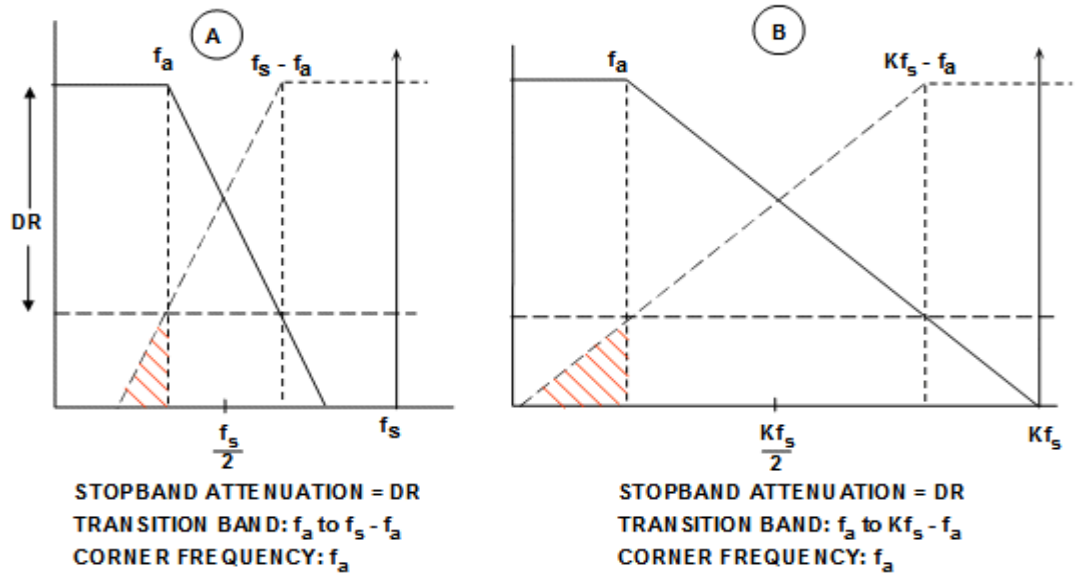


Figure 3.12 Filter characteristics for two different sampling frequencies [14]

Moreover some amplifiers that are used in transmitters have non linear distortion characteristics. These amplifiers can convert any amplitude fluctuation on a signal to a phase modulation. Therefore any amplitude fluctuation or in other words modulation on the signal will result in phase distortion at the output of the amplifier. This is called AM to PM conversion characteristics of an amplifier. This conversion will cause a phase or frequency distortion according to unwanted amplitude modulation.

Amplitude modulation in such systems is related with the amount of energy that is not passed by the filter. In the ideal case, for which the signal power is distributed over the spectrum up to infinity, perfect sharp phase transitions and periods of constant phase will be observed without any amplitude modulation in between different phases and during a period of constant phase. However, since we filter the output of the digital synthesizer, the sharp phase

transitions are smoothened, widened and amplitude modulations during phase transitions and periods of constant phase are observed. In such cases, the passband width and the flatness of the passband of the filter is important.

Finally, group delay is a generally unwanted effect of filters. Usually group delay is required to be in nanoseconds in the passband of the filter.

To conclude, the strictness of the filter parameters increases or decreases the complexity of the filter. In some cases impractical values of parameters could be reached to design a filter fulfilling system requirements. In such cases, at least the sampling frequency should be updated to provide flexibility for the designer to design the filter. Since further analysis of a required filter could only be explored for a specific case, in Chapter 6 detailed analysis will be made for a specific system.

3.2.8 Hardware

Beyond the noises, harmonics, spurs, and images that are directly produced by DDS plus DAC system, faulty board designs interfacing DDS and DAC could also degrade SNR and SFDR performance of the analog output.

Board design procedures and methods are too complicated to cover in detail. In brief few points that designers have to consider are

1) Grounds of analog and digital circuits must be separated. Otherwise noise created by fast transitions of digital circuits, will raise the noise floor of the analog output.

2) Required analog output has to be separated from other analog signals like clocks as much as possible. Moreover a shield has to be used in order to separate clock circuits from analog output. Otherwise EMI or interference due to conduction will be observed in the spectrum of analog output, degrading the SFDR performance.
3) Transmission lines must be matched to the characteristic impedance of the DAC output so that reflections due to the wrong termination will be prevented.

These three most significant points are critical. To guarantee the proper operation of their systems, designers may have to analyze and understand the design procedures of analog boards in more detail.

CHAPTER 4

DSS DESIGN ON FPGA

4.1 GENERAL

DSS system that is desired to be designed in this thesis work requires high modulation capabilities such as modulation variety, fast transition times, very high frequency and phase resolution. In order to meet these requirements DDS technology is taken as reference. However DDS systems produce only single tone signals if no additional digital systems are integrated with it. In order to attain modulation capabilities like amplitude modulation 'AM', frequency modulation 'FM', phase modulation 'PM' and more complex modulations to DDS, digital control systems is designed and integrated with DDS. In this chapter these designs, their methodologies and their outputs will be explained in detail. Hardware and software platforms that are used in our designs will also be introduced.

4.2 HARDWARE AND SOFTWARE PLATFORM

In this thesis, all DDS and digital control systems are implemented on a Field Programmable Gate Array (FPGA). FPGAs consist of millions of transistors to be programmed in order to serve for a specific application. Programming transistors means to make required connections in between transistors to form required digital circuits. The connection in between the transistors is done according

to the bit file produced by the user. The bit file is a hardware description file compiled from high level programming languages like VHDL or Verilog.

Design methodology of VHDL is totally different from other software languages written for processors. Since different digital circuits could be implemented in different parts of a FPGA, several applications can run at the same time in a FPGA in contrast to a processor. Processors can only process one task at a time, therefore the sequence of a program also identifies the work sequence of a processor. However logic implemented on a FPGA will not have a sequence unless it is specified by the user. The digital logic implemented by a user will be always working and the only way to put these circuits in a sequence could be done by using states. This parallel processing is a great advantage of FPGA compared to processors in areas such as signal processing.

In this thesis, especially FPGAs of Xilinx Inc. are preferred. Consequently the development environment of Xilinx which is Integrated Software Environment (ISE) is used to design digital circuits using VHDL. ISE development platform is also integrated with MATLAB Simulink environment. A product called the System Generator designed by Xilinx uses similar graphical interface as Simulink and can be used with MATLAB. System Generator enables users to design digital circuits visually with blocks.

In the following sections, DDS and its control circuits designed with System Generator will be explained.

4.3 SINGLE TONE PRODUCED BY DDS

As mentioned in Chapter 2, DDS has fundamental blocks like accumulator and look up table. Using System Generator, a DDS is designed as seen in Figure 4.1.

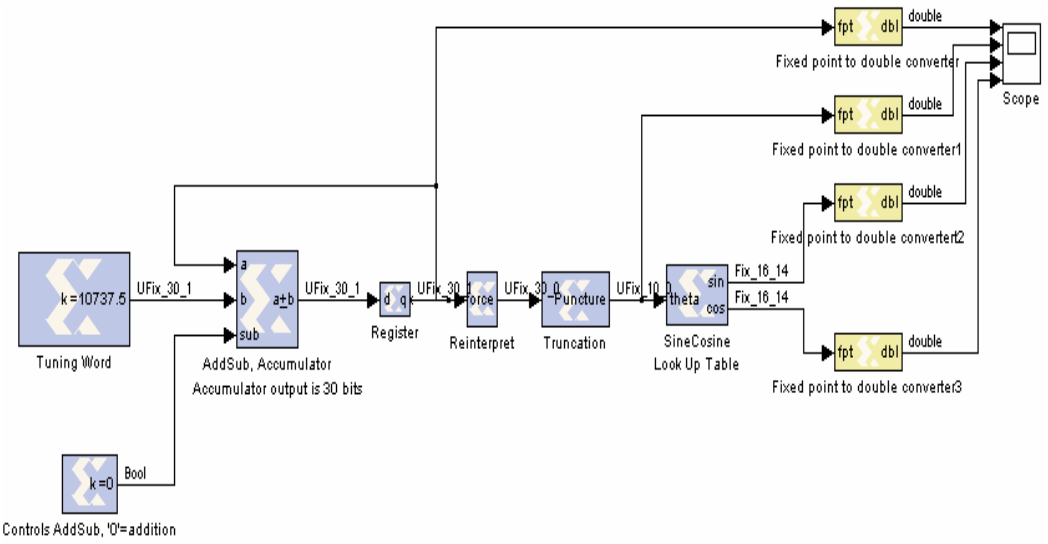


Figure 4.1 DDS design in System Generator

The accumulator is formed by an adder with a feedback loop and input tuning word. The accumulator is followed by a lookup table. As better seen in Figure 4.2, a truncation takes place since FPGA LUT is addressed with 10 bits in order to observe phase truncation better in the following simulation. It should be noted that LUT can hold maximum 2^{16} addresses in a FPGA. In this design, most significant 10 bits of the 30 bit accumulator is taken and pointed to LUT memory which is (2^{10}x16) 2kB.

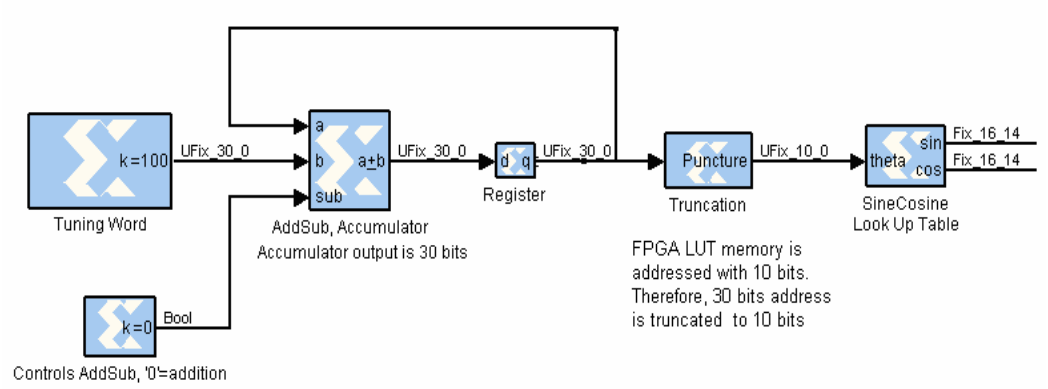


Figure 4.2 Closer look to DDS designed in System Generator

On the scope truncation can be seen as in Figure 4.3. Accumulator output increases as seen in the upper trace; however phase word, lower trace, increases according to 10 most significant bits of the accumulator resulting in a phase error.

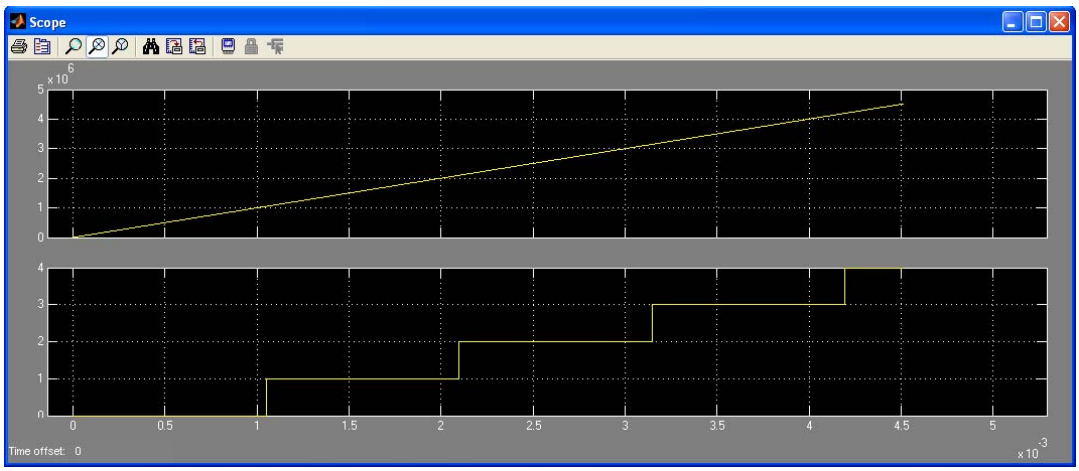


Figure 4.3 Simulation of phase truncation

The system is working with 100 MHz clock. The tuning word was chosen to be 10737 in order to produce 1 KHz output. The output of the DDS is as seen in Figure 4.4.

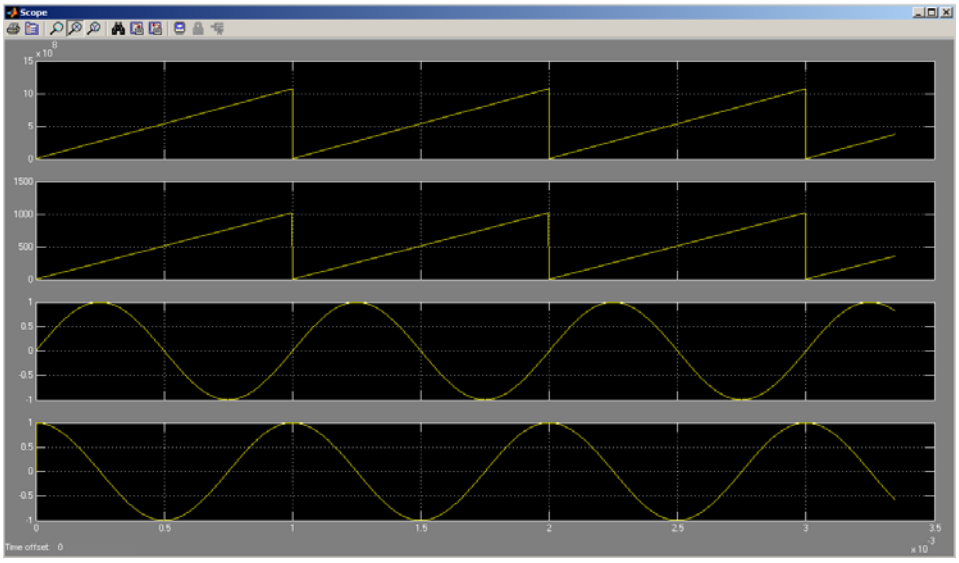


Figure 4.4 1 kHz sine and cosine produced by DDS

In Figure 4.4, first trace is the output of accumulator, second trace is the output of phase word and the last two traces are sine and cosine, respectively. 1 KHz signal is represented by 100000 samples; therefore it is difficult to observe sample steps. Now a 10 MHz signal will be produced with this system.

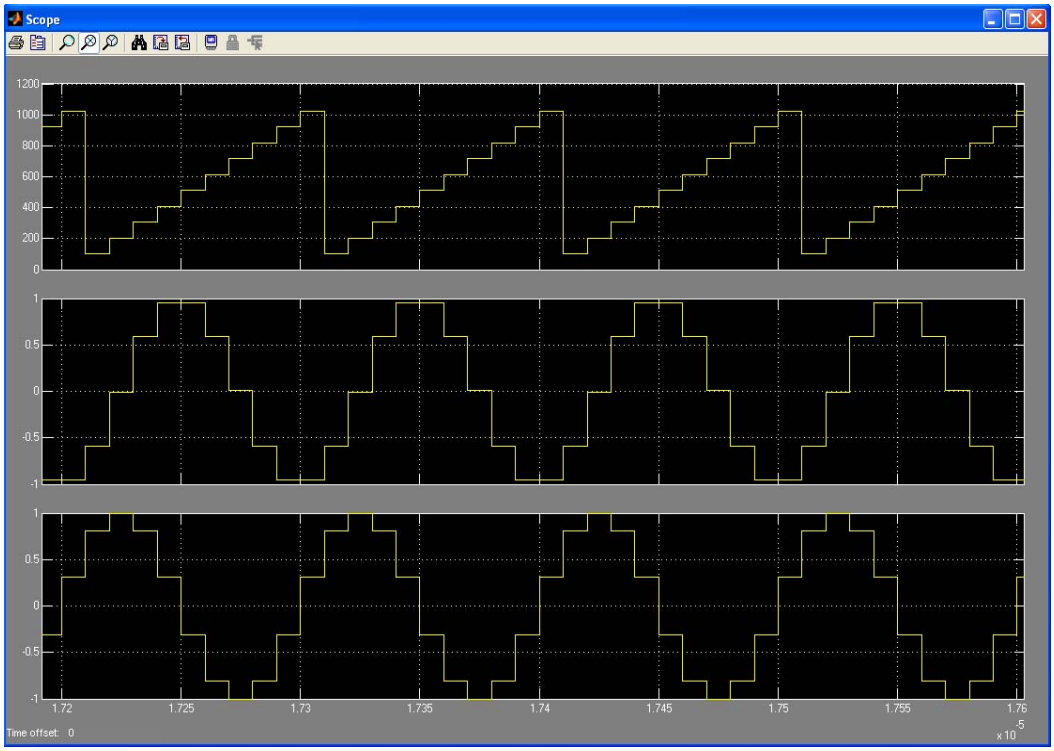


Figure 4.5 10MHz sine and cosine produced by DDS

In Figure 4.5, since system is again working at 100MHz, ten samples of 10 MHz sine and cosine signals are seen. Phase word of the LUT and phase of the signal increases linearly, so that samples corresponding to that phase are latched to the output of the DDS.

The samples of the output are hold for one clock duration since the outputs are latched and hold at that signal level for one clock period.

4.4 FREQUENCY MODULATION

Frequency modulation is the linear change of the instantaneous frequency of a signal according to a message signal *m(t)* where *m(t)* could be any information wanted to be transmitted between links.

Change of instantaneous frequency of a signal corresponds to change of tuning word for a DDS system. In order to adapt frequency modulation capability, a DDS must have a control logic that will change tuning word according to information.

As seen in eqn. 4.1, the instantaneous frequency of signal *s(n)* is a function of information *m(n)* where *g(.)* could be any function.

$$s(n) = A_c \cos\left[2\pi f_o(n)n + \theta\right] \tag{4.1}$$

$$f_o(n) = g(m(n)) \tag{4.2}$$

If *g(x)* is a linear function of *m(n)* then at the output, frequency jumps will be observed at every change of *m(n)*. Moreover *g(.)* could be a frequency sweeper function which sweeps the frequency of *s(n)* slowly to a desired frequency. For example some radar transmitters employ frequency sweepers. In these radars, pulses transmitted by the radar contain a signal whose frequency is swept between two frequencies linearly during the pulse duration. These kinds of pulses are called chirps.

In System Generator, a dynamic system working in two different modes is designed to be implemented on FPGA. In one mode, the system changes the frequency of the output signal according to the input in between four different frequencies which is called frequency shift keying(FSK). In the other mode it sweeps the output frequency of the output signal in between a defined frequency range.

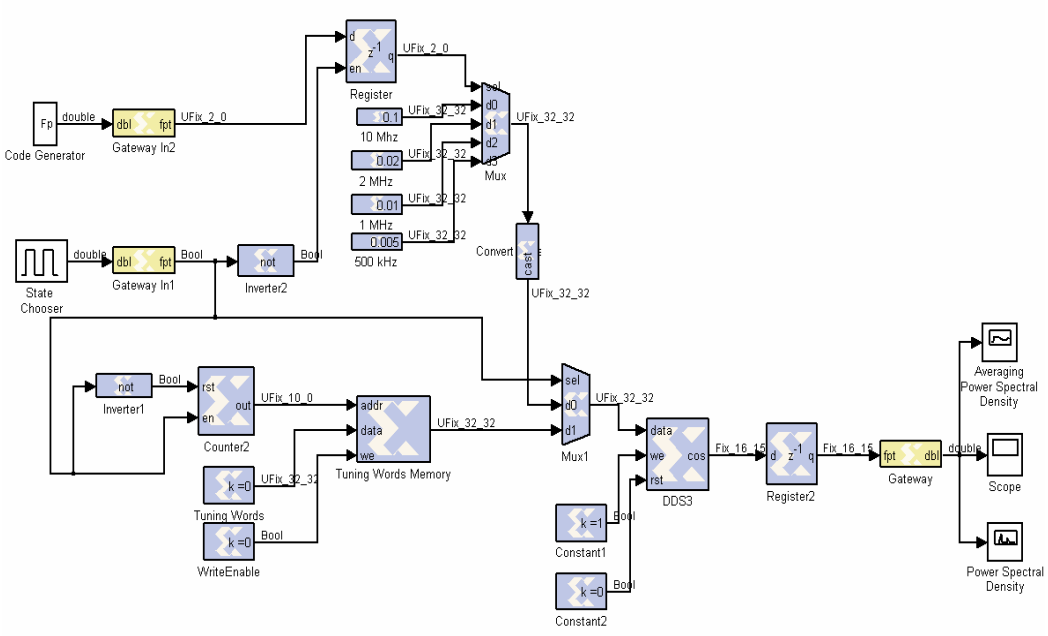


Figure 4.6 Frequency modulating DDS

The designed system shown in Figure 4.6 can sweep between 1 MHz and 10 MHz in 5 micro seconds. The tuning word memory is chosen to sweep frequency in 5 micro seconds with a 100 MHz clock. The user can change the sweeping speed and the frequency ranges by changing the content of the memory. The tuning word memory is formed by 500 tuning words. Since the system clock is 100 MHz, 500 tuning word will be outputted in 5 micro seconds which is the desired time period. The calculation of tuning words is done after eqn. 2.1. The linear increase of tuning word results in a linear frequency sweep in the output as seen in Figure 4.7.

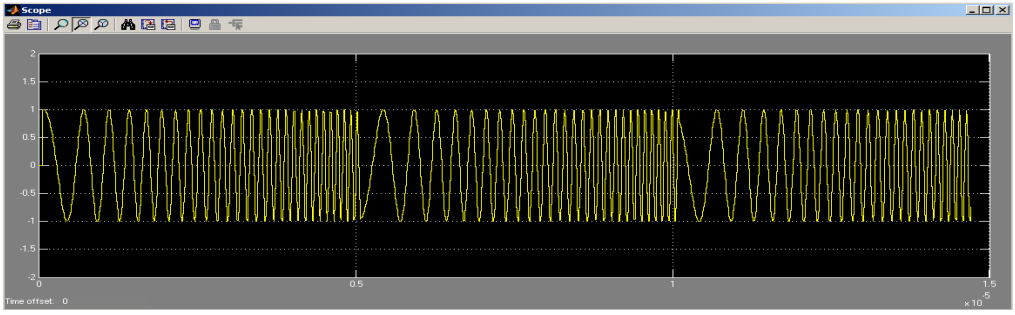


Figure 4.7 Chirps

In order to observe the swept frequency range, average power spectral density of the output is plotted as seen in Figure 4.8.

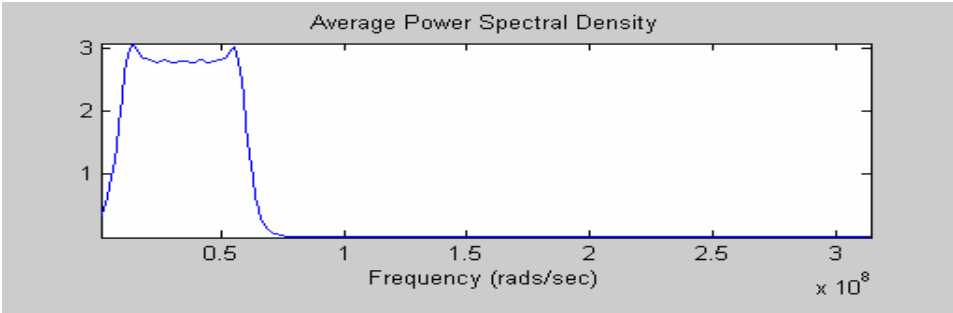


Figure 4.8 Average power spectral density (PSD) of a chirp

In the other mode the output is shifted in between four frequencies according to random code generator working at 200 kHz. Four chosen frequencies are 500 kHz, 1 MHz, 2 MHz and 10 MHz. The output of this random sequence is as seen in Figure 4.9.

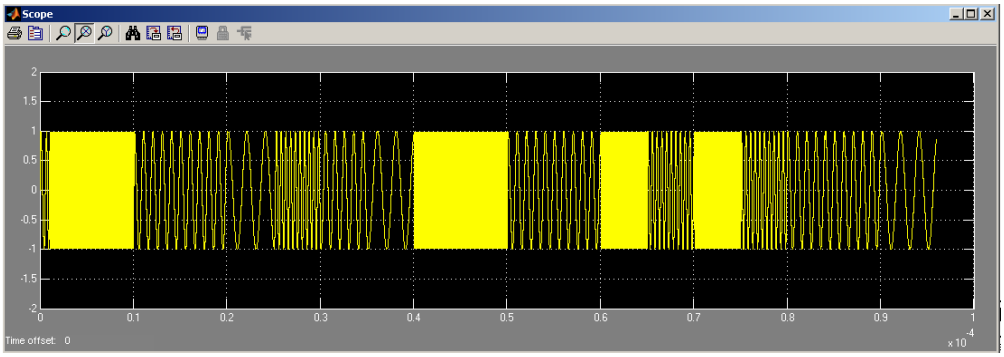


Figure 4.9 Frequency jumps

Since the smallest time scale of a DDS is the system clock period, output modulation could be changed at every clock by simply controlling the outputs of DDS at every clock. As a result of this, designers have a superior control over the modulation capabilities and the synthesizer system at a resolution of system clock.

4.5 PHASE MODULATION

Similar to frequency modulation, phase modulation is an instant change of signal's phase according to the information wanted to be transmitted. An instant change of output signal's phase corresponds to addition of offset to the address pointed by the accumulator in order to point to another address that will add required phase to the output.

In parallel to the designed frequency modulation system, another phase memory or dynamic control system may be designed to add address offsets to the output of the accumulator. However another approach will be discussed in order to phase modulate the output signal.

Let us start again write Eqn 4.1 in the canonical form so that phase of the signal varies in time instead of frequency:

$$s(n) = A_c \cos[2\pi f_o n]\cos[\theta(n)] - A_c \sin[2\pi f_o n]\sin[\theta(n)] \qquad (4.3)$$

As observed in eqn. 4.3, instead of directly modulating the output signal by using the internal architecture of DDS, the signal can be modulated using canonical representation of bandpass signals. This operation is, in other words, upconversion of the baseband signal. Here it could be concluded that DDS can also be used as an upconverter besides its modulation and synthesizer capabilities.

Upconversion of a baseband signal is not only limited by the Nyquist Band which is the frequency band located up to the half of the sampling frequency, zone 1 in Figure 4.10. The nature of sampling causes replicas of the signal to appear in the spectrum at frequencies $|f_O + Kf_S|$, where $K \geq 2$. As mentioned in Chapter 3.2.6, these replicas, such as the replica in zone 3 in Figure 4.10, could also be filtered and transmitted by overcoming the sinc effect. Thus it could be concluded that a careful frequency planning for DDS will upconvert the baseband signal to the desired frequencies.

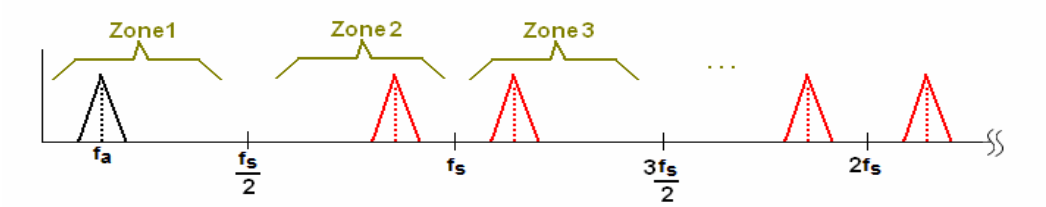


Figure 4.10 Upconversion caused by sampling

In order to perform the operation in eqn 4.3, the system shown below is designed in System Generator.

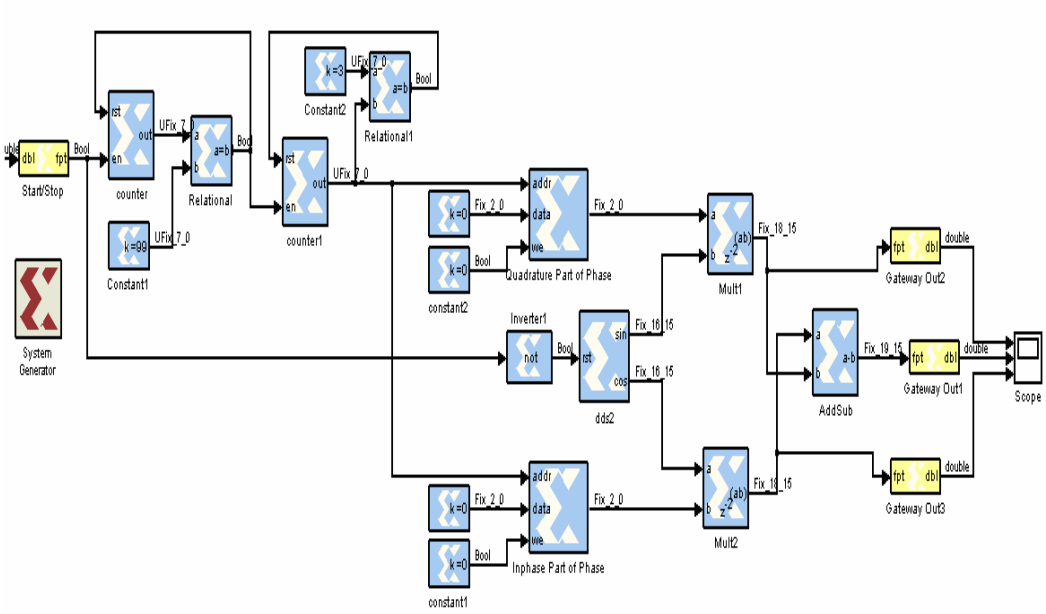


Figure 4.11 Phase modulating DDS

The inphase (I) and quadrature (Q) parts of phase modulating the carrier are stored in memories. System is again working with 100 MHz and DDS is producing 4 MHz cosine and sine signals. For every 100 clocks, memories output one code resulting in a 1 MHz modulation rate. The codes stored in the memories are amplitude levels that will be multiplied with cosine and sine. These values are actually the projections of modulated signal on the inphase and quadrature axes in the constellation diagram. In this design, signal is QPSK modulated with phase values $\pi/4$, $3\pi/4$, $5\pi/4$ and $7\pi/4$ as seen in Figure 4.12. The amplitude of the signal is 1.414V.

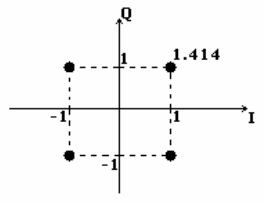


Figure 4.12 Constellation diagram of QPSK modulated signal

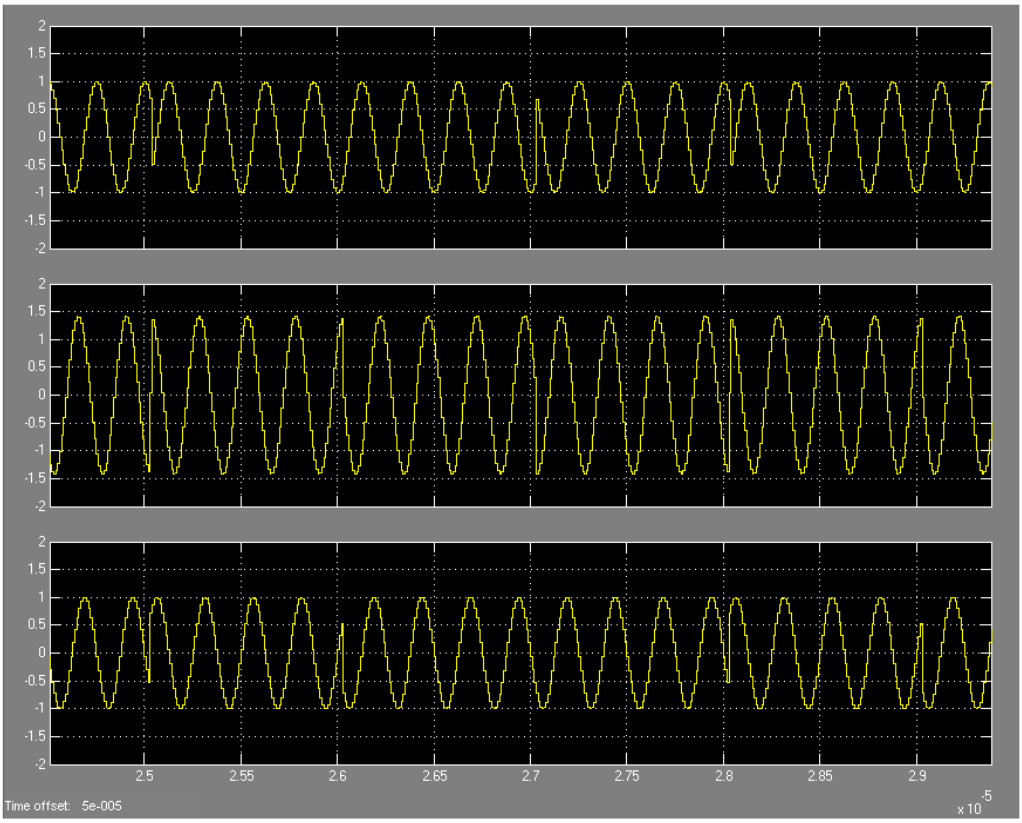


Figure 4.13 QPSK modulated signal produced by DDS

The output of the system is as shown in Figure 4.13. First and third traces output the inphase and quadrature components of the signal, respectively. Second trace is the QPSK modulated signal.

The phase modulation capability of a DDS system can be extended by various codes stored in the memory. Once again as in frequency modulation, phase changing speed is limited by the clock speed. Moreover, phase resolution is very high since there is a digital control over phase offset.

4.6 NONLINEAR MODULATIONS

Beyond the fundamental modulation methods like AM,FM and PM, it is possible to produce signals which are modulated nonlinearly with more complex methods such as Continuous Phase Modulation 'CPM'.

CPM is a method to change the phase of a signal linearly in a certain period of time instead of jumping from one phase value to the next instantly. Phase jumps in time domain result in expansion of signal bandwidths. Since the radio spectrum is shared by many users, the expansion of signal bandwidth is not a desired situation. Moreover as explained in Chapter 3.2.7, the smaller the bandwidth of the signal compared to sampling frequency, the better the design of analog filters will be. Besides if the bandwidth of the signal decreases and the same analog filter is used, then higher energy will be passed through the filter resulting in smaller AM.

In order to test CPM capabilities of DDS, a special form of CPM, Minimum Shift Keying 'MSK', is chosen to be designed in System Generator. MSK signals are produced by changing the phase by $\pi/2$ or $-\pi/2$ (depending on the binary data) linearly in the time determined by MSK symbol duration.

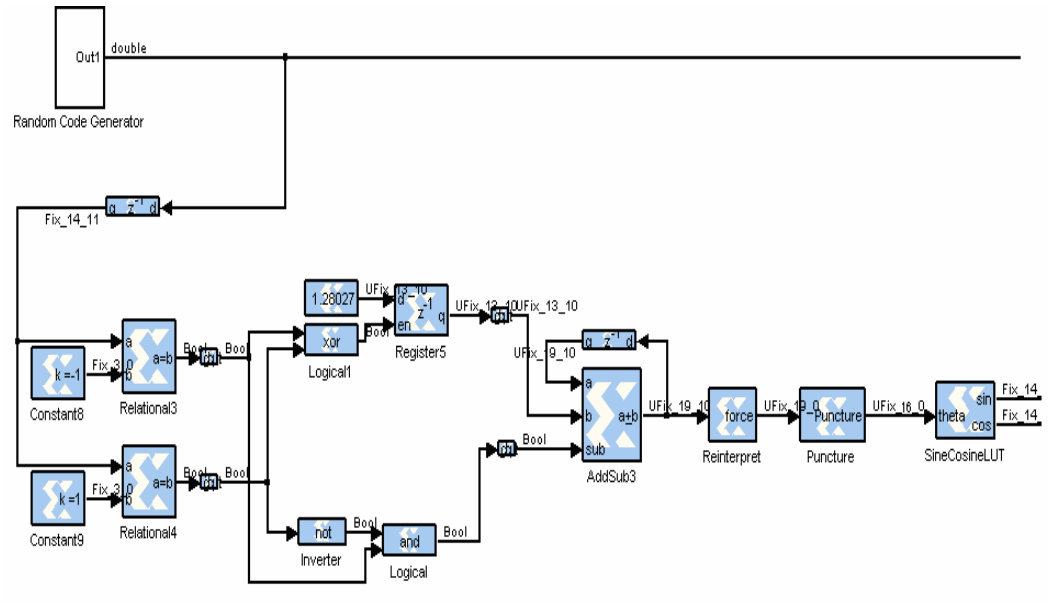


Figure 4.14 MSK modulating DDS Part1

The system is designed again with the same methodology as explained in phase modulation. Firstly I and Q parts of the phase to be modulated are produced at the baseband and upconverted with the single tone produced by DDS. Modulation rate is 1 MHz, carrier frequency is 4 MHz and system is working with 100 MHz clock. Since modulation duration is 1usec, there are 1000 steps to change the phase of the signal $\pi/2$ or - $\pi/2$. A Sine-Cosine LUT is pointed by 1000 step counter. Each step increment causes LUT to output consecutive cosine and sine of corresponding phase which are in phase and quadrature parts of phase.

In Figure 4.14, the code generator, counter, and LUT are depicted. Following this in Figure 4.15 upconverter part of the MSK modulator could be seen.

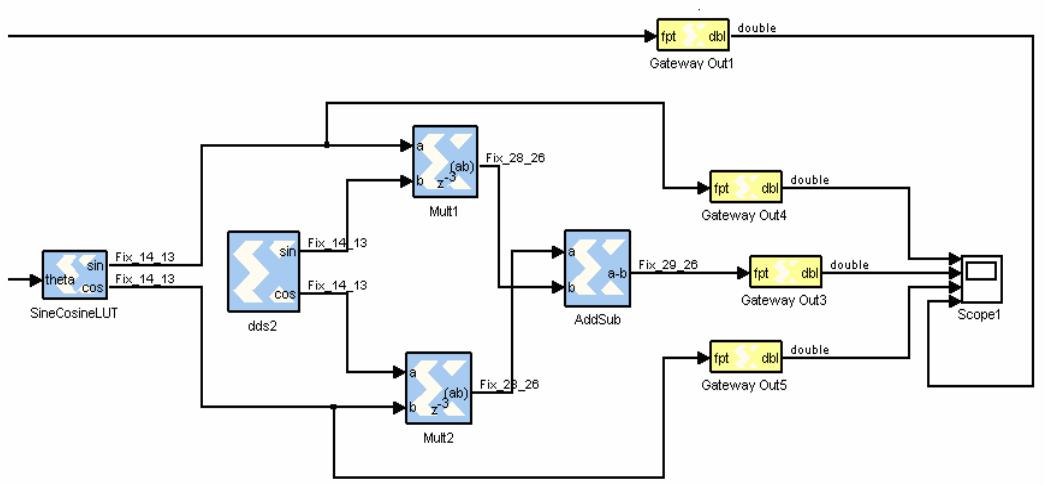


Figure 4.15 MSK modulating DDS Part2

The output of the modulator is plotted in Figure 4.16. First and third traces show the phases of I and Q components in π radians, respectively. The second trace is the output of the upconverted signal whereas the fourth trace is the binary word. As seen in the second trace, the amplitude of the signal is constant and no sharp phase transitions could be observed.

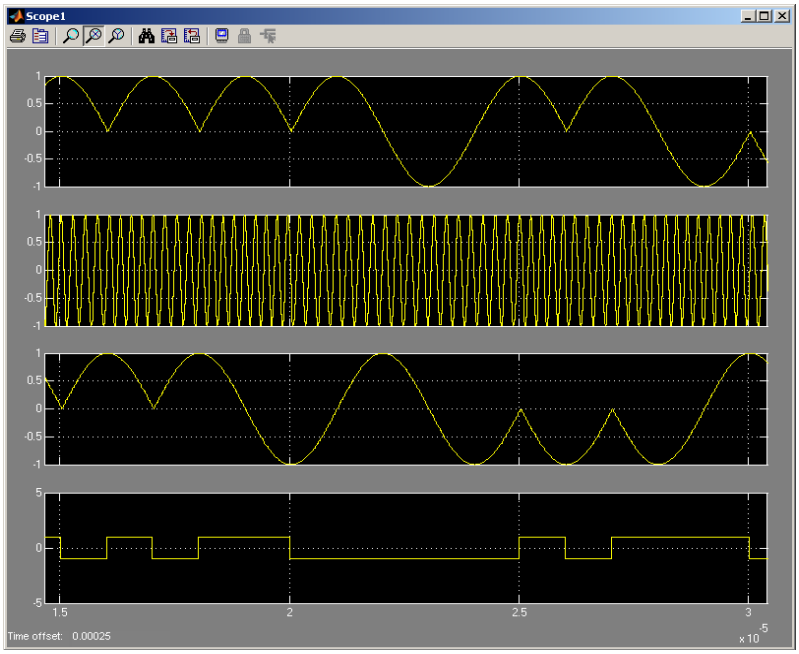


Figure 4.16 MSK modulated signal produced by DDS

In order to see the effects of CPM in the spectrum, spectra of classical QPSK and MSK are plotted in Figure 4.17 and Figure 4.18, respectively. The bandwidth of the signal in the second spectrum is much smaller compared to bandwidth of the signal in the first spectrum.

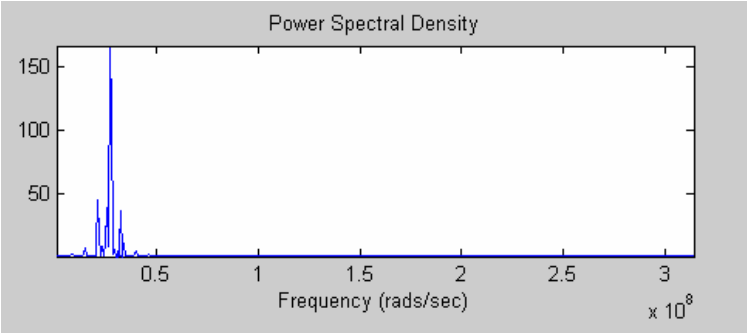


Figure 4.17 Spectrum of QPSK modulated signal

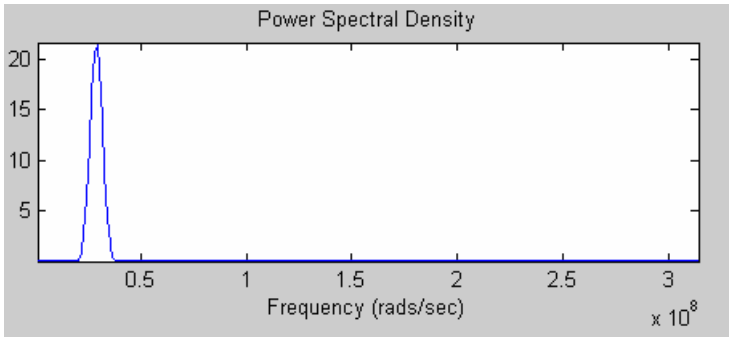


Figure 4.18 Spectrum of CPM modulated signal

Especially, in the second spectrum, it is apparently seen that sidelobe levels of the signal drops quite quickly, reducing the bandwidth of the signal. This will result in less AM at the output of the signal since higher energy will be passed through the analog filter.

All designs mentioned till now are transformed to ISE development environment and synthesized to be implemented on a FPGA. At this point it is important to emphasize that all of these modulating systems can be implemented on a FPGA together within a single design. This will give the flexibility of controlling modulation techniques and signal processing chains to the user. Moreover the FPGA LUT depth is 2^{16} which means 0.0055° phase resolution and with these systems the frequency or phase of the signal can be switched in just one sample time which is sampling period.

In Chapter 5, the designed and implemented DSS hardware will be explained. Following this some of the digital designs mentioned in this chapter will be implemented in that hardware and real outputs of DDS-DAC system will be observed.

CHAPTER 5

HARDWARE SETUP

5.1 GENERAL DESCRIPTION

The general aim of this thesis is to be able to implement digital signal synthesizer satisfying high dynamic performance requirements at defined frequency ranges. For this purpose analysis of critical parameters of DSS are made in Chapter 3 and following this in Chapter 4 DDS systems are designed in software platforms such as ISE in order to be implemented in FPGAs. After these studies, it is observed that SFDR or SNR performance limitation will not be caused by a DDS system since FPGAs offer extended DDS capabilities such as very high phase, frequency and amplitude resolution, fast switching times and controllability. Therefore, in order to be able to come up with an approximate digital synthesizer output performance, it is understood that selection of a DAC is a critical issue obliging a designer to focus on and compare DAC available in the market.

The process of DSS implementation started with the comparison and evaluation of the DAC currently available in the market. After making a decision on a DAC that is satisfying system requirements, a FPGA is integrated with this DAC by interfacing the digital input and control pins of the DAC with the pins of the FPGA. With this integration, outputs of DDS cores implemented in the FPGA were successfully connected to the DAC. The addition of an analog filter

to this setup completed the digital signal synthesizer satisfying system analog design requirements.

In this chapter, firstly design requirements will be introduced. Then systematic work done throughout the comparison of DAC will be explained. Finally configuration of the hardware setup will be described in order to gain a deeper insight to DSS implementation.

5.2 COMPARISION OF DAC

Analog Device and Maxim are the leading analog integrated circuit manufacturers in the world. These two companies have very wide range of products including DACs and 'Analog to Digital Converters' (ADC). Even among DACs, there are various product families addressing all kinds of applications. Therefore, the design specifications should be precisely defined in order to be able to choose the best DAC for a definite design. Considering the analog performance requirements of this thesis such as synthesizing signals between 50-100 MHz with 60dB SFDR, we put forward these criteria for DAC.

DACs have to

1. Have at least 60dB SFDR performances in a frequency range of 50-100MHz. The 60dB SFDR requirement is determined by parameters such as received signal dynamic range and provided to us by system designers.
2. Have at least 12 input bits. The SNR level can not be lower than 60dB for a system requiring 60dB SFDR in the light of the assessment in Chapter 3.2.1. The minimum DAC input bit number should not be lower than 12 bits in order to leave a margin of 12dB over the theoretical expectations.

3. Have at least 200 MSPS sampling rate since this rate is the minimum sampling rate in order to place the first image signal in a considerable frequency away from the real signal for a modulated signal above 50MHz.

According to criteria introduced above, following converters given in tables 5.1 and 5.2 of Analog Device and Maxim were found, respectively.

Table 5.1 DACs of Analog Device that are under consideration

Part Number	Description	Resolution (Bits)	DAC Update Rate	Number of Outputs
AD9736	14-Bit, 1.2 GSPS TxDAC+® D/A Converter	14	1.2GSPS	1
AD9735	12-Bit, 1.2 GSPS TxDAC+® D/A Converter	12	1.2GSPS	1
AD9779	Dual 16-Bit, 1.0 GSPS D/A Converter	16	1GSPS	2
AD9778	Dual 14-Bit, 1.0 GSPS D/A Converter	14	1GSPS	2
AD9776	Dual 12-Bit, 1.0 GSPS D/A Converter	12	1GSPS	2
AD9786	16-Bit, 160 MSPS TxDAC+® with 2×/4×/8× Interpolation and Signal Processing	16	500MSPS	1
AD9777	Dual 16-Bit, 160 MSPS, 2x/4x/8x Interpolating TxDAC+® D/A Converter	16	400MSPS	2
AD9775	Dual 14-Bit, 160 MSPS, 2x/4x/8x Interpolating TxDAC+® D/A Converter	14	400MSPS	2
AD9773	Dual 12-Bit, 160 MSPS, 2x/4x/8x Interpolating TxDAC+® D/A Converter	12	400MSPS	2
AD9755	12-Bit, 300 MSPS TxDAC+® w/ Dual Latched MUXd Input Ports & Internal Clk Doubling PLL	14	300MSPS	1
AD9753	12-Bit, 300 MSPS TxDAC+® w/ Dual Latched MUXd Input Ports & Internal Clk Doubling PLL	12	300MSPS	1
AD9744	14-Bit, 210 MSPS TxDAC® D/A Converter	14	210MSPS	1
AD9742	12-Bit, 210 MSPS TxDAC® D/A Converter	12	210MSPS	1
AD9857	14-bit , 200 MSPS Quadrature Digital Upconverter	14	200MSPS	1

Table 5.2 DACs of Maxim Inc. that are under consideration

Part Number	Description	Resolution (Bits)	DAC Update Rate	Number of Outputs
MAX5891	16-Bit, 600Msps High-Dynamic Performance DAC with LVDS Inputs	16	600 MSPS	1
MAX5890	14-Bit, 600Msps High-Dynamic Performance DAC with LVDS Inputs	14	600 MSPS	1
MAX5889	12-Bit, 600Msps High-Dynamic Performance DAC with LVDS Inputs	12	600 MSPS	1
MAX5895	16-Bit, 500Msps Interpolating and Modulating Dual DAC with CMOS Inputs	16	500 MSPS	2
MAX5894	14-Bit, 500Msps Interpolating and Modulating Dual DAC with CMOS Inputs	14	500 MSPS	2
MAX5893	12-Bit, 500Msps Interpolating and Modulating Dual DAC with CMOS Inputs	12	500 MSPS	2
MAX5888	3.3V, 16-Bit, 500Msps High-Dynamic Performance DAC with Differential LVDS Inputs	16	500 MSPS	1
MAX5887	3.3V, 14-Bit, 500Msps High-Dynamic Performance DAC with Differential LVDS Inputs	14	500 MSPS	1
MAX5886	3.3V, 12-Bit, 500Msps High-Dynamic Performance DAC with Differential LVDS Inputs	12	500 MSPS	1
MAX5878	16-Bit, 250Msps High-Dynamic Performance, Dual DAC with LVDS Inputs	16	250 MSPS	2
MAX5877	14-Bit, 250Msps High-Dynamic Performance, Dual DAC with LVDS Inputs	14	250 MSPS	2
MAX5876	12-Bit, 250Msps High-Dynamic Performance, Dual DAC with LVDS Inputs	12	250 MSPS	2
MAX5885	3.3V, 16-Bit, 200Msps High-Dynamic Performance DAC with CMOS Inputs	16	200 MSPS	1
MAX5884	3.3V, 14-Bit, 200Msps High-Dynamic Performance DAC with CMOS Inputs	14	200 MSPS	1
MAX5883	3.3V, 12-Bit, 200Msps High-Dynamic Performance DAC with CMOS Inputs	12	200 MSPS	1

In order to be able to place the image signals as far as possible from the original signal, lower the noise level and increase the resolution, the DACs with the higher update rates and input bit numbers are to be employed. Therefore our approach was to select one of the 12-14-16 bit families with the highest update rate. However DAC families with update rates higher than 500 MSPS of both companies were newly released to the market at the time of selection. Thus their SFDR and SNR performance definitions were not clear. This directed selection procedure to focus on Analog Device's 400 MHz DAC and Maxim's 500 MHz DAC families.

Analog Device's 16 bit 400 MSPS AD9777 and Maxim's 16 bit 500MSPS DAC were compared. At this point since SFDR and SNR are our dominant selection criteria, SFDR performances of these DACs were compared. The SFDR performance graphics found in the datasheets of these two DAC are shown in Figure 5.1.

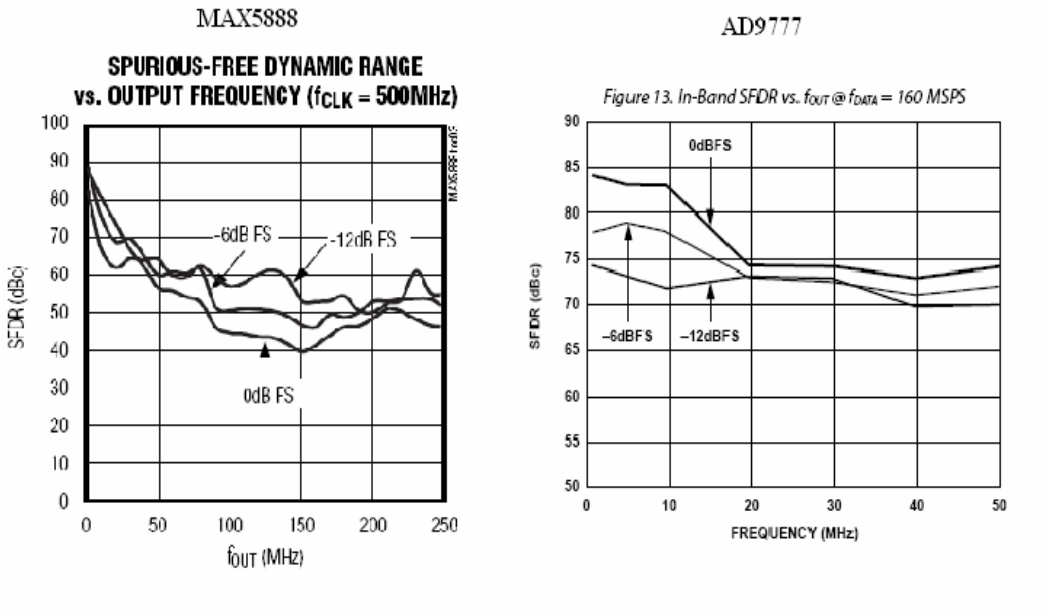


Figure 5.1 SFDR performance graphs of Max5888 [20] and AD9777 [21]

DACs can adjust their output current levels. The normalized output power of a DAC corresponding to its maximum output current is called the full scale (FS) power. The SFDR performances of DAC vary according to the currents they are driving. Therefore, there are three SFDR plots in Figure 5.1 for each DAC. These plots are drawn according to 3 different output current levels such as all, half and one fourth of their maximum current. These current levels result in 0dB, -6dB and -12dB output power levels relative to the full scale output power respectively.

Using Figure 5.1, now let us take their worst SFDR performances as reference and compare them. DAC MAX5888's 0dB FS and DAC AD9777's -12dB FS plot will be compared. At 25 MHz output, AD9777's SFDR performance is approximately 73dB which is 10dB better than MAX5888. At 50MHz output, AD9777's SFDR performance is 70dB which is 15dB better than MAX5888. Therefore it is clearly observed that the SFDR performance of AD9777 is better than that of MAX5888 up to 50 MHz. Moreover after 50MHz the dynamic performance of AD9777 is in a tendency of increasing its SFDR over 70dB which is 15dB better than that of MAX5888. Besides AD9777 includes interpolator and upconverter circuits embedded in the integrated circuit which give the designer flexibility to produce signals at the baseband.

According to these comparisons and observations, we decided to focus on AD9777. To start with, the Evaluation Board (EB) of AD9777 was purchased in order to test and verify the performance of AD9777.

The SFDR performance of AD9777 is verified by testing the SFDR performance of AD9777 at three different frequencies. The spectrum

analyzer E4440A of Agilent is used to analyze the spectrum of the AD9777 at these three different frequencies. Firstly a sinusoidal at 40MHz is produced. In Figure 5.2 the spectrum of the AD9777 40MHz output is shown.

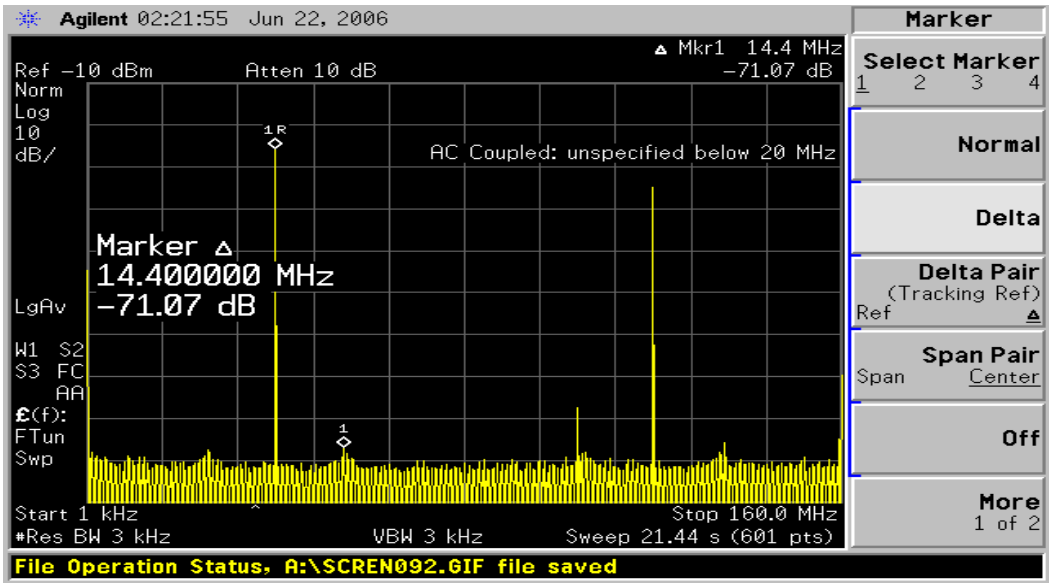


Figure 5.2 AD9777's SFDR performance at 40MHz

First of all since we are producing sinusoidal signals, we are expecting pulses placed at those frequencies in the spectrum. In Figure 5.2 there are three significant pulses. Our sampling frequency is 160MHz and the spectrum analyzer is spanning frequencies up to 160 MHz starting from 1kHz. The first significant peak is placed at 40MHz which is our desired signal. Secondly the image of this signal is placed at 120MHz (160MHz-40MHz), the second biggest peak on the right. Although these signals are expected signals and not spurs, the peak standing in between these two peaks at approximately 104MHz is a spur. The SFDR measurements are made up to Nyquist

Band; therefore spurs up to 80MHz should be considered. Up to 80MHz there are very small spurs almost hidden in the noise. The dynamic range between 40MHz signal and the spurs is 71.07dB as shown by markers. This dynamic range verifies the SFDR characteristic of AD9777 at 40MHz.

Secondly 67.5MHz single tone is produced with AD9777 whose spectrum is shown in Figure 5.3. A marker is placed on the 67.5MHz sinus peak. Sampling rate is 270MHz so image is placed at 202.5MHz, the second biggest peak on the right. Finally the signal in the middle of these two peaks is the first harmonic of 67.5MHz signal placed at 135MHz. The difference between the 67.5MHz signal and first harmonic is 68dB. SFDR measurements are usually made in the Nyquist Band which is 0-135MHz band in our case. The noise floor is placed at 84dBm and no other spurs can be observed over the noise floor resulting in approximately 82dB SFDR at 67.5MHz.

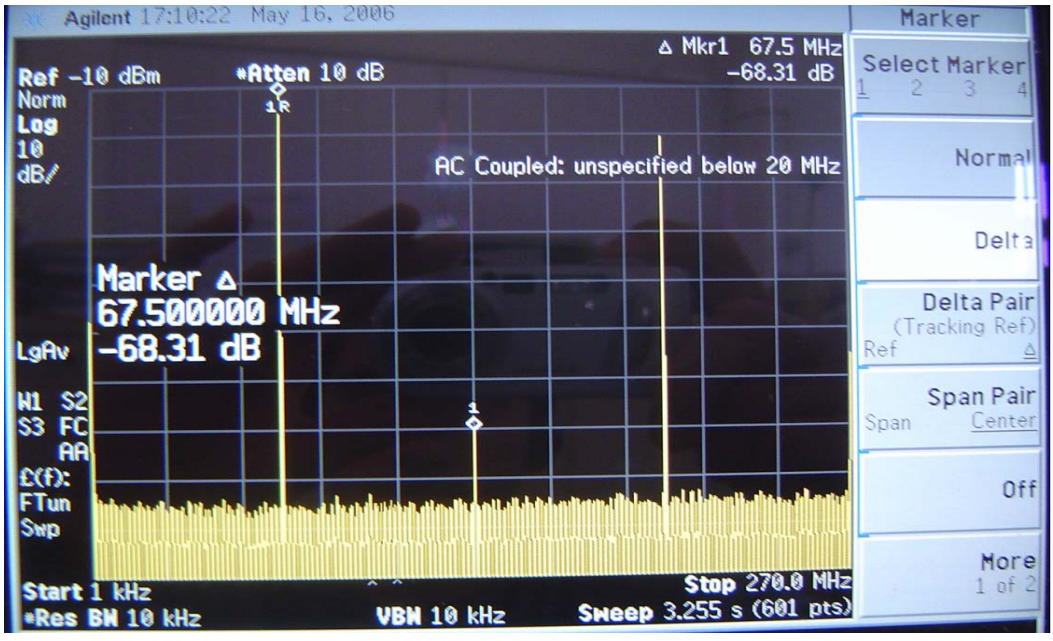


Figure 5.3 AD9777's SFDR performance at 67.5MHz

Finally 100MHz sinus is produced with AD9777. The spectrum of 100MHz sinus is shown in Figure 5.4.

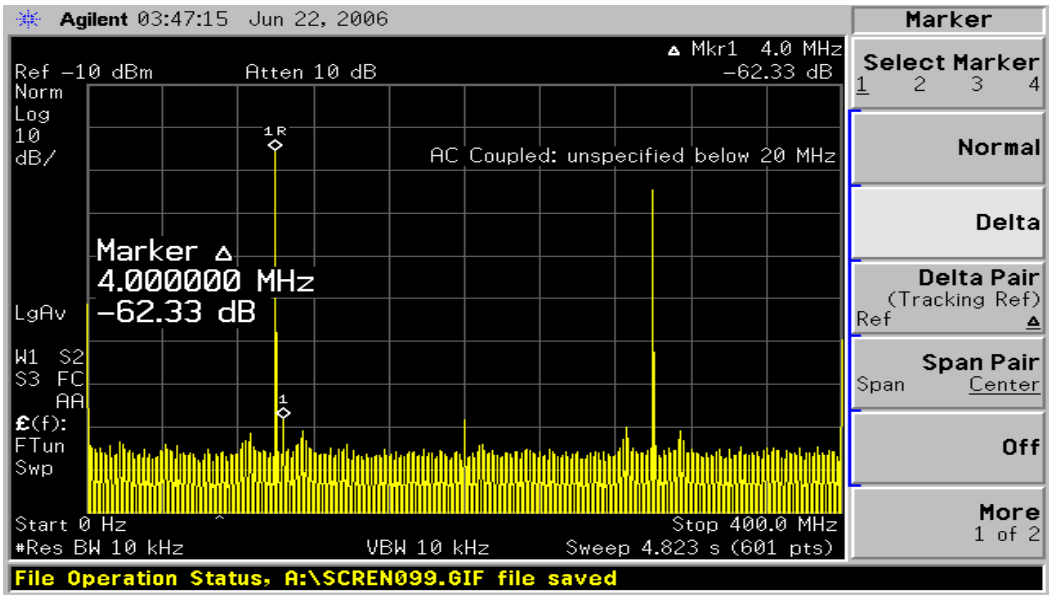


Figure 5.4 AD9777's SFDR performance at 100MHz

Again in Figure 5.4, real and imaginary signals are seen. However in this spectrum, there is also a 62.33dB weaker spur inside the Nyquist Band which is placed 4 MHz apart from 100MHz signal, shown by markers. At this point it is important to remind that this 104MHz spur is also seen in spectrum of 40MHz. The sampling rates and output frequencies are different for these two cases however 104MHz spur appeared in both of them. It could be sensed that 104MHz signal can be interference instead of being a spur of DSS system. On the other hand this spur still does not violate our 60dB SFDR requirement.

AD9777's SFDR performance measurements at various frequencies in our setup verified that both the SFDR performances given in AD9777's datasheet are realizable and the SFDR performance of AD9777 matches our system requirements. Therefore, implementation of the targeted digital signal synthesizer is continued with AD9777 Evaluation Board.

5.3 HARDWARE SETUP

In order to construct a digital synthesizer setup, the AD9777 evaluation board is connected to a FPGA board whose functional block diagram is seen in Figure 5.5. The board includes a Spartan XC3S200 (Xilinx) FPGA on it. Spartan-3 series of Xilinx are cheap and middle capacity FPGAs. XC3S200 consists of 4,300 logic cell equivalents, 216Kb RAM, twelve 18x18 multipliers, 173 user defined I/O signals and four digital clock managers.

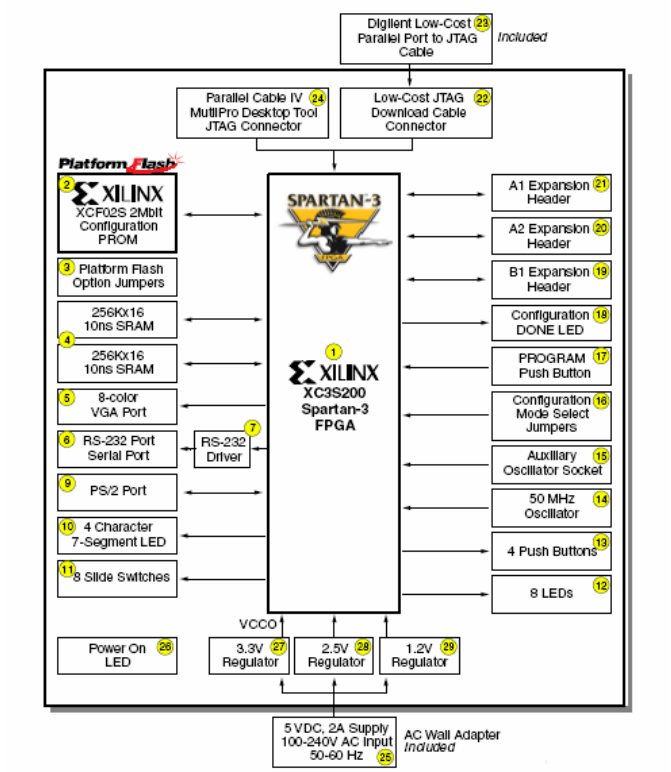


Figure 5.5 Functional block diagram of Spartan Board [22]

In Figure 5.5, the expansion slots among the interfaces of the Spartan Board can be seen. These slots are used to control digital inputs of AD9777 evaluation board. AD9777's digital input's electrical standard is LVTTL. Spartan Board expansion slots are also configured to support LVTTL standard in order to drive AD9777 evaluation board directly.

As seen in Figure 5.6, AD9777 is a two channel DAC. These two channels could be used as two independent channels for direct IF or as orthogonal outputs of a quadrature modulator.

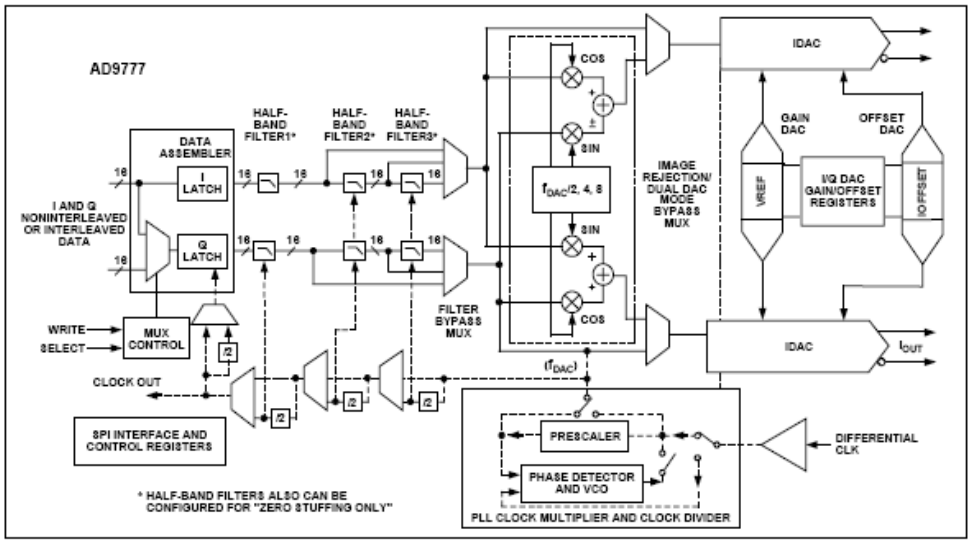


Figure 5.6 Functional block diagram of AD9777's inner architecture

AD9777 has interpolation filters with quadrature modulation capabilities. Input sampling rate of AD9777 is 160 MSPS; however the output could be increased up to 400 MSPS with interpolation filters. There are three filters interpolating the input signal 2 times, 4 times or 8 times, respectively. Following this, quadrature modulators could be used in order to produce the real part of a complex modulated signal. The baseband signal could only be upconverted to $f_s/2$, $f_s/4$ or $f_s/8$ frequencies. These interpolation or modulation functionalities of AD9777 could be programmed using a serial interface.

Moreover AD9777 has a 'Phase Locked Loop' (PLL) circuitry that enables AD9777 to lock to an external clock. In order to synchronize DAC with external digital circuits, AD9777 produces a DATACLK signal which is a shifted version of input clock as seen in Figure 5.7.

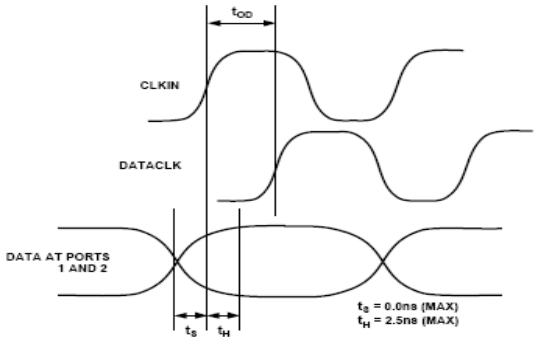


Figure 5.7 Shifted DATACLK

Digital systems have to be synchronized with DATACLK signal for the DAC to sample digital words accurately. Otherwise imprecise sampling causes unexpected outputs. Similarly in order to synchronize the Spartan board and the AD9777 EB, the DATACLK signal produced by AD9777 is used in the Spartan board.

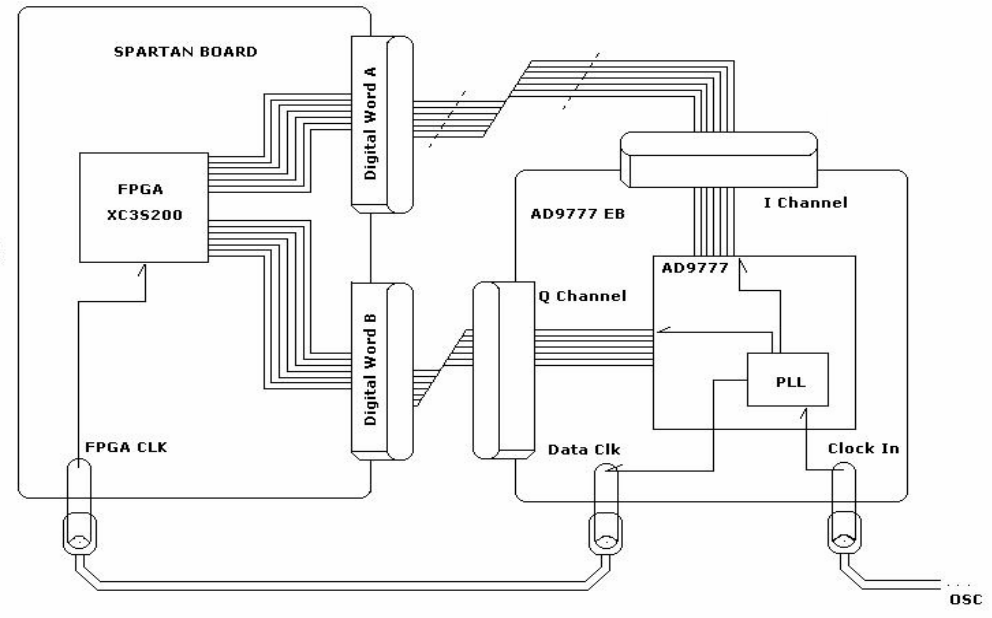


Figure 5.8 Functional block diagram of the hardware setup

The interface in between the Spartan Board and EB could be seen in Figure 5.8. System clock will enter AD9777. AD9777 PLL will be locked to the system clock and distribute necessary system clocks like latch clocks to the inner circuits and DATACLK to the digital control circuits. DATACLK will be carried to the Spartan Board via coaxial cables. The extension connectors of Spartan board will be connected to digital inputs of AD9777 via parallel cables. Since Spartan works with DATACLK, there will not be any erroneous clock latch in the AD9777 input. According to input clock and required system clock, PLL also has the capability of multiplying the system clock to obtain required clocks.

The boards are fixed in a box and shielded. Resulting DSS shown in Figure 5.9. is achieved.

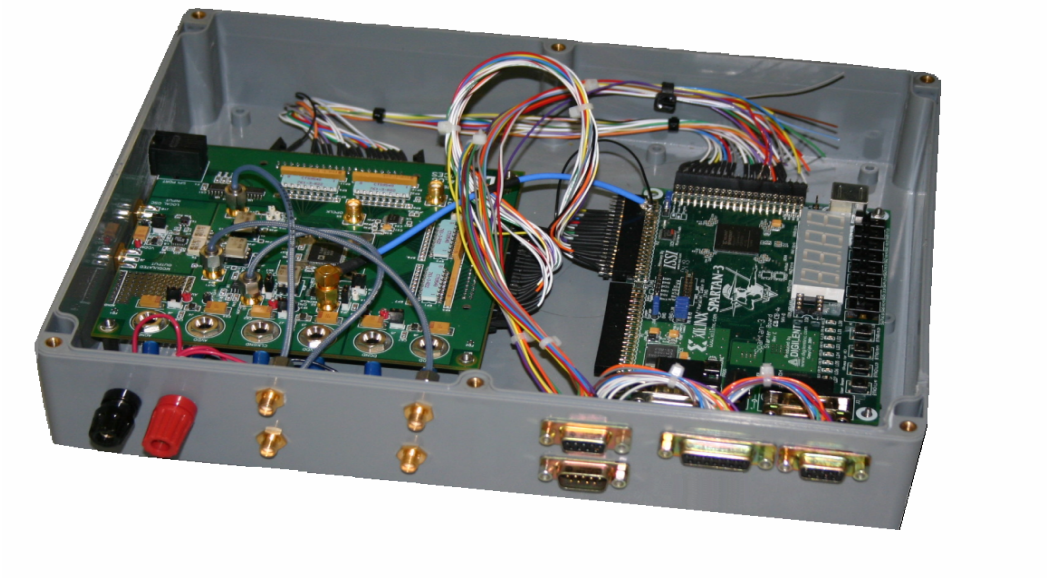


Figure 5.9 The view of the hardware setup

A closer view of the hardware setup is shown in Figure 5.10. In this figure the digital signals, clock, analog outputs, and boards are shown on the figure. This DSS system also includes a RS232 port in order to debug and communicate with a computer.

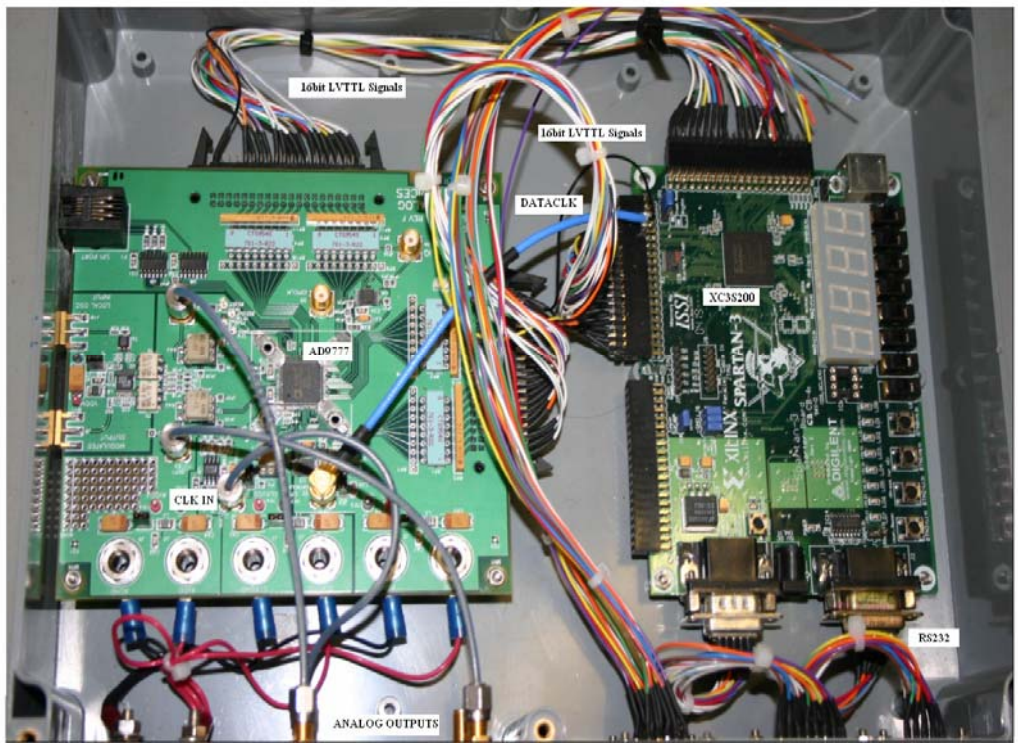


Figure 5.10 A closer look to the hardware setup

During the implementation process, many problems were faced. In the next section these problems will be discussed in order to give a clue about the problems of designing digital and analog signals mixed systems.

5.4 IMPLEMENTATION PROBLEMS

Design of analog mixed digital circuits is an important and difficult problem. This problem becomes even harder while designing a system with a 60dB SFDR. Since the SFDR performance of a system could also be distorted by coupling of other analog signals in a system or EMI.

In this thesis, we tried to design a system which is resistant to coupling of unwanted analog signals and distortion of digital circuits. Designing such a system requires a careful planning. Since this problem is very complicated and too wide to be considered in this thesis in detail, only main points of the possible problems will be explained in this section.

First of all, the system must not be affected by EMI. Since there are low voltage TTL signals carried with approximately 25cm cables, this system is quite open to EMI such as radio broadcast which is quite close to our system's operating frequencies. After this system is implemented, all signals spread over the radio frequency range is observed in the spectrum of the output. In order to overcome this problem, the system is shielded with another grounded box.

Secondly, analog signals are also quite open to city supply couplings. If the supply circuits of the system are not filtered, then 50Hz couplings around the carrier signals could be observed. This 50Hz not only causes an amplitude modulation but also increases the phase noise. Therefore our system supplies are highpass filtered in order to cancel this effect.

Another problem that may be observed is the increase of noise level because of the digital circuits. Since digital circuits constantly pull and raise current, a noise is generated on the return path of the current. If a board mixed with analog and digital circuits is designed, then the ground plane of the board will be polluted with this noise, raising the noise level of analog signal. Since separate boards are used for analog and digital circuits in our system, the noise level of AD9777 is not directly affected by the noise formed by digital circuitry.

During the measurements with oscilloscopes, an amplitude modulation was observed on the output signals even after all the precautions were taken. Later it was realized that the amplitude modulation seen on the oscilloscope was caused by unlocked sampling clock of the oscilloscope. Since the oscilloscope was not locked to the system clock, sampling at a different phase caused this amplitude modulation.

As a result, implementation of a DSS system is successfully completed. In Chapter 6, analysis of this DSS will be made with different system configurations. These implementations will help understand the characteristics of digital signal synthesizers in a deeper way.

CHAPTER 6

MEASUREMENTS AND VERIFICATIONS

6.1 GENERAL

Up to this chapter theoretical and practical parameters of DSS systems were discussed. Using these parameters and considering system requirements put forth in this thesis, a Digital Signal Synthesizer is implemented as mentioned in Chapter 5.

In this chapter the spectral and time domain analysis of the signals produced by this DSS system will be made. Firstly periodic QPSK signals modulated at a rate of 7.5MHz and upconverted to 67.5MHz with 60dB SFDR are to be produced. These signals will be examined in order to observe sinc effects of sample-hold, image and harmonic signals, glitch effects, SNR and SFDR performances in a real hardware setup. Later a randomly generated QPSK signal will be produced in order to observe smooth spectral sinc lobes. Moreover we will try to observe and make a comparison of the magnitude of amplitude modulation that is going to appear on the synthesized signals according to band limitations of different analog filters.

6.2 PARAMETERS OF HARDWARE SETUP

Assessment of important system parameters is made in Chapter 3. Based on that study, hardware configuration of 67.5MHz QPSK modulated signal synthesizer will be investigated in this section in

order to verify that our hardware setup matches the analog performance requirements targeted in this thesis.

Moreover, again referring to Chapter 3 and system requirements, how the sampling frequency is chosen will be explained and the effects of the system clock on analog performance will be examined.

Our system is desired to have a 60dB SFDR. In order to match this, we must ensure that DDS and DAC blocks match these requirements. In Chapter 4, it is shown that DDS LUT table width can be chosen as 16 bits resulting in a worst case phase truncation spur with -96dBc according to calculations given in Chapter 3.2.3. Besides, DDS output bit number which is the DAC input bit number is chosen as 16, resulting in a -97.76dBc quantization noise again according to calculations in Chapter 3.2.1. In addition to these, as discussed in Chapter 5 spur levels observed in the real outputs of AD9777 EB verified that SFDR performance of the DAC AD9777 is quite higher than 60dB and matches the system requirements.

The desired modulated signal should be upconverted to 67.5MHz. In order to place the band of the modulated signal in the linear region of the sinc function caused by sample-and-hold operation, the highest frequency of the signal band must be smaller than 0.4 times the sampling frequency. Since our symbol rate is 7.5MHz, our highest frequency component will be 75MHz theoretically. This results in 187.5MHz sampling frequency in order to avoid the sinc effect. However, since we want to decrease amplitude modulation caused by band limitation, we will try to increase analog filter's bandwidth around 67.5MHz as much as possible. In order to be able to widen the band, the image signal must be placed apart from the main signal as much as possible resulting in a possible increase of

sampling frequency. Considering the inner architecture of DAC AD9777, we choose the sampling frequency as 270MHz which is an integer multiple of 67.5MHz. Previously it is mentioned in Chapter 3 that if the sampling frequency is an integer multiple of output frequency, then spur power will be concentrated on harmonics of output signal. It is observed that even if the spur power is concentrated on the harmonics by choosing the sampling frequency as four times the output frequency, SFDR level is still below 70dB.

One last important system parameter is the jitter and phase noise performance of the system clock. Since clock phase noise is additive to output noise level, the system noise is desired to have a better phase noise performance than the SNR requirement. In order to match this requirement Analog Signal Generator of Agilent E8257D is used. Phase noise is usually measured for different frequencies apart from the carrier frequency. The worst phase noise of E8257D is measured to be -75dBc/Hz at 100Hz and matches the system requirements.

6.3 PERIODIC QPSK SIGNAL

We will produce a phase modulated signal and upconvert it to 67.5MHz. The phases such as $\pi/4$, $3\pi/4$, $5\pi/4$ and $7\pi/4$ radians are used to modulate 67.5MHz signal. This phase sequence is used repetitively to modulate the output signal resulting in a periodic pattern. Each phase is represented by a rectangular window of 133ns width at the baseband resulting in a 7.5MHz symbol rate at the output.

This periodic QPSK modulated signal is produced by firstly producing I and Q components of the phases and upconverting them

to 67.5MHz. The amplitude of the rectangular phase word is taken as *1.414A* where A is a constant, resulting in *1A* or *-1A* I and Q components according to phase sequence mentioned above.

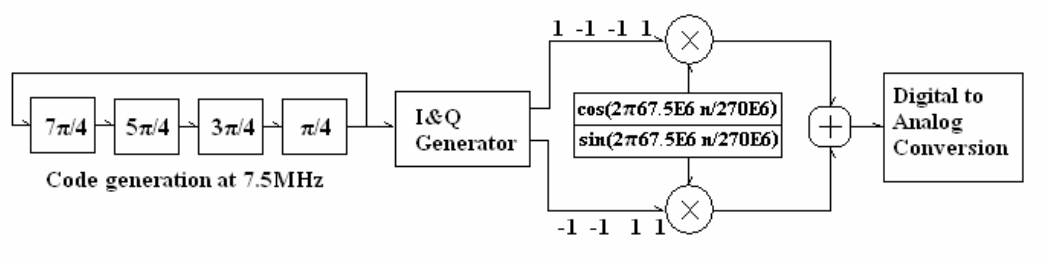


Figure 6.1 Periodic QPSK modulating DSS

In Figure 6.1, the functional block diagram of the hardware setup producing the required modulation and upconversion is shown. The phase information is an input to the system. The I&Q modulator generates rectangular windows for a duration of 133ns (7.5MHz symbol rate) multiplied with the I and Q.

The time domain unfiltered output of this system is observed by using a digital oscilloscope as seen in Figure 6.2. At this point, it is important to emphasize that the time domain observations of all systems implemented in this thesis are made by using a 1GSPS digital oscilloscope and since digital oscilloscopes are also samplers, some quantization errors caused by oscilloscopes could be observed in the time domain.

Figure 6.2 is a direct plot of the DAC output. Since the output of the synthesizer is not filtered and the sampling frequency is four times the carrier frequency, sharp transitions and a square wave are

observed. Unstable areas marked with white circles are the phase transition instants which are also sharp since the spectrum of the plotted signal is quite wide resulting in sharp transitions in time domain.

If the time scale is carefully observed, it will be seen that constant phase durations which are the periods in between two white unstable phase transition instants, are 133ns. Moreover the markers are 133ns apart from each other and are pointing different phases. Thus while one marker is pointing the peak of the sinusoidal, the other is pointing zero since there are 90 degree phase difference in between two consecutive phases.

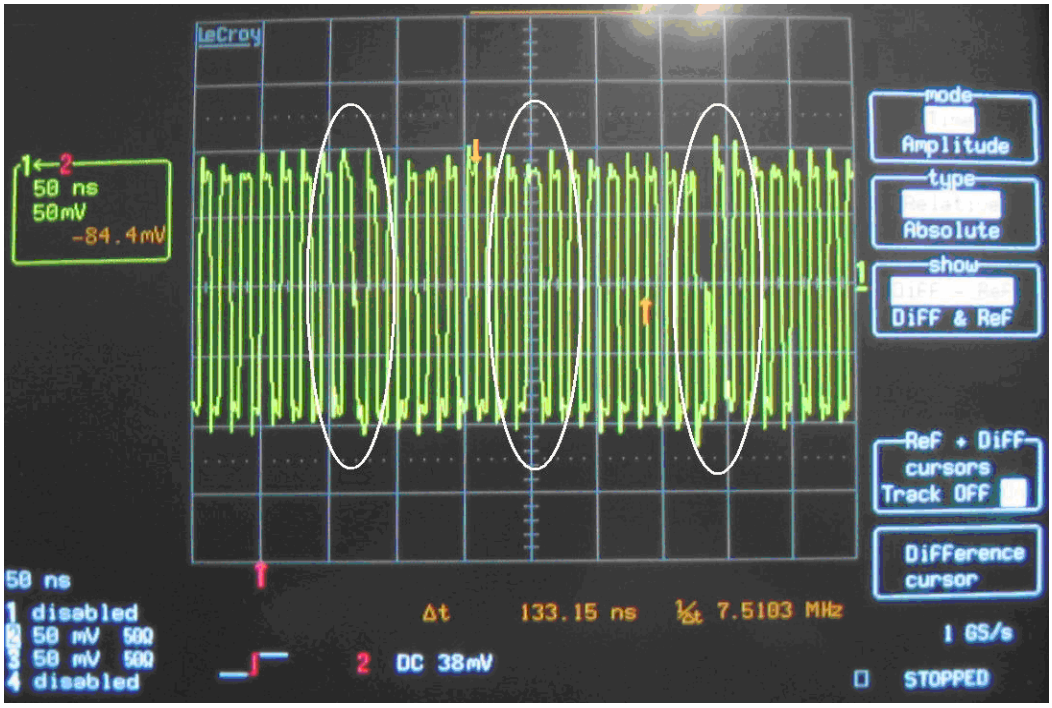


Figure 6.2 A snapshot of unfiltered, QPSK modulated signal

In Chapter 2, the glitch effect is mentioned. Now in time domain analysis, these glitches are easily observed. The small peaks seen in Figure 6.2 on each rising or falling edge are the glitches.

Being modulated with the same phase sequence repetitively, upconverted signal is a periodic signal with a period of 133*4, 532ns which is 1.875MHz. Since this signal is periodic, the spectrum of this signal is expected to be formed of pulses separated by 1.875MHz [16]. Referring to derivations in Chapter 2.4, the spectrum of a signal produced by a digital synthesizer is as follows,

$$X_{SH}(f) = \frac{1}{2}\sum_{m=-\infty}^{\infty}[X_{lp}(f - f_c - mf_s) + X_{lp}^{*}(-f - f_c + mf_s)]\, sinc\,(\frac{f}{f_S}) \tag{6.1}$$

In the equation above, mathematical representations of sampling and the sample-and-hold effect are shown. However, in order to be able to use this equation to obtain the spectrum of a periodically modulated 67.5MHz signal, *X(f)* in the equation should be replaced with the mathematical representation of a periodic signal.

The Fourier Transform of a periodic signal is,

$$X_p(f) = \sum_{k=-\infty}^{\infty} X[k]\delta(f - kf_p) \tag{6.2}$$

where *X[k]* is Fourier series coefficients and f_p is the frequency of periodicity. Substituting $X(f)$ with $X_p(f)$ results in,

$$X_{SH}(f) = \frac{1}{2}\sum_{m=-\infty}^{\infty}\sum_{k=-\infty}^{\infty}[X[k]\delta(f - f_C - kf_p - mf_s) + X^{*}[k]\delta(-f - f_C + kf_p + mf_s)]\, sinc(\frac{f}{f_S}) \tag{6.3}$$

In order to find the exact placement of the pulses in the spectrum, we insert the frequency values into the eqn. 6.3 resulting in:

$$X_{SH}(f) = \frac{1}{2}\sum_{m=-\infty}^{\infty}\sum_{k=-\infty}^{\infty}\left[X[k]\delta\left(f - 67.5*10^{6} - k1.875*10^{6} - m270*10^{6}\right) + X^{*}[k]\delta\left(-f - 67.5*10^{6} + k1.875*10^{6} + m270*10^{6}\right)\right] sinc\left(\frac{f}{270*10^{6}}\right) \quad (6.4)$$

It could be deduced from eqn 6.4 that the spectrum will consist of pulses equally placed 1.875MHz apart from each other. In addition, images of the signal will be placed around multiples of the sampling frequency. From eqn 6.4 we could expect that the spectrum of the signal will be shaped by the sinc function.

Moreover it should be noted that since phase words are pulse code modulated with rectangular windows in time domain, the spectrum of the output signal or in other words Fourier series coefficients, *X[k]*, should be samples of a sinc function of 7.5MHz.

Now let us observe and verify these theoretical findings in the spectrum analyzer. In Figure 6.3 the spectrum of DSS output is seen up to 1.08GHz.

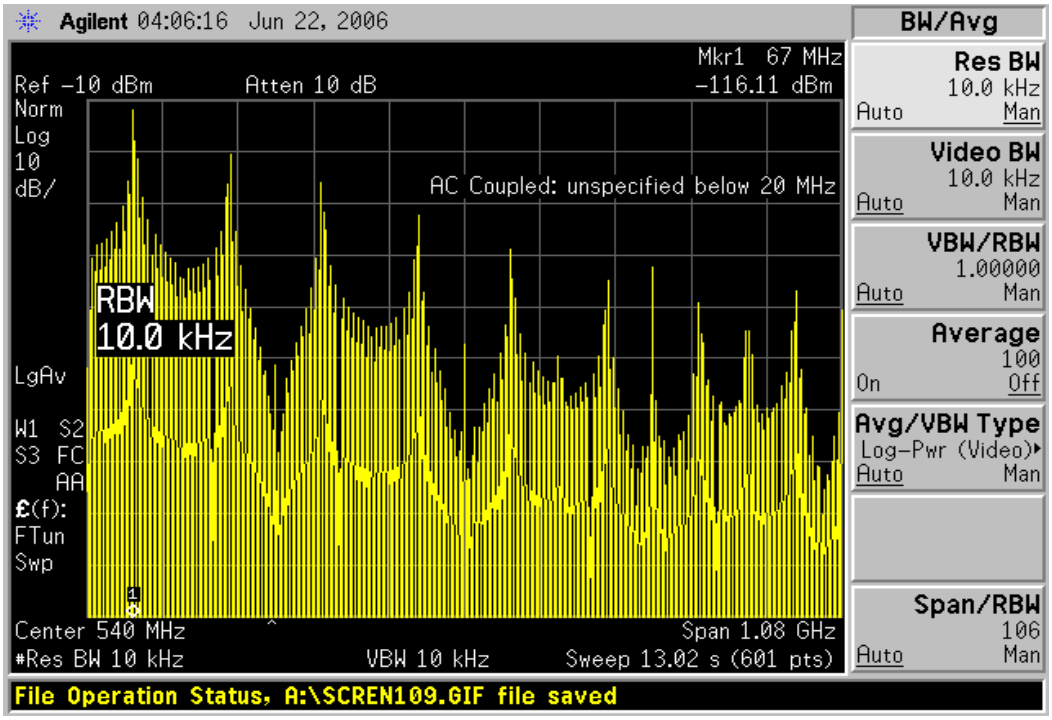


Figure 6.3 The spectrum of QPSK modulated signal up to 1GHz which is periodic with 4 codes

As seen in Figure 6.3 general envelope of the spectrum is shaped with sample-hold sinc function and zeros of this function are placed at 270MHz, 540MHz, 810MHz and 1080 MHz since our sampling frequency is 270MHz. Moreover the signal centered at 67.5MHz, the first marker, is the desired signal and images of this signal are placed at 202.5MHz, 337.5MHz, 472.5MHz, 607.5MHz, 742.5MHz and 877.5MHz verifying our image signal placement expectations at frequencies $|\pm K.f_S \pm n.f_O|$. Again in the same figure, attenuation on these image signals caused by sample-hold sinc function could be observed. Finally the bands surrounding these signals are shaped with another sinc function since phase words are pulse code modulated with rectangular windows in time domain with a rate of 7.5MHz. This sinc function will be observed in Figure 6.4 better.

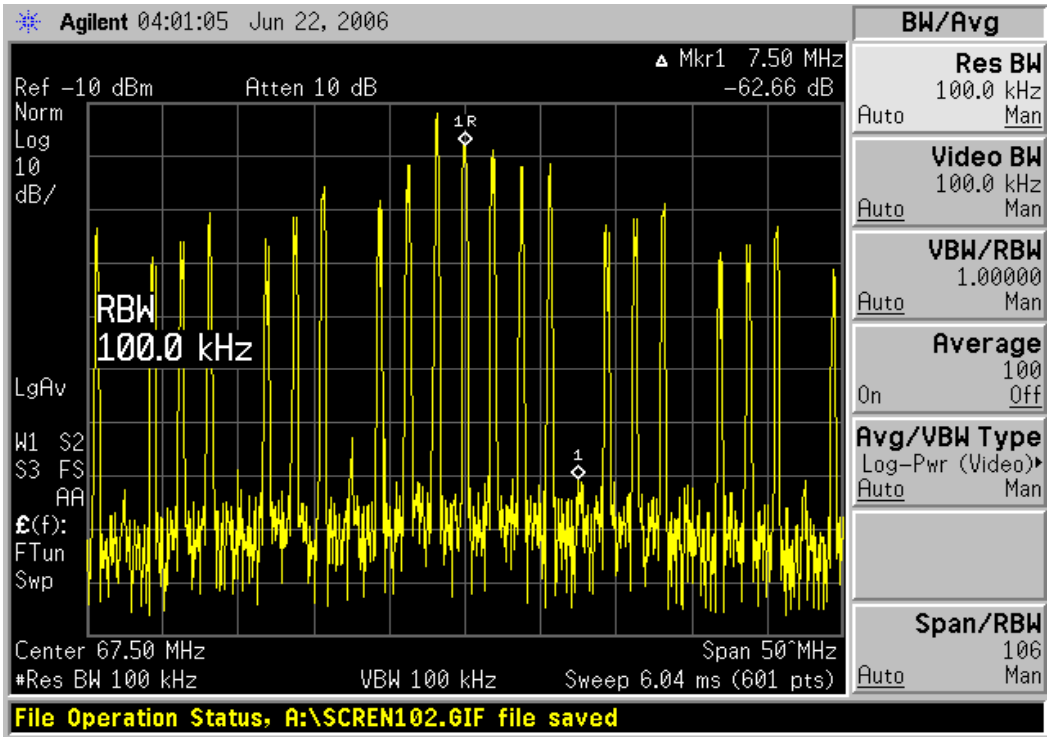


Figure 6.4 The spectrum of QPSK modulated signal around 67.5MHz which is periodic with 4 codes

In Figure 6.4, the pulses caused by the periodicity of the phase sequence could be observed better. The pulses are placed 1.875MHz apart from each other. The zeros seen on the figure are the zeros of the sinc function which is the Fourier Transform of the rectangular window used to pulse code modulate the phase words at a rate of 7.5MHz. To conclude, the band of the QPSK modulated signal at 67.5MHz signal is shaped with a sinc function whose zeros are placed at integer multiples of 7.5MHz around 67.5MHz. Since pulses are placed 1.875MHz apart from each other, one sinc lobe of the band represents three pulses.

Now let us increase the number of codes in one phase sequence to 7 codes instead of four codes.

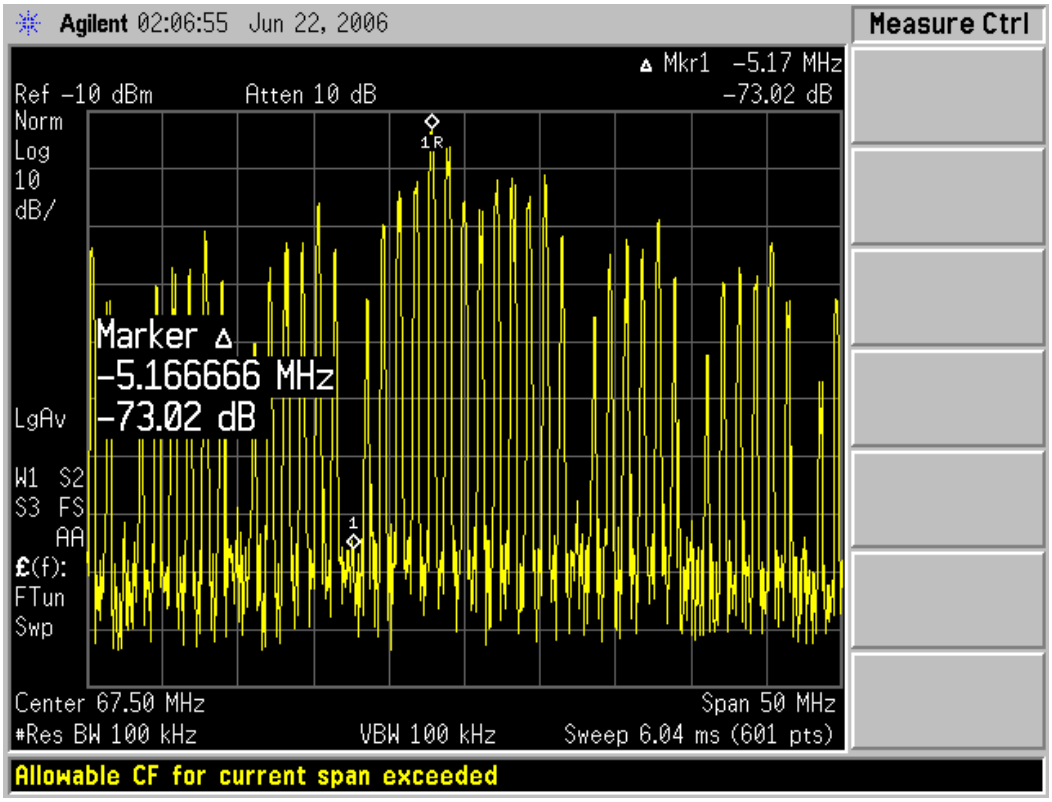


Figure 6.5 The spectrum of QPSK modulated signal around 67.5MHz which is periodic with 7 codes

Since the length of the sequence increases, the frequency of the phase repetition decreases resulting in closer pulses in the spectrum as seen in Figure 6.5. The samples are placed 1.07MHz apart from each resulting in a better observation of 7.5MHz wide sinc lobes.

In Figure 6.3, envelope of the sample-hold sinc effect is shown up to 1GHz. Now in Figure 6.6 this sinc effect will be analyzed up to 270MHz in order to analyze if this sinc function is effective on the modulated signal's band.

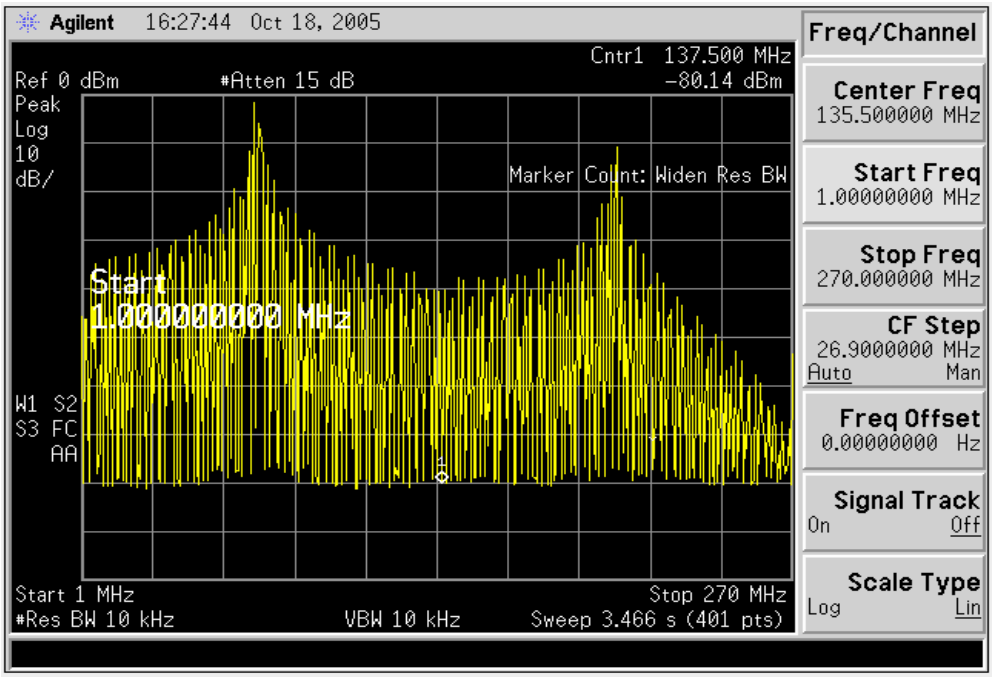


Figure 6.6 The spectrum of QPSK modulated signal up to 270 MHz which is periodic with 7 codes

As seen in Figure 6.6, the sinc effect is significant after approximately 170-180Mhz. If we choose our signal's bandwidth 60MHz (The decision of bandwidth will be discussed in section 6.5), the last frequency that should be filtered with analog filter is around 67.5+30=97.5 which is quite far away from the frequencies where significant effect of sinc is observed. Moreover in Chapter 3.2.6 it is mentioned that the sinc function is not too significant until 0.4 f_s. For 270MHz, we can say that sinc magnitude response does not bring a significant distortion up to 108MHz. Our signal's band is the 37.5-97.5MHz region and less than 1.7dB attenuation exits in this region. This attenuation level is normal even inside the passband of an analog filter. Besides this sinc effect can also be compensated with an analog filter.

At this point, another advantage of higher sampling rate is clearly observed. The sinc effect is not significant even for a wideband signal inside the Nyquist Band. Therefore, it could be concluded that the sampling frequency decision made during DSS design is correct.

6.4 RANDOM QPSK SIGNAL

Up to this section, periodic QPSK modulated signals are produced resulting in sampled spectrum. However, in order to observe sinc patterns clearly and also to verify patterns found in the previous section, we will now use a random code generator. Different from the first system a random code generator is implemented before the I&Q generator as seen in Figure 6.7. In this case, time domain characteristics of the system are the same; however smooth sinc functions are expected to be observed in the spectrum.

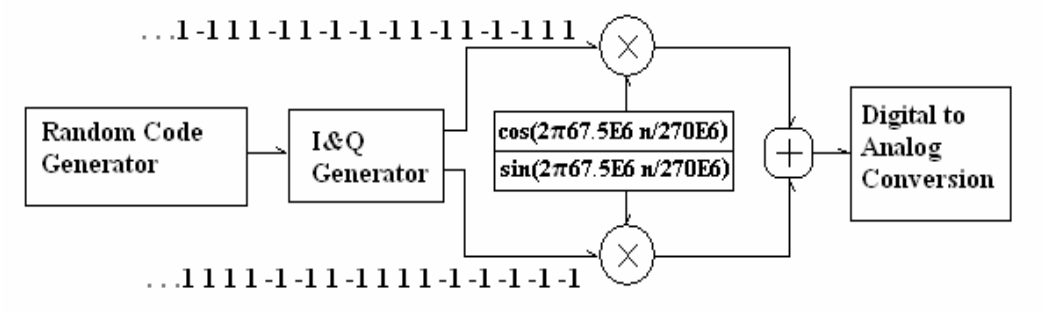


Figure 6.7 Non-Periodic QPSK modulating DSS

In Figure 6.8 and Figure 6.9 classical sinc functions could be observed. In the first figure, the bandwidth of the main lobe is measured. The spectrum is centered at 67.5MHz and the man lobe width is 15MHz as expected. The second plot verifies the constant

13dB difference in between the main lobe and the first side lobe which is also expected for a magnitude response of a sinc function.

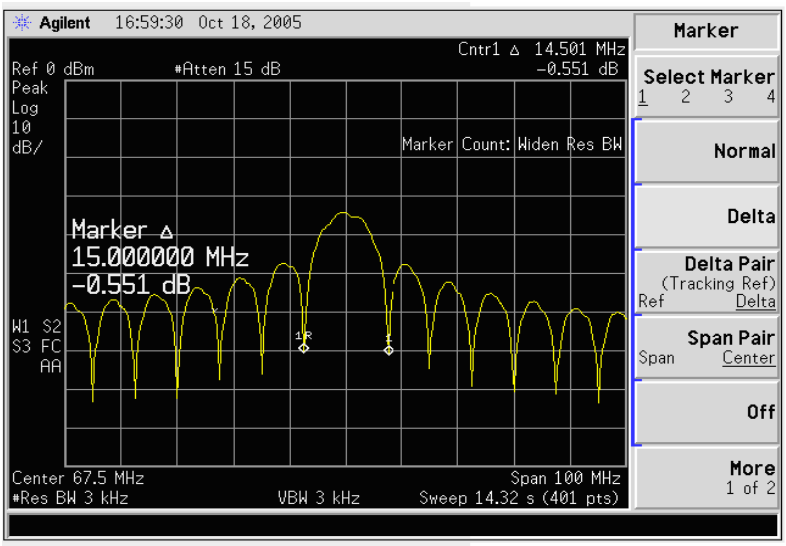


Figure 6.8 Spectrum 1 of non-periodic QPSK modulated signal

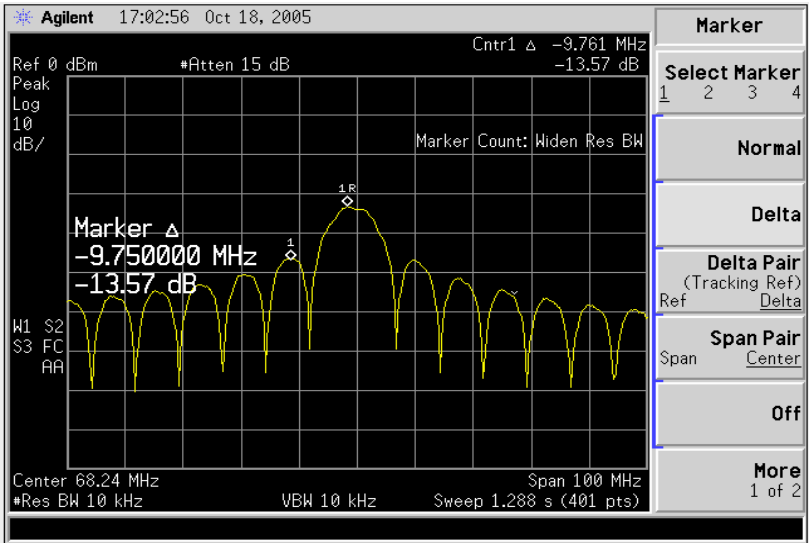


Figure 6.9 Spectrum 2 of non-periodic QPSK modulated signal

When the spectral plots of non-periodic QPSK signal are compared with the plots of periodic QPSK signal, it is seen that spectral envelopes and frequency placements of sinc zeros are consistent with each other.

Similarly, in Figure 6.10 again sample-hold sinc effect and images could be observed in the spectrum of QPSK signal up to 540MHz.

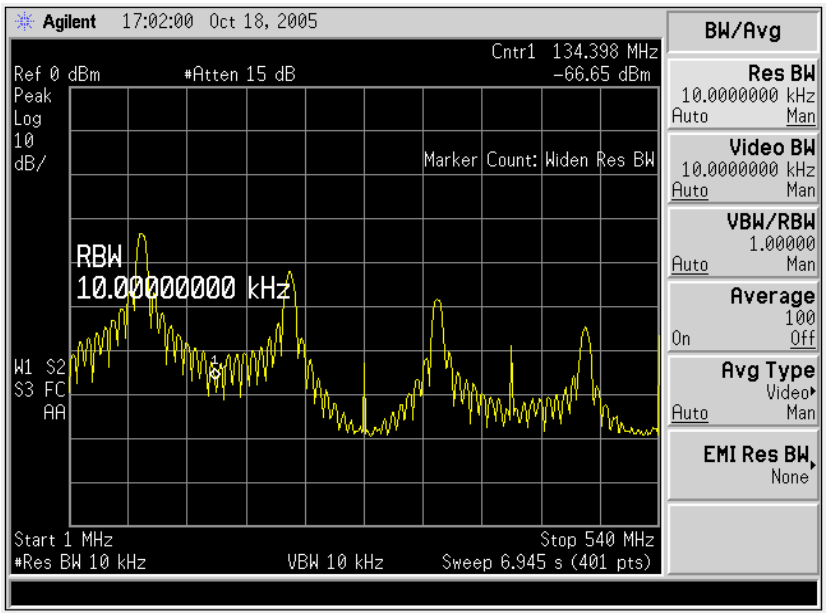


Figure 6.10 Spectrum of non-periodic QPSK modulated signal up to 540MHz

Spectral and time domain characteristics of the designed DSS system are clearly observed in these plots. Moreover correctness of the spectral and time domain outputs according to theoretical results verified the system. However, it should be noted that analog filtering has not been performed yet. In the next section analog filter characteristics will be discussed.

6.5 DISCUSSION OF ANALOG FILTERS

The unfiltered output of a DSS contains sharp transitions resulting in very wide bandwidth and unwanted signals such as images and harmonics in the spectrum. Therefore the DDS output has to be filtered in order to limit the bandwidth, to filter image signals and harmonics, and to smooth the time domain output which effectively means interpolation.

There are basically four parameters that could be used as reference while designing an analog filter. These four parameters are

1) 3dB passband width
2) Suppression amount
3) Transition band width
4) Group delay

The tradeoffs between these parameters are described in Chapter 3.2.7. In our case, bandpass filter has to

1) Be centered around 67.5MHz since our signal is centered at 67.5MHz,
2) Suppress image and harmonic signals at least 60dB since we have 60dB SFDR requirement,
3) Have minimum group delay response in the passband region since higher group delay results in narrower eye diagrams. For our system there is not a definite eye diagram opening requirement; however this is a general problem in communications [23].

Ideally our filter is preferred to suppress 60dB just out of the passband. However this is not possible since in real applications, as mentioned in Chapter 3.2.7, filters require transition bands in order

to increase their suppression levels up to the required levels. Moreover the design of a passband filter with very low group delay, as required in our system, is another problem. In order to be able to decrease group delay in the passband region, we have to increase the transition bandwidth [24], resulting in a considerable higher transition bandwidth. Thus for our system we have to define the transition bandwidth margins before starting to design the filter.

Foreseeing these requirements, highest possible sampling frequency is chosen for our DSS system in order to place harmonics and image signals apart from the desired signal as much as possible. In our DSS system, the closest image signal is placed at 202.5MHz and the closest harmonic which is a considerable 40dB below the main signal is placed at 135MHz. So our filter should suppress at least 20dB around 135MHz and 60dB in the rest of the spectrum.

In addition to these, the AM to PM conversion characteristics of amplifiers are mentioned in Chapter 3.2.7. In the case of using this DSS system with an amplifier that has AM to PM conversion characteristics, AM on the output of DSS has to be decreased as much as possible by passing signal power as much as possible through the filter. Therefore in order to analyze the passband width, we have to analyze where the signal power is concentrated. Since we are using rectangular pulse windows, we have to analyze the power distribution of a sinc function in the spectrum. In order to do that, total power and the power inside the mainlobe and the side lobes are calculated in MATLAB.

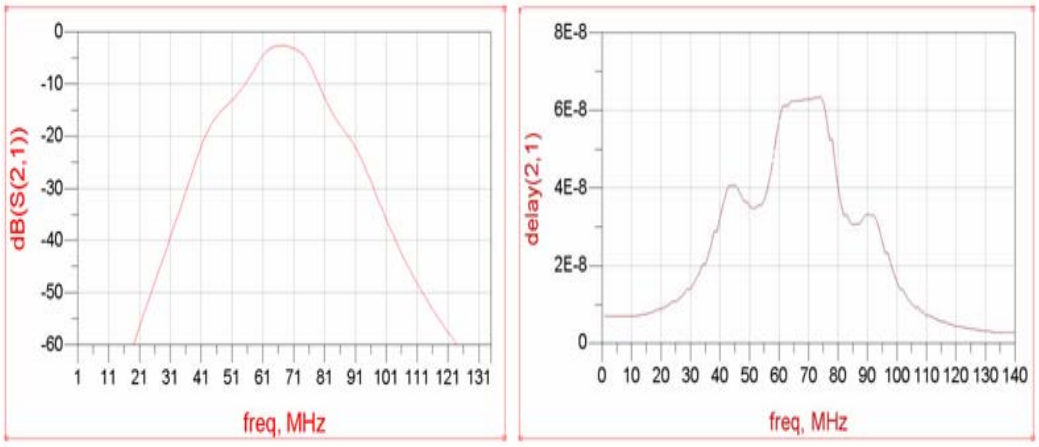
Table 6.1 Power Distribution in the Sinc Envelope

Power Distribution in the Sinc Envelope	
power in	percent of the total power
Mainlobe	91.17%
Mainlobe + 1 sidelobe	95.46%
Mainlobe + 2 sidelobe	96.96%
Mainlobe + 3 sidelobe	97.72%
Mainlobe + 4 sidelobe	98.18%
Mainlobe + 5 sidelobe	98.49%
Mainlobe + 6 sidelobe	98.71%
Mainlobe + 7 sidelobe	98.87%
Mainlobe + 8 sidelobe	99.00%
Mainlobe + 9 sidelobe	99.11%
Mainlobe + 10 sidelobe	99.20%

As seen in Table 6.1, 97.72% of the signal power is concentrated in the main lobe plus three lobes following the main lobe at both sides. Instead of using all power spectrum, it is concluded that filtering the main lobe and three side lobes will be efficient since after the third sidelobe, there is no significant power increase.

Our transition bandwidth criteria are not strict; however if the filter is designed to pass main lobe plus three lobes then the passband width of the filter becomes 7.5*8=60MHz so highest frequency of the passband should be extended to 67.5+60/2=97.5MHz. There is 37.5 MHz gap left up to 135MHz where the first harmonic of the signal is placed at a considerable 40dB below the main signal. Along this 37.5MHz transition band, the analog filter has to increase its suppression at least up to 20dB so that the first harmonic will be 20+40=60dB below the main signal satisfying the SFDR requirement.

Having identified the problem, two filters designed by RF engineers in ASELSAN Inc. are used in the system. Firstly a filter with a passband of 15MHz is used. Figure 6.11 shows the magnitude response and group delay response of this filter. The filter could suppress 60dB after 60MHz transition bandwidth.



(a) (b)

Figure 6.11 (a) Magnitude response (b) group delay of the analog filter with 15MHz passband

Amplitude modulation is observed in the time domain signal as depicted in Figure 6.12. At this point it is important to emphasize that the AM to PM conversion of amplifiers are not additive so the phase distortion is only valid for the instant of AM. Since during the phase transitions, it is difficult to measure AM on the signal, it is decided to measure the AM fluctuation in between phase transitions.

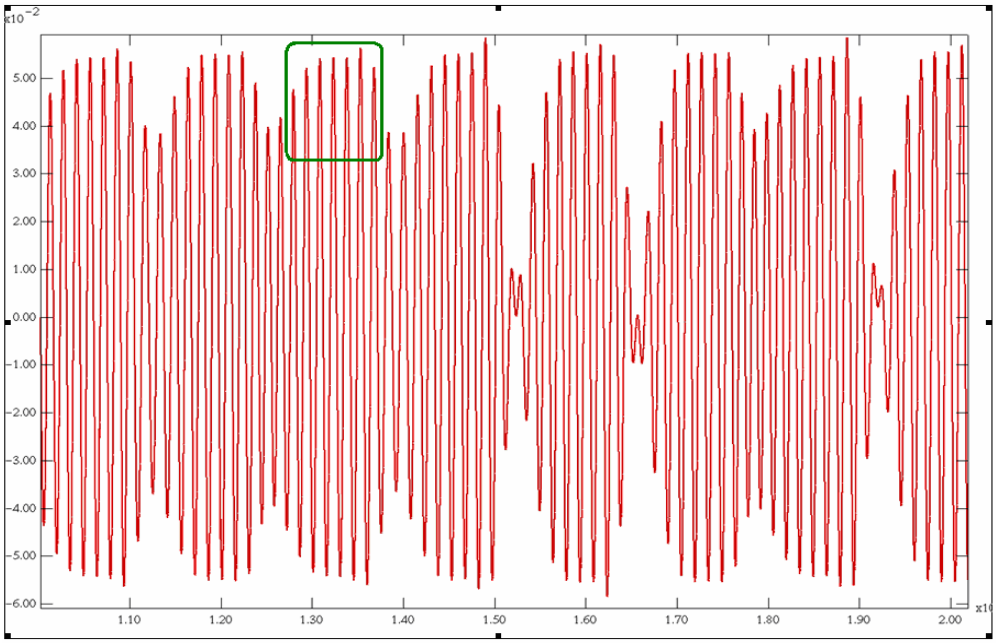


Figure 6.12 Time domain simulation of QPSK signal filtered with the analog filter which has 15MHz passband centered at 67.5MHz

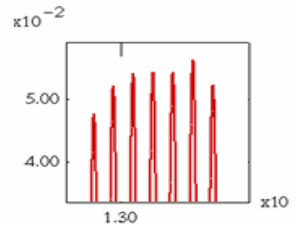
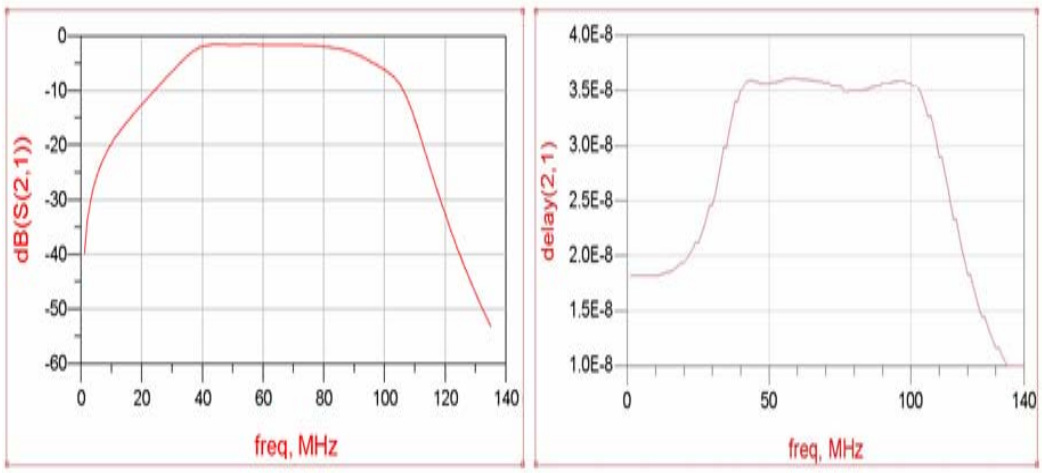


Figure 6.13 Amplitude modulation on the signal filtered with 15MHz passband filter

A closer look at the amplitude modulation inside the constant phase region is given in Figure 6.13 which is the zoom of the rectangular region in Figure 6.12. Had there been no AM, these sinusoidal peaks' amplitudes should have been the same, although there is a variation. The cause of this variation is AM due to the band limitation. The

biggest peak of these peaks is 1.01dB stronger than the rms of these peaks.

Now let us consider another filter whose magnitude response and group delay response can be seen in Figure 6.14. The filter's passband width is 60MHz. This filter is a much more complex filter compared to the previous filter, since this filter can also suppress by 55dB at 135MHz even if it has four times wider passband.



(a) (b)

Figure 6.14 (a) Magnitude response (b) group delay of analog filter with 60MHz passband centered at 67.5MHz

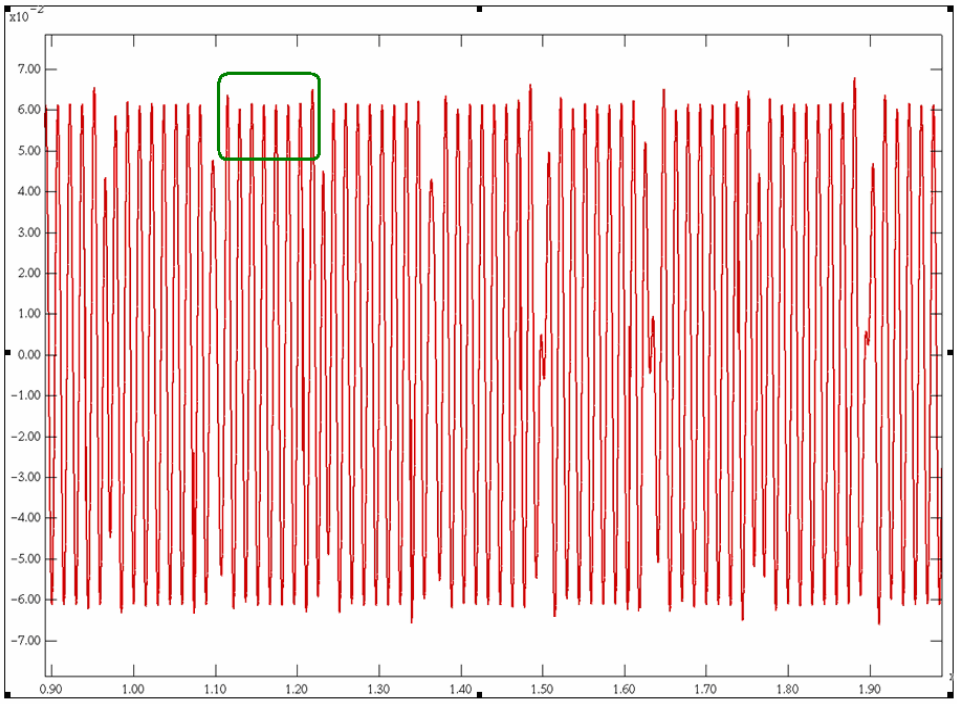


Figure 6.15 Time domain simulation of QPSK signal filtered with the analog filter which has 60MHz passband centered at 67.5MHz

The output of this filter is shown in Figure 6.15. At first sight there is a significant improvement in the variation of the amplitudes in new output compared to Figure 6.12. However let us measure the difference in between the strongest and rms of peaks in Figure 6.16

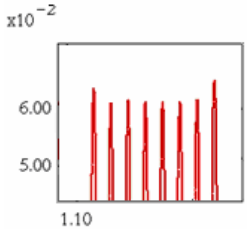


Figure 6.16 Amplitude modulation on the signal filtered with wideband filter

Since the output amplitude fluctuation is decreased, periods of constant phase can be observed better in Figure 6.15. The ratio of the biggest peak of these peaks to the rms of these peaks drops to 0.38dB with this new filter. This significant drop and AM suppression is due to the larger signal power passed through the filter. In summary, amplitude modulation observed in the output signal has a significant drop after increasing the passband width of the filter from 15MHz to 60MHz as expected.

Now let us observe analog filters' effects on the signals produced by our DSS system. The time domain outputs of the random QPSK modulator are stored in the memory of the oscilloscope sampling at 1GSPS and then plotted. In Figure 6.17 500 samples of unfiltered output are plotted.

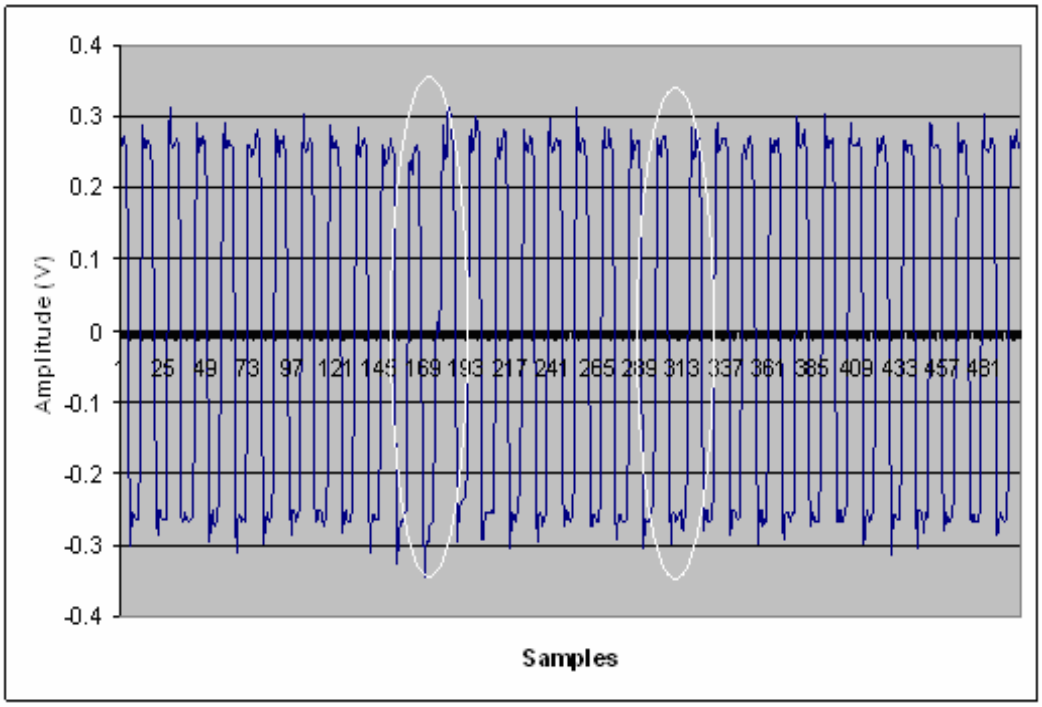


Figure 6.17 67.5MHz QPSK modulated unfiltered signal

In Figure 6.17 two sharp phase transitions can be seen since phase can be immediately changed in digital domain by changing the phase of the next digital word that is going to be converted to analog.

At this point, it should be noted that although DSS can make these sharp phase transitions, analog filtering smoothens the transitions. In Figure 6.18 and Figure 6.19 the real time plots of this system's output filtered with 15MHz passband filter and 60MHz passband filter will be shown, respectively. We are going to compare how AM levels and phase transitions are affected by filtering with two different filters.

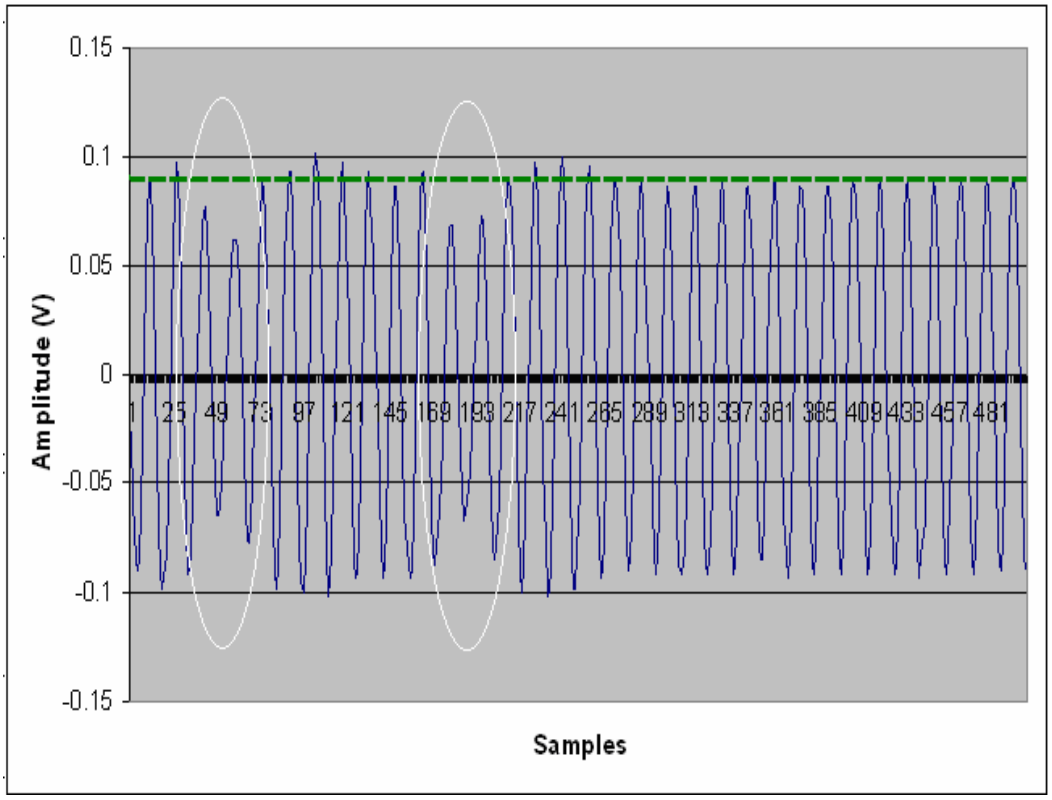


Figure 6.18 Output is filtered with 15MHz passband filter

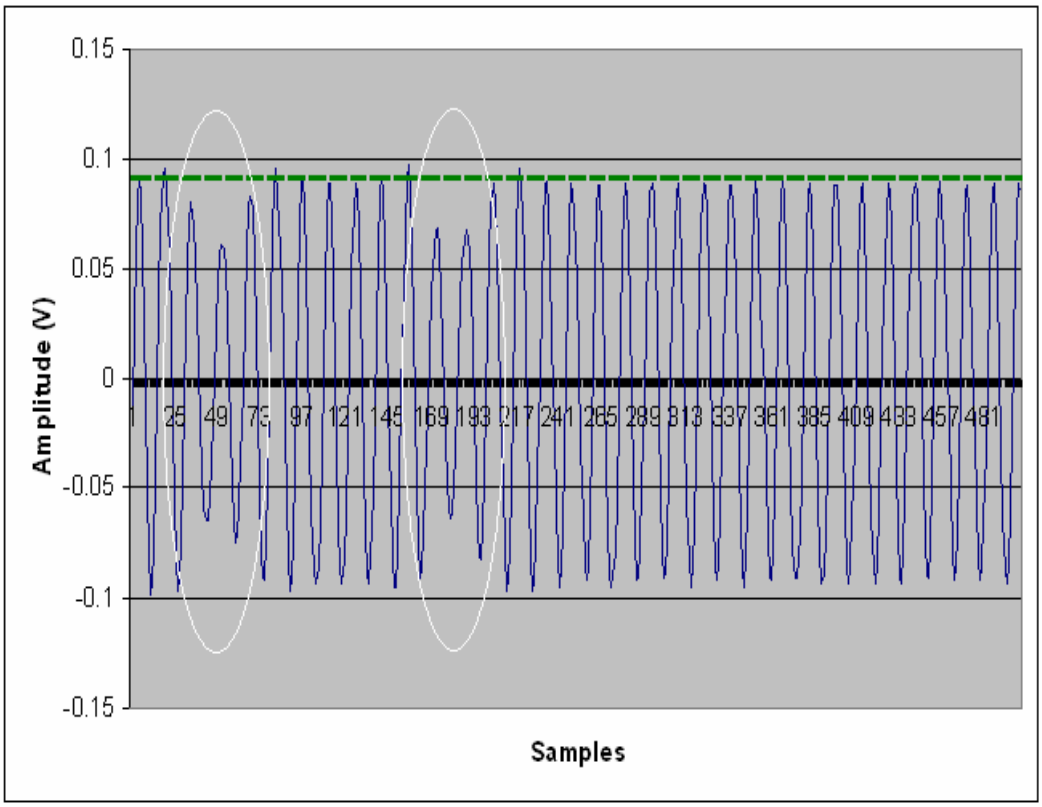


Figure 6.19 Output is filtered with 60MHz passband filter

The dashed lines seen in both Figure 6.18 and Figure 6.19 show the approximate rms values of the sinusoidal peaks of these two filter outputs in two consecutive figures. The amplitude deviations are quite high in the 15MHz filtered system compared to the 60MHz filtered system. In both figures a significant phase transition smoothening could be observed compared to the unfiltered case in Figure 6.17. Moreover also filtering results in reduction of glitches which are results of very high frequency components in the spectrum. These results are consistent with the simulations on the effects of analog filter's bandwidth on AM modulation.

The spectrum of the filtered periodic modulated signal is shown in Figure 6.20. With a passband of 60MHz six side lobes and the main lobe are passed through the filter and rest of the spectrum is suppressed at least 60dB.

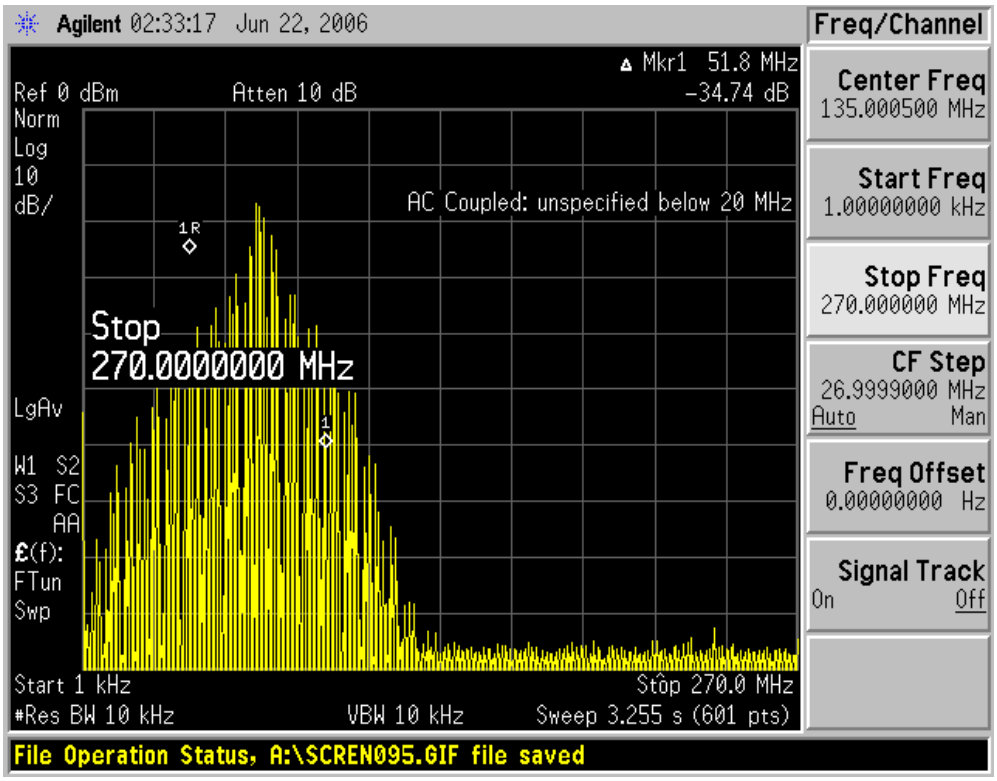


Figure 6.20 Spectrum of wideband filtered periodic QPSK modulated signal

Finally, all three components of the hardware setup (DDS, DAC and analog filter) are discussed in this chapter. With the integration of the filter to the system, the desired modulated signal is successfully produced with required analog performance.

6.6 SUMMARY OF FINDINGS

A single tone centered at 67.5MHz was produced first with a sampling frequency of 270MHz. Noise floor was observed at 101dBm with 3 kHz resolution bandwidth (135dBm/Hz). First harmonics and shifted images of the 67.5 MHz signal were observed at multiples of 135 MHz and 202.5 MHz respectively. Nyquist Band SFDR was measured to be 83dB and first harmonic, the biggest harmonic, was observed to be 68dB lower than the original signal.

A signal centered at 67.5MHz was QPSK modulated at a symbol rate of 7.5MHz with four periodic codes as a second study. Since the code was periodic, the spectrum was observed as discrete points placed at 1.88MHz apart from each other. In time domain these codes were shaped with rectangular envelopes. Thus, sinc envelope centered at 67.5MHz with nulls at multiples of 7.5MHz was observed in the spectrum. Since the spectrum were filled with sidelobes of the original and image signals, the sinc effect of sample and hold were clearly observed. The first null of 270MHz sample and hold function was placed at 270MHz in the spectrum. It was also observed that the original signal centered at 67.5MHz was placed almost in the constant region of this 270MHz sample and hold sinc function.

Another signal is formed by modulating again with periodic code consisting of seven codes. In this case, samples seen in the spectrum were placed 1.07MHz apart from each other. As a result of this sinc lobes shaped by code envelopes were observed better. In order to see complete sinc envelopes of codes, random code generator was implemented in FPGA and the 67.5MHz signal was QPSK modulated with these codes. Perfect sinc lobes were observed at the output. The similarity of spectrum envelopes of periodic and random modulated

signals with the theoretical expectations verified the proper operation of synthesizer.

In time domain, before the output was filtered, the glitches were observed that occurred after sample latches. The phase transitions were sharp. After filtering the output with a bandpass filter, it was observed that glitches were mostly cleared and the transitions were smoothened because of the band limitation and suppression of unwanted harmonics.

At this point it was required to analyze the amplitude modulation inside the envelopes of codes due to band limitation. Firstly the modulated signal was filtered with a bandpass filter with 15MHz passband centered at 67.5MHz. In time domain, there was a 1dB deviation compared to rms of sinusoidal peaks. Another filter with 60MHz passband was used to filter the output resulting in 0.38dB amplitude modulation inside the envelope of the code.

Finally spectra of the filtered, periodic and random modulated signals were observed. Since the analog filter could suppress more than 60dB at frequencies that are 60MHz apart from the carrier signal, all harmonics and images were cleared.

CHAPTER 7

CONCLUSION

In this thesis, implementation of a Digital Signal Synthesizer that can synthesize and modulate signals between 50-100MHz with a 60dB SFDR is accomplished. Different modulation techniques are adopted on this synthesizer. The designed DSS offers the controllability and programmability of the modulation type, symbol rate, and carrier frequency without any need of hardware changes during operation. Moreover the unwanted amplitude modulation on the output signal is decreased to minimal values.

In this implementation, a Spartan XC3S200 FPGA of XILINX is integrated with a high speed and high SFDR DAC of Analog Device, namely AD9777. FPGA is used to synthesize digital words of the desired signals and drive these digital words to DAC. For this purpose, on the top of the DDS technology, modulator, and control architectures are designed and utilized on the FPGA. The DAC is used to convert these digital words to analog signals such as voltage or current. Finally the output of the DAC is interpolated and smoothened using a wideband bandpass analog filter.

We examined the spectrum of the DSS output to show the proper operation of our system and derive some design rules. For DSS systems with very high SFDR requirements, a very careful frequency planning should be made considering both the sampling frequency and output center frequency. Moreover, the sinc envelope in the frequency spectrum caused by sample-and-hold nature of analog to

digital conversion should also be considered during frequency planning. Especially for wideband applications, the band should be placed in a frequency region where the band is not attenuated by the sinc effect severely. At this point it is also important to mention that the DAC chosen for the system is very important from the point of view of sampling frequency and SFDR performance. In addition, the DAC input bit number defines the dynamic range and the quantization noise level, which are also very important for the system's performance.

The phase noise of output is dominantly affected by the phase noise of system clock. The phase noise of the clock is directly added to the noise level of the output by a degradation amount of output to sampling frequency ratio. The DDS LUT width also has an effect on the phase noise of the system. The phase truncation caused by limited LUT width creates deterministic periodic spurs in the spectrum. However, the phase noise performance of system clock is more influential on the output phase noise performance than the phase truncation spurs.

For the transmitters in which, performance degradations caused by amplitude modulation are important, smoothing filter's passband should be increased. However, in order to be able to increase the passband and suppress the images and harmonics by reasonable amounts, the sampling frequency should be increased in order to place the image signals apart from the fundamental signal. This will give a margin for the filters in order to increase the suppression amount of the filter to required levels while keeping passband group delay performance of the filter good.

Finally in order to maintain the programmability, controllability and the flexibility in a transmitter, FPGA integrated with DAC architecture provides an ideal solution and in this thesis implementation of such a DSS system is achieved while keeping high SFDR, phase/frequency resolution and low AM. All findings verified that this implemented DSS system meets all design requirements supporting that this architecture is a viable solution for complex transmitter systems.

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