CHARGE BALANCED NEURAL STIMULATION INTERFACE CIRCUIT FOR FULLY IMPLANTABLE COCHLEAR IMPLANTS

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submitted by **HALIL ANDAÇ YIĞIT** in partial fulfillment of the requirements for the degree of **Master of Science in Electrical and Electronics Engineering Department, Middle East Technical University** by,

Prof. Dr. Halil Kalıpçılar
Dean, Graduate School of **Natural and Applied Sciences** _____

Prof. Dr. İlkay Ulusoy
Head of Department, **Electrical and Electronics Eng.** _____

Prof. Dr. Haluk Külah
Supervisor, **Electrical and Electronics Eng., METU** _____

Examining Committee Members:

Prof. Dr. Tayfun Akın
Electrical and Electronic Eng., METU _____

Prof. Dr. Haluk Külah
Electrical and Electronics Eng., METU _____

Prof. Dr. Nevzat Güneri Gençer
Electrical and Electronic Eng., METU _____

Assoc. Prof. Dr. Serdar Kocaman
Electrical and Electronic Eng., METU _____

Assist. Prof. Dr. Dinçer Gökçen
Electrical and Electronic Eng., Hacettepe University _____

Date: 18.06.2020

I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

Name, Surname: Halil Andaç Yiğit

Signature:

ABSTRACT

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Yiğit, Halil Andaç
Master of Science, Electrical and Electronics Engineering
Supervisor: Prof. Dr. Haluk Külah

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Cochlear implants (CI) are the most successful prosthesis, which helps people suffering from profound deafness; however, aesthetic concerns and daily battery replacement are the main problems. These problems can be solved by a low power fully implantable cochlear implant (FICI). The FICI system should operate with ultra-low power consumption while covering high input dynamic range. Moreover. the system should ensure safe stimulation with single battery usage. In this thesis, a low power FICI interface circuit is designed while focusing on the charge balanced stimulation and single supply implantation. The interface circuit takes input from multi-channel piezoelectric transducers and stimulates the electrodes with pulse width modulated output currents. By pulse width modulation, a time gap is formed between two consecutive channels, and this gap is used for charge balancing operation. The system is tested with an in-vitro test setup and it safely stimulates the single channel cochlear electrode with 50 dB input dynamic range while consuming lower than 800 µW power from a single 1.8 V supply.

Keywords: Charge balance, cochlear implants, low power electronics, neural stimulation

ÖZ

TAMAMEN İMPLANTE EDİLEBİLEN İMPLANTLAR İÇİN ŞARJ DENGELİ SİNİR UYARIMI ARAYÜZ DEVRESİ

Yiğit, Halil Andaç
Yüksek Lisans, Elektrik ve Elektronik Mühendisliği
Tez Danışmanı: Prof. Dr. Haluk Külah

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Koklear implantlar işitme kaybı yaşayan hastaların sorunlarını gideren protezlerdir. Harcadıkları gücün yüksek olması ve hastaların yaşadığı estetik endişeler bu cihazlarda karşılaşılan ana sorunlardır. Bu problemler tamamen implante koklear implanlar (FICI) ile çözülebilir. FICI sistemi yüksek giriş dinamik aralığını kapsayıp çok düşük güç tüketimi ile çalışmalıdır. Tüm bunlara ek olarak system tek pil ile güvenilir bir şekilde çalışmalıdır. Bu tez çalışmasında, tek bir pil kullanarak şarj dengeli uyarım sağlayan düşük güç tüketimine sahip bir FICI arayüz devresi tasarlanmıştır. Arayüz devresi çok kanallı piezoelektrik transdüserlerden girdi alır ve elektrotları darbe genişliği modülasyonlu çıkış akımlarıyla uyarır. Darbe genişliği modülasyonu ile iki ardışık kanal arasında bir zaman aralığı oluşturulur ve bu boşluk yük dengeleme işlemi için kullanılır. Bu system bir in-vitro test kurulumu ile test edilmiştir ve tek kanallı koklear elektrodu 50 dB giriş dinamik aralığı ile 800 μW'dan daha az güç harcayarak 1.8 V'luk güç kaynağından güvenli bir şekilde uyarılmıştır.

Anahtar Kelimeler: Düşük güç elektroniği, Koklear Implant, nöron uyarımı, yük dengesi

To My Family

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ABBREVIATIONS

ADC: Analog to Digital Convertor

AM: Amplitude Modulation

CCS: Constant Current Stimulator

CI: Cochlear Implant

CIS: |Continuous Interleaved Sampling

DAC: Digital to Analog Converter

FES: Functional Electrical Stimulation

FICI: Fully Implantable Cochlear Implant

PWM: Pulse-Width Modulation

CHAPTER 1

INTRODUCTION

1.1. Motivation

Nearly half a billion people around the world, which is more than 5% of the world population, suffer from disabling hearing loss [1]. If the hearing loss is greater than 90 dB sound pressure level (SPL), the only treatment is cochlear implant.

In normal hearing, sound waves traveling through air and collected by the outer ear and reach the tympanic membrane via the ear canal. The soundwaves at the membrane cause vibrations on the middle ear where three small three bones are placed. The third and the last bone is attached to another membrane which is called oval window. The oval window is placed on the cochlea and its movements cause pressure oscillations in the cochlear fluid. Cochlear fluid oscillations initiate a movement on the basilar membrane (BM). Sensory hair cells in the cochlea, which are placed on the BM, senses the movement of the BM. These hair cells are part of the organ of Corti. When the BM moves, the hair cells are releasing the chemical transmitter for the nerve stimulation.

The hair cells are fragile and can be affected from genetic defects, loud sounds, some drugs, and aging. Deafness occurs when the hair cells are damaged or completely absent (Figure 1.1) [2]. Without the normal stimulation of hair cells, spiral ganglion and terminals of the organ of Corti eventually lose its function and total deafness cannot be recovered without using any implants [3]. To regain hearing ability, cochlear implants are developed in different approaches. However, today's cochlear implants have some problems. In this thesis, a new generation cochlear implant interface electronics is designed and implanted to eliminate these problems.

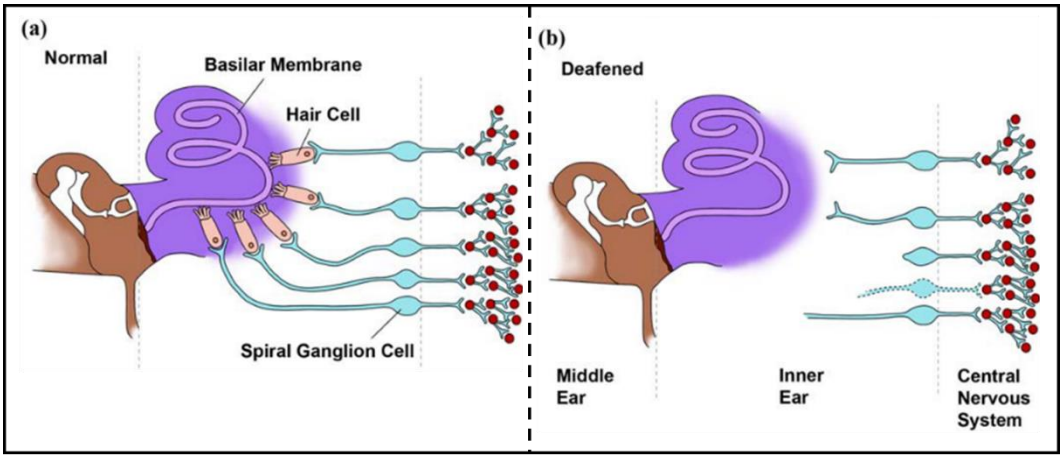


Figure 1.1. Anatomic model of normal ear (a) and totally deafened ear (b) [2]

1.2. Conventional Cochlear Implants

The cochlear implants (CI) are one of the most successful neural prosthesis and helps more than 120000 deaf people in the world [4]. The first idea of the electrical stimulation is tested by A. Volta in the early 1800. He placed a metal rod in his ear canal and heard a crackling sound when he applied 50 V to the metal [5]. After then, the evolution of the CIs takes nearly two decades, and today multi-channel implants are manufactured and started to use at mid of the 1980s [6]–[8].

The modern CI system can be seen from Figure 1.2 and block diagram of the system given in Figure 1.3. The system consists of two main parts which are inner and outer. The outer part includes microphone, battery, speech processor, external transmitter and decoder. Integrated circuit, receiver and intracochlear electrodes are placed in the inner part.

The microphone collects the input sound and converts it to the electrical signal. After the input signal is digitalized, digitalized signal is mapped and modulated at the digital signal processing (DSP) unit. Mapping operation is required for covering the high input range [9]. The modulation is required for the communication between internal and external parts. The digital input signal is carried via an RF link with a high

frequency carrier signal to the inner part. The input signal should be amplified for the transfer due to high power loss on the communication. The power amplifier is used for amplification, then amplified signal is sent to the inner ear via the transmitter. Battery in the external part requires daily replacement due to high power consumption in the transmission.

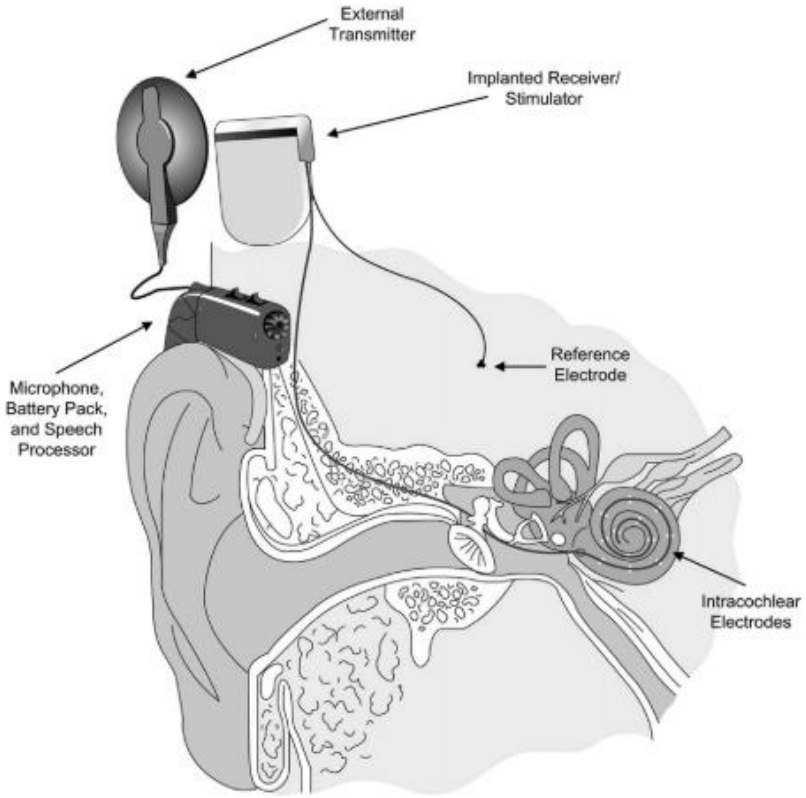


Figure 1.2. Modern cochlear implant system [7]

The internal receiver takes the modulated signal and transmitted power via the RF link. The transferred power is used to power-up integrated electronic blocks. The modulated signal is first demodulated and channel (frequency & amplitude) information is acquired. The stimulator circuits generate the biphasic current pulses according to the signal data and stimulate the neurons with the intracochlear electrodes. The stimulation information and inner part system information can be sent to the external side by back telemetry. Back telemetry uses the same RF link and transfers data from the inner part to the outer part. This data can be used for patient

fitting or learning the condition of the internal part. The patient fitting can be done externally for adjusting the comfort level of the patients [10]–[12].

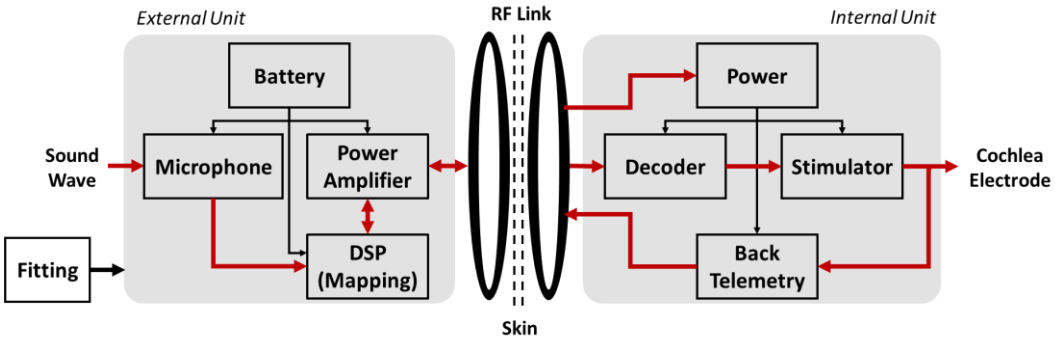


Figure 1.3. Block diagram of the modern cochlear implant system [10]

The sound data is processed and encoded before the transmission. The speech processing operation techniques are important features of CIs due to it affects speech recognition of patients [13]. Sound processing strategies are developed with the time and some of the successful ones are continuous-interleaved-sampling (CIS) [11], spectral maxima sound processor (SMPS) [14], an advanced combinational encoder (ACE) [12] and high resolution (Hires) [15]. These strategies are still used at conventical CIs.

Among different sound processing strategies, CIS is the most commonly used one. The block diagram of the CIS strategy can be seen in Figure 1.4. In the CIS, the input is given through bandpass filters, and envelope detection or Hilbert transform operation is performed for each filtered output. The envelope of each output goes into the compression stage where the operation made by logarithmic mapping. Then mapped outputs are multiplied by the biphasic pulse train in which the stimulation rate is predefined. Every channel pulse train is the shifted version of each other, and a channel does not overlap with other channels. In this way, the interaction between channels is prevented in the stimulation. Since every channel is stimulated one by one, the power consumption of the system is equal to a single-channel implant [13], [16], [17].

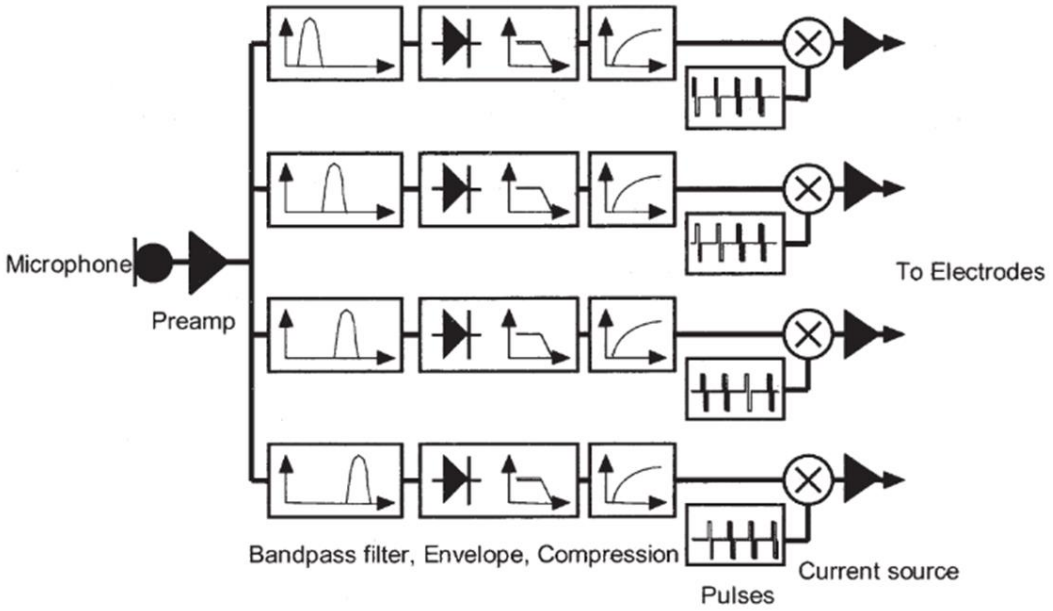


Figure 1.4. Block diagram of the CIS strategy [13]

In years, the improvements are made for the speech recognition and perception for patients. These improvements are made at the sound-processing, stimulation rate, intracochlear electrode and channel numbers. However, the main problem of CIs is the outer part because the outer part cannot be used in rainy days, water sports and shower. Also, they create aesthetic concerns for younger users. Besides, due to high power consumption and energy inefficiency battery should be replaced daily. These problems can be solved by fully implantable cochlear implants by combining internal and external parts of the CIs in a single chip. For this implantation, a microphone should be replaced with another sound transducer and an ultra-low power system should be designed with an external battery.

1.3. Fully Implantable Cochlear Implants

The fully implantable cochlear implants (FICI) should be placed into the ear and operate for a long time without replacement. The first problem of the FICI systems is the sound transducer. Since the CIs use a microphone, it cannot be placed into the ear. FICI system requires an implantable sound transducer and an ultra-low power interface circuit for operation. There are implantable sound transducers for implantable devices using a piezoelectric sensor [18], [19]. These designs use single

channel output; hence they require additional electrical filters for sound processing which results in higher power consumption. Another idea is presented in [20], [21] for implantable sound transducers. In these designs, the sensor array is placed on the eardrum, and the array senses and filters the sound mechanically. By using sensor array as an input transducer, the power consumption can be decreased further for the FICI system. However, the sensor requires a custom interface circuit for low-power operation.

In [22], an ultra-low power cochlear implant processor is proposed as a FICI system. In the system, (Figure 1.5) the inputs come from the electret microphone and this microphone covers 77 dB SPL dynamic range. The microphone output is compressed to 57-dB dynamic range with automatic gain control (AGC) unit after the pre-amplification. At the output of the AGC, the signal goes into 16 different bandpass filters. The filtered signals pass through the envelop detector and then translated to the digital domain by analog to digital converter (ADC). Since the ADC is logarithmic, it also compresses the analog envelop with digital mapping. Digital signals are stored and used at the scanners according to the CIS strategy. The proposed system consumes 211 µW. However, the system is not complete because the stimulator part is missing which consumes most of the power of the FICI.

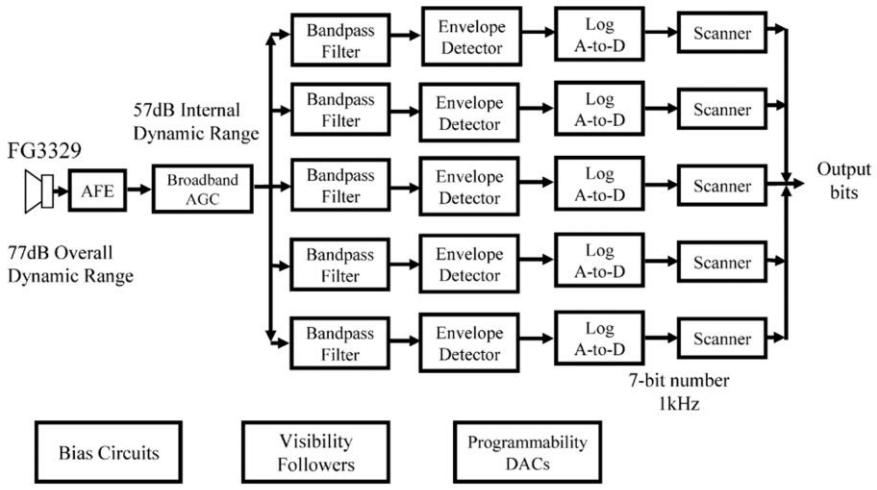


Figure 1.5. Block diagram of the [17]

Another study for a FICI system is described in [23]. The block diagram and signal flow can be seen in Figure 1.6. The signal from the microphone is converted into current. Then filtered by bandpass filters with a clipping detector. There is a feedback loop between the filter and voltage to current converter. This feedback is achieved with an AGC. The filtered signal goes to the limiter, full wave rectifier and low pass filter for envelop detection respectively. After the envelope detection, the signal is compressed and amplified for stimulation. By the compress operation, 60 dB input dynamic range is fitted to the less than 20 dB electrical range. This operation is performed for 16 distinct channels and the processor of the system uses 126 µW. The author also has an estimate, the power consumption of the stimulator part is around 2.0 mW. This power consumption is quite high for an implantable system due to the limited battery volume.

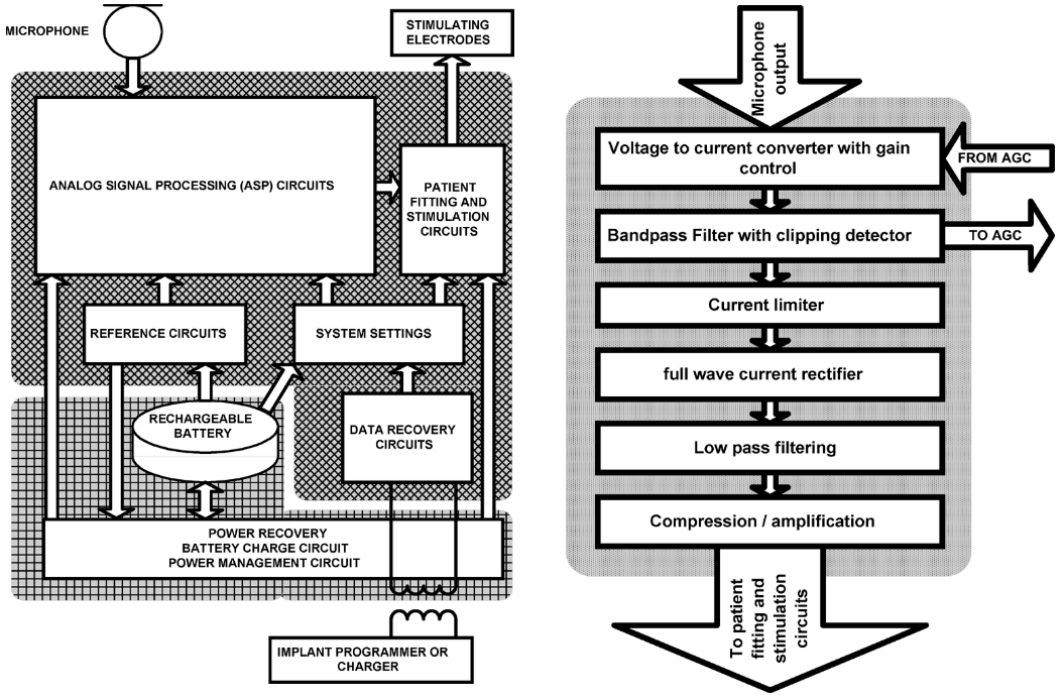


Figure 1.6. Block diagram and signal flow of the [23]

There is another study about FICI which uses a single piezoelectric sensor for input instead of a microphone [24]. The block diagram of the FICI is given in Figure 1.7. The single piezoelectric sensor input is taken by a charge amplifier and amplified by the programmable gain amplifier. Then the analog signal goes to a driver for successive approximation register (SAR) ADC. The digitalized input is filtered, passed through an envelope detection and compressed. The biphasic currents are generated with an arbitrary waveform generator. The arbitrary waveforms are generated for efficient stimulation with genetic algorithms according to the CIS strategy. The generated biphasic currents are scaled with patients fitting bits and stimulate the electrodes. The total power consumption of the system is 572 µW. However, the system uses six different voltage supplies which cannot be inserted to human body without voltage regulators and converters. The extra circuitry increases the power consumption dramatically.

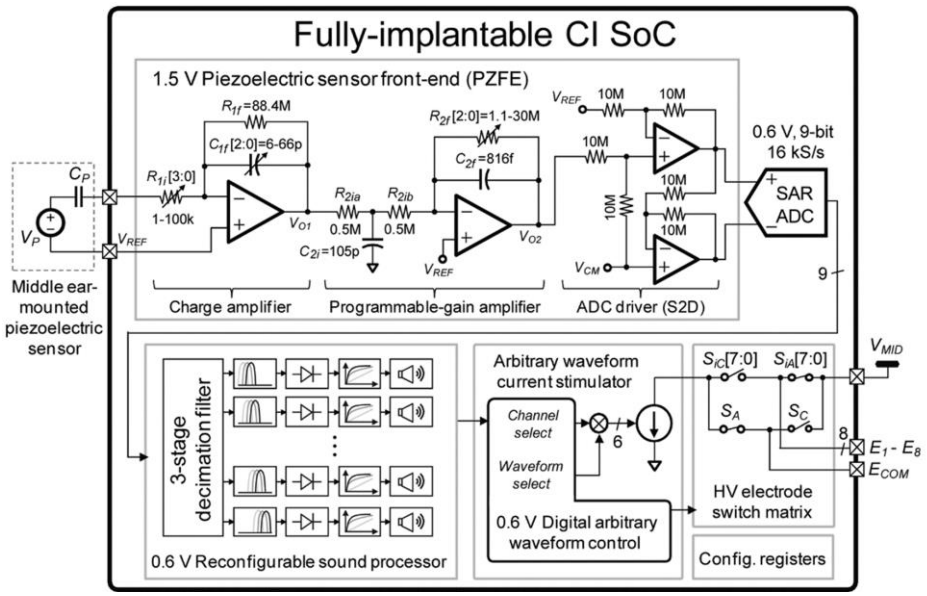


Figure 1.7. Block diagram of the [24]

Another study using 8 channel piezoelectric sensors for a FICI system is proposed in [25]. The system block diagram is given in Figure 1.8. The system takes input from 8 different bandpass characteristic piezo electric sensors. The outputs of the sensors are compressed and amplified with logarithmic amplifier. The amplified signal is also

converted to the current at the amplifier. Then the current output is rectified and filtered for envelope detection operation. The envelope of the signal is sampled and held for the stimulation operation according to the CIS strategy. The stimulation current is generated by the sampled signal and adjusted by patient fitting bits. The output current anodic and cathodic phases are adjusted at the switch matrix for the stimulation. The complete system consumes less than 500 µW.

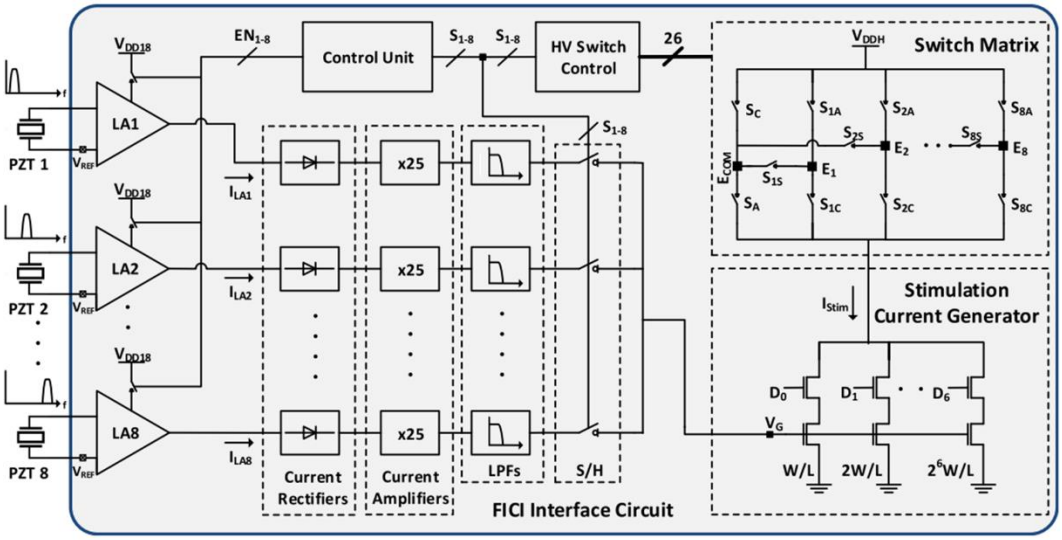


Figure 1.8. Block diagram of the [25]

The systems are in [22] and [23] are just focusing front-end sound processing electronics and their stimulator parts are missing. Even if the FICI systems in [24], [25] look like completed systems, they use inefficient passive charge balancing techniques and require more than one voltage supply for neural stimulation. However, single battery usage and dynamic charge balancing are required for fully implantation. In the balanced stimulation, anodic and cathodic cycles become equal. However, due to the imperfections of the electronic circuits, the current differs between these cycles. This difference may harm tissues after some time and system cannot operate. [24], [25] systems use passive techniques that are not suitable for fully implantable systems because passive charge balancing requires large areas and generates uncontrollable

high currents. Hence, a low-power active charge balance technique is required for a complete FICI system.

1.4. Balanced Neural Stimulation

Functional electrical stimulation (FES) is a technique in biomedical engineering that enables stimulation of the nerves with electrical signals. Cochlear implants also use this technique for stimulating neurons [6]. As a stimulator, cochlear implants use biphasic current pulses. The biphasic current transfer charges and discharges the neuron by changing the stimulation current direction. However, matching the charging and discharging currents is impossible due to the imperfections and mismatches in the integrated circuits. The mismatch at the charging and discharging cycles results in charge accumulation which causes tissue lesions and electrode corrosion. Because of this reasons, the charge balance circuit is a vital part of the FICI systems.[26].

The stimulation type is a parameter for charge balance circuits [27]. The most used stimulation types are voltage-controlled stimulation (VCS) [28], constant charge or switched-capacitor stimulation (SCS) [29] and constant current stimulation (CCS) [30], [31]. VCS is the most efficient stimulator type; however, the control of the charge is not possible by this technique because the charge is highly dependent to the electrode-tissue impedance. In SCS technique, the charge is highly controllable, but the integrated capacitors occupy a very large area of the chip. Due to area problem, it is not suitable for the multi-channel implantable systems. CCS techniques offer high charge controllability and moderate efficiency with small area occupancy and it is the most used technique for implantable devices [30], [31].

Figure 1.9 presents the schematic of the constant current stimulator and generated biphasic current. The stimulation starts with enabling cathodic switch (SW_C) and current flows from the common electrode and the current controlled by $I_{DISCHARGE}$

current source. In the anodic phase, SW_C is disabled and SW_A is enabled and current flows to the common electrode. Due to the imperfections of the circuits, charge accumulates after the stimulation at the capacitive load. Charge balance circuits are required to limit charge accumulation within the safety region [32]. The safe limit for the unbalanced charge is 15 nC/phase or 100 nA DC current error between the sink and source cycle [33].

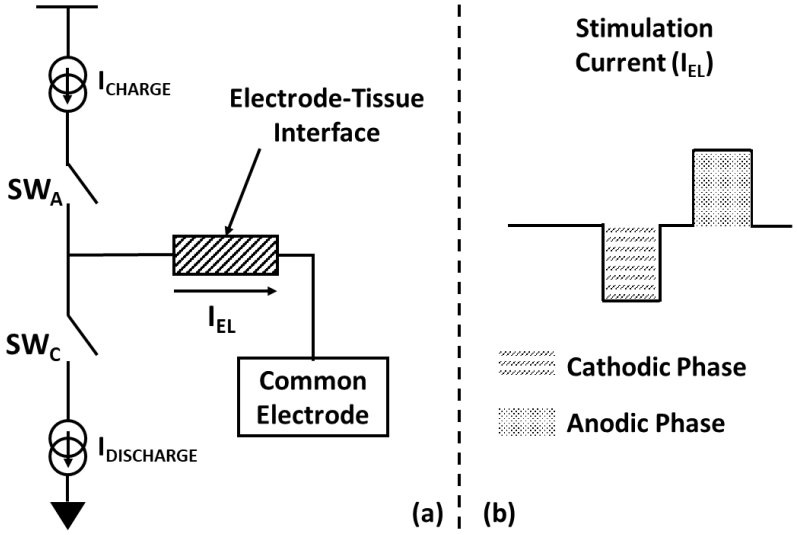


Figure 1.9. Simple CSS structure (a) and generated biphasic pulse waveform (b)

Charge balance circuits can be passive or active. The blocking capacitor [34], [35] and the electrode shorting [25], [36] are the most used methods for passive charge balancing. In the blocking capacitor technique, a large capacitor is placed at the output of the stimulator and this capacitor prevents the DC current error. However, required capacitor values is too high for an implantable IC. Due to area requirement, this method is not suitable for the multichannel implantable devices. In the electrode shorting method, the electrode is shorted after the stimulation for dissipating remaining charge. The shorting current ratings cannot be controlled, and the high current ratings may harm tissues. Electrode shorting is also not suitable with multi-electrode structure due to interface between another channel when the shorting operation occurs. This problem can be solved with active charge

balance techniques. Mostly used active charge balancing techniques are dynamic current matching [37], [38] and charge monitoring techniques. In the dynamic current balance method, the matching is performed for the anodic and cathodic phase currents for charge balanced operation. In the charge monitoring technique, the charge is monitored, and compensation is applied. The compensation can be via offset current [26] and pulse injection [39], [40]. None of these works are focused on ultra-low power application which is required for the FICI system. The charge balance circuit should be suitable with the multi-channel CIS strategy band it should consume minimum power and occupy minimum area.

1.5. Objectives of the Thesis

The main objective of this thesis is implementing a new single battery FICI interface circuit with active charge balancing. This work is also a part of FLAMENCO (A Fully Implantable MEMS-Based Autonomous Cochlear Implant) Project (www.flamenco.metu.edu.tr). The scope of the project is implementing a fully implantable and autonomous cochlear prosthesis which takes sound input from 8 channel piezo-electric sensor, stimulates the auditory neurons with biphasic currents, and is powered up with a rechargeable battery. The FICI interface circuit design criteria can be listed as follows:

1. The power consumption of the system determines the lifetime and charging requirement of the implantable device. The implanted system should consume less than 800 µW power to operate more than 15 days (16 working hours) with 200 mWh implantable battery without any recharge [25].
2. The FICI interface circuit must fit into a complete cochlear prosthesis system. Due to its implantation area, the circuit volume is restricted, and the interface circuit should be designed with on-chip components with an area less than 5 mm^2 [41].
3. Another vital criterion for the FICI interface electronics is the safe operation at the stimulation part. For safe stimulation a reliable charge balance circuit is

required. The charge balance circuit should be implanted together with the system and consumes low power (< 50 µW).

4. The FICI system should have high dynamical input sound range for speech recognition and perception. The circuit should provide low input noise characteristics and operate with at least 50 dB dynamic range for good hearing.
5. The stimulation current should be adjustable for the maximum (up to 2 mA while using metal electrode(area is 0.01 cm^2) [42]) and minimum comfort levels for each patient. Therefore, the designed FICI system has an adjustable current level for patient fitting.

1.6. Organization of the Thesis

The remaining part of the thesis is as follows:

Chapter 2 presents the implementation of the ultra-low power pulse-width modulated FICI system. The implanted FICI system is used for validation of the PWM technique for the next implantation. In this method, output biphasic current amplitude is fixed and its time changes with the input sound level. The circuit blocks are given with schematic and simulations results. The experimental test results include the single channel sensor performance of the system with electrical load.

Chapter 3 includes the improved version of the proposed FICI system with an active charge balance circuit and a DC-DC converter. The aim of the design is charge balanced PWM FICI circuit interface for safe operation and adding DC-DC converter for single supply implantation. The implanted FICI system generates PWM stimulation currents and the time gap between two consecutive channels are used for charge balancing. The charge balance circuit monitors the electrode voltages and applies short current pulses. In addition, the whole system can operate with single 1.8 battery. The improvements of the FICI are presented with schematics and simulation results. The experimental tests are performed with 8-channel sensor array and the circuit stimulates the electrical and artificial (in-vitro) loads.

Chapter 4 presents synchronous charge balance method. The charge balance circuit is designed for amplitude modulated FICIs ([25]). However, it can be used with multi-channel PWM FICI circuit. In this method, the charge balance circuit monitors the electrode voltages and applies the synchronous balancing current without disturbing the stimulation. The proposed charge balance technique is suitable with constant current stimulators and multichannel CIS strategy. Circuit schematics, simulations and experimental tests are given for the implemented circuit.

Chapter 5 concludes the thesis with brief summary of the designs and possible future improvements of the FICI system.

CHAPTER 2

PULSE WIDTH MODULATED FICI INTERFACE CIRCUIT

2.1. Motivation

The vital part of the safe neural stimulation is charge balancing operation [26]. According to the previously reported studies, balancing operation is generally performed in passive methods. For a FICI system, the limited volume of the implanted area requires an active charge balancing because passive techniques occupy large area. In multi-channel FICI systems the charge balance current cannot be generated during stimulation to prevent the interaction between electrodes. Time gap can be generated after stimulation by pulse width modulated (PWM) biphasic current instead of using amplitude modulated currents.

In this chapter, only low power PWM FICI interface circuit is designed for the validation of the system. The system is designed for 8 channels and tested with single channel. The aim of the design is generating PWM modulated signals with piezo electric transducers and analyzing the circuit blocks.

The design of the circuit is made on the EDA software CADENCE. The schematic, and layout simulations are made with SPECTRE (simulation tool). For DC, AC and transient analyses, the noise factor is not taken, and temperature value is set to 37 degrees. Noise analyses are performed for critical blocks.

2.2. Circuit Design and Description

The FICI circuit generates biphasic current at the output for stimulating neurons. The stimulation charge is controlled by the pulse width of the current. The pulse width of the biphasic current is adjusted according to the piezo-electric sensor voltage output. The block diagram of the circuit is given in Figure 2.1. The circuit consists of 7 main

blocks which are amplifier, rectifier, sample & hold circuit, logarithmic voltage to current converter, current comparator, stimulator circuit and control block. First of all, the piezo electric output is amplified, then rectified for the peak detection. Then, the peak is sampled and held for 125 μs, and the voltage value is converted to the current by compressing. The compressed current value is compared with reference current, which is controlled by control block for pulse time determination. After all, the stimulator circuit generates the biphasic current output. The circuit has three different supplies for the operation. The digital blocks (Control Block) controlled by 1.5 Volts, the stimulator block uses 5 Volts and the rest of the circuit (Analog Blocks) uses 3.3 Volts for low power consumption. Operation uses Continuous Interleaved Sampling (CIS) stimulation strategy. In this strategy, the electrodes are stimulated one by one for 125 μs in 1 ms period and amplifiers are enabled with the same timing without concerning input.

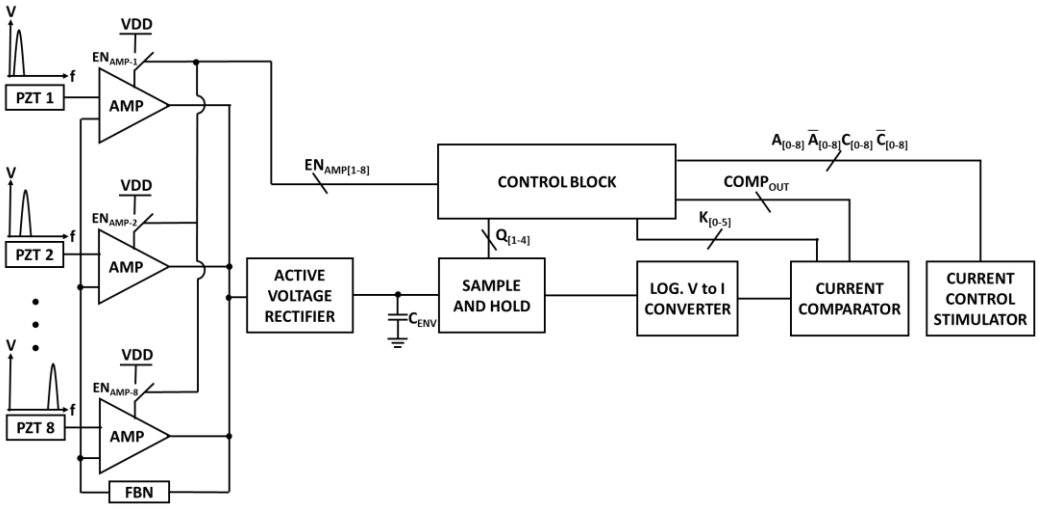
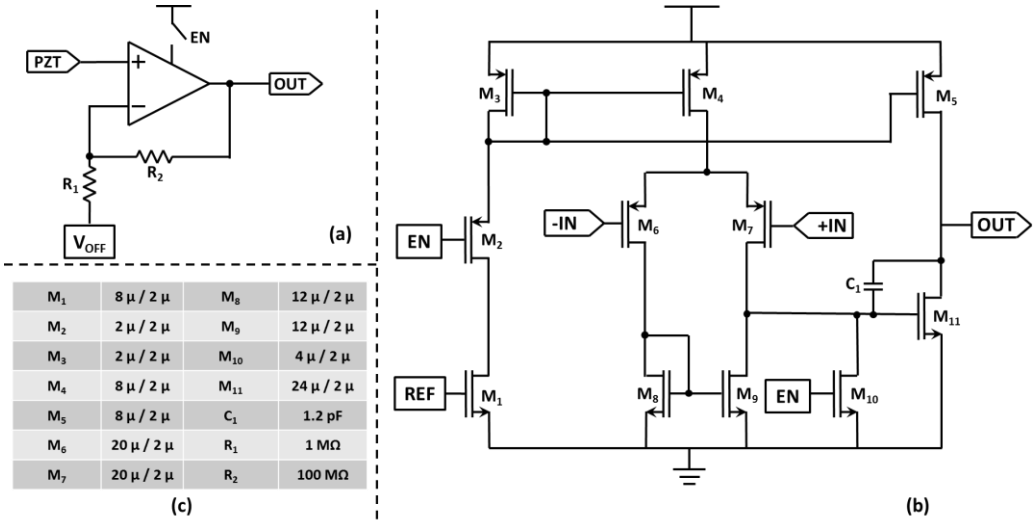


Figure 2.1. Block diagram of the pulse-width modulated FICI interface circuit

2.2.1. Input Amplifiers

The first stage of the interface circuit is an amplifier because output voltages of the piezo electric sensors are around hundreds of μVs which is low for processing. The non-inverting operational amplifier is used for the input stage with a fixed gain. Since the voltage supply level is 3.3 V and maximum voltage output of the transducer is

20 mV, gain is fixed to 100. Figure 2.2 shows the input amplifier topology. The input amplifiers consist of two stages. The first stage is PMOS differential pair and the second stage is NMOS common source amplifier. The M_2 and M_{10} transistors are added for the enable operation. The amplifier is enabled for 125 μs in every 1 ms, so the amplifier should give response in 125 μs. Also, the PMOS input pair is chosen for better noise characteristic. The on-chip C_1 capacitor is added to the system for the compensation and stability.



M_1	8 μ / 2 μ	M_8	12 μ / 2 μ
M_2	2 μ / 2 μ	M_9	12 μ / 2 μ
M_3	2 μ / 2 μ	M_{10}	4 μ / 2 μ
M_4	8 μ / 2 μ	M_{11}	24 μ / 2 μ
M_5	8 μ / 2 μ	C_1	1.2 pF
M_6	20 μ / 2 μ	R_1	1 MΩ
M_7	20 μ / 2 μ	R_2	100 MΩ

(c)

Figure 2.2. Input amplifier (a), schematic (b) and component parameters (c)

The AC analysis is made for close loop amplifier circuit with the corners (Figure 2.3.). Corner analyses are made for observing process variations effect. These variations directly affect the threshold voltages (V_T) and speed of the circuit. There are 5 corners in the technology which are tabulated in the Table 2.1.

Table 2.1. *Process corners*

Abbreviation	*Corner*	*Nmos V_T*	*Pmos V_T*
NOM	Nominal	Nominal	Nominal
WP	Worst Power	Low	Low
WO	Worst One	Low	High
WS	Worst Speed	High	High
WZ	Worst Zero	High	Low

The amplifier gives the constant 40 dB gain up to 10 kHz bandwidth. Since the daily speech frequency is between 300 Hz to 3400 Hz, 10 kHz bandwidth is enough for this system. The lowest phase margin is 40˚ so the amplifier is stable in every corner. In addition, amplifier has 6 μV simulated input referred noise in frequency range between 10 Hz to 10 kHz, which is low enough to provide high SNR for middle ear piezo-electric sensor [20].

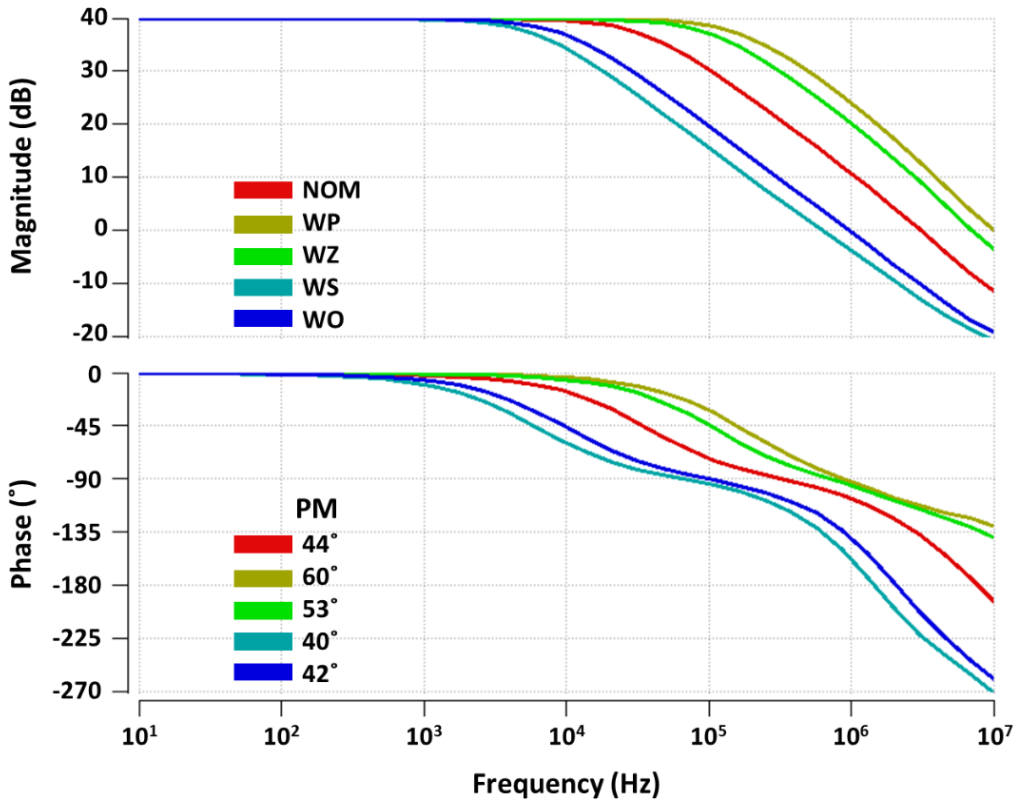


Figure 2.3. AC analysis of the input amplifiers (Corners can be seen from Table 2.1.)

2.2.2. Voltage Rectifier

For the peak detection, full wave rectification is required. Instead of passive rectifier, an active rectifier is used to minimize the voltage loss. The designed voltage rectifier (Figure 2.4) consist of 5 operational amplifiers; 3 of them is connected as buffer, 1 of them is analog inverter and the last one is connected as a comparator. The operation principle of the rectifier is as follows: the input and its inverse (respect to V_{DC}) are

compared and the higher one generates the output. For negative of the input, resistive negative unity feedback is used.

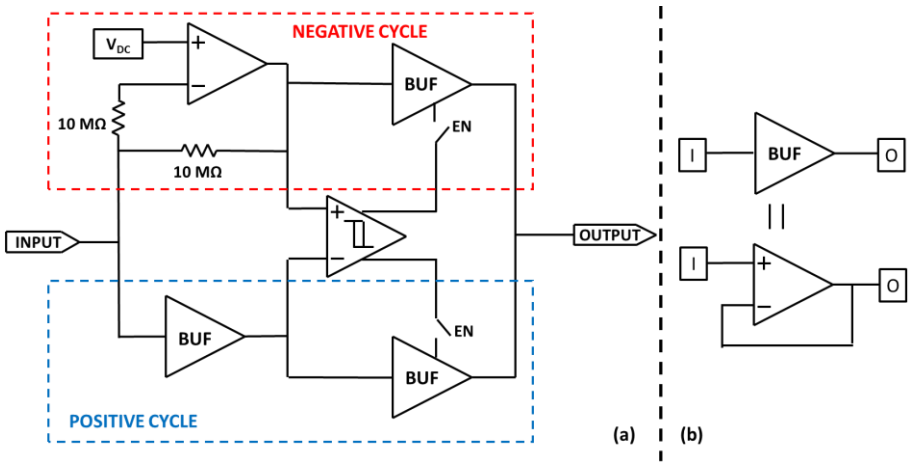


Figure 2.4. Voltage rectifier schematic (a) and buffer connection (b)

Figure 2.5 shows the transient analysis of the voltage rectifier circuit. The output is the full wave rectified version of the input with small delay. The delay is smaller than 10 µs, which is tolerable for our system.

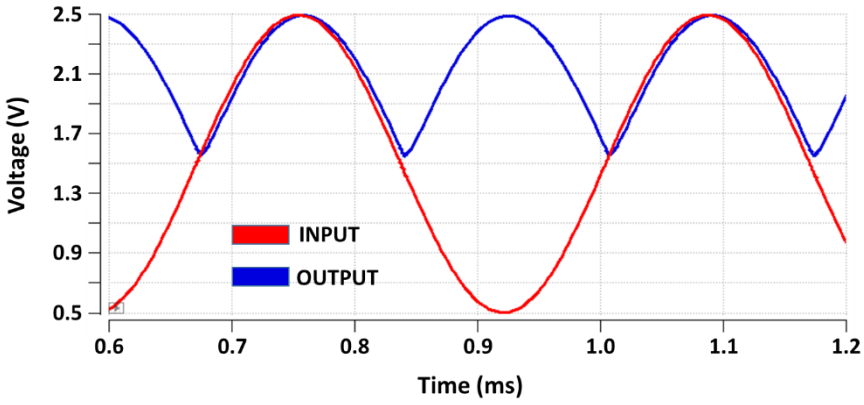
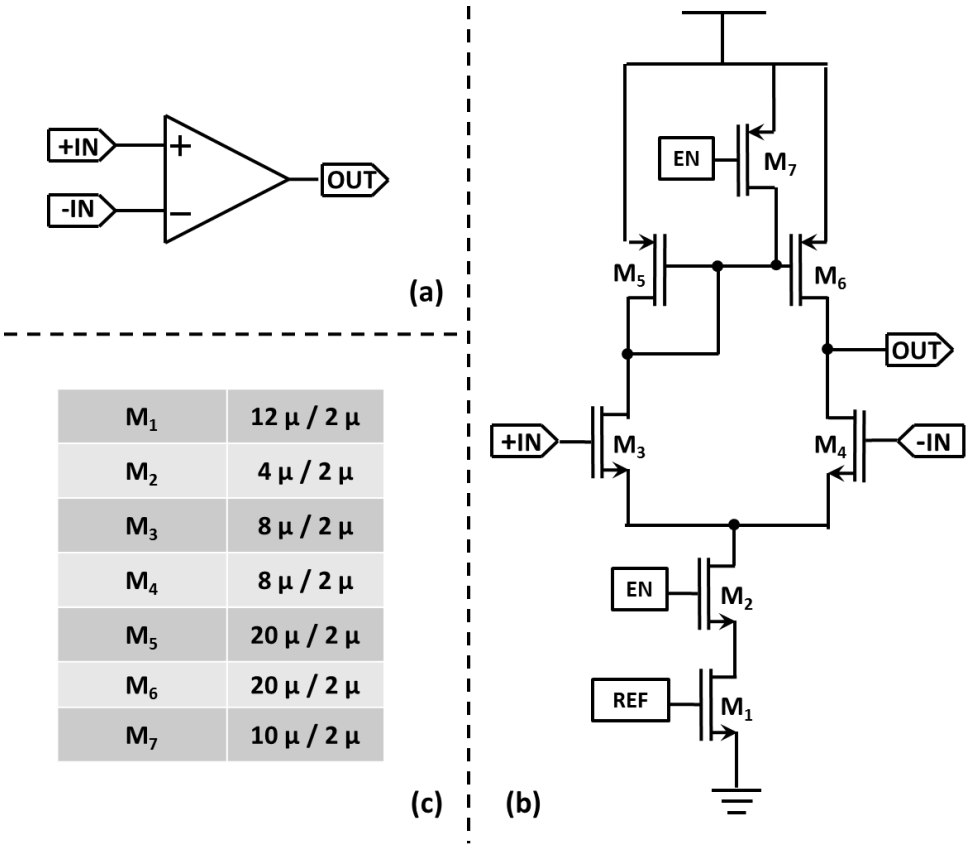


Figure 2.5. Voltage rectifier transient analysis results

Figure 2.6 shows the amplifier topology of the voltage rectifier. The amplifiers are designed as single stage differential amplifiers. Due to its gain, bandwidth, stable characteristic and low power consumption a single stage amplifier is chosen. The M_2

and M_7 transistors are added for enabling operation. When the enable is high, the amplifiers operate and generate output. When the enable is low, the output of the amplifier becomes HIGH Z which means the output resistance becomes very high and does not affect the output value.



M_1	12 µ / 2 µ
M_2	4 µ / 2 µ
M_3	8 µ / 2 µ
M_4	8 µ / 2 µ
M_5	20 µ / 2 µ
M_6	20 µ / 2 µ
M_7	10 µ / 2 µ

Figure 2.6. Amplifiers symbol (a), schematic (b), transistor sizes (c)

The corner open loop AC analysis is made for the amplifiers to observe bandwidth and gain characteristics (Figure 2.7). The operational amplifiers have 50 dB gain which implies 1/300 error rate on the buffering operation. The bandwidth is higher than 8 kHz for the corners and covers the daily speech range.

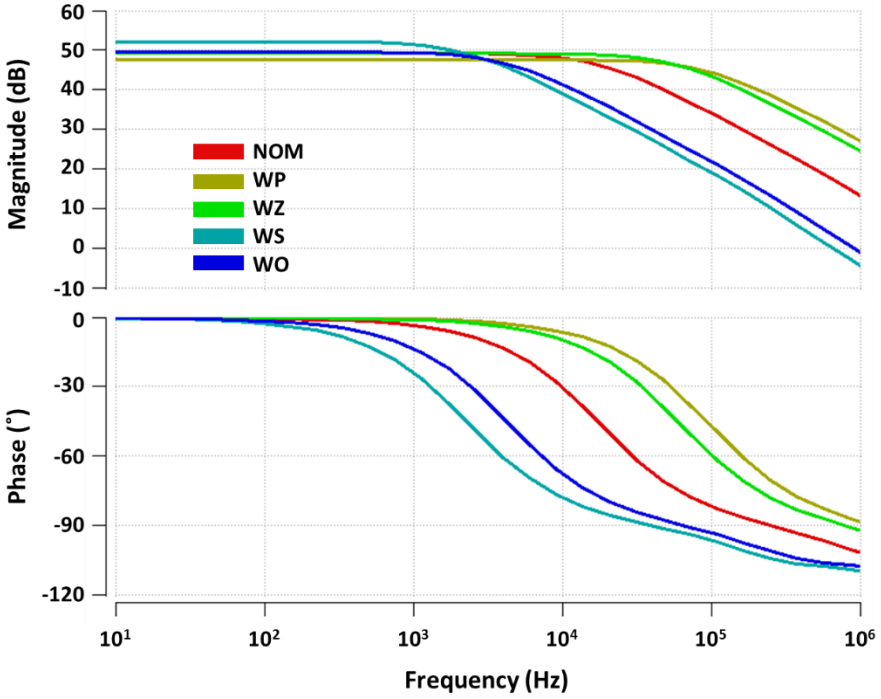


Figure 2.7. Voltage rectifier amplifiers AC analysis (Corners can be seen from Table 2.1.)

The comparator schematic is given in Figure 2.8. The differential PMOS pair with biased active load is used to have dual output with equal delay times The outputs become rail to rail with inverters at the output of the differential pair.

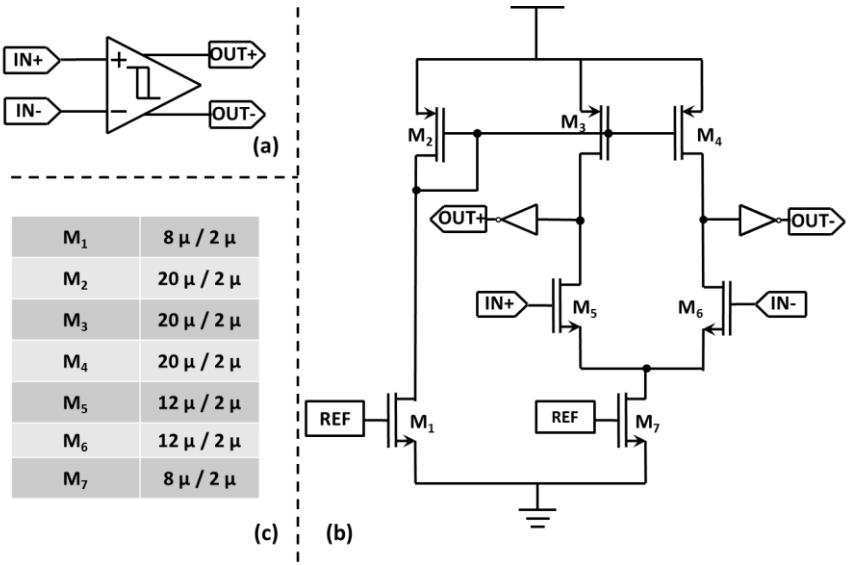


Figure 2.8. Comparator symbol (a), schematic (b), transistor sizes (c)

Figure 2.9 shows the AC analysis of the comparator. The gain of the comparator is greater than 42 dB for all corners. DC analysis of the comparator (Figure 2.10) shows the minimum voltage difference for the comparison, which is 4 mV. Since the comparator input is amplified, the input referred comparison difference is 40 µV.

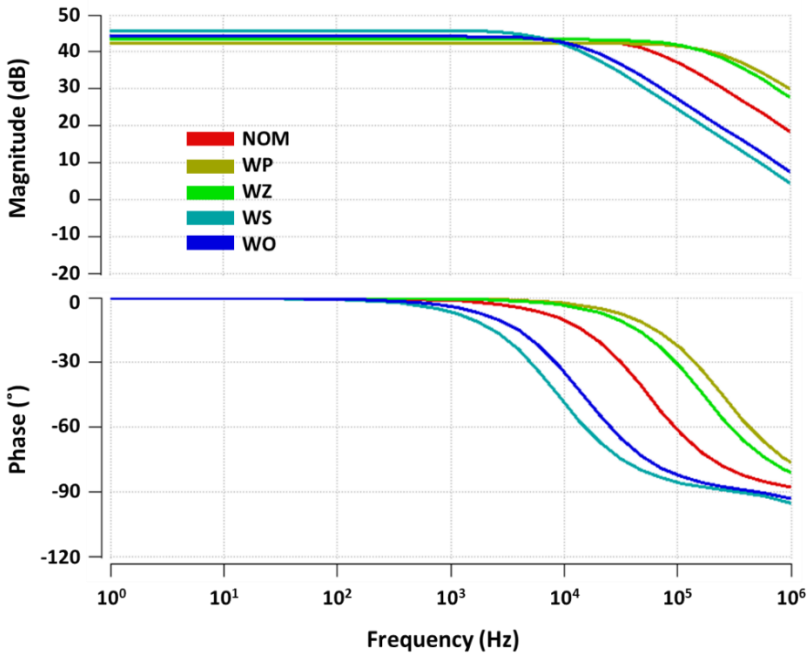


Figure 2.9. AC analysis of the rectifier comparator (Corners can be seen from Table 2.1.)

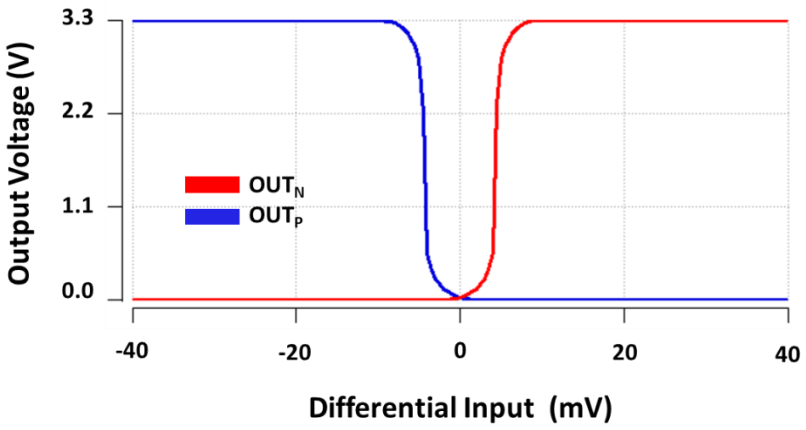


Figure 2.10. DC analysis of the comparator

2.2.3. Sample and Hold Circuit

Sample & hold circuit is used for acquiring DC peak voltage from the rectified signal and holding this DC peak for a certain time. Since the rest of the circuit determines the pulse width, the change at the DC voltage results in unbalanced stimulation. The sample time and hold time are 125 μs which is the same with the single channel stimulation time. The sample & hold circuit (Figure 2.11) consists of 4 branches which are controlled with 4 control signals. These branches are used to have easy time management and continuous operation. If one branch structure is activated, the output voltage can be sampled every 375 μs for 125 μs. Every branch uses 3 phases which are charge, hold and discharge. In the first phase, the capacitor is connected to the input via diode and charges to peak of the input voltage. In the second phase, the capacitor voltage is connected to the output and holds the voltage for a certain time. In the last phase, the capacitor is shorted and discharged to zero volts. The sizes of the switches are arranged to minimize the leakage current and have fast charging.

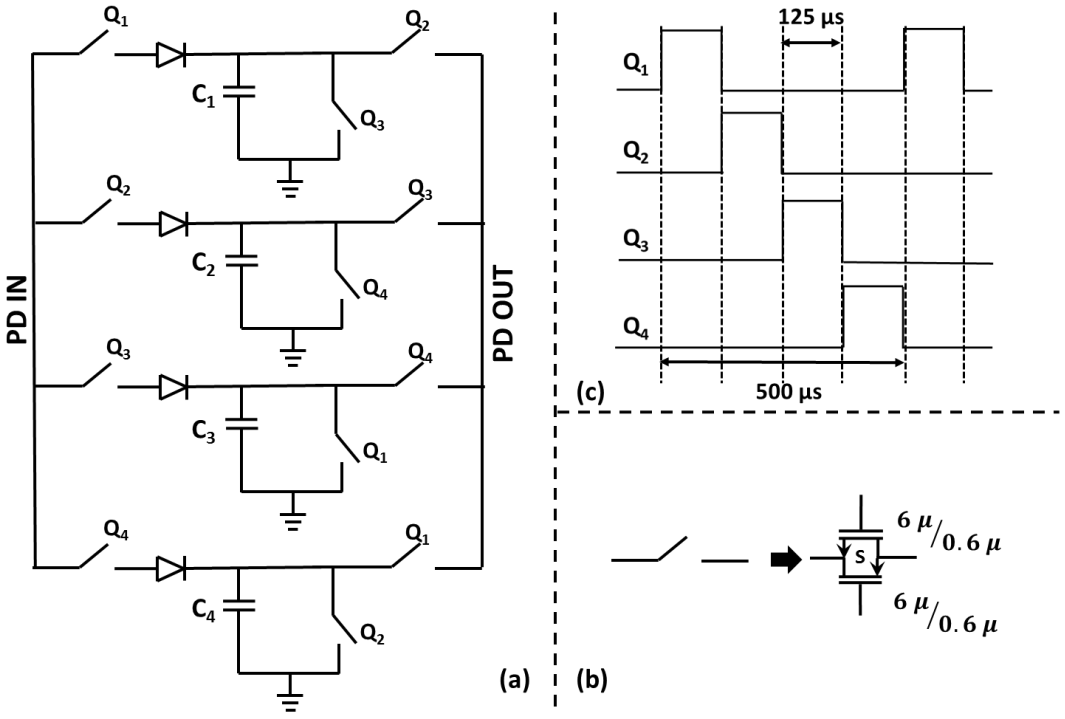


Figure 2.11. Sample hold circuit schematic (a), switch sizes (b), operation time diagram (c)

Transient analysis of the sample hold circuit is given in Figure 2.12. The control signals are given in binary form. The output follows the input with a certain level difference due to diode structure. Since the input comes over a certain DC offset, the diode voltage reduction does not affect to operation. The output spikes do not effect the operation since the next block bandwidth is not high and filters the spikes.

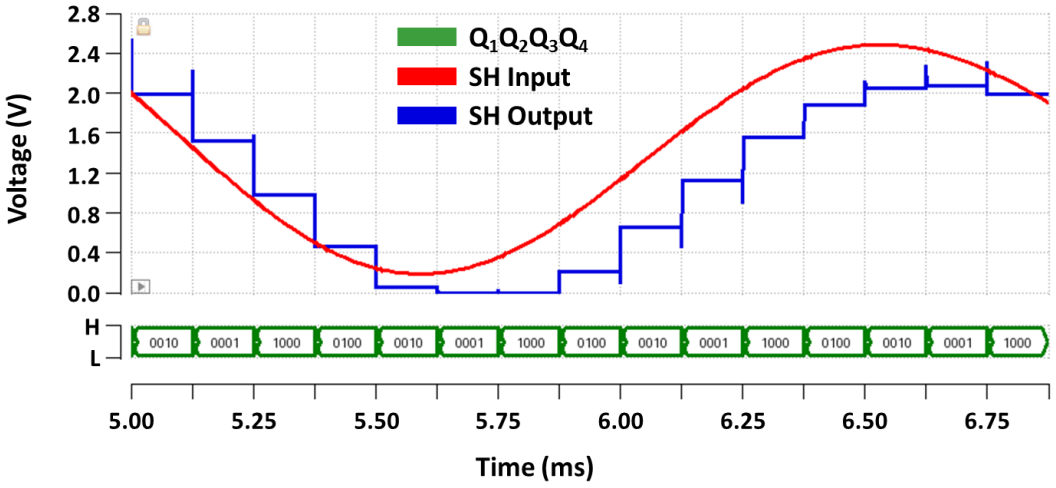


Figure 2.12. Sample hold circuit transient analysis

2.2.4. Logarithmic Voltage to Current Converter

The logarithmic voltage to current converter is used for compression and current output. The compression is necessary for a cochlear implant system since the sound input range is between 40 dB to 120 dB. The circuit makes a mapping for 60 dB (60 dB – 120 dB) input range to 12 dB output biphasic current range. The circuit should convert the input voltage to the output current for the comparison. These two operations are combined in this block. Schematic of the circuit can be seen from Figure 2.13 and the transistor sizes are tabulated in Table 2.2. The circuit uses three different currents for the output generation which are reference current (I_{REF}), PMOS current (I_P) and NMOS current (I_N). I_{REF} is generated by a constant voltage and used a bias limiter. The reference current is copied by M_2, M_3, M_{14} and M_{15} and the input voltage DC level is shifted by a reference current on M_{10}. This shifted input voltage generates logarithmic current I_P on M_1, since M_{12} transistor is forced to operate under threshold

by DC shift. However, as the input increases, the I_P current is getting smaller and loses its effect. In this region, M_{11} generates the logarithmic current I_N by working under threshold condition which is kept under threshold with the M_8 and M_{18} diodes. The output current (I_{OUT}) is generated by subtracting, I_P and I_N currents from the multiple of the reference current (αI_{REF}).

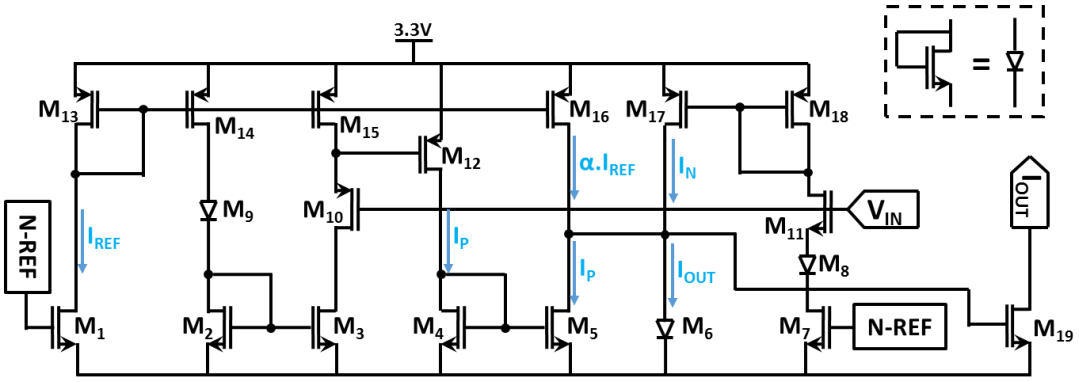


Figure 2.13. Schematic of the logarithmic voltage to current converter circuit

Table 2.2. *Transistor sizes of the logarithmic V-I converter circuit*

M_1	3 µ / 5 µ	M_6	10 µ / 1 µ	M_{11}	1 µ / 5 µ	M_{16}	12 µ / 5 µ
M_2	3 µ / 5 µ	M_7	1 µ / 5 µ	M_{12}	1 µ / 9 µ	M_{17}	14 µ / 5 µ
M_3	3 µ / 5 µ	M_8	1 µ / 5 µ	M_{13}	2 µ / 5 µ	M_{18}	10 µ / 5 µ
M_4	4 µ / 5 µ	M_9	2 µ / 5 µ	M_{14}	2 µ / 5 µ	M_{19}	10 µ / 1 µ
M_5	1 µ / 5 µ	M_{10}	1 µ / 9 µ	M_{15}	2 µ / 5 µ		

The simulation results of the logarithmic voltage to current converter can be seen from Figure 2.14. The output of the circuit can be fitted on the logarithmic curve. The measurement and the simulation results are matched. However, at the low inputs, the comparison gain is different. Since the input voltage is too low, this does not create a major problem. The output biphasic current bandwidth error is around 1 to 2 µs which is a tolerable output error.

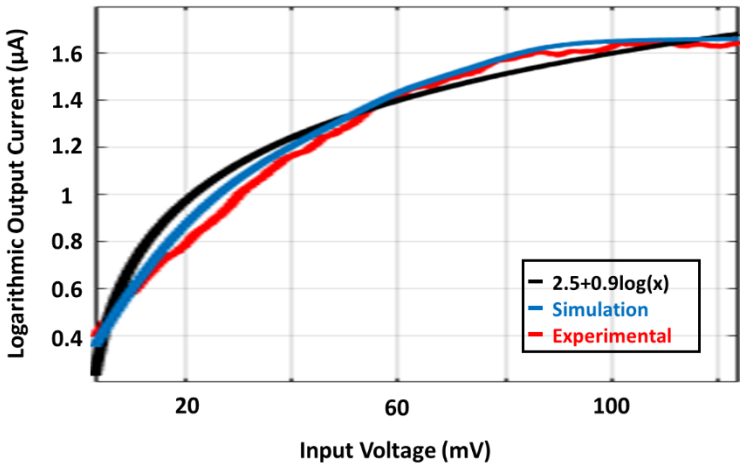
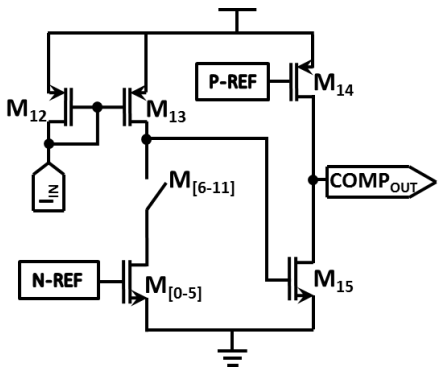


Figure 2.14. DC analysis of the logarithmic V-I converter

2.2.5. Current Comparator

The current comparator is used to determine the pulse width of the output current. The logarithmic current is compared with a reference current which is generated from 6 bit Digital to Analog Converter (DAC). The reference current value is controlled by $M_{[6-11]}$ transistors according to the digital counter. If the reference current passes the input current value the counter is stopped, and the counter time become the output current pulse width. The schematic of the current comparator is given in Figure 2.15. M_{14} and M_{15} construct the pseudo inverter to prevent glitches. In addition, a CMOS inverter is added to the output for rail to rail operation. Figure 2.16 shows the output reference current respect to digital inputs. The least significant bit (LSB) of the system corresponds to 16.5 nA output current.



M_0	1 µ / 3 µ	M_8	4 µ / 3 µ
M_1	2 µ / 3 µ	M_9	8 µ / 3 µ
M_2	4 µ / 3 µ	M_{10}	16 µ / 3 µ
M_3	8 µ / 3 µ	M_{11}	32 µ / 3 µ
M_4	16 µ / 3 µ	M_{12}	40 µ / 3 µ
M_5	32 µ / 3 µ	M_{13}	40 µ / 3 µ
M_6	1 µ / 3 µ	M_{14}	10 µ / 3 µ
M_7	2 µ / 3 µ	M_{15}	10 µ / 3 µ

Figure 2.15. Schematic of the current comparator circuit

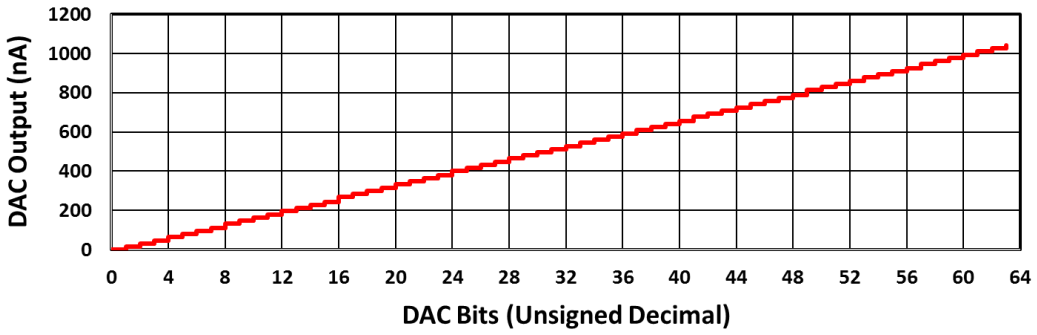


Figure 2.16. Reference current output

Figure 2.17 shows the performance of the DAC with integral nonlinearity (INL) and differential nonlinearity (DNL) errors. INL is the absolute difference between the ideal current and the actual value. The maximum INL error is 0.35 LSB and acceptable for our operation. DNL is the deviation between two analog values correspond to adjacent input digital values. The maximum DNL error is 0.6 LSB, which is less than one LSB, so the DAC has monotonic transfer function.

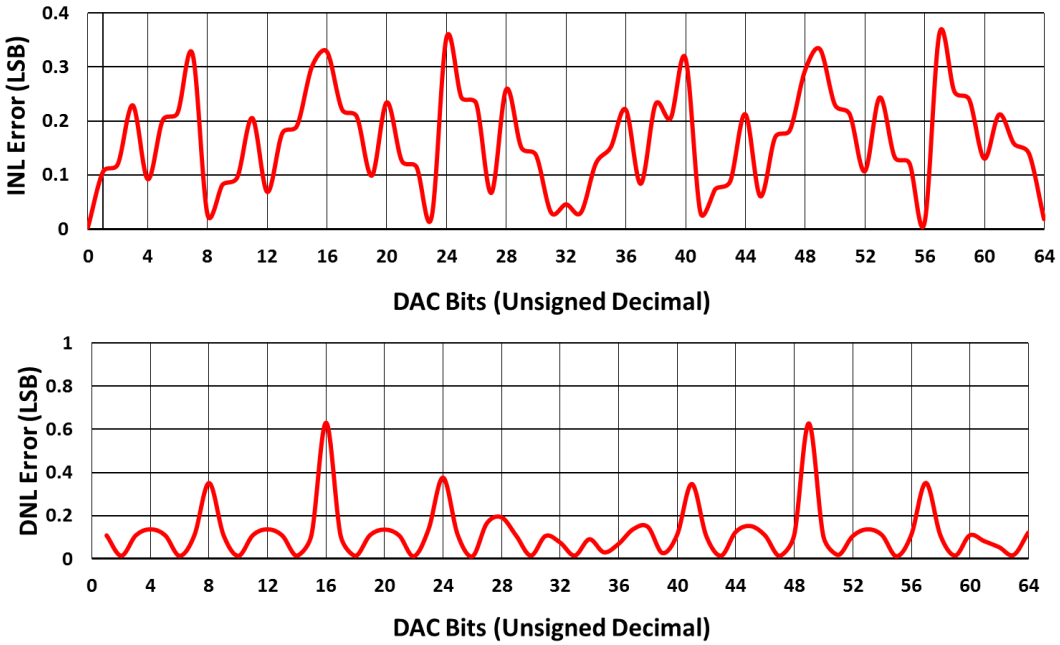


Figure 2.17. DAC reference current INL error and DNL error

2.2.6. Control Block

Control block (Figure 2.18) generates all digital signals of the circuits with clock and current comparator output. The main counter is 9-bit counter and controls the other counters. The most significant 3-bit (K<7:9>) of this counter determines active channel number, amplifier enable bits and sample hold circuit bits. 6-bit counter controls DAC bits and current comparator output reset this counter. After reset, operation, 6-bit counter starts to count again for another phase. The 1-bit counter determines the phase of the stimulation. In the first phase, it is low (S_2 = L) which means cathodic phase (C<1:8>). When the count is high (S_2 = H), anodic phase is enabled (A<1:8>). 1 to 8 demultiplexer circuit determines the channel number and 1 to 2 demultiplexer determines the phase. Common electrode signals (A<0> and C<0>) are determined by 8 input NOR gates. All digital signals are generated with 1.5 Volts supply, and they need to be level shifted for other blocks.

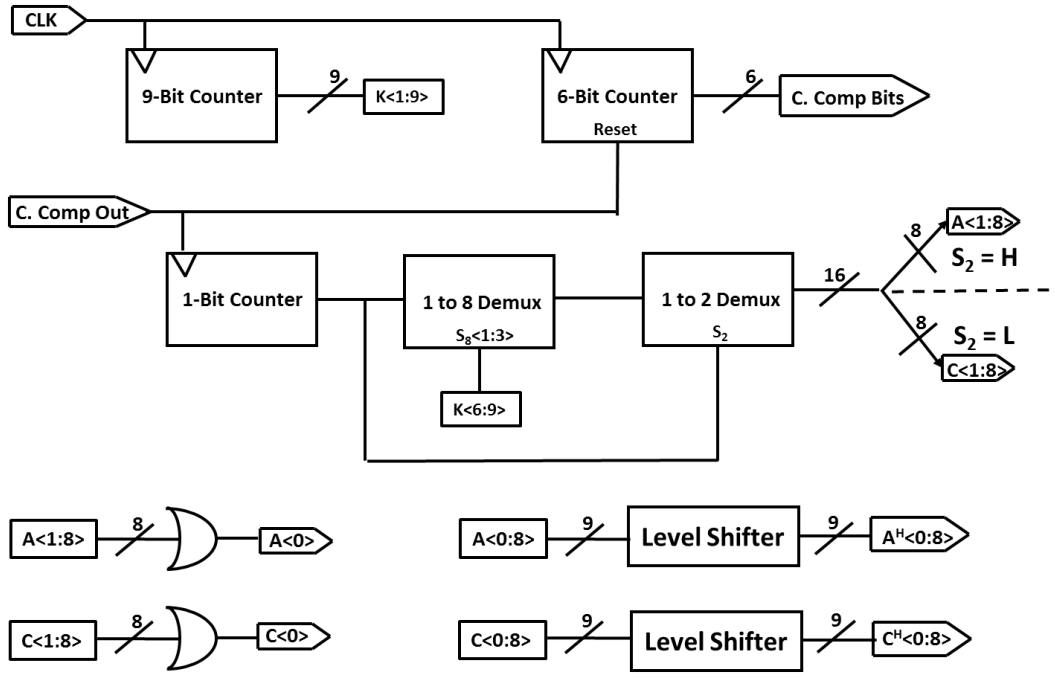
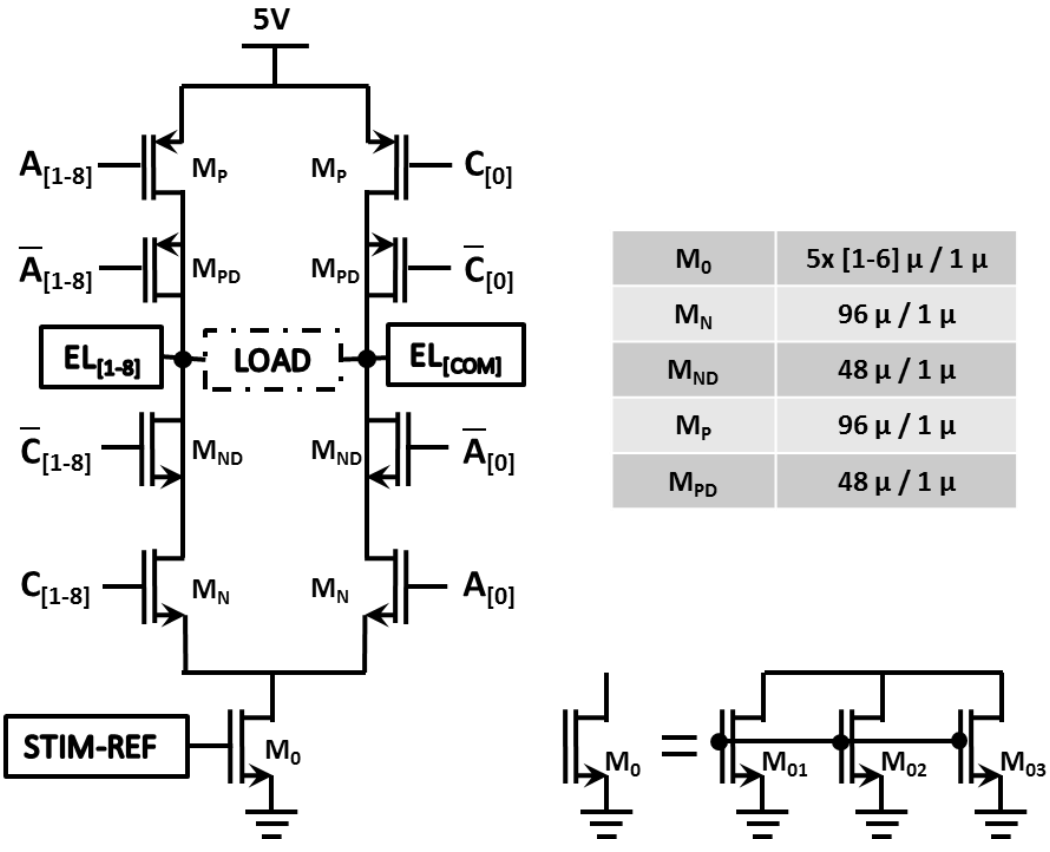


Figure 2.18. Logic diagram of the control block

2.2.7. Stimulator Circuit

Stimulator circuit provides high currents to the nerve in two different phases. Stimulator type of the designed FICI is a single supply constant current control stimulator. The M_0 transistor generates constant current for the stimulation and it consists of 3 different size transistors. The width of these transistors is 1 μm (M_{01}), 2 μm (M_{02}) and 4 μm (M_{03}). By these transistors constant current can be adjusted for each patient. In the anodic phase, one of the $A_{[1-8]}$ switch is set to low, $A_{[0]}$ switch is set to high and current flows from electrode ($EL_{[1-8]}$) to common electrode (EL_{COM}). In the cathodic phase, the current flows in reverse direction with the enabling "C" switches (The operation principle is same with the switch matrix of [25]). M_{ND} and M_{PD} transistors are added for eliminating charge insertion errors to minimize unbalanced charge after the stimulation [43].



M_0	5x [1-6] μ / 1 μ
M_N	96 μ / 1 μ
M_{ND}	48 μ / 1 μ
M_P	96 μ / 1 μ
M_{PD}	48 μ / 1 μ

Figure 2.19. Stimulator circuit schematic

2.2.8. Clock Generation

Figure 2.20 shows the schematic of the clock generator. The circuit contains 3-stage current starved ring oscillator, a hysteresis (HYS) and a CMOS inverters. The voltage-controlled oscillator (VCO) has a feedback connection between its 3rd inverter output and 1st inverter input. The clock signal is constructed from delays of the inverters which is controlled by M_0. The hysteresis inverter is added to the circuit for glitch elimination. CMOS inverter is added to the system to increase driving capability of the clock signal.

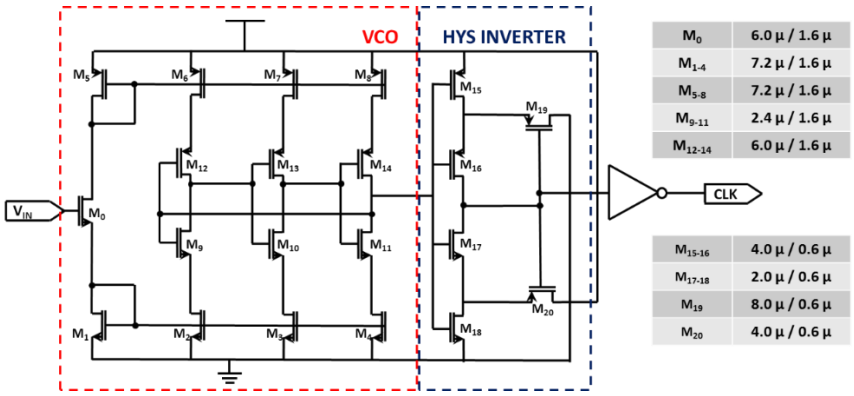


Figure 2.20. Schematic of the clock generator

The clock generator transient simulation is given in Figure 2.21. The circuit generates rail-to-rail clock signal with 1.5 V supply. The frequency deviation of the output is 5 kHz which is acceptable for the operation since it is very low. The spikes at the output does not create any problem because digital circuits change their states at mid voltage levels (1.65 V)

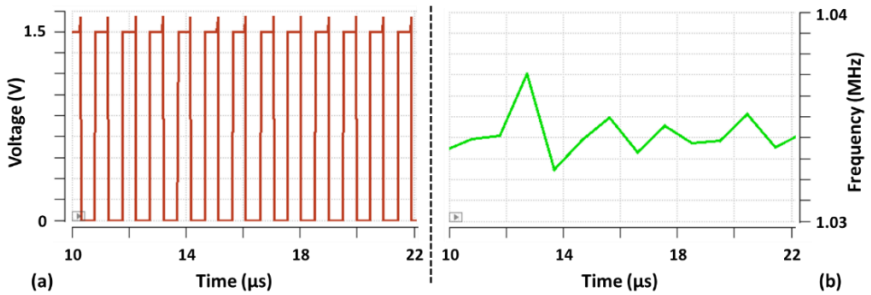


Figure 2.21. Oscillator transient analysis output voltage (a), output frequency (b)

2.2.9. Simulation of the Overall Circuit.

The FICI interface circuit is designed and implemented in 180 nm high voltage (TSMC Taiwan Semiconductor Manufacturing Company) process. The layout of the circuit can be seen from Figure 2.22 and for all simulations the extracted view of the layout is used. The active area of the design is 1 mm x 0.5 mm and the area with pads is 1.2 mm x 2.5 mm.

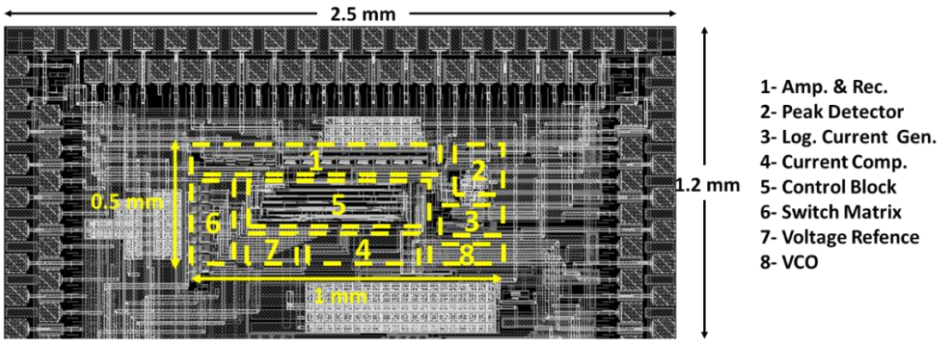


Figure 2.22. Layout of the FICI interface circuit

The power consumption of the interface circuit is simulated with a constant 10 mV input voltage (Table 2.3). While analog blocks consume 16 µW from 3.3 V supply, the digital blocks are driven with 1.5 V supply with 4.5 µW power consumption. Also, the stimulator and its drivers consume 481 µW from 5 V supply which is 93.7% of the total power.

Table 2.3. *Simulated Voltage Consumption of the Circuit*

Circuit Blocks	***Supply***	***1-ch***	***8-ch***
Amplifier	3.3 V	1.3 µW	10.5 µW
Voltage Rectifier	3.3 V	2.8 µW	2.8 µW
Logarithmic V to I	3.3 V	5.2 µW	5.2 µW
Current Comparator	3.3 V	5.5 µW	5.5 µW
Stimulator	5.0V	61.5 µW	481 µW
Clock Generator	1.5 V	0.3 µW	0.3 µW
Front-End Circuit	-	20.3 µW	32.0 µW
Total	-	82.0 µW	513.0 µW

The overall simulation of the interface circuit is made by an increasing ramp input (Figure 2.23). The simulation results show that the biphasic current is generated after a certain input voltage. The output current pulse-width increases by the increasing input. The maximum channel duration is 125 µs and the maximum pulse width is 62 µs. The 8 channels are stimulated one by one with 125 µs time difference. Every channel period is set to 1 ms and each channel has constant 400 µA peak current amplitude.

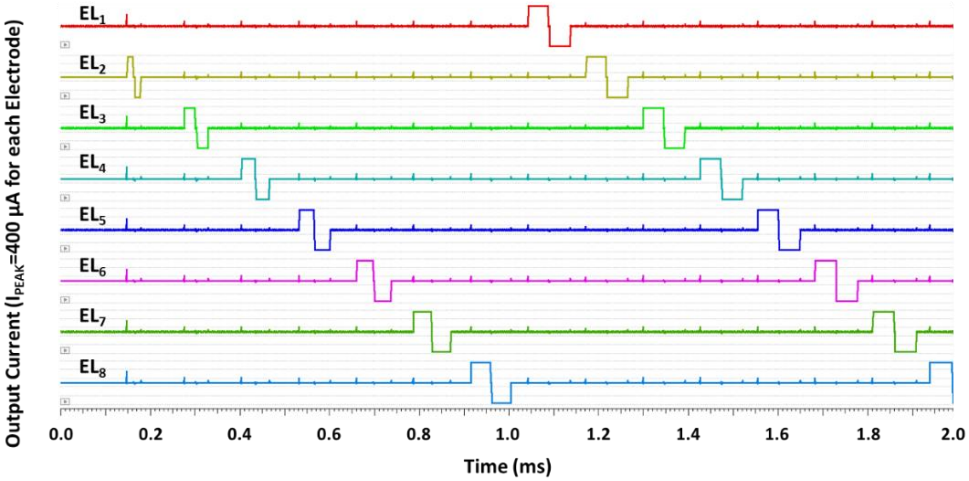


Figure 2.23. Overall circuit transient analysis for a ramp input

2.3. Experimental Test Results

The experimental tests are made by fabricated chip whose micrograph is given in Figure 2.24. Printed circuit board (PCB) (Figure 2.25) is designed for electrical and acoustic tests. At the output, a series RC circuit is connected as an artificial neural load (3 kΩ and 100 nF) [44].

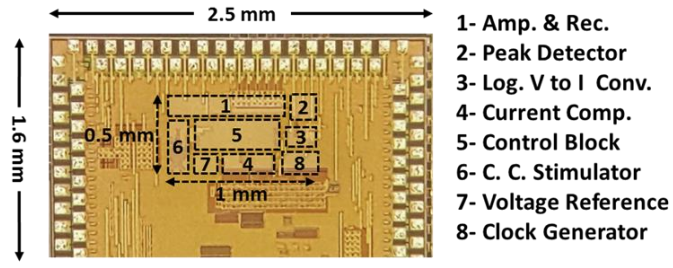


Figure 2.24. The micrograph of the fabricated chip

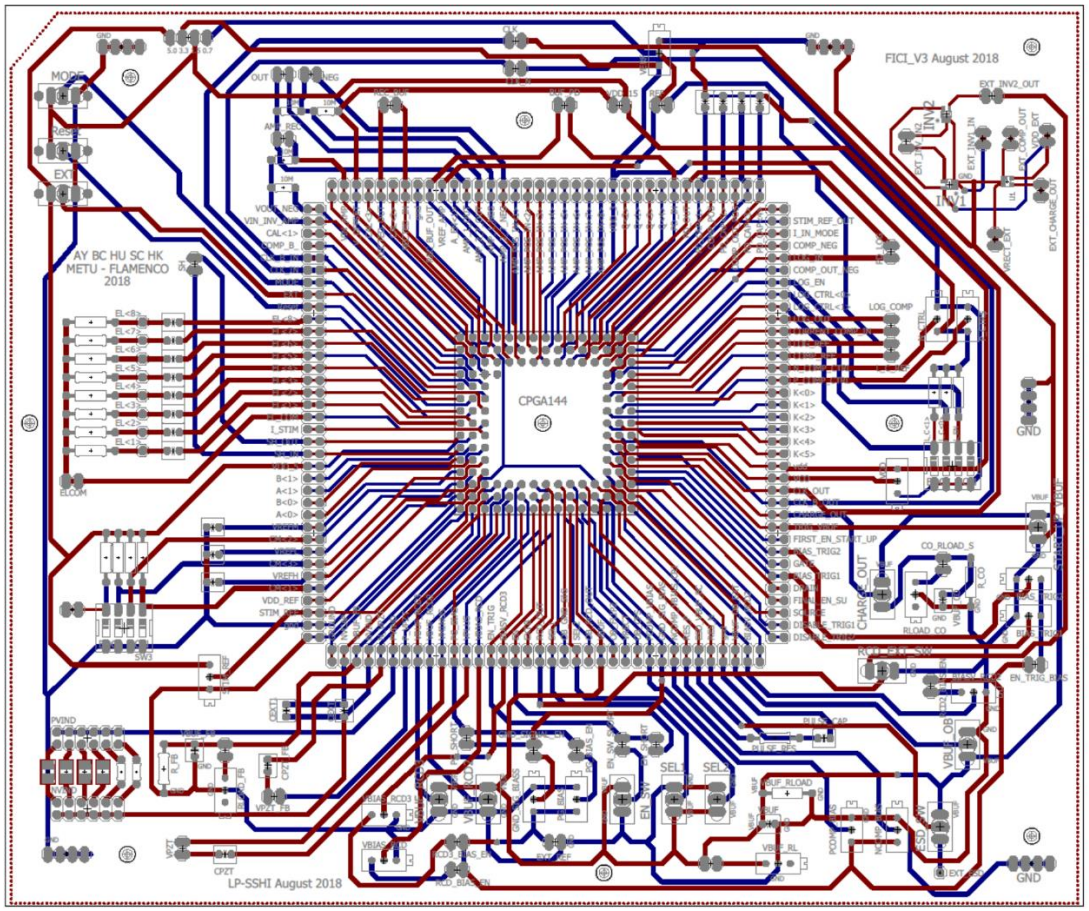


Figure 2.25. FICI system test PCB layout

2.3.1. Electrical Tests

The electrical tests are made to observe operation of analog blocks and stimulation current waveforms. Figure 2.26 shows the analog block analysis for amplitude modulated (AM) input. AM signal is used to observe the rectification operation, because sinusoidal input results in DC output. For that purpose, the AM signal is constructed with 300 Hz signal tone with 3 kHz carrier frequency. From the results, minimum voltage for rectification is around 1 mV and the offset of the rectifier is below 5 mV which are acceptable for the circuit operation. The logarithmic current output is higher than the expected value due to process variations. This problem is solved by increasing current comparator reference voltage by 10%.

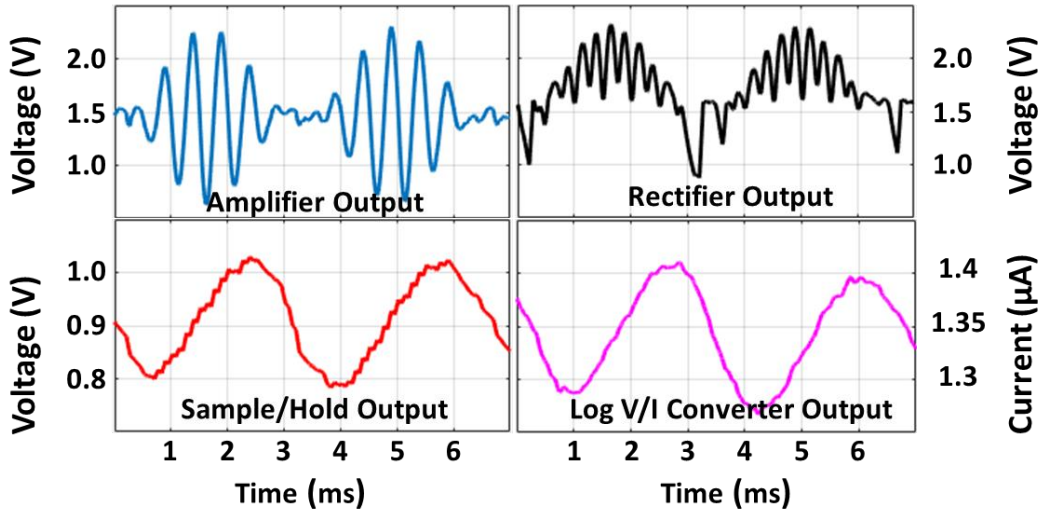


Figure 2.26. Transient analysis of the analog blocks.

The single channel stimulation is tested with constant 1 kHz sinusoidal input to observe generated biphasic current. The period of the stimulation current is 1 ms with 400 µA peak value, and time of the anodic and cathodic pulses are equal. This implies that charge balanced operation can be performed with this circuit which is suitable for 8 channel operation.

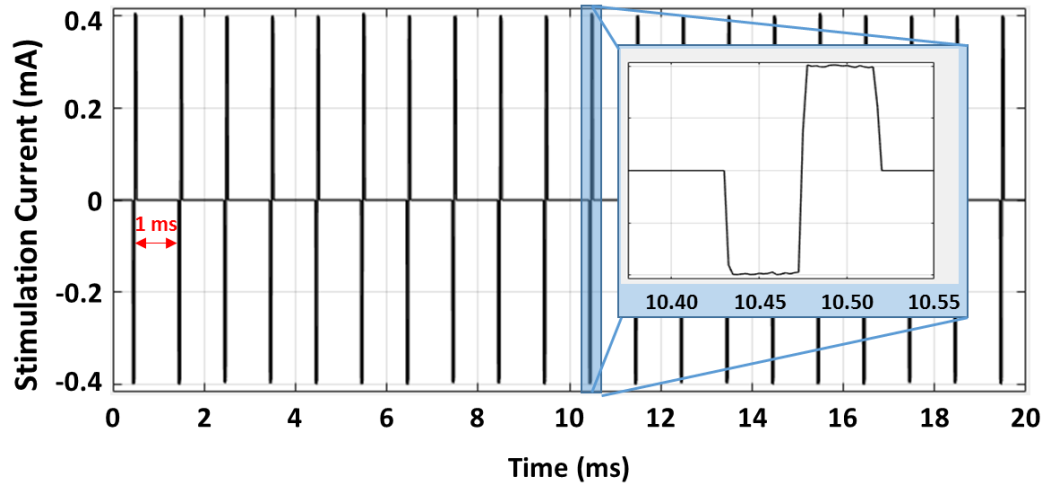


Figure 2.27. The generated output biphasic currents respected to constant input signal

The pulse width of the generated output currents varies from 18.5 µs to 60 µs with changing input voltage amplitude. Figure 2.28 shows the injected charge respect to input voltage. The injected charge changes from 7 nC to 24 nC while input changes 1 mV to 130 mV. Interface circuit can compress 45 dB input range to 10 dB. The amount of the charge can be controlled with the stimulation current amplitude and it can be increased up to 1.5 mA. However, impedance of the load limits the maximum current rating.

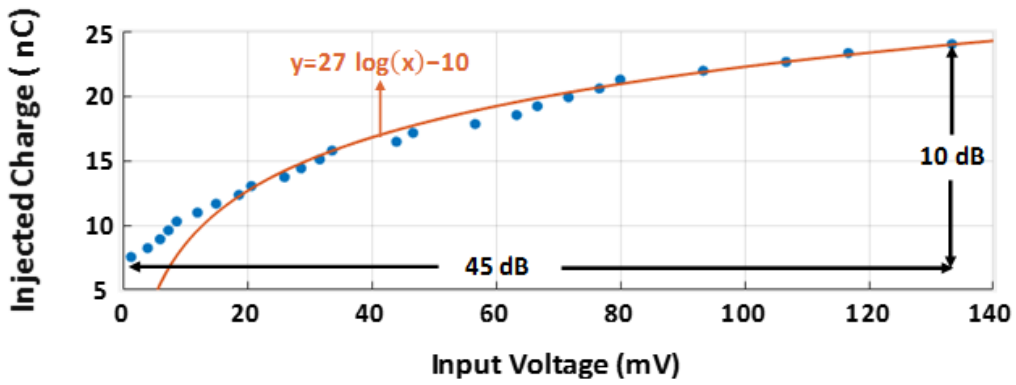


Figure 2.28. The injected charge amount respect to input voltage

2.3.2. Sound Tests

The FICI interface circuit is tested with a constant sinusoidal sound input. The test setup can be seen from Figure 2.29 (block diagram at Figure 2.30). The sound input is given with the earphone to the single channel piezo-electric sensor [20] which is placed in ear-canal model. The ear canal model length is the average ear canal length of an adult. The microphone is inserted with the headphone to determine the sound input level. The FICI interface circuit is placed on the test PCB and connected to the power supply.

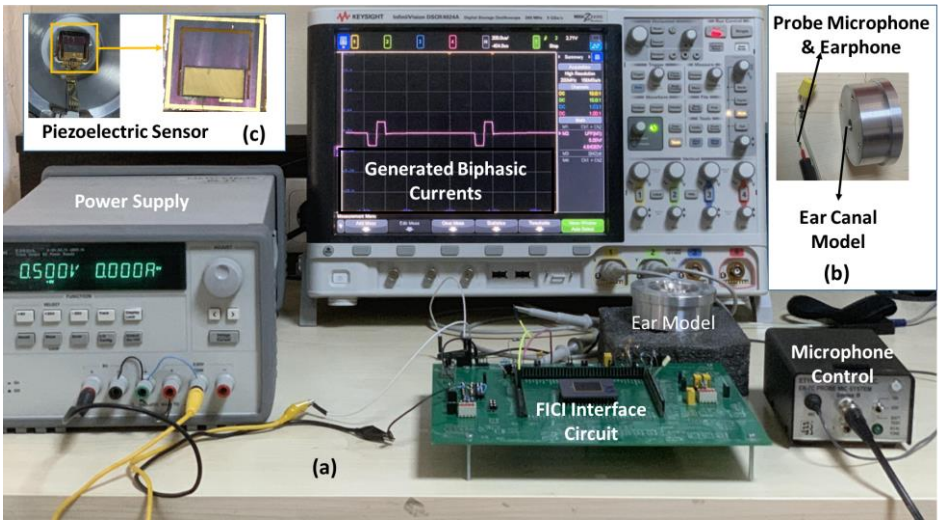


Figure 2.29. Sound Test Setup (a), ear model (b), piezo-electric sensor (c).

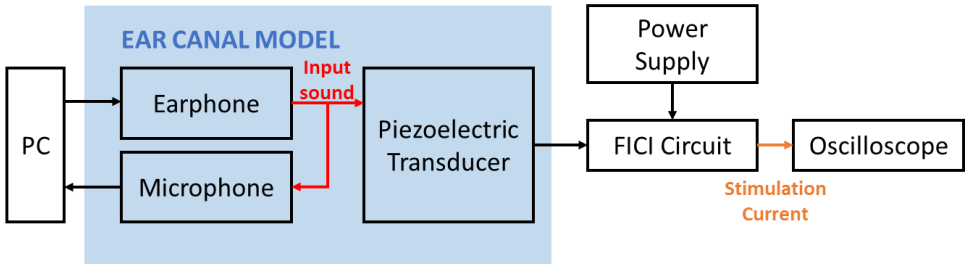


Figure 2.30. The block diagram of the test setup.

The input signal frequency is set to 800 Hz, also the input sound pressure level (SPL) is changed from 60 dB to 105 dB and the output current is generated on electrical load. The current waveforms are recorded via oscilloscope and can be seen from Figure 2.31. All generated current waves have the same amplitude and period, which are 400 μA and 1 ms respectively. Threshold of the system is calculated as 60 dB SPL. The biphasic current pulse widths are changed from 18.5 μs to 60 μs while input changes from 60 dB to 105 dB.

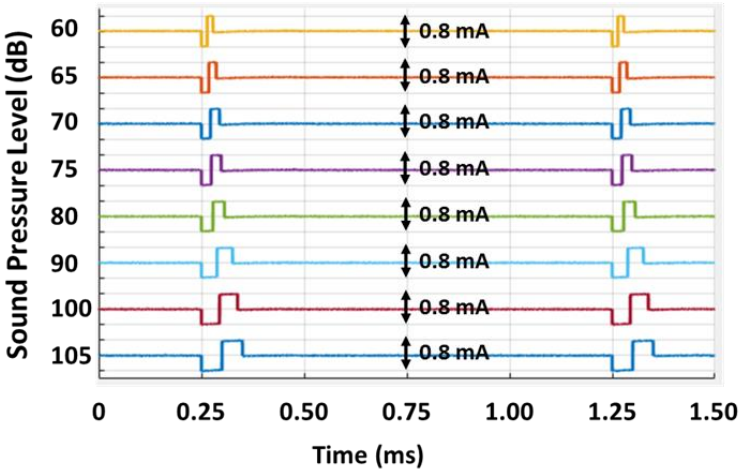


Figure 2.31. The generated output current waveforms respect to input SPL

Figure 2.32 shows the injected charge to the electrical load in the one phase respect to input sound pressure level. The output charge varies between 6 nC to 20 nC with 45 dB input change. This input range is compressed to 10.4 dB output stimulation range, and the injected charge follows a linear trend line. With these linear electrical compression higher sound perception and speech recognition can be achieved.

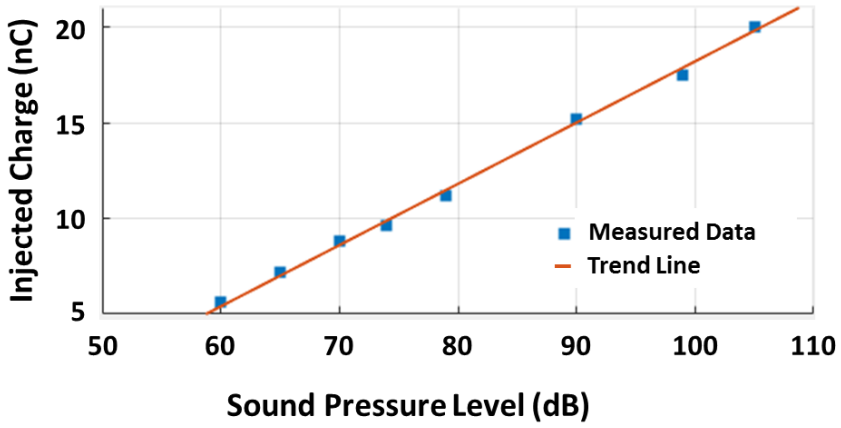


Figure 2.32. Injected charge to the electrode according to the SPL of the sound

2.4. Summary of the Chapter

In this chapter, first generation pulse width modulated FICI interface circuit is introduced. The circuit takes input from piezo-electric sensors and is amplified with subthreshold op-amps. After the amplification, its envelope is taken by active rectifier

and low pass filter. The envelope is converted to the DC signal by sample hold circuit and DC voltage is converted to the current and compressed with the novel logarithmic converter. The logarithmic current goes into current ADC and digitalized for determining pulse width of the generated biphasic currents. The system is tested with an electrical model of the electrode tissue interface and the system provides 9 nC/phase for 70 dB single tone input. The comparison with the state of the art FICI interface circuit is given in Table 2.4. System consumes 513 µW power of which front-end power is 32 µW by occupying 0.6 $mm^{2,}$ which were the lowest values up to September 2019.

Table 2.4. *Comparison with state of art FICI system*

Parameter	[22]	[23]	[24]	[45]	***This Work*** [46]
Technology	*1.5 µm*	*1.5 µm*	*0.18 µm*	*0.18 µm*	*0.18 µm*
Electrode Number	*8-16*	*8-20*	*8*	*8*	*8*
Dynamic Range (dB)	77	60	60	40	45
Actieve Area (mm^2)	88.3	21	3.36	0.6*(1)*	0.5
Stimulation Method	AM	AM	AM	AM	PWM
Front End Power (μW)	211	*126*	93	51.2	*32*
Total Power (μW)	-	2126*(2)*	572	691.2	513

(1) Calculated from chip micrograph.

(2) Stimulator is not designed and its power is predicted by [23] as 2 mW.

CHAPTER 3

PWM FICI WITH ACTIVE CHARGE BALANCE CIRCUIT

3.1. Motivation

In this design, the FICI introduced in the previous chapter is improved and charge balance circuit, DC-DC converter and voltage reference circuit is added to the system. The input stage is changed from voltage mode to current mode for simple addition circuit. The novel voltage to current converter circuit is replaced with a passive diode and voltage oscillator circuit is improved for more stable clock signal. In addition to the previous design the low power voltage reference circuit is added with 3 different voltage outputs for operating fully on-chip. Moreover, the DC-DC converter is added to the system for decreasing supply number. The circuit operates with a single 1.8 V supply.

The charge balance circuit is implanted to the system for safe operation and it limits the electrode voltage difference within the range of 100 mV. For charge balancing short pulse injection method is used similar to [47], [48]. However, it is improved for low power consumption and multi-channel operation. The charge balance circuit monitors the electrode voltage and compares with an offset in window comparators. If the offset is higher than 60 mV, the charge balance current is generated to neutralize the unbalanced charge.

The overall system is tested with in-vitro test setup and it can generate pulse width modulated output currents with charge balancing while using a single supply, on chip oscillator and voltage reference circuit. The circuit can work with 50 dB input dynamic range while consuming less than 1 mW power.

3.2. Charge Balanced FICI Circuit Design and Description

The charge balanced FICI interface circuit block diagram is given in Figure 3.1. The input voltages are generated from sound vibration by 8 distinct channel piezo electric transducers. Clock gated trans-conductor amplifiers are used for amplifying the output of the piezo electric transducers and current rectifier is used to extract amplitude information. The system uses CIS strategy and one channel is active all the time, the output currents of 8 rectifier block can be added with current mirrors. The rectified current (I_{REC}) is logarithmically compressed and converted to the voltage on a diode for storage. Diode voltage goes to analog to digital converter (ADC) and pulse width of the stimulation is determined by digital output. The ADC digital output is converted to the stimulation control bits and amplitude of the stimulation is determined by patient fitting bits. After the stimulation, the charge balance circuit monitors the electrodes and generates charge balance currents to compensate the mismatches of the biphasic current phases. If the difference between electrode voltages is higher than 60 mV, short charge balance current is generated. In the electrode voltage difference determination, window comparators are used.

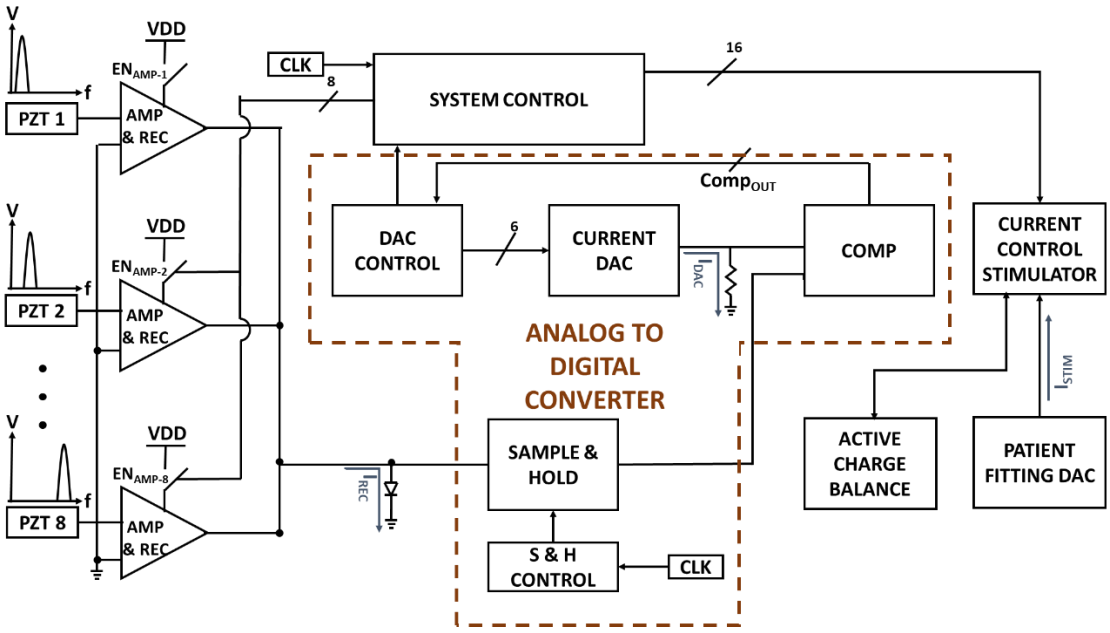


Figure 3.1. Block diagram of the charge balanced FICI system

3.2.1. Input Trans-Conductance Amplifiers and Current Rectifier

Before the digitization, the transducer outputs have to be processed with analog blocks. The block diagram of the amplifier and rectifier can be seen in Figure 3.2. The low gain transconductance amplifier takes the input voltage and converts it to differential current output. The gain of the amplifier is not high because the amplifier should work with 60 dB dynamic range. Rectified current is created by the absolute difference of the positive and negative currents. The M_1 transistor is added at the output of the rectifier for offset cancelation. The current of the M_1 should be set to offset of the 8 channel and it can be adjusted with V_{BIAS} voltage. The diode is used for both current to voltage conversion and compressing the input dynamical range. The compressing ratio also can be adjusted with V_{BIAS} voltage. In the structure, sub threshold MOS diode is used instead of P-N junction diode for high output range. The front-end analog blocks use 1.8 V and clock gating to decrease power consumption.

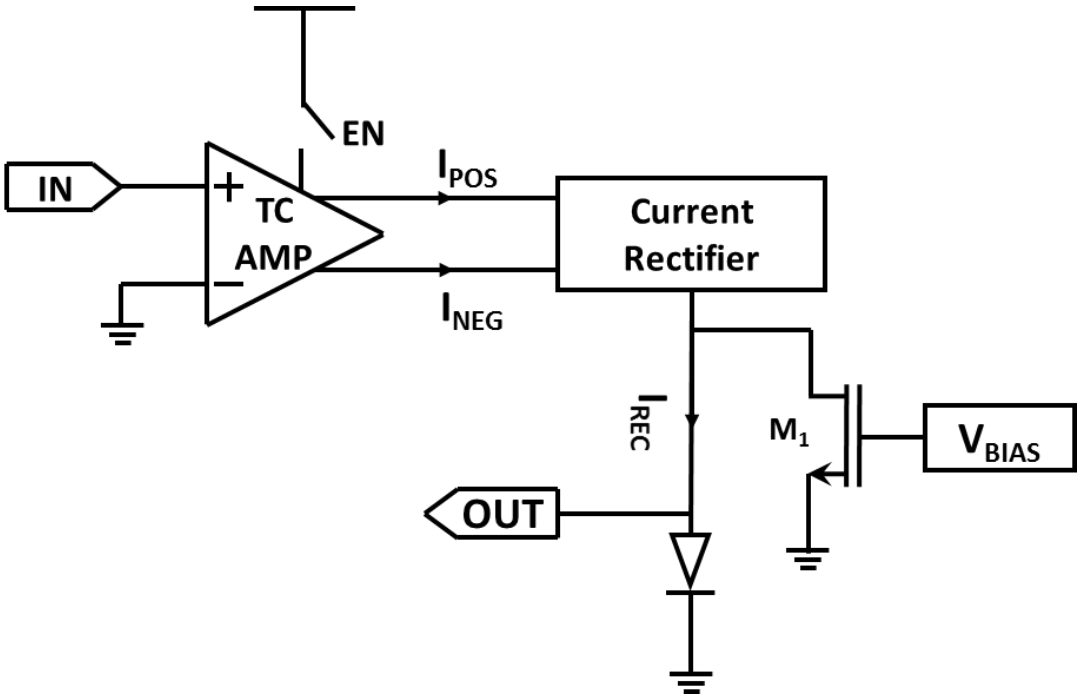
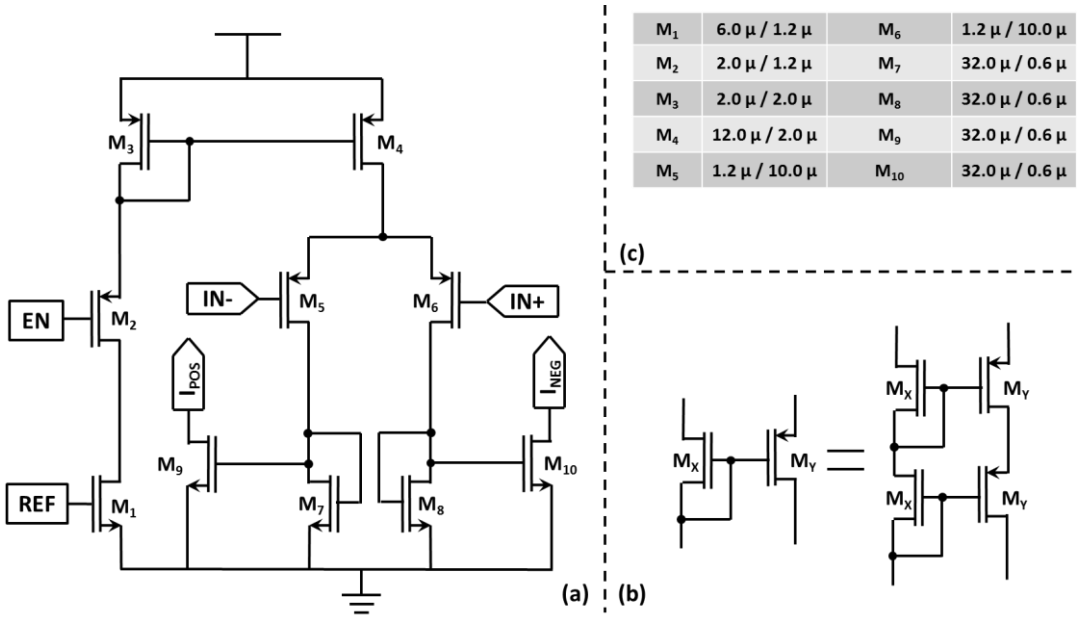


Figure 3.2. Block diagram of the input stage

Schematic of the transconductance amplifier is given in Figure 3.3. The input stage should have high dynamic range, low input noise, low power consumption and work with negative voltages. For high dynamical range, input gain is chosen as low as possible. For that purpose, the minimum detectable voltage is chosen as 400 µV and gain is set to 1.5 µA/V which is enough to cover up to 60 dB input dynamical range. The input referred noise level should be lower than 200 µV to achieve at least 12 dB SNR at the minimum input. The input pair is chosen as PMOS for negative voltage operations and low input referred noise figure. The transistors operate at low threshold condition and the supply of the amplifier is 1.8 V for low power consumption. For the negative and positive current symmetry, current mirrors should not be affected from channel length modulation. Hence, the all current mirror structure is cascaded current mirror to obtain high copying ratio and output resistance. When the EN signal low, the output currents and power consumption become zero.



M_1	6.0 µ / 1.2 µ	M_6	1.2 µ / 10.0 µ
M_2	2.0 µ / 1.2 µ	M_7	32.0 µ / 0.6 µ
M_3	2.0 µ / 2.0 µ	M_8	32.0 µ / 0.6 µ
M_4	12.0 µ / 2.0 µ	M_9	32.0 µ / 0.6 µ
M_5	1.2 µ / 10.0 µ	M_{10}	32.0 µ / 0.6 µ

Figure 3.3. Schematic of the operational amplifier (a) current mirror structure (b) and sizes (c)

The noise analysis result is given in Figure 3.4. The analysis is made by biasing the amplifier and giving the input zero. The input referred squared noise is simulated from 10 Hz to 10 kHz. Moreover, the input referred noise is calculated from square root of the area which is 156 µV. The input noise is smaller than the 200 µV and acceptable for our system. The noise can be further decreased by increasing reference voltage by consuming more power.

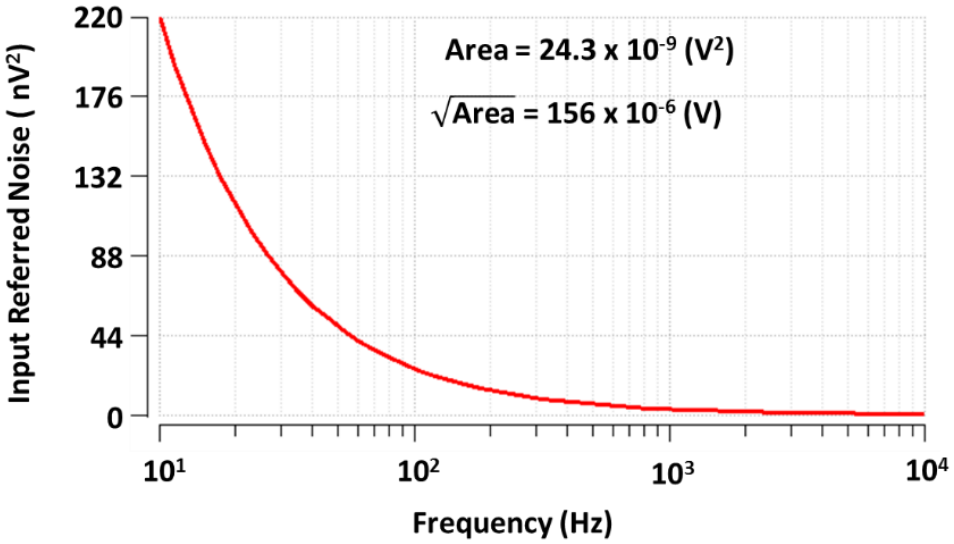
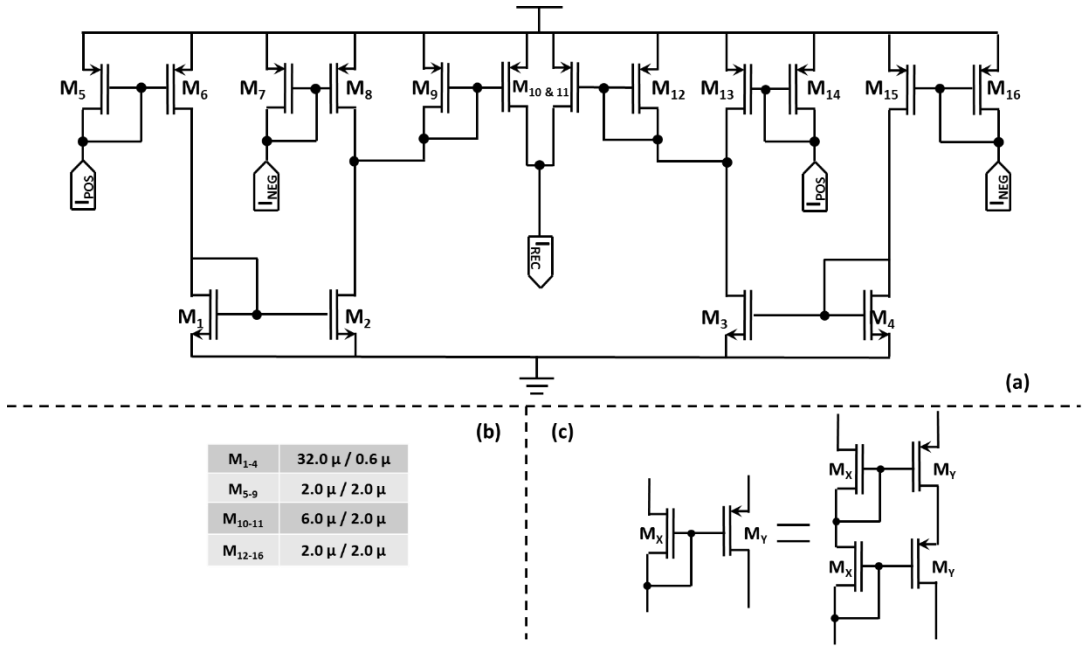


Figure 3.4. Analysis of input referred squared noise

The rectifier circuit schematic is given in Figure 3.5. It is a symmetrical structure and generates rectified current from the positive and negative currents. In this circuit, subtraction from lower currents to higher currents leads to zero which is used to create rectified current. Right side of the circuit subtracts I_{POS} from I_{NEG}. If I_{POS} is higher than I_{NEG} the output will be difference of the currents and other part contributes zero current. If I_{NEG} is higher, the left side operates and generates the output current. Also, in the design, the current mirrors are cascaded to enhance output resistance and decrease the channel length modulation effect.



M_{1-4}	32.0 µ / 0.6 µ
M_{5-9}	2.0 µ / 2.0 µ
M_{10-11}	6.0 µ / 2.0 µ
M_{12-16}	2.0 µ / 2.0 µ

Figure 3.5. Schematic of the current rectifier (a), transistor sizes (b) and current mirror sturcture (c)

Transient analysis of the system is performed, and results are plotted on the Figure 3.6. The input is given as 100 Hz sinusoidal input with 200 mV_{PEAK} and the positive and negative currents are generated with 180° phase shift. Output currents change from 40 nA to 340 nA, and the rectified current is applied to the diode. Logarithmic compression characteristic is achieved as an output voltage and it is connected to the sample hold circuit.

The DC analysis is performed for the circuit to observe compression rate and the input dynamical range (Figure 3.7). Circuits can operate from 400 µV to 400 mV which covers 60 dB range. The output is compressed between 140 mV to 340 mV which leads 8 dB electrical range. The compression range can be extended by adjusting the offset cancellation current and increasing the reference voltage.

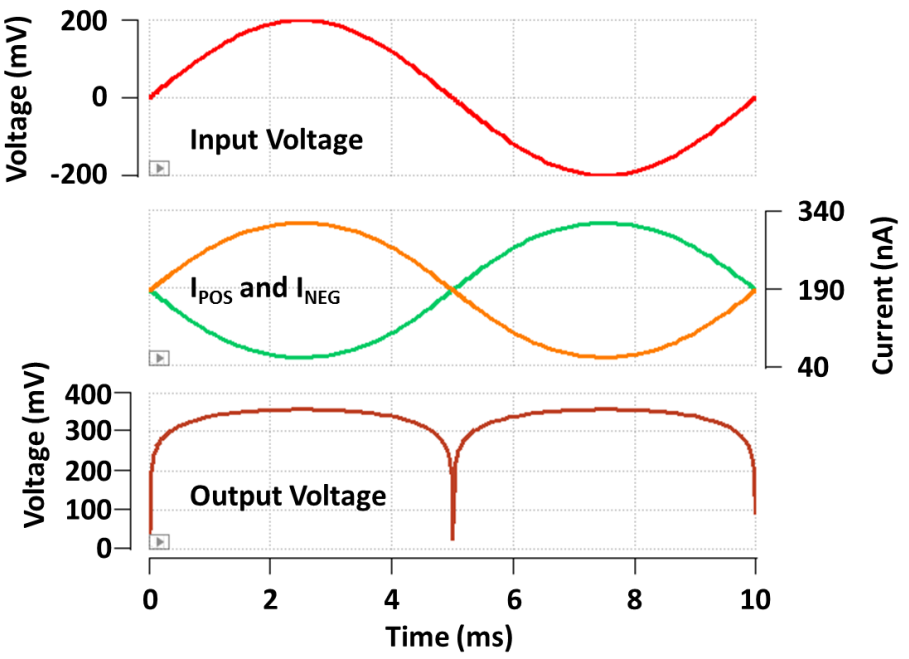


Figure 3.6. The amplifier and rectifier (diode load is connected to the rectifier) voltages when the input is sinusoidal wave with 200 mV_{PEAK} voltage and 100 Hz frequency

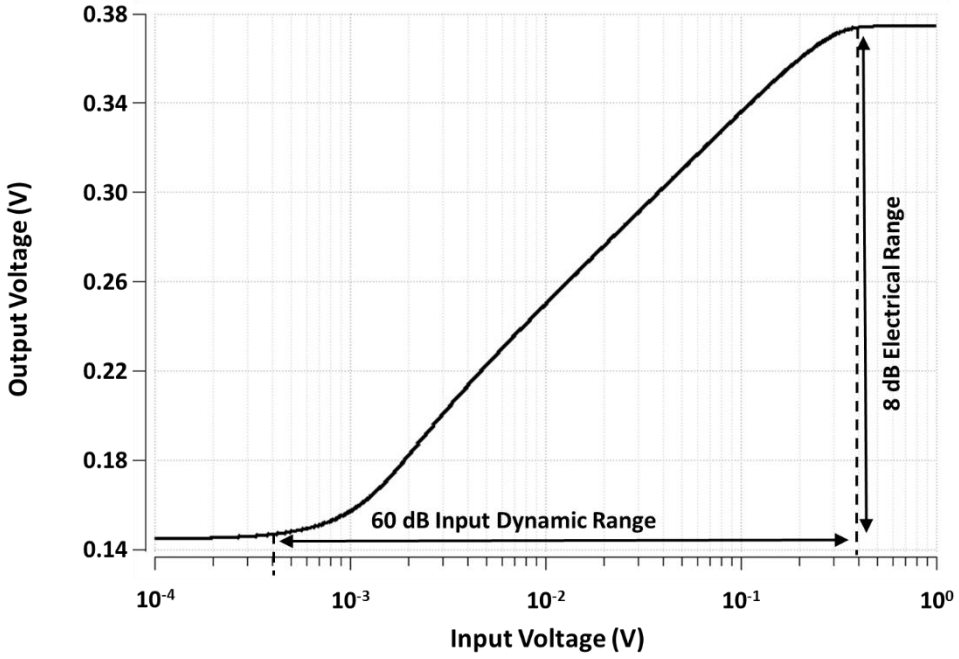


Figure 3.7. Output voltage of the rectifier respect to input transducer voltage with an output diode

3.2.2. Analog to Digital Converter

3.2.2.1. Sample & Hold Circuit

The same sample & hold technique is used with small changes compared to previous circuit (Figure 3.8). The diode structure is changed to low threshold transistor for decreasing the voltage drop. Triple diode is changed to single diode to prevent the effect of process variations in each branch. The branch number is decreased to three to lower the area occupancy. The control block of the circuit is implemented for shortening the layout nets for decreasing mismatches between the branches. The control block of the sample hold circuit is constructed by 3 bit shift register and an AND gate. The shift register input is generated from the inverse of the first and the second bits. The capacitor values are chosen as 9 pF to data storage for 125 μs. The switch sizes are optimized for current ratings and input capacitances.

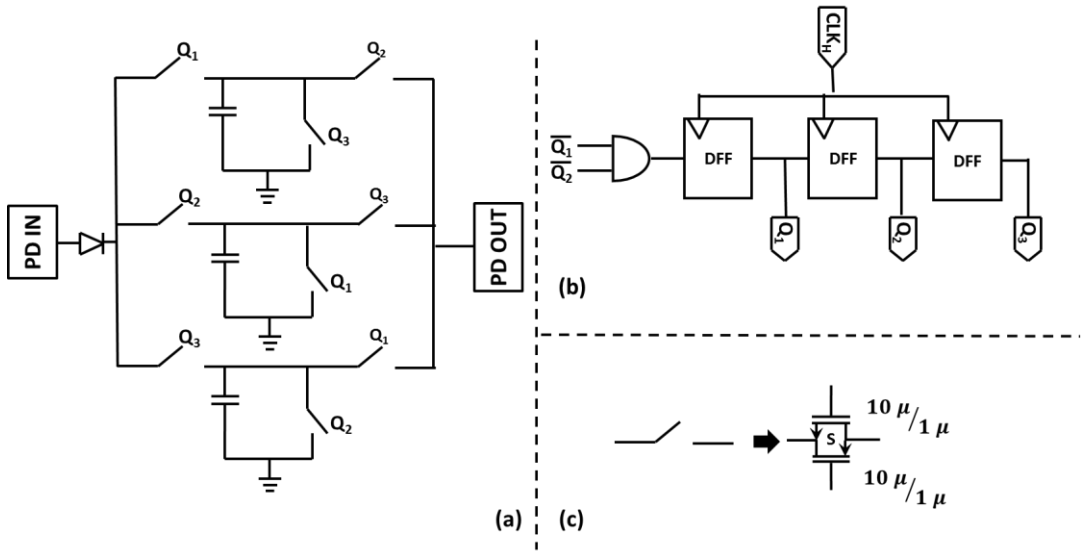


Figure 3.8. Sample & hold schematic (a), logic diagram (b), switch sizes (c)

The sample hold circuit simulation is given in Figure 3.9. The control signals are generated for 125 μs and the sampling operation is achieved with 100 mV difference. By increasing the on-chip capacitor values the generation of the spikes are eliminiated.

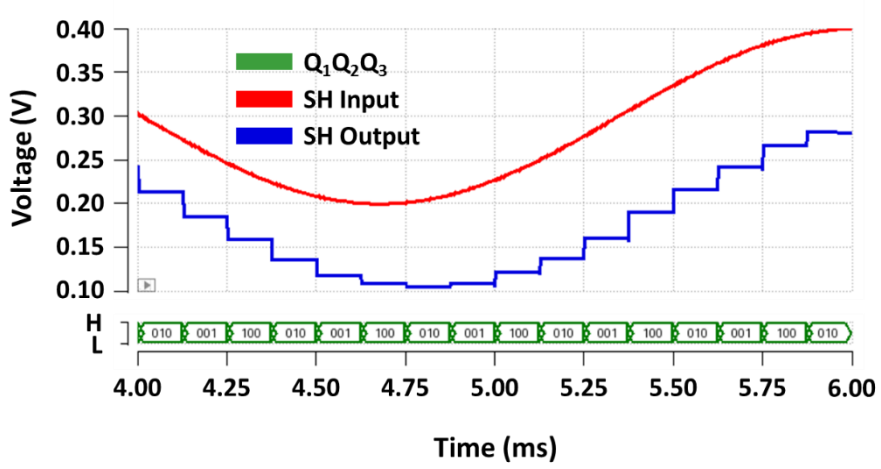
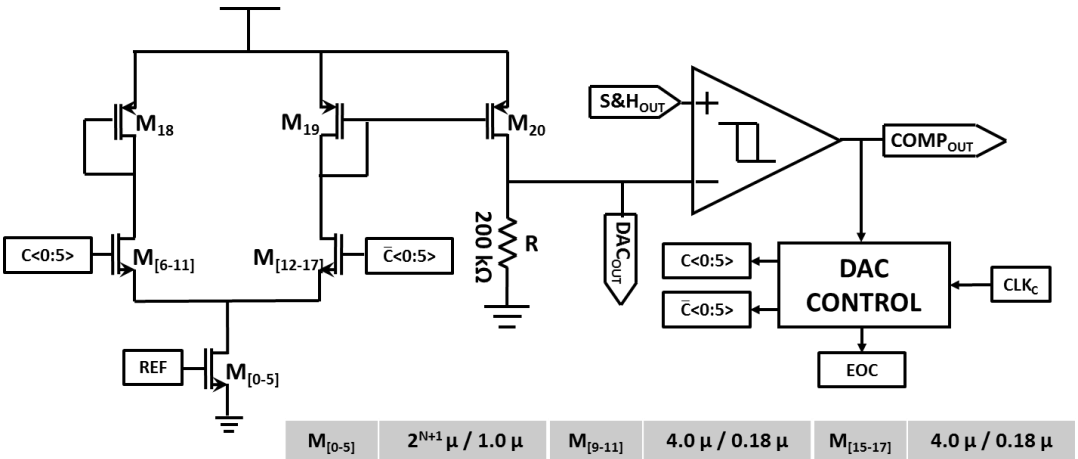


Figure 3.9. Transient simulation of the sample & hold circuit

3.2.2.2. Digital to Analog Converter and DAC Control Block

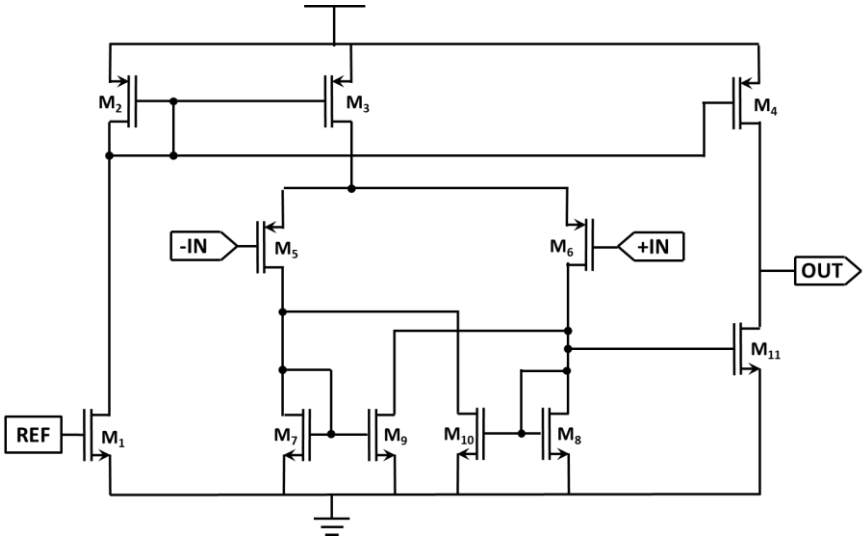
Analog to digital converter is used to determine the pulse width of the stimulation current. Schematic of the designed DAC is given in Figure 3.10. The ADC converts the logarithmic compressed voltage to the digital output. The reference voltage of the ADC is generated by current DAC and on-chip poly resistor. The refence and input logarithmic voltages are compared with hysteresis comparator. The ADC works with 1.8 V supply voltage for minimizing the power consumption.



$M_{[0-5]}$	2^{N+1} µ / 1.0 µ	$M_{[9-11]}$	4.0 µ / 0.18 µ	$M_{[15-17]}$	4.0 µ / 0.18 µ
$M_{[6-8]}$	2.0 µ / 0.18 µ	$M_{[12-14]}$	2.0 µ / 0.18 µ	$M_{[18-20]}$	4 µ / 1.0 µ

Figure 3.10. Schematic of the DAC and DAC control block

The hysteresis comparator is used for eliminating false outputs. The schematic of the comparator is given in Figure 3.11. The $M_{[1-4]}$ transistors are used for biasing, $M_{[7-10]}$ create hysteresis and M_{11} transistor is added as a common source for gain enhancement. Since the input values of the comparator are close to the ground, the input pair is chosen as PMOS.



M_1	6.0 µ / 1.2 µ
M_2	2.4 µ / 0.6 µ
M_3	14.4 µ / 0.6 µ
M_4	2.4 µ / 0.6 µ
M_5	12.0 µ / 0.6 µ
M_6	12.0 µ / 0.6 µ
M_7	5.0 µ / 0.6 µ
M_8	5.0 µ / 0.6 µ
M_9	6.0 µ / 0.6 µ
M_{10}	6.0 µ / 0.6 µ
M_{11}	11.0 µ / 0.6 µ

Figure 3.11. Schematic of the hysteresis comparator

The comparator is tested with DC sweep to observe hysteresis loop in Figure 3.12. The input is swept with 200 mV common input. The hysteresis of the system is around 10 mV which is less than 2 LSB.

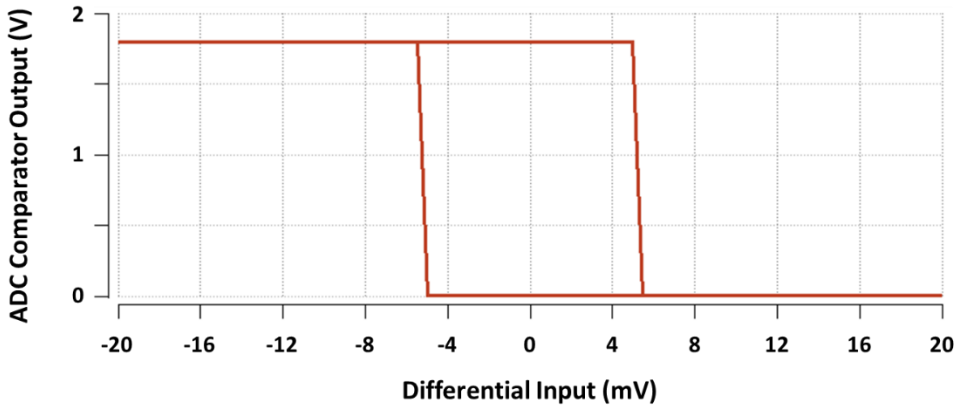


*Figure 3.12.*Comparator DC characteristic

The control block of the ADC is constructed from two 6-bit counters, a 6-bit digital comparator and a S-R Latch. The counter ‘A’ is the main counter, controls the DAC bits and is enabled with comparator output. The counting operation is controlled by ‘CLK_C’ which is the fastest clock of the system and represents the ADC clock. When the comparator output goes to high, the counter ‘A’ stops the counting operation and comparator output is latched, then ‘C/D’ signal goes to high. The ‘C/D’ signal controls the charge and discharge cycles and enables the counter ‘B’. 6-bit comparator compares the counter ‘B’ output with counter A output. When the outputs are equal, end of conversion (EOC) signal goes to high. ADC_{RESET} signal is generated every 125 µs and ADC operation is started with this signal for every channel.

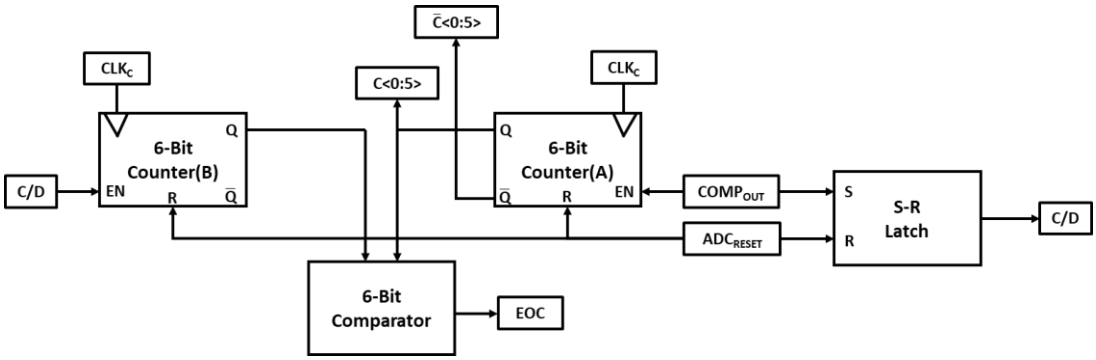


Figure 3.13. Logic diagram of the DAC control

The current DAC is constructed with differential switches (M [6-17]) (Figure 3.14) to eliminate mismatches and charge injection. The switch sizes are chosen as minimum to decrease charge injections and increase operating frequency. DAC is constructed with 6 bits and controlled by 1 MHz clock signal which is generated by ‘DAC Control’ block. The reference voltage output with respect to DAC bits is given in Figure 3.14. The reference voltage is set to the maximum output of the transconductance amplifier voltage. The LSB of the DAC is 6 mV and the maximum output voltage is 380 mV. Also, the INL and DNL errors are calculated from DAC characteristic and given in Figure 3.15. The errors are plotted as proportional to LSB while, the maximum INL error is 0.32 LSB and the maximum DNL error is 0.5 LSB. The effect of the differential switches and low size switches can be seen when the results are compared

with the previous design. Using these differential switches results in decrease in error rates.

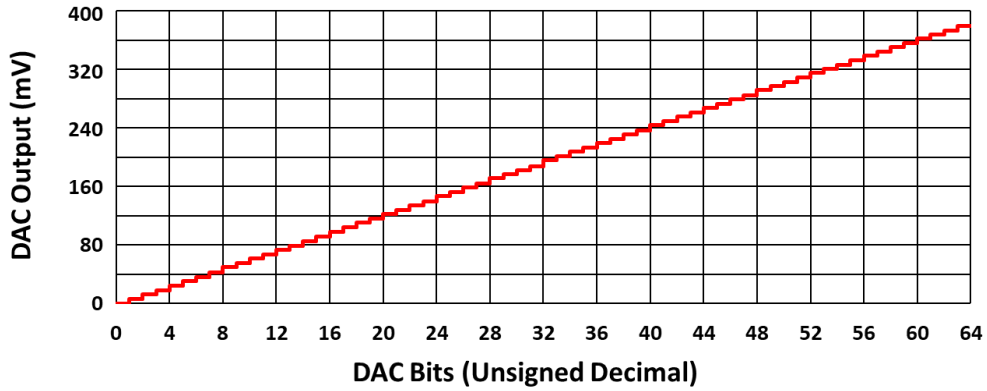


Figure 3.14. ADC reference voltage output with 200 kΩ load

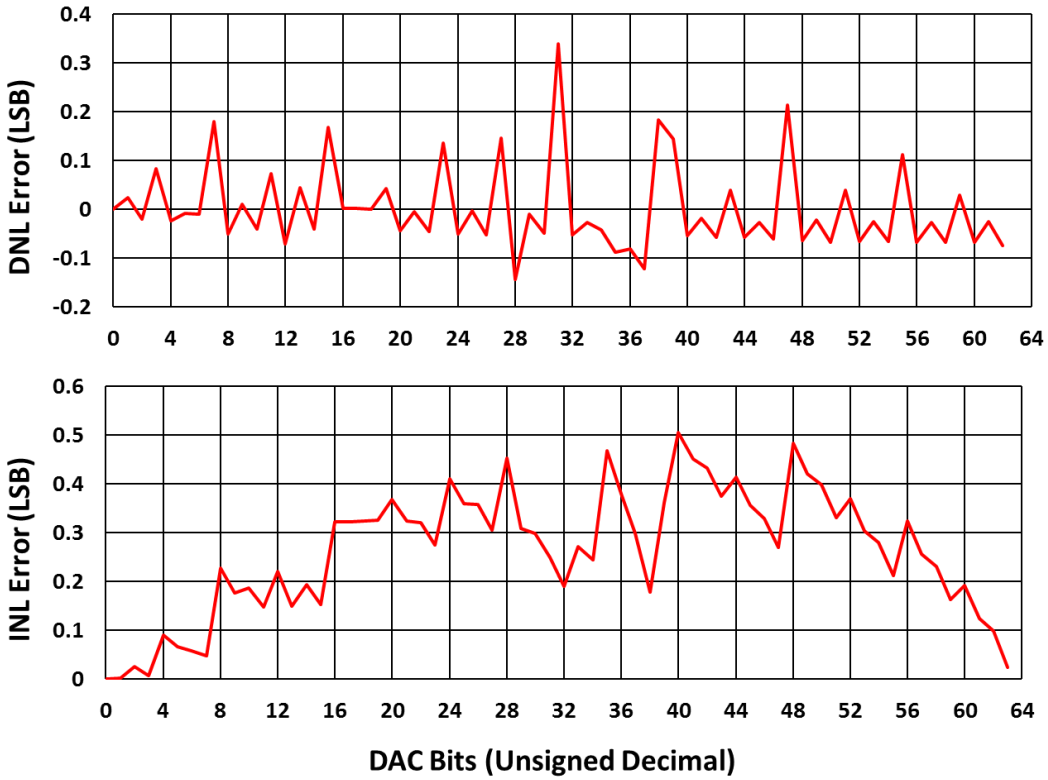


Figure 3.15. INL and DNL errors of the designed DAC

3.2.3. Control Block

The logic diagram of the control block is given in Figure 3.16. The system starts with CLK_L (Low Frequency Clock) signal edges. Then, 8-bit shift register the channel information is generated. The 'C/D', 'EOC' and channel signals are processed with combinational logic and it generates stimulator switch conditions. The channel number selects the electrode number. Anodic and cathodic phases of the selected electrodes are chosen by 'C/D' signal, and stimulation operation ends with 'EOC' signal. CLK_H (Channel Clock) signal controls the shift registers and maximum stimulation time. ADC_{RESET} is generated from transition edges of the CLK_H signal and starts to ADC bits. While, the CLK_H is generated form CLK_C signal by frequency dividers (7-bit counter), CLK_L is generated from CLK_H with 3 bit frequency divider. All digital blocks are connected to the 1.8 V supply and designed with minimum sizes to minimize the power consumption.

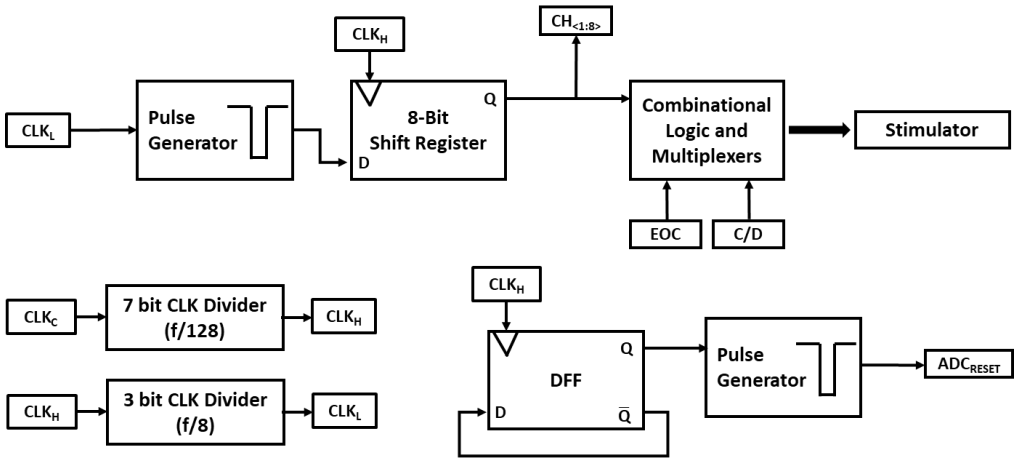
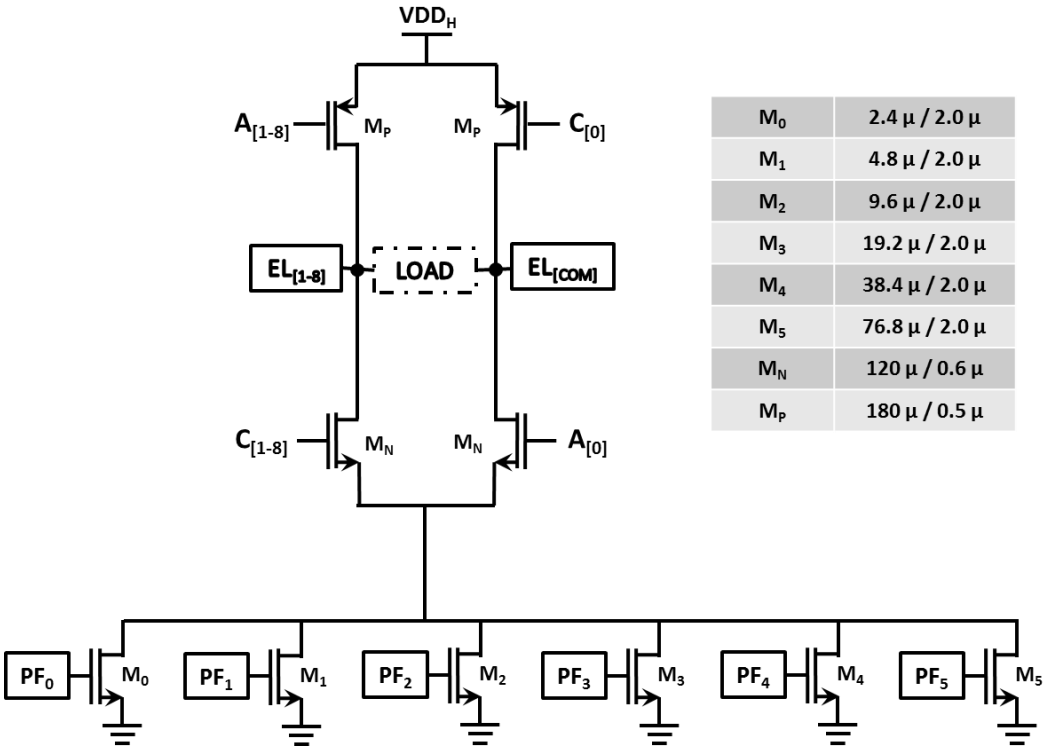


Figure 3.16. Logic diagram of the control block

3.2.4. Stimulator Circuit

The single supply constant current stimulator circuit (Figure 3.17) is used for generating pulse width modulated output and charge balance currents. The circuit consists of 9 branches and 6-bits current DAC. The 8 distinct electrode and 1 common

electrode are used for the stimulation. The stimulation is done in two phases. In the anodic phase, the current flows from electrode to common and enabled by $A_{[0-8]}$ switches. In the cathodic phase, the current direction is reversed and controlled by $C_{[1-8]}$ switches .The current DAC is controlled with patient fitting bits and controls the amplitude of the currents. Also, the DAC is arranged with single cascoded stage for low headroom voltage. The gate voltages of $M_{[0-5]}$ are connected to the digital bits for the current adjustment.



M_0	2.4 µ / 2.0 µ
M_1	4.8 µ / 2.0 µ
M_2	9.6 µ / 2.0 µ
M_3	19.2 µ / 2.0 µ
M_4	38.4 µ / 2.0 µ
M_5	76.8 µ / 2.0 µ
M_N	120 µ / 0.6 µ
M_P	180 µ / 0.5 µ

Figure 3.17. Stimulator circuit and patient fitting DAC schmeatics

The stimulation current amplitude characteristic is given in Figure 3.18. The circuits are tested in the transient mode with 6 V voltage supply and low load condition. The stimulation current and charge balance current can be calibrated according to the patient from 0 to 2.25 mA. The INL and DNL errors are smaller than 1 LSB which is

36 µA due to channel length modulation. The output drifts from its trend-line slightly. However, the effect of the small drifts is insignificant for the patient fitting.

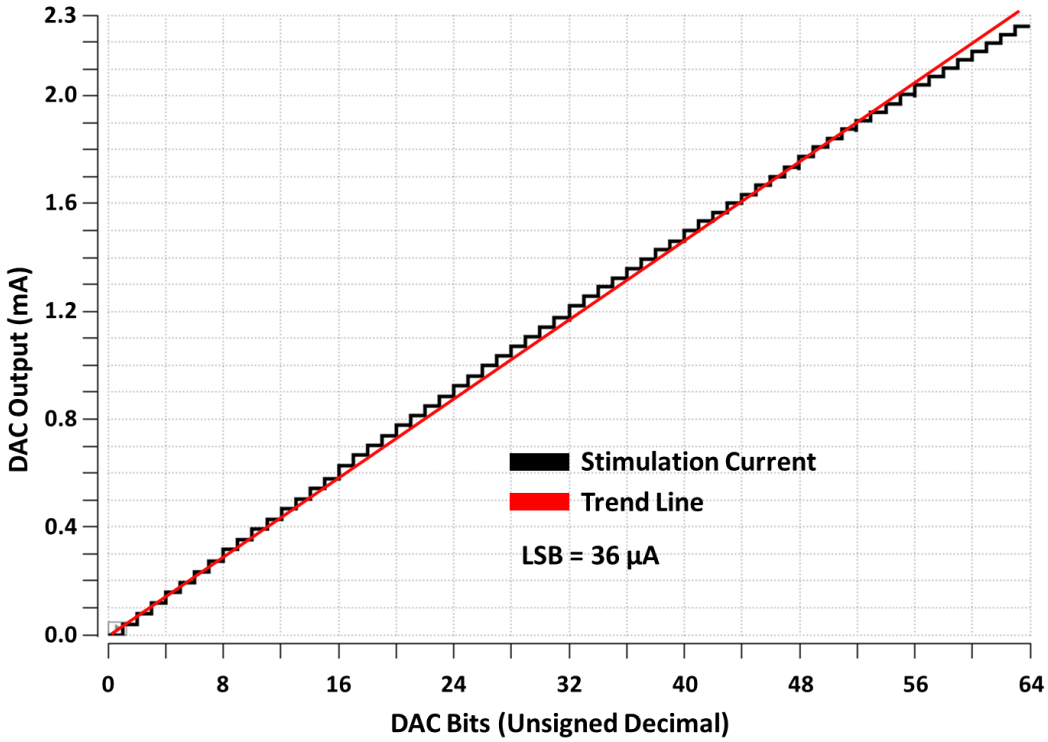


Figure 3.18. Patient fitting DAC characteristic

3.3. Charge Balance Circuit Design and Description

The charge balance circuit block diagram can be seen from Figure 3.19. After the stimulation, if there is time, CB_{EN} signal is generated and the switches (SW_{EL} and SW_{COM}) are shorted. The window comparators compare the electrode voltages and decide for charge balance operation. If one of the electrode voltages is higher than the other voltage with an offset, the charge balance current is generated. The charge balance currents are short pulses whose pulse widths and amplitudes are predetermined. After one short pulse, the charge balance circuit operates again until

the charge is neutralized. The charge balance circuit uses two supply voltages and clocked gates to minimize power consumption. While the high supply voltage is 6 V for comparators and switches, low supply voltage is 1.8 V for digital blocks. At the end of the comparators, digital level shifters are added for the supply change.

The control block of the charge balance system consists of a combinational logic and multiplexer same as the main control block. The charge balance circuit starts to operate with EOC signal. The operating switches are chosen by channel information ($CH_{<1:8>}$ signals). When the CLK_{CB} signal is low, the comparators and switches are operated and control the unbalanced charged. When clock signal is high, the charge balance current is generated on the stimulator and balancing operation is performed. The same stimulator is used for the charge balance current and the current amplitude determines PF bits. The PF bits can be connected to the EOC signal for different CB current amplitude.

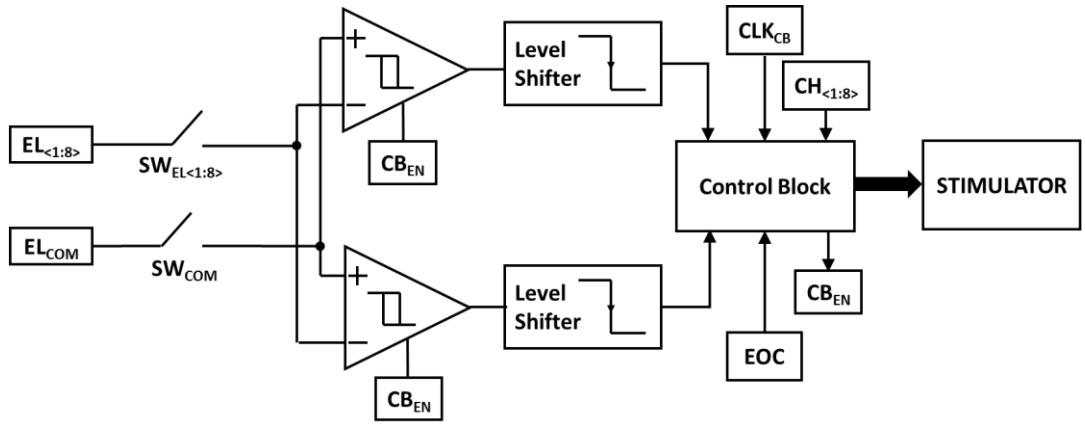
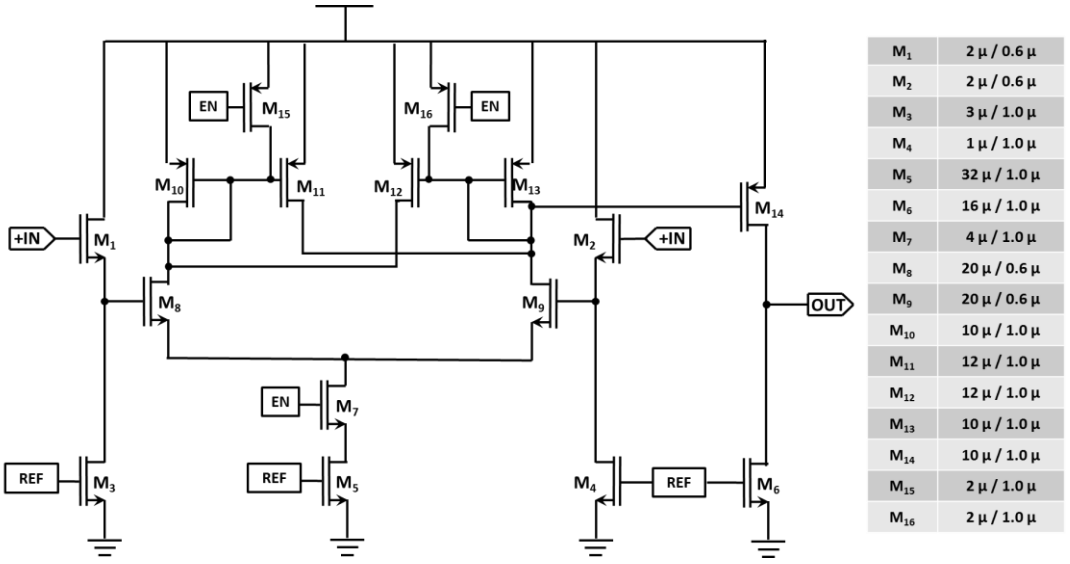


Figure 3.19. Charge balance circuit block diagram

3.3.1. Window Comparator

The window comparators (Figure 3.20) are used for the detection of the unbalanced charges. The comparators are designed with low power consumption with hysteresis. The low voltage design is required for the system implantation. The hysteresis structure is added to eliminate glitches. Enable signal is also added to decrease the

power consumption when charge balance circuit is not active. The analog level shifter is used for the window of comparator and $M_{[1-4]}$ transistors are used as a level shifter. Input of the amplifiers are connected to the common drain structures and DC level of the input is decreased. The decrease rate is determined by the reference current which is generated by $M_{[3-4]}$ and these currents are different for windowing. The DC level shift is also used to extend the input common mode range. As a second stage $M_{6\&14}$ is added in common source structure to increase driving capacity and gain.



M_1	2 µ / 0.6 µ
M_2	2 µ / 0.6 µ
M_3	3 µ / 1.0 µ
M_4	1 µ / 1.0 µ
M_5	32 µ / 1.0 µ
M_6	16 µ / 1.0 µ
M_7	4 µ / 1.0 µ
M_8	20 µ / 0.6 µ
M_9	20 µ / 0.6 µ
M_{10}	10 µ / 1.0 µ
M_{11}	12 µ / 1.0 µ
M_{12}	12 µ / 1.0 µ
M_{13}	10 µ / 1.0 µ
M_{14}	10 µ / 1.0 µ
M_{15}	2 µ / 1.0 µ
M_{16}	2 µ / 1.0 µ

Figure 3.20. Charge balance window comparator schematic

The window comparator is simulated with hysteresis DC analysis in Figure 3.21. In the graph, input voltage difference is swept over 5 V common input for two cross connected comparators. The window is arranged as 60 mV and hysteresis is set to 20 mV. With that configuration, the charge balance circuit limits the absolute electrode difference to 60 mV. The window voltage can be increased or decreased according to the electrode capacitance by adjusting reference voltage of the comparators.

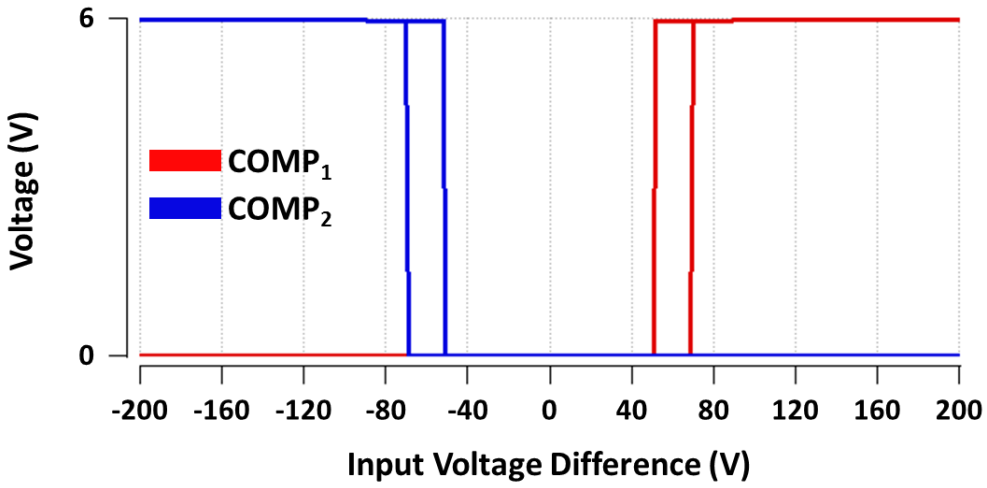


Figure 3.21. DC analysis of the window comparators

3.4. Voltage Reference Circuit

FICI system is an implantable system and requires voltage references for analog blocks and charge balance circuit. The voltage reference circuit (Figure 3.22) consists of 3 depletion, 2 low threshold and 1 normal NMOS. It has a chain structure and uses low threshold regions to generate 3 different reference voltages [49]. The generated voltages are 750 mV, 1.25 V and 1.70 V (Figure 3.23). These voltages should not be affected from the supply voltage since the battery voltage decreases with time. The temperature dependence is not important for this circuit since it is placed in the human body where the temperature change will be restricted with few degrees.

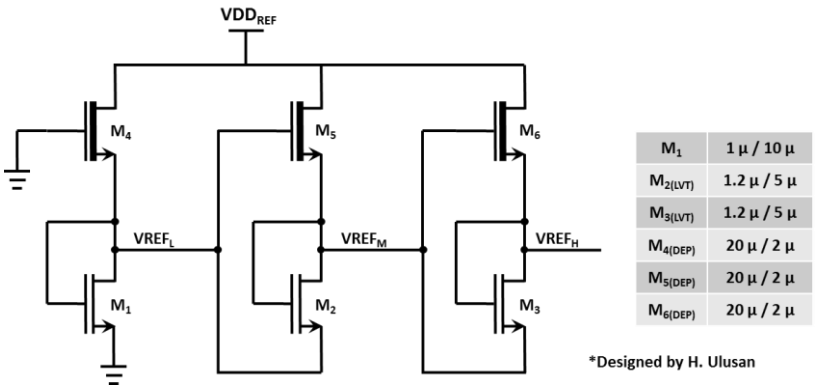


Figure 3.22. Schematic of the voltage reference circuit

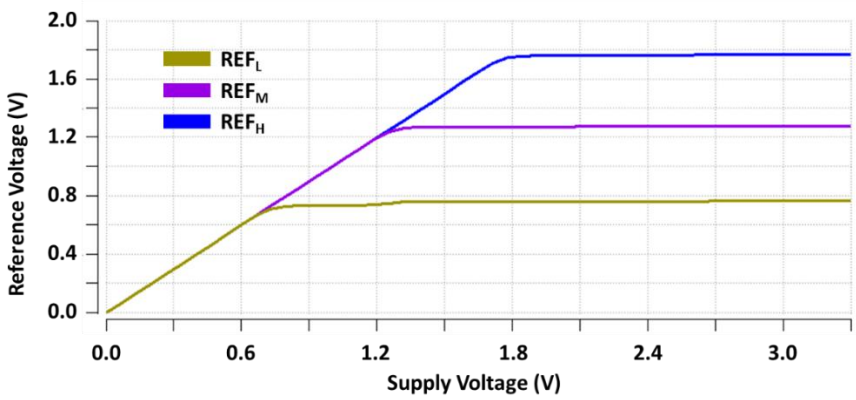


Figure 3.23. Voltage reference supply dependency

3.5. Clock Generator

Since the older version of the clock generator does not give stable output, the current starved structure is changed by adding inverters to the system (Figure 3.24). The rail to rail operation is required for glitch free operation, but the current starved stage outputs cannot operate rail to rail without inverters. Hence, the inverters are added at the output of the current starved stages. Such that, every stage output becomes rail to rail and stable output is achieved. Due to the corner variations, the oscillation frequency is adjustable by V_{IN} signal.

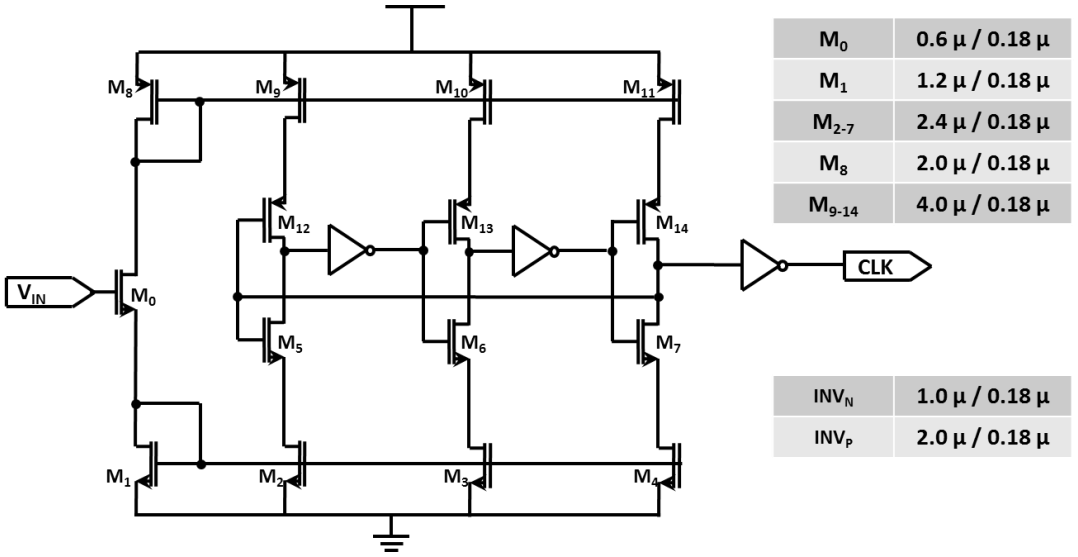


Figure 3.24. Schematic of the current starved voltage-controlled oscillator

The oscillator is calibrated to the 1 MHz for operation with adjusting the V_{IN} signal to the 750 mV. The transient simulation is given in Figure 3.25, and the generated waveform oscillates with 50% duty cycle with 1 MHz frequency. The generated signal frequency has small changes with less than 10 Hz and does not affect the operation.

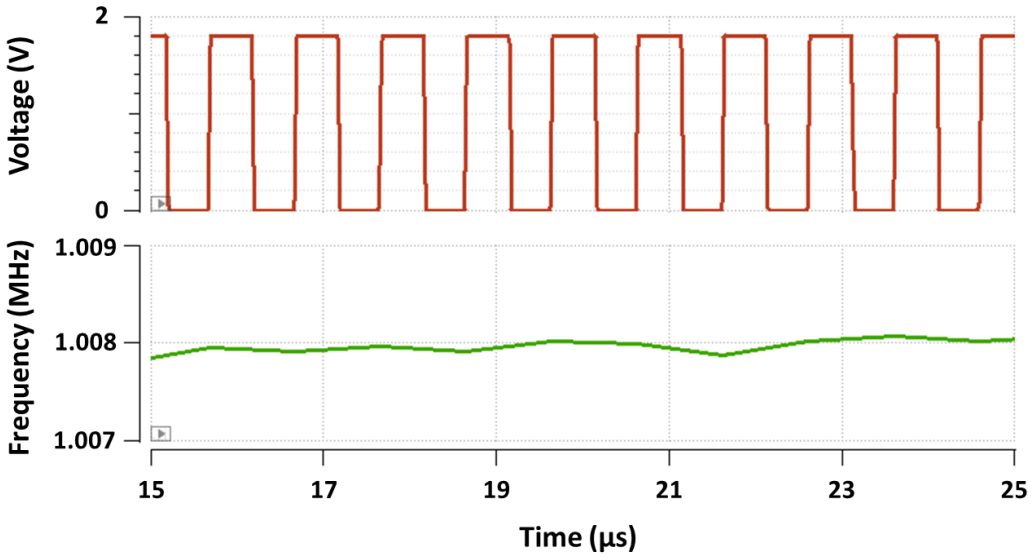


Figure 3.25. Oscillator circuit transient characteristic

3.6. DC-DC Converter

The charge pump circuit [50] is used for generating high DC voltage for stimulation and charge balance circuit as a DC-DC converter. For 5.4 V supply from the 1.8 V battery two-stage charge pump circuit is used. One stage charge pump circuit schematic is given in Figure 3.26. Circuit uses 12 switches and 6 on chip capacitors. The two-phase non-overlapped clock signal is used for driving switches. In one of the phases, node X or Y is charged to V_{N-1} (N: stage number) voltage and then boosted with the input voltage (V_0). When ϕ_1 is high, node X is equal to V_{N-1} and then ϕ_2 is high, it is boosted with the input voltage (VDD). The same operation is valid for node Y with reverse of the clocks. The switch gates (M_{N3-6} and M_{P3-6}) are driven by

bootstrap capacitors ($C_{3\text{-}6}$) which are used as a level shifter to supply high gate voltage for switching.

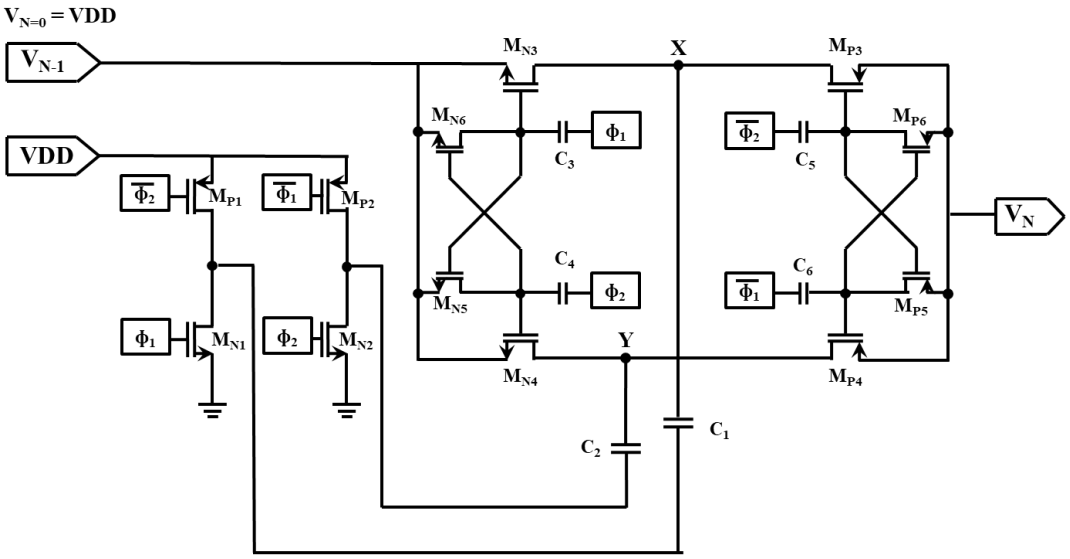


Figure 3.26. Schematic of one stage charge pump circuit. Designed by Mert Koç, METU BioMEMS Group

In Figure 3.27, transient analysis is performed with the stimulation. Two channel stimulation current is generated with 500 μA peak. The average voltage rating is 5.2 and minimum voltage is 4.86 for this operation. Loading characteristic of the DC-DC converter can be seen in Figure 3.28. The clock frequency of charge pump is adjusted to 5 MHz. The output current is changed, and output voltage is observed. Due to output resistance of the system, the output voltage is decreased with increasing current. However, the FICI system does not require constant current from the high voltage supply. The average current of the system is maximum 500 μA and the efficiency of the system is around 80% for this current range.

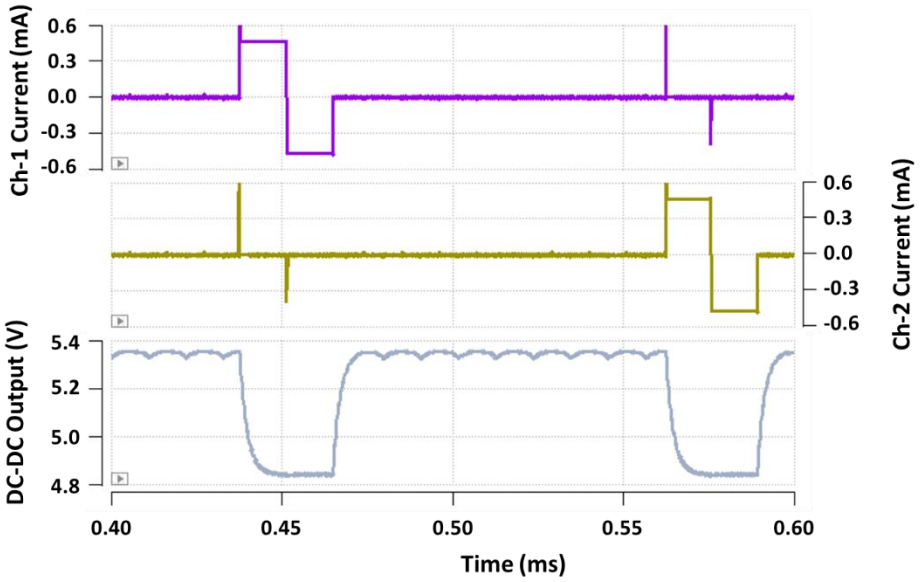


Figure 3.27. Transient analysis of the charge pump circuit

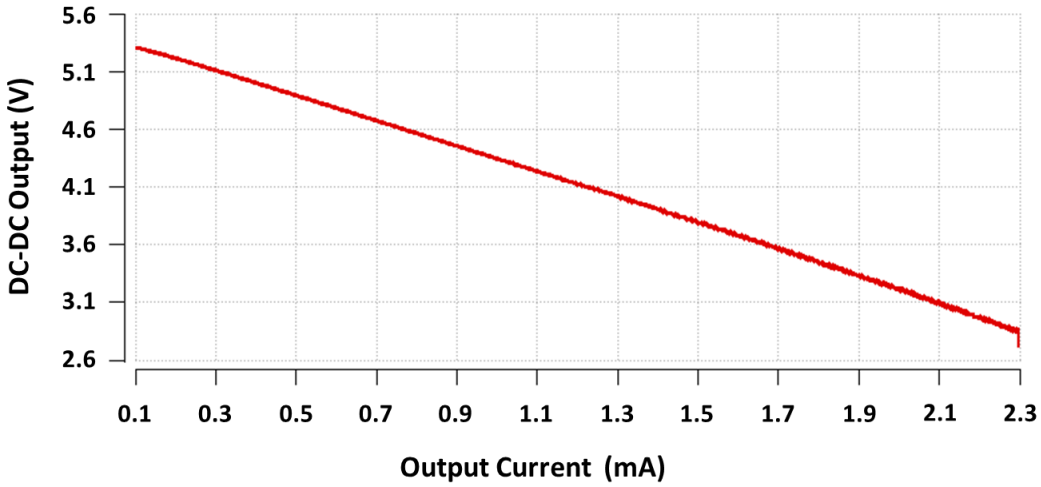


Figure 3.28. DC-DC load characteristic

3.7. Simulation of the Overall Circuit

The extraction of the circuit layout (Figure 3.29) is used for the simulations. The layout of the circuit consists of 8 main blocks and tests circuits. The total area of the design is 2.5 mm x 2.5 mm with 2.44 mm^2 active area (without test circuits and PADs). DC-DC converter block occupies the most of the area due to the on-chip capacitors.

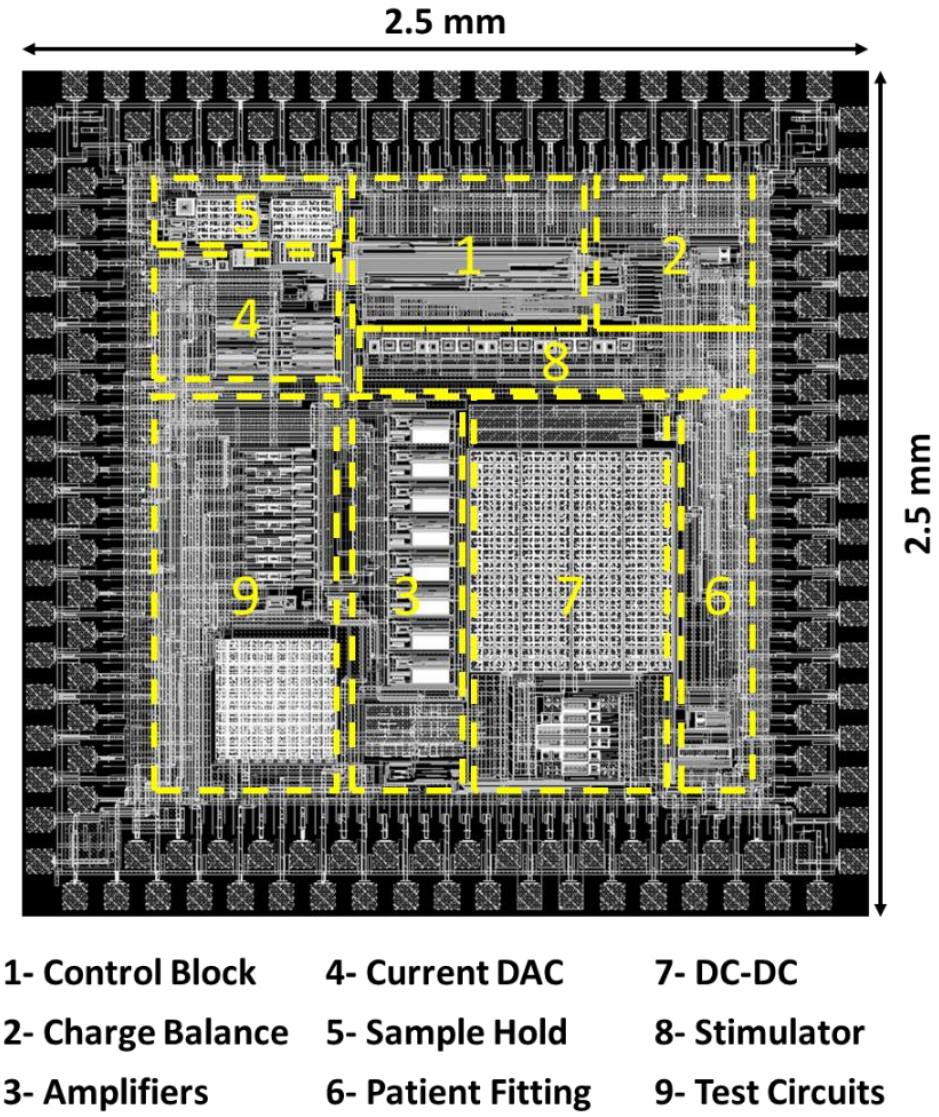


Figure 3.29. Layout of the designed FICI system

The overall simulation of the circuit is given in Figure 3.30. In the simulation, the electrode capacitances are initially charged to observe the effect of the charge balance circuit. The channel 3 and 4 capacitors are charged with positive voltages and the channel 6 capacitor is charged with negative voltage. The electrode capacitors are chosen as 100 nF [44] and charge balance current is set to stimulation current peak due to high capacitance. Every input voltage is selected with different frequency and amplitude. The circuit works with internal clock generator and DC-DC converter, and

circuit neutralizes the charge at the electrode by limiting the electrode voltage difference to 60 mV and stimulates the electrode with pulse width modulated biphasic currents. The spikes are occurring due to mismatch between switch timings at stimulator however, the amount of injected charge is not affected from these spikes and also stimulation safety controls by charge balance circuit.

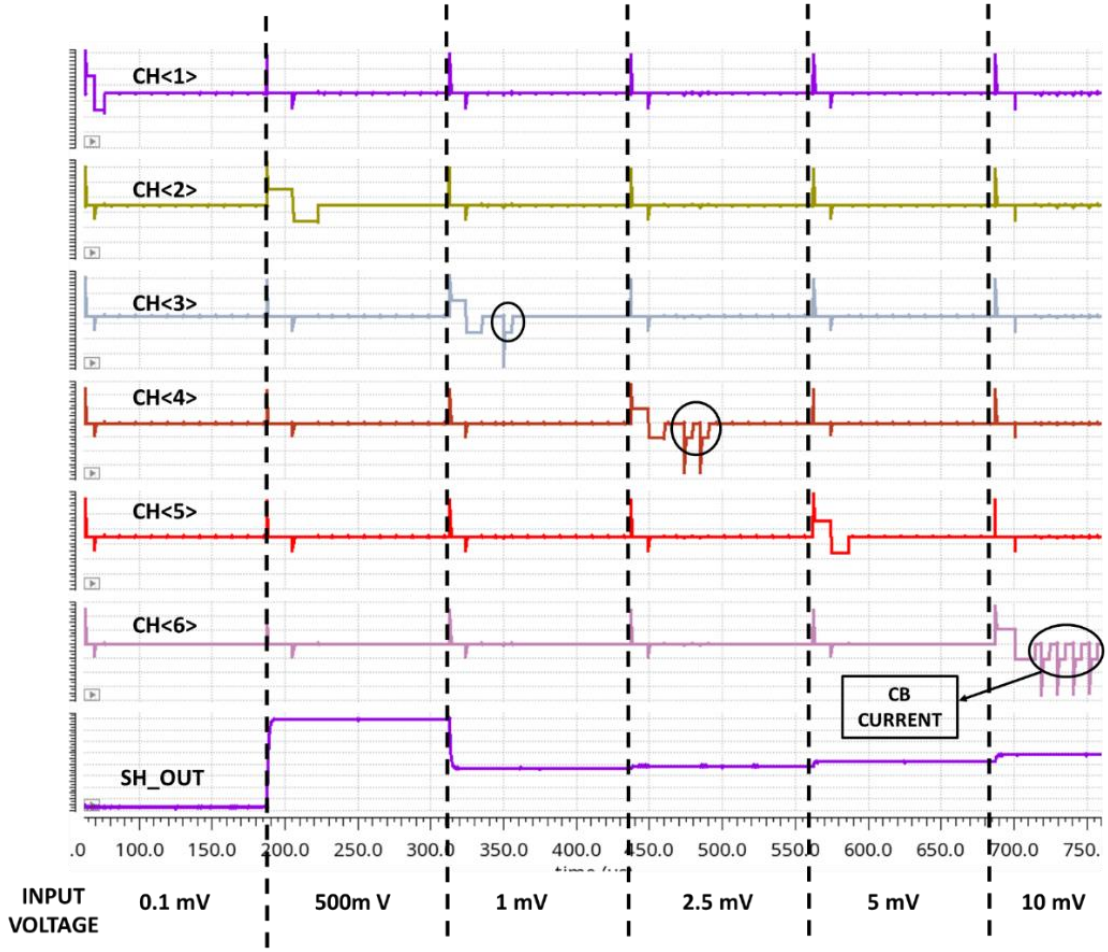


Figure 3.30. Simulation of the overall circuit

3.8. Experimental Test Results

The experimental tests are made by fabricated chip which has a CPGA 144 package and micrograph is given in Figure 3.31. Electrical and sound tests of the chip is

performed with designed PCB (Figure 3.32). The electrical electrode model is used for the test which is series 3 kΩ resistor and 50 nF capacitor.

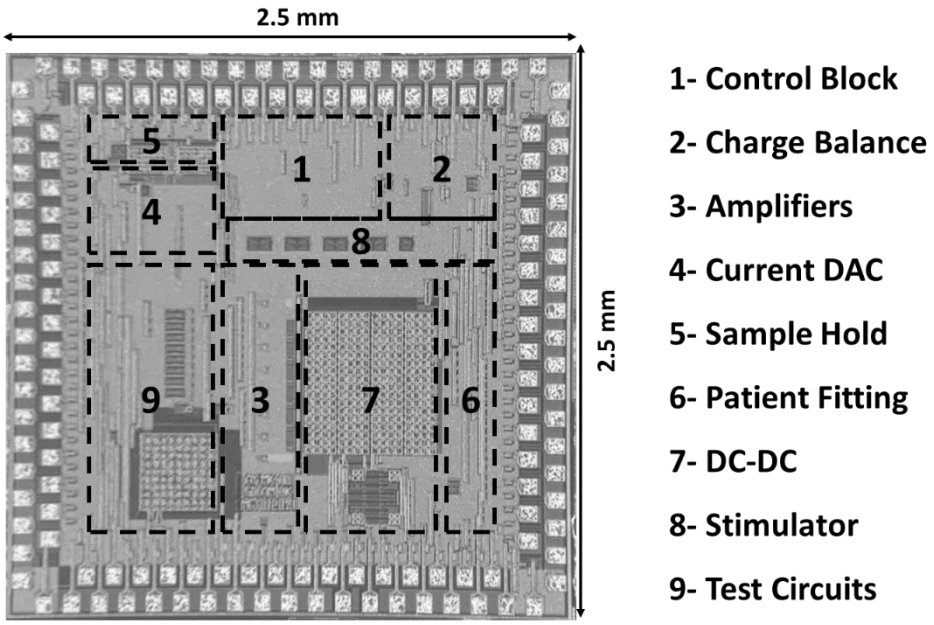


Figure 3.31. Charge balanced FICI system chip micrograph

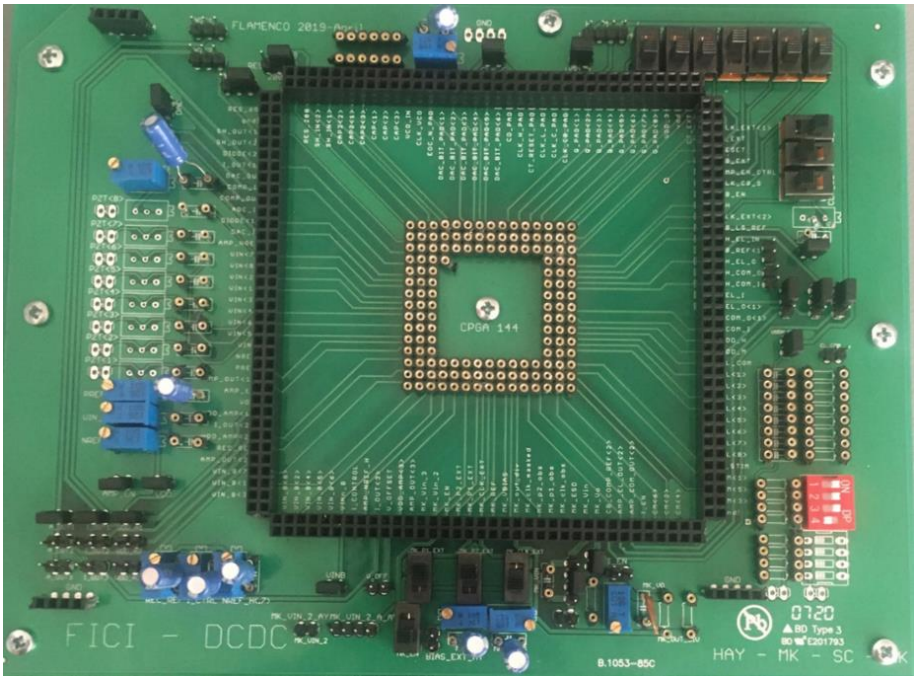


Figure 3.32. Charged balanced FICI system test PCB

3.8.1. Electrical Tests

Electrical tests are performed with signal generator input, series resistor and capacitor load as an electrode. The aim of these measurements is to see characteristic of the main blocks of the circuits.

3.8.1.1. Front-End Analog Blocks

To test analog blocks a low frequency (100 Hz) signal is generated and given to the system as an input. The low frequency is chosen to observe rectification and amplification operation. If the input signal frequency is higher the output will be a DC signal. The amplifier and rectifier circuits work properly, and output current is connected to an on-chip diode. The rectified output voltage is compressed between 0.1 V and 0.6 V. The sample hold circuit also operates properly with 125 µs pulse durations. However, the sample hold output differs from one branch to other branch due to capacitance mismatches. Nevertheless, difference is not higher than 5 mV which is smaller than 1 LSB of ADC, and it is a tolerable noise.

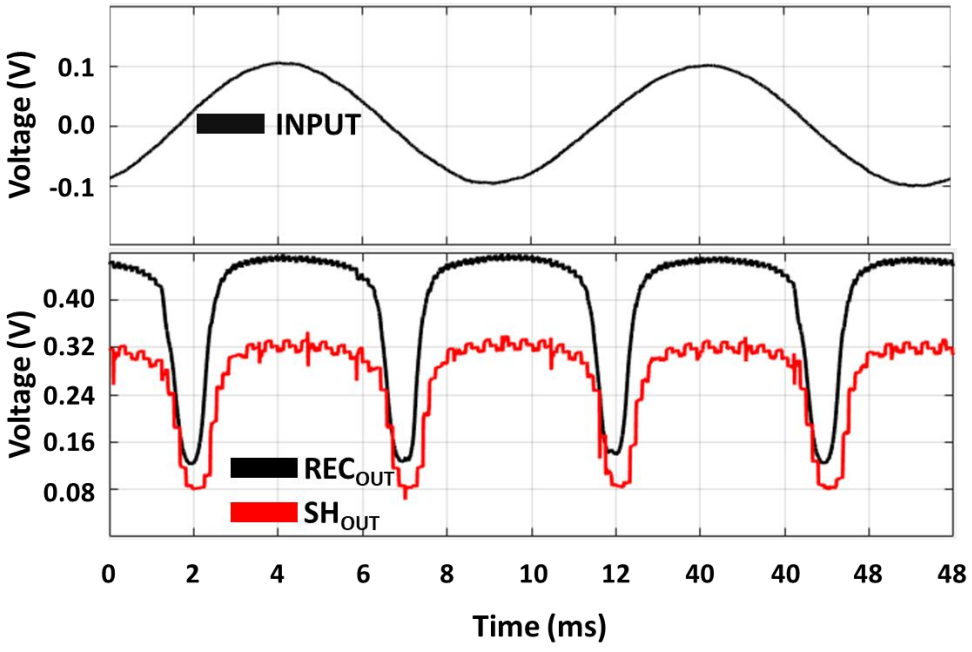


Figure 3.33. Transient analysis of the amplifier, rectifier and sample hold circuits

3.8.1.2. Analog to Digital Converter

To observe DAC characteristic a transient analysis is performed with maximum input voltage and resistor voltage is observed (Figure 3.34). The clock frequency is lowered to minimize the effect of the oscilloscope probe. The trend line is generated from the noisy experimental data by mean operation. From the trend line characteristic of the DAC, errors are calculated.

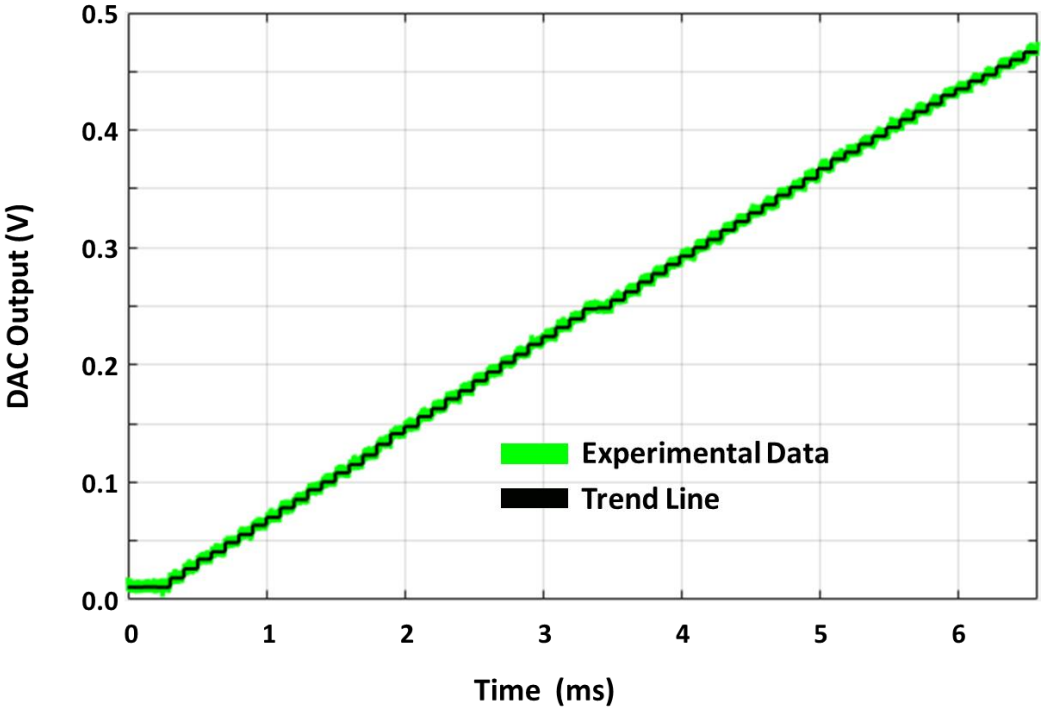


Figure 3.34. ADC transient characteristic.

The DNL and INL characteristics of the DAC are given in Figure 3.35. The error values are higher than the simulation results due to the external noise (line noise, probe loading, supply noise etc.) coming from the environment during the measurements.

However, the errors are less than 1 LSB which is 7.23 mV. These error rates can be tolerated with the system and ADC works properly.

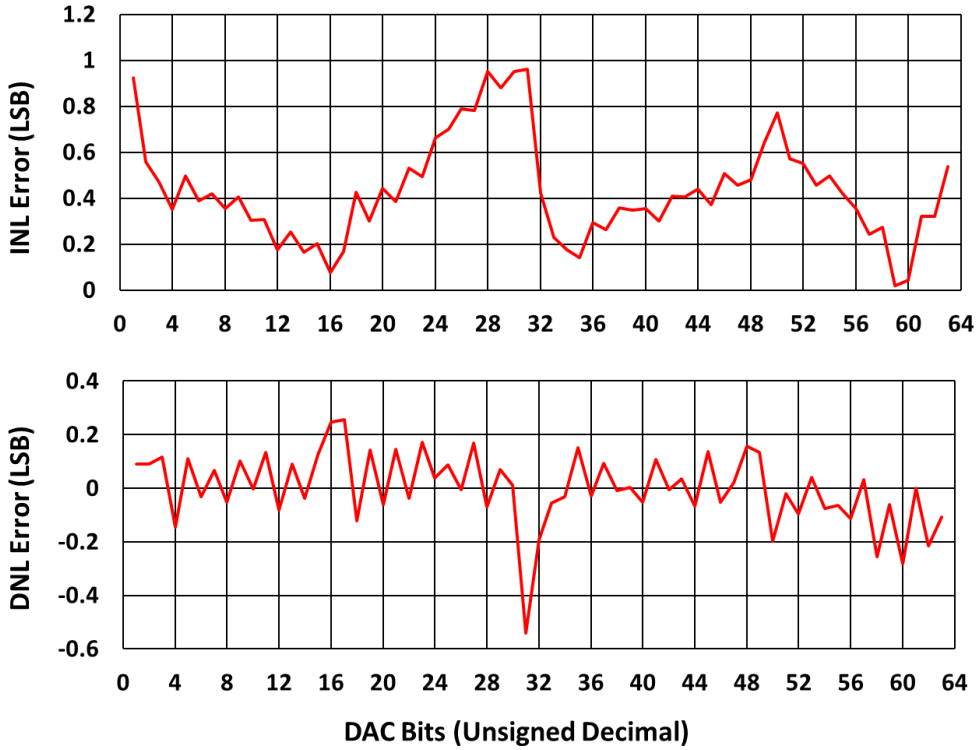


Figure 3.35. DNL & INL errors of the fabricated ADC

3.8.1.3. Charge Balance Circuit

The system is tested with constant input voltage to see charge balance current generation and its effect.

Figure 3.36 shows the stimulation currents with and without charge balance circuits. The red lines represent the safe voltage limits which is ±100 mV. When the charge balance circuit is enabled, the voltage difference is limited in the red region. However, without charge balance circuit the electrode voltage difference saturates at the 400 mV.

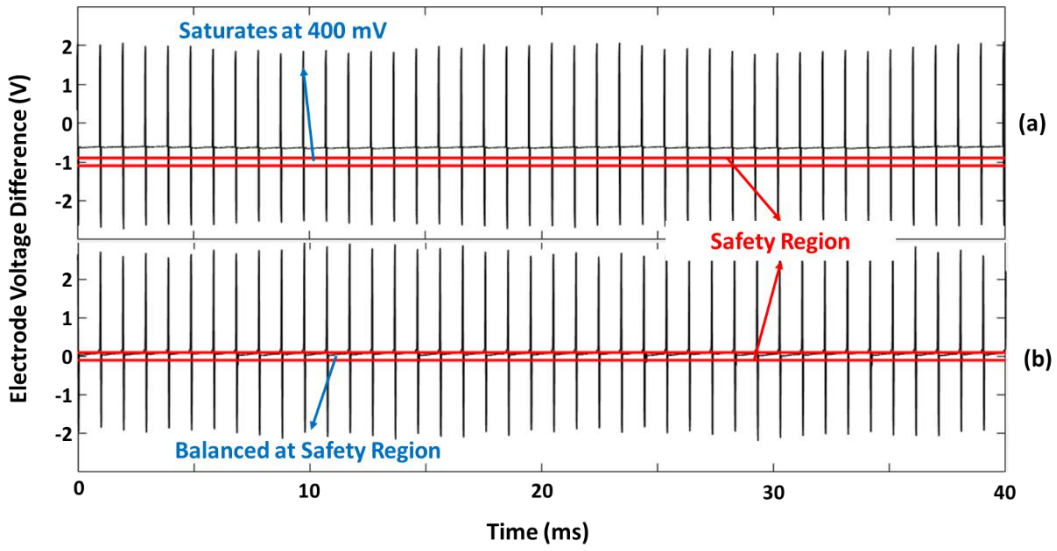


Figure 3.36. Stimulation without (a) and with (b) charge balance circuit

Figure 3.37 shows the closer view of the constant current stimulation electrode. When the electrode voltage difference becomes higher than 80 mV, the charge balance current is generated, and the voltage difference becomes zero.

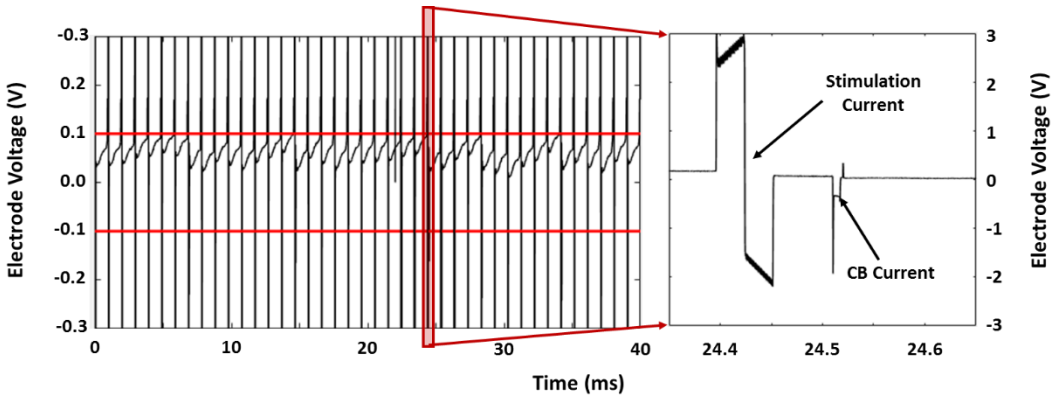


Figure 3.37. Closer view of the charge balanced stimulation

3.8.1.4. DC-DC Converter Circuit

The DC-DC converter is tested with one channel system to observe minimum voltage ratings (Figure 3.40). The input is chosen as a ramp input for observing pulse width

modulation effect. The amplitude of the biphasic current output is chosen as 520 µA. The system operates with a single 1.8 V supply and high voltage supply is generated by DC-DC converter. The output of DC-DC converter is 5.1 V without stimulation and 4.7 V with stimulation. In 4.7 V maximum tolerable impedance is 5 kΩ and 50 nF. To increase impedance limit, extra stage can be added to the DC-DC converter or the supply voltage can be increased up to 2 V.

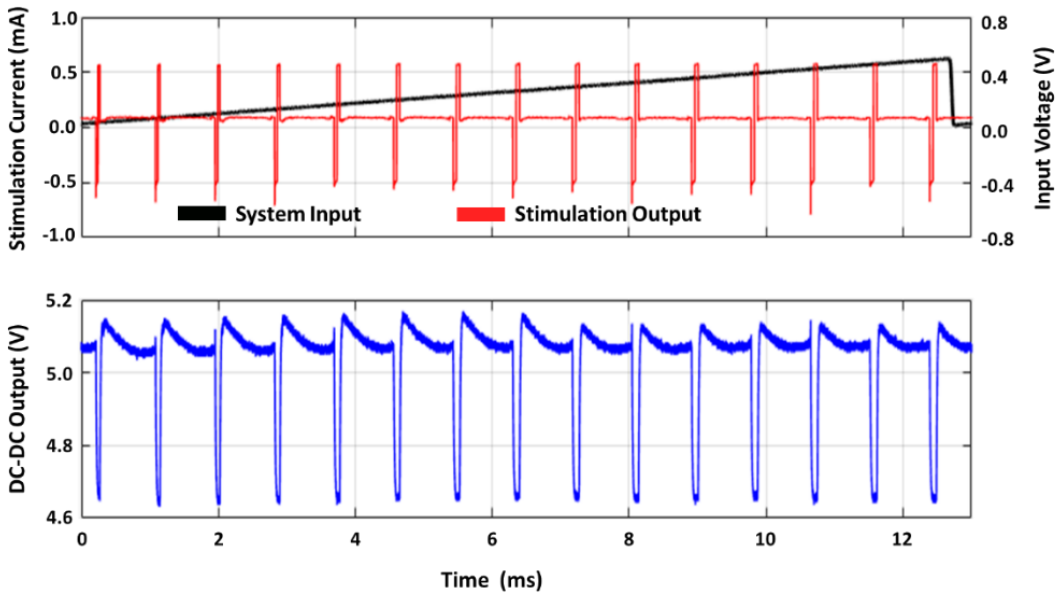


Figure 3.38. Transient analysis of the system with DC-DC converter

3.8.1.5. Oscillator and Voltage Reference Circuits

The oscillator circuit is designed for 1 MHz output. The output of the oscillator can be seen from Figure 3.39. The duty cycle is not 50% due to the mismatch of the oscillator branches coming from the process variations. However, the charge balance circuit compensates this error. The oscillator circuit performance is tested with complete system. ADC and control blocks are operating without any problem.

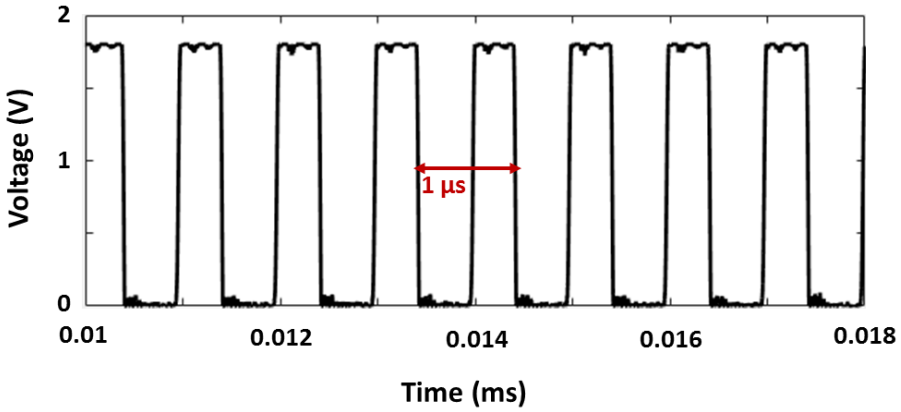


Figure 3.39. Oscillator circuit transient analysis

DC analysis results of the voltage reference circuit can be seen from Figure 3.40. The voltage supply is swept, and the reference output is observed. After the 1.5 V supply voltage, all reference voltages are constant, and the circuit can operate up to 5 V. The low reference for front end analog blocks and high references are used for biasing charge balance circuit analog blocks.

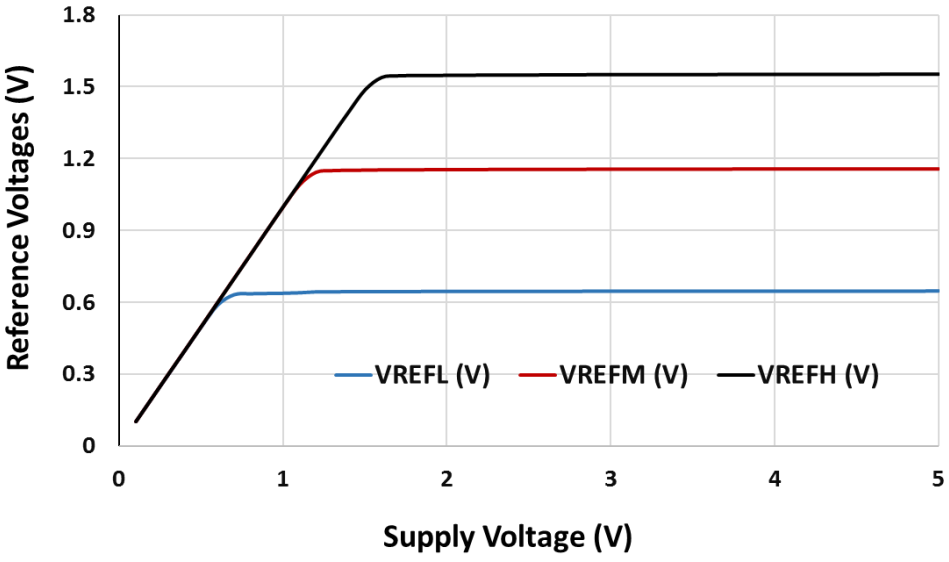


Figure 3.40. Voltage reference circuit output variation respect to supply voltage

3.8.1.6. Multi-Channel Operation

The system is tested with internal DC-DC converter, clock generator and reference circuits. The 8 channel test results are given in Figure 3.41. The output currents are plotted, and every channel current amplitude is set to 500 µA. All the inputs are shorted and ramp signal is given to every channel and stimulation frequency is set to 1 ms. The circuit can perform 8-channel operation according to the CIS strategy.

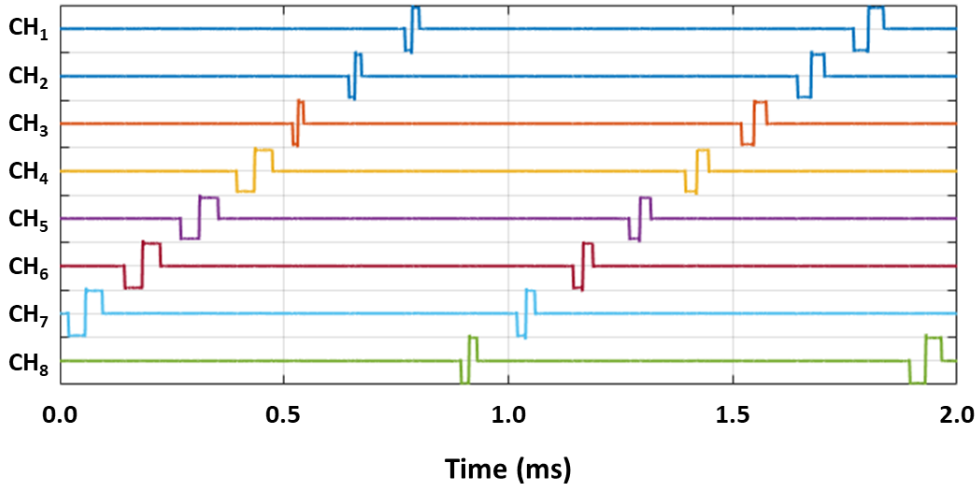


Figure 3.41. 8 channel FICI system output

3.8.1.7. Power Consumption Tests

Constant 60 dB input sound equivalent signal is used to calculate the daily speech power requirement. For the test, the 8 channel inputs are connected to single sinusoidal input signal with 1 kHz frequency and 1 mV peak voltage. Then the system supply current is observed for the power calaculation. Figure 3.42 shows the charge pump circuit output and single supply current. The DC-DC circuit generates 4.8V when stimulation occurs and 5.2 V at the charge balancing. The average power of the system is calculated as 695 µW which is consumed from a 1.8 V single battery and it is low enough for a long term fully implantable operation Table 3.1 summarizes the power consumption of the circuit blocks. The charge pump circuit creates high voltage supply

with 80% efficiency. The total implantable system consumes 695 µW from a 1.8 V single battery which is low enough for a long term fully implantable operation.

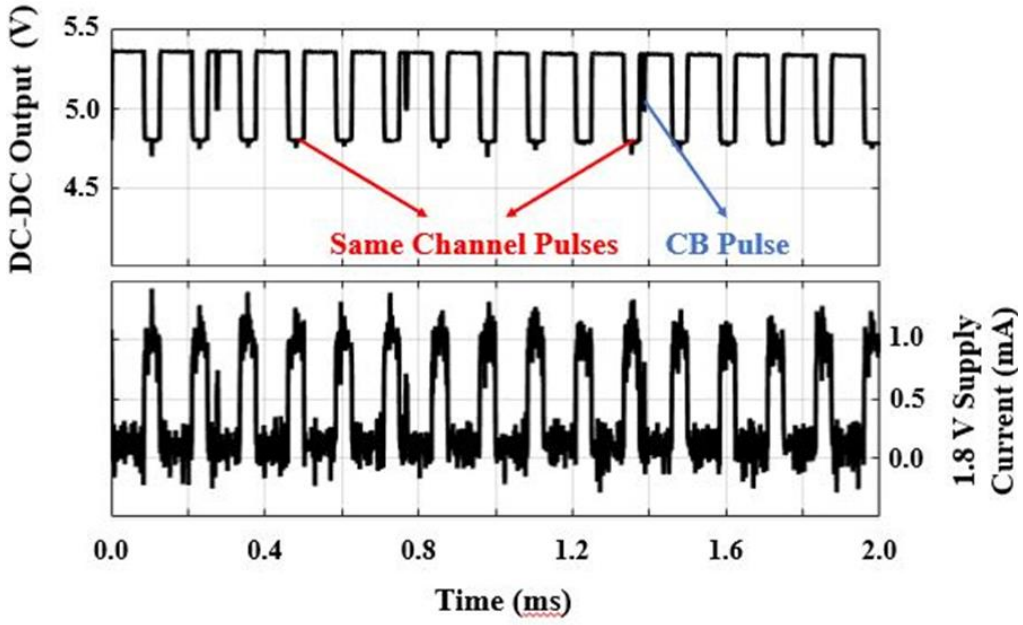


Figure 3.42. Power measurement result of the 8ch FICI system.

Table 3.1. *Power consumption of the interface Circuit*

Circuit Blocks	***Current (µA)***	***Supply Voltage (V)***	***Power (µW)***
Front-end Analog Blocks	2.0	1.8	3.60
ADC	3.6	1.8	6.48
Control Block	7.9	1.8	14.22
Oscillator & Reference	6.1	1.8	10.98
Stimulator	98.1	4.8	471.0
Charge Balance	6.1	5.2	31.72
Front End	19.6	1.8	35.28
Charge Pump (CP)	87.2	1.8	157.0
Total without CP	-	-	538.0
Total with CP	386.1	1.8	695.0

3.8.2. In Vitro Tests

3.8.2.1. Piezo-Electric Transducer

The piezo-electric transducer are designed and fabricated by Berat Yüksel (METU BioMEMS Group) and presented in [51]. The fabricated multi-channel piezoelectric acoustic transduce operates within the speech range (250- 5500 Hz). The transducer consists of eight different cantilevers with thin film PLD-PZT piezoelectric layers. The volume of the transducer is 5 mm x 5 mm x 0.6 mm and it can be easily implanted in middle ear cavity. The second channel characteristic is given in Figure 3.43. The output of the transducer is plotted respect to SPL. Second channel can generate output voltage up to 80 mV_{P-P} when it is excited with 100 dB SPL. At 100 dB SPL, the maximum output voltage is 140 mV_{P-P} and it is generated by the first channel when 316 Hz and 100 dB SPL sound signal excitation is applied.

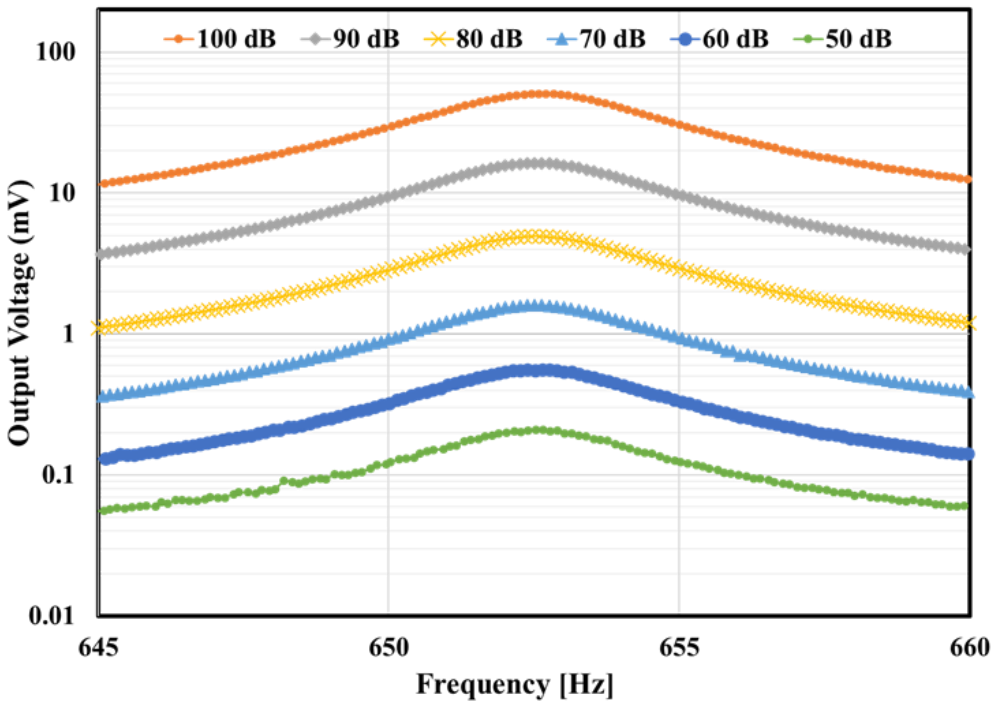


Figure 3.43. Second channel piezo-electric transducer characteristic designed by Berat Yüksel (METU BioMEMS Group)

3.8.2.2. In Vitro Test Setup

The in-vitro test setup can be seen from Figure 3.44 (block diagram is represented in Figure 3.45). The input is given from a headphone and recorded with prob-microphone to detect pressure levels. The 8 channel piezo electric transducer array [51] converts the sound signal into the electrical signals. These electrical signals are processed with FICI interface circuit and generate PWM modulated charge balanced output currents. The output currents stimulate the single channel cochlea electrode (produced by MED-EL) and electrode voltages are observed from oscilloscope.

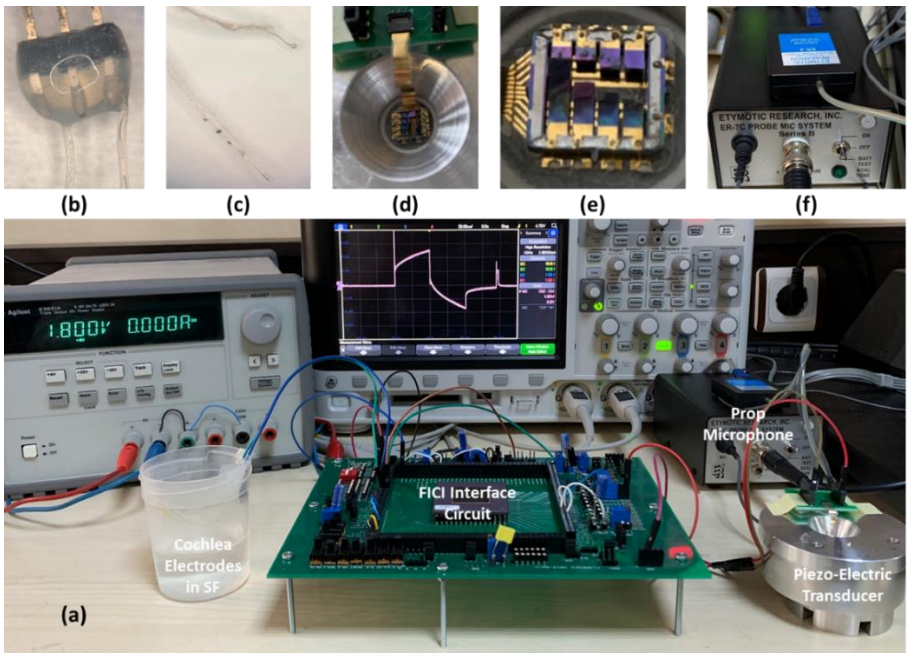


Figure 3.44. The *in-vitro* test setup (a), the cochlea electrode connections (b), the cochlea electrode array conductors (c), piezo electric transducer holder(d), 8 channels piezo electric transducer (e), the probe microphone and headphone (f)

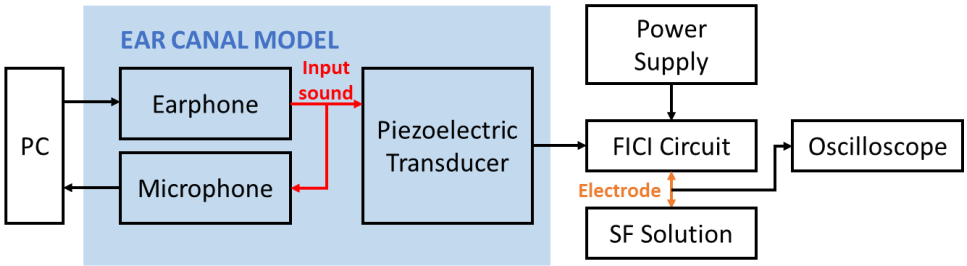


Figure 3.45. Block diagram of the *in-vitro* test setup

3.8.2.3. In Vitro Test Results

The system is tested with constant 70 dB sound level to observe the implemented system. Figure 3.46 shows the generated biphasic currents with and without charge balance circuit. The electrode voltage difference is limited with charge balance circuit between ±100 mV range. The stimulation occurs with 1 kHz frequency with 1 mA generated current output. For in-vitro tests the output capacitor is inserted at the output at the DC-DC converter for the regulation due to high stimulation current.

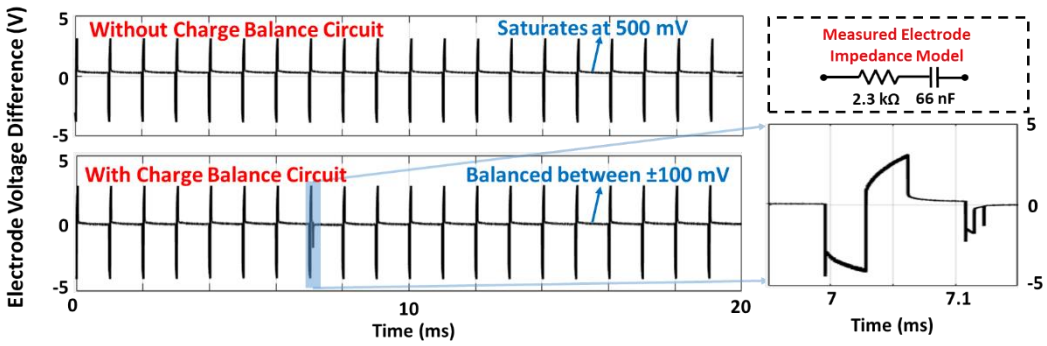


Figure 3.46. Charge balance circuit effect with constant 70 dB input sound

Figure 3.47 shows the single channel operation of the system by changing input voltage. The input of the system is 2.2 kHz sound data (5th Channel) with a changing pressure level. System generates biphasic current pulses whose peak value is 1 mA. The system can operate with minimum 50 dB input and generate current with 20 µs pulse width. The maximum pulse width is 62 µs and it is generated when the peak to peak value of the input is higher than 100 dB. The circuit can compress 50 dB input dynamic range to 10 dB electrical range for the stimulation. For the tests, an off-chip op-amp with 30 V/V gain is inserted at the input to detect lower SPL levels.

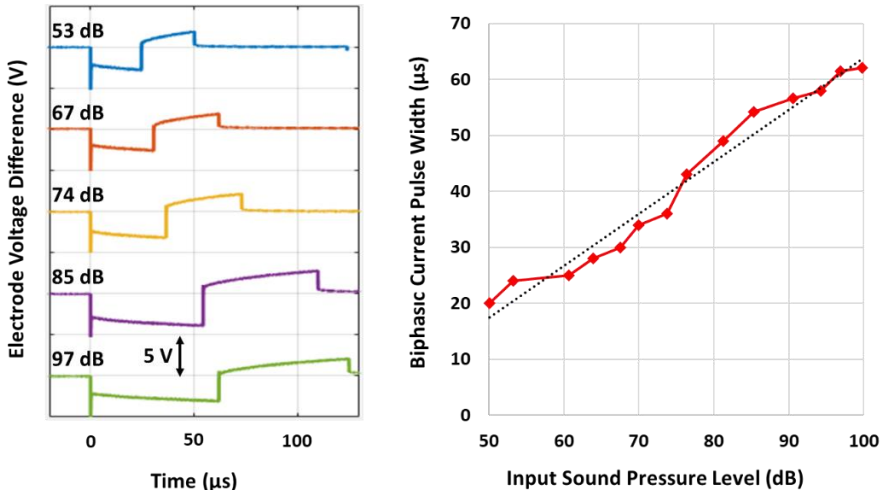


Figure 3.47. Single channel FICI system current outputs for different input SPL

3.9. Summary of the Chapter

In this chapter, design of the charge balanced pulse width modulated FICI interface circuit is presented. The circuit takes input from 8 distinct bandpass piezo-electric sensors and amplifies with trans-conductor amplifiers. The output currents of the clock gated 8 amplifiers are added, rectified and compressed by diode. The compressed diode voltage is digitalized with 6-bit ADC. Digital output determines the pulse width of the biphasic current. After the stimulation the charge balancing is achieved. The charge balance circuit monitors the electrode voltage and generates short charge balance current pulses if the difference is higher than threshold value. The electrodes stimulate according to the CIS strategy and maximum pulse width is 62 µs. System has a 50-dB input dynamical range and every channel stimulates with 1 kHz frequency. The system is tested with in vitro test environment and provides 34 nC/phase for 70 dB single tone input. The comparison with the state of the art FICI interface circuits is given in Table 3.2. The other FICI systems have lower power consumption; however, they do not have full implantable charge balance systems. They also require additional rectifiers and DC-DC converters for a single battery implantation. The proposed system consumes total 695 µW from a single battery and limits the electrode voltages by charge balance currents while stimulating 8 distinct channels with 50 dB dynamical range.

Table 3.2. *Comparison with the state of the art*

	[22]	[23]	[24]	[45]	[46]	[25]	***This Work***
Technology	*1.5 μm*	*1.5 μm*	*0.18 μm*	*0.18 μm*	*0.18 μm*	*0.18 μm*	*0.18 μm*
Electrode Number	*8-16*	*8-20*	*8*	*8*	*8*	*8*	*8*
Dynamic Range (dB)	77	60	60	40	45	60	50
Actieve Area (mm^2)	88.3	21	3.36	0.6(1)	0. 5	1.96	2.44
Patent Fitting	7-bit	5-bit	6-bit	7-bit	3-bit	7-bit	6-bit
Stimulation Method	AM	AM	AM	AM	PWM	AM	PWM
Front End Power (μW)	211	*126*	93	51.2	32	19.7	*36.3*
Total Power (μW)	-	2126(2)	572	691.2	513	471.7(3)	538(4) / 695(5)
Max. Stimulator Voltage Compliance	-	-	7 V	10 V	5 V	8 V	6 V
Charge Balance	-	-	B. Cap (8x220nF)	Electrode Shorting	-	Electrode Shorting	Pulse Injection
Supply Voltages (V)	2.8	3.8	0.6-1.5-1.8-3.3-7.0-9.0	1.8 -3.3-5.5	1.8 -3.0-5.0	1.8 -3.3-5.5	1.8

(1) Calculated from chip micrograph

(2) Stimulator is not designed and predicted by [23]

(3) Calculated from 5.5 V supply

(4) Calculated without DC-DC converter

(5) Calculated with DC-DC converter

CHAPTER 4

SYNCHRONOUS CHARGE BALANCE CIRCUIT FOR CCS

4.1. Motivation

In this chapter another charge balance circuit is designed for constant current stimulator circuits. This design can be used with AM and PWM FICI system. It is synchronous charge balance method which generates the charge balance current with the stimulation and neutralizes the unbalanced charge at the electrode. Synchronous charge balancing is required when stimulator systems do not have any time between the channels. The charge balanced circuit is activated before the stimulation and monitors the electrode voltage, then generates charge naturalized current at the stimulation cycles.

The charge balanced system should be suitable with any functional electrical stimulation (FES) device which uses constant current stimulator and consumes ultra-low power for implantation. The charge balance method requires an improvement on the stimulator circuit to operate.

4.2. Single Supply Constant Current Stimulator

Figure 4.1 shows the single supply CSS and load characteristics. Single supply CSS structure is more suitable than conventional CSS structure for implantable devices due to volume limitation. The single supply CSS uses four switches for three different cycles. These cycles are off, sink and source. In the off cycle, the S_C and S_A inputs are set to LOW and there is no current on the LOAD. In the sink cycle, S_C input is set to HIGH, S_A input is set to LOW and the electrode current flows through the common electrode (EL_COM). In the source cycle, inputs are inverted with respect to sink

cycle and electrode currents flow to common electrode. The stimulation current is generated by M_{CTRL} transistor and controlled by V_{CTRL} voltage. In charge balanced stimulation, the electrode currents must be equal at the sink and source cycles. Electrode voltage and charge must be zero after the stimulation. For constant current operation, M_{CTRL} transistor should be in the saturation region, the drain voltage should be greater than the gate voltage and electrode voltage range varies from V_{CTRL} to VDD (Supply Voltage).

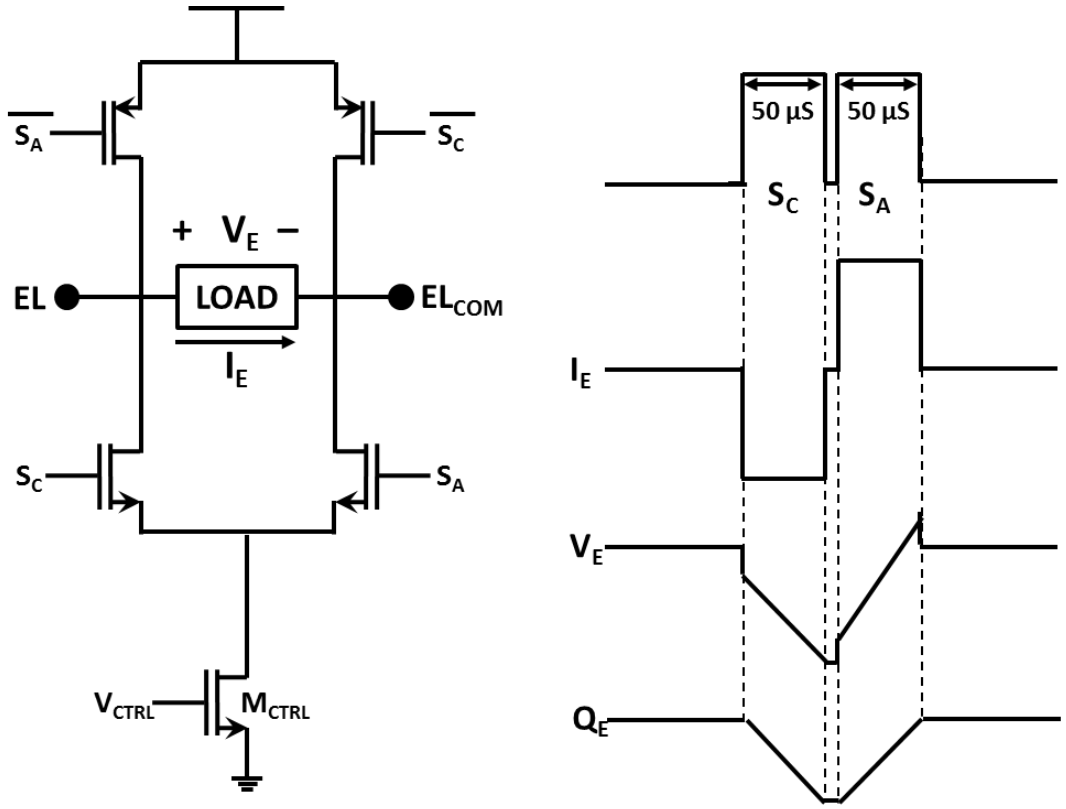


Figure 4.1. The single supply CSS and charge balanced load characteristics

4.3. Modified Single Supply CSS and Operation Principle

Single supply CSS structure is modified with the addition of an extra current source (M_{CB}) and a switch (Sw_0) (Figure 4.2). The charge balance current (I_{CB}) is generated

by M_{CB}, controlled by voltage V_{CB} and cycle controlled by switch Sw_0. The electrode voltage is monitored by charge balance circuit before the stimulation occurs. The monitoring operation is enabled by charge balance enable (CB_{EN}) signal.

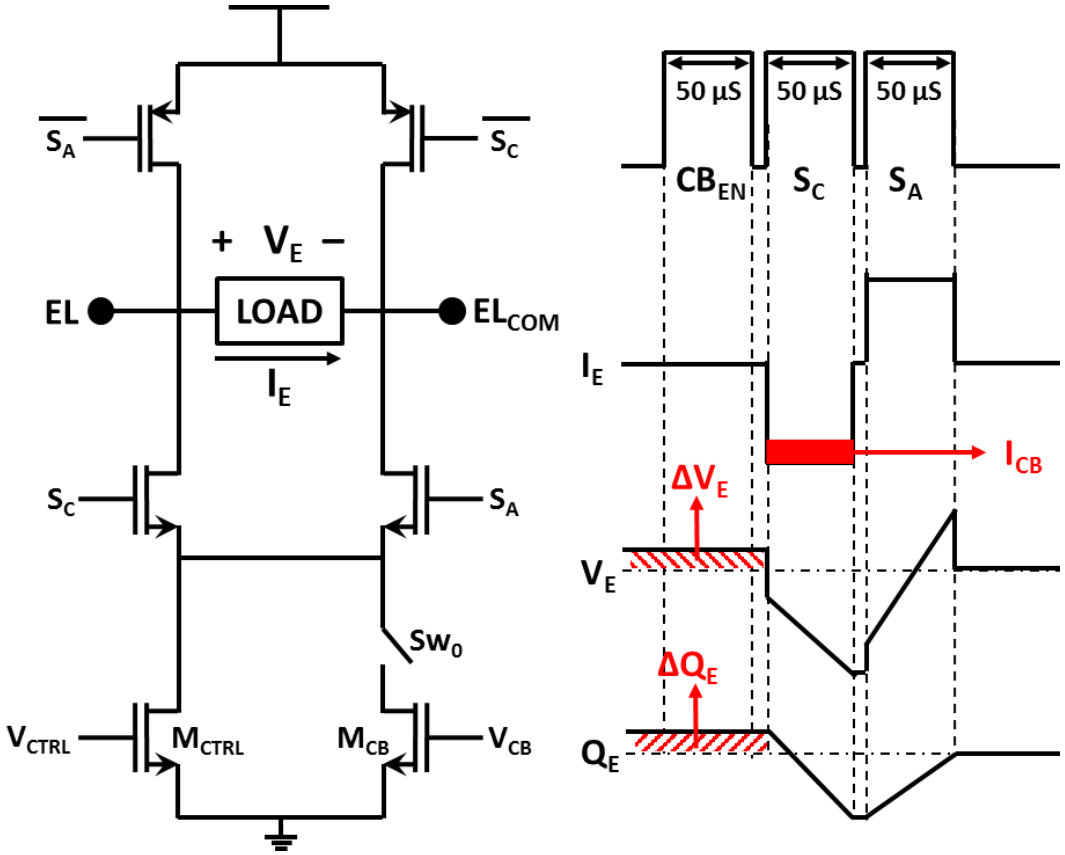


Figure 4.2. Modified CSS and charge unbalanced load characteristic

Charge balance circuit generates V_{CB} voltage from electrode voltage difference (ΔV_E) and determines the charge balance cycle from the sign of the electrode voltage while CB_{EN} is HIGH. In the stimulation, the charge balance current is generated from the stored V_{CB} signal at pre-determined cycle. With the charge balance current, the electrode charge stays in the safe region. By enabling charge balance current together with the stimulation current, synchronous operation is achieved.

4.4. Block Diagram of the Charge Balance Circuit

Figure 4.3 shows the overall block diagram of the synchronous charge balance circuit including the connection of the sub blocks. The system can be inspected in three major parts which are sensing, control and output. The charge balance circuit is designed in XFAB 0.18 µm High Voltage technology.

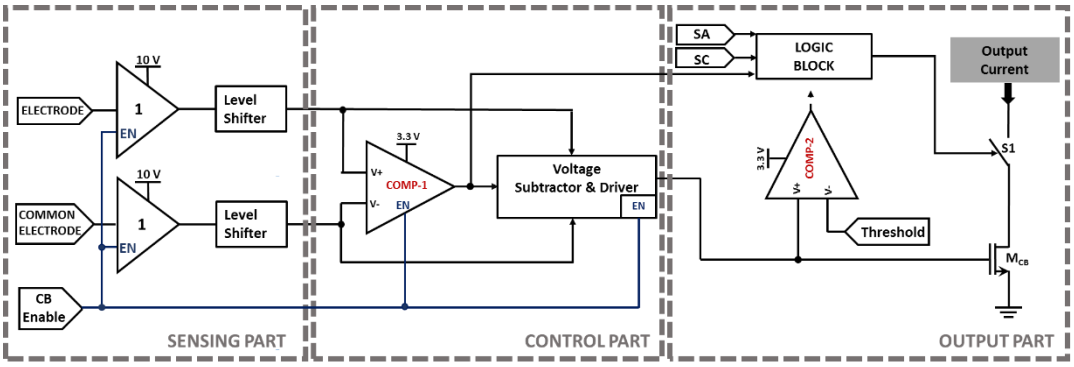
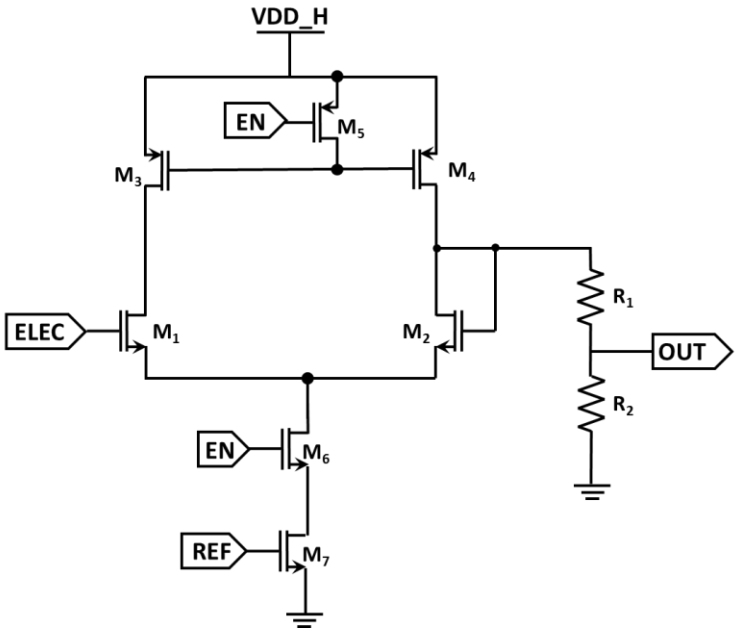


*Figure 4.3.*Block diagram of the charge balance circuit

The sensing part is used for sampling the voltages on the electrodes which varies from 2 V to 10 V. The input buffers are used for sampling the electrode voltage without effecting stimulation current. Resistive level shifters are connected at the output of the buffers to decrease the voltage level lower than 3.3 V for minimizing power consumption. The control part determines the voltage difference between electrodes and the polarity of the difference. Output current is generated according to the electrode voltage polarity and the difference at the output part. By using electrode voltage polarity, high voltage control block (HV CONTROL) determines the charge balance current time. If the voltage difference is higher than the threshold voltage, the voltage difference is converted to the charge balance current on M_{CB} transistor. The threshold operation is used for power saving.

4.4.1. Sensing Part

Sensing part is used to detect electrode voltage without disturbing balance. The system is enabled before the stimulation and samples the electrode voltage. One stage differential amplifier satisfies the gain requirement. The schematic of the sensing part can be seen from Figure 4.4. Since the electrode voltages are high as 10 V, the all transistors $M_{1\text{-}7}$ are chosen as high voltage transistors. Their junctions can operate properly up to 10 V and threshold voltages are high. The input transistors are chosen as N-type because they should operate at the higher voltages. The resistors are added at the output of the buffer for level shifting operation. The output voltage is divided by five and compressed between 0.4 - 2 Volts. The supply voltage is decreased to the 3.3 Volts for the rest of the circuit by level shifting operation. By decreasing the supply voltage, the area and the power consumption are significantly decreased.



M_1	40 µ / 2.9 µ
M_2	40 µ / 2.9 µ
M_3	10 µ / 2.9 µ
M_4	10 µ / 2.9 µ
M_5	5 µ / 2.9 µ
M_6	5 µ / 10 µ
M_7	5 µ / 10 µ
R_1	10 MΩ
R_2	2.5 MΩ

Figure 4.4. Schematic of the sensing part

Figure 4.5 shows the DC sweep analyses of the sensing part with corners. The input electrode voltage is swept from 0 Volts to 10 Volts and output is recorded. The sensing part can operate in all corners for the input range 2 V to 10 V with linear characteristics.

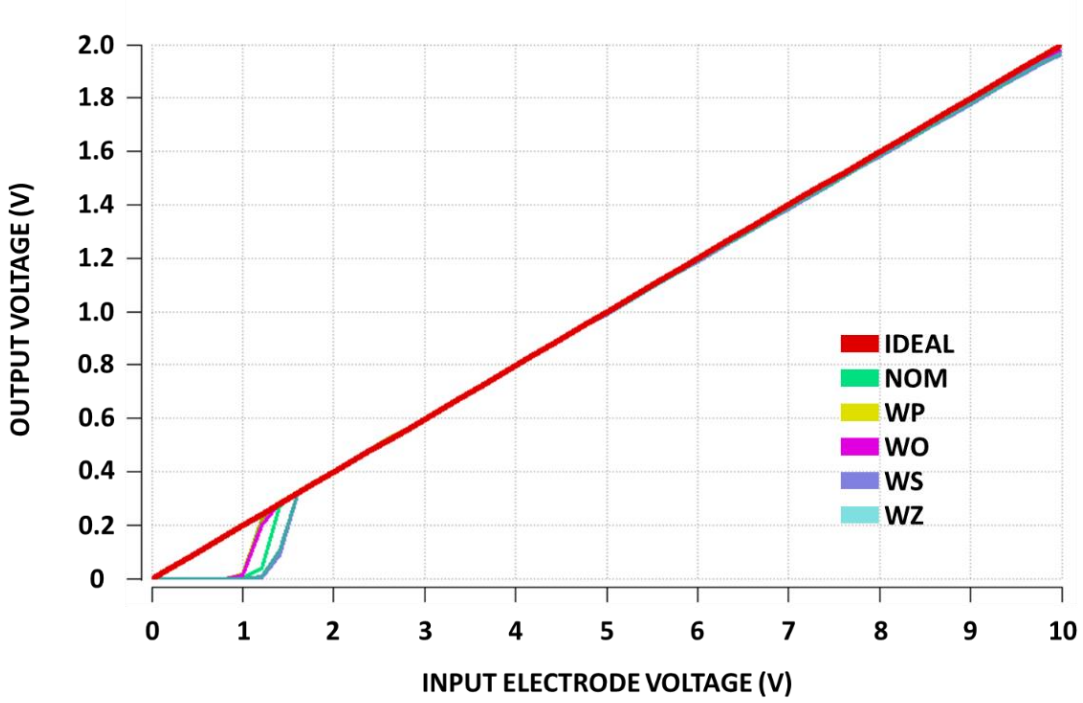


Figure 4.5. Corner simulation of the sensing part (Corners can be seen from Table 2.1.)

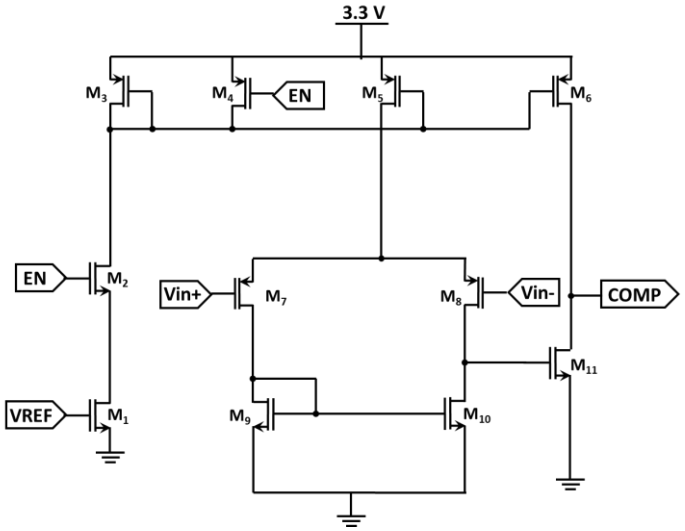
4.4.2. Control Part

Control part determines the charge balance current value and its polarity. The difference between electrode voltages is used for determining current value. The comparison of the input voltages determines the polarity of the unbalanced charged. The control part is enabled before the stimulation, together with the sensing part. The supply voltage of the control part is 3.3 V and its input is generated by sensing part. It consists of 3 blocks which are comparator, voltage subtractor circuit and its driver.

4.4.2.1. Comparator

The comparator is used to determine the polarity of the unbalanced charge and its output is used in the voltage subtractor driver circuit. The schematic of the comparator can be seen from Figure 4.6, which is a two-stage op-amp. The $M_{1\text{-}4}$ transistors are biasing transistors. The first stage of the comparator is P-type differential amplifier and the second stage is a common source amplifier for increased gain. The all transistors are working in the subthreshold region for lower power consumption. The

P-type differential pair gives better noise performance since they have n-well implantation.



M_1	17.5 µ / 0.35 µ
M_2	3.5 µ / 0.35 µ
M_3	4.0 µ / 2.0 µ
M_4	4.0 µ / 2.0 µ
M_5	4.0 µ / 2.0 µ
M_6	4.0 µ / 2.0 µ
M_7	8.0 µ / 2.0 µ
M_8	8.0 µ / 2.0 µ
M_9	5.0 µ / 2.0 µ
M_{10}	5.0 µ / 2.0 µ
M_{11}	10.0 µ / 2.0 µ

Figure 4.6. Schematic of the comparator

Figure 4.7 shows the common mode characteristic of the amplifier. Since the electrode voltages of the common mode is not constant, the comparator should give same gain in the range between 0.4 V to 2 V. Figure 4.8 represents the AC analysis of the comparator with corner analyses. The comparator gives 55 dB gain in all corners. The phase margin of the amplifier is greater than 31.0˚, so the amplifier is stable.

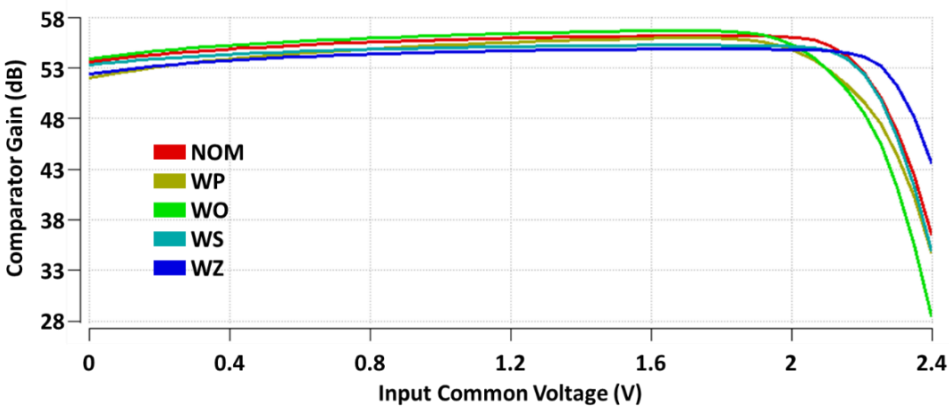


Figure 4.7. Comparator gain respect to input common voltage (Corners can be seen from Table 2.1.)

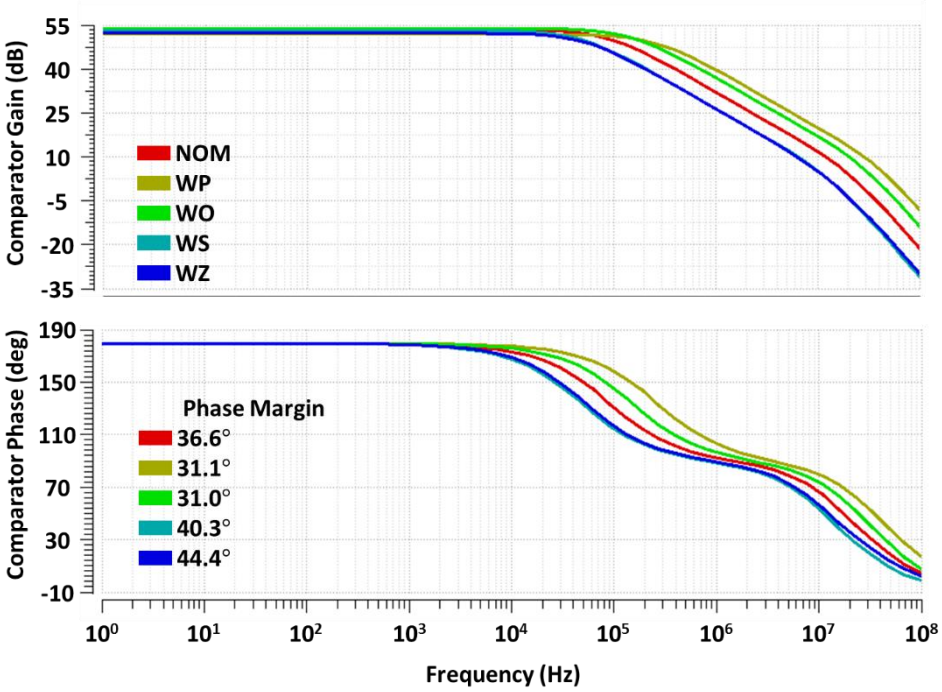


Figure 4.8. Comparator corner AC analysis (Corners can be seen from Table 2.1.)

4.4.2.2. Voltage Subtractor Driver Circuit

Voltage subtractor circuit requires a driver circuit because the subtractor circuit cannot subtract high voltages from low voltages. The driver circuit solves this problem and arranges the inputs of the subtractor circuit according to the input voltage magnitudes. Driver circuit uses 4 CMOS pass logic as switches, comparator output and its inverse. The schematic of the driver circuit can be seen from Figure 4.9. The switch sizes are minimized to decrease capacitive effect at the output. S_1 and S_4 switches pass the lower voltage, S_2 and S_3 switches pass the higher voltage. The switches are controlled by the comparator output and its inverse.

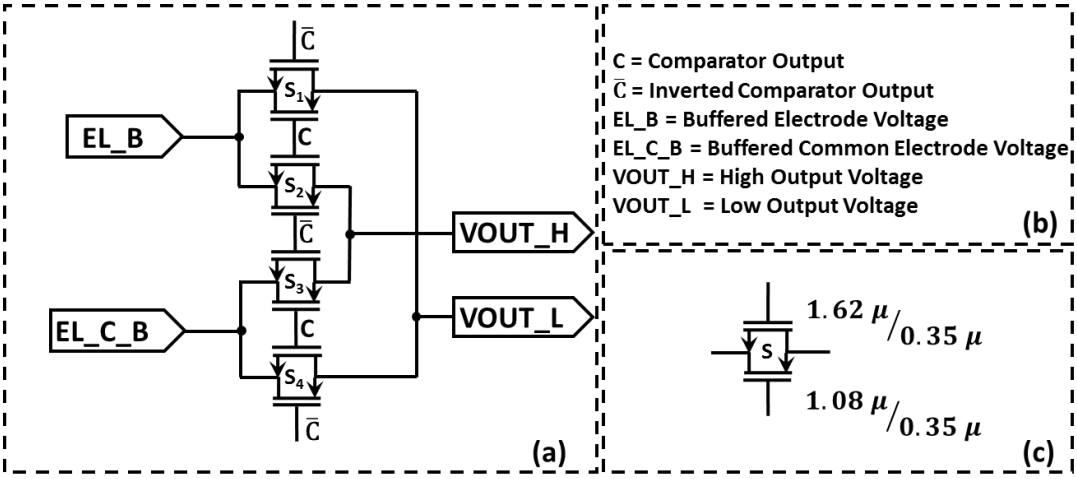


Figure 4.9. Driver circuit schematic (a), abbreviations (b) and switch sizes (c)

4.4.2.3. Voltage Subtractor Circuit

The voltage subtractor generates the output voltage according to the input difference and the charge balance current is generated according to the output voltage of the subtractor. The output voltage should not be affected from input common voltage. Figure 4.10 shows the schematic of the voltage subtractor circuit. The sizes of the transistors are given in Table 4.1. The bias current is generated via M_6 and M_2 transistors. The M_4 and M_5 transistors are kept in the linear region and their currents are controlled by the input voltage. The M_1 and M_2 transistors are used as current limiter. After the generation of the I_1 and I_2, they are subtracted on M_9 and M_{10} transistors. The current is amplified once more and changes the direction from sink to source with M_{11} and M_{12} transistors. The output voltage is generated on gate of the diode connected M_{14}. The buffer and C_S capacitance are used for storing generated voltage. The M_{13} transistor is used for discharging of M_{14} which is a high voltage transistor and has higher threshold voltage. M_{14} generates higher gate voltage with small current. The gate of the M_{CB} requires high voltages to generate charge balance current because M_{CB} is also high voltage transistor. The C_S is a small on-chip capacitance with 2 pF capacitance. The capacitor saves the data before the stimulation

and stores voltage to generate the charge balance current at the stimulation. The buffer at this stage is same as the comparator of this part.

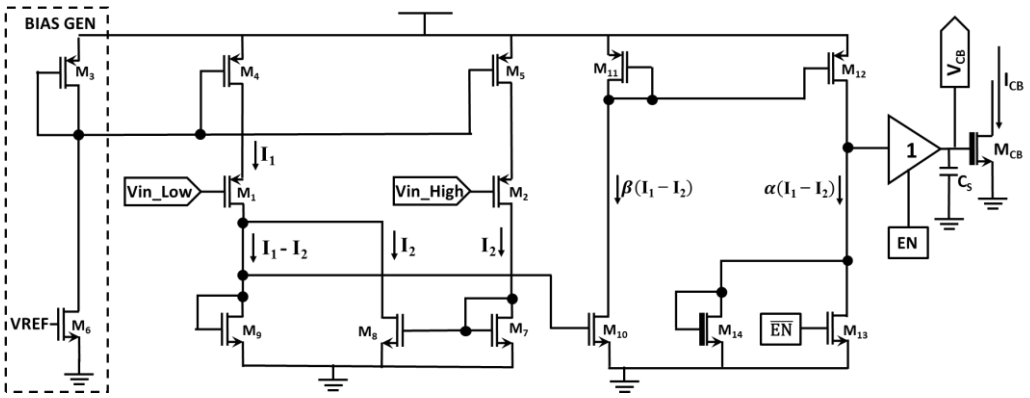


Figure 4.10. Schematic of the subtractor circuit

Table 4.1. *Subtractor circuit transistor sizes*

Transistor	***Sizes***	***Transistor***	***Sizes***
$M_{1\text{-}2}$	$1.00\,\mu\,/\,10.00\,\mu$	M_{10}	$5.25\,\mu\,/\,0.35\,\mu$
M_{3}	$1.00\,\mu\,/\,0.35\,\mu$	M_{11}	$0.35\,\mu\,/\,0.35\,\mu$
$M_{4\text{-}5}$	$2.00\,\mu\,/\,0.35\,\mu$	M_{12}	$24.50\,\mu\,/\,0.35\,\mu$
M_{6}	$2.50\,\mu\,/\,5.00\,\mu$	M_{13}	$2.50\,\mu\,/\,0.50\,\mu$
$M_{7\text{-}8}$	$20.00\,\mu\,/\,1.00\,\mu$	M_{14}	$2.50\,\mu\,/\,15.00\,\mu$
M_{9}	$0.35\,\mu\,/\,0.35\,\mu$		

The DC characteristic of the circuit is given in Figure 4.11. The subtractor circuit gives nearly the same output voltage for different input common mode voltages. This characteristic is achieved by adjusting sizes of the M_1, M_2, M_4 and M_5 transistors. The M_4 and M_5 are in the linear region even if the input voltages are very low.

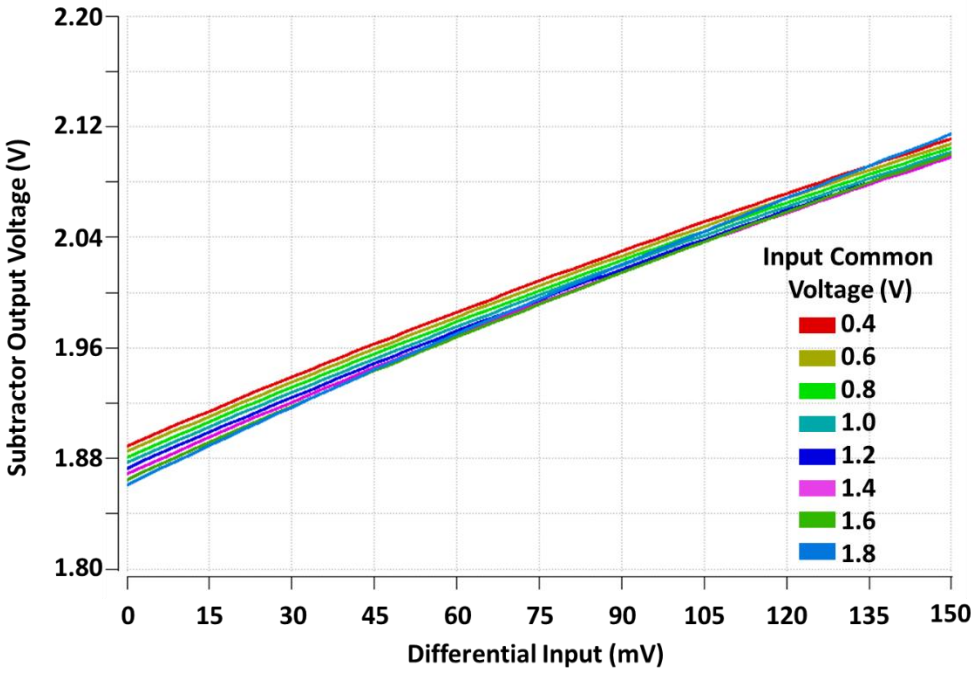


Figure 4.11. Subtractor circuit characteristic

4.4.3. Output Part

The output part works in both before and at the stimulation. Before the stimulation, digital blocks arrange the operation cycle according to the comparator output with using basic logic gates (Figure 4.12).The SC and SA inputs are the timing inputs for the source and sink cycles of the constant current stimulator.

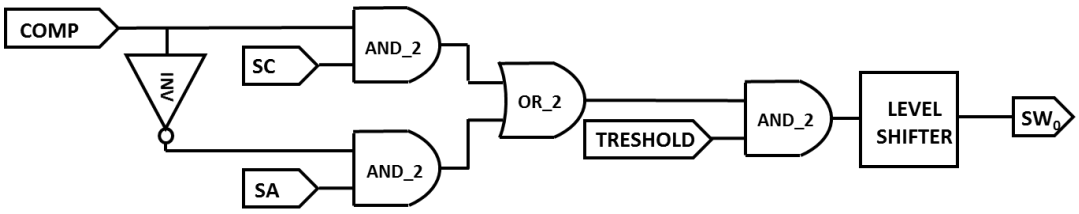
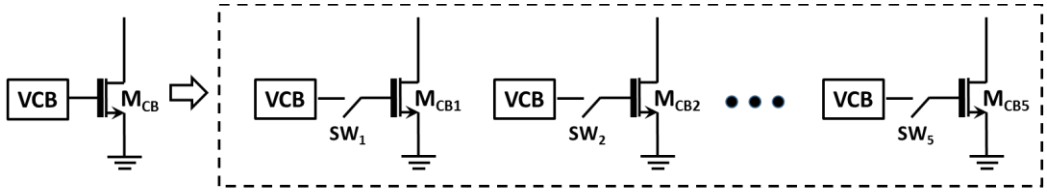


Figure 4.12. Logic diagram of the control block

Output part comparator, which is the same as the control part comparator is used for determining threshold for charge balancing. By threshold operation, the power consumption is decreased and noise on the electrode voltages cannot generate charge

balance current. M_{CB} (Figure 4.13) generates the output charge balance current and its size is adjustable. It has to be adjusted according to the capacitor of the electrode. The charge balance current multiplier can be adjusted from 1 to 63 by closing switches ($SW_{1\text{-}5}$).



Transistor	M_{CB1}	M_{CB2}	M_{CB3}	M_{CB4}	M_{CB5}
Size	75 µm / 15 µm	150 µm / 15 µm	300 µm / 15 µm	600 µm / 15 µm	1200 µm / 15 µm

Figure 4.13. Output transistor schematic

4.4.4. Simulation of the Overall Circuit

All the simulations are performed by using extracted view of the drawn layout (Figure 4.14). Overall simulation of the charge balance circuit is given in Figure 4.15. The electrode charge is calculated from the capacitance voltage by scaling the capacitance value. The test is conducted with constant stimulation current, which is 500 µA, using 3 kΩ, 100 nF ([44]) electrical load. The charge balance current is activated when the total charge of the electrode passes the threshold value. The charge balance current is activated in the sink cycle of the operation and the net charge of the electrode is kept in the safe region.

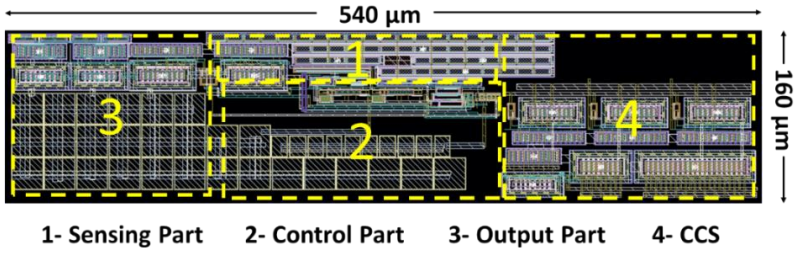


Figure 4.14. Layout of the synchronous charge balance circuit

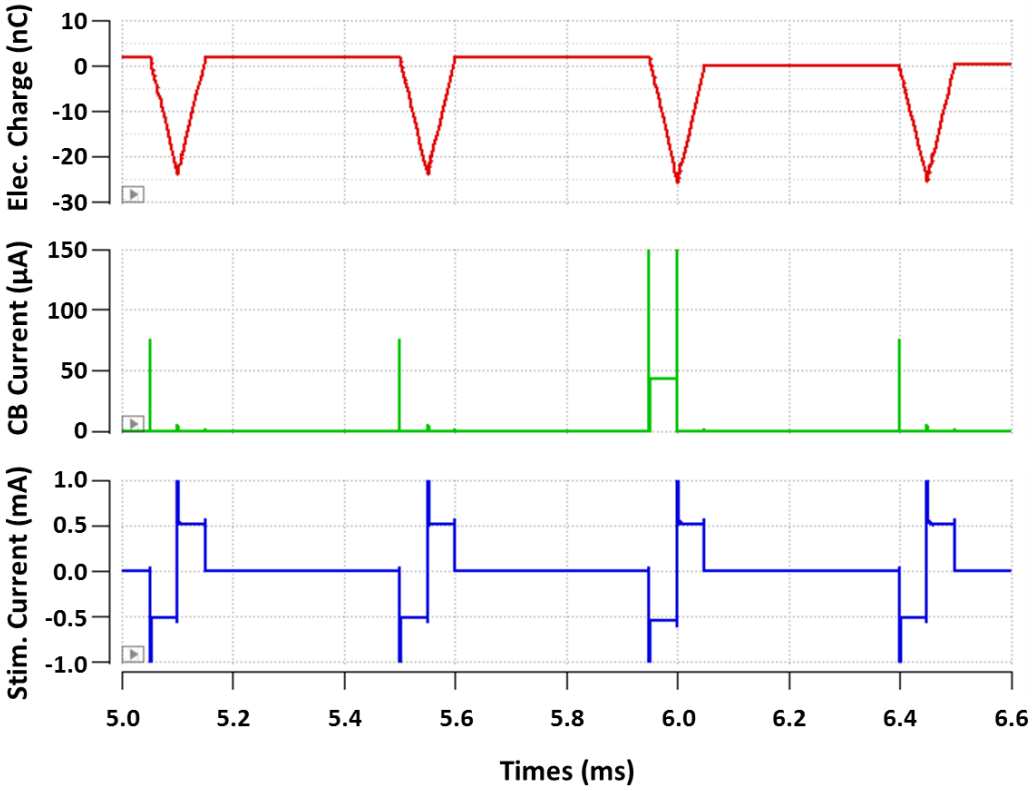


Figure 4.15. Current and charge waveforms of the charge balanced system

Figure 4.16 shows the balancing operation with different constant stimulation currents. The electrode charge is calculated from the integral of the electrode current. To observe the charge balance performance, constant current stimulation is used with a constant mismatch in each cycle. Series 100 nF and 3 kΩ ([44]) are used as an electrical load. The circuit keeps the net charge under certain threshold without disturbing the stimulation. The unbalanced charged increases with increasing stimulation current. In addition, charge balance current generation frequency is also increased.

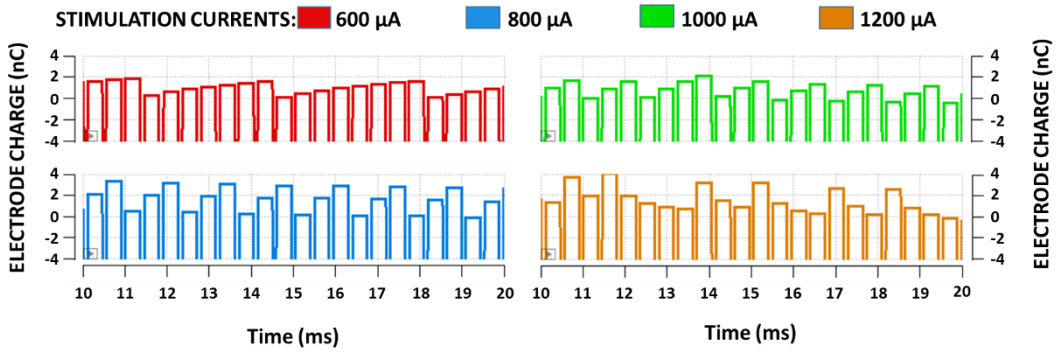


*Figure 4.16.*Simulation of the charge balanced circuits with different constant stimulation currents

4.5. Experimental Test Results

The fabricated chips micrograph can be seen from Figure 4.17 and active area of the charge balance circuit is 160 µm x 540 µm. Circuit is tested with different constant current stimulations and capacitor voltages are recorded. The electrode charge is calculated from the capacitor voltage. The system tested with both DC and transient analyses. The DC analysis of the test results shows the generated charge balance current ratings with respect to the input voltage difference. The transient analysis shows the time domain operation of the charge balance circuit with constant stimulation current.

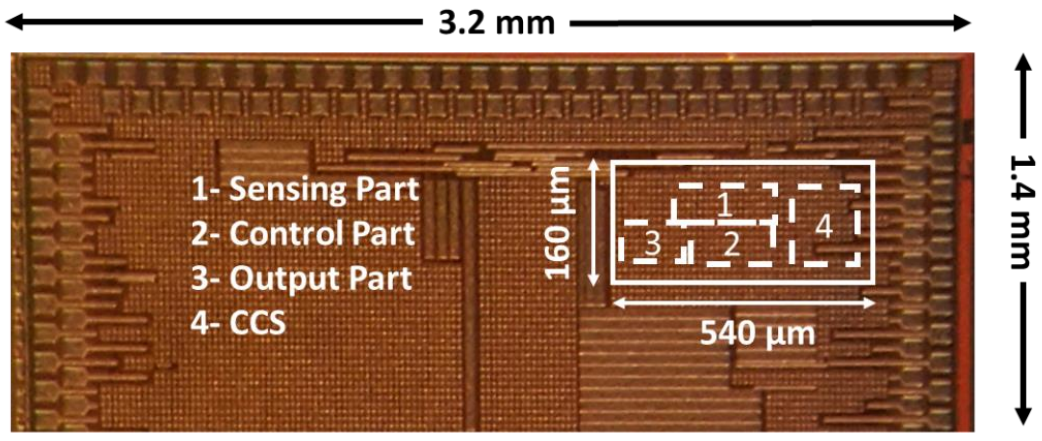


Figure 4.17. Die micrograph of the fabricated charge balance circuit

4.5.1. DC Analysis of the System

Figure 4.18 shows the DC analysis of the system. For this test, the electrode voltages are replaced with a DC source. The common electrode (V_{HIGH}) voltage is kept constant and electrode voltage is swept. At the output, generated charge balance current is observed. As shown in the graph, the output charge balance current is not affected from the input offset voltage and can supply same current for the same voltage difference. The input difference range can be extended by increasing level shifter gain. The output current is not zero even if the input voltage difference is zero. This problem is solved by threshold comparator.

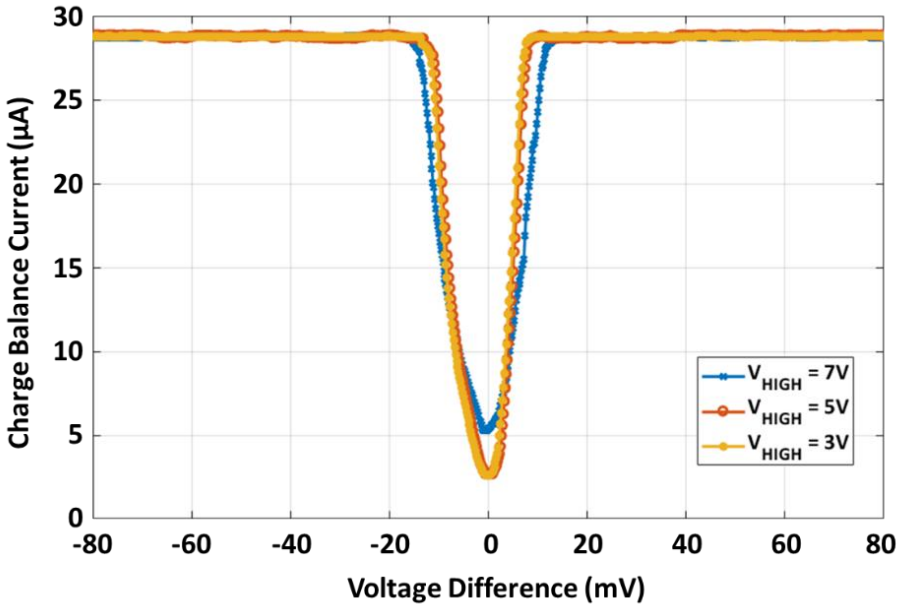


Figure 4.18. DC analysis of the charge balance circuit

4.5.2. Transient Analysis of the System

Single supply current stimulator circuit is first tested without charge balance circuit and maximum residual charge is calculated for different stimulator current levels. Then, synchronous charge balance circuit is connected to the system and same tests are performed. The results can be seen from Figure 4.19. The charge of the capacitor is calculated from the voltage of the electrode capacitor.

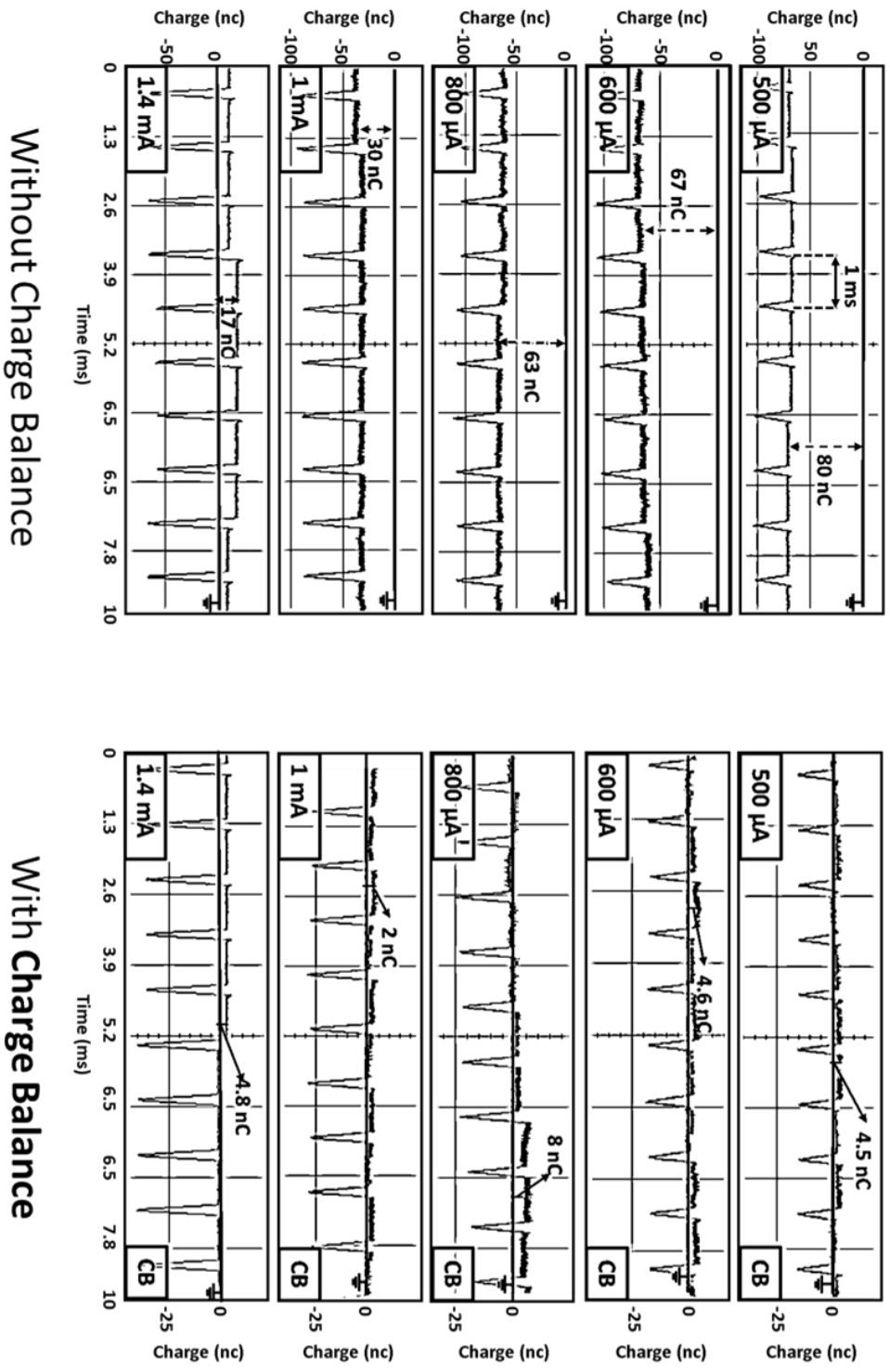


Figure 4.19. Transient analysis of the single supply current stimulator with & without charge balance circuit.

Charge balance circuit effects respected to constant stimulation current is given in Figure 4.20. From the graph the charge balance circuit limits the residual charge at the electrode. The maximum charge at the electrode is 8 nC with this value the system does not harm the human tissue during stimulation. Since 100 nF capacitance is used as an electrode capacitance, the maximum electrode voltage does not exceed 12 mV.

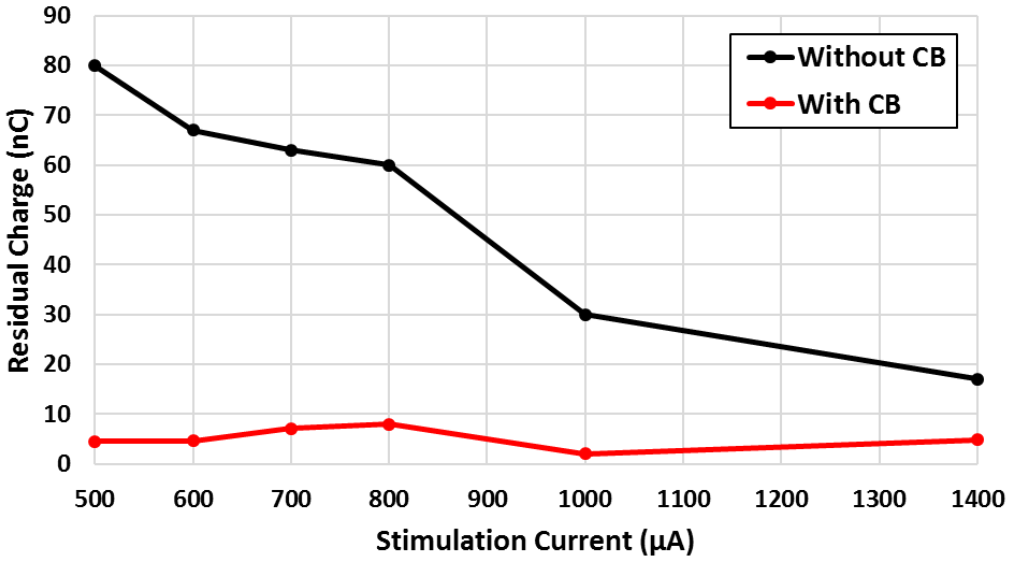


Figure 4.20. Variation of the residual charge with the stimulation current.

4.5.3. Summary of the Chapter

This alternative charge balance method can be used with single supply constant current stimulator. The power consumption of the design is quite low (6.36 µW) which is achieved by clock gating the charge balance circuit with enable signal for 50 µs in 1 ms stimulation period. Also, the charge balance circuit generates output current synchronously with the stimulation current and does not disturb the other electrodes and does not require an extra time after the stimulation. Low power consumption, low area occupancy and synchronous operation make the system more suitable for the implantable devices. The comparison of the circuit with the state-of-the-art charge balance circuit is given in Table 4.2. This work has the lowest power consumption with a good precision as low as 12 mV to the best of our knowledge.

Table 4.2. *Comparison of the state of art charge balance circuits*

Parameter	[52]	[53]	**[26]**	**[35]**	***FICI System***	***This Work*** [54]
Process	0.35 µm	0.7µm	PCB	0.35 µm	0.18 µm	0.18 µm
Electrode Voltage Compliance	22 V	15 V	30 V	4.2V	6 V	10 V
CB Method	Inter-Pulse Charge Control	Dynamic Current Balancin	Short Pulse Injection	Blocking Capacitor	Short Pulse Injection	Synchronous Charge Balance
Safety Window	<0.1 V	<6nA	<0.1 V	N/A	<0.1 V	<20 mV
Precision	<20 mV	<0.4%	<0.1 V	<22 mV	<60 mV	<12 mV
Power (µW)	56	47	N/A	N/A	31.72	6.36

CHAPTER 5

CONCLUSION AND FUTURE WORK

5.1. Summary of Contributions

In this thesis, a single battery fully implantable cochlear implant interface circuit with active charge balance has been designed and implemented. The aim of the designed interface circuit is low power operation, single battery usage for long term implantation and charge balanced stimulation for the safe operation. This implemented interface circuit is finally merged with multi-channel piezo-electric transducers and the full-system performance of the circuit is verified by in-vitro tests.

Accomplishment of this thesis can be listed as follows:

1. Literature is reviewed to understand the hearing mechanism in the previously designed CIs and FICIs and charge balance methods. The aim of the new design is to improve the previously designed FICIs and eliminate the drawbacks.

2. A new FICI interface circuit architecture for low power consumption with charge balanced stimulation is introduced. The major advantages of the proposed circuit can be explained as follows: It is fully-implantable with a single battery and ensures safe stimulation without harming tissue. The final system consists of four main parts. The first part is front end structure which takes the input from piezo electric sensors and converts it to the digital data. The second part generates pulse width modulated stimulation current from the digital data. The third part is charge balance circuit which monitors the electrode voltages and limits the voltage difference by generating charge balance current. The fourth part is the required blocks for implantation which are DC-DC converter, clock generator and voltage reference circuits. The proposed circuit is designed and implemented in TSMC 180 nm high voltage process which has high voltage transistors for stimulation part and low voltage transistor for the front-end part. The performance of the chip is tested with in vitro

experiments. The system consumes 695 µW from 1.8 V single battery and charge balance circuit limits the electrode voltage within 60 mV range. The system can operate up to 18 days with 200 mWh battery without any recharge. The input dynamical range of the system starts with 50 dB SPL (light traffic sound) and covers 100 dB SPL (factory machinery sound). The single chip area occupies 2.44 mm^2 which can be implantable inside the ear. The multi-channel stimulation currents generated according to the CIS strategy and the frequency of the single channel is 1 kHz.

3. Another charge balance circuit is designed for the FICI system which is synchronous charge balance circuit. This charge balance circuit does not require time gap at the stimulation. It generates charge balance current with the stimulation cycles. The circuit occupies very low area and consumes only 6.36 µW which is desired for implantable stimulators. The circuit consist of three main parts. The first part observes the electrodes by operational amplifiers. The second part calculates electrode difference and third parts generates the charge balance current. The charge balance circuit is tested with electrical load and it limits the electrode voltage difference within 60 mV range.

5.2. Future Work

Since the FICI system looks like ready for implantation, some parts of the system have potential for a future research. The future work can be listed below:

1. In vivo tests can be performed with animal subjects for the validation of charge balanced FICI system. These tests were performed in BioMEMS Research Group by B. Yüksel, H. Ulusan and me. Hence, same tests can be done for this chip.

2. The new generation of the system can be designed with a higher resolution ADC to extend input dynamical range and more precise stimulation currents. Moreover, the channel number of the system can be increased to 16. The DC-DC converter can be improved. The charge pump stage numbers can be increased to increase electrode voltage compliance. The regulation circuit can be added at the

output of the DC-DC circuit for more stable output voltage. An on-chip output capacitance can be added to the charge pump circuit.

3. For patient fitting and battery recharge, a wireless data and power transmission module can be added to the system. Memory elements and microprocessor are required for data transmission and rectifier circuit is required for the power transmission.

4. The synchronous charge balance circuit can be designed with a multi-channel structure and merged with any FICI system. Then, in vitro and in vivo tests can be performed for the validation of the operation.

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