HIGH POWER, GAN, QUARTER-WAVE LENGTH SWITCHES FOR X-BAND APPLICATIONS

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submitted by **DUYGU IŞINSU TURAN** in partial fulfillment of the requirements for the degree of **Master of Science in Electrical and Electronics Engineering Department, Middle East Technical University** by,

Prof. Dr. Halil Kalıpçılar
Dean, Graduate School of **Natural and Applied Sciences** _____

Prof. Dr. İlkay Ulusoy
Head of Department, **Electrical and Electronics Eng.** _____

Prof. Dr. Hatice Özlem Aydın Çivi
Supervisor, **Electrical and Electronics Eng., METU** _____

Dr. Fatih Koçer
Co-Supervisor, **Analog Devices, Inc., Chelmsford, MA, USA** _____

Examining Committee Members:

Prof. Dr. Sencer Koç
Electrical and Electronics Eng., METU _____

Prof. Dr. Hatice Özlem Aydın Çivi
Electrical and Electronics Eng., METU _____

Prof. Dr. Haluk Külah
Electrical and Electronics Eng., METU _____

Prof. Dr. Şimşek Demir
Electrical and Electronics Eng., METU _____

Prof. Dr. Ekmel Özbay
Electrical and Electronics Eng., Bilkent University _____

Date: 04.12.2019

I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

Name, Surname: Duygu Işınsu Turan

Signature:

ABSTRACT

HIGH POWER, GAN, QUARTER-WAVE LENGTH SWITCHES FOR X-BAND APPLICATIONS

Turan, Duygu Işınsu
Master of Science, Electrical and Electronics Engineering
Supervisor: Prof. Dr. Hatice Özlem Aydın Çivi
Co-Supervisor: Dr. Fatih Koçer

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RF switches are one of the main building blocks of many communication and radar systems. In time-multiplex systems they are used to switch between the high power transmit path and the high sensitivity receive path, and thus needs to exhibit low insertion loss, while achieving high isolation. Low insertion loss for such switches reduces signal degradation on either path, while high isolation reduces signal leakage from the transmitter to the receiver.

Since switches are connecting the antenna and the transmit/receive paths, they should also be very linear, in order not to introduce any nonlinearities to the signal. They should be able to handle large input power values, especially when used in radar systems.

This thesis presents two single pole double throw switches built on Gallium Nitride (GaN) on silicon carbide (SiC) technology as a part of transceiver module designed for X-band radar applications. Both of the switches are designed to handle 25 Watts of input power. Fabricated die of Configuration I shows nearly 0.3 dB of insertion loss for most of the part of the band of interest. The die area of the switch is 2.9 x 2.1 mm^2. Measurement results of Configuration II exhibits an isolation of better than 50 dB while offering insertion loss better than 0.8 dB for most of the band. Both of the

switches are very well matched. Measured return loss of switches are better than 15 dB, and 13 dB, for Configuration I, and Configuration II, respectively, for the frequency band of operation.

Keywords: RF Switch, Single Pole Double Throw, High Power, GaN, High Isolation

ÖZ

X-BANT KULLANIMI İÇİN YÜKSEK GÜÇLÜ, GAN, ÇEYREK DALGA BOYU ANAHTARLAR

Turan, Duygu Işınsu
Yüksek Lisans, Elektrik ve Elektronik Mühendisliği
Tez Danışmanı: Prof. Dr. Hatice Özlem Aydın Çivi
Ortak Tez Danışmanı: Dr. Fatih Koçer

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RF anahtarlar birçok haberleşme ve radar sisteminin yapıtaşlarındandır. Zaman çoğullamalı sistemlerde yüksek güçlü verici yolu ile hassasiyeti yüksek alıcı yolu arasında anahtarlama yaptıklarından düşük araya grime kaybı ve yüksek izolasyon sağlamaları önem arz etmektedir. RF anahtarlar birçok haberleşme ve radar sisteminin yapıtaşlarındandır. Zaman çoğullamalı sistemlerde yüksek güçlü verici yolu ile hassasiyeti yüksek alıcı yolu arasında anahtarlama yaptıklarından, düşük araya girme kaybı ve yüksek izolasyon sağlamaları önem arz etmektedir. Bu tip anahtarlar için düşük araya girme kaybı her iki yol için sinyal gücü kaybını engellerken yüksek izolasyon vericiden alıcıya sinyal sızmasını azaltır.

Anahtarlar anten ve verici/alıcı yollarını birbirine bağladıklarından doğrusal olmaları sinyale doğrusal olmayan bileşenler katmamaları açısından ayrıca önemlidir. Anahtarların özellikle radar sistemlerinde kullanıldıklarında yüksek giriş güçlerine dayanıklı olmaları gerekmektedir.

Bu tezde X-bant radar uygulamalarında kullanılmak üzere tasarlanmış alıcı-verici devresinin bir parçası olarak Silisyum Karbür (SiC) üzerine Galyum Nitrür (GaN) teknolojisi kullanılarak inşa edilmiş tek kutuplu çift atışlı iki anahtar sunulmaktadır. Anahtarların ikisi de 25 Watt'lık giriş gücüne dayanmak üzere tasarlanmıştır. Üretilen

Konfigürasyon I X-bandın çoğunda yaklaşık 0.3 dB'lik araya girme kaybı göstermektedir. Çip alanı 2.9 x 2.1 mm^2'dir. Konfigürasyon II için ölçüm sonuları, X-bandın çoğunda 50 dB'den yüksek izolasyon sunarken ilgili bandın tamamında 0.8 dB'den daha başarılı araya girme kaybı göstermektedir. İki anahtar da başarılı bir şekilde eşlenmiştir. Anahtarlar için ölçülen dönüş kaybı Konfigürasyon I için 15 dB'den, Konfigürasyon II için 13 dB'den başarılıdır.

Anahtar Kelimeler: RF Anahtar, Tek Kutup İki Atım, Yüksek Güç, GaN, Yüksek İzolasyon

To My Family

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CHAPTER 1

INTRODUCTION

RF switches have a wide range of use especially in communication and radar systems. They enable RF signal transmission between antennas and transmit/receive ports for transceiver systems. The transceiver systems are mainly composed of power amplifier (PA) and low noise amplifier (LNA). The switches used in transceiver systems provide switching between these components and antenna, and thus should exhibit low insertion loss while achieving high isolation.

This thesis presents the theory, design, and evaluation of two single pole double throw switches built on Gallium Nitride (GaN) on silicon carbide (SiC) technology to complete the signal chain of a fully integrated transceiver module designed for X-band radar applications. The switches presented in this thesis are designed to handle 25 Watts (44 dBm) of input power, which is output power of the power amplifier in the transceiver.

There exist many substrates to build the overall design on like GaAs, Silicon-on-Insulator (SOI), etc. in addition to GaN. Beside Field Effect Transistors (FETs), other switch device candidates are PIN diodes. PIN diodes are composed of three regions; P-region (p-type semiconductor), I-region (intrinsic semiconductor), and N-region (n-type semiconductor). When forward-biased, PIN diodes conduct, and allows signal transmission, and when reverse-biased, they behave as capacitors. Both FETs and PIN diodes can be modelled as resistors when they are in ON-state, and capacitors when they are in OFF-state, where ON-state resistances are current-controlled for PIN diodes, and voltage-controlled for FETs. In case of power consumption consideration, PIN diodes are disadvantageous because of the current-driven behaviour. FET based switches consume significantly low power compared to PIN diodes.

As FET based switches are appropriate for power consumption considered applications, some of the substrates, such as SOI and GaAs, are not capable of handling high power because of their relatively low breakdown voltages. In order to improve power handling capacity of the OFF-state branch, stacking of transistor technique may be used which increases the complexity, and the size of the design. Although GaAs have higher breakdown voltage compared to SOI substrate, GaAs pHEMTs suffer from gate leakage current which limits the power performance [1].

Apart from HEMT and PIN diode based switches, microelectromechanical systems (MEMS) switches are also available in literature. MEMS switches provide open or short circuit by mechanical movement in RF transmission line. To obtain desired mechanical movement, electrostatic, magnetostatic, piezoelectric or thermal forces may be used. Since MEMS switches use mechanical movements, performance of these switches are close to ideal switch performance with high isolation and low insertion loss [2]. Being fabricated with air gaps also helps increasing isolation performance by diminishing off-state capacitance [3]. Main drawback of MEMS switches is their inadequate power handling performance [4].

The motivation behind using GaN substrate is mainly its high power capability caused by its wider bandgap compared to other technologies. In addition to high power capability, GaN also provides a fully integrated module. In case of using GaAs, LNAs need additional components in front of them, which are PIN diodes. PIN diodes are used to protect LNA from high power input signals which may permanently damage LNA. However, these limiters generally cannot be integrated into the same substrate as LNA itself, and thus increases the system size [5]. GaN devices, on the other hand can handle high power, thanks to the high bandgap of GaN, and do not need input limiter circuits [6]-[8]. Simplification of transceiver block is illustrated in Figure 1.1.

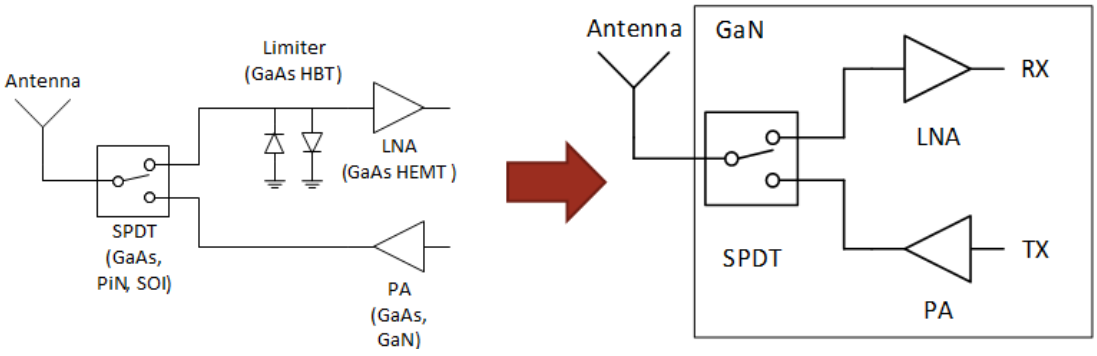


Figure 1.1 Simplification of Transceiver Diagram When Built on GaN

Some of the RF switches available in literature are listed in Table 1.1., which are built on GaN substrate. The switches are generally wideband switches with reasonable insertion loss, and isolation performance.

Table 1.1. *Performance of Some of GaN Based Switches Available in Literature*

Reference	**Operating Frequency (GHz)**	**IL (dB)**	**Isolation (dB)**	**Return Loss (dB)**	**Power (dBm)**	**Comp (dB)**	**Chip Size (mm^2)**
Campbell et al. (2010)	0-12	1	30	12	41	0.4	1.15x1.66
	0-18	1.5	25	12	40	0.4	1.15x1.66
Janssen et al. (2008)	8-11	3.5	30	10	44	-	4x1.8
Masuda et al. (2012)	0-12	1.2	30	-	39.2	1	1.8x2.4
Bettidi et al. (2008)	8-12	2	35	15	37	1	3.2x1.2
Osmanoglu et al.(2014)	0-12	1.4	20	14.5	40.5	0.2	1.7x0.94
Ciccognani et al.(2008)	8-11	1	37	13	>39.5	1	2.4x1.9
Alleva et al. (2008)	8-11	1	37	13	39	1	2.4x1.9
	2-18	2.2	25	11	38	1	2x1.7

Among the available X-band switches, the switch presented in [9] has the best performance with 1dB of insertion loss, 37 dB of isolation with 1-dB compression point at 39.5 dBm. The operating frequency band of the switch is 8-11 GHz. In this thesis, designing RF switches with similar insertion loss, isolation performance while enhancing power handling capability is aimed. The goals for the switch design for this work is given in Table 1.2.

Table 1.2. *The Goals for the Switch Design*

Operating Frequency (GHz)	8-12
Insertion Loss (dB)	< 2
Isolation (dB)	>25
P1dB (dBm)	>40
Input Power (Watts)	25

1.1. Thesis Organization

The content of this thesis is composed of 4 chapters. Next chapter focuses on the main switch topologies, and evaluation parameters for switches.

Chapter 3 presents the overview of GaN technology, discussing advantages and disadvantages among other available technologies. Moreover, detailed design of both switch configurations, measurement and simulation results for small signal and large signal parameters are presented.

On the 4th and the last chapter, conclusions are drawn, and performance comparison of the switches that are subject to this thesis and similar switches available in literature is laid out.

CHAPTER 2

BASIC CONSEPTS IN RF SWITCH DESIGN

2.1. Switch Topologies

Switches provide signal flow among desired ports, and create signal paths. Based on number of input and output ports switches are named. Single pole single throw (SPST) switches enable signal flow from one input port to one output port. Single pole double throw (SPDT) switches direct signal from one input port to one of two output ports, etc. In Figure 2.1, SPST, SPDT, double pole single throw (DPST), and double pole double throw (DPDT) switch diagrams are illustrated.

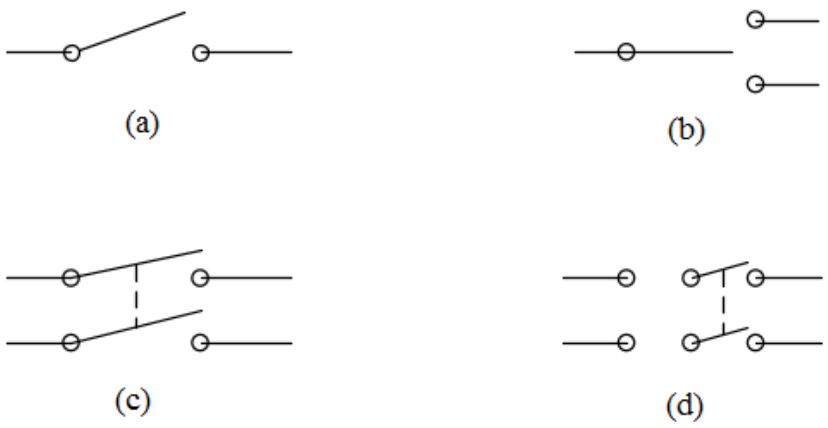


Figure 2.1. Switch Diagrams for SPST (a), SPDT (b), DPST (c), and DPDT (d) Switches

For transceivers, generally SPDT switches are used to direct signals between antennas and transmit/receive paths. In addition to transceiver modules used in radars, RF switches are also crucial components for wireless applications, which are currently used in dual-band, and triple-band cell phones. A switch in a cell phone may be used to transmit a signal or receive voice and/or data, which is called switching modes of operation. It can also be used to select of operation based on the information received

from the baseband antenna. This is called switching bands of operation. In Figure 2.2 and 2.3 usage of SP4T switches in cellular phones are illustrated. Figure 2.2 illustrates schematic of a cell module which provides operation at two different frequency bands while the module presented in Figure 2.3 can serve for four different frequency bands. Low pass filters (LPF) located between power amplifiers (PA) and antenna helps to reduce the magnitude of harmonics at high frequencies. Saw acoustic wave (SAW) filters between low noise amplifiers (LNA) and antenna are used as narrowband filters.

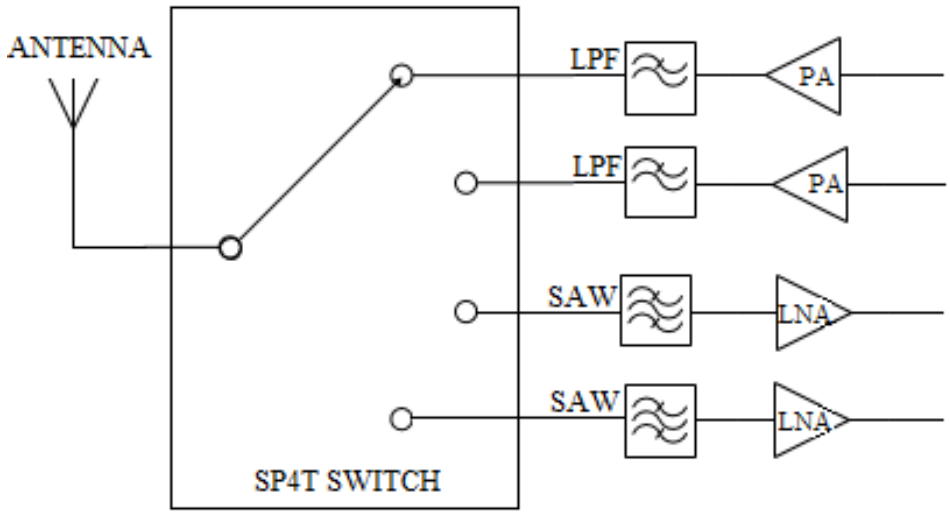


Figure 2.2. SP4T Switch Usage

Diplexers, which are combination of low pass filters (LPF) and high pass filters (HPF), separate low band and high pass filters.

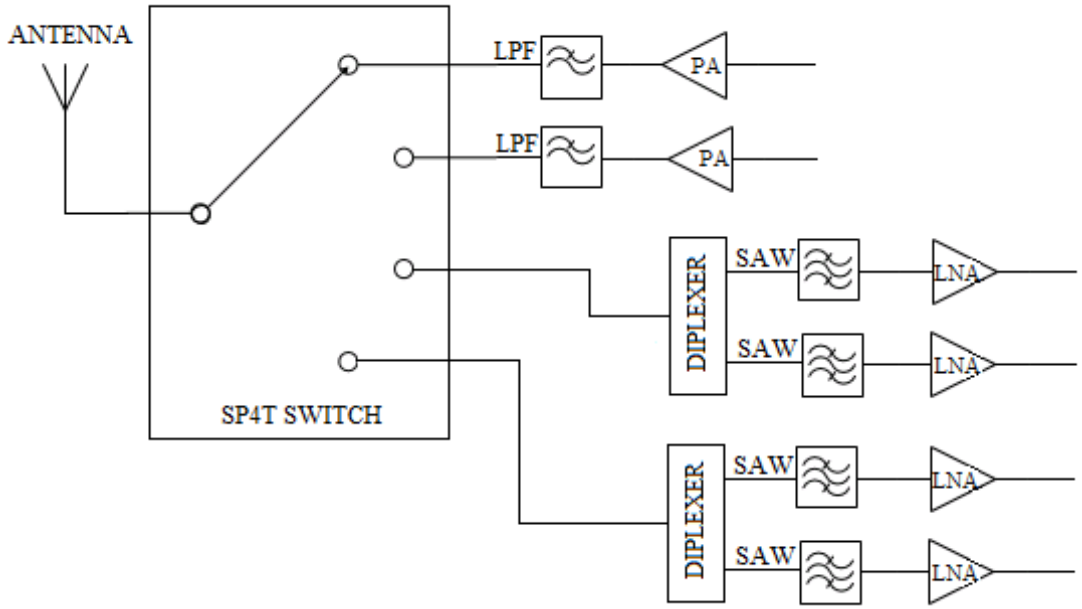


Figure 2.3. SP4T Switch Usage for Cellular Phone Application

2.2. Switch Design Considerations

Switches generally consist of series and shunt branches, where series branch is for signal flow and shunt part is for grounding leakage signal. Series and shunt elements of switch can include transistors, quarter wave-length transmission lines, PIN diodes, etc. Most common RF switch design approach is using transistors for shunt and series branches as in Figure 2.4 (a). Figure 2.4 (b) presents a switch configuration with series quarter wave-length transmission line and shunt transistor.

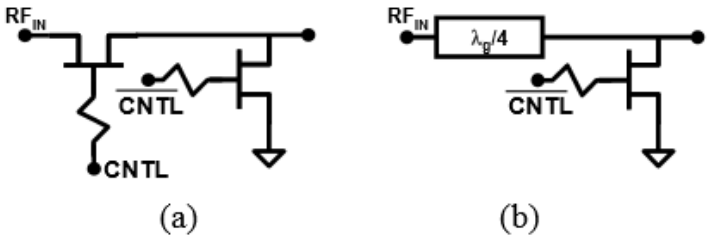


Figure 2.4. Serial Transistor (a) and Serial Transmission Line (b) Architectures

For Figure 2.4 (a), when series transistor, which is controlled by CNTL voltage, is in ON-state, shunt transistor is in OFF-state. Therefore, input signal flows through series

transistor, which behaves like a small resistance, to the output port. OFF-state transistor does not allow the signal to leak to the ground, because of its capacitive behavior in OFF-state. In order to stop the signal flow between input and output ports, a voltage below pinch-off should be applied to the series transistor from its gate and 0 V is appropriate for control voltage of shunt transistor; because GaN transistors are generally depletion type devices. Leakage signal is grounded through the shunt transistor.

Quarter wave transmission line behaves as open circuit when loaded with ground, and acts as short circuit when it is terminated by open circuit. The switch with quarter wave transmission line as series element illustrated in Figure 2.4 (b) works as follows; when the transistor is ON, the transmission line is terminated with a small-valued on resistance and transmission line is open circuited; when the transistor is in OFF-state, transmission line is loaded with off capacitor and shorted transmission line allows signal flow from input port to output port. In order to have a properly working switch, R_{on} should be low enough to have desired short-circuit behavior. Width of the transmission line is determined by 50-ohm termination, and the length is calculated as the quarter of the wavelength of the related operating frequency.

For configuration (a), most of the insertion loss is caused by series element. Limited isolation is another crucial concern for (a) which degrades with increasing frequency. The degradation is caused by parasitic capacitance which has impedance inversely proportional with frequency, and also gate width of the series device. Since length of quarter wavelength transmission line is inversely proportional with frequency, configuration (b) is disadvantageous if area is a critical parameter for design. However, for transceiver modules where the area of the design is mostly dictated by power amplifier, it is not the case.

If power handling should be taken into the consideration, topology (b) is more advantageous. For topology (b), the power handling is mostly dictated by the gate control voltage of transistor when the transistor is in its OFF-state. However, power

handling capability of topology (a) is determined not only by the control voltage of the shunt transistor but also by the current limit of the series device.

2.2.1. Switch Core with Transistors

Transistors can be modelled as a 2-port element, behaving like resistance when they are in ON state, and capacitor when they are in OFF state. 2 port model of a transistor is illustrated in Figure 2.5.

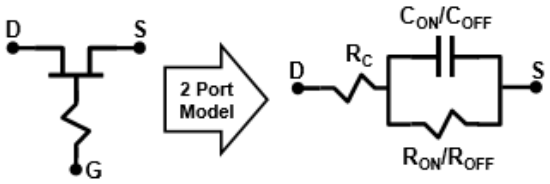


Figure 2.5. Two-Port Model of a Transistor

When transistors are in their linear regime current-voltage characteristic of the transistor is follows;

$$I_{DS} = \mu_n c_{ox} \frac{W}{L}(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2, \quad (2.1)$$

where μ_n is permeability constant, c_{ox} is gate oxide capacitance of the transistor per unit area, V_T is threshold voltage, V_{GS} is gate source voltage of the transistor, V_{DS} is drain source voltage of the transistor.

Drain to source voltages of switch FETs are negligibly small, providing the opportunity to model a transistor as a resistor with the resistance;

$$R_{DS} = \frac{1}{\mu_n c_{ox} \frac{W}{L}(V_{GS} - V_T)}, \quad (2.2)$$

When a gate control voltage below pinch-off value of the transistor is applied, internal capacitances, namely c_{gd}, c_{gs}, c_{gb}, c_{bs} get dominant and the transistor can be modelled as an off capacitor, as illustrated in Figure 2.6.

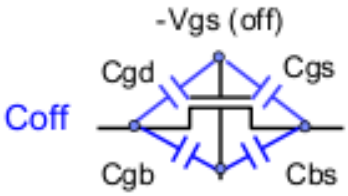


Figure 2.6. Internal Capacitances of a Transistor

Impedance of a capacitance is;

$$Z_C = \frac{1}{\mathrm{j}\omega \mathrm{c}} \tag{2.3}$$

where ω is defined as rational frequency which is equal to 2π times the operating frequency.

2.2.2. Switch Core with Quarter Wave Transmission Line

For a transmission line which is loaded with some impedance Z_L where Z_L is different than the characteristic impedance Z_0, the wave will be reflected from load to source, leading change in input impedance.

For a line of length *l*, the resultant input impedance of the transmission line, Z_{in}, can be expressed as;

$$Z_{in} = Z_0 \frac{Z_L + Z_0 \tanh(\gamma l)}{Z_0 + Z_L \tanh(\gamma l)}, \tag{2.4}$$

where γ is the line propagation constant.
For lossless line;

$$Z_{in} = Z_0 \frac{Z_L + iZ_0 \tan(\beta l)}{Z_0 + iZ_L \tan(\beta l)}, \tag{2.5}$$

β is the same as the angular wavenumber and can be expressed as;

$$\beta = \frac{2\pi}{\lambda}, \tag{2.6}$$

For quarter wavelength transmission line where $l=\lambda/4$,

$$\beta l = \frac{\pi}{2}, \tag{2.7}$$

The resultant Z_{in} is than;

$$Z_{in} = \lim_{\beta l \to \pi/2} Z_0 \frac{Z_L + iZ_0 \tan(\beta l)}{Z_0 + iZ_L \tan(\beta l)} = Z_0 \frac{iZ_0}{iZ_L} = \frac{Z_0^2}{Z_L}, \tag{2.8}$$

Therefore; as Z_L approaches to infinity (open load), Z_{in} approaches to zero (short circuit), and vice versa.

Quarter wavelength transmission lines have 90 degrees of phase length, and while drawing on Smith chart for S_{11} and S_{22}, they introduce 180 degrees of phase shift.

2.3. Important Switch Parameters

2.3.1. Scattering Parameters (s-Parameters)

For multi-port networks s-parameters define RF energy propagation. For a 2-port system the power diagram is as in Figure 2.7.

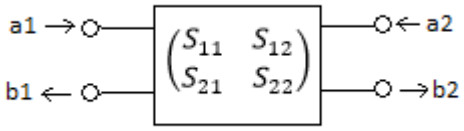


Figure 2.7. 2-Port System Expressing Energy Flow

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \cdot \begin{pmatrix} a_1 \\ a_2 \end{pmatrix}, \tag{2.9}$$

where a_1, a_2, b_1, b_2 are called complex travelling waves.

$$b_1 = S_{11}.a_1 + S_{12}.a_2 \tag{2.10}$$

$$\text{If } a_2 = 0;\ S_{11} = b_1/a_1$$

$$b_2 = S_{21}.a_1 + S_{22}.a_2 \tag{2.11}$$

If $a_2 = 0;\ S_{21} = b_2/a_1$

2.3.2. Insertion Loss (IL)

In the ON-state of the switch, the signal is mostly transmitted through the switch with some small absorption and reflection. The insertion loss may be defined as the ratio of the transmitted power to the difference between the incident and reflected power. If the reflected power is negligibly low then S_{21} can express the insertion loss.

Insertion loss is caused by the resistive characteristics of series element of switch that can be transistor, quarter wave transmission line etc. If the switching device is characterized by a small resistance in ON-state, insertion loss of the device can be expressed as [27];

$$S_{21} = \frac{Z_0}{R_{on} + Z_0} \tag{2.12}$$

Ideally $R_{on} = 0$ and S_{21}=1. For the switches that uses transistors as series elements, switch insertion loss is a function of R_{DS}. Since on resistance of a transistor is inversely proportional with the width of the transistor, using transistors with larger gate widths decreases insertion loss up to a width value where the effect of intrinsic capacitances (C_{GS}) become realizable for insertion loss. After that gate width value, IL turns out to be proportional with the gate width of the transistor.

2.3.3. Isolation

When the switch is OFF, most of the incoming signal is reflected as a small part of the signal is transmitted through the switch. Isolation defines the attenuation of the input power that is received at the output port when the switch is in its OFF state. Isolation level of a switch is an indicator to understand how successfully the switch is turned OFF. Ideally no leakage signal should exist at the output port when switch is OFF. Isolation is generally expressed in decibels (dB). For FET based switches, isolation is degraded with increasing C_{off} of the series element of the switch.

2.3.4. R_{on} . C_{off} Product

Desire of lower resistance at ON-state, and higher impedance at OFF-state lead to the concept of figure of merit. The ratio of ON impedance to OFF impedance may be used to characterize a switch.

$$\frac{Z_{on}}{Z_{off}} = \frac{R_{on}}{1/jwC_{off}} = jwR_{on}C_{off} \tag{2.13}$$

Figure of merit is the $R_{on}.C_{off}$ product for switches, which result in seconds. A smaller FOM is better since it means low ON-resistance compared to high OFF-state impedance. FOM is a technology-dependent parameter. FOM of the small volume material illustrated in Figure 2.8 can be extracted by calculating the capacitance and resistance of the material with resistivity of ρ, and dielectric constant of ε_r.

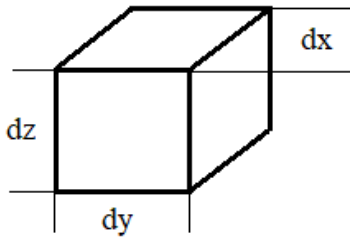


Figure 2.8. An element of the active area of a semiconductor

The capacitance of the material is $C = \varepsilon_r\varepsilon_0 dxdy/dz$, and the resistance is $R = \rho dz/dxdy$. FOM is then;

$$R.C = \rho\frac{dz}{dx.dy}\varepsilon_0\varepsilon_r\frac{dx.dy}{dz} = \rho\varepsilon_0\varepsilon_r \tag{2.14}$$

Thus; it can be stated that $R_{on}.C_{off}$ is a technology dependent metric which is based on the basic material properties of dielectric constant and resistivity. However, experimental values may be higher due to contact resistance and fringing fields.

The reciprocal of the product determines the upper frequency response limit of the technology. Technologies with smaller FOM values can achieve higher operational frequencies. This comparison can be both among different switching technologies such as FET, PIN and MEMS and within a technology such as 0.25 µm and 0.15 µm

GaAs pHEMT. $R_{on}.C_{off}$ products for different devices are illustrated in Table 2.1. PIN diodes have high frequency advantage over HEMTs as depicted in the table. Better $R_{on}.C_{off}$ product means better small signal switch, however this parameter does not hold power capability information of the technology.

Table 2.1 *Figure of Merit for Various Switch Technologies*

Process	R_{on} (Ω-mm)	C_{off} (fF/mm)	$R_{on}*C_{off}$ (fs)
0.18 thick film SOI	1.9	255	485
0.18 thin film SOI	0.81	310	250
GaAs PHEMT	1.4	160	224
GaAs PIN Diode	1.7	50	85
Silicon PIN Diode	1.7	50	85

2.3.5. Voltage Standing Wave Ratio (VSWR)

Voltage standing wave ratio (VSWR) of a switch defines how effectively the ports of the switch is matched to the load. In case of impedance mismatch between the load and the port, all of the power of the signal cannot be transferred to the load and some of the power is reflected back. Generally, RF systems are 50 Ω systems. Therefore; the impedance of the switch arms should be as close as 50 Ω. Ideal value of the VSWR is 1:1, and increases as the mismatch gets more evident.

In terms of VSWR values of the switch ports that are in OFF state, there are two types of switches, namely absorptive and reflective switch. For reflective switches the ports in OFF state are not matched to 50 Ω, having a high VSWR ratio. On the other hand, absorptive switches should have well matched ports to the loads regardless of the switch mode.

2.3.6. Return Loss

In addition to VSWR, another parameter to express impedance mismatch is return loss. Return loss is the amount of the reflected power with regard to incident power of a port, which is expressed in decibels.

2.3.7. Power Handling

Power handling capability defines the amount of power the device can handle with no performance degradation. Power is commonly expressed in dBm.

Since it has the greatest bandgap among semiconductors, GaN is the most appropriate technology for high power applications. For the technologies which have lower transistor breakdown voltages than they have to face when they are in OFF state, stacking the transistors may be a solution. Stacking means connecting the transistors in series to divide the voltage among the FETs. If the gate widths of the transistor are carefully adjusted, voltage on each transistor will be equal. While increasing power handling at OFF state, stacking of transistors introduce multiplied R_{on} to the circuit which will cause increase in insertion loss. Therefore; GaN technology offers another advantage with its high breakdown voltage.

2.3.8. Linearity

Ideally, linear systems should not include signals at different frequencies than the input signal frequency at their outputs. On the other hand, it is not much possible since nearly all components used in the circuit design brings some nonlinearity terms with them. 1-dB compression point (P1dB) and third order intercept point (IP3) are two important parameters for linearity. Both two criteria will be investigated for this work in the following sections.

By using memoryless Volterra series, input-output relationship or transfer characteristics of a device can be expressed by using (2.15).

$$y(t) = a_0 + a_1 x(t) + a_2 x(t)^2 + a_3 x(t)^3, \quad (2.15)$$

Higher order terms are not included for simplification.

2.3.8.1. Intermodulation Distortion (Third Order Intercept)

In case of two-tone input signal is applied, where

$$x(t) = A_1 \cos\omega_1 t + A_2 \cos\omega_2 t, \quad (2.16)$$

Then, the output signal can be expressed as

$$y(t) = a_0 + a_1(A_1\, cos\, \omega_1 t + A_2\, cos\, \omega_2 t) + a_2(A_1\, cos\, \omega_1 t + A_2\, cos\, \omega_2 t)^2 + a_3(A_1\, cos\, \omega_1 t + A_2 cos\, \omega_2 t)^3, \quad (2.17)$$

The intermodulation products $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ are in interest because of existing in operational frequencies and hence hard to be filtered out. Frequency spectrum which includes main tones and intermodulation terms are depicted in Figure 2.9.

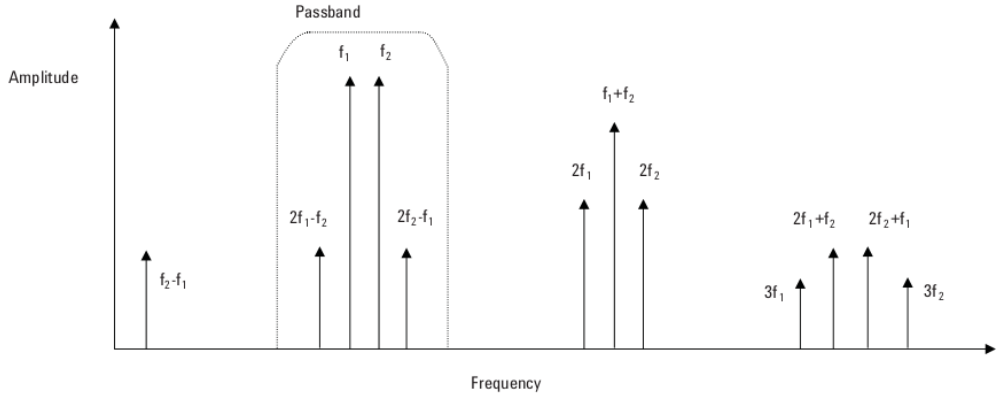


Figure 2.9. Intermodulation Terms for 2-Tone Signal

The coefficients of $\cos(2\omega_1 - \omega)t$ and $\cos(2\omega_2 - \omega_1)t$ are; $\frac{3a_3A_1^2A_2}{4}$ and $\frac{a_3A_1A_2^2}{4}$.

If $A_1 = A_2 = A$;

the fundamental signals grow by A, but the intermodulation terms grow with A^3 as input power increases.

There is a risk of domination by third order product term at the output which grows three times of the growth of the fundamental signal in terms of dB. Output power behavior of desired signal and third order intermodulation product under increasing input power is given in Figure 2.10. The input power level where fundamental term and IM3 interception occurs is input third order intercept point (IIP_3), whereas the corresponding output power level is called output third order intercept point (OIP_3).

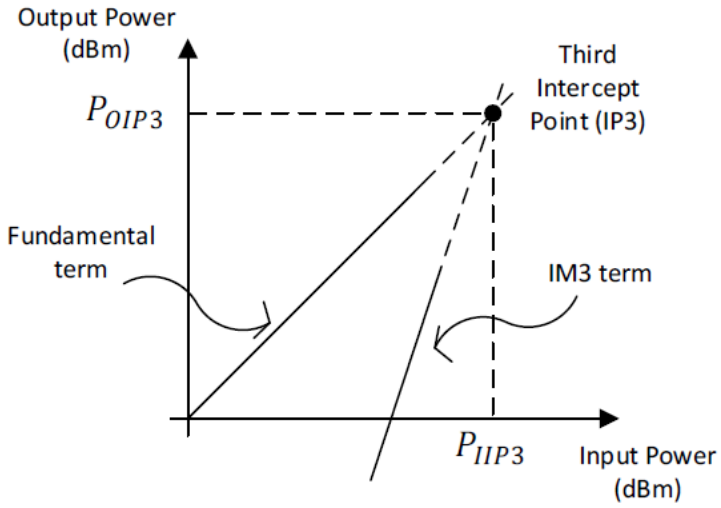


Figure 2.10. Growth Rate of Desired Signal and IM3 Products as Input Power Increases

2.3.8.2. 1-dB Compression Point (P1dB)

P1dB is the input power level where main output signal is 1 dB compressed compared to the desired signal as explained in Figure 2.11.

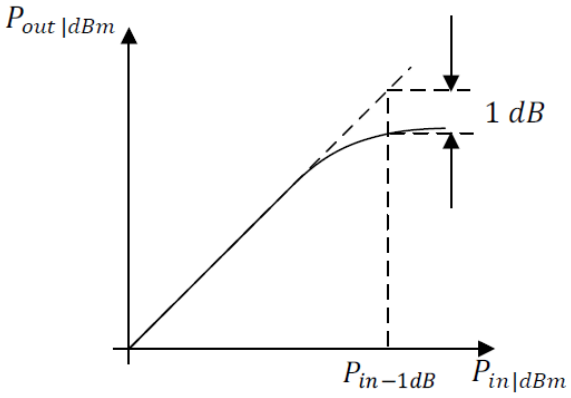


Figure 2.11. Output 1 dB Compression Point

Assuming 1-tone input signal is in the form

$$x(t) = A\,cos\omega t \tag{2.18}$$

$$y(t) = a_1 A cos\omega t + a_2 A^2 cos^2 \omega t + a_3 A^3 cos^3 \omega t, \tag{2.19}$$

$$y(t) = \frac{a_2 A^2}{2} + \left(a_1 A + \frac{3a_3 A^3}{4}\right)\cos\omega t + \frac{a_2 A^2}{2} cos2\omega t + \frac{a_3 A^3}{4} cos3\omega t, \tag{2.20}$$

If a_1 and a_3 have opposite signs, than $\frac{3a_3 A^3}{4}$ shows a compressive characteristics for fundamental signal. Input 1-dB compression point occurs at;

$$20\log\left|a_1 + \frac{3}{4}a_3 A_{in,1dB}^2\right| = 20\log|a_1| - 1dB \tag{2.21}$$

$$A_{in,dB} = \sqrt{0.145\left|\frac{a_1}{a_3}\right|} \tag{2.22}$$

CHAPTER 3

SWITCH DESIGN

3.1. Why GaN? (Technology Comparison)

Components that are used to design switches can be constructed from numerous materials such as silicon (Si), gallium arsenide (GaAs), indium gallium arsenide (InGaAs), indium phosphide (InP), and gallium nitride (GaN). GaN technology is the most appropriate one for high power usage among the other technologies. GaN technology offers higher breakdown voltages and higher current capability for transistors [16]. The reason why GaN transistors can withstand higher voltages is the wide bandgap, 3.4 eV, of this material. To compare, GaAs and Si have bandgap of 1.4 eV and 1.1 eV, respectively [17].

Table 3.1. *Comparison of Switch Technologies [18]*

Device	**PIN Diode**		**MESFET/ HEMT**	**HEMT**	**CMOS**
Technology	Si	GaAs	GaAs	GaN/SiC	Si
Insertion Loss	Low	Moderate	Moderate	Moderate	High
Isolation	Good	Good	Excellent	Good	Good
Bandwidth	Narrow	Narrow	Ultrabroad	Broadband	Broadband
Power handling	Very high	Moderate	Moderate	High	Low
Switching speed	Low	High	Very high	High	High
Power consumption	High	High	Low	Moderate (high power); Low (low power)	Low
Integration capability	Limited	Good	Good	Good	Excellent
Size	Large	Small	Small	Very small	Very small

Comparison of switch technologies based on basic switch parameters are given in Table 3.1.

High saturation velocity of electrons on GaN means higher current density when combined with the large charge capability. RF power is proportional to the current and voltage swings at load, thus, proportional maximum saturated current and the breakdown voltage of the device. Unlike PIN diode switches, HEMT devices operate with no DC power consumption. DC power consumption is present for PIN diode switches while the diodes are conducting.

Another reason for choosing GaN is the aim of producing a fully integrated transceiver module including power amplifier and low noise amplifier in addition to single pole double throw switch, working in X-band (8-12 GHz). The single pole double throw switch provides signal transmission between antennas and transmit/receive paths. Since the switch has 25 Watts of input power which is output of the power amplifier, power handling is an important parameter for design. Recent developments on GaN technology made it the technology of choice for building high power amplifiers [19]. Moreover, thanks to its wide bandgap, it has been shown that very robust low noise amplifiers (LNA) can be built on GaN substrates that can achieve noise figure values comparable to their GaAs counterparts [20]. These developments made it possible to create fully integrated high power/low noise transceivers which are area and cost efficient.

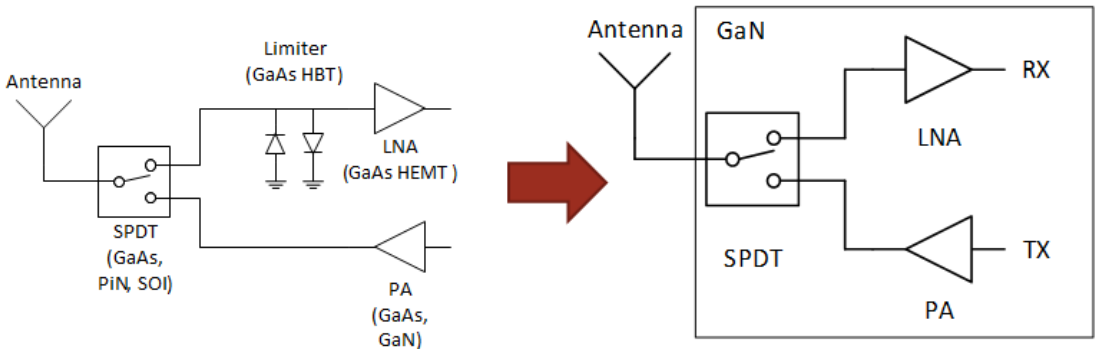


Figure 3.1. Simplification of Transceiver Diagram When Built on GaN

When low noise amplifiers are built on Gallium Arsenide substrate, the design gets more complicated with the need of using additional limiters as depicted in Figure 3.1.

3.2. Technology Overview

The switches have been designed on NP25-00 technology provided by WIN Semiconductors. The technology is based on a 0.25 µm gate length process on 4'' (100 µm) GaN on SiC substrates. A representative cross-sectional view of HEMT and passive components is presented in Figure 3.2.

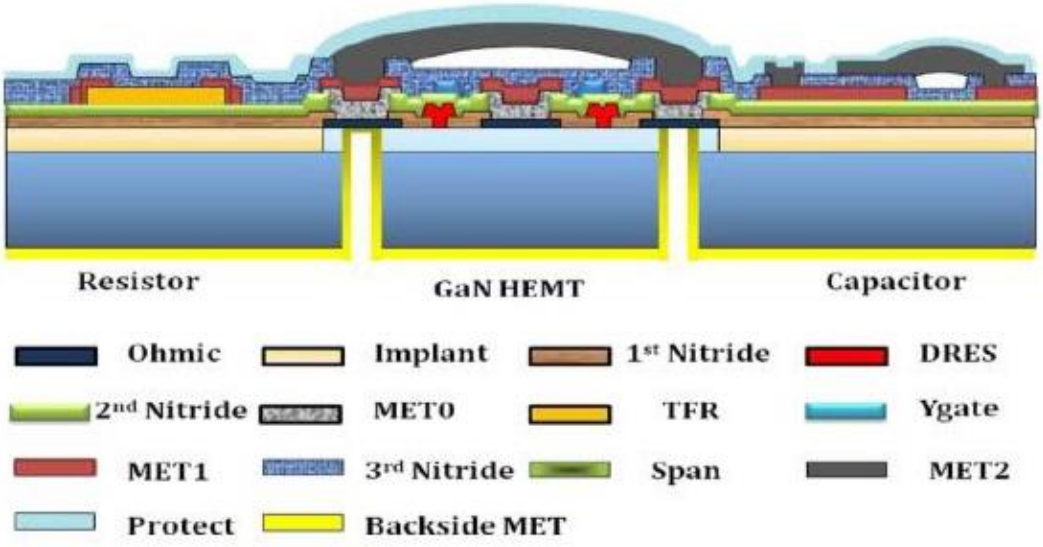


Figure 3.2. Cross Sectional View of HEMTs and Passive Components [21]

AlGaN barrier layer isolates the gate and the channel so that very low current flows between the channel and the gate. The channel is the region where electrons flow from source to drain. The channel is made of high quality GaN with a large mobility and a high saturation velocity, providing high current capability. The substrate provides heat spreading, mechanical support, and electromagnetic confinement. For GaN FETs, two candidates for substrate are Si or SiC. The thermal conductivity of SiC is three times

higher than that of Si [17]. For high power density applications SiC is the substrate of choice due to its high thermal conductivity.

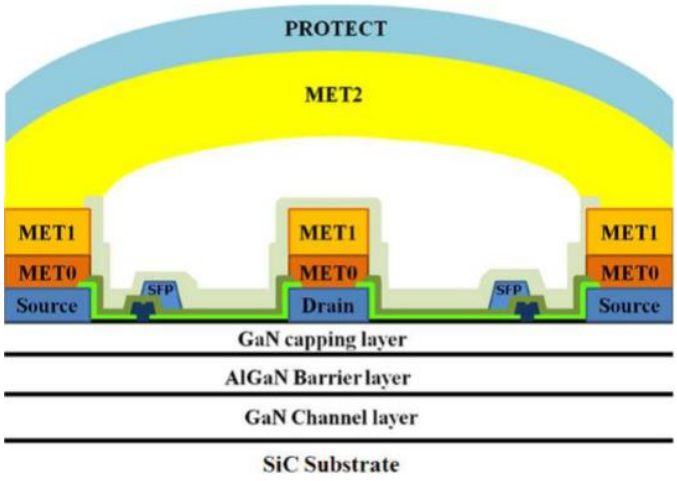


Figure 3.3. Simplified Cross Sectional View of HEMT Built on GaN on SiC Process

The GaN on SiC approach combines the high power density capabilities of GaN with the superior thermal conductivity and low RF losses of SiC [17]. Thanks to high thermal conductivity of GaN (about 330 W/mC, compared to nearly 145 W/mC for Si and 52 W/mC for GaAs), GaN FETs can dissipate more power with less increase in temperature. Figure 3.3 illustrates the cross-section of GaN transistor.

The layout of the passive components such as thin film resistor (TFR), round inductor, micro strip line, pad that are used during design phases are shown in Figure 3.4 (a), (b), (c), (d) [22].

Tantalum nitride (TaN) thin film resistors are typically used for biasing the transistors. They have approximately sheet resistance of 50 Ω/square.

Micro-strip lines consist of two metal layers, namely metal 1 and metal 2.

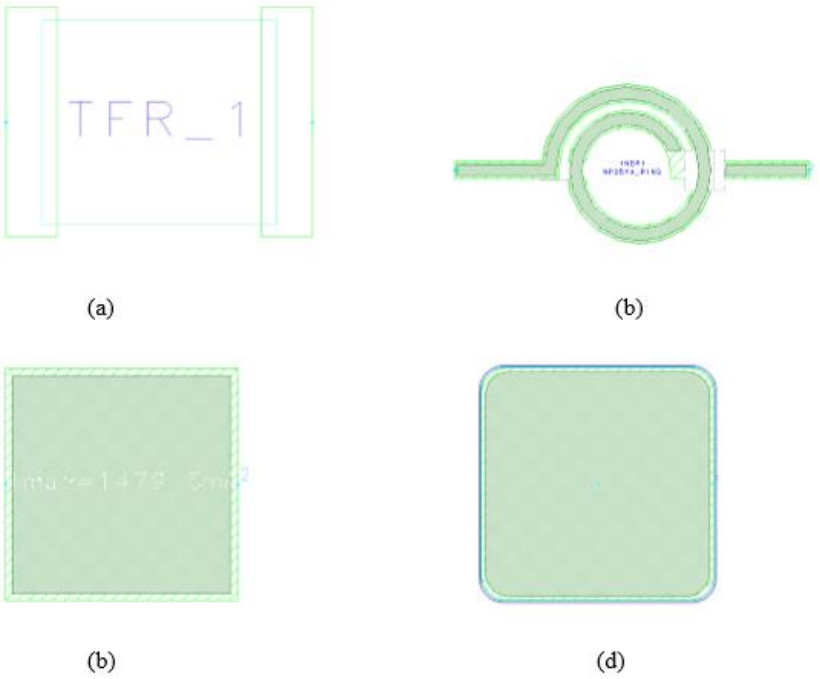


Figure 3.4. Layout of Passive Components: Thin Film Resistor (a), Round Inductor (b), Micro Strip Line (c), and Pad (d)

Table 3.2. *GaN HEMT Critical DC Parameters*

Parameters	**Units**	**Min**	**Nominal**	**Max**
Saturation Current, I_{DSS}	mA/mm	540	840	1140
Max Saturation Current, I_{dmax}	mA/mm	790	1040	1290
Threshold Voltage, V_{th}	V	-3.9	-2.9	-1.9
Cut-off Frequency, f_t	GHz	17	24.5	32
Turn-on Resistance, R_{on}	Ohm.mm	1.9	2.8	3.7

Table 3.2 defines critical parameters for GaN HEMT devices. Maximum saturation current is an important parameter for high power design which defines the maximum allowable current value that a transistor can handle. GaN technology offers high maximum saturation current values providing the opportunity to design high power circuits. Cut-off frequency defines the boundry where the energy of the system starts to be reduced rather than passing through. Maximum cut-off frequency (f_t) of the process is 24.5 GHz also provides a safe region for X-band (8-12 GHz) design.

3.3. Design Procedure and Environment

Design flow for RF integrated circuit (IC) starts with designing circuit with ideal components. If the simulation results meet the design goals, than the ideal elements are replaced by the corresponding process design kit (PDK) models, and layout is created. To investigate the effects of coupling caused by passive components, electromagnetic (EM) structure is obtained by extracting active device from the layout. The EM structure is electromagnetically simulated. If the EM simulation results are consistent with the design goals, layout versus schematic (LVS) check is performed to control how successfully the schematic and layout of the designs are matched. To investigate the compatibility of the design with the manufacturing rules, design rule check (DRC) is applied. If all the steps are successfully passed, the layout is sent to factory for production, which I called "tapeout". The products are measured to be compared with the simulation results.

In this thesis, the circuits are designed and simulated using Advanced Design System (ADS) software, EM simulations are performed by using a 2D electromagnetic solver provided by ADS. The switches are manufactured at the WIN Semiconductor fab, which is located at Taiwan. All of the simulation results in this thesis refer to results obtained from EM simulations.

3.4. Switch Configuration I

3.4.1. Design and Fabrication

For the switches which include transistors as series elements, most of the loss is caused by that series transistors. Increase in insertion loss with series FET element is more visible for AlGaN/GaN technology. This is because of the relatively high contact resistances of HFETs of AlGaN/GaN technology which introduce higher on-resistance to the design. Hence; as the series element of the switch, quarter wavelength transmission line has been depicted in order to achieve minimum insertion loss. For 50 Ω termination, width of the transmission line is set to 100 μm, and the length of

the transmission line for 10 GHz is calculated to be 2.94 mm.

Quarter wavelength transmission lines behave as short circuit when they are open loaded and as open circuit when loaded with short circuit. This behavior can be observed from Figure 3.5, where the transmission line is simulated with open and short circuit load from 10 MHz to 10 GHz.

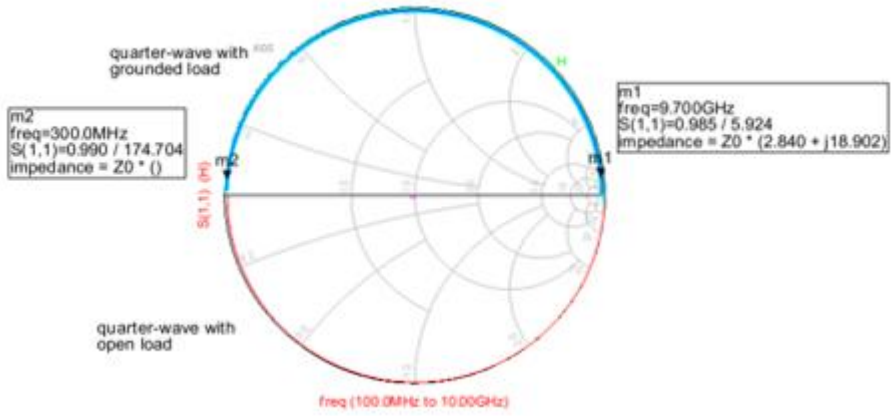


Figure 3.5. Quarter Wave Transmission Line Behavior

The quarter wavelength transmission lines are terminated with shunt transistors and thanks to high power handling capability of GaN devices, three shunt transistors was sufficient to achieve good linearity. The gate widths of the transistors are 9x100 µm, 5x100 µm and 3x100 µm.

Figure 3.6 presents the circuit topology of the first SPDT switch configuration which consist of quarter wavelength (λ/4) transmission line as series element and three transistors, with the gate widths of 9x100 µm, 5x100 µm and 3x100 µm, as shunt elements. In order the switch to work in desired manner on resistances should be low enough to introduce short-circuit behavior. Ron can be calculated by using (3.1) [23];

$$R_{on} = 2Z_0(10^{-\frac{S21(dB)}{20}} - 1) \tag{3.1}$$

By using the formula (3.1), the resistance values of the transistors with gate periphery 9x100 µm, 5x100 µm and 3x100 µm have been calculated as 3,64 Ω, 5.43 Ω and 8.26 Ω, respectively at 10 GHz. As they are used in parallel, required low resistance

values have been obtained to be 1.72 Ω. Corresponding resistance of the transmission line is calculated as 0.77 Ω for the middle of the band (10 GHz).

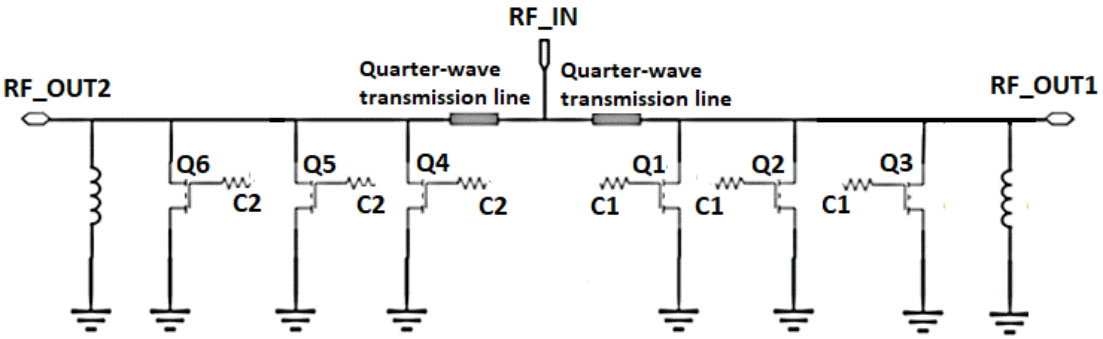


Figure 3.6. Circuit Schematics of Switch I

Since GaN transistors are depletion type devices, 0 Volt is appropriate to put the transistors in ON state.

The working principle of the switch is as follows; when the transistors of an arm are put into on-state by applying 0 V to the gates, the transistors behave as small valued shunt resistors, and consequently quarter wavelength transmission line can be dealt as open circuit [23]. While an output port has no receiving signal, the signal should flow through the other branch. Control voltage (-40V) below pinch-off is applied to the related transistors. This high turn-off voltage allows a high linearity in the transistor as any voltage swing across drain or source terminal will be coupled to gate ensuring the transistor is OFF even at the highest voltage swings [24]. When OFF capacitances are high enough, and thus transistors behave as open circuit, quarter wavelength transmission line allows the signal transmission to the related output port. Since the switch which is subject to this thesis deal with high power signals, the transistors should also withstand such high power levels and the voltages on each transistor should not exceed the breakdown voltage. The devices with relatively low breakdown voltages require stacked design configuration with active devices connected in series in order to divide the maximum voltage of input signal. However, this configuration brings some disadvantage with it as increase in insertion loss and complexity of the design. Thanks to the high breakdown voltage of GaN switch transistors, the required

voltage that a transistor should withstand for the related switch design is no higher than the breakdown voltage which is nearly 100 Volts. Therefore, the design can be simplified by using less transistors.

In addition to the voltage value on transistor when the transistor is OFF exceeding the breakdown voltage of the device, the destruction or degradation of performance of switch can also be caused by the RF drain current at on state exceeding maximum saturation current. For GaN on SiC process, Idss,max is given as 1200 mA/mm. Therefore; maximum current values that transistors can safely handle are calculated as 1080 mA, 600 mA, and 360 mA for transistors with gate widths 9x100 µm, 5x100 µm, and 3x100 µm, respectively. Figure 3.7 represents the current values on each transistor when the transistors are ON with no degradation in signals. To satisfy the power requirements harmonic balance simulations are performed.

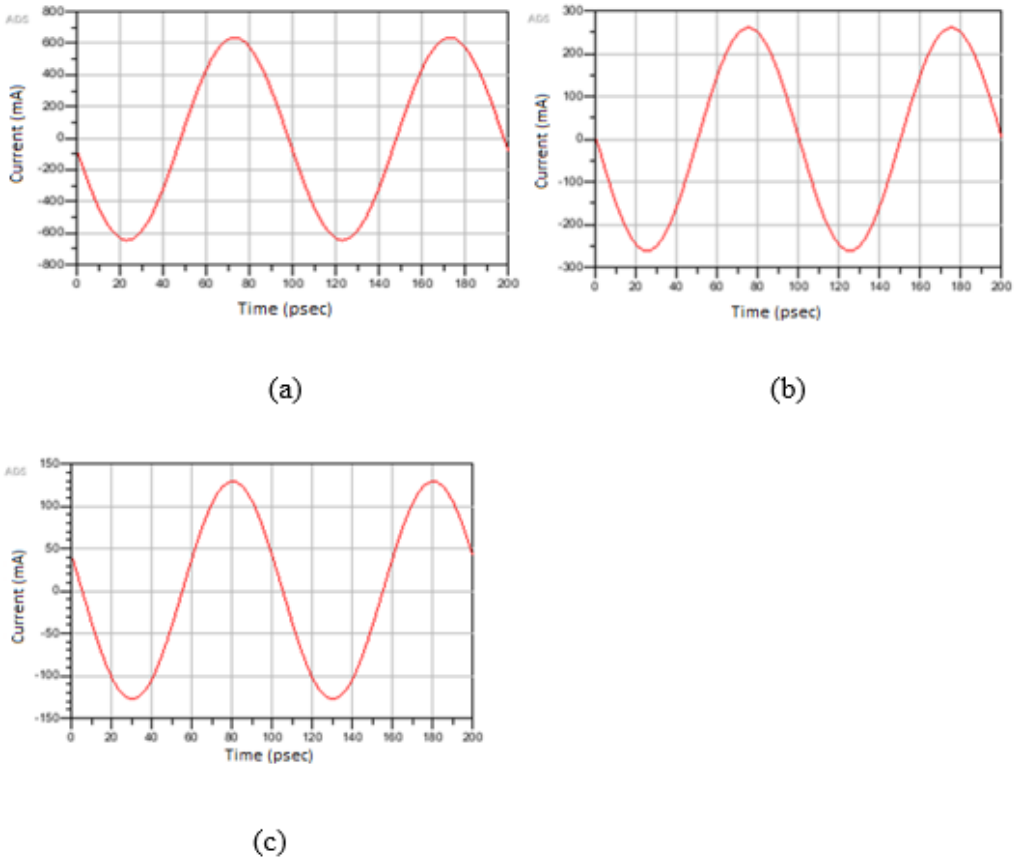


Figure 3.7. Current Values Passing Through Transistor Q1/Q4 (a), Q2/Q5 (b), and Q3/Q6 (c)

For series transmission line-shunt transistor switches, power handling capability is mostly dictated by gate control voltage which keeps the transistor in its OFF-state. When the transistor is OFF, maximum allowed voltage on transistor is;

$$V_{max} = V_b - V_P, \tag{3.2}$$

where V_b is the gate-drain breakdown voltage and V_p is the pinch-off voltage.

Maximum power handling of the switch in this state is;

$$P_{max} = \frac{V_{max}^2}{2Z_0}, \tag{3.3}$$

where Z_0 is the characteristic impedance of the system.

$$P_{max} = \frac{(V_b - V_p)^2}{2Z_0} \ [Watts]. \tag{3.4}$$

For the NP25-00 process, pinch of voltage of the transistors are nearly -2.9 Volts, and breakdown voltage of the transistors are 121 Volts, as stated in the handbook of the process [25]. To calculate maximum power handling of the switch by using formula (3.4), 153.51 Watts can be achieved as the maximum power that can be handled.

Transmission lines are composed of MET1 and MET2 layers, where MET2 is more capable for current handling. Maximum current density of MET2 layer is 8 mA/μm and 800 mA for 100 μm-transmission line.

In order a transistor to withstand high voltages the gate width should be widened. However, as the size of the transistor is increased, the effect of parasitic capacitances become more realizable. To overcome this problem, an inductor in parallel with the transistor can be used. When the transistor is ON, the inductor is in parallel with a small resistance, Ron, and inductor has no effect. For the OFF state of the transistor, it is parallel with parasitic capacitance resulting resonance at desired frequency.

Another solution to overcome high voltages for each transistor is transistor stacking for shunt transistors. By this method the voltage on the transistor is divided in multiple transistors by connecting one transistor's drain to another's source. The disadvantage of this method is the rise in the complexity of the design, and also increase in the dimensions of the circuit. Thanks to high breakdown voltage of the GaN transistors,

which is nearly 100 Volts, there is not any need to stack transistors which allows to achieve a simplified design.

A gate resistance is also included for each transistor in the design in order to isolate RF signal path and the control port from each other [19]. Isolation between RF signal paths and control ports is degraded for gate resistances below 1.5 – 2 kΩ. By careful tuning, 4 kΩ has been chosen as gate resistance value.

Layout of the switch includes back-via elements to provide ground connection through the wafer. The schematic view and the layout of the back-via is represented in Figure 3.8 (a), (b). The element behaves as a series combination of a small-valued resistor and an inductor. The equivalent circuit diagram of back-via in terms of inductive and resistive behavior is given in Figure 3.8 (c). In figure 3.8 (c), R_BV stands for back-via resistance and L_BV is for back-via inductance. Referring to the factory guide, R_BV is equal to 0.012 Ω and L_BV has an inductance value of 12 pH.

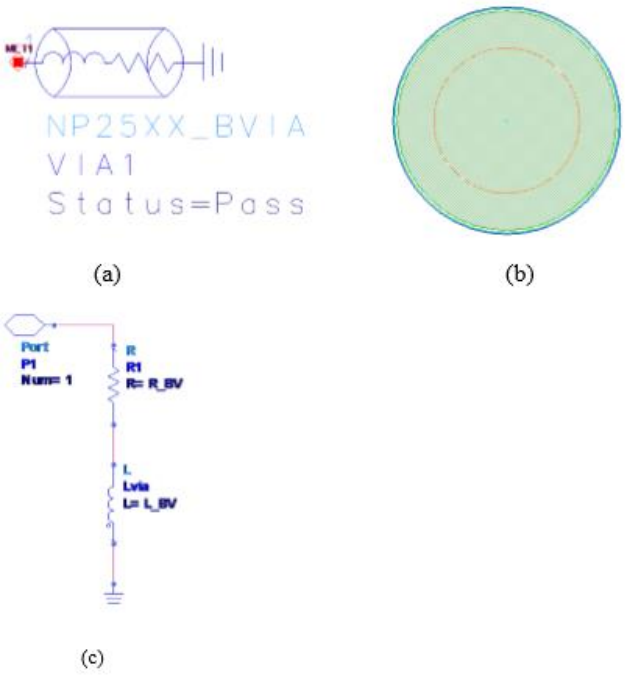


Figure 3.8. Schematic View (a), Layout (b), and Inductive and Resistive Behavior (c) of Via

Figure 3.9 and 3.10 show the layout of designed switch and photograph of the fabricated switch, respectively. The pads on north-south direction are the DC bias pads

which provide biasing for the transistors. Pad dimensions for DC bias pads are 100 µm x 100 µm, with center-to-center distance of 400 µm (because of probe availability). Two of the pads are devoted for DC biasing of two separate switch arms, whereas the other two pads are utilized for grounding. For RF signal pads which are set for ground-RF signal-ground combination for both 2 output ports and an input port, the pad dimensions are 200 µm x 100 µm for ground pads, where RF signal pads are 100 µm x 100 µm. The pads are 200 µm apart from each other. The die size of the switch is 2.9 x 2.1 mm^2.

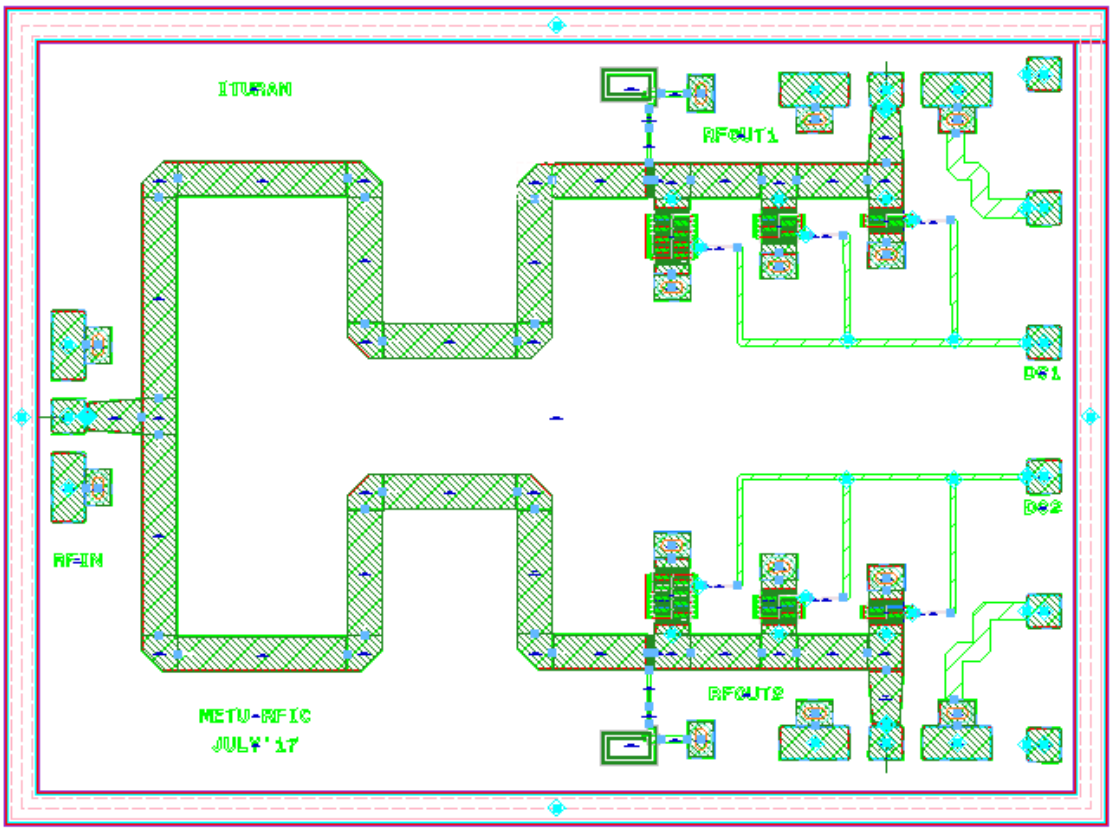


Figure 3.9. Layout of Switch I

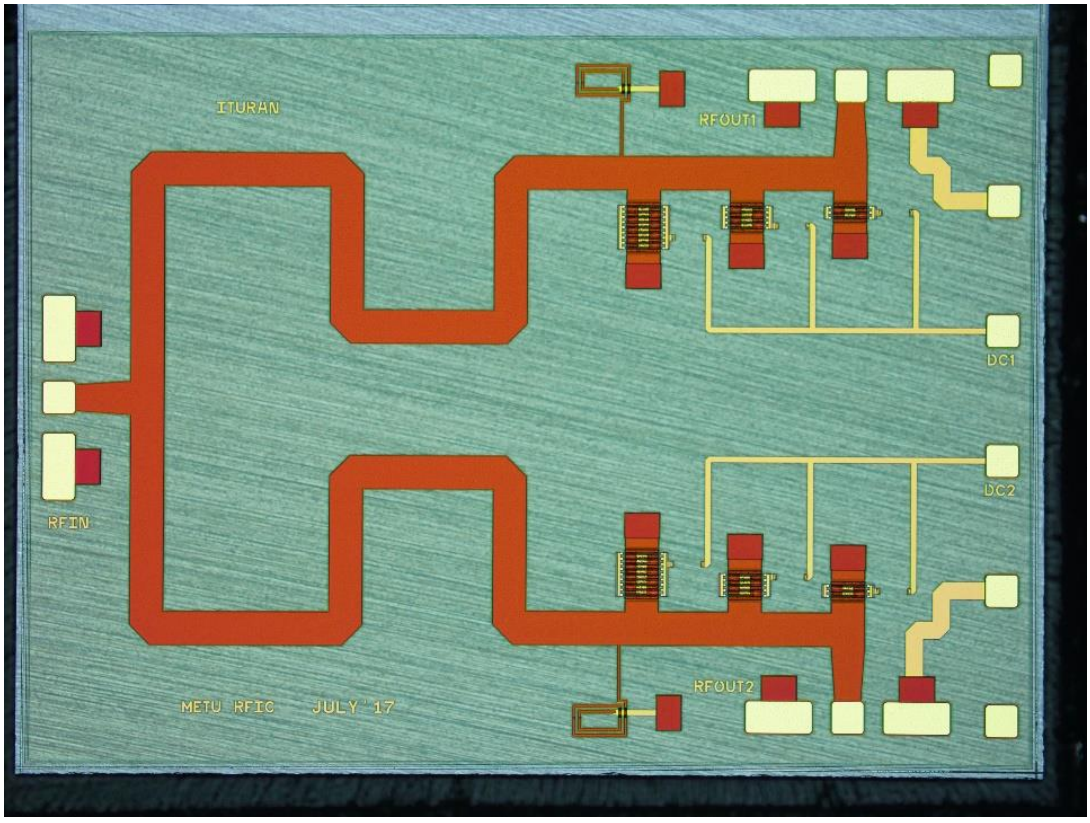


Figure 3.10. Die μphotograph of Fabricated Switch I

3.4.2. Simulation and Measurement

3.4.2.1. Small Signal Performance

After extracting the active components from the design the EM simulation is performed by using 2D electromagnetic solver provided by ADS. The EM-simulated part of the switch layout is depicted in Figure 3.11.

Four samples of the fabricated switch were measured to investigate s-parameters on probe station. The measurements are performed using calibrated probe station. Probe station allows to directly contact to the pads of the wafers by precisely positioned probes. Since printed circuit board (PCB) is not used during the measurement, the effects of wirebonds and the microstrip lines are eliminated. S-parameters of the dies are monitored via Agilent Network Analyzer (E3861A).

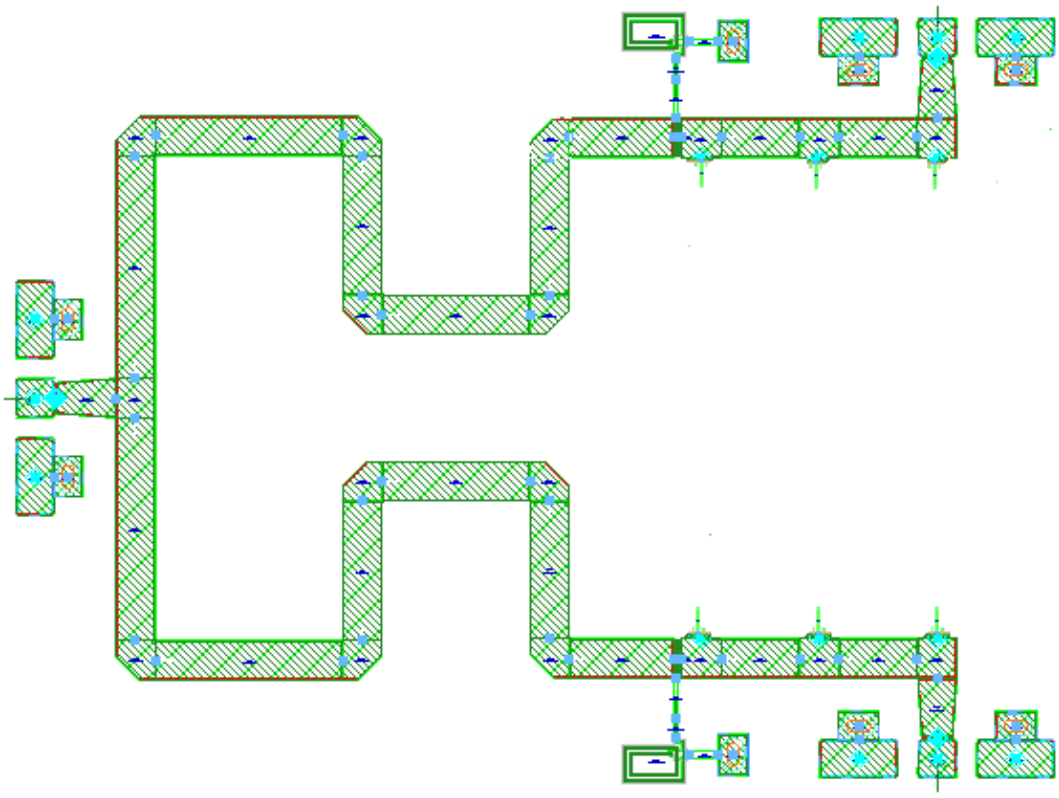


Figure 3.11. Layout of Switch I for EM Simulation

The comparison of EM simulation and measurement results for small signal parameters including insertion loss, isolation, and return loss for 7-13 GHz band are plotted in Figure 3.12, 3.13, and 3.14, respectively.

Measurement results are expected to be worse than the simulation results. However, as shown in Figure 3.12, measured insertion loss, which is nearly 0.3 dB, is much better than the simulation results. The root cause of this conflict is because of switch models used during simulation. Since the selected technology is still under development by the factory, the provided switch models are not recent enough to fully capture the performance of the latest switch transistors.

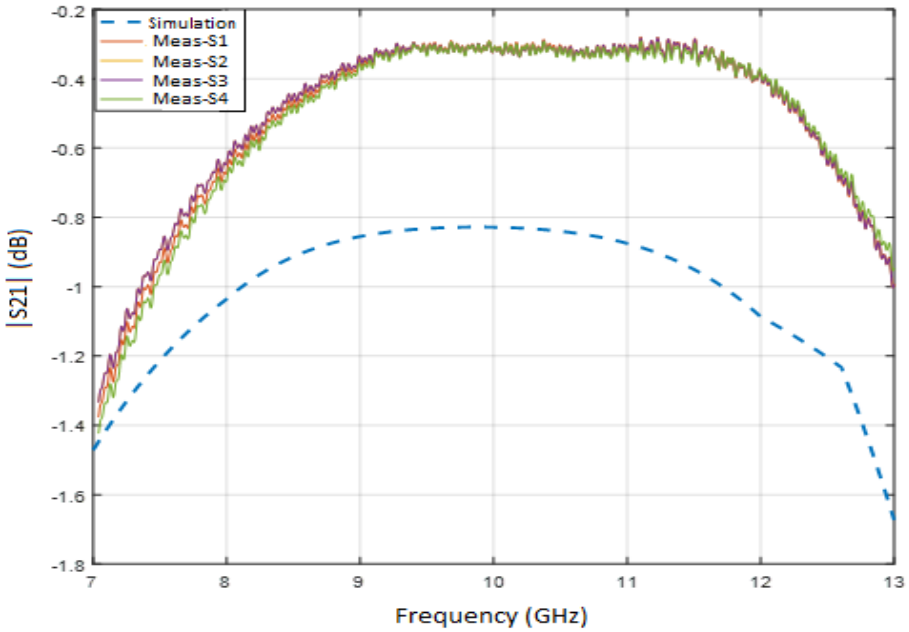


Figure 3.12. Simulated and Measured $|S_{21}|$ at On State

Another reason of the inconsistency may be inaccurate modelling of the circuit components. For insertion loss case of the switch, the transistors are OFF. Therefore; there exists only capacitive parasitic coming from transistor. On the other hand; λ/4 transmission line has certain loss due to its loss characteristic. Equivalent circuit diagram of the conducting branch of the switch is presented in Figure 3.13. R defines the resistance of the λ/4 transmission line, where C(Q1), C(Q2) and C(Q3) stand for parasitic capacitances of 0FF-state transistors.

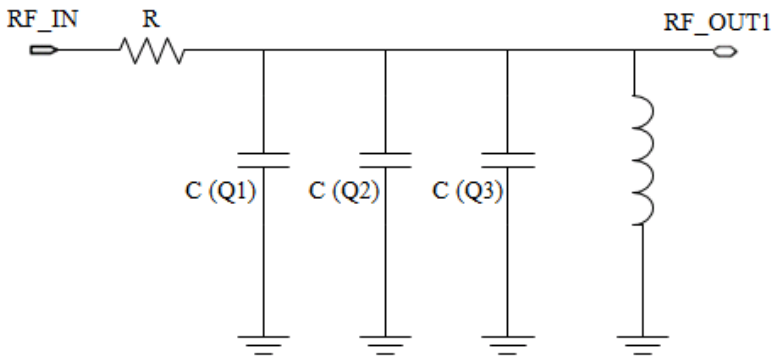


Figure 3.13. Equivalent Circuit Diagram of Conducting Branch

The inconsistency between simulation and measurement results may be caused by inexact modelling of the resistance of the transmission line and parasitic capacitance of transistors. The most likely parameter that can be inaccurately modelled is the resistance of transmission line, which can be effected from the skin-effect. At high frequencies current flowing in conductor tend to accumulate near the outer surface of the conductor. Skin depth is a distance measured from the outer surface of the conductor toward the center of the conductor in which the current density drops to 37% of its value at the surface [26]. Skin effect causes change in effective resistance of the conductor by changing the effective cross sectional area. Since resistance is inversely proportional with the cross sectional area, decrease in effective cross sectional area results in higher resistance. During insertion loss simulation, skin-effect may be exaggerated which resulted in higher resistance of the transmission line and increase in insertion loss. On the other hand; curve trends of simulation and measurement results are similar. Roll-offs, caused by capacitive components, occur at nearly same frequency ranges, which may prove accurate modelling of parasitic capacitances.

Comparison of simulation and measurement results for isolation is expressed in Fig. 3.14. Simulated isolation has been observed to be better than 31 dB, where the measurement results are better than 29 dB for the frequency band of interest. Both simulation and measurement results achieve 32 dB of isolation at nearly 10 GHz.

Impedance matching is crucial in systems which require high power handling, low noise figure, and maximum linearity. Simulated and measured return losses are presented in Fig. 3.15. Simulated and measured return losses are better than 13 dB for the frequency band of interest, demonstrating successfully matched ports to 50 Ω loads. The ripples at measurement lines are caused by connector defects occurred during calibration process.

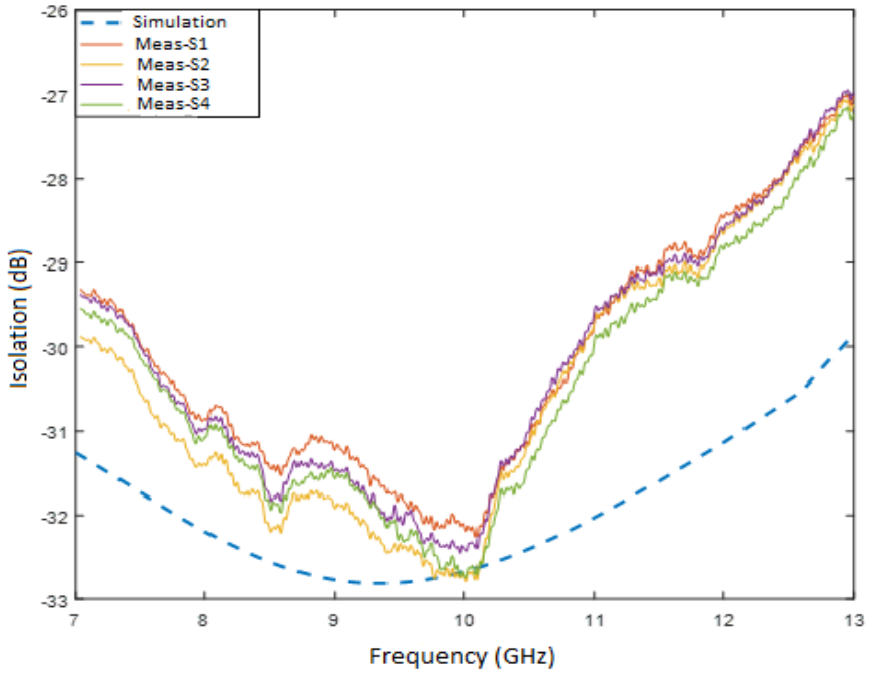


Figure 3.14. Simulated and Measured Isolation

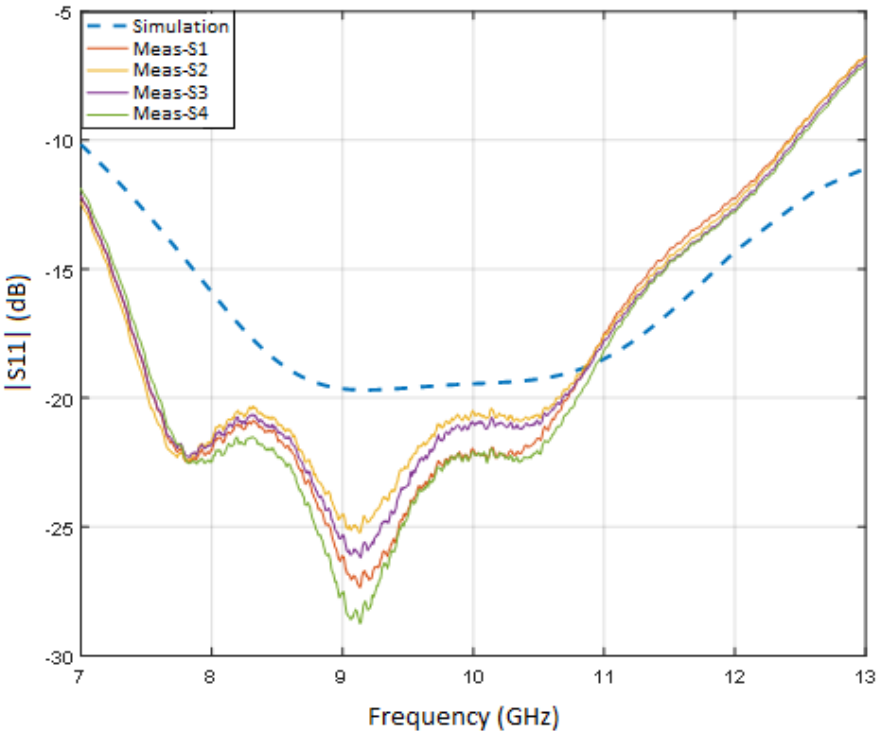


Figure 3.15. Simulated and Measured $|S_{11}|$

3.4.2.2. Large Signal Performance

Simulation of power handling and linearity could not be performed due to lack of large signal switch transistor models. To measure power handling and linearity performance of the switch, PCB was designed and fabricated. Evaluation PCB is required in order to transfer bias voltages and RF inputs to IC, and RF outputs to measurement devices. The layout of the designed evaluation PCB is presented in Figure 3.16. The PCB thickness is chosen to provide signal transmission with minimum attenuation. The fabricated PCB is a single layer PCB with 20 mil thick RO4003C material. With the given substrate thickness, a microstrip line width of 1.1 mm corresponds to a 50 Ω transmission line, which transmit the RF input signals to the RF input ports of the switch, and output signals to the measurement devices. For DC biasing of the gates of switch transistors supply rails are placed. For each supply rail, three shunt capacitors with 1 nF, 100 nF, and 1 µF capacitance are placed as decoupling capacitors. The photograph of the fabricated PCB, and the PCB with the switch die and three connectors are given in Fig. 3.17 (a), and (b). The connector located at the top of the photo is DC biasing, where the other connectors are for RF signal paths. As RF connectors, Southwest 2.92 mm end launch connector is used.

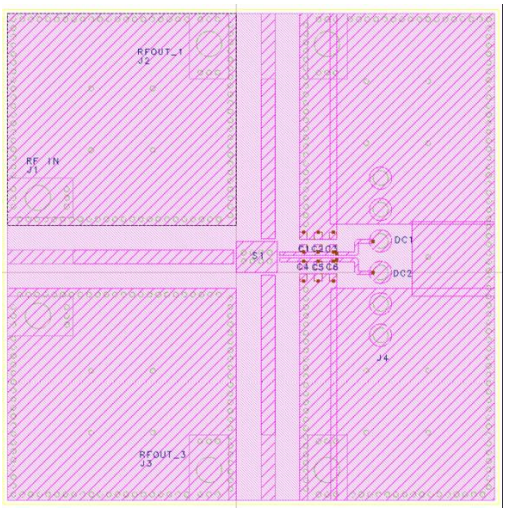
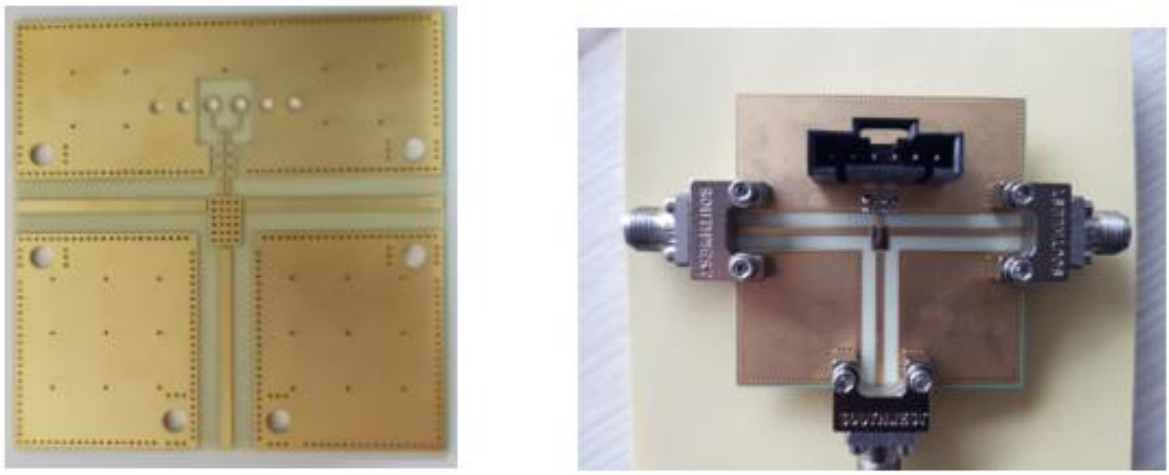


Figure 3.16. Layout of Designed Evaluation PCB



(a) (b)

Figure 3.17. Fabricated PCB (a), PCB with the Switch, and Connectors (b)

As input source of the switch a power amplifier fabricated using the same technology with the SPDT switch has been used. The output of the power amplifier is nearly 25 Watts, which is equal to 44 dBm. Hence; as stated before power handling is an important parameter for the design. Linearity is another concern for not to introduce any harmonic component to the system.

P1dB measurement is performed by using the setup given in Figure 3.18. Both switch configuration I and configuration II are investigated with the same setup which includes a signal generator, two amplifiers, the switch to be measured, an attenuator with 30 dB attenuation, and a spectrum analyzer. The amplifier symbolized with PA is the power amplifier that is fabricated with the same technology of the switches which are subject to this study. The signal generator produces an input signal at 10.6 GHz.

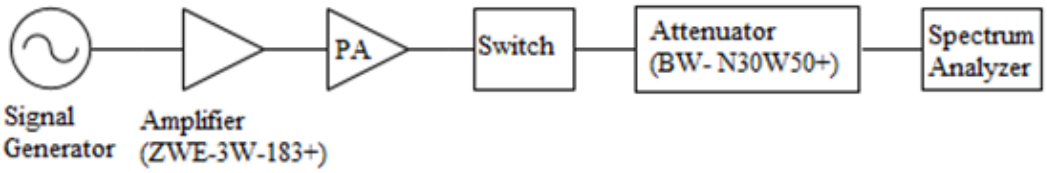


Figure 3.18. The Schematic of P1dB Measurement Setup

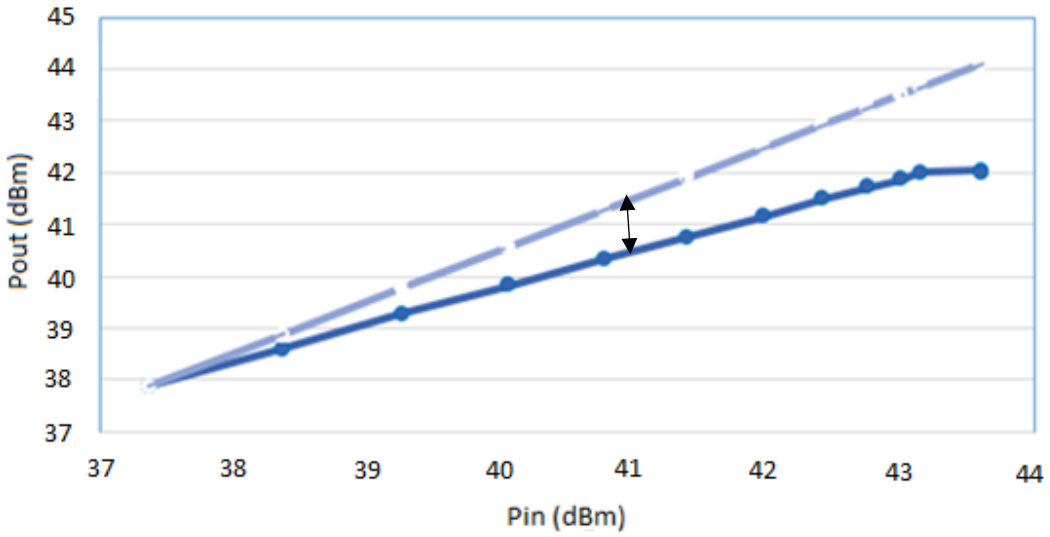


Figure 3.19. Measured Output Power versus Input Power

P1dB can be depicted from Pout-Pin graph illustrated in Figure 3.19 which was drawn taking the additional losses into consideration. Since the measurement setup includes a noncommercial power amplifier with relatively low linearity, measurement is limited with the linearity of the power amplifier. 1 dB compression point of the switch is measured nearly at 41 dBm of input power which is close to 1 dB compression of power amplifier, and so may not reflect the actual linearity of the switch.

3.5. Switch Configuration II

3.5.1. Design and Fabrication

Isolation is a critical concern for high power applications. Configuration II has been designed aiming to achieve high isolation. Two successive series transmission line-shunt transistor configuration have been included to design, venturing slight increase in insertion loss, and widened die area. Successive transmission line also improves insertion and isolation caused by reflection. Since the reactance of shunt switch may introduce mismatch and results in reflection, additional λ/4 transmission line helps to enhance the performance of the switch [23]. This configuration also provides low

insertion loss, because behavior of double series transmission line, shunt FET structure is closer to short circuit, which means open circuit at load.

Every transmission line is terminated with two transistors. The gate peripheries of the transistors are 9x100 µm, 5x100 µm, 3x100 µm, and 3x100 µm for Q1/Q5, Q2/Q6, Q3/Q7, and Q4/Q8, respectively. In order to decrease the loading effect of transistors caused by parasitic capacitances, the gate peripheries of the transistors are scaled down. The switch is symmetric and each two branches of the switch have identical components and therefore identical responses under identical conditions. Figure 3.20 illustrates the schematic of the switch.

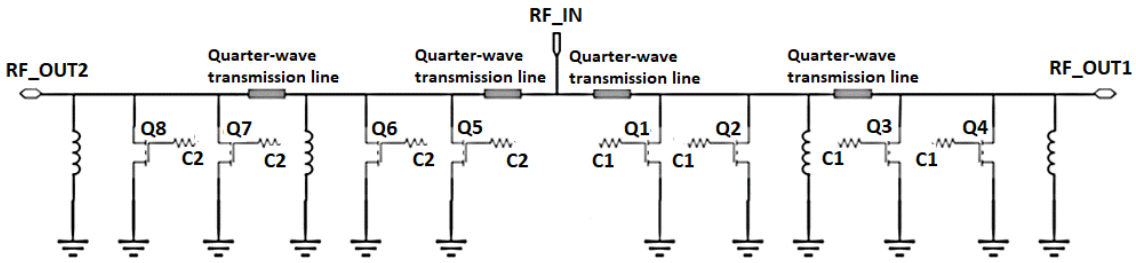


Figure 3.20. Schematic of Configuration II

By using the formula (3.1), the resistance values of the transistors with gate periphery 9x100 µm, 5x100 µm and 3x100 µm have been calculated as 3,64 Ω, 5.43 Ω and 8.26 Ω, respectively at 10 GHz. As they are used in parallel, required low resistance values have been obtained to be 2.18 Ω and 4.13 Ω. In order to obtain best response from the transmission line length and width of the transmission lines are carefully tuned. To provide successful synchronization with the 50 Ω termination, width is set to 100 µm.

For proper operation of the switch, RF drain current passing through transistors should not exceed maximum saturation current, $I_{dss,max}$, which is equal to 1200 mA/mm for GaN/SiC technology. Maximum current values that transistors can handle without degradation or destruction of performance are calculated as 1080 mA, 600 mA, 360 mA, and 360 mA, for transistors Q1/Q5, Q2/Q6, Q3/Q7, and Q4/Q8, respectively.

Figure 3.21 represents the current values on each transistor when the transistors are ON with no degradation in signals, all of the transistors are in safe operation region.

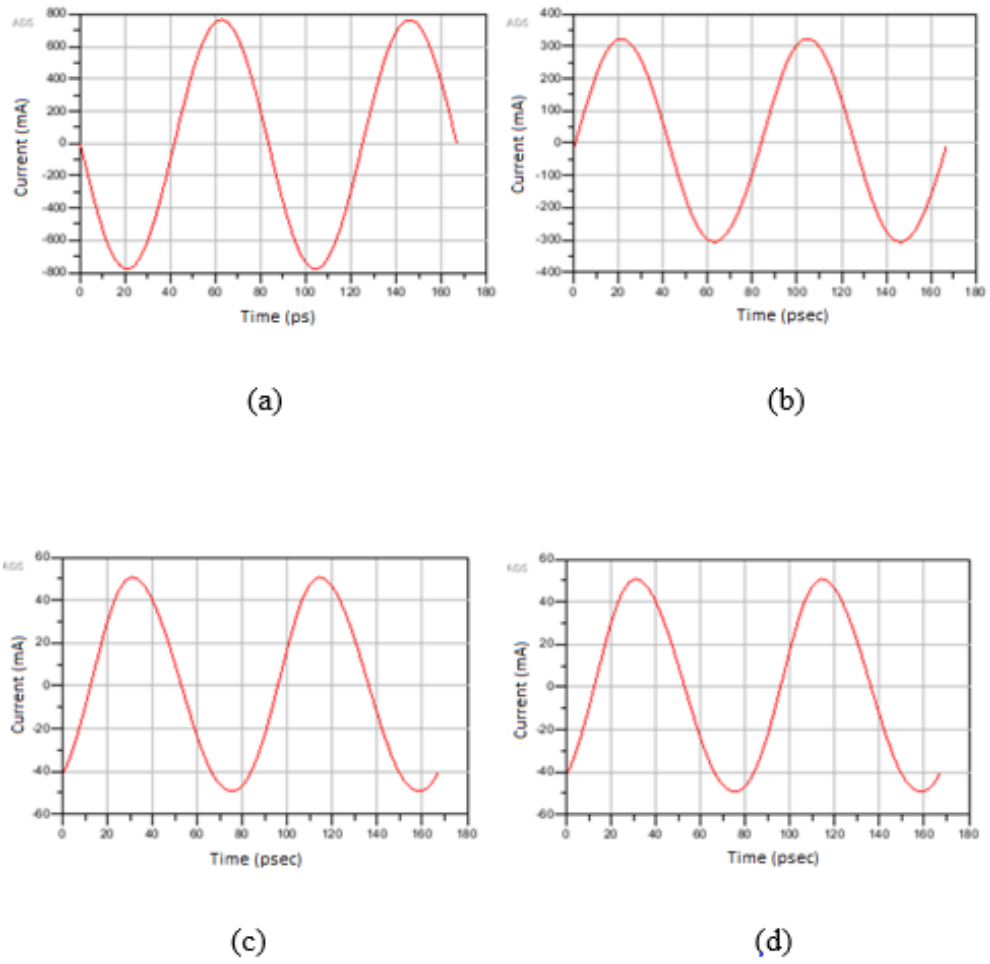


Figure 3.21. Current Values Passing Through Transistor Q1/Q5 (a), Q2/Q6 (b), Q3/Q7 (c), and Q4/Q8 (d)

Figure 3.22 and 3.23 show the layout of designed switch and photograph of the fabricated switch, respectively. Figure 3.24 illustrates isometric 3D view of the design. The pads on north-south direction are the DC bias pads which provide biasing for the transistors. Pad dimensions for DC bias pads are 100 µm x 100 µm, with center-to-center distance of 400 µm (because of probe availability). Two of the pads are devoted for DC biasing of two separate switch arms, whereas the other two pads are utilized for grounding. For RF signal pads which are set for ground-RF signal-ground

combination for both 2 output ports and an input port, the pad dimensions are 200 µm x 100 µm for ground pads, where RF signal pads are 100 µm x 100 µm. The pads are 200 µm apart from each other. The die size of the switch is 4.1 x 2.7 mm^2.

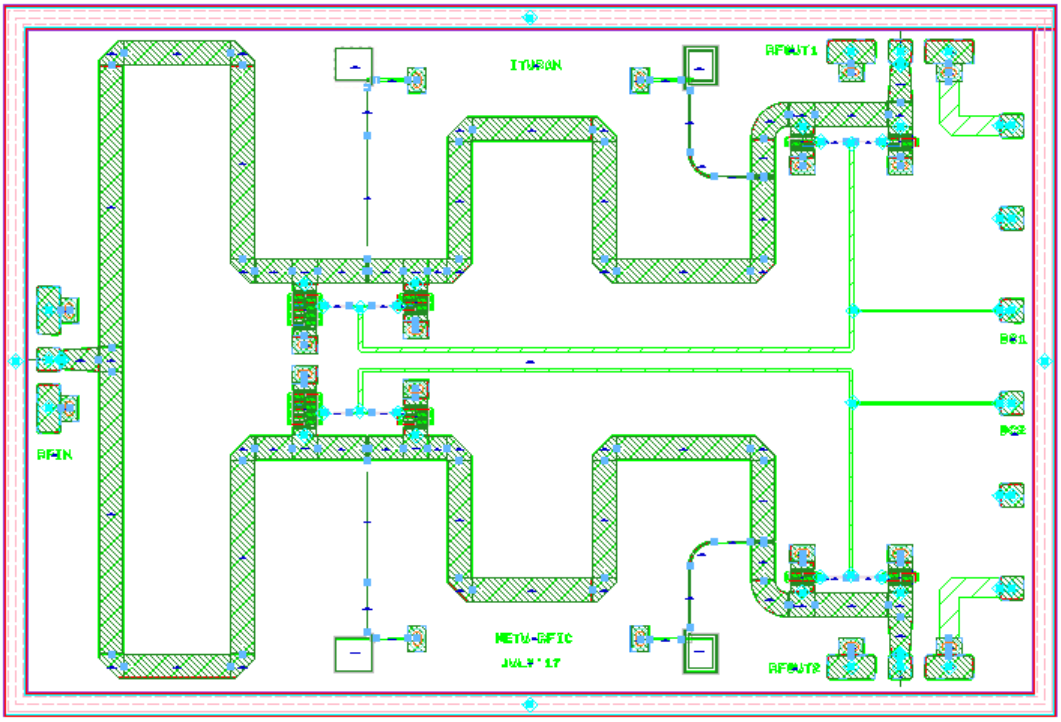


Figure 3.22. Layout of Switch II

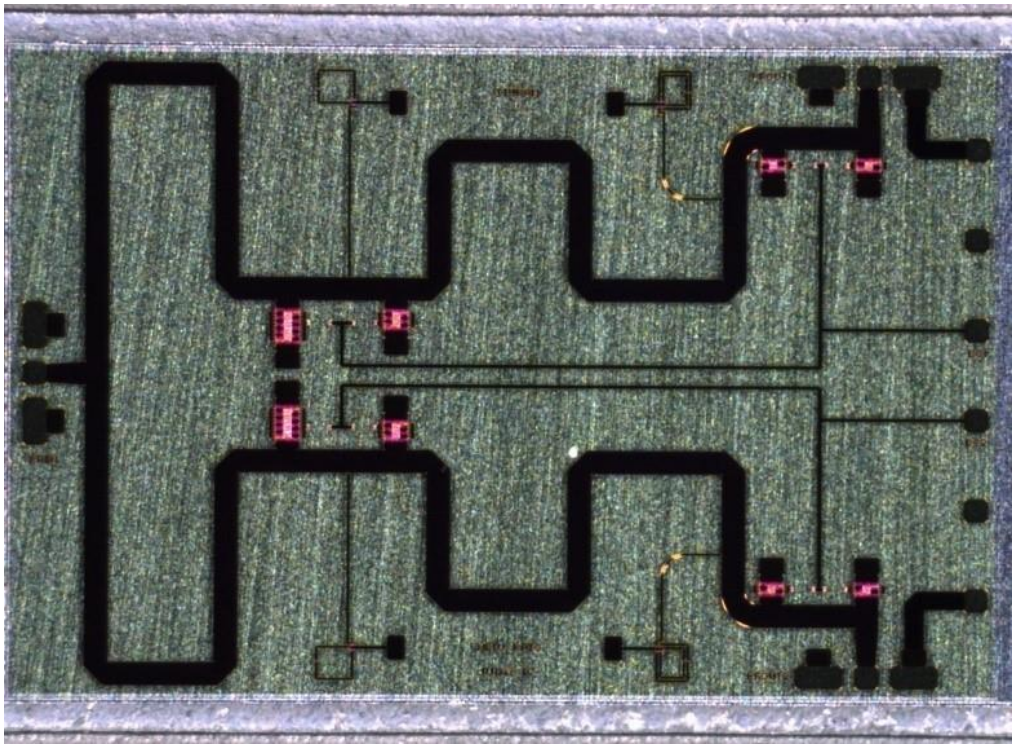


Figure 3.23. Die Photograph of the Fabricated Switch II

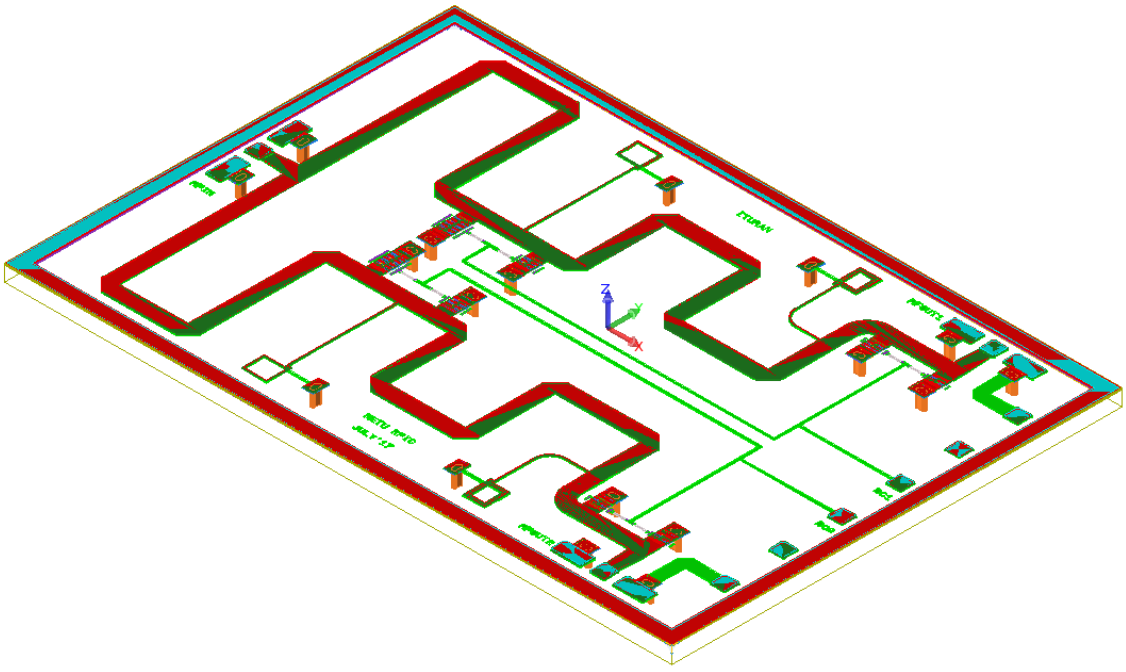


Figure 3.24. Isometric 3D View of Switch II

3.5.2. Simulation and Measurement

3.5.2.1. Small Signal Performance

EM simulation of the design has been performed by using 2D electromagnetic solver provided by ADS. Layout which has been under EM simulation is given in Figure 3.25. This layout is obtained by excluding active components of the circuit in order to determine the coupling effects of passive elements.

Four samples of the fabricated switch were measured to investigate s-parameters and power handling characteristics. Measured small-signal results for insertion loss, isolation, and return loss are plotted in comparison with simulation results in Fig. 3.26, Fig. 3.27, and Fig. 3.28, respectively. Insertion loss, isolation and return loss in both switch settings are same due to symmetrical layout of the switch.

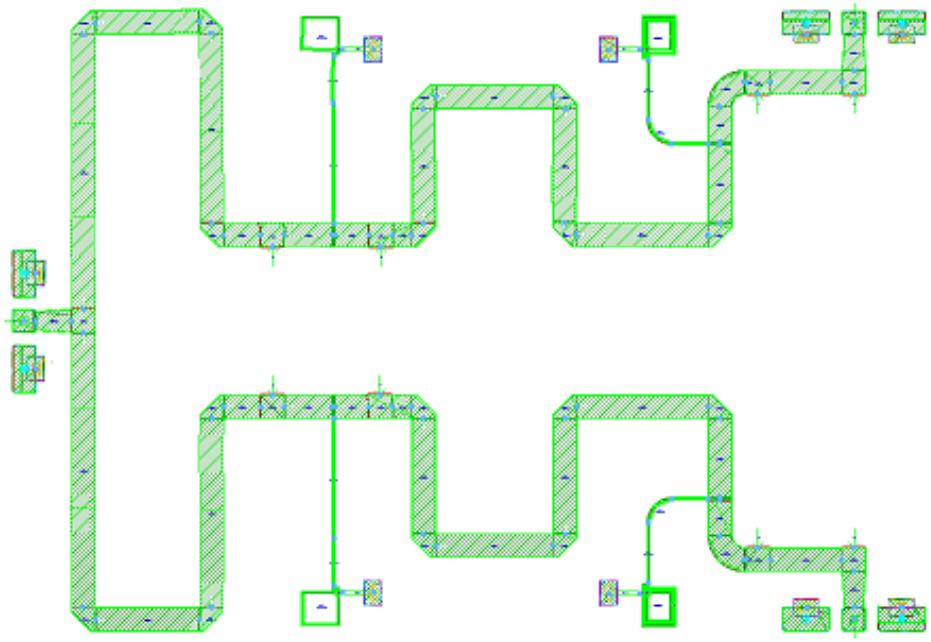


Figure 3.25. Layout of Switch II for EM Simulation

IC measured by probe station exhibits an insertion loss of better than 0.8 dB for the whole X-band, while simulation results vary between 1.2 dB and 1.4 dB in the frequency range of interest. Similar to Configuration I, Configuration II also has better measured insertion loss than predicted by simulation. One of the possible reason is out of date switch transistor models provided by the factory whereas exaggerated skin-effect for quarter-wave transmission line during simulation procedure may also be the cause of the conflict as discussed in section 3.4.2.1. On the other hand; curve trends of simulation and measurement results are similar. Roll-offs, caused by capacitive components, occur at nearly same frequency ranges, which may prove accurate modelling of parasitic capacitances.

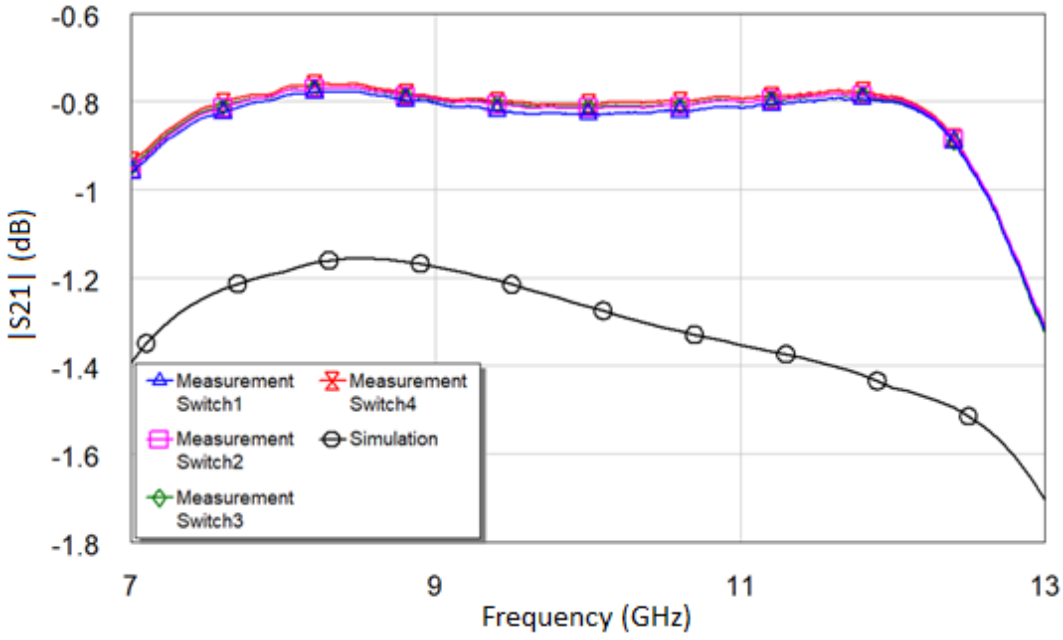


Figure 3.26. Simulated and Measured |S21| at On State

The equivalent circuit diagram for conducting branch is given in Figure 3.27. For insertion loss case, switch transistors are turned OFF to provide signal flow through the transmission line. R defines the resistance of the quarter wavelength transmission line whereas C(Q1), C(Q2), C(Q3), and C(Q4) stand for parasitic capacitances of 0FF-state transistors. Since number of resistive components are increased compared to the first switch configuration, insertion loss is higher than the first configuration.

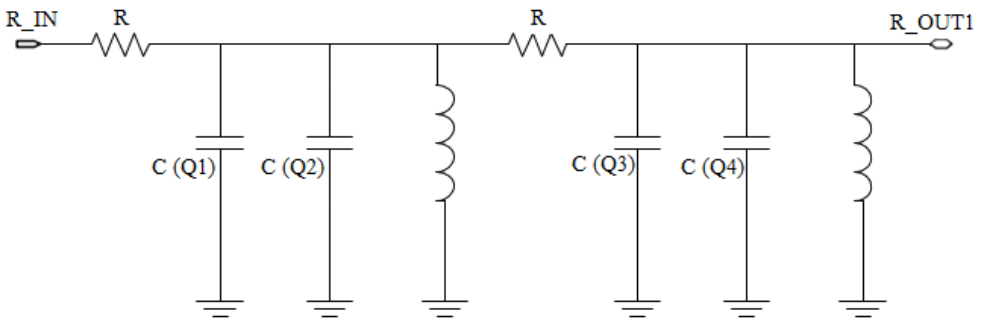


Figure 3.27. Equivalent Circuit Diagram of Conducting Branch

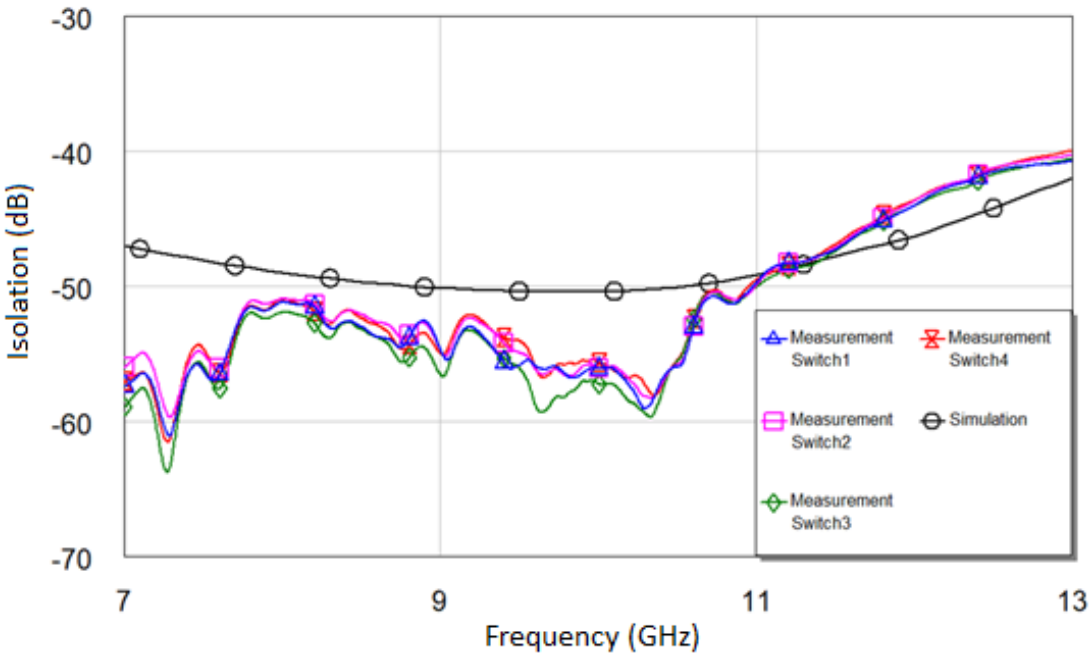


Figure 3.28. Simulated and Measured Isolation

Comparison of simulated and measured isolation of Configuration II is presented in Figure 3.28, which are consistent with each other. Simulation result of isolation is around 50 dB while measurement result is better than 50 dB for most of the band. Since for isolation case switch transistors are put into ON state, on resistances of the transistors and transmission line which is nearly at open state are in effect. Since the compensation inductors are in parallel with the small-valued on-resistances, they do not have impact on the result. Ripples at measurement lines are caused by connector defects occurred during calibration process.

The switch is very well matched, and provides a measured return loss of better than 13 dB, for 8-12 GHz band as presented in Figure 3.29.

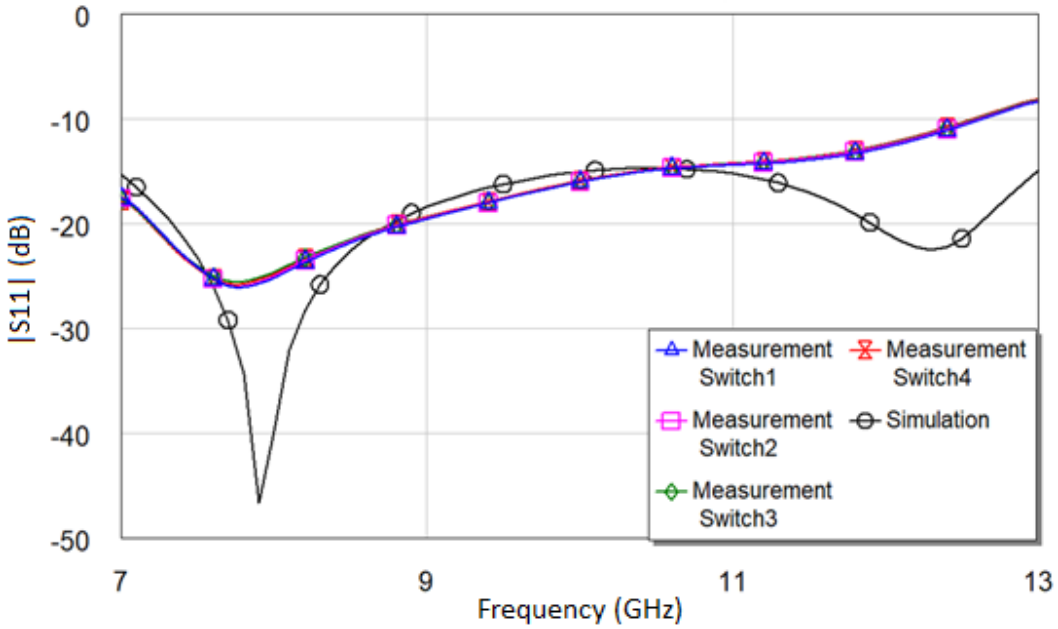
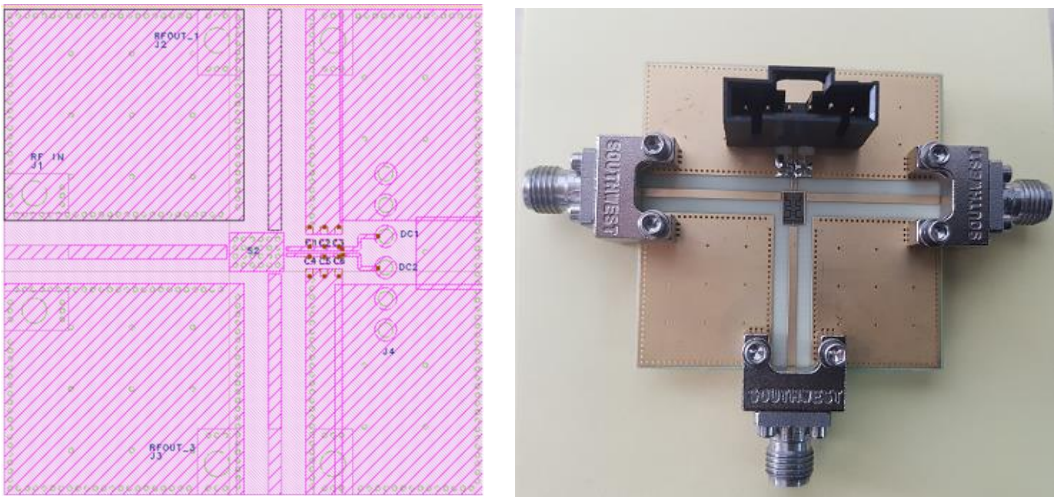


Figure 3.29. Simulated and Measured $|S_{11}|$

To investigate the power handling capability of the switch, an evaluation PCB was designed and fabricated. The layout of the PCB is given in Figure 3.30 (a). The fabricated PCB, which is presented in Fig 3.30 (b), is a single layer PCB with 20 mil thick RO4003C material. With the given substrate thickness, a microstrip line width of 1.1 mm corresponds to a 50 Ω transmission line, which transmit the RF input signals to the RF input ports of the switch, and output signals to the measurement devices. For DC biasing of the gates of switch transistors supply rails are placed. For each supply rail, three shunt capacitors with 1 nF, 100 nF, and 1 µF capacitance are placed as decoupling capacitors. Decoupling capacitors filter out the undesired signals coming from the DC supplies by creating self-resonance circuits. The connector located at the upper side of the photo at Figure 3.30 (b) is for DC biasing, whereas the other three connectors are for RF signal transmission.



(a) (b)

Figure 3.30. Layout of the Designed Evaluation PCB (a), Fabricated PCB (b)

The setup used to determine P1dB includes a signal generator, two amplifiers (one of them is fabricated by the same factory), after the switch there exists an attenuator with 30 dB attenuation. Final signal is examined by a spectrum analyzer. The measurement setup is illustrated in Figure 3.18. The power amplifier fabricated within the same research project and the switch which is under investigation are also photographed in Fig.3.31.

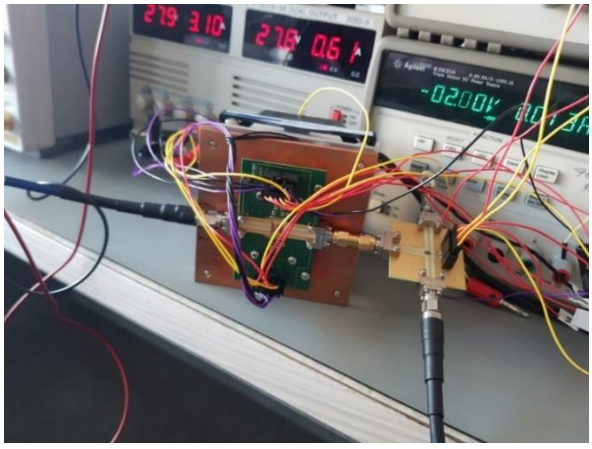


Figure 3.31. Power Amplifier as Input Source and the Switch Under Investigation

Additional losses introduced by the PCB and RF cables are also considered and measured with varying frequency.

Taking the additional losses into consideration, the resultant P1dB graph is drawn in Figure 3.32. Based on this linearity measurement, 1-dB compression point (P1dB) is observed at nearly 43.3 dBm at 10.6 GHz. This value is very close to the compression point of the amplifier, therefore may not represent the linearity of the switch.

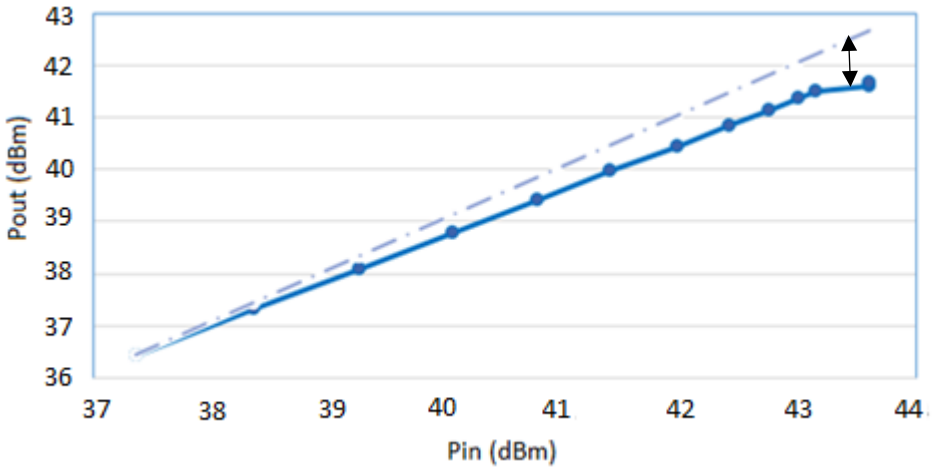


Figure 3.32. Measured Output Power versus Input Power

CHAPTER 4

CONCLUSION AND FUTURE WORK

Within this thesis, design, simulation, and evaluation of two single pole double throw (SPDT) switches, working in X-band are presented. The switches are based on AlGaN/GaN HEMT on SiC substrate technology provided by WIN Semiconductors. The switches are designed to handle 25 Watts (44 dBm) of input power, while achieving low insertion low, and high isolation values. In order to achieve very low insertion loss quarter wavelength topology is employed eliminating the need for the series device. In order to enhance isolation performance of the switch two successive series transmission line, shunt transistor topology is used in Configuration II.

Some published results of GaN high power switches in X-band and up to 18 GHz are presented in Table I. The switch configuration II presented in this thesis has the highest isolation with 50 dB for most of the frequency band of interest, where switch configuration I has one of the best insertion loss, 0.3 dB, among the GaN switches available in literature. Measured insertion loss of Configuration II is nearly 0.8 dB for X-band. Both of the switches are very well matched. Measured return loss of the switches are better than 15 dB, and 13 dB, for Configuration I, and Configuration II, respectively. This performance is achieved with careful tuning and co-design of the transmission lines, shunt transistors, and resonance inductors. Linearity performance of the switches are also successful among the switches available in literature with measured 1-dB compression point at 41 dBm, and 43.3 dBm, for Configuration I, and Configuration II, respectively.

Table 4.1. *Performance Comparison*

Reference	**Operating Frequency (GHz)**	**IL (dB)**	**Iso. (dB)**	**Return Loss (dB)**	**Power (dBm)**	**Comp (dB)**	**Chip Size (mm^2)**
Campbell et al. (2010)	0-12	1	30	12	41	0.4	1.15x1.66
	0-18	1.5	25	12	40	0.4	1.15x1.66
Janssen et al. (2008)	8-11	3.5	30	10	44	-	4x1.8
Masuda et al. (2012)	0-12	1.2	30	-	39.2	1	1.8x2.4
Bettidi et al. (2008)	8-12	2	35	15	37	1	3.2x1.2
Osmanoglu et al. (2014)	0-12	1.4	20	14.5	40.5	0.2	1.7x0.94
Ciccognani et al. (2008)	8-11	1	37	13	>39.5	1	2.4x1.9
Alleva et al. (2008)	8-11	1	37	13	39	1	2.4x1.9
	2-18	2.2	25	11	38	1	2x1.7
Config I	**8-12**	**0.3**	**30**	**15**	**41**	**1**	**2.9x2.1**
Config II	**8-12**	**0.8**	**44**	**13**	**43.3**	**1**	**4.1x2.7**

The only drawback of the switches is the relatively large die area, which may not be a problem for integrated systems with a PA and an LNA where the total die size is mostly dictated by PA. Another disadvantage may be bandwidth restriction arising from transmission line. Since working principle of quarter wave-length transmission lines is based on corresponding frequency, the performance of the switch degrades as frequency changed from the operational frequency. As future work another switch in diminished dimensions can be designed with similar power, insertion loss, and isolation performance to the switches subject to this thesis.

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