

GAN-HEMT BASED KU-BAND RF POWER AMPLIFIER DESIGN FOR
SATCOM APPLICATIONS

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submitted by **AHMET MERT POLATER** in partial fulfillment of the requirements
for the degree of **Master of Science in Electrical and Electronics Engineering De-
partment, Middle East Technical University** by,

Prof. Dr. Halil Kalıpçılar
Dean, Graduate School of **Natural and Applied Sciences**

Prof. Dr. İlkey Ulusoy
Head of Department, **Electrical and Electronics Engineering**

Prof. Dr. Şimşek Demir
Supervisor, **Electrical and Electronics Engineering, METU**

Examining Committee Members:

Prof. Dr. Sencer Koç
Electrical and Electronics Engineering, METU

Prof. Dr. Şimşek Demir
Electrical and Electronics Engineering, METU

Prof. Dr. Gülbin Dural
Electrical and Electronics Engineering, METU

Assoc. Prof. Dr. Lale Alatan
Electrical and Electronics Engineering, METU

Assist. Prof. Dr. Ahmet Hayrettin Yüzer
Electrical and Electronics Engineering, Karabük University

Date:

I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

Name, Last Name: AHMET MERT POLATER

Signature :

ABSTRACT

GAN-HEMT BASED KU-BAND RF POWER AMPLIFIER DESIGN FOR SATCOM APPLICATIONS

POLATER, AHMET MERT

M.S., Department of Electrical and Electronics Engineering

Supervisor : Prof. Dr. Şimşek Demir

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As many of today's wireless applications need, transmitters of satellite communication (SATCOM) applications require one of the vital circuits in microwave world; a unique RF power amplifier, the sub circuit which is located just before the antenna of the transmitter. RF power amplifiers are the circuits used to amplify the low-power RF signals to achieve adequately high-power signals for various applications. Different than the traditional Si transistor-technology based power amplifiers, the main aim of this dissertation is to study gallium nitride (GaN) high electron mobility transistor (HEMT) based Ku-band RF power amplifier design for SATCOM between a missile's transmitter and a satellite's receiver. The reason of common usage of GaN transistor technology in RF power amplifier design in the last ten years caused by the emerging need of more linear operation at higher frequencies; i.e. the frequencies used in SATCOM applications. Therefore, a GaN HEMT based RF power amplifier design with 1 Watt (30 dBm) output power working at 14 GHz center frequency has been studied and designed. All performance parameters are explained by simulation results and measurements. Firstly, the design, whose performance parameters

have been verified with schematic and electromagnetic (EM) simulations, has been prototyped with printed circuit board (PCB) etching devices such as LPKF. The observations made after prototyping showed that the performance difference between simulation results and measurements caused by the manufacturing and assembly errors. As an example of such undesired errors, “poor grounding” of the main transistor can be given due to lack of filled vias under the transistor. For such high frequency applications, poor grounding can cause a great degradation on the gain. As a result, the observations have proved that the used transistor does not work properly even though the impedance matching appears as successful for this work. Therefore, it has been understood that more sensitive production method should be chosen. Secondly, a professional foundry is preferred for PCB manufacturing and seems that effects of the problems caused by the first method are eliminated or decreased remarkably. In addition, a “rework” process is conducted after manufacturing for fine tuning. Lastly, a comparison table of simulation results with two different manufacturing methods are also exhibited in this study.

Keywords: RF, Radio Frequency, Microstrip Line, Power Amplifier, Ku-Band, GaN, HEMT, High Electron Mobility Transistor, SATCOM, Satellite Communication, PCB, Printed Circuit Board, Discrete Design.

ÖZ

UYDU İLETİŞİM UYGULAMALARI İÇİN GAN-HEMT TABANLI KU-BANT RF GÜÇ YÜKSELTEÇ TASARIMI

POLATER, AHMET MERT

Yüksek Lisans, Elektrik ve Elektronik Mühendisliği Bölümü

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Günümüzde kullanılan birçok kablosuz uygulamada ihtiyaç duyulduğu gibi, uydu iletişim uygulamalarında yer alan göndermeç birimi de, mikrodalga dünyasının en önemli devrelerinden; özgün bir RF güç yükseltecine bünyesinde yer alan antenden hemen önce ihtiyaç duyar. RF güç yükselteçleri, zayıf güçteki RF giriş işaretlerini uygulamaya göre ihtiyacı değişen yüksek güçlü çıkış işaretlerine dönüştürmekte kullanılan devrelerdir. Bu çalışmanın temel amacı; bir füze göndermeçi ile bir uydu almacı arasında kurulan uydu iletişiminde kullanılmak üzere, geleneksel Si transistör teknolojisi temelli tasarlanan güç yükselteçlerinden farklı olarak, galyum nitrat (GaN) yüksek elektron mobiliteli transistör (HEMT) temelli, Ku bantta çalışan bir güç yükselteci geliştirmektir. GaN teknolojisine sahip transistörlerin, geçtiğimiz on yıldır RF güç yükselteç tasarımlarında yaygın olarak kullanılmaya başlanmasının sebebi olarak, uydu iletişimi gibi yüksek frekanslı uygulamalarda duyulan “daha doğrusal çalışma ihtiyacı” gösterilebilir. Bu amaçla, 14 GHz merkez frekansında çalışan ve 1 Watt (30 dBm) çıkış gücüne sahip GaN HEMT tabanlı bir güç yükselteci, bu tez kapsamında çalışılmış ve tasarlanmıştır. Tüm performans parametreleri, benzetim ve

ölçüm sonuçları ile açıklanmıştır. İlk adım olarak, şematik ve elektromanyetik (EM) benzetim çalışmaları ile doğrulanmış RF güç yükselteç tasarımı, LPKF olarak adlandırılan baskılı devre kartı (Printed Circuit Board, PCB) kazıma cihazı ile prototiplenmiştir. Prototipleme sonrası gerçekleştirilen gözlemler, benzetim ve ölçüm sonuçları arasında oluşan performans farklılığının, üretim ve komponent dizim hatalarından kaynaklandığını göstermiştir. Bu istenmeyen hatalara bir örnek olarak, transistör altında yer alan via'ların içinin doldurulmuş olmamasından kaynaklı, transistörün yeteri kadar topraklanamaması gösterilebilir. Bu çalışma ve benzeri yüksek frekanslı uygulamalarda yetersiz topraklama, transistörün kazancında çarpıcı seviyelerde azalmaya yol açabilmektedir. Bu uygulamada da ölçüm sonuçları sonrası benzer bir gözlemde bulunulmuş, empedans uyumlaması başarılı olarak değerlendirilmiş ancak transistör istenilen kazanç ile çalıştırılamamıştır. Sonuç olarak, daha hassas bir üretim yönteminin tercih edilmesi gerektiği anlaşılmıştır. İkinci adım olarak profesyonel bir PCB üretim tesisi tercih edilmiş ve ilk üretim yöntemi sonrası karşılaşılan birçok problemin etkisinin büyük ölçüde azaldığı veya ortadan tamamen kaldırıldığı görülmüştür. Ek olarak, bu iki üretim yönteminden sonra eniyileme amaçlı gerçekleştirilen “re-work” süreci ile benzetim ve üretim sonuçları, karşılaştırmalı olarak tablo üzerinde bu çalışmanın kapsamında sunulmuştur.

Anahtar Kelimeler: RF, Radyo Frekansı, Mikroşerit Hat, Güç Yükselteci, Ku-Bant, GaN, HEMT, Yüksek Elektron Mobiliteli Transistör, PCB, Baskılı Devre Kartı, Uydu Haberleşme.

to my family...

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TABLE OF CONTENTS

ABSTRACT	v
ÖZ	vii
ACKNOWLEDGMENTS	x
TABLE OF CONTENTS	xi
LIST OF TABLES	xiv
LIST OF FIGURES	xv
LIST OF ABBREVIATIONS	xx
CHAPTERS	
1 INTRODUCTION	1
1.1 Background	1
1.2 Aim of the Study	4
1.2.1 In-house & Fast Prototyping	4
1.2.2 Cost Effectiveness	5
1.2.3 Rework Flexibility	5
1.2.4 Easy Detection of Errors	6
1.3 Aim and Specifications	6
1.4 Thesis Outline	8
1.5 Achievements	9

2	THEORY OF POWER AMPLIFIER DESIGN	11
2.1	Class Choice of the Amplifier	11
2.2	Device Technology	13
2.2.1	GaN & HEMT	13
2.2.2	Transistor Choice	14
2.3	Power Amplifier Design Parameters	14
2.3.1	Operating Point / Quiescent Point / Q-Point / Bias Point	15
2.3.2	Gain of an Amplifier (In terms of Scattering Parameters, S_{21})	16
2.3.3	Max Gain and Source & Load Impedance Choice	16
2.3.4	Efficiency	17
2.3.4.1	Drain Efficiency	18
2.3.4.2	Power Added Efficiency (PAE)	18
2.3.5	Linearity & Output Power	19
2.3.5.1	P_{1dB} & P_{SAT}	21
2.3.5.2	Harmonic Distortions (HD_2, HD_3, \dots, HD_n)	23
2.3.5.3	Third Order Intercept Point (IP3)	25
2.3.6	Stability	26
2.3.6.1	Unconditionally Stable	26
2.3.6.2	Conditionally Stable	27
3	DESIGN AND SIMULATION RESULTS	29
3.1	Early Design with Ideal Lumped Elements	31

3.2	Improved Final Design with both Distributed and Non-Ideal Lumped Elements	33
3.3	PCB Layout by ALTIUM	42
3.4	Electromagnetic Simulations by CST	43
4	IMPLEMENTATION AND MEASUREMENTS	47
4.1	Production Process	47
4.1.1	Circuit Prototyping by Using LPKF	47
4.1.2	Final Circuit Production by "Professional Facility" (<i>Simpro Elektronik</i>)	50
4.2	Measurements	51
4.2.1	Measurement Equipment and Setup	51
4.2.2	Final Measurement Results	54
4.2.2.1	Gain Measurement Results	56
4.2.2.2	Linearity Measurement Results	60
4.2.2.3	P_{1dB} Measurement	60
4.2.2.4	Harmonic Distortion (HD) Measurements	60
4.2.2.5	Intermodulation Distortion (IMD) Measurements	62
4.2.3	Investigation of Reasons of Gain Degradation	62
4.2.3.1	CST Based Investigation	63
4.2.3.2	New Circuit Production Based Investigation	64
5	CONCLUSION, ACHIEVEMENTS AND FUTURE WORK	67
	REFERENCES	73

LIST OF TABLES

TABLES

Table 1.1	Design Specifications for Power Amplifier	7
Table 1.2	Radio Link Design for Having SNR > 10 dB	7
Table 2.1	Four Main Classes of Amplifiers and Characteristics	12
Table 2.2	HD Power Level Changes w.r.t RF Input Power	24
Table 3.1	Values of the Lumped Elements of Early Design	32
Table 3.2	S-Parameters of Early Design at Center Frequency	33
Table 3.3	Values of the Lumped Elements of DC Section of Improved Final Design	37
Table 3.4	Values of the Lumped and Distributed Elements of RF Section of Improved Final Design	39
Table 3.5	S-Parameters of Improved Design at Center Frequency	40
Table 3.6	S-Parameters Comparison of Early and Improved Designs	41
Table 4.1	Measurement for P_{1dB}	60
Table 4.2	Existence of Harmonic Distortions at Critical RF Input Levels	61
Table 5.1	Comparison of Simulation Results and Measurements	68
Table 5.2	Final Gain Value After Response Calibration	70

LIST OF FIGURES

FIGURES

Figure 1.1	Presentation of Candidate SATCOM Application for Missile Guidance	2
Figure 1.2	Basic Transmitter and Receiver Blocks with EIRP and SNR	3
Figure 2.1	Basic Conduction Angle Behavior for Main Amplifier Classes	12
Figure 2.2	Structure of a GaN HEMT Device	14
Figure 2.3	Q-Point Options on Possible Load Lines of GaN Transistor Technology by Qorvo [1]	15
Figure 2.4	Conducted IV Curve Analysis by AWR; Schematic and Graph	16
Figure 2.5	Input, Output, Source, Load Impedances and Source, Load Reflection Coefficients	17
Figure 2.6	Smith Chart Load Pull Analysis by AWR and Results for Max Efficiency and Power Transferred to Load	19
Figure 2.7	Port Types Used for Various Parameter Simulations in AWR, A: P_{1dB} and P_{SAT} Simulation, B: S-Parameter Simulation, C: IP3 Simulation	20
Figure 2.8	P_{1dB} and P_{SAT} Analysis of the Power Amplifier Designed by AWR	22
Figure 2.9	Input Power = -20 dBm, HD Analysis Conducted by AWR	23
Figure 2.10	Input Power = 0 dBm, HD Analysis Conducted by AWR	23
Figure 2.11	Input Power = +20 dBm, HD Analysis Conducted by AWR	24

Figure 2.12 IMD Analysis Conducted by AWR	25
Figure 2.13 R-C Stability Network Used in Final Design	27
Figure 2.14 Stability Analysis Conducted by AWR	28
Figure 3.1 Block Schematic Power Amplifier with All Sub-Networks	29
Figure 3.2 Schematic of Early Design with Ideal Lumped Elements	31
Figure 3.3 S-Parameters of Early Design with Ideal Lumped Elements	32
Figure 3.4 Schematic Showing the Replacement of Ideal Elements with Non-ideal Elements	34
Figure 3.5 Microstrip Line-Dielectric Structure with Important Design Parameters	36
Figure 3.6 Schematic of Improved Final Design with both Distributed and Non-Ideal Lumped Elements	36
Figure 3.7 DC Section of Improved Final Design with Non-Ideal Lumped Elements	37
Figure 3.8 RF Section of Improved Final Design with Non-Ideal Lumped Elements	38
Figure 3.9 S-Parameters of Improved Design with both Distributed and Non-Ideal Lumped Elements	40
Figure 3.10 (a) 2D and (b) 3D Layout of Final Design with both Distributed and Non-Ideal Lumped Elements on AWR	42
Figure 3.11 2D and 3D Layout of Final Design without SMDs via ALTIUM	42
Figure 3.12 2D Layout Showing Drop Structure for Rework Flexibility	43
Figure 3.13 Meshed Layout of Final Design with both Distributed and Non-Ideal Lumped Elements on CST	44

Figure 3.14 Power Amplifier’s CST Configuration for Conducting EM Simulation	44
Figure 3.15 Power Amplifier Final Design EM Simulation Result by CST	45
Figure 4.1 Power Amplifier Circuit Produced by LPKF	48
Figure 4.2 Complete Power Amplifier by LPKF a) General View b) Right Side View c) Front Side View d) Vertical Right View e) Vertical Left View	49
Figure 4.3 Power Amplifier Circuit Produced by Professional Facility (<i>Simpro Elektronik</i>)	50
Figure 4.4 Complete Power Amplifier by Professional Facility (<i>Simpro Elek- tronik</i>) a) General View b) Vias Under Transistor c) X-ray Image of Tran- sistor d) X-ray Image of Complete PA e) X-ray Image of Conical Inductor	51
Figure 4.5 Workspace for Power Amplifier Measurements	52
Figure 4.6 First Configuration of Measurement Setup for S-Parameters	52
Figure 4.7 First Measurement Setup for S-Parameters a) Network Analyzer b) Power Amplifier under Test c) DC Supply d) Calibration Set Used for Network Analyzer	53
Figure 4.8 Second Configuration of Measurement Setup for P_{1dB} and P_{SAT} . . .	53
Figure 4.9 Second Configuration of Measurement Setup for P_{1dB} and P_{SAT} a) Signal Generator b) Signal Analyzer c) Power Amplifier d) DC Supply . . .	54
Figure 4.10 Gain and Input Matching Performance of the Power Amplifier Cir- cuit Produced By LPKF	54
Figure 4.11 Input and Output Matching Performance of the Power Amplifier Circuit Produced By LPKF	55
Figure 4.12 First S-Parameter Measurement of PA Produced by Professional Facility	55

Figure 4.13 Optimization Applied S-Parameter Measurement of PA Produced by Professional Facility	56
Figure 4.14 Replacement of SMA Connectors in the Design	56
Figure 4.15 S-Parameter Measurement of PA After Replacement of SMA Connectors	57
Figure 4.16 Optimization Applied S-Parameter Measurement of PA After Replacement of SMA Connectors	57
Figure 4.17 Improvement of Gain Gradually	58
Figure 4.18 Output Power Measurement Using Signal Generator & Analyzer	59
Figure 4.19 Observation of Harmonic Distortions (HD_2 and HD_3) with Different Power Levels of Input Signals	61
Figure 4.20 Observation of Intermodulation Distortions (IMD_3 , IMD_5 , IMD_7 and higher levels of IMDs) with Different Power Levels of Input Signals	62
Figure 4.21 Meshed Circuit on CST & E-Field Monitoring on Circuit & Microstrip Line Insertion Loss Simulations on CST without Connector Effects	63
Figure 4.22 Simple Microstrip Line Production by LPKF for Measurement of Connector-to-Connector Insertion Loss	64
Figure 4.23 Three Different Microstrip Line & Connector Configurations for Measurement of Connector-to-Connector Insertion Loss	65
Figure 4.24 Connector-to-Connector Insertion Loss Measurements from 13.6 GHz to 14.6 GHz	65
Figure 4.25 Connector-to-Connector Insertion Loss Measurements from 1.0 GHz to 10.0 GHz	66
Figure 4.26 Connector-to-Connector Insertion Loss Measurements from 10.0 GHz to 15.0 GHz	66

Figure 5.1 Gain vs. Frequency Result After Conduction of "Response Calibration" 69

LIST OF ABBREVIATIONS

2D	2 Dimensional
3D	3 Dimensional
AC	Alternative Current
BER	Bit Error Rate
dB	Decibel
DC	Direct Current
DFN	Dual Flat No Lead
EM	Electromagnetic
EIRP	Effectuated Isotropic Radiated Power
GaN	Gallium Nitride
HD	Harmonic Distortion
HEMT	High Electron Mobility Transistor
IC	Integrated Circuit
IM3	3rd Order Inter Modulation
IP3	3rd Order Intercept Point
Ku	Kurtz Under
LEO	Low Earth Orbit
LNA	Low Noise Amplifier
P1dB	1dB Compression Point
PA	Power Amplifier
PAE	Power Added Efficiency
PCB	Printed Circuit Board
PSAT	Saturation Point

RF	R adio F requency
Rx	R eceiver
SATCOM	SAT ellite COM munications
SMD	S urface M ount D evice
SMT	S urface M ount T echnology
SNR	S ignal to N oise R atio
Tx	T ransmitter
UAV	U nmanned A ir V ehicle

CHAPTER 1

INTRODUCTION

1.1 Background

In today's world, military and commercial developments drive each other [2–4]. Fast technological developments/innovations in the communication industry increases the pace of the domination of the humanity on space. As a result of such domination, more and more satellites have been launched and sent to the space, to respond the needs of military & commercial communication-based applications [5–10].

On the contrary to early years of satellite technology, now satellites that have been launched are not used for a single purpose; only for commercial applications or only for military applications but instead they serve for both [11–19]. To achieve such capability of multiuse, communication frequencies of satellites are distinguished as 'military bands' and 'civilian bands' by the related authorities.

Military bands of satellites are commonly used for a live, strong communication with aircrafts, UAVs, ships, land vehicles, and even now with (long distance flying, smart, and sophisticated) missiles; does not matter where they are; cause geographical obstacles do not affect the state of the satellite communication (SATCOM). This situation makes SATCOM very desirable for military applications. In fact, such vehicles/platforms need military SATCOM for plenty of communication abilities; safe/encrypted communication, duty (mission) update capability, verification of the current location in terms of coordinates, transferring an image or video for surveillance or tracking a target etc. Therefore, it must be stated that each SATCOM application requires different/various bandwidths and in telecommunication/RF engineering world it is a very well-known fact that the bandwidth needed is directly related to the amount of data

wished to be transferred [20]. In other words, if the transferred data is small even a narrow band is enough/sufficient to achieve a successful satellite communication, while a large band is a must for large data transmission-based applications, i.e. sending an image or video recorded by a camera located on an UAV to ground station via SATCOM.

In this study, the major focus is on a satellite communication application preferred by a long distance-flying, sophisticated missile system which mostly needs a narrow-band transmitter system to send its current coordinate information. Therefore, after its ‘launch’ it can get a mission update in terms of the target’s current location, as shown in Figure 1.1.

To achieve this ability in a missile system, the main motivation was to design a RF power amplifier, one of the most important sub-circuits of a SATCOM transmitter, working in Ku band, which is the common frequency band for satellite communication [21,22].

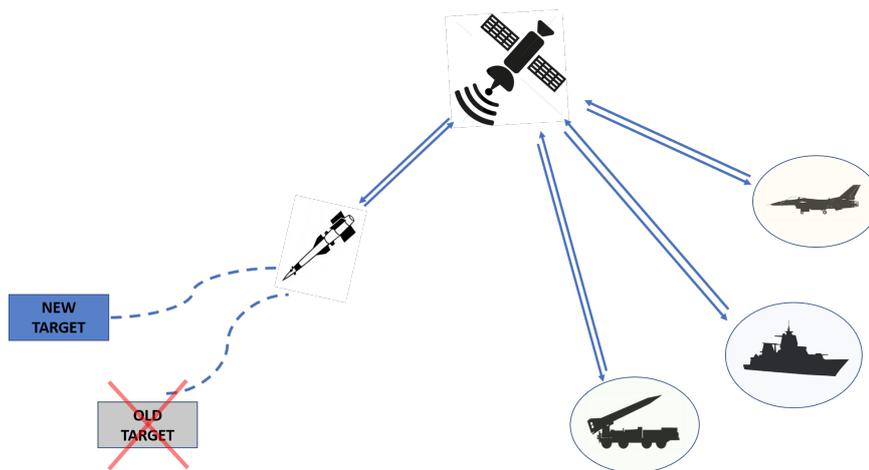


Figure 1.1: Presentation of Candidate SATCOM Application for Missile Guidance

Redundancy and maximum range of a communication system is mainly and directly related to the ability of designing a successful power amplifier since PA has a dominant contribution on the magnitude of transmitter’s output power. To understand this relationship, two major terms appears in communication channel between transmitter and receiver; effective isotropic radiated power (EIRP) and signal to noise ratio (SNR).

Effective isotropic radiated power (EIRP) is the power level just after the antenna of the transmitter without any propagation in the channel. Therefore, when the gain of the transmitter antenna is subtracted from the EIRP value, the output power of the RF power amplifier is left, which summarizes the importance of a power amplifier in a SATCOM application. The other term, which is SNR, is related with all transmitter-channel-receiver block chain. In other words, SNR helps designer to understand the unwanted noise level on the desired transmission signal after all the propagation through the channel, with the effects of channel noise and receiver antenna. Simply there are three methods to increase the SNR level, first the distance of communication channel can be decreased so that the channel noise infected to the signal can be reduced. Second, the gain of receiver antenna, the antenna belonging to the receiver side, may be increased but unfortunately due to the volume/area considerations it is a power/gain-limited solution. Third, the output power of the transmitter can be increased, which emphasized again the first term, EIRP.

To express what has been explained above in terms of EIRP and SNR, a simple block diagram has been shared in Figure 1.2.

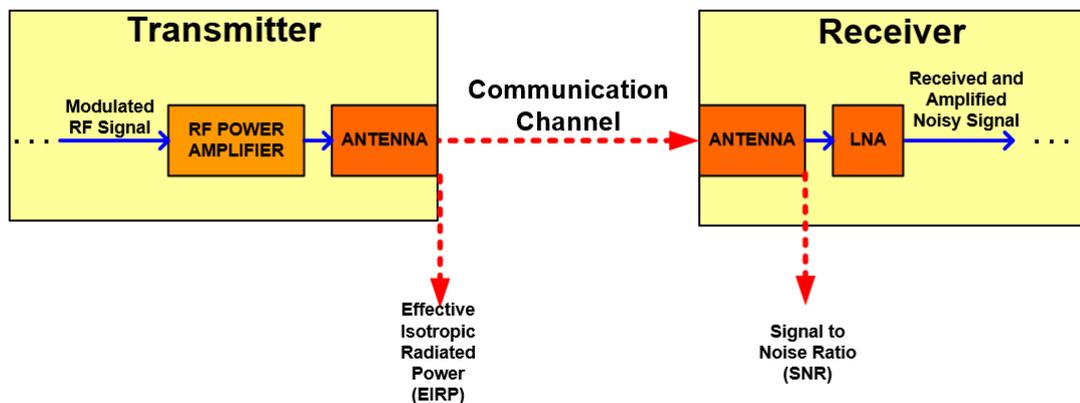


Figure 1.2: Basic Transmitter and Receiver Blocks with EIRP and SNR

1.2 Aim of the Study

In this research, GaN transistor technology based RF power amplifier design has appeared as the main topic which is wanted to be worked on. A detailed literature survey about GaN based RF power amplifier designs has been conducted and understood that GaN technology delivers unmatched performance at high frequency levels due to many advantages (Comparing to older, conventional transistor technologies such as Si or GaAs) such as; high power density, reduced size and part counts, excellent gain and efficiency, robust operation and long pulse capability, high operating voltage for improved system power efficiency etc. [23–27].

All of the advantages of GaN technology summarized above enable us to build high frequency transmitter systems, which helps to create powerful innovative applications like airborne Ku-Band satellite communication.

Conducted detailed literature survey has shown that there are many RF amplifier and transmitter designs based on IC technology [28–35] instead of discrete design working on X-band and higher bands. The reason of this choice is not hard to understand; at such high levels of frequencies, i.e. Ku band, PA design gets smaller and smaller, as a consequence the importance of the parasitic effects become significant. Therefore, preferring a die package helps designer to get rid of such unwanted effects and to achieve better performance.

On the other hand, obtaining a stand-alone working, unmatched transistor and building a discrete power amplifier design with all SMD peripherals has its own advantages. These advantages can be summarized in four main categories as shown below.

1.2.1 In-house & Fast Prototyping

By the help of the drilling devices like LPKF S103, which is chosen for the production process of power amplifier circuit, circuit has been printed on Rogers4003 material. Later, SMD assembly process has been conducted by hand, including the soldering of DFN packaged GaN transistor. Finally, circuit has become ready for performance measurements without needing any IC production, which is only possible at limited

number of factories located at different countries or even continents all around the world. In addition, by doing so the production time in this work has been diminished cause the lead time of an all IC-based power amplifier can reach up to “months”. For this study, the circuit manufacturing via LPKF took just two days including the soldering process of SMDs, although getting used to LPKF had also taken some time.

1.2.2 Cost Effectiveness

GaN based IC design in a single chip with all subnetworks of a PA is much more costly process than a Si-based IC or discrete design. Demanding a sample production, i.e. limited number of productions, from a IC production factory, instead of a mass production, makes the unit price much more higher. Even though there are methods in IC production to decrease the unit manufacturing costs such as using multi-project wafers (also known as multi-project chips), it is not enough to compete with others. To conclude, prototyping a Ku-band GaN RF power amplifier via a discrete design seems much more logical.

1.2.3 Rework Flexibility

After almost every new RF power amplifier design, the measurement results appear as shifted, distorted or changed a little bit or dramatically comparing with the outcomes of the simulation. To cope with such variations, power amplifier designer may need to conduct one or many “rework” operation. Unfortunately, this option is not valid for an IC-based design. In other words, if something goes wrong in the design or is wrong calculated, the chip becomes useless since designer can not do rework inside the chip. On the other hand, for a discrete design each component can be replaced or modified easily. For the power amplifier design, one of the most common problems is “burned component” due to unexpected heat problem. For the chosen approach for this work, it does not create a crisis situation cause even the burned transistor can be removed and soldered again in a discrete design, which provides rework flexibility to the designer.

1.2.4 Easy Detection of Errors

Prototyping is one of the most important steps of a design and even the most experienced engineers know that prototypes have errors, which is the purpose of prototype's existence. Errors can be caused by many reasons such as; design errors, manufacturing errors, environmental errors etc. Before finalizing the design and claiming to have a real "product", detection of such errors plays a significant role for removing them.

It is known that when a design gets smaller and smaller, it becomes harder to detect the errors via visual inspection or basic measurement tools, which is a major disadvantage of IC/die technology comparing to discrete design. For instance, in a discrete design, if an inductor in the input matching network of the PA fails due to high voltage rating, it is very easy to detect. In other words, burned components can be found by visual inspection or short circuit test can be applied by a simple multimeter.

1.3 Aim and Specifications

The aim of this study is to design and implement a single stage, discrete RF power amplifier using a GaN transistor technology. Simulations of the amplifier are conducted on AWR via the nonlinear transistor model, CGHV1F006S, provided by Cree-Wolfspeed itself. Aimed PA specifications are determined according to an application for establishing a digital communication system and sending a coordinate information, i.e. latitude and longitude in terms of degrees, minutes and seconds. The data transmitted is related with the bandwidth of the transmitter, i.e. operational bandwidths of all sub-components of the transmitter including the power amplifier.

For digital communication, the reliability of the transmission-reception chain is measured by the bit error rate (BER) which depends on signal to noise ratio (SNR) at the receiver side. For this study, SNR value at the receiver side needed, is assumed as greater than 10 dB for 10^{-5} BER. The assumption is done by considering common modulation types used in SATCOM such as BPSK and QPSK [36].

For this work, a successful radio link between a missile's transmitter and GOKTURK-1, which is the low-earth-orbit (LEO) satellite of TURKEY, is taken into considerations (Located at 680 km above the earth's ground). Specifications of the PA design are decided and shown in Table 1.1. Radio link calculation is also shown in Table 1.2.

Table 1.1: Design Specifications for Power Amplifier

Parameter Name	Aimed Value
Frequency	Ku band, centered at 14 GHz
Bandwidth	Around 100 MHz
Gain	S21 > 10 dB
Output Power	>30 dBm (1 Watt)
Power Added Efficiency	>15%
Input Return Loss	S11 better than -10 dB
Output Return Loss	S22 better than -10 dB
Isolation	S12 better than -10 dB

Table 1.2: Radio Link Design for Having SNR > 10 dB

Tx PA Output (dBm)		TX Antenna Gain (dBi)			TX Output (dBm), i.e EIRP		
30		30			60		
Frequency (MHz)		Communication Range (km)			Path Loss (dB)		
14000		680			-172.02		
Received Signal (dBm)	Rx Antenna Gain (dBi)	Rx LNA's Input (dBm)	LNA's Gain (dB)	Rx's NF (dB)	Bandwidth (MHz)	Noise Floor (dBm)	SNR (dB)
-112.02	40	-72.02	30	10	100	-84	11.98

In Table 1.2, bandwidth (100 MHz) requirement may seem as "unnecessarily large" for sending just the coordinate information. It is a rightful claim since the coordinate

information is a small data and it does not require such a wide bandwidth. However, sophisticated transmitter systems do not send only the coordinate information, but also the video/colorful picture data in these days. Therefore, this requirement is kept large as much as possible to make the design a promising candidate for future/present alternative applications.

1.4 Thesis Outline

In general, the following chapters consists the outcomes of conducted literature survey, considered analytical derivations, planned design, computer simulations related to the schematics of the design, related measurements of scattering parameters & linearity and finally the data collections from the observations made. While explaining the effort summarized above, the work is divided by specific chapters to be more clear for the reader.

Chapter 2 describes basically the theory of the power amplifier design, chosen amplifier class, important PA design parameters and used transistor technology, in terms of both GaN and HEMT choices.

Chapter 3 discusses the design and simulation results. In this chapter, two-leveled design process is explained step by step. Related schematics and the simulation results of each level are exhibited. Respectively, the levels are;

- 1- Early Design with Ideal Lumped Elements
- 2- Improved Final Design with both Distributed and Non-Ideal Elements

The chapter follows with explanations of the final design's sub-networks; biasing network, stability part of the circuit, input and output matching networks, gain stage and additional parts for rework capability.

In Chapter 4, the equipment used during the circuit production & measurement are presented and the measurement results of the manufactured amplifier are discussed.

Lastly, Chapter 5 concludes the entire work done by comparing the simulation results and the outcomes of the measurements, while explaining the numerical differences

between them. Also, solution proposals for the future works are exhibited to decrease or even completely remove the manufacturing errors which create the main variance.

1.5 Achievements

In this study, a discrete GaN based single stage power amplifier, which works as Ku-band for SATCOM applications, is designed, manufactured and lastly measured. According to the optimized schematic simulation results, the design has a gain around 12.8 dB while EM based simulations indicates the gain as 9.87 dB. After two different manufacturing process (LPKF and professional facility), best gain values are measured as 5.02 dB and 4.29 dB. When response calibration is applied to those values, it is observed that the real power gain is around 7.3-7.4 dB.

Apart from the gain parameter, for both cases; "optimized schematic simulation" and "professional facility production", isolation, input and output return losses better than -10 dB are achieved with a stable operation around the fundamental frequency, i.e. 14 GHz - 14.1 GHz.

CHAPTER 2

THEORY OF POWER AMPLIFIER DESIGN

Each RF power amplifier is unique and specifically designed for the desired application. Uniqueness of the design is caused by the different requirements of various applications. Some examples of PA design requirements can be sorted as high linearity, high output power, high gain, or high efficiency depending on the application. However, trying to improve any parameter of a PA to achieve related requirement, can make another parameter worse. That's why PA design is an iterative process and full of trade-offs. Before going into the details of each design parameter's theory, one should keep in mind that the design priority is on the choice of the class of amplifier.

2.1 Class Choice of the Amplifier

Depending on the quiescent point and conduction angle, the class of an amplifier is determined. Deciding the class of a power amplifier has a significant importance since the class is the limiting/dominant factor on the main properties of an amplifier such as linearity, efficiency etc.

Depending on the application, there are many different amplifier classes that has been developed; Class A, Class B, Class AB, Class C etc. A detailed theoretical explanation for each class is not given because it is not the scope of this study but instead, a brief comparison table for the four main amplifier classes is shown in Table 2.1 with their distinguishing parameters so the preference reason of corresponding class can be understood easily.

Table 2.1: Four Main Classes of Amplifiers and Characteristics

Type	Conduction Angle	Linearity	Efficiency	Gain	Power Capability
Class A	360°	Excellent	Poor (Theoretically limited with 50%)	High	Low
Class B	180°	Medium	Good (Theoretically limited with 78.5%)	Medium/High	High
Class AB	$180^\circ < n < 360^\circ$	Good	Fair	High	Medium/High
Class C	$n < 180^\circ$	Poor	Good (Theoretically 100%)	Low	High

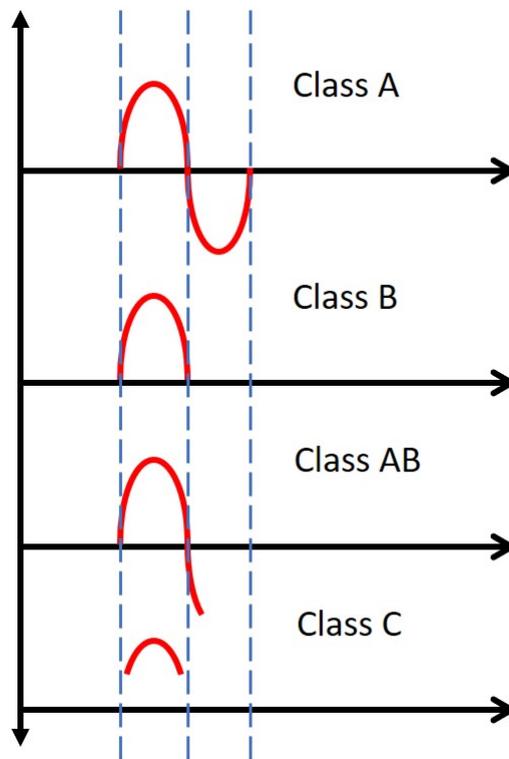


Figure 2.1: Basic Conduction Angle Behavior for Main Amplifier Classes

Behaviour and main properties of four main class type of amplifiers are shown in Figure 2.1 and Table 2.1 respectively. As shown on the third row of Table 2.1 and Figure 2.1, Class AB is a hybrid type of Class A and Class B whose conduction angle is between 180° and 360°. By evaluating Class A and Class B, it is clearly

seen that there is a trade-off relationship between linearity and efficiency. Therefore, depending on the chosen conduction angle, required efficiency and linearity values can be adjusted by the designer. In addition, Class C exhibits a limited conduction angle, poor gain and linearity behavior which is not preferred due to the tendency of having unwanted harmonic distortions very easily at the output. Therefore, Class AB has been chosen to obtain moderate levels of linearity, efficiency and gain in a single stage design and to avoid extremely good or bad linearity and efficiency values. Choice of Class AB can also be verified with the other SATCOM PA designs in the literature.

2.2 Device Technology

2.2.1 GaN & HEMT

When the scientific background of this type of transistor technology is investigated, analytical derivations has shown that GaN based transistors have advantages in terms of handling much more input power compared to conventional, power & frequency limited (Limited as low frequency with high power or high frequency with low power) Si based transistors and also comparing to one of today's most popular transistor technology; GaAs. When GaN and GaAs technologies based applications (Amplifiers, switches etc.) are put into an analytical comparison, it is observed that GaAs based designs are more likely to work at low voltages and currents while GaN based fabricated amplifiers can operate at the voltages around 40 V and higher. Even though both technologies are made of III-V compound semiconductors, the characteristics differ due to the key material characteristics like; relative dielectric constant, breakdown voltage, electron mobility and thermal conductivity. One comparison, as an illustration, can be considered based on band-gap difference; GaN has a bandgap about 3.4 eV while GaAs has 1.4 eV. Another example can be given related to the thermal conductivity; analytical derivations have shown that GaN has a thermal conductivity around 1.7 W/cm-K, which is almost three times bigger than GaAs thermal conductivity; 0.46 W/cm-K. Therefore, the superiority of GaN over its closest competitor, GaAs, has been proven numerically.

To visualize the GaN material based HEMT technology, Figure 2.2 is given with its main layers and materials.

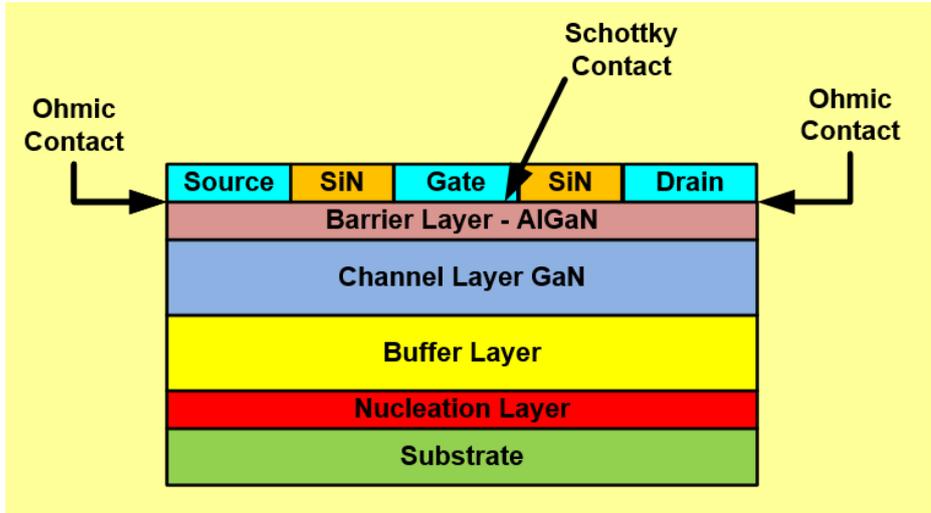


Figure 2.2: Structure of a GaN HEMT Device

2.2.2 Transistor Choice

In this design; an unmatched, discrete and 3x4 DFN-packaged GaN based high electron mobility transistor; CGHV1F006S has been chosen from Wolfspeed-Cree’s “General-Purpose Broadband” product family. According to the datasheet given, the transistor, in an open form, is suitable for the operations between DC-18 GHz frequency. On the other hand, the packaged version’s operational frequency is limited by 15 GHz due to the parasitic effects of plastic packaging. In this design, having a 14 GHz centered PA design is considered to be risky but the entire aim is to observe the behavior of the discrete design at such high frequency levels. It is hoped that an adequate gain and input/output matching performance will be obtained.

2.3 Power Amplifier Design Parameters

As briefly mentioned before, there are many PA design parameters which have influences on each other. To understand the trade-offs between them, various theoretical definitions should be made briefly and investigated one by one.

2.3.1 Operating Point / Quiescent Point / Q-Point / Bias Point

The Q-point ($I_Q - V_Q$) may be the most important parameter of a PA design since location of the Q-point on the load line determines the class of the amplifier which directly affects the main properties of the PA; efficiency, linearity etc. That’s why a designer starts with an I-V curve analysis of the chosen transistor so that the proper biasing can be applied.

For this design, $V_{drain}=+40\text{ V}$ & $V_{gate}=-2.4\text{ V}$ with $I_{drain}=81.9\text{ mA}$ has been chosen as the Q-point as shown in Figure 2.4. As shown in Figure 2.4, the transistor model provided by Cree-Wolfspeed has some missing points on the swept load lines caused by “poor convergence problem” occurred at NI AWR simulation platform. Therefore, it is recommended to examine the natural curve behavior of any GaN transistor, shown in Figure 2.3 below, expressed by another GaN specialized company Qorvo.

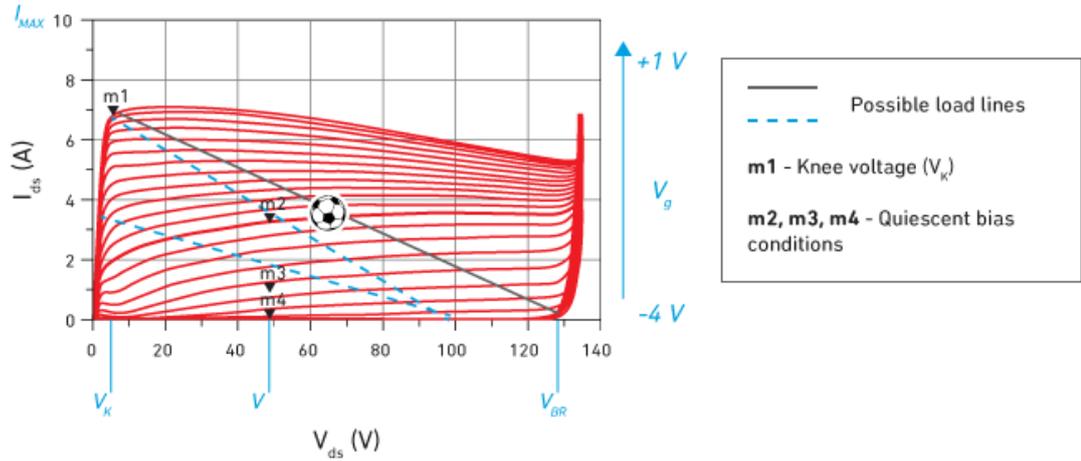


Figure 2.3: Q-Point Options on Possible Load Lines of GaN Transistor Technology by Qorvo [1]

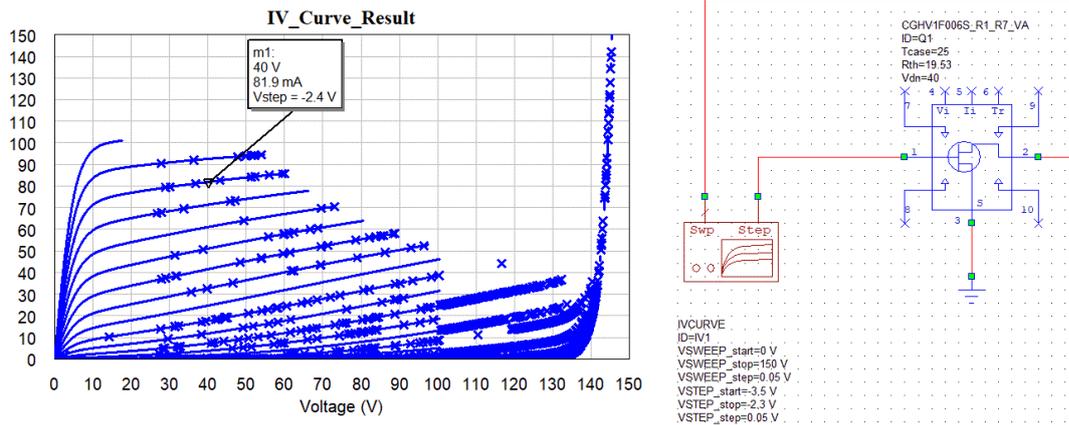


Figure 2.4: Conducted IV Curve Analysis by AWR; Schematic and Graph

2.3.2 Gain of an Amplifier (In terms of Scattering Parameters, S_{21})

The main reason of the usage of an amplifier is to obtain larger RF signal at the output than the RF signal at the input. The question of “How much larger?” can be answered with the definition of amplifier’s “gain”. There are many names and definitions for “gain”; operating gain, transducer gain, available gain, max available gain, unilateral gain, max unilateral gain etc., but for simplicity and to be understood easily, the gain of an amplifier in this work is mostly expressed with scattering parameters; S_{21} .

To achieve peak S_{21} , input and output impedances should be matched properly to achieve ideally zero input and output reflections (Γ_{IN} & Γ_{OUT}). Meanwhile, optimum source and load impedances, which have been driven from load & source pull analysis, should also be considered (Γ_{Source} and Γ_{Load}). A sample result of a load pull analysis, which has been conducted in the scope of this work, is presented in Section 2.3.4 Efficiency.

2.3.3 Max Gain and Source & Load Impedance Choice

By considering just a simple fact of circuit theory, it is known that the design of a conjugate matching circuit solves the reactance problem of impedance and helps the designer to transfer the max real power through the load. In microwave circuits, this

method is improved and extended a little bit and therefore “bi-conjugate matching” term is born, where the input and output are simultaneously conjugately matched so that transducer gain is maximized with respect to the source and load impedances. In other words, to achieve maximum gain in a PA design, optimal source and load impedances should be considered. Unfortunately, when these impedances are investigated on Smith Chart by using load/source pull analysis, single points are attained for max gain but more flexibility in the design can be achieved by sacrificing from the peak gain.

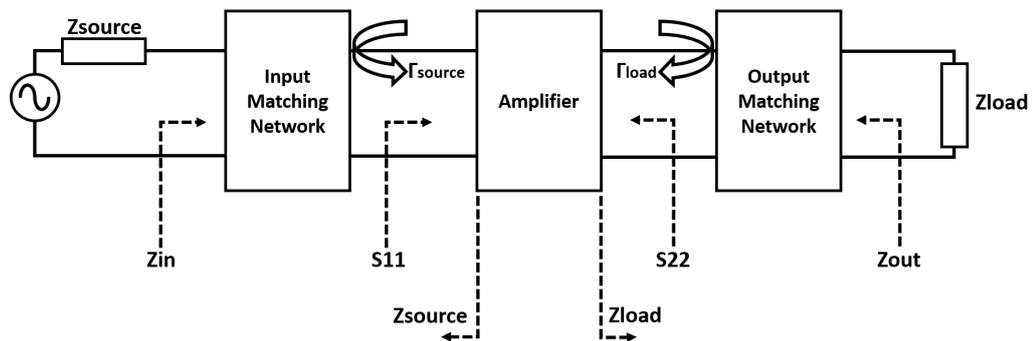


Figure 2.5: Input, Output, Source, Load Impedances and Source, Load Reflection Coefficients

2.3.4 Efficiency

While amplifying an RF signal at the input to get larger RF signal at output, laws of basic physics of course must hold. Therefore, it is known that it is not possible to get more RF power, at the output of a power amplifier, without dissipating none. This is the definition of conservation of energy for power amplifier design application. In other words, DC power (i.e. biasing) must be used to achieve more RF power. At this point, it is met with one of the most crucial parameters in PA design; efficiency. Efficiency is so important because it tells not only the energy conversion ratio from DC to RF, but also it expresses the amount of DC power dissipation as undesired heat.

In the literature, there are two different named efficiency definition even though their purpose of existence is same; “Drain Efficiency” and “Power Added Efficiency”.

2.3.4.1 Drain Efficiency

Drain efficiency is expressed by;

$$\eta_{\text{drain}} = \frac{\text{RF}_{\text{OUT}}}{\text{DC}_{\text{IN}}} \quad (2.1)$$

As can be seen from Equation 2.1, drain efficiency does not include the effect of RF_{IN} into account. So, the designer should be aware of the way of calculation.

2.3.4.2 Power Added Efficiency (PAE)

Drain efficiency analysis can be confusing or even called misleading due to the reason explained above. Therefore, another efficiency definition also be has been made; Power Added Efficiency (PAE) and expressed by;

$$\text{PAE} = \frac{\text{RF}_{\text{OUT}} - \text{RF}_{\text{IN}}}{\text{DC}_{\text{IN}}} \quad (2.2)$$

For this work, PAE is the preferred definition of efficiency.

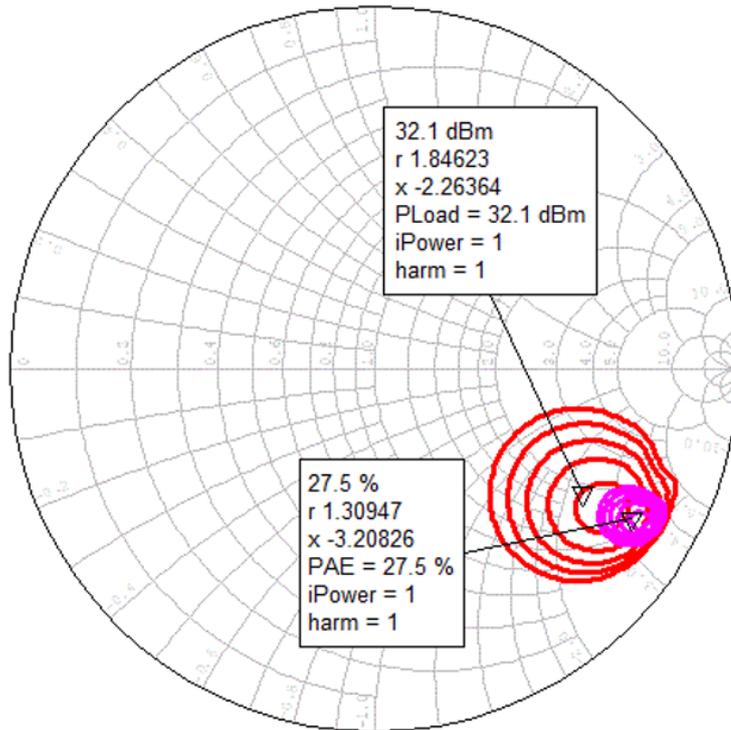


Figure 2.6: Smith Chart Load Pull Analysis by AWR and Results for Max Efficiency and Power Transferred to Load

To understand the relationship between the achievable efficiency value and the maximum power delivered to the load, which is related with chosen impedance, PAE and P_{Load} circles are drawn on Smith Chart by using AWR. As Figure 2.6 indicated, achievable maximum PAE and P_{Load} are 27.5% and 32.1 dBm, respectively. By deciding an impedance value of the design, sacrifices would be made from max P_{Load} & max PAE and other requirements such as, input & output match, linearity, stability etc. will be achieved. This is another proof that PA design is an iterative process.

2.3.5 Linearity & Output Power

Output power (P_{OUT}) and linearity are closely related parameters in PA design. For instance, if a designer's ultimate goal was achieving highest power at the output, working linear or nonlinear region does not matter, which may result deprivation from linearity while driving the amplifier so close to the saturation point (P_{SAT}). On the other hand, if the main purpose is to get an amplifier which works in linear region,

two terms appear; P_{1dB} and $IP3$, which limits the magnitude of the RF signal at the output. To simulate the behavior of the amplifier in terms of linearity & maximum output power and find out P_{1dB} , $IP3$ and P_{SAT} points, different types of excitation ports and different frequency sweep options are used. Those port types are shown in Figure 2.7.

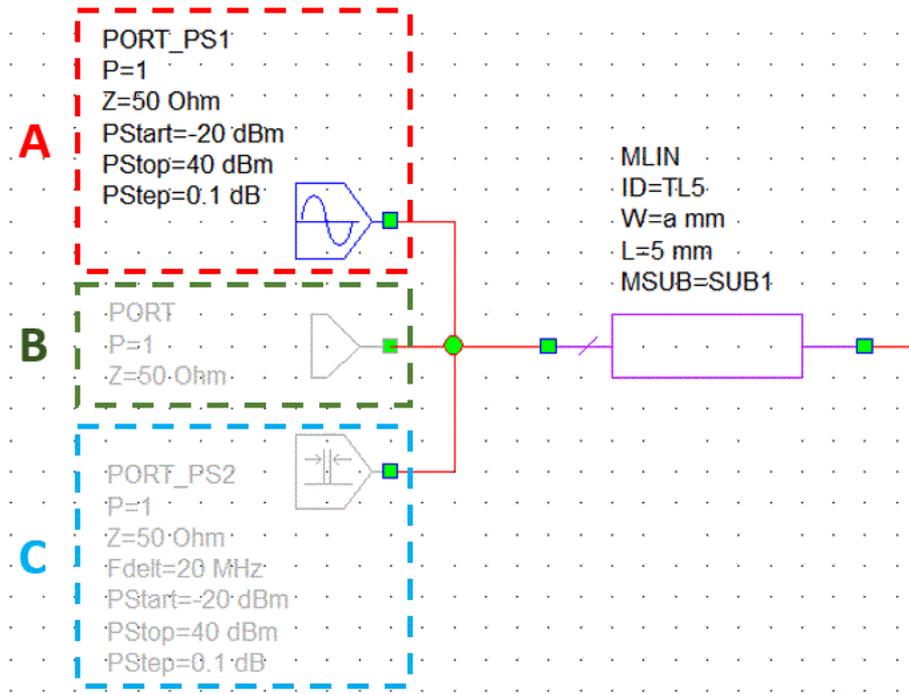


Figure 2.7: Port Types Used for Various Parameter Simulations in AWR, A: P_{1dB} and P_{SAT} Simulation, B: S-Parameter Simulation, C: $IP3$ Simulation

Configuration Port A: Port A (marked with red dashes) is used to simulate P_{1dB} and P_{SAT} points. The frequency of excitation is kept constant and equal to the fundamental frequency of the project for this port. This type of port helps to sweep single tone RF input signal's power level starting from P_{Start} dBm up to P_{Stop} dBm. In addition, increment size of the input power can be controlled by P_{Step} . To simulate and find out the locations of these points accurately, P_{Step} is chosen small as 0.1 dB. Lastly, the termination impedance can also be adjusted to any value desired but to prevent unexpected return losses, 50 Ohm is chosen as the microstrip line's.

Configuration Port B: Port B (marked with green dashes) is the simplest port form of NI AWR simulation platform, the designer can not play with the power level or the frequency of RF input signal. This port is practical for creating correct schematics to simulate S-parameters in small signal conditions. Only the value of termination impedance can be changed for this type. A small change on settings of this type of port (changing the port type "termination" to "source") allow designer to assign constant, user dependent power level. This property has been used for observing harmonic distortions (HD_2 , HD_3 etc.) for different RF input powers.

Configuration Port C: Port C (marked with blue dashes) is the most complex port configuration among Port A, B and C. This port allows to apply two tone excitation with a delta F frequency separation. By doing so, third order or higher level of inter modulation distortions can be simulated and IP3 point can be estimated by sweeping the power level of RF input as done for configuration "Port A".

2.3.5.1 P_{1dB} & P_{SAT}

To analyze linearity behavior of the amplifier and find out the exact locations of P_{1dB} (1 dB compression point) and P_{SAT} (saturation point), port "A" shown in Figure 2.7 is used and the frequency setting of the simulation is adjusted to a single frequency (tone) which is the center frequency of the operational bandwidth; 14 GHz. By using port "A" the input RF power is swept from -20 dBm to +40 dBm with 0.1 dB steps so that the linear and nonlinear working regions can be observed with the degradation of gain. It is known that where small signal operation is not valid anymore, the gain of the amplifier will start to decrease. When the compression on the gain is equal to 1 dB, P_{1dB} point would be found. Likewise, when the input power is continued to increase more and more, the amplifier would be saturated and the P_{SAT} point, where the amplifier couldn't provide any gain, would be achieved. The main points on the result of the simulation for P_{1dB} and P_{SAT} shown in Figure 2.8.

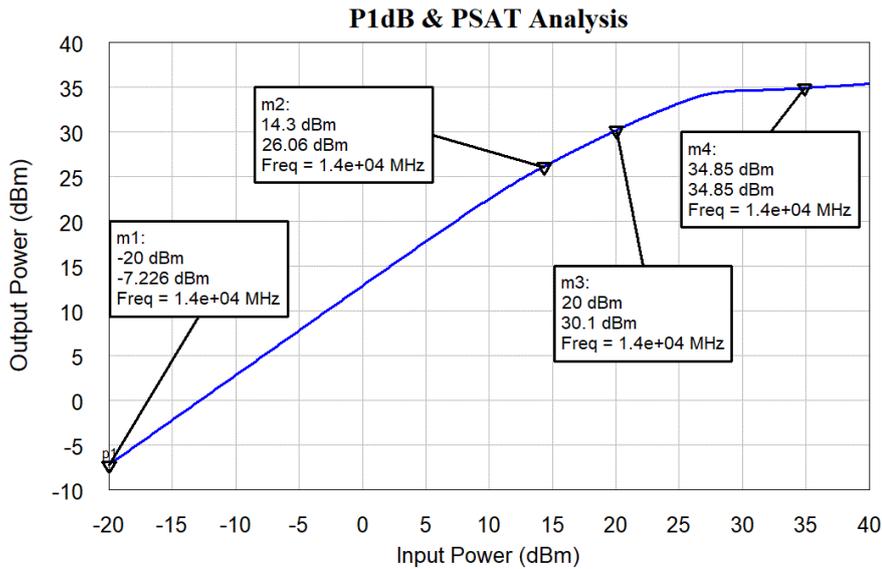


Figure 2.8: P_{1dB} and P_{SAT} Analysis of the Power Amplifier Designed by AWR

m1: The point where the amplifier is driven by smallest RF input power. At this RF input level, the amplifier works so linear. -20 dBm input power is applied and -7.226 dBm output power is achieved. The gain is around; $-7.226 \text{ dBm} - (-20 \text{ dBm}) = 12.774 \text{ dB}$

m2: One of the critical points, because at this point the gain of the amplifier is equal to; $26.06 \text{ dBm} - 14.3 \text{ dBm} = 11.76 \text{ dB}$ The value of gain tells that the gain is compressed by 1 dB. Therefore, this point is called P_{1dB} .

m3: Apart from many theoretical definitions, it is needed to define a practical, realistic input RF power for the PA. GaN-HEMT based power amplifiers which works in nonlinear region are preferred mostly to get higher efficiency. When the gain is analyzed; $30.1 \text{ dBm} - 20 \text{ dBm} = 10.1 \text{ dB}$

The gain seems acceptable for the purpose of this work cause 30 dBm output power is exceeded while the gain is compress just around 2.7 dB from the peak gain value, expressed via m1 point in Figure 2.8.

m4: Saturation point, P_{SAT} . 34.85 dBm input power is applied and same power is obtained at the output. In other words, gain is equal to 1.

2.3.5.2 Harmonic Distortions (HD_2, HD_3, \dots, HD_n)

"Harmonic distortions" are defined as the generation of undesired harmonic signals which occur exactly at the multiples of the fundamental signal. In other words, the term called HD_1 is actually the fundamental output signal of the amplifier whose frequency value is f_0 . As the level of single-tone RF input is increased, non-linearity behaviour of the amplifier gets stronger and stronger. As a result, second (at $2f_0$), third (at $3f_0$) or higher order harmonic distortions start to grow, consecutively.

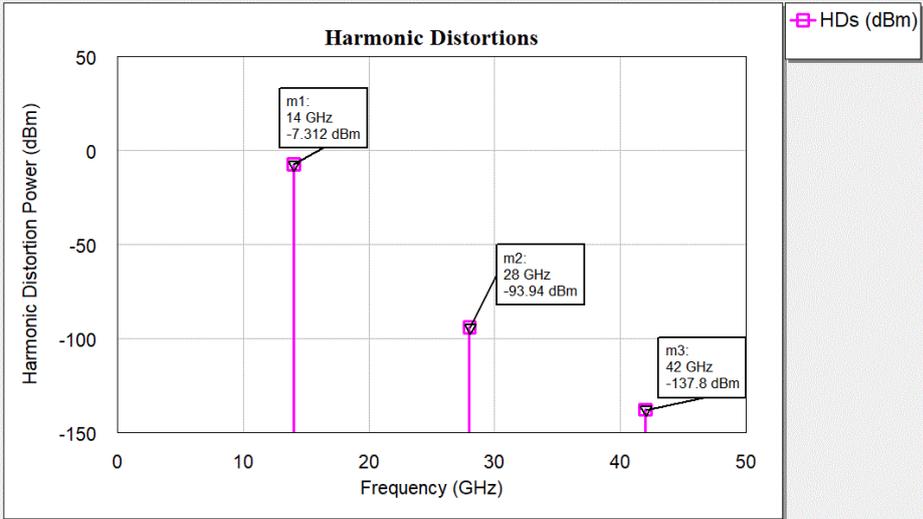


Figure 2.9: Input Power = -20 dBm, HD Analysis Conducted by AWR

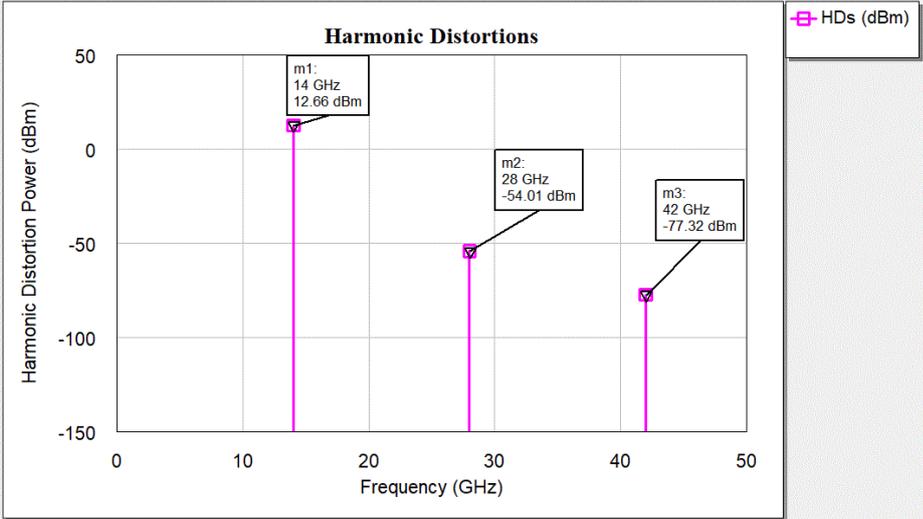


Figure 2.10: Input Power = 0 dBm, HD Analysis Conducted by AWR

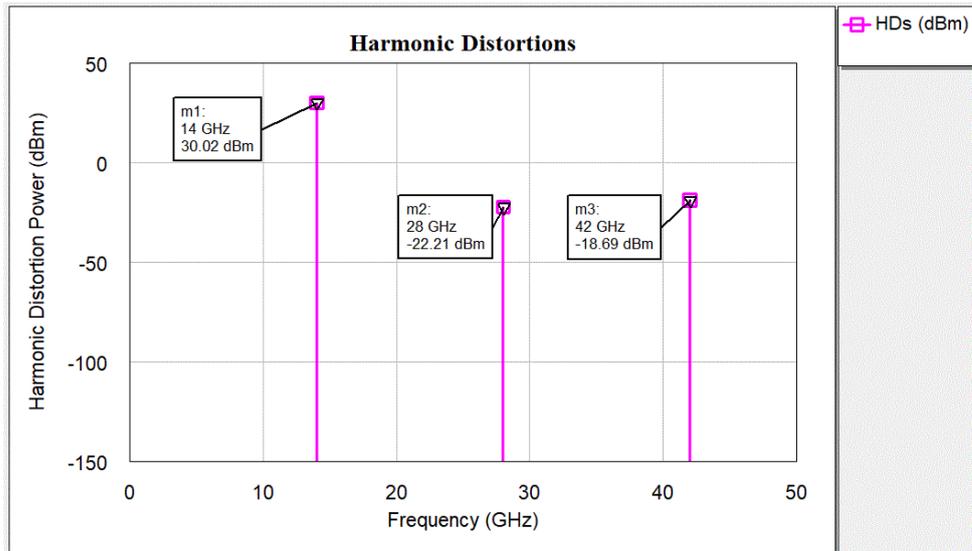


Figure 2.11: Input Power = +20 dBm, HD Analysis Conducted by AWR

The change at the power levels of harmonic distortions, when the input power has been increased, are summarized at Table 2.2.

Table 2.2: HD Power Level Changes w.r.t RF Input Power

RF Input Power (dBm)	HD₁ @ 14 GHz (Fundamental Signal) (dBm)	HD₂ @ 28 GHz (Second Harmonic) (dBm)	HD₃ @ 42 GHz (Third Harmonic) (dBm)
-20	-7.312	-93.94	-137.8
0	12.66	-54.01	-77.32
20	30.02	-22.21	-18.69

As values in Table 2.2 indicates, when the input power level is increased by 20 dB each time, similar growth has been observed at fundamental output signal level (i.e. HD₁), while the increase at the power levels of HD₂ and HD₃ occur much more. In fact, HD₃ magnitude becomes larger than HD₂ after some specific value of input power.

2.3.5.3 Third Order Intercept Point (IP3)

Another design parameter that helps to understand the linearity performance of a PA is called IP3, third order intercept point. IP3 can be summarized as the point where the fundamental output signal's magnitude is equal to the magnitude of the third order intermodulation (IMD_3).

IMD_3 point is very crucial in the design because different than the harmonic distortions (HDs), intermodulation distortions (IMDs) are defined as “in-band” undesired signals at the output and they can not be filtered out easily. Therefore, behaviour of intermodulation components should be simulated at first, so that the precautions could be made.

The only way to conduct the simulation for IMD_3 , IMD_5 or etc. is possible by applying a “two-tone” test. Different than the P_{1dB} simulation, two tone with a specific Δf are applied to the input. To achieve that, configuration of "port C" shown in Figure 2.7 is enabled in the simulation and again different power levels are swept differently than harmonic distortion simulation this time by applying "two-tone".

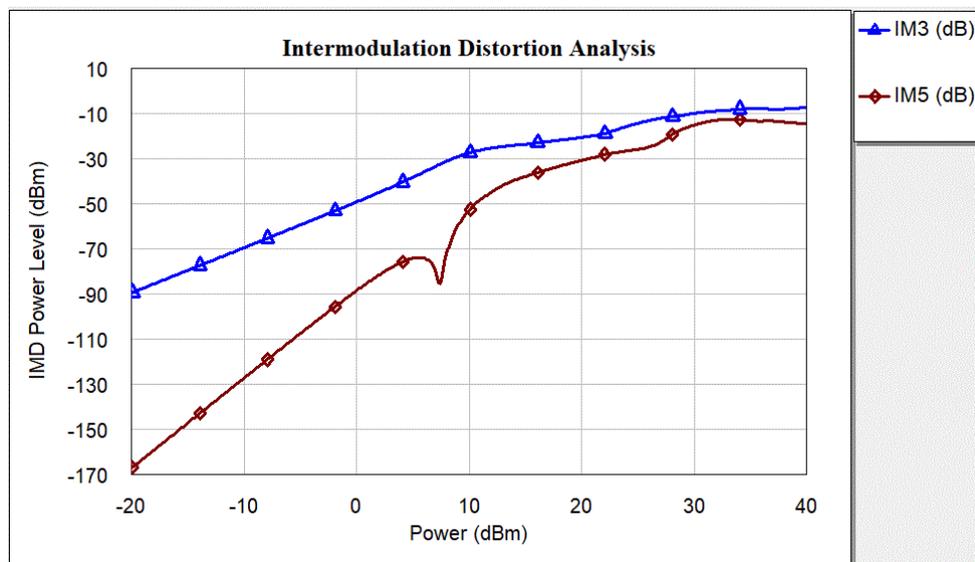


Figure 2.12: IMD Analysis Conducted by AWR

As Figure 2.12 indicates, as the input power level shown in x-axis is increased, the magnitudes of IMD_3 and IMD_5 have grown up rapidly. The rate of increase is directly related with the slope of them. The slope for IMD_3 can be called 3 times larger than fundamental signal, where the similar relationship is valid for IMD_5 ; 5 times bigger slope than the fundamental signal. Therefore, theoretically interception of any IMD's power with the power level of fundamental signal is inevitable if the input is increased without stopping. Due to the distortion on IMD_3 curve shown in Figure 2.12, it is hard to tell the exact point of IP3 but a logical prediction for IP3 would be around 24-25 dBm. This value can be determined and understood easily if the slope of the curve of IMD_3 in Figure 2.12 would be kept almost constant. This value is also supported by general "10 dB difference" relation between IP3 and P_{1dB} .

2.3.6 Stability

Stability is probably the most important term in a PA design. The importance of the stability can be explained by the words of an experienced designer said once "if a PA designer wouldn't consider the stability criteria from the beginning of the design period, most likely there will be an oscillator design completed, not a PA". To avoid such a catastrophic result, two different stability definitions have been made; "Unconditionally Stable" and "Conditionally Stable".

2.3.6.1 Unconditionally Stable

For this type of stability condition, the PA works stable for all frequencies, which is the most desired scenario. On the other hand, for most cases, achieving this condition causes degradation on other design parameters. For this type of stability, in the analysis part, it would be observed that the stability circles does not cross the Smith Chart.

2.3.6.2 Conditionally Stable

As many power amplifiers available in the market, the design of this study works as “conditionally stable”, which means that some frequencies should be avoided to prevent instability. The design has been built for this work, has a stability circuit consisting of a capacitor in parallel with a resistor at the gate bias network as shown in Figure 2.13. Although the stability circuit ensures a safe operation at the center frequency of the design, 14 GHz, and close frequencies, it does not guarantee the stability for all frequencies, which is the reason of the emphasis on “conditional”.

There are many stability parameters; K , B_1 , μ_{u1} , μ_{u2} . Even though all of them indicates the status of the stability, theoretically they have slight differences. Therefore, choosing only one of those parameters as reference and expressing the stability, would not be sufficient. Figure 2.14 shows all four stability parameters of the final design in a frequency range starting from DC to 30 GHz.

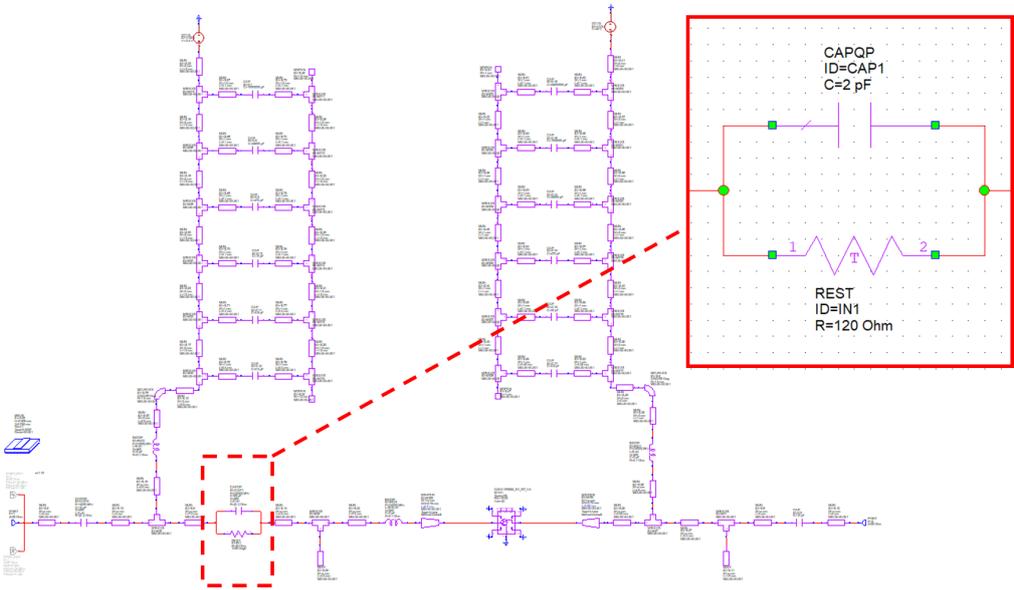


Figure 2.13: R-C Stability Network Used in Final Design

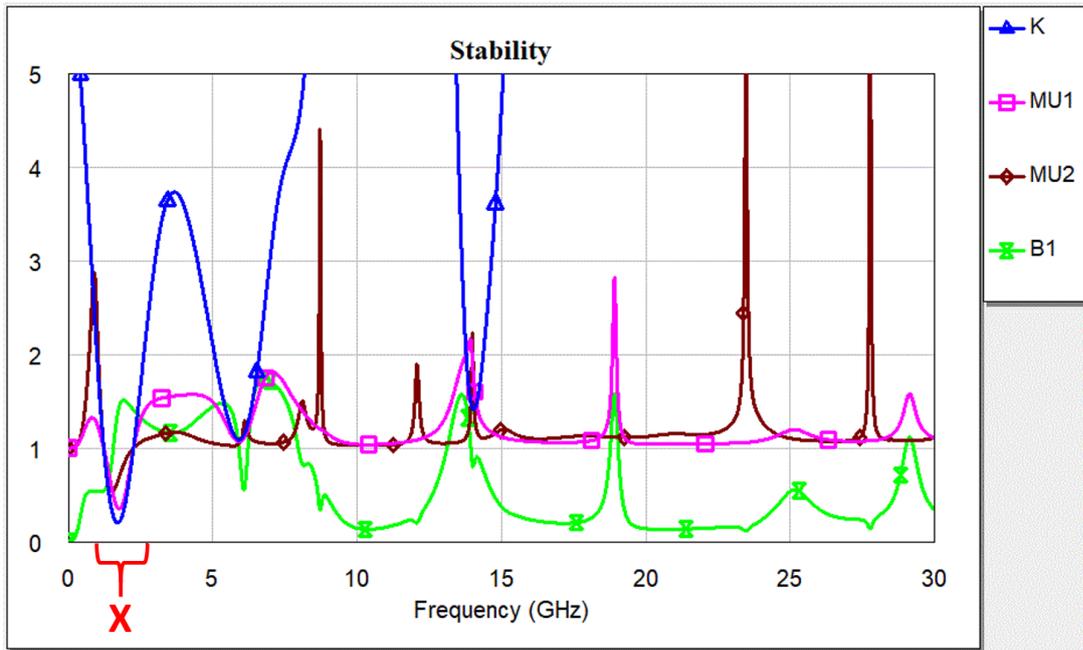


Figure 2.14: Stability Analysis Conducted by AWR

Briefly, the definitions for stable operation are stated as; $K > 1$, $Mu_1 > 1$, $Mu_2 > 1$ and lastly $B_1 > 0$. As “red colored X” mark in Figure 2.14 indicates that the conditions summarized are not hold for those frequencies between 1.29 GHz and 2.259 GHz.

CHAPTER 3

DESIGN AND SIMULATION RESULTS

In this chapter, power amplifier design process has been explained with all sub-networks and simulation results. From beginning to the end, the design process has mainly two stages.

- Early Design with Ideal Lumped Elements
- Improved Final Design with both Distributed and Non-Ideal Elements

Before going into the details of these design stages, it should be better to look at a basic PA design with its main sub-circuits, which has been illustrated in the block diagram in Figure 3.1.

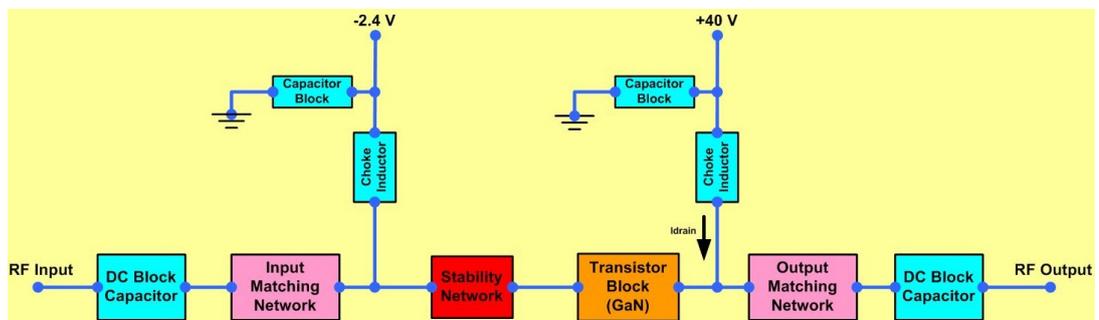


Figure 3.1: Block Schematic Power Amplifier with All Sub-Networks

Function of each block, shown in Figure 3.1, have been explained briefly one by one:

DC Block: This part is just made by a single capacitor to block any DC from RF ports. There are two of them, one at the input RF port and the other is at the output of the design.

Input Matching Network: It is one of the most important sub-circuits of the design with output matching network. It may consist many types of elements; shunt/series capacitors, shunt/series inductors, shunt/series resistors, open/short stubs etc. For having a good value of input return loss and for achieving a successful power transfer to the load, input matching network plays a crucial role.

RF Choke: It is an inductor used for leading the RF signal through the gate of the transistor and blocking any noise coming from the DC sources; drain or gate. Larger the inductor value means more noise rejection due to the high impedance seen from the drain or gate. There are actually two of them used in the design; one at the gate bias, the other at the drain. An RF choke inductor may be used as a part of the matching networks at the input or the output, as used in this work.

Filtering Block: It consist of many AC ripple/noise filtering capacitors with different values depending on the frequency that is wanted to be filtered out. They must be used at both gate and drain DC supply parts.

Stability Network: This network can be built by various types of configurations, but for this design, a parallel RC circuit (series to the gate) has been chosen.

Transistor: The heart of the design, it is the part that has junction and provides the amplification ability on RF input signal. Chosen transistor technology is so effective at the behavior of the amplifier, for this work a GaN-HEMT technology has been preferred.

Output Matching Network: It has the same function and properties with input matching network, the only difference that it is located at the output part. On the other hand, any change or addition at the output for building an output matching circuit affects the input matching performance. Therefore, many iterations should be made both at the input and the output matching circuits until adequate S_{11} and S_{22} values are obtained.

3.1 Early Design with Ideal Lumped Elements

An early design has been completed with ideal, lumped circuit elements. In other words, all components are assumed to be lossless, frequency independent, noiseless and work perfectly linear. In addition, microstrip transmission lines for connecting the circuit elements on a real, manufactured PCB were not included at this stage. Even though the first design is referred to “early design”, it has some advantageous features too since the relationship of design parameters, which has been explained in the previous chapters, is considered carefully and theory has been applied successfully. For instance a proper bias and a good matching circuit, which has been derived from the outcomes of load pull test, have provided a remarkable value of gain. Figure 3.2, shows the early circuit design with all elements, which corresponds to the elements of block diagram shown in Figure 3.1.

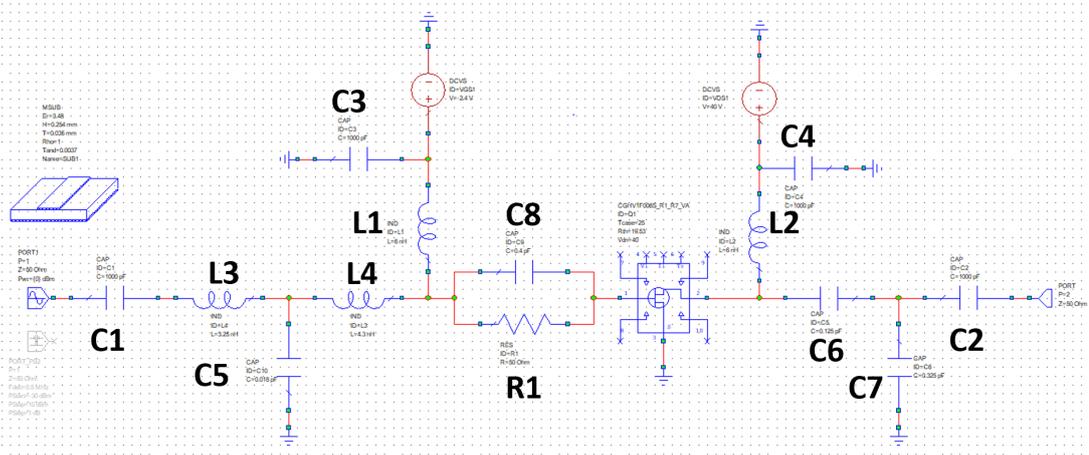


Figure 3.2: Schematic of Early Design with Ideal Lumped Elements

Table 3.1: Values of the Lumped Elements of Early Design

Parameter	Function	Value
C1	DC Block Capacitor	1000 pF
C2	DC Block Capacitor	1000 pF
C3	Noise Filtering Capacitor	1000 pF
C4	Noise Filtering Capacitor	1000 pF
L1	RF Choke Inductor / Part of Input Matching Network	6 nH
L2	RF Choke Inductor / Part of Output Matching Network	6 nH
L3	Part of Input Matching Network	3.25 nH
C5	Part of Input Matching Network	0.018 pF
L4	Part of Input Matching Network	4.3 nH
C8	Part of Stability Network	0.4 pF
R1	Part of Stability Network	50 Ohm
C6	Part of Output Matching Network	0.125 pF
C7	Part of Output Matching Network	0.325 pF

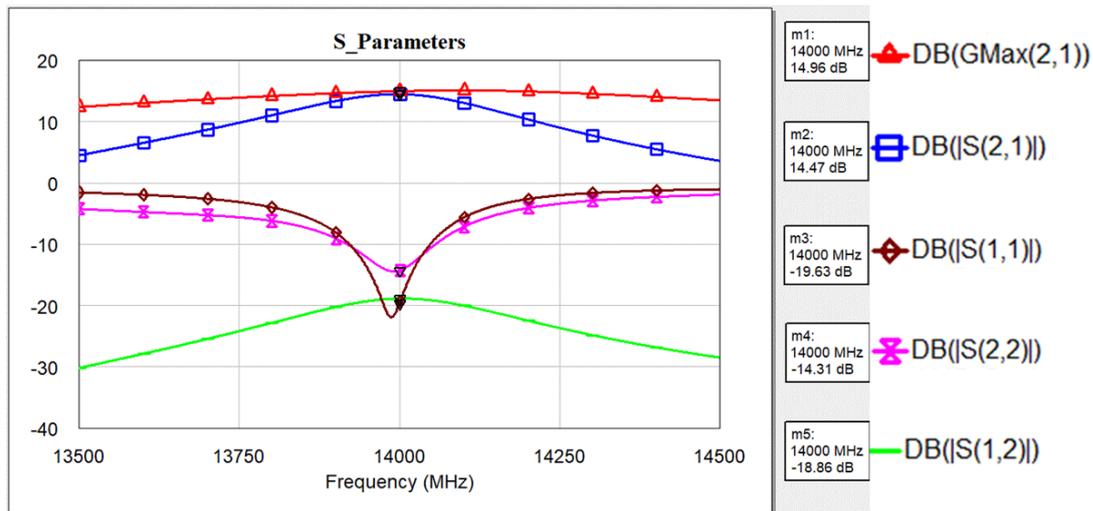


Figure 3.3: S-Parameters of Early Design with Ideal Lumped Elements

Table 3.2: S-Parameters of Early Design at Center Frequency

Parameter	Definition	Value (@14 GHz)
$\max(S_{21})$	Achievable Max Gain	14.96 dB
S_{21}	Gain	14.47 dB
S_{11}	Input Return Loss	-19.63 dB
S_{22}	Output Return Loss	-14.31 dB
S_{12}	Input-Output Isolation	-18.86 dB

Table 3.1 shows the lumped element's values used in early design, which has been exhibited in Figure 3.2. As clearly seen from capacitor and inductor values, the numbers for DC blocking and noise filtering capacitors are roughly determined and some of the SMD values (like $C_5=0.018$ pF) are impossible to put into practice. Such problems are investigated in detail and have been overcome in the following design stages by necessary replacements. At this level, response of scattering parameters, which is shown in Figure 3.3 and values indicated in Table 3.2, seems promising. This statement can be verified by the negligible difference between S_{21} achieved and $\max(S_{21})$, where $\max(S_{21})$ is defined as the maximum transducer power gain for an unconditionally stable two port circuit.

3.2 Improved Final Design with both Distributed and Non-Ideal Lumped Elements

As the next step, the early design has been improved by both; “replacing the ideal lumped elements with non-ideal ones” and “including distributed circuit elements”.

Non-ideal lumped elements are referred to the realistic models provided by SMD manufacturers. These models consist noise, loss (parasitic effects) while performing temperature and frequency dependent behaviors. Finally, none of the models works perfectly linear as observed in real life. An example of the replacement of ideal lumped elements with non-ideal ones has been shown in Figure 3.4.

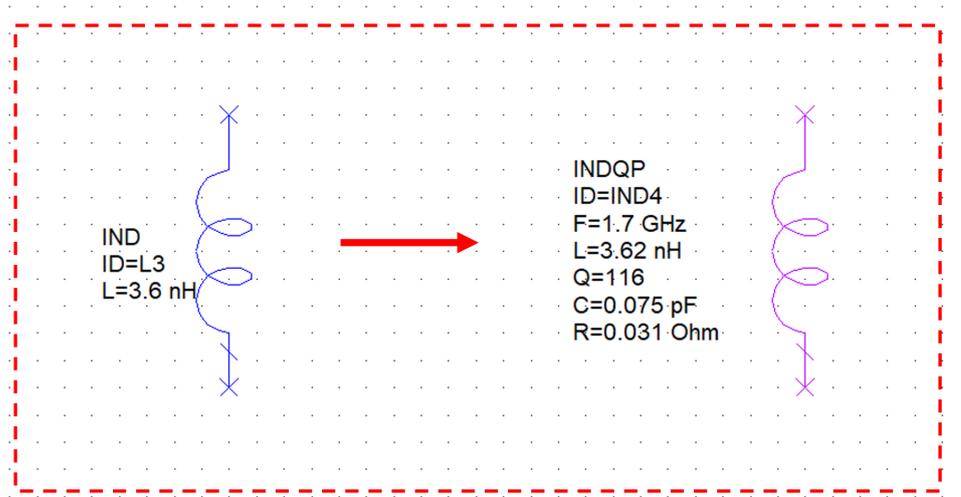


Figure 3.4: Schematic Showing the Replacement of Ideal Elements with Non-ideal Elements

The conversion in Figure 3.4 is based on one of the inductor models of Coilcraft; 0603HP-3N6X_E. The inductor on the left shows the ideal model while the inductor on the right exhibits the realistic, non-ideal inductor. When two inductor model is investigated, it will be observed that the model called INDQP has many parameters.

- “F” means frequency at which L, Q and R specified. For this inductor example, those values are expressed for the frequency value of 1.7 GHz.
- “L” refers to the actual, measured inductance value. Instead of ideal inductance value, which was 3.6 nH, it is measured as 3.62 nH.
- “Q” corresponds to quality factor.
- “R” is the series resistance. In real life, it is impossible to have a zero resistance for an inductor or a capacitor cause there is no "ideal" component in practice. Relatively, if the resistance could be zero, the quality factor of the component would be infinite because it is known that;

$$Q = \frac{\omega L}{R} \quad (3.1)$$

- “C” is the unwanted, parasitic capacitance value. This value is so crucial for the inductors used in high frequency applications due to the SRF limitation. Parasitic capacitance, C, determines self-resonance frequency (SRF) value together with L. If a designer does not care SRF value, the inductor used in the design may behave as a capacitor if SRF value is exceeded. C value in Figure 3.4 is determined by the SRF value given.

$$\text{SRF} = \frac{1}{2\pi\sqrt{LC}} \quad (3.2)$$

Since SRF is given as 9.7 GHz in Coilcraft’s datasheet, C is calculated as approximately 75 fF. For this work, while choosing the components, having SRF > 14 GHz is taken into consideration.

Distributed elements are simply microstrip lines for connecting surface mounted components on a printed circuit board. On the other hand, in this work they are also modelled and used as part of input and output matching circuits. Similar usage of microstrip lines can be encountered in many designs in the literature. Width of a microstrip line with dielectric constant and thickness of the substrate determine the characteristic impedance of the line.

For this work, Rogers4003C substrate with dielectric constant (ϵ) of 3.48 and thickness of 0.508 mm (h) has been used. Consequently, the microstrip line thickness has been chosen as $w = 1.13$ mm (Illustrated in Figure 3.5) after a proper calculation for achieving 50 Ohm characteristic impedance.

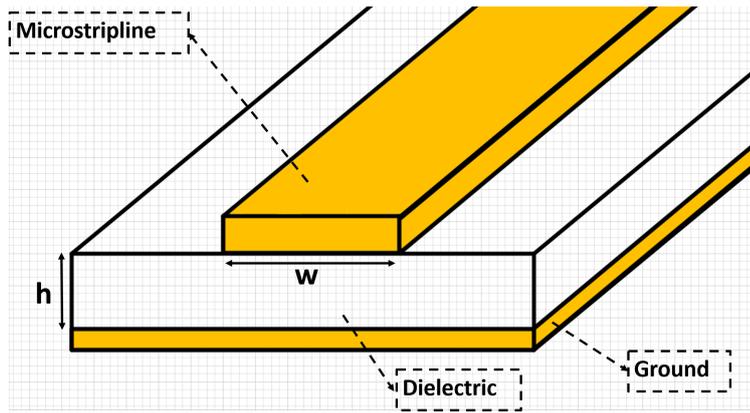


Figure 3.5: Microstrip Line-Dielectric Structure with Important Design Parameters

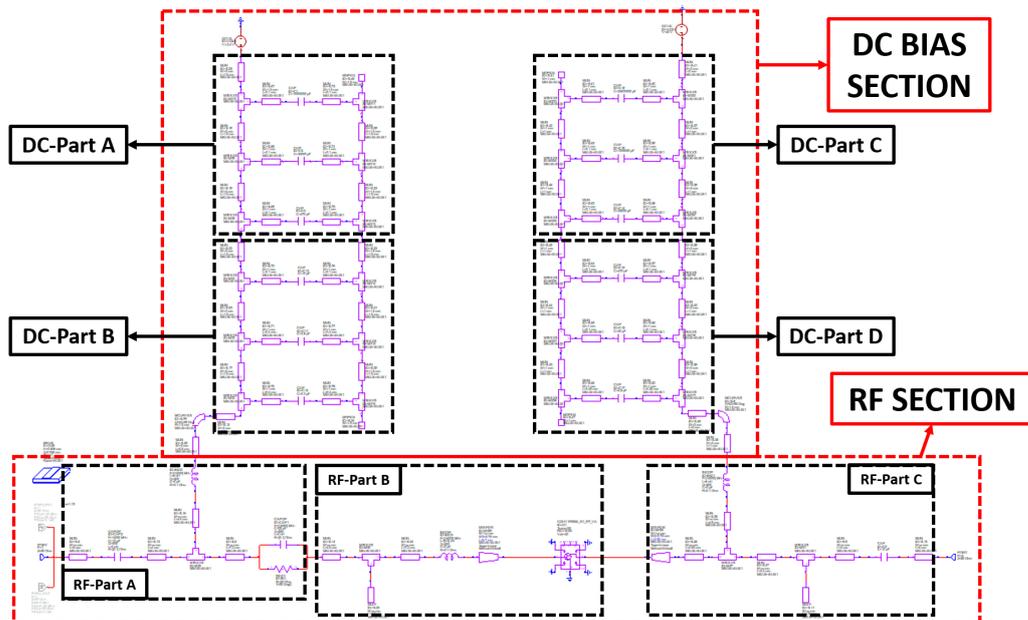


Figure 3.6: Schematic of Improved Final Design with both Distributed and Non-Ideal Lumped Elements

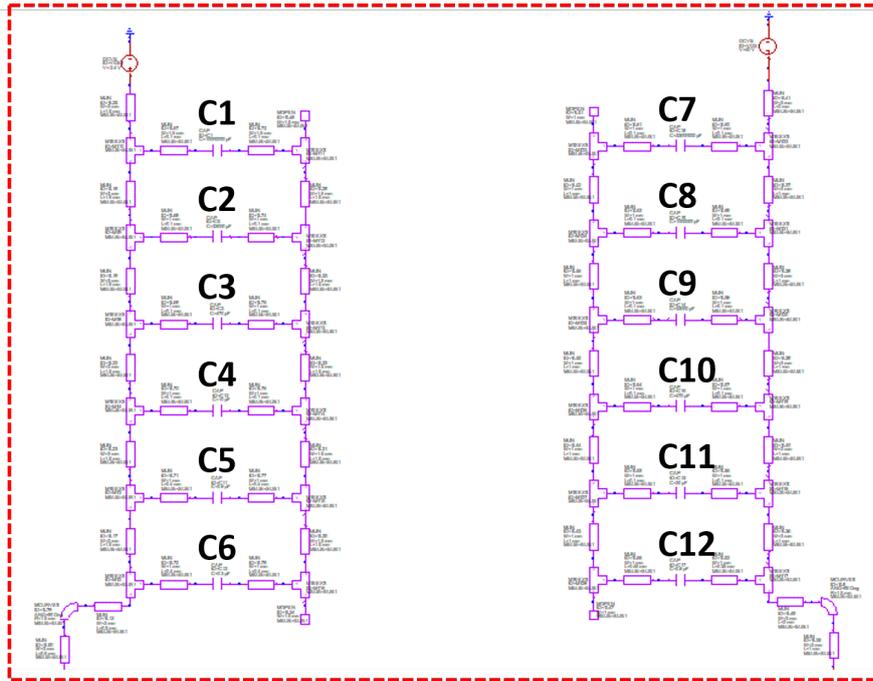


Figure 3.7: DC Section of Improved Final Design with Non-Ideal Lumped Elements

Table 3.3: Values of the Lumped Elements of DC Section of Improved Final Design

Parameter	Function	Value
C1	Noise Filtering Capacitor	10 uF
C2	Noise Filtering Capacitor	33 nF
C3	Noise Filtering Capacitor	470 pF
C4	Noise Filtering Capacitor	10 pF
C5	Noise Filtering Capacitor	0.8 pF
C6	Noise Filtering Capacitor	0.3 pF
C7	Noise Filtering Capacitor	33 uF
C8	Noise Filtering Capacitor	1 uF
C9	Noise Filtering Capacitor	33 nF
C10	Noise Filtering Capacitor	470 pF
C11	Noise Filtering Capacitor	20 pF
C12	Noise Filtering Capacitor	0.8 pF

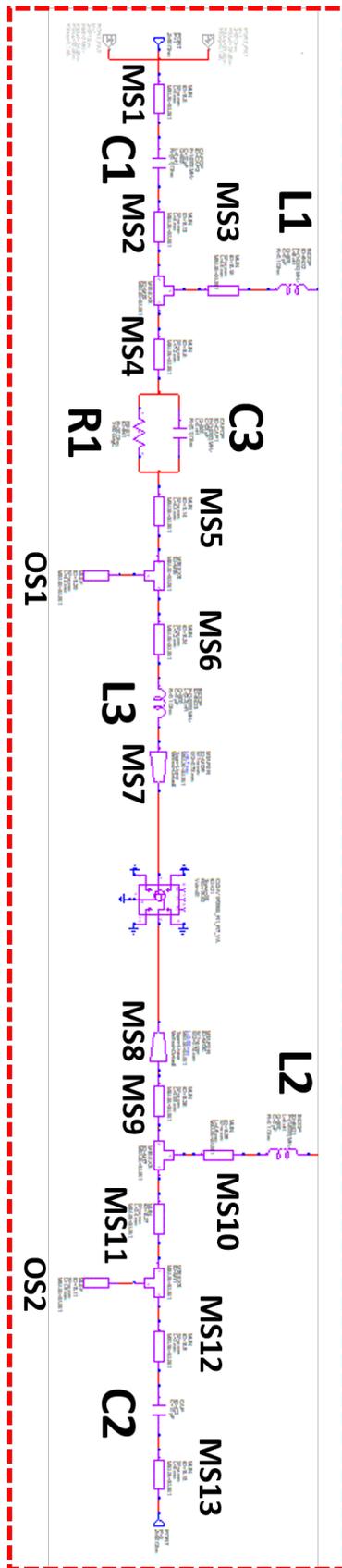


Figure 3.8: RF Section of Improved Final Design with Non-Ideal Lumped Elements

Table 3.4: Values of the Lumped and Distributed Elements of RF Section of Improved Final Design

Parameter	Function	Value
C1	DC Block Capacitor	10 pF
C2	DC Block Capacitor	10 pF
C3	Part of Stability Network	2 pF
R1	Part of Stability Network	120 Ohm
L1	RF Choke Inductor / Part of Input Matching Network	6 nH
L2	RF Choke Inductor / Part of Output Matching Network	6 nH
L3	Part of Input Matching Network	2.2 nH
OS1	Open Stub with width equals to 1.13 mm (Part of Input Matching Network)	L = 4.5 mm
OS2	Open Stub with width equals to 1.13 mm (Part of Output Matching Network)	L = 1.9 mm
MS1	Microstrip Line with width equals to 1.13 mm	L = 5 mm
MS2	Microstrip Line with width equals to 1.13 mm	L = 4 mm
MS3	Microstrip Line with width equals to 1.13 mm	L = 4.6 mm
MS4	Microstrip Line with width equals to 1.13 mm	L = 7.3 mm
MS5	Microstrip Line with width equals to 1.13 mm	L = 4.6 mm
MS6	Microstrip Line with width equals to 1.13 mm	L = 7.2 mm
MS7	Tapered Microstrip Line with width of w1 and w2 equals to 1.13 mm and 0.75 mm, respectively	L = 6.7 mm
MS8	Tapered Microstrip Line with width of w1 and w2 equals to 1.13 mm and 0.75 mm, respectively	L = 2.55 mm
MS9	Microstrip Line with width equals to 1.13 mm	L = 0.05 mm
MS10	Microstrip Line with width equals to 1.13 mm	L = 4.8 mm
MS11	Microstrip Line with width equals to 1.13 mm	L = 2.4 mm
MS12	Microstrip Line with width equals to 1.13 mm	L = 3 mm
MS13	Microstrip Line with width equals to 1.13 mm	L = 5 mm

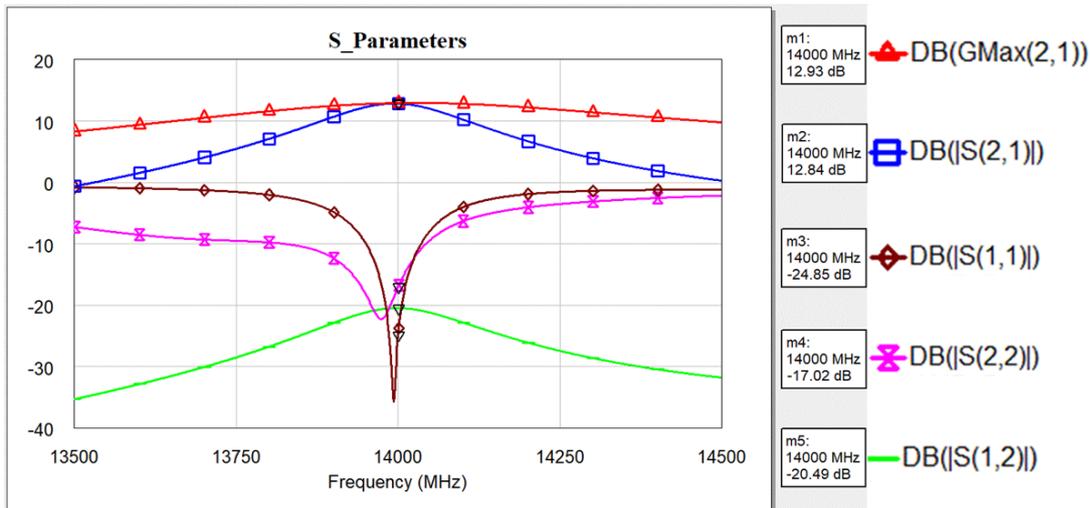


Figure 3.9: S-Parameters of Improved Design with both Distributed and Non-Ideal Lumped Elements

Table 3.5: S-Parameters of Improved Design at Center Frequency

Parameter	Definition	Value (@14 GHz)
$\max(S_{21})$	Achievable Max Gain	12.93 dB
S_{21}	Gain	12.84 dB
S_{11}	Input Return Loss	-24.85 dB
S_{22}	Output Return Loss	-17.02 dB
S_{12}	Input-Output Isolation	-20.49 dB

After all the changes applied to the design, the response of the S-parameters has been preserved. Therefore, a very similar behavior to early design has been achieved after so many iterations on design parameters, as shown in Figure 3.9. To be more accurate about the final design's response, values on Table 3.5 can be investigated. Numerical results indicate a slight decrease on the gain (S_{21}) of the amplifier by approximately 1.7 dB even though the input and output return loss (S_{11} & S_{22}) with isolation (S_{12}) are improved. Such a small decrease on gain actually is an expected scenario due to the inclusion of insertion loss by addition of many microstrip lines.

Table 3.6 is given for a complete S-parameter comparison of early and final design. If two designs are compared, it will be realized that the number of used SMDs has been decreased due to the addition of microstrip lines. Some of the lumped components in early design, whose values are impossible to achieve with current SMD technology available in the market, are replaced with stubs which are made by again microstrip lines.

Table 3.6: S-Parameters Comparison of Early and Improved Designs

Parameter	Definition	Early Design Value @14 GHz	Final Design Value @14 GHz
$\max(S_{21})$	Achievable Max Gain	14.96 dB	12.93 dB
S_{21}	Gain	14.47 dB	12.84 dB
S_{11}	Input Return Loss	-19.63 dB	-24.85 dB
S_{22}	Output Return Loss	-14.31 dB	-17.02 dB
S_{12}	Input-Output Isolation	-18.86 dB	-20.49 dB

After determining "lengths of microstrip lines" and "values of SMDs" belonging to RF section, shown in Table 3.4, biasing part (DC section) is also designed with proper microstrip elements with noise/ripple filtering capacitors. Theoretically, this addition has no impact on RF response of the circuit. Therefore, the lengths of the microstrip lines at the DC section is not given, only the lumped elements' values are given in Table 3.3 to show that the SMDs can be procured. Figure 3.10 is showing the final layout in both two dimensional (2D) and three dimensional(3D) views. As can be noticed, connectors for DC biasing, RF input and output are not included at this version of layout.

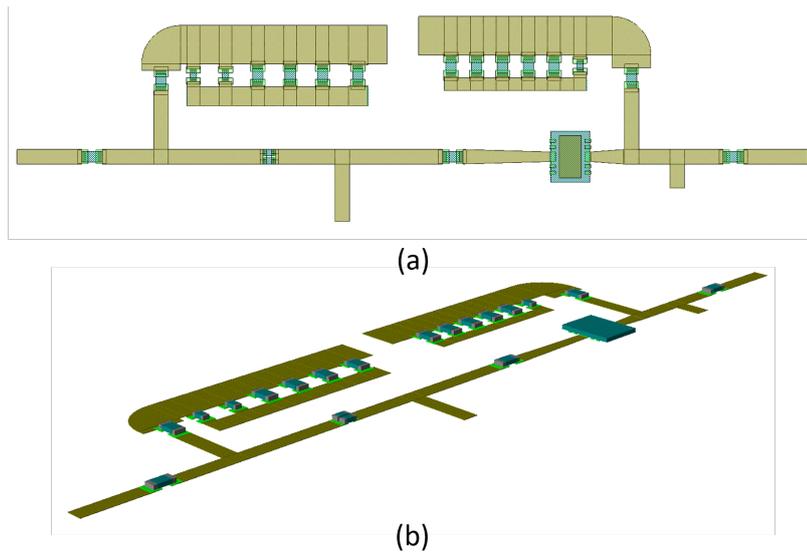


Figure 3.10: (a) 2D and (b) 3D Layout of Final Design with both Distributed and Non-Ideal Lumped Elements on AWR

3.3 PCB Layout by ALTIUM

The layout made in AWR has been exported to ALTIUM and the missing connectors are added with realistic models created in ALTIUM. Completed layout is shown in the Figure 3.11.

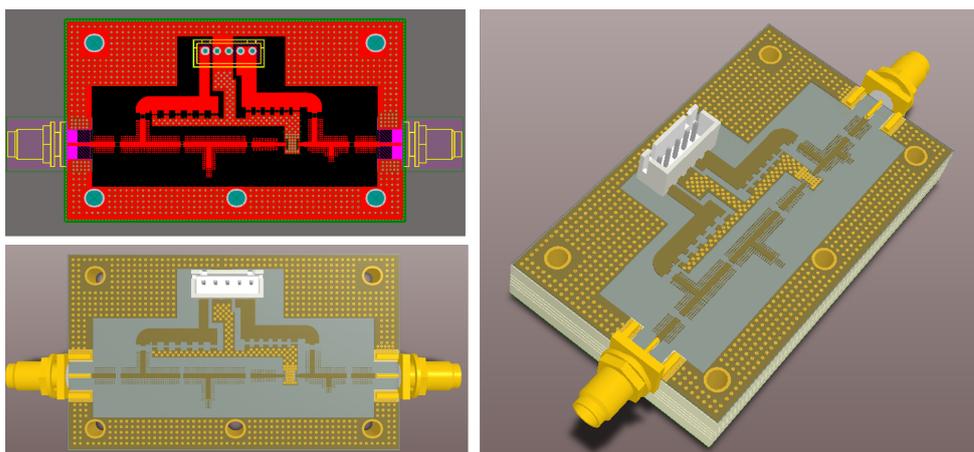


Figure 3.11: 2D and 3D Layout of Final Design without SMDs via ALTIUM

Along both side of microstrip lines of RF section, 200 μm x 200 μm sized copper cells (The size of cells is determined according to the sensitivity of etching ability of LPKF Protomat S103.) have been added in ALTIUM. These cells' main purpose is to provide the flexibility for post process. After observing the measurements, cells would be used for tuning optimization. Depending on different cases, they can be used to obtain tapered lines, to increase the length or width of a microstrip stub etc. with proper soldering. Ku band can create unwanted and unexpected behaviours that are contrary to the simulation results, due to the nature of working with high frequencies. Unexpected behaviour can be a frequency shift or an impedance distortion and these cells are going to help the designer to deal with such bad scenarios. Detailed picture about the cells is given in Figure 3.12.

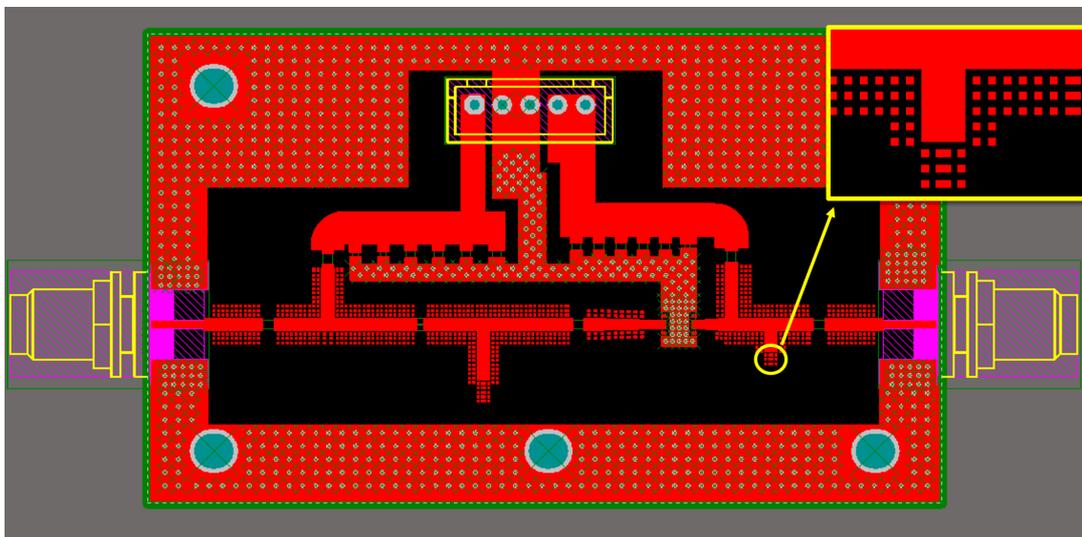


Figure 3.12: 2D Layout Showing Drop Structure for Rework Flexibility

3.4 Electromagnetic Simulations by CST

A layout file imported from ALTIUM and related "s2p" files for each lumped element in the design (all SMDs and GaN transistor) has been included to the EM simulation conducted in CST. Apart from RF signal's input and output ports, there are totally fourteen other ports defined for SMD components. These ports are shown with small red dots in Figure 3.13. Same figure also shows the "meshed" circuit for EM simulation.

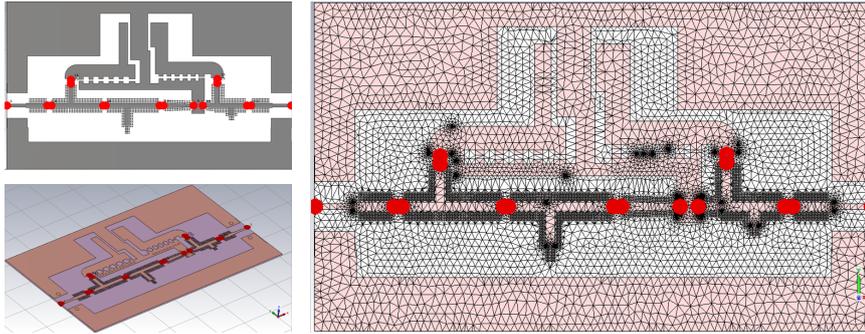


Figure 3.13: Meshed Layout of Final Design with both Distributed and Non-Ideal Lumped Elements on CST

CST circuit configuration for conducting EM simulation and the related result about S-parameters are shown in Figure 3.14 and Figure 3.15 respectively.

In Figure 3.14 it can be easily seen that the EM behaviour of the meshed microstrip lines are buried into the big white box in the middle. The box has sixteen pins which correspond to sixteen ports created while meshing process. Between the pins related SMD component (actually its manufacturer model) is connected.

Different than resistor, capacitors or inductors; a small to-port box, written "TS" on it, has been plugged to the configuration for modeling the behavior of GaN transistor. Related s2p file (i.e Having same biasing conditions) has been uploaded to the two-port box.

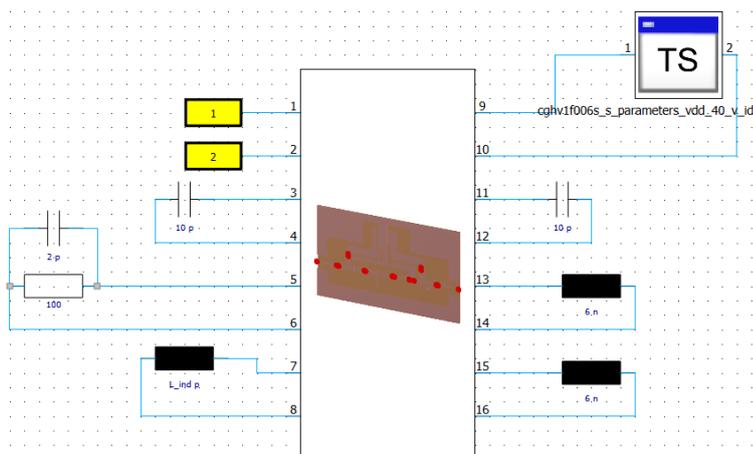


Figure 3.14: Power Amplifier's CST Configuration for Conducting EM Simulation

S-parameter response exhibited at Figure 3.14 has been very surprising. It seems that the characteristic of scattering parameters has been kept unchanged. On the other hand, the response is seemed to be shifted as approximately 1 GHz and peak gain appears to be on around 12.95 GHz. Such large amount of shift is thought provoking. In addition, each S-parameter's magnitude has become worst by 3 to 4 dB, minimum. At this point two different choices have been appeared. The first choice forces to make dramatic changes on the design by relying on CST completely. The second choice, on the other hand, is slanted towards waiting for the measurement results of manufactured circuit. If the measurement results resemble to the CST simulation result, a produced PA with shifted response would not be a loss. In fact, new versions of the PA could be built by the simulation results of CST. Therefore, the second choice is preferred.

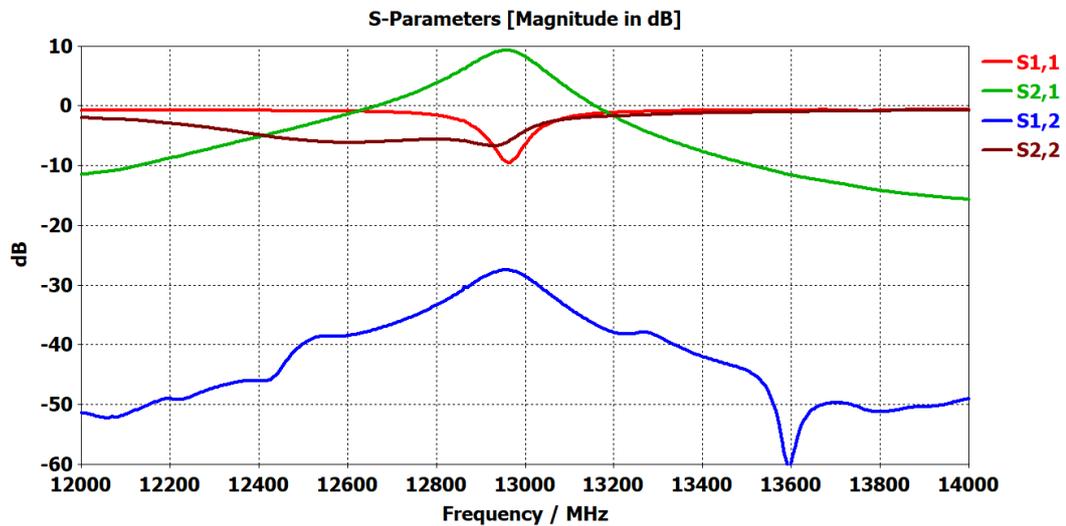


Figure 3.15: Power Amplifier Final Design EM Simulation Result by CST

CHAPTER 4

IMPLEMENTATION AND MEASUREMENTS

4.1 Production Process

For manufacturing process, two different methods have been preferred. First, the PA has been produced by a drilling/etching device called LPKF, later the components of the circuit have been soldered by hand. This method was actually the only way has been thought at the beginning as summarized in Chapter 1 under the title of "In-house Production". Since the power amplifier produced via this method has been affected by many environmental factors and manufacturing errors like over-etching of dielectric or over-heating due to poor grounding, it did not meet the expected performance criteria. Therefore the second method; the idea of the production of PA by a professional facility has appeared. Although this method is more costly than LPKF solution, it is still a cheaper and faster solution than the IC based design and manufacturing.

4.1.1 Circuit Prototyping by Using LPKF

Picture of the power amplifier circuit produced by LPKF Protomat S103 has been shown in Figure 4.1. In the same figure, there are also some details given with zoomed sub-pictures. Sub-pictures in right and left circles in Figure 4.1 show the used conical inductors as RF-choke purpose. The amount of the solder used on the legs of the conical inductor is kept minimum to avoid any capacitive effect caused by the over-soldering (i.e. solder balls).

The picture in the middle circle shows the SMD package choice. For such high frequency applications, SMD component's pad size together with microstrip line width play an important role on the reflections that may occur at the combining points. Therefore, to prevent such reflection problems, component packages should be chosen carefully. For this design, when there is only component on the RF line in series, 0603 package is preferred due to the good match of pad size and line width. However, if the case is similar to the sub-picture in the middle circle, a parallel RC circuit on the line, then the 0402 package SMDs are chosen and soldered closely as shown. By doing so, again a good match of width of microstrip line and pad size is tried to be achieved.

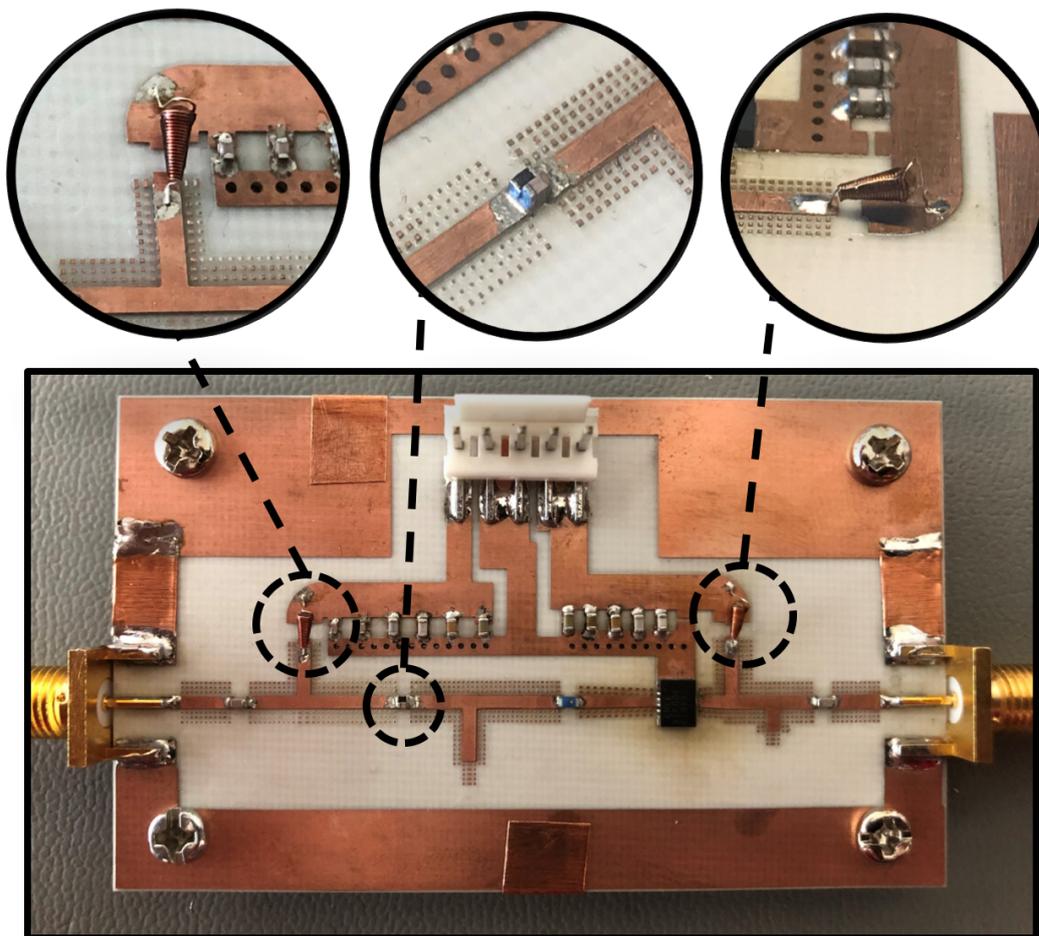


Figure 4.1: Power Amplifier Circuit Produced by LPKF

Another important design issue is the lack of vias shown in Figure 4.1. Since LPKF does not have the ability to create "filled vias", limited number of vias are created (Under the transistor and on the ground plane just above the transistor) and they are filled by solder manually. To do that filling operation manually, the vias had been drilled with larger diameters and this situation has created another undesired capacitance problem under the transistor. As a result, serious grounding problem has been occurred. This problem proves its significant effect as degradation on the gain, which can be seen in Figure 4.10.

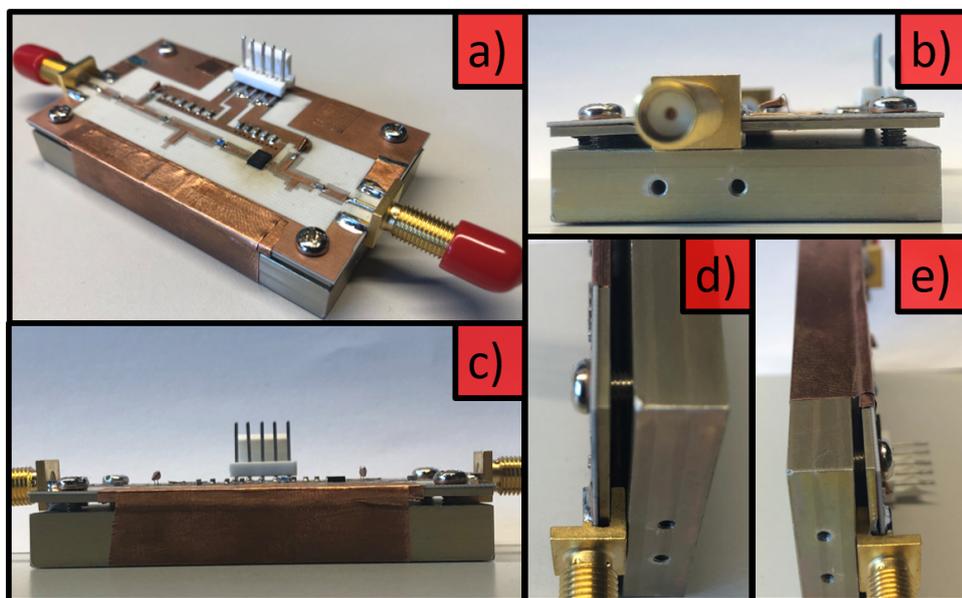


Figure 4.2: Complete Power Amplifier by LPKF a) General View b) Right Side View c) Front Side View d) Vertical Right View e) Vertical Left View

Figure 4.2 shows the original power amplifier circuit with modifications for cooling purposes by different angles. Since the heat could not be dissipated homogeneously, a thicker metal piece has been added under the default thin metal located below the circuit. As shown in "a", "c" and "e" copper tapes are attached so that the heat can flow easily through every direction on the metal. Unfortunately, original thin metal and later added thicker metal do not have a direct contact all over their surfaces and they have a air gap between them, as can be seen in "b" and "d".

4.1.2 Final Circuit Production by "Professional Facility" (*Simpro Elektronik*)

To obtain a better PA performance, lessons learned during the PA production by LPKF have been considered before sending the circuit's gerber files to the professional PCB facility (*Simpro Elektronik*). For instance, even though it increases the cost, all the available areas are stuffed with "filled vias".

To adopt the manufacturing ability of the PCB facility, number of the layers are increased to six. To turn this change to an advantage, the inner layers are determined as dummy, ground layers. Therefore, by applying these two changes, the effect of heating problem is reduced dramatically. Also the vias under transistor had been drawn smaller so that the number of them is increased as shown in "b" and "c" of Figure 4.4. This modification decreased the undesired capacitance issue that exists under the transistor.

To get rid of assembling problems caused by manufacturing errors, solder paste is used for each component and later on the PA board is sent to industrial PCB ovens. After manufacturing, each component in the power amplifier has been investigated by X-ray as shown in Figure 4.4.

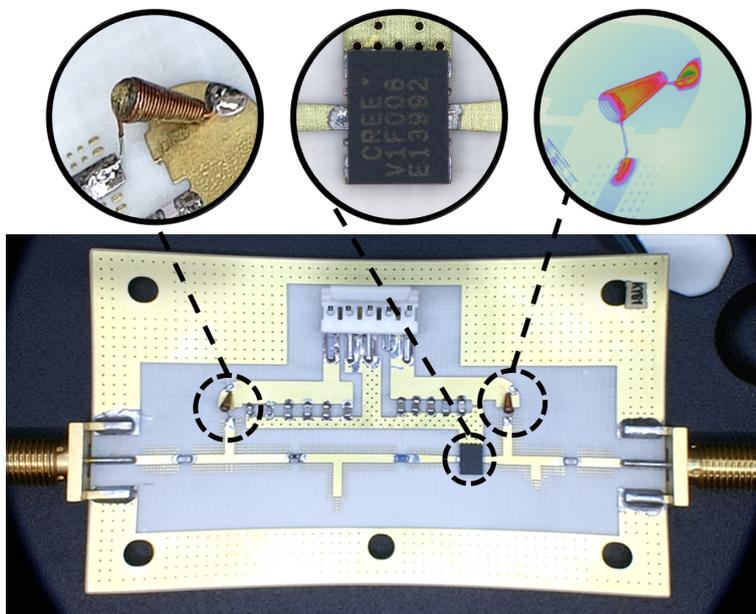


Figure 4.3: Power Amplifier Circuit Produced by Professional Facility (*Simpro Elektronik*)

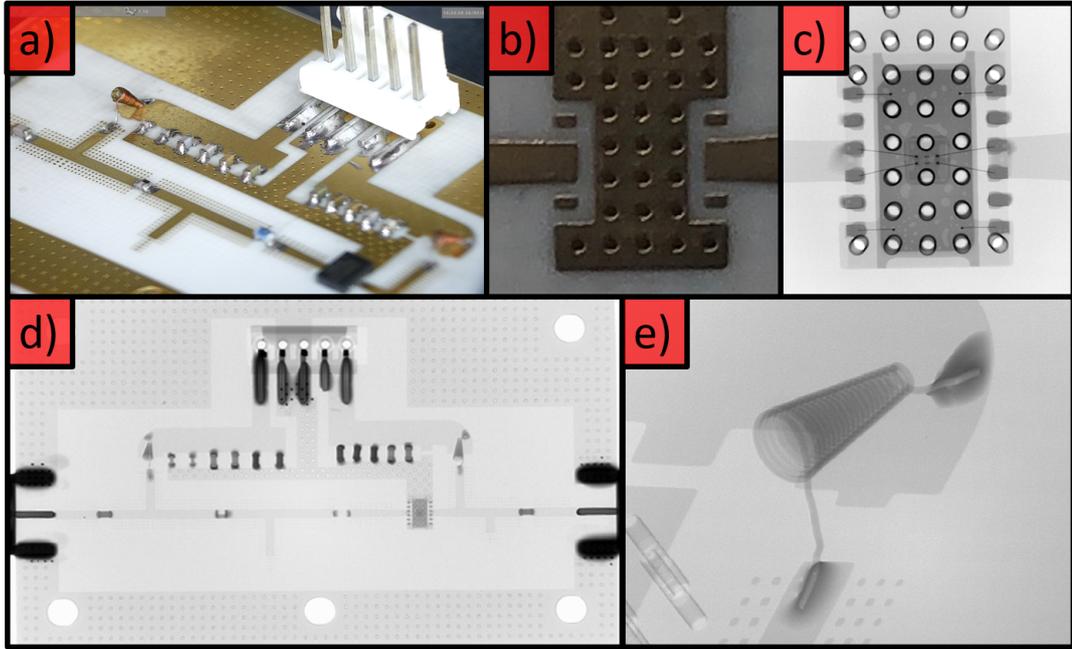


Figure 4.4: Complete Power Amplifier by Professional Facility (*Simpro Elektronik*)

- a) General View b) Vias Under Transistor c) X-ray Image of Transistor d) X-ray Image of Complete PA e) X-ray Image of Conical Inductor

4.2 Measurements

4.2.1 Measurement Equipment and Setup

Two different setups have been prepared for measurement of S-parameters and linearity parameters; P_{1dB} and P_{SAT} . Both prototypes; by LPKF and by professional facility, have been measured by same setups. These setups and the used devices can be investigated by the block diagrams in Figure 4.6 and Figure 4.8 while the real measurement environment has been illustrated in Figure 4.5, Figure 4.7 and Figure 4.9,.

The equipment models used in these setups are given below;

- Network Analyzer; KEYSIGHT - N5244A PNA-X, 43.5 GHz
- Signal Generator; KEYSIGHT - E8267D PSG, 100 kHz to 44 GHz
- Signal Analyzer; KEYSIGHT - N9040B UXA, 2 Hz to 50 GHz

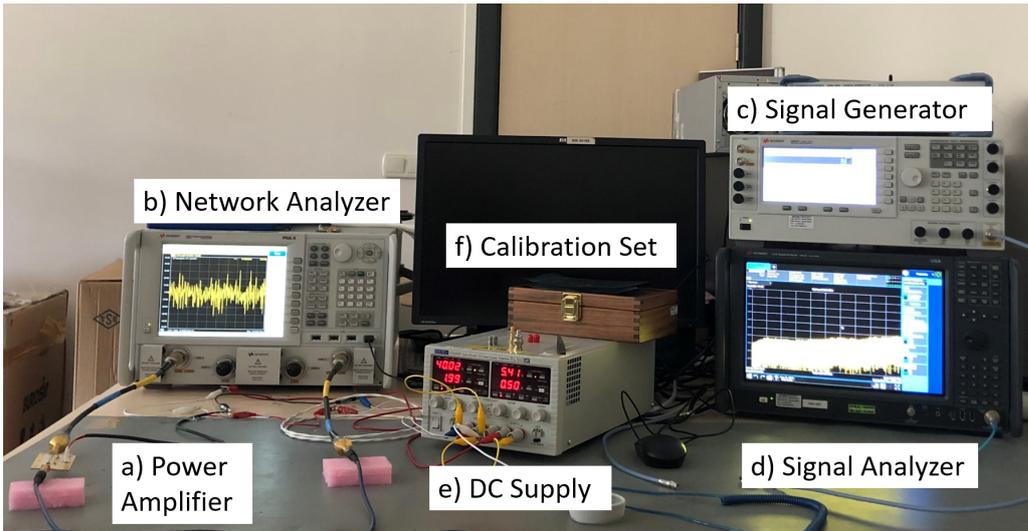


Figure 4.5: Workspace for Power Amplifier Measurements

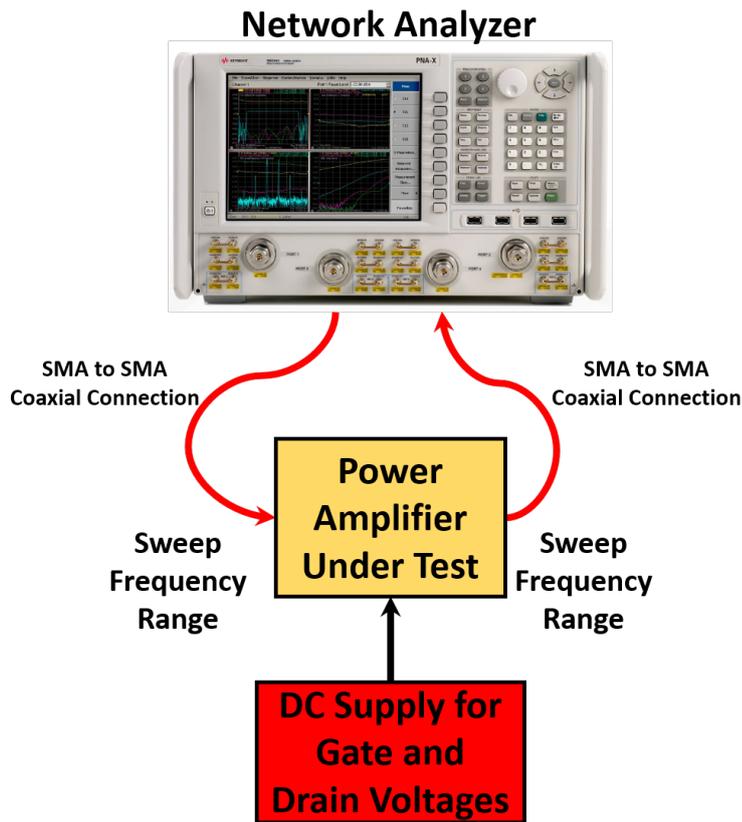


Figure 4.6: First Configuration of Measurement Setup for S-Parameters

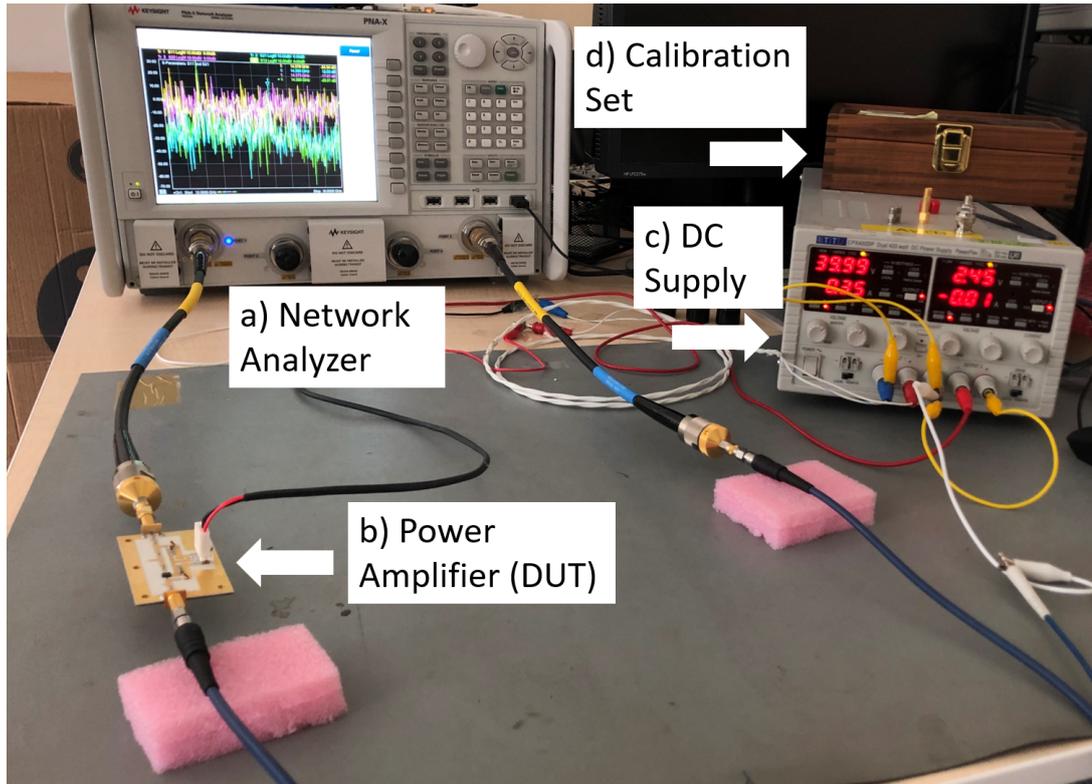


Figure 4.7: First Measurement Setup for S-Parameters a) Network Analyzer b) Power Amplifier under Test c) DC Supply d) Calibration Set Used for Network Analyzer

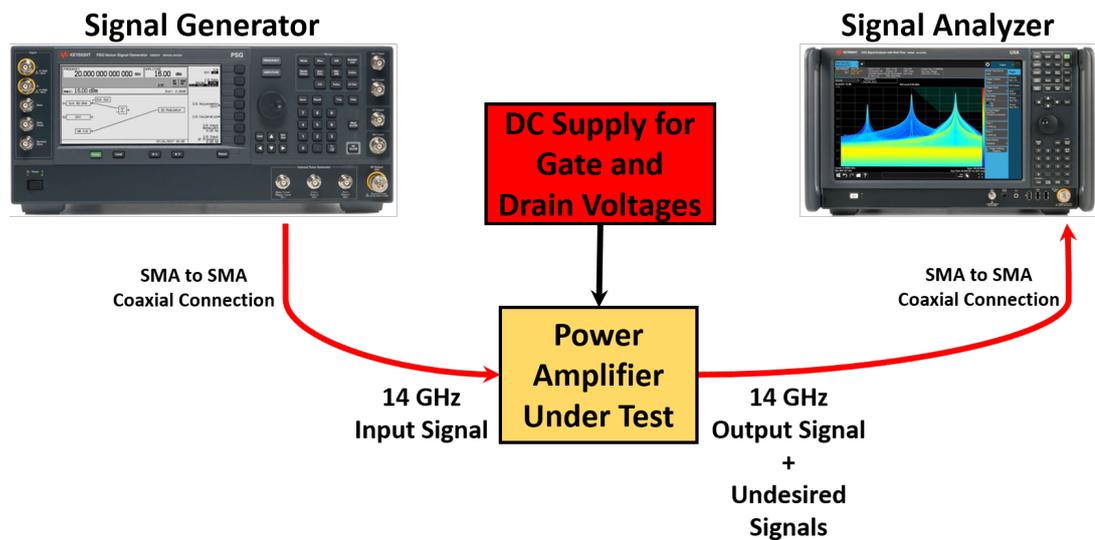


Figure 4.8: Second Configuration of Measurement Setup for P_{1dB} and P_{SAT}

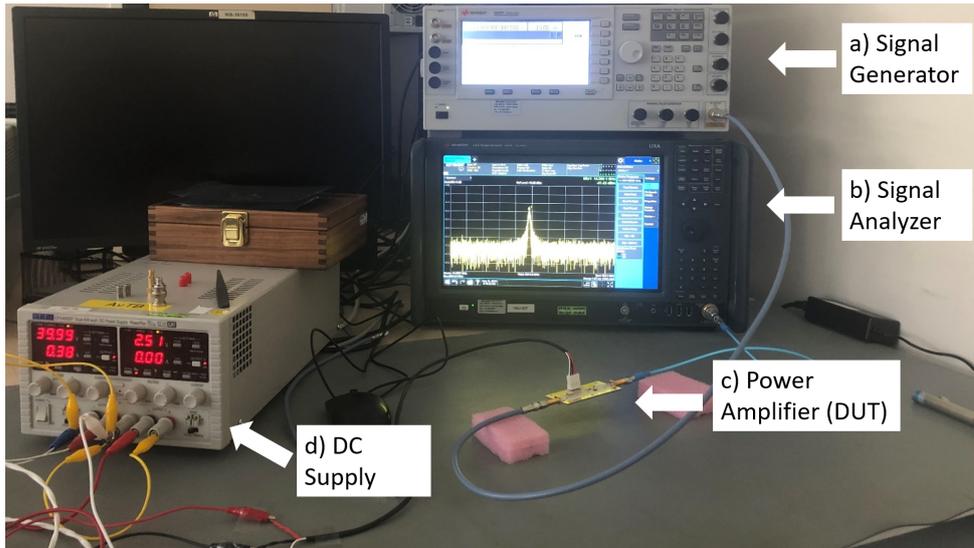


Figure 4.9: Second Configuration of Measurement Setup for P_{1dB} and P_{SAT} a) Signal Generator b) Signal Analyzer c) Power Amplifier d) DC Supply

4.2.2 Final Measurement Results

One of the meaningful measurements of the power amplifier prototype by LPKF is given in Figure 4.10 in a very narrow frequency span. As can be seen, the gain is measured lower than it is expected and has been seen in simulations.



Figure 4.10: Gain and Input Matching Performance of the Power Amplifier Circuit Produced By LPKF

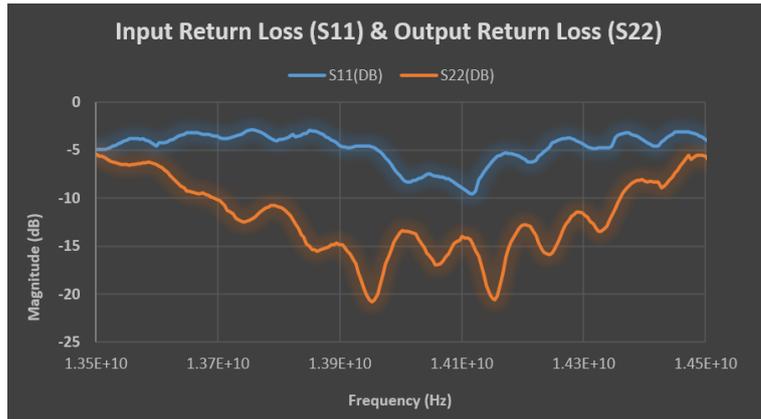


Figure 4.11: Input and Output Matching Performance of the Power Amplifier Circuit Produced By LPKF

Due to the low-performance of S-parameter measurements and heating problem, P_{1dB} and P_{SAT} measurement could not be conducted for the prototype by LPKF. In fact, input and output matching performance of the PA shown in Figure 4.11 has raised doubts about the functionality of the power amplifier.

The measurements have continued with the power amplifier prototype produced by the professional facility. SMDs and the connectors have been kept same at first. Related S-parameter results have been shown in Figure 4.12.

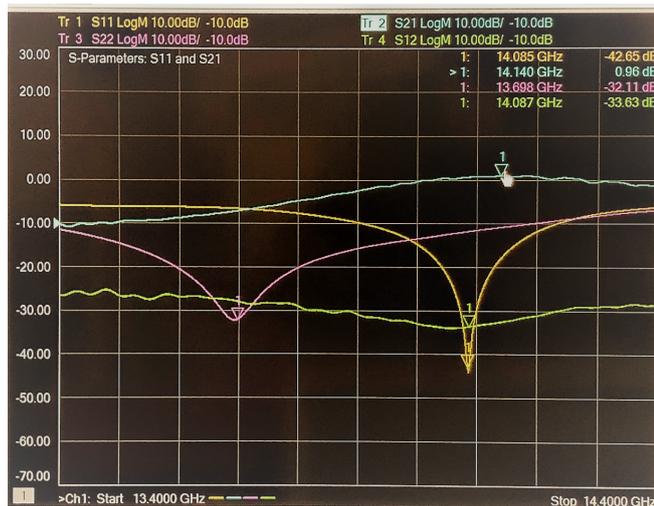


Figure 4.12: First S-Parameter Measurement of PA Produced by Professional Facility

4.2.2.1 Gain Measurement Results

After the measurement shown in Figure 4.12, it has been understood that the circuit could not perform as desired at such level of frequencies and it needs rework as predicted at the beginning of this work. Arbitrary touches onto cells alongside of the microstrip lines has provided a small increase at the gain of the amplifier as shown in Figure 4.13. On the other hand, such improvement was not enough and still needed to define the main performance problem.

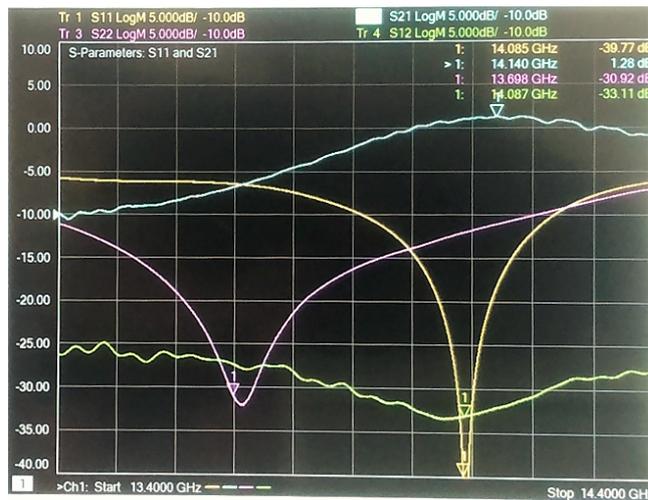


Figure 4.13: Optimization Applied S-Parameter Measurement of PA Produced by Professional Facility

As the next step to cope with the design's problem, SMA connectors are replaced by an alternative model which supports applications up to 18 GHz, as shown in Figure 4.14.

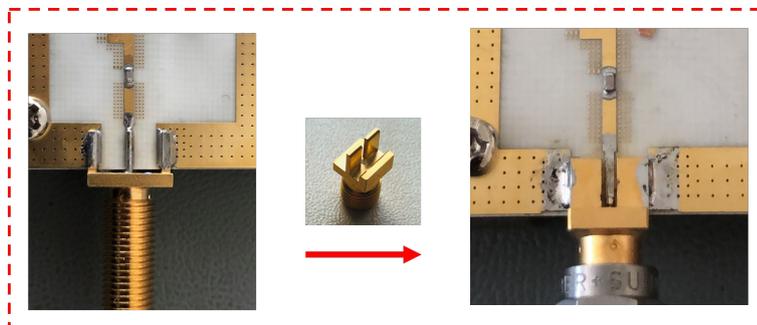


Figure 4.14: Replacement of SMA Connectors in the Design

Replacement of the connectors has been effective on the design since the gain of the design has been increased from 1.28 dB to 2.50 dB while matching performance has been conserved. New response has been illustrated in Figure 4.15 but still requires optimization by using the cells mentioned before alongside microstrip lines and stubs. Therefore, the optimization had been applied one more time and the performance has improved again a little bit more in terms of gain, i.e. gain has become 3.03 dB, as shown in Figure 4.16. Also, it has been realized that the RF choke part at the output causes leakage in terms of RF signal. Applied optimization includes modifications on that part of the circuit, too.



Figure 4.15: S-Parameter Measurement of PA After Replacement of SMA Connectors

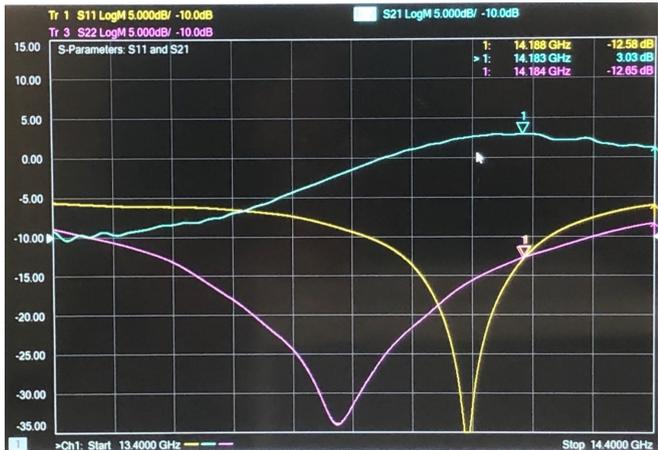


Figure 4.16: Optimization Applied S-Parameter Measurement of PA After Replacement of SMA Connectors



GAIN: 0.86 dB



GAIN: 1.58 dB



GAIN: 2.20 dB



GAIN: 2.71 dB



GAIN: 2.87 dB



GAIN: 3.03 dB

Figure 4.17: Improvement of Gain Gradually

To be sure about the exact value of measured gain, additional measurement has been conducted by signal generator and signal analyzer. First, -10 dBm input signal at 14.1 GHz (Frequency value having the largest gain on network analyzer) has been applied by signal generator through the measurement cables. Then, the signal power has been monitored by signal analyzer as -15.14 dBm. By doing that, the insertion loss of the cables is identified as -5.14 dBm. Second, the amplifier is put between signal generator and signal analyzer through the same coaxial cable configuration and the measurement repeated without changing any other parameter. This time, the output signal power has been read as -11.77 dBm, which concludes that the gain of the amplifier is equal to 3.37 dB. This situation verifies the measurements conducted by network analyzer. The visuals related to the measurement is given in Figure 4.18.

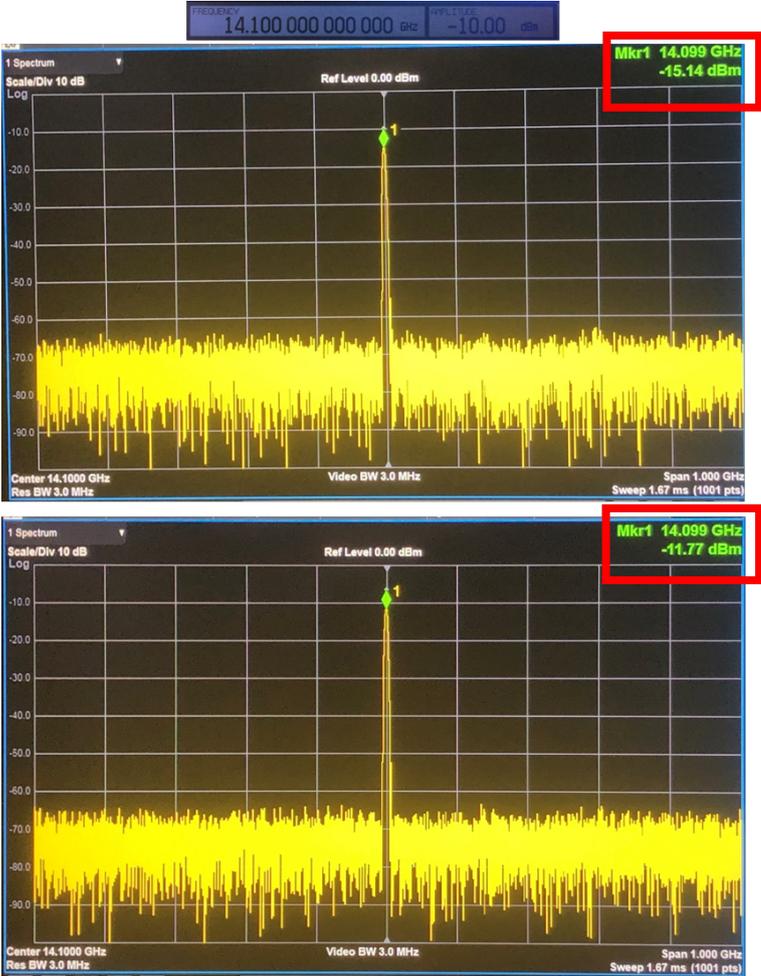


Figure 4.18: Output Power Measurement Using Signal Generator & Analyzer

4.2.2.2 Linearity Measurement Results

4.2.2.3 P_{1dB} Measurement

To test the linearity behavior of the amplifier, P_{1dB} point has been identified as the first step. First, -20 dBm input power is applied through the amplifier and the gain is measured. Second, the input power is increased by 1 dB, until input power reaches 20 dBm. It has been realized that when the input power becomes 17 dBm, the gain is decreased by 1 dB, i.e. the compression had occurred. The change of input power vs. output power is given as in the Table 4.1.

Table 4.1: Measurement for P_{1dB}

RF Input Power (dBm)	RF Output Power (dBm)	Difference (dB Scale)	Cable Loss (dB)	PA's Gain (dB)
-20	-20.93	-0.93	-5.14	4.21
-19	-19.97	-0.97	-5.14	4.17
-18	-18.95	-0.95	-5.14	4.19
-17	-17.97	-0.97	-5.14	4.17
-16	-16.98	-0.98	-5.14	4.16
-15	-15.99	-0.99	-5.14	4.15
-10	-11.13	-1.13	-5.14	4.01
-5	-6.04	-1.04	-5.14	4.1
0	-1.08	-1.08	-5.14	4.06
5	3.95	-1.05	-5.14	4.09
10	8.52	-1.48	-5.14	3.66
15	13.27	-1.73	-5.14	3.41
16	14.21	-1.79	-5.14	3.35
17	15.05	-1.95	-5.14	3.19
18	15.88	-2.12	-5.14	3.02
19	16.65	-2.35	-5.14	2.79
20	17.43	-2.57	-5.14	2.57

4.2.2.4 Harmonic Distortion (HD) Measurements

Harmonic distortions are one of the most critical non-linearity reason of many. Therefore, the rate of grow of HDs is important for power amplifier design. Even though there is not any specific linearity goal in the scope of this work, it should be investigated as it is done for every power amplifier design.

For this work, single tone input power is changed from -20 dBm to 20 dBm. It is observed that for small RF input values from -20 dBm to 0 dBm, even the strongest harmonic distortion, which is HD₂, could not be observed. On the other hand, as the signal level gets closer to 10-20 dBm, HD₂ and HD₃ components become remarkable at the frequencies of 2f₀ and 3f₀ respectively. Screenshots from the measurement and numerical results are given in Figure 4.19 and Table 4.2 in a detail way. After exceeding P_{1dB}, HD₂ and HD₃ grow rapidly, degradation on the gain becomes remarkable, which can be shown in Table 4.2.

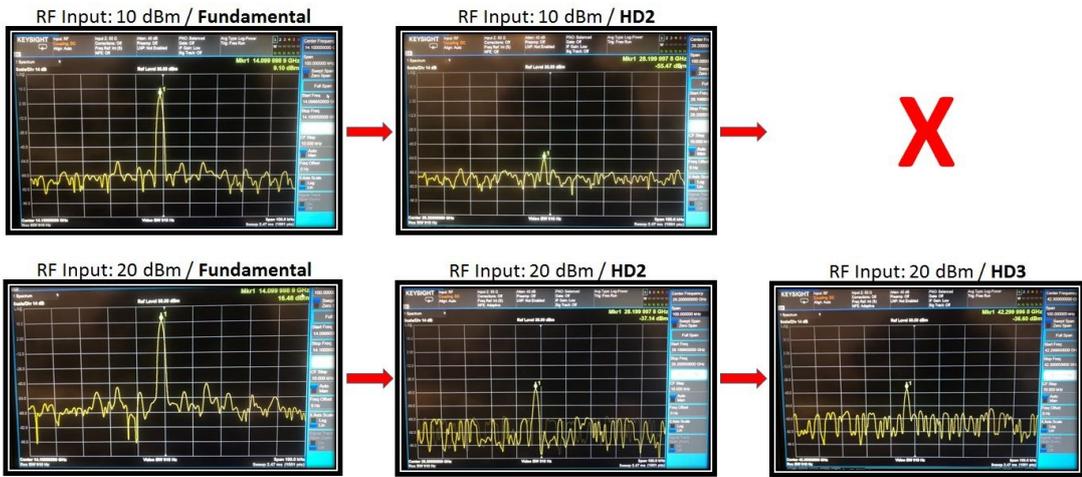


Figure 4.19: Observation of Harmonic Distortions (HD₂ and HD₃) with Different Power Levels of Input Signals

Table 4.2: Existence of Harmonic Distortions at Critical RF Input Levels

RF Input Power	Fundamental Frequency (i.e. HD1) (@14.1 GHz)			HD2 (@28.2 GHz)	HD3 (@42.3 GHz)
	Without PA	With PA	Gain		
-20 dBm	-25.14 dBm	-20.85 dBm	4.29 dB	-	-
0 dBm	-5.14 dBm	-0.91 dBm	4.23 dB	-	-
10 dBm	4.86 dBm	9.1 dBm	4.24 dB	-55.47 dBm	-
17 dBm (P _{1dB} Point)	11.86 dBm	15.05 dBm	3.18 dB	-44.47 dBm	-46.53 dBm
20 dBm	14.86 dBm	16.48 dBm	1.62 dB	-37.14 dBm	-36.6 dBm

4.2.2.5 Intermodulation Distortion (IMD) Measurements

As mentioned before, different than the harmonic distortions, there is another non-linearity factor in power amplifier design, which is intermodulation distortion. IMDs are more dangerous than HDs because they are products of two-tone inputs and called as "in-band" distortions. Therefore, they can not be filtered out easily as harmonic distortions. The effect of IMDs are shown in Figure 4.20 via increase of the input power level of "two-tone" step by step. As seen from Figure 4.20, when the output power of fundamental signal reaches -4.25 dBm, IMD_3 components start to appear right next to fundamental signal. After that point, every 5 dB increase at the input level respectively creates IMD_5 and later IMD_7 rapidly.

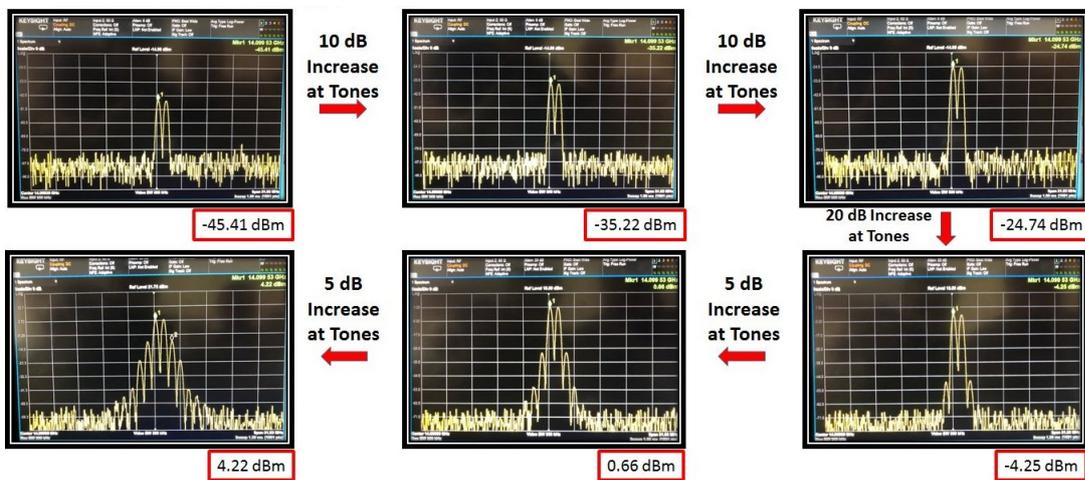


Figure 4.20: Observation of Intermodulation Distortions (IMD_3 , IMD_5 , IMD_7 and higher levels of IMDs) with Different Power Levels of Input Signals

4.2.3 Investigation of Reasons of Gain Degradation

At this point, it may seem that the improvement period of the design is completed, however additions on the design for canceling the contributions of parasitic effects and secondary effects (Such as connector losses and microstrip insertion loss) can be made. In fact, the gain difference, around 5.5 dB - 6 dB, between the EM simulation result on CST and the measurements is investigated and the factors which contributes the difference has been identified. It is deduced that the gain of the amplifier can be in-

creased up to 7-8 dB by sufficient modifications with correct methodology. Therefore, effects of the factors which causes gain degradation is subtracted and new "response calibration" has obtained.

4.2.3.1 CST Based Investigation

Simulations conducted between 13.5 GHz and 14.5 GHz on CST design environment have shown that insertion loss value observed on simple microstrip lines is changing from 1.045 dB to 1.35 dB, related results can be seen from Figure 4.21. This value is independent from the insertion loss which will occur due to SMA connectors at input and output of the circuit.

Additional information about simulation in Figure 4.21;

- Mesh size is automatically assigned by adaptive meshing property of CST. Smallest cell size is assigned based on upper frequency; 14.5 GHz.
- To avoid undesired coupling between two microstrip line, the microstrip lines with cells and without cells are placed adequately far away from each other.

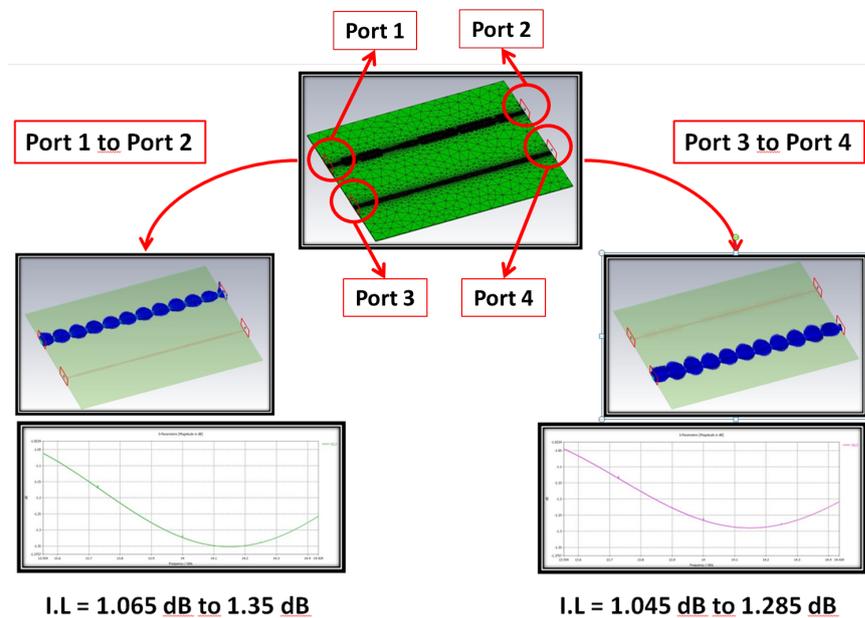


Figure 4.21: Meshed Circuit on CST & E-Field Monitoring on Circuit & Microstrip Line Insertion Loss Simulations on CST without Connector Effects

4.2.3.2 New Circuit Production Based Investigation

It is clearly known that the input and output SMA connectors also introduce insertion loss which contributes gain degradation. Therefore, to observe the effect of them, the circuits in Figure 4.23 are produced and this time connector based insertion loss are not only simulated but also measured together with the loss on microstrip lines. All results are shown in Figure ??.

Case 1) "A1-to-A2 Configuration": RF signal is applied to connector A1, which is the input port and output is measured from output port A2. For this configuration, there is not any tuning cells along the microstrip line.

Case 2) "C1-to-C2 Configuration": RF signal is applied to connector C1, which is the input port and output is measured from output port C2. For this configuration, only thing different is that there are tuning cells along the microstrip line. Connector type is same as Case 1.

Case 3) "B1-to-B2 Configuration": RF signal is applied to connector B1, which is the input port and output is measured from output port B2. For this configuration, different than the Case 2, SMA connector type is changed. Again, there are tuning cells along the microstrip line.

From Case 1 through Case 3, it is aimed to change only one parameter so that controlled design environment could be achieved.

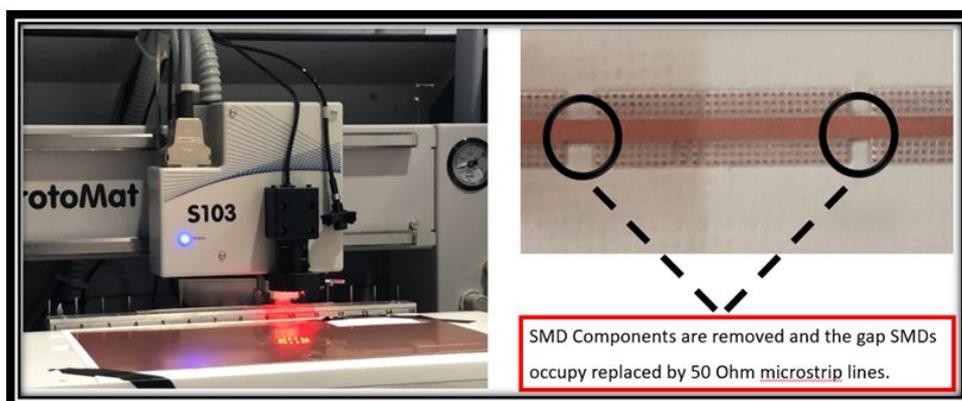


Figure 4.22: Simple Microstrip Line Production by LPKF for Measurement of Connector-to-Connector Insertion Loss

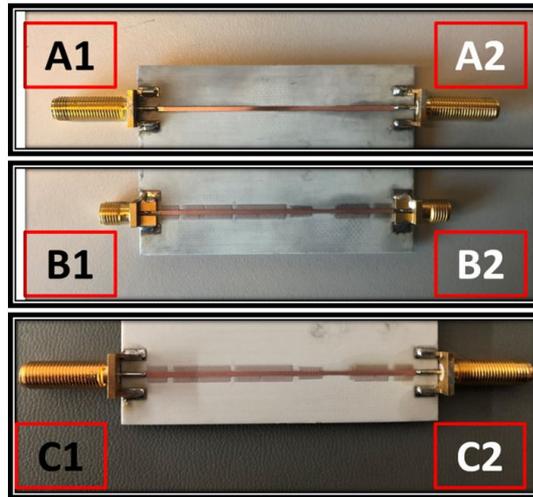


Figure 4.23: Three Different Microstrip Line & Connector Configurations for Measurement of Connector-to-Connector Insertion Loss

As seen in Figure 4.22 and Figure 4.23, new microstrip lines are produced with same substrate (RO4003C) and same length. Different connectors are used for B1-to-B2 and C1-to-C2 configurations to investigate the insertion loss effect of different SMA connectors at 14 GHz. On the other hand, for A1-to-A2 and C1-to-C2 configurations, connector type is kept same to see whether or not there is a "loaded microstrip line" effect due to the cell around the microstrip line. By doing so, a controlled design of experiment is built to observe the individual effects of connector types and cells along microstrip lines on the insertion loss value.

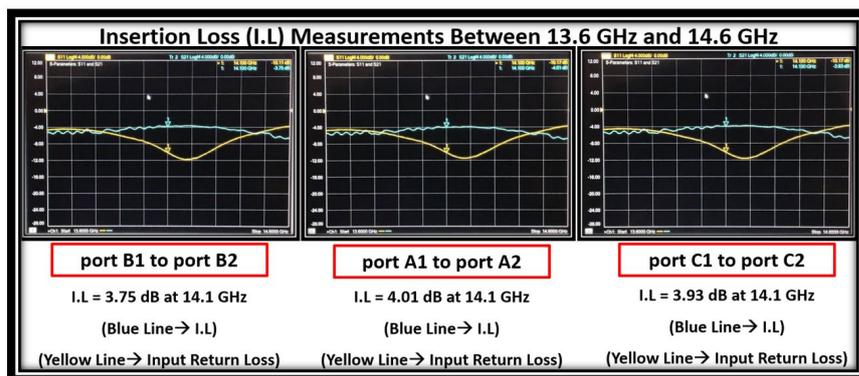


Figure 4.24: Connector-to-Connector Insertion Loss Measurements from 13.6 GHz to 14.6 GHz

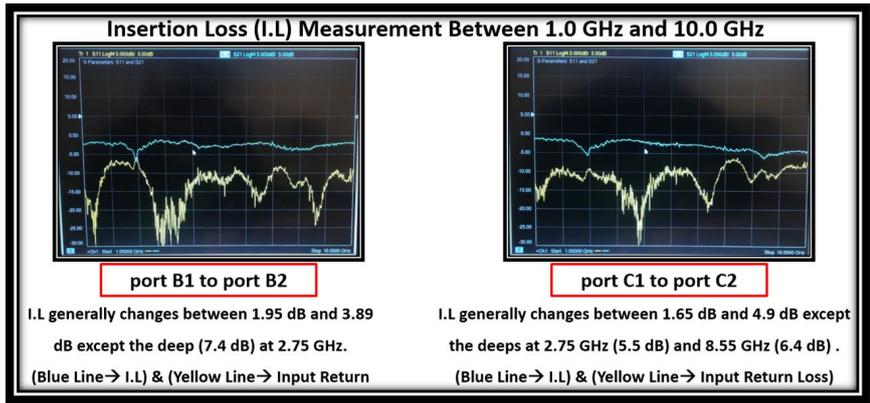


Figure 4.25: Connector-to-Connector Insertion Loss Measurements from 1.0 GHz to 10.0 GHz

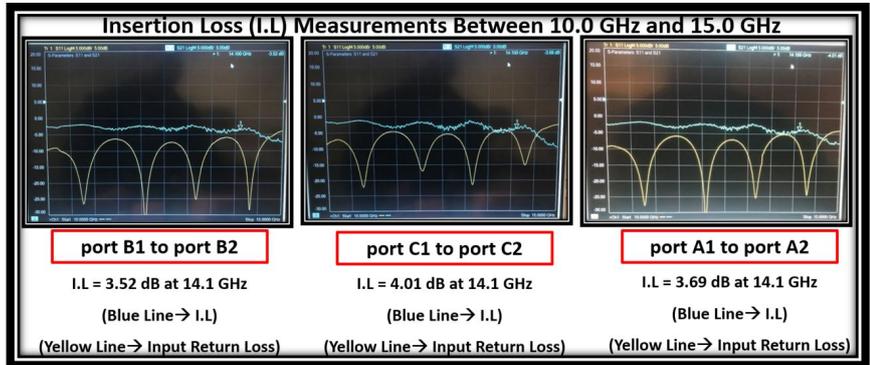


Figure 4.26: Connector-to-Connector Insertion Loss Measurements from 10.0 GHz to 15.0 GHz

Measurements conducted between 13.6 GHz and 14.6 GHz have shown that insertion loss value observed on both "simple microstrip lines" and "SMA connectors" together, is changing from 3.75 dB to 4.01 dB, related results can be seen from Figure 4.24, Figure 4.25, Figure 4.26. For measurements on three frequency bands (13.6 - 14.6 GHz, 1.0 - 10.0 GHz, 10.0 - 15.0 GHz), the calibration of network analyzer is done three times. When simulation-based microstrip line insertion loss value is subtracted from measurement-based loss results (I.L. of SMAs and MSLs), it is possible to obtain the insertion loss value occurring only due to SMA connectors which is measured to be between 2.4 dB to 3 dB.

CHAPTER 5

CONCLUSION, ACHIEVEMENTS AND FUTURE WORK

In this study, GaN-HEMT based Ku-band power amplifier design is taken into account for SATCOM applications. In this aspect, firstly a schematic model was developed in simulation platform, NI AWR. For simulations, two-staged design process was followed. First, the power amplifier was built by ideal lumped components. Then, the model was converted to a realistic model by addition of distributed circuit parts and the schematic simulations were repeated.

After many optimization steps, the design was frozen and PCB files are created by ALTIUM. Those files are exported to CST for conducting EM simulation. The result of the EM simulation was not shocking but surprising due to the unexpected frequency shift occurred on the S-parameter response of the power amplifier. At that point, it has been decided to proceed without changing anything in the design and preferred to see the measurement results after manufacturing. After the manufacturing process, it is observed via measurements that the shift on the response observed on CST is not true, because the shift on response is not remarkable.

First prototype, produced by LPKF, had many problems but sources of those problems were identified. The identification of the problem sources brought solutions with itself. Therefore, the second prototype was prepared.

Second power amplifier prototype was produced by a professional PCB facility (*Simpro Elektronik*) to minimize the manufacturing errors. Those errors cause big performance problems at such high frequencies as Ku-band.

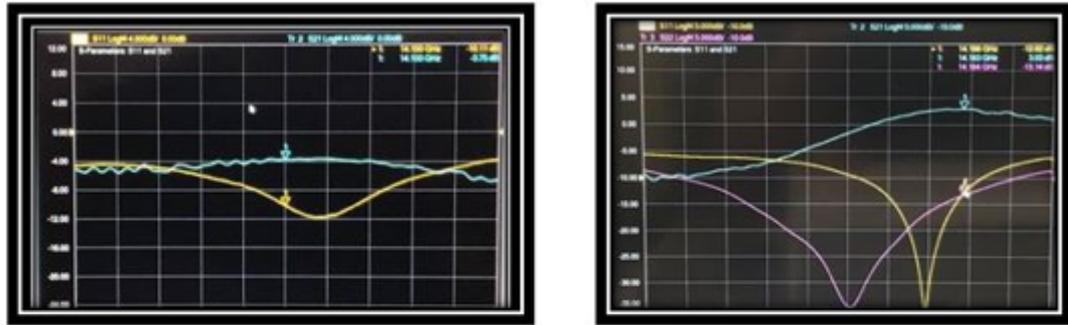
Second prototype had performed better and the claim at the beginning of this study was proven; implementation of a single stage discrete power amplifier design rather than an IC, can be possible at frequency band as Ku despite performance difference. The performance difference refers to mainly "gain degradation" in this case.

All the results obtained from simulations and measurements conducted are given in Table 5.1 for comparison.

Table 5.1: Comparison of Simulation Results and Measurements

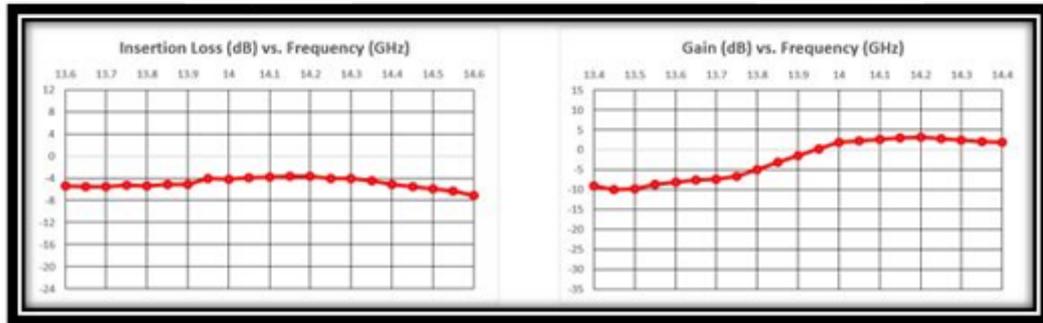
Parameter	Definition	Schematic Simulation Early Design Result @ 14 GHz	Schematic Simulation Final Design Result @ 14 GHz	EM Simulation Result @ 12.95 GHz	LPKF Prototype Production Measurement @ 13.987 GHz	Facility Production Measurement @ 14 GHz
S21	Gain	14.47 dB	12.84 dB	9.87 dB	5.02 dB	4.29 dB
S11	Input Return Loss	-19.63 dB	-24.85 dB	-9.92 dB	-6.29 dB	-12.62 dB
S22	Output Return Loss	-14.31 dB	-17.02 dB	-6.73 dB	-5.83 dB	-13.14 dB
S12	Isolation	-18.86 dB	-20.49 dB	-27.2 dB	-25.11 dB	-25.57 dB
P1dB	1 dB Compression Point	15.2 dBm	14.3 dBm	Null	Null (IC Fail)	17 dBm
K, Mu, B	Stability	Stable	Stable	Stable	Stable	Stable

To increase the gain many efforts are shown but high gain, as much as observed at EM simulations (around 10 dB), could not be achieved. That's why the problem becomes the identification of reasons of "gain degradation" and weights of those reasons. Two methods are applied; first method is to understand the degradation due to the loss occurring on microstrip line, which is line RF input signal mainly travels on it. This factor and its effect are analyzed by the simulations conducted on CST. Second method is based on manufacturing single microstrip line whose length is same as the power amplifier. By doing this, the degradation effect on gain caused by also the SMA connectors is observed. When the total effect is de-embedded, "response calibration" of the circuit is obtained. Even though the observations show that some of the power is also lost at the bias parts, it could not be possible to quantify the amount of the lost power exactly.

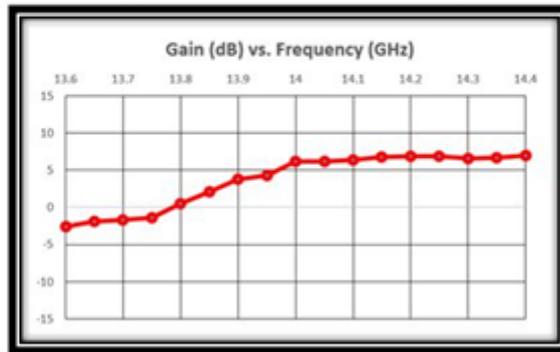


a)

b)



c)



d)

Figure 5.1: Gain vs. Frequency Result After Conduction of "Response Calibration"

In Figure 5.1, there are two measurement screenshots shown at top called as "a)" and "b)"; the measurement on left (part a) belongs to the connector-to-connector insertion loss (blue line) and input return loss (yellow line) of a simple microstrip line with SMAs. On the other hand, the measurement on the right (part b) is the regular scattering parameter result of the power amplifier. This time, blue line represents the gain

while yellow line shows again the input return loss. Insertion loss values (with respect to the bandwidth) of the left picture and gain values (with respect to the bandwidth) of the right picture are transferred to a chart type of "scatter with smooth lines and markers" (part c) and subtracted from each other to achieve a "response calibration" (part d).

Table 5.2: Final Gain Value After Response Calibration

Facility Production Gain Value	Final Gain Value After Response Calibration
4.29 dB	7.3 - 7.4 dB

When the effects that causes gain degradation are subtracted from the latest (S_{21}) measurement, it is possible to obtain response calibration for gain vs. frequency profile as shown in Figure 5.1 and get a comparison given in Table 5.2.

If it is wanted to sum up all the work done in the scope of this study step by step, it can be said that firstly a single stage GaN-HEMT solid-state power amplifier is desired to be designed and manufactured based on discrete design, rather than IC. Secondly, schematic design and simulations are conducted by NI AWR. Thirdly, EM simulations are done by using CST. Later on, layout is optimized on ALTIUM. All the schematic design and simulations was based on 14 GHz center frequency and measurements showed that the optimum performance has occurred at center frequency of 14.1 GHz. Many design goals such as operational bandwidth (100 MHz min.), input & output return losses (-10 dB min.), isolation (-10 dB min.) and stability requirements, considered at the beginning of the project, are achieved. However, maximum gain of the amplifier was observed as 4.29 dB, approximately 5.5-6 dB less than the aimed value. Due to the failure of this parameter, 30 dBm output power requirement could not be achieved. Apart from the design goals, many linearity related terms such as harmonic and intermodulation distortions are also observed and measured at the output of the amplifier together with the fundamental output signal at 14.1 GHz. Due to the measured low gain, 1 dB compression point has differed than the simulations. Manufacturing process showed that power amplifier discrete (hybrid) design at Ku-band suffers from many parameters such as soldering quality, SMD package

size, SMA connector choice, RF leakage at biasing part etc. To eliminate their effects which are resulted with degradation on gain, "response calibration" has conducted. So, the effect of insertion loss which mainly occurs on microstrip lines and SMA connectors is de-embedded.

To sum up, even though the parasitic effects and secondary manufacturing errors have caused a significant degradation at the gain, it is experienced and understood that a discrete, stable power amplifier design with successful input and output return losses, rather than all IC-based design, is possible at Ku-band. To achieve the desired output power, alternative solutions such as a multistage design, can be preferred in the future.

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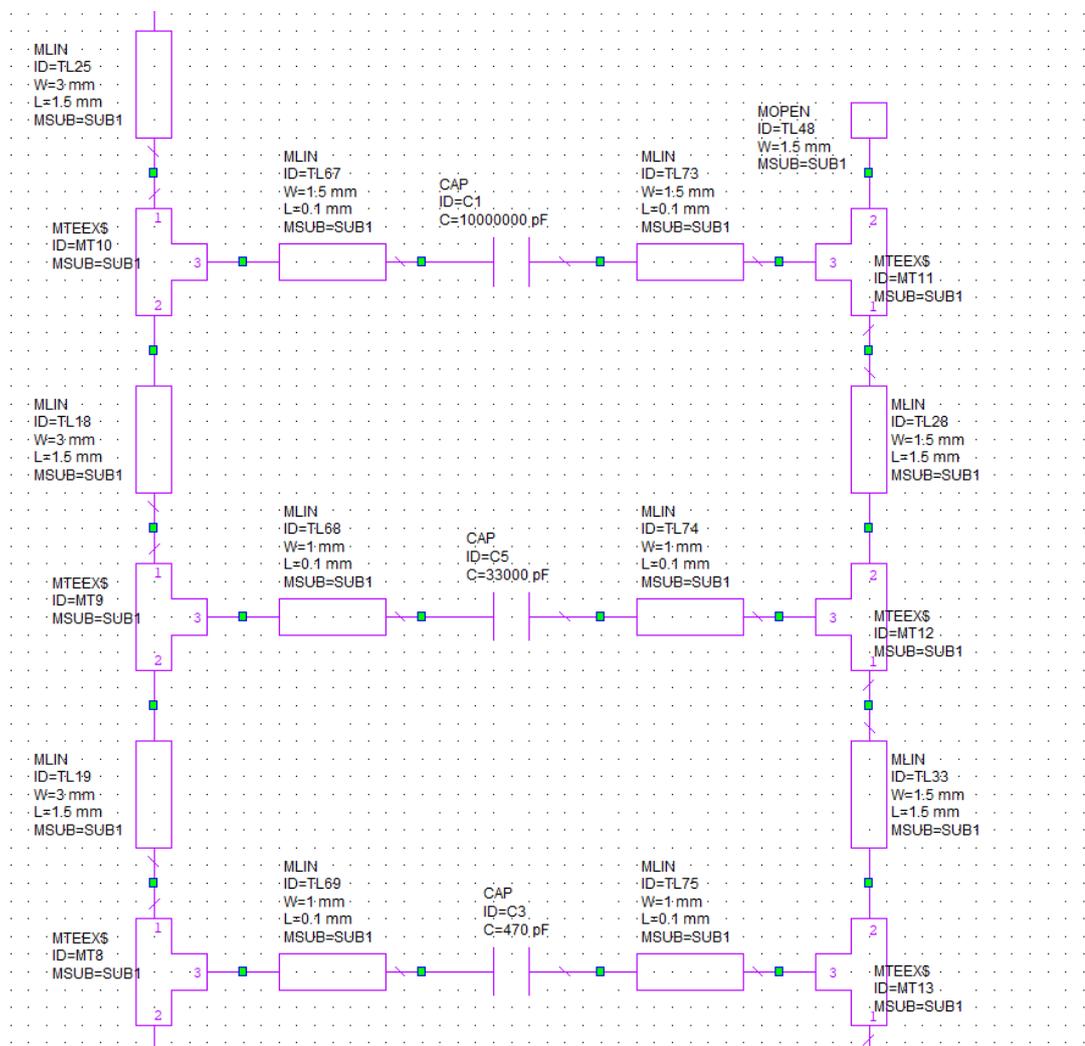
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APPENDIX

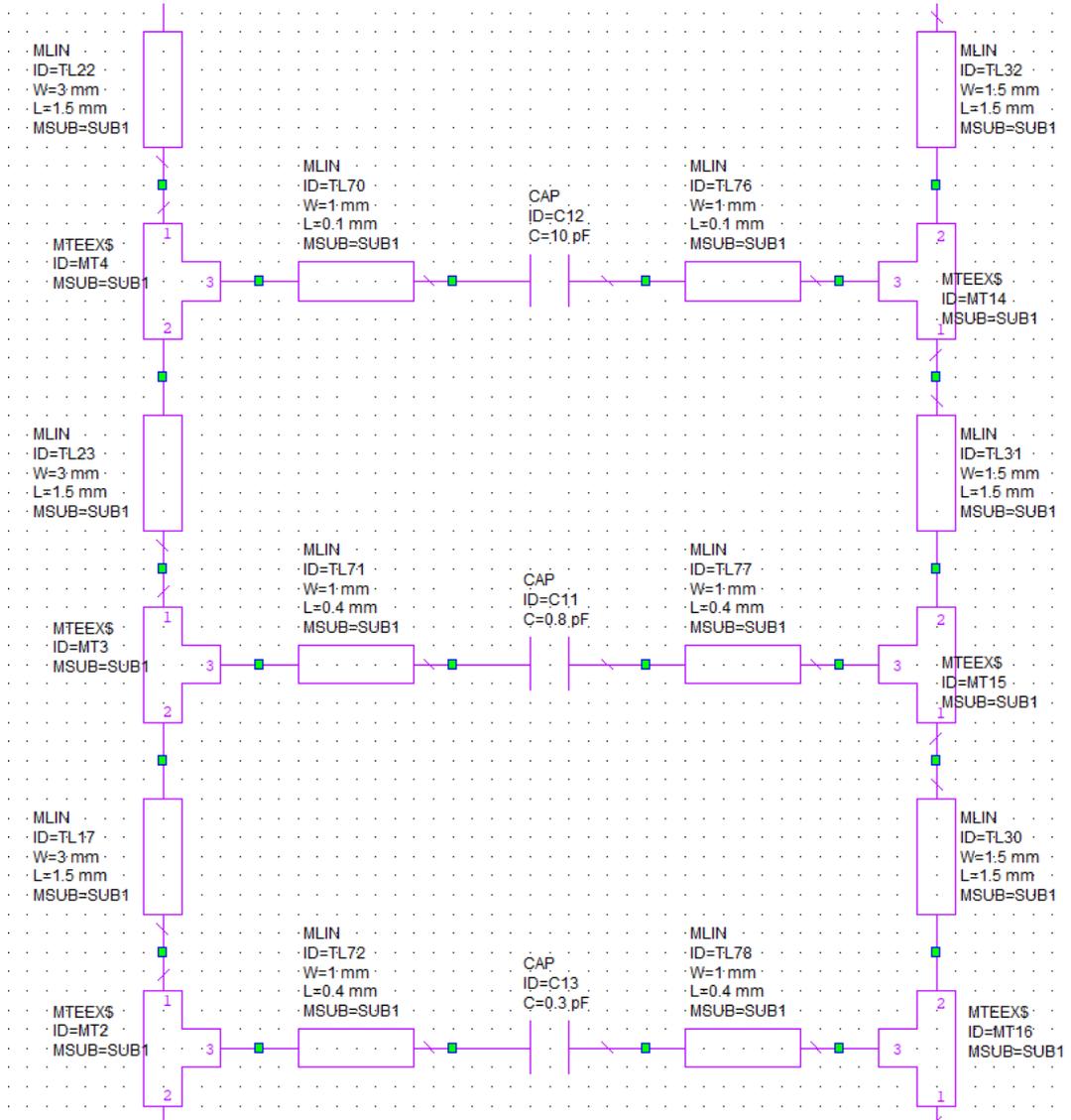
DC Section of Improved Final Design with Nonideal Lumped Elements

PART A



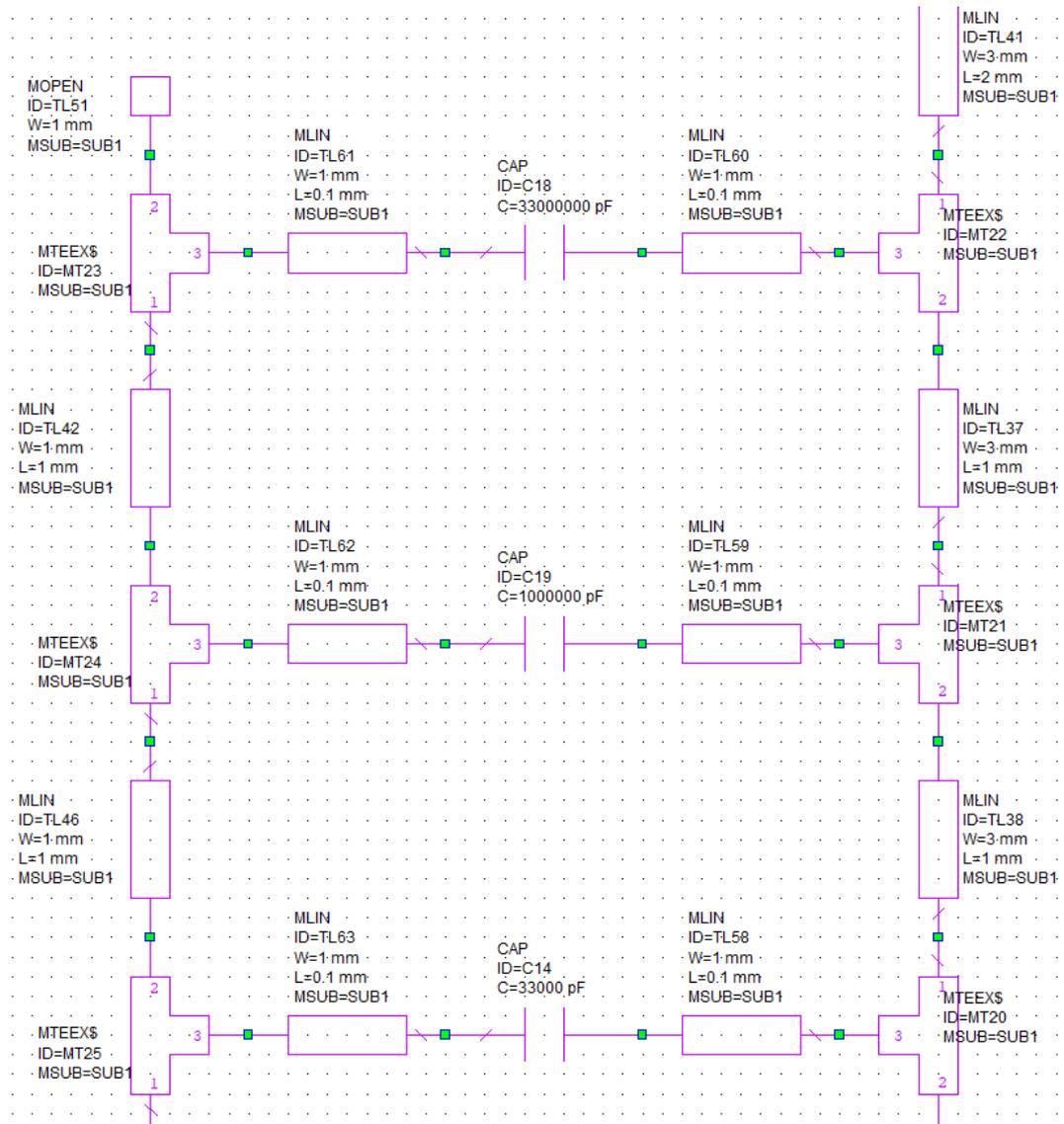
DC Section of Improved Final Design with Nonideal Lumped Elements

PART B



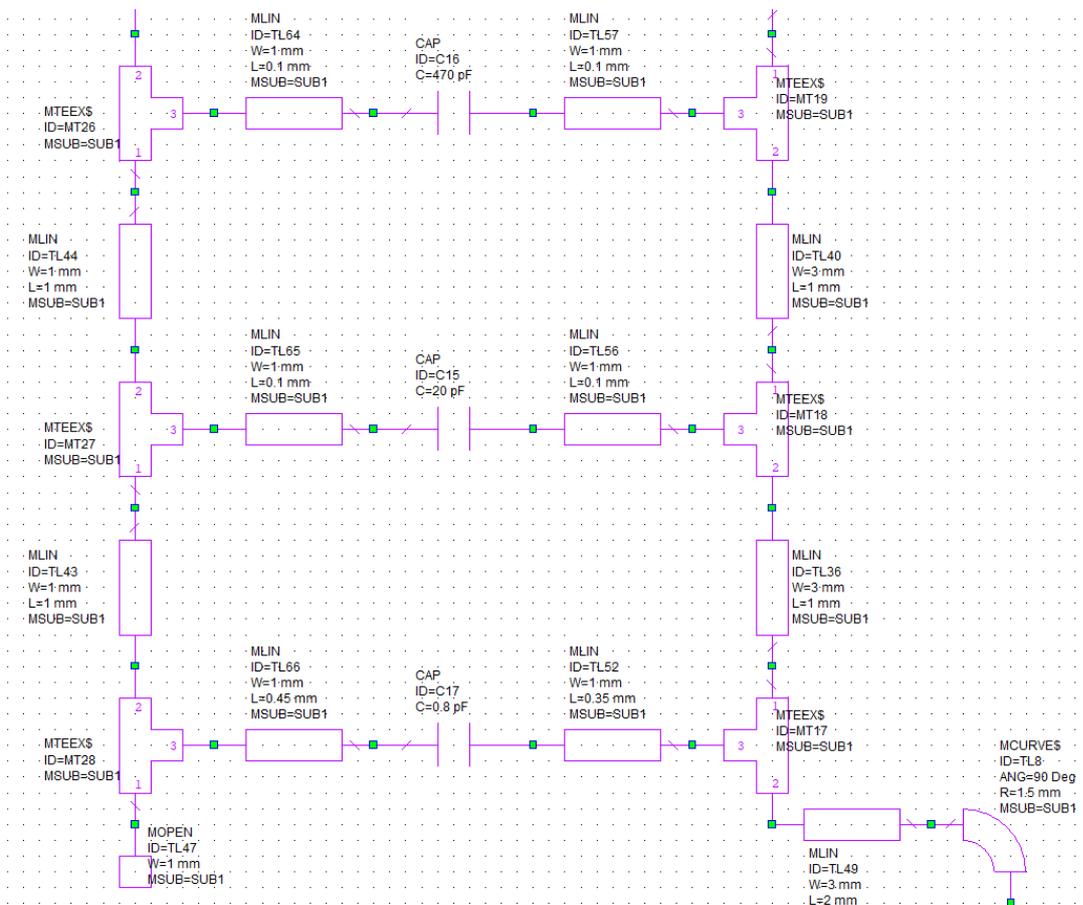
DC Section of Improved Final Design with Nonideal Lumped Elements

PART C



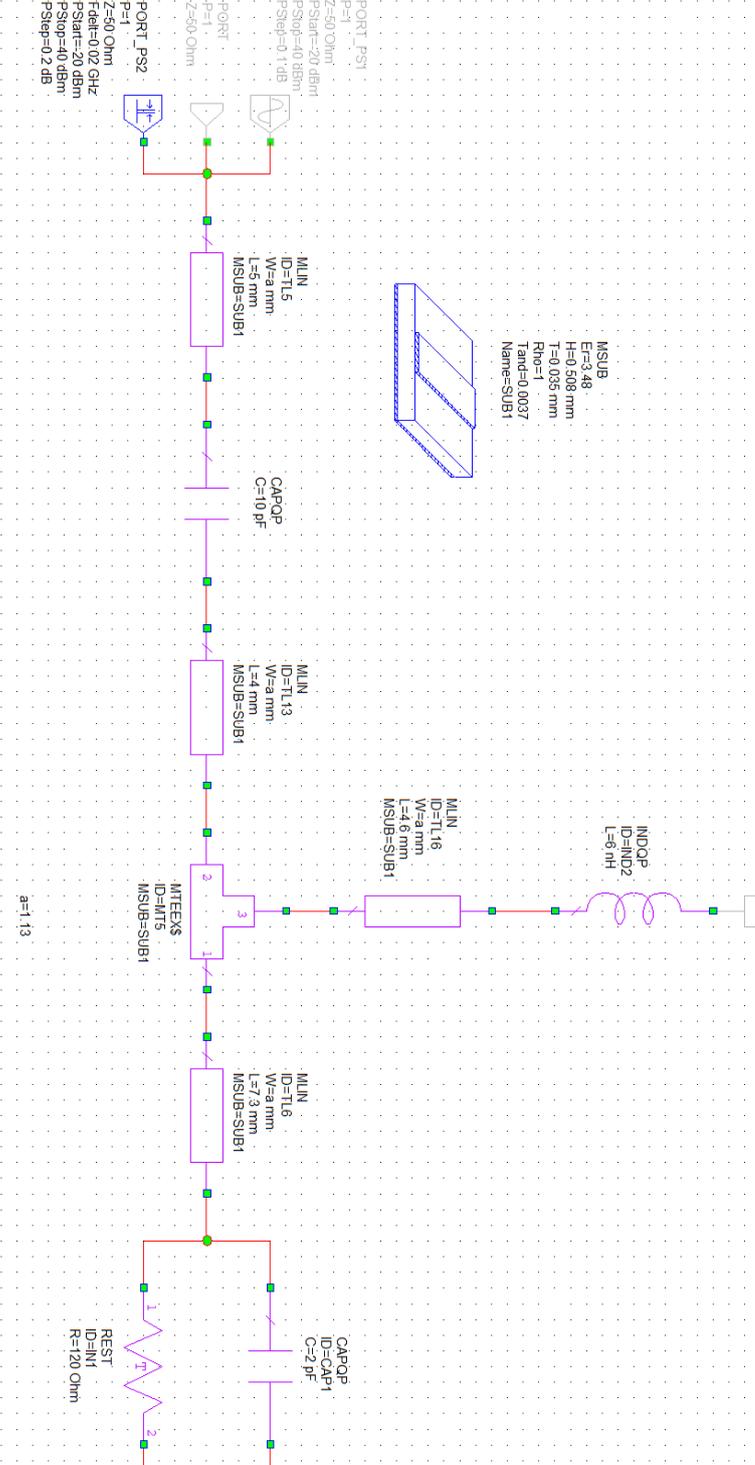
DC Section of Improved Final Design with Nonideal Lumped Elements

PART D



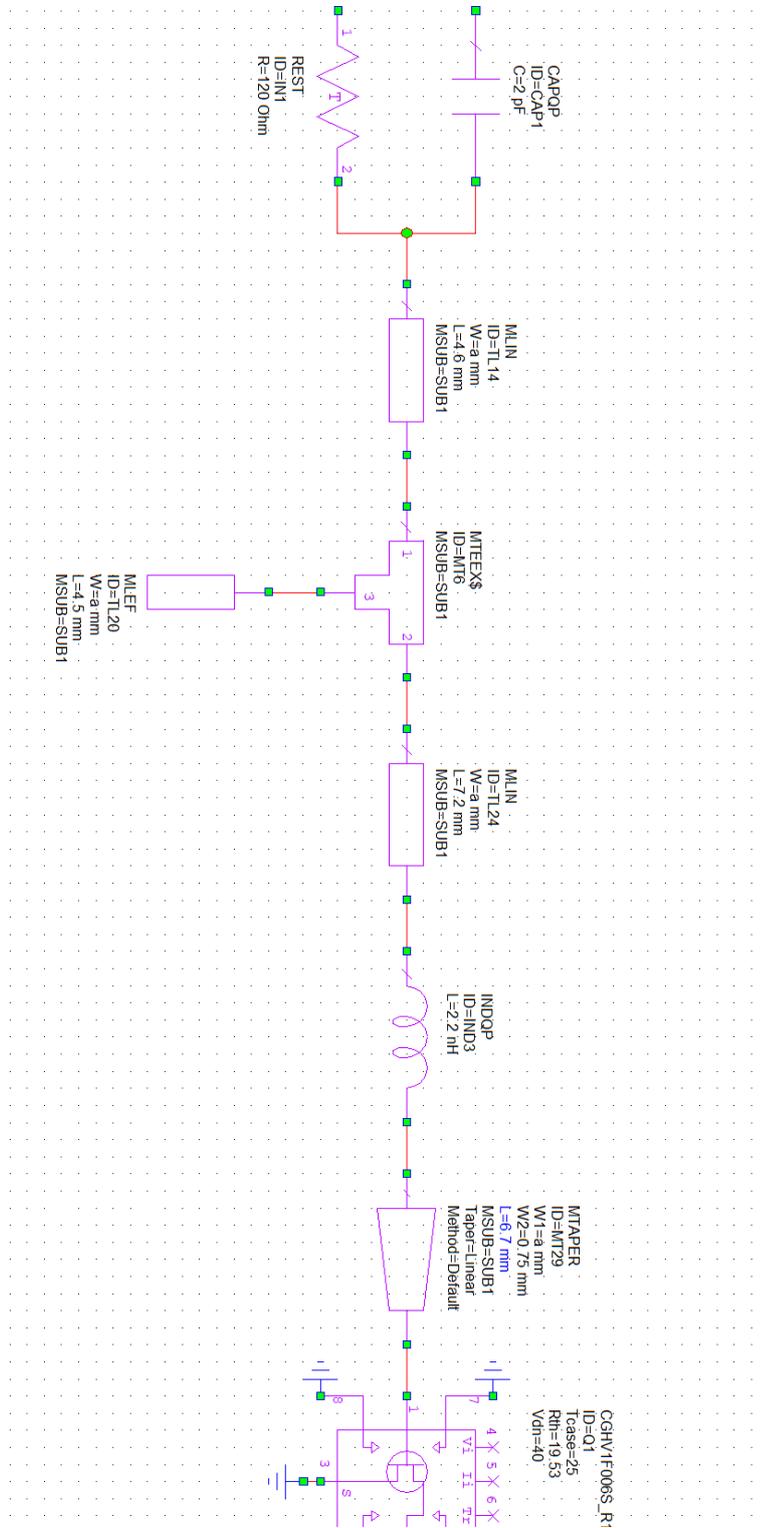
RF Section of Improved Final Design with Nonideal Lumped Elements

PART A



RF Section of Improved Final Design with Nonideal Lumped Elements

PART B



RF Section of Improved Final Design with Nonideal Lumped Elements

PART C

