

FABRICATION AND CHARACTERIZATION OF PEDOT:PSS HOLE  
TRANSPORT LAYERS FOR SILICON SOLAR CELLS

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TRANSPORT LAYERS FOR SILICON SOLAR CELLS**

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## **ABSTRACT**

### **FABRICATION AND CHARACTERIZATION OF PEDOT:PSS HOLE TRANSPORT LAYERS FOR SILICON SOLAR CELLS**

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Heterojunction silicon solar cells have gained considerable interest in recent years with the demonstration of record-high device performances. However, these devices are typically based on inorganic layers fabricated at high temperatures under vacuum environment, using toxic precursors. The low temperature budget, non-toxic chemical contents, and wide range of adjustability in physical and electrical properties make poly(3,4-ethylenedioxythiophene):poly(styrenesulfonate) (PEDOT:PSS) a promising candidate as an organic hole-transport layer (HTL) for low-cost silicon solar cells. In this thesis, effects of process conditions and chemical additives on the electrical performance of PEDOT:PSS layers on p-type silicon [(p)Si] are analyzed. Electrical performance is assessed in terms of contact resistivity and contact saturation current density. A rapid measurement procedure is proposed and utilized to extract contact resistivity of (p)Si/PEDOT:PSS interface, without the necessity for metal deposition or numerical simulations. Ultimately, contact resistivities smaller than  $0.3 \Omega \cdot \text{cm}^2$ , and contact saturation current densities near  $200 \text{ fA/cm}^2$  are demonstrated.

Keywords: solar cell, silicon, organic, heterojunction

## ÖZ

### **SİLİSYUM GÜNEŞ HÜCRELERİ İÇİN PEDOT:PSS DELİK GEÇİRGEN TABAKALARIN ÜRETİMİ VE KARAKTERİZASYONU**

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Hetero-eklem silisyum güneş hücreleri son zamanlardaki rekor yükseklikte verim değerlerinin gösterilmesiyle birlikte ilgi çekmektedir, ancak bu yüksek performanslı hücreler büyük oranda sağlığa zararlı kimyasallar kullanarak, yüksek ısı işlemlerinden geçerek ve vakum ortamında gerçekleştirilmektedir. Düşük ısı bütçesi, sağlığa zararlı olmayan kimyasal içeriği ve fiziksel ve elektriksel özelliklerinin geniş bir aralıkta ayarlanabilmesi PEDOT:PSS tabakalarını düşük fiyatlı hetero-eklem silisyum güneş hücreleri için umut vadeden bir aday yapmaktadır. Bu tez kapsamında, p-tipi silisyum [(p)Si] üzerine kaplanan PEDOT:PSS tabakalarının üretim koşullarının ve kimyasal bileşendeki değişikliklerin elektriksel performansa etkileri incelenmiştir. Elektrik performans kontak direnci ve pasivasyonu açısından farklı test yapıları kullanılarak incelenmiştir. (p)Si/PEDOT:PSS arayüzünün kontak direncinin ölçülmesi için metal kaplaması ve benzetim gerektirmeyen bir prosedür sunulmaktadır. Bu karakterizasyon yöntemlerine dayanan bir optimizasyon sürecinin sonunda  $0.3 \Omega \cdot \text{cm}^2$ 'den küçük bir kontak direnci ve yaklaşık  $200 \text{ fA/cm}^2$  değerinde kontak saturasyon akım yoğunluğu elde edilmiştir.

Anahtar Kelimeler: güneş hücresi, silisyum, organik, heteroeklem



To my family

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## LIST OF ABBREVIATIONS

### ABBREVIATIONS

2D	Two dimensional
3D	Three dimensional
4PP	Four-point probe
ARC	Anti-reflection coating
a-Si	Amorphous silicon
c-Si	Crystalline silicon
CZ	Czochralski
DIW	Deionized water
DMSO	Dimethyl sulfoxide
ETL	Electron transport layer
FZ	Float-zone
FF	Fill factor
FS	Fluorosurfactant
IPA	Isopropanol
IR	Infrared
HF	Hydrofluoric acid
HTL	Hole transport layer
PCD	Photo-conductance decay
PEDOT:PSS	poly(3,4-ethylenedioxythiophene):poly(styrenesulfonate)
poly-Si	Polycrystalline silicon
PES	Polyethylene sulfonate

PTFE	Polytetrafluoroethylene
RCA	Radio Corporation of America
SRH	Shockley-Read-Hall
TCF	Transparent conductive film
TL	Transport layer
TLM	Tranmission length method
UHV	Ultra-high vacuum
UV	Ultraviolet



## CHAPTER 1

### INTRODUCTION

#### 1.1 Historical evolution of silicon solar cells

Silicon solar cells have evolved considerably since the first cell demonstrated in 1942 [1]. Earlier cells, fabricated before the end of 1980s, had full area metal electrodes in direct contact with silicon at the rear surface [see Fig. 1.1] [2, 3]. The power conversion efficiencies (or briefly 'efficiencies') of these devices were limited by the high recombination rate near the silicon metal-interface, as well as the recombination in the relatively low quality silicon wafer bulk [see Fig. 1.2 (a)]. With the advances in the electronic quality of crystalline silicon wafers, losses associated with the surfaces have become the primary limiting factors in achieving higher efficiencies. With the introduction of partial metal contacting at the rear side, and a dielectric passivation layer in between these metal contacts, the efficiencies had increased significantly [4]. Ultimately, an efficiency of near 25 % was achieved in mid 1990s in a laboratory environment with the partial rear contact structure [1, 5]. However, the relatively complicated processing of this high efficiency cell was not suitable for the fabrication of low-cost, industrial solar cells. It was not until late 2000s where this device structure became compatible with industrial scale fabrication processes, and became one of the most widely utilized solar cell device structures of today [6, 7]. The progress with these devices on an industrial scale is still on-going with a relatively steady increase in cell efficiencies [8, 9]. However, ultimately this device structure is expected to reach an efficiency plateau due to the direct contact between the metal-silicon base. Hence, a higher performance cell structure is currently of significant interest to the community: cells with passivated contacts. The main characteristic of a passivated contact is that the metal is not in direct contact with the silicon base [10]. The inter-

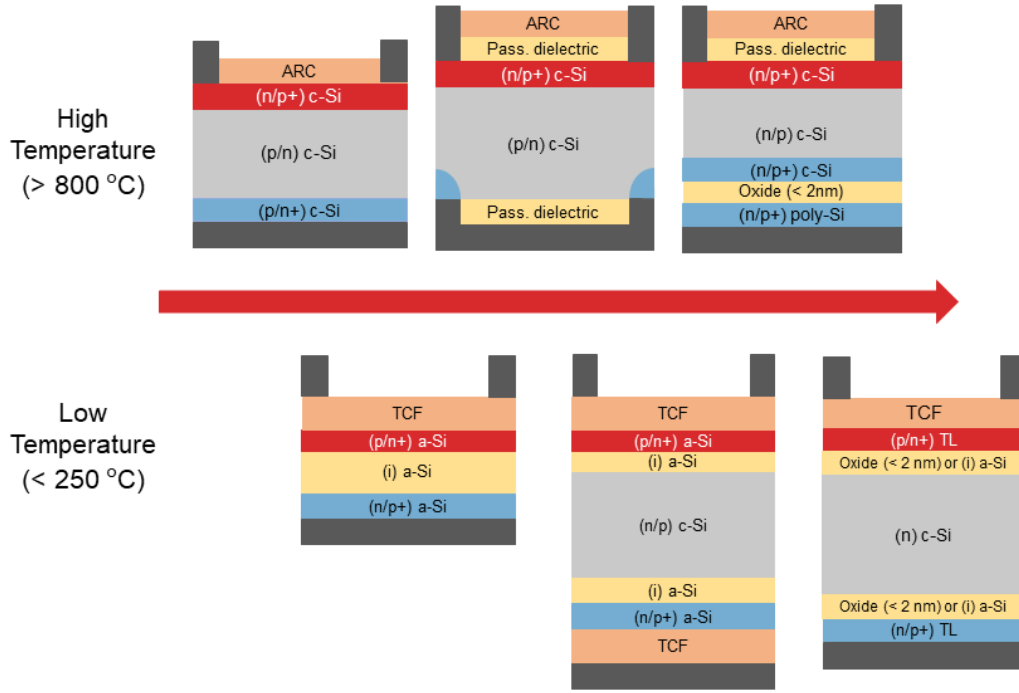


Figure 1.1: Evolution of silicon solar cells fabricated by low ( $< 250\text{ }^{\circ}\text{C}$ ) and high ( $> 800\text{ }^{\circ}\text{C}$ ) temperature processes. The red horizontal arrow represents the time flow with the left-end representing earlier times. The spacing between the schematics are not in scale.

layer between silicon and metal can be an ultra-thin dielectric layer, or an electron or hole selective transport layer (denoted briefly as 'hole/electron transport layer' or 'carrier transport layer' throughout the thesis) which is a semiconductor layer that is typically thicker than the thin dielectrics, or a combination of both the transport and thin dielectric layers. In general, an ultra-thin dielectric layer in contact with a transport layer having a high doping density can suppress the minority carrier concentration at the metal interface very effectively. For instance, it was shown that a very thin silicon oxide layer ( $< 2\text{ nm}$ ) between a highly doped polycrystalline silicon (poly-Si) layer and the silicon base, and an additional dopant diffused layer in the c-Si base yields extremely low recombination rates near the surface, while still maintaining low contact resistivity [11]. With increasing interest in this particular device structure in 2010s, cell efficiencies above 26 % was recently achieved in laboratory environment [12]. However, one of the main drawbacks of the poly-Si contacts and the mentioned preceding device structures is that they rely on high temperature pro-



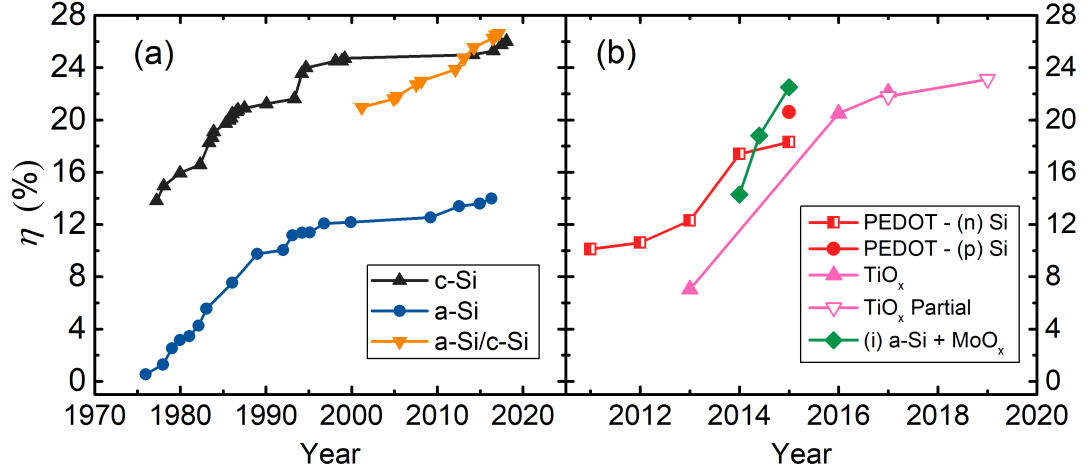


Figure 1.2: Evolution of power conversion efficiencies of (a) crystalline silicon (c-Si), amorphous silicon (a-Si) and c-Si/a-Si hybrid silicon solar cells, (b) c-Si based solar cells with non-silicon based carrier transport layers.

cesses ( $> 800^\circ\text{C}$ ) performed under a vacuum environment (e.g. doping), which also rely on toxic chemicals, limiting the cost-reduction potential of the devices. Therefore, there is still a need for simpler and non-toxic fabrication techniques that would yield high performance-to-cost ratios.

One of the first demonstrations of low temperature silicon solar cells ( $< 250^\circ\text{C}$ ) was based on thin amorphous silicon (a-Si) layers, with an intrinsic layer between the amorphous p- and n-type layers, instead of the thick and doped crystalline silicon base [13]. Despite the advances in this technology over decades, and its common use in consumer electronics, the device structure offers limited efficiencies compared to its alternatives which are more suitable for large scale energy production [Fig. 1.2 (a)]. With the utilization of a doped c-Si as the absorber layer instead of the intrinsic amorphous silicon [(i) a-Si] layer, however, the efficiencies of devices utilizing a-Si layers have increased drastically [14]. In this device structure, thin (i) a-Si serve as extremely good passivation layers for the c-Si absorber surface, while the highly doped (p) a-Si and (n) a-Si serve as carrier transport layers. Today, the highest efficiency single-junction silicon solar cell (26.7 %) utilizes such a-Si layers on c-Si surfaces [15]. However, despite the reduced temperature budget, this technology still relies on processes performed in vacuum environment and the industrial fabrication equipment

is relatively expensive compared to its alternatives, due to the delicate processing conditions.

Over the last decade, carrier transport layers based on materials other than silicon have also been demonstrated as viable candidates. In this respect, Fig. 1.2 (b) shows the efficiencies of prominent examples of such devices, with various device structures. Among these examples,  $\text{MoO}_x$  is a hole transport layer that is typically fabricated using thermal evaporation and works the best when a thin (i) a-Si layer is inserted between  $\text{MoO}_x$  and c-Si. Currently, the record cell efficiency for this layer is 22.5 %, where it was utilized in a hybrid configuration with the layer deposited at the front side as an emitter, combined with an (n) a-Si layer at the other side of the cell [16]. Configurations without (i) a-Si typically yield worse interface passivation, yet still viable performance overall [17].  $\text{TiO}_x$ , on the other hand, is an electron transport layer (ETL) that is typically deposited by atomic layer deposition and can yield very high quality passivation along with a low contact resistivity, without the need for an (i) a-Si layer. For these devices, an efficiency record of 22.1 % was demonstrated for a hybrid configuration with a full-area  $\text{TiO}_x$  as an ETL at the rear side, and a diffused boron emitter at the front side [18]. An improved efficiency of 23.1 % was recently achieved recently for a hybrid cell utilizing a diffused homojunction emitter at the front side, and a partially contacted  $\text{TiO}_x$  transport layer combined with a passivating dielectric at the rear side [19]. This is also the highest efficiency that had been achieved for a cell utilizing a transport layer material other than silicon so far. Besides the hybrid cells, complete heterojunction cells were also realized by, for example, utilizing full-area (i) a-Si/ $\text{MoO}_x$  and  $\text{TiO}_x$  contacts at the front and rear side of the cell, respectively, with a record-high efficiency of 20.7 % [20]. Furthermore, although most demonstrations of alternative transport layer materials in literature are currently with inorganic materials, an organic material, PEDOT:PSS which is deposited by spin-coating from a dispersion under ambient air, have also been demonstrated as a highly viable candidate [21]. In first demonstrations of devices utilizing PEDOT:PSS, the layers were deposited at the front side of an n-type c-Si base as an emitter [22, 23, 24]. However, it was later shown that if the layer is used at the rear-side of p-type c-Si base an HTL, much higher efficiencies can be achieved, and indeed, a record-high efficiency of 20.6 % was demonstrated [21]. Given that PEDOT:PSS layers are the primary focus of this

thesis, more details on them are to be discussed in an upcoming section.

Overall, although only a couple of outstanding results are shown here for transport materials alternative to silicon, there is a wide range of possibilities in terms of material choice, especially considering the parallel nature of the research with heterojunction devices based on absorber materials alternative to silicon (e.g. perovskite) where a large literature on different carrier transport layers exist. Furthermore, solar cells utilizing such different transport layer materials have typically been quite diverse in terms of device structure they are utilized in. These differences make it hard to make a fair comparison in terms of device efficiency. A comparison in terms of performance parameters that are specifically related to the contact quality of silicon and the transport layers is more informative. These parameters are discussed in the following section.

## 1.2 Performance parameters of solar cells

The electrical characterization and performance assessment of silicon solar cells have been particularly detailed, possibly due to the technological advancements that have progressed in parallel with the semiconductor industry and the availability of standardized silicon wafers to a wide community. Combined with the progress in the rapid device simulation tools that are free of cost [25], the lower level performance parameters (e.g. surface recombination velocity) that are important for the high level performance parameters (e.g. cell efficiency) have also become more widely acknowledged [26]. Accordingly, the experimental extraction and reporting of the individual lower level performance parameters have gained more significance, and have become more widely demanded by the community. Here, the parameters that are relevant to this thesis are described briefly to lay a background for the analyses presented in following chapters.

The relation between the current density ( $J$ ) and voltage ( $V$ ) of a solar cell can be expressed, assuming a single diode formation, unity ideality factor and an infinitely-large shunt resistance, as

$$J(V) = J_{sc} - J_0 \left( e^{(V+J(V)R_s)/V_{th}} - 1 \right) \quad (1.2.1)$$

where  $J_{sc}$  is the short-circuit current density which is a function of the spatial photo-generation rate and minority carrier collection probability throughout the device,  $J_0$  is the saturation current density which is a function of the cumulative recombination rate, and  $R_s$  is the area weighted series resistance which is the sum of resistive losses in the device. Besides the explicitly expressed  $J_{sc}$  in Eq. (1.2.1), the main (or the high level) performance parameters of a solar cell are the open-circuit voltage  $V_{oc}$ , the fill-factor (FF), and the cell efficiency ( $\eta$ ). The FF is defined as

$$FF = \frac{V_{mpp} J_{mpp}}{V_{oc} J_{sc}}, \quad (1.2.2)$$

where  $V_{mpp}$  and  $J_{mpp}$  are the voltage and current density at the maximum power point of the device, and  $\eta$  is the ratio of the maximum output power that can be supplied by the device divided by the incident power on the device ( $P_{in}$ ), expressed as

$$\eta = \frac{V_{oc} J_{sc} FF}{P_{in}}. \quad (1.2.3)$$

The low level performance parameters in a solar cell are those that contribute to the total  $J_0$  and  $R_s$  in Eq. (1.2.1), which are the determinants of the high level performance. The total  $J_0$  and  $R_s$  in a device is typically a sum of individual loss channels associated with different locations of the device. The majority carrier contact resistivity ( $\rho_c$ ) and the contact saturation current density ( $J_{0c}$ ) are the two low level parameters that quantitatively represent the resistive and recombination losses, and hence the electrical performance of a carrier transport layer. Whereas a high  $\rho_c$  corresponds to a high  $R_s$  and a low FF, a high  $J_{0c}$  represents a high recombination rate and a low  $V_{oc}$  (and a low FF if  $J_{0c}$  is too excessive [27]). The current density ( $J$ ) of a hypothetical solar cell having electrical losses only at one of the full-area contacts can then be expressed, analogous to Eq. (1.2.1), as

$$J(V) = J_{sc} - J_{0c} \left( e^{(V+J(V)\rho_c)/V_{th}} - 1 \right). \quad (1.2.4)$$

Solving this equation through a numerical iteration method yields the maximum achievable  $V_{oc}$ , FF, and  $\eta$  of a solar cell utilizing the transport layer with the given  $J_{0c}$  and  $\rho_c$ . Figure 1.3 shows the effect of  $J_{0c}$  and  $\rho_c$  on  $\eta$ . Full-area contacts having low  $\rho_c$ , below approximately  $0.3 \Omega\text{cm}^2$ , limit the  $\eta$  mainly through  $J_{0c}$ . For  $0.3 \Omega\text{cm}^2 < \rho_c < 2 \Omega\text{cm}^2$ , both  $J_{0c}$  and  $\rho_c$  are crucial. For  $\rho_c > 2 \Omega\text{cm}^2$ , on the other hand, resistive losses dominate and  $\rho_c$  dominate  $\eta$ . Ultimately, a carrier transport layer should

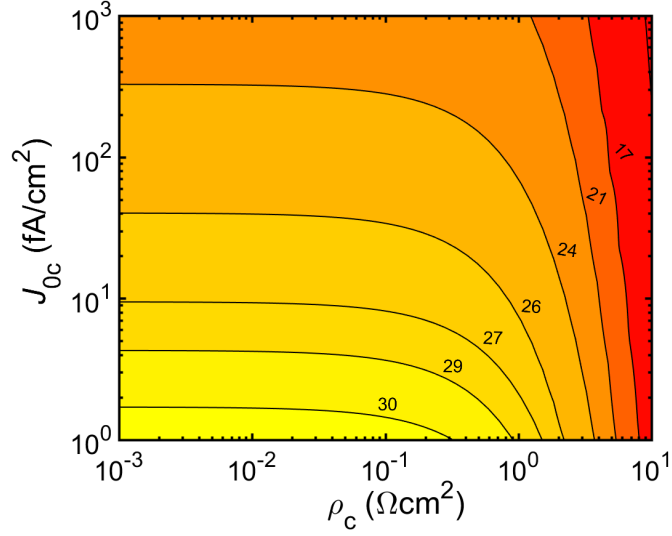


Figure 1.3: Power conversion efficiency versus contact resistivity ( $\rho_c$ ) and contact saturation current density ( $J_{0c}$ ) calculated by the numerical solution of Eq. (1.2.4), assuming a constant  $J_{sc} = 43.8 \text{ mA/cm}^2$ .

be optimized to realize the highest efficiency, similar to a results shown in Fig. 1.3, yet by taking into account all the contributors to  $J_0$  and  $R_s$  in the device and not those related to just one contact.

Lastly, note that alternative to the numerical calculation of Eq. (1.2.1), high level performance parameters can be calculated using low level parameters through relatively simple relations.  $V_{oc}$  can be expressed by a re-arrangement of Eq. (1.2.1) at  $J(V) = 0$ , yielding

$$V_{oc} = V_{th} \ln \left( \frac{J_{sc}}{J_{0c}} + 1 \right). \quad (1.2.5)$$

Also, FF can be expressed by an empirical model [28]

$$FF_0 = \frac{v_{oc} - \ln(v_{oc} + 0.72)}{v_{oc} + 1}, \quad (1.2.6)$$

$$FF = FF_0(1 - 1.1r_s) + \frac{r_s^2}{5.4}, \quad (1.2.7)$$

where  $FF_0$  is the recombination limited fill factor,  $v_{oc}$  is the  $V_{oc}$  normalized to  $V_{th}$ , and  $r_s = R_s/(V_{oc}/J_{sc})$  is the series resistance normalized to the characteristic resistance of the device. The expression in Eq. (1.2.7) is accurate to four digits in the third decimal place for  $v_{oc} > 10$  and  $r_s < 0.4$ . Overall, these relations are useful for the

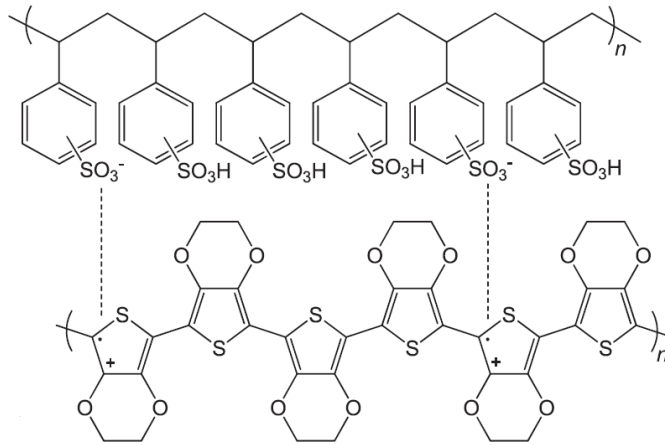


Figure 1.4: Chemical structure of PEDOT:PSS, with the PSS chain shown on the top and the PEDOT chain on the bottom. Image retrieved from [29].

conversion of lower level parameters to high level solar cell parameters, without the need for an iterative method.

### 1.3 An overview of PEDOT:PSS and its use as a hole transport layer in silicon solar cells

The discovery of a conductive polymer in 1977 was one of the major events of the century [30]. With electrical properties that can be varied between an insulator and a metal, and high processability of polymers, these materials were utilized in applications such as organic electronic devices, and eventually resulted in a Nobel prize in chemistry to its founders in 2000. Poly(3,4 ethylenedioxythiophene) (PEDOT) is one of these conductive polymers, first discovered in 1988 [31]. However, PEDOT alone does not dissolve in common solvents and is not easily processable since it does not remain stable in an aqueous dispersion. To keep the positively charged PEDOT arising from the polymerization process stabilized and to yield a stable aqueous dispersion, negatively charged poly(styrenesulfonate) (PSS) was utilized, ultimately forming the polymer blend called PEDOT:PSS. In an aqueous dispersion of the blend, the hydrophobic and electrically conductive PEDOT chains are covered by the hydrophilic, and electrically insulating PSS chains, forming a core-shell structure. The conductive PEDOT:PSS grains and the free PSS filling in between them

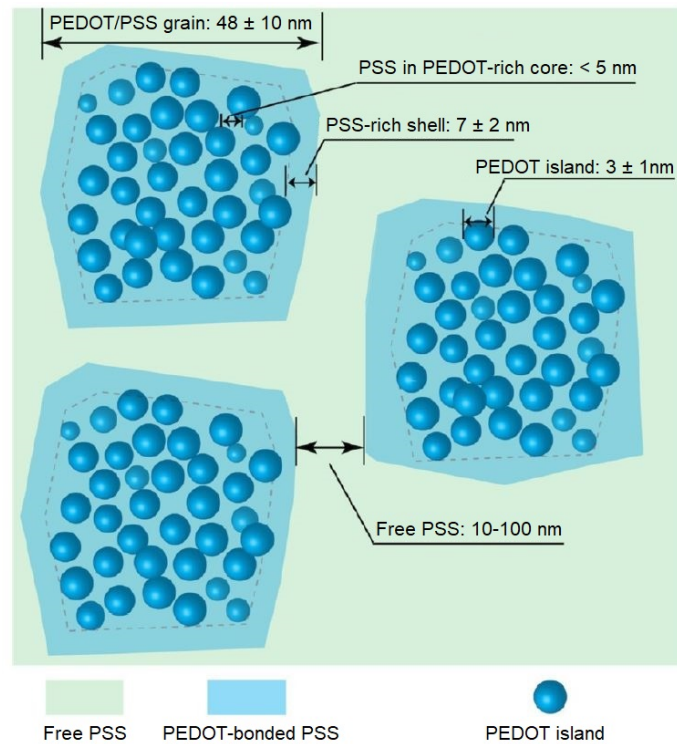


Figure 1.5: Morphological model of a pristine PEDOT:PSS film. Image retrieved from [32].

yield the morphological structure shown in Fig. 1.5 upon dry film formation. In a chemically unmodified form, these films still are not sufficiently conductive to be used in electrical applications due to the excess insulating PSS surrounding the PEDOT:PSS grains [32]. To improve electrical conductivity, chemical additives called 'secondary dopants' was first incorporated in the dispersion in 2001 [33]. These secondary dopants remove the excess PSS from the films, result in an improved interconnection between the PEDOT grains and yield a higher film conductivity that is suitable for device applications.

Following the commercialization of PEDOT:PSS dispersions and the key discovery on secondary dopants, PEDOT:PSS have been utilized in wide range of applications including solar cells, energy storage devices, thermoelectric devices, humidity sensors, and flexible electronic devices [34, 35]. The number of total publications on PEDOT:PSS spread among various fields are currently between 4,900-12,000, those on solar cells utilizing PEDOT:PSS for any solar cell structure are between 700-4,700,

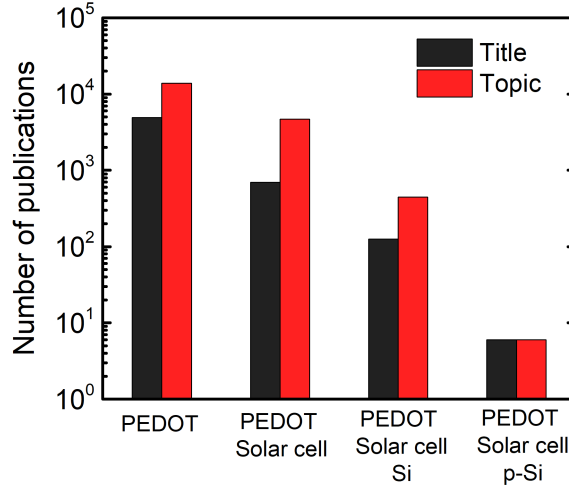


Figure 1.6: Number of publications having a title with the exact key-words related to PEDOT:PSS, and those that are related to PEDOT:PSS, yet without the exact key-word match at the title. Data taken from Web of Science in August, 2019 [36].

those on silicon solar cells utilizing PEDOT:PSS are between 125-445, and lastly those utilizing specifically a p-type silicon base with a PEDOT:PSS layer is 6 [36]. Overall, the total literature on PEDOT:PSS is extremely vast, yet the share of silicon based solar cells is only minor compared to the total.

The first proof-of-concept for Si-PEDOT:PSS solar cells was demonstrated by Avatshi et al. in 2011 [22], where PEDOT:PSS was used as an HTL at the front side of an n-type silicon cell with an efficiency of 10.1 %. Following this demonstration, efficiencies were improved by a few percent in the following years with the same device structure [23, 24]. Yet, the significant leap in efficiencies occurred with the identification of the major loss mechanism for these devices: the parasitic light absorption in PEDOT:PSS at the front side where light enters the device. Accordingly, by inserting PEDOT:PSS at the rear side of n-type silicon, an efficiency of 17.4 % was achieved for the 'backPEDOT' type cells in 2014 [37]. However, an emitter layer at the rear side of a device is disadvantageous in terms of minority carrier collection and demanding in terms of wafer bulk and front surface quality. Therefore, by replacing the n-type base with a p-type one, an efficiency of 20.6 % was finally achieved in 2015 [21], which is also the highest efficiency reported for a Si-PEDOT:PSS solar cell to date. However, curiously, there is no other demonstration of (p)Si/PEDOT:PSS cells by



another work group besides the group that demonstrated the record-high efficiencies in the first place. Moreover, the experimental details of these high efficiency devices has not been disclosed except for a brief mention of the silicon surface preparation step, and use of 'adapted' [21] and 'special grade' [38] PEDOT:PSS blends seemingly supplied by the leading PEDOT:PSS manufacturer Hereaus GmbH, who appears as a partner in all the works [37, 39, 21, 40, 21, 41, 42, 38]. The details of how a very high performing PEDOT:PSS contact is fabricated still hold great value, yet remain an unknown to the community.

#### **1.4 Outline of the Thesis**

There are two main objectives of this thesis; development of a characterization scheme for the performance assessment of PEDOT:PSS layers on p-type silicon surfaces, and use of this characterization scheme to identify the effects of different experimental procedures and chemical additives on the electrical performance of these layers. Accordingly, Chapter 2 of the thesis describes the characterization methodology utilized in the thesis to extract the low level performance parameters discussed in Chapter 1.2, namely  $J_{0c}$  and  $\rho_c$ . In Chapter 3, details on silicon surface preparation, the fabrication procedure of PEDOT:PSS layers, and the electrical performance and the stability of the fabricated layers are presented. Finally in Chapter 4 the key findings of the thesis are highlighted and future work on the subject is discussed.



## CHAPTER 2

### CHARACTERIZATION METHODOLOGY

#### 2.1 Surface passivation

In the thesis, contactless photo-conductance decay measurements were utilized for the extraction of  $J_{0c}$ . With these technique, the sample is illuminated from the top by an IR-lamp flash with a decaying light intensity, and the conductance change associated with the photogenerated carriers in the wafer is measured by inductive coils located underneath the sample. A schematic of the measurement setup is provided in Fig. 2.1. Since the measurement is contactless and there is no net current flowing through the sample, the cumulative generation rate is balanced by the recombination rate within the sample, yielding

$$\iiint G(x, y, z) dx dy dz = \iiint U(x, y, z) dx dy dz, \quad (2.1.1)$$

where  $G(x, y, z)$  and  $U(x, y, z)$  are the generation and recombination rates within the sample, respectively, and the integration is throughout the entire volume of the sample. Considering that the sample is laterally homogeneous in two-dimensions, and that the generation rate and excess carrier concentration ( $\Delta n = \Delta p$ , assuming quasineutrality) is uniform in the quasineutral bulk of the wafer, Eq. (2.1.1) simplifies to

$$G = \frac{\Delta n}{\tau_{\text{eff}}} \quad (2.1.2)$$

where  $\tau_{\text{eff}}$  is the effective minority carrier lifetime which is a combination of various recombination channels within the wafer including the Shockley-Read-Hall (SRH) recombination both at the bulk and at the surfaces, and the intrinsic recombination in silicon, namely Auger and radiative recombinations. Separating the bulk and surface recombination channels, assuming that the recombination at the surfaces is symmet-

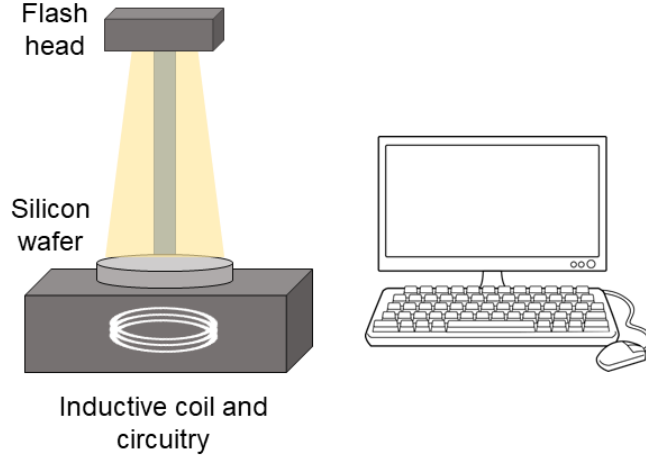


Figure 2.1: A schematic of the photoconductance decay measurement setup.

rical and is dominated mainly by SRH recombination yields

$$\frac{\Delta n}{\tau_{\text{eff}}} = 2J_{0c} \frac{np - n_i^2}{qWn_i^2} + \frac{\Delta n}{\tau_{\text{bulk}}} \quad (2.1.3)$$

where  $J_{0c}$  is the surface saturation current density,  $n$  and  $p$  are the electron and hole concentrations in the quasi-neutral bulk,  $n_i$  is the intrinsic carrier concentration,  $W$  is the thickness of the bulk, and  $\tau_{\text{bulk}}$  is the bulk minority carrier lifetime. Under high-injection conditions ( $\Delta n \gg N_A$  or  $N_D$ ), Eq. (2.1.3) becomes

$$\frac{1}{\tau_{\text{eff}}} - \frac{1}{\tau_{\text{bulk}}} = \frac{2J_{0c}}{qWn_i^2} \Delta n. \quad (2.1.4)$$

Calculation of  $J_{0c}$  from Eq. (2.1.4) requires the knowledge of  $\tau_{\text{bulk}}$ , which is not precisely known when the the bulk of the wafer is highly defective and the cumulative recombination is dominated by SRH recombination. However, when high-resistivity FZ wafers are utilized, the intrinsic recombination associated with Auger recombination is much more dominant than SRH recombination under high-injection conditions and bulk lifetime can be calculated with high accuracy ( $\tau_{\text{bulk}} = \tau_{\text{intrinsic}}$ ). Assuming  $J_{0c}$  is independent of  $\Delta n$ , the right-hand side of Eq. (2.1.4) becomes a function of  $\Delta n$ , and with the knowledge of  $\tau_{\text{eff}}$  extracted from the PCD measurement,  $J_{0c}$  can be calculated from the slope of a  $\tau_{\text{eff}}^{-1} - \tau_{\text{intrinsic}}^{-1}$  versus  $\Delta n$  relation.

## 2.2 Contact resistivity

For the extraction of  $\rho_c$  associated with the hole transfer from silicon to PEDOT:PSS layers, two main test structures were utilized. Whereas one relies on metallized test structures, the other does not require a metallization procedure, and allows for a much faster evaluation of  $\rho_c$ . In the following two sub-sections, the methodology associated with these test structures and their limitations are discussed.

### 2.2.1 Metallized test structures

The metallized structures used for the evaluation of  $\rho_c$  of PEDOT:PSS/(p)Si interface had full area contacts on both sides of the wafer. These structures had both sides coated with PEDOT:PSS due to their relatively simple fabrication procedure. However, this simplicity comes at the cost of uncertainty when the contacts are non-ohmic. In case of a non-ohmic contact, the resistance associated with the current flow from PEDOT:PSS to silicon and from silicon to PEDOT:PSS is different, and the measured  $\rho_c$  is a combination of both these mechanisms and the resistivity associated with the bulk of silicon, which can be expressed as

$$\rho_{\text{total}} = \rho_{\text{PS}} + \rho_{\text{bulk}}W + \rho_{\text{SP}} \quad (2.2.1)$$

where  $\rho_{\text{total}}(\Omega\text{cm}^2)$  is the total resistivity of the test structure,  $\rho_{\text{PS}}$  is the contact resistivity of hole transport from PEDOT:PSS to silicon,  $\rho_{\text{bulk}}(\Omega\text{cm})$  is the bulk resistivity of the silicon wafer,  $W$  is the wafer thickness, and  $\rho_{\text{SP}}$  is the contact resistivity of hole transport from silicon to PEDOT:PSS. If the thickness of the wafer is measured by precisely by a certain characterization method (e.g. scanning electron microscopy), the contribution of wafer bulk to Eq. (2.2.1) can also be known precisely when combined with the four point probe measurements of the wafer. However, the extraction of the exact wafer thickness may be time consuming, and possibly destructive for the sample. Assuming that the specified range of error for the wafers by the wafer supplier is accurate, the uncertainty associated with the wafer thickness brings an uncertainty of  $R_{\text{Si}}(W \times |U^2 - 2U|)^2$ , where  $U$  is the fractional uncertainty of wafer thickness and  $R_{\text{Si}}$  is the sheet resistance of the bare silicon wafer measured by a four-point probe setup. Considering that the wafers utilized in this thesis had a specified

thickness of  $279 \pm 15 \mu\text{m}$ , and  $\rho_{\text{bulk}}$  specification between 1-5  $\Omega\text{cm}$ , the uncertainty in the measurements is less than  $20 \text{ m}\Omega\text{cm}^2$ . This brings about an uncertainty of less than 10% for  $\rho_{\text{total}} > 200 \text{ m}\Omega\text{cm}^2$ , which was the range of interest in this study.

The uncertainty in terms of both  $\rho_{\text{SP}}$  and  $\rho_{\text{PS}}$  is larger than that of the contribution of the bulk since the geometrical symmetry of the structures obscures the individual identification of the two mechanisms. A deeper analysis of the interface can perhaps yield a model that can enable the identification of individual sources, yet this is out of the scope of this work. Ultimately, the metallized measurements utilized in this work, in fact, yield an upper limit for  $\rho_{\text{SP}}$ , and its actual value may be overshadowed by  $\rho_{\text{PS}}$ , which is not of direct interest for solar cell operation. To overcome the question of ohmic nature of (p)Si/PEDOT:PSS contacts, and to identify  $\rho_{\text{SP}}$  more precisely, structures having very low  $\rho_c$  for both current flow directions can be utilized. However, this requires single side processing with multiple additional process steps with increased complexity, and such procedure was not utilized in this thesis.

## 2.2.2 Non-metallized test structures

A methodology involving four-point probe (4PP) measurements for the extraction of  $\rho_c$  between transport layers and silicon of the same type (e.g. n or p) has been recently proposed as a practical alternative to measurements involving patterning and metallization steps (e.g. Cox and Strack and TLM) [44]. The methodology relies on the measurement of the following sheet resistances:

1. bare silicon wafer ( $R_{\text{Si}}$ ),
2. transport layer on a highly-resistive substrate (e.g. glass, or highly resistive silicon wafer) ( $R_{\text{TL}}$ ),
3. transport layer on the silicon wafer measured at the first step ( $R_{4\text{PP}}$ ).

Using the measured  $R_{\text{Si}}$  and  $R_{\text{TL}}$ , one can simulate  $R_{4\text{PP}}$  for varying  $\rho_c$  values using, for example, a three-dimensional finite-element-method solver. The simulation results of  $R_{4\text{PP}}$  can then be used to fit  $\rho_c$  to the experimentally measured  $R_{4\text{PP}}$ . However, some of the main softwares than can be utilized for this purpose are not available

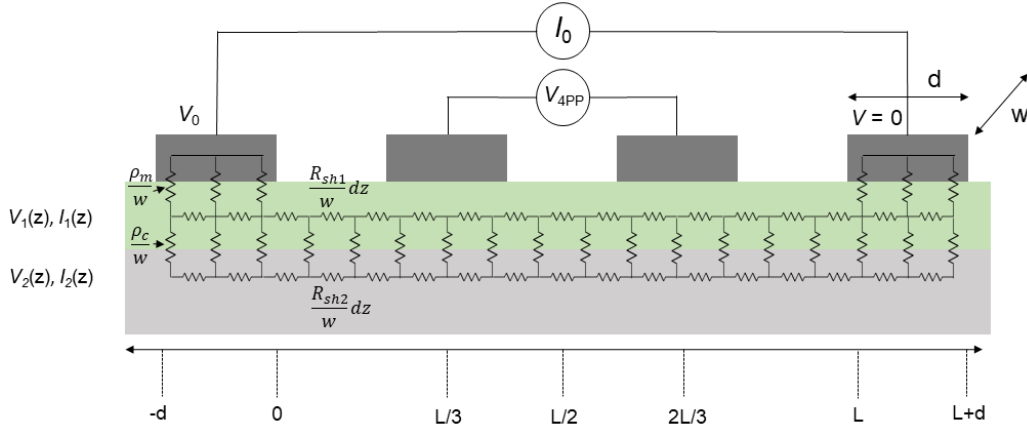


Figure 2.2: Two-dimensional circuit schematic representation of four-point probe measurement of a heterojunction structure.  $L$  is the spacing between the current supplying outer probes, with equal distance between each probe,  $d$  is the width of the probe tips,  $w$  is the depth of the structure,  $R_{TL}$  is the sheet resistance of the transport layer (TL),  $R_{Si}$  is the sheet resistance of silicon, and  $\rho_c$  is the contact resistivity between the TL and silicon.

to a large portion of community, and performing simulations for each sample is not time-effective, especially considering a 3D structure. Ultimately, availability of an analytical formulation for  $R_{4PP}$  can increase the accessibility of the technique.

Here, an analytical approach is utilized assuming a 2D geometry, and the results of this model is compared to the results of 3D simulations performed using Silvaco ATLAS. A schematic of the modeled 4PP structure is provided in Fig. 2.2. It is assumed here that the contact resistivity between the voltage sensing inner contacts and the underlying layer is infinitely-large, and hence the probes do not induce any electrical change within the measured structure. It is further assumed that the sensed voltage is equal to the voltage of the underlying layer at the middle of the voltage-sense contacts that are located at  $z = L/3$  and  $z = 2L/3$ , resulting in the following expressions for the measured voltage and resistance

$$V_{4PP} = V_1(L/3) - V_1(2L/3), \quad (2.2.2)$$

$$R_{4PP} = \frac{V_{4PP}}{I_0}. \quad (2.2.3)$$

Under these assumptions, the electrical structure of the problem is the same analyzed

by Huang et al. for TLM measurements of heterojunction layers [45], where two main regions and sets of equations are defined under the metal contacts and outside them. Accordingly, the solution to the current problem on 4PP just requires a rearrangement and derivation of some of the unknowns not provided in the original work. Whereas the details of this derivation is provided in Appendix A, the outcome of it is provided below

$$R_{4PP} = \left[ \frac{R_{sh1}}{wk_p} (a_{1p}(e^{k_p 2L/3} - e^{k_p L/3}) - b_{1p}(e^{-k_p 2L/3} - e^{-k_p L/3})) + \frac{R_{sh1}}{wk_n} (a_{1n}(e^{k_n 2L/3} - e^{k_n L/3}) - b_{1n}(e^{-k_n 2L/3} - e^{-k_n L/3})) \right] \left[ \frac{L}{w} \left( \frac{R_{sh1} R_{sh2}}{R_{sh1} + R_{sh2}} \right) + \frac{2}{(\lambda_p - K)G_n} \left( \frac{R_{sh1} - K R_{sh2}}{R_{sh1} + R_{sh2}} \right) \right] / V_0 \quad (2.2.4)$$

where  $R_{sh1}$  and  $R_{sh2}$  are the sheet resistances of layers that are in direct contact with the probe head and not in contact with it, respectively,  $k_p$ ,  $k_n$ ,  $a_{1p}$ ,  $a_{1n}$ ,  $b_{1p}$ ,  $b_{1n}$ ,  $\lambda_p$ ,  $K$ , and  $G_n$  are variables that are provided in Appendix A. For a certain probe geometry,  $R_{4PP}$  is a function of  $R_{Si}$ ,  $\rho_c$  and  $R_{TL}$ .

Figure 2.3 shows a comparison of the  $R_{4PP}$  calculated by 3D simulations conducted by Silvaco ATLAS, and by using Eq. (2.2.4). Note that to calculate  $R_{4PP}$  from 3D simulations, Eq. (2.2.3) is multiplied by a correction factor of 4.532 [46]. Overall, there is a slight error in the 2D analytical model associated with the electrically-long contact assumption, as well as neglecting the 3D nature of the problem. Yet, the relative error is less than 5 % compared to the 3D simulation results for  $200 < R_{Si} + R_{TL} < 1000$ , which is applicable for approximately all the experimentally produced cases in this thesis.

One of the main advantages of having an expression relating  $\rho_c$  with  $R_{4PP}$  is that it can be utilized in a self-consistent measurement procedure.  $R_{4PP}$  is a function of three unknowns:  $R_{Si}$ ,  $\rho_c$  and  $R_{TL}$ , which can be expressed as

$$R_{4PP} = f(R_{Si}, R_{TL}, \rho_c). \quad (2.2.5)$$

Measuring  $R_{Si}$  among these unknowns is simple since it just requires the bare wafer and no additional fabrication process. This knowledge reduces the unknowns to two:  $\rho_c$  and  $R_{TL}$ . However, unlike the extraction of  $R_{Si}$ , extraction of  $R_{TL}$  using a separate



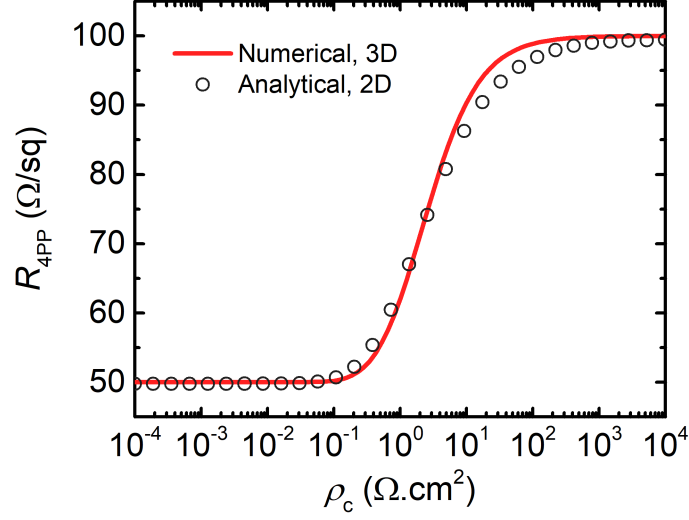


Figure 2.3: Comparison of three-dimensional numerical simulations, two-dimensional analytical model in Eq. (2.2.4) for measured sheet resistance versus contact resistivity for  $R_{Si} = R_{TL} = 100 \text{ } \Omega/\text{sq}$ .

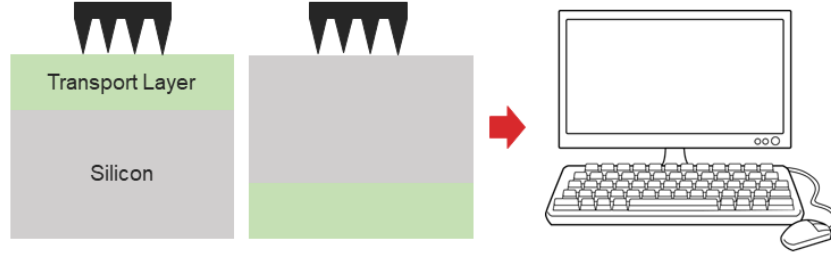


Figure 2.4: Schematic of a double-side four-point probe measurement procedure followed by the calculation of  $\rho_c$  by numerical iteration using a personal computer.

substrate is both time and material consuming, and results in a certain degree of error related with the difference that may occur due to the difference between the the sheet resistance of this layer deposited on a separate substrate and the transport layer that is actually deposited on the low resistivity wafer that is used for the evaluation of  $\rho_c$ . With the knowledge of Eq. (2.2.4), on the other hand, one can perform two measurements on a single sample to extract both  $\rho_c$  and  $R_{TL}$ : one measurement from the transport layer coated side of a single-side transport layer coated silicon wafer, the other from the silicon side of the same wafer. This results in two equations for the

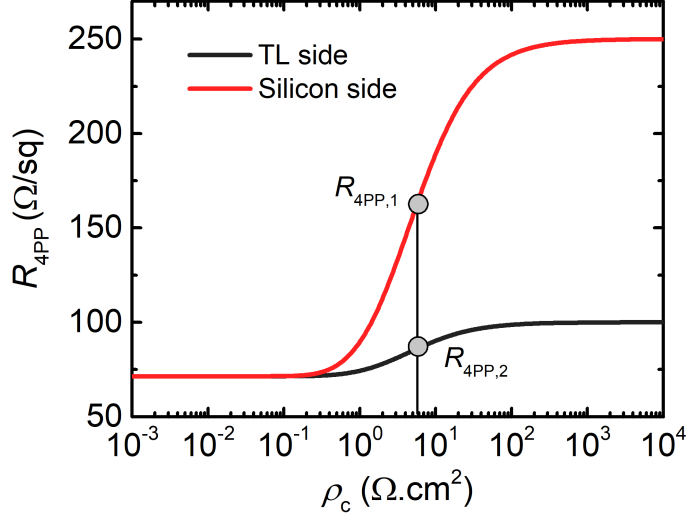


Figure 2.5: Sheet resistance measured by four-point probe measurements performed from two different sides of a sample coated with a transport layer at only one side.

two unknowns,  $\rho_c$  and  $R_{TL}$ , with a unique solution:

$$R_{4PP,1} = f(R_{Si}, R_{TL}, \rho_c), \quad (2.2.6)$$

$$R_{4PP,2} = f(R_{TL}, R_{Si}, \rho_c), \quad (2.2.7)$$

where  $R_{4PP,1}$  and  $R_{4PP,2}$  are the results of the 4PP measurements performed from the bare silicon side and transport layer coated side of the wafer, respectively. Supplying these two sets of equations to a numerical solver on a personal computer, one can obtain a solution within a seconds. This methodology was utilized throughout the thesis for the rapid evaluation of  $\rho_c$ .

## CHAPTER 3

### EXPERIMENTS

From wafer cleaning to the completion of film deposition procedure, there are several steps that can affect the reproducibility and the electrical performance of the fabricated layers. Optimization of each of these steps holds a certain value in achieving high performance layers. In this chapter, details on each of these steps is provided to the best of author's knowledge.

#### 3.1 Silicon wafer preparation

For the  $\rho_c$  and  $J_{0c}$  analyses conducted throughout this thesis, double-side polished silicon wafers were utilized. After extracting the 4" wafers from their cases, they were cleaved by a diamond scribe into quarters of 4" wafers on a clean room grade wiper, or cut down to  $2 \times 2 \text{ cm}^2$  pieces using an IR-wavelength laser. Ultimately, whereas the larger, quarter-4" wafers were mainly used for the evaluation of  $J_{0c}$ , smaller samples were used for the  $\rho_c$  analyses. Following the cleaving step, code names were scribed on the samples using the IR laser. The processes up to this point were performed outside the clean room, yet still in a laboratory with protective wear to minimize wafer contamination. Samples were then vertically placed in sample holders designed to minimize the direct contact of the wafers and the holder, and these holders were then transferred in protective boxes to the clean room for the upcoming chemical processes.

Prior to the chemical oxide growth, the wafers were first rinsed under deionized water (DIW), followed by an HF-dip (5 vol.%), both in allocated polypropylene (PP) beakers, and went through an RCA-2 cleaning at 75 °C for 10 min in PTFE beakers.

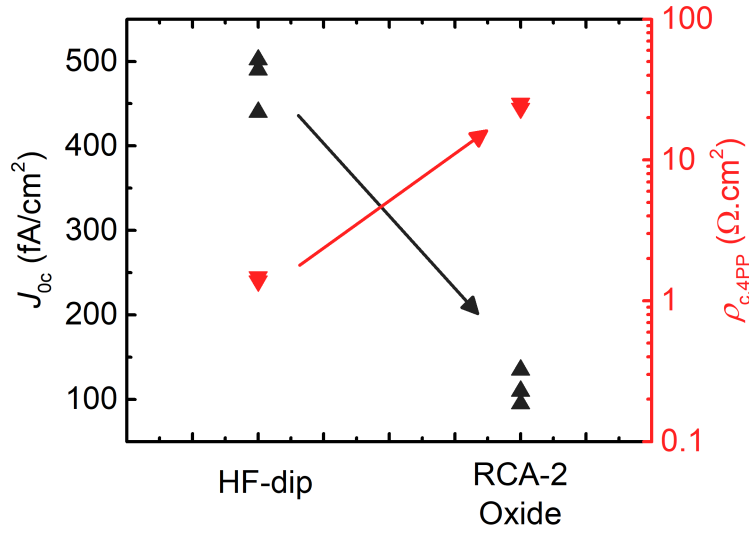


Figure 3.1: Contact saturation current density and contact resistivity for silicon surfaces that have recieved an HF-dip prior to the depositions and a chemical oxide grown by RCA-2 cleaning procedure.

The wafers then recieved an HF-dip to remove the chemical oxide and grow another chemical oxide, or they stayed in this bare form, which is denoted here as 'HF-dipped'.

The final state of the wafer surface is extremely important, and a non-optimal interface between the transport layer and silicon can very easily kill the device performance. Whereas an interfacial silicon oxide layer can improve surface passivation, it also blocks charge transport between the silicon and transport layer. If there are highly doped layers at both ends of this oxide layer, the high carrier tunneling probability can still provide sufficiently well transport through the oxide up to a certain thickness. However, lack of such high doping density, or the presence of additional tunnel blocking layers near the interface can be detrimental for tunneling.

Figure 3.1 demonstrates the trade off between passivation and contact resistivity for PEDOT:PSS layers deposited on p-type silicon. An RCA-2 oxide provides passivation yielding a  $J_{0c}$  around and below 100 fA/cm<sup>2</sup>, yet at the cost of  $\rho_c$  well above 10  $\Omega \text{cm}^2$ , which is detrimental for device operation. Throughout the course of this thesis, it was not possible to obtain reasonably low  $\rho_c$  values for samples having chemical

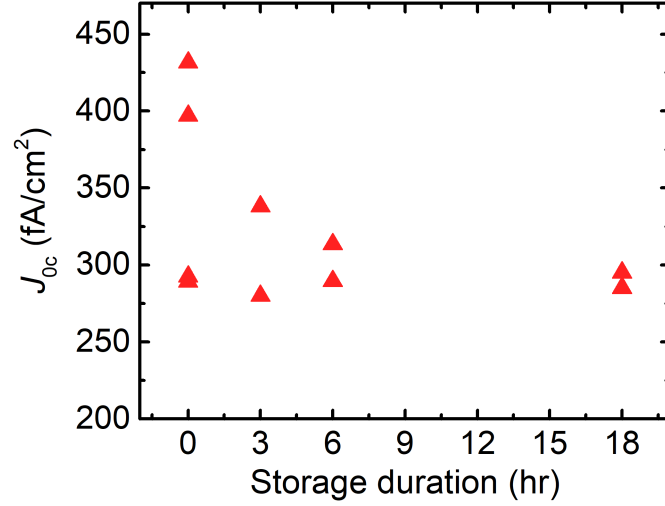


Figure 3.2: Contact saturation current density versus storage duration under ambient air for HF-dipped samples. The PEDOT:PSS dispersion had 0.1 wt.% FS, 5 wt.% DMSO, and the samples were annealed at 110 °C following the depositions.

oxides, regardless of the composition of the deposited PEDOT:PSS layer. Without an oxide, on the other hand, the surface passivation is relatively poor, but  $\rho_c$  is much lower and is suitable for further optimization and high-performance device operation. Consequently, HF-dipped silicon wafers were utilized throughout this thesis, unless specified otherwise.

An HF-dipped surface is hydrophobic with dangling bonds at the surface, which makes it highly susceptible to contamination from surroundings. Furthermore, a native oxide layer, possibly also incorporating other elements present in ambient air, still forms very slowly at the surface under the oxygen containing ambient. Considering that the PEDOT:PSS depositions in this work were not performed at a clean-room ambient, but in an uncontrolled laboratory environment open to any outside influence, it is crucial to analyze the effect of storage conditions prior to PEDOT:PSS deposition. This is, in fact, also an industrially important aspect since solar cell production lines typically are not in high quality clean rooms.

To analyze the effect of storage duration under non-clean room ambient, test samples were fabricated at different storage durations following the HF-dip in the clean room. The shortest duration between the HF dip and PEDOT:PSS deposition was around 10

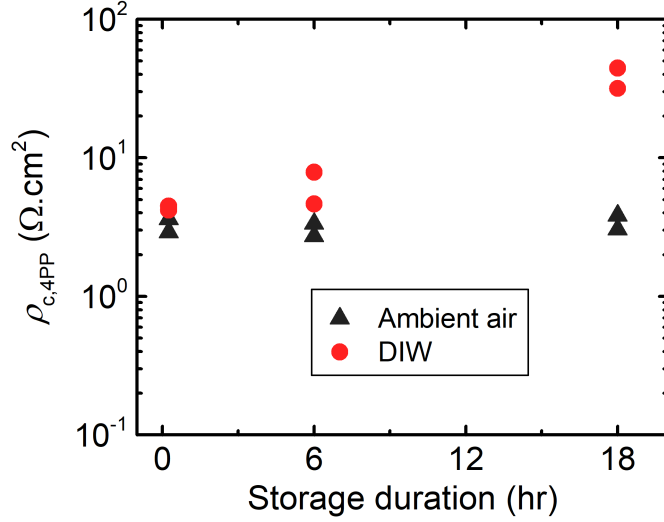


Figure 3.3: Contact saturation current density versus storage duration under ambient air, and in deionized water (DIW) for HF-dipped samples. The PEDOT:PSS dispersion had 0.1 wt.% FS, 5 wt.% DMSO, and the samples were annealed at 110 °C following the depositions.

min due to physical limitations related to the transportation of the samples from clean room to the deposition site. The longest duration was 18 hr, representing approximately the upper limit for the length of a work day. Besides storage under ambient air, storage in DIW in a PP beaker, also in a non-clean room ambient, was tested. The top of the beaker was covered by a clean room grade wiper to minimize accumulation of airborne particles at the water surface that may eventually stick to the wafers when being removed from DIW. The DIW storage experiment was only conducted to observe the changes in  $\rho_c$ .

Figures 3.2 and 3.3 shows the  $J_{0c}$  and  $\rho_c$  results of these experiments. With increasing storage duration, scattering in  $J_{0c}$  lessens and its value converges to a lower limit. Furthermore,  $\rho_c$  stays near constant regardless of storage duration up to 18 hr under ambient air. When stored in DIW, on the other hand,  $\rho_c$  increases considerably with storage duration, which becomes very distinctive at 18 hr. When stored in DIW, one can see with bare eye that the silicon surface becomes gradually hydrophilic, indicating a faster silicon oxide growth rate as compared to storage in ambient air. At 18 hr, a very large portion of the surface becomes hydrophilic. The increase in  $\rho_c$  is

likely associated to this relatively fast oxide growth in DIW.

Based on the results shown in Figs. 3.2 and 3.3, the samples were stored in ambient air following the HF-dip. The storage duration for passivation analysis samples was kept approximately greater than 6 hr, and that of contact resistivity analysis samples were typically greater than 1 hr, to be on the safe side based on the high scattering observed in  $J_{0c}$  data for a storage duration of 10 min.

### **3.2 Preparation and modification of PEDOT:PSS dispersions**

Achieving reproducible coatings, both in terms of morphology and electrical performance is a preliminary condition for controlled experiments. In this section, first the test results regarding the effect of dispersion preparation steps on electrical performance is presented. These dispersion preparation steps were followed to perform experiments on chemical modification of PEDOT:PSS dispersions and their effect on electrical performance, whose results are also presented in this section.

The PEDOT:PSS dispersions have many different commercially available grades, targeting various applications. The dispersions differ from each another in terms of parameters such as the PEDOT-to-PSS ratio, solid content, viscosity, achievable conductivity, and the dispersant [31]. Some of these characteristics result in significant differences in the electrical performance. For example, a smaller PEDOT-to-PSS ratio corresponds to a smaller work-function of the fabricated layers, which yields an increased conductivity in return [47, 48]. Furthermore, unless the commercial dispersion is targeted specifically for the desired application, it needs to be chemically modified by the end-user to improve processability, coating quality, stability, and optical and electrical performance. The improvement in one of these aspects usually also has an additional effect on others, which may or may not be desirable. Therefore, identification of the performance changes in different aspects is critical in the optimization of the dispersion.

In this thesis, Hereaus PH1000 dispersions were utilized, which has a PEDOT-to-PSS ratio of 1 to 6, and one of the highest rated conductivities ( $>1000$  S/cm) among the commercial products. The rated work function of a fabricated layer is between 4.8-

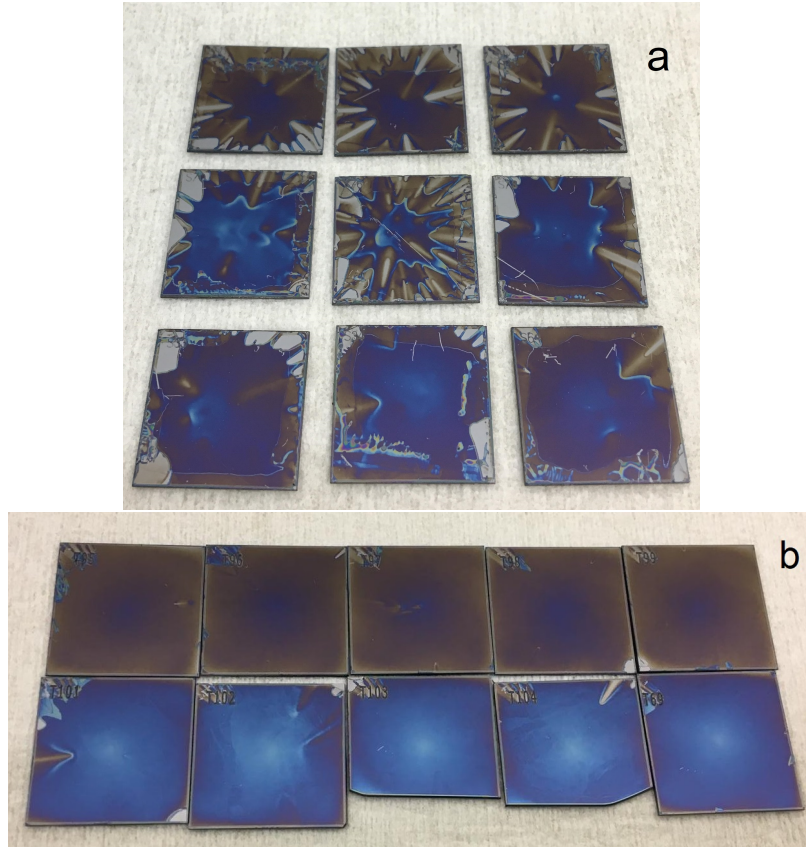


Figure 3.4: Photographs of PEDOT:PSS layers coated from an (a) unoptimized and an (b) optimized dispersion preparation recipe.

5 eV. Note that the choice of PH1000 was based on the fact that it had a low PSS content, which was thought as an advantage for an efficient carrier transport between silicon and PEDOT. However, a quantitative analysis between different PEDOT:PSS grades were not conducted. Considering that PH1000 is not designed specifically for enabling high performance (p)Si/PEDOT:PSS interfaces, the performance results presented here can be regarded as highly open to further improvement with a specifically tailored PEDOT:PSS dispersion.

The PH1000 dispersions have a supplier specified average particle size of 30 nm, with a solid content in water of 1.0-1.3 wt.%, and a viscosity of 10-60 mPa.s [49]. Yet, it is possible that there are agglomerates larger than several hundred nanometres in the dispersion [50]. To eliminate such particles, the dispersions were filtered via hydrophilic polyethylene sulfonate (PES) syringe filters with a pore diameter of 0.2 or 0.45  $\mu\text{m}$ . PES filters were chosen to avoid excessive resistance to dispersion



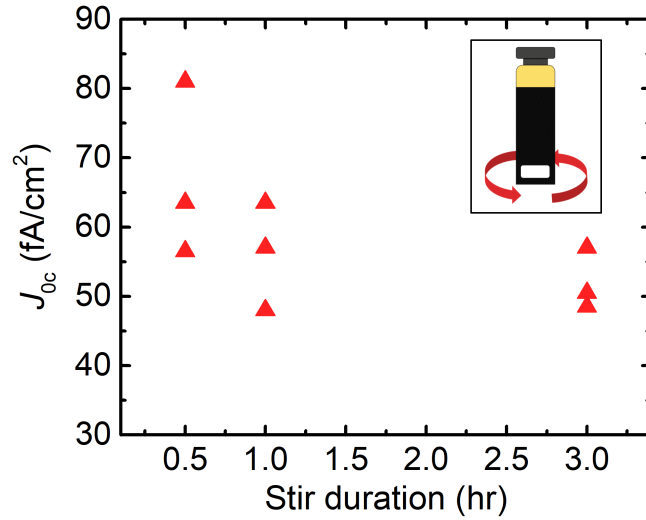


Figure 3.5: Effect of stir duration of PEDOT:PSS dispersions on the surface passivation of silicon wafers that had an RCA-2 oxide chemically grown at 75 °C for 1 min. PEDOT:PSS dispersion had 0.5 wt.% FS and 5 wt.% DMSO.

flow through the filter, which can be encountered with hydrophobic filters made of materials such as PVDF and PTFE.

For the experiments on dispersion preparation, PEDOT:PSS was mixed with a non-ionic fluorosurfactant (FS3100) and dimethyl sulfoxide in 4 mL amber colored vials with a diameter of 14.75 mm and height of 45 mm. First, FS was dropped in the vial, followed by DMSO and PEDOT:PSS. After each chemical addition, the vial was weighted on a scale with a sensitivity of 0.1 mg. Following the addition of all the required chemicals, they were rigorously shaken for 30 sec. Then, a PTFE coated magnetic stirrer, with a diameter of 6 mm and a length of 10 mm, was dropped in the vial and left to stir for a certain duration.

Since the FS containing dispersions are prone to foaming, the shaking and stirring processes can influence the coating quality resulting from these chemicals considerably. An example of the outcome of such shaky motion is shown in Fig. 3.4(a), as opposed to the outcome of a stable stirring process shown in Fig. 3.4(b).

Besides the morphological differences visible to the bare human eye, the electrical performance can be affected by the stirring conditions as well. Fig. 3.5 shows the dif-

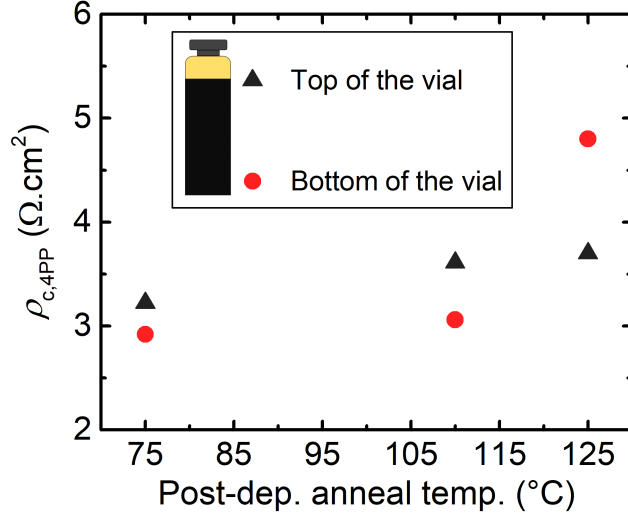


Figure 3.6: Effect of dispersion extraction location from the vial on the contact resistivity.

ference in  $J_{0c}$  of wafers passivated at different stir durations, where the wafers have RCA-2 grown chemical oxides at the surface. With increasing stir duration, the scattering in  $J_{0c}$  becomes smaller, accompanied by a slight decrease in the average  $J_{0c}$ . Moreover, since the experiments were typically performed using approximately the complete volume of the dispersion in a vial, the spatial homogeneity within the vial was important for the interpretation of experimental results as well. Fig. 3.6 shows the results of an experiment conducted in terms of  $\rho_c$ , combined with an experiment analyzing the effect of post-deposition annealing temperature of the samples on an hot-plate, whose details are to be discussed separately in an upcoming section. The dispersions in this experiment were stirred for 3 hr prior to the depositions, and the depositions were completed within less than an hour. The results does not indicate a strong and consistent dependence of the electrical performance on the leftover dispersion volume. For example, whereas  $\rho_c$  is slightly smaller for samples produced from dispersions extracted from the bottom of the vial and annealed at 75 and 110 °C, it is larger for a post-deposition annealing performed at 125 °C. Regardless of this difference in trends, the difference in  $\rho_c$  does not seem to be at an alarming level that would shadow the outcome of a controlled experiment.

Based on the results of provided in Figs. 3.5 and 3.6, the dispersion stir duration was

kept at a minimum of 2 hr in the upcoming experiments. Furthermore, to minimize the differences related to the spatial non-homogeneity within a vial, the coatings were performed in a random order in terms of control parameters of the experiment. As a last remark, note that more experiments conducted with an extended experimental set can still reveal the trends regarding dispersion preparation in more detail and clarity, which were only studied here in a limited manner.

### **3.3 Chemical additives**

#### **3.3.1 The surfactant**

The contact angle between the aqueous PEDOT:PSS dispersion and a hydrophobic silicon surface is too large to provide a reasonably well coating. Therefore, a surfactant needs to be incorporated into the dispersion to provide sufficient wettability of the silicon surface. In the following subsections the electrical performance associated by the usage of two surfactants, namely a non-ionic fluorosurfactant (FS) and isopropanol (IPA), are presented.

##### **3.3.1.1 Fluorosurfactant**

Even a very low amount of non-ionic FS (< 0.1 wt.%) can provide significant improvement in terms of surface wettability of silicon. Regarding the morphological modification induced in PEDOT:PSS layers due to FS addition, they are claimed to promote phase segregation [51, 52], and the conformational change of PEDOT chains from benzoid to quinoid [53]. As for their effect on the electrical performance, it was shown that the addition of a 0.01 wt.% FS reduced the sheet resistance to one third of films that did not have any FS, and further increase in FS concentration up to 1 wt.% resulted in slightly larger sheet resistance, possibly because FS is an insulator and blocks the current pathways between PEDOT grains when used in large concentrations [51]. Furthermore, when FS was added in PEDOT:PSS layers which were used as HTLs on n-type silicon solar cells having an RCA oxide, it was shown to improve the  $V_{oc}$  and FF at a concentration of 0.1 wt.%, compared to a coating that does

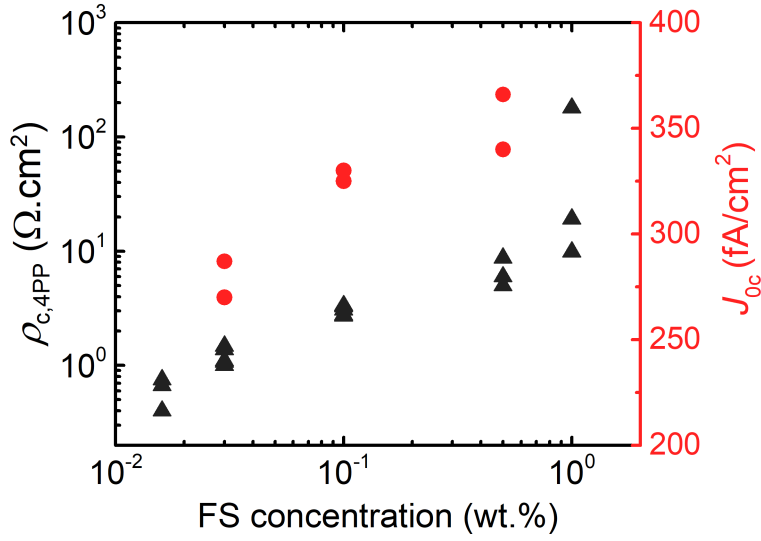


Figure 3.7: Effect of FS concentration on the contact resistivity and contact saturation resistivity of (p)Si/PEDOT:PSS samples.

not have any FS [54]. However, this improvement in FF was actually not associated to a reduction contact and series resistance, but rather with an increase in the shunt resistance of the devices. The advantage was lost at higher FS concentrations as both the FF and  $V_{oc}$  of the fabricated devices decreased.

Here, PEDOT:PSS layers having FS concentrations between 0.016 and 1 wt.% were analyzed in terms of  $\rho_c$  and  $J_{oc}$  as shown in Fig. 3.7. By decreasing the FS concentration from 0.5 to 0.03 wt.%, more than 50 fA/cm $^2$  decrease can be achieved in  $J_{oc}$ . In terms of  $\rho_c$ , on the other hand, the effect is even more significant. By decreasing the FS concentration from 1 to 0.016 wt.% decreases by more than an order of magnitude. Contact resistivities below 1  $\Omega \text{cm}^2$  are observed only for a FS concentration below 0.03 wt.%. These results were verified in several different experimental runs, and by both 4PP technique and the metallized test samples, whose results are in agreement with each other as shown in Fig. 3.8.

These results indicate that lowering the FS concentration even further would result in superior performance, which indeed needs to be investigated further. Yet, for such low FS concentrations, several problems arise: (i) the wettability provided by the FS starts to weaken, (ii) maintaining chemical homogeneity within the vial becomes

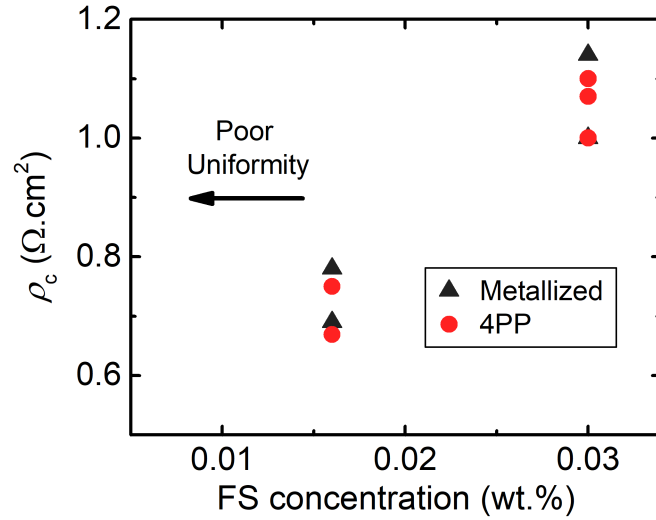


Figure 3.8: Effect of FS concentration on the resistivity of (p)Si/PEDOT:PSS interface, extracted by both 4PP measurements and I-V measurements of double-side full-area metallized samples.

harder, (iii) larger dispersion volumes are required since the added FS mass reaches down to the limit of sensitivity of the weighing scale utilized in this work (i.e. 0.1 mg), resulting in material waste in experiments. As a result, investigation of a more easily processable surfactant becomes attractive, which is discussed in the following section.

### 3.3.1.2 Isopropanol

Isopropanol (IPA) is known to improve the surface wettability, as well as inducing changes in the drying conditions and band structure of the PEDOT:PSS layers, when added in the dispersion [55, 56, 57].

Its effect on the electrical performance is perhaps not as well studied as other commonly used additives (eg. FS, secondary dopants), but there are still rather interesting works on the subject. For example, in one study the work-function of the PEDOT:PSS layer was reduced to 4.3 eV for a (PEDOT:PSS):IPA ratio of 1:1, which was actually used as an electron transport layer (ETL) in an organic solar cell [56]. In another study, on the other hand, the work function was approximately the same (5.2 eV) for

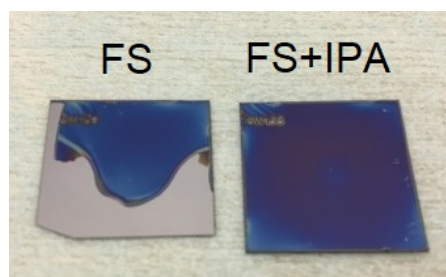


Figure 3.9: Effect of isopropanol (IPA) addition (5 vol.%) on the coating quality of PEDOT:PSS layers having low FS content (0.001 wt.%).

the unmodified dispersion and the dispersion having (PEDOT:PSS):IPA ratio of 3:1.

As mentioned in the previous section, the very low FS content can result in degraded coating quality for PEDOT:PSS layers. The first use of IPA in PEDOT:PSS dispersions in this study was, in fact, to use it as a complementary surfactant for dispersions having very low FS concentrations. Fig. 3.9 shows an example of the difference in coating quality that can be achieved by mixing the two surfactants, where the wafer coated with a 0.008 wt.% FS containing dispersion is on the left, and the wafer coated after adding an additional 5 vol.% IPA to the same dispersion is on the right. The coating performance improved significantly by the addition of IPA. Notably, the effect of this addition on the electrical performance is also negligible, as shown in Fig. 3.10.

The observation that there is no apparent negative effect of IPA addition, at least for concentrations shown in Fig. 3.10, brings the question whether IPA can be used as the sole surfactant in the dispersion, omitting the FS altogether. In terms of the coating quality, that can be achieved utilizing solely IPA, Fig. 3.11 shows the photographs of samples coated by dispersions having various IPA concentrations up to 40 vol.%. For concentrations approximately below 20 vol.% the contact angle between silicon and PEDOT:PSS is still relatively large, and a large volume of dispersion is required to be dispensed on the sample to be coated properly, and still then, the coating performance is rather unreliable. On the other hand, concentrations approximately above 25 vol.% provide reliable wettability. Yet, higher concentrations also appear to increase the formation probability of agglomerations observed in these coatings. The severity of agglomeration formation, however, was not very consistent, and dispersions having high 40 vol. % IPA could also yield agglomeration-free coatings. The exact condi-

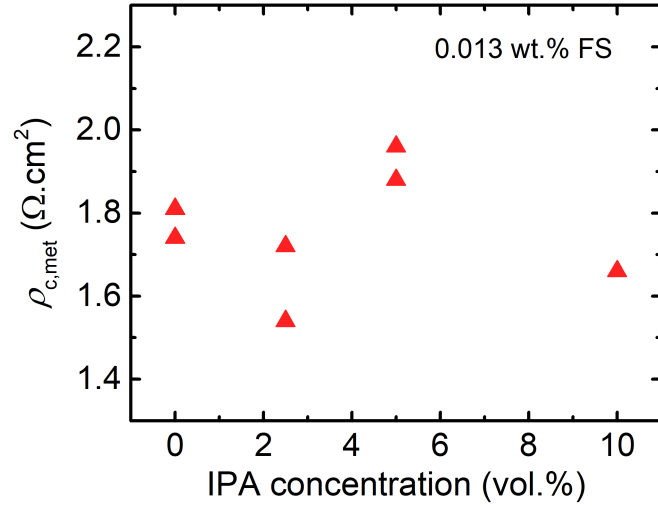


Figure 3.10: Effect of isopropanol (IPA) addition with various volume percentages on the contact resistivity of samples fabricated from a dispersion with additional 0.013 wt.% FS.

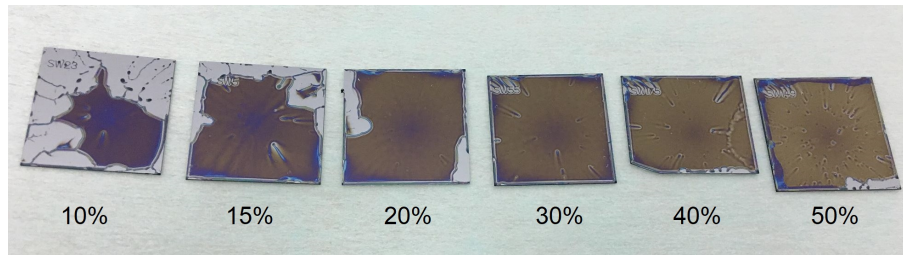


Figure 3.11: Photographs of PEDOT:PSS coatings having IPA as the only surfactant, with various volume percentages.

tions yielding these agglomerations, and whether they have any considerable negative effect on the electrical performance are still under investigation.

The results of experiments where  $\rho_c$  and  $J_{0c}$  were assed for varying IPA concentrations are also shown in Fig. 3.12 and 3.13, respectively. Using IPA as the sole surfactant,  $\rho_c$  values around  $0.5 \Omega \text{cm}^2$  could be achieved in several different sets of experiments, with the lowest one at  $0.28 \Omega \text{cm}^2$ . To author's knowledge, this is also the lowest  $\rho_c$  value reported for a (p)Si/PEDOT:PSS interface. The  $J_{0c}$  is also near  $225 \text{ fA/cm}^2$ , lower than  $250\text{-}300 \text{ fA/cm}^2$  that can be achieved using an FS containing dispersion with the same DMSO concentration. A considerable change in neither  $\rho_c$

nor  $J_{0c}$  was observed by increasing the IPA concentration up to 40 vol. %.

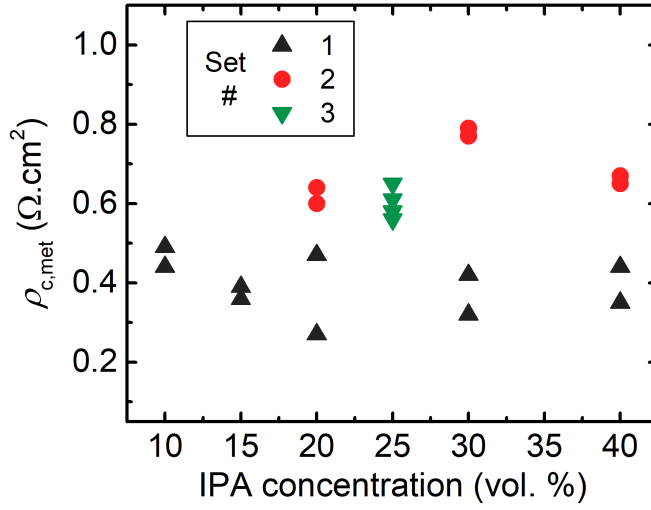


Figure 3.12: Contact resistivity versus IPA concentration for three different experimental sets. Samples were annealed at 110 °C for 15 min following the depositions.

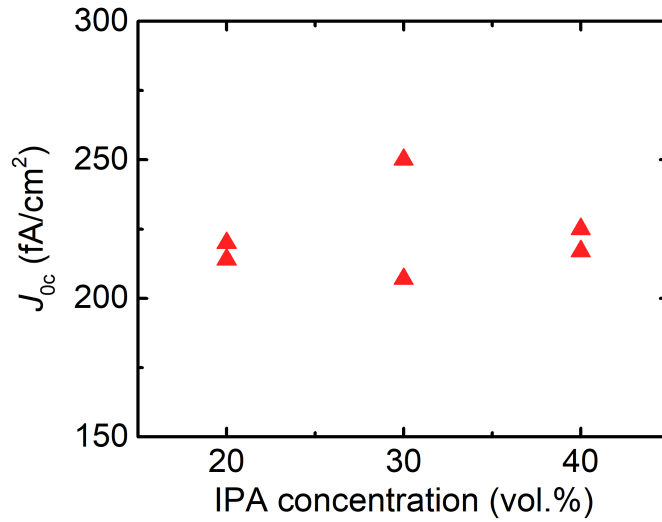


Figure 3.13: Contact saturation current density versus IPA concentration. Samples were annealed at 110 °C for 15 min following the depositions.

Overall, IPA appears as a relatively high performance surfactant with  $\rho_c$  and  $J_{0c}$  values superior to those achieved using FS. Furthermore, the independency of electrical performance from IPA concentration simplifies the dispersion preparation procedure



significantly and reduces the amount of PEDOT:PSS that needs to be utilized in experiments, ultimately making IPA a more attractive choice as a surfactant than FS. Yet, it should be noted that FS is still open to further improvement, and it should not be discarded before its electrical performance limits at even lower concentrations are fully discovered.

### 3.3.2 The secondary dopant

Organic solvents such as dimethyl sulfoxide (DMSO), ethylene glycol (EG), sorbitol and glycerol are known to provide considerable changes in electrical properties [33, 58, 59, 60]. Commonly known as 'secondary dopants', these additives are claimed to induce phase segregation of PEDOT and PSS, a change from benzoid to quinoid structure, and elongated PEDOT chains that yield a high film conductivity [61, 62]. Whereas a benzoid structure tends toward a coil conformation, a quinoid structure favors a linear (or an expanded-coil) conformation which enhances the conductivity along its direction [62]. However, there are also other views regarding the source of conduction increase, which suggest that the change is associated with the thinning of PSS layers, and the growth of PEDOT grains, without a considerable conformational change [63]. Suggesting this hypothesis, correlations between increasing particle size distribution with secondary dopant content [59], and the conductivity grade of dispersions [64] were also observed in other studies. Either way, the solvents that induce these effects commonly have high solubility in water, a high boiling temperature, and a high dielectric constant [61]. Furthermore, once treated with a secondary dopant, the PEDOT:PSS films become insoluble in water as opposed to pristine films which can easily be dissolved. This is attributed to an increased inter-chain interaction within the film treated with a secondary dopant [62].

Dimethyl sulfoxide (DMSO) is the secondary dopant that was mainly studied throughout this thesis. This choice was mainly due to its widespread use among the scientific community and the fact that the rated conductivity value of PH1000 by the supplier is based on films incorporating specifically this compound. Figures 3.14 and 3.15 show the  $\rho_c$  and  $J_{0c}$  values for various DMSO concentrations. A low DMSO concentration results in a high  $\rho_c$ , possibly due to the thick PSS shells between the PEDOT grains

and between the PEDOT grains and silicon surface. The lowest and consistent  $\rho_c$  values are observed for a concentration of 10 wt.%. The 5 wt.% dispersions can also yield similar  $\rho_c$  values with 10 wt.% dispersions, but with lesser reproducibility in general. A DMSO concentration larger than 10 wt.% yields larger  $\rho_c$ , which may be associated with the high concentration of leftover DMSO in the films due to its high boiling temperature. In terms of surface passivation,  $J_{0c}$  peaks at a DMSO concentration of 10 wt.%, and decreases towards lower DMSO concentrations. This may be expected since PSS rich PEDOT:PSS is reported to have a larger work function, and PSS itself provides good passivation on a silicon surface [65]. It is, however, interesting that  $J_{0c}$  is smaller for a DMSO concentration of 20 wt.% as compared to the passivation provided with a DMSO concentration of 10 wt.%. This trend is approximately inverse of the trend seen for  $\rho_c$ . It is possible that DMSO itself may be passivating the surface, which becomes more effective at high DMSO concentrations. Yet, beyond this interpretation, the exact reasoning of the trend is still unclear.

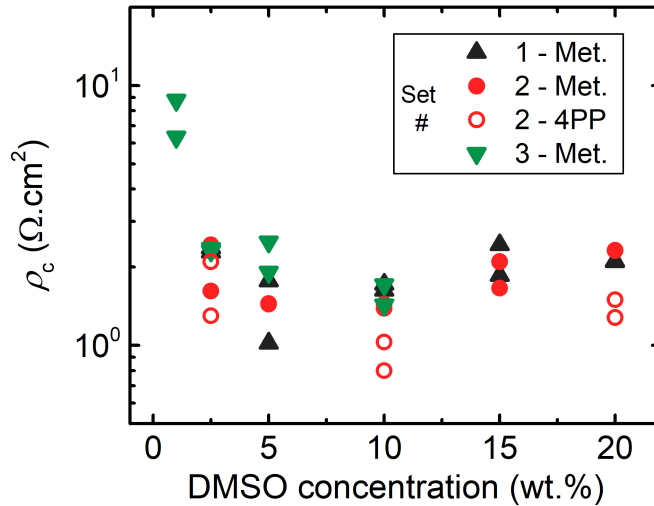


Figure 3.14: Contact resistivity versus DMSO concentration for different experimental sets and with two different experimental methods. The dispersion has 0.03 wt. % FS as the surfactant.

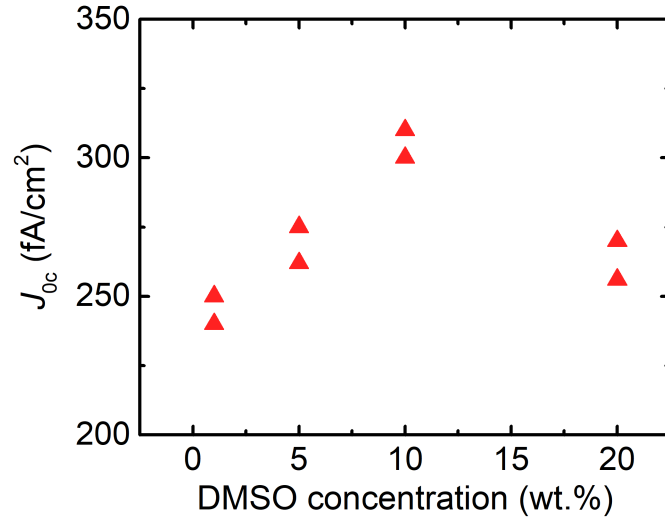


Figure 3.15: Contact saturation current density versus DMSO concentration. Samples were annealed at 110 °C for 15 min following the depositions.

Overall, a trade-off between  $J_{0c}$  and  $\rho_c$  exists, with 2.5 to 20 wt.% DMSO concentrations all being viable choices for a well-functioning HTL. The ultimate choice of concentration can be made based on the particular loss mechanism that is desired to be minimized in the solar cell.

### 3.4 Post-deposition annealing

Following the spin coating process at room temperature, the coated PEDOT:PSS layers typically remain wet to a certain extent. The extent of dryness depends on the concentration of the incorporated chemical additives. For example, films having higher DMSO concentrations, which has a high boiling temperature, typically dry over relatively longer durations. The drying process may be fastened by annealing the sample, exposing it to a vacuum environment, or by spinning for longer durations.

In this work, the samples were annealed on a hot plate with varying temperatures following the spin coating process with a duration of 1 min. This procedure is denoted as "post-deposition annealing" throughout the rest of the work. To avoid full area contact of the wafers with the possibly contaminated hot plate surface, support pieces cut

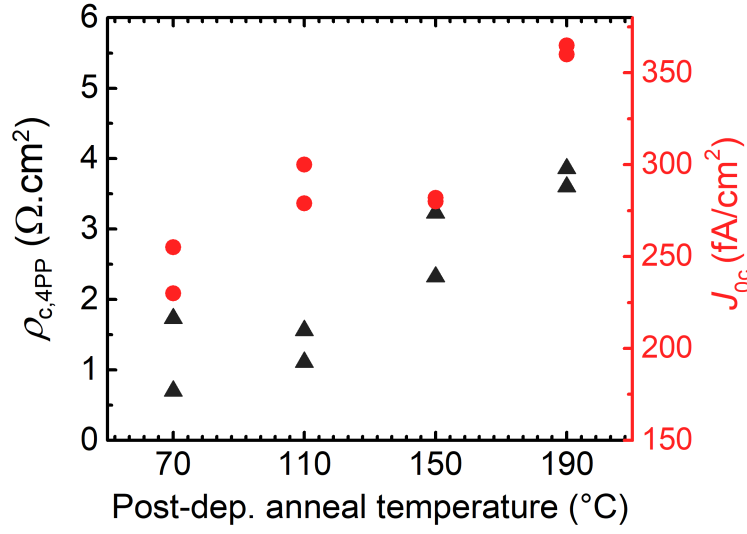


Figure 3.16: Contact resistivity and contact saturation current density versus post deposition annealing temperature. Black and red symbols are for  $\rho_c$  and  $J_{0c}$ , respectively. The PEDOT:PSS dispersions had 10 wt.% DMSO and 0.03 wt. % FS.

from 200  $\mu\text{m}$ -thick multi-crystalline wafers were used to place the processed wafers on the hot plate. After coating the first side of the wafers, they were placed on these support pieces, without directly contacting the hot plate. If the sample is to be coated only on one side (e.g. for 4PP measurements) this annealing step lasts for 15 min. If the sample is to be coated on both sides, the wafer is removed from the hot plate to cool down on a separate stage made of corning glass pieces after drying the first side for 1 min. The sample is also in contact with this stage only from certain locations at the outer edges. After the wafer cools down, the other side of the wafer is coated. The double-side coated wafer is placed on the hot plate again to be annealed for 15 min. At the 8<sup>th</sup> minute of this annealing step, the wafer is flipped to induce similar annealing conditions for the two sides of the wafer.

Figure 3.16 shows the effect of post-deposition annealing on  $\rho_c$  and  $J_{0c}$  for varying annealing temperatures. Both  $J_{0c}$  and  $\rho_c$  decreases considerably with the annealing temperature. The performance remains viable to a degree when annealing at 110 °C, yet it still yields a worse performance than annealing at 70 °C. Based on this trend even lower temperature drying procedures (< 70 °C) seem worthy of investi-

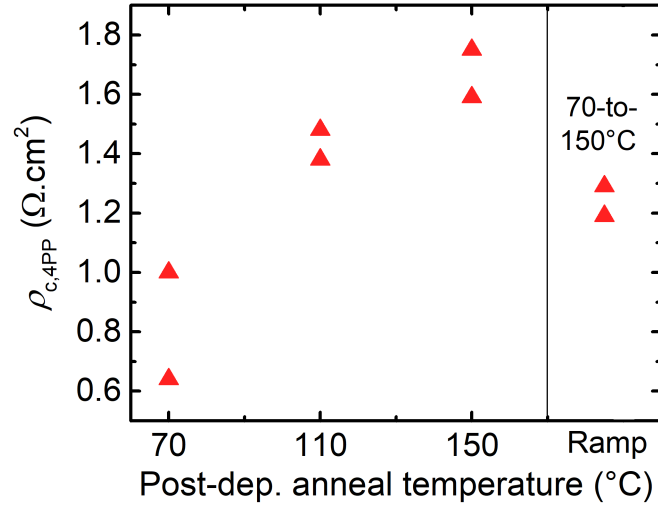


Figure 3.17: Contact resistivity versus post-deposition annealing temperature for the standard annealing conditions where the samples are annealed for 15 min at the specified temperature (left of the black vertical line), and with a ramped annealing profile where the temperature is gradually increased from 70 °C to 150 °C in 2 min steps, followed by an annealing at 150 °C for 8 min.

gation. However, considering that solar cells operate at temperatures up to 70 °C in real-world applications, the temperature of the test samples is to eventually reach this temperature. Then the question is whether the initial drying temperature is the primary determinant in the final performance, and whether annealing initially at lower temperatures, and then ramping up the temperature yields better results than annealing only at a high temperature. Figure 3.17 shows  $\rho_c$  for three different constant annealing temperatures, and when the annealing temperature is increased gradually from the lowest of these temperatures to the highest (i.e. from 70 to 150 °C). The temperature was raised in 20 °C steps at 2 min intervals, reached 150 °C at the 8<sup>th</sup> minute of the annealing procedure and remained there for another 8 min. This procedure yields a lower  $\rho_c$  than annealing directly at 150 °C, yet still higher than that achieved by annealing at 70 °C. This indicates that the initial temperature of the drying sample is a parameter to be considered, but not the only one effective on the end result.

Based on these results, the post-deposition annealing was performed at either 70 or

110 °C while studying the effect of other parameters. Although 70 °C yielded consistently better results, the samples went through annealing in a thermal evaporator located in a water-free glove box, and it had to be ensured that the PEDOT:PSS layers were dry. Therefore, 110 °C was more commonly utilized throughout the thesis, to minimize the interference with the work conducted in the glove box by colleagues.

### 3.5 Metallization

When a metal is coated on an organic layer, typically, there occurs a chemical reaction at the interface resulting in a change in the electronic structure of both the metal and the organic layer. For aluminum, these reactions are reported to be considerable when it is deposited directly on organic layers. Therefore, less reactive metals, such as silver and gold are analyzed here. For a clean Au surface the work function under ultra-high vacuum (UHV) environment is reported to be near 5.4 eV, yet when deposited on an organic layer this reduces by approximately 0.5-1.2 eV. Similarly, for Ag with a UHV work function of around 4.3 eV, the reduction is on the order of 0.5 eV [66]. These work function values are considerably lower than that of PEDOT:PSS which is around 5 eV. However, since both the metal and PEDOT:PSS have very high carrier concentrations, the work function of the metal is likely irrelevant in the final performance. To verify this assumption, silver and gold contacts were used for the metallization of test samples having similar PEDOT:PSS layers, as shown in Table. 3.1. A considerable difference in  $\rho_c$ , resulting from the difference in the metal type, is not observed. Accordingly, Ag was the choice of metal in the experiments reported in this thesis to minimize the cost of research.

An important aspect regarding the performance of metallized samples is the annealing following the metallization, denoted here as the 'post-metallization annealing'. Figure 3.18 and 3.19 show the dependence of  $\rho_c$  on the temperature and duration of this annealing procedure. When the metallized samples are not annealed, the contact resistivity is very high, near  $10 \Omega\text{cm}^2$ . Annealing at 75 and 100 °C decrease  $\rho_c$  considerably, with highest consistency in terms of obtaining low  $\rho_c$  values is observed for 100 °C. For an annealing temperature at and above 125 °C,  $\rho_c$  is significantly larger. These trends are in partially in agreement with the trends observed regarding

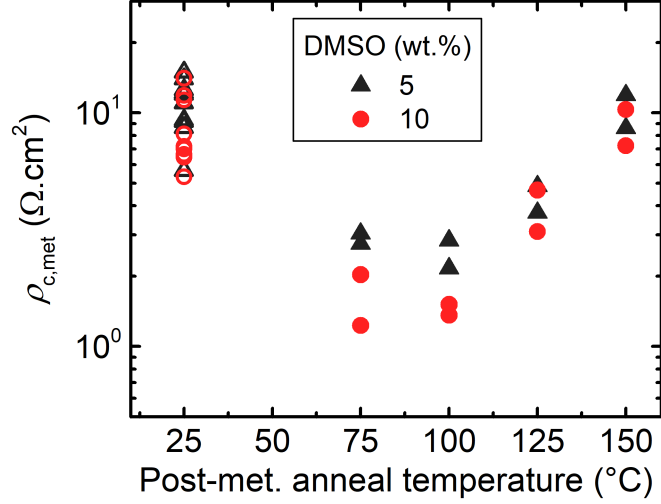


Figure 3.18: Contact resistivity versus post-metallization annealing temperature for PEDOT:PSS films having two different DMSO concentrations.

the post-metallization annealing temperature, where beyond around 110 °C, the electrical properties degraded considerably. However, considering that these layers have already been annealed prior to metallization, the reasoning behind the necessity for an additional annealing step requires further analysis.

To identify the cause of the high  $\rho_c$  observed with non-annealed samples, TLM measurements were performed on PEDOT:PSS layers deposited on n-type wafers. The reasoning behind the choice of an n-type wafer was to limit the current flow within PEDOT:PSS, and analyze solely the interface between the metal and PEDOT:PSS, eliminating the influence of (p)Si/PEDOT:PSS interface on the results. Figure 3.20

Table 3.1: Contact resistivities obtained using silver and gold contacts for the metallized samples.

Material	DMSO (wt.%)	$\rho_{c,met}$ ( $\Omega cm^2$ )	
Ag	5	2.16	2.84
	10	1.51	1.36
Au	5	2.47	2.43
	10	1.61	1.76

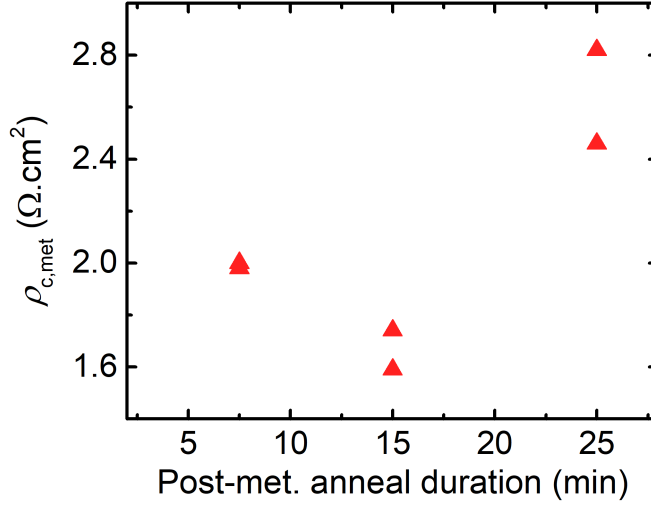


Figure 3.19: Contact resistivity versus post-metallization annealing duration at a temperature of 100 °C.

shows the results of this experiment. With  $\rho_c$  values below 10 mΩcm<sup>2</sup>, the PEDOT:PSS/Ag interface has a negligible  $\rho_c$  as compared to that of (p)Si/PEDOT:PSS. This result indicates that the change induced in the (p)Si/PEDOT:PSS/Ag stack during the post-metallization annealing procedure is mainly associated with the (p)Si interface. Yet, the details of such change is currently not clear, and requires a deeper analysis that is not provided in this thesis.

As a last remark regarding the metallization procedure, it should be noted that thermal evaporation of a metal is currently the bottleneck of experiments in terms of duration, with the completion of metallization and following measurements lasting over 5 hours for a double side coating. To speed up the experimental procedure further, a metallization technique alternative to thermal evaporation should be utilized. For instance, screen printing can be a viable alternative for this purpose. As a non-vacuum based process that is applicable at room temperature, it is fast and reproducible, and is also a industrially relevant technique. It was also demonstrated in a work that Ag pastes can actually be made viable to be used with PEDOT:PSS [41]. For future experiments, this aspect should likely be studied in detail.



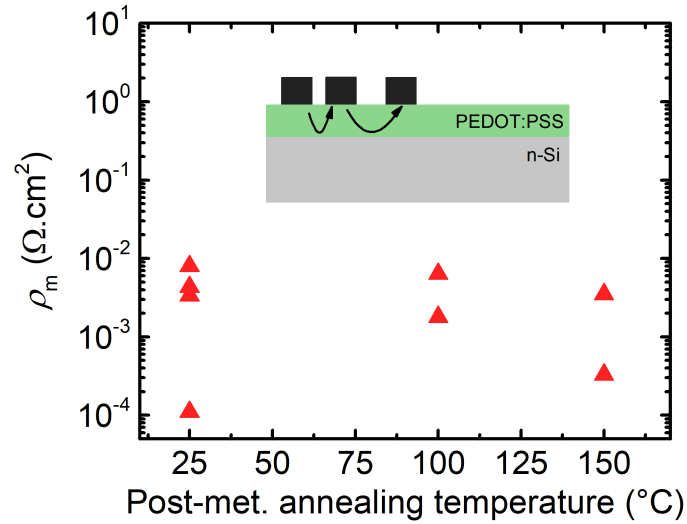


Figure 3.20: Contact resistivity of the PEDOT:PSS/Ag interface versus post-metallization annealing temperature. The  $\rho_c$  values were extracted from TLM measurements performed on PEDOT:PSS layers deposited on n-type silicon wafers, where the current flow is confined in the p-type PEDOT:PSS, as indicated by the schematic in the figure.

### 3.6 Stability

Stability is a crucial aspect for solar cells, specifically considering that the performance should be maintained over extended periods (e.g. > 20 year) unlike those used in consumer electronics of today. The necessity of stability under ambient air, on the other hand, is not actually a must since the cause of degradation can be prevented by encapsulation techniques that can block the ambient air and its constituents, while also blocking part of the sunlight spectrum that can speed up degradation processes (e.g. ultraviolet light). Regardless, it's important to identify if there is a performance degradation over time and the possible causes of it. Preventive measures can then be taken for a stable cell operation. In this thesis, these encapsulation techniques were not studied. However, the performance changes occurring under ambient conditions were tracked on a basic level and for a limited duration, without any control on the environment. The documentation was mostly done on passivation evaluation samples, with only limited data on contact resistivity evaluation samples. Due to the lack of a covering metal layer, passivation samples are exposed to the ambient conditions

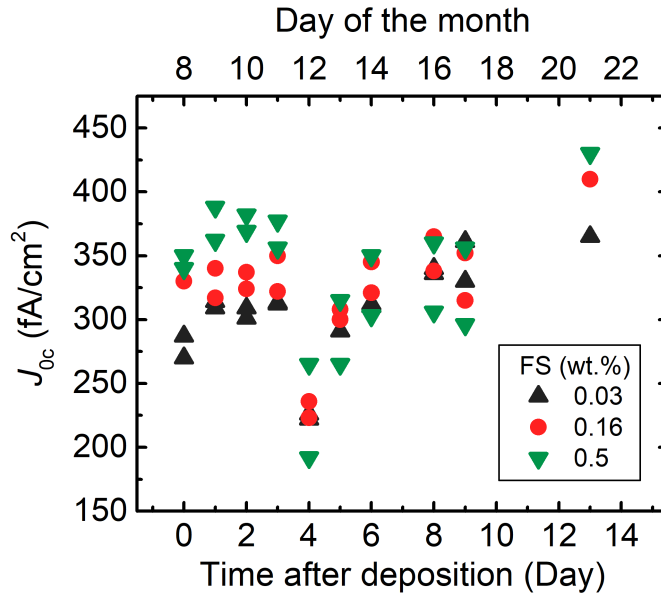


Figure 3.21: Change in contact saturation current density following the deposition of PEDOT:PSS layers having different concentrations of FS. The samples were stored under ambient air.

significantly, and were expected to be more sensitive to environmental conditions as compared to metallized samples, yet this assumption also requires validation. For all the data provided in this section, the time after deposition and the day of the month when the measurement was performed is reported to identify if performance changes occur at the same time for samples with different PEDOT:PSS layers. Unfortunately, a humidity and temperature logger was not installed in the laboratory to see if the data relates to the electrical performance changes.

Figure 3.21 shows the change in  $J_{0c}$  following the depositions for three different FS concentrations, where the samples were stored under non-clean room laboratory environment. There is an increase in  $J_{0c}$  of around 50 fA/cm<sup>2</sup> within the first day of depositions, which remains approximately stable for 3 days. At the fourth day,  $J_{0c}$  drops significantly for all samples, and slowly restores to its previous value within 2 days. Yet, the distinction between different FS concentration containing samples is no longer present. It was shown in another work that upon exposure to ambient air, films incorporating FS can show an initial decrease in terms of sheet resistance within the first tens of hours following the depositions [53]. This decrease in sheet resistance

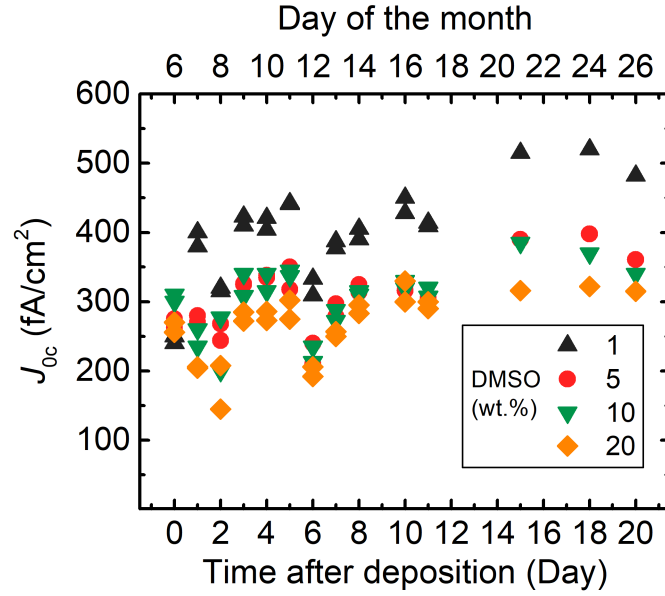


Figure 3.22: Change in contact saturation current density following the deposition of PEDOT:PSS layers having 0.1 wt.% FS and different concentrations of DMSO. The samples were stored under ambient air.

was shown to be followed by an eventual increase, which occurred much rapidly for thinner films that had lower FS content. These findings can perhaps also be related to the disappearance of the trend with respect to FS content on a given day in Fig. 3.21.

Figure 3.22 shows the change in  $J_{0c}$  for samples having PEDOT:PSS layers with different DMSO concentration. Even after 1 day following the depositions, a distinct trend appears where the  $J_{0c}$  of samples having larger DMSO concentrations decrease within the two days following the depositions, whereas the  $J_{0c}$  of the sample having 1 wt.% DMSO increases. Changes in  $J_{0c}$  occur over time, yet samples having larger DMSO concentrations continue to have  $J_{0c}$  values lower than those having lower DMSO concentrations. Assuming that DMSO reduces the amount of PSS in the films [63], the trend in Fig. 3.22 is, in fact, in agreement with the literature on the subject, where the degradation in PEDOT:PSS films is mostly associated with the PSS, rather than PEDOT [67, 68].

Figure 3.23 shows the stability of the deposited films which were annealed at different post-deposition annealing temperatures. The trend with respect to the annealing temperature at a given day does not change over time; a lower annealing temperature

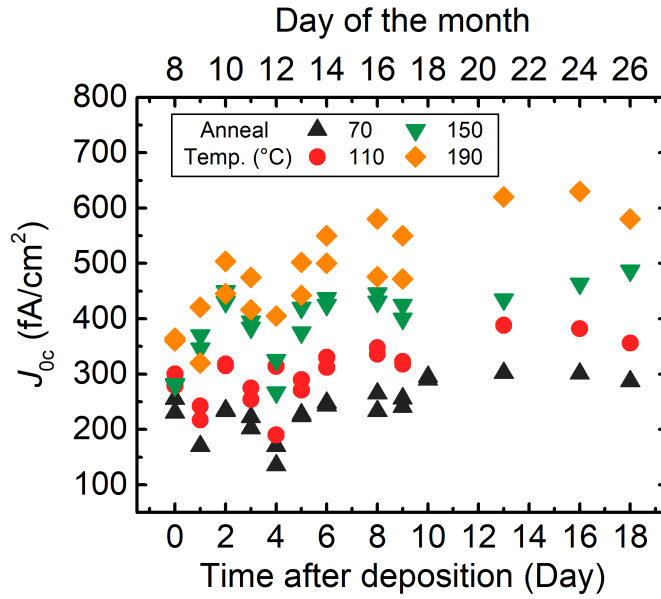


Figure 3.23: Change in contact saturation current density following the deposition of PEDOT:PSS layers having 0.1 wt.% FS and 5 wt.% DMSO, annealed at different temperatures. The samples were stored under ambient air.

yields a lower  $J_{0c}$ . The change in  $J_{0c}$  with respect to time is also more significant for samples annealed at higher temperatures. Overall, a low temperature post-deposition annealing appears optimal. The trend with respect to annealing temperature at a given day, is also similar when IPA is used as a surfactant instead of FS. Yet, it is interesting that samples annealed at 150 °C remain stable up to 5 days, whereas those annealed at lower temperatures show considerable changes over the same duration, specifically within the first day. The insensitivity of samples annealed at 150 °C is interrupted at the seventh day, along with samples that had recieved a lower temperature annealing, where  $J_{0c}$  increases by up to 100 fA/cm<sup>2</sup>. The cause of this change is not clear, yet it shows that the sensitivity to ambient conditions is present with samples annealed at 150 °C as well.

Overall, the response of  $J_{0c}$  to the environmental conditions also becomes apparent when the data is analyzed in terms of the day of the month measurements were taken. On some particular days there appears significant changes over approximately all PEDOT:PSS configurations, indicating the presence of a major performance determinant besides the constituents of the PEDOT:PSS layers. For example, on 12th of August,

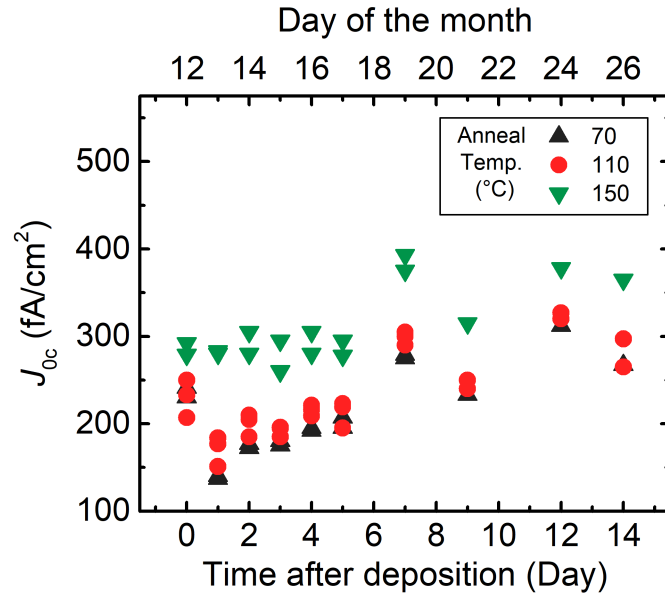


Figure 3.24: Change in contact saturation current density following the deposition of PEDOT:PSS layers with 30 vol.% IPA and 10 wt.% DMSO, annealed at different temperatures. The samples were stored under ambient air.

all  $J_{0c}$  values degrade significantly (by 50-150 fA/cm<sup>2</sup>) compared to the previous day. Identifying the cause of this change, and combining the finding with an effective encapsulation technique can perhaps enable consistently high performance cells.

The degradation observed in an actual solar cell structure, where the sample is fully-metallized at the rear side and partially metallized on the front, is also of interest. Since the focus of the thesis was on test structures rather than a complete solar cell fabrication, the data on this particular structure is rather limited, but still available. For this end, ion implantation of phosphorus was performed on one side of double-side polished CZ p-Si wafers to form an emitter. These wafers then went through a dopant activation step at a tube furnace at 950 °C. They were cleaned by an RCA-2 procedure, both before and after this annealing step. PEDOT:PSS was then coated on the p-type side of the wafer, and recieved thermal evaporation of Ag on both sides of the wafers. A metal grid, designed to minimize resistive losses, was formed on the front side and the rear side was fully-metallized. Overall, these cells were fabricated specifically to analyze the resistive losses and FF on a device level. Due to the polished and un-passivated front surface, the low quality bulk, and large metallization

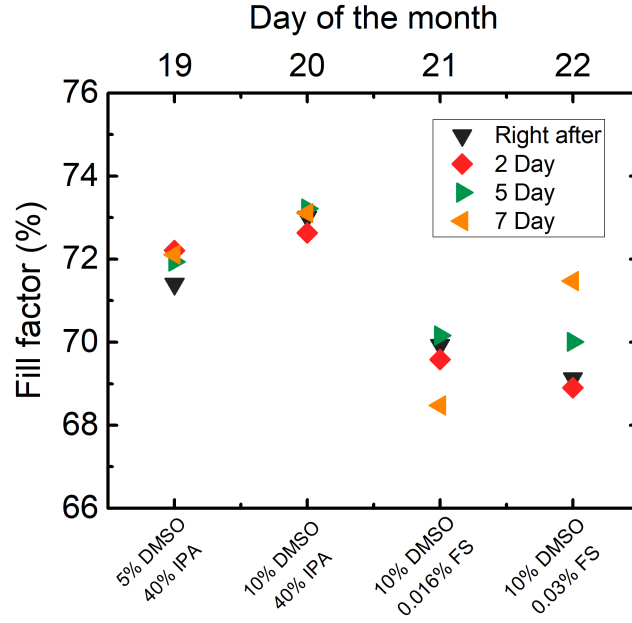


Figure 3.25: Fill factors (FFs) of solar cells fabricated using various PEDOT:PSS dispersions, and the change in FFs within a week of storage under ambient air.

fraction at the front side, their  $V_{oc}$ ,  $J_{sc}$  and consequently the efficiency were very limited. Furthermore, a previously unobserved abnormality was observed related to the PEDOT:PSS quality for this batch, where the contact resistivity was higher than what was typically observed and reported in previous sections of the thesis. Regardless, Fig. 3.25 shows the FFs of these cells. Note that considering the lack of a calibration sample for the efficiency measurements at the time of experiments, the system related deviations in FF is actually unknown. Yet, assuming that the deviations from measurement to measurement does not shadow fluctuations in FF resulting from actual device degradation, the FF remains relatively stable over time up to 7 days, especially for samples containing IPA instead of FS. These results are promising considering that the degradation appears limited in an actual solar cell structure even without encapsulation. Yet, many more experiments covering an extended duration are required for a definitive conclusion.

## CHAPTER 4

### CONCLUSIONS AND FUTURE WORK

A characterization scheme to analyze the performance of PEDOT:PSS layers on (p)Si surfaces in terms of  $\rho_c$  and  $J_{0c}$  was implemented. The scheme was used to analyze the effects of different fabrication procedures including the preparation of the silicon surface and PEDOT:PSS dispersions, effects of chemical additives in the dispersions, and additional post-deposition processes. The presence of a chemical oxide was found detrimental to charge carrier transport, and an HF-dip prior to the depositions, and subsequent storage under ambient air, were shown to yield significantly lower  $\rho_c$ , yet at the cost of larger  $J_{0c}$ . Furthermore, a commonly used additive in previous works in literature, non-ionic fluorosurfactant, was identified as one of the major limiting factors in achieving low  $\rho_c$ . An alternative surfactant, IPA, was shown to yield consistently low  $\rho_c$  and  $J_{0c}$ , with much less sensitivity to the incorporated IPA content as compared to the sensitivity to the FS content. Incorporation of DMSO with approximately larger than 5 wt.% was shown to yield optimal results in terms of  $\rho_c$ , with a nonlinear dependence on the concentration for  $J_{0c}$ . Shortly after the coating, however, passivation provided by the low DMSO content PEDOT:PSS layers degraded considerably while high DMSO content layers yielded consistently lower results. Post-deposition annealing was shown to also have significant effect on the electrical performance, as well as the stability of the structures, with lower temperatures yielding better performance overall. A ramped annealing profile resulted in slight improvement in terms of  $\rho_c$  compared to the all-high temperature annealing conditions, which may be beneficial in identifying the root cause of the dependency on annealing conditions. A similar dependency on annealing temperature was also observed with metallized samples; an annealing temperature above room temperature and below approximately 100 °C appears as a must for achieving low  $\rho_c$  with metallized samples.

Higher temperatures degrade the electrical performance, at least in terms of  $\rho_c$ , significantly. Using TLM measurements, the cause of the post-metallization annealing dependency was identified to be possibly related to the changes in (p)Si/PEDOT:PSS interface rather than PEDOT:PSS/Ag interface. Overall, the best performing contacts fabricated in this thesis incorporate IPA as a surfactant, and yield  $\rho_c < 0.28 \Omega\text{cm}^2$ , which is the lowest reported to date for a PEDOT:PSS contact on silicon, and  $J_{0c}$  near  $200 \text{ fA/cm}^2$ . These PEDOT:PSS contacts are the second best reported in literature in terms of maximum achievable cell efficiency with 24.42 %, following the contacts of Zielke et al. [21].

Overall, this thesis analyzes the trends with experimental conditions in terms of the secondary level performance parameters,  $J_{0c}$  and  $\rho_c$ , which were not provided in literature previously. The characterization procedure is aimed to be a rapid preliminary test standard in similar work, and aid in the early identification of trends, without fabricating complete solar cells or perhaps even metallized structures. However, the lower level cause (molecular interactions, morphological changes) of why  $J_{0c}$  and  $\rho_c$  responds to different experimental procedures as they do, is not covered in this work in general. There are works in literature that can aid in the interpretation of these results. Yet, the works are mostly focused on PEDOT:PSS/air or vacuum interface, and detailed analysis on (p)Si/PEDOT:PSS interface is rather limited. By combining the electrical characterization procedures with other characterization methods and combining the findings with a deeper interface chemistry knowledge, a higher understanding and an electrical performance are expected to be achieved.



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## APPENDIX A

### ANALYTICAL MODEL FOR THE FOUR-POINT PROBE STRUCTURE

Outside the contacts the following set of equations hold

$$dI_1(z) = -dI_2(z) \quad (\text{A.0.1})$$

$$dI_2(z) = (V_1(z) - V_2(z)) \frac{w}{\rho_c} dz \quad (\text{A.0.2})$$

$$dV_1(z) = -I_1(z) \frac{R_{sh1}}{w} dz \quad (\text{A.0.3})$$

$$dV_2(z) = -I_2(z) \frac{R_{sh2}}{w} dz \quad (\text{A.0.4})$$

where  $I_0 = I_1 + I_2$ . Rearranging these equations one obtain

$$\frac{d^2 I_1(z)}{dz^2} - \frac{R_{sh3} + R_{sh2}}{\rho_c} I_1(z) = -\frac{R_{sh2}}{\rho_c} I_0 \quad (\text{A.0.5})$$

$$I_1(z) = -(d_1 e^{z\xi_{c2}} + d_2 e^{-z\xi_{c2}}) + \frac{R_{sh2}}{R_{sh1} + R_{sh2}} I_0 \quad (\text{A.0.6})$$

$$I_2(z) = (d_1 e^{z\xi_{c2}} + d_2 e^{-z\xi_{c2}}) + \frac{R_{sh1}}{R_{sh1} + R_{sh2}} I_0 \quad (\text{A.0.7})$$

where

$$\xi_{c2} = \sqrt{\frac{R_{sh1} + R_{sh2}}{\rho_c}} \quad (\text{A.0.8})$$

Inserting  $I_1(z)$  and  $I_2(z)$  into A.0.3 and A.0.4, respectively

$$V_1(z) = -\frac{R_{sh1}}{w\xi_{c2}} (-d_1 e^{z\xi_{c2}} + d_2 e^{-z\xi_{c2}}) - \frac{R_{sh1}R_{sh2}}{R_{sh1} + R_{sh2}} I_0 \frac{z}{w} + d_3 \quad (\text{A.0.9})$$

$$V_2(z) = -\frac{R_{sh2}}{w\xi_{c2}} (d_1 e^{z\xi_{c2}} - d_2 e^{-z\xi_{c2}}) - \frac{R_{sh1}R_{sh2}}{R_{sh1} + R_{sh2}} I_0 \frac{z}{w} + d_4 \quad (\text{A.0.10})$$

Under the contacts the following set of equations hold

$$dI_1(z) = (V_0 - V_1(z))\frac{w}{\rho_c}dz - dI_2(z) \quad (\text{A.0.11})$$

$$dI_2(z) = (V_1(z) - V_2(z))\frac{w}{\rho_c}dz \quad (\text{A.0.12})$$

$$dV_1(z) = -I_1(z)\frac{R_{sh1}}{w}dz \quad (\text{A.0.13})$$

$$dV_2(z) = -I_2(z)\frac{R_{sh2}}{w}dz \quad (\text{A.0.14})$$

Rearranging the equations one obtain the following equations

$$\frac{d^2 I_1(z)}{dz^2} = \frac{R_{sh1} I_1(z)}{\rho_m} + \frac{R_{sh1} I_1(z)}{\rho_c} - \frac{R_{sh2} I_2(z)}{\rho_c} \quad (\text{A.0.15})$$

$$\frac{d^2 I_2(z)}{dz^2} = -\frac{R_{sh1} I_1(z)}{\rho_c} + \frac{R_{sh2} I_2(z)}{\rho_c} \quad (\text{A.0.16})$$

which can be expressed in matrix form as

$$\begin{bmatrix} \frac{d^2 I_1(z)}{dz^2} \\ \frac{d^2 I_2(z)}{dz^2} \end{bmatrix} = \begin{bmatrix} \frac{R_{sh1}}{\rho_m} + \frac{R_{sh1}}{\rho_c} & -\frac{R_{sh2}}{\rho_c} \\ -\frac{R_{sh1}}{\rho_c} & \frac{R_{sh2}}{\rho_c} \end{bmatrix} \begin{bmatrix} I_1(z) \\ I_2(z) \end{bmatrix} \quad (\text{A.0.17})$$

Let

$$\begin{bmatrix} I_1(z) \\ I_2(z) \end{bmatrix} = \begin{bmatrix} c_1 \\ c_2 \end{bmatrix} e^{kz} \quad (\text{A.0.18})$$

and

$$k^2 \begin{bmatrix} I_1(z) \\ I_2(z) \end{bmatrix} = \begin{bmatrix} \frac{R_{sh1}}{\rho_m} + \frac{R_{sh1}}{\rho_c} & -\frac{R_{sh2}}{\rho_c} \\ -\frac{R_{sh1}}{\rho_c} & \frac{R_{sh2}}{\rho_c} \end{bmatrix} \begin{bmatrix} I_1(z) \\ I_2(z) \end{bmatrix} \quad (\text{A.0.19})$$

Then;

$$\begin{bmatrix} \frac{R_{sh1}}{\rho_m} + \frac{R_{sh1}}{\rho_c} - k^2 & -\frac{R_{sh2}}{\rho_c} \\ -\frac{R_{sh1}}{\rho_c} & \frac{R_{sh2}}{\rho_c} - k^2 \end{bmatrix} \begin{bmatrix} I_1(z) \\ I_2(z) \end{bmatrix} = 0 \quad (\text{A.0.20})$$

The solution for k can then be found by equation the determinant to 0

$$\det \begin{vmatrix} \frac{R_{sh1}}{\rho_m} + \frac{R_{sh1}}{\rho_c} - k^2 & -\frac{R_{sh2}}{\rho_c} \\ -\frac{R_{sh1}}{\rho_c} & \frac{R_{sh2}}{\rho_c} - k^2 \end{vmatrix} = 0 \quad (\text{A.0.21})$$

and 4 roots of  $k$  is extracted from this relationship

$$k_{p,n} = \pm \sqrt{\frac{\frac{R_{sh1}}{\rho_m} + \xi_{c1}^2 \pm \sqrt{\left(\frac{R_{sh1}}{\rho_m} + \xi_{c1}^2\right)^2 - \frac{4R_{sh1}R_{sh2}}{\rho_m(R_{sh1} + R_{sh2})}\xi_{c1}^2}}{2}} \quad (\text{A.0.22})$$

where  $n$  and  $p$  subscripts in  $k_p$  and  $k_n$  indicate whether the  $\pm$  sign is negative or positive inside the square rooted expression, and for both  $k_p$  and  $k_n$  the sign of the  $\pm$  outside the square changes as well. Inserting  $k_{p,n}$  into A.0.20, one obtains

$$\lambda_{p,n} = \frac{I_2(z)}{I_1(z)} = -\frac{\xi_{c1}^2 \left( \frac{R_{sh1}}{R_{sh1} + R_{sh2}} \right)}{k_{p,n}^2 - \xi_{c1}^2 \left( \frac{R_{sh2}}{R_{sh1} + R_{sh2}} \right)} \quad (\text{A.0.23})$$

Accordingly,

$$I_1(z) = a_{1p}e^{k_p z} + b_{1p}e^{-k_p z} + a_{1n}e^{k_n z} + b_{1n}e^{-k_n z} \quad (\text{A.0.24})$$

$$I_2(z) = \lambda_p(a_{1p}e^{k_p z} + b_{1p}e^{-k_p z}) + \lambda_n(a_{1n}e^{k_n z} + b_{1n}e^{-k_n z}) \quad (\text{A.0.25})$$

Inserting A.0.24 and A.0.25 into A.0.11 and A.0.12, using the relation  $\rho_m(\lambda_{p,n} + 1)k_p = R_{sh1}/k_{p,n}$  and rearranging then yields

$$V_1(z) = V_0 - \left[ \frac{R_{sh1}}{wk_p}(a_{1p}e^{k_p z} - b_{1p}e^{-k_p z}) + \frac{R_{sh1}}{wk_n}(a_{1n}e^{k_n z} - b_{1n}e^{-k_n z}) \right] \quad (\text{A.0.26})$$

$$V_2(z) = V_0 - \left[ \lambda_p \frac{R_{sh2}}{wk_p}(a_{1p}e^{k_p z} - b_{1p}e^{-k_p z}) + \lambda_n \frac{R_{sh2}}{wk_n}(a_{1n}e^{k_n z} - b_{1n}e^{-k_n z}) \right] \quad (\text{A.0.27})$$

Overall, there are 9 unknowns ( $a_{1n}, a_{1p}, b_{1n}, b_{1p}, d_1, d_2, d_3, d_4, I_0$ ) that need to be determined to calculate  $R_{\text{comb}}$ , and therefore, 9 independent equations are required for the solution as follows

1.  $I_1(-d) = 0$  and  $I_2(-d) = 0$  assuming the contacts are electrically long.
2.  $I_1(0) = I_1(L)$ ,  $V_1(L/2) = V_0/2$ , and  $V_2(L/2) = V_0/2$  due to symmetry. There is no current flow through the interface at  $z = L/2$ , where also the derivatives of  $I_1(z)$  and  $I_2(z)$  with respect to  $z$  are equal to zero.
3.  $I_1(0), I_2(0), V_1(0), V_2(0)$  are continuous at  $z = 0$ , at the boundary of the contacted and non-contacted regions.

To calculate  $V_{4PP}$ , the knowledge of  $d_1, d_2, d_3$  and  $I_0$  is required, which are as follows

$$d_1 = \frac{\frac{R_{sh1}}{wk_n}(a_{1n} - b_{1n}) + \frac{R_{sh1}}{wk_p}(a_{1p} - b_{1p}) + R_{sh1}(a_{1p} + b_{1p} + a_{1n} + b_{1n})\frac{L}{2w} - \frac{V_0}{2}}{\frac{R_{sh1}}{w\xi_{c2}}(e^{L\xi_{c2}/2} - Pe^{-L\xi_{c2}/2} + P - 1) - \frac{(P+1)R_{sh1}L}{2w}} \quad (\text{A.0.28})$$

$$d_2 = Pd_1 \quad (\text{A.0.29})$$

$$d_3 = V_0 - \left( \frac{R_{sh1}}{wk_p}(a_{1p} - b_{1p}) + \frac{R_{sh1}}{wk_n}(a_{1n} - b_{1n}) - \frac{R_{sh1}}{w\xi_{c2}}d_1(P-1) \right) \quad (\text{A.0.30})$$

$$I_0 = V_0 \left[ \frac{L}{w} \left( \frac{R_{sh1}R_{sh2}}{R_{sh1} + R_{sh2}} \right) + \frac{2}{(\lambda_p - K)G_n} \left( \frac{R_{sh1} - KR_{sh2}}{R_{sh1} + R_{sh2}} \right) \right]^{-1} \quad (\text{A.0.31})$$

where

$$P = \frac{1 - e^{L\xi_{c2}}}{e^{-L\xi_{c2}} - 1} \quad (\text{A.0.32})$$

$$K = \frac{(\lambda_p F_p + \lambda_n F_n) \tanh(\xi_{c2}L/2) + 1}{(F_p + F_n) \tanh(\xi_{c2}L/2) - 1} \quad (\text{A.0.33})$$

$$G_{p,n} = \frac{wk_{p,n}}{R_{sh2}} \left( \frac{1}{\lambda_{p,n} - \lambda_{n,p}} \right) \left( 1 - \lambda_{n,p} \frac{R_{sh2}}{R_{sh1}} \right) \tanh(k_{p,n}d) \quad (\text{A.0.34})$$

$$F_{p,n} = \frac{k_{p,n}}{R_{sh2}\xi_{c2}} \left( \frac{1}{\lambda_{p,n} - \lambda_{n,p}} \right) \left( R_{sh2} - \lambda_{n,p}R_{sh2} \right) \tanh(k_{p,n}d) \quad (\text{A.0.35})$$

$$H_{p,n} = \frac{1}{wk_{p,n}} \frac{(\lambda_{p,n}R_{sh2}R_{sh1} + R_{sh1}R_{sh2}) \coth(k_{p,n}d)}{1 + \lambda_{p,n}} \quad (\text{A.0.36})$$

$$a_{1p,n} = \pm \frac{I_0 \left( H_{n,p} + \frac{R_{sh1}R_{sh2}L}{2w} \right) - V_0 \frac{R_{sh1} + R_{sh2}}{2}}{(H_n - H_p)(1 + \lambda_{p,n})(1 - e^{-2k_{p,n}d})} \quad (\text{A.0.37})$$

$$b_{1p,n} = -a_{1p,n}e^{-2k_{p,n}d} \quad (\text{A.0.38})$$