SYSTEM INTEGRATION OF MEMS DEVICES ON FLEXIBLE SUBSTRATE FOR FULLY IMPLANTABLE COCHLEAR IMPLANT APPLICATIONS

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ABSTRACT

SYSTEM INTEGRATION OF MEMS DEVICES ON FLEXIBLE SUBSTRATE FOR FULLY IMPLANTABLE COCHLEAR IMPLANT APPLICATIONS

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This master thesis is a result of multidisciplinary research bringing together concepts in electronics engineering, implant technologies, materials science, microfabrication, and device physics. Advancements in healthcare technology and in-vivo implants, electronic devices implemented on flexible substrates are highly demanded in the near future. In order to create a physically flexible device which consists of rigid sub-systems serving distinct purposes and made up of varying types of materials, we need reliable and durable integration methods for each sub-system. Moreover, the connection of these subsystems on a flexible substrate is a new subject that requires development. Furthermore, developed system has to be implantable and biocompatible. Under these concerns, the aim of this master thesis is to develop physically flexible, implantable and biocompatible system by the application of new methods to integrate rigid components to flexible substrate. Rigid components can be micro electromechanical system (MEMS) based sensors chips and CMOS electronics. Since advancement in semiconductor technology requires multichip integration and trending 3D integration techniques, through silicon via technology is utilized in this thesis to solve multichip MEMS integration challenges. Flexible substrate which houses the overall system is a polymeric and biocompatible material for this study.

The thesis starts by introducing the subject by giving the motivation of the study and the literature review of the field. Next, the methods and the applications of the study will be given in two main fabrication chapters. Development of a wafer level, void free TSV fabrication process flow was developed. TSV structures with 100 µm diameter and 350 µm depth were copper filled with via sealing and bottom-up electroplating process which is a two-step technique. Fabrication of parylene flexible substrate specifically designed to designate MEMS piezoelectric cantilever chips was presented. Four-point Kelvin measurement tests explained that yields 0.8 mΩ average TSV resistance on fabricated TSVs and feasibility study of TSV integration to MEMS piezoelectric resonator devices has been presented in the results and discussion chapter. Then, Finally, the conclusions and the future work are explained

Keywords: Cochlear implants, Microfabrication, Through silicon via, Flexible electronics, MEMS packaging, 3D integration, MEMS resonators

ÖZ

MEMS CİHAZLARININ KOKLEAR İMPLANT UYGULAMALARI İÇİN ESNEK ALT TABAN ÜZERİNE ENTEGRASYONU

Soydan, Alper Kaan
Yüksek Lisans, Mikro ve Nanoteknoloji
Tez Danışmanı: Prof. Dr. Haluk Külah
Ortak Tez Danışmanı: Dr. Dilek Işık Akcakaya

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Bu yüksek lisans tezi, elektronik mühendisliği, implant teknolojileri, mataryel bilimi, mikrofabrikasyon ve cihaz fiziği konseplerini bir araya getiren çoklu discipline sahip bir araştırmanın sonucudur. Sağlık teknolojisi ve vücut içi implant cihazların gelişimi, elektronik cihazların vucüt için uyumlu esnek zemin üzerine entegre edilmesine ihtiyaç duymaktadır. Farklı amaçlara hizmet eden, birbirinden farklı maddelerden yapılmış sabit alt sistemlerden oluşan, fiziksel olarak esnek bir cihaz geliştirmek için güvenilir ve sağlam bağlantılara ihtiyaç vardır. Ayrıca, bu bağlantılar ile alt sistemlerin entegrasyonu, geliştirilmesi gereken yeni bir konudur. Bunlara ek olarak, geliştirilen sistemin vücut içi implant olarak kullanılabilir olması gerekmektedir. Bu tez çalışmasının amacı, yeni metotlar uygulayarak sabit alt sistemlarin esnek zemin üzerine entegrasyonu ile yapılmış, biyouyumlu ve vücut içi implant yapılabilir esnek bir elektronik sistem geliştirmektir. Bu çalışmada sabit alt sistemler PZT sensorler ve CMOS elektroniğinden oluşurken esnek zemin olarak biyouyumlu bir polimerik malzeme kullanılacaktır. Bu çalışmada, bütün bir pul seviyesinde, boşluksuz yapıda TSV üretimi ve geliştirilmesi sürecinin akışı ve MEMS piezoelektrik rezonatör cihazlarına TSV entegrasyonunun fizibilite çalışması sunulmuştur. 100 μm çapa ve 350 μm derinliğe sahip TSV yapıları, iki aşamalı bir teknik olan örtme ve aşağıdan yukarıya elektrokaplama işlemi ile bakırla doldurulmuştur. Dört noktalı Kelvin ölçümü sonucu, üretilen TSV'lerde 0,8 mΩ direnci tekli yapılardan

gözlenmiştir. Ayrıca, TSV'li çip çerçeveleri MEMS akustik sensörüne epoksi ile bağlanmış, TSV'den gelen rezonatör sinyalinde önemli bir sakınca göstermediği gözlenmiştir. Bu yazı, tez konusunun tanıtılması, çalışmanın motivasyonunun belirtilmesi ve alanın literatür incelemesi ile başlayacaktır. Daha sonra, çalışmada uygulanan metotlar ve uygulamalar açıklanacaktır. Son olarak, varılan sonuçlar ve çalışmanın devamı için planlamalardan bahsedilecektir.

Anahtar Kelimeler: Koklear implant, Mikrofabrikasyon, Silisyum boyunca bağlantı, Esnek elektronik, MEMS paketleme, 3B entegrasyon

To My Family

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LIST OF ABBREVIATIONS

ABBREVIATIONS

BHF	Buffered Hydrofluoric Acid
CI	Cochlear Implant
DRIE	Deep Reactive Ion Etching
ECD	Electrochemical Deposition
FEA	Finite Element Analysis
FICI	Fully Implantable Cochlear Implant
IPA	Isopropyl Alcohol
MEMS	Microelectromechanical Systems
PDMS	Polydimethylsiloxane
PEH	Piezoelectric Energy Harvester
PLD	Pulsed Laser Deposited
PZT	Lead Zirconate Titanate
RIE	Reactive Ion Etching
SEM	Scanning Electron Microscope
TSV	Through Silicon Via

CHAPTER 1

INTRODUCTION

In March 2019, report of the World Health Organization (WHO) has revealed that approximately 466 million people around the world has disabling hearing loss which corresponds to more than 5% of the total population. This figure refers to the people who has level of hearing loss greater than 40 dB sound pressure level [1]. Until the hearing loss of average 90 dB SPL level, disabling hearing loss is characterized as mild, moderate and severe, which can be treated with external hearing aids. However, greater hearing loss levels than 90 dB SPL is considered as severe to profound and requires a treatment with cochlear implants (CI) [2]. Cochlear implants are considered to be one of the most successful devices to function as recovery of a sensory deprivation. Cochlear implants are used to bypass the nonfunctional parts of the patient by picking the sound and sending it to the cochlea [3].

Typical cochlear implants has outer modules that compose of microphone, battery, processor and transmitter antenna that is coupled with the internal receiver unit [4]. In Figure 1.1, these outer components are numbered as 1, 2 and 3. Whereas, in this study that is conducted under the Fully-Implantable MEMS-Based Autonomous Cochlear Implant (FLAMENCO) project by the European Union's Horizon 2020 research and innovation programme, we propose a system that has no external components, thus call this system as fully implantable. Also, energy efficient because it uses MEMS technology and it is autonomous it can harvest its energy by itself and adapts signal levels to each patient.

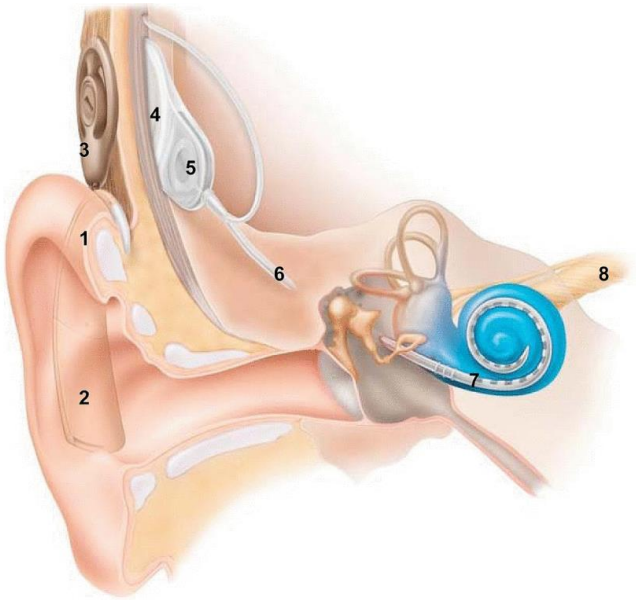

Figure 1.1. Schematic design of a typical cochlear implant (www.cochlear.com).

1.1. Motivation

Over the last decades, MEMS sensor and transducer technology based on piezoelectricity has been focusing on human health and medical applications [5], [6]. In the FLAMENCO[1] Project was proposed thanks to these developments. In the project, multi-chip system for fully implantable cochlear implants (FICI), consisting of energy harvester and transducer chips are produced [7],[8]. In Figure 1.2, the transducer stack that houses the acoustic sensor comprises of an energy harvester on top for the long lasting usage of the system without additional medical operations by charging the re-chargeable battery. Energy harvesting is realized by the simultaneous working of the piezoelectric cantilever and the interface electronics that regulates the charging of the battery. A multi-frequency piezoelectric (PZT) cantilever set establishes the acoustic sensing of the implant. Acoustic vibration is converted to the electrical signals that are converted to a desired waveform by the conditioning

[1] A Fully- Implantable MEMS-Based Autonomous Cochlear Implant, ERC Consolidator Grant, Project ID: 682756

electronics prior to transmission to the electrodes implanted inside the cochlea. In order to utilize the acoustic vibrations picked by the ear channel, both energy harvester and the acoustic transducers are planned to be implanted on eardrum or ossicles. Hence, 3D integration MEMS transducer package is required. These are the main components of the fully implantable cochlear implant proposed and developed. However, there are great concerns regarding the integration of the system.

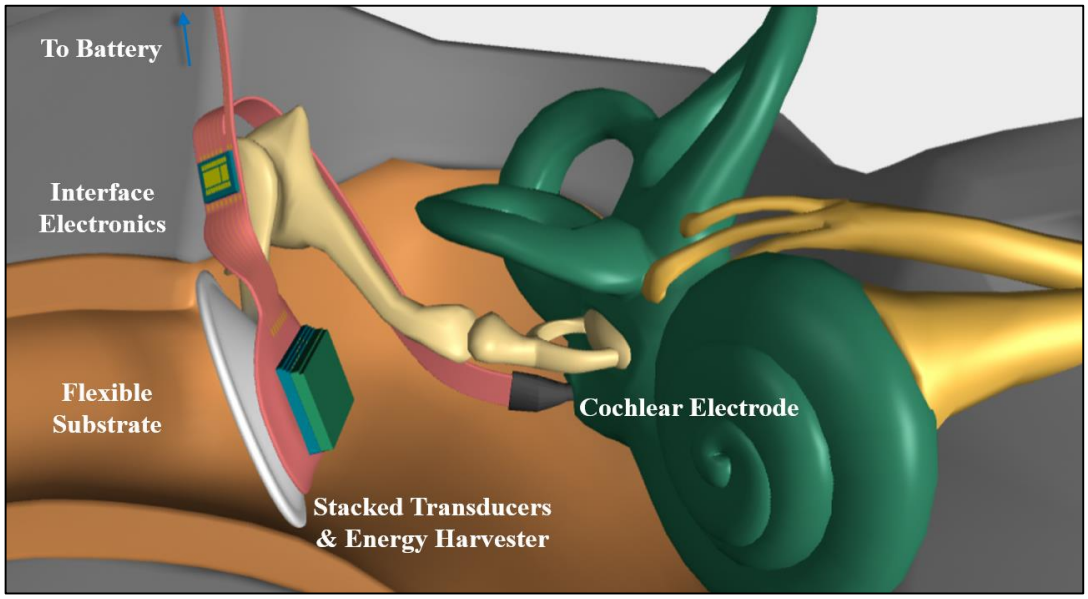

Figure 1.2. Drawing of overall FICI system in-vivo implanted illustration.

Weight of the resonator chip package needs to be below 20 mg, because it will be implanted to a resonating body in the inner ear and increased weight may damage and suppress the movement of the ossicles or tympanic membrane [9]. Therefore, the packaging of the systems becomes challenging, as the whole chip needs to be low weight and occupy as little space as possible. Moreover, bulk and thin film piezoelectric materials are utilized in the transducer and the harvester units of the FICI system. However, piezoelectric materials are highly sensitive to temperature, in fact process temperature above 200°C is advised to be avoided when working with thin films [10]. Further, wire bond technology that is common and easy solution in many of the electronic chip integration applications would not be applicable in this study. This is because it is not a reliable solution to use in implant applications that are in-

vivo. Also, because the FICI system will be implanted on a random shaped location, and the connection need to extend in any direction inside the ear, rigid components will be integrated on a flexible substrate. Electrical connections on flexible substrate cannot be taken as it requires flat and tough surface. Many experiments on this matter in our group have failed and it is understood that a robust and reliable connection technique is needed.

1.2. Objective of Thesis

In this work, early efforts to develop a feasible method for the system integration of a fully implantable cochlear implant using copper electroplated TSVs and a flexible parylene substrate was studied. The whole system requires a platform to be electrically connected. Fully integrated system composes of a 3D integrated MEMS transducer package, an interface circuit for piezoelectric energy harvesting [11] and a conditioning circuit that is designed to process signals from the acoustic transducer for stimulation of the auditory neurons [12]. For this purpose, a parylene carrier with connecting electrodes was designed and fabricated.

3D packaging technology enables production of compact, low weight and robust MEMS devices saving space and resources. Through silicon via (TSV) allows integration of separate devices by electrically connecting them to a low volume package. While, TSV technology have been available for long time, distinct constraints of materials and methods used in MEMS fabrication processes lead to different requirements and production flows. There is via-last approach that offers design flexibility [14] however, it is not applicable when there are suspended resonator structures or temperature sensitive materials as observed in MEMS technology. In such fabrication flows, via first approach can be adopted, where TSV is prepared at the beginning of the process flow. To overcome these limitations, via first TSV integration is a promising solution for 3D integration.

TSVs were produced using number of methods, the carrier wafer method, via sealing and bottom-up electroplating method. In this regard, electroplating wafer holders were

designed to research on as many methods as possible and develop one of the most promising one. The via sealing and bottom-up electroplating method allows the production of TSVs that are compatible for 3D integration. Fabricated TSVs were examined by dicing them to reveal cross-sections using a wafer dicer. Furthermore, they were tested for their electrical resistance.

Filling of the vias during TSV fabrication is the most challenging, in which we used the commonly employed Cu electroplating process. There are two filling mechanisms; conformal and bottom-up [15]. Filling defects in TSV such as voids and seams are more likely to occur in conformal plating, unless additive ratios are well adjusted, whereas bottom-up filling mechanism does not cause them. Bottom-up TSV filling can be realized either by use of a carrier wafer or by sealing the bottom of the TSVs. Temporary bonding to a carrier wafer is costly and detachment process increases its complexity [16]. Thus, via sealing was chosen since it uses a seed layer directly coated onto the TSV wafer and makes the bottom-up plating possible without further processing.

Another 3D integration solution without TSV technology is also proposed using the specially designed and fabricated flexible substrates for the packaging of the chips. All these efforts coincide with the More than Moore trend shown in Figure 1.3, that has been adopted over the recent years for the advancement of the semiconductor industry.

In this thesis, the development of a wafer level TSV fabrication workflow, utilizing bottom-up filling mechanism with the via sealing technique was presented. Feasibility of the system integration with void free TSVs and MEMS acoustic transducer was shown after bonding them using room temperature cured epoxy. Integration of the 3D MEMS piezoelectric resonator stack is bonded on a flexible substrate for signal transfer and implantation purpose. These solutions are important for the further development of the semiconductor and electronics technology as we divert from the destination that was pointed by Moore's and started evolving in more advanced systems by combining technologies.

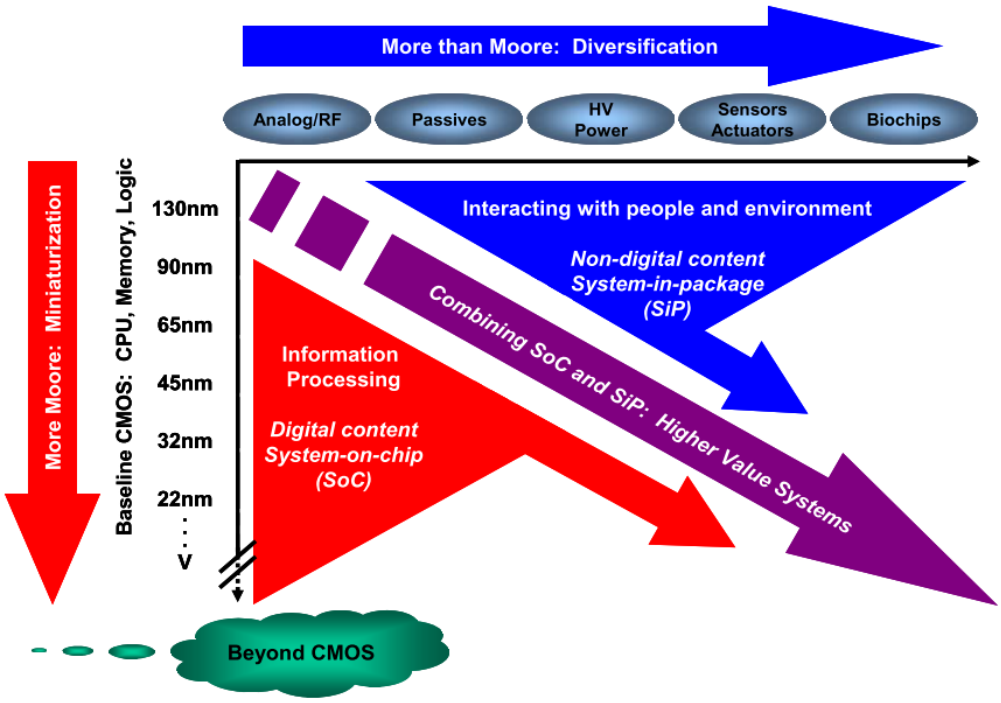

Figure 1.3. Illustration of the future trend for the advancement of the semiconductor technology that merges miniaturization trend of Moore's Law and diversification with other technologies such as MEMS sensors and actuators [14].

1.3. Outline of Thesis

Thesis constitutes of five chapter as explained in main points as followed.

Chapter 2 explains the development of the TSV fabrication, literature, experimentations, and parametric optimization of the proposed process flow. The chapter starts with the importance and the challenges of the TSV integration technology, details of the fabrication methods from the literature and elaborates on the constraints and requirements of the system. Next, fabrication of the empty TSV that is ready for the ECD process, toughest part of the overall fabrication. The chapter continues with the experiments carried out for the establishment of the fabrication flow and preferred electroplating method for the TSV filling step, via sealing and bottom-up ECD, and optimization of its parameters are presented for the defect free result. Finally, the chapter ends with the additional process details for leveling the

wafer surface with TSV for the device fabrication processes and explanation of the double side metal patterning for interconnections.

Chapter 3 presents the literature survey of flexible electronic and biomedical implant technology, design and fabrication workflow of the single and twin type of flexible substrates with metal thin film interconnects for creation of integration platform for the FICI system. The chapter starts with the diverse techniques involved in flexible electronics and their fabrication techniques in the literature. The chapter continues with the 3D integration options of the transducer chips, designing of the proposed flexible substrates and basic COMSOL Multiphysics simulation as the preliminary work of their fabrication. Then, fabrication workflow of the parylene substrate as the flexible platform of the system is explained with the challenging photolithography process, which manages the vertical metal patterning. The chapter conclude with the comparison of the two integration methods proposed.

Chapter 4 illustrates the experimental results of the TSV characterization, working of the piezoelectric MEMS resonators, feasibility testing and flexible substrate integration with room temperature cured silver epoxy. First, four-point Kelvin measurement of the fabricated TSV and wafer level resistance map preparation explained after showing the test setup. Then working principals of the piezoelectric resonators used in the study are explained. Chapter continues with the feasibility testing of the TSVs showed after bonding the fabricated frames with the acoustic transducer chip. Finally, integration testing of the TSV to the single type of the parylene substrate and integration of the twin type of parylene substrate.

In the last chapter, Chapter 5, the overall thesis is summarized while emphasizing the key points and discussing the objectives and results. The study is concluded with the main idea, future work, and suggestions on the related research topic.

Supplemental tables are given in Appendix for some of the process recipe details and the information of used plating solution.

CHAPTER 2

DEVELOPMENT AND OPTIMIZATION OF TSV FABRICATION FOR MEMS RESONATOR INTEGRATION

This chapter demonstrates the development and the process optimization of the through silicon via (TSV) fabrication procedure. It starts by the summary of the literature survey on processes involved and various methods of the TSV fabrication. Continues with the development of the ready to fill TSV wafer fabrication procedure with first and second fabrication cycles. Bottom-up TSV filling process setup and the fabrication workflow are illustrated for the fabricated TSV wafers. Then, followed by demonstrating the work done to choose the method that successfully applied in this study, which is via sealing seed layer method. Moreover, detailed explanations of the TSV fabrication process and optimization steps are elaborated. Finally, demonstration of the additional process steps for TSV integration to the MEMS resonator device fabrication are given.

2.1. Literature Survey on the TSV Fabrication

TSV fabrications differs as via-first and via-middle integration. In via first, high temperature processes can be conducted for the TSV independent of the CMOS or MEMS devices on the substrate. However, in vi-middle integration, process temperature in the industry does not exceed 600 °C and if the process subsequent of a metal layer formation the limit is even lower than 400 °C [17]. Etching of the substrate, dielectric layer deposition, metallization, filling and the flattening steps are the general in the literature. Filling step is the most critical for a successful fabrication. Commonly, electroplating process is preferred as it is well established and easy to utilize. It uses a seed layer on the surface and oppositely charging this layer against the plating solution is enough to initiate the coating. Electrochemical deposition is not

the only way for the filling of the TSV. There is electroless filling process and magnetic assembly of nickel wires methods other than utilizing the electroplating process for the TSV filling [18], [19]. However, most frequently used process is the ECD. Hence, it is easier to develop its methods that are named by the way how the seed layer is established. These methods are carrier wafer seed layer, conformal seed layer and via sealing seed layer. Using the seed layer as one of the given method, copper filling of the TSV performed by the electrodeposition process.

Conformal seed layer method is the most frequently utilized in the industrial applications. Properly adjusting all the chemical components of the ECD solution is a challenging work but it ought to be managed for successful result. Additive optimization is the key element of the process. Voltammetry analysis during the plating, evaluation for putting the right input to the solution and observing the feedback of this change is constantly performed along so many experiment cycles [20].

In the carrier wafer seed layer method, providing the seed layer from additional wafer called carrier wafer is performed. This method actually does not use seed layer deposited on the TSV wafer if does not indicated. It provides easy process without utilizing advanced conformal deposition tools or expensive plating chemistries. On the other hand, a way to get the contact from the seed layer at the back of the wafer with empty TSV holes has to be found. In order for that, laser resizing is applied to etch the edge of the TSV wafer prior to the electroplating process [21] which includes additional etching step by the laser. Moreover, square shaped large through holes are etched on the TSV wafer and copper foil is used to attach the conductive to the seed layer on the carrier wafer [22]. Although, this does not add extra process, it complicates the through etching process of TSV because of the difference in aspect ratios of the structures. In this study, a wafer holder is designed to overcome this issue without adding such complications.

Via sealing seed layer method is the preferred TSV filling method in this thesis, as a result of the experiments carried out in the study. It is a promising method because of resolving some of the concerns experienced in other options. Method constitutes of two steps, the via sealing as the first and bottom-up as the second ECD process step. As it can be envisioned that the successful sealing of TSV openings is crucial for the second step to work as desired. Because the second step basically uses the sealed copper as its seed layer. TSV with 25 µm diameter and 200 µm depth is filled with this method [23].

2.2. Ready to Fill TSV Wafer Fabrication

Electrochemistry behind Cu electroplating and TSV filling is a complex process where variables such as the used chemicals, the chemical bath, used filling method, surface morphology each play an important role in the success of the whole fabrication. Therefore, ECD process optimization requires many trial and error steps which means that a large number of sample wafers are required thus, fabrication of the sample wafers with via holes is the primary step of the whole process. Si wafers to be used in such processes must have properties that are in alignment with the application. In this work, Si wafers of thicknesses in the 320 - 300 µm range were needed due to the through via etching capability of the DRIE tool at a given aspect ratio (AR). AR is the division of the depth to the structure to its diameter.

Wafers we had in hand were 525 - 550 µm therefore required thinning in DRIE process followed by through via hole etching and dielectric layer formation on via sidewalls. These steps are common for both methods, the carrier wafer and via sealing seed layer, used in this work. Both methods make use of through etched via holes whereas; the conformal seed layer method uses blind via hole.

The main process flow is optimized as in Figure 2.1. There is also a shorter version of this process flow in Figure 2.3, which was used in the development of the first fabrication cycle to determine parameters used in the main process flow.

2.2.1. Wafer Thinning Process

A regular silicon wafer with 525 - 550 µm thickness is brought down to 320 - 300 µm level using the DRIE process. The necessity to use thinner wafer has been arisen from the through via etching capability of the DRIE tool at a given AR.

Selection of the aspect ratio of a TSV with the desired properties (eg. vertical walls, small scallop size etc.) is a challenging task that is addressed under 2.2.2 section in this chapter, where the through etching process of the TSV is explained. Keeping the diameter of the TSV at a fixed number and reducing the wafer thickness decreases the aspect ratio. This mainly helps the through etching to become faster and more importantly defect free. After observing this, thicknesses of the wafers are varied between 400 and 200 µm to test the thin wafer handling capabilities. Although wafer thickness values vary, after the first fabrication trials wafer thickness set to 300 - 320 µm. Moreover, set of diameter values are experimented before making the decision to use TSV diameter fixed to 100 µm in the study after the initial development cycle. It is important to add that, AR is a parameter that affects the copper ECD filling of the TSV, as it is explained in section 2.3.

Wafer thinning could have been carried out with mechanical grinding, chemical mechanical polishing (CMP) or simply wet etching processes apart from the dry etching, which uses DRIE plasma. However, among those options dry etch is known to have faster etch rate than its counterparts [24]. In addition, obtained surface roughness and the total thickness variation is better than what is expected from a mechanical etch. Wet etch process is sensitive to variations in the temperature and solution composition parameters that cannot be strictly controlled as the dry etching where DRIE tool adjust the set values with sensor and controllers such as mass flow controller (MFC) and pressure sensor. Furthermore, the CMP tool is not available in the facility. Therefore, dry etch process was preferred.

For this process to be performed with the plasma of a DRIE tool it is important to know how the wafer is clamped during the process. STS Multiplex-Pegasus DRIE tool

uses electrostatic clamping, while HRM tool uses mechanical clamping. This means that HRM has to put mechanical pins onto the wafer surface to hold it during the process that are preventing the plasma etching. In order to get the smooth and flat surface with minimum total thickness variation (TTV) possible, DRIE tool (STS Multiplex Pegasus) is used.

Backside of the wafers are thinned down to keep the device surface untouched. During the thinning process thus, backside surface is exposed to the plasma. Electrostatic clamping is expected to seal the front side of the wafer to the chuck inside the chamber during the process. However, in reality, chuck is not effective enough to prevent the plasma leakage from the tiny openings and eventually damaging the front surface. Even more critically, since there is nothing to stop it, the side of the wafer edges are etched as well. Nonuniform etching at the edges creates notches and cavities that can lead to the breakdown of the wafer. Therefore, before getting started with the thinning step, front side of the wafer is coated with the protective silicon di-oxide layer, which at the same time coats the wafer edges. As illustrated in the Figure 2.1, thinning step comes after the SiO_2 deposition.

PECVD (STS Multiplex - ASE HRM) tool is used for the SiO_2 deposition process. Thickness of the required protective layer empirically determined to be 0.5 µm for the 230-250 µm etch thickness. Thickness needs to be higher if a thicker wafer is used. When SiO_2 layer is thicker than required plasma etching is delayed at the region near to the wafer edge due to thick protective layer, leaving a region with higher surface than the rest of the wafer. This is why the SiO_2 layer thickness should be in the sweet spot where it is strong enough to protect but weak enough to disappear just to etch the edges same as the rest of the surface.

In the Pegasus DRIE tool, the thinning recipe has SF_6 and O_2 gases at 10/1 ratio. Recipe is used as five equally divided etch cycles with wait time in between each etching cycle. Unlike the regular vertical etching of the DRIE tool that uses Bosch Process, which is elaborated in the next section, there is no passivation cycles. Hence,

no passivation gases are used. Etch rate of the recipe is 13 µm per minute for silicon. Dopant type or the atomic planes was not observed to cause a significant effect on the etch rate. After the thinning process, rest of the protective SiO_2 layer is removed with BHF solution.

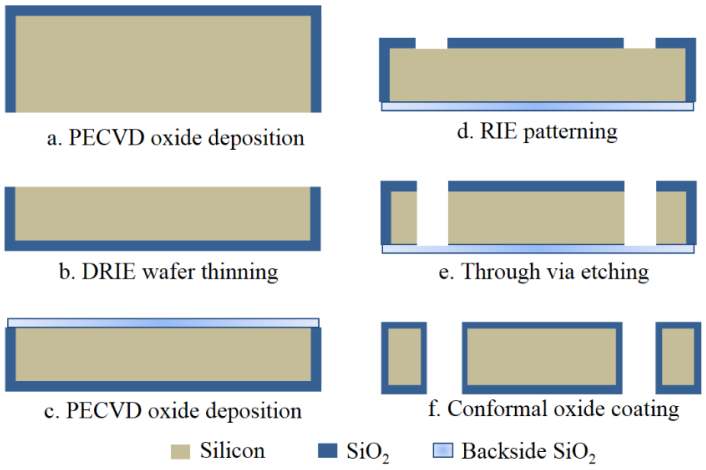

Figure 2.1. Process flow of the ready to fill TSV wafer fabrication.

2.2.2. Through Via Etching

In this section, Bosch Process is introduced, development of the first fabrication cycle is summarized and optimized process flow shown in Figure 2.1 is explained. Since this is a critical process step, other intermediate steps such as photolithography and SiO_2 deposition process are described under this section together with DRIE process.

Bosch Process is used for the vertical etching of the silicon substrate in anisotropic manner and allows us to create high aspect ratio structures [25]. It utilizes time multiplex cycles in the order of first passivation and then etching. Substrate bias power is maintained during the process similar to the other process tool where plasma power is used. Process starts with the conformal deposition of passivation polymer layer, which is created by the C_4F_8 (Octofluorocyclobutane) gas flow inside the chamber. In the etch cycle, C_4F_8 gas purged from the chamber and SF_6 (Sulfur hexafluoride) gas introduced to the chamber. Inductively coupled power (ICP) forms the dense and powerful etch plasma simultaneous with the vertical ion bombardment to the bias

powered substrate. This is also known as the ion-assisted reaction as demonstrated in Figure 2.2 [26]. Deposited polymer layer protects the vertical surfaces against etching while horizontal surfaces continue to be etched because the passivation layer removed with the physical etch due to the directional ion bombardment. Thus, etching proceed in the vertical direction.

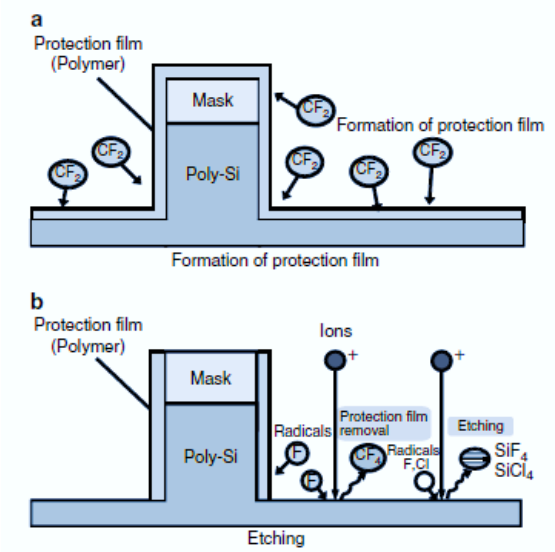

Figure 2.2. Ion-assisted reaction and sidewall protection, a) passivation, b) etching steps [26].

Each passivation and etch step has isotropic component that creates micro or nano sized patterns on the etched sidewalls called scallops. It is a very complex system to optimize for a specific purpose, such as to have fast and anisotropic etching at the same time. Scallops get bigger and create excessive undercut if fast process is applied with the reduced passivation or increased etch power. In comparison, slower process creates very little scallops and almost flat sidewall; however, still it etches the same thickness of process mask. Therefore, obtaining flat sidewall with high aspect ratio requires thicker and stronger process mask and even multiple photolithography steps. For example, in DRIE tool (STS Multiplex Pegasus), the slower recipe name is 'Structure' and the faster one is the 'Santez'. Using the 3 µm photoresist mask, Structure recipe etches 75 µm while Santez recipe etches up to 350 µm silicon depth

with the same mask. Details of these two recipe are given in the appendix. This justifies the usage of Santez recipe for the DRIE through via etching process.

2.2.2.1. Development of the Firs TSV Fabrication Cycle

Apart from the DRIE recipe decision, the design consideration of TSV, the diameter is also critical for the through etching step. For this decision, a process mask with 150, 100 and 50 µm diameter TSV is designed. First fabrication cycle is carried out with this mask to see which TSV diameter is applicable. This fabrication cycle is continued to be elaborated under the section The First Fabrication Cycle for Electroplating Process.

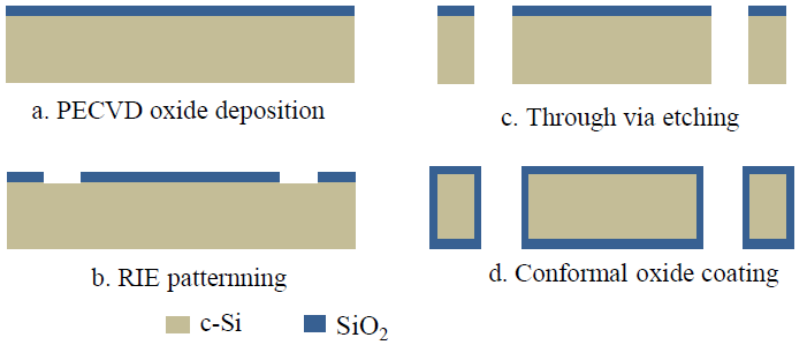

Figure 2.3. First ready to fill TSV wafer fabrication, process flow drawing.

In the first TSV fabrication cycle, Piranha and BHF cleaned single crystalline silicon wafers were directly taken to the PECVD SiO_2 deposition step for hard mask formation on front side. Deposited oxide thickness was 1.6 µm. Then, SPR 220-3 photoresist was spun at 3000 rpm for 30 seconds using the spin coating tool. Resulted thickness is 3.2 µm polymer layer. Soft bake was applied for 3 minutes on the hot plate that is at 115 °C prior to 8 seconds of mask exposure with 12 mJ UV lamp. Development step took 54 seconds. It is performed by immersing the wafer in MF-24 developer solution for the suggested development duration and following cleaning steps in deionized water (DI). Wafer then dried with the help of N_2 gun. Next, PECVD SiO_2 was patterned with buffered HF solution with HF:NH4F (1:7) ratio in 23:30 minutes. Microscope observation at this point yields different etch rates in vertical

direction for different circle diameters as shown in Figure 2.4. Thus, 2:30 minutes more BHF etch applied till all the circles are opened, making the total process time 26 minutes.

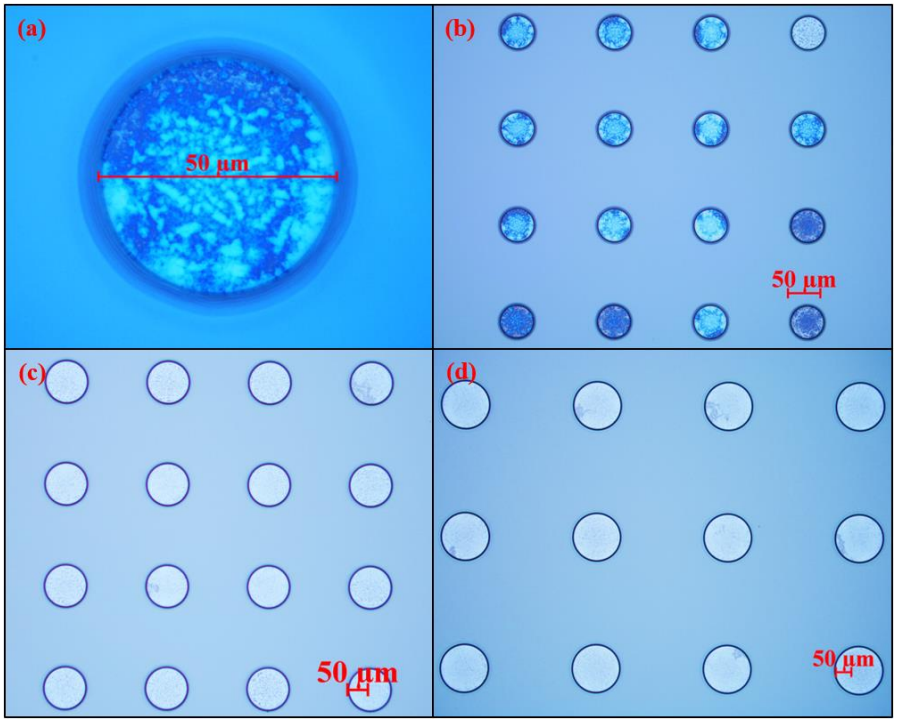

Figure 2.4. BHF etch result after 23:30 minutes process showing remaining SiO_2 for, (a) 50 µm close-up, (b) 50 µm array, (c) 100 µm array, and (d) 150 µm diameter circle array.

Through via etching step took 24 minutes to open the alignment mark structure because they are the widest pattern. Santez[2] recipe is used for this process. Recipe has 7 seconds etch and 3 seconds passivation and 15 seconds stabilization time. Six times a minute process is applied 4 times for the 24 minutes process. Via holes with 150 µm diameter were opened after two more 6 x 1 minute process. 6 x 30 second process was enough to open the 100 µm diameter vias. 50 µm diameter vias were left unopened because continuing the process was started to damage the opened via structures. This shows how the process time dramatically increases when the opening diameter is smaller. Alumina wafer used after the first 24 minutes part of the process to protect

[2] Properties of the recipe is given in Appendices A.

the process chamber. It makes Helium (He) cooling gas flow applied to the backside of the wafer ineffective to cool the wafer. When the wafer gets hot, process mask on the surface becomes weak and does not last longer.

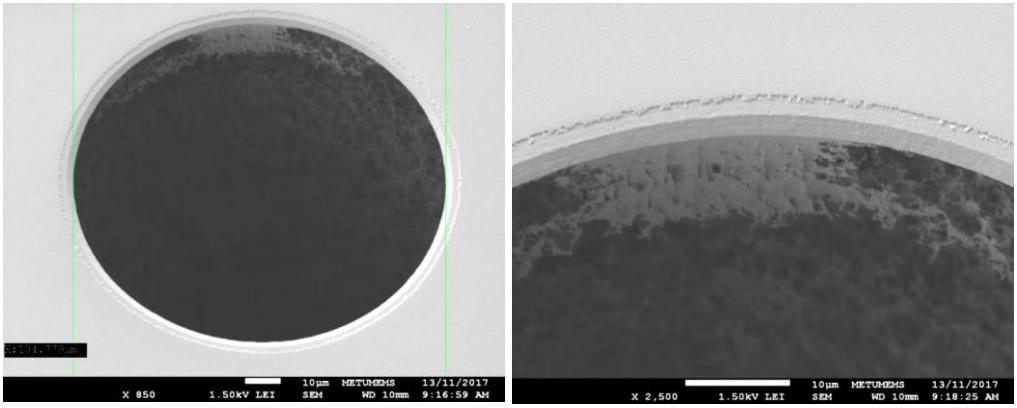

Figure 2.5. SEM observation of 100 µm TSV opening on 30° tilted wafer.

Result of the through via etching step of the first fabrication cycle is investigated with the SEM observation by tilting the wafer at an angle of 30° to the horizontal level. Opening diameter of the structures were also measured and via with 100 µm diameter is demonstrated in Figure 2.5. Particular one is chosen as design parameter for the rest of the TSV fabrication. Because it can be through etched only with additional 3 minutes DRIE process to 150 µm diameter via, taking 39 minutes through etching time in total. Through via structures with aspect ratio of 5.5 was obtained. Furthermore, in the TSV filling section, preference of narrower TSV diameter is justified. After DRIE diameters are measured as 155.6 µm, 104.8 µm and 54 µm for the all three via openings. Fabrication flow in figure Figure 2.3 continued in the insulation layer deposition section.

Other process observations from the first TSV fabrication cycles was the use of RIE process instead of the BHF process for the SiO_2 patterning step and utilizing backside protection layer for the through via etching. Microscope observation after through via

etching shown in Figure 2.6 demonstrated that isotropic nature of the BHF process caused over etch and damage occur on the edges of the via openings.

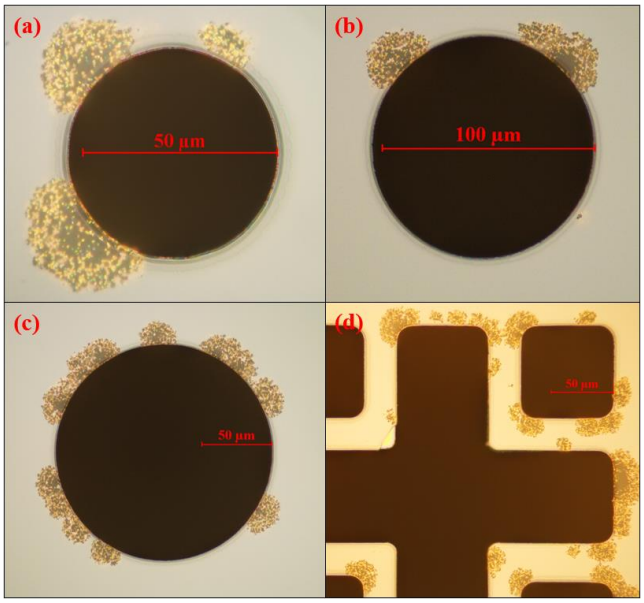

Figure 2.6. Damage of over etched SiO_2 mask observed after DRIE through etch on 50, 100, 150 µm diameter TSV holes in (a), (b), (c) respectively and the alignment mark (d).

Wafer level image after the DRIE process can be seen in Figure 2.7 left image, showing the via hole openings in different diameters from the front side. The necessity for a protective layer at the backside of the wafer was understood after observing the exiting side of the through etch process. Since in reality, it is not possible for all TSV to open simultaneously, the image on the right in Figure 2.7 will occur at the backside of the wafer in any through etching process. To prevent the surface from the plasma damage, additional PECVD SiO_2 layer is applied.

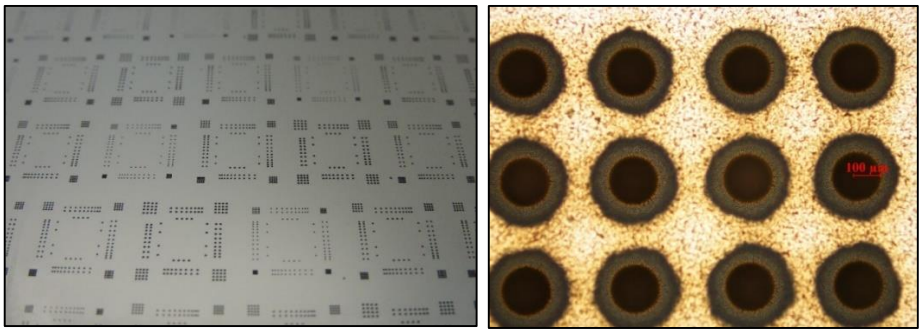

Figure 2.7. Front side of the wafer level photo after DRIE through etch on the left, backside surface of the wafer, showing the plasma damage at the 150 diameter opening edges from microscope image.

2.2.2.2. Optimization of Empty TSV Fabrication Cycle

After determining the TSV diameter, main process flow shown in Figure 2.1 is continued with the optimization of TSV fabrication cycle. Process mask with only 100 µm diameter opening was designed and used in this cycle. Since there is only one diameter value, different speeds of DRIE etch rate is no longer a problem.

Firstly, wafers thinned down to 390 - 380 µm with 5 x 3 minutes process in Pegasus DRIE making 15 minutes total dry etch time. PECVD SiO_2 layer of 0.5 µm deposited to the front surface prior to thinning, process took 6 minutes 30 seconds. Next, SiO_2 layer removed by immersing the wafers in BHF solution for half an hour and cleaned in Piranha solution for half an hour. Then, PECVD SiO_2 coating applied on front side for hard mask purpose with 1 µm and backside of the wafers for protecting the etch plasma exit surface with 0.5 µm layer. Photolithography step was the same as the process previously described in section 2.2.2.1.

SiO_2 hard mask layer is patterned with RIE process instead of BHF as illustrated in Figure 2.1(d). step. Etching of 1 µm PECVD SiO_2 took 13 minutes with resulted minimal over etch. Following fabrication step was through via etching in DRIE tool. Through etching step took 27 minutes in total using the Santez recipe. Fabricated empty TSV structures were ready for dielectric layer formation on sidewalls after the photoresist and SiO_2 removal and other cleaning processes.

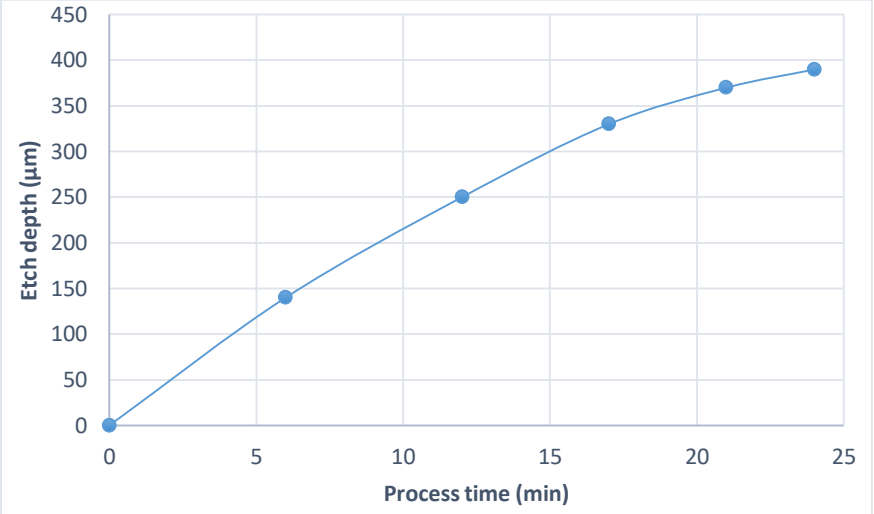

Figure 2.8. DRIE etch depth versus process time for the mask alignment marks.

Since the process is carried out stepwise, after each 6 x 1 minute of etching, microscope observation to measure the etch depth yield the etch depth against process time curve in Figure 2.8 for the alignment marks on the wafer. TSV opening with 100 µm diameter are small for the microscope light to allow proper observation but, it can be estimated that the etch rate get even more dramatic retardation. Nevertheless, effect of wafer thinning clearly seen on the same diameter of opening. When the wafer thickness goes down around 160 µm, through via etching takes 12 minutes less. This helps to improve the obtained sidewall quality by reducing the over etch of scallops.

In the next fabrication runs, increased DRIE thinning process applied for total of 18:45 minutes to thin down the wafer to 320 µm. The workflow described earlier in this section was followed for the front side protection and subsequent cleaning steps. Used backside protection SiO_2 layer was increased to 0.6 µm to account for the deeper thinning, which is around 230 µm. Thinner SiO_2 layer was ineffective at protecting the wafer edge. This time, 0.5 µm SiO_2 layer is deposited only for backside protection. Hard mask for through via etch process is not used on front side. However, at the photolithography step, SPR 220-3 photoresist spun on wafer at 2000 rpm instead of 3000 rpm. This is to increase the photoresist thickness from 3.2 µm to 3.9 µm and make sure enough masking performance in subsequent processes is available. Soft

bake was increased to 4 minutes and exposure was applied for 10 minutes. Development step was 58 seconds.

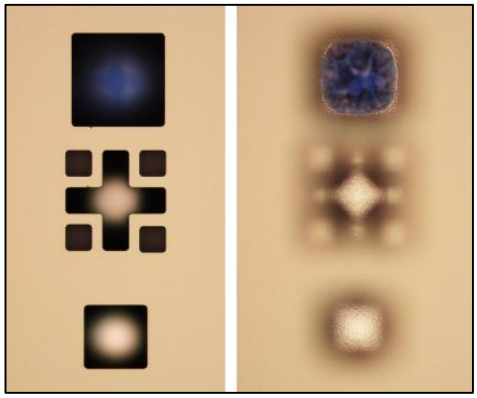

Figure 2.9. Microscope image of the alignment mark after 13 minutes of DRIE process, focus at top surface and focus at bottom from left to right respectively.

Through via etching process took 18 minutes to etch all TSV openings on the wafer. It is proven to use only photoresist based process mask is enough for this process. Microscope observation when the first alignment mark opened shows the SiO_2 layer as a membrane at the bottom of the opening in Figure 2.9 in 13 minutes of through etch process. Largest alignment mark was almost through etched until the protective SiO_2 layer at the bottom while other marks haven not been opened.

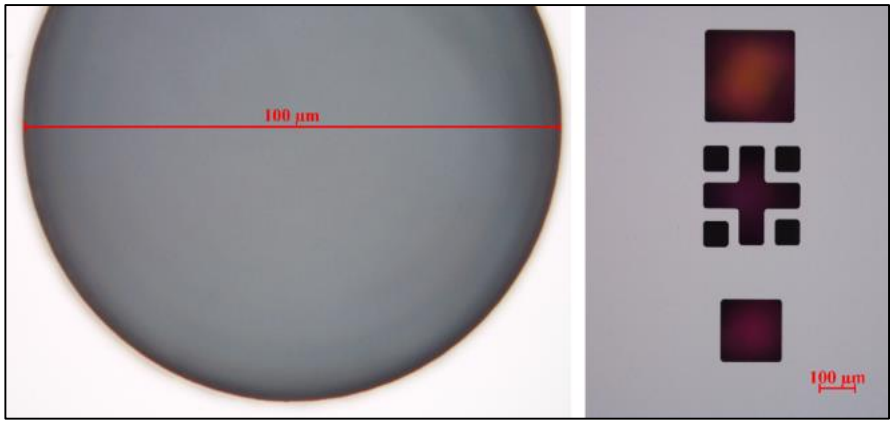

Figure 2.10. Through etched via opening on the left and alignment mark on the right after 18 minutes DRIE process from front side.

Diameter distribution of via openings along the wafer was investigated with microscope observation on the whole wafer when the through via etching process is finished. On the front side, opening diameters were similar along the wafer with only minimal over etch around 1 µm was observed as shown in Figure 2.10. However at the backside, openings at the center region were etched more than the ones at the edge region of the wafer as shown in Figure 2.11. Widest openings were obtained in between the center and the edge regions. Etch plasma exiting damage observed in Figure 2.7 is prevented by the use of protective SiO_2 layer.

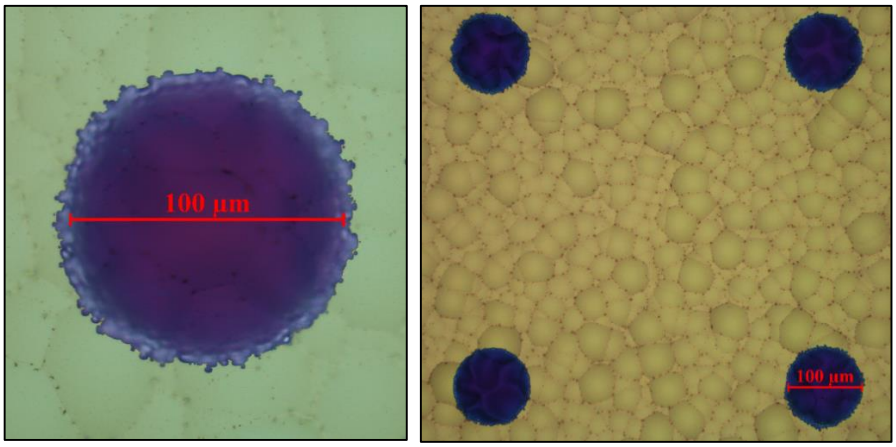

Figure 2.11. Through etched via opening after 18 minutes DRIE process from backside, on wafer center region and edge region from left to right.

After the through etching step, PRS-2000 solution removes the remaining photoresist. Additional polymer removal process using the O_2 plasma is used to clean the burned photoresist residuals. Then, using the Piranha and BHF solutions respectively for half an hour, organic residuals and SiO_2 layer is removed. Physical opening of the through via take place when the SiO_2 membrane is dissolved although light can pass through.

2.2.3. Insulation Layer Deposition

Conformal coating of the electrical isolation layer on the TSV sidewalls and the wafer surface is critical for eliminating the possible leakage currents to the single crystalline silicon substrate from the metal lines. For this purpose, various materials with high

dielectric strength has been used such as spin on dielectric polymers, parylene, chemical vapor deposition oxide and thermal oxide.

Spin on dielectric polymers are coated on a wafer with annular trench, then TSV structure ready for filling step is formed by etching the center silicon pillar [27]. This option is prone to many errors such as air bubble stuck in the annular trench may prevent the polymer coating. Also, it needs many more process mask just for this process step. Parylene coating has been utilized in some of the studies since it can be coated at room temperature [28]. It is more conformal coating option than spin on polymer coating. Although they used parylene-HT, which stands for high temperature, process temperatures above 250 °C may cause damage at the dielectric layer. For this concern, SiO_2 layer is more reliable than polymers. SiO_2 layer can be formed by thermal oxide or plasma deposition process. Plasma deposition systems can process even single wafer where thermal oxide need tens of wafers to be practical. This is because thermal oxide takes hours while plasma deposition can be in minutes. Therefore, plasma enhanced chemical vapor deposition (PECVD) process is utilized in most of the studies [29].

At this point in this chapter, PECVD process has already been mentioned many times but they were all done on flat surfaces whereas in this section, it is expected to be conformal on vertical TSV sidewall. Investigation of the conformal coating performance on sidewalls shows that the region near to the bottom of the TSV has the thinnest layer thickness in Figure 2.12 [30]. Considering this analysis, PECVD SiO_2 deposition for electrical isolation on the TSV sidewalls is deposited from the both front and backside of the wafers to provide thicker film at even the hardest point to reach.

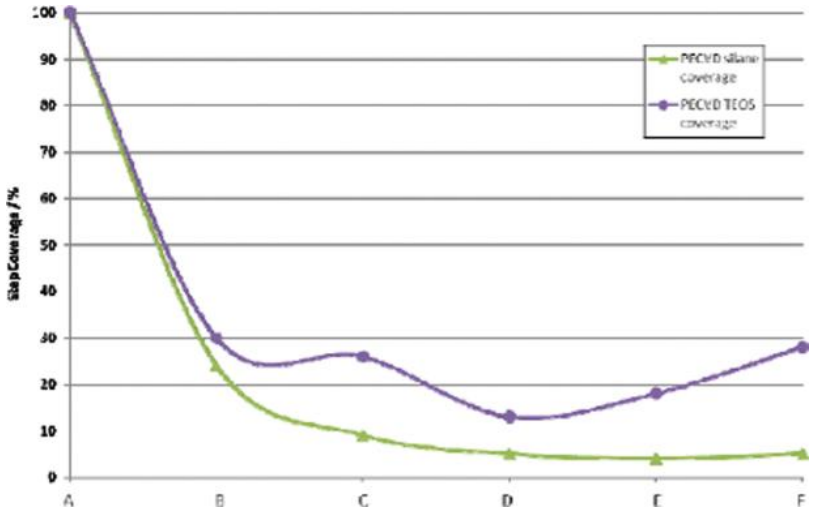

Figure 2.12. Two different PECVD SiO_2 layer thickness deposited at 175 °C on a blind via, given in percentage for regions top to bottom from A to F [27].

Wafers are 1 µm PECVD oxide coated from both sides to create the electrical insulation layer. Recipe of SiH_4 and N_2O with N_2 based mixture is used at 300 °C process temperature. Deposition rate is almost linear with 0.077 µm/min, slight decrease can be observed as the deposit thickness increased. This process recipe was used in all fabrication cycles in STS PECVD system without a change. Ready to fill TSV wafer fabrication ends with this step as illustrated in Figure 2.1 (f). For the copper filling step, seed layer is deposited according to the bottom-up electroplating method followed.

2.2.4. Seed Layer Formation

For the filling of the through via with a conductive material, copper electrodeposition (ECD) process is used. Seed layer is necessary because this process requires initial conductive layer to initiate the growth. As briefly described in the literature survey section, formation of this layer depends on the TSV fabrication method. For the ready to fill TSV wafer fabrication, this is the final step.

In this study, since through etched via structures are used, carrier wafer seed layer and via sealing seed layer methods were chosen for the TSV filling step. Thus, seed layer formations were done according to these methods. Blind via structures are not used

because of the limitations of the process capabilities. Blind via filling is done with the conformal seed layer process, which requires deposition of the seed layer through its sidewall and the bottom. Furthermore, the dielectric layer coating must be conformal prior to the seed layer which requires thermal oxide process to make sure its quality. These potential issues also limit the aspect ratio of the TSV that can be fabricated. Whereas in through etched structures, seed layer at the bottom of the TSV is enough and even PECVD oxide can be used, since it is deposited from both front and backside of the wafer.

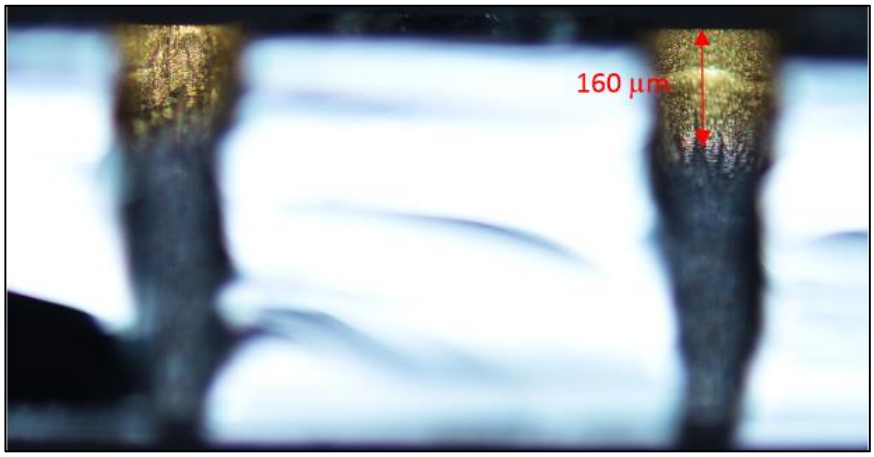

Figure 2.13. Broken wafer sample cross section showing the Cr/Au sputter deposited seed layer depth inside the TSV.

For the seed layer formation, metal sputtering (AJA Magnetron Sputter System) is used. 30 nm thick Chromium and without taking the wafer out of the chamber, immediate coating of 500 nm Gold is performed. In the TSV fabrication with carrier wafer seed layer method, this coating applied on 6" handle wafer. On the other hand, metal sputtering is done on 4" TSV wafer front side surface in the via sealing seed layer method. Result of this process from the cross sectional view of a 100 µm diameter TSV structure can be seen in Figure 2.13. Deposited metal can reach up to 160 µm depth. After this process, wafers are ready for the filling by copper electrochemical deposition (ECD) process.

2.3. Bottom-up TSV Filling by Electroplating

In this step, the desired seed layer setup is to have it close the bottom of the through via opening to let the vertical growth in upward direction. This process is the most critical step of the TSV fabrication because there are many challenges involved. This is because having the seed layer at the bottom of via hole in perfect contact is difficult. It can be done by two ways; carrier wafer method or via sealing method. The first one needs temporary bonding to an external conductive layer such as conductive film or seed layer on another wafer called carrier. Second one is naturally providing seed layer at the bottom of the through via by sealing the via opening using the seed layer on the via edge.

In this section, first, electroplating process setup is explained and the first fabrication cycle is illustrated. According to the experienced cycle, two process methods to be experimented are selected to enable bottom-up TSV filling; carrier wafer method, via sealing method. Designing and manufacturing of the wafer holders for the both methods are explained and the rest of the details regarding the development of the bottom-up TSV filling by copper electroplating is described as follows. The current pulse timing for the electroplating process is determined using different timings with the number of experiments conducted in carrier wafer method. It is aimed to find the best current pulse timing in our electroplating setup for our TSV structures. Carrier wafer method is suitable for quickly performing the experiment and checking the result of deposition by separating the TSV wafer from the carrier wafer. Otherwise, it would be necessary to dice the wafer each time to observe the deposit from the cross section.

After determining the pulse timing to work with, it was decided that in order for carrier wafer method to be successful for the final TSV fabrication process flow, it needs additional processes to be developed first. That are temporary bonding and releasing processes for TSV wafer on carrier wafer before and after the electroplating process respectively. Thus, via sealing method is chosen since it uses a seed layer directly

coated onto the TSV wafer and makes the bottom-up plating possible without further bonding and releasing processes. This method consists of two steps as via sealing and bottom-up electroplating in order. Only, an additional photolithography step for the seed layer masking with the film photoresist is introduced in this method. A special wafer holder for bottom-up electroplating step is designed and manufactured for this method. Experiment cycles started with the previously determined pulse current timing. It was observed to give the best result in this method as well, even though a few more other pulse schemes are tried. The problem was even though in some TSVs desired void free filing profile was obtained, wafer level uniformity was not satisfied. Until this stage in the experiments, same copper electroplating solution is used that has no additives. Finally, in order to increase wafer level uniformity, additives are introduced into the solution and after couple of experiment it is achieved.

2.3.1. ECD Process Setup

TSV filling process performed with the electrochemical deposition setup ECSI Fibrotools (ElectroChemical Systems, Inc.). Its five main components are shown in Figure 2.14 as pulse current supply, pump controller and electrode input/output, anode metal disk, filtering and stirring pump, heater. In addition to all, there is cathode placed inside of the plating bath as in face-to-face manner with the anode on top.

First unit is the pulse power supply, which is used to set the level of the applied current and to adjust its pulse scheme and direction. It can apply voltage or current depending on the selection. For setting the applied current, its magnitude is observed from the current reading coming from the circuit starting from the supply, anode, electrolyte solution and cathode back to supply again. Pulse timing is adjusted by setting ON/OFF time of the current. If only ON time is entered, current supply acts like a DC current supply. Furthermore, this unit has the process time counter that can be set to finish the process when the desired duration ends. Second unit is pump controller and input/output port of the pulse power supply unit. Its positive port is connected to the anode and negative port is connected to the cathode in normal operation. Third unit is

the metal disk that works as the anode. It can be changed for different size of wafers as 4” or 6”. Metal disk does not dissolve during the process, and it is covered with a fabric material with fibrils against deposition. Fourth unit is the water pump for stirring the electrolyte solution in the plating bath and simultaneously filtering the impurities and contamination that may in the solution. Fifth unit is the heater that is generally used in gold electroplating process.

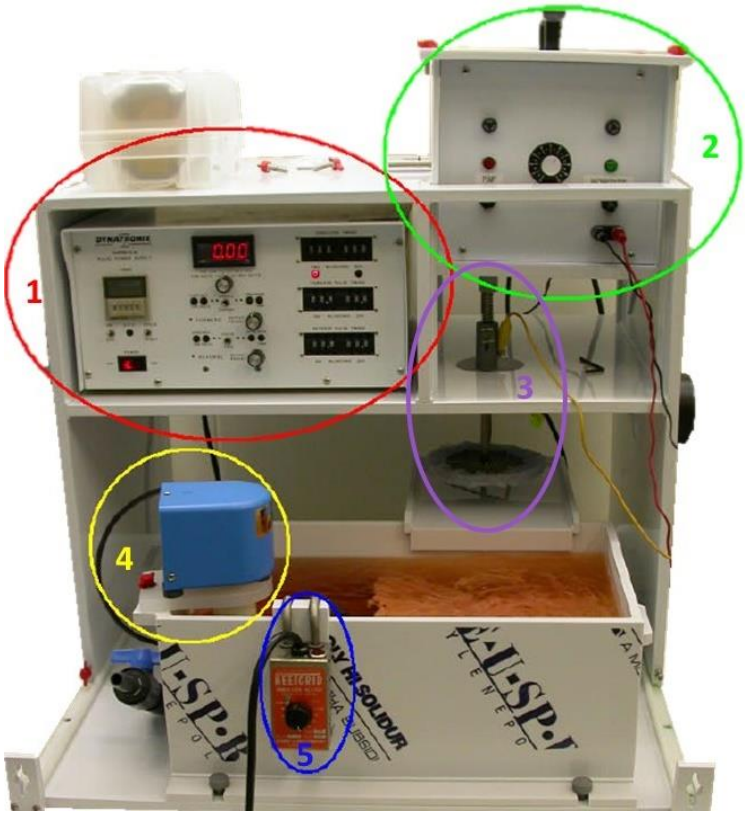

Figure 2.14. ECSI Fibrotools electrochemical deposition process setup; 1) Pulse power supply, 2) Pump controller and input/output port, 3) Anode disk, 4) Filtering and stirring pump, 5) Heater ((Electro Chemical Systems, Inc.)

Cathode of the system is the wafer under the deposition process, which is installed in wafer holder with electrode connections to the wafer seed layer from its handle that is connected to the pulse power supply. Depending on the process method, requirements for the wafer holder changes. For the two different methods of bottom-up TSV filling

method studied, special electroplating wafer holders were designed and manufactured, that are explained under the related sections.

2.3.2. The First Fabrication Cycle for Electroplating Process

Fabricated wafers from the first process flow shown in Figure 2.15 are continued to be used in electroplating process as the first cycle. Thickness of the wafer is 550 µm as there was no thinning process in this cycle. For the first bottom-up electroplating process with the setup described Figure 2.14, first wafer holder is designed and also fabricated. This tool is basically designed to get electrical contact from the bottom side of the wafer. As it is shown in the same figure, there is metal line coming from its handle and circling at the bottom. In the circler part, meal line is transformed into mesh structure and embedded into silicone to isolate from the electrolyte solution, and to cover-up wafer seed layer. Mesh is randomly exposed outside from the silicone to create electrodes. Cr/Au seed layer sputtered TSV wafer is film photoresist coated to seal TSVs from the bottom and prevent deposition to seed layer. Seed layer is left open on the wafer edge to allow electrical connections. TSV openings with 150 µm diameter are easily seen from away whereas smaller ones are not. The first bottom-up electroplating process flow in illustrated in Figure 2.16 as the continuation of first ready to fill TSV wafer fabrication process flow.

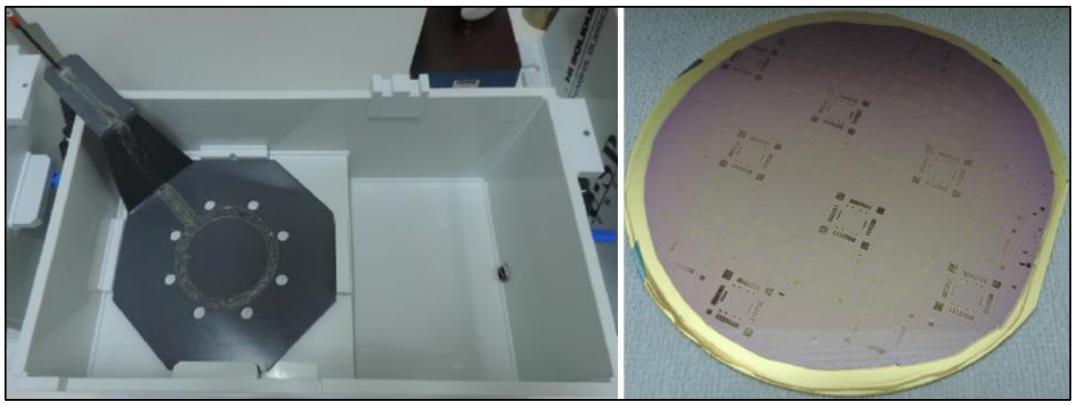

Figure 2.15. First bottom-up electroplating wafer holder placed inside the plating bath on the left, film photoresist coated TSV wafer with seed layer on the right.

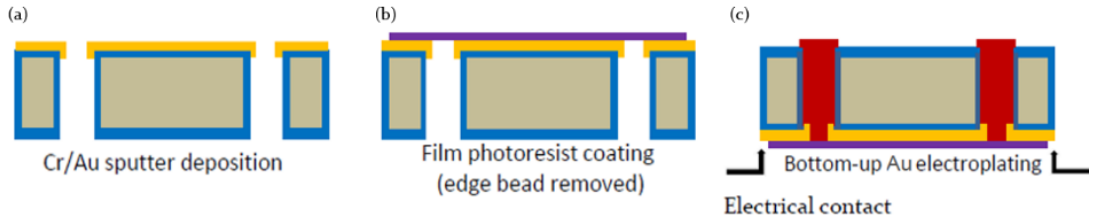

Figure 2.16. The first bottom-up electroplating process flow

The Au electroplating process is conducted for 3 hours at 50 °C. using 24 mA as forward current pulse scheme of 0.4 seconds ON, 9.6 seconds OFF time. We wanted to obtain something observable, thus, we boosted the current accordingly. Normally, 6 mA current was set in this setup in use for the flat surface applications. Approximate plating area was 1.22 cm^2 but the total area exposed to the electrolyte solution is probably higher than this value, because the silicone of the holder electrode is not satisfying to be water proof.

Result of the process showed that the seed layer on the sidewalls continued to grow through the side walls of the TSV during the gold electroplating process. As shown in Figure 2.17, inside of via holes were left empty after the process. This is a significant problem that was addressed by the effort to close up the bottom of the TSVs with the seed layer prior to the bottom-up electroplating process. For this reason, carrier wafer method and via sealing method are adopted for the development of the TSV fabrication. TSVs with diameter 100 µm observed to be filled faster than the wider ones, thus, 100 µm is chosen for the TSV diameter in next fabrication cycle. Furthermore, it was discovered that the wafer holder was not preventing the electrolyte leakage to the seed layer and the electrodes. Also, it was not providing uniform current distribution along the wafer. Deposition was observed to be overfilling on the edge region while center region had only half filled TSVs. Therefore, wafer holder with O-rings and uniformly distributed electrodes is designed for both methods.

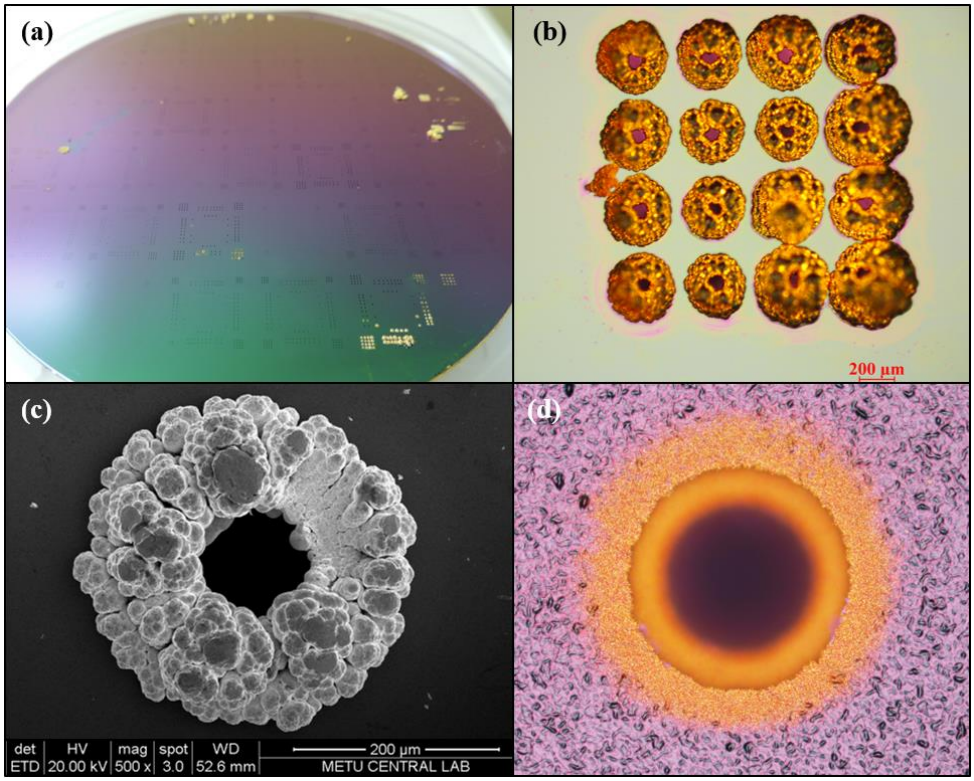

Figure 2.17. Result of the first bottom-up electroplating process, (a) wafer front side, (b) over filled TSV from wafer edge region, (c) torus shaped deposit in SEM, (d) seed layer surface

2.3.3. Carrier Wafer Method

In this method, fabricated TSV wafers coming from the process flow illustrated in Figure 2.1, together with the 6" carrier wafer with seed layer went through the bottom-up Cu ECD process illustrated in Figure 2.16. TSV wafers has only 100 µm diameter opening type. Using the seed layer on the carrier wafer, we are able to provide the seed layer at the bottom of the TSV. Thus, bottom-up TSV filling by copper electroplating process is able to be performed. Seed layer area is assumed to be as wide as the addition of the exposed are of all TSVs which is approximately 1 cm^2.

When they put together in the ECD holder, it is already squeezing the TSV wafer from its edges by the O-rings. However, it was realized from the initial electroplating experiments that the center of TSV wafer was not in contact with the carrier wafer seed layer. To solve this issue, carrier wafer is first coated with PECVD SiO_2 layer to

create compressive stress. This bends the carrier wafer as its center becomes higher than the edge and works for intended purpose of squeezing the TSV wafer from its center as well. With this extra layer, two wafer are aimed to be in uniform contact along the TSV wafer bottom surface.

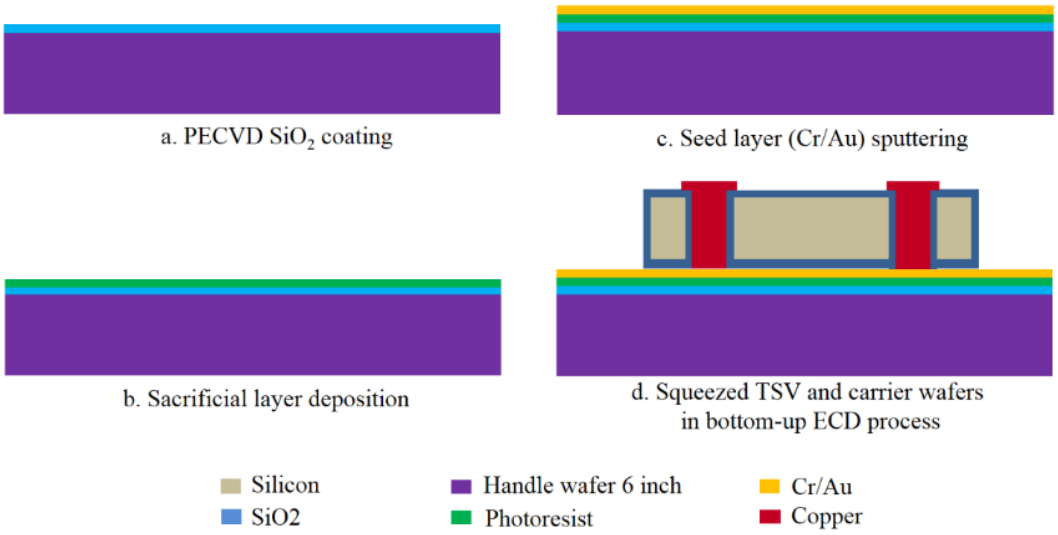

Figure 2.18. Process flow of carrier wafer method.

Using the PECVD tool, 2 µm SiO_2 film is coated on the front side of the 6" carrier wafer. Stress measurement after the coating is showed compressive stress enough to bend the wafer to form 42,5 µm bow. Then, PR 220-3 photoresist spin coated on the SiO_2 surface at 3000 rpm resulting in 3 µm layer. This is for having a sacrificial layer between the seed layer and the carrier wafer substrate so that we can release the TSV wafer after the electroplating copper growth from the seed layer is finished. Finally, the seed layer is sputter deposited as Cr/Au layer in 30 nm / 500 nm film thickness prior to the electroplating process using the carrier wafer holder.

2.3.3.1. ECD Wafer Holder Design for Carrier Wafer

Initial work to enable the TSV fabrication process was to design and manufacture electroplating wafer holder that is crucial for the bottom-up filling step shown in Figure 2.18. The holder is designed to be compatible with ECSI Fibrotools

(ElectroChemical Systems, Inc.). From the experience gathered in the first wafer holder design, issues resolved in next tools.

3D model of the designed and manufactured holder is illustrated in Figure 2.19, showing all the necessary details. It has top and bottom parts. Each part has one ISO standard O-ring for electrode isolation purpose from the electrolyte. Channels are created for inserting them in designated location. Outer O-ring in bottom part has a diameter slightly greater than 6" and cross section of 3.53 mm that can seal electrode and the seed layer when squeezed between up and bottom parts. Other O-ring in top part has diameter slightly smaller than 4" to make sure it touches the TSV wafer edge. Leakage to electrode or the seed layer causes unstable current readings and undesired deposition on electrodes during process. In addition, deposition between holder electrodes and the wafer seed layer can cause an unwanted bonding that may lead to breaking of wafer while its separation.

For the electrical connection, top part has electrode channel that has connection to the handle via little hole to the channel from the other side. Electrode ring fabricated from a copper sheet by laser cut according to the channel dimensions. Electrode channel is positioned to align with the TSV wafer as close as possible and maintain contact to the carrier seed layer. Soldered contact pins on the electrode ring maintain uniform current distribution on the seed layer along the carrier wafer. Pins are made from flexible and gold coated electrodes that are able to retract when the holder clamps the wafer tight between its two parts. Also, when they are closed, electrode channel stays between the two electrodes. This way, electrical connection from the handle of the holder through the carrier wafer seed layer and the electrolyte to the anode is able to be established without electrolyte leaking to the electrode.

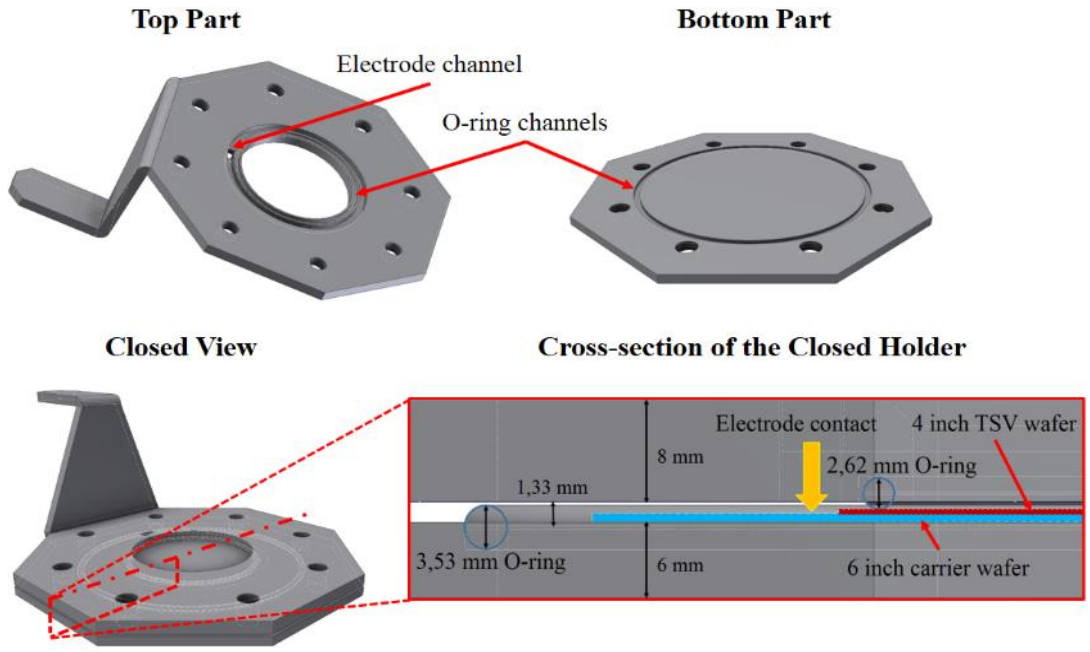

Figure 2.19. Design of electroplating wafer holder for carrier wafer process showing its top part, bottom part and their closed view with cross sectional cut view with wafers, electrode and O-ring placements.

2.3.3.2. Direct Current Source

In order to observe the effect of the current timing on filling process, electroplating experiments started with the DC current source. This is done by only enabling the ON time of the pulse current supply.

First experiment is conducted with the direct current source mode selected and highest current value allowed from the electroplating solution that is 53.8 mA/cm^2. Carrier and the TSV wafers placed and aligned inside the wafer holder as in Figure 2.20. Within an hour of process, at some TSVs, protrusions are observed while rest has some filling or no filling (Figure 2.21). Nonuniformity was significantly high along the wafer. Protrusions were empty from the inside, because the deposition was following the fastest way as the TSV sidewalls while leaving the core unfilled.

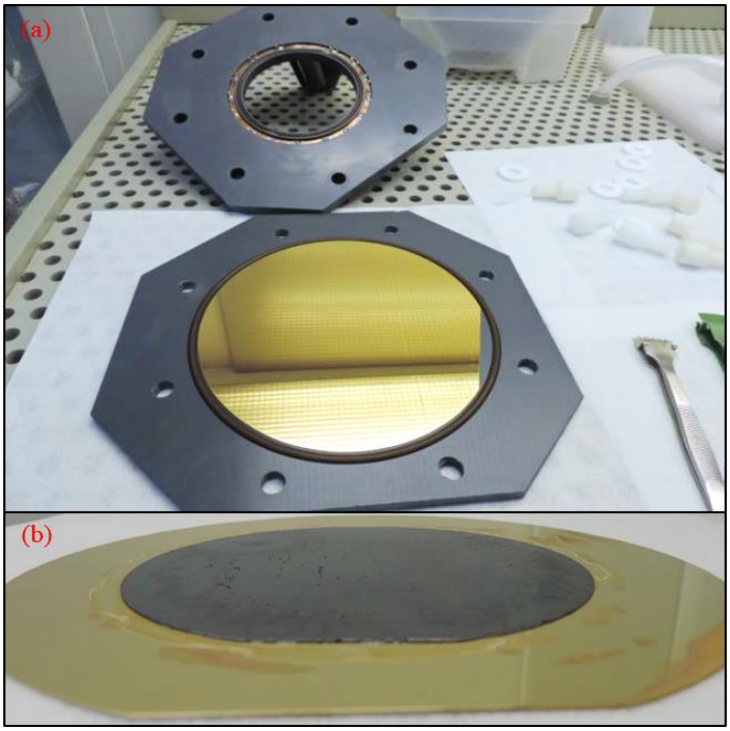

Figure 2.20. (a) before plating carrier wafer placement into the holder, (b) after the plating process with the applied DC.

In Figure 2.21, backside images are taken from the TSV wafer after separeation from the carrier wafer. Also, the situation on the seed layer is observed with SEM analysis showed that some of the TSVs were empty because the Cu pillars filling them were left on the seed layer. As shown in Figure 2.22, deposited copper pillars are in porous structure because of the fast process and the applied direct current. In addition, it is observed that the deposit copper tries to go upward without creating agglomerations away from the through holes but only near region around the pillars. Cu pillars are mostly found near the edge regios. It indicates that the force applied by the holder O-rings helped to seal them better than the central TSVs and promoted upward growth while in other TSVs lateral growth was delayingthe TSV filling.

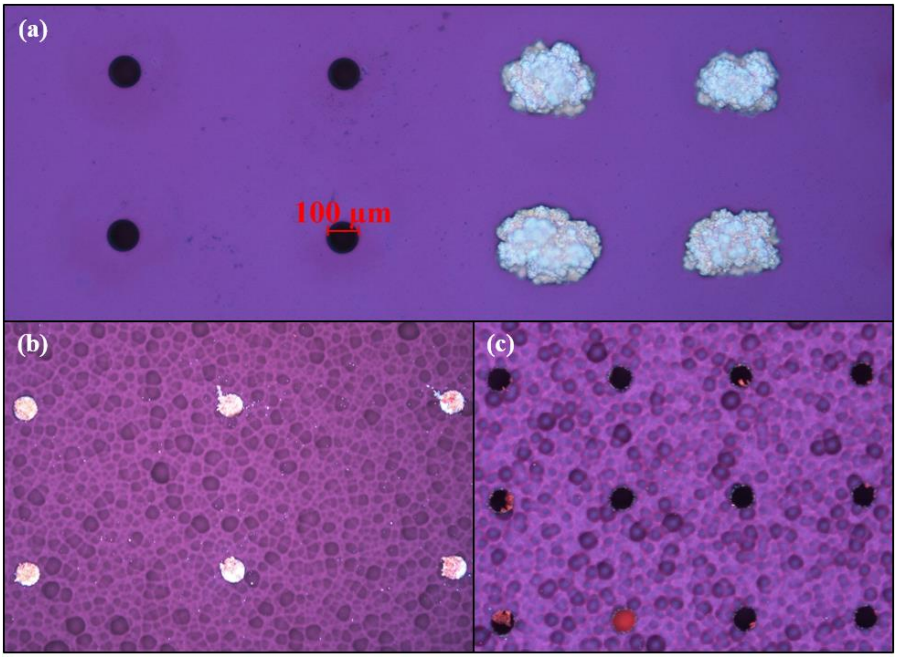

Figure 2.21. First carrier wafer electroplating experiment, (a) front side protrusions, half- filled and unfilled TSVs, (b) backside deposits after separated and (c) deposited particles on sidewalls.

In the second experiment with the direct current source, average of 23.5 mA/cm^2 is applied in 4 hours of electroplating process. This time some of the TSVs on center region are also filled and porosity of the deposit copper was reduced, but previous problems are continued. Similar result is obtained with the first experiment, deposition is triying to proceed from the sidewalls of TSV only. Hollow deposits are shown in Figure 2.23. Thus it was concluded that it is not possible for this setup to be able fill TSVs in desired void free manner with the direct current. Experiments continued with using pulse current source.

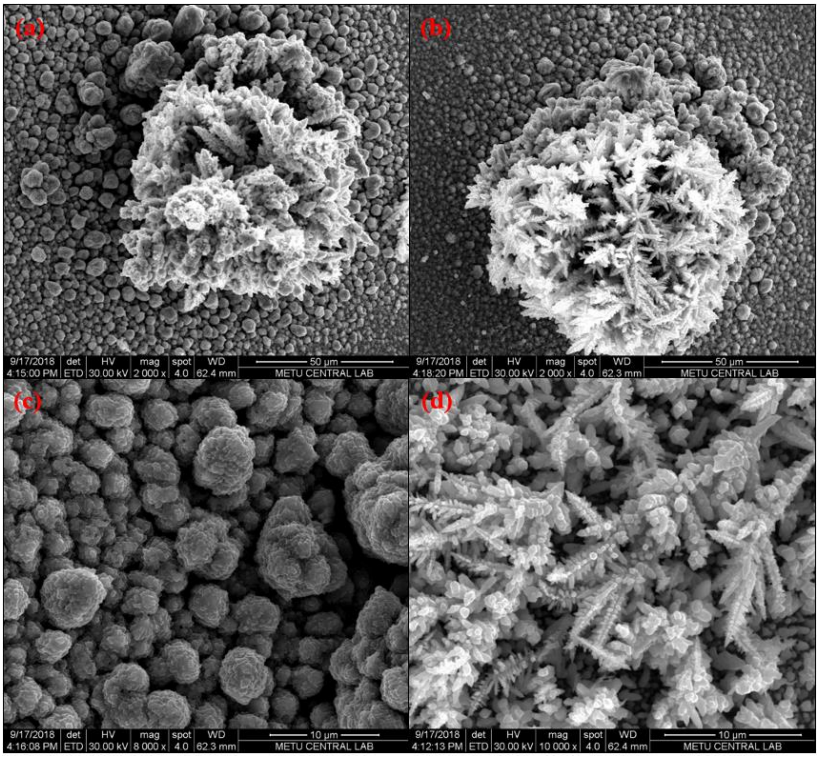

Figure 2.22. First carrier wafer method result that are analyzed with SEM, (a) and (b) Cu pillars, (c) and (d) Close-up observation of the pillar above them.

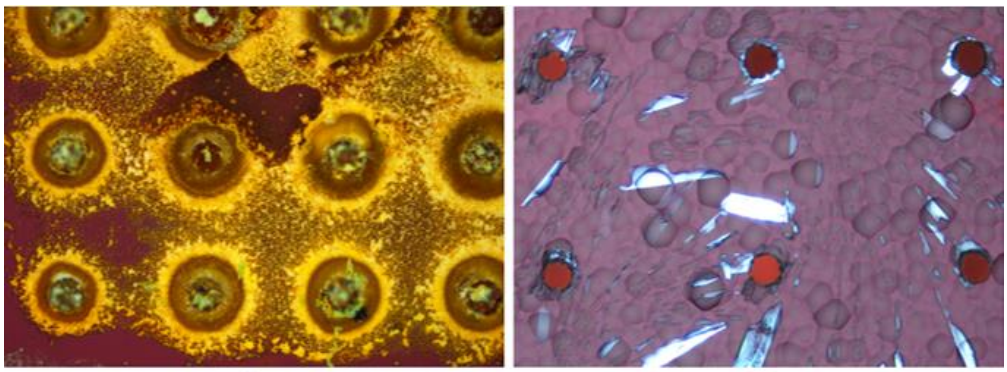

Figure 2.23. Second direct current source experiment in carrier wafer method, (a) Deposits on carrier wafer surface, (b) Partially filled TSVs.

2.3.3.3. Pulse Current Source

Using the pulse power supply, ON and OFF timings are adjusted as shown in Table 2.1. Experiment number 3, 4 and 5 are conducted with the pulse current source. There

were no additives introduced. Calculated total seed layer that is exposed to electrolyte solution was 0.8 cm^2. Process time of the experiments were varying between 90 minutes to 120 minutes.

Table 2.1. *Experiments conducted in carrier wafer method.*

Experiment Number	**1**	**2**	**3**	**4**	**5**	**6**
Set current (mA)	53.8	23.5	52.0	40.5	520	40,.5
ON time (ms)	all	all	0.1	0,.7	0.5	4.5
OFF time (ms)	-	-	0.9	0.3	1.5	1.5
Duty cycle	-	-	0.10	0.7	0.25	0.75
Frequency (Hz)	-	-	1000.0	1000.0	500.0	166.7

In these experiments, by keeping the other parameters fixed, ON and OFF pulse timings were altered. Pulse timing that can give solid and hollow free Cu pillars were tried to be obtained while filling the TSVs. Within the limits of the supply, minimum OFF timing of 0,1ms and 0,1 duty cycle parameters are selected in the beginning. In the experiment #3, the bottom-up filling could not be observed inside TSV. Deposition was in lateral direction along the carrier wafer and TSV wafer interface only. In the experiments #3 to #6, duty cycle is increased by rising ON time and frequency reduced by the increased total pulse width. This eventually showed to be the right modification for the electroplating setup to give the desired result. As shown in Figure 2.24, deposits on the carrier wafer after the separation are in solid shape and shadowed the TSV wafer accurately. Also, their separation became harder as deposition started filling TSVs and creating kind of a bonding between two wafers. In experiment #6, the hollow Cu pillar structures are filled from the inside compared to the pillar from the experiment #5 where they have still hollows.

According to the obtained trend, increasing the duty cycle in our electroplating setup for the TSVs in aspect ratio of 4 to 3.5 is giving better filling inside TSVs. Lateral

filling between two wafers reduced and bottom-up filling started to dominate. Electroplating with pulse current is proved to yield in stronger and hollow free deposits compared to direct current source. At this point, experiments with carrier wafer method stopped as we need temporary bonding process for further improvement. Couple of trials for the temporary bonding showed that it would need more number of iterations than anticipated. Never the less, using this method, being able to observe the deposits directly after the process allowed us to experience the process setup and obtain valuable information in a short time. Bottom-up TSV filling process experiments are continued with via sealing method.

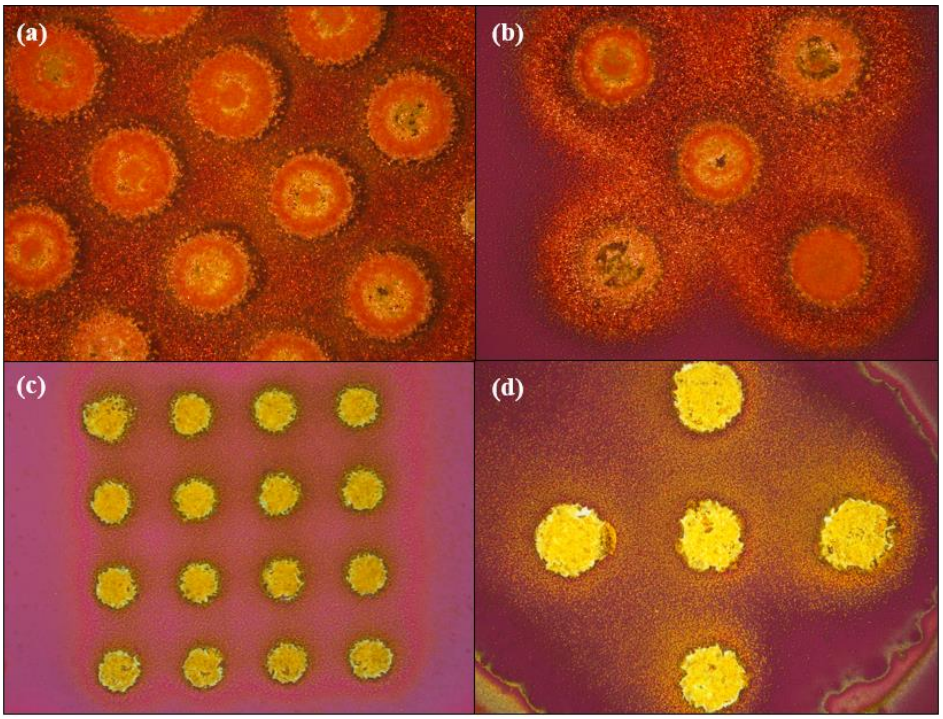

Figure 2.24. Carrier wafer pulse current experiments, (a) and (b) Experiment #5, (c) and (d) Pulse current experiment #6.

2.3.4. Via Sealing Method

Ready to fill TSV wafers are prepared for this process. In wafer level TSV fabrication process, 550 µm thick, silicon wafer with (100) crystal plane go through the thinning process. Down to 350 µm thickness is obtained in deep reactive ion etching (DRIE)

system with 13µm/min etching speed. On wafer front side, thin 0.5 µm PECVD SiO_2 layer is deposited prior to thinning for protecting the wafer edges and front side surface from the etch plasma. Thinning applied to the backside not to modify the polished front surface since backside is not polished. Then, backside surface is 0.5 µm PECVD SiO_2 coated for the through etch process. Main portion of the developed TSV fabrication flow is shown in Figure 2.25, described in six main steps from (a) to (f).

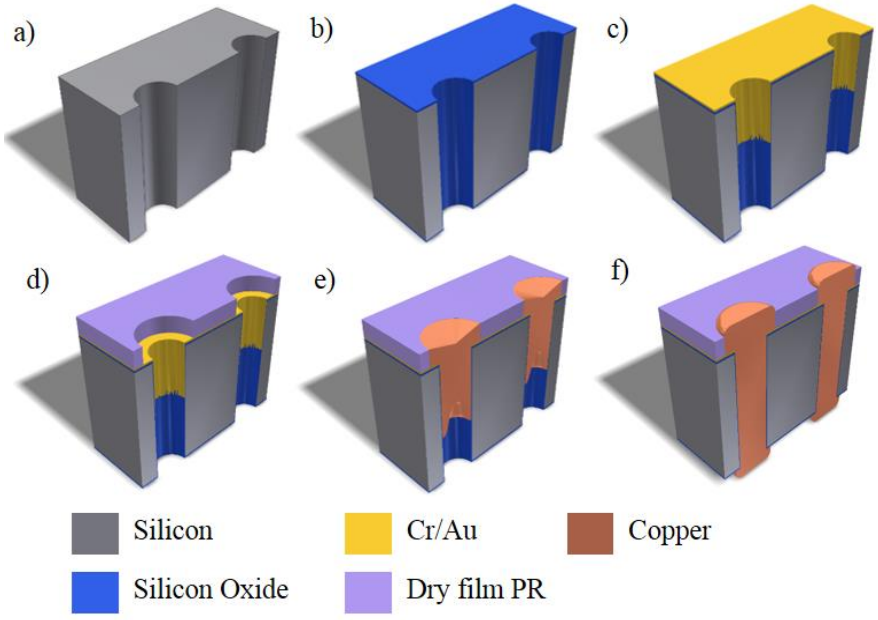

Figure 2.25. Via sealing and bottom-up electroplating process flow in six steps.

PRS 220-3 photoresist is spin coated on silicon oxide surface of thinned wafer at 3000 rpm. Mask layer thickness of 3.2 µm is obtained. Next, patterned with DRIE mask for SiO_2 etching in reactive ion etching (RIE). Then, through via structures are etched inside silicon substrate using Bosch Process in DRIE. Diameter of 100 µm TSV structures with 350 µm depth are formed. SiO_2 film on backside prevents etch plasma damaging the backside surface and acts as an etch stop layer (a).

In the next step, 1 µm PECVD SiO_2 layer as electrical isolation function is deposited from both front and backside of the wafer to establish film that is as conformal as possible. As the deposited depth increases, film thickness on the TSV sidewalls

decreases [30]. Thus, deposition from both sides provides more uniform film thickness along the sidewalls. Recipe of SiH4 and N2O based mixture with N_2 is used at 300 °C process temperature (b).

Adhesion layer of 30 nm Cr deposition prior to 500 nm Au seed layer is carried out with magnetron sputtering system (AJA International Inc.). Depth of the continuous deposition layer can reach up to 160 µm in our configuration on sidewall of 100 µm diameter holes (c).

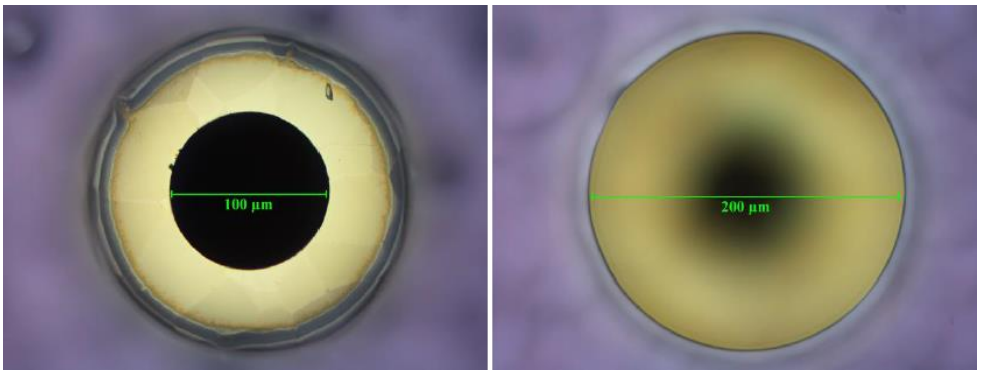

Figure 2.26. Film photoresist coated TSV opening, objective focused on see layer surface and focused on boundary of the photoresist edge from left to right respectively.

Electroplating process compatible, 50 µm thick dry film photoresist (Laminar-E9220) is manual laminated. Membrane like polymer film is obtained on via openings before the development. Possible air bubbles stuck between wafer and the film are able to escape thanks to the through etched via during the lamination. Film adheres to the surface after the short soft bake applied on hotplate. Successful patterning is obtained with the MF-24A solution that is TMAH based photoresist developer. 4,5 seconds exposure in the alignment step and 65 seconds in the development are applied. In Figure 2.26, openings with 100 µm radius are formed around the TSVs. This layer works as a masking for the seed layer where deposition is not desired. Also, it functions as a mold for the TSV bumps during the via sealing electroplating (d).

Using regular topside contact electroplating holder, via sealing step carried out. This is the first part of the two-step bottom-up filling technique. Pulse current supply with

different duty cycles are used in experiments. It takes longer to seal up via openings than fill them in bottom-up step. Commercial sulfuric acid based Cu solution (Transene) is used for the base. Although sealing can be realized without them, additives are introduced later (e).

In the second step of the TSV copper filling process, wafer is turned upside down and installed into the bottom-up electroplating holder, which is described in Figure 2.27. Remaining part of the TSV is filled. Electroplating process with and without additives are carried out as explained in the following sections in detail (f).

When the TSV copper filling process is finished, film photoresist is removed with MF-24A solution, as it is a negative type of photoresist. In the rest of the fabrication, depositing conformal Cr/Au layer and its patterning on front and backside surfaces is carried out to create connections between TSVs.

2.3.4.1. ECD Wafer Holder Design for Bottom-up Process

This tool is designed and manufactured together with the carrier wafer holder. For the same purpose, that is to have contact from the seed layer while preventing the electrolyte solution to leakage holder electrodes and seed layer. It is also compatible with the same electroplating system. Only difference is that, this time it provides contact from the backside of the wafer directly while wafer surface facing the solution is considered as front side. As it is demonstrated in Figure 2.27, it consists of two main parts as upper and bottom part. Upper part has one O-ring in contact with the wafer surface from the edge. Bottom part has two O-rings one for sealing from the outside of the wafer edge in contact with the top part and one for inside in contact with the wafer edge. In the bottom part, electrode ring is embedded between two O-rings. It has connection from handle to the bottom of the holder. Electrode ring has retractable tiny electrodes that are gold coated against corrosion and welded to the electrode ring. When the wafer squeezed between two main parts, flexible electrodes in contact with the seed layer retract without breaking the wafer. When the processed wafer is removed, flexible electrodes go back to their default position as desired. Electrodes

located on the ring are evenly distributed to maintain uniform current distribution along the wafer.

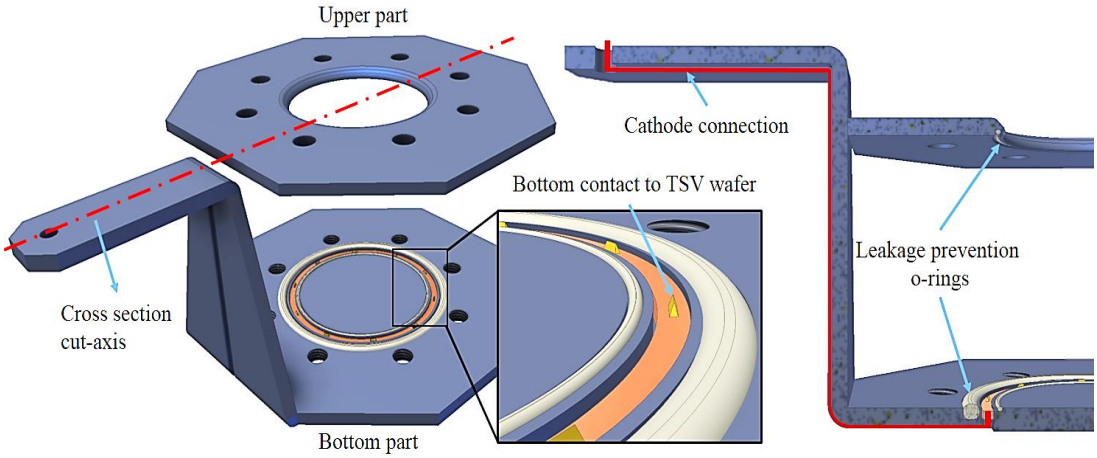

Figure 2.27. Electroplating wafer holder for bottom-up TSV filling process.

2.3.4.2. ECD with Base Cu Solution

In this part of the study, first objective was to find a pulse scheme of the current that can be used to seal the TSV openings during the ECD. Different pulse timings and frequencies are experimented. Following this step, bottom-up filling is experimented using the sealed via openings as seed layer.

Via sealing method is started with the additive-free copper electroplating solution (Transene). According to the experiments carried out in the carrier wafer method, frequency of the pulse is further reduced. Process time depends on the observed deposits and determined by the microscope observations between each hour of process. Parameters of the applied current source are listed in Table 2.2 according to the experiment number. In the first experiment, six hours of process with 8 ms ON time and 2 ms OFF time result in still unsealed via openings for the most of the wafer. Following this trial, pulse frequency is reduced to 10 Hz from 100 Hz. Pulse timing with 80 ms ON time, 20 ms OFF time is used. In the experiment #2, sealing finished in 3 hours using 32,5 mA/cm^2 current and subsequent bottom-up filling step took 3,5

hours with reduced current amplitude of 28,5 mA/cm^2. In the experiment #3, frequency of the current pulse is increased to 20 Hz by reducing ON/OFF times to half. However, this result in wafer level nonuniformity, where some of the TSVs are sealed while some of them are filled completely and some could not be sealed after 6 hours of process. Thus, current pulse scheme is determined to be used as in the experiment #2 in the next TSV wafer fabrication cycles.

After the via sealing and bottom-up filling process, wafers are diced to observe TSVs from the cross section. Result of experiment #3 is shown in Figure 2.28. Along the wafer, even the neighboring TSVs have different filling profile. Even though, this was only sealing step and only the closing of the via openings was expected, some TSV filled through their depth with voids inside.

Table 2.2. *Via sealing experiments.*

	No Additive			**Additives**	
Experiment Number	**1**	**2**	**3**	**4**	**5**
Set current density at sealing (mA/cm^2)	35.5	32.5	32.7	32.4	33.0
Set current density at bottom-up (mA/cm^2)	-	28.5	-	-	24
ON time (ms)	8.0	80,0	400	80.0	80.0
OFF time (ms)	2.0	20.0	10.0	20.0	20.0
Duty cycle	0.8	0.8	0.8	0.8	0.8
Frequency (Hz)	100.0	10.0	20.0	10.0	10.0

From the experiment #2 SEM analysis as seen in Figure 2.29, better results are obtained in terms of TSV filling performance and wafer level uniformity of the filling profiles in comparison to other trials. In center regions, smaller voids are observed in TSV cross sections compared to the TSVs from the wafer edge. Although most of the TSVs have voids inside them, void-free TSVs are obtained as well. In between the center and the edge regions, voids started to get bigger. From the samples in edge

region, larger voids are observed. In Figure 2.30, TSV cross sections with huge V-shaped void and void-free filling profiles are juxtaposed for comparison.

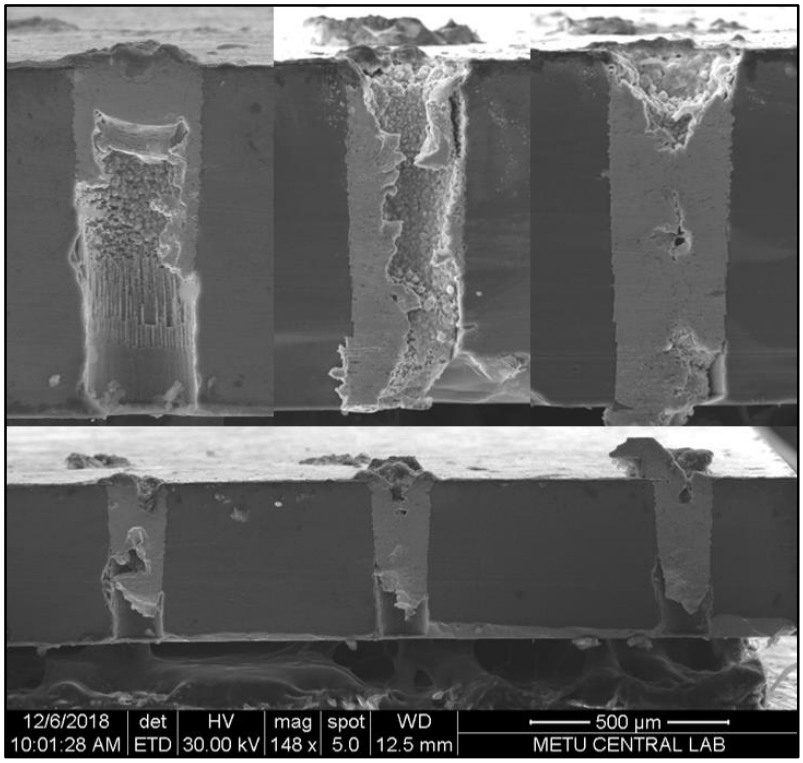

Figure 2.28. Via sealing electroplating experiment #3, SEM observations.

In Figure 2.30a, highlighted V-shape void structure is shown that is observed in most of the TSVs from the wafer edge region. It can be concluded that, since seed layer deposited surface continues on the TSV walls at least 160 µm deep, during the sealing bump ECD process, growth starts inside the TSV on sidewall seed layer. It forms the deposit reaching until the highlighted V-shaped line before the sealing finished. When bottom-up ECD step proceeded, process starts from the deposits on the TSV walls and then seal up at the certain level leaving a closed void behind. Bottom-up step continues along the rest of the TSV depth until the backside surface as it is the upper side during the process. In Figure 2.30b, image on the right side shows the desired void-free TSV filling.

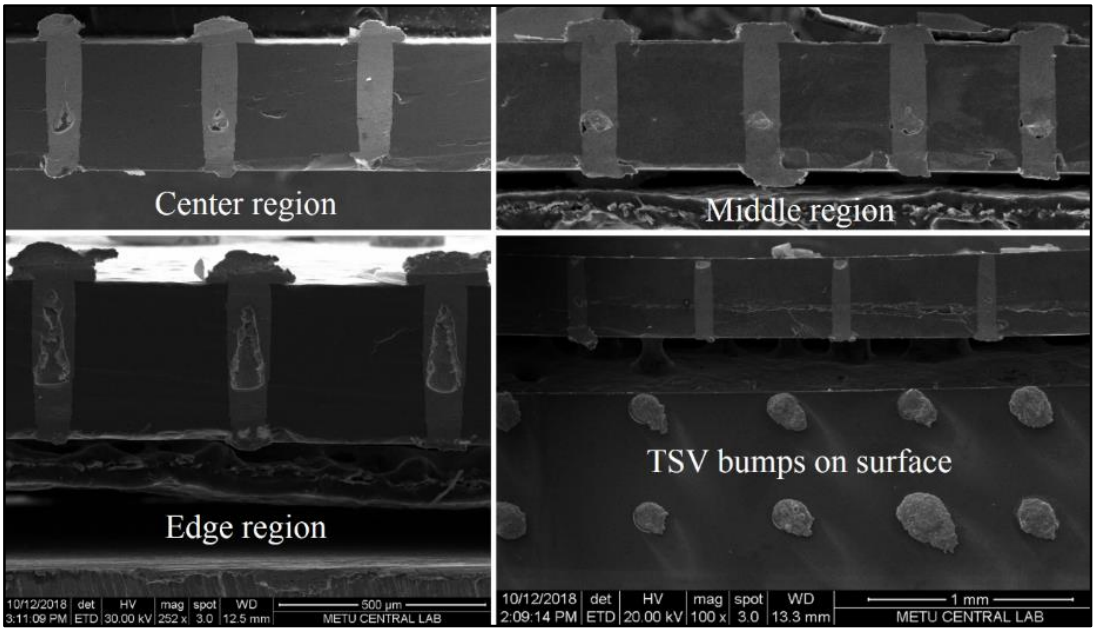

Figure 2.29. Via sealing and bottom-up electroplating experiment #2, SEM observations by location on the wafer.

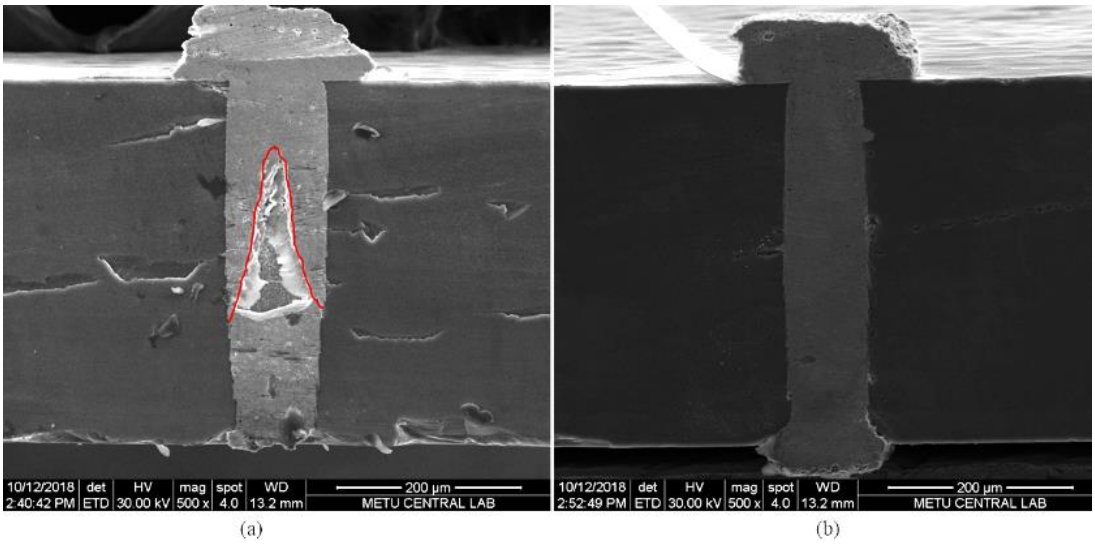

Figure 2.30. TSV cross sections of experiment number 2, a) wafer edge region having filling profile with V-shaped void, b) void free TSV from the center region.

2.3.4.3. ECD with Additives

Wafer level uniformity without additives could not be obtained. Void free TSVs on center region are obtained, however, TSVs at surrounding region have voids. In

addition, formation of the TSV bumps shape are rough and their height differ along the wafer. Thus, electroplating with additives is experimented to resolve these issues. Current pulse scheme is used as 0.8 duty cycle with 10 Hz as in the previous best filling achieved. After couple of trials, it proved to be successful at providing wafer level uniformity. This part of the experiment is irreversible since once an additive is added, it cannot be removed from the copper electroplating solution. Therefore, a literature review is done to observe and get some insight on the matter.

Table 2.3. *Some bottom-up copper electroplating studies with additives for TSV filling*

Ref.	Copper Ion (g/l)	Acid (g/l)	Cl (ppm)	Leveler (ml/l)	Suppressor (ml/l)	Accelerator (ml/l)	AR
[28]	112	50	70	3	10	6	2.0
[29]	110	15	100	3	8	3	2.6
[30]	80	20	50	7	5	5	3.3
[29]	110	15	50	6	10	3	5.0
[31]	110	12	50	8	10	3	6.6
[32]	200	25	70	0-4	25	2	7.0
[33]	200	25	70	10	25	2	8.0

Related studies are listed in Table 2.3 according to increasing aspect ratio of the TSV filled. Mainly, as the AR increases, suppressor and leveler ratios increase while accelerator ratio decreases. This may be due to the requirement to overcome premature closure of the via opening.

From the above table, the AR 3,3 is the most relevant among them. Initially, only 3ml/l leveler was added to increase wafer level uniformity in experiment #4. Current set to 32,4 mA/cm^2 during 5 hours of process. However, it promoted the diverse filling profiles along the wafer in the absence of other additives as their cross sections are observed from the SEM analysis shown in Figure 2.31. Close-up view of the filling profiles were arranged from least filled to the most as if they are showing the progress of the electroplating incrementally, even though they are coming from the same process as their sample level view shown underneath them. Completely filled and void free TSVs are obtained together with the others as seen in Figure 2.32, although this trial not continued with bottom-up step. In the SEM images there is 50 µm thick film

PR layer between the TSV openings on the seed layer for and the 350 µm wafer thickness.

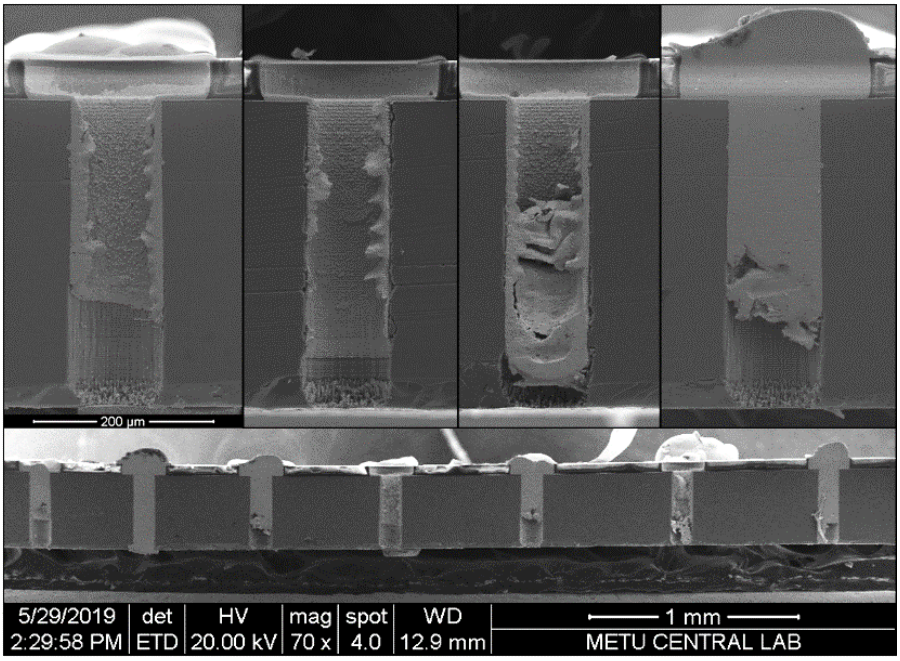

Figure 2.31. Via sealing process experiment #4, SEM analysis of single TSV and die level TSVs showing resulted irregular filling.

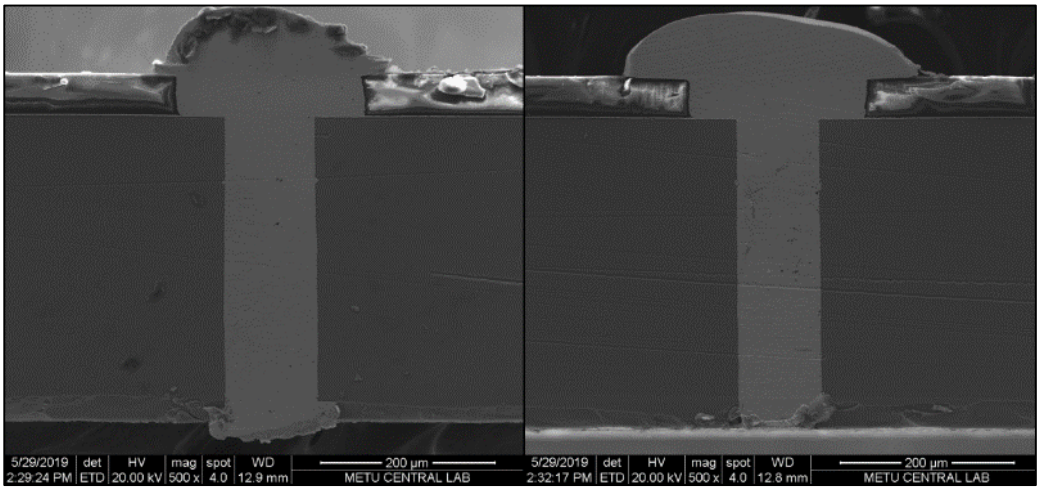

Figure 2.32. Via sealing process, experiment #4 SEM analysis of filled TSVs.

In the second trial with additives in experiment #5, suppressor and accelerator are also included in both 1 ml/l ratio. Via sealing step is performed with 33 mA/cm^2 applied

for 3,5 hours. Cone shaped TSV bumps are obtained. Comparison of the two via sealing experiments #4 and #5 from the top view of TSV bumps are shown in Figure 2.33. Following bottom-up step takes 2 hours. In the all TSV filling experiments performed, the best wafer level uniformity is obtained from this solution configuration as all TSVs are fabricated void free with very similar bumps height and shape as seen in Figure 2.34.

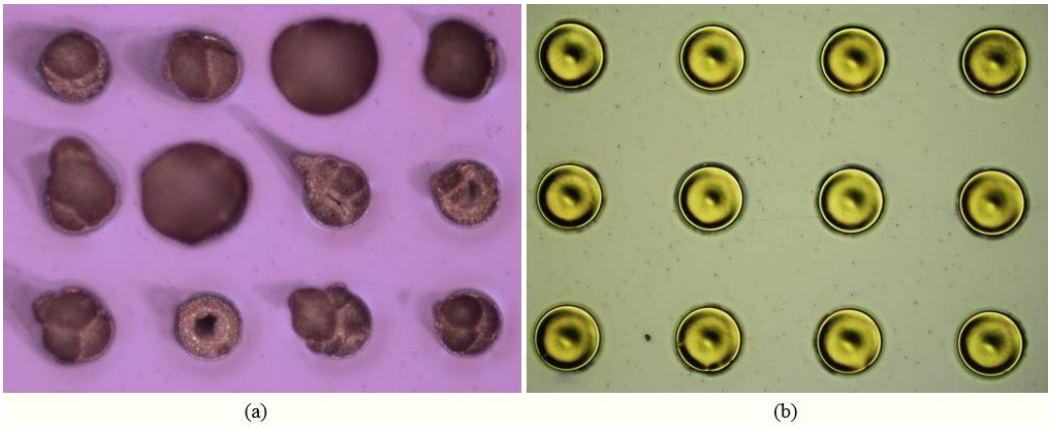

Figure 2.33. Via sealing microscope observation, a) only 3ml/l leveler, b) added suppressor and accelerator in 1ml/l ratio.

After the experiment #5, wafer is diced to obtain samples from three different regions on the wafer as edge, middle and center. Samples are observe the cross sections with SEM in the Figure 2.35. Wafer level uniformity confirmed with this analysis and further microscope observations. For the obtained TSV bump shapes on front side of the wafer, in the experiment #4 convex bumps became concave in the experiment #5.

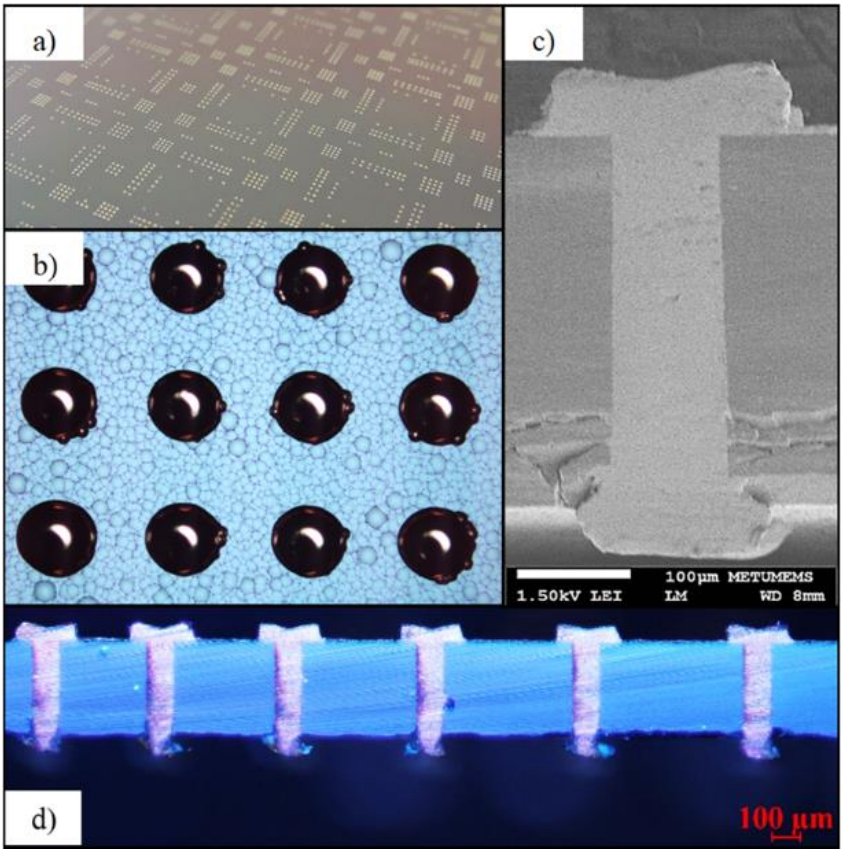

Figure 2.34. Via sealing and bottom-up process experiment #5, a) front side wafer level perspective of sealed TSVs, b) TSV bumps at backside, c) SEM image of a cross section, d) microscope image of void free TSVs.

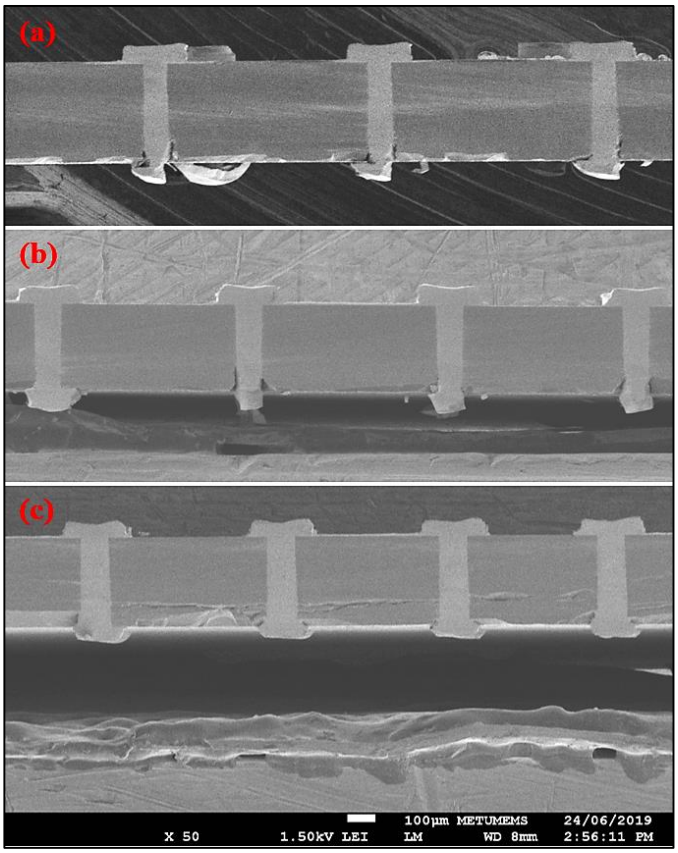

Figure 2.35. SEM analysis of the samples from a) edge, b) middle, c) center regions of the via sealing and bottom-up electroplating with all additives.

2.4. Lapping Process

When TSV integration is preferred to be in via first approach, flat surface is desired for the subsequent process steps to be performed. Most importantly, photolithography quality and resolution depends on flatness of the surface, even though rough structures can be patterned with spray photoresist. For this reason, the wafer from the via sealing experiment #2 is taken to lapping process. Lapping step is performed intentionally before the bottom-up filling step to have the backside surface of the wafer flat during the process. Since it is crucial to temporarily bond the wafer to the lapping chuck and fixing the wafer in a little tilted way can cause it to break or uneven levelling along the wafer. Crystal bond, a polymer that is easily melting above 65 °C temperature is applied on backside of the wafer. Then, wafer is bonded to a Teflon piece for the

lapping chuck using a bonding tool with pressure piston. Lapping process is applied for an hour till it stops thinning down further. Lapping chuck rotation speed is set to a value between 105 and 120 rpm during the process. After the wafer released with applied heat on the hot plate, cleaning processes continued. It is crucial to get rid of all crystal bond on the surface and inside the via holes. Results can be seen in Figure 2.36 as an array of TSV bumps on the left and a single one on the right as close-up view showing 200 µm bump diameter. Along the wafer, all TSV bumps are flattened but 28 µm difference is measured in their height since some of the TSVs had deposits till the backside surface that was supposed to be flat. Experiment #5 overcome this difference uniformity of bumps height on the surface.

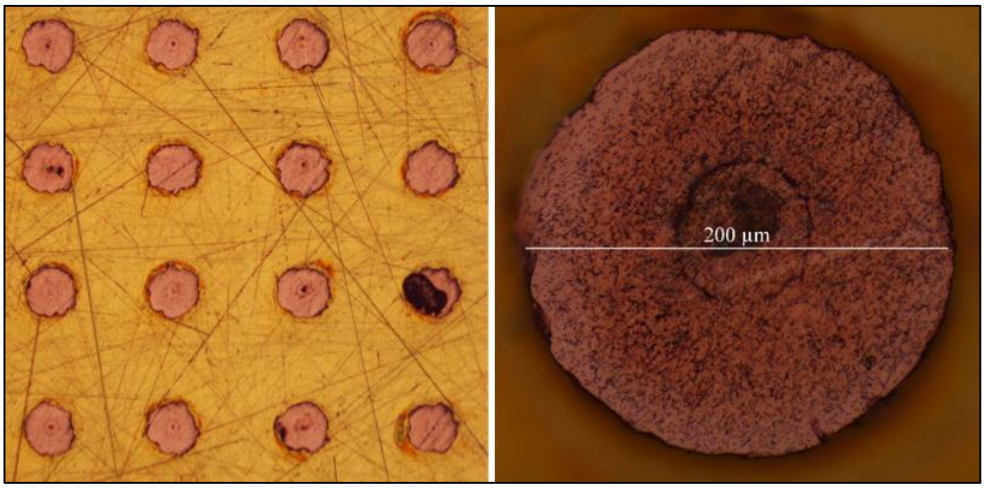

Figure 2.36. Lapping result of the wafer from the experiment via sealing and bottom-up #2.

2.5. TSV Connection Patterning

After the lapping step, TSV connections are created by double side metal patterning process. First, Cr/au layers are sputter deposited on front and backside surfaces. Then, spray photoresist, is used to coat 7 – 8 µm polymer layer on processed side. Other side of the wafer is coated with spray photoresist to protect unwanted etching as well prior to the processed side. It consists of S-1813 photoresist that is diluted with Acetone. Next, photolithography process is carried out with 50 seconds exposure prior to a short soft bake. Then, 2 minutes of development process with MF-24A solution is done.

Lastly, patterned mask is used in Cr/Au etching process. Gold etching step takes 3:45 minutes for 500µm layer using Transene solution. Next, 40 seconds Ti etching is carried out with prepared solution of HF and H_2O_2 and deionized water. All of these steps are repeated for backside of the wafer as well. Front side of the wafer with variety of TSV routings after metal patterning is available in

Figure 2.37. Test structures are fabricated by connecting three TSVs for the four-point Kelvin measurement as shown on the close-up view on the right.

Figure 2.37. Front side of the wafer after Cr/Au patterning as wafer level and the close-up view from left to right.

Functionality of the spray photoresist in terms of step coverage is analyzed by tilting the wafer up against the microscope objective. As seen in Figure 2.38, side walls of the bumps are coated with gold layer. This means the etchant could not leak through the photoresist at its weakest possible point as vertical walls.

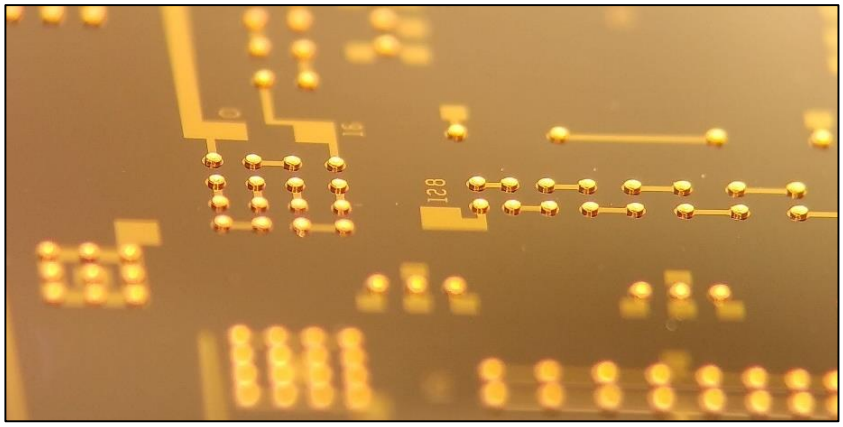

Figure 2.38. Tilted wafer level view observing the TSV bumps after the Cr/Au patterning.

2.6. Chip Frame with TSV

In order to test the TSV on application with the transducers as feasibility experiment, fabrication of the frames is required with TSV that are compatible to 3D integration on transducer chips. When the fabrication of the wafer with TSV is finished, test structures are created in double side metal patterning process and wafer is taken to the characterization phase as explained in Four-Point Kelvin Measurement section. Once

it is completed, process continues on the wafer as it is taken to the chip frame formation phase.

In this step, front side of the wafer is coated with spray photoresist as in the TSV connection creation step. Layer is patterned with the frame formation mask of the transducers by aligning it to the marks of the TSV mask. As the whole wafer has 1 µm thick silicon oxide coating, RIE process is applied for the patterning of the layer only on the front side. If BHF is used in this step, backside surface of the wafer has to be protected against unwanted oxide etch. Following DRIE process etched the silicon through the backside surface and chip frames with TSV identical to the transducer chips are fabricated. Through etching process takes 13 minutes in 1 minute process steps to reach 350 µm depth without damaging the mask layers and the TSVs.

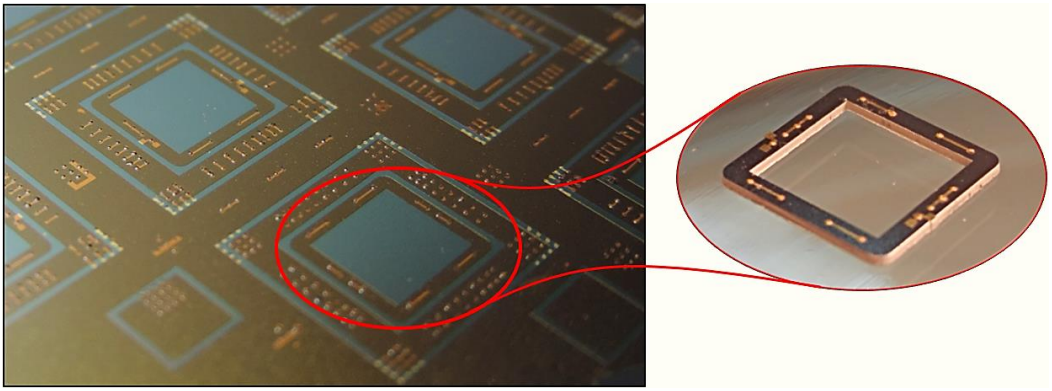

Figure 2.39. Process wafer for the chip frame separation and the frame with TSV after process.

CHAPTER 3

FLEXIBLE SUBSTRATE FABRICATION AND 3D INTEGRATION OF MEMS RESONATORS

In this chapter, designing stage and fabrication flow optimization of the substrate for 3D integration of the MEMS resonating devices is explained. The substrate that provides electrical connections should be flexible to make it possible to place the transducers on the eardrum/ossicles easy during the surgical operation. As this is an in-vivo device that needs to implanted, it should be biocompatible. In addition, it should establish packaging of the transducers once they are integrated. Hence, a flexible, biocompatible and robust substrate is required. In the FLAMENCO Project proposal, first designs were made as its conceptual drawing of the package and the interconnects presented in Figure 3.1. This package composes of a stack of the piezoelectric transducer chips placed on a flexible substrate, and they are connected to the CMOS IC chip.

The idea of the transducer stack with multiple chip, each having couple of cantilevers is abandoned by studies of Bedirhan İlik [37] before this study is carried out. Instead of multiple chip stack, transducer chip having all eight of the cantilevers on a single chip is designed and it was manufactured [8]. And the number of total chip was reduced to two as in the model shown in Figure 3.2.

In addition, in the first proposal of the project, wire bonding is planned to provide the interconnections between chips and the flexible substrate. Later it was found that it is not applicable to establish wire bonds on an electrode pad when the substrate is flexible. Even if the contacts are formed, many researchers in our group have experienced that they are prone to vibration and they might peel off easily during testing. Further, during the wire bonding, flexible polymer used as the electrical

isolation layer gets punctured and short circuit can occur between two distinct metal layers. This brings reliability concerns that needed to be resolved with robust interconnection strategies that are proposed in this study.

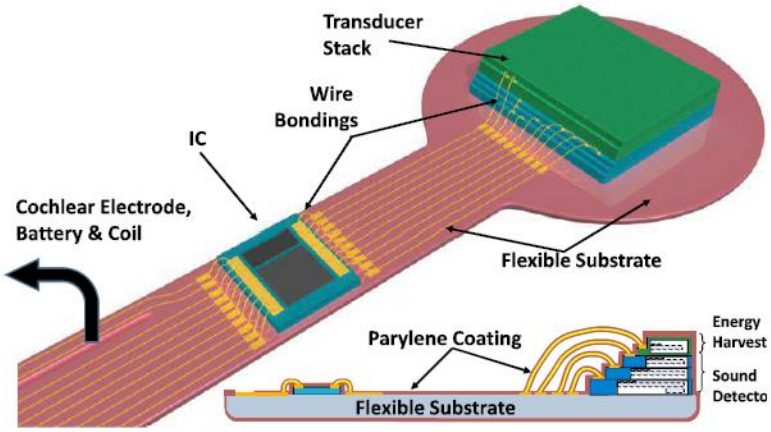

Figure 3.1. Proposed packaging and interconnections concept of the transducers and IC on flexible substrate from FLAMENCO Project Proposal.

3.1. Literature Review on Flexible Substrates in Bioelectronics

Use of conventional flat and rigid assembled PCBs in some applications regarding bioelectronics technology becomes problematic. Applications such as sports and leisure devices, smart textiles or biomedical implants demand comfortable integration of the electronic circuit on an irregular surface where there is not enough flat space. Hence, in most cases, wearable and implantable circuits need flexible substrate assemblies. Thus, the circuit can follow the rather random outline and shapes of the part onto or into where the circuit is integrated depending on the application. Some of the biomedical applications can be given as bladder monitoring system [38], the retina implant as bionic eye [39], neural recording systems [40] and wearable or in-vivo cardiovascular monitoring devices [41], [42] as examples.

In the literature, flexible substrate integrations to overcome rigid to flexible transition were managed by forming the metal lines inside the polymer substrate and leaving openings for the rigid chip to get electrical connections by flip-chip bonding. Wireless power transfer device is fabricated by integrating antenna and the CMOS rectifier chip

on parylene flexible substrate and final conformal coating of parylene for biocompatibility [43]. Polyimide is also used as the flexible the substrate for the intracranial pressure (ICP) microsystem sensor biocompatible packaging integration with ZIF connector for brain monitoring device [44]. This kind of flexible substrates which connects rigid components on one side and ZIF connector at the other are generally called as flat flexible cable (FFC). Further, PDMS coated printed circuit board as stretchable circuits is fabricated by injection-molding method after fabricating the metal connections on a sacrificial layer. In order not to damage the polymer layer, they chose this process order [45]. In addition, diverse flexible electronics solutions are proposed where a silver ink composed of Ag nanoparticles is developed for flexible microelectrode printing purpose [46] and transparent nanowire transistors fabricated on flexible plastic [47].

3.2. Proposed Flexible Substrate Design

For designing the applicable solution, fabrication has to be planned beforehand. To describe the overall fabrication procedure adopted in this study, a flexible material is utilized as the substrate, which carries the metal lines and pads for interconnect electrodes. The polymer is deposited on a wafer and it is coated with metal films. Both the metal film and the sheet can be patterned by photolithography and following etching steps forming the flexible substrate and interconnects. Transducer chips can be 3D integrated prior to bonding on substrate or can be bonded separately on the substrate then bonded together. Flexible substrate is released from the process wafer after the transducers are bonded or prior to the bonding depending on the procedure. First generation of the similar flexible substrate was designed and fabricated by Aziz Koyuncuoğlu [8].

Mainly, two different integration methods are designed for the 3D integration of MEMS transducer on a flexible substrate. They vary depending on how the connections are taken from the package. As it can be either from the one side of the package or from the both top and bottom side of the package.

In the first option, flexible substrate is designed for the use of TSV where one of the chip in contact with the flexible substrate can transfer the other chips signals through the TSV. Thus, only one place designated for the chip placement is available since two chips are 3D integrated prior to the placement on the substrate. This method is called as 'front-to-back integration' of the transducers and connection from the package is maintained from one side using single head type of flexible substrate.

In the other option, there is two places designated for the chip placement on a single flexible substrate similar to two branches of the same tree. As both chips are directly in contact with the flexile substrate from the front side, there is no TSV integration needed. When the chips are bonded to their places from the front side surface, they are bonded from their backside by turning one of the branch of the substrate onto the other one they are integrated in 3D manner. Thus, this method is named as 'back-to-back integration' of the transducers and connections are provided from both top and the bottom sides of the package using twin type of flexible substrate.

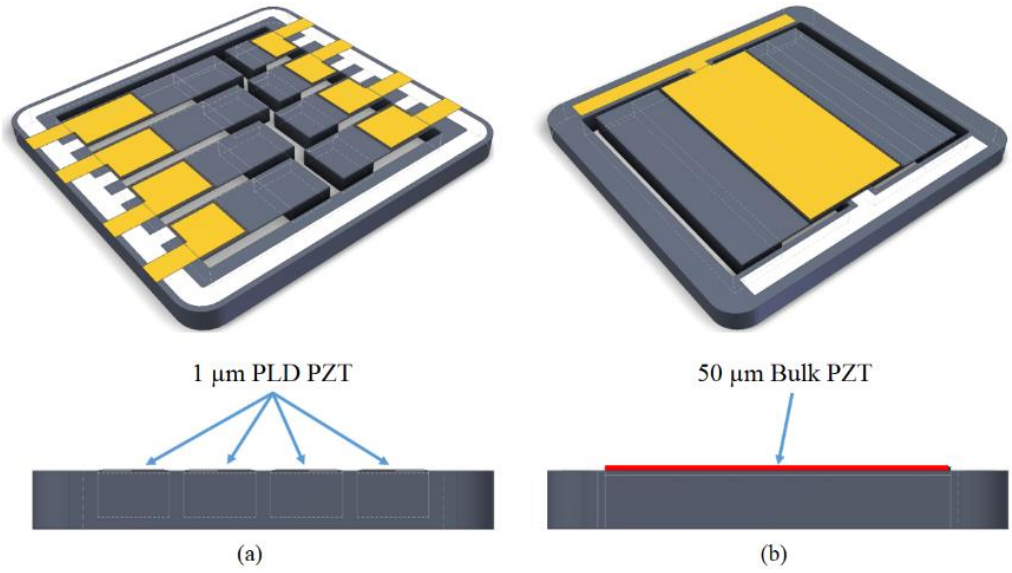

Figure 3.2. Perspective view and orthographic side view of the acoustic transducer (a) and piezoelectric energy harvester chip (b) models.

The piezoelectric material is rising from the surface of the transducer body when bulk type is used in the energy harvester chip. Figure 3.2 shows the model of the both

MEMS resonators designed and fabricated under the FLAMENCO Project. Height of the orthographic views are scaled two times to exaggerate and make the height difference between piezoelectric layer of the two chips visible in the energy harvester chip. For the acoustic chip, cantilevers are bending upwards due to induced stress by the deposited layers. Thus, both chips should have some recess structure above them to allow packaging without damaging the cantilevers. To solve this issue, cavity structures are formed on the wafer and parylene is shaped with a recess at locations coinciding with the cantilevers.

Commonly used BioMEMS material, parylene is chosen for the substrate polymer because of its easiness of processing, availability and its great mechanical and chemical properties. Parylene is deposited in room temperature, thus its process is compatible for low temperature MEMS materials, especially the piezoelectric materials. Further, it forms uniform and conformal polymer layer, it can fill all the cavities on any surface. It is etched using oxygen plasma. For its selectivity in any etch process system its etch speed relatively lower than that of photoresist. Speed of etching varies in etch systems. In order of increasing etch speed; oxygen plasma, inductively coupled plasma reactive ion etching (ICP-RIE) and inductively coupled plasma deep reactive ion etching (ICP-DRIE) system [48]. Basically, as the vertical ion bombardment which etch any material physically becomes more pronounced, speed increases. As the deposited parylene layer thickness increases, the low selectivity of etching definitely becomes a major drawback. Aside from this circumstance, it is a low cost and an accessible material utilizing overall easy coating system.

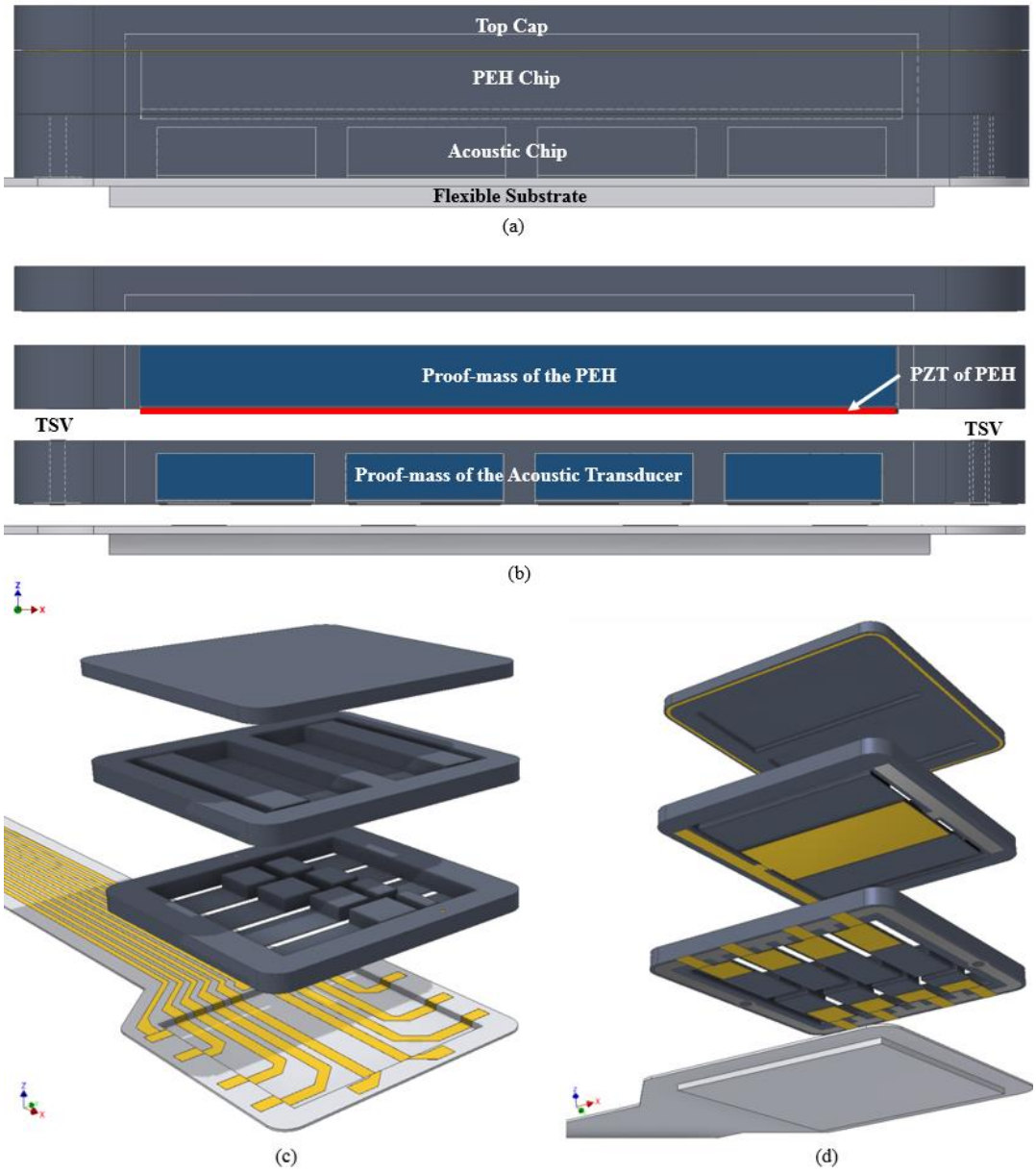

Figure 3.3. Side view of the 3D integration of transducer chips on flexible substrate in proposed front-to-back method, (a) model of the bonded package, (b) exploded model of the package, (c) perspective view from top corner, (d) perspective view from bottom corner.

As its chemical properties, it is frequently used in wearable electronics, biomedical applications and all types of implants. It is an inert material and resistive against organic solvents. It does not disturb the tissue in contact, thus it provides biocompatibility [49]. For the physical properties, young's modulus of parylene-C, the most commonly used and accessible type of parylene, is 2.76 GPa. Comparing the young's modulus with a single crystal silicon would give better idea of what the value represents. Depending on crystal orientation as (100) and (110), it is in the range of 130 GPa to 169 GPa for a silicon respectively which makes parylene a very flexible material [50]. This contrast between two materials is critical. Since the MEMS chips are fabricated with micromachining on crystalline silicon substrate, this study is focused on establishing electrical and mechanical connections between rigid and the flexible and making the transition.

As, the application of placing rigid chips on flexible material prone to fail as we experienced in the previous experiments in our project, in a flexible parylene, harder material needed to be merged on the substrate where chips will be located. Making this location rigid would help to make the package robust, as it will be a suspended membrane structure covering the devices. Titanium nitride (TiN) is chosen to provide rigidity as it is commonly used in the industry for adding toughness to the surface it is coated. It is known to provide resistance against corrosion, heat and wear [51]. Besides the toughness, it is also a biocompatible material and used in many biomedical applications [52]. TiN films can be deposited by physical vapor deposition (PVD) or chemical vapor deposition (CVD) processes, but the speed can be low. Additionally, gas tunnel type plasma reactive spraying process is developed for the formation of thick Titanium nitride in a short time [53], which is not available in clean a room environment. For the layer thicknesses needed, basic finite element modelling (FEM) simulations were carried out as this method has not been experimented.

3.2.1. Front-to-Back Integration

This method is developed for establishing contacts of the 3D integrated transducer package from a single surface at the location where it is fixed on the eardrum or ossicles. It utilizes the TSV integration on one of the transducer chip to have the electrodes of the other chip transferred to the same surface that is in contact with the flexible substrate. Thus, flexible substrate having one designated location for the chip placement is designed. Figure 3.1 shows the stacked chips on flexible substrate and some important details of the chips such as TSV location on acoustic transducer chip and the bulk piezoelectric structure stands on top of the acoustic transducer cantilevers. Package is planned to be integrated starting from bonding the acoustic chip and the PEH chip in 3D manner. Then, top cap die is bonded on top of the PEH chip covering the top side of the transducers. Finally, the 3D integrated chip stack is placed onto the designated location by flip-chip bonding and it is connected to the flexible substrate electrodes.

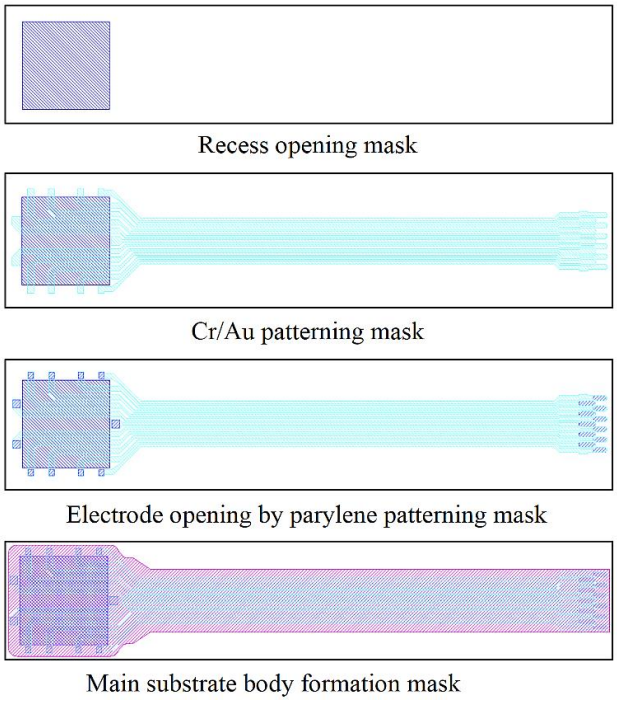

Figure 3.4. Process masks designed for the fabrication of the flexible substrate for front-to-back transducer integration.

For the fabrication of the flexible substrate, five process masks are designed as recess mask, TiN patterning mask, Cr/A u patterning mask, electrode opening mask and substrate body mask However, for the single head type, TiN patterning is not applied so, other four of the masks are used as depicted in Figure 3.4 according to the process order. Left end of the substrate is designed to allocate the 3D integrated transducers and the right end of the it is designed to fit for a zero insertion force (ZIF) connector with 11 electrodes. Location of the electrodes on the substrate is designed to match with the transducer chip electrodes.

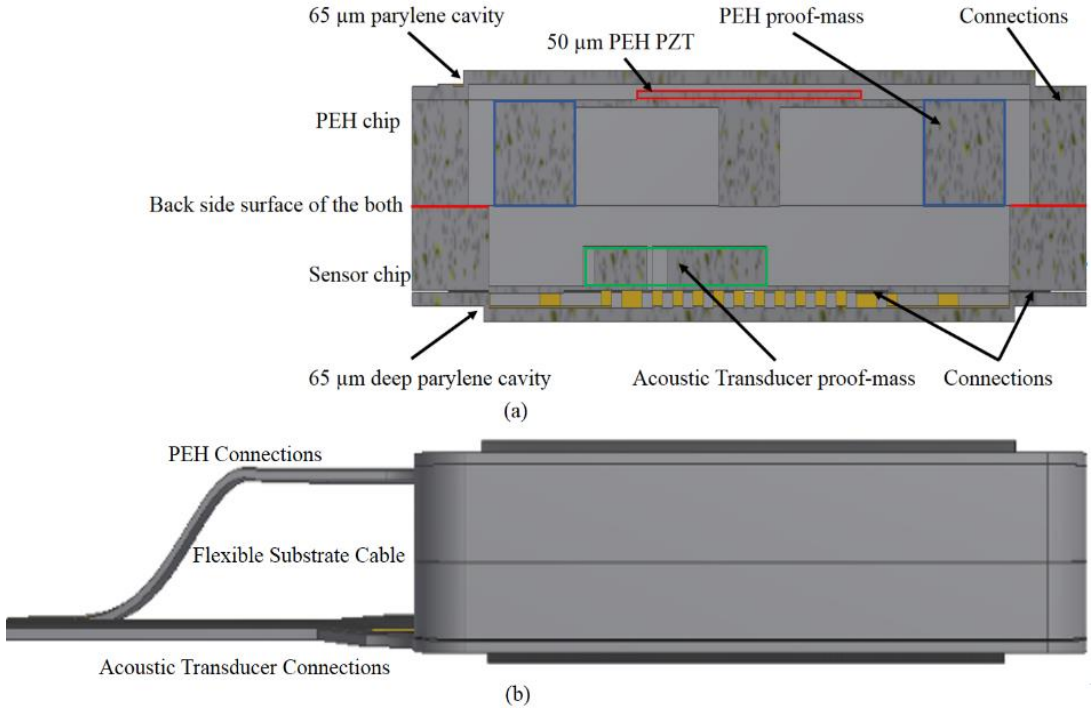

Figure 3.5. Drawing of the back-to-back integration method, (a) inside of the package from the cross section, (b) side view of the package and the cable part of the flexible substrate

3.2.2. Back-to-Back Integration

In this method, contacts from the integrated transducer package is taken from the both top and bottom side by bonding the backside of the chips to each other so that the front side surfaces are facing outside. Thus, having TSV inside one of the chip is no longer a necessary. Twin type of flexible substrate is used in this method. First, each chip is

bonded to their allocated location on the head segment of the substrate. Thus, electrodes of the two chips are connected to the same substrate. Then the backside bonding is carried out, bringing the two heads together as illustrated in Figure 3.5. In this drawing, the models scale in the z-axis is exaggerated four times to allow more details to be highlighted.

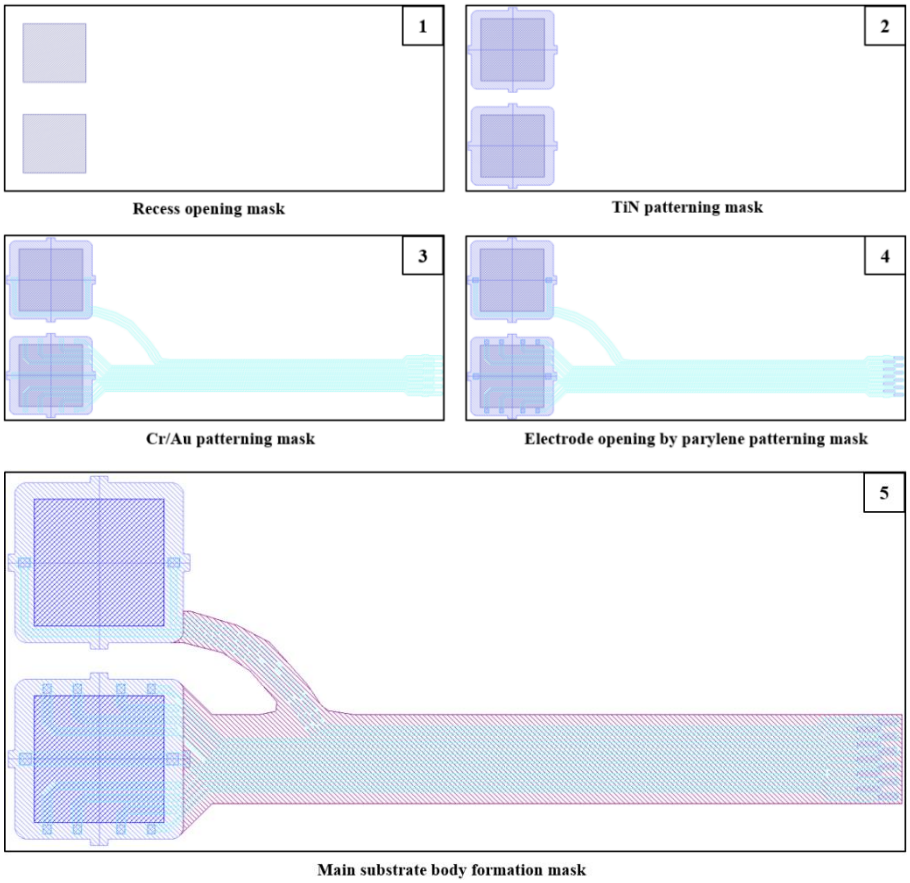

Figure 3.6. Process masks designed for the fabrication of the twin type of flexible substrate for back-to-back transducer integration.

Actual shape of the twin type of flexible substrate body is drawn on mask number 5 as shown in Figure 3.6. All process masks are illustrated in the drawing according to processing order. A branch is connecting the second head segment to the main body of the substrate. When the two head is occupied with chips, branch is bended towards the main head and backside of the two chips are bonded. Other end of the substrate at right side is for the ZIF connector.

3.2.3. FEM Simulations for Layer Thickness Optimizations

It was common in the both methods at the design phase that there was unknown parameters such as the layer thicknesses of parylene, gold and TiN. Both single and twin type of substrates are fabricated on the same wafer. Hence, determined values would be the same for both substrate models.

A basic bending simulation is carried out under constant pressure to determine if this is a functioning approach to the make parylene harder and how thick the deposited parylene and TiN film should be in applicable conditions for minimal displacement of the membrane under constant pressure.

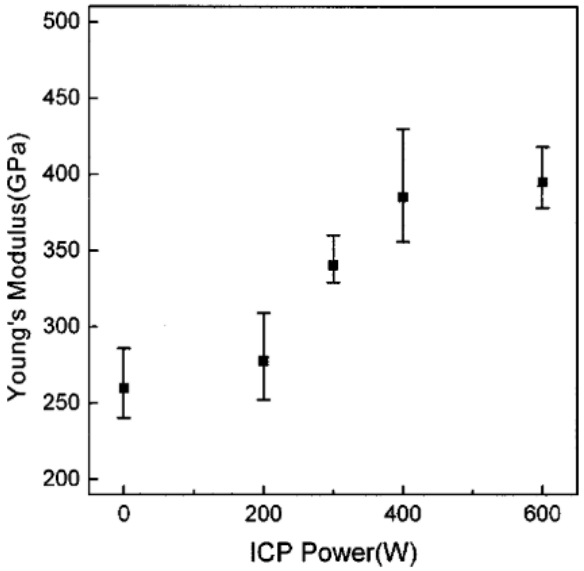

Figure 3.7. Sputtering power dependency of TiN coatings Young's modulus *[54]*.

The values used in the simulation as the material properties are listed in Table 3.1. Young's modulus value of the TiN coating from magnetron sputtering depends on the plasma power [54]. In the case of this study, 300 W is used for the sputtering process which corresponds to 340 GPa obtained from the Figure 3.7.

Table 3.1. *Material parameters for COMSOL structural mechanics simulation*

	Materials		
Properties	Parylene	Gold	Titanium Nitride
Young's Modulus (GPa)	2.8	70	340
Poissons Ratio	0.33	0.44	0.25
Density (kg/m^3)	1289	19300	5600

COMSOL structural mechanics simulation for observing the effect of the gold layer and titanium nitride layer thickness variations with different parylene thicknesses on the deflection of the membrane is performed. Simulation setup consists of 5x5 mm^2 parylene membrane that is clamped from all its edges. Uniform pressure is applied on the surface. For the estimation of the rectangular membrane deflection under uniform load, Galerkin's method is used as the derived equation for x, y coordinate system is given below [55].

$$w = \frac{7p}{128D\left(b^4 + \frac{4}{7}a^2b^2 + a^4\right)}\left(x^2 - a^2\right)^2\left(y^2 - b^2\right)^2 \tag{3.1}$$

From the equation (3.1), p stands for pressure, a and b are the half of the dimensions of a rectangle and D is given in equation (3.2). As the maximum deflection occurs at the center of the membrane at (y = x = 0) point, the equation simplifies as expressed in the following equation (3.3).

$$D = \frac{Eh^3}{12(1-\nu^2)} \tag{3.2}$$

$$w_{\max} = \frac{7pa^4b^4}{128D\left(b^4 + \frac{4}{7}a^2b^2 + a^4\right)} \tag{3.3}$$

For the equation (3.1), if it is applied to a square membrane, in (a = b) case, expression becomes simplified as Eqn. 3.3, and when the maximum deflection point at the center is inserted, expression further simplified as Eqn. 3.4. This gives the final form of the equation, which gives a linear solution closer to the simulation. Whereas in the FEM

simulation COMSOL creates matrixes for the meshes created in the model and tries to converge the results which gives the closest to the real model.

$$w = 0.0213\frac{p}{Da^4}\left(x^2 - a^2\right)^2\left(y^2 - a^2\right)^2 \tag{3.3}$$

$$w_{\max} = 0.0213\frac{pa^4}{D} \tag{3.4}$$

First, simulation for observing the effect of the parylene layer thickness variation is performed on 5x5 mm^2 parylene membrane by applying range of constant pressure from 0.5 to 5 kPa. Set of simulations sweeping the parylene thickness from 15 to 55 µm was conducted under the range of pressure. The setup is shown in Figure 3.8 with the induced stress on the 45 µm parylene. Resulted values are illustrated in Figure 3.9 showing the changes in deflection depending on parylene layer thickness.

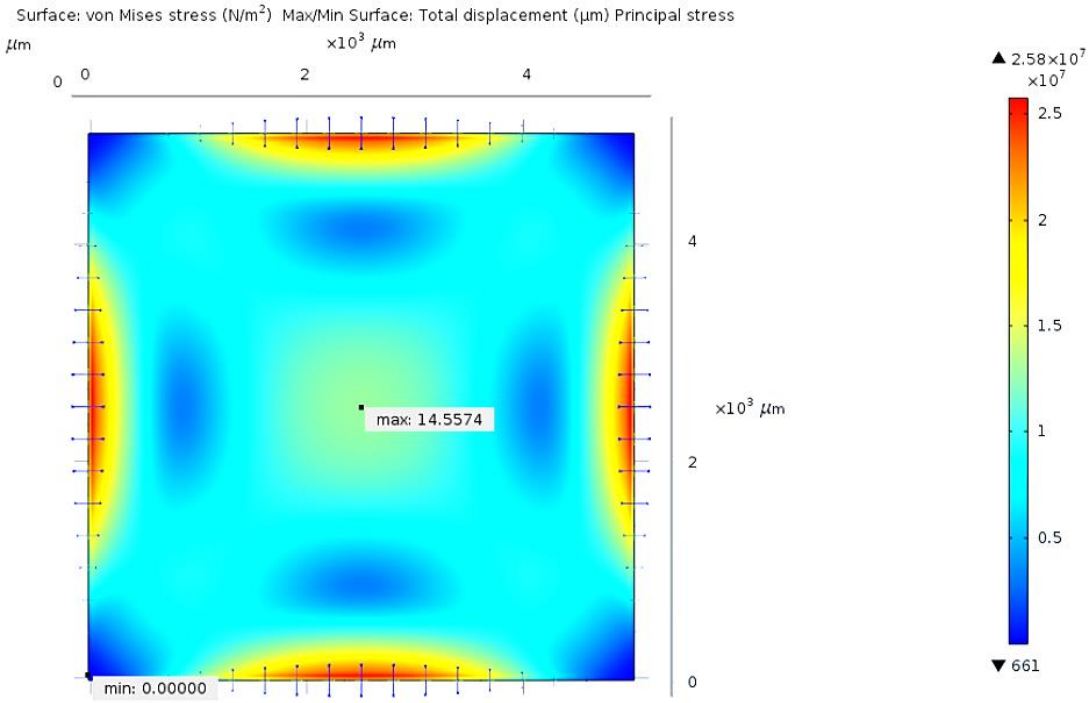

Figure 3.8. COMSOL model of 5x5mm^2 parylene membrane under 1 kPa applied pressure showing the induced stress distribution along the membrane and the maximum deflection.

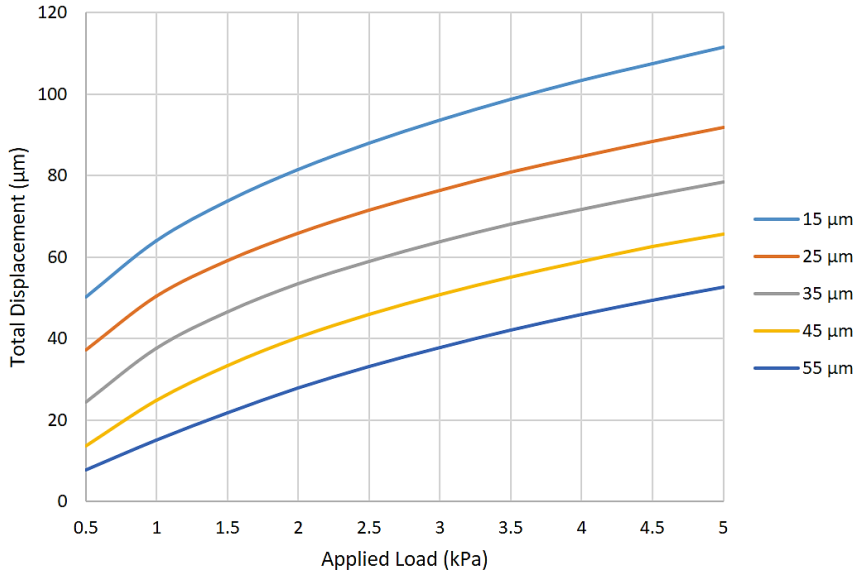

Figure 3.9. Deflection of square membrane under the range of applied uniform load for different layer thickness of parylene.

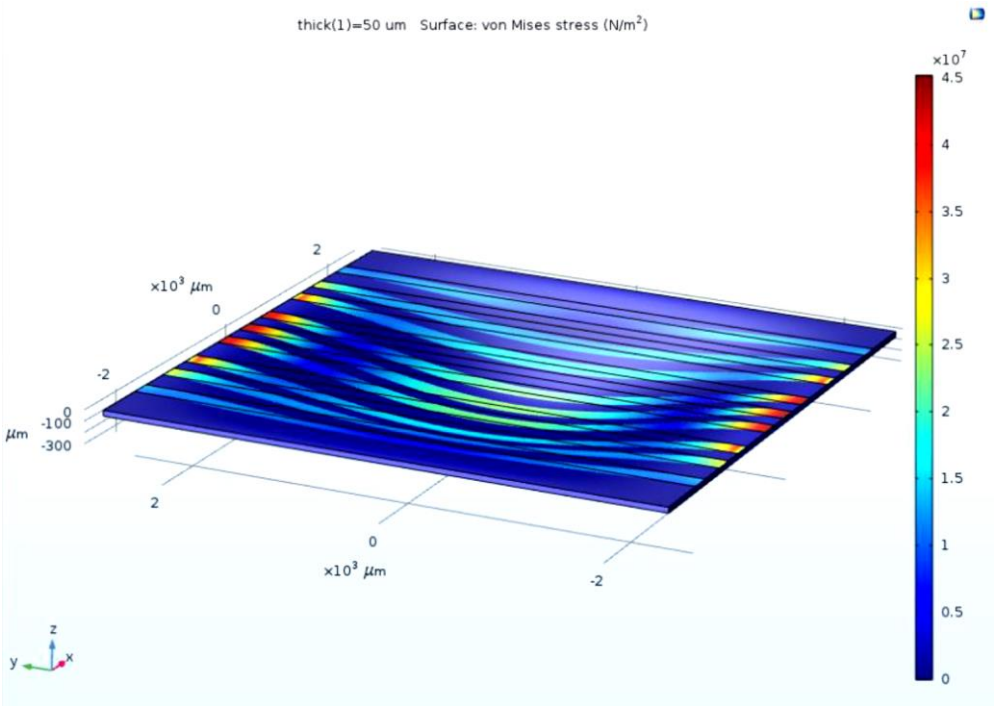

Figure 3.10. COMSOL model of 5x5mm parylene membrane under 1 kPa applied pressure showing the induced stress distribution along the membrane.

Later, the effect of gold layer thickness was evaluated on different parylene membrane thicknesses. Membrane with the same dimensions is used with 200 µm wide, 9 gold stripes on the surface as shown in Figure 3.10. Three different gold thicknesses are simulated to keep the values in the applicable range for the cleanroom processes. As the results are presented in Figure 3.11, increase of gold layer thickness does not contribute significantly to the membrane deflection.

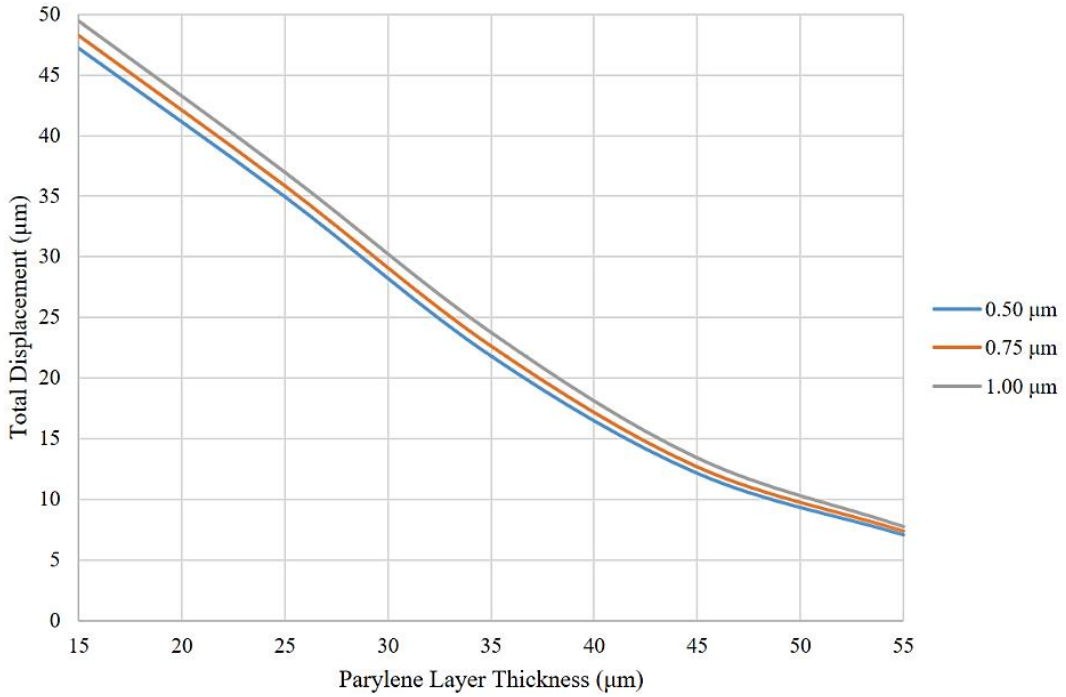

Figure 3.11. Deflection of different thickness of square parylene membranes under constant 1 kPa uniform load with varying gold layer thicknesses.

Titanium nitride thickness was simulated on 35 µm parylene membrane under the same range of applied load as the previous simulations. Different values starting from 0.5 µm to 3 µm were used. According to the simulation results shown in Figure 3.12, the contribution of TiN layer is worth adding it on the structure for reducing its deflection. For the comparison, deflection of the parylene only membrane is also included in the same graph.

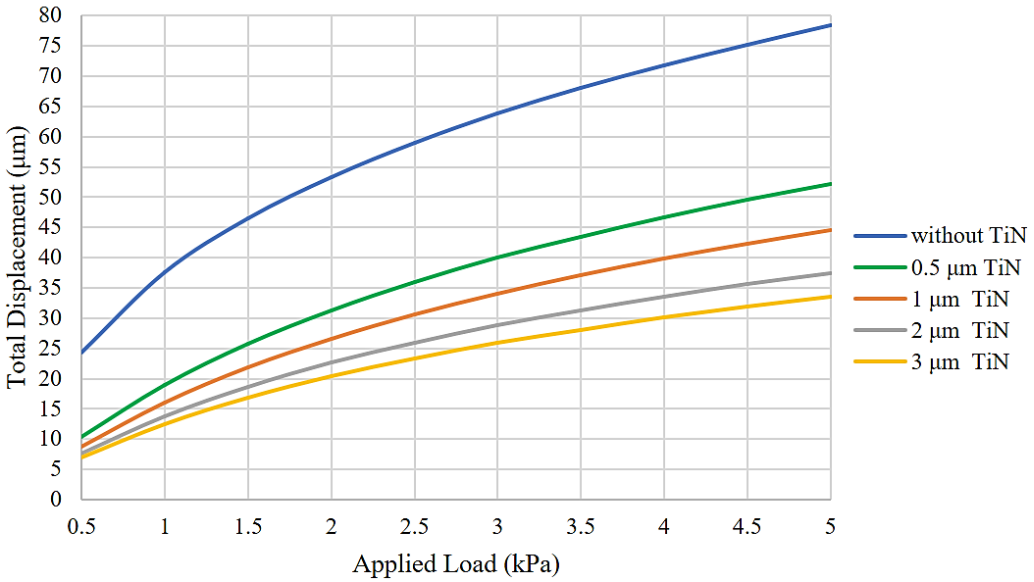

Figure 3.12. Deflection of different thickness of TiN layers on 35 µm parylene membrane under the range of uniform load.

Finally, the set of simulations for a square membrane composed of all three layers included were conducted. This time, gold layer was chosen as 0.75 µm and TiN as 1 µm thick constant for the fabrication feasibility. The parylene thickness parameter was swept in 15 to 55 µm range and deflections from 25.4 µm to 3.1 µm were observed respectively. 35 µm was selected for the parylene thickness which gives 9.85 µm deflection. Thicker parylene would not be applicable in the fabrication since the duration of the coating and etching processes drastically increases above applicable levels.

3.3. Fabrication of the Flexible Substrate

MEMS fabrication techniques such as micromachining and thin film deposition and photolithography are utilized in a wafer level fabrication of the flexible substrate. Developed process flow with 8 steps is illustrated in Figure 3.13. In addition to those process steps, shape of the substrate body is formed with final photolithography step.

Regular photolithography process is used for 2D structure patterning. When High-aspect-ratio micromachining processes such as DRIE or LIGA [56] are involved in

the process flow, there is third dimension is introduced. In our case, because of the recess structure, third dimension is created by DRIE. Thus, in this fabrication flow, the most challenging process step is the metal patterning in vertical direction through the recessed structure.

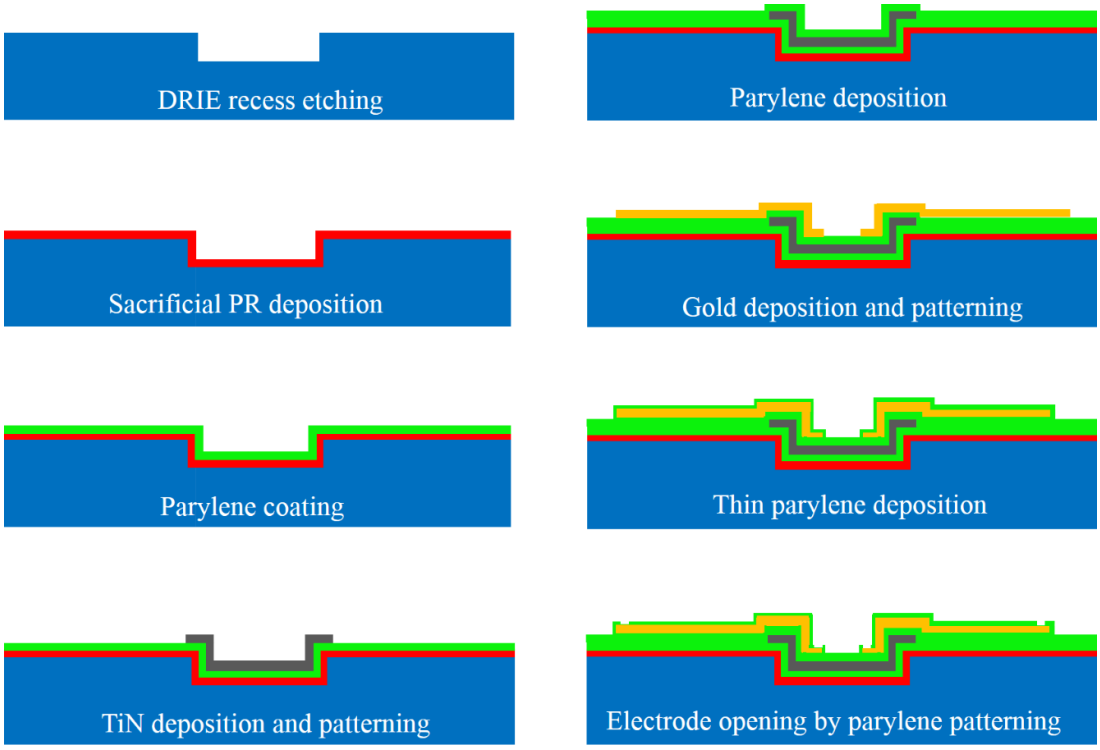

Figure 3.13. Fabrication flow of the flexible substrate.

The first DRIE process which determines the depth of the recess structures is critical for successful gold layer patterning. Because of the bulk piezoelectric on top of the PEH chip, we want recess depth to be at least deeper than 50 µm for functional packaging. Before the fabrication, in order to determine the depth, 100 µm and 50 µm recesses were created. Sacrificial spray photoresist and subsequent parylene layers were deposited as 8 µm and 10 µm respectively. Then, spray resist coated for patterning trial. UV exposure with a routing mask is applied for 3 times 30 seconds with 45 seconds waits between each exposure. Normally, spray resist exposure is performed with single 45 seconds exposure. Development was performed with 2 minutes and 20 seconds duration which was normally only 2 minutes. The longer

recipe worked for 50 µm recess. But increasing the number of exposure cycles or the development time does not help to remove the unwanted photoresist for 100 µm depth. After the trials wafer with 100 µm recess was diced and SEM analysis for both wafers were carried out as shown in Figure 3.14.

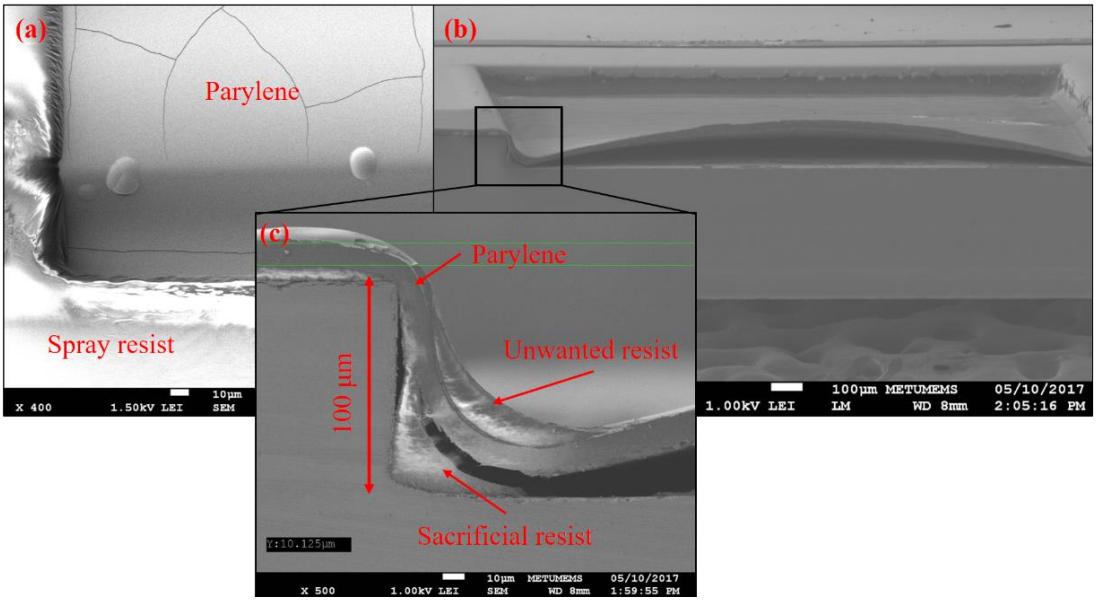

Figure 3.14. SEM images, a) tilted view of 50 µm recess structure successfully patterned, b) 100 µm recess, c) cross section of close-up corner showing the unwanted photoresist and other polymer layers.

According to the first trials, recess depth determined to be 65 µm which is in the allowable limits for patterning a layer. Fabrication is started with the cleaning of the single crystalline substrate wafer. 4" wafer go through the standard cleaning procedures. Then, photolithography process is carried out. SPR 220-3 photoresist spin coated at 2000 rpm. Soft bake is applied for 3:30 minutes. DRIE mask number 1 in Figure 3.6 is used in the exposure step that takes 10 seconds, followed by 53 seconds development with MF-24A TMAH based developer solution. It is a dark field mask that drawn features are in transparent pattern. First alignment marks are form at the alignment location that will be followed by the rest of the alignment marks in the proceeding processes. DRIE process is performed using the 'Structure' recipe in STS Pegasus for etching approximately 60 - 65 µm deep cavities in 12:30 minutes process time.

Right after the DRIE process, removal of the remaining photoresist and surface cleaning processes are done. Later, spray photoresist composed of S-1813 with Acetone mixture is coated everywhere on the wafer as a sacrificial layer. Hard bake process performed on sacrificial PR layer for about 2.5 hours at 110 °C. Parylene deposition process has been carried out following this process. 55 gram of Parylene-C dimer was put into the furnace. Layer thickness measurement with Dektak profilometer tool after coating showed 25 micrometers layer thickness. Both polymer layers are creating a conformal layer that smoothens the cavity edges as shown in Figure 3.15.

Later, Titanium nitride sputtering is performed at low power and short process time with wait intervals in order not to damage the parylene, since the deposition is on parylene layer that has sacrificial photoresist layer underneath that is temperature sensitive. At first, recipe with 200W active power in half an hour process steps and 15 minutes wait durations in between for cooling is used. Expected deposition speed was lower than 6 nm/min which is observed at deposition with active power 300 W. Dummy chip is placed on the surface, because the roughness of the wafer surface is 1 µm, which is much higher than the expected TiN thickness. After the long deposition process, layer thickness measured in Dektak on the smooth SiO_2 reference surface, which resulted in 210 - 220 nm of TiN. We have checked the data log of the AJA sputter tool but there was no problem in the process. Obviously 200 W was too low active power for working recipe with the TiN source.

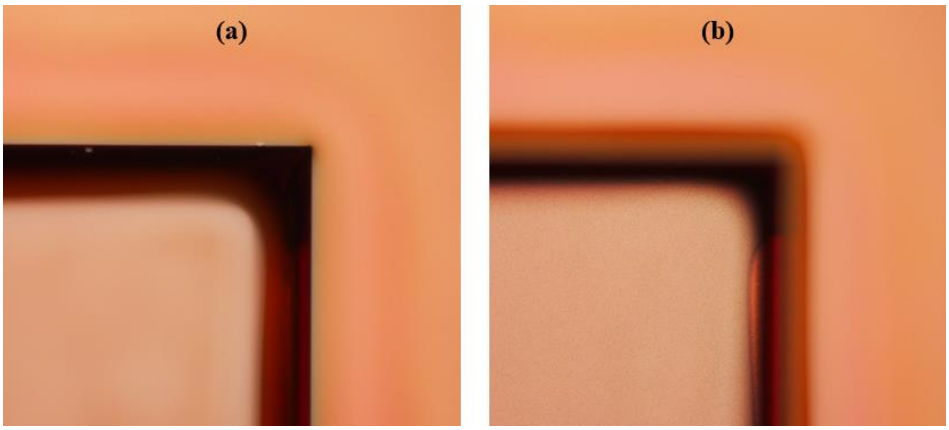

Figure 3.15. Recess corner after sacrificial photoresist and parylene layers coated, microscope objective focused to the top surface (a), and focused to the lower surface.

New recipe with 20 steps each step as 10 minutes sputtering and 5 minutes wait time is used for the second trial. 800 - 840 nm TiN thickness is measured on the dummy die from the Dektak tool, which add up with the previous thickness and makes 1 µm film thickness in total.

Wafer with TiN layer is coated with film photoresist. Laminar-E9220 is manual laminated on hot plate at 65°C. Its patterning is performed using process mask number 2 in Figure 3.6, which was actually designed for the chip alignment at the end of the carrier fabrication process. Since this mask has a dark field pattern, when it is used with negative type of photoresist as in film resist, it will cover only the drawn features. Alignment marks are 5 µm larger than the alignment marks of the first mask. As previously stated, exposure time of 4,5 seconds and development time of 65 seconds are applied in the photolithography step and wafer is ready for the TiN patterning step.

Wet etching of the TiN layer is carried out using 45 ml HF, 1250 ml HNO_3 and 450 ml H_2O mixture [57]. After the mixture is prepared, 15 minutes waited before using to get ready. Etching of 1 micrometer of TiN took only 19 seconds. Patterned film photoresist and TiN are shown in Figure 3.16.

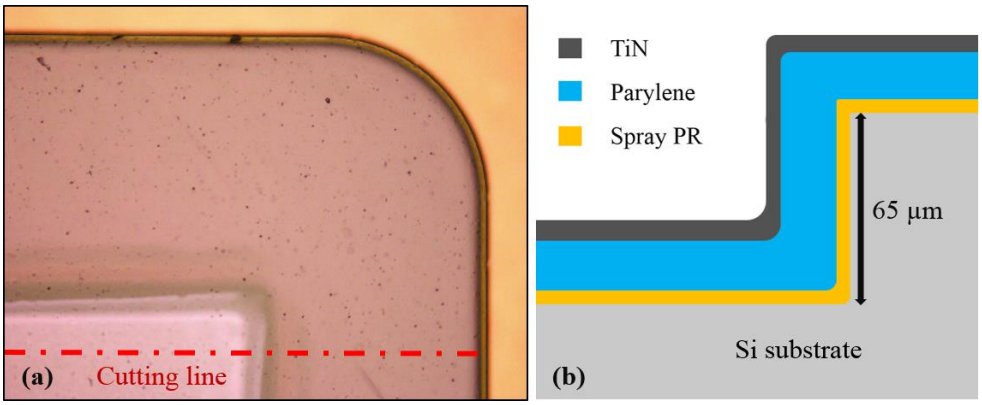

Figure 3.16. (a) recess corner after patterning of TiN film under film photoresist, (b) drawing of the cross section in reference to cutting line.

After the wet TiN etching process, film PR is removed by immersing the wafer in MF-24A solution overnight. Deposition of the second layer of parylene is carried out with 22 gram of parylene-C dimer. A layer of 10 µm is obtained. Cavity edges are smoothened more and more after the 7 - 8 µm sacrificial resist and 35 micrometers of parylene layers.

Next, low power gold sputtering is carried out to prevent any damage to the parylene due to high temperature. Process was performed under 100 W for 950 seconds for deposition of 500 nm Au layer. Working distance was 5 millimeters and the chamber pressure during deposition was around 5 millitorr. In order to obtain 750 nm targeted line thickness, subsequent 475 seconds of process added after the first step.

Then in the third photolithography step, wafer has the gold deposition on the surface that spray photoresist is coated. It is chosen for the mask layer in this photolithography process because of the cavities. Process mask number 3 from Figure 3.6, which is clear field, is used for patterning of the electrodes and the paths, as shown in Figure 3.17. Alignment patterns are 5 µm smaller than the alignment marks of the DRIE alignment marks for visibility during alignment of the clear field mask.

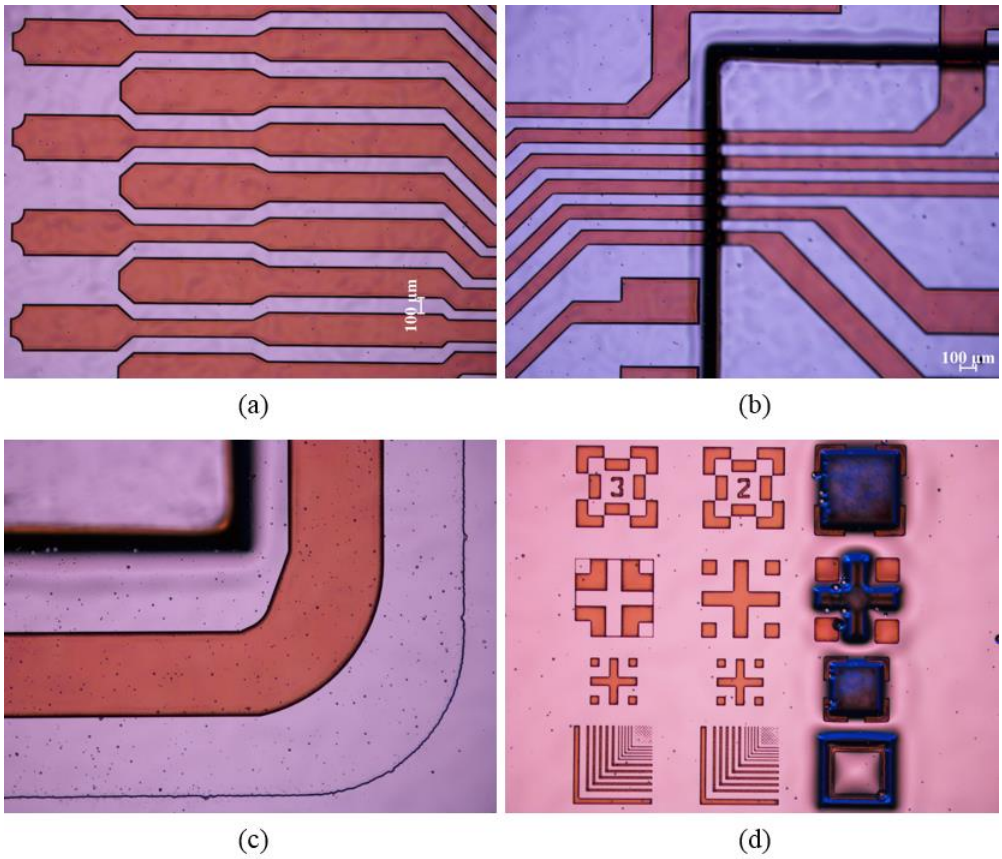

Figure 3.17. Flexible substrate after metal mask photolithography, (a) ZIF electrodes, (b) chip electrodes, (c) recess corner, (d) alignment mask till metal patterning stage of the process flow.

This photolithography step is the most critical process in this fabrication. Firstly, regular parameters are applied as 50 seconds exposure with 12,5 millijoule UV lamp and 2 minutes of development process with MF-24A solution. However, pattern would be short circuiting all the lines from the bottom corner and edge of the cavity. Photoresist that needs to be etched is not exposed enough because of the high aspect ratio at the sidewalls. Also, duration of the development step is extended in all the trials, but from the observations it was decided that it does not have much contribution on the patterns as it was no etching unwanted resists. In the second trial, 4 times 20 seconds exposure time with 75 seconds wait interval is applied with 24,5 millijoule UV lamp. This helped to remove most of the unwanted resist but there was still a thin layer remaining at the middle of the sidewalls vertical surface. In Figure 3.18,

microscope observations are carried out by tilting the wafer in order to observe the cavity sidewalls. Hence, another trial needed to find the optimized exposure parameters. In the third trial, 12,5 millijoule UV lamp is used with recipe of 5 times 40 seconds exposure duration with one minute of wait time in between. Desired photolithography process with no resist remaining on sidewalls is obtained. Development takes 2:20 minutes in this last trial which was the best case. Result of the second trial as unwanted and the third trial as the desired photolithography processes are juxtaposed for comparison in Figure 3.19.

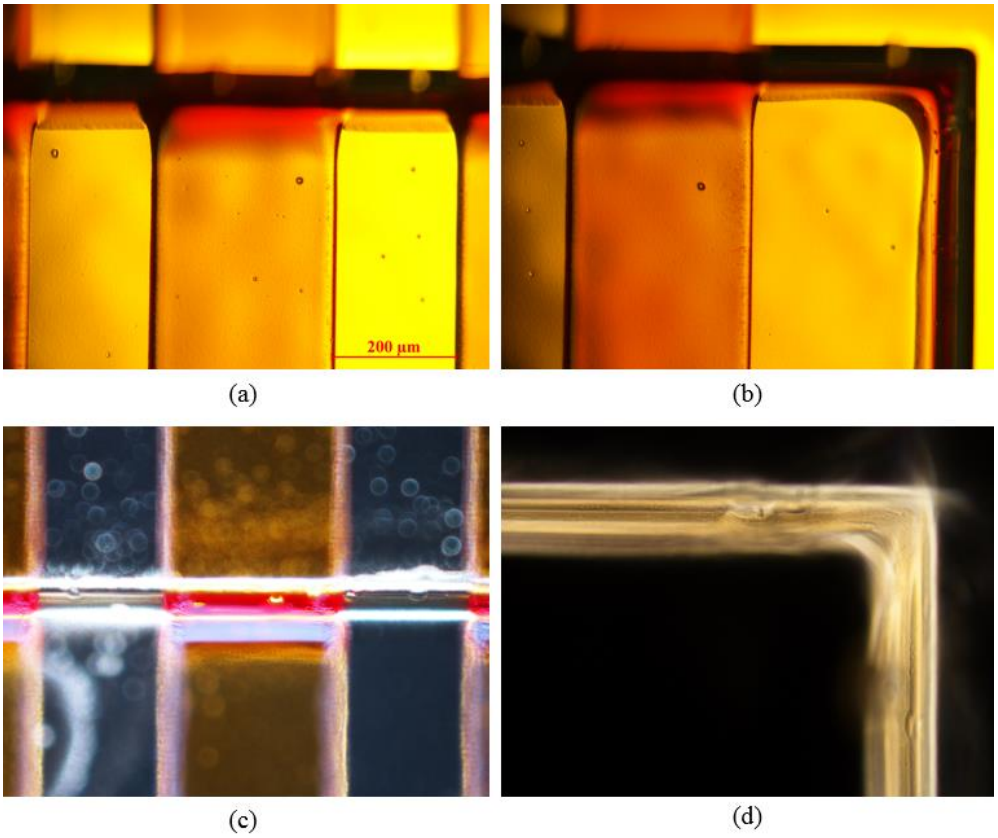

Figure 3.18. Microscope images from the tilted wafer after regular photolithography (a) and (b), second photolithography trial (c) and (d).

Process continued with wet etching of 750 µm thick gold layer. A quick check is performed with probe station by scratching photoresist layer on top confirmed that there is no short circuit between the electrodes. Photoresist layer is removed and the surface is cleaned at the end.

In Figure 3.18 and Figure 3.19, the images shown has the cross sectional structure of 65 µm recess as shown in Figure 3.16 (b).

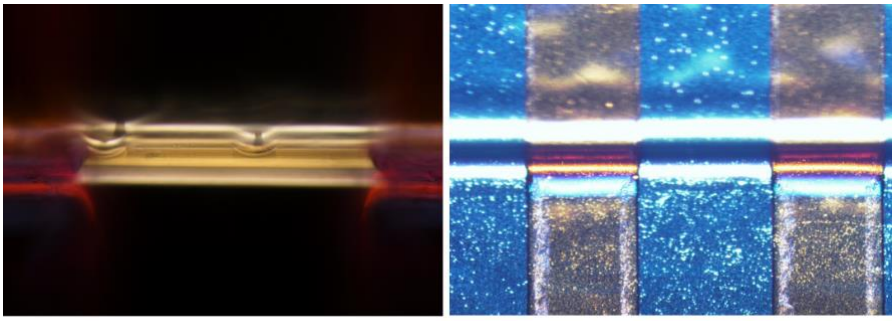

Figure 3.19. Images from the tilted wafer after second (a) and third (b) photolithography trials.

Parylene coating is performed on the patterned metal layer. Layer thickness was targeted to be 1 µm, using 2.25 gram of parylene dimer. It will cover the metals working as a dielectric layer where otherwise it could cause short circuit at the integration the transducers. Photolithography process is continued after the spray PR coating with regular parameter. In the alignment step, process mask number 4 from Figure 3.6 is used to leave the electrode pads open while covering the rest of the wafer.

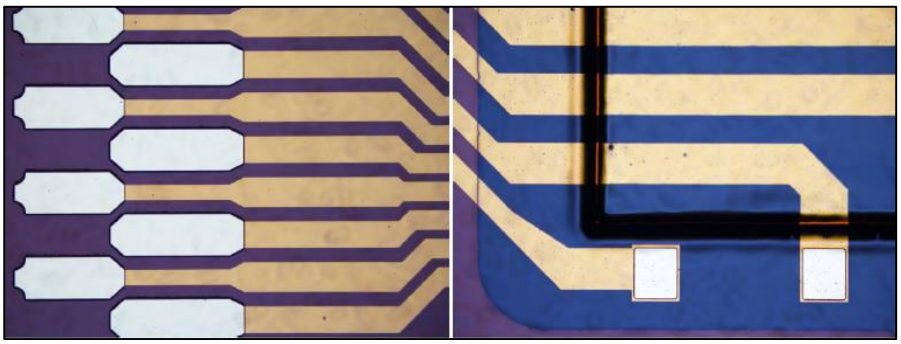

Figure 3.20. Electrode pads are opened after the parylene RIE process.

Etching of 1 µm parylene is done in STS RIE in 6:30 minutes. Microscope observation as in Figure 3.20 and multimeter confirmation is carried out to get contacts from the electrode openings. Later, rest of the PR is removed on the surface.

In the last process, again spray photoresist is coated on the surface. Substrate body mask number 5 in Figure 3.6 is used for patterns. It is used to establish the outlines of the 36 µm thick parylene layer. Etching of the thick polymers layer is not continued in the cleanroom. Following the photoresist patterns as guidance lines, cutting is performed with bistoury under a microscope. Releasing of the flexible substrates from the process wafer is carried out using acetone etching of the sacrificial layer after the transducer chips are bonded to the designed head segments. The process of parylene carrier fabrication ends after this step. Wafer with the fabricated flexible and recessed substrates are ready for the flip-chip bonding. It is photographed in Figure 3.21.

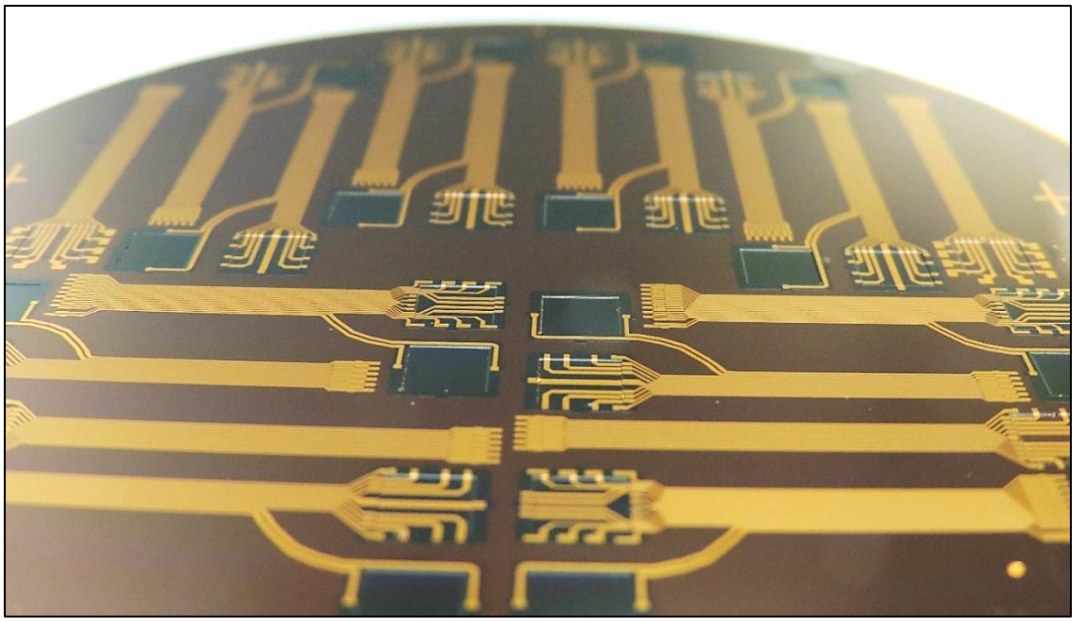

Figure 3.21. Flexible substrate wafer at the final stage of the fabrication flow before releasing.

CHAPTER 4

RESULTS AND DISCUSSION

In this chapter, characterization of the fabricated TSVs and the flexible substrates were presented individually. Then, as the ultimate goal of the study, feasibility of the two proposed 3D integration methods were tested for the fully implantable cochlear implant application. In the first method, TSV technology is utilized to transfer the chip signals vertically through its frame to the same flexible substrate as the other chip. In the second method, solution without using the TVS was searched using only the flexible substrate. Chips were bonded to each other from their backside hence the electrodes on the front side get bonded to the designated locations on flexible substrates.

Measurement of the fabricated TSVs small resistance is carried out with probe station using the four-point Kelvin structures created on fabricated TSVs. Next, wafer level TSV resistance map is created in one by one measurement along the wafer. Then feasibility of the TSV integration method for MEMS piezoelectric resonator devices were elaborated using the fabricated acoustic transducers in the project group. Fabricated frames with TSV are aligned on top of the acoustic transducer chips and they are bonded for 3D integration structure using the flip-chip bonder tool. This structure is created as a model of piezoelectric energy harvester and the transducer chip integration where transducer chip is fabricated with TVS. Testing the feasibility of the model reveals what we would observe in the actual implementation. Performance of the transducers from the TSV connections are gathered at excitation table experiments and results are discussed by comparison to the actual chip signals. Finally, the back to back combined 3D resonator stack is implemented to the flexible parylene substrate for packaging. ZIF connector soldered on a designed PCB was used to acquire the signals.

4.1. Four-Point Kelvin Measurement

Resistance measurement of the fabricated TSVs is performed with probe station using the four-point Kelvin test structure (Figure 4.3b). It is a suitable measurement technique for retrieving low resistance values because it eliminates other resistances such as probe to contact pad and probe wiring resistances [58]. First wafer level TSV resistance map was created for the fabricated wafer from the experiment number 2 in the Via Sealing Method section. On the wafer, TSVs were located on the electrode positions of the acoustic transducer chip mask as illustrated in Figure 4.2. While the resistance map was created, locations of the Kelvin structures were put on each cell and the chip names were used as the reference.

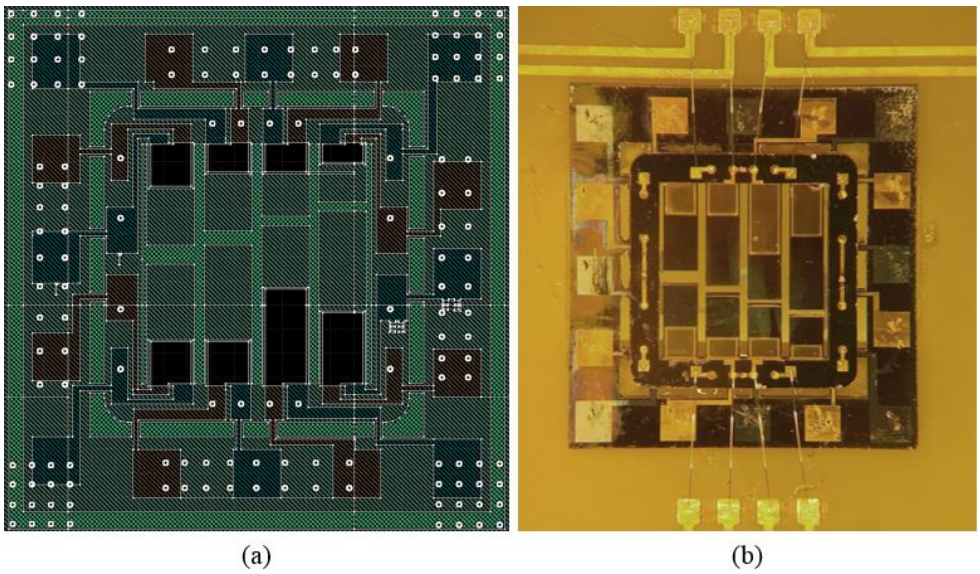

Figure 4.1. Aligned TSV frame and the acoustic transducer, (a) masks in the Cadence software, (b) aligned and bonded in 3D for the testing.

As presented in Figure 4.2, since the wafer was broken from the line next to A2 - E3, some of the Kelvin patterns were missing connections, thus, measurements could not be obtained. In general, nonuniformity of the filling profiles observed from the SEM analysis were verified as the different resistances distributed along the wafer. For the 400 μm height and 100 μm diameter of the TSVs resistance formula for cylinder is used to estimate 0.89 mΩ resistance. For the resistivity of the copper (ρ), 1.75 x 10^{-8}

Ω·m is used. As the thinning process etches the edges of the wafer more compared to the center, the thickness can vary. Thus, in the resistance map some of the TSV resistances were observed to be lower than the estimated value as their height is around 370 - 380 µm.

$$A = \rho \frac{h}{\pi r^2} \tag{4.1}$$

		-	-	54.4	-	45.7			
		-	A2	-	A3	6.6			
		115	-	-	24.6	40			
-	15.9	85	-	-	6.7	10.8	30.4	3.5	
B1	-	B2	1.3	-	9.6	B5	11.2	B6	
68.6	34.8	106	3.7	-	4.3	18.2	1.9	12.8	
16.3	2.2	33.5	6.4	29.3	6.7	2.8	104	22.3	
1.1	0.9	C3	1	C4	5.5	C5	2.7	-	
2.1	1.2	22.3	0.9	30.6	2.8	386	18.3	1.8	
7.6	6.4	584	-	0.8	18.5	30.1	10.8	1.5	0.8
D1	10.8	D2	-	0.9	7.1	6.1	D6	2.6	D7
1.6	1.5	20.8	-	3.5	2.1	12.5	3.4	1.6	0.8
4.4	5.3	17.6	308	6.7	7.2	2.3	8.3	1.5	
5.3	E2	5.8	E3	4.1	E4	3.8	E5	6.3	
71.9	5.5	-	-	3.8	4.7	7.8	8.7	3.5	
		62	51.2	2.3	3.6	0.9			
		F1	98.6	2.9	3.5	F4			
		8.1	19.5	3.5	8.9	2.2			

Figure 4.2. Through silicon via resistance map in milliohms, acquired from the four-point Kelvin measurements.

Next, Kelvin resistance measurements were conducted on the TSV wafer number 5 in the Via Sealing Method section. Single TSV resistance in average of 0.8 mΩ is measured, which was calculated as 0.75 mΩ using the volume resistance formula for cylindrical structure as an estimate since the real TSV walls are not ideally straight due to nature of the DRIE process. Diameters of the TSVs were the same but the wafer thickness was around 350 µm for this wafer. Scallop structures on the walls and the taper angle of the through via profiles are not taken into account. Wafer level

uniformity was obtained. In the edge region along the wafer, lower resistance values were observed compared to the center region. This is due to the thickness different where wafer edges were thinner than the center.

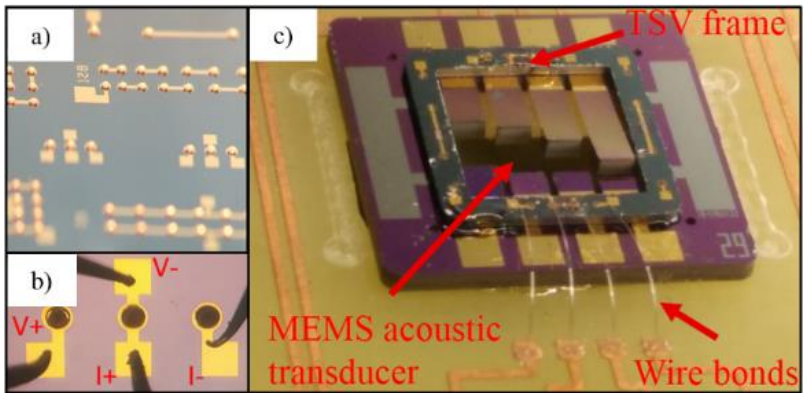

Figure 4.3. a) front side tilted view TSV patterns, b) four-point Kelvin measurement on TSV c) epoxy bonded TSV frame to acoustic transducer chip for feasibility test.

4.2. Acoustic Transducer Feasibility Test with TSV

Then, TSV frame is separated from the TSV test wafer by through silicon etching in DRIE. Frame dimensions are completely the same as the MEMS resonator chip frames. Its outer frame is for easy access to the electrodes and the connections are laser cut when TSV is integrated. Next, TSV electrodes and the chip electrodes are bonded with the conductive epoxy that is room temperature curable (Silver Bond, Transene), simultaneously for the mechanical fixation, regular epoxy is used.

The output voltage of the transducer before and after the TSV integration with respect to its resonance frequency is shown on Figure 4.5. Test setup consisting of an excitation table, a controller unit and a computer with Lab View application were used to collect the test results as illustrated in Figure 4.4. Four acoustic transducer chips are tested and their results are listed in Table I. Results with minor frequency shifts and small amplitude change where acquired. In average, 90% of the signal was recorded despite voltage drop. Decrease in signal can be attributed to the room temperature epoxy bonding.

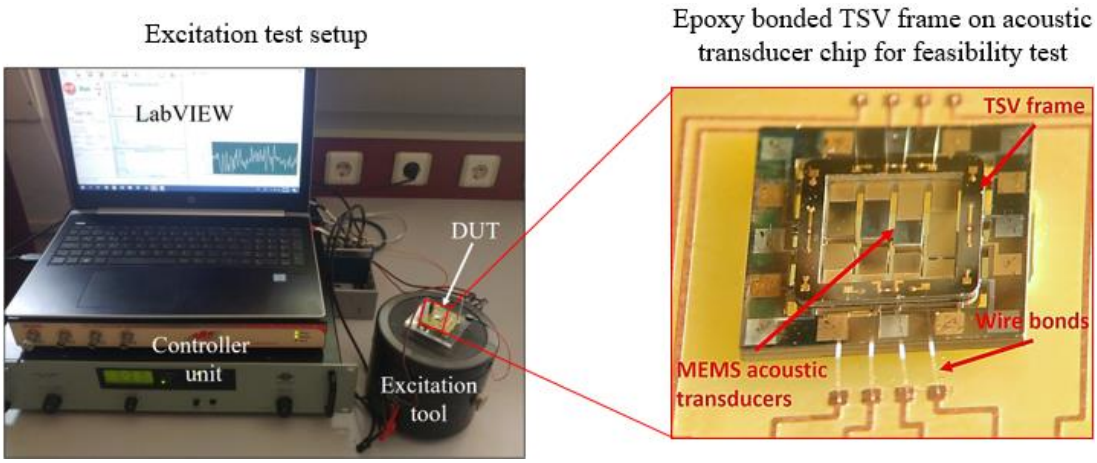

Figure 4.4. Excitation table test setup for testing the feasibility of the TSV with transducer chip.

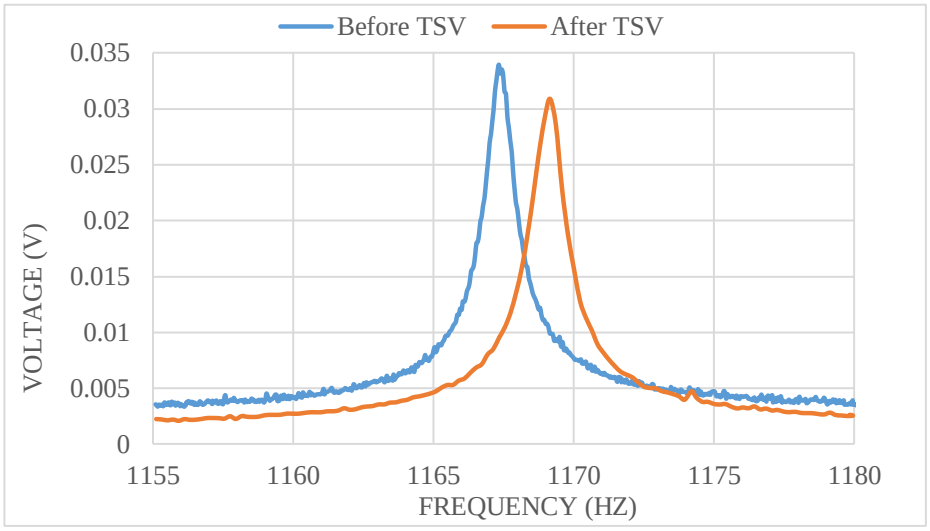

Figure 4.5. Excitation frequency vs. output voltage of transducer and its signal from TSV.

Careful handling of the transducer and the frame during bonding can yield 100 percent success. Proposed method is the most compact and the low weight solution for the cochlear implant developed in the FICI. To our knowledge 3D integration of such implants have not been reported in the literature. In the future application, transducer chip frame is planned to be fabricated with TSV and it will be connected to the energy harvester frame for the 3D integration. Proposed method is the most compact and the low weight solution for the cochlear implant developed in the FLAMENCO Project.

Table 4.1. *Excitation table test results in comparison with connection status.*

	Without TSV		**With TSV**	
	Frequency (Hz)	***Voltage (mV)***	***Frequency (Hz)***	***Voltage (mV)***
1	797.86	63.4	798.94	55.6
2	1154.52	25.1	1157.23	22.8
3	1167.34	33.9	1169.15	30.9
4	1639.98	23.3	1642.81	21.7

4.3. Experiment on Flexible Substrate Integration

The integration of acoustic transducer and energy piezoelectric energy harvester chips, two methods as proposed in chapter 3. Integration was experimented by three main steps as presented in Figure 4.6. First, MEMS resonators were bonded to their places using pick and place tool (T-3002-FC3). Electrical connections were taken by room temperature cured silver epoxy and the physical strength of the bond enhanced by using normal epoxy. Next, parylene substrate outlines were cut using bistoury under microscope. Then the wafer is immersed into acetone for 5 hours to release the substrates. In the first model, chips are bonded in the front-to-back formation. For the experimental purpose, a frame with TSV and acoustic transducer is used. Its 3D model and real integration are shown in Figure 4.7. First, two chip frames are bonded using silver epoxy for the electrode connection and regular epoxy for the rest of surface for strengthening the bonding. Then, 3D integrated die stack is bonded to the designated place on the parylene substrate where the signals are taken to the PCB once the substrate is connected to the ZIF connector. In the second method, Chips were bonded to their designated location on the flexible substrate from their front side. Thus, electrode connections are taken to the substrate this step. Then, the branch of the substrate holding the PEH chip is folded onto the acoustic transducer chips backside and bonded using an epoxy. The sample image and the sample before folding step connected to ZIF connector are shown in Figure 4.8.

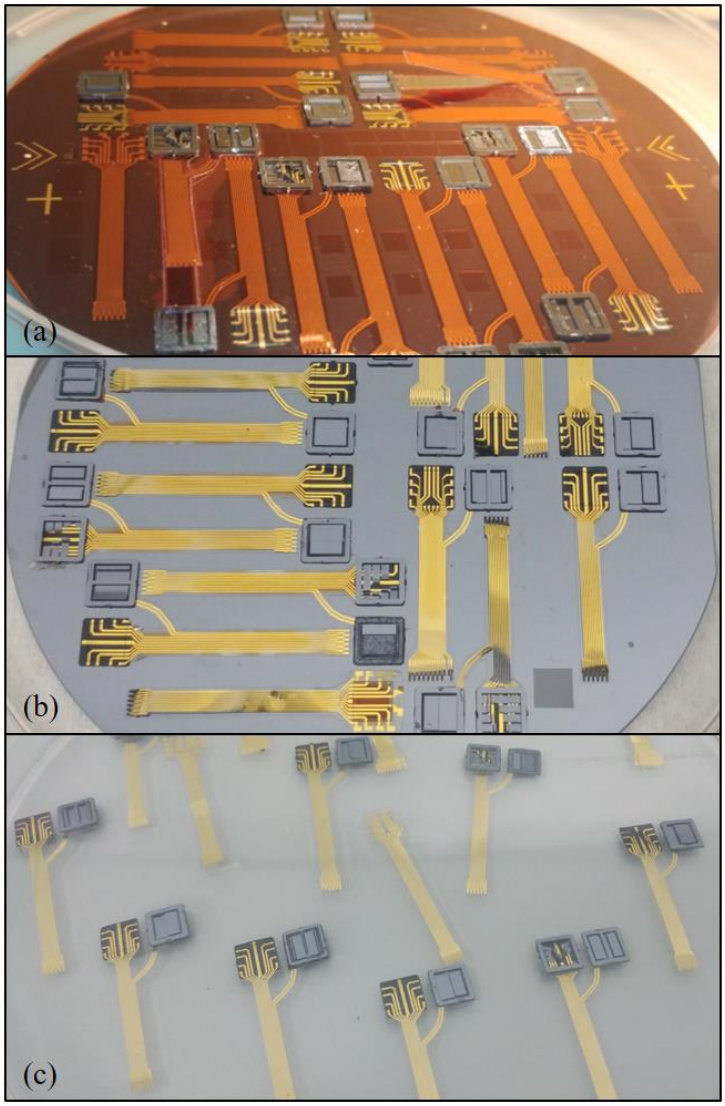

Figure 4.6. a) MEMS piezoelectric resonator bonding on flexible substrate fabrication wafer, b) immersing the wafer in acetone for releasing, c) released flexible substrates with bonded chips.

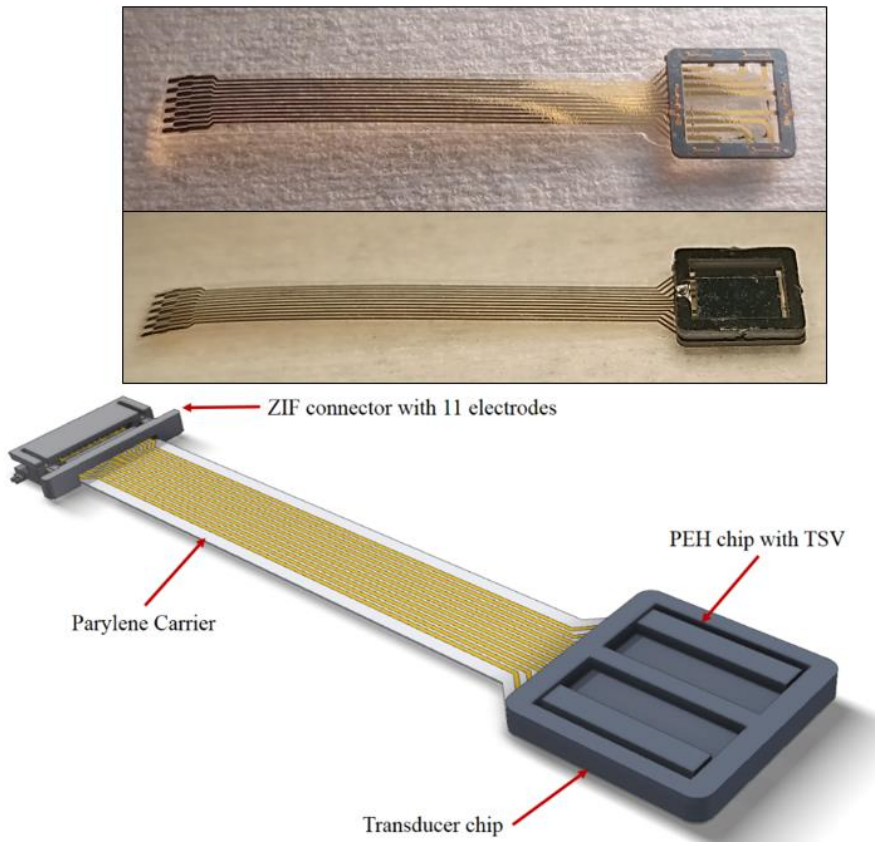

Figure 4.7. Front-to-back integrated transducer and PEH on single flexible substrate with ZIF connector as the first method.

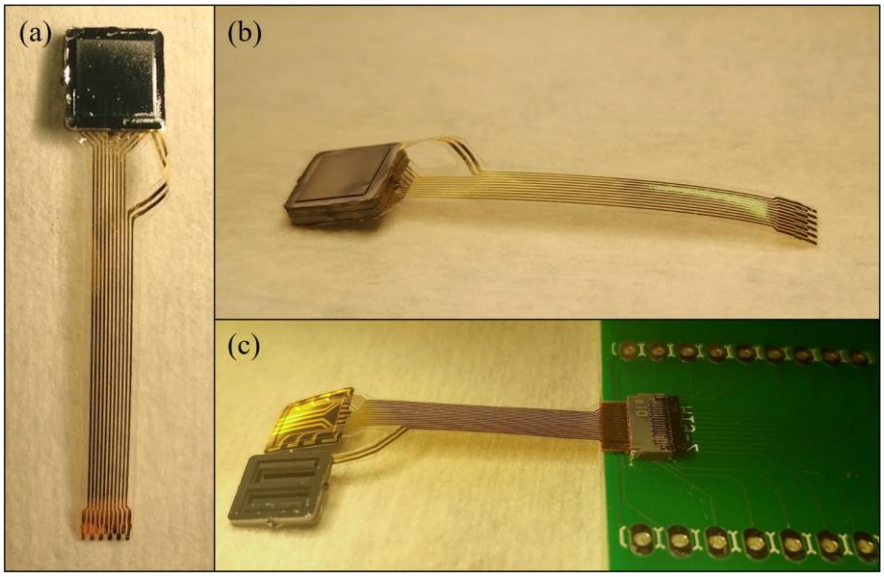

Figure 4.8. Back-to-back integration, flexible substrate with 11 electrodes, a) top view, b) side view, c) substrate with 19 electrodes inserted into the ZIF connector on PCB as the second method.

CHAPTER 5

CONCLUSION

In this thesis, system integration of the Fully Implantable Cochlear Implant that satisfies the constraints and requirements brought by the used materials, shape of the designed MEMS devices or the nature of the biocompatible in-vivo implantation has been explained. Different integration schemes are introduced consisting of the challenging through silicon via fabrication and packaging that is adopted from the CMOS fabrication technologies and the utilization of flexible electronics in biomedical applications. The fabrication and performance testing of the bottom-up electroplated TSV connections are demonstrated. Utilizing the designed bottom-up electroplating holder, void free TSV fabrication process is successfully developed. TSV resistance is measured using the four-point probe method from the Kelvin structures as 0.8 mΩ that is accurate to the calculation. For the feasibility testing of the MEMS resonator device integration with TSV connections, TSV frames are fabricated and bonded to the acoustic transducer chip. Normal chip output is compared to the output from the TSV in the excitation table tests. This simplified testing method allows us to see close estimate of the actual TSV integration. Thus, MEMS resonator devices can be integrated with TSV in cochlear implant application without major drawback. Furthermore, two methods were proposed one of which has the TSV integration and other one does not require TSV connection. Both methods were experimented with the piezoelectric acoustic transducer and the piezoelectric energy harvester chips for FICI application.

In the future study, developed TSV fabrication can be integrated directly into the MEMS resonator fabrication procedure. Cap chips as mean to enclose the chips acting as a lid will be utilized. Further, TSVs can be integrated to the cap chips as another packaging option which does not involve resonator chip fabrication.

Proposed 3D integration solutions in this study can be implemented in variety of different applications that need low weight, flexible, robust integration that can be done under low temperature conditions.

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APPENDICES

A. STS Multiplex Pegasus DRIE Process Recipes

Table A.1. *Santez recipe parameters.*

Parameters	Etch	Passivate
Gas	SF6	C4F8
Duration	7.0	3.0
Flow	600.0	250.0
13.56 MHz Coil Power	4000.0	2500.0
13.56 MHz Platen Power	5.0	0.0

Table A.2. *Structure recipe parameters.*

Parameters	Etch	Passivate
Gas	SF6	C4F8
Duration	2.5	1.5
Flow	375.0	250.0
O2 flow	35.0	0.0
13.56 MHz Coil Power	2200.0	2200.0
13.56 MHz Platen Power	0.0	5.0
380 KHz Platen Power	50.0	0.0

B. Details of Cu Electroplating Solution

Table A.3. *Acid Type Copper Electroplating Solution Properties.*

Temperature (°C)	21.11 - 48.89
Current Density (mA/mm^2)	0.215 – 0.538
Anode	Copper
Anode to cathode ratio	1:1
Agitation	Mechanical
Voltage (V)	4-6
Filtration	Continuous
Plating Tank	Glass, fiberglass, pvc, ceramic, rubber
pH	2.5 - 3.5
pH control	Sulfuric Acid
Deposition rate @ 0.215 mA/mm^2	12.7 µm/hour
Copper concentration (gram/liter)	44.935