OPTIMIZATION OF FABRICATION STEPS FOR N-TYPE c-Si SOLAR CELLS

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ABSTRACT

OPTIMIZATION OF FABRICATION STEPS FOR N-TYPE C-SI SOLAR CELLS

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Crystalline silicon (c-Si) solar cells fabricated on p-type wafers are still dominating the photovoltaic (PV) industry due to advantages in device processing and early focus on p-type cells in the development phase of the industry. Over the years, studies on n-type Czochralski (CZ) substrates have shown that they can be more desirable for the terrestrial applications due to superior material and process advantages such as higher minority carrier lifetime, easier passivation of the surface, absence of light induced degradation (LID) and low sensibility to metallic impurities compared to p-type substrates. With these advantages, n-type CZ based c-Si solar cells with ultimate energy conversion efficiency hold a great potential in the future PV industry.

The goal of this thesis is to optimize boron doping, passivation of boron emitter surface and metallization processes for fabrication of n-type c-Si solar cells. For boron doping, boron trichloride (BCl_3) was used as a gas precursor with LYDOP^{TM} system designed by SEMCO engineering. In order to obtain proper sheet resistance distribution for boron emitter during fabrication, uniformity of borosilicate glass (BSG) formation during high temperature boron diffusion was investigated.

Also, most boron diffusion technologies result in the formation of an undesirable layer at the Si interface which is called as boron-rich layer (BRL). Three different methods were used for removing BRL, namely low temperature oxidation (LTO), chemical etching treatment (CET) and nitric acid oxidation of silicon (NAOS). To fabricate n-type c-Si solar cells, one side of the Si wafer should be protected by a proper masking during the diffusion process. Hence, masking property of silicon dioxide (SiO_2) was investigated for boron diffusion. In addition, to increase the minority carrier lifetime by passivated boron doped surface, aluminum oxide (Al_2O_3) passivation and aluminum oxide/ silicon nitride (Al_2O_3/SiN_x) stack passivation layers were deposited onto surface of the solar cells using atomic layer deposition (ALD) and plasma enhanced chemical vapor deposition (PECVD) techniques. Finally, aluminum was deposited on p^+ emitter by thermal evaporation technique to obtained low contact resistance.

This thesis provides useful information and contributes to research and development activities on the formation of boron emitter that is the most problematic step in the fabrication of high-efficiency n-type c-Si solar cells.

Keywords: Boron doping, Boron-rich layer, N-type solar cell, Passivation, Low-contact resistance.

ÖZ

N-TİPİ KRİSTAL SİLİSYUM GÜNEŞ GÖZESİ ÜRETİMİ İÇİN FABRİKASYON BASAMAKLARININ OPTİMİZASYONU

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Fotovoltaik endüstrisinin gelişim evresinde p-tipi gözelerin üzerine yoğunlaşmasından ve cihaz üretiminde ki avantajlarından dolayı, endüstride p-tipi alttaş üzerine kristal silisyum (c-Si) güneş gözelerinin üretimi halen ağır basmaktadır. Yıllar boyunca, n-tipi CZ (Czochralski) alttaş üzerine yapılan çalışmalar, daha yüksek azınlık taşıyıcı ömrü, yüzeyin daha kolay pasifleştirilmesi, ışık kaynaklı bozulmanın olmaması ve metal kirliliklere karşı düşük duyarlılık gibi yüksek kaliteli malzeme ve işlem avantajlarından dolayı karasal uygulamalar için daha cazip olduğunu göstermiştir. Bu avantajlarla birlikte, temel enerji dönüşümünde çok yüksek verim gösteren n-tipi CZ-tabanlı kristal silisyum güneş gözeleri, endüstrinin geleceğinde büyük bir potansiyele sahiptir.

Bu tezin amacı, n-tipi kristal silisyum güneş gözeleri üretiminde kullanılan, bor katkılama, bor emitör yüzeyini pasifleştirme ve metalizasyon işlemlerini optimize etmektir.Bor katkısı için, SEMCO mühendisliği tarafından tasarlanan LYDOP^{TM} sistemi, BCl_3 öncü gazı ile birlikte kullanılmıştır. Güneş gözesi üretimine uygun olan bor emitör levha direncini elde etmek için, yüksek sıcaklıkta gerçekleşen bor difüzyonu sırasında yüzeyde oluşan borosilikat camın (BSG) homojenliği incelenmiştir. Ayrıca, çoğu bor difüzyon teknolojisi, silisyum arayüzeyinde bor

elementi açısından zengin, istenmeyen bor-zengin katman (BRL) oluşturur. Oluşan bu bor-zengin katmanı çıkarmak için, düşük sıcaklık oksidasyonu (LTO), kimyasal aşındırma işlemi (CET) ve silisyumun nitrik asit oksidasyonu (NAOS) gibi üç farklı yöntem kullanılmıştır. N-tipi kristal silisyum güneş gözesi üretimi için, silisyum diliminin bir yüzü difüzyon işlemi boyunca uygun biçimde maskelenerek korunmalıdır. Bu nedenle bor difüzyon işlemi için SiO_2'nin maskeleme özelliği araştırılmıştır. Buna ek olarak, azınlık taşıyıcı ömrünü, pasifleştirilen bor katkılı yüzey ile arttırmak için, Al_2O_3 pasifleştirme ve Al_2O_3/SiN_x yığın pasifleştirme tabakaları, atomik katman biriktirme (ALD) ve plazma destekli kimyasal buhar biriktirme (PECVD) teknikleri kullanılarak yüzey üzerine kaplanmıştır. Son olarak, düşük kontak direnci elde etmek için alüminyum, termal buharlaştırma yöntemi ile p+ emitör üzerine biriktirilmiştir.

Bu çalışma, n-tipi kristal silisyum güneş gözelerinin üretim süreci için en sorunlu adım olan bor emitörünün oluşumu hakkında yararlı bilgiler sağlamaktadır ve bu tip yüksek verimli güneş gözelerinin araştırılmasına ve geliştirilmesine katkıda bulunmaktadır.

Anahtar Kelimeler: Bor katkılama, Borca-zengin katman, N-tipi güneş gözesi, Pasifleştirme, Düşük kontak direnci.

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CHAPTER 1

INTRODUCTION

Energy is the most significant need for the tomorrows whole. Today, fossil-based fuels such as coal, oil or natural gas are generally used as energy sources. However, these kind of energy sources let off excessive amount of carbon dioxide and other greenhouse gases like methane and nitrous oxide into atmosphere. High emission rate of greenhouse gases to the atmosphere result in global warming and damage our natural life. Beyond this danger, these sources will run out one day. That is to say, they are limited and non-renewable so are not providing long-term solutions to increased global energy consumption. For these reasons, researchers turn towards investigating renewable energy sources like solar energy, wind energy, geothermal energy, etc. to save our environment and discover sustainable energy for the future. Among these renewable energy sources, solar energy is more favored compared to others since it is infinite and easily attainable.

Therefore, there are lots of studies on generating electricity from the sunlight using photovoltaic (PV) technology. Sun provides ample amount of energy that reaches on the Earth in each second in the form of radiation and heat. It is an unlimited energy source and available for free [1]. The power of solar energy originates in nuclear fusion reaction that take place in the sun. The sun consists of gaseous cloud with hydrogen and helium atoms. Due to the high temperature and pressure in the sun, electrons break off their nuclei.

Radiant energy emitted from the sun is called as electromagnetic (EM) energy. In other words, the sun light is in the form of electromagnetic radiation. Depending on its wavelength, electromagnetic radiation can be in different forms like radio waves, microwaves, X-rays and gamma rays (Figure 1-1).

The significant wavelength ranges for solar energy and its applications is from 300 to about 1200 nm. Visible spectrum that can be seen by human eye also falls within this range (400 – 700 nm[2]).

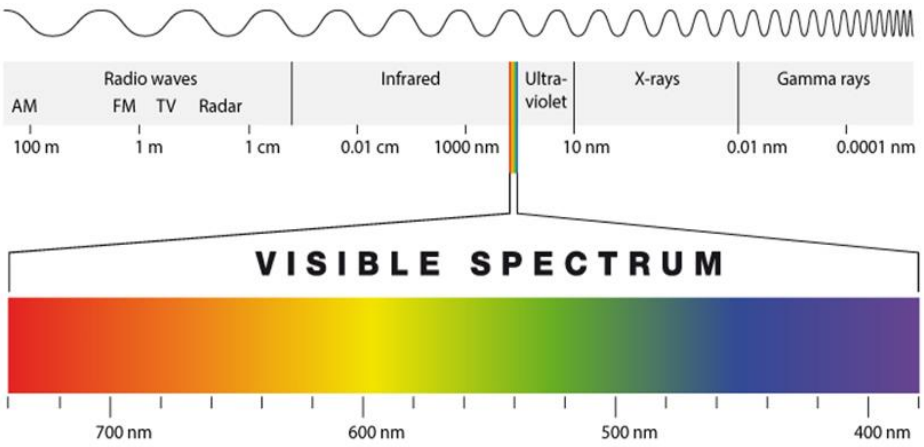


Figure 1-1 Electromagnetic radiation spectrum [2].

In addition to the wave properties, light also exhibit particle-like behavior. These particles are called as photons. They are discrete energy packets with energy levels that differ according to wavelength.

Some observed physical phenomena in solar energy applications cannot be explained easily with the wave properties of radiation. Hence, the energy of particles or photons, bundles of light energy is of great importance. Photon energy is formulated by following equation[3];

$$E = h\nu \qquad \text{(Eq. 1.1)}$$

, where h is the Planck's constant $(6.6256x10^{-34}\ J.s)$ and ν is the frequency. For working principle of photovoltaic device, this photon energy is very important.

The technology that use absorbed photons within semiconductors to generate direct current (DC) is called photovoltaics.

Semiconductor materials, whose conductivity ranges between that of conductors and insulators are utilized for the photovoltaic technology. These materials are found in group IV (elemental) of the periodic table, or they can be a combination of group III and group V (called III-V compound semiconductors), or a combination of group II and group VI (called II-VI compound semiconductors). Silicon (Si), germanium (Ge), gallium arsenide (GaAs) and gallium phosphide (GaP) are some of the most widely used semiconductors.

Among these semiconductors Si is the most preferable material for photovoltaic devices, since it is the most abundant material in the Earth and it has also absorption properties that quite well suited to the solar spectrum. Furthermore, it has different forms such as mono-crystalline, poly-crystalline and amorphous silicon. Mono-crystalline structures are always used in photovoltaic devices because they present the most quotable properties and the highest performance devices[4].

1.1. Motivation

Researchers recently showed that n-type substrates possess some superior properties like better tolerance to metallic impurities (e.g. Fe) and absence of light-induced degradation (LID). These advantages induced a shift in PV industry from p-type substrates to n-type substrates. In addition, according to the International Technology Roadmap for Photovoltaic (ITRP) 2019 results, the use of n-type wafers is foreseen to catch up p-type wafer use in ten years, Figure 1-2.

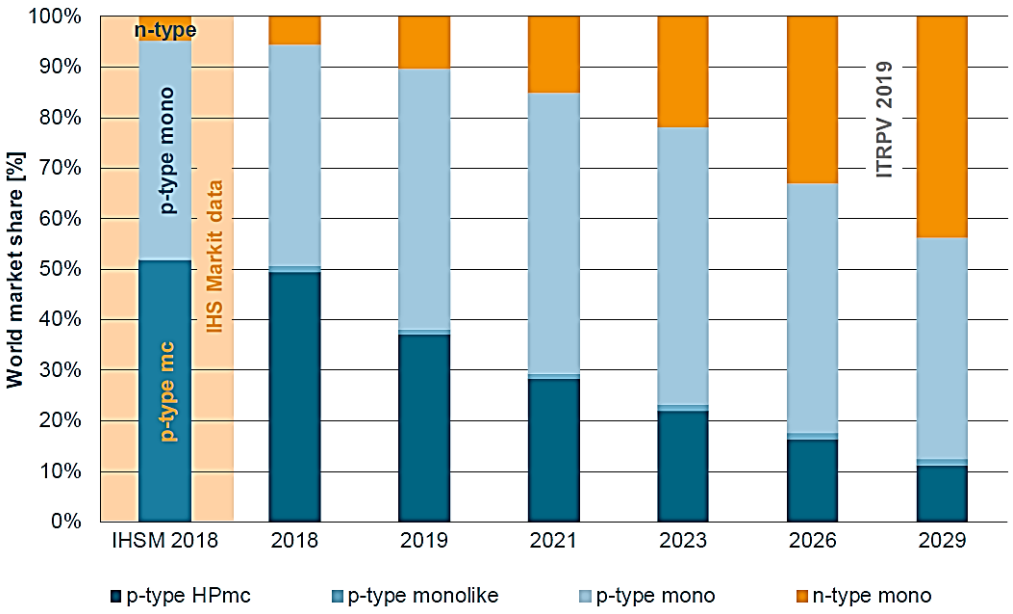


Figure 1-2 Distribution of different types of wafers to be used in solar cell production for the next ten years [5].

Although n-type substrates gain importance in PV applications, fabrication of n-type based solar cells have some intricate process steps such as; B-doping, removal of BRL, passivation of B-emitter and contact formation on p^+ layer.

Formation of uniform B-doped emitter and removal of BRL, which is known to act as recombination centers are very critical steps for the fabrication of high efficiency cells. In addition, the as-cut n-type wafer thickness is constantly decreasing with the aim of more efficiently using Si and reducing the cell cost, as shown in Figure 1-3.

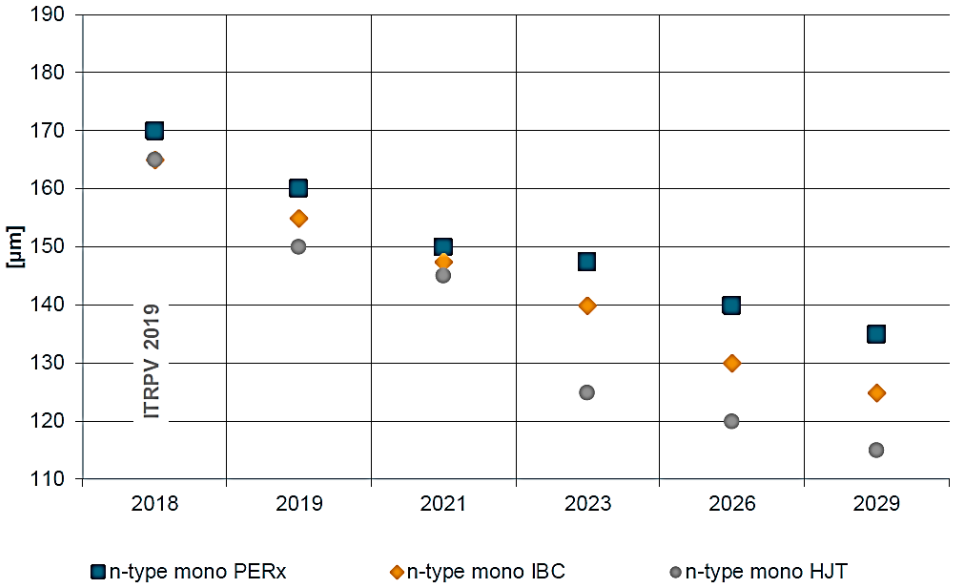


Figure 1-3 Estimated as-cut n-type wafer thickness for the next ten years [5].

Surface recombination of the solar cells increases with decreasing wafer thickness. Hence, surface passivation becomes inevitable to obtain high efficiency n-type solar cells.

Therefore, the aim of this study, is the optimization of fabrication steps of n-type solar cells such as B-doping with BCl_3, removal of BRL, passivation of B-emitter and contact formation.

1.2. Solar Cell Overview

The power generating device, which directly turns incident sunlight into electricity using the photovoltaic effect is called as a solar cell. The basic operation flow of transforming radiant energy to electrical power includes three fundamental steps like absorption of incoming photons, separation of the light-generated electron-hole pairs by the effect of induced electric field and transportation of separated carriers to an external load.

The first step includes absorber materials that are typically semiconductors to take incoming radiant solar energy to produce free electron- hole pairs using absorbed energy to excite its valance electrons. For the second step, p-n junction is the significant element. It is formed by combination of p^+ emitter and n-type substrate region for n-type solar cells. The p-n junction creates a built-in electric field that induces separation of charge carriers and helps for the collection of free carriers. Lastly, the third step is related with the metal grid that can collect electrons and cause the flow of current in the external load, as shown in Figure 1-4.

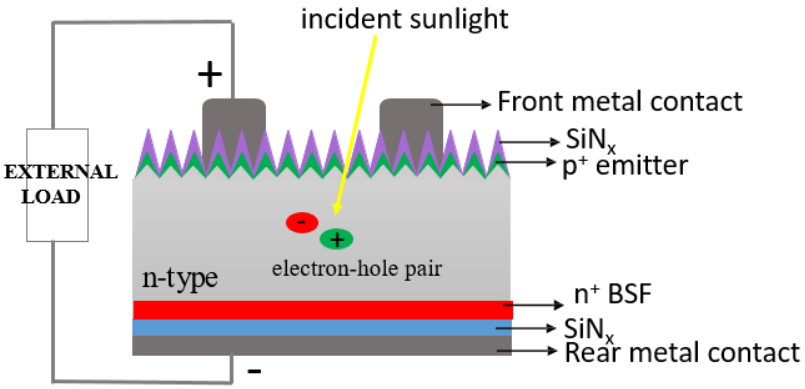


Figure 1-4 Cross section of a simple n-type solar cell.

Figure 1-4 shows a schematic of basic n-type solar cell. It is formed by p^+ emitter on the front side, n^+ back-surface field (BSF) on the back side, silicon nitride (SiN_x) layer on the front and back side for passivation with anti-reflection coatings (ARC) and metal parts on the front and back side for contacts. The heavily phosphorus-doped (n^+) layer on the rear side of n-type solar cell is called as back surface field (BSF). The electric field is generated at the interface of n/n^+ layers due to the carrier density difference that prevents minority carrier flow to the rear contact [6]. Thanks to this barrier effect of BSF, it reduces the back-surface recombination.

Furthermore, SiN_x capping on the front and rear side of the cell improves surface passivation by reducing dangling bond density on the surface of Si. It provides field induced passivation due to its built-in positive charge. In addition to its passivation property, SiN_x also improves the absorption of incoming light and increases the number of electron-hole pairs in the base region.

1.3. p-n Junction

Depending on electron and hole concentrations, there are two types of semiconductor materials that are called as either p- or n-type. Unlike in p-type materials, the electron concentration in n-type materials is more than the holes. Also, they are typically used as a substrate (or base) for all semiconductor based electronic devices. When these two regions come together, p-n joint or junction is formed and electrons diffuse from n- to p-type region and holes diffuse from p- to n-type region under the influence of concentration difference.

Moreover, electrons near the junction jump from n- to p- and holes around the interface pass from p- to n- region. This charge carriers motion results in a space charge region at the junction point, which is called as the depletion region. In the depletion region, electrons remain on the p- side of the junction and holes remain on the n-side of the junction. The induced electric field occurs across the depletion zone from n-type region to the p-type region due to the separated static positive and negative charges. The induced electric field is responsible from the drift current in the junction region.

That is to say, while the concentration gradient is responsible for the diffusion current, induced electric field results in a drift current, as shown in Figure 1-5.

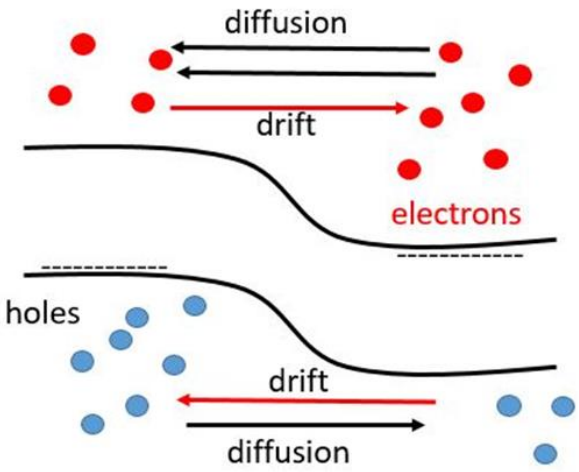


Figure 1-5 Energy band diagram of the p-n junction.

1.4. Incident Solar Irradiance and Air Mass Concept

All energy which comes from the Sun is called as solar radiation and using photovoltaic technology, this radiant energy can be converted into electricity. Solar constant is the power intensity of the solar radiation hitting per unit square of the Earth. It is measured as watts per square meter (W/m^2). The average value of solar irradiance is about 1367 W/m^2 at the outside of the Earth's atmosphere. While solar radiation is coming to the Earth surface, it sustains to Earth's atmosphere that includes air molecules, dust, nitrogen, carbon dioxide, ozone and water vapor. Therefore, solar intensity of the solar radiation decreases while it passes thorough the atmosphere. In other words, solar radiation at the Earth surfaces depend on atmospheric condition and solar altitude.

The ratio of the light travelled path length through the atmosphere to the vertical depth of the atmosphere is called as Air Mass (A.M.).

The formula of the Air Mass is as follows;

$$Air\ Mass = \frac{1}{\cos(\theta)} \qquad \text{(Eq.1.2)}$$

, where θ is the angle between incoming light and normal of the atmosphere surface and it is called as zenith angle. There are three main Air Mass concepts that are AM0 AM1 and AM1.5 as schematically shown in Figure 1-6 [7]. When the zenith angle is equal to 0, the Air Mass is called AM0. While the AM0 condition occurs for the atmosphere, AM1 condition valid at the Earth's surface When light comes with an angle of 48.2°, the condition is called as AM1.5 that is also known as 1.5G (Global). Global includes both direct and diffuse radiation. Furthermore, solar irradiance corresponds to 1000 W/m^2 when AM 1.5G condition is used.

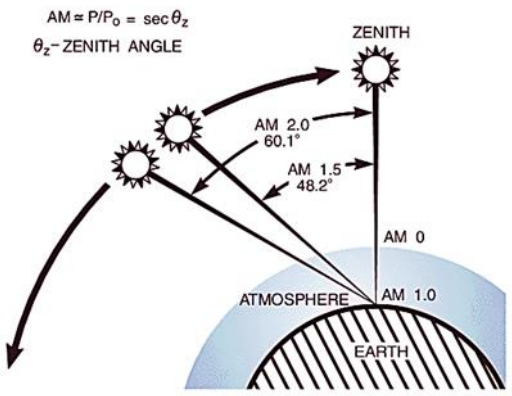


Figure 1-6 Schematic representation of air mass with respect to the zenith angle. [7].

Solar spectrum is generally shown as a function of wavelength. Figure 1-7 shows all AM conditions like AM0, AM1.5 D (Direct) and AM1.5 G, separately.

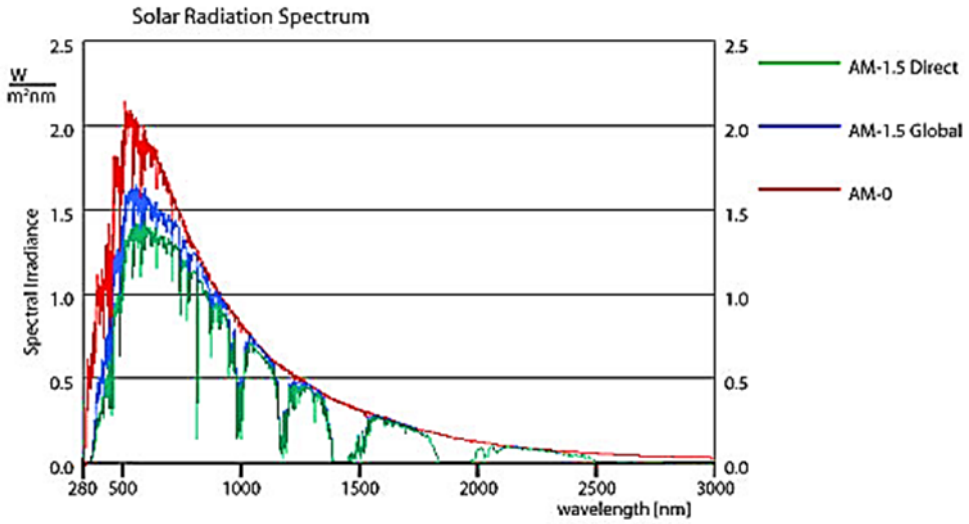


Figure 1-7 Solar spectrum as a function of wavelength [7].

1.5. Fundamental Solar Cell Parameters and I-V Characterization

For the characterization of the fabricated solar cells, some significant cell parameters are used, such as the open circuit voltage (V_{oc}), the short circuit current (I_{sc}) and the fill factor (FF). These parameters can be determined from current-voltage (I-V) curve of cell upon exposure to sunlight [8]. For the dark case, solar cell acts as a diode. Under illumination, the I-V curve shifts up along the y-axis due to the light generated current. The amount of upward shifting depends on the amount of light generated current [9].

For terrestrial applications AM 1.5 (standard incident spectrum) is used for observing illuminated I-V characteristics. Figure 1-8 shows an illuminated I-V curve and power curve of the PV cell.

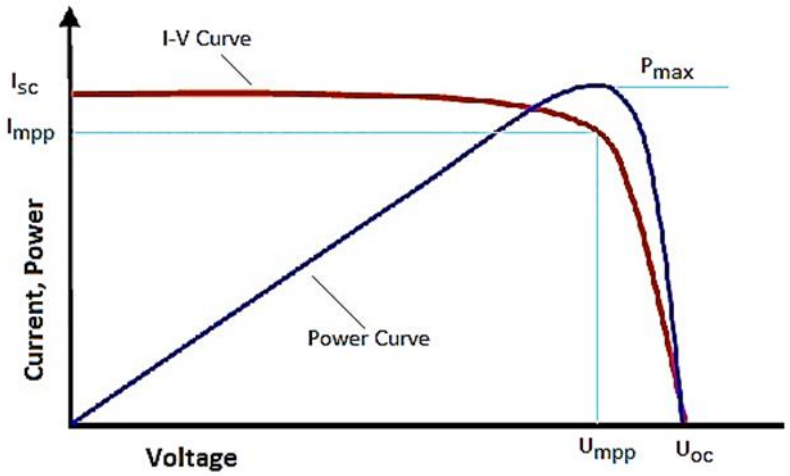


Figure 1-8 Typical I-V characteristics of a solar cell [10].

The I-V curve of the cell can be explained by ideal diode equation given below,

$$I = I_L - I_0\left(e^{\frac{qV}{nkT}} - 1\right) \qquad \text{(Eq.1.3)}$$

The first part of the equation (I_L) represents light generated current that causes upward shifting of the I-V curve along the y-axis. The part of the equation after minus sign is related to dark condition. Hence, I_0 is the saturation current, V is the voltage of the cell, q is the electron charge, k is the Boltzmann constant and lastly, T is the cell temperature in Kelvins.

As shown in Figure 1-8, the open-circuit voltage (V_{OC}) is the maximum voltage value of the PV cell while the current is zero. On the other hand, the short-circuit current (I_{SC}) is the current along the solar cell while the voltage difference is zero. For high efficiency Si-based solar cells, the value of the V_{OC} is between 0.65-0.70 V [11].

Moreover, solar cell produces maximum power at the point maximum power voltage (V_{MP}) and maximum power current (I_{MP}). For an ideal solar cell, V_{MP} equals to V_{OC} and I_{MP} equals to I_{SC}. By using these parameters, fill factor (FF) that is the other important output parameter can be extracted using the equation below,

$$\mathrm{FF} = \frac{\mathrm{V_{mp}\ x\ I_{mp}}}{\mathrm{V_{oc}\ x\ I_{sc}}} \qquad \text{(Eq.1.4)}$$

Fill factor is characterization method of ideality of solar cell. The I-V curve that belongs to ideal solar cell has a rectangular shape. However, the shape of ideal I-V curve changes due to some losses. Fill factor gives significant information about deviation of solar cells from ideality.

The short-circuit current (I_{SC}) depends on some factors like the area of the solar cell, the number of photons, the spectrum of the incident light, the optical properties (absorption and reflection) of the solar cell and the collection probability of the cell. It can be described by the equation given below.

$$I_{SC} = \int_{E_g}^{\infty} q.N_{ph}(\lambda).EQE(\lambda)d\lambda \qquad \text{(Eq.1.5)}$$

,where E_g (1.1eV) is the band gap energy of the Si, N_{ph} is the amount of incoming photon, λ is the wavelength and EQE is the external quantum efficiency which is the ratio of the numbers of charge carriers collected by the PV cell to the number of photons at a given wavelength incoming on the cell. It can be defined as;

$$\frac{EQE}{1 - Reflection - Transmisson} = \frac{electrons/_{sec}}{absorbed\ photons/_{sec}} = IQE \quad \text{(Eq.1.6)}$$

R refers to reflectance. It is the percentage of the light reflected from the cell. IQE is the internal quantum efficiency, that is the ratio of the number of carriers collected by the cell to the number of photons of a given wavelength absorbed by the cell.

For the open-circuit voltage (V_{OC}) expression, the current on the left-side of the E.q.1.3 is set to zero. Then, V_{OC} can be defined as;

$$\mathrm{V_{OC}} = \frac{\mathrm{nkT}}{\mathrm{q}} \ln\left(\frac{\mathrm{I_L}}{\mathrm{I_0}} + 1\right) \quad \text{(Eq.1.7)}$$

$$\mathrm{I_0} = 1.5 \text{ x } 10^5 \exp\left(-\frac{\mathrm{E_g}}{\mathrm{kT}}\right) \quad \text{(Eq.1.8)}$$

The most significant parameter to characterize the fabricated solar cell is the "*energy-conversion efficiency* (η)". It is the ratio of electrical power output (P_{out}) to the incident photon power (P_{in}). It can be defined using the following equation;

$$\eta = \frac{\mathrm{FF.V_{oc.}I_{sc}}}{\mathrm{P_{in}}} = \frac{\mathrm{P_{out}}}{\mathrm{P_{in}}} \quad \text{(Eq.1.9)}$$

Other important output parameters are shunt and series resistances. They are parasitic resistances abbreviated by R_{sh} and R_s, respectively. To understand these parameters, an equivalent electrical circuit for solar cell can be used as shown in Figure 1-9 [12]. Figure illustrates an equivalent circuit containing one diode for PV cell. Shunt resistance (R_{sh}) refers to the leakage current.

It stands against the leakage current along the p-n junction. To obtain a high current value, this parasitic resistance should be high in the PV device. The slope of I-V curve is used for calculation of shunt resistance when voltage is zero.

The fabricated PV device has different resistance types originated from bulk and metal contacts. Series resistance refers to the sum of these resistance

It has an active role on solar cell performance. Series resistance should be low to obtain a cell with high efficiency. For an ideal solar cell, it is zero.

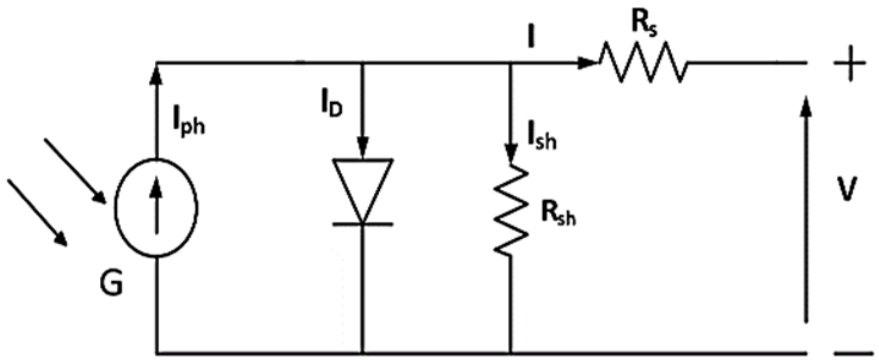


Figure 1-9 Equivalent Circuit of Solar Cell [12].

The ideal diode equation under illumination ((E.q.1.3)) can be expanded as follows;

$$I = I_L - I_0\left(e^{\frac{q(V+I.R_S)}{n.k.T}} - 1\right) - \frac{V + I.R_S}{R_{SH}} \qquad \text{(Eq.1.10)}$$

Here n is the ideality factor that is generally in the range of 1 and 2. Furthermore, I is the terminal current and the other parameters in the Eq.1.10 are the same with the parameters in the Eq.1.3.

CHAPTER 2

N-TYPE SILICON AND BORON EMITTER FORMATION

2.1. Background Information of N-type Silicon

Today, most of the commercial PV cells are generated from p-type substrates, even though the first active solar cell was produced by Darly Chapin, Calvin Souther Fuller and Gerald Pearson interestingly on n-type silicon substrate in 1953 at Bell Laboratories [13]. Smith et al.[14] tried to observe performances of the n-type and p-type solar cells under extraterrestrial radiation. They investigated that n-type base PV cell's performance broke down faster than p-type. Therefore, the PV cell production technology tended to shift from n-type to p-type base after 1960 due to important space program research since p-type substrates have more resistance to the radiation. The other reason for supremacy of p-type based solar cell is easy fabrication procedures like controllable negatively doped emitter formation (phosphorous doping).

Beyond all these advantages of a p-based PV cell, it has some disadvantages like light-induced degradation (LID) and higher sensitivity to metal impurities. The LID is related to boron-oxygen (BO) defects [15, 16, 17]. These defects are activated and act as recombination centers under illumination. Hence, they severely decrease the minority carrier lifetime [18, 19, 20]. The other drawback of p-type substrate is the higher sensitivity to metal impurities. Some common metal impurities like iron are accumulated during crystallization and these can limit the minority carrier lifetime [21].

As the Si PV industry is prone to offer solar cells with improved efficiencies, the quality of base material is progressively gaining importance [22].

Studies on n-type Czochralski (CZ) wafers have shown that it is a very suitable material for terrestrial PV applications with the advantages of higher minority carrier lifetime [23], absence of light-induced degradation and lower sensitivity to metallic impurities when compared to conventional p-type substrates. By virtue of all these advantages, n-type based solar cells have potential to get higher efficiencies.

2.2. An Overview: Boron Emitter Formation

There are two types of semiconductors that are intrinsic and extrinsic. Intrinsic semiconductors have no impurity atoms in their lattice as shown schematically in the left hand side of Figure 2-1 [24]. The electron and hole concentrations of intrinsic semiconductors are equal to each other at room temperature. Hence, conductivity is very low since valance electrons are covalently bonded.

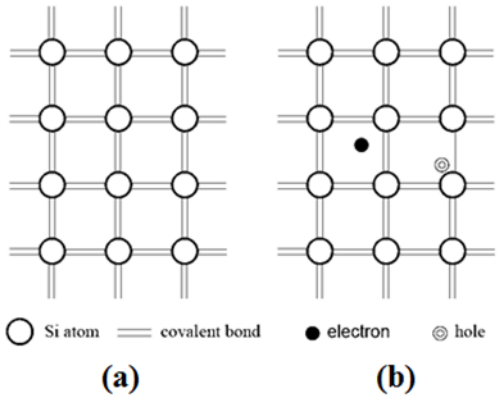


Figure 2-1 Schematic representation of Si crystal lattice with (a) no broken bonds and (b) broken bond and a carrier [24.]

To modify the conductivity of semiconductors, some impurities are introduced into the lattice structure that is called as doping and the doped semiconductors are extrinsic. For n-type Si substrate, the most important doping material is B (3 valance electrons). The number of outer electrons are used to define the type of doping.

When B is utilized for doping, it can catch the one outer electron of Si and leaving a hole in the valance band of Si atoms as shown in Figure 2-2. Therefore, the majority charge carriers will be holes that move in the opposite direction of electrons. Depending on the majority charge carriers, semiconductors are called as p- or n-type. The B doped semiconductors are called as p-type since holes are the majority charge carriers with higher concentration in Si lattice [25]..

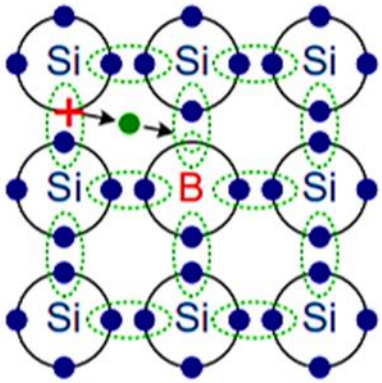


Figure 2-2 B-doped Si lattice structure [25].

B-doped layer is used for two purposes in PV technology. For p-type cell, it is used as back surface field (BSF) while it is utilized as an emitter layer for n-type solar cells. There are some different techniques to form B-doped p^+ emitter layer like thermal diffusion technique [26], ion implantation [27, 28, 29], inkjet printing [30], screen-printing [31, 32], spray-on method [33], spin-on technique [34, 35] and sputtering [36].

Among these techniques, thermal diffusion of B from borosilicate glass (BSG) into the Si substrate is the most preferable and well-known method. Moreover, two important precursors are used for doping process that are boron tribromide (BBr_3) and boron tricloride (BCl_3).

In this thesis, liquid BCl_3 was preferred to create p^+ emitter on the front side of n-type substrate. Thermal diffusion method is performed in the quartz-tube furnace running at low pressures within the 200-600 mbar range. Temperature controlled bottle containing liquid BCl_3 precursor is located on the back side of the diffusion furnace. There are two main steps for diffusion process that are deposition and drive-in steps. For these stages, auxiliary gases are utilized to enhance the doping like nitrogen (N_2) and oxygen (O_2). These gases are injected by two different injectors positioned on the back side of the furnace. To carry BCl_3 vapors through the quartz-tube and distribute it inside the tube homogeneously, N_2 gas is used. At the deposition step, O_2 gas introduced to quartz-tube as the reaction gas. It oxidizes BCl_3 on the surface of the Si wafers at high temperature (900-960 °C) and form boron trioxide (B_2O_3) or boron glass by the equation given below [37];

$$2BCl_3 + \left(\frac{3}{2}\right) O_2 \rightarrow B_2O_3 + 3\,Cl_2 \qquad \text{(Eq.2.1)}$$

B_2O_3 reacts with Si on the Si wafer to create SiO_2 and elemental B or doping element (B);

$$2B_2O_3 + 3Si \rightarrow 4B + 3\,SiO_2 \qquad \text{(Eq.2.2)}$$

The mixture of B_2O_3 and SiO_2 is called as BSG. After uniform deposition of BSG layer on the Si wafer, elemental B diffuse into the Si to create B emitter.

Diffusion process reactions occur at high temperatures since the diffusivity of the B within the Si substrate is very low [38, 39], as shown in Figure 2-3.

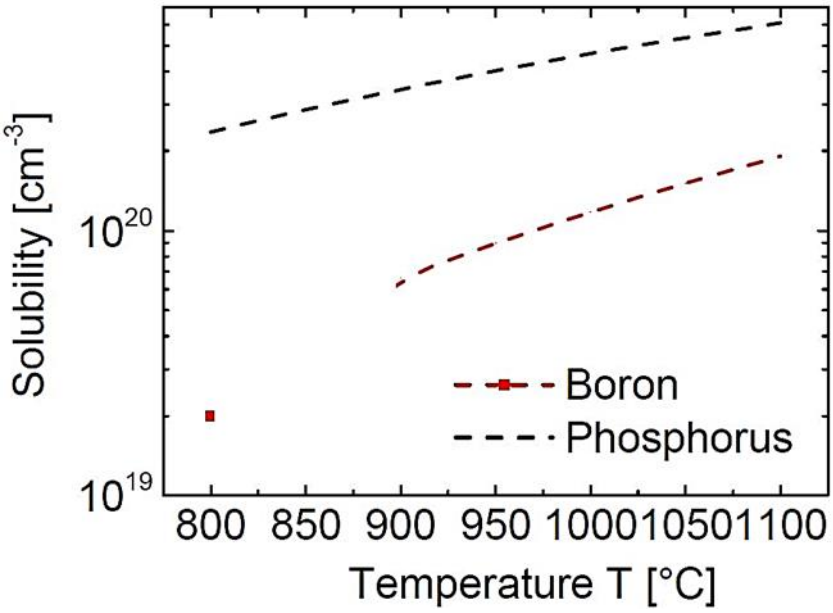


Figure 2-3 Solid solubility of B and P in Si [39].

2.2.1. Characteristics of Boron-Rich Layer

All B-doped emitter forming techniques result in the formation of a boron-rich layer (BRL) between BSG and p^+ region [38], which can inhibit surface passivation and act as a high recombination site due to the inactive B, allocated metal impurities and structural defects. It has also significant effects on the degradation of bulk lifetime due to crystal defects that may occur during cooling-down period considering the thermal expansion differences between BRL and Si [39].

Therefore, removal of BRL is an inevitable step for the fabrication of high efficiency n-type solar cells. Boron-rich layer consists of Si-B compound, as given Equation 2.3 [40, 41, 42];

$$Si + 6\,B \rightarrow SiB_6 \qquad \text{(Eq.2.3)}$$

Chemical compound of BRL was analyzed by researchers in different compositions such as SiB_4 [43]and SiB_5 [41]. However, SiB_6 composition is generally suggested in the literature [44].

The BRL has a hydrophilic surface and is insoluble in hydrofluoric acid (HF). Furthermore, existence of the BRL causes uniform and very low sheet resistance on the doped surface [45]. Therefore, there are two commonly used methods in the literature to remove undesirable BRL that are thermal oxidation [46] and chemical etching treatment [47, 48]. For thermal oxidation technique, in-situ thermal oxidation during the temperature ramp down step in the diffusion process [49, 50] or low-temperature oxidation (LTO) after doping [51] methods are utilized. The other method that is used for the removal of BRL is chemical etching. The chemical mixture that consists of nitric acid (HNO_3), glacial acetic acid (CH_3COOH) and HF is preferred for this technique [52].

Figure 2-4 shows TEM images of the removal of the BRL gradually by the chemical etching treatment. By looking at the TEM images, it can be seen that a 4-minute etching time is enough for the complete remove of BRL as suggested by D.J.Coyle [53].

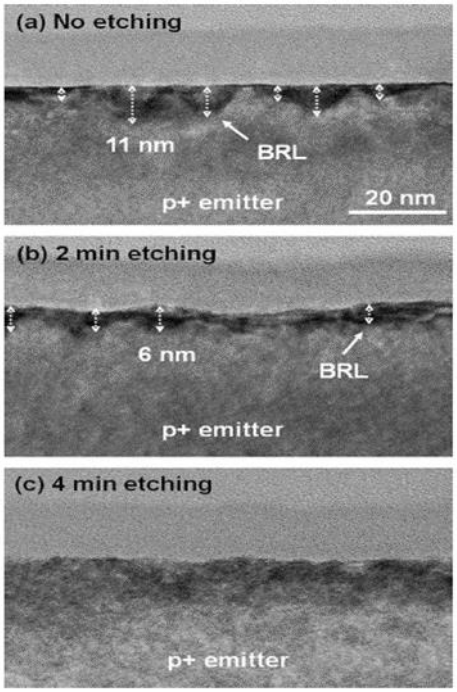


Figure 2-4 Cross-sectional TEM images of B emitter with different etching times of a) reference, b)2 min and c) 4 min [53].

To determine the thickness of BSG and BRL, some different measurement methods are used such as secondary electron microscopy (SEM) [54], atomic force microscopy (AFM) [37], transmission electron microscopy (TEM) [55] and high resolution electron microscopy (HREM) [52].

2.3. Loss Mechanisms

The maximum theoretical efficiency limit for solar cells including a single p-n junction is defined as Shockley-Queisser (SQ) limit. Calculated maximum conversion efficiency is around 33% under AM 1.5 solar spectrum [56]. There are three loss mechanisms reducing the maximum theoretical performance that are optical losses, resistive losses and recombination losses.

The light reflected from the surface of bare Si and metal contacts on the front side of the solar cell cause optical losses. Also, absorption in the metal and the other dielectric layers and the light that passes through the cell without absorption (transmission) result in optical losses. Since photon absorption decreases, the short-circuit current (I_{sc}) decreases due to optical loss mechanisms.

To prevent optical losses and enhance I_{sc}, texturing and anti-reflective coating deposition are preferred in PV industry.

Firstly, texturing process has great importance on absorption of light by solar cells since bare Si has a flat surface and high reflectivity. Texturing forms different surface morphologies on Si surface and provide multiple light interactions with the solar cell surface [57]. For texturing process of single crystalline cell, anisotropic etching utilizing alkali solutions is performed to achieve pyramidal surface morphology on the PV cell. Potassium hydroxide (KOH) solution that is used as alkali solution in the texturing technology has different etching rates for different crystal orientations. Etching results in the formation of pyramid structures randomly on the bare Si surface. Etching rate of the KOH solution for the (111) plane is very low. Hence, only (111) planes (side surfaces of the pyramids) remain on the Si surface that has (100) crystallographic orientation after texturing, as shown schematically in Figure 2-5.

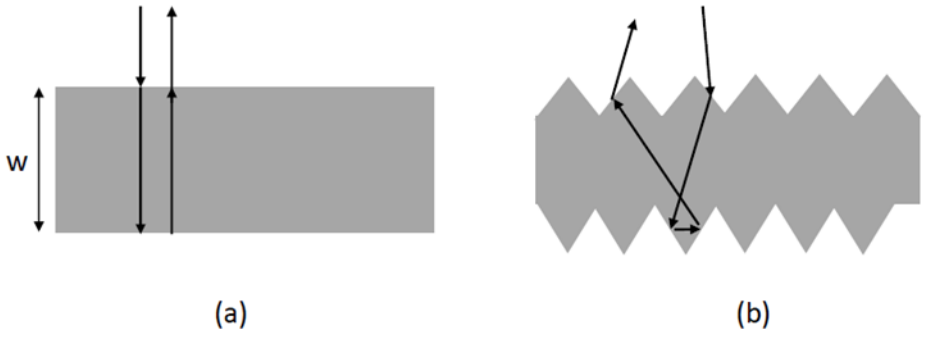


Figure 2-5 Reflection of light from flat (100) surface (a), from textured (111) surface.

The other method to improve I_{sc} is anti-reflective coating (ARC) deposition on the Si surface. Capping textured front side Si surface with silicon nitride (SiNx) enhance the light absorption of a cell. Plasma enhanced chemical vapor deposition (PECVD) technique is utilized for the coating process. It is the well-known and standard process step in industrial fabrication of Si solar cells. The theory depends on the Equation 2.4;

$$d = \frac{\lambda_0}{4n_1} \qquad \text{(Eq.2.4)}$$

, where *d* and *n* are the thickness and the refractive index of the coated SiN_x layer, respectively. λ_0 refers to incident light wavelength. According to Equation 2.4, if the thickness of the coated single SiN_x layer is in the range of the wavelengths of the incident light, the reflectivity is minimum at λ_0. For the standard solar cell, the thickness of the SiN_x layer varies from 70-75 nm with the refractive index is around 2, and this thickness cause blue color on the surface of the solar cell. Moreover, 70-75 nm SiN_x layer provides minimum reflection at around 600-650 nm for incident light [58].

The next loss mechanism apart from optical losses is originated from parasitic shunt (R_{sh}) and series (R_s) resistance and it is called as resistive or ohmic losses. Shunt resistance mostly comes from defects and impurities at or near the junction and it causes shorting of the junction at the cell edges. On the other hand, bulk resistance of the substrate such as, resistance between different conductors and insulators layers and resistance between Si and metal contacts result in series resistance in solar cell operation. All these parasitic resistances have large effects on the fill factor (FF) of the PV cell since high R_s reduce the I_{sc} while low R_{sh} decrease V_{OC} drastically. To obtain high FF and prevent power loss, some models and calculation approaches are used in literature[59].

Lastly, recombination losses limit the cell performance. The photon excited electron that have moved to conduction band from the valance band of a semiconductor, drop back into an empty state (hole) in the valance band. As a result, the e-h pair disappear; this process is called as *recombination*. It is a very significant electronic process in semiconductors [60]. Recombination quantify the *minority carrier lifetime* that is the average time lapse from the point of generation to the recombination of carriers. The carrier lifetime plays a major role on the conversion efficiency of the PV cells. Recombination mechanisms can be investigated in two types that are *bulk recombination* and *surface recombination*.

To get high efficiency solar cells, all these recombination types have to be minimized for increasing minority carrier lifetime.

The bulk recombination can be divided into three physical recombination mechanisms that are radiative, Auger and Shockley-Read-Hall (SRH) recombination. The reverse photogeneration process that release electron energy as a photon called as radiative recombination. It is an intrinsic recombination type like Auger. Auger recombination occurs in highly doped semiconductors. In this recombination mechanism, the excess energy originated from electron-hole recombination is transferred to a second electron. This excited second electron emits a photon due to its relaxation motion to its original position. The last physical recombination type is Shockley-Read Hall (SRH) recombination. It is related to defect states in the semiconductor band-gap. Impurities and crystal defects in semiconductor lattice structure results in the defect states. SRH recombination consists of two-steps due to the defect levels in the forbidden region. This defect level traps the electrons before relaxation to the valance band. For Si, the dominant physical recombination types are Auger and SRH due to its indirect band-gap. All the physical recombination types in bulk can be seen schematically in Figure 2-6.

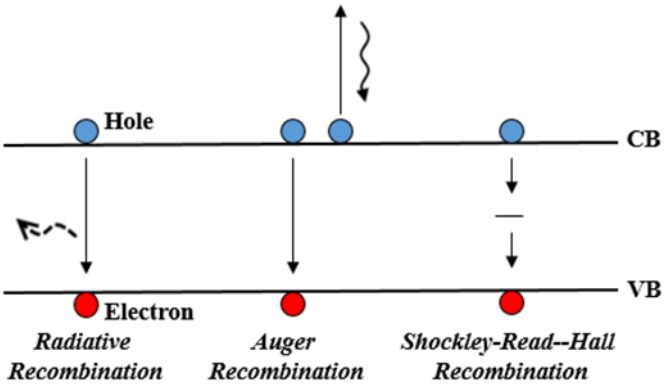


Figure 2-6 Schematic representation of bulk recombination mechanisms.

All these bulk recombination types effect the overall lifetime of the material, so while calculating bulk lifetime, all of them have to be taken in the account. Below equation shows calculation of bulk lifetime;

$$\frac{1}{\mathrm{T}_{bulk}} = \frac{1}{\mathrm{T}_{radiative}} + \frac{1}{\mathrm{T}_{SRH}} + \frac{1}{\mathrm{T}_{Auger}} \qquad \text{(Eq. 2.5)}$$

Table 2-1 shows summary of the bulk recombination mechanisms and affected parameters of solar cell operation.

Table 2-1 Loss mechanisms and affected parameter.

Loss mechanism	Affected Parameter
Optical Losses	I_{sc}
Recombination Losses	V_{oc},I_{sc}
Ohmic Losses	FF

Different from the bulk recombination mechanisms, the surface of the substrate also acts as a recombination center and the concept is called as *surface recombination*. It is resulted from unsatisfied dangling bonds at the surface of the crystal.

The function of surface state density and cross section of surface traps is defined as *surface recombination velocity* (SRV) and it is used for characterization of surface recombination [61]. *The effective lifetime* (T_{eff}) takes into account all four recombination mechanisms and expressed by;

$$\frac{1}{T_{eff}} = \frac{1}{T_{radiative}} + \frac{1}{T_{SRH}} + \frac{1}{T_{Auger}} + \frac{1}{T_{surface}} \qquad \text{(Eq. 2.6)}$$

The surface recombination part of the Equation 2.6 can be calculated by;

$$\frac{1}{T_{surface}} = \frac{2s}{d} \qquad \text{(Eq. 2.7)}$$

,where s is the surface recombination velocity (SRV) and d is the substrate thickness. For photovoltaic industry, the use of thin wafers is preferable for cost reduction. However, there is a trade-off between thickness of the substrate and surface recombination according to Equation 2.7. Thinner substrates experience higher surface recombination. Hence to fabricate solar cells with high efficiency, passivation of front and back surface of the solar cell is gaining importance in PV technology.

2.4. Passivation of B-doped Emitter

During the wafer slicing process from the ingot, the covalent Si-Si bonds are broken at the surface of the Si substrate. These broken bonds are defined as dangling bonds (non-saturated bonds) that cause surface states in the forbidden region and electrons and holes are easily trapped in this energy states which are located near mid-gap. To keep the losses originated from surface recombination at a tolerable level, passivation process must be performed.

It is known that SRV of the defect zones has very big effect on limiting solar cell efficiency [62]. Therefore, surface passivation process is very significant step for the fabrication of solar cells with high efficiency.

There are two fundamental passivation principles generally used together to reduce SRV in PV industry. They are *chemical passivation* and *field effect passivation* [62].

The *chemical passivation technique* is related to saturation of dangling bonds at the surface by capping the surface with a dielectric layer or amorphous silicon. Annealing technique with hydrogen gas is also utilized for chemical passivation. Additional hydrogen atoms are introduced to the surface to reduce the dangling bond density during annealing process [63]. The materials like SiN_x [64], thermally-grown silicon dioxide (SiO_2) [65] and aluminum oxide (Al_2O_3) [66] can be used for chemical passivation. Some of these materials are used as stacks (i.e. SiN_x/SiO_2 [67], Al_2O_3/SiN_x [68]) to achieve better passivation.

The second passivation principle is *field effect passivation*. This passivation technique originates from fixed charges of the dielectric layer or the dopant gradient. These fixed charges act as a BSF and creates internal electric field. Depending on the types of fixed charge (positive or negative) and the emitter (p or n), this built-in electric field repels one type of carriers from the surface and reduce SRH recombination and SRV.

For boron emitter (p-type), Al_2O_3 is usually preferred as a negatively charged dielectric layer [69, 70]. Boron emitter has negative charges (electrons) as minority carriers so using negatively charged dielectric layer for the passivation keeps electrons away from the surface and enhance the passivation. Unlike Al_2O_3, SiO_2 and SiN_x have positive fixed charges so their passivation effect on boron emitter is poor. They are commonly used for passivation of n-type emitters. Atomic layer deposition (ALD) method is used for coating Al_2O_3 on the surface. After coating process, it needs annealing process under N_2 gas for the activation of Al_2O_3. Although it causes an extra thermal activation step for fabrication, it gives excellent passivation results.

2.5. Contact Formation on Boron Doped Emitter

Formation of metal contacts on the front and back surfaces of the solar cell is very crucial part of the fabrication process for the collect electrical power from the PV cell. Typical metallization techniques include thermal evaporation and screen printing etc. Screen printing method; however, is highly utilized in industry because it is a simple, well-known, high-throughput and low-cost method. There are some parameters to determine the quality of the metallization like contact resistivity between the metal and the emitter, the line resistance of the contacts, the aspect ratio and the shadow factor. For high-quality contact formation, all these parameters are to be minimized.

There are two contact types to occur when a metal and a semiconductor is joined. They are Schottky junction (rectifying contact) and Ohmic contact (non-rectifying contact). The difference between the work functions of metal and semiconductor determines the contact type. The work function has a specific value for each material and it is equal to the energy difference between vacuum level and Fermi level of the material. Figure 2-7 schematically shows Schottky contact formation between a metal and n-type semiconductor. The work function of the metal and semiconductor are depicted as $q\Phi_m$ and $q\Phi_s$, respectively. For the case that the metal has higher work function than the semiconductor, the Schottky barrier ($q\Phi_B$) forms at the contact region as illustrated in Figure 2-7. A Schottky barrier is a potential barrier for electrons. Depending on the combination of metal and semiconductor, the value of the barrier ($q\Phi_B$) changes. The barrier can be predicted by Schottky- Mott rule that depend on the difference between the work functions of the metal ($q\Phi_m$) and electron affinity of the semiconductor ($q\ \chi$). Due to the fermi level pinning effect originated from metal-induced gap states and their occupation by electrons, the value of the semiconductor and metal work functions does not have a big role on the heights of the Schottky barriers, in opposition to the Schottky-Mott rule. In this contact type, the flow of the carriers occurs in one direction due to the high resistance rectifying contact arising from Fermi energy level differences between metal and semiconductor.

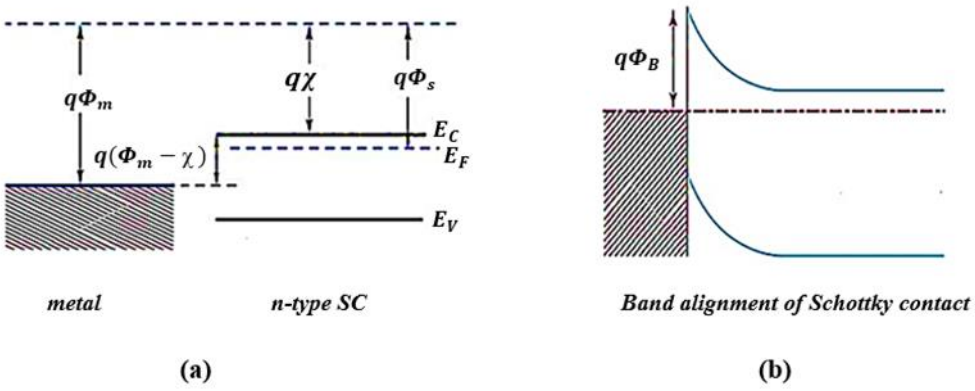


Figure 2-7 Band diagram a) before and b) after Schottky contact formation between a metal and n-type semiconductor.

Figure 2-8 shows forward and reverse bias condition of the Schottky contact. For the forward bias case of Schottky contact, the built-in potential barrier is reduced proportional to the applied voltage. Hence, electrons can move from semiconductor to metal easily due to higher electron concentration in the semiconductor.

When reverse bias is applied to the rectifying contact, the built-in potential barrier is enlarged by the additional applied potential.

Therefore, very few electrons in semiconductor can manage to pass towards the metal side and this electron flow is called as reverse saturation current.

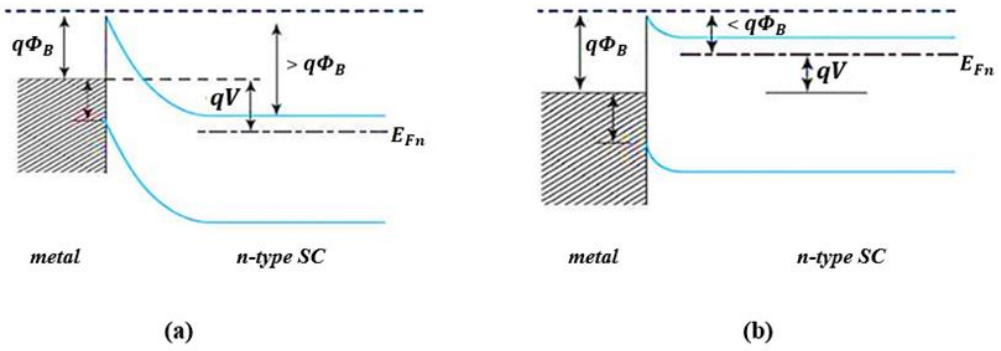


Figure 2-8 Schottky junction a) under reverse bias and b) under forward bias.

The other contact type is ohmic (non-rectifying) contact. It is a low resistance junction and provide current conduction from metal to semiconductor and vice versa. Unlike Schottky contact, current flow in both directions is allowed with low contact resistance. Due to its negligible contact resistance, ohmic contact shows linear I-V characteristics and it is more preferable for PV devices. For the case of ohmic contact formation, the work function of semiconductor must be larger than that of metal as can be seen in Figure 2-9.

It is not possible to get non-rectifying contact by a standard fabrication process in industrially since this contact can only be obtained from heavily doped regions.

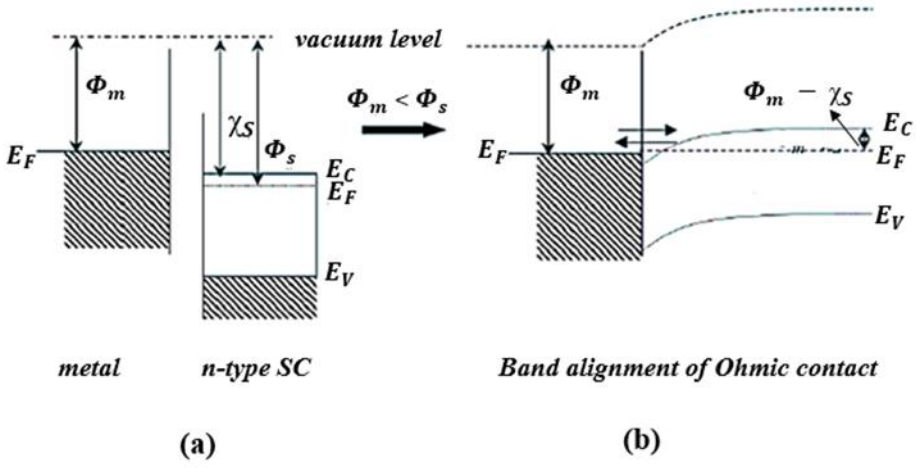


Figure 2-9 Ohmic contact formation.

The Schottky junction can be also utilized to solve fabrication problem of ohmic contact. The built-in potential barrier can be surpassed by increasing the doping concentration. The higher doping concentration results in reduction of the width of depletion region forming at the metal-semiconductor (MS) junction. The tunneling current will flow through decreased width of the depletion region [71]. By this way, low contact resistance can be obtained although built-in Schottky barrier exists at the MS junction.

However, heavily doped regions depict high recombination rate that degrades the solar cell efficiency, so it is not desirable for PV industry. To partly solve this problem, selective emitter technology is used as a new approach [72].

Aluminum (Al) is the common metal used for the standard solar cell structure. However, even though it is a good metal for ohmic contact for p^+ layers, it is not a good electrical conductor. To solve low electrical conductivity issue of Al, mixed aluminum/silver (Al/Ag) pastes are used within screen-printing technology. The aim of this mixed metal pastes technology is taking advantage of the good ohmic contact property of the Al and high electrical conductivity of Ag [73].

CHAPTER 3

EXPERIMENTS

In this chapter, the fabrication steps of n-type solar cells that were carried out in GÜNAM is discussed. Moreover, devices used in fabrication processes and the characterization techniques are detailed in this section. The process flow is shown in Figure 3-1.

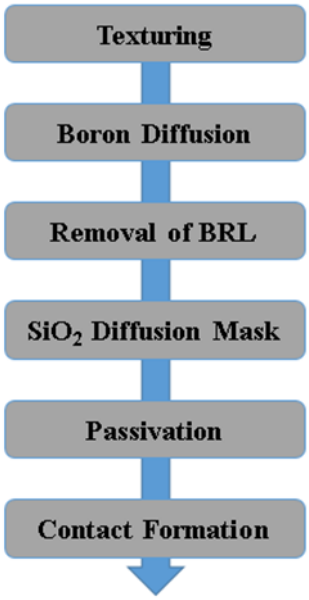


Figure 3-1 Process flow of the experiment.

3.1. Texturing Experiment

In this study, 200 μm thick 156 mm square n-type mono crystalline Si wafers with a resistivity of 1-3 ohm.cm was used. There are two texturing methods that are alkaline and organic texturing processes. The mixture of the potassium hydroxide (KOH) and deionized water (DI) solution is common for both texturing methods. The difference between them is that while alkaline process includes IPA solution the organic texturing recipe use alka-tex solution. Moreover, organic texturing solution can be utilized for more than one cassette. Hence, IPA free KOH solution was used in our experiments to reduce the chemical use.

Before starting the texturing process, 2 minutes HF/HCl dipping was carried out for the samples to remove very thin oxide layer on the surface of the samples. The solution concentration was 5:5:1 (HF: HCl: DI water. Afterwards, samples were rinsed 2 minutes with DI water.

For the organic texturing process, firstly, 1 kg granular KOH was added to 26-liter DI water to initiate the KOH bath, which was heated to 80 °C. Then, 100 ml alka-tex organic solution was added into the heated KOH bath ultrasonic agitation. After a while, samples were immersed in the KOH bath for 20 minutes with the help of a teflon holder. 20 minutes was enough for each cassette (25 samples) to obtain textured surfaces. Table 3-1 shows IPA free texturing process recipe used in this work.

Table 3-1 IPA-free texturing process.

IPA-free Texturing Recipe			
Solution Content	**DI Water**	**KOH**	**Alka-tex**
Quantity	26 lt	1 kg (granular)	100 ml
Temperature		80 °C	
Process Time		20 minutes	

After texturing process, standard RCA 1 and RCA 2 processes have been performed to clean the remaining impurities. For RCA 1 cleaning process, ammonium hydroxide (NH_4OH), hydrogen peroxide (H_2O_2) and DI water solution was used. RCA 2 solution, on the other hand, consisted of hydrogen chloride (HCl), H_2O_2 and DI water. At the end of the process, samples were immersed into HF bath and then rinsed with DI water, which helped to remove the oxide layer formed during the RCA cleaning processes. The recipes of the cleaning processes are tabulated and provided in Table 3-2 and Table 3-3.

Table 3-2 RCA 1 cleaning process recipe.

RCA 1 cleaning Recipe			
Solution Content	**DI Water**	**NH_4OH**	**H_2O_2**
Quantity	13 lt	500 ml	500 ml
Temperature		75 °C	
Process Time		10 minutes	

Table 3-3 RCA 2 cleaning process recipe.

RCA 2 cleaning Recipe			
Solution Content	**DI Water**	**HCl**	**H_2O_2**
Quantity	13 lt	500 ml	500 ml
Temperature		75 C	
Process Time		10 minutes	

3.1.1. Reflection Measurement

Absorption of a solar cell is very important in obtaining high device efficiency. Texturing and anti-reflective coating processes are utilized to reduce reflection and increase absorption. To characterize the absorption quality of the surface, reflection measurements are preferred.

The setup used for the reflection measurements compose of a light source, chopper, integrating sphere, monochromator, lens, photodetector and lock-in amplifier, as shown in Figure 3-2.

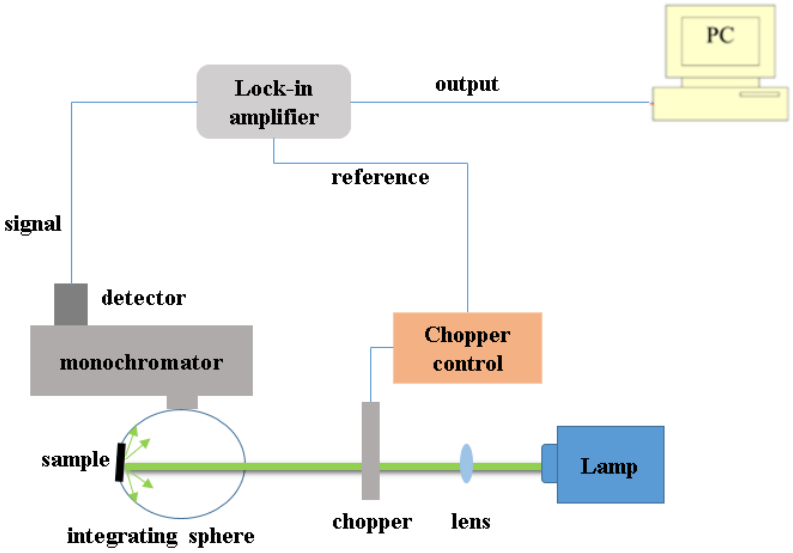


Figure 3-2 The setup used for the reflection measurements.

Textured surface includes two types of reflection that are specular and diffuse reflections. Hence, the reflection measurements were performed using an integrating sphere to collect both reflection types.

Halogen lamp is used as the light source. Collimated light was directed onto the surface of the sample that was mounted in the other edge of the integrating sphere. The holder has angled posture to provide multiple reflections in the integrating sphere.

Monochromatic has input slit positioned on the integrating sphere and the diffused light enters from this input. Also, it has output slit attached to the photodetector that takes diffused light from the monochromatic. The chopper providing modulation of the light beam is positioned in front of the halogen lamp. The wavelength range for the measurements were 300-1100 nm. To obtain total reflection of the samples, two measurements were performed. The first one was taken from the calibration disk. It is the reference sample used for complete reflection. The other measurement is carried out for the dark measurement and no sample is used during the measurement. The formula of the total reflection is given as;

$$Total\ Reflection = \frac{measured - dark}{calibration - dark} \qquad \text{(Eq. 3.1)}$$

3.2. Boron Diffusion Experiment

B diffusion was carried out for textured and cleaned n-type square wafers. In this study, uniformly doped B emitter layer was formed using LYDOP^{TM} system, which enabled to reduce total gas consumption and improved the doping homogeneity across the wafer and the batch to batch variation. In addition, more extensive control was provided on the doping gas flow rate by utilizing BCl_3 as a gas source. The aim of the study was to optimize the B diffusion recipe and to obtain a uniformly doped surface. Figure 3-3 shows the schematic of the furnace used in experiments.

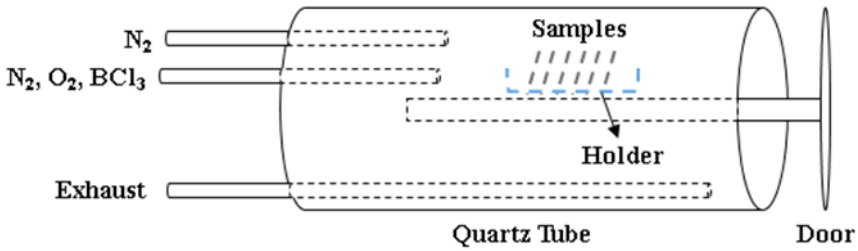


Figure 3-3 Schematic of Boron diffusion furnace.

Diffusion processes were performed under vacuum at 940 °C. Three inlets were located on the back side of the quartz tube. Two of them did belong to the precursor gases for the diffusion process and the third one was the exhaust line. BCl_3 was used as a dopant source. N_2 and O_2 gases were auxiliary gases for diffusion. N_2 gas utilized for transporting BCl_3 to the furnace was called as N_2 carrier. N_2 gas was also used to get uniform gas distribution inside the quartz tube. Lastly, O_2 gas played an important role on the creation of a uniform diffused layer. It oxidized the BCl_3 and helped for the drive-in step.

At the end of the doping process, p^+ layer was formed on both sides of the samples as schematically shown in Figure 3-4.

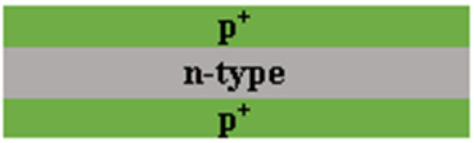
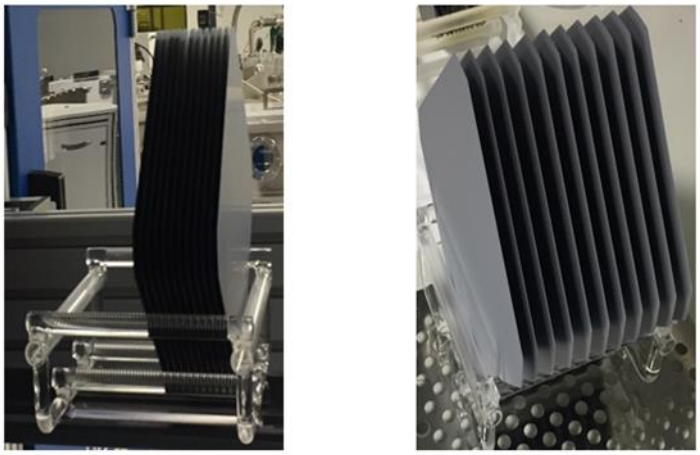


Figure 3-4 B-doped n-type silicon.

During the doping experiments, it was noticed that the sheet resistance changes between the front side (the surface looking to door side of the furnace) and back side (the surface looking to gas side of the furnace) of the samples.

The sorting of the n-type samples on the quartz holder is thought as a reason of this effect. Hence, the effect of different sorting styles was investigated.

In particular, one (standard sorting style) and four (new sorting style) spaces between the samples were investigated as shown in Figure 3-5. After diffusion processes, sheet resistance measurements were carried out for both front and back surfaces of the samples.



(a) (b)

Figure 3-5 Sorting types of n-type samples before doping process a) standard sorting b) new sorting style.

3.2.1. Sheet Resistance Measurement

Sheet resistance value helps us to understand the doping density and resistivity and the homogeneity of the doped surface. It is a measure of resistance of thin films that are nominally uniform in thickness.

The common method utilized for measuring the sheet resistance is four-point probe (4PP) technique. This measurement technique gives the resistivity of the substrate and impurity concentration can be estimated from the resistivity. The theory of 4 PP measurement technique based on four probes touching to the surface of the sample. The distance between these probes is equal. The outer two probes inject the current while the inner two probes measure the voltage as shown in Figure 3-6.

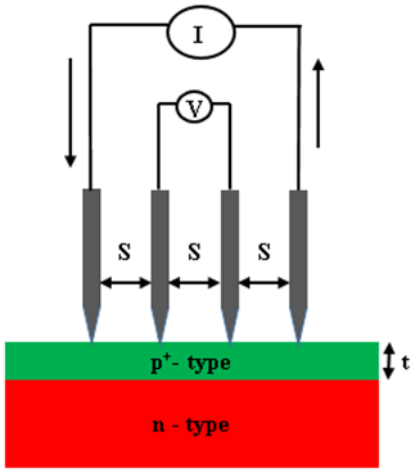


Figure 3-6 The setup of four-point probe technique.

Resistance is measured utilizing Ohm's law. However, the thickness of the substrate must be known. If probes having equal distance with each other placed on an infinite slab material, then the resistivity is given by,

$$\rho = \frac{\pi}{\ln(2)} x \frac{V_{measured}}{I_{applied}} x\ t\ [ohm.cm], for\ t \leqslant \frac{S}{2} \qquad \text{(Eq. 3.2)}$$

, where t is the thickness of the wafer, S is the distance between each probe and I and V are the applied current and measured voltage, respectively.

For bulk resistivity, thickness of the sample is bigger than the spacing of the probes then the sheet resistance is defined as;

$$R_{Sheet} = \frac{\rho}{t} = \frac{\pi}{\ln(2)} x \frac{V_{measured}}{I_{applied}} \left[\Omega/_{sq}\right] \qquad \text{(Eq. 3.3)}$$

3.2.2. Secondary Ion Mass Spectrometer (SIMS) Measurement

The other technique used to evaluate boron diffused surface is Secondary Ion Mass Spectrometry (SIMS). It is generally utilized to investigate the impurity concentration of the doped layer. This measurement technique based on the charged particles (secondary ions) (in the energy range of 5-20 keV). They are emitted from the surface of the sample when the surface is bombarded with energetic primary particles (in the energy range of 0.2-30 keV). The primary particles can be electrons, ions, neutrals and photons.

The primary ion beam interacts with the surface of the sample under vacuum. The use of positively charged ions as primary ions cause generation of negatively charged ions. When negatively charged ions are preferred as primary ions, then positively charged ions form in the system. A simple schematic of the SIMS method is provided in Figure 3-7.

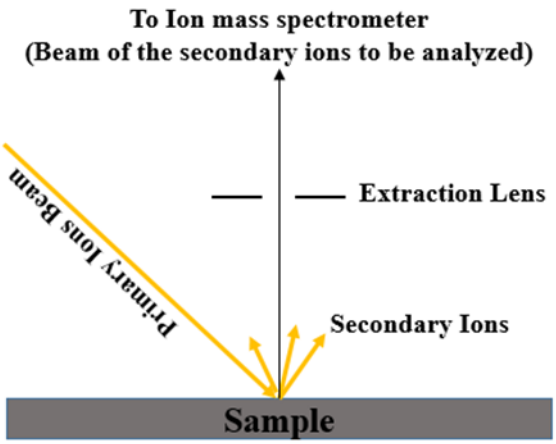


Figure 3-7 Simple schematic of SIMS method.

There two modes for SIMS measurement that are dynamic (DSIMS) and static (SSIMS). In dynamic mode, primary ion beams exceed the static limit (~ 1 E12 ions/cm^2) so it has high sputtering rate. It is used for bulk analyses of element or isotopes. In other words, it detects trace impurities in the samples. For the depth profiling of elements, this mode of SIMS is preferred. The static mode of SIMS gives information about the top monolayer of the sample and it is used for thin samples and organic materials. It needs much lower energy for primary ion beam (usually Ga or Cs)

3.3. Removal of Boron-Rich Layer (BRL) Experiment

For the desirable and uniform B emitter formation, the BRL must be removed or etched because it is known to act as high recombination site and can interfere with surface passivation. Also, it causes very high surface concentration after doping process. It is located between the BSG and doped layer as shown in Figure 3-8. There isn't standard thickness for the BRL and BSG. Generally, O_2 and N_2 gases flow used in diffusion process determine the thickness of these layers [74, 75].

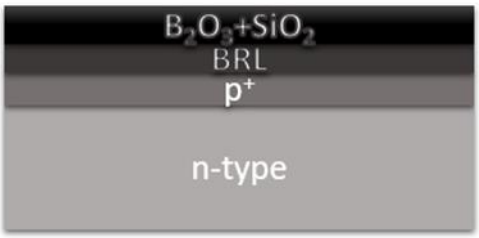


Figure 3-8 Schematic of position of the BRL.

Some methods are utilized to remove unwanted BRL without damaging p^+ emitter. These methods are ex-situ low temperature oxidation (LTO) and chemical etching treatment (CET).

3.3.1. Low Temperature Oxidation

For the low temperature oxidation process, the B diffusion furnace was used. Ex-situ oxidation technique was conducted at 800 °C in this study. The B doped samples were oxidized after doping process. H_2, O_2 and N_2 gasses were used for the oxidation. The oxidation type used in the study is pyrogenic oxidation that is a kind of wet oxidation. In this oxidation type, H_2 and O_2 gasses are injected to the quartz tube and form H_2O vapor inside the tube as shown in Figure 3-9. The extension rate of pyrogenic oxide is and the oxide thickness is larger compared to dry oxidation. Also, it reduces oxide contamination because of carry-over of fast-ions from the source. The equation of the wet oxidation is given as follows,

$$Si(s) + 2H_2O(g) \rightarrow SiO_2(s) + 2H_2(g) \qquad \text{(Eq. 3.4)}$$

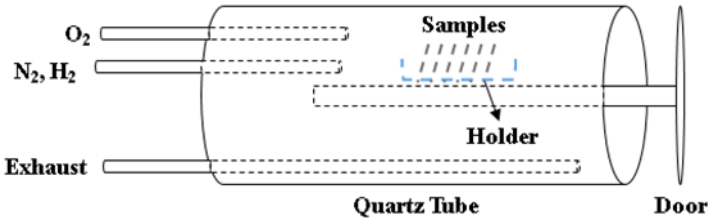


Figure 3-9 Boron diffusion furnace used for the thermal oxidation.

The theory of the BRL removal with the deposited oxide layer on the doped Si surface is based on the kinetics of the oxide extension. The reaction occurs at the Si-SiO_2 interface. When the formation of SiO_2 layer is completed, almost 46 % of the oxide layer penetrates within the substrate, while 54 % of the layer extends on the top of the substrate surface as seen in Figure 3-10. The penetrating part of the oxide layer oxidizes the BRL and makes the removal of it easier with hydrofluoric acid (HF).

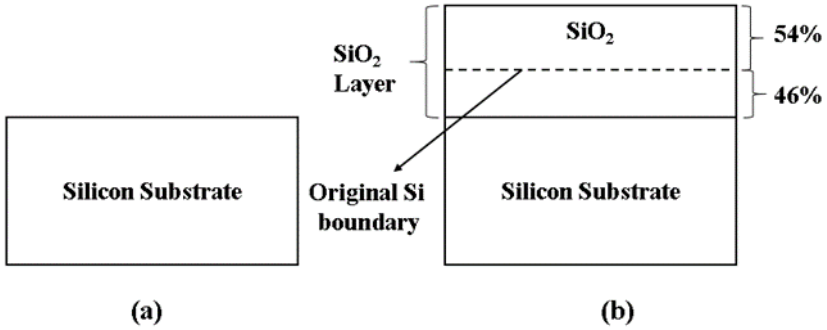


Figure 3-10 Thermal oxidation a) before SiO_2 and b) after SiO_2 extension.

For this experiment, RCA cleaning processes were performed following doping. Then, the oxidation process was carried out for doped and cleaned wafers. SEM analysis was performed to observe the thickness of the BRL. However, the resolution of the SEM was not enough to detect BRL.

Hence, the experiment set including different oxide thicknesses was designed to remove or etch BRL since the exact thickness of it was not known.

Table 3-4 shows experiment sets of the oxidation process applied to oxidize BRL. These thicknesses were determined by checking the oxide thickness (μm) versus oxidation time (minute) graph of the SEMCO technologies company.

Table 3-4 Experiment sets for thermal oxidation technique.

Experiment Sets	Number of Wafer (Quantity)	Thickness of SiO_2 (nm)
Reference	4	0
1.Set	4	25
2.Set	4	50
3.Set	4	100
4.Set	4	150
5.Set	4	200

The 200 μm thick 156 mm square n-type mono crystalline Si wafers with a resistivity of 1-3 ohm.cm doped with BCl_3 using diffusion furnace. Then, the samples were then divided into 6 sets. One of them was set as the reference sample. For each set, different oxide thicknesses such as 25, 50, 100, 150, 200 nm was grown on the p^+ layer. All doped and oxidized wafers were etched by HF to remove BSG and BRL. Then, sheet resistance measurements were performed for one wafer in all sets to observe the uniformity after oxidation and the changing of sheet resistance depending on the oxide thickness. Moreover, one wafer for each set was reserved for the trial of passivation with SiN_x. For remaining two samples for each set were utilized for the optimization of contact formation on B emitter.

For SIMS measurement, the new n-type sample set was prepared for doping process. Standard cleaning process (RCA 1 & RCA 2) after doping was performed for all B-doped n-type samples. Then, oxide layer was grown again with the thicknesses of 25, 50, 100, 150 and 200 nm using LTO technique.

After LTO process, all samples were cleaned with the standard cleaning processes to get them ready for SIMS measurements. All SIMS measurements were conducted by Central Laboratory in METU.

For sending B-doped n-type samples to Fraunhofer Institute for ECV measurements and Central Laboratory to SIMS measurements, one more B doping process was carried out for twenty-four n-type square and six n-type single side polished quarter round wafers as seen in Figure 3-11. For this experiment, the LTO processes were performed with the thickness of 25, 50, 100, 150 and 200 nm for the samples shown in Figure 3-11. Then, SIMS and ECV results of the samples with different etched oxide thickness have been compared with each other.

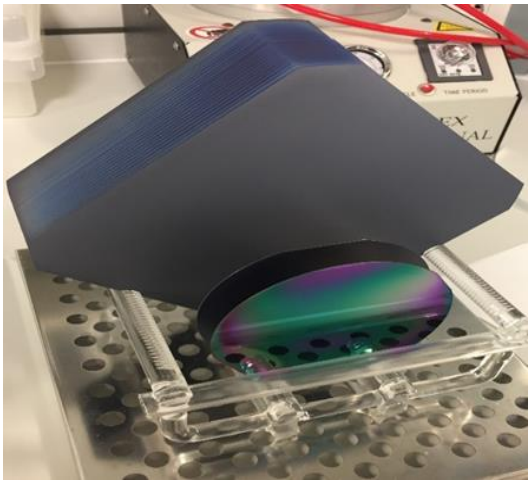


Figure 3-11 Photo of the B-doped Ferrotech CZ n-type and FZ p-type round samples.

3.3.2. Chemical Etching Treatment

The other technique utilized for removal of BRL is chemical etching treatment (CET). Two chemical mixtures with different chemical ratios were prepared to optimize the CET method.

The first chemical mixture consisted of hydrofluoric acid (HF), acetic acid (CH_3COOH) and nitric acid (HNO_3) with the ratio of 1:100:100, respectively. Following doping process, CET method was applied to doped n-type samples for different times from 0 to 10 minutes.

Secondly, the same chemical mixture was used with the ratio (10:100:100) to observe etching rate and optimize the CET method. Then, CET process was applied to boron doped n-type samples for different times from 0 to 10 minutes.

Lastly, CET process was carried out for B-doped and oxidized n-type samples to investigate the effects of etching on the oxidized sample. In this study, SiO_2 was grown on B-doped n-type wafers with oxide thickness 25 and 50 nm by LTO technique. These thicknesses were chosen depending on their sheet resistance from LTO study. After HF dipping, the CET was applied for the oxidized samples. CET process resulted in the formation of undesirable porous Si on the surface.

For this reason, the samples were immersed in 1% KOH (7 lt DI water / 0.07 lt KOH) solution for 8 minutes to remove porous Si. Before measuring the sheet resistance of the samples, they have been placed into HF solution again till they become hydrophobic.

3.4. Silicon dioxide (SiO_2) diffusion mask

For the fabrication of n-type solar cells with $p^+/n/n^+$ structure utilizing diffusion furnace method, the diffusion mask or single-side etching studies must be conducted because both sides of the sample have been doped during the diffusion process.

In this study, SiO_2 was used as a diffusion mask for B. The 200 μm thick 156 mm square n-type mono crystalline Si wafers with (1-3 ohm.cm) resistivity were textured and cleaned for diffusion mask experiment. The oxide layer was grown with the thicknesses of 20, 40, 80, 160 and 320 nm on the surface of the cleaned and textured n-type wafers before performing B diffusion.

For oxidation process, high-temperature oxidation (HTO) method was applied at 900 °C because it has a much higher extension rate than the LTO method due to the higher temperature. Lastly, to prepare samples for sheet resistance measurements, they were dipped into HF solution.

Figure 3-12 shows color-change of the sample depending on the different thicknesses.

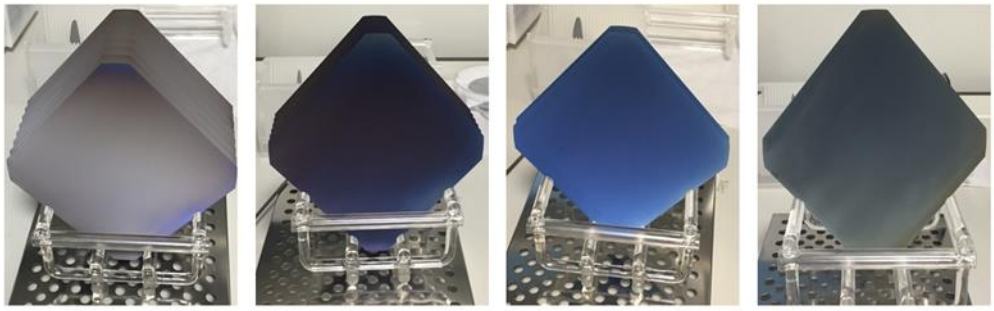


Figure 3-12 Photos of the n-type samples with different oxide thicknesses of a) 20, b) 80, c) 160 and d) 320 nm

The B doping was performed two times because of the changing of the sorting style of the samples located on the quartz holder for B diffusion experiments in order to investigate the masking property of SiO_2. In other words, two B diffusion processes were performed for the samples with different sorting styles on the quartz holder. After diffusion step, all samples were immersed in HF solution to remove the oxide layer. Then, sheet resistances of the samples were measured using 4PP method to evaluate the masking property of SiO_2.

3.5. Passivation of B-doped Emitter Experiment

Passivation step is a very significant part for obtaining solar cells with high efficiency. In this part of thesis studies, the effect of different passivation layers was investigated. Al_2O_3 and Al_2O_3/SiN_x stack layers were used to see the effect of passivation on the minority carrier lifetime.

3.5.1. Al_2O_3 Passivation Layer

The cleaned and double side polished Fraunhofer FZ p-type round wafers (bulk lifetime ~ 1000µs) were used for the passivation experiments. For the passivation of the B emitter, Al_2O_3 deposition was carried out with the ALD technique.

Different temperatures were investigated during Okyay tech. ALD for optimization of the passivation. With different temperatures, two pulse durations that are 15 and 30 milliseconds were applied to optimize the process, as illustrated in Table 3-5. The pulse duration is the time elapse during vapor and precursor injection. Also, Al_2O_3 layer is deposited in cycles in which the surface of the sample is exposed to various vapor and precursor gases. In each cycle, a monolayer of material is deposited. For this trial, the number of cycles was kept constant at 80.

Table 3-5 The applied recipes for Okyay tech. ALD process.

Pulse duration (ms)	**Temperature (°C)**
15	230, 200, 180, 150
30	230, 200, 180, 150

To characterize or understand the quality of the passivation, the lifetime measurements were conducted using Quasi-steady-state photoconductance (QSSPC). Before measuring the lifetime to determine the quality of the passivation, annealing process was performed at 425 °C with H_2-N_2 (1:20) gasses for 30 minutes to activate the Al_2O_3 passivation layer. The measurements were performed before and after activation process to see the effect of activation on the lifetime results.

In the second passivation study trial, cleaned and double side polished Fraunhofer FZ p-type round wafers (bulk lifetime ~ 1000µs) were utilized again. The minimum and maximum temperature of the Okyay tech. ALD system that are 150 and 260 °C were used for process, respectively.

Also, 15 and 10 ms pulse durations were tried for observing passivation quality. All processes consisted of 80 cycles in this trial. These parameters were chosen depending on the lifetime results of the first passivation trial. The parameters used for the second passivation trial are tabulated and provided in Table 3-6.

Table 3-6 The applied recipe for second trial of Okyay tech. ALD process.

Pulse duration (ms)	**Temperature (°C)**
15	150, 260
10	150, 260

The passivation layer was activated with H_2 and N_2 gases at 425 °C. Also, the lifetime measurements were conducted by QSSPC both before and after activation.

The passivation processes including different cycles such as 20, 40, 80 and 160 were carried out in order to determine growth per cycle (GPC) and observe the effect of thickness on lifetime.
In this study, the pulse duration and temperature were kept constant at 15 ms and 150 °C, respectively, depending on the previous tables. The thickness of the Al_2O_3 film was measured using the ellipsometry technique.

The p-type wafers with high bulk lifetime (bulk lifetime ~ 1000μs) were utilized in previous optimization studies. Lastly, the B doped and oxidized n-type square wafers were used with the ALD recipe that revealed the best lifetime results.

The B doping process was performed for four groups, separately. To remove BRL formed during the diffusion process, LTO processes for different oxide thicknesses such as 0, 25, 50 and 100 nm were carried out for four groups of eight samples each.

The shape of the Okyay tech. ALD chamber in where samples were placed was not suitable for square wafers so the doped and oxidized samples were cut in spherical shape with laser prior to passivation process. After ALD process, the minority carrier lifetime of the samples was measured by QSSPC system.

In addition, Solaytec ALD system was used for passivation to see effect of deposition system on lifetime. Different brands of p-type wafers were utilized for Al_2O_3 film deposition. After deposition, different annealing processes were carried out for the activation of passivation layer. Then, the lifetime results have been compared with each other.

3.5.2. Al_2O_3/SiN_x Stack Layer Passivation

The stack layer passivation was investigated to enhance the lifetime of the samples. The B-doped and oxidized n-type wafers were utilized in this experiment. The different etched oxide thicknesses such as 25, 50 and 100 nm were grown on the B-doped samples. The samples were coated with Al_2O_3 using the Okyay tech. ALD system. After ALD process, the surface of the samples was capped with the SiN_x layer practiced using PECVD system to investigate the effect of stack layer on the lifetime.

The minority carrier lifetime of the samples was measured at different stages utilizing QSSPC system. For example, firstly, the lifetime measurement was performed for the Al_2O_3 deposited and activated samples. Then, the same samples were coated with the SiN_x and lifetime measurement was performed again.

Lastly, the second annealing process was carried out for the Al_2O_3 deposited and SiN_x coated samples prior to lifetime measurements. The annealing recipe was the same as the activation process.

In addition, the effect of Al_2O_3 in stack passivation layer and the firing process for Al_2O_3/SiN_x stack layer coated samples were investigated in this experiment.

For this study, six Ferrotech FZ p-type wafers were utilized without doping. The Al_2O_3 layer was deposited with different thicknesses of 4, 8 and 16 nm for each two samples via Okyay tech. ALD system. Then, the samples having different thickness of passivation layer were divided into two groups of three samples in order to apply two different activation recipes. The first recipe was performed using N_2 and H_2 gasses with the ratio of 10000 sccm/500 sccm at 425 °C for 30 minutes. For the other recipe, just N_2 gas with the flow of 10000 sccm was preferred and the process was performed at 550 °C for 10 minutes. The first measurement was performed after activation. Then, the measurement was repeated after capping the Al_2O_3 deposited surface with SiN_x.

Lastly, for the samples with SiN_x/Al_2O_3 stack passivation layer, the firing process was applied at 900 °C prior to lifetime measurements. All these processes were conducted for two different activation recipes.

3.5.3. Quasi-steady-state photoconductance (QSSPC) measurement

For the extraction of the minority carrier lifetime, generally, quasi-steady-state photoconductance technique is preferred. This method determines the minority carrier lifetime from the decay of photo induced conductance [76]. In other words, it analyzes the photoconductance decay transients after very short light pulse from flash lamp or other light sources.

The photoconductance change is defined as follows;

$$\Delta\sigma = qW(\mu_n + \mu_p)\Delta n \qquad \text{(Eq. 3.4)}$$

, where $\Delta\sigma$ is the change in photoconductance, W is the thickness of the sample. μ_n and μ_p are the mobilities of electron and holes, respectively. The QSSPC system calculates the excess charge carrier density from Equation 3.4.

Through the use of excess charge carrier density, *the effective lifetime* is calculated by;

$$\tau_{effective} = \Delta n / d(\Delta n)/dt \quad \text{(Eq. 3.5)}$$

The Equation 3.5 is related to transient measurements. For the case of quasi-steady-state, generation and recombination of the electron-hole pairs must be in balance. Also, photogeneration rate of the excess carriers becomes important in QSSPC case and it must be added to Equation 3.5. Then the effective lifetime equation becomes as follows;

$$\tau_{effective} = \frac{\Delta n}{G - \frac{\partial n}{\partial t}} \quad \text{(Eq. 3.6)}$$

, where, G is the photogeneration rate of the excess carriers and Δn is the photogenerated excess electrons.

Also, the QSSPC system gives the implied open circuit voltage (iV_{oc}). It is the maximum open-circuit voltage (V_{oc}) value that can be reachable in current state of the sample and it can be defined as;

$$\text{iVoc} = \frac{nkT}{q} \ln(\frac{np}{n_i^2}) \quad \text{(Eq. 3.7)}$$

, where *n* and *p* are the total electron and hole concentrations respectively, n_i is the intrinsic carrier density, *k* is the Boltzmann constant and *T* is the absolute temperature of the sample.

For the measurement of all these parameters, Sinton Instruments WCT-120 lifetime tester was utilized, which can be seen in Figure 3-13.

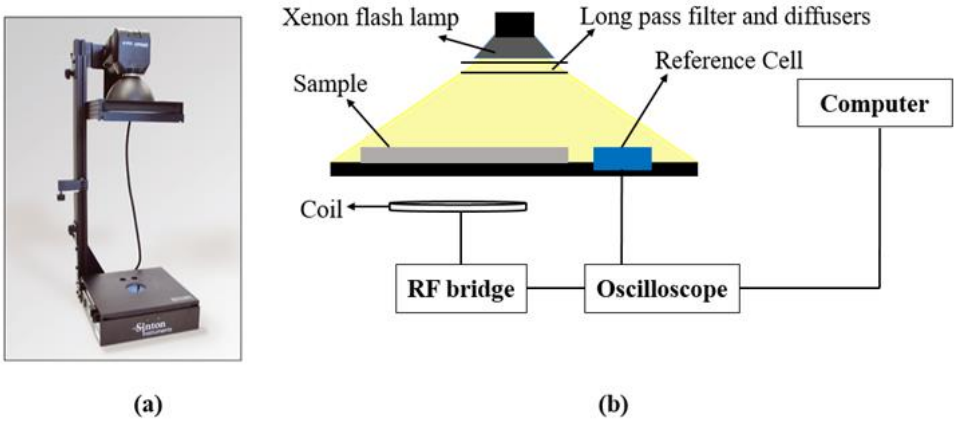


Figure 3-13 a) Image of the Sinton WCT-120 lifetime tester, b) schematics of the measurement setup used in this work.

At the beginning of the measurements, the very short light pulse coming from the flash lamp generates the excess charge carriers and enhance the photoconductance. This phenomenon results in the changing in photoconductance because when the light pulse is over, the photoconductance drops again. For the QSSPC case, the longer flash is preferred in order to keep generation rate constant. The photoconductance values are saved by the coil connected to RF bridge and extracts excess charge carrier density from Equation 3.4 and then calculates the effective lifetime from Equation 3.6

3.6. Contact Formation

In this experiment, the effect of the Al on the contact resistivity has been investigated. For the B doped n-type samples used in experiments, the LTO process has been carried out with different times of 30, 60, 120, 180 and 240 minutes.

Transmission line measurement (TLM) method was utilized for all metalized and fired samples to observe the contact resistivity. For the contact resistivity measurements, TLM mask was designed to be used during metallization process, as shown in Figure 3-14.

Before thermal evaporation process, the mask having grid lines with different distance with each other was adhered on the surface of the samples. The distance between five grid lines was changing from 1 to 4 mm.

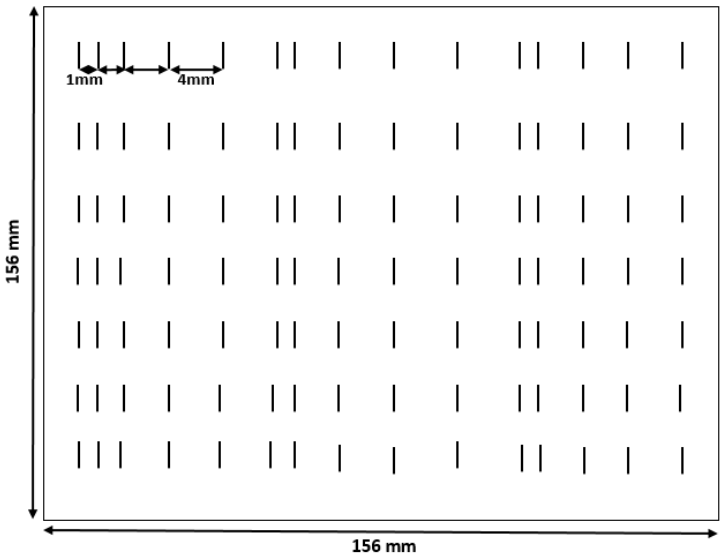


Figure 3-14 Transmission line measurement mask.

After metallization, various firing processes have been performed at three different temperatures consisting of four different sample conveying velocity to optimize the contact formation and get lower contact resistivity. Table 3-7 shows the details of the firing processes.

Table 3-7 Firing processes.

Temperature (°C)	**Conveying velocity (cm/s)**
800	100, 200, 300, 400, 500
850	100, 200, 300, 400, 500
900	100, 200, 300, 400, 500

In order to supply sufficient samples for the different firing process combinations (Table 3-7), the square wafers have been cut using the laser before firing processes in order to have enough sample for all combinations. The cut samples had two rows of five metal grids with different distances between them, as illustrated in Figure 3-15.

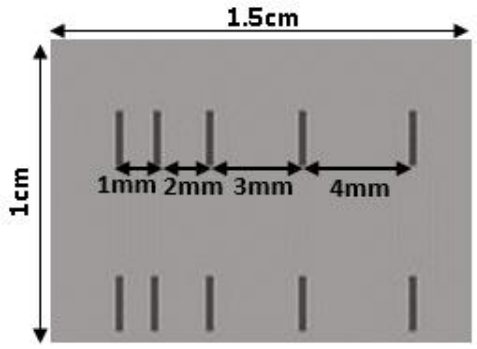


Figure 3-15 The samples for TLM.

For the cut samples, the different firing processes were performed. The metal on the sample surface was run out after firing processes so the thermal evaporation process was carried out, again before TLM measurements. At this time, a small TLM mask was used for the cut samples.

After all these processes, the contact resistivity measurements have been made from the metal grid lines formed on the surface.

3.6.1. Transmission line measurement (TLM) method

TLM method is a common way to be used for determining the contact resistivity. This measurement technique is based on the metal grids or contacts that have different distances with each other on the semiconductor samples. For the case of the current flow towards to the two metal grids on the semiconductor, the total resistance can be defined as Equation 3.8;

$$R_T = 2R_m + 2R_C + R_{Semi} \quad \text{(Eq. 3.8)}$$

, where R_m is the resistance of contact metal, R_C corresponds to metal/semiconductor interface, the R_{Semi} is resistance of the semiconductor and R_T is the total resistance. Figure 3-16 shows the case of Equation 3.8.

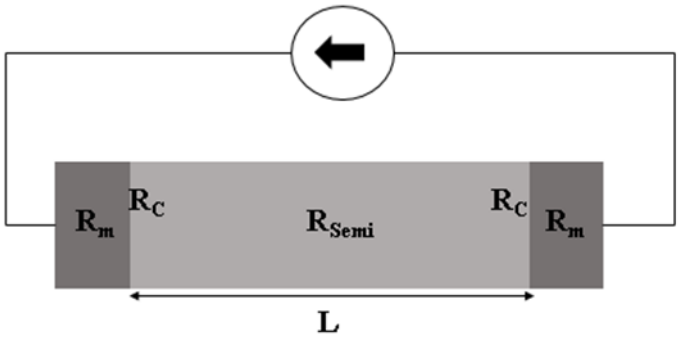


Figure 3-16 Schematics of the simple resistor including all resistances.

However, in most cases, the resistance of metal contact is lower than the resistance between metal and semiconductor interface ($R_m << R_C$), so the Equation 3.8 can be written as;

$$R_T = 2R_C + R_{Semi} \quad \text{(Eq. 3.9)}$$

The resistance of the semiconductor can be defined with Equation 3.10;

$$R_{Semi} = R_S \frac{L}{W} \quad \text{(Eq. 3.10)}$$

, where R_S is the sheet resistance of the semiconductor, L is related to the distance between two metals and W is the length of the metal bars.
Then, the equation of the total resistance becomes;

$$R_T = R_S \frac{L}{W} + 2R_C \quad \text{(Eq. 3.11)}$$

By using equation 3.11, the total resistance of each resistor built with different lengths on the sample surface can be measured and plotted as R_T versus L graph, as shown in the Figure 3-17.

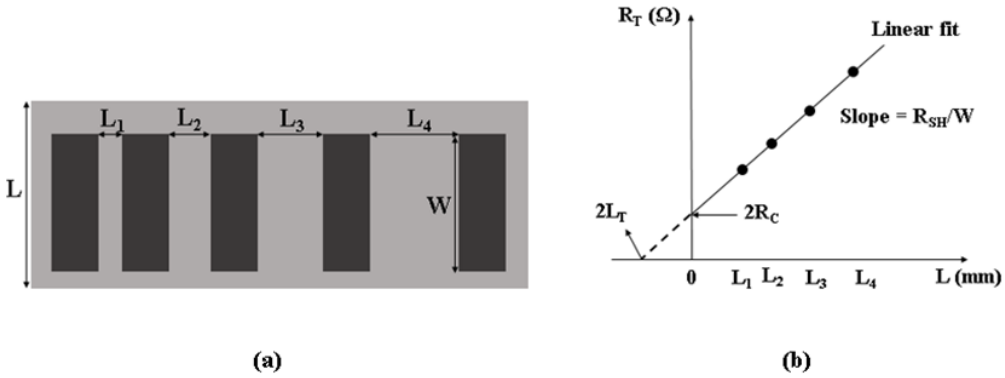


Figure 3-17 a) Top view of the TLM mask, b) the linear curve of the total resistance versus gap distance data.

Also, as the gap distance (L) goes to zero, the total resistance equals to twice of the contact resistance, as defined in Equation 3.12.

$$R_T = 2R_C \qquad \text{(Eq. 3.12)}$$

The half of the interception point of the linear fitted line with the y-axis gives contact resistivity, as seen in the Figure 3-17b.
In addition, the slope of the curve gives sheet resistance of the semiconductor that can be calculated by,

$$Slope\ (m) = \frac{R_{SH}}{W} \qquad \text{(Eq. 3.13)}$$

For the evaluation and comparison, contact resistivity is preferred because the size of the contacts effects contact resistance. The current flow is uniform through the semiconductor but the uniformity breaks down into the metal grids, as illustrated in Figure 3-18. Hence, the physical length and width of the contact cannot be utilized to determine the contact area.

The significant amount of the current pass through the edge of the metal grids and the current goes down exponentially as it goes far away from the edge. This phenomenon is called as *current crowding* [77]. Current crowding effect determines the transfer length (L_T) of the contact.

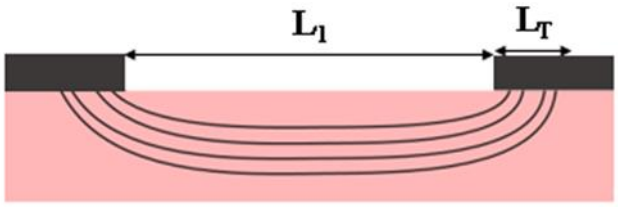


Figure 3-18 The sketch of the current flow inside the semiconductor and towards the metal.

The transfer length (L_T) can be found from the intersection point when the total resistance (R_T) is zero by extrapolating to the horizontal axis, as depicted in Figure 3-17b.

CHAPTER 4

RESULTS AND DISCUSSION

In Chapter 3, the experimental methods used for this thesis are discussed in detail. This thesis has mainly focused on the optimization of B doping process to get homogeneous sheet resistance to be used for the fabrication of n-type c-Si solar cells. Furthermore, other fabrication steps such as removal of BRL, diffusion mask for B doping, passivation of B emitter and contact formation to the surface of the p^+ layer was investigated to optimize n-type c-Si solar cell production in GÜNAM. Various measurement techniques like 4PP, SIMS, QSSPC and TLM were utilized for each fabrication step. In this chapter, the results obtained from optimization efforts are comprehensively discussed

4.1. Texturing

200 μm thick 156 mm square n-type mono crystalline silicon (c-Si) wafers with (1-3 ohm.cm) resistivity were textured to be used for the experiments. For the optimization of fabrication steps of n-type solar cell, too many textured samples were needed. The organic texturing technique was preferred for the process, as explained in the previous chapter since it enables texturing of more than one cassette (25 samples). By this way, it has been aimed to reduce the chemical use. The mixture of the KOH and alka-tex solution was utilized for each cassette at 80 °C for 20 minutes for the texturing process. Five cassettes including of twenty-five samples were textured, consecutively using organic texturing method.

One textured sample was taken from each cassette for the reflection measurement after performing standard cleaning process for all cassettes. Figure 4-1 shows the reflectance characteristics of the textured samples that belong to different cassettes.

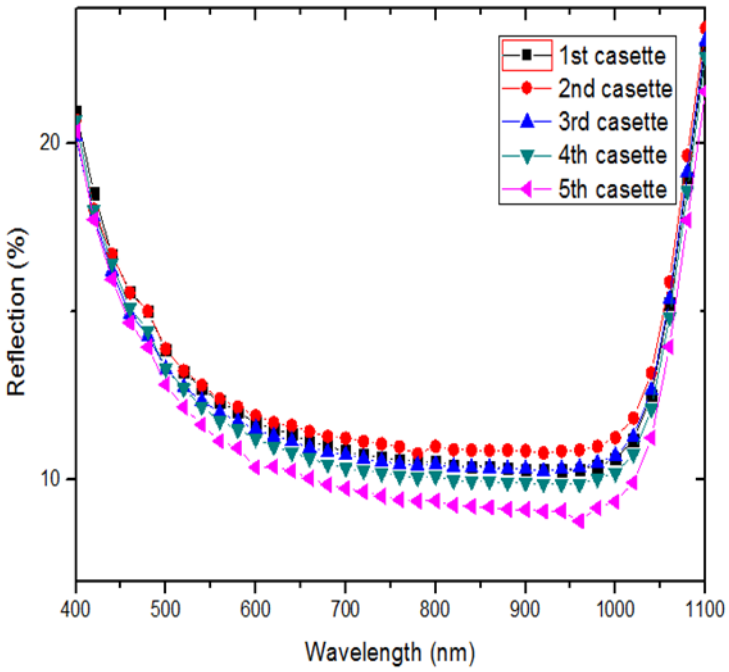


Figure 4-1 Reflection (%) versus wavelength graph for the textured n-type samples.

The results were close to each other, as seen in Figure 36 and they are in the acceptable range without an anti-reflective coating. In other words, the textured samples were usable for the optimization of experiments.

The number of the cassettes refers to immersion sequence into the solution. The lower reflection rate was obtained, as the immersion sequence increases. This trend can be explained via that as the mixture is used, the concentration of it changes. Therefore, the samples from the last cassette immersed into the solution had the lowest reflection rate.

4.2. Boron Diffusion

B diffusion studies were carried out under vacuum using SEMCO LYDOP^{TM} furnace system. BCl_3 gas was preferred as a precursor. Also, N_2 and O_2 gases are used as auxiliary gases, as discussed in previous chapter. Formation of a homogeneous B doped surface is the most significant challenge and difficult step during the fabrication of n-type solar cells.

Sheet resistance measurements via 4PP method were made to investigate the homogeneity of the B doped surface. During sheet resistance measurements, the non-uniformity of the sheet resistance between door side sample and gas side sample surfaces was observed.

Measured sheet resistance values were in the range of 45-50 ohm/sq for gas side of the last sample located on the gas injection side and for door side of the last sample positioned on the door side. However, sheet resistance results were around 150-200 ohm/sq for the other sides of the all samples. Figure 4-2 shows the photograph of n-type samples before starting the diffusion process. These results showed that the outer surfaces of the samples have uniform doping while the precursor gases were unable to reach between the sorted samples on the holder. This behavior can be attributed to the use of expired BCl_3 gas. Even still, the replacement of the tube containing BCl_3 gas was avoided due to safety reasons.

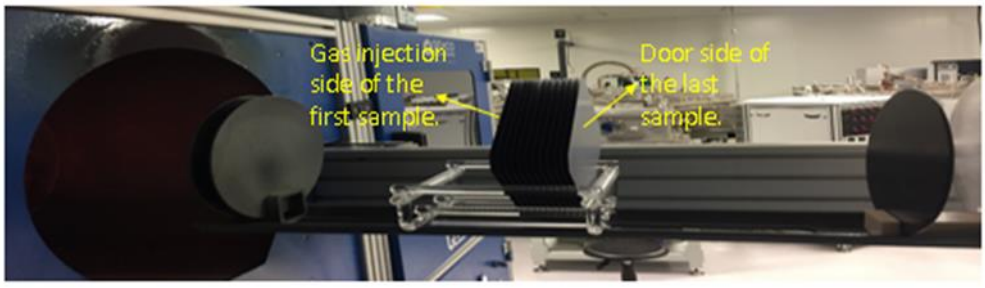


Figure 4-2 Photograph of n-type samples sorted on the quartz holder.

The sorting style of the n-type wafers on the quartz holder was changed because this was a safer solution to obtain homogeneously boron doped layers on all the surfaces of n-type samples. The quartz holder has slits to put the wafers for doping process. In standard placement of the wafers, a slit is left between each sample. To enhance the doping process, four slits were left between each wafer in order to allow BCl_3 gas to reach all surfaces of the samples.

After practicing doping with this new sorting style, the surfaces of samples were found to contain uniform BSG layer in black color, as shown in the photo provided in Figure 4-3.

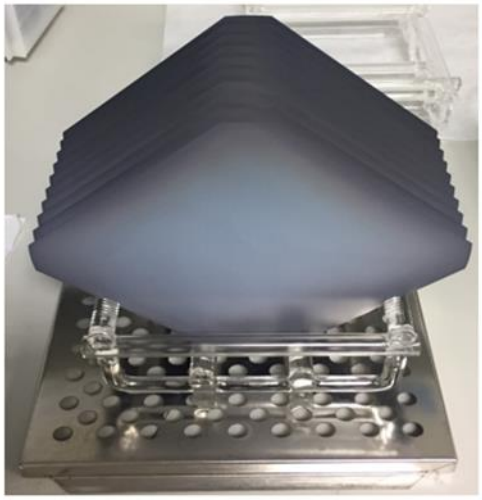


Figure 4-3 A photo of the Ferrotech CZ n-type wafers after doping process.

LTO process was carried out for 25 minutes to ten B-doped samples before measuring their lifetime by 4PP. After doping, LTO process was preferred to remove BSG layer and BRL easily using HF. The sheet resistance results of ten samples were around 45-55 ohm/sq as depicted in Figure 4-4. These results showed that leaving four slits between each sample enhanced doping process and resulted in the obtainment of uniformly doped layers on the surfaces of all n-type samples.

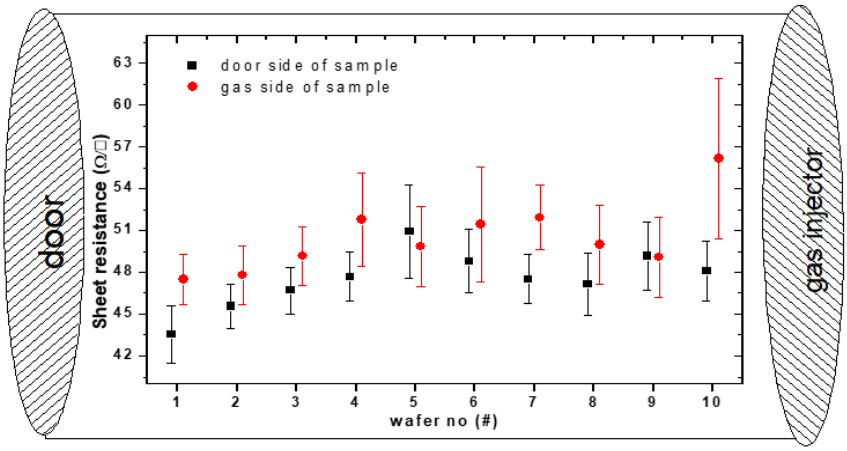


Figure 4-4 Sheet resistances for the door side and gas injector side of the B-doped samples.

In Figure 4-4, black squares and red dots illustrate the sheet resistance values of door and gas injector sides of samples, respectively. Generally, the first and last samples are not taken into account as a rule of thumb in industry and disregarded as dummy samples. Hence, there was no big difference between the obtained results when the sheet resistance of door and gas injector sides of the other samples (2-9) were considered. By using new sorting style, uniform B-doped surfaces were obtained that can be used for other optimization processes.

4.3. Removal of Boron-Rich Layer (BRL)

Every B doping technique result in undesirable BRL formation between BSG and p^+ layer, as it was mentioned in Chapter 3. LTO and chemical etching treatment (CET) methods were carried out to remove BRL. 156 mm square textured n-type mono crystalline Si wafers were utilized for this study.

4.3.1. Low-Temperature Oxidation (LTO)

Firstly, LTO technique was tried to remove BRL. Scanning electron microscopy (SEM) analysis was used to determine the thickness of the BRL following B doping. However, the contrast of the image was not enough to investigate the BRL as shown in Figure 4-5.

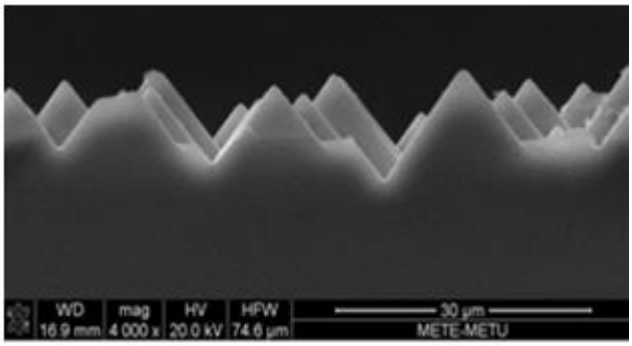


Figure 4-5 The SEM image of B-doped n-type c-Si sample.

To etch BRL, different oxide thicknesses were grown as in the Table 3-4. SiO_2 was deposited pyrogenically. Pyrogenic oxidation is a wet oxidation method. It has higher extension rate than dry oxidation. In this oxidation method, H_2 and O_2 gases are injected into the quartz tube to create H_2O inside.

The deposited oxide thickness was found by using oxide thickness (nm) versus time (minute) graph from SEMCO Company. After LTO process, sheet resistance measurements were carried out by 4PP technique. The sheet resistance values were utilized to understand that the BRL was removed because the presence of BRL leads to very high sheet resistance results.

The Figure 4-6 shows sheet resistance results belonging to B-doped samples etched with different oxide thicknesses on their surface. Prior to sheet resistance measurements all samples were immersed into HF solution.

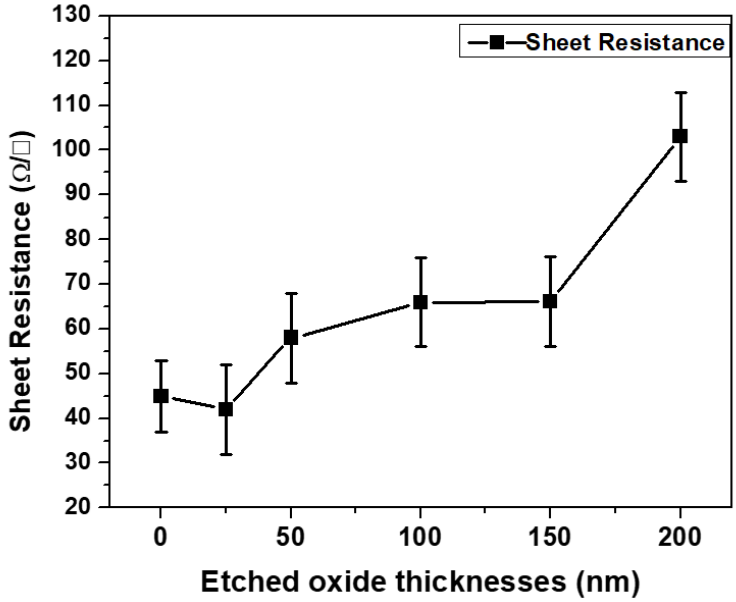


Figure 4-6 Sheet resistance (Ω/sq) versus etched oxide thickness (nm) graph.

The Figure 4-6 shows that the etched oxide thickness increases with the sheet resistances of the B-doped n-type samples. The dopant concentration of the samples decreases with increasing etched oxide thickness.

For this reason, increased etched oxide thickness causes increased sheet resistance results. The reduction in sheet resistance for an oxide thickness of 25 nm may be an experimental or measurement-induced error. The sheet resistance mapping for B-doped n-type samples with different etched oxide thicknesses can be seen in Figure 4-7.

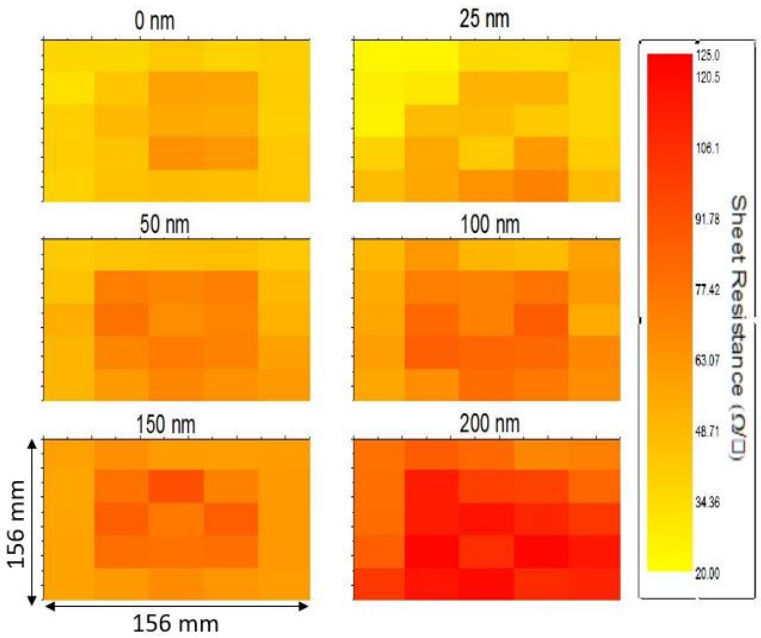


Figure 4-7 The sheet resistance mapping for different etched oxide thicknesses.

The results proved that LTO technique can be used for the removal of BRL and obtain desirable sheet resistance distributions for the solar cells.

To investigate the SIMS results, B doping was carried out again for pseudo square n-type c-Si wafers. Before sending B-doped samples to SIMS measurements, oxide layer was deposited with thicknesses of 25, 50, 100, 150 and 200 nm at 800 °C using a low-temperature oxidation technique.

To optimize removal of BRL, LTO technique after B doping followed by an etching step with HF based solution was applied. Then, SIMS measurement was carried out for all samples. In Figure 4-8, sheet resistances measured by 4PP are shown for different etched oxide thicknesses. Results have shown that reasonably well sheet resistance values can be obtained for different etched oxide thicknesses.

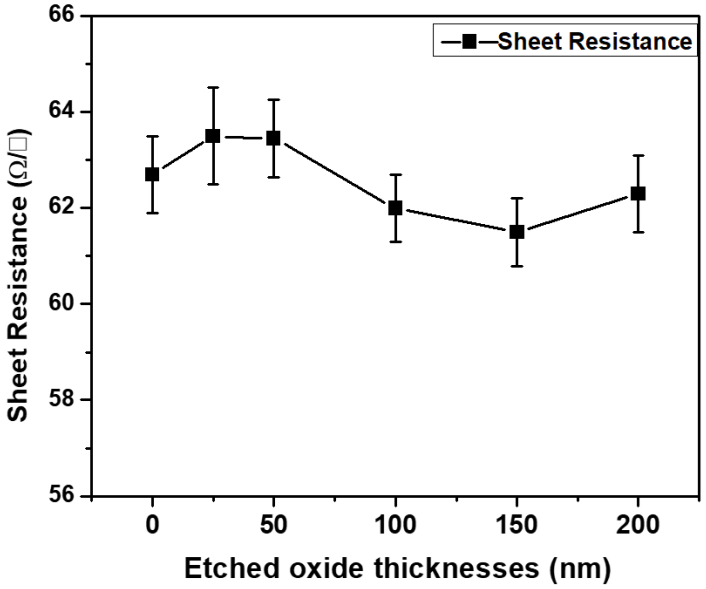


Figure 4-8 Sheet resistance (ohm/sq) versus etched oxide thicknesses (nm).

In addition, SIMS boron profiles at different LTO thicknesses are illustrated in the Figure 4-9. The maximum B concentration was around 10^{20} cm^{-3}, which is close to the solubility limit of boron at 940 °C. As the oxide thickness increases, surface concentration of B decreases due to the removal of dense BRL layer from the surface.

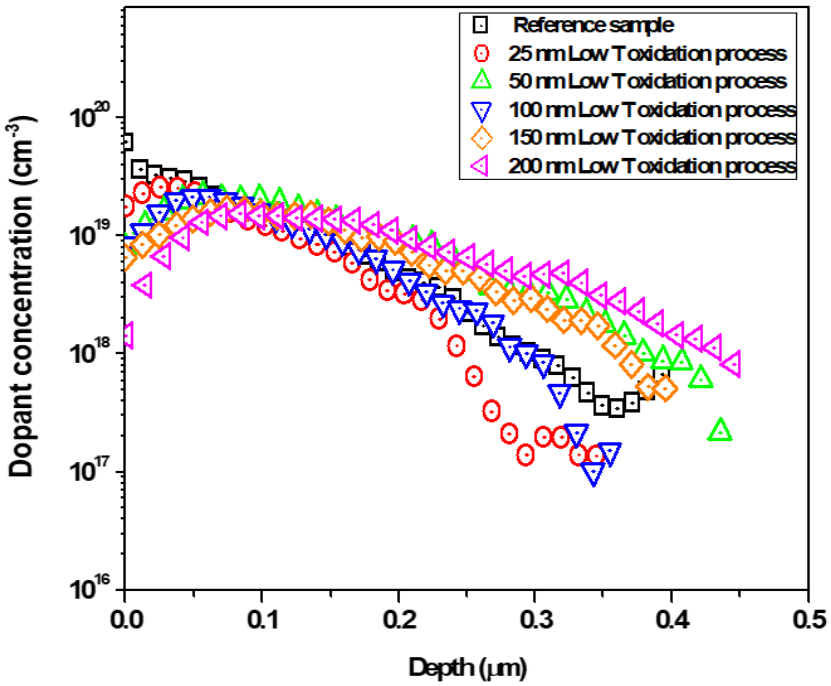


Figure 4-9 SIMS Boron profiles as a function of etched oxide thicknesses.

To verify the SIMS boron profile results, B-doped samples was sent to Fraunhofer for ECV measurements. For this study, two low quality single side polished round n-type wafers were utilized. After doping process, two round wafers were cut into 6 quarter pieces by laser for LTO process. The deposited oxide thicknesses were the same as the previous study. Then, the ECV boron profile was obtained from B doped and etched samples, results of which are provided in Figure 4-10.

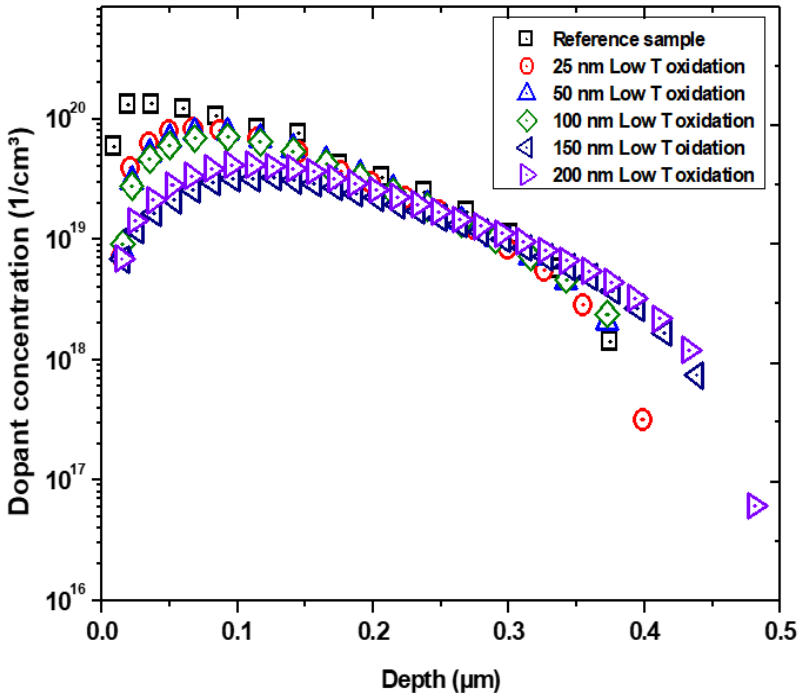


Figure 4-10 ECV Boron profiles for different etched oxide thicknesses.

B profiles showed similar trend towards the depth of the wafer for SIMS and ECV measurements. Both results show that surface dopant concentration of B decreases with an increase in etched oxide thickness due to removal of BRL from surface. The longer LTO process time is needed to obtain thicker oxide layer. Hence, B profile depth increases with extending oxide thickness since LTO process act as a drive-in step for doping process. In drive-in step of B doping process, B element diffuses towards the substrate from BSG layer. In addition, SIMS and ECV boron profile results proved that B doping process is reproducible. However, active dopant concentration was found to be higher than total dopant concentration, as can be seen in ECV B-profiles. This discrepancy can be due to the calibration errors of ECV and SIMS devices.

4.3.2. Chemical Etching Treatment

Chemical etching treatment was preferred as an alternative method for the removal of BRL. Two different solutions were used for wet etching process. After etching process, porous Si formation was observed on surface. To remove this undesirable layer, KOH dipping was carried out for 8 minutes to all etched samples. The 1% KOH solution was used for the removal of porous Si (7lt DI water/ 0.07lt KOH).

The first chemical solution consisted of hydrofluoric acid (HF), acetic acid (CH_3COOH) and nitric acid (HNO_3) with a ratio of 1:100:100, respectively. B-doped samples were exposed to this chemical mixture from 0 to 10 minutes. Table 4-1 clarifies the experiment set.

Table 4-1 Sheet resistance values with respect to different etching times for a chemical mixture (1:100:100).

Etching Time (min.)	**Sheet Resistance (Ω/sq)**
0	45
2	72
4	85
6	100
8	196
10	215

The results have shown that sheet resistance increases with the etching time due to the reduction of surface concentration. In addition, it can be said that 2- and 4-minutes etching resulted in a reasonable sheet resistance value.

In order to see the effect of HF on the sheet resistance change and optimize CET process, the same chemical mixture was utilized only by increasing the HF rate. Then the chemical ratio of the solution was changed to 10:100:100. Table 4-2 shows sheet resistance results obtained from different etching time.

Table 4-2 Sheet resistance values with respect to different etching time for (10:100:100) chemical mixture.

Etching Time (min.)	Sheet Resistance (Ω/sq)
0	45
2	238
4	390
6	450
8	576
10	662

It can be seen from Table 4-2 that the second chemical mixture is more powerful than the first chemical solution. HF enhanced the etching power of the solution. Higher sheet resistance values were obtained with shorter etching times. The powerful etching decreased surface concentration sharply and resulted in a very high sheet resistance. Also, the results showed that the etching rate of the chemical solution can simply be enhanced by increasing the HF ratio. However, less HF ratio should be utilized for a controllable CET process.

The CET process was carried out again for B-doped oxidized n-type samples in order to see how the sheet resistance of oxidized samples do get affected from etching process applied for different times. For this study, 25 and 50 nm oxide layers were deposited onto B-doped n-type samples. These thicknesses were chosen depending on the sheet resistance values obtained from previous experiments. The chemical mixture having (1:100:100) ratio was preferred for controllable etching. Then, CET process was performed from 0 to 14 minutes for both samples having different oxide thickness. Figure 4-11 shows sheet resistance results for different etching times.

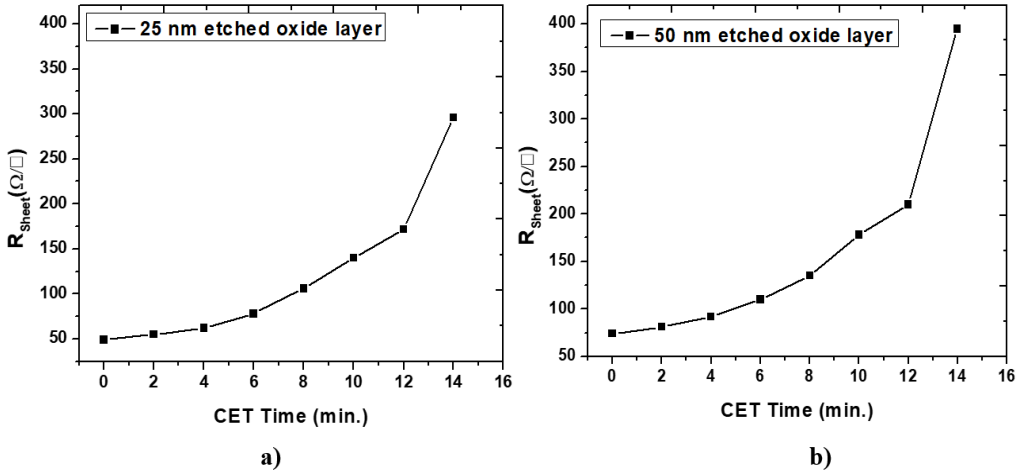


Figure 4-11 Sheet resistance results of samples having different etched thicknesses of a) 25 nm and b) 50 nm with respect to etching time.

As expected, sheet resistance results taken from a sample with 50 nm etched oxide layer were higher due to the lower boron surface concentration. However, the sheet resistance values in the range of 55-75 ohm/sq were obtained at different etching times for both samples.

4.4. Silicon Dioxide (SiO_2) Diffusion Mask

To fabricate n-type based solar cells with BCl_3 diffusion in a tube furnace diffusion masking step must be performed. Various oxide thicknesses were grown by HTO process at 900 °C to deduce the sufficient thickness for masking B diffusion. The HTO method was preferred to reach high oxide layer in a shorter time. 20, 40, 80, 160 and 320 nm oxide thicknesses have been tried for observing masking property of SiO_2. Sheet resistance measurements were used to investigate the masking property. The results were compared to that of bare undoped n-type silicon and bare doped n-type silicon.

As explained in B diffusion experiment section, the sorting style of the n-type samples has been changed to enhance doping process. Hence, the different masking results have been obtained from different sorting type.

The Figure 4-12 shows the sheet resistance results obtained from standard sorting style including one space between each sample.

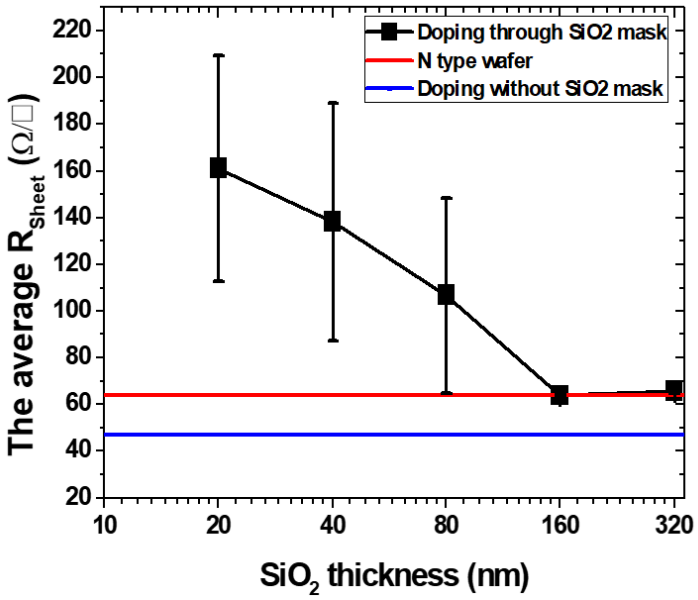


Figure 4-12 The average sheet resistance versus extend oxide thickness for masking.

As can be seen from Figure 4-12, sheet resistance value was measured as 65 Ω/sq for undoped n-type wafer, while it was 45 Ω/sq for unmasked boron doped n-type wafer. Hence, an effective masking function was observed for SiO_2 with a thickness of 160 and 320 nm. For thickness below 160 nm, the average sheet resistance values were very high due to low doping level. This means that there was B element leakage towards substrate under 160 nm. The average sheet resistance measurement was taken from 25 different points on both surfaces of the fabricated samples.

After changing sample sorting style on the quartz holder, diffusion mask study was repeated again. At this time, there were four spaces were left between each sample to enhance doping for both sides of samples.

The same oxide thicknesses were tried again to obtain comparable results. The door side and gas injector side of the samples was investigated, separately.

Figure 4-13(a) and Figure 4-13(b) show sheet resistance results that belong to door side and gas injector side of the n-type wafers, respectively.

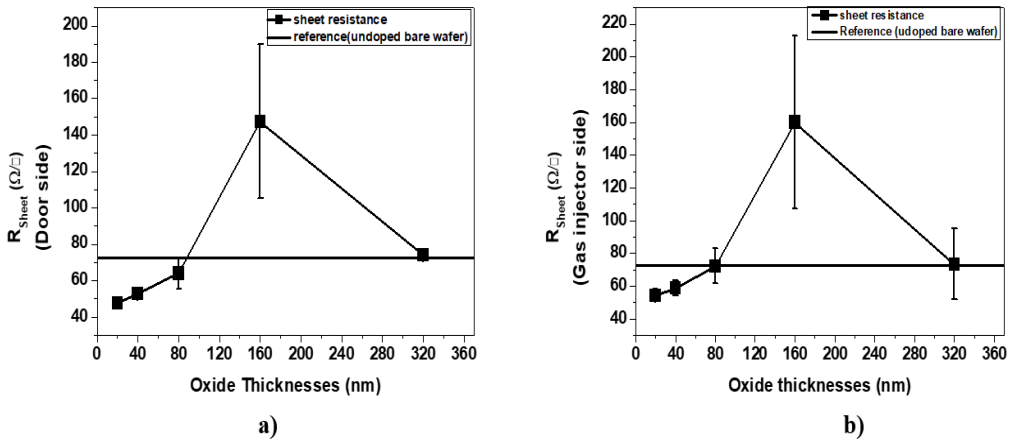


Figure 4-13 a) Sheet resistance of door side and b) gas injector side of the samples versus extend oxide for masking.

It can be seen in Figure 4-13 that changing sorting style of n-type wafers on quartz holder affect the masking property of SiO_2. The oxide thickness presenting diffusion mask function grew up from 160 nm to 320 nm. The thicker oxide layer prevented B diffusion because B element can reach to both sides of the sample, easily in this sorting style. The results obtained from new sorting style is more realistic because the B diffusion gave more accurate results for both sides of sample in this case.

4.5. Surface Passivation

Surface passivation is a critical step to reach high photovoltaic conversion efficiency with n-type based solar cells. Two passivation methods that are Al_2O_3 and Al_2O_3/SiN_x stack layer was used to increase the minority carrier lifetime. The cleaned and double side polished Fraunhofer FZ p-type round wafers (bulk lifetime ~ 1000 µs) were preferred for the passivation experiments.

4.5.1. Al_2O_3 Passivation Layer

Emitter passivation studies were carried out using Okyay tech. ALD. Various temperature and cycle combinations were applied to reach the best passivation condition.

In first trial of Al_2O_3 deposition, 15 and 30 millisecond pulse duration were applied for four different temperatures (150, 180, 200 and 230 °C) and the cycle of ALD process kept constant at 80 cycles. An annealing process was performed at 425 °C to activate the passivation function of deposited Al_2O_3. The details of the processes are given in Chapter 3. After annealing process, lifetime measurement was carried out for all Al_2O_3 deposited and activated samples, results of which are provided in Figure 4-14.

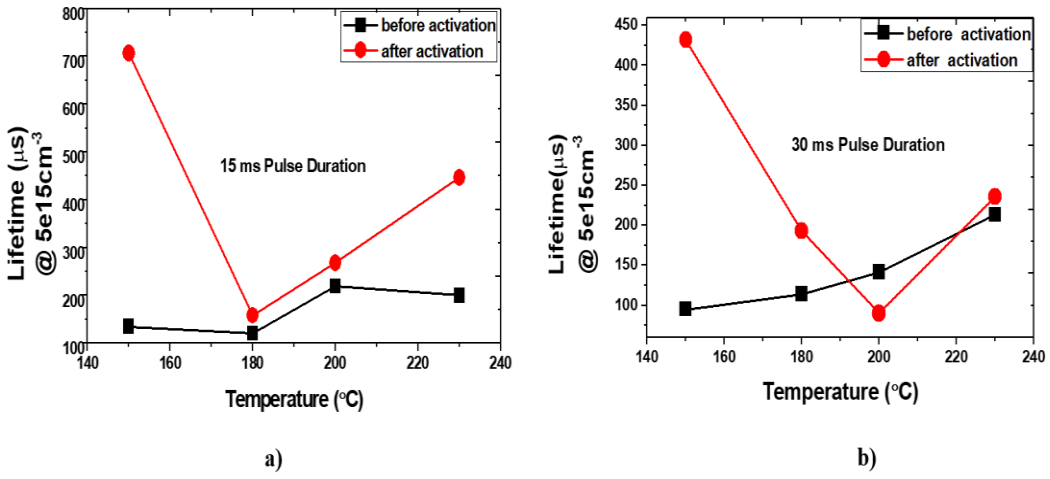


Figure 4-14 Lifetime versus ALD temperature graph for pulse durations of a) 15 ms and b) 30 ms.

The better passivation was obtained from recipe that include 15 millisecond pulse duration and 150 °C temperature as shown in Figure 4-14a. After activation, around 700 µs lifetime was achieved for this recipe.

In the second trial, 10 ms and 15 ms pulse durations were applied depending on previous experiment to see the lower pulse duration effect on lifetime. Also, the minimum and maximum temperatures limit of Okyay tech. ALD system that are 150 and 260 °C were used for process. The temperature of 150 °C was retried since the best lifetime result was obtained at this temperature in the previous trial. In addition, to see the limit of ALD system, a maximum temperature of 260 °C was also applied in this trial. After activation process, lifetime of samples was measured using QSSPC device. The Table 4-3 illustrates the lifetime results that belong to different ALD recipes.

Table 4-3 Lifetime results for the second trial for optimization of Okyay tech. ALD system.

	Pulse Duration (ms)			
	10		**15**	
Temperature (°C)	**Before activation**	**After activation**	**Before activation**	**After activation**
150	71 µs	153 µs	78 µs	651 µs
260	213 µs	236 µs	162 µs	165 µs

The better minority carrier lifetime results were obtained for 15 millisecond pulse duration at 150 °C again. Hence, this recipe proved that it can be used for passivation of B doped n-type surface. However, lifetime results can still be enhanced to obtain very high efficiency from n-type substrate.

After determination of pulse duration and temperature of the recipe, the number of the cycles was also investigated.

In this study, 15 ms pulse duration and the temperature of 150 °C was kept constant and various number of cycles (20, 40, 80 and 160) for ALD process was applied to determine the growth per cycle (GPC) and observe the effect of thickness on the minority carrier lifetime. The thickness of Al_2O_3 layer was measured by ellipsometry technique.

It is shown in Figure 4-15 that Al_2O_3 film thickness scales linearly with the number of ALD cycles.

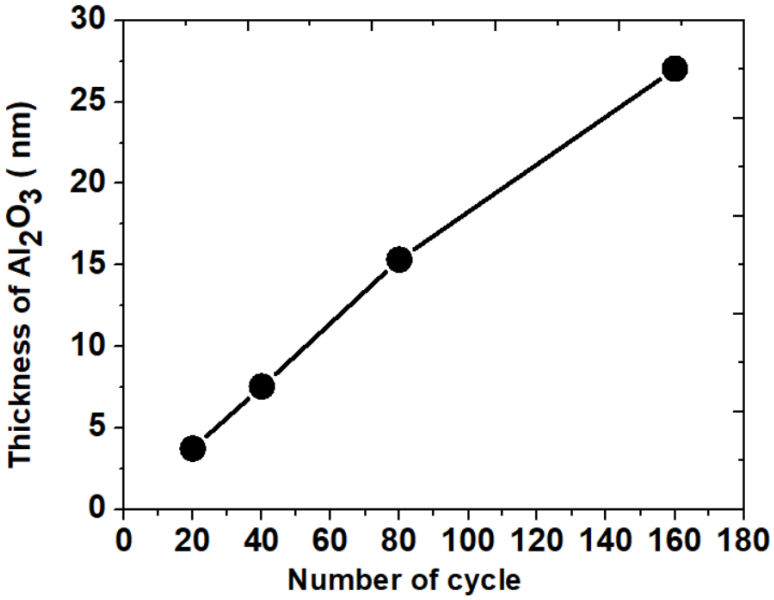


Figure 4-15 Thickness as a function of the number of ALD cycles for Okyay tech. ALD method at 150 °C.

The slope of the film thickness as a function of the number of ALD cycles is called as growth per cycle (GPC) of the ALD process. The GPC of 0.19 nm/cycle was observed for Al_2O_3 deposited by Okyay tech. ALD used in this study.

To determine growth per cycle ratio, thickness of Al_2O_3 film was just measured from the center of sample surface.

However, it was realized during the ellipsometer measurement that the thickness of Al_2O_3 film was not uniform on the surface. For 80 ALD process cycle, the thickness of Al_2O_3 film at the center of sample was 14 nm while it was 25 nm at the edge of sample, as schematically shown in Figure 4-16.

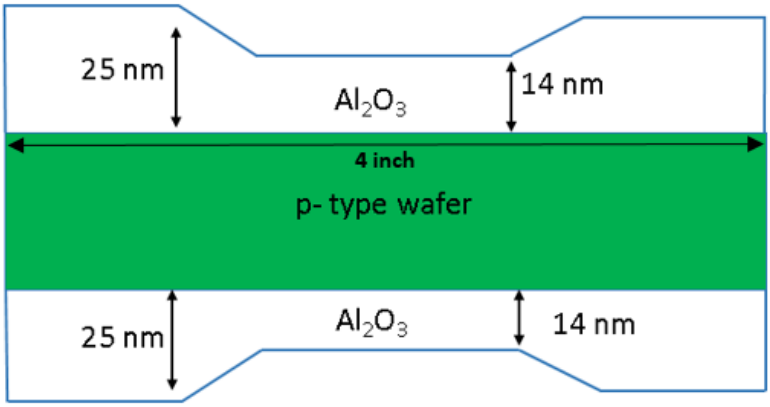


Figure 4-16 Schematic representation of the thickness distribution of Al_2O_3 layer on the surface.

A possible reason to explain the current situation is the leakage from the edges towards back side of the sample during the deposition process. Hence, the edges of sample had thicker Al_2O_3 film.

All optimization processes of Okyay tech. ALD was performed using p-type substrates to deduce suitable process for B doped n-type samples. In this part of passivation studies, B doped n-type wafers were tried to be passivated using the ALD recipe that resulted in the best lifetime (15 ms pulse duration: 150 °C: 80 cycle).

After B doping process, different thicknesses (25, 50, 100 nm) of oxide layers were grown on the surface. The lifetime of samples was measured after ALD processes followed by an activation step, results of which are provided in Figure 4-17.

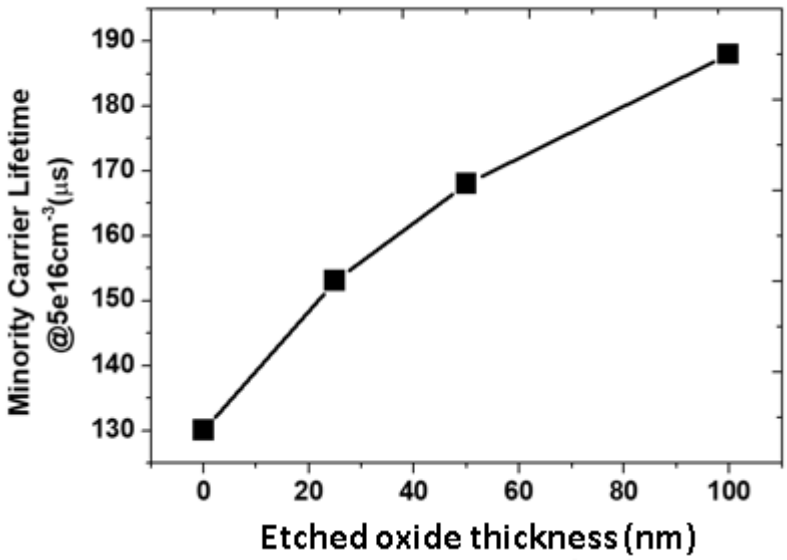


Figure 4-17 Lifetime values with respect to different etched oxide thicknesses.

As expected, lifetime increases with the increase of etched oxide layer thickness. Because the surface concentration of B decrease with increasing etched oxide thickness, the probability of surface recombination also decreases and this situation results in higher lifetimes. However, the obtained results were very poor when compared to the lifetime values obtained from p-type substrates.

To find out exact cause of the poor lifetime results, a different ALD system bought from Solaytec was used for the forthcoming passivation experiments. Solaytec ALD is an industrial system and it can be used to deposit 10 nm Al_2O_3 film onto 100 wafers in an hour. 156 mm pseudo square textured different brands of FZ p-type mono crystalline silicon wafers from Ferrotech, Green energy, Norway, Solar Energy, and Edison were utilized during the passivation process. After coating 10 nm Al_2O_3 film, three different activation recipes were utilized.

These activation recipes include GÜNAM recipe (425 °C: 10000 sccm N_2:500 sccm H_2: 30 min.), Solaytec recipe (450 °C: 10000 sccm N_2: 30 min.) and an industrial recipe (550 °C. 10000 sccm N_2: 10 min.).

Two samples from each brand were utilized for the measurements and the average of the lifetime values were taken for plotting lifetime graph. The average lifetime results of different annealing processes are shown in the Figure 4-18.

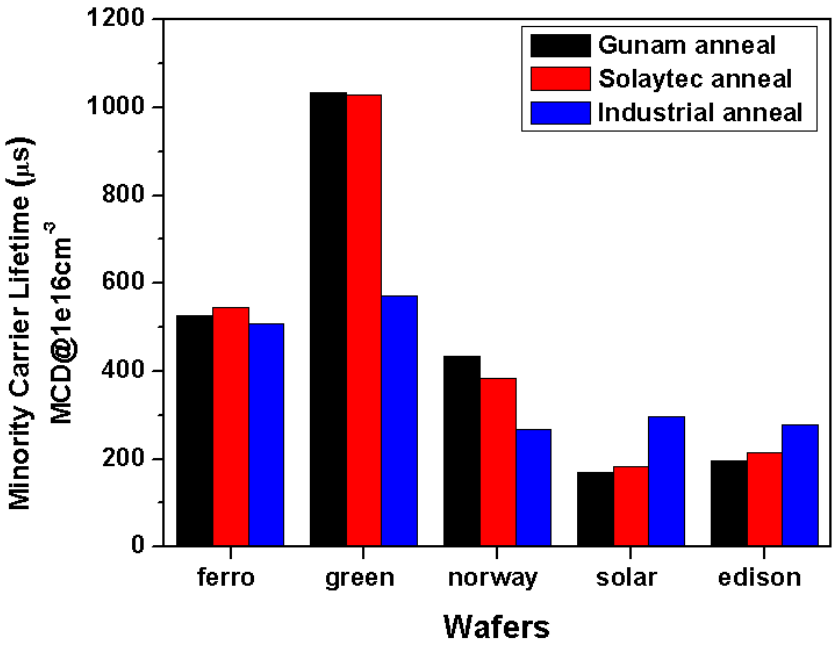
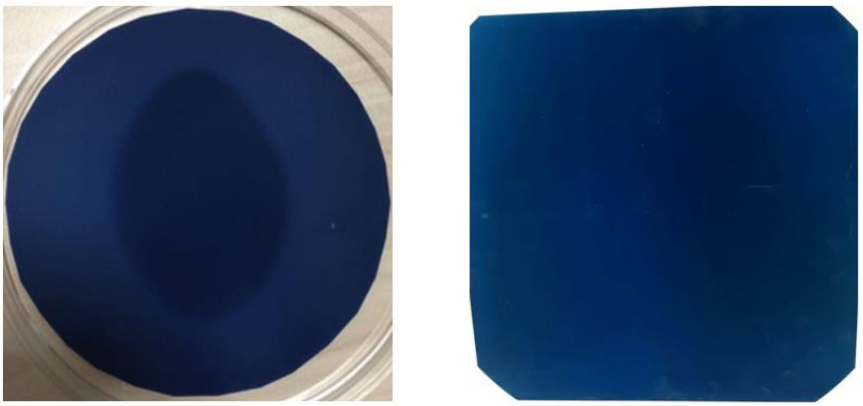


Figure 4-18 Average lifetime results according to the different annealing process.

The maximum lifetime value of 1.4 millisecond was obtained using green energy wafer and GÜNAM annealing recipe. These promising results showed that texturing and cleaning processes were not problematic for previous ALD passivation trials (with Okyay tech. ALD) because the same processes were applied for prior to Solaytec ALD. The uniform Al_2O_3 film formation on the surface could not be achieved using the Okyay tech. ALD being different from Solaytec ALD.

As discussed before, the non-uniformity of Al_2O_3 film (Okyay tech. ALD) on the surface was evident by naked eye after SiNx coating, refer to Figure 4-19a. In contrast, a uniform Al_2O_3 coating was obtained by Solaytec ALD system as shown in Figure 4-19b.



a) b)

Figure 4-19 Photos of samples after a) Okyay tech. ALD and b) Solaytec ALD.

4.5.2. Al_2O_3/SiN_x Stack Layer Passivation

For the passivation of B emitter, the effect of Al_2O_3/SiN_x (15nm / 75 nm) stack layers were investigated to see the effect of Si_3N_4 layer on the minority carrier lifetime.

In this experiment, B doped CZ n-type wafers were utilized with Okyay tech. ALD system after growing oxide layer with different thicknesses (25, 50, 100 nm) by LTO method. ALD process was carried out for doped and etched samples followed by the activation step (425 °C: 10000 sccm N_2:500 sccm H_2:30 min.). Then, SiN_x layer was deposited onto Al_2O_3 film to investigate its effect on the lifetime. Lastly, the second activation process was performed for the samples having Al_2O_3/SiN_x stack layer on their surface.

Minority carrier lifetime of the samples were measured after activation, SiN_x coating and the second activation processes, results of which are provided in Figure 4-20.

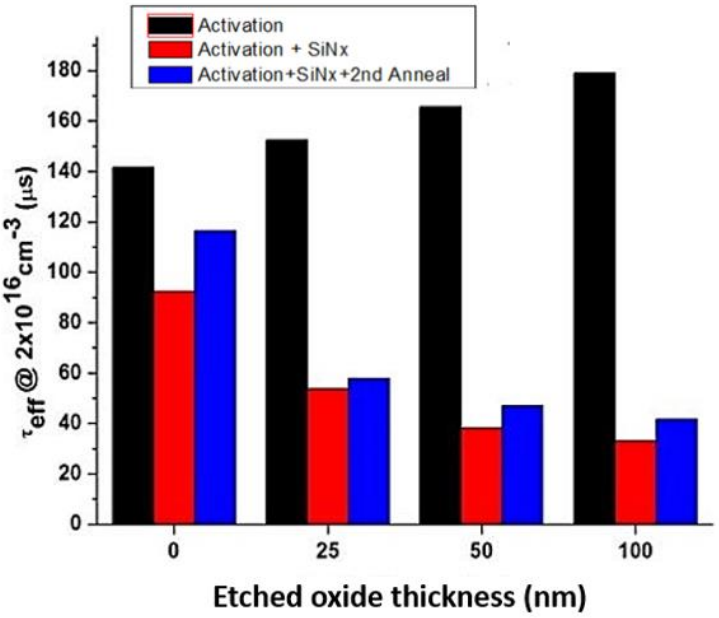


Figure 4-20 Lifetime results for different etched oxide thicknesses at different process steps.

In Figure 4-20, depending on decreasing BRL, as the etched oxide thickness increases, the lifetime value was found to increase, as expected (black bars). However, minority carrier lifetime value of the samples sharply decreased after SiN_x coating (red bars). The second activation process applied for enhancing lifetime values but it also did not work (blue bars). Moreover, the lifetime values obtained from Okyay tech. ALD process followed by the activation step was not enough for the fabrication of n-type based solar cell. In addition, blistering formation was observed after SiN_x coating on the sample surfaces due to H_2 release. Therefore, this undesirable blistering formation on the surface could be the reason for poor lifetime results.

To investigate the effect of Al_2O_3 layer thickness in stack (Al_2O_3/SiN_x) layer passivation, Al_2O_3 films with different thicknesses (4, 8, 16 nm) were deposited using Okyay tech. ALD, which was followed by SiN_x (75 nm) layer deposition on those films.

Firing process was applied at 900 °C for the samples having Al_2O_3/SiN_x stack passivation layers on their surfaces to observe the corresponding changes in the lifetime values. In activation step two different temperatures (425 and 550 °C) were used with N_2 and H_2 gases (10000 sccm: 500 sccm) for the optimization of annealing. For this study, undoped Ferrotech FZ p-type wafers were utilized and lifetime values were monitored after activation, SiN_x coating and firing process.

Figure 4-21 shows lifetime results for different ALD film thicknesses at different process steps. These values do belong to an experiment with an activation temperature of 425 °C.

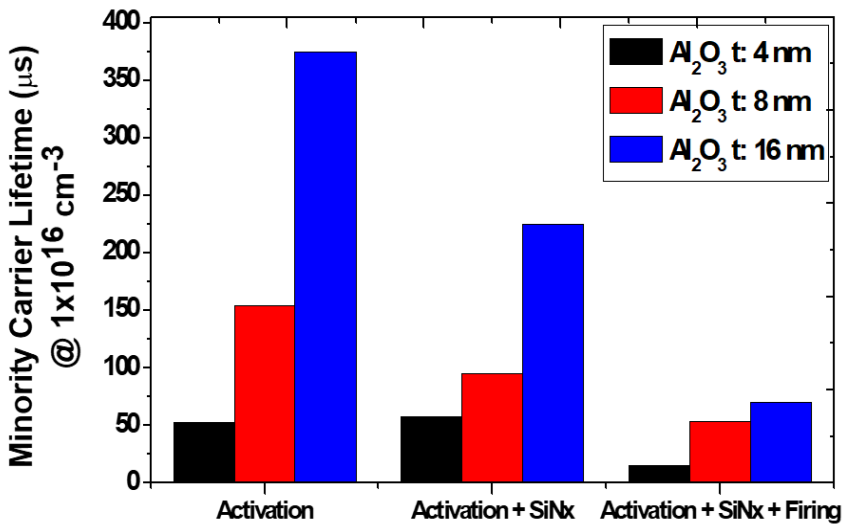


Figure 4-21 Results of the lifetime for different ALD film thicknesses at different process steps (for 425 °C activation temperature).

The lifetime results belonging to experiment that includes an activation temperature of 550 °C are shown in Figure 4-22.

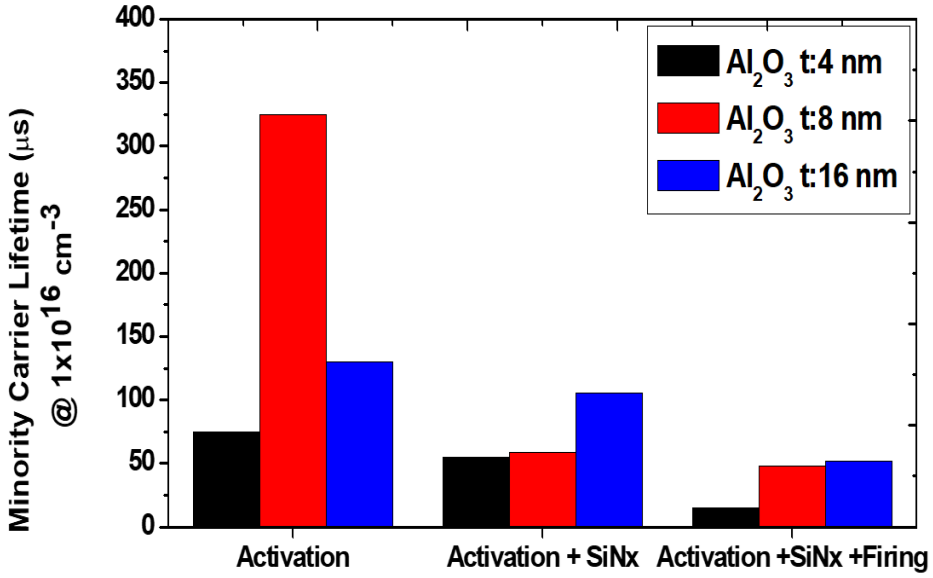


Figure 4-22 Results of the lifetime for different ALD film thicknesses at different process steps (for 550 °C activation temperature).

Upon comparison of the results, it is clear that higher lifetime values were obtained from 16 nm ALD film thickness for an activation temperature of 425 °C. In addition, activation temperature of 425 °C seemed more suitable for the activation process. However, the results were still very poor for the fabrication of high efficiency n-type based solar cells. The uniform ALD film layer couldn't be deposited. Also, blistering formation on the surface after SiN_x capping couldn't be solved.

4.6. Contact Formation

The contact resistivity was optimized using evaporated aluminum films. During the optimization processes, different firing temperatures (800, 850 and 900 °C) were used with different firing belt speeds (100, 200, 300, 400 and 500 cm/min). Before thermal evaporation, LTO processes with 30, 60, 120, 180 and 240 minutes were performed to remove BRL.

The electrical quality of the contact formation on the B-doped Ferrotech CZ n-type wafers was then studied by TLM method. The contact resistivity values lower than 10 mΩcm was achieved, as shown Figure 4-23. It was observed that contact resistivity increases with the firing temperature.

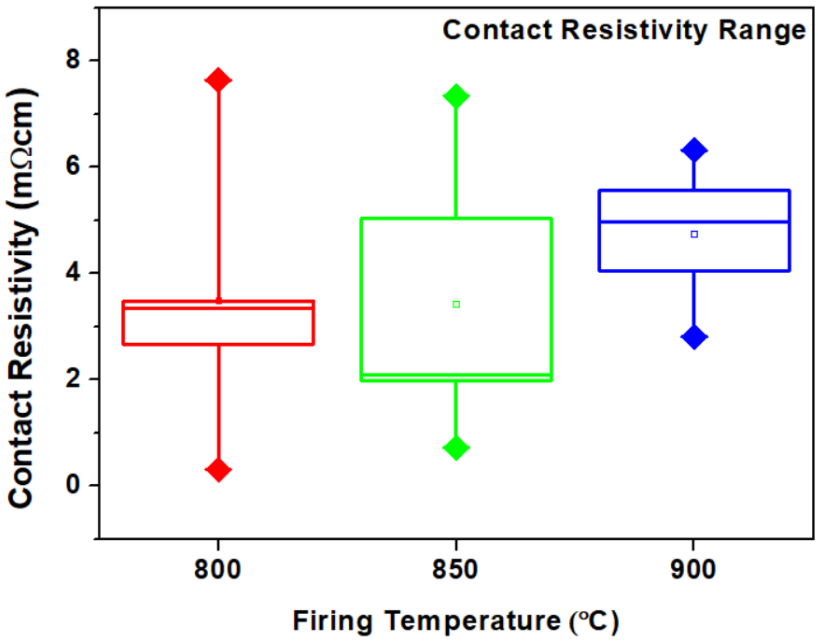


Figure 4-23 Changes in contact resistivity with firing temperatures.

CHAPTER 5

CONCLUSION

Solar energy is the best option among the other renewable energy sources for the modern world's energy demand because it has more advantages like cost-effective, non-toxic and availability compared to the other energy sources. In addition, solar cells are utilized for directly converting solar energy to the electricity in photovoltaics (PV) technology. Silicon is the industrially standard material for the fabrication of solar cells and p-type Si is commonly utilized as substrate for the fabrication of solar cells due to the advantages in device processing. However, studies on the use of n-type substrates have shown that it is a very suitable material for terrestrial PV applications with the advantages of lower sensitivity to metallic impurities and absence of light induced degradation (LID) when compared to conventional p-type substrates. By virtue of all these advantages, n-type based solar cells are highly promising and have huge potential in terms of efficiency.

However, fabrication process for n-type based solar cells has technical difficulties in terms of boron doped emitter formation, removal of boron-rich layer (BRL), boron diffusion mask, passivation of boron emitter and contact formation. In this work, all these fabrication steps of n-type solar cell have been tried to be optimized.

Before starting the optimization of fabrication steps, organic texturing method has been tried for the texturing of multi cassettes in one solution in order to reduce the usage of chemicals. Then, uniform boron doped emitter has been tried to be obtained, removal of BRL layer formed by BCl_3 and masking of dopant species with the use of thermally grown oxide have been studied in detail.

In addition, chemical etching treatment (CET) method was also utilized for removal of BRL. Effect of low temperature oxide thickness and chemical etching duration on dopant profile and oxide thickness on dopant masking was investigated through sheet resistance and profiling measurement.

Atomic layer deposition (ALD) of Al_2O_3 for passivation of the emitter and contact formation optimization through TLM measurements were conducted for fabrication of n-type c-Si solar cells. 156 mm pseudo square CZ n-type and FZ p-type wafers were utilized during optimization processes and they have been cut in chamber shape sometimes by laser according to the chamber of process device.

Organic texturing method including alka-tex was applied to five cassettes n-type wafers and these cassettes were immersed in the solution for 20 minutes consecutively. Around %10 reflection has been observed without antireflection coating.

Boron doping is usually carried out using BBr_3 in liquid form. The alternative material for B doping is BCl_3 used in the gas form, which can have the advantageous of the efficient impurity gettering due to the involvement of Cl atoms. SEMCO LYDOP™ furnace system was used for boron doping. Diffusion processes have been conducted under vacuum condition. Uniform sheet resistance values in the range of 50-60 ohm/sq have been achieved for both sides of n-type samples by changing sorting style of wafers on the quartz holder and boron injection duration in process.

Undesirable boron-rich layer which can inhibit surface passivation and act as a high recombination site generally forms between borosilicate glass and p^+ region after boron doping process. Therefore, removal of BRL is an inevitable step for fabrication of high efficiency n-type solar cell. Low temperature oxidation method was performed at 800 °C with different thicknesses (25, 50, 100, 150, 200 nm) to remove BRL. It was observed that desired sheet resistance values can be obtained by changing etched oxide thicknesses. In addition, SIMS and ECV results proved that LTO technique was useful to remove BRL.

Chemical etching treatment technique was also carried out for removal of BRL. Different etching times from 0 to 10 minutes were applied to see changing of sheet resistance. Sheet resistance results at the different etching time showed that CET method can also be used for reaching desired sheet resistance and remove BRL.

Masking property of high temperature oxidation at 900 °C was studied as a function of layer thickness. Different oxide thicknesses (20, 40, 80, 160, 320 nm) have been tried to investigate the masking property of SiO_2 for boron and successful mask was obtained for thickness above 320 nm.

For emitter passivation, Al_2O_3 was used and growth per cycle (GPC) was determined in the Okyay tech. ALD process. Cleaned and double side polished Fraunhofer FZ p-type round wafers (bulk lifetime ~ 1000μs) were used for lifetime measurement. Symmetrical samples were preferred for measurement and the lifetime values were determined by quasi-steady-state photoconductance (QSSPC) method. For activation of passivation layer, annealing process was carried out after ALD process. Annealing processes at different temperature (425 and 550 °C) were applied with different gas combination such as N_2 and N_2/H_2 in order to optimize annealing process. The best results were observed in the annealing recipe including 425 °C temperature with N_2/H_2 gasses. To determine the GPC of Okyay tech. ALD, different ALD cycles (20, 40, 80 and 160 cycles) were utilized at 150 °C and the GPC of 0.19 nm/cycle was observed for Al_2O_3 deposited by Okyay tech. ALD. For Al_2O_3 passivation layer, lifetime measurements were poor before and after annealing process. Uniform Al_2O_3 thin film layer deposition couldn't be obtained during the optimization processes. In addition, the ALD system bought from Solaytec Company has been used for Al_2O_3 passivation and compare the results previous processes. After annealing process at 425 °C, the best lifetime value reached 1.4 millisecond.

This high lifetime result proved that the used cleaning and texturing processes before ALD methods were not problematic. Al_2O_3/SiN_x stack passivation layer was also tried to enhance lifetime results.

However, blistering formation on sample surface was observed after depositing SiNx onto Al_2O_3 layer so the measured lifetime values could not be useful for n-type based solar cell fabrication.

Contact formation with aluminum (Al) was obtained using thermal evaporation method. Transmission line method (TLM) was used for determining quality of contact formation. Boron doped n-type samples were utilized during the metallization processes. LTO process was performed with different minutes (30, 60, 120, 180 and 240 minutes) for doped samples to remove BRL before evaporation process. For optimization of contact formation, firing processes were performed at different temperature (800, 850 and 900 °C) and different firing belt speed (100, 200, 300, 400 and 500 cm/min). The contact resistivity results lower than 10 mΩcm.

The experiences gained in experiments that are carried out for optimization of n-type based solar cell production steps were crucial. The information and data obtained from this study will guide the fabrication of n-type based solar cell structures in the future. However, fabrication steps for n-type solar cell can be further improved.

In future works, n-type solar cell can be produced by using optimized fabrication steps. For passivation of B-doped emitter surface, Solaytec ALD system can be used and Al_2O_3/SiN_x stack layer passivation method can be re-optimized by using this system. In addition, single-side etching method can be optimized instead diffusion mask with SiO_2 to diversify the production method and see effect on the conversion efficiency results. Furthermore, different metallization techniques like screen-printing can be tried for contact formation to compare TLM results.

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