PERFORMANCE EVALUATION AND COMPARISON OF LOW VOLTAGE GRID-TIED THREE-PHASE AC/DC CONVERTER CONFIGURATIONS WITH SI AND SIC SEMICONDUCTOR SWITCHES

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
MIDDLE EAST TECHNICAL UNIVERSITY

BY

OĞUZHAN ÖZTOPRAK

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF MASTER OF SCIENCE
IN
ELECTRICAL AND ELECTRONICS ENGINEERING

JUNE 2019

Approval of the thesis:

PERFORMANCE EVALUATION AND COMPARISON OF LOW VOLTAGE GRID-TIED THREE-PHASE AC/DC CONVERTER CONFIGURATIONS WITH SI AND SIC SEMICONDUCTOR SWITCHES

submitted by **OĞUZHAN ÖZTOPRAK** in partial fulfillment of the requirements for the degree of **Master of Science in Electrical and Electronics Engineering Department, Middle East Technical University** by,

Prof. Dr. Halil Kalıpçılar
Dean, Graduate School of **Natural and Applied Sciences** _____

Prof. Dr. İlkay Ulusoy
Head of Department, **Electrical and Electronics Eng.** _____

Prof. Dr. Ahmet Masum Hava
Supervisor, **Electrical and Electronics Eng., METU** _____

Examining Committee Members:

Prof. Dr. Ali Nezih Güven
Electrical and Electronics Eng., METU _____

Prof. Dr. Ahmet Masum Hava
Electrical and Electronics Eng., METU _____

Prof. Dr. Kemal Leblebicioğlu
Electrical and Electronics Eng., METU _____

Assist. Prof. Dr. Emine Bostancı
Electrical and Electronics Eng., METU _____

Assist. Prof. Dr. Hasan Hüseyin Eroğlu
Electrical and Electronics Eng., Bartın Uni. _____

Date: 13.06.2019

I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

Name, Surname: Oğuzhan Öztoprak

Signature:

ABSTRACT

PERFORMANCE EVALUATION AND COMPARISON OF LOW VOLTAGE GRID-TIED THREE-PHASE AC/DC CONVERTER CONFIGURATIONS WITH SI AND SIC SEMICONDUCTOR SWITCHES

Öztoprak, Oğuzhan
Master of Science, Electrical and Electronics Engineering
Supervisor: Prof. Dr. Ahmet Masum Hava

June 2019, 175 pages

In this thesis, as compared to silicon IGBT (Si-IGBT) technology, the advantages of using higher efficiency and faster wide bandgap silicon carbide (SiC) semiconductor switches in low voltage three-phase grid-tied PWM DC/AC voltage source converters (VSCs) are investigated in terms of sizing, efficiency and economic considerations for MW-scale photovoltaic power plant applications. As the cost and energy efficiency of a VSC strongly affect the total system economics, this thesis proposes a design methodology optimizing the total cost of ownership (TCO) during the VSC design stage. Return on investment (ROI) and payback period (PP) are considered as the basic parameters for optimization. In the design, hybrid device (Si-IGBT with SiC diode, H-IGBT) and SiC-MOSFET semiconductor switches are weighed along with Si-IGBT technology based conventional design as reference. The power semiconductor module, passives (LCL filter), and heatsink are designed and compared with the reference design. A 30 kW VSC system is simulated, designed and tested in the laboratory to confirm the performance studies, then economic assessments are conveyed. Additionally, in this thesis, with wide bandgap devices switching at relatively high switching frequencies, the influences of feedback signal noise filter, PWM, and control delays on the VSC control performance are investigated. Grid

current control and converter current control methods are compared via modelling and simulation, then recommendations made.

Keywords: Efficiency, Photovoltaic, Return on Investment (ROI), Silicon Carbide (SiC), Voltage Source Converter (VSC)

ÖZ

SI VE SIC YARI İLETKEN ANAHTARLI, ALÇAK GERİLİM 3 FAZ ŞEBEKE BAĞLANTILI AC/DC GÜÇ DÖNÜŞTÜRÜCÜ TOPOLOJİLERİNİN PERFORMANS DEĞERLENDİRMESİ VE KARŞILAŞTIRILMASI

Öztoprak, Oğuzhan
Yüksek Lisans, Elektrik ve Elektronik Mühendisliği
Tez Danışmanı: Prof. Dr. Ahmet Masum Hava

Haziran 2019, 175 sayfa

Bu tezde, alçak gerilim dağıtım şebekesine bağlı üç fazlı PWM DC/AC gerilim kaynaklı dönüştürücülerde (VSC), silikon IGBT (Si-IGBT) teknolojisine kıyasla daha yüksek verime sahip ve daha hızlı olan geniş bant aralıklı silisyum karbür (SiC) yarı iletkenlerin kullanılmasının avantajları MW ölçekli fotovoltaik santral uygulamaları özelinde boyutlandırma, verimlilik ve ekonomik hususlar açısından incelenmiştir. Bir gerilim kaynaklı DC/AC dönüştürücünün maliyet ve enerji verimliliği toplam sistem ekonomisini güçlü bir şekilde etkilediğinden, bu tez, gerilim kaynaklı dönüştürücü tasarımı aşamasında toplam sahip olma maliyetini (TCO) eniyileştiren bir tasarım yöntemi önermektedir. Bu çalışmada yatırımın geri dönüşü (ROI) ve amorti süresi (PP) eniyileştirme için temel parametreler olarak kabul edilmiştir. Tasarımda, hibrit IGBT (SiC diyotlu Si-IGBT, H-IGBT) ve SiC-MOSFET yarı iletken anahtarları, referans olarak geleneksel Si-IGBT teknolojisi ile karşılaştırmalı değerlendirilmektedir. Çalışma kapsamında güç yarıiletken modülü, pasif süzgeçler (LCL) ve soğutucu tasarlanmış ve referans tasarımı ile karşılaştırılmıştır. Performans çalışmalarını doğrulamak için 30 kW'lık bir gerilim kaynaklı DC/AC dönüştürücü tasarlanmış, benzetimi yapılmış, laboratuvar ortamında test edilmiş ve ardından ekonomik değerlendirmeler yapılmıştır. Ek olarak bu tezde yüksek anahtarlama frekanslarında çalışan geniş bant aralıklı yarı iletkenli bir gerilim kaynaklı DC/AC dönüştürücüde geri besleme hattı sinyal gürültü süzgeci gecikmesi, PWM gecikmesi ve kontrol gecikmesinin sistemin kontrol performansı üzerindeki etkisi araştırılmıştır. Şebeke akım kontrolü ve dönüştürücü akım kontrol yöntemleri, modelleme ve benzetim ile karşılaştırılarak önerilerde bulunulmuştur.

Anahtar Kelimeler: Verim, Fotovoltaik, Yatırım Getirisi, Silisyum Karbür (SiC), Gerilim Kaynaklı Dönüştürücü (VSC)

To My Family and To My Nation

ACKNOWLEDGEMENTS

I would like to express my sincere thanks to my supervisor, Prof. Dr. Ahmet M. Hava, for his guidance, support, and valuable critiques throughout my study. Without his valuable expertise, I would not be able to complete my graduate study.

I would like to share my special appreciation with Mr. Fatih Kavaslar, Mr. Semih Kavurucu and Mr. Volkan Öztemel for sharing their precious engineering experience with me. In addition, I share my appreciation with Mr. Halim Özmen for sharing his semiconductor market forecast with me. With their contributions, I have gained an engineering insight about design and economics of three-phase VSCs.

I am grateful to my friends Alican Madan, Arın Cengiz, and Merih Eren for all the beneficial discussions we had during my thesis study. These discussions often resulted in new solutions in the points where I was stuck and enhanced my motivation.

I express my deepest gratitude to my family, my father Mesut, my mother Aysun, and my brother Alperen, for their unconditional support during my graduate study. Their support has always motivated me and made me stay strong in the most difficult points of my graduate study.

Finally, I would like to express my sincere gratitude to my dearest love Ainash Seitova for her endless support in all aspects of my life and for her patience during my thesis study. Without her support, I would not be able to complete this thesis.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

CCF	Converter current feedback
DEG	Distributed energy generation
DER	Distributed energy resources
DES	Distributed energy storage
EMI	Electromagnetic interference
FIT	Feed-in-Tariff
GaN	Gallium nitride
GCF	Grid current feedback
H-IGBT	Hybrid IGBT
IGBT	Insulated gate bipolar transistor
MOSFET	Metal oxide semiconductor field effect transistor
MPPT	Maximum power point tracking
NPC	Neutral point clamped
PCB	Printed circuit board
PCBA	Printed circuit board assembly
PCC	Point of common coupling
PF	Power factor
PP	Payback period
PSU	Power supply unit
PV	Photovoltaic
PWM	Pulse-width modulation

ROI	Return on investment
Si	Silicon
SiC	Silicon carbide
SPWM	Sinusoidal PWM
SVPWM	Space-vector PWM
STATCOM	Static compensator
TCO	Total cost of ownership
THD	Total harmonic distortion
UPS	Uninterruptible power supply

CHAPTER 1

INTRODUCTION

1.1. Background and Motivation

Electrical energy is the most crucial energy type in the modern world as it has many advantages such as easy generation, easy control and efficient transmission over long distances. Its distribution is not difficult, and it can be provided to the customers at exactly demanded amount and quality achieving high availability. In addition, electrical energy is a very convenient energy form and it can be simply converted in an economic and efficient way to other energy forms such as chemical energy (batteries), heat energy (electric heaters), mechanical energy (any kind of electric motors), lightning energy (LEDs, fluorescent lambs etc.), and so on.

As the human population increases in the world and developing countries keep investing on industrialization, total demand for electrical energy also increases in the world. There are various ways to generate electrical energy. Thermal power plants use fossil resources, nuclear power plants use radioactive elements, and hydro power plants use the potential energy of water as primary source. Renewable energy sources use primary sources such as solar energy, wind energy, biomass or geothermal energy. Although thermal power plants and nuclear power plants have been commonly used in generation of electrical energy so far, the possible harmful effects of nuclear and thermal power plants on the environment and human health decreased their popularity in 21st century. According to the 2018 energy outlook document of BP [1], share of nuclear energy in global electricity generation decreased to approximately 10% whereas it was above 15% at the end of 20th century as seen in **Figure 1.1**. At the same time, share of renewable energy sources dramatically increased in 21st century (approached almost 10%) and it is expected to keep increasing in the future.

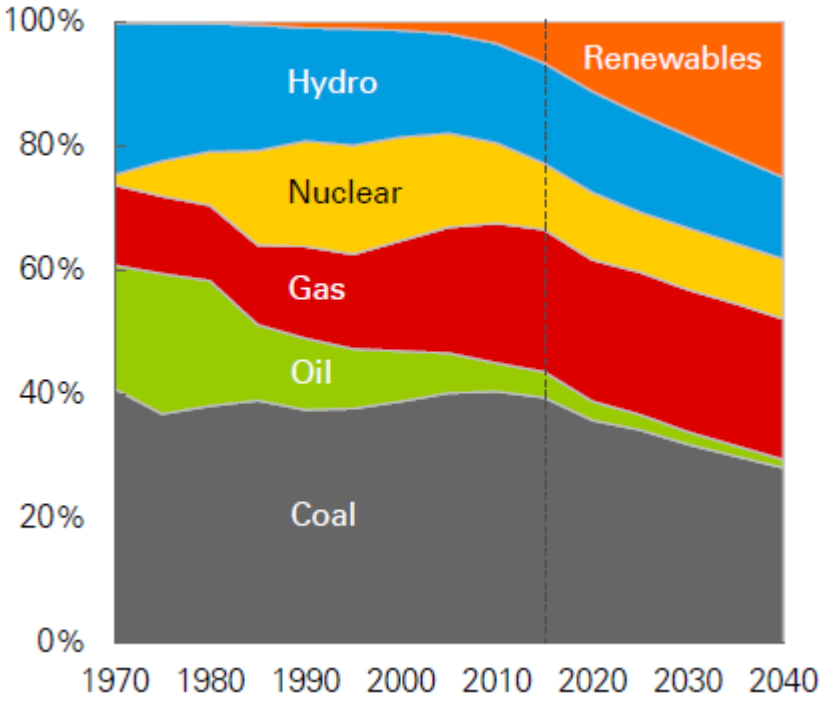


Figure 1.1 Share of total electricity generation in the world.

With increasing investments on renewable energy systems and smart grid applications, traditional power systems, where power is generated in huge power plants and transmitted long distances before consumption, has started changing. Distributed energy generation (DEG) and distributed energy storage (DES) concepts have appeared. Microgrid applications, where distributed energy resources (DER), storage units, generators, industrial loads, and residential loads are connected to the same grid, have emerged. A sample microgrid system diagram is given in **Figure 1.2** [2]. As seen in **Figure 1.2**, microgrid systems integrate a variety of applications including renewables and storage systems in a combined power system achieving higher flexibility, efficiency, and reliability. Thus, renewable energy applications can be operated in a more efficient way within microgrid systems and they become more attractive as distributed energy generation concept gets more popular with microgrid applications.

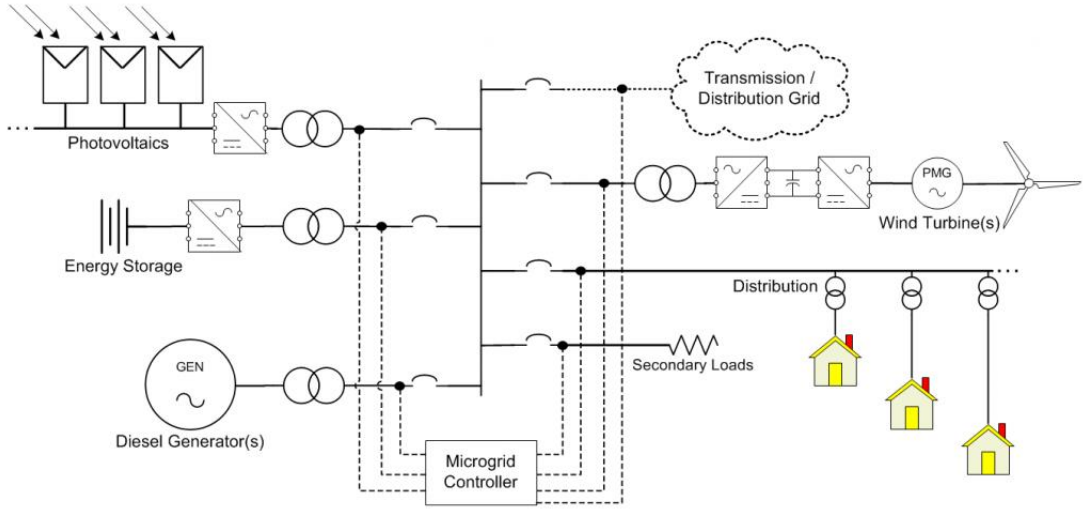


Figure 1.2 Sample microgrid system diagram [2].

Wind energy and solar energy are the most common renewable energy forms in today's world. According to the Renewable Capacity Statistics 2018 report published by IRENA (International Renewable Energy Agency), total installed wind energy capacity has increased to 513.9 GW in 2017 globally including 494.6 GW on-shore and 19.3 GW off-shore installation [3]. According to the same report, total installed solar energy capacity has increased to 390.6 GW in 2017 including 385.6 GW photovoltaic (PV) installation and 4.9 GW concentrated solar plant installation. The increase of installed wind and solar energy capacity in the last 10 years can be seen in **Figure 1.3**. As clearly seen, most of the wind installations are completed as on-shore systems and most of the solar energy installations are completed as PV installations.

Renewable energy capacity also keeps increasing in Turkey. According to the information on the website of Republic of Turkey Ministry of Energy and Naturel Resources [4], total installed wind energy capacity has increased to 7 GW and total installed PV capacity has reached 5 GW by February 2019 in Turkey.

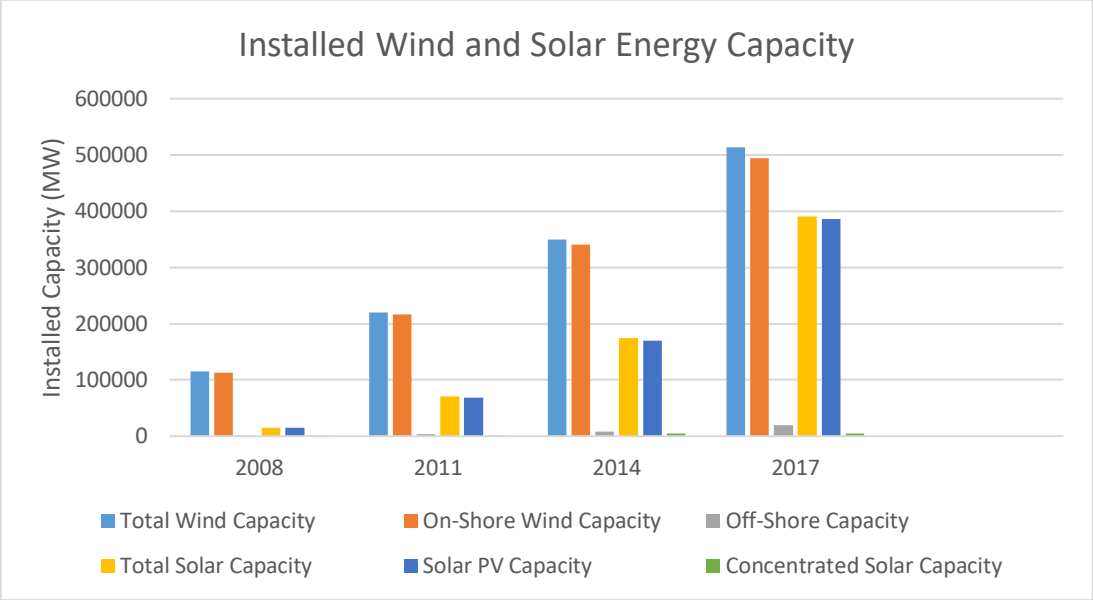


Figure 1.3 Globally installed wind and solar energy capacity [3].

As renewable energy system installations have increased dramatically in the 21st century, they become the most popular components in microgrid power systems. Although multi-megawatt scale wind turbine plants can directly connect to the medium voltage AC grid, low voltage AC microgrids form the most common microgrid system type. In this modern grid structure, renewable energy resources, storage systems, electric vehicles, uninterruptible power supplies, industrial loads, and many other applications are expected to connect to the low voltage AC grid through a grid-connected voltage source converter (VSC) [5]. In addition, grid-connected VSCs can contribute to the stability, reliability and efficiency of the power system as active filters and static compensators (STATCOMs).

Grid-connected VSCs are widely utilized since the beginning of early 2000s with spreading of silicon based insulated gate bipolar transistors (IGBTs). First, they were used in rectifiers of transformerless uninterruptible power supply (UPS) products. Then, wind-turbine systems also started using them in back to back connected converter structure as shown in **Figure 1.2**. As wind-turbine applications are usually configured as MW-scale systems and 690 V AC grid connection is commonly used in

these applications, high power grid-connected VSCs are used in these systems. In 2004, Germany announced a feed-in-tariff (FIT) value between 0.540 – 0.624 EUR/kWh over 20 years for PV installations and pioneered the PV applications in the world [6]. Since then, grid-connected VSCs have been utilized in PV applications at accelerated rate. In the following years, grid-connected VSC market has exponentially increased with the dramatic increase of on-grid renewable energy applications. Now, on-grid energy storage applications are expected to dominate the market in the 3rd decade of 21st century and grid-connected VSCs are expected to be one of the most important components in on-grid energy storage systems too.

In PV systems, two different approaches emerged for grid-connected VSCs. First approach is central converter approach (the term inverter is avoided as it is less comprehensive than converter) and proposes using MW-scale grid-connected VSCs in solar farm applications just like wind-turbine systems. Power levels of central converters start from 250 kVA and can go up to 1 – 2 MVA. Depending on the product ratings, they can either connect to 690 V AC or 400 V AC grid. Second approach is string converter approach and proposes using grid-connected VSCs with lower power rating. Single-phase string converters are common in residential applications below 10 kVA and three-phase string converters are common in 10 kVA – 150 kVA power range. String converters mostly connect to 400 V AC grid. In addition to individual operation in rooftop applications, they can also be used in parallel connected configurations in solar farms as seen in **Figure 1.4** which shows the single line diagram of a typical PV power plant with string converter approach. A DC/DC converter, which is responsible for obtaining maximum energy harvest from PV modules, is used in this diagram but it is not essential, and it may not be used in some configurations. More information will be provided about PV systems in Chapter 2. While the PV application is dominant in general, it can be stated that the VSC is the most essential component of the modern grid connected energy systems.

In this study, three-phase grid-connected VSCs in the power range 10 kVA – 150 kVA are investigated. Although power level of these converters is not as high as MW-scale

grid-connected VSCs, the commercial volume of them is significant as they are used in many products such as UPSs, PV converters, battery converters, active filters, STATCOMs and so on. In the specified power range, a technical and economic analysis is conducted about grid-connected VSCs in this dissertation. A design method is given, technical performance is evaluated, and an economic assessment is conducted. Although the conducted analysis and obtained results are applicable to most of the grid-connected VSC applications, specifically a PV power plant application is chosen in this study to illustrate and emphasize the investigation.

Grid-connected VSC is the most technological component in a PV system and it can be denoted as the heart of a PV power plant. Moreover, it contributes to approximately 5–15% of the whole investment cost. Therefore, design, cost, and performance of these grid-connected converters are very crucial, and their study has an important value in today's research world.

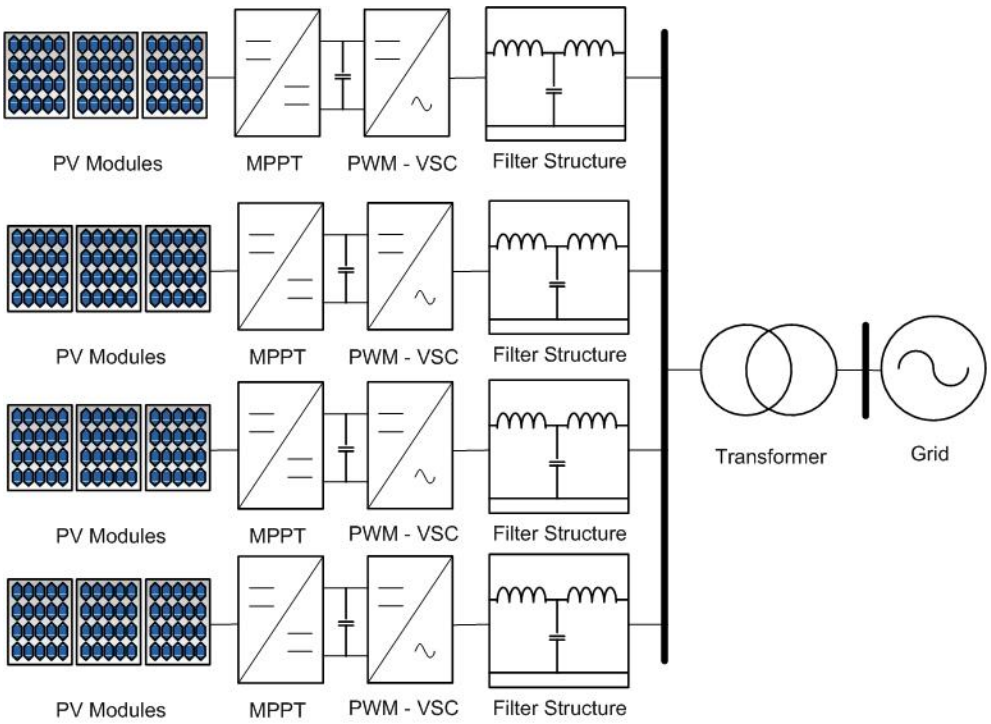


Figure 1.4 Single line diagram of a PV power plant with string converter approach.

1.2. State of the Art and Future Trend

Three-phase grid-connected VSCs for 400 V AC grid applications in the power range of 10 kVA – 150 kVA have been commonly used for more than 20 years in many applications and design of these converters are well established today. Great amount of know-how is available in terms of topology, filter design and control architecture. Semiconductor technology and device capabilities are the main parameters which determine the design limits for these converters. As Si-IGBTs are the most common device today, grid-connected VSC designs are carried out taking the Si-IGBT ratings into account.

The simplest converter topology is two-level VSC topology in today's grid-connected VSC applications. The main advantage of this topology is its simplicity and low cost. Typical DC bus voltage is kept around 750 V DC in 400 V AC grid applications and 1200 V IGBTs are suitable for this topology. However, switching frequency in this configuration is typically kept below 20 kHz in 50 kW applications and below 10 kHz for 100 kW and higher power ratings for efficiency considerations due to limited switching capability of IGBTs. The natural consequence of limited switching frequency is increased size, weight and cost of the magnetics. Size of magnetics significantly affects the size and cost of a product. In the same power range, a typical grid-connected VSC is 2-3 times larger and heavier compared to a motor drive inverter due to its filter size. Also, it costs typically 2-3 times more. A typical three-phase two-level grid-connected converter with an LCL filter structure is given in **Figure 1.5**.

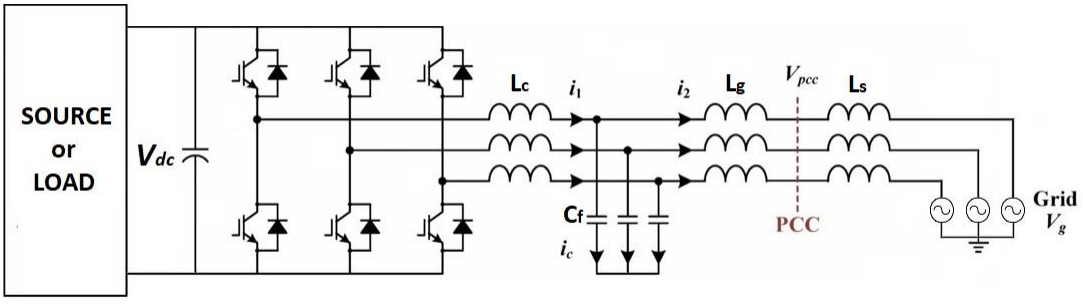


Figure 1.5 Two-level three-phase grid-connected VSC with LCL filter.

In increasing power levels, limited switching capability of conventional IGBT devices motivated designers to choose three-level topologies instead of two-level topologies. With three-level topologies, effective switching frequency can be further increased, and higher efficiency values can be achieved. However, initial cost and control complexity of the converter increases [8] - [10]. In addition, reliability decreases due to higher number of semiconductor switches. NPC type (neutral point clamped) and T type three-level converters are developed and commonly used as three-level topologies in today's applications. **Figure 1.6** shows the circuit schematics of NPC type and T type three level converter topologies.

Control of grid-connected VSCs is implemented digitally in most of the applications today by using a digital signal processor (DSP). Digital control increases the reliability and flexibility of the products. Typically, an outer voltage control loop is used to regulate the DC bus voltage and an inner current control loop is used to control the injected current to the grid. PLL algorithm is used to obtain phase angle information and synchronize with the grid. Current control can be implemented by using either grid-current feedback (GCF) or converter-current feedback (CCF) configurations depending on the measurement point of the current. A basic control diagram of a grid-connected VSC is shown in **Figure 1.7**. Each method has its own advantages and disadvantages. A detailed analysis of current control model is presented in Chapter 3.

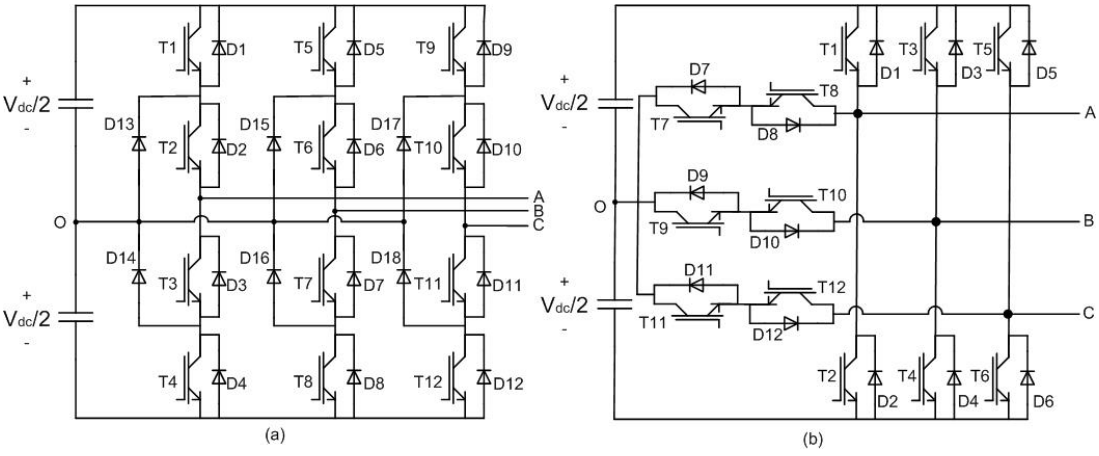


Figure 1.6 Three level converter topologies. (a) NPC type. (b) T type.

Typical filter structure used in grid-connected VSC applications is LCL filter. As also seen in **Figure 1.5**, LCL filter is composed of a converter-side inductor (L_c), a filter capacitor (C_f) and a grid-side inductor (L_g). As the VSC connects to the low voltage grid, leakage inductance of the distribution transformer (L_s) also contributes to the grid-side inductance of the filter. The main responsibility of the filter is attenuation of high frequency harmonic components which are caused by the switching action of the PWM-VSC so that injected current into the grid satisfies the grid regulations. IEEE recommended practice and requirements for harmonic control in electric power system document defines the limits for harmonic components in grid-connected equipment [11].

Today's design limits are set by Si-IGBT technology. Limited switching capability of the Si-IGBT devices result in lower switching frequencies and bigger filter size. If switching frequency is increased sacrificing the efficiency, heatsink size gets bigger. Thus, more complicated three-level topologies are improved but in fact, limitations of Si-IGBT devices still apply to three-level topologies too. Thus, thirst for increasing efficiency and reducing the size of the product brings the silicon carbide (SiC) and gallium nitride (GaN) devices into play in design of grid-connected VSCs.

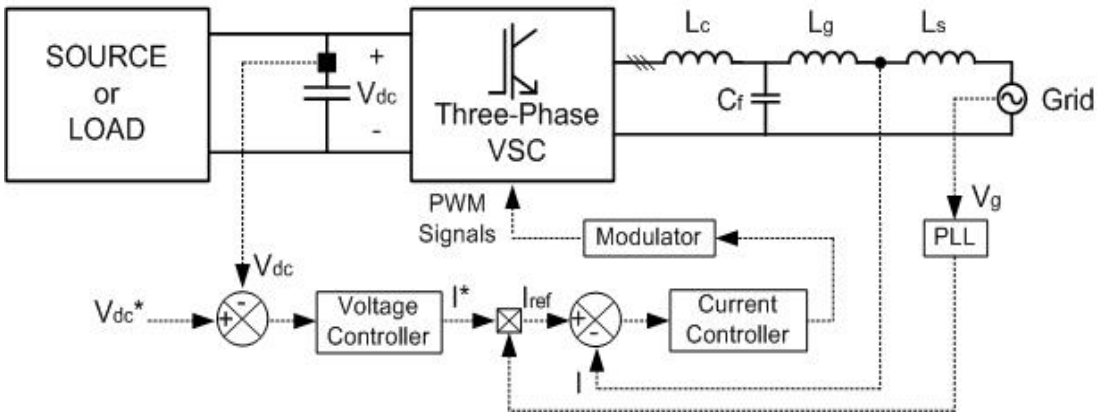


Figure 1.7 A basic control diagram of grid-connected VSC.

With the recent developments in semiconductor technology, wide bandgap semiconductors, especially SiC, make it possible to develop new power transistors with better performance compared to conventional Si based transistors [12] [13]. Basically, higher switching performance is achieved with SiC devices. Thus, switching frequency of the converters can be increased substantially and more efficient PWM-VSC designs can be conducted. As a result, filter size can be reduced achieving a weight and size reduction in the product. Moreover, lower conduction losses can be provided with low on-state resistance of SiC-MOSFETs. Eventually, efficiency can be increased with low switching and conduction losses as long as switching frequency is kept within a reasonable range. Device rating of SiC-MOSFETs can be compared with Si-IGBTs as shown in **Figure 1.8** [14]. As seen, SiC-MOSFET switching capability is superior over Si-IGBT at same power level so SiC-MOSFET is a better option at higher switching frequencies. In fact, SiC-MOSFET can be even used at applications within IGBT device ratings for higher efficiency considerations.

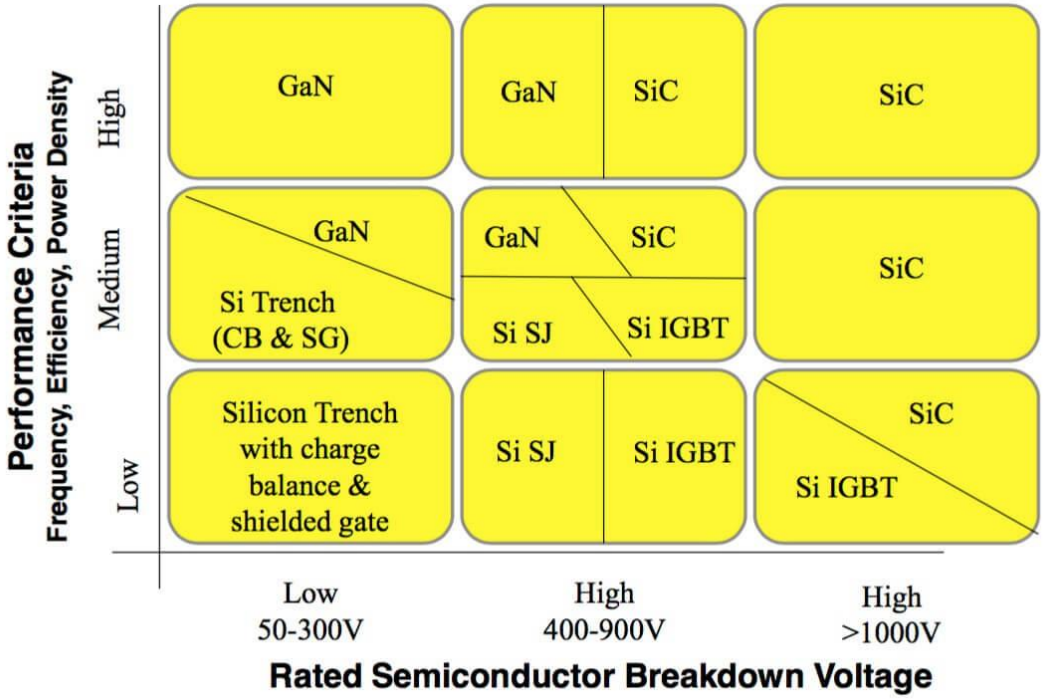


Figure 1.8 Comparison of SiC-MOSFET and Si-IGBT ratings [14].

1.3. Prior Work

In the literature, many valuable design studies have been conducted about grid-connected VSC concept. Although most of them have made significant contributions to the literature, only particular ones can be mentioned here. Three-phase converter topologies are investigated in [8], a step-by-step design procedure is given in [15] and a design method is proposed taking topology and PWM method into account in [9]. Multilevel converter topologies are analyzed in detail in [16]-[17] and effects of modulation methods are also discussed in [18]-[20].

Filter stage is also one of the most important parts of a grid-connected VSC systems as shown in **Figure 1.4** and **Figure 1.5**. Thus, filter design has been investigated in many studies. Design of a grid-connected PWM-VSC with LCL filter is studied in [21]-[22]. In addition, control and analysis of three-phase grid-connected VSCs with LCL filter are analyzed in detail in [23]-[26].

With the penetration of SiC semiconductors into the market, many researches focused on the advantages and merits of SiC devices in VSC systems. High efficiency values are achieved with superior switching characteristics of SiC-MOSFETs in different topologies and different power levels. SiC devices are used in three-level T-Type configuration in a 480 V AC grid-connected VSC for a PV application and a peak efficiency value over 98.2% is reported at 40 kW for 50 kHz switching frequency in [27]. In another research, five-level topology is used, and 99.2% peak efficiency is achieved for a 60-kW 480 V AC grid-connected VSC at 50 kHz switching frequency [28]. Studies on usage of SiC devices in two-level converter topology are also available. A comparison is conducted between Si-IGBTs and SiC JFETs through a two-level grid-connected VSC application in Fraunhofer ISE. Based on experimental measurements, the European efficiency with 4^{th} generation IGBTs is calculated as 95.4% for a 5-kW application with 16 kHz switching frequency. However, the European efficiency is calculated as 96.6% with SiC JFETs for the same application although the switching frequency is increased to 48 kHz [29]. In [30], a retrofitting

approach is used and Si-IGBT modules with Si diodes are exchanged with hybrid IGBT (H-IGBT) modules with Si-IGBT and SiC Schottky barrier diodes. In this study, approximately 0.3% efficiency increase is achieved for a two-level converter topology in 50-kW application with retrofitting. Another retrofitting approach is reported by Mitsubishi. Gate turn-off thyristor inverter is retrofitted with all SiC semiconductor switches in a traction application that uses two-level PWM converter topology with regenerative braking feature and 40% power saving is achieved according to the measurements taken between January 17 and May 8, 2015 [31].

The improvements provided by SiC devices result in economic advantages too. Financial gain calculations due to higher efficiency of SiC devices are calculated in [29]. A system cost analysis is conducted among three-level topology with Si-IGBTs and two-level topology with SiC JFETs through power module, magnetics and heatsink costs in [32]. Actually, economic evaluations have been already mentioned for conventional designs with Si-IGBT devices in the literature. A design algorithm for grid-connected VSCs considering the cost and operating factors is presented through a total cost of ownership (TCO) analysis, return on investment (ROI) and payback period (PP) calculations for three-level and two-level topologies in [33]. Similar to these studies, an economic assessment is carried out between two-level and three-level converter designs for UPS applications in [34]-[35]. These studies propose taking economic assessment of a conducted design into account and imply the importance of economic parameters in power electronics applications.

Based on prior work, topology, filter sizing and control architecture of grid-connected VSCs are already investigated in detail so far. Advantages of SiC devices in terms of switching frequency and efficiency are also mentioned in many studies. However, a study which focuses on both power hardware design and economic assessment of a three-phase grid-connected VSC application with SiC devices in detail is not available in the literature.

1.4. Scope of the Thesis

This thesis is dedicated to the technical and economic investigation of grid-connected three-phase VSCs with SiC devices in PV power plant applications. There are two main contributions of the thesis.

The first contribution is the guidance for retrofitting design approach where Si based power hardware (power module, heatsink and filter) of an already existing PV converter is exchanged with a new power hardware with a H-IGBT or a SiC-MOSFET module. Switching frequency is enhanced. Then, heatsink sizing and filter design are conducted accordingly. While transitioning from the Si to SiC technology, it is possible to either start a totally new design from scratch or to increment a design from Si technology. In this study, the second approach is preferred. This approach guides the Si-based design engineer to the result in fair comparison with the SiC technology.

Second contribution is the grid-connected three-phase VSC design methodology which takes the economic aspects into account during design process. While in industry typically the application field constraint is gained via know-how, a-priori design involving the application conditions is rare due to lack of knowledge and methodology in merging the technical and economical specs into one pot considering the specific application. This study exactly attempts to guide the VSC design for PV applications considering the TCO, ROI and PP parameters. A PV system case study is conducted in detail to demonstrate the approach. Analysis are conducted in six different locations to show the effect of geography (irradiance, temperature etc.) on the economic performance of a design. Therefore, economic aspects of the design are assessed easily.

The thesis has six chapters. Chapter 2 presents the PV system configurations in solar systems. Components of a typical PV power plant system are introduced. Central converter and string converter approaches are compared. Standards and regulations about grid-connected VSCs in PV applications are mentioned. At the end of the

chapter, a PV power plant configuration is designed with string converter approach. This plant will be used as an example in the VSC studies in the following chapters.

In Chapter 3, grid-connected converter technologies are reviewed in terms of topology, modulation method, semiconductor technology, filter structure and control architecture. Two-level topologies are specifically focused and compared for PV applications in terms of common-mode voltage and leakage current components due to parasitic capacitance between PV modules and ground. Moreover, GCF and CCF control configurations are mentioned and stability of the VSC is investigated for particular cases with pole-zero charts for GCF configuration.

Chapter 4 is dedicated to the design of a 30-kVA three-phase grid-connected VSC. A loss calculation algorithm is developed to calculate the semiconductor losses at given conditions and steady-state thermal model of the system is used for heatsink sizing. Determination of LCL filter parameters is explained and an inductor design method is presented for converter side inductance with powder cores. Inductor losses are calculated including both core and copper losses. An algorithm is developed the calculate the core losses of the converter side inductors of a grid-connected PWM-VSC. Once the hardware design is completed, control method of the VSC is also given. Steady-state operation is shown with simulations and expected efficiency values are calculated. Calculated efficiency values are verified by experimental results. In this chapter, a reference design is provided with Si-IGBT module. This reference design is accepted as base and progressive design cases are proposed with H-IGBT and SiC-MOSFET modules to mention the advantages of H-IGBT and SiC-MOSFET modules. In each case, presented design steps are repeated for H-IGBT and SiC-MOSFET modules. Eventually, efficiency curves (efficiency vs load) are obtained and euro efficiency values are calculated for four different design cases with Si-IGBT, H- IGBT and SiC-MOSFET modules.

Chapter 5 presents the economic assessment of the conducted designs in Chapter 4. A differential economic evaluation method is presented. Common parts of the designs

are excluded from economic evaluation. Only power semiconductor module, heatsink and inductor costs are taken into account and a differential TCO (ΔTCO) analysis is provided through cost difference of these components. Once the cost difference between initial investment values is determined, PV simulations are completed in determined six different locations for the PV power plant that is designed in Chapter 2. Obtained efficiency curves in Chapter 4 are used in calculation of annual energy harvest values. The differences between annual energy harvest values are calculated and by using the FIT values in these six locations, differences between annual yield values are obtained. Then, PP values are determined for all six locations for every design case with different power semiconductor modules. In addition, differential ROI (ΔROI) values are calculated for each case. As a result, economic feasibility of H-IGBT and SiC-MOSFET modules are evaluated in this chapter in PV power plants with string converter approach.

Chapter 6 provides the conclusion for the dissertation. A summary of the obtained results and experience during the study is provided. Achieved improvements and developments are mentioned. Future work is addressed.

CHAPTER 2

THREE-PHASE GRID-CONNECTED PV SYSTEM CONFIGURATIONS

2.1. Introduction

As mentioned in Chapter 1, distributed energy generation concept has merged since the beginning of 2000s with the integration of renewable energy resources into the power system. Among renewable energy resources, especially PV systems have captured an enormous attention in the last decade. PV systems can be installed either as grid-connected systems, which are often called as “on-grid PV systems”, or stand-alone systems which are often called as “off-grid PV systems”. In this chapter, on-grid PV systems are investigated, and a background is provided about on-grid PV system applications and system components.

First, most common on-grid PV application types are presented, and their trade mechanism in energy market is explained. Second, two main system components, PV modules and PV converters, are introduced. Especially solar farm applications are focused, and PV converters are investigated in a more detailed way through these applications. PV converter types are compared in terms of cost and performance for MW-scale PV power plants applications. Efficiency definitions for PV converters are provided and important standards and regulations that PV converters have to satisfy about power quality, safety and grid control are mentioned.

At the end of the chapter, an example 1-MW PV power plant is designed with 30-kW PV converters for six different locations. PV module configurations are designed taking the application site environmental conditions into account and all the electrical parameters of the PV power plant on both DC and AC sides are provided.

2.2. On-Grid PV Application Types

There are various on-grid PV application types depending on the power range, application site, and grid-connection type.

Residential applications are common up to 10 kVA power level. Usually these systems are installed as rooftop applications and single-phase grid-connection is commonly preferred, so single-phase PV converters are used. Beyond 10 kVA power level, commercial rooftop applications are common. Suitable office, residence, shopping mall, factory, etc. roofs can be used for solar installations. Power levels can go up to MVA scale depending on the available roof area. Three-phase PV converters are available for these applications in 10 kVA – 150 kVA power level, and they are named as string converters in PV industry. Most of the time rooftop applications are directly connected to the low voltage grid.

Apart from rooftop applications, there are solar farm applications. Solar farms can be installed in the power range starting from 250 kVA to multi MVA scale. Central converters are developed for these PV power plant applications, but string converters can also be used in parallel connected configurations. Usually these PV power plants are connected to the medium voltage grid via a distribution transformer.

Generated electrical energy in on-grid PV systems can be used for own consumption or sold to the utility grid depending on the application properties. In each region, there are different laws and regulations to set the rules regarding the electricity trade in on-grid PV applications. As renewable energy applications are supported by most of the governments and local authorities due to their positive environmental effects, usually it is guaranteed to sell the generated electricity in on-grid PV systems. A feed-in-tariff (FIT) value is determined for the cost of the unit electrical energy that is sold to the utility grid from an on-grid PV system by local authorities and energy trade is conducted on this value. Economic assessment of an on-grid PV system (PP, ROI) can be carried out using these FIT values.

2.3. PV Modules

PV modules are the actual DC sources in grid-connected PV systems. They are usually denoted in total as “PV generator”. The main responsibility of PV modules is the photovoltaic energy conversion. Basically, PV modules absorb the incoming sunlight and generate DC current with this absorbed energy. In other words, they operate according to the photoelectric effect [36].

The current-voltage characteristics of PV modules are not linear. Between open-circuit voltage and short-circuit current point, there is an optimum operation point which is named as maximum power point (MPP). When PV modules operate at this point, maximum energy harvest is achieved [39]. **Figure 2.1** shows the I-V characteristics of a single PV module and its series/parallel connected configurations. As clearly seen, parallel connection of modules increases the overall current whereas the series connection of modules increases the overall voltage.

In PV applications, 1000 V is the today’s standard for maximum voltage and higher voltages such as 1500 V are also getting more attraction day by day. Thus, it is a common practice to connect PV modules in series as much as possible in such a way that open-circuit voltage does not exceed maximum voltage rating of the used equipment in PV system. Especially in solar farms, where the PV modules are distributed over a large area, higher PV voltage has a crucial importance in terms of DC cabling losses. Therefore, forming strings by series connection of PV modules is a very common method. Once the maximum allowable voltage limit is approached by series connection of PV modules, only then parallel strings are added to the PV module group to achieve desired power level.

There are various types of PV modules available in the market. Monocrystalline, polycrystalline and thin-film modules are the most common PV module types. Each PV module type has its own advantages in terms of cost, performance and feasibility depending on application site.

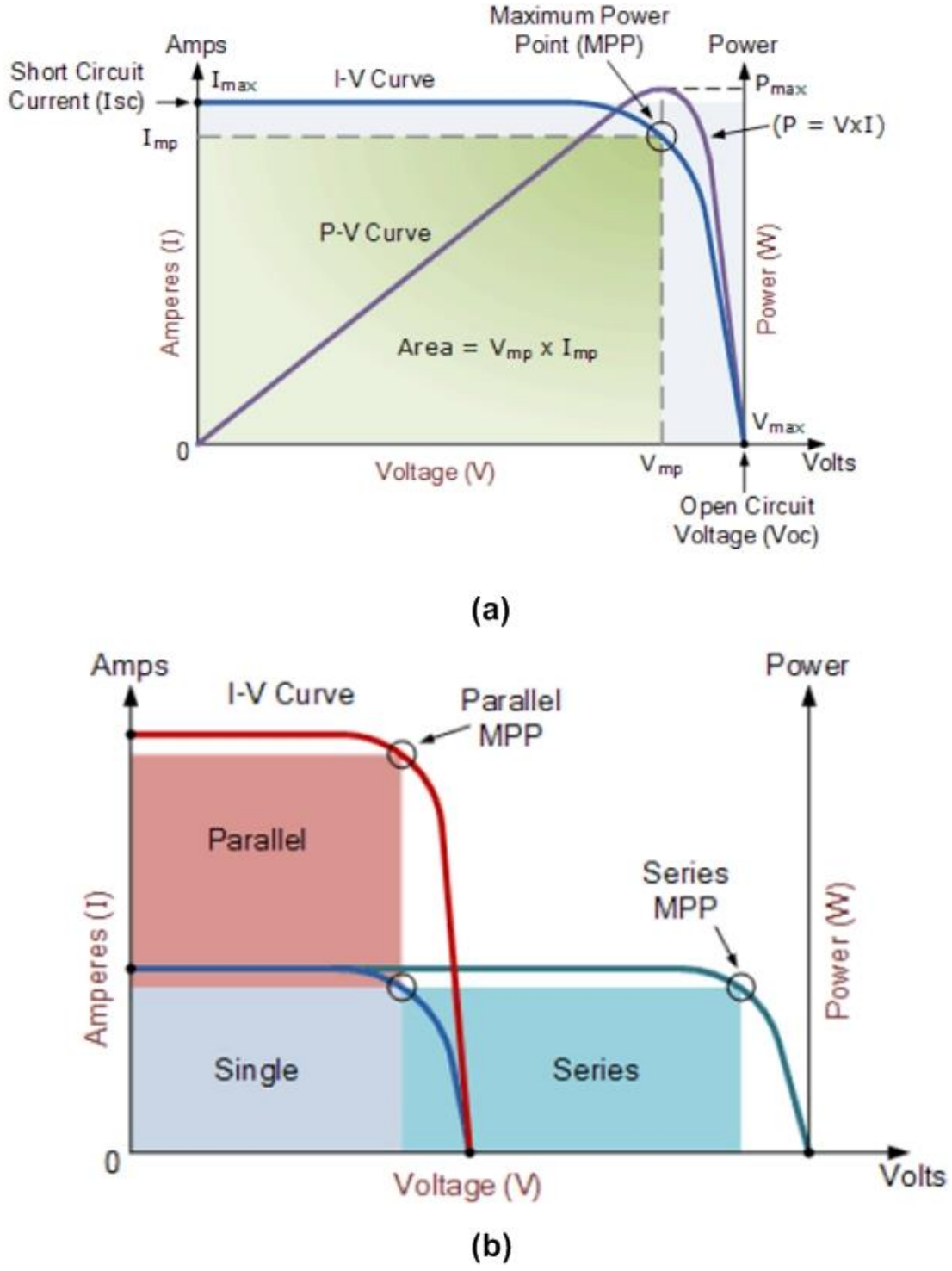


Figure 2.1 (a) I-V characteristics of a PV module (b) I-V characteristics of series/parallel connected PV modules [39].

Monocrystalline modules have the highest efficiency values, so they are the most space efficient modules. That is why they are commonly preferred in rooftop applications where available space is limited. Moreover, they have quite long lifetime. Most of the manufacturers give warranty over 20 years for monocrystalline PV modules. However, their cost is high, and it increases the initial investment cost [37].

On the other hand, polycrystalline PV modules are less efficient compared to monocrystalline PV modules, and they require larger space for the same output power level. However, their manufacturing process is relatively simpler, and this decreases their cost [37]. Thus, polycrystalline PV modules are commonly preferred especially in solar farm applications where space is not a very crucial constraint. As expected, a polycrystalline PV module is selected for the PV power plant application in this study.

Different than monocrystalline and polycrystalline PV modules, there are also thin film PV modules. Amorphous silicon (a-Si) and cadmium telluride (CdTe) are the most common materials that are used in their structure. Their flexible structure makes them superior in applications where an irregular surface needs to be covered with PV modules. Another great advantage of them is that their mass production is very simple. Therefore, their cost is low. However, their efficiency is low, so they occupy a larger area for a specific power output compared to other PV module technologies.

2.4. PV Converters

PV converters are responsible for converting the DC current, which is generated by PV modules, to AC in synchronization with grid voltage in on-grid PV systems. In this way, they inject the obtained power from PV modules to the utility grid. By structure, a PV converter is actually composed of a grid-connected VSC. However, PV converter term is commonly used in PV industry instead of grid-connected VSC. Thus, in this chapter also PV converter term is used instead of grid-connected VSC.

There are several PV converter types as also mentioned in on-grid PV application types earlier in this chapter. PV converters can be grouped in three main categories named as micro converters, string converters, and central converters.

Micro converters are available below kVA range. They perform maximum power point tracking (MPPT) operation at PV module scale. Their biggest advantage is maximum energy harvest from each PV module in a whole PV system. However, as the number of micro converters is equal to number of PV modules in such a system, the cost is high, and they are not common in applications beyond 10 kVA.

Single-phase string converters are available till 10 kVA power level and three-phase string converters are available in the power range 10 kVA – 150 kVA. String converters provide MPPT control at string or multi-string level. They are commonly used in rooftop applications. However, they can also be used in solar farm applications in parallel connected configurations. Most of the string converters can directly connect to the low voltage utility grid without needing a special transformer.

Central converters are developed for MW-scale power plants. They are available from 250 kVA to 2500 kVA power level. They perform MPPT control at PV power plant scale and they usually require a special transformer to connect the utility grid. Their biggest advantage is low cost per kW compared to string converters.

Both string converters and central converters have certain advantages in PV power plant systems. **Table 2.1** provides a comparison between string and central converters for solar farm applications. Although string converters have higher cost, they provide more MPPT inputs for the same power level, higher redundancy and higher design flexibility. In addition, low weight of string converters provides higher portability and increases technical service convenience. As a result, although central converters have been more common in solar farm applications before, recently string converters have also found themselves a significant place in these applications. **Figure 2.2** shows the share of string converters in the installed PV systems in the USA. As clearly seen, share of string converters continuously increase since 2015 and it is expected to keep increasing in the future. Thus, string converter approach is chosen to be the focus in this study. All the discussions and explanations are carried on through a solar farm application with string converters.

Table 2.1 Three-phase central converter vs string converter comparison

	Central Converter	**String Converters**
Power Range	250 kW to 2.5 MW	10 kW to 150 kW
Application	Solar farms	Solar farms and rooftop applications
Efficiency	High	Lower
Cost per kW	Low	Higher
Number of MPPT	Usually single MPPT input at central level	Multiple MPPT inputs for the same power level
Redundancy	Low	High
Monitoring	Power plant level	String level
Weight per Product	Typically, above 500 kg	Typically, below 100 kg
Design Flexibility	Low	High
Additional Costs	Container or another structure for housing	AC switchgear board for grid connection

String converters can be either in single-conversion or double-conversion structure depending on whether they employ a DC-DC converter at the input or not. Both approaches have different advantages. Although single-conversion approach yields higher peak efficiency, it has limited MPPT voltage range because MPPT algorithm is carried out by the grid-connected VSC. For 400 V AC grid, theoretically minimum 580 V (in SVPWM) or 650 V (in SPWM) DC bus voltage is required for linear operation depending on the modulation method [40]. If MPP voltage is below this limit, PV converter cannot track MPP and energy harvest from PV modules cannot be maximized. On the other hand, employing a boost converter at the input brings the advantage of increased MPPT voltage range. MPPT range can be even extended till 100 – 200 V levels. However, this approach has the disadvantage of higher cost and lower peak efficiency. Geographical conditions and application properties determine which approach is superior. Very high temperature in sunny days or low irradiance in cloudy days are two common situations which may decrease the PV string voltage significantly. If application site is subjected to these conditions, double conversion approach is a better option. In this study, double conversion structure is preferred in order to maximize the energy harvest from PV modules and not to lose any irradiation.

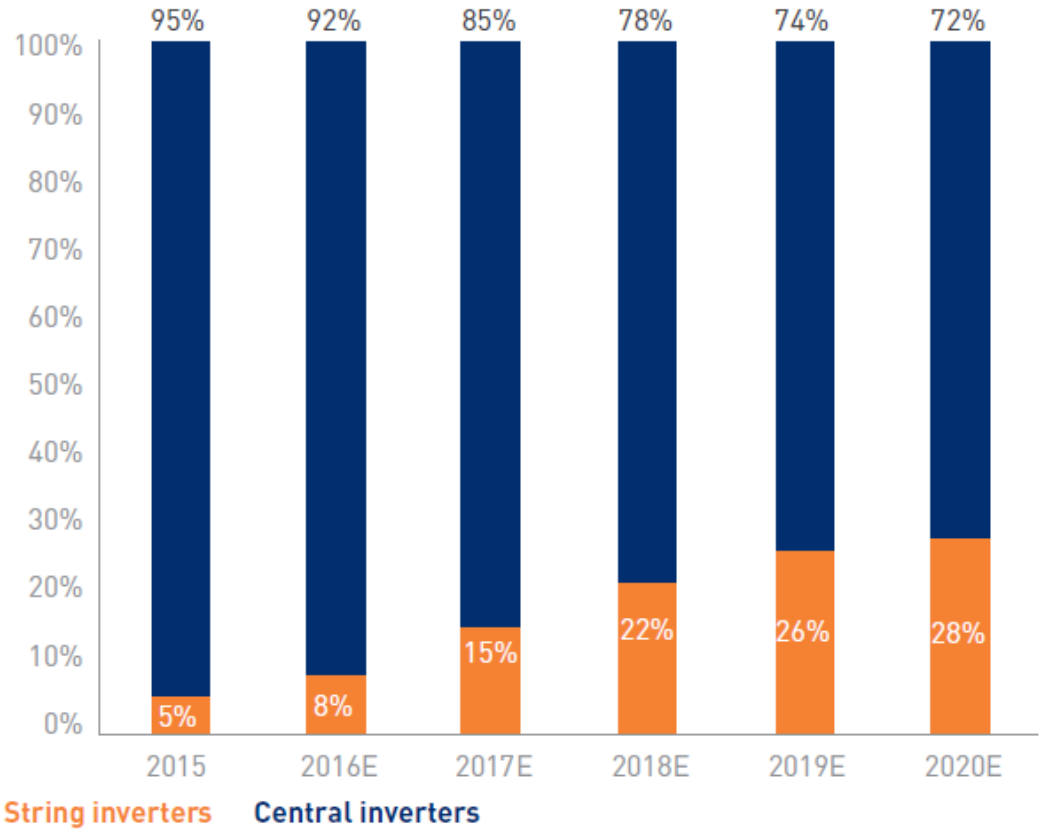


Figure 2.2 Share of string converters in installed PV systems in the USA [7].

2.4.1. Efficiency of PV Converters

Efficiency of PV converters is crucial as it directly affects the amount of energy injected to the grid. However, PV converters do not always operate at rated power due to intermittent nature of PV energy. Typical output power characteristics of a PV power plant for sunny and cloudy days are given in **Figure 2.3**. As clearly seen, a PV power plant operates close to its rated power for only 3-4 hours in a sunny day while it does not even approach this value in a cloudy day. That is why, an efficiency parameter called “euro efficiency” is proposed to define a weighted efficiency value using efficiency vs load curves of the converters. By definition, euro efficiency equation is given in (2.1) [66].

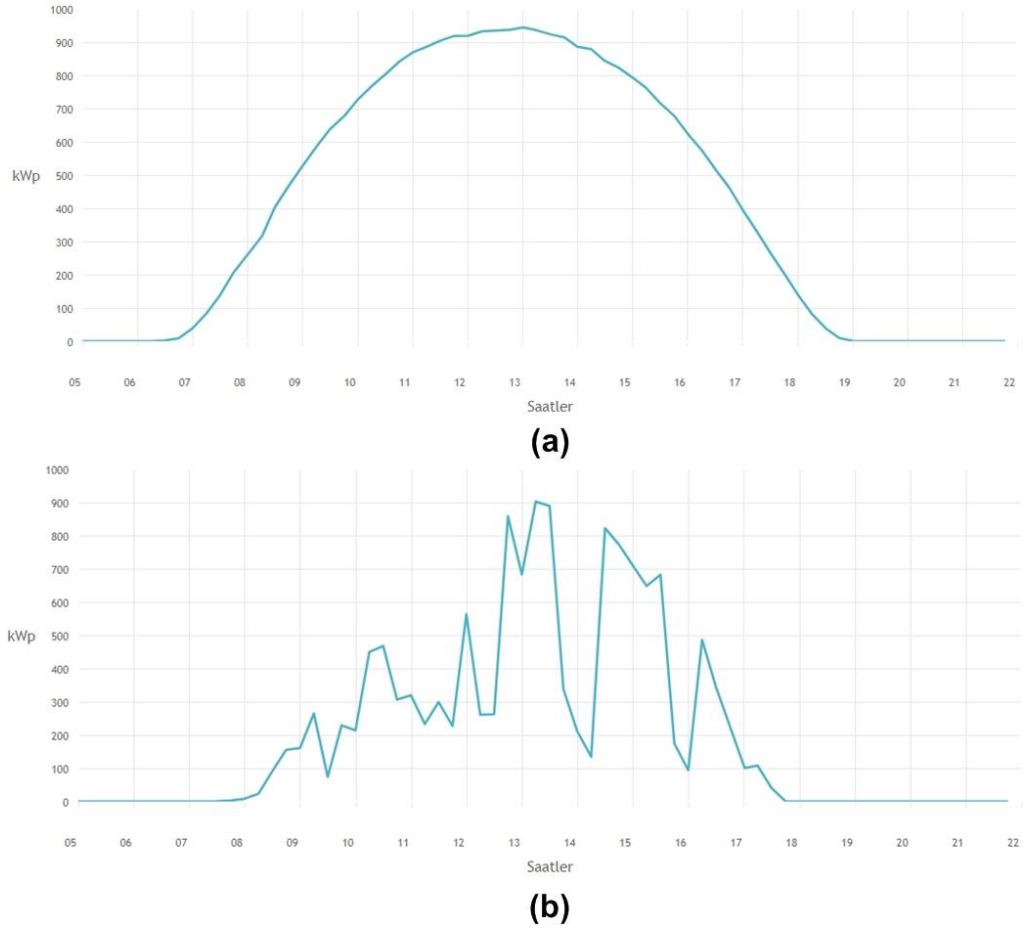


Figure 2.3 Typical power characteristics of a 1 MW power plant. (a) Sunny day. (b) Cloudy day [45].

In addition to euro efficiency, another efficiency concept named as "CEC efficiency" is proposed by California Energy Commission. CEC efficiency is more commonly used for PV converters in the USA and it is more suitable for regions with higher irradiance. By definition, CEC efficiency equation is given in (2.2) [66].

$$\eta_{euro} = 0.03\eta_{5\%} + 0.06\eta_{10\%} + 0.13\eta_{20\%} + 0.10\eta_{30\%} + 0.48\eta_{50\%} + 0.2\eta_{100\%} \quad (2.1)$$

$$\eta_{CEC} = 0.04\eta_{10\%} + 0.05\eta_{20\%} + 0.12\eta_{30\%} + 0.21\eta_{50\%} + 0.53\eta_{75\%} + 0.05\eta_{100\%} \quad (2.2)$$

2.4.2. Standards and Regulations

PV converters have to satisfy a set of standards and regulations. IEEE Std 519^{TM}-2014 is the most common recommendation document for power quality requirements for the grid-connected applications [11]. Limits are set for injected harmonic components to the grid up to 50th component. This is essential for sustaining the power quality of the grid and all grid-connected converters must satisfy the requirements in this document. Thus, design of the PWM-VSC must be conducted taking these limits into account and especially sizing of the filter components must be done accordingly. **Table 2.2** provides the current distortion limits for power generation equipment connected to the low voltage grid (from 120 V to 69 kV) in percent of maximum demand load current (fundamental frequency component) at the point of common coupling (PCC). Note that current distortions that cause DC offset are not allowed and even harmonic limits are limited to 25% of the defined odd harmonic limits.

IEC 61727:2004 provides utility interface characteristics for grid-connected power electronics equipment in PV systems [41]. This standard is a must for commercial on-grid PV converters. According to IEC 61727, PV converters are required to disconnect from the grid within given tripping times in **Table 2.3** when grid voltage or frequency goes out of the shown limits.

Table 2.2 Current distortion limits for power generation equipment connected to the low voltage grid in percent of maximum demand load current at the PCC

Individual Harmonic Order (Odd Harmonics)					
3≤h<11	11≤h<17	17≤h<23	23≤h<35	35≤h<50	TDD
4	2	1.5	0.6	0.3	5

Table 2.3 IEC 61727 tripping time requirements for the PV converter

	Lower Limit	**Upper Limit**	**Tripping Time**
Grid Voltage	50%	135%	0.1s / 0.05s
	85%	110%	2.0 s
Grid Frequency	-1 Hz	+1 Hz	0.2 s

In addition to voltage and frequency deviations, islanding protection is also mentioned in IEC 61727 and IEC 62116:2014 standard is proposed as test procedure for islanding prevention measures for utility interconnected PV systems [42]. According to IEC 61727, a PV converter must inject 1% of its rated current to the grid periodically to check possible islanding situation and disconnect from the grid within 2 seconds once it detects that it is islanded. Anti-islanding protection has two main purposes. First, it prevents a possible electric shock of technical service technicians if power grid is intentionally disconnected for a maintenance operation. Second, it prevents the possible asynchronization between the grid and PV converter when the grid is available again after a power cut period.

Apart from the standards about power quality and grid interface, there are also standards related with safety. IEC 62109-1:2010 defines the minimum requirements about the design of PV converters for protection against electric shock and other hazards such as fire [43]. The second part of this standard, which is named as IEC 62109-2:2011, covers particular safety requirements about PV converters (DC to AC power conversion products) in PV systems [44].

According to IEC 62109-2, continuous residual current limit is set as 300 mA for the PV converters up to 30 kVA power rating. For the converters with higher power rating, continuous residual current limit is determined as multiplication of rated power value (in kVA) with 10 mA (for example the limit is determined as 600 mA for 60 kVA PV converter). In case of detection of a continuous residual current which is larger than the specified limits, PV converter must disconnect from the grid and turn off in 0.3 seconds. In addition, PV converter is also expected to detect the sudden changes in residual current as they may be related with an electric shock incident. Again, according to the same standard, PV converter must disconnect from the grid and turn off in 0.3 seconds in case of a 30-mA residual current jump. Similarly, tripping times are set as 0.15 seconds and 0.04 seconds in case of 60-mA and 150-mA residual current jump incidents respectively.

When on-grid PV installations first emerged, PV converters were expected to operate at unity power factor all the time injecting only active power to the grid. In other words, they were operating in grid following mode. However, with increasing number of on-grid PV systems, today PV converters are supposed to operate in grid supporting mode. EN50549-1 mentions some of the grid supporting functions such as static voltage support by reactive power control and dynamic grid support with fault-ride-through properties [46]. Future trend shows that islanded mode operation may also be required from PV converters in microgrid applications. Thus, next step can be named as grid forming mode operation of PV converters.

2.5. Solar Farm Applications

As mentioned earlier in this chapter, solar farm applications are the main focus in this study. A typical layout for a solar farm application is given in **Figure 2.4**. PV modules convert the solar irradiation into DC current and they are connected in series to form PV strings. DC combiner boxes are used to gather the output currents of PV strings. If PV converters can control each string in the power plant with independent MPPT inputs, then DC combiner boxes may not be needed, and PV strings can be directly connected to the MPPT inputs. However, this approach has a higher cost as it requires a separate DC-DC converter for each string. Thus, if there is no significant difference between the operating conditions of the strings, in other words, if it is not crucial to control each string independently, single MPPT approach is chosen due to its low cost. In solar farm applications, as PV modules are subject to the almost same conditions, this approach is commonly preferred and DC combiner boxes are used.

As seen in **Figure 2.4**, string fuses are used in DC combiner boxes. Strings are connected to the same busbar (positive and negative busbars) in the DC combiner box and they must be protected with fuses because if one of the strings is shaded, currents of other strings can flow into the shaded string and damage the PV modules. A DC isolator is also used in DC combiner box to isolate the PV strings from PV converter in case of a technical service or maintenance operation. However, as this DC isolator

is not a circuit breaker, it must be turned on/off under no load conditions. Otherwise, arcing may occur, and DC isolator or even DC combiner box itself may be damaged.

Output of DC combiner box is connected to the DC-DC converter of the PV converter. Here, it is a common practice to use NH fuse ("Niederspannungs Hochleistungs" in German) at the input of the PV converter to provide short circuit protection at DC side. This DC-DC converter is usually chosen as a boost converter and it guarantees the operation of the PV modules at MPP, maximizing the energy harvest from PV modules. At its output, it creates the DC link voltage for the three-phase grid-connected PWM-VSC.

As there are many string converters in a solar farm, an AC switchgear board is necessary to control the grid-connection of the converters. AC circuit breakers are used here to provide protection for possible short-circuit at the output of PV converters. These circuit breakers are also used to de-energize the converters for maintenance operations.

Outputs of the converters are gathered at the AC switchgear and they are connected to the grid through a transformer. This transformer provides galvanic isolation between PV modules and the grid. Typically, a 1250 kVA transformer is used in a 1-MW PV power plant. It is common to employ a capacitor bank to compensate the reactive power consumption of this power transformer. Otherwise, reactive power consumption of the transformer may cause a penalty especially at nights depending on the utility policy.

2.6. An Example PV Power Plant

A 1-MW PV power plant application is configured in this section later to be analyzed in this study. String converter approach is chosen with 30-kW converters because string converters provide more MPPT inputs for same power level and provide better redundancy compared to central converters. Thus, higher annual energy harvest is expected with string converters.

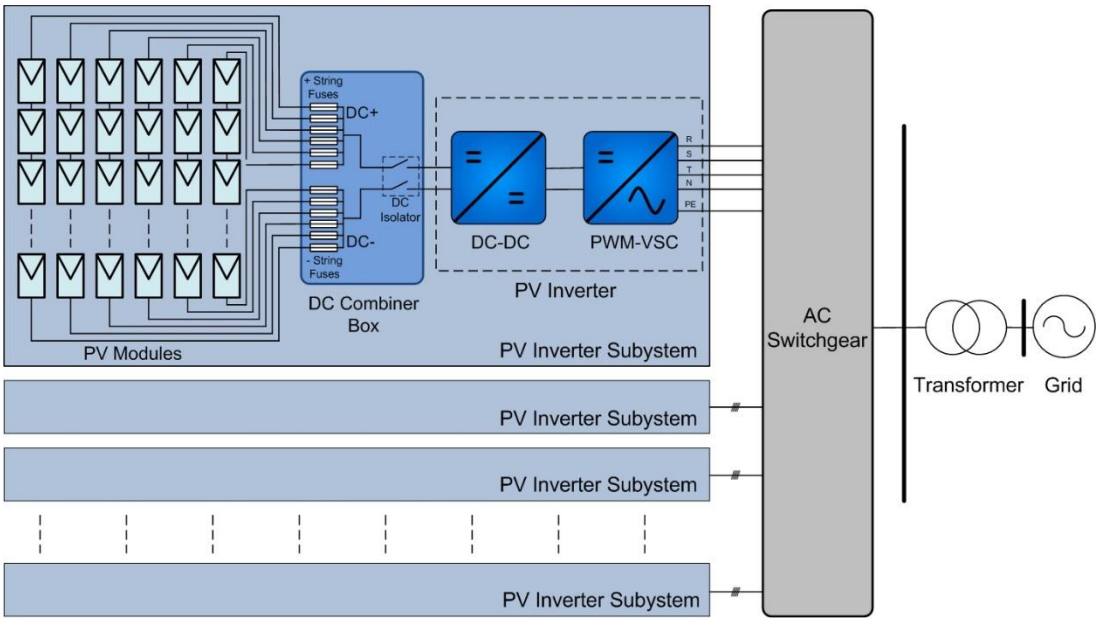


Figure 2.4 Typical solar farm layout with string converter approach.

Nominal DC power is adjusted as approximately 15% higher than rated AC power because DC-AC overloading is a common practice in MW scale PV power plants [7]. The main reason of this common practice is that nominal DC power of the PV modules are defined in standard test conditions (1000 W/m^2 irradiance and 25 °C module temperature) and these conditions are rarely supposed to occur in real conditions. Either irradiance does not reach 1000 W/m^2 levels or PV module temperature exceeds 25 °C with increasing current at full-load.

The maximum voltage ratings of the equipment used in the PV system (PV converters, cables, circuit breakers and so on) is defined as 1000 V in this study. Thus, open-circuit voltage of the PV modules should not exceed 1000 V. Voltage temperature coefficient (U_{oc}) of the PV modules is used to calculate the maximum possible voltage at the coldest condition as show in equation (2.3). However, the coldest temperature that PV modules can experience under sunlight depends on the climate of the installation location. In addition, it is difficult to guess the irradiance level at the coldest moments during daytime. Thus, with a safety margin, it is assumed that -25 ºC is the coldest temperature that PV modules experience under 1000 W/m^2 irradiance.

$$V_{max} = V_{oc}(25°C) * (\frac{100+(25°C - T_{coldest})*U_{oc}}{100}) \quad (2.3)$$

JKM260PP-60 polycrystalline PV module (260 W) is used in this PV power plant application. According to the equation (2.3), series connection of 23 modules exceed the 1000 V limit at 1000 W/m^2 irradiance and -25 ºC conditions [38]. Thus, at most 22 series modules can be used in one string. As 30-kW PV converters are used in the power plant, 6 strings can be used for one converter resulting in 34320 W rated DC power. This means a 114.4% DC to AC loading for the PV converter. Totally, 4356 PV modules (260 W) and 33 PV converters (30-kW) are used in the PV power plant.

PV power plant is configured for six geographically different locations namely Palermo (Italy), Napoli (Italy), Milano (Italy), Konya (Turkey), Sion (Switzerland) and Tallinn (Estonia). PV converter ratings and PV power plant properties such as PV module inclination angle, azimuth angle and PV module configuration are given in **Table 2.4**. Similarly, FIT values and annual global irradiance values are also provided for each location in **Table 2.4**.

AC grid voltage is specified as 400 V and grid frequency is specified as 50 Hz. 4-wire connection is used at PV converter output (3 phases + neutral cables in addition to PE). In the PV simulations, cabling loss of the power plant is taken as 1%.

2.7. Conclusion

In this chapter, a background about on-grid PV systems is provided. On-grid PV system types are introduced, and system components are investigated. The most common PV modules and PV converter types are shown, and their application areas are defined. Efficiency definitions and required standards about PV converters are mentioned. In addition, a solar farm application is introduced and common practices in the design of a solar farm application are shown in a detailed way. At the end, a 1-MW PV power plant design is completed in three different locations later to be used in economic assessment studies.

Table 2.4 PV converter ratings and PV power plant properties

<table>
<tr><th colspan="4">Power Plant Properties</th><th colspan="2">PV Converter Properties</th></tr>
<tr><td>No. of PV Modules</td><td colspan="3">4356</td><td>No. of Converters</td><td>33</td></tr>
<tr><td>Nominal DC Power</td><td colspan="3">1132.56 kW</td><td>Rated Power</td><td>30 kW</td></tr>
<tr><td rowspan="2">PV Module and Properties at Standard Test Condition</td><td colspan="3" rowspan="2">Jinko Solar JKM260PP-60
- P_{MPP} = 260 W - V_{MP} = 31.1 V
- V_{OC} = 38.1 V - I_{MP} = 8.37 A
- I_{SC} = 8.98 A - η = 15.89 %</td><td colspan="2">VSC</td></tr>
<tr><td>DC Bus Voltage</td><td>750 V</td></tr>
<tr><td rowspan="2">PV Module Configuration</td><td colspan="3" rowspan="2">22 modules/string, 6 strings/converter</td><td>f_{sw} (kHz)</td><td>8 – 48</td></tr>
<tr><td>Grid Frequency</td><td>50 Hz</td></tr>
<tr><td>PV Module Azimuth Angle</td><td colspan="3">180°</td><td>Filter Structure</td><td>LCL</td></tr>
<tr><td>Power Plant Cabling Loss</td><td colspan="3">1%</td><td>AC Connection</td><td>3P/N/PE</td></tr>
<tr><td rowspan="6">Annual Irradiance (kWh/m^2) and PV Module Inclination (°) in Each Location</td><td>Palermo (Italy)</td><td>29°</td><td>1784 kWh/m2</td><td>Grid Voltage</td><td>400 V</td></tr>
<tr><td>Napoli (Italy)</td><td>31°</td><td>1644 kWh/m2</td><td>Power Factor</td><td>1</td></tr>
<tr><td>Milano (Italy)</td><td>32°</td><td>1307 kWh/m2</td><td colspan="2">Boost Converter</td></tr>
<tr><td>Konya (Turkey)</td><td>30°</td><td>1763 kWh/m2</td><td>Input Voltage</td><td>450 – 650 V</td></tr>
<tr><td>Sion (Switzerland)</td><td>35°</td><td>1383 kWh/m2</td><td>Output Voltage</td><td>750 V</td></tr>
<tr><td>Tallinn (Estonia)</td><td>37°</td><td>946 kWh/m2</td><td>f_{sw} (kHz)</td><td>8</td></tr>
<tr><td>Feed-In-Tariff (FIT) [47] - [51]</td><td colspan="3">0.133 USD/kWh in Turkey
*0.110 USD/kWh in Switzerland
*0.060 USD/kWh in Estonia
**0.044 USD/kWh in Italy</td><td colspan="2">Two parallel operating boost converters using dual-pack Si-IGBT modules</td></tr>
</table>

*CHF/USD rate is accepted as 1.00 and EUR/USD rate is accepted as 1.12 to convert the FIT values of Italy, Switzerland, and Estonia to USD.

**This is guaranteed minimum price (ritiro dedicato) in 2018 for photovoltaic installations in Italy.

CHAPTER 3

THREE-PHASE GRID-CONNECTED PWM-VSC TECHNOLOGIES

3.1. Introduction

Three-phase grid-connected VSCs are the most important components in modern power grids. As mentioned in Chapter 1, various applications such as renewable energy applications, storage systems and uninterruptible power supplies connect to the grid through a grid-connected VSC. As also mentioned in Chapter 2, three-phase grid-connected VSCs in 10 kVA – 150 kVA power range are employed in string converters which have a significant commercial value in today's PV market. Thus, design of three-phase grid-connected VSCs has gained an enormous attention. This chapter is specifically dedicated to the review of state of the art of three-phase grid-connected PWM-VSC technologies in 10 kVA – 150 kVA power range and analysis of used three-phase grid-connected PWM-VSC structure in this study.

The PWM-VSC is responsible for converting the DC current into AC current by switching of the semiconductor switches in a suitable manner and the filter between the VSC and the grid is responsible for attenuation of the harmonic current components which are generated by the switching action of the PWM-VSC. Switching signals of the semiconductors are created by modulator according to the control algorithm. Thus, topology of the PWM-VSC, semiconductor technology, filter properties and modulation methods are closely related. Basically, a design path requires a deep understanding of the relation between these parameters.

Many parameters affect the design of a grid-connected VSC. Cost, reliability, efficiency, size, weight and lifetime are some of these parameters. Each application has its own requirements. Size and volume can be more crucial for grid-connected VSCs in on-board electric vehicle chargers while cost and efficiency are more

important for a grid-connected VSC that is used in a PV power plant. Thus, topology, modulation method and filter structure requirements may change according to the application type and a solid background is necessary on today's grid-connected VSC technology in the desired power range to be able to conduct a proper design.

In this chapter, topologies, modulation methods, filter structures, semiconductor technologies, and control architectures which are widely used in today's three-phase grid-connected PWM-VSCs in 10 kVA – 150 kVA power range are introduced and explained in detail.

3.2. Topology and Modulation Method

3.2.1. Topologies

Among three phase converters, two-level converter topology is the simplest and one of the most common ones. The main advantage of this topology is that it can be implemented with only 6 transistors and 6 diodes as shown in **Figure 3.1**. Thus, cost of this topology is low, and its control is not complex. Reliability of the system is high as number of components is low. However, this topology has limitations. Each power transistor is responsible for blocking the whole DC bus voltage and voltage blocking rating of the semiconductors must be high accordingly. Switching of high DC voltage may cause undesired electromagnetic interference (EMI) problems due to high dV/dt rate. It also increases switching losses. Due to efficiency considerations, it is very difficult to increase switching frequency beyond 10 kHz level with conventional silicon IGBT technology beyond 100 kVA power levels. As a result, compared to multi-level converter topologies, larger filter is necessary at the output of the VSC to achieve required power quality standards.

1200 V Si-IGBTs are the optimum solution for two-level topology in 400 V AC grid applications but switching capability of Si-IGBTs is limited as mentioned. This encouraged the use of three-level topologies. With the penetration of three-level topologies into the market, 600 V IGBTs, which have better switching performance compared to 1200 V IGBTs, have also found themselves a place in 400 V AC grid

applications. Although control complexity, number of components (semiconductors, gate drives etc.) and initial cost of the final product increase, three-level topologies become standard in industry in grid-connected VSCs with Si-IGBTs at power levels especially beyond 10 kVA due to their higher efficiency advantage. Most common three-level topologies, namely NPC type and T type, are shown in **Figure 1.6**.

On the other hand, recent developments in wide bandgap semiconductor technology made SiC-MOSFETs and SiC Schottky barrier diodes available. Today Si-IGBT modules can be replaced by either full SiC-MOSFET modules or H-IGBT modules. With enhanced switching performance of SiC devices, switching losses can be kept at a reasonable level and two-level topology can still achieve a satisfactory efficiency level at higher switching frequencies by keeping other advantages of two-level topology such as low cost, low complexity, high reliability and simplicity. Thus, two-level topology again captured the attention of the designers with new SiC devices and two-level topology with SiC devices is chosen as the main focus in this study.

Two-level VSC topology with LCL filter can be implemented in three ways depending on the connection of DC bus midpoint with star point of filter capacitors and grid neutral point. It can be implemented without splitting the DC bus voltage as shown in **Figure 3.1 (a)**, or it can be implemented by splitting the DC bus voltage with a midpoint connection as shown in **Figure 3.1 (b)** and **Figure 3.1 (c)**. In **Figure 3.1 (b)**, DC bus voltage is split, and midpoint is connected to the star point of the filter capacitors. In **Figure 3.1 (c)**, again DC bus voltage is split, and midpoint is connected to both star point of filter capacitors and grid neutral. From now on, these topologies are called as floating, semi-floating and solidly-connected topologies respectively.

In PV applications, parasitic capacitances exist between PV modules and ground. These parasitic capacitances significantly affect the converter topology selection (especially in transformerless topologies) because common mode voltages can create a leakage current to the ground through these capacitances. A limit is set to these ground leakage currents in the standard IEC 62109-2 as mentioned in Chapter 2 [44].

Thus, parasitic capacitances from DC bus to the ground must be taken into account and they are also modelled in **Figure 3.1** with gray dashed lines ($C_{g\text{-}pv}$). Magnitude of these parasitic capacitances may vary from 50 nF/kW to 200 nF/kW according to the physical conditions of the PV modules (mechanical position, moisture rate, temperature etc.) [52] [53]. This value is assumed as 200 nF/kW to take the worst conditions into account in this study.

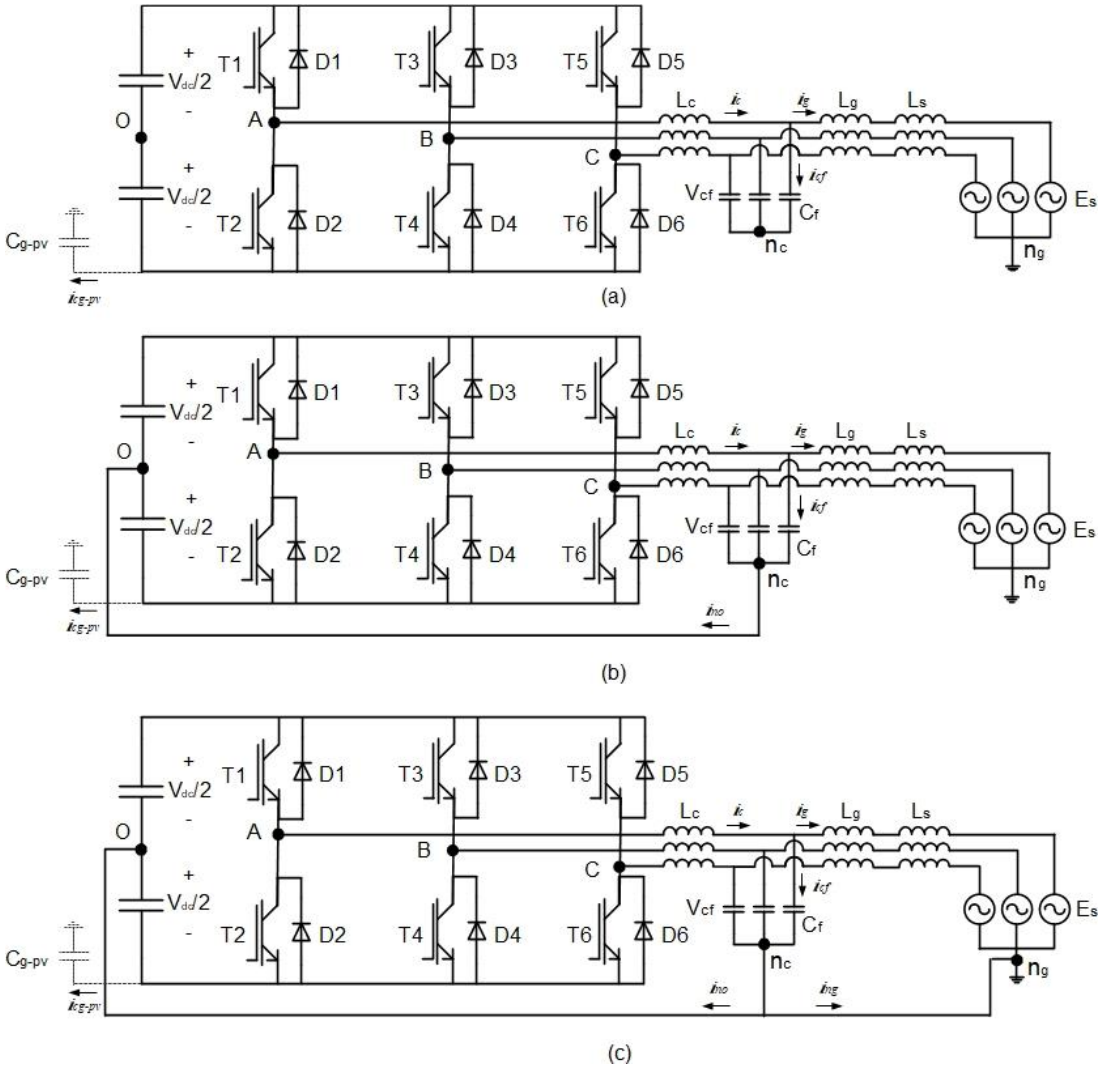


Figure 3.1 Two-level converter topologies.
(a) Floating topology, DC bus voltage is not split. (b) Semi-floating topology, midpoint of DC bus and star point of filter capacitors are connected. (c) Solidly-connected topology, midpoint of DC bus, star point of filter capacitors, and grid neutral are connected.

3.2.2. Modulation Methods

Sinusoidal PWM (SPWM) is the easiest modulation method and it can be applied to all three topologies in **Figure 3.1**. In this modulation method, three converter legs are switched according to the PWM signals which are generated by three sinusoidal modulation waves that are 120 º lagging each other. Basically, modulation waves are compared with triangular carrier, which determines the switching frequency, to generate PWM signal. However, DC bus voltage must be as high as twice of the peak phase voltage value in SPWM modulation. It means theoretical limit for minimum DC bus voltage is 653.2 V with SPWM modulation for a typical 400 V AC grid application. Generally, DC bus voltage is kept above 680 V in this modulation method.

Minimum DC link voltage requirement of SPWM method can be enhanced if no conducting path exists between the neutral point of the grid and converter. In this case, any zero-sequence signal can be injected into the SPWM modulation waveforms and the potential difference between midpoint of DC link voltage and neutral of grid can be easily varied. As zero-sequence components at the output of the converter cancel each other, they are not injected to the grid. As seen in **Figure 3.2**, the reference SPWM modulation waves V_a*, V_b* and V_c* can be used to compute a zero-sequence signal V_o and the modified reference signals V_a**, V_b** and V_c** are obtained adding V_o to reference SPWM modulation waves.

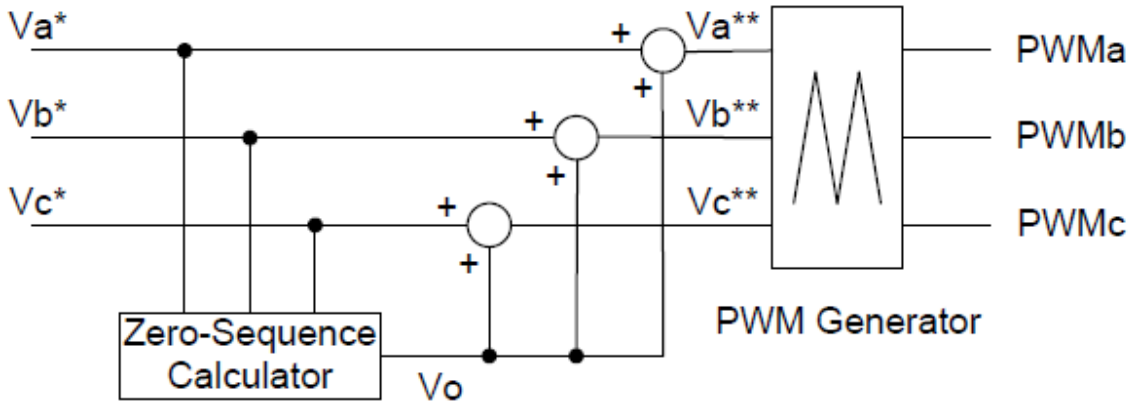


Figure 3.2 Generation of zero-sequence injected modulation waves.

SVPWM is the most common modulation method which is generated from SPWM by zero-sequence signal injection. The main advantage of SVPWM is that it is quite easy to implement it in digital environment. The computation of required zero-sequence signal V_o for SVPWM is given in [19]. According to [19], the magnitudes of three reference modulation waves (V_a*, V_b* and V_c*) are compared, smallest one is selected, and it is scaled with 0.5 to compute V_o.

Thanks to the extended volt-second linearity range provided by SVPWM, DC bus utilization can be increased up to 15.4% compared to SPWM method. That is why SVPWM is the most common PWM method if three-wire grid connection is allowed. However, four-wire AC connection is required at some application sites and SVPWM cannot be used in these applications. Thus, SVPWM can only be used with floating and semi-floating topologies.

Figure 3.3 shows the hexagonal diagram of switching states of the VSC for SVPWM operation. Average variation of space vector (denoted as V_{ref}) moves in a circular trajectory in counter-clockwise direction and average variation of line to line voltage at converter output is sinusoidal. V_{ref} can be expressed with the equations (3.1) and (3.2). Note that S_a, S_b and S_c represent the switching states in each leg, and they can be either 1 or 0 according to the state of the switches. According to this hexagonal diagram, peak voltage that can be achieved at one phase (let us say phase A) with SVPWM operation can be calculated with the equation (3.3). As clearly seen, peak voltage that can be achieved in one phase is 0.577 V_{DC} in SVPWM operation while it is only 0.5 V_{DC} in SPWM. It means a 15.4% extension in volt-second linearity.

$$V_{ref} = \frac{2}{3} V_{DC} (S_a + aS_b + a^2 S_c) \tag{3.1}$$

$$a = 1\angle 120° \tag{3.2}$$

$$V_{A-peak} = \frac{2}{3} V_{DC}\ x\ cos(30°) = \frac{2}{3} V_{DC}\ x\ \frac{\sqrt{3}}{2} = 0.577 V_{dc} \tag{3.3}$$

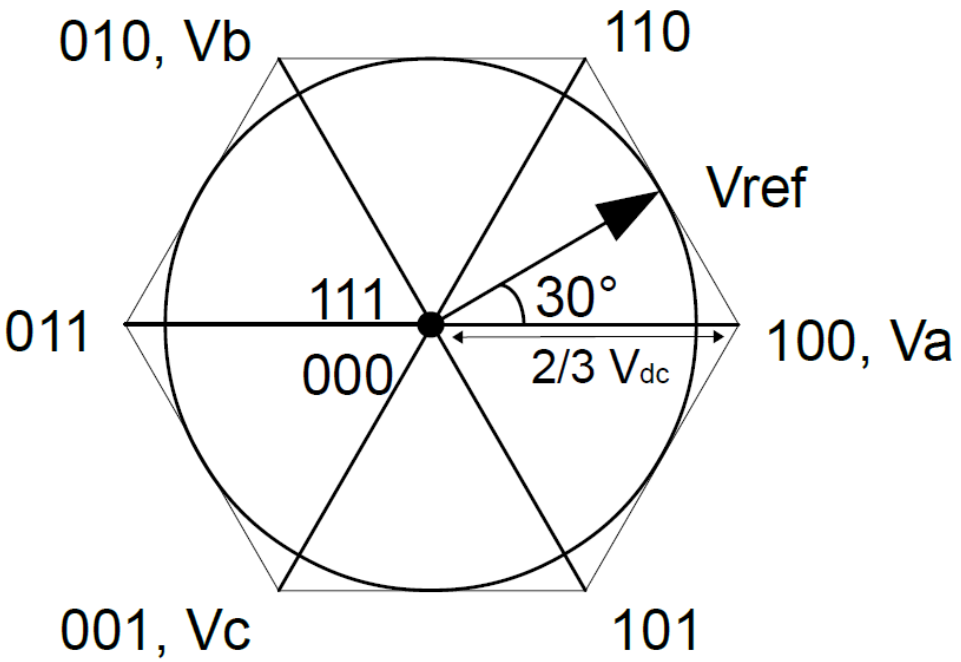


Figure 3.3 Hexagonal diagram of switching states for SVPWM operation.

3.2.3. Simulation Results

The difference between the current paths among topologies in **Figure 3.1** is shown through simulations for both SPWM and SVPWM modulation methods in **Figure 3.4** – **Figure 3.8**. As SVPWM modulation cannot be applied to solidly-connected topology, it is not included in the simulations. In the first set of simulations, parasitic capacitance ($C_{g\text{-}pv}$) is neglected, and DC bus voltage is accepted as a constant voltage source for convenience. Moreover, source inductance is assumed to be included in grid side inductance. Simulation system parameters are provided in **Table 3.1**.

Converter current (i_c), capacitor current (i_{cf}) and capacitor voltage (V_{cf}) waveforms are obtained at steady-state for one fundamental cycle (20 ms) for each case. In addition, phase voltage (V_{AO}) and line to line voltage (V_{AB}) data are recorded too. The converter circulated common mode current between LCL filter star point and DC bus midpoint (i_{no}) is obtained for semi-floating and solidly-connected topologies. Moreover, the current between LCL filter star point and grid neutral (i_{ng}) is also obtained for solidly-connected topology. Finally, harmonic spectrums of i_c, V_{cf}, V_{AO}, V_{AB}, and i_{no} are shown.

In this way, paths of current components, especially common mode current components, are better understood.

As clearly seen in **Figure 3.4**, converter current ripple is larger in semi-floating and solidly-connected topologies compared to floating topology. This is also seen in the harmonic spectrums of converter currents. Harmonic component at carrier frequency (16 kHz) is significantly larger in semi-floating and solidly-connected topologies. The reason of this situation can be better understood when **Figure 3.5** is investigated. Harmonic spectrums of phase voltages and line to line voltages are given for these three topologies in **Figure 3.5** for SPWM operation. As clearly seen, the voltage components produced by the VSC are actually same for all topologies. However, when midpoint of DC bus (point O) and LCL filter star point (point n_c) are connected, a conducting path is created for the common mode current components and they can circulate in the VSC through this conducting path (O-n_c path in **Figure 3.1**).

Figure 3.6 further focuses on the properties of common mode current component that circulates in the VSC in solidly-connected topology. Harmonic spectrums of $V_{AO,}$ i_c and i_{no} are focused around carrier frequency region. As clearly seen, V_{AO} and i_c have some sideband harmonic components around carrier frequency. However, i_{no} has only carrier frequency component. Only common mode components at carrier frequency and its multiples flow through the conducting path between DC midpoint and LCL filter when this path is provided in semi-floating and solidly-connected topologies.

Table 3.1 Simulation system parameters

DC Bus Voltage (V_{DC})	750 V DC
Grid Voltage (line to line)	400 V AC
Grid Frequency (f_g)	50 Hz
Switching Frequency (f_{sw})	16 kHz
Converter Side Inductance (L_c)	800 µH
Grid Side Inductance (L_g)	400 µH
Filter Capacitance (C_f)	25 µF
Corner Frequency (L_c - C_f)	1125.4 Hz
LCL Parallel Corner Frequency	1949.2 Hz
Parasitic Capacitance ($C_{g\text{-}pv}$)	3 µF

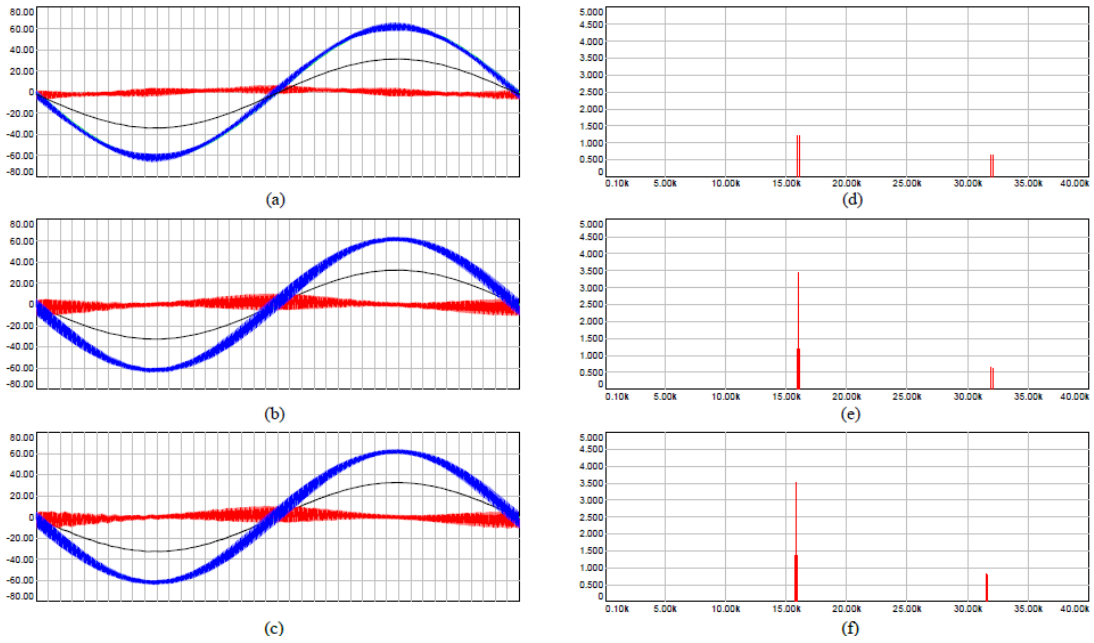


Figure 3.4 SPWM simulation results for i_c (blue), V_{cf} (black, scaled by 0.1) and i_{cf} (red) waveforms and i_c harmonic spectrums for all topologies.
(a) Floating topology waveforms. (b) Semi-floating topology waveforms. (c) Solidly-connected topology waveforms. (d) i_c spectrum in floating topology. (e) i_c spectrum in semi-floating topology. (f) i_c spectrum in solidly-connected topology.

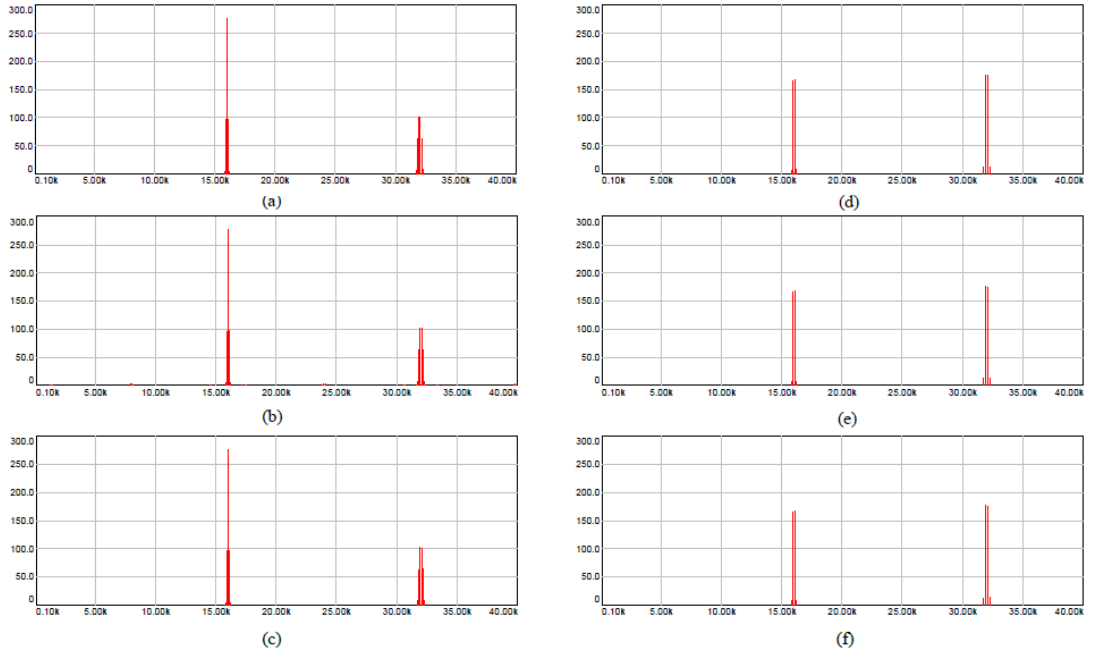


Figure 3.5 SPWM V_{AO} and V_{AB} harmonic spectrums for all topologies.
(a) V_{AO} spectrum in floating topology. (b) V_{AO} spectrum in semi-floating topology. (c) V_{AO} spectrum in solidly-connected topology. (d) V_{AB} spectrum in floating topology. (e) V_{AB} spectrum in semi-floating topology. (f) V_{AB} spectrum in solidly-connected topology.

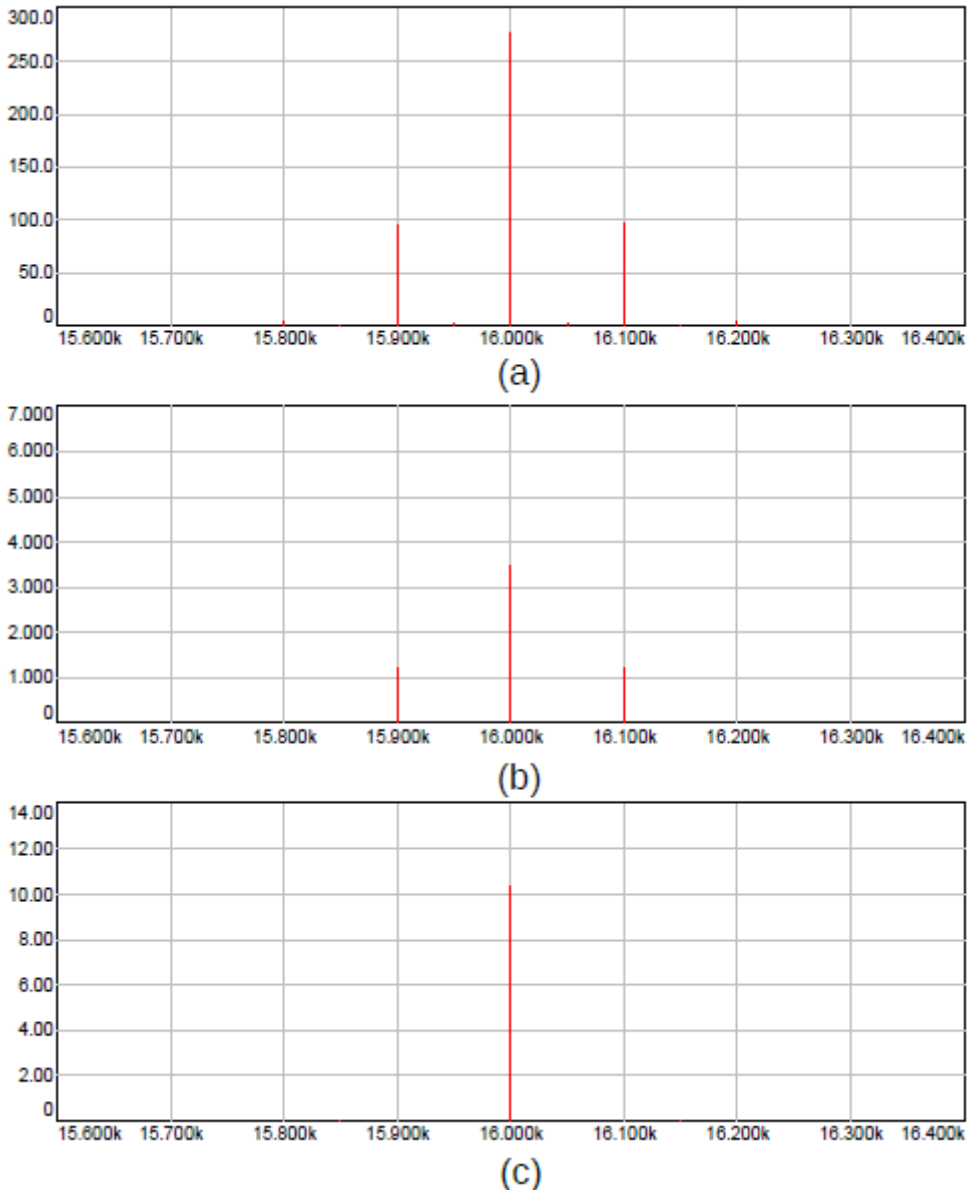


Figure 3.6 SPWM operation harmonic components for solidly-connected around carrier frequency. (a) V_{AO}. (b) i_c. (c) i_{no}.

Simulation results are obtained for SVPWM modulation too. As mentioned, solidly-connected topology cannot be used with SVPWM because injected zero-sequence components directly flow to the grid via solid connection between grid neutral and DC bus midpoint. Thus, simulation results are obtained for only floating and semi-floating topologies. **Figure 3.7** shows the i_c, V_{cf}, and i_{cf} waveforms for floating and

semi-floating topologies with SVPWM. While the difference between SPWM and SVPWM is not significant in floating topology, injected zero-sequence components significantly affect the capacitor voltage in semi-floating topology. In addition, low frequency oscillations are clearly seen in converter current in **Figure 3.7 (b)** in this topology and these low frequency components are also noticed in the harmonic spectrum of converter current in **Figure 3.7 (d)**. In order to focus on the effects of injected zero-sequence components, harmonic spectrums of capacitor voltages are compared for semi-floating topology for both SPWM and SVPWM in **Figure 3.8**.

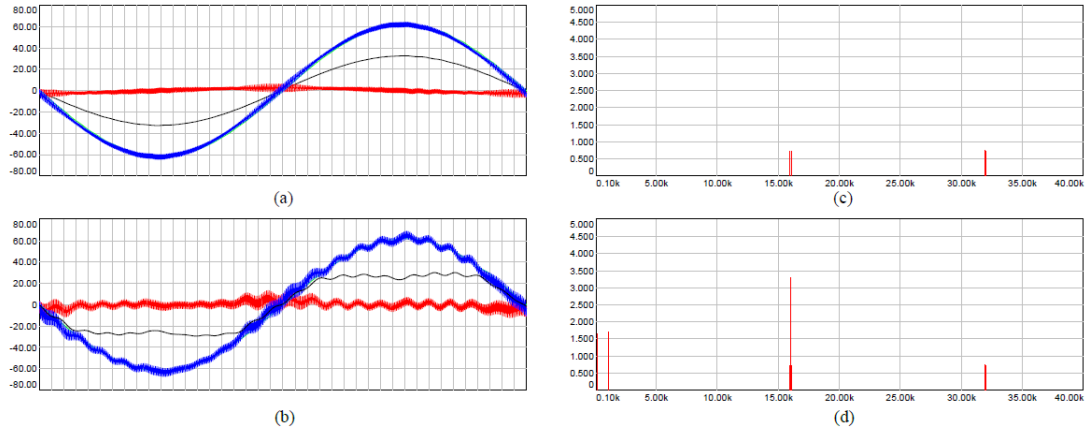


Figure 3.7 SVPWM simulation results for i_c (blue), V_{cf} (black, scaled by 0.1) and i_{cf} (red) waveforms and i_c spectrums for floating and semi-floating topologies.
(a) Floating topology waveforms. (b) Semi-floating topology waveforms. (c) i_c spectrum in floating topology. (d) i_c spectrum in semi-floating topology.

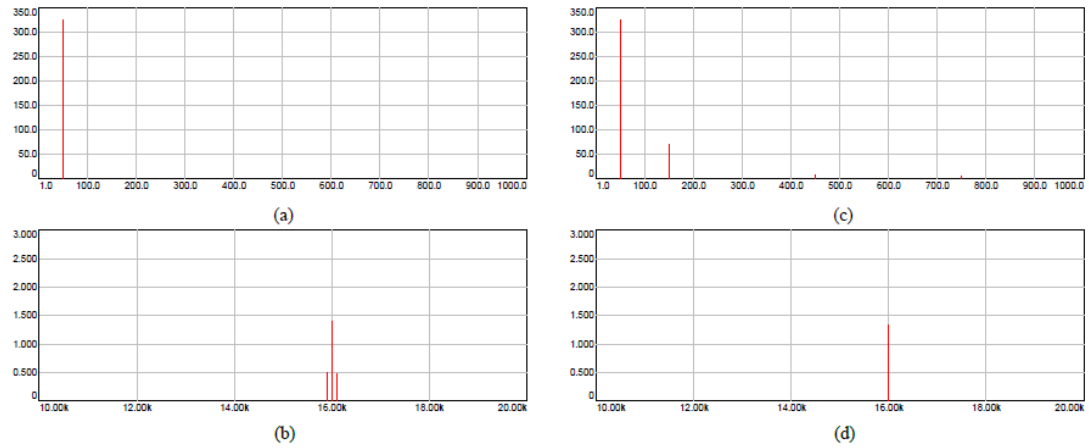


Figure 3.8 SPWM and SVPWM V_{cf} spectrums for semi-floating topology.
(a) SPWM, low frequency components. (b) SPWM, high frequency components.
(c) SVPWM, low frequency components. (d) SVPWM, high frequency components.

As seen in **Figure 3.8 (c)**, injected zero sequence components create harmonic components at capacitor voltage in low frequency region (up to 1 kHz). This is expected as the fundamental frequency of injected zero-sequence components is 150 Hz. Thus, low frequency harmonic components appear in capacitor voltage spectrum at triplen harmonics (150 Hz, 450 Hz, 750 Hz) as expected. Moreover, these harmonic components may also excite the LCL resonance frequency if LCL filter resonance frequency is close to this low frequency region.

Another set of simulations are conducted to show the effect of parasitic capacitance. As mentioned, parasitic capacitance from PV modules to the ground ($C_{g\text{-}pv}$) is accepted as 200 nF/kW. In a 30-kW PV converter application, parasitic capacitances from positive and negative DC bus to the ground are assumed as 6 μF. As they can be assumed as series connected at high frequency (around carrier frequency), only a parasitic capacitance of 3 μF from negative DC bus to the ground is modelled. In fact, much smaller parasitic capacitances also exist from semiconductors to the heatsink or chassis of the product and they cause needle-like leakage currents at switching instants due to high dV/dt rate. However, effects of these capacitances are kept beyond the scope of this study and only the ground leakage current ($i_{cg\text{-}pv}$) due to $C_{g\text{-}pv}$ is analyzed.

Common-mode equivalent circuits of all topologies are given in **Figure 3.9**. As clearly seen, all the common-mode current components created by VSC are expected to flow through $C_{g\text{-}pv}$ in floating topology. On the other hand, in semi-floating topology, another current path is provided for common-mode current components. Most of the common-mode current components flow through filter capacitances and the rest flows through $C_{g\text{-}pv}$. In solidly-connected topology, $C_{g\text{-}pv}$ is already short-circuited and no current is expected to flow through it. Total generated common-mode current (i_{cm}) by VSC and ground leakage current ($i_{cg\text{-}pv}$) which flows through $C_{g\text{-}pv}$ can be expressed with transfer functions given in equations (3.4) – (3.5) for floating topology, equations (3.6) – (3.8) for semi-floating topology, and (3.9) – (3.12) for solidly-connected topology.

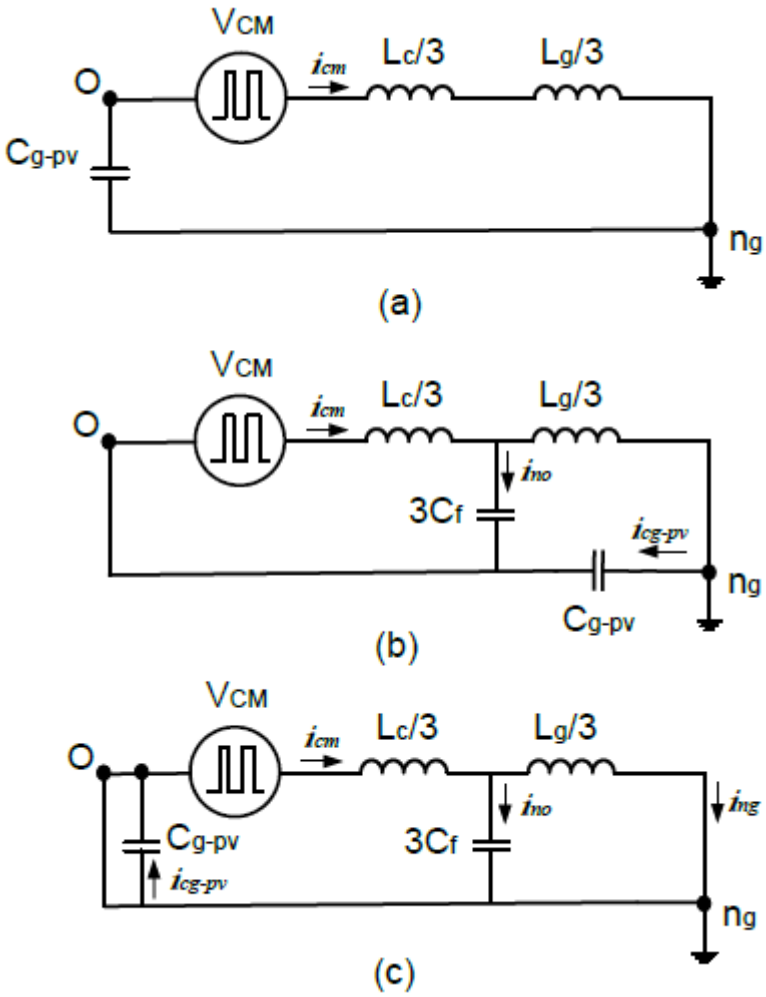


Figure 3.9 Common-mode equivalent circuits for all topologies. (a) Floating topology. (b) Semi-floating topology. (c) Solidly-connected topology.

$$\frac{i_{cm-A}(s)}{V_{cm-A}(s)} = \frac{3sC_{g-pv}}{s^2C_{g-pv}(L_c+L_g)+3} \tag{3.4}$$

$$i_{cg-pv-A}(s) = i_{cm-A}(s) \tag{3.5}$$

$$\frac{i_{cm-B}(s)}{V_{cm-B}(s)} = \frac{s^3C_fL_gC_{g-pv}+s(3C_{g-pv}+9C_f)}{s^4L_cC_{g-pv}L_gC_f+s^2(L_gC_g+L_cC_g+3L_cC_f)} \tag{3.6}$$

$$i_{cg-pv-B}(s) = i_{cm-B}(s)\ x\ \frac{C_{g-pv}}{s^2C_fL_gC_g+3C_f+C_g} \tag{3.7}$$

$$i_{no-B}(s) = i_{cm-B}(s)\ x\ \frac{s^2C_fL_gC_{g-pv}+3C_f}{s^2C_fL_gC_g+3C_f+C_g} \tag{3.8}$$

$$\frac{i_{cm-C}(s)}{V_{cm-C}(s)} = \frac{s^2 3C_f L_g + 3}{s^3 L_g C_f L_c + s(L_c + L_g)} \quad (3.9)$$

$$i_{cg-pv-C}(s) = 0 \quad (3.10)$$

$$i_{ng-C}(s) = i_{cm-C}(s)\ x\ \frac{1}{s^2 C_f L_g + 1} \quad (3.11)$$

$$i_{no-C}(s) = i_{cm-C}(s)\ x\ \frac{s^2 C_f L_g}{s^2 C_f L_g + 1} \quad (3.12)$$

By keeping the other parameters same as provided in **Table 3.1**, simulations are repeated for all topologies taking the $C_{g\text{-}pv}$ into the account. In addition, equivalent series resistance of filter capacitors (50 mΩ) and series resistance of converter side inductors (20 mΩ) are also included in the simulation model. However, they are not included in transfer function calculations as they increase the equation complexity a lot. Moreover, as resistors are not frequency dependent components, they are not expected to affect the frequency behavior, but they only affect the magnitude of the admittance bode plots.

Figure 3.10 provides the waveforms of the ground leakage currents ($i_{cg\text{-}pv}$) and converter circulated common mode currents (i_{no}) in all topologies for 1 ms period. As i_{no} does not exist in floating topology, its waveform is labelled as not applicable. In addition to the waveforms, the rms magnitudes of the $i_{cg\text{-}pv}$ and i_{no} are also given in **Table 3.2**. In floating topology, $i_{cg\text{-}pv}$ is observed as 5.429 A. In fact, in floating topology, $i_{cg\text{-}pv}$ corresponds to i_{ng} as the common-mode equivalent circuit is completed with this parasitic capacitance between ground and the PV converter. In semi-floating topology, $i_{cg\text{-}pv}$ significantly reduces, and it is observed as 106 mA (similar to floating topology, $i_{cg\text{-}pv}$ can be again considered as i_{ng}). However, i_{no} is observed as 7.577 A in this topology. It means that common-mode components circulate inside the VSC (through $3C_f$ in **Figure 3.9 (b)**) instead of flowing to the ground through $C_{g\text{-}pv}$. Filter capacitor current increases in this situation but still it is a common practice to allow this current circulate in the VSC instead of letting it flow to the ground.

Figure 3.11 (a) provides the common-mode voltage (V_{cm}) and $i_{cg\text{-}pv}$ waveforms for floating topology. **Figure 3.11 (b)** provides the harmonic spectrum of V_{cm}, **Figure 3.11 (c)** provides the harmonic spectrum of $i_{cg\text{-}pv}$, and **Figure 3.11 (d)** provides the admittance bode plot of transfer function $i_{cg\text{-}pv}/V_{cm}$. As clearly seen, most of the $i_{cg\text{-}pv}$ components are at 16 kHz switching frequency. However, as also shown in **Figure 3.11 (c)**, admittance transfer function has a peak point at 4.6 kHz region and some of ground leakage current ($i_{cg\text{-}pv}$) components are also observed around this frequency region as seen in **Figure 3.11 (d)**. In fact, due to parasitic resistances in the circuit, peak point of admittance transfer function is expected to be at a much lower value. Anyway, still it is obvious that circuit has its lowest impedance value at this frequency. Although VSC is not expected to generate any voltage component below carrier frequency, practical conditions such as device nonlinearities, dead time and etc., may cause some voltage components which can excite this frequency. In this case, $i_{cg\text{-}pv}$ current may also have significant amount of harmonic components at this frequency.

Figure 3.12 (a) shows V_{cm}, $i_{cg\text{-}pv}$, and i_{no} waveforms for semi-floating topology. **Figure 3.12 (b)** shows harmonic spectrum of V_{cm}, **Figure 3.12 (c)** shows harmonic spectrum of $i_{cg\text{-}pv}$, **Figure 3.12 (d)** shows harmonic spectrum of i_{no}, **Figure 3.12 (e)** provides the admittance bode plot of transfer function $i_{cg\text{-}pv}/V_{cm}$ and **Figure 3.12 (f)** provides the admittance bode plot of transfer function i_{no}/V_{cm}. Now it is observed that most of the common-mode current components at switching frequency circulate inside VSC. While the peak value of i_{no} at switching frequency is larger than 10 A, peak value of $i_{cg\text{-}pv}$ at carrier frequency is less than 150 mA. **Figure 3.12 (e)** shows that $i_{cg\text{-}pv}/V_{cm}$ admittance bode plot has peak points at 1.1 kHz and 8.12 kHz. As expected, we observe harmonic components at these frequencies in $i_{cg\text{-}pv}$ harmonic spectrum in **Figure 3.12 (c)**. Again, it shall be noted that admittance bode plot peak points are observed as higher than practical conditions because of neglecting the parasitic resistance in derivation of admittance transfer functions.

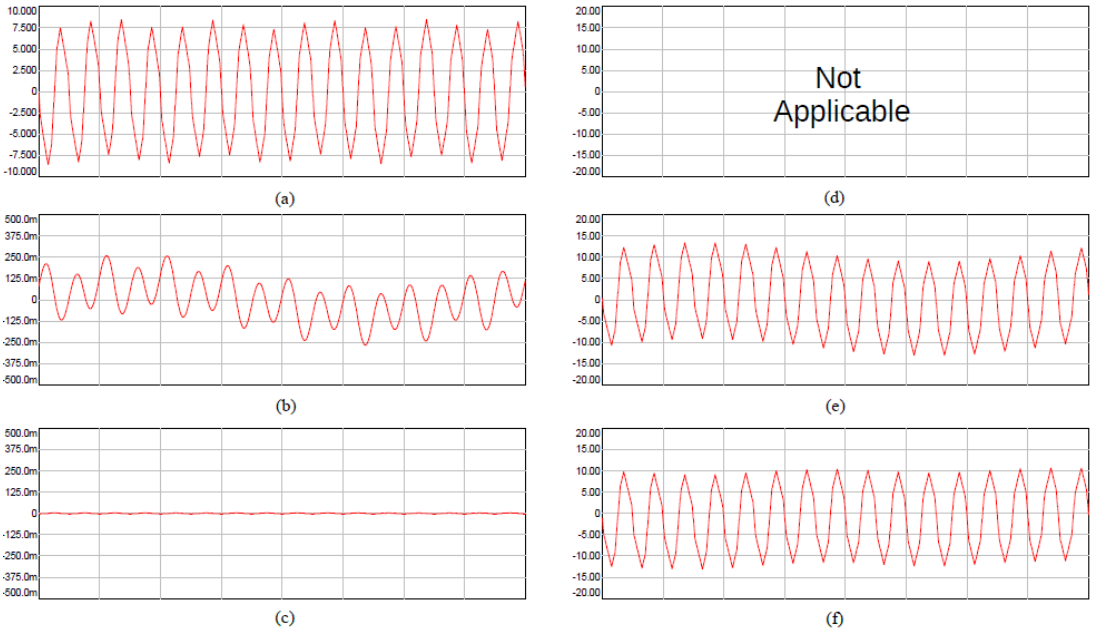


Figure 3.10 $i_{cg\text{-}pv}$ and i_{no} waveforms with SPWM modulation in all topologies.
(a) $i_{cg\text{-}pv}$ waveform in floating topology. (b) $i_{cg\text{-}pv}$ waveform in semi-floating topology. (c) $i_{cg\text{-}pv}$ waveform in solidly-connected topology. (d) i_{no} waveform in floating topology. (e) i_{no} waveform in semi-floating topology. (f) i_{no} waveform in solidly-connected topology.

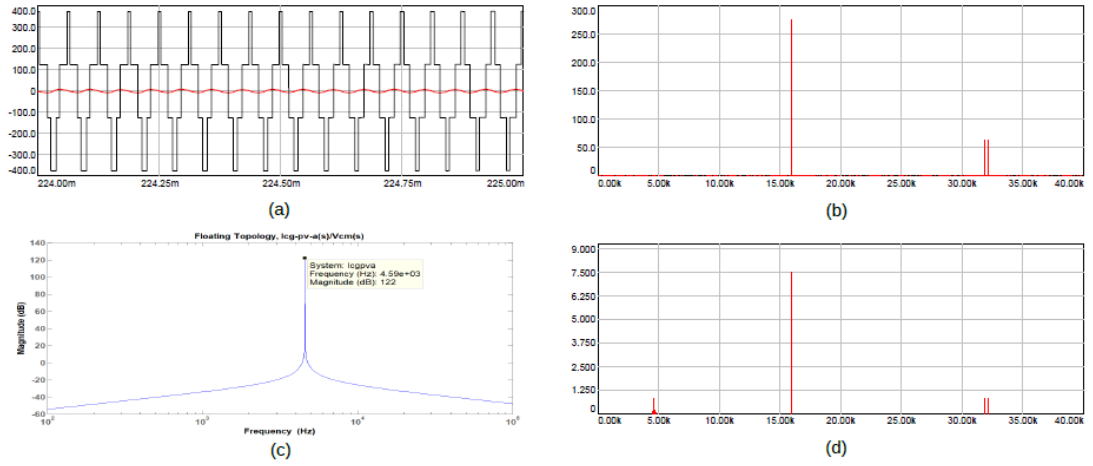


Figure 3.11 (a) V_{cm} (black) and $i_{cg\text{-}pv}$ (red) waveforms. (b) V_{cm} harmonic spectrum. (c) $i_{cg\text{-}pv}/V_{cm}$ bode plot. (d) $i_{cg\text{-}pv}$ harmonic spectrum for floating topology with SPWM modulation.

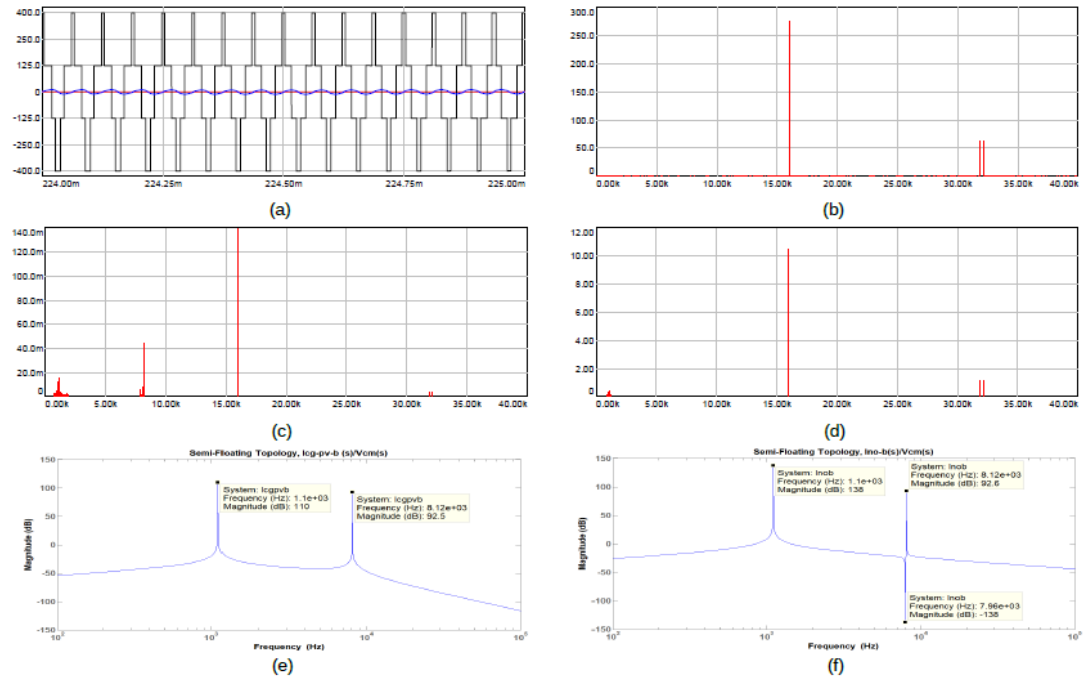


Figure 3.12 (a) V_{cm} (black), $i_{cg\text{-}pv}$ (red), and i_{no} (blue) waveforms. (b) V_{cm} harmonic spectrum. (c) $i_{cg\text{-}pv}$ harmonic spectrum. (d) i_{no} harmonic spectrum. (e) $i_{cg\text{-}pv}/V_{cm}$ bode plot. (f) i_{no}/V_{cm} bode plot for semi-floating topology with SPWM modulation.

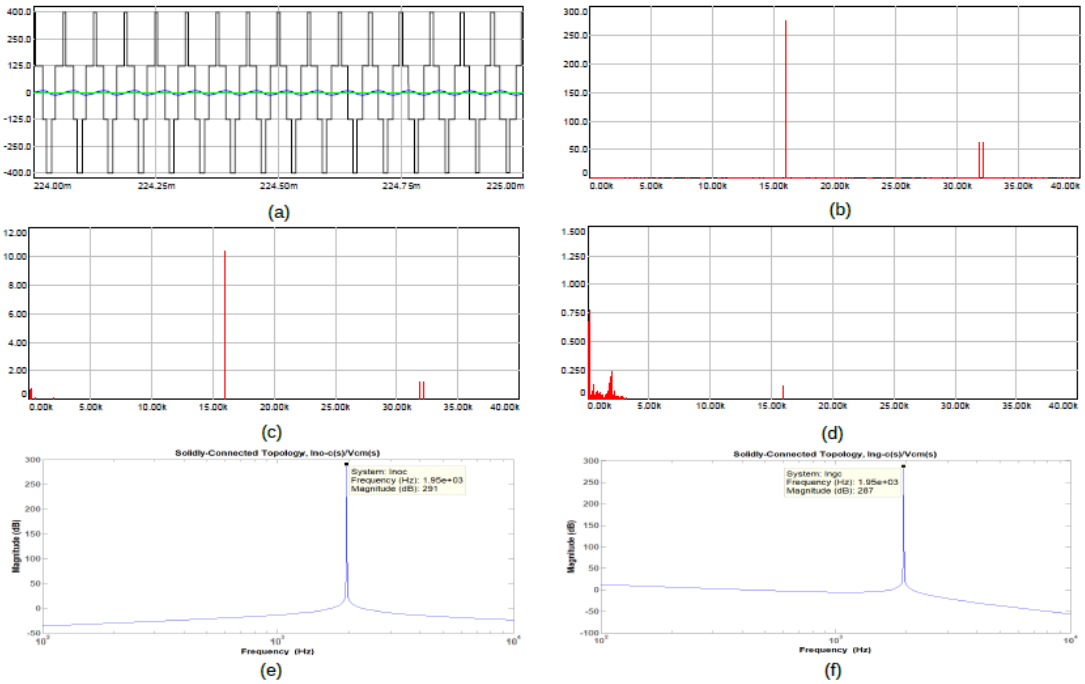


Figure 3.13 (a) V_{cm} (black), i_{no} (blue), and i_{ng} (green) waveforms. (b) V_{cm} harmonic spectrum. (c) i_{no} harmonic spectrum. (d) i_{ng} harmonic spectrum. (e) i_{no}/V_{cm} bode plot. (f) i_{ng}/V_{cm} bode plot for solidly-connected topology with SPWM modulation.

Figure 3.13 (a) shows V_{cm}, i_{no}, and i_{ng} waveforms for solidly-connected topology. As the $i_{cg\text{-}pv}$ is negligible in solidly-connected topology, its harmonic spectrum and bode plot are not given in **Figure 3.13**. **Figure 3.13 (b)** shows the harmonic spectrum of V_{cm}, **Figure 3.13 (c)** shows the harmonic spectrum of i_{no}, **Figure 3.13 (d)** shows the harmonic spectrum of i_{ng}, **Figure 3.13 (e)** provides the admittance bode plot of transfer function i_{no}/V_{cm}, and **Figure 3.13 (f)** provides the admittance bode plot of transfer function i_{ng}/V_{cm}. As clearly seen, while $i_{cg\text{-}pv}$ current is almost completely prevented, i_{no} current circulates inside the VSC. Similar to semi-floating topology, peak value of i_{no} current at carrier frequency is observed as larger than 10 A.

Table 3.2 shows that $i_{cg\text{-}pv}$ is observed as only 1 mA in solidly-connected topology whereas i_{no} and i_{ng} currents are observed as 7.564 A and 1.239 A respectively. While i_{no} circulates in the converter, i_{ng} flows to the grid but this current does not flow through parasitic capacitances unlike floating and semi-floating topologies. Thus, this current is measured just like other phase currents by residual current measurement system and can be interpreted like a phase current by residual current protection system. As the continuous residual current limit is set as 300 mA for a 30-kW PV converter in IEC 62109-2, only semi-floating and solidly-connected topologies satisfy the standard with SPWM according to the simulation results. Floating topology require common mode filter for the suppression of common mode components.

The ground leakage current problem can be worse if a boost converter is used at the input of the VSC. Boost converter can also contribute to the common-mode components which flow to the ground through parasitic capacitances. Thus, effects of parasitic capacitances can be worse in practice. Advantage of solidly-connected topology is better understood with this ground leakage current problem analysis.

Table 3.2 $i_{cg\text{-}pv}$, i_{no}, and i_{ng} currents in all topologies with SPWM

Topology	$i_{cg\text{-}pv}$	i_{no}	i_{ng}
Floating	5.429 A	Not Applicable	5.429 A ($i_{cg\text{-}pv}$)
Semi-Floating	0.106 A	7.577 A	0.106 A ($i_{cg\text{-}pv}$)
Solidly-Connected	0.001 A	7.564 A	1.239 A

Figure 3.14 shows the harmonic spectrums of $i_{cg\text{-}pv}$ and i_{no} in semi-floating topology with different LCL filter capacitance (C_f) values. As clearly seen, $i_{cg\text{-}pv}$ component at switching frequency significantly increases while C_f decreases. It is an expected result because the impedance on the i_{no} path increases as C_f decreases and more current components flow through $C_{g\text{-}pv}$. While $i_{cg\text{-}pv}$ is 106 mA originally (when C_f = 25 µF), it is observed as 263 mA when C_f is reduced to 10 µF. With this analysis, it is seen that only L_c limits the i_{no} current. Moreover, semi-floating topology may also require a common-mode filter to satisfy the IEC 62109-2 standard depending on its LCL filter capacitor. In this way, advantage of solidly-connected topology is better emphasized.

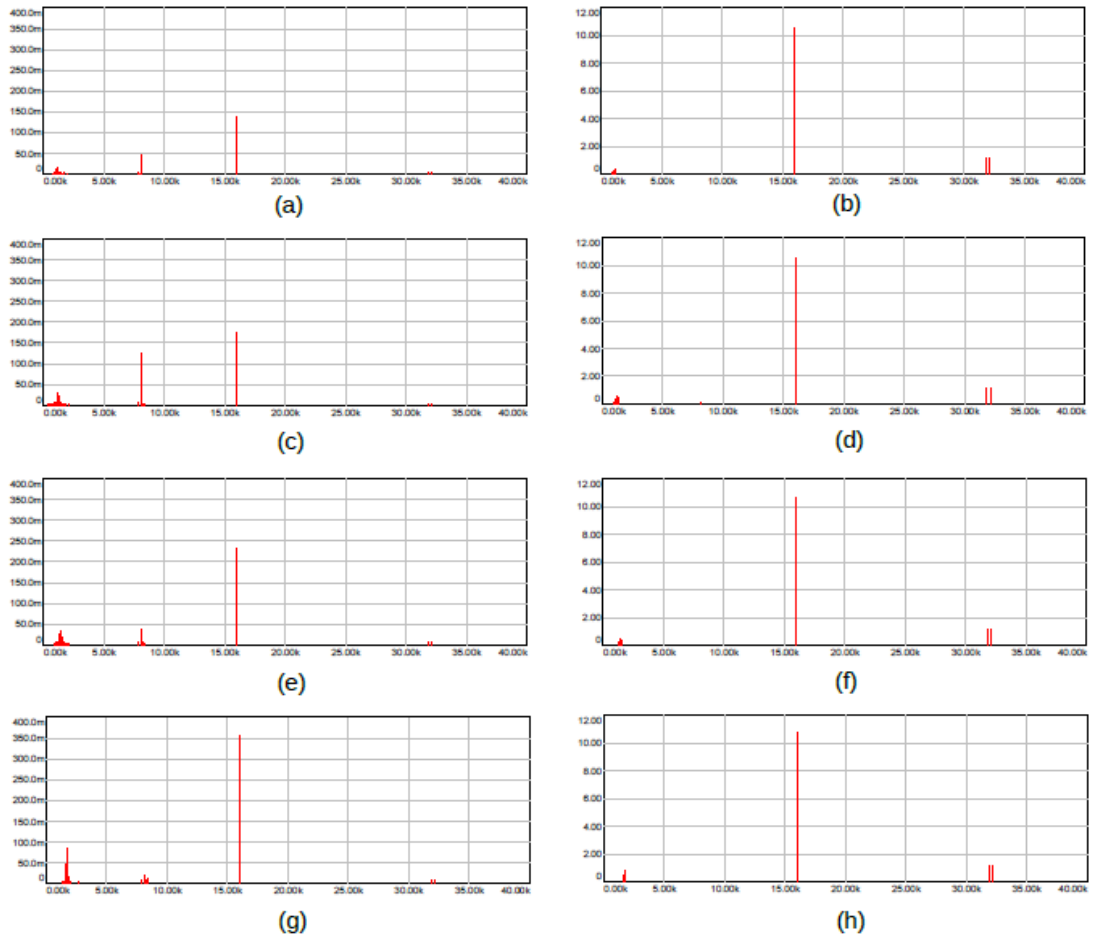


Figure 3.14 $i_{cg\text{-}pv}$ and i_{no} harmonic spectrums for semi-floating topology with different LCL filter capacitance values.
(a) $i_{cg\text{-}pv}$ spectrum for C_f = 25 µF. (b) i_{no} spectrum for C_f = 25 µF.
(c) $i_{cg\text{-}pv}$ spectrum for C_f = 20 µF. (d) i_{no} spectrum for C_f = 20 µF.
(e) $i_{cg\text{-}pv}$ spectrum for C_f = 15 µF. (f) i_{no} spectrum for C_f = 15 µF.
(g) $i_{cg\text{-}pv}$ spectrum for C_f = 10 µF. (h) i_{no} spectrum for C_f = 10 µF.

Table 3.3 provides a comparison between all topologies in terms of ground leakage current, minimum DC bus voltage requirement, LCL filter sizing and losses. Floating topology shows superior performance in terms of converter current ripple so that smaller converter side inductor (L_c) can be used with this topology. In addition, SVPWM modulation can be applied to this topology to reduce DC bus voltage. However, in PV applications, existence of significantly large parasitic capacitance from PV modules to the ground creates leakage current problem due to common-mode components. Thus, floating topology is not feasible in PV applications.

On the other hand, solidly-connected topology is basically a half-bridge structure. As mentioned earlier, SVPWM modulation method cannot be implemented in this topology, and volt-second linearity cannot be extended. Theoretical limit for DC bus voltage is 653.2 V DC for 400 V AC grid applications. However, this topology is superior in terms of suppression of common-mode components which is a very important feature in PV applications [29]. Therefore, this topology is commonly used in PV applications and it is also focus of the dissertation. As there is no other option, SPWM is used with this topology.

Table 3.3 Comparison of two-level VSC topologies with LCL filter for 400 V AC grid applications

Topology	Floating	Semi-Floating	Solidly-Connected
Theoretical Limit for Minimum DC Bus Voltage	565.7 V	565.7 V	653.2 V
Converter Current Ripple at Carrier Frequency	Low	High	High
Converter Side Inductance Loss	Low	High	High
Ground Leakage Current due to Common Mode Components	High	Low	Almost Zero
Common Mode Filter Requirement	High	Low	Lowest

3.3. Semiconductor Technology

Before the invention of MOSFETs and IGBTs, thyristors were commonly used in three-phase grid-connected VSCs and switching frequency could not be increased more than a few kHz. As a result, attenuation of switching components was achieved

with bulky filters. Then, MOSFETs appeared in the market as majority carrier devices with their superior switching characteristics. But the voltage blocking capability of MOSFETs was limited and they were not suitable for three-phase grid-connected VSC applications. In addition, their high on-state losses were not suitable for high power applications. That is why MOSFETs could not be used in three-phase grid-connected VSC designs in 400 V AC grid systems. Eventually, IGBTs appeared in the market in early 1990s combining the switching performance of MOSFETs and on-state performance of minority carrier devices. IGBTs can block high voltages at kV level and they show superior on-state performance compared to MOSFETs in high power applications. In this way, 1200 V IGBTs are commonly used in two-level VSC topologies and they dominated the grid-connected VSC applications. **Figure 3.15** shows the development process of the power semiconductor technology.

In the last decade, wide bandgap semiconductors emerged in the market for different applications. **Figure 3.16** shows a study of Keysight Technologies on classification of expected applications with GaN and SiC devices [13]. According to this map, GaN transistors are expected to take part in communication equipment, switch mode power supplies and automotive electronics. On the other hand, SiC-MOSFETs are expected to be dominant in high voltage applications such as electric vehicles, renewable energy systems, and traction applications. In addition, SiC Schottky diodes have also found a significant place in these applications. Future trend shows that SiC-MOSFETs and SiC Schottky diodes are expected to replace conventional Si based IGBTs and diodes with their superior switching and conduction characteristics.

The main advantage of SiC Schottky diodes is the absence of stored minority charge carriers which causes reverse recovery losses. Removal of these stored charge carriers causes reverse recovery current and contributes to the switching losses of the transistors. Moreover, reverse recovery current may also cause a voltage spike at switching moments unless necessary precautions are taken. Thus, replacement of Si diodes with SiC Schottky diodes brings a great advantage in switching performance of the power modules.

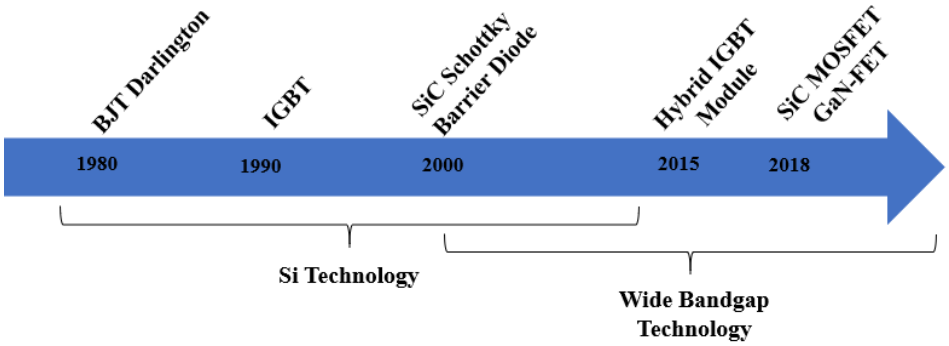


Figure 3.15 Development history of power semiconductors in grid-connected applications.

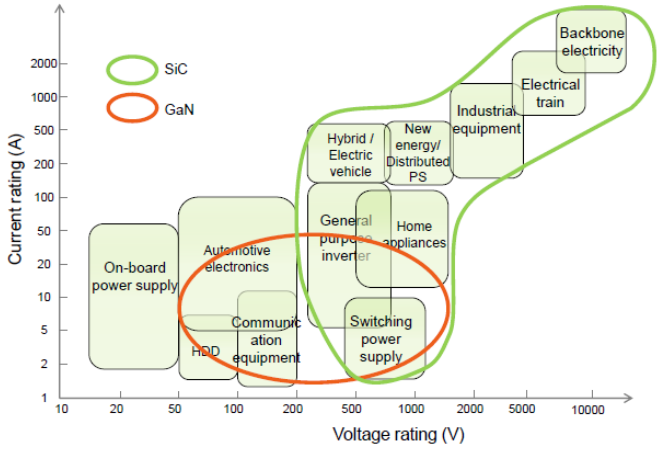


Figure 3.16 Classification of GaN and SiC devices according to applications [13].

Similarly, SiC-MOSFETs do not have minority charge carriers in their structure either. Thus, they have superior switching characteristics compared to Si based IGBTs. In addition, thanks to high dielectric strength of SiC material, a thinner semiconductor layer is used in SiC-MOSFET and SiC Schottky barrier diode structures for the same voltage blocking capability compared to their Si based counterparts. In this way, smaller on-state resistance is achieved resulting in a better conduction performance. Thus, 1200 V SiC-MOSFETs and SiC Schottky barrier diodes can be manufactured with satisfactory on-state performance.

Increasing efficiency concerns and the thirst for reducing filter size and cost in VSC designs has resulted in the H-IGBT and SiC-MOSFET modules to replace the classical 1200V Si-IGBT modules in low voltage grid applications (specifically 400 V AC grid

applications). While the hybrid technology, which replaces the Si diode with SiC diode, allows the IGBT turn-on (diode turn-off) to be fast, the SiC-MOSFET module further expands the switching frequency of the converter. In either case, efficiency increases, and LCL filter size can be reduced for size and cost reduction.

A basic comparison is provided about semiconductor loss parameters for Si-IGBT, H-IGBT, and SiC-MOSFET modules for both transistor and diode components in **Table 3.4**. SiC-MOSFET module ampere rating is selected as smaller than Si-IGBT and H-IGBT modules to conduct a fairer comparison as it has superior conduction and switching characteristics. Thus, 75-A SiC-MOSFET module is selected to compare with 150-A Si-IGBT and H-IGBT modules. Note that suggested gate resistance values in the device datasheets are used to obtain the switching loss data of the modules. In practice, gate resistance can be slightly increased to slow down the switching of the device in case of possible EMI problems due to limited layout quality.

As clearly seen in **Table 3.4**, H-IGBT module has superior switching performance compared to conventional Si-IGBT module. Replacement of conventional Si PN junction diode with SiC Schottky barrier diode removes the reverse recovery losses. In fact, removal of stored charge in the junction capacitance of SiC Schottky barrier diode still causes a finite amount of loss but it can be assumed as negligible, so it is assumed that switching action of SiC Schottky barrier diodes are simply lossless.

SiC-MOSFET module has even better switching performance than H-IGBT module because it reduces the switching losses of the transistor too in addition to the diode. This is expected due to the majority carrier device structure of the SiC-MOSFET. In this way, superior switching performance of SiC-MOSFET makes it a much better option in terms of semiconductor losses. While Si-IGBT module has approximately 48 mJ energy loss in one PWM cycle at 150 A current, 600 V blocking voltage and 150 °C junction temperature conditions, this value is only 2.44 mJ for SiC-MOSFET module. It means that SiC-MOSFET module is approximately 20 times better than Si-IGBT module in terms of switching losses.

Table 3.4 Si-IGBT, H-IGBT and SiC-MOSFET modules semiconductor loss parameters

		Si-IGBT Module	**H-IGBT Module**	**SiC-MOSFET Module**
Voltage Rating (V)		1200	1200	1200
Current Rating (A)		150	150	75
Conduction Losses (T_j = 150 °C)				
IGBT/ MOSFET	V_{ceo}	0.7 V	0.7 V	NA
	r_{ce} / $r_{ds\text{-}on}$	10 mΩ	12 mΩ	38 mΩ
DIODE	V_{fo}	0.9 V	0.8 V	0.8 V
	r_f	7.8 mΩ	13 mΩ	20 mΩ
Switching Losses (V_{CC}=600 V, T_j = 150 °C, I_C=150 A)				
IGBT/MOSFET	E_{ON}	19.2 mJ	9.6 mJ	0.82 mJ
	E_{OFF}	15.8 mJ	9.4 mJ	1.62 mJ
DIODE	E_{RR}	13 mJ	NA	NA

In order to emphasize the advantage of H-IGBT and SiC-MOSFET modules over conventional Si-IGBT module, transistor and diode switching characteristics are specifically provided for our particular 400 V AC grid connected 30-kW VSC case. As phase current is 43.3 A in this case, it is reasonable to focus on 0 – 60 A range for switching energies of the devices. Blocking voltage is accepted as 600 V and fixed heatsink temperature is adjusted in such a way that junction temperature of the devices is 150 °C in all cases. Gate voltages are assumed as $\pm$15 V for all cases. Under these circumstances, transistor switching energies (E_{ON} and E_{OFF}) and diode switching energies (E_{RR}) are provided in **Figure 3.17** and in 0 – 60 A range.

Similarly, on-state characteristics of the modules can be plotted too in order to compare the conduction loss performance of the semiconductor power modules in the same current range. **Figure 3.18** shows the on-state voltage drop vs current plots of both transistors and diodes in Si-IGBT, H-IGBT and SiC-MOSFET power modules at 150 °C junction temperature. Again, gate voltages are assumed as +15 V while transistors are conducting.

As clearly seen, conduction characteristics of SiC-MOSFET is worse than its competitors when current exceeds 25 A. However, this is expected as SiC-MOSFET module ampere rating is almost half of its competitors in this example. In fact, conduction loss of the SiC-MOSFET module can be also better than Si-IGBT module if a SiC-MOSFET with a higher ampere rating is selected. However, this approach dramatically increases the cost and results in an oversized design. Thus, it is not preferred. SiC Schottky barrier diode of the SiC-MOSFET module also has worse on-state characteristics than its competitors in this example. Again, it is because of smaller ampere rating of the SiC-MOSFET power module. If SiC-MOSFET ampere rating was also selected as 150 A, then it would have better on-state characteristics due to higher ampere rating.

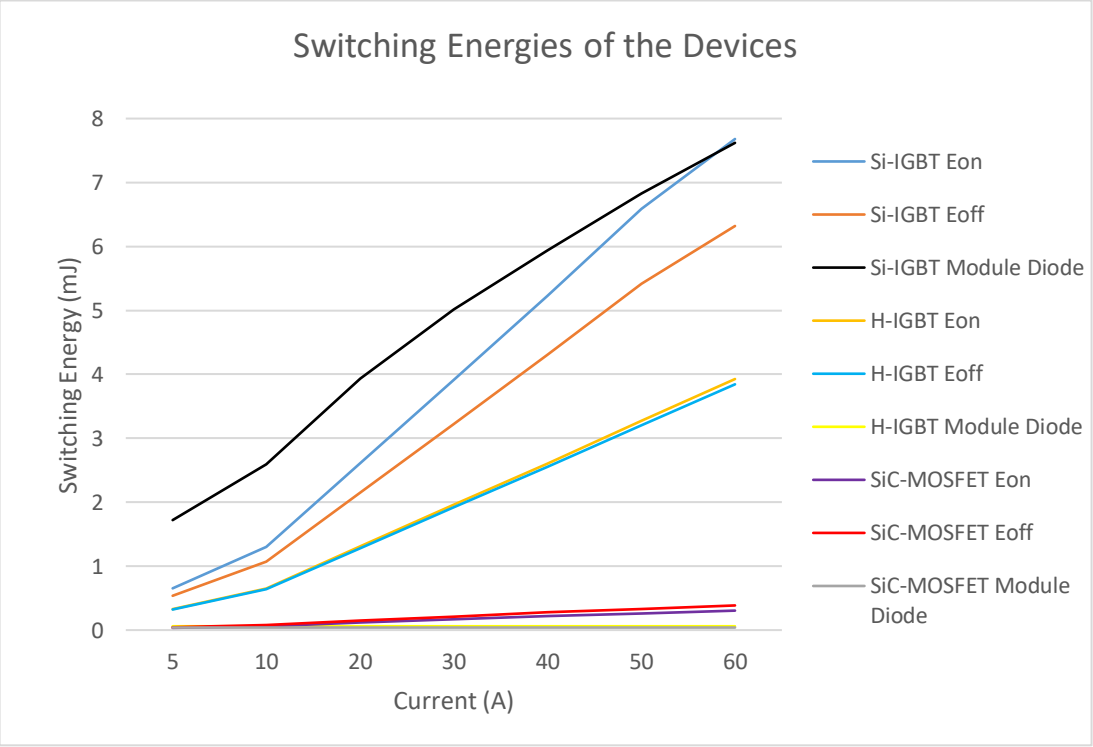


Figure 3.17 Switching energies of Si-IGBT, H-IGBT and SiC-MOSFET modules in 0 – 60 A range.

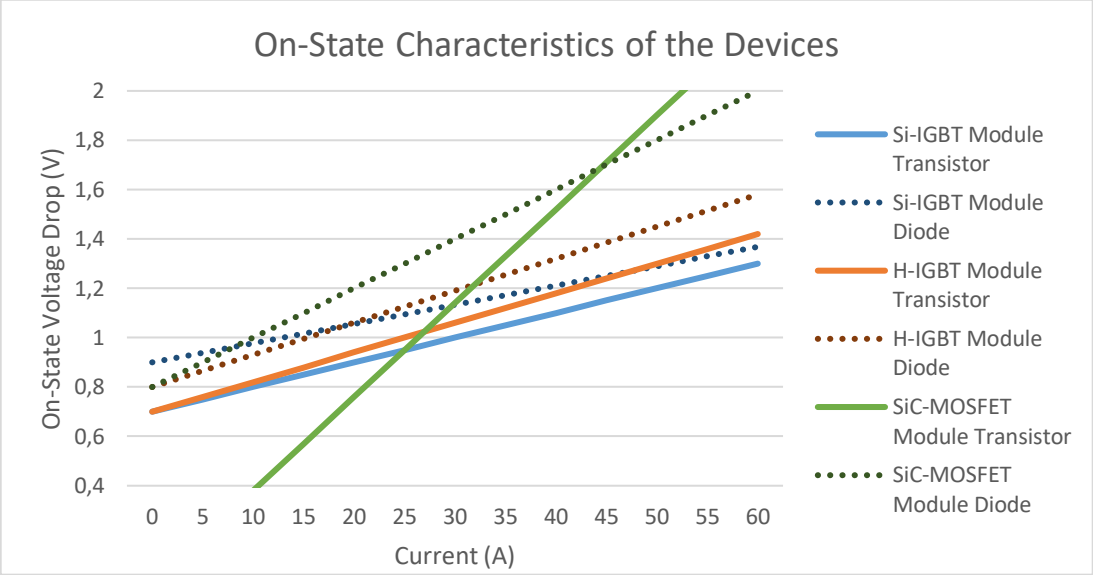


Figure 3.18 On-state voltage drop characteristics of Si-IGBT, H-IGBT and SiC-MOSFET modules in 0 – 60 A range.

Total semiconductor losses (including both transistor and diode losses) vs switching frequency plots are given in **Figure 3.19** for a 30-kW grid-connected VSC application with the same parameters given in **Table 3.1** for Si-IGBT, H-IGBT and SiC-MOSFET modules. As clearly seen, slightly higher conduction losses of H-IGBT and SiC-MOSFET modules do not affect the total semiconductor loss performance beyond 5 kHz switching frequency. On the other hand, thermal limit of Si-IGBT module transistor is reached when the switching frequency increases to 24 kHz in this VSC application. Used algorithm and equations to calculate the semiconductor losses for this application are given in Chapter 4.

In terms of performance, SiC-MOSFET module is the best and Si-IGBT module is the worst. However, cost of the device is also a very important parameter in device selection and design of the final product. Thus, economic aspects should be also taken into account while comparing the device performance. Various designs are conducted for each of these modules in Chapter 4 and economic aspects of the conducted designs are evaluated in Chapter 5.

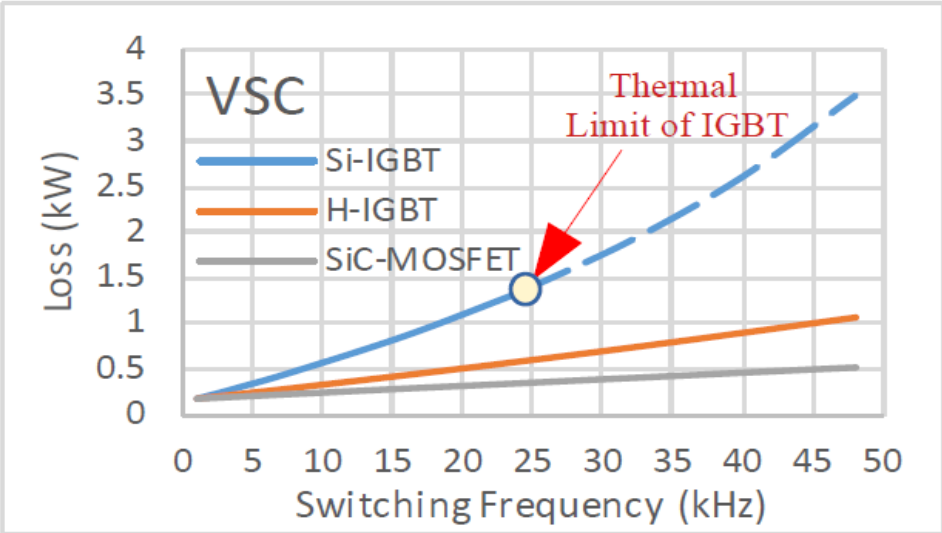


Figure 3.19 Si-IGBT, H-IGBT and SiC-MOSFET modules losses vs switching frequency for a 30-kW three-phase grid-connected VSC application.

3.4. Filter Structures

Today, most of the grid-connected VSCs use PWM modulation methods to convert DC current to AC current as also mentioned earlier in this chapter. Basically, semiconductor switches are switched at high frequencies (in kHz range) compared to fundamental grid frequency (50 – 60 Hz) to generate a sinusoidal output waveform. PWM operation naturally causes harmonic components at converter output especially at carrier frequency and its multiple frequencies. Unfortunately, it is not possible to prevent these switching harmonic components and generate exactly sinusoidal output waveform with PWM switching. However, a filter structure is used to interface the VSC to the grid and switching harmonic components are attenuated with this filter. Sufficient waveform quality can be achieved by proper selection of filter type and proper sizing of filter components. In this way, total harmonic distortion (THD) of the output waveform can be kept below 5% in grid-connected VSC applications.

The switching frequency of the VSC should be chosen as high as possible without violating the minimum efficiency criteria so that the created switching harmonic components appear at higher frequencies. As filter structure operates as a low pass

filter to attenuate the harmonic components at switching frequency, corner frequency of the filter can be set at a higher frequency with smaller filter components if switching frequency is higher. Basically, the higher the carrier frequency, the smaller the required filter size for desired power quality.

Most common filter types are L, LC, LCL and LLCL configurations as shown in **Figure 3.20**. L filter is composed of a single inductor and its attenuation characteristics is 20 dB/decade. Hence, L filter does not give satisfying results in terms of attenuation of switching harmonics. The performance of L filter can be increased by adding a shunt capacitor to the filter. Filter capacitor is selected in such a way that it provides a low impedance path for high frequency components so that attenuation performance is increased. However, in grid-connected applications, inductance of the grid also becomes part of the filter between PWM-VSC and grid so there is no real LC filter in practice in grid-connected applications but there is LCL filter.

LCL filter is the most common filter structure in grid-connected PWM-VSC applications as it has tremendous advantages over simple L filters. It can give satisfactory results with relatively smaller inductor and capacitor components compared to simple L filter [21] [25]. Thus, it has an important size and weight advantage. Basically, it acts like a simple L filter at low frequencies providing attenuation at 20 dB/decade rate due to large impedance of filter capacitance at low frequencies. However, at high frequencies, filter capacitance impedance drops significantly and LCL filter provides attenuation at 60 dB/decade rate. This is crucial for the attenuation of switching harmonics. Moreover, third order characteristics of LCL filter results in improved dynamic performance. Due to all these advantages, LCL filter is selected as the proper filter structure in this grid-connected VSC study. In some applications, another trap filter, which is tuned to the switching frequency to attenuate PWM components, can be added parallel to the filter capacitor branch. This filter structure is called LLCL filter as shown in **Figure 3.20 (d)**.

Although LCL filter has superior performance over simple L filter in terms of harmonic attenuation, it also brings a major stability problem due to LC resonant pole-pair in its structure. LCL filter has a very low impedance at its resonance frequency, so undesired harmonic components at the VSC output can be amplified inevitably causing a stability problem. In literature, passive damping and active damping methods are proposed to prevent this stability problem [21] - [26]. Passive damping methods suggest using resistors to damp the resonance oscillations. While this method provides a certain and easy solution to the problem, it reduces the efficiency and decreases the lifetime of the other components in the product due to additional heat generation. On the other hand, active damping methods suggest enhancing the control loop to damp the resonance oscillations. Active damping methods do not affect the efficiency but usually filter capacitor voltage or current is used in active damping methods and measurement of these variables require additional sensors increasing the total cost of the product.

Stability of the VSC actually depends on the parallel resonance frequency of the LCL filter, control frequency and switching frequency. It is also related with current measurement point depending on whether the converter current or grid current is measured for current regulation. That is why design of LCL filter must be considered together with the control structure of the VSC to prevent a possible stability problem.

Block diagram of LCL filter is given **Figure 3.21**. Grid inductance can also be accepted as part of L_g inductor in the stability analysis. Transfer function of the LCL filter is given in equation (3.13) and open-loop bode plot of the LCL filter system with the given filter parameters in **Table 3.1** is provided in **Figure 3.22**.

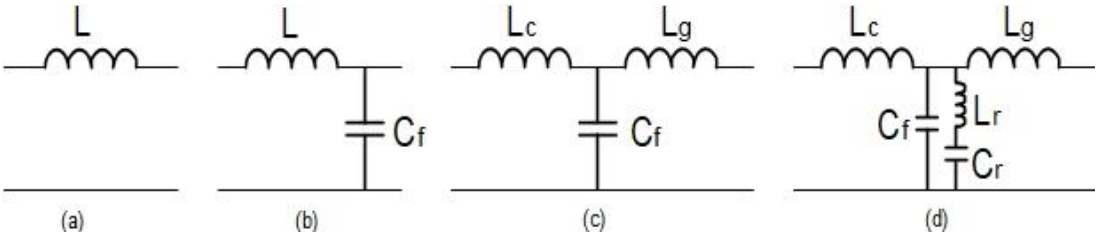


Figure 3.20 Filter types. (a) L filter. (b) LC filter. (c) LCL filter. (d) LLCL filter.

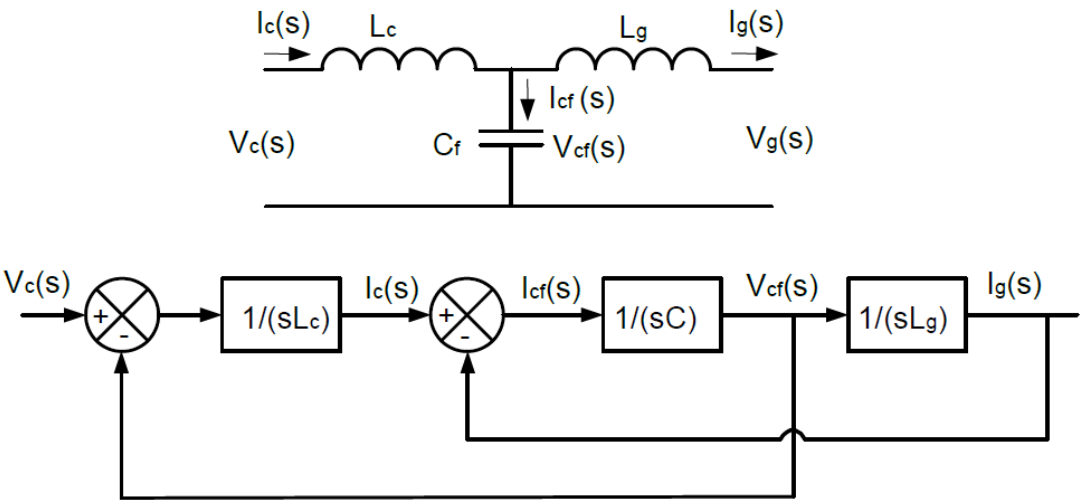


Figure 3.21 LCL filter block diagram.

$$\frac{I_g(s)}{V_c(s)} = \frac{1}{s^3 L_c C_f L_g + s(L_c + L_g)} \tag{3.13}$$

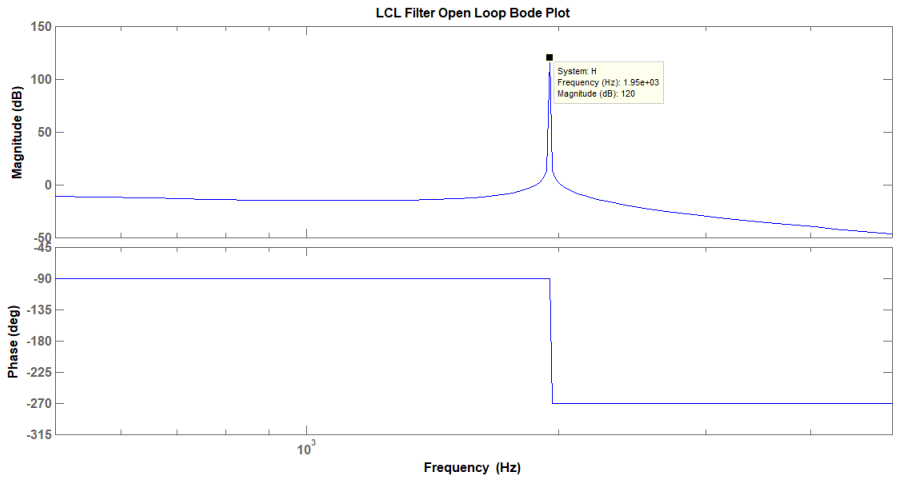


Figure 3.22 LCL filter open loop bode plot.

As clearly seen, magnitude response of the open loop bode plot of LCL filter makes a peak at parallel resonance frequency of the filter (1950 Hz in this example). At the same frequency, phase response of the system also makes a very sharp change from -90° to -270°. It means that any voltage component created by the VSC at this frequency is expected to be amplified by the filter. Stability may be lost in this

situation. Theoretically, in SPWM operation, VSC output spectrum is expected to include fundamental frequency component in low frequency region and carrier frequency and its multiple components at high frequency region while parallel resonance frequency of the LCL filter is located somewhere between them (equation (3.14) provides a rule of thumb for the location of LCL resonance frequency). However, practical conditions such as deadtime, device nonlinearities, parasitics, etc. may generate voltage components at LCL resonance frequency. Moreover, grid quality cannot be trusted in grid-connected VSC applications either. Grid may contain undesired noise components at LCL resonance frequency which may excite the resonance oscillations. VSC must have immunity against these noise components. Thus, damping is necessary in certain situations depending on the positions of parallel resonance frequency, control frequency and switching frequency. Moreover, control architecture also affects the stability and damping considerations.

$$10f_{grid} < f_{LCL-resonance} < 0.5f_{switching} \tag{3.14}$$

3.5. Control Architecture and Stability Analysis

3.5.1. Voltage Oriented Current Control Loop

As mentioned in Chapter 1, grid-connected VSCs usually use a dual control loop. An outer control loop is responsible for the regulation of DC bus voltage while a faster (up to 20 times) inner control loop regulates the output current. These control loops can be considered as completely decoupled and they can be designed independently. This control method is often denoted as voltage-oriented current control.

Voltage oriented current control diagram is shown in **Figure 3.23** and **Figure 3.24** for both stationary and synchronous frame control. The outer control loop is usually implemented as a simple PI controller. Basically, the error value between the reference value and measured DC bus voltage value is compensated by the PI controller and its output is used as a magnitude reference for the current controller. In stationary frame control, using this magnitude reference, current reference for active power can be generated in synchronization with the grid voltage using a phase-locked-loop (PLL)

algorithm. In addition, reactive power component can also be adjusted with an external command. PLL algorithm determines the angle of the reactive power component as 90° leading or lagging the grid fundamental voltage depending on whether inductive or capacitive reactive power command is given. Typically, today, grid-connected VSCs operate at unity power factor in PV power plant applications so reactive power command is automatically set as 0 in such applications. However, in the future, it is known that PV converters are expected to inject/absorb reactive power to/from grid within their capabilities according to the commands from utility to contribute to the grid stability. Thus, PLL algorithm is supposed to determine the angle of reactive power component reference too according to the given reactive power command.

In stationary frame control, current control is implemented as per phase control. In other words, each phase current is controlled independently with proposed topology. Proportional resonant (PR) controllers can be used in stationary frame control method to achieve infinite gain at a specific frequency. 3^{rd}, 5^{th}, 7^{th}, 9^{th}, 11^{th} etc. harmonic components can be cancelled by employing proportional resonant controllers.

On the other hand, synchronous frame (also known as dq frame) control can also be used to regulate the output current of the VSC. In synchronous frame, a rotating frame at grid frequency is used, and three AC phase signals are converted to two DC signals. It is easier to control DC signals because zero steady-state error can be easily achieved with an integrator. That is why PI controller is commonly used in this control method. In addition, it is sufficient to control only two signals rather than three to implement the current control in rotating frame. In synchronous frame, two DC signals, which are commonly named as d and q signals, control the active and reactive power.

Both stationary and synchronous frame control methods can be used for regulating the output current of the grid-connected three-phase VSC. Both methods can achieve satisfactory performance when they are applied correctly. Thus, details of the comparison between stationary frame and synchronous frame control methods are kept beyond the scope of this course.

Current controller is responsible for compensating the error value between the current reference and measured current value. Its output defines the VSC output voltage reference. Grid voltage can be fed forward the VSC output voltage reference to increase the immunity of VSC to the grid voltage abnormalities.

Inner current control loop requires a special emphasis as its configuration is very crucial in terms of stability of the LCL filter as mentioned. Thus, voltage control loop is kept beyond the scope of the study and current control loop is focused. Bandwidth of the current controller cannot be high enough to control the switching components at VSC output because of inevitable sampling and PWM delays in the control loop. Thus, it is a common method to design the controller according to the low frequency model where LCL filter can be denoted as a simple L filter which consists of converter side and grid side inductances. Determination of proportional and integral gain of the current PI controller is given in the equations (3.15) – (3.19) [54].

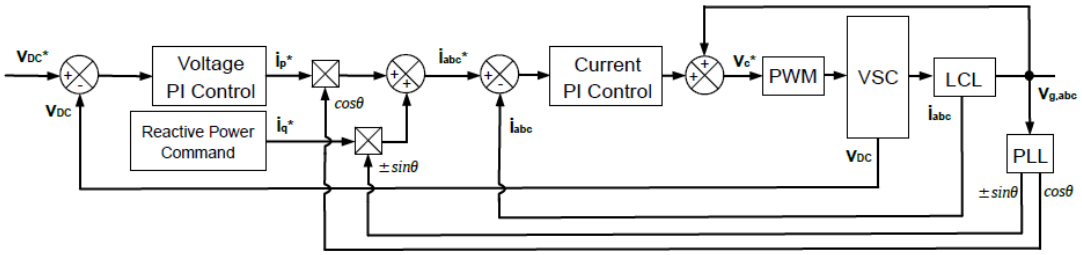


Figure 3.23 Voltage-oriented current control of three-phase grid-connected VSC in stationary frame.

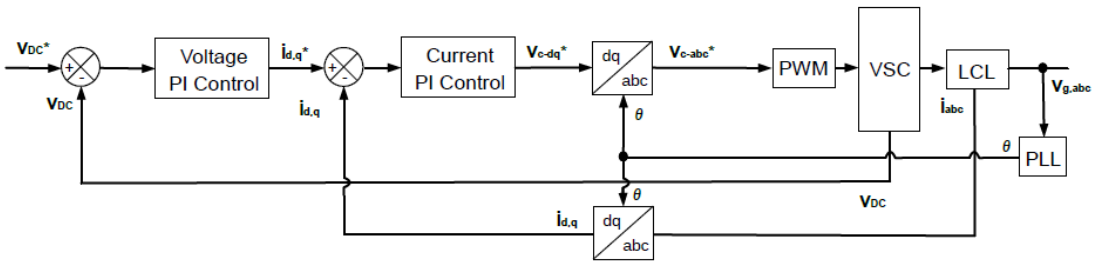


Figure 3.24 Voltage-oriented current control of three-phase grid-connected VSC in synchronous frame.

$$G_{PI}(s) = K_p + \frac{K_i}{s} \tag{3.15}$$

$$K_i = \frac{K_p}{T_i} \tag{3.16}$$

$$K_p = \frac{L_c + L_g}{\alpha T_s} \tag{3.17}$$

$$\alpha = \frac{1 + cos\theta}{sin\theta} \tag{3.18}$$

$$T_i = \alpha^2 T_s \tag{3.19}$$

As a phase margin, which is greater than 45°, defines a good design point in terms of stability considerations and disturbance rejection ratio, it is a common practice to determine θ as greater than 45°. Based on θ selection, α parameter is usually set as somewhere between 1.8 – 3. According to [26], α=3 corresponds to a good design point with approximately 4% overshoot and 3-4 sampling period settling time.

3.5.2. GCF Configuration and Stability Analysis

Either converter current (i_c) or grid current (i_g) can be used by the current control loop of a VSC with an LCL filter as mentioned before. These two configurations are respectively named as converter current feedback (CCF) and grid current feedback (GCF) configurations and control loops of them are given in **Figure 3.25**. As clearly seen, control loops include both s domain and z domain transfer functions because LCL filter is a continuous plant by nature although current control algorithm is implemented digitally. Noise filter is also implemented as an analog circuit just before the analog-to-digital converter (ADC) of the processor. Continuous and discrete plants are separated by sampling blocks as seen in **Figure 3.25**.

Both options have their own advantages and disadvantages. They will be mentioned briefly later in this chapter. However, it is a known fact that GCF is easier to implement in terms of sampling and measurement. Thus, GCF structure is used in this study so further analysis is conducted on GCF configuration. However, similar analysis can also be conducted for CCF configuration using the same methodology.

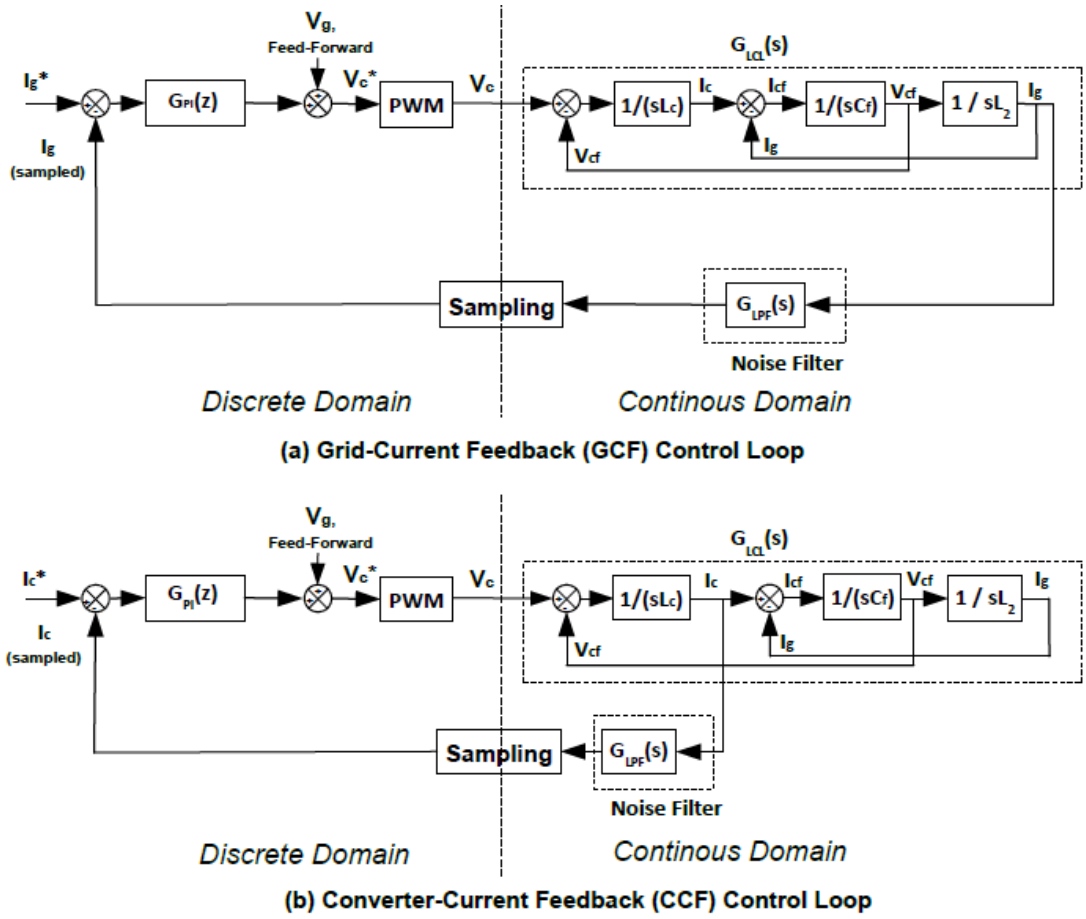


Figure 3.25 GCF and CCF Loops.

Converter current feedback (CCF) configuration allows the direct measurement of semiconductor current so that it can provide an instantaneous protection for the semiconductor. In addition, it has inherent damping characteristics. It means that it does not require an active damping modification in its control loop for stability [25]. However, it does not directly measure the grid current so that exact control of power factor is not possible. Reactive power consumption of the filter capacitor can be estimated and taken into account while designing the control loop, but this does not provide an exact solution due to aging of the filter components. Moreover, sampling of the fundamental current component on converter side is a difficult task due to PWM ripple components that it contains.

On the other hand, measurement of fundamental current component is easier in terms of sampling in grid current feedback (GCF) configuration. Because negligible amount of PWM ripple components exist in grid current. In addition, the current at PCC is directly measured in GCF configuration so that exact power factor control is possible. This is a very important feature for grid-connected VSC applications. Thus, GCF configuration is used in this study. However, it must be taken into account that GCF configuration requires active damping modifications in its control loop to ensure stability in certain situations [23]-[26]. Position of LCL resonance frequency and control frequency determine the stability of GCF configuration. Holmes *et al*. define a critical frequency, which is defined in equation (3.20), in discrete time analysis of GCF configuration to determine stability regions [24]. If LCL resonant frequency is above this critical frequency, stability can be achieved without damping. However, if it is below this critical frequency, damping is necessary to ensure stability.

$$f_{critical} = \frac{f_{sampling}}{6} \tag{3.20}$$

It is an easy and a common method to tune the controller in s domain as if the current control is implemented in analog domain. Then, designed controller can be transformed into discrete domain via bilinear (Tustin) transformation. Conducting the controller design in discrete domain from the beginning gives more appropriate results but it takes a considerable amount of design effort and it is beyond the scope of this study. However, stability analysis should be conducted in discrete domain to address the sampling phenomenon and discrete PWM nature of the converter. That is why control loop of GCF configuration is analyzed both in continuous and discrete domains. The control loops of GCF configuration in both continuous domain and discrete domain are given in **Figure 3.26**. Active damping using the capacitor voltage or current is not included in the control loops as it is beyond the scope of the study. Detailed information is available about active damping methods in GCF configuration in [23]-[26].

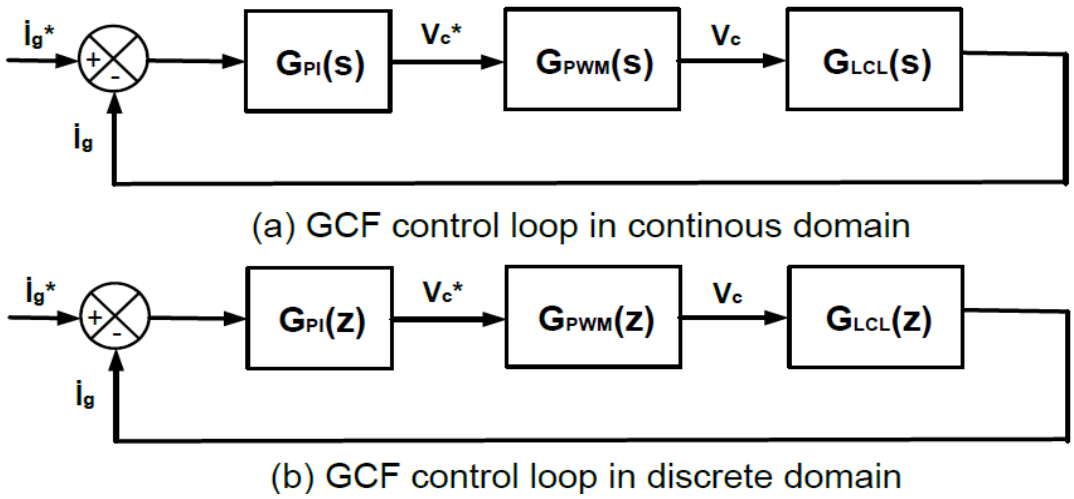


Figure 3.26 GCF configuration control loops for stability analysis. (a) Continuous domain. (b) Discrete domain.

Grid voltage is supposed to include only positive-sequence components at fundamental frequency that is why grid is modelled as a short-circuit in the proposed control loops. In addition, measurement delays such as transducer and noise filter delays are neglected here. These delays are further analyzed in detail in Chapter 6.

Transfer functions in s domain are given in the equations (3.21) – (3.23). In these equations, $G_{PI}(s)$ represent the PI controller whereas K_P is proportional gain and K_i is integral gain. $G_{PWM}(s)$ must be included in control loop models in continuous domain to model PWM delay which is known to exist in practical application. Otherwise, designed controller in s domain would not give accurate results when it is transformed into discrete domain. In single – update PWM method, PWM delay can be at worst equal to one PWM cycle period when samples are taken at the beginning of each switching period and recent state of the system are not sampled till the beginning of next switching period. Thus, T_{PWM} is selected as equal to $1/f_{sw}$.

$$G_{PI}(s) = K_p + \frac{K_i}{s} \tag{3.21}$$

$$G_{PWM}(s) = \frac{1}{1+sT_{PWM}} \tag{3.22}$$

$$G_{LCL}(s) = \frac{I_g(s)}{V_c(s)} = \frac{1}{s^3 L_c C_f L_g + s(L_c + L_g)} \tag{3.23}$$

To be able to conduct a stability analysis on the system properly, all the transfer functions in the continuous domain control loop must be transformed into discrete domain. In discrete domain control loop, $G_{PI}(z)$ denotes the PI controller in z domain and it can be obtained via applying Tustin transformation to $G_{PI}(s)$. $G_{PWM}(z)$ can be modelled with a unit delay operator z^{-1} if sampling frequency is selected as equal to switching frequency. $G_{LCL}(z)$ can be obtained by applying zero-order-hold (ZOH) discretization method (with sampling period T_s) to transfer function $G_{LCL}(s)$. Equations (3.24) – (3.26) gives the discrete domain transfer functions.

$$G_{PI}(z) = K_p + \left(\frac{K_i * T_s}{2}\right) x \left(\frac{z+1}{z-1}\right) \tag{3.24}$$

$$G_{PWM}(z) = z^{-1} \tag{3.25}$$

$$G_{LCL}(z) = \frac{T_S}{(L_c+L_g)(z-1)} - \left(\frac{sin(\omega_{res} * T_S)}{\omega_{res}(L_c+L_g)}\right)\left(\frac{z-1}{z^2-2*z*cos(\omega_{res}*T_S)+1}\right) \tag{3.26}$$

An example stability analysis is conducted with the LCL filter parameters given in **Table 3.1**. In order to take the worst case into account in terms of stability, LCL filter components are assumed as ideal lossless components. LCL resonance frequency is set approximately as 1950 Hz in this example. Discrete control loop in **Figure 3.26 (b)** is used with the transfer functions given in equations (3.24) – (3.26). Current controller parameters K_p and K_i are set as 5 and 10000 respectively (θ is set as 55° and corresponding α value is 1.92 with 8 kHz sampling frequency).

Stability analysis is conducted for two sampling frequencies: 8 kHz and 16 kHz. Critical frequencies correspond to 1.33 kHz and 2.66 kHz respectively according to the equation (3.20). **Figure 3.27** shows the pole-zero plot for each case. As expected, system is stable with all poles inside the unit circle when sampling frequency is selected as 8 kHz (LCL resonance frequency is higher than critical frequency). However, system is not stable when sampling frequency is selected as 16 kHz (LCL resonance frequency is lower than critical frequency).

Note that selected proportional gain value is not re-tuned when sampling frequency is increased to 16 kHz. Normally, re-tuning of the controller parameters results in a

doubled proportional gain when sampling frequency is doubled, and it even pushes the system poles more towards the outside of the unit circle. Although proportional gain is kept relatively low, still stability cannot be achieved when sampling frequency is doubled, and critical frequency is made greater than LCL resonance frequency.

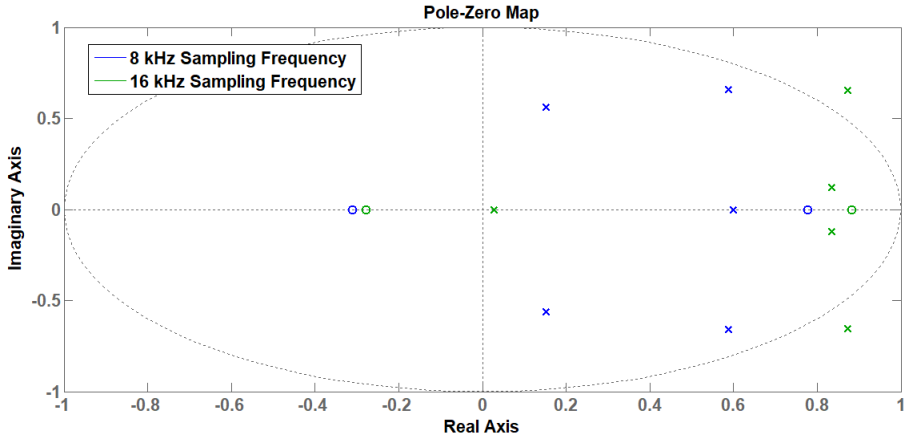


Figure 3.27 Pole-zero map for discrete GCF loop for two different sampling frequencies.

3.6. Conclusion

In this chapter, state of the art in grid-connected three-phase VSC technologies is reviewed. Present topologies, modulation methods, filter structures and control methods are summarized. Specifically, on-grid PV applications is considered and three two-level VSC topologies (namely floating, semi-floating, and solidly-connected) are compared comprehensively taking the ground leakage current into account. Solidly-connected VSC topology is chosen for design due to its superior common-mode component suppression characteristics. As zero-sequence injection is not possible with this topology, SPWM is chosen as modulation method. In Chapter 4, a design methodology will be presented with this chosen topology and modulation method and a reference design with conventional Si-IGBT will be implemented. Then, progressive design cases with H-IGBT and SiC-MOSFET modules are proposed and economic assessments of the proposed design cases are presented in Chapter 5.

CHAPTER 4

DESIGN OF A GRID-CONNECTED VSC INCLUDING POWER MODULE SELECTION, HEATSINK SIZING, INDUCTOR DESIGN AND CONTROL ARCHITECTURE

4.1. Introduction

In previous chapters, a background information is provided about on-grid PV systems and today's three-phase grid-connected VSC technologies. Using this background information, a reference hardware design for a 30-kW grid-connected three-phase VSC with Si-IGBT modules is investigated in this chapter. In addition, four fundamental design cases are proposed for retrofitting approach with H-IGBT or SiC-MOSFET modules. Each design case is evaluated in terms of efficiency by theoretical calculations. First and third design cases are also verified by experimental results.

As mentioned in Chapter 3, solidly-connected topology is used in this study due to its superior characteristics in suppressing common-mode components in PV applications. LCL filter structure is employed because of its numerous advantages over simple L filter in grid-connected VSC applications. PV converter is designed as a double-conversion converter with a boost converter at the input and a grid-connected PWM-VSC at the output. General circuit scheme of the PV converter is shown in **Figure 4.1**.

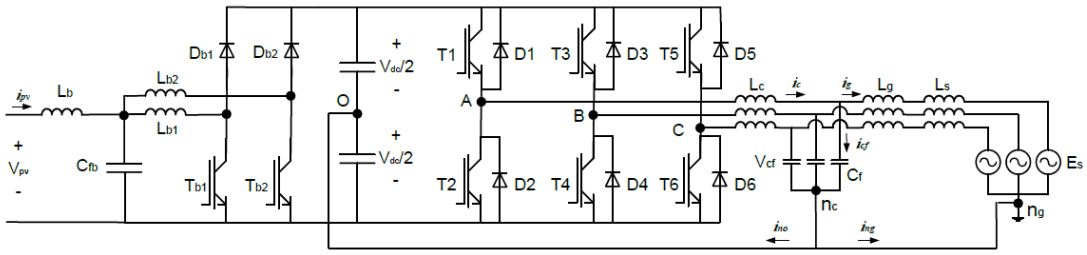


Figure 4.1 PV converter general circuit scheme.

While design of boost converter is kept beyond the scope of this study, its efficiency is still taken into account when total efficiency is calculated. However, its hardware design is not included in this study. Instead, grid-connected three-phase VSC hardware structure is investigated in detail including semiconductor sizing, heatsink sizing, and LCL filter sizing.

First, design specifications of the reference design are provided in **Table 4.1** and then a design methodology is presented. Sizing of semiconductors, heatsink, and inductors are mentioned in this design methodology. Moreover, reference design is confirmed by the proposed design methodology. Finally, progressive design cases are provided with H-IGBT and SiC-MOSFET modules. Heatsink and inductors are also re-sized in each design case.

Table 4.1 Design specifications of the reference design

Rated Output Power (P_o)	30 kW
DC Bus Voltage (V_{DC})	750 V DC
Grid Voltage (line to line)	400 V AC
Grid Frequency (f_g)	50 Hz
Power Factor (PF)	1
THD at Rated Power (THD)	<5%
Efficiency at Rated Power	>97.5%

4.2. Design Methodology

It is a common practice to start a design by determining the capabilities of the semiconductor module. So, first, semiconductor losses are analyzed. An algorithm is developed to calculate semiconductor losses in a two-level three-phase VSC topology taking the steady-state thermal analysis into account as junction temperature significantly affects the semiconductor losses. Equations for both conduction and switching losses are provided. In addition, steady-state thermal analysis is conducted together with sizing of the heatsink and cooling system.

After heatsink, sizing of inductors is completed. Converter side inductor design with powder cores is provided in detail. Copper losses are calculated taking the skin effect

and proximity effect into account. Core losses are calculated with a specifically developed algorithm for core loss calculation in grid-connected VSC applications. Eventually, inductor losses are also taken into account as well as semiconductor losses in efficiency calculations. Design flow chart is provided in **Figure 4.2**.

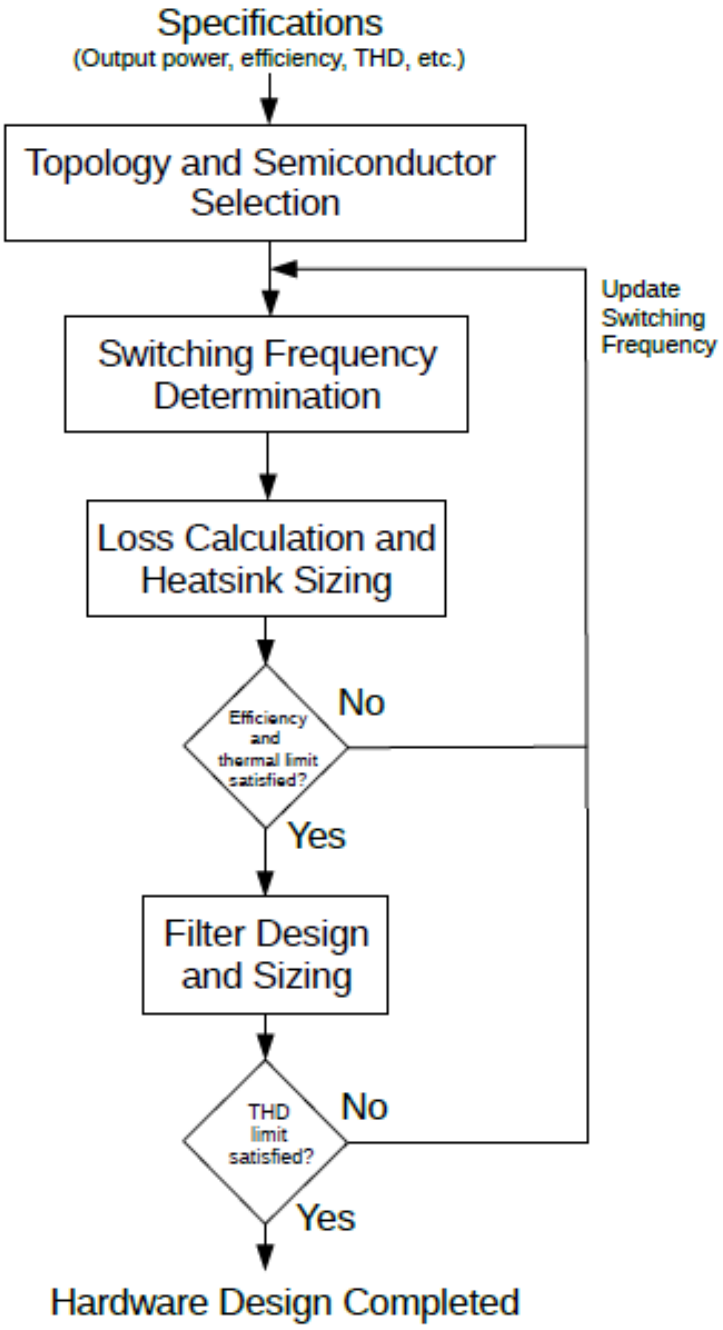


Figure 4.2 Design methodology flowchart.

4.2.1. Semiconductors and Loss Calculation Algorithm

The major source of power loss in a VSC is the semiconductors. Thus, semiconductor capability determines the limits for the switching frequency and efficiency of the whole converter. As efficiency is one of the most important criteria in a grid-connected VSC and as semiconductor losses form majority of the losses, it is very crucial to estimate the semiconductor losses of a VSC in early design stages because it is not possible to put an efficiency aim without estimating the semiconductor losses. However, semiconductor losses depend on many parameters such as DC link voltage, switching frequency, junction temperature, output power and so on [55]. Thus, estimating the semiconductor losses and junction temperature is not straightforward since both junction temperature and semiconductor losses affect each other. In this chapter a loss calculation algorithm, which also takes steady-state thermal analysis and junction temperature into account, is presented.

Figure 4.4 presents a flow diagram for the loss calculation algorithm for a two-level three-phase converter application for unity power factor operation. First, application inputs such as output power (P_o), DC link voltage (V_{DC}), line to line rms grid voltage ($V_{g\text{-}rms}$), grid frequency (f_g) and switching frequency (f_{sw}) are defined. Then algorithm can calculate the frequency modulation (ratio of switching frequency to fundamental frequency, M_f), amplitude modulation (ratio of peak phase voltage to half of DC bus voltage, Ma), output RMS current (I_o) and output peak current value (I_{op}) using the equations (4.1) – (4.4).

$$M_f = \frac{f_{sw}}{f_g} \tag{4.1}$$

$$M_a = \frac{V_g}{0.5\ x\ V_{DC}}\ x\ \sqrt{\frac{2}{3}} = \frac{V_{phase-rms}\ x\ \sqrt{2}}{0.5\ x\ V_{DC}} \tag{4.2}$$

$$I_o = \frac{P_o}{V_g\ x\ \sqrt{3}} \tag{4.3}$$

$$I_{op} = I_o * \sqrt{2} \tag{4.4}$$

Once the application inputs are defined and other necessary parameters are calculated using the given equations, it is time to define semiconductor parameters. Semiconductor parameters can be classified in three groups as follows:

i. Static Parameters : Static parameters are related with conduction losses. On-state junction voltage drop (V_{ceo} for IGBTs) and on-state resistance (r_{ce} for IGBTs and $R_{ds\text{-}on}$ for MOSFETs) are static parameters. Similarly, forward voltage (V_f) and forward resistance (r_f) of the diodes are also static parameters. These parameters mostly depend on junction temperature and current magnitude (especially V_{ceo} and V_f).

ii. Dynamic Parameters : Dynamic parameters are related with switching losses and switching times. Rise time (t_r) and fall time (t_f) are dynamic parameters. Manufacturers usually provide turn-on energy (E_{ON}) and turn-off energy (E_{OFF}) under certain circumstances for loss calculations. Similarly, reverse-recovery energy (E_{RR}) can also be given for diodes.

iii. Thermal Parameters : Thermal parameters are related with the thermal analysis model of the device and the package. Junction to case thermal resistance ($R_{th(j\text{-}c)}$) is given for estimating the junction temperature with respect to the case of the device and case to sink thermal resistance ($R_{th(c\text{-}s)}$) may be provided for specific thermal grease material.

Static and dynamic parameters of the semiconductors are defined first. Then, characteristics of static and dynamic parameters are approximated with 2^{nd} or higher order polynomials depending on the number of available data points. As output current is not constant but sinusoidally varying in converter applications, this approximation is necessary to determine the static and dynamic parameters in each PWM cycle according to the corresponding to the current magnitude in that PWM cycle.

It is essential to define static and dynamic parameters at two different junction temperatures to be able to use interpolation or extrapolation methods to determine corresponding static and dynamic parameters at a specific junction temperature.

After defining the static and dynamic parameters and approximating their characteristics vs current magnitude with polynomials, thermal parameters of the semiconductor device and surroundings are defined. Junction to case thermal resistances of both transistor and diode, case to heatsink thermal resistance of the package, heatsink thermal resistance and ambient temperature values are given as inputs to the algorithm.

In order to start iterations for loss calculation, initial value of the junction temperature is set as the maximum junction temperature at which static and dynamic parameters are defined. Then conduction losses and switching losses are calculated. Total losses can be multiplied with 1.05 as a safety margin in practical designs. At the end, heatsink temperature and junction temperature are estimated. Estimated junction temperature and initial value of junction temperature is compared. If the difference is greater than 1 °C, it means junction temperature is expected to be lower than initially guessed value in this application and initial value is updated. Iterations are repeated till the difference between estimated junction temperature value and initial value becomes less than 1 °C. Another criterion may be also set such as comparing the difference as a percent value instead of specifying it as 1 °C. However, it is set as 1 °C in this study since measuring the temperature with high sensitivity and keeping the ambient temperature same during the experiments are quite cumbersome.

4.2.1.1. Conduction Losses

An ideal switch is expected to hold zero voltage on itself while conducting a current and dissipate zero power. However, there is no ideal switch in practice and semiconductor switches also have an on-state voltage drop while conducting a current creating conduction losses. Conduction losses can be calculated by summing the power loss on junction voltage drop and power loss on the equivalent series on-state resistance of the semiconductor device. Equations (4.5) – (4.8) show how to calculate the conduction losses in a two-level three-phase VSC [55], [58]. Note that $I_{tr\text{-}av}$ represent the average current of the transistor and $I_{tr\text{-}rms}$ represent the rms current of

the transistor whereas $I_{d\text{-}av}$ represent the average current of the diode and $I_{d\text{-}rms}$ represent the rms current of the diode. This conduction loss equation is given for IGBTs, but it can be also applied to MOSFETs by ignoring the first term which includes junction voltage drop and replacing the r_{ce} term with $r_{ds\text{-}on}$ term.

$$P_{con-tr} = V_{ceo} * I_{tr-av} + r_{ce} * I_{tr-rms}^2 \quad (4.5)$$

$$P_{con-d} = V_{fo} * I_{d-av} + r_f * I_{d-rms}^2 \quad (4.6)$$

$$P_{con-tr} = \left(\frac{1}{2\pi} + \frac{M_a * PF}{8}\right) * V_{ceo}(T_j) * I_{op} + \left(\frac{1}{8} + \frac{M_a * PF}{3\pi}\right) * r_{ce}(T_j) * I_{op}^2 \quad (4.7)$$

$$P_{con-d} = \left(\frac{1}{2\pi} - \frac{M_a * PF}{8}\right) * V_{fo}(T_j) * I_{op} + \left(\frac{1}{8} - \frac{M_a * PF}{3\pi}\right) * r_f(T_j) * I_{op}^2 \quad (4.8)$$

4.2.1.2. Switching Losses

Another source of loss for semiconductors is the switching losses. There is a finite period where both voltage and current are not zero in switching of a semiconductor switch in hard-switching circuits and this causes the switching losses.

As seen in **Figure 4.3**, magnitude of conducted current, magnitude of blocked voltage and switching times affect the switching losses. However, these waveforms are not ideal as given in **Figure 4.3** in practice. Thus, it is not easy to calculate the switching losses straightforwardly by calculating the triangle area under switching loss waveform. Thus, IGBT and MOSFET manufacturers provide data about dynamic characteristics of the device such as turn-on energy loss (E_{on}), turn-off energy loss (E_{off}), reverse recovery loss of the anti-parallel diode (E_{rr}) under certain conditions (specific junction temperature, gate resistance, voltage and current). Switching losses of transistor and diode can be calculated using these data with the equations (4.9) and (4.10) [59]. Note that V_{DC} denotes the DC link voltage and V_{NOM} denotes the nominal DC voltage for which the E_{on} and E_{off} are given. In addition to these switching losses, power loss at the output capacitance of the MOSFET should be also taken into account while calculating the switching losses of a SiC-MOSFET module. Output capacitance switching loss of a MOSFET can be calculated with the equation (4.11).

Note that effect of DC link voltage must be also taken into account in estimation of switching losses [60]. It is proposed that dependency of IGBT switching losses and diode reverse recovery losses on switching voltage can be modelled with exponents 1.3 and 0.6 respectively [55]. However, dependency of MOSFET switching losses on switching voltage is assumed as linear in loss calculations.

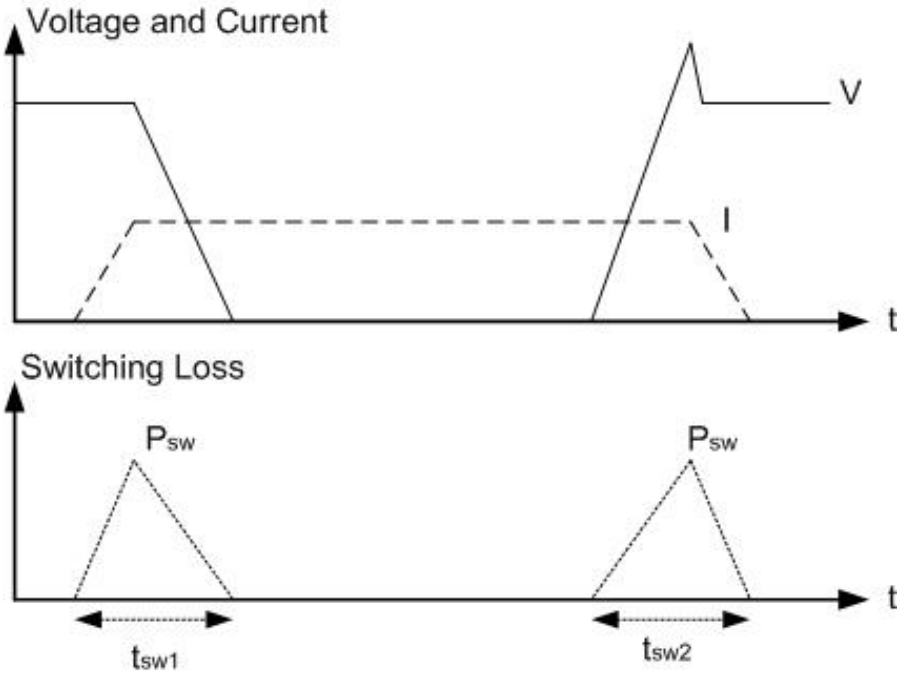


Figure 4.3 Idealized switching characteristics of semiconductor switches.

$$P_{sw-tr} = f_g * \left(\frac{V_{DC}}{V_{NOM}}\right)^{1.3} \sum_{k=1}^{M_f/2} [E_{on}\left(I_{op}\, sin\left(\frac{2k\pi}{M_f}\right)\right) + E_{off}(I_{op} sin(\frac{2k\pi}{M_f}))] \quad (4.9)$$

$$P_{sw-d} = f_g * \left(\frac{V_{DC}}{V_{NOM}}\right)^{0.6} \sum_{k=1}^{M_f/2} [E_{rr}\left(I_{op}\, sin\left(\frac{2k\pi}{M_f}\right)\right)] \quad (4.10)$$

$$P_{MOSFET-Coss} = \frac{1}{2} C_{oss} V_{DC}^2 f_{sw} \quad (4.11)$$

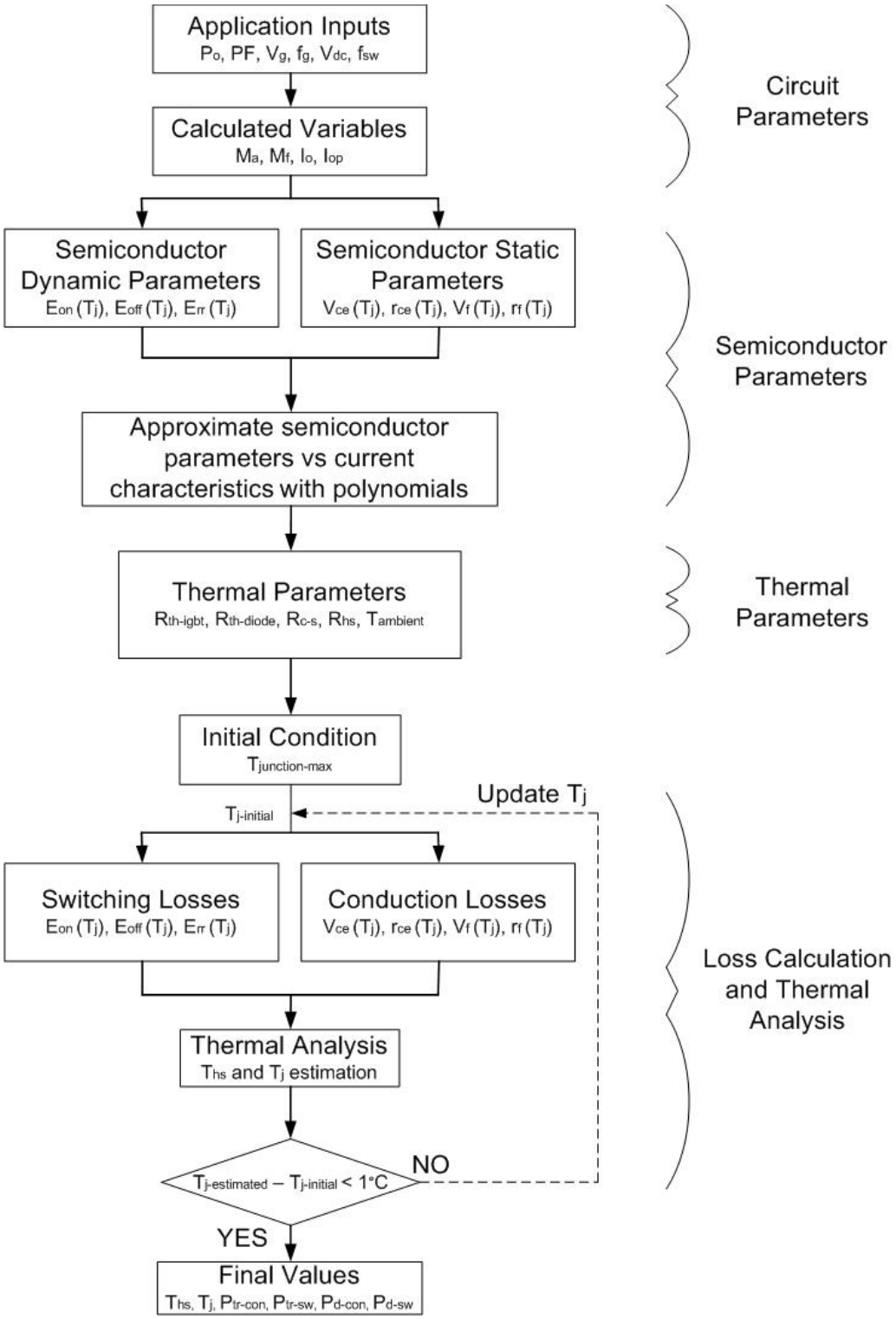


Figure 4.4 Developed loss calculation algorithm.

4.2.2. Thermal Model, Heatsink Sizing and Thermal Analysis

As mentioned, semiconductors are the main power loss source in a power converter and unless necessary precautions are taken, the dissipated power in the semiconductors may cause too high junction temperature and semiconductors may be permanently damaged. Heatsinks are employed attached to the semiconductors to provide a thermal path for dissipated power on semiconductors. Junction temperature of the semiconductors is kept within a reasonable range in this way. Heatsinks must have low thermal resistance values to be able to provide a good thermal conductivity between the semiconductors and surroundings. As the amount of heat energy which is supposed to be thrown out of the semiconductors increases, size of the heatsink increases too. Somehow, if amount of semiconductor losses is decreased in a VSC achieving a higher efficiency value, a smaller heatsink can also function well. This means an advantage in weight, size and cost of the VSC.

In order to conduct a steady-state thermal analysis and estimate the heatsink, case and junction temperatures, heatsink thermal resistance must be estimated. This is essential because semiconductor losses depend heavily on junction temperature [55]. Similarly, it is not possible to estimate the junction temperature in steady-state thermal model unless heatsink resistance is estimated. Thus, a method to estimate the thermal resistance of a heatsink based on its raw material, geometry and air flow capability of the fans is also given.

Thermal resistance is inversely proportional with the thermal conductivity of the raw material and surface area. That is why heatsinks are designed in a way to increase the surface area as much as possible. An example heatsink is shown in **Figure 4.5**. As clearly seen, surface area of the heatsink is increased with thin fins. Usually elements with a high thermal conductivity such as copper (~ 400 W/m K) and aluminum (~ 235 W/m K) are used in the structure of a heatsink as raw material. Copper has superior thermal conductivity characteristics, but it is heavier and more expensive then aluminum. Therefore, aluminum is also a good choice as raw material of a heatsink.

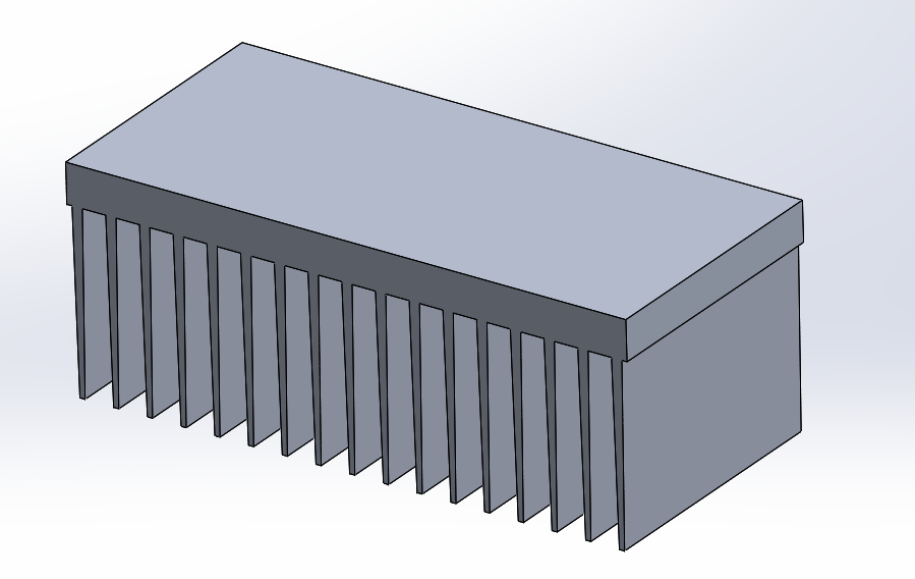


Figure 4.5 Example heatsink drawing.

Smoothness of the heatsink surface is essential because heat transfer from semiconductor case to heatsink occurs through this surface. In case of any imperfectness in this surface, semiconductor and heatsink touch each other only at certain points and the rest of the contact area is filled with air. Air is a very good thermal insulator and if heatsink surface is rough even in millimeters range, air cavities between the semiconductor and heatsink increases the thermal resistance dramatically.

Semiconductors are mostly mounted on heatsink surface with screws to prevent air cavities between semiconductor and heatsink. However, if screws are applied with excessive amount of torque, contact distance between one side of the semiconductor package and the heatsink may increase [56]. An example of this situation can be seen in **Figure 4.6**. Thus, applying correct amount of torque to each screw is essential.

A thermal grease component is applied between semiconductor package and heatsink to prevent air cavities. Applying thermal grease component requires high amount of attention. If applied thermal grease layer is too thin, it may not be enough to prevent the existence of air cavities. However, if the applied thermal grease layer is too thick, the thermal resistance of the layer may be more than expected [57].

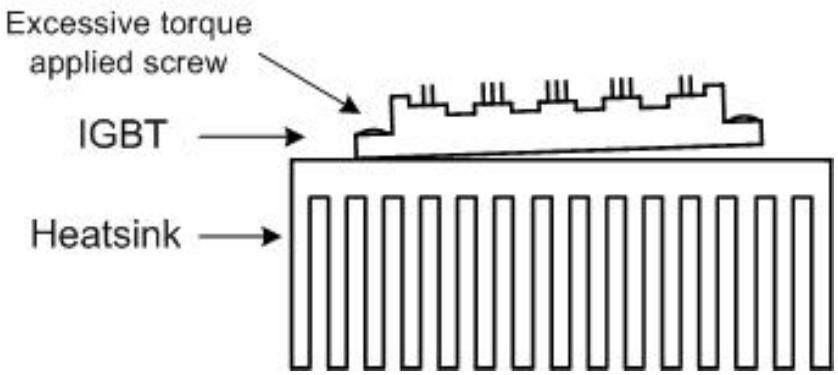


Figure 4.6 An example of excessive applied torque to a screw on semiconductor.

In addition to raw material, heatsink shape, mounting method of the semiconductor and thickness of the thermal grease, cooling type also affect the thermal resistance of the system. Various cooling methods can be used depending on the application such as natural air cooling, forced air cooling, liquid cooling and so on.

Liquid cooling is an expensive solution, but it has superior performance over air cooling. As heat capacity of liquid coolants is higher than air, they can transfer the heat more efficiently. Size of a heatsink can be reduced by using liquid cooling instead of air cooling. However, liquid cooling is only preferred at applications where size of the product is very critical. Otherwise, it is not very common because of its high cost.

Air cooling can be divided into two categories as natural and forced cooling. Natural cooling may be preferred at low power applications where heatsink alone is enough to throw the dissipated heat in the semiconductors away without a forced air flow. Natural cooling may also be preferred at applications where noise level must be below a certain level (residential applications, libraries etc.) as fans are noisy components by their nature. However, designing a power converter without a fan requires larger heatsink and this increases both size and cost of the product. Using a fan provides an air flow through the heatsink and decreases the heatsink to ambient thermal resistance. Thus, forced air cooling is chosen and investigated for thermal analysis in this study.

First, operating point of heatsink and fan system must be determined to be able to find the corresponding thermal resistance value. Both heatsink and fan pressure vs air flow

characteristics can be approximated by second order polynomials as shown in **Figure 4.7 (a)**. Common solution of these two polynomials have two roots. One of the roots correspond to the true air flow – pressure operating point.

Thermal resistance of the heatsink is inversely proportional with the air flow as air flow increases the heat transfer through the heatsink surface. By obtaining thermal resistance vs air flow data points, thermal resistance characteristics with respect to air flow can also be approximated by a polynomial. Once the air flow operating point is determined, thermal resistance of the heatsink can be easily estimated by taking the corresponding thermal resistance value in thermal resistance vs air flow polynomial as shown in **Figure 4.7 (b)**.

Degree of the polynomial can be better determined by analyzing the thermal resistance vs air flow data points. Second degree polynomial may not be enough to approximate the thermal resistance vs air flow characteristics of the heatsink. That is why data points and approximated curve should be compared and a higher order polynomial should be used for approximation if it is necessary.

Steady-state thermal model of the semiconductors and heatsink is useful estimating the junction temperature of the semiconductors. Semiconductor junction can be considered as a heat source in practice and dissipated heat must be taken out to prevent junction temperature reaching very high values. Today's Si semiconductor technology allows junction temperatures up to 150 °C or 175 °C without permanent damage to the device but it is a common practice to keep semiconductor junction temperature below 125 °C for higher lifetime of the semiconductors. SiC technology allows higher junction temperatures safely but package technology is the limiting factor so still junction temperatures in the range of 150 °C may not be a good solution.

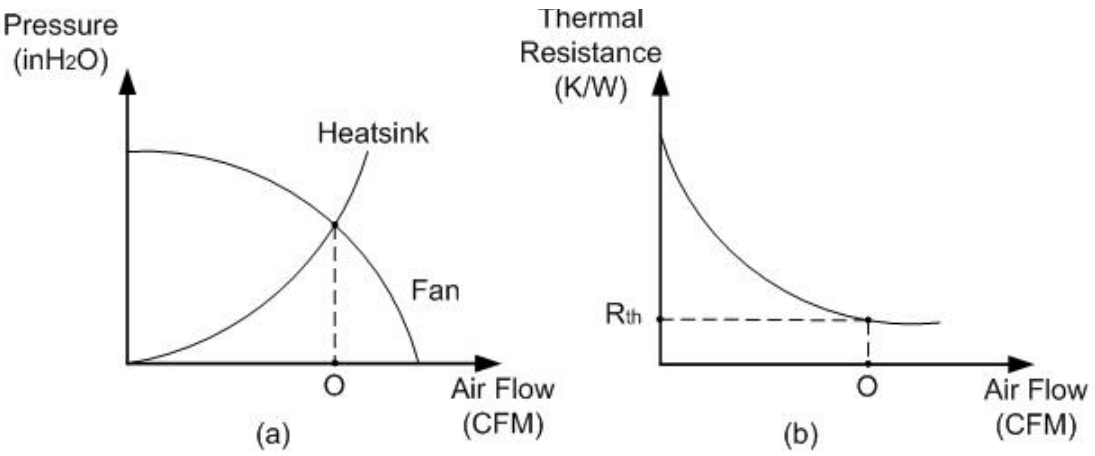


Figure 4.7 (a) Fan and heatsink pressure vs air flow characteristics. (b) Heatsink thermal resistance vs air flow characteristics.

Generated heat energy in the junction of the semiconductor is first transferred to the semiconductor package case through junction to case thermal resistance. Then, it is transferred to the heatsink through case to heatsink thermal resistance. Although a thermal grease layer is used between semiconductor and heatsink here, still a finite thermal resistance, which cannot be neglected, exists between semiconductor case and heatsink. Then heat energy is conducted to ambient environment through thermal resistance of the heatsink. This steady-state model is shown in **Figure 4.8 (a)**.

Dynamic model of this thermal system can be modelled with first order circuits including resistors and capacitors. However, only steady-state thermal model of the system is analyzed in this study and capacitors can be ignored at steady-state model. Thus, as an electrical analogy of this thermal model can be represented in steady-state with simple resistors. as shown in **Figure 4.8 (b)**. This model is used in estimating the junction temperature in the loss calculation algorithm which is given in **Figure 4.4**. Heatsink and junction temperatures are calculated with the equations (4.12) and (4.13).

In fact, more realistic thermal models can be much more complicated. Detailed simulation tools are required to simulate these thermal systems. However, the simple thermal model described in this study is also very efficient to estimate heatsink temperature, semiconductor package case temperature and semiconductor junction temperature according to the ambient temperature.

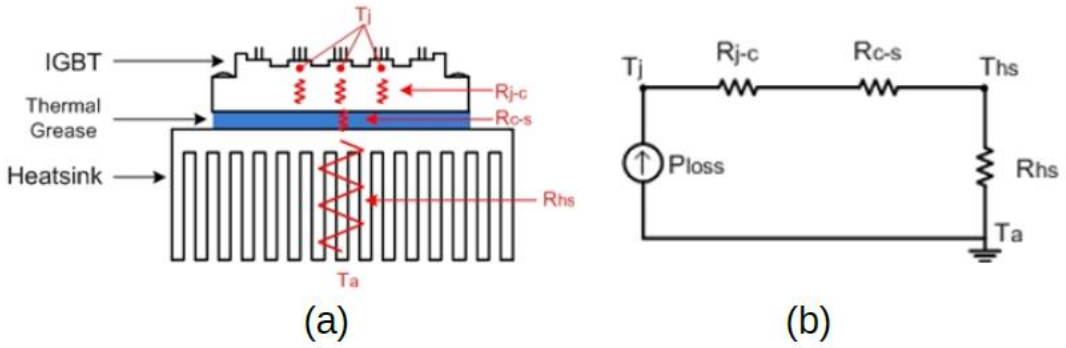


Figure 4.8 (a) Steady-state thermal model of the semiconductor and heatsink. (b) Electrical analogy of the thermal model.

$$T_{hs} = P_{loss}\, x\, R_{hs} + T_a \tag{4.12}$$

$$T_j = P_{loss}\, x\, \left(R_{j-c} + R_{c-s}\right) + T_{hs} \tag{4.13}$$

4.2.3. Inductor Design and Inductor Losses

4.2.3.1. Inductor Design

Converter side inductor and grid side inductor have different characteristics. While converter current includes a significant amount of high frequency PWM components, grid current is mostly composed of low frequency fundamental component. Thus, especially converter side inductor requires a special attention and design of converter side inductor is focused in this part of the dissertation.

Inductance factor is a parameter that defines the inductance per square of number of turns. It is usually provided by core manufacturers because it provides an easy and straightforward guidance for the design engineer. Equations (4.14) – (4.16) can be used for a uniform linear magnetic circuit. By substituting (4.14) and (4.15) in (4.16), we get the equation (4.17). So, inductance factor (A_L) can be defined with equation (4.18). In the equations (4.14) – (4.17), F, I, ϕ and R denote magnetomotive force (MMF), current , magnetic flux and magnetic reluctance respectively. L represents inductance, λ represents flux linkage and l represents the magnetic mean length. μ_0 and μ_r represent permeability of free space and relative permeability respectively.

$$F = NI = \phi R \tag{4.14}$$

$$R = \frac{l}{\mu_0 \mu_r A} \tag{4.15}$$

$$\lambda = N\phi = LI \tag{4.16}$$

$$L = \frac{N^2}{R} = \frac{N^2 \mu_0 \mu_r A}{l} \tag{4.17}$$

$$A_L = \frac{L}{N^2} = \frac{\mu_0 \mu_r A}{l} \tag{4.18}$$

Powder cores are used in the design of converter side inductor. An E-shaped powder core is also used in this study. DC bias curve of the core material is provided by the manufacturer [63]. Equation (4.19) gives the linear approximation of the DC bias performance of the core material. Depending on the inductance requirement of the application, number of turns is determined, and nominal inductance value is estimated for one core. Then, inductance value can be increased by stacking more cores.

$$A_L \left(\frac{nH}{Turns^2}\right) = -0.019 * NI + 108 \tag{4.19}$$

4.2.3.2. Copper Losses

Copper losses are simply the resistive losses in the windings of the inductor. For fundamental frequency components, copper loss calculations are quite straightforward as AC resistance can be accepted as equal to DC resistance at 50 Hz frequency. However, converter side inductor current includes high frequency PWM components at switching frequency. Skin effect and proximity effect should be taken into account calculating the copper losses due to high frequency components.

While DC current is expected to flow uniformly in a conductor, current density increases towards the surface of a conductor as frequency increases. This is called skin effect and the measure of how closely current flows to the surface of inductor is called skin depth. Equation (4.20) provides the skin depth value as a function of frequency and **Table 4.2** provides the skin depth values at different frequencies. If used foil in the inductor winding is thicker than the skin depth at corresponding frequency, current cannot use the whole conductor cross-section and AC equivalent resistance of the conductor is higher than its DC resistance in this case.

$$\delta = \sqrt{\frac{\rho}{\pi * f * \mu_r * \mu_0}} \tag{4.20}$$

Table 4.2 Skin depth values for copper at different frequencies

δ Calculation Parameters for Copper		**δ Values at Different Frequencies**	
Resistivity (ρ)	1.68 x 10^{-8} Ωm	8 kHz	0.729 mm
Relative Permeability (μ_r)	1	16 kHz	0.515 mm
Permeability of free space (μ_0)	4π x 10^{-7} Hm^{-1}	24 kHz	0.421 mm
		32 kHz	0.364 mm
		48 kHz	0.298 mm

A copper foil with 0.3 mm thickness is used in this study so skin depth does not create a problem till 48 kHz switching frequency. However, proximity effect must also be taken into account in copper loss calculations. Current components in each turn of a winding induce "parasitic" current components in adjacent conductors in the structure of a foil winding and cause additional losses. This is called "proximity effect". Dowell's equation can be used to estimate the AC resistance of a winding. Jimenez presented a good method to calculate the AC equivalent resistance of a foil inductor [64]. According to his thesis, ratio of AC resistance to DC resistance can be calculated with the equations (4.21) – (4.26).

$$n_w = \frac{h_w}{h_c} \tag{4.21}$$

$$\Delta = \frac{d_w}{\delta} \tag{4.22}$$

$$\Delta' = \sqrt{n_w} * \Delta \tag{4.23}$$

$$c_1 = \frac{sinh(2\Delta') + sin(2\Delta')}{cosh(2\Delta') - cos(2\Delta')} \tag{4.24}$$

$$c_2 = \frac{sinh(\Delta') - sin(\Delta')}{cosh(\Delta') + cos(\Delta')} \tag{4.25}$$

$$\frac{R_{ac}}{R_{dc}} = \Delta' * \left[c_1 + c_2 * n_w^2 * \frac{2}{3} * (N^2 - 1)\right] \tag{4.26}$$

Δ is named as penetration ratio and it is defined by the ratio of the foil thickness (d_w) to the skin depth (δ). n_w is named as porosity factor and defined by the ratio of layer width (h_w) to the core window size (h_c). Number of turns is denoted by N as usual. Using porosity factor, altered penetration ratio (Δ') is calculated. In calculation of AC resistance to DC resistance ratio, altered penetration ratio is used.

The copper losses of an inductor can be calculated using the equation (4.27).

$$P_{copper} = I_{fundamental}^2 * R_{dc} + I_{PWM}^2 * R_{ac} \quad (4.27)$$

4.2.3.3. Core Losses

Core losses can be calculated using the equation (4.28). The coefficients a, b and c are determined according to core type and frequency. B denotes the half of the peak to peak magnetic flux and f denotes the frequency. Equations (4.29) – (4.31) and DC magnetization curve of the core material is used to calculate B value.

$$P = aB^b f^c \quad (4.28)$$

$$B = \frac{B_{ACmax} - B_{ACmin}}{2} \quad (4.29)$$

$$H_{ACmax} = \left[\frac{N}{l} * \left(I_{DC} + \frac{\Delta I}{2}\right)\right] \rightarrow DC\ magnetization\ curve\ \rightarrow B_{ACmax} \quad (4.30)$$

$$H_{ACmin} = \left[\frac{N}{l} * \left(I_{DC} - \frac{\Delta I}{2}\right)\right] \rightarrow DC\ magnetization\ curve\ \rightarrow B_{ACmin} \quad (4.31)$$

In an inverter application, output current sinusoidally varies and converter side inductor current includes the switching frequency components as well as sinusoidally varying fundamental component. Thus, core loss calculations should be conducted for each PWM cycle in one fundamental cycle and total energy loss should be multiplied by fundamental frequency to estimate total core losses. However, variance of inductance with fundamental current should be also taken into account as it directly affects the peak to peak current ripple in each PWM cycle. A core loss calculation algorithm is developed taking these considerations into account. Developed core loss calculation algorithm is provided in **Figure 4.9**.

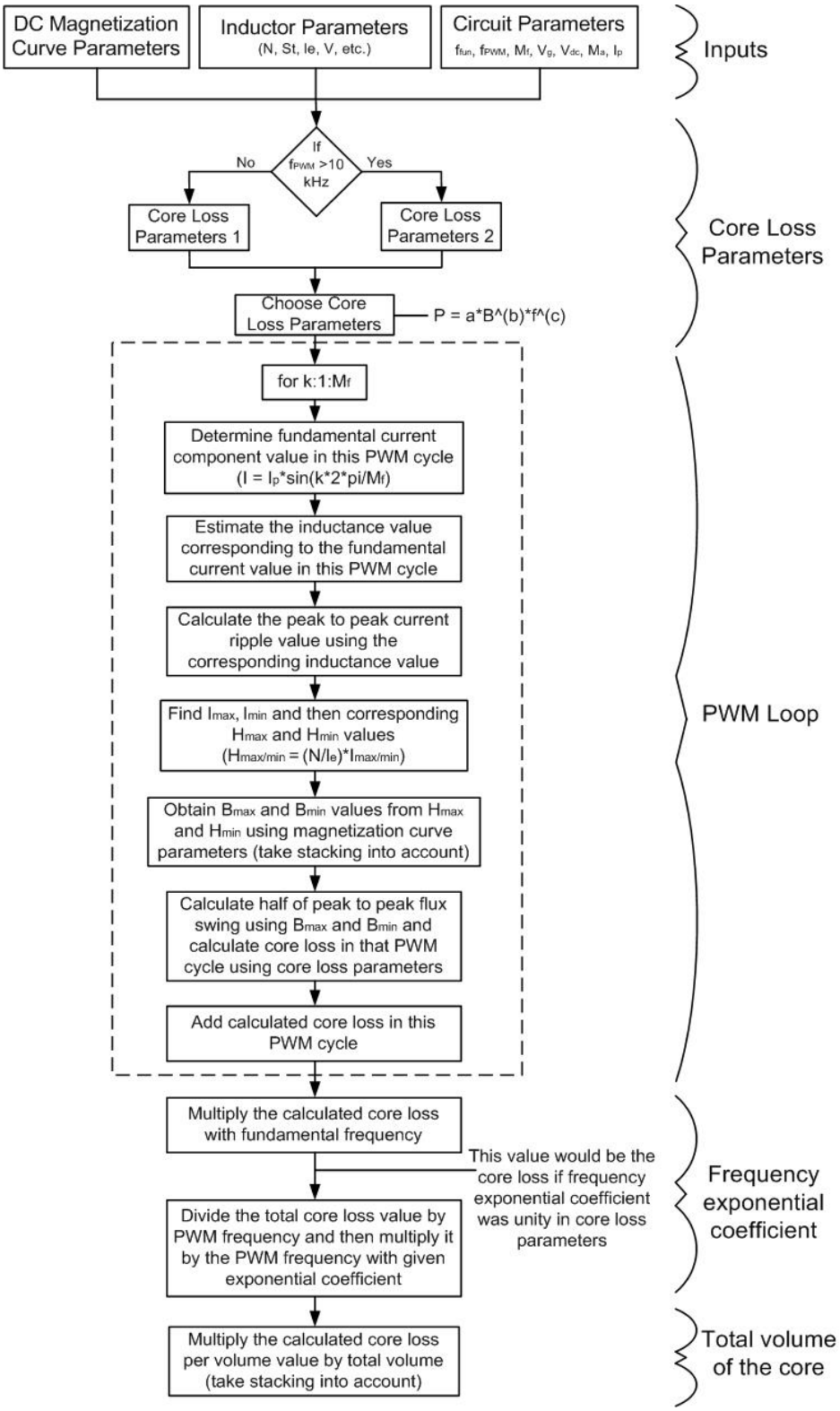


Figure 4.9 Developed loss calculation algorithm.

4.3. Reference Design

As mentioned in the beginning of this chapter, a reference VSC design with Si-IGBT module is provided first in this study and then progressive design cases with H-IGBT and SiC-MOSFET modules are given. Design specifications are already provided in **Table 4.1**. VSC topology and progressive VSC design cases are shown in **Figure 4.10**.

Reference design is conducted according to the design methodology which is presented earlier in this chapter. First, semiconductor losses vs switching frequency plots are obtained at certain conditions and a suitable switching frequency is selected. Then, heatsink sizing is completed. Finally, sizing of filter inductors is completed, and efficiency calculations are conducted.

Figure 4.11 shows the semiconductor losses vs switching frequency plots for Si-IGBT, H-IGBT, and SiC-MOSFET modules. Although the boost converter is beyond the scope of this study, boost converter losses with each semiconductor module is also given in **Figure 4.11**. As clearly seen, SiC-MOSFET and H-IGBT modules have a superior performance in terms of losses with increasing f_{sw}. Si-IGBT module transistor and diode exceed the maximum junction temperature limit in the VSC and boost converter applications respectively once f_{sw} exceeds 24 kHz.

In order to meet the efficiency criteria, switching frequency is selected as 8 kHz for reference design with Si-IGBT module. Semiconductor losses are calculated as 520 W at rated power (30 kW) at 8 kHz if heatsink temperature is kept at 80 °C.

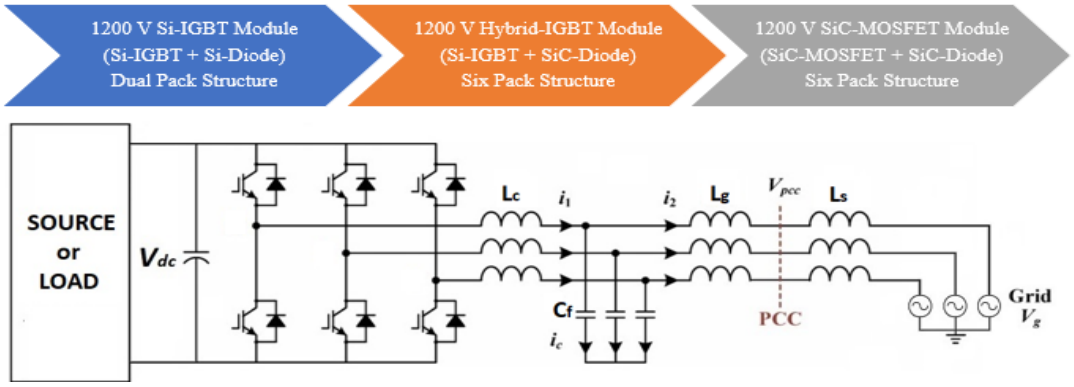


Figure 4.10 VSC structure and progressive VSC design cases.

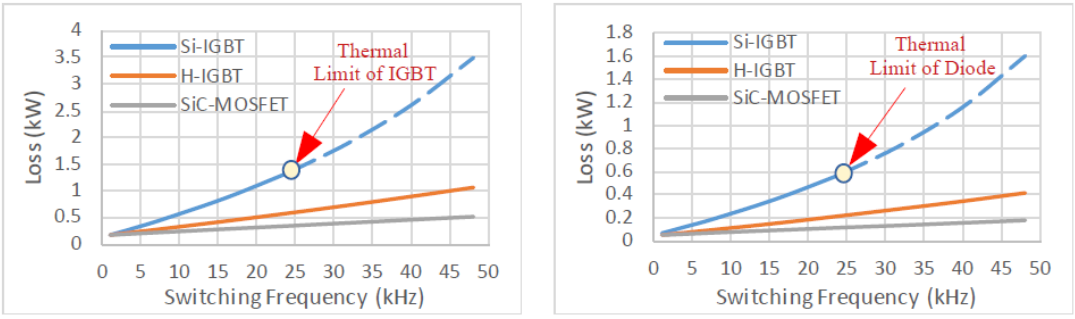


Figure 4.11 Semiconductor losses vs switching frequency for VSC (left) and boost converter (right).

After determining switching frequency, heatsink sizing is completed according to the calculated semiconductor losses. Dimension definitions of the heatsink are shown in **Figure 4.12** [62]. In reference design, fin thickness and distance between fins are determined as 2 mm and 4 mm, respectively. Height is chosen as 72 mm and base thickness is determined as 22 mm (fin height is 50 mm). Heatsink length (fin length) in airflow direction is set as 135 mm. With the same cooling system, the number of fins (N_f) can be decreased/increased without changing the other dimensions according to the required thermal resistance value. The total width of the heatsink can be calculated as N_f x 6 mm.

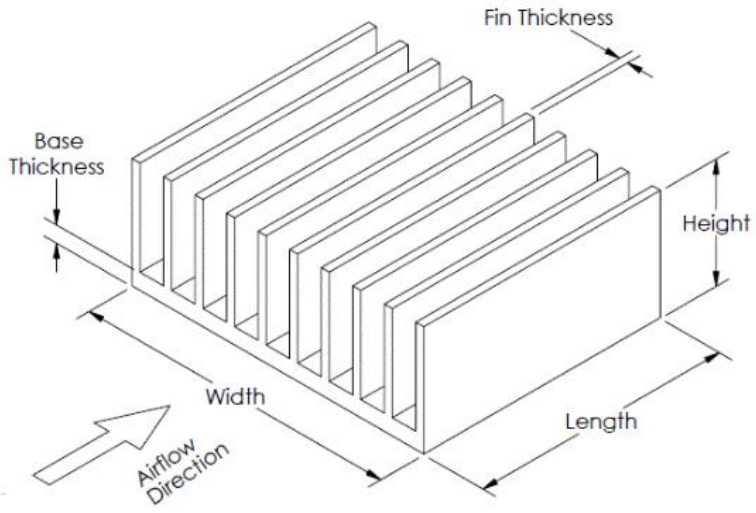


Figure 4.12 Dimension definitions of the stacked-fin heatsink [62].

Two axial fans (SA155055) are operated parallel for cooling [61]. The pressure vs airflow characteristics of the fan and heatsink system are given in **Figure 4.13 (a)**. As seen, the operating point of this system corresponds to the air flow rate of 68.98 CFM. Now thermal resistance of the heatsink can also be found. **Figure 4.13 (b)** shows the corresponding thermal resistance value of the heatsink as 0.0718 K/W [62].

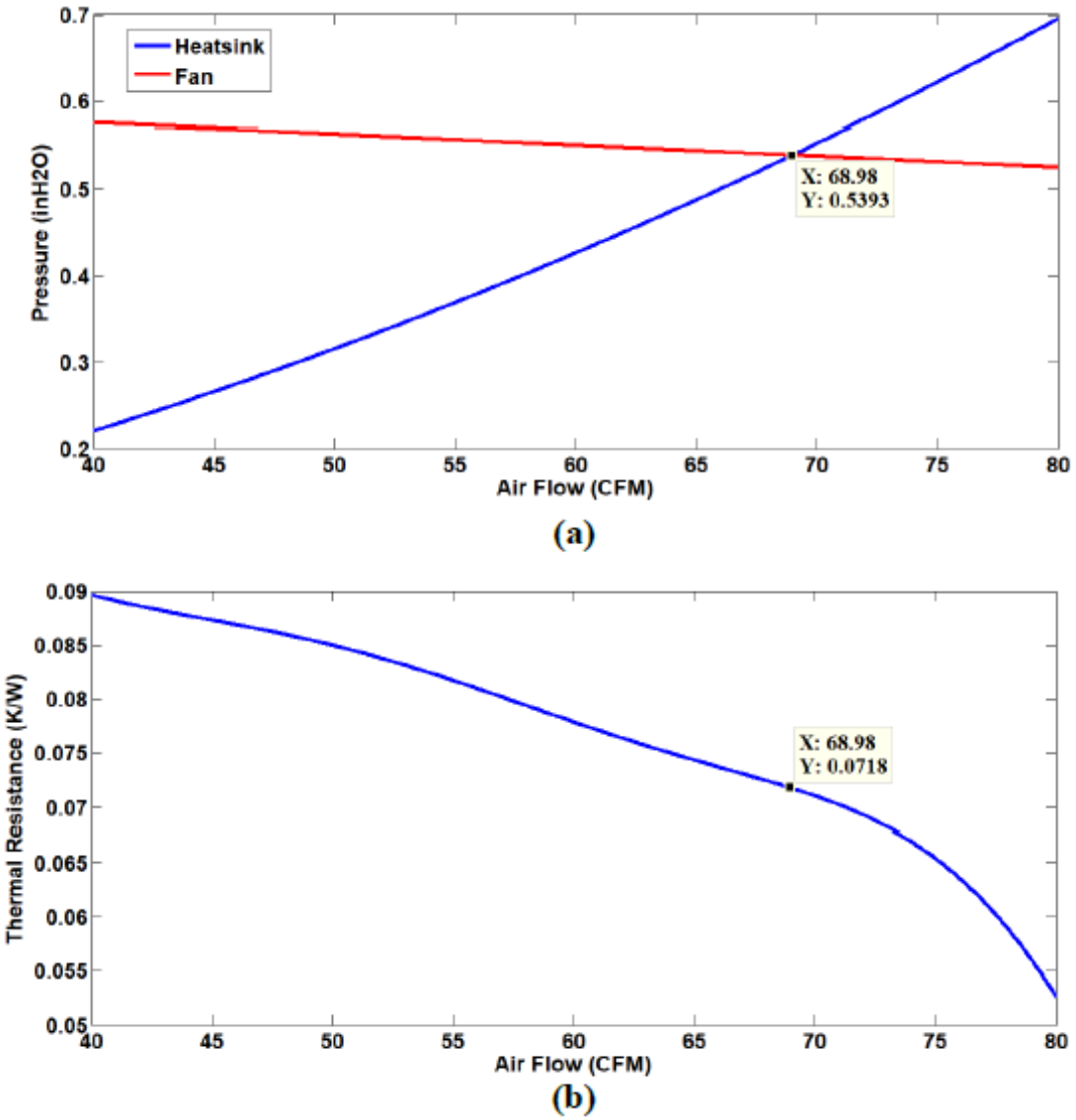


Figure 4.13 (a) Pressure vs air flow characteristics of heatsink and fan. (b) Thermal resistance vs air flow characteristics of the heatsink.

Theoretical calculations show that thermal resistance value is 0.0718 K/W with this heatsink and fan system. Of course, thermal resistance is expected to be higher in practice because heatsink surface is not fully utilized by semiconductor modules and there is always a finite amount of air flow leakage between fans and heatsink. As shown later in this chapter, thermal resistance is measured very close to 0.077 K/W in the experiments. However, the difference between calculated and measured thermal resistance is less than 10% and this error rate is acceptable in thermal analysis.

In determination of LCL filter parameters, converter side inductor has priority as it determines the peak to peak current ripple at converter output. In half-bridge topology with SPWM, the maximum peak to peak current ripple occurs at zero-crossings of the grid voltage in unity power factor operation. Equation (4.32) gives the maximum peak to peak current ripple magnitude. Based on design experience, the maximum limit for the peak to peak current ripple magnitude is set as 50% of the peak value of the fundamental current at converter output. Fundamental rms current is 43.48 A in this application and peak current value is 61.48 A. Thus, maximum allowed peak to peak current ripple magnitude shall be less than 30.74 A and this value corresponds to a minimum inductance value of 762 μH. In this study, converter side inductance is value is set as 800 μH.

Usually converter side inductance to grid side inductance ratio is determined as somewhere between 2 and 1. This ratio is determined as 2 in this study and grid side inductance is determined as 400 μH. In fact, leakage inductance of the distribution transformer also contributes the grid side inductance. A 1250-kVA transformer, which is commonly used in MW-scale PV power plants, with 10% leakage inductance has approximately 40 μH and it also contributes to the grid-side inductance in practice.

$$\Delta I_{pp} = {}^{V_{dc}}/_{4f_{sw}L} \tag{4.32}$$

In terms of reactive power considerations at fundamental frequency, filter capacitor is expected to be lower than 5%. At 30-kVA and 400-V line to line grid voltage, base impedance is calculated as 5.33 Ω. Base inductance and base capacitance values at

fundamental frequency are calculated as approximately 16.97 mH and 597 μF. Thus, filter capacitor capacitance should be smaller than 29.85 μF and it is determined as 25 μF. In these conditions, filter inductors and filter capacitance are determined as 7.07% and 4.18% respectively.

Design parameters are given in **Table 4.3** for the reference design.

Table 4.3 Design parameters for the reference design

DC Bus Voltage (V_{DC})	750 V DC
Grid Voltage (line to line)	400 V AC
Grid Frequency (f_g)	50 Hz
Sampling Frequency (f_s)	8 kHz
Switching Frequency (f_{sw})	8 kHz
Converter Side Inductance (L_c)	800 μH (4.71%)
Grid Side Inductance (L_g)	400 μH (2.36%)
Filter Capacitance (C_f)	25 μF (4.18%)
Corner Frequency (L_c - C_f)	1125.4 Hz
LCL Parallel Corner Frequency	1949.2 Hz

4.3.1. Simulation Results

In order to provide proof of concept, first computer simulations are used to show that a VSC system operates stable with the given parameters in **Table 4.1**. As powder cores are used in the study, variation of nominal inductance value of the inductors with current is also modelled in the simulations. The nominal inductance value of converter side inductance is assumed to vary between 600 μH and 800 μH with fundamental current component. Similarly, grid side inductance is also assumed to vary between 300 μH and 400 μH. In this way, peak to peak PWM current ripple value can be shown in a more realistic way in converter current and capacitor current. **Figure 4.14** – **Figure 4.15** shows the waveforms of grid voltage (E_s), grid current (i_g), converter current (i_c), capacitor voltage (V_{cf}) and capacitor current (i_{cf}). In addition, variation of converter side and grid side inductances (L_c and L_g) with respect to the grid current (i_g) are also shown.

As seen in the waveforms, inductance value decreases as current increases. That is why total inductance value takes its minimum value at the peak points of the current [68]. As clearly seen in grid current waveform in **Figure 4.14**, system is less stable in these points and small oscillations start in grid current. A more stable operation can be achieved by decreasing the proportional gain value in the current controller, but this decreases the control bandwidth. It is a proper design know-how to keep the proportional gain as high as possible to achieve higher control bandwidth. In this study, proportional gain is adjusted in such a way that (K_p = 5.5) a further increase in it may significantly distort the grid current waveform at peak points. THD value of the grid current is calculated as 1.775% and this value is within the acceptable limits.

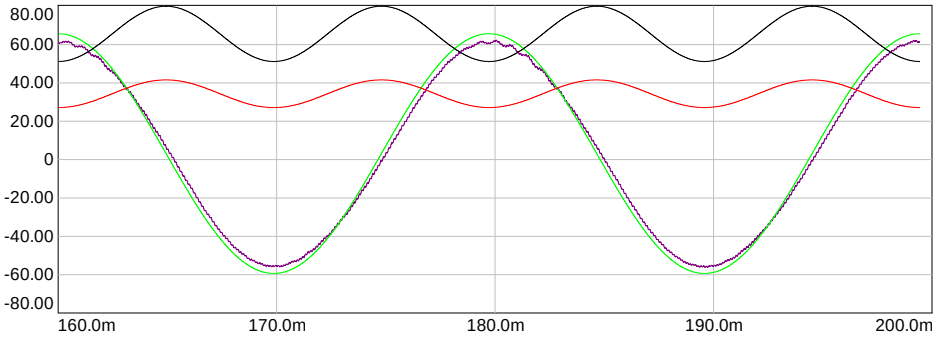


Figure 4.14 Steady state simulation of reference design at full-load including inductance variance with fundamental current component.
E_s (green, scaled by 0.2), i_g (violet), L_c (black, scaled by 100k), L_g (red, scaled by 100k) waveforms.

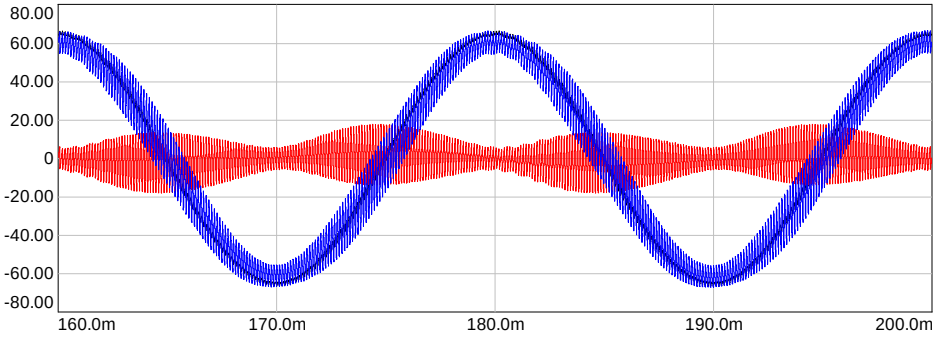


Figure 4.15 Steady state simulation of reference design at full-load.
V_{cf} (black, scaled by 0.2), i_c (blue), i_{cf} (red).

4.3.2. Experiment Setup and Test Results

In addition to simulation results, experiments are also conducted to verify the reference design of grid-connected VSC. A grid-connected PWM-rectifier (60-kW rated power) is used to form DC bus voltage for the grid-connected PWM-VSC to be tested. An isolation transformer is used at the input of this PWM rectifier. Grid-tied VSC converts DC to AC and injects power to the AC grid in synchronization with grid voltage. Measurements are taken from both DC side and AC side of the grid to conduct efficiency calculations. A diagram of the experiment setup is shown in **Figure 4.16**. In this configuration, electricity consumption is also minimized because the power that PWM rectifier draws from grid is eventually given back to the grid by the tested grid-connected PWM-VSC. Only the losses of isolation transformer, PWM rectifier and grid-connected PWM-VSC is consumed.

A power analyzer is used to measure current and voltage at the output of grid-connected PWM-VSC. Input DC voltage is measured with a multimeter and input DC current is measured with a clamp-ammeter. Measurement devices that are used in the experiments is given in **Table 4.4**.

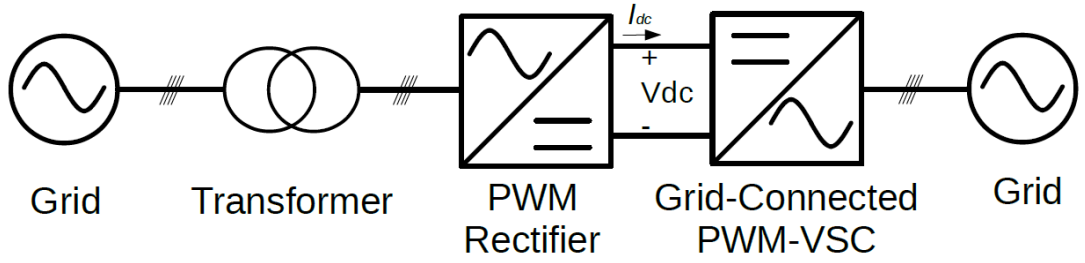


Figure 4.16 Experiment setup diagram.

Table 4.4 Measurement devices

Measured Quantity	Measurement Device	Accuracy
DC Voltage	Fluke 87V Industrial Multimeter	±0.05%
DC Current	Fluke 325 True-RMS Clamp Meter	±2%
AC Voltage	Fluke 434 Series II Energy Analyzer	±0.2%
AC Current	Fluke 434 Series II Energy Analyzer (i430-Flex 10x)	±0.5%

Photos of measurement devices are provided in **Figure 4.17**. **Figure 4.18 (a)** shows the grid-connected PWM-VSC itself and **Figure 4.18 (b)** shows the whole experiment setup.

Gate resistance significantly affects the switching losses. Increasing gate resistance slows the switching of the semiconductors (lower dV/dt and dI/dt rate) and increases the switching losses. However, this method reduces possible EMI problems. In case of a limited layout quality, it is a common practice to use higher gate resistance than recommended value. **Table 4.5** provides the used gate resistance values in the experiments with different semiconductor modules.

Experimental waveforms of phase current and phase voltage from energy analyzer screen are also provided in **Figure 4.19** for half-load and full-load operation. As also observed in the simulation results, current waveform is slightly distorted when it reaches its peak values at full-load operation. It is because the inductance of powder core inductors reaches its minimum value at these points as explained earlier.

Table 4.5 Gate resistance values used in the experiments

Semiconductor Module	Internal Gate Resistance	Additional Gate Resistance
Si-IGBT Module	5 Ω	5 Ω
H-IGBT Module	5 Ω	5 Ω
SiC-MOSFET Module	4 Ω	4 Ω

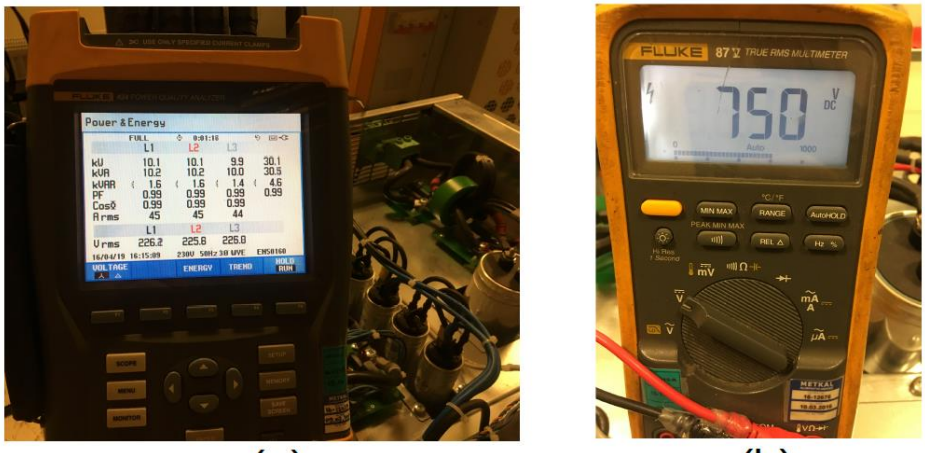
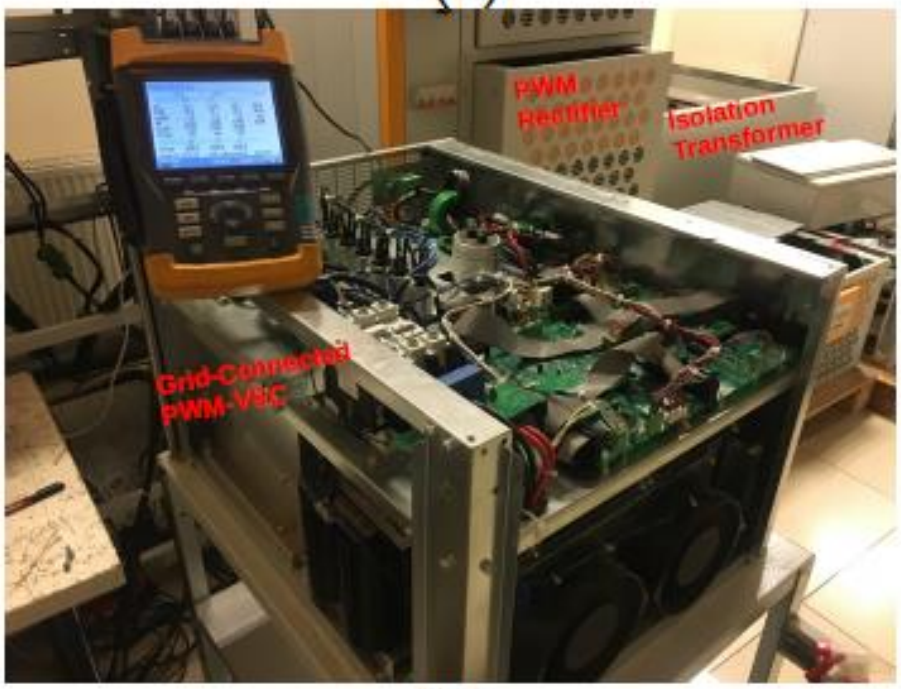


Figure 4.17 Photos of measurement devices. (a) Power analyzer. (b) Multimeter.

(a)



(b)

Figure 4.18 Experiment setup photos. (a) VSC. (b) Experiment setup.

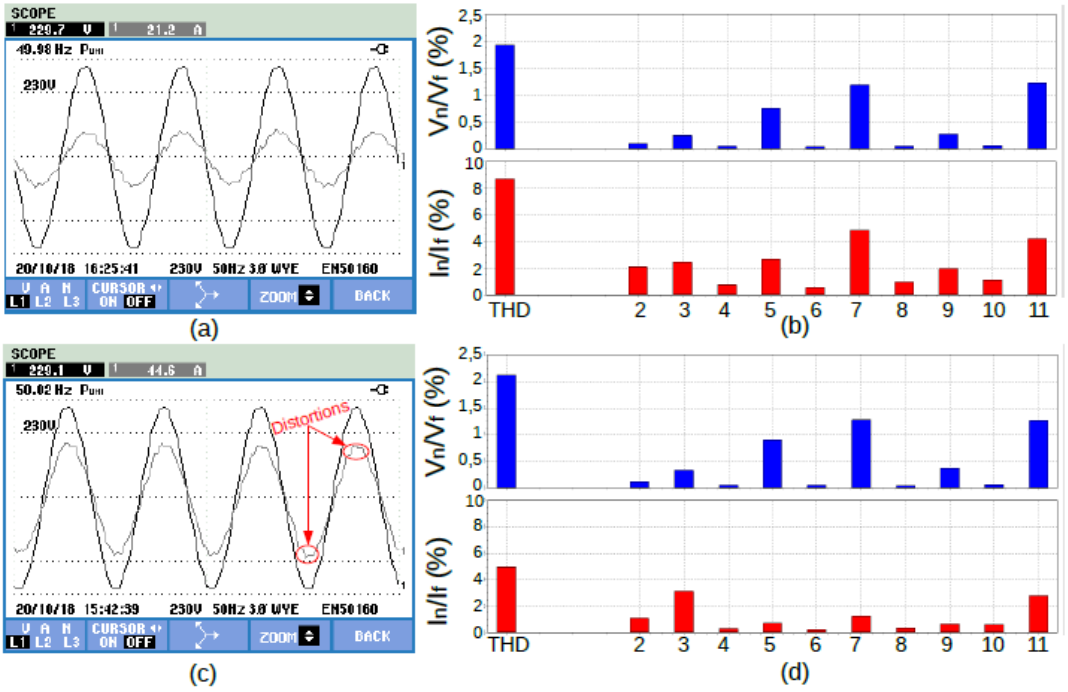


Figure 4.19 Experimental phase voltage and current waveforms and harmonic spectrums.
(a) Phase voltage and current waveforms for half-load.
(b) Phase voltage and current harmonic spectrums for half-load.
(c) Phase voltage and current waveforms for full-load.
(d) Phase voltage and current harmonic spectrums for full-load.

In addition to the experimental waveforms, **Figure 4.19** also shows the measured harmonic spectrums of phase voltage and current for half-load and full-load conditions. However, as the harmonic components are shown as percent of fundamental component in **Figure 4.19**, harmonic current components at half-load seem larger than full-load condition. It is because fundamental component is at only half of its rated value in half-load conditions. In order to make a more comprehensive analysis, harmonic components should be expressed with their absolute magnitudes instead of percent of fundamental component.

Figure 4.20 presents the harmonic spectrums of phase voltage and current with their RMS magnitudes. As clearly seen, 3rd, 7th, and 11th current harmonic components significantly increase in full-load conditions. As total inductance value reduces to its minimum value at peak points of fundamental current in full-load conditions,

harmonic components in low frequency region become more dominant in current harmonic spectrum. In commercial products, the low frequency harmonic components can be prevented with using proportional resonant controllers as mentioned before. By using parallel resonant controllers which are tuned to 150 Hz, 250 Hz, 350 Hz, 450 Hz and 550 Hz, low frequency harmonic components (3^{rd}, 5^{th}, 7^{th}, 9^{th}, and 11^{th} components) can be easily mitigated [67].

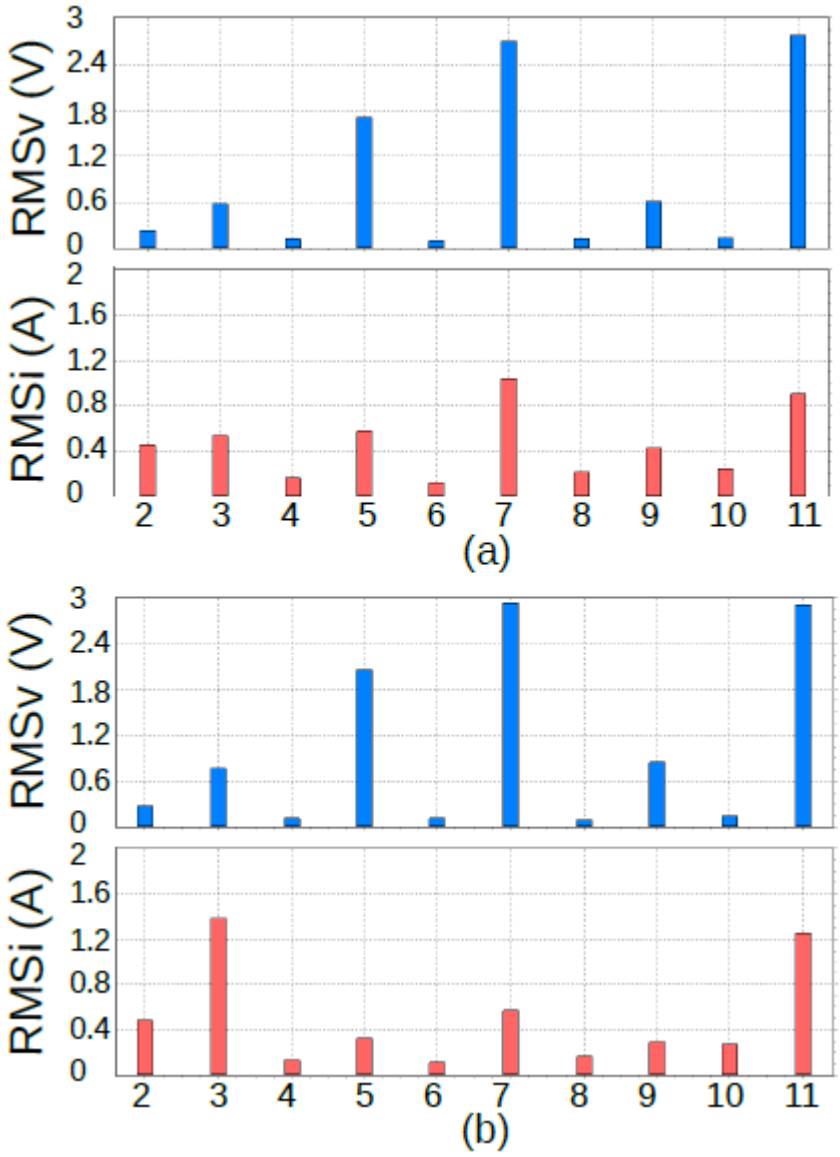


Figure 4.20 Voltage and current harmonic spectrums of experimental measurements. (a) Half-load. (b) Full-load.

4.4. Scalability and Design Expansions

4.4.1. Scalability of the Heatsink and Inductors

In reference design, both heatsink, and inductors are chosen with scalable structures. In this way they can be easily scaled up or down in progressive VSC design cases with varying switching frequency.

Heatsink is determined as stacked-fin structure as shown in **Figure 4.21**. Extruded aluminum fins can be stacked together and compressed from both sides. Fin number can be increased or decreased according to the semiconductor losses and heatsink thermal resistance requirement.

Similarly, inductors are also determined in a scalable structure. Stacked E-shaped powder cores are used in inductor structure and inductance can be varied by increasing or decreasing number of stacks or number of turns. A 5-stack and a 2-stack inductor are shown in **Figure 4.22**. Again, inductance can be easily scaled too with varying switching frequency in progressive design cases.

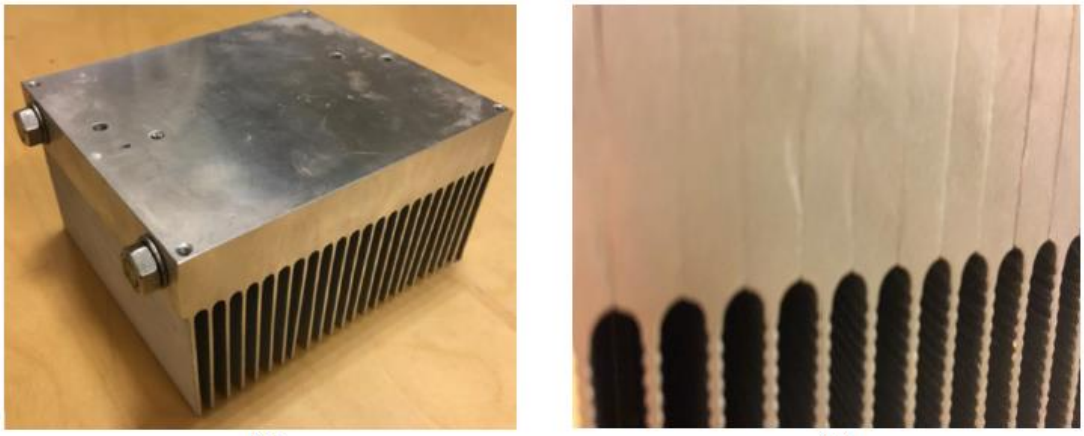


Figure 4.21 (a) Stacked fin heatsink structure. (b) Stacked-fins.

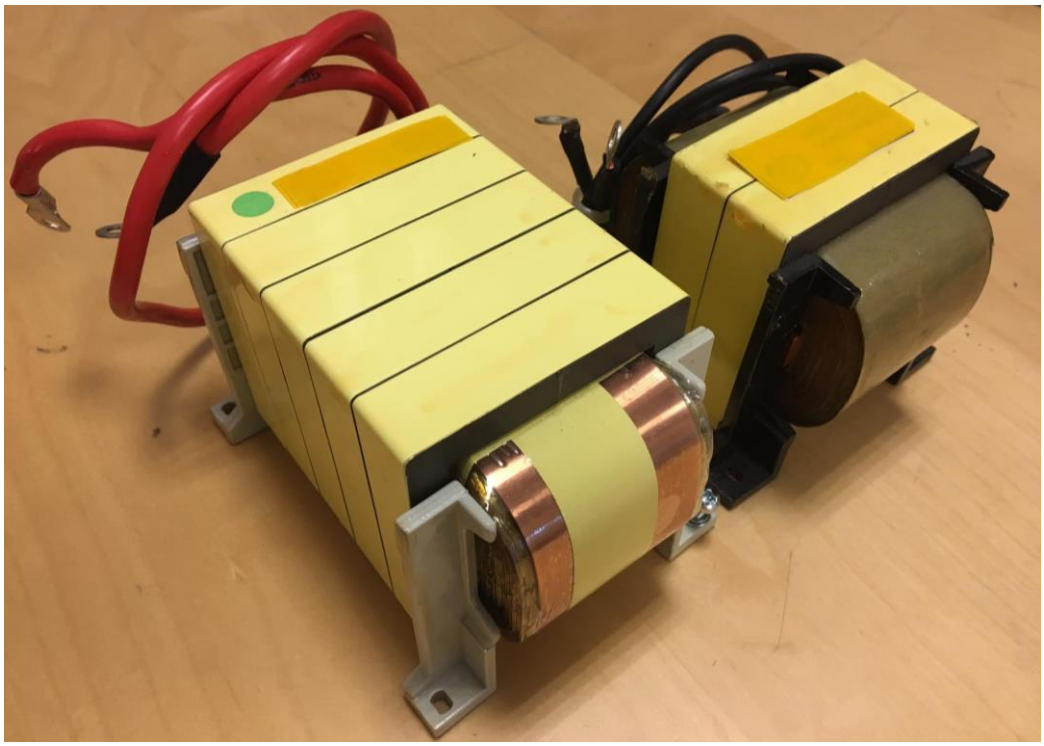


Figure 4.22 Inductors with 5 and 2 stacked E-cores.

4.4.2. Designing with Constant Switching Frequency and Inductance Product (f_{sw}*L=Constant)

Peak to peak current ripple at converter output is kept constant in progressive VSC design cases. This is only possible by keeping the switching frequency times converter side inductance product constant in all cases. This approach allows a fair comparison between the design cases in terms of inductor sizing. **Figure 4.23** shows a demonstration of this approach. When switching frequency is increased to 16 kHz from 8 kHz, peak to peak current ripple magnitude reduces to half of its original value. However, in order to keep the peak to peak current ripple magnitude same, converter side inductance must be reduced to 400 µH from 800 µH when switching frequency increases to 16 kHz from 8 kHz.

As peak to peak current ripple is kept same in design cases, filter capacitance is not changed. Thus, effect of filter capacitance on cost of the VSC is also kept beyond the scope of this study.

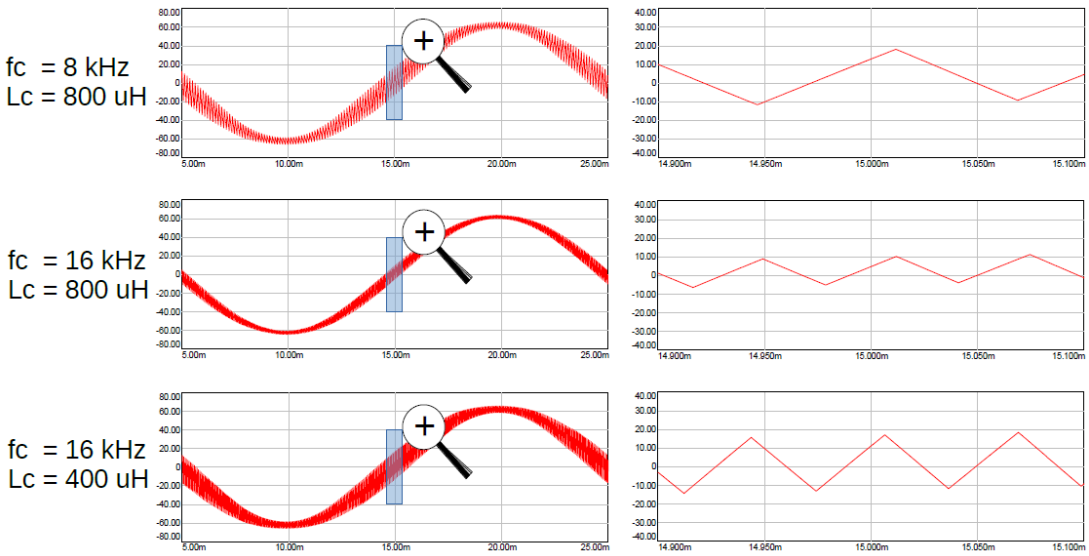


Figure 4.23 Demonstration of switching frequency and converter side inductance relation.

4.5. Progressive VSC Design Cases

The four progressive VSC design cases of this study are summarized in **Table 4.6**. In the first case, a standard Si-IGBT VSC is taken as reference and only the semiconductor module is changed without any change in f_{sw}, heatsink design, and LCL parameters. In the second case, the heatsink structure is optimized for the H-IGBT and SiC-MOSFET modules for again the same f_{sw} such that the rated heatsink temperature is kept at 80 ˚C (Case-1 Si-IGBT rated temperature at rated power). In the third and fourth cases, the inductor size is reduced with the increasing f_{sw} such that the PWM ripple current is kept the same as in the first and second cases. In the third case, the f_{sw} is increased and inductor size is reduced for the H-IGBT and SiC-MOSFET modules with same heatsink as in case 1. In fourth case, f_{sw} is increased aggressively to reduce the size of inductors as much as possible. However, f_{sw} of SiC-MOSFET module is not increased beyond 48 kHz to keep third harmonic of f_{sw} below 150 kHz for EMC considerations.

Note that although absolute maximum junction temperature of SiC-MOSFET is higher compared to Si-IGBT devices due to superior thermal performance of SiC, heatsink

temperature is not further increased as the high temperature of heatsink may affect the lifetime of other components such as electrolytic dc link capacitors in VSC structure. Also, the semiconductor package limits the absolute junction temperature. Absolute maximum junction temperature of SiC devices is expected to increase with developing package technology. In the four design cases, the f_{sw} value is increased in integer multiples of 8 kHz however, in later stages further optimization of f_{sw} will be discussed.

Table 4.6 Reference design and progressive VSC design cases

Cases	Property	Si-IGBT	H-IGBT	SiC-MOSFET	COMMENTS
1. Only semiconductor module is different among VSCs, same heatsink and LCL structure are used	f_{sw} (kHz)	8	8	8	Both experimental and calculated results. Efficiency improves and heatsink temperature drops with SiC and H-IGBT
	N_f	25	25	25	
	$R_{th\text{-}heatsink}$ (K/W)	0.077	0.077	0.077	
	$T_{heatsink\text{-}max}$ (°C)	80	62	57	
	L_c (µH)	800	800	800	
	L_g (µH)	400	400	400	
2. Heatsink size is reduced for H-IGBT and SiC-MOSFET modules	f_{sw} (kHz)	Case 1	8	8	Calculated results. 40% and 60% heatsink size reductions achieved with H-IGBT and SiC-MOSFET
	N_f	//	15	10	
	$R_{th\text{-}heatsink}$ (K/W)	//	0.135	0.170	
	$T_{heatsink\text{-}max}$ (°C)	//	80	80	
	L_c (µH)	//	800	800	
	L_g (µH)	//	400	400	
3. Heatsink as in Case 1, f_{sw} is increased and inductor size is reduced for H-IGBT and SiC-MOSFET modules	f_{sw} (kHz)	Case 1	16	32	Both experimental and calculated results. with H-IGBT and SiC modules 50% and 75% inductor size reductions achieved
	N_f	//	25	25	
	$R_{th\text{-}heatsink}$ (K/W)	//	0.077	0.077	
	$T_{heatsink\text{-}max}$ (°C)	//	74	72	
	L_c (µH)	//	400	200	
	L_g (µH)	//	200	100	
4. Heatsink as in Case 1, f_{sw} is aggressively increased to further reduce inductor size for H-IGBT and SiC-MOSFET modules	f_{sw} (kHz)	Case 1	24	48	Calculated results. 66% and 83% inductor size reductions achieved with H-IGBT and SiC modules
	N_f	//	25	25	
	$R_{th\text{-}heatsink}$ (K/W)	//	0.077	0.077	
	$T_{heatsink\text{-}max}$ (°C)	//	88	81	
	L_c (µH)	//	267	133	
	L_g (µH)	//	133	67	

4.5.1. Semiconductors

As mentioned earlier, 150-A dual-pack Si-IGBT module is selected in the design whereas H-IGBT and SiC-MOSFET modules are selected in 6-pack structure. While Si-IGB and H-IGBT modules are selected with 150-A rating, SiC-MOSFET modules is selected with 75-A rating. It is because MOSFET structure is different than IGBT structure and smaller die size can provide the same current capacity for SiC material compared to Si material. SiC prices are expected to fall down in the future and SiC-MOSFETs can be used in parallel-connected configurations for lower on-state losses in this case. Moreover, SiC-MOSFET package technology is also expected to develop and absolute maximum junction temperature of SiC-MOSFET devices is expected to further increase. Thus, smaller die size can provide the same current rating capacity for SiC-MOSFETs compared to Si-IGBTs.

Calculated semiconductor losses and heatsink temperatures are shown in **Figure 4.24**. As clearly seen in, H-IGBT and SiC-MOSFET modules significantly decrease the semiconductor losses and heatsink temperature in the first case where the switching frequency and heatsink structure are kept same. In the second case, where the heatsink design is enhanced for H-IGBT and SiC-MOSFET modules, heatsink temperature reaches 80 °C in all designs and semiconductor losses slightly increase for hybrid IGBT and SiC-MOSFET modules with increasing heatsink and junction temperature. In third and fourth steps, switching frequency is increased while keeping the heatsink design same as case 1 and consequently semiconductor losses increase for H- IGBT and SiC-MOSFET designs. While heatsink temperature stays below 80 °C in third case, it surpasses 80 °C for both H-IGBT and SiC-MOSFET design with aggressively increased switching frequency. As clearly seen, the H-IGBT module brings the advantage of reduced diode switching losses whereas SiC-MOSFET module further significantly reduces the transistor switching losses too.

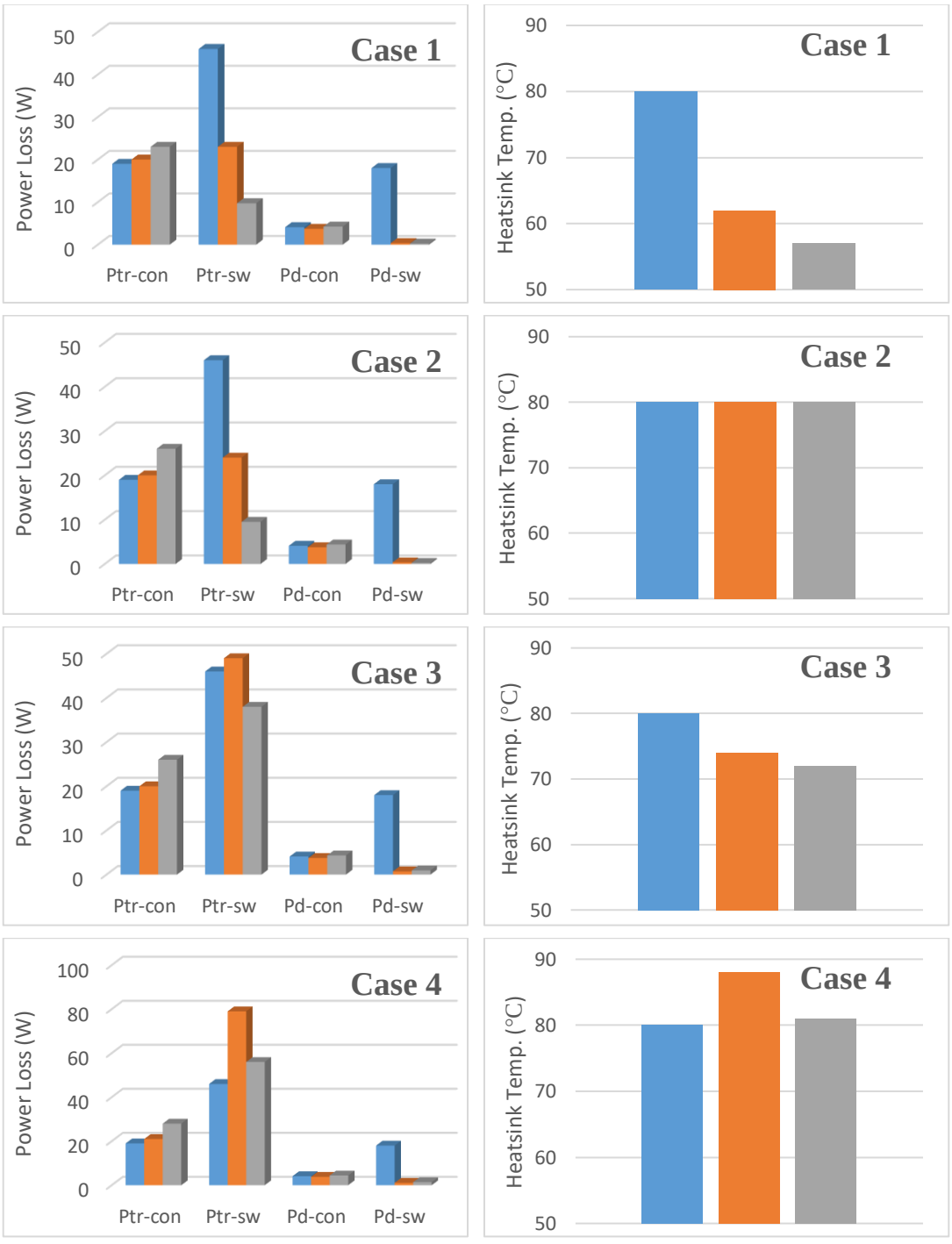


Figure 4.24 Calculated semiconductor losses and heatsink temperature values for all cases with Si-IGBT (blue), H-IGBT (Orange) and SiC-MOSFET (gray) modules.

4.5.2. Heatsink

With same fan system, heatsink structure is re-designed in the second case for H-IGBT and SiC-MOSFET module designs. In this case, switching frequency is kept constant and heatsink thermal resistance is adjusted in a way that at rated power, heatsink temperature becomes 80 °C. Loss calculation algorithm is used to find the required thermal resistance values for 80 °C heatsink temperature for H-IGBT and SiC-MOSFET module designs. After various attempts, it is found that 0.135 K/W and 0.170 K/W thermal resistance values satisfy the 80 °C heatsink temperature condition at rated power according to the equation (4.12).

After determining the required thermal resistance values, heatsink number of fins is changed to find the correct configuration which satisfies the calculated thermal resistance values. Length, fin thickness and distance between fins dimensions are not changed. Number of fins is determined as 15 and 10 for 0.135 K/W and 0.170 K/W thermal resistance values respectively.

4.5.3. LCL Filter Components

Sendust made stacked powder cores are used in the converter side inductors as the converter current includes high frequency PWM ripple components and it is common to utilize them for the 30-kW power ratings. However, low frequency cores with lower cost are better option for grid side inductors as grid current has negligible amount of f_{sw} components. Converter side inductor designs are completed with stacked E-shaped cores and 0.3 mm Cu foil is used in winding structures. In this structure, the inductance value approximately increases linearly with stacked core count. Thus, inductance values in **Table 4.6** can be realized. With 0.3 mm thickness Cu foil windings and given f_{sw} values, the skin and proximity effects are calculated and taken into account. As mentioned, the converter side inductor is designed such that $L \times f_{sw}$ product remains same in every design case. Thus, the peak to peak current ripple is kept constant at the VSC output and LCL filter capacitor is not changed in different design cases.

Powder cores are used in the design of converter side inductor. An E-shaped powder core is also used in this study. Depending on the inductance requirement of the application, number of turns is determined, and nominal inductance value is estimated for one core. Then, inductance value can be increased by stacking more cores. Number of turns is limited by the window area of the core. In this study, copper foil with 0.3 mm thickness is used in the windings and it is not possible to fit more than 50 turns into the core with this foil structure.

Conducted inductor designs for cases with different switching frequencies are provided in **Table 4.7**.

Approximated resistance values for the copper losses are calculated for each inductor set for both fundamental current component and high frequency switching component. Note that resistance at fundamental frequency 50 Hz is assumed to be equal to DC resistance and winding resistance of the grid side inductor is also included in this value. High frequency resistance of the converter side inductor is calculated using the equation (4.26). As switching frequency increases, proximity effect becomes more dominant and copper losses of high frequency components dramatically increase. However, it is worth to note that the rms value of high frequency current components is less than 10% of the rms value of fundamental current component in this study, thus they do not make a significant contribution to the copper losses.

For core loss calculation, equation (4.28) is used. For Kool Mμ 26μ cores; a, b and c coefficients are given as 45.48, 1.774 and 1.46 for frequencies higher than 10 kHz and 170.17, 1.774 and 1.03 for frequencies lower than 10 kHz [63].

Total inductor losses (including both core and copper losses) vs switching frequency characteristics are given in **Figure 4.25**. As switching frequency increases, stack number and number of turns decrease. This substantially decreases the core and copper losses. So as expected, total inductor losses also decrease with increasing switching frequency in this study.

Table 4.7 Converter side inductor designs

Switching Frequency (f_{sw})	Minimum Required Inductance	Stack Number	Number of Turns (N)	Inductance (At 0 A)
8 kHz	800 µH	5	38	780 µH
10 kHz	640 µH	4	38	624 µH
12 kHz	533 µH	4	35	530 µH
14 kHz	457 µH	3	38	467 µH
16 kHz	400 µH	3	35	396 µH
18 kHz	355 µH	3	33	352 µH
20 kHz	320 µH	2	38	311 µH
22 kHz	290 µH	2	36	279 µH
24 kHz	267 µH	2	35	264 µH
26 kHz	246 µH	2	34	249 µH
28 kHz	228 µH	2	33	235 µH
30 kHz	213 µH	2	32	221 µH
32 kHz	200 µH	2	31	207 µH
48 kHz	133 µH	2	25	135 µH

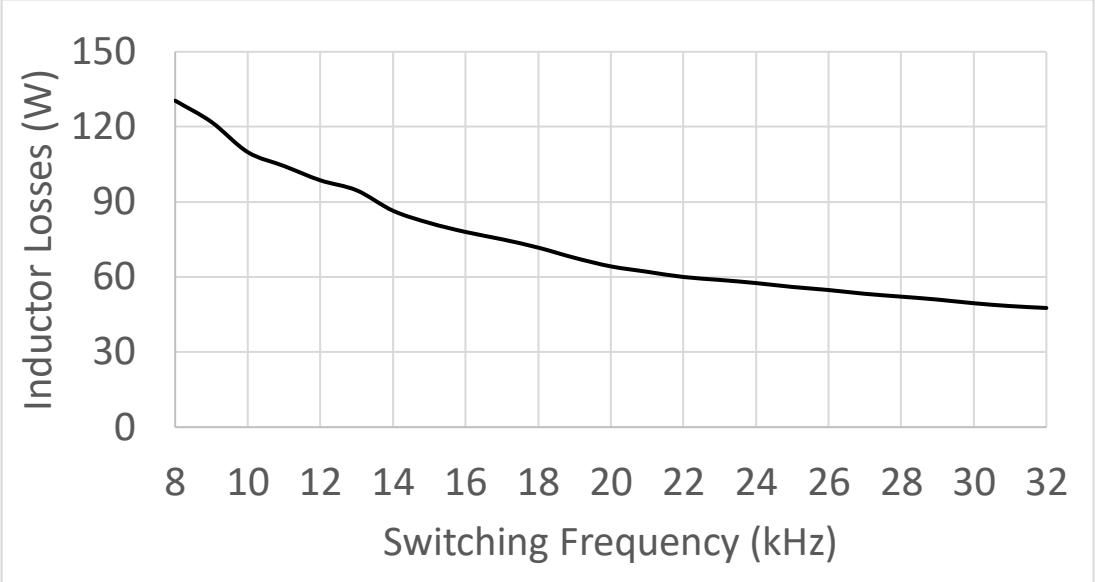


Figure 4.25 Total inductor losses vs switching frequency.

4.5.4. Further Design Optimization

Four progressive design cases are introduced as shown in **Table 4.6**. However, switching frequency is determined as only integer multiples of 8 kHz in these design cases (8 kHz, 16 kHz, 24 kHz, 32 kHz and 48 kHz). However, an optimum design point in terms of economic considerations may lie somewhere between integer multiples of 8 kHz. Determining the optimum point is only possible after evaluating the trade-offs between efficiency, heatsink cost and inductor cost w.r.t. the increasing switching frequency. As switching frequency increases, inductor losses decrease, and semiconductor losses increase while the latter is dominant. However, inductor cost decreases too. Thus, there is supposed to be a cost – efficiency point which provides the optimum design solution in terms of economic considerations. This analysis is conducted in Chapter 5 where differential cost approach between the designs is introduced and economic criteria such as return on investment and payback period are evaluated in different conditions.

4.6. Efficiency

4.6.1. VSC Design Case Efficiency Curves

In a grid-connected VSC, the main losses are; semiconductor losses, inductor losses (core and ohmic), capacitor ESR losses, and power supply unit consumption (feeding fans, relays, sensors, processors, gate drives etc.). The power supply unit consumption is measured in the lab as 80 W. Semiconductor losses are calculated with a developed loss calculation algorithm for the two-level VSC. Similarly, inductor losses are also calculated using a developed algorithm for both core and copper losses.

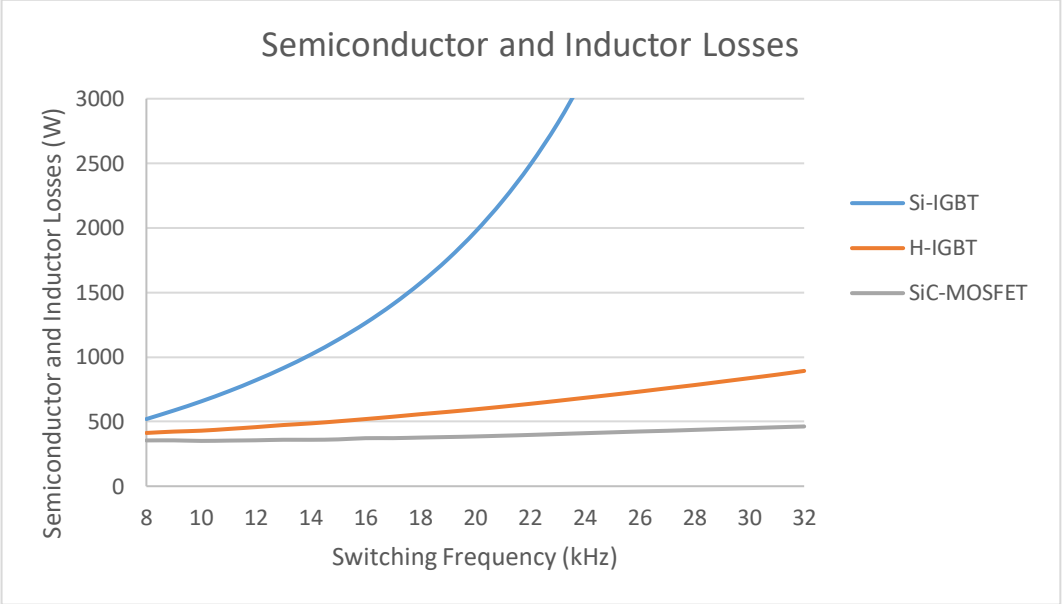


Figure 4.26 Total semiconductor and inductor losses vs switching frequency.

As semiconductor and inductor losses are the dominant components in total losses in a VSC, total semiconductor and inductor losses are plotted w.r.t. the switching frequency as shown in **Figure 4.26**. Although inductor losses decrease with increasing switching frequency (**Figure 4.25**), total amount of losses increase with increasing switching frequency because semiconductor losses are more dominant than inductor losses. However, the increase of total amount of losses exponentially increases in Si-IGBT design whereas the total loss plots have more linear characteristics for H-IGBT and SiC-MOSFET designs. For SiC-MOSFET module case, total amount of losses is almost flat because a significant portion of increase in semiconductor losses is compensated by decrease in inductor losses with increasing switching frequency.

In addition to inductor losses and semiconductor losses, capacitor losses are also taken into account. As PWM ripple is kept constant in all cases, LCL filter capacitor rms current does not change. Similarly, the dc bus filter capacitor has the same rms current ripple and only the ripple frequency varies, where the ESR does not change significantly. Therefore, the capacitors on both sides of the converter are the same and their performances are the same for all the four cases. ESR of LCL filter capacitor is

around 50 mΩ and rms value of PWM current is less than 3.5 A. Thus, total amount of LCL filter capacitor losses is expected to be lower than 2 W. Including the DC bus capacitor losses, total amount of capacitor losses are accepted to be lower than 5 W and it does not make a significant effect in total amount of losses.

Accounting for all the losses of the VSC (power semiconductor, inductor, etc.), the efficiencies for all the four cases and power module types as a function of the load current are calculated and shown in **Figure 4.27**. For the first and third case, the calculations are verified by laboratory measurements.

In terms of efficiency, case 1> case 2> case 3 > case 4 indicate the SiC-MOSFET is advantageous. While case 2 reduces the heatsink size, case 3 provides inductor size reduction. Case 4 inductor size is significantly reduced at the cost of large efficiency degradation. It is apparent that there is trade-off between the inductor size/cost /loss reduction and module losses. While these indicators provide direction to a designer, PP and ROI assessment is the key to final design.

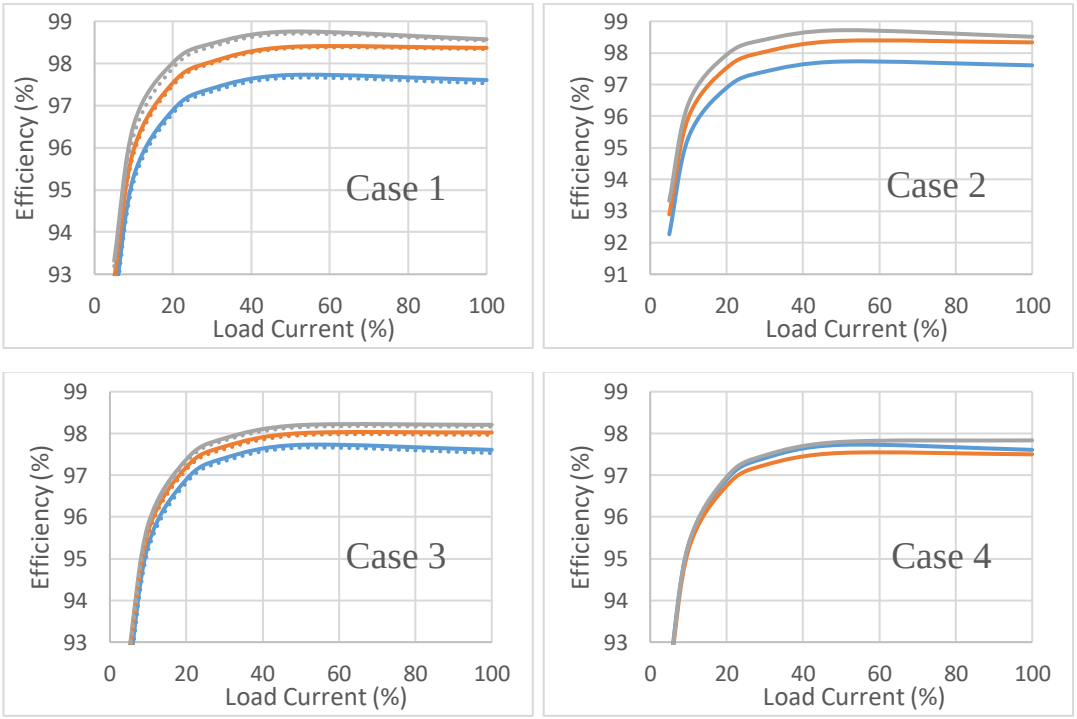


Figure 4.27 Calculated (solid) and measured (dashed) VSC efficiency curves, blue: Si-IGBT module, orange: H-IGBT module, gray: SiC-MOSFET module.

4.6.2. Euro Efficiency

As mentioned earlier in Chapter 2, an efficiency parameter called “euro efficiency” is introduced to define a weighted efficiency value using efficiency vs load curves of the converters. By definition, euro efficiency is given in equation (4.33). Based on this fact, a single operating point is not enough to conduct a design for a PV converter, or it is not enough to judge the techno-economic feasibility of the new device technology.

Although the boost converter is not taken into economic evaluation in this dissertation with the main focus being the VSC performance and cost (such that the study is valid also for single stage systems), the total energy efficiency, which affects the energy harvesting amount requires taking the boost converter efficiency into account too. For this purpose, the boost converter energy efficiency is calculated and measured and taken into account in detail. While the boost converter operates with input voltage range of 450-650 V, its output is fixed at 750 V, thus the switching losses are not voltage (MPPT point) dependent. The boost converter is implemented with dual-pack Si-IGBT modules and its efficiency is calculated for 650 V input for the sake of simplicity. Measured efficiency curve of the boost converter for 8 kHz switching frequency is given in **Figure 4.28** for these conditions.

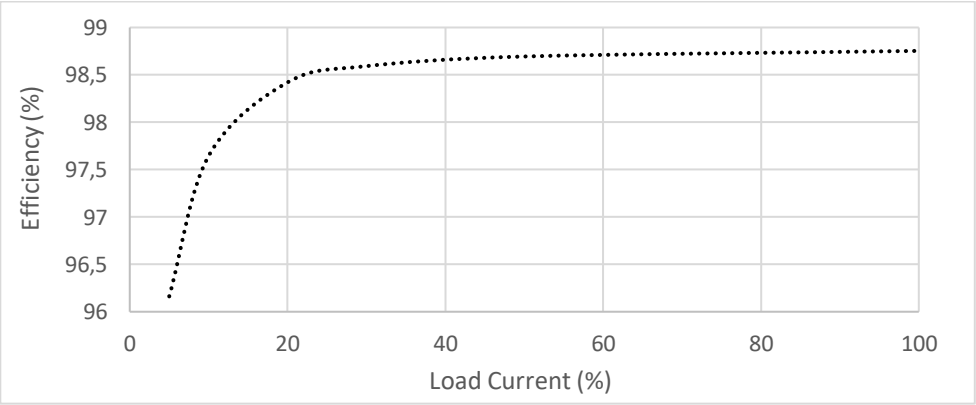


Figure 4.28 30-kW boost converter measured efficiency curve vs load.

$$\eta_{euro} = 0.03\eta_{5\%} + 0.06\eta_{10\%} + 0.13\eta_{20\%} + 0.10\eta_{30\%} + 0.48\eta_{50\%} + 0.2\eta_{100\%} \quad (4.33)$$

The boost converter efficiency (**Figure 4.28**) is multiplied by VSC efficiency to obtain the total efficiency of the PV conversion system. These total efficiency values are used in estimating the annual energy harvest through PV simulations. Before progressing to economic issues, it is helpful to assess the technologies in terms of euro efficiency. The calculated euro efficiency values are given in **Table 4.8** and they account for the boost converter (with Si-IGBT module) losses too. According to **Table 4.8**, as expected, the SiC-MOSFET technology is superior overall. In fact, efficiency of SiC-MOSFET cases can be further increased if a SiC-MOSFET module with a higher current rating is used or by paralleling the SiC-MOSFET transistors. Increasing efficiency reduces the cooling requirements and results in a smaller heatsink structure. That is why it is essential. However, economic considerations must be also taken into account during design stages. Thus, although design cases with SiC-MOSFET modules have the highest efficiency values, determining the best of the four cases (and even further, optimization via fine-tuning) still requires economic assessment.

Table 4.8 PV converter (VSC and boost converter) euro efficiency values for the four basic design cases and three module types

Efficiency (%)	Case 1	Case 2	Case 3	Case 4
Si-IGBT	95.82	95.82	95.82	95.82
H-IGBT	96.49	96.47	96.13	95.66
SiC-MOSFET	96.85	96.80	96.32	95.91

4.7. Conclusion

In this chapter, a design methodology for a grid-connected VSC is introduced. Specifically, it is introduced how to conduct a hardware design. An algorithm to calculate semiconductor losses is presented and sizing of heatsink and inductors are shown. Calculation methods of inductor core and copper losses are given. In this way, calculation of major losses in a VSC structure is shown.

After design methodology is given in detail, a reference design with Si-IGBT modules is conducted. First, specifications are given and then the hardware design is completed

with presented design methodology. Design is verified by both simulations and experimental results.

Then, four progressive design cases are proposed with H-IGBT and SiC-MOSFET modules. Calculation of major loss components are conducted for all of the designs and efficiency vs load plots are obtained for all design cases. In addition, calculations are verified by experimental efficiency measurements for first and third design cases. Finally, euro efficiency concept is introduced and euro efficiency values of all four design cases are compared.

While the technical details compared in this chapter among different design cases with different semiconductor technologies, it is economic evaluation which determines the applicability and feasibility of each design. Thus, a techno-economical evaluation is needed to see the economic performance of each four design cases or propose a better design than these four proposed design cases.

Moreover, it is also essential to make a forecast about future as price of semiconductor modules keep changing. Thus, in addition to techno-economic evaluation with present market conditions, forecasts should also be given about future market conditions. All these points are mentioned in detail in Chapter 5.

CHAPTER 5

ECONOMIC ASSESSMENT OF GRID-CONNECTED VSC DESIGNS THROUGH A 1-MW PV POWER PLANT APPLICATION

5.1. Introduction

The voltage source converter (VSC) of the grid connected photovoltaic (PV) systems is the most technological component in a PV system and contributes to 5–15% of the whole investment. As the cost and energy efficiency of a VSC are two factors that determine the total system economics, the system total cost of ownership (TCO) should be optimized during the VSC design. While, in industry, typically the application field constraint is gained via know-how, a-priori design involving the application conditions is rare due to lack of knowledge and methodology in merging the technical and economical specs into one pot considering the specific application.

In this chapter, the developed VSC designs in Chapter 4 with H-IGBT and SiC-MOSFET modules are evaluated economically through a 1-MW PV power plant application which was introduced in detail in Chapter 2. The same PV power plant application is considered in six different locations namely Palermo (Italy), Napoli (Italy), Milano (Italy), Konya (Turkey), Sion (Switzerland), and Tallinn (Estonia). In this way, effects of climatic conditions (mostly irradiance) and FIT values on the economic performance of the design are taken into account. The annual global irradiance values and FIT values of these locations are already given in **Table 2.4** in Chapter 2. Moreover, other technical details of PV power plant such as PV module configuration and inclination angle of PV modules are also provided in **Table 2.4**.

First, economic terms which are used in the economic assessment are introduced. Second, PV power plant economics are mentioned, and PV converter based economic assessment approach is introduced. Then, energy harvesting concept and trade

mechanism in PV power plants via feed-in-tariff (FIT) values are explained. Finally, formulization of the optimization problem is defined. At the end, economic assessment among VSC design cases is conducted, and results are discussed.

5.2. Economic Terms

In this chapter, TCO (total cost of ownership), ROI (return on investment), and PP (payback period) parameters are taken into account in economic evaluation of PV power plant investments with different grid-connected three-phase VSC design cases with different semiconductor module technologies. In this way, optimum techno-economical solution is obtained. Economic assessment is conducted through a specific MW-scale PV power plant application and TCO, ROI, and PP parameters are calculated for this specific application. However, results can be generalized to all solar farm applications.

While PP defines the duration that the investment pays the initial investment back, ROI can be denoted as a measure of net profit at the end of plant lifetime with respect to the initial investment. TCO, ROI and PP parameters are defined with the equations (5.1), (5.2), and (5.3) respectively.

$$TCO = \sum(Initial\ Investment + Operation\ \&\ Maintenance\ Cost) \quad (5.1)$$

$$PP\ (Year) = \frac{Total\ Investment\ (USD)}{Total\ yield\ equal\ to\ the\ total\ investment\ (USD/year)} \quad (5.2)$$

$$ROI\ (\%) = \frac{Net\ Profit\ at\ the\ end\ of\ lifetime\ (USD)}{Total\ Investment\ (USD)}\ x\ 100 \quad (5.3)$$

5.3. PV Power Plant Economics

PV power plants captured the attention of many investors in most of the world since the beginning of second decade of 21st century. Especially the decreasing cost of PV modules and determination of energy trade mechanism in many regions clearly attracted investors to this field. Thus, many economic analysis and study has been conducted about the TCO of a PV power plant and possible PP values and ROI rates at the end of PV power plant's lifetime.

TCO defines the whole cost of a plant including initial investment, maintenance, and operation costs [33]. For a solar farm application, initial investment includes the costs of the followings:

- Real estate cost
- Civil works (excavation operations, road access, etc.)
- Engineering and project management costs
- Ground mounting system construction
- PV modules
- PV converters (and its container if it exists)
- DC combiner boxes
- DC and AC cables
- Transformer and its container (including substation)

In addition, installation of these components and their first tests on the field are also included in the initial investment costs. Once all the tests on the field are completed successfully, commissioning is carried out. At this stage, initial investment costs finish, and maintenance and operation costs start.

Maintenance and operation costs can be also sorted item by item as follows:

- Security costs (security guard, camera system, etc.)
- Internal consumption (lightning system, security guard container consumption, etc.)
- Operator costs
- Maintenance and repairment costs

Lifetime of a PV power plant is considered to be minimum 20 years. Actually, it can extend up to 30 years with proper operation and maintenance service, but it is accepted as 20 years in this study since most of the PV module and PV converter suppliers can provide warranty up to maximum 20 years. Thus, operation costs (including the

security and control of the PV power plant) within 20 years of lifetime should be also taken into account.

In addition, maintenance costs must be also considered for proper operation of the plant during its lifetime. Some of the PV converter components such as DC electrolytic capacitors and fans have limited lifetime compared to total lifetime of the PV power plant. They are usually replaced with their new counterparts periodically at each 5 year and these replacement costs must be also included in maintenance costs. Moreover, PV converters are the most vulnerable components in a PV power plant, and it is stated that PV converter failures account for 61% of the total energy loss in PV power plant applications among all failures [7]. Thus, technical service costs of especially PV converters should be taken into account too while calculating the maintenance costs. In other words, a complete TCO analysis should include all the initial investments, operation and maintenance costs.

5.4. PV Converter Economics and Differential TCO Approach

As mentioned in TCO analysis of a PV power plant, maintenance and repairment costs of PV converters have significant importance in PV power plant applications. In addition, as PV converters are the most vulnerable components in the whole PV system, technical service convenience of the PV converters is also essential.

In fact, ratings of the components in the market and present manufacturing technology allow designing a 30-kW grid-connected PV converter as complete PCBA (printed circuit board assembly). In this way, manufacturing can be automized and possible defects which may decrease the product lifetime can be minimized. However, as a retrofitting approach is followed in this study, a new design is not developed from scratch but an already existing design with Si-IGBT technology is retrofitted with H-IGBT and SiC-MOSFET modules. Thus, handmade prototypes are prepared in this study. In this way, results of this study can be accepted as basis in terms of economic assessment and better designs can be assumed to provide better results in terms of economic considerations.

5.4.1. Differential TCO Approach

As mentioned in PV power plant economics, a complete TCO analysis of a PV power plant requires detailed analysis of initial investments, operation costs, and maintenance costs. However, such an analysis requires overwhelming effort especially at the design stage. Even for one PV converter, it is quite cumbersome to conduct such a detailed TCO analysis. Thus, an alternative differential TCO approach is proposed here to simplify the TCO analysis without losing ability to compare fairly the different VSC design cases in terms of economic aspects.

In this differential TCO approach, only the cost difference between different PV converter designs are accounted and economic assessment of the proposed design cases are conducted through these cost difference values. In this way, a PV converter based economic assessment is conducted. This approach significantly simplifies the economic analysis [33].

First of all, initial investment of PV power plant except the PV converters (PV module cost, cabling cost, DC combiner box cost, transformer cost and so on) are accepted equal in all cases. Moreover, maintenance and operation costs are also accepted equal for all systems with different PV converter designs with Si, hybrid and SiC power modules. In this way, operation and maintenance costs do not contribute to “cost difference” analysis and only the cost difference between initial costs of different PV converter designs is taken into account.

In PV converter, common components (DSP board, power supplies, fans etc.) and boost converter are also excluded from cost analysis too as they only bring offset to the calculations [33]. Eventually, only cost difference among power semiconductors, heatsinks, and inductors are considered to determine the total cost difference among alternative designs. In each design case, the component of the reference design is accepted as base value (X USD for semiconductors, Y USD for heatsinks, and Z USD for inductors) and the cost of the components in other designs are given in terms of this value. This cost differential approach allows a fair comparison.

5.4.2. PV Converter Components Included in Differential TCO Analysis

As mentioned, only the three main hardware components (semiconductor module, heatsink, and inductors) are taken into account in differential TCO analysis. A three-phase 30-kW VSC design with Si-IGBT is taken as reference and semiconductor module is changed with H-IGBT and SiC-MOSFET modules in different design cases. By keeping the switching frequency and inductance product constant in all design cases, four progressive design cases are proposed with different heatsink and inductor combinations. These proposed design cases are summarized in **Table 4.6** in Chapter 4. In this chapter, differential TCO analysis of these proposed design cases with different semiconductor power module, heatsink, and inductor components are given.

5.4.2.1. Semiconductors

As two-level topology is used in this 400 V AC grid-connected VSC design study, only 1200 V semiconductor modules are taken into consideration. In order to conduct a fair comparison between Si-IGBT, H-IGBT and SiC-MOSFET modules, price per ampere values are evaluated for one transistor – diode pair. However, as there are six transistor – diode pairs in a two-level VSC topology, cost difference of H-IGBT and SiC-MOSFET solutions w.r.t. the Si-IGBT technology (ΔC_s) is calculated as six times of cost difference of one transistor – diode pair. This evaluation is conducted based on the quotations obtained from a local distributor and recent posted e-market prices.

Table 5.1 shows the obtained semiconductor cost per ampere values of different semiconductor modules for one device. As shown in **Table 5.1**, Si-IGBT technology cost per ampere is around 0.095 – 0.115 USD for one device. The gap between minimum and maximum cost per ampere value is caused by packaging technology and package type (discrete package, dual pack package, 6-pack package and so on). Presently, H-IGBT technology with SiC Schottky diodes costs approximately 2.5 – 4 times of Si-IGBT technology in terms of cost per ampere. Depending on the current rating of the diode, cost per ampere values of H-IGBT modules vary between 0.23 – 0.42 USD for one transistor – diode pair.

Table 5.1 Semiconductor cost per ampere comparison for one device

Package Type	Brand	Model	Transistor		Diode		Cost Per Ampere
			Technology	Current	Technology	Current	
Dual Pack	Semikron	SKM150GB12T4	Si-IGBT	150 A	Si-Diode	150 A	0.112 USD
6-Pack	Semikron	SEMiX151GD12E4s	Si-IGBT	150 A	Si-Diode	150 A	0.095 USD
6-Pack	Semikron	SKiM459GD12F4V4	H-IGBT	450 A	SiC Schottky	250 A	0.260 USD
Dual Pack	Semikron	SKM200GB12T4SiC2	H-IGBT	200 A	SiC Schottky	160 A	0.392 USD
Dual Pack	Semikron	SKM200GB12F4SiC2	H-IGBT	200 A	SiC Schottky	160 A	0.420 USD
Dual Pack	Semikron	SKM200GB12F4SiC3	H-IGBT	200 A	SiC Schottky	80 A	0.237 USD
6-Pack	Semikron	SKiiP39AC12F4V19	H-IGBT	150 A	SiC Schottky	80 A	0.254 USD
6-Pack	Fuji	6MSI100VB-120-50	H-IGBT	100 A	SiC Schottky	100 A	0.366 USD
6-Pack	Semikron	SKiiP25AC12F4V19	H-IGBT	50 A	SiC Schottky	30 A	0.410 USD
Dual Pack	Semikron	SKM500MB120SC	SiC-MOSFET	500 A	-	-	0.639 USD
6-Pack	Semikron	SKiiP26ACM12V17	SiC-MOSFET	75 A	SiC Schottky	30 A	0.920 USD
Discrete	Cree	C3M0016120K	SiC-MOSFET	115 A	-	-	0.654 USD
Discrete	Cree	C2M0025120D	SiC-MOSFET	90 A	-	-	0.757 USD
Discrete	Rohm	SCT3030KLHR	SiC-MOSFET	72 A	-	-	0.750 USD
Discrete	Infineon	IDWD40G120C5	-	-	SiC Schottky	110 A	0.189 USD
Discrete	Infineon	IDWD20G120C5	-	-	SiC Schottky	62 A	0.167 USD
Discrete	Cree	C4D15120A	-	-	SiC Schottky	43 A	0.269 USD

As clearly seen in **Table 5.1**, H-IGBT modules with same 200-A transistors have different cost per ampere values (0.42 USD, 0.392 USD, and 0.237 USD) due to their different properties. While the most expensive one utilizes a 160-A SiC Schottky diode, the cheapest one has an 80-A SiC Schottky diode in its structure. This is an important point in terms of design and semiconductor sizing. If the designed grid-connected VSC is supposed to operate at unity power factor (or close to unity power factor) and if bi-directional power flow capability is not required, diode current rating can be selected much smaller than transistor current rating. Because in this operation mode, diode current is significantly lower than transistor current. This is also clearly seen in **Figure 4.24**. Diode conduction losses are significantly lower than transistor conduction losses at unity power factor operation of a grid-connected VSC.

On the other hand, although both transistor and diode current ratings are equal for SKM200GB12F4SiC2 and SKM200GB12T4SiC2 H-IGBT modules, there is still a cost difference between them. SKM200GB12F4SiC2 module transistor has lower switching losses and thus has better switching performance. Thus, its cost per ampere for one transistor – diode pair is higher compared to SKM200GB12T4SiC2.

SiC-MOSFET technology is much more expensive than Si-IGBT and H-IGBT technology in present market conditions. Without SiC Schottky diode, it is observed that SiC-MOSFET transistor cost per ampere values vary between 0.6 USD – 0.8 USD for one transistor. For SiC Schottky diodes, obtained quotations show that cost per ampere values vary between 0.15 USD – 0.25 USD. With a rough estimation, if SiC Schottky diodes are also included in SiC-MOSFET module costs, it can be concluded that the cost of SiC-MOSFET technology per ampere for one device (transistor – diode pair) would vary between 0.8 USD – 1 USD. Forecast of a local semiconductor sales representative imply that although an approximately 15% price reduction is expected in SiC Schottky diodes in the next 5 years, no major price reduction is expected in SiC-MOSFET transistors in the next 5 years due to manufacturing difficulties and limited amount of orders.

The 150-A Si-IGBT module is accepted as reference with X USD cost in this study. Based on the cost per ampere values provided in **Table 5.1**, the minimum cost per ampere difference between H-IGBT and Si-IGBT module is around 0.115. This corresponds to 17.25 USD cost difference per one transistor - diode pair for 150-A modules. As there are 6 transistor – diode pairs in two-level VSC structure, cost difference between H-IGBT and Si-IGBT modules can be assumed as 103.5 USD. For convenience, the cost of 150-A H-IGBT is accepted as X+100 USD in this study.

Taking the possible price reduction in SiC Schottky diodes in near future into account, cost per ampere of SiC-MOSFET with a SiC Schottky diode is estimated as 0.74 USD. As mentioned earlier, it is not a good approach to compare Si-IGBT and H-IGBT with a SiC-MOSFET at the same current rating. Thus, in this study, 75-A SiC-MOSFET module is selected for comparison with 150-A Si-IGBT and 150-A H-IGBT modules. The minimum cost difference between Si-IGBT and SiC-MOSFET per one transistor – diode pair is calculated as 38.7 USD in these conditions. This corresponds to 232.2 USD cost difference for whole VSC. Although no major price reduction is expected in SiC-MOSFETs, taking the possible minimal price reductions into account, cost of 75-A SiC-MOSFET module is accepted as X+200 USD in this study.

Determined cost difference values for semiconductors are shown in **Table 5.2**. Economic assessment of proposed design cases in present market conditions is conducted according to the cost difference values provided in **Table 5.2**. For possible lower price differences in the future, the study will be extended in a later stage and economic assessment is repeated for several future market estimations.

5.4.2.2. Heatsink and Inductors

For the stacked fin heatsink, cost is linearly proportional to the number of fins (N_f). Based on market prices, the proportionality constant between cost and N_f is evaluated as 1 in this application for the selected stacked fin heatsink dimensions. Equation (5.4) defines the cost difference (ΔC_{hs}) relation in the proposed heatsink design.

The energy formula, I^2L parameter is a good indicator to estimate the inductor cost. As the rated current is same in all cases, inductor cost is assumed as linearly proportional with inductance. The proportionality constant between inductor cost (USD) and inductance (μH) is obtained as 0.022 for stacked powder core inductors (converter side inductors) and 0.008 for low frequency core inductors (grid side inductors) based on market prices. Equations (5.5) and (5.6) show the cost difference relation in the converter side inductors ($\Delta C_{i\text{-}hf}$) and grid side inductors ($\Delta C_{i\text{-}lf}$). Since the VSC is three-phase, the cost difference values for inductors must be multiplied by three to find the total cost difference between VSCs due to inductor cost difference. As current ripple is kept constant at the VSC output, LCL filter capacitor is not changed in different design cases and its cost is excluded from cost difference analysis.

$$\Delta C_{hs}\ (USD) = \Delta N_f\ x\ 1 \tag{5.4}$$

$$\Delta C_{ind-hf}\ (USD) = \Delta L(\mu H)\ x\ 0.022 \tag{5.5}$$

$$\Delta C_{ind-lf}\ (USD) = \Delta L(\mu H)\ x\ 0.008 \tag{5.6}$$

5.4.2.3. Differential TCO Analysis of Proposed Design Cases

The cost difference analysis is summarized in **Table 5.2**. Based on the table each case has a different cost offset w.r.t the basic Si-IGBT design. With the SiC-MOSFET modules currently quoted with small counts and high cost, VSC with such components provides high cost relative to others. However, the higher efficiency resulting in higher annual yield is worth assessment the payback time. Furthermore, the SiC-MOSFET prices can decline over the coming several years, while the Si-IGBT has relatively fixed price (further, as some components become obsolete, their price may increase, as happened to power darlington BJTs in the 1990s).

As a conclusion, full assessment and price reduction prediction studies are important factors in evaluating the PV systems with ROI and PP parameters. This chapter establishes a method and the benefits are assessed via the given design and economic parameters. The results are based on the given quotes and better accuracy can be obtained with mass purchase quotes.

Table 5.2 Cost difference among 30-kW VSCs with different semiconductor modules in four proposed design cases

Case	Module	Semiconductor (C_s)[USD]	Heatsink (C_{hs})[USD]	Inductors (C_{ind})[USD]	Total Cost ($C_s+C_{hs}+C_{ind}$)[USD]
1	Si-IGBT	X	Y	Z	(X+Y+Z)
	H-IGBT	X + 100	Y	Z	(X+Y+Z) + 100
	SiC-MOSFET	X + 200	Y	Z	(X+Y+Z) + 200
2	H-IGBT	X + 100	Y – 10	Z	(X+Y+Z) + 90
	SiC-MOSFET	X + 200	Y – 15	Z	(X+Y+Z) + 185
3	H-IGBT	X + 100	Y	Z – 31.2	(X+Y+Z) + 68.8
	SiC-MOSFET	X + 200	Y	Z – 46.8	(X+Y+Z) + 153.2
4	H-IGBT	X + 100	Y	Z – 41.6	(X+Y+Z) + 58.4
	SiC-MOSFET	X + 200	Y	Z – 52.0	(X+Y+Z) + 148

5.5. Energy Harvest, FIT Value, and Annual Yield

Annual yield is economically the most important parameter for a PV power plant. Thus, all parameters should be optimized to get the highest annual yield in a PV power plant investment. Three main factors affect the annual yield:

- Geography (irradiance and temperature)
- Power conversion efficiency
- FIT value

First, geographical properties should be investigated in detail. Annual global irradiance, average temperature value through the year, and wind data (if it is available) should be evaluated. Basically, higher irradiance means higher energy input per unit area and lower temperature means higher PV module efficiency. Thus, it is a common method to choose locations with high irradiance and high altitude as average temperature decreases with altitude, but irradiance does not change. Moreover, windy locations are also preferred as wind provides cooling for PV modules especially at noon times where the irradiance reaches its peak point, but efficiency of PV modules decrease because of high temperature.

PV simulation programs can estimate the annual energy that can be obtained at PV module output with a specific PV module configuration at a specific location. It is

possible to obtain realistic estimations about possible annual energy harvest with proper meteorological data. Thus, it is a common practice to run PV simulations before making a decision about the location of PV power plant investment.

Second important factor which affects the annual energy yield is the PV converter efficiency. Here, both the power conversion efficiency and MPPT capability has crucial roles. As mentioned earlier in Chapter 2, single conversion PV converters can achieve higher peak efficiency values but their MPPT range is limited. In cloudy days, PV module string voltage may significantly drop due to low irradiance. Similarly, PV string voltage may again drop significantly in very hot summer days because of high temperature. In such conditions, double conversion topologies can still keep tracking the MPP point of the PV strings and keep harvesting the maximum energy from PV modules. In this study also a double conversion topology is used with a boost converter at PV input and a grid-connected VSC at the output.

Power conversion efficiency determines the amount of energy injected to the power grid. That is why even small enhancements in PV converter efficiency can achieve high economic gains in long term. However, as PV power plants do not always operate at rated power, PV converter efficiency vs load current curves should be taken into account while evaluating the efficiency of a PV converter. As also mentioned earlier, "euro efficiency" and "CEC efficiency" terms are already proposed in literature based on these efficiency curves [66]. Basically, the higher the PV converter efficiency, the higher the annual yield of the PV power plant.

Last but not the least, feed-in-tariff (FIT) value also has a crucial role in economic assessment of a PV power plant. Even though annual energy harvest is very high in a specific location, if FIT value is low in that region, annual income of the sold energy will be low too. Thus, FIT value must be taken into account too in order to achieve shorter PP and higher ROI rate. FIT values are taken from www.res-legal.eu website and they are accepted as 0.133 USD/kWh for Turkey, 0.110 USD/kWh for Switzerland, 0.060 USD/kWh for Estonia, and 0.044 USD/kWh for Italy [47] - [51].

5.6. Formulization of Optimization Problem

Four design cases are proposed in Chapter 4 with H-IGBT and SiC-MOSFET modules. These design cases are economically evaluated through a 1-MW power plant application in six different locations in this chapter. Three of them (Palermo, Napoli and Milano) have the same FIT value (ritiro dedicato, guaranteed minimum price for PV energy in Italy) so the effect of irradiance on ROI and PP is compared for these locations. In the remaining three locations (Konya, Sion and Tallinn), effect of both irradiance and FIT on ROI and PP are evaluated. Annual global irradiance and FIT values are provided in **Table 2.4** for each location [47] - [51]. PV*SOL (Valentin Software) is used to conduct photovoltaic simulations for these particular cases [65].

In fact, different criteria can be set for optimization of the design with H-IGBT and SiC-MOSFET modules. Most common two paths can be defined as optimization of ROI value by achieving a high efficiency and optimization of size of the converter by increasing f_{sw} and sacrificing efficiency. While the first path results in a higher efficiency and higher annual yield, the latter path results in a more compact and lighter product which increases portability and technical service convenience. In this study, first path is followed, and the optimization criterion is set as the highest ROI rate.

As a differential TCO approach is followed in this study, PP and ROI evaluations are also conducted according to this differential TCO approach. Equation (5.7) gives the cost equation of a VSC design. $C_{VSC\text{-}REF}$ denotes the cost of reference VSC design and it is a function of semiconductor cost (C_s), heatsink cost (C_{hs}), and inductor cost (C_{ind}). Cost of k^{th} VSC design ($C_{VSC\text{-}k}$) can be defined with respect to the cost of reference design. $\Delta C_{VSC\text{-}k}$ defines the cost difference between k^{th} VSC design case and reference VSC design. As expected, $\Delta C_{VSC\text{-}k}$ is also a function of ΔC_s (semiconductor cost difference w.r.t. the Si-IGBT solution), ΔC_{hs} (heatsink cost difference w.r.t. reference heatsink), and ΔC_{ind} (inductor cost difference w.r.t. the reference design inductors) as shown in equation (5.7).

$$C_{VSC-k} = C_{VSC-REF}(C_s, C_{hs}, C_{ind}) + \Delta C_{VSC-k}(\Delta C_s, \Delta C_{hs}, \Delta C_{ind}) \quad (5.7)$$

As all the other expenses and costs (including operation and maintenance costs) except initial PV converter cost are accepted equal in the proposed differential TCO approach, cost difference between k^{th} VSC design case and reference VSC design also defines the TCO difference for k^{th} design case. As seen in equation (5.8), TCO difference for k^{th} design case is denoted with ΔTCO_k.

$$\Delta TCO_k = \Delta C_{VSC-k}(\Delta C_s, \Delta C_{hs}, \Delta C_{ind}) \tag{5.8}$$

Based on differential approach, annual energy harvest values of each design case are also defined in terms of their difference with respect to the annual energy harvest of reference design. In equation (5.9), $E_{PV\text{-}k}$ defines the annual energy harvest value of k^{th} VSC design case, $E_{PV\text{-}REF}$ denotes the annual energy harvest value of the reference VSC design, and $\Delta E_{PV\text{-}k}$ denotes the annual energy harvest difference between k^{th} VSC design case and reference VSC design. Accordingly, annual yield of k^{th} VSC design case and annual yield difference between k^{th} VSC design case and reference VSC design can be defined with the equations (5.10) and (5.11) respectively. $YLD_{PV\text{-}k}$ represents the annual yield of k^{th} VSC design and $\Delta YLD_{PV\text{-}k}$ represents the annual yield difference between k^{th} VSC design case and reference VSC design.

$$E_{PV-k} = E_{PV-REF} + \Delta E_{PV-k} \tag{5.9}$$

$$YLD_{PV-k} = FIT\ x\ E_{PV-k} \tag{5.10}$$

$$\Delta YLD_{PV-k} = FIT\ x\ \Delta E_{PV-k} \tag{5.11}$$

Since PP and ROI are determined as the main criteria in economic assessment in this study, they must be also defined according to proposed differential approach. According to this approach, PP defines the payback period of the additional investment with respect to the reference design and ROI defines the ratio of net profit at the end of lifetime to this additional investment. The inequality which is given in (5.12) defines the relation with PP and ΔTCO_k. As solar energy harvest is not constant through the year, it is more appropriate to provide PP as an integer value in terms of years. Thus, PP (year) is defined as the minimum value which satisfies the inequality given in (5.12).

$$\Delta YLD_{PV-k}\ x\ PP(year)_{min} \geq \Delta TCO_k \quad (5.12)$$

Total net profit difference at the end of the lifetime for k^{th} design case is given in equation (5.13). $\Delta P_{PV\text{-}k}$ represents the total net profit difference at the end of lifetime between k^{th} VSC design case and reference VSC design. Lifetime of the PV power plant is denoted by $t_{lifetime}$. Equation (5.14) gives the ROI rate according to the total net profit difference. In this equation, $\Delta ROI_{PV\text{-}k}$ shows the ROI rate of k^{th} design according to the total net profit difference at the end of lifetime ($\Delta P_{PV\text{-}k}$) and ΔTCO_k.

$$\Delta P_{PV-k} = (t_{lifetime}\ x\ \Delta YLD_{PV-k}) - \Delta TCO_k \quad (5.13)$$

$$\Delta ROI_{PV-k} = \frac{\Delta P_{PV-k}}{\Delta TCO_k} \quad (5.14)$$

Lifetime of the PV power plant is assumed as 20 years in this study. It is a known fact that PV modules degrade each year. **Figure 5.1** shows the performance degradation of the PV module JKM260PP-60 in years. In order to take this effect into account, in this study, it is assumed that annual energy harvest decreases 1% every year due to degradation of PV modules. At the end of 20 years, PV modules are supposed to operate with approximately 82.6% of their initial performance. This effect is modelled in the study with the equation (5.15). $E_{PV\text{-}n}$ denotes the annual energy harvest in n^{th} year and $E_{PV\text{-}1}$ denotes the annual energy harvest in 1^{st} year in this equation.

In addition to degradation of PV modules, cabling losses are also taken into account in PV simulations and modelled as 1% of annual energy harvest.

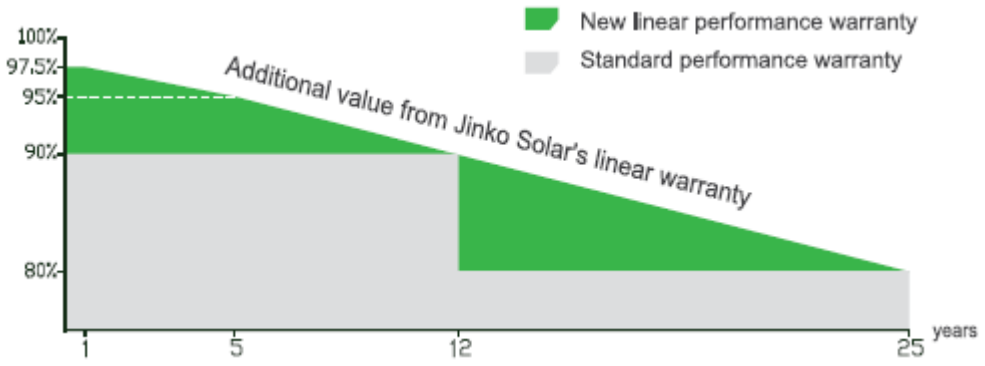


Figure 5.1 Degradation of PV module in time.

$$E_{PV-n} = E_{PV-1}\ x\ (0.99)^{n-1} \tag{5.15}$$

Although economic assessment of four proposed design cases in this PV power plant model give an idea about the advantages and disadvantages of the VSC designs with H-IGBT and SiC-MOSFET modules, variation of switching frequency with only integer multiples of 8 kHz limits the optimization process in the proposed design cases. In fact, an optimum design point may exist between integer multiples of 8 kHz for H-IGBT and SiC-MOSFET modules. Thus, a further design optimization is conducted. This further design optimization is considered as a multi-variable optimization process and optimum ΔROI value is tried to be found at several semiconductor module costs and switching frequencies. The analysis is conducted in Konya as Konya is the location with highest FIT value and it has the second highest irradiance value among all six locations. Moreover, same optimization process is also repeated for Palermo as Palermo has the highest irradiance value among all locations. **Figure *5.2*** shows a conceptual drawing of the optimization results. With the prime variables being the semiconductor cost difference and the switching frequency, the overall performance is measured with differential return on investment. This optimization may yield various local optimums, and it is important to assess these cases and find the global optimum for maximum benefit.

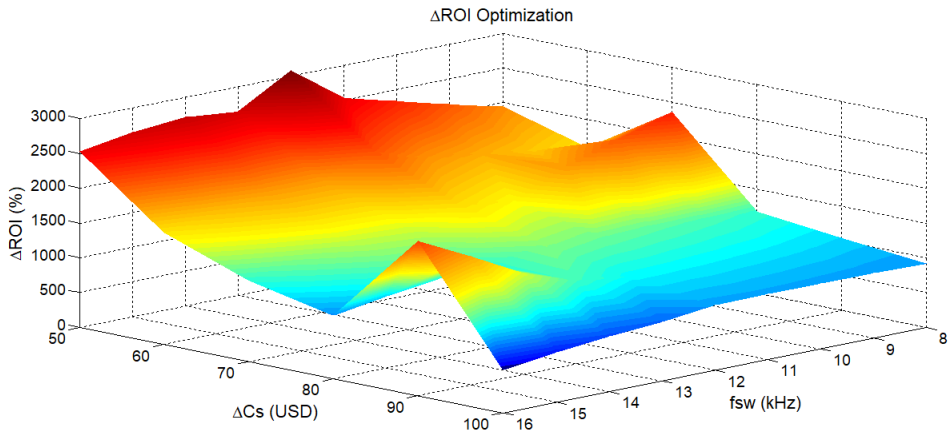


Figure 5.2 Multi-variable optimization surface plot for optimum ΔROI value.

5.7. Economic Assessment

Economic assessment is conducted with different VSC design cases for the given economic PV power plant model. First, economic assessment of four proposed VSC design cases is completed with present market conditions. Second, economic assessment is repeated for future conditions taking the possible price reductions in semiconductor modules into account. Finally, further design optimization is carried out in addition to four proposed design cases to obtain the optimum the switching frequency for highest ΔROI values with both H-IGBT and SiC-MOSFET modules.

5.7.1. Economic Assessment of the Four Proposed Design Cases with Present Market Conditions

Proposed VSC design cases in Chapter 4 are evaluated with present market conditions in six different locations. The predictions and estimations about possible price fall of H-IGBT and SiC-MOSFET modules are only mentioned later in this chapter.

Cost difference between PV converters is found as shown in **Table 5.2** for each design case. This cost difference value for one PV converter is multiplied with total number of PV converters in 1-MW PV power plant (33) to find the total cost difference.

Table 5.3 shows the annual energy harvest (MWh/year) for all design cases in six different locations for the 1st year of installation and payback period considering the 20 years of power plant lifetime with present market conditions. Note that payback periods are given as integer values in terms of years because it is more reasonable to use annual energy harvest values as energy harvest is not constant throughout the year. In **Table 5.3**, the cases with payback period longer than 20 years are labeled as not economically feasible (NEF).

Table 5.3 shows that case 2 with H-IGBT module has the lowest PP values in all locations. Although the SiC-MOSFET module provides higher annual energy harvest compared to other modules, its high cost degrades its investment value with present market conditions. However, it is a question what the cost of SiC-MOSFET module

should be to provide better ΔROI values then H-IGBT module. This question is answered later in this chapter when detailed analysis is conducted about estimations about future market conditions.

Table 5.3 Annual energy harvest of all design cases for six different locations for the 1 MW plant

Case	**Module**		**Annual Energy Harvest in 1st Year of the Installation (MWh/year) and Payback Period (Year)**					
			Palermo	**Napoli**	**Milano**	**Konya**	**Sion**	**Tallinn**
1	Si-IGBT (Ref)	Annual Harvest	1.946	1.799	1.428	1.966	1.612	1.117
		Payback Period	-	-	-	-	-	-
	H- IGBT	Annual Harvest	1.960	1.812	1.438	1.980	1.623	1.125
		Payback Period	<6	<7	<8	<2	<3	<8
	SiC-MOSFET	Annual Harvest	1.966	1.818	1.443	1.986	1.629	1.129
		Payback Period	<8	<9	<11	<3	<4	<10
2	H-IGBT	Annual Harvest	1.959	1.811	1.437	1.980	1.623	1.124
		Payback Period	<6	<6	<8	<2	<3	<7
	SiC-MOSFET	Annual Harvest	1.965	1.817	1.442	1.985	1.628	1.128
		Payback Period	<8	<9	<11	<3	<4	<10
3	H-IGBT	Annual Harvest	1.953	1.805	1.432	1.973	1.617	1.120
		Payback Period	<8	<9	<12	<3	<4	<11
	SiC-MOSFET	Annual Harvest	1.956	1.808	1.435	1.976	1.620	1.122
		Payback Period	<12	<13	<17	<4	<6	<16
4	H-IGBT	Annual Harvest	1.943	1.796	1.425	1.963	1.609	1.115
		Payback Period	NEF	NEF	NEF	NEF	NEF	NEF
	SiC-MOSFET	Annual Harvest	1.948	1.801	1.429	1.969	1.614	1.118
		Payback Period	NEF	NEF	NEF	<15	NEF	NEF

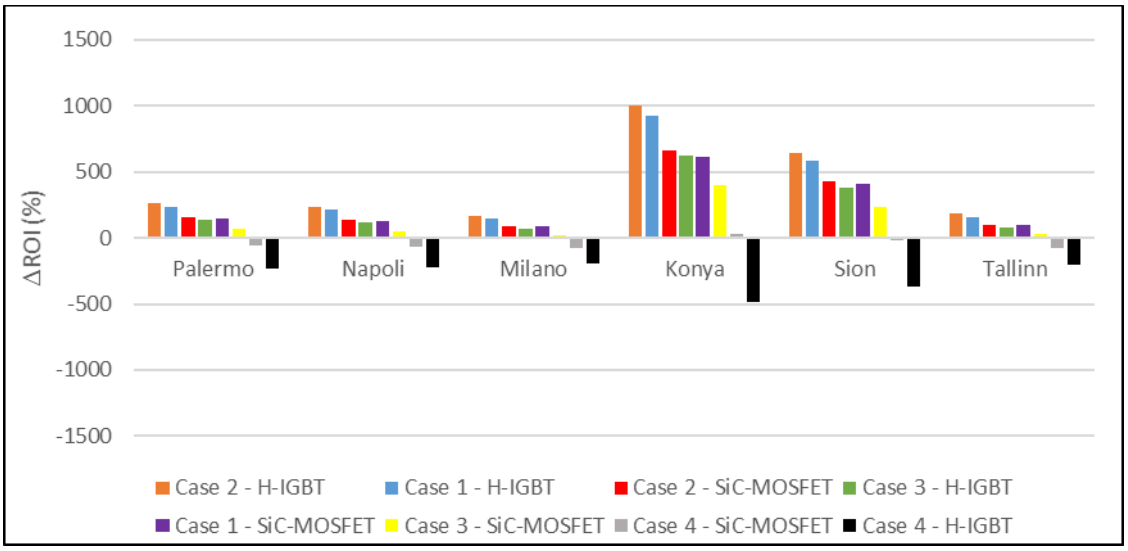


Figure 5.3 ΔROI (%) comparison of four design cases with present market conditions (200 USD ΔC_s value for SiC-MOSFET and 100 USD ΔC_s value for H-IGBT) in six different locations.

Figure 5.3 shows the ΔROI values in each location as bar graph. When ΔROI values of three cities in Italy (Palermo, Napoli and Milano) are compared, ΔROI values are higher in Palermo. Although FIT values are same for these cities, higher irradiance in Palermo brings the advantage of higher annual energy harvest. Thus, net profit is higher in this location at the end of 20 years lifetime. If all locations are compared, Konya has the highest ΔROI values because irradiance in Konya is quite high (second highest irradiance after Palermo) and its FIT value is highest among six cities.

As clearly seen in **Figure 5.3**, when f_{sw} is aggressively increased in case 4, H-IGBT module cannot pay the initial investment back in none of the locations. SiC-MOSFET module can pay the initial investment back only in Konya. Although this approach reduces the inductor size and cost significantly increasing portability and technical service convenience, it sacrifices efficiency because of high semiconductor losses, and it is not favorable economically with present market conditions.

It is also noticed in **Figure 5.3** that bar graphs have a similar pattern in every location. While design cases 1 and 2 with H-IGBT module show the best performance in all locations, same design cases with SiC-MOSFET module follow them. Design case 3

with H-IGBT module also achieves very close ΔROI value to the design cases 1 and 2 with SiC-MOSFET module in all locations. However, design case 3 with SiC-MOSFET module has lower ΔROI values than same design case with H-IGBT module. So, while location affects the ΔROI value of a design, it does not significantly affect the relative performance of a design case w.r.t the other design cases.

5.7.2. Estimations About Future Market Conditions

As H-IGBT and SiC-MOSFET prices are expected to fall in the future, an analysis about the future market conditions can be made to compare the proposed design cases at different module prices. **Figure 5.4** – **Figure 5.8** provides the ΔROI bar graphs in each location at different ΔC_s values.

Figure 5.4 shows the ΔROI performance of each design case with present market conditions. As also mentioned before, design cases 1 and 2 with H-IGBT have the highest ΔROI values in all locations with present market conditions.

Figure 5.5 and **Figure 5.6** show the cases where the cost difference between H-IGBT and Si-IGBT modules falls to 75 USD and 50 USD. At the same time the cost difference between SiC-MOSFET and Si-IGBT modules falls to 150 USD and 100 USD respectively. It is seen in **Figure 5.5** that ΔROI value in design case 3 with H-IGBT significantly increases when cost difference between H-IGBT and Si-IGBT modules falls to 75 USD. Moreover, as seen in **Figure 5.6**, if cost difference further falls to 50 USD, design case 3 with H-IGBT even has the highest ΔROI value among all design cases.

Figure 5.5 and **Figure 5.6** show that the better switching performance of H-IGBT module (compared to Si-IGBT module) can only be used when the cost difference between H-IGBT and Si-IGBT modules fall to 50 USD level. It is because the cost advantage gained by the reduction of inductance (with increasing f_{sw}) can be only valuable compared to initial cost of semiconductors when the cost difference between semiconductor modules falls to 50 USD levels. As a result, when the cost difference

between H-IGBT and Si-IGBT module falls to 50 USD, design case 3 with H-IGBT (f_{sw}= 16 kHz) has the highest ΔROI value among all design cases in all locations.

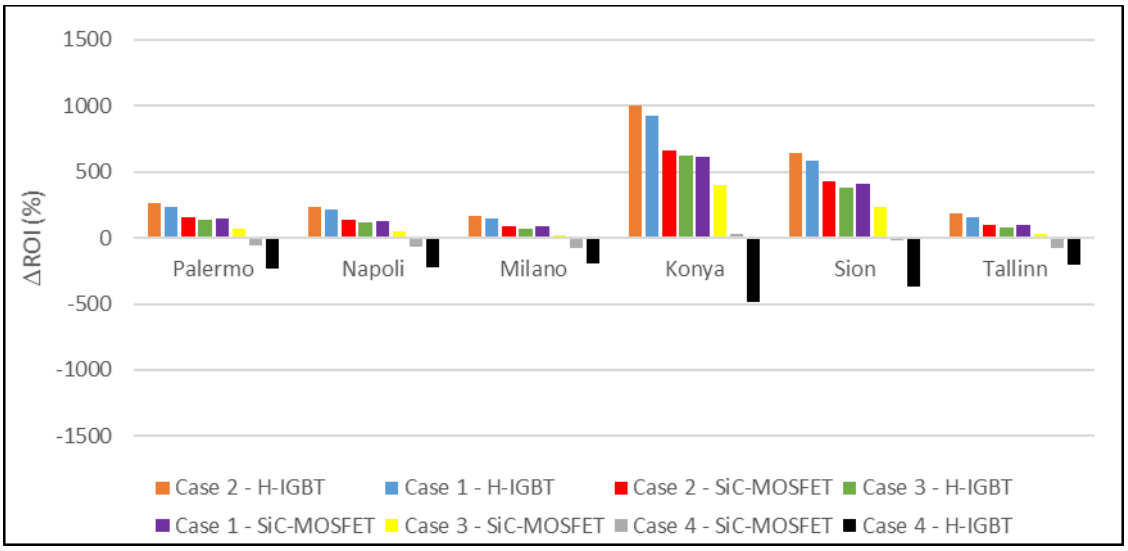


Figure 5.4 ΔROI (%) comparison of four design cases for 200 USD (SiC-MOSFET) and 100 USD (H-IGBT) ΔC_s values.

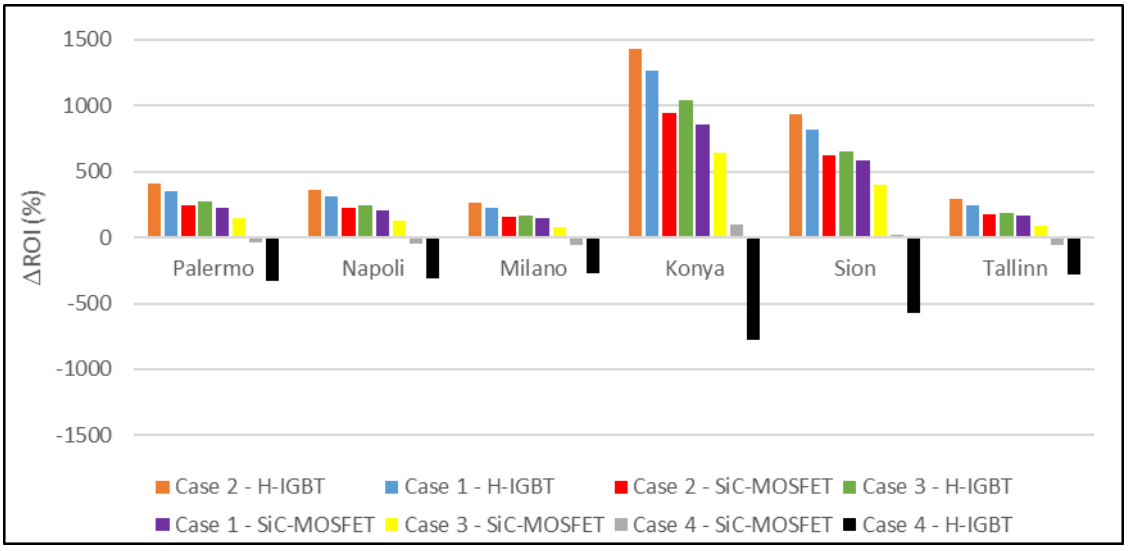


Figure 5.5 ΔROI (%) comparison of four design cases for 150 USD (SiC-MOSFET) and 75 USD (H-IGBT) ΔC_s values.

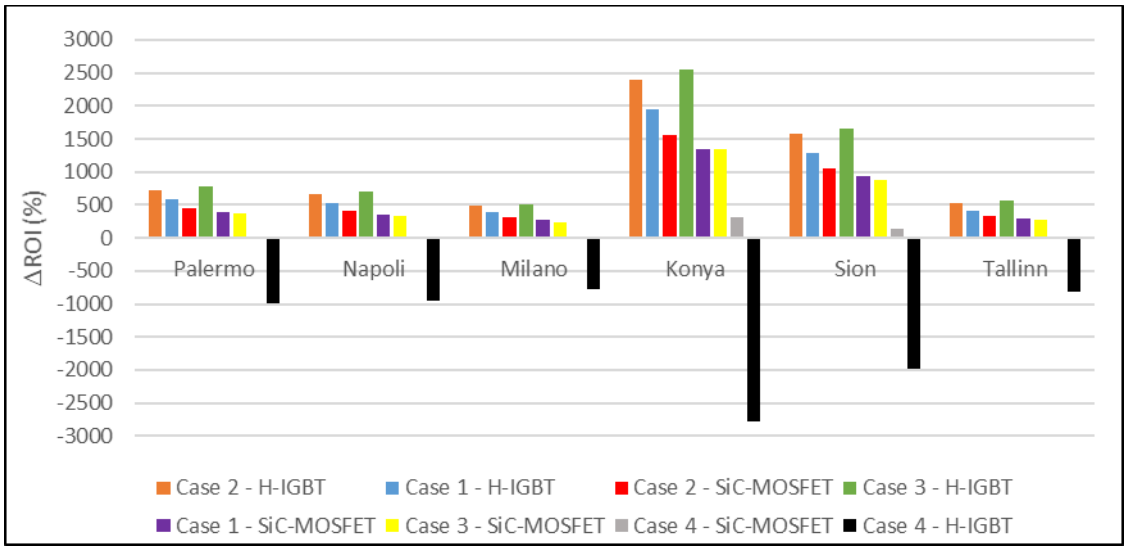


Figure 5.6 ΔROI (%) comparison of four design cases for 100 USD (SiC-MOSFET) and 50 USD (H-IGBT) ΔC_s values.

Similarly, the switching capability advantage of SiC-MOSFET module also becomes valuable when the cost difference between SiC-MOSFET and Si-IGBT modules decrease. **Figure 5.7** and **Figure 5.8** show the ΔROI values in all locations when cost difference of SiC-MOSFET and Si-IGBT modules fall to 75 USD and 60 USD respectively. As clearly seen, when the cost difference falls to 75 USD, design case 3 with SiC-MOSFET (f_{sw}= 32 kHz) becomes economically the most attractive solution with its highest ΔROI value. Furthermore, when cost difference further decreases to 60 USD, design case 3 with SiC-MOSFET achieves a far higher ΔROI value than other design cases in all locations. Moreover, even design case 4 with SiC-MOSFET, where the f_{sw} is aggressively increased to 48 kHz, also has a comparable ΔROI value with other design cases when cost difference between Si-IGBT and SiC-MOSFET modules fall to 60 USD levels.

This analysis proves that as the module price of the H-IGBT and SiC-MOSFET modules fall down, designs with higher frequencies will be more attractive. This is because as module price falls down, semiconductor prices become more comparable with inductor and heatsink prices so that the gain in inductor or heatsink gets more meaningful. Therefore, higher switching frequency capability of H-IGBT and SiC-

MOSFET modules will be only advantageous when their cost difference with respect to Si-IGBT approach 50 USD levels.

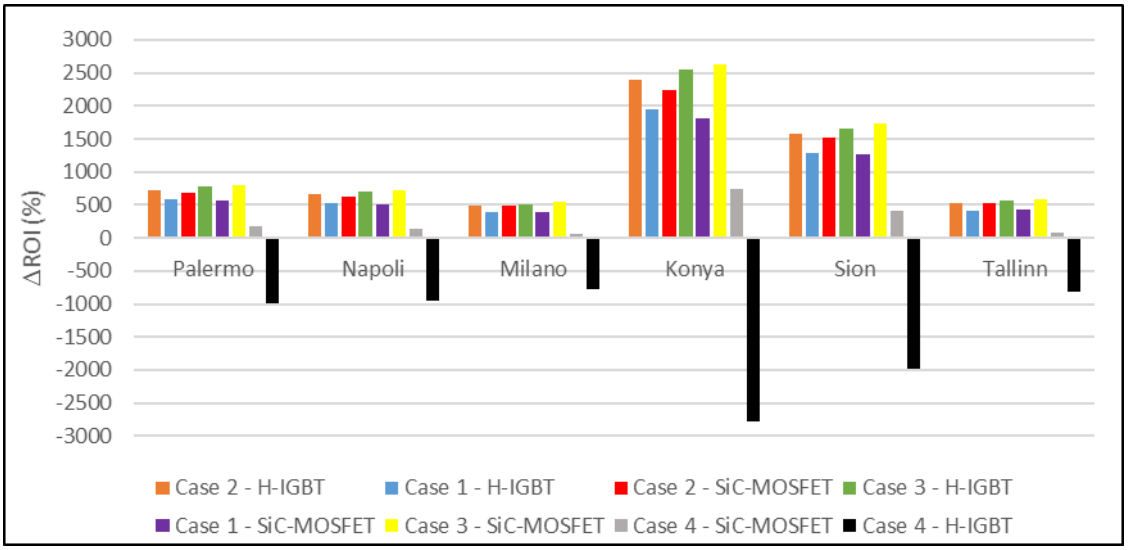


Figure 5.7 ΔROI (%) comparison of four design cases for 75 USD (SiC-MOSFET) and 50 USD (H-IGBT) ΔC_s values.

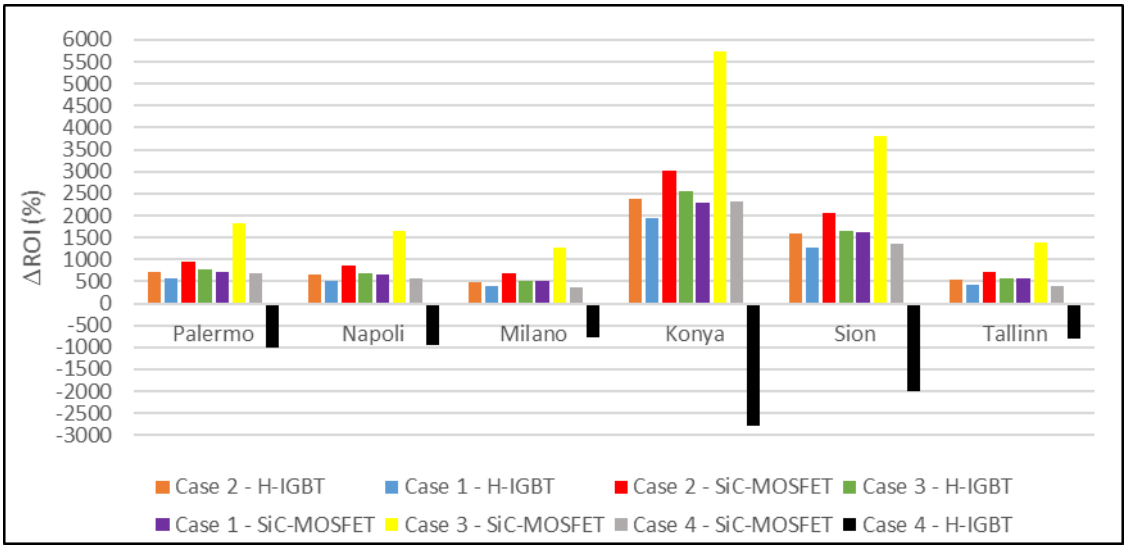


Figure 5.8 ΔROI (%) comparison of four design cases for 60 USD (SiC-MOSFET) and 50 USD (H-IGBT) ΔC_s values.

5.7.3. Economic Assessment of ΔROI-Optimized Design Cases

As mentioned earlier in this chapter, proposed four design cases may not correspond to the optimum VSC design which achieves the highest ΔROI value. In order to find the optimum switching frequency which would result in the highest ΔROI value for VSC designs with both H-IGBT and SiC-MOSFET modules, the switching frequency is swept between 8 kHz – 16 kHz for H-IGBT, and between 8 kHz – 32 kHz for SiC-MOSFET modules. Of course, ΔROI value also depends on the cost of the semiconductor module. Thus, a multi-parameter optimization is required, and surface plots are used to conduct this multi-parameter optimization process. Semiconductor cost difference is placed on X-axis, switching frequency is placed on Y-axis, and ΔROI value is shown at Z-axis.

Figure 5.9 provides the flowchart for ΔROI optimization of design cases with H-IGBT and SiC-MOSFET modules with exhaustive search method. First, power module is selected (H-IGBT or SiC-MOSFET) and location is determined. Then semiconductor cost difference sweep loop is started. While the cost difference between H-IGBT and Si-IGBT modules is swept between 100 USD and 50 USD, the cost difference between SiC-MOSFET and Si-IGBT is swept between 200 USD and 60 USD. Inside the cost difference loop, frequency sweep loop is placed. In this way, possible maxima of ΔROI values are observed at each cost difference value.

Once the optimum switching frequency is determined, further optimization can be conducted about heatsink size. Through the whole study, 80 °C heatsink temperature at rated power is considered temperature limit for heatsink. Any heatsink structure which results in a lower heatsink temperature at rated power is considered oversized. Thus, heatsink size is reduced in case a lower heatsink temperature is calculated. Converter cost can be decreased in this manner. This approach results in a higher ΔROI value at the end of PV power plant lifetime.

In this study, this design optimization is conducted in two locations: Konya and Palermo. Konya is selected as it achieves the highest ΔROI values among all selected

six locations and Palermo is selected as it has the highest irradiance value among all six locations.

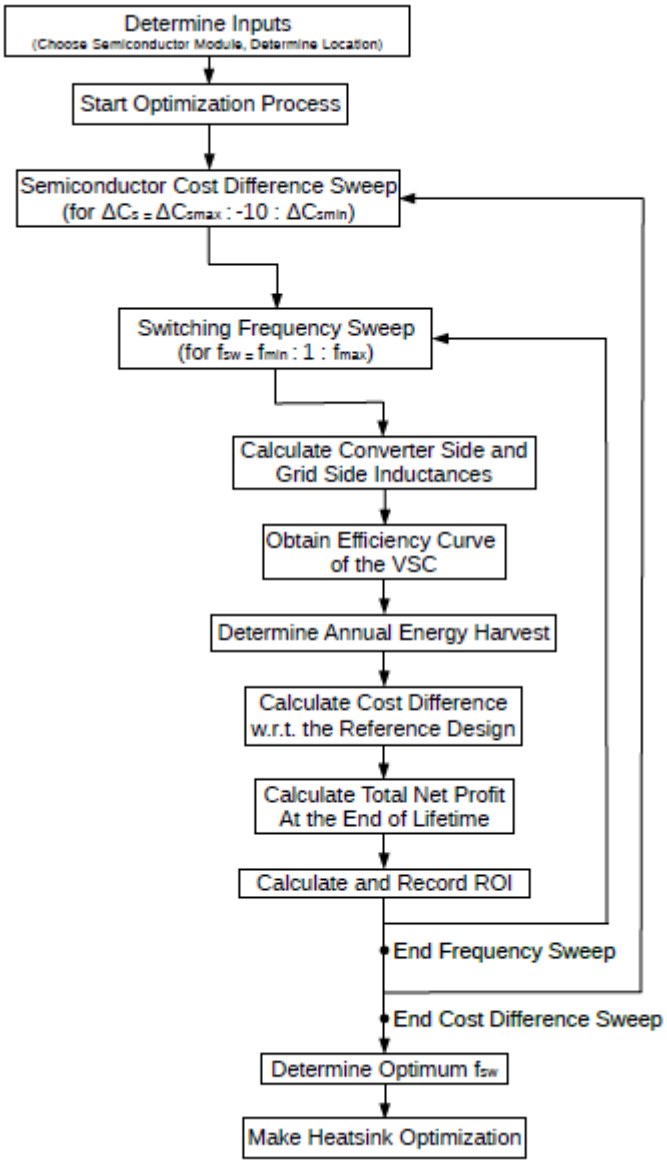


Figure 5.9 ΔROI design optimization flowchart by exhaustive search.

5.7.3.1. ΔROI Optimization for Konya

In order to find the optimum design point in Konya, switching frequency is swept between 8 kHz and 16 kHz for H-IGBT designs. Switching frequency and inductance product is kept constant in all switching frequencies. Similarly, switching frequency is swept between 8 kHz and 32 kHz for SiC-MOSFET designs.

As mentioned earlier, it is a better approach to take this optimization procedure as a multi-parameter optimization process. Thus, surface plots are prepared for Konya location according to the draft chart shown in **Figure 5.2**.

Figure 5.10 (a) shows the ΔROI values at the end of frequency sweep operation for design cases with H-IGBT module and **Figure 5.10 (b)** shows the ΔROI value surface plots at the end of heatsink optimization. In **Figure 5.10 (a)**, it is observed that 12 kHz switching frequency provides the highest ΔROI value in a wide range of ΔC_s values. This is better seen in **Figure 5.11** where the ΔROI vs ΔC_s curves are provided for several frequencies between 8 kHz and 16 kHz. As seen in **Figure 5.11**, 12 kHz switching frequency (gray curve) provides the highest ΔROI value when ΔC_s value is between 55 USD and 85 USD. Thus, further heatsink optimization is conducted for 12 kHz design case.

As clearly seen in **Figure 5.10 (b)**, the design case at 12 kHz with heatsink optimization provides the best ΔROI value compared to other VSC designs at other switching frequencies. **Figure 5.11** approves this result too. As seen with black dashed line in **Figure 5.11**, heatsink optimized design case at 12 kHz provides the highest ΔROI value in all ΔC_s values among all VSC design cases with H-IGBT module in Konya location.

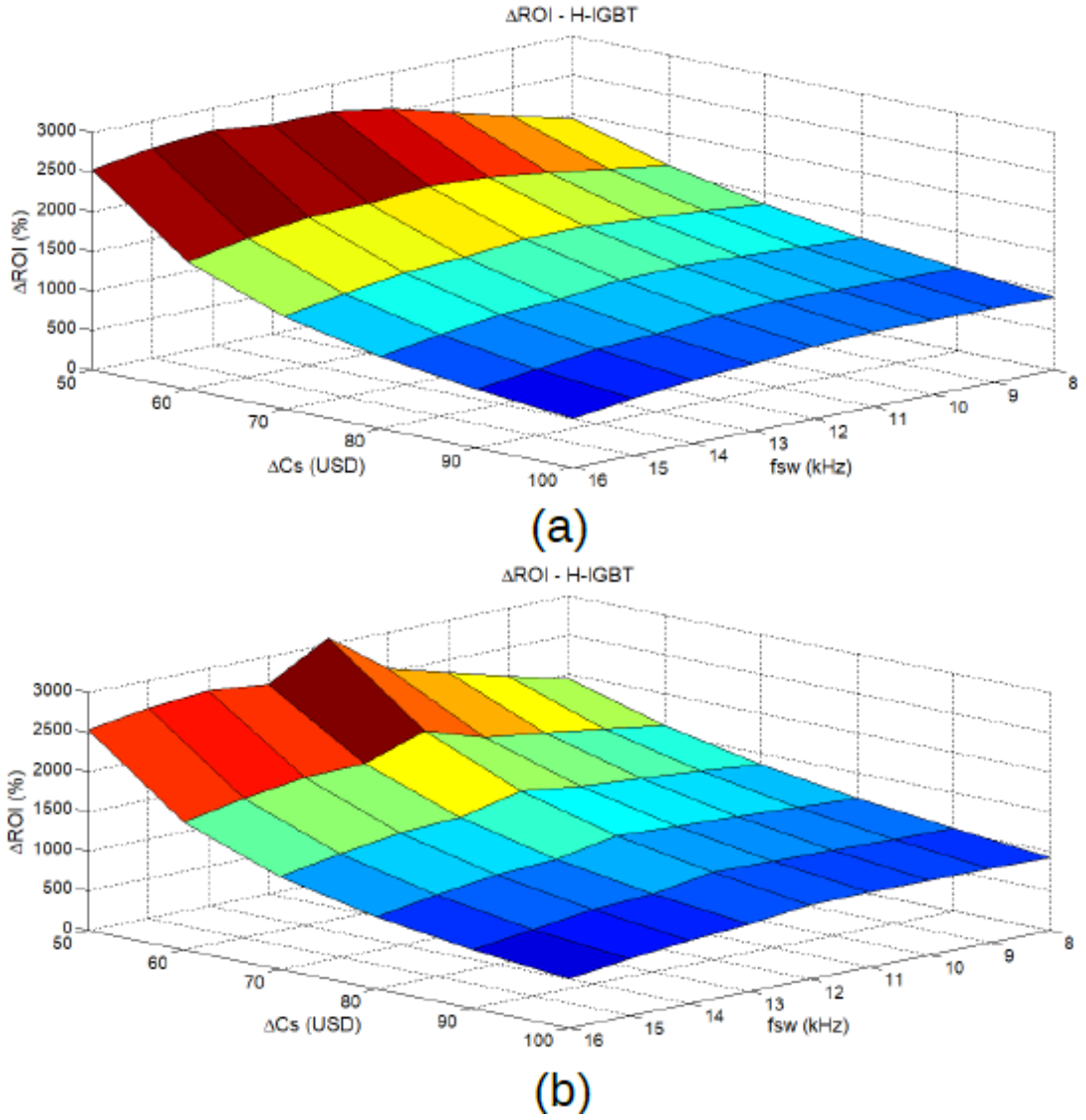


Figure 5.10 Multi-variable ΔROI optimization plots for VSC designs with H-IGBT module in Konya location. (a) f_{sw} sweep plot. (b) Heatsink optimized plot.

As a result, even though case 2 (f_{sw}= 8 kHz) appears most advantageous today as it maintains efficiency and reduces heatsink cost, case 3 (f_{sw}= 16 kHz) can be improved by trading off IGBT switching losses for improving efficiency (the inductor size and loss reduction is also traded off). Reducing f_{sw} from 16 kHz to 12 kHz, the nominal efficiency is improved. Under this condition, the heatsink temperature falls from 74 ˚C to 68 ˚C. With another iteration, heatsink size can be reduced such that the nominal heatsink temperature (80 ˚C) is restored, where the optimum ΔROI curve is obtained.

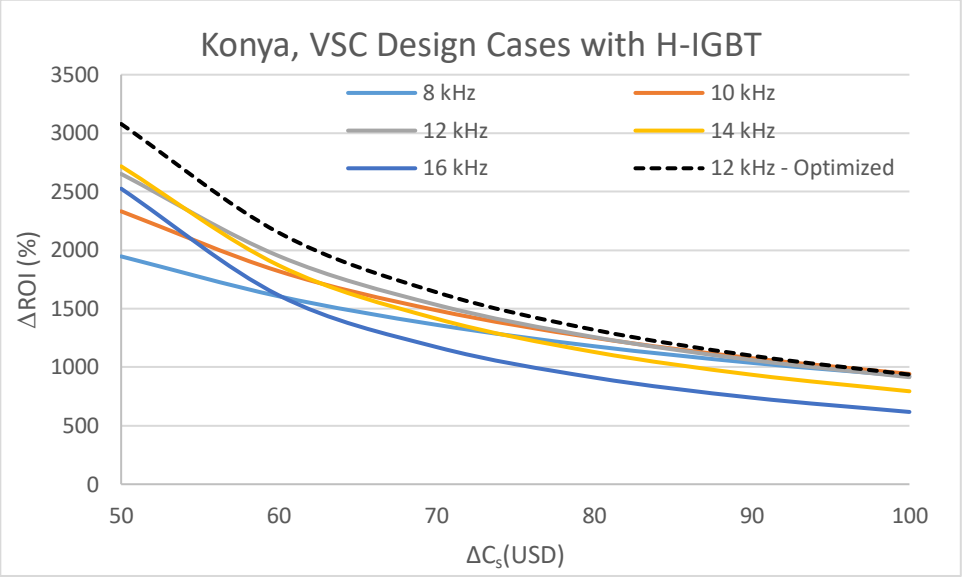


Figure 5.11 ΔROI vs ΔC_s curves for VSC designs with H-IGBT module at various switching frequencies in Konya location.

Same steps are repeated for VSC design cases with SiC-MOSFET too. **Figure 5.12 (a)** and **Figure 5.12 (b)** provides the multi-variable ΔROI optimization plots for VSC design cases with SiC-MOSFET in Konya location. While **Figure 5.12 (a)** provides the ΔROI surface plot for frequency sweep operation, **Figure 5.12 (b)** provides the ΔROI surface plot at the end of heatsink optimization.

In **Figure 5.12 (a)**, it is seen that VSC design case at 22 kHz switching frequency achieves the highest ΔROI value in a wide range of ΔC_s values. Although 32 kHz switching frequency provides the highest ΔROI value when ΔC_s value falls to 60 USD level, 22 kHz switching frequency provides the highest ΔROI value in a wide range of ΔC_s values. This is better seen in **Figure 5.13** where the ΔROI vs ΔC_s curves are provided for several frequencies between 20 kHz and 30 kHz. As seen in **Figure 5.13**, 22 kHz switching frequency (yellow curve) provides the highest ΔROI value when ΔC_s value is between 70 USD and 200 USD. Thus, heatsink optimization is conducted for 22 kHz design case.

As clearly seen in **Figure 5.12 (b)**, the optimized design at 22 kHz provides a far higher ΔROI value compared to other VSC designs at other switching frequencies.

Figure 5.13 approves this result too. Black dashed line in **Figure 5.13** shows that the optimized VSC design case at 22 kHz provides the highest ΔROI value in all ΔC_s values for VSC design cases with SiC-MOSFET module in Konya location.

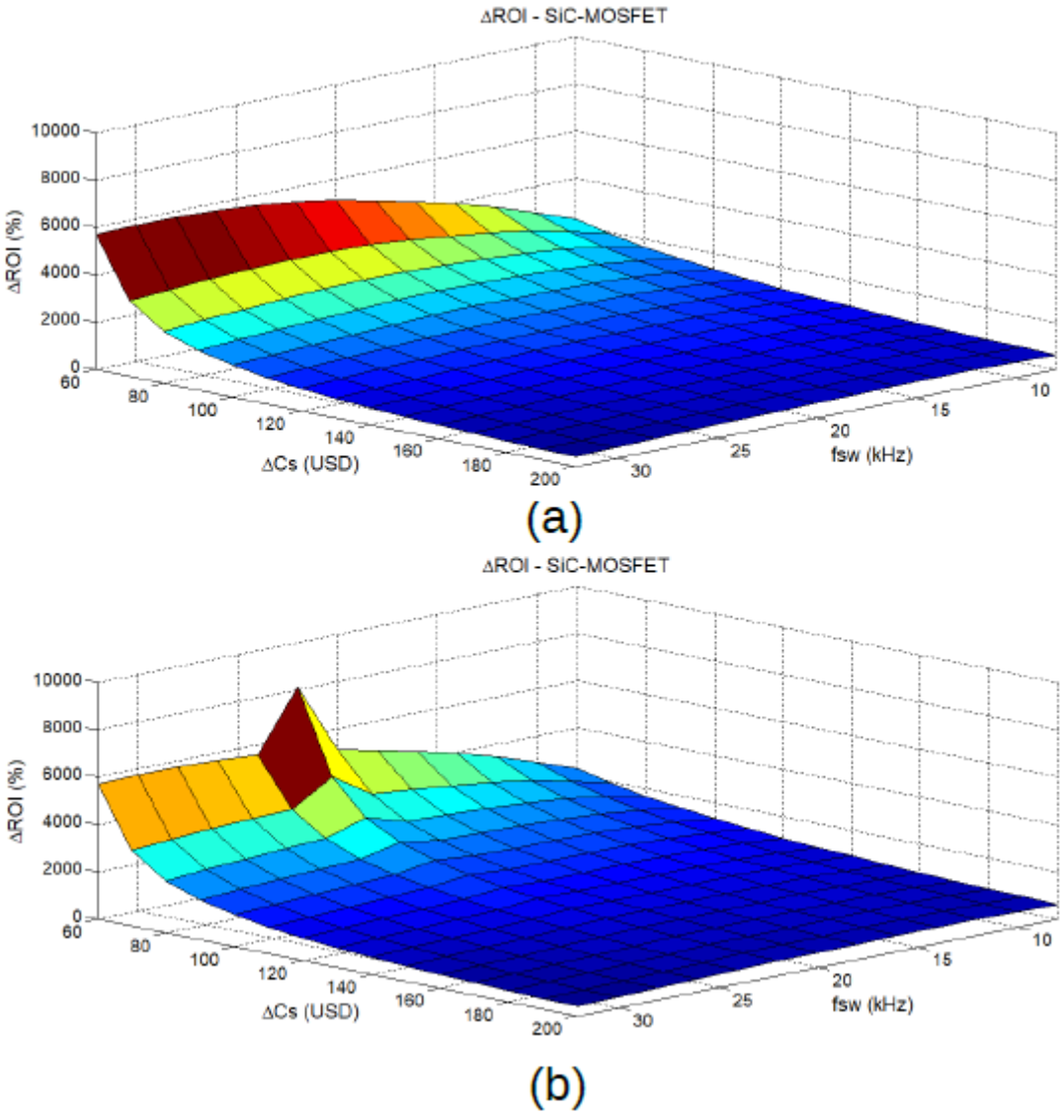


Figure 5.12 Multi-variable ΔROI optimization plots for VSC designs with SiC-MOSFET module in Konya location. (a) f_{sw} sweep plot. (b) Heatsink optimized plot.

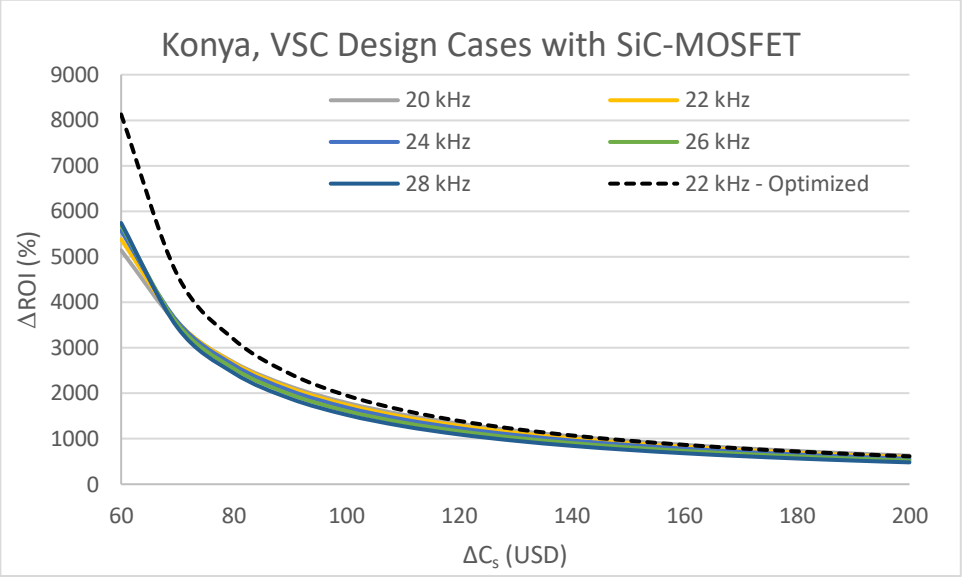


Figure 5.13 ΔROI vs ΔC_s curves for VSC designs with SiC-MOSFET module at various switching frequencies in Konya location.

For the SiC-MOSFET cases, it is apparent that case 2 (f_{sw}= 8 kHz) improves the ΔROI via heatsink size reduction. But f_{sw} of 8 kHz is too low for such devices. On the other hand, case 3 (f_{sw}= 32 kHz) has too high f_{sw} reducing the efficiency and ΔROI. Thus, similar to H-IGBT cases, case 3 can be enhanced by reducing f_{sw} from 32 kHz to 22 kHz and improving nominal efficiency. In this case, the heatsink temperature falls from 72 ˚C to 66 ˚C. Therefore, heatsink size is reduced with another iteration and 80 ˚C nominal heatsink temperature is restored achieving the optimum solution.

In order to compare H-IGBT and SiC-MOSFET technologies, their ΔROI vs ΔC_s curves are compared for their ΔROI optimized design cases. **Figure 5.14** provides their ΔROI optimized curves in the same graph. In present market conditions, VSC design with H-IGBT achieves 936.84% ΔROI value whereas VSC design with SiC-MOSFET achieves only 613.30% ΔROI value. The difference between ΔROI values at present market conditions is defined in equation (5.16) and denoted by $\Delta\Delta ROI_{Present}$. It is found as 323.54% for Konya location. Thus, H-IGBT is economically more favorable in present market conditions in Konya location.

$$\Delta\Delta ROI_{Present} = \Delta ROI_{Present(H-IGBT)} - \Delta ROI_{Present(SiC-MOSFET)} \quad (5.16)$$

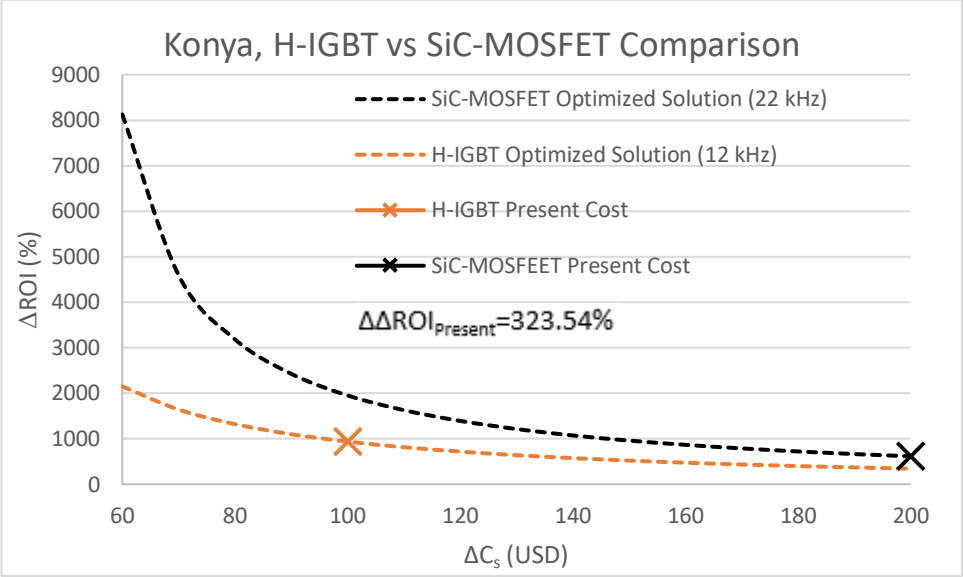


Figure 5.14 Comparison of ΔROI-optimized design solutions with H-IGBT and SiC-MOSFET modules in Konya location.

However, if ΔC_s value is equal for both H-IGBT and SiC-MOSFET modules, SiC-MOSFET module achieves a higher ΔROI value in the entire cost range. In addition, switching frequency of ΔROI-optimized VSC design with SiC-MOSFET is at 22 kHz whereas this value is only 12 kHz for VSC design with H-IGBT module. Since switching frequency of design with SiC-MOSFET is almost twice of design with H-IGBT, design with SiC-MOSFET has an advantage in size and weight of the product and provides higher portability and technical service convenience.

As also clearly seen in **Figure 5.14**, ΔROI of VSC design with SiC-MOSFET shows an exponential increase when the ΔC_s falls below 100 USD level. After this point, ΔROI value of VSC design with SiC-MOSFET is at least twice of the ΔROI value of VSC design with H-IGBT. Thus, obviously, SiC-MOSFET technology will have a huge advantage over H-IGBT technology in case SiC-MOSFET prices fall rapidly at some point and catch the H-IGBT prices.

Another comparison between H-IGBT and SiC-MOSFET technologies is shown in **Figure 5.15**. While ΔROI optimization surface plot of H-IGBT is limited up to 100 USD ΔC_s value and 16 kHz f_{sw} value, surface plot of SiC-MOSFET extends up to 200

USD ΔC_s value and 32 kHz f_{sw} value. As seen in **Figure 5.15**, SiC-MOSFET achieves a higher ΔROI value for whole ΔC_s range when price of H-IGBT and SiC-MOSFET is same (as also observed in **Figure 5.14**). It is also observed in **Figure 5.15** that optimum switching frequency of H-IGBT is 12 kHz (1.5 times of Si-IGBT technology) whereas it is 22 kHz for SiC-MOSFET (almost 3 times of Si-IGBT technology). General opinion in the industry about SiC-MOSFETs also favors three times switching frequency compared to Si-IGBT technology. So, in this analysis, outcome of exhaustive search is found to be compatible with expert knowledge.

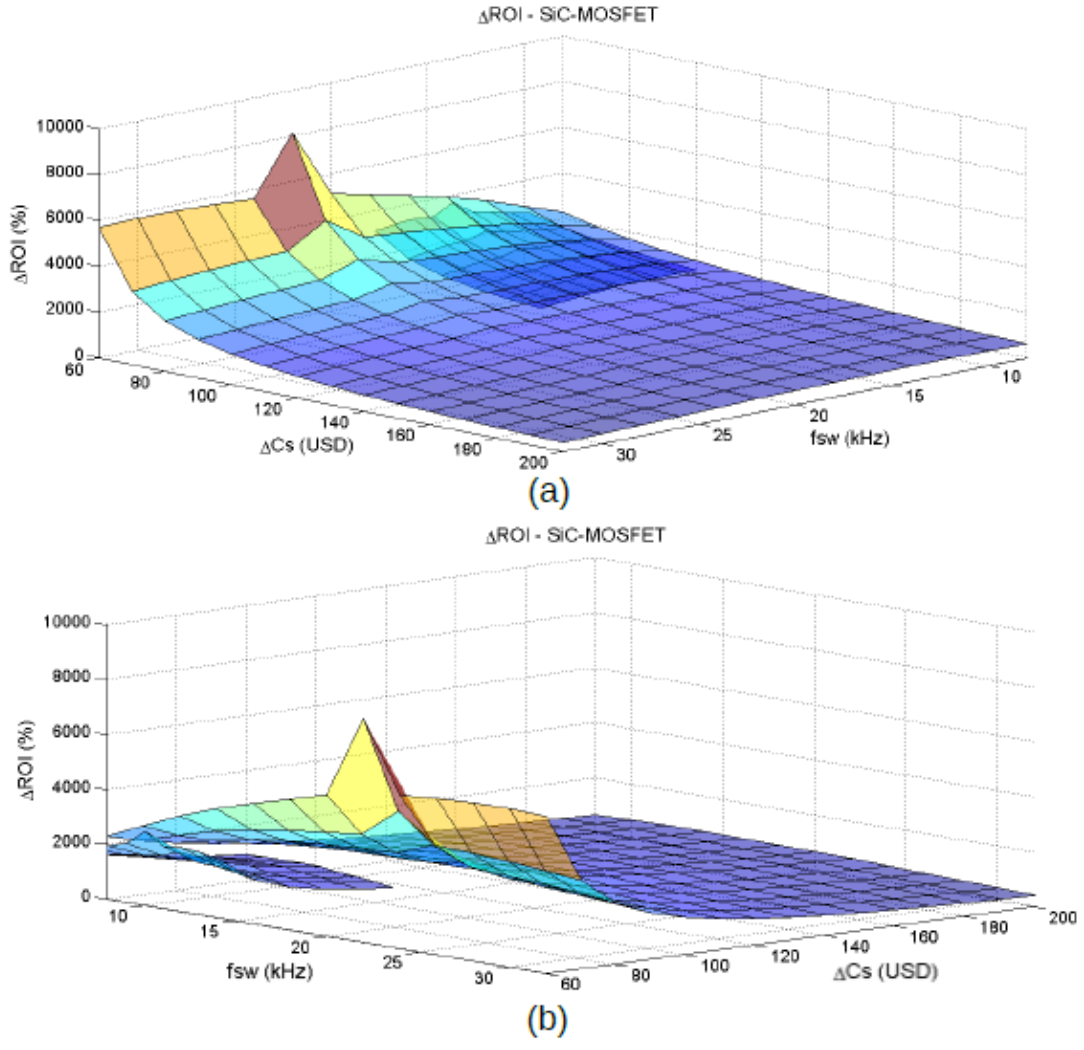


Figure 5.15 Comparison of ΔROI-optimized surface plots of VSC designs with H-IGBT and SiC-MOSFET modules for Konya location. (a) Original view. (b) 90° clockwise rotated view.

5.7.3.2. ΔROI Optimization for Palermo

Same design optimization process is repeated for Palermo location too. While **Figure 5.16** – **Figure 5.17** provide the optimization graphs for VSC designs with H-IGBT module, **Figure 5.18** – **Figure 5.19** provide the optimization graphs for VSC designs with SiC-MOSFET modules in Palermo location.

Figure 5.16 (a) shows the ΔROI surface plot at the end of frequency sweep for design cases with H-IGBT and **Figure 5.16 (b)** shows the ΔROI surface plot at the end of heatsink optimization. In **Figure 5.16 (a)**, it is observed that 12 kHz f_{sw} value provides the highest ΔROI value in a wide range of ΔC_s values. This is better seen in **Figure 5.17** where the ΔROI vs ΔC_s curves are plotted for several frequencies between 8 kHz and 16 kHz. **Figure 5.17** shows that 12 kHz f_{sw} (gray curve) provides the highest ΔROI value in Palermo location when ΔC_s is between 55 USD and 95 USD. Thus, further heatsink optimization is conducted for 12 kHz design case.

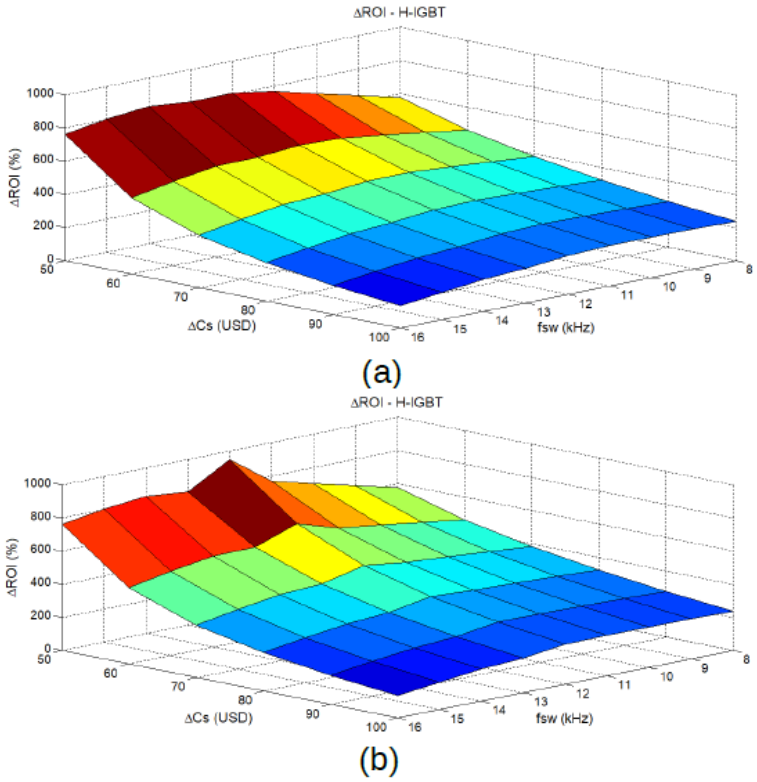


Figure 5.16 Multi-variable ΔROI optimization plots for VSC designs with H-IGBT module in Palermo location. (a) f_{sw} sweep plot. (b) Heatsink optimized plot.

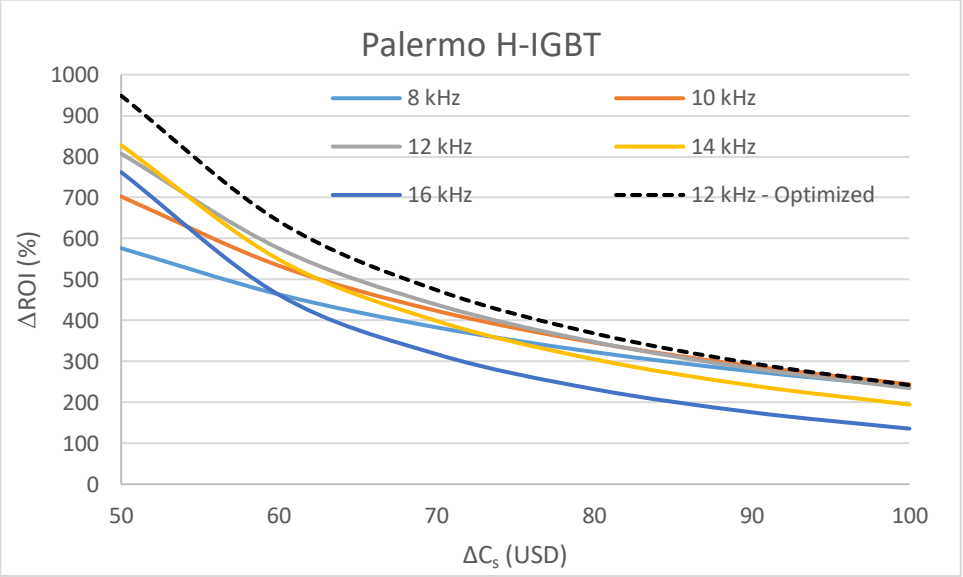


Figure 5.17 ΔROI vs ΔC_s curves for VSC designs with H-IGBT module at various switching frequencies in Palermo location.

As clearly seen in **Figure 5.16 (b)**, the design case at 12 kHz with heatsink optimization provides the best ΔROI value compared to other VSC designs at other switching frequencies in Palermo. **Figure 5.17** approves this result too. As seen with black dashed line in **Figure 5.17**, heatsink optimized design case at 12 kHz provides the highest ΔROI value in all ΔC_s values among all VSC design cases with H-IGBT module in Palermo location.

Again, same optimization procedure is repeated for VSC design cases with SiC-MOSFET module. **Figure 5.18 (a)** shows the ΔROI surface plot at the end of frequency sweep operation and **Figure 5.18 (b)** provides the ΔROI surface plot at the end of heatsink optimization for VSC designs with SiC-MOSFET in Palermo location. In **Figure 5.18 (a)**, it is seen that VSC design case at 22 kHz f_{sw} achieves the highest ΔROI value in a wide range of ΔC_s values. Although higher switching frequencies towards 32 kHz provide higher ΔROI values when ΔC_s falls to 60 USD level, 22 kHz switching frequency provides the highest ΔROI value in a wide range of ΔC_s values. **Figure 5.19** shows it in a better way with the ΔROI vs ΔC_s curves for several frequencies between 20 kHz and 30 kHz. As seen in **Figure 5.19**, 22 kHz switching

frequency (yellow curve) provides the highest ΔROI value when ΔC_s is between 70 USD and 180 USD. Thus, further heatsink optimization is conducted for 22 kHz design case.

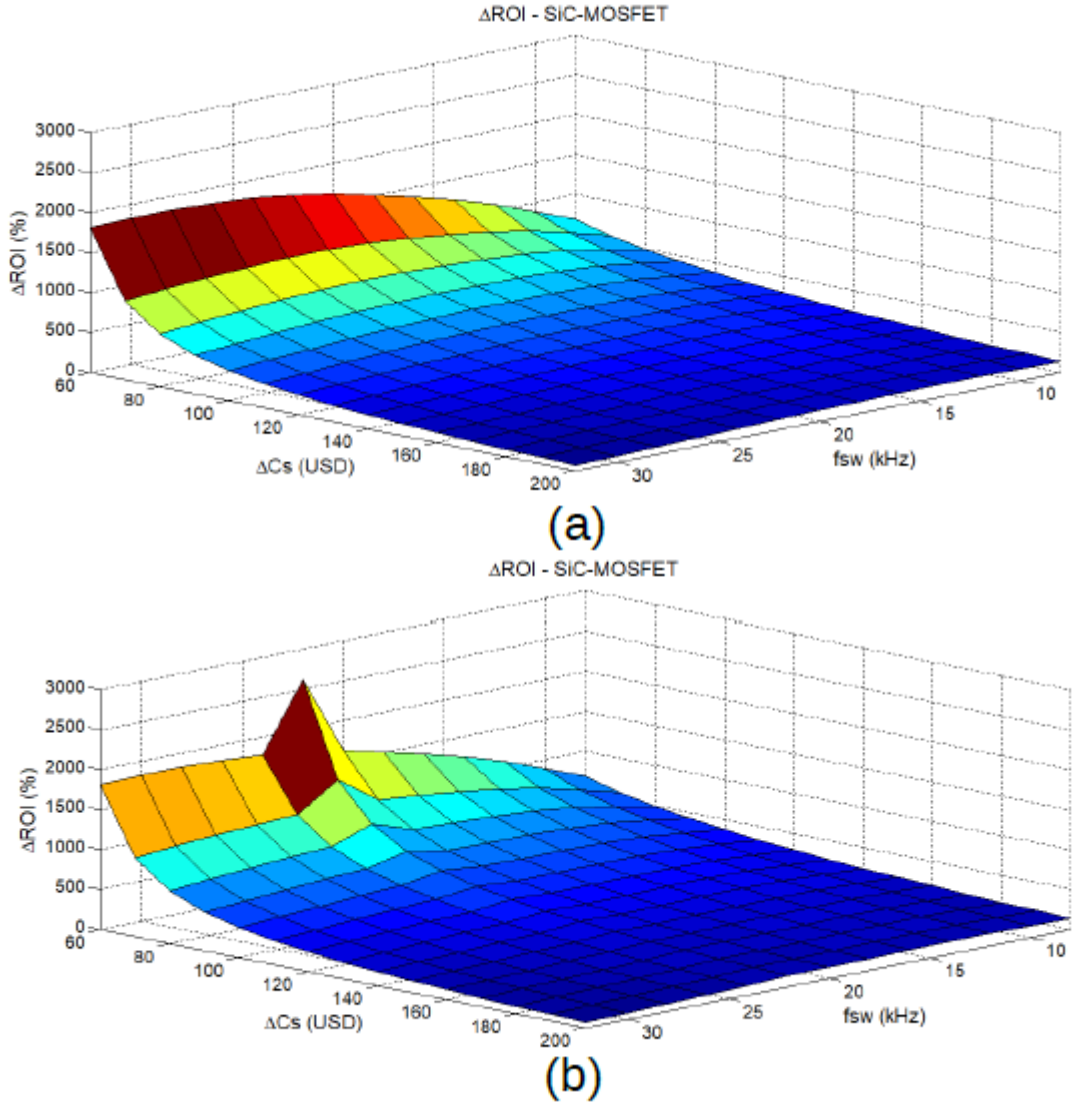


Figure 5.18 Multi-variable ΔROI optimization plots for VSC designs with SiC-MOSFET module in Palermo location. (a) f_{sw} sweep plot. (b) Heatsink optimized plot.

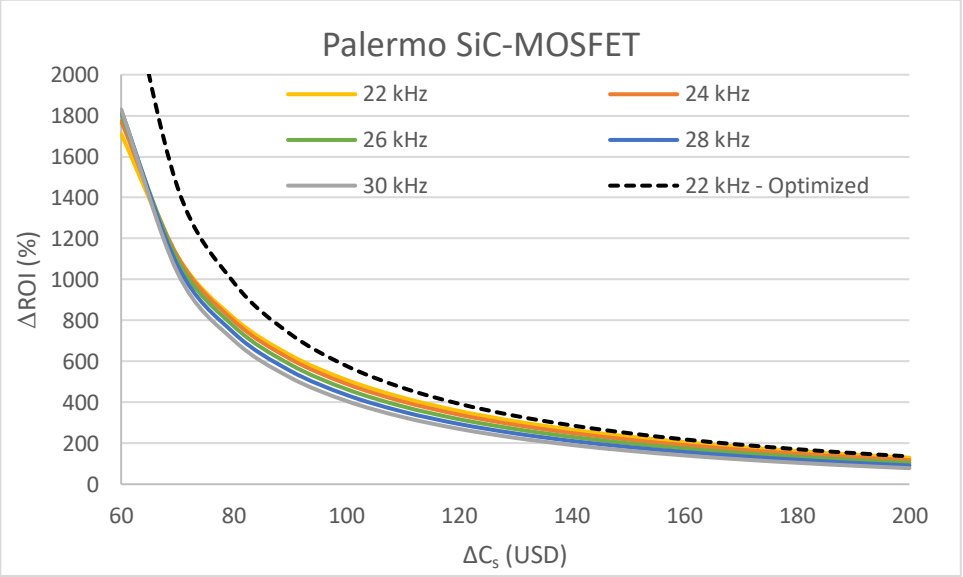


Figure 5.19 ΔROI vs ΔC_s curves for VSC designs with SiC-MOSFET module at various switching frequencies in Palermo location.

As clearly seen in **Figure 5.18 (b)**, the optimized design at 22 kHz provides a far higher ΔROI value compared to other VSC designs at other switching frequencies in Palermo location. Black dashed line in **Figure 5.19** also shows that the optimized VSC design case at 22 kHz provides the highest ΔROI value in all ΔC_s values for VSC design cases with SiC-MOSFET module in Palermo location.

Just like Konya location, ΔROI vs ΔC_s curves of VSC design cases with H-IGBT and SiC-MOSFET technologies can be compared in Palermo location too for their ΔROI optimized design cases. **Figure 5.20** provides ΔROI-optimized curves of VSC designs with H-IGBT and SiC-MOSFET in the same graph. In present market conditions, VSC design with H-IGBT achieves 242.07% ΔROI value whereas VSC design with SiC-MOSFET achieves only 135.69% ΔROI value. Thus, $\Delta\Delta ROI_{Present}$ value is 106.38% for Palermo location. Thus, again, H-IGBT is more favorable economically in present market conditions in Palermo location. However, lower FIT value in Palermo (compared to Konya) resulted in a lower $\Delta\Delta ROI_{Present}$ value. Thus, the difference between H-IGBT and SiC-MOSFET solutions is smaller in Palermo location.

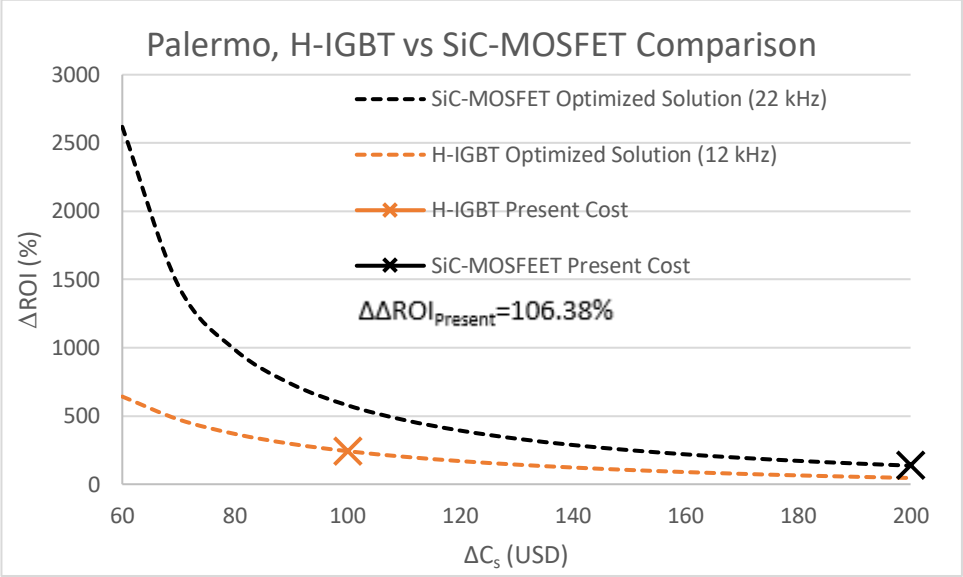


Figure 5.20 Comparison of ΔROI-optimized design solutions with H-IGBT and SiC-MOSFET modules in Palermo location.

However, just like Konya location, if ΔC_s is equal for both H-IGBT and SiC-MOSFET modules, SiC-MOSFET module achieves a higher ΔROI value in the entire cost range in Palermo too. And still, f_{sw} of ΔROI-optimized VSC design with SiC-MOSFET is at 22 kHz whereas it is only 12 kHz for VSC design with H-IGBT module. Since f_{sw} of SiC-MOSFET design is almost twice of H-IGBT design, it has an advantage in size and weight of the product and provides higher portability and technical service convenience.

5.7.3.3. Extension of ΔROI Optimization to a Wide Power Range

Although ΔROI optimization procedure by exhaustive research is completed for a 30-kW VSC design for PV power plant applications in Konya and Palermo, this optimization procedure can be applied to a wider power range. As mentioned earlier, thanks to differential TCO approach, only semiconductor module, heatsink, and inductors are taken into account in cost analysis of a PV converter. Thus, optimization procedure can be easily extended to a wide power range taking the costs of these components into account.

As shown in **Table 5.1**, semiconductor costs are defined as per ampere values. Therefore, in the same voltage level (1200 V), semiconductor costs can be accepted as linearly proportional with ampere. For inductance, same principle also applies. If percent ripple is assumed to be constant in different power ranges, cost of inductor can be considered as linearly proportional with ampere. For convenience, heatsink cost is also assumed to be linearly proportional with ampere. In this way, thanks to scalable structure of heatsink and inductor, obtained results for Konya and Palermo for 30-kW VSC application can be extended to a wider power range.

Equation (5.17) shows the normalized equation of cost difference analysis. If it is assumed that costs of semiconductor, heatsink, and inductor are linearly proportional with rated current of the VSC, then ΔTCO_k analysis can be conducted with the normalized version of converter cost of k^{th} VSC design case which is shown with $C_{VSC\text{-}k(Normalized)}$ in equation (5.17). Similarly, semiconductor cost can also be normalized with reference semiconductor cost ($C_{s\text{-}REF}$) which is equal to the total semiconductor cost of the reference VSC design with Si-IGBT module. Equation (5.18) shows the normalized version of semiconductor cost ($C_{s\text{-}k(Normalized)}$).

$$C_{VSC-k(Normalized)} = \frac{C_{VSC-REF} + \Delta C_{VSC-k}}{C_{VSC-REF}} \tag{5.17}$$

$$C_{s(Normalized)} = \frac{C_s + \Delta C_s}{C_s} \tag{5.18}$$

Assuming that the annual energy harvest and annual yield values do not significantly change with the power rating of the PV converter in the analyzed 1-MW PV power plant, ROI curves of the optimized VSC design cases with H-IGBT and SiC-MOSFET modules can be also plotted w.r.t. the normalized semiconductor cost ($C_{s(Normalized)}$). **Figure 5.21** and **Figure 5.22** provides the ROI curves of the optimized VSC designs with H-IGBT and SiC-MOSFET modules w.r.t. $C_{s(Normalized)}$ in Konya and Palermo respectively.

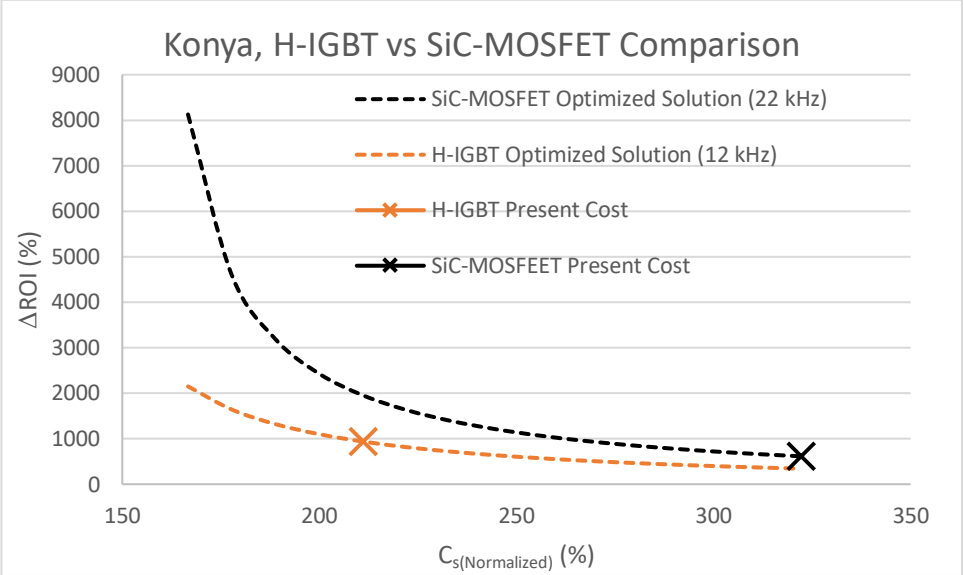


Figure 5.21 ΔROI vs $C_{s(Normalized)}$ curves in Konya.

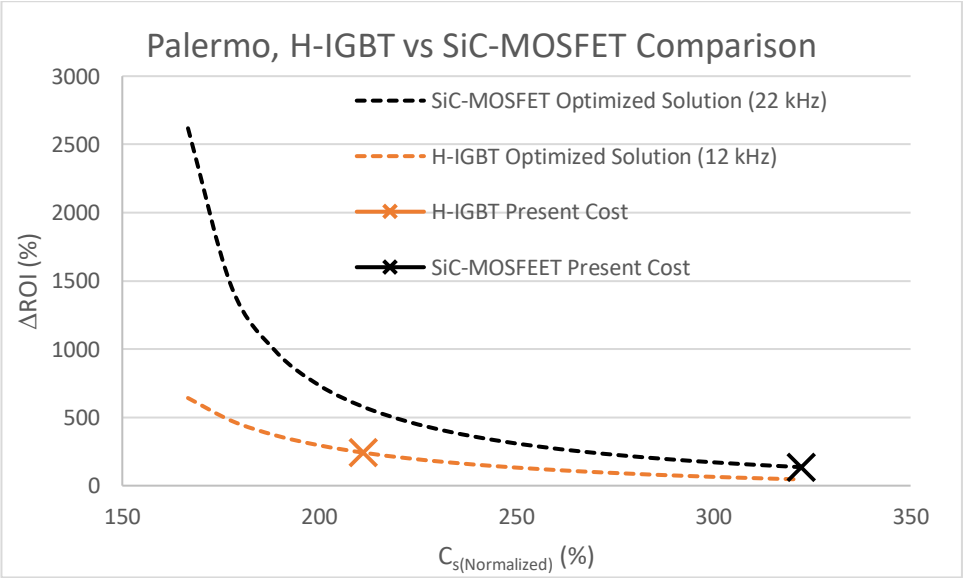


Figure 5.22 ΔROI vs $C_{s(Normalized)}$ curves in Palermo.

Sting PV converters are available in 10 kVA – 150 kVA power range and with developing manufacturing skills and enhanced PCB designs, power density and layout quality of the PV converter designs continuously keep improving. In this way, rated power of string PV converters is inclined to increase. Thanks to their high portability and modularity, compact string PV converters with 100 kVA or more rated power

rating can be a good alternative to big bulky central PV converters in PV power plant application. In these aspects, extension of outcomes of this economic assessment to high power string PV converters above 100 kVA is an essential property.

5.8. Conclusion

In this chapter, economic assessment of the four design cases which are presented in Chapter 4 is completed. ROI and PP are taken as the basic criteria for the economic assessment. Four proposed design cases for a 30-kW grid-connected PV converter with both H-IGBT and SiC-MOSFET modules are evaluated through a 1-MW PV power plant application. The economic assessment is completed in six different locations and different geographic conditions and FIT values. Moreover, a design optimization process is proposed, and further design optimizations are conducted to maximize the ROI value in Konya and Palermo locations.

It is essential to imply that all the economic assessment conducted in this chapter assumed that lifetime of the PV power plant is 20 years. For lower lifetime, these ROI cannot be realized. Thus, manufacturing technology of the PV converters and a reliable design has a crucial role in economic evaluation of a grid-connected VSC through a PV power plant application. In these aspects, lifetime of H-IGBT and SiC-MOSFET modules should be proven just like Si-IGBT technology to trust on the results of economic assessment conducted in this chapter.

It is seen that irradiance and FIT value has an enormous effect on economic success of an investment on PV converters in solar farm applications. It is shown that the higher the irradiance and FIT values achieve shorter PP and higher ROI values. In the same conditions, a PV power plant investment in Konya achieves the highest ROI values because it has the highest FIT value. On the other hand, Palermo achieves the highest ROI values among the three cities in Italy (Palermo, Napoli, Milano) with same FIT value due to its high irradiance. In these aspects, importance of location on economic performance of a solar farm application is shown.

As clearly seen in **Figure 5.10**, **Figure 5.12**, **Figure 5.16**, and **Figure 5.18**, ROI values increases as cost difference w.r.t. the Si-IGBT module decreases. This is an expected result. In addition, it is clearly seen there are optimum switching frequencies where maximum ROI values are reached. While a lower switching frequency results in a higher inductor cost, a higher switching frequency decreases the efficiency and energy harvest. Thus, an economic assessment should be conducted based on the cost of the converter and annual yield of the PV power plant to find the optimum switching frequency for highest ROI value.

Based on the basic four cases and additional optimized VSC design cases, it can be seen that the H-IGBT solution has a low f_{sw} limit where the SiC-MOSFET option provides almost twice f_{sw} which gives a smaller and lighter design. This reduces the real estate and cooling cost contributing to better TCO. While the optimum switching frequency for highest ROI value is found as 12 kHz for VSC designs with H-IGBT module, it is found as 22 kHz for VSC designs with SiC-MOSFET modules in Konya and Palermo locations. Based on this comparison, it is understood that SiC-MOSFET module has better switching capabilities than H-IGBT modules. Although optimum switching frequency for highest ROI value may change by various parameters such as irradiance, FIT, semiconductor cost difference and so on, roughly it can be noted that H-IGBT and SiC-MOSET technologies allow increasing switching frequency approximately 1.5 times and 3 times respectively compared to Si-IGBT technology in grid-connected three-phase VSC designs.

In order to evaluate the optimum designs with H-IGBT and SiC-MOSFET modules, there are two approaches. For the same cost difference w.r.t. the Si-IGBT module, it is apparent that the optimum VSC design with SiC-MOSFET provides better ROI as its ROI curve is always above the ROI curve of optimum VSC design with H-IGBT. However, for the current market condition, the cost difference between H-IGBT and SiC-MOSFET modules favors the H-IGBT as it is quoted at significantly lower price. For the SiC-MOSFET option to compete with the H-IGBT option, the SiC-MOSFET

module cost must be decreased such that the cost difference between the SiC-MOSFET and H-IGBT modules is less than 50 USD level.

Another comparison can be made with reference to Si-IGBT option. It is apparent from all ROI vs cost difference w.r.t. the Si-IGBT module graphs, when the cost difference w.r.t Si-IGBT decreases to less than approximately 100 USD, both technologies yield exponential ROI improvement, with the SiC-MOSFET solution being the best. Therefore, these graphics point out to the end of the Si-IGBT era.

CHAPTER 6

CONCLUSION

In this thesis, techno-economical assessment of low-voltage (380 V AC – 400 V AC) grid-connected three-phase VSCs is completed through a 1-MW PV power plant application. The benefits of techno-economical design are specifically illustrated via a three-phase grid-connected 30-kW PV converter system. As major contribution, with the evolution of new generation wide bandgap devices, techno-economic assessment of VSC designs with H-IGBT and SiC-MOSFET semiconductor modules is covered in comparison with the conventional VSC designs with Si-IGBT modules. Eventually, an insight is given about the techno-economical feasibility of employing H-IGBT and SiC-MOSFET semiconductor modules in VSC designs for grid-connected PV converters at present market conditions. Moreover, scenarios for possible future market conditions are also mentioned.

Technically, design of a 30-kW VSC converter is carried out through the study including the topology selection, semiconductor sizing, heatsink sizing and inductor sizing. First, a detailed comparison is provided between two-level VSC topology configurations depending on the midpoint connection of DC bus voltage. Possible residual current problems due to common-mode components are examined taking safety standards of grid-connected PV converters into account and half-bridge topology is chosen due to its superior characteristics in suppressing common-mode ground leakage current components. Second, a loss calculation algorithm is developed to calculate semiconductor losses and carry out efficiency calculations. Using the calculated losses and efficiency values, a steady-state thermal analysis is completed to size semiconductor module and heatsink properly. Lastly, depending on the determined switching frequency, inductor design is completed with powder core inductors. An algorithm is developed to calculate core losses. Moreover, copper losses

are also calculated taking the skin effect and proximity effect into account. In this way, a complete efficiency calculation is carried out.

Sizing of semiconductors, heatsink, and magnetic components (inductors) are shown through a reference design example with conventional Si-IGBT technology. The design is verified by both simulations and experiments. Then, the reference design with conventional Si-IGBT module is retrofitted with H-IGBT and SiC-MOSFET modules. Four design cases are proposed at various switching frequencies taking the industry know-how into account. In all proposed design cases, the switching frequency and inductance product is kept constant. As both heatsink and inductor components are selected in scalable structures, they are easily re-sized in each design step. Two of these proposed designs are verified experimentally for both H-IGBT and SiC-MOSFET modules.

After verification of the VSC design cases technically, cost analysis of proposed VSC design cases is carried out. In order to conduct an economic assessment based on the cost differences between proposed VSC designs with Si-IGBT, H-IGBT, and SiC-MOSFET modules, a cost differential approach is followed. Only the cost differences between semiconductor, heatsink and inductor components are taken into cost difference analysis. In this way, cost differences between proposed VSC design cases are calculated. These values are later used in economic assessment of the VSC designs.

As electrical energy is the main outcome that is sold to the utility grid in PV power plant applications, economic assessment of the proposed designs is carried out according to the annual energy harvest of the PV power plant. Six different locations are determined for economic assessment and same PV plant configuration is used in all locations. Inclination of PV modules is optimized in each location to maximize energy harvest. Eventually, annual energy harvest of PV power plant is estimated via PV simulations with proposed VSC designs and annual yield is calculated using the FIT value of each location specifically.

After calculation of PV converter cost differences and the annual energy harvest differences of each VSC design case, economic assessment relation between annual yield difference and cost difference between VSC designs is mathematically formulated and numerically assessed. This relation is defined with the term ΔROI (differential return on investment) and further design optimization is sought for highest ΔROI by exhaustive search in a wide range of switching frequencies and semiconductor cost difference values. Based on the economic assessment results obtained with six different locations and three different power module technologies, the obtained results are evaluated, and the following outcomes are obtained:

- At present market conditions, it is observed that H-IGBT technology is already an economically feasible investment in locations with high irradiance and high FIT value (Konya in this study). However, in locations with low irradiance, neither H-IGBT nor SiC-MOSFET solutions can provide economically feasible solutions. As an example, in this study, it is observed that VSC design with H-IGBT (case 2 design) in Konya location achieves 1006% ΔROI value whereas same design in Palermo achieves only 265% ΔROI value. This shows that there may be a significant difference between ΔROI values for same design in different locations. Although the irradiance level is similar for Konya and Palermo, different FIT values cause a significant ΔROI difference in these designs. Another example can be given as design case 4 with SiC-MOSFET module. This design case achieves a positive ΔROI value only in Konya (31%) due to high irradiance and high FIT value. In all the other locations, this design results in negative ΔROI values.
- At present market conditions, SiC-MOSFET cannot be competitive against H-IGBT due to its high initial cost. Although designs with SiC-MOSFET modules can provide higher efficiency and higher annual yield, their high cost degrades their investment value economically at present conditions. Their main benefit is size and weight reduction, and only when such benefits overweight the differential energy harvesting advantage, they can be practical.

- In 30-kW application, with the prices of H-IGBT and SiC-MOSFET falling, especially when the price difference w.r.t. the Si-IGBT module becomes less than 100 USD, it is observed that ΔROI values exponentially increase, pointing to the end of Si-IGBT era. If a wider power range is considered, this 100 USD cost difference corresponds a semiconductor cost which is approximately 200% of initial semiconductor cost. Cost gain achieved by reducing the size of inductors with increasing switching frequency is only economically feasible when costs of H-IGBT and SiC-MOSFET modules get lower. In this specific 30-kW VSC application, it is observed that optimum switching frequency for H-IGBT is 1.5 times higher than switching frequency of conventional Si-IGBT solution for maximum ΔROI value. On the other hand, optimum switching frequency for SiC-MOSFET module is observed as almost 3 times of conventional Si-IGBT solution for maximum ΔROI value.
- The race between the H-IGBT and SiC-MOSFET will favor the latter when the price difference between the two diminishes. The SiC-MOSFET solution in this case does not only maximize the ROI, but also reduces the size and weight of the converter bringing real estate and additional advantages. However, current market forecasts show that no major price reduction is expected in SiC-MOSFET modules in the coming 5 years. Thus, H-IGBT may be the dominant semiconductor technology for a period of 10 years between 2020 and 2030 in grid-connected VSC designs.

While the results of this study are shown for 30-kW system for on-grid PV applications, the approach can be easily generalized to other grid-connected VSC applications with premium energy efficiency such as UPS rectifiers, wind-turbine converters, active filters and so on. Thanks to scalability of the components used in the VSC structure and easy parallel connection of grid-connected converters, results of this study can be easily extended to other grid-connected VSCs in 10 kVA – 150 kVA power range.

At the end of the economic assessment in this thesis, it is observed that Si-IGBT era is already coming to an end. H-IGBT technology is expected to be the dominant semiconductor technology in the next 10 years and SiC-MOSFET technology is expected to replace H-IGBT technology after 10 years. Thus, new VSC designs should seriously consider employing H-IGBT and SiC-MOSFET semiconductor modules in their designs. In these aspects, such an economic assessment with design optimization provided in this thesis is necessary at pre-design stage for an environment-friendly and a competitive product design.

As future work, optimization criteria may be changed as power density and a similar optimization procedure can be repeated for VSC designs. The aim of higher switching frequency and smaller product size in the optimization can result in different outcomes. In addition, three-level or any other VSC topologies/configurations can be also techno-economically investigated. In three-level topologies, 600 V GaN devices can be also used in addition to the 1200 V SiC devices. In these aspects, such a study can cover the economic feasibility GAN devices too in three-level VSC topologies.

REFERENCES

[1] BP Energy Outlook, 2018 Edition, BP Energy Economics, 2018, pp.46.

[2] "Hybrid Microgrids", Northern Power Systems (NPS), http://www.northernpower.com/energy-storage/system-designhybrid-microgrids/ [Accessed: March 07, 2019].

[3] IRENA (2018), Renewable capacity statistics 2018, International Renewable Energy Agency (IRENA), Abu Dhabi.

[4] Republic of Turkey Ministry of Energy and Natural Resources, 2019 [online] Available: https://www.enerji.gov.tr/tr-TR/Sayfalar/Gunes [Accessed: Feb 27, 2019].

[5] Sudipta Chakraborty, Marcelo G. Simões and William E. Kramer, "Power Electronics for Renewable and Distributed Energy Systems: A Sourcebook of Topologies, Control and Integration", Springer, 2013.

[6] G. Stryi-Hipp, "The effects of the German renewable energy sources act (EEG) on market, technical and industrial development", 19th European Photovoltaic Solar Energy Conference, Paris, 7-11 June 2004.

[7] M. Jain, V. Rustagi, "Inverter Design and Selection", India Solar Excellence, BRIDGE TO INDIA Energy Private Limited, 2018.

[8] Z. Ozkan, A.M. Hava, "Three-phase inverter topologies for grid-connected photovoltaic systems", Conference Records of IPEC Hiroshima 2014, pp. 498-505, May 2014.

[9] Kantar, E., Hava, A.M.: Design of grid connected PWM converters considering topology and PWM methods for low voltage renewable energy applications. In: Proceedings of IPEC Hiroshima, Japan, 2014, 18–21 May 2014.

[10] R. Teichmann, S. Bernet, "A comparison of three-level converters versus two-level converters for low voltage drives traction and utility applications", IEEE Trans. Ind. Applicat., pp. 855-865, May/June 2005.

[11] IEEE Std 519™-2014, IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems, 2014.

[12] J. Millan, P. Godignon, X. Perpina, A. Perez-Tomas, J. Rebollo, "A survey of wide bandgap power semiconductor devices", IEEE Trans. Power Electron., vol. 29, no. 5, pp. 2155-2163, 2014.

[13] R. Takeda, “Wide Bandgap Power Device Evaluation Challenges and Technologies”, Keysight Technologies, November 2016.

[14] “The question is: Who really needs GaN or SiC Power Devices”, Alex Avron, PntPower.com, Published on December 8, 2016, https://www.pntpower.com/question-really-needs-gan-sic-power-devices/, [Accessed: March 26, 2019].

[15] M. Liserre, F. Blaabjerg, and A. Dell’Aquila, “Step-by-step design procedure for a grid-connected three-phase PWM voltage source converter”, International Journal of Electronics, vol. 91, no. 8, pp. 441–460, Aug 2004.

[16] A. Nabae, I. Takahashi, H. Akagi, "A new neutral-point clamped PWM inverter", IEEE Trans. Ind. Appl., vol. IA-17, no. 5, pp. 518-523, 1981.

[17] N.S. Choi, J.G. Cho, G.H. Cho, "A general circuit topology of multilevel inverter", Power Electronics Specialists Conference 1991. PESC ’91 Record. 22nd Annual IEEE, pp. 96-103, 24-27 Jun 1991.

[18] A.M. Hava, R.J. Kerkman, T.A. Lipo, "Carrier-Based PWM-VSI Overmodulation Strategies: Analysis Comparison and Design", IEEE Transactions on Power Electronics, vol. 13, pp. 674-689, July 1998.

[19] A.M. Hava, R.J. Kerkman, T.A. Lipo, "Simple Analytical and Graphical Methods for Carrier-Based PWM-VSI Drives", IEEE Transactions On Power Electronics, vol. 14, no. 1, 1999.

[20] J. W. Kolar, H. Ertl, F. C. Zach, "Influence of the modulation method on the conduction and switching losses of a PWM converter system", Conf. Rec. 25th IEEE IAS Annu. Meeting, pp. 502-512, Oct. 1990.

[21] M. Liserre, F. Blaabjerg, and S. Hansen, "Design and control of an LCL-filter-based three-phase active rectifier," IEEE. Trans. Industrial Applications, vol. 41, pp. 1281-1291, 2005.

[22] B.G. Cho, S.K. Sul, “LCL Filter Design for Grid-connected Voltage-source Converters in High Power Systems,” IEEE. Trans. Industrial Applications, pp. 1548 – 1555, 2012.

[23] J. Dannehl, F.W. Fuchs, S. Hansen, and P.B. Thogersen, "Investigation of Active Damping Approaches for PI-Based Current Control of Grid-Connected Pulse Width Modulation Converters with LCL Filters," IEEE. Trans. Industrial Applications, vol. 46, pp. 1509-1517, 2010.

[24] S. G. Parker, B. P. McGrath, and D. G. Holmes, "Regions of Active Damping Control for LCL Filters" IEEE Trans. Ind. App., 2012-IPCC-463.

[25] Y. Tang, P. C. Loh, P. Wang, F. H. Choo and F. Gao, "Exploring inherent damping characteristics of LCL-filters for three-phase grid-connected VSI," IEEE Trans. Power Elec., vol. 27, no. 3, pp. 1433-1443, Mar. 2012.

[26] J. Dannehl, C. Wessels, and F.W. Fuchs, “Limitations of voltage-oriented PI current control of grid-connected PWM rectifiers with LCL-filters”, IEEE Trans. Ind. Electron., vol. 56, no. 2, pp. 380–388, Feb. 2009.

[27] J. Mookken, B. Agrawal, J. Liu, “Efficient and Compact 50kW Gen2 SiC Device Based PV String Inverter”, PCIM Europe 2014, 20-22 May 2014.

[28] Y. Shi, L. Wang, R. Xie, Y. Shi, H. Li, "A 60kW 3kW/kg 5-Level T-Type SiC PV Inverter with 99.2% Peak Efficiency", IEEE Trans. Ind. Electron. in press, 2017.

[29] B. Burger, D. Kranzer, "Extreme high efficiency PV-power converters", Power Electronics and Applications 2009. EPE'09. 13th European Conference on, pp. 1-13, 2009.

[30] S. Wall, X-C. Hong, L. Sha, J-R. Xie, “High-efficiency PV inverter with SiC technology”, IET Renewable Power Generation, vol. 12, issue: 2, pp. 149 – 156, Feb. 2018.

[31] “Mitsubishi Electric’s Railcar Traction Inverter with All-SiC Power Modules Achieves 40% Power Savings”, Mitsubishi Electric Corporation Public Relations Division, No.2939, 22 June 2015.

[32] U. Schwarzer, S. Buschhorn, K. Vogel, “System Benefits for Solar Inverters using SiC Semiconductor Modules”, PCIM Europe 2014, 20-22 May 2014.

[33] E. Kantar, A. M. Hava, "Optimal design of grid-connected voltage source converters considering cost and operating factors", IEEE Trans. Ind. Electron., no. 99, pp. 1-1, 2016.

[34] İ. Güneş, M. Ardıç, Am. M. Hava, “Energy savings in uninterruptible power supply systems by means of modern power conversion techniques”, 5th International Ege Energy Symposium and Exhibition (IEESE-5), 27-30 June 2010

[35] F. Cammarota, S. Sinigallia, "High-efficiency on-line double-conversion UPS", 29th Int. Telecommun. Energy Conf. (INTELEC), pp. 657-662, 2007.

[36] Y. Kalisky, “Spectroscopy and solar energy – in honor to Professor Renata Reisfeld”, Journal of Luminescence, vol. 193, pp. 10-12, January 2018.

[37] “Which solar panel type is the best? Mono- vs polycrystalline vs thin film”, Energy Informative, https://energyinformative.org/best-solar-panel-monocrystalline-polycrystalline-thin-film/, [Accessed: March 23, 2019].

[38] JKM260PP-60 poly crystalline module datasheet, Jinko Solar.

[39] “Solar cell I-V characteristics”, http://www.alternat_ve-energy-tutor_als.com/energy-art_cles/solar-cell-_-v-character_st_c.html, [Accessed: March 15, 2019].

[40] N. Mohan, T. M. Undeland, and W. P. Robbins, “Power Electronics: Converters, Applications, and Design.” 3rd Edition, John Wiley & Sons, Inc., 2002.

[41] IEC 61727:2004, Photovoltaic (PV) systems - Characteristics of the utility interface, IEC 61727 Standard, 2004.

[42] IEC 62116:2014, Utility-interconnected photovoltaic inverters - Test procedure of islanding prevention measures, IEC 62116 Standard, 2014.

[43] IEC 62109-1:2010, Safety of power converters for use in photovoltaic power systems - Part 1: General requirements, IEC 62109 Standard, 2010.

[44] IEC 62109-2:2011, Safety of power converters for use in photovoltaic power systems - Part 2: Particular requirements for inverters, IEC 62109 Standard, 2011.

[45] "Remote monitoring system", Mavi Solar Remote Monitoring System, http://www.mavisolar.com/language/en/remote-monitoring-system/, [Accessed: March 17, 2019].

[46] A. Lüthi, "Smart PV Inverters", Sputnik Engineering AG Biel/Bienne, IEA PVPS Task 14 – Utility Workshop.

[47] Feed-in-Tariff, Italy, Res-legal.eu, http://www.res-legal.eu/search-by-country/italy/single/s/res-e/t/promotion/aid/feed-in-tariff-ii-ritiro-dedicato/lastp/151/, [Accessed: April 07, 2019].

[48] Feed-in-Tariff, Italy, Prezzi minimi garantiti per l'anno 2018, https://www.arera.it/allegati/operatori/elettricita/180125tab.pdf, [Accessed: April 07, 2019].

[49] Feed-in-Tariff, Turkey, Res-legal.eu, http://www.res-legal.eu/search-by-country/turkey/single/s/res-e/t/promotion/aid/feed-in-tariff-7/lastp/207/, [Accessed: April 07, 2019].

[50] Feed-in-Tariff, Switzerland, Res-legal.eu, http://www.res-legal.eu/search-by-country/switzerland/single/s/res-e/t/promotion/aid/feed-in-tariff-1/lastp/396/ , [Accessed: April 07, 2019].

[51] Feed-in-Tariff, Estonia, Res-legal.eu, http://www.res-legal.eu/search-by-country/estonia/single/s/res-e/t/promotion/aid/premium-tariff-1/lastp/123/, [Accessed: April 07, 2019].

[52] T. Kerekes, R. Teodorescu, C. Klumpner, M. Sumner, D. Floricau, P. Rodriguez, "Evaluation of three-phase transformerless photovoltaic inverter topologies", IEEE Trans. Power Electron., vol. 24, no. 9, pp. 2202-2211, 2009.

[53] C. Hou, C. Shih, P. Cheng, A. Hava, "Common-mode voltage reduction pulse width modulation techniques for three-phase grid connected inverters", IEEE Trans. Power Electron., vol. 28, no. 4, pp. 1971-1979, 2013.

[54] E. Kantar, "Design and control of PWM converter with LCL type filter for grid interface of renewable energy systems", M.S. thesis, The Graduate School of Natural and Applied Sciences of Middle East Technical University, Ankara, July 2014.

[55] A. Wintrich, U. Nicolai, W. Tursky, T. Reimann, "Application Manual Power Semiconductors", Semikron International GmbH, 2015.

[56] AN-4166 Heatsink Mounting Guide, Fairchild

[57] AN 18-001 Thermal Paste Application, Semikron, 19.01.2018

[58] Dr. Dusan Graovac, Marco Pürschel, "IGBT Power Losses Calculation Using the Datasheet Parameters", Infineon Application Note, V1.1, January 2009.

[59] Dimensioning program IPOSIM for loss and thermal calculation of Infineon IGBT modules, Infineon.

[60] S. C. Das, G. Narayanan, A. Tiwari, "Experimental Study on the Dependence of IGBT Switching Energy Loss on DC Link Voltage", IEEE International Conference on Power Electronics Drives and Energy Systems (PEDES-2014), Dec 2014.

[61] SA155055 Savior Axial Fan Datasheet

[62] Thermal Resistance Calculator – Plate Fin Heatsink, MyHeatSink, Longwin, https://myheatsinks.com/calculate/thermal-resistance-plate-fin, [Accessed: October 07, 2018].

[63] 00K8020E026 Kool Mμ Powder Core Datasheet, Magnetics

[64] H. O. Jimenez, “Ac resistance evaluation of foil, round and litz conductors in magnetic components”, M.S. Thesis, Department of Energy and Environment, Chalmers University of Technology, Göteborg, 2013.

[65] PV*SSOL premium, R5, Valentin Software GmbH, 2016

[66] “European or CEC Efficiency”, On- Grid Inverter Efficiency Curve, PVSyst, http://files.pvsyst.com/help/inverter_euroeff.htm, [Accessed: July 14, 2019].

[67] M. Liserre, R. Teodorescu, F. Blaabjerg, "Multiple harmonics control for three-phase grid converter systems with the use of PI-RES current controller in a rotating frame", IEEE Trans. Power Electron., vol. 21, no. 3, pp. 836-841, 2006.

[68] Z. Özkan, A. M. Hava, “Current control of single phase VSC systems with inductor saturation using inverse dynamics model-based compensation”, IEEE Transactions on Industrial Electronics, vol. 66, no. 12, pp. 9268-9277, 2019.