DESIGN OF A RADIATION HARDENED PWM CONTROLLER BUILT ON SOI

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ABSTRACT

DESIGN OF A RADIATION HARDENED PWM CONTROLLER BUILT ON SOI

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Design of efficient and compact switch-mode power supplies (SMPS) is a popular topic in power electronics. Silicon has been used as semiconductor material of switches in DC-DC converters for decades. However, preference of using GaN as semiconductor material of switches in these topologies has recently increased due to their superior properties. GaN FETs have lower gate capacitance, lower channel resistance, higher frequency operation, higher breakdown voltage and higher temperature operation than silicon MOSFETs. Those properties provide increase in the efficiency of DC-DC converters and reduction in the size of filter components of them.

This thesis focuses primarily on developing an efficient DC-DC converter, and secondly a compact converter. Design of a low-power and radiation hardened PWM (Pulse Width Modulation) controller has helped the DC-DC converter in this thesis has a high

efficiency. In order to increase efficiency further, GaN devices have been used as switches because they have lower gate capacitance and channel resistance, which means lower switching and conduction losses, than those of silicon MOSFETs. On the other hand, using GaN FETs has enabled working at high frequencies in order to reduce the size of filter components and producing a compact DC-DC converter as required in most of the applications today.

The PWM controller has been designed as integrated circuit, manufactured and tested. 0.18 μm SOI (Silicon-On-Insulator) technology has been used throughout the design. The PWM controller is a current mode controller and has internal blocks which are error amplifier, SR latch, clock generator, voltage reference, current sense and inverter. Error amplifier is designed with 83.8° phase margin in order to have a stable DC-DC converter. Clock of the controller is implemented by a ring oscillator with a duty cycle adjustment circuit whose output gives a clock with duty cycle of %32 and frequency up to 10 MHz. Furthermore, it has an external pin through which an external clock signal might be given. A reference voltage of 1.27 V is produced in order to compare it with the output of the current sense block. A delay generation circuit has been designed by using inverters, which provides reduction of switching losses. Experimental results show that the PWM controller is able to drive a GaN FET, whose input capacitance is 588 pF, at 10 MHz. At this condition, the PWM controller is supplied with 5 V, and it has a power dissipation of 15 mW. Efficiency of the DC-DC converter is measured as 83.1% with 3.2 V_{DC} input. The converter also gives 3 V_{DC} output at 100 mA load with 30 V_{DC} input voltage in a closed loop configuration. The circuit shows stable operation under full-load to no-load transition. The PWM controller chip size is 2.5mm x 3mm. The controller is radiation hardened thanks to the internal resistance of SOI technology.

Keywords: PWM Controller, GaN FET, SOI, switching power converter, DC-DC converter, efficiency, switching loss, conduction loss, closed loop, radiation hardened

ÖZ

SOI TABANLI RADYASYONA DAYANIKLI PWM DENETLEYİCİ TASARIMI

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Verimli ve kompakt anahtarlamalı güç kaynağı tasarımı güç elektroniğinde popüler bir konudur. DC-DC çeviricilerdeki anahtarların yarı iletken malzemesi olarak uzun yıllardır silikon kullanılmaktadır. Ancak son zamanlarda bu devrelerde anahtar yarı iletken malzemesi olarak GaN'ın kullanımı üstün özellikleri sayesinde artmıştır. GaN FET'ler silikon MOSFET'lere göre daha düşük kapı kapasitansına, daha düşük kanal direncine, daha yüksek frekansta çalışma özelliğine, daha yüksek dayanma gerilimine ve daha yüksek sıcaklıkta çalışma özelliğine sahiptir. Bu özellikler DC-DC çeviricilerin hem verimliliğini yükseltmeye hem de filtre elemanlarının boyutlarını küçültmeye katkı sağlamaktadır.

Bu tezde öncelikli olarak verimli bir DC-DC çevirici geliştirmeye, ikinci olarak ise kompakt bir çevirici ortaya çıkarmaya odaklanılmıştır. DC-DC çeviricinin verimliliğini artırmak için düşük güç tüketimine sahip ve radyasyona dayanıklı bir PWM denetleyici

tasarlanmıştır. Bunun yanında GaN elemanlar silikon MOSFET'lere göre daha düşük kapı kapasitansına ve kanal direncine dolayısıyla daha düşük anahtarlama ve iletim kayıplarına sahip olduğu için verimliliği daha da artırmak adına anahtar olarak GaN elemanlar kullanılmıştır. Diğer taraftan tasarımda GaN FET'lerin kullanılması filtre elemanlarının boyutlarını küçültmek için yüksek frekanslara çıkmaya ve bugün birçok uygulamada gerek duyulan kompakt DC-DC çevirici üretimine izin vermiştir.

PWM denetleyici bütünleşik devre şeklinde tasarlanmış, ürettirilmiş ve testleri gerçekleştirilmiştir. Tasarımda 0.18 μm SOI teknolojisi kullanılmıştır. PWM denetleyici akım modu ile çalışır ve hata yükselteci, SR mandalı, saat üreteci, gerilim referansı, akım algılama ve invertör dahili bloklarından oluşur. DC-DC çeviricinin kararlı olması için hata yükselteci 83.8° faz payı ile tasarlanmıştır. Denetleyicinin saati, 10 MHz frekansa kadar çalışma özelliğine ve %32 görev döngüsüne sahip görev döngüsü ayarlanabilir bir halka osilatörü tarafından uygulanır. Bunun yanında dışarıdan saat sinyali vermeye yarayan bir harici bacağa da sahiptir. Akım algılama bloğunun çıkışını bir referans gerilim değeriyle kıyaslamak adına 1.27 V'luk bir referans gerilimi üretilir. Anahtarlama kayıplarını düşürmek adına invertörler yardımıyla bir gecikme yaratıcı devre tasarımı yapılmıştır. Deneysel sonuçlar PWM denetleyicinin 588 pF giriş kapasitansına sahip bir GaN FET'i 10 MHz frekansta sürebildiğini göstermiştir. Bu şartlar altında PWM denetleyici 5 V ile beslenmiş ve 15 mW güç tüketmiştir. DC-DC çeviricinin verimliliği 3.2 V_{DC} giriş gerilimi için %83.1 olarak ölçülmüştür. Çevirici aynı zamanda 30 V_{DC} giriş gerilimi için kapalı döngü yapılandırmasında çıkışından 100 mA çekilirken 3 V_{DC} çıkış gerilimi üretmiştir. Devre tam yükten yüksüz duruma geçiş esnasında kararlı bir operasyon göstermiştir. Çip boyutları 2.5mm x 3mm'dir. Denetleyici, SOI teknolojisinin radyasyona dirençli yapısından dolayı radyasyona dayanıklıdır.

Anahtar Kelimeler: PWM Denetleyici, GaN FET, SOI, anahtarlamalı güç çevirici, DC-DC çevirici, verimlilik, anahtarlama kaybı, iletim kaybı, kapalı döngü, radyasyona dayanıklı

To My Parents,

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CHAPTER 1

INTRODUCTION

1.1. Scope

The scope of this thesis is to share the results achieved during the research work about designing a low-power and radiation hardened PWM (Pulse Width Modulation) controller in order to obtain an efficient and compact GaN-based DC-DC (Direct Current-Direct Current) converter. The research work has carried on from September 2016 to August 2018. The objective of this thesis is to give detailed overview of this research work.

1.2. Background and Motivation

In the industry, almost every electronic module needs power conditioner and distributer units, and hence DC-DC converters. DC-DC converters using switching scheme require switching transistors in the circuit. These switches are ON and OFF at proper time of intervals in order to regulate output voltages properly. Besides switches, there are other components in the circuit such as capacitors, inductors and diodes. Furthermore, a PWM controller is needed for these circuits in order to give PWM pulses. Circuit schematic of a basic buck-type DC-DC converter is shown in Figure 1.1. This is only a representative schematic.

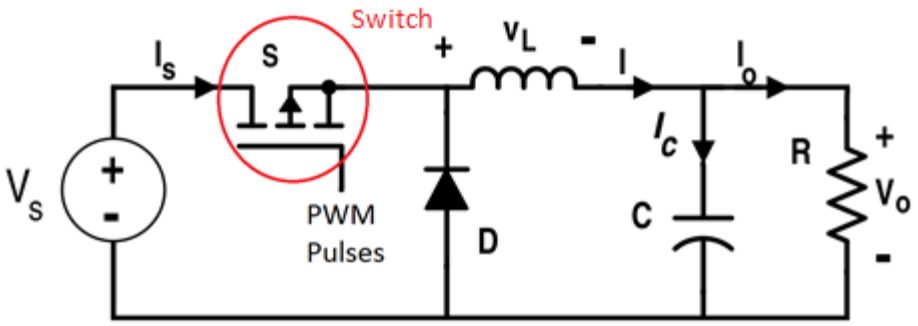


Figure 1.1: Schematic of a Buck Converter

Demand in obtaining high efficiency in these converters increases day by day. In order to have high efficiency, losses in these circuits should be minimized. There are some loss mechanisms in converters, namely losses of circuit components, switching loss and conduction loss. Losses of components are heat dissipation due to their internal resistance. Switching loss occurs during switching time intervals due to non-instantaneous commutation times. It depends on the rise and fall times of the PWM pulses, which are mainly determined by the gate capacitance of the switching transistors. Conduction loss is the heat dissipation across switching transistors due to their channel resistance. These losses should be kept as low as possible in order to design an efficient DC-DC converter.

Main focus of this thesis is to design an efficient DC-DC converter. In order to achieve this goal, primary objective has been selected as designing a low-power PWM controller. PWM controller in this thesis has been designed as IC (integrated circuit). In order for it to dissipate less power, gate capacitances of the transistors inside the IC have been kept as low as possible by size optimization by choosing W (width) and L (length) values as small as possible. Second, number of components inside the IC has been kept as low as possible. Third, layout of the controller has been optimized in order to avoid parasitic capacitances developed within the IC. Finally, a delay generator circuit has been designed and added in order to reduce switching losses across switching transistors of the DC-DC converter.

In order to further increase efficiency, GaN devices has been chosen for switching transistors in the DC-DC converter because they have superior properties over silicon [1], [2]. Silicon MOSFETs (Metal Oxide Semiconductor Field Effect Transistors) have widely been used in DC-DC converters as switches throughout the years because they are reliable and their production have become standard [3]. However, III-V semiconductor materials have started to become popular recently. These materials have a lot of advantages over silicon. Among these materials, especially GaN (Gallium Nitride) has begun to be used in DC-DC converters.

As the gate charge of GaN FETs (Field Effect Transistors) is low, their gate capacitance is smaller than silicon MOSFETs [4]. This means that switching losses can be reduced simply by replacing silicon MOSFETs with GaN FETs. Furthermore, channel resistance of GaN FETs are smaller than silicon MOSFETs [5]. This leads to lower conduction losses. Combining all of these, efficiency of DC-DC converters can be increased by choosing GaN FETs as switches even if they are operated at high frequencies. Therefore, second objective for obtaining an efficient DC-DC converter in this thesis was using GaN devices as switching transistors. This has reduced switching and conduction losses, and increased efficiency.

The main focus of this thesis was obtaining an efficient DC-DC converter. The second focus was designing a compact converter having small filter components. DC-DC converters are requested to be small in size, thin and compact in most of the applications; however, big filter components such as capacitors and inductors prevent those converters from meeting these requirements. Since silicon has small band gap, it has high gate charge and output capacitance, and cannot operate at high frequencies [6]. Therefore, filter components remain large if silicon MOSFETs are used in converters. However, GaN is a wide band gap material so it has lower gate charge and output capacitance, and can operate at high frequencies [7]. Furthermore, higher electron saturation velocity of GaN allows for higher operating frequencies. Comparison of electron saturation velocities between silicon and GaN is given in Table 1.1 [8]. That is why it is possible to reduce the size of filter components if GaN FETs are used as switches in these circuits. Therefore,

using GaN FETs in this thesis has also helped the author reduce the size of filter components in the DC-DC converter.

Table 1.1: Comparison of Electron Saturation Velocities of Silicon and GaN

	Silicon	**GaN**
Saturated (peak) electron velocity (10^7 cm/s)	1.0 (1.0)	1.3 (2.7)

In reality, there is a trade-off between efficiency and size of converters. In order to reduce the size of converters, switching frequency should be increased. However, increasing frequency also increases switching losses. Therefore, a technology change from silicon to GaN was required in this thesis in order to obtain high efficiency while switching at high frequency levels. Furthermore, an optimal frequency has been selected in order not to reduce efficiency too much.

GaN has other advantages than providing high efficiency and compact filter design. Since GaN FETs have wide band gap and high potential barrier, their leakage current is smaller than that of silicon MOSFETs at the same temperature level. This allows GaN FETs to be operated at very high temperature levels. [9]

Another advantage of GaN FETs is that they have high breakdown voltage. Therefore, they can withstand high voltage and power levels. That is why they are preferred in high voltage and power applications. Breakdown field of silicon and GaN is compared in Table 1.2. [8]

Table 1.2: Comparison of Breakdown Fields of Silicon and GaN

	Silicon	**GaN**
Breakdown Field (MV/cm)	0.3	3.5

Besides all of these, GaN is an attractive material in space industry because it is inherently radiation hardened. "GaN Reliability Enhancement and Technology Transfer Initiative" (GREAT2 project, ESTEC contract. no.21.499/08/NL/PA) has some results about radiation sensitivity of GaN. Tests examining the effects of total ionizing dose (TID), proton radiation (displacement damage) and single event burn-out (SEB) effects under heavy ions have been conducted both on UMS GH50-10 and UMS GH25-10 MMIC processes. Protons with energy 35 MeV up to a fluence of 1.5 x 10^{12} protons/cm^2 have been used. The total dose applied was 1 Mrad, with a dose rate of 36 krad/h. Both processes were irradiated with heavy ions Ar, Kr and Xe to test for single event effects (SEE) and single event burn-out (SEB) voltage threshold values. For UMS GH50-10 process, TID effects and proton irradiation resulted in less than 10 % change in key parameters like saturation current, maximum transconductance and threshold voltage. Under heavy ion excitation (Xenon: LET_{GaN} = 52.93 MeV/mg/cm^2) some small drift (~10%) was observed in open channel current (Idss) and threshold voltage (V_t) for UMS GH50 devices, but still passing the target drift specification of ≤15%. Overall, for the UMS GH50 process, initial tests have shown that the DC static burnout occurred between 180 V to 200 V, while under heavy ion excitation single event burnout (SEB) typically occurred in the range of 125 V to 150 V and is correlated with the breakdown performance of a particular wafer batch. For UMS GH50-10 process, TID effects and proton irradiation resulted in less than 10 % change in key parameters like saturation current, maximum transconductance and threshold voltage. SEB of GaN-HEMT radiation test structures under Xe irradiation, with a LET of 53 MeV/mg/cm², occurred at 130 V to 140 V, whereas DC static burn-out occurred between 165 V and 205 V. All of these test results shows

that GaN is inherently radiation hardened, while silicon needs some extra processes and hermetic packages to become space qualified. Thereof, GaN is widely preferred in space industry both for this reason and for all other advantages. [10], [11]

Since GaN has all of the advantages mentioned above, it has been used as switching transistor material in this thesis. In the industry, there are excessive number of PWM controllers driving silicon MOSFETs [12]-[15]. However, those controllers cannot be used for driving GaN FETs as they cannot reach high frequencies. Therefore, it is seen that there is a lack of PWM controllers designed for controlling GaN FETs in the industry. The low-power PWM controller designed in this thesis has been aimed to close the gap in the industry.

While designing the PWM controller, one important point was the type of GaN FET used. There are normally-on (depletion) models [16] as well as normally-off (enhancement) models [17] of these FETs. Early GaN transistors were introduced in 2000s. Conventional GaN transistors operates in normally-on state, which means that a negative gate voltage is required in order to turn-off the device. Due to safety concerns of designers, normally-off models of GaN FETs were developed later. Latter ones operate similar to conventional enhancement mode silicon MOSFETs. In this way, know-how about silicon MOSFETs can easily be applied to normally-off GaN FETs. There are also cascode structures bringing silicon MOSFET and normally-on GaN FET together for pseudo-normally-off operation. Therefore, PWM controller should be appropriate for the GaN FET that is used. I (current) – V (voltage) characteristics of different types of GaN FETs can be seen in Figure 1.2. In this thesis, a normally-off GaN FET has been used. [18], [19]

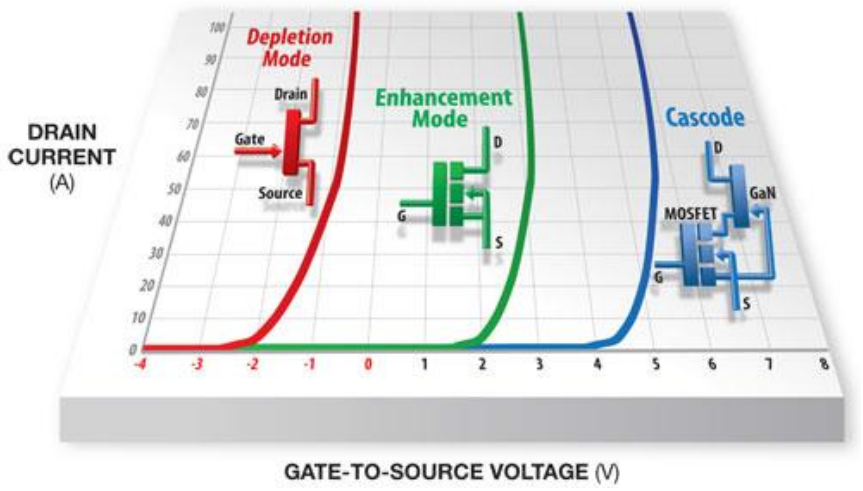


Figure 1.2: I-V Characteristics of Different Types of GaN FETs [18]

The PWM controller that has been designed in this thesis is an integrated circuit and have similar characteristics as the controllers appropriate for silicon MOSFETs. However, this integrated circuit operates at high frequencies and capable of driving GaN FETs. For this purpose, SOI (Silicon-On-Insulator) technology has been used during the design of this controller. In this technology, parasitic capacitances that are produced within the circuit are smaller [20]. Therefore, it allows the circuit to operate at high frequencies. Moreover, SOI is an inherently radiation hardened technology as GaN. Advanced SOI technology is considered to have inherent resistance to transient ionizing radiation effects and SEE (Single Event Effects) thanks to its buried insulating oxide layer. However, BOX (Buried Oxide) layer may introduce some problems about TID, especially in FDSOI (Fully Depleted Silicon-On-Insulator). [21], [22]

TID causes threshold voltage shift and leakage current increase in SOI MOSFETs. In modern FDSOI processes, threshold voltage shift and off-state leakage current are mainly due to thick BOX and field oxide. This problem may be overcome with thin gate oxide layers. Further improvements may be done in order to decrease the effects of TID. In modern radiation applications, innovative methods have been used for that purpose. Some of these methods are detailed as below. [21]

Material Modification: By introducing deep electron traps into the buried oxide to compensate hole traps, standard SOI wafers can be modified to be total dose tolerant wafers. [21]

Device Structure Innovation: With the help of a shallow source and a deep drain, the innovated BUSFET (Body Under Source FET) structure has been proposed to reduce radiation-induced back-channel leakage without using hardened BOX. [21]

Back-gate Biased Double SOI: A new method DSOI (Double-SOI) has just been proposed to improve total dose tolerance of SOI devices. With the help of back-gate biasing to force an external electric field to depress back-channel formation during total dose irradiation. [21]

In terms of SEE, SOI is more resistant than bulk CMOS (Complementary Metal Oxide Semiconductor) technology. Single event benefit of SOI over bulk can be viewed as follows;

- Bulk drains are the most sensitive areas in CMOS circuits since they collect charge most efficiently.
- Placement of an insulator beneath a fully-bottomed junction (i.e., SOI) truncated this charge collection and an ion could not deposit sufficient charge in the limited drain depletion region as shown in Figure 1.3. [22]

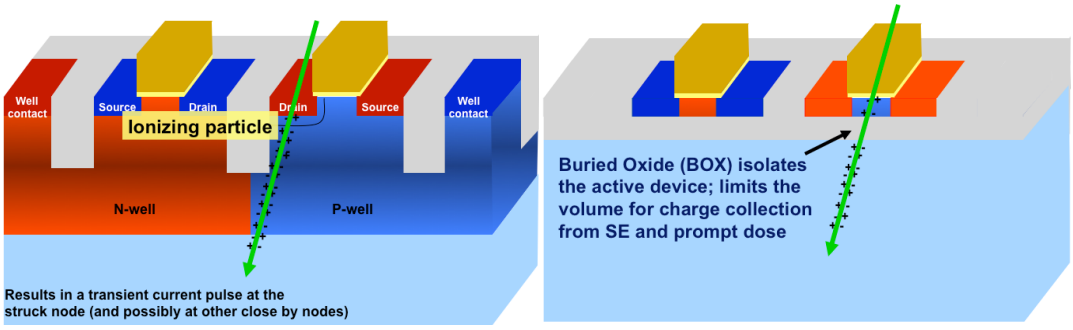


Figure 1.3: Single Event Effects on Bulk and SOI Devices [22]

Besides, SEL (Single Event Latch-up) is not seen in SOI due to its internal structure with BOX [23]. For these advantages, it is preferred in space industry. Fabrication of standard silicon bulk CMOS technology and FDSOI can be seen in Figure 1.4.

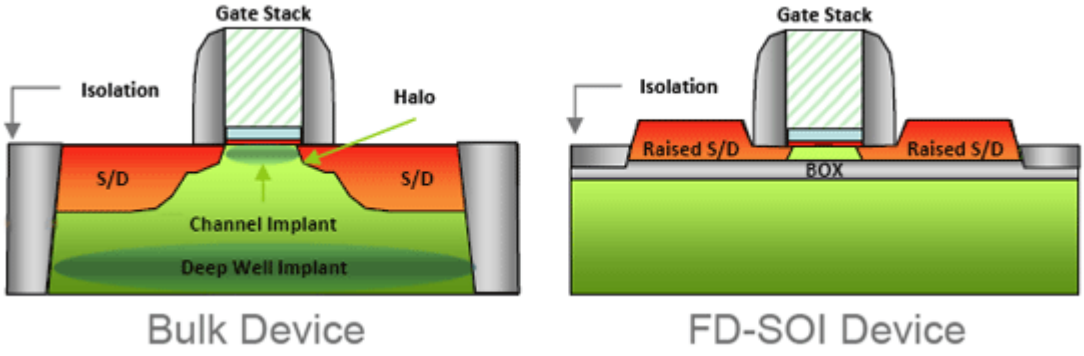


Figure 1.4: Fabrication of Standard Silicon CMOS and SOI [24]

In Figure 1.5, schematic of a PWM controller controlling a buck converter is shown. Again, this is only a representative schematic. As one can see from Figure 1.5, PWM controller adjusts duty cycle of the pulses it produces by getting feedback from output of the DC-DC converter. This circuit is a closed loop feedback system; therefore, stability of the circuit is important.

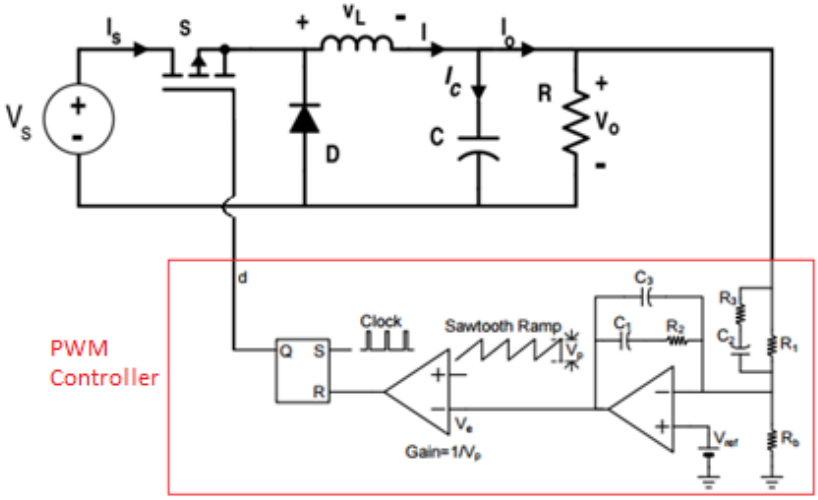


Figure 1.5: Schematic of PWM Controller

1.3. Project Objectives

The primary objective of this thesis is to design an efficient DC-DC converter. To this end, design considerations and methods for producing a low-power PWM controller is demonstrated. Besides, application of GaN devices in DC-DC converters for obtaining high efficiency is investigated and tested.

The second major objective of this thesis is to study and design a compact DC-DC converter by increasing switching frequency. For this purpose; a frequency determination study has been conducted in order to find optimal frequency value, and GaN and SOI technologies have been investigated and applied in order to reach that frequency level.

In this chapter, reasons of choosing the subject of this thesis are considered. Aim and motivation about this work are mentioned. A background information about the subject and how this information should be used in order to realize the objectives of this thesis are given. In the next chapter, some preliminary studies conducted before skipping to analysis and design phase are considered.

CHAPTER 2

PRELIMINARY STUDY

2.1. Design Considerations for Low-Power PWM Controller

The primary objective of this thesis is to design an efficient GaN-based DC-DC converter. In order to increase efficiency, power dissipation of the PWM controller has been minimized. 0.18 μm SOI technology has been utilized during design of the PWM controller, and supply voltage of this technology is 5 V. In order to reduce the losses due to PWM controller, current drawn from this supply has been kept as small as possible. This is achieved through some design techniques stated below.

First, PWM controller is a mixed-signal device including both analog and digital parts. The transistors inside the controller whose gates are encountered with digital signals are prone to draw instantaneous currents during switching instants. This current is proportional with gate capacitance of the transistors as stated in

$$I = C\ \frac{dV}{dt} \tag{2.1}$$

where, *I* is instantaneous current drawn by the transistor, *C* is the gate capacitance and *dV/dt* is instantaneous rate of voltage change. In order to reduce this current, gate capacitances of these transistors have been reduced by size optimization. Gate capacitance of a MOSFET in triode region is

$$C_{gs} = C_{gd} = \frac{1}{2}C_{ox}WL + C_{ov} \tag{2.2}$$

$$C_g = C_{gs} + C_{gd}. \tag{2.3}$$

On the other hand, gate capacitance of a MOSFET in saturation region is

$$C_{gs} = \frac{2}{3}C_{ox}WL + C_{ov} \tag{2.4}$$

$$C_{gd} = C_{ov} \tag{2.5}$$

$$C_g = C_{gs} + C_{gd} \tag{2.6}$$

where, C_g is gate capacitance, C_{gs} is gate-to-source capacitance, C_{gd} is gate-to-drain capacitance, C_{ox} is oxide capacitance per unit area, W is the width of the transistor, L is the length of the transistor and C_{ov} is overlap capacitance. C_{ox} depends on the material and thickness of the oxide layer. Therefore, only adjustable parameters are W and L in order to control gate capacitance. In this thesis work, L values of the transistors have been chosen as their lowest possible value, which is 0.5 μm for the transistors used in this work. Then, W values have been adjusted according to design specifications of PWM controller blocks.

Second, number of components in the PWM controller has been kept as few as possible because more components means more current drawn from the supply. Error amplifier block of the PWM controller has been consisted of 2 stages, and an output stage has not been placed inside it because there was not any unintended responses in simulations observed without an output stage. Furthermore, some extra functionalities like UVLO (Under Voltage Lock-Out) or hysteresis between turn-on and turn-off voltage have not been utilized in order not to increase power dissipation of the PWM controller, and hence to reduce efficiency of the DC-DC converter.

Third, parasitic capacitances within the IC have been tried to be kept as low as possible because they cause unexpected instantaneous currents drawn from the supply according to equation (2.1) again. Although SOI technology provides low parasitic capacitances thanks to its buried oxide layer, some extra precautions have been taken by applying some layout techniques. Capacitance value between two metal layers is

$$C = \varepsilon \frac{A}{d} \tag{2.7}$$

where, ε is the permeability of the material used, A is the overlapped area between two metal layers and d is the distance between the layers. During the design of the PWM controller, 2 metal layers have been used. In order to reduce parasitic capacitances developed within the chip, overlapped area between these metal layers has been kept as small as possible. In order to do that components have been placed in a sequence as they have in their schematics. In order to avoid winding routes, all components have been placed in a compact manner. This manner has shorten the lengths of metal routes leading to lower voltage drops across them and lower power dissipation due to lowered route resistances. Furthermore, metal layers have been drawn by avoiding overlaps in crossing areas as much as possible. If unavoidable, overlap areas have been kept as small as possible by reducing the widths of the routes on these areas.

Finally, a delay generator circuit has been designed in the PWM controller in order to reduce switching losses across GaN FETs in the DC-DC converter. During turn-on and turn-off transition times, an unwanted current might flow through the switching transistors in DC-DC converters. This phenomenon occurs during the time that both high-side and low-side transistors are on. Switching loss area is shown in Figure 2.1. In order to reduce this loss, a delayed response of these transistors is required. To this end, a delay generator circuit, whose details are given in later chapters in this thesis, has been designed in order to increase the time gap between beginnings of turn-on/off times of the transistors.

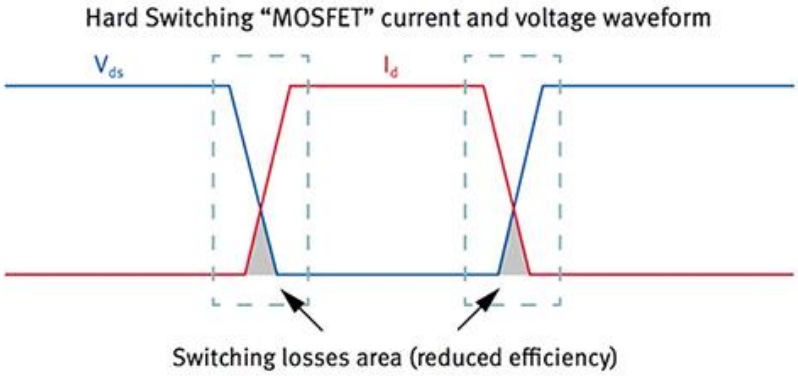


Figure 2.1: Switching Loss Area [25]

2.2. Determination of Operating Frequency

2.2.1. GaN FETs

In order to determine the operating frequency of the DC-DC converter designed in this thesis, a review has been conducted about GaN FETs in the industry. In this way, a know-how about which frequency levels are suitable for the GaN FETs has been gained.

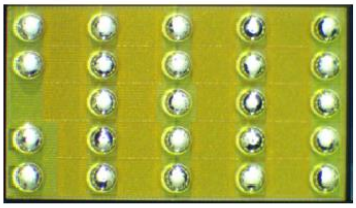
There are some companies providing GaN FETs that are suitable for space applications. Some of them are given in this thesis [26]-[28]. Since the power supply of a satellite might give high voltage levels, a transient voltage that can appear on the switching FET should be taken into account during switching times. Therefore, it is appropriate to select a switch that can withstand high voltage levels for space applications. Furthermore, it is good to choose a FET whose $R_{DS(ON)}$ (Drain-to-Source Resistance) and input/output capacitances are low in order to reduce losses and increase operating frequency.

The first company producing GaN FETs is EPC. Some portion of the datasheet of EPC2034 [26], which is an enhancement mode power transistor, can be seen in Figure 2.2. V_{DS} (Drain-to-Source Voltage) limit of EPC2034 is 200 V, maximum $R_{DS(ON)}$ value is 10 mΩ, input capacitance is 940 pF and output capacitance is 530 pF.

EPC2034 – Enhancement Mode Power Transistor
Preliminary Specification Sheet

Status: Engineering
Features:

- V_{DS}, 200 V
- Maximum $R_{DS(on)}$, 10 mΩ
- I_D, 31 A
- Pb-Free (RoHS Compliant), Halogen Free



EPC2034 – Enhancement Mode Power Transistor
Preliminary Specification Sheet

DYNAMIC CHARACTERISTICS

Parameter		Conditions	Typical Value
C_{ISS}	Input Capacitance	V_{DS} = 100 V, V_{GS} = 0 V	940 pF
C_{OSS}	Output Capacitance		530 pF
C_{RSS}	Reverse Transfer Capacitance		5 pF
R_G	Gate Resistance		0.5 Ω
Q_G	Total Gate Charge	V_{DS} = 100 V, I_D = 20 A, V_{GS} = 5 V	8.5 nC
Q_{GS}	Gate to Source Charge	V_{DS} = 100 V, I_D = 20 A	2.6 nC
Q_{GD}	Gate to Drain Charge		1.4 nC
$Q_{G(th)}$	Gate Charge at Threshold		1.8 nC
Q_{OSS}	Output Charge	V_{DS} = 100 V, V_{GS} = 0 V	80 nC
Q_{RR}	Source-Drain Recovery Charge		0

T_J = 25 °C unless otherwise stated
Specifications are with Substrate shorted to Source

Figure 2.2: Datasheet of EPC2034 [26]

The second company is GaN Systems. Some portion of the datasheet of GS66508T [27], which is an enhancement mode GaN transistor, can be seen in Figure 2.3. V_{DS} limit of GS66508T is 650 V, $R_{DS(ON)}$ value is 55 mΩ at 25 °C, input capacitance is 260 pF and output capacitance is 65 pF.

GS66508T
Top cooled 650V enhancement mode GaN transistor
Preliminary Datasheet

Features
- 650V enhancement mode power switch
- Top cooled configuration
- Ultra low FOM Island Technology™ die
- Low inductance GaN*PX*™ package
- Reverse current capability
- Dual gate pads for optimal board layout
- Zero reverse recovery loss
- RoHS 6 compliant

GS66508T
Top cooled 650V enhancement mode GaN transistor
Preliminary Datasheet

Drain-to-Source On Resistance (T_J=25°C)	$R_{DS(on)}$	55	mΩ	V_{GS}=6V, T_J=25°C, I_D = 9A
Drain-to-Source On Resistance (T_J=150°C)		140	mΩ	V_{GS}=6V, T_J=150°C, I_D = 9A

Input Capacitance	C_{ISS}	260	pF	V_{DS}=400V, V_{GS}=0V, f=1MHz
Output Capacitance	C_{OSS}	65		
Reverse Transfer Capacitance	C_{RSS}	2.0		
Effective Output Capacitance, Energy Related (note 3)	$C_{O(ER)}$	88	pF	V_{GS}=0V, V_{DS}=0 to 400V
Effective Output Capacitance, Time Related (note 4)	$C_{O(TR)}$	143	pF	I_D=const., V_{GS}=0V, V_{DS}=0 to 400V
Total Gate Charge	$Q_{G(TOT)}$	5.8	nC	V_{GS}=0 to 6V, V_{DS}=400V
Gate-to-Source Charge	Q_{GS}	2.1	nC	
Gate-to-Drain Charge	Q_{GD}	1.8	nC	
Reverse Recovery Charge	Q_{RR}	0	nC	
Output Charge	Q_{OSS}	57	nC	V_{GS}=0V, V_{DS}=400V
Turn On Delay	$t_{d(on)}$	4.1	ns	V_{DD}=400V, V_{GS} = 6V, I_D = 16 A, R_G=5Ω, T_J=25 °C (note 5)
Rise Time	t_r	3.7	ns	
Turn Off Delay	$t_{d(off)}$	8	ns	
Fall time	t_f	5.2	ns	
Turn On Delay	$t_{d(on)}$	4.3	ns	V_{DD}=400V, V_{GS} = 6V, I_D = 16 A, R_G=5Ω, T_J=125 °C (note 5)
Rise Time	t_r	4.9	ns	
Turn Off Delay	$t_{d(off)}$	8.2	ns	
Fall time	t_f	3.4	ns	

Figure 2.3: Datasheet of GS66508T [27]

GS66508T has lower input/output capacitance values than the ones of EPC2034 [26], [27]. Therefore, GS66508T can reach higher frequency levels. From Figure 2.3, the maximum operating frequency for this transistor can be calculated as

$$t_{d(on)} = 4.1 \text{ ns} \quad (2.8)$$

$$t_r = 3.7 \text{ ns} \quad (2.9)$$

$$t_{d(off)} = 8 \text{ ns} \quad (2.10)$$

$$t_f = 5.2 \text{ ns} \quad (2.11)$$

$$\text{Total wasted time} = 21 \text{ ns} \quad (2.12)$$

$$\text{Operating frequency} < 47 \text{ MHz}. \quad (2.13)$$

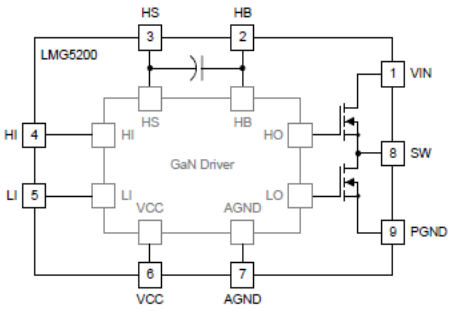
The third company producing GaN FETs is Texas Instruments. However, Texas Instruments does not produce GaN FETs separately but they produce it with their driver integrated. Some portion of the datasheet of LMG5200 [28], which is a GaN half-bridge power stage, can be seen in Figure 2.4. Input voltage limit of LMG5200 is 80 V, maximum $R_{DS(ON)}$ value is 18 mΩ, total gate charge is 3.8 nC and output capacitance is 225 pF.

GaN TECHNOLOGY PREVIEW
LMG5200 80-V, GaN Half-Bridge Power Stage

1 Features

- Input Voltage up to 80-V DC
- Integrated 80-V, 18-mΩ, GaN FETs
- Optimized Pinout for Easy PCB Layout
- Internal Bootstrap Supply Voltage Clamping to Prevent GaN FET Overdrive
- Supply Rail Undervoltage Lockout
- Independent High-Side and Low-Side TTL Logic Inputs
- Fast Propagation Times (29.5 ns Typical)
- Excellent Propagation Delay Matching (2 ns Typical)
- Low Power Consumption

Simplified Application



POWER STAGE					
$R_{DS(on)HS}$	High-side GaN FET on-resistance	I_{OUT} = 5 A, V_{VCC} = 5 V, T_J = 25°C	14	18	mΩ
$R_{DS(on)LS}$	Low-side GaN FET on-resistance	I_{OUT} = 5 A, V_{VCC} = 5 V, T_J = 25°C	14	18	mΩ
V_{SD}	GaN 3rd quadrant conduction drop	I_{SD} = 500 mA, VIN floating, V_{VCC} = 5 V, HI, LI low	2		V
$I_{L\text{-}VIN\text{-}SW}$	Leakage between VIN to SW when the high-side GaN FET and low-side GaN FET are off	V_{IN} = 80 V, (HI = LI = 0 V) V_{VCC} = 5 V, T_J = 25°C	25	150	µA
$I_{L\text{-}SW\text{-}GND}$	Leakage between SW and GND when the high-side GaN FET and low-side GaN FET are off	V_{SW} = 80 V, HI , LI = 0 V, V_{VCC} = 5 V, T_J = 25°C	25	150	µA
C_{OSS}	Output capacitance of high-side GaN FET and low-side GaN FET	V_{DS} = 50 V, V_{GS} = 0 V (HI = LI = 0 V)	225	280	pF
Q_G	Total gate charge	V_{DS} = 50 V, I_D = 10 A, V_{GS} = 5 V	3.8		nC
Q_{OSS}	Output charge	V_{DS} = 50 V, I_D = 10 A	20		nC
Q_{RR}	Source to drain reverse recovery charge	Not including internal driver bootstrap diode	0		nC

DYNAMIC CHARACTERISTICS					
t_{HIPLH}	Propagation delay(1)	HI turning from low to high and SW node being pulled to VIN (LO is low), V_{VIN} = 50 V, V_{VCC} = 5 V	29.5	47	ns
t_{HIPHL}		HI turning from high to low and SW node being tristated (LO is low), V_{VIN} = 50 V, V_{VCC} = 5 V	29.5	47	ns
t_{LPLH}		LI turning from low to high and switch node being pulled to PGND (HI is low), V_{VIN} = 50 V, V_{VCC} = 5 V	29.5	47	ns
t_{LPHL}		LI turning from high to low and switch node being tristated (HI is low), V_{VIN} = 50 V, V_{VCC} = 5 V	29.5	47	ns
t_{MON}	Delay matching: LI high and HI low (2)	V_{VIN} = 50 V, V_{VCC} = 5 V	2	8.0	ns
t_{MOFF}	Delay matching: LI low and HI high(2)	V_{VIN} = 50 V, V_{VCC} = 5 V	2	8.0	ns
t_{PW}	Minimum input pulse width that changes the output		10		ns

Figure 2.4: Datasheet of LMG5200 [28]

From Figure 2.4, the maximum operating frequency of this integrated circuit can be calculated as

$$\text{Propagation delay} = 59 \text{ ns} \tag{2.14}$$

$$\text{Operating frequency} < 17 \text{ MHz}. \tag{2.15}$$

2.2.2. GaN FET Drivers and Controllers

There are number of drivers in the industry that are designed for driving GaN FETs. One of them is PE29100 from Peregrine Semiconductor [29]. Its properties are shown in Table 2.1.

Table 2.1: Properties of PE29100 [29]

ATTRIBUTE	VALUE
Description	Gate Driver
Frequency (MHz)	33 MHz
Max Pulsed Output Current (A)	2
Rise Time (ns)	1
Fall Time (ns)	1
Propagation Delay (ns)	8
Dead-time Control	Resistor Settable
Package	Flip-chip
Package (mm)	2 x 1.6 mm

These drivers only drive GaN FETs, but they do not control the duty cycle of gate pulses. Therefore, PWM controllers instead of drivers are needed for DC-DC converters. However, there are few controllers in the industry that are specifically designed for controlling GaN FETs. One of them is TPS53632G from Texas Instruments [30]. Characteristics of TPS53632G are shown in Figure 2.5.

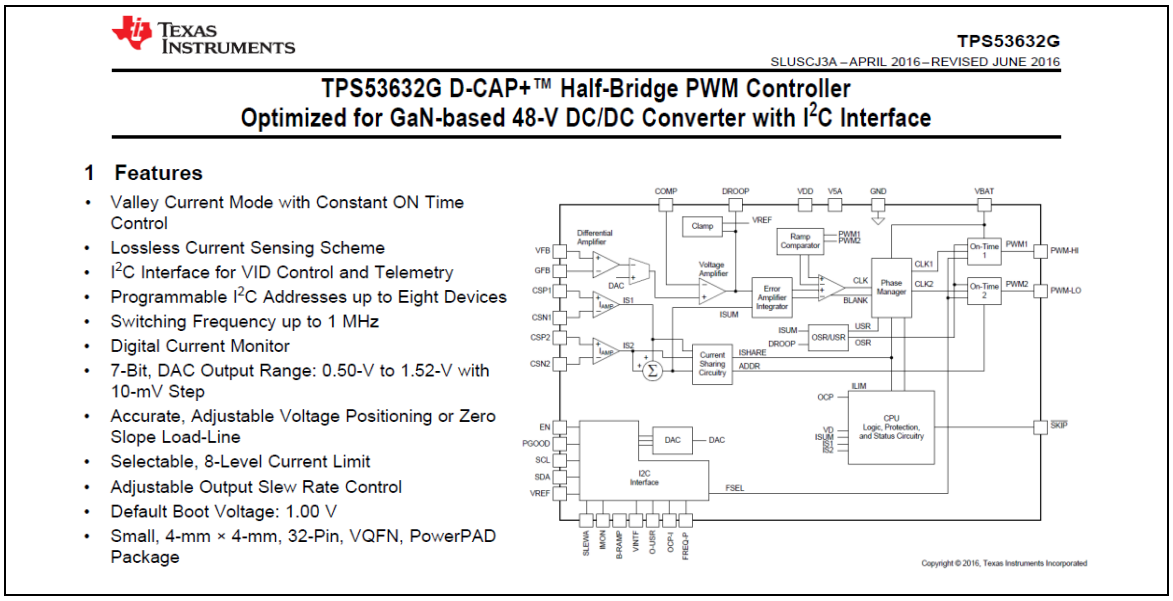


Figure 2.5: Characteristics of TPS53632G [30]

While determining the specifications of the PWM controller in section 2.4 of this thesis, parameters of TPS53632G have been taken as reference points. Properties of TPS53632G are given in Table 2.2. Its maximum switching frequency is 1 MHz, but it is a more complex IC than a standard PWM controller. Therefore, choosing the frequency level of this work higher than 1 MHz makes sense.

Table 2.2: Properties of TPS53632G [30]

ATTRIBUTE	VALUE
V_{in} (min)	2.5 V
V_{in} (max)	24 V
V_{out} (min)	0.5 V
V_{out} (max)	1.52 V
I_{out} (max)	60 A
Switching Frequency (max)	1 MHz
Technology	Standard CMOS

2.2.3. Simulations

After the search of GaN FETs in the industry, a basic buck converter circuit has been constructed in Spice environment in order to guarantee that these FETs are capable of operating at high frequency levels. In sections 2.2.1 and 2.2.2 of this thesis, it is stated that choosing a frequency level lower than 17 MHz and higher than 1 MHz is reasonable after the conducted review. Therefore, the frequency level has been chosen as 10 MHz. The schematic view of the simulation circuit that is designed for EPC2034 is given in Figure 2.6. Other circuits for simulating other GaN FETs are also similar to this one.

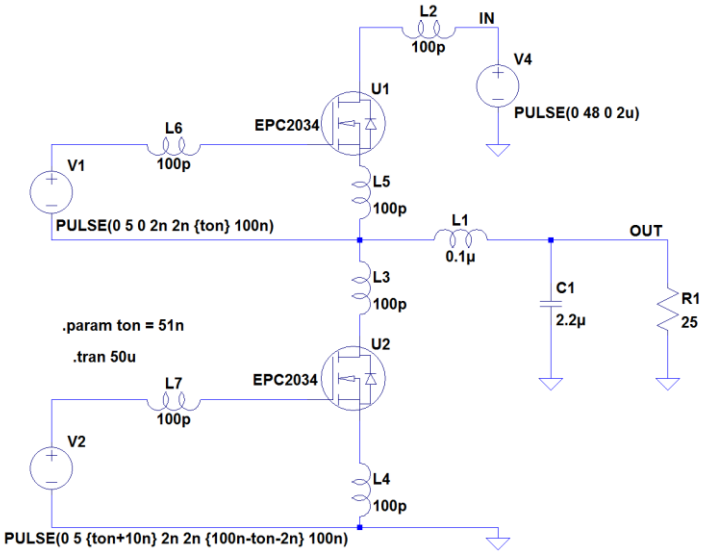


Figure 2.6: Schematic View of Simulation Circuit

Start-up characteristics and simulation results of EPC2034, GS66508T and LMG5200 can be seen in Figure 2.7, Figure 2.8 and Figure 2.9, respectively.

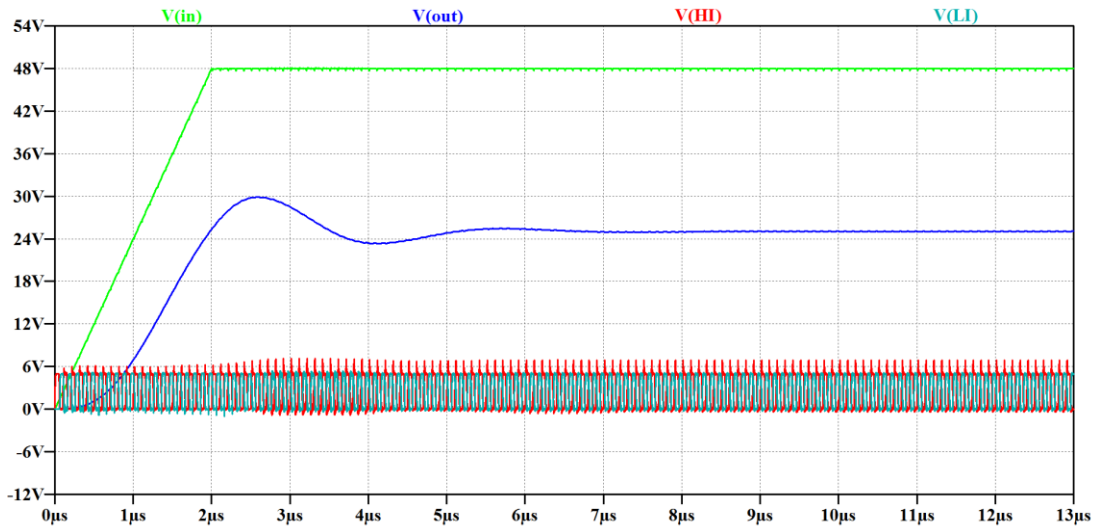


Figure 2.7: Simulation Results of EPC2034

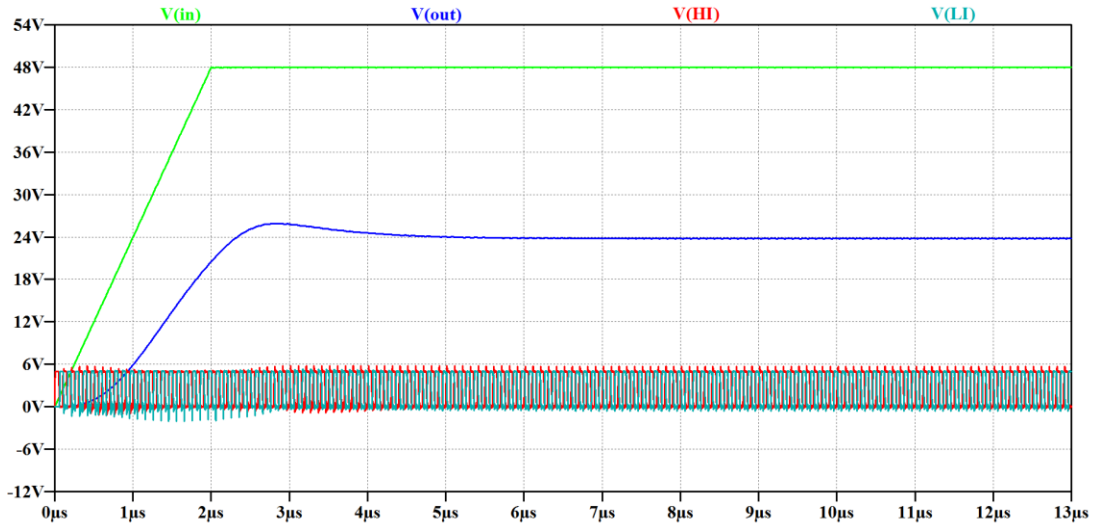


Figure 2.8: Simulation Results of GS66508T

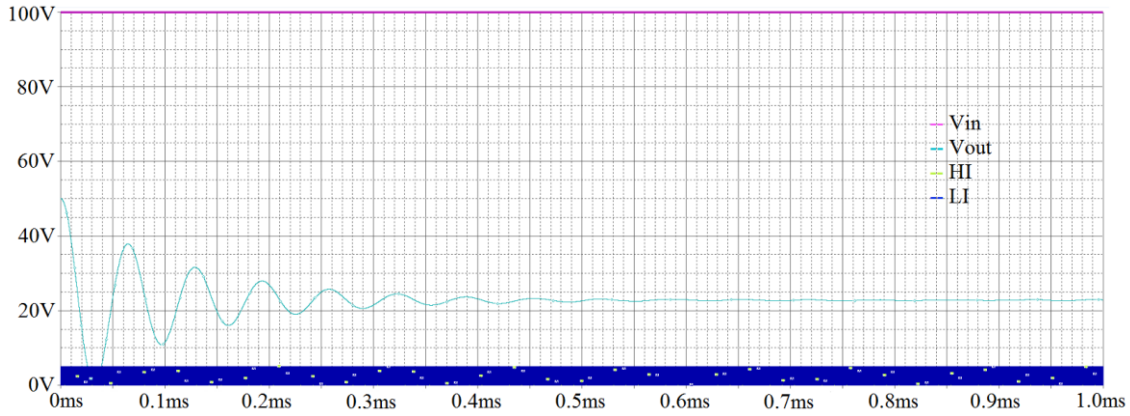


Figure 2.9: Simulation Results of LMG5200

These simulation results proves that these transistors are capable of operating at 10 MHz frequency. Therefore, choosing 10 MHz operating frequency for the PWM controller as ultimate goal seems to be reasonable. Furthermore, circuits including these GaN FETs show smooth start-up characteristics. The smoothest one seems to be the one with GS66508T.

2.3. Determination of DC-DC Converter Control Method

DC-DC converters are widely used in electronics industry because almost every module needs and includes a power supply and distribution unit inside. DC-DC converters provide required supply voltages with required power level to sub-modules in a module. Therefore, designing these converters is a milestone in designing a whole module.

In a DC-DC converter, controller part is very important and a special care must be taken while designing the controller part due to the fact that it regulates output voltages by adjusting duty cycle and determines how stable the system is. There are some controlling techniques in literature. The one that best suits the design should be chosen in order to make the design more robust. Two of the most commonly used methods are voltage mode control and current mode control.

2.3.1. Voltage Mode Control (VMC)

VMC (Voltage Mode Control) is a simple control method including just one feedback loop which is called as voltage control loop. This loop usually consists of an error amplifier and a voltage comparator. A simple diagram for VMC is shown in Figure 2.10 together with a buck converter.

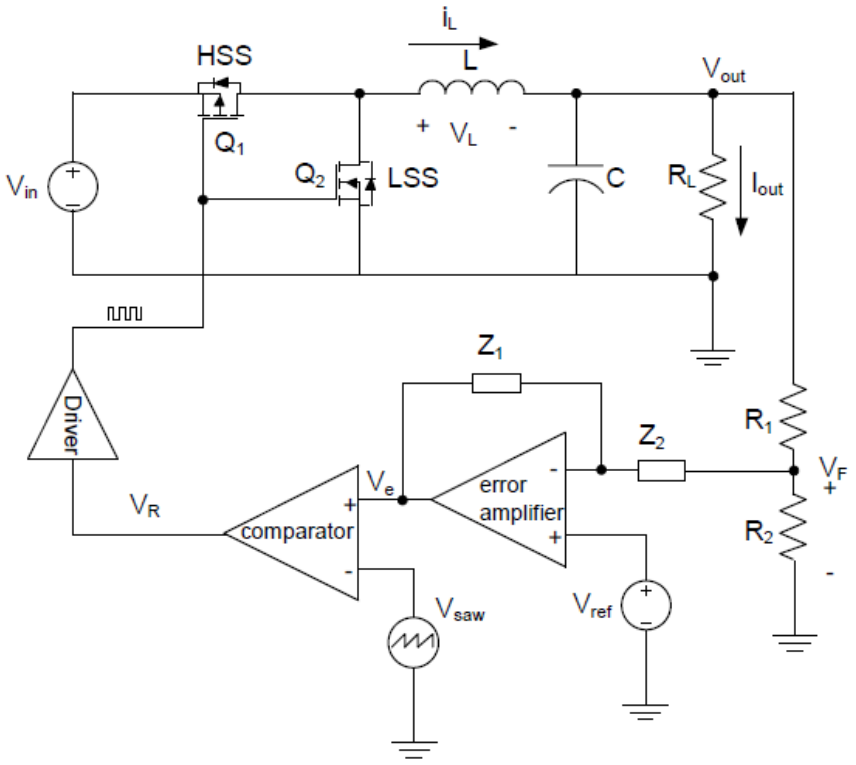


Figure 2.10: Voltage Mode Control [31]

In this method, V_{out} is divided by a voltage divider and V_F is obtained. Then, V_F is compared with a reference voltage V_{ref} and the difference is amplified in order to produce V_e. V_e is then compared with a saw-tooth wave V_{saw} and a square wave at the output of the comparator is produced. Output voltage of the converter is regulated by an internal adjustment of the duty cycle of the produced square wave which in turn opens and closes the switches in the buck regulator.

The advantages and disadvantages of this method can be given as follows:

Advantages

• Single feedback loop

• Good noise margin

• Low impedance output

Disadvantages

• Slow dynamic response

• Double-pole compensation

• Output capacitors affect compensation

• V_{in} affects loop gain

2.3.2. Current Mode Control (CMC)

CMC (Current Mode Control) includes two feedback loops namely external voltage loop and internal current loop. While external voltage loop senses output voltage and regulates it, internal current loop senses peak inductor current and controls it. CMC scheme includes error amplifier, comparator, SR (Set-Reset) latch, current sensor and clock generator. A simple diagram for CMC is given in Figure 2.11 combined with a buck converter.

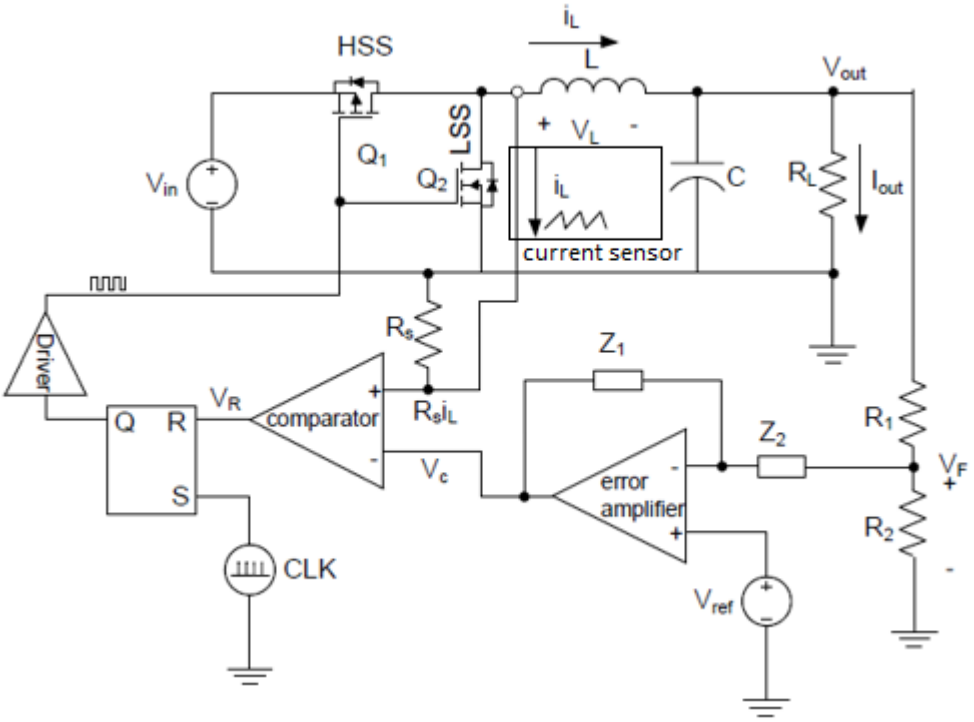


Figure 2.11: Current Mode Control [31]

A control voltage V_C is generated through external voltage feedback loop in a similar way as in VMC method. V_{out} is divided by a voltage divider and V_F is obtained. Then, V_F is compared with a reference voltage V_{ref} and the difference is amplified in order to produce V_C. V_C is compared with a voltage generated by sensing peak inductor current which is equal to $R_s i_L$ and V_R voltage is produced at the output of the comparator. When V_R is high SR latch is reseted and when a clock comes the latch is set. In this method, both the external loop and internal loop can adjust duty cycle in order to regulate output voltage.

The advantages and disadvantages of this method can be given as follows;

Advantages

- Fast response to input voltage changes
- Single-pole compensation
- Inherent current limiting
- Parallel-ability with load sharing

Disadvantages

- Two feedback loops
- Slope compensation is needed for duty cycle greater than 50%

2.3.3. VMC vs. CMC

Since current mode control employs two feedback loops, controlling the output voltage of converter is easier than voltage mode control which uses just one voltage feedback loop. [31]

The extra loop (internal current control loop) makes an improvement in phase margin and stability, and it does not need so much complicated circuit for phase compensation. Usually type II compensation is enough and it makes the design of converter simpler. However, type III compensation is needed for voltage control mode to improve the phase margin of converter. [31]

Voltage mode control has different characteristics when moving from continuous conduction mode to discontinuous conduction mode so designing a compensation circuit that can operate properly in both modes is impossible while current mode control has almost the same characteristics in both CCM (Continuous Conduction Mode) and DCM (Discontinuous Conduction Mode) modes. [31]

Since in CMC, the inductor current should be sensed it needs extra circuitry (current sensor) which causes power loss and complexity of system. [31]

Noise and spikes on the current sense signal is one of the major issues in CMC and obtaining smooth ramp from sensed signal is not simple so inevitably sometimes filter is added to current sensor circuit to suppress the noise and spikes. Figure 2.12 and Figure 2.13 show the difference between ideal current-sensed and practical current-sensed signal's waveforms respectively. [31]

Figure 2.12: Ideal Current Sense

Figure 2.13: Practical Current Sense

2.4. Specifications

Defining the efficiency requirement of a converter is not an easy task due to the trade-off between efficiency, size, power density and cost. In literature, there are DC-DC converters with a power range of in the order of kWs having maximum efficiency of around 98% [32], [33], [34], [35] and [36]. However, high power DC-DC converter design is not the scope of this thesis. On the other hand, there are some articles in literature about designing low power DC-DC converter showing efficiencies between 62% and 83.6% [37], [38], [39], [40], [41], [42], [43] and [44]. Therefore, an optimal value of efficiency has been selected as a requirement. This requirement is that the maximum efficiency of the DC-DC converter designed in this thesis should be greater than 80%. Besides, power dissipation of the PWM controller affects the efficiency of the converter. Therefore, it should be kept low in order to increase efficiency. Texas Instrument has an analog GaN FET controller IC (TPS40400) whose supply current is typically 6 mA from a 12 V supply [45]. Therefore, it is reasonable for the PWM controller IC designed in this thesis to aim lower than 6 mA supply current and lower than 72 mW power dissipation.

Section 2.2.3 of this thesis shows that the simulation results proves some GaN transistors in the industry are capable of operating at 10 MHz frequency. Therefore, choosing 10 MHz operating frequency for the PWM controller as ultimate goal seems to be reasonable.

CMC (Current Mode Control) has a single pole and it is simpler to make a current mode controller stable than a voltage mode controller which has two poles. Since a PWM controller driving GaN FETs in DC-DC converters with high frequency has been designed in this thesis, stability is a critical parameter. Since CMC is advantageous over VMC in terms of stability and other parameters stated in section 2.3 of this thesis, current mode control method has been chosen.

The specifications of the PWM controller and the DC-DC converter that has been designed in this thesis is shown in Table 2.3.

Table 2.3: Specifications

	PWM Controller	**DC-DC Converter**
Maximum Efficiency		> 80%
Supply Current	< 6 mA	
Power Dissipation	< 72 mW	
Operating Frequency	10 MHz	10 MHz
Control Method	Current Mode Control	
V_{in}	5 V	3.2 V – 30 V
V_{out}		2.5 V – 4 V
Output Current	< 10 A	
Maximum Loading		500 mA
Process	Silicon-on-Insulator	

This chapter covers in detail the preliminary studies conducted before going on to analysis and design stage. Design methodologies about producing a low-power PWM controller is discussed. Then, operating frequency and control method is determined after a literature survey and some calculations. The operating frequency is 10 MHz, and control method of the PWM controller is current mode control. Finally, specifications of this work is given in a table. The next chapter explains the schematic and simulation works done for the PWM controller.

CHAPTER 3

SCHEMATICS AND SIMULATIONS OF THE PWM CONTROLLER

Main elements of a current mode controller are error amplifier, comparator, SR latch, clock generator and current sense circuit as given in Figure 2.11. Besides these main elements, voltage reference and inverter circuits have been used in this design.

3.1. Error Amplifier

In order to compare V_F and V_{ref} in Figure 2.11, an error amplifier has been designed. While designing the amplifier, XFAB's xt018 SOI technology has been used. In this technology, nmva (10V drain ext. NMOS (N-channel Metal Oxide Semiconductor)) and pmva (10V drain ext. PMOS (P-channel Metal Oxide Semiconductor)) transistors have been picked and used in the amplifier.

The schematic view of the error amplifier is given in Figure 3.1.

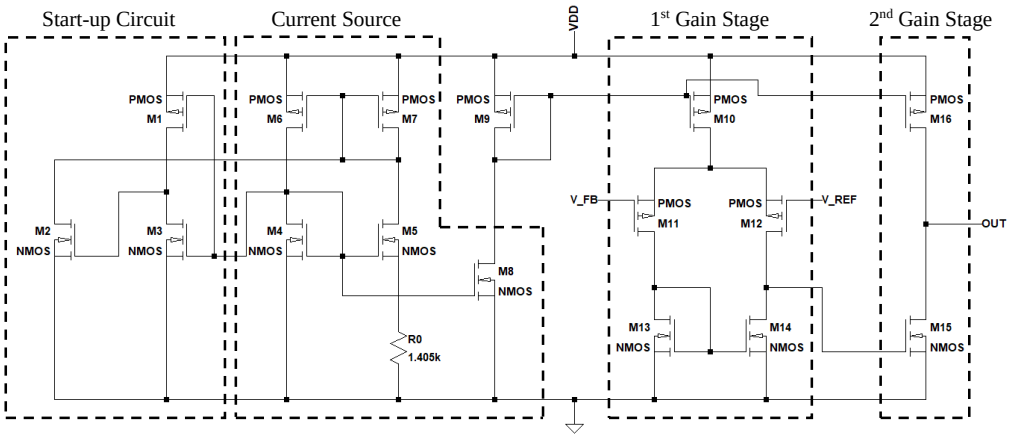


Figure 3.1: Schematic View of the Error Amplifier

The amplifier consists of a start-up circuit, current source and 2 gain stages. First gain stage is a differential amplifier with active load. Second gain stage is a common source amplifier. In order to provide required currents to transistors, a current source stage is included in the error amplifier. This stage is a self-biased low current reference generator stage. Since for this topology there are two solutions, one of which is zero output current solution, a start-up circuitry is needed. As shown in Figure 3.1, M2 in the start-up circuit is turned on during start-up and makes the circuit start. After the circuit reaches steady-state, M2 is turned off by properly adjusting the size of M3. In steady-state operation of the amplifier, start-up circuit does not affect the circuit.

Sizes of the transistors have been adjusted accordingly in order to have a desired gain. After that, stability analysis has been done. First, a 500 pF output capacitor has been connected at the output of the amplifier. The resultant Bode plot for this case is given in Figure 3.2 and results can be stated as

$$\text{Crossover frequency} = 1.6 \text{ MHz} \tag{3.1}$$

$$\text{Phase Margin} = 81.1°. \tag{3.2}$$

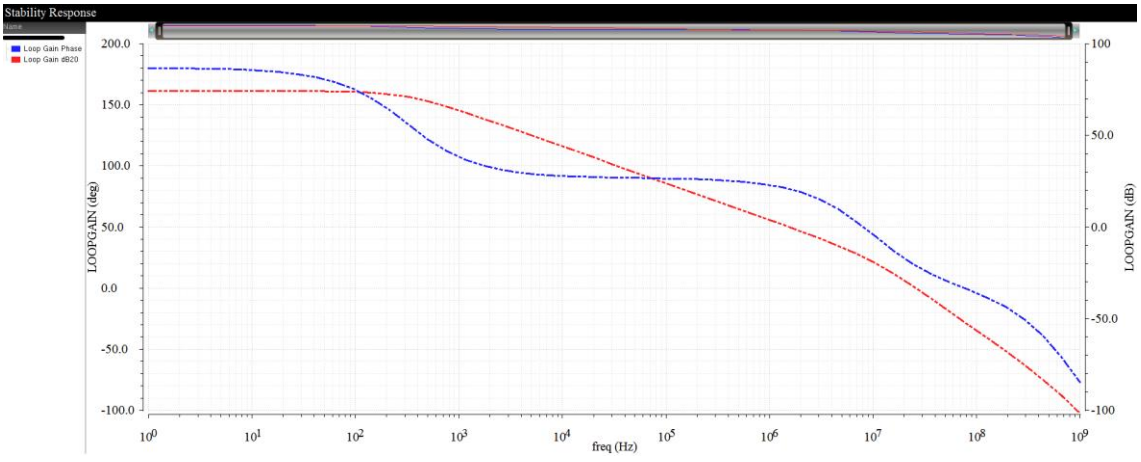


Figure 3.2: Bode Plot for 500 pF Output Capacitor

In this case for a current mode controller, the single pole can be approximated as

$$\omega_P = \frac{1}{C_{out}R_{load}} \tag{3.3}$$

where, C_{out} is the output capacitance of the DC-DC converter and R_{load} is the load resistance of DC-DC converter.

Second, ESR (Equivalent Series Resistance) value of output capacitor has been introduced into the system. Then, stability analysis has been repeated for a 500 pF output capacitor with 10Ω ESR value. These values are fictitious values. The resultant Bode plot for this case is given in Figure 3.2, and results can be stated as

Crossover frequency = 1.6 MHz (3.4)

Phase Margin = 83.8°. (3.5)

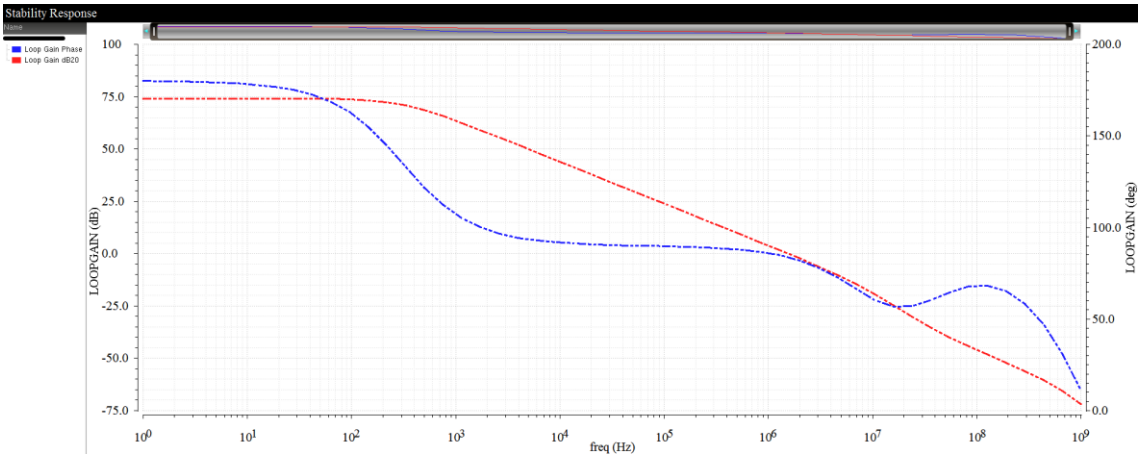


Figure 3.3: Bode Plot for 500 pF Output Capacitor with 10Ω ESR

In this case for a current mode controller, the single pole and zero can be approximated as

$$\omega_P = \frac{1}{C_{out}R_{load}} \tag{3.6}$$

$$\omega_Z = \frac{1}{C_{out}ESR} \tag{3.7}$$

where, C_{out} is the output capacitance of the DC-DC converter, R_{load} is the load resistance of DC-DC converter and *ESR* is the equivalent series resistance of output capacitor. Since a left-half plane zero is introduced into the system, phase margin of the amplifier is increased slightly in this case.

In order to make the system more stable and robust, a compensation circuit can be placed into the system. Since CMC scheme includes a single pole, it is simpler to make current mode controller stable than to make a voltage mode controller stable. Therefore, a Type-II compensation scheme is enough for a current mode controller if needed. The schematic view of a Type-II compensator connected between inverting input and output pins of the error amplifier is given in Figure 3.4.

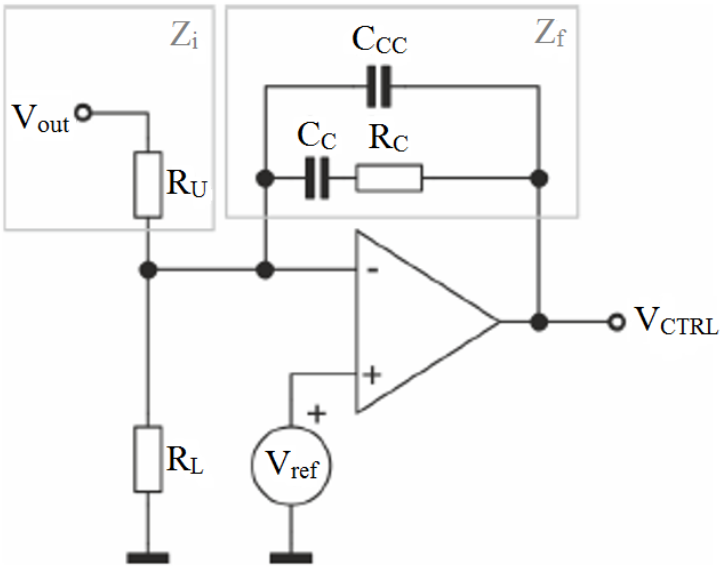


Figure 3.4: Type-II Compensator

Transfer function of this system can be given as

$$H(s) = \frac{Z_f}{Z_i} = \frac{\left(\frac{1}{sC_C} + R_C\right)\frac{1}{sC_{CC}}}{\frac{1}{sC_C} + R_C + \frac{1}{sC_{CC}}} \Big/ R_U$$

$$H(s) = \frac{1 + C_C R_C s}{(C_{CC} + C_C) R_U s + R_U C_C C_{CC} R_C s^2}$$

Can be simplified for $C_c >> C_{cc}$ (3.8)

where, *H(s)* is the transfer function and other parameters are given in Figure 3.4.

Poles and zeros of this system can be mentioned as

$$\omega_{Z1} = \frac{1}{R_C C_C} \quad (3.9)$$

$$\omega_{P0} = \frac{1}{R_U C_C} \quad (3.10)$$

$$\omega_{P1} = \frac{1}{R_C C_{CC}} \quad (3.11)$$

where, ω_{Z1} is the zero, ω_{P0} is the first pole at origin and ω_{P1} is the second pole.

Since a current mode controller has one pole and one zero, it is easy to make the converter stable by a Type-II compensator. In order to make the system stable, the conditions of

$$C_{out}\, R_{load} = R_C\, C_C \quad (3.12)$$

$$C_{out}\, ESR = R_C\, C_{CC} \quad (3.13)$$

must be satisfied, where C_{out} is the output capacitance of the DC-DC converter, R_{load} is the load resistance of DC-DC converter and *ESR* is the equivalent series resistance of output capacitor.

By doing this, the pole of current mode controller is cancelled by the zero of Type-II compensator and the zero of current mode controller is cancelled by the second pole of Type-II compensator. [46]

Since the phase margin of the error amplifier is 83.8°, no compensation circuit is required. Type-II compensator has been studied in case of an instability scenario encountered during tests.

The other simulated results of the error amplifier are about open loop gain and PSRR (Power Supply Rejection Ratio). As shown on Figure 3.2 and Figure 3.3, open loop gain of this amplifier is 74dB. Gain from supply to output of the amplifier has also been simulated in order to calculate PSRR. Supply-to-output gain is 0.109 (-19.25 dB) and is shown in Figure 3.5.

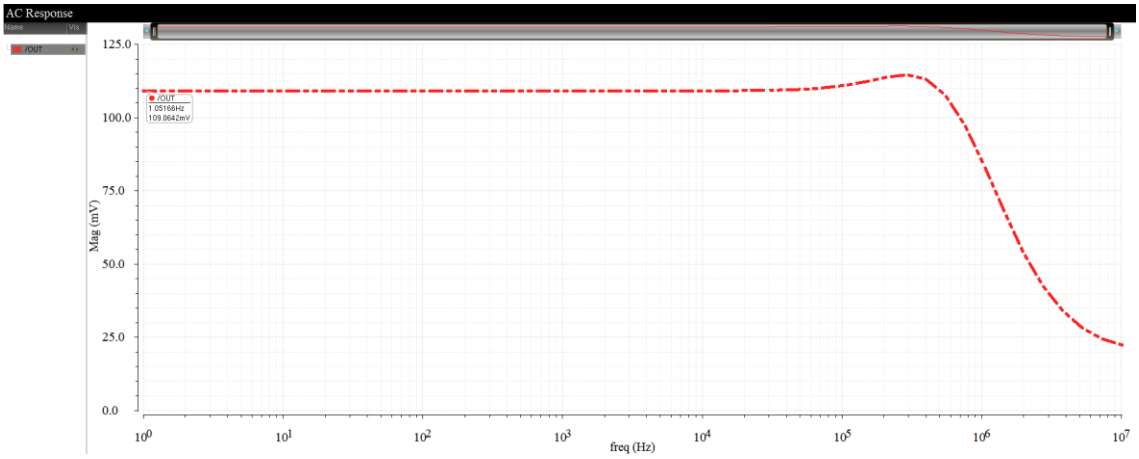


Figure 3.5: Supply-to-Output Gain

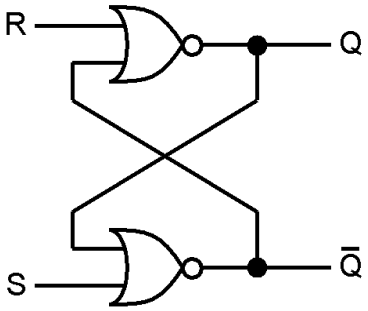
From these results, PSRR is calculated as

$$\text{PSRR} = \frac{A_v}{A_{vdd}} = 93.75 \text{ dB} \tag{3.14}$$

where, A_V is the open loop gain of the error amplifier and A_{Vdd} is the supply-to-output gain of the error amplifier.

3.2. SR Latch

In CMC scheme, SR latch is used. SR latch is usually used in switch mode controllers in order to prevent multiple and unwanted transitions per switching period. Block diagram and truth table of an SR latch can be given as in Figure 3.6.



S	*R*	*Q*	*Q'*	
0	0	NC	NC	No change. Latch remained in present state.
1	0	1	0	Latch SET.
0	1	0	1	Latch RESET.
1	1	0	0	Invalid condition.

Figure 3.6: SR Latch Truth Table

In order to construct an SR latch, two NOR (Not OR) gates are required. Therefore, NOR gates have been designed firstly. While designing NOR gates and SR latch, XFAB's xt018 SOI technology has been used. In this technology, nmva (10V drain ext. NMOS) and pmva (10V drain ext. PMOS) transistors have been picked and used in the NOR gate.

Schematic view of the NOR gate is shown in Figure 3.7.

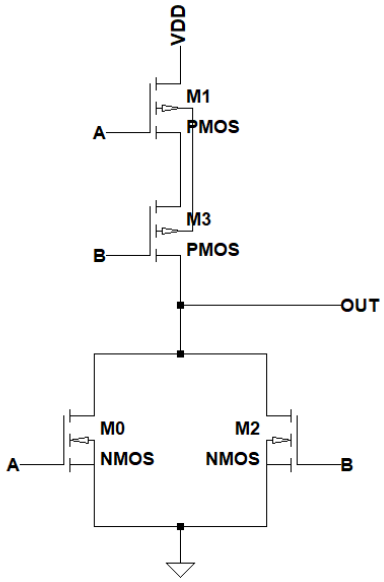


Figure 3.7: Schematic View of the NOR Gate

Simulations for NOR gate have been conducted with a 1pF capacitive load. Simulation results can be seen in Figure 3.8.

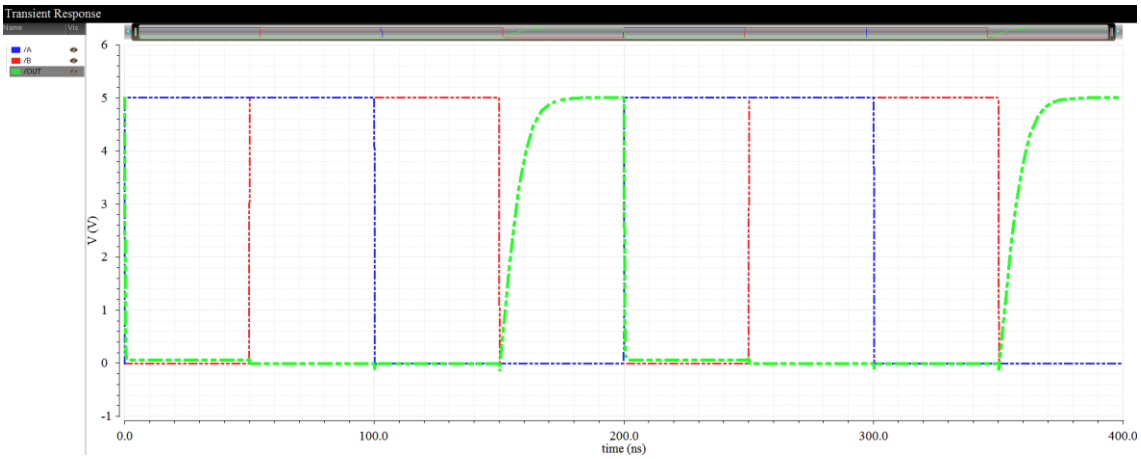


Figure 3.8: Simulation Results of the NOR Gate

Truth table of a NOR gate is given in Table 3.1. Simulation results in Figure 3.8 are consistent with the truth table given in Table 3.1. According to simulation results given in Figure 3.8, rise time of the NOR gate is approximately 6ns. Fall time of it is considerably small.

Table 3.1: NOR Gate Truth Table

INPUT		**OUTPUT**
A	**B**	**X**
0	0	1
0	1	0
1	0	0
1	1	0

By using the designed NOR gates, an SR latch has been constructed. Schematic view of the SR latch is shown in Figure 3.9.

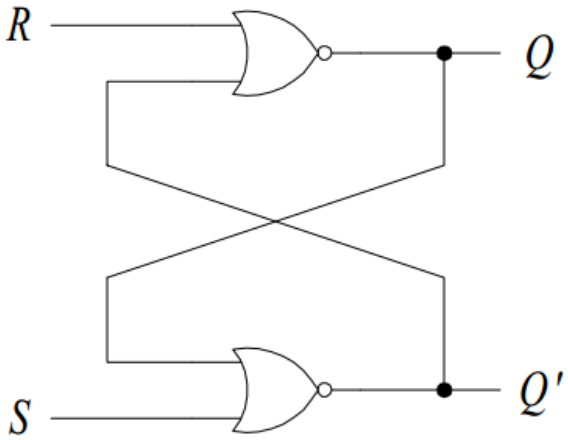


Figure 3.9: Schematic View of the SR Latch

The circuit in Figure 3.9 has been simulated and it has been seen that the results are consistent with the truth table given in Figure 3.6. Simulation results for two different cases are given in Figure 3.10 and Figure 3.11.

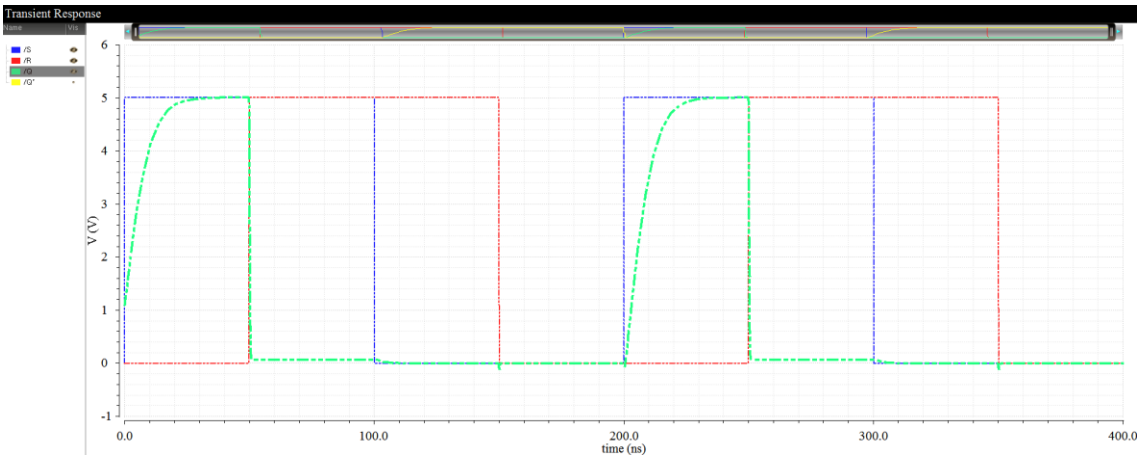


Figure 3.10: Simulation Result of the SR Latch (Case 1)

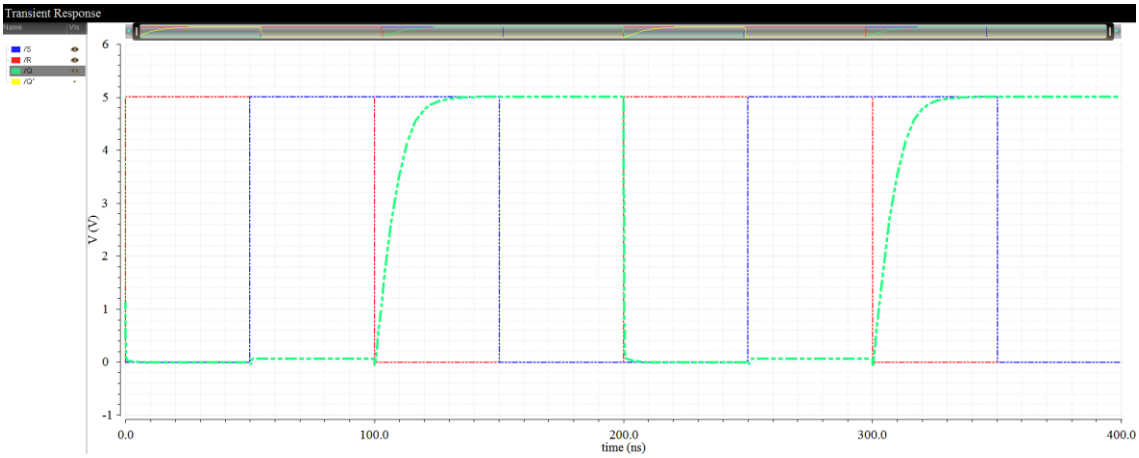


Figure 3.11: Simulation Result of the SR Latch (Case 2)

Rise and fall times of SR Latch is almost same with the ones of NOR gate. Rise time of it is approximately 6ns. Fall time is considerably small.

3.3. Clock Generator

A clock signal is required for switching converter schemes. This clock signal determines switching frequency of the converter. In CMC, clock signal drives SR latch and is supposed to be a square wave with a duty cycle lower than %50 in order not to deal with slope compensation.

While designing the clock generator, XFAB's xt018 SOI technology has been used. In this technology, nmva (10V drain ext. NMOS) and pmva (10V drain ext. PMOS) transistors have been picked and used in the generator. A ring oscillator with external frequency adjustment has been designed first, and a duty cycle control circuit has been placed after the oscillator.

The schematic view of the clock generator is given in Figure 3.12.

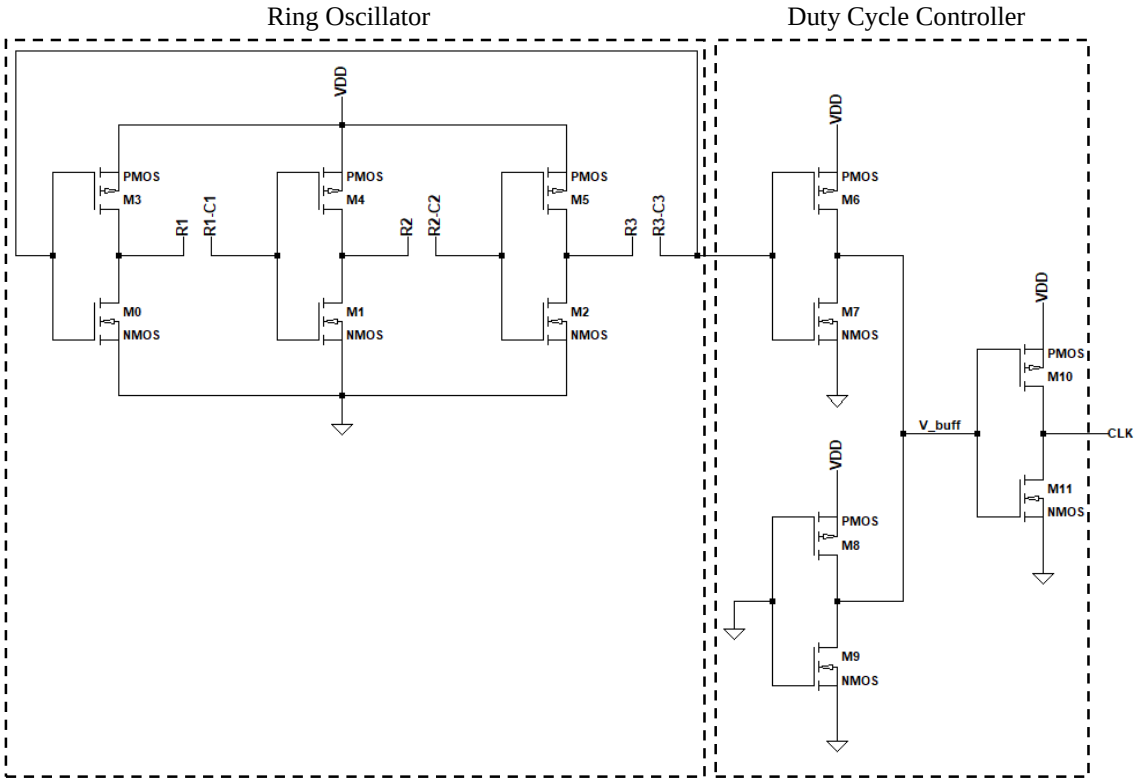


Figure 3.12: Schematic View of the Clock Generator

Frequency of the ring oscillator is adjusted by placing external resistor and capacitors. Duty cycle of the clock signal is controlled by changing the gate voltages of M8 and M9 in Figure 3.12. *V_buff* in Figure 3.12 can be approximated as

$$V\_buff = VDD \frac{r_{o7} // r_{o9}}{r_{o7} // r_{o9} + r_{o6} // r_{o8}} \tag{3.15}$$

where, *VDD* is the supply voltage, r_{o6} is the output resistance of M6, r_{o7} is the output resistance of M7, r_{o8} is the output resistance of M8 and r_{o9} is the output resistance of M9. *V_buff* depends on drain-to-source (output) resistance of M8 and M9 which can be controlled by gate voltage of M8 and M9. By adjusting *V_buff*, duty cycle of the clock signal can be controlled [47]. Gate voltage of M8 and M9 is pulled to ground in order to get minimum duty cycle.

External resistor and capacitor values have been adjusted in simulation environment so that the clock frequency was adjusted to 10 MHz. Duty cycle has become around %30. Ring oscillator output (blue), V_buff (red) and clock signal (green) can be seen in Figure 3.13.

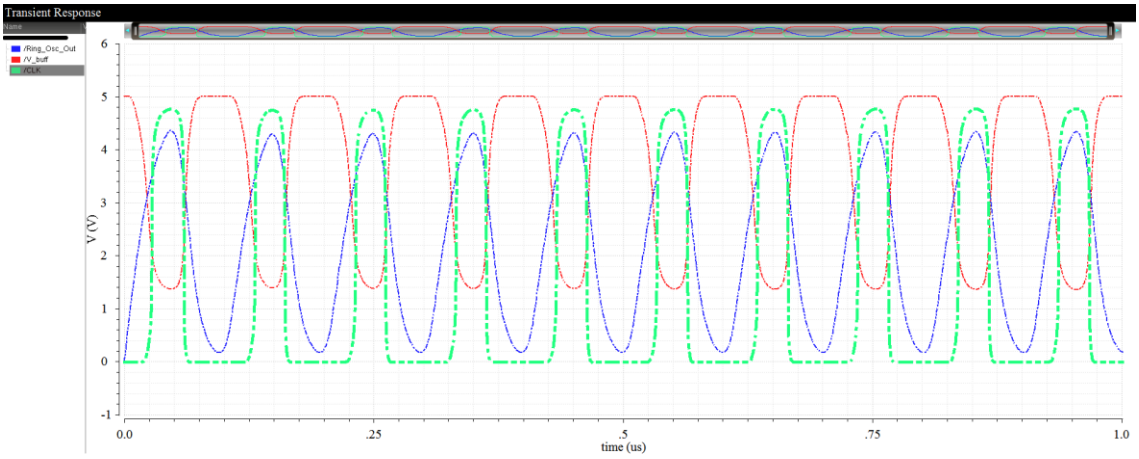


Figure 3.13: Output of the Clock Generator

3.4. Voltage Reference

In order to compare VF and Vref in Figure 2.11, a reference voltage is needed. Therefore, a bandgap reference circuit has been designed. In bandgap reference, XFAB's xt018 SOI technology has been used. In this technology, rpp1 (P+ poly (non-salicided)) resistors and qnv5 (5V NPN) transistors have been picked and used. Furthermore, previously designed error amplifier opamp has been used in the reference circuit.

Schematic view of the voltage reference circuit is shown in Figure 3.14. Output reference voltage can be calculated as

$$V_{ref} = V_{BE,0} + V_{R,1} \tag{3.16}$$

$$V_{R,1} = I_{R,1}\, R_1 = 2\, I_{R,0}\, R_1 \quad (R2 = R3) \tag{3.17}$$

$$I_{R,0} = \frac{V_{R,0}}{R_0} = \frac{V_{BE,0} - V_{BE,1}}{R_0} = \frac{\Delta V_{BE}}{R_0} \tag{3.18}$$

$$V_{ref} = V_{BE,0} + 2\,\frac{R_1}{R_0}\,\Delta V_{BE} \tag{3.19}$$

where, V_{ref} is the output reference voltage, $V_{BE,0}$ is the base-to-emitter voltage of Q0, $V_{BE,1}$ is the base-to-emitter voltage of Q1, ΔV_{BE} is the base-to-emitter voltage difference of the transistors, *R0* is the resistance value of R0, *R1* is the resistance value of R1, *R2* is the resistance value of R2, *R3* is the resistance value of R3, $V_{R,0}$ is the voltage across R0, $V_{R,1}$ is the voltage across R1, $I_{R,0}$ is the current flowing through R0 and $I_{R,1}$ is the current flowing through R1. In order to calculate the output reference voltage, some assistant formulas are required such as

$$\Delta V_{BE} = \frac{kT}{q} \ln\left(\frac{J_{C,0}}{J_{C,1}}\right) \tag{3.20}$$

$$I_C = A_E\, J_C \tag{3.21}$$

where, k is the Boltzmann constant, T is temperature, q is the electron charge, I_C is the collector current, A_E is the emitter area and J_C is the collector current density.

After this formulation, the conditions have been selected as

$$\frac{J_{C,0}}{J_{C,1}} = 8 \tag{3.22}$$

$$\frac{R_1}{R_0} = 5.5 \tag{3.23}$$

$$R_2 = R_3. \tag{3.24}$$

With $V_{BE,0}$ = 0.68 V, V_{ref} can be calculated as 1.27 V.

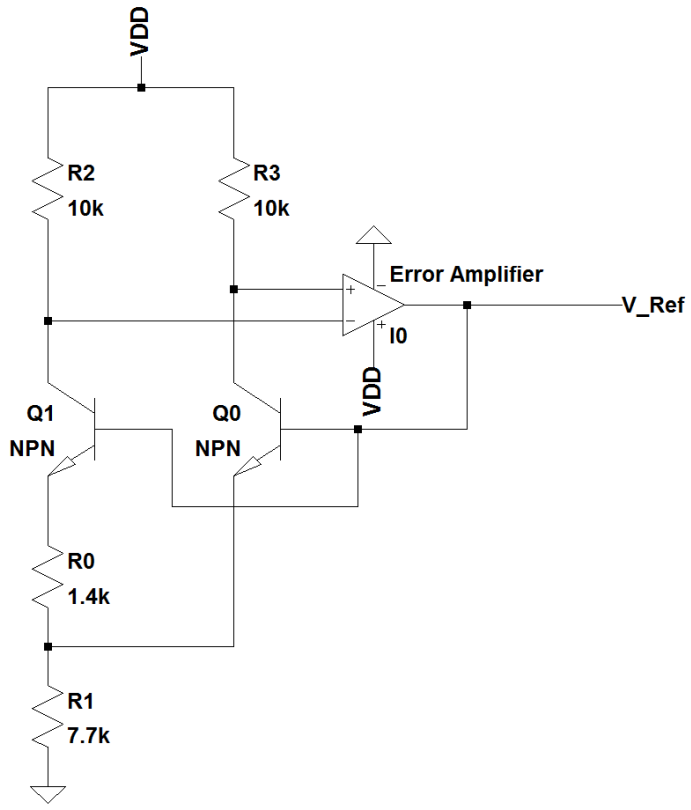


Figure 3.14: Schematic View of the Voltage Reference

Simulation results can be seen in Figure 3.15. Reference voltage is 1.27 V as expected.

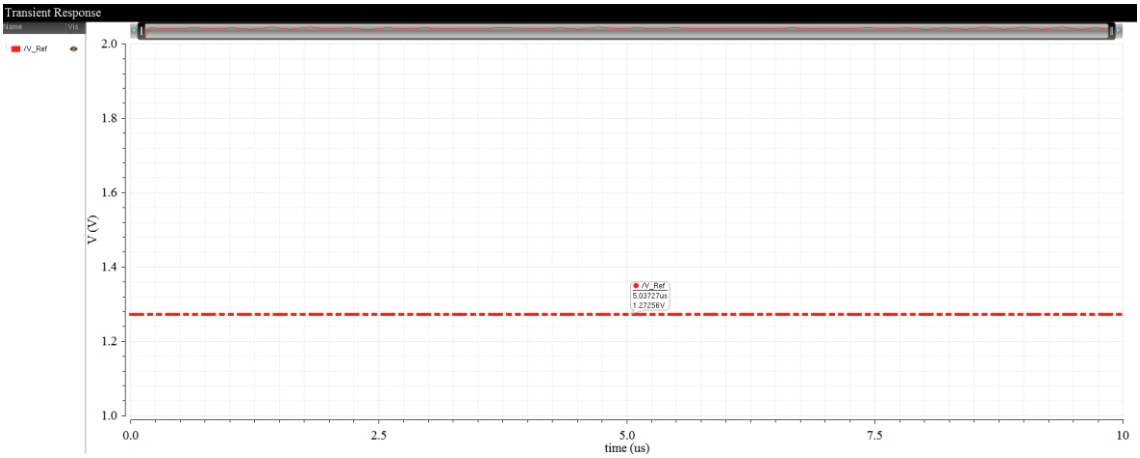


Figure 3.15: Output Voltage of the Voltage Reference

3.5. Current Sense

In CMC, current drawn by the inductor of the output filter of the DC-DC converter should be sensed and compared with output voltage of the error amplifier. Therefore a current sense circuit has been designed and implemented. While designing, XFAB's xt018 SOI technology has been used. In this technology, rpp1 (P+ poly (non-salicided)), rpp1s (P+ poly) resistors and qpva5 (5.0V PNP) transistors have been picked and used.

Schematic view of the current sense circuit is given in Figure 3.16.

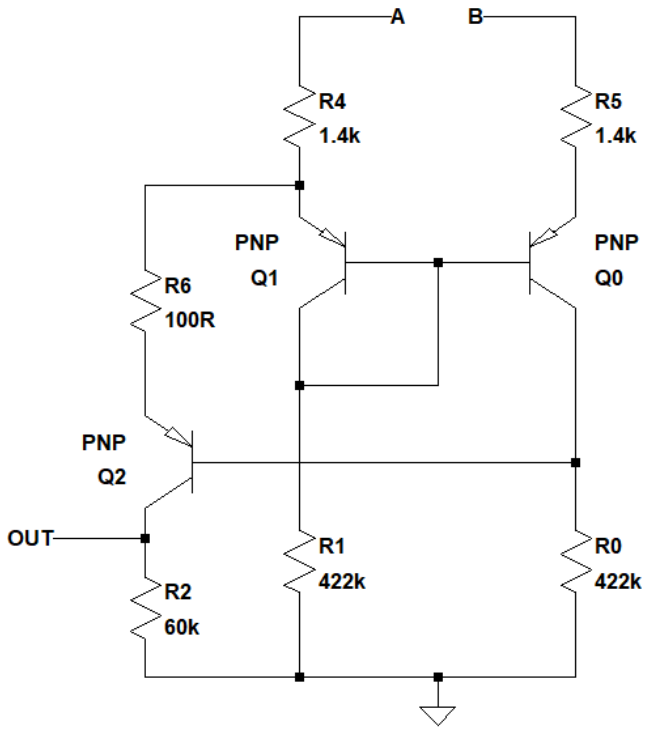


Figure 3.16: Schematic View of the Current Sense

Current sense circuit has been simulated by placing a sense resistor between node A and node B in Figure 3.16. Simulation results can be seen in Figure 3.17. Output voltage versus current flowing through the sense resistor can be observed in the graph. Sensitivity of the current sense circuit can be adjusted by changing the value of sense resistor.

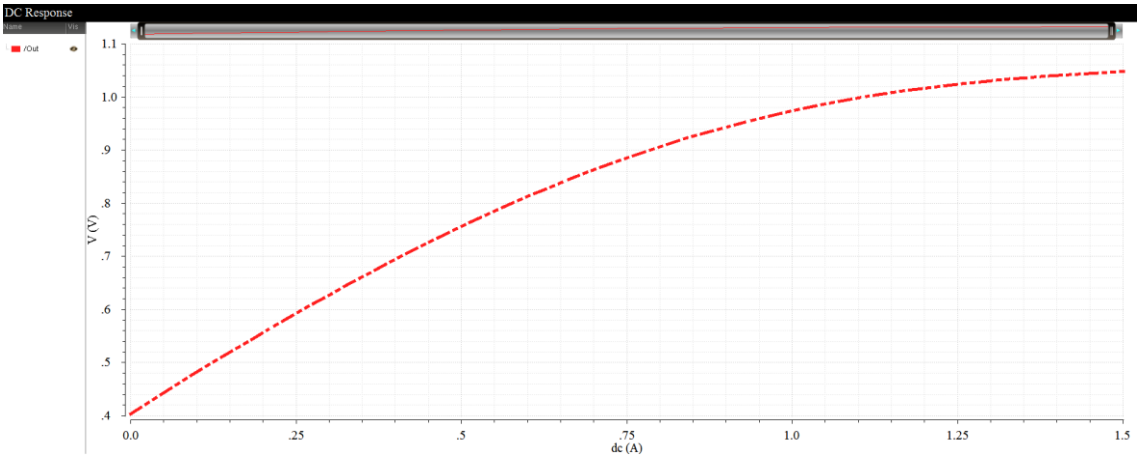


Figure 3.17: Output Voltage of Current Sense vs. Current Flowing Through Sense Resistor

3.6. Inverter

A delay generator circuit has been designed in the PWM controller in order to reduce the switching losses and increase the efficiency of the DC-DC converter implemented in this thesis. Inverters has been utilized in order to create delay. In the inverter, XFAB's xt018 SOI technology has been used. In this technology, nmva (10V drain ext. NMOS) and pmva (10V drain ext. PMOS) transistors have been picked and used in the amplifier.

The schematic view of the inverter is given in Figure 3.18.

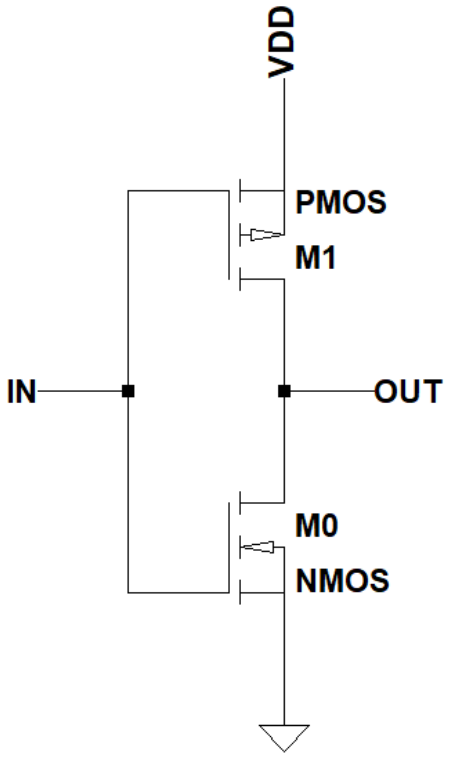


Figure 3.18: Schematic View of the Inverter

Since carrier mobilities of NMOS and PMOS transistors are different from each other [48], widths of the transistors have been chosen differently in order to get symmetric rise and fall time responses. The width of the PMOS transistor has been selected as twice as the one of the NMOS transistor.

Simulation results are given in Figure 3.19. Input (green) and output (red) signals can be observed in the graph for a 500 pF output capacitor.

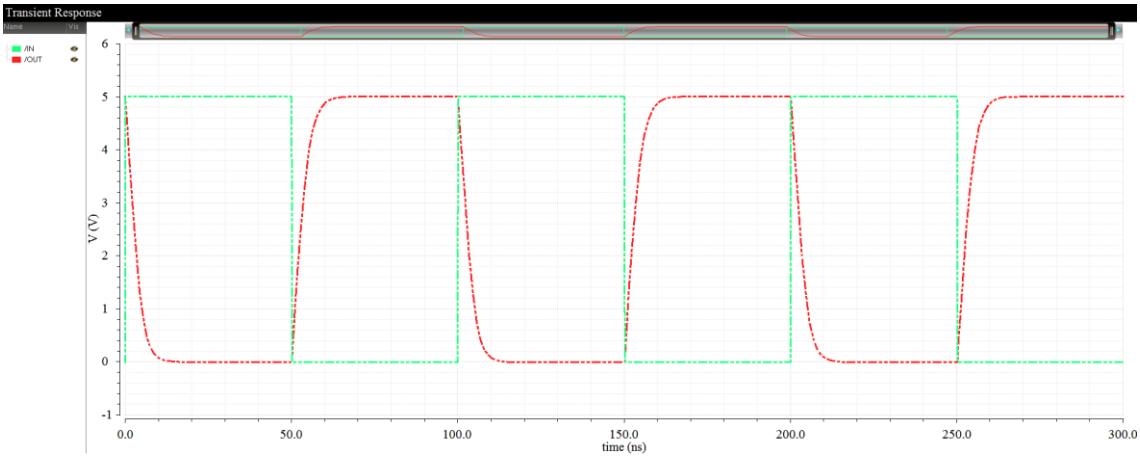


Figure 3.19: Simulation Results of the Inverter

According to simulation results given in Figure 3.19, rise and fall times of the inverter are approximately 6 ns. This means that an inverter block creates 6 ns delay.

3.7. Overall PWM Controller

After designing all blocks of PWM controller, the controller has been constructed as in Figure 3.20.

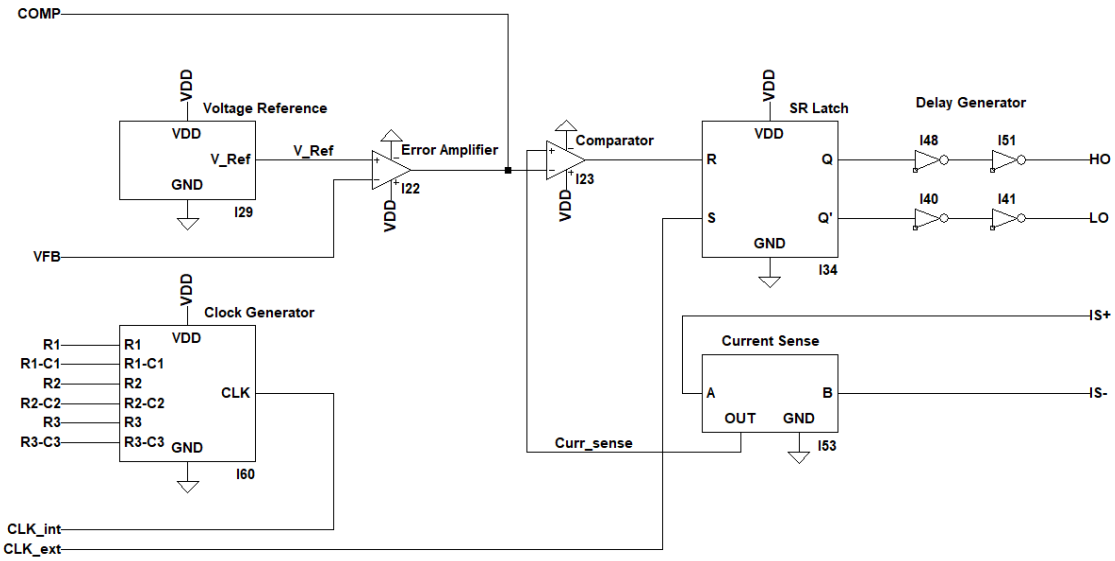


Figure 3.20: Schematic View of the PWM Controller

Voltage reference circuit produces a reference voltage, which is approximately 1.27 V. Error amplifier takes this reference voltage (V_Ref) and feedback voltage (VFB), and produces an output voltage, which is then compared with the output voltage of the current sense circuit (Curr_sense). Current sense circuit senses the current flowing through output filter inductor of DC-DC converter, and produces a voltage proportional with the current sensed. Then, comparator compares this voltage (Curr_sense) and the output voltage of the error amplifier. Comparator in the PWM controller is identical with the error amplifier used. After that, SR latch takes output of the comparator as its reset signal, and takes the clock generated by clock generator as its set signal. Clock generator circuit has 2 options. It can either generate clock signal internally, or be disabled for allowing an external clock signal. Either option can be used. Finally, outputs of the SR latch are given to two stage inverters. This final stage is used in order to give outputs of the SR latch enough transition time before switching transistors in DC-DC converter switch their state. This method significantly reduces the switching losses of the GaN FETs used in the DC-DC converter.

Since the PWM controller uses CMC, it has two different loops, namely external voltage loop and internal current loop. Therefore, either loop can be activated according to load of the DC-DC converter. In order for a proper current mode control, current flowing through output filter inductor should be sufficient enough for its peak value to reach a threshold in order to activate reset of SR latch in every switching cycle. A simulation circuit has been constructed as in Figure 3.21.

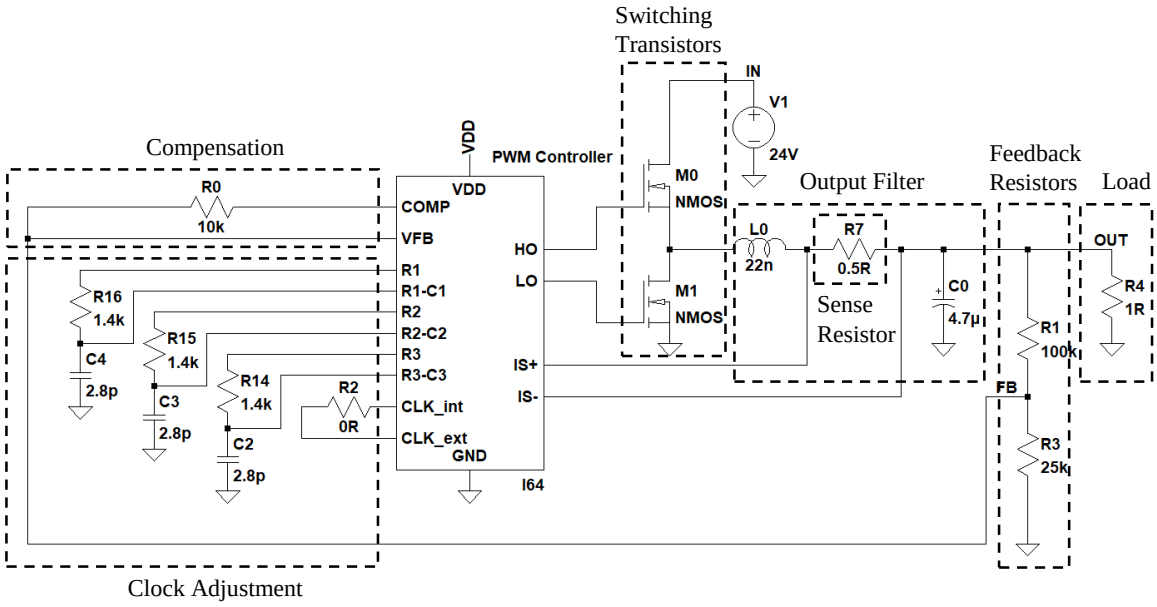


Figure 3.21: PWM Controller Simulation Circuit

Simulation circuit uses a synchronous DC-DC buck converter topology. In the simulation circuit, input voltage has been given as 24 V. Switching transistors have been selected from XFAB's xt018 SOI technology (nmva (10V drain ext. NMOS)). Clock has been adjusted to 10 MHz by placing proper resistors and capacitors in the clock adjustment circuit. Compensation is provided only by 10 kΩ resistor.

Simulation results are given below. Figure 3.22 shows the response of PWM controller with R_{Load}=5Ω. First, internal current loop becomes active, and then external voltage loop takes place. Therefore, this condition and load value are not appropriate for a proper

current mode control. Output voltage profile of the controller can be seen in the graph. Output voltage settles in 24 us without overshoot and reaches to approximately 4 V in steady-state condition. On the other hand, Figure 3.23 and Figure 3.24 shows the response of PWM controller in a proper current mode control with R_{Load}=1Ω. In Figure 3.23 , output voltage characteristics in start-up can be seen. It can be seen that output voltage settles in 8 us without overshoot and reaches to approximately 1 V in steady-state condition. More details about current mode can be observed in Figure 3.24. When the current flowing through output filter inductor reaches 2.8 A, switching operation begins. Reverse switching operation is activated when set signal of SR latch, which is the clock generated by clock generator, becomes high. It can be seen that output filter inductor current oscillates between 3.3 A and -0.9 A. Duty cycle is approximately %40 with R_{Load}=1Ω. Furthermore, start-up characteristics of output voltage of DC-DC converter without any overshoot shows that the circuit is stable enough. Therefore, no compensation circuit (e.g. type II compensation) except a 10 kΩ resistor is needed. In steady-state condition, the PWM controller draws 2.3 mA from the 5 V supply according to simulation results given in Figure 3.25.

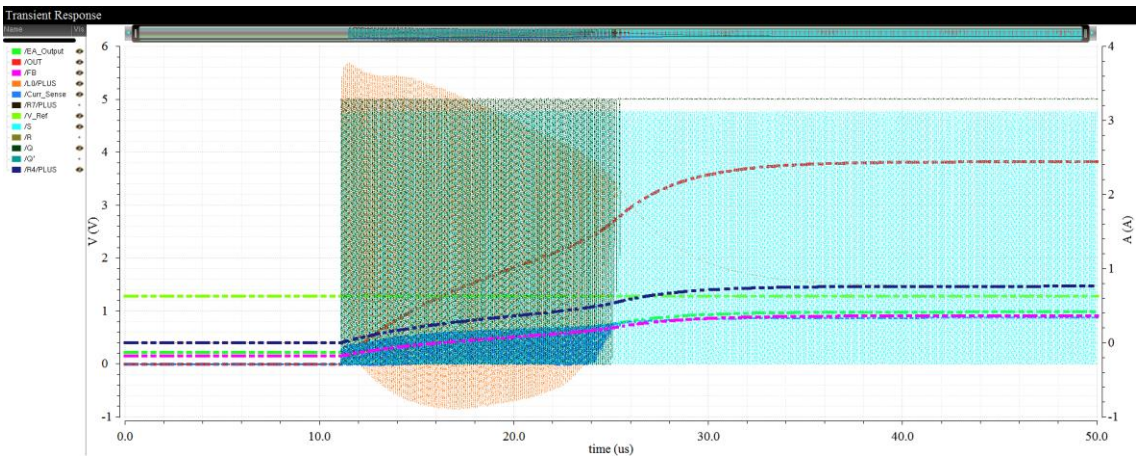


Figure 3.22: Response of PWM Controller for R_{Load}=5Ω

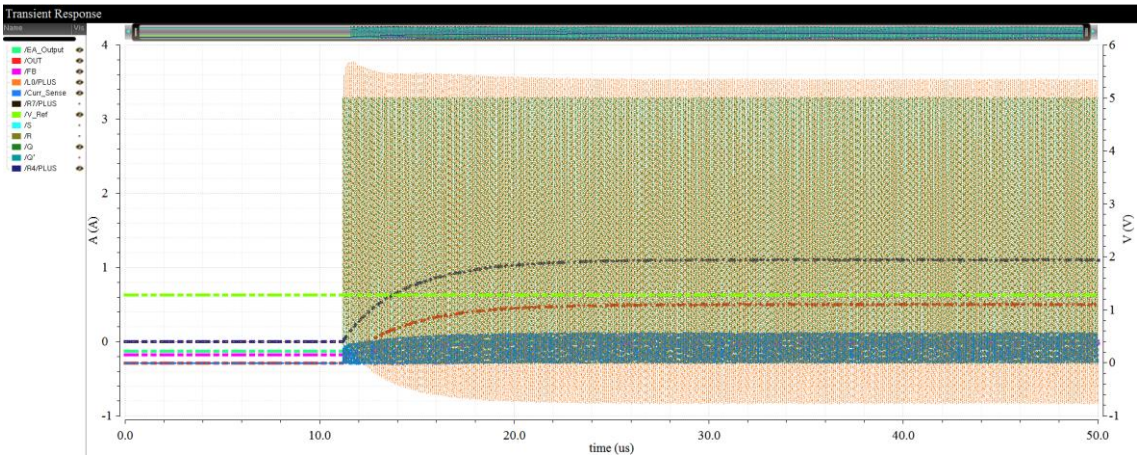


Figure 3.23: Response of PWM Controller for R_{Load}=1Ω

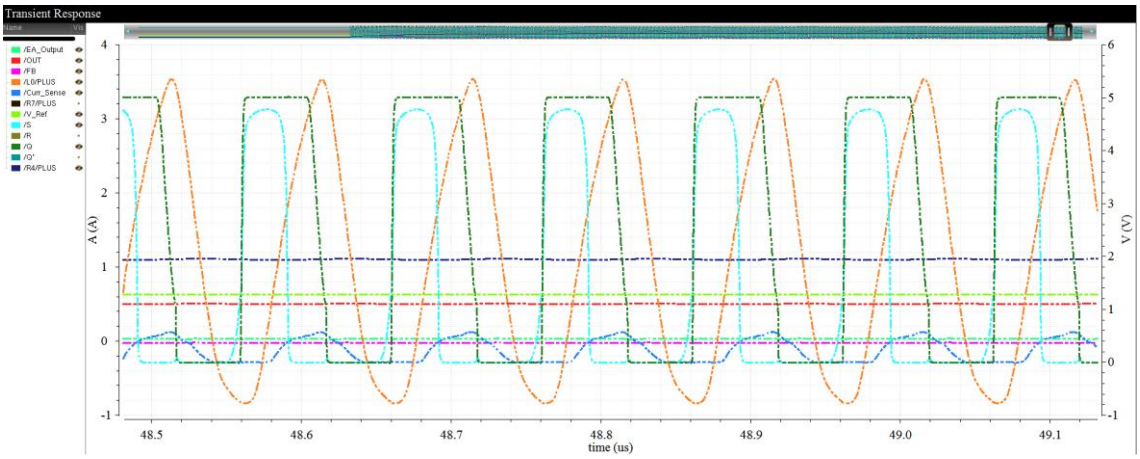


Figure 3.24: Detailed Response of PWM Controller for R_{Load}=1Ω

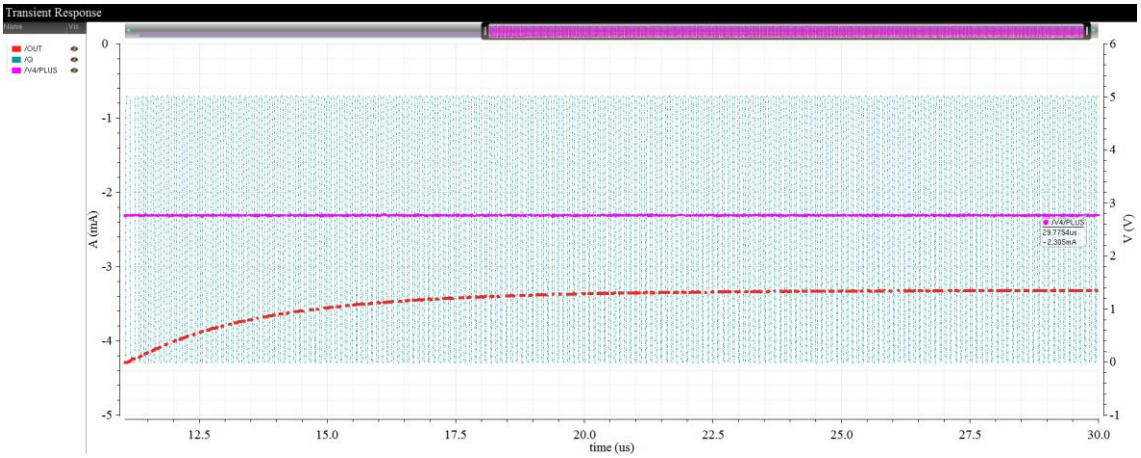


Figure 3.25: Current Drawn by the PWM Controller in Simulation Environment

In this chapter, each block of the PWM controller is discussed in detail. Schematic views and simulation results of the blocks are given. Besides, design niceties of some blocks are discussed in detail. Then, schematic view and simulation results of the overall PWM controller are given. It is seen that the PWM controller is capable of operating at 10 MHz in a buck converter and draws 2.3 mA current from the supply. This shows that the controller works properly in simulation environment. The next chapter tells about the layout work of the controller.

CHAPTER 4

LAYOUT OF THE PWM CONTROLLER

After schematic and simulation works have been done, layout of the PWM controller has been drawn. Since the production of the PWM controller chip has been realized in XFAB, available modules of the foundry have been used. Only MET1 and MET2 layers have been used for metal layers throughout the layout work except in ESD (Electrostatic Discharge) protection pads. Layout of each block of the PWM controller has been drawn separately. Details about the layouts of each block are given in this chapter.

4.1. Error Amplifier

Layout of the error amplifier is given in Figure 4.1. It includes 8 nmva, 8 pmva transistors and an rpp1 resistor.

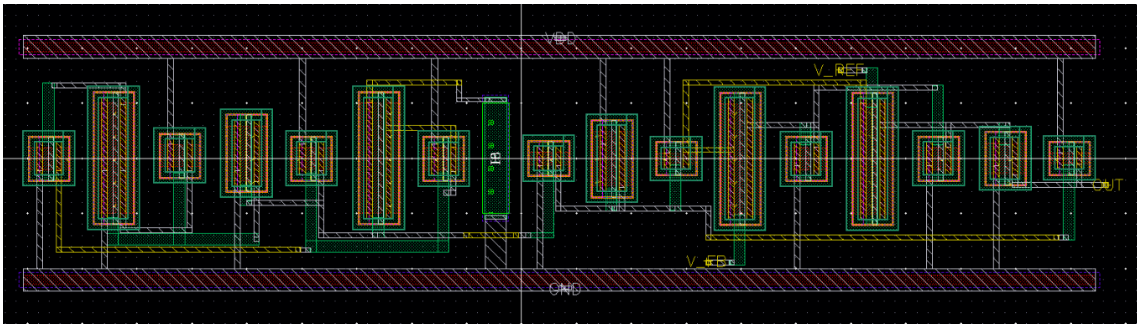


Figure 4.1: Layout of the Error Amplifier

XFAB foundry has some modules and some rules associated with these modules. In order to be sure that the foundry will be able to produce the integrated circuit that is drawn, these rules should not be violated. Therefore, Cadence has a tool named DRC (Design Rule Check) to check whether the rules of foundry has been violated or not. DRC has been done for the error amplifier, and no errors has been found.

All design rules might have been followed, but there may be wrong connections made in the layout. In order to be sure that all electrical connections have been made in a correct way, Cadence has a tool named LVS (Layout vs. Schematic). LVS checks whether schematic and layout match in terms of nets and connections in the design. LVS check has been done for the error amplifier and it has been seen that the schematic and the layout have matched.

DRC and LVS check have been done for all of the PWM controller blocks, and all of them have passes the checks. However, details of these checks are not given in the following sections.

4.2. SR Latch

Since SR latch consists of 2 NOR gates, layout of a NOR gate has been drawn first. While layout of the NOR gate can be seen in Figure 4.2, layout of the SR latch is given in Figure 4.3. NOR gate includes 2 nmva and 2 pmva transistors. On the other hand, SR latch consists of 2 NOR gates.

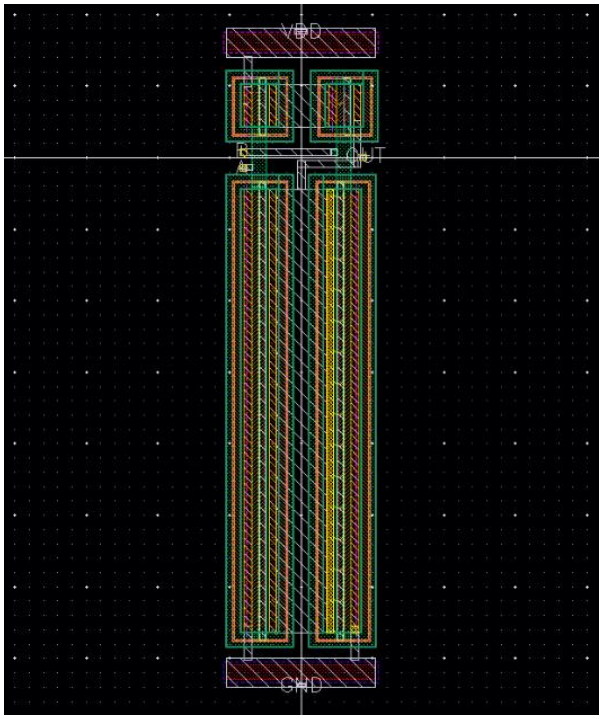


Figure 4.2: Layout of the NOR Gate

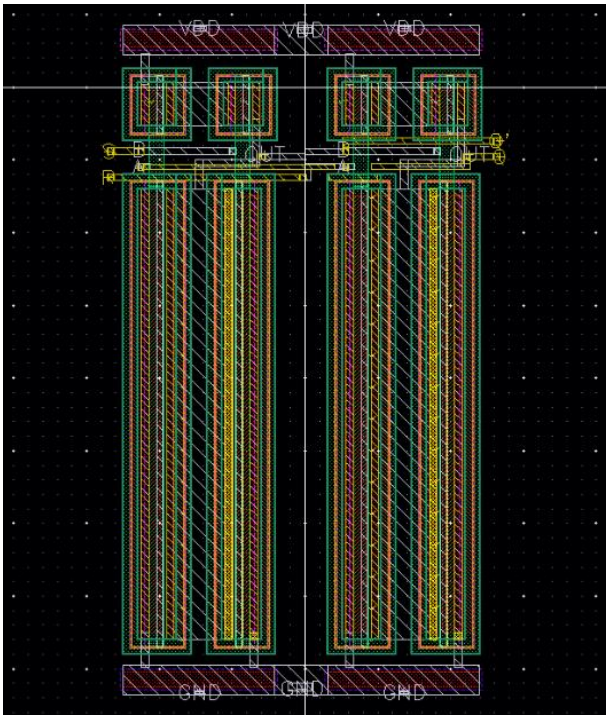


Figure 4.3: Layout of the SR Latch

4.3. Clock Generator

Layout of the clock generator can be seen in Figure 4.4. This circuit is composed of 6 nmva, 6 pmva transistors and a LOGIC0_5V circuit. This LOGIC0_5V circuit produces digital 0V. Since connecting gate of a transistor to a supply is risky in terms of ESD in integrated circuits, XFAB's readymade logic circuit has been used for connecting the gate of the transistor to 0V.

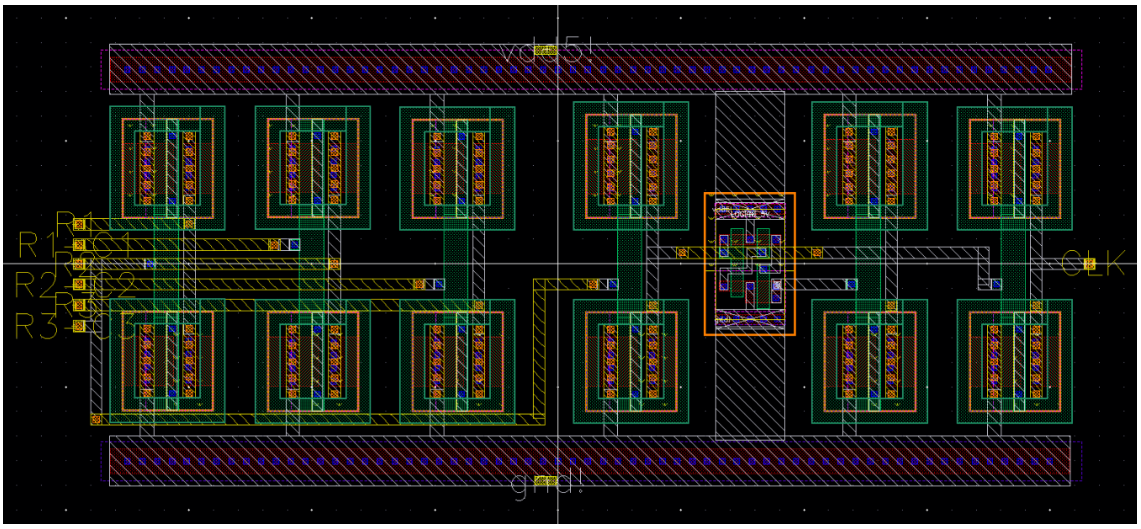


Figure 4.4: Layout of the Clock Generator

4.4. Voltage Reference

Layout of the voltage reference is given in Figure 4.5. Voltage reference includes 2 qnv5 BJTs, 4 rpp1 resistor and the error amplifier designed beforehand. Since one of the BJTs has a multiplication factor of 8, eight parallel BJTs have been drawn in the layout.

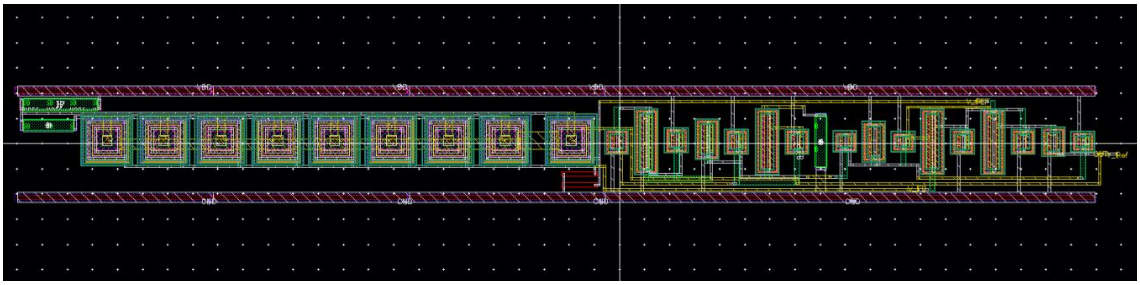


Figure 4.5: Layout of the Voltage Reference

4.5. Current Sense

Layout of the current sense can be observed in Figure 4.6. The circuit includes 3 qpva5 BJTs, 5 rpp1 resistors and an rpp1s resistor.

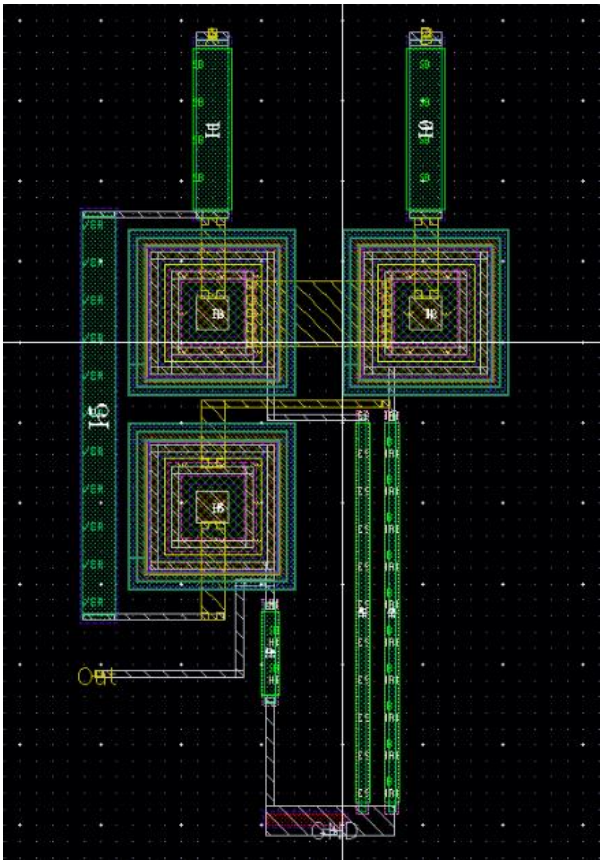


Figure 4.6: Layout of the Current Sense

4.6. Inverter

Layout of the inverter is given in Figure 4.7. It consists of an nmva and a pmva transistors.

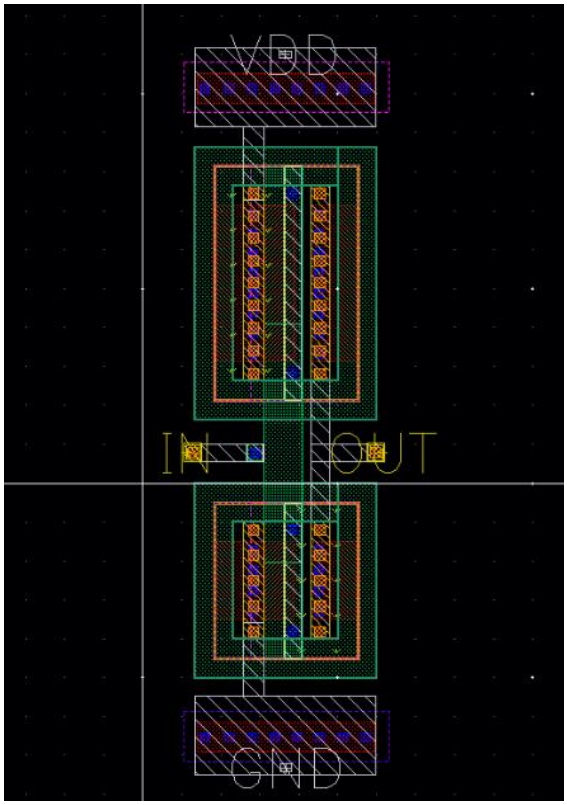


Figure 4.7: Layout of the Inverter

4.7. Overall PWM Controller

After layouts of all blocks have been completed, all these blocks have been brought together. All necessary connections between blocks have been made through MET1 and MET2 layers. Layout of the overall PWM controller can be observed in Figure 4.8.

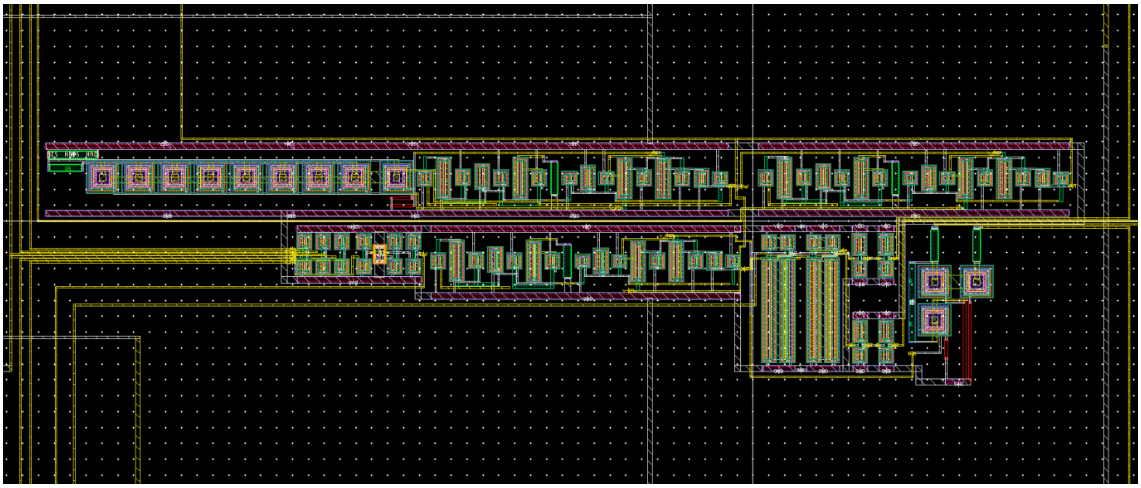


Figure 4.8: Layout of the Overall PWM Controller

Layout is extremely important in terms of power dissipation. Therefore, layout optimization has been made in order to produce a low-power PWM controller IC. As can be seen in Figure 4.8, all components have been placed close to each other in a compact manner and in a sequence as they have in the schematic. In this way, winding routes and overlapped metal layer area have been avoided. In the layout, only 2 metal layers have been used. This has also reduced the chance of overlapped area between metal layers. If overlap region is unavoidable, these areas have been kept as small as possible by reducing the widths of the routes on these areas.

Since ESD is extremely important in an integrated circuit, proper ESD protection pads have been used for input, output, input/output and supply pins in order not to damage the circuit when supplied. These ESD protection pads have been selected in the library of XFAB, and can be categorized as follows;

APR10DPC	->	Analog input/output
ISPC	->	Digital input
BT8BC	->	Digital output
VDDIPADPC	->	vdd5!
GNDIPADPC	->	gnd!
VDDORPADPC	->	VDDOR
GNDORPADPC	->	GNDOR
FILLER60PC	->	for filling blank regions
CORNER6PC	->	for filling corners

VDDOR and GNDOR nets are pad frame supplies and used in order to create a cage around the chip for better ESD protection. Fillers and corners are used for filling blank areas in layout. ESD protection pads have been placed in the layout by the help of fillers and corners as in Figure 4.9. Final layout view of PWM controller can be seen in Figure 4.10. Final chip size is 2.5mm x 3mm.

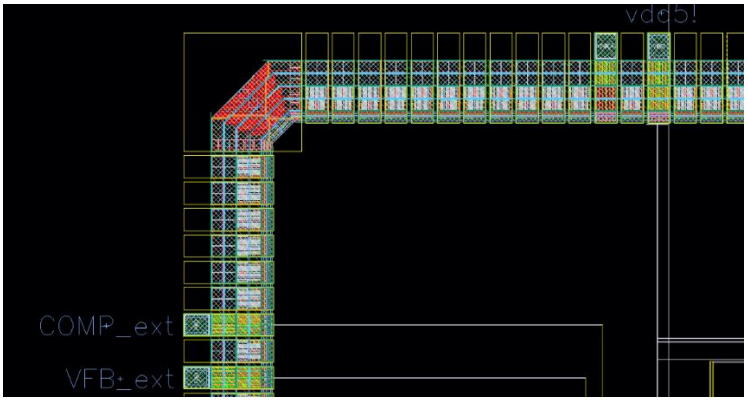


Figure 4.9: Placement of ESD Protection Pads in Layout

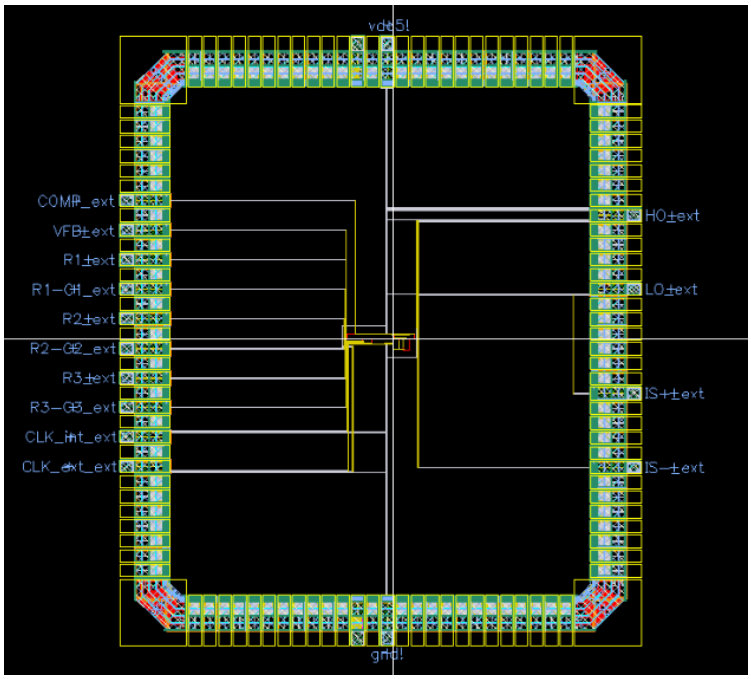


Figure 4.10: Final Layout View of the PWM Controller

After layout of PWM controller has been completed, DRC and LVS checks have been made in order to be sure that the design has obeyed all of the rules of XFAB and all of the connections have been made in a correct way. The results are positive.

This chapter covers layout details of the blocks of the PWM controller and the controller itself. Layout techniques used in order to reduce parasitic capacitances developed within the chip and lower the power dissipation of the controller are discussed. The details about how ESD protection pads are used are mentioned, and final layout view of the controller is given. The next chapter explains test process and test results of the PWM controller and the DC-DC converter designed.

CHAPTER 5

TEST & RESULTS

5.1. Packaging of the PWM Controller Integrated Circuit

PWM IC (Integrated Circuit) has been fabricated by XFAB after 6 months of production time using xt018 process. In this process, 0.18 μm SOI technology has been utilized. Micro-image of the IC is shown in Figure 5.1. Chip size is approximately 2.5mm x 3mm, and all of the pads are ESD protected. Since XFAB deposits a passivation layer on very top of the chip in order to protect it from contamination and humidity, only ESD protected pads are visible.

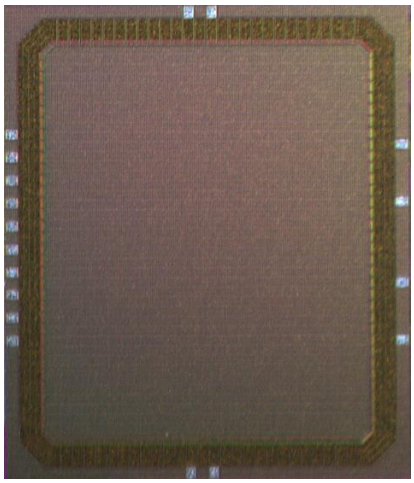


Figure 5.1: Micro-image of PWM Controller

A package for the IC was required in order to put it on a test PCB (Printed Circuit Board) properly. Since the chip size is approximately 2.5mm x 3mm, a package with the sizes appropriate for the chip has been selected. Part number of the chosen IC package is

CSB02813 from Spectrum Semiconductor Materials, Inc [49]. It is a DIP (Dual In-Line Package) socket and through-hole mounted on a PCB. In other words, its pins are soldered on the opposite side of the component. Since CSB02813 has 28 pins, it has a pin distribution as two parallel rows each having 14 pins. The image of the package is shown in Figure 5.2.

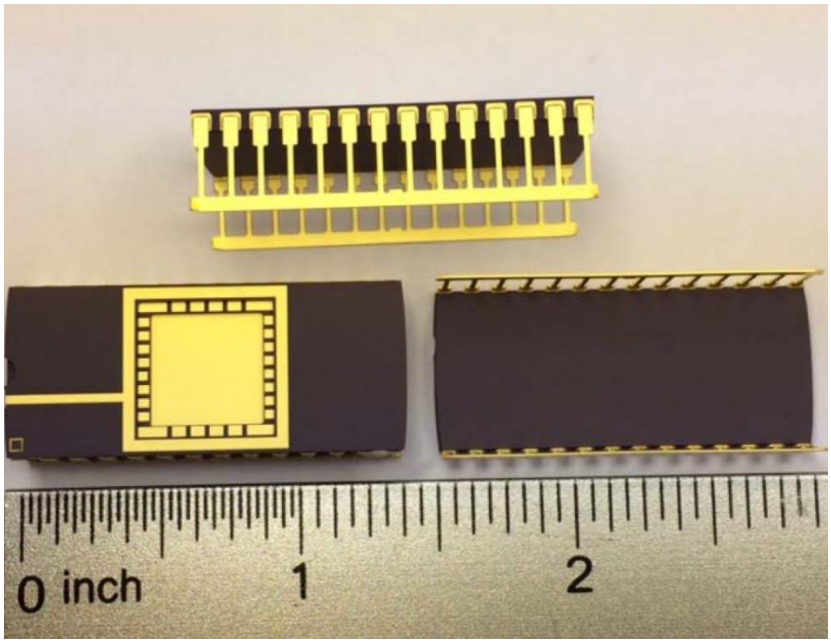


Figure 5.2: PWM Controller IC Package (CSB02813) [49]

Since wire-bonds create inductance, it is better to use wire-bonds as short as possible because inductance takes an important role and affects the circuit in high frequency designs. Furthermore, these parasitic inductances reduce the efficiency. Test circuit in this thesis has been operated at 10 MHz, so the outputs of the PWM controller had relatively high current switching rates. Therefore, wire-bonds have been made as short as possible and pin configuration has been made accordingly. Pin configuration is shown in Table 5.1. While lead numbers and mechanical dimensions of the package can be observed in Figure 5.3, bonding pattern of it can be seen in Figure 5.4. Dimensions are in inches in these figures.

Table 5.1: Pin Configuration of PWM Controller

1	vdd5!
2	VDDOR
3	-
4	COMP
5	VFB
6	R1
7	R1-C1
8	R2
9	R2-C2
10	R3
11	R3-C3
12	CLK_int
13	CLK_ext
14	-

15	GNDOR
16	gnd!
17	-
18	-
19	-
20	IS-
21	IS+
22	LO
23	HO
24	-
25	-
26	-
27	-
28	-

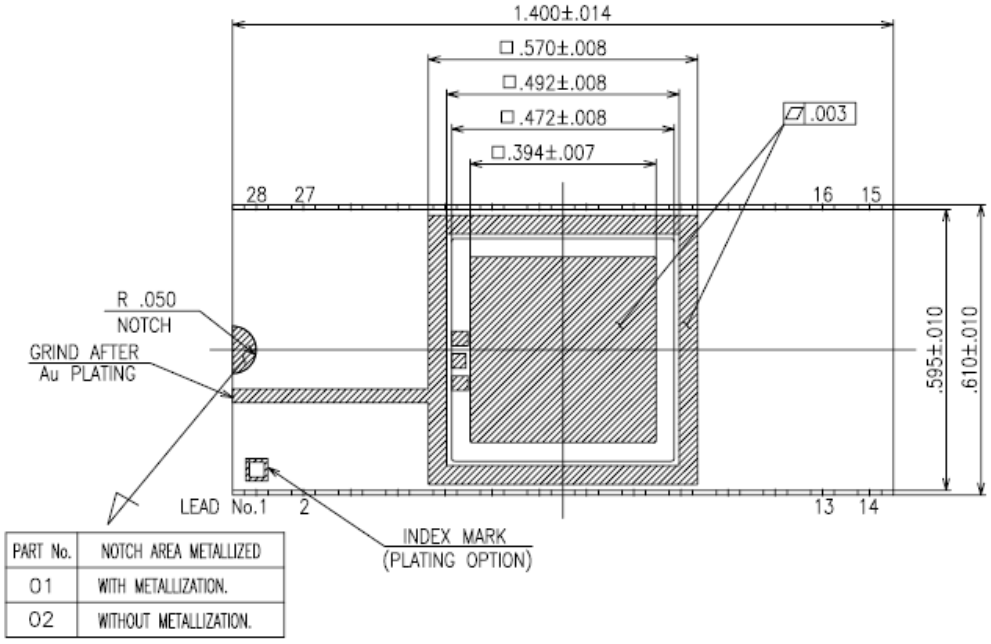


Figure 5.3: Lead Numbers and Mechanical Dimensions of CSB02813 [49]

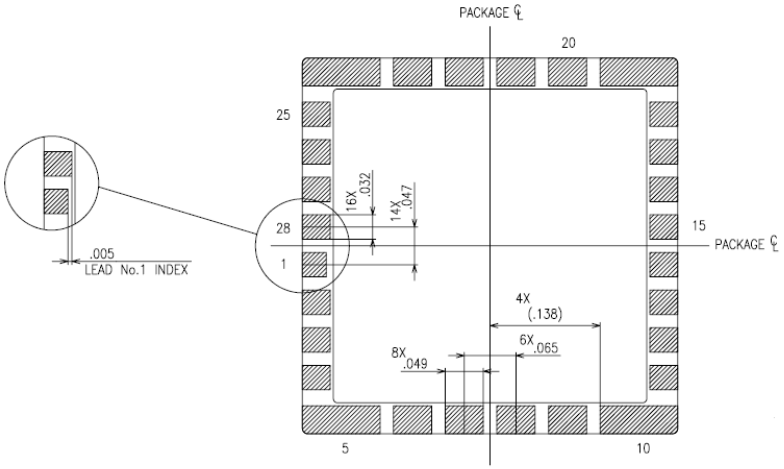


Figure 5.4: Bonding Pattern of CSB02813 [49]

Die of the PWM controller has been placed in the middle of the package, and wire-bonded according to the pin configuration given in Table 5.1. The image of PWM controller IC in its package after wires have been bonded can be seen in Figure 5.5. Details of wire-bonding can be observed in Figure 5.6. Wires are gold plated.

Figure 5.5: PWM Controller IC in the Package

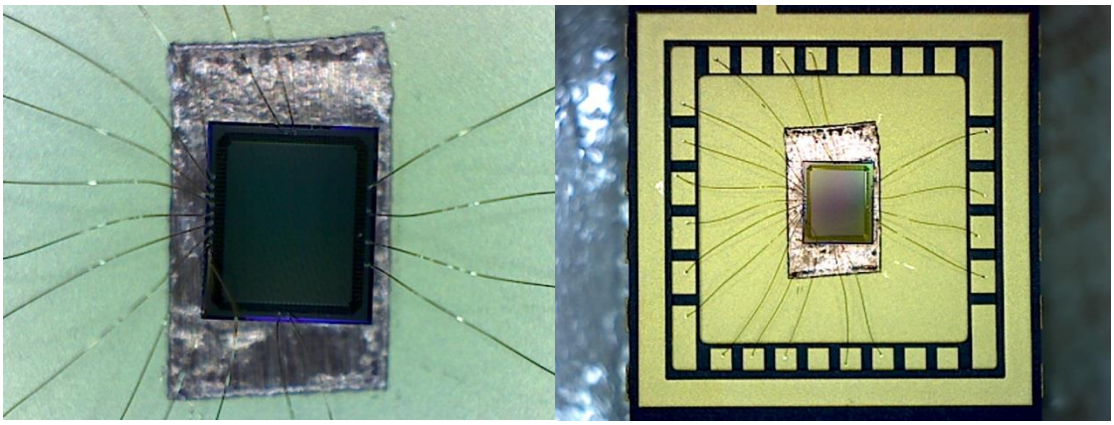


Figure 5.6: Details of Wire-Bonding

5.2. Test Board

In order to test the PWM controller IC, a test board with 2 layers has been drawn. In this test board, a buck-type converter including the PWM controller has been utilized. The schematic view of the test board can be seen in Figure 5.7.

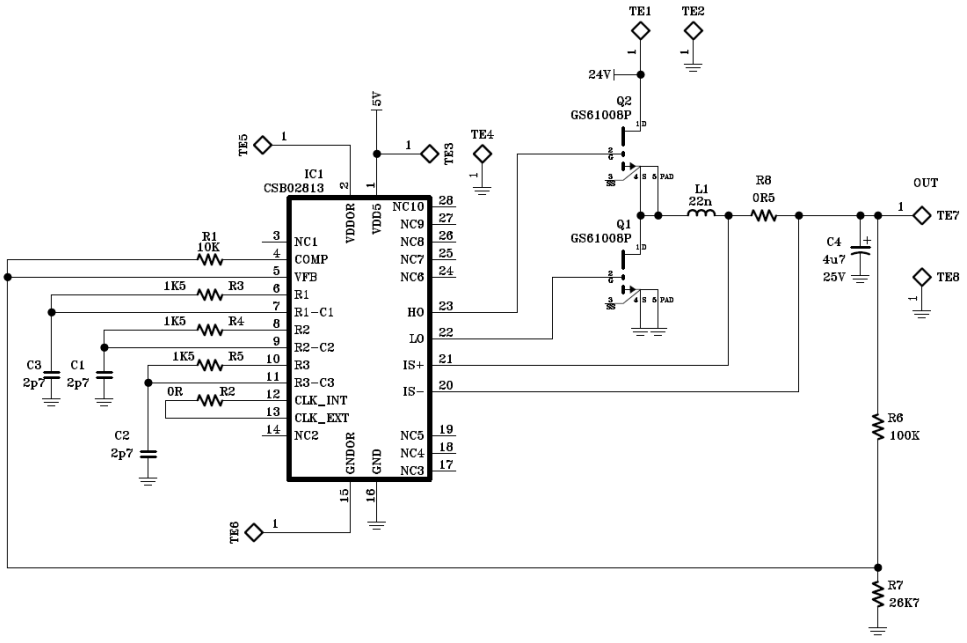


Figure 5.7: Schematic View of the Test Board

The buck converter includes 2 switching GaN FETs, which are GS61008P from GaN Systems. The circuit has a 22 nH output filter inductor whose rms current rating is 3 A. This inductor is from Midi Series Air Core Inductors from Coilcraft. It also contains a 0.5 Ω current sense resistor; which is a 2010 package, 1 W sense resistor. The output filter capacitor is a 4.7 μF tantalum-type capacitor. Other components are standard resistors and ceramic-type capacitors. The BOM (Bill of Materials) of the circuit is given in Table 5.2.

Table 5.2: Bill of Materials of the Test Board

Quantity	**Reference Number**	**Type**	**Value**	**Package**	**Tolerance**	**Voltage**	**Current**	**Power**
1	R1	Resistor	10k	0805	%1			0.1W
1	R2	Resistor	0R	1206				
3	R3, R4, R5	Resistor	1k5	0805	%1			0.1W
3	C1, C2, C3	Capacitor	2p7	0603	%1	200V		
1	R6	Resistor	100k	0805	%1			0.1W
1	R7	Resistor	26k7	0805	%1			0.1W
1	R8	Resistor	0R5	2010	%1			1W
1	C4	Capacitor	4u7	TAN-B	%20	25V		
1	L1	Inductor	22n	1812SMS	%2		3A	
2	Q1, Q2	GaN FET						
1	IC1	PWM Controller IC		CSB02813				

Test circuit is a buck converter whose input voltage is typically 24 V. Output voltage of the circuit can vary between 2.5 V and 4 V. In order to obtain a DC voltage at the output, PWM controller supplied from an external 5 V adjusts its duty cycle with the help of feedback taken from output voltage through a resistor voltage divider. There is also current feedback taken from R8 sense resistor because the converter uses CMC (Current Mode Control) method. Since there is a high-side (Q2) and a low-side (Q1) GaN FET in the circuit, this topology is a synchronous buck converter. One of the FETs is conducting

at a time. In order to adjust the frequency of PWM controller output; R3, R4, R5, C1, C2 and C3 are used. Their values have been chosen such that the switching frequency would be approximately 10 MHz. If clock signal is wanted to be given externally, R2 can be removed and external clock signal can be given at 13^{th} pin of the PWM controller. Finally, L1 and C4 constructs the output filter of the converter. Since the switching frequency is high, value of the inductor could be chosen as small as 22nH. This means that the sizes of filter elements are smaller than the ones in a standard converter with silicon MOSFETs in order to make a compact design.

Layout of the test circuit has been drawn using 2 layers. During layout, some points were needed to be taken care of. One of them was about ground connections. Since the frequency of the circuit is high, parasitic inductances built between pins and ground may become problematic. This may lead unwanted and different voltage levels seen on different ground points. Moreover, they cause extra and unwanted power dissipation in the circuit. In order to minimize parasitic inductances, traces have been kept as small as possible and a full ground plane has been made on the bottom side of the board. Other point was about sensing current. Since the sense resistor senses the main current flowing, it is wanted to sense it precisely. In order to increase precision of sensing, Kelvin connection has been used. Kelvin connection means that sense traces, which are the traces from sense resistor ends to receiving circuit, should be connected directly to sense resistor terminals and should be thinner than main current flowing path. This method minimizes the chance of incorrect reading.

The test board has been drawn and produced in Aselsan facilities. The final view of bare board can be observed in Figure 5.8. Dimensions of the board is 43 mm x 50 mm x 1.5 mm. Populated test board can be seen in Figure 5.9.

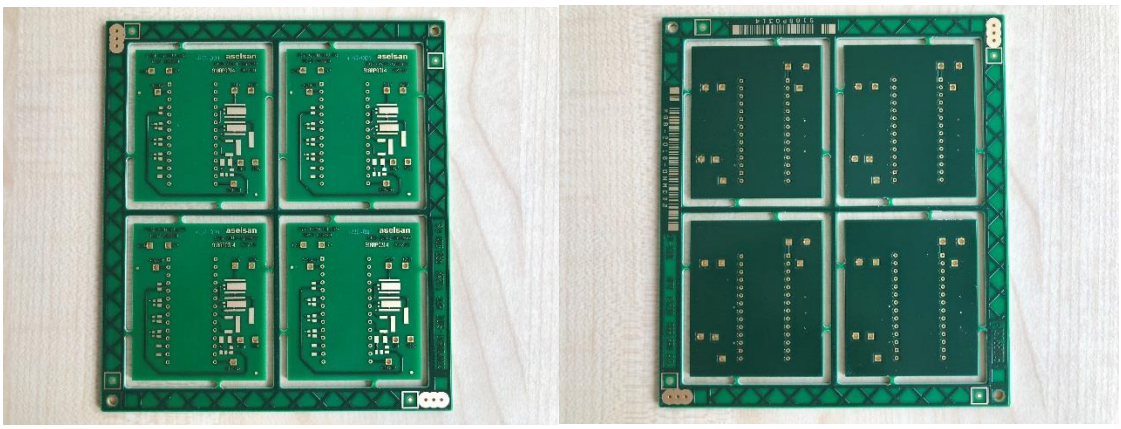


Figure 5.8: Bare Test Board

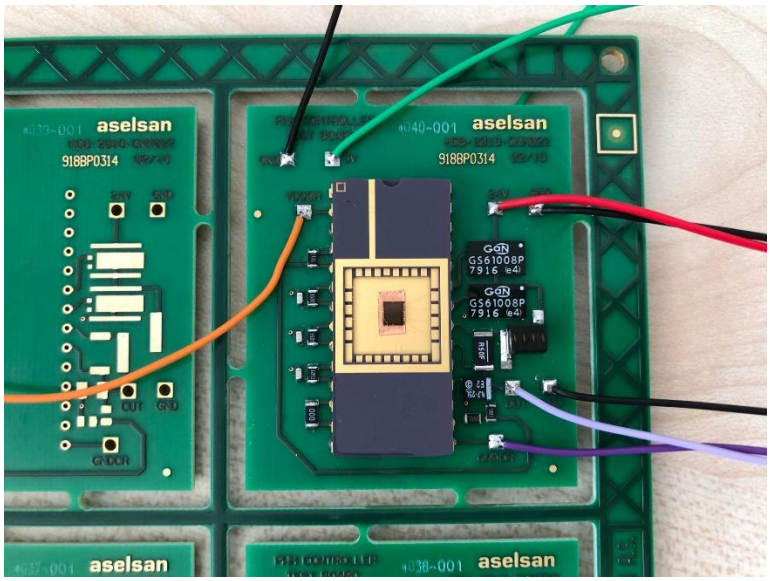


Figure 5.9: Populated Test Board

5.3. Test Results

In the beginning of tests, PWM controller IC has been tested separately from the test board. First of all, its clock generator block has been tested. 5V supply has been given and output of the clock generator circuit has been checked. It can be seen in Figure 5.10.

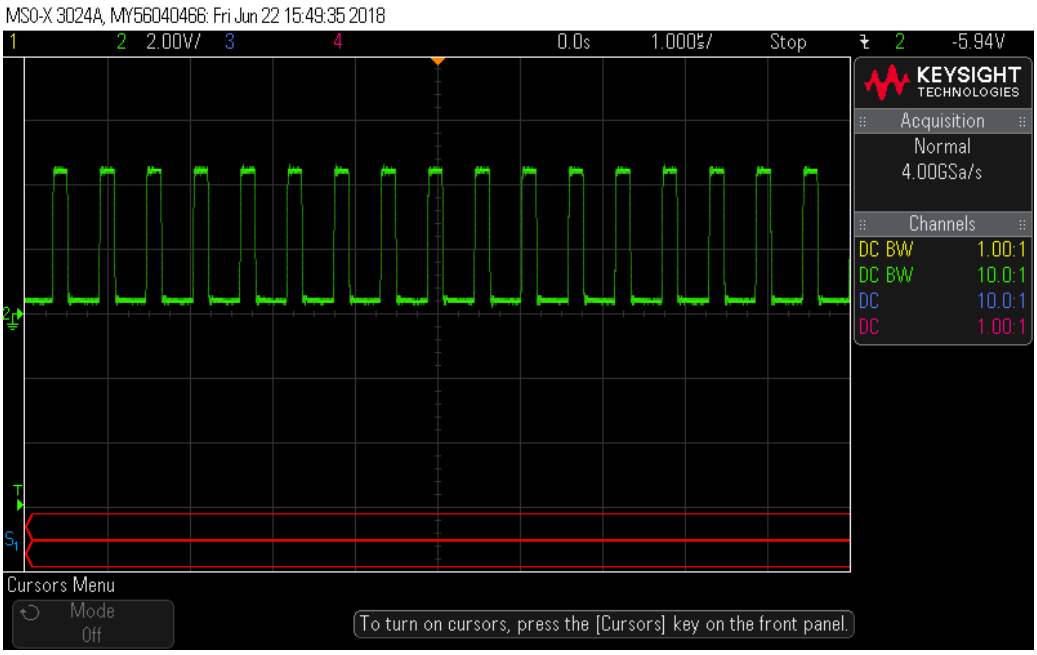


Figure 5.10: Output of the Clock Generator

It has been observed that the clock generator produces a clock signal whose duty cycle is %32. The duty cycle is as expected, but the frequency is lower (~2 MHz) than the expected value of 10 MHz. It may be due to inductances produced after wire-bonding and parasitic capacitances produced within the chip. However, frequency of the oscillator circuit can be adjusted by external resistors and capacitors. Therefore, it can be adjusted by changing their values accordingly. Furthermore, the chip has a "CLK_external" pin on which an external clock can be given in order to have a precise clock signal.

Second, set and reset signals have been sent to SR latch circuit externally, and outputs of the PWM controller (HO and LO) have been observed. Transition scenario can be seen in Figure 5.11. In the figure, Ch1 (yellow) is HO and CH2 (green) is LO. This is the transition time when set signal is sent to SR latch. It can be seen that logic of SR latch works properly. Rise and fall time of HO and LO can be observed in Figure 5.12. These times are between 10 and 15 ns. This means that the outputs of PWM controller is capable of driving at 10 MHz easily.

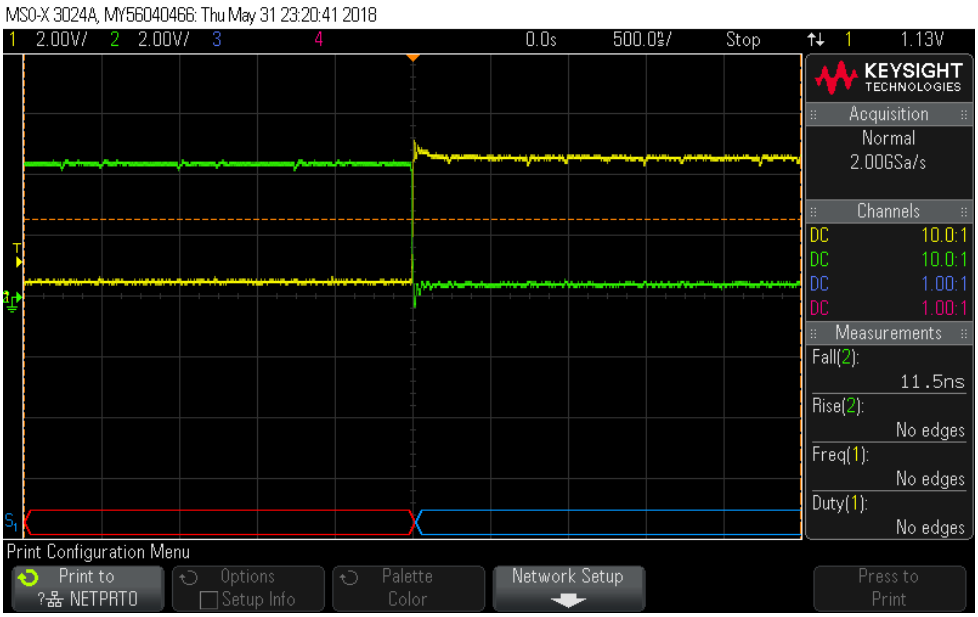


Figure 5.11: Transition of Outputs of the PWM Controller

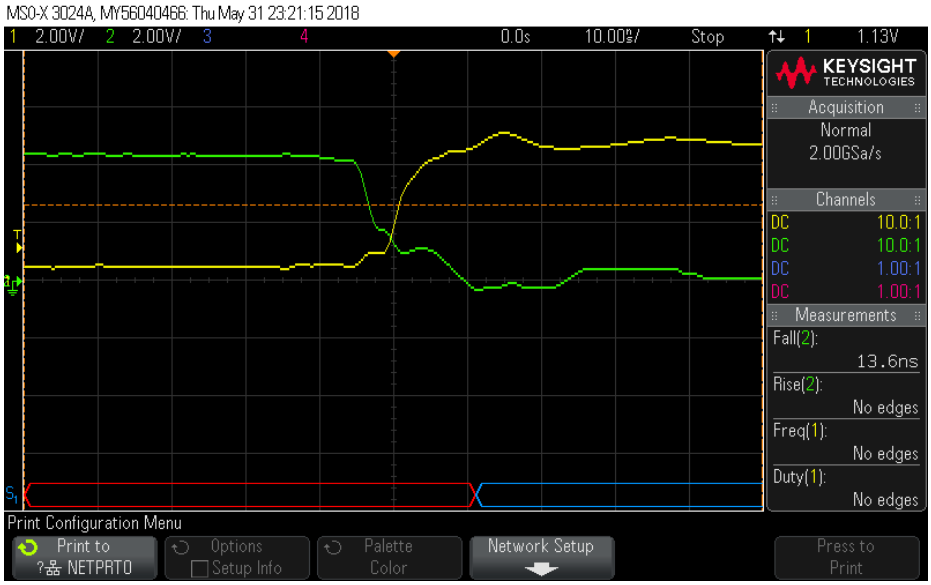


Figure 5.12: Rise and Fall Times of Outputs of the PWM Controller

After that, a clock signal at 10 MHz and corresponding reset signal have been given to PWM controller externally. These clock and reset signals are given in Figure 5.13. Ch1 (yellow) is clock and CH2 (green) is reset signal. Then, outputs of the controller (HO and LO) have been checked. Outputs can be seen in Figure 5.14. While Ch1 (yellow) represents HO, Ch2 (green) shows LO. From the figure, it can be observed that PWM controller is capable of giving a 10 MHz output. The time gap between HO and LO is approximately 10 ns, which is calculated as 12 ns in simulations. This shows that the delay generator circuit in PWM controller works properly. It gives switching transistors enough time before they switch their state, and reduces switching losses. In this way, it is proved that one of the efficiency enhancement methods discussed and proposed in this thesis has worked properly. Ripples on the signals are due to incapability of signal generator giving a pure square wave at 10 MHz. Harmonics produced by signal generator have been seen on outputs of the PWM controller.

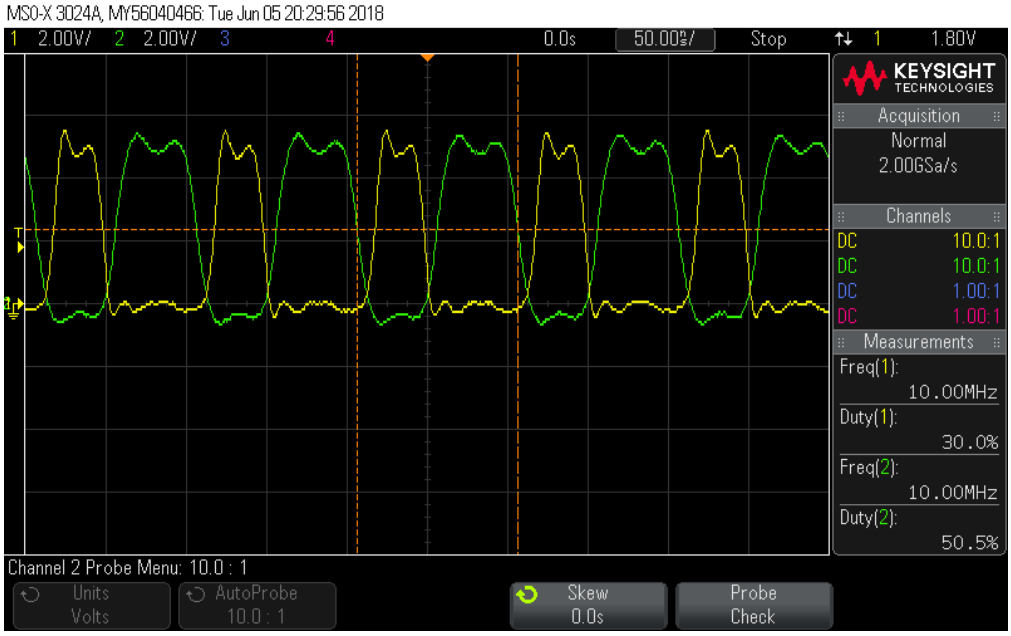


Figure 5.13: Clock and Reset Signals

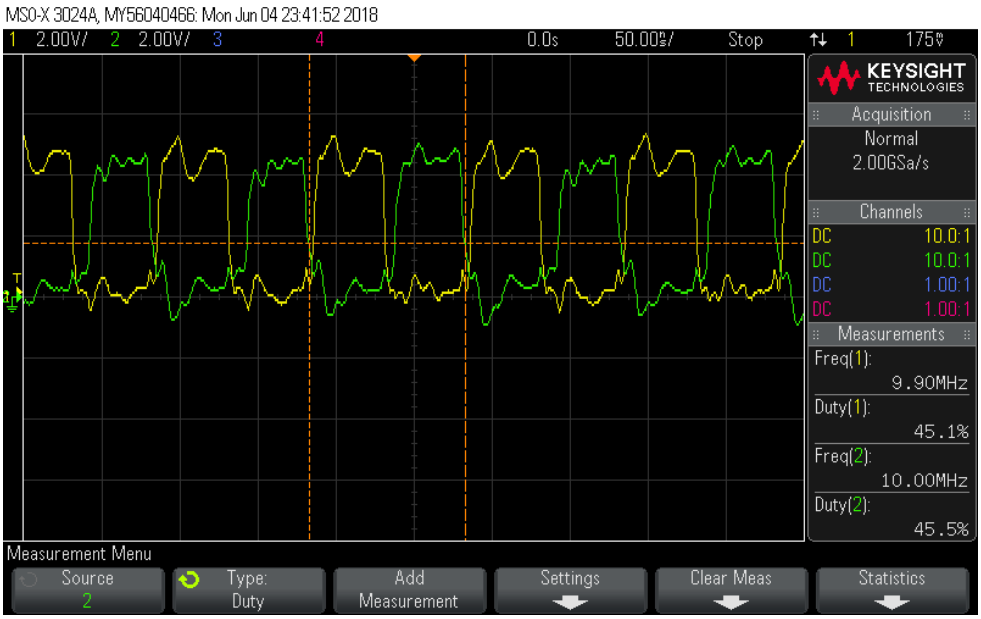


Figure 5.14: Outputs of the PMW Controller

Later, test circuit has been operated in open loop configuration by cutting feedback connection between output of the DC-DC buck converter and feedback pin of the PWM controller. Clock and reset signals have been given externally, and PWM controller has driven GaN FETs at 10 MHz. Duty cycle of PWM output was 45% as given in Figure 5.14. Since input capacitance of the GaN FETs is low, which is 588 pF, PWM controller was able to drive them at 10 MHz. As a result, 1 V_{DC} output of the converter has been seen with given 24 V_{DC} input. Input-output relationship can be seen in Figure 5.15 at start-up of the converter. Ch1 (yellow) represents input voltage, and Ch2 (green) represents output voltage.

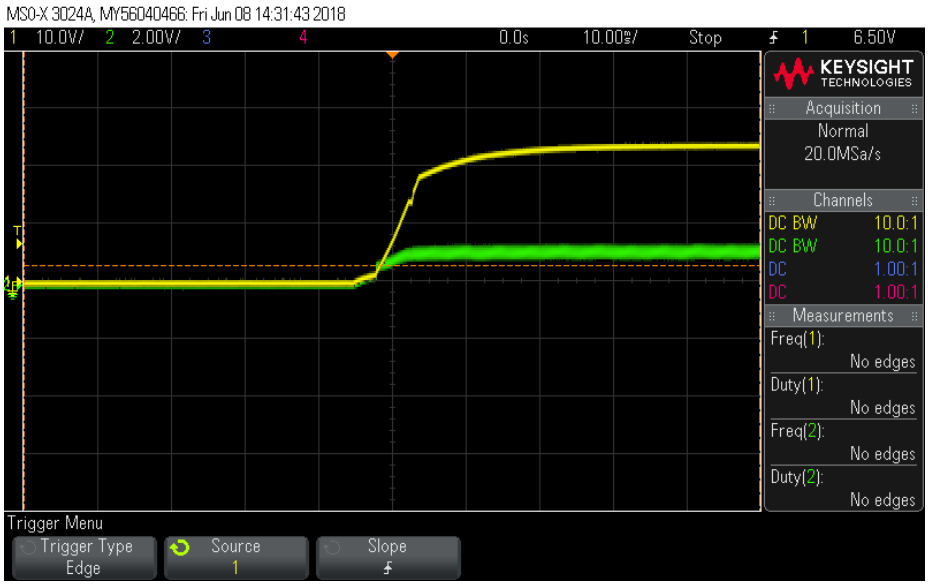


Figure 5.15: Start-up of the DC-DC Converter in Open Loop Configuration

After that, closed loop configuration has been tested. For this, output of the DC-DC buck converter and feedback pin of the PWM controller have been connected by a 10 kΩ resistor. In other words, test circuit has been fully operated. A clock signal with 10 MHz frequency and %32 duty cycle has been given externally. PWM controller chip has been supplied with 5 V, and 24 V_{DC} input has been given. PWM controller has driven GaN FETs at 10 MHz. Input-output relationship in closed loop configuration can be observed in Figure 5.16. Ch1 (yellow) represents input voltage, and Ch2 (green) represents output voltage. It can be observed from the figure that output voltage has reached steady-state without any over-shoot. This shows that the closed loop configuration is stable.

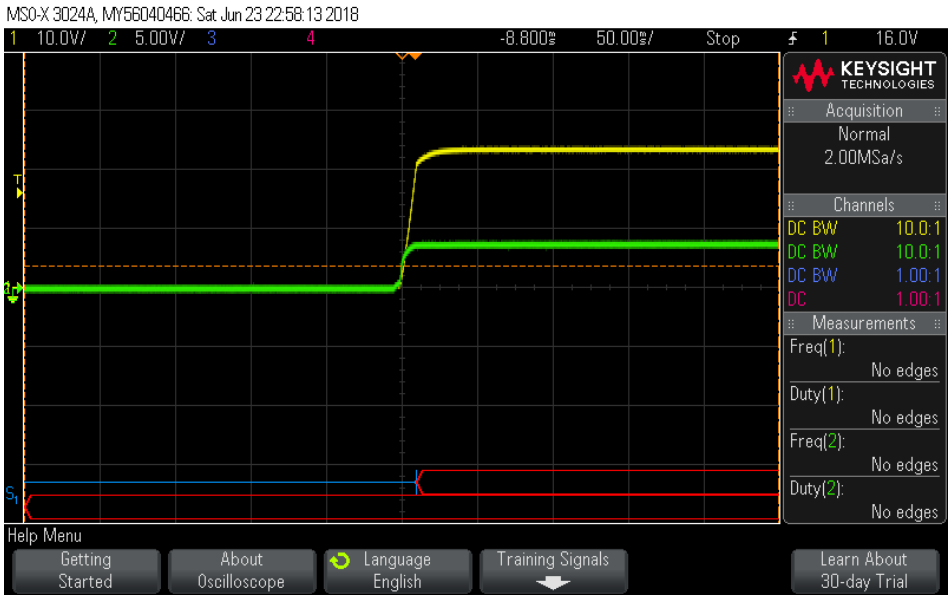


Figure 5.16: Start-up of the DC-DC Converter in Closed Loop Configuration

In this closed loop configuration, DC-DC converter has been operated with a 100 mA constant current load. With given input voltage of 24 V_{DC}, output voltage has been measured as 3 V_{DC} with this feedback configuration and load. Output voltage with 10 MHz clock signal can be observed in Figure 5.17. After the circuit has reached steady-state condition, change of output voltage has been observed at transition from full-load to no-load case. This transition can be seen in Figure 5.18. In these figures, Ch1 (yellow) represents input voltage, and Ch2 (green) represents output voltage. It is seen that the transition is smooth without any over-shoot. This means that load regulation of the feedback loop is good.

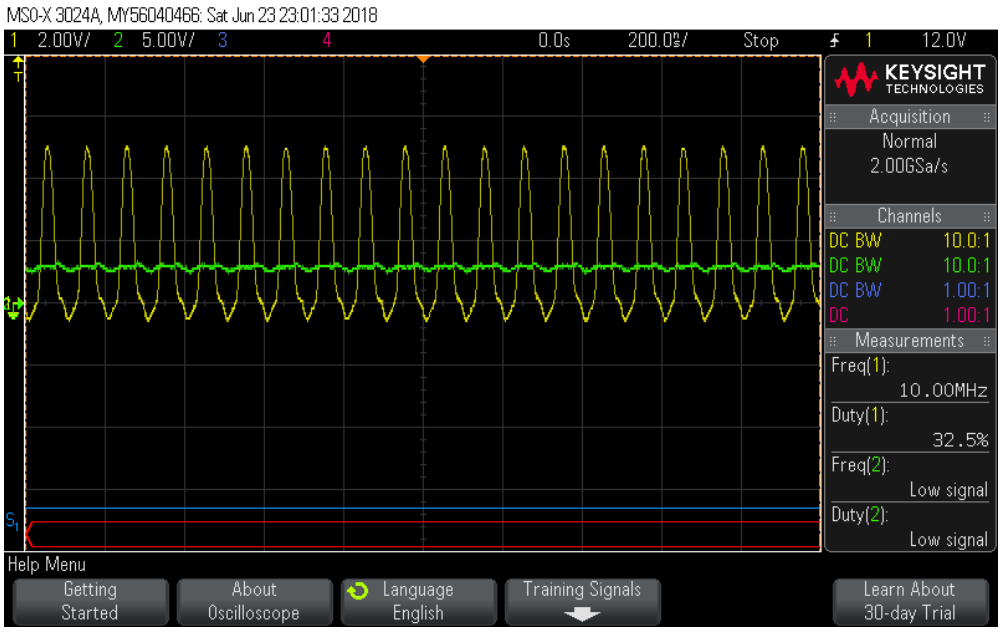


Figure 5.17: Output Voltage with Clock Signal

Figure 5.18: Full-load to No-load Transition

In section 2.4 of this thesis, it is stated that the maximum input voltage of the DC-DC converter should be 30 V. Therefore, the converter has also been tested with 30 V input. Input-output relationship in closed loop configuration for 30 V input can be observed in Figure 5.19. Ch1 (yellow) represents input voltage, and Ch2 (green) represents output voltage.

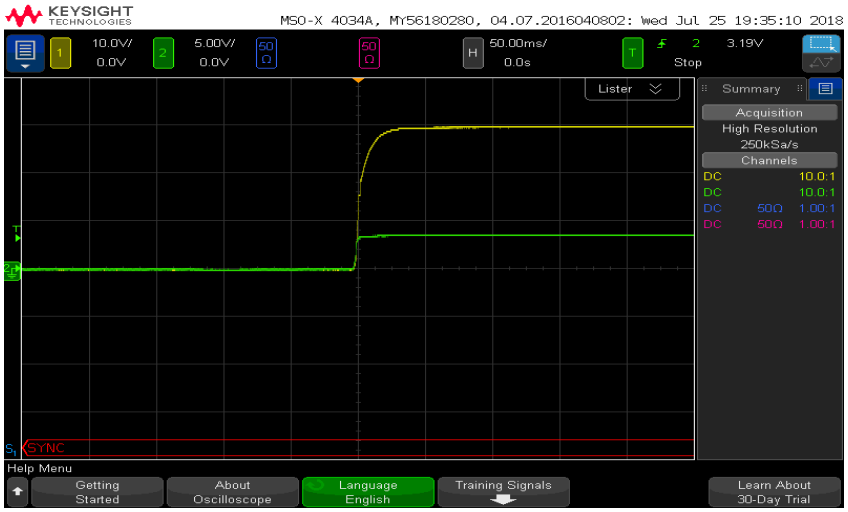


Figure 5.19: Start-up of the DC-DC Converter in Closed Loop Configuration with 30 V Input

In section 2.4 of this thesis, it is also proposed that the maximum output current of the PWM controller should be 10 A. In Figure 5.12, it can be seen that the rise and fall times of the outputs of the controller is around 10 ns. Therefore, the specification can be proved by

$$I_{max} = C \frac{dV}{dt} \tag{5.1}$$

where, I_{max} is the maximum output current of the PWM controller, C is the gate capacitance of the GaN FET used and dV/dt is the rise and fall time of the outputs of the controller. C is 588 pF and dV/dt is 5V/10ns. Therefore, peak output current of the PWM controller for this design can be calculated as 0.3 A, which is lower than 10 A.

All of these tests proves that the PWM controller produced in this thesis with SOI technology works properly. Then, the current drawn by PWM controller from 5 V supply has been recorded. It is 3 mA, and can be seen in Figure 5.20. This value is slightly larger than the one seen in simulations due to wire-bond and setup cables creating impedance and the parasitic inductors developed within the chip. This means that the chip dissipates around 15 mW power in real life, and the specifications about supply current and power dissipation in section 2.4 of this thesis has been satisfied. The main objective of this thesis was to design a low-power PMW controller in order to increase the efficiency of the DC-DC converter. These results prove that the PWM controller designed in this thesis is really a low-power controller. Texas Instruments has an analog GaN FET controller device whose functionalities are similar to the controller in this thesis, namely TPS40400 [45]. Comparison table between TPS40400 and the PWM controller designed in this thesis can be seen in Table 5.3.

Figure 5.20: Current Drawn by the PWM Controller

Table 5.3: Comparison between TPS40400 and the PWM Controller Designed in This Thesis

	TPS40400 [45]	**PWM Controller Designed in This Thesis**
Typical Supply Current (mA)	6	3
Typical Power Dissipation (mW)	72	15

After measuring a 15 mW power dissipation of the PWM controller, efficiency calculations has been done for the optimal condition. The optimal condition for obtaining maximum efficiency has been observed when the input voltage of the DC-DC converter is 3.2 V and output load is 100 mA. At this condition, the output voltage is 3 V and input current drawn from 3.2 V is 108 mA. The power calculations can be done as

$$P_{PWM} = 15 \text{ mW} \tag{5.2}$$

$$P_{in} = (3.2 \text{ V})\ (108 \text{ mA}) = 346 \text{ mW} \tag{5.3}$$

$$P_{out} = (3.0 \text{ V})\ (100 \text{ mA}) = 300 \text{ mW} \tag{5.4}$$

where, P_{PWM} is the power dissipation of the PWM controller, P_{in} is the input power of the DC-DC converter and P_{out} is the output power of the DC-DC converter. Using these values, efficiency can be calculated as

$$\eta = \frac{P_{out}}{P_{in} + P_{PWM}} = \frac{300 \text{ mW}}{346 \text{ mW} + 15 \text{ mW}} = 83.1\% \tag{5.5}$$

where, η is the efficiency of the DC-DC converter. It proves that the specifications about efficiency in section 2.4 of this thesis has been met. This shows that the DC-DC converter has a high maximum efficiency when compared with most of its low-power counterparts in literature. The comparison table can be observed in Table 5.4.

In order to fulfill all specifications in section 2.4 of this thesis, the DC-DC converter has been operated at 500 mA load and its output voltage is adjusted to 2.5 V and then 4 V by divider resistors. The converter has shown a stable operation under these conditions.

Table 5.4: Comparison Table

	[37]	[38]	[39]	[40]	[41]	[42]	[43]	[44]	This Work
Process	130nm CMOS	130nm CMOS	180nm CMOS	130nm CMOS	250nm CMOS	180nm CMOS	350nm CMOS	350nm CMOS	180nm SOI
V_{in} (V)	1.2	1.2	1.8	2.5	3.6	1.8	3.3	2.5	3.2
V_{out} (V)	0.9	0.3 - 0.88	1.2	1.8	2.2	1.2	2.3	0.9 - 1.5	3
Max. loading (mW)	350	266	360	600	724	360	161	7.5	1500
Switching Frequency (MHz)	170	300	50	50	200	50	200	0.2 – 1	10
Filter Inductance (nH)	2	2	-	19.9	51	10	22	-	22
Max. Efficiency (%)	77.9	74.5	81.86	76.8	77	83.6	62	66.7	83.1

Test setup used during these tests can be observed in Figure 5.21.

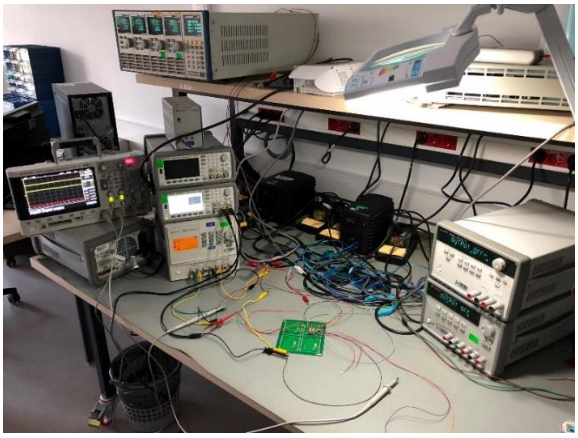


Figure 5.21: Test Setup

In this chapter, test process and test results of the PWM controller and the DC-DC converter are given. First, details of packaging of the PWM controller die is mentioned. The die is wire-bonded and packaged in order to place it properly in the test board. Then, design details of the test board is given. After that, test results are given and discussed. The PWM controller is able to drive the GaN FETs at 10 MHz frequency, and dissipates 15 mW low power. Maximum efficiency of the DC-DC converter is 83.1%. A comparison table comparing the results of this work and the ones of other works in the literature is given. A detailed discussion about this table is found in the next chapter. Next chapter also gives conclusions derived from this work and possible future works.

CHAPTER 6

CONCLUSION AND FUTURE WORK

6.1. Conclusion

In most of the applications today, high conversion efficiency for DC-DC converters is desired. The major objective of this work was to design a DC-DC converter having high conversion efficiency. Second objective was to make this converter compact by reducing the sizes of its filter elements.

In order to increase efficiency, low-power PWM controller IC design was focused on. A low-power PWM controller means low power loss in a DC-DC converter, and hence high efficiency. Low-power consumption of the PWM controller has been realized by applying the techniques proposed in this thesis. These were transistor size optimization, having minimum number of components inside the IC, layout considerations and design of assisting blocks like delay generator circuit. Besides, GaN devices has been used as switches in the DC-DC converter in order to further increase the efficiency. GaN has superseded silicon thanks to its attractive properties. GaN FETs have lower gate charge when compared to the ones in silicon MOSFETs, which reduces switching losses. It has lower channel resistance leading to reduced conduction losses. GaN also has lower leakage current, and can operate at higher temperature levels. Therefore, using GaN further increases the efficiency of the DC-DC converter. GaN is also a radiation resistant process, so it is an attractive material for space applications.

High frequency operation has been utilized in order to reduce the size of filter components, and make the DC-DC converter more compact. Again, GaN has helped the converter reach high switching frequencies without causing too much losses. GaN FETs

has lower input capacitance and gate drive voltage than the ones in silicon MOSFETs. Therefore, they provide high frequency operation in the order of MHz's without degrading the efficiency too much. On the other hand, the PWM controller was to be able to operate at high frequency levels. Therefore, SOI technology has been utilized. SOI has lower parasitic capacitances than the ones in standard CMOS process due to its buried oxide layer. This provides higher operation frequency levels for SOI. Moreover, SOI technology is an inherently radiation hardened process as GaN. Therefore, it is preferred in space applications.

In this thesis, a low-power radiation hardened PWM controller IC capable of driving GaN FETs and improving the efficiency of a DC-DC converter has been studied. First, schematics of individual blocks of the PWM controller and the controller itself have been drawn and simulations of them have been realized in Cadence environment. Error amplifier, SR latch, clock generator, voltage reference, current sense and inverter circuits have been drawn and simulated individually. Then, all blocks have been brought together and the overall PWM controller has been simulated. After being verified by simulation results, layouts of these blocks have been drawn. Later, ESD protection pads have been placed in order not to damage the IC during tests. After that, proper files have been sent to XFAB for production.

After 6 months of production time, the PWM controller IC has arrived. Then, tests have been conducted. Based on the results given in this work, the following conclusions and comments can be made:

- The PWM controller designed in this work draws 3 mA current from the supply. This low current is achieved by applying proposed methods. Choosing 500 nm minimum length for the transistors inside the IC reduces their input capacitance and instantaneous gate current. No extra elements and functionalities like UVLO or hysteresis are placed inside the IC leading to less current demand from the supply. Layout optimization is done in order not to create parasitic capacitances. These methods provides 3 mA low current drawn by the PWM controller IC.

- A 10 ns delay generated by the delay generator block of the PWM controller reduces switching losses across GaN FETs leading to reach high efficiency levels.
- Maximum efficiency level of 83.1% for the DC-DC converter is achieved when the input voltage of the DC-DC converter is 3.2 V and the output voltage is 3 V. This level is reached by low power consumption of the PWM controller IC, delay generation technique and using GaN devices as switches.
- 22 nH inductance value of the filter inductor of the DC-DC converter is achieved. This low level is reached by operating the converter at 10 MHz high frequency. 10 MHz is realized by utilizing GaN devices as switches and applying SOI technology on the PWM controller IC. This leads to compact filter and converter design.
- The PWM controller shows stable operation under 1500 mW load. This level is the tested maximum loading level of the DC-DC converter.

A comparison between the DC-DC converter designed in this work and the similar ones in other works in the literature is done in Table 5.4. As can be seen in the table, 83.1% maximum efficiency achieved in this work is higher than the most counterparts in the literature. However, efficiency should not be considered alone. There is a correlation and trade-off between efficiency, size, power density and cost. Most of the works in the table has an operation frequency higher than 10 MHz in order to make a more compact design. Therefore, their switching losses are higher and efficiencies are lower than the ones in this work. However, it can also be said that there is not too much difference between the filter inductance values. The lowest inductance value in the table is 2 nH [37], [38], but the size difference of a 2 nH and a 22 nH inductor is not significant. Therefore, the design in this work has advantages over them. On the other hand, there is a work in the table [41] whose filter inductance value is higher and efficiency value is lower than the ones in this work. Furthermore, one work in the table [44] has lower frequency and still lower efficiency levels than the ones in this work. All of these comparison results shows that this work contributes to literature in terms of design and implementation of an efficient and compact DC-DC converter.

6.2. Future Work

There are many opportunities for future research in order to improve the design proposed in this thesis. Some extra functionalities like UVLO (Under Voltage Lock-Out) or hysteresis between turn-on and turn-off voltage might be added to the PWM controller. The frequency level might be increased without degrading the efficiency by applying different PWM methods like digital implementation. This design has been simulated and tested only in a buck-type DC-DC converter. In the future, the design might be adapted to different converter topologies like flyback DC-DC converters having higher levels of input voltage. Besides, there are various III-V semiconductors and heterostructures in the market so that one of them might be chosen instead of GaN for more efficient solutions according to application. Moreover, different processes might be used instead of SOI in order to increase operating frequency further and lower the cost and production time. Since this study has focused on space applications, a radiation hardened process has been selected. For future studies, the produced PWM controller IC might be tested for TID or SEE in appropriate facilities in order to be sure that the chip is really radiation tolerant. On the other hand, it is possible to select a technology which is not inherently radiation hardened if the application is not associated with space or nuclear plants.

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