DEVELOPMENT OF A TUNER TOPOLOGY FOR MULTIHARMONIC MATCHING AND IMPLEMENTATION ON TUNABLE DUAL BAND POWER AMPLIFIER DESIGN

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
MIDDLE EAST TECHNICAL UNIVERSITY

BY

HASAN HÜSEYİN KILIÇ

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF DOCTOR OF PHILOSOPHY
IN
ELECTRICAL AND ELECTRONICS ENGINEERING

AUGUST 2018

Approval of the thesis:

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submitted by **HASAN HÜSEYİN KILIÇ** in partial fulfillment of the requirements for the degree of **Doctor of Philosophy in Electrical and Electronics Engineering Department, Middle East Technical University** by,

Prof. Dr. Halil KALIPÇILAR
Dean, Graduate School of **Natural and Applied Sciences** _____

Prof. Dr. Tolga ÇİLOĞLU
Head of Department, **Electrical and Electronics Engineering** _____

Prof. Dr. Şimşek DEMİR
Supervisor, **Electrical and Electronics Eng. Dept., METU** _____

Examining Committee Members:

Prof. Dr. Gönül TURHAN SAYAN
Electrical and Electronics Eng. Dept., METU _____

Prof. Dr. Şimşek DEMİR
Electrical and Electronics Eng. Dept., METU _____

Assoc. Prof. Dr. Mehmet ÜNLÜ
Electrical and Electronics Eng. Dept.,
TOBB University of Economics and Technology _____

Assoc. Prof. Dr. Tayfun NESİMOĞLU
Electrical and Electronics Eng. Dept., METU-NCC _____

Assist. Prof. Dr. Ahmet Hayrettin YÜZER
Electrical and Electronics Eng. Dept., Karabük University _____

Date: 13.08.2018

I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

Name, Last name : Hasan Hüseyin KILIÇ

Signature :

ABSTRACT

DEVELOPMENT OF A TUNER TOPOLOGY FOR MULTIHARMONIC MATCHING AND IMPLEMENTATION ON TUNABLE DUAL BAND POWER AMPLIFIER DESIGN

KILIÇ, Hasan Hüseyin
Ph.D., Department of Electrical and Electronics Engineering
Supervisor: Prof. Dr. Şimşek DEMİR

August 2018, 101 pages

In this thesis work, the effect of multi-harmonic load matching on improving the efficiency of power amplifiers is investigated. Techniques of efficient power amplifier design are discussed and analyzed in terms of multi-harmonic matching.

Several circuit topologies are evaluated for multi-harmonic matching by discussing the advantages and the limitations. Specifically, a detailed multi-harmonic analysis of the triple stub topology is presented. The already-known single frequency impedance matching capability of the triple stub circuit is extended to the 2nd and the 3rd harmonic frequencies. It is shown by analysis for the first time that the triple stub topology is able to satisfy impedance matching not only at the fundamental frequency but also at the 2nd and the 3rd harmonic frequencies simultaneously without any limitation on the fundamental and the harmonic impedances.

A novel, highly efficient dual band power amplifier utilizing a tunable triple stub load matching circuit is also designed and implemented. Thanks to the tunable structure, efficiency is maximized in both operating bands of the power amplifier; even tough, the upper band is located at the 2nd harmonic of the lower band.

Keywords: Multi-harmonic Matching, Triple Stub Topology, Dual Band Power Amplifier, High Efficiency Power Amplifier, Tunable Power Amplifier

ÖZ

ÇOKLU HARMONİK UYUMLAMA İÇİN UYUMLAYICI TOPOLOJİSİ GELİŞTİRİLMESİ VE ÇİFT BANTLI AYARLANABİLİR GÜÇ YÜKSELTECİ TASARIMINA UYGULANMASI

KILIÇ, Hasan Hüseyin
Doktora, Elektrik ve Elektronik Mühendisliği Bölümü
Tez Yöneticisi: Prof. Dr. Şimşek DEMİR

Ağustos 2018, 101 sayfa

Bu tez çalışmasında, çoklu-harmonik yük uyumlamasının güç yükselteçlerin verimliliğini artırmadaki etkisi incelenmiştir. Verimli güç yükselteç tasarımında kullanılan teknikler çoklu-harmonik uyumlama açısından ele alınıp analiz edilmiştir.

Çeşitli devre yapıları, avantajları ve kısıtlamalarından bahsedilerek, çoklu-harmonik uyum açısından ele alınmıştır. Özel olarak, üçlü saplama topolojisinin detaylı çoklu-harmonik analizi gösterilmiştir. Üçlü saplama topolojisinin, halihazırda bilinen tek frekans empedans uyumlama kabiliyeti, 2. ve 3. harmonik frekanslara da genişletildi. Analizle ilk defa gösterildi ki, üçlü saplama topolojisi, sadece ana frekansta değil, 2. ve 3. harmonik frekanslarda da aynı anda, ana ve harmonik empedanslarda bir sınırlama olmaksızın, empedans uyumlama yapabilmektedir.

Ayarlanabilir bir üç saplamalı yük uyumlama devresini kullanan orjinal bir yüksek verimli, çift bantlı güç yükselteç de tasarlanıp gerçeklenmiştir. Ayarlanabilir yapı sayesinde, üst çalışma bandı, alt çalışma bandının 2. harmoniğinde bulunmasına rağmen, verimlilik iki bantta da maksimize edilebilmiştir.

Anahtar kelimeler: Çoklu-Harmonik Uyumlama, Üçlü Saplama Topolojisi, Çift Bantlı Güç Yükselteç, Yüksek Verimli Güç Yükselteç, Ayarlanabilir Güç Yükselteç

To my wife Sevde and my son Muhammed Yiğit

ACKNOWLEDGEMENTS

I would like to thank Prof. Dr. Şimşek Demir for valuable supervision, guidance and motivation of this thesis for years.

I would like to thank Prof. Dr. Gönül Turhan Sayan and Assoc. Prof. Dr. Mehmet Ünlü for providing valuable suggestions during Thesis Monitoring Committee meetings and participating in the thesis defense jury.

I would like to thank Assoc. Prof. Dr. Tayfun Nesimoğlu and Assist. Prof. Dr. Ahmet Hayrettin Yüzer for participating in the thesis defense jury.

I would like to thank Wolfspeed Inc. for providing samples and nonlinear model of the GaN transistor. I would also like to thank Aselsan Inc. for its facilities I benefited during my thesis work.

I would like to express my gratitude to my friend Ümit Sarıer for his assistance during testing of the power amplifier. I would also like to thank my friends Sedat Pehlivan and Murat Aslan for their support while assembling the power amplifier.

Last but not least, I am grateful to my beloved wife Sevde Kılıç for her support, motivation and understanding during this thesis study. Finally, I express my deepest gratitude to my family for raising me and encouraging me throughout my life.

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LIST OF ABBREVIATIONS

1G	:	1st Generation mobile networks
2G	:	2nd Generation mobile networks (GSM/EDGE)
3G	:	3rd Generation mobile networks (WCDMA/HSPA etc.)
4G	:	4th Generation mobile networks (LTE)
5G	:	5th Generation mobile networks
DE	:	Drain Efficiency
DC	:	Direct Current
EDA	:	Electronic Design Automation
EDGE	:	Enhanced Data Rates for Global Evolution
EM	:	Electromagnetic
G	:	Gain
GaN	:	Gallium Nitride
GSM	:	Global System for Mobile Communications
GHz	:	Gigahertz, 10^9 hertz (unit of frequency)
HSPA	:	High Speed Packet Access
ICT	:	Information and Communication Technology
LTE	:	Long-Term Evolution
MHz	:	Megahertz, 10^6 hertz (unit of frequency)
PA	:	Power Amplifier
PAE	:	Power Added Efficiency
RF	:	Radio Frequency
WCDMA	:	Wideband Code Division Multiple Access

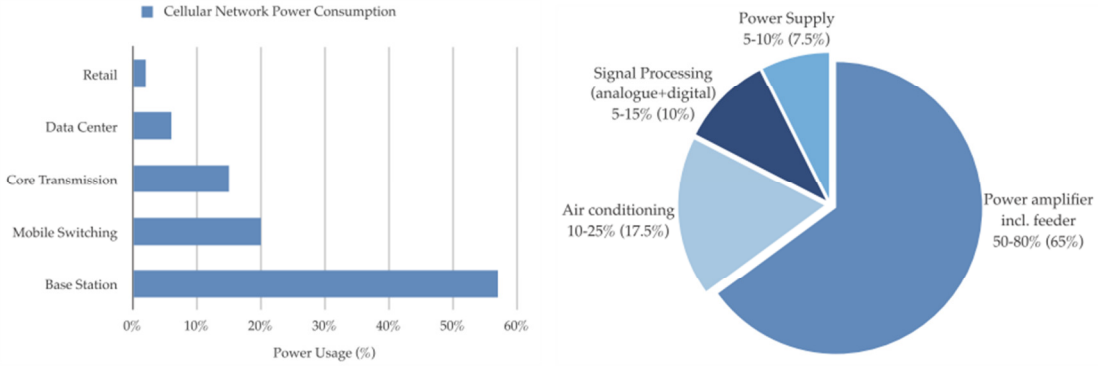
CHAPTER 1

INTRODUCTION

1.1 Motivation

With the rapid evolution of information and communication technology (ICT), next generation wireless communication systems are challenged by the emerging requirements. Higher data transmission speed requirements lead to operation at higher carrier frequencies. On the other hand, multiple radio frequency bands bring the requirement of multi-band and multi-mode operations. In addition to satisfying these requirements, mobile communication systems should be able to operate with minimum power consumption not only for reducing the operation cost but also for maintaining a green environment by reducing CO_2 emissions [1-5].

In a typical cellular (mobile) network, base stations are responsible from more than 55% of the overall power consumption as shown in Figure 1.1a [1], [2]. On the other hand, power amplifiers are the main consumer of power in a base station with an average of 65% share as Figure 1.1b states. Then, approximately a third of the cellular network power is only reserved for the power amplifier existing in the base station. Thus, maximizing the efficiency of the power amplifier significantly helps on reducing the overall power consumption of the mobile network. As a result, total CO_2 emissions from mobile networks, which is estimated to reach 345 million tons by 2020, will be reduced and this will contribute energy efficient wireless communication (green communication) to be established [5].



(a) **(b)**

Figure 1.1 Distribution of power consumption in a cellular network (a) and base station (b) [1]

Over the years, mobile technology advances and new generations of wireless networks become available as shown in Figure 1.2. 1st generation (1G) is an analog system providing transmission of voice; while, the 2nd generation (2G) is a digital system introducing services such as text messaging. 3rd generation (3G), introduced in early 2000s, provides faster data transmission speeds and enables services like video call and mobile internet. 4th generation (4G) is the current standard providing speeds up to 1 Gbps. Finally, 5th generation (5G) is the next generation wireless system and is expected to support huge number of mobile connections [7].

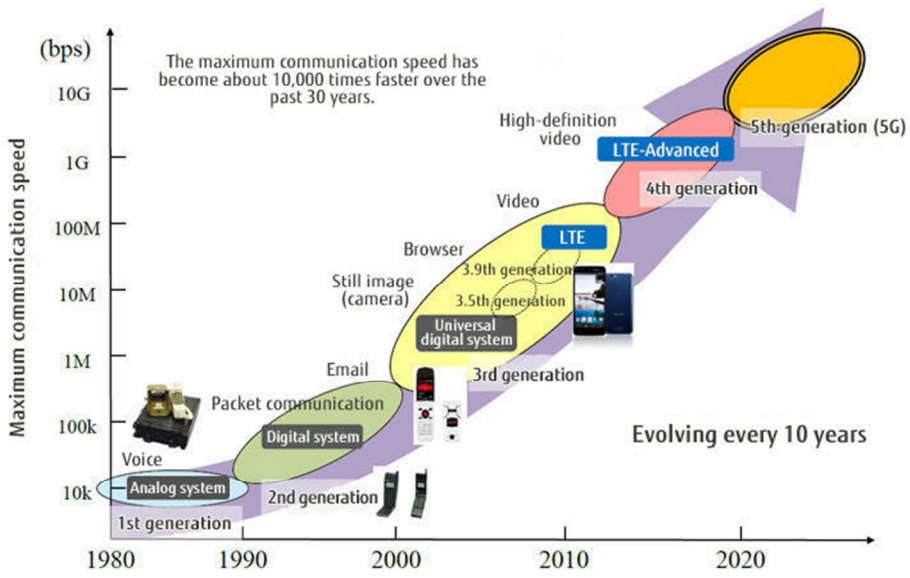


Figure 1.2 Evolution of mobile communication systems [6]

Figure 1.3 shows the trend in global mobile subscriptions by technology. It is estimated that total number of mobile subscriptions will reach 9.1 billion including 1 billion 5G subscriptions by the end of 2023 [8]. Even though 5G is expected to appear in 2020, the share of 2G, 3G and 4G will stay to be significant. Then, mobile systems and mobile devices should be able to operate at multiple bands to support different generations of the mobile systems. Therefore, efficient multi-band and broadband power amplifiers are required; in order to decrease the overall power consumption of the global mobile network.

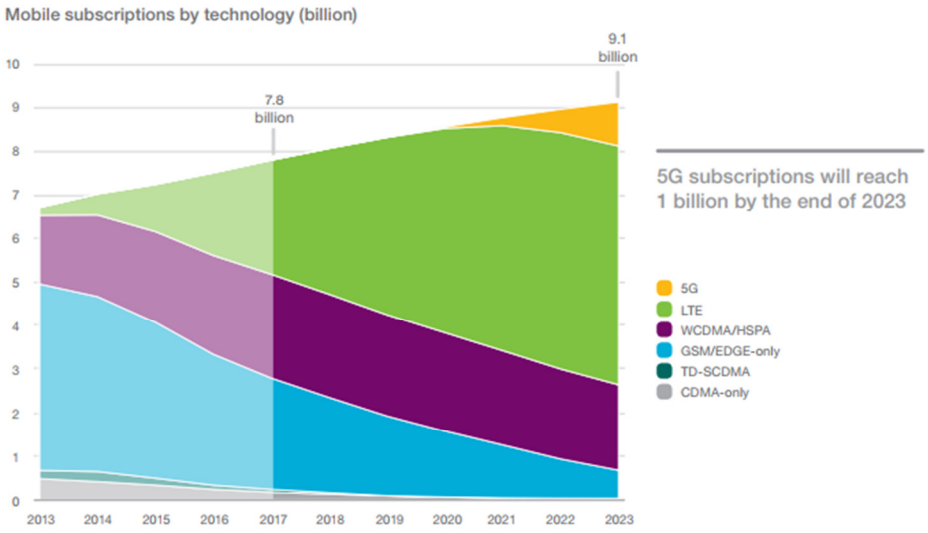


Figure 1.3 Global mobile subscriptions trend [8]

1.2 Research Objectives

This research has two main objectives as emphasized in the title of the thesis also. The first objective is to propose a tuner topology for multi-harmonic impedance matching. For this purpose, triple stub tuner, whose single frequency impedance matching capability is readily known, is analyzed. The impedances matched by the triple stub tuner are obtained analytically up to the 3rd harmonic frequency. Then, the obtained analytical expressions are examined by numerical optimization technique for simultaneous multi-harmonic matching.

The second objective of this thesis is to propose a tunable load matching circuit for a dual-band power amplifier to increase efficiency. The upper band

frequency of the power amplifier is aimed as twice the lower band frequency that brings the problem of optimum multi-harmonic load matching at both operating bands for maximum efficiency. In order to provide a solution to this specific problem, a tunable load matching circuit in the form of triple stub topology is proposed for the dual-band power amplifier.

1.3 Achievements

This research has led the following achievements;

It is shown that triple stub topology is able to perform impedance matching at the 2^{nd} and the 3^{rd} harmonic frequencies in addition to the fundamental frequency matching by tuning the lengths of the 6 transmission lines. A simple modification of triple stub topology utilizing 3 stub pairs is shown to provide reactive multi-harmonic matching by tuning the 6 stub lengths only. Then, a more easily tunable multi-harmonic impedance tuner can be obtained for an amplifier load pull system where only the stub lengths are varied.

A tunable, high efficiency dual band power amplifier is designed and successfully implemented to cover 1 GHz and 2 GHz frequency bands. Optimum 2^{nd} harmonic load at 1 GHz band is satisfied by tuning one stub length existing in the load matching circuit with the use of a pin diode. Then, more than 85% drain efficiency is achieved at 1 GHz. In addition, a technique for intelligent control of the pin diode is proposed and a simple band selective power detection circuit is designed for this purpose. By this way, self-tunable and concurrent dual-band PA operation can be obtained.

1.4 Thesis Outline

This thesis is composed of six chapters including this chapter. Chapter 2 and Chapter 3 are the review chapters. The scopes of the upcoming chapters are summarized as follows;

Chapter 2 presents an overview of high efficiency power amplifier structures. Specifically, the switch-mode and the harmonic-tuned power amplifiers are discussed in detail. Additionally, some recent researches related to high efficiency power amplifiers are mentioned.

Chapter 3 discusses the multi-harmonic matching circuits. The application areas of the multi-harmonic matching circuits are studied. Moreover, an investigation of the literature related to the commonly used circuit structures for multi-harmonic tuning is presented.

Chapter 4 provides a detailed analysis of the triple stub structure in terms of the 2^{nd} and the 3^{rd} harmonic matching in addition to the fundamental matching. Two different topologies of the triple stub circuit are analyzed for this purpose. First, the analytical expressions of the transformed fundamental and multi-harmonic impedances are obtained. Then, these expressions are optimized numerically to match with the predefined objective impedance points inside the smith chart. The results of this analysis show that it is possible to match any combination of the fundamental, the 2^{nd} and the 3^{rd} harmonic loads with only a series transmission line integrated to the traditional triple stub matching circuit. Moreover, a simpler and more easily tunable circuit is proposed for purely reactive multi-harmonic matching to be used in single frequency power amplifiers.

Chapter 5 presents the design and implementation steps of a highly efficient tunable dual band power amplifier. At the beginning of the design, the operating bands of the power amplifier are aimed as 1 GHz and 2 GHz. This selection of the operating bands brings the problem of optimum harmonic load matching at the lower band since the 2^{nd} harmonic of the lower band overlaps with the upper band. To overcome this limitation, a novel, tunable load matching circuit is proposed to be able to satisfy optimum multi-harmonic matching in both operating bands for maximizing the efficiency of the power amplifier. It is also discussed how the power amplifier structure can be made self-tunable for automatic control of harmonic loads in both operating bands. For this purpose, a simple band-selective power detection

circuit, which can easily be integrated into the power amplifier circuit, is proposed and implemented.

Chapter 6 summarizes and concludes the work done for this research and discusses the future work this research may promote.

CHAPTER 2

HIGH EFFICIENCY POWER AMPLIFIERS

2.1 Introduction

There are several important specifications that need to be considered during power amplifier design. High output power is a critical parameter for an RF transmitter to be able to operate at extended ranges. On the other hand, high efficiency is required for minimizing DC supply requirements and optimizing the thermal performance. Linearity is another requirement especially in communication systems for appropriate transfer of the information data. All these three important parameters are difficult to be optimized simultaneously. Hence, a compromise should be made according to the application.

This chapter intends to provide a brief overview of the techniques used in high efficiency power amplifier design. The chapter starts with the definitions of drain efficiency (DE) and power added efficiency (PAE) which are the two frequently used terms to specify how much efficient a power amplifier is. Then, a review of the high efficiency power amplifier modes is presented. The switched-mode and harmonic-tuned approaches are analyzed in detail with a discussion of state-of-the-art results from the literature.

2.2 Measures of Efficiency in Power Amplifiers

Efficiency in power amplifiers is a measure of how much the DC power input is converted to the RF power output. The unconverted DC power is dissipated as heat which is a waste of energy. Hence, increasing the efficiency of a power amplifier means the reduction of the wasted energy.

Drain efficiency (DE) and power added efficiency (PAE) are the two definitions used to represent the efficiency of power amplifiers.

DE is a measure of how much the DC power is converted to the RF power. The mathematical expression of DE is given as;

$$\eta_{drain} = \frac{P_{RFout}}{P_{DCin}} \tag{2-1}$$

PAE, on the other hand, takes the RF input power into consideration also and uses the net RF power for calculating the efficiency. Then, PAE is expressed as;

$$\eta_{\text{power-added}} = \frac{P_{RFout} - P_{RFin}}{P_{DCin}} \tag{2-2}$$

It can be concluded from DE and PAE expressions that DE is always greater than PAE. Knowing that the RF input power and the RF output power are related by the power gain (G) of the amplifier, PAE can be expressed in terms of DE as;

$$\eta_{\text{power-added}} = \eta_{drain}\frac{G-1}{G} \tag{2-3}$$

Equation (2-3) shows that DE and PAE get close to each other as the power gain of the amplifier is increased. Table 2-1 shows PAE/DE ratio at various power gain levels. According to the results of Table 2-1, PAE and DE differ by 10% for a power amplifier with 10 dB power gain; whereas, PAE and DE are nearly the same when the power gain is increased to 30 dB.

Table 2-1 PAE/DE ratio at various gain levels

Gain (dB)	*PAE/DE*
10	0.9
20	0.99
30	0.999

2.3 High Efficiency Power Amplifier Modes

Power amplifiers can be classified into several modes (classes). The differences in the biasing points and the load impedances lead to different classes of operation. There is always a tradeoff between the linearity and the efficiency in the power amplifier design. Hence, power amplifier modes can be grouped into two main categories; namely, linear modes and high efficiency modes [9].

Linear power amplifier modes include classes; A, AB, B and C. The main difference between these modes is the biasing point of the active device which affects the conduction angle. Class-A amplifier has the best linearity with 360 degrees of conduction angle. However, the maximum theoretical efficiency of a Class-A amplifier is 50%. The linearity degrades from Class-A through Class-C; since, the conduction angle decreases as can be seen from Table 2-2. On the other hand, drain efficiency improves from Class-A through Class-C.

Table 2-2 Comparison of linear power amplifier modes [10]

Power Amplifier Class	Conduction Angle (Degrees)	Drain Efficiency (%)
Class-A	360	50
Class-AB	180-360	50-78.5
Class-B	180	78.5
Class-C	<180	78.5-100

High efficiency power amplifiers can be classified as switch-mode and harmonic-tuned amplifiers [11]. In switch-mode operation, the active device (transistor) is operated as a switch [12]. Class-D and Class-E amplifiers are the two examples of the switch-mode amplifiers. On the other hand, harmonic-tuned amplifiers such as Class-F, Inverse Class-F and Continuous Class-F, perform waveform shaping at the drain terminal of the transistor by presenting optimum harmonic terminations. Then, efficiency is maximized; since, non-overlapping drain voltage and drain current waveforms are formed.

In the upcoming sections the switch-mode and harmonic-tuned power amplifiers are handled in detail.

2.3.1 Switch-Mode Power Amplifiers

In switch-mode power amplifiers, the active device behaves a switch. Figure 2.1 shows the idealized circuit schematic of a switch-mode PA. The ideal switch used in Figure 2.1 presents a perfect short circuit and a perfect open circuit when it is "ON" and "OFF" respectively. Besides, the ideal switch makes instantaneous transitions between "ON" and "OFF" states.

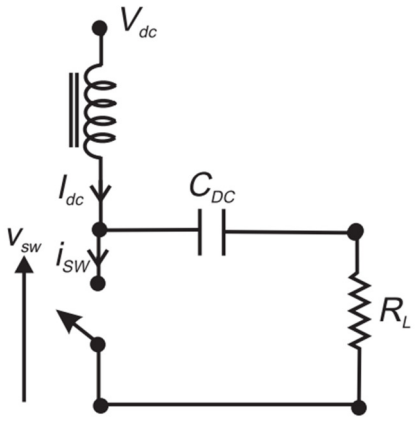


Figure 2.1 Idealized circuit of a switch-mode PA [9]

When the switch is "ON", current peaks and voltage vanishes across the switch terminals. On the other hand, when the switch is "OFF", voltage peaks and current vanishes. Then, the ideal voltage and current waveforms are obtained as given in Figure 2.2.

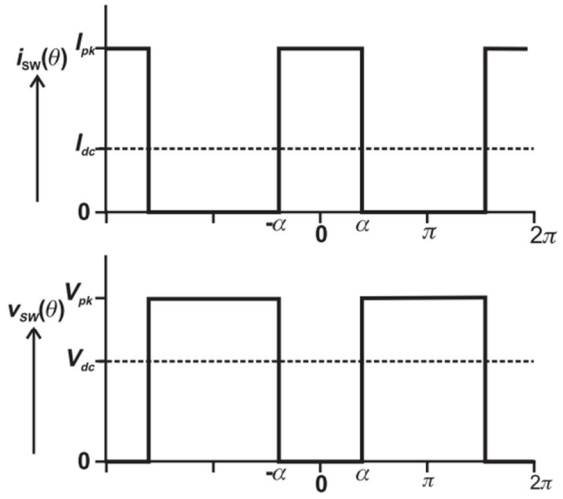


Figure 2.2 Idealized voltage and current waveforms of a switch-mode PA [9]

The non-overlapping current and voltage waveforms shown in Figure 2.2 imply zero power dissipation resulting in no heat dissipation. Despite the zero power dissipation, the efficiency of the idealized circuit is not 100% due to the harmonics of the voltage and current waveforms. The maximum efficiency is obtained as 81% when the waveforms are symmetrical square wave with 50% duty cycle [9].

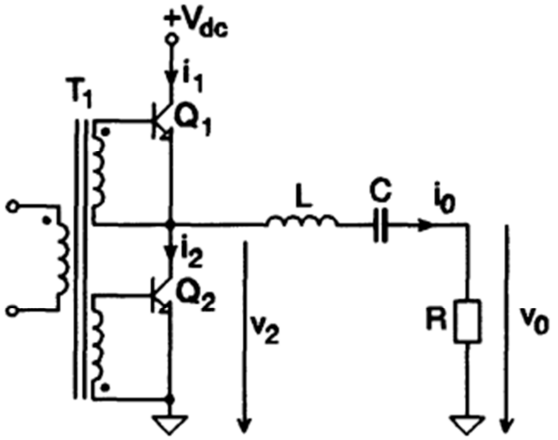
The two types of switch-mode power amplifiers are Class-D and Class-E amplifiers which are discussed in detail as the following.

2.3.1.1 Class-D PA

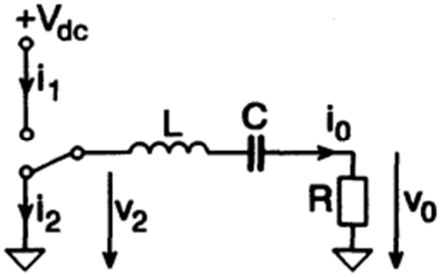
Class-D PA uses two alternately switched active devices for operation. Besides, there is a band-pass or low-pass filter at the load for harmonic suppression. Figure 2.3 shows the basic and the idealized circuits of a Class-D PA.

The active devices, Q_1 and Q_2, appearing in Figure 2.3 are alternately switched to "ON" and "OFF". Then, v_2 voltage can be expressed as a square wave with 50% duty cycle as given in (2-4).

$$\mathrm{v}_2(\theta) = \begin{cases} V_{DC}, & 0 \le \theta \le \pi \\ 0, & \pi \le \theta \le 2\pi \end{cases} \qquad (2\text{-}4)$$



(a)



(b)

Figure 2.3 Class-D PA; (a) basic circuit, (b) equivalent idealized circuit [13]

The series LC resonant circuit at the load side produces a sinusoidal current waveform at the output. Since the voltage waveform is a square wave when the voltage is switched, this structure is named as voltage-mode Class-D PA [17]. There is also current-mode Class-D PA where the current waveform is a square wave and the parallel LC resonant circuit at the load produces sinusoidal voltage waveform [16].

The switching losses arising from the parasitic capacitances and resistances of the active devices lead to nonzero switching times and degraded efficiency. In addition, the non-ideal resonant circuits limit the maximum efficiency of Class-D PAs. Hence, the practical operating frequency of Class-D PAs is restricted to several megahertz frequencies [14]

The design equations of Class-D PA with the switching losses taken into account are developed and presented in [15].

2.3.1.2 Class-E PA

Class-E PAs have been widely studied in the literature [18-23]. The circuit given in Figure 2.4 shows the idealized circuit schematic of a Class-E PA in which the active device is represented by an ideal switch. The C_P capacitor appearing in the schematic represents the parallel combination of the parasitic capacitor of the active device and the externally added capacitor. $L_S C_S$ series resonator is tuned to the operating frequency to maintain a sinusoidal current waveform.

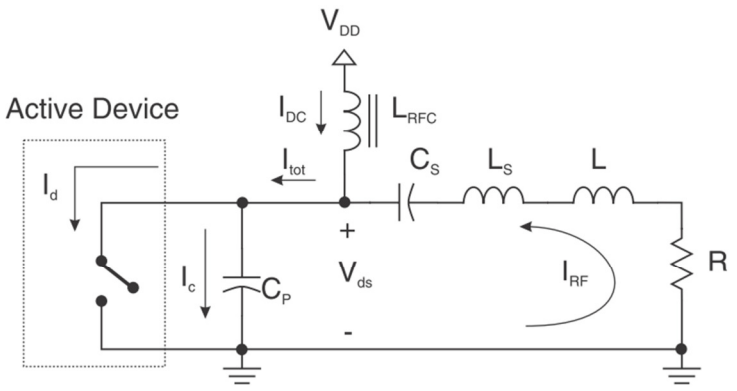


Figure 2.4 Ideal Class-E PA circuit [11]

Detailed analysis of Class-E PA is reported in [18] and [19]. 100% theoretical efficiency is not practically possible because of the non-idealities in both the active device and the external components. 80% PAE obtained at 0.5 GHz is reported in [20] with a transmission line Class-E PA design. In addition, DE greater than 80% is practically achieved in a 50% fractional bandwidth starting from 1.2 GHz and going up to 2 GHz [23].

2.3.2 Harmonic-Tuned Power Amplifiers

Harmonic-tuned power amplifiers have been widely researched due to their exceptional output power and efficiency performances at high frequencies [24-38]. In harmonic-tuned approach, proper voltage and current waveform shaping is carried out by multiple resonant load circuits for suitable harmonic terminations. By this way, the overlapping of voltage and current waveforms is avoided for zero power dissipation. The ideal operation requires the control of infinite number of harmonic loads to reach 100% theoretical efficiency. In a real application, control of harmonics greater than 3rd degree is not practical due to circuit complexity.

Harmonic-tuned power amplifiers can be classified as Class-F, Inverse Class-F and Continuous Class-F PAs. Class-F and Inverse Class-F PAs differ from the termination types of even and odd order harmonics. Both PAs require perfect open or perfect short terminations at harmonics. Hence, they are inherently narrowband. Continuous Class-F PAs do not require perfect open and perfect short harmonic terminations. Then, high efficiency can be achieved in a wider bandwidth as compared to Class-F and Inverse Class-F PAs.

2.3.2.1 Class-F and Inverse Class-F PAs

The idealized circuit schematic which can be applied to both Class-F and Inverse Class-F PAs is shown in Figure 2.5. Class-F PA uses open-circuit termination for odd order harmonics and short circuit termination for even order harmonics. On the other hand, Inverse Class-F (Class-F^{-1}) PA has even order harmonics short-circuited and odd order harmonics open-circuited. Then, Class-F PA produces square wave voltage waveform and half-sinusoidal current waveform. Similarly, Inverse Class-F PA generates half-sinusoidal voltage waveform and square-wave current waveform as shown in Figure 2.6. In both techniques, the current and voltage waveforms do not overlap; hence, no power dissipation occurs.

Most of the harmonic-tuned applications perform waveform shaping by tuning the 2nd and the 3rd harmonics only because of the practical reasons [24-30].

Then, the ideal current and voltage waveforms are approximated as maximally flat waveforms [24], [25]. This results in the reduction of the maximum achievable efficiency from the theoretical limit of 100%. When the 2nd and the 3rd harmonics are considered only, the maximum theoretical efficiency of a Class-F PA reduces to 90.7% [25].

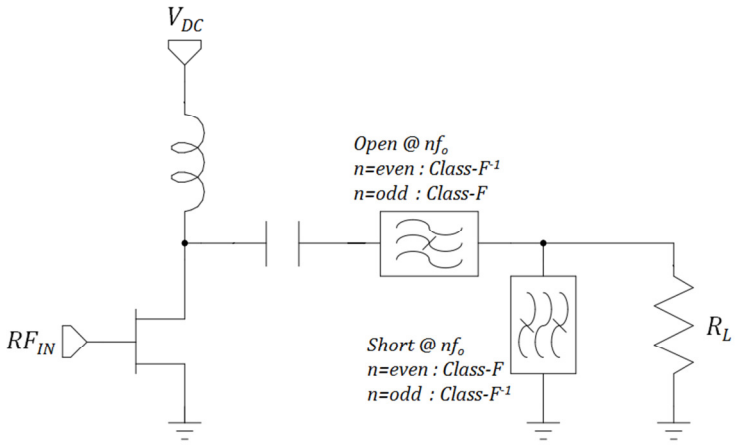


Figure 2.5 Class-F and Inverse Class-F (Class F^{-1}) structure with ideal harmonic terminations

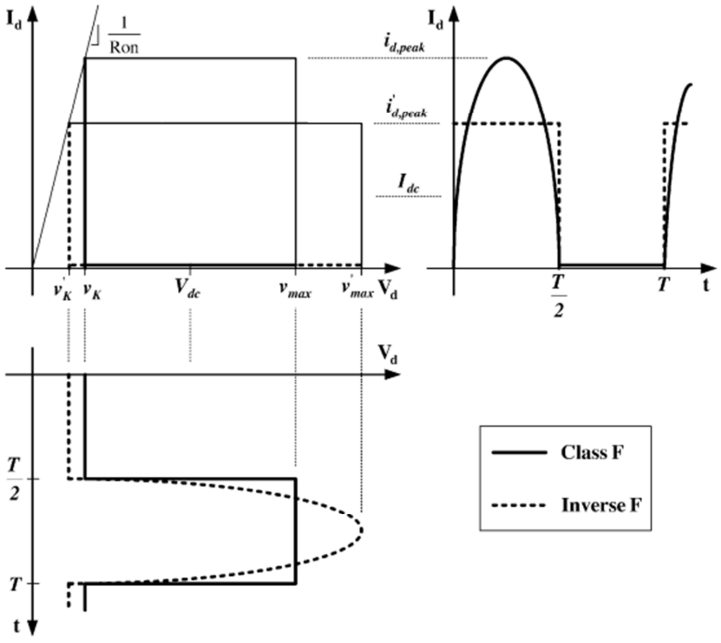


Figure 2.6 Ideal current and voltage waveforms of Class-F (solid line) and Inverse Class-F (dotted line) [26]

It is shown both by analysis and experimentally that Inverse Class-F PA has superior PAE performance compared to the Class-F PA under the same biasing condition when the active device has a finite on-resistance. [26]. On the other hand, Kim et al. presents similar PAE (~70%) and output power (>47 dBm) performances from Class-F and Inverse Class-F designs at 3.54 GHz [30]

The state-of-the-art PAE results for Class-F operation at 2 GHz and 3.1 GHz are presented in [27] and [28] respectively. Schmelzer and Long report a peak PAE of 85% and an output power of 16.5W at 2 GHz [27]. Chen and Peroulis obtained 82% PAE and 10W output power at 3.1 GHz by controlling the harmonics up to 4^{th} degree [28].

A state-of-the-art result for Inverse Class-F operation is presented in [31]. Roberg et al. designed and realized an Inverse Class-F PA with only the 2^{nd} and the 3^{rd} harmonics tuned producing PAE of 84% at 2.14 GHz.

A concurrent 0.8/1.25 GHz dual-band operation with Class-F operation in the lower band and Inverse Class-F operation in the upper band is realized in [32]. More than 80% PAE is obtained in both frequency bands.

2.3.2.2 Continuous Class-F PA

Class-F and Inverse Class-F PAs require perfect open and perfect short harmonic terminations as discussed before. Due to this requirement, these amplifiers have narrow bandwidth of operation.

Continuous Class-F mode is introduced as a harmonic-tuned PA technique realizing high efficiency in wider bandwidths. It is shown that the same output power and efficiency performances can be maintained with different combinations of the fundamental and 2^{nd} harmonic terminations as compared to the fixed terminations of typical Class-F mode where the 2^{nd} harmonic termination is restricted to be a short-circuit [33], [34]. Continuous Class-F mode assumes a perfect open termination at the 3^{rd} harmonic as in the Class-F mode.

As practical implementations of Continuous Class-F mode, an octave bandwidth (0.55-1.1 GHz) and 50% bandwidth (1.45-2.45 GHz) power amplifiers are realized and more than 70% DE is measured in [35] and [36] respectively.

Continuous Inverse Class-F mode is also devised as a wideband modification of Inverse Class-F mode [37]. It is shown that a broader solution space for the ideal open-circuit 2^{nd} harmonic termination of Inverse Class-F mode is possible for different fundamental loads without sacrificing the output power and efficiency performances. Then, thanks to this wider solution space of the fundamental and the 2^{nd} harmonic loads, bandwidth of the power amplifier can be extended. Similar to the Continuous Class-F mode, this mode also assumes the same perfect short 3^{rd} harmonic termination with the Inverse Class-F mode.

A Continuous Class F/F^{-1} mode transferring technique is developed and experimentally presented in [38]. By this way, it is shown that the bandwidth can be enhanced more as compared to the standard continuous modes.

2.4 Summary and Conclusions

In this chapter, the techniques used in high efficiency power amplifier design are discussed in detail. Initially, the techniques are classified as switch-mode and harmonic-tuned. Then, various classes of PA operation are investigated underneath the corresponding technique. The state-of-the-art results are also presented for each class of operation.

Switch-mode PAs are usually preferred in low frequency designs because of the simplicity of the structure. At high frequency, the non-ideal switching behavior of the active device causes reduced performance. Hence, harmonic-tuned PAs are the preferred and widely studied research area for high frequency, high efficiency PAs. Harmonically tuned PAs practically reach PAE values as high as 85% in narrowband applications [31]. Some broadband applications even exceeding octave-band are also reported in the literature with considerable PAE values greater than 70% [38].

CHAPTER 3

MULTI-HARMONIC MATCHING CIRCUITS

3.1 Introduction

Multi-harmonic matching is critical for high efficiency power amplifier design as stated in Chapter 2. Especially, harmonic-tuned approaches require specific harmonic terminations for appropriate waveform shaping. Then, a matching circuit is required at the load side of a power amplifier to present the active device both the optimum fundamental termination for maximum output power and the required harmonic terminations for maximum efficiency.

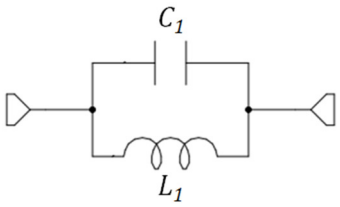
Multi-harmonic matching networks can be in the form of lumped or distributed. Lumped-element matching networks are generally preferred for low frequency designs [39-45]. On the other hand, distributed-element circuits are the preferred types of matching networks at high frequency applications [46-60].

This chapter provides an overview of multi-harmonic matching circuits employed in power amplifiers. First, examples of lumped-element matching networks are presented. Then, various forms of distributed-element circuits are analyzed.

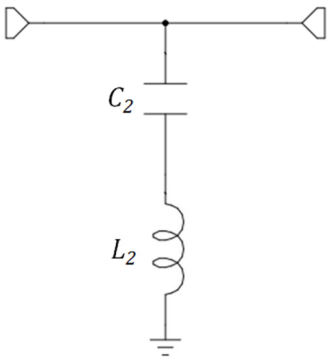
3.2 Lumped-Element Harmonic Matching Circuits

Class-F and Inverse Class-F PAs require perfect open and perfect short harmonic loads. Figure 3.1 shows two *LC* resonator circuits with resonant frequencies given in (3-1). The L_1C_1 resonator presents open-circuit at f_1 frequency. Similarly, a short circuit termination is obtained with the L_2C_2 resonator at f_2 frequency.

$$f_1 = \frac{1}{2\pi\sqrt{L_1C_1}},\ f_2 = \frac{1}{2\pi\sqrt{L_2C_2}} \tag{3-1}$$



(a)

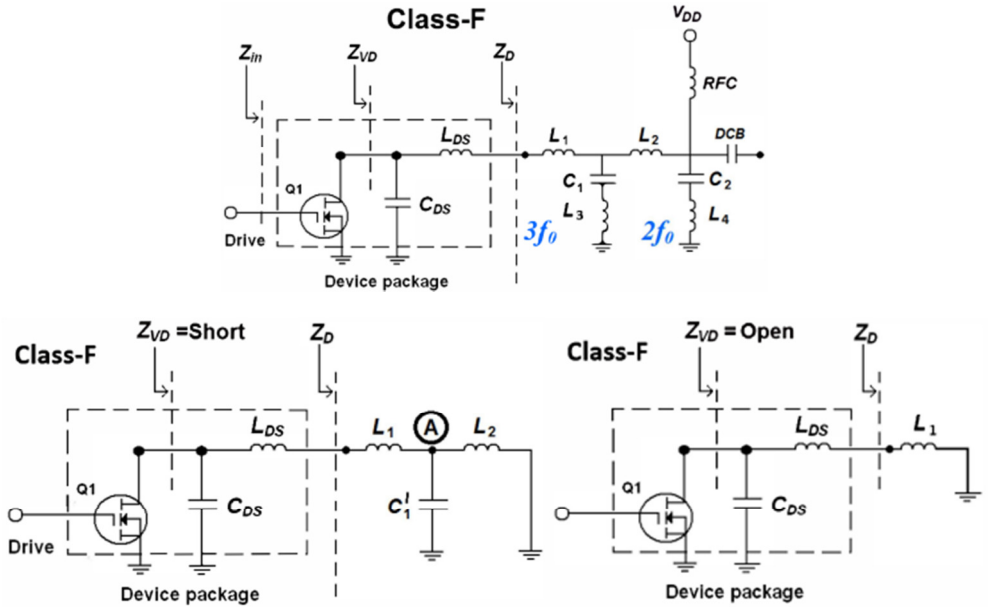


(b)

Figure 3.1 Parallel L_1C_1 **(a)** and series L_2C_2 **(b)** resonator circuits

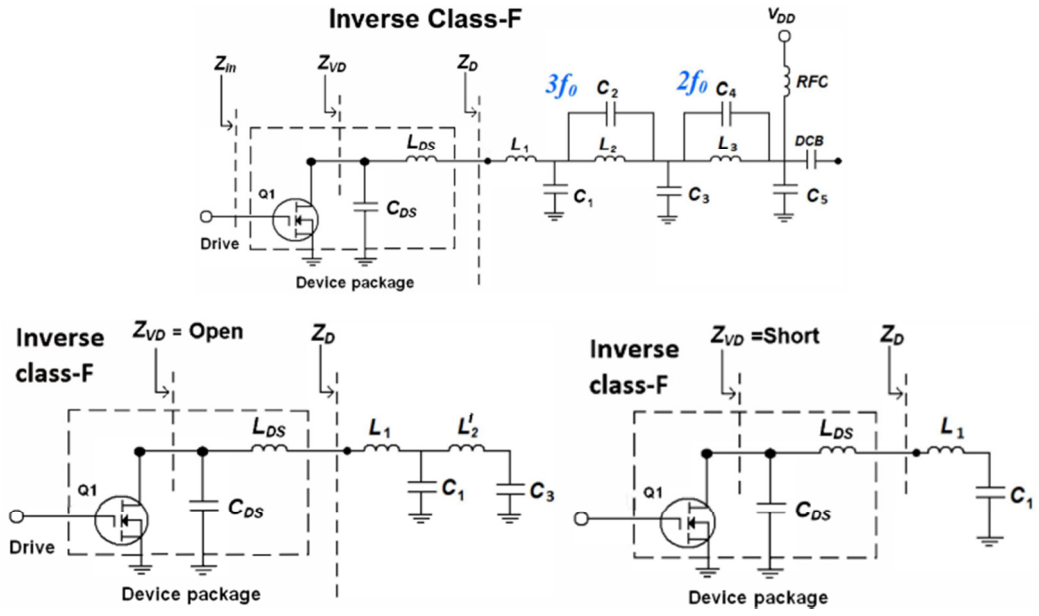
In Class-E PAs, L_1C_1 resonator tuned to the 2nd harmonic frequency is used at the load to provide open impedance at this harmonic frequency [39], [41]. A two-resonator harmonic matching network is also proposed for Class-E PAs employing active devices with large output capacitance [43].

Class-F and Inverse Class-F PAs require multi-harmonic reflective (open or short) terminations. In most of the practical applications, the 2nd and the 3rd harmonics are controlled only [45]. Then, Class-F PA requires short-circuit termination at $2f_o$ and open-circuit termination at $3f_o$. Inverse Class-F PA, on the other hand, requires open-circuit termination at $2f_o$ and short-circuit termination at $3f_o$. Two separate lumped-element matching circuits to satisfy $2f_o$ and $3f_o$ termination requirements of Class-F and Inverse Class-F PAs are proposed in [45] as demonstrated in Figure 3.2 and Figure 3.3.



(a) **(b)**

Figure 3.2 Class-F $2f_o$ / $3f_o$ matching circuit, **(a)** $2f_o$ equivalent, **(b)** $3f_o$ equivalent [45]



(a) **(b)**

Figure 3.3 Inverse Class-F $2f_o$ / $3f_o$ matching circuit, **(a)** $2f_o$ equivalent, **(b)** $3f_o$ equivalent [45]

3.3 Distributed-Element Harmonic Matching Circuits

Distributed-element circuits are the most widely preferred type of harmonic matching networks especially for high frequency PAs [46-60]. Figure 3.4 shows the two simple resonant transmission line structures for creating short and open terminations. The circuits resonate at the frequency when transmission line lengths are equal to quarter wavelength. Then, by using a combined form of the resonant transmission line circuits tuned at specific harmonics, a multi-harmonic matching circuit can be obtained.

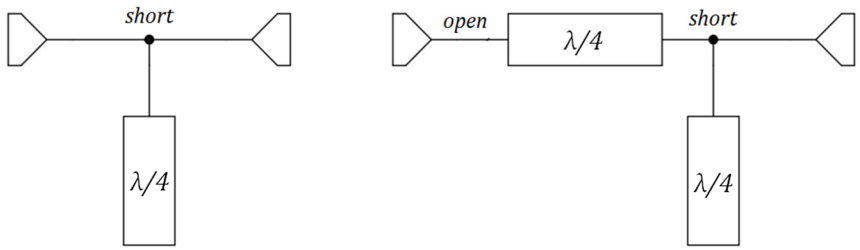


Figure 3.4 Resonant transmission line circuits

Multi-harmonic matching circuits are generally comprised of series transmission line sections together with open-ended and short-ended stubs [50]. Most of the time, the 2nd and the 3rd harmonic terminations are only considered for multi-harmonic matching networks. Moreover, optimum fundamental load matching should also be carried out together with the 2nd and the 3rd harmonic load matching for maximum output power. Then, a topology similar to the one shown in Figure 3.5 can be preferred [54].

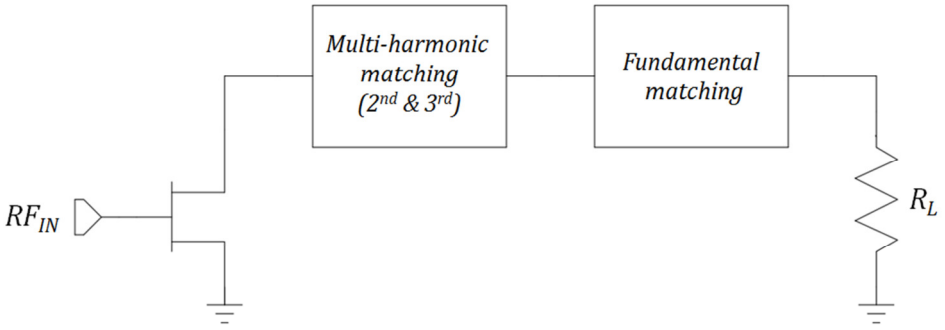


Figure 3.5 Simultaneous fundamental and multi-harmonic matching

Figure 3.6 shows the two examples of transmission line multi-harmonic load matching circuits that can be used for Class-F PAs. C_1 capacitor is used to create a short-circuit termination for λ/4 transmission line. C_2 capacitor is a DC-block capacitor passing fundamental and harmonic frequencies with no RF loss ideally. Since λ/4 transmission line at fundamental frequency becomes a λ/2 transmission line at the 2nd harmonic frequency, both circuits demonstrated in Figure 3.6, present a short-circuit to the left-hand side. Similarly, a λ/12 and λ/4 transmission lines at fundamental frequency serve as λ/4 transmission lines at the 3rd harmonic frequency. In addition, λ/6 transmission line becomes a λ/2 transmission line. Then, open-circuit termination to the left-hand side is satisfied at the 3rd harmonic frequency for both circuits. Since Z_1 and Z_2 characteristic impedances have no effect on harmonic terminations, their values can be tuned for fundamental frequency matching.

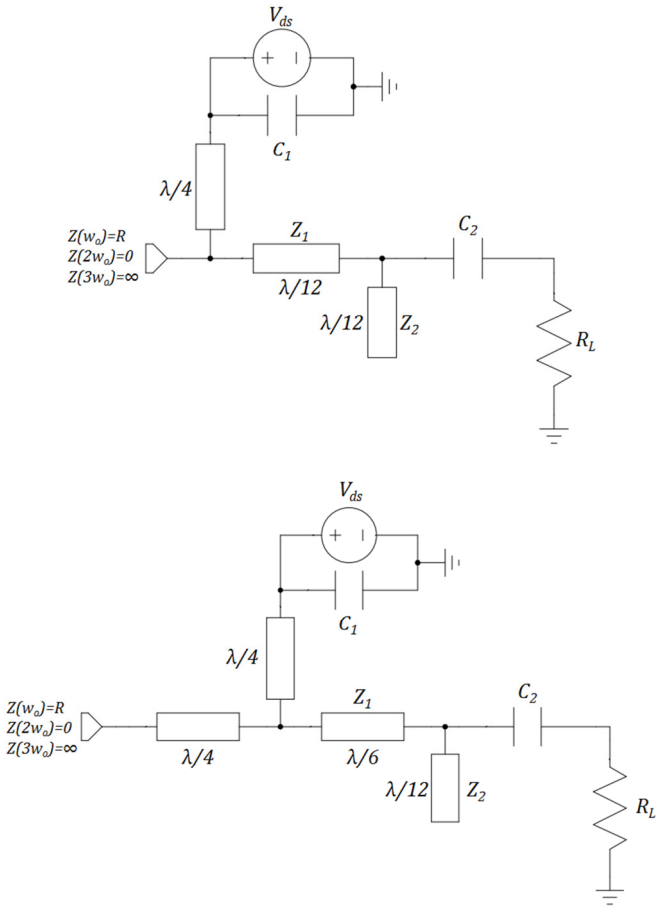


Figure 3.6 Class-F transmission line multi-harmonic load matching networks [12]

Similar multi-harmonic matching circuits can also be created for Inverse Class-F PAs as demonstrated in Figure 3.7. This time, both circuits satisfy open-circuit and short-circuit terminations at the 2nd and the 3rd harmonic frequencies respectively.

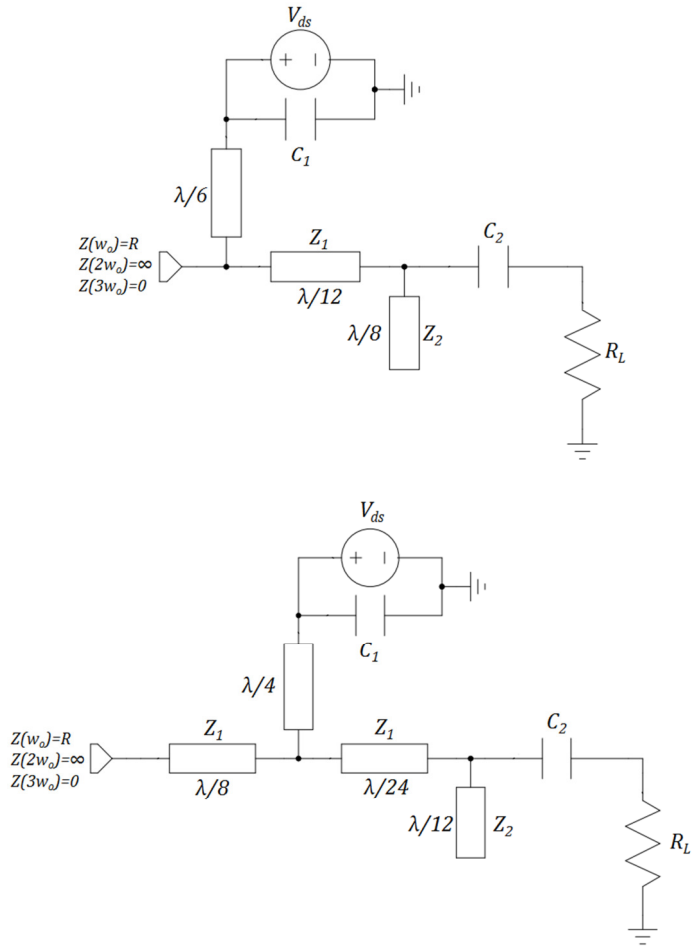


Figure 3.7 Inverse Class-F transmission line multi-harmonic load matching networks [12]

Giannini et al. analyzed the double-stub circuit given in Figure 3.8 by considering only the fundamental, the 2nd and the 3rd harmonic frequencies [50]. Closed form expressions are obtained for different terminations of the two stubs and some feasibility maps are presented [49]. During the synthesis of the circuit, the 2nd and the 3rd harmonic loads are taken as purely reactive lying on the outer border of smith chart. Then, it is shown that, a large number of possible cases for simultaneous

fundamental and purely reactive 2nd and 3rd harmonic matching can be solved with the proposed circuit in Figure 3.8.

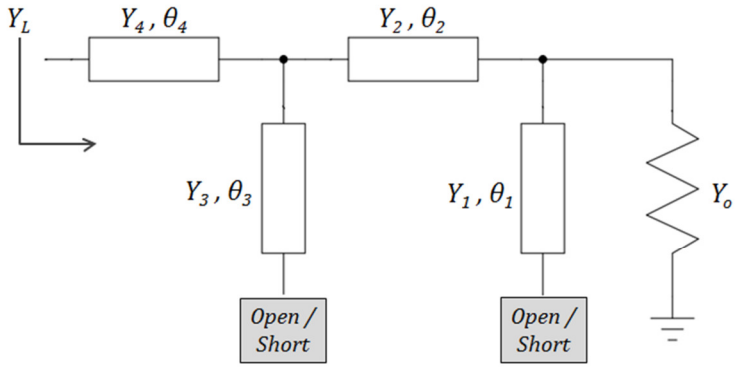


Figure 3.8 Harmonic matching network analyzed in [50]

A triple probe automatic slide screw load pull tuner is patented for simultaneous fundamental and harmonic load pull measurements with only the 2nd and the 3rd harmonics are included [58].

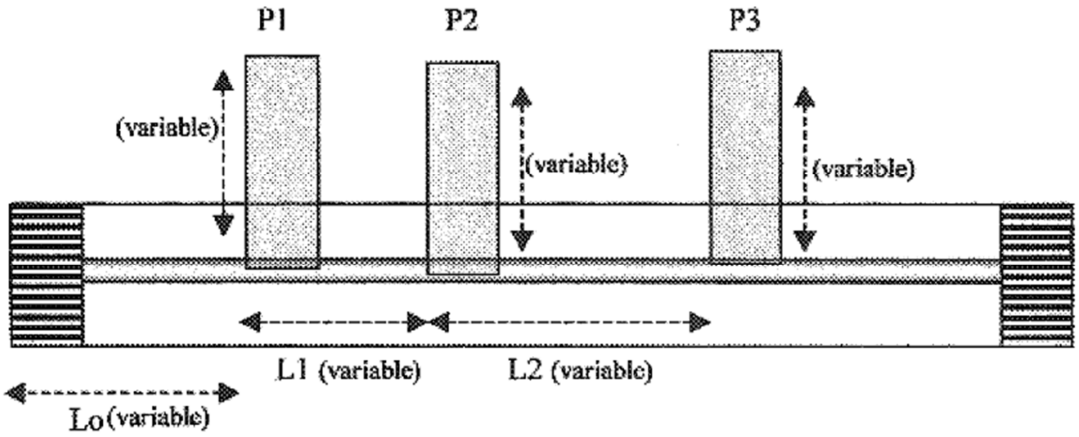


Figure 3.9 Triple probe automatic slide screw load pull tuner [58]

Tsironis owns another patent for a four-probe automatic load pull tuner capable of tuning four harmonic frequencies [59]. The automatic tuner system is

calibrated at f_o, $2f_o$, $3f_o$ and $4f_o$ frequencies with nearly 500 million calibration points containing the load combinations of four frequencies.

3.4 Summary and Conclusions

This chapter presents an overview of the various multi-harmonic matching circuits of high efficiency power amplifiers reported in the literature. First, lumped-element type matching circuits usually preferred at low frequency designs are discussed. Then, various examples of distributed-element type multi-harmonic matching circuits are examined. Some idealized circuits satisfying the harmonic terminations required for Class-F and Inverse Class-F PAs are presented and analyzed.

CHAPTER 4

MULTI-HARMONIC ANALYSIS OF TRIPLE STUB MATCHING CIRCUIT

4.1 Introduction

Triple stub matching circuit is well known for its impedance matching capability by tuning the lengths of the three stubs [61], [62]. This capability, which is applicable at a single frequency, is readily proven by graphical analysis on the Smith Chart [61]. Moreover, Unlu et al. showed the ability of triple stub circuit in controlling the phase and the amplitude as well as impedance matching [63], [64].

In this chapter, the triple stub topology is investigated in terms of the 2^{nd} and the 3^{rd} harmonic load matching capability in addition to its already known fundamental load matching capability. Since the analysis is performed at three frequencies, there are three load impedances to be matched simultaneously. Then, by considering the real and the imaginary parts of the load impedances separately, six different equations should be solved together, meaning that at least six independent variables of transmission lines are required for a unique solution.

The analysis starts with a classical triple stub topology with open-ended stubs of variable lengths and fixed-length interconnecting transmission lines. The cascaded ABCD parameters of the stubs and the series transmission lines are calculated for the analysis. Then, analytical expressions for the fundamental and harmonic impedances are obtained.

Because of the requirement of at least six variables for multi-harmonic analysis, two different modifications to the classical triple stub circuit are analyzed specifically. One modification is adding an extra series transmission line and using three stub lengths and three series transmission line lengths as variables. This modified topology is investigated for the simultaneous fundamental and harmonic matching covering all possible impedances without any restriction. Another

modification is adding three more stubs with variable lengths to the opposite side of the existing stubs. This second modified topology is also analyzed for the simultaneous fundamental and harmonic matching with the harmonic impedances restricted to be purely reactive which is specifically applicable to high efficiency power amplifiers.

4.2 Classical Triple Stub Matching Circuit

The conventional triple stub matching circuit with open circuit terminated stubs is given in Figure 4.1. Since open ended stubs are easy to implement in printed structures, this configuration is selected for the analysis. The interconnecting transmission line lengths are also fixed at $\lambda_o/8$ to obtain simplified expressions at the fundamental and harmonic frequencies. This structure is already known to be capable of providing impedance transformation from the system impedance, Z_o, to any impedance, Z_{in}, by tuning the stub lengths, l_1, l_2 and l_3. However, this readily known impedance matching process is applicable at a single frequency; since, the electrical lengths of the stubs and the interconnecting transmission lines vary with the frequency.

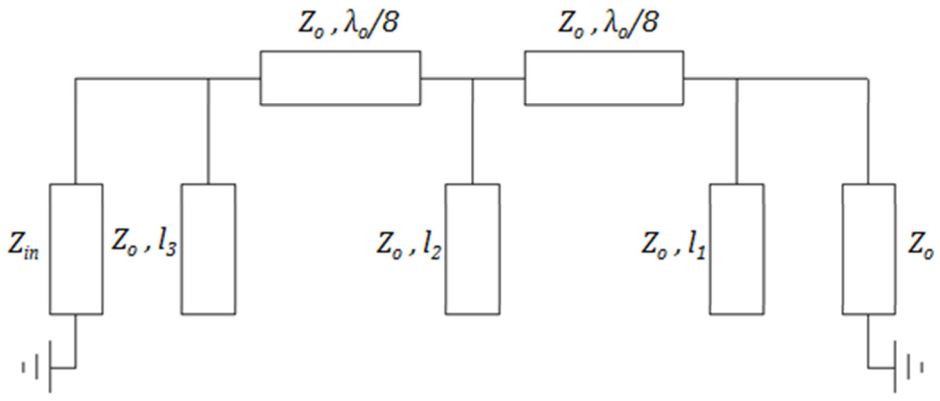


Figure 4.1 Conventional triple stub matching circuit with open-ended stubs

The circuit given in Figure 4.1 is analyzed at the 2nd and the 3rd harmonic frequencies in addition to the fundamental frequency for the first time. For this purpose, it is beneficial to use ABCD parameters.

ABCD parameters of a transmission line with impedance, Z, and physical length, l, can be written as;

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} cos\beta l & jZsin\beta l \\ jYsin\beta l & cos\beta l \end{bmatrix} = \frac{1}{\sqrt{1+S^2}} \begin{bmatrix} 1 & jSZ \\ j\frac{S}{Z} & 1 \end{bmatrix} \quad (4\text{-}1)$$

$$S = tan\beta l \;\&\; Y = \frac{1}{Z}$$

Then, the ABCD matrix of a $\lambda_o/8$ long transmission line at the fundamental frequency, f_o, can be simplified as;

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & jZ \\ j\frac{1}{Z} & 1 \end{bmatrix} \quad (4\text{-}2)$$

Similarly, ABCD parameters of an open circuit terminated stub with impedance, Z, and physical length, l, can be written as;

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ jYtan\beta l & 1 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ j\frac{S}{Z} & 1 \end{bmatrix} \quad (4\text{-}3)$$

$$S = tan\beta l \;\&\; Y = \frac{1}{Z}$$

The overall ABCD parameters of triple stub matching circuit given in Figure 4.1 can be obtained by cascading the individual ABCD parameters of the transmission lines and the open-ended stubs as follows;

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \frac{1}{2} \begin{bmatrix} 1 & 0 \\ j\frac{z_o}{Z_o} & 1 \end{bmatrix} \begin{bmatrix} 1 & jZ_o \\ j\frac{1}{Z_o} & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ j\frac{y_o}{Z_o} & 1 \end{bmatrix} \begin{bmatrix} 1 & jZ_o \\ j\frac{1}{Z_o} & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ j\frac{x_o}{Z_o} & 1 \end{bmatrix} \quad (4\text{-}4)$$

$$x_o = tan\beta_o l_1 \,, y_o = tan\beta_o l_2 \,, z_o = tan\beta_o l_3$$

Then, Z_{in} at the fundamental frequency can be calculated as;

$$Z_{in}(f_o) = \frac{AZ_o + B}{CZ_o + D} = \frac{2x_o + y_o + x_o y_o + j(-2 - y_o)}{2z_o + y_o + y_o z_o + j(2x_o z_o + y_o z_o + x_o y_o + x_o y_o z_o + y_o - 2)} \quad (4\text{-}5)$$

At the 2nd harmonic frequency, $2f_o$, $\tan(\beta\lambda_o/8)$ term goes to infinity; so, $\lambda_o/8$ long transmission lines behave as $\lambda/4$ transformers. Then, Z_{in} expression can be simplified as;

$$Z_{in}(2f_o) = \frac{1 - x_1 y_1 + j y_1}{1 - y_1 z_1 + j(x_1 + z_1 - x_1 y_1 z_1)} \quad (4\text{-}6)$$
$$x_1 = \tan(2\beta_o l_1)\,, y_1 = tan(2\beta_o l_2)\,, z_1 = \tan(2\beta_o l_3)$$

The variables x_1, y_1 and z_1 can be written in terms of x_o, y_o and z_o as follows;

$$x_1 = \frac{2x_o}{\sqrt{1 - {x_o}^2}}\,, y_1 = \frac{2y_o}{\sqrt{1 - {y_o}^2}}\,, z_1 = \frac{2z_o}{\sqrt{1 - {z_o}^2}} \quad (4\text{-}7)$$

At the 3rd harmonic frequency, $3f_o$, $\tan(\beta\lambda_o/8)$ term becomes -1 and Z_{in} expression can be written as;

$$Z_{in}(3f_o) = \frac{-2x_2 - y_2 + x_2 y_2 + j(2 - y_2)}{-2z_2 - y_2 + y_2 z_2 + j(-2x_2 z_2 - y_2 z_2 - x_2 y_2 + x_2 y_2 z_2 + y_2 + 2)} \quad (4\text{-}8)$$
$$x_2 = \tan(3\beta_o l_1)\,, y_2 = tan(3\beta_o l_2)\,, z_2 = \tan(3\beta_o l_3)$$

The variables x_2, y_2 and z_2 can be written in terms of x_o, y_o and z_o as follows;

$$x_2 = \frac{3x_o - {x_o}^3}{1 - 3{x_o}^2}\,, y_2 = \frac{3y_o - {y_o}^3}{1 - 3{y_o}^2}\,, z_2 = \frac{3z_o - {z_o}^3}{1 - 3{z_o}^2} \quad (4\text{-}9)$$

For a given set of $\{Z_{in}(f_o),\ Z_{in}(2f_o),\ Z_{in}(3f_o)\}$, 6 equations can be obtained in terms of x_o, y_o and z_o by separating the real and imaginary parts of Z_{in} expressions. With 3 unknowns and 6 equations, it is not possible to find a solution for all possible $\{Z_{in}(f_o),\ Z_{in}(2f_o),\ Z_{in}(3f_o)\}$ sets. Hence, the number of unknowns should be increased to at least 6. For this purpose, two different modifications to the

conventional triple stub topology given in Figure 4.1 are investigated in terms of harmonic matching.

4.3 Modifications to the Conventional Triple Stub Circuit

4.3.1 Modified Circuit-1

In the circuit given in Figure 4.2, 3 extra stubs with lengths l_4, l_5 and l_6 are inserted at the other side of the series transmission lines as given in Figure 4.1. Then, triple stub pairs are obtained and the 6 stub lengths, $l_1, l_2, l_3, l_4, l_5, l_6$, are assigned as the variables for the 6 equations.

Following the same analysis steps in Section 4.2, Z_{in} expressions at the fundamental, the 2nd and the 3rd harmonics can be obtained as given in (4-10), (4-11) and (4-12) respectively.

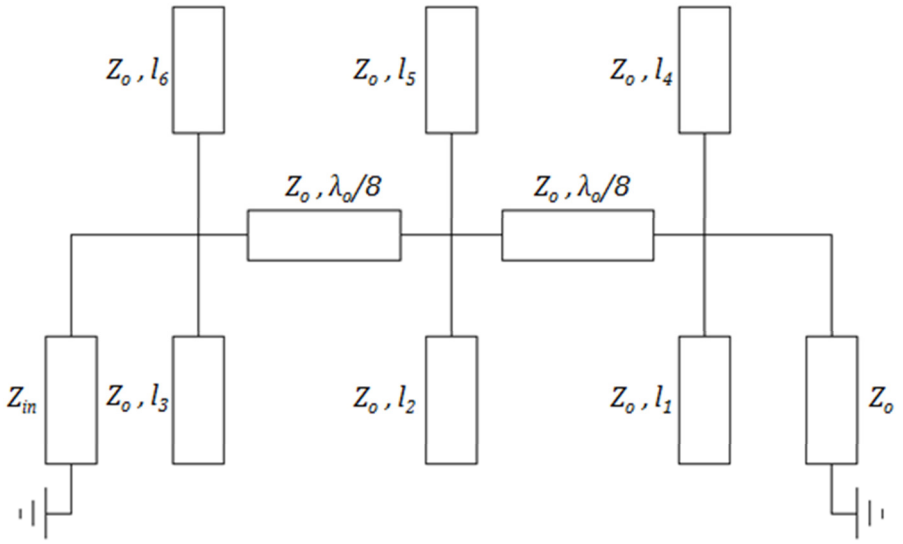


Figure 4.2 Modified circuit-1

$$Z_{in}(f_o) = \frac{2x_o' + y_o' + x_o'y_o' + j(-2 - y_o')}{2z_o' + y_o' + y_o'z_o' + j(2x_o'z_o' + y_o'z_o' + x_o'y_o' + x_o'y_o'z_o' + y_o' - 2)} \quad (4\text{-}10)$$

$$x_o' = tan\beta_o l_1 + tan\beta_o l_4 \, , y_o' = tan\beta_o l_2 + tan\beta_o l_5 \, , z_o' = tan\beta_o l_3 + tan\beta_o l_6$$

$$Z_{in}(2f_o) = \frac{1 - x_1'y_1' + jy_1'}{1 - y_1'z_1' + j(x_1' + z_1' - x_1'y_1'z_1')}$$
$$x_1' = \tan(2\beta_o l_1) + \tan(2\beta_o l_4)\,, y_1' = tan(2\beta_o l_2) + \tan(2\beta_o l_5)\,, \quad (4\text{-}11)$$
$$z_1' = \tan(2\beta_o l_3) + \tan(2\beta_o l_6)$$

$$Z_{in}(3f_o)$$
$$= \frac{-2x_2' - y_2' + x_2'y_2' + j(2 - y_2')}{-2z_2' - y_2' + y_2'z_2' + j(-2x_2'z_2' - y_2'z_2' - x_2'y_2' + x_2'y_2'z_2' + y_2' + 2)} \quad (4\text{-}12)$$
$$x_2' = \tan(3\beta_o l_1) + \tan(3\beta_o l_4)\,, y_2' = tan(3\beta_o l_2) + \tan(3\beta_o l_5)\,,$$
$$z_2' = \tan(3\beta_o l_3) + \tan(3\beta_o l_6)$$

4.3.2 Modified Circuit-2

The circuit given in Figure 4.3 is another modification to the circuit given in Figure 4.1 with 3 transmission line lengths, l_2, l_4, l_6, and 3 stub lengths, l_1, l_3, l_5, are assigned as the variables. Different from the conventional triple stub structure, the transmission line lengths, l_2, l_4, are not fixed at $\lambda_o/8$. Moreover, an additional transmission line with length l_6 is inserted to the Z_{in} side.

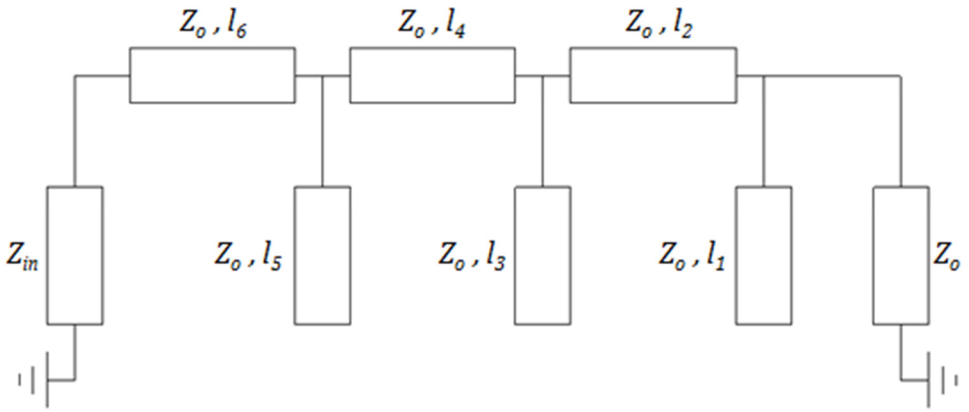


Figure 4.3 Modified circuit-2

The analytical expressions can be obtained from the result of multiplication of individual ABCD matrices as below;

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}$$
$$= K \begin{bmatrix} 1 & jS_6Z_o \\ j\frac{S_6}{Z_o} & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ j\frac{S_5}{Z_o} & 1 \end{bmatrix} \begin{bmatrix} 1 & jS_4Z_o \\ j\frac{S_4}{Z_o} & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ j\frac{S_3}{Z_o} & 1 \end{bmatrix} \begin{bmatrix} 1 & jS_2Z_o \\ j\frac{S_2}{Z_o} & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ j\frac{S_1}{Z_o} & 1 \end{bmatrix}$$
$$S_i = tan\beta_o l_i \, , i = 1,2, \dots ,6 \tag{4-13}$$
$$K = \frac{1}{\sqrt{1+{S_6}^2}\sqrt{1+{S_4}^2}\sqrt{1+{S_2}^2}}$$

4.4 Analysis of the Modified Circuits

The analytical expressions of the two modified circuits are analyzed in detail for multi-harmonic matching together with the fundamental matching. Since the expressions are complex nonlinear expressions, a numerical optimization procedure is followed for the analysis. First, predefined impedance goals to be matched are formed for the fundamental frequency and the two harmonic frequencies. Then, the six transmission line lengths assigned as the variables are optimized for each circuit to determine whether it is possible to satisfy a matching condition for the whole objective impedance set or not. Optimization Toolbox™ of MATLAB® is used as a tool for this analysis.

The objective impedances to be matched at the fundamental frequency are chosen as the 27 impedance points uniformly distributed inside the smith chart as given in Figure 4.4. The aimed impedances at the 2nd and the 3rd harmonic frequencies are selected differently for the two circuits. For circuit-1, the objective harmonic impedances are 12 purely reactive impedances uniformly distributed on the outer border of the smith chart as shown in Figure 4.5. Hence there are 3888 (27x12x12) impedance combinations in total to be analyzed for circuit-1. Whereas for circuit-2, the harmonic impedances to be matched are not restricted to be reactive only; instead, 15 more impedances uniformly distributed inside the smith chart are selected in addition to the 12 reactive impedances as shown in Figure 4.6. Then, there are 19683 (27x27x27) impedance combinations in total to be analyzed for circuit-2.

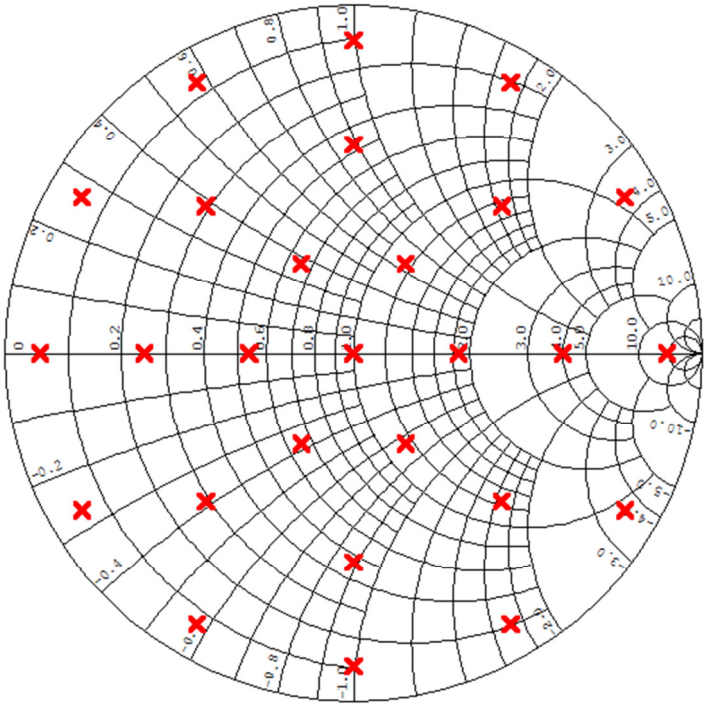


Figure 4.4 Objective impedances at the fundamental frequency (circuit-1 & circuit-2)

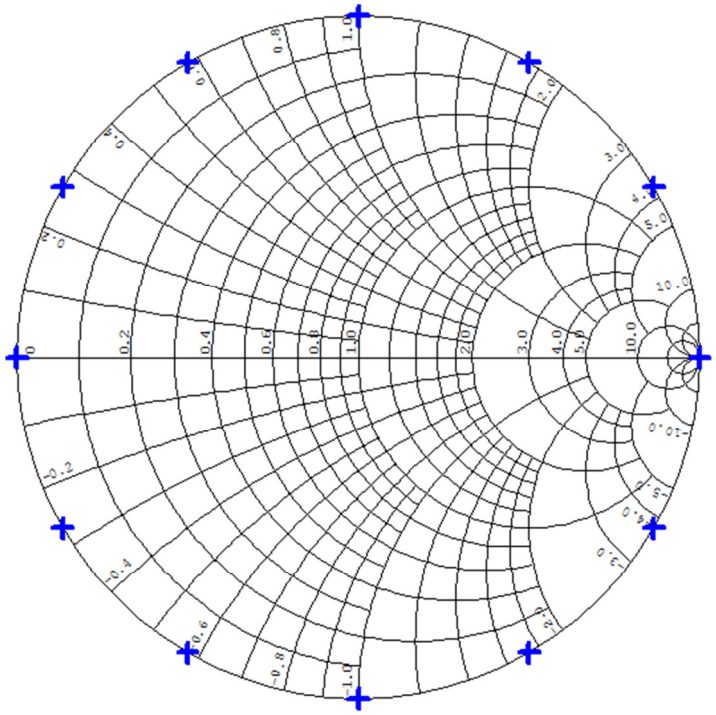


Figure 4.5 Objective impedances at the 2nd and the 3rd harmonic frequencies (circuit-1)

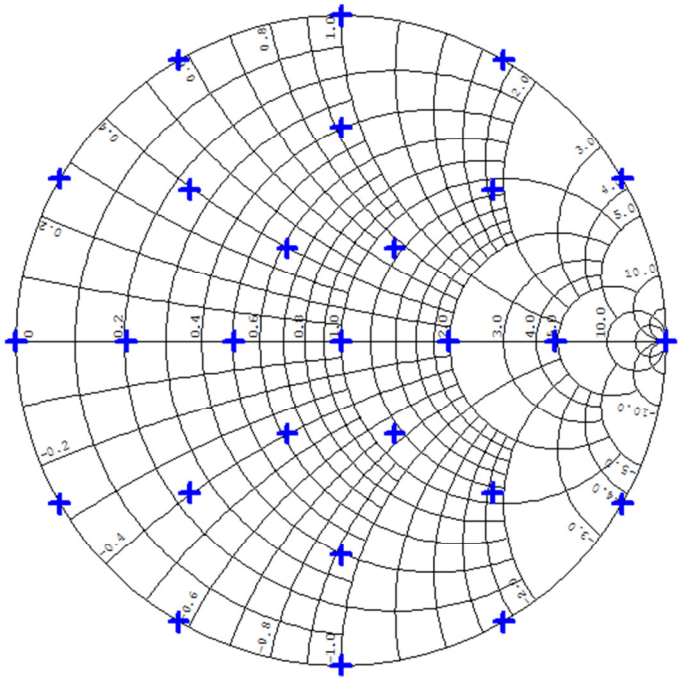


Figure 4.6 Objective impedances at the 2nd and the 3rd harmonic frequencies (circuit-2)

The analysis starts with creating a function named as *error_function* which accepts 6 transmission line lengths, 3 objective impedance magnitudes and 3 objective impedance phases extracted from the objective impedances, assigned at the fundamental and the two harmonics, as inputs. The function outputs a single absolute error,E_{abs}, from $Z_{in}(f_o)$, $Z_{in}(2f_o)$, $Z_{in}(3f_o)$ calculated from the 6 transmission line lengths using the analytical expressions obtained previously and $\Gamma_{obj}(f_o), \Gamma_{obj}(2f_o), \Gamma_{obj}(3f_o)$ obtained from the the selected objective impedances. The flow of the *error_function* is explained in Figure 4.7.

The next step is to operate *error_function* for all possible impedance combinations and try to find a solution to the 6 transmission line lengths for all of these combinations. This procedure is also explained as a flow chart in Figure 4.8. First, a fundamental and two harmonic objective impedance combination is selected. Then, an initial guess is made with the 6 transmission line lengths and the 6 transmission line lengths are optimized until the *error_function* output is lower than the goal of 0.0001. If the optimization does not converge, the initial guess is changed and the optimization process is repeated for a solution. This procedure is continued for all possible combinations of the objective impedances.

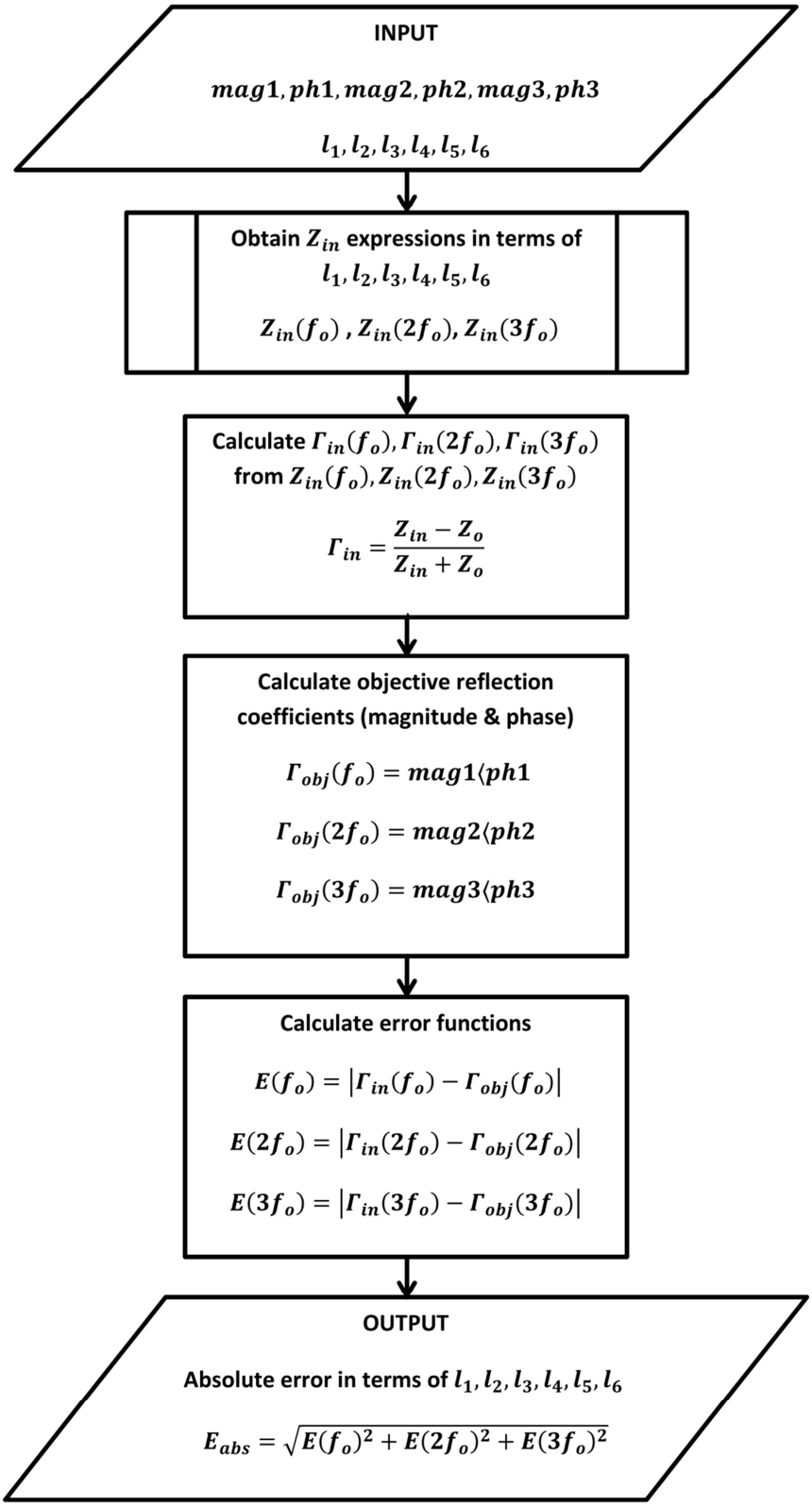


Figure 4.7 Flow of the *error_function*

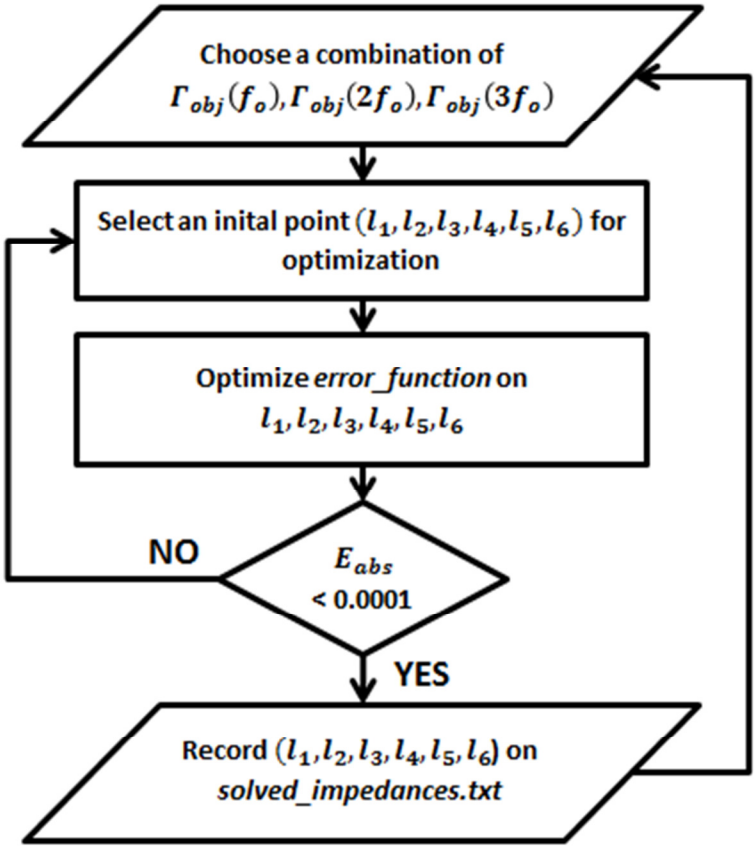


Figure 4.8 Optimization flow

The pattern search optimization algorithm is followed during optimization flow. Moreover, $(0, \lambda_o/2)$ bound is applied to the transmission line lengths during optimization.

4.5 Analysis Results

Circuit-1 and circuit-2 are analyzed in terms of fundamental and harmonic matching by following the previously explained procedure. It is clear that the objective impedances of circuit-1 are a subset of the objective impedances of circuit-2. The analysis of circuit-2 is also separated into four different cases where each case has fundamental objective impedances the same as in Figure 4.4; whereas, the 2nd and the 3rd harmonic objective impedances differ according to some specific power amplifier applications. These four cases are explained as the following.

4.5.1 Case-1 Results

This case has both the 2nd and the 3rd harmonic impedances purely reactive with 12 impedance points lying on |Γ|=1 at Smith Chart. The analysis of both circuit-1 and circuit-2 are performed for this case. Purely reactive harmonic load impedances, available in this case, are required for harmonic-tuned power amplifiers to satisfy optimum load waveform shaping as discussed in Chapter-2.

The results of the optimization carried out for both circuits show that circuit-1 and circuit-2 are able to satisfy matching to 3888 (27x12x12) possible impedance combinations available for this case. Figure 4.9 shows the 3888 solutions of circuit-2 marked together inside the three smith charts representing the fundamental, the 2nd and the 3rd harmonics respectively. The confinement of the overlapped solutions proves the validity of the optimization process. For example, as seen in the sample zoomed impedance point in Figure 4.9, 144 (12 x12) solutions are available at each blue dot for the fundamental frequency. Likewise, 324 (12x27) solutions are available at each blue dot for the 2nd and the 3rd harmonic frequencies.

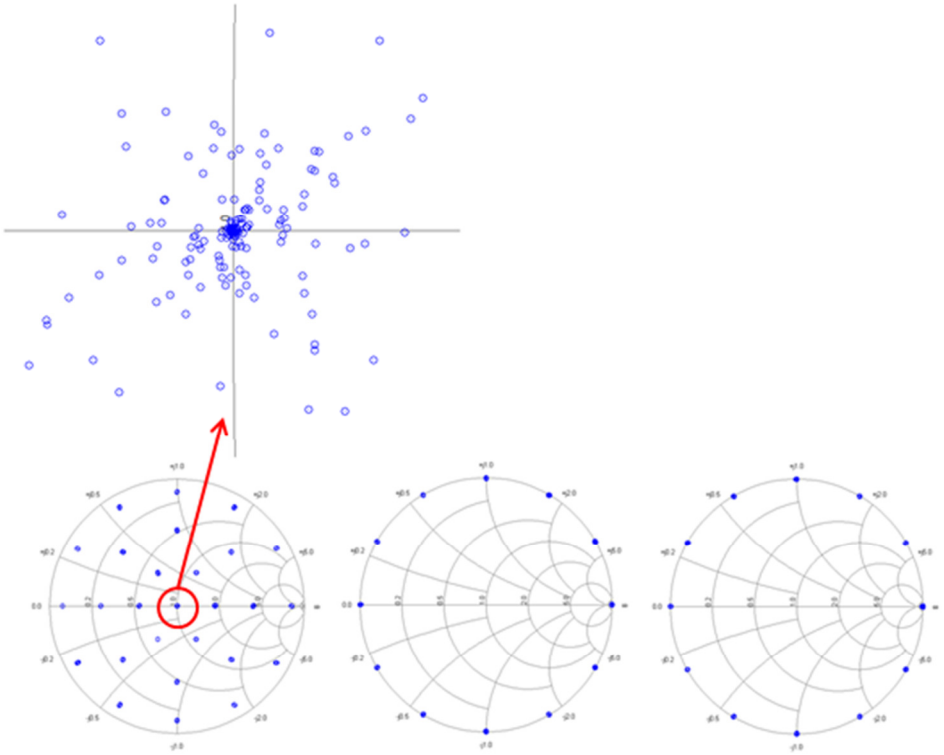


Figure 4.9 Optimization results for case-1

4.5.2 Case-2 Results

This case has both the 2nd and the 3rd harmonic impedances to be non-reactive with each spanning 15 impedance points uniformly distributed inside the smith chart. In terms of power amplifier application, this case may be applicable to a triple band power amplifier where the operating bands fall into the harmonics of the lower band. Then, the power amplifier wants to see non-reactive loads not only at the fundamental frequency but also at the 2nd and the 3rd harmonic frequencies.

The optimization results show that circuit-2 is able to provide impedance matching to all possible combinations available in this case also. There are 6075 (27x15x15) combinations in total and Figure 4.10 presents the solutions of all these combinations in three smith charts.

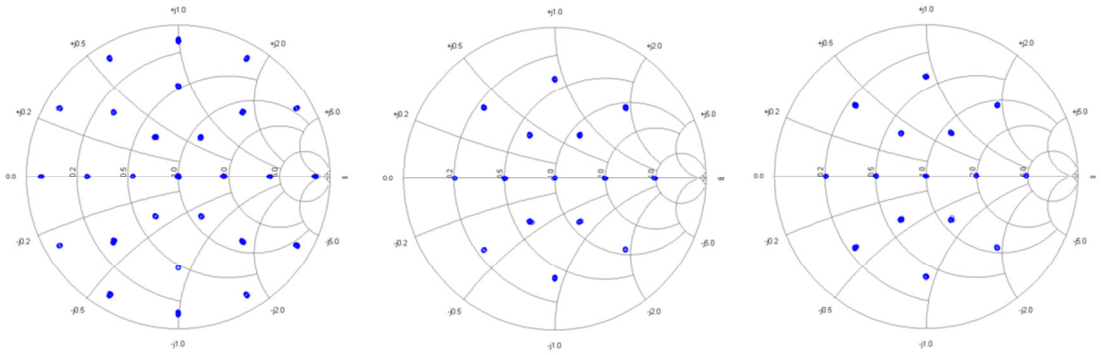


Figure 4.10 Optimization results for case-2

4.5.3 Case-3 Results

In this case, the 2nd harmonic impedances are purely reactive and the 3rd harmonic impedances are complex. For a dual-band power amplifier application where the upper band falls into the 3rd harmonic of the lower band, this impedance configuration may be needed not only to satisfy optimum load match at the operating bands but also to present reactive impedance to the 2nd harmonic of the lower band for better efficiency.

The optimization results show that circuit-2 is able to provide impedance match to all possible combinations available in this case. There are 4860 (27x12x15) combinations in total and Figure 4.11 presents the solutions of all these combinations in three smith charts.

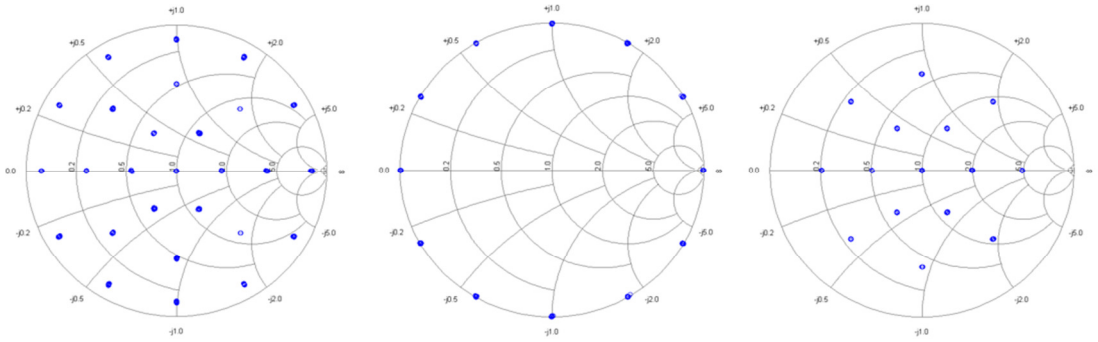


Figure 4.11 Optimization results for case-3

4.5.4 Case-4 Results

In this case, the 2nd harmonic impedances are complex and the 3rd harmonic impedances are purely reactive. For a dual-band power amplifier application where the upper band falls into the 2nd harmonic of the lower band, this impedance configuration may be used not only to satisfy optimum load match at the operating bands but also to present reactive impedance to the 3rd harmonic of the lower band for better efficiency.

It can be concluded from the optimization results that circuit-2 is able to provide impedance match to all possible combinations available in this case. There are 4860 (27x12x15) combinations in total and Figure 4.12 presents the solutions of all these combinations in three smith charts.

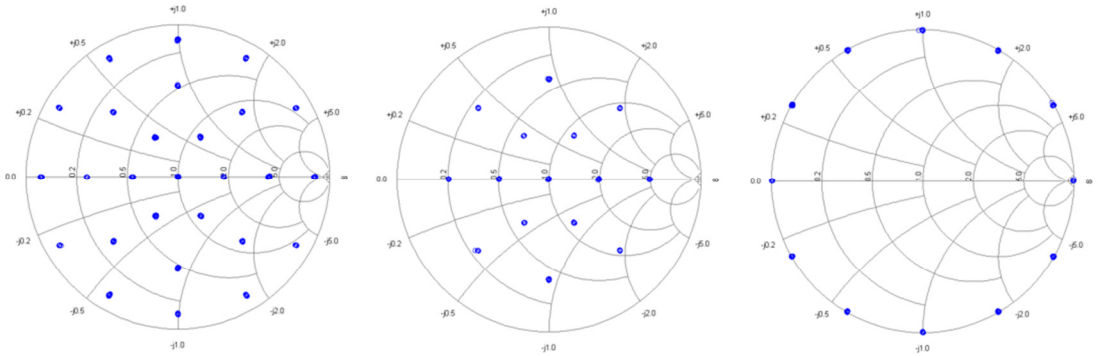


Figure 4.12 Optimization results for case-4.

The results obtained for four different cases show that the triple stub topology of circuit-2 is able to satisfy impedance matching to any impedance not only at the

fundamental frequency but also at the 2nd and the 3rd harmonic frequencies simultaneously. Moreover, the structure of circuit-1 is able to satisfy matching to any fundamental impedance and purely reactive harmonic impedances at the same time by only changing the stub lengths. This is very beneficial for a power amplifier load pull system; since, both fundamental and harmonic load pull can be performed in the same structure with only tuning the stub lengths which is an easier process compared to the series transmission line tuning.

4.6 Summary and Conclusions

This chapter presents an extended analysis of triple stub matching circuit by investigating this topology in terms of multi-harmonic matching in addition to fundamental matching. Multi-harmonic analysis is restricted to the 2nd and the 3rd harmonics for simplicity and practicability. Since, a complete analysis requires at least six variables of transmission line lengths, two modified versions of the conventional triple stub circuit are handled. First, the analytical expressions for the transformed impedances at fundamental and harmonic frequencies are obtained for both circuits. Then, these expressions are tried to be matched with some predefined fundamental and harmonic impedances simultaneously by optimizing the variables of transmission line lengths.

The first version is created as a six-stub topology with three stub pairs. In this version the stub lengths are assigned as variables and the lengths of the series transmission lines are fixed at $\lambda_o/8$, similar to the conventional triple stub topology. This modified topology is investigated specifically for a power amplifier application, so that, the harmonic impedances to be matched are restricted as being purely reactive. The results of the analysis demonstrate that the topology with three stub pairs is able to satisfy the purely reactive 2nd and 3rd harmonic impedance matching together with the fundamental matching of any impedance simultaneously. Moreover, this type of multi-harmonic matching is satisfied simply by tuning the length of the stubs. These properties make this topology an ideal candidate for a power amplifier load pull system.

The second version of the modified circuit is generated by adding an extra series transmission line to the traditional triple stub circuit. Then, three stub lengths and three series transmission line lengths are optimized for multi-harmonic matching analysis. Unlike to the first version, no restriction is placed not only to the fundamental impedances but also to the harmonic impedances. The analysis results show that this second topology can be used as a complete multi-harmonic matching circuit including the fundamental and the first two harmonic frequencies. Any impedance combination of three frequencies can be matched with this topology.

CHAPTER 5

HIGH EFFICIENCY TUNABLE DUAL BAND POWER AMPLIFIER DESIGN

5.1 Introduction

In the previous chapter, it is shown that triple stub topology can perform impedance matching at the fundamental frequency and the first two harmonic frequencies simultaneously. A typical application where simultaneous matching of the fundamental and the harmonic impedances is required is high efficiency power amplifiers as discussed in Chapter 2. In this chapter, the multi-harmonic matching property of the triple stub topology is applied to a dual band high efficiency power amplifier design.

Power amplifiers require purely reactive load impedances at harmonic frequencies for increased efficiency. Most of the time, it is feasible and practical to consider only the 2^{nd} and the 3^{rd} harmonics. In multi-octave band or some multi-band power amplifier applications, the 2^{nd} or the 3^{rd} harmonics of an operating frequency may fall into another operating frequency. Then, it may not be possible to show the optimum harmonic impedances to the active device for all operating frequencies at the same time; because, fundamental load should not be reactive for optimum output power. Hence, the load should present non-reactive impedances inside the operating band and reactive impedances at the harmonics of the operating band to obtain the highest efficiency and the highest output power at the same time. This cannot be achieved with a fixed load matching circuit; instead, a tunable load matching circuit is required.

In this chapter, a dual band power amplifier design is presented. Before starting the design, the two operating frequencies of the dual band power amplifier are selected as 1 GHz and 2 GHz inside L-Band, which is a widely used frequency spectrum for both mobile communications and military applications. It is obvious

that the upper operating frequency (2 GHz) is exactly the same as the second harmonic of the lower operating frequency (1 GHz). The aim is to achieve more than 10W output power and maximum possible efficiency in both operating frequencies. In order to reach this goal, a tunable load matching circuit is designed. The previously analyzed triple stub structure forms the basis for the tunable matching circuit due to its proven multi-harmonic matching capability and tunability. Moreover, it is investigated how the tunable matching circuit can be made to automatically tune itself according to the operating frequency. A structure that can easily be integrated onto the input matching circuit of the power amplifier is proposed for this purpose.

The upcoming sections give a detailed discussion of the dual-band power amplifier design with the requirements mentioned above. A typical design flow of a power amplifier is given in Figure 5.1. As can be seen from Figure 5.1, there are three basic phases of a PA design as explained the following;

The first and initial phase is named as the analysis phase. Before starting a design, there are some specifications to be fulfilled such as output power, efficiency and frequency band. Then, a suitable active device should be selected according to the given specifications. After that, a proper PA topology should be chosen by determining the biasing point of the active device. The analysis phase concludes with the source and load pull analyses of the active device at the selected biasing point.

The second phase is called as the design phase. At this phase, the source and load matching networks are designed using the idealized models of the components such as transmission lines and lumped elements. Load matching network is required to provide impedance transformation from the system impedance (50 ohm) to the optimum fundamental and harmonic loads determined during load pull analysis. On the other hand, source matching network should be designed to maximize the gain by assuring the stability also.

The third and the final phase is the implementation phase. In this phase, the idealized matching circuits designed previously are realized in microstrip technology on a suitable dielectric. The complete PA structure is optimized to satisfy the

required parameters such as output power, efficiency and waveforms. Then, the designed PA is fabricated and measured. If the fabricated PA satisfies the requirements, the design flow is ended. Otherwise, the performance is tried to be improved by post-tuning. If the specifications cannot be met by post-tuning also, the implementation phase should be repeated again by reverse engineering.

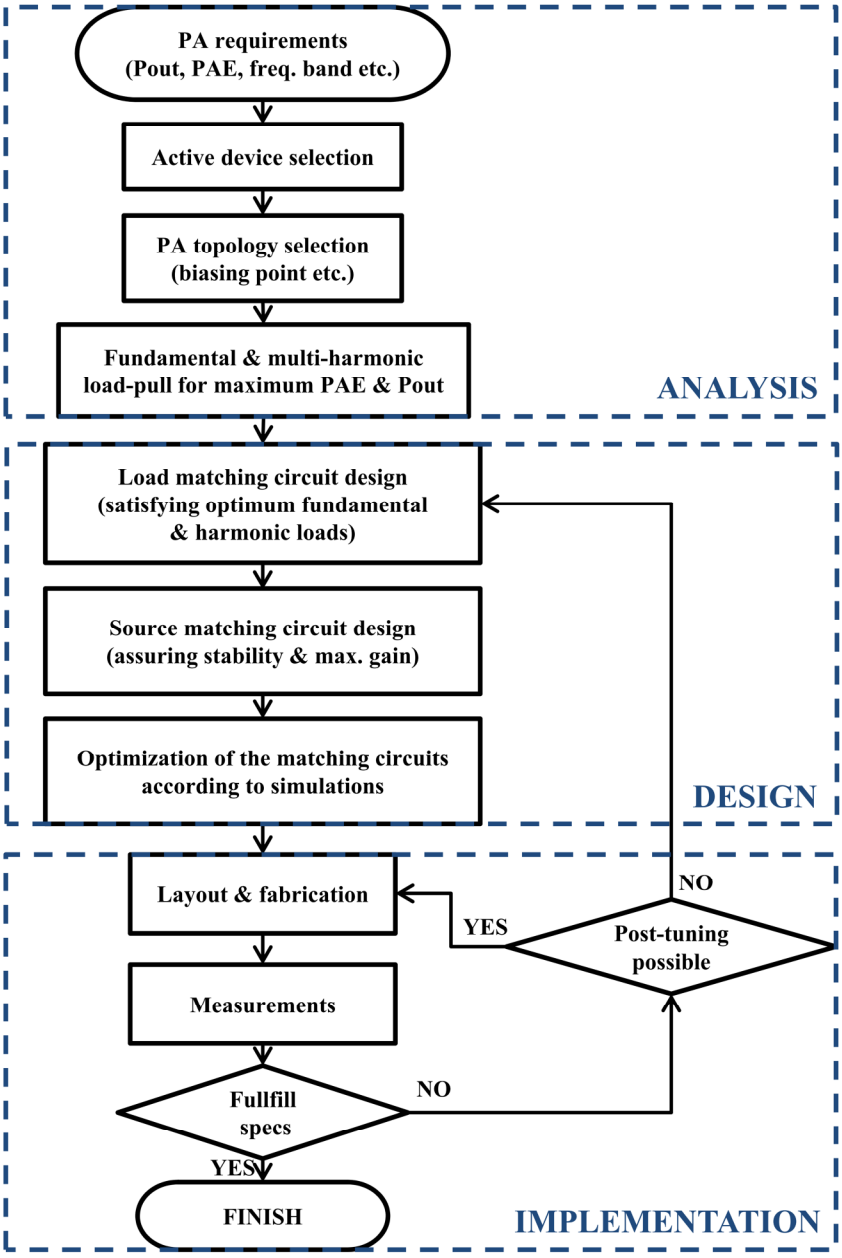


Figure 5.1 Power amplifier design flow

5.2 Analysis Phase

This phase includes all the works that should be carried out before going into the detailed power amplifier design. First, a suitable transistor should be selected to satisfy the design goals presented in Table 5-1. Then, the biasing point of the transistor is determined according to the selected PA topology. Finally, the optimum fundamental and harmonic load impedances of the selected transistor should be extracted from multi-harmonic load pull analysis. Multi-harmonic load pull analysis can be performed either by using the nonlinear model of the active device or by using an active load pull measurement system.

Table 5-1 Aimed design specifications of the dual band PA

Parameter	Design Goal
Operating Bands	1 GHz & 2 GHz
Output Power	>10 W
PAE	>70%

5.2.1 Transistor Selection

Before starting the design, a suitable active device is investigated. In order to achieve the design goals given in Table 5-1, a 15W GaN transistor from Wolfspeed Inc. with part number CGH60015D is chosen as the active device for the power amplifier [65]. Since the transistor is a GaN transistor, it supports 28V operation. Moreover, the transistor is in bare die form; therefore, the package parasitics are not dealt with during the design. The nonlinear model of the transistor provided by Wolfspeed Inc. is used in the RF simulations performed in Microwave Office® EDA software of National Instruments.

5.2.2 PA Topology and Biasing Point Selection

After CGH60015D GaN transistor is selected as the active device, the PA topology and the biasing point of the transistor are selected accordingly.

In Chapter 2, different high efficiency PA classes are discussed in detail. Class-F/F^{-1} and Continuous Class-F/F^{-1} PAs are seen as the widely preferred techniques at high frequencies. All these techniques perform waveform shaping by tuning the harmonics at the drain side of the transistor. Then, a harmonic-tuned PA topology is preferred in this work. Instead of obeying the specific harmonic terminations required for Class-F/F^{-1} or Continuous Class-F/F^{-1} techniques, a more general analysis is followed by selecting the optimum harmonic loads from the outcome of a multi-harmonic load pull analysis of the transistor. During the multi-harmonic load pull analysis, efficiency is chosen as a parameter to be maximized.

The biasing point of the transistor is chosen to be located in between Class-AB and Class-B biasing conditions. According to the datasheet of CGH60015D, the maximum drain current is obtained as 3.5A [65]. Then, V_{ds}=28V and I_{ds}=100mA biasing condition recommended in the datasheet also is an appropriate choice for the design.

5.2.3 Load Pull Analysis

Since a harmonic-tuned PA is designed, the required fundamental and harmonic load impedances should be extracted from the load pull simulations. The simulations are performed when the transistor is based at V_{ds}=28V and I_{ds}=100mA conditions. Two separate load pull simulations are executed at 1 GHz and 2 GHz. An iterative procedure explained in Figure 5.2 is followed during the load pull simulations. First, a load pull analysis is performed at the fundamental frequency to obtain the fundamental load resulting in the maximum output power. During this analysis, the 2nd harmonic load is maintained as short-circuit (Γ=-1) and the 3rd harmonic load is kept as open-circuit (Γ=1) which is the same with the harmonic terminations of a Class-F PA. After the optimum fundamental load is extracted, the 2nd and the 3rd harmonic load pull simulations are carried out consecutively. The goal of these harmonic load pull simulations is to maximize the efficiency. After finding the optimum harmonic loads, the fundamental load pull analysis is repeated

again since the initial Class-F harmonic loads have changed. The load pull analysis can be ended after this fundamental load pull or some iterations can be continued.

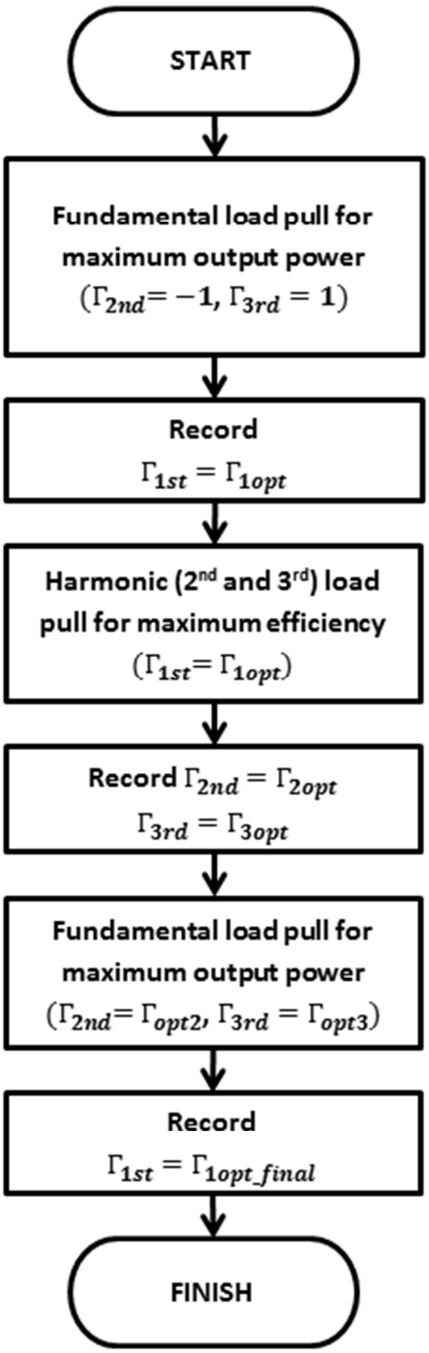


Figure 5.2 Fundamental and harmonic load pull steps

The typical outputs of load pull simulations are the contours representing the loads resulting in the same output power or efficiency. In Figure 5.3, the fundamental

load pull simulation results obtained at 1 GHz and 2 GHz are shown. Each contour in the smith chart shows the positions of the loads resulting in the same output power. As the output power decreases the contours expand meaning that the solution set includes larger number of loads. The innermost contour represents the loads producing the maximum output power. The fundamental load is tried to be located inside this innermost contour to be able to achieve the maximum available output power. The similar contours are also available as the output of harmonic load pull analysis.

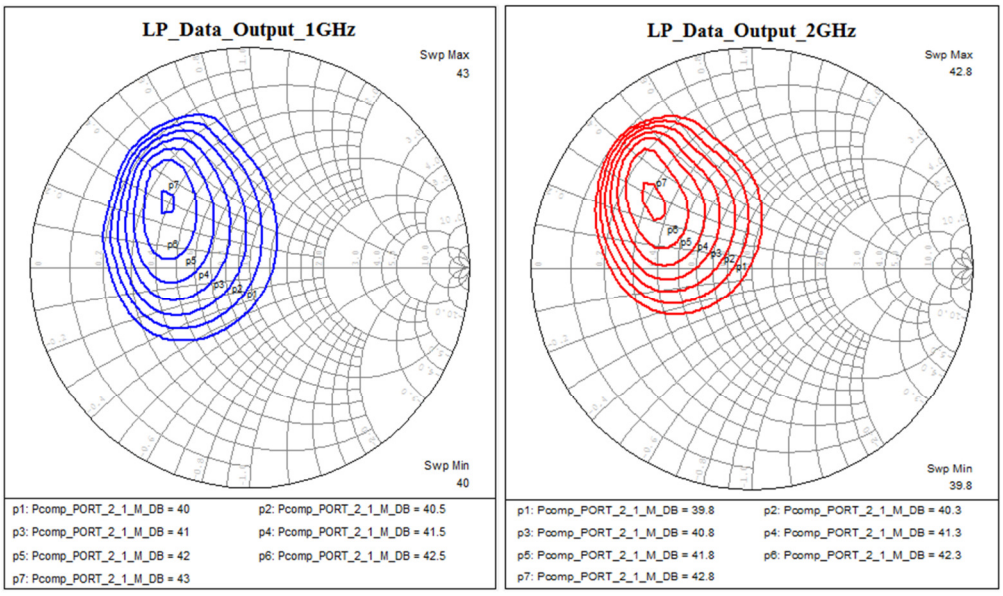


Figure 5.3 Fundamental load pull contours at 1 GHz and 2 GHz

The load pull simulations produce the optimum fundamental and harmonic impedances at 1 GHz and 2 GHz, as shown in Figure 5.4. The first conclusion from these results is that the harmonic load impedances are purely reactive residing in the outer circle of the Smith Chart as expected. Another point is that two different loads are required at 2 GHz for two different operating frequencies as anticipated before.

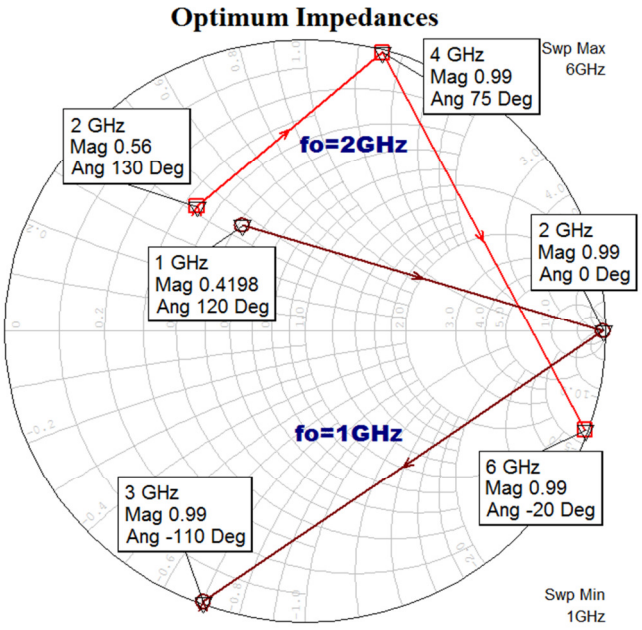


Figure 5.4 Optimum fundamental and harmonic loads at 1 GHz and 2 GHz

After obtaining the optimum load impedances as given in Figure 5.4, a tunable load matching circuit transforming the system impedance (50 ohm) to these impedances is designed in the next phase. A source matching circuit is also designed to complete the power amplifier structure.

5.3 Design Phase

The analysis phase is completed after the optimum fundamental and harmonic impedances are obtained at 1 GHz and 2 GHz. Then, a load matching circuit which transforms the system impedance (50 ohm) to the optimum impedances is designed in the design phase. The load matching circuit is preferred to be tunable because of the different multi-frequency load requirements. A source matching circuit is also designed in this phase to maximize the gain and maintain the stability of the power amplifier. Finally, the design of a band-selective power detection circuit embedded on the source matching circuit is presented. All circuit designs introduced in this section are performed by using the idealized transmission line models and lumped elements. The realization of the idealized transmission lines in microstrip form will be presented in the “Implementation Phase” section.

5.3.1 Load Matching Circuit Design

A load matching circuit design is required to transform the system impedance (50 ohm) to the impedances appearing in Figure 5.4 at the two operating frequencies. The problem is that two different load impedances are required at 2 GHz for optimum operation at both 1 GHz and 2 GHz fundamental frequencies. The solution is to design a tunable matching circuit which satisfies 1 GHz, 2 GHz and 3 GHz loads at 1 GHz operation and 2 GHz, 4 GHz and 6 GHz loads at 2 GHz operation in two different circuit forms.

Triple stub structure can be made tunable as shown in Figure 5.5 where the lengths and the terminations of the stubs, TL_1, TL_2, TL_3 , are reconfigured with the use of the switches, SW_1, SW_2 SW_3, and the tuning stubs, TL_7, TL_8, TL_9. The termination of the tuning stubs can be arranged either as open circuit or short circuit. An ideal switch presents a perfect short in the ON state, and a perfect open in the OFF state. Hence, when the switches are OFF, TL_1, TL_2 and TL_3 become open ended stubs. When the switches are ON, TL_7, TL_8 and TL_9 are merged with TL_1, TL_2 and TL_3 respectively. Then, two different matching circuits can be obtained at two different operating frequencies as long as the switches are controlled according to the operating frequency.

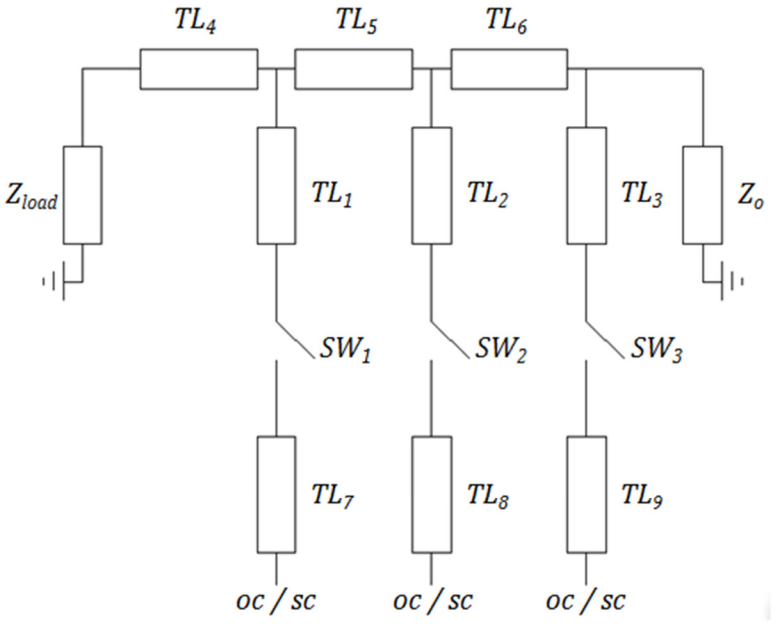


Figure 5.5 Triple stub circuit with tunable stubs

A simpler version of the structure given in Figure 5.5 is adopted for the load matching circuit of the dual band power amplifier as shown in Figure 5.6. In this circuit, the stub closest to the load, TL_1, is only made tunable. Moreover, the stubs, TL_2 and TL_7, are intentionally chosen as short-ended.

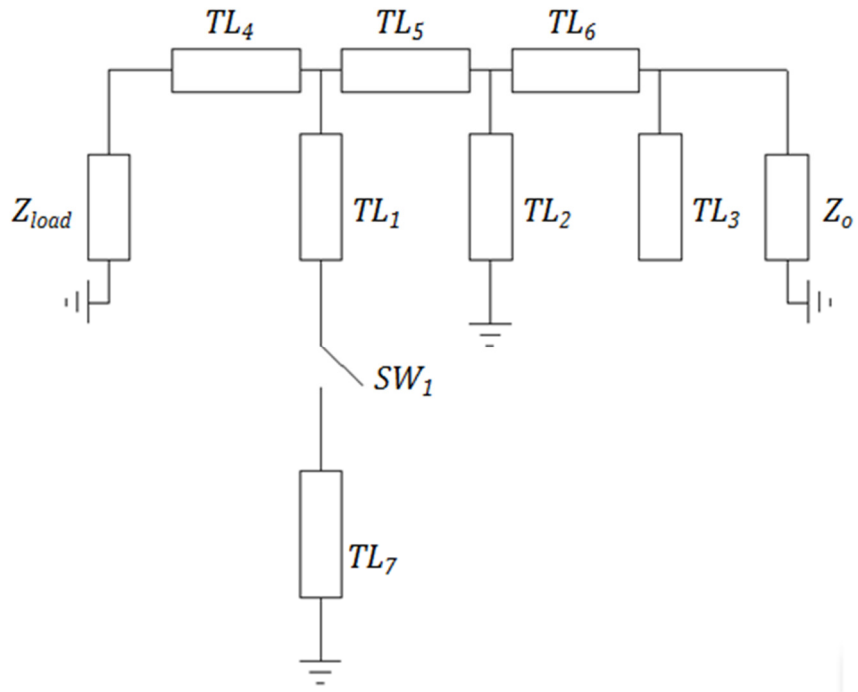


Figure 5.6 Simplified tunable triple stub circuit

When the switch is ON, the equivalent circuit of the tunable matching circuit given in Figure 5.6 is as shown in Figure 5.7. Then, TL_1 and TL_7 are connected in series to form a short ended stub with a longer electrical length. This condition is adopted for 1 GHz operation. On the other hand, when the switch is OFF, TL_7 is isolated from TL_1 leading to the equivalent circuit given in Figure 5.8 where TL_1 becomes open circuit terminated. At 2 GHz operation, this equivalent circuit is used for matching the fundamental and harmonic loads.

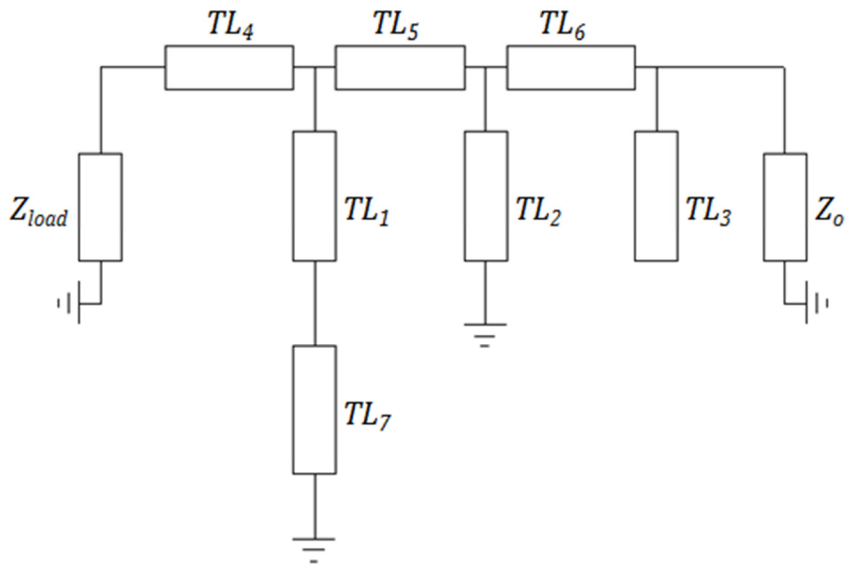


Figure 5.7 Equivalent circuit when the switch is ON (1 GHz operation)

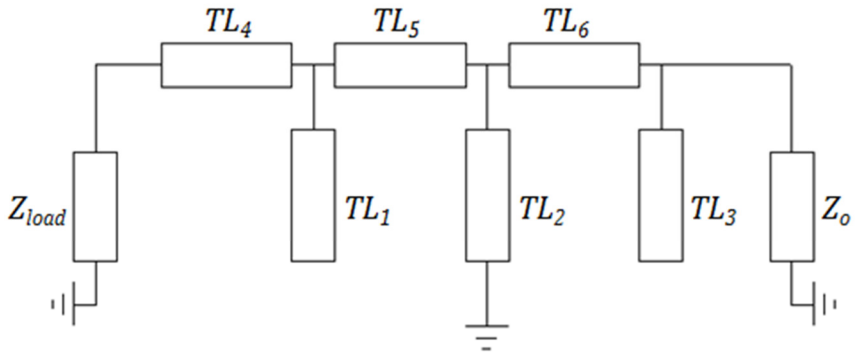


Figure 5.8 Equivalent circuit when the switch is OFF (2 GHz operation)

The required loads for 1 GHz operation shown in Figure 5.4 are tried to be matched with the circuit given in Figure 5.7. Similarly, the optimum loads for 2 GHz operation are to be satisfied with the circuit given in Figure 5.8. In order to gain an additional degree of freedom the transmission line characteristic impedances are not restricted to 50 ohm. Besides, the characteristic impedances of TL_1 and TL_7 are assigned the same for simplicity. Then, the electrical lengths and the impedances of the transmission lines are optimized to satisfy matching to the required loads. The optimized transmission line parameters are shown in Table 5-2.

Table 5-2 Transmission line parameters of the load matching circuit after optimization

Transmission Line	Impedance (Ohm)	Electrical Length @1 GHz (Degrees)
TL_1	25.1	12.1
TL_2	19.8	30
TL_3	13	24.4
TL_4	41.2	47.3
TL_5	11.5	29.1
TL_6	19.2	24.6
TL_7	25.1	74.5

With the optimized transmission line parameters, the simulated loads are obtained as given in Figure 5.9. It can be deduced from the results that the simplified tunable matching circuit is able to satisfy all required load impedances with little variation.

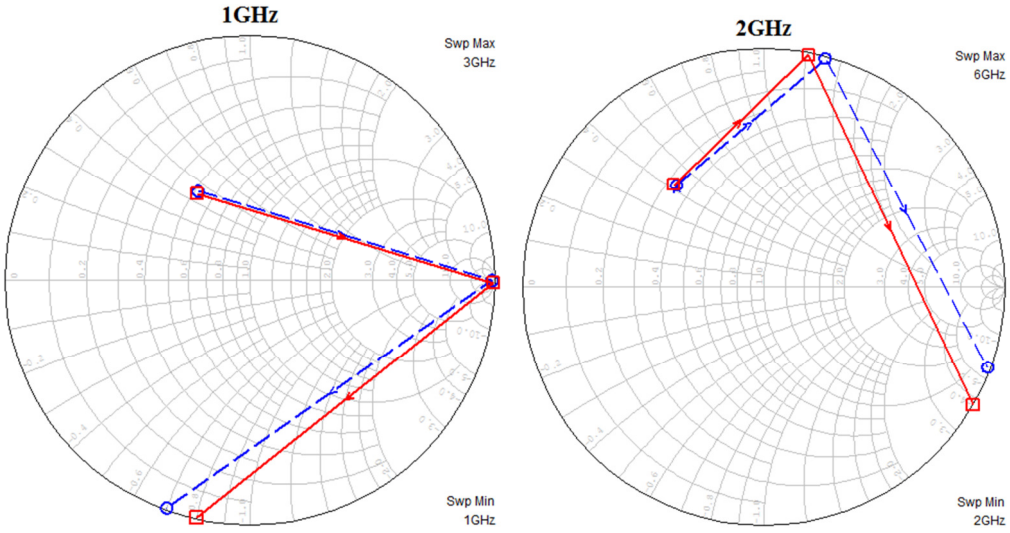


Figure 5.9 Optimum vs. simulated fundamental and harmonic loads at 1 GHz and 2 GHz (dashed: optimum, solid: simulated)

The switch required in the tunable circuit can be implemented with a pin diode. Pin diode is a device which shows a low resistance when sufficient current passes through the diode under forward bias condition. On the other hand, the pin diode presents a low capacitance when reverse biased. Then, a simple RF switch can be implemented by controlling the biasing of the pin diode.

MA4PBL027 pin diode from MACOM Inc. is selected for switch implementation due to its low package parasitics and low reverse capacitance [66]. Under 10mA forward current and -10V reverse voltage conditions, the MA4PBL027 pin diode can be modeled as a resistor and a capacitor respectively as shown in Figure 5.10.

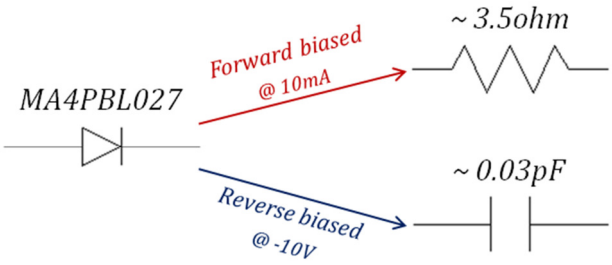


Figure 5.10 Approximate model of MA4PBL027 under forward and reverse biased conditions

Previously, the idealized switch model with zero resistance and zero capacitance is used during load simulations. When non-ideal switch model is used, the simulated loads are obtained as shown in Figure 5.11. Because of the very low OFF state capacitance of MA4PBL027, the fundamental and harmonic loads for 2 GHz operation are very close to the ideal condition. However, for 1 GHz operation, the 2nd harmonic load simulated as perfect open with the ideal model deviates because of the small finite ON state resistance (~ 3.5 ohm) of the pin diode.

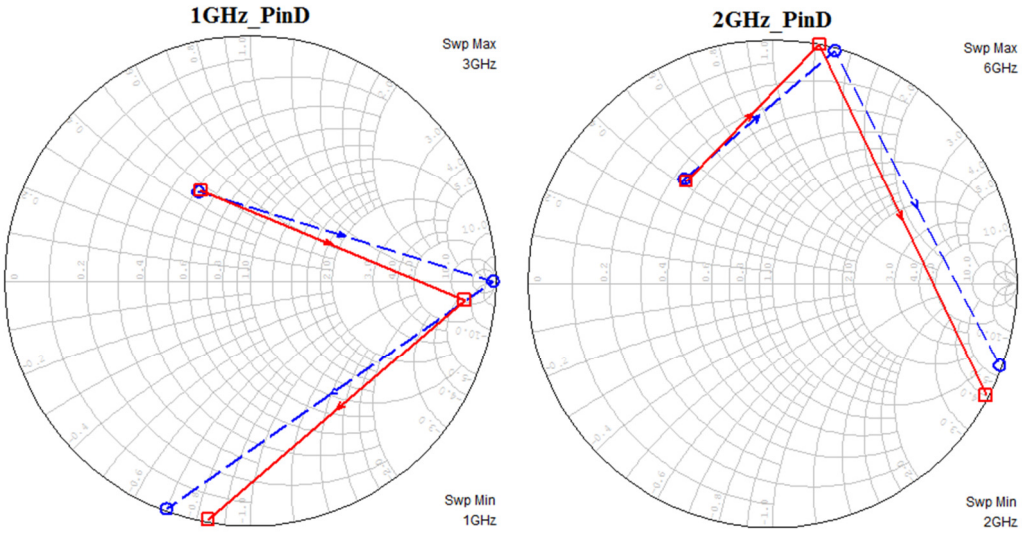


Figure 5.11 Optimum vs. simulated fundamental and harmonic loads at 1 GHz and 2 GHz when approximate model of MA4PBL027 is used (dashed: optimum, solid: simulated)

5.3.2 Source Matching Circuit Design

After the tunable load matching circuit is designed, a source matching circuit is required to provide optimum source impedances to the active device to maximize the gain of the power amplifier. Then, the power added efficiency of the amplifier is also increased; since, the input power required for the power amplifier is minimized when the gain is maximized. Source matching circuit is also designed to make the power amplifier unconditionally stable in order to prevent possible oscillations.

The circuit given in Figure 5.12 shows the basic structure of the source matching circuit. Triple stub topology is preferred similar to the load matching circuit. A tunable circuit is not preferred at the source side unlike to the load side; since, harmonic matching at the source side has less critical effect on the output power and efficiency as compared to the harmonic matching at the load side.

In addition to the transmission lines, some lumped components are used in the source matching circuit. R_1 and R_2 are simply used for suppressing in-band and out-of-band (low frequency) oscillations respectively. C_1 is put in parallel with R_1 to

minimize the gain drop at 2 GHz due to R_1 by providing a low impedance path. L_1 is simply used to provide a gate biasing path for the transistor.

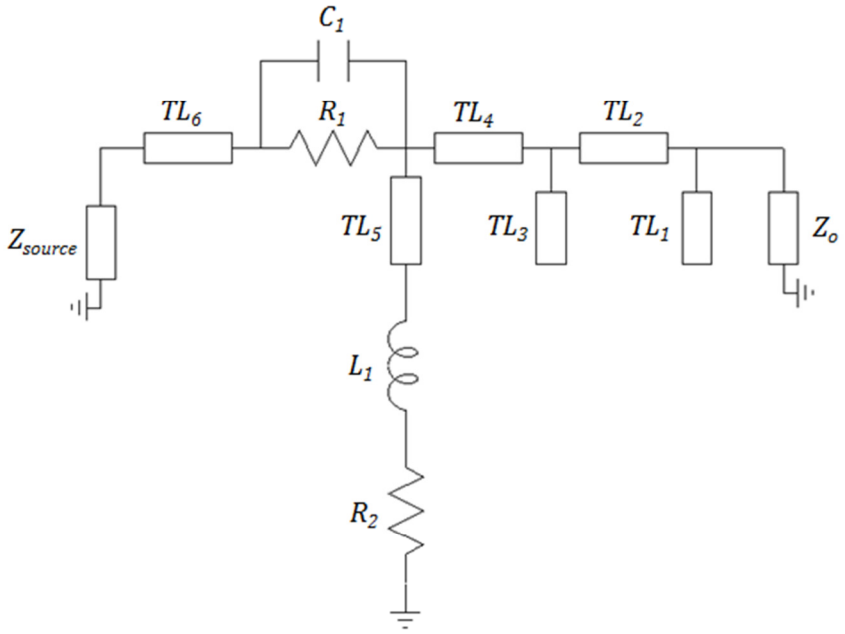


Figure 5.12 Topology of the source matching circuit

After optimizing the circuit for maximum gain and stability, the transmission line parameters and lumped component values are obtained as given in Table 5-3 and Table 5-4 respectively.

Table 5-3 Transmission line parameters of the source matching circuit after optimization

Transmission Line	Impedance (Ohm)	Electrical Length @1 GHz (Degrees)
TL_1	56.3	15.2
TL_2	27.6	57.3
TL_3	61.3	55.3
TL_4	18.1	45.6
TL_5	35.7	11.1
TL_6	43.9	18

Table 5-4 Lumped component values in the source matching circuit

Component	Value
R_1	10 ohm
R_2	25 ohm
C_1	5.1 pF
L_1	10 nH

Previously, the load matching circuit is designed as tunable with two different operating conditions according to the state of the switch whether ON or OFF. Hence, an external control is required to change the state of the switch according to the operating frequency. However, the source matching circuit is designed as a fixed circuit with only one operating condition; therefore, no external control is needed. One way to control the tunable load matching circuit is to detect the frequency of the input signal and create a suitable biasing voltage for the pin diode accordingly. The following section presents a simple way of performing this method. A band-selective circuit is designed and integrated at the end of one of the stubs in the source matching circuit. This circuit is designed to pass and suppress the coupled signals to the end of the stub at 1 GHz and 2 GHz operating frequencies respectively.

5.3.3 Band-Selective Power Detection Circuit Design

As mentioned previously, a band-selective power detection circuit is inserted at the end of the open circuited stub available in the source matching circuit. TL_1 stub in Figure 5.12 is used for this purpose. The aim is to design a circuit which suppresses 2 GHz and passes 1 GHz. Moreover, in order not to degrade the performance of the already designed source matching circuit given in Figure 5.12, the circuit should provide high impedance close to open circuit towards the end of TL_1 stub at both 1 GHz and 2 GHz. By this way, the termination of TL_1 is maintained at near open circuit for both 1 GHz and 2 GHz operations. The proposed circuit is a

double stub circuit as shown in Figure 5.13. The lengths of the transmission lines, TL_{d1} and TL_{d2} are fixed at λ/4 at 2 GHz. By this way the impedance at node-1 is always maintained at short-circuit, so that, the signal at 2 GHz is suppressed. At the same time, short-circuit at node-1 is transformed to an open-circuit thanks to the λ/4 length of TL_{d1} at 2 GHz. After fixing the lengths of TL_{d1} and TL_{d2}, the parameters of TL_{d3} and TL_{d4} are optimized to transform 50 ohm impedance in the left-hand-side to high impedance in the right-hand-side at 1 GHz. With the optimized transmission line parameters given in Table 5-5, the impedance level at the right-hand-side at 1 GHz is around 1000 ohm which is near open circuit.

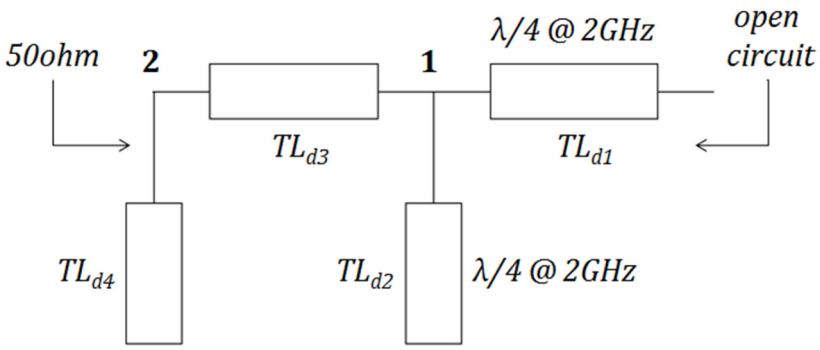


Figure 5.13 Band-selective power detection circuit

Table 5-5 Optimized transmission line parameters of the circuit given in Figure 5.13

Transmission Line	Impedance (Ohm)	Electrical Length @2 GHz (Degrees)
TL_1	78.3	90
TL_2	71.7	90
TL_3	79.6	64.6
TL_4	16.3	115

5.4 Implementation Phase

At this phase, the matching circuits designed previously using ideal transmission lines are realized in microstrip technology on a 20 mil thick RO4003C substrate (ε_r=3.66) [67]. The biasing circuits are also integrated into the matching circuits. Finally, the measurement results of the fabricated power amplifier are presented.

5.4.1 Realization of the Matching Circuits

The complete circuit schematic of the designed power amplifier with the source and the load matching circuits integrated is shown in Figure 5.14. The corresponding layout is also given in Figure 5.15.

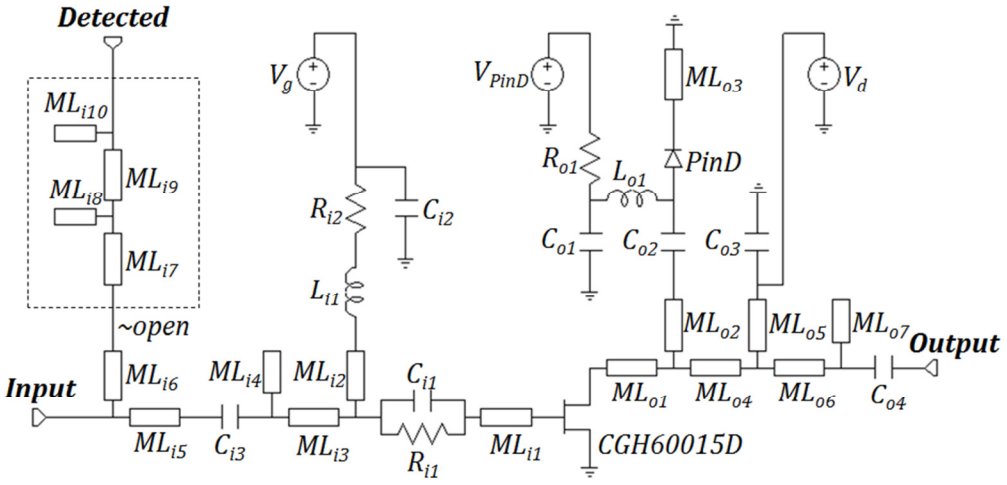


Figure 5.14 Complete circuit schematic of the designed power amplifier

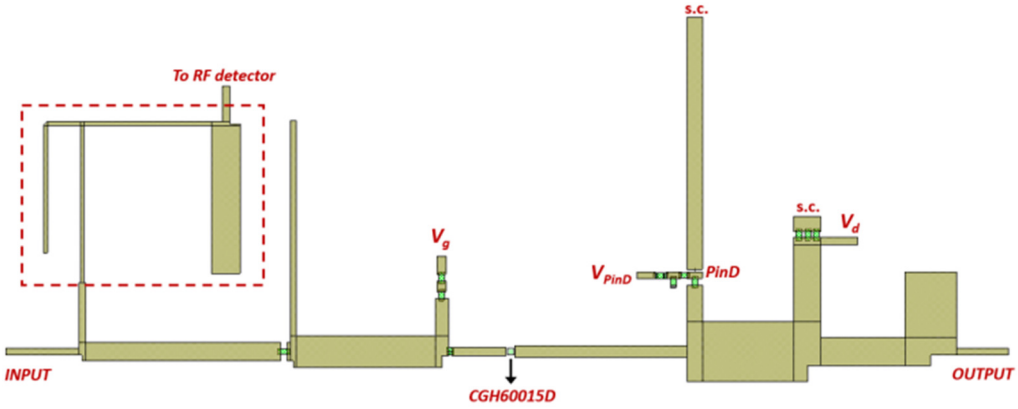


Figure 5.15 The layout of the designed power amplifier

The parameters of the microstrip lines shown in Figure 5.14 are first obtained by an equivalent transformation of the ideal transmission line parameters calculated in "Design Phase" section. Then, the equivalent microstrip line parameters are optimized yielding the parameters given in Table 5-6.

Table 5-6 Microstrip line parameters after optimization

Microstrip Line	Width (mm)	Length (mm)
ML_{i1}	1.35	7.53
ML_{i2}	1.83	5.36
ML_{i3}	4.39	19.44
ML_{i4}	0.76	30.04
ML_{i5}	2.59	27.76
ML_{i6}	0.89	8.39
ML_{i7}	0.51	21.84
ML_{i8}	0.51	22.86
ML_{i9}	0.51	17.78
ML_{i10}	4.06	21.34
ML_{o1}	1.78	24.02
ML_{o2}	2.18	6.10
ML_{o3}	2.18	35.15
ML_{o4}	8.43	12.41
ML_{o5}	3.93	13.23
ML_{o6}	4.03	11.69
ML_{o7}	7.20	9.18

In the circuit given in Figure 5.14, C_{i3}, C_{o2} and C_{o4} are the DC blocking capacitors. In addition, C_{i2}, C_{o1} and C_{o3} are the RF decoupling capacitors. The termination of ML_{o5} is made short circuited via C_{o3} capacitor. On the other hand, the short-ended ML_{o3} provides a current flow path for the pin diode when forward biased.

Three biasing voltages, named as V_d, V_g and V_{PinD}, are required for power amplifier operation. V_d and V_g voltages are used as +28V and -2.9V respectively which yield around 100mA quiescent current. V_{PinD} does not have a fixed value; instead, two different biasing voltages are used according to the operating frequency. At 1 GHz operation, the pin diode should be forward biased; therefore, a sufficiently high positive voltage should be applied from V_{PinD}. +5V is used for V_{PinD} in forward biased condition and the forward biased current is adjusted to around 20 mA with R_{o1} resistor. On the other hand, the pin diode should be reverse biased with a sufficiently negative voltage at 2 GHz operation. Since the GaN transistor operates with a high drain voltage, the voltage swing across the pin diode is also high when the RF output is available. Figure 5.16 shows the simulated voltage swing across the pin diode terminals under reverse biased condition. Then, a sufficiently negative voltage is required for the pin diode not to enter into breakdown during reverse biased condition. During the trials, it is observed that -25V is adequate as the reverse biasing voltage of the pin diode.

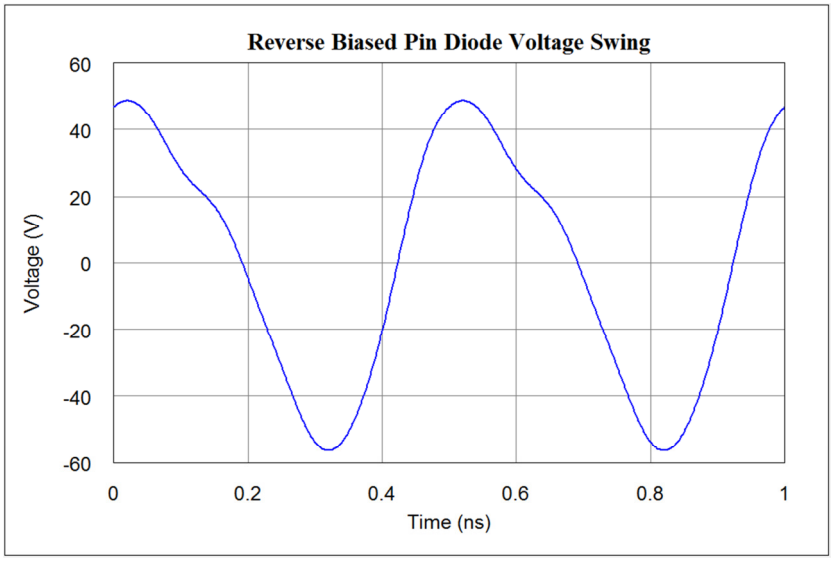


Figure 5.16 The voltage swing across the pin diode terminals under reverse biased condition

5.4.2 Simulated RF Performances

With the optimized microstrip line parameters given in Table 5-6, the simulation results of the various RF characteristics are summarized from Figure 5.17 through Figure 5.26.

Figure 5.17 shows the simulated Rollets's stability factor (K-factor) at 1 GHz and 2 GHz operations. Since K-factor is greater than unity over a wide frequency range covering the non-operating frequencies also, stable operation of the power amplifier is ensured.

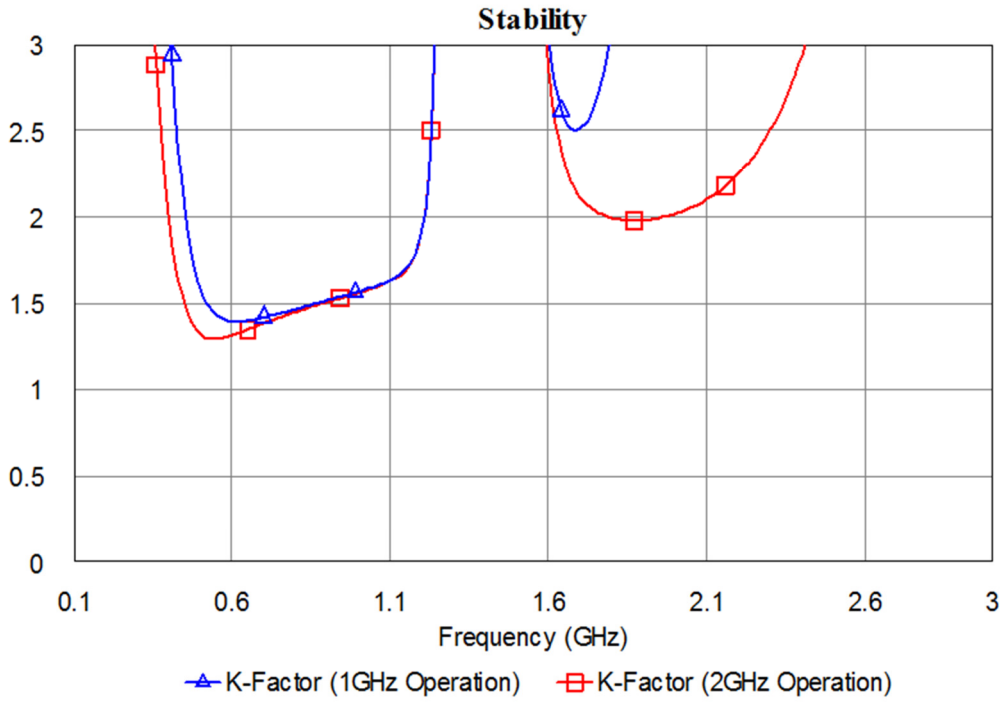


Figure 5.17 Simulated Rollet's stability factor for 1GHz & 2GHz operations

Figure 5.18 shows the output of the band-selective power detection circuit. Approximately 10 dB coupling exists between the input port and the detected port for 1 GHz operation. At 2 GHz, the signal disappears at the detected port thanks to the high suppression of the designed circuit. Then, the signal obtained from the detected port can be used as an indication of 1 GHz signal at the input which can also be used to control the pin diode at the output for a self-tunable PA structure.

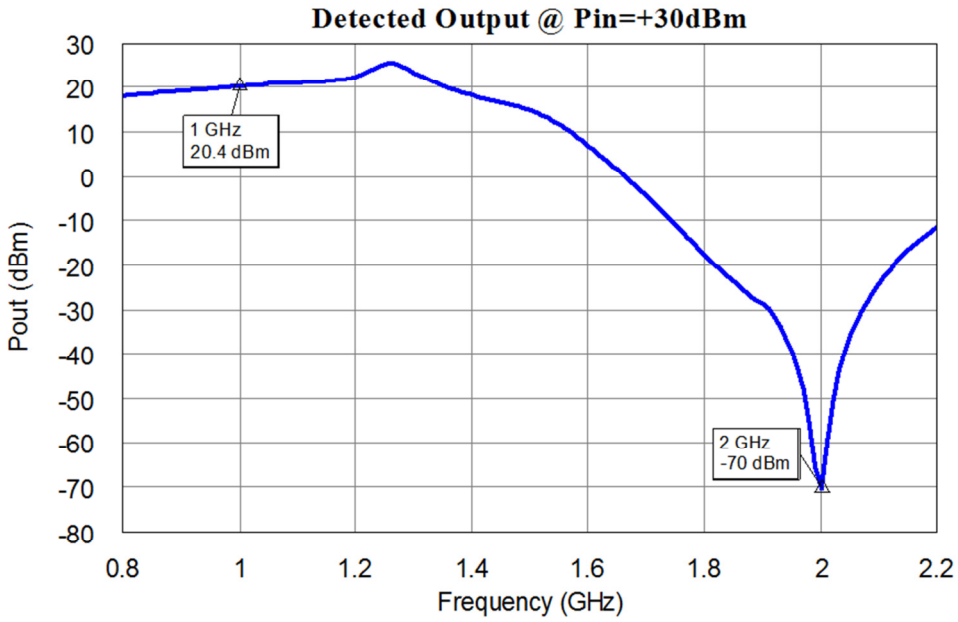


Figure 5.18 Simulated detector output @ Pin=+30 dBm

Figure 5.19 and Figure 5.20 show the simulated S11 and S21 at lower band (1 GHz) and upper band (2 GHz) operations respectively. The simulated small signal gains are around 20 dB at 1 GHz and 16 dB at 2 GHz. In addition, nearly 11 dB of power gain is simulated at both frequencies when the input power is held constant at +30 dBm.

The simulated output power and PAE graphs obtained at +30 dBm of input power are demonstrated in Figure 5.21 and Figure 5.22. At 1 GHz, nearly 42 dBm output power is obtained together with PAE close to 75%. At 2 GHz, around 41 dBm output power and 70% PAE are achieved. These output power and PAE performances are achieved with harmonic levels lower than -30 dBc as shown in Figure 5.23 and Figure 5.24.

The current and voltage waveforms appearing at the drain of the transistor are plotted in Figure 5.25 and Figure 5.26. The overlapping of the current and voltage waveforms are minimized for both operating frequencies thanks to the harmonic load matching. This waveform shaping results in PAE levels greater than 70% for both operating bands.

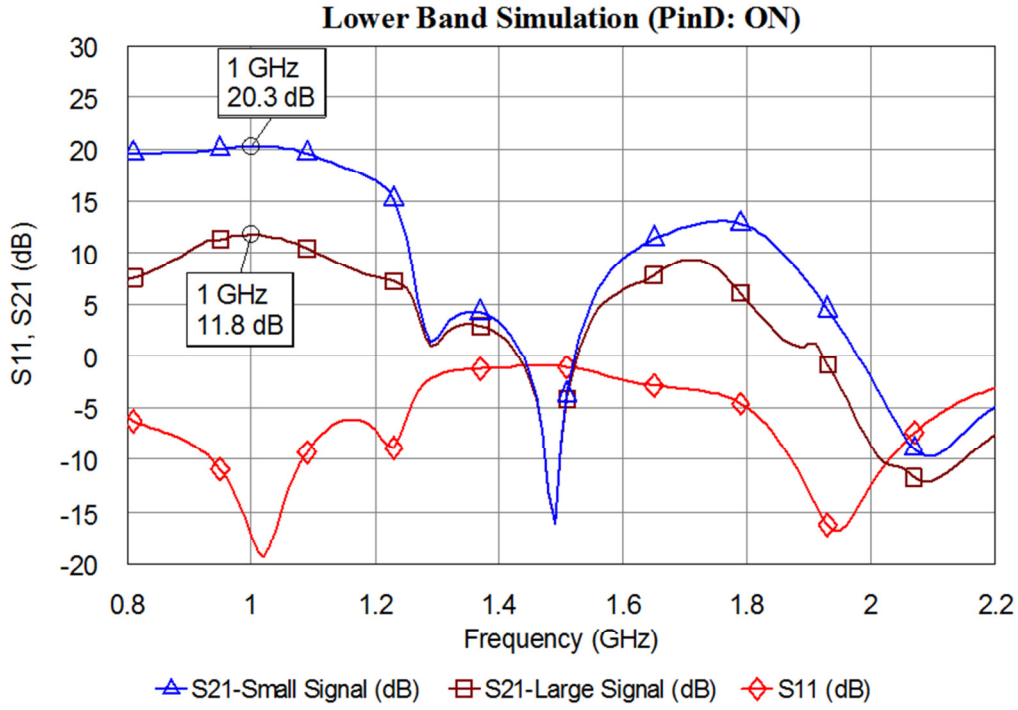


Figure 5.19 Lower band S11&S21 simulation results (pin diode: ON)

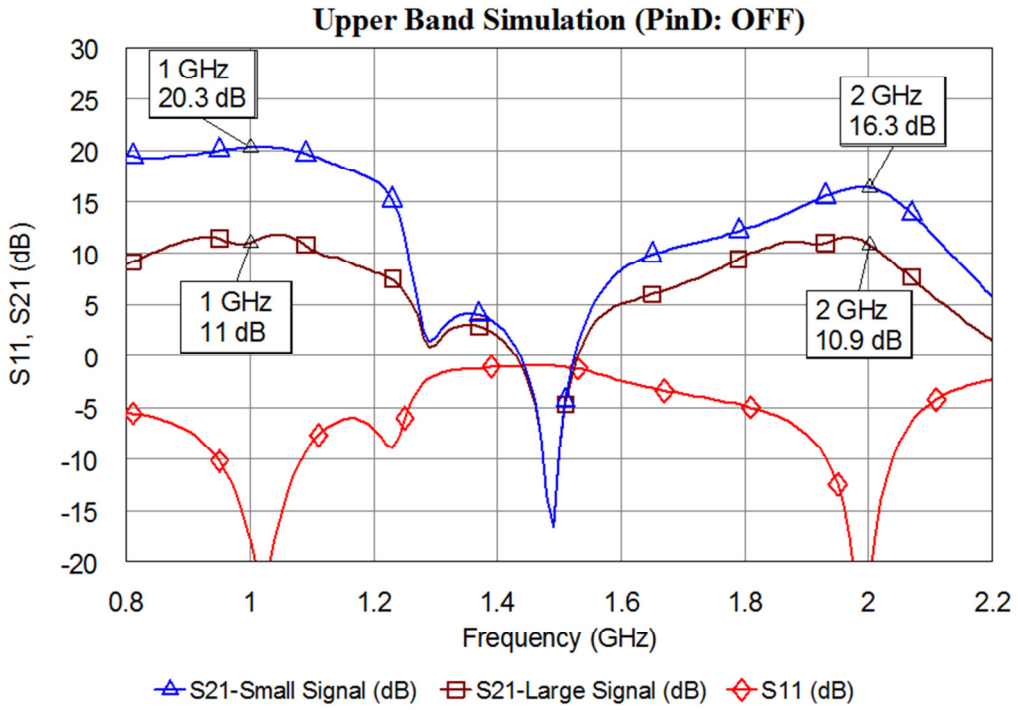


Figure 5.20 Upper band S11&S21 simulation results (pin diode: OFF)

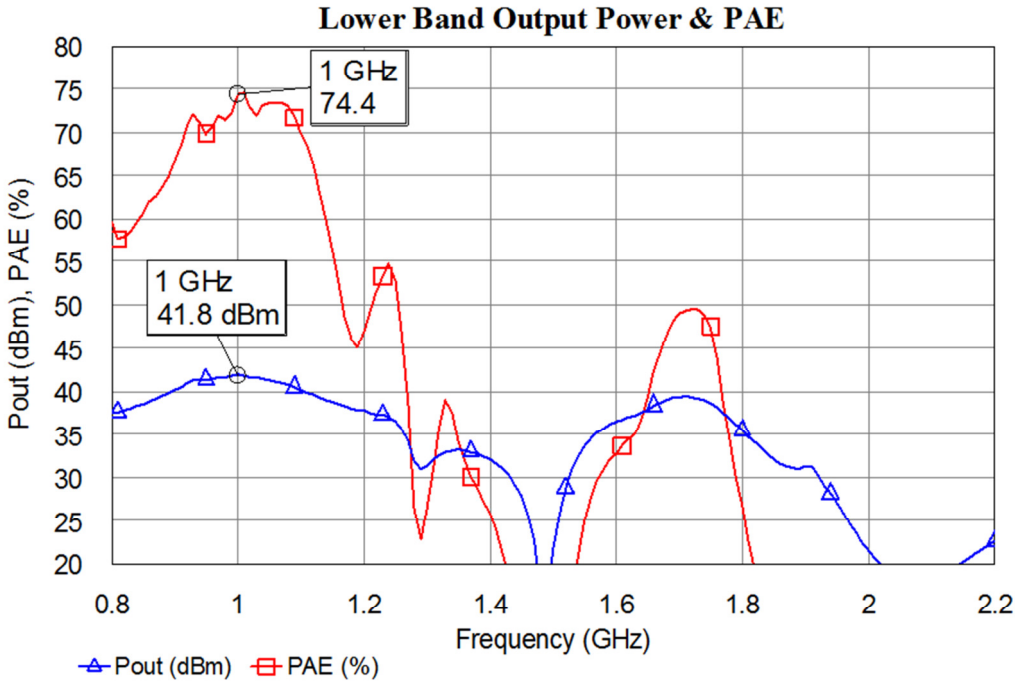


Figure 5.21 Lower band output power & PAE simulation results (pin diode: ON)

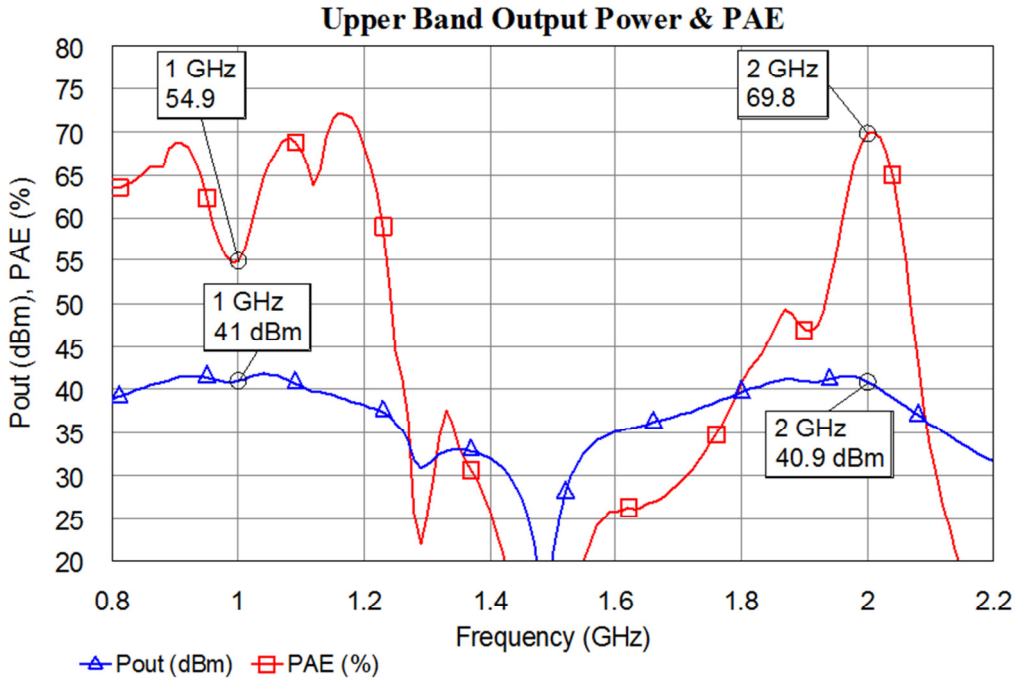


Figure 5.22 Upper band output power & PAE simulation results (pin diode: OFF)

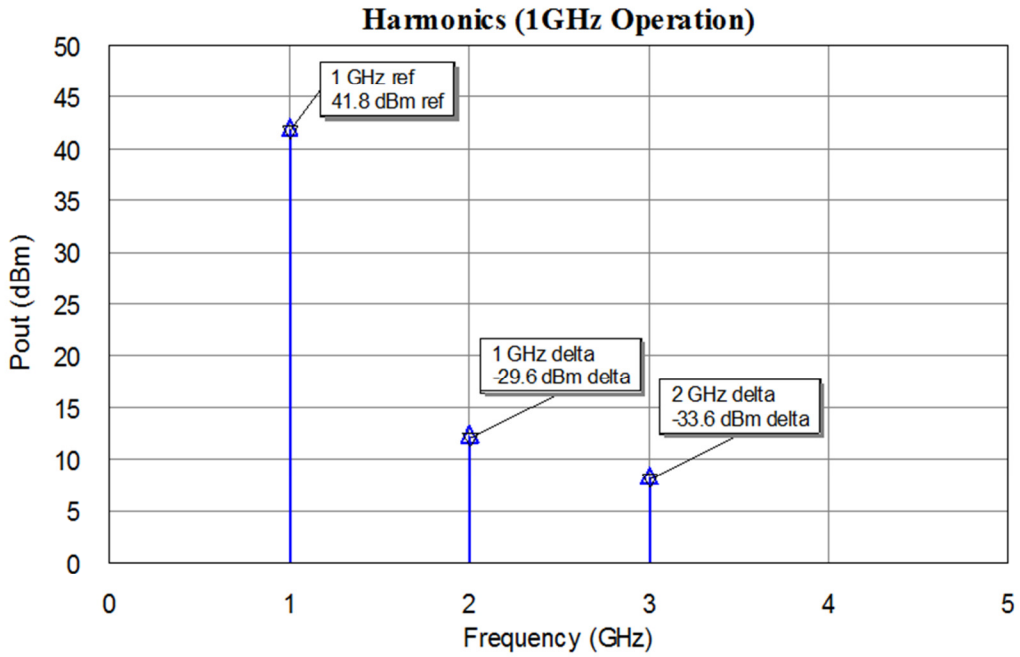


Figure 5.23 Simulated harmonics @ 1GHz (pin diode: ON)

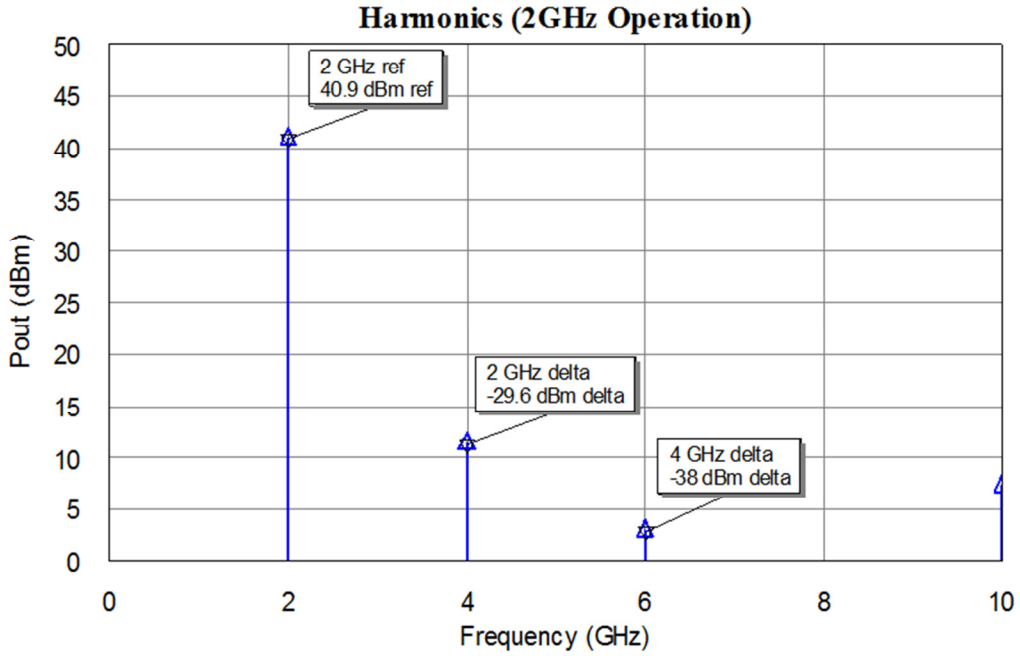


Figure 5.24 Simulated harmonics @ 2GHz (pin diode: OFF)

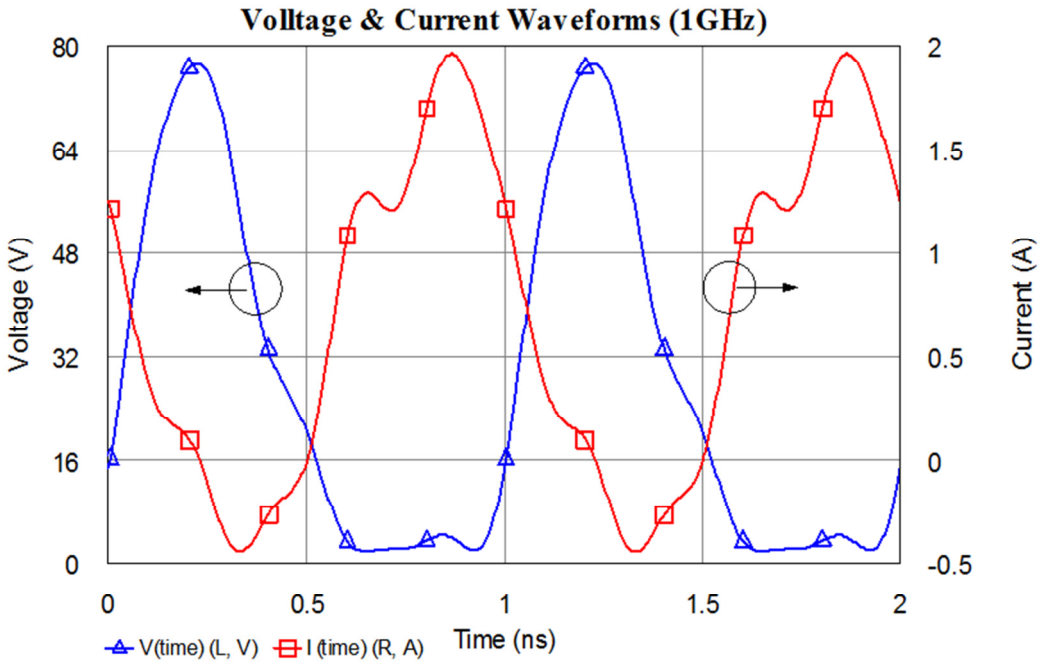


Figure 5.25 Simulated voltage and current waveforms @ 1GHz (pin diode: ON)

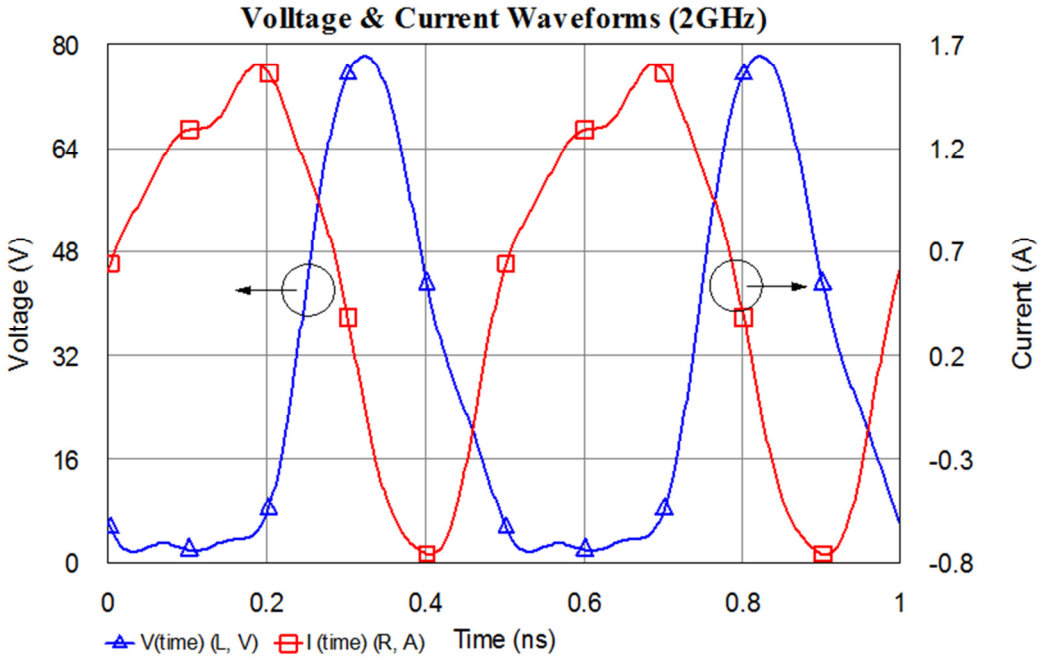


Figure 5.26 Simulated voltage and current waveforms @ 2GHz (pin diode: OFF)

5.4.3 Fabrication of the Power Amplifier and Measurements

The realized dual band power amplifier is pictured in Figure 5.27. The zoomed GaN transistor die is mounted on an aluminum base by Sk70N thermal epoxy from Namics Corporation for improved thermal performance. The overall size of the PA is about 140 mm x 60 mm.

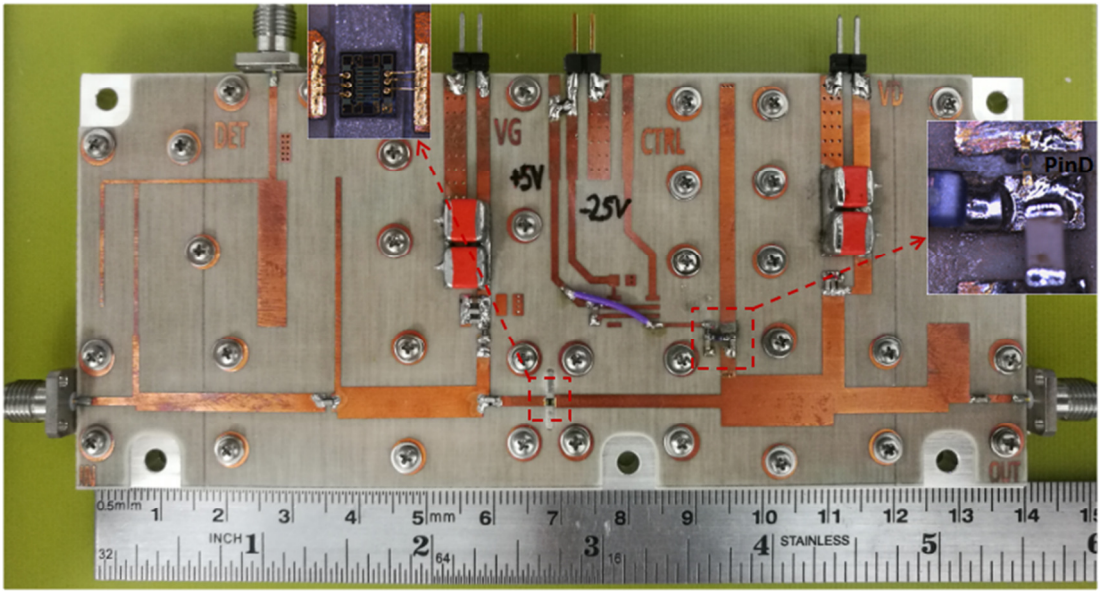


Figure 5.27 Realized dual-band power amplifier

The setup demonstrated in Figure 5.28 is used while measuring the performance of the fabricated PA. A driver PA is used to bring the power output of the signal source to the power levels required to saturate the fabricated PA. An isolator is placed between the driver PA and the main PA not to degrade the performance of the driver PA due to the input return loss variations of the main PA. An attenuator is inserted at the output of the main PA to bring the power levels inside the limits of the power meter and spectrum analyzer. The drain supply of the main PA (+28V) and the required supply of the driver PA (+15V) are applied from the two separate power supplies. Besides, a triple output power supply is allocated for the gate supply (-2.9V) and the alternating pin diode supplies (+5V & -25V).

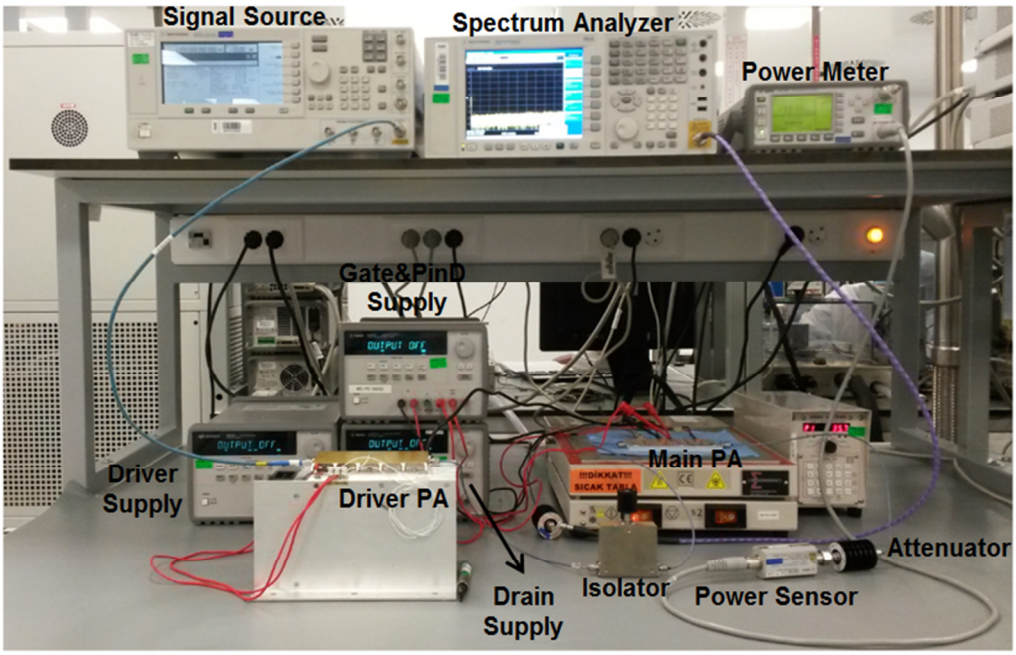


Figure 5.28 Measurement setup

The measurements are separated as the small signal and the large signal measurements. Network analyzer is the main device used for the small signal measurements. On the other hand, power meter and spectrum analyzer are used for the large signal measurements.

5.4.3.1 Small Signal Measurements

The small signal measurements are summarized in Figure 5.29, Figure 5.30 and Figure 5.31 together with the simulated results for comparison. Figure 5.29 shows the measured coupling between the input port and the detected port of the realized PA. The coupling levels are measured around -13dB and -55dB at 1 GHz and 2 GHz respectively. The frequency response of the measured coupling shows a good correlation with the simulated coupling. Figure 5.30 and Figure 5.31 show the comparison of the measured and the simulated small signal gain and input return loss performances for two different operating modes of the pin diode. Even though, the measured results follow the pattern of the simulated results closely up to 1.5 GHz, the measured gain peak above 1.5 GHz shifts from 2 GHz towards 1.7 GHz with approximately 3dB decrease in the gain.

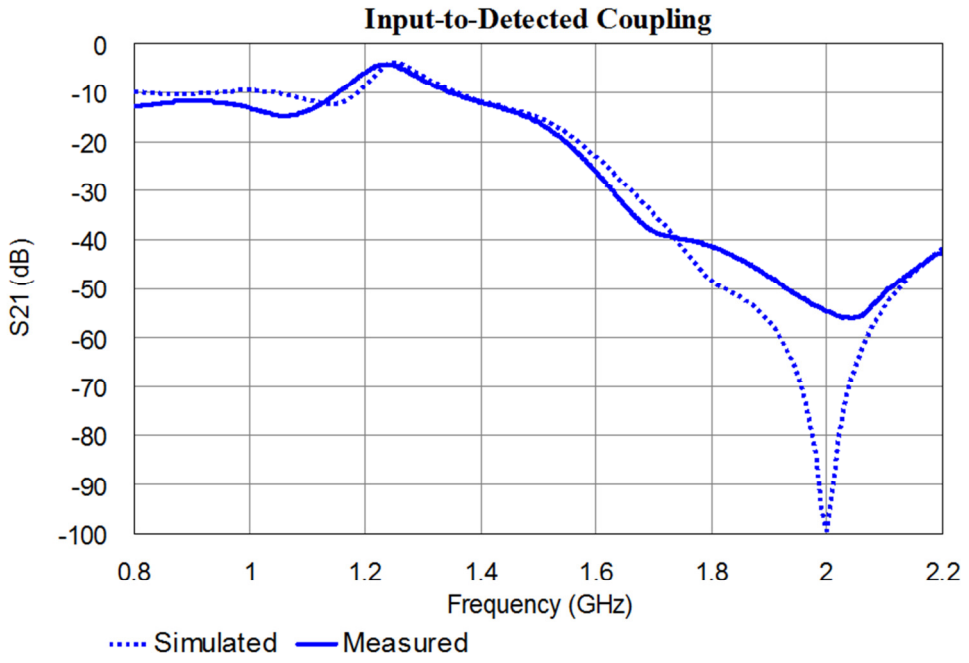


Figure 5.29 Measured (solid) vs. simulated (dashed) coupling between the input and detected ports

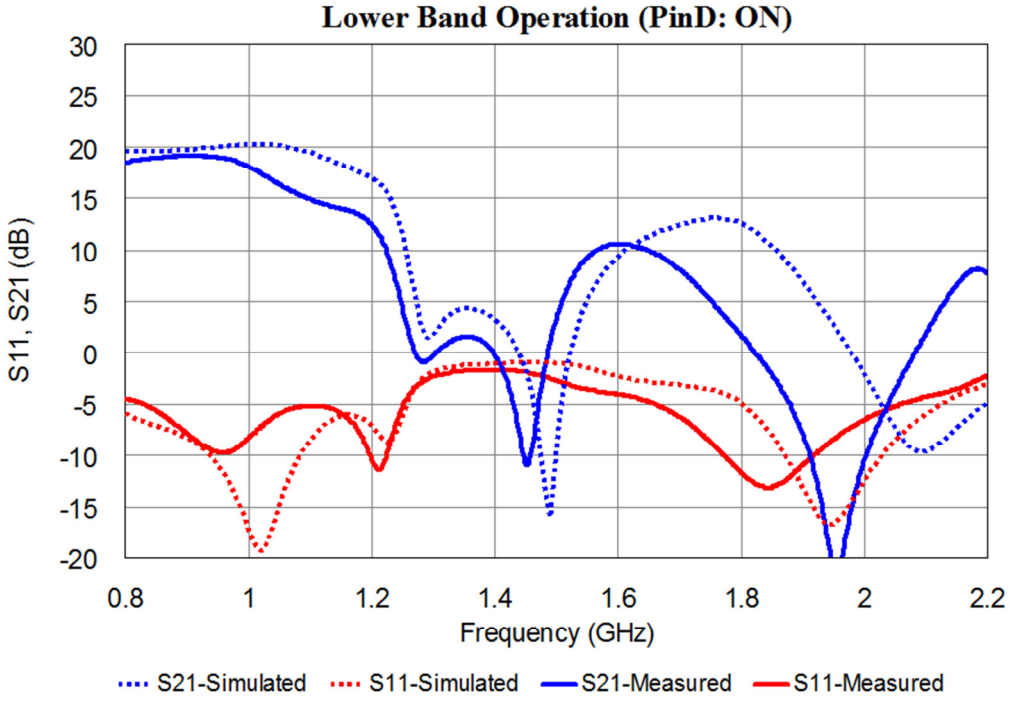


Figure 5.30 Measured (solid) vs. simulated (dashed) S11 & S22 (pin diode: ON)

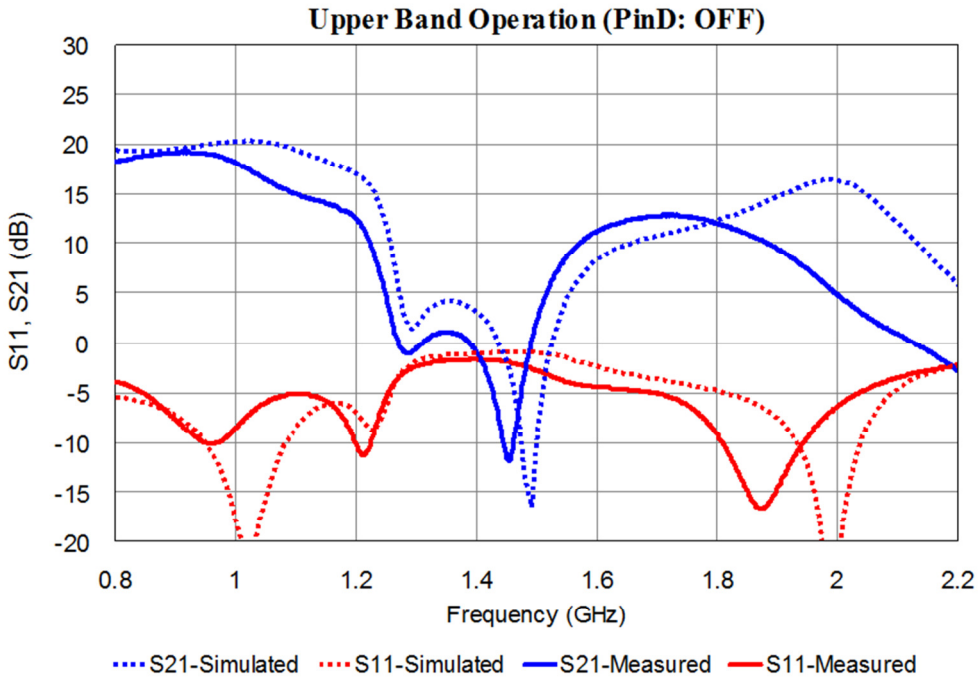


Figure 5.31 Measured (solid) vs. simulated (dashed) S11 & S22 (pin diode: OFF)

According to the measured small signal responses presented in Figure 5.30 and Figure 5.31, the lower band and the upper band shift towards 0.9 GHz and 1.7 GHz respectively as compared to the simulated bands of 1 GHz and 2 GHz. Then, the large signal measurements are carried out around these shifted frequency bands to obtain optimum performances.

5.4.3.2 Large Signal Measurements

Small signal measurements show that gain is maximized around 0.9 GHz for lower band operation when pin diode is ON. On the other hand, 1.7 GHz is the approximate frequency of the peak gain for upper band operation when pin diode is OFF. Then, output power, PAE and DE measurements are carried out in the vicinity of 0.9 GHz and 1.7 GHz and the results are shown in Figure 5.32. The graphs given in Figure 5.32 include two separate measurements which are shown as dashed and solid traces. Dashed traces correspond to the measurements obtained by externally connecting and disconnecting C_{o2} and ML_{o3} shown in Figure 5.14 instead of pin diode. “Ideal short” is achieved by a thru ribbon-bond

connection between C_{o2} and ML_{o3}. On the other hand, "Ideal open" is realized by removing this ribbon-bond connection.

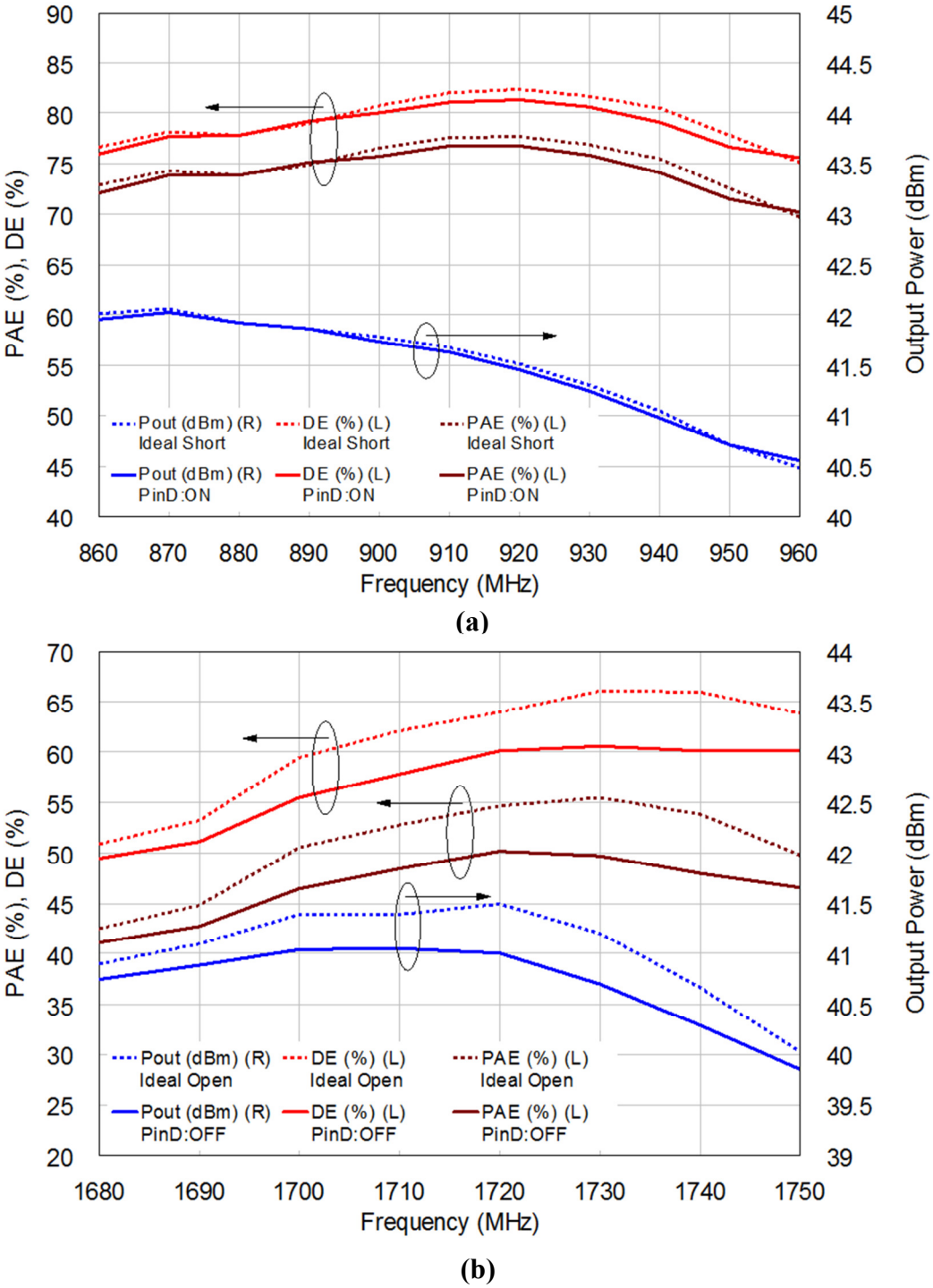
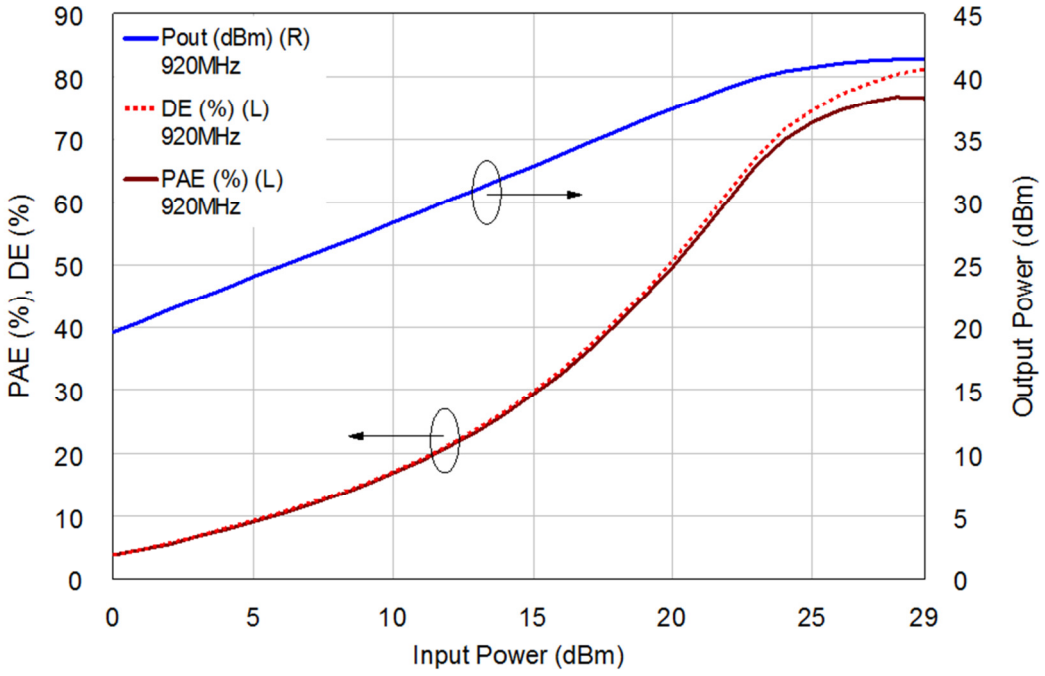
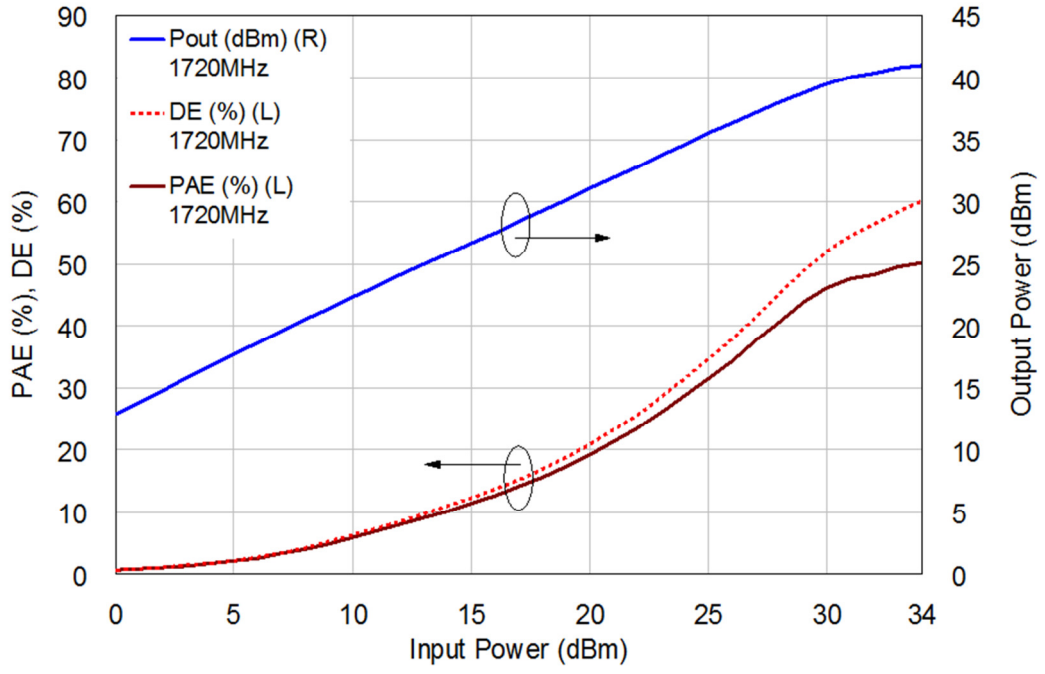


Figure 5.32 Measured Pout, DE and PAE in terms of frequency (dashed: ideal, solid: pin diode)
(a) at lower band (b) at upper band



(a)



(b)

Figure 5.33 Measured Pout, DE and PAE in terms of input power

(b) at 920MHz & pin diode :ON (b) at 1720MHz & pin diode: OFF

As shown in Figure 5.32, “Ideal short” measurement closely follows the measurement obtained by a pin diode with ON state. This is because of the low series resistance of the pin diode when forward biased. On the other hand, the deviation between “Ideal open” measurement and “Pin diode: OFF” measurement is more significant. At 1720 MHz, 0.5 dB decrease in the output power and 5% reduction in the efficiency are observed when pin diode is used. The main reason for this variation is that the large voltage swing appearing on the pin diode modulates the OFF state capacitance of the pin diode. Then, the isolation achieved by the reverse biased pin diode is degraded during large signal measurements and the measured performance deviates from the perfect isolation case (“Ideal open” case).

The large signal measurements with pin diode show that maximum efficiencies are achieved at 920 MHz and 1720 MHz when the pin diode is ON and OFF respectively. At 920 MHz, the measured output power, DE and PAE are 41.5 dBm, 81.3% and 76.7% respectively. At 1720 MHz, 41 dBm output power is obtained together with 60.2% DE and 50.2% PAE.

Figure 5.33 shows the output power, DE and PAE measured at 920 MHz and 1720 MHz in terms of input power. The maximum efficiencies at 920 MHz and 1720 MHz are obtained at 29 dBm and 34 dBm input power levels respectively.

Figure 5.30 and Figure 5.31 show identical small signal performance at lower band for both states of the pin diode. Since the pin diode is mainly used for tuning the 2^{nd} harmonic load at lower band, the fundamental load does not change according to the state of the pin diode. Then, small signal parameters which depend mainly on fundamental source and load impedances do not change whether pin diode is ON or OFF. As explained before, the purpose of pin diode tuning at lower band is to be able to satisfy optimum harmonic load impedances; mainly the 2^{nd} harmonic load impedance. Then, efficiency at lower band will be improved. Figure 5.34 and Figure 5.35 give a comparison of the large signal measurements obtained for ON and OFF states of the pin diode at lower band of operation. It can be seen that, pin diode tuning not only enhances the efficiency; but also, reduces the harmonic levels. For example, at 920 MHz, both DE and PAE are improved more than 15% without a

change in the output power, when pin diode is switched from OFF state to ON state. On the other hand, 2nd harmonic level drops from -10 dBc to -25 dBc and 3rd harmonic level is lowered about 5 dB. These results clearly prove the use of the proposed tunable structure.

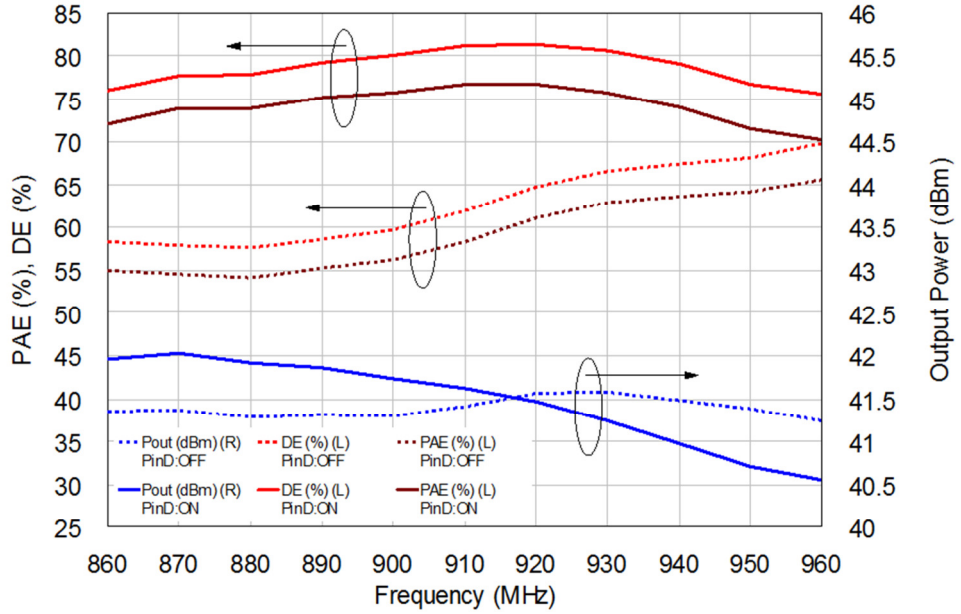


Figure 5.34 Lower band Pout, DE and PAE (solid: pin diode: ON, dashed: pin diode: OFF)

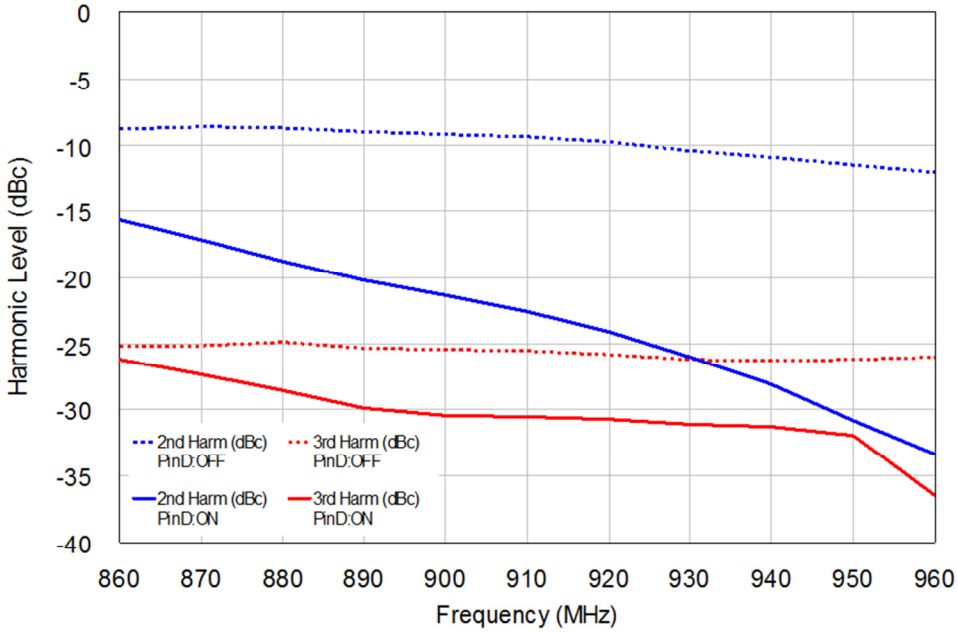


Figure 5.35 Lower band harmonic levels in dBc (solid: pin diode: ON, dashed: pin diode: OFF)

5.4.4 Post-Tuning

In Section 5.4.3, the small signal and the large signal measurements of the implemented dual band PA are presented. The measured results mainly differ from the simulated results in terms of the optimum band frequencies. While the PA is aimed to operate at 1 GHz and 2 GHz band frequencies with maximized efficiencies, the realized PA gives maximum efficiency at 0.92 GHz and 1.72 GHz frequencies. In this section, the reasons for this band shift are investigated in detail and the design of a modified dual band PA to recover the aimed band frequencies is presented.

As mentioned previously, the EM and nonlinear simulations of the PA are performed in Microwave Office^{TM} simulation environment. During these simulations, built-in EM-based models named as X-models are used for microstrip bends and tee-junctions assuming better accuracy. However, after examining carefully, it is seen that the maximum width restriction of some X-models are exceeded. For example, EM-based microstrip tee-junction model in Microwave Office named as MTEEX^{TM} has minimum width and maximum width restrictions as 0.25*substrate_thickness and 4*substrate_thickness respectively [72]. However, most of the optimized microstrip line widths given in Table 5-6 exceed the maximum width limit of 2 mm for a substrate thickness 0.5 mm. Then, the use of X-models out of limits in the simulations is suspected to be the reason for the shift of band frequencies.

In addition to EM-based models, there are also closed-form models available in Microwave Office^{TM} for microstrip junctions. These closed form models basically use the results of analytical expressions instead of EM simulation results. Then, all EM-based (X) models used in the previous simulations are replaced by the corresponding closed-form models to see the effect on simulated performance. Figure 5.36 shows the comparison of the small signal gains simulated by EM-based and closed form models with the measured gain. It is clear that closed form models are more successful in estimating the measured gain especially at the upper band as compared to the EM-based models exceeding the maximum width restrictions of the model.

The output power and PAE simulations are also repeated again for the case of closed-form models. As shown in Figure 5.37, the lower band and the upper band frequencies with peak efficiencies are nearly the same with the measured results.

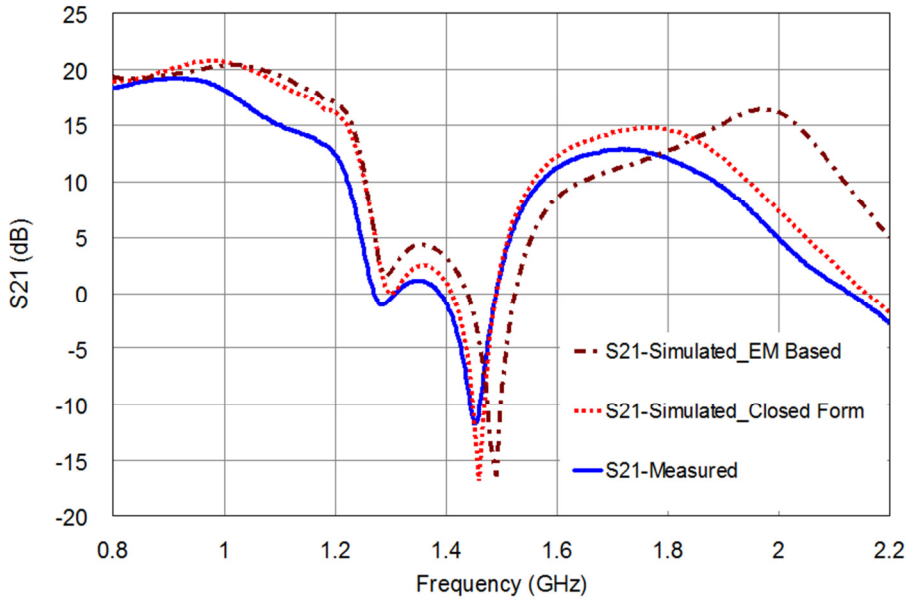


Figure 5.36 Comparison of measured gain with the simulated gains obtained by EM-based and closed-form microstrip models (pin diode: OFF)

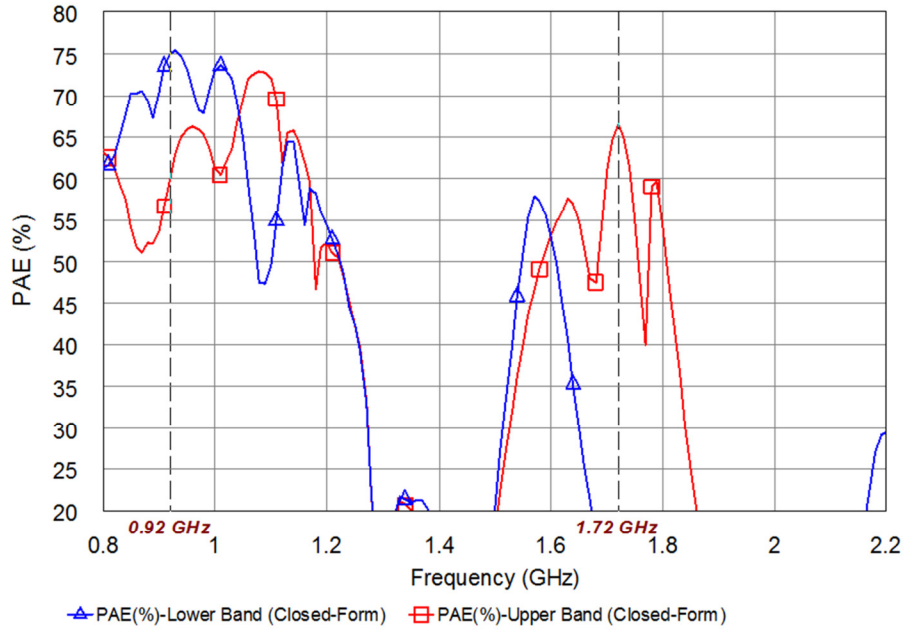


Figure 5.37 Simulated output power and PAE with closed-form microstrip models

After determining the reason for the observed band shift as the use of EM-based microstrip junction models out of limits, a modified design is performed by using closed form microstrip junction models. Table 5-7 lists the optimized microstrip line parameters of the modified PA which has the same schematic representation with the previous design as given in Figure 5.14.

Table 5-7 Optimized parameters of microstrip lines in Figure 5.14 for the modified PA

Microstrip Line	Width (mm)	Length (mm)
ML_{i1}	1.02	7.48
ML_{i2}	1.83	5.33
ML_{i3}	3.58	19.44
ML_{i4}	0.72	26.35
ML_{i5}	1.66	27.38
ML_{i6}	0.89	6.89
ML_{i7}	0.51	21.84
ML_{i8}	0.51	22.86
ML_{i9}	0.51	17.78
ML_{i10}	4.06	20.57
ML_{o1}	1.75	23.42
ML_{o2}	2.69	2.33
ML_{o3}	2.69	34.75
ML_{o4}	6.55	12.96
ML_{o5}	1.15	7.98
ML_{o6}	2.39	6.37
ML_{o7}	5.88	9.75

The picture of the implemented PA after post-tuning is shown in Figure 5.38. The small signal and the large signal measurements of the revised PA are also summarized from Figure 5.39 to Figure 5.43.

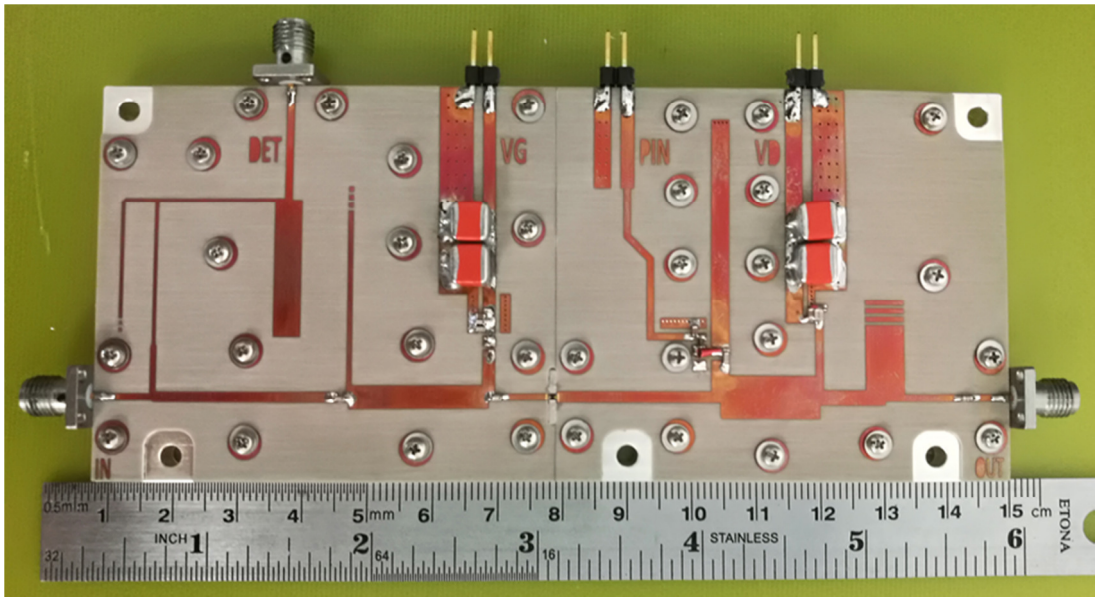
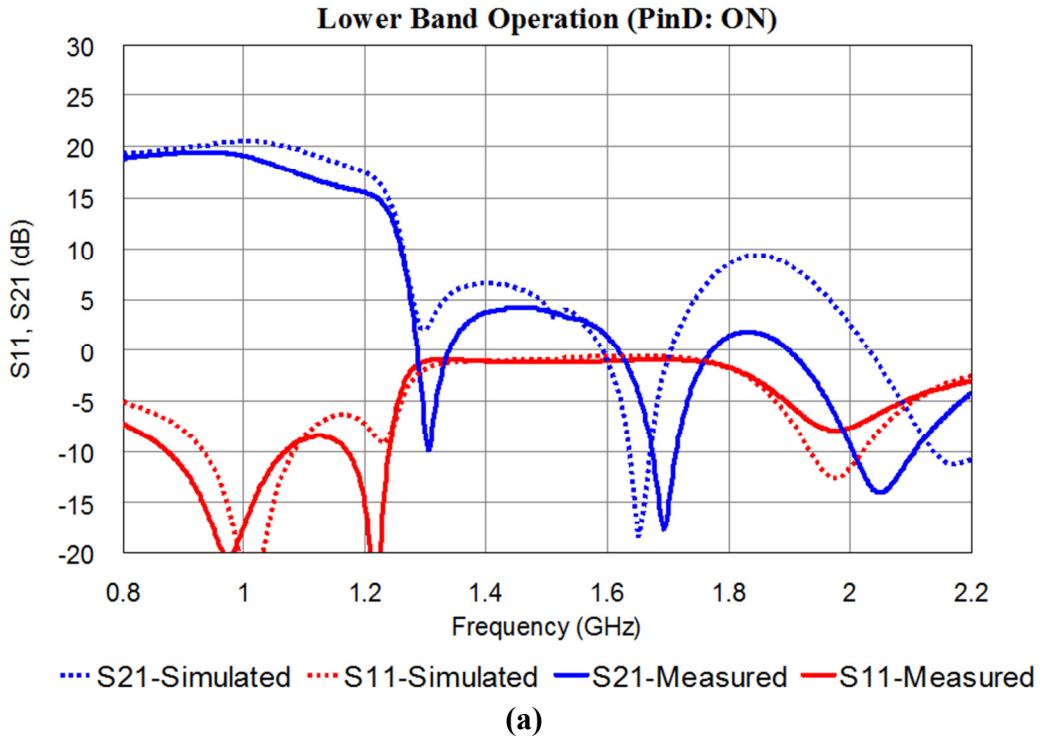


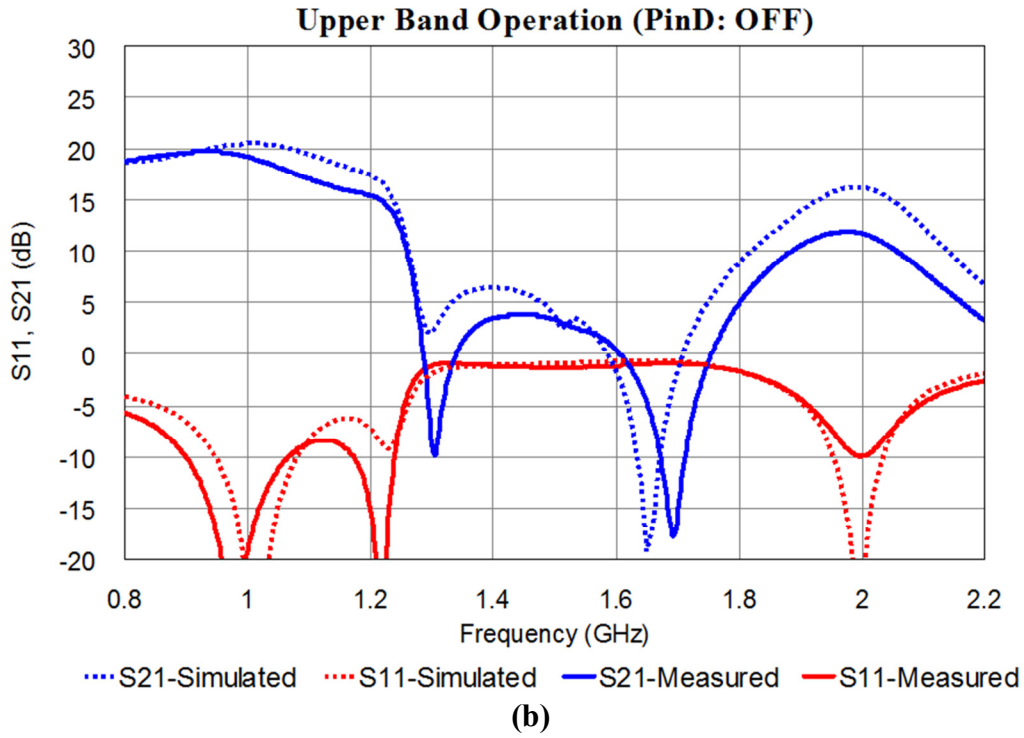
Figure 5.38 The picture of the revised power amplifier

In Figure 5.39, the simulated and the measured small signal parameters (S11 and S21) are plotted for ON and OFF states of the pin diode. It can be observed from the measurement results that the frequencies where S21 peaks and S11 dips closely follow the simulation results. Even though the measured gain at 2 GHz when pin diode is OFF is about 4 dB lower than the simulated gain, the form of the S21 plot around 2 GHz is very similar to the simulated S21.

After 1 GHz and 2 GHz bands are successfully verified by the small signal measurements, the large signal measurements are taken in the vicinity of 1 GHz and 2 GHz frequencies when pin diode is made ON and OFF respectively. Figure 5.40 shows the output power, DE and PAE measurement results according to the input frequency. The input power is held constant at +29 dBm and +34 dBm levels for ON and OFF states of the pin diode respectively, because of the small signal gain difference observed in the lower band and upper band frequencies. In addition, similar to the first implementation, upper band measurements are observed for both biasing the pin diode OFF and replacing the pin diode with ideal open condition. The frequencies, where DE and PAE peak, are very close to 1 GHz and 2 GHz as expected.

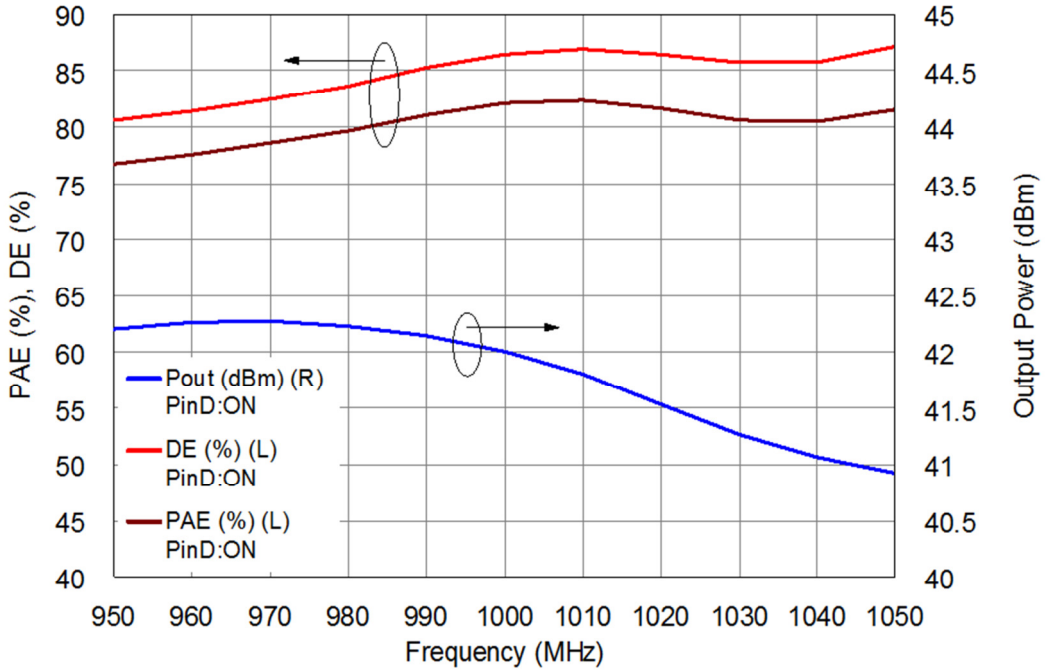


(a)

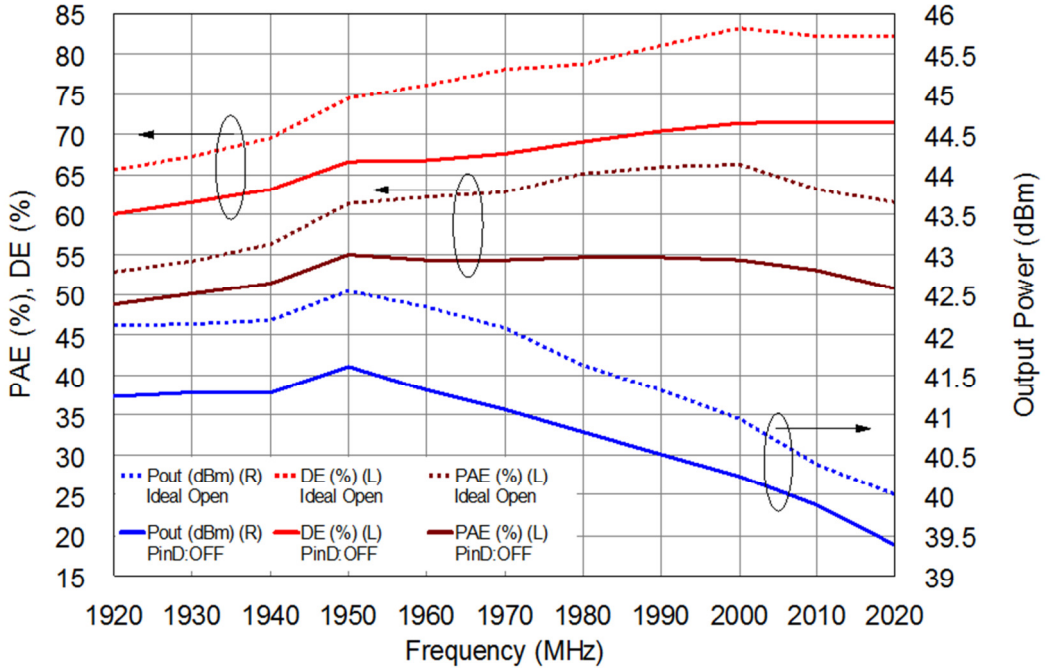


(b)

Figure 5.39 Comparison of the small signal measurements (solid) and simulations (dashed) of the revised PA (a) pin diode: ON (b) pin diode: OFF



(a)



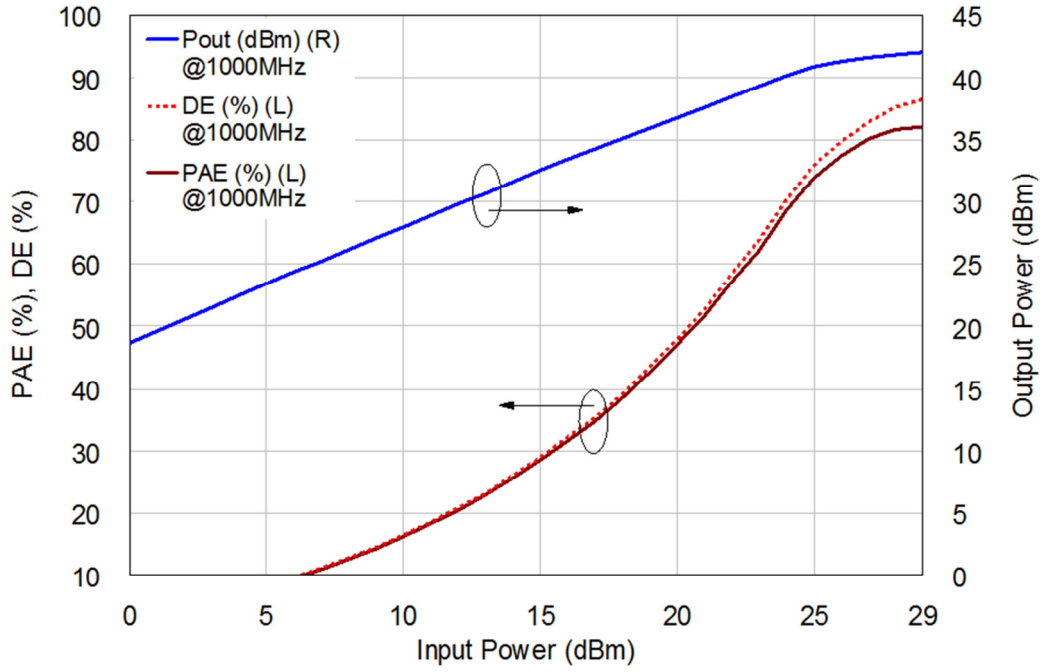
(b)

Figure 5.40 Large signal measurements of the revised PA

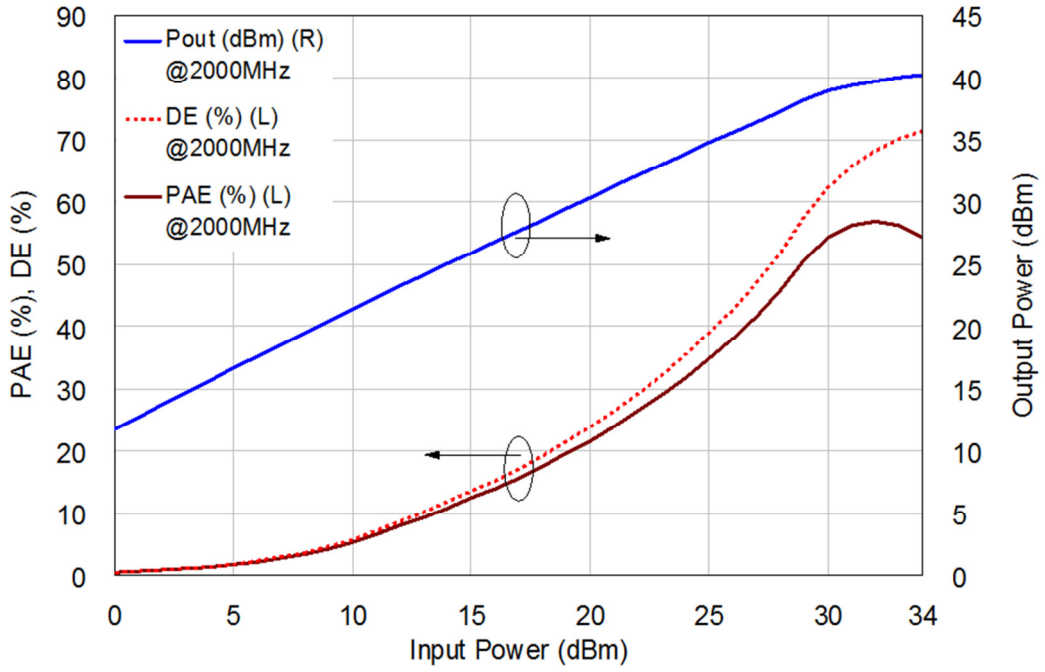
(a) pin diode: ON (b) pin diode: OFF

Figure 5.41 shows the output power, DE and PAE plotted for 1 GHz and 2 GHz when the input power is swept. Then, output power is measured as 42 dBm at 1 GHz with DE of 86.4% and PAE of 82% when the input power is +29 dBm. On the other hand, the measured output power is 40.2 dBm at +34 dBm of input power and DE and PAE are measured as 71.4% and 54.4%.

Figure 5.39 shows identical small signal performance at 1 GHz for both states of the pin diode. Then, the need for pin diode switching at lower band operation should be proven to show the advantage of the proposed tunable structure. For this purpose, output power, DE and PAE measurements at lower band (950-1050 MHz) are also taken for OFF state of the pin diode and compared with the ON state measurements as given in Figure 5.42. At 1 GHz, the output power drops about 0.5 dB when the pin diode is switched from ON to OFF state. More importantly, efficiency is enhanced by more than 20% when the pin diode is made ON. Lower band harmonic output also differs according to the state of the pin diode as Figure 5.43 states. At 1 GHz input frequency, the 2^{nd} (2 GHz) and the 3^{rd} (3 GHz) harmonic levels at the output are obtained as -9 dBc and -28 dBc respectively when the pin diode is OFF. When the pin diode state is switched to ON, the 2^{nd} and the 3^{rd} harmonic levels drop to -32 dBc and -34 dBc respectively. The improvement in the 2^{nd} harmonic level is more significant than the 3^{rd} harmonic level as expected; since, the function of the pin diode is mainly to tune the 2^{nd} harmonic at lower band operation.



(a)



(b)

Figure 5.41 Large signal measurements of the revised PA according to input power
(a) pin diode: ON & @ 1 GHz (b) pin diode: OFF & @ 2 GHz

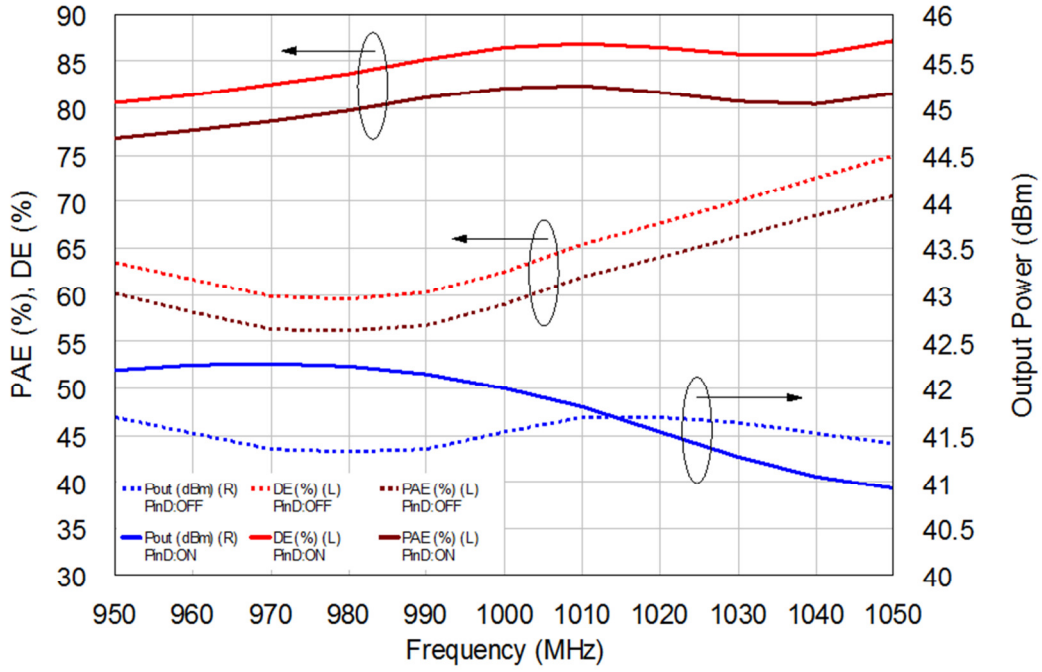


Figure 5.42 Comparison of the measured lower band performance of the revised PA dashed: pin diode: OFF, solid: pin diode: ON

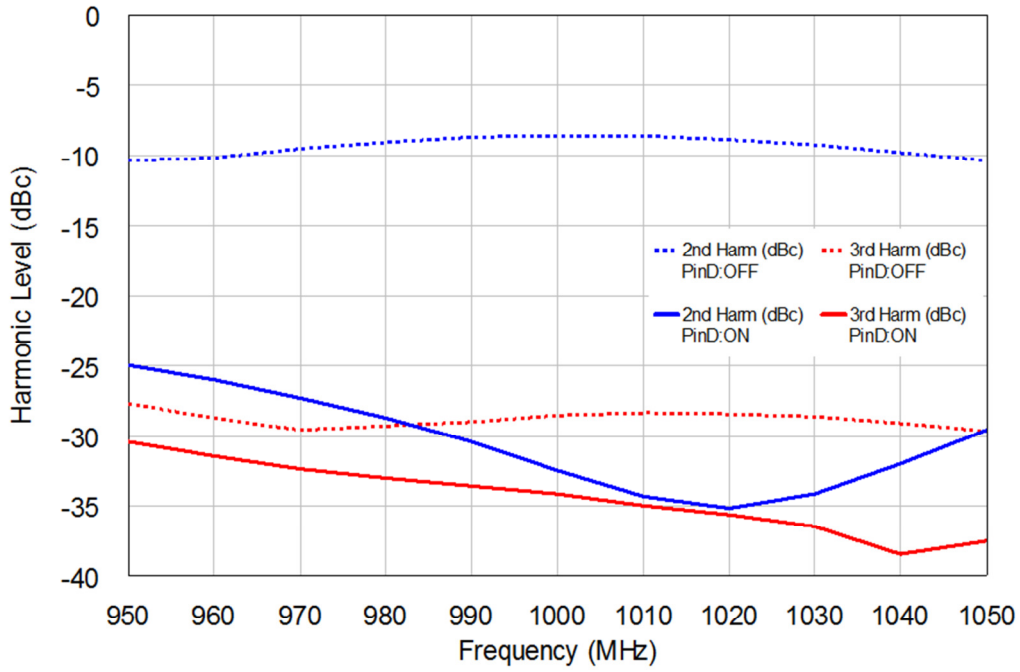


Figure 5.43 Comparison of the lower band harmonic measurements of the revised PA dashed: pin diode: OFF, solid: pin diode: ON

5.5 Summary and Conclusions

This chapter has presented the design steps of a high efficiency, tunable dual-band PA. Before starting the design, it is challenged to satisfy high efficiency for a dual band PA application where the upper frequency band is located at the 2nd harmonic of the lower band. Then, the operating bands are aimed as 1 GHz and 2 GHz initially. A tunable load matching circuit in the form of a triple stub topology is designed to fulfill the required fundamental and harmonic loads for both operating band frequencies. Moreover, a band-selective detection circuit integrated into the source matching circuit is proposed to be used for controlling the tunable load matching circuit according to the operation band.

The designed PA is implemented on a 0.5 mm thick RO4003C substrate. When the implemented PA is measured, the two frequency bands with the best large signal performances appear as 920 MHz and 1720 MHz. Then, the reasons for this deviation of the band frequencies from the aimed 1 GHz and 2 GHz frequencies are investigated in detail. After carrying out some reverse simulations, it is detected that the variations between the simulations and the measurements occur because of the degraded accuracy of the EM-based microstrip junction models used in the simulations. Then, a revised design is implemented by using the correct models for microstrip junctions in the simulations. The revised design satisfy the aimed band frequencies with good large signal performance. It is also shown by measurements that 2nd harmonic load tuning at 1 GHz results in more than 20% efficiency improvement thanks to the tunable PA structure.

In Table 5-8, the measured output power, DE and PAE performances of the two implemented PAs in this section are compared with the published results of some state-of-the-art dual band PAs. To the author's knowledge, the 1 GHz / 2 GHz PA is the only PA in the literature satisfying $f_2/f_1=2$ with more than 85% drain efficiency at lower band operation.

The PAs listed for comparison satisfy concurrent dual band operation while the implemented PAs are non-concurrent. However, the proposed self-tunable

structure easily makes the PA structure concurrent without any considerable degradation in the measured efficiencies.

Table 5-8 Performance comparison with state-of-the-art dual-band PAs

Ref.	f_1 & f_2 (MHz)	f_2/f_1	Pout (dBm)	DE/PAE (%)
[32]	800	1.56	40.6	- / 81.7
	1250		41.8	- / 80
[68]	800	2.38	46	68 / -
	1900		46	68 / -
[69]	685	2.69	41	76 / 71
	1840		41.9	61.3 / 52.7
[70]	1700	1.26	40.5	- / 78
	2140		39.8	- / 77.1
[71]	1900	1.37	41.1	80 / 74
	2600		40.8	72 / 66
This work-1 [73]	920	1.87	41.5	81.3 / 76.7
	1720		41	60.2 / 50.2
This work-2	1000	2	42	86.4 / 82
	2000		40.2	71.4 / 54.4

CHAPTER 6

CONCLUSIONS AND FUTURE WORK

High efficiency power amplifiers (PAs) are essential components for wireless communication systems to reduce the power usage of the wireless network. There are two basic approaches; namely, switch-mode and harmonic-tuned, for designing high efficiency PAs. Switch-mode PAs; such as, Class-D and Class-E PAs, operate the active device (transistor) as a switch to satisfy zero DC power consumption in theory. The non-ideal switching behavior of the transistor at high frequency operation makes it difficult to satisfy the ideal switching waveforms which results in efficiency degradation. Hence, switch-mode PAs are generally preferred in low frequency region where the transistor can be operated close to an ideal switch. Harmonic-tuned PAs, on the other hand, produce non-overlapping current and voltage waveforms at transistor drain by terminating harmonics with optimum impedances to satisfy zero DC power consumption in theory. Since, multi-harmonic terminations can be implemented by distributed transmission lines at high frequency, harmonic-tuned approach is the preferred design technique for high frequency, high efficiency PAs. Class-F and Inverse Class-F PAs are two fundamental examples of harmonic-tuned PAs. Besides, Continuous Class-F and Continuous Inverse Class-F PAs are devised for wideband applications.

Harmonic-tuned PAs require purely reactive harmonic terminations. Because of the practical reasons, the harmonics greater than the 3^{rd} degree are usually ignored during the design. Then, multi-harmonic matching networks are designed at the load side of the PA to satisfy optimum fundamental load for maximum power output and optimum reactive harmonic (2^{nd} and 3^{rd}) loads for maximum efficiency. Lumped element multi-harmonic networks are generally preferred at low frequency applications. On the other hand, distributed element multi-harmonic networks are preferred at high frequency applications.

In this study, the triple stub topology is investigated in terms of multi-harmonic matching in addition to fundamental matching which is readily known. In terms of multi-harmonic matching, the 2nd and the 3rd harmonics are considered only. Then, in order to have a complete analysis, at least 6 variables are required; since there are 3 real and 3 imaginary impedances to be solved at 3 different frequencies (fundamental, the 2nd and the 3rd harmonics). Two different modifications of the triple stub topology are handled with different fundamental and multi-harmonic load combinations. In the first modification, 3 additional stubs are added next to each stub existing in the conventional triple stub circuit. Then, the lengths of the 6 stubs are assigned as the variables. The analytical expressions for the impedances at the fundamental, the 2nd and the 3rd harmonics are obtained in terms of the 6 variables. Since, the obtained analytical expressions are complex and nonlinear, numerical optimization technique is used to solve the expressions. Predefined impedance points in the smith chart are used as the goals for the optimization process. The fundamental impedances are selected to be uniformly distributed inside the smith chart; while, the harmonic impedances are selected to be purely reactive lying on the outer circle of the smith chart. This specific case is applicable to harmonic-tuned PAs. The optimization results show that this circuit with three stub pairs can perform matching to any impedance at fundamental and any reactive impedance at the 2nd and the 3rd harmonics simultaneously by tuning the 6 stub lengths only. A second modification of the conventional triple stub circuit with one additional series transmission line is also analyzed. The lengths of the 3 stubs and the 3 series transmission line lengths are tuned for the analysis. Unlike to the first modification, the impedance goals for the optimization are chosen as uniformly distributed inside smith chart for the fundamental and the harmonics. Then, the optimization results show that the second modification is able to perform a complete multi-harmonic impedance matching without any restriction on the impedances to be matched.

A tunable, high efficiency, dual-band PA utilizing harmonic-tuned approach is designed and implemented in the scope of this study also. A specific dual-band application where the upper band is located at the 2nd harmonic of the lower band is

aimed. For this purpose, 1 GHz and 2 GHz frequencies are selected as the band frequencies. Then, the problem of 2nd harmonic load tuning at the lower band (1 GHz) arises; since, the load at 2 GHz is dictated by the output power optimized fundamental load at the upper band (2 GHz). In order to provide a solution to this specific problem, a tunable load matching circuit is proposed and implemented. The proposed circuit is a triple stub circuit with one of the stub lengths is tuned according to the operating band by the use of a pin diode. Then, two different forms of matching circuits can be obtained at 1 GHz and 2 GHz according to the state of the pin diode. By this way, it becomes possible to satisfy optimum fundamental and multi-harmonic loads at both operating bands. In the first implementation, the optimum frequency bands are measured as 920 MHz and 1720 MHz with drain efficiencies 81.3% and 60.2% respectively. After the reasons for the shift in the measured bands from the aimed 1 GHz and 2 GHz bands are detected, a second implementation is realized by correcting the simulation models. 86.4% and 71.4% drain efficiencies are measured at 1 GHz and 2 GHz respectively in the revised implementation. It is also verified by measurements that harmonic tuning at the lower band improves the efficiency by at least 20%.

The future works related to this study can be listed as follows;

Multi-harmonic analysis of triple stub topology performed in Chapter 4 can be extended. The fundamental and multi-harmonic impedances are already expressed in terms of the variables of transmission line lengths. A complete solution for the transmission line lengths in terms of the fundamental and multi-harmonic impedances can be investigated either analytically or numerically.

In addition to triple stub tuner, multiple-stub tuners can be analyzed in terms of multi-harmonic matching. For example, multi-harmonic analysis of a four-stub tuner can be studied by including the 4th harmonic to the analysis.

The implemented tunable dual-band PAs require external control voltages for the pin diode. The automatic control of the pin diode can be realized by using the detected signal at the input. The detected signal is an indication of the lower band signal applied to the input. Then, an RF detector can be used to transform the

detected RF signal to a TTL compatible DC control voltage. A pin diode driver controlled by a TTL voltage can be designed to produce positive and negative output voltages required to make pin diode ON and OFF respectively. As a result, with the inclusion of an RF detector and a pin diode driver, the PA can be made self-tunable which enables concurrent dual-band operation.

The proposed tunable structure can be applied to an octave bandwidth PA; such as, 1-2 GHz PA, to enhance the efficiency. The 2^{nd} harmonic tuning problem at lower band edge exists in an octave bandwidth PA also. The obtainable efficiency at the lower band edge is lower than the maximum achievable efficiency with a classical fixed load matching circuit. Then, the idea of using tunable load matching circuit can be applied for octave-band application similar to dual-band application. Instead of tuning only one stub in the triple stub circuit, tuning of all three stubs with the use of three pin diodes can be considered to satisfy the octave bandwidth operation.

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CURRICULUM VITAE

PERSONAL INFORMATION

Surname, Name: Kılıç, Hasan Hüseyin
Nationality: Turkish (TC)
Date and Place of Birth: 2 December 1986, Ankara
Marital Status: Married
Phone: +90 312 592 60 00 / 81534
email: kilichasanh@gmail.com

EDUCATION

Degree	Institution	Year of Graduation
MS	METU Electrical and Electronics Eng.	2011
BS	METU Electrical and Electronics Eng.	2009
High School	Süleyman Demirel Science High School, Isparta	2004

WORK EXPERIENCE

Year	Place	Enrollment
2009-Present	Aselsan	RF/Microwave Design Engineer

FOREIGN LANGUAGES

Advanced English

PUBLICATIONS

1. H. Kilic and S. Demir, "A highly efficienct dual-band GaN power amplifier utilizing pin diode based tunable harmonic load matching," in *IET Microwaves, Antennas & Propagation*, Aug. 2018, in press.