ANALYSIS AND EVALUATION OF HFO_2 BASED RESISTIVE RAM DEVICES FOR NEW GENERATION NON-VOLATILE MEMORIES

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ANALYSIS AND EVALUATION OF HFO_2 BASED RESISTIVE RAM DEVICES FOR NEW GENERATION NON-VOLATILE MEMORIES

submitted by **SERDAR BURHAN TEKİN** in partial fulfillment of the requirements for the degree of **Master of Science** in **Micro and Nanotechnology, Middle East Technical University** by**,**

Prof. Dr. Halil Kalıpçılar _____
Dean, Graduate School of **Natural and Applied Sciences**

Prof. Dr. Burcu Akata Kurç _____
Head of Department, **Micro and Nanotechnology**

Assoc. Prof. Dr. Alpan Bek _____
Supervisor, **Physics Dept., METU**

Assoc. Prof. Dr. Şeref Kalem _____
Co-supervisor, **BİLGEM, TÜBİTAK**

Examining Committee Members:

Assist. Prof. Dr. Saffettin Yıldırım _____
Physics Dept., İstanbul University

Assoc. Prof. Dr. Alpan Bek _____
Physics Dept., METU

Assoc. Prof. Dr. İsmail Rafatov _____
Physics Dept., METU

Assoc. Prof. Dr. Serhat Çakır _____
Physics Dept., METU

Assist. Prof. Dr. Emre Yüce _____
Physics Dept., METU

Date: *10.08.2018*

I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

Name, Last Name: SERDAR BURHAN TEKİN

Signature:

ABSTRACT

ANALYSIS AND EVALUATION OF HFO_2 BASED RESISTIVE RAM DEVICES FOR NEW GENERATION NON-VOLATILE MEMORIES

Tekin, Serdar Burhan
M.Sc. in Micro and Nanotechnology
Supervisor: Assoc. Prof. Dr. Alpan Bek
Co-supervisor: Assoc. Prof. Dr. Şeref Kalem

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The objective of this thesis is to investigate the most suitable embedded non-volatile memory (eNVM) cell for the 28 nm and below CMOS technology. HfO_2 based resistive RAM (RRAM) memories are one of the most important candidates for new generation eNVMs due to their compatibility, reliability, low power consumption and high speed operation. In the scope of this thesis, several HfO_2 based memory stacks were built and characterized by optical and electrical characterization methods. Raman and X-Ray diffraction (XRD) measurements were conducted for investigating the structural properties and effects of crystallinity on the oxide material. By these measurements, the difference between crystalline and amorphous HfO_2 was observed. Also, the monoclinic and tetragonal phases of multi-crystalline HfO_2 were determined. Temperature dependent dielectric permittivity measurements were performed on both samples. Amorphous HfO_2 showed a greater temperature dependence compared to crystalline one. After that, 50 nm Ti metal was deposited on both crystalline and amorphous HfO_2 coated wafers at different sizes as top electrode

by thermal evaporation and 100 nm Al metal was coated on the back side of p-Si by the same way as bottom electrical contact. Therefore, capacitance-voltage (C-V) measurements were performed on these fabricated HfO_2 based MOS devices. According to the results, dielectric constant of crystalline HfO_2 based device is greater than the amorphous HfO_2 based one. Then, 10 nm HfO_2 based 1R resistive RAM (RRAM) devices having different metal electrode structures were examined by quasi-static current-voltage (I-V) measurements. Switching mechanisms of each type of memory stack were compared and the most efficient memory types were determined among these structures. According to the experiments, atomic layer deposited TiN and TiWN bottom electrodes are very promising in terms of reliability and power consumption. Finally, a packed crystalline HfO_2 based 4K-1T1R RRAM device was electrically characterized by an FPGA based I-V measurement platform. According to the results, the device can be a suitable candidate for implementing security devices such as physical unclonable functions (PUFs) and random number generators (RNGs).

Keywords: Resistive RAM, RRAM, ReRAM, OxRAM, HfO_2, resistive switching, non-volatile memory, MOS, capacitance, high-k dielectric

ÖZ

YENİ NESİL UÇUCU OLMAYAN BELLEKLER İÇİN HFO_2 TABANLI REZİSTİF RAM AYGITLARININ ANALİZ VE DEĞERLENDİRMESİ

Tekin, Serdar Burhan
Yüksek Lisans, Mikro ve Nanoteknoloji
Tez Yöneticisi: Doç. Dr. Alpan Bek
Ortak Tez Yöneticisi: Doç. Dr. Şeref Kalem

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Bu tezin amacı, 28 nm ve CMOS teknolojisi için en uygun, gömülü uçucu olmayan bellek (eNVM) hücresini araştırmaktır. HfO_2 tabanlı rezistif RAM (RRAM) bellekleri; uyumluluk, güvenilirlik, düşük güç tüketimi ve yüksek hızlarda çalışabilmelerinden dolayı yeni nesil eNVM'ler için en önemli adaylardan biridir. Bu tez kapsamında, çeşitli HfO_2 tabanlı bellekler oluşturulmuş olup, optik ve elektriksel ölçüm yöntemleri ile karakterize edilmiştir. Yapısal özelliklerin ve oksit materyalin kristalinitesinin etkilerinin araştırılması için Raman ve XRD ölçümleri yapılmıştır. Bu ölçümlerle, kristal ve amorf HfO_2 arasındaki fark gözlemlenmiş olup, çok kristalli HfO_2'nin monoklinik ve tetragonal fazları belirlenmiştir. Daha sonra, her iki örnekte de sıcaklığa bağlı dielektrik permitivite ölçümleri yapılmıştır. Amorf HfO_2, kristal yapıdakine kıyasla daha yüksek sıcaklık bağımlılığı göstermiştir. Daha sonra, 50 nm Ti metali, hem kristal hem de amorf HfO_2 kaplı örnekler üzerine termal buharlaştırma yöntemi ile farklı boyutlarda kaplanmış olup, 100 nm Al metali ise alt elektriksel kontak olarak p-Si tabakasının arka yüzeyine

aynı yöntem ile kaplanmıştır. Böylelikle, kapasitans-voltaj (C-V) ölçümleri bu fabrikasyonu yapılmış MOS cihazları üzerinde gerçekleştirilmiştir. Elde edilen sonuçlara göre, kristal yapıdaki HfO_2'nin dielektrik sabitinin amorf yapıdaki HfO_2'ye göre daha fazla olduğu gözlemlenmiştir. Daha sonra, farklı metal elektrod yapılarına sahip 10 nm HfO_2 tabanlı 1R rezistif RAM (RRAM) cihazları, yarı-statik akım-voltaj (I-V) ölçümleri ile incelenmiştir. Her tip bellek yapısının anahtarlama mekanizmaları karşılaştırılmış olup, bu yapılar arasında en verimli bellek tipi belirlenmiştir. Deneylere göre, atomik katman kaplama yöntemi ile üretilmiş, TiN ve TiWN alt elektrod yapısına sahip bellekler güvenilirlik ve güç tiketimi açısından çok ümit vadedicidir. Son olarak, kristal HfO_2 tabanlı, paketlenmiş 4K-1T1R RRAM cihazının, FPGA tabanlı I-V ölçüm platformu kullanılarak elektriksel karakterizasyonu yapılmıştır. Ölçüm sonuçlarına göre cihaz, fiziksel klonlanamaz fonksiyonlar (PUF) ve rastgele sayı üreteci (RNG) gibi güvenlik cihazlarının uygulamalarında kullanılmak için uygun bir aday olabilir.

Anahtar kelimeler: Rezistif RAM, RRAM, ReRAM, OxRAM, HfO_2, rezistif anahtarlama, uçucu olmayan bellek, MOS, kapasitans, yüksek sabitli dielektrik

To my family

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CHAPTER 1

INTRODUCTION

Developments in semiconductor memory technology and its application fields increase the requirements of devices having lower power consumption, higher density, higher speed, better reliability and scalability [1]. There is almost no electronic device that does not use a memory unit. In Figure 1.1, the various application fields of memory technologies are summarized. No such application can be performed without a physical memory.

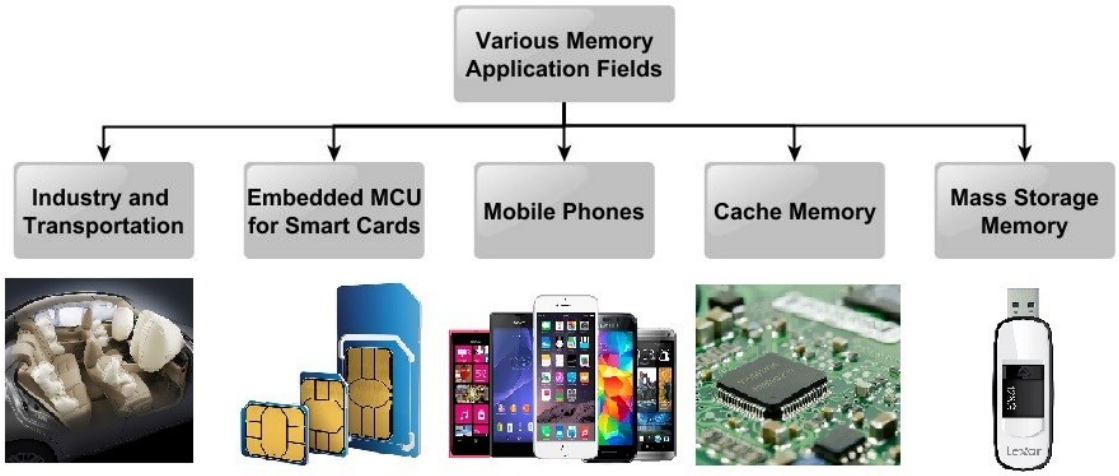

Figure 1.1: Memory application fields.

Currently used Flash memory is developing in line with these requirements. According to International Technology Roadmap for Semiconductors (ITRS) it is already scaled down to 16 nm but it was started to face with various challenges for smaller technologies such as 10 nm and below nodes [2,3].

Motivation of this thesis is to explore an efficient embedded non-volatile memory (eNVM) cell for the 28 nm and below CMOS technology. The results obtained in this thesis are aimed to contribute the investigation of the optimum dielectric material and metal electrode combinations for new generation eNVMs. In Figure 1.2, market growth of emerging non-volatile memories are shown. There is a clear exponential growth between the years of 2012 and 2018 [4]. This marketing trend indicates the importance of research on new generation non-volatile memory technologies.

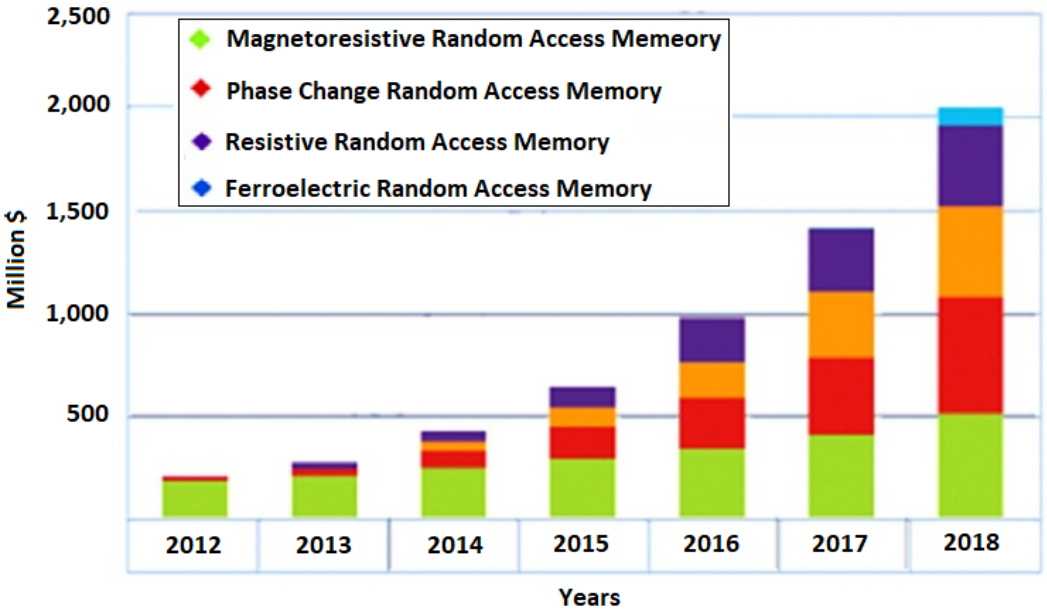

Figure 1.2: Market growth of emerging non-volatile memory technologies. Adopted from [4].

In 1967, floating gate (FG) structure was suggested to be used as a non-volatile memory element by D. Kahng and S. M. Sze at Bell laboratories [4]. Since that time, semiconductor memory is a fundamental part of modern electronic systems. In the same year, first study about using resistance switching as a memory operation was realized [5]. An Al/SiO_x/Au structure was used for exploring resistance switching and a fast switching operation was observed. However, it was thought that the formation and rupture of a conductive filament through the SiO_x layer was because of an electronic

effect instead of resistance switching of the material. After this study, research on non-volatile memories have been conducted for years but the first practical application on resistive random access memory (RRAM) was recorded on 2002. Zhuang et al. fabricated a 1T1R RRAM array based on 0.5 μm CMOS technology [6]. In 2004, a binary transition metal oxide based RRAM was fabricated by Samsung Advanced Institute of Technology in Korea [7]. It is known for about a half decade that the use of semiconductor memory devices having floating gate structure increased greatly and they were scaled down while developing to have higher operation speeds, higher densities and lower costs. However, for the technologies below 2X nm, it was understood that scaling down the same technology will not be useful because of the floating gate structure. Therefore, the popularity of novel RRAM devices increased in recent years and it became one of the important candidates for future non-volatile memories having sub-2X nm technology nodes [8].

Organization of this thesis is as follows. In Chapter 2, background information about memory technologies including volatile and non-volatile memories are given. Then, the structure and working principle of currently used Flash memory technology are explained. Consequently, the scaling problems and limitations of Flash memory are given. After that, a few emerging non-volatile memories are described briefly and then our focus on RRAM and its working principles are explained. In Chapter 3, before investigating the complex device architectures, two different atomic layer deposited (ALD) 50 nm amorphous and crystalline HfO_2 layers on p-type Si wafer were characterized by optical and temperature dependent electrical measurements and their results are given. In Chapter 4, metal oxide semiconductor (MOS) devices were built by metal depositions on those crystalline and amorphous HfO_2 coated wafers and C-V measurements were performed in order to analyze the HfO_2 properties of the samples. In Chapter 5, advanced RRAM devices having metal insulator metal (MIM) structures were electrically characterized by I-V measurements and the results are summarized. Finally, in Chapter 6, again the studies on electrical characterization of a packed RRAM memory device having 4000 cell arrays, 1 transistor 1 resistor (1T1R) structure are explained.

CHAPTER 2

A REVIEW ON MEMORY TECHNOLGY

2.1 General Background

In today's electronic devices and computing systems, memory is accepted as the main component. Basically, there are two types of memories, namely, volatile and non-volatile memories. Volatility is the ability to store data which has been written inside the memory as bits. Volatile memories need a continuous power supply in order to store the written data. Otherwise, all the stored data is erased immediately. On the other hand, non-volatile memories can store data for a long time (for years) without any power supply [9]. In Figure 2.1, various volatile and non-volatile memory devices are shown schematically.

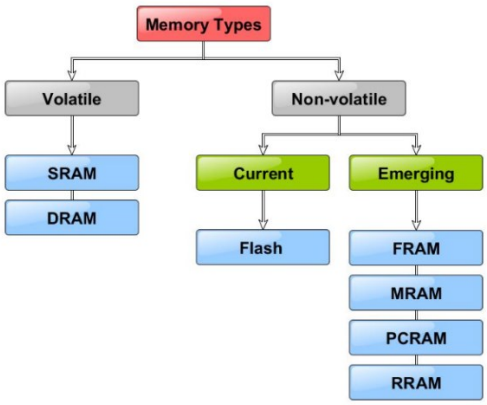

Figure 2.1: Memory classification. SRAM: Static Random Access Memory, DRAM: Dynamic Random Access Memory, FRAM: Ferroelectric Random Access Memory, MRAM: Magnetoresistive Random Access Memory, PCRAM: Phase Change Random Access Memory, RRAM: Resistive Random Access Memory.

2.2 Volatile Memory Technology

Random Access Memory (RAM) is a semiconductor memory. In RAM, each location in the memory space has a unique address and they are accessed in a fixed time. The read and write cycles are random that they can be in any order as desired [9].

Static Random Access Memory (SRAM) and Dynamic Random Access Memory (DRAM) are the main volatile memories. SRAM is composed of 6 transistors (6T). The structure of SRAM is shown in Figure 2.2.

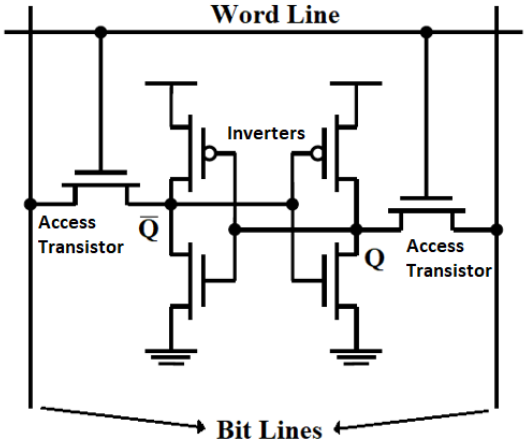

Figure 2.2: SRAM cell structure. Adopted from [10].

There are two cross-coupled inverters used for data storage like a flip-flop circuit. They store data as logic 1 (On state) and Logic 0 (Off state). Q and $\overline{Q}$ are the binary signals in the storage cells and they are the inverse of each other. Two access transistors transfer the binary signals to the word line (WL) and bit lines (BLs). SRAM provides really fast write and erase operations in order of a few nanoseconds and has a good endurance (capacity of write/read/erase cycle of a memory), greater than 10^{16} cycles [4,9].

DRAM has a 1 transistor one capacitor (1T1C) cell structure connected to WL and BL. The structure of DRAM is shown in Figure 2.3. Logic 1 and Logic 0 operations are

carried out by charging and discharging the capacitor. Since it only needs two components, its construction is easier and cheaper than SRAM. Its endurance value is also as high as SRAM ($>10^{16}$). It has a low retention (amount of time store the data which determines the volatility) value because of the leakage currents in the capacitor [4,9].

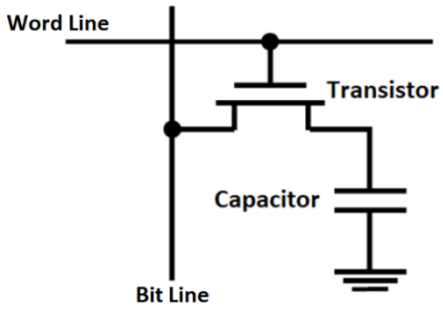

Figure 2.3: DRAM cell structure. Adopted from [9].

2.3 Non-Volatile Memory Technology

In contrast to volatile memories, non-volatile memories can keep the data for a long time (order of years) even without any power supply. This feature makes it attractive in many application fields such as industry, transportation, consumer electronics, mass memory storage and embedded systems [4]. The most popular and widely used non-volatile memory is Flash memory.

As shown in the Figure 2.4, storage element of the Flash memory is a 1 transistor (1T) structure together with a floating gate (FG) layer which is an oxide layer above the source and drain, below the gate of the transistor. Flash memory has a charge trapping mechanism where the electrons are trapped inside the FG layer [4,11].

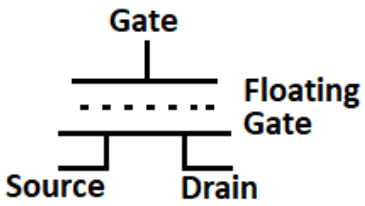

Figure 2.4: Schematic view of 1T floating gate (FG) structure.

2.3.1 Structure and Working Principles of Flash Memory

Flash memory structure is composed of a metal oxide semiconductor (MOS) transistor and a FG layer which is placed between the channel and the control gate (CG) of the transistor as shown in Figure 2.5. The FG layer is electrically isolated from the channel and the CG by oxide layers [9,12].

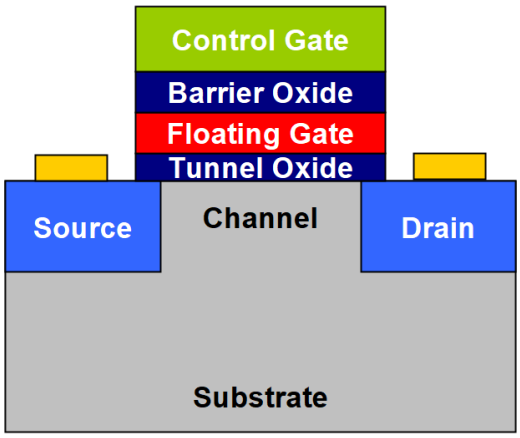

Figure 2.5: Flash memory 1T FG structure.

Application of a positive potential to the CG causes electrons to pass through the tunnel oxide layer and trapped into the FG. Storing electrons in the FG increases the threshold voltage of the transistor and this corresponds to programming operation. In order to erase the data, a negative voltage is applied to the CG, so that the stored electrons travel back from the FG to the substrate through the tunnel oxide. This phenomena is explained

by Fowler-Nordheim (FN) tunneling [10,12]. The change in the threshold voltage is calculated as follows,

$$\Delta V_T = V_T - V_{T0} = \frac{-\overline{Q}}{C_{FC}}$$

where V_T and V_{TO} are the threshold voltages of the Flash memory with and without charges in the FG, respectively. $\overline{Q}$ is the stored charge with respect to its position in the gate oxide and C_{FC} is the capacitance between the CG and the FG [13].

Besides the programming and erase, there is also read operation. A voltage bias between the thresholds voltages of the programming and erase operations is applied to the CG, a read voltage is applied to the drain and the source terminal is grounded at the same time for the read operation [10]. These operations are shown in Figure 2.6.

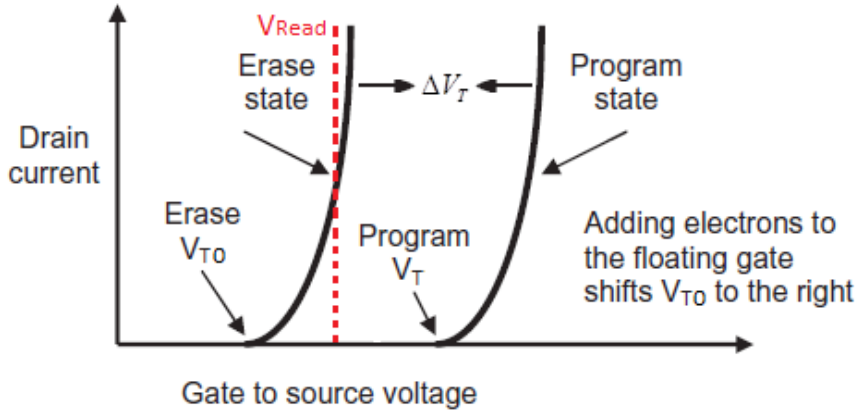

Figure 2.6: Current-Voltage characteristics of Flash memory. Adopted from [11].

There are two major types of Flash memory having different cell structures. These are NOR Flash and NAND Flash as shown in Figure 2.7.

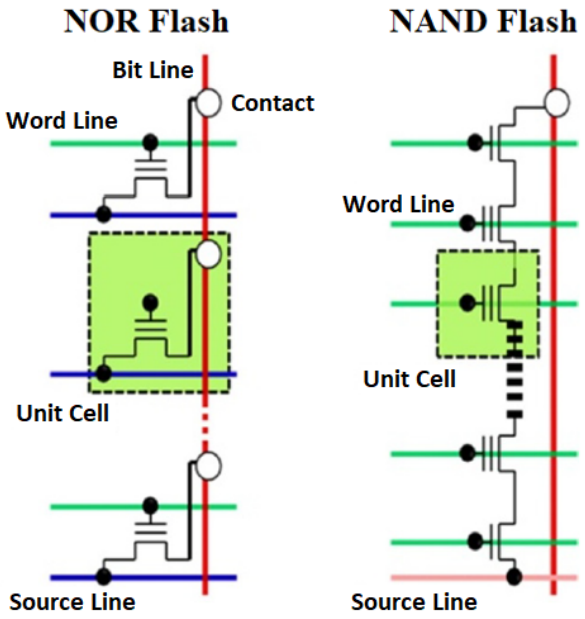

Figure 2.7: NOR Flash and NAND Flash cell array combinations. Adopted from [4].

The transistors of NOR Flash cell are connected in parallel to the bit line (BL), while in NAND Flash they are connected in series. The parallel connection in NOR Flash allows reading and programming of the cells individually. This feature of NOR Flash makes it suitable for code storage in embedded systems. Series combination of NAND Flash is advantageous in terms of space consumption. It occupies less space than NOR Flash. This reduces the cost of manufacturing and increases the density. Therefore, NAND Flash is useful for the storage of large files such as videos and audios. They are also useful for SD cards, USB drivers and MMC cards [4,12]. The properties, advantages and disadvantages of NOR and NAND Flash memories are summarized and compared in Table 2.1. The information written in the table was retrieved from [4].

Table 2.1: Features of NOR and NAND Flash memories.

Features	NOR	NAND
Memory size	≤ 512 Mbit	1 to 8 Gbit
Sector size	Approximately 1 Mbit	Approximately 1 Mbit
Program time	9 µs/word	400 µs/page
Erase time	1 s/sector	1 ms/sector
Read access time	< 80 ns	20 µs
Write parallelism	8 to 16 words	2 Kbyte
Output parallelism	Byte/word/dword	Byte/word
Read parallelism	8 to 16 words	2 Kbyte
Access method	Random	Sequential
Price	High	Very Low
Reliability	Standard	Low

2.3.2 Scaling and Limitations of Flash Memory

Requirement of devices having lower power consumption, higher density, higher speed, better reliability and scalability was increased with the increasing developments in semiconductor memory technology and its application fields [1]. Tunnel oxide thickness is one of the issues for scaling Flash memory because undesired capacitive coupling and leakage currents occur together with reduced oxide layer thickness. These factors negatively affect the device performance, and reliability. Another factor is that, scaling down reduces the device density to store electrons which limits the data storage. In addition to these, the operation voltage of Flash memory is relatively high (more than 10.0 V) for low power operations [3,4]. There are still ongoing efforts to improve Flash memory for solving these problems such as different lithography techniques and 3D Flash architectures but these methods are cost effective and technically not feasible [2]. For this purposes, new generation non-volatile memories having different structures and working mechanisms have started to investigate as alternative to Flash memory. In the next section, the structures, types and operating mechanisms of these memories are explained in detail.

2.4 Emerging Non-Volatile Memories

Since it is uncertain whether Flash memory in the future will meet the requirements of scalability, low power consumption, high speed, high density, reliability, high retention, high endurance and low cost, research has focused on new generation two terminal memory structures. Ferroelectric Resistive Random Access Memory (FRAM), Magnetoresistive Random Access Memory (MRAM), Phase Change Random Access Memory (PCRAM) or Phase Change Memory (PCM) and Resistive Random Access Memory (RRAM) are the most important candidates for new generation non-volatile memories [1,4,14].

2.4.1 Ferroelectric Random Access Memory (FRAM)

Ferroelectric random access memory (FRAM) is one of the non-volatile memory types introduced as an alternative to Flash memory. Two different materials are used for this memory type. These are perovskite and layered structures. $PbZr_xTi_{1-x}O_3$ (lead zirconate titanate or PZT) is the widely used perovskite material for FRAM. $Sr_{1-y}Bi_{2+x}Ta_2O_9$ (strontium bismuth tantalate or SBT) and $Bi_{4-x}La_xTi_3O_{12}$ (lanthanum substituted bismuth titanate or BLT) are the two choices of layered materials [14,15].

FRAM has two different cell structures namely transistor-capacitor type (1T1C) FRAM and FET type (1T) FRAM as shown in Figure 2.8a. 1T1C type is similar to DRAM in terms of cell structure. Unlike DRAM, the cell is also connected to Plate Line (PL) along with the WL and BL. This type has very low operation voltage and very good performance in terms of endurance and programming speed but it has a large cell size which is a disadvantage for high density applications. On the other hand, the 1T type has a small cell structure, good endurance and it is suitable for high density applications. However, since it has a complicated structure, its fabrication and integration to CMOS technology is challenging [14,15].

Application of an electric field to a ferroelectric material can polarize the material and the dipoles align towards the electric field direction. When the electric field is removed, the dipoles keep their polarization states. The required voltage for polarization is between 1.5 V and 3.0 V for layers having thicknesses range from 70 nm to 100 nm [14]. This polarization property is used as the memory element. In Figure 2.8b, the hysteresis curve which shows the dependence of polarization to the electric field of the ferroelectric material is shown [4,16].

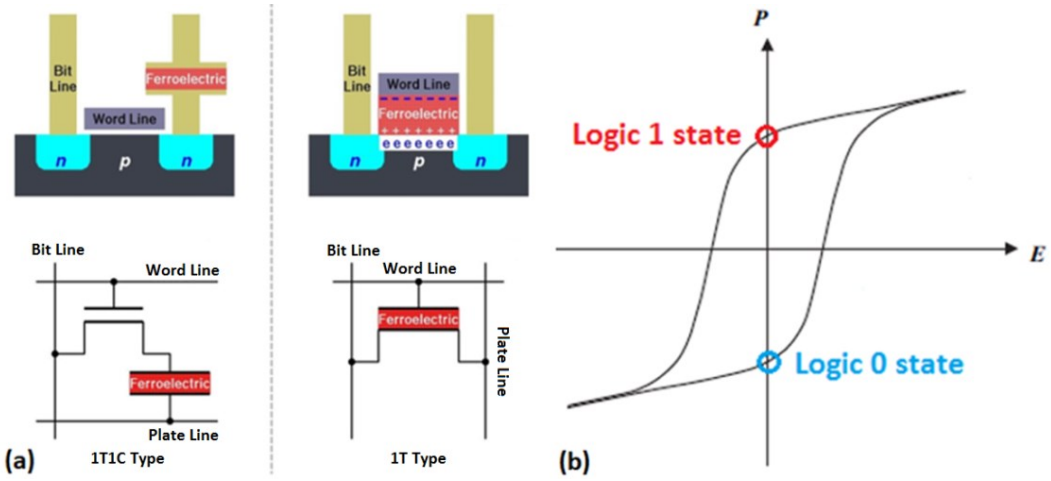

Figure 2.8: (a) Two different cell structures of FRAM (b) hysteresis curve of FRAM. Adopted from [4,17].

2.4.2 Magnetoresistive Random Access Memory (MRAM)

Magnetoresistive random access memory (MRAM) is a non-volatile memory which uses magnetic charges (magnetic tunneling junction or MJT) to store data. It has two ferromagnetic plates as the magnetic storage element, one having fixed magnetic polarity namely pinned layer (reference layer). The polarity of the other one can be switched and it is called free layer. These plates are separated by a thin insulating layer named as tunnel barrier [4,16]. The MRAM architecture composed of a transistor and a MJT is shown in Figure 2.9a.

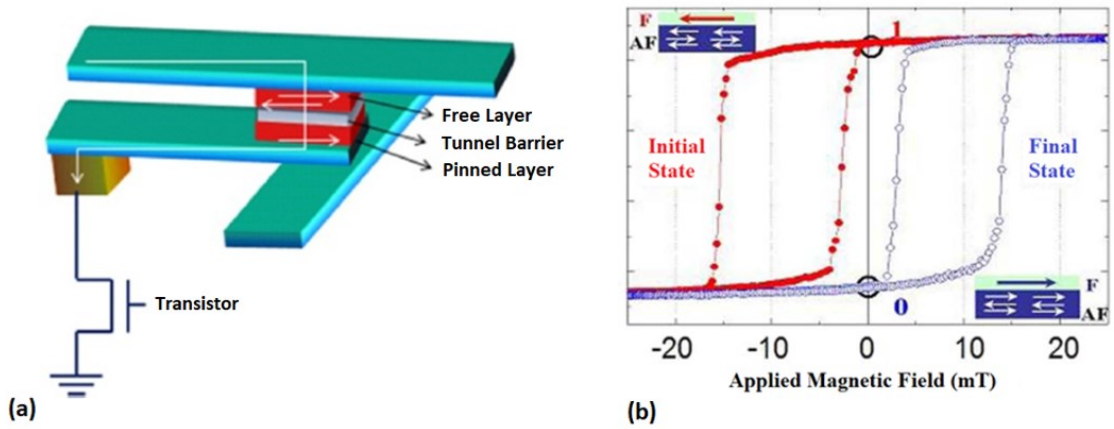

Figure 2.9 (a) MRAM cell architecture (b) hysteresis curve of MRAM. Adopted from [4,18].

When the magnetic polarity of the free layer and the pinned layer is the same, it corresponds to Logic 1 state. If the polarity of the free layer is changed to be the opposite of the pinned layer, resistance increases and the device switches to Logic 0 state [4,18]. The shift of the hysteresis loop between the Logic 1 and Logic 0 states during switching is shown in Figure 2.9b. MRAM is a really fast and scalable memory device with high endurance. Therefore, it can be used in many application fields such as networking, data storage and industrial controls. It still has challenges like the need of high write voltage. Research is still under way to develop MRAM and eliminate its deficiencies [14,18].

2.4.3 Phase Change Random Access Memory (PCRAM)

The memory environment in the phase change RAM (PCRAM), in other words phase change memory (PCM), is a chalcogenide alloy of materials from IV, V and VI groups which has two different phases, amorphous and crystalline [4]. Chalcogenide materials are also used in rewritable disks, CDs and DVDs. Germanium (Ge), Antimony (Sb) and Tellurium (Te) are the most promising materials for the chalcogenide alloy for PCRAM and they are shortly known as GST [19]. Phase change name is coming from the high resistance difference between the crystalline and the amorphous phases of the

chalcogenide material. Crystalline phase is equal to low resistive state (LRS or Logic 1) while the amorphous phase is equal to high resistive state (HRS or Logic 0) [12].

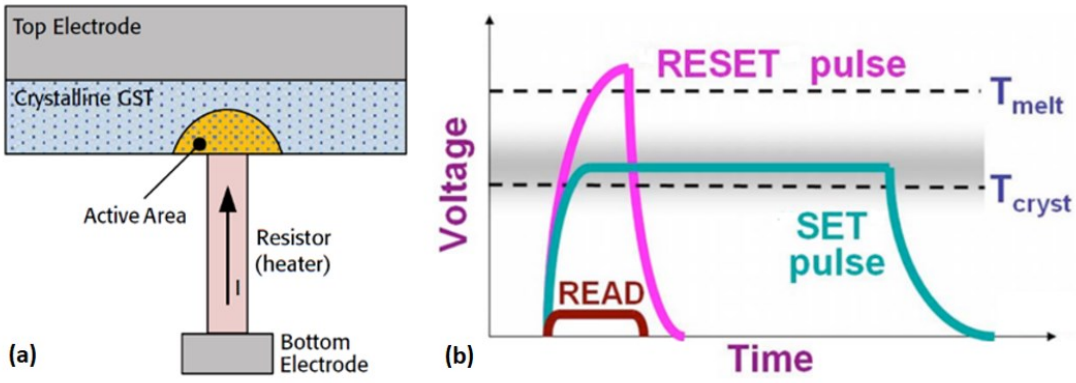

Figure 2.10 (a) PCRAM device structure (b) programming operations. Adopted from [19,20].

In Figure 2.10, device structure and programming operations by the application of electrical pulses are shown. The write and erase operations are realized by switching the device between these two resistive states. Consider the device is at HRS initially. In order to set the device to LRS, a Set pulse is applied to the resistor until the active area is sufficiently heated and exceeded the crystallization temperature (T_{cryst}). Then, to reset the device back to HRS, higher current than that of the Set operation is applied to the resistor and melts the center of the cell. If the applied voltage is cut off suddenly right after exceeding the melting temperature (T_{melt}), it quenches the active region into the amorphous phase having high resistance [12,20]. PCRAM has high endurance, scalability beyond 22 nm technology node and fast operation speeds but it still has problems such as reliability and the requirement of high Reset voltage to switch. Although there are such issues, it is one of the promising candidates for future non-volatile memory market [12,20].

2.4.4 Resistive Random Access Memory (RRAM)

Among the emerging technologies, RRAM is a very important candidate for future non-volatile memories and it is the focus of this thesis. Its important feature is compatibility with CMOS technology. Generally, it has a metal-insulator-metal (MIM) structure where a highly resistive material (typically a metal oxide) as the active layer is sandwiched between two metal electrodes namely top electrode (TE) and bottom electrode (BE) [21]. A simple schematic structure of RRAM is shown in Figure 2.11.

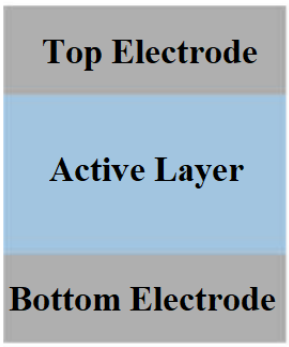

Figure 2.11: RRAM structure.

As implied by its name, data storage in this memory type is accomplished by resistive switching operation between the high resistive state (HRS) and low resistive state (LRS) of the active medium. Material selection for both the active layer and the metal electrodes are very important to perform a good switching operation [22].

Switching operation of RRAM is composed of three steps. These are “Forming” step (formation of a conductive filament inside the dielectric material), “Reset” step (rupture of the conductive filament) and “Set” step (reformation of the conductive filament), respectively [23]. These three steps are shown in Figure 2.12. The first and the most important step for a good switching operation is the Forming step. It is carried out by applying a voltage pulse to the TE while grounding the BE. In this step, a soft breakdown occurs inside the initially insulating oxide layer.

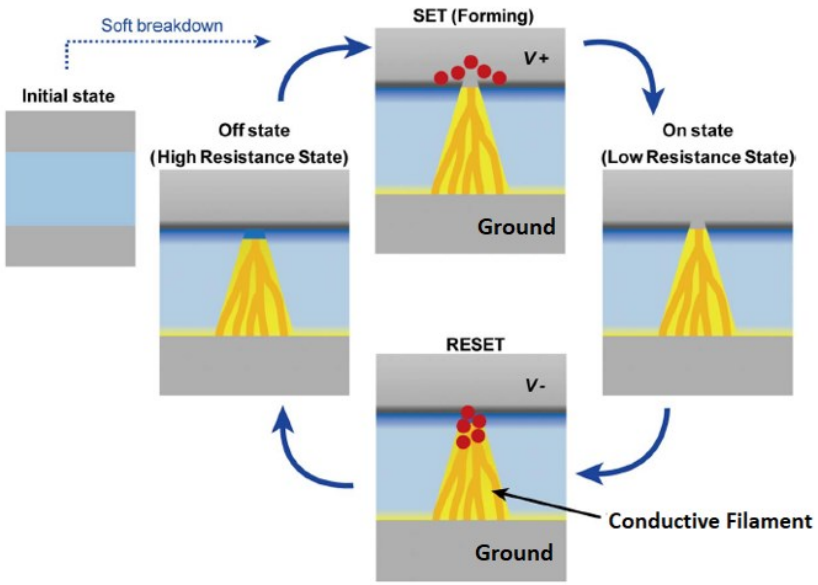

Figure 2.12: RRAM cell structure and switching operation steps. Adopted from [12].

Therefore, a conductive filament forms between the top and bottom electrodes. The device switches to LRS by this way. A compliance current (CC) is applied during this process in order to prevent the oxide layer from a hard breakdown [24]. Conductive filament formation is explained by oxygen ion diffusion from the metal electrode and the ion migration through the oxide region triggered by the applied electric field [25].

The second step is the Reset step. This process is the reverse of the Forming, where previously formed conductive filament is partially ruptured and the oxide layer in the conductive phase switches back to the HRS. The third step is the Set step. In this step, a new conductive channel is created from the partially ruptured conductive filament and the device switches to LRS [26]. This step is the same as the Forming step. The only difference between these two steps is the amplitude of the applied voltage. In the Forming step, larger voltage values are needed to create the conductive filament. Once it is formed, it does not break down completely. Therefore, the voltage needed for a Set step is smaller than the voltage needed for a Forming step and the resistance of the HRS after the Reset step is smaller than the resistance of the initial (pristine) state before the Forming state [26,27].

There are two different types of switching modes in order to operate the resistive switching mechanism as shown in Figure 2.13. These are unipolar and bipolar modes. In unipolar switching, the polarity of the voltage needed to create or rupture the conductive filament is the same. This means that both Set and Reset voltages have the same polarity and the switching operation depends on the amplitude of the voltage pulse [22].

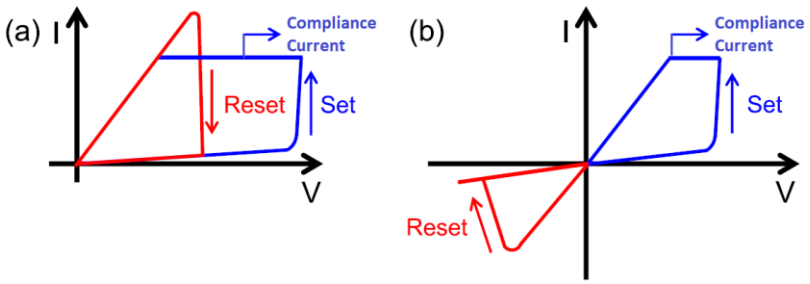

Figure 2.13: Operation modes of (a) unipolar, (b) bipolar resistive switching. Adopted from [27].

The Reset and Set processes in unipolar switching is explained by thermal acceleration of redox transitions and chemical reduction of the metal oxide at high temperatures, respectively. In bipolar switching, the Reset and Set voltages have reverse polarity and the switching operation is performed by changing the polarity of the applied voltage. The Reset and Set processes in bipolar switching is explained by ion diffusion and migration induced by the electric field and temperature [27].

Many different materials such as solid electrolytes, group IV and III-V semiconductors, perovskites, organic compounds and metal oxides show resistive switching characteristics [5,16]. Among these various types, transition metal oxide based RRAM (TiO_x, AlO_x, NiO_x, TaO_x and HfO_x) has really good properties such as low power consumption, good endurance, CMOS compatibility, high speed, high density and reliability. Also easily oxidizing metals like Ti, TiN, W, Zr and Hf are preferable as the metal electrodes [3,10].

CHAPTER 3

STRUCTURAL ANALYSIS OF ATOMIC LAYER DEPOSITED HfO_2 THIN FILMS ON 300 mm p-TYPE Si WAFER

In this chapter, before investigating complex device architectures, two different crystalline (named in this work as "Logic Por") and amorphous (named in this work as "Tuned Recipe") HfO_2 layers on p-type Si wafer were investigated by Raman spectroscopy, X-ray diffraction (XRD) and temperature dependent dielectric permittivity measurements. These measurements gave us useful information about the structural properties of HfO_2 based wafers. After these measurements, effects of crystalline and amorphous phases on capacitive properties of MOS devices produced from these wafers have been investigated and the results are summarized in Chapter 3.

Devices having high-k dielectric materials became attractive for future CMOS technology due to their thermal stability to have direct contact with Si. Among the various high-k material candidates for replacing SiO_2, HfO_2, with a dielectric constant k=16-25, is a promising counterpart because it is compatible with silicon integrated circuit (IC) processing [28].

In this study, both samples were prepared on epi-ready double-side polished p-type Si (001) wafers via atomic layer deposition (ALD) system. The thickness of the HfO_2 was kept as 50 nm for both type of layers. The deposition process was made by ASM™ Company in Netherland. Cross-sectional views of both samples are shown in Figure 3.1.

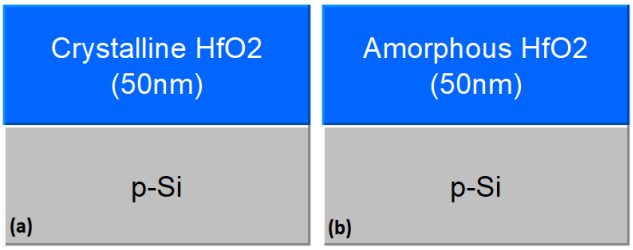

Figure 3.1: ALD deposited 50 nm (a) crystalline (Logic Por) (b) amorphous (Tuned Recipe) HfO_2 layers on p-type Si wafer.

3.1 Raman Spectra of 50 nm Crystalline and Amorphous HfO_2 Coated Si Wafers

Raman spectroscopy measurements were performed by using DPSS Nd-YAG laser at 532 nm wavelength. 750 mm, f9/8 Andor SR750 spectrometer with 150 mm^{-1} grating used to collect the signals. 70 µm laser beam diameter was focused on the samples with a Nikon Eclipse LV100 microscope and the collected signals were transferred to the spectrometer by optical fiber.

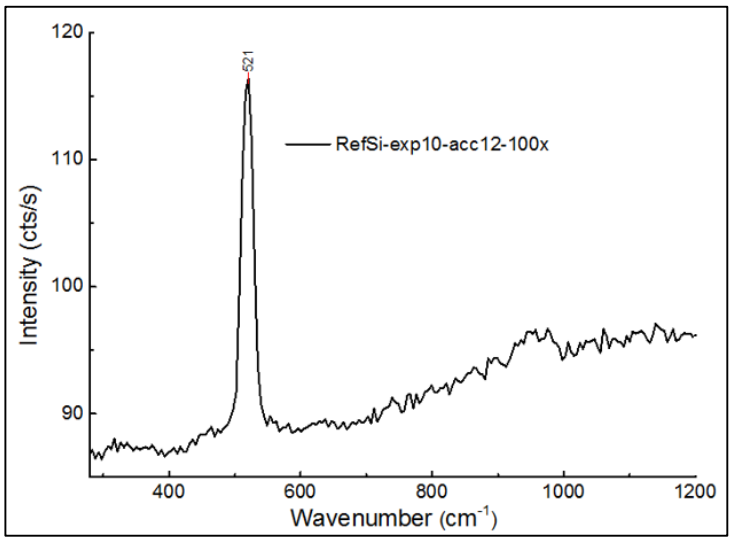

Figure 3.2: Raman spectrum of reference p-type Si wafer.

Firstly, Raman spectrum of polished p-type Si wafer was measured as reference which is shown in Figure 3.2. A strong Raman signal of Si was observed at 521 cm^{-1} and

attributed to the well-known transverse-optical (TO) phonon vibration of Si-Si bonds as expected. Then, the same measurements were performed on 50 nm crystalline and amorphous HfO_2 wafers. Since the 50 nm HfO_2 layers of both types of HfO_2 are very thin, laser penetrates into the bulk Si surface so that there are significant contributions from the Si wafer as well.

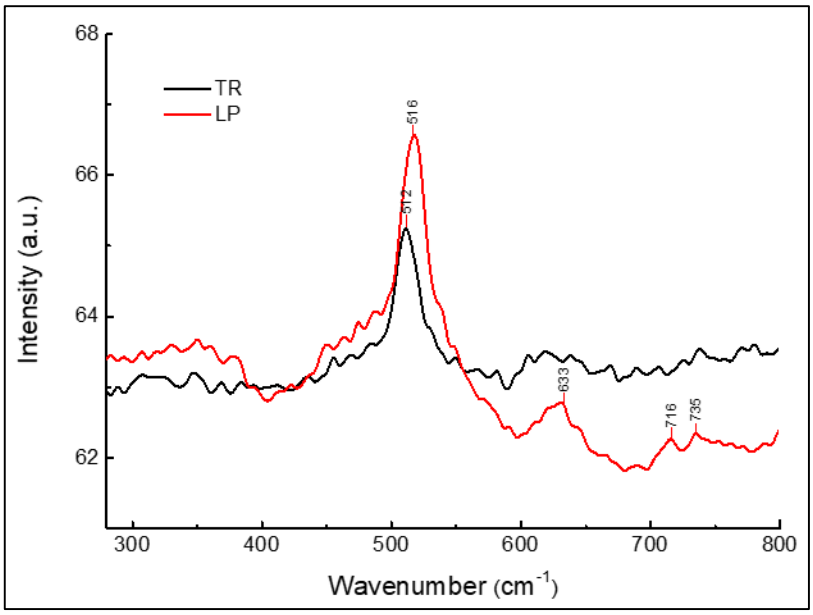

Figure 3.3: Raman spectrum of crystalline (red line) and amorphous (black line) HfO_2 layers on p-type Si wafer.

In Figure 3.3, Raman spectrum of crystalline and amorphous HfO_2 coated layers are shown. In crystalline HfO_2, TO Raman line of the Si wafer is dominant indicating Si-Si lattice vibrations at 521 cm^{-1}. The most significant feature of the Raman peak is the 5 cm^{-1} shift at the main TO line as observed at 516 cm^{-1}. This effect is attributed to interface between Si and HfO_2, where Si in the wafer and the oxygen in the HfO_2 are binding together and giving rise to line observed at 516 cm^{-1}. In the amorphous case, the shift is even larger, that is at 512 cm^{-1}, indicating that the deformation in the bonding structure is effective. Also, amorphous HfO_2 induces more tensile stress on Si compared to crystalline HfO_2. Therefore, a greater peak shift is observed in the amorphous case.

3.2 XRD Spectra of 50 nm Crystalline and Amorphous HfO_2 Coated Si Wafers

X-ray diffraction (XRD) measurements provide very useful information on the structural properties of a material under investigation. The measurements were performed on a reference p-type Si wafer, 50 nm amorphous HfO_2 and crystalline HfO_2 coated layers. Scan range for all samples is between 20^o and 40^o as a function of 2Θ diffraction angle with a scan speed of 1 deg/min. Figure 3.4 shows the XRD pattern of both side polished reference p-type Si wafer and no diffraction peaks were observed as expected.

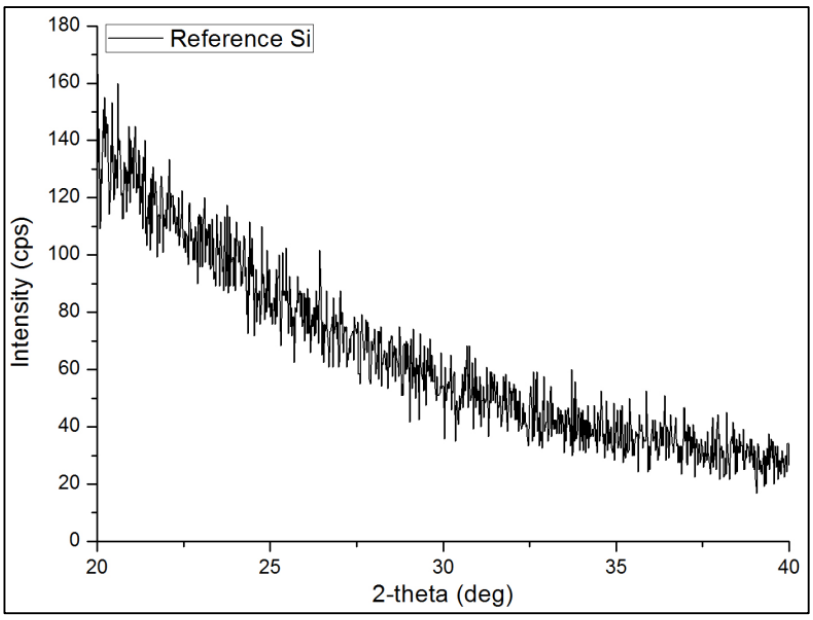

Figure 3.4: XRD spectrum of reference p-type Si wafer.

Crystalline HfO_2 wafer has two phases of HfO_2 which are monoclinic and tetragonal as shown in Figure 3.5.

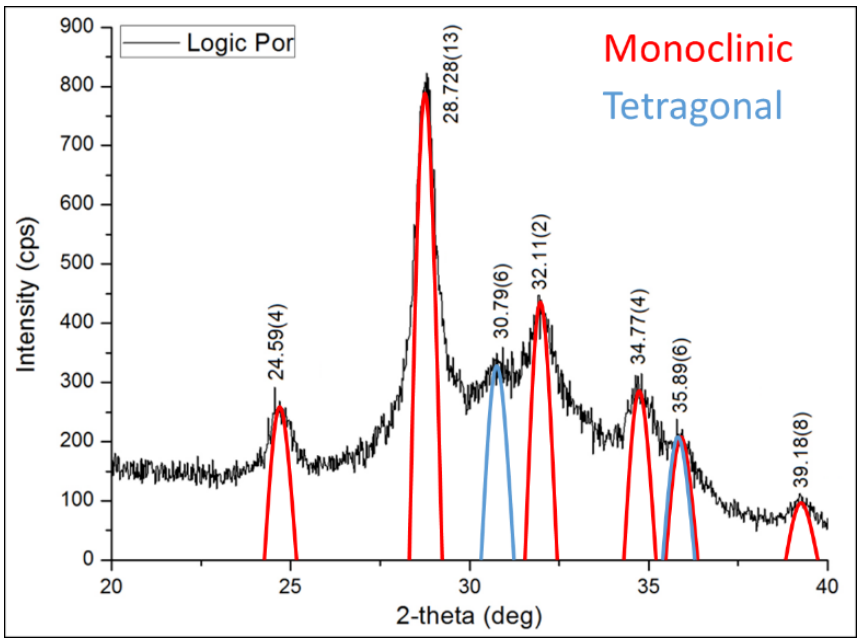

Figure 3.5: XRD spectrum of 50 nm crystalline HfO_2 coated layer on p-type Si.

In Figure 3.6, crystal structures of HfO_2 in monoclinic and tetragonal phases are shown. The monoclinic phase is observed at the major peak with an angle of $2\Theta = 28.728(13)^o$. Its d-spacing and FWHM are 3.1050(14) Å and $0.642(14)^o$.

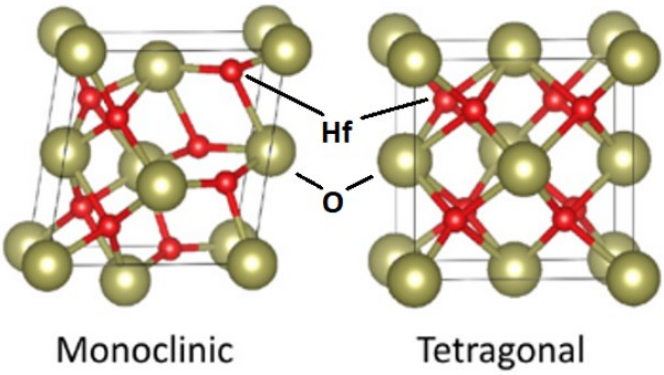

Figure 3.6: Monoclinic (low symmetry) and tetragonal (high symmetry) phases of HfO_2. Adopted from [29].

The following XRD peaks are well-consistent with HfO_2 as well. In the XRD-scan, the peaks around 28.59, 28.72, 32.11, 34.77, 35.89, and 39.18 degrees belong to the (011), (-111), (111), (020), (200), and (021) type diffraction plane family for monoclinic HfO_2, respectively.

The peaks around 30.79 and 35.89 degree belong to the (111) and (200) type diffraction plane family for tetragonal HfO_2, respectively [30,31]. These peaks tells that we have multi-crystalline HfO_2 with monoclinic and tetragonal phases. According to literature, monoclinic phase is the higher temperature phase than the stable tetragonal phase [32]. The major XRD peaks also show that the monoclinic phase peak intensities are higher than the other phase. This means that the major phase is monoclinic and the minor phase is the tetragonal phase within the crystalline film. This also shows that any process that cause a temperature gradient drives the HfO_2 layer irreversibly towards the monoclinic phase during operation, this is referred to in literature as aging effect [33]. The main diffraction peaks are summarized in Table 3.1 for the crystalline 50 nm HfO_2 layer.

Table 3.1: XRD peak positions and relative intensities.

Peak List			
Material Structure	**2-theta (degree)**	**Monoclinic (Peaks)**	**Tetragonal (Peaks)**
Crystalline HfO_2	24.59(4)	(011)	No-Peak
	28.728(13)	(-111)	No-Peak
	30.79(6)	No-Peak	(111)
	32.11(2)	(111)	No-Peak
	34.77(4)	(020)	No-Peak
	35.89(6)	(200)	(200)
	39.18(8)	(021)	No-Peak

On the other hand, In Figure 3.7, amorphous HfO_2 sample shows a wide band scattering at $2\Theta=32.90^o$ with d-spacing of $2.720(13)^o$ and a FWHM of 7.1(3) Å indicating that the material is amorphous.

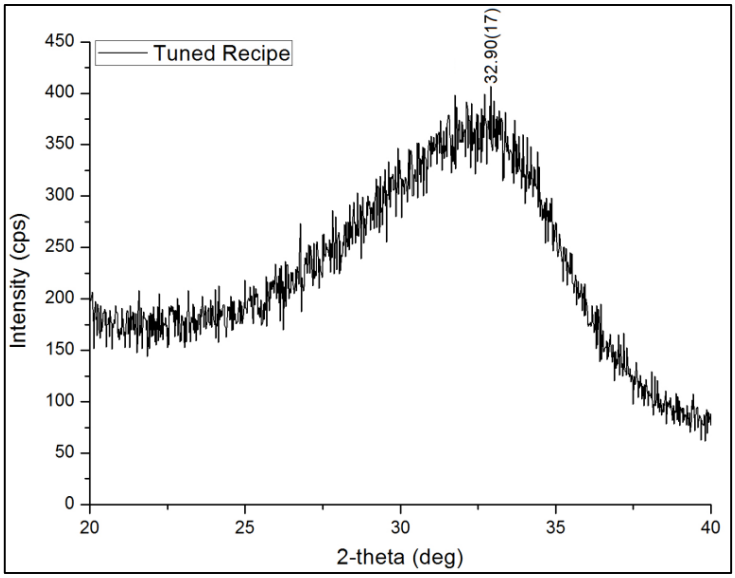

Figure 3.7: XRD spectrum of 50 nm amorphous HfO_2 coated layer on reference p-type Si.

3.3 Temperature Dependent Dielectric Permittivity Measurements on 50 nm Crystalline and Amorphous HfO_2 Coated Si Wafers

Temperature dependent dielectric permittivity measurements were carried out in nitrogen (N_2) atmosphere by squeezing crystalline HfO_2 and amorphous HfO_2 wafers separately between gold circular electrodes having 2.0 cm diameter. The voltage applied by the impedance analyzer (V_{RMS}) was set to 1.00 V. Lower V_{RSM} voltages of 0.10 V and 0.01 V were applied but no characteristic change was observed. Stable measurement results were obtained between 10^2 Hz and 10^7 Hz frequency range.

In Figure 3.8, frequency dependent dielectric permittivity measurement and the loss factor on crystalline HfO_2 wafer are analyzed at 20° C, 40° C and 60° C temperatures. Dielectric permittivity indicates the amount of stored energy in the cell when an external electric field is applied, where loss factor shows the amount of dissipation under an external electric field [30].

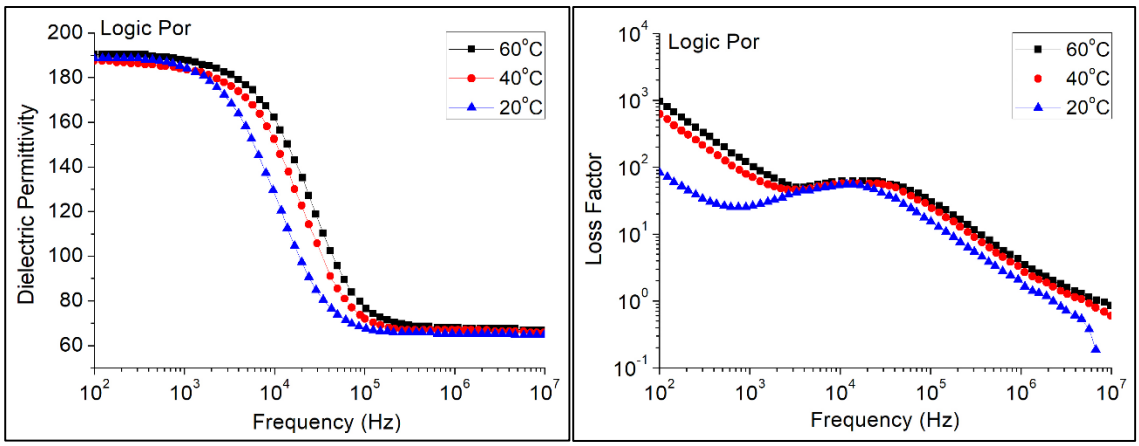

Figure 3.8: Dielectric permittivity and loss factor curves of crystalline HfO_2.

As the temperature increases, permittivity curves shift towards higher frequencies. Similar to the permittivity curve, the maximum point of loss factor curve at 10^4 Hz shifts towards higher frequencies depending on the increasing temperature. The maximum point indicates a dipolar behavior and it tells that the energy loss in the structure is maximum around those frequencies [30]. Linear behavior at low frequencies can be explained as DC conductivity due to electrical behavior at the sample electrode interface.

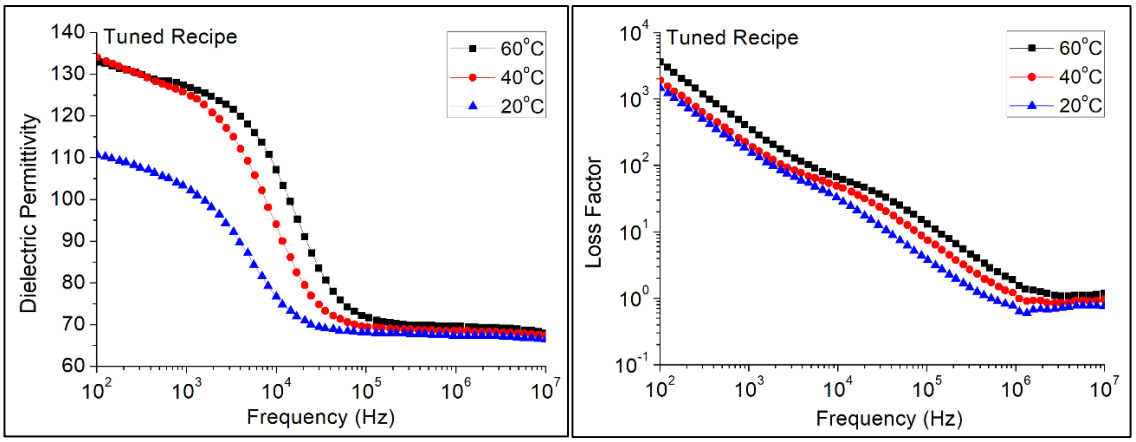

Figure 3.9: Dielectric permittivity and loss factor curves of amorphous HfO_2.

In Figure 3.9, dielectric permittivity and the loss factor measurements on amorphous HfO_2 coated sample at the same conditions as the crystalline HfO_2 wafer are shown and the results are different. Dielectric permittivity of the sample showed a significant increase towards lower frequencies. At higher frequencies between 10^5 Hz and 10^7 Hz, dielectric permittivity remained stable at about 70 independently of the temperature. However, in the lower frequency ranges between 10^4 Hz and 10^2 Hz it reached to 110 at 20^o C. This increasing trend starts at 10^5 Hz for the measurements at 40^o C and 60^o C temperatures. This indicates a significant effect of temperature on the amorphous sample. All the samples observed at low frequencies that is close to DC region show capacitive behavior.

It should be noted that these measurements were performed without depositing metal electrodes on the wafers. Therefore, we cannot consider these results as a results of a MOS device. This can also be the explanation of high dielectric permittivity values. On the other hand, the large permittivity difference between the crystalline and the amorphous phase might be used in memories like those based on phase change materials (PCM) defined in the introduction section which operations rely on the fact that oxide-based materials can be reversibly switched from an amorphous phase (Logic 0 state) to a crystalline phase (Logic 1 state) or vice versa by an external electric current.

CHAPTER 4

METAL DEPOSITION ON 50 nm CRYSTALLINE AND AMORPHOUS HfO_2 COATED Si WAFERS

In this chapter, two different MOS devices were built by metal deposition on previously fabricated and analyzed crystalline and amorphous HfO_2 samples in Chapter 3. Then C-V measurements were performed on the devices which is a widely used method for determining the reliability and quality of oxide materials for semiconductor fabrication. It gives us useful information about bulk material, interface charges and metal-oxide-semiconductor (MOS) device parameters such as dielectric permittivity. This measurement is generally performed on capacitor-type devices like MOS.

4.1 Fabrication and Device Configurations

The devices have two different HfO_2 structures (crystalline/amorphous) as shown in Figure 4.1.

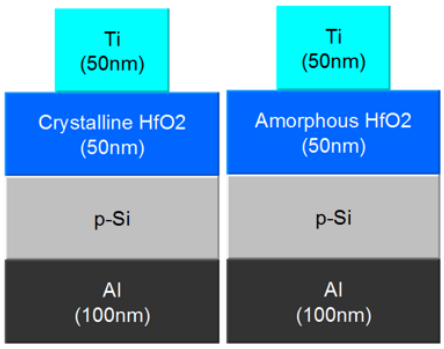

Figure 4.1: Two types of MOS devices having 50 nm crystalline and amorphous HfO_2 based materials.

Each device has 50 nm ALD deposited amorphous and crystalline HfO_2 layers as the oxide material and they both have 50 nm Ti metals as top electrode (TE) deposited by thermal evaporation. In Figure 4.2, TE patterns having three different radius lengths of 2.00 mm, 1.25 mm and 0.63 mm deposited by using a shadow mask are shown. All stacks have p-type Si layer below the HfO_2. 100 nm Al layers were deposited on the back side of p-type Si by thermal evaporation as the bottom electrical contact.

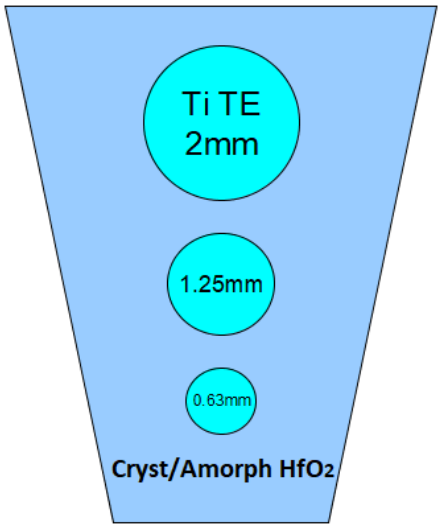

Figure 4.2: Top views of amorphous and crystalline HfO_2 wafers with Ti TE having 0.63 mm, 1.25 mm and 2.00 mm radius.

4.2 Extracting MOS Device Parameters From C-V Measurements

Similar to a MIM structure, a MOS structure is composed of two terminals which are metal TE, semiconductor substrate (such as n or p-type Si) and an insulating oxide layer sandwiched between the electrode and substrate. Interface between the oxide layer and the Si substrate is important for the functional performance of the device [30]. In Figure 4.3, MOS structure and four different operation steps are shown. In this figure, p-type Si is used as substrate which has majority of holes as carriers. In the first step, the device is in thermal equilibrium since no potential is applied. If a negative potential is applied from the metal TE, the holes accumulate at the Si-oxide interface. This is called

accumulation region. Then, if the polarity of the voltage is changed and a small positive voltage is applied, this time the nearest charge carriers to the interface are repelled and a depletion region forms. Finally, in the case of application of a greater positive voltage, the depleted carriers grow towards the oxide and it becomes attractive for electrons to be collected at the interface [30]. This final step is named as inversion region.

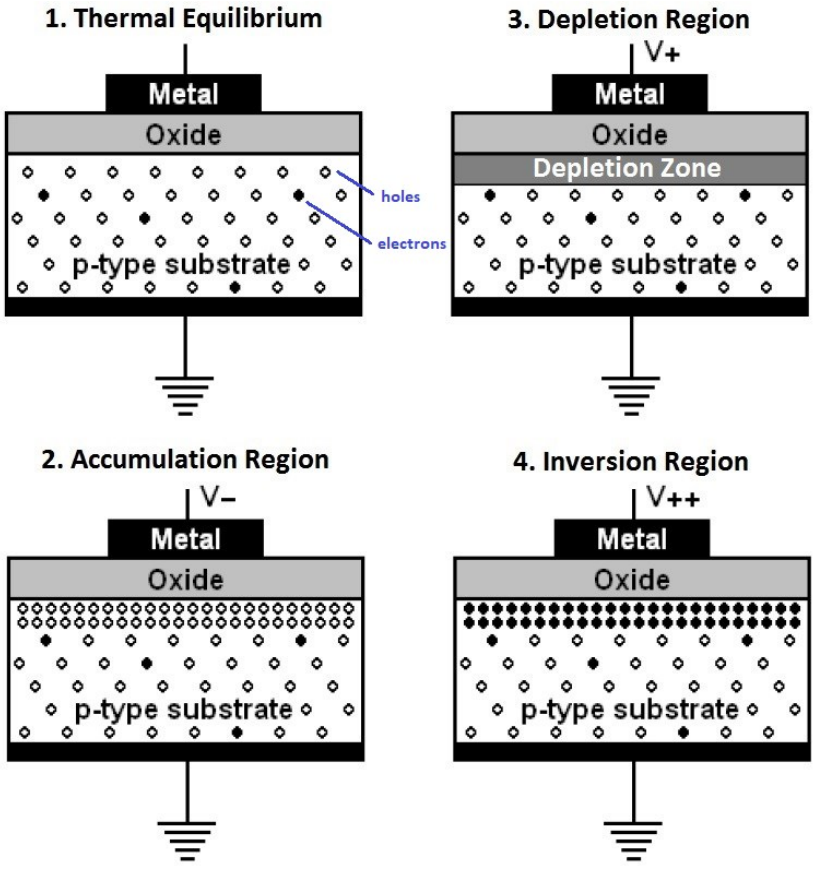

Figure 4.3: p-type MOS capacitor at different operation steps. Adopted from [30].

The dielectric constant ε_{OX} of a MOS capacitor can be calculated as follows.

$$\varepsilon_{OX} = \frac{C_{OX} t_{OX}}{\varepsilon_0 A}$$

where C_{OX} is the measured capacitance in the accumulation region, t_{OX} is the oxide thickness, ε_0 is the permittivity of free space and A is the cross sectional area of metal electrode [34]. In some cases, C_{OX} can be considered as the measured capacitance but sometimes series resistance (R_S) compensation should be done in order to eliminate the undesired impact on the capacitance measurement causes from the electrical contact with the wafer as shown in Figure 4.4 [35].

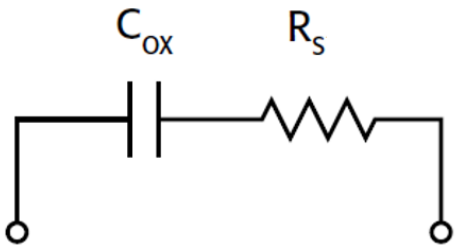

Figure 4.4: Simplified model for determining R_s.

Otherwise, measured capacitance and conductance values can be lower than the real values. R_S can be calculated from the measured capacitance and conductance values as follows.

$$R_S = \frac{\left(\frac{G}{2\pi f C}\right)^2}{\left[1+\left(\frac{G}{2\pi f C}\right)^2\right]G}$$

where C is the measured parallel model capacitance in strong accumulation region, G is the measured conductance and f is the measured frequency. After calculating the R_S, it can be used to extract the corrected capacitance (C_C). The equation of C_C and is given in the next page.

$$C_C = \frac{\left(G^2 + (2\pi fC)^2\right)C}{\left[G - \left(G^2 + (2\pi fC)^2\right)R_S\right]^2 + (2\pi fC)^2}$$

4.3 Experimental Procedure

In Figure 4.5, schematic view of test platform is shown. In this experiment, since the MOS layers were directly deposited on p-type Si wafer, the back side of the Si substrate which is coated with 100 nm Al metal was used as bottom electrical contact and placed on aluminum platform. Then, a micro positioner was used to get electrical contact from the Ti TE.

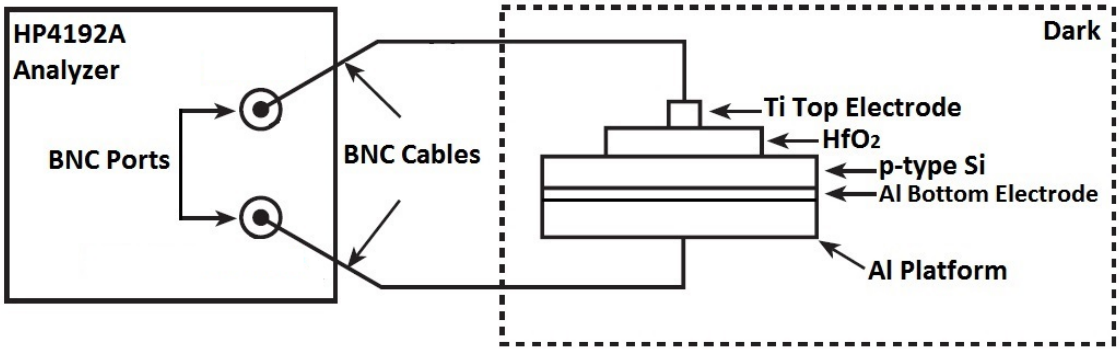

Figure 4.5: HfO_2 based MOS device capacitance measurement scheme.

The micro positioner and the Al platform were connected to the HP4192A impedance analyzer by BNC connections and the tests were performed on LabVIEW™ environment. The impedance measurement platform is shown in Figure 4.6.

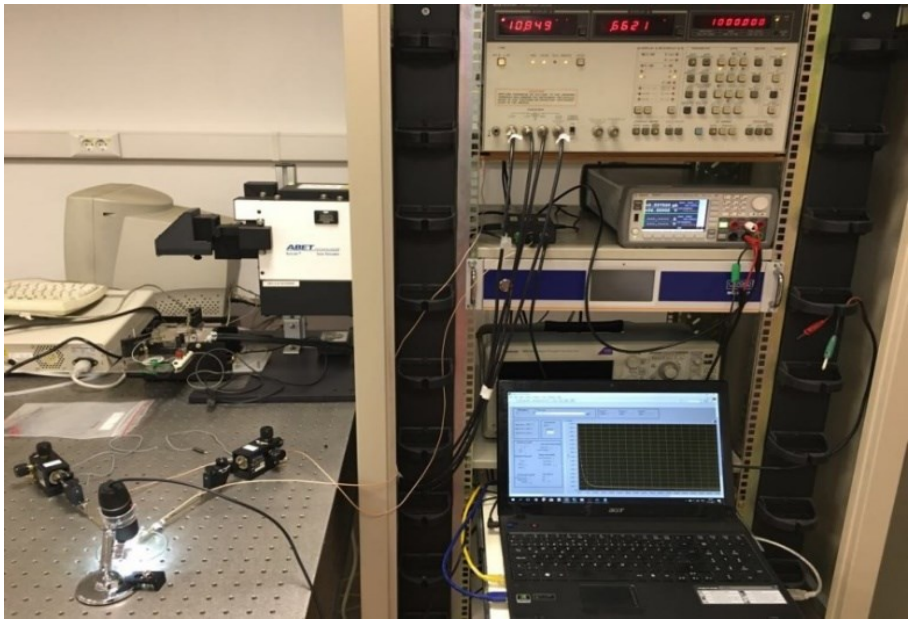

Figure 4.6: Impedance measurement platform.

4.4 C-V Measurement Results of MOS Devices

Frequency dependent capacitance-voltage (C-V) measurements were performed on amorphous and crystalline HfO_2 samples having Ti TE. DC bias voltage was swept from -2.0 V to 2.0 V for each device with a 500.0 mV AC modulation amplitude (V_{osc}). Measurements were performed between 10.0 kHz and 1.0000 MHz AC modulation frequencies. These capacitance measurements can provide us useful information about the oxide material and interface properties of the devices.

In Figure 4.7, frequency dependent capacitance curves of crystalline and amorphous HfO_2 based MOS devices having 0.63 mm, 1.25 mm and 2.00 mm Ti TE and p-type Si are shown.

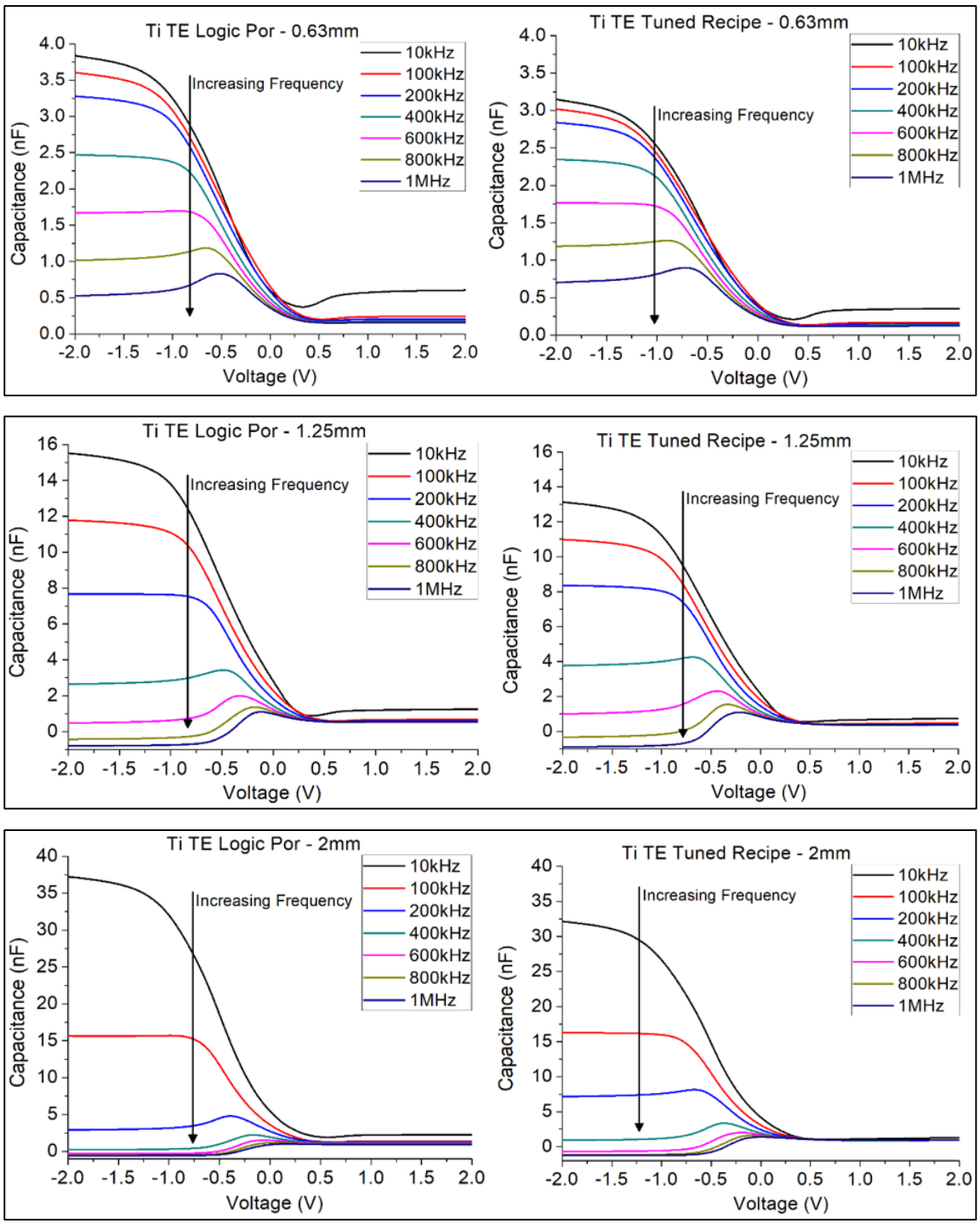

Figure 4.7: C-V curves of crystalline (Logic Por) and amorphous (Tuned Recipe) HfO_2 devices having radius 0.63 mm, 1.25 mm and 2.00 mm Ti TE.

Since it is a p-type MOS device, the accumulation region of the capacitance curve is observed when negative DC voltages are applied. Therefore, the majority carriers (in this case holes) are attracted towards the gate of the device because of the negative polarity of the applied potential. Since the HfO_2 is a good insulator material, the holes accumulate at Si-HfO_2 interface and the MOS device behaves like a parallel plate capacitor. For better understanding, energy band diagram of the device at accumulation region is shown in Figure 4.8.

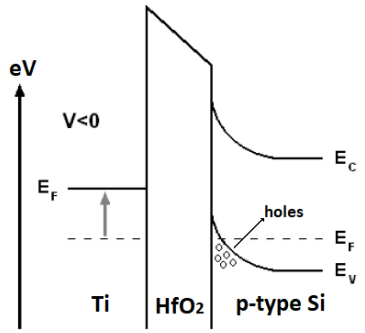

Figure 4.8: Energy band diagram of HfO_2 based p-type MOS device having Ti TE in accumulation region.

When the voltage is swept towards the positive values, the capacitance values start to decrease because the holes are repelled from the Si-HfO_2 interface and a depletion region forms. Correspondingly, the analyzer measures HfO_2 capacitance and the depletion capacitance in series.

When the positive voltage is continued to increase, the depletion zone expands through the semiconductor, the depletion capacitance becomes smaller and we measure smaller capacitance values. Therefore, the slope of the C-V curve becomes negative. The energy band diagram of device in the depletion region is shown in Figure 4.9.

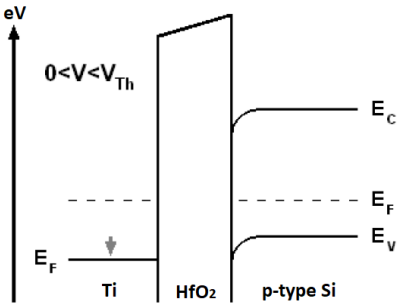

Figure 4.9: Energy band diagram of HfO_2 based p-type MOS device having Ti TE in depletion region.

After a threshold voltage having positive polarity, electron-hole pairs are generated and the electrons are attracted towards the gate. Since the HfO_2 is a good insulator, the electrons accumulates at the HfO_2-Si interface and formed the inversion layer. Therefore, the C-V curve becomes flat and does not decrease anymore because it reaches a maximum depth. The energy band diagram of the device in the inversion region is shown in Figure 4.10.

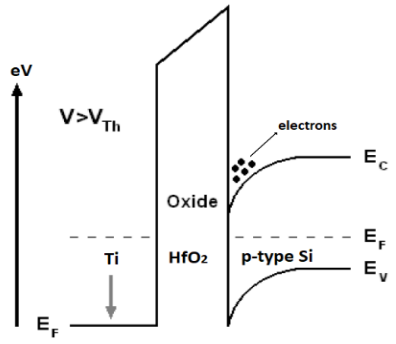

Figure 4.10: Energy band diagram of HfO_2 based p-type MOS device having Ti TE in inversion region.

Also, we observed that the maximum point of the capacitance curves decreased together with the increasing frequency. This is because of the frequency dependency of interface trapped charge relaxation, series resistance (R_S) of the device, test setup and also the leakage current inside the HfO_2 layer [36].

Besides this, capacitance values increased linearly together with the increasing Ti TE area. This is a supporting behavior of our experimental results. In Table 4.1, oxide capacitance (C_{OX}) values measured at the accumulation region and the corresponding dielectric constants of both crystalline (Logic Por) and amorphous (Tuned Recipe) samples at 10 kHz frequency are shown.

Table 4.1: Oxide capacitance (C_{ox}) in the accumulation region and corresponding dielectric constant (ε_o) of crystalline (Logic Por) and amorphous (Tuned Recipe) samples at 10 kHz.

Electrode Radius (mm)	**0.63**	**1.25**	**2.00**
Logic Por			
C_{OX} (nF)	3.8	15.6	37.9
ε_{OX}	17.7	18.3	17.8
Tuned Recipe			
C_{OX} (nF)	3.2	13.2	32.9
ε_{OX}	14.5	15.5	15.1

Capacitance measurements were performed on three different contacts of all 0.63 mm, 1.25 mm and 2.00 mm Ti TEs in order to compare the reliability of amorphous and crystalline HfO_2 layers. According to the results, measured capacitance values from different contacts are accurate. Therefore, we can say that both ALD HfO_2 layers have good reliability. The average calculated dielectric constants of crystalline and amorphous samples are 17.9 and 15.0, respectively as shown in Figure 4.11. It was observed that, crystalline HfO_2 layer has higher dielectric constant which is consistent with the dielectric constant values of HfO_2 in literature. Previously in Chapter 3, we already observed the similar difference between these two HfO_2 layers. This is because crystalline phase of HfO_2 is denser than amorphous phase. Therefore, we can say that

crystalline HfO_2 is a better candidate for oxide based RAMs which needs high-k materials.

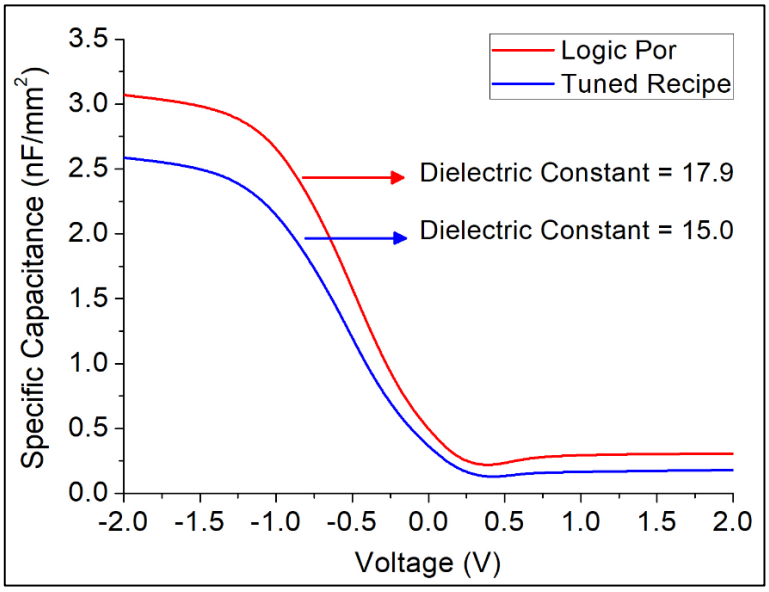

Figure 4.11: C-V curve of crystalline (Logic Por) and amorphous (Tuned Recipe) HfO_2 devices having Ti TE at 10 kHz.

CHAPTER 5

ADVANCED RESISTIVE MEMORY WITH SELECTOR (MARS) SAMPLES

In this chapter, the structures of four different memory stacks namely Advanced Resistive Memory with Selector (MARS) samples manufactured by CEA-LETI™ and ASM™ Cooperation are explained and the results of several electrical measurements are evaluated.

5.1 Fabrication and Device Configurations

The devices have four different bottom electrode (BE) configurations as shown in Figure 5.1.

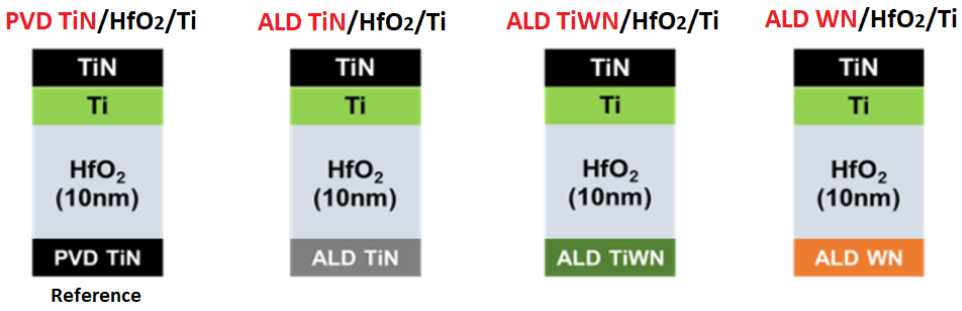

Figure 5.1: HfO_2 based MARS memory stacks having four different BE configurations namely PVD TiN BE, ALD TiN BE, ALD TiWN BE and ALD WN BE.

Each memory stack has 10 nm ALD HfO_2 layer as the memory environment and they have 50 nm TiN on 10 nm Ti layer as the TE material. One of the devices has PVD TiN BE layer and it is considered as the reference memory stack.

Other three memory stacks have additional ALD BE layers composed of TiN, TiWN, WN. The cross-sectional views and the cross-bar structures of metal contacts of the reference PVD and ALD BE memory stacks are shown in Figure 5.2. $HfCl_4$ precursor was used to deposit 10 nm HfO_2 layers at 300° C on blanket wafers. PVD sputtering technique was used to deposit 50 nm TiN over 10 nm Ti TE layers and also the bottom (Metal 1) and top (Metal 2) metal contacts at 350° C. The area of the contact pads is 80 μm^2. Photolithography and reactive ionic etching (RIE) were used for mesa patterning.

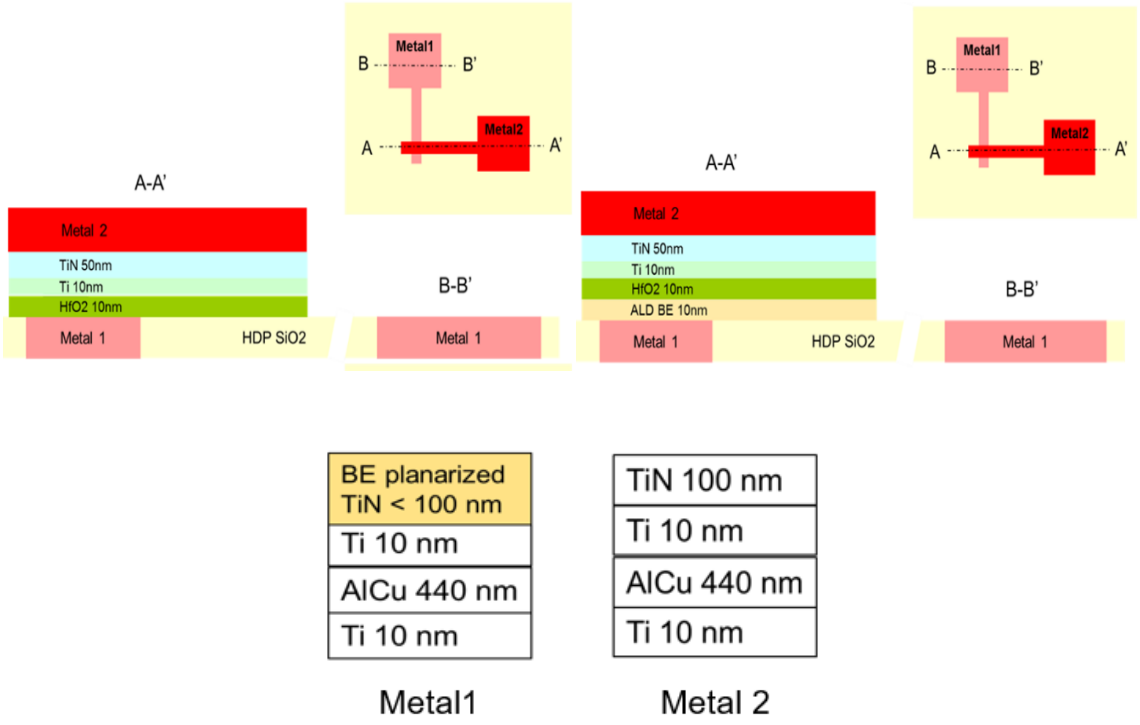

Figure 5.2: Cross-sectional views of reference PVD BE (Left), ALD BE (Right) and bottom (Metal 1) and top (Metal 2) electrical contacts.

5.2 Experimental Procedure

The electrical I-V measurements were performed by a Keithley 4200 SCS (semiconductor characterization system) and with probe station. The memory stacks are composed of 1R (resistive memory layer) structure having two terminals (two electrodes as top and bottom). Therefore, two probes were used to get electrical contact from the contact pads of the devices.

Figure 5.3: I-V measurement platform.

In Figure 5.3, I-V measurement platform is shown. As seen from the photographs, there is a probe station with two micro positioners and the sample placed on the stage of the probe station is observed by an optical microscope. An additional camera system is connected to the computer for probing the contacts. The micro positioners are connected to the Keithley 4200 SCS by BNC connectors. The quasi-static I-V measurements were performed by using the original vendor software.

5.3 Quasi-Static I-V Measurements

In the scope of quasi-static I-V measurements, various tests were performed at three different states of the devices namely initial resistive state (IRS), low resistive state

(LRS) and high resistive state (HRS). Initial resistance measurements were done to evaluate the resistance of as-fabricated devices having the highest resistance values. Then, Forming measurements were performed to determine the Forming voltage of each memory stack, which is a threshold voltage level needed to form a conductive filament between the metal electrodes through the dielectric layer and switches the device from IRS to LRS. Once the Forming was done, the devices were switched between the LRS and the HRS states to observe the switching behaviors. Then the resistivity differences between the HRS and LRS states, namely, memory windows were evaluated.

5.3.1 Initial Resistance Measurement Results

Initial resistance (pristine resistance) of devices is the resistance value of as-prepared samples before the Forming process. Initial resistance values measured on 20 different HfO_2 cells of each memory stack. In Figure 5.4, initial resistance ranges of four different memory stacks are shown. Each bar represents a data set of 20 measurements on each sample.

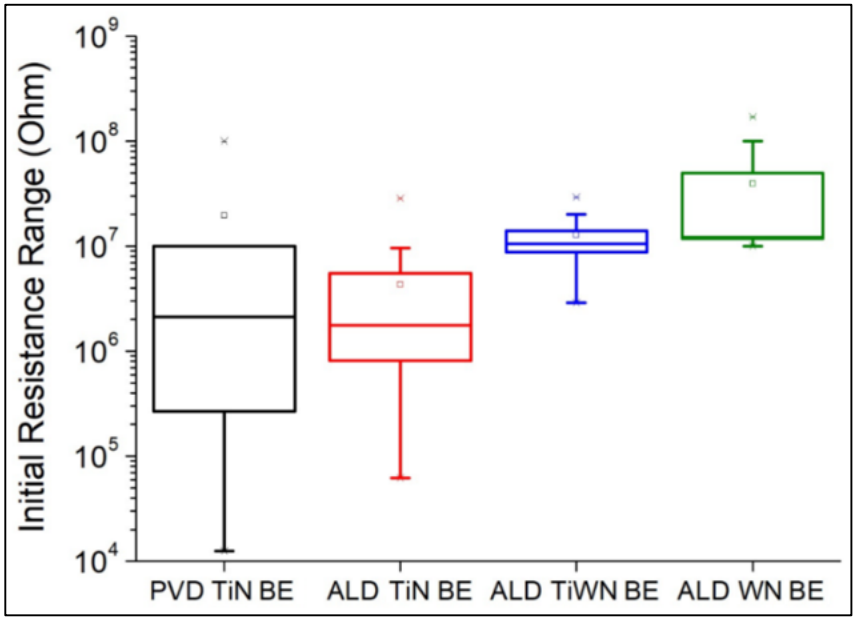

Figure 5.4: Initial resistance ranges measured on 20 different cells of PVD TiN BE, ALD TiN BE, ALD TiWN BE and ALD WN BE.

Wider resistance dispersion was observed in the reference PVD TiN BE compared to other memory stacks. Its initial resistance values range between 10^4 and 10^8 Ohms. ALD BE stacks are compared independent from PVD BE stack. Among the ALD BE stacks, ALD TiN BE has lowest initial resistance. The minimum measured resistance is slightly lower than 10^5 and the maximum resistance value is about 10^7 Ohm. The initial resistance values of ALD TiWN BE and ALD WN BE are more stable and approximately 1 decade higher than the others. Especially on the measurements performed on ALD TiWN BE, it was observed that the initial resistance values are very close to each other and they are in the order of 10^7 Ohm. For the ALD WN BE stack, the lowest observed initial resistance values is 10^7 Ohm and the highest observed one is in the order of 10^8 Ohm. This memory stack has the highest initial resistance values among the all memory stacks.

5.3.2 Forming Voltage Measurement Results

Forming voltage is defined as the voltage needed to trigger a conductive filament formation inside the highly resistive HfO_2 layer and conduct current between the top and bottom electrodes as mentioned before in the introduction chapter. In our experiment, it was conducted by applying a DC voltage from the top electrical contact of the wafers while grounding the bottom electrical contacts. The voltage was swept from 0 V to 4.0 V with a 0.2 V increment and 300 µA compliance current (CC) was applied instantaneously to prevent any unwanted breakdown in HfO_2 layer. This process was performed on 20 different HfO_2 cell of each memory stack and the average Forming voltage of each memory stack was determined. Then the results are compared. In Figure 5.5, Forming voltage distributions measured on 20 different cells of each memory stack are shown.

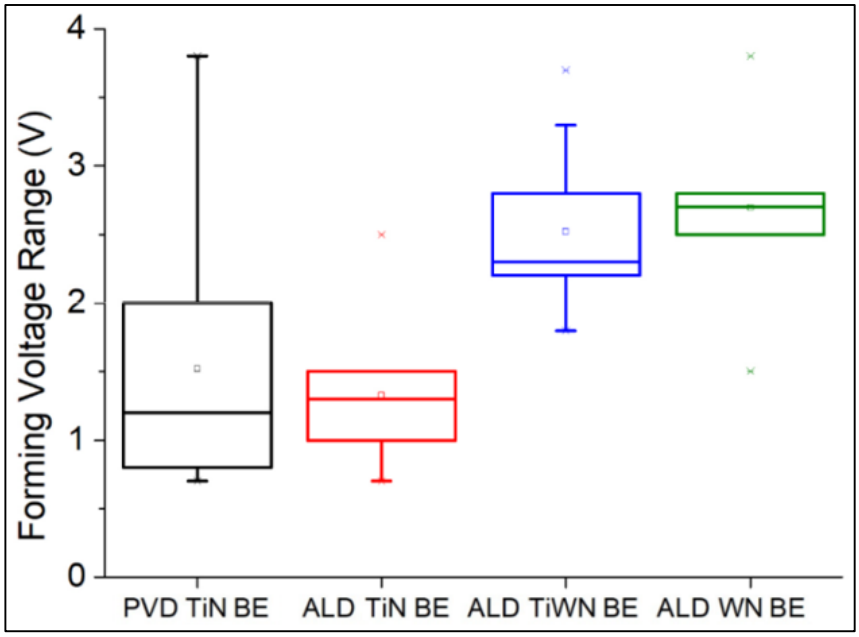

Figure 5.5: Forming voltage distribution measured on 20 different cells of PVD TiN BE, ALD TiN BE, ALD TiWN BE and ALD WN BE.

According to the results, the average Forming voltage for PVD TiN BE is determined as 1.5 V. However, since the Forming voltage distribution is wide, it has been suggested that it does not have a stable structure. On the other hand, the average Forming voltage of ALD TiN BE is determined as 1.3 V which is an important characteristic for low power applications. This stack is more stable than PVD TiN BE as well. ALD TiWN BE also exhibits a stable distribution but its average Forming voltage is 2.5 V that is much higher than ALD TiN BE. ALD WN BE has the highest average voltage among all memory stacks with 2.7 V.

5.3.3 Switching Measurement Results

After evaluating the Forming voltages of each memory stack, switching measurements were performed. 5 quasi-static cycles were observed on 4 different cells of each memory by switching between Reset (Logic 0) and Set (Logic 1) states. Switching was performed by sweeping the voltage between -2.0 V and 2.0 V with 300 µA CC. By this

way, switching accuracy and Set-Reset voltages of memories were evaluated. In Figure 5.6, switching behavior of PVD TiN BE is shown.

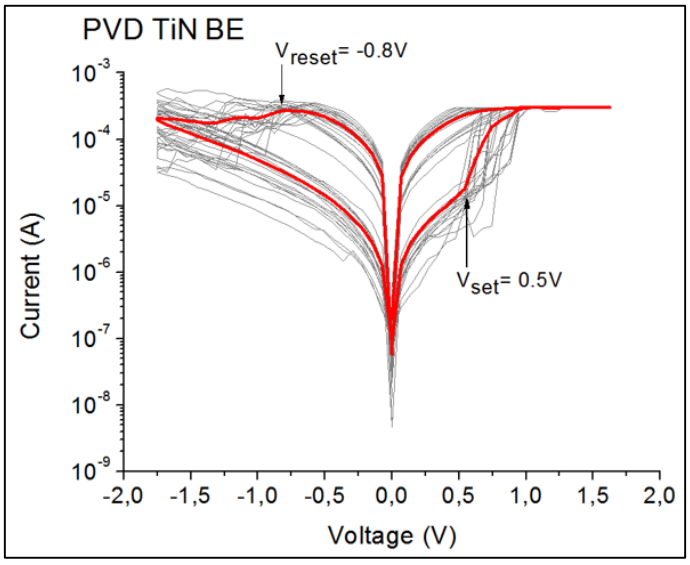

Figure 5.6: 5 Quasi-static switching cycles performed on 4 different cells of PVD TiN BE at 300 µA CC.

The Set voltage is defined as the voltage at the point where the linearity of the I-V curve deteriorates and it is shown as 0.5 V. Same principle is valid for Reset process in the negative region and it is determined as -0.8 V for PVD TiN BE.

In Figure 5.7, switching graph of ALD TiN BE is shown. For this stack, Set and Reset voltages have the same magnitudes with different polarities. Set voltage is 0.5 V while the Reset voltage is -0.5 V. Similar to Forming voltage, ALD TiN BE has the lowest switching voltages in all types.

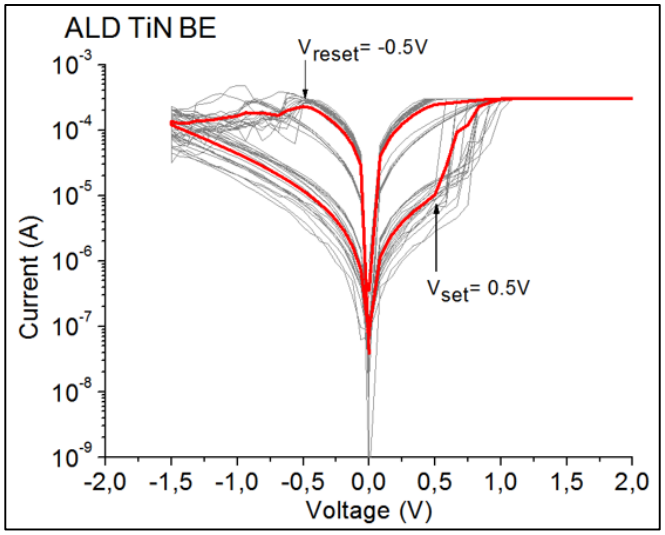

Figure 5.7: 5 Quasi-static switching cycles performed on 4 different cells of ALD TiN BE at 300 µA CC.

For ALD TiWN BE, Set and Reset voltages were evaluated as 0.6 V and -1.0 V, respectively as shown in Figure 5.8. This sample has the highest switching voltage values. Especially Reset voltage is much higher than the others.

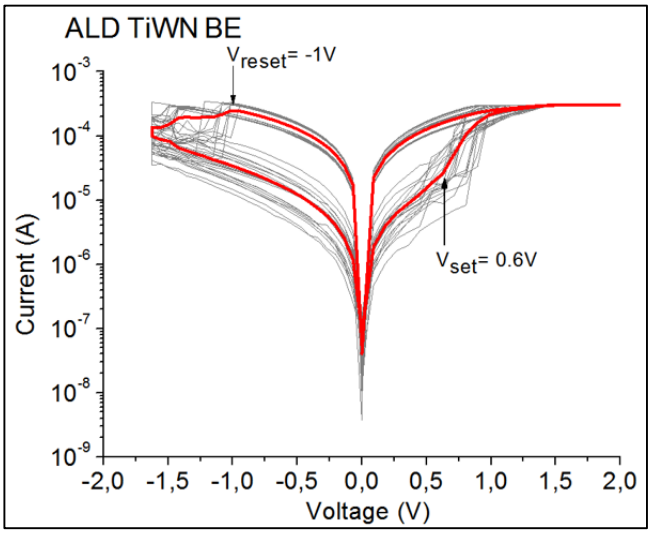

Figure 5.8: 5 Quasi-static switching cycles performed on 4 different cells of ALD TiWN BE at 300 µA CC.

After the Forming process, no switching characteristic was observed for ALD WN BE memory stack as illustrated in Figure 5.9. This behavior tells us that an irreversible break down might occur in the HfO_2 layer after the Forming process and the device could not switched back to HRS. Consequently, no Set process was observed.

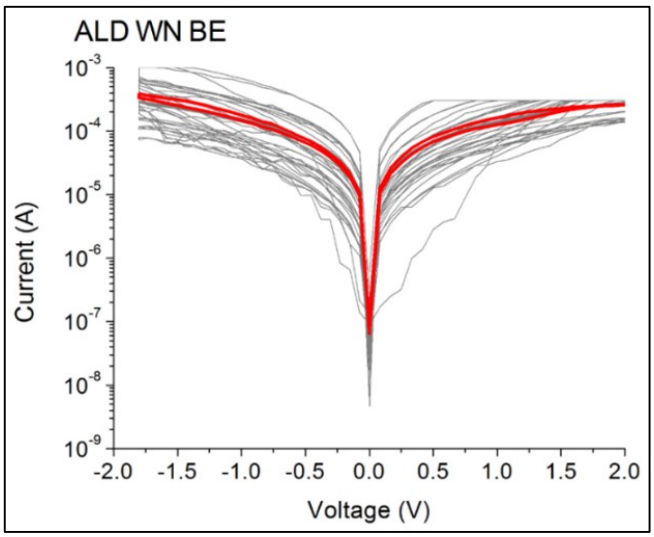

Figure 5.9: 5 Quasi-static switching cycles performed on 4 different cells of ALD WN BE at 300 µA CC.

5.3.4 Memory Window Measurement Results

After observing the switching characteristics, memory window (resistance gap between LRS and HRS) properties of each sample were analyzed. Measurements were performed on 3 different cells of each memory stack by switching the devices 10 times between LRS and HRS. Voltage swept between -2.0 V and 2.0 V under a CC of 300 µA. In Figure 5.10, memory window of reference PVD TiN BE is shown. It has high memory window in Cell 1 and Cell 2 (about 2 decades) but its Cell 3 is very unsteady. In general, its HRS is not steady.

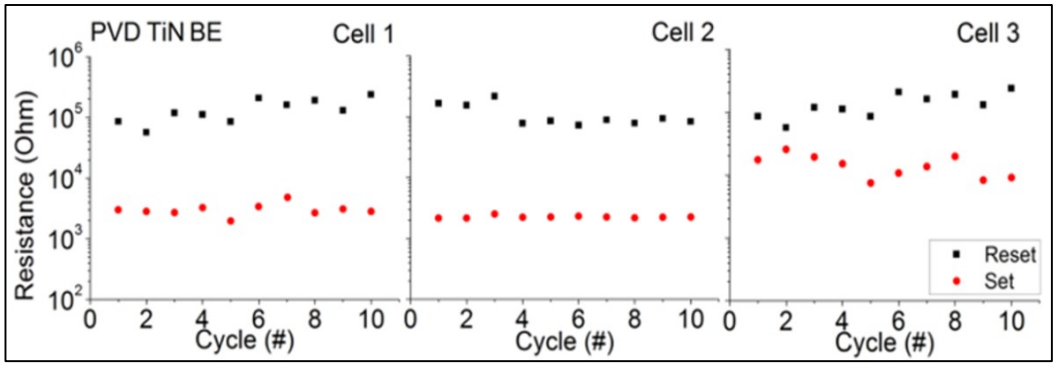

Figure 5.10: Resistance difference between LRS and HRS states (memory window) on 3 different cells of PVD TiN BE at 10 switching cycles.

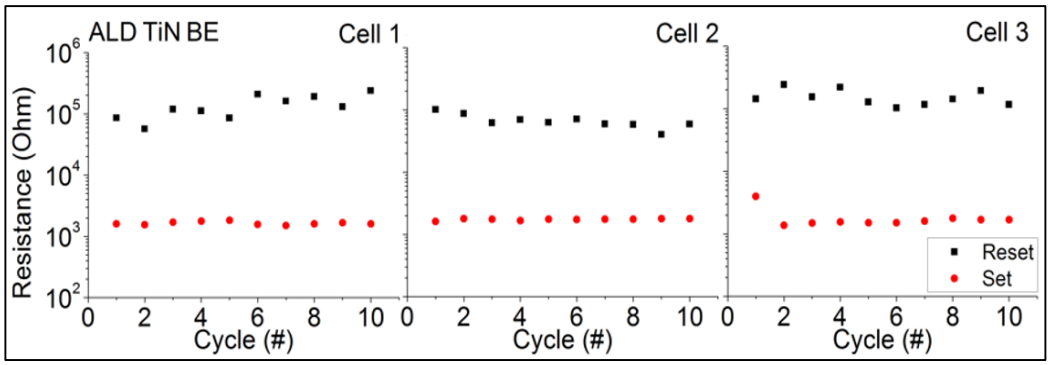

Figure 5.11: Resistance difference between LRS and HRS states (memory window) on 3 different cells of ALD TiN BE at 10 switching cycles.

Figure 5.11 shows the memory window of ALD TiN BE. This memory stack has a high memory window (approximately 2 decades) as well and its HRS and LRS states are more stable compared to PVD TiN BE. ALD TiWN BE has the lowest memory window among the other memory stacks as shown in Figure 5.12. It shows a medium HRS dispersion around 10^5 Ohm but its LRS state is very stable.

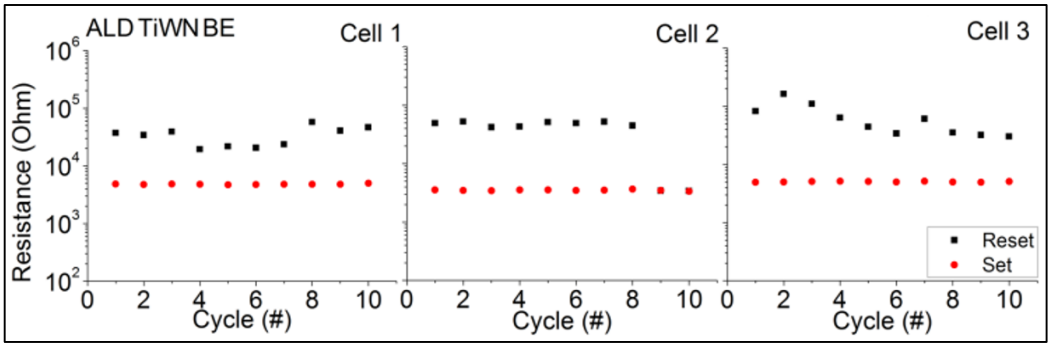

Figure 5.12: Resistance difference between LRS and HRS states (memory window) on 3 different cells of ALD TiWN BE at 10 switching cycles.

In Figure 5.13, since no switching characteristic was observed on ALD WN BE memory stack, memory window behavior could not be analyzed.

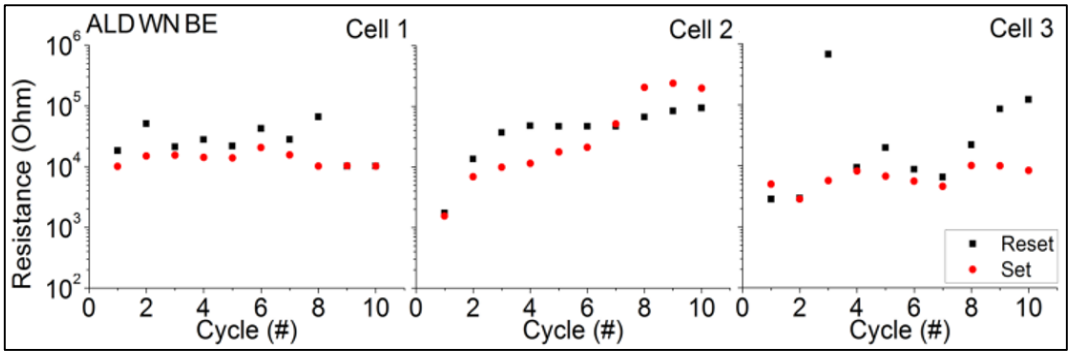

Figure 5.13: Resistance difference between LRS and HRS states (memory window) on 3 different cells of ALD WN BE at 10 switching cycles.

According to the quasi-static I-V measurements, ALD TiN BE and ALD TiWN BE have low operation voltage that is a critical feature for low power applications. Also, their reliability is better than the other memory stacks. It was observed that ALD is a better technique for metal electrode deposition in terms of device performance and reliability compared to PVD.

CHAPTER 6

4K-1T1R IHP MEMORY DEVICE CHARACTERIZATION

In this chapter, the structure of 4K-1T1R (1 Transistor-1 Resistor) packed memory device manufactured by IHP from Germany is explained and the results of several electrical measurements are evaluated.

6.1 4K-1T1R Device Structure

The device is composed of a MIM (metal-insulator-metal) structure having 150 nm TiN TE and BE deposited by magnetron sputtering. Below the TiN TE, there is a 7 nm Ti layer and 8 nm crystalline HfO_2 deposited by ALD. Layers of MIM stack is shown in Figure 6.1. Resistor area of 1T1R structure is 0.4 μm^2 [37].

(a)

Figure 6.1: 1R part of the 1T1R device having 8 nm crystalline HfO_2 layer as the memory environment.

The MIM stack is connected in series to the drain of a select NMOS transistor having 0.25 µm BiCMOS technology. 1T1R test chip configuration and 4Kbit arrays are shown in Figure 6.2. It is constituted by 4000 Cell Matrix, bit-line (BL), source-line (SL), word-line (WL) and operation control circuitry [38]. As explained in the previous chapters, data storage is carried out by switching the resistance of the cell between LRS (Logic 1) and HRS (Logic 0) by Set and Reset operations.

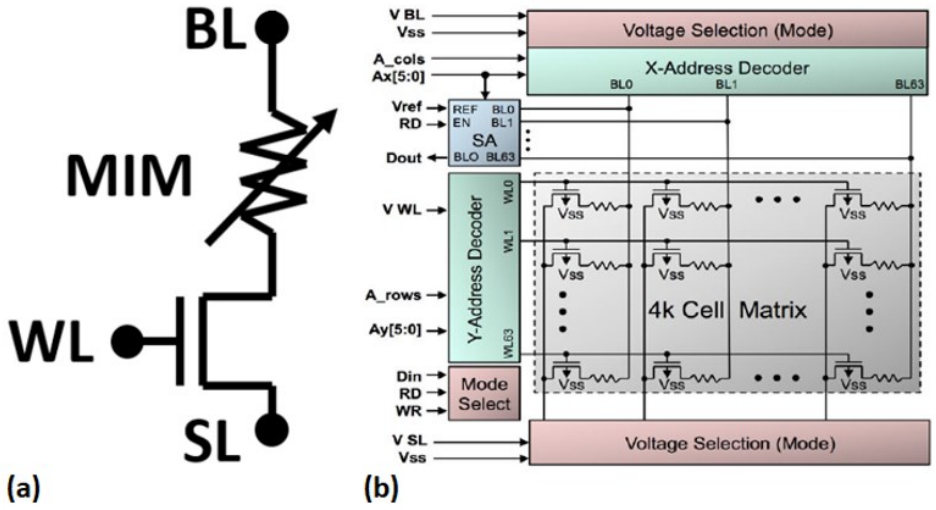

Figure 6.2: (a) 1T1R cell structure (b) 4Kbit cell array structure. Adopted from [38]**.**

6.2 FPGA Based Test Platform

Hardware test platform composed of XILINX™ Artix 7 series AC701 FPGA development board and the user interface of the test software are shown in Figure 6.3. Hardware requirements for RRAM testing were determined by referring to the results of measurements performed on HfO_2 based MARS samples in Chapter 5 and also the pervious measurements on same devices in [37]. Maximum output voltage of the test platform was set to 3.5 V to be able to achieve high Forming voltages.

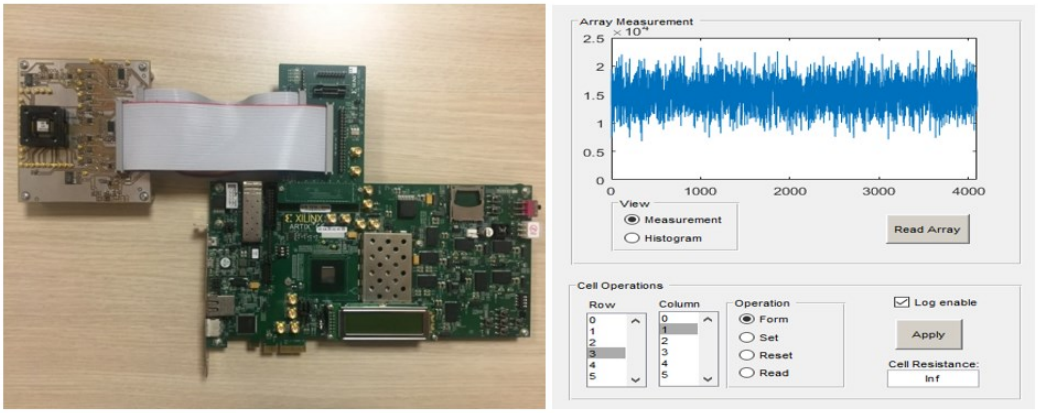

Figure 6.3: RRAM test platform (left) and user interface of test software (right).

Resistance values of the 1T1R RRAM cells can be determined by either applying a read voltage or a read current from the programmable current source or a programmable voltage generator, respectively. Current output upper limit of the test platform can be set to 10 mA for the measurements on the device under test (DUT). Voltages from bit line (BL), source line (SL) and word line (WL) are applied for Forming, switching (Reset/Set) and read operations by the commands from the platform user interface. Table 6.1, gives information about the voltages for memory operations. For the Forming process, voltage pulses are applied from V_{BL} with a 0.01 V increment and a CC of 20 µA.

Table 6.1: Parameters for memory operations.

Operation	**Voltage Values (V)**		
	V_{SL}	V_{BL}	V_{WL}
Forming	0	2.0 – 3.5	1.5
Set	0	0.2 – 3.5	1.5
Reset	0.2 - 3.5	0	2.8
Read	0	0.2	1.5

For the Set process, similar to Forming process, voltage is applied from V_{BL} but with an increment of 0.1 V. Again the CC is set to 20 µA. For the Reset process, voltage is applied from V_{SL} with an increment of 0.1 V and a CC of 10 µA.

6.3 I-V Measurement Results

In Figure 6.4, Forming voltage dispersion of each cell and cumulative probability distribution of crystalline 4K-1T1R packed device is shown. The measurement was performed on each of 4000 cells for one cycle. According to the graph, Forming voltage distribution of the device is between 2.0 V and 3.4 V.

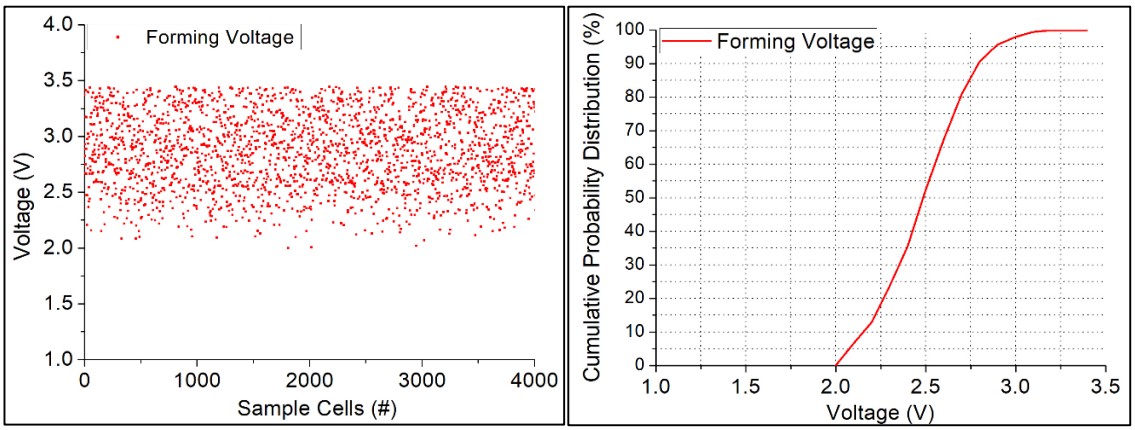

Figure 6.4: Forming voltage distribution (left) and cumulative probability distribution (right) of 1T1R sample over 4000 cells.

After the Forming measurement, switching process was applied to each of the 4000 cells for 1 cycle and the resistance values at HRS and LRS were extracted from the measurement. In Figure 6.5, switching voltage distributions of HRS and LRS and also their cumulative probability distribution are shown. Since the CC was set to 10 µA for Reset and 20 µA for Reset processes, the difference between HRS and LRS (Memory Window) are very close to each other. Therefore, we could not observe a large memory window as observed in on wafer 1R MARS samples in Chapter 5. On the other hand, HRS dispersion is much higher than LRS dispersion similar to MARS samples.

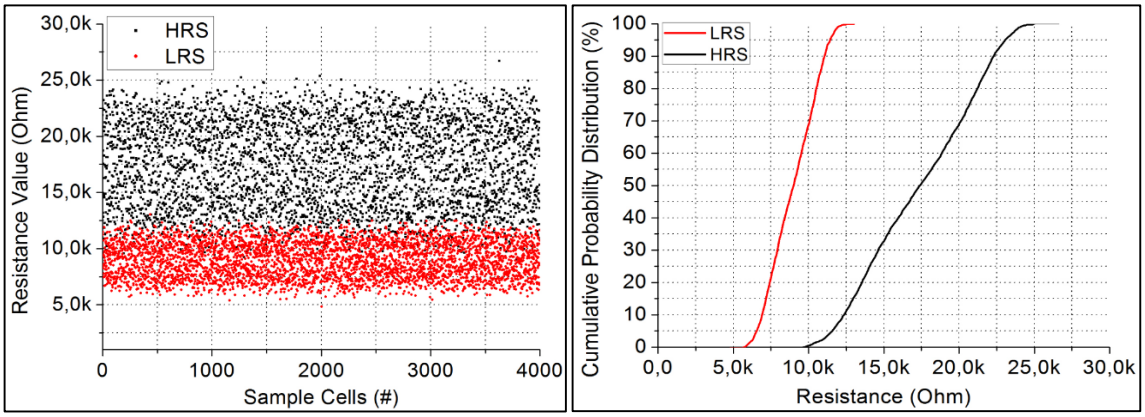

Figure 6.5: HRS and LRS resistance distributions (left) cumulative probability distribution (right) of 1T1R sample over 4000 cells.

The basic parameters used for security applications are the cell array variability of HRS and LRS resistance values. The results from the measurements show that HfO_2 based 4K-1T1R memory device is a suitable candidate for implementing security devices such as physical unclonable functions (PUFs) and random number generators (RNGs) [39,40].

CHAPTER 7

SUMMARY AND CONCLUSION

In this thesis, HfO_2 based RRAMs were investigated in order to explore an efficient embedded non-volatile memory (eNVM) cell for the 28 nm and below CMOS technology nodes. In the scope of the study, it is aimed to contribute the investigation of the optimum dielectric HfO_2 material and metal electrode structures for future eNVMs.

First, a review on memory was given in order to explain currently used technology, its limitations and emerging technologies. Then, in the experimental part, 50 nm crystalline and amorphous coated p-type Si wafers were investigated by Raman spectroscopy and XRD measurements. By this way, structural properties and the effects of crystallinity on transition metal oxide materials were analyzed. The difference between crystalline and amorphous HfO_2 was observed. Monoclinic and tetragonal phases of multi-crystalline HfO_2 were determined. Both Raman and XRD peaks of amorphous HfO_2 are broader than the crystalline one. In the XRD measurement, a monoclinic phase was observed through a major peak at an angle of $2\Theta = 28.728(13)^o$. Its d-spacing and FWHM are 3.1050(14) Å and $0.642(14)^o$. Amorphous HfO_2 sample shows a wide band scattering at $2\Theta=32.90^o$ with d-spacing of $2.720(13)^o$ and a FWHM of 7.1(3) Å.

In addition, temperature dependent dielectric permittivity and loss factor measurements were performed on same amorphous and crystalline samples at 20^o C, 40^o C and 60^o C. According to the results, dielectric permittivity of crystalline HfO_2 is much greater than amorphous HfO_2, but amorphous layer showed a larger temperature dependence. Dielectric permittivity of this sample increased with the increasing temperature.

Also, the large permittivity difference between crystalline and amorphous phases of HfO_2 hints towards its potential for use in PCRAMs.

A further investigation was performed by thermal evaporation of 50 nm Ti layer on both crystalline and amorphous HfO_2 coated wafers at a round geometry with different sizes as top electrodes. A thermally evaporated 100 nm Al planar film was used as back electrode on the entire back side of p-type Si. C-V measurements were performed on the devices in order to determine the reliability and quality of crystalline and amorphous HfO_2 materials. It was observed that the maximum value of the capacitance curves decreased by increasing frequency in both types. This is attributed to the frequency dependency of interface trapped charge relaxation, series resistance (R_S) of the devices and the leakage current inside HfO_2 layer. Besides this, maximum capacitance values in the accumulation region of crystalline HfO_2 are found to be greater than in amorphous HfO_2. Therefore, the calculated dielectric values are found to be greater, as well. Average calculated dielectric constant of crystalline and amorphous HfO_2 samples are 17.9 and 15.0, respectively. Since high-k dielectric materials are attractive for future CMOS technology, it is worthwhile to note the high dielectric constant of crystalline HfO_2.

In addition to C-V measurements, quasi-static I-V measurements were performed on ALD coated 10 nm HfO_2 based 1R resistive RAM (RRAM) devices having four different metal electrode structures. One of the devices has PVD TiN BE as reference stack and the others have ALD coated TiN, TiWN and WN BEs. According to the results, ALD coated BE layer is more reliable than PVD coated BE because PVD TiN BE showed a wide dispersion in initial resistance values, Forming voltage, switching voltage and memory window values. ALD coated BEs are more stable than reference PVD coated BE. Besides these, ALD TiN BE and ALD TiWN BE have lower operation voltages compared to other ones and this is a desired feature for low power applications. The average Forming voltages of PVD and ALD TiN BEs are 1.5 V and 1.3 V, respectively while the ALD TiWN and WN BEs are 2.5 V and 2.7 V, respectively. Besides the Forming voltage, ALD TiN BE has the lowest Set and Reset values as 0.5 V

and -0.5 V, respectively. Set voltage of ALD TiWN BE is also 0.5 V but it has a high Reset voltage as -1.0 V compared to ALD TiN BE. After a high Forming voltage, no resistive switching was observed on ALD WN BE because the device could not switch back to HRS. This might be because a hard dielectric breakdown occur inside the HfO_2 layer. Since no switching was observed on ALD WN BE, no memory window was observed for this memory stack. This means that ALD WN BE is the worst material among the tested ones as BE for these stacks. ALD TiN BE has a memory window nearly one decade higher than ALD TiWN BE. Resistance values of both memory stacks at LRS are very stable and they showed a medium dispersion at HRS. These two memory stacks are very promising in power consumption and reliability respect. They can be good candidates for future RRAM architectures.

An FPGA based I-V measurement platform for 1T1R RRAM arrays was designed by referring to the I-V measurement results obtained from HfO_2 based MARS samples, and a 4K-1T1R packed RRAM device was characterized. First, Forming voltage distribution of each cell in the 4000 array was determined individually by applying the Forming process. Then, each cell was switched for 1 cycle in order to observe the HRS and LRS resistance values. Aim of these measurements was to determine basic Forming and switching parameters of the device to evaluate its potential for using in security applications such as physical unclonable functions (PUFs) and random number generators (RNGs). According to the results, 4K-1T1R array is found to be a good candidate for these applications due to its HRS and LRS cell variability.

As a future prospect, pulsed I-V measurements are suggested to be performed in order to observe the endurance and retention properties of RRAMs. This would provide a deeper insight into the operation properties of RRAMs. Also, I-V measurements at different temperatures can be useful for a more detailed understanding of physics behind. Besides possible implementation of RRAMs in security applications such as PUFs and RNGs, RRAMs also shows promise for use in neuromorphic applications such as neuromorphic hardware systems thanks to their CMOS compatibility, low power consumption and reliability.

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