DESIGN AND IMPLEMENTATION OF A SiC BASED THREE PHASE GRID-CONNECTED CURRENT SOURCE INVERTER FOR SOLAR APPLICATIONS

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ABSTRACT

DESIGN AND IMPLEMENTATION OF A SiC BASED THREE PHASE GRID-CONNECTED CURRENT SOURCE INVERTER FOR SOLAR APPLICATIONS

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In this thesis, analysis, design and implementation of a three-phase 400V, 20 kVA Current Source Inverter (CSI) have been carried out for grid-connected photovoltaic applications based on the multi-string inverter concept. This inverter can be used in large scale photovoltaic (PV) applications by connecting many in parallel at 400V and coupling to medium voltage through a common transformer. The power stage of the inverter is based on the basic full-bridge CSC topology and each power semiconductor which must have bipolar voltage blocking and unidirectional current carrying capability is formed by connecting a Silicon Carbide (SiC) MOSFET and a SiC Shottky Barrier Diode (SBD) in series and switched by employing Pulse Width Modulation (PWM) method with a carrier frequency of 25 kHz.

The Current Source Inverter (CSI) offers several advantages for PV applications in terms of its ability to transfer power through a single power conversion stage over the entire MPP voltage range, direct output current controllability, and low Total Harmonic Distortion (THD) values over a wide range of output power with simpler AC filter. Results of this research have shown that CSI will become a strong alternative to Voltage Source Inverter (VSI) for PV applications with the widespread use of high voltage and current SiC power semiconductors.

Keywords: Silicon Carbide (SiC), Three-Phase Grid Connected Multi-String Inverter, Current Source Inverter (CSI), Photovoltaic, Pulse Width Modulation (PWM)

ÖZ

GÜNEŞ UYGULAMALARI İÇİN ŞEBEKEYE BAĞLI ÜÇ FAZLI SiC TABANLI AKIM KAYNAKLI EVİRİCİ TASARIMI VE UYGULAMASI

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Aralık 2017, 110 sayfa

Bu tez çalışmasında, Akım Kaynaklı Eviriciye (AKE) dayalı üç fazlı şebekeye bağlı 20 kVA anma gücüne sahip bir çoklu-dize evirgecin analizi, tasarımı ve uygulanması gerçekleştirilmiştir. Geliştirilen evirici 400V gerilim seviyesinde paralellenerek ortak bir transformatör vasıtasıyla orta gerilime bağlanarak büyük ölçekli fotovoltaik (PV) uygulamalarda kullanılabilir. Eviricinin güç kademesi, temel tam köprü Akım Kaynaklı Çevirgeç (AKÇ) topolojisine dayalıdır. İki kutuplu voltaj bloke etme ve tek yönlü akım taşıma yeteneğine sahip olması gereken güç yarı iletkenleri, Silicon Carbide (SiC) MOSFET ve SiC Shottky Bariyer Diyotlarını (SBD) bağlayarak oluşturulur ve 25 kHz taşıyıcı frekansı ile Darbe Genişliği Kiplenimi (DGK) yöntemi kullanılarak anahtarlanmıştır.

Akım Kaynaklı Eviriciler (AKE), fotovoltaik uygulamalarda, tek kademeli çevirgeç yapısıyla tüm maksimum güç noktalarında çalışabilmeleri, doğrudan çıkış akımı kontrolü, kısmi çıkış güçlerinde düşük THD değerlerine ve basit çıkış filtre yapısına sahip olmaları gibi birçok avantaj sunmaktadırlar. Bu çalışmada elde edilen sonuçlar, SiC tabanlı yarıiletkenlerin kullanımının yaygınlaşması ile beraber, Akım Kaynaklı

Evirici (AKE) topolojisinin fotovoltaik uygulamalarda Gerilim Kaynaklı Eviricilere güçlü bir alternatif olabileceğini (GKE) göstermektedir.

Anahtar Kelimeler: Silisyum Karbür (SiC), Sebekeye Baglı Çoklu-Dize Evirici, Akım Kaynaklı Evirici (AKE), Fotovoltaik, Darbe Genişliği Kiplenimi (DGK)

To my family

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NOMENCLATURE

θ_s	*dq*-frame reference angle.
η	efficiency
η_{eu}	European efficiency
ω	*dq*-frame angular speed
d	subscript indicating *d*-axis component
q	subscript indicating *q*-axis component
C_{dc}	capacitance of the DC-link capacitor
C_d	capacitance of the damping capacitor
C_{ds}	output capacitance of the MOSFET
C_f	capacitance of the output filter capacitor
C_j	junction capacitance of the diode
f_c	corner frequency of low pass output filter
f_{cr}	frequency of carrier signal used in PWM
f_{sw}	switching frequency of the semiconductors
G	solar insolation/irradiation level
G_n	nominal solar insolation/irradiation level
I_{cnv}	CSI ac-side currents before the LC filter
I_L	DC-link current
I_c	current through the output filter capacitor
I_{dc}	mean DC-link current
I_{dc}*	DC-link current reference
I_{ds}	MOSFET drain source current
I_{mpp}	Maximum power point current
$I_{s,abc}$	output phase a, b, c currents
I_s	current injected into the grid
$I_{sn,abc}$	normalized output current references
I_0	diode saturation current
I_{ph}	the photo-generated current

I_{pv}	PV array current
L_{dc}	total inductance of DC-link reactor
L_f	inductance of the output filter inductor
L_s	leakage inductance of the source terminal
L_{bus}.	leakage inductance of the DC-buses
L_{tr}	transformer leakage inductance
L_{trc}	leakage inductance of the PCB traces
m	modulation index
N_s	number of series connected PV modules in a string
P_{in}	input power of the inverter
P_{loss}	inverter losses
P_{out}	output power of the inverter
R_d	damping resistance
R_g	external gate drive resistance
R_s	series resistance of the PV module
R_p	shunt resistance of the PV module
R_{tr}	winding resistance of the coupling transformer
T	surface temperature of the PV module
T_c	case temperature
T_j	junction temperature
T_n	surface temperature of the PV cells in STC
T_s	switching period
V_F	forward voltage drop of the diode
V_{drive}	gate driver voltage
V_{GS}	gate-source voltage of MOSFET
V_{dc}	DC-side voltage of the CSI.
V_{mpp}	maximum power point voltage
$V_{oc,n}$	open circuit voltage in STC
V_{pv}	voltage of the PV array
V_s	CSI AC-side terminal voltage

LIST OF ABBREVIATIONS

AC	Alternating Current
AEC	Aluminum Electrolytic Capacitor
CSC	Current Source Converter
CSI	Current Source Inverter
CCM	Continuous Conduction Mode
DCM	Discontinuous Conduction Mode
DSP	Digital Signal Processor
DC	Direct Current
ESR	Equivalent Series Resistance
ESL	Equivalent Series Inductance
FACTS	Flexible Ac Transmission System
GaN	Gallium Nitride
GWp	Giga Watt-peak
IGBT	Insulated-Gate Bipolar Transistor
kWp	Kilo Watt-peak
LCC	Life Cycle Costs
MDSPWM	Modified Dead-Band Sinusoidal PWM Technique
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MOV	Metal Oxide Varistors
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
MV	Medium Voltage
NOCT	Nominal Operating Cell Temperature
PCB	Printed Circuit Board
PI	Proportional-Integral
PLL	Phase Locked Loop
P&O	Perturb and Observe

PWM	Pulse Width Modulation
SBD	Schottky Barrier Diode
Si	Silicon
SiC	Silicon Carbide
SHEM	Selective Harmonic Elimination Method
SRFM	Synchronous Reference Frame Method
STC	Standard Test Conditions
SVPWM	Space Vector PWM
TDD	Total Demand Distortion
THD	Total Harmonic Distortion
TVS	Transient Voltage Suppressor
VSC	Voltage Source Converter
VSI	Voltage Source Inverter

CHAPTER 1

INTRODUCTION

1.1 Overview

It is a well-known fact that the energy demand of the world is increasing every year since the industrial revolution. For a long duration fossil based energy resources such as coal, natural gas and oil powered predominantly the world economy due to their relatively lower cost which is mainly associated with their extraction and shipping. However, as these commodities drain out, energy prices also incremented proportionally. The rapid consumption of traditional energy resources together with the increasing CO_2 concentration in the atmosphere has required diversifying from fossil fuels into alternative energy sources. In order to promote the continued expansion of renewable generation and to reduce foreign energy dependency, many countries offer tax breaks and financial incentives. Solar and other renewable energy sources have gained great attention recently because they are not only environmentally friendly but also economically profitable. As a result, overall installed capacity of the renewable energy resources excluding hydroelectric power plants accounts for %14 of the overall installed capacity of the world by the end of 2016 and it will continue to grow up [3].

Being the primary energy source of the Earth, the Sun itself can cover the current annual world energy demand with only 0.02% of the direct radiation on Earth surface. Photovoltaic (PV) cells can be utilized to convert solar energy directly to electricity, without requiring conversion to intermediate mechanical energy forms with zero emission during operation. PV cells have no moving parts and hence require very little maintenance and easy to operate. Module manufacturers also offer a long lifetime performance guarantee extending to 25 years.

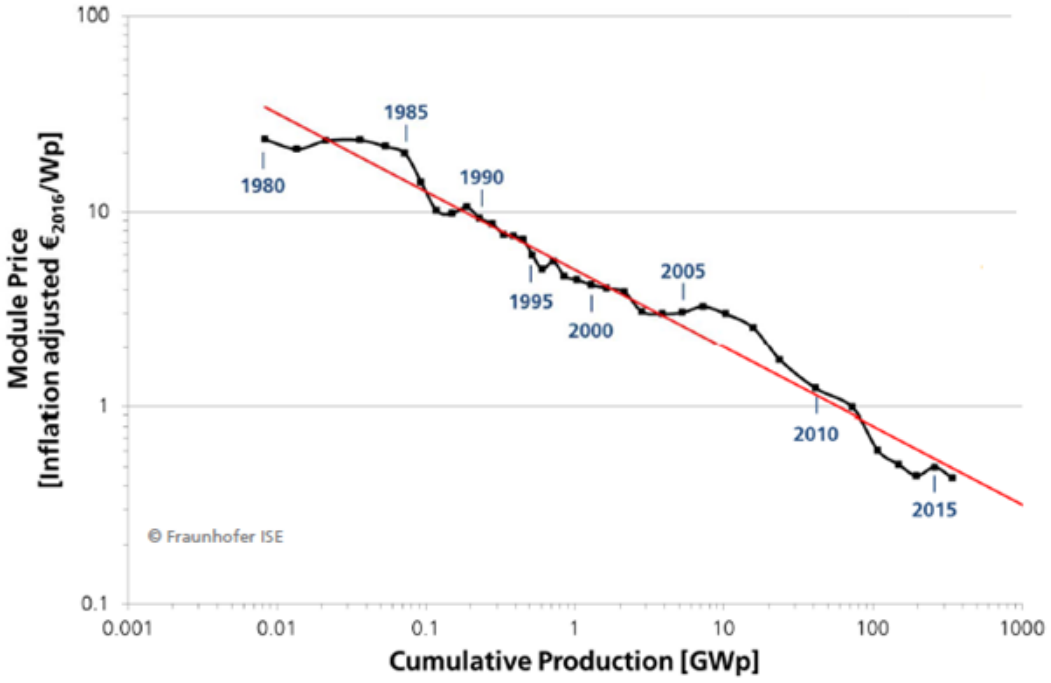


Figure 1.1 PV module price variation trend [6]

In the last 10 years, the efficiency of average commercial wafer-based silicon modules increased from 12% to 17% [6]. Despite all these features, utilization of PV systems for electricity generation was limited related to the high installation cost per unit energy ($/kWh) until a few years ago. However, as shown in Figure 1.1, declining PV module prices with the ever increasing module production in different parts of the world enabled solar electricity generation as a feasible and profitable option for electricity generation. The overall installed capacity of PV systems around the world already reached to 320 GWp in 2017 [6] and it will continue its boosted growth (see the Figure 1.2) in the future [3], [4].

Although there are some applications where PV modules are used for the electrification of dedicated DC loads via a suitable DC/DC converter, most of the PV systems deliver power in AC form. AC PV systems are classified as off-grid PV systems and grid-connected PV systems depending on the grid connection. Off-grid PV systems generally preferred to supply electricity to loads that are located at a considerable distance from utility electricity network as an alternative to extending the

power lines. Typically, they are sized up to 5 kWp and generally utilize a single phase inverter with battery storage to provide energy during low solar radiation [5]. On the other hand, grid-connected PV systems, which constitute the great majority, are installed to provide power to a grid-connected customer or directly to the utility electricity network. Grid-connected PV systems can be installed in various sizes, from small systems of a few hundred watts to very large-scale PV plants of hundreds of MWs [5]. Smaller grid-connected PV systems, which are also called as distributed PV systems, are generally integrated into existing residential, commercial, industrial or state buildings on the demand side of the electricity meter. Customer supplies energy from the utility grid during the absence of sunlight or low solar radiation, whilst exporting power to the network during sunny hours. On the other hand, centralized grid-connected PV systems are not associated with a particular electricity customer rather they perform as a power station. These systems are frequently installed on the ground [5].

PV modules, inverters, other balance of system (BOS) (such as cables, mechanical structure support, cabinets, etc.) are the major equipment of grid-connected PV system. Inverters are basically DC/AC converters which are widely used in industry for a long time.

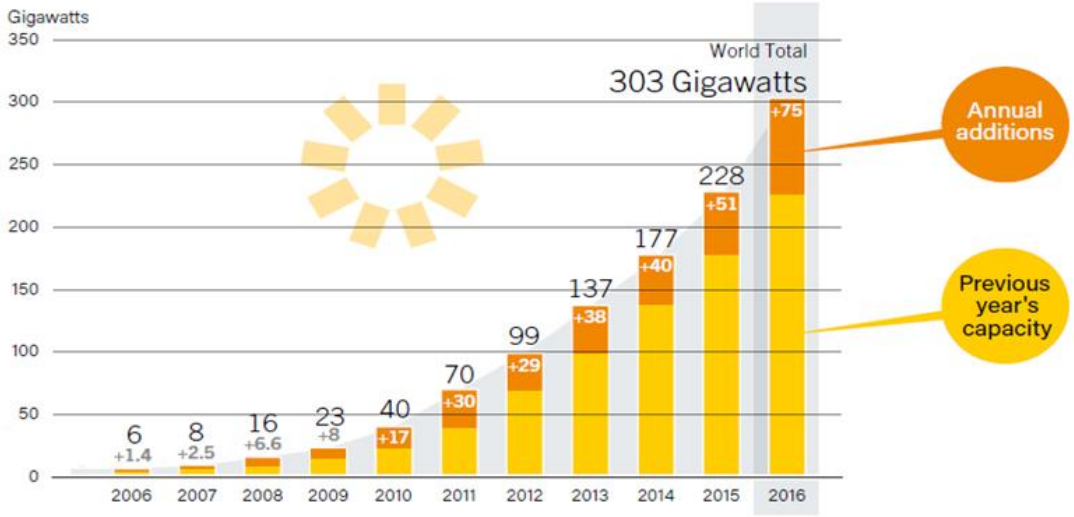


Figure 1.2 Solar PV Global Capacity and Annual Additions, 2006-2016 [3]

Main duties assigned to an inverter in a PV application can be outlined as follows:

- Extracting maximum power out of PV cells by tracking the power output and keeping PV modules at a suitable DC voltage level.
- Delivering a clean AC current at specified frequency to AC side with an acceptable harmonic content [8] in a safe and reliable manner.

Power rating of a standard PV module is typically lower than 300W. Thereby, PV systems are constructed with parallel and/or series connection of multiple PV modules in order to generate desired amount of output power. A number of series connected PV module array is named as PV string. Typically, a number of strings are connected in parallel to deliver a considerable amount of power to the utility network. There are mainly four dominant approaches for PV system construction as shown in Figure 1.3 [1]. While each arrangement utilizes at least one DC/AC converter, some structures include an additional DC/DC converter for input voltage adjustment and/or to prevent power losses caused by discrepancies between PV modules and non-uniform insolation caused by clouding and ghosting.

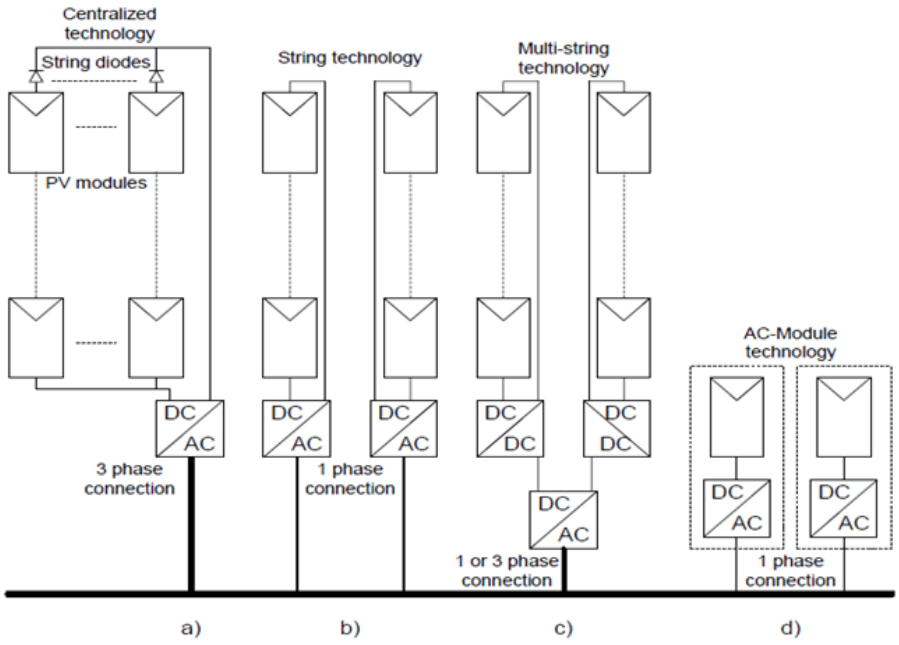


Figure 1.3 Photovoltaic system technologies. a) centralized technology, b) string technology, c) multi-string technology, d) AC-Module technology [7]

Each structure utilizes a different type of inverter and all have its own advantages and disadvantages [1]:

- ***Central inverters***: Central inverters typically employ three-phase connection and for these inverters, parallel PV strings are connected to one common central inverter. It's the lowest cost alternative for utility scale applications. Although they have a higher inverter efficiency compared to other types [6], it has some serious disadvantages which may result in a lower power yield since it requires very long DC cables between PV strings and the inverter, power losses on blocking diodes, input power deficiency due to a common MPPT, power loss due to module mismatch. Another disadvantage of central inverters is the decreased reliability since whole system relies on a single inverter [1].

- ***String inverter****:* They offer a more reliable and modular alternative for both distributed and centralized PV systems. They do not suffer from the deficiencies caused by blocking diodes and common MPPT. They are typically mounted on in the vicinity of its dedicated string hence they require shorter DC cables. Main disadvantage of string inverters is that the price per watt value is higher when compared to central inverters. In some European countries (e.g. Germany and Spain) galvanic isolation is not mandatory. Transformer can be removed from string inverter connection in order to further extend the conversion efficiency.

- ***Multi-String inverter****:* They stay between string inverters and central inverters when the power rating is considered. Price per watt value is close to the central inverters due to utilization of common inverter. Moreover, due to additional DC/DC converter units, they have the advantage of controlling each string separately over central inverters.

- ***Module inverter (micro-inverters)****:* Each inverter is dedicated to a separate PV module. No blocking diodes required for this configuration. Since each

PV module controlled by a separate MPPT control deficiencies caused by module mismatch is eliminated. Due to its modular structure, modification and maintenance of the system is easiest of all. Main drawbacks of this configuration are the highest price per watt value and the lower efficiencies resulted from large voltage amplification between input and output.

In the PV applications with a power rating lower than 10 kWp both three-phase and single phase connections are possible. Beyond that three-phase inverter topologies are more favorable due to reduced energy storage in the DC-link due to the constant power flow to the grid [22]. Some other important figures for commercially available state-of-the art products are listed in the Table 1 [6].

Table 1.1 Commercial Inverter Properties

Inverter Type	Power Range	Efficiency	Market Share	Remarks
String	< 100 kWp	up to 98%	~ 42%	7 - 20 €-cents /Wp Easy to replace
Central	100+ kWp	up to 98.5%	~ 54%	~ 6 €-cents /Wp Often sold only together with service contract
Micro	200-300W	90%-95%	~%1	~ 33 €-cents /Wp

1.2 PV Inverter Types

As pointed previously, installed capacity of the grid-connected PV systems is increasing very rapidly thanks to the advancing PV cell efficiencies and decreasing module prices as a consequence of increasing production and guaranteed life span of more than 20 years [22]. During the last decade, inverters have also improved significantly with a conversion efficiency up to 98.5 [6]. However, PV inverters are

still one of the less reliable part of a PV system with a typical lifetime of 3–7 years, above this duration increased failure rates are reported [9]. Moreover, with the increasing power ratings of PV systems, PV inverters are expected to carry some additional capabilities, like fault ride-through and reactive power injection. In order to promote the expansion of PV applications and to provide a reliable and efficient power conversion, continuous improvements in power electronics area also crucial [1]. Power electronics combines several disciplines such as semiconductors, control theory and power systems. Improvement of all primary converter performance measures such as efficiency, weight, volume, costs and reliability can be continued with improvements and innovations in these fields. For example, with the introduction of alternative semiconductor materials such as SiC and GaN in power electronics area, it is possible to design more compact and more efficient converters due to low switching losses [19,47,51].

Voltage source inverter (VSI) and current source inverter (CSI) are the two mainstream topologies for the grid-connected applications in the industry for a long time. VSI has been the most widely used power inverter topology in AC drive systems and grid-tied applications, while CSI is usually preferred in medium-voltage high-power electric drives and FACTS applications [2,13]. A qualitative comparison of corresponding topologies was presented in [18] and [23]. In a PV application, VSI topology encounters some problems. Ideally a DC-link voltage of 560V will be enough for the proper operation of VSI when connected to AC low-voltage bus. However, in practice voltage source inverters require a minimum 700-750V dc input voltage considering the %10 grid voltage tolerance together with the wide MPP (maximum power point) voltage range of the PV array. This high MPP voltage level will result in open circuit voltages above 1kV, which can be destructive for semiconductors and exceeds the 1kV system voltage limit. In order to operate with lower MPP voltages, VSI topology employed with an additional dc-dc boost converter (BC) or connected to the medium-voltage grid through special a step-up transformer in photovoltaic systems rated at high power levels. Another important problem with the employment of VSI topology is the requirement for large DC-link capacitor to minimize switching frequency voltage ripple on the dc bus voltage. High current ripple on the DC-link

capacitor in VSI compels the utilization of aluminum electrolytic capacitors (AEC) which are critical point of failure in PV inverters [9]. In order to overcome this problem, electrolytic capacitors either derated or replaced with more reliable film capacitors. However, both alternatives increase the size and cost of the PV inverter [9].

Alternatively, CSI topology employs an inductor as the DC-link energy storage element which acts as a constant current source with a low content. With an additional small film capacitor, PV current can be further smoothened in order to enhance MPPT efficiency. Therefore, CSI topology is expected to have a longer lifetime when compared to VSI based solar inverters [27]. Another feature of CSI topology which makes it a viable alternative for PV applications is its inherent voltage boosting functionality. A current source inverter can accept DC-link voltages up to a certain level (depends on the AC voltage level) eliminating the requirement for a DC/DC boost stage. Since CSIs operate with unidirectional DC-current, a series diode on the PV side to prevent reverse currents will not be required [21]. Finally, CSI topology is more advantageous over VSI in terms of short-circuit protection capabilities, direct output current controllability, and simpler AC filter structure [9]. In recent years, all these features attracted the attention of several researchers and several studies are conducted on the utilization of CSI in PV applications and presented in the literature.

Control, modeling and operation of three-phase pulse width modulated (PWM) current source converters in terms of active and reactive power control is presented in [10-15] and CSI modulation techniques are discussed in [14] and [15]. Dynamic modeling and performance during fault conditions of a CSI in a grid-connected PV system reported in [11], while in [9], [16] and [17] issues related to control and MPPT are discussed. In addition to high reliability, a solar inverter is expected to have high power conversion efficiency. Efficiency analysis of the current source topology for a module integrated inverter and for a string inverter performed in [18] and [26] respectively. However, in [26] results are not verified experimentally.

1.3 Scope of Thesis

Within the scope of this thesis, a single stage three-phase inverter with a power rating of 20 kVA and using PWM-CSI topology has been designed and implemented with the use of SiC semiconductors. Developed inverter is designed as a multi-string inverter to be used in high power PV plants. Prospective PV plant can be connected to medium voltage bus through a dedicated step-up transformer with a 0.4kV voltage rating at the converter side. Performance of the designed inverter has been evaluated in terms of power conversion efficiency and harmonic content of the output current on the laboratory prototype. The outline of this thesis is given as follows:

In chapter 2, system description and operation principles of CSI are explained briefly. After that, active and reactive power control method and reference current generation in synchronous reference frame is given. Finally, applicable modulation techniques are stated and a brief description of the employed modulation technique is presented in this chapter.

In Chapter 3, the design principles of CSI are presented. First, design specifications of the developed inverter in view of PV system requirements are stated. Then, the power switches are selected from commercially available SiC MOSFETs and SBDs with an efficiency oriented approach. In the next step, design of the DC-link filter, output filter, overvoltage protection circuit and passive damping circuitry have been presented. Later, design of the control system including maximum power point tracking is elaborated in company with required electronic control system. Finally, design of the power stage is explained in view of implemented layout practices to minimize commutation loop stray inductances.

In Chapter 4, experimental results obtained from the implemented prototype are presented with necessary figures, tables, and data.

In Chapter 5, general conclusions are given with some suggestions for future work.

CHAPTER 2

SYSTEM DESCRIPTION AND OPERATING PRINCIPLES OF PV-CSI

2.1 Introduction

In theory, an idealized current source inverter (see Figure 2.1) is able to generate any desired reference current waveform depending on the application purposes. A practical implementation of Current Source Inverter (CSI) requires a DC-link inductor at the input side to realize the nearly constant DC-link current. Numerous applications and detailed operation principles of CSI can be found in the literature [2], [9-15].

In a CSI, during certain sections of switching period, DC-link inductor is shorted in order to build up the DC-link current and in the remaining time, energy is released to the AC side. CSI operation is similar to the operation of DC-DC boost converter and this is why CSI is also called as boost inverter. Implicit voltage step-up capability of CSI makes it an appealing inverter topology for wide input voltage range photovoltaic (PV) applications.

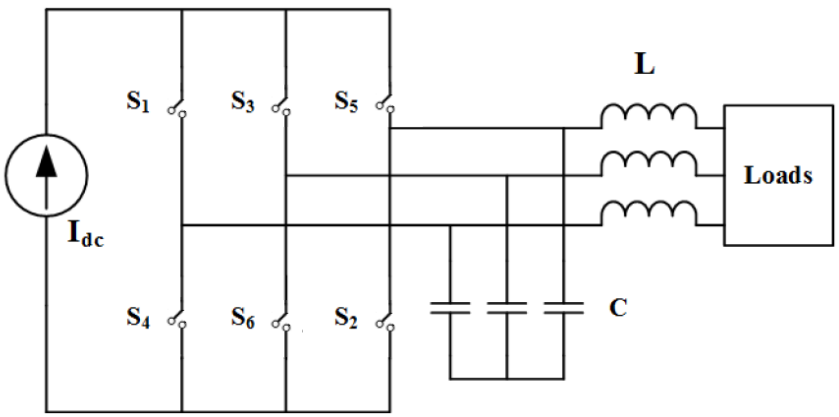


Figure 2.1 Ideal CSI Topology

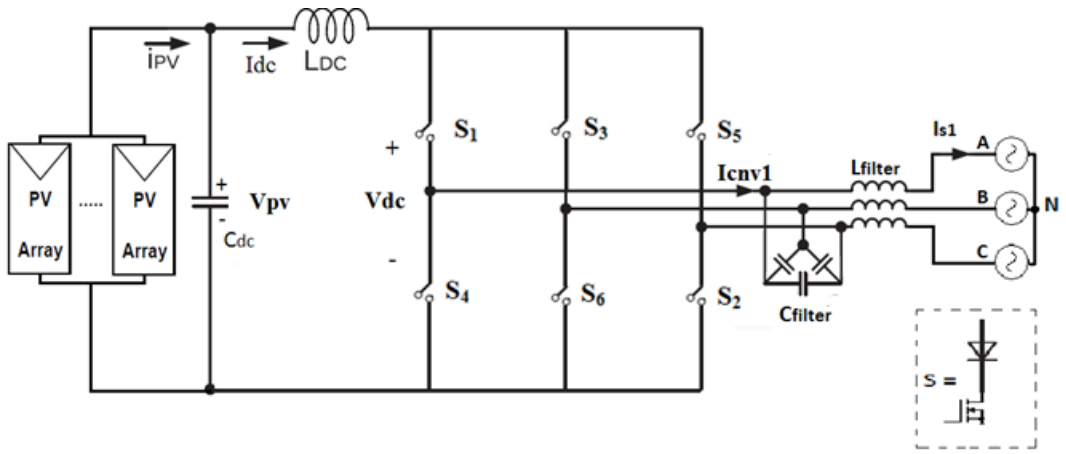


Figure 2.2 Circuit configuration of a three-phase CSI based PV system

In this chapter, the system description and operation principles of a PWM-controlled current source grid-connected PV inverter will be presented. After describing the basic circuit topology of the CSI based PV system, reference current generation including MPPT controller and waveform modulation methods will be described in detail. At the end of the chapter, a brief conclusion related to basic operation principles will be presented.

2.2 System Description

2.2.1 Basic Circuit Configuration

Circuit configuration of a grid-connected three-phase CSI based PV system is given in Figure 2.2. PWM-controlled CSI consists of six fully controllable power electronic switches. Since the voltage on each semiconductor switch can be either positive or negative and the current is unidirectional in a CSI topology, each switch should have unidirectional current carrying, and bipolar voltage blocking capability. In the power stage a series diode is connected to semiconductor switch unless the switch has reverse voltage blocking capability e.g., 1200V RB-IGBTs. CSI is fed from parallel connected PV strings through a DC-link inductor L_{dc}. Input current (I_{dc}) of the CSI which is almost constant during a switching period. A small capacitor is connected in parallel with the PV arrays in order to further smooth out the PV current drawn from the PV

array. Most of the time, CSI employs a second-order low-pass LC filter at the AC side in order to attenuate the switching frequency content of the output current.

2.2.1.1 Structure of PV Cells

A photovoltaic cell is basically a semiconductor diode whose p–n junction generates charge carriers when exposed to light generated when the energy of the incident photon is sufficient to detach the covalent electrons of the semiconductor [32]. This phenomenon depends on the semiconductor material and on the wavelength of the exposed radiation. A thin metallic grid on the front surface of the semiconductor collects free electrons. Figure 2.3 illustrates the simplified physical structure of a PV cell.

There are various types of semiconductor materials used in Photovoltaic cells. Currently, Silicon (Si) is the most widely used material for the manufacturing of PV cells and the great majority of commercially available products are in mono-crystalline and poly-crystalline silicon cells structure [6, 32].

From the power electronics perspective, knowledge on the electrical characteristics and equivalent modeling of PV devices is sufficient for the purpose of developing converters for PV systems.

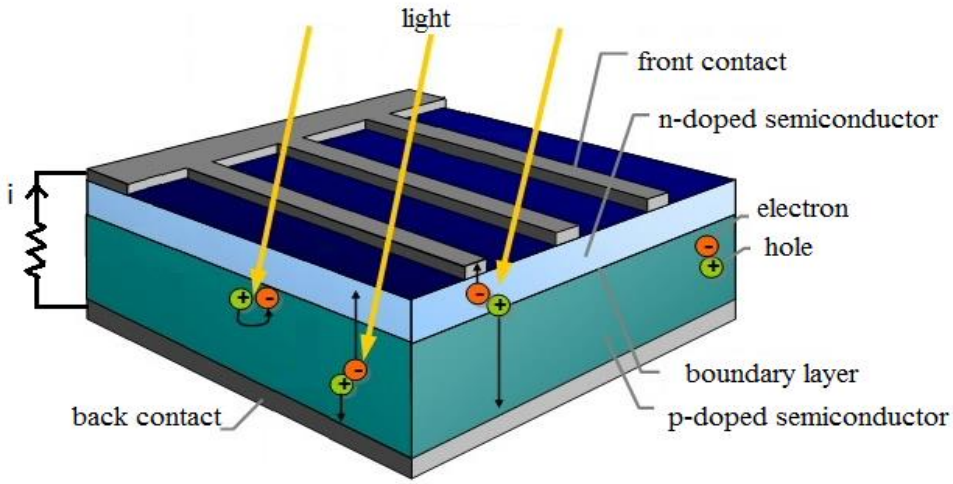


Figure 2.3 Physical structure of a PV cell

2.2.1.2 Electrical modeling of the PV Array

Simplified equivalent circuit of a PV cell (enclosed with dashed lines in Figure 2.4) is composed of a light dependent current source and a diode. The basic equation [32] that mathematically describes the I–V characteristic of the ideal PV cell is

$$I_{pv} = I_{ph} - I_0[e^{\frac{qV}{akT}} - 1] \tag{2.1}$$

Where I_{ph} is the photo current generated by the incident light whose magnitude is proportional to exposed light intensity. Negative part of the equation is the Shockley diode equation which represents the diode current Id. I_0 is the reverse saturation or leakage current of the diode, q is the electron charge (1.60217646 × 10−19 C), k is the Boltzmann constant (1.3806503 × 10−23 J/K), T (in Kelvin) is the temperature of the *p–n* junction, and a is the diode ideality constant whose value typically around 1.3 for poly-crystalline Si PV devices [32] and its exact value determined by empirical analysis.

A more realistic representation of a practical PV device requires additional resistive components to be included in the circuit, as shown in Figure 2.4.

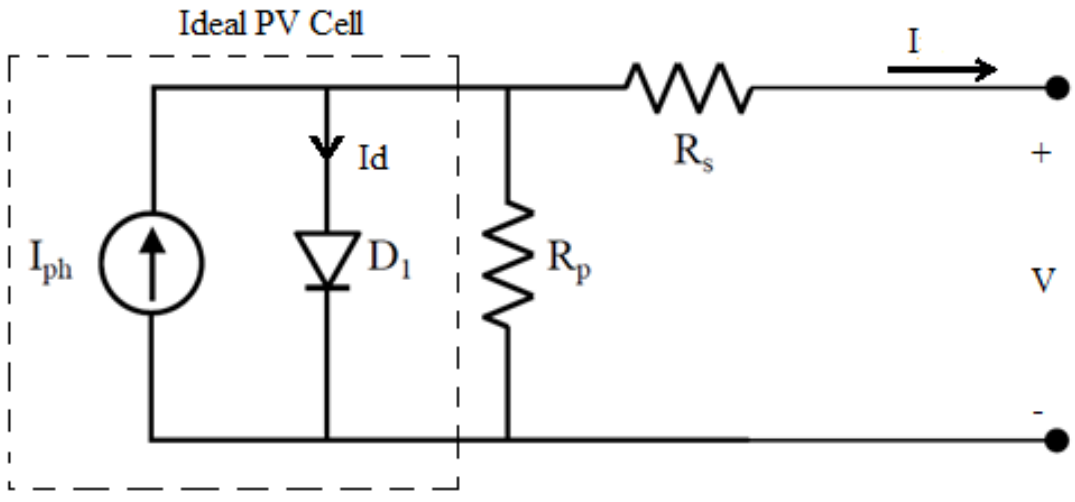


Figure 2.4 Equivalent circuit of a practical PV device

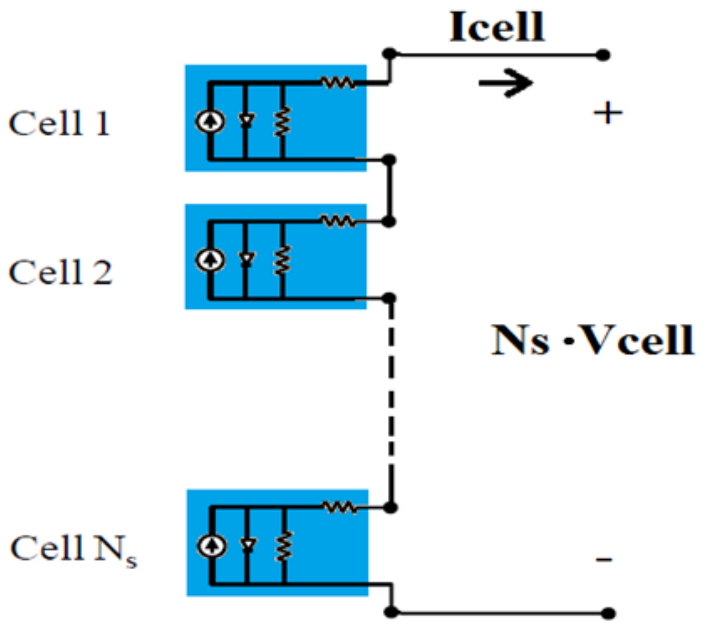
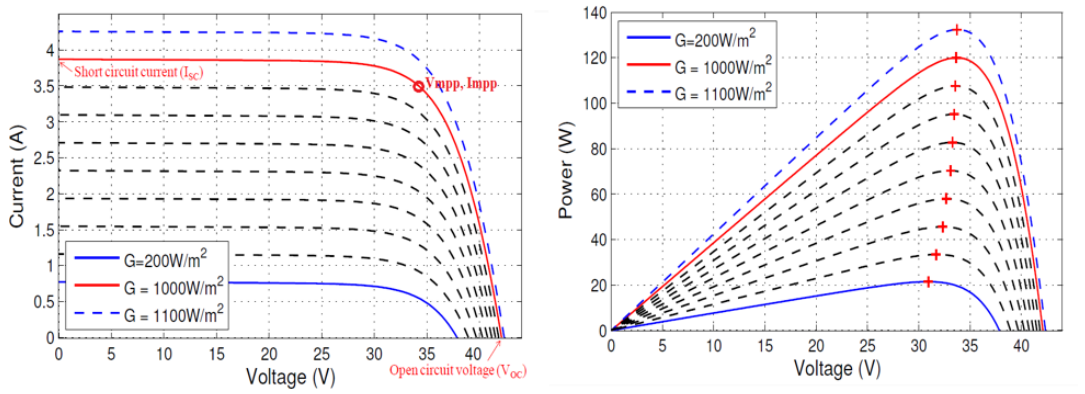


Figure 2.5 Structure of a PV module

Additionally, practical PV applications employ a series and parallel combination of several PV modules where a standard commercial PV module includes typically around 60 PV cells in series in order to obtain high PV voltages as shown in Figure 2.5.

Although there are more sophisticated models with better accuracy, addition of equivalent series resistance, R_s and equivalent parallel resistance, R_p, to the single-diode model in Figure 2.4 offers a fair compromise between accuracy and simplicity for the modeling of a PV module with N_s series connected cells. R_s basically depends on the contact resistance of the metal conductors with the p-type semiconductors, the resistances of the p and n bodies, and the resistance of the DC grid [32]. Then, corresponding equation defining I-V relation can be modified as [32].

$$I = I_{ph} - I_0[e^{\frac{V+R_sI}{V_t a}} - 1] - \frac{V + R_sI}{R_p} \tag{2.2}$$



(a) (b)

Figure 2.6 (a) I-V Characteristics of a small PV module, (b) MPP vs solar insolation

Maximum power point voltage, $V_{mpp,}$ of the PV array changes in a wide range under changing solar radiation level and PV cell temperature as it can be seen in Figure 2.6(b) and Figure 2.7 [45] respectively. Therefore, CSI based PV inverter should be able track MPP continuously and adjust the inverter input current in order to set the PV array operating point to V_{mpp}-I_{mpp}.

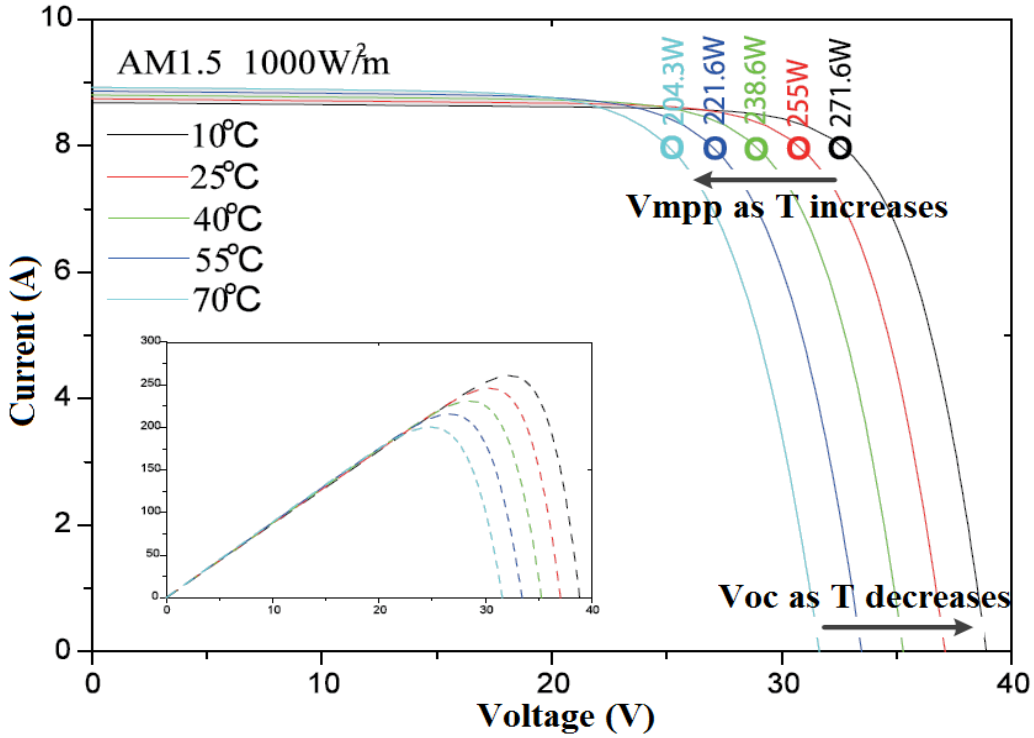


Figure 2.7 I-V characteristics of a PV module at different PV cell temperatures [45]

Additionally, since CSI is a boost type inverter, the maximum allowable series connected PV module count in the PV array must be specified considering MPP voltage at the lowest operating temperature. Therefore, electrical modeling of PV devices and extraction of corresponding I-V characteristics is an essential point in the design of PV system and determination of operating principles of the PV inverter. A more detailed explanation about PV array modeling and determination of the series module count in a CSI based PV system will be given in Chapter 3.

2.3 Basic Operation Principles

The schematic presented in Figure 2.8 illustrates the basic operation principles of a DC-link current-controlled current source PV inverter. The CSI control system is composed of mainly three parts: (i) MPPT controller, (ii) DC-link current controller and (iii) Pulse Width Modulation (PWM) block. The control of the CSI based PV system is mainly built on the control of DC-link current. CSI controller synthesizes the grid synchronized reference current waveforms using measured DC-link current

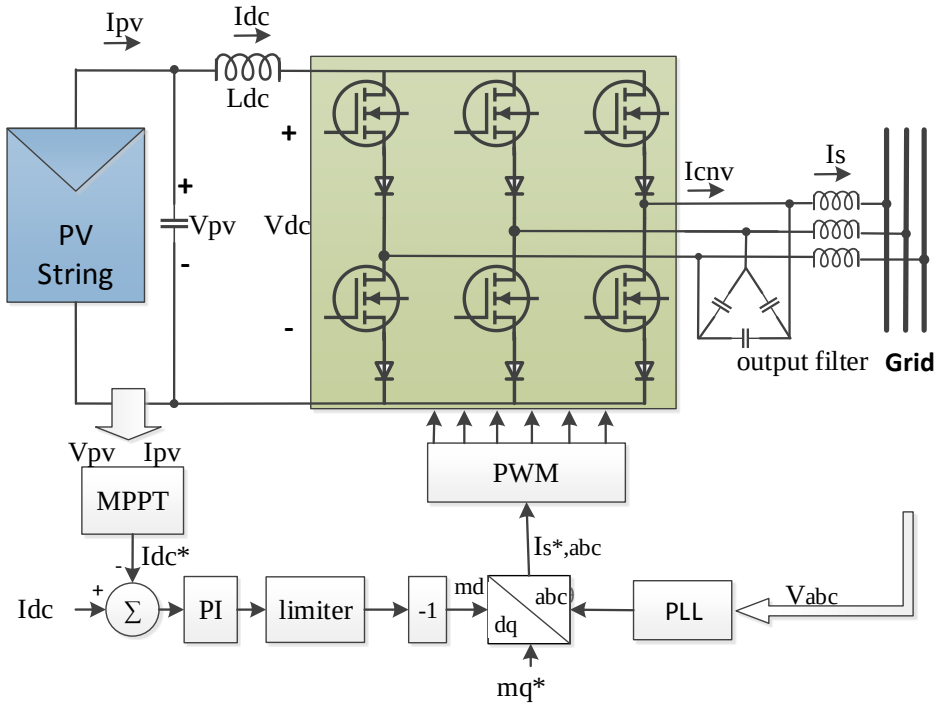


Figure 2.8 Block diagram of power control loop for PV-CSI

and appropriate modulation index generated by the PI controller whose reference is produced by the MPPT controller. As a matter of fact, a simple CSI based PV inverter is able to achieve both DC-link current control and MPPT control using a single DC current sensor with AC and DC voltage sensors without requiring additional sensors for ac current measurement [22]. This implies that the current source PV inverter potentially has a simple control circuit due to its direct current control feature.

2.3.1 MPPT Controller

As explained in section 2.2, appropriate level of the PV current varies with the ambient temperature and the insolation level. Therefore, Grid-connected PV CSI has to continuously track optimum operating point of the DC-link current and adjust modulation index *m* accordingly. There are various MPPT techniques in the literature and a good comparison of most notables is presented in [36]. The Perturb and Observe (P&O) technique is the simplest and most widely used MPPT technique among them.

For the perturb and observe MPPT technique, operating point continuously changed, depending on the resulting extracted PV power variation, direction of the operating point is decided for the next period of the MPPT controller. A flow chart is presented in Figure 2.9, which illustrates implementation of the perturb and observe algorithm on a current source inverter.

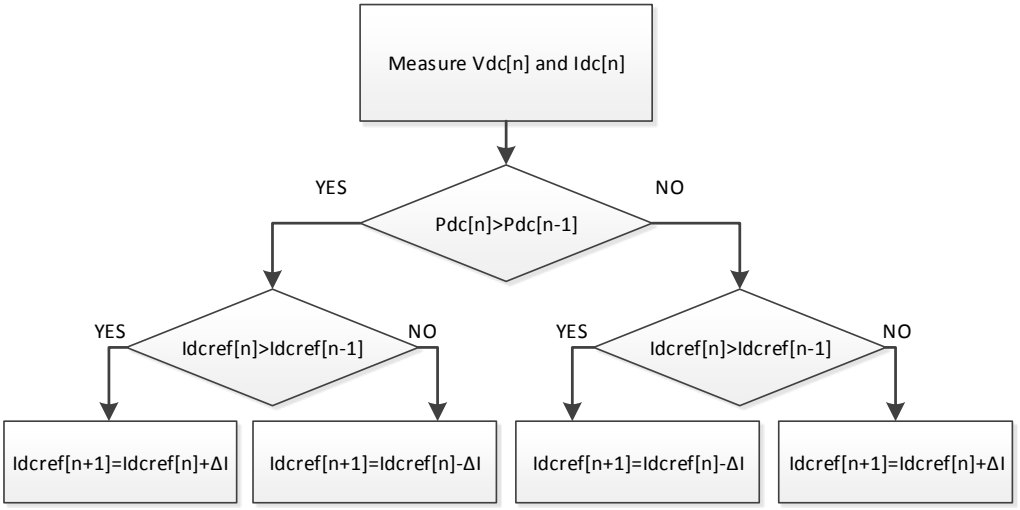


Figure 2.9 Flowchart of the Perturb and Observe algorithm

Implementation of perturb and observe MPPT technique in a current source can be summarized as follows: i) apply a step change in the DC-link current reference ii) if the applied perturbation results in an increase in the input power continue to increment/decrement DC-link current reference in the same direction, otherwise continue with the opposite direction. Gradually, operating point will converge to the MPP. However, in steady state, it will not coincide with the MPP exactly, but it will swing around it continuously.

2.3.2 Reference Current Generation

In order for the proper operation of the CSI based PV system, generation of correct reference current waveforms is another important issue. Due to the direct current control feature of the CSI, the shape of the output current waveform is heavily determined by the reference currents named as $I^*_{\mathrm{s,abc}}$ in Figure 2.8. and by adjusting modulation index and phase shift angle between the current references and the supply voltages, active and reactive power generated by the CSI can be adjusted to the desired levels.

Detailed explanation of decoupled control of current source converters presented in [11-13], [22] and [37]. For the scope of this thesis, emphasis mainly laid on the control of the active power generated by the CSI based PV system, assuming that the PV inverter should inject its current at unity power factor. Principles of reactive power control in a CSI are also addressed briefly, since the grid support by means of flexible reactive power support is gaining importance [18]. In the following subsection principles related to control of active and reactive power components in a CSI Based PV system will be elaborated using Synchronous Reference Frame Method (SRFM).

2.3.3 Active and Reactive Power Control

The use of reference frame theory has been used for a long time to ease the analysis of the electric machines. It is also a powerful tool for the digital implementation of control schemes for other grid connected systems. A number of reference frames have been proposed over the years; among them the stationary and synchronous reference frames are the two most commonly used methods [2]. SRFM provides the

representation of the AC currents and voltages in dc quantities, which enables simpler control system architecture. Grid voltages and currents which are AC side of the PV inverter can be represented as space vectors on a synchronously rotating reference frame. Angular frequency or angular velocity of this frame is defined with angular frequency of the grid. Details of the SRFM are explained qualitatively in [2].

As shown in Figure 2.10, each space vector is expressed in terms of its direct and quadrature components, which are located on the real axis and imaginary axis of the rotating frame, where v_s represents the supply voltages and I_s represents inverter output currents. In this representation, space vector of the grid voltage which is defined on the real axis of the rotating reference frame has only the direct axis component, v_{sd} and equal to the peak value of its phase quantities for balanced AC power system. Therefore, active and reactive power of the PV system can be expressed as [37].

$$P = \frac{3}{2}\mathrm{Re}\{\boldsymbol{v_s}.\boldsymbol{i_s^*}\} = \frac{3}{2}v_{sd}.I_{sd} \tag{2.3}$$

$$Q = \frac{3}{2}\mathrm{Im}\{\boldsymbol{v_s}.\boldsymbol{i_s^*}\} = \frac{3}{2}v_{sd}.I_{sq} \tag{2.4}$$

Equation (2.4) and (2.5) indicates that, active and reactive power output of the PV system reactive and a can be controlled by i_{sd} and i_{sq} respectively in a decoupled fashion.

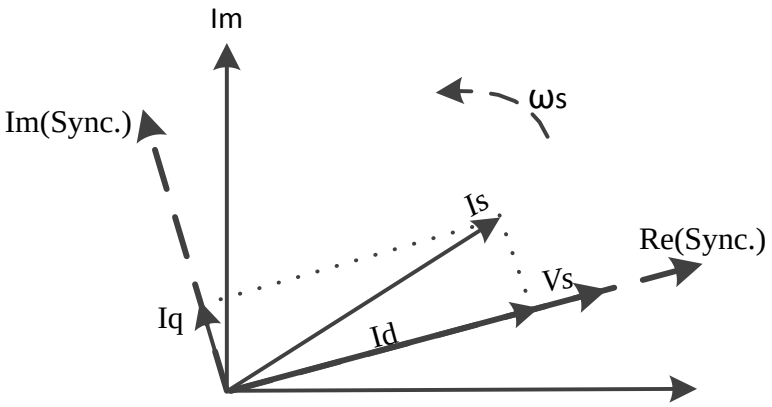


Figure 2.10 Grid Voltage Based Synchronous Reference Frame

The modulation index m (which is the product of the m_d and m_q and $0 \leq m \leq 1$) is defined by the ratio between the amplitude of the reference current signals and the DC-link current [11], where control signals m_d and m_q are obtained as

$$m_d = \frac{I_{cnvd}}{I_{dc}} \quad , \quad m_q = \frac{I_{cnvq}}{I_{dc}} \tag{2.5}$$

where I_{dc} represents DC-link current and I_{cnvd} and I_{cnvq} represents direct and quadrature components of converter currents I_{cnv} (see Figure 2.8) respectively. Since the output filter is aimed to be kept as small as possible for minimizing size of the PV inverter, fundamental frequency of the capacitor current, I_c becomes very small as compared to grid current, Is, and hence can be neglected for the sake of simplicity and converter operates at unity power factor, i.e. $I_{cnvq} = 0$. Then, Equation (2.6) can be modified as [11]

$$m_d = \frac{I_{sd}}{I_{dc}} \quad \text{and} \quad m_q = \frac{I_{sq}}{I_{dc}} = 0 \tag{2.6}$$

If the converter losses are neglected (i.e. conversion efficiency η=1) and using law of the conservation of energy with (2.4) and (2.7) the average value of rectified DC-link voltage (V_{dc}) can be expressed in terms of v_{sd} (equal to line-to-neutral peak voltage V_s) as

$$V_{dc} = \frac{3}{2} \, . v_{sd} . m_d \tag{2.7}$$

The relation between DC-link current and the modulation index can be established by solving the equilibrium equations for the continuous conduction mode (CCM). Change in the inductor current after a switching period (T_s) expired can be expressed by the following equation, as stated by [38]

$$\Delta I_L = \frac{T_s}{2L_{dc}} \left[V_{pv} \, - \frac{3}{2} \, v_{sd} m_d \, \right] \tag{2.8}$$

After applying a step increment to m_d, DC-link current settles to a lower value constituted by the V-I characteristics of the PV array after a certain duration. In a

similar fashion, DC-link current can be increased by decrementing m_{d}.Therefore, active power injected by the CSI, can be controlled by adjusting m_d with a single PI controller as shown in Figure 2.8. PI controller parameters will be tuned using Ziegler Nichols tuning rules [13]. Whereas reactive power output of the CSI, can be adjusted in an open-loop fashion by adjusting q-component I_{sq} as explained in [37].

2.3.4 Phase Locked Loop

The phase angle information is obtained by the Phase Locked Loop (PLL) algorithm and accurate and stable operation of the PLL is very crucial for the proper operation and control of the CSI. There have been many algorithms presented in the literature in order to extract the phase angle information as reviewed in [39]. Among them, Synchronous Reference Frame PLL (SRF-PLL) is a simple and effective method, and operation explained in [40] qualitatively. The basic block diagram of the SRF-PLL is given in Figure 2.11.

2.3.5 Pulse Width Modulation Techniques

The main duty of a Pulse Width Modulator is to produce appropriate switching signal set [S] tracking a given reference current vector, which then applied to the CSI in order to generate desired line currents as shown in Figure 2.12.

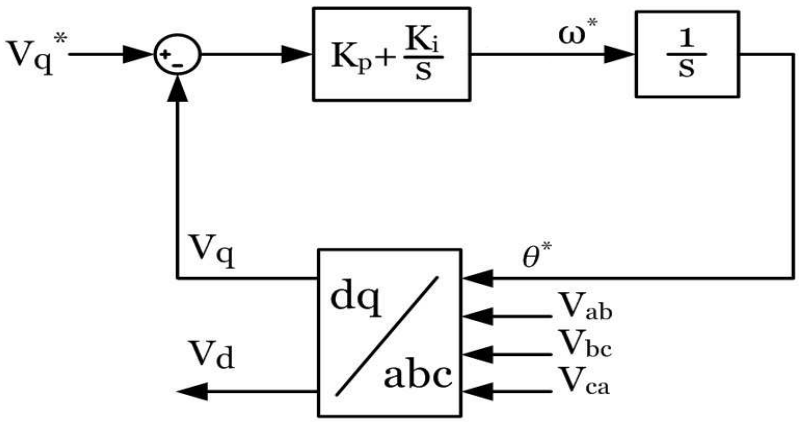


Figure 2.11 Block diagram of the PLL controller

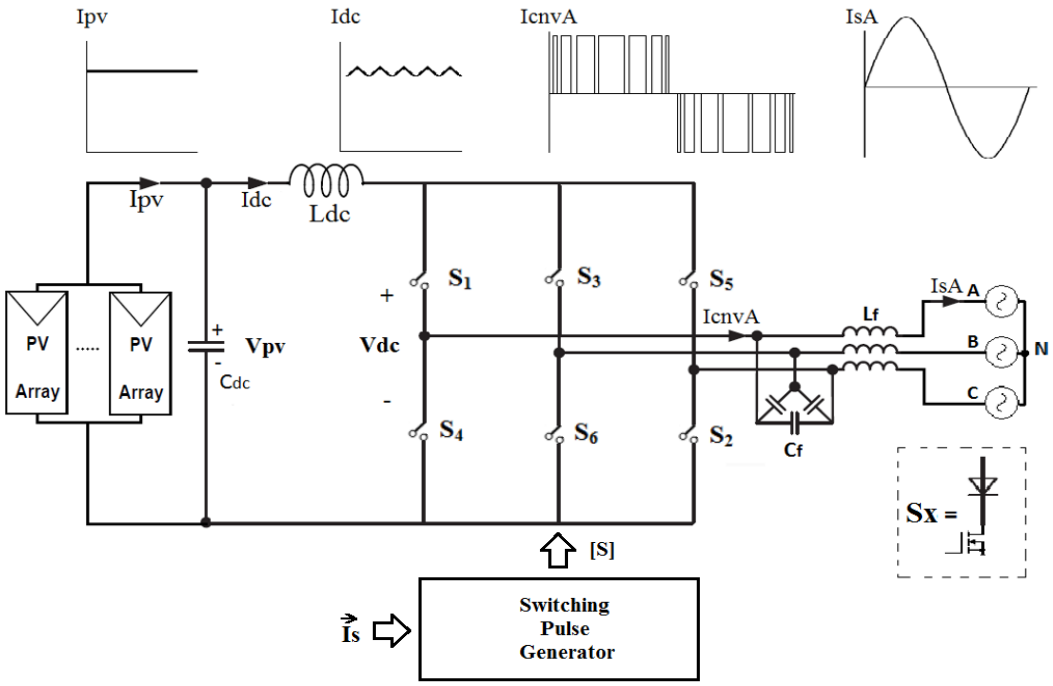


Figure 2.12 Pulse width modulation of output AC currents

Applied gating signal set must satisfy the following main constraints of the CSI: 1) since capacitors are employed at AC side in order to filter chopped PWM line currents, they must not be short-circuited which implies that, at most, one top (S1, S3, or S5, Fig. 2.12) and one bottom switch (S4, S6, or S2) should be closed at any time, 2) current source input cannot be opened; thereby, there must be at least one top (S1, S3, or S5) and one bottom switch (S4, S6, or S2) closed at all times in order to provide path for the DC-link current through the ac side. Combination of two constraints allows nine switching states for basic CSI modulation and corresponding states are listed in Table 2.1 [2], [12] and [15]. These switching states can be classified as zero switching states (state 7-9 in Table 2.1) and active switching states (state 1-6 as depicted in Table 2.1) [2].

The zero state signifies that a switch pair in a phase leg (i.e. S1 and S4 for phase A) conduct simultaneously and the other four switches in the inverter are off, leading to free-wheeling of the DC-link current through the conducting switch pair and $I_{cnvA}=I_{cnvB}=I_{cnvC}=0$. On the other hand, one upper leg and one bottom leg is in conduction for an active switching state. As an example, State 1 indicates that switch

*S*1 in leg A and *S*2 in leg C are in ON-state and the remaining four switches in the inverter are off. Then, the DC-link current I_{dc} flows through *S*1, output filter and the mains, *S*2, and then back to the dc source, resulting in $I_{cnvA} = I_{dc}$ and $I_{cnvB} = -I_{dc}$. The definition of other five active states is also given in the in Table 2.1.

Table 2.1 CSI Switching States

State	On Switches	I_{cnva}/I_{dc}	I_{cnvb}/I_{dc}	I_{cnvc}/I_{dc}
1	1-2	1	0	-1
2	2-3	0	1	-1
3	3-4	-1	1	0
4	4-5	-1	0	1
5	5-6	0	-1	1
6	6-7	1	-1	0
7	1-4	0	0	0
8	3-6	0	0	0
9	5-2	0	0	0

Various PWM techniques have been studied for CSCs, and the most widely used methods can be classified as: i) Sinusoidal PWM (SPWM) [15], ii) Space Vector PWM (SVPWM) [13,14,15,41], and iii) Selective Harmonic Elimination Method (SHEM) [2,13]. SHEM generally preferred at low switching frequencies in order to suppress low order harmonics frequencies in line current [13]. Carrier based modulation methods such as SPWM and its derivatives are well suited for analog applications with a free-running carrier signal. Direct implementation of enhanced control strategies and straightforward implementation opportunity in digital systems are the attractive features of SVPWM. Additionally, SVPWM decreases effective switching frequency, f_{sw} to the half of the carrier frequency, $f_{cr.}$ On the other hand, Modified Dead-Band SPWM (Dead-Band SPWM with a saw tooth carrier) technique [15], provide an easier implementation and similar performance with SVPWM in terms of harmonic spectra and reduction of switching losses. Therefore, it can be employed in the design of the PV-CSI. A more detailed comparison of the two modulation techniques is presented in [13,42].

2.3.6 Modified Dead-Band SPWM (MDSPWM)

Basic block diagram of the Modified Dead-Band SPWM (MDSPWM) is given in Figure 2.13 [15]. It has four fundamental blocks: Decoupling block, dead-band or modulating waveform generation block, tri-logic gating signals generator block, and shorting pulse generator block.

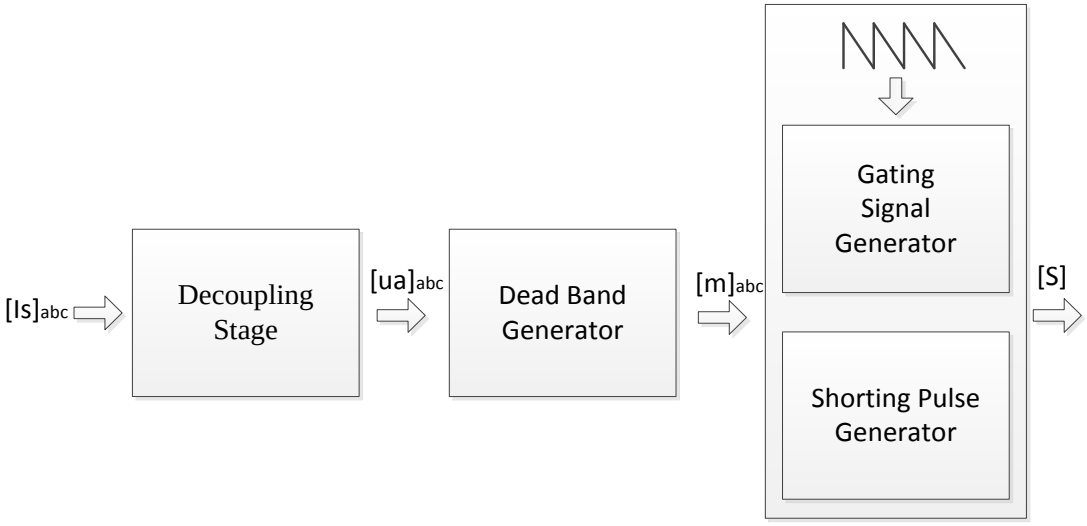


Figure 2.13 Simplified block diagram of the MDSPWM method

The main function of a switching pulse generator is to produce gating signals, when applied to a CSI generate line currents that follow a given set of normalized references $[I_{\mathrm{sn,abc}}]$. If the purpose of the switching pattern generator given in Figure 2.12 is attained, the inverter becomes a current amplifier characterized by:

$$I_{\mathrm{s,abc}} = G_{ac}.\,[I_{\mathrm{sn,abc}}\,]I_{dc} \tag{2.9}$$

Where $I_{\mathrm{s,abc}}$ is actual line currents in frame, $[I_{\mathrm{sn,abc}}]$ is the normalized line current reference vector, G_{ac} is the ac gain that depends upon the PWM technique[15] and equals 1.0 for the MDSPWM. The intersection of a carrier signal with modulating waveform references produces the switching signals per phase for a two level pattern (i.e. 0, 1). The line current of the converter can be expressed in terms of the DC-link current for each phase as follows:

$$I_{s,abc} = [Y]_{abc} I_{dc} \tag{2.10}$$

Where the elements of $[Y]_{abc}$ have three possible values: +1, 0, -1 depending on the switching pattern given in Table 2.1. Switching patterns of two phases are then combined to produce the basic switching pattern signals associated with a three level pattern [43]. Therefore, the generated line currents generated by the CSC and the modulating waveforms u_{abc} are related by the following expression [15]

$$I_{s,abc} = \frac{G}{\sqrt{3}} [T][u]_{abc} I_{dc} \tag{2.11}$$

$$[T] = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \tag{2.12}$$

Since in [T] is not diagonal, the line currents are coupled with respect to modulating waveforms , a decoupling block can be added to switching pattern generator in order to decouple line currents as a linear transformation given by

$$[u]_{abc} = [D][I_{sn,abc}] \text{ where } [D] = T^T \tag{2.13}$$

Finally, Dead-Band generator modifies modulating waveforms $[u]_{abc}$by adding a third harmonic component in order to increase ac gain *G* to 1.0 and to decrease switching frequency such that each switch is always on for 60^o and always off for 120^o in each switching period. A more detailed explanation of MDSPWM is presented in [15,43]

2.4 Summary

In this chapter, system description and operating principles of three-phase CSI based PV system have been presented. Principles of active and reactive power control in view of MPPT control and V-I characteristics of PV array has been demonstrated in rotating synchronous reference frame. Finally, a comparison of candidate CSI modulation techniques is presented. Among them, working mechanism of Modified Dead-band Sinusoidal PWM (MDSPWM), which is used in this study, has been explained briefly. It has been pointed that the MDSPWM provides a fair performance with the ease of implementation.

CHAPTER 3

DESIGN AND IMPLEMENTATION OF THE PV-CSI

3.1 Introduction

Operation principles and control of Current Source PV Inverter in view of modulation method, active and reactive power control technique and MPPT method is presented in Chapter 2. It has been noted that the fundamental duties assigned to a PV inverter as follows:

- Extracting maximum power out of PV cells by tracking the power output and keeping PV modules at a suitable DC voltage level.
- Delivering a clean AC current at specified frequency to AC side with an acceptable harmonic content (THD< 5%) [8] in a safe and reliable manner.

In this chapter, design objectives and implementation principles of the CSI based PV string inverter prototype will be presented. These theoretical methods are modeled and exercised by the aid of PSCAD/EMTDC simulation tool in order to meet the given requirements. As a first step, suitable PV array size will be determined considering the V-I characteristics of the PV array under different environmental conditions and CSI operation principles. To achieve this, an equivalent electrical model is constructed for the employed PV module in MATLAB. Modeling of the PV array is based on the datasheet parameters and equivalent circuit model of PV cell given in Chapter 2. Specifications of power switches are then determined in view of the semiconductor current and voltage levels obtained from the simulations. Among the commercially available SiC semiconductor devices, candidate MOSFETs and reverse blocking Schottky diodes are determined according to semiconductor losses which are calculated with the aid of PLECS. Design of the DC-link filter elements is performed

in the next step which includes determination of the DC-link inductance, L_{dc}, and DC-link capacitance considering peak-to-peak current ripple of the PV array. After that AC filter is designed and then the performance of the control system evaluated and tuned using PSCAD/EMTDC simulation software. Finally, implementation details related to the designed control system and laboratory prototype of the PV CSI are also described in this chapter.

3.2 Objectives and Specifications of the Design

Within the scope of this thesis, the prototype of CSI based multi-string inverter has been designed and developed with a power rating of 20 kVA and it can extract power from multiple of parallel connected PV strings. This inverter is intended to be used in utility scale PV applications which employ a dedicated coupling transformer. As shown in Figure 3.1, multiple of corresponding inverters can be connected in parallel at the low-voltage side (400V, 50 Hz) of the coupling transformer in order to constitute a high power PV system.

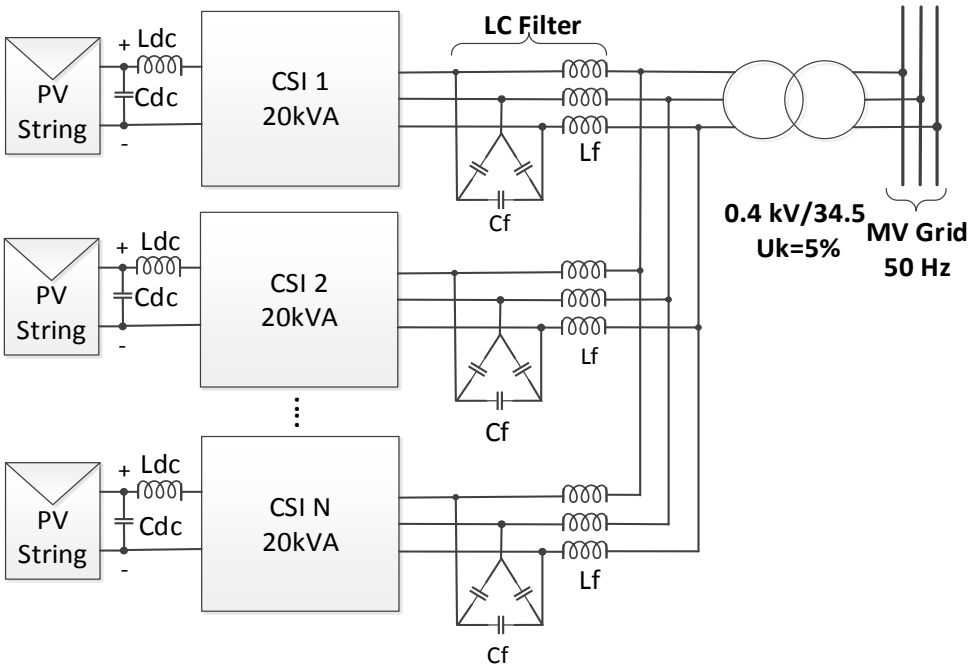


Figure 3.1 Typical large-scale PV power plant based on multi-string inverters

Electrical Characteristics at Standard Test Conditions (STC)

Module Type	CSUN265-60P	CSUN260-60P	CSUN255-60P
Maximum Power-Pmax (W)	265	260	255
Open Circuit Voltage - Voc (V)	37.8	37.7	37.5
Short Circuit Current - Isc (A)	9.01	8.95	8.88
Maximum Power Voltage - Vmpp (V)	30.5	30.3	30.1
Maximum Power Current - Impp (A)	8.69	8.58	8.47
Module Efficiency	16.32%	16.01%	15.70%

Standard Test Conditions [STC]: irradiance 1,000 W/m^2; AM 1,5G; module temperature 25°C. Measuring uncertainty of power is within ±3%.
Tolerance of Pmpp:0~+3%. Certified in accordance with IEC61215, IEC61730-1/2 and UL1703.

Electrical Characteristics at Nominal Operating Cell Temperature (NOCT)

Module Type	CSUN265-60P	CSUN260-60P	CSUN255-60P
Maximum Power-Pmax (W)	195	192	188
Open Circuit Voltage - Voc (V)	35.1	34.9	34.6
Short Circuit Current - Isc (A)	7.24	7.20	7.16
Maximum Power Voltage - Vmpp (V)	28.3	28.1	28.0
Maximum Power Current - Impp (A)	6.89	6.82	6.72

Nominal Operating Module Temperature(NOCT): irradiance 800W/m^2; wind speed 1m/s; ambient temperature 20°C.
Measuring uncertainty of power is within ±3%, Certified in accordance with IEC61215, IEC61730-1/2 and UL1703.

Temperature Characteristics

Voltage Temperature Coefficient	-0.292%/°C
Current Temperature Coefficient	+0.045%/°C
Power Temperature Coefficient	-0.408%/°C
NOCT	45±2°C

Maximum Ratings

Maximum system voltage(V)	1500(IEC)
Series fuse rating(A)	20

Figure 3.2 Electrical characteristics of CSUN255-60P [45]

Using the equation (2.7) it's found that for a linear operation, maximum value of DC-link input of CSI is limited to 489.9V in a 400V AC system, which determines the maximum allowable MPP voltage of the PV system. On the other hand, minimum DC-link operating voltage of PV-CSI strictly depends on the number of series connected PV modules and MPP voltage variation of PV modules with respect to the variations in the operating temperature and solar insolation level. Therefore, in order to specify the input voltage range of the PV inverter, characteristics of employed PV module must be known for all environmental conditions.

However, commercial PV manufacturers generally provide typical specifications of PV modules under specific test conditions rather than the equivalent model and corresponding parameters in their datasheets. As an example, electrical characteristics of employed PV module (CSUN255-60P which is composed of 60 series PV cells) under Standard Test Conditions (STC) and under Nominal Operating Cell Temperature (NOCT) are given in Figure 3.2 [45].

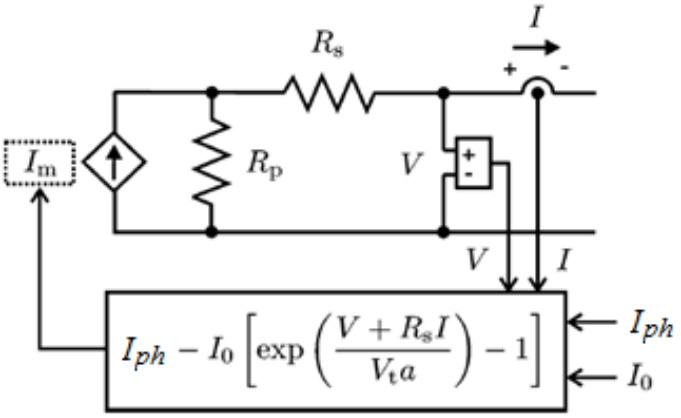


Figure 3.3 PV module equivalent simulation model

Therefore, development of equivalent electrical model of the PV array and corresponding equations are prerequisite for both simulation work and determination of the input specifications. Development of equivalent electrical model of PV arrays was explained briefly in Section 2.2. In this section, an equivalent electrical model, which is illustrated in Figure 3.3, for the employed PV module (CSUN255-60P) will be developed combining the principles given in Section 2.2 and the corresponding PV module characteristics under STC [45] using MATLAB. In order to use in simulations, the I-V characteristics of the PV module can be estimated with the aid of developed electrical model for different temperatures and solar insolation levels.

In section 2.2, it is explained that I-V characteristics of a PV device can be obtained with equation 2.2. In this equation, the assumption $I_{sc} \approx I_{ph}$ is generally used in the modeling of PV devices because in practical devices the series resistance, R_s, is low and the parallel resistance, R_p, is high [32].

Additionally, effect of solar insolation and PV cell temperature on photovoltaic current can be approximated as

$$I_{\mathrm{ph}} = \left(I_{sc,n} + K_{\mathrm{i}}.\,\Delta T\right)\frac{G}{G_{\mathrm{n}}} \tag{3.1}$$

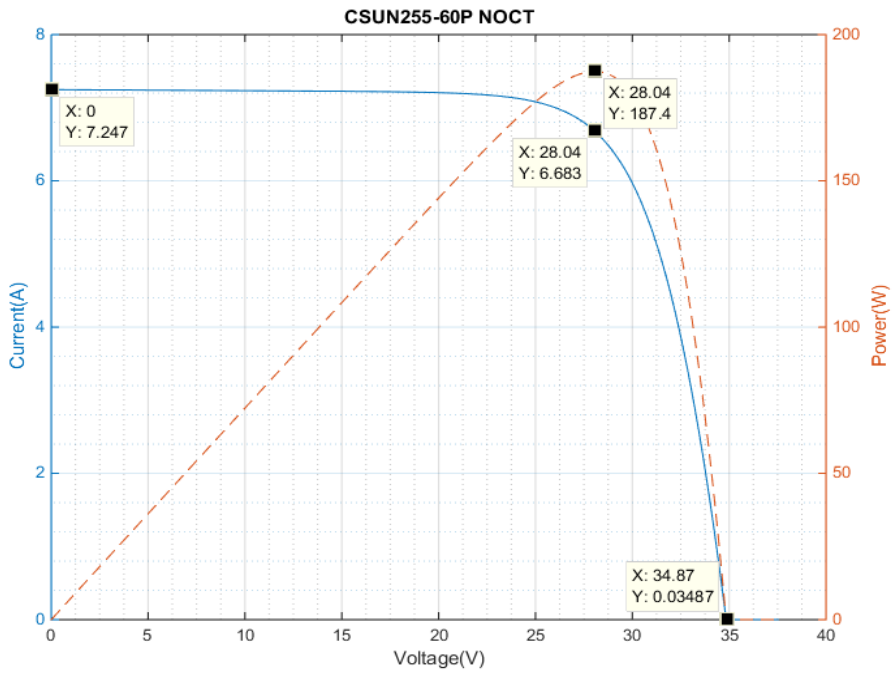


Figure 3.4 P–V and I-V curves of CSUN255-60P at NOCT (800W/m^2 and 45 ^{o}C)

where $I_{ph,n} \approx I_{sc,n}$ (in amperes) is the light-generated current at the nominal condition (usually 25 ^{o}C and 1000 W/m2), G (watts per square meters) is the irradiation on the device surface, and G_n is the nominal irradiation (1000 W/m2), K_i is the temperature coefficient of the current, ΔT is the temperature difference between actual (T) and nominal (T_n) temperatures in Kelvin. Saturation current can be approximated as [32]

$$I_0 = \left(I_{sc,n} + K_i \Delta_T\right) / \left(e^{\frac{V_{oc,n} + K_V \Delta_T}{a V_t}} - 1\right) \tag{3.2}$$

where K_V is open-circuit voltage temperature coefficient.

Finally, as explained in [32], R_s and R_p can be found iteratively, based on the fact that there is an only pair $\{R_s, R_p\}$ that warranties that the maximum power at the (V_{mpp}, I_{mpp}) point of the I–V curve which is calculated by the mathematical model is equal to the maximum experimental power from the datasheet at the same point.

I-V and P-V curves at NOCT (800W/m^2 and ^{o}45) are then sketched by using the developed model for CSUN255-60P PV module is given in Figure 3.4. When they are compared with the datasheet values given in Figure 3.2, it has been seen that developed model gives nearly the same values with the manufacturer data for the remarkable points such as PV module short circuit current, I_{sc}, open circuit voltage, V_{oc}, maximum power point voltage, V_{mpp}, and maximum power point current, I_{mpp}, with an acceptable error. Therefore, developed model can be used to obtain I-V characteristics of the corresponding PV module at different temperature and irradiation levels in order to be used in simulation studies Additionally, this model is also very helpful for obtaining MPP voltage range corresponding to the practical operating values of the PV module surface temperature and solar insolation level which are very essential for the determination maximum number of PV modules that can be connected in series.

Variation of MPP voltage with respect to PV cell temperature and solar insolation is given in Table 3.1. At low operating temperatures, MPP voltage of the PV array should not be higher than the maximum possible DC-link voltage of CSI, which is found to be 489.9V when operating in a 400V AC system, in order to extract maximum power. Otherwise, connection of excessive number of series modules will result in an output power lower than the available PV power when operating at low temperatures. Therefore, by taking maximum MPP voltage of the corresponding module as 32V, the maximum number of series connected modules in a PV string can be found as 15. As a result, a voltage variation between 345V-483V is expected at the DC-link of the CSI.

Table 3.1 Change of the MPP voltage with solar insolation and PV module surface temperature

	10 ^{o}C	**25 ^{o}C**	**45 ^{o}C**	**55 ^{o}C**	**70 ^{o}C**
200 W/m^2	30.3 V	28.5 V	26 V	24.8 V	23 V
400 W/m^2	31.4 V	29.5 V	27.2 V	26 V	24.2 V
600 W/m^2	31.9 V	30.0 V	27.7 V	26.6 V	24.9 V
800 W/m^2	32.2 V	30.3 V	28.0 V	27.1 V	25.2 V
1000 W/m^2	32.25 V	30.5 V	28.3 V	26.9 V	25.5 V

Rated power of the inverter can be obtained by employing five parallel strings each including 15 series connected PV modules. When corresponding PV array is constructed by using CSUN255-60P, DC-link parameters at steady state under STC will be as follows:

$$P_{\mathrm{dc}} = 15 * 5 * 255\mathrm{W} = 19.125\ \mathrm{kW} \tag{3.3}$$

$$I_{\mathrm{mpp}} = 5 * 8.47\mathrm{A} = 42.35\ \mathrm{A} \tag{3.4}$$

$$V_{\mathrm{mpp}} = 15 * 30.5\mathrm{V} = 451.5\ \mathrm{V} \tag{3.5}$$

and specifications of the developed inverter is then can be constituted as in Table 3.2.

Table 3.2 Specifications of the Designed PV-CSI

Power Rating	20 kVA
Supply Voltage	Three-phase, 400V
Max DC Current	42 A
Max DC Voltage	< 490V
Current THD	< 5%
Operating Temperature	< 45 ºC

3.3 Selection of Semiconductor Devices

SiC based power semiconductors in comparison with Si based ones can be listed as follows [19], [47-51]:

- Higher breakdown voltage due to the higher electric breakdown field of the material. Thus much higher doping levels can be achieved and a thinner semiconductor chip is used to achieve the same breakdown voltage like in Si. This results in a lower on-resistance which implies lower conduction losses.

- Higher power density of the device may be achieved due to higher thermal conductivity of SiC-semiconductor.
- These devices can operate at higher switching frequency (lower switching losses) due to the higher saturation electron drift velocity, thinner semiconductor chip and higher thermal conductivity.

SiC Junction Barrier Schottky (JBS) diodes are a majority current carriers, thus do not store charge in their junctions. The reverse recovery charge in the SiC Schottky diode is extremely low and is only the result of the junction capacitance. As a result, they have far superior switching performance than comparably rated bipolar Si PiN counterparts [48]. Furthermore, unlike the silicon PiN diode, the reverse recovery characteristics of SiC Schottkys is independent of forward current and junction temperature [54]. Currently, SiC is a very expensive material to produce power electronic devices in comparison with Si, for devices based on SiC wafers to become more cost competitive and SiC wafer sizes and device yield per wafer have to be increased in order to make SiC cost competitive with Si. [47]. However, when the complete system cost is considered, SiC based design can still have lower overall component costs and in the long term it can be distinctly advantageous due to increased efficiency when the photovoltaic applications is considered [49, 56, 57].

As one of the main motivations behind this thesis work is the investigation of the performance of SiC semiconductors in a CSI based PV inverter, the aim is to design an inverter entirely of SiC power semiconductors, including both the semiconductor switches and the blocking diodes.

3.3.1 Voltage Rating

In a CSI, since the semiconductor switches exposed to line-to-line grid voltages in their off state, semiconductor voltage rating should be higher than the maximum peak value of the rated mains voltage. Considering the permissible mains voltage variation of ±%10, selected SiC MOSFET and diode have to withstand permanent maximum blocking voltage of $\hat{V} = \sqrt{2} * 400 * 1.1$ =620V during normal operation.

Considering recommended 2/3 derating of semiconductor devices [18, 53], operation with 900-V semiconductors is allowed for this application. However, currently 900-V SiC devices are not available commercially at this power range and for the simplicity of the design device paralleling is not considered; therefore, 1200V is selected as the semiconductor blocking voltage rating. If the voltage spikes due to high rate of change of current (di/dt) and parasitic inductances on commutation paths, this selection will provide enough space to be on safe side.

3.3.2 Current Rating

As expressed previously, efficiency is one of the primary objectives for the photovoltaic applications along with the system cost. Since the semiconductors losses constitute the dominant part of converter losses, it needs to be considered primarily. In high efficiency converters, power devices can be paralleled or overrated in order to reduce the power losses at the expense of increased converter cost. Paralleling devices will reduce on-state resistance and conduction loss but switching losses may increase slightly [55]. However, this requires a detailed optimization between initial component costs and life cycle costs (LCC) caused by converter losses. A detailed optimization study for PV converters is presented in [49]. In this study, semiconductors are selected in a way that their junction temperature will be around 125◦C (at an ambient temperature of 45◦C) since the voltage drop of both SiC diode and SiC MOSFET increases with increasing junction temperature as shown in Figure 3.11.

As specified in Table 3.2, rated DC-link current value of the CSI is expected to be around 42A which flows through one upper bridge leg and one lower bridge leg. As a starting point, pulsed drain current rating of the MOSFET and repetitive peak forward current rating of the diode must be higher than the maximum DC-link current. However, for a proper device selection, a detailed thermal analysis should be carried out for the candidate semiconductors. Considering the specified junction temperature (125 ^{o}C) candidate SiC MOSFETs (C2M0080120D, C2M0040120D and C2M0025120D from CREE) and candidate SiC diodes (C4D20120D, C4D30120D, C4D40120D from CREE) have been evaluated, and then C4D40120D (diode) rated as 1200V, 54A at T_c=135^{o}C and C2M0040120D (MOSFET) rated as 1200V,

$R_{DS(on)}$=40mΩ have been chosen to be used in the PV-CSI prototype. Both of the devices are in TO-247-3 package. Calculation of the semiconductor losses and the thermal analysis with the selected semiconductor devices will be given in the following section.

3.3.3 Semiconductor Losses

- **Conduction Losses**

In conventional CSI topology, there are two conducting transistors and two diodes at any given time and each bridge leg carries DC-link current for the same amount of time throughout a power cycle. In other words, each phase leg is ON-state during one-third of the grid period independent of the duty cycle. Since the designed CSI is planned to be operated in CCM with a small DC-link current ripple, its effect on the rms value of semiconductor currents is neglected. Then, total MOSFET and diode conduction losses can be expressed as:

$$P_{\text{cond\_mosfet}}=6*\frac{1}{3}*R_{\text{ds,on}}*{I_{\text{dc}}}^{2} \tag{3.6}$$

$$P_{\text{cond\_diode}}=6*\frac{1}{3}*V_{\text{F}}*I_{\text{dc}} \tag{3.7}$$

- **Switching Losses**

Switching frequency of each power semiconductor pairs, i.e., SiC MOSFET and Si Schottky Diode, is half of the carrier frequency, f_c, in MDSPWM which has been chosen as the modulation technique in this research work. Moreover, one third of the commutations occur under negative voltage as illustrated in Figure 3.5. In a CSI, if the voltage blocked by the switch that is to be turned on is negative before the commutation, turn-off losses will appear in the corresponding semiconductor to be turned off. If the voltage across the switch which is about to be turned on is positive turn-on losses are generated in the same semiconductor [58]. Therefore, regarding the calculation of switching losses it is difficult to find accurate analytical expressions for device currents and voltages during the switch commutations [38]. Instead of that, a simulation software (i.e. PLECS) can be used in order to calculate switching losses.

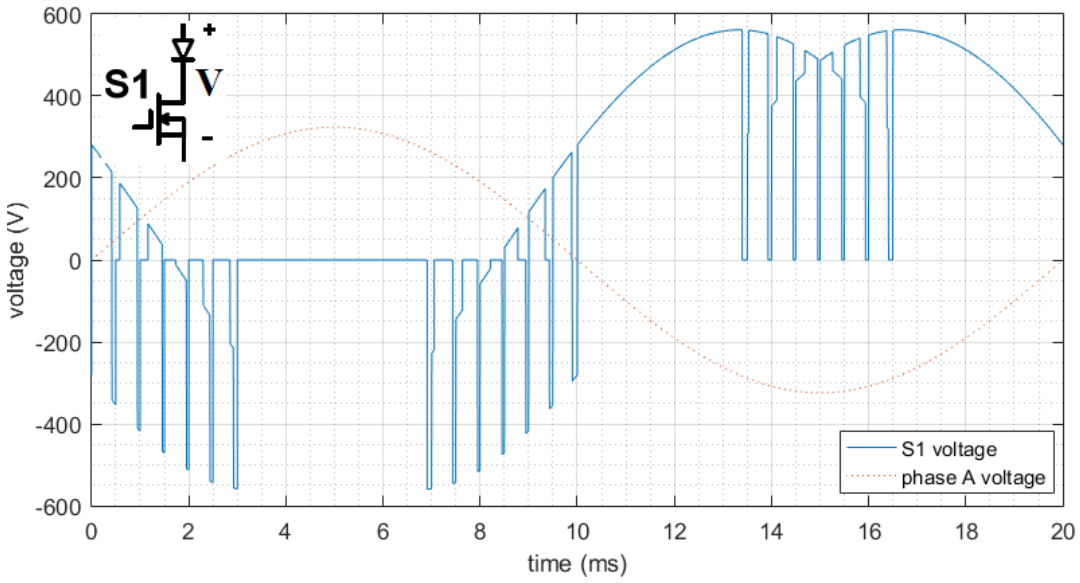


Figure 3.5 Switching voltages of S1 during one grid cycle at unity power factor for m=0.9 and f_{cr}=2 kHz

PLECS specify the ON-state voltage used for the conduction loss calculation as an arbitrary function of device current and the device temperature which is obtained by interpolation of provided datasheet values. In a similar approach, switching losses can be calculated by adding switching energies for each switching instance over a power cycle. These switching energies are found from the datasheet by considering pre- and post-switching voltages, currents, external gate resistance and junction temperature [59]. As an example, Figure 3.6 shows turn-on and -off switching energy losses for the selected MOSFET (C2M0040120D) depending on pre- and post-switching voltages, currents and junction temperature.

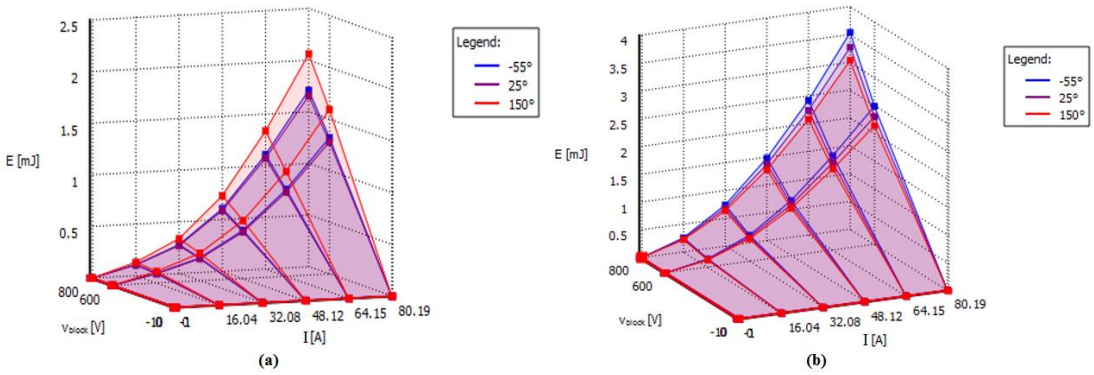


Figure 3.6 Look-up table for switching losses a) turn-off losses b) turn-on losses

Using PLECS, overall semiconductor losses are calculated for different carrier frequencies at rated mains voltage, taking m=1.0 (corresponds to V_{dc}=489V), I_{dc}=42A, junction temperature of MOSFETs as 120 ^{o}C, external gate resistor R_g=22 ohm (selection of external gate resistor will be explained in section 3.8) and corresponding switching loss data is depicted in Figure 3.7. Since the DC-link current ripple and voltage ripple on the output filter capacitors are ignored in these calculations, switching losses increase linearly with the increasing carrier frequency.

Generally, the selection of switching frequency should be performed for the overall system considering power devices' switching losses and passive components' losses together. With higher switching frequencies, power devices' switching losses will be larger, but the loss of DC-link inductor will be smaller because a smaller DC-link inductor value could be selected. However, after a certain point, gain from the passive component losses will be much smaller than increased switching losses. After evaluating the data depicted in Figure 3.7, 25 kHz is selected to be the carrier frequency of the CSI in order to achieve a fair compromise between switching losses and the passive component losses and size. Then, semiconductor losses are calculated by using PLECS for different I_{dc} values for m=1.0 (V_{dc}=489 V) and calculated losses are depicted in Figure 3.8.

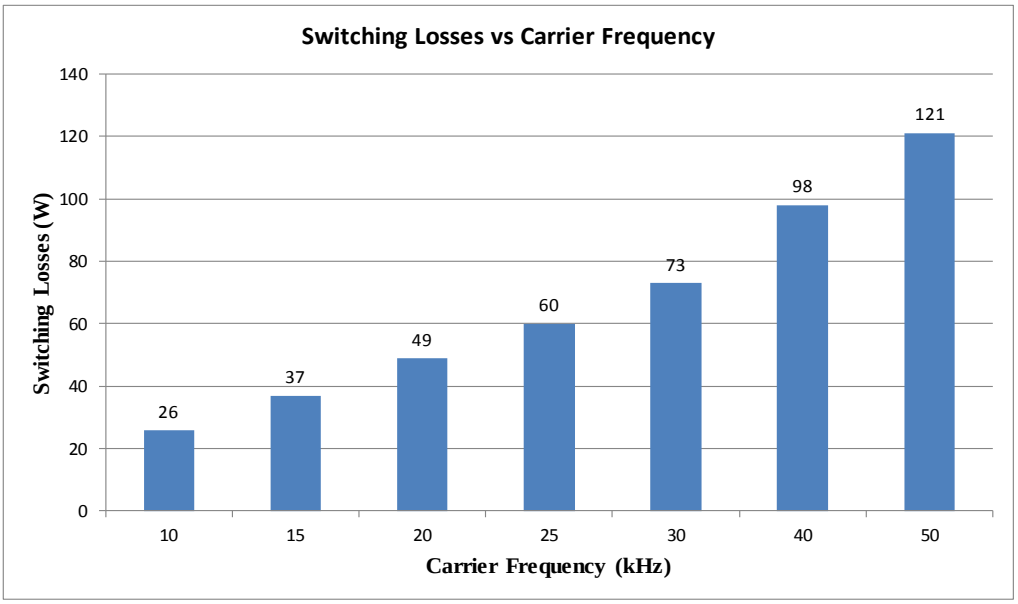


Figure 3.7 Switching losses for different carrier frequencies

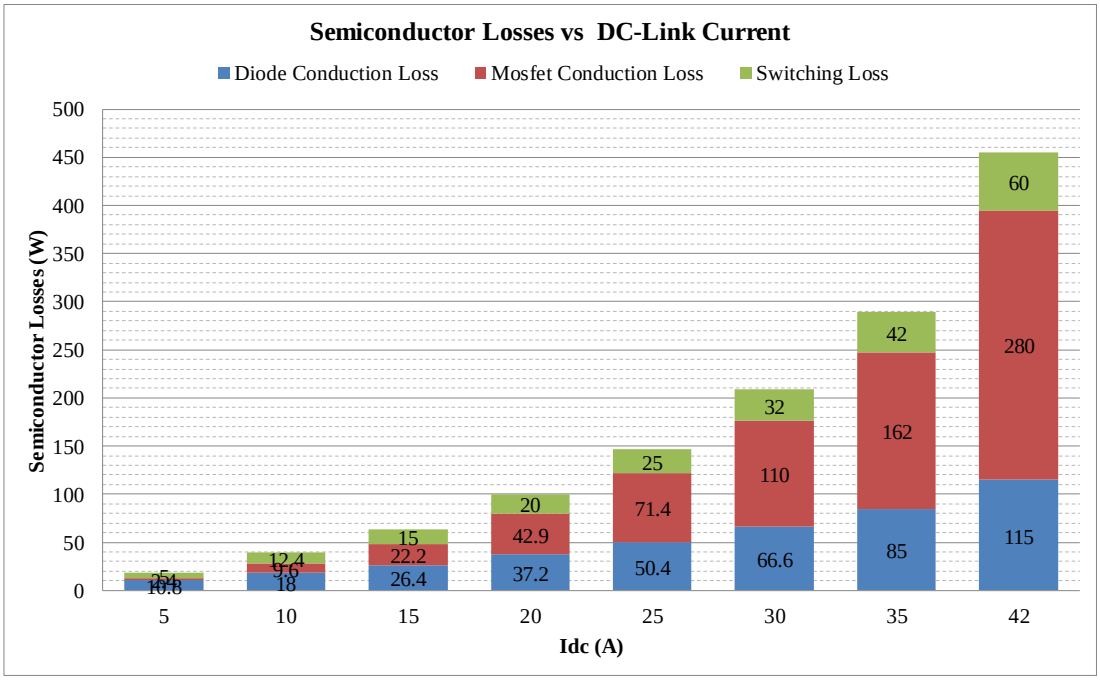


Figure 3.8 Details of semiconductor losses for different DC-link current values

Simulations also shows that the semiconductor losses remain unchanged as the modulation index decreases provided that I_{dc} remains constant. On the other hand, with the decreasing modulation index as result of decreasing MPP voltage of the PV array, P_{dc} or P_{in} also decreases although the I_{dc} remains unchanged. Therefore, efficiency of PV CSI decreases for low modulation indices.

3.4 Design of the Cooling System

Thermal structure of the power stage is given in Figure 3.10. In the developed PV-CSI prototype all semiconductor devices are mounted on a common 150x244mm heatsink (864AS from ARMA Elektronik). The power devices are soldered to the power stage of the CSI from the bottom side. Then, the semiconductor devices are fixed on the top surface of the heatsink using screws.

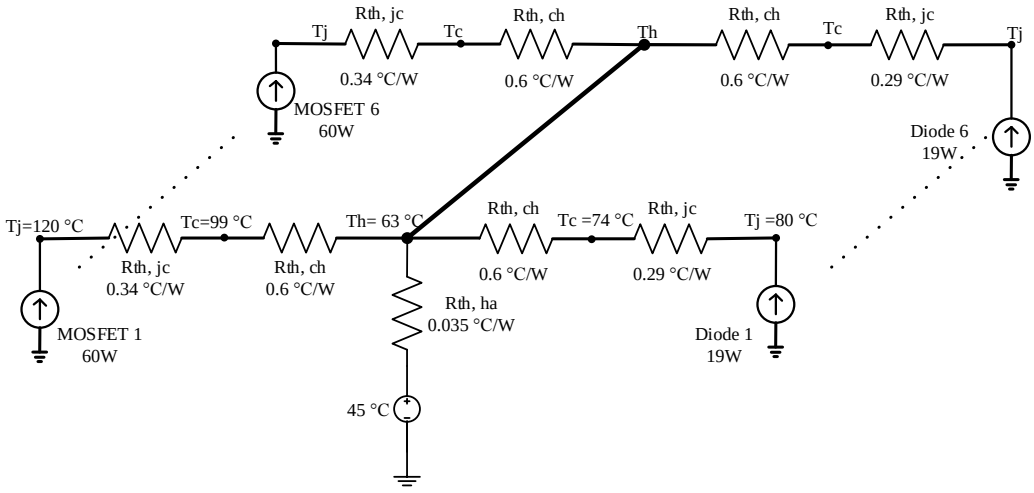


Figure 3.9 Steady-state thermal model

In order to electrically insulate case of semiconductors from common heatsink, Sil-Pad 600 thermal pads are placed between the semiconductors and the surface of the heatsink. Cooling system includes two 120x120mm axial fans in order to obtain an air velocity of 2 m/s. Total power consumption of the fans are measured to be 10W. Steady state thermal model of the cooling system is given in Figure 3.9, in this model $R_{th,jc}$, $R_{th,ch}$ and $R_{th,ha}$ represents steady state semiconductor junction to case thermal impedance, case to heatsink thermal impedance and heatsink to ambient thermal impedances respectively. The maximum junction temperature of MOSFETs is expected to be around 120 ^{o}C and maximum junction temperature of diodes is expected to be around 80 ^{o}C. Corresponding ON-state operating points of the semiconductors are shown on the forward characteristics curves of the corresponding devices in Figure 3.11

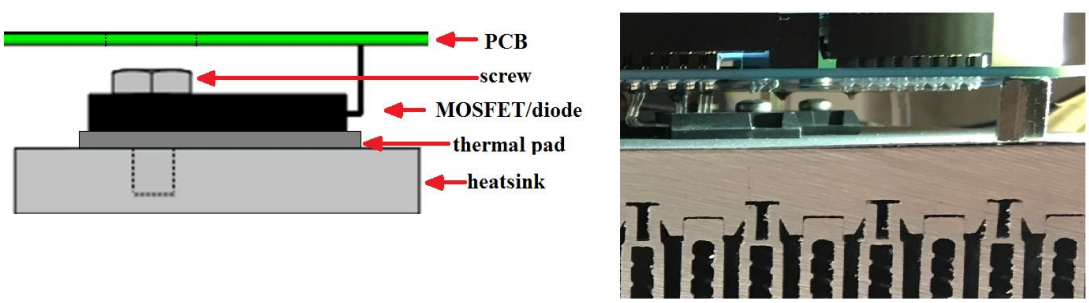


Figure 3.10 Mechanical and electrical connections of the semiconductors

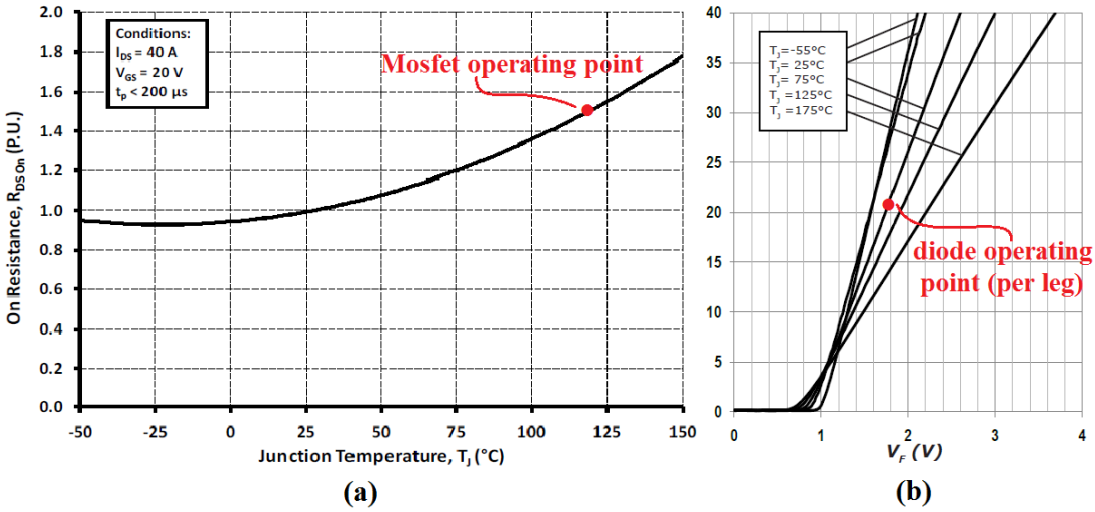


Figure 3.11 ON-state operating points of (a) C2M0040120D, (b) each leg of C4D40120D at rated DC-link current (I_{dc}=42A)

3.5 DC-Link Filter Design

3.5.1 DC-Link Inductor Design

As the energy storage element of the CSI, DC-link inductor has significant contribution to the total power loss, weight and volume of the CSI. The maximum duration of zero state (i.e. free-wheeling) occurs when *dq*-frame reference angle is at an angle of $n * \pi/3$ with respect to α-axis, where the inductor current ripple is given by:

$$\Delta I_{\mathrm{L}}{}^{\mathrm{pp}} = \frac{V_{\mathrm{pv}} * \left(1 - m * \sin\left(\frac{\pi}{3}\right)\right) * T_{\mathrm{s}}}{L_{\mathrm{dc}}} \tag{3.8}$$

In order operate in CCM at low irradiation levels and in order to decrease semiconductor rms currents, DC-link current ripple $\Delta I_{\mathrm{L}}{}^{\mathrm{p-p}}$ is specified as 5% of rated DC-link current. Then, using (3.8) L_{dc} is found to be 2.2 mH by taking expected minimum DC-link voltage as 392V and corresponding modulation index as 0.8.

Therefore, the current carried by the DC-link inductor comprised of a large DC component with a small high frequency AC component at the rated power. There are many types of magnetic materials used in inductor design, including laminated steel,

tape wound materials (silicon steel, amorphous alloy, nanocrystalline alloy etc.), powdered iron, powder core materials (Kool Mμ, sendust), MPP (molypermalloy), High Flux, XFLUX) and ferrite products. Iron powder cores and laminated steel have been neglected due to the comparably high core losses. Remaining three core types are compared in [60], considering the construction of AC boost inductors of a 20 kW voltage-source PWM converter with peak fundamental phase current rating of 41 A.

Achieved minimum volumes of inductors constructed with these three different core materials for the same power loss specification are presented in Figure 3.12 [60]. In this figure, inductance value varies as a function of switching frequency and current ripple and the graph titled as “Best” shows the achievable minimum volumes and the appropriate material type for various DC-link current ripple and switching frequency values by combining the data presented in the remaining three graphs. It has seen that at low DC-link current ripple values the smallest inductor volume for a given power loss specification or from another perspective, for the same inductor size minimum inductor power loss is achieved with tape wound cores.

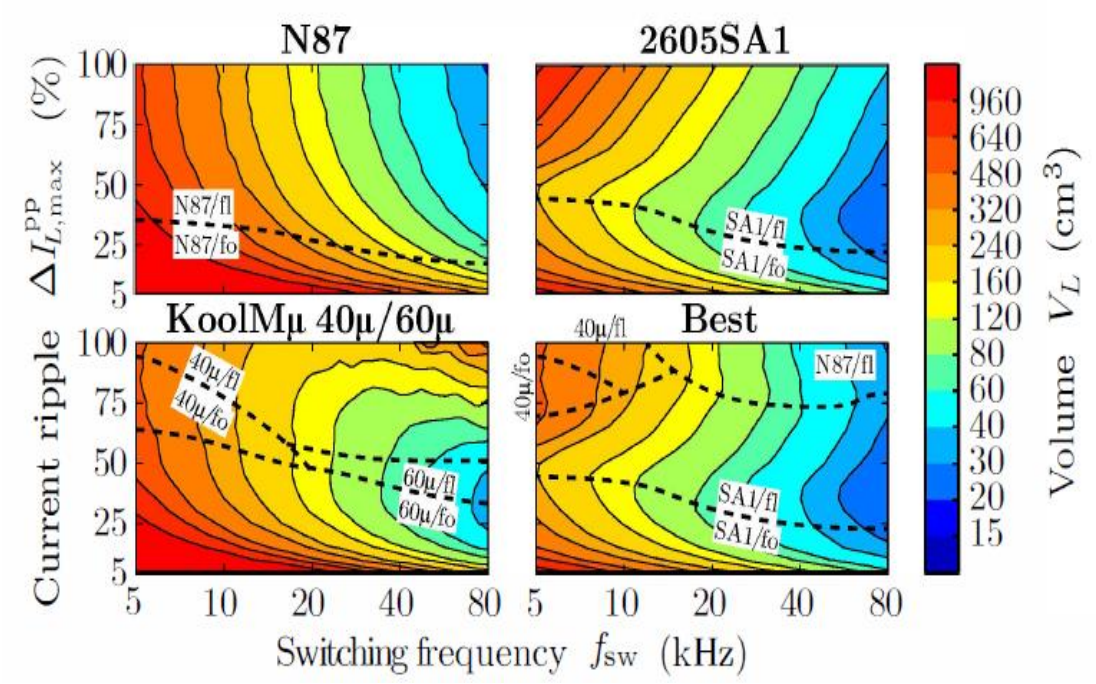


Figure 3.12 Achievable minimum volumes at fixed power loss for powder core (KoolMμ), Ferrite (N87) and tape wound (2605SA1) core materials [60]

As a result, in order to minimize power losses of DC-link inductor, high saturation flux density (1.56 T) amorphous alloy 2605SA1 [62] from Metglas has been selected as the core material.

Using the DC Reactor Design Tool [63] software provided by the manufacturer, AMCC-500 is selected as the DC-link inductor core by resizing inductance to 2.0 mH. Copper foil is decided to be used because of its superior filling factors and easiness of construction and decreased high frequency losses caused by skin effect when compared to of solid wire [55]. Designed inductor (see Figure 3.13) has 64 turns of 0.2mm x 6cm copper foil windings with a total air gap of 3mm.

In practice, the DC-link inductor is usually split into two parts and shared between positive and negative DC-link terminals as shown in Figure 3.14. In this way, leakage currents flowing through parasitic capacitances of PV array and transformer windings can be minimized [70].

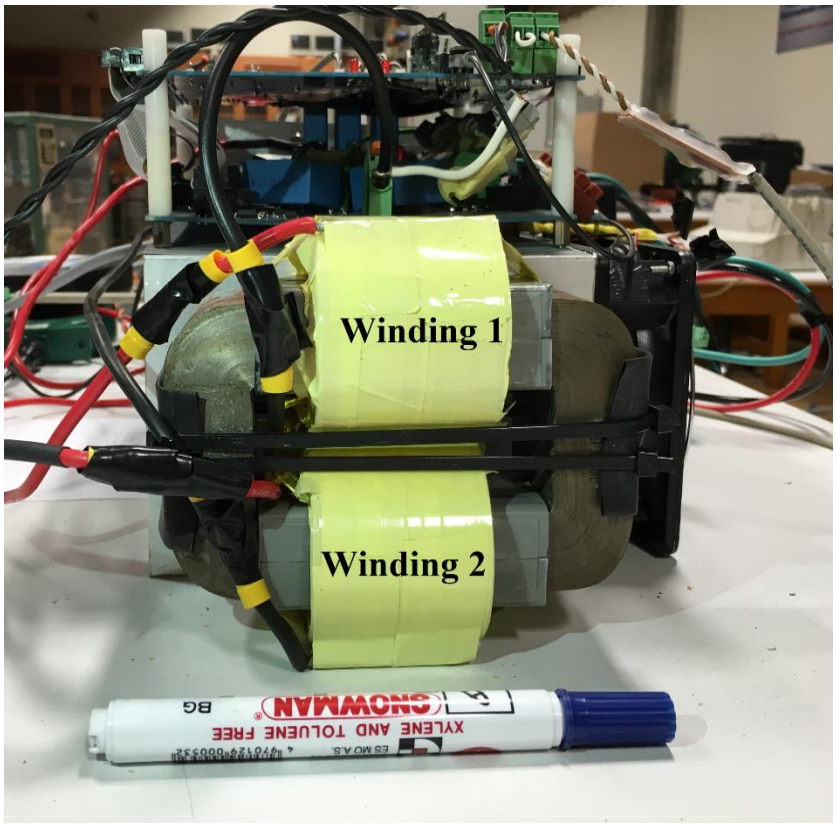


Figure 3.13 DC-link inductor

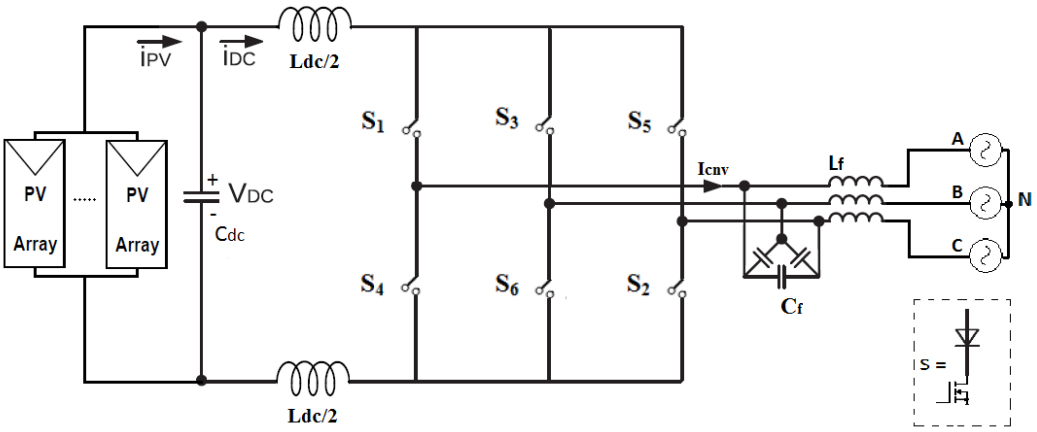


Figure 3.14 Connection diagram of split DC-link inductor

DC-link inductor core loss and copper loss are calculated for different DC-link current values using the software provided by the manufacturer and presented in Table 3.3. AC component of the DC-link current is independent of I_{dc} and mainly related to the modulation index. However, peak-to-peak ripple of DC-link current is not constant and fluctuates as a function of synchronous rotating angle (θ_s) as shown in Figure 3.15. Although the core loss is not linearly related to ΔB ($P_{\text{core}}, (\text{W/kg}) = 6.5 * \text{f}^{1.51}(0.5 * \Delta B)^{1.74}$, for AMCC500 [65]), for the sake of simplicity, core loss taken as the average of the maximum and the minimum core losses during one grid cycle.

Table 3.3 Inductor Losses vs DC-Link Current for *m*=0.8

I_{dc} (A)	Copper Loss (W)	Core Loss (W)
5	0.575	≈ 4
10	2.3	≈ 4
15	5.175	≈ 4
20	9.2	≈ 4
25	14.375	≈ 4
30	20.7	≈ 4
35	28.175	≈ 4
42	40.572	≈ 4

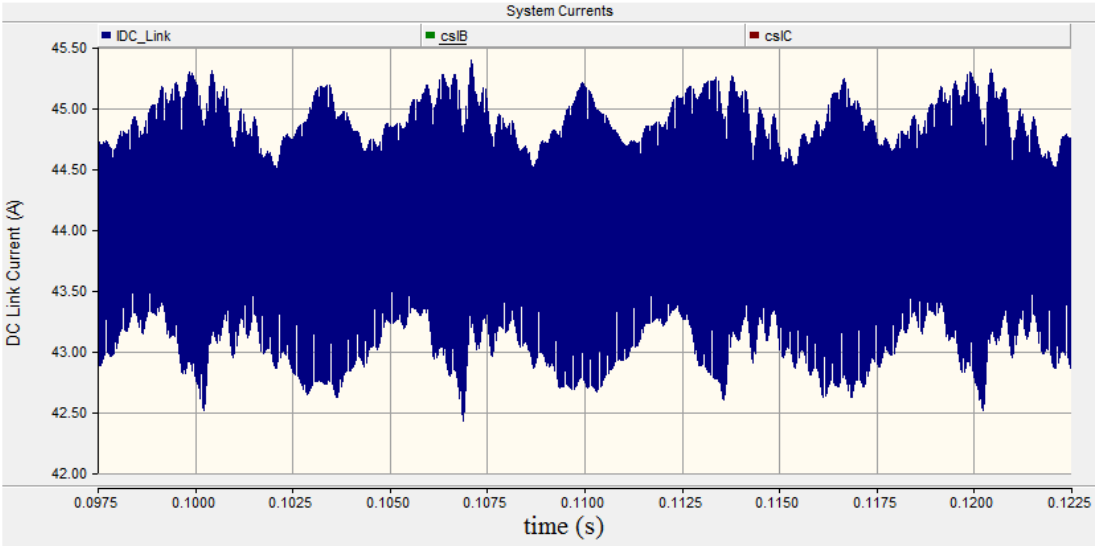


Figure 3.15 DC-link ripple current variation for m=0.8 during one grid period (PSCAD)

3.5.2 DC-Link Capacitor Selection

In order to minimize high frequency fluctuations around the MPP, AC component of the DC-link current should be filtered by using DC-link capacitance, C_{dc}. Limiting the voltage ripple ΔV_{pv} to 2% of MPP voltage will be fairly enough in order to achieve a MPPT efficiency of 99.9% and higher [7].

$$C_{dc} = \frac{\frac{T_s}{2} * \frac{1}{2} * \frac{\Delta I_{dc}{}^{p-p}}{2}}{\Delta V_{pv}} \tag{3.9}$$

Using (3.9), required capacitor size is found to be ≈2.5μF and a low ESR film capacitor (MKP1848530094K2, 3μF-900Vdc) from Vishay has been selected to be used as the DC-link filter capacitor.

3.6 AC Filter Design

According to [8], total harmonic content of the PV inverter output currents must be less than or equal to to 5% of the rated AC current level of the system. Harmonic spectrum of the unfiltered converter output currents (labeled as I_{cnv} in Figure 3.14) is given in Figure 3.16 for f_{cr}= 25 kHz, I_{dc}=42A and for the lowest modulation index, m=0.8 i.e. the worst case. As it can be seen from this figure, dominant harmonics of the CSI appears around the carrier frequency. According to [8], each individual harmonic above 33rd order must be limited to 0.3% of the rated output current of the converter at the fundamental frequency. In order to filter out these undesired harmonic components to comply with the limits in [8], an LC filter is used as explained in Chapter 2. In order to attenuate harmonics of output currents at the switching frequency (see the Figure 3.16), the output filter should have an attenuation of at least -36 dB at 25 kHz. In order to achieve this attenuation, the corner frequency (f_c) of the output filter needs to be tuned to an appropriate frequency, where f_c is expressed as

$$f_c = \frac{1}{2\pi\sqrt{L_f C_f}} \tag{3.10}$$

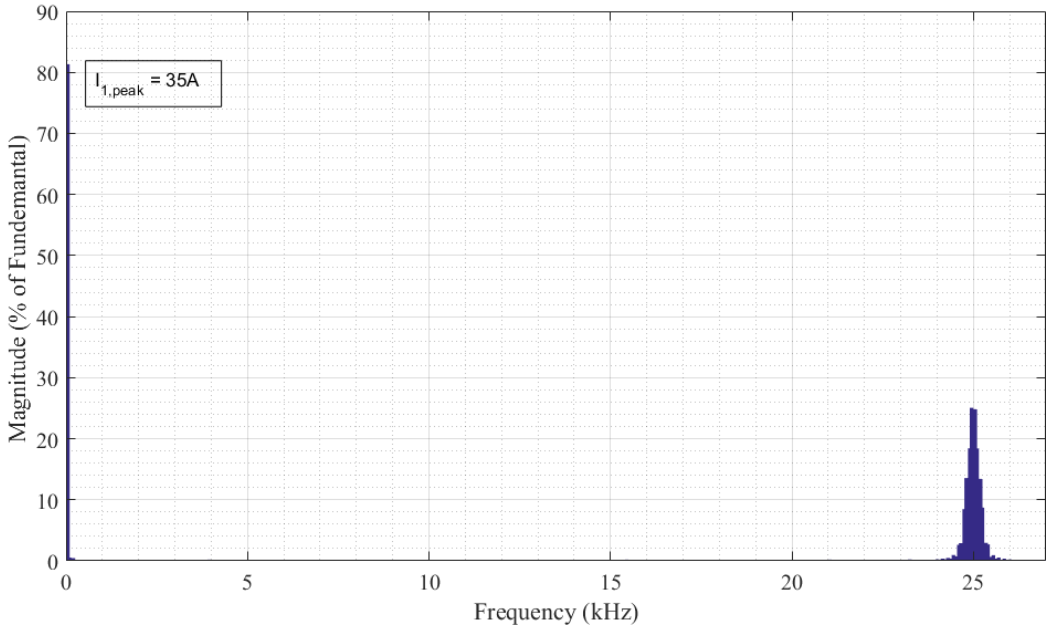


Figure 3.16 Harmonic spectrum of the converter currents (I_{cnv}) for f_{cr} = 25 kHz, m=0.8 and I_{dc}=42A

Since the reduction of the corner frequency will result in larger filter components, selection of a corner frequency around 2.5 kHz will be enough in order to provide an attenuation of -40dB at the carrier frequency with optimum passive component size. By this way, nearly sinusoidal line currents which comply with the harmonic standards in [8] can be obtained.

Capacitors at the AC side are inherent to the Current Source Converters in order to provide a low inductance return path to the converter current pulses. In order to keep impedance of the current path as low as possible developed CSI employs a Δ-connected filter capacitor bank as shown in Figure 3.14. As a general practice, in order to limit the reactive power generated by the output filter capacitor, per phase Y-equivalent filter capacitance is selected to be less than 5 % [1] of the base capacitance C_B which is expressed as:

$$Z_B = \frac{V_N^2}{P_N}, \quad C_B = \frac{1}{\omega_N Z_B} \tag{3.11}$$

Taking P_N =20 kVA, $\omega_N = 2\pi 50$ and nominal line to line converter voltage V_N=400V, per unit capacitance C_B is approximately found as 400 μF, and then the preferred maximum Δ-equivalent filter capacitance is calculated to be ≈6 μF.

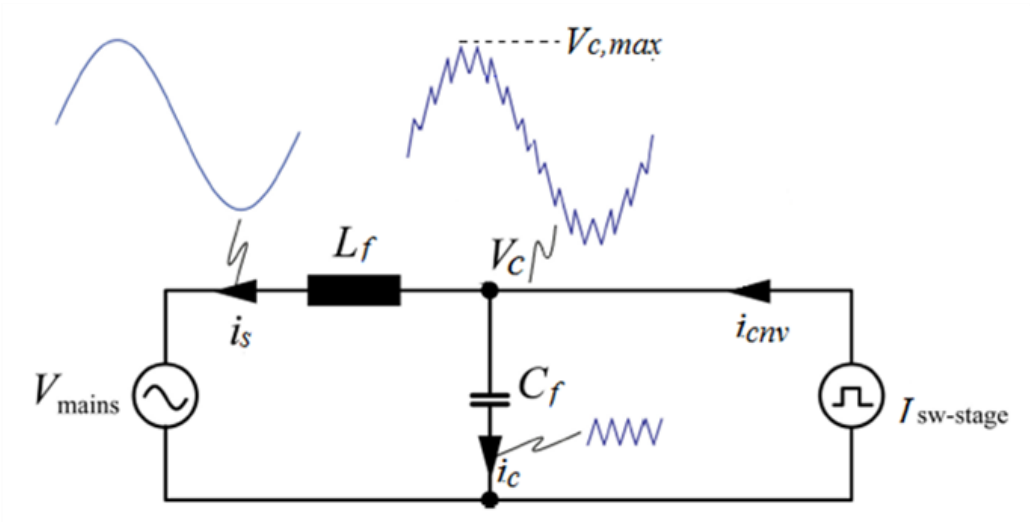


Figure 3.17 Idealized current waveforms for filter elements

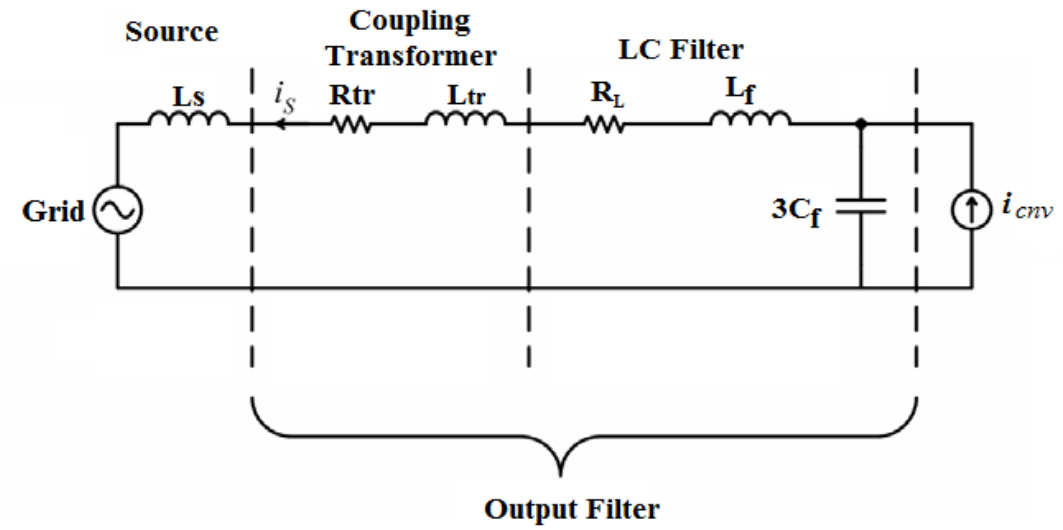


Figure 3.18 Single line diagram of the CSI based grid-connected PV inverter with coupling transformer

On the other hand, minimum size of C_f is limited by the voltage ripple (see Figure 3.17) of the filter capacitors. At the maximum value of the line-to-line voltages, voltage rise and Δ-connected C_f can be related as:

$$\Delta V_{C_f} \propto \frac{(I_{dc} - \hat{I}_s * \sin\left(\frac{\pi}{3}\right)).\left(m * \sin\left(\frac{\pi}{3}\right)\right) * T_s}{2C_f} \tag{3.12}$$

Therefore excessive reduction of C_f must be avoided in order to keep the semiconductor voltages at safe levels. Considering these two constraints, filter capacitance has been decided to be 2uF/phase for delta connected capacitors and two X1 class MKP film capacitors with 1.0uF/530Vac ratings (B32914A5105M from EPCOS) are connected in parallel in order to obtain desired C_f value.

In a large scale PV installation, connection of the PV inverters to the MV level will be possible only through a coupling transformer. Standard power transformers with a power rating of a few MW have nearly 5% voltage drop value as Uk [13], which constitutes a significant amount of inductance when referred to LV side. Therefore, including the cable and busbar inductances, a filter inductance is naturally provided by the leakage inductance of the transformer, L_{tr}. Resulting Y-equivalent single line

diagram of the CSI is illustrated in Figure 3.18 including the external filter inductor L_f which will be used for the fine tuning of the output filter corner frequency.

In the construction of the laboratory prototype, three of single-phase 0.4kV/0.4kV, 10 kVA isolation transformers are employed and connected in three-phase Y-Y configuration. Measurements have shown that leakage inductance (L_{tr}) of the isolation transformer is equal to 1.5mH and equivalent resistance (R_{tr}) is equal to 0.2ohm. Since L_{tr} of the isolation transformer is high enough, additional filter inductance is not employed in the laboratory prototype.

Frequency response of the undamped output filter is then plotted using PLECS and demonstrated in Figure 3.19. It has been seen that the corner frequency of the output filter is realized as 1.68 kHz which is significantly lower than the desired frequency due to large leakage inductance of the employed isolation transformer. Figure 3.19 shows that desired attenuation at the carrier frequency also obtained.

However, due to the weak damping of the filter, the frequency response shows a large amplification factor around corner frequency. Even though the magnitudes of the converter current harmonics are less than 0.3% at this frequency, they can be amplified by a factor more than 100 which may result significant waveform distortion and violation of the harmonic limits in [8].

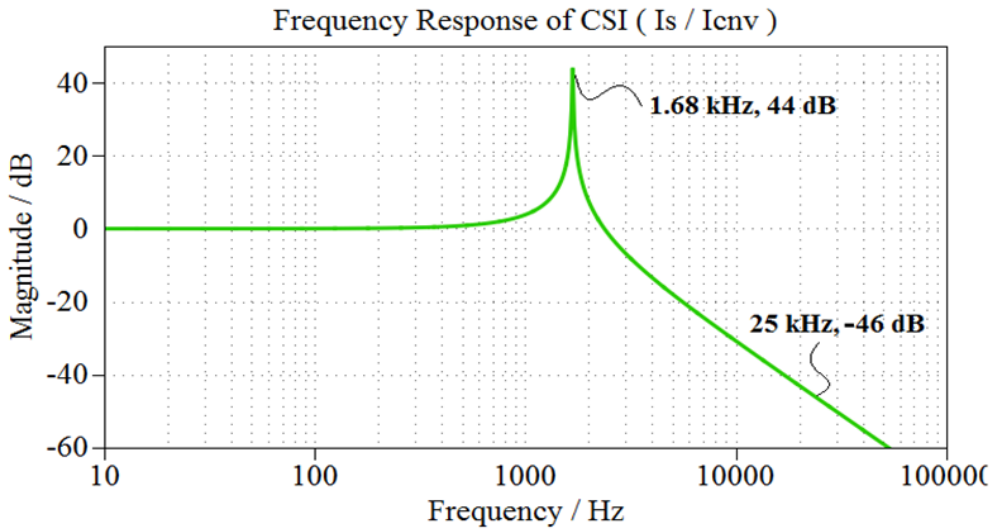


Figure 3.19 Frequency response of undamped output filter

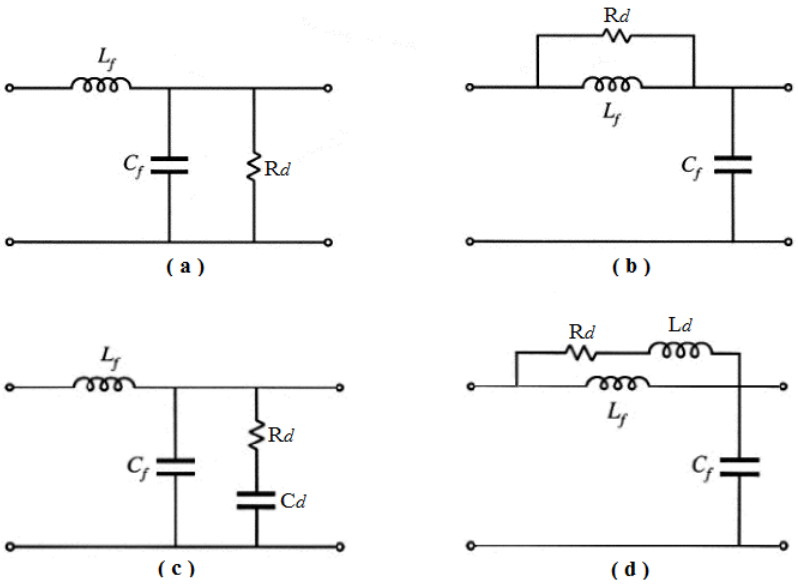


Figure 3.20 Four practical approaches to damping the single-section LC filter: (a) Rd across Cf, (b) Rd across Lf, (c) Cd - Rd across Cf , (d) Ld - Rd across Lf [65]

This can be avoided with the use of passive damping [13,68,69] or active damping [67,68]. Since the active damping requires a complicated control algorithm and it cannot provide continuous damping in the entire frequency range [13], a low loss passive damping circuit will be adopted in this study.

Four practical approaches for passive damping of LC filters are given in Figure 3.20 [65,69]. Although the connection of R_d across C_f as in Figure 3.20(a) results the best damping, it is impractical due to high power losses. Secondly, connection of R_d across L_f results in a degraded filtering performance at the carrier frequency since the filter behaves as a first order R-C filter at high frequencies. Since the method given in Figure 3.20 (d) also shows a degraded attenuation performance at high- frequencies, method given in Figure 3.20(c) (C_d - R_d across C_f) is adopted for the damping of the output filter of the developed CSI prototype.

Using the methods explained in [69], the damping capacitor C_d is decided to be 1 µF and it's selected from the EPCOS X2 MKP film capacitors series, which has a rated voltage of 305 Vac.

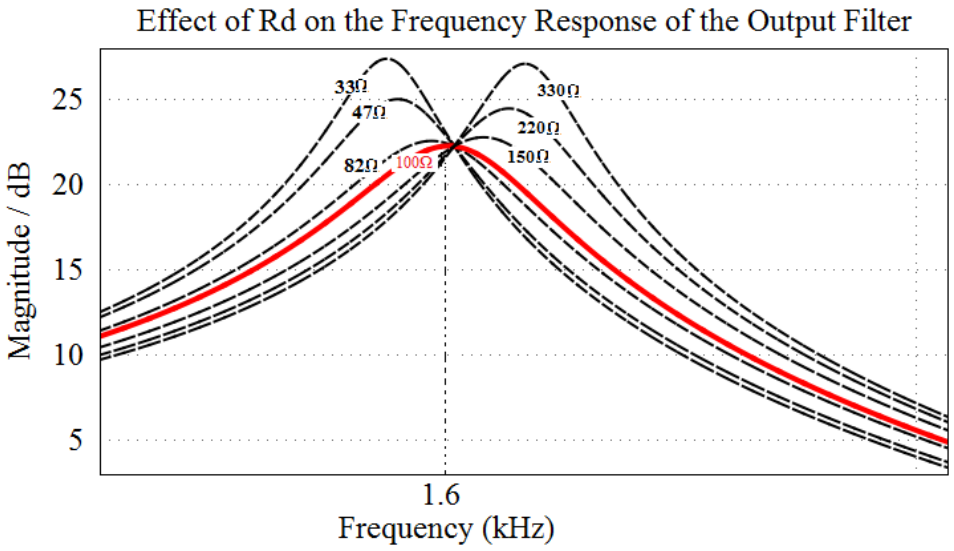


Figure 3.21 Frequency response of output filter for different R_d values

As the resulting transfer function of output filter including the C_d - R_d damping branch is not in the form of a basic second order filter transfer function, it is not possible to find simple expressions for characterization of its transient response. Instead of that, corresponding circuit is simulated in PLECS using various R_d values and corresponding frequency responses are plotted in Figure 3.21 from which optimum R_d found to be 100Ω.

The resultant frequency response of the output filter including the damping circuitry is given in Figure 3.22 and it can be seen that the amplification factor around resonant frequency of the filter has been decreased to ≈10. Since the converter does not produce a visible harmonic content around the resonant frequency, this reduction will be enough in order to comply with the harmonic limits.

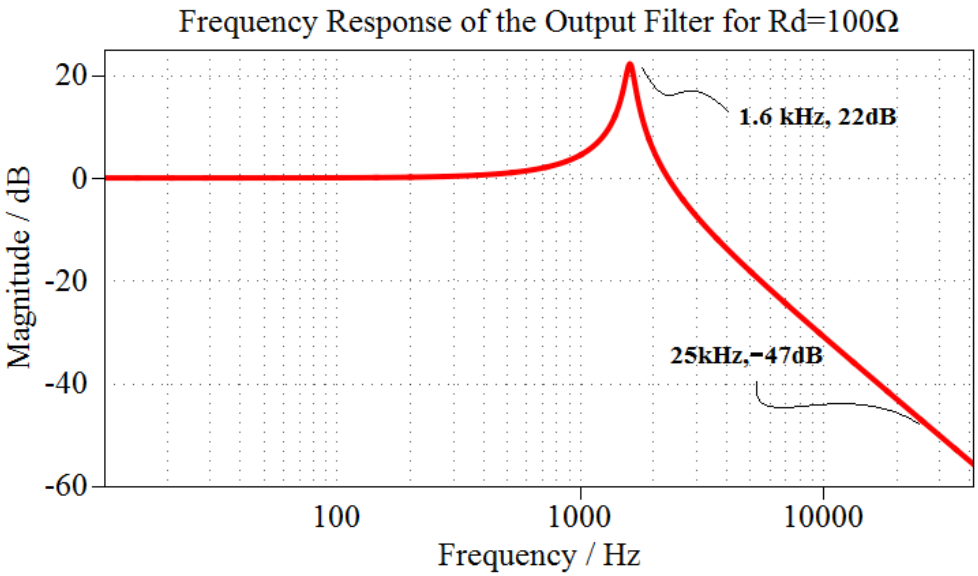
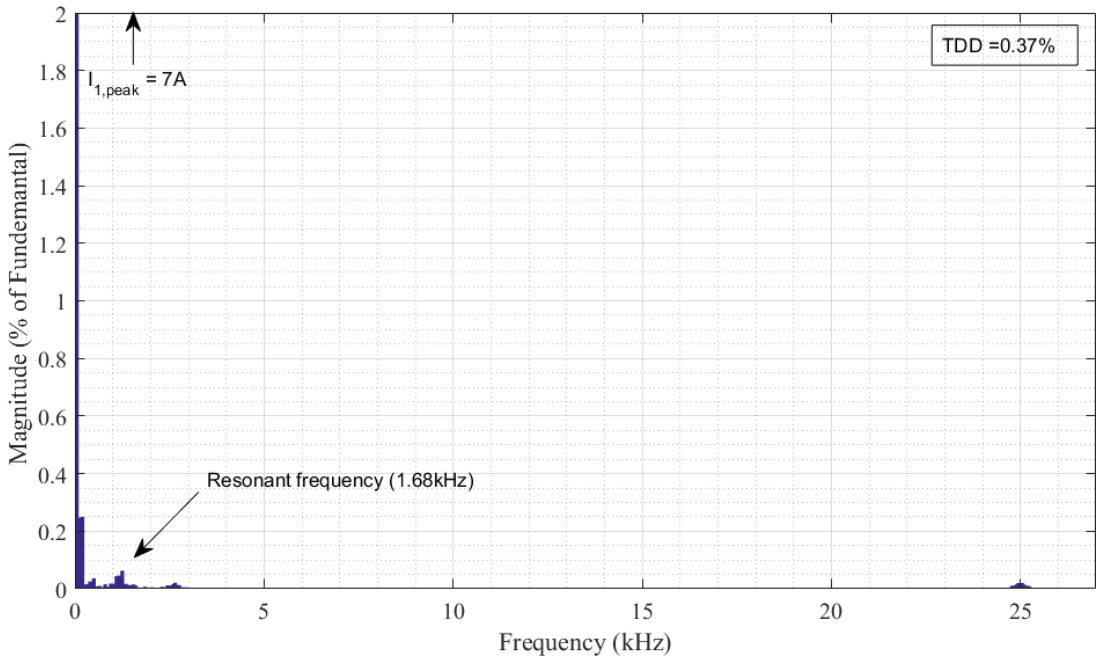
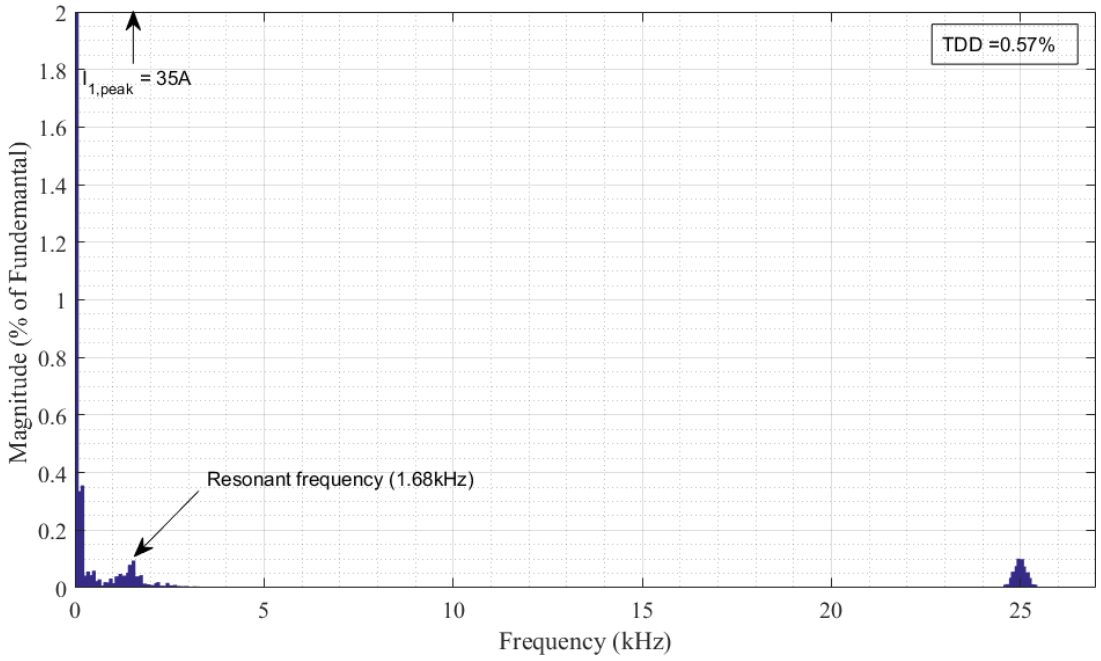


Figure 3.22 Frequency response of output filter for R_d = 100 Ω

Performance of the PV-CSI system including designed output filter and damping circuitry has been simulated in PSCAD and output current waveforms of the inverter before and after filtering is obtained as in Figure 3.24 and harmonic spectrums of the filtered output currents at %20 and %100 of the rated output power are presented in Figure 3.23(a) and Figure 3.23(b) respectively. As it can be seen from the corresponding figures, harmonic content of the output currents is below the limits given in [8] for both of the cases. Finally, from the computer simulations it has seen that the total power dissipation of the damping circuit is only 5W for %100 and 2W for %20 of the rated power of designed inverter.



(a)



(b)

Figure 3.23 Harmonic spectrum of output line currents at (a) 20%, (b) 100% of the rated output power for *m*=0.8

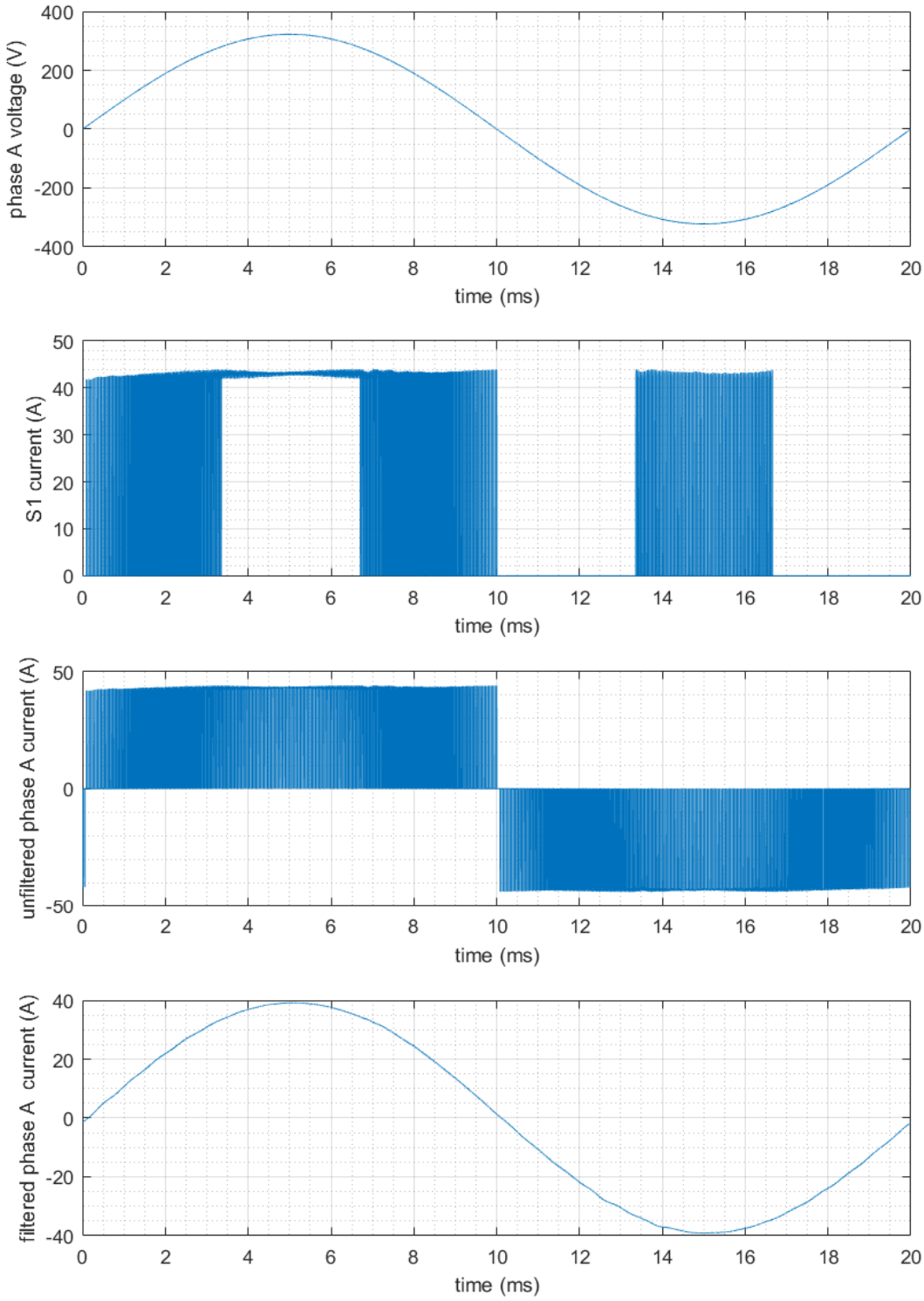


Figure 3.24 Current waveforms of phase-A for one power cycle at unity power factor, I_{dc}=42A and *m*=0.9

3.7 Estimated Inverter Efficiency

As explained in section 3.3, power conversion efficiency of the PV-CSI system strictly depends on the modulation index of the inverter which is primarily constituted by the MPP voltage of the PV array. MPP voltage of the PV array changes mainly as a function of the solar irradiation and PV array operating temperature. Temperature of the PV array is affected by the ambient temperature, solar irradiation level, wind speed etc. Therefore, it is not possible to draw a unique efficiency profile for a current source inverter operating in a PV application. Instead, considering semiconductor losses, DC-link inductor losses, damping circuitry losses and auxiliary power consumption, two efficiency profiles has been sketched for the SiC based CSI in Figure 3.25 for m=1.0 and m=0.8 corresponding to maximum and minimum MPP voltages of the designed PV inverter. Each profile assumes a constant PV array voltage independent of the DC current level.

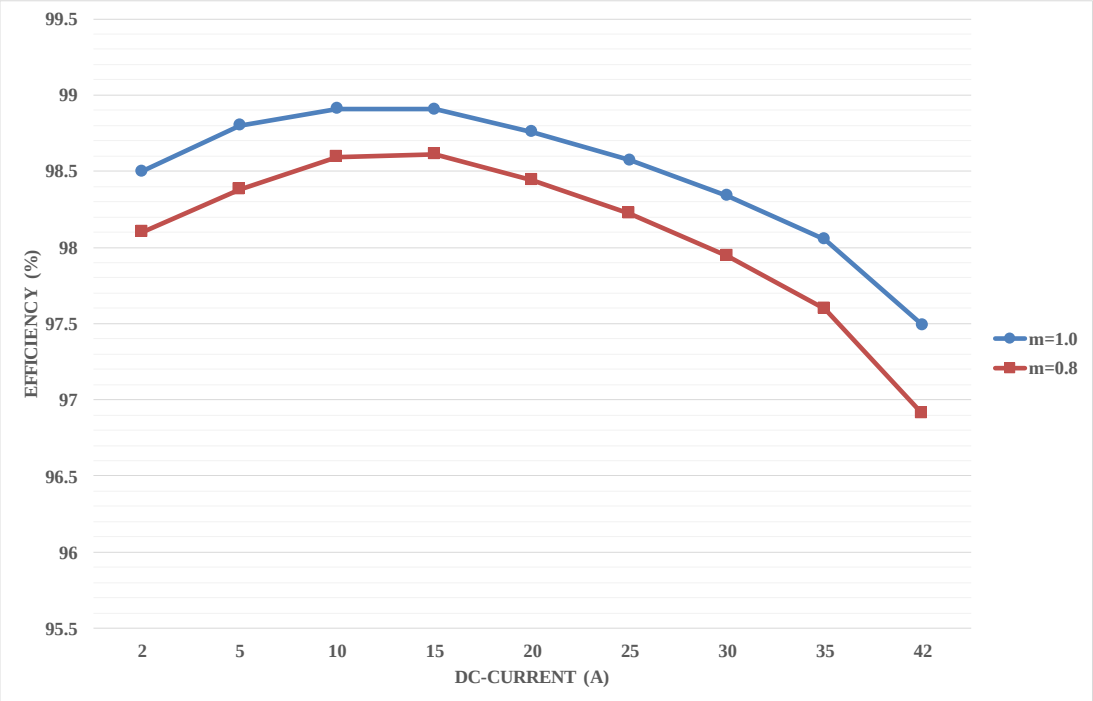


Figure 3.25 Calculated conversion efficiency of the PV-CSI vs DC-link current for m=0.8 and m=1.0

The European Efficiency (η_{eu}) is one of the most widely used methods to evaluate the efficiency of grid-connected PV inverters under partial load conditions. According to the definition of the European efficiency [7], the particular efficiencies, at 5%, 10%, 20%, 30%, 50% and 100% of nominal power, are weighted and summed up according to the probability of seeing that sun irradiance level in the central Europe as follows:

$$\eta_{eu} = 0.03\eta_{5\%} + 0.06.\eta_{10\%} + 0.13\eta_{20\%} + 0.10\eta_{30\%} + 0.48\eta_{50\%} + 0.20\eta_{100\%} \quad (3.13)$$

Using (3.13), European efficiency of the current source inverter is calculated as 98.5% and 98.1% for constant modulation indices of m=1.0 and m=0.8 respectively

3.8 Design of the Overvoltage Protection Circuit

One of the most important and challenging steps in the design of the Current Source Converters is the prevention of the DC-link current interruption during the operation. If a diode, switch, driver or modulation fault occurs and current through DC-link inductor tends to decrease, an example case is illustrated in Figure 3.26, large over-voltage will occur across DC-link inductor and power semiconductors of CSI. This causes avalanche breakdown of the power semiconductors [70,71]. Although the selected MOSFET is able to absorb a certain amount of energy [74] for single pulse avalanche, repetitive pulses cause degradation of device parameters and possible failure of semiconductors [76]. Because of that, in case of a DC-link current interruption, a separate over-voltage protection circuit should take over the inductor current and all switches must be turned-off autonomously in order to protect semiconductor switches.

A few precautions have been reported in the literature in order to overcome this problem [70, 71]. Due to fast switching characteristics of SiC MOSFETs, drain-source voltage of the MOSFET will reach breakdown voltage rating in a very short time. Therefore, employed overvoltage protection scheme in the CSI built with SiC devices must have a very fast response. Moreover, it should not affect the switching performance of SiC MOSFETs in normal operation.

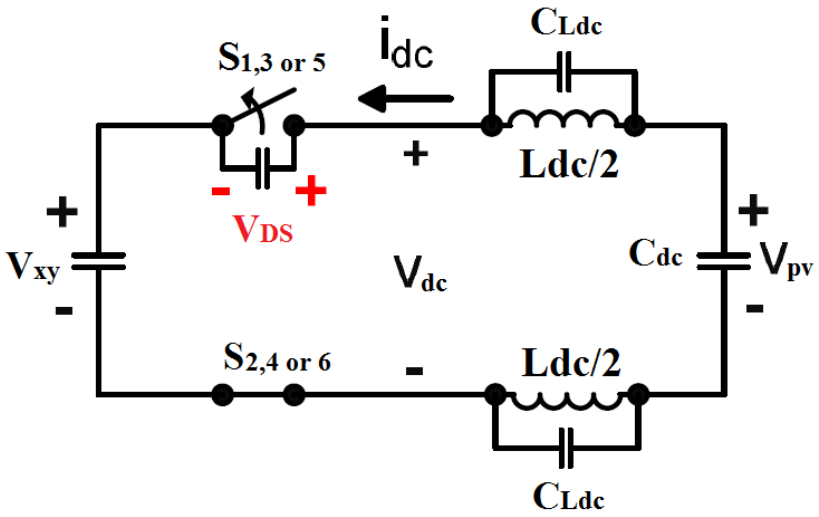


Figure 3.26 Equivalent circuit for DC-link current interruption in a CSI

Employment of high-power TVS diodes between positive and negative buses [71] found as the best alternative among the reported methods matching the both requirements with a few ten ns response time and relatively low capacitance. Various TVS diodes with different power and voltage ratings are available on the market [72].

The reverse stand-off voltage of the TVS diode should be higher than maximum DC-link voltage during normal operation, so that it will not affect operation of the converter. Considering the 10% raise of mains voltage and high-frequency ripple on the output filter capacitors, maximum value of instantaneous DC-link voltage is expected to be 640V during normal operation. Its maximum clamping voltage should be smaller than the rated voltage of the semiconductors (1200V) to be protected. Clamping voltage of commercial TVS diodes is usually lower than 400V, considering the maximum peak pulse current rating of TVS diodes three of 15KPA200A and two of 1.5KE15A are connected in series as illustrated in Figure 3.27. Constructed overvoltage protection circuitry clamps V_{dc} around 1000V in case of a fault and draws 2 µA under normal operating voltage and less than 5 mA at V_{pv}=V_{oc}. Additionally, in case of a fault situation, designed protection circuit generates an isolated output signal to the controller.

Another feature of the employed circuitry is the detection of mains connection loss. As illustrated in Figure 3.28, when mains connection is lost, I_{dc} circulates through output filter capacitor C_f and the corresponding capacitor voltage may rise above the rated semiconductor voltage within one switching cycle. Since $V_{dc}=V_{13}$ (for S1, S2 are in ON-state and ignoring semiconductor voltage drops) overvoltage on filter capacitor will be detected by the overvoltage protection circuitry. Upon the receipt of fault signal, all switches will be turned-off and DC-link current will be vanished on clamping circuitry.

Additionally, metal oxide varistors (MOVs) are connected across the filter capacitors in order to prevent overvoltage on filter capacitors in case of a surge voltage from the power network due to lightning or switching of AC circuit breakers. When there is an over-voltage across these MOVs, which are known as fast acting transient overvoltage suppressors, they behave like a short circuit absorbing the energy which otherwise would over-charge the filter capacitors [13]. Selected MOV (S14K440) is rated for 440 Vrms for normal operation and its clamping voltage is around $1100V$ at 50A [77].

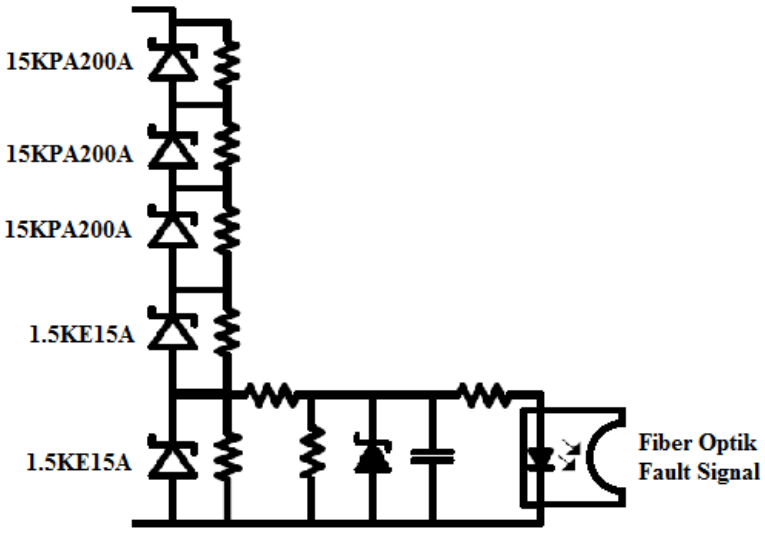


Figure 3.27 Simplified schematic of designed overvoltage protection circuit

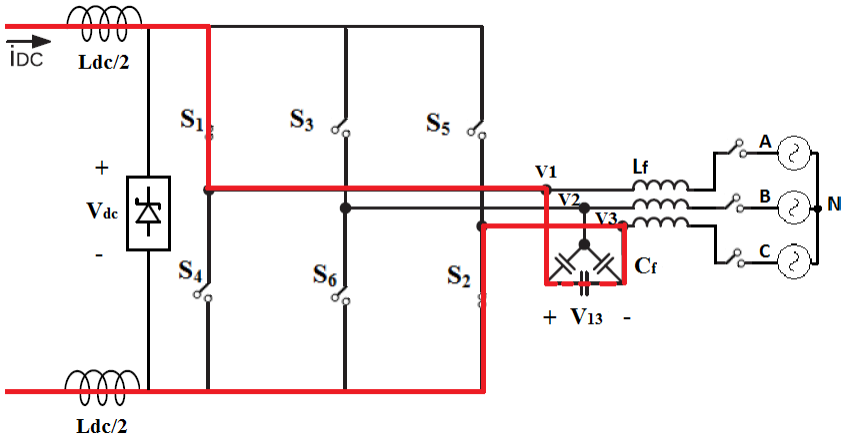


Figure 3.28 Equivalent circuit for mains disconnection

3.9 Design of the MPPT Controller

Operation of a PV inverter based on the maximum power transfer for a given set of operating conditions. Irradiance level and the modules' temperature (which is in turn function of the irradiance level, of the ambient temperature, of the efficiency of the heat exchange mechanism and of the operating point of the modules) are the two main parameters that affect the characteristics of PV array significantly and necessitate a MPP tracking algorithm as explained in Chapter 2. For this purpose, Perturb and Observe (P&O) MPPT technique has been adopted in this study due to its ease of implementation. Although the PV module temperature exhibits smooth variations, irradiance level may change quickly in cloudy days causing a rapid variation of the MPP. Employed P&O MPPT technique has two main parameters requiring optimization in order to track MPP of the PV array efficiently in the case of the rapid variation of irradiation level.

Amplitude of the reference current perturbation (ΔI_{pv}) is one of the two parameters requiring optimization. A high ΔI_{pv} provides a fast tracking in case of rapidly changing atmospheric conditions, however, since the P&O MPPT method continuously seek for a better operating poin, it increases the steady-state losses caused by the oscillation around the MPP The sampling interval of the P&O MPPT algorithm is the other parameter that needs to be optimized to achieve a fast and stable MPP tracking. If the MPPT algorithm samples the PV array voltage and current too quickly, controller

becomes susceptive to possible mistakes caused by the transient behavior of the whole system including PV array [86], thus missing, even if temporarily, the MPP of the PV array. On the other hand, a low sampling rate results in a less efficient power transfer in case of rapidly changing atmospheric conditions.

The key idea behind the optimization of the P&O MPPT parameters relies on the dynamic behavior of the whole system including the converter and PV array. A good analytical approach to the optimization of P&O MPPT parameters can be found in [86]. For the sake of simplicity, in this study MPPT controller parameters are determined using computer simulations built on the PV array model. Firstly, parameters of PI controller tuned using Ziegler-Nichols rules. Then, it has seen that a sampling interval of 10ms guarantees the settlement of the DC-link current before the next perturbation is applied. In order to minimize power deficiency caused by the swing around MPP, amplitude of the reference current perturbation is taken as 1% of the PV array current level of the corresponding operating current level in steady state. However, minimum perturbation amount is limited by the sampling resolution of the controller system (20 mA). In case of a rapid insolation variation, magnitude of the reference current perturbation increases to 2% in order to accelerate the MPPT process, as the power reaches maximum level, magnitude of the perturbation decreases to 1% again.

Performance of the controller under the step variation of the insolation level from 0 to 1000 W/m^2, 1000 W/m^2 to 500 W/m^2 and 500 W/m^2 to 1000 W/m^2 for the PV array temperature of 60 ^{o}C is then evaluated by computer simulations and the response of the system to the step variations of the insolation is given in Figure 3.29. As explained previously, maximum possible DC-link voltage applied to PV array terminals is limited to 489 V under nominal grid voltage and it decreases proportionally to the modulation index. At the beginning of the start-up process of the CSI, modulation index is set to 1.0 in order to set the PV array voltage to the maximum possible DC-link voltage and hence start the inverter with the minimum DC-link current. Since the maximum DC-link voltage is much smaller than the open circuit voltage of the PV array for T_{pv} = 60 ^{o}C, DC-link current rises up to 30A within a few switching cycle.

Then, MPPT controller rises DC-link current to 41A by decreasing DC-link voltage to 450 V within ≈140 ms.

After the CSI reaches steady state, insolation is suddenly decreased to 500 W/m^2 from 1000 W/m^2. However, the MPPT controller cannot update the reference current instantaneously and PI controller forces the inverter to increase DC-link current and decreases modulation index down to the lower *m* limit. In this case, MPP is caught very late or even can be missed since a constant power drawn from the PV array corresponding to the lower *m* limit. In order to accelerate MPPT performance, P&O method is modified such that the MPPT controller assigns the actual DC-link current as the reference DC-link current if the PI controller output reaches minimum or maximum limits. The same problem also exists for the case of rapid variation of solar radiation in positive direction. As it can be seen from Figure 3.29, new MPP point is reached within ≈150 ms in both cases.

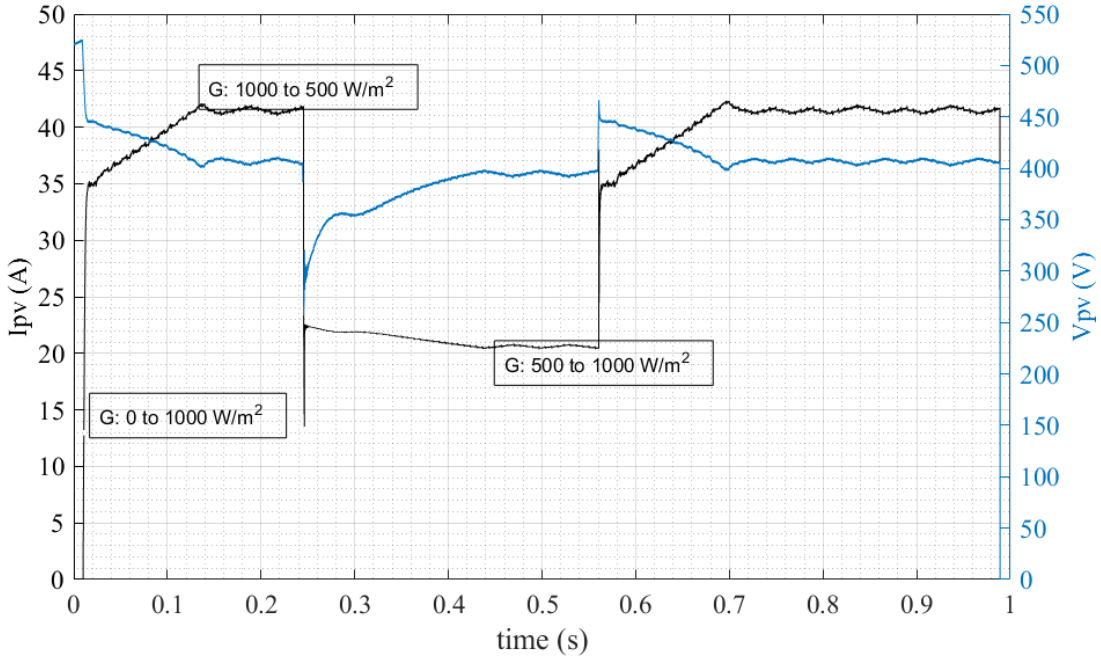


Figure 3.29 Performance of the MPPT controller in presence of rapid irradiance variation at T_{pv} = 60 ^{o}C

3.10 Design of the Control System Hardware and Power Stage

The prototype hardware is constituted from two main sub-sections: controller and power stage. The controller hardware includes a DSP board (1) and external measurement boards (2), (3) while the power stage (4) houses power devices, gate drivers, AC filter capacitors, passive damping circuitry and DC-link overvoltage protection circuitry. Constructed prototype of three-phase current source inverter designed for photovoltaic applications is given Figure 3.31. and description of enumerated components in this figure is presented in Table 3.4. Finally a simplified functional structure of the developed laboratory setup is given in Figure 3.30

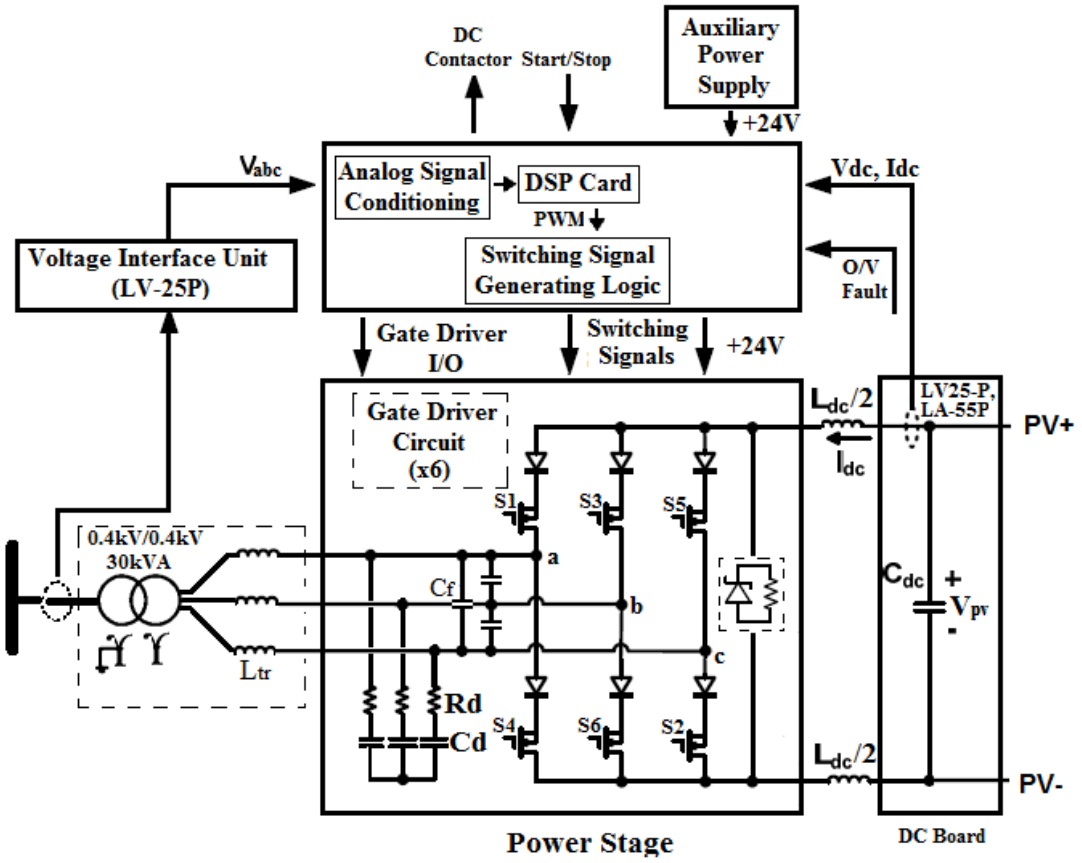


Figure 3.30 Simplified structure of the PV-CSI prototype

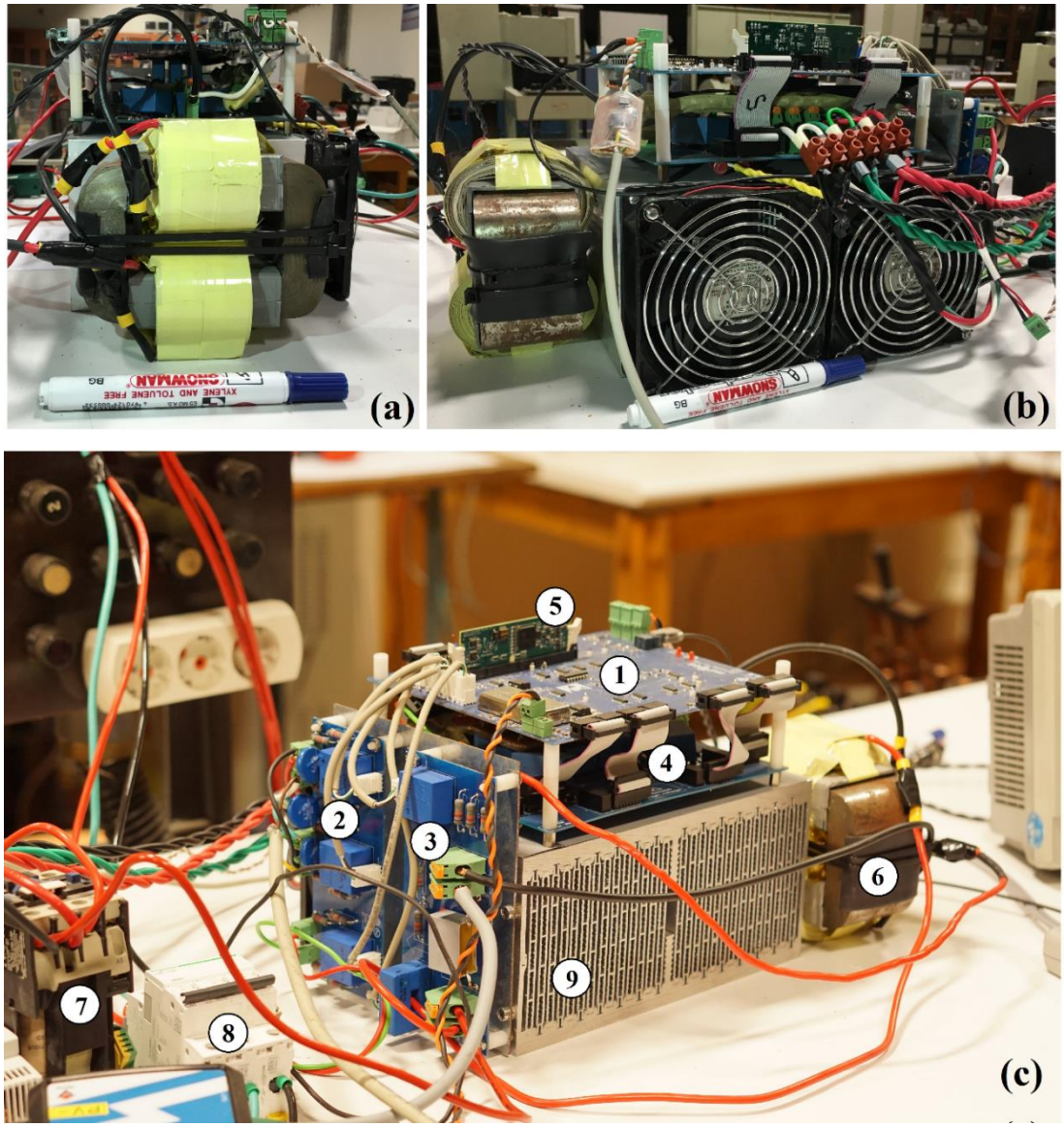


Figure 3.31 20 kVA, three-phase PV-CSI prototype a) side view, b) back view, c) front view

Table 3.4 Enumeration of main components in the developed prototype

1	Controller Board	6	DC link Inductor
2	AC Voltage Interface Unit	7	DC Contactor
3	DC Board	8	AC Circuit Breaker
4	Power Stage	9	Heatsink
5	TMDSCNCD28335 Control Card		

3.10.1 Design of the Controller Hardware

Principles related to the control of the PV-CSI system are described and proposed control method is given in Chapter 2. The control algorithm of the PV-CSI will be realized on TMDSCNCD28335 [80] DSP control card which is numbered with 5 in Figure 3.31. As explained in section 3.9, control of the PV-CSI is based on the adjustment of the reference current modulation index *m,* in order to match mean value of DC-link current (I_{dc}) with the DC-link reference (I_{dc}*) generated by the MPPT controller which requires measurement of DC-link current (I_{dc}) and PV array voltage V_{pv}. The LEM LV25-P voltage transducer is used for the measurement of PV array voltage and LA55-P current transducer is used for the measurement of I_{dc}. Both circuitry is placed on the same measurement board (1) which is designated as DC board as shown in Figure 3.30. Corresponding board also accommodates input filter capacitor C_{dc}.

Controller also requires the measurement of the AC side voltages for the calculation of synchronous rotating angle (θs) which will be used for the generation AC line current references. A separate board (shown as voltage interface unit in Figure 3.30 and numbered as 2 in Figure 3.31) realizes the measurement of the AC line voltages using LEM LV25-P voltage transducer. Transducer signals is then scaled, filtered, biased and conditioned on DSP board in order to map them into measurement range of the DSP control card.

DSP board also includes logic circuitry that performs bi-logic to tri-logic transformation of PWM signals as explained in [15] and generates overlap times by delaying falling edges of the switching signals for 100 ns. Required voltage levels for transducers, DSP card, logic circuitry and the gate drivers provided by auxiliary power supply employed on this board, where total power consumption of corresponding equipment calculated to be ≈7W.

3.10.2 Design of CSI Power Stage

Parasitic inductance and capacitance have been always existed as a natural consequence of the device physics involved in the power electronic applications. All physical circuits have stray inductance caused by device pins, bond wires, PCB traces, etc. Furthermore, all semiconductor devices come together with an output capacitance; typically, proportional to the current rating of the device. In general, standard application guidelines developed for Si devices also apply to SiC devices.

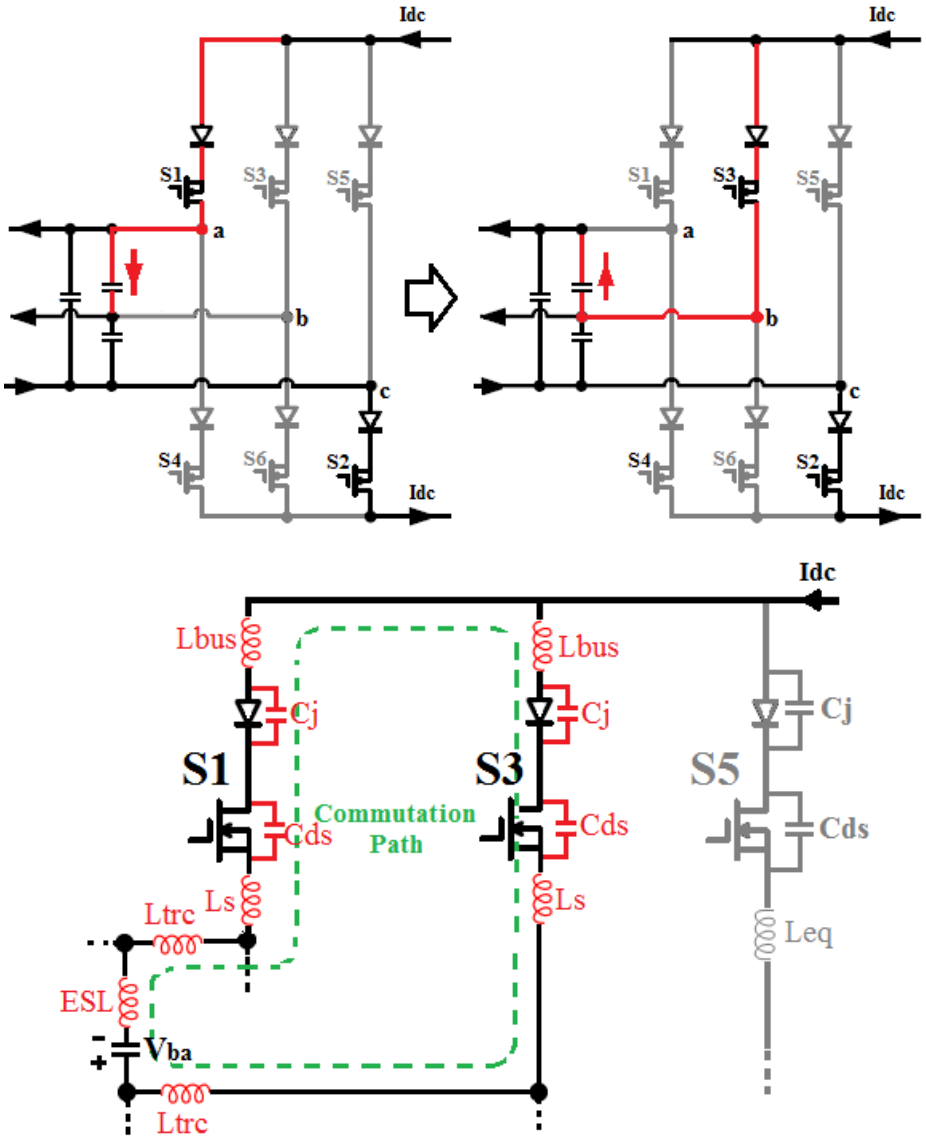


Figure 3.32 (a) Current path before (left) and after (right) S1 to S3 commutation,(b) commutation path for S1-S3 commutation events including parasitic components

However, the unique combination of high voltage, high current and increased switching speed of SiC MOSFETs requires careful construction of the circuit layout to reduce the effects of the parasitics [79,80]. Because faster switching speeds of SiC devices at high voltages and currents results in higher dv/dt and di/dt, voltage drops, even a few nanohenries of stray inductance can be problematic. The voltage drop across this inductance is expressed as V=L*di/dt. If the di/ dt is high enough, the voltage drop across the stray inductances can become significant.

Commutation event between S1 and S3 is illustrated in Figure 3.32 as an example for current source inverter switching process. Figure 3.32(a) shows current flow before (S1 ON, S3 OFF) and after the commutation event (S1 OFF, S3 ON). Circuit components (including parasitic components) that are effective during this commutation process are illustrated on the equivalent circuit in Figure 3.32 (b). Commutation loop inductance is distributed throughout the commutation path and major contribution made by MOSFETs' and diodes' stray inductances caused by the device pins and internal wire bonding, equivalent series inductance (ESL) of output filter capacitors and stray inductance of board traces L_{trc} and L_{bus}. Fast commutation of current from S1 to S3 (high di/dt) may result in significant voltage drops (V=Ldi/dt) across a few nanohenries of stray inductance and outgoing MOSFET may be exposed to voltage overshoot beyond the maximum device voltage rating. Moreover, output capacitance of the semiconductors and stray inductances form a resonant circuit and parasitic resonance may cause a high degree of ringing due to enhanced conductance of SiC devices.

Source inductance (L_s) also has a considerable impact on the device switching energy both at turn-on and at turn-off which is mainly constituted by the internal wire bonding of the source terminal and device leads. This parasitic element, shared between the power and driver loops produces a negative feedback (as expressed in (3.14)) in the gate control signal resulting in an outlasting commutation time.

$$V_{\text{GS}} = V_{\text{drive}} \pm L_{\text{s}} \frac{dI_{\text{ds}}}{dt} \tag{3.14}$$

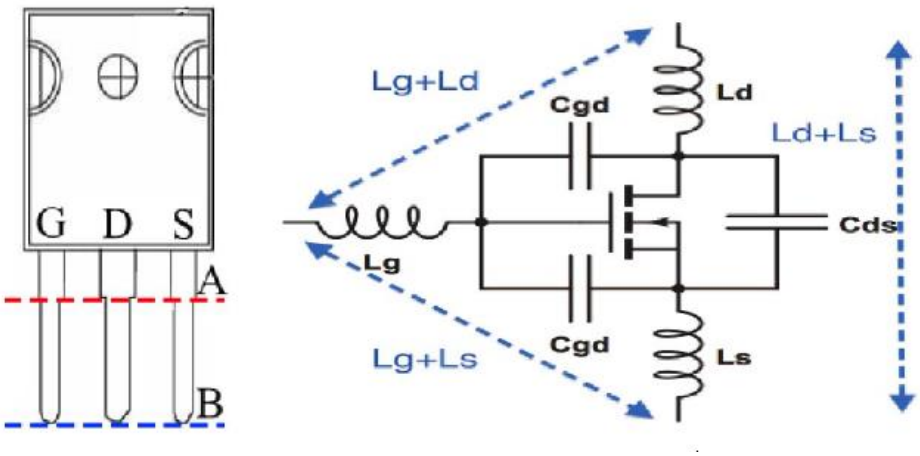


Figure 3.33 Parasitic components on a MOSFET in a TO-247 package

A customary 'rule of thumb' for insertion inductance puts it at about 10nH/cm[78] and L_s increases as the soldering points closes to the point B in Figure 3.33. Therefore, device lead length must be kept as short as possible.

Introducing additional damping resistance into power circuit in order to damp the overshoots and parasitic oscillation is impractical since it will cause power losses. Control of the overshoots (without employing a complicated snubber circuit) can be effectively accomplished by controlling the commutation times also. However, slowing down the switching speed increases switching losses and defeats the purpose of using SiC MOSFETs. Therefore, optimization of the power stage layout must be one of the primary objectives of the design and the stray inductances throughout commutation path should be minimized as possible in order to get maximum performance out of the designed converter. Recognizing that there will always be some amount of ringing present, an engineering tradeoff is required to ensure that voltage overshoot does not damage the device while preserving the switching speed advantage [78]. Then appropriate external gate resistance can be selected such that the switching times are greater than the period of the natural frequency of the resonance.

Commutation event between S1-S5 (which take place on the longest commutation path along with the commutation between S2-S4 on the constructed power stage) is simulated in LTSPICE for different stray inductance values using spice models of

C4D40120A and C2M0040120D. In the preliminary design phase, filter capacitors are planned to be connected in Y-configuration and power stage is planned to be constructed on a two sided PCB board using coplanar PCB traces as shown in Figure 3.34 [79]. If Y-connected filter capacitor bank is employed in the power stage, commutation path will include two series connected capacitors (each has an ESL of ≈ 20 nH) and contribution of filter capacitors to the stray inductance of the commutation loop will be doubled. Inductance of the PCB traces is approximated roughly to be around 40 nH using the techniques explained in [79].

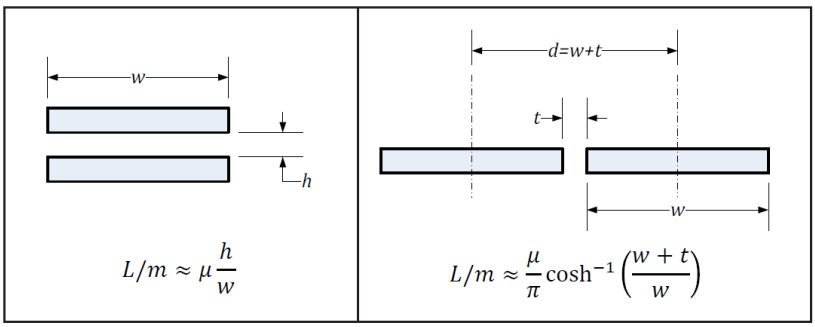


Figure 3.34 Stray inductance approximation for stacked and coplanar PCB traces [79]

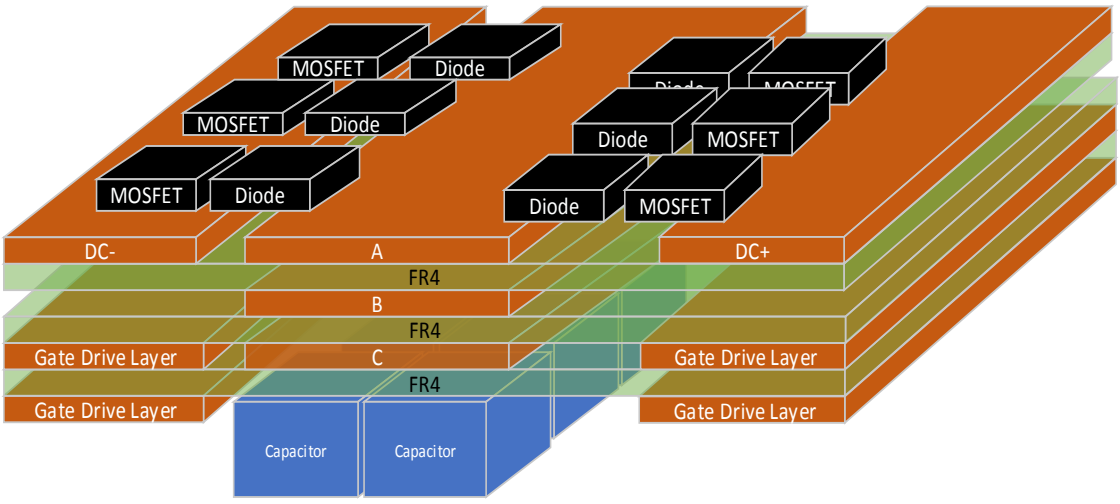


Figure 3.35 Power stage layout

Taking source inductance, L_s, as 10nH, V_{ba}=560V, I_{dc}=42A and R_g=22 Ω, corresponding circuit is simulated in LTSpice and switching waveforms belong to S5 to S1 and S1 to S5 transitions are given in Figure 3.36(a) and Figure 3.36(b) respectively. As can be seen from corresponding figures, although the voltage overshoot does not reach rated blocking voltage, switching waveforms include high-degree of ringing even with a high external gate drive resistance.

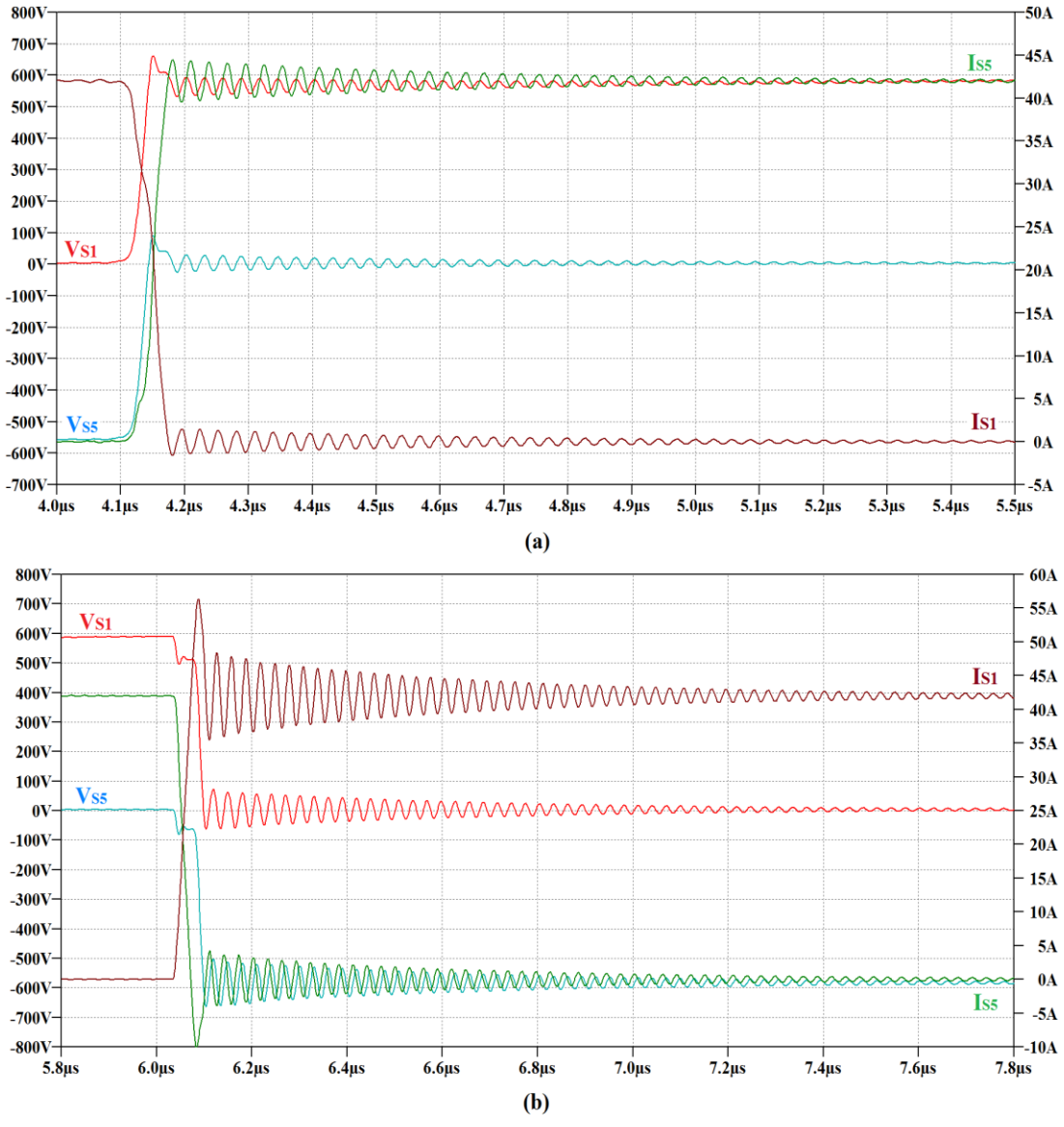
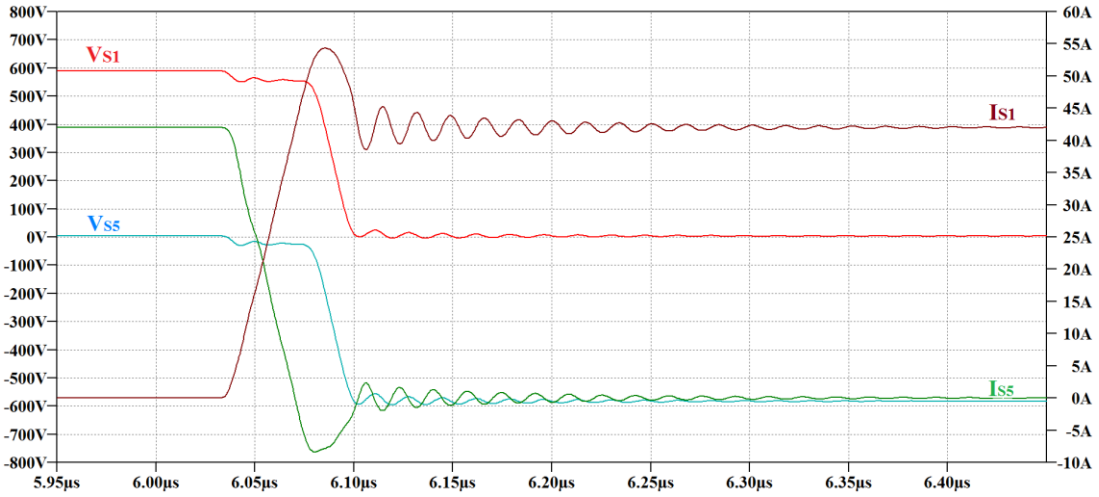
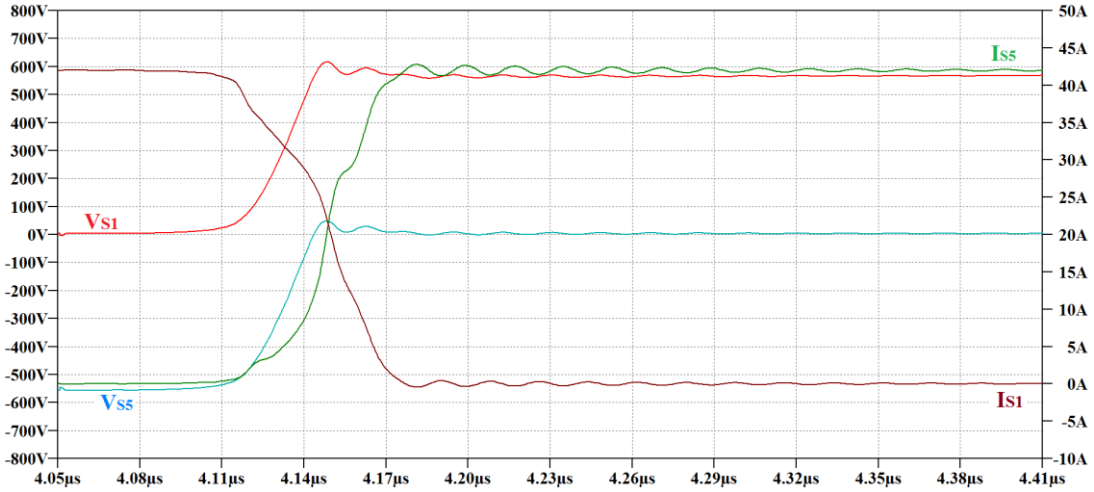


Figure 3.36 Switching waveforms for (a) S5 to S1, (b) S1 to S5 commutations with Rg=22 Ω, Ls=10 nH, ESL=20 nH, Ltrc =40nH

In order to improve switching performance, the parasitic inductance of the commutation loop is minimized by following layout practices. As the parallel (stacked) conductor geometries provide significantly less parasitic inductance than coplanar (side by side, see Figure 3.34) geometries [79], power stage will be constructed on a 4-layer PCB as illustrated in Figure 3.35. Filter capacitor bank is connected in Δ-configuration since it decreases apparent ESL significantly. and physical length of the commutation loop is specifically reduced by approaching the filter capacitors to the semiconductor terminals. For the conductors on the same PCB layer, the IPC-2221 Generic Standard on Printed Board Design recommends 3mm of spacing (t in Figure 3.34) at 1.2kV for polymer or conformal (A5/B4) coated boards [79]. Having said that, upper bridge (S1,S3 and S5 between each other) and lower bridge (S4, S6 and S2 between each other) semiconductors are placed as close as possible (see Figure 3.38) in order to shrink the commutation loop.



(a)



(b)

Figure 3.37 Switching waveforms for (a) S5 to S1, (b) S1 to S5 commutations with Rg=22 Ω, Ls=10 nH, ESL=10nH, Ltrc =10nH

With these modifications, total commutation loop inductance contribution of filter capacitors is expected to be around 20 nH and stacked PCB trace inductance is expected to decrease to 10 nH. Keeping source inductance, L_s, at 10nH and repeating the same simulation with new stray inductance values and R_g=22 Ω, switching waveforms of S1 and S5 are obtained as given in Figure 3.37. As it can be seen from corresponding figures, oscillations in voltage and current waveforms are significantly reduced. Since high-frequency oscillations increase as the gate resistance decreases, after a series of simulations, gate resistance R_g is chosen to be 22 Ω. Considering afore-mentioned power layout practices, power stage of the PV-CSI is constructed as shown in Figure 3.38.

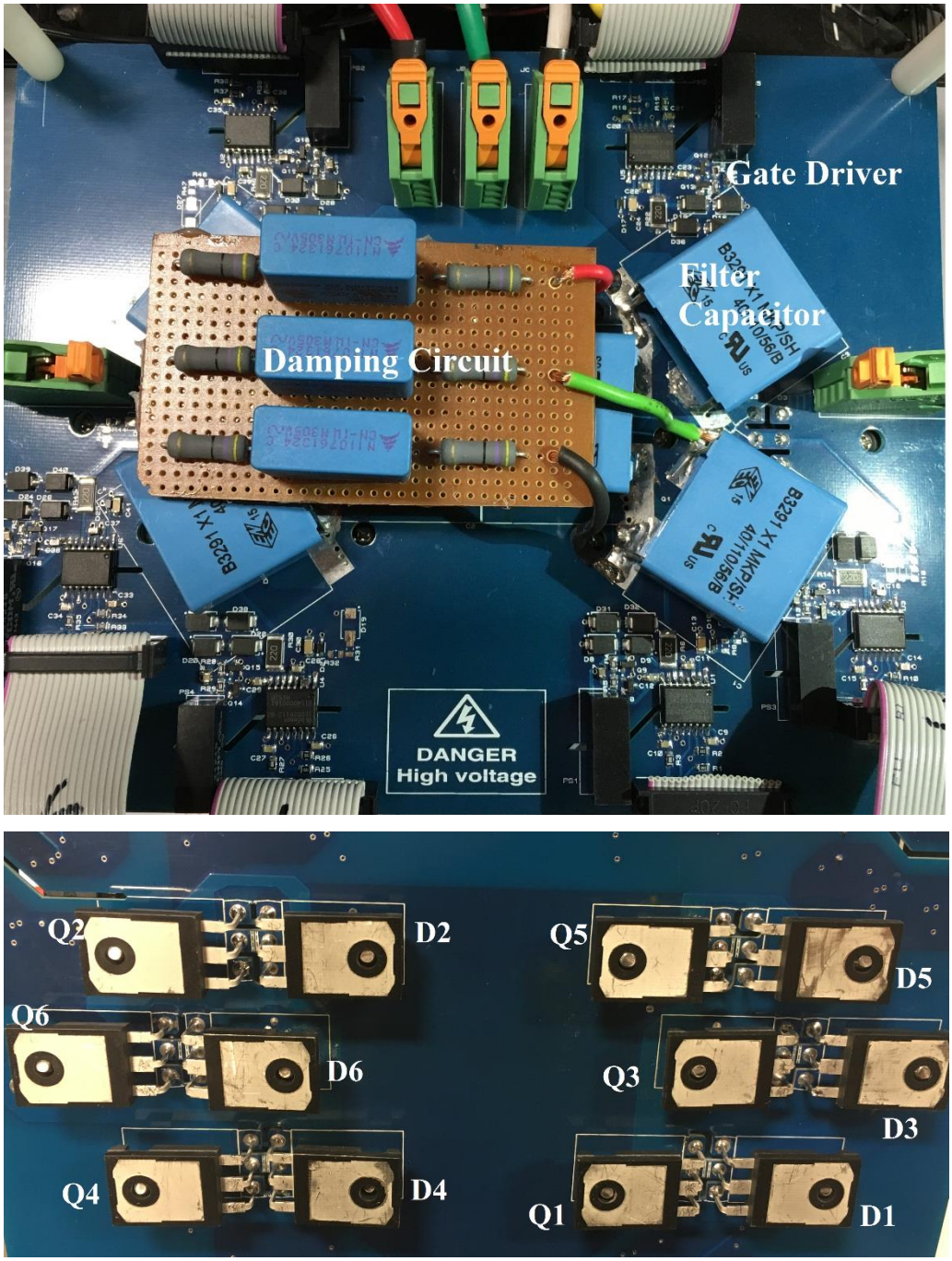


Figure 3.38 Power stage of the PV-CSI prototype (a) top view, (b) bottom view

3.11 Summary

In this chapter, design principles of SiC based 20 kVA PV-CSI have been presented. Initially, the voltage, current ratings of semiconductors have been determined using design specifications and operation principles of CSI. Then, the power switches are selected from commercially available SiC MOSFETs and SBDs with an efficiency oriented approach. Then, using calculated switching losses, carrier frequency is selected as 25 kHz in order to keep switching losses at an acceptable level while decreasing the size of passive components. Then DC-link filter is designed using the specified carrier frequency and specified DC-link current and PV array voltage peak-to-to peak ripple limits. In the next step, design of the output filter and passive damping circuitry have been presented. Then, the controller architecture which includes the DSP board and voltage and current measurement boards explained briefly. Finally, design of the power stage is explained in view of implemented layout practices to minimize commutation loop stray inductances. Components of the laboratory prototype of SiC based PV-CSI are listed in Table 3.5. In the next chapter experimental results of designed laboratory prototype will be presented

Table 3.5 Components of SiC based PV-CSI

Component	Value	Specification	Physical design
S1-S6		1200V-60A [74]	C2M0040120D
D1-D6		1200V-54A [75]	C4D40120D
*C*f	1.0 uF x 2	530 Vac	EPCOS B32914A5105M
*C*dc	3.0 uF	900Vdc	VISHAY MKP1848530094K2
*C*d	1.0 uF	305 Vac	EPCOS B32924H3105M
*R*d	47 Ω x 2		
*L*dc	2.0 mH	Idc=42A	Metglas, AMCC-500, 50x2mm foil,N=64

CHAPTER 4

EXPERIMENTAL RESULTS

4.1 Introduction

This chapter presents the experimental results obtained from the laboratory prototype of SiC based PV-CSI which is designed in previous chapter. During the laboratory tests, developed system has been tested at different operating conditions in order to evaluate the performance of developed inverter in solar applications. Laboratory setup is based on the PV array shown in Figure 4.1. This PV array includes five parallel strings, where each string was constituted with 20 series connected CSUN255-60P modules.

I-V characteristics of CSUN255-60P has been given in Chapter 2 and maximum number of series connected modules in a string was specified as 15. According to characteristics of the corresponding PV module, rated power of the inverter can be obtained around standard test conditions (irradiance 1,000 W/m², module temperature 25°C). However, these two conditions are not available together most of the time. Measurements have shown that PV cell temperature reaches 60 ºC at noontimes in summer season. Therefore, in order to be able to test the developed inverter under rated power, laboratory setup uses 18 modules in each string. Developed laboratory setup does not include additional filter reactors as explained in Chapter 3. Detailed description of the laboratory setup will be presented in the following section.

Figure 4.1 PV array used in the experiments

In this Chapter, current and voltage waveforms of power semiconductors will be given in order to verify the design criteria and demonstrate operating characteristics of CSI. Voltage and current waveforms both on AC and DC sides of CSI based PV system will be presented at various operating conditions in order to show the compliance of the developed system with the corresponding standards. Measured efficiency of the developed system at different operating conditions will then be presented and compared with the efficiency profile given in Chapter 3.

Measuring apparatus that are used for the records are listed in Table 4.1. Measurements are taken with the use of two oscilloscopes: WaveJet 324 from Lecroy which has analog bandwith of 300 MHz and a data acquisition capability of 500K samples and MDO4054 from Tektronix which has an analog bandwith of 500 MHz and the data acquisition capability of 20M samples. Inverter output current waveform quality has been analyzed by using PW3198 power quality analyzer from HIOKI and 9661 clamp on current sensors from the same manufacturer. Since the upper bandwidth of 9661 is specified as 5 kHz, output current waveforms are also recorded

with Pearson Model 110 current transducer with an upper bandwidth limit of 20 MHz in order to analyze carrier frequency harmonics. Measurements of system voltages including voltage measurements of semiconductors performed with Keysight N2891A high voltage differential probes and currents through power semiconductors were measured with battery powered CWT06 ultra-mini Rogowski coil has a bandwidth of 34 Hz-30MHz. Rogowski coil is an electrical device for measuring AC currents or high current pulses. Since a Rogowski coil has an air core unlike the other types of current transformers, it can respond to fast-changing currents. Furthermore, CWT06's thin coil enables current measurements through TO247 pins. DC-link current has been measured with Fluke 80i-110s AC/DC current probe. Whereas, AC component of the DC-link current recorded with Pearson Model 110 current transducer.

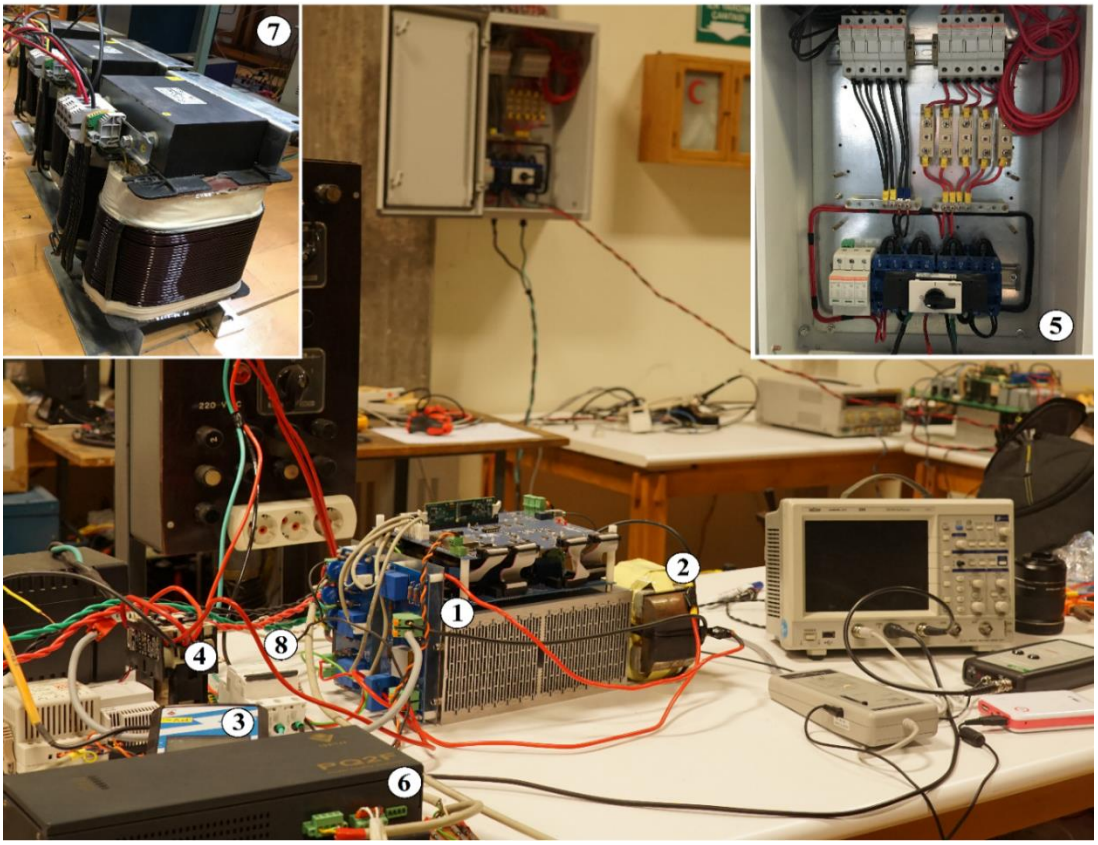
Finally, output power and input power of the inverter has been measured by using PQ++ power quality analyzer and DC power measuring device respectively. A more detailed explanation about the measurement of efficiency will be presented in section 4.6.

Table 4.1 List of Measurement Devices

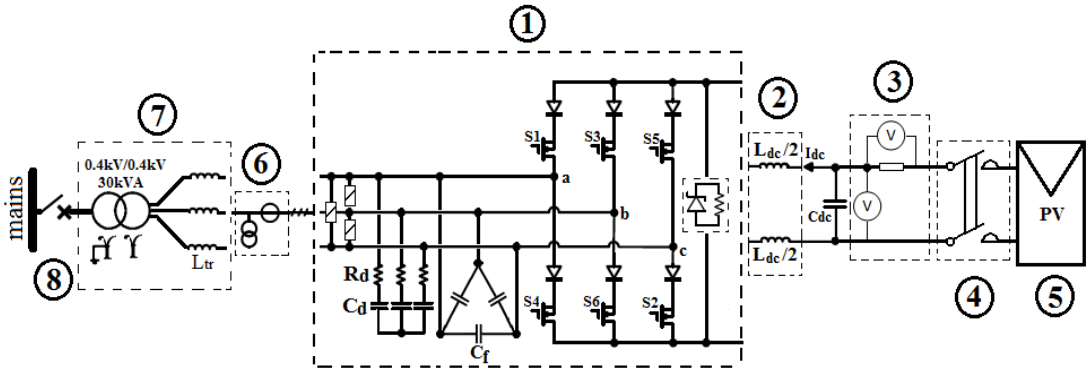
LeCroy WaveJet 324 Oscilloscope
Tektronix MDO4054C Oscilloscope
HIOKI PW3198 Power Quality Analyzer
PQ^{++} Power Quality Analyzer
Fluke 80i-110s Current Probe
Pearson Model 110 Current Monitor (20 MHz)
CWT06 ultra-mini Rogowski coil (34 Hz-30MHz)
Keysight N2891A High Voltage Differential Probe (70 MHz)
DC power meter based on precision resistance

4.2 Laboratory Prototype

The view and simplified circuit diagram of the constructed test setup are given in Figure 4.2 and enumerated components in this figure listed Table 4.2 Enumeration of the components in the test setup.



(a)



(b)

Figure 4.2 a) view, b) simplified schematic of the laboratory test setup

Table 4.2 Enumeration of the components in the test setup

1	power stage and controller hardware	5	PV combiner box
2	DC-link inductor	6	PQ^{++} Power Quality Analyzer
3	Input power measurement circuit	7	Coupling transformer
4	DC contactor	8	AC circuit breaker

4.3 Test Results

4.3.1 Switching Waveforms

Before employing system tests, the effect of stray inductance on each possible commutation path (an example path given for S1 and S3 in Figure 3.32) in CSI power stage had been tested using the switching test setup given in Figure 4.3. Corresponding test setup is built on the designed power stage by adding an additional aluminum electrolytic bulk capacitor bank which behaves as a constant DC voltage source for a short switching period.

Figure 4.3 illustrates the commutation between S1-S5 which take place on the longest commutation path along with the commutation between S2-S4 on the constructed power stage. Initially, capacitor bank is charged up to 560V by an external voltage source. Later, S4 and S5 are turned-on until I_{dc} reaches its rated value (42A). As I_{dc} reaches 42A, S1 is turned-on and S5 turned-off, where inductor current I_{dc} is transferred from S5 to S1 and freewheels through S1 and S4.

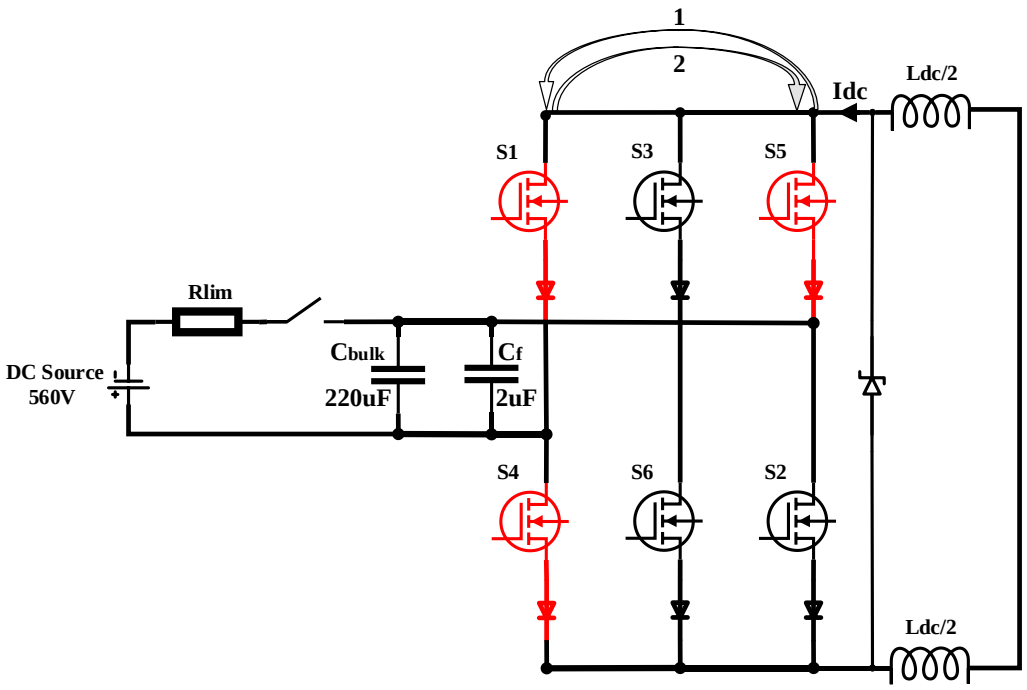


Figure 4.3 Switching test setup

After a few µs, S5 is turned-on and S1 is turned-off, where inductor current is transferred back to S5. Finally, S1 is turned-on and S5 is turned-off where inductor current (I_{dc}) freewheels through S1 and S4 until its energy is discharged on the semiconductors. The on-state gate voltage is selected as +20 V and off-state gate voltage selected as -5 V for MOSFET and R_g is 22 Ω. The overlap time is 100 ns. For the switching tests, semiconductors are not mounted on a heatsink and ambient temperature is measured to be 24 ^oC. Semiconductor currents are captured using CWT06 (34 Hz-30MHz) and semiconductor voltages are captured using N2891A (70 MHz). Since the sensitivity of CWT06 specified as 50mV/A (20x division) and gain of the corresponding current channels are set to 10x, each vertical division on the scope screen corresponds to 10A for semiconductor currents. Figure 4.4 and Figure 4.5 shows voltage and current waveforms that belong to S1 to S5 and S5 to S1 commutation events respectively.

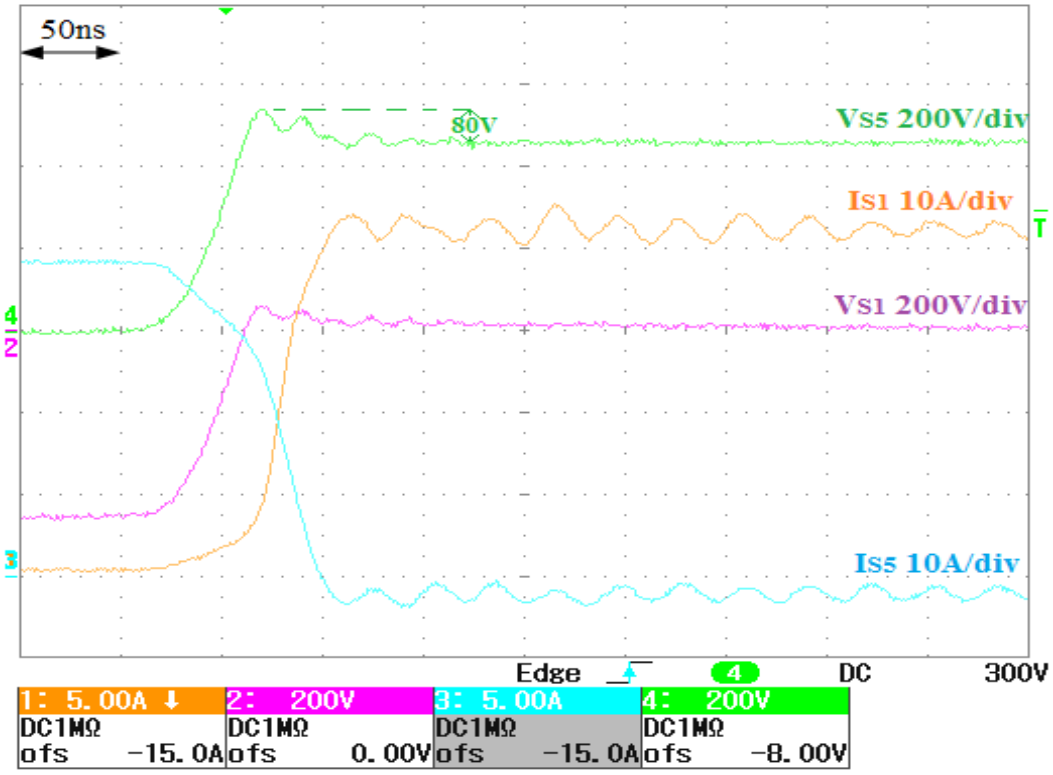


Figure 4.4 Switching waveforms belong to the S5 to S1 commutation event, Ch1: S1 current (orange, 10A/div), Ch2: S1 voltage (pink, 200V/div), Ch3: S5 current (blue, 10A/div), Ch4: S5 voltage (pink, 200V/div), time scale 50ns/div, sampling rate 1 GS/s

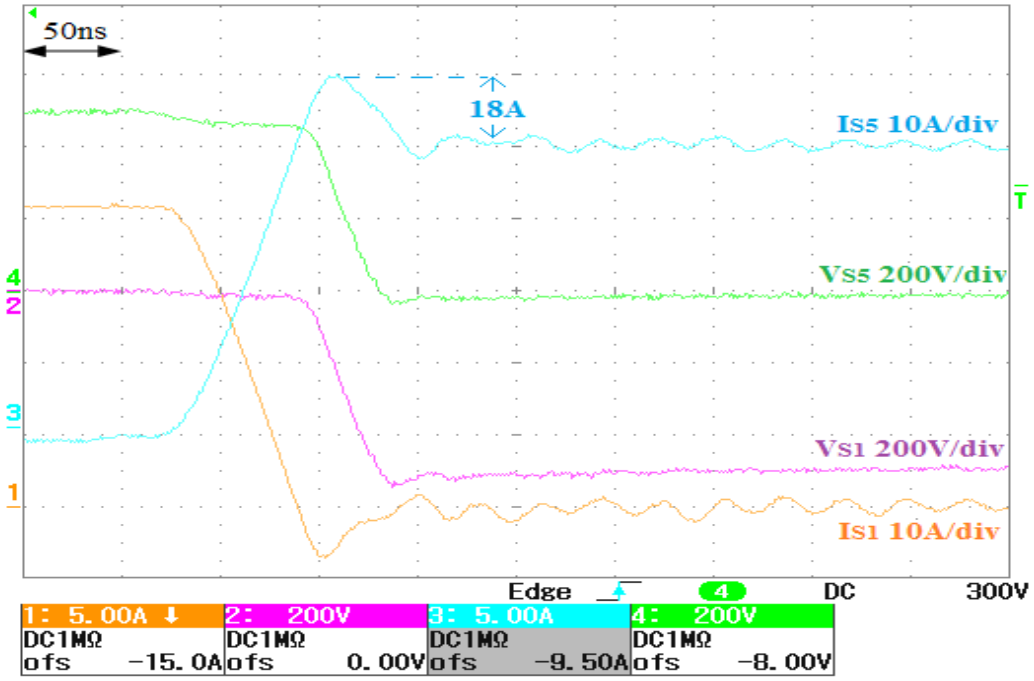


Figure 4.5 Switching waveforms belong to the S1 to S5 commutation event, Ch1: S1 current (orange, 10A/div), Ch2: S1 voltage (pink, 200V/div), Ch3: S5 current (blue, 10A/div), Ch4: S5 voltage (green, 200V/div), time scale 50ns/div, sampling rate 1 GS/s

It has seen that switching waveforms show similar characteristics with the simulated switching characteristics given in Figure 3.37. In the S5 to S1 commutation event, turn-off of SiC MOSFET of S5 occurs and SiC MOSFET of S5 blocks positive voltage. High rate of decay in current through commutation path due to fast turn-off of SiC MOSFET, an overvoltage of 80V is superimposed on off-state voltage of S5

Maximum voltage exposed by the semiconductors was calculated to be around 670V (considering the filter capacitor high frequency voltage ripple together with the %10 rise of the mains voltage). Therefore, maximum voltage blocked by the MOSFETs will be 750V in the turn-off process. Before S5 is turned-off, voltage drop on the MOSFET associated with S1 is approximately zero and negative voltage on S1 is blocked by the series diode that belong to S1. Although S1 receives turn-on signal 100 ns (overlap time) earlier than S5 receives turn-off signal, switching process will not start until the overlap time elapses. As S5 turn-off process starts, voltage on the corresponding S1 diode decreases to zero and S1 current builds up under zero

MOSFET voltage resulting in a negligible switching loss. A small amount of high frequency ripple is observed on S5 and S1 currents after the commutation event as a result of interaction between S3 and S5 parasitic capacitances and stray inductance of S1. Corresponding high frequency ripple is damped in 600ns after switching process is completed.

On the other hand, S1 to S5 commutation process starts immediately after S5 receives turn-on signal. Negative voltage on the S1 blocked by the associated series diode and the voltage drop on the MOSFET associated with S1 stays around 0 V after the commutation. Although the employed SiC Schottky diode is a majority carrier device, it has still reverse recovery charge which results purely from capacitive charging of the reverse biased junction during turn-off. Capacitive charging of the reverse biased junction results in a reverse current of -8A on S1 during turn-off as shown Figure 4.5 which results in a switching loss much lower than S5. Corresponding S1 current and output capacitance discharge currents of MOSFETs associated with S3 and S5 switches results in an current overshoot of 18A on S5 as shown in Figure 4.5. Finally, it can be pointed that the switching times consistent with the values specified in the corresponding device datasheet [74].

4.3.2 Performance of the Overvoltage Protection Circuit

This part presents performance of the designed overvoltage protection circuit given in Figure 3.28. Performance of the designed clamping circuit has been evaluated with procedure illustrated in Figure 4.6. In this experiment, an electrolytic capacitor is charged up to $\approx 220Vdc$ with an external variable DC power source.

Then, taking S5 and S2 into ON-state, DC-link current is built up through a current limiting resistor. When the inductor current exceeds maximum expected inductor current ≈44A, both of the semiconductor switches taken into OFF-state and overvoltage protection circuit takes over the inductor current. Recorded inductor current and DC-link voltage test waveforms are presented in Figure 4.7. In this record, inductor current has been captured using CWT06 and DC-link voltage has been captured using N2891A.

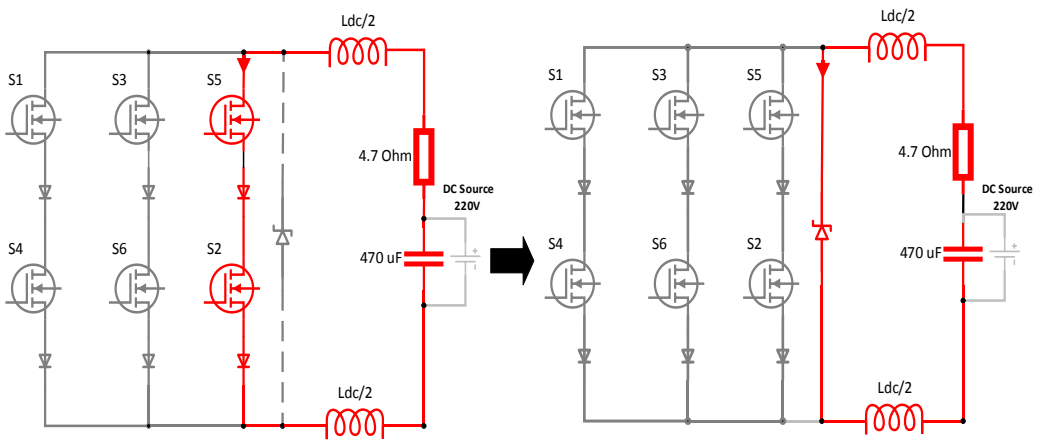


Figure 4.6 Test of overvoltage protection circuit

Since the gain of CWT06 specified as 50mV/A (20x division) and gain of the channel 1 (blue waveform) is set to 10x, each vertical division on the scope screen corresponds to 10A for channel 1 instead of 5A as shown in the scope screen.

When the shorting branch is turned off at time t_1, DC-link voltage is clamped at around ≈800 V and the inductor energy is dissipated on the TVS diodes in ≈130 µs. At time t2, current vanishes and TVS diodes goes into high impedance state. However, at time t1 DC-link voltage exhibits a large overshoot (reaching up to 1.2 kV) for a short time duration before the protection circuitry fully takes over the inductor current. Since this pulse will stay single avalanche SOA of the employed MOSFET, it could be handled by MOSFET as explained in section 3.8.

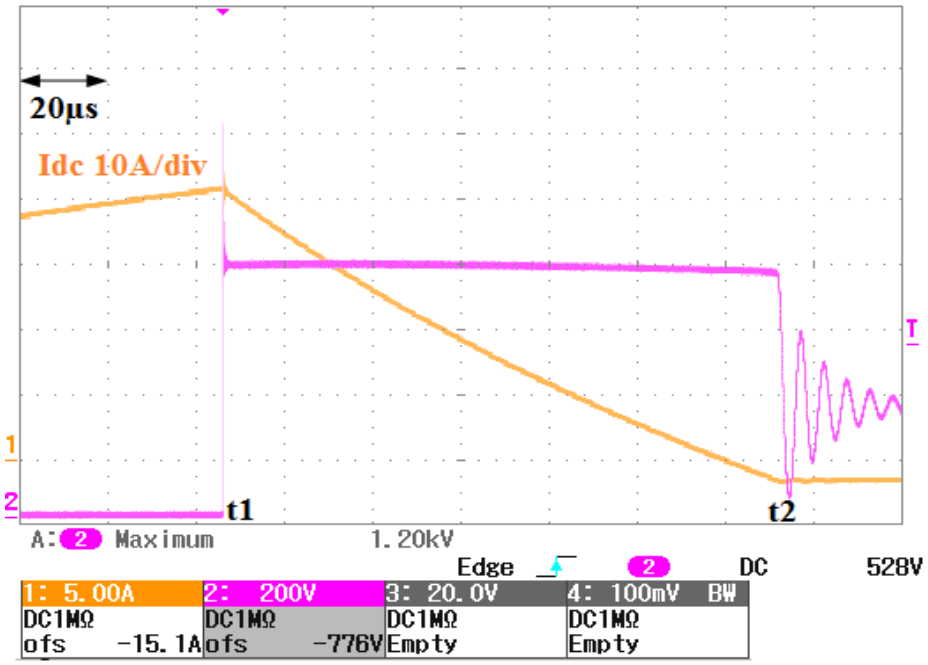


Figure 4.7 Overvoltage protection waveforms in case of an inductor current interruption, inductor current (Ch1:orange, 10A/div), DC-link voltage (Ch:2, pink, 200V/div), time scale 20µs/div

4.3.1 DC-Link Voltage and Current Waveforms

In order to observe the maximum PV array voltage ripple and inductor current ripple, PV-CSI prototype is operated in open-loop at a fixed modulation index of 0.8 (m=0.8) using the setup given Figure 4.2. In this experiment, voltages measured with Keysight N2891A high voltage differential probe and DC-link and AC output currents are measured with Fluke 80i-110s current probe. Due to limited bandwidth of Fluke 80i-110s (100 KHz), DC-link current also recorded with Pearson Model 110 current transducer in order to observe the AC component of the DC-link current accurately. As it can be seen from Figure 4.8, the maximum peak to peak ripple of the DC-link current is measured to be 2A as specified in Chapter 3. Unfiltered DC-link voltage is given in Figure 4.9, PV array voltage is given in Figure 4.8 and Figure 4.10 when operating at m=0.8 and m=1.0 respectively. As specified in Chapter 3, PV array voltage ripple (ΔV_{pv}) limited to 2% ($\approx$ 10V) of MPP voltage in the steady state.

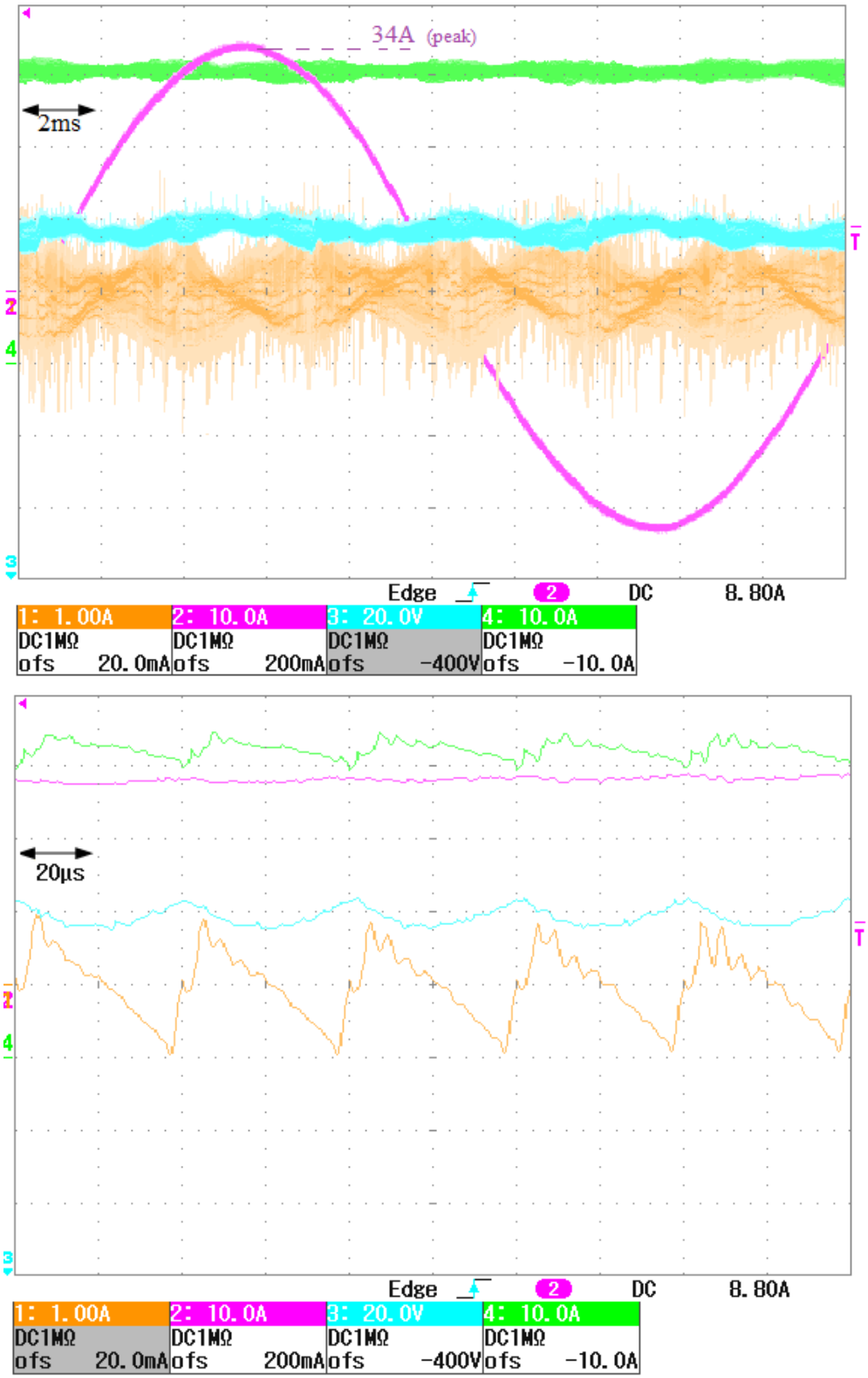


Figure 4.8 DC-link waveforms at I_{pv}=42A and *m*=0.85, Ch1: AC component of I_{dc} (orange, 1A/div), Ch2: phase A current (pink, 10A/div), Ch3: V_{pv} (blue, 10V/div, offset=-400V), Ch4: I_{dc} (DC+AC)(green, 10A/div), (upper: 2ms/div, 25MS/s, lower: 20us/div, 1GS/s)

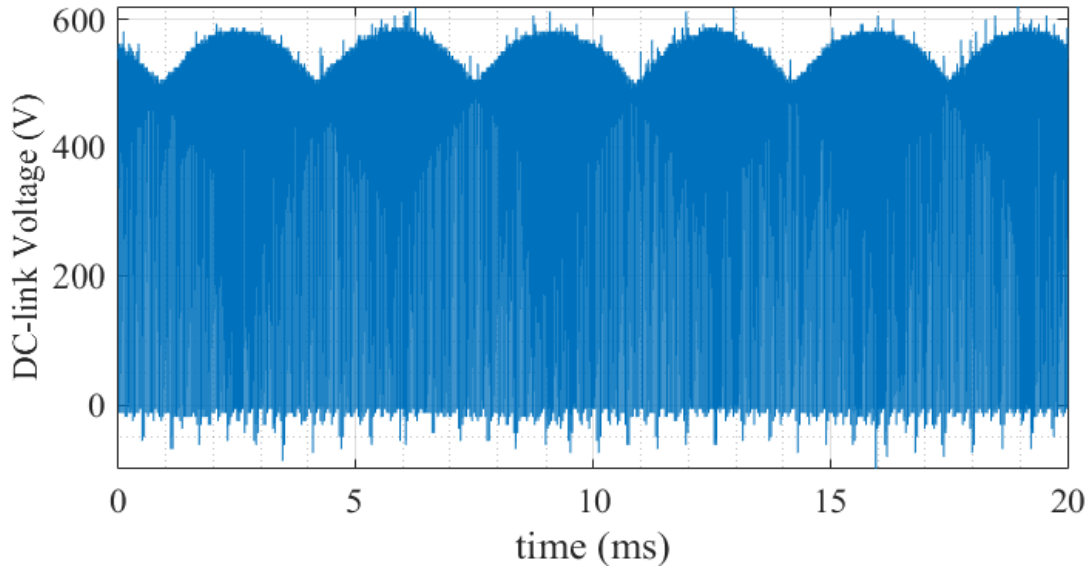


Figure 4.9 DC-link voltage waveform at m=0.83, sampling rate 25MS/s

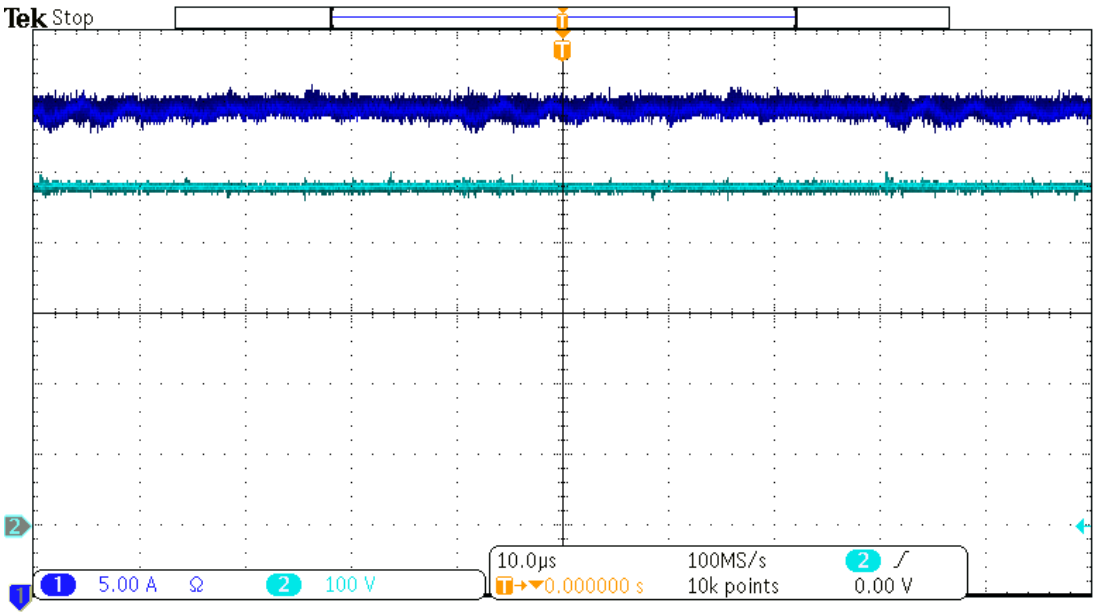


Figure 4.10 PV array voltage and current waveforms at rated DC-link current and for *m*=1.0

4.3.2 MPPT Response of the Inverter

Performance of the MPPT controller can be evaluated on the start-up current and voltage waveforms of the PV array given in Figure 4.11. In this test PV array surface temperature is measured to be 57 ºC and solar insolation is measured as 990 W/m^2.

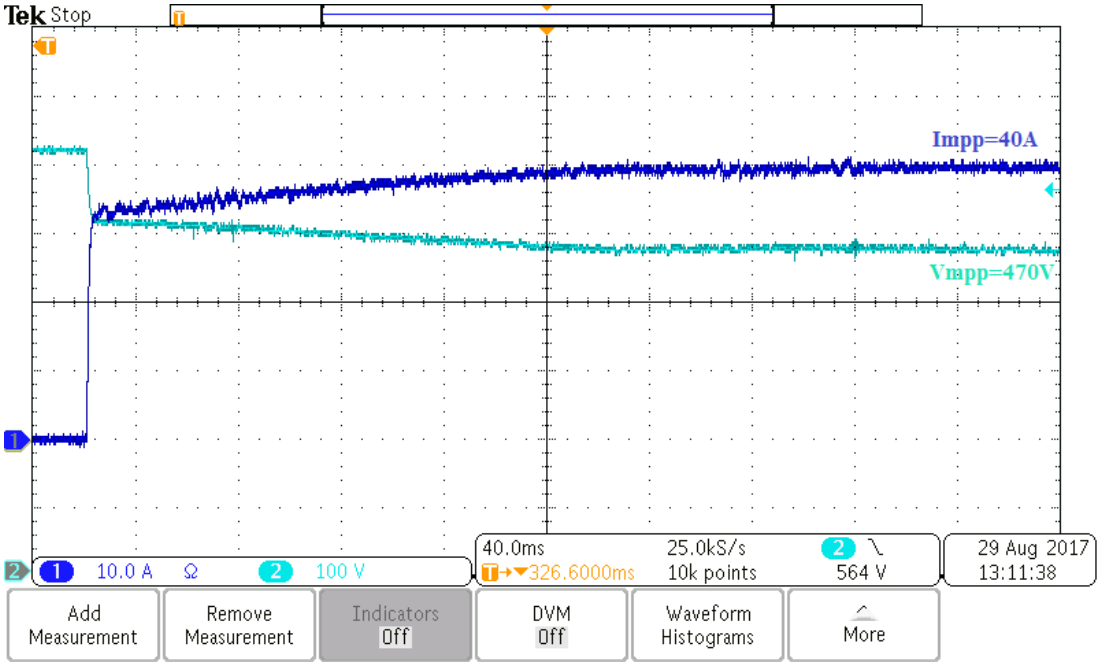


Figure 4.11 I_{pv} (blue) and V_{pv} (light blue) waveforms during start-up

As explained in section 3.9, maximum possible DC-link voltage (for m=1.0) applied to PV array terminals is 489V under nominal grid voltage and it decreases proportionally with the modulation index (m). At the beginning of the start-up process of the inverter, modulation index is set to 1.0 in order to set the PV array voltage to the maximum possible DC-link voltage and draw minimum DC-link current. Since the maximum DC-link voltage is smaller than the open circuit voltage of the PV array, input current of the inverter increases 30A within a few switching cycle and then, MPPT controller increases the input current of the inverter to MPP current within ≈160ms. It has seen that MPPT performance of the CSI in the laboratory matches with the simulation results.

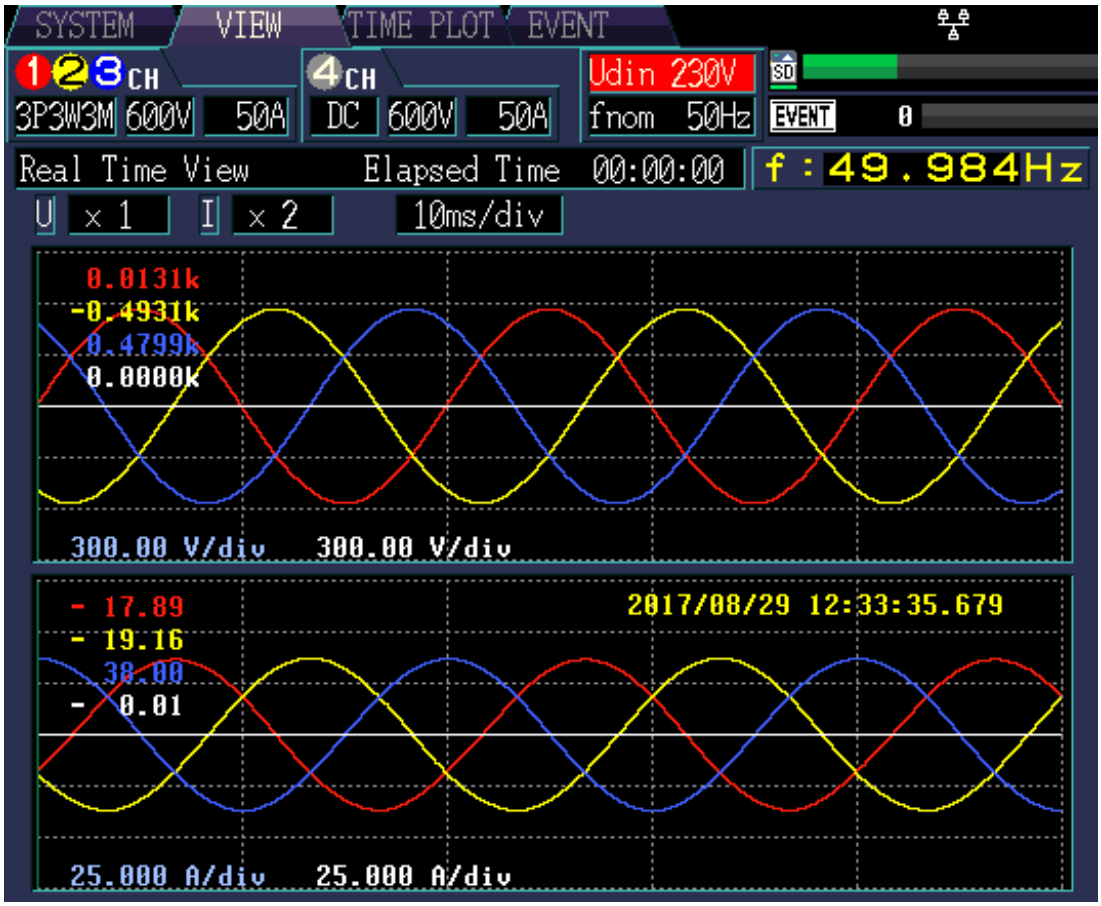
4.3.3 Harmonic Content of the Output Current Waveforms

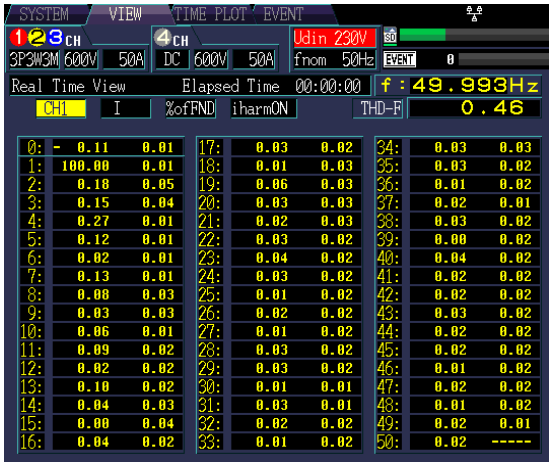
AC side phase current and line voltage waveforms have been recorded at different output power levels with the use of PW3198 power quality analyzer from HIOKI using 9661 clamp on current sensors from the same manufacturer. Output current waveforms

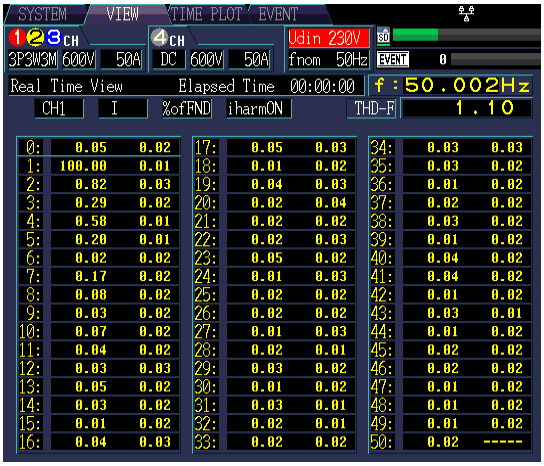
measured at the grid side of the coupling transformer for 19kW, 11kW and 3kW output power given in Figure 4.12, Figure 4.13 and Figure 4.14 respectively. For each power level, individual harmonics up to the 50th order and THD values at both the grid side and at the converter side of the coupling transformer are also given in corresponding figures. Although the measurement uncertainty of the employed current sensors (0.6%) is higher than the limits (0.3%) in [8] for the harmonics above the 33rd order, corresponding records give a good idea about the THD of the current waveforms and the harmonic content at the resonant frequency (1.6 kHz) of the output filter. It is worth to note that the reported THD values in Figure 4.13 and Figure 4.14 must be proportioned to the fundamental frequency current at rated inverter output power. Since the upper bandwidth of current sensors used with power quality analyzer is specified as 5 kHz, in order to evaluate the high frequency content of the inverter output currents, an additional measurement of output current also performed with Pearson Model 110 current transducer (20 MHz) and a sample record given with the harmonic spectrum of the output current at the grid side of the transformer in Figure 4.15.

It has been seen that both measurements result similar THD values with a small discrepancy due to the magnetizing current of the coupling transformer superimposed on the grid side currents. Additionally, there is not a visible harmonic content around the corner frequency of the output filter (1.6 kHz) indicating a successful damping.

Both measurements have shown that designed PV-CSI produces very clean output current waveforms and comply with the harmonic limits given in [8], over the entire operating range.

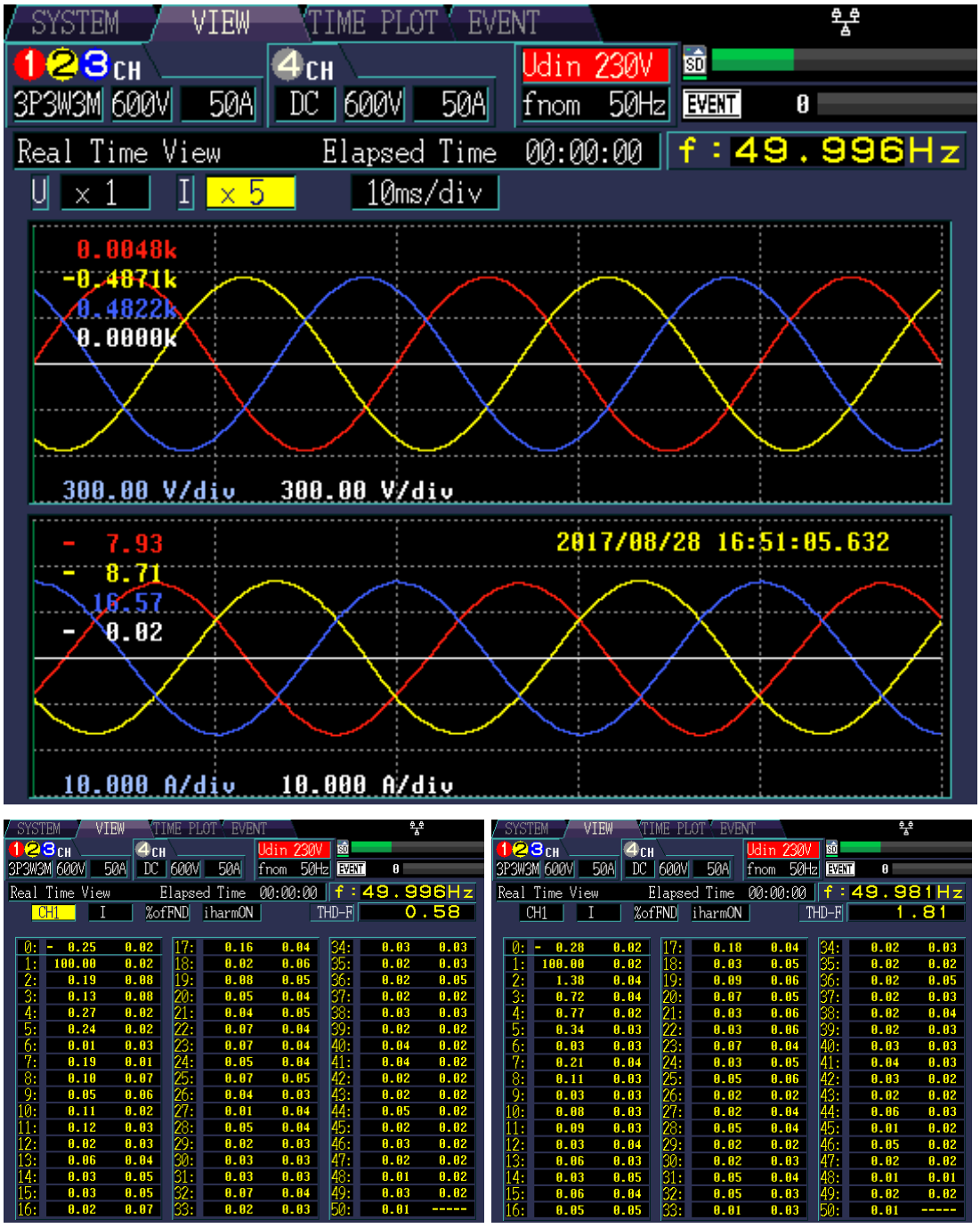






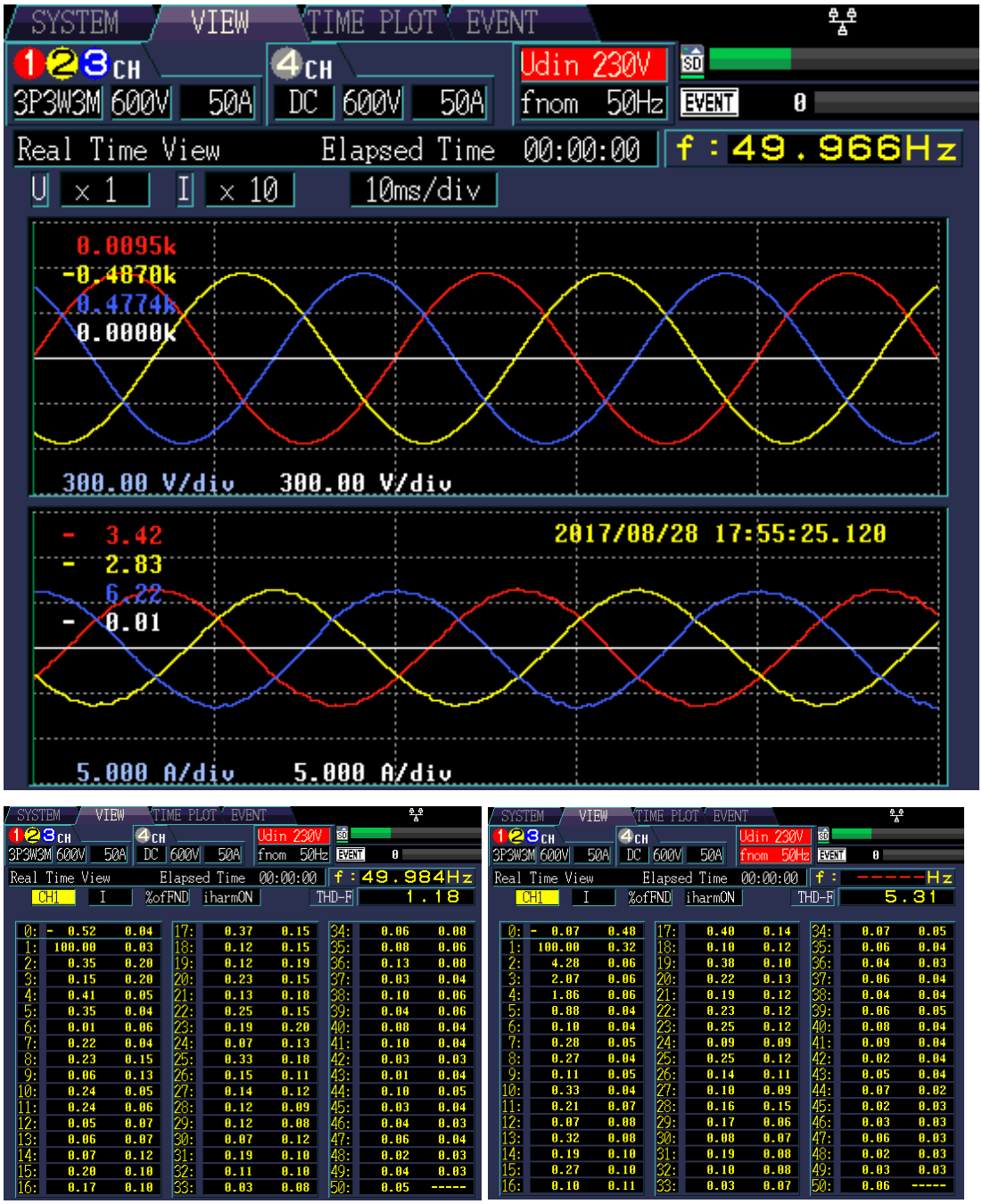
(a) **(b)**

Figure 4.12 AC side line current waveforms (grid side) of PV-CSI at 19 kW and their harmonic spectra at (a) converter side, (b) grid side of the transformer



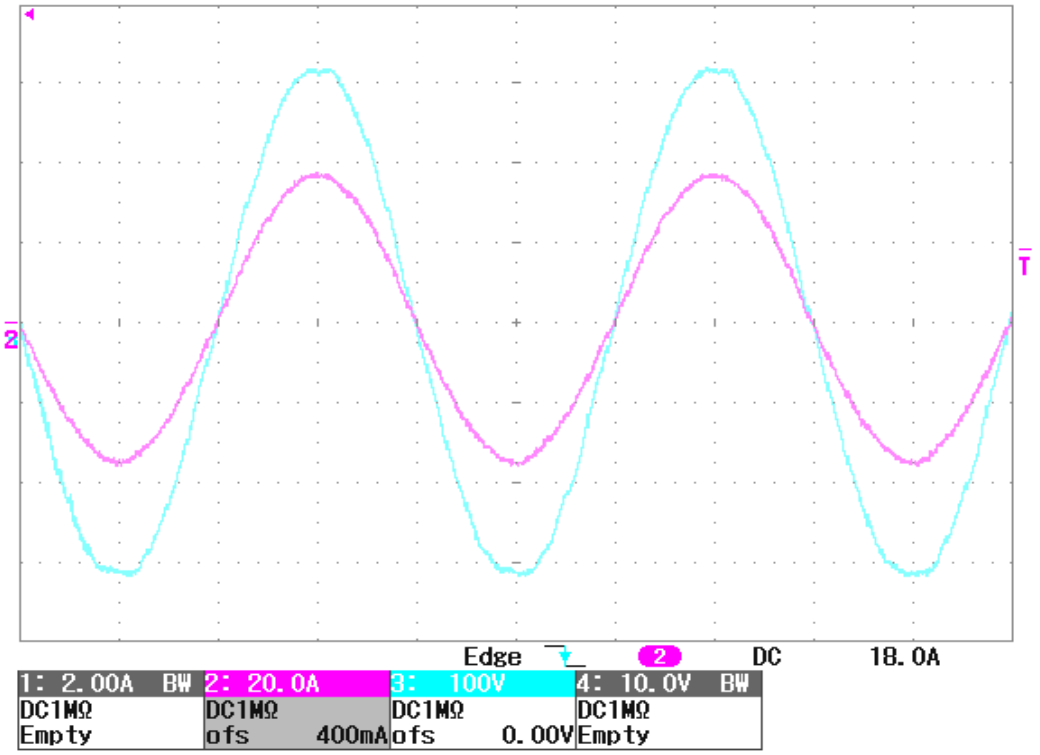
(a) **(b)**

Figure 4.13 AC side line current waveforms (grid side) of PV-CSI at 11 kW and their harmonic spectra at (a) converter side, (b) grid side of the transformer

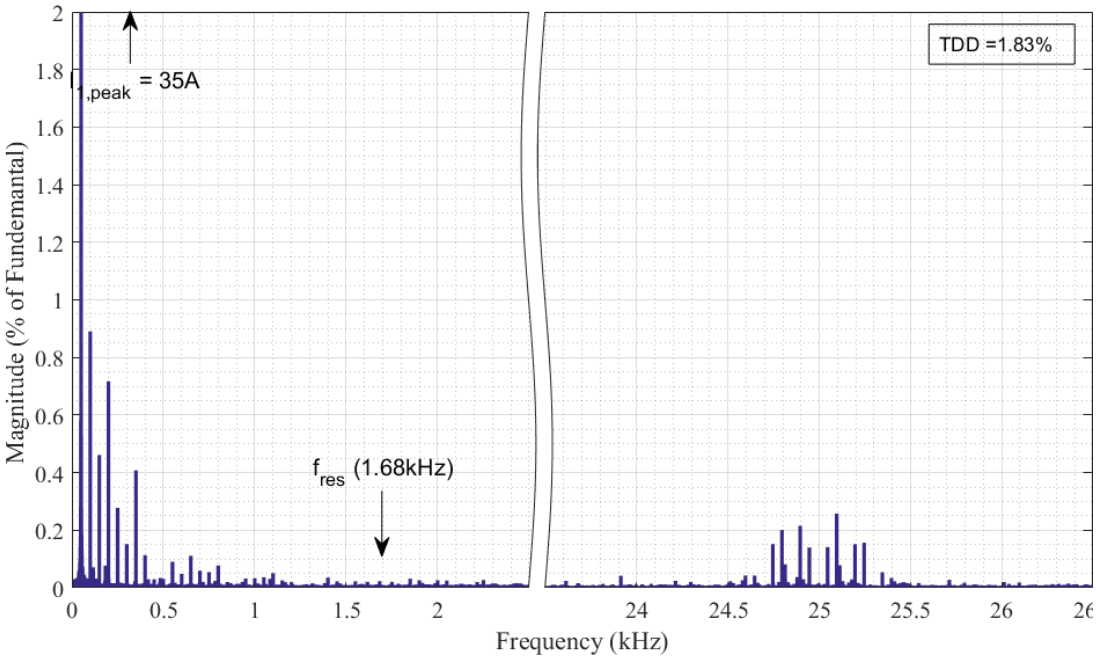


(a) **(b)**

Figure 4.14 AC side line current waveforms (grid side) of PV-CSI at 3 kW and their harmonic spectra at (a) converter side, (b) grid side of the transformer



(a)



(b)

Figure 4.15 (a) Waveforms of grid voltage (Ch:3, blue, 100V/div) and currents injected to grid (Ch:2, pink, 20A/div) at the grid side of the coupling transformer,(b) harmonic spectra of the output current for Idc=42A, *m*=0.83 (time/div=5ms, sampling rate=10 MS/sec)

4.3.4 Efficiency measurement

In order to explain different techniques for determining the power conversion efficiency η, the following simple equation is used.

$$\boldsymbol{\eta} = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{loss}}} = \frac{P_{in} - P_{\text{loss}}}{P_{\text{in}}} \tag{4.1}$$

Where η is the overall power conversion efficiency of the inverter, P_{in} the input power, P_{out} the output power from the converter, and P_{loss} the total power loss. The equation shows there are three options for calculating the efficiency. First, measuring the output power (P_{out}) and input power (P_{in}), secondly measuring the output power (P_{out}) and the power losses (P_{loss}). and finally, measuring the input power (P_{in}) and the power losses (P_{loss}). The accuracy of the calorimetric method has been shown to be superior compared with the input–output method [83]. The low uncertainty of efficiency achieved by calorimeters (constant accuracy for losses) makes them suitable as a reference measurement for the input–output method with high-efficiency devices [82,83].

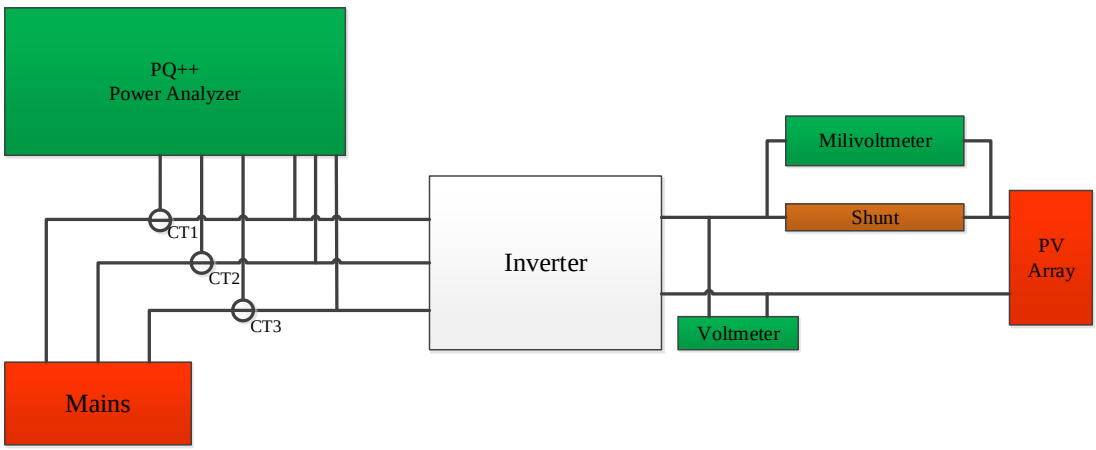


Figure 4.16 Block diagram illustrates the set-up used to measure the efficiency of CSI

Although the calorimetric method is more appropriate for high efficiency converters, the measurement of the power losses is not easy and very time consuming and requires

a calorimeter system. Because of that, efficiency measured based on the measurements of P_{in} and P_{out} using the setup given in Figure 4.16.

For the calculation of power conversion efficiency, a measurement accuracy better than ±0,5% of the full-scale value is recommended for each power measured [87]. The PQ^{++} Power Quality Analyzer, used for the measurement of output AC power, conform to IEC 61000-4-30 Class A instrument requirements. Its voltage and current measurement uncertainty is limited to 0.1% of nominal input voltage and nominal input current. DC power measurement device uses a 0.1 mΩ shunt resistor with a temperature coefficient of 100ppm/°C. Corresponding device calibrated at 500V and 10A with the use of Fluke 289 true-rms multimeter, which has a measurement accuracy of 0.03% for voltage measurement and of 0.3 %. Current measurement

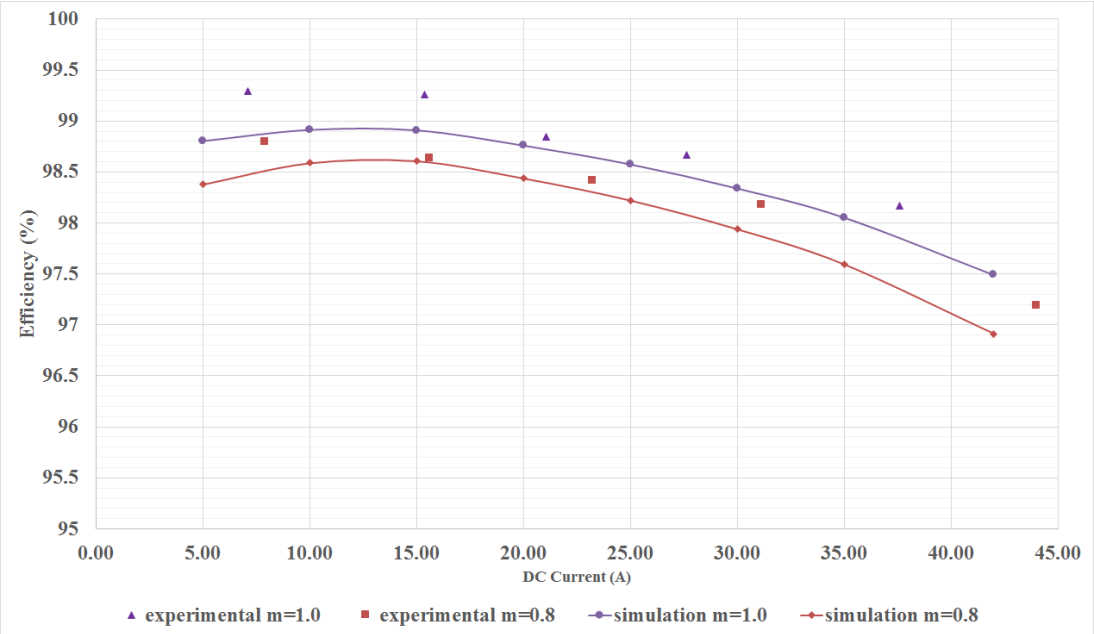


Figure 4.17 Measured and calculated efficiencies of PV-CSI at different DC-link current values for *m*=1.0 and *m*=0.8

Using the setup shown in Figure 4.16, input and output power of SiC based CSI prototype designed for PV applications is measured at different DC-link current values

for maximum (m=1.0) and minimum (m=0.8) modulation indices at an ambient temperature of 27 ^{o}C. Measured efficiency values are given with calculated efficiency profile in Figure 4.17.

Although there is a small discrepancy between the calculated and measured efficiency values, especially at low power levels, due to the power measurement errors, both profiles show similar trend. It has been seen that the highest efficiency of the inverter is achieved at one third of the rated output power and then decreases exponentially with the increasing output power. Moreover, efficiency of the inverter decreases with the decreasing MPP voltage and correspondingly with decreasing modulation index. However, the achieved efficiency values are still remarkable since the CSI based PV inverter does not require an additional DC/DC conversion stage.

CHAPTER 5

CONCLUSIONS AND FUTURE WORK

5.1 Conclusions

The design and implementation of a high efficiency three-phase single stage CSI based PV inverter which has a power rating of 20 kVA has been carried out in this research work. A prototype has been designed and developed as a high efficiency multi-string inverter (excluding DC/DC converter stages) which can be used in large scale PV applications as an alternative to the central inverters when paralleled at LV side of a dedicated coupling transformer.

Implemented laboratory prototype of the CSI based PV inverter is composed of a single stage full-bridge current-source converter built with SiC MOSFETs and SiC Schottky diodes. Line currents are modulated by using Modified Dead-Band Sinusoidal Pulse Width Modulation technique (MDSPWM) with a carrier frequency of 25 kHz. Designed inverter employs an LC low-pass output filter and a R-C type passive damping circuit connected in parallel with the filter capacitors.

This research work shows that CSI based PV string inverter has many advantages over VSC based central inverters, such as

- Elimination of requirement for high DC-link voltage,
- Shorter DC cables between PV strings and the inverter,
- Output power can be expanded,
- Lower power losses due to the distributed MPPT.

Designed inverter performs successfully for all input voltage levels in MPP voltage range with a satisfactory performance at both steady state and transient state. Output currents of the inverter have very low distortion values at partial and rated power levels complying with IEEE Std. 929-2000. TDD of the output currents measured to be less than %2 between 15%-100% of the rated output power.

Efficiency of the laboratory prototype is calculated both experimentally and with the aid of computer simulations. It has been seen that the peak efficiency of the inverter is achieved at one third of the rated output power and it decreases dramatically with the exponentially increasing conduction losses. Designed inverter has a European efficiency of 98.5% when operating at maximum input voltage. However, efficiency of the inverter decreases with the decreasing MPP voltage and European efficiency of the inverter drops down to 98.1% for minimum modulation index (m=0.8). However, the achieved efficiency values are still remarkable since the CSI based PV inverter does not require an additional DC/DC conversion stage.

5.2 Future Work

In this study, semiconductor selection has been performed in a way that the semiconductor junction temperatures (T_j) stay below 125 ^oC for the maximum DC-link current resulting in high conduction losses at rated power. In high efficiency converters, power devices can be overrated in terms of semiconductor continuous current rating or can be paralleled in order to reduce on-state resistance and conduction losses with the expense of increasing switching loss. As a future work, an optimization study may be conducted in order to find optimum on-state resistance involving the initial component costs and long term cost caused by converter losses.

Secondly, DC-link current ripple has been selected as 5% of the rated DC-link current in order to ensure CCM at low irradiation levels which results in a heavy DC-link inductor. If the inverter enters into Discontinuous Conduction Mode, DCM, it can no longer maintain linear relation between input and output voltage and output current waveform quality also decreases. As a future topic, DCM condition can be avoided

with a lower DC-link inductance by increasing switching frequency dynamically as the DC-link current approaches to DCM region. Alternatively, the controller can be modified in order to operate with higher DC-link current ripple and to allow DCM operation at low DC-link current levels, as depicted in [31]

Efficiency of the CSI decreases with the decreasing modulation index due to the conduction losses in the null-state. In order to minimize null-state losses a seventh switch may be added to basic CSC topology, namely CSI7 topology, as proposed in [44]. This topology has also advantages in terms of ground leakage current minimization for transformerless small scale PV-applications. In brief, implementation of CSI7 topology with SiC semiconductors will be an interesting future work topic.

Finally, with the increase in distributed generation based on renewable sources, PV inverters are expected to provide reactive power support under various operating conditions by the grid operators in many countries. Another further work may evaluate the reactive power performance of the designed inverter in detail.

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