DEVELOPMENT OF K BAND MICROSTRIP PATCH ANTENNA ARRAY FOR TRAFFIC RADAR

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
MIDDLE EAST TECHNICAL UNIVERSITY

BY

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IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF MASTER OF SCIENCE
IN
ELECTRICAL AND ELECTRONICS ENGINEERING

NOVEMBER 2017

Approval of the thesis:

DEVELOPMENT OF K BAND MICROSTRIP PATCH ANTENNA ARRAY FOR TRAFFIC RADARS

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ABSTRACT

DEVELOPMENT OF K BAND MICROSTRIP PATCH ANTENNA ARRAY FOR TRAFFIC RADARS

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November 2017, 56 pages

In this thesis work, two microstrip patch antenna arrays are designed for the traffic radar applications. Both of them operate at the 24.125 GHz with 250 MHz bandwidth. Two different series feed networks are used, namely shunt connected series feed network and in line coupled series feed network.

The one with shunt connected series feed network is manufactured and measured to make comparisons with the simulation results. It is observed that simulation and measurement results are very similar. 7 degree beamwidth is achieved in both azimuth and elevation planes as well as less than -14 dB side lobe levels in the radiation patterns.

In the second design, 30 degree and 12 degree beamwidths are achieved for azimuth and elevation planes, respectively. While the side lobe level of the azimuth plane is smaller than -15 dB; in the elevation plane, the side lobe level could only be minimized down to -13 dB due to the existence of delay sections.

Keywords: Microstrip Patch Antenna Array, Shunt Connected Series Feed Network, In Line Coupled Series Feed Network, K Band Antenna Applications

ÖZ

TRAFİK RADARLARI İÇİN K BANDDA MİKROŞERİT YAMA ANTEN DİZİLERİ GELİŞTİRİLMESİ

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Tez Yöneticisi : Prof. Dr. Özlem Aydın Çivi

Kasım 2017 , 56 sayfa

Bu tez çalışmasında trafik radarlarında kullanmak üzere iki mikroşerit yama anten dizisi tasarlanmıştır. İkisi de 24.125 GHz'de 250 MHz bant genişliği ile çalışmaktadır. İki farklı seri besleme tipi kullanılmıştır, biri paralel bağlı seri besleme tekniği, diğeri ise seri bağlaşık besleme yapısına sahiptir.

Paralel bağlı seri besleme tekniği kullanılan dizi üretilmiş ve ölçümleri yapılmıştır. Ölçümler ve simulasyon çok benzer sonuçlar vermektedir. Hem yükseliş hem yanca düzlemlerinde 7 derecelik huzme genişliğine sahiptir. Ölçülen huzme örüntülerinde yan huzme seviyeleri -14 dB'den düşük gözlenmiştir.

İkinci tasarım yanca düzleminde 30, yükseliş düzleminde 12 derecelik ışıma örüntüsüne sahiptir. Yanca düzlemi yan huzme seviyeleri -15 dB'den düşük gözlenmiştir. Tasarım kıvrımlı iletim hatları içerdiğinden, yükseliş düzleminde farklı denemeler yapılarak yan huzme seviyeleri -13 dB'ye kadar düşürülebilmiştir.

Anahtar Kelimeler: Mikroşerit Yama Anten Dizisi, Paralel Bağlı Seri Besleme Bağlantısı, Seri Bağlaşık Besleme Yapısı, K Bant Anten Uygulamaları

To my family

ACKNOWLEDGEMENTS

I would like to thank my supervisor Prof. Dr. Özlem Aydın Çivi, also Assoc. Prof. Dr. Lale Alatan and Prof. Dr. Sencer Koç, for their guidance and support.

I would like to thank also my friends Orhun Tevfik Altuntaş, İrem Çelebi, Merve Uslu, Fatmanur Tunç, Sinem Doğan, Ertuğrul Eryiğit, Muzaffer Gökçe, Serkan Karadağ and Nazmi Çelebi, for their priceless friendship and support through my thesis work.

Lastly, I would like to express my gratitude to my dearest family, for their encouragement, trust and patience.

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INTRODUCTION

Together with the improving technology, automotive engineering is improving as in all engineering areas. In parallel with these developments, maximum speeds that can be reached by vehicles increase also day by day. Irresponsible usage of high-speed vehicles puts human life in danger. To prevent this danger, the speeds of vehicles need to be monitored and both drivers and police officers should be informed. Traffic radars are used to measure the speed of approaching vehicles. Most of them display all measured speeds, some only display speeds above a preset limit to alert the drivers or traffic police. The full system, which has been used to measure the speed, consists of electronic units, such as digital signal processor and array antenna [1]. Antenna array continuously transmits the electromagnetic waves, and when the vehicle comes across it, the waves are reflected back towards the antenna such that system measures the speed of vehicle [1].

It is important for radar antennas to be small and high-performance in terms of applicability. Microstrip patch antenna arrays are widely used in traffic radar applications since they are electrically thin, lightweight, low cost, inexpensive to manufacture and conformable to planar and non-planar surfaces [2]. Microstrip patch antenna arrays consist of metallic patches on grounded substrates. The patches can take many different shapes such as rectangular and circular [3].

Microstrip patches have various types of feeding techniques. Microstrip line feeds, probe feeds and aperture coupled feeds are the most common structures:

1. Microstrip line feed structure is shown in Figure 1.1. Microstrip feed line is

connected directly to the patch such that feed lines and elements are on the same substrate leading to planar structures [4].

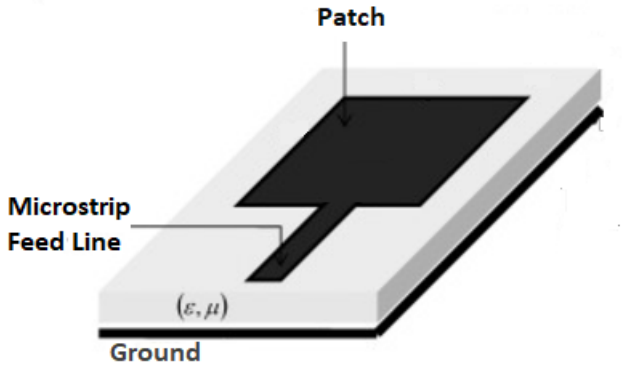

Figure 1.1: Microstrip line fed patch

2. Probe feeds consist of coaxial lines whose centre conductor is attached to the patch while the outer conductor is attached to the back side of the printed circuit board. In this technique, unwanted radiation caused by feeding lines is minimized. Figure 1.2 shows a coaxial fed patch.

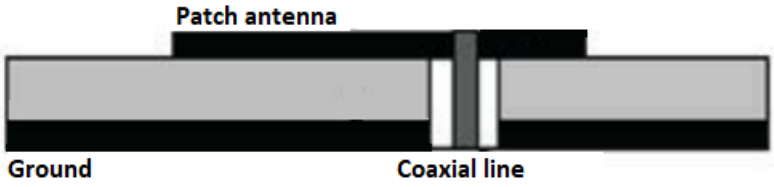

Figure 1.2: Coaxial fed patch

3. Aperture coupled feeds contain two substrates separated by a ground plane as shown in Figure 1.3. On the bottom side of the lower substrate there is a microstrip feed line whose energy is coupled to the patch through a slot on the ground plane separating the two substrates. The ground plane between the substrates also isolates the feed from the radiating element and minimizes interference of spurious radiation for pattern formation and polarization purity [3].

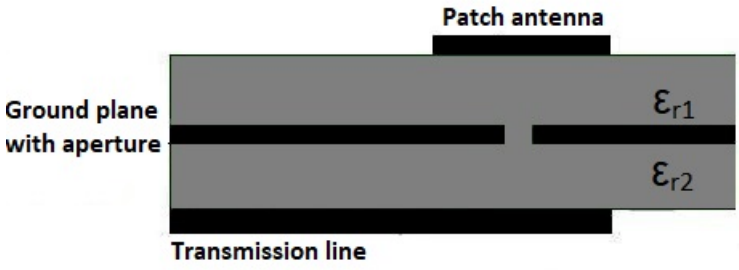

Figure 1.3: Aperture coupled patch

Microstrip patch antenna arrays on the other hand, are commonly designed with corporate feed networks and series feed networks.

Corporate feed networks, shown in Figure 1.4, are the most preferred structure used in microstrip patch antenna arrays. Each array element has its own feeding line, which are connected to others via two way combiners [5]. Since the design of two way combiner is not very complex, corporate networks are very popular; however, they occupy very large space, long length of used lines cause large losses, and discontinuity between line corners causes large mutual coupling effects that distort the radiation patterns.

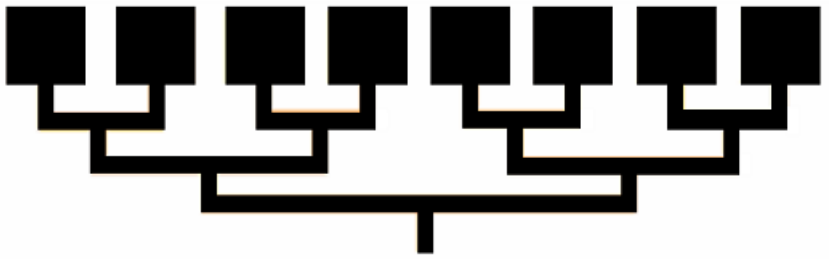

Figure 1.4: Corporate feed network

Series feed networks are another type of structure used in microstrip patch antenna arrays. Antenna patches are serially fed from single transmission line in this type of structures. This feeding architecture provides minimization of feed line lengths which is a very important criteria for antenna efficiency [6]. Narrower bandwidth characteristics are indicated with the series fed arrays [7, 8].

There are two common usage of series feed structures. One of them is shunt connected series feed, namely out of line feed, shown in Figure 1.5 and the other one is in line feed shown in Figure 1.6.

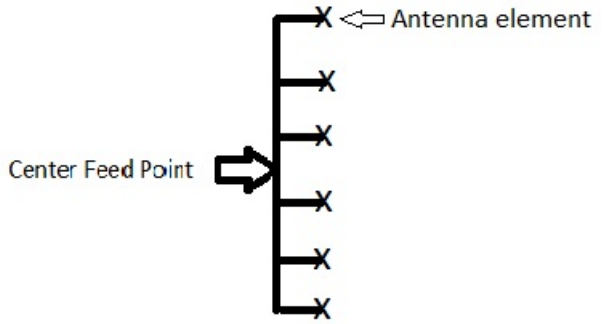

Figure 1.5: Shunt connected series feed network

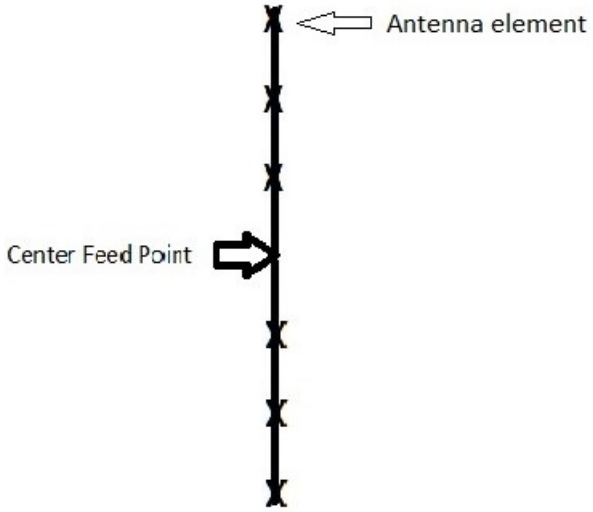

Figure 1.6: In line series feed network

In Figure 1.5, an example of shunt connected series feed network is given. Several feeding lines protrude from the common feed line, and antenna element is placed at the end of each feeding line [5]. Elements are aligned side by side and this configuration looks like corporate feed networks.

In Figure 1.6, an example of in line series feed network is given. This type of networks consist of main feeding line, and elements are directly placed on this line consecu-

tively. Each element connects to the other one in different ways. There can be either coupled connections or direct connections as shown in Figure 1.7. Since optimization of coupling region and size of elements are not controlled easily, coupled in line series networks are not very common. However, these networks give flexibility to the designers for the way for amplitude tapering by using all the parameters[9]. Directly connected in line series feed networks on the other hand, are less flexible for the designers. Dimensions of elements and included transmission lines between elements are used for amplitude tapering [10]. In brief, both architectures can be designed with identical patch elements and different connection lines or identical transmission lines and elements with different dimensions; however, in line coupled architectures have extra design parameters, which are the coupling region parameters.

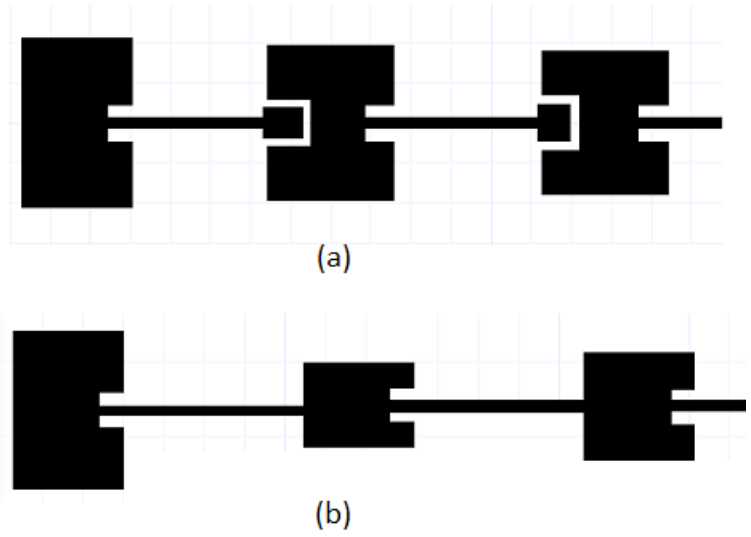

Figure 1.7: In line coupled (a) and direct connected (b) series fed arrays

In traffic radars there is small space for array implementation. Since series feed structures occupy the smallest space among many feeding networks, two microstrip patch antenna arrays with series feed structure are designed in this study. In these arrays, center frequency and bandwidth are chosen as 24.125 GHz and 250 MHz. One of the designed array has shunt connected series feed network with identical elements and different transmission lines and the other one has in line series feed network with identical transmission lines and different patch elements as shown in Figure 1.7(a).

In Chapter 2, design steps of shunt connected series fed microstrip patch antenna array are given, and specific array with preset requirements are explained. Measurement results of the produced antenna are presented and compared with the simulation results.

In Chapter 3, design steps of inline coupled microstrip patch antenna and in line coupled series fed microstrip patch antenna array are given. Parametric studies are presented for the design and analysis of single patch antenna. Specific array with preset requirements is explained, and simulation results are given.

Chapter 4 gives conclusion and anticipated future work.

CHAPTER 2

SHUNT CONNECTED SERIES FED MICROSTRIP PATCH ANTENNA ARRAY

2.1 General Information

Microstrip patch antenna arrays can be designed with wide variety of feeding networks. Shunt connected series feed structure is one of the most common structures used in traffic monitoring applications. One common feed line between elements gives extensions to the feed points of those elements. Generally, all the elements are chosen identical, and power divider partitions between the elements shape the radiation pattern. A sample schematic design of shunt connected series fed array is shown in Figure 2.1.

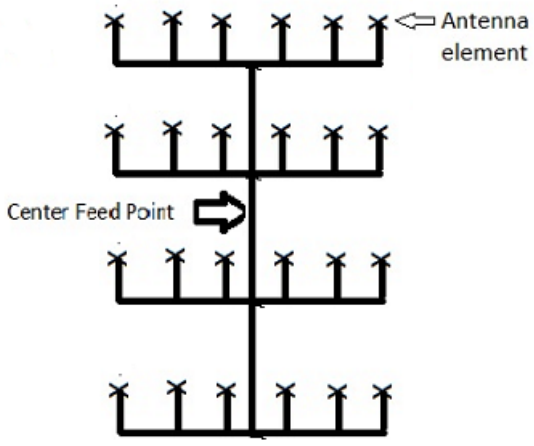

Figure 2.1: Array with shunt connected series feed network

The design steps of array are designated according to the requirements of project. Figure 2.2 illustrates the steps of design process.

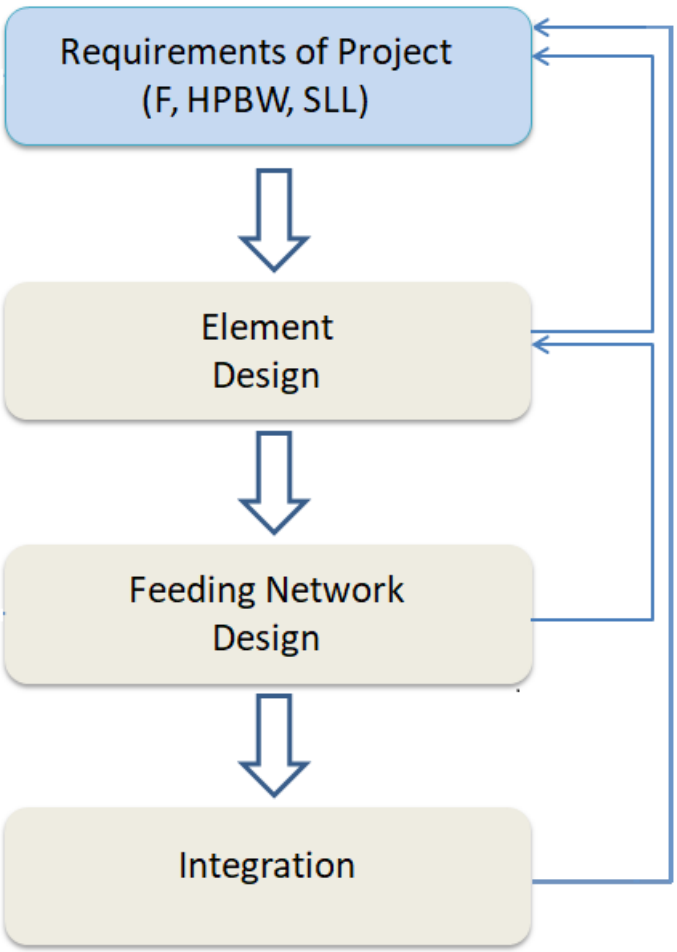

Figure 2.2: Design process

The first step for the design is to determine the dimension of the array. Beamwidth of the array pattern is strictly related with the size of the array. The size of the array is defined by the number of elements and the space between them. Basically, as array dimension gets larger, the beamwidth decreases, which means narrower main beam and an increase in directivity. General expression for the half power beamwidth (HPBW) in radian is given in Formula 2.1, where λ is the free space wavelength at operating frequency, N is the number of elements, and d is the space between patches. In order to provide in-phase feeding, identical inter-element spacings are chosen.

$$HPBW = \frac{\lambda}{(N-1)d} \tag{2.1}$$

The second step is to design elements. Inset fed microstrip patch antennas are widely used for the shunt connected series fed arrays. The geometry of inset-fed microstrip patch antenna is shown in Figure 2.3.

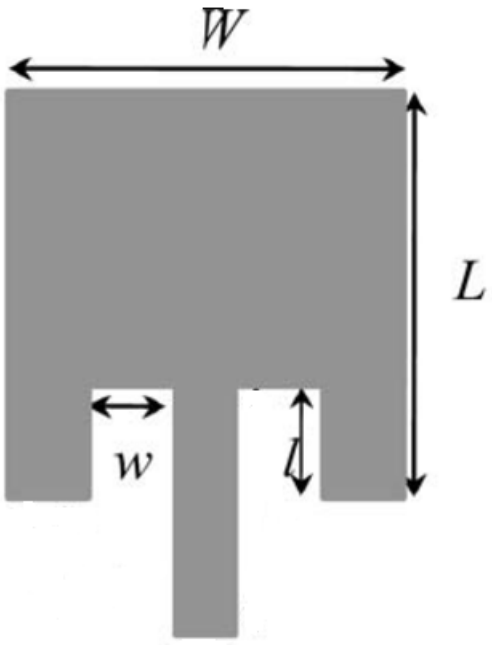

Figure 2.3: Inset-fed microstrip patch antenna element

The impedance of the array element is a function of the inset feed point. As the inset feed point moves from the edge toward the centre of the patch, that is, as l increases, input impedance decreases monotonically and reaches zero at the centre [3].

The third step is to design feeding network. Feeding networks generally comprises of power divider structures.

Antenna arrays can be designed to control their radiation characteristics by properly selecting the amplitude distribution between the elements. Typically, the level of the side lobes can be controlled by tapering the distribution across the array; the more tapering from the center of the array toward the edges, the lower the side lobe level [3]. In practice, the amplitude tapering is provided with the power divider structures. As expressed before, structure consists of a common feed line used for the entire array and each element extends from this feed line [5]. In the network, feeding line of each individual element has different power coefficient values that are selected according to the side lobe level requirements of the design. Impedances of power division points are calculated from power division coefficients. All the elements and all the power division points, namely extensions, are impedance matched [11]. Figure 2.4 indicates a sample power divider structure. Impedances of power division points,

$Z_{n+1,n}$, $Z_{n+2,n+1}$, $Z_{n+3,n+2}$, are calculated from the given formula in 2.2, where P_n, P_{n+1}, P_{n+2}, P_{n+3} are power coefficients of elements and the $Z_{element}$ is the input impedance of the element that is identical with the impedance of the feeding lines.

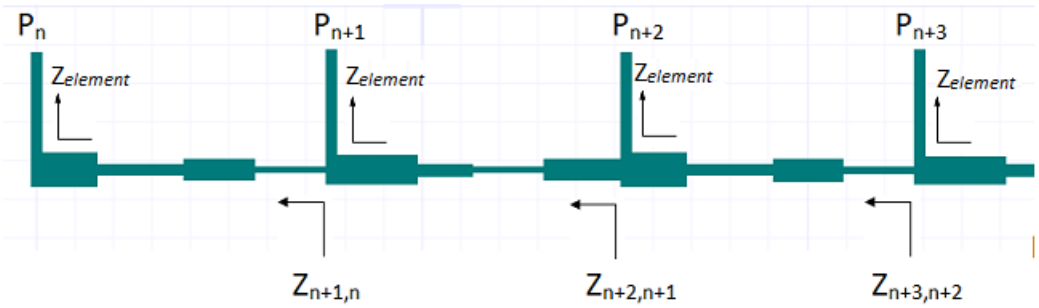

Figure 2.4: Sample power divider structure

$$\frac{P_{n+1}}{P_n} = \frac{Z_{n+1,n}}{Z_{element}}, \frac{P_{n+2}}{P_{n+1}+P_n} = \frac{Z_{n+2,n+1}}{Z_{element}}, \frac{P_{n+3}}{P_{n+2}+P_{n+1}+P_n} = \frac{Z_{n+3,n+2}}{Z_{element}} \quad (2.2)$$

The quarter wave impedance transformation technique is used for impedance matching between power division points. This technique includes a simple impedance transformation in order to minimize the reflected energy when a transmission line is connected to a load, Z_L. In this technique, a transmission line with different characteristic impedance and with a length of one-quarter of the guided-wavelength is used to match a line to a load. Figure 2.5 indicates the application of this technique. Matching Z_{in} to Z_L is provided by Z_0 with the given formula in 2.3.

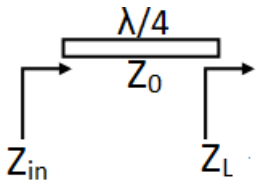

Figure 2.5: Quarter wave impedance matching with Z_0

$$Z_0 = \sqrt{Z_{in}Z_L} \quad (2.3)$$

In some cases, due to manufacturing restrictions, two stage quarter wave impedance transformation is needed. Representation of transformation is shown in Figure 2.6, and the formula is given in 2.4.

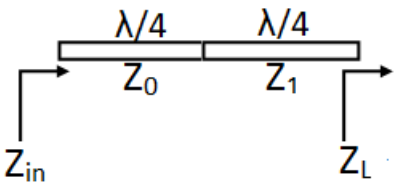

Figure 2.6: Two stage quarter wave impedance matching with Z_0 and Z_1

$$\frac{Z_0}{Z_1} = \sqrt{\frac{Z_{in}}{Z_L}} \tag{2.4}$$

Calculated impedances of power division points are implemented on power divider structure using the given formula in 2.3 and 2.4. After the implementation, the designed power divider structure is integrated with the elements as the final step.

In the following sections, design requirements and design methodology of specific array are explained. Measurement and simulation results are given comparatively.

2.2 Design of the Array

Microstrip patch antenna array with shunt connected series feed structure operating at 24.125 GHz is designed, manufactured and tested. Design is completed in Ansys HFSS 3D Layout Simulation Programme. Design requirements are given in Table 2.1.

Table 2.1: Design requirements

Frequency	24 - 24.25 GHz
Bandwidth	250 MHz
E-Plane HPBW	7 degrees
H-Plane HPBW	7 degrees
Side Lobe Level	-15 dB

The design steps designated before are implemented according to the design requirements of this study. 24-24.25 GHz band is assigned for industrial, scientific and medical (ISM) applications [12]. Most of the European countries use this band for traffic radar applications. 7 degree beamwidth requirement emerged due to the specification of radar product which is used for single lane monitoring systems.

First, the size of the array is determined. For the in-phase feeding, inter-element spacing is chosen as λ_g which equals to 0.56λ at operating frequency. 7 degree half power beamwidth ($\approx$ 0.13 radians) requirement is provided with 14 elements according to the given formula in 2.1, as calculated in Equation 2.5. Since HPBW requirements for both E and H-planes are same; array has 14x14 elements.

$$0.13 = \frac{\lambda}{(N-1)d} = \frac{\lambda}{(N-1)0.56\lambda} \tag{2.5}$$

Second, identical elements are designed. Inset fed microstrip patch antenna as shown in Figure 2.3 is used. The element is designed to have 100 Ω input impedance. Input impedances smaller than 100 Ω are not preferred; because when input impedance of element decreases, characteristic impedances of transmission line used in the power divider structure decrease accordingly; that is, width of lines increases. Thick feeding lines cause undesired mutual coupling between elements and lines. On the other hand, input impedances larger than 100 Ω are not preferred either; because in this case, the width of lines gets smaller, which causes manufacturing difficulties. 20 mils thickness RO4350 substrate having dielectric constant ε=3.66 and loss tangent tanδ=0.0037 is used in both simulation and fabrication. Dimensions of the designed patch are given in Table 2.2.

Table 2.2: Dimensions of the element

Width (W)	4.25 mm
Length (L)	2.97 mm
Inset Width (w)	0.3 mm
Inset Length (l)	0.6 mm

The third step is design of power divider structures. Same amplitude tapering is used for both horizontal and vertical power dividers. Power coefficients are determined from the in-house software in an attempt to obtain -20 dB side lobe level (SLL). The coefficients are given in Table 2.3.

Table 2.3: Power coefficients of elements

Elements	Power Coefficients
Element 1	P_1= 0.16
Element 2	P_2= 0.25
Element 3	P_3= 0.4225
Element 4	P_4= 0.5625
Element 5	P_5= 0.81
Element 6	P_6= 1
Element 7	P_7= 1
Element 8	P_8= 1
Element 9	P_9= 1
Element 10	P_{10}= 0.81
Element 11	P_{11}= 0.5625
Element 12	P_{12}= 0.4225
Element 13	P_{13}= 0.25
Element 14	P_{14}= 0.16

As realized from Table 2.3, power divider structure is bilaterally symmetric around the feed point. Only a half of the structure is designed, then it is symmetrized and copied to the other side of the center feeding point. In this process, first, a row of the array is designed. Figure 2.7 shows power coefficients P_1, P_2, P_3, P_4, P_5, P_6, P_7 and impedances of power division points Z_{21}, Z_{32}, Z_{43}, Z_{54}, Z_{65}, Z_{76}.

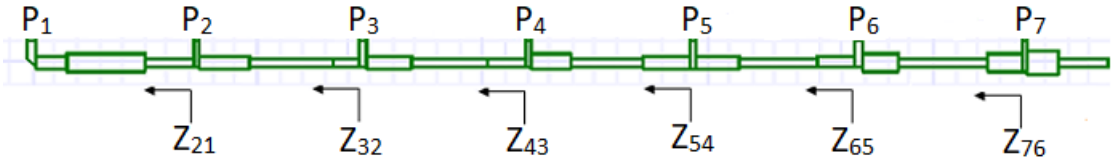

Figure 2.7: Half row of power divider structure

Impedances of power division points are calculated using the formula given in 2.2. Sample calculations for Z_{21} and Z_{32} are given in Equation 2.6.

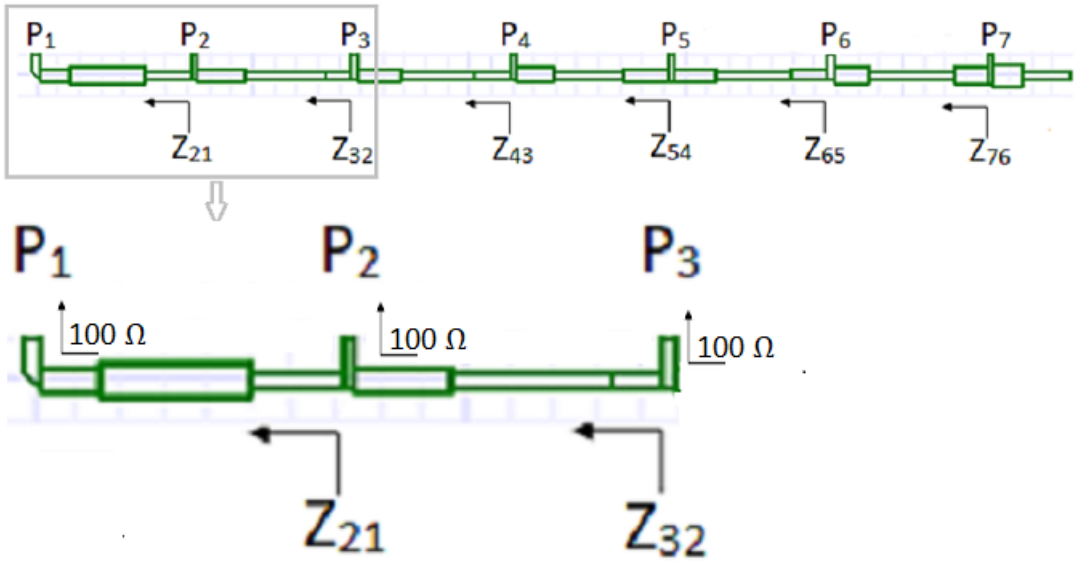

Figure 2.8: Zoomed power division points

$$\frac{P_2}{P_1} = \frac{0.25}{0.16} = \frac{Z_{21}}{100} \qquad \frac{P_3}{P_2 + P_1} = \frac{0.4225}{0.25 + 0.16} = \frac{Z_{32}}{100} \tag{2.6}$$

On the basis of the given formula, all the impedances are calculated and listed in Table 2.4.

Table 2.4: Power coefficients and impedances of power division points

Power Coefficients	Impedances of Power Division Points
P_1= 0.16, P_2= 0.25	Z_{21}= 156.25 Ω
P_3= 0.4225	Z_{32}= 103.2 Ω
P_4= 0.5625	Z_{43}= 67.54 Ω
P_5= 0.81	Z_{54}= 57.97 Ω
P_6= 1	Z_{65}= 45.35 Ω
P_7= 1	Z_{76}= 30.25 Ω

Calculated power division impedances are implemented with quarter wave impedance transformation formulas given in 2.3 and in 2.4. As an example, Figure 2.9 may be considered. In this power divider partition 100 Ω is matched to the Z_{21}, which is 156.25 Ω, by using two stage quarter wave transformation. From the formula in 2.4, two impedances used between power division points are calculated as follows (in

Equation 2.7):

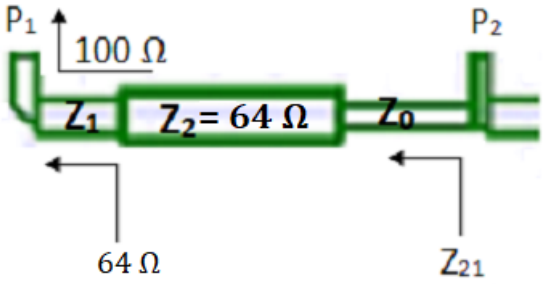

Figure 2.9: Power divider partition

$$\frac{Z_1}{Z_0} = \sqrt{\frac{100}{156.25}} = \frac{80}{100} \tag{2.7}$$

As expressed before, each element is placed λ_g apart from each other. In the example of power divider partition (Figure 2.9), transmission lines used for the quarter wave impedance transformation (Z_0 and Z_1) occupy totally $\lambda_g/2$ length. The rest of $\lambda_g/2$ length between two feeding lines is covered by the resultant transmission line of the first stage impedance transformation. To clarify, 100 Ω is down converted to 64 Ω (by using Z_1, according to the given formula in 2.3) at the first stage of impedance transformation; hence, 64 Ω transmission line is placed in the rest of $\lambda_g/2$ length. This procedure is applied for all power divider partitions between the elements. Figure 2.10 shows half row of the power divider structure with transmission lines, namely Z_0, Z_1, Z_2, Z_3, Z_4, Z_5, Z_6, Z_7, Z_8, Z_9, Z_{10}, Z_{11}, Z_{12}, Z_{13}. Calculated impedance values of those lines are given in Table 2.5.

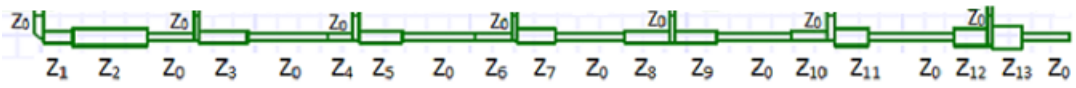

Figure 2.10: Half row of power divider structure

Table 2.5: The impedance values of transmission lines

Z_0=100 Ω	Z_1=80 Ω
Z_2=64 Ω	Z_3=78 Ω
Z_4=101.5 Ω	Z_5=70 Ω
Z_6=82.18 Ω	Z_7=63.5 Ω
Z_8=76.14 Ω	Z_9=60.6Ω
Z_{10}=67.34 Ω	Z_{11}=55.84 Ω
Z_{12}=55 Ω	Z_{13}=48 Ω

In brief, amplitude distribution is provided with impedances of power division points which are calculated from power coefficients, and phase distribution is provided with the distance between patches λ_g. These two form the array structure.

During the design of each power divider partititon, differences of s_{21} scattering parameters of adjacent feeding lines are used to check whether designed structure meets the requirements or not. As mentioned before, shunt connected series feed structures contain one main feeding line, and several feeding lines for the elements. s_{21} of each single feeding line is calculated with $10\log\frac{P_i}{P_{in}}$ where P_i is the power coefficient of i_{th} element and P_{in} is the sum of power coefficients of feeding lines, that is, power coefficient of the main feeding line. Calculated s_{21} values are listed and differences of adjacent single feeding lines are controlled from Ansys HFSS 3D Layout Simulation Programme. Table 2.6 gives the calculated differences and the simulated ones.

Table 2.6: s_{21} differences of adjacent feeding lines

Feeding Line	Calculated s_{21} Differences	Simulated s_{21} Differences (24.125 GHz)
2 and 1	$10\log\frac{0.16}{4.205} - 10\log\frac{0.25}{4.205}$ = -1.94 dB	-1.950 dB
3 and 2	$10\log\frac{0.25}{4.205} - 10\log\frac{0.4225}{4.205}$ = -2.28 dB	-2.253 dB
4 and 3	$10\log\frac{0.4225}{4.205} - 10\log\frac{0.5625}{4.205}$ = -1.24 dB	-1.196 dB
5 and 4	$10\log\frac{0.5625}{4.205} - 10\log\frac{0.81}{4.205}$ = -1.59 dB	-1.523 dB
6 and 5	$10\log\frac{0.81}{4.205} - 10\log\frac{1}{4.205}$ = -0.91 dB	-0.836 dB
7 and 6	$10\log\frac{1}{4.205} - 10\log\frac{1}{4.205}$ = 0 dB	-0.199 dB

In addition to the amplitudes, the phases of s_{21} parameters of each power divider partition are considered during the design process. Aimed broadside pattern is obtained with the minimum phase difference between input ports of elements. Difference between phases of s_{21} of adjacent feeding ports is at most 2.5 degrees in the structure.

Designed half is copied to the other side of feeding point in order to complete a row of the power divider structure given in Figure 2.11. Amplitude of s_{n8} of each feeding line is obtained by full wave simulations, where *n* is the port number of feeding line. Figure 2.12 indicates simulated s_{n8} values in the frequency band. Comparison of calculated and simulated ones at the 24.125 GHz are given in Table 2.7. It is observed that required tapering is obtained by this design.

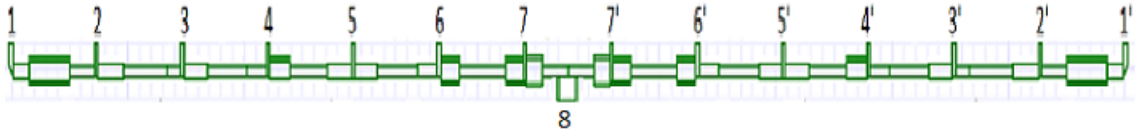

Figure 2.11: Power divider

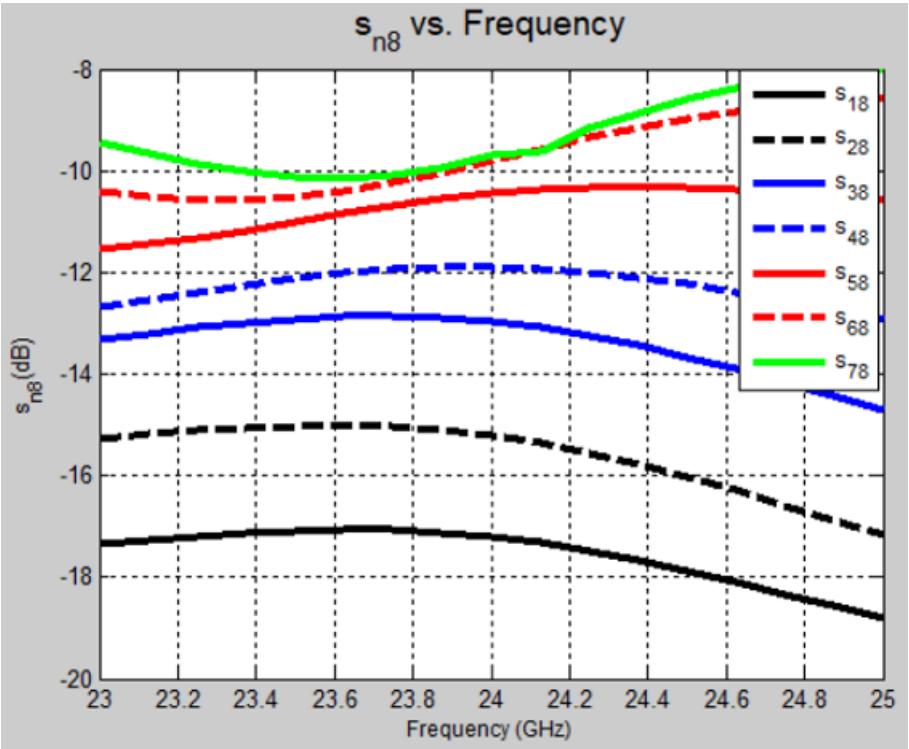

Figure 2.12: s_{n8} values of power divider

Table 2.7: s_{n8} of feeding lines

Calculated s_{n8}	Simulated s_{n8} (24.125 GHz)
$s_{18} = 10 \log \frac{0.16}{8.410}$ = -17.20 dB	-17.32 dB
$s_{28} = 10 \log \frac{0.25}{8.410}$ = -15.26 dB	-15.36 dB
$s_{38} = 10 \log \frac{0.4225}{8.410}$ = -12.98 dB	-13.10 dB
$s_{48} = 10 \log \frac{0.5625}{8.410}$ = -11.74 dB	-11.89 dB
$s_{58} = 10 \log \frac{0.81}{8.410}$ = -10.15 dB	-10.45 dB
$s_{68} = 10 \log \frac{1}{8.410}$ = -9.24 dB	-9.80 dB
$s_{78} = 10 \log \frac{1}{8.410}$ = -9.24 dB	-9.71 dB

As a final step for the row of the array design, power divider structure is integrated with the antenna elements. It is shown in Figure 2.13. A row of the array is fabricated and measured.

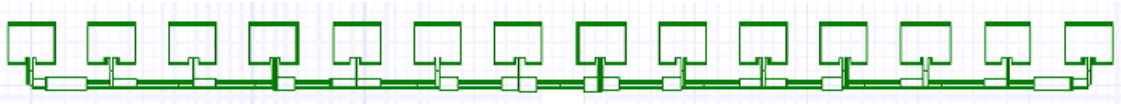

Figure 2.13: One row of array

Array has 14x14 elements, that is, the structure shown in Figure 2.13 is repeated 13 times in rows. Those rows are connected to each other with vertical power divider structure whose power coefficients that provide the amplitude tapering are the same as the ones used for the horizontal structure. Figure 2.14 shows half of this vertical power divider structure along with the impedances of power division points Z_{32}, Z_{43}, Z_{54}, Z_{65}, Z_{76} and used transmission lines.

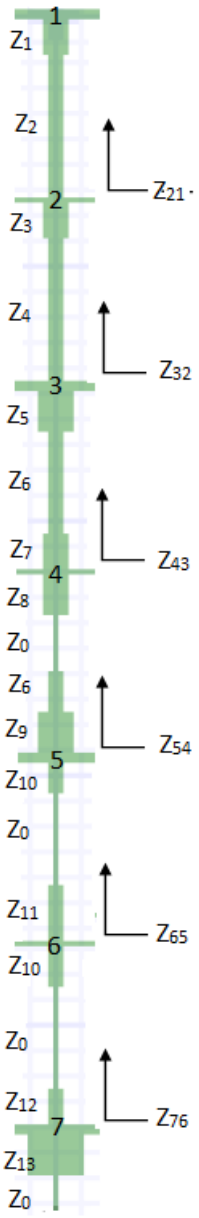

Figure 2.14: Half column of power divider structure

The formula given in Equation 2.2 is used for the calculation of the impedances of power division points. Right and left sides of rows are combined. They give 50 Ω impedance for the vertical power division points; hence, 50 Ω is used at the denominator of formula given in 2.2. Sample calculations for Z_{21} and Z_{32} are given in Equation 2.8.

$$\frac{P_2}{P_1} = \frac{0.25}{0.16} = \frac{Z_{21}}{50} \qquad \frac{P_3}{P_2 + P_1} = \frac{0.4225}{0.25 + 0.16} = \frac{Z_{32}}{50} \tag{2.8}$$

Previously, the design steps of power divider structure are explained (design of horizontal power divider structure). The same steps are applied in the rest of the vertical power divider structure design as follows.

First, impedances of power division points are calculated (as illustrated in Equation 2.8), and they are given in Table 2.8.

Table 2.8: Impedances of power division points

Power Coefficients	Impedances of Power Division Points
P_1=0.16, P_2=0.25	Z_{21}=78 Ω
P_3=0.4225	Z_{32}=52 Ω
P_4=0.5625	Z_{43}=34 Ω
P_5=0.81	Z_{54}=29 Ω
P_6=1	Z_{65}=23 Ω
P_7=1	Z_{76}=15 Ω

Second, calculated impedances are matched to the half sides of the rows using quarter wave impedance transformation. Power divider column has small impedance values at the power division points. Hence, for some parts, more than two stage quarter wave impedance transformation is used. Figure 2.14 shows half column of the power divider structure with transmission lines, namely Z_0, Z_1, Z_2, Z_3, Z_4, Z_5, Z_6, Z_7, Z_8, Z_9, Z_{10}, Z_{11}, Z_{12}, Z_{13}. Calculated impedance values of those lines are given in Table 2.9.

Table 2.9: Impedance values of transmission lines

Z_0=100 Ω	Z_1=62.5 Ω
Z_2=78 Ω	Z_3=48 Ω
Z_4=62.5 Ω	Z_5=43 Ω
Z_6=75 Ω	Z_7=50.5 Ω
Z_8=51.64 Ω	Z_9=47Ω
Z_{10}=56 Ω	Z_{11}=59 Ω
Z_{12}=55 Ω	Z_{13}=34 Ω

Third, differences between the amplitudes of s_{21} parameters of adjacent feeding lines are compared with the calculations. Table 2.10 shows the calculated differences and simulated differences of s_{21} at the 24.125 GHz.

Table 2.10: s_{21} differences of adjacent feeding lines

Calculated s_{21} Differences	Simulated s_{21} Differences (24.125 GHz)
$10\log\frac{0.16}{4.205} - 10\log\frac{0.25}{4.205}$ = -1.94 dB	-1.890 dB
$10\log\frac{0.25}{4.205} - 10\log\frac{0.4225}{4.205}$ = -2.28 dB	-2.199 dB
$10\log\frac{0.4225}{4.205} - 10\log\frac{0.5625}{4.205}$ = -1.24 dB	-1.212 dB
$10\log\frac{0.5625}{4.205} - 10\log\frac{0.81}{4.205}$ = -1.59 dB	-1.590 dB
$10\log\frac{0.81}{4.205} - 10\log\frac{1}{4.205}$ = -0.91 dB	-0.898 dB

As a final step, designed half is copied to the other side of the feeding point in order to complete a column of power divider structure. Amplitude and phase of s_{n8} of each feeding line are compared with calculations, and vertical power divider structure shows similar performance as horizontal one. Calculated and simulated values are close to each other which indicates that proposed tapering is obtained.

A column of power divider is combined with 14 rows of array and manufactured. Figure 2.15 shows manufactured array.

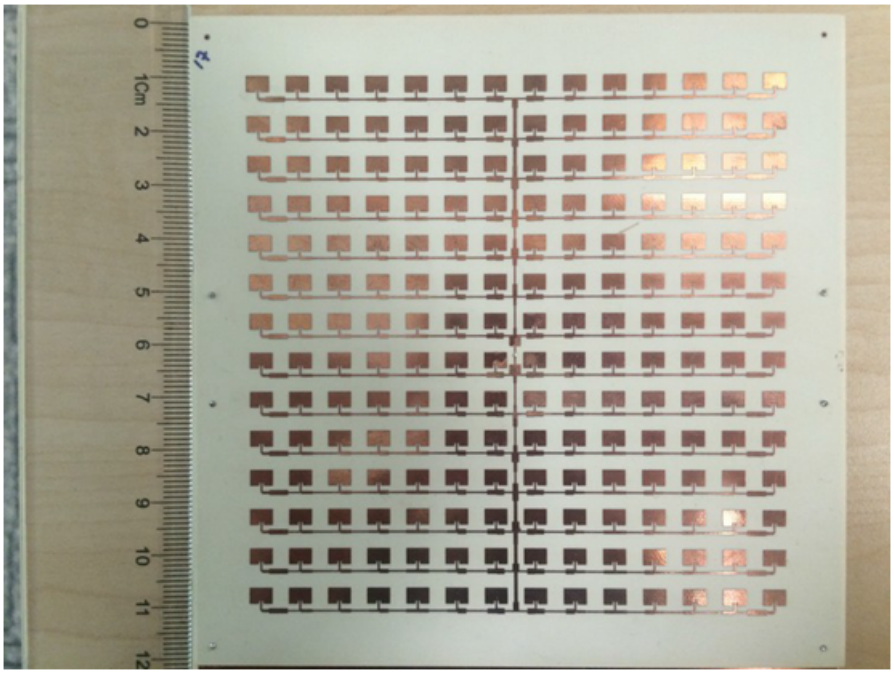

Figure 2.15: Fabricated array

Designed shunt connected series fed array will be used at the front end of a printed circuit board of the traffic speed radar. Electronic units at the board will provide

the centre feeding of array from back layer. However, there is a necessity about usage of SMPM (sub miniature push on-micro) surface mount connector during tests and measurements. The connector used in the measurements is produced by Cinch Connectivity Solutions. The connector is shown in Figure 2.16.

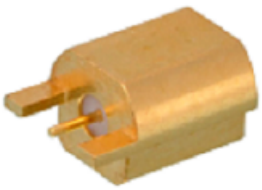

Figure 2.16: Used end launch edge mounted SMPM connector

Transition from coplanar waveguide to microstrip transmission line structure is performed in attempt to use shown connector. In these structures the signal line and two ground planes lie on the same side of the circuit substrate, surface-mount devices can be readily integrated with coplanar wave guide transmission lines [13]. According to mechanical drawing of connector, dimensions of structure are determined. Fabricated transition structure and mounted connector are shown in Figure 2.17.

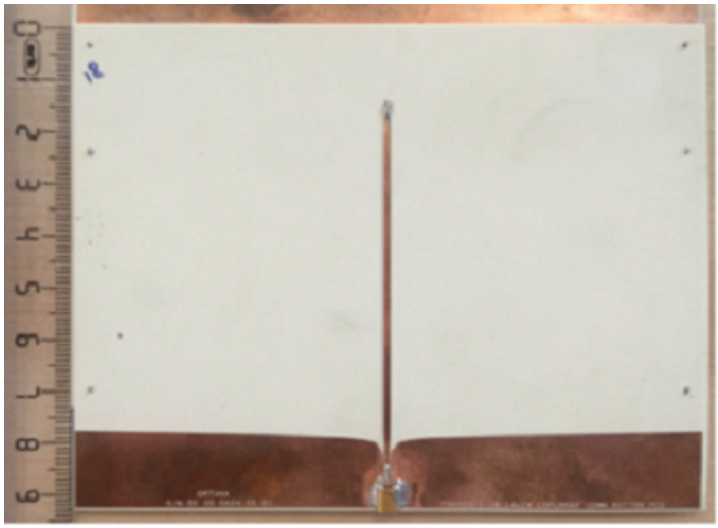

Figure 2.17: Coplanar waveguide to microstrip line transition structure and SMPM connector

Fabricated antenna array and transition structure are soldered at the points marked by red circles shown in Figure 2.18; so their grounded back layers are stacked up.

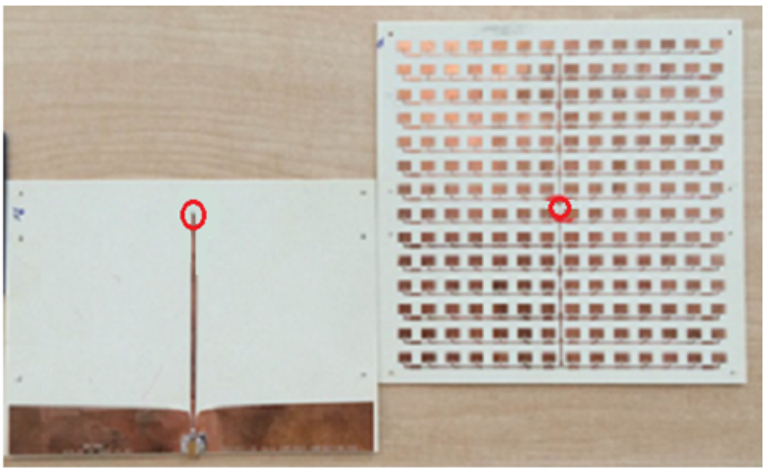

Figure 2.18: Soldering points of two layers

2.3 Measurement Results

Radiation patterns and return loss of fabricated array element, a row of array and 14x14 elements array are measured in METU Electrical and Electronics Engineering Department.

Input return loss (s_{11}) graph of a single element is shown in Figure 2.19. s_{11} is almost -40 dB at the operating frequency. 10 dB bandwidth is almost 1 GHz (23.6-24.6 GHz).

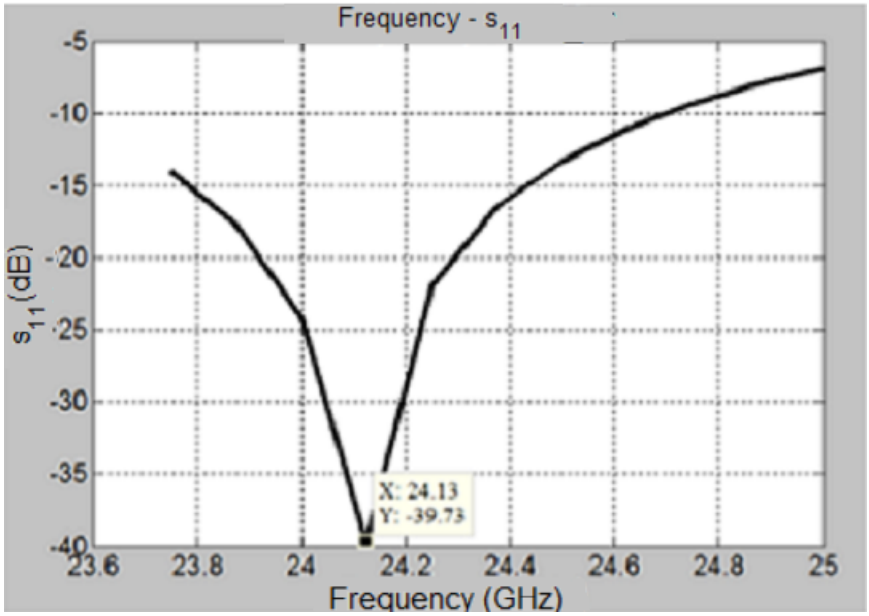

Figure 2.19: s_{11} of a single element

A row of array shown in Figure 2.13 is manufactured and measured. Simulation and measurement results of s_{11} parameters are given in Figure 2.20. In the operating band, reflection characteristics of measurements and simulation are similar and s_{11} values are less than -10 dB.

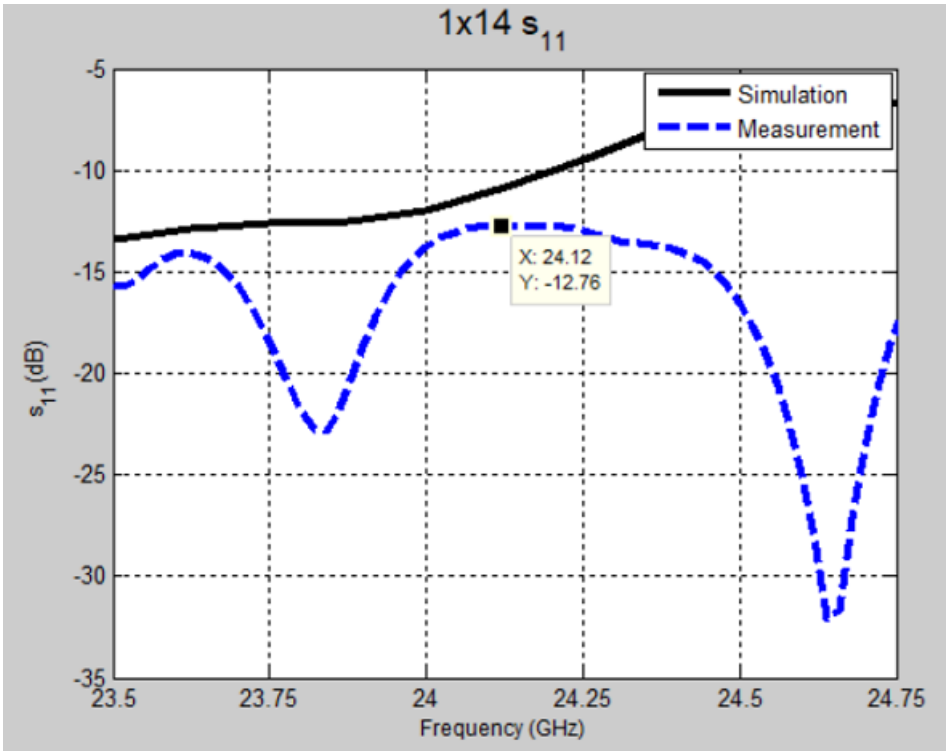

Figure 2.20: Comparison of simulation and measurement results of s_{11} for 1x14 array

Figure 2.21 shows s_{11} graph of 14x14 shunt connected series fed microstrip patch antenna array with transition structure. Measurements give better results than simulation both at the centre frequency and at the operating band. The reason for this difference lies in the fact that soldering is used for the integration of the transition structure during measurements, which provides better results than the via used in the simulation.

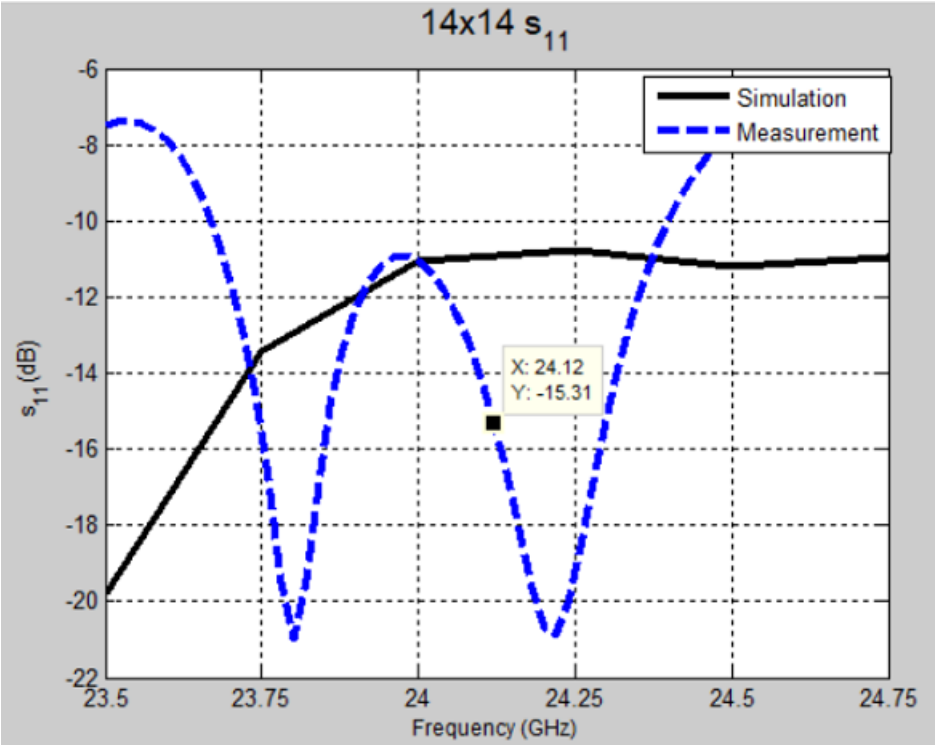

Figure 2.21: Comparison of simulation and measurement results of s_{11} for 14x14 array

Simulation and measurement results of H-plane and E-plane radiation patterns are plotted in the Figure 2.22 and 2.23, respectively. 7 degree beamwidth is satisfied for both E-plane and H-plane.

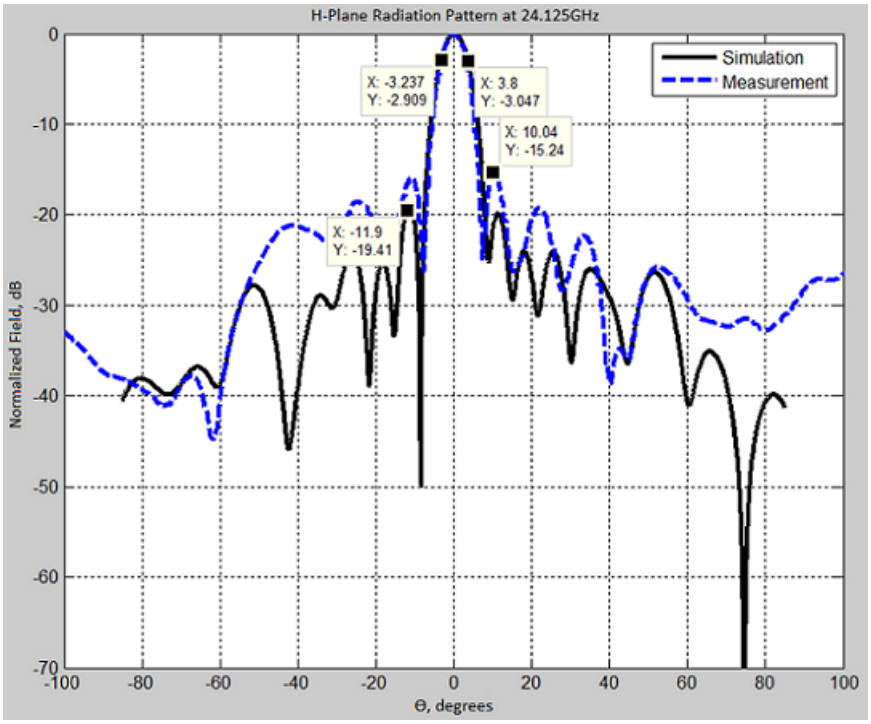

Figure 2.22: Comparison of simulation and measurement of H-plane radiation pattern at 24.125 GHz

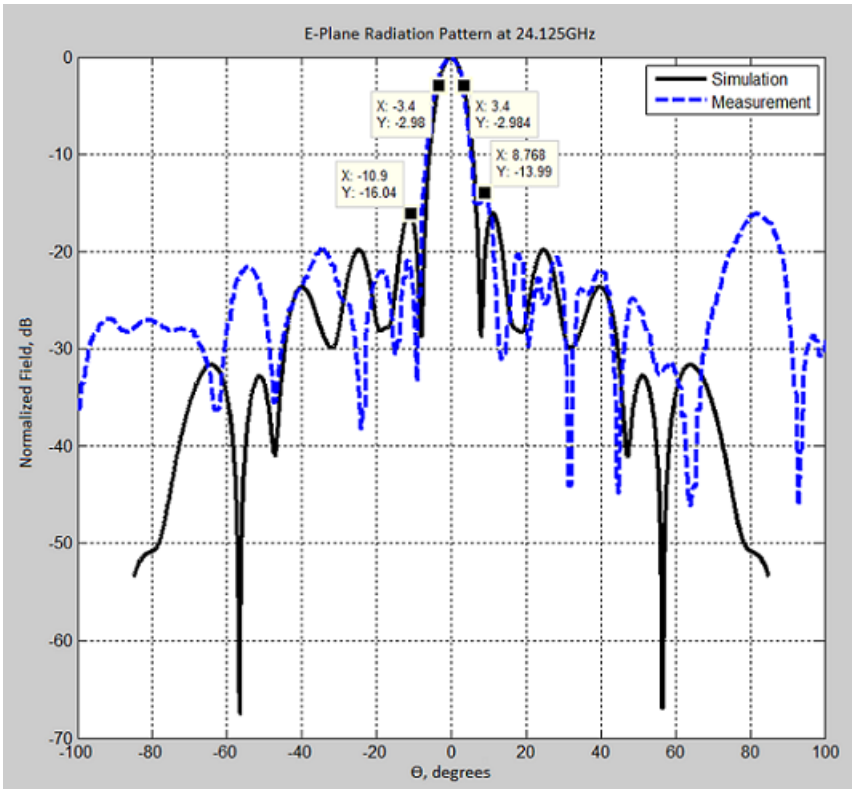

Figure 2.23: Comparison of simulation and measurement results of E-plane radiation pattern at 24.125 GHz

As shown in Figure 2.22, for H-plane, aimed -20 dB side lobe level is achieved in simulation; however in measurements it is observed as approximately -15 dB. The discrepancy in side lobe level is due to the fact that grounded dielectric layer is taken as infinitely large in the simulation while it is finite (12x12 cm) in the manufactured array.

During the design steps, calculations are performed in order to obtain -20 dB side lobe level for E-plane. Yet, during the simulation, it emerges as -16 dB and during the measurement, as -14 dB as shown in Figure 2.23. This discrepancy is due to the extra layer used for connector implementation. Extra layer structure is aligned on E-plane which increases the side lobe level even in simulations; however, this layer structure is not used in the final radar product. Figure 2.24 shows E-plane radiation pattern without extra layer. It is seen that SLL is almost -20 dB.

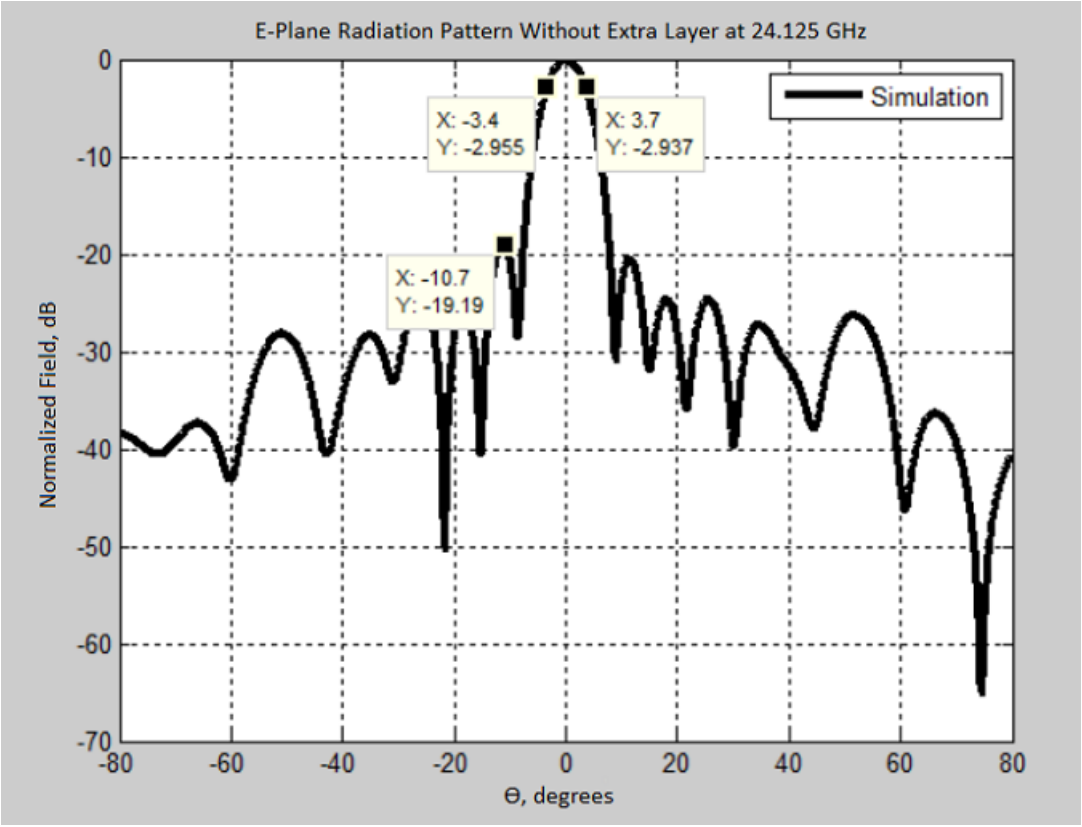

Figure 2.24: Simulation of E-plane radiation pattern without coplanar to microstrip transition structure at 24.125 GHz

14x14 elements microstrip patch antenna array for traffic radar applications is manufactured and measured. It is observed that simulation and measurement results are

very similar. 7 degree HPBW is obtained in both H and E-planes as well as less than -14 dB side lobe levels in the radiation patterns.

CHAPTER 3

IN LINE COUPLED SERIES FED MICROSTRIP PATCH ANTENNA ARRAY

3.1 General Information

The recently proposed approach used for the feeding networks of microstrip patch antenna arrays is in line coupled series feed structure [9]. In this type of structure, specialized patches are consecutively fed by a transmission line and the signal is transmitted through radiating elements. While input line of a patch has direct connection, output transmission line is coupled electromagnetically. Figure 3.1 shows the specialized patch element and Figure 3.2 shows a schematic of array.

Coupling region dimensions of a patch, *cgap*, *cw* and *ch*, mostly adjust the coupled signal level to the adjacent patch. The amplitude and the phase of the coupled signal can be easily controlled by the parameters seen on Figure 3.1 [14]. In other words, amplitude tapering is only ensured with this type of specialized patches in the E-plane. On the other hand, power divider structure similar to ones described in Chapter 2 is used for the amplitude tapering in the H-plane.

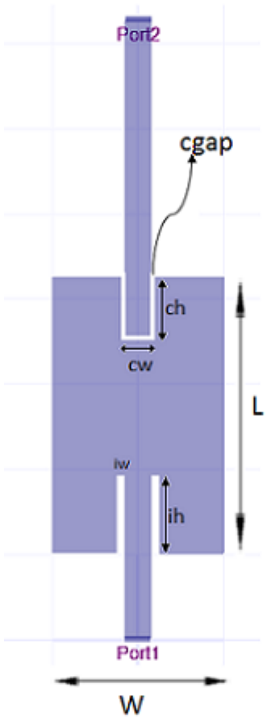

Figure 3.1: In line coupled element

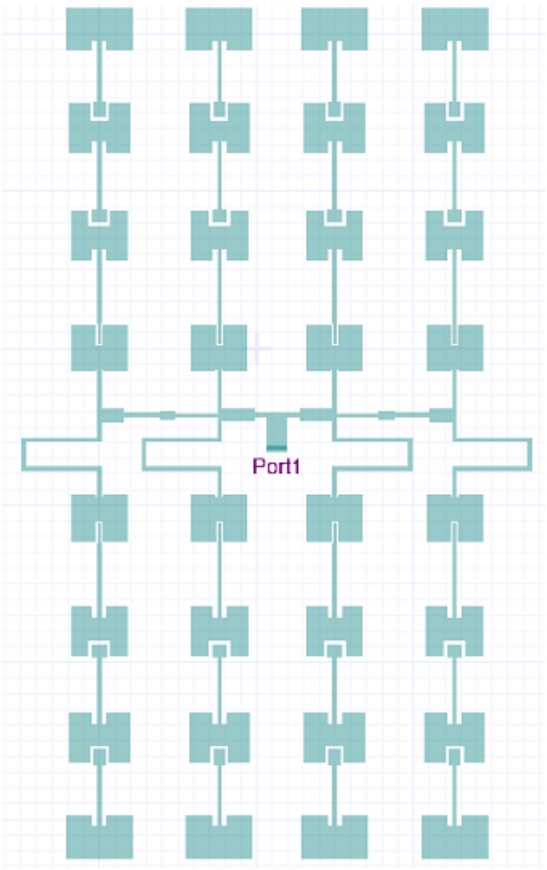

Figure 3.2: Array with in line coupled series feed network

The steps of design process are very similar to those given in Chapter 2. Those steps are designated according to the requirements of a project.

First, the size of the array is determined from $HPBW = \frac{\lambda}{(N-1)d}$ given in Chapter 2, Formula 2.1. The beamwidth of the array pattern is strictly related with the size of array.

Second, specialized patches are designed separately and connected to each other consecutively in the E-plane. Input impedances of the patches are same; as a result, patches are connected to each other with identical transmission lines. Distances between patches are also identical and has the value λ_g for the in-phase feeding. As expressed before, amplitude tapering is provided with the patches in the E-plane. Each patch has different power coefficient value which is selected according to the side lobe level requirement of the design. Transmitted signal from one element to the adjacent one is determined by coupling between input and output signal level. In fact, it is an expression of s_{21} parameter. s_{21} parameters of elements are calculated from the formula given in 3.1 where P_i is the power coefficient of i_{th} element and $P_{in(i)}$ is the power coefficient at the input of that element [15].

$$s_{21}(dB) = 10log(1 - \frac{P_i}{P_{in(i)}}) \tag{3.1}$$

Third, power divider structure is designed. As expressed before, amplitude tapering is provided by power divider structure in the H-plane. Design steps are the same as those given in Chapter 2:

- Power coefficients are determined.
- Impedances of power division points are calculated.
- Power division points are matched to each other using the quarter wave impedance transformation technique.
- Amplitudes and phases of s_{21} of the feeding lines are checked.

The final step is the integration of specialized patches with the power divider structure.

In the following sections, design of an in line coupled inset fed patch antenna is explained by simulations. Design requirements and design methodology of specific array are explained. Simulated input return loss plot and radiation patterns are presented.

3.2 Design of a In Line Coupled Inset Fed Microstrip Patch

In line coupled inset fed patches are radiating elements with specialized geometry. As mentioned in the previous section, transmitted signal from the patch is determined by electromagnetic coupling. The level of coupling from a patch is measured with s_{21} parameter of that patch.

Coupling region dimensions of the patches, *cgap*, *cw* and *ch*, have the largest effect on the s_{21} values of those patches. In order to show how the dimensions of a patch affect the s_{21} and resonant frequency, a sample patch with 100 Ω input impedance is designed at 24.125 GHz in HFSS 3D Layout. The dimensions of the sample patch are given in Table 3.1. s_{21} value of the patch is -1.63 dB and s_{11} value is -22 dB at the center frequency.

Table 3.1: Dimensions of the sample patch

W	2.00 mm
L	3.25 mm
iw	0.10 mm
ih	0.92 mm
cw	0.40 mm
ch	0.75 mm
cgap	0.05 mm

In HFSS 3D Layout, parametric analyses are applied in order to show s_{21} variance with respect to the different dimensions of the patch. In the parametric analyses, all the dimensions, except for the analysed one, are kept constant. Figures 3.3, 3.4, 3.5 and 3.6 show s_{21} variance with respect to *cgap*, *cw*, *ch* and *W*, respectively. s_{21} is inversely proportional to *cgap*, *cw* and *W* while it is proportional to *ch*.

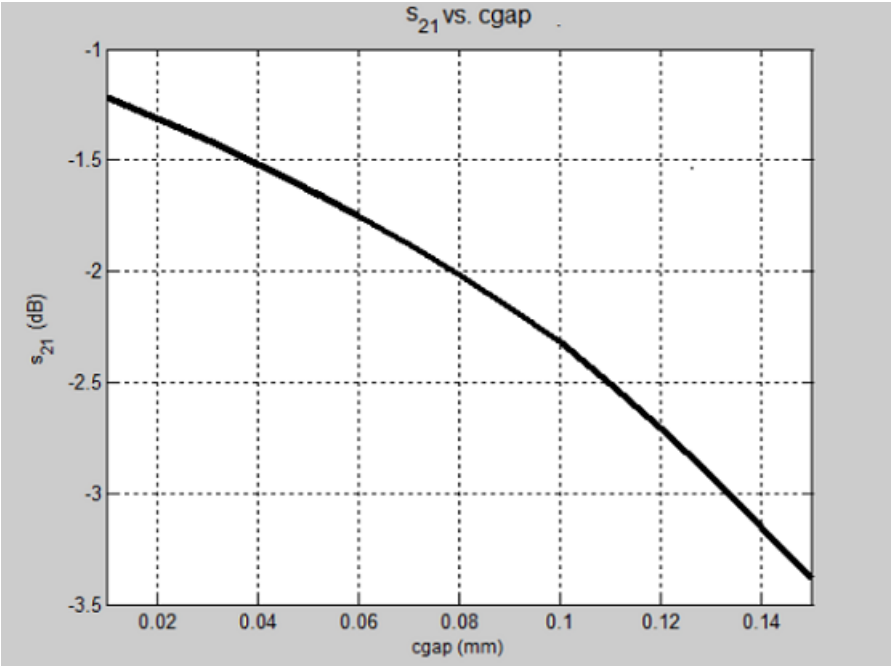

Figure 3.3: s_{21} vs. *cgap*

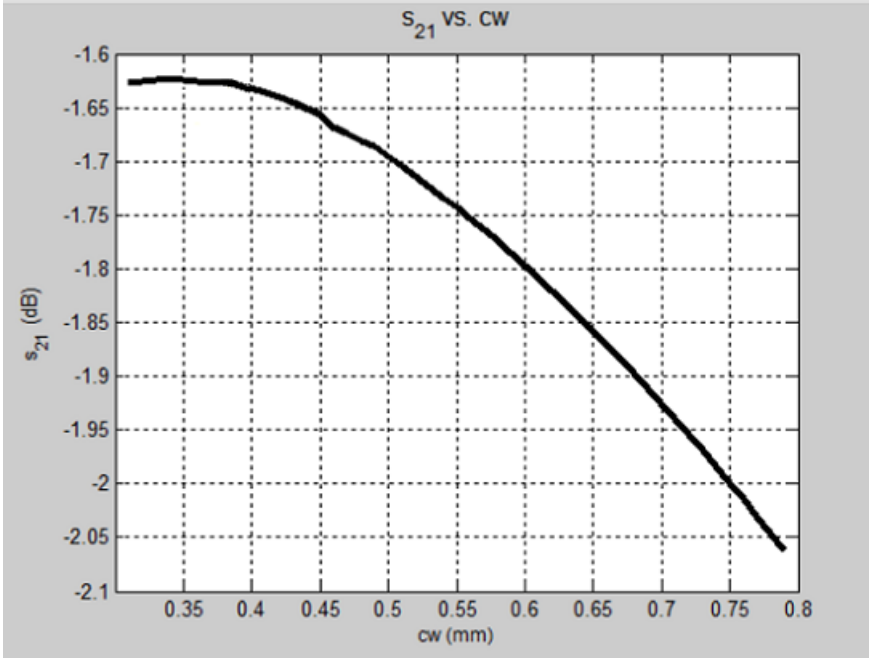

Figure 3.4: s_{21} vs. *cw*

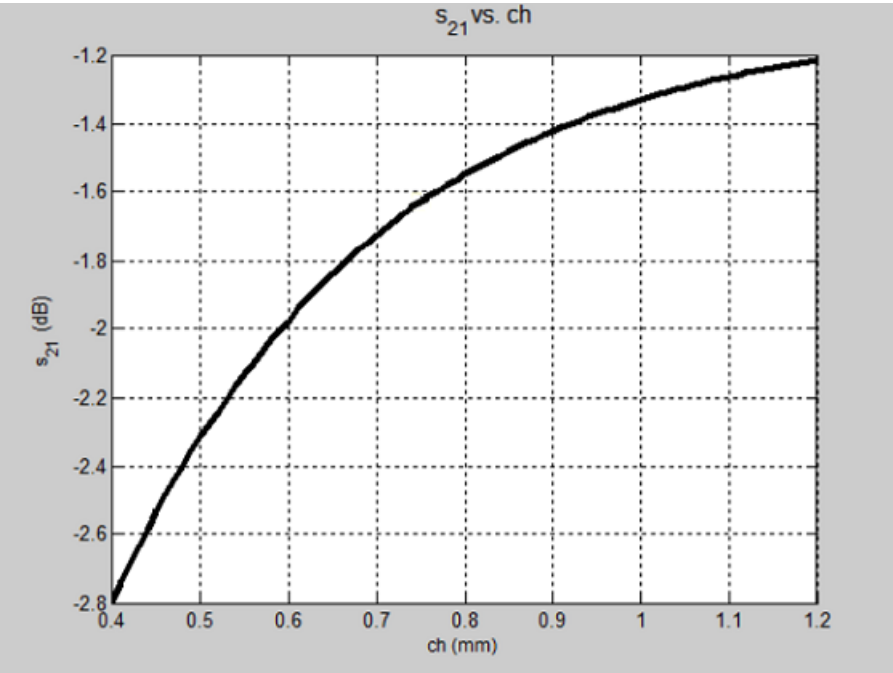

Figure 3.5: s_{21} vs. *ch*

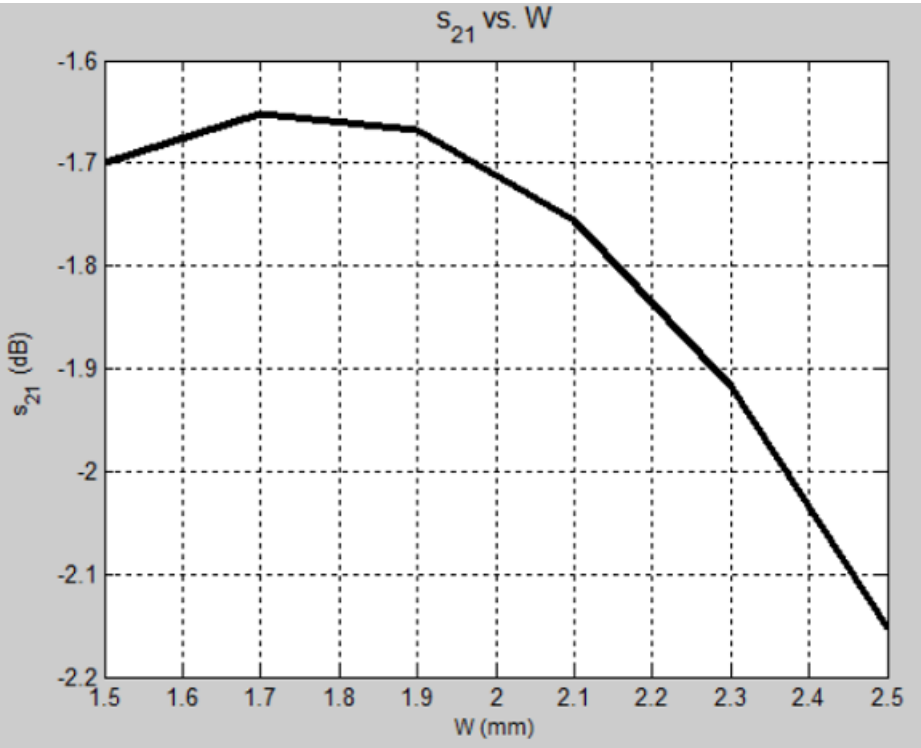

Figure 3.6: s_{21} vs. *W*

Figure 3.7, 3.8, 3.9, 3.10 and 3.11 indicate s_{11} behaviour based on the different dimensions of the patch. *cgap* and *ch* do not affect the resonant frequency, whereas *cw*

and W slightly affect it. It is observed that resonant frequency is mostly determined by L of the patch.

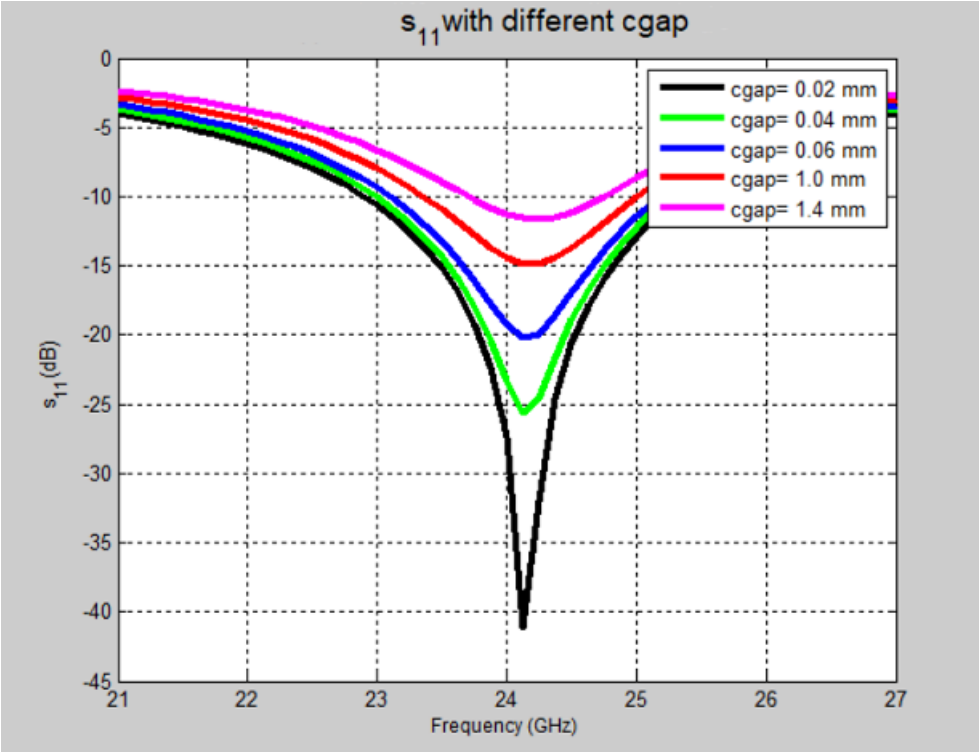

Figure 3.7: s_{11} with different *cgap*

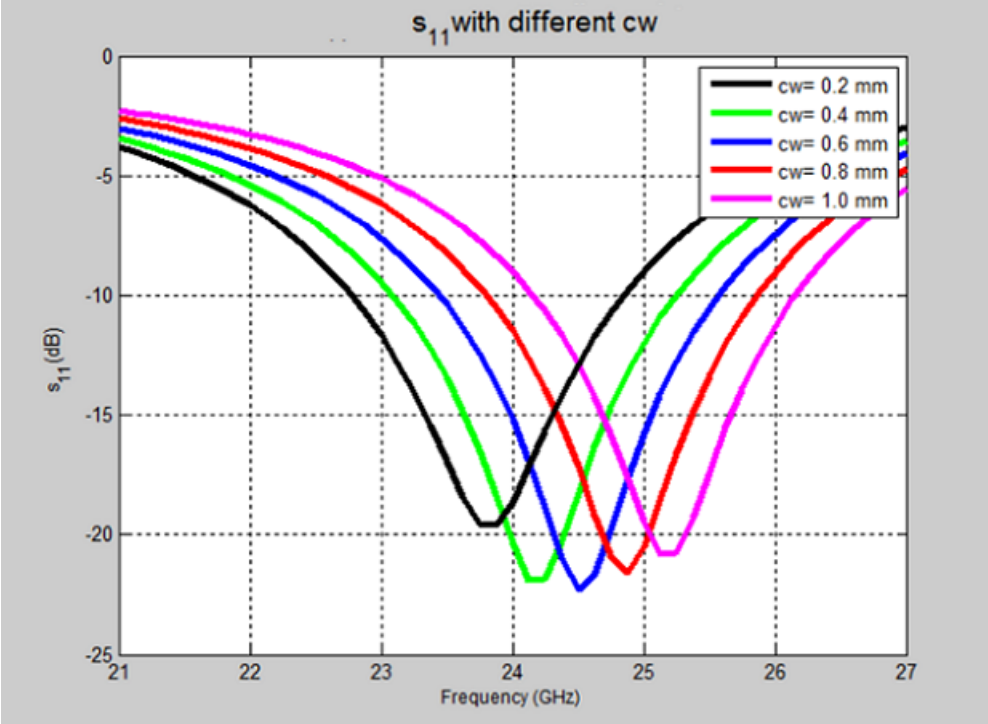

Figure 3.8: s_{11} with different *cw*

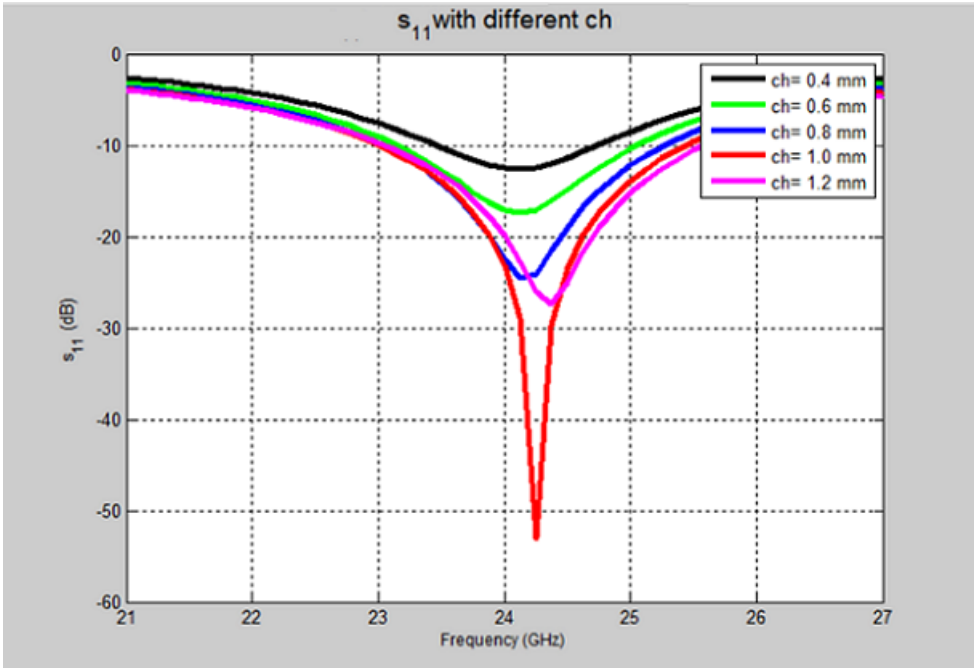

Figure 3.9: s_{11} with different *ch*

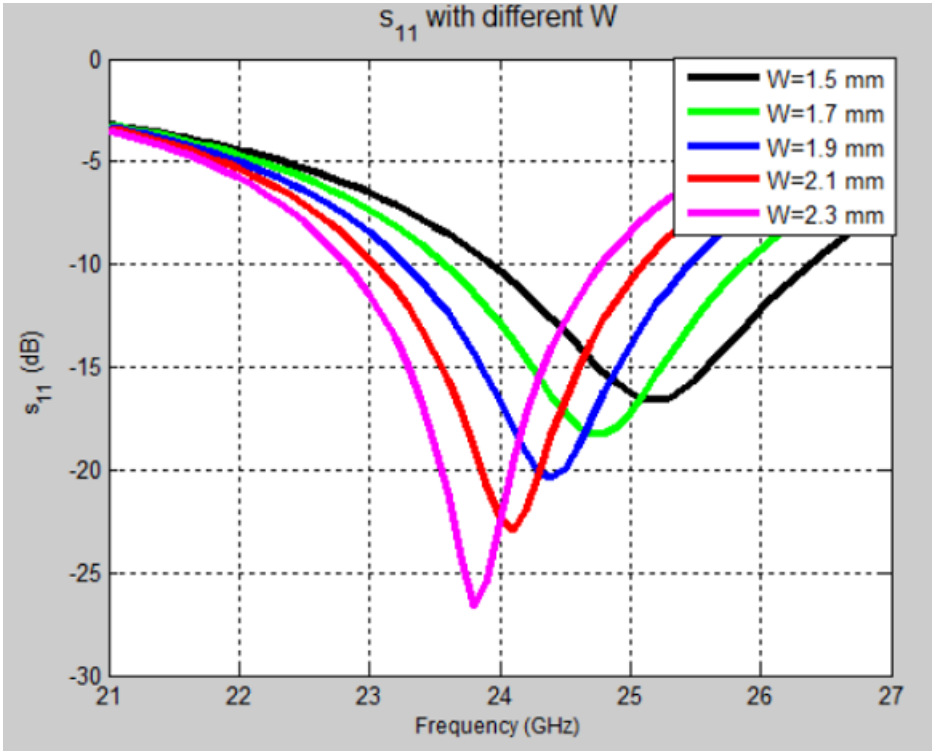

Figure 3.10: s_{11} with different *W*

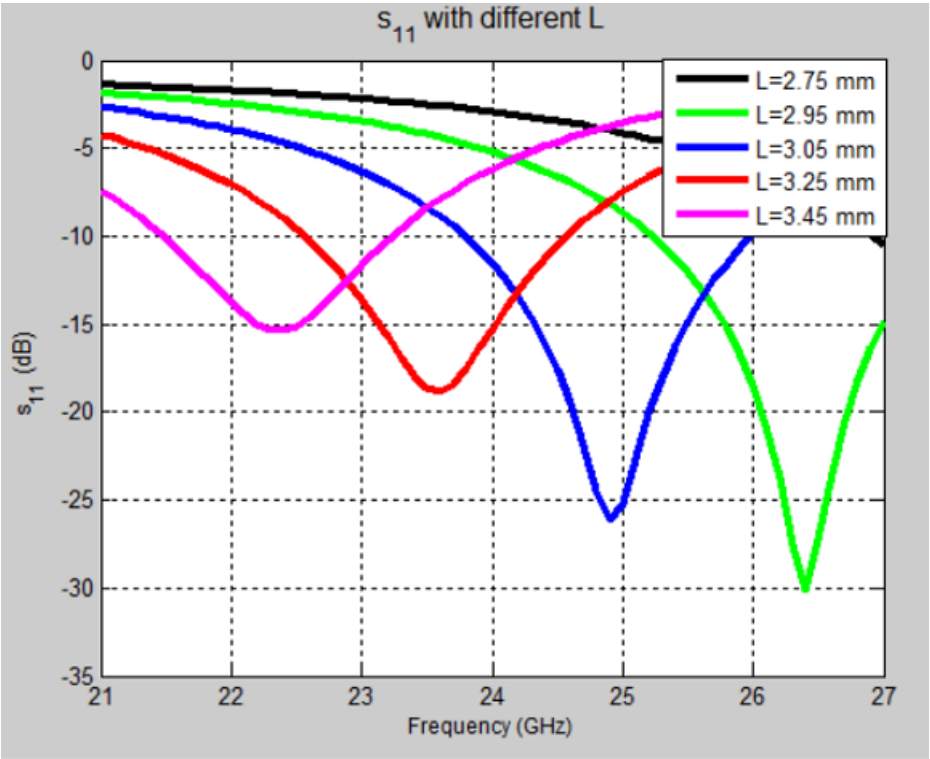

Figure 3.11: s_{11} with different L

In brief, dimensions of specialized patches are mostly determined according to operation frequency, and proposed s_{21} value.

3.3 Design of the Array

Microstrip patch antenna array, which includes in line coupled series feed structure operating at 24.125 GHz, is designed in HFSS 3D Layout Simulation Programme. 20 mils thickness RO4350 substrate having dielectric constant ε=3.66 and tangent loss tanδ=0.0037 is used. The design requirements are given in Table 3.2.

Table 3.2: Design requirements

Frequency	24 - 24.25 GHz
Bandwidth	250 MHz
E-Plane HPBW	12 degrees
H-Plane HPBW	30 degrees
Side Lobe Level	-15 dB

The design steps designated in the first section of this chapter (Section 3.1) are im-

plemented according to the design requirements of this study.

First, the size of the array is determined. Inter-element spacing is chosen as λ_g which equals to 0.56λ at operating frequency. 12 degree (≈ 0.21 radians) E-plane half power beamwidth requirement is provided with eigth elements, whereas 30 degree (≈ 0.53 radians) H-plane half power beamwidth requirement is provided with four elements according to the given formula in Chapter 2, Equation 2.1.

Second, patches are designed individually. As mentioned previously (in Section 3.1), amplitude tapering in the E-plane is provided by the patch structures. Since eight patches are symmetric around the feed point, four patches, which comprise half column of the array, are designed and copied to the other half. Power coefficients of the patches are determined from the in-house software in order to obtain -20 dB SLL, and those coefficients are given in Table 3.3. Each of the four patch elements is numbered successively according to their position with respect to the center feeding point of a column. To clarify, number 1 refers to the first patch which is right next to the feeding point.

Table 3.3: Power coefficients and s_{21} values of each element

Element Number	Power Coefficient
1	1
2	0.7225
3	0.4489
4	0.2025

s_{21} values of individual patches are calculated from the formula given in 3.1. The calculation is given in Equation 3.2 and the results are given in Table 3.4.

$$
\begin{aligned}
s_{21}(Element1) &= 10log(1 - \frac{1}{2.3739}) \\
s_{21}(Element2) &= 10log(1 - \frac{0.7225}{1.3739}) \\
s_{21}(Element3) &= 10log(1 - \frac{0.4489}{0.6514})
\end{aligned}
\tag{3.2}
$$

Table 3.4: Calculated s_{21} values of each element

Element Number	s_{21} Value
1	-2.38 dB
2	-3.24 dB
3	-5.08 dB

It is concluded in the previous section that, s_{21} is inversely proportional to *cgap* and *cw* while it is proportional to *ch*. Identical, 100 Ω transmission lines are used between the patches, which means that widths of input and output transmission lines of those patches are same. Lengths of output transmission lines of the patches are determined according to the distance between patches which is λ_g. The expected value of the phase of the s_{21} is zero for the in-phase feeding. Based on this information, four patch elements of the half column of the array are designed one by one. The dimensions of the patches are given in Table 3.5.

Table 3.5: Dimensions of the elements

Element Number	W (mm)	L (mm)	iw (mm)	ih (mm)	cw (mm)	ch (mm)	cgap (mm)
1	3.58	2.99	0.10	0.15	0.40	1.30	0.09
2	3.65	3.18	0.30	0.76	1.39	0.96	0.22
3	3.89	3.19	0.30	0.72	1.16	1.10	0.14
4	4.25	2.85	0.30	0.60	-	-	-

s_{21} values of the designed patches are given in Figure 3.12,and their values at the center frequency are compared with the calculations in Table 3.6. It is observed that calculated values are almost obtained in the design.

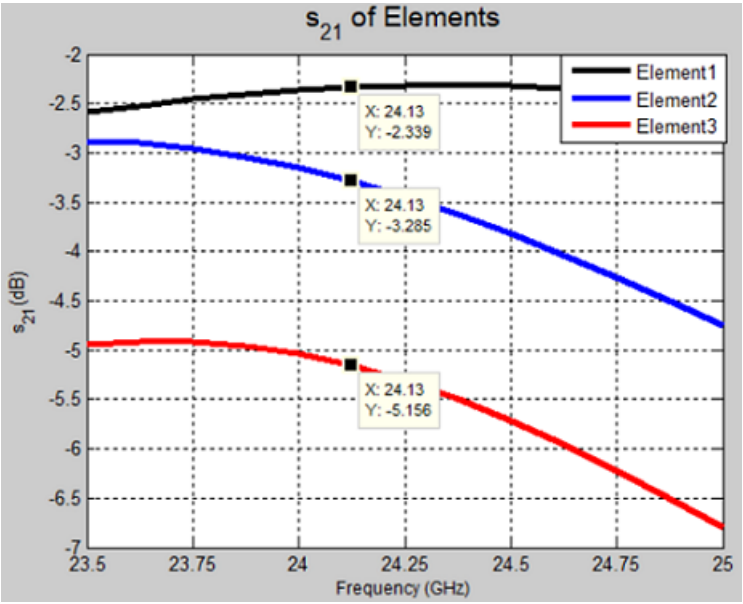

Figure 3.12: s_{21} of elements

Table 3.6: Comparison of calculated and simulated s_{21} value of each element

Element Number	Calculated s_{21} Values	Simulated s_{21} Values (24.125 GHz)
1	-2.38 dB	-2.33 dB
2	-3.24 dB	-3.28 dB
3	-5.08 dB	-5.15 dB

Individually designed elements are integrated, and half column of the array is completed. This half is symmetrised with the delay section which has 180 degree electrical length in order to ensure in-phase feeding. Symmetrical halves of the delay section are located at identical distance (2.17 mm) from the feeding point of a column as shown in Figure 3.13(a). First antennas are connected to feeding points at the each side of the delay section as shown in Figure 3.13(b). To test whether in-phase feeding of elements is satisfied, phase difference between Port 1 and Port 3 is calculated by full wave simulations and plotted in Figure 3.14. It is observed that phase difference is 180 degrees as expected.

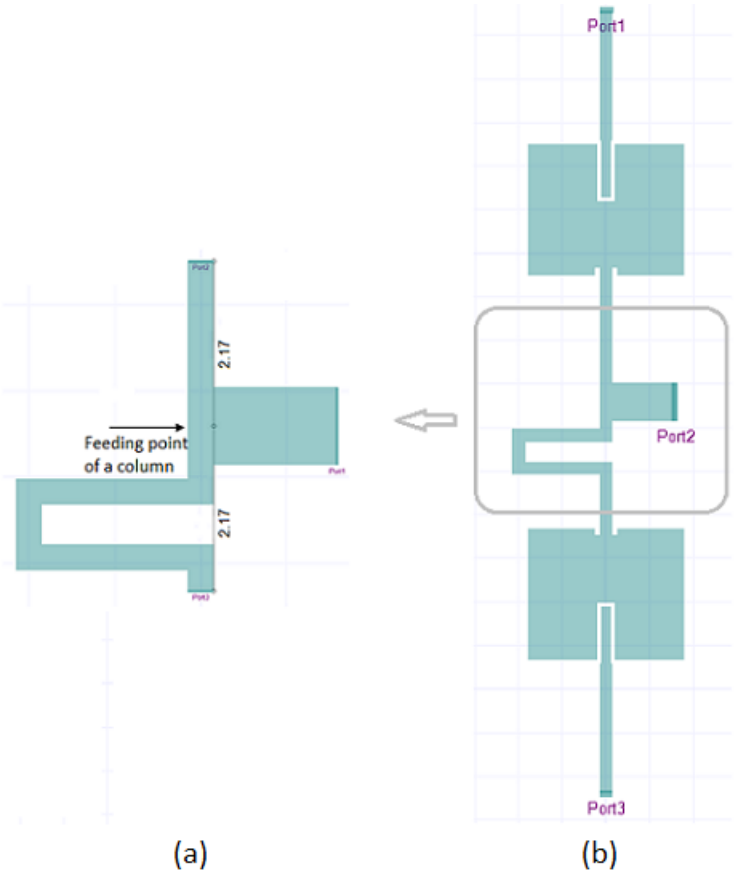

Figure 3.13: 180 degree electrical length delay section structure

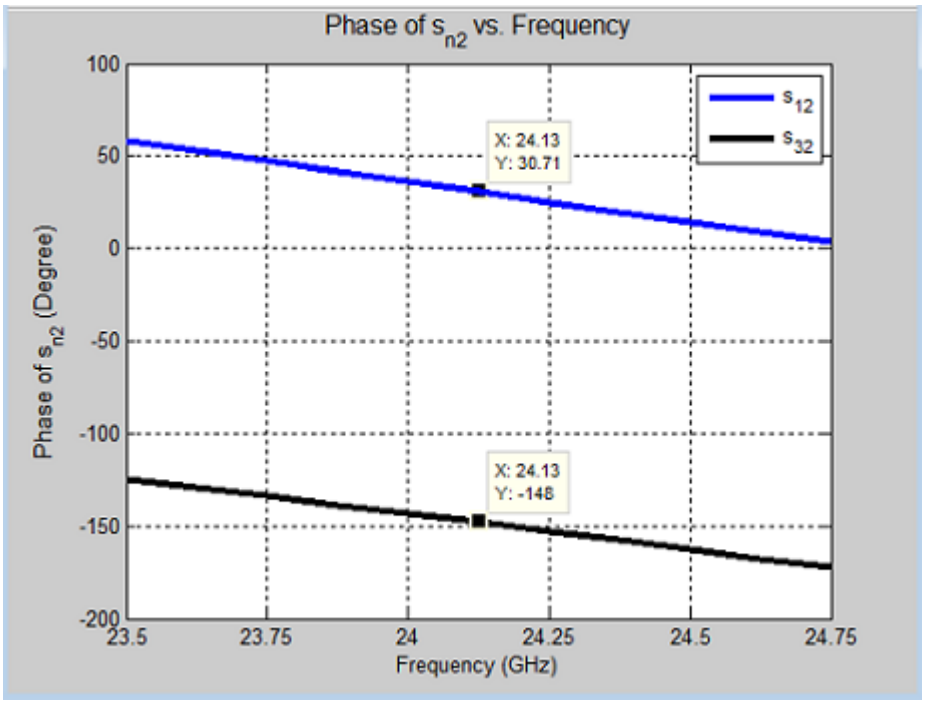

Figure 3.14: Phase difference between two elements located at each side of the delay section

Figure 3.15 shows half side with numbered elements and the column of array, and Figure 3.16 shows E-plane radiation pattern of the column of array. It is observed that 12 degree HPBW requirement is achieved. Asymmetry in the side lobes, which are -15 dB and -13 dB, are caused by the delay section. Current distribution on the column is obtained by full wave simulations and plotted in Figure 3.17. Although elements are symmetric except meandered delay section, current distribution over the column is not symmetric. The symmetry is disturbed due to the coupling between meandered delay line and adjacent patch. It is also observed that the current on the corners of delay section is strong, so that delay section also radiates and distorts the symmetry in the radiation pattern of the array.

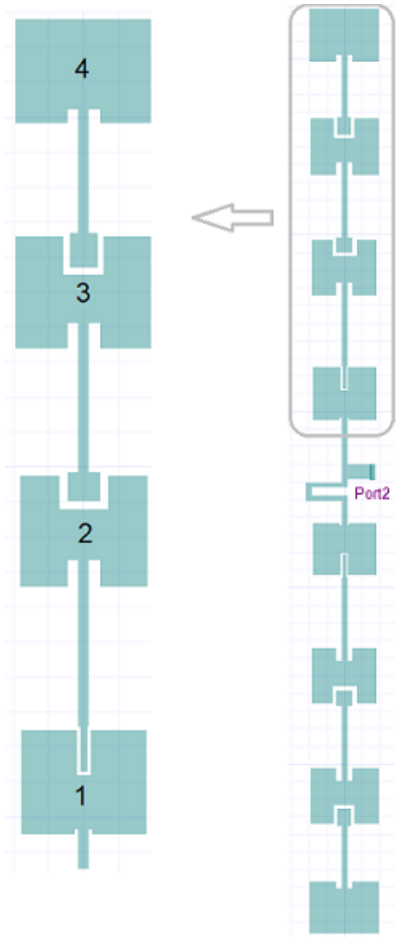

Figure 3.15: Half and full side of a column of the array

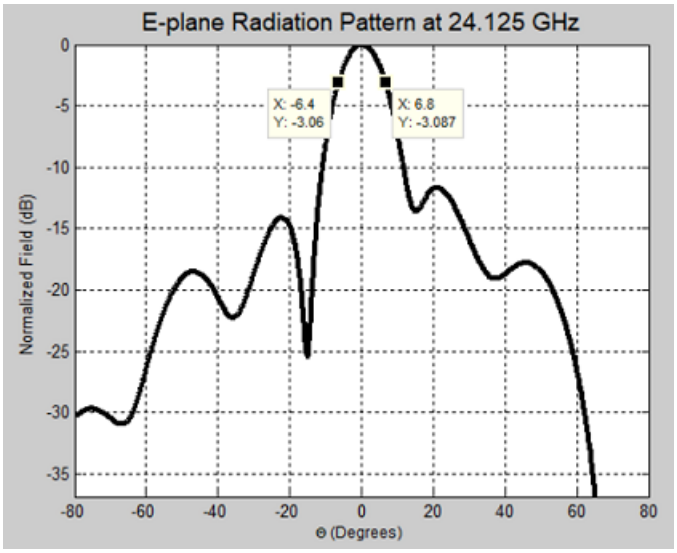

Figure 3.16: E-Plane radiation pattern of a column of the array

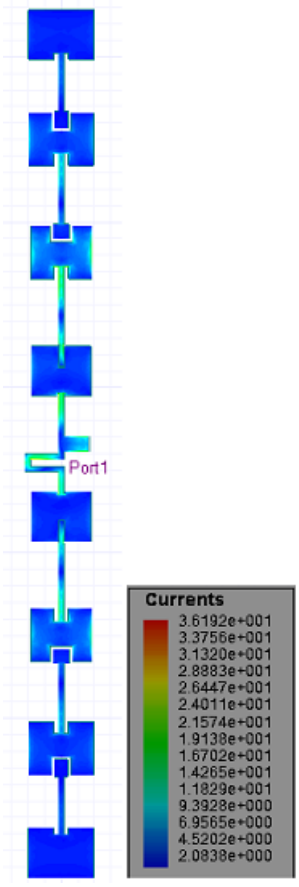

Figure 3.17: Current distribution

Third step for the in line coupled series fed microstrip antenna array is designing power divider structure for the H-plane. There are four elements, and the structure

is bilaterally symmetric as similar to the design in Chapter 2. The design of power divider structure is explained in Section 2.2. The same steps are applied. First, power coefficients are determined in an attempt to obtain -20 dB side lobe level. Second, impedances of power division points are calculated from the formula given in Equation 2.2. Half of the power divider structure is illustrated in Figure 3.18. Power coefficients and impedances of power division points are given in Table 3.7.

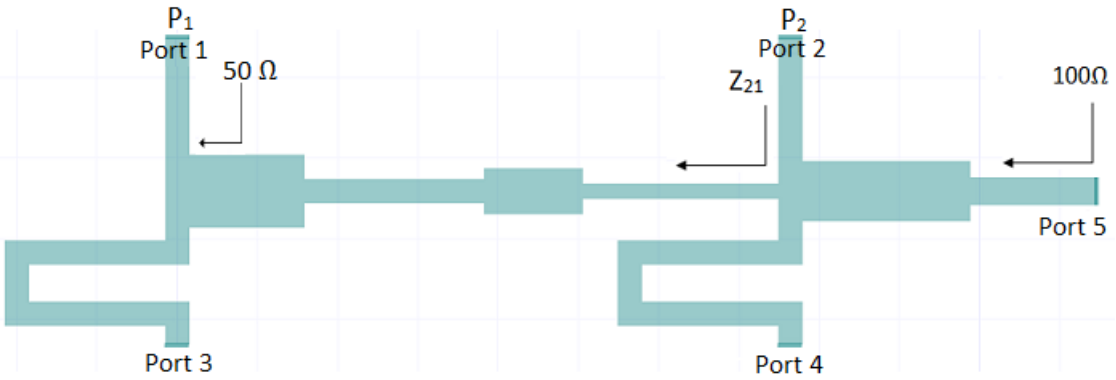

Figure 3.18: Half row of the power divider structure

Table 3.7: Power coefficients and impedances of power division points

Power Coefficients	Impedances of Power Division Points
P_1= 0.16, P_2= 1	Z_{21}= 312.5 Ω

As a third step for the power divider structure design, Z_{21} is matched to 50 Ω, which is the impedance of the delay section. Structure is shown in Figure 3.19. Four times quarter wave impedance transformation are applied. Used transmission lines and impedances of those lines are given in the Table 3.8.

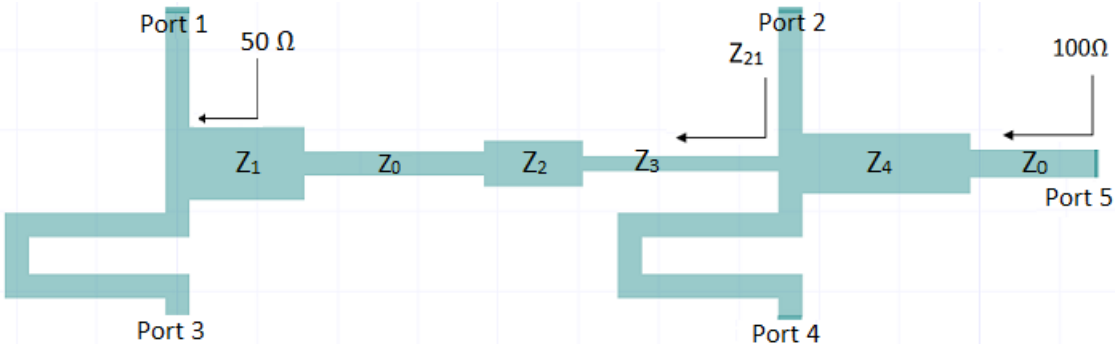

Figure 3.19: Half row of the power divider structure

Table 3.8: Impedance values of transmission lines

Impedance values of transmission lines
Z_0=100 Ω
Z_1=61 Ω
Z_2=75 Ω
Z_3=115 Ω
Z_4=66 Ω

Half row of the power divider structure is symmetrized and copied to the other side as shown in Figure 3.20. Amplitude and phase of s_{n5} of each feeding line are checked from this structure (n is the port number of the each feeding line). Figure 3.21 shows s_{n5} values with respect to the frequency.

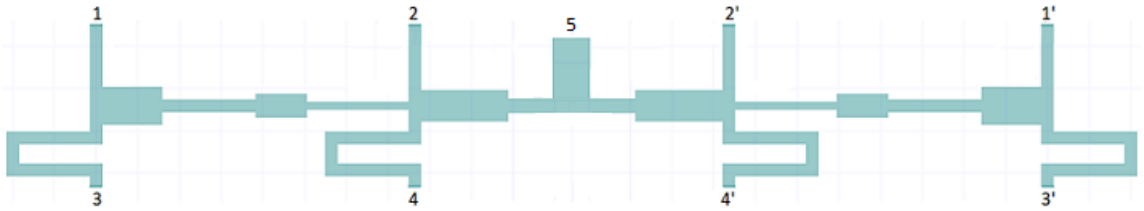

Figure 3.20: Power divider

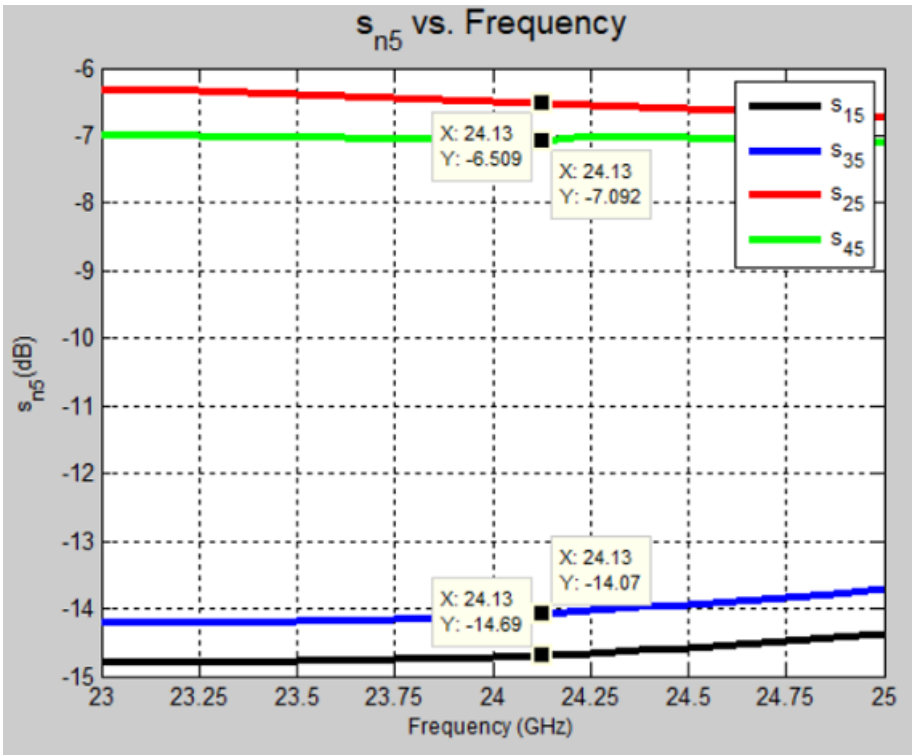

Figure 3.21: s_{n5} vs. frequency

Comparison of calculated and simulated s_{n5} values at the 24.125 GHz are given in Table 3.9. Simulation values are close to the calculated ones which satisfies that chosen power coefficient values are obtained.

Table 3.9: s_{n5} of feeding lines

Calculated s_{n5}	Simulated s_{n5} (24.125 GHz)
$s_{15} = 10 \log \frac{0.08}{2.32}$ = -14.62 dB $s_{35} = 10 \log \frac{0.08}{2.32}$	s_{15} = -14.69 dB s_{35} = -14.07 dB
$s_{25} = 10 \log \frac{0.5}{2.32}$ = -6.67 dB $s_{45} = 10 \log \frac{0.5}{2.32}$	s_{25} = -6.51 dB s_{45} = -7.09 dB

Power divider structure is integrated with the columns of the array. The final design of in line coupled series fed microstrip patch antenna array is shown in Figure 3.22.

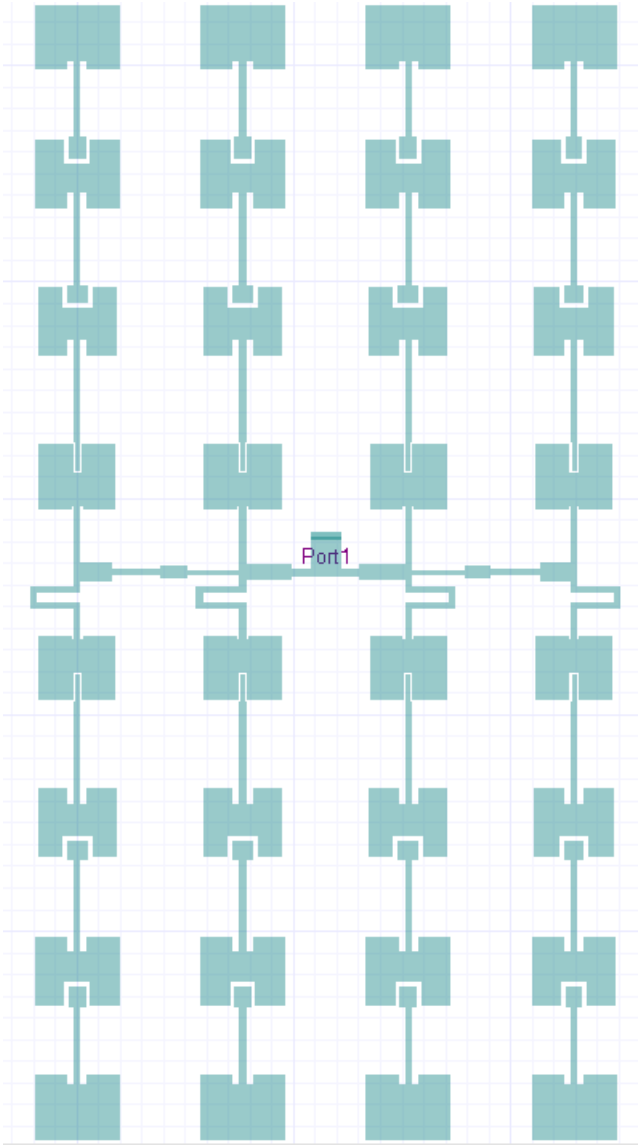

Figure 3.22: In line coupled series fed microstrip patch antenna array

3.4 Simulation Results

Radiation patterns and return loss of designed array are given in this section.

Input return loss, s_{11}, of the designed array is shown in Figure 3.23. In the operating band, return loss values are less than -15 dB. 10 dB bandwidth is 1.75 GHz (23.875-25.625 GHz).

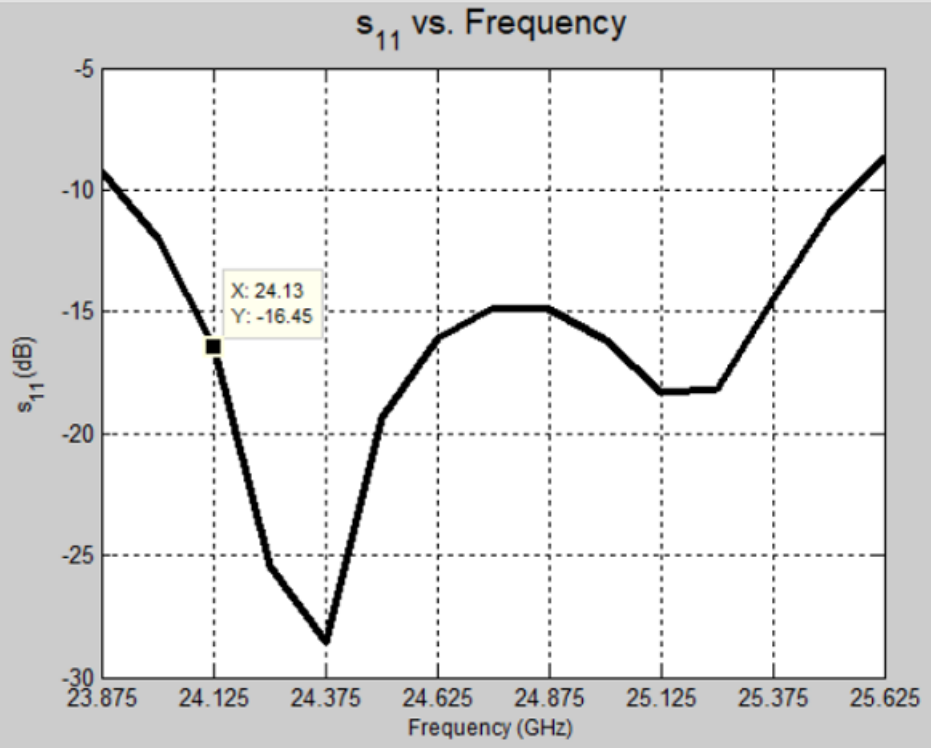

Figure 3.23: s_{11} vs. frequency

E-plane radiation pattern is given in Figure 3.24. It is shown that 12 degree beamwidth is obtained. However, there is asymmetry in the side lobes. Design calculations are performed in order to obtain -20 dB SLL. During the simulation it emerges as nearly -13 dB. This discrepancy and asymmetry are due to the delay sections. Those sections affect the symmetry of the design and cause larger side lobe levels. In order to justify this argument, simulations without delay sections are performed, that is, horizontal power divider structure is not used as shown in Figure 3.25. All ports are excited with predetermined power coefficients (Port1, Port2, Port7 and Port8 are 0.16 and Port3, Port4, Port5 and Port6 are 1), and Port2, Port4, Port6 and Port8 are excited with 180 degree phases in order to provide in-phase feeding. E-plane radiation pattern of this structure are given in Figure 3.26. It is shown that when power divider structure and delay sections are not used, the pattern is symmetric and side lobes are around -16 dB. Coupling between delay section and adjacent patch and radiation from delay line distort the pattern and causes asymmetry.

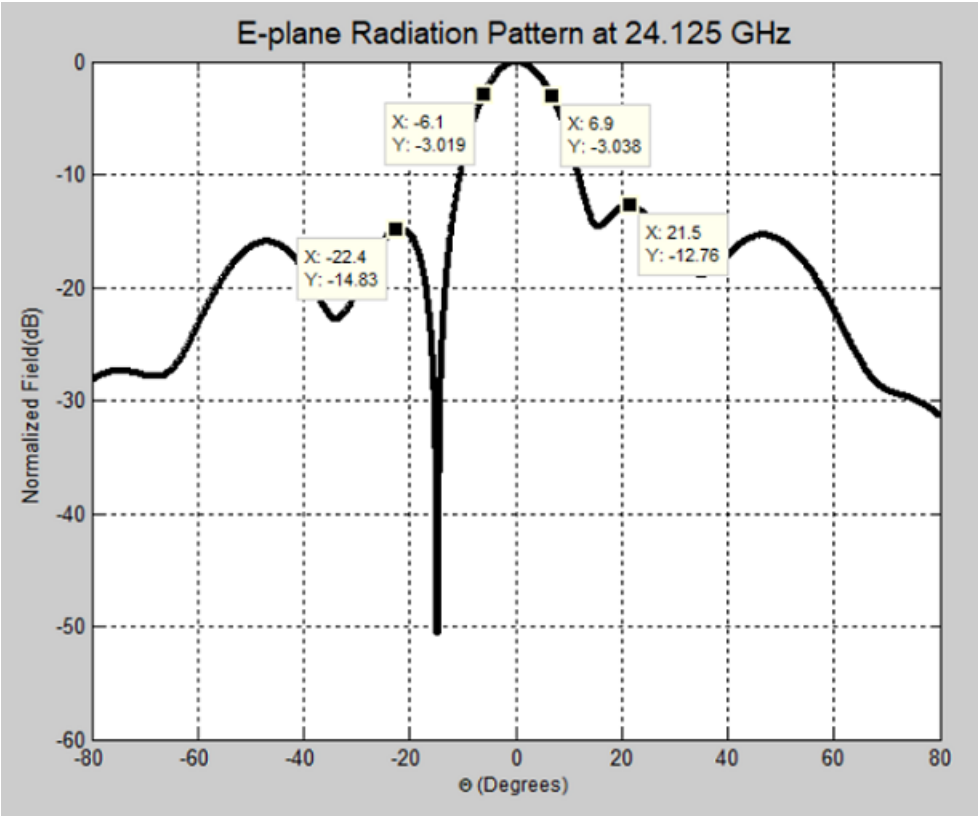

Figure 3.24: E-plane radiation pattern of the designed array

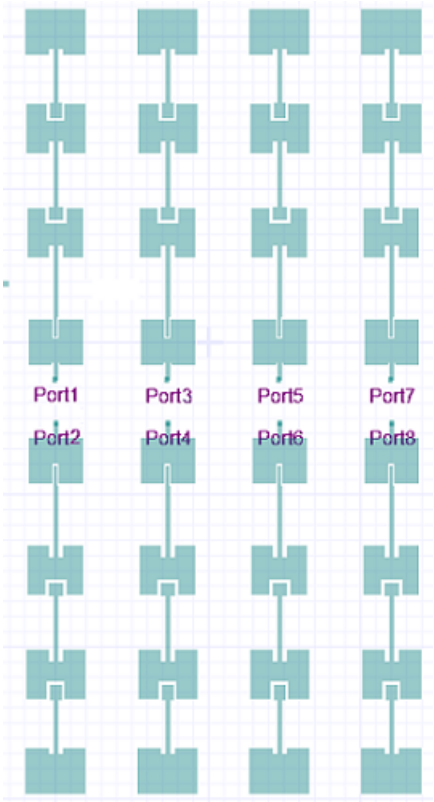

Figure 3.25: Array without power divider structure

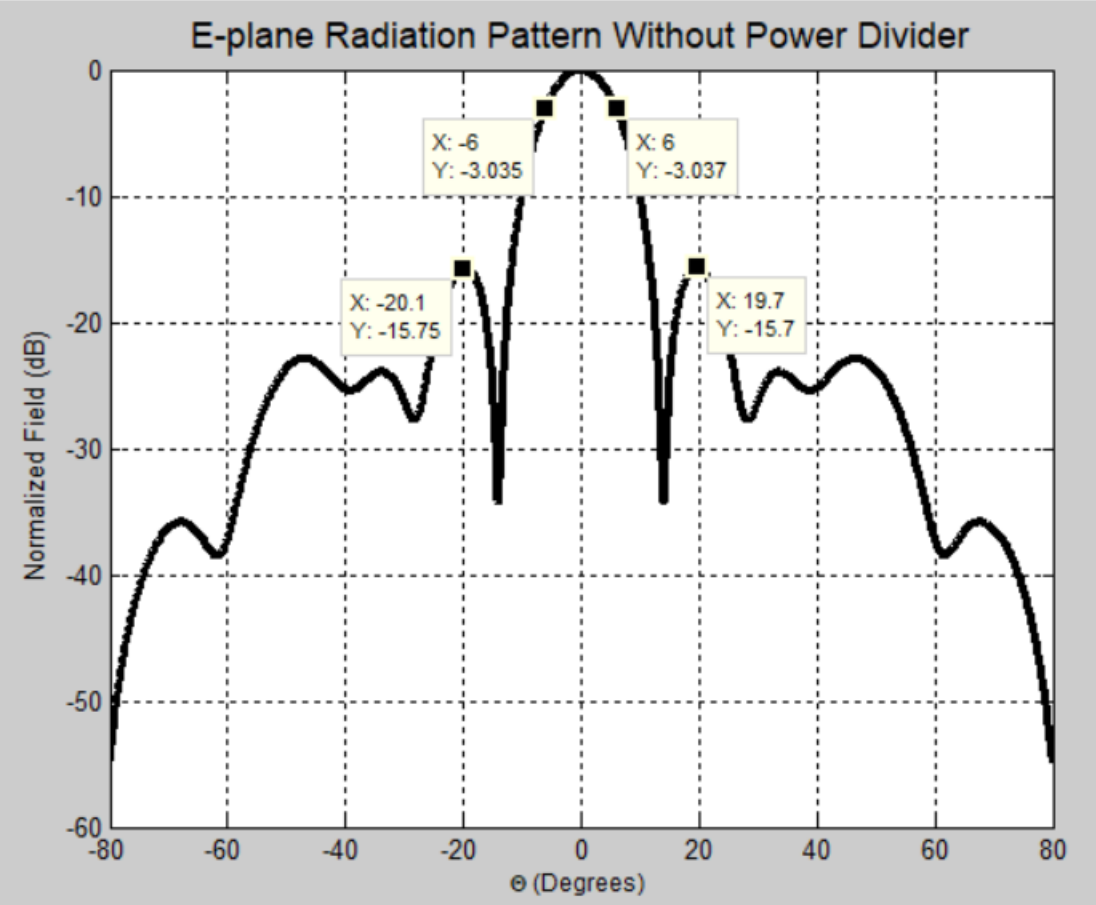

Figure 3.26: E-plane radiation pattern of the array given in Figure 3.25

H-plane radiation pattern is given in Figure 3.27. It is shown that 27.6 degree HPBW is obtained. From the array factor, beamwidth is calculated as 28 degrees, simulation results are compatible with calculation.

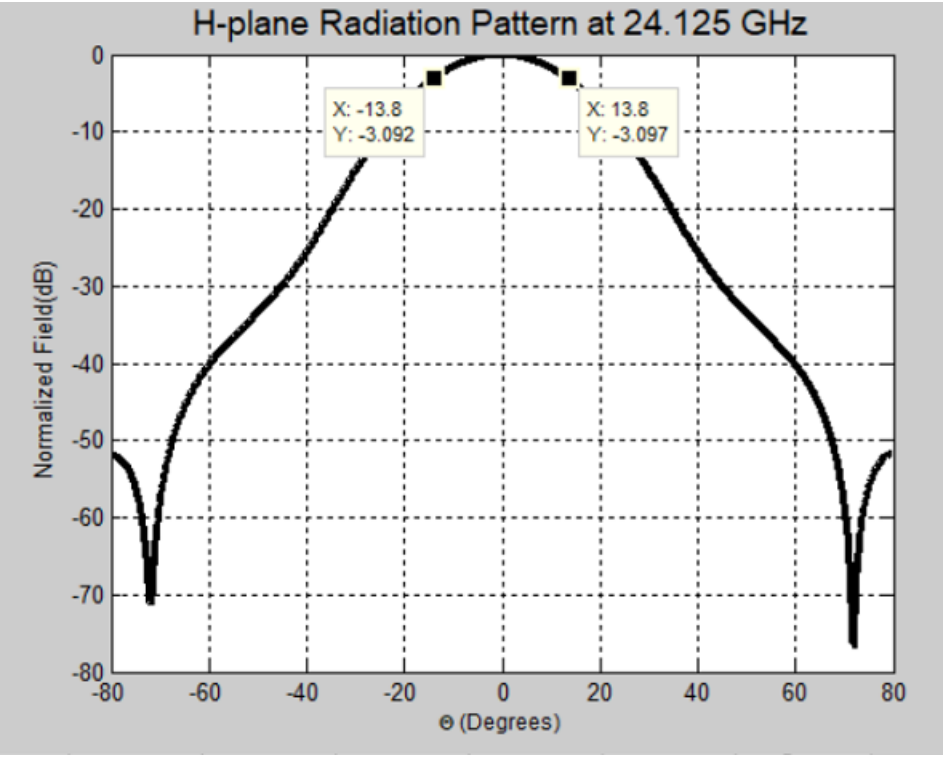

Figure 3.27: H-plane radiation pattern of the designed array

Designed array in this chapter is not fabricated. For that reason, only the simulation results are given. The results are consistent with the calculations.

CHAPTER 4

CONCLUSION

This thesis presents design of two different microstrip patch antenna arrays with series feeding networks. Both arrays are designed for traffic radar applications, and they operate at 24.125 GHz with 250 MHz bandwidth.

First designed array, which is presented in Chapter 2 is a microstrip patch antenna array with shunt connected series feed network. In this type of networks, elements are located side by side, and their views look like shunt architectures. However, all the elements are fed from a single line power divider structure. This design has some important features. Beamwidth requirements determine the dimension of the array. Amplitude tapering on the other hand, is provided according to the side lobe level requirements. One of the most common approaches for the amplitude tapering is modifying power divider structure between identical elements.

Designed array in Chapter 2 is proposed for monitoring a single lane on the roads. For that reason, it has a 7 degree narrow beamwidth for both E and H-planes. 14 x 14 patch elements are included in this design. Amplitude tapering for the side lobe level requirement is provided with different transmission lines between elements, while elements are identical with 100 Ω input impedance. Proposed power divider structure has different impedance values at the corners of power division points. In order to implement them, more than one stage quarter wave impedance transformation is used. The design is fabricated and measured. For the measurements, SMPM connector is used and coplanar waveguide to microstrip line transition structure provides the integration of this connector. Measurements show good agreement with the simulation results. In the measurements, it is shown that 7 degree HPBW is obtained in both

planes. Side lobe levels are -15 dB and -14 dB in the H and E-planes, respectively.

Chapter 3 gives the design of in line coupled series fed microstrip patch antenna array. In this type of networks, elements are fed through single line consecutively with a specific feature. Feeding lines do not have direct connections with the elements, adjacent elements are fed from coupling regions. Dimensions of coupling regions have an important effect on the amplitude tapering which is provided by the coupled feeding signals.

Designed array in Chapter 3 has different beamwidth requirements for H and E-planes. It has 30 degree beamwidth in H-plane and 12 degree beamwidth in E-plane. Therefore array consists of 4 x 8 elements. Adjacent elements on the columns of array are not connected to each other directly, and signal is transmitted from coupled regions of the elements. Transmission lines between elements are identical. On the one hand amplitude tapering is provided with the dimensions of elements especially by adjusting the coupling region parameters. On the other hand, a power divider structure is used for amplitude tapering at the azimuth plane. Simulation results are consistent with the design requirements. 12 degree and 28 degree HPBW are obtained in the E and H-planes, respectively. Side lobe level in the E-plane is nearly -13 dB. This array is not manufactured.

Different feeding techniques for the microstrip patch antenna arrays, such as combination of series and corporate feeding structures, will be studied as a future work.

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