

ELECTRICAL CHARACTERIZATION OF ELECTRON SELECTIVE TITANIUM
DIOXIDE AND HOLE SELECTIVE MOLYBDENUM TRIOXIDE
HETEROCONTACTS ON CRYSTALLINE SILICON

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
MIDDLE EAST TECHNICAL UNIVERSITY

BY

DOĞUŞCAN AHİBOZ

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF MASTER OF SCIENCE
IN
PHYSICS

SEPTEMBER 2017

Approval of the thesis:

ELECTRICAL CHARACTERIZATION OF ELECTRON SELECTIVE TITANIUM
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ABSTRACT

ELECTRICAL CHARACTERIZATION OF ELECTRON SELECTIVE TITANIUM DIOXIDE AND HOLE SELECTIVE MOLYBDENUM TRIOXIDE HETEROCONTACTS ON CRYSTALLINE SILICON

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September 2017, 79 pages

Transition metal oxides are promising materials as an alternative to the conventional charge transport layers in photovoltaic solar cells with the advantages of carrier selectivity and low processing temperatures. In this study, electronic properties of the hole transporting – electron blocking layer (HT-EBL) of sub-stoichiometric Molybdenum (III) Oxide (MoO_{3-x}) and electron transporting – hole blocking layer (ET-HBL) of Titanium (II) Oxide (TiO_{2-x}) were studied. For this purpose, carrier selective metal oxide layers with different thickness and deposition conditions were deposited over n-type and p-type crystalline silicon wafers in the structure of Metal-Oxide-Semiconductor (MOS) capacitor. Admittance analysis (capacitance and conductance methods) and current – voltage methods were employed for the characterization of the MOS capacitors. At the end of this study, best deposition

condition and the metal oxide thickness for the most effective carrier transportation at the silicon – metal oxide interface and through the metal oxide layer were determined.

Keywords: Sub-stoichiometric Titanium Dioxide, Sub-stoichiometric Molybdenum Trioxide, Admittance Measurement, Current Voltage Measurement, Hole Selectivity, Electron Selectivity.

ÖZ

SİLİSYUM ALTTAŞ ÜZERİNDE BÜYÜTÜLMÜŞ, ELEKTRON GEÇİRGEN TİTANYUM DİOKSİT VE HOL GEÇİRGEN MOLİBDEN TRİOKSİT İNCE FİLM TABAKALARININ ELEKTRİKSEL KAREKTERİZASYONU

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Tez Yöneticisi: Prof. Dr. Raşit Turan

Eylül 2017, 79 sayfa

Düşük sıcaklıkta üretim ve seçici yük geçirgenliği üstünlüğü taşıyan geçiş metallerinin oksitleri, fotovoltaik güneş gözelerinde geleneksel olarak kullanılan yük taşıyıcı tabakaların umut veren bir alternatifidir. Bu araştırmada, eksik katlı Molibden (III) Oksiti'nin hol geçirgen – elektron engelleyici ve Titanyum (II) Oksiti'nin elektron geçirgen – hol engelleyici tabakalarının elektronik özellikleri çalışıldı. Bu amaç için metal oksitler, n-tipi ve p-tipi silisyum alt taş üzerinde farklı koşullar altında ve tabaka kalınlıklarında Metal - Oksit – Yarı İletken (MOS) Kapasitörler yapmak üzere büyütüldü. MOS kapasitörlerin karakterizasyonu için Admittans Analizi (kapasitans ve iletkenlik yöntemleri) ve Akım – Gerilim yöntemleri kullanılmıştır. Bu çalışmanın sonucunda silisyum – metal oksit ara yüzeyinde ve metal oksit tabakası boyunca etkili yük iletimini sağlamak için gerekli olan ideal metal oksit tabaka büyütme şartları ve tabaka kalınlığı tespit edilmiştir.

Anahtar kelimeler: eksik katlı titanyum dioksit, eksik katlı molibden trioksit, admitans ölçümü, akım gerilim ölçümü, elektron geçirgenliđi, hol geçirgenliđi.

To my family

ACKNOWLEDGMENTS

First and foremost I offer my heartfelt gratitude to my supervisor, Prof. Dr. Raşit Turan, who has supported me during the course of my thesis with his patience and knowledge at the same time as allowing me the room to work in my own way. I attribute the level of my Masters degree to his encouragement and effort and without him this thesis, too, would not have been completed.

I would like to thank Dr. Hisham Nasser who encouraged me to study transition metal oxide, for many perceptive conversations during the development of the ideas in this thesis, and for helpful comments and reviews on the text.

I am much obliged to GÜNAM members Prof. Dr. Mehmet Parlak, Hande Emine Çiftpınar, Dr. Fırat Es, and Ergi Dönerçark for their help during my research. I am also highly grateful to Dr. Özlen Ferruh for her guidance and valuable comments.

I am very thankful to my precious friends Gilda Afshari (Zerrin Taş), Nevra Akalın, Merve Akkaya, Erolcan Akbaba, Koray Kaymazlar and Fırat Yalçın who I spent my years together at the physics department

I feel very lucky to have valuable friendship and support of Yasemin Durmuş, Havle Güney, Serra Memiş, Başak Sezgi Bilen. I appreciate the joy Araylın Gaipova and my beloved bacanak Okan Ata Küçük brought to my house while I am dealing with this thesis.

My uttermost gratitude to Özge Azeri for her love, patience and invaluable support which have been encouraging me in my professional and personal life. It is my greatest honor and biggest happiness to have her in my life.

The last but not the least, special thanks to my mother Feriha Gül supporting me whenever I need her, and my grandparents who brought me up with love and encouragement - Saadet Gül and Ahmet Kaya Gül. I would like to thank all members of my family for their continuous affection and heartening.

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LIST OF ABBREVIATIONS

HT-EBL	Hole transporting-electron blocking layer
ET-HBL	Hole blocking-electron transporting layer
MoO ₃	Exact stoichiometric molybdenum trioxide
MoO _{3-x}	Sub-stoichiometric molybdenum trioxide
TiO ₂	Exact stoichiometric titanium dioxide
TiO _{2-x}	Sub- stoichiometric titanium dioxide
MOS	Metal oxide semiconductor
TMOS	Transition metal oxide semiconductor
CB	Conduction band
VB	Valence band
E _g	Band gap energy
E _C	Conduction band edge energy
E _V	Valence band edge energy
E _F	Fermi level energy
E _i	Intrinsic fermi level energy
DC	Direct current
AC	Alternating current
SCR	Space charge region
PPC	Parallel Plate Capacitor

SiO ₂	Silicon Dioxide
PDA	Post deposition annealing
ALD	Atomic Layer Deposition
TDMAD	Tetrakis(dimethylamido)titanium
HF	Hydrogen Flourur
UV-Vis	Ultra violet-vissible
FN	Fowler Nordheim

CHAPTER 1

INTRODUCTION

Crystalline silicon (cSi) based solar cells consisting of diffusion-doped homo-junctions, such as standard (sometimes called Aluminum Back Surface Field Al-BSF) and Passivated Emitter and Rear Contact (PERC) designs which require high thermal budget, to effectively separate photo-generated charge carriers have dominated the photovoltaic industry for the last decades [1]. In these types of homojunction designs, solar cells carrier selectivity is usually achieved by forming heavily doped Si zones which require high production costs and complicated deposition systems. Fabricating a cost effective homo-junction cSi solar cell is usually accompanied with several technological as well as optoelectronic challenges including Auger recombination, minority carrier transport, recombination based losses, and the need of indispensable elevated temperature doping processes [2]. Considerable number of the above mentioned challenges can be eliminated by the use of selective contacts to completely replace doped silicon layers while holding the capacity to effectively separate photo-generated charge carriers without exploiting high temperature doping processes[3].

Recently, sub-stoichiometric molybdenum trioxide has been attempted to substitute p-type amorphous silicon layer in Silicon Heterojunction (SHJ) [4] Solar Cell and 22.5% conversion efficiency has been reported [5]. More feasible cell architecture with hole collecting MoO_{3-x} deposited on top of n-type crystalline silicon (moly-poly) and p-type crystalline silicon (moly-BSR) were established with conversion efficiencies of 16.7% and 16.4% respectively [6]. Even more simpler and cost effective low temperature budget concept, the Dopant Free Hetero-Contact; DASH Cell as

illustrated, has been recently introduced with photon conversation efficiency of 19.42% [2].

Titanium dioxide (TiO_2) has been intensively utilized in a wide range in the field of semiconductor, environmental sciences, and industry owing to its chemical stability, distinct optical and electrical properties, and non-toxicity [7]-[8]. Its high dielectric constant (κ) makes it a suitable candidate to serve as a passivation layer in cSi solar cells and gate dielectric with even thinner thicknesses than that can be achieved by other dielectric materials such as SiO_2 and Si_3N_4 [9],[10]. Recently, TiO_2 has attracted an attention as carrier selective transport layer in photovoltaic devices [11].

In recent times, cSi solar cells based on TiO_{2-x} electron transport and surface passivation layer have been demonstrated by Gad et al. and integrated in high efficiency cSi solar cell designs with efficiencies exceeding 20% [12],[13]. Moreover, TiO_2 has been used in organic solar cells designs such as dye-sensitized and organic heterojunction bulk structures as transport layer or protection layer against degradation [14].

1.1. Semiconductor Heterojunctions

A heterojunction is formed when two semiconductors with different bandgap energies (E_g), dielectric constant (ϵ), electron affinity ($q\chi$), and work function ($q\phi_s$) are connected [15]. Figure 1 illustrates energy band diagram of the two semiconductors (n-type semiconductor-1 and p-type semiconductor-2) materials before the junction between the two semiconductors is formed. Contrary to semiconductor homojunction, the conduction band energy levels (ΔE_c) of two semiconductors (E_{C1} and E_{C2}) as well as the valance band energy levels (ΔE_v) of two semiconductors (E_{V1} and E_{V2}) are not equal.

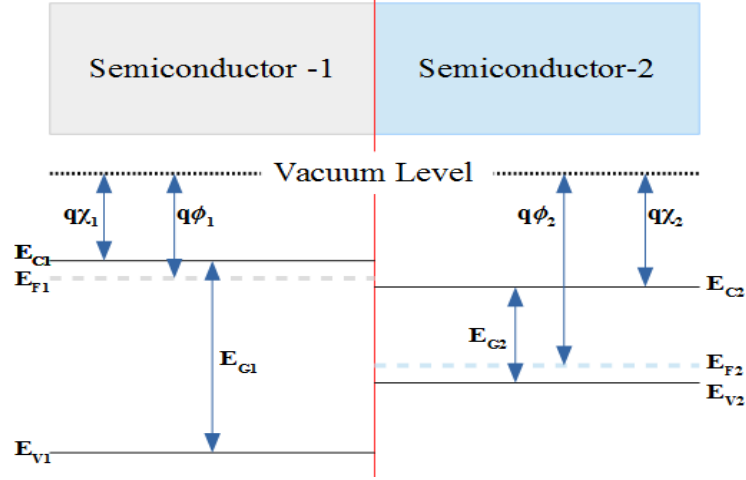
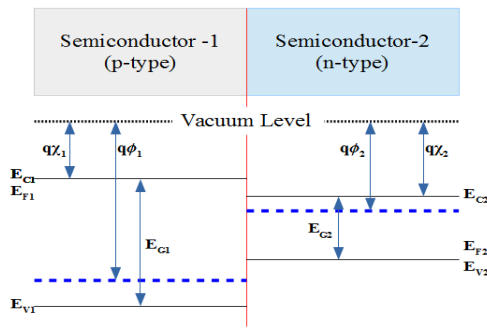


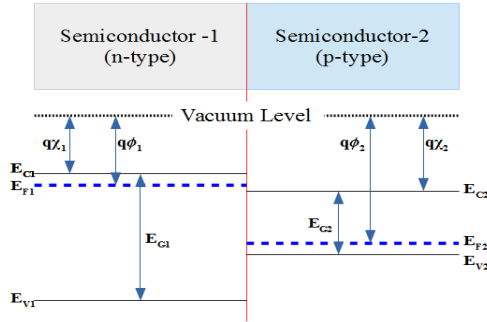
Figure 1. Band diagram of two distinct semiconductors before heterojunction formation

1.1.1. Band Alignment of Heterojunctions

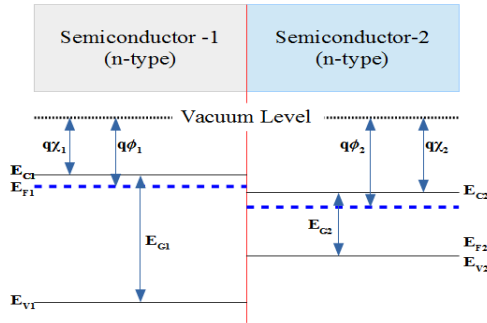
When the two semiconductor in the Figure 1 form a heterojunction, free charge carriers are exchanged between the semiconductors until a thermodynamic equilibrium is achieved. Thermodynamic equilibrium requires Fermi levels of any two semiconductor materials which are in contact to be balanced. Band alignment of isotype (p-p and n-n) and anisotype (p-n and n-p) heterojunctions are depicted in figure 2 according Anderson's method [16]. Each heterojunction in Figure 2 has an abrupt interface which means that the interface region is very thin (few atomic layers) concerning carrier diffusion lengths. The work functions of the two different semiconductors ($W_1 = \phi_{f1}$ and $W_2 = q\phi_{f2}$ for semiconductor-1 and semiconductor-2, respectively) change after thermodynamic equilibrium is established since Fermi levels of two semiconductors (ϕ_{f1} and ϕ_{f2}) are balanced at the equilibrium. As a consequence, a potential gradient close to carrier band edges of the semiconductors is formed. This gradient can be modeled as a sharp potential barrier as shown in Figure 2. By treating them as a Schottky barrier, a built-in potential (ϕ_{bi}) can be related to



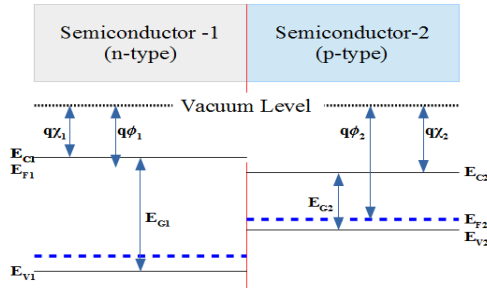
(a)



(b)



(c)



(d)

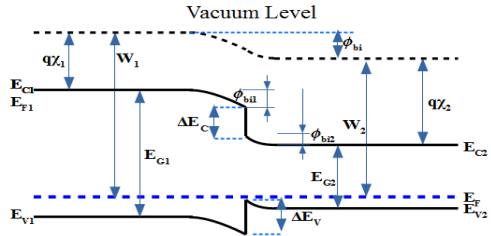
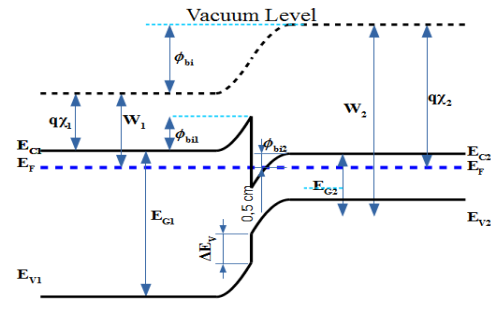
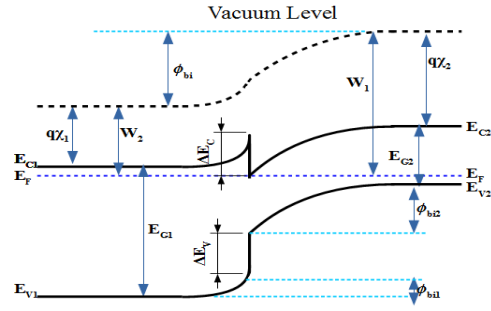
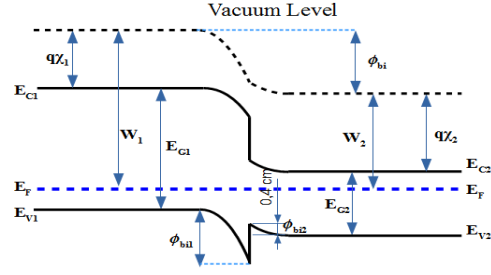


Figure 2. Energy levels before heterojunction formation (left) and band alignments of (a) p-n, (b) n-p, (c) n-n, (d) p-p semiconductors.

band bending between band edges of the two semiconductors according to the following relation:

$$\phi_{bi} = \phi_{b1} + \phi_{b2} \quad (1)$$

where ϕ_{b1} and ϕ_{b2} are the band bendings in semiconductor-1 and semiconductor-2, respectively [15]. Band bending is due to the fact that ϕ_f is constant everywhere within the heterojunction

If the energy difference between conduction or valence band edges of two semiconductors is very large, a band discontinuity occurs in addition to the band bending. These band discontinuities are the reasons of the energy band differences ΔE_C and ΔE_V for conduction and valence band of two semiconductors, respectively. ΔE_C is expressed according to Anderson's electron affinity as [17]:

$$\Delta E_C = q\chi_1 - q\chi_2 \quad (2)$$

where $q\chi_1$ and $q\chi_2$ are electron affinities of two semiconductors. However, a more general approach on ΔE_C is required since the electric displacement (\vec{D}) at the junction is not continuous due to the presence of dipoles or charges trapped at the interface thus ΔE_C is given by [18]

$$\Delta E_C = q\chi_1 - q\chi_2 + \delta_{dip} \quad (3)$$

where δ_{dip} is dipole potential at the interface.

1.1.2. Current Characteristics of a Heterojunction

Current density (J) passing through a p-n junction is the sum of two different currents

$$J = J_{diff} + J_{drift} \quad (4)$$

where J_{diff} is the diffusion current originated from particle exchange due to the difference in some charge carriers between p-type and n-type semiconductors. J_{drift} is created by the movement of the charge carriers yet to be \vec{D} Current density (J)-applied bias (V) characteristics of an ideal p-n homojunction diode is given by the following relation:

$$J = J_o \left[\exp \left(\frac{qV}{k_B T} \right) - 1 \right] \quad (5)$$

where k_B is the Boltzmann constant, T is temperature, V is applied DC bias, and J_o is saturation current density. J in the relation (4) is an idealization which assumes that electrical field across the interface between two semiconductors is continuous and the junction between them is abrupt. A fitting parameter η modifies relation (5); also known as diode ideality factor, which bears the effect of non-idealities such as discontinuous \vec{D} at interface of a p-n junction. Such non-uniformities are originated from the interface dipoles or charges trapped interface. A more general model for J is given as

$$J = J_o \left[\exp \left(\frac{qV}{\eta k_B T} \right) - 1 \right] \quad (6)$$

which is valid for metal – semiconductor and semiconductor- semiconductor junctions. In the case of J_{diff} is the dominant term in equation 2, η is ~ 1 (ideally $\eta = 1$). When $J_{\text{diff}} \sim J_{\text{drift}}$, $\eta = 2$. At high V values, $\eta > 2$ due to series resistance (R_s). Another reason for the η being larger than 2 is the case when there is a high-level injection of minority carriers into the diode. Most of the experimental results in the absence of the high-level injection can be modeled as in forward bias by neglecting generation-recombination current densities [15].

In general, different magnitudes of band discontinuities and barrier heights at carrier bands (Figure 2) in heterojunctions result in domination of total current by a single type of carrier (holes or electrons). Thermionic emission theory of a metal-semiconductor junction can be used for modeling anisotype heterojunction. J through an anisotropic heterojunction is given by [16]

$$J = J_{01} \exp\left(\frac{-q\phi'_1}{k_B T}\right) - J_{02} \exp\left(\frac{-q\phi'_2}{k_B T}\right) \quad (7)$$

where ϕ'_1 and ϕ'_2 are barrier heights under applied DC bias, J_{01} and J_{02} are reverse saturation currents of semiconductor-1 and semiconductor-2, respectively. J_{01} and J_{02} are determined by three different parameter: i) doping densities of semiconductor-1 and semiconductor-2, ii) electronic conduction mechanism, and iii) effective mass of the charge carriers in the semiconductor materials [19]. It is clearly seen from relation (6) that two potential barriers determine the carrier transport. Anisotype heterojunction depicted in figure 2(b), which is not yet to be applied any external potential difference (V), an electron in CB of semiconductor-1 experiences a barrier of $q\phi_1$. Similarly, a hole in VB of semiconductor-2 experiences barrier of $\Delta E_v - q\phi_2$. As soon as thermodynamic equilibrium is established, the net current J must be zero. In that case, J_{01} and J_{02} can be related using relation (6) [19]

$$J_{01} \exp \left[\frac{-q\phi_1}{k_B T} \right] = J_{02} \exp \left[\frac{-(\Delta E_V - q\phi_2)}{k_B T} \right] \quad (8)$$

and J_{02} is

$$J_{02} = J_{01} \exp \left[\frac{-q\phi_1}{k_B T} \right] \exp \left[-\frac{(q\phi_2 + q\phi_1 - \Delta E_V)}{k_B T} \right] \quad (9)$$

By putting (8) into (6) current density (J) can be expressed as

$$J = J_{01} \exp \left(\frac{-q\phi_1}{k_B T} \right) \left[\exp \left(\frac{-q(\phi'_1 - \phi_1)}{k_B T} \right) - \exp \left(\frac{\Delta E_V - q\phi'_2 - q\phi_2}{k_B T} \right) \right] \quad (10)$$

or

$$J = J_{01} \exp \left(\frac{-q\phi_1}{k_B T} \right) \left[\exp \left(\frac{q\phi_{S1}}{k_B T} \right) - \exp \left(\frac{-q\phi_{S2}}{k_B T} \right) \right] \quad (11)$$

ϕ_{S1} and ϕ_{S2} are the potentials of neutral regions of semiconductor-1 and semiconductor-2, respectively. By the fact that electric \vec{D} is continuous at an abrupt junction, a solution of Poisons' equation gives

$$N_1 \varepsilon_1 (\phi_1 - \phi_{S1}) = N_2 \varepsilon_2 (\phi_2 - \phi_{S2}) \quad (12)$$

where N_1 and N_2 are the doping densities, ε_1 and ε_2 dielectric constants of semiconductor-1 and semiconductor-2, respectively [19]. Putting relation (11) into (10) the following relation is obtained:

$$J = J_{01} \exp\left(\frac{-q\phi_1}{k_B T}\right) \left\{ \exp\left[\frac{qV}{mk_B T}\right] - \exp\left[\frac{-q(m-1)V}{mk_B T}\right] \right\} \quad (13)$$

where m is given by

$$m = 1 + \frac{N_1 \varepsilon_1}{N_2 \varepsilon_2} \quad (14)$$

Unless a heterojunction is driven into high injection condition, J is limited by the diffusion rate of electrons from semiconductor-1 to semiconductor-2. Therefore, J_{01} is equal to J_{diff} of electrons according to the following relation

$$J_{01} = XqN_1 \frac{D_n}{L_n} \quad (15)$$

where N_1 is the acceptor density, D_n and L_n are the electron diffusivity and electron diffusion length, respectively. Parameter X is the probability of an electron which has enough energy to cross the potential barrier at the junction to succeed to transport through to the semiconductor-2 from the semiconductor-1.

An isotype and an anisotype heterojunctions differ from each other by carrier transport mechanism at low injection levels. In general, $\phi_{b1} - \phi_{s1} \gg \phi_{b2} - \phi_{s2}$ hence the isotype heterojunction behaves like semiconductor – metal junction[20]. Therefore, J is governed by the thermionic emission of electrons which is given by the Richardson–Dushman equation as [21]

$$J_{Th} = A_T (k_B T)^2 \exp\left(-\frac{q\phi_b}{k_B T}\right) \quad (16)$$

where ϕ_b is the height of the potential barrier which electrons have to overcome to be emitted while A_T is given by

$$A_T = \frac{em_e}{2\pi^2\hbar^3} \quad (17)$$

where e , m_e and, \hbar are the fundamental electronic charge, effective mass of electron in the material in which emission takes place, and reduced Planck constant, respectively. In thermionic emission theory, it is assumed that an electron with energy greater than $q\phi_b$ which is heading towards barrier region is just transported. J_{Th} of n-n isotype heterojunction (Figure 2(b)) is given by [22]

$$J = J_0 \left(1 - \frac{V}{\phi_{bi}}\right) \left[\exp\left(\frac{qV}{k_B T}\right) - 1 \right] \quad (18)$$

where reverse saturation current is

$$J_0 = q^2 N_{D1} \phi_{bi} (2\pi m_e k_B T)^{-\frac{1}{2}} \left[\exp\left(\frac{q\phi_{bi}}{k_B T}\right) \right] \quad (19)$$

N_{D1} is the donor concentration on the semiconductor-1. However, thermionic emission model is not sufficient at high voltages and doping levels. The barrier heights and shapes in the Figure 2, quantum mechanical tunneling current mechanism must be considered.

Time independent solution of the Schrödinger equation for a particle under a potential in 3 dimensions is expressed as:

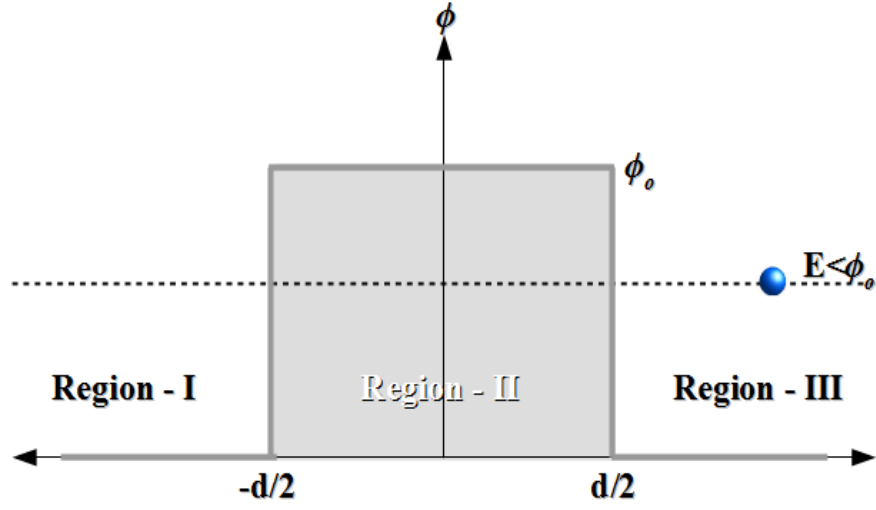


Figure 3. A step function for a particle with an energy less then barrier height

$$\frac{\hbar}{2m} \nabla^2 \psi(r) + \phi_o \psi(r) = E \psi(r) \quad (20)$$

Where $\psi(\mathbf{r})$ and ϕ_o are state function and potential that particle experienced, respectively. When a particle experiences a step potential barrier, as shown in figure 3, solution of the Schrödinger equation is obtained by considering suitable boundary conditions in one dimension as following[23]:

$$\psi(x) = \begin{cases} Ae^{ikx} + Be^{-ikx} & ; \quad x < -\frac{d}{2} \\ Ce^{ikx} + De^{-ikx} & ; \quad -\frac{d}{2} < x < \frac{d}{2} \\ Fe^{ikx} & ; \quad x > \frac{d}{2} \end{cases} \quad (21)$$

A, B, C, D , and F are constants in the solution of the Schrödinger's equation in three different regions in spatial extent and d is the thickness of the barrier. Wave vector where the potential is zero is k , and similarly, κ is the wave vector where the particle is yet to be experienced potential which are given by:

$$k = \left(\frac{2mE}{\hbar^2} \right)^{1/2} \text{ and } \kappa = \left(\frac{2m(\phi_o - E)}{\hbar^2} \right)^{1/2} \quad (22)$$

coefficient A in the (21) is related to the amplitude of the wave coming from region-III. After knowing A , other coefficients can be determined. Likely, A can be determined for a physical system by sending a current of particles which amplitude can be determined easily, i.e., changing the working power of a hot filament emitting electrons through a potential barrier. By knowing the coefficient F , amplitude of wave transmitted wave can be determined so that transmission T probability can be determined according to the following relation:

$$T = \frac{|F|^2}{|A|^2} = \left[1 + \frac{\phi_o^2}{4E(\phi_o - E)} \sinh^2 \left(\frac{d\sqrt{2m(\phi_o - E)}}{\hbar} \right) \right]^{-1} \quad (23)$$

By defining a function such that

$$\Gamma(d, \phi_o, E) = \frac{\phi_o^2}{4E(\phi_o - E)} \sinh^2 \left(\frac{d\sqrt{2m(\phi_o - E)}}{\hbar} \right) \quad (24)$$

By using relation (23), relation (22) is simplified as

$$T = \frac{1}{1 + \Gamma(d, \phi_o, E)} \quad (25)$$

Physical picture which is emerging from the equation (24) is highly idealized, indeed, most of the physical system has no well-defined potential barrier like that. However complex potential barriers similar to the ones in Figure 4 can be approximated as collections of infinitesimally thin rectangular potential barriers.

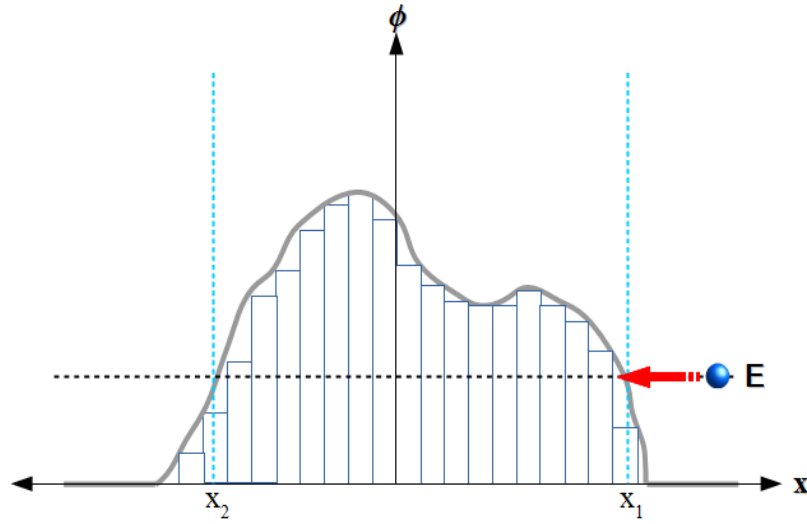


Figure 4. A generic potential barrier approximated as infinitesimal rectangular potential barriers.

For the infinitesimal i^{th} barrier with length dx equation (24) becomes

$$\begin{aligned} \Gamma_i(dx, \phi_o, E) &= \frac{\phi_o^2}{4E(\phi_o - E)} \sinh^2 \left(\frac{dx \sqrt{2m(\phi_o - E)}}{\hbar} \right) \\ &= \frac{\phi_o^2}{4E(\phi_o - E)} \sinh^2(\alpha) \end{aligned} \quad (26)$$

Expanding the hyperbolic term in power series and neglecting the higher order terms in (25) gives:

$$\Gamma_i(d, \phi_o, E) = \frac{\phi_o^2}{4E(\phi_o - E)} \frac{2m(\phi_o - E)(dx)^2}{6\hbar^2} \quad (27)$$

Probability of the particle to be tunneled from x_1 to x_2 is given by

$$T = \prod_i T_i \approx e^{-\frac{2\sqrt{2m}}{\hbar} \int_{x_1}^{x_2} \sqrt{(\phi_o - E)} dx} \quad (28)$$

When the energy of a particle is smaller than the potential barrier edge at both side of the barrier, tunneling process is called direct tunneling. A thin layer of dielectric material can be considered as a rectangular potential barrier when charge carriers incident on it. When a linear dielectric experiences an external electric field (\vec{F}) or charges are embedded in the dielectric, the potential at either sides of the dielectric changes. The potential at a point on the dielectric can be obtained after some basic electrostatic analysis as follows:

$$\phi(x) = \phi_b - qF \quad (29)$$

This potential drop transforms the rectangular potential barrier into trapezoidal potential barrier in the Figure 5. Putting the relation (28) into relation (27) gives:

$$T_{direct} = e^{-\frac{4\sqrt{2m}}{3q\hbar E} [(\phi_o - E)^{3/2} - (\phi_o - E - qdF)^{3/2}]} \quad (30)$$

If a current density J_o flows through a dielectric potential barrier such as the barrier in Figure 5 and the average energy of the electron is less than both ϕ_a and ϕ_b , a current

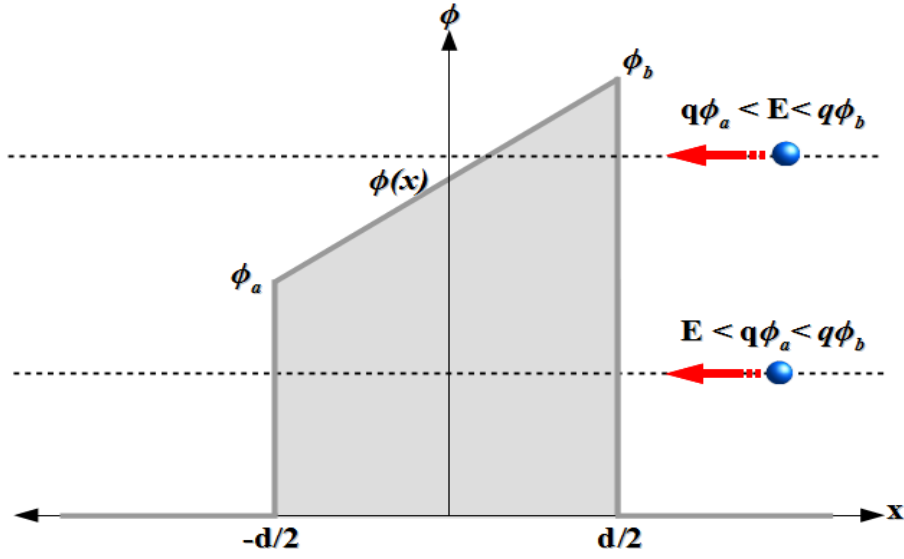


Figure 5. Direct and Fowler-Nordheim tunneling through barrier

density J is measured at the other side of the barrier. The direct tunneling probability is given by:

$$T_{direct} = \frac{J}{J_o} \quad (31)$$

Therefore, direct tunneling current density J_{direct} is given by

$$J_{direct} = J_o e^{-\frac{4\sqrt{2m}}{3q\hbar E}[(\phi_o - E)^{3/2} - (\phi_o - E - qdF)^{3/2}]} \quad (32)$$

When the tunneling occurs through a triangular (Figure-5), it is called Fowler – Nordheim tunneling. In this case equation (30) becomes by Wentzel-Kramers-Brillouin (WKB) approximation as:

$$J_{FN} = J_o e^{-\frac{4\sqrt{2m}}{3q\hbar E}(\phi_o - E)^{3/2}} \quad (33)$$

1.1.3. Capacitance of a Heterojunction

A parallel plate capacitor (PPC) is a device which consists of a dielectric material sandwiched between two conducting plates as shown in Figure 6.

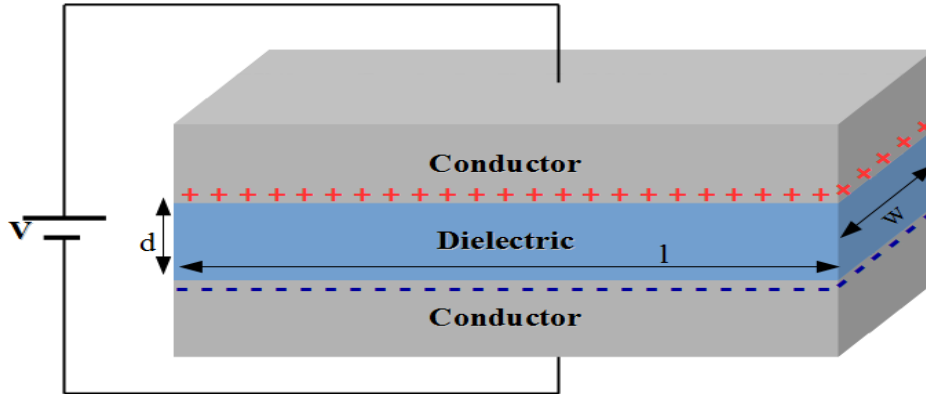


Figure 6. Schematic diagram of a parallel plate capacitor

Capacitance is an electrical response when a potential difference applied across a material as shown in Figure 6. When a potential difference between the conductor plates is applied, charges with different polarities yet with the same number accumulate on the opposite sides of the dielectric material. Capacitance of a PPC is given by

$$C = \frac{Q}{V} \quad (34)$$

By solving Poisson's equation at the boundaries, capacitance of PPC can be found as

$$C = \kappa \epsilon_0 \frac{A}{d} \quad (35)$$

where κ is the relative dielectric constant, d is the thickness dielectric material, and A is the area of dielectric – conductor interface ($A = l \times w$ in Figure 6).

When potential difference between the two conductors is originated from a small amplitude time-varying \vec{E} then the capacitance of the PPC is considered as differential capacitance given by

$$C = \frac{dQ}{dV} \quad (36)$$

A semiconductor p-n junction can be modeled as two PPC with depletion approximation. Depletion approximation is based on the assumption that space charge region, d_1 and d_2 as shown in Figure 7, is free from mobile charge carriers. Only fixed charges exist due to the presence of fixed charges, i.e., dopant atoms (N_A^- and N_D^+). The neutral region of semiconductor and interface at semiconductor-1 and semiconductor-2 abrupt junction is considered as two conductors and space charge region(SCR)-1 as a dielectric layer. Indeed, similar arguments hold for SCR-2. Hence, total capacitance of the space charge region is

$$C_{SC} = \frac{C_1 + C_2}{C_1 C_2} \quad (37)$$

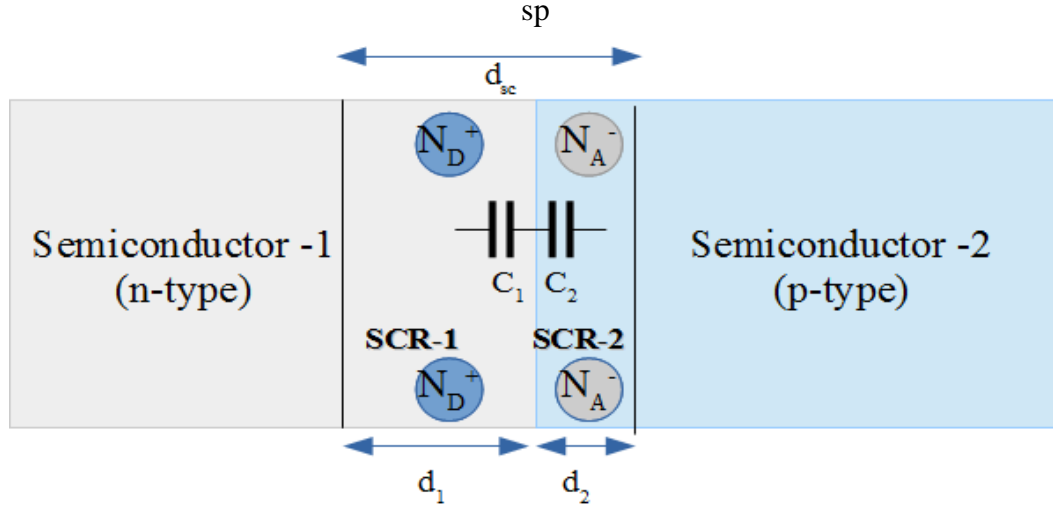


Figure 7. Space –charge region of an isotype heterojunction.

where C_1 and C_2 are the capacitance of SCR-1 and SCR-2 and C_{sc} is the total capacitance of space charge region. As mentioned in section 1.1.2, electrostatic boundary conditions require \vec{D} to be continuous at the junction according to the following expression:

$$\varepsilon_1 \vec{D}_1 = \varepsilon_2 \vec{D}_2 \quad (38)$$

where $\varepsilon_1 = \kappa_1 \varepsilon_0$ and $\varepsilon_2 = \kappa_2 \varepsilon_0$ are the dielectric constant, \vec{D}_1 and \vec{D}_2 are the electric displacement in semiconductor-1 and semiconductor-2, respectively. ϕ_{b1} and ϕ_{b2} can be found by solving Poisson's equation with boundary condition presented in relation (38) with assumption of an abrupt junction for an anisotype heterojunction (Figure 7) as:

$$\phi_{b1} = \frac{\varepsilon_2 N_A (\phi_{bi} - V)}{\varepsilon_1 N_D + \varepsilon_2 N_A} \quad (39)$$

and

$$\phi_{b2} = \frac{\varepsilon_1 N_D (\phi_{bi} - V)}{\varepsilon_1 N_D + \varepsilon_2 N_A} \quad (40)$$

Portion of the space charge regions in Semiconductor-1 and Semiconductor-2 are

$$d_1 = \left[\frac{2\varepsilon_1 \varepsilon_2 N_A (\phi_{bi} - V)}{q N_A (\varepsilon_1 N_D + \varepsilon_2 N_A)} \right]^{\frac{1}{2}} \quad (41)$$

and

$$d_2 = \left[\frac{2\varepsilon_1 \varepsilon_2 N_d (\phi_{bi} - V)}{q N_A (\varepsilon_1 N_D + \varepsilon_2 N_A)} \right]^{\frac{1}{2}} \quad (42)$$

Total thickness of the space charge region ($d = d_1 + d_2$) becomes

$$d = \left[\left(\frac{N_D}{N_A} \right)^{\frac{1}{2}} + \left(\frac{N_A}{N_D} \right)^{\frac{1}{2}} \right] \left[\frac{2\varepsilon_1 \varepsilon_2 (\phi_{bi} - V)}{q (\varepsilon_1 N_D + \varepsilon_2 N_A)} \right]^{\frac{1}{2}} \quad (43)$$

Putting equations relations (41) and (42) into relation (37) gives:

$$C_{sc} = \left[\frac{q N_A N_D \varepsilon_1 \varepsilon_2}{2 (\varepsilon_1 N_D + \varepsilon_2 N_A) (\phi_{bi} - V)} \right]^{\frac{1}{2}} \quad (44)$$

Potential distribution of an isotype heterojunction due to large band discontinuities

Potential distribution can be obtained by the fact that continuity of \vec{D} holds for the isotype heterojunction [19]

$$\frac{\varepsilon_2 N_2}{\varepsilon_1 N_1} = \frac{\exp\left(\frac{q(\phi_{b1} - V_1)}{k_B T}\right) - \frac{q(\phi_{b1} - V_1)}{k_B T} - 1}{\exp\left(-\frac{q(\phi_{b2} - V_2)}{k_B T}\right) + \frac{q(\phi_{b2} - V_2)}{k_B T} - 1} \quad (45)$$

and C_{SC} is

$$C_{SC} = \left\{ \frac{q \varepsilon_2 N_2 \left[1 - \frac{k_B T}{q} \left((\phi_{bi} - V) - (\phi_{b1} - V_1) \left(1 - \frac{\varepsilon_1 N_1}{\varepsilon_2 N_2} \right) \right)^{-1} \right]}{2(\phi_{b2} - V_2) - k_B T} \right\}^{\frac{1}{2}} \quad (46)$$

When a heterojunction is under forward bias, majority carriers are injected from one semiconductor region to the other, i.e., electrons from semiconductor-1 to semiconductor-2 (Figure 7). After crossing the junction, injected minority carrier recombines with majority carrier. This movement of carriers results in a current density flow and change in charge storage in neutral regions of the heterojunction. Total electronic charge in semiconductor-2 in a cross-sectional area (A) due to injections of electrons from the semiconductor-1 is given by [15]:

$$Q_n = A \frac{L_n^2}{D_n} J_n(x_p) = \tau_n A J_n(x_p) \quad (47)$$

Similarly, the total charge in the semiconductor due to the injection of holes is given by:

$$Q_p = A \frac{L_p^2}{D_p} J_p(x_n) = \tau_p A J_p(x_n) \quad (48)$$

where n and p stand for electron and holes in n-region and p-region, relatively, and τ is the average minority carrier life time. $J_n(x_p)$ and $J_p(x_n)$ are diffusion current densities in neutral regions of the semiconductor concerning edges of the space charge region. Using relation (6) diffusion capacitance C_d can be found as

$$C_d = A \left[\frac{L_n^2}{D_n} \frac{dJ_n(x_p)}{dV} + \frac{L_p^2}{D_p} \frac{dJ_p(x_n)}{dV} \right] = A \left[\tau_n \frac{dJ_n(x_p)}{dV} + \tau_p \frac{dJ_p(x_n)}{dV} \right] \quad (49)$$

By the fact that current is dominated by a single type charge carrier in an isotype heterojunction, one of the terms in relation (48) can be ignored depending on the type of majority carriers. The second term on the right side of relation (48) can be neglected for n-n type heterojunction. Furthermore, C_d of an n-n isotype heterojunction can be found by inserting relation (18) into relation (48)

$$C_d = \frac{AXq^2 N_1 L_n}{mk_B T} \exp\left(\frac{-q\phi_1}{k_B T}\right) \left\{ \exp\left[\frac{qV}{mk_B T}\right] + (m-1) \exp\left[\frac{-q(m-1)V}{mk_B T}\right] \right\} \quad (50)$$

1.1.4. Differential Conductance of a Heterojunction

The conductance of a material is just the inverse of its resistance. It is a measure how easily a current density flows through a cross sectional area (A) of a material. In case of small potential excitation, differential conductance is given by

$$G = A \frac{dJ}{dV} \quad (51)$$

Conductance of the anisotype heterojunction in Figure 2(b) is obtained by putting relation (12) into relation (50)

$$G = \frac{Aq^2 J_{01}}{mk_B T} \exp\left(\frac{-q\phi_1}{k_B T}\right) \left\{ \exp\left[\frac{qV}{mk_B T}\right] + (m-1) \exp\left[\frac{-q(m-1)V}{mk_B T}\right] \right\} \quad (52)$$

Solution for n-n isotype semiconductor is given as:

$$G = \frac{AXq^2 N_1 D_n}{mk_B T L_n} \exp\left(\frac{-q\phi_1}{k_B T}\right) \left\{ \exp\left[\frac{qV}{mk_B T}\right] + (m-1) \exp\left[\frac{-q(m-1)V}{mk_B T}\right] \right\} \quad (53)$$

It is clear that there exists a relation between relation (49) and relation (52) such that

$$C_D = \tau_n G \quad (54)$$

for an n-n isotype heterojunction. Similarly, for a p-p isotype heterojunction

$$C_D = \tau_p G \quad (55)$$

1.2. Metal – Oxide – Semiconductor Capacitors

A Metal - oxide - semiconductor (MOS) capacitor is a device which importance lays on the fact that it holds a base for very large circuit integration (VLSI) and it is an easy way of studying semiconductor - oxide interface. A typical MOS capacitor is shown in Figure 8 which consists of an oxide layer deposited on a semiconductor and metal contacts deposited over the semiconductor and the oxide layer.

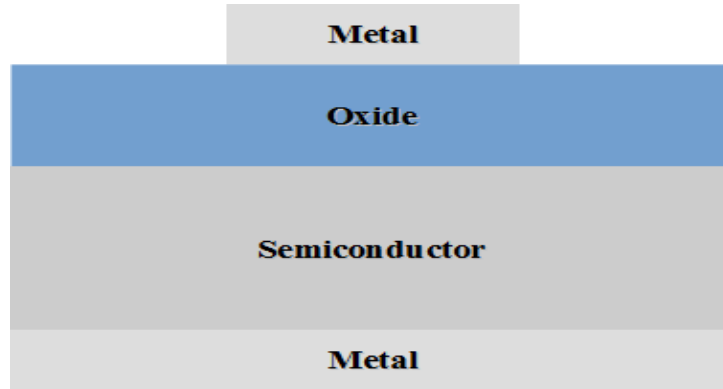


Figure 8. A schematic of a typical MOS capacitor

A MOS capacitor differs from a semiconductor junction in two ways; i) space charge region presents just below the oxide – semiconductor interface in semiconductor, ii) total charge neutrality holds for the p-n junction and not for the MOS capacitor. Band diagram for an ideal (defect free abrupt oxide – semiconductor interface and oxide bulk) MOS with n-type semiconductor (n –type MOS) capacitor at equilibrium is depicted in Figure 9. Once a MOS capacitor is in equilibrium, fermi levels of metal ϕ_m and that of the semiconductor ϕ_s line up. If $\phi_m \neq \phi_s$ before thermal equilibrium is established, CB and VB of semiconductor bend towards equilibrium. Consequently, a potential across the oxide layer is formed which tilts conduction band of the oxide material. This potential is called flat band voltage (since it corresponds to deviation from flat carrier bands). If $\phi_m = \phi_s$ then $\phi_{FB} = 0$, all carrier bands are flat and there is no potential difference across the oxide layer assuming that there exist no charges at oxide – semiconductor interface and within the oxide layer.

1.2.1. Equilibrium Under Applied External Potential Difference

Distribution of charge carriers in an ideal MOS capacitor highly depends on the external field. Charge distribution changes towards to thermodynamic equilibrium after time-independent potential (V) applied. Four different equilibrium

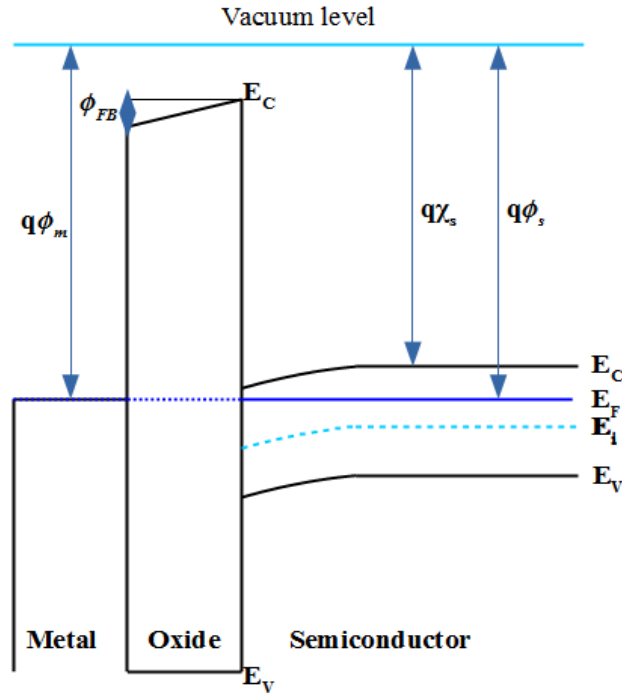


Figure 9. Band diagram of an ideal MOS capacitor at equilibrium without any external applied potential difference

configurations for charge distribution exist depending on magnitude and polarity of V ; accumulation, depletion, flat band, and inversion.

When positive V (with respect the metal contact on the oxide layer, conventionally) $> \phi_{FB}$ is applied, as shown in Figure 10, $q\phi_m$ increases. After the equilibrium is established, E_F exceeds CB edge of the semiconductor near the interface. Electrons in the semiconductor accumulate beneath the oxide – semiconductor surface. Electrons on the top metal contact are repelled away from the oxide layer in the influence of electrostatic potential. This physical picture of MOS capacitor is called accumulation condition or regime. The oxide layer can be considered as a PPC in the accumulation regime. Oxide capacitance C_{ox} according to PPC model is given by:

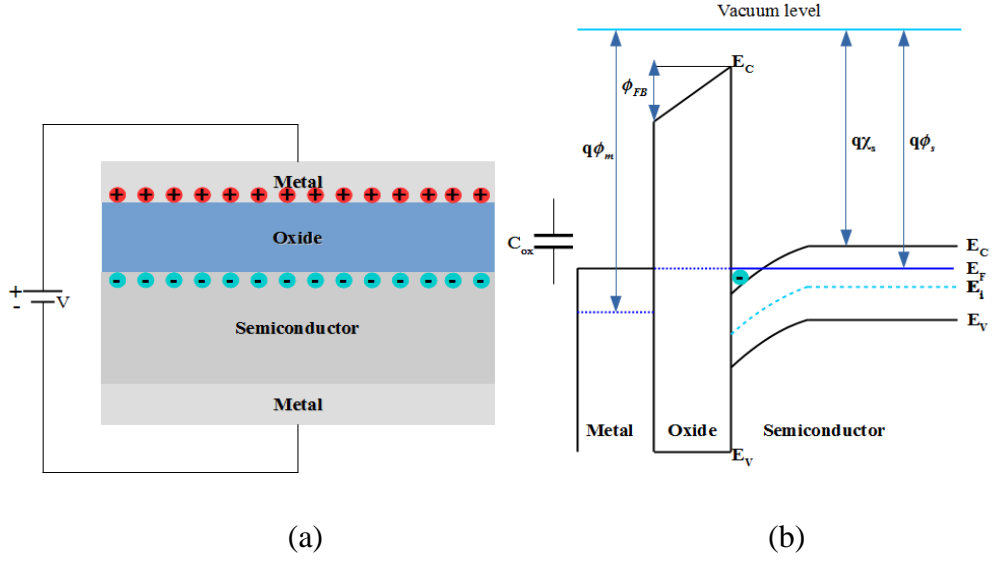


Figure 10. MOS capacitor at accumulation condtion (a) charge distribution over MOS capacitor, (b) band diagram

$$C_{ox} = \kappa_{ox} \epsilon_o \frac{A}{d_{ox}} \quad (56)$$

where the ox stands for that quantity, belong oxide material.

If $V = \phi_{FB}$ then ϕ_m and ϕ_s align at the same level after equilibrium is established. The voltage drop across oxide layer is compensated by V . Therefore; all the bands become flat as shown in Figure 11. In that case, the semiconductor is neutral. The ϕ_{FB} depends on the difference between the ϕ_m and ϕ_s such that

$$\phi_{FB} = \phi_m - \phi_s = \phi_{ms} \quad (57)$$

Work function difference between metal and semiconductor $q\phi_{ms}$ is given by[15]

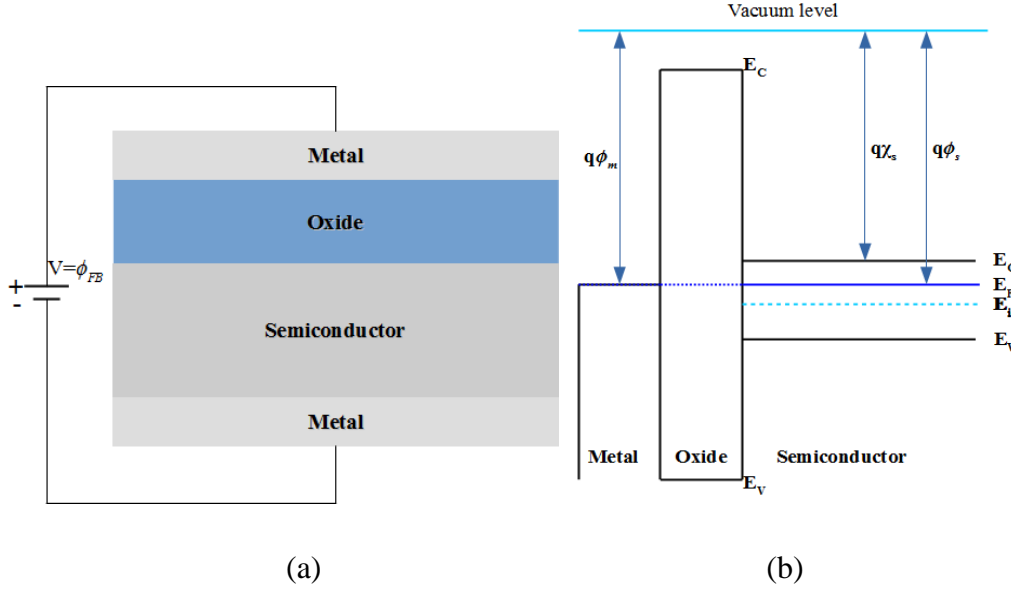


Figure 11. MOS capacitor at flat band condition (a) charge distribution over MOS capacitor, (b) band diagram

$$q\phi_{ms} = q\phi_m - q\phi_s = q\phi_m - \left(q\chi_s + \frac{E_G}{2} - q\phi_B \right) \quad (58)$$

Where E_g is band gap of the semiconductor and $q\phi_B = E_F - E_i$ is the difference between intrinsic Fermi energy (E_i) and actual Fermi energy (E_F) of the semiconductor.

Once negative V is applied, ϕ_m is lifted up since electrons are injected into metal. Conduction electrons beneath the oxide - semiconductor interface are depleted under the influence of electrostatic potential. A space charge region is created under the interface as shown in Figure12. This condition is usually termed as depletion condition. Charge density exists only on space charge region due to fixed charges inside the semiconductor. Hence, space charge region capacitance C_{SC} can modeled as PPC and given by

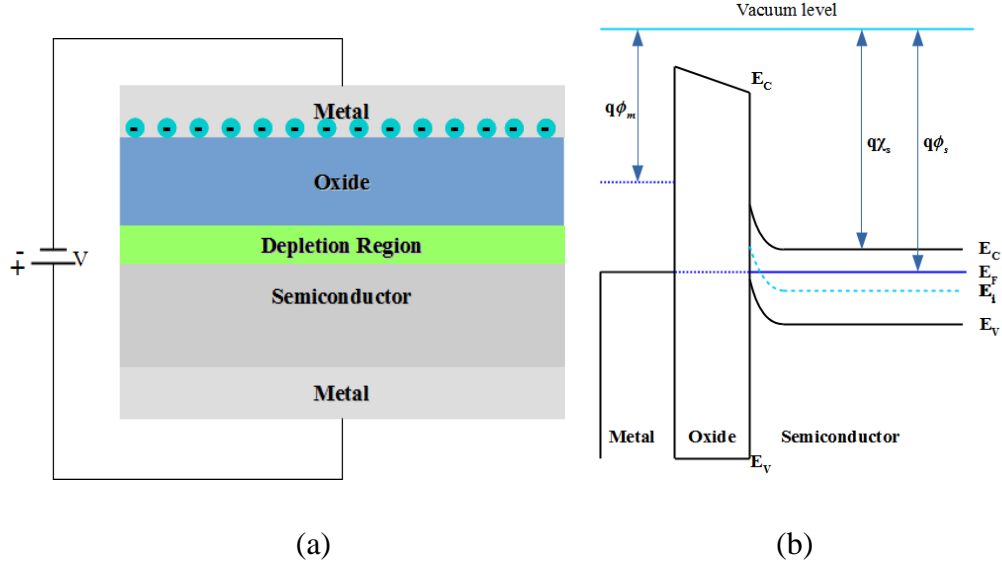


Figure 12. MOS capacitor at depletion condition (a) charge distribution over MOS capacitor, (b) band diagram

$$C_{SC} = \kappa_s \epsilon_0 \frac{A}{w} \quad (59)$$

Solution of Poisson's equation for a potential generic $\psi(x)$ under the interface through the semiconductor at a distance x gives surface potential of the semiconductor ψ_{sur} since $\psi(x)$ is constant at by the definition it can be set as zero[15]

$$\psi_{sur} = \frac{qN_D w_{sc}^2}{2\kappa_s \epsilon_0} \quad (60)$$

where w_{sc} is the thickness of space charge region, and κ_s is the relative dielectric constant of the semiconductor. When $V \ll 0$, a positively-charged inversion layer is formed due to the presence of high \vec{E} at the semiconductor surface as depicted in Figure 13.

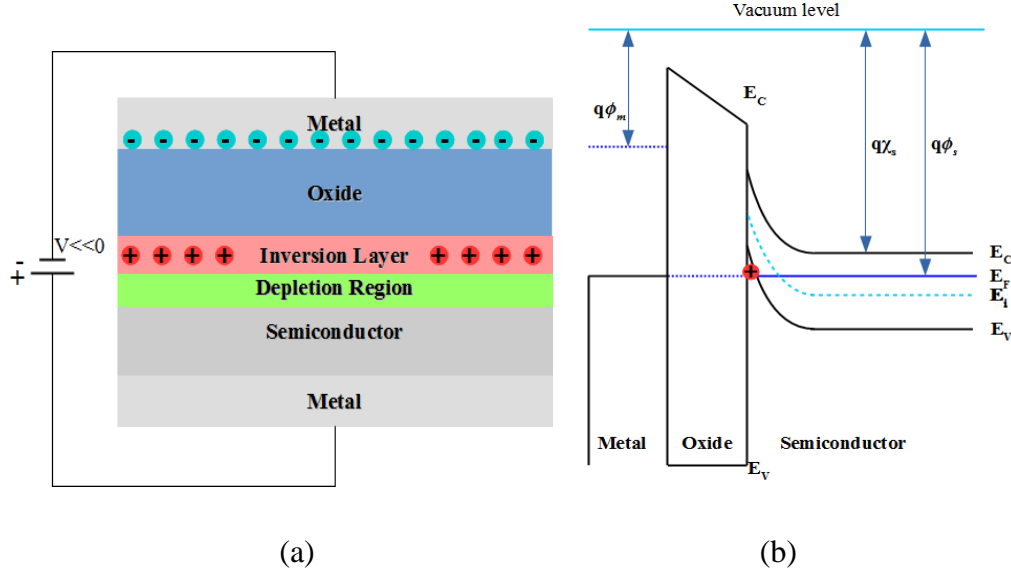


Figure 13. MOS capacitor at inversion condition (a) charge distribution over MOS capacitor, (b) band diagram

Without a doubt, the total charge is present in space charge region due to the depleted fixed atoms and inverted layer under the strong inversion condition. Condition for surface inversion is given by[15]

$$\psi_{sur}^{inv} \cong 2\phi_B = \frac{2k_B T}{q} \ln\left(\frac{N_D}{n_i}\right) \quad (61)$$

where n_i is the intrinsic carrier concentration of the semiconductor and *inv* stands for inversion. Once space charge region extends its maximum thickness, strong inversion is formed. Maximum length of space charge region w_{max} is given by:

$$w_{max} = \left(\frac{2\kappa_s \epsilon_0 \psi_{sur}^{inv}}{q N_D}\right)^{\frac{1}{2}} \cong \left(\frac{4\kappa_s \epsilon_0 \phi_B}{q N_D}\right)^{\frac{1}{2}} \quad (62)$$

The condition for applied potential difference to achieve strong inversion defined as a threshold voltage ϕ_T is in which w_{SC} reaches its maximum. ϕ_T is given as

$$\phi_T = \psi_{sur}^{inv} + \frac{qN_D w_{max}}{C_{ox}} \cong \left(\frac{4qN_D \phi_B}{C_{ox}^2} \right)^{\frac{1}{2}} + 2\phi_B \quad (63)$$

The capacitance of the MOS capacitor has a minimum value due to the threshold. A depleted MOS capacitor whose surface is not yet to be inverted can be considered as two capacitors (C_{ox} and C_{SC}) in series so that capacitance of the MOS capacitor is

$$C_{min} = \frac{C_{ox} C_{SC}}{C_{ox} + C_{SC}} = \frac{\kappa_{ox} \epsilon_0 A}{d_{ox} + \frac{\kappa_{ox}}{\kappa_s} w_{max}} \quad (64)$$

where C_{min} is the minimum capacitance value that the MOS capacitor has.

1.2.2. Charges Trapped at Interface and Inside Oxide Layer

Ideal MOS capacitor is discussed in previous section; ignoring interface effects such as emission and capture of charge carriers and presence of any charge within the oxide layer. However, a MOS capacitor always contains electronic states at the oxide and the semiconductor interfaces. Discontinuity of crystal structure at the surface causes unpaired electrons (dangling bonds). Electronic states at the oxide – semiconductor interface are mostly originated from the unpaired electrons [24]. Figure 14 illustrates electronic states that present at the interface. These states are called as

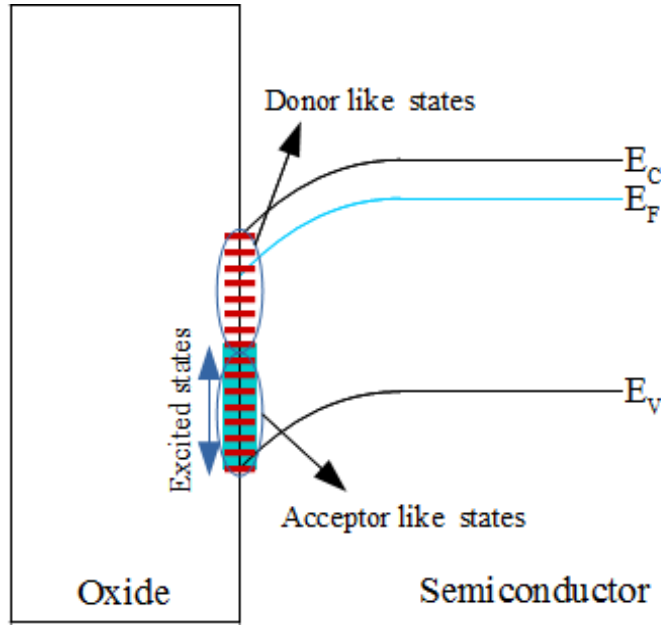


Figure 14. Oxide – semiconductor interface in the presence of interface trapped states

interface trapped states, and when a charge is trapped in that state, then it is termed as interface trapped charge (Q_{it}). Blue shaded area at the interface in Figure 14 represents excited trap states with applied potential difference to MOS capacitor. Trap states with energy level lower than semiconductor midgap ($\sim E_i$) exhibit acceptor-like behavior while trap states with energy level greater than midgap exhibit like donor type behavior. Capacitance due to the interface trapped charges C_{it} is given by[25]

$$C_{it} = q^2 D_{it} \quad (65)$$

where D_{it} is the number of charges per unit area trapped at the interface.

Three different types of charges are trapped by oxide[26]. They are categorized as i) fixed oxide charges (Q_f) which are the charges originated from oxide fabrication process and have no electrical interaction with the semiconductor, ii) oxide trapped

charges (Q_{ot}) which are holes or electrons trapped in the oxide, iii) Mobile ionic charges (Q_m) which are mainly due to ionic impurities within the oxide[25].

When a potential difference V is applied across a MOS capacitor, potential drops across the interface and oxide layer. Consequently, ϕ_{FB} is not as same value as for an ideal MOS capacitor. ϕ_{FB} is given including effects of trapped charges by[25]

$$\phi_{FB} = \phi_{ms} - \frac{1}{C_{ox}} \left(Q_f + Q_{it} + \int_0^{d_{ox}} \frac{x}{d_{ox}} \rho_m(x) dx + \int_0^{d_{ox}} \frac{x}{d_{ox}} \rho_{ot}(x) dx \right) \quad (66)$$

where ρ_m and ρ_{ot} are charge distributions of mobile ionic and oxide trapped charges within the oxide layer. Effective number of charges in the oxide; N_{eff} , can be defined as

$$N_{eff} = \frac{1}{q} (Q_f + Q_m + Q_{ot}) \quad (67)$$

Thus relation (66) can be expressed as

$$\phi_{FB} = \phi_{ms} - \frac{q(D_{it} + N_{eff})}{C_{ox}} \quad (68)$$

1.2.3. Equivalent Circuit Models of MOS Capacitor.

A MOS capacitor can be modeled as series and parallel PPCs whether it is considered as an ideal or actual device. Circuit models for capacitance of a MOS capacitor under different equilibrium conditions are shown in Figure 15[25]. The most general form of

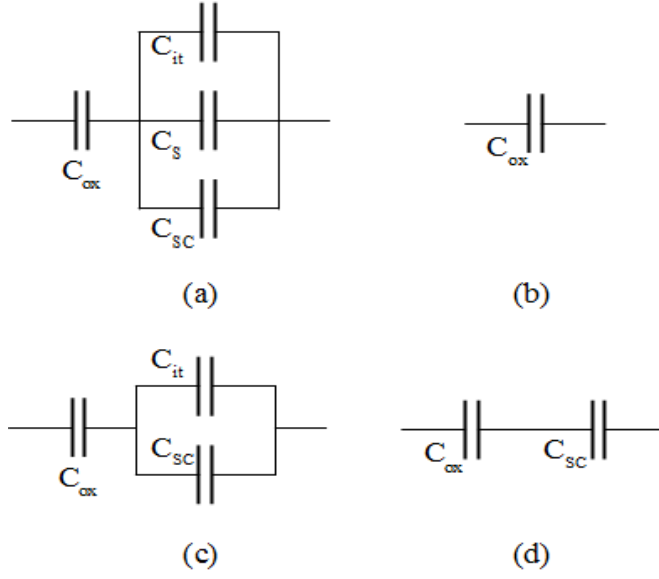


Figure 15. PPC circuit models for a MOS capacitor; (a) general form, (b) accumulation, (c) depletion, (d) inversion

the circuit model (Figure 15(a)) consist of 3 parallel capacitor which are due to; i) charges trapped interface (C_{it}), ii) carriers stored in bulk of the semiconductor (C_s), iii) fixed charges at space charge region (C_{sc}) and a capacitor in series due oxide capacitance (C_{ox}). Capacitance of a MOS capacitor is dominated by C_{ox} . Hence, C_{ox} is the capacitance of a MOS capacitor under accumulation condition (Figure 15(b)).

As soon as the semiconductor surface is not inverted, a MOS capacitor can be modelled as three component capacitive circuit as shown in Figure 15(c). C_{sc} can be considered as an variable capacitor whose capacitance depends on how far space charge region extends as a response of applied V . Once the surface inverted, C_{sc} is fixed. In that case a MOS capacitor is modelled as two capacitors in series (C_{ox} and C_{sc}). The most general form of a MOS capacitance based on Figure-15(a) is given as[25]

$$C = \frac{C_{ox}(C_{sc} + C_{it} + C_s)}{C_{ox} + C_{sc} + C_{it} + C_s} \quad (69)$$

1.2.4. Admittance of a MOS Capacitor

Circuit models in section 1.2.3 are only consideration of circuits comprising of capacitive elements. Circuits models including resistive elements are shown in Figure 16[25],[26].

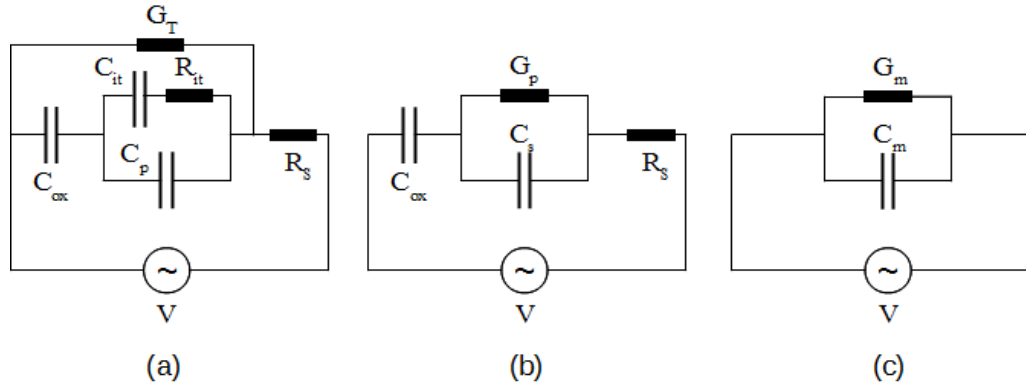


Figure 16. Equivalent circuits of a MOS capacitor; (a) exact, (b) simplified, and (c) measured

An exact circuit model is illustrated in Figure 16(a) where parallel capacitors in Figure 15 are collectively represented as C_p . Moreover, a resistive element R_{it} is included in order to represent potential loss due to the possible emission or capture of the carriers at the interface. Similarly, leakage current generated by tunneling of the charge carriers is considered as tunneling conductance G_T . A simplified version of exact circuit model is shown in Figure 16(b). C_p is reduced to C_s and the interface is represented by parallel conductance G_p . However, any measuring device is incapable of distinguishing all of these circuit components since they are hypothetical, rather a measured capacitance (C_m) and measured conductance (G_m) as in Figure-16(c). Admittance (Y) of the simplified circuit (Figure 16(b)) is given as[27]

$$Y_m = G_m + i\omega C_m \quad (70)$$

where $\omega = 2\pi f$ is the angular frequency of applied AC signal. Impedance (Z) of a circuit is just the inverse of Y

$$Z_m = \frac{1}{Y_m} = \frac{G_m}{G_m^2 + (\omega C_m)^2} - i \frac{\omega C_m}{G_m^2 + (\omega C_m)^2} \quad (71)$$

If Figure 16(b) is driven into strong accumulation condition ($V \gg 0$ for a n-type MOS capacitor) the circuit can be simplified to a circuit that R_s is in series with the circuit in Figure 15(b), in these conditions, Z of the circuit in Figure (16) is calculated by

$$Z_{ma} = R_s - \frac{1}{i\omega C_{ox}} \quad (72)$$

where *ma* stands for 'measured at accumulation.' R_s and C_{ox} can be related to C_{ma} and G_{ma} by matching imaginary and real parts of the right sides of relation (72) and relation (73) and R_s is found as

$$R_s = \frac{G_{ma}}{G_{ma}^2 + (\omega C_{ma})^2} \quad (73)$$

Similarly, C_{ox} is

$$C_{ox} = C_{ma} \left[1 + \left(\frac{G_{ma}}{\omega C_{ma}} \right)^2 \right] \quad (74)$$

R_s of a MOS capacitor is originating from many possible sources such as: i) resistance of the probe connections and rear contacts of the measurement system, ii) oxide or contaminations present on the rear contact plate of the measurement system and iii) material originated resistivities such as non-uniform doping profile under oxide – semiconductor junction and depletion layer edge.

If G_T is neglected from the circuit in Figure 16(a), Y of the circuit becomes as:

$$Y = \frac{\omega^2 R_{it} C_{it}^2}{1 + (\omega R_{it} C_{it})^2} + i\omega \left(C_s + \frac{C_{it}}{1 + (\omega R_{it} C_{it})^2} \right) - \frac{i}{\omega C_{ox}} \quad (75)$$

Y of the circuit in Figure 16(b) by neglecting R_s becomes

$$Y = G_p + i\omega C_p - \frac{i}{\omega C_{ox}} \quad (76)$$

If the two circuits are equivalent, G_p and C_p can be express by solving relations (75) and (76) together

$$G_p = \frac{\omega^2 R_{it} C_{it}^2}{1 + (\omega R_{it} C_{it})^2} \quad (77)$$

and

$$C_p = C_s \frac{C_{it}}{1 + (\omega R_{it} C_{it})^2} \quad (78)$$

An alternative expression for G_p is driven by reducing the circuit in Figure 16(a) to (c)[25]

$$G_p = \frac{\omega^2 G_m C_{ox}^2}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \quad (79)$$

1.2.5. High-Frequency Curve of a MOS Capacitor

Admittance measurement is performed by applying a small AC signal to a MOS capacitor which has been already subjected to DC bias. The purpose of giving an AC signal is to create small perturbation on the MOS capacitor which is in equilibrium with the DC signal so that charge carriers response under different conditions (i.e. under accumulation) can be examined. Charges in a MOS capacitor at low frequencies are in equilibrium with both AC and DC signals. They can follow the signal so that equilibrium is established. However, charges which are not in equilibrium at high frequency with the AC signal while equilibrium with the DC signal holds. Furthermore, an extreme condition exists such that charges are not in equilibrium with both AC and DC frequencies[28]. Hf C-V curves of an n-type MOS capacitor are shown in Figure 17. An ideal Hf C-V curve reaches its maximum value at accumulation and minimum value just after ϕ_{TH} (Figure 17(a)). The presence of oxide and interface trapped charges alter the C-V response of the MOS capacitor. When N_{eff} of oxide charges present within oxide layer, the C-V curve shifts parallel to the voltage axis relative to the polarity of N_{eff} (positive oxide charges causes to shift towards negative voltages while negative oxide charges moves the curve towards positive voltages)[29]. A positive shift due to negative N_{eff} is shown in Figure 17(b). As a result, a flat band voltage $\Delta\phi_{FB}$ occurs. On the other hand, D_{it} does not shift the C-V curve as much as N_{eff} does. Even though a small $\Delta\phi_{FB}$ can be observed since trapped charges respond a change due to changing the DC bias (ΔV), the major change in C-V curve reveals itself in depletion regime. The C-V curves stretch out over the voltage axis[15]. The amount of stretching depends on D_{it} and its energy distribution.

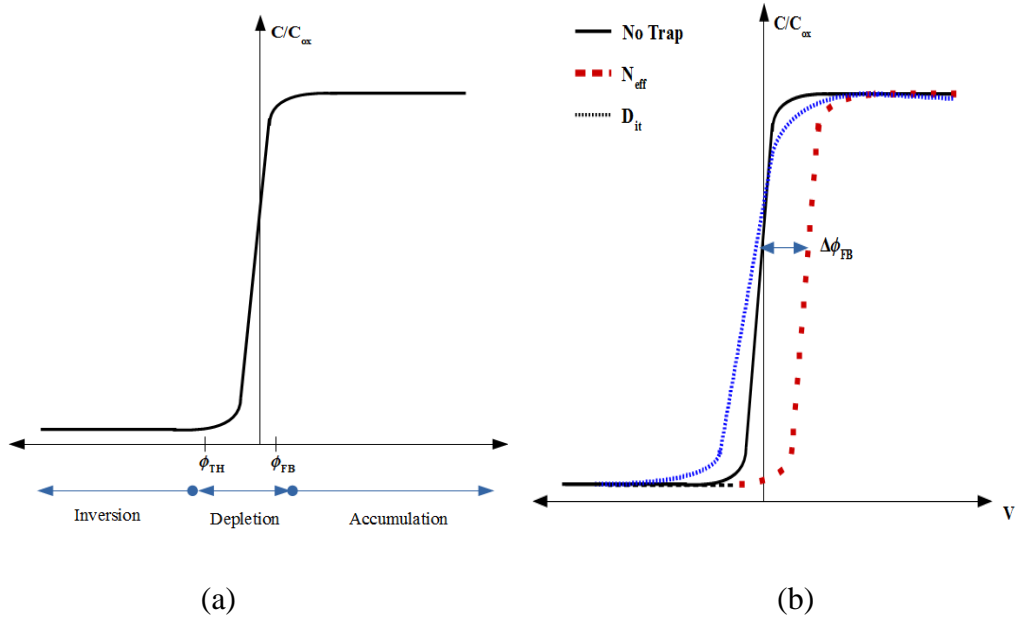


Figure 17. High frequency capacitance–voltage curves of an n–type MOS capacitor; (a) without traps charges, (b) with oxide charges and interface trapped charges.

1.2.6. The Conductance Method

An admittance measuring technique to determine D_{it} was suggested by Nicollian[30] et al. which is known as conductance method. Conductance method is widely used and trusted worthy owing to its high sensitivity in the range between CB edge and mid gap[25]. However, this method is ineffective to determine D_{it} with energy too close to mid-gap level[30]. G_p is related with trap level relaxation time constant ($\tau_{it} = R_{it}C_{it}$) and D_{it} whose relation can be obtained by combining relations (65) and (77).

$$\frac{G_p}{\omega} = \frac{q\omega D_{it}\tau_{it}}{1 + (\omega\tau_{it})^2} \quad (80)$$

and in terms of C_{ma} and G_{ma}

$$\frac{G_p}{\omega} = \frac{\omega G_m C_{ox}^2}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \quad (81)$$

Frequency dependence of G_p arises from τ_{it} which is the emission and capture rates at the oxide semiconductor interface and modeled by Shockley-Read-Hall statistics[31].

$$\tau_{it} = \frac{\exp\left(\frac{\Delta E}{k_B T}\right)}{\sigma_c \vartheta_{Th} D_{dos}} \quad (82)$$

where σ_c is the capture cross-section of the trap level at the oxide-semiconductor interface and ΔE is the difference between energy level of the trap state and the band edge; conduction band edge (E_{CB}) for n-type semiconductor and valence band edge (E_{VB}) for p-type semiconductor while $k_B T$ and ϑ_{th} are the average thermal energy and average thermal velocity of the majority carriers at T , respectively, and D_{dos} is the effective density of states at majority carrier band. Interface trap levels are assumed to be non-degenerate in this model[30]. Charge carriers are emitted or captured by the trap levels which are in very close proximity of E_f ($\sim k_B T$).

An approximate relation for D_{it} is given as[30]

$$D_{it} = \frac{2.5}{qA} \left(\frac{G_p}{\omega} \right)_{max} \quad (83)$$

where *max* stands for the value of G_p . In most of the cases, measured G_p curves at high frequencies is indistinguishable, the peak usually appears around 10 kHz [32]. Another approximation for D_{it} is given by

$$D_{it} = \frac{0.4}{qA} \left(\frac{G_p}{\omega} \right)_{10kHz} \quad (84)$$

where 10 kHz is used to indicate G_p peak at 10 kHz AC modulation frequency is used.

1.3. Electrical Conduction in Amorphous Semiconductors

Amorphous semiconductors are class of disordered materials which are lacking long range of structural order. They only possess a short range of order which is not sufficient to define a unit cell as in crystalline semiconductors[33]. Electronic structure of the material is determined by its molecular orbitals. Molecular orbitals of material are highly affected from the potential neighboring its atom[34]. If the potential surrounding does not severely affect the molecular orbital in an amorphous solid, it can exhibit similar electronic band structure with its crystalline state. However, there exist significant differences such as available electronic states within the forbidden energy gap which are not present in crystalline semiconductors[35]. Density of the electronic states in an amorphous semiconductor is illustrated according to Mott-Davis model in Figure 18. By the fact that electronic states exist between E_C and E_V , ΔE is called forbidden gap mobility or mobility gap. The tail of the E_C and E_V host localized (low mobility) states while extended (high mobility) states present where $E > E_C$ and $E < E_V$. These states are originated from bonding disorder of the semiconductor. Moreover, mobility gap has a narrow localized state band which arises from structural defects[36]. Carrier transport in an amorphous semiconductor occurs in three different ways; i) transport through extended states which is similar to carrier transport in crystalline semiconductors, ii) hopping conduction in the localized states, iii) hopping conduction via localized states around E_F [35]. Hopping conduction occurs when a carrier in a localized state gains enough energy to hop from its site to another. This hopping movement can require a phonon to assist. Typically hopping conduction is

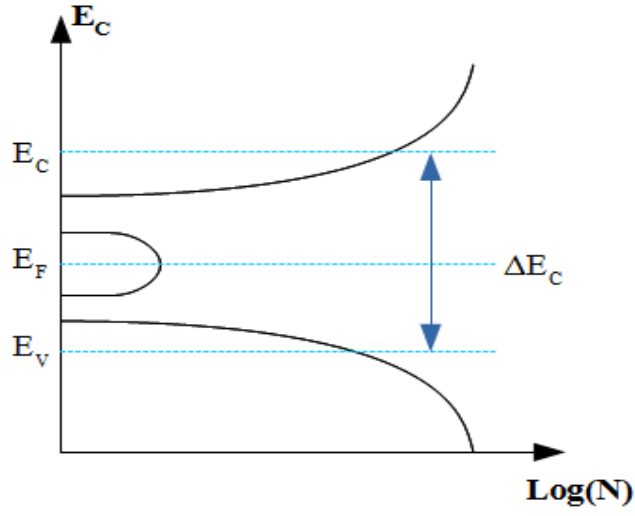


Figure 18. Density of electronic states in an amorphous semiconductor

much less than extended state conduction. Furthermore, it depends on temperature and applied AC frequency. Frequency depend hopping conductivity $\sigma(\omega)$, also known as AC conductivity, is given by

$$\sigma(\omega) = \frac{\sigma_{DC}}{(1 - (\omega\tau)^2)} \quad (85)$$

where σ_{DC} is the DC conductivity. Frequency dependence of the hopping conduction is given by the

$$\sigma(\omega) = c\omega^{-s} \quad (86)$$

where c is a proportionality constant. S is found to be $0.7 - 1.0$ for hopping conduction.

1.4. Transition Metal Oxides

1.4.1. Sub-stoichiometric Titanium Dioxide

TiO₂ thin films can be formed in amorphous or crystallized in rutile, anatase, or brookite structures. Rutile structure is thermodynamically the most stable structure among the other crystalline structures of TiO₂ [7]. On the other hand, stable brookite structure is hard to obtain [37]. Anatase and brookite phases are considered as the metastable phases of the TiO₂ which can be transformed to rutile phase by post deposition thermal treatments [38]. Deposition of TiO₂ at temperatures lower than 150°C results in amorphous TiO₂ films [39]. Anatase phase of TiO₂ is usually formed by deposition at relatively higher temperatures or by post deposition (PDA) at elevated temperatures [40],[41]. Moreover, the size of anatase nanocrystals and phase transformation from anatase to rutile nanocrystals with the thermal treatment at temperatures above 350°C was demonstrated [42]. Band gap energy is reported just above 3 eV for the rutile TiO₂ and ~3.2 eV for the anatase phase [7],[43]. High band gap energy reduces the parasitic light absorption when it is utilized as a window layer covering the solar cell surface [44]. Anatase form of TiO₂ is more desirable for photovoltaic applications owing to its indirect band gap which results in longer charge carrier lifetimes [43]-[45]. Moreover, lower value of lattice mismatch of anatase TiO₂ deposited on cSi makes it a good candidate for cSi based photovoltaic applications [46].

TiO_{2-x} – cSi n-n isotype heterojunction band alignment based on work function values of TiO_{2-x} which are taken from literature is depicted in Figure 19[47],[48]. Band bending of both CB and VB contributes to ϕ_{bi} and a large VB discontinuity exists in the n-n isotype TiO_{2-x} – cSi heterojunction.

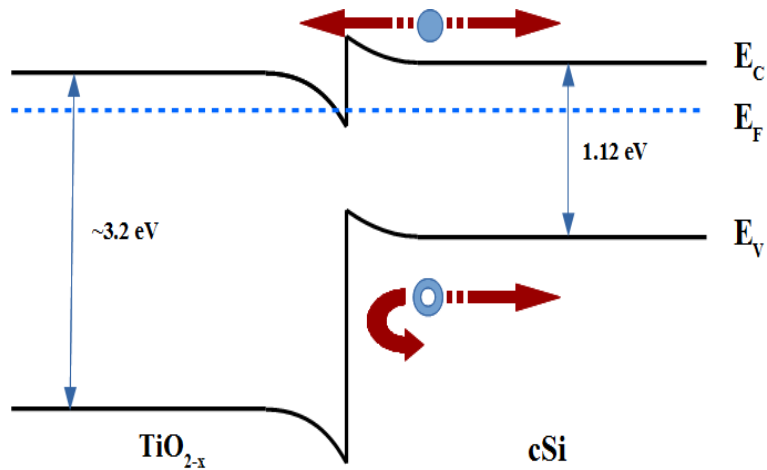


Figure 19. Energy band diagram of n-n isotype TiO_{2-x} – cSi heterojunction

Conduction band electrons can be transported in several ways: i) thermionic emission, ii) thermionic field emission (thermionic emission + FN tunneling), and iii) field emission (direct tunneling) in the n-n isotype TiO_{2-x} – cSi heterojunction. Same transport mechanisms are also valid for an electron on the CB of TiO_{2-x} . Electrons in the CB with sufficient energy to overcome the potential barriers of the CB can either go towards metal contact (see Figure 19 red arrows indicating directions) or towards gate metal due to the electrostatic potential. However, hole transport is limited to only one direction. Holes in cSi VB experience huge potential barrier at the interface and can be transported only through the metal contact on cSi. This transport mechanism is the origin of electron transporting – hole blocking nature of the TiO_{2-x} deposited on cSi substrates.

Electrical and structural properties of TiO_2 layer are highly dependent on the point defects in the bulk matrix of TiO_2 . Common point defects are known to be (i) oxygen or (ii) titanium vacancies, and (iii) titanium interstitials. Oxygen vacancies are formed when oxygen ions are detached from their hosting lattice site due to TiO_2 reduction [7]. On the other hand, titanium vacancies are originated from TiO_2 oxidation while titanium interstitials occur during the displacement of Ti atoms from their lattice site to the interstitial side during the TiO_{2-x} reduction duration.. Recently, Bak et al. has

shown that Ti vacancies have acceptor type point defect characteristics [49]. Defects originated from the reduction of TiO_2 (O vacancies and Ti interstitials) lead to n-type charge transport nature of TiO_2 since ionization results in the creation of quasi-free electrons in the TiO_2 film [49],[50].

High-quality TiO_{2-x} is critical for both charge carrier lifetimes and electron selective transport. Trapped charges inside the bulk of TiO_{2-x} due to the point and the structural defects can reduce or increase the conductivity of the charge carriers. Determination of these trapped charges and revealing any correlation between their effective number and the electrical response of TiO_{2-x} is crucial to fabricate the desired effective electron transporting–hole blocking layer (ET-HBL) TiO_{2-x} thin films. Another parameter which affects the carrier transport across the $\text{TiO}_{2-x}/\text{cSi}$ interface is the presence of interface trap charge states. Low levels of interface trap charge density and TiO_{2-x} film surface uniformity are crucial to reduce recombination of electrons at the $\text{TiO}_{2-x}/\text{cSi}$ interface.

1.4.2. Sub-Stoichiometric Molybdenum Trioxide

MoO_{3-x} is naturally n-type with a bandgap exceeding 3 eV which alleviates parasitic light absorption that present in narrower bandgap carrier collecting materials [44]. Its large work function ranging between 6-7 eV, depending on oxygen stoichiometry, makes MoO_{3-x} a possible candidate as a selective heterocontact [51]. Energy band diagram of $\text{MoO}_{3-x}/\text{p-type cSi}$ n-p anisotype heterojunction is shown in Figure 20.

In general, d-level oxidation corresponds to MoO_{3-x} conduction while occupancy of these levels determines conductivity characteristics in MoO_{3-x} and other transition metal-oxides, in general [52]. Stoichiometric molybdenum trioxide (MoO_3) has

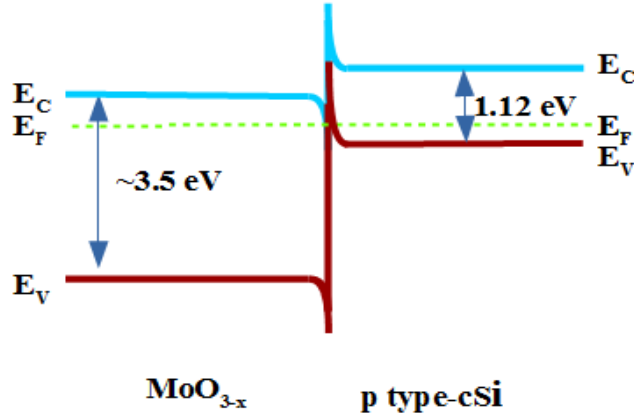


Figure 20. Energy band diagram of MoO_{3-x} /p-type cSi n-p anisotype heterojunction

insulator like behavior while molybdenum dioxide (MoO_2) shows metallic behavior. Recent studies have demonstrated that Mo^{+6} cation is responsible for the insulating behavior while Mo^{+5} and Mo^{+4} cations are responsible for the metallic behaviors in sub-stoichiometric MoO_{3-x} [53]. Oxygen vacancy introduces 4d levels within molybdenum trioxide bandgap which is responsible of hole selective transport [54]. Wong et al. reported that PDA at 180°C in inert gas environment induces gap states just below the fermi level energy within the band gap of MoO_{3-x} [55]. These gap states are originated from oxygen vacancies and they have ability to capture electrons [56]. Furthermore, It was reported by Arvizu et al. that anoxic PDA between 100°C and 225°C induces oxygen vacancies in MoO_{3-x} and PDA at temperatures $> 200^\circ\text{C}$ results in phase transformation and crystallization of MoO_{3-x} [57].

CHAPTER 2

EXPERIMENTAL DETAILS

2.1. Device Preparation

2.1.1. Crystalline Silicon Wafer Preparation

Mono-crystalline silicon (cSi) substrates were used to produce TMOs capacitors. Before TMO deposition, cSi surfaces were subjected to standard Radio Corporation of America (RCA) cleaning and a dilute hydrofluoric (HF) solution dip just before the evaporation to assure surface cleanliness, remove the oxide thin film grown during RCA cleaning procedure, and to eliminate undesired contamination at cSi and TMO interface. Wafers were rinsed after each cleaning processes with deionized water (DI) for 10 minutes.

2.1.2. Titanium Dioxide Thin Film Atomic Layer Deposition

Atomic layer deposition (ALD) is a widely used technique in semiconductor production processes owing to its capability of producing extremely uniform thin films [58] with superior surface coverage. Moreover, it is possible to achieve control at Å scale over the film thickness with ALD. A brief summary of thin film production process by ALD and ALD mechanism are illustrated in Figure 21 [59],[60]. TiO_{2-x} thin films were deposited on both p-type (5-10 ohm.cm) and n-type cSi (1-3 ohm.cm)

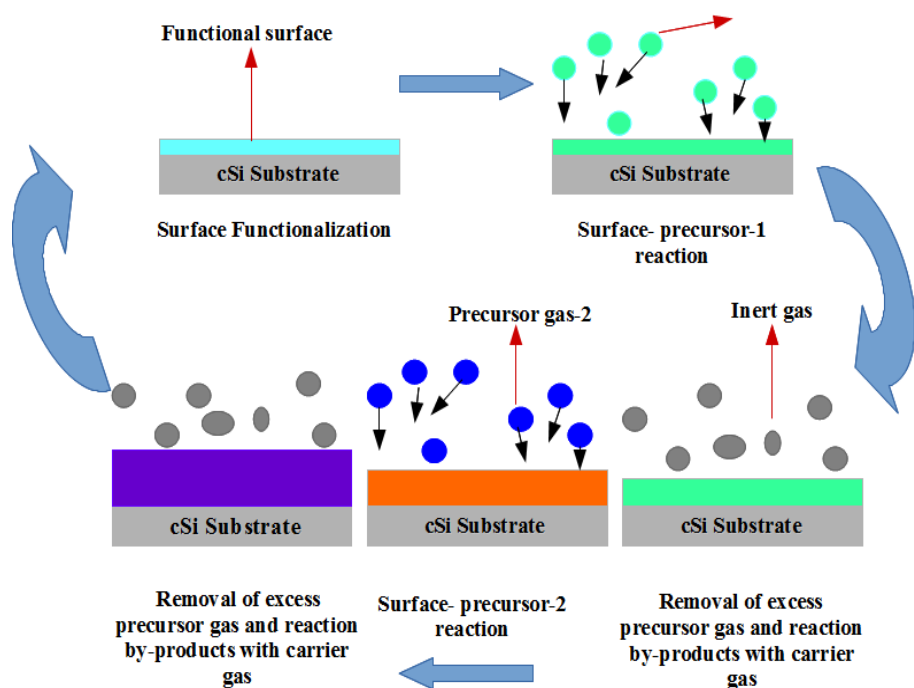


Figure 21. Atomic layer deposition cycle

substrates using a thermal-mode atomic layer deposition (ALD) system (V-Edge TYA-16). Tetrakis(dimethylamido)titanium (TDMAT) (Sigma-Aldrich) and H_2O were used as titanium and oxygen precursors, respectively. TDMAT was heated in a stainless cylinder to 75°C . Nitrogen (N_2) of 5N purity was used as carrier and purge gas at flow rate of 20 sccm resulting in a working pressure of 0.3 mbar. Each ALD reaction cycle consisted of 0.015 s pulse of TDMAT, 15 s purge with N_2 , 0.015 s pulse of H_2O , and 15 s purge with N_2 . The depositions were carried out for 300 reaction cycles at different substrate temperatures varying between 50°C and 300°C . To study the effect of post deposition annealing (PDA) on $\text{TiO}_{2-x}/\text{cSi}$ interface quality, the as-deposited TiO_{2-x} thin films prepared at 250°C were annealed at 300°C and 350°C in a flowing N_2 atmosphere for a total time of 1 h.

2.1.3. Molybdenum Trioxide Deposition by Thermal Evaporation

Physical vapor deposition (PVD) via thermal evaporation is simple and effective technique to deposit various materials such as metals and metal oxides. The general deposition mechanism of thermal evaporation is illustrated in Figure 22.

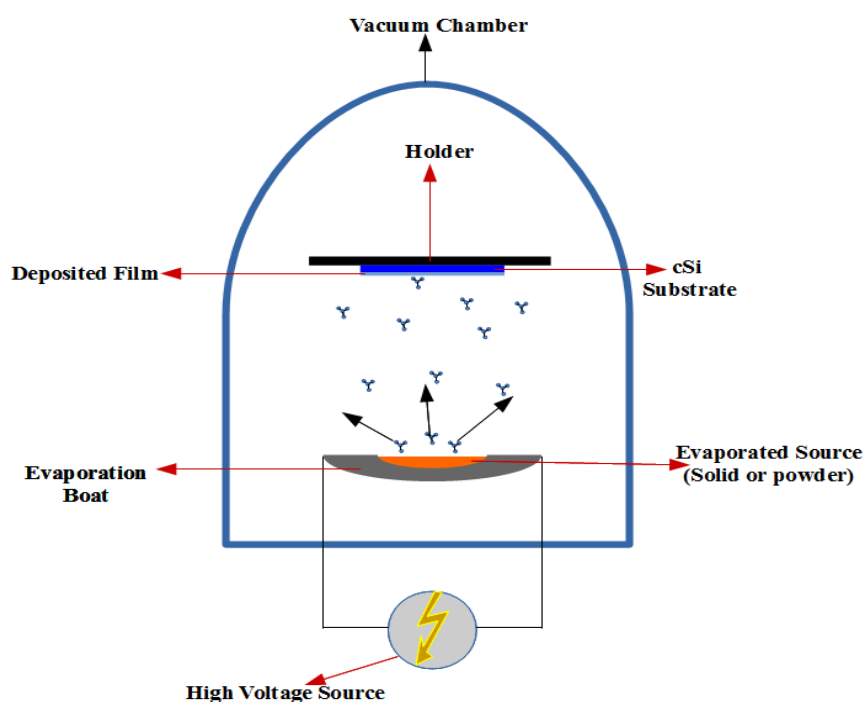


Figure 22. Thermal evaporation deposition mechanism

MoO_{3-x} thin films studied in this work were deposited by vacuum sublimation from 99.99% pure MoO₃ powder positioned 20 cm away from the cSi samples. MoO₃ powder was evaporated at a temperature of ~790°C at a deposition pressure of $\sim 1 \times 10^{-6}$ torr to obtain a deposition rate of 0.15–0.2 Å/sec (as monitored by a crystal oscillator). The cSi substrates were kept at room temperature during deposition. MoO_{3-x} thin films were evaporated on to n-type and p-type float zone (FZ), c-Si wafers. Three different MoO_{3-x} thicknesses were considered in this study: 20, 40, and 90 nm deposited on p-type cSi wafers. Set of MoO_{3-x} thin films with 90 nm thickness grown

on p-type cSi wafers were subjected to PDA in N₂ environment using a flow rate of 150 sccm for 1 hour in the temperature range of 200°C and 400°C.

2.1.4. Metallization

Native SiO₂ removal from cSi surface prior to rear side metallization was done by dilute HF solution in order to remove native oxide which is grown during MoO_{3-x} deposition. Immediately after rear side HF treatment, ~400 nm of silver (Ag) for n-type and aluminum for p-type cSi substrates, respectively, were evaporated by thermal evaporation technique. To complete the TMOS capacitors, ~400 nm thick Ag circular dots with a radius less than 300 μm each were deposited on top of TMO thin films through a shadow mask. The final structure of the fabricated MOS capacitors is depicted in Figure 23.

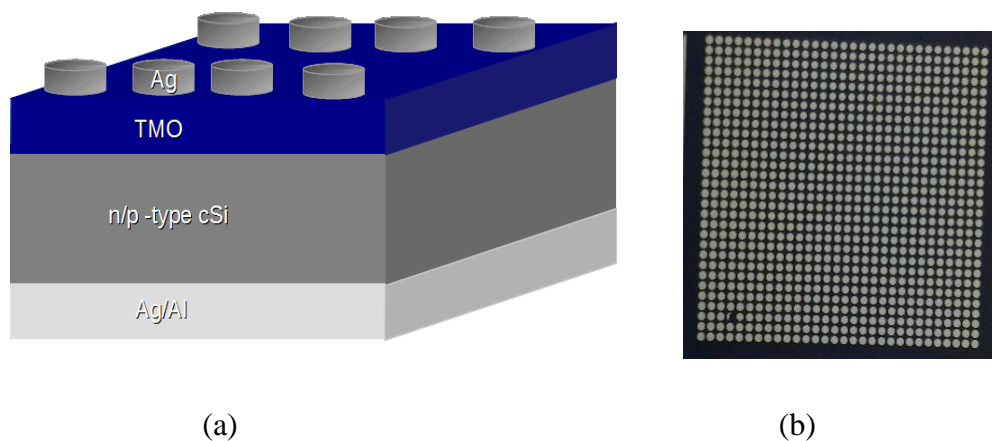


Figure 23. (a) Schematic of Transition Metal-Oxide-Semiconductor (TMOS) capacitor (b) actual device (top view)

2.2. Device Characterization

2.2.1. Electrical Transport Measurements

Electrical characterization of the TMOS capacitors were done by admittance (Y) and current voltage measurements at room temperature under dark and light ambient. For measurements under light, a UV-visible light source was utilized. Electrical measurement setup is illustrated in Figure 24.

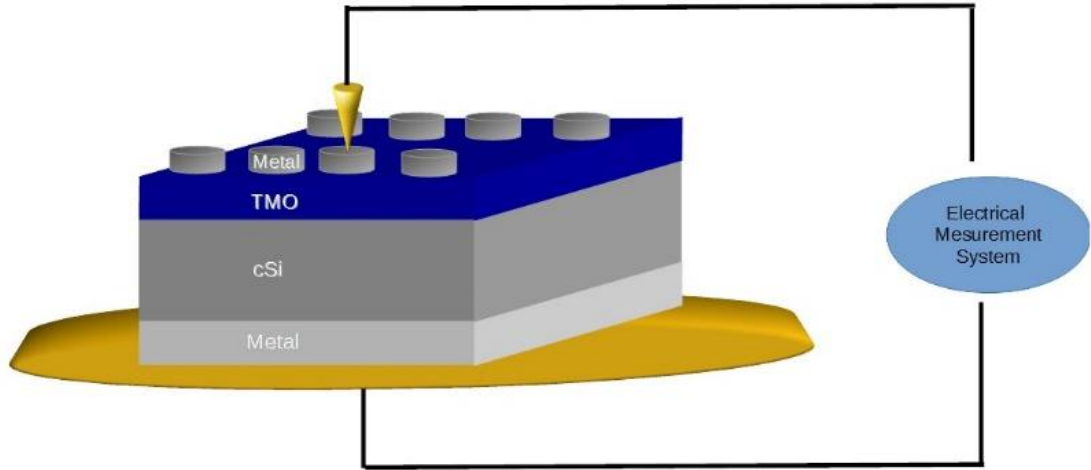


Figure 24. Electrical measurement setup schematics

A gold coated micro needle was used as probe and rear side of the TMOS capacitor were in contact with a plate which can support whole rear area of the TMOS capacitor. Admittance measurements were conducted using HP 4192 LF impedance analyzer. AC modulation frequency was held fixed at each frequency in the (1 kHz–10 MHz) range for each measurement while the DC bias sweeps between -10 V and +10 V to observe the general capacitance behavior and the high-frequency C-V hysteresis. Moreover, Capacitance–Frequency (C-F) measurements were performed by sweeping the AC modulation frequency from 5 Hz to 10 MHz while the DC bias was kept constant under the accumulation condition. During both DC bias and AC frequency

dependent admittance measurements, AC modulation amplitude was fixed at 50 mV in order to satisfy small signal condition.

Effect of the R_s is discussed in section 1.4.2, however, some methods (such as the conductance method) neglect the effect of R_s . As the R_s of a MOS capacitor is low, the electrical parameters can be extracted from the admittance data. Still, a series resistance correction on C and G ensures getting more precise results. These corrections were done on the measured data before extracting that electrical parameter which usually require relations that eliminate the contribution of R_s . Corrected C and G is given as [31]

$$C_c = \frac{(G_m^2 + \omega^2 C_m^2) C_m}{[G_m - (G_m^2 + \omega^2 C_m^2) R_s]^2 + \omega^2 C_m^2} \quad (87)$$

And

$$G_c = \frac{(G_m^2 + \omega^2 C_m^2) [G_m - (G_m^2 + \omega^2 C_m^2) R_s]}{[(G_m^2 + \omega^2 C_m^2) R_s]^2 + \omega^2 C_m^2} \quad (88)$$

I-V measurements were conducted using Kietley 4001 Source Meter. DC bias was swept at rate of 0.01 V. The position of the probes was kept fixed at the same circular pin contact during each I-V and C-V measurement to avoid any unsystematic measurement arising from possible local non-uniformities in the TMO thin films.

2.2.2. Optical Measurements

Thickness of TMO films were measured by model spectroscopic ellipsometry. Band gap of TMOs were calculated from data obtained by UV-visible absorption spectra model spectrometer and spectroscopic ellipsometry.

CHAPTER 3

RESULTS & DISCUSSION

3.1. Electron Selective Atomic layer Deposited $\text{TiO}_{2-x}/\text{cSi}$ Metal-Oxide-Semiconductor-Capacitor

Hf C-V, G-V and R_s -V hysteresis curves of $\text{TiO}_{2-x}/\text{n-type cSi}$ MOS capacitor produced at 200°C ALD temperature are shown in Figure 25. Each parameter (C, G, and R_s) shows strong dependence on applied AC frequency. Frequency dependence of the capacitance and conductance values for the the MOS capacitor is shown in Figure 25(a). At accumulation capacitance; with applied DC bias ≥ 0 V, saturation was not observed when the applied AC frequency is relatively low. Saturation is observed at ~ 1 MHz as modulation frequency and the capacitance knees down at higher AC modulation frequencies. This behavior of accumulation capacitance is attributed to the frequency dependence of the interface trapped charges relaxation and R_s originating from the device and the measuring system [25],[61]. Frequency dependence of R_s becomes insignificant under strong accumulation at values just above 0.1 k Ω as can be seen in Figure 25(c). R_s peaks are frequency dependent which is due to the dependence of the interface charges relaxation on the AC frequency. Similar dependency also appears in the conductance measurement under the depletion and accumulation regimes which is related to the charges trapped at the TiO_{2-x} -cSi interface [31]

Furthermore, leakage conductivity via defect state in the TiO_{2-x} is responsible for decreasing capacitance since conductance values (Figure 25(b)) increases with frequency at accumulation regime. $\sigma - \omega$ curve of TiO_{2-x} is plotted in Figure 26. Frequency dependence of σ (as discussed in section 1.3) is related to hopping

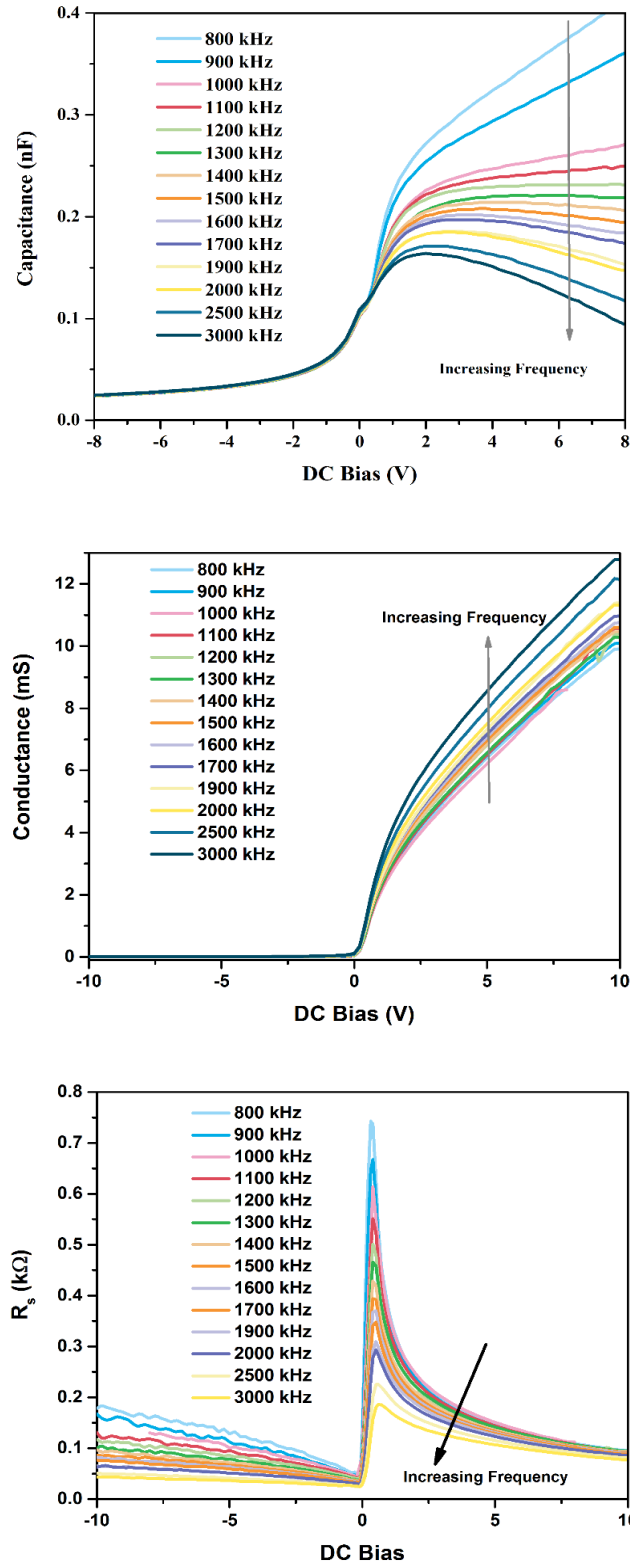


Figure 25. (a) C-V, (b) G-V, and (c) R_s -V high frequency hysteresis curves of n-type TiO_{2-x} MOS capacitor deposition at 200°C

conduction from localized electronic states on the band tails of TiO_{2-x} when the conductivity-frequency proportionality constant s in the relation (86) is between 0.7 – 1.0. Measured s value was found to be 0.84 as indicated from the fitting in Figure-26. This shows that the hopping conduction contributes to the frequency dispersion of C-V and G-V curves.

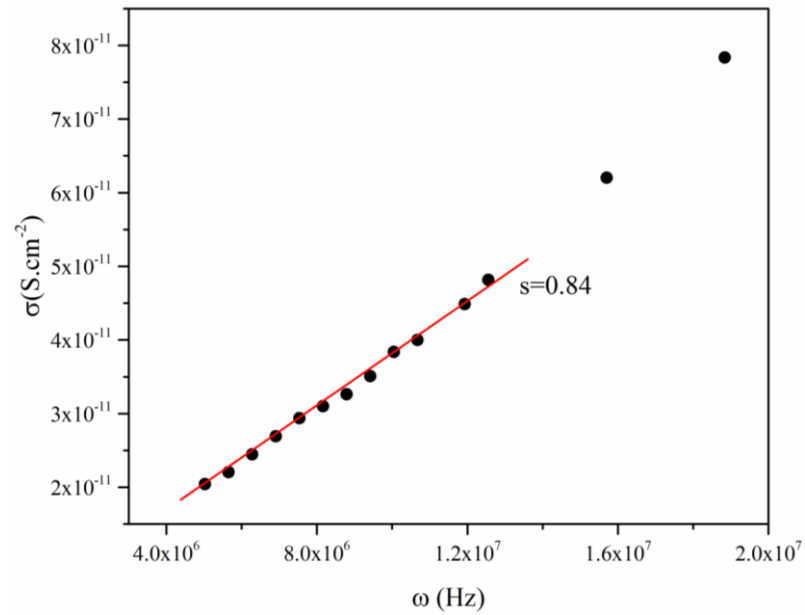


Figure 26. σ - ω graph of n-type TiO_{2-x} MOS capacitor deposited at 200°C.

3.1.1. Effect of ALD Temperature on Electrical Properties of the $\text{TiO}_{2-x}/\text{cSi}$ MOS Capacitors

Figure 27 shows the thickness of TiO_{2-x} thin films deposited at different substrate temperatures and as measured by spectroscopic ellipsometry.

It can be seen that the thickness of TiO_{2-x} decreases as the deposition temperature increases while the band gap was found to vary between 3.28–3.38 eV which is

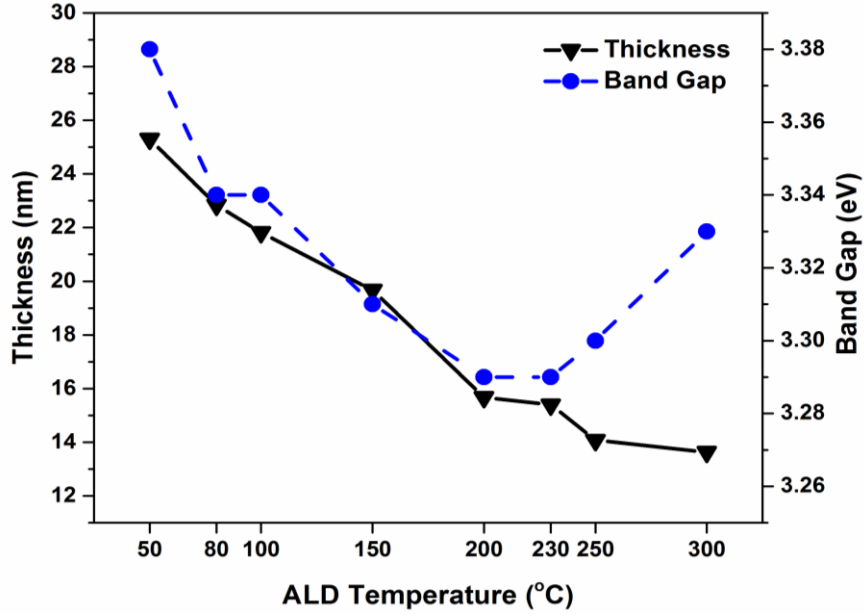


Figure 27. Thickness and band gap of the TiO_{2-x} prepared at different deposition temperatures as measured by spectroscopic ellipsometry.

consistent with the values reported for TiO_2 thin films deposited with ALD technique in the literature [7],[47]-[62]. Band gap values decrease with increasing the deposition temperature and the lowest band gap value was obtained for sample deposited at 200°C. Further increase in the deposition temperature above 200°C results in an increase in the band gap of the TiO_{2-x} films.

C-V curves of TiO_{2-x} – cSi MOS capacitors with different ALD temperatures at 1 MHz AC modulation frequency are plotted in the Figure 28.

Different relative ϕ_{FB} shift around the voltage axis; as shown in Figure 28 for each sample deposited at different temperature may suggests that each deposition temperature results in different oxide trapped charge density. It is worth mentioning that, there exist less relative ϕ_{FB} shift between samples with high ALD temperature ($T > 150^\circ\text{C}$). Measured electrical parameters of the MOS capacitors with different ALD temperature are listed in Table 1. The ϕ_{FB} values of the MOS capacitors decline with increasing the ALD temperature as shown in Table 1.

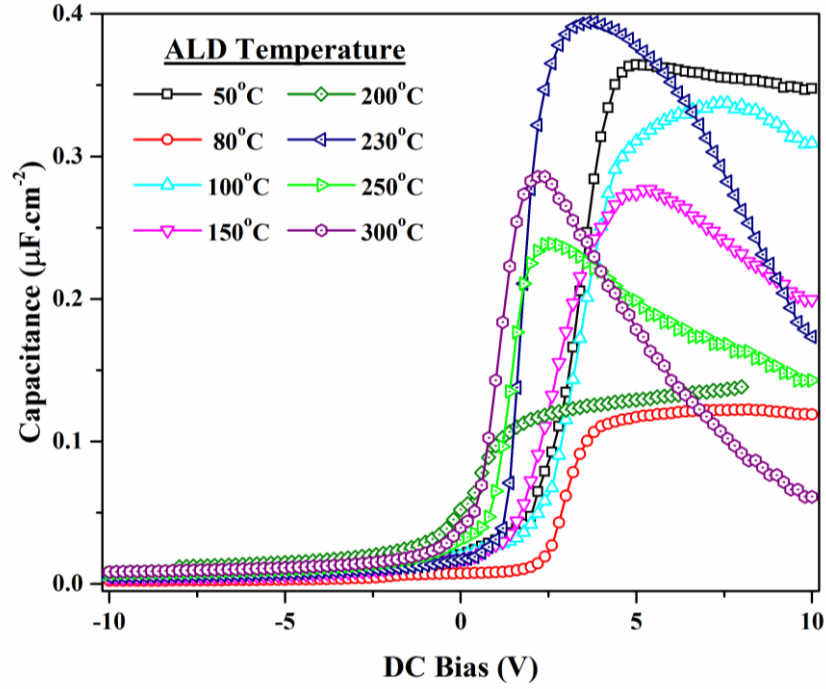


Figure 28. C-V characteristics of the TiO_{2-x} – cSi MOS capacitors with different ALD temperatures under 1MHz AC modulation frequency

Table 1. Measured electrical parameters of TiO_{2-x} /n-type cSi MOS capacitors with different ALD temperature

ALD Temperature	R_s (k Ω)	Φ_{FB} (V)	Φ_{bi} (V)	$J_{leakage}$ ($\mu\text{A.cm}^{-2}$)	η	D_{it} ($10^{12}\text{eV}^{-1}.\text{cm}^{-2}$)
50°C	0.11	3.40	0.36	398.11	1.51	8.02
80°C	0.17	3.06	0.82	0.34	2.02	5.43
100°C	0.12	3.29	0.37	1.51	3.31	4.81
150°C	0.06	2.76	0.56	3.16	1.60	7.45
200°C	0.11	0.92	0.40	18.6	3.85	5.64
230°C	0.07	1.69	0.68	9.54	3.23	1.90
250°C	0.05	1.40	0.52	5.62	3.96	3.35
300°C	0.04	1.02	0.45	1152.26	3.27	3.13

Series resistance is a parameter that limits the device performance.. Fabrication and measurement were simultaneous and identical for all the fabricated MOS capacitors. Therefore, we assume that the oxide and the interface are the major reasons for the series resistance differences of the MOS capacitors. R_s values were calculated from measured admittance data and tabulated in Table-1. The lowest value of R_s is measured to be 45.1 Ω for the sample deposited at 300°C whereas the sample deposited at 80°C exhibited a R_s of 171 Ω . A decreasing trend with increasing the deposition temperature is observed after 200°C. Barrier heights are extracted from the C-V data as discussed in sections 1.1.3 and 1.2.2. ϕ_{bi} shows no trend with the ALD temperature. Extracted ϕ_{bi} values are between 0.36 – 0.82 V which are in the range of the values in literature.[63]-[64].

Measured values of the interface trap levels have wide range of energy spectra. Among these, the ones falling within cSi band gap are the most important spectra since they act as recombination centers. The values of D_{it} within cSi CB and mid gap energies are shown in Table 1 for different deposition temperatures. Lowest D_{it} of $1.90 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ was obtained for the sample deposited at 230°C while the highest value of $D_{it} = 8.02 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ was obtained for the sample deposited at 50°C. There exists correlation between ϕ_{FB} and D_{it} such that increasing D_{it} results in relative ϕ_{FB} shift (Figure 28). By considering relation (66), it can be suggested that negative charges trapped at the interface causes a ϕ_{FB} shifts over the DC bias axis toward to positive values. J-V characteristics of TiO_{2-x} / n-type- cSi MOS capacitors are plotted in Figure 29

Leakage current densities (J_{leakage}) which is the J values at $V < 0$, of the TiO_{2-x} / n-type- cSi MOS capacitors at -1V are shown in Table 1. J_{leakage} values greatly vary in magnitude for each deposition temperature. The highest value of J_{leakage} is $1.15 \times 10^{-3} \text{ A.cm}^{-2}$ for the sample deposited at 300°C. It is expected that J_{leakage} increases with decreasing film thickness of a high- κ dielectric material such as TiO_{2-x} since direct and FN tunneling probability increases with decreasing

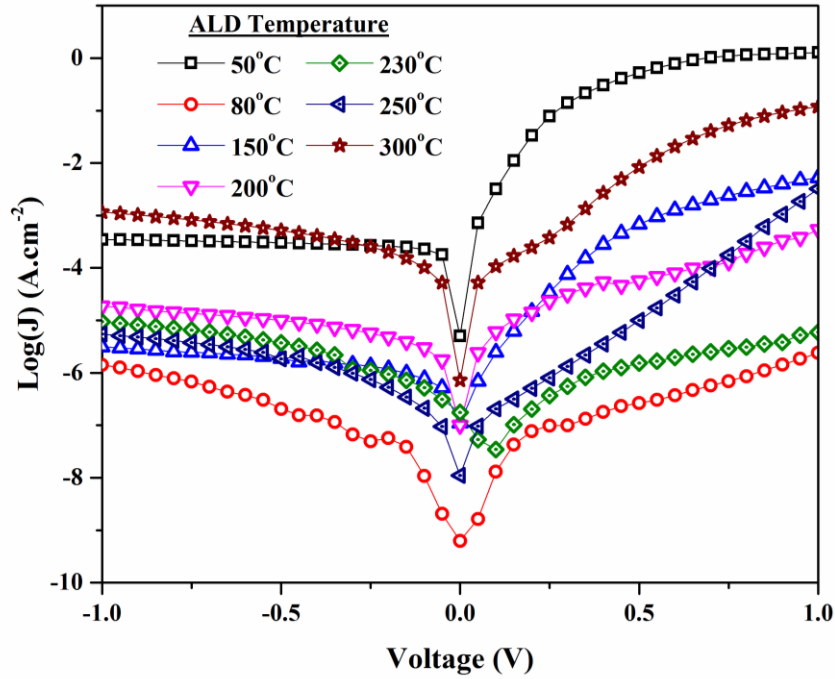


Figure 29. J-V curves in semi-log scale for the MOS capacitors with different deposition

the thickness of the dielectric thin film. Although there exist a slight difference in the thicknesses of a round~0.45 nm between the MOS capacitors fabricated at 250°C and 300°C ALD temperatures, still the J_{leakage} difference between these two capacitor is ~3 order of magnitude. Therefore, this difference cannot be explained by the increase of quantum mechanical tunneling probability. High J_{leakage} value may arise from the structural defects in the TiO_{2-x} thin films. On the other hand, the lowest value of $1.41 \times 10^{-6} \text{ A.cm}^{-2}$ is obtained for the sample deposited at 80°C which is expected since low temperature deposition of TiO_{2-x} results in amorphous film formation. Apart from these two J_{leakage} values, the obtained J_{leakage} values of all the other produced TiO_{2-x} / n-type- cSi MOS capacitors are comparable with the reported values in the literature for ALD deposited TiO_{2-x} thin films[61],[65]. Moreover, TiO_{2-x} / n-type- cSi MOS capacitors with ALD temperature of 80°C and 230°C have symmetrical J-V curves around J-axis, in addition $J_{\text{leakage}} > J_{\text{F}}$ in the DC bias range of -1V – +1V. This phenomena is not peculiar to this study, in fact it also observed by others

[41],[64],[65]. This phenomenon can be explained by considering the Figure 19. When the potential barriers on the either side of TiO_{2-x} / n-type- cSi heterojunction are comparable, thermionic emission from CB of Si to CB of TiO_{2-x} is comparable to the emission from CB of TiO_{2-x} to CB of Si. In other words, two materials exhibit metal-semiconductor junction like conduction mechanism. Furthermore, difference between emission rates of TiO_{2-x} / Ag and Si/Ag may be the reason for observing $J_{\text{leakage}} > J_{\text{F}}$. Moreover, η of the TiO_{2-x} / n-type- cSi MOS capacitors were shown in the Table 1. The MOS capacitors with higher ALD temperatures exhibit larger η values than those deposited at lower temperatures. It is worth mentioning that there exist a correlation between D_{it} and η values where it was found that TiO_{2-x} / n-type- cSi MOS capacitors with $\eta > 3$ exhibit less D_{it} .

The highest value of $3.37 \times 10^{-7} \text{ A.cm}^{-2}$ was obtained for the 250°C deposited sample after post deposition annealing at 350°C which can be attributed to the less crack density in the film and low average density of the interface states [66]. Similarly, J values at positive voltages are different for each MOS capacitor deposited at different temperatures which is due to the existence of different barrier heights.

3.1.2. Effect of PDA on TiO_{2-x} / n-type- cSi MOS Capacitor with ALD at 250°C

Figure 30 shows the changes in capacitance characteristics of TiO_{2-x} / n-type- cSi MOS capacitor prepared at 250°C and annealed at 300°C and 350°C .. The dominant change after PDA is at accumulation capacitance which suggests that TiO_{2-x} experienced some structural changes since the accumulation capacitance is highly correlated to $\kappa_{\text{TiO}_{2-x}}$. Moreover, a capacitance valley between 0-1 V appears after PDA which is in related to VB discontinuity of two material at the junction in the case of n n isotype heterojunction [18].

The ϕ_{FB} shift with increasing PDA temperature is clearly seen in Figure 30 which is identical to ϕ_{FB} shift for the cases when TiO_{2-x} thin films are deposited at higher ALD temperatures. This suggests that there exists a correlation between ϕ_{FB} and the thermal

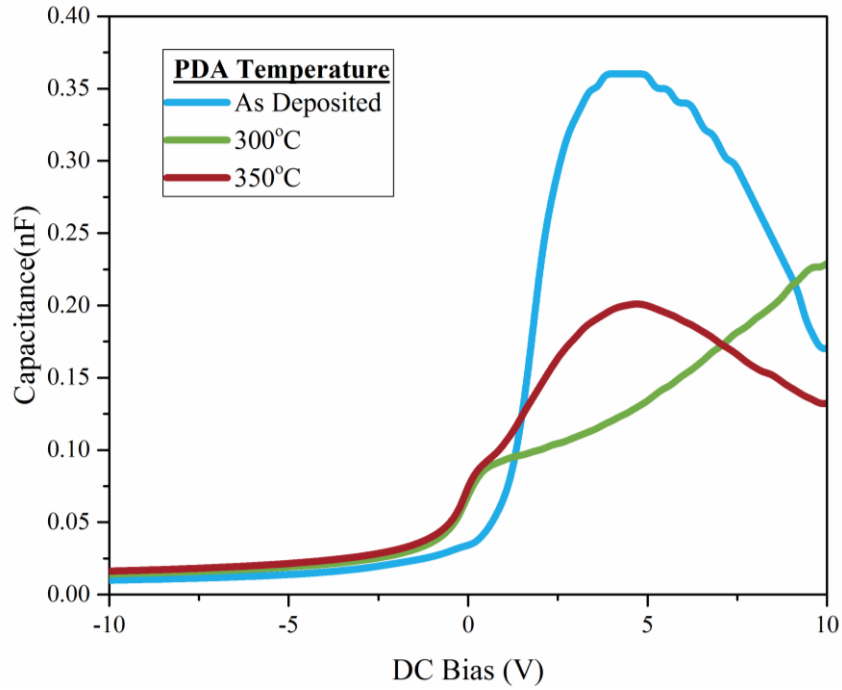


Figure 30. C-V curves of the TiO_{2-x} / n-type- cSi MOS capacitors with 250°C ALD temperature annealed at 300°C and 350°C under 1MHz AC modulation frequency

conditions at relatively high temperatures. As the temperature of thermal conditions increases (ALD temperature or PDA), C-V curves of the TiO_{2-x} / n-type- cSi MOS capacitor shift toward negative voltages. Hence, it is an indication of the presence of trapped positive charges either at TiO_{2-x} / n-type- cSi interface or in the TiO_{2-x} itself. Electrical parameters of TiO_{2-x} / n-type- cSi MOS capacitor with 250°C ALD temperature before and after PDA are tabulated in Table 2.

The influence of PDA was also investigated for TiO_{2-x} / n-type cSi MOS capacitor deposited at 250°C by frequency dependent C-V measurement. PDA shifts the C-V curves towards lower frequencies as shown in Figure 31. These shifts indicate that the interface trapped states relaxation time distribution as well as the interface quality change with PDA. Measured D_{it} values for different PDA temperatures are tabulated in Table 2. It can be seen that PDA at 300°C and 350°C improve the interface quality since D_{it} decreases with PDA at these temperatures.

Table 2. Measured electrical parameters of TiO₂-x /n-type with 250 ALD temperature before and after PDA cSi MOS capacitors with different ALD temperature

PDA Temperature	R_s (k Ω)	Φ_{FB} (V)	Φ_{bi} (V)	$J_{leakage}$ ($\mu A.cm^{-2}$)	η	D_{it} ($10^{12}eV^{-1}.cm^{-2}$)
As Dep.	0.05	1.40	0.52	5.62	3.96	3.35
300°C	0.10	-0.25	0.51	25.02	2.87	2.19
350°C	0.13	-0.21	0.61	0.34	2.56	2.98

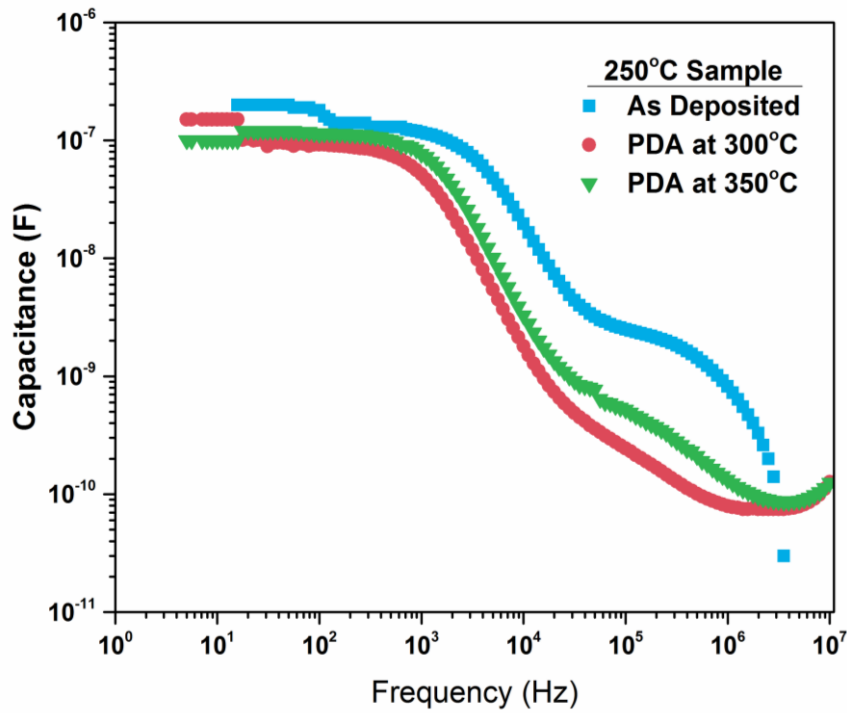


Figure 31. Frequency dependence of the accumulation capacitance of the MOS capacitor deposited at 250°C and treated with different post-deposition temperatures.

Yet, the sample annealed at 350°C has a larger number of D_{it} than that annealed at 300°C. This can be attributed to the fact that PDA at elevated temperatures (above 350°C) can result in the formation of i) surface boundaries between TiO_x and cSi substrate or ii) interfacial Si- TiO_2 layer; in the sample annealed at 350°C [7]

The effect of PDA on R_s of the samples deposited at 250°C is tabulate in Table 2. It can be seen that R_s value increases drastically with increasing the PDA temperature. This increase in R_s with increasing PDA temperature is attributed to the fact that PDA above 300°C can form (i) grain boundaries between TiO_{2-x} and cSi which are formed due to TiO_{2-x} crystallization at nano-scale and (ii) an interfacial layer at TiO_{2-x} /cSi interface which contributes to series resistance [7],[42].

PDA at 300°C has no pronounce effect on η values of the MOS capacitor with a slight change of ~ 0.01 V which implies PDA at this temperature did not alter the conduction band alignment. However, it is clear that structural changes occurred considering the reduction of accumulation capacitance with PDA. It can be suggested that changes occurred at VB discontinuities of TiO_{2-x} and cSi junction. On the other hand, 0.1 V increment was measured after PDA at 350°C which suggests that PDA this temperature triggers the band bending of the CB of the two materials.

Results of G-V measurement are shown in Figure 32. Conductance values decrease dramatically with increasing PDA temperature at accumulation and depletion regimes. Furthermore, a conductance saturation occurs at the accumulation for the as deposited sample and sample with PDA at 350°C whereas the sample with PDA at 300°C shows no saturation; in fact, increases moderately.

Effect of PDA on J-V characteristic is plotted Figure 32. $J_{leakage}$ increases with PDA at 300°C (Table 2) and decreases with PDA at 350°C from $5.62 \mu A.cm^{-2}$ to $0.34 \mu A.cm^{-2}$. Furthermore, η of the TiO_{2-x} / n-type- cSi MOS capacitor with ALD 250°C decreases with the increasing PDA temperature as shown in Table 2. The J-V curve TiO_{2-x} / n-type- cSi MOS capacitor annealed at 350°C exhibits three different conduction mechanism. At low forward bias, conduction mechanism includes the contributions of both J_{diff} and J_{diff} ($\eta \sim 2$), at moderate bias $\eta = 2.56$, while further increase in the DC bias results in high injection condition with $\eta > 3$.

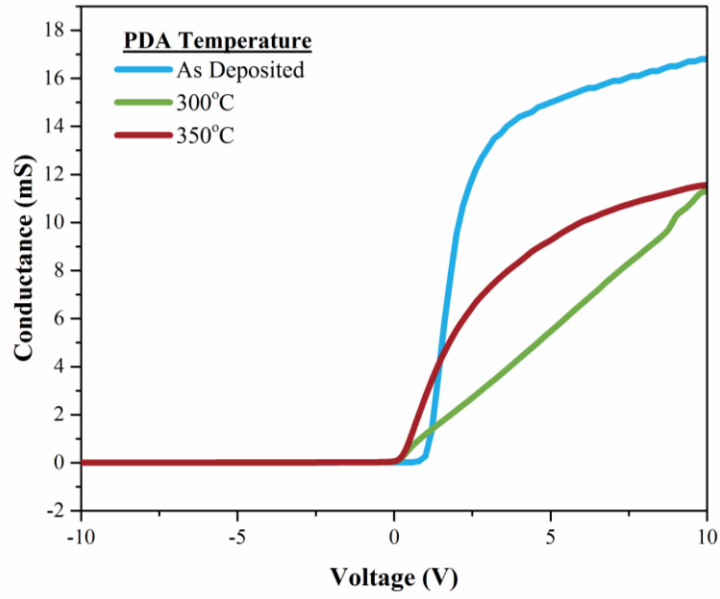


Figure 32. G-V curves of the TiO_{2-x} / n-type- cSi MOS capacitors with 250°C ALD temperature annealed at 300°C and 350°C under 1MHz AC modulation frequency

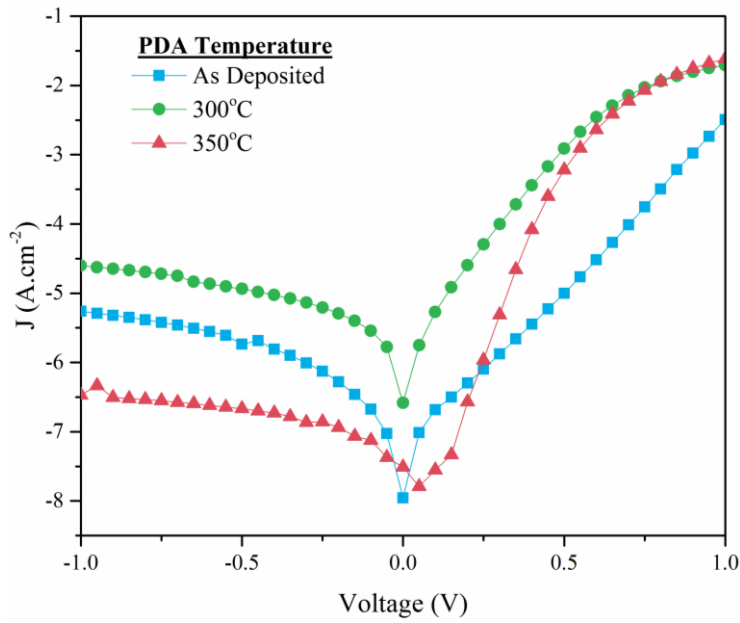


Figure 33. J-V curves of the TiO_{2-x} / n-type- cSi MOS capacitors with 250°C ALD temperature annealed at 300°C and 350°C

3.2. Hole Selective Thermally Evaporated MoO_{3-x} /cSi MOS Capacitor

Figure 34 shows the Hf capacitance-voltage and conductance-voltage characteristics at different AC modulation frequencies of 90 nm thick MoO_{3-x} deposited on p-type cSi wafer which is common for all the produced MoO_{3-x} – cSi MOS capacitors.

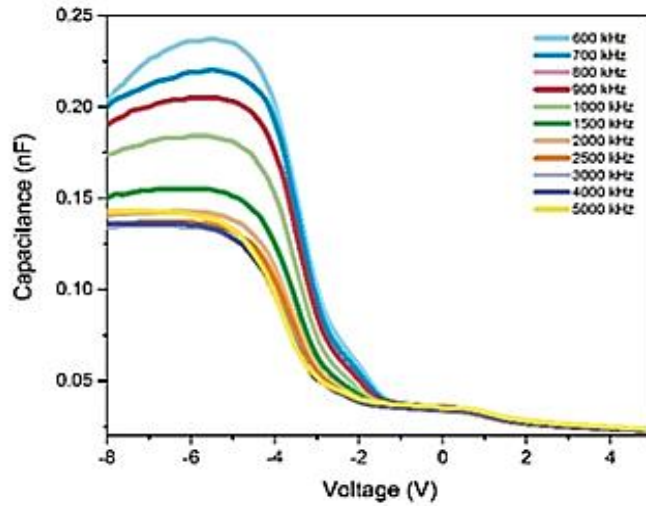


Figure 34. Hf -Capacitance-Voltage characteristics of 90 nm MoO_{3-x} /p-type cSi MOS capacitor

It can be seen that as frequency increases, oxide capacitance decreases. With changing the applied AC frequency, dispersion in CV curves is observed in accumulation regime accompanied with formation of peak maxima. In depletion and weak inversion regimes at $\sim 0\text{V}$; in Figure 34, frequency dependent dispersions were not observed, yet peak maxima dominate the curves. Ideally, no frequency dependent dispersion of oxide capacitance or peak in the accumulation, depletion, or weak inversion regimes is

expected[25]. All of these three types of peaks anomalies for MoO_{3-x} / cSi MOS capacitor are frequency dependent.

3.2.1. Effect of MoO_{3-x} Thickness

Measured electrical parameter of MoO_{3-x} / p-type cSi MOS capacitors with different thicknesses are tabulated in Table 3. C-V curves of the MoO_{3-x} /p-type-cSi MOS capacitors are shown in Figure 35. Ideally, it is expected that when the thickness of dielectric layer is doubled its capacitance reduces to half of its initial value.

Table 3. Effect of the MoO_{3-x} thickness on MoO_{3-x} / p-type cSi MOS capacitors' electrical parameters.

Thickness	90 nm	40 nm	20 nm
R_s (kΩ)	1.32	1.34	1.55
Φ_{bi} (V)	0.83	0.53	0.57
Φ_{FB} (V)	-0.68	-1.27	-1.79

However, accumulation capacitance of the MoO_{3-x} /p-type cSi MOS capacitors do not meet that expectation. On the contrary, the 20 nm and 40 nm thick MOS capacitor have similar capacitance value at the strong accumulation regime. This can be explained by tunneling and leakage current mechanisms. As discussed in section 1.1.2, decreasing MoO_{3-x} layer thickness increases the pure field emission and thermionic field emission rates, and the probability of recombination of charge carriers before reaching metal contact reduces. Furthermore, Φ_{FB} of the MoO_{3-x} /p-type-cSi MOS capacitors shifts towards negative voltages suggesting that number of the negative charges increases with MoO_{3-x} layer thickness. Similarly, R_s of MoO_{3-x} /p-type-cSi MOS capacitors decreases with increasing MoO_{3-x} thickness. On the other hand, Φ_{bi} of the MoO_{3-x}/p-type-cSi MOS capacitors are almost identical for 20 nm and 40 nm thick

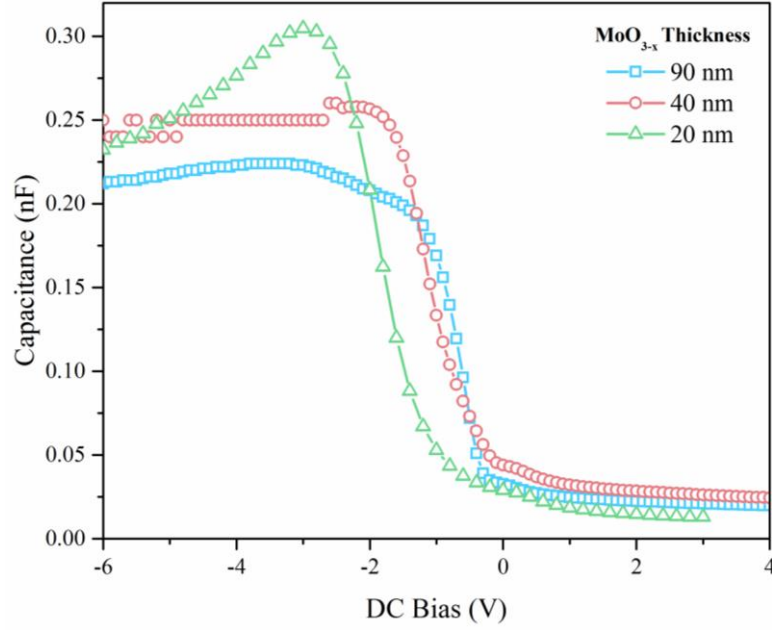


Figure 35. Hf -Capacitance-Voltage characteristics of MoO_{3-x} /p-type cSi MOS capacitor with different MoO_{3-x} thicknesses under 500kHz AC modulation.

MoO_{3-x} s. Moreover, the ϕ_{bi} of the MoO_{3-x} /p-type cSi MOS capacitors with 20 and 40 nm thick MoO_{3-x} (Table 3) are nearly the same. However, ϕ_{bi} increases by ~ 0.3 V when the film thickness is 90 nm. This may imply that band alignment of the p-type / MoO_{3-x} depends on the film thickness. This dependency is probably originated with changing oxide stoichiometry of MoO_{3-x} . G-V curves of MoO_{3-x} /p-type cSi MOS capacitors are plotted in Figure 36. MoO_{3-x} /p-type cSi MOS capacitor with 40 nm thickness has two different threshold points for conduction; i) transition from inversion to depletion, ii) leakage conduction due to applied high field at weak accumulation. The highest conductivity is measured for 40 nm thick MoO_{3-x} /p-type cSi MOS capacitor under accumulation condition.

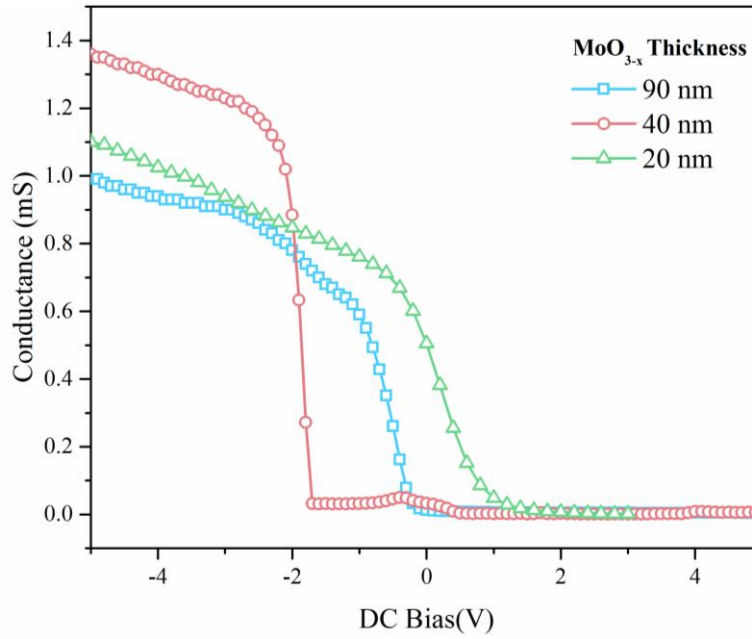


Figure 36. Hf -Capacitance-Voltage characteristics of MoO_{3-x} /p-type cSi MOS capacitor with different MoO_{3-x} thicknesses under 500kHz AC modulation.

3.2.2. Effect of PDA on P-Type MoO_{3-x} / cSi MOS Capacitor

Effect of PDA on the measured electrical parameters measured from the 90 nm thick MoO_{3-x} / p-type cSi MOS capacitor are tabulated in Table 4.

Table 4. Effect of the PDA on the electrical properties of 90 nm p-type MoO_{3-x} – cSi MOS capacitor

PDA Temperature	As Deposited	200°C	300°C	400°C
D_{it} ($10^{12} \text{eV.cm}^{-2}$)	9.46	6.61	27.32	20.85
R_s ($\text{k}\Omega$)	2.04	2.74	0.12	0.21
Φ_{bi} (V)	0.62	0.39	0.55	0.18
Φ_{FB} (V)	-0.57	1.35	-1.24	-2.52
C_{ox} (nF)	0.21	0.13	2.42	0.63
E_g	3.51	3.54	3.79	4.25

Capacitance values at accumulation (C_{ox}) vary greatly in magnitude which is clearly seen in the Table 4. To illustrate this more, C-V curves of the MoO_{3-x} /p-type cSi MOS capacitor are normalized to C_{ox} and depicted in Figure 37. PDA at 200°C reduces D_{it} suggesting that PDA improves the interface quality. PDA at temperatures $> 200^\circ C$ increases formation interface trap state at the p-type cSi/ MoO_{3-x} interface. D_{it} rises to 3 times than its value after PDA at 300°C. Formation an interfacial layer between MoO_{3-x} can be responsible from this increase in D_{it} . Large changes on accumulation capacitance are mostly originated from the changes in the dielectric properties of MoO_{3-x} . Contrary to all the other 90 nm thick MoO_{3-x} /p-type cSi MOS capacitors, a positive ϕ_{bi} was found. This is caused by PDA at 200°C in N_2 environment which

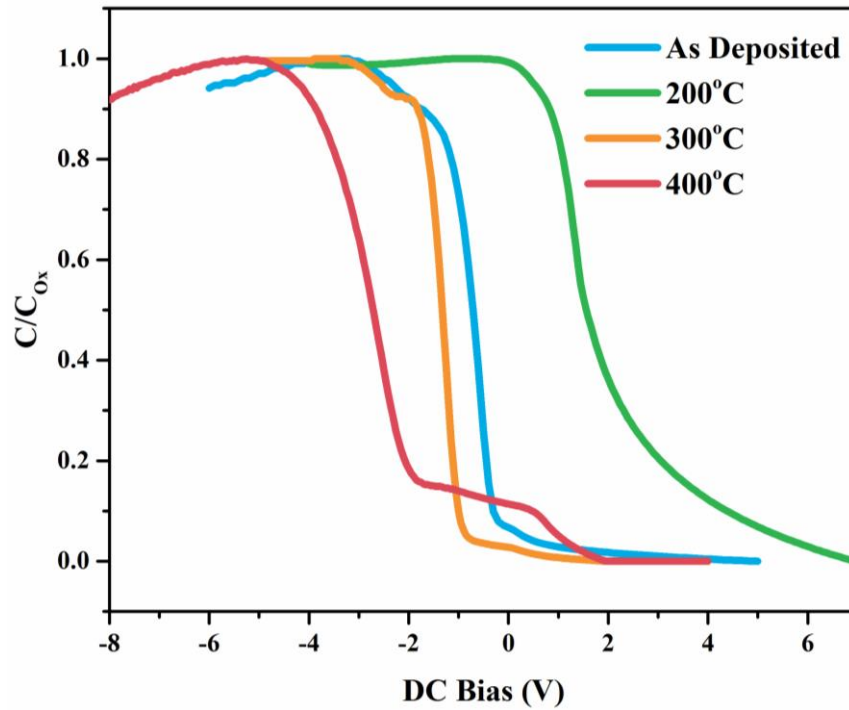


Figure 37. Normalized C-V curves at 1 MHz AC modulation frequency of 90 nm p-type MoO_{3-x} – cSi MOS capacitors with different PDA temperatures.

induces oxygen vacancies which form gap states just below the fermi level energy within the band gap of MoO_{3-x} [55] [57]. These gap states can trap electrons[56]. Therefore, ϕ_{bi} of the as deposited 90 nm thick MoO_{3-x} /p-type cSi MOS capacitor shifts toward positive voltages with PDA at 200°C in the presence of electrons trapped within the MoO_{3-x} gap states originated from oxygen vacancies. Formation of gap states within MoO_{3-x} increases fermi level of MoO_{3-x} [55]. Reduction in ϕ_b with PDA can be caused by the increment of fermi level of MoO_{3-x} . E_g of the as deposited sample and the PDA at 200°C are almost identical as show in Table 1 which suggests that MoO_{3-x} is still keeps its amorphous nature with PDA at this temperature. PDA at temperatures > 200°C results in phase transformation and crystallization of MoO_{3-x} [57]. On the other hand, measured E_g of MoO_{3-x} drastically increased with PDA at 300°C and 400°C due to crystallization and phase transformation.

R_s of the 90 nm thick MoO_{3-x} /p-type cSi MOS capacitor increased with PDA at 200°C which may be related to increased electron trapping at the MoO_{3-x} gap states. However, the R_s reduced significantly with PDA at 300°C and 400°C.

The effect of PDA on conductance response as a function of applied bias voltage for 90 nm thick MoO_{3-x} is shown in Figure 38. G values of the 90 nm thick MoO_{3-x} / p-type cSi MOS capacitor increase with PDA at 300°C and 400°C. Due to partial crystallization of the MoO_{3-x} at high PDA temperatures, structural defects are induced. Due to the leakage conductance from defects, high G values are observed. A sharp peak at ~1.5 V appears which is an indication of high D_{it} localized near to cSi CB edge[26]. On the hand, G of the MOS capacitor decreases after PDA at 200°C. Since the fermi energy MoO_{3-x} increases respect to vacuum level[55] by introduction of the gap states into the MoO_{3-x} band alignment of the cSi – MoO_{3-x} changes. This case is illustrated in Figure 39 with E_f and band alignment suggestion from literature[51],[55], [56],[67]. In Figure 39(a), electron injected from gate to MoO_{3-x} faces a potential barrier at the MoO_{3-x} – Si interface. Once they have enough energy to overcome the barrier, electron from MoO_{3-x} are conducted to Si or they can recombine with the hole in the VB of MoO_{3-x} . On the other hand, holes on VB of Si cannot be injected through MoO_{3-x} since there exist a vast potential difference between VB of MoO_{3-x} and Si.

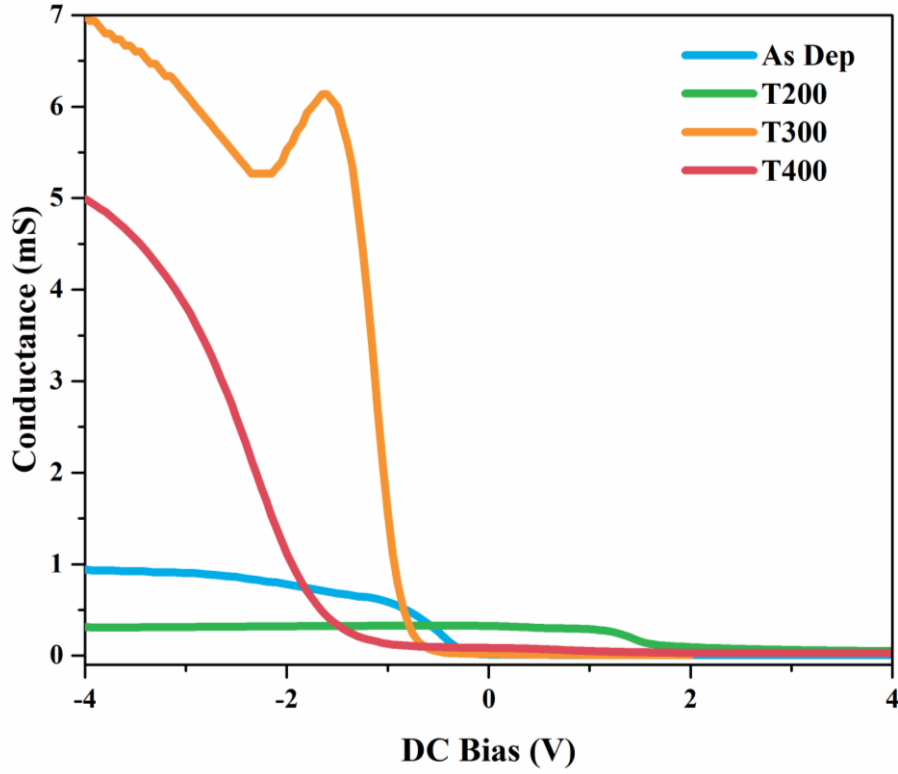


Figure 38. G-V curves at 1 MHz AC modulation frequency of 90 nm p-type MoO_{3-x} – cSi MOS capacitors with different PDA temperatures.

Therefore, conduction is dominated by electronic conduction. However, when the gap state exist, position of the fermi levels MoO_{3-x} and cSi change as discussed previously. After alignment of E_f between MoO_{3-x} and cSi is established, the band discontinuity can be increased at CBs of MoO_{3-x} and cSi (Figure 39(b)). Furthermore, potential gradient exist between CB of MoO_{3-x} and VB of the cSi due to broken MoO_{3-x} – p-type cSi junction, which causes flow of electrons from CB of MoO_{3-x} trough VB of cSi and holes from VB of cSi to CB of MoO_{3-x} . Growing potential gradient between CB of MoO_{3-x} and VB of the cSi due to E_f alignment after PDA at 200°C may be contribute. Similarly, decrease in C_{ox} with PDA at 200°C (Table 4) is originated from the transport of accumulated holes beneath the MoO_{3-x} – cSi interface via gap states. In figure 39(c), origin of hole selectivity of MoO_{3-x} at the open circuit condition is illustrated. A created electron – hole pair near the junction faces different potential barriers. Electrons on the CB of Si cannot be conducted if they don't have enough energy.

However, holes on VB of cSi can be transferred via induced gap states through the gate. In addition, holes in VB of cSi can be flow through MoO_{3-x} by recombining with electrons on CB of MoO_{3-x} to recombination via broken junction which may be the reason conduction decrease.

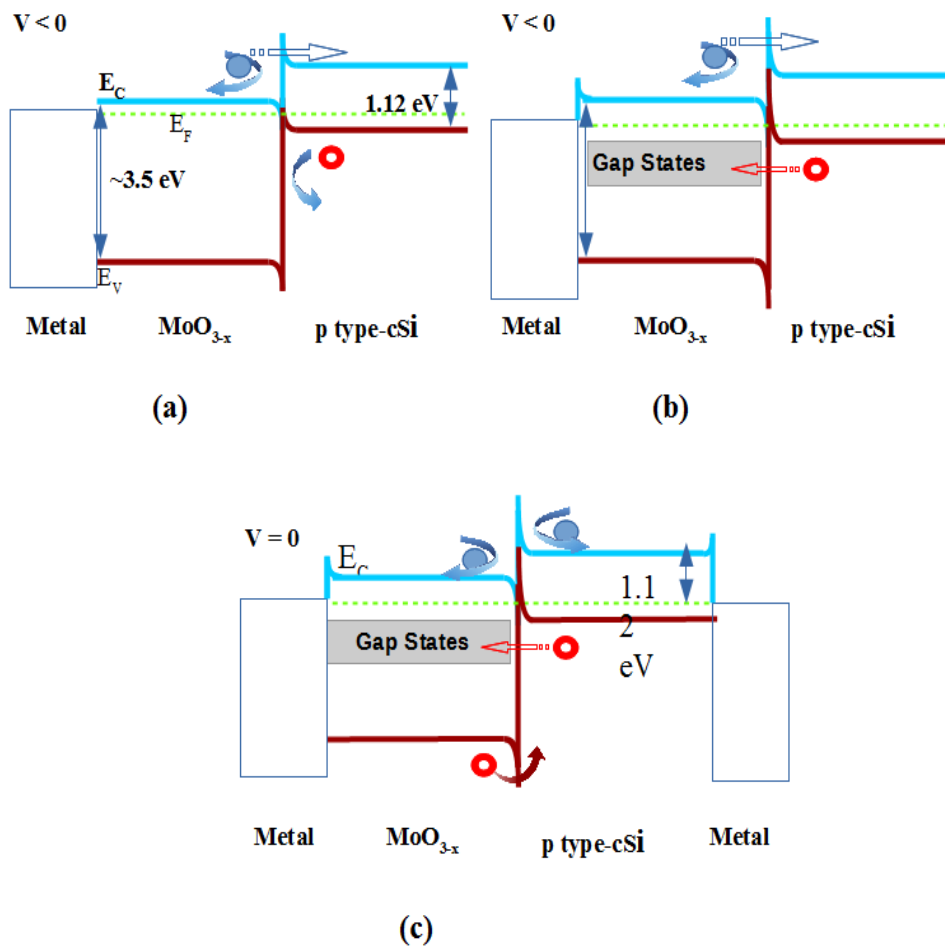


Figure 39. Separation of charge carrier on the carrier bands of $\text{MoO}_{3-x}/\text{c-Si}$ n-p anisotype heterojunction under negative DC bias (a) without gap states (b) with gap states, and (c) without applying DC bias in the presence of gap states.

CHAPTER 4

CONCLUSIONS

In this study, the effect of film thickness, deposition and post deposition condition on electrical transport properties of electron selective atomic layer deposited TiO_{2-x} /n-type cSi and hole selective thermally evaporated MoO_{3-x} /p-type cSi MOS capacitors were studied with electrical transport measurements (admittance and current voltage)

TiO_{2-x} /n-type cSi MOS capacitor produced with ALD technique with seven different substrate temperatures; 50°C, 80°C, 100°C, 150°C, 200°C, 250°C, and 300°C. Furthermore, effect of the PDA at 300°C and 350°C was examined on TiO_{2-x} / n-type cSi MOS capacitor with ALD temperature of 250°C. HF capacitance hystereses are observed for all the MOS capacitors which are due to the presence of interface trapped charges. We have obtained D_{it} values in the range of $\sim 10^{12} \text{ eV}^{-1}.\text{cm}^{-2}$ and shown that TiO_{2-x} - cSi interface trap density decreases down to $1.90 \times 10^{12} \text{ eV}^{-1}.\text{cm}^{-2}$ with proper substrate deposition and PDA temperatures. Similarly, R_s of the samples measured under the accumulation regime decreases with increasing the deposition temperature. A regular trend in the ϕ_{FB} of TiO_{2-x} / n-type cSi MOS capacitor was not observed, yet significant changes in ϕ_{FB} values were observed with PDA which can be attributed to the annealing-induced structural and morphological modifications in TiO_{2-x} . The $J_{leakage}$ values of the MOS capacitors vary with deposition temperature, thermal annealing, and substrate type in the $\sim 10^{-3}$ - $10^{-7} \text{ A.cm}^{-2}$.

MoO_{3-x} /p-type cSi MOS capacitors were produced with thermal evaporation technique with 3 different MoO_{3-x} thicknesses of 20 nm, 40 nm, and 90 nm. In order to see effects

of PDA, 90 nm thick MoO_{3-x} /p-type cSi MOS capacitors was annealed at 200°C, 300°C, and 400°C. It has been revealed that, 90 nm and 40 nm thick MoO_{3-x} on p-type cSi wafers have similar series resistance while 20 nm thick sample shows lower series resistance. Series resistance increases with the annealing temperatures. Density of interface trapped charges reduced from $9.46 \text{ eV}^{-1}\text{cm}^{-2}$ with PDA at 200°C while increased to $27.32 \text{ eV}^{-1}\text{cm}^{-2}$ and $20.85 \text{ eV}^{-1}\text{cm}^{-2}$ with PDA at 300°C and 400°C, relatively. In addition, a ϕ_{FB} shift toward the positive voltages with PDA at 200°C is observed which is an indication of electron trapping in the gap states of MoO_{3-x} . Annealing at elevated temperatures; above 300°C, alters the nature of MoO_{3-x} as it starts to behave as an insulator accompanied by an increase in energy bandgap as demonstrated from UV-VIS and SE analysis.

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