# A LOW POWER INTEGRATED TEMPERATURE SENSOR WITH DIGITAL OUTPUTS FOR ON-CHIP TEMPERATURE MONITORING APPLICATIONS

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## ABSTRACT

### A LOW POWER INTEGRATED TEMPERATURE SENSOR WITH DIGITAL OUTPUTS FOR ON-CHIP TEMPERATURE MONITORING APPLICATIONS

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This thesis presents the design and implementation of a low power temperature sensor with digital outputs for on-chip temperature monitoring applications. The temperature sensor is based on the substrate bipolar transistor which generates the bandgap reference voltage and proportional to absolute temperature (PTAT) voltage. The bandgap reference voltage is temperature and supply independent thus it is used to generate the reference signals for Analog to Digital Converter (ADC), while the PTAT voltage generated by the temperature sensor is connected to the input of the ADC. The ADC is implemented with a Successive Approximation Register (SAR) ADC, which converts the analog temperature signal to a 12-bit digital data. The SAR ADC with a split capacitive array Digital to Analog Converter (DAC) is chosen for low power and low area advantages for medium resolution applications. All the bias voltages and bias currents are generated with respect to the reference currents that are generated from the bandgap voltage. The configuration of the bias signals and operation specifications are all configurable through the Serial Programming Interface (SPI). The digital controller provides the communication with external electronics through SPI, controlling the process parameters via configuration memory and on-chip calibration.

The on-chip calibration is designed to compensate the errors coming from predominantly small temperature variations of the ADC bias voltages generated in the bias generator, ADC noise, comparator offset voltage, and nonlinearity of PTAT voltage. The output data format is a serial 12-bit data generated by the output serializer block. The number of output pads decreased by a serializer block, reducing the required power and area. The external pins include only power and SPI communication pins.

The operation region of the temperature sensor is between -55 ºC to 125 ºC. A resolution of 0.08 ºC is achieved by the 12-bit SAR ADC. The total power consumption of the full chip is at most 2 mW with a 3.3 V power supply. The full chip is designed and implemented using a 0.35 μm CMOS process in an area of the 2 mm × 2 mm, and it is submitted to a multi-project wafer (MPW) run for fabrication.

Keywords: On-chip thermal monitoring, BJT-based temperature sensor, SAR ADC, parasitic bipolar transistor, serializer

# ÖZ

## SICAKLIK GÖZLEMLEME UYGULAMALARI İÇİN DÜŞÜK GÜÇ TÜKETİMLİ SAYISAL ÇIKIŞLI TÜMLEŞİK SICAKLIK SENSÖRÜ

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Tez Yöneticisi : Prof. Dr. Tayfun Akın

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Bu tez çip içinde sıcaklık görüntüleme uygulamaları için düşük güç tüketimli sayısal çıkışlı sıcaklık sensörü tasarım ve uygulamasını sunmaktadır. Sıcaklık sensörü mutlak sıcaklığa orantılı voltaj üreten dikey bipolar tranzistorlü band aralığı referans kavramı baz alınarak tasarlanmıştır. Band aralığı referans voltajı sıcaklık ve güç değişiminden etkilenmez, bu yüzden analog-sayısal çevirici için referans voltaj ve akım üretmede kullanılır. Analog-sayısal çeviricinin girişine sıcaklık sensörü tarafından mutlak sıcaklığa orantılı üretilen voltaj uygulanır. Analog sıcaklık sinyalini 12-bitlik veriye çevirmek için ardışık yaklaşıklama kaydedicili analog-sayısal çevirici tasarlanmıştır. Ayrık kapasitör dizilişli sayısal-analog çevirici yapısı orta çözünürlük uygulamalarındaki düşük güç ve küçük alan avantajından dolayı ardışık yaklaşıklama kaydedicili analog-sayısal çevirici için seçilmiştir. Tüm voltaj ve akım kutuplama sinyalleri kutuplama bloğu tarafından band aralığı referans voltajı baz alınarak üretilmiştir. Kutuplama sinyalleri ve işlem isterleri seri programlama arayüzü kullanılarak yapılandırılır. Sayısal denetleyici bloğu seri programlama arayüzü vasıtasıyla dışarıyla iletişimi, işlem değişkenlerinin kontrollerini ve çip içinde kalibrasyon sağlar. Çip içinde yapılan kalibrasyon çoğunlukla analog-sayısal çevirici

için kutuplama bloğu tarafından üretilen sinyallerin sıcaklıkla değişmesinden kaynaklanan sapmaları, analog-sayısal çevirici gürültüsünü ve karşılaştırıcı devresinde oluşan sapma voltajını denkleştirir. Çıkış verisi çıkış sıralandırıcısı tarafından seri 12- bit veri formunda üretilir. Sıralandırıcının çıkış ped sayısını azaltması güç ve alan kazandırır. Dış pinler sadece güç ve seri programlama arayüzü pinleridir.

Sıcaklık ölçüm aralığı olarak -55ºC-125ºC sıcaklık bandı referans alınmıştır. 12-bit ardışık yaklaşıklama kaydedicili analog-sayısal çeviricisiyle 0.08 ºC çözünürlük elde edilmiştir. Toplam güç tüketimi kutuplama devresi hariç 3.3 V güç kaynağında 2 mW'tır. Tüm çip 2 mm × 2 mm alana 0.35 μm CMOS teknolojisi kullanılarak gerçekleştirilmiş ve üretime gönderilmiştir.

Anahtar kelimeler: Çip içinde sıcaklık görüntüleme, BJT-tabanlı sıcaklık sensörü, ardışık yaklaşıklama kaydedicili analog-sayısal çevirici, parasitic bipolar transistor, sıralayıcı

*To my family and fiancée*

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# CHAPTER 1

# INTRODUCTION

Temperature sensors have very important role in various systems as most of the systems exhibits temperature dependence. Temperature measurement and control are fundamental features since characteristics of many electronic and mechanical systems differ with temperature. Therefore, temperature monitoring is essential for compensating the temperature sensitivity, for preventing the thermal damage, and for ensuring the safety of the systems.

The electronic industry developed enormously since the invention of the first transistor. Behavior characteristics of the semiconductor materials transform the high-end technology entirely. There is a rapid transform of electronic devices which are in use in everyday life. Unfortunately, performance of semiconductor materials presents extensive temperature dependency. Temperature impacts on semiconductor characteristics caused influences on speed, power, and system reliability [1]. As a result, monitoring temperature of the system provides control on the process and sustains desired performance. Hence, the demand for low cost, high performance, and small area temperature sensor is increasing. This thesis study presents the design and implementation of a low power digital output temperature sensor for on-chip thermal monitoring applications.

Chapter 1 summarizes the comparison of common temperature sensors, then explains the basic operation principle of the CMOS smart temperature sensor developed in this

thesis. Then, Chapter 2 analyzes the design of a low power BJT-based temperature sens**o**r with digital outputs. Chapter 3 presents the implementation of proposed temperature sensor. Chapter 4 introduces the simulation results and system verification and comparison of proposed temperature sensor with similar works in the literature. Chapter 5 summarizes the proposed work and listed the future works for the implemented temperature sensor.

## 1.1 Temperature Sensing

The importance of measuring the temperature rises from the fact that many processes are temperature dependent. Most of the production plants and systems need temperature monitoring to guarantee the process reliability, prevent the failure of the costly system equipment. Temperature sensors are fundamental for various fields for example processed food industries, nuclear plants, automotive hood monitoring, chemical handling, medical devices, and microprocessors. Various types of temperature sensors have been developed to meet the specific requirements of these application fields.

## 1.2 Temperature Sensors

Temperature sensor can be characterized with respect to their output signals, input signals, material types, and sensed object. Most commonly temperature sensors are divided into two categories namely, contact and noncontact temperature sensors.

Contact temperature sensors are in contact with the object sensed and use conduction method to sense the temperature change. Sensor and the object whose temperature is measured are in thermal equilibrium. There are many contact temperature sensors and the most popular ones are Thermocouple, Resistive Temperature Device (RTD), Thermistor, and Integrated Silicon Based sensors.

Noncontact temperature sensors use convection and radiation to monitor the temperature without the need of thermal equilibrium between the sensor and the object. They are mostly preferred when the object is moving, inaccessible, or making contact cause error by changing the temperature or damaging the object or sensor. Pyrometers,

line-scanners, infrared thermometers, thermal imagers are the most popular noncontact temperature sensors [2].

These two basic categories can be divided into sub categories; electro-mechanical, resistive and electronic [3]. In this chapter most popular contact temperature sensors will be explained in detail with their advantages and disadvantages.

### 1.2.1 **Thermocouple**

A thermocouple is composed of at least two dissimilar metals joined together to form two junctions. One junction is used as a reference temperature and the other one is the measuring junction. The difference between the thermal characteristics of two dissimilar metals is used to sense the temperature variation. When two dissimilar metals are bend together there is a continuous current flow leading to the voltage generation that can be correlated with the temperature.

The measurement circuit can be seen in Figure 1.1. Temperature measurement is done at the junction point of the metal lines.

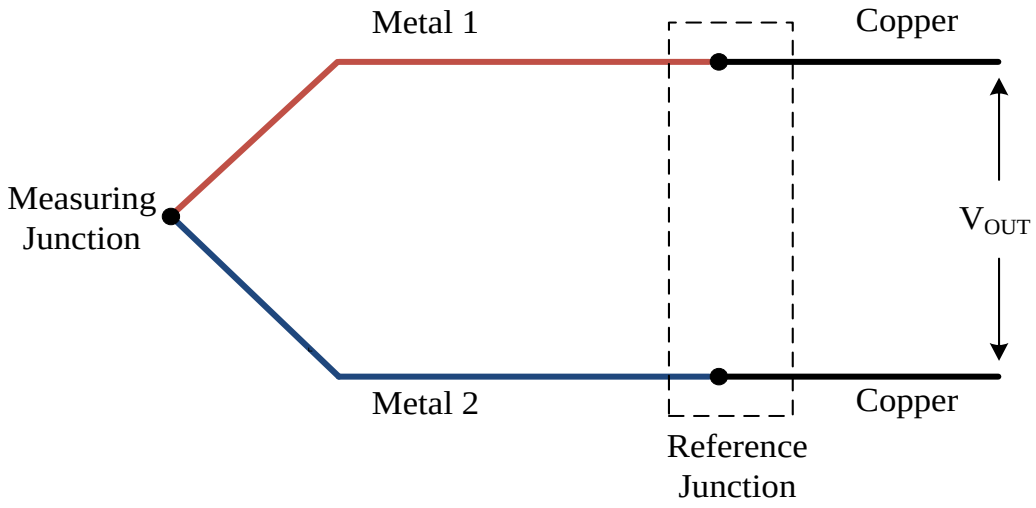


Figure 1.1 Thermocouple temperature measurement circuit

Thermocouples have a wide range of temperature measurement, small size and low cost but highly nonlinear with respect to thermistor, RTD and CMOS sensors.

Thermocouples need good protection as thermal characteristics of the metals can change with stress or bending.

### 1.2.2 Resistance Temperature Detector (RTD)

Resistance temperature detectors consist of a material that has an accurate known resistance to temperature relationship generally, platinum, copper or nickel. RTDs do not need a reference temperature, they sense the absolute temperature.

It is fundamental to emphasize on the platinum resistive thermometers for their excellent thermal characteristics. Thermal characteristics of the platinum is the most stable over the largest temperature range. Platinum resistance thermometers provide the most accurate, reliable, and stable results and they are easy to use. The most preferred RTD is Pt-100 that has a 100 ohms at 0℃ [4]. The main error comes from the electrical design of the RTD which is self-heating of the generated current on the material.

### 1.2.3 Thermistor

Thermistors whose electrical resistance changes with the temperature, divided into two groups namely Negative Temperature Coefficient (NTC) and Positive Temperature Coefficient (PTC). Thermistors have very high resistance change per degree of temperature resulting a high sensitivity. On the other hand, self-heating is a bigger problem due to the high resistance change.

### 1.2.4 Integrated Circuit Temperature Sensors

Integrated circuit (IC) technology has developed far since the invention of the first transistor in 1947. IC technology has a revolutionary effect on the electronic industry: cost and performance are the main advantages. Today we see the ICs everywhere, computers, mobile phones, cars; mainly in almost every modern electrical device.

The advantages of the IC temperature sensor come from its easy implementation with the other ICs and user friendly output forms. On-chip thermal monitoring provides the

required data to the thermal management system in order to maintain thermal protection of the silicon ICs. Thermal protection prevents the irreversible damages and decrease of expected lifetime of the silicon ICs.

On-chip thermal monitoring IC temperature sensors are usually classified as its input source and output signaling. IC's own package temperature is generally used as input temperature source and there are three types of output signaling method; analog, logic, and serial digital output. Analog output systems need an external ADC to integrate another IC. As a result, analog output temperature sensors increase cost, area consumption, and reduce the ease of integration. On the other hand, digital output temperature sensor provides high integrity, low cost, simple external circuit, and smartness.

The smart IC temperature sensors is achieved by integration with analog to digital converter (ADC) which sustain easy interfacing with the Very Large Scale Integration (VLSI) circuits [5]. Figure 1.2 gives the basic diagram of the integration of the smart temperature sensor [6].

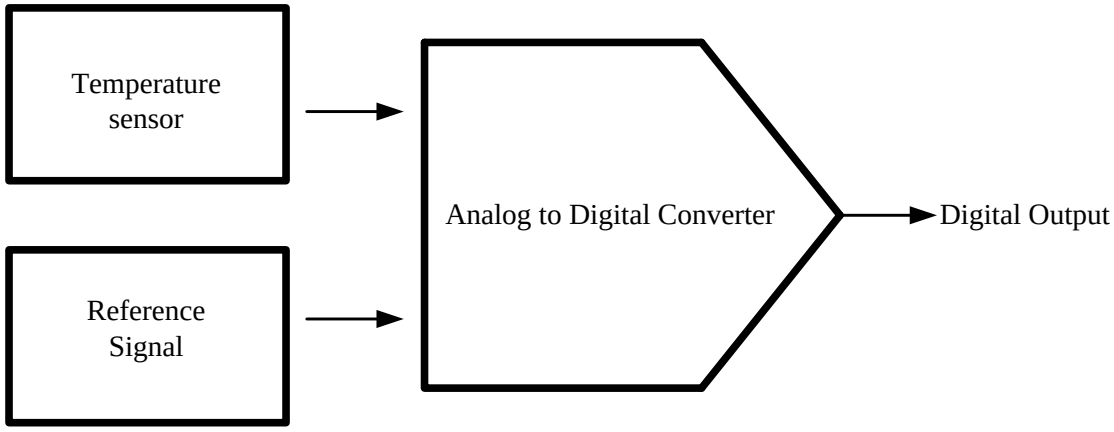


Figure 1.2 Smart temperature sensor integration diagram.

Smart temperature sensors can be used with the other ICs or placed on-chip. As a consequence, sensors are required to be small in size, low power, and low cost. The other common specifications of the smart temperature sensors are accuracy, resolution, supply voltage, supply current, speed, and temperature range.

In this work CMOS process is used for realization of smart temperature sensor on the grounds that CMOS technology provides low cost, high functionality, and robustness.

## 1.3 Comparison

Table 1-1 shows the comparison between the most common temperature sensors used in the industry [7]. In comparison with the other temperature sensors, silicon based temperature sensors are not the best regarding the temperature range, accuracy, and sensitivity. Yet their high performance with low cost, user-friendly output formats, integrity with the other ICs, and high stability at extreme environmental conditions over their lifetime make them number one choice. Additionally, they do not need cold-junction compensation or complicated linearization.

IC temperature sensors can be placed into the hot spots contrary to the other temperature sensors. For instance, almost all of the Central Processing Units (CPUs) use the remote sensing IC technology. In remote sensing technology, a transistor is placed in the CPU and the measured temperature signal is connected the temperature sensor block away from the CPU.

Furthermore, output signals of the sensor can be programmable by additional blocks and system gets smarter. Smart temperature sensors do not only measure the temperature but also take action in the system. For instance; sensors send the signals to cooling fan in devices, reduce the clock frequency in order to save power or stop the clock when the undesired temperature condition arises. In short smart temperature sensors guarantee the system to work in the safe temperature range.

All in all, smartness, cost and easy integration with other ICs make the IC temperature sensor at the very top of the list despite the small temperature range and comparably low accuracy.

Table 1.1 The comparison of the main characteristics of the common temperature sensors [7].

| | **Thermocouple** | **RTD** | **Thermistor** | **Silicon Based IC** |
|---|---|---|---|---|
| **Temperature Range** | -270 -1800 ºC | -250-900 ºC | -100-450 ºC | -55-150 ºC |
| **Accuracy** | 0.5 ºC | 0.01 ºC | 0.1 ºC | 1 ºC |
| **Sensitivity** | 10s of μV / ˚C | 0.00385 Ω / Ω / ˚C (Pt) | several Ω / Ω / ˚C | -2 mV/°C |
| **Linearity** | Requires at least a 4th order polynomial or equivalent look up table | Requires at least a 2nd order polynomial or equivalent look up table | Requires at least 3rd order polynomial or equivalent look up table | At best within ±1°C. No linearization required. |
| **Ruggedness** | The larger gage wires of the thermocouple make this sensor more rugged. Additionally, the insulation materials that are used enhance the thermocouple's sturdiness. | RTDs are susceptible to damage as a result of vibration. This is due to the fact that they typically have 26 to 30 AWG leads which are prone to breakage. | The thermistor element is housed in a variety of ways, however, the most stable, hermetic Thermistors are enclosed in glass. Generally, thermistors are more difficult to handle, but not affected by shock or vibration. | As rugged as any IC housed in a plastic package such as dual-in-line or surface outline ICs. |
| **Excitation** | None Required | Current Source | Voltage Source | Supply Voltage |
| **Form of Output** | Voltage | Resistance | Resistance | Voltage, Current, or Digital |
| **Cost** | $1 to $50 | $25 to $1000 | $2 to $10 | $1 to $10 |

## 1.4 CMOS Smart Temperature Sensor

There are four main smart temperature sensor architectures in CMOS process namely, MOS transistors-based architecture, ring oscillator, propagation delay, and BJT based temperature sensors.

### 1.4.1 MOSFET-Based Temperature Sensors

In CMOS process, two of the temperature dependent characteristics of MOSFETs can be used. One is the variation of the mobility and the other one is the decrease of the threshold voltage with respect to temperature. However, both of these variations are quite nonlinear and process and technology dependent. Therefore, MOSFETs are not preferred for high accuracy sensors.

When MOSFET is biased at zero temperature coefficient point in sub-threshold region, bias current of the MOSFET is constant with respect to temperature and linear relation between the gate-source voltage and temperature is achieved. This relation can be written as follows

$$V_{GS} - V_T = \frac{\eta kT}{q} ln\left(\frac{I_D}{I_0}\right), \tag{1.1}$$

where $I_0$ is a process dependent parameter and ŋ is the subthreshold slope factor [8].

In addition, MOSFETs can replace the BJTs in generation of proportional to absolute temperature voltage architectures. Inaccuracy of this architecture can be decreased to ±2℃ in a limited temperature range from 10℃ to 80℃ [9].

### 1.4.2 **Ring Oscillator**

Ring oscillator senses temperature due to its frequency dependency to temperature. Ring oscillators generally consists of odd numbers of inverters. The frequency of the ring oscillator can be obtained as linearly proportional to temperature by arranging the width and length of the MOSFET transistors in inverter chain [10]. Generated voltage pulse is transmitted to time-to-digital controller rather than analog-to-digital converter. Figure 1.3 shows the basic block diagram of a ring oscillator temperature sensor [11].

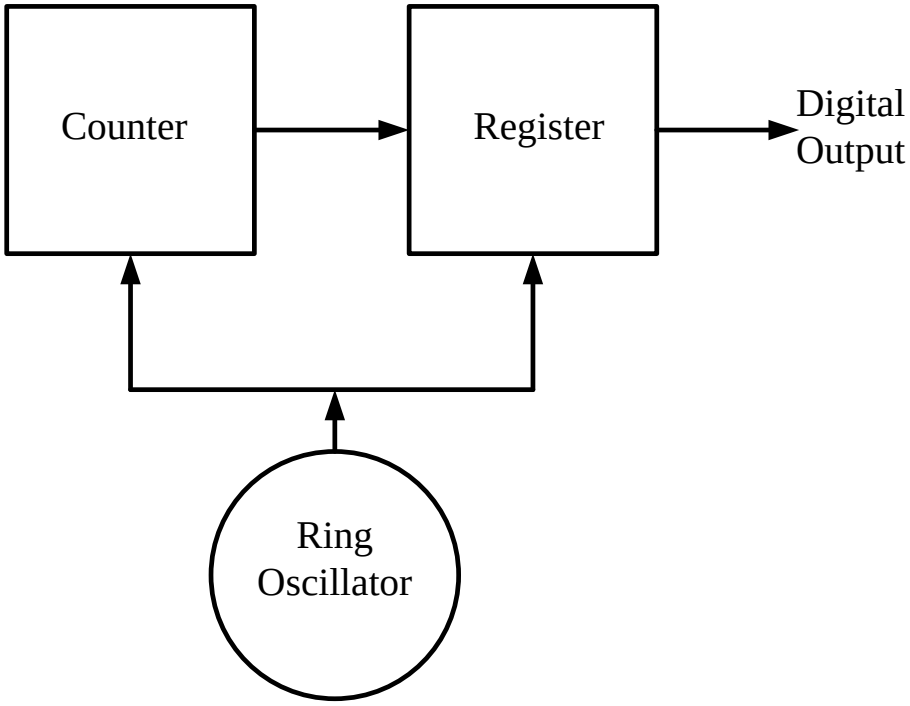


Figure 1.3 Basic diagram of a ring oscillator temperature sensor.

### 1.4.3 **Propagation Delay**

In this architecture, a delay which is proportional to the temperature is generated by chain of delay cells. This output delay signal is connected to cyclic Time-to-Digital Converter which digitalize the input signal according to the pulse width [12]. Figure 1.4 shows the basic design structure of propagation delay temperature sensor.

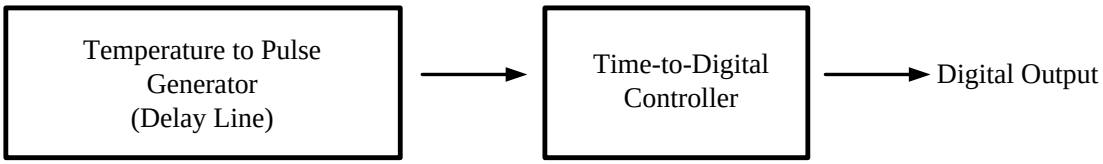


Figure 1.4 Basic diagram of temperature propagation delay-based temperature sensors.

Temperature range of the propagation delay oscillators is limited and propagation delay oscillators provide low resolution.

Table 1.2 presents the performance parameters of the CMOS smart temperature sensors. BJT-based temperature sensors provide widest temperature range of operation with a high resolution and accuracy with respect to other CMOS temperature sensors. On the ground of these advantages BJT-based temperature sensor is presented in this work.

Table 1.2 Comparison of the smart CMOS temperature sensors [13].

| | **BJT** | **MOSFET** | **Propagation Delay** | **Ring Oscillator** |
|---|---|---|---|---|
| Temperature Range (℃) | -50 - 150 | -10 to 70 | 0 to 70 | 0 to 70 |
| ADC Integration | Yes | Yes | No | No |
| Resolution (℃) | ±0.05 | ±0.1 | +0.5 | ±0.5 |
| Accuracy (℃) | ±1 | >±1 | ±1 | Unknown |
| Power Consumption | High | Low | Medium | Low |

### 1.4.4 **BJT-Based Smart Temperature Sensor**

Fortunately, implementation of the bipolar transistor in standard CMOS process is possible. Experimental investigations about the temperature characteristics of the bipolar transistors were carried out by Wang and Meijer [14]. The results of the experiment are quite surprising. Bipolar transistors which are fabricated in CMOS technology have similarly useful voltage-current characteristics for temperature sensing as bipolar transistors fabricated in bipolar technology. CMOS technology is more preferable due to its low cost and easy integration with VLSI circuits.

There are two types of BJTs; lateral bipolar transistors and substrate transistors. Temperature characteristics of the substrate bipolar transistors are more ideal than the lateral bipolar transistors. The relation between the base-emitter voltage and collector current is more steady. Moreover, the stress tolerance of substrate bipolar transistor is higher than the lateral bipolar transistor [15]-[17].

The main principle behind the temperature sensing of bipolar transistor is the temperature characteristics of base-emitter voltage. The base-emitter voltage equation can be written as,

$$V_{BE} = \frac{kT}{q} ln\left(\frac{I_C}{I_S}\right), \tag{1.2}$$

where $q$ is the electron charge, $k$ is the Boltzmann's constant, $T$ is the absolute temperature, $I_C$ is the collector current and $I_S$ is the saturation current [8]. As seen from the equation 1.2 $V_{BE}$ is linearly dependent to absolute temperature under constant saturation and collector currents. Yet, saturation current is temperature dependent and this dependency is deeply explained in Chapter 2.

Base-emitter voltage of the BJT is also process dependent on the basis of the fact that there may be material, geometrical, and process variations during the manufacturing process. The saturation current of the BJT dependent to many parameters such base-emitter area, temperature, intrinsic carrier concentration, and so on. The proportional saturation currents for two BJTs fabricated by the same process are achieved by proportional base-emitter area selection. On the other hand, proportional collector

currents are obtained in many ways. One of the basic method is arranging the transistor ratios which are biased with same supply voltages.

Fortunately, by subtracting two base-emitter voltages having proportional saturation and collector currents from each other, process independent yet temperature dependent voltage signal is obtained. The achievement of this difference voltage is analyzed in Chapter 2 in detail. This base-emitter voltage difference can be obtained by applying:

i. Two different emitter currents to a transistor with the help of a switch,
ii. Two different emitter currents to two identical transistors which are connected side by side,
iii. Same emitter currents to two transistors with different emitter areas,
iv. One constant current source to one transistor and same constant current source other transistor having N multiple of the base-emitter area [18].

Generation of $\Delta V_{BE}$ according to these methods is given in Figure 1.5.

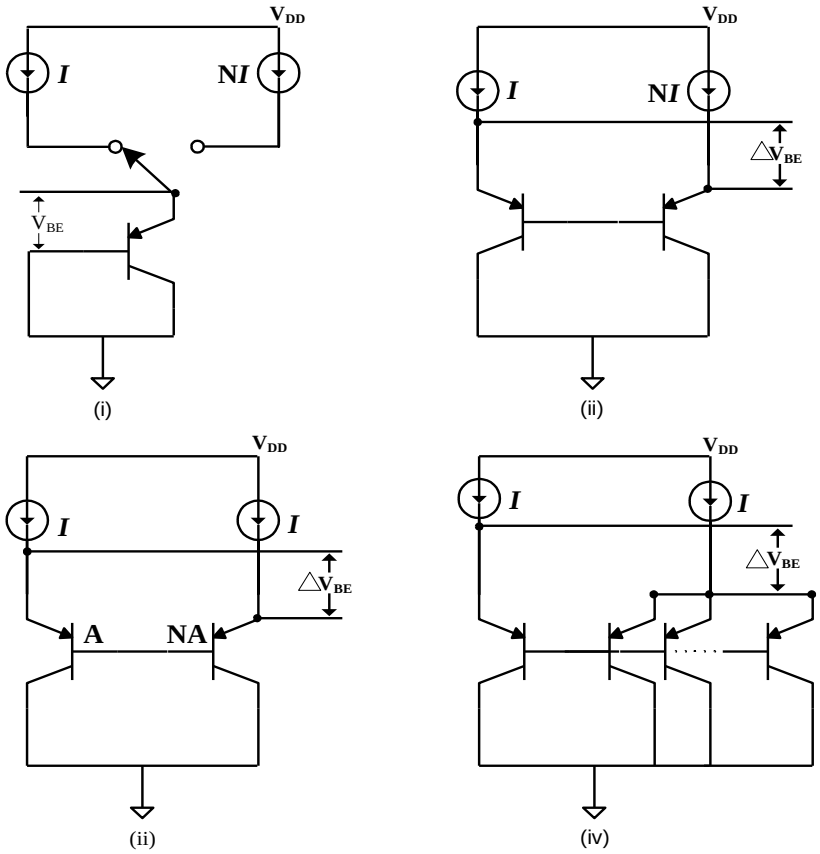


Figure 1.5 Generation of the $\Delta V_{BE}$ applying (i), (ii), (iii), and (iv) consecutively.

The introduced techniques shown above for difference voltage generation is basis of the temperature sensing. This voltage can be converted to current by a simple circuit modification. The voltage or current proportional to absolute temperature is the input of the ADC. ADC digitizes that analog signal to N-bit data where N is determined according to the resolution specification of the system. ADC converts the input signal by comparing the reference signal. Any variation in reference signal directly changes the output data therefore, reference voltage needs to be constant during the conversion time. Hence, it is absolutely critical to obtain temperature, supply, and process independent reference voltage.

Surprisingly, bipolar transistors introduce both negative and positive temperature dependent characteristics which are called negative temperature coefficient (NTC) and positive temperature coefficient (PTC) respectively. By the summation of these two TC with appropriate constants temperature independent reference voltage is obtained as can be seen in Figure 1.6.

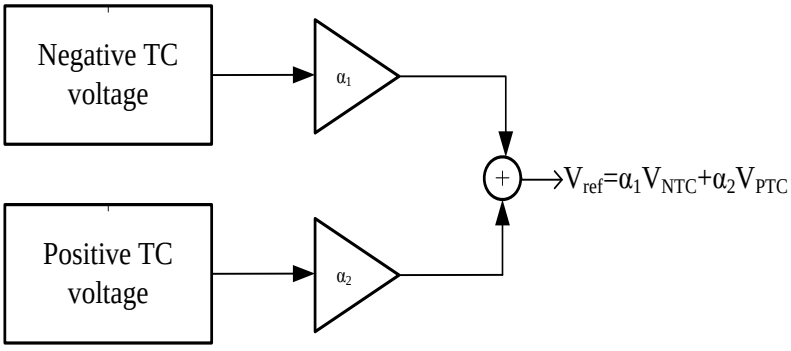


Figure 1.6 Bandgap reference generation technique.

Both of the reference and temperature voltages are obtained with respect to the temperature behavior characteristics of the BJT. Hence temperature characteristics are analyzed in detail in Chapter 2.

There are several ADC types in the literature. The ADC selection is determined considering the ADC parameters; resolution, speed, accuracy, power consumption, area, and circuit complexity. Figure 1.7 shows the distribution of the ADC selection with respect to the market segments, sampling rate, and resolution.

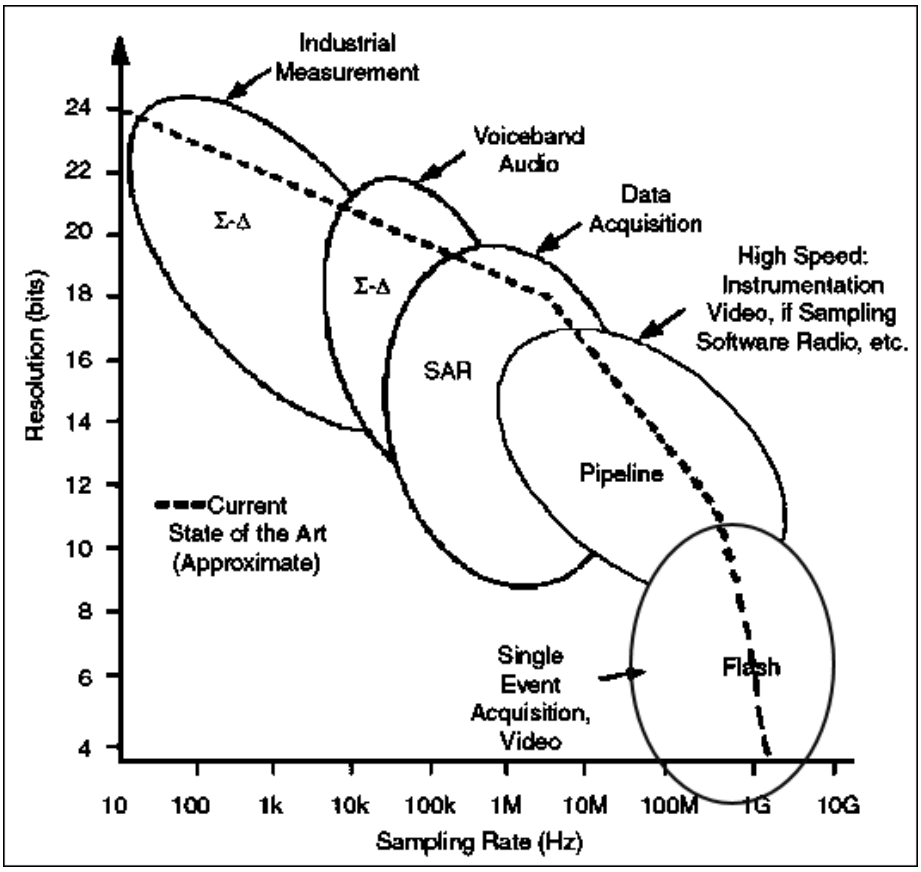


Figure 1.7 ADC architecture, applications, resolution, and sampling rates [19].

Temperature of the chip does not change rapidly therefore high speed ADCs are not in scope. There is a positive correlation between the high resolution and power consumption. However, low power consumption is priority of this work therefore high resolution ADCs which dissipate high power is removed from selection. Thus, Successive Approximation Register (SAR) ADC is a reasonable choice for low power and relatively low sampling rates. The detailed design and implementation of SAR ADC is explained in Chapter 2 and Chapter 3.

On the grounds of what is mentioned above, temperature sensor gets critically important as it provides high performance with low cost and easy integration. The performance specifications of the designed smart temperature sensor are given in Table 1.3.

Table 1.3 Design specifications of the smart temperature sensor.

| | |
|---|---|
| **Technology** | 0.35 μm CMOS process |
| **Temperature Range** | -55 ℃ to 125 ℃ |
| **Accuracy** | ±0.5 ℃ |
| **Resolution** | 0.08 ℃ |
| **System Clock Frequency** | 1 kHz |
| **Effective Sampling Rate** | 714 S/s |
| **Power Consumption** | ≤ 2 mW |

## 1.5 Applications

The application areas of silicon temperature sensors are overheating protection, transmission, heating and air-conditioning, white goods and power supplies, engine oil, and coolant. Due to the wide range of the application areas there are so many silicon temperature sensors in the industry. For instance, KTY81 and KTY82 silicon temperature sensor families which are produced by NXP founded by Philips Semiconductors provide accurate and reliable measurements throughout the car from air conditioning to engine cooling over the wide range of the temperature. Another example is Si705x digital temperature sensors produced by Silicon Labs with $I^2C$ interface which can be used in medical and computer equipments, battery protection and cold chain storage in addition to other application fields [20], [21].

## 1.6 Motivation of the Thesis

Up to now, different types of temperature sensors have been explained with their advantages and disadvantages. In addition, main characteristics of sensors are listed and comparison is stated according to performance parameters between silicon temperature sensor and other temperature sensors.

The advantage of the silicon temperature sensor is to integrate in the system level IC design. Furthermore; silicon temperature sensor has analog, logic, and serial digital output signal selections that make user-friendly output formats. Another great advantage of IC temperature sensor is its low cost.

The main purpose of this thesis is to design and implement a low power temperature sensor with digital outputs for on-chip temperature monitoring applications. This is realized with use of thermal characteristics of substrate bipolar transistors and integration with ADC. Furthermore, the other aim is to increase the smartness of the sensor by on-chip calibration method. Additionally, all bias voltage and currents are generated in chip so there is no need for any bias supply except from the power supply. The designed sensor can be implemented in micro bolometer-based readouts to measure the temperature in order to increase the control of operation parameters.

This thesis explains the design and implementation of a low power integrated temperature sensor with digital outputs for on-chip temperature monitoring application realized with a 0.35 μm CMOS process.

# CHAPTER 2

## SYSTEM DESIGN

The whole system consists of five blocks namely; temperature sensor and reference generation block, analog to digital converter, bias generator, digital controller, and output stage. Each of these stages will be explained in detail with its sub-blocks and details of the operation are analyzed.

The proportional to absolute temperature (PTAT) voltage is obtained with the structures mentioned in Chapter 1 and bandgap reference voltage is generated by the bandgap reference generation circuit. Bandgap reference voltage is used to generate reference voltage and currents for the ADC. The temperature voltage and reference voltages are connected to positive and negative inputs of the ADC respectively. ADC digitize the temperature voltage with 12-bit resolution in order to obtain 0.1℃ sensor resolution. The digitalized 12-bit data is sent to calibration block in digital controller. The calibration block is simple adder-subtracter block with a selection of twenty temperature regions multiplexer. 12-bit temperature data is calibrated according to the its temperature region and sends to output serializer block. Output serializer serializes the data and sends to output pads.

All necessary voltage and current bias signals for ADC are generated in bias generated block. Bias currents are generated for the comparator block in the ADC therefore they affect the gain of the comparison block. Furthermore, bias voltages are used for reference high and low voltages for the Digital to Analog Converter (DAC) array and common mode voltage. ADC performance is very dependent to bias signals since the

conversion result is determined according to reference voltages and gain of the comparator is important for least significant voltage distinguish. Hence, these bias signals must be temperature and supply independent for high accuracy of the system.

All timing signals are generated in the timing generator that is placed in the digital controller and transmitted to output serializer and the ADC. Temperature sensor is connected to the external electronics via Serial Programming Interface (SPI) block. SPI is a 4-wire architecture which enables the communication with outside world. All performance parameters of the sensor are configurable and they can be controlled via SPI block. SPI gets configuration data and timing data. SPI transmits configuration data which contains values of bias signals, operation select signals, and calibration logic to configuration memory. Furthermore, timing signals are transmitted to the timing generator and timing generator generates the necessary signals for operation. Figure 2.1 gives the block diagram of the whole system with a clear statement of the main connections between the blocks.

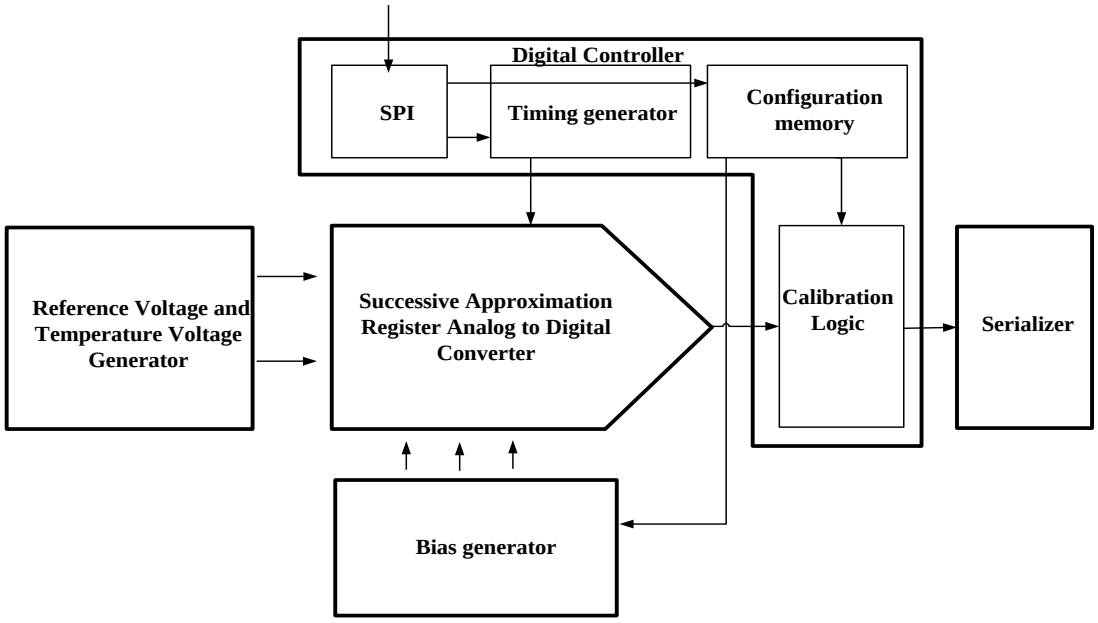


Figure 2.1 Top level block diagram of the proposed digital output temperature sensor architecture.

## 2.1 Temperature Sensor and Reference Generation Block

### 2.1.1 Temperature Sensor Voltage Generation

Temperature sensing is the most critical part of the design for accurate, sensitive, and linear system. CMOS temperature sensors mostly suffer from accuracy therefore temperature signal must carry the lowest noise as possible and have linear characteristics along the full temperature region.

In CMOS technology, sensing the temperature is feasible with lateral bipolar transistors and vertical bipolar transistors which are also known as substrate bipolar transistors [22].

As stated in the introduction part characteristics of lateral and vertical bipolar transistors are investigated and concluded that they can be used as temperature sensors in CMOS process. Substrate bipolar transistor has the most ideal voltage-current characteristics and the least stress dependency. The collector current equation of the bipolar transistor is described as,

$$I_C = I_S e^{\frac{qV_{be}}{kT}}, \tag{2.1}$$

where the $q$ is the electron charge, $k$ is the Boltzmann's constant, $T$ is the absolute temperature, and $I_S$ is the saturation current which is equal to

$$I_S = \frac{qAn_i^2\overline{D}}{W_B N_d}, \tag{2.2}$$

where the product of $W_B N_d$ is called the Gummel number $G_B$ expressing the number of impurities per unit area of the base width.

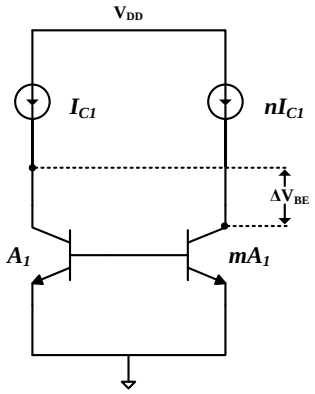


Figure 2.2 Base emitter voltage difference generation circuit.

If two BJTs which have the different base-emitter areas as $mA_1 = A_2$, biased at the different currents $I_{C1} = nI_{C2}$ as seen in Figure 2.2 the voltage difference across the base-emitter junction equals to

$$V_{BE_1} - V_{BE_2} = \frac{kT}{q} ln\left(\frac{I_{C1}}{I_{S1}}\right) - \frac{kT}{q} ln\left(\frac{I_{C2}}{I_{S2}}\right), \tag{2.3}$$

$$\Delta V_{BE_1} = \frac{kT}{q} ln\left(\frac{I_{C1}}{I_{S1}}\frac{I_{S2}}{I_{C2}}\right), \tag{2.4}$$

$$\Delta V_{BE_1} = \frac{kT}{q} \ln(mn). \tag{2.5}$$

This voltage drop is linearly proportional to the absolute temperature and called as PTAT voltage. For the moment voltage drop is assumed as ideal, non-idealities will be discussed in Chapter 3.

The difference voltage generation circuit must be modified in order to realize the circuit. For this purpose, the circuit topology in Figure 2.3 is used [23]. This circuit also forms the main principle of the temperature independent reference voltage generation which will be explained later. Here, the amplifier sets its input voltage at nearly equal values. Therefore, the difference voltage is occurred on $R_1$. The current flowing over the transistors is set by changing the $R_2$ and $R_3$ values. The derivation of the current flowing over $R_1$ can be calculated as follows;

$$\Delta V_{BE} = \frac{kT}{q} ln\left(\frac{I_{C1}}{I_{S1}}\frac{I_{S2}}{I_{C2}}\right), \tag{2.6}$$

$$\Delta V_{BE} = \frac{kT}{q} \ln\left(m\frac{R_3 + R_1}{R_2}\right), \tag{2.7}$$

$$I_{temp} = \frac{1}{R_1}\frac{kT}{q} \ln\left(m\frac{R_3 + R_1}{R_2}\right). \tag{2.8}$$

As derived in the equation 2.8 the current flowing over transistors is also proportional to absolute temperature which is called the PTAT current.

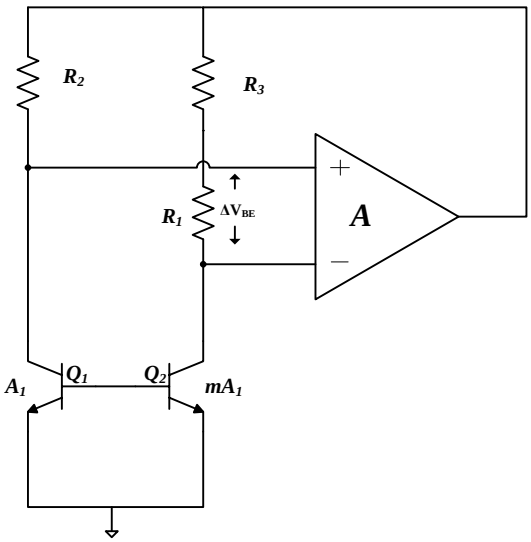


Figure 2.3 Conventional implementation of the circuit [23].

Up to this point the PTAT voltage and PTAT current generation circuits are analyzed in conventional ways in order to clarify the basic principle of the temperature sensor operation.

### 2.1.2 **Bandgap Reference Voltage Generation**

Generation of the PTAT voltage is one of the most critical part and the other one is the generation of the voltage reference. The reference voltage must be temperature and supply independent. Surprisingly, bipolar transistors have negative and positive temperature coefficients (TC). Hence by adding these two TCs with proper ratios temperature independent voltage can be obtained as reference voltage. It is noted that

process parameters are mostly temperature dependent, thus temperature independent reference voltage is inherently process independent as well.

#### 2.1.2.1 Negative Temperature Coefficient

The base-emitter voltage of the bipolar transistor has a negative TC. The known base-emitter voltage equation of the bipolar transistor can be written as

$$V_{BE} = V_T ln \frac{I_C}{I_S}, \tag{2.9}$$

where the thermal voltage $V_T = \frac{kT}{q}$ and equals to 26 mV at room temperature.

Negative TC is shown by taking the derivative of the $V_{BE}$ with respect to temperature:

$$\frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T} ln\left(\frac{I_C}{I_S}\right) - \frac{V_T}{I_C}\frac{\partial I_S}{\partial T}. \tag{2.10}$$

On the other hand, the effective hole diffusion constant $\overline{D_p}$ is related to the effective hole mobility $\bar{\mu}$ via the Einstein relation:

$$\overline{D_p} = \frac{kT}{q}\bar{\mu}. \tag{2.11}$$

When the effective hole diffusion constant is substituted in the saturation current equation given in the saturation current equation is written as;

$$I_S = \frac{kTAn_i^2(T)\overline{\mu_p}(T)}{G_B(T)}. \tag{2.12}$$

To go one step further temperature dependencies of each terms in the equation 2.12 must be investigated. Temperature relation of the intrinsic carrier concentration $n_i$ is given as;

$$n_i^2 \propto T^3 \exp\left(\frac{E_g(T)}{kT}\right), \tag{2.13}$$

where silicon bandgap energy $E_g \approx 1.12eV$ [23]. Additionally, the temperature dependency of the effective hole mobility is known as,

$$\mu_p \propto \mu_o T^{-m}, \tag{2.14}$$

where m is -3/2 and by inserting all parameters to equation 2.12 saturation current is obtained as

$$I_S = bT^{4+m} exp\left(-\frac{E_g}{kT}\right), \tag{2.15}$$

where b is a constant replaced for other constants [23].

Derivative of the saturation current is equal to;

$$\frac{\partial I_S}{\partial T} = b(4+m)T^{3+m} exp\left(-\frac{E_g}{kT}\right) - \left(\frac{E_g}{kT^2}\right) bT^{4+m} exp\left(-\frac{E_g}{kT}\right). \tag{2.16}$$

Inserting this derivation to equation 2.10

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_T}{T} ln \frac{I_C}{I_S} - (4+m)\frac{V_T}{T} + \frac{E_g}{kT^2} V_T, \tag{2.17}$$

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_{BE} - (4+m)V_T - E_g/q}{T}. \tag{2.18}$$

At T = 300°K, $V_{BE} \approx 750mV$, and negative TC is calculated as;

$$\frac{\partial V_{BE}}{\partial T} = -1.5mV/°\text{K}. \tag{2.19}$$

In practice, temperature gradient changes from -1.2 to -2.2 $mV/°$K as $V_{BE}$ varies with the bias current [18]. The absolute value of the negative TC increases with the decreasing collector current therefore low collector current is desirable as it boosts the sensitivity to -2.2 $mV/°$K. Moreover, low bias current prevents the self-heating and high power consumption as well.

### 2.1.2.2 Positive Temperature Coefficient

Positive TC is obtained from the base-emitter voltage difference of the two transistors. Taking derivative of the equation 2.5 positive TC voltage can be obtained as;

$$\frac{\partial \Delta V_{BE}}{\partial T} = \frac{k}{q}\ln(mn). \tag{2.20}$$

The positive TC is not dependent to collector current as seen from 2.20.

Up to that point the negative and positive TC voltages have been covered. By summing up these two voltages with a proper ratio as seen in Figure 2.4, we get the zero temperature dependency:

$$V_{REF} = V_{BE} + \alpha \Delta V_{BE}. \tag{2.21}$$

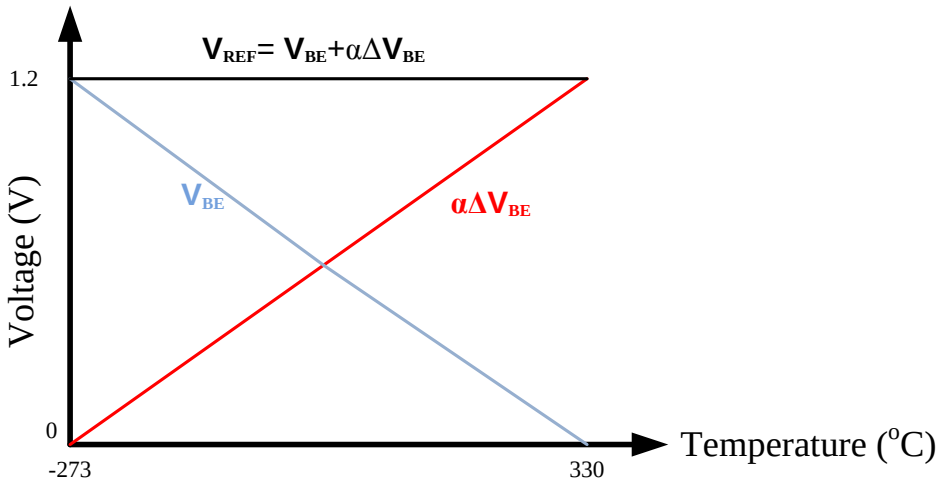


Figure 2.4 Temperature dependency of the positive and negative TC voltages and bandgap voltage.

When equation 2.21 is solved for zero temperature coefficient, $V_{REF}$ will be obtained around 1.2 V. This value is the same as the silicon bandgap voltage thus this voltage is called as bandgap reference.

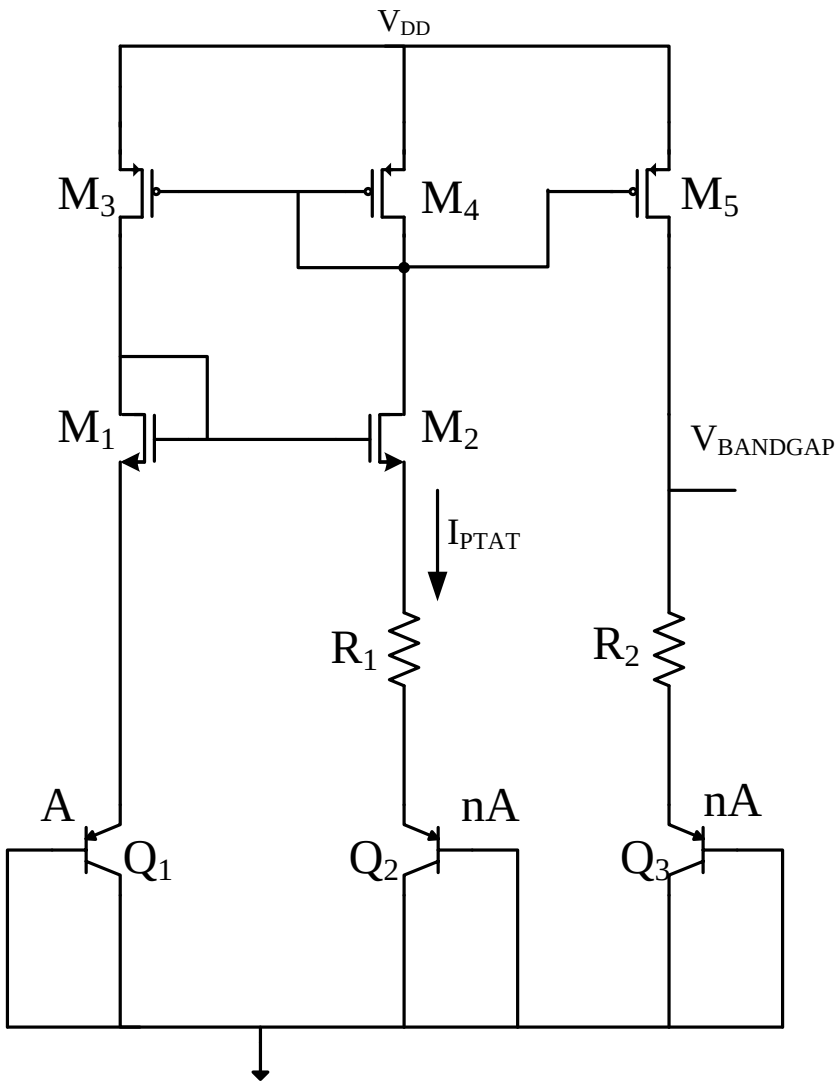


Figure 2.5 Generation of PTAT current and bandgap reference circuit [23].

Figure 2.5 shows the topology of the PTAT current and bandgap reference generation circuit. MOSFETs are replaced with resistor in order to generate current flow. Transistors $M_1, M_2$ and $M_3, M_4$ are identical pairs supplying same current to BJTs. In addition, MOSFETs ensure the voltage equality at the source nodes of $M_1$ and $M_2$ which eliminates the amplifier usage. Hence power consumption and area are improved with respect to amplifier implemented structures.

The generated PTAT current is mirrored with $M_5$ as a result bandgap reference voltage and PTAT voltage are created respectively. PTAT current is equal to

$$I_{PTAT} = \frac{V_T}{R_1}\ln(n), \tag{2.22}$$

and the resulting bandgap voltage can be written as

$$V_{PTAT} = R_2\frac{V_T}{R_1}\ln(n) + V_{EB(Q_3)}. \tag{2.23}$$

## 2.2 Analog to Digital Converter

Digital systems affected the VLSI world extensively since they offer low cost and high speed operation with more accuracy. Data acquisition systems build an interface between the physical world and digital world. Physical parameters are sensed by many kinds of sensors which provide measured data in analog form. This analog signal must be converted to digital signal in order to make interface with digital systems. Analog to digital converters offer great variety of solutions according to the system requests [24].

There are various ADC types for different types of applications. ADC type must be selected according to system specification.

Flash ADC is used for applications which require high sampling rates with large bandwidth. Flash ADC contains numbers of comparator and each comparator enables one step conversion. To illustrate, for N-bit resolution, flash ADC needs $2^N$-1 comparators and $2^N$-1 reference signals. Therefore, for high resolution, power consumption is relatively large [25].

Pipeline ADC can be used at high sampling rates providing high resolution. Pipeline ADC is comprised of many stages, each stage which contains flash ADC, DAC, and gain stage operating at the same time. Pipeline ADC has advantages over speed and resolution however it occupies large area [26].

Sigma-Delta ADC structure comprised of relatively complex circuits with respect to other ADC types. Input signal is sampled at a slower rate of Nyquist rate which is called as oversampling. As a result, Sigma-Delta ADC has slowest operation speed. On the other hand, oversampling provides high accuracy [27].

For this work low power ADC which provides 0.1℃ resolution is the main consideration. Additionally, temperature variation is relatively slow therefore high speed ADC is not a limitation. Therefore, flash and pipeline ADCs are eliminated due to their high power and occupation of large area. On the other hand, Sigma-Delta ADC provides high accuracy but it operates at extremely slow rates. Additionally, Sigma-Delta structure has relatively complex circuits. Moreover, there are many Sigma-Delta ADC integrated temperature sensors in the literature.

Successive Approximation Register (SAR) ADC which is comprised of sample and hold circuit, DAC, comparator and SAR logic consumes relatively low power and provides good resolution at medium sampling rates. Therefore, successive approximation register ADC is the best choice for consideration in this work.

### 2.2.1 **Successive Approximation Register (SAR) ADC**

SAR ADC is generally preferred for the medium resolution and speed applications. The topology of the SAR ADC is rather basic than the other ADCs and yet powerful by its accuracy, low power, and low cost. Furthermore, it is predominantly preferable in on-chip designs due to small size.

Figure 2.6 gives the basic SAR ADC architecture which consists of four blocks, sample and hold circuit, comparator, digital to analog converter (DAC), and SAR logic.

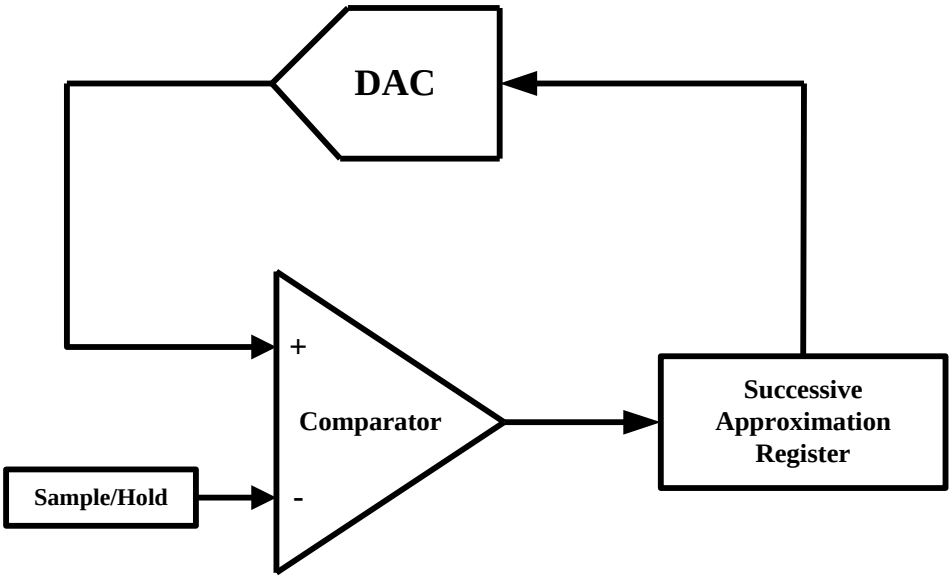


Figure 2.6 Block diagram of the SAR ADC architecture.

The input signal is sampled at each clock cycle or every 12 clock cycles according to input signal variation timing and the sampled signal is hold during one conversion time at the sample-hold block. The comparator compares the input voltage and the voltage generated by the capacitive DAC array. The comparator gives logic 1 if the DAC voltage is higher than the input voltage and logic 0 if the DAC voltage is smaller than the input voltage. The SAR block operates according to the comparator output. At the first clock cycle most significant bit (MSB) is set to one and according to the comparator output its real value is decided. If the comparator output is high meaning that input voltage is smaller than the predicted DAC voltage, then MSB is set zero and if the comparator output is low is stays at voltage high. Then the next register pulls high and the same operation takes place. After 12 clock cycles, all register values are determined and the digital equivalent of the input signal is obtained.

SAR ADC completes the whole conversion step at 12 clock cycles and does not sample the input voltage before it finishes the conversion cycle. Hence sample and hold circuit samples the input signal at multiple of 12 clock cycles. In other words, ADC clock must be 12 times faster than the system clock. In this design, the timing signals generated in the SAR logic is used for sample the signal instead of using two different clocks which makes the design simpler.

#### 2.2.1.1 Comparator

Comparator block consists of three gain stages and a Schmitt trigger. Figure 2.7 presents the topology of the comparator. The preamplifiers amplify the difference of input voltages and Schmitt trigger sets the output voltage high or low regarding the input voltage difference.

In order to prevent the mismatches and high noise, instead of designing one gain stage having the gain of 60 dB, three gain stages with a gain of 20 dB are used with offset cancellation capacitors. The gain of the Schmitt trigger is high enough to pull the signal to digital high.

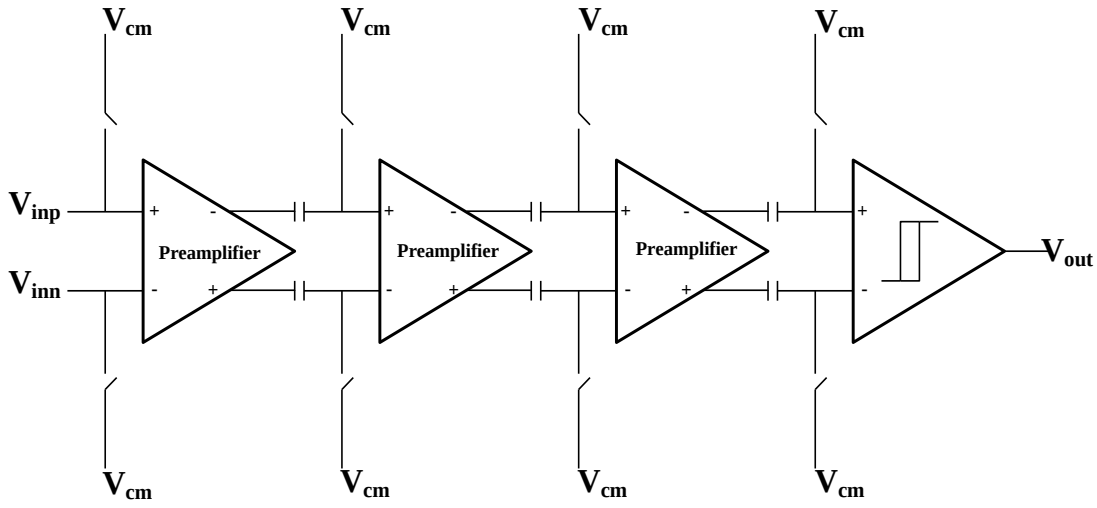


Figure 2.7 Block diagram of the proposed comparator architecture.

Comparator suffers from the offset voltage arising from the process mismatches of the transistors. The offset voltage can be suppressed by dynamic offset cancellation technique. As seen in Figure 2.7 capacitances are connected in series to output of each gain stage to cancel the offset voltage. The offset voltage is stored in the ac-coupling capacitors. At the beginning of each conversion cycle the switches are turned on setting the inputs of the preamplifiers and Schmitt trigger to common mode voltage to cancel the offset voltage. At the other half of the conversion cycle switches are turned off and input voltage is amplified to last stage and comparator output is set. This is a one comparison cycle operation.

#### 2.2.1.2 DAC Array

Digital to analog converters transforms digital data to analog signal. There are several DAC architectures mainly comprised of resistors, capacitors or both of them which are called hybrid arrays.

In SAR ADCs, DAC generates a prediction voltage according to current SAR logic for comparison with the input voltage. In each cycle registers are updated according to comparator output and in the next cycle DAC creates closer voltage to input voltage.

Charge scaling DACs are conventionally the most preferred architectures in SAR ADCs. The reason behind this is their overwhelming advantages over the other DAC types. First of all, capacitive array in the charge scaling DACs does not dissipate DC power hence power consumption is significantly decreased. Secondly, a sample and hold circuit is not necessary as voltage can be sampled and hold in the capacitor array. Thirdly, integral nonlinearity (INL) which is the maximum difference between the output and the line aligned with the two end points of the output curve, is improved.

Figure 2.8 shows the basic structure of N-bit binary-weighted capacitive (BWC) DAC. The traditional switching method of the BWC DAC consists of three stages; in the sample stage bottom plate of the capacitors are connected to $V_{in}$ and top plates are connected to ground. Input voltage is stored in the bottom plates of the capacitors. In the hold stage top switches are opened and bottom capacitors are connected to ground. The charge stored in the top plates goes to negative form of $V_{in}$. In the redistribution stage, the prediction of the DAC bits is done. The bottom plate of MSB is connected to $V_{REF}$ and conversion is started. This cycle is repeated for each bit sequentially [28].

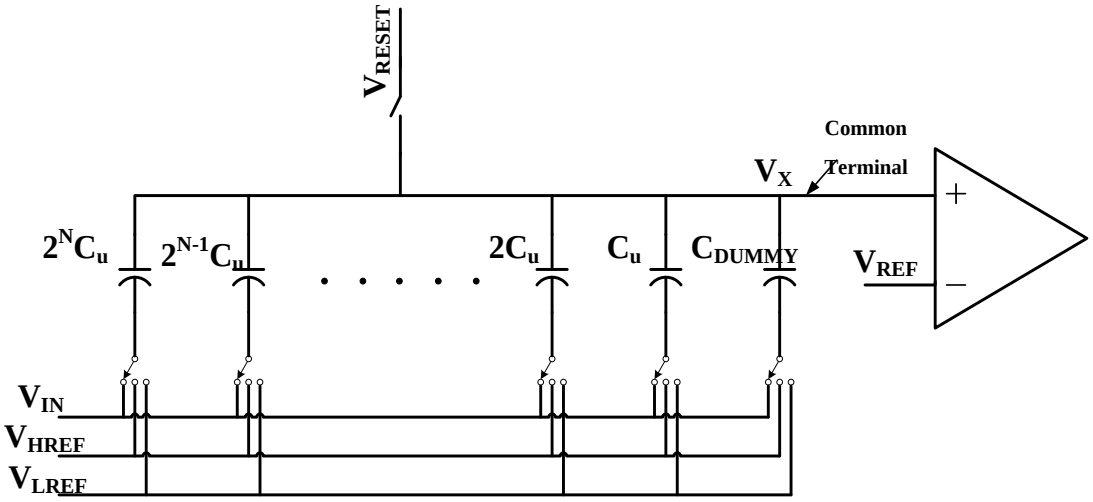


Figure 2.8 N-bit binary-weighted capacitive DAC structure.

The energy efficiency of the conventional switching method is a new switching technique which reduces the conventional switching energy by 37% which is analyzed by Ginsburg and Chandrakasan [29]. At each conversion cycle an up or down transition occurs regarding to the prediction at the moment. Up transition occurs when input voltage is greater than the current predicted voltage and next MSB is connected to $V_{HREF}$ which increases $V_x$ which is the voltage of the common terminal. On the other hand, when input voltage is smaller than the prediction, current bit is connected to $V_{LREF}$ and next bit is connected to $V_{HREF}$ which decreases $V_x$, this is called down transition. The energy dissipations during the up and down transitions are analyzed for four switching methods. The switching methods are conventional switching method in which switching occurs simultaneously, conventional switching method in which two switching steps are used instead of one, charge sharing method and splitting capacitor method. Energy saving is equal during the up transition for all switching methods. However, capacitor splitting method saves energy 37% during the down transition with respect to others [29].

The main power and area consumption in SAR ADC arise from the comparator and DAC block. Furthermore, low power is one of the principal concerns of this thesis, thus split capacitor architecture is the most appropriate selection for DAC block.

In addition to the power efficiency, capacitor splitting method has a great area advantage over BWC DAC. As the resolution increases the MSB capacitor increases

in the BWC DAC and by splitting the MSB capacitor into sub-array this problem is handled. Figure 2.9 presents the preferred capacitor structure.

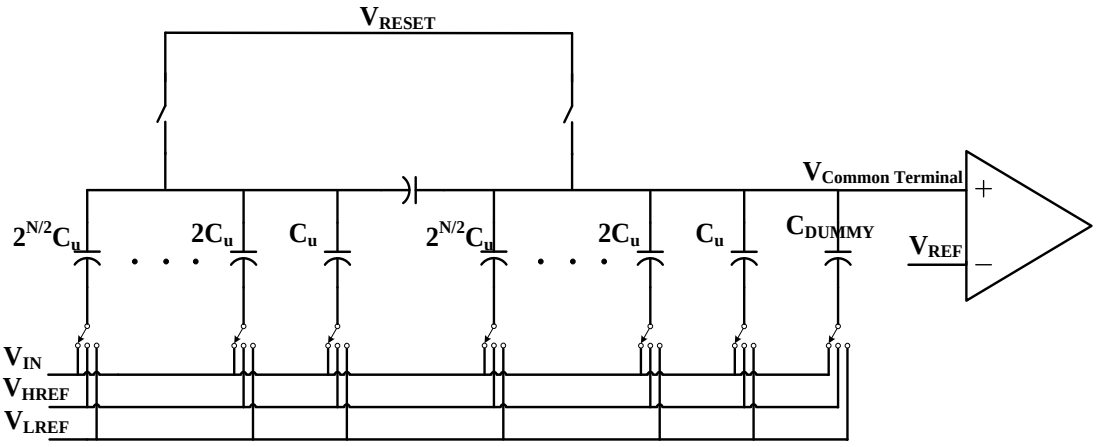


Figure 2.9 N-bit split capacitor DAC structure.

There are static and dynamic parameters that affect ADC performance. Static parameters are dominant at low frequencies whereas dynamic parameters are dominant at high frequencies. The linearity condition for the DAC is equal to,

$$3\sigma(D_{IN} = 1024) < 0.5LSB, \tag{2.24}$$

where $\sigma$ is the standard deviation of the mismatch of capacitor. The condition analyzed where the maximum linearity error occurs and it occurs at the first cycle of the conversion where MSB is 1 and all other bits are 0. Assuming the input voltage range of the ADC as 2 V and LSB is calculated as;

$$LSB = \frac{2}{2^{12}} = 488\mu V. \tag{2.25}$$

In a 0.35 µm CMOS process, standard deviation of DAC is calculated as 22.47, three times calculated value is smaller than half of the LSB voltage which ensures the linearity condition [30].

The capacitive DAC array functions sample and hold circuit inherently. There is no need for the additional sample and hold circuit. In the sampling stage all bottom plate switches are connected to $V_{IN}$ and top plate switch is connected to $V_{CM}$, then the input voltage is sampled to the array. The sampled input voltage is hold in the DAC until the

conversion is completed. After the sampling stage top plate switch disconnected and bottom plate of the MSB capacitor switch is connected to $V_{HREF}$ and rest of the switches are connected to $V_{LREF}$. The comparison is done and the MSB bit is determined according to the voltage difference between input and reference voltage. This is the process of one conversion cycle. After determination of the MSB bit, the next MSB capacitor switch is connected to $V_{LREF}$ while keeping the rest of the capacitors except the determined bits at $V_{LREF}$. This operation repeats 12 cycles until the LSB determination. Switching sequence progress according to the binary search algorithm.

The integral non-linearity (INL) and dynamic non-linearity (DNL) are the dominant parameters for medium resolutions. INL and DNL is affected by capacitor matching and parasitic capacitances. The INL and DNL of the BWC DAC is smaller than the split capacitor DAC however considering the huge area advantage of the split capacitor array, nonlinearity performance can be neglected [31].

#### 2.2.1.3 Successive Approximation Register

Binary search algorithm is performed by the successive approximation register. SAR logic is comprised of two arrays of 12 registers as given in Figure 2.10.

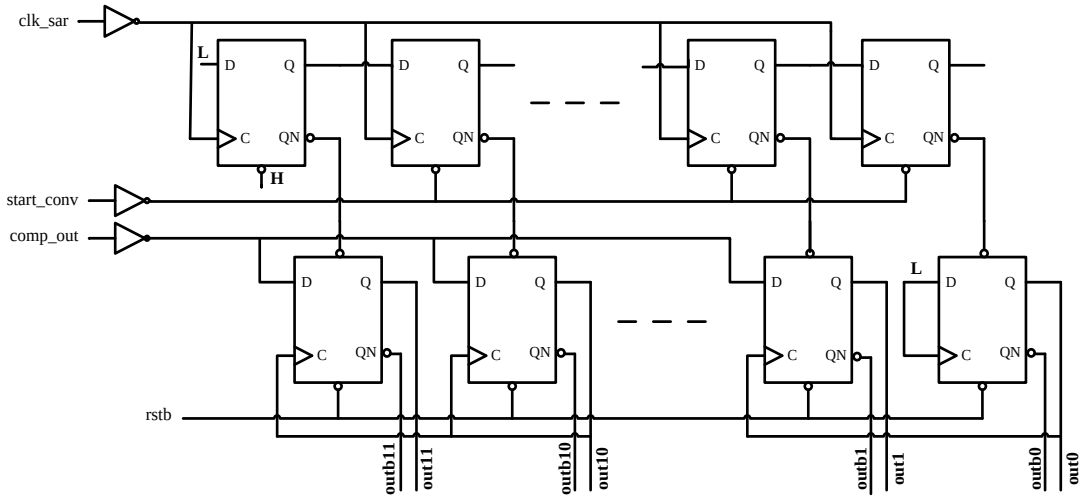


Figure 2.10 SAR register block diagram.

In the first conversion cycle MSB is set to one and other bits are set to zero. The comparator decides whether the input voltage is smaller or larger than the reference voltage. If the input voltage is smaller than the reference voltage, MSB is set to zero and next MSB is set to one. Otherwise MSB stays at one and the next MSB is set to one. This algorithm is performed for each DAC bit and after 12 clock cycles, all the DAC bits are decided.

## 2.3 Bias Generator

In this thesis all of the necessary bias currents and voltages are generated in the bias generator block. In other words, apart from the power supply, external voltage or current supplies are not necessary.

The bias generator block is required to generate supply and temperature independent bias signals due to the fact that the temperature and power supply variations affect performance negatively. The bandgap voltage is generally the most preferred source for bias circuits to generate reference currents. In this method bandgap voltage is connected to the gate of a transistor and the drain current is generated as a reference current. The topology of the reference current generation from bandgap voltage is shown in Figure 2.11. This reference current is mirrored to create a reference current bias for voltage and current generation.

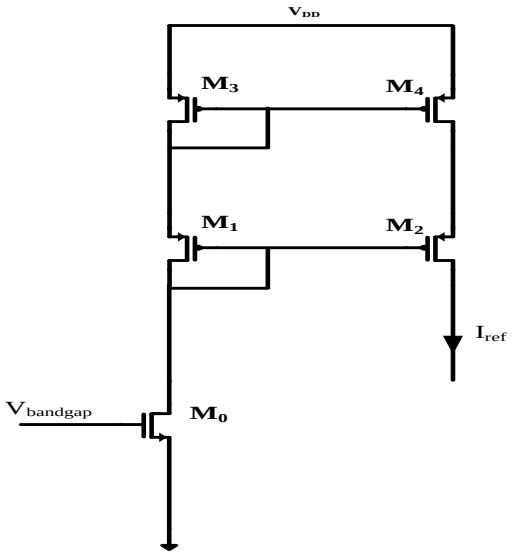


Figure 2.11 Bandgap reference current generation architecture.

## 2.4 Digital Controller

Digital controller block consists of a Serial Programming Interface (SPI), configuration memory, timing controller, and calibration logic. Block diagram of the digital controller is given in Figure 2.12. Digital controller has three functions first one is to communicate the external electronics through the Serial Programming Interface (SPI), the second one is to generate timing signals, and third one is on-chip calibration.

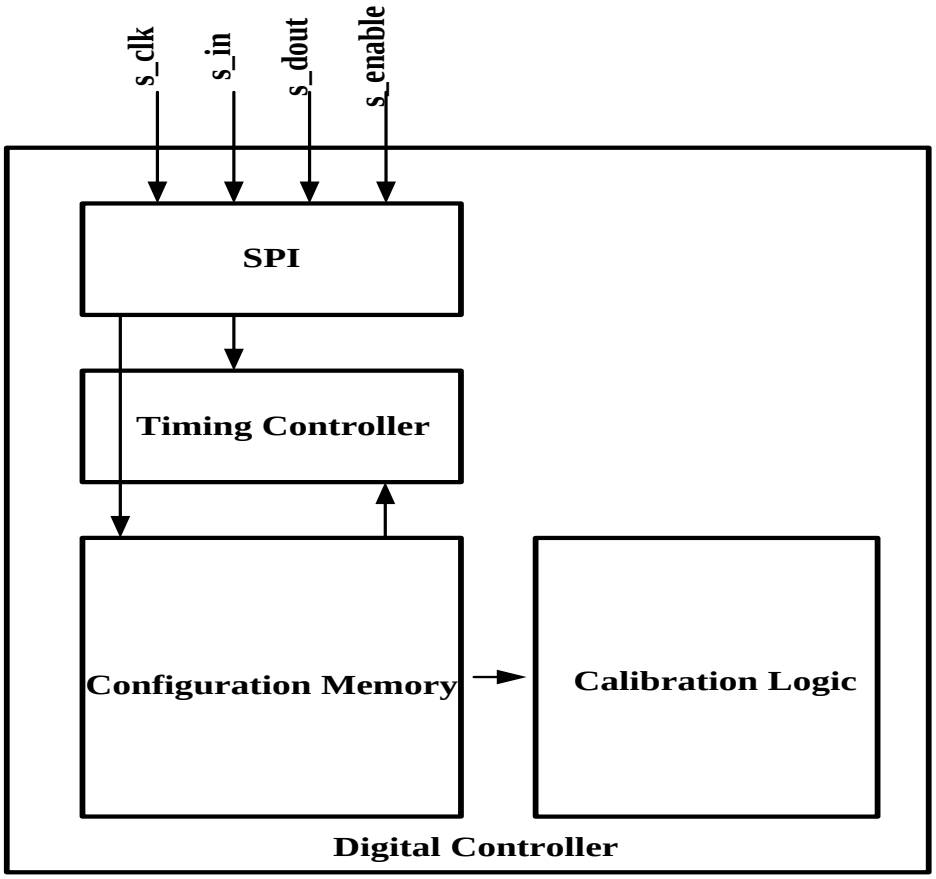


Figure 2.12 Block diagram of the digital controller.

## 2.5 Output Stage

A serializer block which serializes the 12-bit data at the system clock frequency is used for the output stage. Serializer consists of two arrays of 12-bit shift registers. After the conversion is completed 12-bit SAR data is loaded to the serializer block by the conversion done signal and the data is shifted to output for 12 clock cycle. Serializer shifts the LSB first and MSB last. Data valid signal is generated to indicate the serialization process which is set to one during the serialization process (12 clock cycles).

# CHAPTER 3

# IMPLEMENTATION OF THE TEMPERATURE SENSOR

This chapter analyzes the implementation of the low power temperature sensor with digital outputs. Implementation of the main blocks and critical sub-blocks of the design is discussed and integration of these blocks is explained in detail. Then top level floorplan and layout of the chip are stated. Furthermore, layout techniques are discussed to prevent devices mismatches, parasitic capacitances, and charge coupling. Design and implementation of the proposed temperature sensor is realized with a 0.35 μm CMOS technology.

## 3.1 PTAT Voltage and Bandgap Reference Generation

### 3.1.1 PTAT Current Generation

Figure 3.1 presents the structure of proposed PTAT current generation circuit. PTAT current created in this circuit can be written as

$$I_{PTAT} = \frac{1}{R_1}\frac{kT}{q}\ln(n), \tag{3.1}$$

where $k, q$ are constants and n is emitter area ratio. Resistor $R_1$ is determined according to the power consumption limitation of the design. The transistor pairs $M_0$ and $M_1$, $M_2$ and $M_3$, $M_4$, $M_5$, $M_8$, and $M_9$, $M_6$, $M_7$, $M_{10}$ and $M_{11}$ are identical pairs biased with same gate voltage. Thus, equal currents flow over all branches.

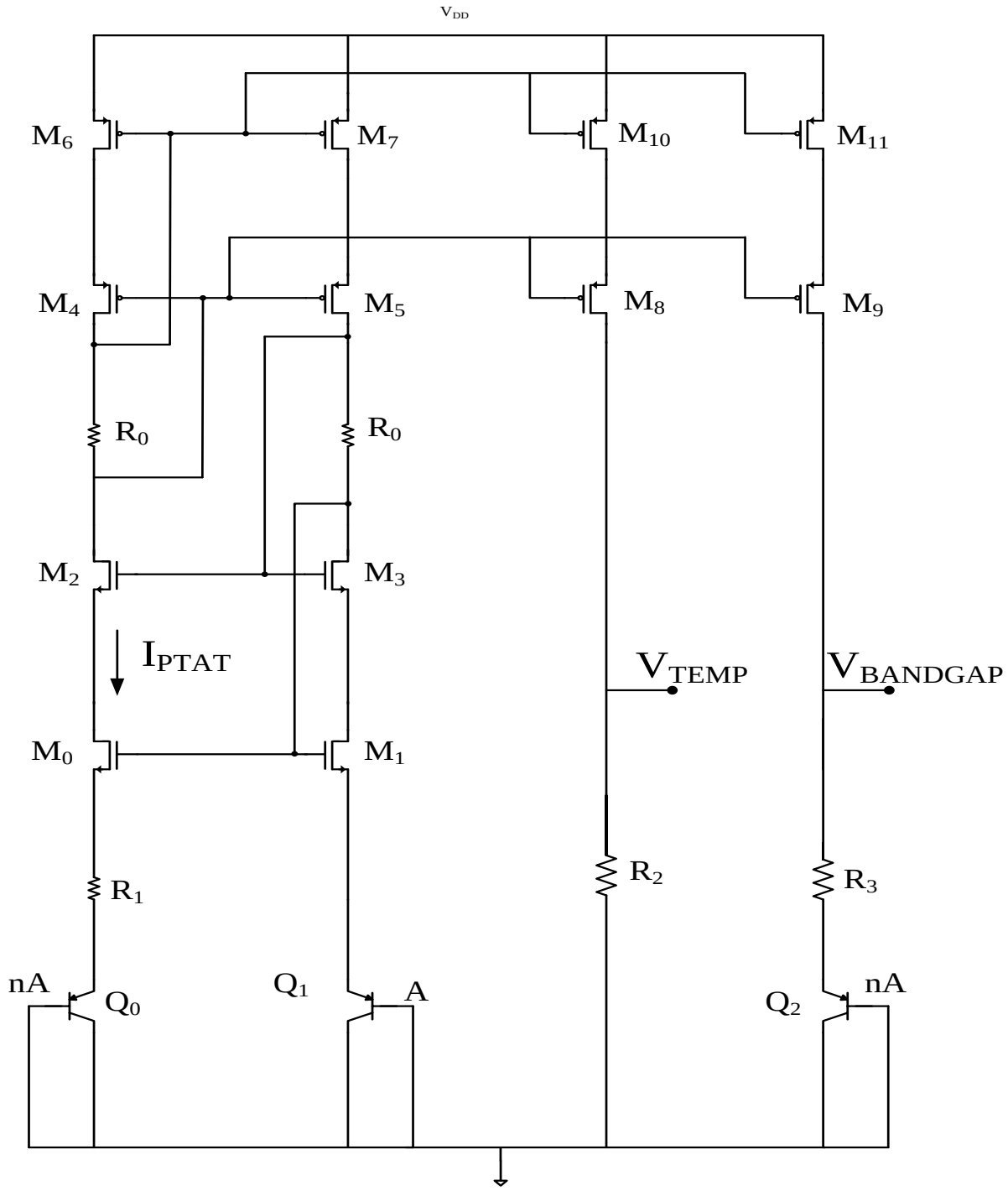


Figure 3.1 Integrated bandgap reference generation and PTAT current generation [23].

As seen in equation 3.1 PTAT current is linearly proportional to temperature in ideal case. However, resistors implemented in CMOS process have inherently nonlinear characteristics. Resistor values are dependent to complex functions of CMOS process

technology. As a consequence, resistor implementation suffers from low linearity and accuracy.

Off-chip discrete resistors are highly accurate with respect to their on-chip counterparts. However, external discrete element usage provides many disadvantages. Firstly, the cost increases. Secondly, number of pads needs to be increased for signal routing external and back which results in area increment. Lastly, along the signal routing via pads capacitive and inductive parasitics are introduced which reduces the accuracy. On-chip resistors have low accuracy but provides low cost, high integrity therefore they are preferred considering the disadvantages of the discrete element usage externally.

Implementation of resistors can be realized with diffusion or polysilicon layers in CMOS process. In Table 3.1 performance characteristics of resistors implemented in CMOS technology is given. Diffusion resistors provides higher sheet resistivity therefore they are implemented smaller areas than polysilicon resistor. On the other hand, polysilicon resistor has lower noise since they are isolated from substrate. In addition, they have low capacitor parasitics providing higher speed. Furthermore, polysilicon resistors do not have voltage dependency unlike diffusion layer resistors. Most importantly, polysilicon resistors have low temperature coefficient (TC) and higher accuracy. TC is the most critical specification for this thesis since operation is performed along very wide temperature range. Hence, polysilicon resistor which has lowest thermal coefficient is chosen for implementation.

Table 3.1 Passive resistor components performance summary in a 0.35 μm CMOS process.

| **Layer** | **Sheet Resistivity (Ω/□)** | **Temperature Coefficient** ($10^{-3}$/K) |
|---|---|---|
| n-well | 1160 | 3.9 |
| n-diffused | 85 | 1.6 |
| p-diffused | 143 | 1.6 |
| Poly-silicon | 40 | 0.8 |
| Metal-1 | 90 | 3.4 |
| Metal-top | 43 | 3.4 |

There are various polysilicon resistors in CMOS technology. In this work, resistor providing lowest TC which is -0.2 $10^{-3}$/K. Moreover, sheet resistance of this resistor is 200 Ω/□ which maintain high values in small area.

In order to increase the accuracy of resistors, process errors must be minimized. The well known equation of the resistance is

$$R = \rho \frac{L}{Wt}, \tag{3.2}$$

where $\rho$ is resistivity, L is the length, W is the width, and t is the depth. Each of the parameters in the equation present errors due to process or operation of the chip.

After modification of $\rho$ into $\rho_s$ which is resistivity per depth named as the sheet resistivity and including the errors of process equation of resistance can be rewritten as

$$R = \left(1 + \frac{\Delta\rho_s}{\rho_s}\right) \frac{\left(1 + \frac{\Delta L}{L}\right)}{\left(1 + \frac{\Delta W}{W}\right)} \rho_s \frac{L}{W}. \tag{3.3}$$

To ensure good accuracy $\Delta\rho_s, \Delta L,$ and $\Delta W$ should be minimized or $\rho, W$, and L should be maximized. Resistivity is defined by process so it cannot be changed. Resistivity introduces errors owing to process and operation which consist of random variation and systematic gradients in process. To minimize random variation area must be increased yet increasing area results in higher systematic gradient error. There is a conflict so resistance value is determined carefully. L and W present random and systematic errors too. As oppose to $\rho_s$ increasing L and W minimizes the errors slightly. Moreover, dummy resistors can be added in layout to reduce systematic gradient. Layout technique is important due to the fact that good layout reduces the resistor matching error below 0.1% [32]. In conclusion, polysilicon resistors have good accuracy, low dependence to temperature, and voltage variations but consume large area for good accuracy.

After deciding the PTAT generation circuit and resistor type, by flowing the PTAT current over the polysilicon resistor, PTAT voltage is generated. This voltage varies from 1.2 V to 2.2 V. Desired resolution of the sensor is 0.1℃ from -55℃ to 125℃ so 1800 points need to be analyzed by the ADC. The smallest voltage which must be distinguished by the ADC is calculated as 555 μV. Therefore, LSB voltage of the ADC needs to be equal or smaller than 555 μV.

### 3.1.2 **Bandgap Reference Voltage Generation**

Bandgap reference generation is obtained proper summation of positive TC and negative TC voltages. Positive TC voltage is difference base-emitter voltage and negative TC is base-emitter voltage. Figure 3.1 states also the architecture of bandgap reference generation.

Bandgap reference voltage is stated to be constant with respect to temperature however, in practical it deviates very small value across the 1.2 V. This deviation results from process spread, series resistances, and curvature which is caused by the non-ideal characteristics of $V_{BE}$ and $\Delta V_{BE}$. Summation of all this errors caused inaccuracy of the system. Additionally, SAR ADC also introduces errors to the system. These errors are tried to be compensated in the calibration block.

Bandgap reference generation is implemented according to achieve the smallest deviation along the full temperature range. This is implemented by selection of proper ratios for $R_1$ and $R_3$.

This architecture suffers from multiple operation points of operation. In the analysis of given structure zero current flow is also an operating point. Therefore, a start-up circuit is necessary for desired operation. Start-up circuit is activated at the beginning of the operation. When the desired current flow is reached, the start-up circuit is disabled.

Additionally, stability simulation is performed to verify the bandgap reference voltage generation.

## 3.2 Bias Generator

All bias voltages and currents of the ADC are generated by the bias generator. Generated bias signals should be temperature and supply independent. Bandgap reference circuit is used for temperature and supply independent reference current generation for each bias signal. This reference current is mirrored to voltage and current DACs which are chosen architectures to produce bias signals. These DACs consists of current mirroring circuitry which is comprised of multiplying PMOS transistors. Bias generator consists 6 voltage DACs and 4 current DACs, both of the voltage and current DAC is configurable by 5-bit selection. There are 2 types of voltage DACs which provide the voltage variation from 0.1 V to 3.2 V with 0.1 mV steps. Current DACs supply 1 μA to 31 μA with 1 μA steps for preamplifiers in comparator and 5 μA to 155 μA with 5 μA steps for Schmitt trigger.

## 3.3 SAR ADC Implementation

The integration of the system is done considering some specifications. The desired resolution of the system is 0.1 °C and temperature range of operation is -55 °C to 125 °C. Thus, ADC must sustain at least 1800 output data. This can be achieved by 12-bit DAC selection.

The temperature signal which is PTAT voltage is directly connected to the input of the ADC. The temperature data is carried as voltage generated from PTAT current flowing over resistor. Considering the low power operation current values are hold in a specific range. Therefore, temperature voltage range is limited so the ADC input voltage range is limited and full scale operation is not necessary.

In order to ensure high performance operation, total noise of the ADC must be smaller than half of the LSB voltage. ADC noise is dominated by comparator and DAC blocks. In the DAC kTC noise of capacitors are dominated and it affects the value of capacitors. The kTC noise of the capacitors is equal to:

$$V_{noise,RMS} = \sqrt{\frac{kT}{C}}, \tag{3.4}$$

where $k$ is the Boltzmann constant.

The Signal Noise Ratio(SNR) due to the thermal noise can be written as

$$SNR_{thermal} = \frac{P_{thermal}}{P_{signal}} = 10log\left(\frac{\frac{1}{2}\left(\frac{FS}{2}\right)^2}{\frac{2kT}{C_u}}\right), \tag{3.5}$$

where $FS$ is input voltage range. Whereas theoretical Signal-Noise Quantization Ratio (SNQR) can be written as

$$SNQR_{theorotical} = 6.02n + 1.76, \tag{3.6}$$

where $n$ is the number of bits and for 12-bit ADC SNQR equals to 76 dB. To have high performance ADC thermal SNR must be greater than the theoretical SQNR. Thus unit capacitance value is limited by SQNR. On the other hand, parasitic capacitance of the switch must be taken into consideration while deciding the capacitor value. The DAC capacitances must be larger than the parasitic capacitance of the switches in order to avoid inaccurate voltage division. Hence unit capacitance must be as large as possible to ensure low kTC noise and correct voltage division. The value of chosen unit capacitor is 1.14 pF. This can be implemented by MIM capacitors in a 0.35 μm

CMOS process. MIM capacitors are selected due to their smallest thermal coefficients. Moreover, DAC noise for chosen capacitance is much smaller than half of the LSB.

### 3.3.1 Switch Architecture

The switches are used to sample the necessary voltages during the ADC operation. They transmit input voltage, reference voltages for binary search algorithm, and common mode voltages for reset the DAC. The switches are used at the bottom of each capacitance and at the junction points at the top.

The switches present parasitic capacitances which change the value of the capacitor which they are connected and causes the ADC error as sampled voltage value is changed. As a result, small parasitic capacitance is desired for accuracy of the system. The preferred shared-like switch structure is given in Figure 3.2. This structure shows the minimum parasitic capacitance.

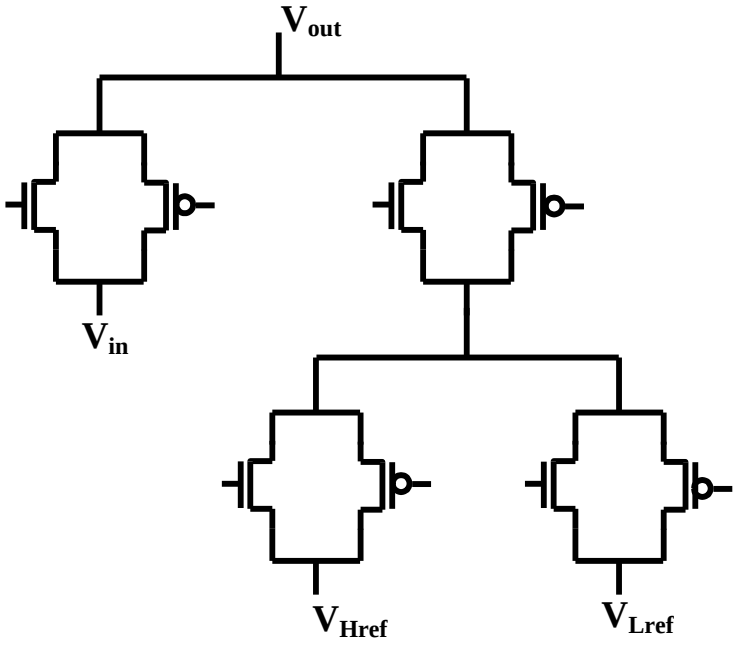


Figure 3.2 Proposed shared-like switch architecture.

The switch structure is decided with respect to smallest parasitic capacitance. The other important parameter is settling time of the DAC which is related to the switch

sizes. The transmission gates have on-resistance when they are on. The value of the resistor can be written as

$$R_{on} = \frac{1}{\mu C_{ox}\left(\frac{W}{L}\right)V_{OV} - V_{DS}}, \tag{3.7}$$

where $V_{OV}$ is the over drive voltage and $V_{DS}$ is the drain to source voltage. The on-resistance equation is changed with respect to on-transistor PMOS or NMOS. The switches represent on-resistance when they are on. As a result, when NMOS transistor is on parameters of the NMOS transistor is taken for the equation and when the PMOS transistor is on parameters of the PMOS transistor is taken for $C_{ox}$, W, L, $V_{OV}$, and $V_{DS}$.

Maximum voltage difference occurs at the beginning of the conversion when D=1024. In that case the MSB capacitor is connected to the reference voltage and rest of the capacitors are connected to the common mode voltage. The resistance of each line in the DAC array is equal to the sum of constant switch on-resistance and voltage switch resistance which they are connected to.

The smallest voltage difference at the output occurs for the LSB. Smallest time needed for this case is equal to

$$t = RCln2^N, \tag{3.8}$$

for 12-bit resolution [33].

In this work sampling rate is 714 S/s. In this time period charging and discharging occurs. Substituting the t in the equation the limitation for the value of R is taken for the reference limit for the switch size.

### 3.3.2 **Comparator**

Comparator compares the two analog signals and create a digital output according to the input voltage difference. Comparator is the most crucial block for the ADC performance since it must distinguish the LSB voltage. LSB voltage must be smaller than 555 $\mu V$ hence it must be guaranteed that comparator differentiate that much of a signal. Comparator comprised of three preamplifiers with a gain of 20 dB and a high

gain Schmitt trigger as a last stage. Instead of using one amplifier with a gain of 60 dB considering noise and offset voltage errors three gain stages are used. Moreover, cascading the gain stages extends the frequency of operation. Gain stages amplifies the input difference voltage and sends to Schmitt trigger to pull the voltage to low or high logic. The minimum voltage difference that Schmitt trigger sense is 1000 multiple of LSB voltage that is 555 mV.

Comparator is a power hungry block therefore attention is showed for power dissipation as design process. Yet it is the highest power dissipated part in the system.

In the conventional SAR ADCs mostly static and dynamic latched comparators are used. In this work, static latch comparator is preferred as a result of that dynamic latched comparators presents high input offset voltage. Figure 3.3 shows the preamplifier topology and Figure 3.4 shows the Schmitt trigger topology.

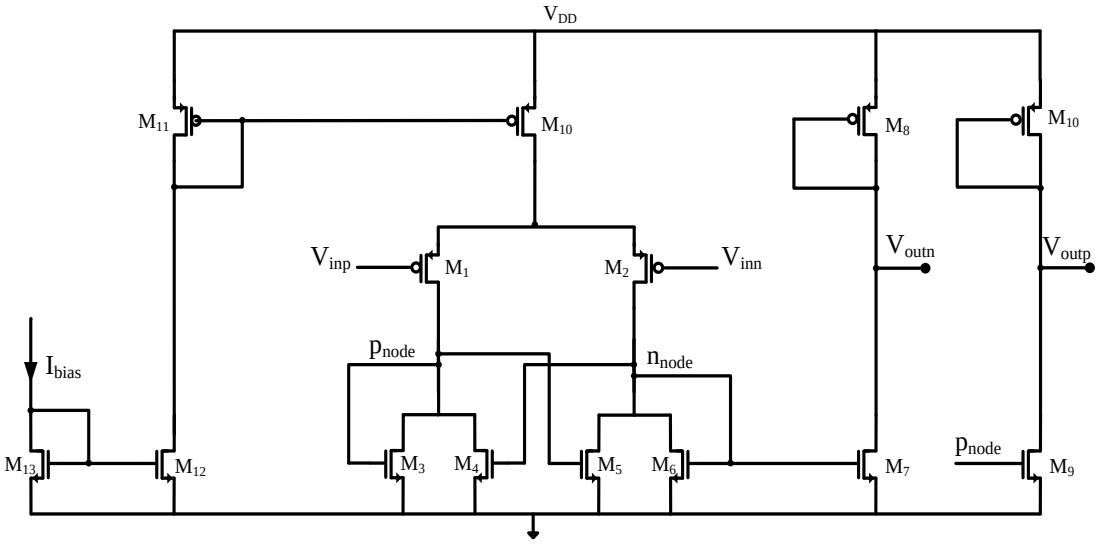


Figure 3.3 Proposed preamplifier topology.

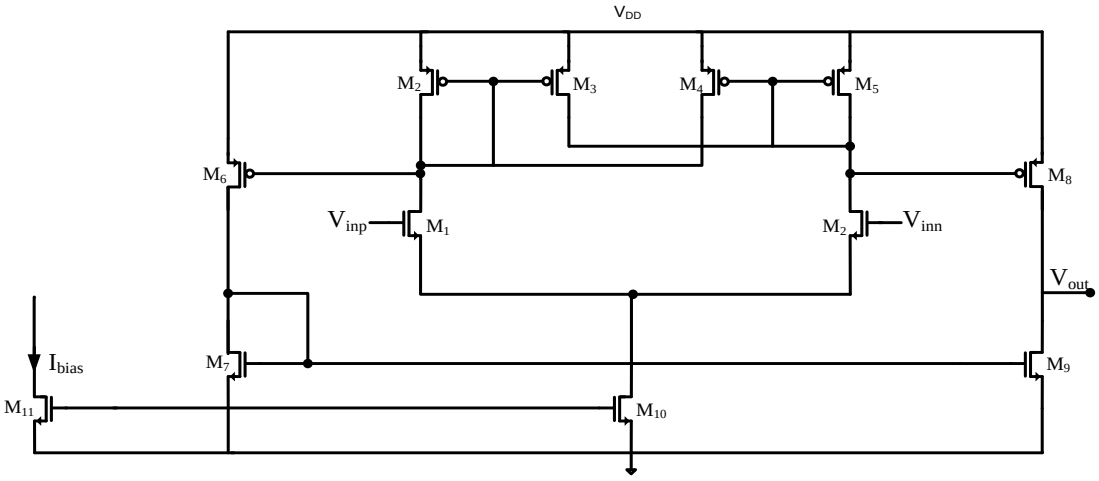


Figure 3.4 Proposed Schmitt trigger topology.

## 3.4 Digital Controller

### 3.4.1 Timing Signal Generation of the System

All timing signals of the system are generated by a digital controller.

Temperature signal is sampled at the beginning of each conversion cycle so sampling rate is 12 times clock cycles. This is sufficient for two considerations. First one is that temperature of the sensor does not change rapidly. Second consideration is that sample and hold operation which is performed by DAC array is carried out successfully during the conversion. In other words, temperature data can be kept in the array during one conversion cycle.

At the beginning of each conversion cycle ADC start signal is generated. This signal is generated every 12 clock cycles. The ADC operates at 12 kHz. At the rising edge of the clock, binary search algorithm is performed and a comparison voltage is generated at the DAC array. At the falling edge of the clock comparison of the DAC voltage and reference voltage is done at the comparator and SAR bits are updated with respect to the comparator output. For the offset cancellation of the comparator three timing signals having small delays with respect to each other are generated and applied at consecutive order to preamplifiers. Comparator timing signals are generated in a consecutive order in order to ensure offset cancellation operation.

Sampling rate of the sensor can vary between 714 S/s to 1 MS/s. Hence serial 1-bit data can be transmitted to output at a rate of 70 ns to 100 μs. The transmission of the 12-bit temperature data can be completed in 1 μs at the highest clock frequency that the sensor can operate. However, the temperature of the signal does not change that rapidly. Therefore, the sampling rate of the sensor is chosen as 714 S/s and transmission of 12-bit temperature output data is completed in 1.4 ms.

### 3.4.2 **SPI**

SPI is a four-wire system which provides communication with the external electronics. The four-wire system consists of a serial input data, serial system clock, active low enable signal and serial output data. Serial input bus comprised of 20-bit registers, 4-bits are address and 16-bits are input data as seen from Figure 3.5.

| 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| address<3:0> | | | | data<15:0> | | | | | | | | | | | | | | | |

Figure 3.5 Serial programming interface register table.

SPI starts transmission from LSB to MSB. Furthermore, SPI samples the input data at the rising edge of the clock so input data has to be written or read at the falling edge of the clock by external electronics. Figure 3.6 shows the timing diagram of SPI.

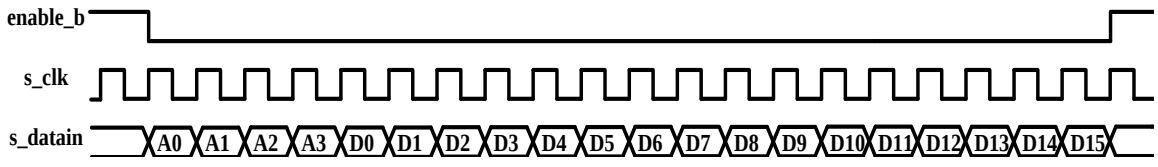


Figure 3.6 Timing diagram of the serial programming interface.

### 3.4.3 **Configuration Memory**

The configuration memory comprised of 16-bit words. Serial input data is written to according memory address at the rising edge of the clock right after all serial input data transmission is completed. Memory consists of 10 rows of 16-bit register array. Figure 3.7 shows simple register structure which is used in memory. Configuration memory stores all timing data for ADC, start signals for the bandgap generation block, bias generator current and voltage values, and calibration data for twenty regions. Moreover, desired operation parameters are implemented into configuration memory inherently so with applied reset the sensor starts desired operation.

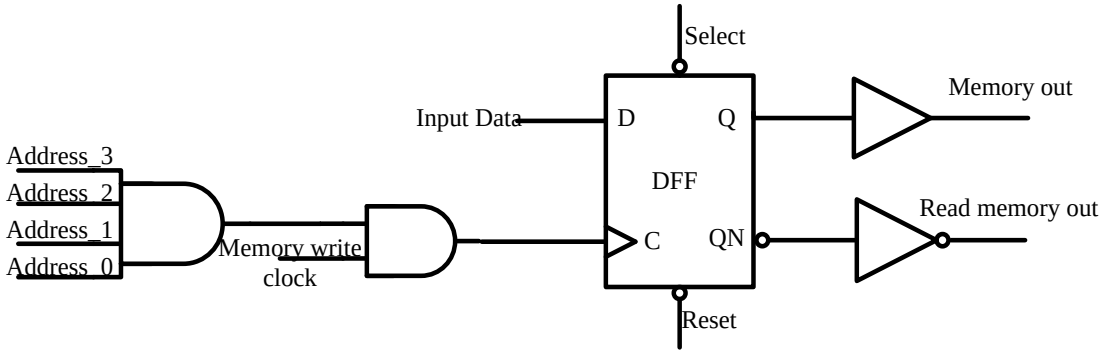


Figure 3.7 Proposed structure of the 1-word memory.

## 3.5 Top Level Layout

Figure 3.8 presents the floorplan of the system. The placement of the blocks is thought carefully for low noise and high performance operation. The temperature sensor and reference generation block is placed near the ADC block considering the routing of the temperature and bandgap reference signals. Moreover, for low noise and low voltage drop along the signal buses they must be routed in minimum distance. As a result, bias generator block which generates high and low reference voltages for DAC and bias currents for the comparator block is placed just below the ADC part. Digital controller has an interface with pads via SPI therefore it is placed the left part of the sensor. The configuration memory stores the calibration data for twenty different regions over the full temperature range, timing data, and bias voltages and currents data. It is placed below the timing generation and SPI logic. Furthermore, calibration

logic is placed between the configuration memory and bias generator. The serializer is placed at the middle of the chip since it takes calibrated data from bottom side and transmits serial data to the right of the sensor to the output pads. The input pads are located at the left side whereas output pads are placed at the right side of the sensor. The supply pads are located at the top and bottom nearest to power hungry blocks considering the digital and analog power distinction. They are placed top of the ADC and bottom of the bias generator. Table 4.1 states the pad list of the temperature sensor.

Table 3.2 Pad list of the temperature sensor.

| Pad No | Pad Name | Pad No | Pad Name |
|---|---|---|---|
| 1 | ESD Ground | 16 | Dummy pad |
| 2 | sys_clk | 17 | Analog Supply |
| 3 | rstb | 18 | Analog Supply |
| 4 | sdin | 19 | dval |
| 5 | slatch | 20 | data_out |
| 6 | sdout | 21 | Pad Supply |
| 7 | ESD Supply | 22 | Pad Ground |
| 8 | Digital Supply | 23 | Analog Ground |
| 9 | Digital Ground | 24 | Analog Ground |
| 10 | Digital Ground | 25 | Analog Supply |
| 11 | Analog Supply | 26 | vtemp_test |
| 12 | Analog Ground | 27 | Analog Supply |
| 13 | Analog Ground | 28 | Digital Ground |
| 14 | Analog Supply | 29 | Digital Ground |
| 15 | Analog Supply | 30 | Digital Supply |

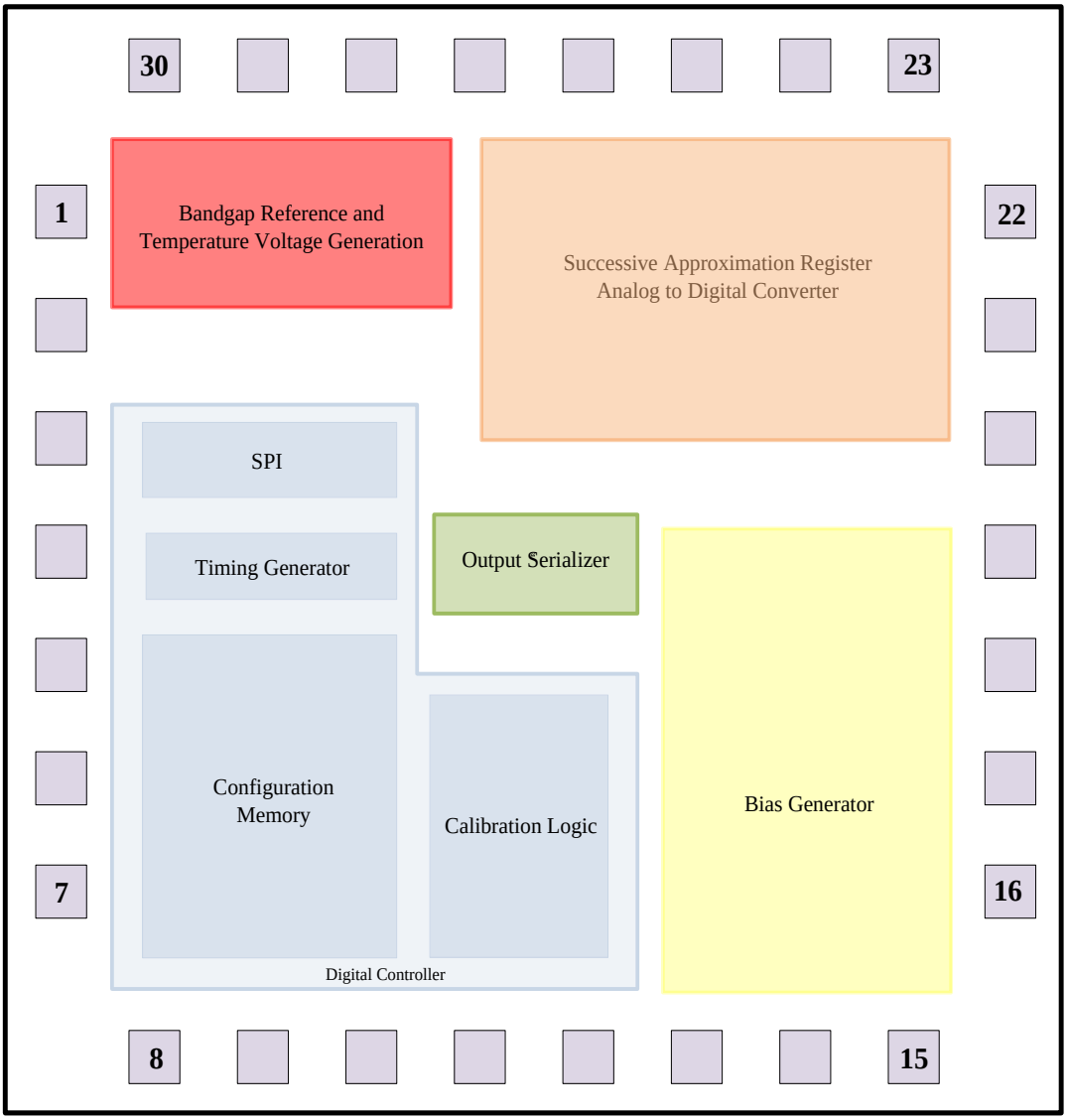


Figure 3.8 Top level floorplan of the temperature sensor chip.

Figure 3.9 shows the top layout of the temperature sensor chip. The size of the temperature sensor chip is 2 mm × 2 mm. In this chip every schematic and layout block except input output(IO) pads is drawn using custom design. The IO pads are taken from standard cell library in 0.35 μm CMOS technology for Cadence. Therefore, the pad frame in the chip layout is covered in gray in order to protect intellectual property of Cadence in CMOS fabrication.

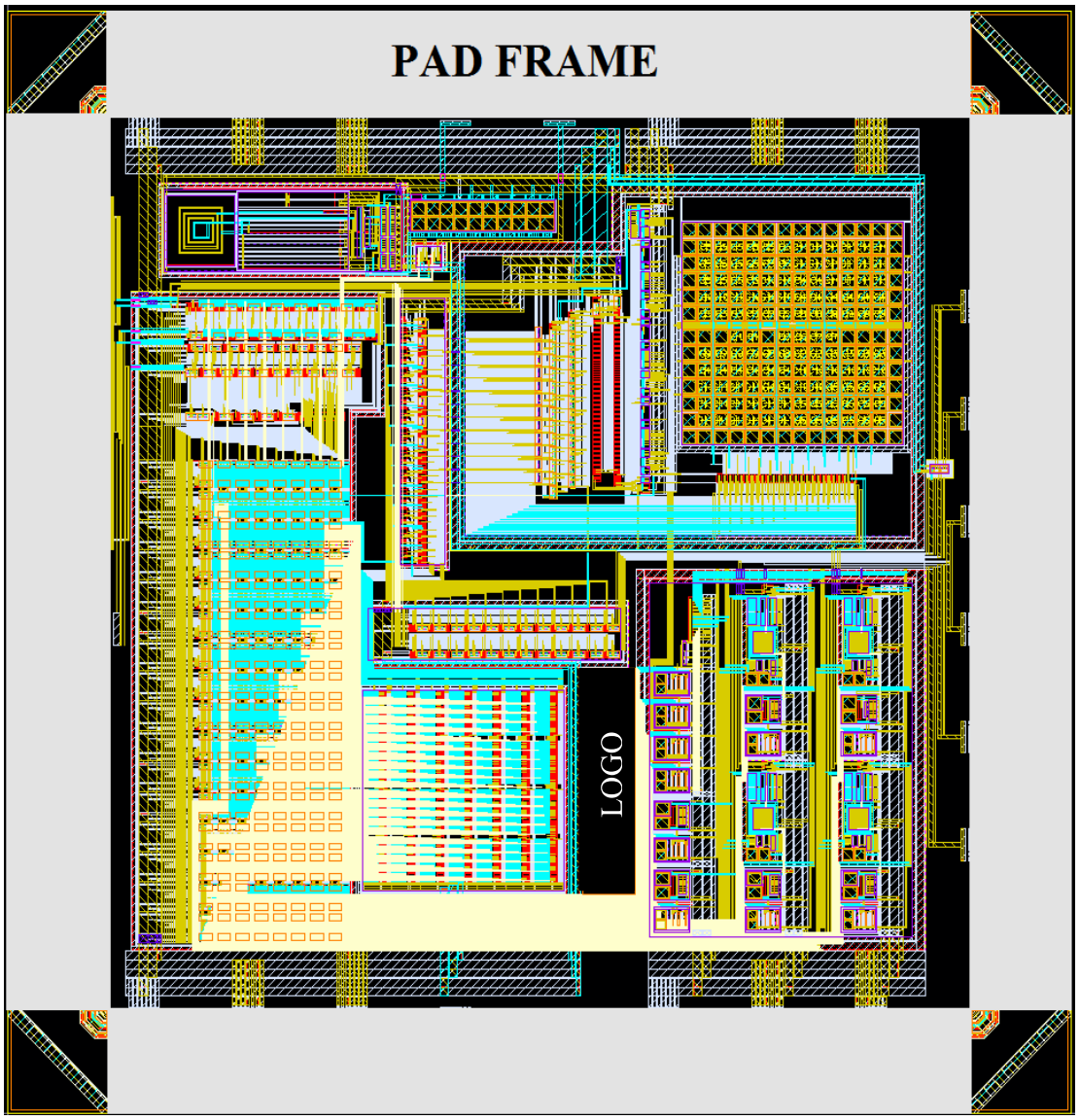


Figure 3.9 Top level layout of the temperature sensor chip implemented in a 2 mm × 2 mm area.

During the layout process the RC delay of the signals, signal coupling, parasitic capacitance, latch up, matching, and noise are considered deeply.

In order to simplify layout drawing of digital part of the design which is comprised of digital controller, output serializer, SAR logic, and timing of ADC a standard digital cell library is created.

The analog part of the design included temperature sensor and reference circuitry, comparator, DAC, and bias generator is drawn carefully regarding the

mismatches, noise distribution, and charge coupling. Matching is one of the most important concern in layout. The BJTs in the bandgap circuitry and capacitors in the split array DAC are drawn with respect to the common centroid technique to reduce the linear gradient errors. They are very critical blocks and affect the linearity. Besides dummy devices are used to ensure symmetry and reduce side gradients. Common centroid structure is applied for input stages of the amplifiers in the comparator and unity-gain amplifiers in bias generator as well as common centroid structure shows high matching performance.

Furthermore, critical signals and powers are shielded to avoid charge coupling. All of the blocks and critical sub-blocks are surrounded with the guard rings to minimize the injection of noise to substrate and prevent decoupling. Analog and digital powers are set apart from each other, besides all power lines are routed separately to all blocks to prevent charge and noise coupling.

# CHAPTER 4

# SIMULATION RESULTS

This chapter presents the simulation results of the core blocks and fundamental operations. All simulations are performed using the Spice circuit level simulator. The simulations of the core blocks are given first, then top level simulations are presented. All simulations are performed covering the full temperature range that is from -55°C to 125°C. Top level simulation is performed for 20 different temperature points for the full range to ensure a high level performance.

## 4.1 Bandgap Reference and Temperature Signal Generation

One of the most critical parts of the design is bandgap reference generation since it is used by the ADC block for reference signal and temperature independent current reference generation. Figure 4.1 shows the bandgap reference voltage variation with respect to temperature. The maximum variation is measured as 4.809 mV along the full temperature range. This errors mainly comes from the TC of the resistors used in the architecture and nonlinearity of the base-emitter voltage.

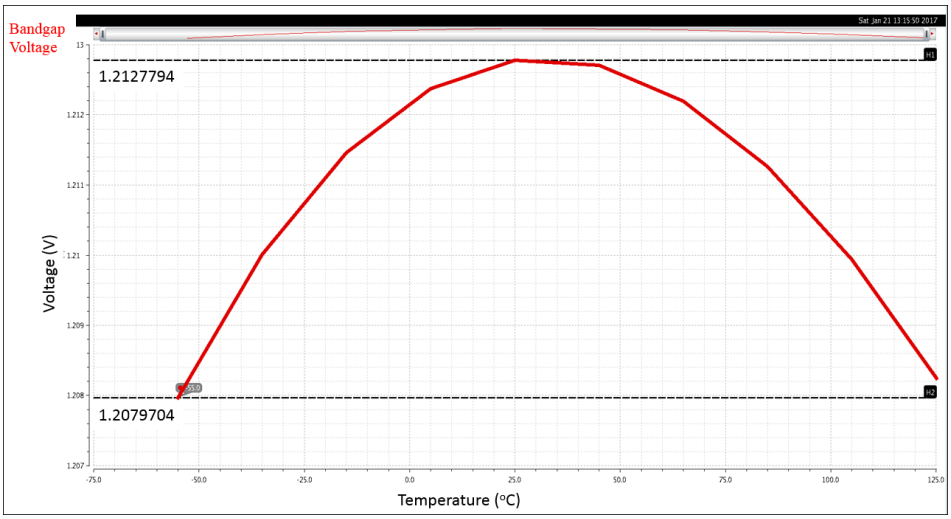


Figure 4.1 Bandgap reference voltage variation with respect to temperature.

Measured temperature signal is carried by PTAT voltage. Figure 4.2 gives the PTAT voltage variation with respect to temperature.

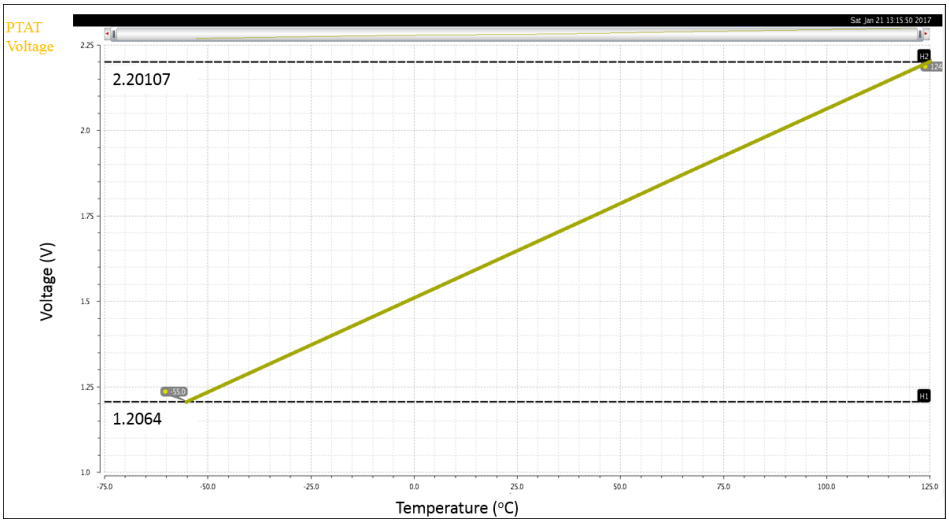


Figure 4.2 PTAT voltage variation with respect to temperature.

The nonlinearity of the PTAT voltage is measured as 0.2%. PTAT voltage variation is 1 V across the full range therefore, least significant voltage that must be detected by the ADC for 0.1 ℃ resolution is 0.555 µV as stated in Chapter 3. In order to detect least significant voltage corresponding 0.1 ℃ voltage change, the LSB voltage of the ADC must be equal to 0.555 µV. This will be justified in the next part while discussing the ADC simulations.

Low power consumption is the most crucial specification of the design. As a result, bias currents are kept as low as possible keeping the linearity and accuracy of the sensor as high as possible.

The total power consumption of the bandgap reference voltage and the temperature voltage generator block is 387 µW at worst case at 125℃.

## 4.2 Bias Generator

Figure 4.3 states the temperature variations of the high reference voltage, low reference voltage, common mode voltage, and reset voltage.

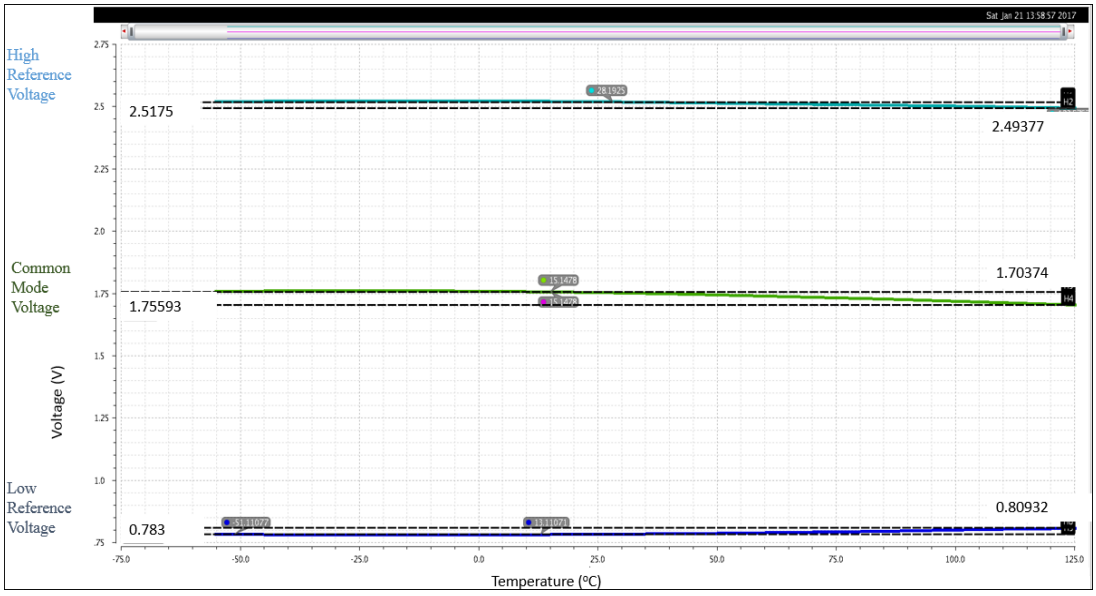


Figure 4.3 Transient response of the ADC bias voltages in full temperature range.

High and low voltage variations are ±11 mV and ±13 mV respectively. On the other hand, common mode and reset voltage variations are ±26 mV. Common mode and reset voltages are generated in same values, and their responses are the same, therefore their temperature dependence do not result in offset errors on the output data. However, reference voltages cause errors. These errors are tried to be minimized in the calibration logic.

Additionally, Figure 4.4 gives the variation of bias currents for gain stages and Schmitt trigger with respect to the temperature. Bias currents of gain stages are identical and

changes ±0.58 µA in full temperature range. On the other hand, variation of bias current of Schmitt trigger is ±3.4 µA. These variations in bias signals lead to static error in the ADC output and this error will be compensated in the calibration logic.

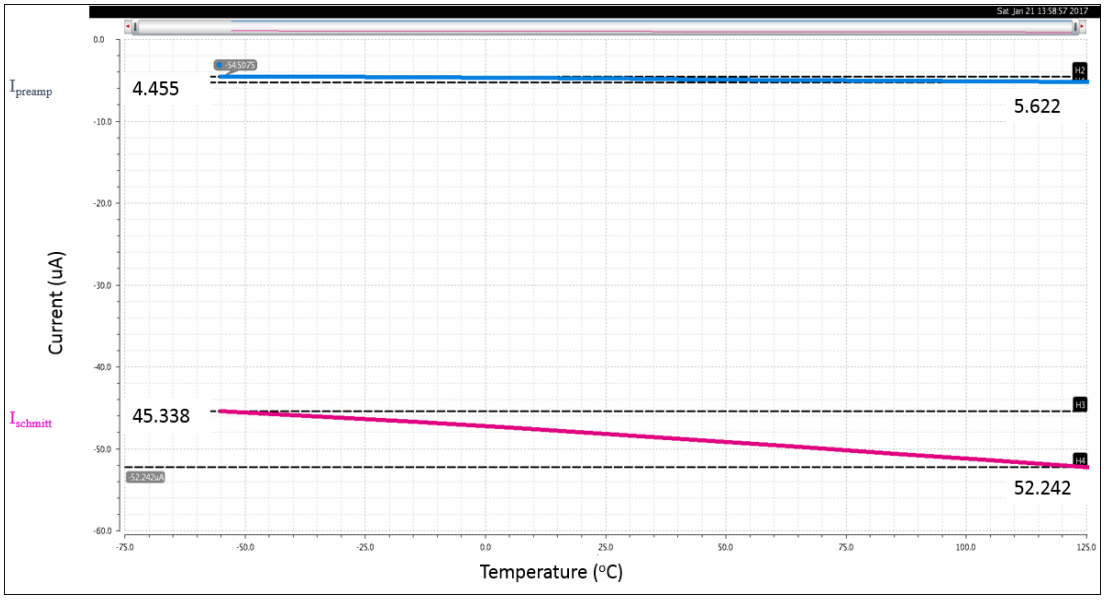


Figure 4.4 Temperature variation of the ADC bias signals.

## 4.3 Successive Approximation ADC

### 4.3.1 ADC Timing Signals

The ADC operation starts with an adc_start signal, then input voltage is sampled and successive approximation registers are reset at the rising half of the clock. At the falling clock conversion starts and first comparison is done. After each comparison, inputs of the preamplifiers and Schmitt trigger in comparator are reset to common mode voltage. Figure 4.5 shows the timing diagram of the ADC.

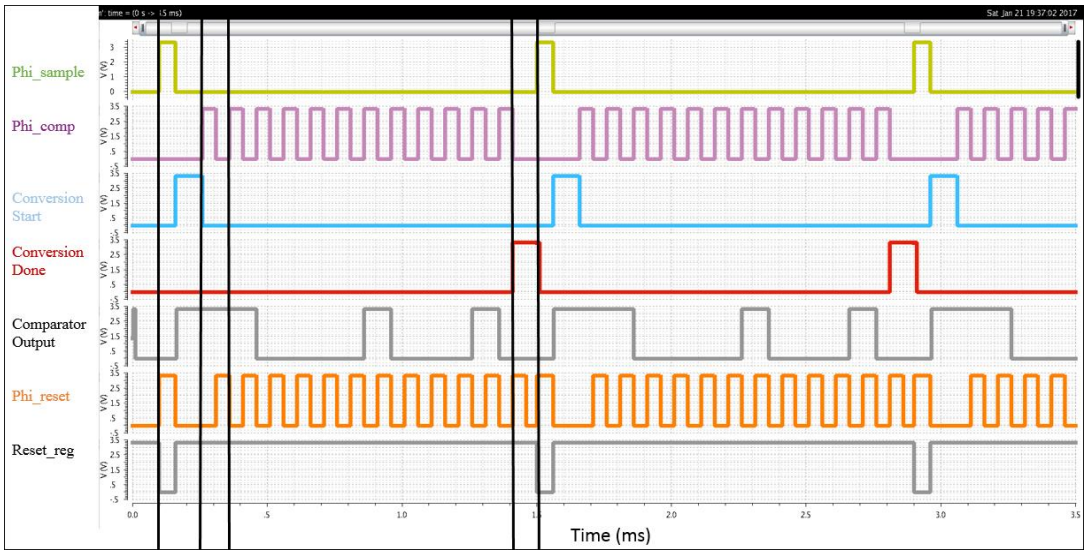


Figure 4.5 ADC timing diagram.

### 4.3.2 **Comparator**

Figure 4.6 presents the gain and the frequency response of differential preamplifiers in sequential order. The gain of each step is 20 dB.

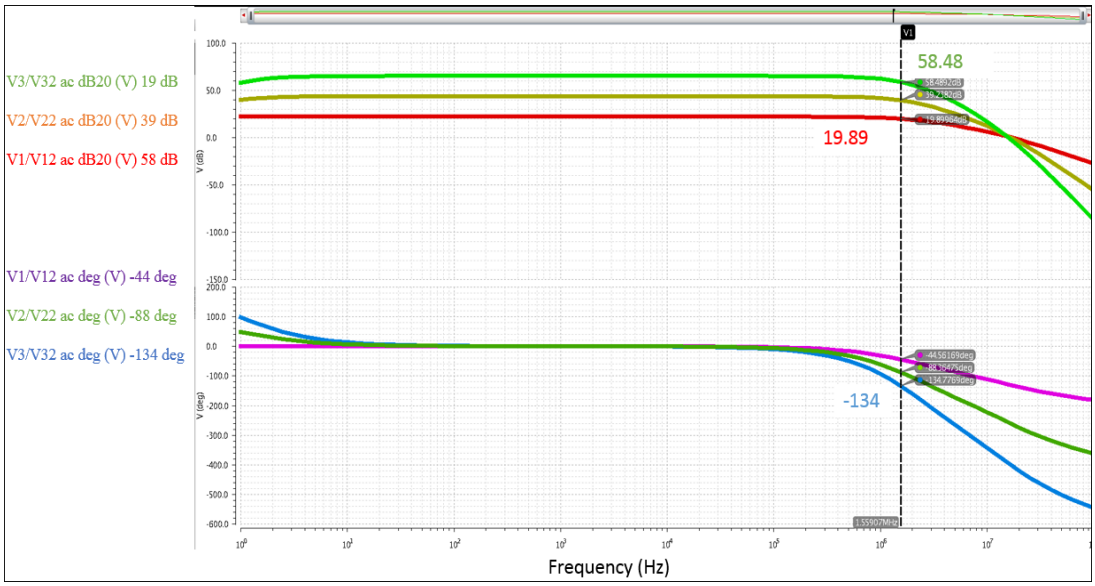


Figure 4.6 Gain and frequency response of the differential outputs of preamplifier chain.

The total input referred noise of the comparator is measured as shown in Figure 4.7. This is significantly smaller than half of the LSB voltage.

| Device | Param | Noise Contribution | % Of Total |
|---|---|---|---|
| I13.M0.m1 | id | 5.27998e-05 | 30.58 |
| I13.M4.m1 | id | 4.03408e-05 | 17.85 |
| I0.M14.m1 | fn | 2.67992e-05 | 7.88 |
| I0.M11.m1 | fn | 2.67992e-05 | 7.88 |
| I13.M11.m1 | id | 1.92701e-05 | 4.07 |
| I0.M10.m1 | id | 1.88077e-05 | 3.88 |
| I0.M9.m1 | id | 1.88077e-05 | 3.88 |
| I0.M14.m1 | id | 1.77942e-05 | 3.47 |
| I0.M11.m1 | id | 1.77942e-05 | 3.47 |
| I0.M13.m1 | fn | 1.76233e-05 | 3.41 |

Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Summarized Noise = 9.54862e-05
Total Input Referred Noise = 2.42968e-05
The above noise summary info is for noise data

Figure 4.7 The total input referred noise of the comparator.

### 4.3.3 **Successive Approximation Logic**

Each SAR bit goes high at it determination step than its value is determined with respect to comparator output at that time. Figure 4.8 shows justification of the operation of successive approximation register logic.

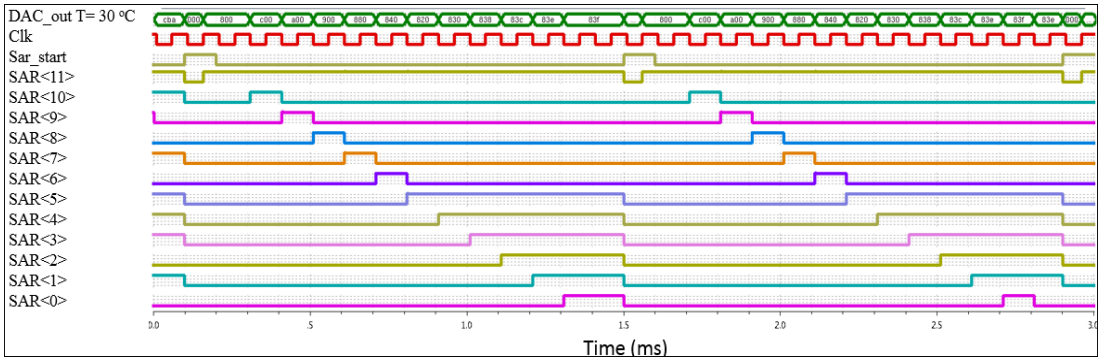


Figure 4.8 SAR operation diagram.

## 4.4 Serializer

Serializer starts transmission from the least significant bit to the most significant bit. Figure 4.9 shows the transmission of 12-bit temperature data for temperatures -13℃, 6℃, and 25℃. Digital temperature data is loaded to the serializer with rising conv_done signal and serializer starts transmission by rising dval signal which implies output data is valid. Conversion done signal is synchronized with the rising edge of the clock and sterilizer gives the serial output data at the falling edge of the clock. Moreover, ADC SAR registers are updated at the rising edge of the clock while comparison is done at the falling edge of the clock.

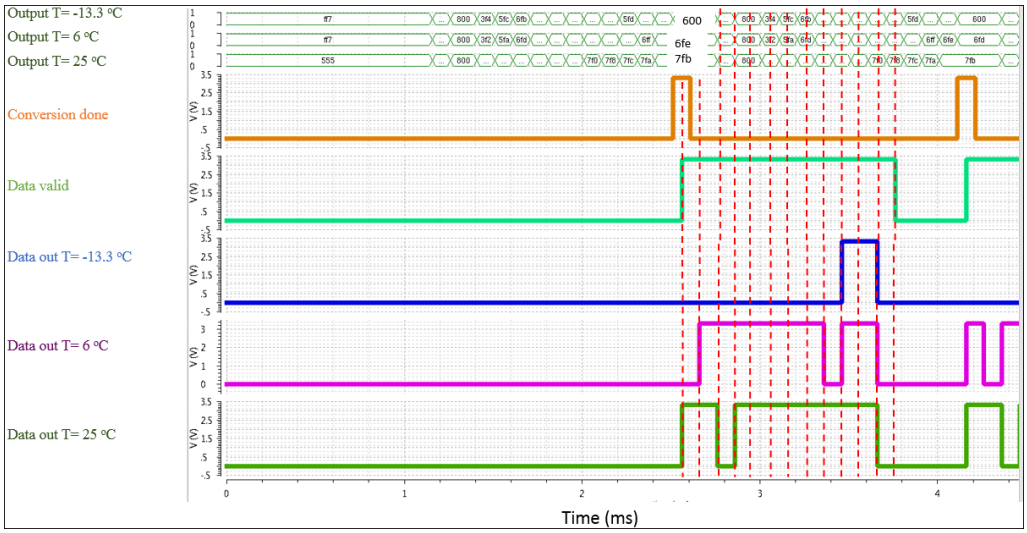


Figure 4.9 Output serializer data transmission.

## 4.5 Top Level Simulation

Simulation of the full system is performed for twenty different points for three different simulation setups throughout the full temperature range.

First, in order to eliminate temperature variations of bias signals and show ADC internal inaccuracy, and nonlinearity of the PTAT voltage, constant bias voltage and currents are used. 12-bit ADC output data with respect to temperature voltage is shown in Figure 4.10. The simulation is from -55℃ to 125 ℃ with 10.5 ℃ temperature step. The non-linearity of the PTAT voltage is calculated as 0.2%.

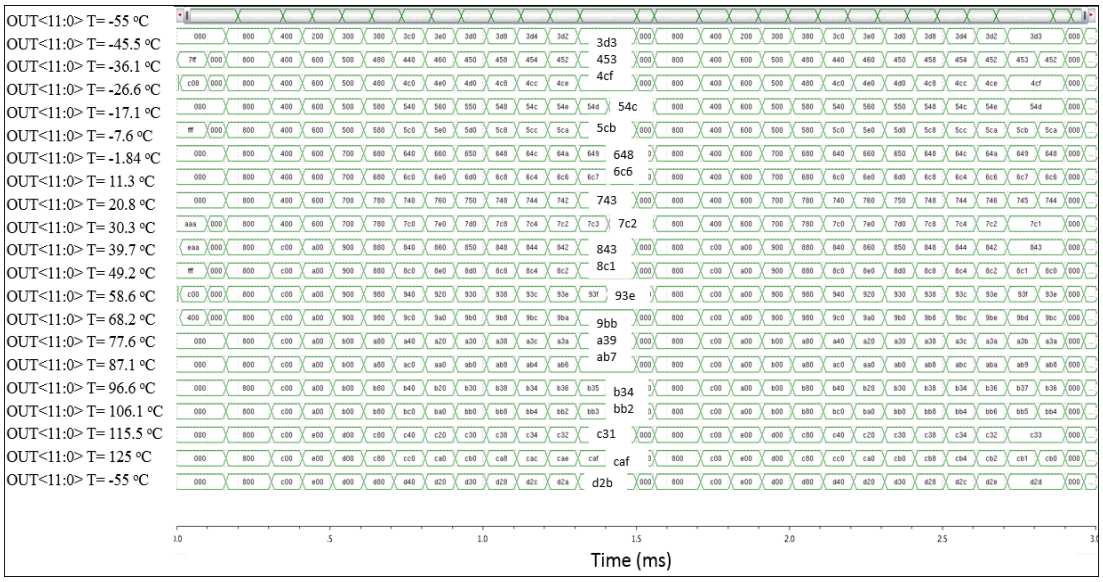


Figure 4.10 Simulation of the temperature voltage and SAR ADC with constant bias signals.

The accuracy of the system can be seen in Figure 4.11.

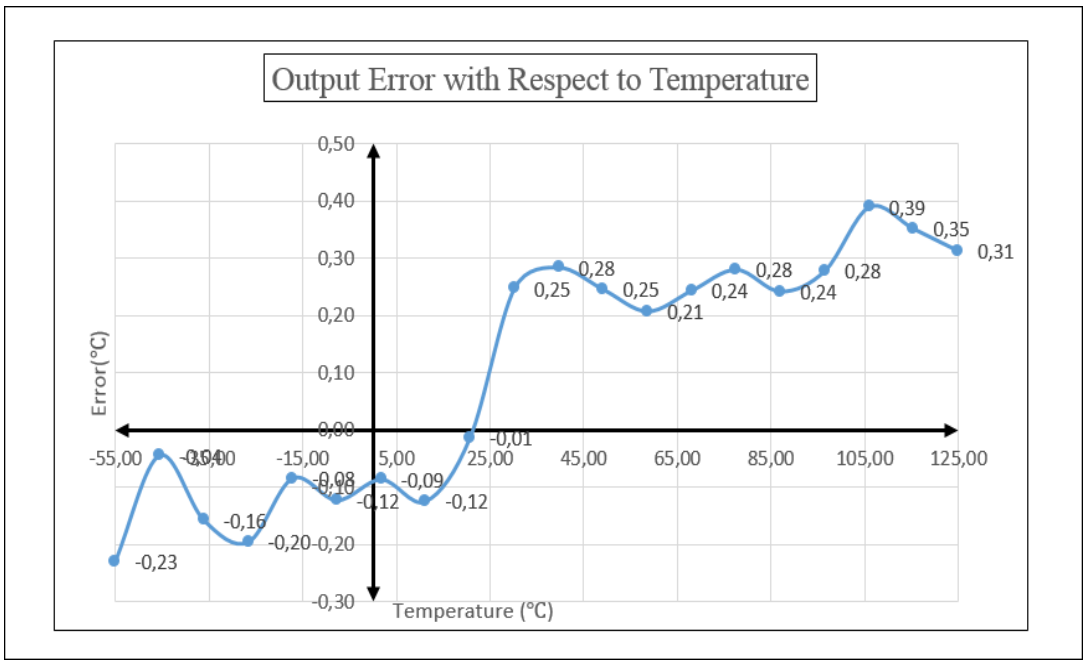


Figure 4.11 Accuracy error of the simulation with respect to temperature.

In the second step bias generator is activated and 12-bit ADC output data for same temperature points is given in Figure 4.12.

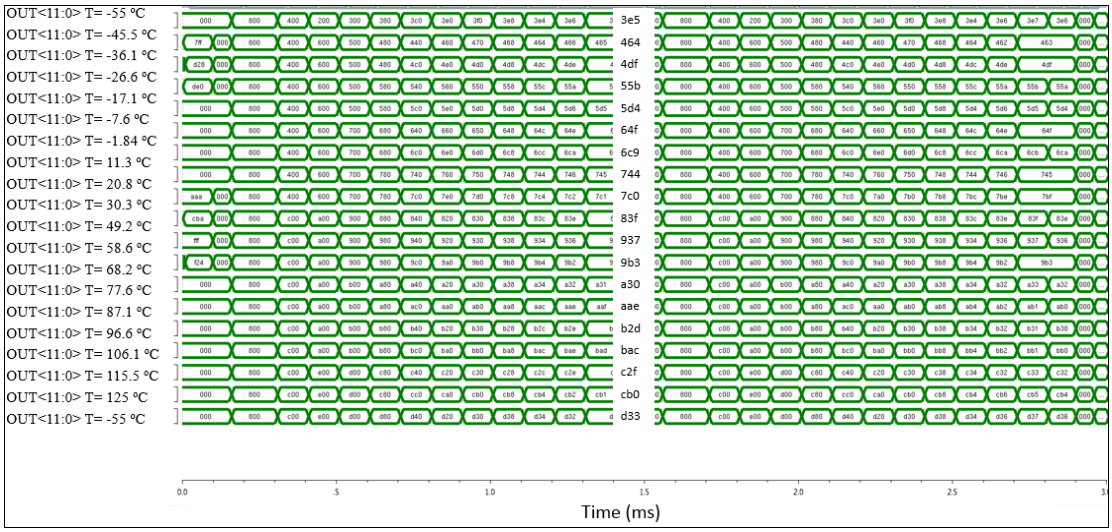


Figure 4.12 ADC outputs with simulation of the system with activation of bias generator.

Figure 4.13 presents the accuracy of the system where the ADC outputs are not calibrated yet.

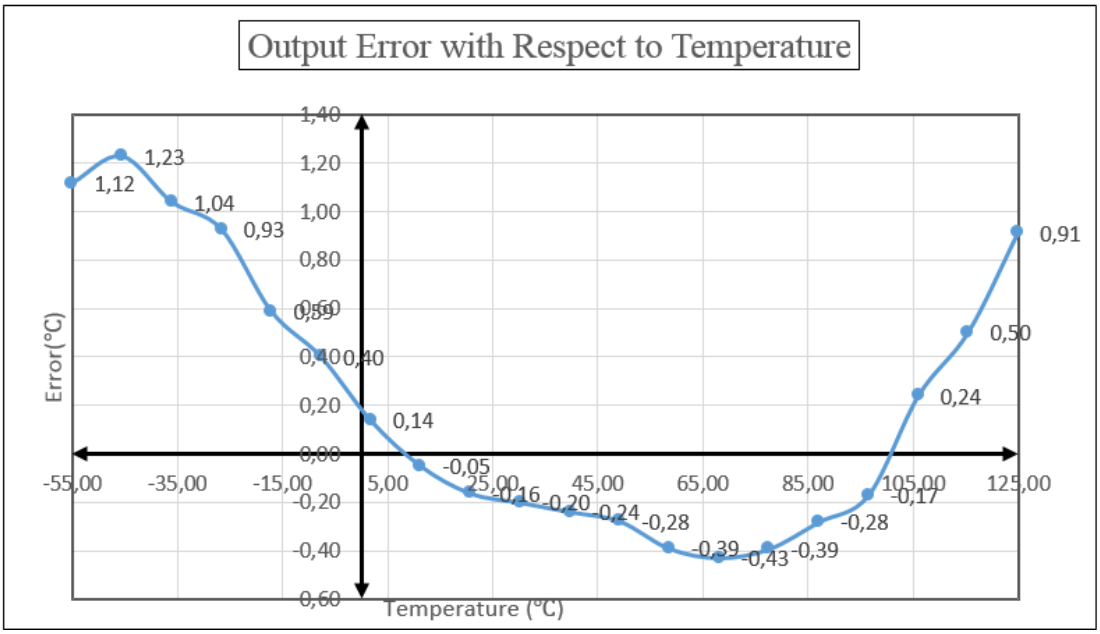


Figure 4.13 Accuracy error of the system without calibration.

In the last step, full chip simulation is performed with activation of calibration logic block. Figure 4.14 shows 12-bit outputs of the full chip simulation with respect to temperature.

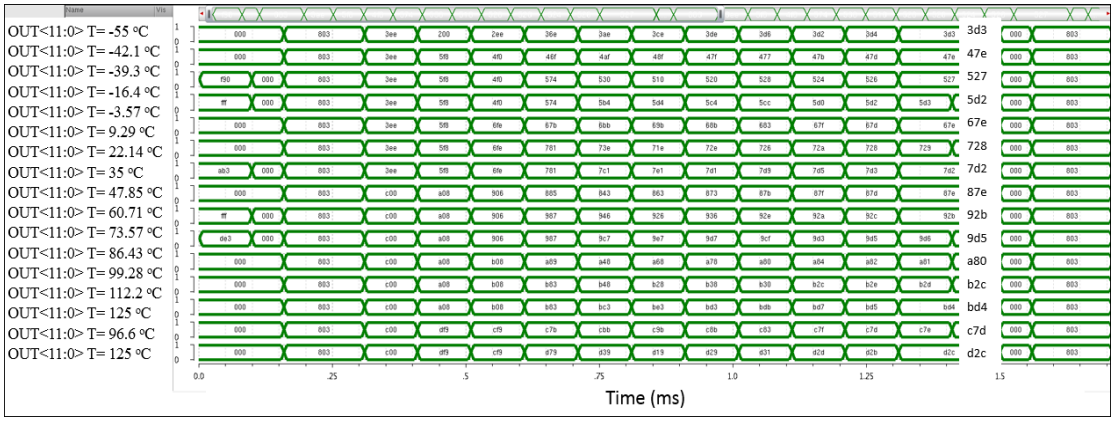


Figure 4.14 System outputs of the full chip simulation with respect to temperature.

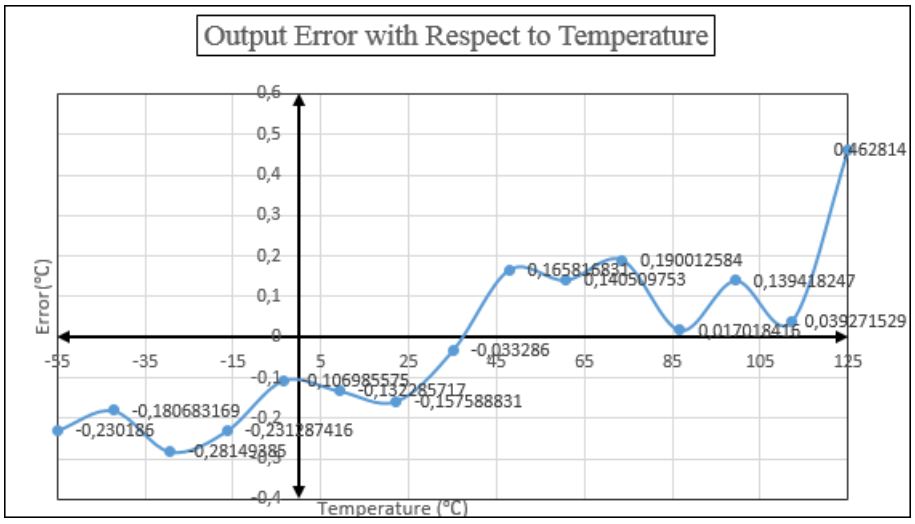


Figure 4.15 Accuracy error of the sensor along the full temperature range.

The total power consumption of the bandgap reference generation, digital blocks and ADC block is 1 mW at the worst case. The total power consumption of the full chip including the bias generator increased to 2 mW at the worst case.

Table 4.1 gives the comparison of the implemented temperature sensor with other examples in the literature. Note that the comparison is stated between the simulation results of the proposed work and the test results of the fabricated sensors of given works. The test results of the proposed work are expected to vary due to fabrication process however this change is going to try to be minimized with calibration. Implemented smart temperature sensor stands on a good position regarding the resolution and accuracy with respect to compared sensors. Note that the stated accuracies of the other sensors are after the packaging of wafer-level calibration. Furthermore, this sensor operates between -55 ℃ to 125 ℃ with reasonable low power consumption considering the architecture of the system. In addition, this sensor provides the widest temperature range with respect to similar works in the literature

Table 4.1 Performance comparison of the temperature sensors.

| **Reference** | **[34]** | **[12]** | **[22]** | **[35]** | **This work*** |
|---|---|---|---|---|---|
| Technology | 0.032 µm | 0.7 µm | 0.7 µm | 0.5 µm | 0.35 µm |
| Architecture | Bandgap +V/F | Bandgap +TDC | Bandgap Sigma Delta ADC | Bandgap +SAR | Bandgap +SAR |
| Output Type | Digital | Digital | Digital | Digital | Digital |
| Temperature Range (℃) | -10 to 110 | 0 to 100 | -40 to 130 | 10 to 100 | -55 to 125 |
| Accuracy (℃) | ±2 | 0.3-3 | ±1 | 0.26 | -0.23-0.46 |
| Resolution (℃) | 0.19 | 0.001-1 | 8-bits | 11 bit | 0.08 |
| Power Consumption (mW) | 3.78 | 0.125-2.5 | 0.012 | 6.5 | 2 |
| Area ($mm^2$) | 0.02 | 1.5 | 1.5 | 2.04 | 4 |

*Performance parameters of this work are based on the simulation results.

# CHAPTER 5

## SUMMARY AND FUTURE WORK

The main research motivation of this thesis is focused on the low power smart temperature sensor for on-chip temperature monitoring applications. For this purpose, design and implementation of a low power integrated temperature sensor with digital outputs is presented. The chip is implemented with a 0.35 μm CMOS process and submitted to foundry for fabrication. All essential simulations of the critical blocks and top system are performed in order to verify the functionality of the sensor. The performance parameters which satisfy the specification of the sensor are analyzed.

In the lights of the analyses and results of the presented work, the achievements of this thesis can be summarized as;

1. The electrical temperature sensors are investigated and IC smart temperature sensor architectures are focused. The principle behind the operation basics are stated in detail.
2. In order to digitalize the temperature signal for high system integrity, design and implementation of the SAR ADC is performed. The advantages and disadvantages of the ADC types are compared regarding the system requirements.
3. The capacitive DAC types are analyzed for low INL and DNL ratios. The split capacitive DAC is designed based on the low noise limitation. The design of

the comparator is stated with the deep explanation of gain and noise perspectives.

4. All bias voltages and currents of the ADC are generated by the bias generator block internally. Thus, no external voltage or current source is required for sensor operation except from the power supply.
5. All timing signals necessary for system operation is generated by digital controller which communicates with external electronics via SPI. Digital controller stores the SPI data in configuration memory.
6. On-chip calibration providing high accuracy is executed for twenty different regions of full temperature range.
7. Size of the sensor is 2 mm x 2 mm, realized with a 0.35 μm CMOS process.
8. Total power consumption of the bandgap generation and ADC block is 1 mW whereas the power consumption of the sensor is 2mW at worst case.
9. Simulation results are presented to justify the operation and performance parameters of the sensor is analyzed.

Verification of the design and implementation of sensor is conducted with Spice simulations, however, there is still some works to perform. The list of the planned flow is as follows;

1. The Printed Board Circuitry should be implemented for the physical tests of the temperature sensor.
2. Software and firmware should be written in order to perform the tests.
3. Calibration of the manufactured chip is performed in environmental temperature chamber with a high accuracy temperature sensor.
4. Full system and block level verification tests should be performed on manufactured chip in order to ensure the performance of the sensor.
5. Modification of calibration logic and curvature correction technique for PTAT voltage can be improved in order to obtain high accuracy system.
6. In order to decrease the power consumption, replacement of SAR ADC with a Sigma-Delta ADC and integration of the PTAT voltage and Sigma-Delta ADC can be considered.

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