# DESIGN AND IMPLEMENTATION OF AN UNREGULATED DC-DC TRANSFORMER MODULE USING LLC RESONANT CONVERTER

## A THESIS SUBMITTED TO THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES OF MIDDLE EAST TECHNICAL UNIVERSITY

BY

## ÖZTÜRK ŞAHİN ALEMDAR

## IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONICS ENGINEERING

DECEMBER 2016

Approval of the thesis:

## DESIGN AND IMPLEMENTATION OF AN UNREGULATED DC-DC TRANSFORMER MODULE USING LLC RESONANT CONVERTER

submitted by ÖZTÜRK ŞAHİN ALEMDAR in partial fulfillment of the requirements for the degree of Master of Science in Electrical and Electronics Engineering Department, Middle East Technical University by,

Prof. Dr. Gülbin Dural Ünver Dean, Graduate School of Natural and Applied Science	es
Prof. Dr. Tolga Çiloğlu Head of Department, <b>Electrical and Electronics Engine</b>	eering
Assist. Prof. Dr. Ozan Keysan Supervisor, Electrical and Electronics Engineering De	pt
Examining Committee Members:	
Prof. Dr. Muammer Ermiş Electrical and Electronics Engineering Dept., METU	
Assist. Prof. Dr. Ozan Keysan Electrical and Electronics Engineering Dept., METU	
Prof. Dr. Işık Çadırcı Electrical and Electronics Engineering Dept., Hacettepe University	
Assoc. Prof. Dr. Mehmet Timur Aydemir Electrical and Electronics Engineering Dept., Gazi University	
Assist. Prof. Dr. İbrahim Mahariq Electrical and Electronics Engineering Dept., University of Turkish Aeronautical Association	
Date:	20 December 2016

I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

> Name, Last Name : ÖZTÜRK ŞAHİN ALEMDAR Signature :

#### ABSTRACT

# DESIGN AND IMPLEMENTATION OF AN UNREGULATED DC-DC TRANSFORMER MODULE USING LLC RESONANT CONVERTER

Alemdar, Öztürk Şahin M.S., Department of Electrical and Electronics Engineering Supervisor: Assist. Prof. Dr. Ozan Keysan

December 2016, 137 pages

A traditional high-power front-end DC-DC converter can be replaced with an array of paralleled standardized converter modules when modular design is applied. Modular front-end DC-DC converters represent many desirable properties such as expandability of output power capacity, redundancy implementation, simplified thermal management, and reduced design cost. However, in order to benefit from modular design, load current sharing must be accomplished among the paralleled modules. In this thesis, an LLC resonant converter is proposed as an unregulated DC-DC transformer (DCX) module for modular front-end DC-DC converter applications. In order to achieve current sharing capability, the droop current sharing method is employed in the LLC DCX module. To implement the droop method, both voltage feedback loop of the converter and inherent gain characteristic of the LLC resonant converter topology are utilized. To select the circuit components of the proposed module, a methodical design process is presented. Practical design considerations including planar transformer implementation, secondary-side rectifier selection, primary-side MOSFET selection and control loop implementation are investigated. A 500kHz 200W LLC DCX module converting 360-400VDC input to 12.5-11.75VDC output is built and its performance characteristics are demonstrated. The dimension of the module is 106mm  $\times$  61mm  $\times$  13mm and it achieves 89.9% efficiency at full load. A two-module array 400W front-end DC-DC converter and a three-module 400W front-end DC-DC converter having 2+1 redundancy configuration are implemented to demonstrate both steady-state and transient current sharing performance of the proposed module.

Keywords: LLC resonant converter, DC-DC transformer, DCX, current sharing, modular power converter.

# LLC REZONANT ÇEVİRİCİ KULLANARAK REGÜLE OLMAYAN DA-DA TRAFO TASARIMI VE GERÇEKLENMESİ

Alemdar, Öztürk Şahin

Yüksek Lisans, Elektrik ve Elektronik Mühendisliği Bölümü Tez Yöneticisi: Yrd. Doç. Dr. Ozan Keysan

#### Aralık 2016, 137 sayfa

Modüler tasarım sayesinde geleneksel yüksek güçlü bir ön-uç DA-DA çevirici, birbirine parallel standart çevirici modüllerinden oluşan bir dizi ile yer değiştirilebilir. Modüler ön-uç DA-DA çeviriciler çıkış gücünün arttırılabilir olması, yedeklilik uygulanabilmesi, basit 1s1l yönetim, düşük tasarım maliyeti gibi birçok istenen özelliğe sahiptirler. Ancak, modüler tasarımdan fayda sağlanması için birbirine parallel modüller arasında yük akımı paylaşımı sağlanmalıdır. Bu tez çalışmasında, LLC rezonant çeviricinin modüler ön-uç DA-DA çevirici uygulamalarında regüle olmayan bir DA-DA trafo (DCX) olarak kullanılması önerilmiştir. LLC DCX modüle akım paylaşım kabiliyetinin kazandırılması için gerilim düşümü akım paylaşım yöntemi kullanılmıştır. Gerilim düşümü yönteminin uygulanmasında gerilim geri besleme döngüsü ve LLC rezonant çeviricinin kendine has kazanç karakteristiği kullanılmıştır. Önerilen modülün devre elemanlarının belirlenmesi için sistemli bir tasarım süreci sunulmuştur. Düzlemsel trafonun gerçeklenmesini, sekonder taraf için doğrultucu seçimini, primer taraf için MOSFET seçimini ve kontrol döngüsünün gerçeklenmesini içeren pratik tasarım konuları incelenmiştir. 360-400VDA giriş gerilimini 12.5-11.75VDA çıkış gerilimine çeviren 500kHz 200W'lık bir LLC DCX modül ortaya konmuş ve bu modülün performans karakteristikleri sunulmuştur. 106mm × 61mm × 13mm

ölçülere sahip modülün verimi tam yükte %89.9 olarak ölçülmüştür. Önerilen modülün sürekli ve süreksiz durumda akım paylaşım performansının gözlemlenmesi amacıyla iki modülden oluşan 400W'lık ön-uç DA-DA çevirici ile üç modülden oluşan 2+1 yedeklilik yapısına sahip 400W'lık ön-uç DA-DA çevirici gerçeklenmiştir.

Anahtar Kelimeler: LLC rezonant çevirici, DA-DA trafo, DCX, akım paylaşımı, modüler güç çevirici.

To my wife

To my family

#### ACKNOWLEDGMENTS

Firstly, I would like to express my sincere gratitude to Assist. Prof. Dr. Ozan Keysan for his continuance motivation, significant guidance and endless encouragement. I feel really lucky to be one of his first graduate students.

I would also like to express my gratitude to my committee members: Prof. Dr. Muammer Ermiş and Prof. Dr. Işık Çadırcı for helping me develop my background in power electronics.

I would like to thank ASELSAN Inc. for its valuable support throughout my graduate studies. Outstanding laboratory and component resources have benefited my work greatly.

I would also like to thank my director H. Aydın Yahşi and my colleagues Özgür Yaman and M. Tufan Ayhan for their enduring support and encouragement.

There is no words of thanks or gratitude that can represent my indebtedness to my family. I am very thankful for their unending support during my whole life.

And lastly, I would like to express my heartfelt thanks to my wife Ünzile Oral Alemdar. I feel deeply grateful to her for her endless patience, support and motivation not only for this study but also at every aspect of my life.

## **TABLE OF CONTENTS**

ABSTRACT
ÖZvii
ACKNOWLEDGEMENTS x
TABLE OF CONTEXT xi
LIST OF TABLES xiv
LIST OF FIGURES xix
LIST OF ABBREVIATIONS xx
LIST OF SYMBOLS xxi
CHAPTERS 1
1. INTRODUCTION1
1.1. DC Distributed Power Systems
1.2. Modular Front-end DC-DC Converter
1.3. Power Supply Architecture in Phased-array Radar Systems
1.4. LLC Resonant Converter for DCX Module Design
1.4.1. Operation at Resonance
1.4.2. Below-resonance Operation
1.4.3. Above-resonance Operation
1.5. Literature Review
1.6. Thesis Outline
2. DESIGN OF CURRENT SHARING METHOD

	2.1.	Droop Current Sharing Method	.23
	2.2.	Droop Voltage Implementation by using Inherent Load Regulation	
	Chara	ecteristic	. 29
	2.3.	Droop Voltage Implementation by using Resonant Tank	. 32
	2.4.	Droop Voltage Implementation by using Voltage Feedback Loop	.37
3	. DE	ESIGN OF LLC DCX MODULE	.41
	3.1.	Voltage Transfer Function of the LLC Resonant Converter	.41
	3.2.	Selection of L <sub>n</sub> and Q <sub>e</sub> Parameters	.47
	3.3.	Maximum Gain Requirement of the LLC DCX Module	. 50
	3.4.	Design Method Developed for the LLC DCX Module	. 55
	3.5.	Required Inductive Energy for ZVS	. 60
4	. IM	PLEMENTATION OF LLC DCX MODULE	. 63
	4.1.	Planar Transformer Design	. 63
	4.1	.1. Leakage Inductance of the Planar Transformer	.73
	4.2.	Secondary-side Rectifiers	.77
	4.2	.1. Loss calculation for secondary-side rectifiers	. 80
	4.3.	Primary-side MOSFETs	. 83
	4.3	.1. Loss calculation for primary-side MOSFETs	. 85
	4.4.	Building Blocks of the LLC DCX Converter	. 88
	4.5.	Voltage Feedback Loop Design	.91
5	. EX	PERIMENTAL RESULTS	101
	5.1.	Test Results of Individual LLC DCX Module	101
	5.2.	Test Results of Modular Front-end DC-DC converter	112
	5.2	.1. Two-module 400W Front-end DC-DC converter	112
	5.2	.2. 2+1 Three-module Front-end DC-DC converter	115

6. C	CONCLUSIONS and FUTURE WORK	119
6.1.	Conclusions	119
6.2.	Future Work	121
REFE	RENCES	123
APPENDIX		

## LIST OF TABLES

## TABLES

Table 2-1. Primary-side resistances of the LLC DCX module. 31
Table 2-2. Secondary-side resistances of the LLC DCX module.    31
Table 2-3. The tolerances of the components selected for the LLC DCX module.35
Table 3-1. Circuit parameters resulting from the selected $\sqrt{Lr/Cr}$ value
Table 3-2. Rearranged circuit parameters. 60
Table 4-1. Skin depth of copper for different operating frequencies.    67
Table 4-2. Comparison of FERD20U50 and two Schottky diodes.    79
Table 4-3. The key parameters of the primary-side MOSFET: STL33N60M285
Table 5-1. Steady-state current sharing performance of the 2+1 front-end DC/DC
converter

## LIST OF FIGURES

## FIGURES

Fig. 1-1. (a) Distributed Power System. (b) DPS with modular approach2
Fig. 1-2. (a) Modular front-end DC/DC converter. (b) Current sharing without
forced current sharing control
Fig. 1-3. (a) Sample single output power supply: MEAN WELL RCP-1000-48 [9].
(b) Block diagram of RCP-1000-487
Fig. 1-4. (a) Sample multiple output power supply: MEAN WELL IPC-300A [10].
(b) Block diagram of IPC-300A7
Fig. 1-5. Modular front-end DC/DC converter based on DCX modules
Fig. 1-6. Modular front-end DC/DC converter based on interleaved modules 10
Fig. 1-7. Six-module phased-array radar system [23]11
Fig. 1-8. DPS architecture developed for a phased-array radar system 12
Fig. 1-9. LLC resonant converter
Fig. 1-10. Voltage gain characteristic of the LLC resonant converter
Fig. 1-11. Operating point of the LLC resonant converter at resonance 15
Fig. 1-12. Current and voltage waveforms of the LLC resonant converter at
resonance16
Fig. 1-13. Operating region of the LLC resonant converter at below resonance 17
Fig. 1-14. Current and voltage waveforms of the LLC resonant converter at below
resonance
Fig. 1-15. Operating region of the LLC resonant converter at above resonance 19
Fig. 1-16. Current and voltage waveforms of the LLC resonant converter at above
resonance
Fig. 2-1. (a) Parallel connection of two power converters. (b) Load regulation
characteristics of the paralleled converters

Fig. 2-2. Effect of the mismatch in output voltage set points on current sharing
accuracy: (a) Large mismatch. (b) Small mismatch. (c) No mismatch [22]25
Fig. 2-3. Effect of the load regulation slope on current sharing accuracy: (a) Large
slope. (b) Small slope. (c) Zero slope [22]25
Fig. 2-4. Load regulation characteristic of the LLC DCX module
Fig. 2-5. Load regulation characteristics of N LLC DCX modules connected in
parallel27
Fig. 2-6. Required droop characteristic for the LLC DCX module
Fig. 2-7. DC equivalent circuit of the LLC resonant converter at fixed resonant
frequency operation
Fig. 2-8. Droop characteristic of the LLC DCX module at fixed resonant frequency
operation
Fig. 2-9. Inherent voltage gain characteristic of the LLC resonant converter33
Fig. 2-10. Droop voltage implementation by using resonant tank
Fig. 2-11. Two-module array with mismatch in resonant tanks35
Fig. 2-12. Schematic of the two-module array built in Simplorer
Fig. 2-13. Current sharing performance of the two-module array
Fig. 2-14. The block diagram of the active droop method
Fig. 2-15. Operating line of the LLC DCX module
Fig. 2-16. The block diagram of the active droop method employed in the LLC
DCX module
Fig. 3-1. Building blocks of the LLC resonant converter
Fig. 3-2. The equivalent circuit of the converter
Fig. 3-3. The equivalent circuit of the converter with FHA method
Fig. 3-4. Plots of $M_g$ with different $L_n$ and $Q_e$ combinations: (a) $L_n = 5$ , (b) $L_n =$
10, (c) $L_n = 15$
Fig. 3-5. A typical operating region of a conventional LLC resonant converter 47
Fig. 3-6. Relationship between attainable peak gain and Ln-Qe combination [42].48
Fig. 3-7. Redrawn attainable peak gain curves
Fig. 3-8. DC equivalent circuit of the LLC DCX

Fig. 3-9. Forward voltage drop versus forward current characteristic of
FERD20U50 device [57]
Fig. 3-10. Gain requirement of the LLC DCX module for different input voltages.
Fig. 3-11. The relationship between $M_{g_max}$ and $Q_e$ for different $\sqrt{Lr/Cr}$ values 55
Fig. 3-12. Peak gain curves with $M_{g_max}$ -Qe curves
Fig. 3-13. Voltage derating characteristics of EPCOS MKP series [39] 57
Fig. 3-14. Selection of $\sqrt{Lr/Cr}$ parameter
Fig. 3-15. Circulating magnetizing current (a) before turning on Q <sub>2</sub> , (b) before
turning on Q <sub>1</sub>
Fig. 3-16. Equivalent circuit of the LLC resonant converter during the dead time 61
Fig. 4-1. Prototype of the proposed LLC DCX module
Fig. 4-2. Transformer of the LLC DCX module
Fig. 4-3. Maximum flux density swing [49]
Fig. 4-4. E32/6/20 planar E core: (a) single E-shaped half (b) dimensions in mm
(c) transformer core [40]66
Fig. 4-5. Core loss curves of 3F4 material [50]
Fig. 4-6. (a) Transformer windings. (b) Interleaved winding structure
Fig. 4-7. 8-turn 8-layer PCB manufactured for the primary winding69
Fig. 4-8. 4-turn 4-layer PCB manufactured for the secondary winding 69
Fig. 4-9. Transformer winding: (a) sandwiched PCBs. (b) with planar E core 70
Fig. 4-10. Loss breakdown of the planar transformer73
Fig. 4-11. MMF distribution through the planar transformer
Fig. 4-12. (a) A typical structure of an FERD device [56]. (b) Schematic
representation of an FERD device [55]77
Fig. 4-13. Secondary-side rectifier: FERD20U50 (a) top side (b) bottom side 78
Fig. 4-14. Current waveform of each secondary-side rectifier
Fig. 4-15. Average forward power dissipation versus average forward current
curves for FERD20U50 [57]
Fig. 4-16. Reverse leakage current versus applied reverse voltage for FERD20U50
[57]

Fig. 5-8. Output voltage response to a load step of 1A to 17A: $CH_1 = I_0$ (orange),
$CH_4 = V_o \text{ (green)}.$ 107
Fig. 5-9. Output voltage response to a load step of 17A to 1A: $CH_1 = I_0$ (orange),
$CH_4 = V_o \text{ (green)}.$ 107
Fig. 5-10. Output voltage ripple at full load condition: $CH_1 = I_o$ (orange), $CH_4 = V_o$
(green)
Fig. 5-11. Two heat sinks used for the module
Fig. 5-12. Thermal image of the upper side of the module 110
Fig. 5-13. Thermal image of the bottom side of the module
Fig. 5-14. Two-module array 400W front-end DC/DC converter 112
Fig. 5-15. Current sharing error between two modules
Fig. 5-16. Current sharing response of two modules to a load step of 17A to 34A:
$CH_1 = I_o$ of Module 1 (orange), $CH_2 = I_o$ of Module 2 (blue), $CH_4 = V_o$ (green).113
Fig. 5-17. Current sharing response of the modules to a load step of 34A to 17A:
$CH_1 = I_o$ of Module 1 (orange), $CH_2 = I_o$ of Module 2 (blue), $CH_4 = V_o$ (green).114
Fig. 5-18. Three-module array having 2+1 redundancy configuration 115
Fig. 5-19. Transient current sharing performance of the three-module array: $CH_1 =$
$I_o$ of Module 1 (orange), $CH_2 = I_o$ of redundant module (blue) 117
Fig. 5-20. Output voltage response of the three-module array: $CH_4 = Output$
Voltage (green) 117

## LIST OF ABBREVIATIONS

AC	Alternating Current
CTR	Current Transfer Ratio
dB	Decibel
DC	Direct Current
DCX	DC-DC Transformer
DPS	Distributed Power System
DSP	Digital Signal Processor
EA	Error Amplifier
ESR	Equivalent Series Resistance
FERD	Field Effect Rectifier Diode
FEA	Finite Element Analysis
FHA	First Harmonic Approximation
IC	Integrated Circuit
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PCB	Printed Circuit Board
PFC	Power Factor Correction
PoL	Point of Load
PWM	Pulse Width Modulation
RMS	Root Mean Square
SR	Synchronous Rectification
T/R	Transmit/Receive
VCO	Voltage Controlled Oscillator
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

## LIST OF SYMBOLS

Ae	Effective Cross-sectional Area of Magnetic Core
$A_L$	Inductance Factor
В	Magnetic Flux Density
B <sub>max</sub>	Maximum Magnetic Flux Density
B <sub>min</sub>	Minimum Magnetic Flux Density
С	Capacitance
CBOOT	Bootstrap Capacitor
$C_{eq}$	Equivalent Drain-Source Capacitance
$C_{EX}$	External Capacitance
Cj	Junction Capacitance
Co	Output Capacitor
Copto	Optocoupler Output Capacitance
Cr	Resonant Capacitor
CS <sub>error</sub>	Maximum Relative Current Sharing Error
CS <sub>OUT</sub>	Current Sense Amplifier Output Signal
CTR <sub>MAX</sub>	Maximum Current Transfer Ratio
D	Duty Cycle
D <sub>BOOT</sub>	Bootstrap Diode
Е	Energy Stored in Magnetic Field
E/v	Energy Density
$f_0$	Resonant Frequency
$f_{crossover}$	Crossover Frequency
$\mathbf{f}_{\mathbf{n}}$	Normalized Switching Frequency
$f_{n\_max}$	Maximum Normalized Switching Frequency
$f_{n \ min}$	Minimum Normalized Switching Frequency

$f_p$	Pole Frequency in Degrees
$\mathbf{f}_{r1}$	Resonant Frequency of $C_r$ and $L_r$
$f_{r2}$	Resonant Frequency of $C_r$ and sum of $L_r$ and $L_m$
$\mathbf{f}_{\mathrm{sw}}$	Switching Frequency
$\mathbf{f}_{z}$	Zero Frequency in Degrees
FB	Feedback Signal
$G_0$	Mid-band Gain
$G_1$	Optocoupler Circuit Gain
G <sub>2</sub>	Op-amp Circuit Gain
Н	Magnetic Field Intensity
h <sub>ins_pri</sub>	Thickness of Primary-Side Insulator
$h_{ins\_sec}$	Thickness of Secondary-Side Insulator
h <sub>pri</sub>	Thickness of Primary-side Turn
hsec	Thickness of Secondary-Side Turn
h <sub>space</sub>	Space between Primary-side and Secondary-side Winding
Ι	Current
I <sub>H</sub>	Highest Output Current
If	Diode Forward Current
I <sub>FL</sub>	Full Load Output Current
$I_{f\_avg}$	Diode Average Forward Current
I <sub>f_RMS</sub>	Diode RMS Forward Current
$I_L$	Lowest Output Current
I <sub>leak</sub>	Leakage Inductance Current
I <sub>Lm</sub>	Magnetizing Current
$I_{Lm\_peak}$	Magnetizing Peak Current
Io	Output Current
Ioe	Equivalent Output Current
Ios	Output Current Sense Signal
Iot	Total Output Current
I <sub>pri</sub>	Primary-side Current
Ipri_AC_RMS	Primary-side AC RMS Current

Ipri_peak	Primary-side Peak Current
Ipri_RMS	Primary-side RMS Current
$I_{pri\_mos\_RMS}$	Primary-Side MOSFET RMS Current
Ires	Resonant Tank Current
$I_{sec\_RMS}$	Secondary-side RMS Current
$I_{sec\_winding\_AC\_RMS}$	Secondary-side Winding AC RMS Current
$I_{sec\_winding\_RMS}$	Secondary-side Winding RMS Current
$I_{sec\_winding\_DC}$	Secondary-side Winding DC Current
KI	Proportionality Constant
1	Mean Turn Length
L <sub>leak</sub>	Leakage Inductance
L <sub>m</sub>	Magnetizing Inductance
L <sub>n</sub>	Inductance Ratio between $L_m$ and $L_r$
Lr	Resonant Inductor
n	Transformer Turn Ratio
Ν	Number of Modules
N <sub>pri</sub>	Primary-side Turn Number
N <sub>turn</sub>	Turn Number
$M_{g}$	Voltage Gain
$M_{g\_AC}$	AC Voltage Gain
$M_{g\_FL}$	Voltage Gain at Full Load
$M_{g\_max}$	Maximum Voltage Gain
$M_{g\_min}$	Minimum Voltage Gain
$M_{g\_NL}$	Voltage Gain at No Load
Qe	Quality Factor
Qg	Gate Charge
$Q_{g\_ZVS}$	ZVS Gate Charge
Qrr	Reverse Recovery Charge
$R_{AC\_pri\_winding}$	Primary-side Winding AC Resistance
$R_{AC\_sec\_winding}$	Secondary-side Winding AC Resistance
R <sub>d</sub>	Droop Resistance

$R_{ds\_on}$	On-state Drain-Source Resistance
$R_{DC\_pri\_winding}$	Primary-side Winding DC Resistance
$R_{DC\_sec\_winding}$	Secondary-side Winding DC Resistance
RFORWARD	Forward Resistor
Re	Equivalent Load Resistance
R <sub>1</sub>	Load Resistance
R <sub>l'</sub>	Primary-Referred Equivalent Load Resistance
Ro	Equivalent Series Output Resistance
R <sub>pri</sub>	Primary-side Equivalent Resistance
RPULLUP	Pullup Resistor
$R_{pw}$	Resistance of Primary-side Winding
R <sub>sec</sub>	Secondary-side Equivalent Resistance
R <sub>sw</sub>	Resistance of Secondary-side Winding
R <sub>q</sub>	On-state Drain-Source Resistance of Primary-side Switch
$P_{core\_loss\_300kHz}$	Core Loss at 300kHz
$P_{core\_loss\_500kHz}$	Core Loss at 500kHz
$P_{pri\_copper\_loss}$	Primary-side Winding Copper Loss
$P_{pri\_mos\_cond\_loss}$	Primary-Side MOSFET Conduction Loss
$P_{pri\_mos\_gate\_loss}$	Primary-Side MOSFET Gate Drive Loss
$P_{pri\_mos\_loss}$	Primary-Side MOSFET Power Loss
$P_{pri\_mos\_sw\_loss}$	Primary-Side MOSFET Switching Loss
$P_{sec\_AC\_copper\_loss}$	Secondary-side Winding AC Copper Loss
$P_{sec\_copper\_loss}$	Secondary-side Winding Copper Loss
$P_{sec\_DC\_copper\_loss}$	Secondary-side Winding DC Copper Loss
$P_{sec\_diode\_cond\_loss}$	Secondary-side Diode Conduction Power Loss
$P_{sec\_diode\_loss}$	Secondary-side Diode Power Loss
$P_{sec\_diode\_rev\_loss}$	Secondary-side Diode Reverse Power Loss
$P_{winding\_copper\_loss}$	Winding Copper Loss
R <sub>LED</sub>	Led Resistor
R <sub>PULLDOWN</sub>	Pulldown Resistor
t <sub>dead</sub>	Dead Time

t <sub>rr</sub>	Reverse Recovery Time
V <sub>BIAS1</sub>	Bias Voltage 1
V <sub>BIAS2</sub>	Bias Voltage 2
Vc	Control Voltage
V <sub>CC</sub>	CC Supply Voltage
$V_d$	Droop Voltage
$V_{drop}$	Voltage Drop
$V_{ds}$	Drain-Source Voltage
V <sub>EE</sub>	EE Supply Voltage
$V_{\rm f}$	Diode Forward Voltage Drop
V <sub>FL</sub>	Full Load Output Voltage
$V_{gs}$	Gate-Source Voltage
$V_{gs\_th}$	Gate-Source Threshold Voltage
Vhb	Fundamental Component of V <sub>hb</sub>
$V_{hb}$	Voltage at Half-bridge Node
V <sub>in</sub>	Input Voltage
V <sub>in_nom</sub>	Nominal Input Voltage
V <sub>NL</sub>	No Load Output Voltage
Vo	Output Voltage
$V_{o'}$	Resonant Tank Output Voltage
$V_{of}$	Optocoupler Diode Forward Voltage
V <sub>ol</sub>	Op-amp Output Voltage Low Level
Vos	Output Voltage Sense Signal
V <sub>pt</sub>	Fundamental Component of $V_{\text{pt}}$
V <sub>pt</sub>	Voltage across Primary-side Winding
V <sub>rev</sub>	Diode Reverse Voltage
V <sub>rrm</sub>	Repetitive Peak Reverse Voltage
V <sub>REF</sub>	Reference Voltage
V <sub>Ro</sub>	Voltage Drop on Ro
W	Turn Width
Wp	Pole Frequency in Radians

Wpri	Width of Primary-side Turn
Wsec	Width of Secondary-side Turn
Wz	Zero Frequency in Radians
Х	Node X
Y	Node Y
Ζ	Node Z
$\Delta B$	Magnetic Flux Density Difference
$\Delta I_{o\_max}$	Difference between Highest and Lowest Output Current
$\Delta M_g$	Voltage Gain Difference
$\Delta t$	Time Difference
$\Delta V$	Voltage Difference
$\Delta V_{o(SP)}$	Output Voltage Set Point Accuracy Range
$\Delta \phi$	Magnetic Flux Difference
$\mu_0$	Absolute Permeability

#### **CHAPTER 1**

#### **INTRODUCTION**

#### 1.1. DC Distributed Power Systems

Technological progress in electronic systems continuously demands more improved capabilities from power supplies. Power supplies play a critical role in the overall performance and the reliability of many critical systems such as; computer systems, network systems, telecommunication systems and aerospace & defense systems. High efficiency, high power density, improved reliability and cost-effectiveness are the ever-present design requirements of power supplies. In order to meet these requirements, power supplies mainly leverage the advances in power device technology, passive component technology, packaging technology, cooling technology and control technology [1].

In addition to the technological advances, power supply architecture has undergone significant changes to meet design requirements. For example, instead of single stage centralized power systems, Distributed Power Systems (DPS) are widely adopted in modern power supplies thanks to their modular design [2, 3]. A typical DPS with intermediate bus architecture employs power factor correction (PFC) converter, front-end DC/DC converter and multiple point-of-load converters (PoL) as shown in Fig. 1-1(a). In this system, the PFC converter carries out AC/DC rectification and shapes the input current of the power supply to maximize the real power drawn from the mains. The most popular PFC converter is certainly the Boost PFC converter which has 400VDC output voltage [4, 5]. The front-end DC/DC

voltage distribution bus with step down operation. Generally, the bus voltage level is 12VDC for computer systems, 28VDC for aerospace & defense systems and 48VDC for telecommunication systems. Lastly, PoLs are connected to the low voltage intermediate bus to generate voltage levels required for load subsystems. In order to obtain tight voltage regulation and improved transient/dynamic response, PoLs are usually placed in the close vicinity of the loads.

Building blocks of the DPS architecture can be configured as an array of paralleled standardized converter modules with modular approach as shown in Fig. 1-1(b). Both high voltage and low voltage intermediate busses between these blocks make implementation of module arrays easier. In the literature, configuring a power supply or converter as a module array is usually referred as modular power system or multi-module power system. In such a configuration, several individual modules



(a)



Fig. 1-1. (a) Distributed Power System. (b) DPS with modular approach.

share the load current, thus power processing is distributed among many paralleled units. This means traditional high-power centralized power converter is replaced with a cluster of low power modules. Such a modular power converter offers the following benefits arising from parallel configuration [2]:

- Scalability: Scalability is the ability of a system to handle growing volumes of work or its potential to be enlarged in order to accommodate an increasing number of elements [6]. For a power converter, scalability can be defined as the ability to expand its output power capacity in accordance with changing load requirements. By increasing or decreasing the number of paralleled modules, the output power capacity of a modular power converter can be increased or reduced accordingly, which makes modular power converters scalable systems. After designing standardized off-the-shelf modules, various number of modules can easily be combined to meet new capacity requirements.
- Redundancy & Reliability: A system has redundancy if it contains spare elements that will be employed in case of a failure in the elements that must work to fulfil the required function [7]. Redundancy ensures continuity of operation of a system under fault conditions. Therefore, redundancy implementation increases reliability of the system which can be defined as the probability that it will perform its required function under given conditions for a stated time interval [7]. Redundancy implementation becomes possible in power converters with modular design. A modular power converter can continue to operate in case of failures in the array by the addition of spare or in other words redundant modules. Generally power converters are configured as N+k modules, where N is the minimum number of modules required for the output capacity and k is the number of redundant modules. In such a configuration, power converter can tolerate k failures before it fails. Redundant modules increase the reliability of the power converter significantly. Furthermore, paralleling reduces electrical and thermal stresses on semiconductors and passive components which increases the reliability.

- Thermal Management: Heat generated by semiconductors and passive components must be dissipated in order to carry on continues safe operation of power converters. Also, achieving low working temperatures improves reliability of power converters [8]. In a modular power converter, power processing is distributed among the modules and hence heat sources are distributed. This means possible hot spots are prevented and heat releasing components have larger volume and surface area, which increases conductive and convective heat dissipation. Therefore, the need for expensive liquid or forced air cooling technologies can be eliminated, which simplifies thermal management in modular power converters.
- **Cost-effectiveness:** Centralized power converters are custom-designed products which have long design cycles, resulting in high engineering cost. Also, expensive high power components, protection circuits and cooling equipment increase the cost of these power converters. Designing a modular power converter actually implies designing a standardized module that can be combined in several ways to meet a unique need. When standardized modules are available, design of a modular power converter turns out to be a straightforward task, which reduces the engineering cost. Moreover, being able to use relatively inexpensive low-rating devices and cooling equipment may decrease the bill of materials cost.

As mentioned above, modular power systems have many desirable features. However, in order to benefit from modular configuration, load current sharing among the converter modules should be implemented. Power converters do not share the load current inherently when they are paralleled. Unless forced current sharing is implemented in the converter array, load sharing among the modules is determined by no-load output voltage set point and output resistance of each converter module. Even if standardized modules are used, mismatches still exist due to component tolerances. Because of these mismatches, some of the converter modules may deliver a disproportionate fraction of the load current. A module with higher output voltage will tend to have higher output current up to its current limit setting. Although each module delivers some current, total output current will be shared unequally among the modules. A modular front-end DC/DC converter is shown in Fig. 1-2 to demonstrate inherent current sharing performance of the modules.  $V_{o1}$ ,  $V_{o2}$ ,  $V_{o3}$ ,  $V_{o4}$  and  $R_{o1}$ ,  $R_{o2}$ ,  $R_{o3}$ ,  $R_{o4}$  are no-load output voltage set points and output resistances of the converter modules respectively.  $V_o$  is the output voltage level established by the module array which is also the input voltage of the PoLs on the system. Total output current,  $I_o$ , is delivered by the sum of each module's output current:  $I_{o1}$ ,  $I_{o2}$ ,  $I_{o3}$  and  $I_{o4}$ . It is clear that current proportions delivered by the modules may differ significantly unless forced current sharing control is designed into the array.

In a current-sharing array, the modules deliver almost the same amount of power. Therefore, power derating taken into account during the design of a module can be minimized. Also, modules tend to have similar working temperatures during operation due to the equal distribution of loading. As a result, modules have similar service lives resulting in improved overall reliability. Therefore, in a converter array, individual modules must be designed to deliver load current equally in order to take advantages of parallel operation.



Fig. 1-2. (a) Modular front-end DC/DC converter. (b) Current sharing without forced current sharing control.

#### **1.2.** Modular Front-end DC-DC Converter

Traditional front-end DC/DC converter is a regulated single- or multiple-output converter for providing required power to load subsystems directly as shown in Fig. 1-3 and Fig. 1-4. It includes a transformer to fulfill isolation and voltage step down operation. However, this centralized structure becomes ineffective in terms of efficiency and power density as the output power and/or the number of output voltages is increased. Thus, DPS approach with modular configuration can be applied to improve the overall performance of the converter.

In a DPS structure, power processing functions are distributed among the converter blocks. The front-end DC/DC converter provides an isolated low voltage distribution bus to power the non-isolated PoLs which are employed for voltage generation and regulation. Being single-output makes implementation of modular design easier for the front-end DC/DC converter. In addition, once the PoLs are



Fig. 1-3. (a) Sample single output power supply: MEAN WELL RCP-1000-48 [9]. (b) Block diagram of RCP-1000-48.



Fig. 1-4. (a) Sample multiple output power supply: MEAN WELL IPC-300A [10]. (b) Block diagram of IPC-300A.

assigned to regulation, the front-end DC/DC converter can be designed as a semiregulated or unregulated converter, which allows design optimization to achieve the highest efficiency [11, 12].

Once the front-end DC/DC converter can be configured as an unregulated, singleoutput DC/DC converter, it can be replaced by a "bus converter" or a "DC/DC transformer (DCX)" [13, 14] that is a hard-switching or soft-switching converter which is optimized for a single conversion ratio. PoLs generally accept the input voltage with a margin of  $\pm 10\%$  [11]. Therefore, unregulated bus voltage can be adopted at the input of the PoLs when the required bus voltage range is provided by the front-end DC/DC converter. DCX can be made very efficient with high power density [15, 16]. Moreover, DCX can easily be implemented using modular design. Standardized DCX modules can be combined as an array to take advantages of modular design addressed in Chapter 1.1. By using DCX modules, the front-end DC/DC converter can be designed modularly as shown in Fig 1-5.



Fig. 1-5. Modular front-end DC/DC converter based on DCX modules.

Interleaving technique can also be employed to realize modular design in front-end DC/DC converters [17, 21]. Standardized modules can be combined in various multiphase configurations to implement interleaved structure. Interleaving have the following advantages [20]:

- Output capacity of the converter can be expanded by adding parallel phases.
- Using phase-shedding technique, unneeded phases can be shut down to enhance light load efficiency.
- Output filter capacitor size can be reduced due to the current ripple cancellation achieved by the interleaving technique.

However, there are also a few disadvantages; a multi-module interleaved converter employs a single, centralized controller, an analog IC or a DSP, which is located in one of the modules in the array. This centralized controller, which is presented in Fig. 1-6, generates gate driving signals ( $DS_1-DS_6$ ) distributed through the array. Also, in order to implement load current sharing among the paralleled modules, current amount supplied by each module must be processed in the controller. Generally, current sense signals ( $CS_1-CS_3$ ) are gathered from the modules for this purpose. As a result, wire connection is required between the paralleled modules.

When modular configuration is considered, interleaving technique suffers from reduced reliability due to the centralized controller. Also, the number of control and sense signals changes when the number of modules is increased or decreased. This situation requires rearrangements in the controller of the module array resulting in reduced flexibility in design. In addition, physical implementation of the array is not a trivial task due to the wire connection between the modules. In order to overcome these problems, converter modules have to be configured as "democratic" modules in the modular front-end DC/DC converter. Democratic means each module will operate as a standalone unit in the array independently without any communication or wire connection [22]. Democratic configuration also makes possible the implementation of true N+1 redundant arrays. In the event of a module failure, remaining modules can continue to operate properly as any interconnection is not required.



Fig. 1-6. Modular front-end DC/DC converter based on interleaved modules.

In order to implement a democratic array, current sharing method applied into the array must also be democratic. One of the commonly employed democratic current sharing method is the droop method which is fairly simple and inexpensive to implement [22]. A DCX array with current sharing capability can easily be implemented by using this method. A democratic DCX array not only allows for implementation of redundancy but also high efficiency and high power density can easily be achieved in the modular front-end DC/DC converter design.
#### 1.3. Power Supply Architecture in Phased-array Radar Systems

Modular front-end DC/DC converters are widely adopted in power supplies of military systems, such as, communication, navigation and radar systems. Especially, in radar systems, modular configuration comes into prominence as the total power demand increases. A phased-array radar is an electronically scanned radar which means instead of moving the radar antenna physically, the radio signal beam produced by the radar antenna is steered electronically in order to scan a volume of space. In order to form the beam, an array of several hundred of transmit/receive modules (T/R modules) comprising an antenna is employed by the radar system. An example six-module system is illustrated in Fig. 1-7. As shown in Fig. 1-7, each module in the array transmits with a time/phase delay in order to produce the main beam in the desired pointing direction by using superposition of waves.



Fig. 1-7. Six-module phased-array radar system [23].

When DPS architecture is adopted to power such a radar system, a single nonisolated PoL is employed to feed a small group of T/R modules, typically two to eight, and PoLs are distributed throughout the array [24]. The PoLs can be mounted on the same baseplate as the T/R modules so as to improve both voltage regulation and dynamic step response. Generally, voltage level required by the T/R modules is around 10VDC or less. As a result, the low voltage bus level can be determined as 12VDC. In order to provide the isolated low voltage bus, a modular front-end DC/DC converter based on DCX modules can be employed after the PFC converter. A part of DPS architecture developed for a phased-array radar system is shown in Fig. 1-8.



Fig. 1-8. DPS architecture developed for a phased-array radar system.

#### 1.4. LLC Resonant Converter for DCX Module Design

In this study, an LLC resonant converter, which is shown in Fig. 1-9, is proposed as an unregulated DCX module to build the modular front-end DC/DC converter for the application addressed in Chapter 1.3. A 200W LLC DCX module having 360-400VDC input and 12VDC (12.5VDC-11.75VDC) output is designed. The converter has a half-bridge configuration with center-tapped transformer and also low forward voltage drop diodes are employed as secondary-side rectifiers.

The LLC resonant converter is a multi-resonant converter and frequency modulation is used to control the converter. It utilizes three passive components: resonant inductor  $L_r$ , resonant capacitor  $C_r$  and transformer magnetizing inductance  $L_m$  to fulfill the power conversion with variable frequency control. Since the resonant tank consists of three elements, there exist two resonant frequencies,  $f_{r1}$  and  $f_{r2}$ , in this converter. One is the resonant frequency of  $C_r$  and  $L_r$ , the other one is the resonant frequency of  $C_r$  and sum of  $L_r$  and  $L_m$  [25];

$$f_{r1} = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{1-1}$$

$$f_{r2} = \frac{1}{2\pi\sqrt{(L_r + L_m)C_r}}$$
(1-2)

Generally,  $f_{r1}$  is referred to as the resonant frequency of the LLC resonant converter which is abbreviated as  $f_0$  in the literature. It is clear that  $f_{r1}$  is greater than  $f_{r2}$ .



Fig. 1-9. LLC resonant converter.

A typical voltage gain characteristic of the LLC resonant converter is shown in Fig. 1-10. As seen from Fig. 1-10, with variable frequency control, conversion gain of the converter can be manipulated. Also, voltage gain characteristic of the converter is load-dependent. As load is reduced, peak gain obtained from the resonant tank increases and it moves close to the  $f_{r2}$ . Gain of the resonant tank is equal to unity when switching frequency of the converter  $f_{sw}$  is equal to the resonant frequency  $f_{r1}$ . Unity gain is obtained at the resonant frequency regardless of the load condition of the converter. From the voltage gain characteristic of the converter, it can be seen that the LLC resonant converter can provide a voltage gain both greater than unity and lower than unity. Therefore, it has both boost and buck characteristic.

The LLC resonant converter has three operational modes depending on the switching frequency,  $f_{sw}$ , [26]:

- Operation at resonance, the converter works exactly at  $f_{sw} = f_{r1}$
- Below-resonance operation, the converter works at a frequency  $f_{r2} < f_{sw} < f_{r1}$
- Above-resonance operation, the converter works at a frequency  $f_{sw} > f_{r1}$



Fig. 1-10. Voltage gain characteristic of the LLC resonant converter.

#### 1.4.1. Operation at Resonance

The first mode is the operation at the resonant frequency. The operating point of the LLC resonant converter in this mode is shown in Fig. 1-11. Fig. 1-12 illustrates critical current and voltage waveforms through the converter for this operation mode.

In this mode, the switching period of the converter is exactly equal to the resonant period. The magnetizing inductance never resonates and the voltage gain obtained from the resonant tank is equal to unity. The peak efficiency of the LLC resonant converter is achieved in this mode [11]. Primary-side and secondary-side RMS currents are the lowest. Primary-side switches achieve zero voltage switching (ZVS) and secondary-side switches achieve zero current switching (ZCS).



Fig. 1-11. Operating point of the LLC resonant converter at resonance.



Fig. 1-12. Current and voltage waveforms of the LLC resonant converter at resonance.

#### 1.4.2. Below-resonance Operation

The second mode is the operation at below resonance. The operating region of the LLC resonant converter in this mode and the waveforms through the converter are shown in Fig. 1-13 and Fig. 1-14 respectively.

In this operating mode, the switching period is longer than the resonant period. The magnetizing inductance resonates and the multi-resonant nature of the converter appears. The resonant tank provides a voltage gain higher than unity. Primary-side switches achieve zero voltage switching (ZVS) and secondary-side switches achieve zero current switching (ZCS). As shown in Fig. 1-14, the peak value of the resonant current circulating through the  $L_m$  is larger in this operating mode resulting in higher conduction losses through the converter.



Fig. 1-13. Operating region of the LLC resonant converter at below resonance.



Fig. 1-14. Current and voltage waveforms of the LLC resonant converter at below resonance.

#### 1.4.3. Above-resonance Operation

The third mode is the operation at above resonance. The operating region of the LLC resonant converter in this mode and the waveforms through the converter are shown in Fig. 1-15 and Fig. 1-16 respectively.

In this operating mode, the switching period is shorter than the resonant period. The magnetizing inductance never resonates. The voltage drop across the series  $C_r-L_r$  tank becomes positive at frequencies above the resonant frequency. Therefore, the resonant tank provides a voltage gain lower than unity. Primary-side switches achieve zero voltage switching (ZVS). However, as shown in Fig. 1-16, turn off current of the primary-side switches are higher in this operating mode resulting in higher switching losses in the primary-side switches. In addition, secondary-side switches cannot achieve zero current switching (ZCS) [68].



Fig. 1-15. Operating region of the LLC resonant converter at above resonance.



Fig. 1-16. Current and voltage waveforms of the LLC resonant converter at above resonance.

### 1.5. Literature Review

The LLC resonant converter is an attractive candidate for implementing an unregulated DCX module [27, 28]. Primary-side switches of the LLC resonant converter can achieve zero voltage switching (ZVS) for no load to full load range. The energy required for the ZVS transitions occurring in primary-side switches is provided by the magnetizing inductance of the transformer and does not depend on the load current. In addition, turn off current of the primary-side switches are low. These two characteristics diminish the switching loss of this converter significantly. Moreover, secondary-side rectifiers can achieve zero current switching (ZCS), so

reverse recovery loss associated with these rectifiers are minimal. As a result, the LLC resonant converter can achieve very high efficiency levels while operating at very high switching frequencies such as 1MHz [29, 30]. The switching frequency determines the size of a power converter, the converter size decreases with increasing frequency.

The LLC resonant converter was designed as a DCX in previous literatures [11, 12, 15, 16, 31-33]. LLC DCX operating at the resonant frequency to achieve the highest efficiency is presented in [16]. Similarly, in [31], LLC DCX converter based on GaN devices is designed and constant resonant frequency operation is realized. However, in practical implementation,  $L_r$  and  $C_r$  always have some tolerances. Moreover, component parameters change with aging. As a result, operating at the calculated resonant frequency at all time is not possible [11]. A novel resonant frequency tracking method is proposed in [11] to solve this issue. Previous studies [11, 16, 31] focus on a single LLC DCX converter but array operation and current sharing topics are not addressed.

Previous studies are generally focused on current sharing methods developed for interleaved LLC resonant converter modules. Output plane analysis of some resonant converters was presented in [34] and it is shown that a resonant converter having load dependent regulation characteristic possess current sharing ability. Inherent current sharing ability of the LLC resonant converter was presented in [17]. The negative load characteristic of the LLC resonant converter makes implementation of a current-sharing array possible. Load sharing characteristics of a three phase interleaved LLC resonant converter was addressed in [18]. It is stated that any mismatch between the resonant tank components of the interleaved modules can lead to serious imbalance in current sharing. To solve this problem, star connection of transformer primary windings of three modules is proposed in [18]. A two-phase multi-module LLC resonant converter employing current-controlled inductor to deal with component mismatch issue was presented in [19]. An active approach depending on average current mode control is proposed in [21] for multi-module interleaved LLC resonant converter to solve the same problem. The

proposed current sharing methods in [18-21] are not applicable for the design of a democratic DCX module because of the reasons addressed in Chapter 1.2.

Design of an unregulated LLC DCX module with current sharing capability was presented in [35]. In order to use the droop current sharing method, a notch filter structure with an additional inductor and capacitor is utilized in cascaded with the resonant tank of the converter. Using additional components is not a good practice as it degrades efficiency and power density.

## 1.6. Thesis Outline

This thesis is divided into six chapters and organized as follows:

Chapter 1 introduces the concept of DPS, modularity in front-end DC-DC converters and the power architecture in the phased-array radar systems. It includes a brief overview of the LLC resonant converter topology.

In Chapter 2, the droop current sharing method is investigated for the LLC resonant converter. Droop voltage implementation is described for the proposed LLC DCX converter.

In Chapter 3, a methodical design process is presented for the selection of the resonant tank components of the proposed LLC DCX converter.

In Chapter 4, implementation of the proposed LLC DCX converter is presented. Practical design considerations for implementing a low-profile, high performance LLC DCX converter are provided.

In Chapter 5, experimental results are presented for the 500kHz, 200W LLC DCX module having 360-410VDC input and 12.5-11.75VDC output. Current sharing performance of the proposed module is demonstrated using a two-module array 400W front-end DC/DC converter. In addition, a three-module array which has 2+1 redundancy configuration is implemented to observe current sharing performance of the modular front-end DC/DC converter.

Finally, Chapter 6 is the conclusion chapter and some possible future works are outlined.

### **CHAPTER 2**

#### **DESIGN OF CURRENT SHARING METHOD**

In previous chapter, the importance of load current sharing in a modular power converter was discussed. To implement a current-sharing array, individual modules must be designed to deliver load current equally. Droop current sharing method is employed in the proposed LLC DCX converter for this purpose. In this chapter, firstly, the droop method will be reviewed and designed for the LLC DCX converter. Secondly, some implementation techniques used for this method will be investigated. Lastly, closed-loop control method, which is utilized to implement the droop method will be presented.

## 2.1. Droop Current Sharing Method

In droop current sharing method, current sharing is achieved by load regulation characteristics of the paralleled converters [22]. Fig. 2-1 shows parallel connection of two power converters in order to demonstrate the droop method. As shown in Fig. 2-1, in this method, current sharing among the converters is determined by either the difference between the no-load output voltage set points or the difference between the slopes of the load regulation characteristics of the converters. Due to the mismatches in these parameters, the power converter #1 delivers slightly more load current than the power converter #2. In order to achieve an acceptable current sharing accuracy, i.e. the difference between the current amount delivered by individual modules, load regulation characteristic of the modules must be properly designed.

Paralleled converters shown in Fig. 2-1 have mismatched load regulation characteristics due to the tolerances of the employed components which is unavoidable. The effect of the mismatch in the output voltage set points on current sharing accuracy is illustrated in Fig. 2-2, whereas the effect of the load regulation slope on current sharing accuracy is illustrated in Fig. 2-3. It should be noted that the slopes of the load regulation characteristics are assumed to be the same for the paralleled converters.



Fig. 2-1. (a) Parallel connection of two power converters. (b) Load regulation characteristics of the paralleled converters.



Fig. 2-2. Effect of the mismatch in output voltage set points on current sharing accuracy: (a) Large mismatch. (b) Small mismatch. (c) No mismatch [22].



Fig. 2-3. Effect of the load regulation slope on current sharing accuracy: (a) Large slope. (b) Small slope. (c) Zero slope [22].

As can be seen from Fig. 2-2, the current sharing accuracy improves as the mismatch in the output voltage set point decreases. Paralleled converters share the load current equally when the output voltage set points are matched, as shown in Fig. 2-2(c). As can be seen from Fig. 2-3, the current sharing accuracy in the array can also be improved by increasing the slope of the load regulation characteristics. When power converters with ideal load regulation characteristics are paralleled, load current cannot be shared among the converters, the converter with the highest output voltage delivers the entire load current, as shown in Fig. 2-3(c).

The output voltage set point mismatching is caused by tolerances of the components used in the output voltage feedback loop and it is unavoidable. From the industrial practice, the output voltage set point accuracy is generally  $\pm 1\%$ . For a 12V commercial power converter product, the output voltage set point lies between 11.88V and 12.12V [36] [37]. In order to implement the droop method, pre-selection of the output voltage set point accuracy can be adopted as a design approach. Then, the required load regulation slope can be determined to ensure the specified current sharing accuracy. Achieving a current sharing accuracy of 10% is a good practice [22]. The best possible current sharing accuracy for a predetermined output voltage set point mismatching is achieved when the load regulation slope is maximized, as shown in Fig. 2-3. However, it should be noted that there is a trade-off between the slope and the load regulation range. Output voltage droop increases as the load regulation slope becomes steeper.

The desired load regulation characteristic of the LLC DCX module to implement the droop method is shown in Fig. 2-4.



Fig. 2-4. Load regulation characteristic of the LLC DCX module.

The droop voltage,  $V_d$ , and the droop resistance,  $R_d$ , are defined as;

$$V_d = V_{NL} - V_{FL} \tag{2-1}$$

$$R_d = \frac{V_d}{I_{FL}} \tag{2-2}$$

where  $V_{NL}$  and  $V_{FL}$  are the no load and full load output voltage respectively and  $I_{FL}$  is the full load current.

Load regulation characteristics of N LLC DCX modules connected in parallel as an array are illustrated in Fig. 2-5. The array share the total output current,  $I_{ot}$ . It can be seen that the load regulation characteristics of the modules lie within the defined output voltage set point accuracy range  $\pm \Delta V_{o(SP)}$ . The module with the highest output voltage set point delivers the highest current,  $I_H$ , whereas the one with the lowest output voltage set point delivers the lowest current,  $I_L$ .



Fig. 2-5. Load regulation characteristics of N LLC DCX modules connected in parallel.

From Fig. 2-5, the current sharing accuracy of the paralleled modules is determined by their output voltage set point mismatching. The difference between the highest and the lowest module current is defined as;

$$\Delta I_{o\_max} = \frac{2 * \Delta V o_{(SP)}}{R_d} \tag{2-3}$$

The maximum relative current sharing error can be defined as [22];

$$CS_{error} = \frac{\Delta I_{o\_max}}{I_{ot}/N}$$
(2-4)

I<sub>ot</sub>/N is equal to the full load current of the single module;

$$I_{ot}/N = I_{FL} \tag{2-5}$$

From Eq. (2-3), (2-4) and (2-5), the maximum relative current sharing error can be redefined as [22];

$$CS_{error} = \frac{2 * \Delta V o_{(SP)}}{V_d}$$
(2-6)

For the array of the LLC DCX modules, the current sharing error is specified as 10%. For a good trade-off between the output voltage set point accuracy and the required droop voltage, the output voltage set point accuracy is determined as  $\pm 0.3\%$  for the designed LLC DCX module. From Eq. (2-6), the minimum required droop voltage can be calculated as 0.75V when the output voltage set point is selected as 12.5V for the module.

The output voltage range of the LLC DCX module is positioned such that the output voltage is 12.5V at no load and 11.75V at full load condition to achieve the specified current sharing error. Fig. 2-6 shows the required droop characteristic to implement the droop method.



Fig. 2-6. Required droop characteristic for the LLC DCX module.

The required droop characteristic, in other words, the required droop voltage can be implemented in several ways [35]:

- By using inherent load regulation characteristic of the converter
- By using resonant tank of the converter
- By using voltage feedback loop of the converter

Next, these methods will be investigated for the proposed LLC DCX converter.

# 2.2. Droop Voltage Implementation by using Inherent Load Regulation Characteristic

To achieve the current sharing error of 10%, the required droop voltage of 0.75V may be realized by the equivalent output resistance and secondary-side rectifier of the LLC DCX module. When it is designed as a DCX, the LLC resonant converter is usually open loop designed and operated at the resonant frequency to maximize the conversion efficiency. When such a configuration is selected for the designed LLC DCX module, the voltage gain of the resonant tank,  $M_g$ , turns out to be unity.  $M_g$  is defined as;

$$M_g = \frac{2 * n * V_o'}{V_{in}}$$
(2-7)

where  $V_o'$  is the resonant tank output voltage,  $V_{in}$  is the input voltage and n is the transformer turn ratio.

In such a configuration, the DC equivalent circuit of the LLC resonant converter can be drawn as shown in Fig. 2-7.



Fig. 2-7. DC equivalent circuit of the LLC resonant converter at fixed resonant frequency operation.

The equivalent output resistance,  $R_o$ , depends on the on-state resistances of the primary-side switches,  $R_q$ , the resistances of the transformer primary and secondary windings,  $R_{pw}$  and  $R_{sw}$ . Since the leakage inductance is utilized as the resonant inductance, it has no contribution on the total  $R_o$ . The  $R_o$  causes voltage drop  $V_{Ro}$  at the output of the converter due to the load current. Secondary-side rectifiers similarly cause voltage drop  $V_f$ . The equivalent rectifier is placed separately. The sum of  $V_{Ro}$  and  $V_f$  can be manipulated as the droop voltage to implement the droop method.

Component	Resistance	
Primary-side switch on state resistance, R <sub>q</sub>	240 mΩ	
Primary winding, R <sub>pw</sub>	202.5 mΩ	
Equivalent primary-side resistance, R <sub>pri</sub>	442.5 mΩ	

The primary-side resistances of the designed circuit are shown in Table 2-1.

Table 2-1. Primary-side resistances of the LLC DCX module.

The equivalent primary-side resistance of the circuit must be referred to the secondary side. The relationship for this purpose is defined as [38];

$$R_{sec} = \frac{\pi^2}{8 * n^2} * R_{pri}$$
(2-8)

The secondary-side resistances of the designed circuit are shown in Table 2-2.

Component	Resistance	
Secondary referred primary-side resistance, R <sub>sec</sub>	2.2 mΩ	
Secondary winding, R <sub>sw</sub>	1.3 mΩ	
Equivalent output resistance, R <sub>o</sub>	3.5 mΩ	

Table 2-2. Secondary-side resistances of the LLC DCX module.

The voltage drop caused by the R<sub>o</sub> is defined as;

$$V_{Ro} = I_o * R_o \tag{2-9}$$

In addition, the voltage drop caused by the secondary-side rectifiers can be approximated from the manufacturer's datasheet [57];

$$V_f = 0.18V + 0.016\Omega * I_f \tag{2-10}$$

where I<sub>f</sub> is the average diode current.

If the total voltage drop caused by the  $R_o$  and the secondary-side rectifiers is employed as the droop voltage and also no-load output voltage set point is selected as 12.5V, the droop characteristic of the module can be drawn as shown in Fig. 2-8.



Fig. 2-8. Droop characteristic of the LLC DCX module at fixed resonant frequency operation.

The required droop voltage 0.75V calculated in Chapter 2.1 is not achieved. The maximum current sharing error can be calculated as 39.5% from Eq. (2-6) when the output voltage set point accuracy is determined as the same. This means, in a 400W two-module array, one module will deliver 19.8A, whereas the other will deliver 13.2A. This situation is not acceptable. It is clear that when the LLC resonant converter is operated at the resonant frequency, the droop voltage resulting from the circuit components is not adequate to implement the droop method while meeting the desired current sharing error. The required droop voltage can be realized by adding series resistance to the output of the module. It is simple to implement, however, the series resistance results in excessive power dissipation. As a result, the droop voltage obtained from the inherent load regulation characteristic is not adequate and this method cannot be applied.

## 2.3. Droop Voltage Implementation by using Resonant Tank

The inherent voltage gain characteristic of the LLC resonant converter can also be manipulated to implement the required droop voltage. A typical voltage gain characteristic of the LLC resonant converter having 500kHz resonant frequency is shown in Fig. 2-9. As can be seen from Fig. 2-9, the voltage gain obtained from the resonant tank decreases as the load current increases when the converter works at a fixed switching frequency either in the below or above resonant frequency region. Switching frequencies of 300kHz and 750kHz are marked in Fig. 2-9 in order to demonstrate the inherent gain characteristic of the resonant tank.



Fig. 2-9. Inherent voltage gain characteristic of the LLC resonant converter.

By selecting the operating frequency of the converter, the required droop voltage can be provided without adding any additional resistance to the circuit. The output voltage of the resonant tank is defined as;

$$V_o' = M_g * \frac{V_{in}}{2 * n}$$
(2-11)

As can be seen from Fig. 2-9,  $\Delta M_g$  can be utilized to implement the required droop voltage.  $\Delta M_g$  is the difference between the voltage gain of the resonant tank at no load and full load conditions, which are  $M_{g_NL}$  and  $M_{g_FL}$  in Fig. 2-9. The required droop voltage can be obtained without any additional power loss which makes this approach attractive.

The main drawback of this approach is the operating point of the LLC resonant converter gets far away from the resonant frequency. Therefore, the efficiency of the converter decreases. At below resonant frequency region, primary-side RMS current circulating in the resonant tank increases resulting in increased conduction losses. At above resonant frequency region, turn off current of the primary-side switches increases resulting in increased switching losses.



Fig. 2-10. Droop voltage implementation by using resonant tank.

A sample implementation of this approach is shown in Fig. 2-10. In order to obtain the droop voltage of 0.75V, the LLC DCX is operated at 300kHz, at below resonant frequency region. This approach can also be implemented at above resonant frequency region. The major difference between these regions is the operating frequency of the converter must be increased much away from the resonant frequency at above resonant frequency region in order to obtain the required  $\Delta M_g$ . The voltage gain curves of the resonant tank become less sensitive to the load condition at above resonant frequency region. On the other hand, at below resonant frequency region  $\Delta M_g$  can be obtained more easily with a switching frequency close to the resonant frequency. This situation can be observed in Fig. 2-9.

When voltage gain characteristic of the resonant tank is used to provide the required droop voltage, any mismatch occurring between the resonant tanks of paralleled modules results in current sharing mismatch [18]. It is clear that the obtained droop characteristic is directly dependent on the resonant tank components in this approach. High gain obtained from the resonant tank makes the LLC resonant converter sensitive to the operating frequency. At fixed switching frequency operation, a serious current sharing error may be obtained due to different voltage gain characteristics.

The resonant tank consists of three passive components:  $L_r$ ,  $C_r$  and  $L_m$  which have some tolerances resulting from mass production. The tolerances of the resonant components selected for the LLC DCX module are shown in Table 2-3 [39] [40].

Component	Tolerance	Min.	Тур.	Max.	Unit
Cr	5%	14.2	15	15.8	nF
L <sub>m</sub>	3%	62.1	64	65.9	μH
Lr	3%	6.2	6.4	6.6	μH

Table 2-3. The tolerances of the components selected for the LLC DCX module.

To observe the effect of the resonant tank mismatch on current sharing error, a sample design is conducted and parallel operation of two module, as shown in Fig. 2-11, is simulated in Simplorer software. Resonant tank components are selected from Table 2-3 to simulate possible resonant tank mismatch that can be resulted from the mass production of a module. Schematic of the two-module array built in Simplorer is shown in Fig 2-11.



Fig. 2-11. Two-module array with mismatch in resonant tanks.



Fig. 2-12. Schematic of the two-module array built in Simplorer.



Fig. 2-13. Current sharing performance of the two-module array.

Fixed switching frequency operation at 330kHz is selected to obtain the droop voltage of 0.75V. It should be noted that the transformer turn ratio is arranged as 19:1:1 for the sample design to obtain the desired output voltage range at the output of the array. No load output voltage of the array is set to 12.6V. Simulation result of the full load operation is illustrated in Fig. 2-13. From Fig. 2-13, the output voltage of the array is almost 11.7V. The total output current of the array is 34.2A at full load steady state operation. The output current of the modules are 25A and 9.2A respectively. The current sharing error of the two-module array can be calculated as 46% which is unacceptably large.

In conclusion, inherent voltage gain characteristic of the resonant tank can be used to implement the required droop characteristic. However, the modules may have different droop characteristics due to their non-identical resonant tanks. This situation may lead to large current sharing error. Therefore, this method cannot be employed for the LLC DCX module.

### 2.4. Droop Voltage Implementation by using Voltage Feedback Loop

To solve the component mismatch issue, the droop current sharing method can be implemented actively by using the voltage feedback loop of the converter. For this purpose, an output current sense signal is injected into the voltage feedback loop to modify its characteristic to obtain the required droop voltage. The block diagram of the active droop method is depicted in Fig. 2-14.



Fig. 2-14. The block diagram of the active droop method.

In Fig. 2-14,  $V_{OS}$  and  $I_{OS}$  are the sense signals which are proportional to the output voltage  $V_o$  and the output current  $I_o$  respectively. The sum of these sense signals is compared to reference voltage  $V_{REF}$  at the error amplifier EA. Control loop minimizes the difference between the  $V_{REF}$  and the sum of the sense signals. Therefore, the output voltage decreases as the output current increases. Control voltage  $V_C$  is the output of the EA and it is applied to the voltage-controlled oscillator VCO to determine the switching frequency  $f_{sw}$  of the converter.

In this study, the droop method is implemented by using this approach. The conversion gain of the LLC resonant converter decreases as the switching frequency is increased from the below resonant frequency region to the resonant frequency as shown in Fig. 2-15. The LLC DCX module is designed to operate at the below resonant frequency region at no load and to operate in the close vicinity of the resonant frequency at full load. The output voltage of the module is decreased by increasing the switching frequency as the load current increases. The peak efficiency of the LLC resonant converter is achieved at the resonant frequency. Therefore, maximizing full load efficiency is realized by the control algorithm of the LLC DCX module. An example operating line of the designed module is marked in Fig. 2-15.



Fig. 2-15. Operating line of the LLC DCX module.

As can be seen from the operating line shown in Fig. 2-15, the LLC DCX module operates at different frequencies determined by the load condition. Also, in order to achieve this variable frequency operation, a closed loop control is employed. These are the main differences between the proposed module and open loop, fixed frequency designed DCX converters.

The block diagram of the active droop method employed in the LLC DCX module is shown in Fig. 2-16. Load current is directly sensed from the output of the converter and a proportionality constant,  $K_I$ , is applied to this sense signal. A summer block, an error amplifier EA and a voltage-controlled oscillator VCO are employed to determine the switching frequency  $f_{sw}$ , thus the conversion gain of the LLC DCX converter. The building blocks of the voltage feedback loop is addressed in Chapter 4.5 in detail.



Fig. 2-16. The block diagram of the active droop method employed in the LLC DCX module.

In this chapter, the droop current sharing method has been reviewed and related design parameters have been determined for the proposed LLC DCX module. Some implementation techniques used for the droop method have been investigated. To implement the droop method, voltage feedback loop of the converter is modified and the inherent gain characteristic of the LLC resonant converter is utilized. Compared to the other techniques, this technique does not degrade the efficiency of the module. In addition, this technique is not affected from any resonant tank mismatch between the paralleled modules. Next chapter, resonant tank design of the proposed LLC DCX module will be provided.

### **CHAPTER 3**

## **DESIGN OF LLC DCX MODULE**

The LLC resonant converter consists of three resonant tank components leading to design complexity. In this chapter, a methodical design process will be developed to select the resonant tank components of the proposed LLC DCX module. Voltage transfer function of the topology will be obtained and then circuit parameters will be determined in a systematic way.

#### 3.1. Voltage Transfer Function of the LLC Resonant Converter

To design an LLC resonant converter, voltage transfer function of the topology must be developed. For this purpose, a circuit model of the converter is required. In order to obtain a model, the topology can be divided into three main blocks as shown in Fig. 3-1 [41]:

- Square-wave generator: Primary-side switches generate a unipolar squarewave voltage, V<sub>hb</sub>, across the resonant tank. Switches are driven in a complementary way with %50 duty cycle for this purpose. A dead time is required between the primary-side switches in order to prevent the possibility of shoot-through and to provide a time interval for ZVS to be achieved.
- Resonant tank: Energy circulates in the resonant circuit due to the applied voltage, V<sub>hb</sub>, and some of it is delivered to the load through the transformer. A bipolar square-wave voltage, V<sub>pt</sub>, appears on the primary-side winding of the transformer. This voltage is transferred to the secondary side by the turn ratio, n.

• **Rectifiers:** In order to convert AC input to DC output and supply the load resistance R<sub>1</sub>, rectification is required on the secondary side of the transformer. Diodes or synchronous rectifiers can be employed for this purpose. The output capacitor, C<sub>o</sub>, smooths the rectified voltage and current to provide the output voltage, V<sub>o</sub>.



Fig. 3-1. Building blocks of the LLC resonant converter.

By considering these blocks, the equivalent circuit of the converter can be drawn as shown in Fig. 3-2. In Fig. 3-2,  $R_{I}$ ' is the primary-referred equivalent load resistance,  $I_{res}$  is the resonant tank current,  $I_{Lm}$  is the magnetizing current and  $I_{oe}$  is the equivalent output current. It is difficult to define equations for the converter circuit shown in Fig. 3-2 due to the square waveforms of the voltages. Thus, it is difficult to develop a voltage transfer function.



Fig. 3-2. The equivalent circuit of the converter.



Fig. 3-3. The equivalent circuit of the converter with FHA method.

In order to simplify the equivalent circuit, operating characteristic of the resonant tank can be utilized. The resonant tank has the effect of filtering the higher harmonic components of the applied square wave voltage. Especially when the converter operates in the vicinity of the resonant frequency, almost a sine wave of current circulates in the resonant tank. Owing to this feature, the fundamental harmonic of the square wave can be used as the input voltage in the model while ignoring all higher-order harmonics and then equations can be defined for the equivalent circuit using ac analysis. This method is referred to as First Harmonic Approximation (FHA) method in the literature [38]. It should be noted that the accuracy of the model obtained with this method decreases as the operating point of the converter gets far away from the resonant frequency. When the FHA method is applied, the equivalent circuit of the converter can be redrawn as shown in Fig. 3-3.

In Fig. 3-3,  $v_{hb}$  and  $v_{pt}$  are the fundamental components of  $V_{hb}$  and  $V_{pt}$  respectively. RMS magnitudes of  $v_{hb}$  and  $v_{pt}$  can be defined as;

$$v_{hb} = \frac{\sqrt{2}}{\pi} * V_{in} \tag{3-1}$$

$$v_{pt} = \frac{2\sqrt{2}}{\pi} * n * V_o \tag{3-2}$$

Re is the AC equivalent load resistance which is defined as [38];

$$R_e = \frac{8 * n^2}{\pi^2} * R_l \tag{3-3}$$

From Fig. 3-3, AC voltage gain of the circuit,  $M_{g_AC}$ , can be defined by using the relationship between the fundamentals;

$$M_{g\_AC} = \frac{V_{pt}}{V_{hb}} = \left| \frac{(jwL_m || R_l)}{(jwL_m || R_e) + jwL_r + \frac{1}{jwC_r}} \right|$$
(3-4)

From Eq. (3-1), (3-2) and (3-4), voltage transfer function of the converter can be defined as;

$$V_o = M_{g\_AC} * \frac{V_{in}}{2 * n}$$
(3-5)

where  $V_{in}$  is the input voltage and  $V_o$  is the output voltage. Instead of  $M_{g_AC}$ ,  $M_g$  will be used as the notation for the voltage gain.

As can be seen from Eq. (3-4), each of the resonant tank component, the load condition and the switching frequency determine the voltage gain of the converter. This makes evaluation of the impact of each parameter on the voltage gain difficult and voltage transfer function described in Eq. (3-5) becomes useless. To make it more useful, Eq. (3-4) can be expressed in a normalized format by using the resonant frequency as the base [41]. The normalized frequency  $f_n$  is defined as;

$$f_n = \frac{f_{sw}}{f_0} \tag{3-6}$$

In addition to normalization, two key elements can be defined to convert Eq. (3-4) into simplified format that is easy to utilize for converter design [42] [43] [44];

$$L_n = \frac{L_m}{L_r} \tag{3-7}$$

$$Q_e = \frac{\sqrt{L_r/C_r}}{R_e} \tag{3-8}$$

where  $L_n$  is the inductance ratio between  $L_m$  and  $L_r$ ,  $Q_e$  is the quality factor.

By using Eq. (3-6), (3-7) and (3-8), voltage gain of the circuit can be expressed as;

$$M_g = \left| \frac{L_n * f_n^2}{\left[ (L_n + 1) * f_n^2 - 1 \right] + j \left[ (f_n^2 - 1) * f_n * Q_e * L_n \right]} \right|$$
(3-9)

In addition, voltage transfer function of the converter can be written as;

$$V_o = M_g(f_n, L_n, Q_e) * \frac{V_{in}}{2 * n}$$
(3-10)

In Eq. (3-10),  $L_n$  and  $Q_e$  are dependent on physical circuit parameters and their values determine the gain behavior of the circuit with regard to  $f_n$  or in other words switching frequency  $f_{sw}$ . As stated in Chapter 1.4, variable frequency control is used in the LLC resonant converter. Once  $L_n$  and  $Q_e$  are selected,  $M_g$  can be adjusted by variable switching frequency. Therefore, major consideration is to select proper  $L_n$  and  $Q_e$  values in order to design an LLC resonant converter satisfying gain requirements of the application.

In order to visualize and to understand how  $M_g$  behaves with respect to different  $L_n$  and  $Q_e$  combinations, the curves obtained from Eq. (3-9) are plotted in Fig. 3-4. To see both the effects of  $L_n$  and  $Q_e$ ,  $L_n$  is held constant at each plot, respectively 5, 10, and 15, and  $Q_e$  is varied between 0.1 and 0.5 for each value of  $L_n$ . It should be noted that ZVS boundary is also shown in Fig. 3-4. The LLC resonant converter cannot achieve ZVS everywhere in the operating range. ZVS can be achieved only on the right side of the peak of the gain curves. This boundary is marked with black dashed lines in Fig. 3-4.

From Fig. 3-4, it is clear that change in load or in other words change in  $Q_e$  reshapes the voltage transfer function of the converter for a fixed L<sub>n</sub>. Voltage gain of the circuit decreases as the load increases at the below and above resonant frequency region. At the resonant frequency, gain is always unity and independent from L<sub>n</sub> and  $Q_e$  parameters. All curves pass through this point. In addition, increasing  $Q_e$  shrinks the gain curve for a fixed L<sub>n</sub> and attainable peak gain becomes smaller. On the other hand, decreasing L<sub>n</sub> boosts the gain curve for a fixed Q<sub>e</sub>. M<sub>g</sub> changes more dramatically with respect to f<sub>n</sub> and the peak value of M<sub>g</sub> becomes larger.

It is clear that  $L_n$  and  $Q_e$  can be selected in various combinations to design a converter. Trial and error method may be adopted for this purpose. However, it is time-consuming. Therefore, selection process should be conducted in a systematic way. Next section, selection of  $L_n$  and  $Q_e$  parameters will be discussed.



Fig. 3-4. Plots of  $M_g$  with different  $L_n$  and  $Q_e$  combinations: (a)  $L_n = 5$ , (b)  $L_n = 10$ , (c)  $L_n = 15$ .
#### **3.2.** Selection of L<sub>n</sub> and Q<sub>e</sub> Parameters

Conventionally, LLC resonant converters are designed to have line regulation and load regulation. In order to achieve these regulations, selected  $L_n$  and  $Q_e$  parameters should satisfy gain requirements of the application. A typical operating region of a conventional LLC resonant converter is shown in Fig. 3-5.

In Fig. 3-5,  $f_{n_min}$  and  $f_{n_max}$  are used to define the minimum and maximum boundaries for the operating frequency of the converter respectively.  $M_{g_min}$  and  $M_{g_max}$  shows the minimum and maximum gain levels to achieve line and load regulation. For instance, operating point of the converter will be point B when the input voltage is set to its minimum at full load condition whereas it will be point C when the input voltage is set to its maximum without changing the load. Load condition also changes the operating point of the converter. Operating point will move from point C to point D when the output power of the converter is decreased to no load condition. Generally, the converter is designed to operate at point A, which is the resonant frequency point, at nominal input voltage and full load condition.



Fig. 3-5. A typical operating region of a conventional LLC resonant converter.

In Fig. 3-5, it is clear that the gain curve presenting point B appears to be the converter's actual gain curve at full load condition. Therefore, this point determines the maximum gain requirement of the converter,  $M_{g_max}$ , which is the most critical parameter for the design. Only  $L_n$  and  $Q_e$  combinations satisfying maximum gain requirement can be chosen as a valid design.

In order to evaluate different combinations of  $L_n$  and  $Q_e$ , peak gain curves, which are shown in Fig. 3-6, can be utilized [42]. These curves show the combinations of different  $L_n$  and  $Q_e$  values that can attain same peak voltage gain. After maximum gain requirement of the application is determined, let's assume it is chosen as 2, any combination of  $L_n$  and  $Q_e$  appearing on the gain line 2 can be selected as a valid design. Therefore, these curves can be utilized as data sets for new designs.

These curves can also be redrawn as shown in Fig. 3-7 [41]. In Fig. 3-7, the horizontal axis is  $Q_e$  and the vertical axis is attainable peak gain which is determined by corresponding  $L_n$  value. These curves can also be used in a similar way. As shown in Fig. 3-7, once maximum gain requirement is determined, let's assume it is chosen as 2, it can be plotted into the gain curves to select  $L_n$  and  $Q_e$  for the designed converter.



Fig. 3-6. Relationship between attainable peak gain and L<sub>n</sub>-Q<sub>e</sub> combination [42].



Fig. 3-7. Redrawn attainable peak gain curves.

The LLC DCX converter designed in this study does not have load regulation. In fact, it has a predetermined output regulation characteristic to implement the droop method. Therefore, operating region of the LLC DCX differs from the regulated LLC resonant converter. Importance of point B is described previously. However, the LLC DCX does not operate at such a point. The output voltage of the module decreases as the load increases to implement the droop method which means required gain decreases with increasing load. Therefore, maximum gain requirement of the LLC DCX does not appear at full load condition. Since the gain curves shrinks with increasing load as shown in Fig. 3-5, this situation becomes an advantage for the design of the LLC DCX.

In order to clarify the LLC DCX situation, point B shown in Fig. 3-5 is investigated. At full load and minimum input voltage condition, the regulated LLC resonant converter will operate at point B where the switching frequency is equal to  $f_{n_min}$  and gain is equal to 1.4. As addressed in Chapter 2.3, the maximum gain requirement of the LLC DCX appears at no load and at the minimum input voltage condition, in other words when  $Q_e$  is zero. At this condition, the LLC DCX operates at its minimum switching frequency. When  $f_{n_min}$  is also selected as the minimum switching frequency level for the LLC DCX, it is clear that attainable peak gain turns out to be almost 1.8 from Fig. 3-5. Therefore, maximum gain requirement of the LLC DCX can be satisfied more easily.

It is clear that load regulation characteristic of the LLC DCX affects the selection of  $L_n$  and  $Q_e$ . In order to visualize the effect of the predetermined load regulation characteristic on the selection of  $L_n$  and  $Q_e$ , a simple design methodology is developed. Firstly, the maximum gain requirement of the LLC DCX module will be obtained. Secondly,  $L_n$  will be determined graphically by using the relationship between  $M_{g_max}$  and  $Q_e$ . Finally, instead of  $Q_e$ , characteristic impedance,  $\sqrt{L_r/C_r}$ , parameter will be determined by using circuit analysis to finalize the design.

### 3.3. Maximum Gain Requirement of the LLC DCX Module

The LLC DCX's input voltage range is previously specified as 360V-400VDC. Also, the output voltage of the converter will change between 12.5V and 11.75V with respect to the load condition. Therefore, the module will require different amounts of voltage gain at the output of the resonant tank to operate properly.

Required voltage gain for a specific condition can be determined using Eq. (3-11);

$$M_g = \frac{n * (V_o + V_{drop})}{V_{in}/2}$$
(3-11)

where  $V_o$  is the output voltage of the module and  $V_{drop}$  is the voltage drop in the power stage due to power losses. It should be noted that Eq. (3-11) is a rearranged form of Eq. (3-5).

In order to find minimum and maximum gain requirement of the module, two endpoints of the operation, namely, no load and full load condition should be analyzed. Before calculating  $M_g$ ,  $V_{drop}$  should be calculated for both full load and no load condition. In order to calculate  $V_{drop}$ , the DC equivalent circuit of the converter shown in Fig. 3-8 is utilized.



Fig. 3-8. DC equivalent circuit of the LLC DCX.

In Fig. 3-8,  $R_o$  is the equivalent DC output resistance which is determined as 3.5 m $\Omega$  in Chapter 2.1. The  $R_o$  causes a voltage drop due to the load current. Secondary-side rectifier also causes voltage drop similarly. However, it must be analyzed separately because of its nonlinear operation.

At full load, voltage drop on the Ro, VRo, can be determined as;

$$V_{Ro} = I_o * R_o$$
 (3-12)  
 $V_{Ro} = 17A * 3.5m\Omega = 0.06V$ 

Voltage drop on the equivalent secondary-side rectifier,  $V_f$ , must be investigated in a different manner. In order to determine  $V_f$ , forward voltage drop versus forward current characteristic of the rectifier can be used. FERD20U50 is selected as the rectifier for the LLC DCX module. Forward voltage drop versus forward current characteristic of the FERD20U50 is shown in Fig. 3-9.

At steady state operation, each rectifier conducts half of the output current. As shown in Fig. 3-9, the forward voltage drop can be determined as 0.33V for 125°C junction temperature;

$$V_f = 0.33V$$

Then,  $V_{drop}$  can be calculated using Eq. (3-13);

$$V_{drop} = V_{Ro} + V_f \tag{3-13}$$

$$V_{drop} = 0.06V + 0.33V = 0.39V$$



Fig. 3-9. Forward voltage drop versus forward current characteristic of FERD20U50 device [57].

Then, the output voltage of the resonant tank,  $V_o'$ , can be calculated using Eq. (3-14);

$$V_o' = V_o + V_{drop}$$
 (3-14)  
 $V_o' = 11.75V + 0.39V = 12.14V$ 

Since the converter will operate at its resonant frequency at full load,  $M_g$  is equal to unity. In order to determine the nominal input voltage of the LLC DCX, Eq. (3-11) can be used. When n is selected as 16, nominal input voltage can be calculated as;

$$V_{in\_nom} \cong 385V$$

which is the output voltage set point of the previous stage, namely, the Boost PFC converter. The required gain at full load condition is determined as "1" as it is stated in Chapter 2.4. The converter will operate at the resonant frequency point as it is desired.

In order to calculate the required gain at no load condition, a similar process can be applied. Firstly, at no load condition, the output current is almost zero and hence the voltage drop on  $R_o$  can be taken as;

$$V_{Ro} \cong 0V$$

In order to calculate the voltage drop on the secondary-side rectifiers at no load, Fig. 3-9 can be utilized. As shown in Fig. 3-9, the forward voltage drop can be determined as 0.18V for 25°C junction temperature;

$$V_f = 0.18V$$

Then, the output voltage of the resonant tank can be calculated using Eq. (3-14);

$$V_o' = 12.5V + 0.18V = 12.68V$$

As a result, the required gain at no load and nominal input voltage condition can be calculated as 1.054 by using Eq. (3-11).

Required gain values for the no load and full load condition in case of the minimum and maximum input voltage can be calculated similarly. However, instead of a single operating point, the required gain values can be represented as a curve with regard to the LLC DCX's load regulation characteristic by using Eq. (3-11). In Fig. 3-10, the required gain curves are plotted for the nominal, minimum and maximum input voltage.



Fig. 3-10. Gain requirement of the LLC DCX module for different input voltages.

In Fig. 3-10, the vertical axis is the required voltage gain and the horizontal axis is the output voltage range of the module which is previously determined for the droop method. The gain curve obtained at the minimum input voltage determines the maximum gain requirement of the converter,  $M_{g_max}$ . The LLC DCX must be designed according to this requirement.

Before designing the LLC DCX converter, its switching frequency range should be specified. The resonant frequency of the converter is specified as 500kHz. Since the converter requires gain values greater than 1, minimum switching frequency of the converter is determined as 300kHz. It should be noted that power density of the module decreases as the minimum switching frequency boundary is decreased. From Fig 3-10, it is clear that the module requires gain values lower than 1 when the maximum input voltage is supplied. Therefore, maximum switching frequency of the converter is determined as 600kHz. It should be noted that switching losses of the switches increases as the maximum switching frequency boundary is increased.

#### **3.4.** Design Method Developed for the LLC DCX Module

To design the LLC DCX module, proper  $L_n$  and  $Q_e$  value satisfying the maximum gain requirement is going to be selected. Maximum gain requirement of the converter,  $M_{g_{max}}$ , is directly dependent on the output regulation characteristic of the module as shown in Fig. 3-10. Since the output voltage changes with the load condition,  $M_{g_{max}}$  is also dependent on the load condition, the value of the R<sub>1</sub>. Then, by using Eq. (3-3) and Eq. (3-8), it is simple to derive dependence of  $M_{g_{max}}$  on  $Q_e$ when a value is chosen for the characteristic impedance,  $\sqrt{L_r/C_r}$ , in advance. For different  $\sqrt{L_r/C_r}$  values,  $M_{g_{max}}$  versus  $Q_e$  curves can be obtained for the designed converter as shown in Fig. 3-11.

These obtained curves can be placed inside the peak gain curves as shown in Fig. 3-12 to determine L<sub>n</sub>. Design of the converter can be done easily by selecting L<sub>n</sub> and  $\sqrt{L_r/C_r}$ .



Fig. 3-11. The relationship between M<sub>g max</sub> and Q<sub>e</sub> for different  $\sqrt{L_r/C_r}$  values.



Fig. 3-12. Peak gain curves with  $M_{g_max}$ -Qe curves.

It should be noted that the peak gain curves are rearranged by considering 300kHz minimum switching frequency in Fig 3-12. Since the switching frequency affects the attainable peak gain value, peak gain curves changes when a minimum frequency limit is set. This is the reason why the curves are different from the ones shown in Fig 3-7. As can be seen from Fig. 3-12, the possible largest L<sub>n</sub> value is 15 due to the maximum required gain at no load condition. Large L<sub>n</sub> value makes utilization of the leakage inductance of the transformer as the resonant inductor possible. Otherwise, the resonant inductor must be implemented separately resulting in reduced power density. After L<sub>n</sub> is selected as 15,  $\sqrt{L_r/C_r}$  can be selected. From Fig. 3-12,  $\sqrt{L_r/C_r}$  can be selected as any value below 40. When  $\sqrt{L_r/C_r}$  is larger than 40, the resonant tank cannot satisfy the required gain at full load. In other words, Q<sub>e</sub> cannot be greater than 0.27 when L<sub>n</sub> is selected as 15 for the module.

At this stage, the aim is to select a right  $\sqrt{L_r/C_r}$  value in order to finalize the design. Selected  $\sqrt{L_r/C_r}$  affects three important design criteria. Firstly, the value of the resonant capacitor C<sub>r</sub> becomes determined when a value is assigned to  $\sqrt{L_r/C_r}$ ;

$$C_r = \frac{1}{2\pi * f_0 * \sqrt{L_r/C_r}}$$
(3-15)

Secondly, AC voltage rating of the C<sub>r</sub> is determined by the selected  $\sqrt{L_r/C_r}$  value. RMS voltage of the C<sub>r</sub> can be determined using Eq. (3-16) [45];

$$V_{Cr_{RMS}} = \frac{2 * n * V_{out} + 2 * I_{pri_peak} * \sqrt{L_r/C_r} - V_{in}}{2\sqrt{2}}$$
(3-16)

where  $I_{pri_peak}$  is the primary-side peak current and  $V_{in}$  is the input voltage. It is clear that maximum RMS voltage appears at the full load and minimum input voltage.

Implementation of the  $C_r$  is a critical issue in the design of a high frequency LLC resonant converter.  $C_r$  handles high frequency AC current circulating in the resonant tank. Therefore, before a capacitor is selected as  $C_r$ , its voltage rating has to be derated with regard to the operating frequency. Generally, Metallized Polypropylene film capacitors are selected as the resonant capacitor due to their several characteristics [46]. In Fig. 3-13, voltage derating characteristics of a family of 2000VDC/700VAC rated Metallized Polypropylene film capacitors are shown.



Fig. 3-13. Voltage derating characteristics of EPCOS MKP series [39].

As can be seen from Fig. 3-13, a 15nF capacitor can withstand only up to 80VAC when it is operated at 600kHz switching frequency. Therefore, voltage derating becomes a critical aspect of the design process.

From Eq. (3-16), it seems that smaller  $\sqrt{L_r/C_r}$  will be advantageous when the resonant capacitor's RMS voltage is considered. However, the selected  $\sqrt{L_r/C_r}$  value also has impact on the magnitude of the primary-side current. Once  $\sqrt{L_r/C_r}$  is selected, magnetizing inductance L<sub>m</sub> becomes determined from Eq. (3-17) because of the previously selected parameters, namely, f<sub>0</sub> and L<sub>n</sub>;

$$L_m = \frac{L_n * \sqrt{L_r / C_r}}{2\pi * f_0}$$
(3-17)

 $L_m$  directly determines the primary-side RMS current which affects the efficiency of the converter. Circulating current in the resonant tank decreases as  $L_m$  increases. Primary-side RMS current causes conduction loss on the primary-side switches. By assuming primary-side current has sinusoidal waveform at the full load condition, its magnitude can be derived as;

$$I_{pri_RMS} = \sqrt{\frac{\left(\frac{I_o * \pi}{2 * n}\right)^2 + \left(\frac{V_{in}/2}{2 * L_m * 2 * f_{sw}}\right)^2}{2}}$$
(3-18)

where  $I_0$  is the output current and  $f_{sw}$  is the switching frequency of the converter.

Now, three important design criteria that are affected from the selected  $\sqrt{L_r/C_r}$  value are clarified. In order to carry out the selection of  $\sqrt{L_r/C_r}$  for the designed LLC DCX module, the curves obtained from Eq. (3-15), (3-16) and (3-18) are plotted in Fig. 3-14.



Fig. 3-14. Selection of  $\sqrt{L_r/C_r}$  parameter.

From available commercial products,  $C_r$  is selected as 27nF. Therefore,  $\sqrt{L_r/C_r}$  value corresponds to 11.8 as seen from Fig. 3-14. By using these parameters, circuit parameters can be calculated as shown in Table 3-1.

Circuit Parameter	<b>Calculated Value</b>	
Lr	3.8µH	
L <sub>m</sub>	56μΗ	
Required $A_L$ for $L_m$	219nH/T <sup>2</sup>	

Table 3-1. Circuit parameters resulting from the selected  $\sqrt{L_r/C_r}$  value.

Previously, the turn ratio n is selected as 16. From available commercial products, a core with 250nH/T<sup>2</sup> is selected. Then, circuit parameters are rearranged as shown in Table 3-2. L<sub>n</sub> is selected as 16, whether or not these parameters can provide the required gain values will be verified during bench tests.

Circuit Parameter	Selected Value	
Selected $A_L$ for $L_m$	for $L_m$ 250 nH/T <sup>2</sup>	
L <sub>m</sub>	64µH	
L <sub>n</sub>	16	
Lr	4μΗ	
Cr	27nF	
$\sqrt{L_r/C_r}$	12.1	
$f_0$	485kHz	

Table 3-2. Rearranged circuit parameters.

### 3.5. Required Inductive Energy for ZVS

To achieve ZVS in the primary-side half-bridge switches, sufficient inductive energy is required during the dead time interval to charge or discharge the drainsource capacitances of these switches. During the dead time, magnetizing current,  $I_{Lm}$ , circulates through the drain-source capacitances of the switches and the resonant tank as shown in Fig. 3-15.

With the help of this circulating current, voltage of the half-bridge node,  $V_{hb}$ , is discharged to zero at the end of the dead time before turning on  $Q_2$  whereas  $V_{hb}$  is charged to  $V_{in}$  at the end of the dead time before turning on  $Q_1$ . The equivalent circuit of the converter during the dead time is shown in Fig. 3-16.



Fig. 3-15. Circulating magnetizing current (a) before turning on  $Q_2$ , (b) before turning on  $Q_1$ .



Fig. 3-16. Equivalent circuit of the LLC resonant converter during the dead time In Fig. 3-16,  $I_{Lm_peak}$  is the peak magnetizing current which can be defined as;

$$I_{Lm\_peak} = \frac{V_{in}/2}{2 * L_m * 2 * f_{sw}}$$
(3-19)

In order to achieve ZVS, two drain-source capacitances must be charged or discharged during the dead-time which means Eq. (3-21) must be met;

$$I = C * \frac{\Delta V}{\Delta t} \tag{3-20}$$

$$I_{Lm\_peak} \ge 2 * C_{eq} * \frac{V_{in}}{t_{dead}}$$
(3-21)

where t<sub>dead</sub> is the dead time and C<sub>eq</sub> is the equivalent drain-source capacitance.

From Eq. (3-19) and (3-21), a boundary can be defined for the maximum value of the  $L_m$ ;

$$L_m \le \frac{t_{dead}}{16 * C_{eq} * f_{sw}} \tag{3-22}$$

For the designed LLC DCX module, the dead time is determined as 150nsec and the equivalent output capacitance of the primary-side MOSFET is equal to 135pF [48]. When maximum switching frequency 600kHz is considered,  $L_m$  must be smaller than 115µH to achieve ZVS.  $L_m$  is selected as 64µH previously which ensures soft switching clearly.

In this chapter, a methodical design process has been developed to select the circuit components of the proposed LLC DCX module. Firstly, voltage transfer function of the topology was obtained by using FHA method and the selection of two key design parameters;  $L_n$  and  $Q_e$  was evaluated for the LLC DCX module. Secondly, circuit parameters were determined by using peak gain curves and circuit analysis. Finally, the circuit parameters were analyzed to ensure ZVS operation of the proposed LLC DCX module.

A conference paper was presented at the 8th International Conference on Power Electronics, Machines and Drives (PEMD 2016) covering some of the work presented in Chapter 2 and Chapter 3 [A1]. The paper is given in the Appendix.

Next chapter, implementation of the proposed design will be provided.

#### **CHAPTER 4**

# **IMPLEMENTATION OF LLC DCX MODULE**

LLC DCX module prototype, which is illustrated in Fig. 4-1, is implemented to verify the feasibility of the design presented in Chapter 3. The dimension of the module is 106mm × 61mm × 13mm and it achieves 3.36 W/cm<sup>3</sup> (55.1 W/in<sup>3</sup>) power density. In this chapter, some practical design considerations including transformer implementation, secondary-side rectifier selection, primary-side MOSFET selection and control loop implementation are presented for the proposed LLC DCX module.



Fig. 4-1. Prototype of the proposed LLC DCX module.

# 4.1. Planar Transformer Design

In a power converter, the transformer can be implemented by using either conventional wire-wound structures or planar magnetics. Planar transformers have the following advantages over conventional wire-wound transformers [47]:

- Reduced height (low-profile)
- Greater surface area, resulting in improved heat dissipation capability.
- Winding structure facilitates interleaving
- Less AC winding resistance
- Repeatability of winding structure

In order to benefit from these advantages and to achieve high power density, the transformer of the LLC DCX converter is implemented as a planar transformer. The designed transformer is shown in Fig. 4-2. The windings of the transformer are implemented by using multilayer printed circuit boards (PCB) and a planar E core is utilized. Also, leakage inductance of the planar transformer is used as the resonant inductor,  $L_r$ , of the LLC DCX converter to improve the power density.

The design of a planar transformer requires analysis of both core and copper losses and also design of winding arrangement. Firstly, a core is selected for the transformer. Then, the windings are designed by considering the skin effect, the proximity effect and the interleaving concept.

The worst case for the LLC resonant converter's transformer is the minimum switching frequency condition, which is determined as 300kHz previously for the proposed converter. In this case, magnetic flux density, B, reaches its maximum value which is critical for both core saturation and core loss. In order to estimate the effective cross-sectional area of the core  $A_e$ , Eq. (4-3) can be used;



Fig. 4-2. Transformer of the LLC DCX module.

$$V = N_{turn} * \frac{\Delta \phi}{\Delta t} \tag{4-1}$$

$$\frac{V_{in}}{2} = N_{pri} * \frac{A_e * \Delta B}{\Delta t}$$
(4-2)

$$A_e = \frac{V_{in}/2}{2 * f_{sw} * \Delta B * N_{pri}}$$
(4-3)

where  $\Delta B$  is the maximum flux density swing as shown in Fig. 4-3 and N<sub>pri</sub> is the number of primary turns.

In order to avoid from saturation and to decrease the core loss,  $\Delta B$  is initially chosen as 300mT. With  $V_{in} = 360V$ ,  $f_{sw} = 300$ kHz and  $N_{pri} = 16$ , the required A<sub>e</sub> is calculated as 63mm<sup>2</sup>.

E22/6/16 planar E core having 78mm<sup>2</sup> core area can be selected for this application [65]. However, its window breadth is considerably narrow, 5.9mm, leading to larger DC resistance through the windings. Thus, a larger core is selected.

E32/6/20 planar E core with 3F4 material grade is selected from FERROXCUBE, which is shown in Fig. 4-4 [40]. The transformer consists of two gapped E-shaped parts to achieve the required  $A_L$  value. Its core area is equal to 130mm<sup>2</sup>.



Fig. 4-3. Maximum flux density swing [49].



Fig. 4-4. E32/6/20 planar E core: (a) single E-shaped half (b) dimensions in mm (c) transformer core [40].

From Fig. 4-4, the window breadth is 9.275mm. For E32/6/20 core, the maximum flux density swing can be calculated as 150mT at 300kHz which means the peak flux density is 75mT. As shown in Fig. 4-3, the core has a triangular excitation with 50% duty cycle which means in order to calculate the core loss, manufacturer data for sinusoidal excitation can be utilized [66]. The core loss curves of the selected material is shown in Fig. 4-5.



Fig. 4-5. Core loss curves of 3F4 material [50].

The core loss density of the material is determined as 300kW/m<sup>3</sup> from Fig. 4-5. Then, the core loss at 300kHz can be calculated as;

$$P_{core\_loss\_300kHz} = 1.6W$$

Loss calculation is also done for 500kHz, the resonant frequency, by considering the full load operation at nominal input voltage. Core loss at 500kHz can be calculated as;

$$P_{core\_loss\_500kHz} = 1.1W$$

Transformer design also requires analysis of losses in the windings. At high frequency operation, AC resistance of the windings increases exponentially because of the skin effect and the proximity effect [51] and hence the windings may lead to serious power losses. In order to eliminate these effects, thickness of the copper layers must be considerably less than the skin depth and also primary and secondary windings must be interleaved [47] [52]. For the designed converter, operating frequencies and corresponding skin depths belonging to copper at 100 °C are shown in Table 4-1.

Turn ratio of the transformer is determined as 16:1 and the number of primary turns is selected as 16 previously. Therefore, the secondary winding will be a single turn. To have a center-tap configuration, two single turns in series, namely SW<sub>1</sub> and SW<sub>2</sub>, are implemented in the secondary winding as shown in Fig. 4-6(a). Since the secondary winding handles high output current, these single turns are realized by two paralleled turns to decrease the DC resistance of the winding. Parallel turns are located at two successive layers. In order to implement an interleaved structure, winding structure is arranged as shown in Fig. 4-6(b).

<b>Operating Frequency</b>	Skin Depth	
300kHz	139µm	
500kHz	108µm	
600kHz	99µm	

Table 4-1. Skin depth of copper for different operating frequencies.



Fig. 4-6. (a) Transformer windings. (b) Interleaved winding structure.

It is not possible to implement this interleaved structure in a single PCB due to the manufacturing constraints. Therefore, in order to realize this structure, two different PCBs are manufactured. For the primary winding, a PCB having 8 turns at 8 layers is manufactured which is shown in Fig. 4-7. 8 turns are connected in series with interlayer vias. This PCB is utilized to implement the 8-turn primary winding at each interleaving section. Therefore, two of this kind of PCB are used in the transformer.

For the secondary winding, a PCB having 4 turns at 4 layers is manufactured which is shown in Fig. 4-8. As previously mentioned, turns located at 1<sup>st</sup> and 2<sup>nd</sup> layers are paralleled for the first turn whereas turns located at 3<sup>rd</sup> and 4<sup>th</sup> layers are paralleled for the second turn of the center-tap winding. Thus, the secondary winding is implemented in a single 4-layer PCB. This PCB is also used for implementing the power and control stages of the LLC DCX converter.



Fig. 4-7. 8-turn 8-layer PCB manufactured for the primary winding.



Fig. 4-8. 4-turn 4-layer PCB manufactured for the secondary winding.



Fig. 4-9. Transformer winding: (a) sandwiched PCBs. (b) with planar E core.

With the help of these three PCBs, transformer winding is realized in a sandwiched structure as shown in Fig. 4-9. To connect 8-turn primary winding sections to each other, in other words upper and lower PCBs, a trace is implemented in the middle PCB which already hosts the secondary winding.

The primary winding section is located at eight layers. In order to avoid from high AC resistance, thickness of the copper layers is determined as  $35\mu$ m which is considerably less than the skin depth values shown in Table 5. It is clear that AC resistance of the winding becomes maximum at 600kHz. From Dowell's formula, AC resistance of the winding is equal to 1.02 times of DC resistance at 600kHz [67]. Since the skin depths of 500kHz and 600kHz are almost the same, the ratio can also be used for 500kHz. Primary winding current is equal to the resonant tank current, I<sub>R</sub>. The waveform of the I<sub>R</sub> at the resonant frequency is shown in Fig. 1-12 previously. It has almost a sinusoidal waveform which means the primary winding current has only AC component. Primary RMS current can be determined as 1.6A from Fig. 3-14. The DC resistance of the primary winding is calculated for copper at 100 °C by using the trace width and the mean turn length which are determined

as 5mm and 88mm respectively. As can be seen from Fig. 4-7, there exist interlayer vias on the primary winding leading to increased DC resistance. Due to these vias, 50% margin is put on the DC resistance of the primary winding;

$$R_{DC_pri_winding} = 280 \, m\Omega$$

Then, AC resistance of the winding and primary winding copper loss can be calculated as;

$$R_{AC\_pri\_winding} = 286 \ m\Omega$$

$$P_{pri\_copper\_loss} = I_{pri\_AC\_rms}^{2} * R_{AC\_pri\_winding} = 0.72W$$

Center-tap configuration is used for the secondary winding which puts additional layer within the winding structure. When one side of the center-tap conducts, the other side acts as a passive layer in the high field region. It will have equal and opposite currents flowing on its two surfaces leading to significant loss [47]. In order to avoid from high AC resistance, thickness of the copper layers should be kept smaller than the skin depth. Thickness of the copper layer is determined as 35µm to decrease the AC resistance of the 1-turn secondary winding. Each section consists of a single layer secondary winding. From Dowell's formula, AC resistance of the winding is equal to 1.01 times of DC resistance at 500kHz [67]. Trace width of the secondary winding is determined as 8mm and the mean turn length is taken as 88mm. As can be seen from Fig. 4-8, there exist interlayer vias on the secondary winding leading to increased DC resistance. Due to these vias, 50% margin is put on the DC resistance of the secondary winding. For copper at 100 °C, DC and AC resistance of the each secondary winding can be calculated as;

 $R_{DC\_sec\_winding} = 5.4 \ m\Omega$ 

 $R_{AC\_sec\_winding} = 5.45 m\Omega$ 

To calculate the current flowing on each winding, the total secondary-side RMS current can be calculated as;

$$I_{sec\_RMS} = \frac{\pi}{2\sqrt{2}} * I_o = 18.9A$$

The RMS current of each winding can be calculated as;

$$I_{sec\_winding\_RMS} = \frac{\sqrt{2} * I_{sec\_RMS}}{2} = 13.36A$$

The DC current of each winding can be calculated as;

$$I_{sec\_winding\_DC} = \frac{\sqrt{2} * I_{sec\_RMS}}{\pi} = 8.5A$$

The AC RMS current of each winding can be calculated as;

$$I_{sec\_winding\_AC\_RMS} = \sqrt{I_{sec\_winding\_RMS}^{2} - I_{sec\_winding\_DC}^{2}} = 10.3A$$

Then, secondary-side winding copper loss can be calculated as;

$$P_{sec\_DC\_copper\_loss} = 2 * I_{sec\_winding\_DC}^{2} * R_{DC\_sec\_winding} = 0.78W$$

$$P_{sec\_AC\_copper\_loss} = 2 * I_{sec\_winding\_AC\_rms}^{2} * R_{AC\_sec\_winding} = 1.13W$$

$$P_{sec\_copper\_loss} = P_{sec\_DC\_copper\_loss} + P_{sec\_AC\_copper\_loss}$$
(4-4)
$$P_{sec\_copper\_loss} = 1.91W$$

The total winding copper loss of the transformer can be calculated as;

$$P_{winding\_copper\_loss} = P_{pri\_copper\_loss} + P_{sec\_copper\_loss}$$
(4-5)

 $P_{winding\_copper\_loss} = 2.63W$ 

Fig. 4-10 shows a breakdown of theoretical power losses of the module at the full load of nominal input voltage condition.



Total Power Loss = 3.73W

Fig. 4-10. Loss breakdown of the planar transformer.

#### 4.1.1. Leakage Inductance of the Planar Transformer

Some flux generated by the primary winding do not link with the secondary winding and leaks from the magnetic core. These flux lines complete their paths through the air, winding layers and insulator layers. The energy stored in this magnetic field appears as series leakage inductance,  $L_{leak}$ , in the equivalent electrical circuit. Leakage inductance of the planar transformer is used as the resonant inductor of the proposed LLC DCX converter to improve the power density. Therefore, the magnitude of the leakage inductance becomes a critical aspect of the design process.

The magnitude of the leakage inductance can be calculated by analyzing magneto motive force (MMF) and energy distribution through the planar transformer [53] [54]. MMF distribution through the planar transformer is shown in Fig. 4-11.

In Fig. 4-11,  $h_{pri}$  is the thickness of primary-side turn,  $h_{ins\_pri}$  is the thickness of primary-side insulator,  $h_{sec}$  is the thickness of secondary-side turn,  $h_{ins\_sec}$  is the thickness of secondary-side insulator,  $h_{space}$  is the space between primary and secondary windings arising from kapton tape and PCB coating,  $w_{pri}$  is the width of each primary-side turn and  $w_{sec}$  is the width of each secondary-side turn. It should be noted that the center-tap turn SW<sub>2</sub> does not conduct in Fig. 4-11, it acts as a passive layer.



Fig. 4-11. MMF distribution through the planar transformer.

Since permeability can be taken constant through the winding and insulator layers, the energy density associated with the leakage field can be defined as;

$$E/_{v} = \frac{1}{2} * B * H$$
 (Joules/m<sup>3</sup>) (4-6)

$$E/_{v} = \frac{1}{2} * \mu_{0} * H^{2}$$
 (Joules/m<sup>3</sup>) (4-7)

The stored energy in any portion of the layers can be defined as;

$$E = \int \frac{1}{2} * \mu_0 * H^2 \, dv \tag{4-8}$$

The differential volume can be defined as  $l \times w \times dy$  for the planar transformer from Fig. 4-11. 1 is the mean turn length and w is the turn width. The total energy associated with the leakage inductance can defined as the sum of the energy stored in each elementary layer;

$$E = \frac{1}{2} * \mu_0 * \sum \int_0^y H^2 * l * w \, dy \tag{4-9}$$

The field intensity, H, depends on the total ampere-turns linked by the leakage flux path. By assuming the stored energy is entirely contained in the core window, the flux path can be taken equal to the turn width, w. If windings are spaced uniformly, H can be taken constant throughout the layers. Therefore, for the first primary winding layer, H can be expressed by;

$$H = \frac{I_{pri} * y}{w_{pri} * h_{pri}} \tag{4-10}$$

Similarly, H can be expressed by Eq. (4-11) for the first insulator layer;

$$H = \frac{I_{pri}}{w_{pri}} \tag{4-11}$$

For other layers, H can be expressed similarly. Then, the total energy can be written using Eq. (4-9);

$$E = \frac{1}{2} * \mu_{0} * \left[ \frac{16 * \int_{0}^{h_{pri}} \left(\frac{I_{pri} * y}{w_{pri} * h_{pri}}\right)^{2} * l * w_{pri} dy \\ + 2 * \int_{0}^{h_{sec}} \left(\frac{8 * I_{pri} * y}{w_{sec} * h_{sec}}\right)^{2} * l * w_{sec} dy \\ + \left(\frac{I_{pri}}{w_{pri}}\right)^{2} * \left(2 * h_{pri} + 2 * h_{ins\_pri}\right) * l * w_{pri} \\ + \left(\frac{2 * I_{pri}}{w_{pri}}\right)^{2} * \left(2 * h_{pri} + 2 * h_{ins\_pri}\right) * l * w_{pri} \\ + \left(\frac{3 * I_{pri}}{w_{pri}}\right)^{2} * \left(2 * h_{pri} + 2 * h_{ins\_pri}\right) * l * w_{pri} \\ + \left(\frac{5 * I_{pri}}{w_{pri}}\right)^{2} * \left(2 * h_{pri} + 2 * h_{ins\_pri}\right) * l * w_{pri} \\ + \left(\frac{5 * I_{pri}}{w_{pri}}\right)^{2} * \left(2 * h_{pri} + 2 * h_{ins\_pri}\right) * l * w_{pri} \\ + \left(\frac{6 * I_{pri}}{w_{pri}}\right)^{2} * \left(2 * h_{pri} + 2 * h_{ins\_pri}\right) * l * w_{pri} \\ + \left(\frac{6 * I_{pri}}{w_{pri}}\right)^{2} * \left(2 * h_{pri} + 2 * h_{ins\_pri}\right) * l * w_{pri} \\ + \left(\frac{6 * I_{pri}}{w_{pri}}\right)^{2} * \left(2 * h_{pri} + 2 * h_{ins\_pri}\right) * l * w_{pri} \\ + \left(\frac{6 * I_{pri}}{w_{pri}}\right)^{2} * \left(2 * h_{pri} + 2 * h_{ins\_pri}\right) * l * w_{pri} \\ + \left(\frac{8 * I_{pri}}{w_{pri}}\right)^{2} * \left(2 * h_{pri} + 2 * h_{ins\_pri}\right) * l * w_{pri} \\ + \left(\frac{8 * I_{pri}}{w_{pri}}\right)^{2} * \left(2 * h_{pri} + 2 * h_{ins\_pri}\right) * l * w_{pri} \\ + \left(\frac{8 * I_{pri}}{w_{pri}}\right)^{2} * \left(2 * h_{pri} + 2 * h_{ins\_pri}\right) * l * w_{pri} \\ + \left(\frac{8 * I_{pri}}{w_{pri}}\right)^{2} * \left(2 * h_{ins\_pri} + 2 * h_{ins\_pri}\right) * l * w_{pri} \\ + \left(\frac{8 * I_{pri}}{w_{pri}}\right)^{2} * \left(2 * h_{ins\_pri} + 2 * h_{ins\_pri}\right) * l * w_{pri} \\ + \left(\frac{8 * I_{pri}}{w_{pri}}\right)^{2} * \left(2 * h_{ins\_pri} + 2 * h_{ins\_pri}\right) * l * w_{pri} \\ + \left(\frac{8 * I_{pri}}{w_{pri}}\right)^{2} * \left(2 * h_{ins\_pri} + 2 * h_{ins\_pri}\right) * l * w_{pri} \\ + \left(\frac{8 * I_{pri}}{w_{pri}}\right)^{2} * \left(2 * h_{ins\_pri} + 2 * h_{ins\_pri}\right) * l * w_{pri} \\ + \left(\frac{8 * I_{pri}}{w_{pri}}\right)^{2} * \left(2 * h_{ins\_pri} + 2 * h_{ins\_pri}\right) * l * w_{pri} \\ + \left(\frac{8 * I_{pri}}{w_{pri}}\right)^{2} * \left(2 * h_{ins\_pri} + 2 * h_{ins\_pri}\right) * l * w_{pri} \\ + \left(\frac{8 * I_{pri}}{w_{pri}}\right)^{2} * \left(2 * h_{pri} + 2 * h_{ins\_pri}\right) * l * w_{pri} \\ + \left(\frac{8 * I_{pri}}{w_{pri}}\right)^{2} * \left(2 * h_{pri} + 2 * h_{ins\_pri}\right) * l * w_{pri} \\ + \left(\frac{8 * I_{pri}}$$

Primary referred leakage inductance can be obtained from the associated stored energy;

$$E = \frac{1}{2} * L_{leak} * I_{pri}^{2}$$
(4-13)

The proposed planar transformer has been built with:  $h_{pri} = 35 \ \mu m$ ,  $h_{ins\_pri} = 220 \ \mu m$ ,  $h_{sec} = 35 \ \mu m$ ,  $h_{ins\_sec} = 300 \ \mu m$ ,  $h_{space} = 250 \ \mu m$ ,  $w_{pri} = 5 \ mm$ ,  $w_{sec} = 8 \ mm$ . Using Eq. (4-12) and Eq. (4-13), the leakage inductance can be calculated as 3.53  $\ \mu H$ . It is measured as 3.87 $\mu$ H with an RLC meter. Measurement is done from the primary-side winding of the transformer while secondary-side windings are shorted. To achieve better matching, finite element analysis (FEA) can be used. It is clear that the magnitude of the leakage inductance can be changed by adjusting the physical parameters of the planar transformer: copper thickness and width, insulator

thickness between layers, the space between primary and secondary winding, number of turns and interleaving arrangement.

## 4.2. Secondary-side Rectifiers

It is difficult to implement synchronous rectification (SR) in the LLC resonant converter. Unlike PWM converters, driving signals of the primary-side switches cannot be applied to the secondary-side switches directly for the LLC resonant converter. Generally, specific IC controllers are employed to generate the driving signals of the SR MOSFETs. This makes SR implementation both complex and expensive. For the designed LLC DCX, Field-Effect Rectifier Diode (FERD) technology is selected for the secondary-side rectifiers to achieve a rectification performance close to that of SR MOSFETs. FERD is an attractive technology for applications where SR with MOSFETs is complex and the efficiency of the Schottky diode is limited. FERD devices have low conduction losses thanks to their low forward voltage drop and low reverse leakage current. In addition, they have the ability of fast recovery and high frequency operation without large electromagnetic interference [55].

FERD technology uses aspects of MOSFET structure to provide a good combination of performance of conventional Schottky technology and reliability of PN-junction technology. Fig. 4-12 shows a typical structure and equivalent schematic representation of an FERD device [56].



Fig. 4-12. (a) A typical structure of an FERD device [56]. (b) Schematic representation of an FERD device [55].

As shown in Fig. 4-12, an FERD device can be represented as a MOSFET in which the gate node is shorted to the source node. Polarity of the FERD is the same with the intrinsic body diode but structural parameters are rearranged to have a high performance diode. Basically, gate oxide thickness, channel length, distance between channels and doping concentrations of layers are modified for this purpose.

FERD20U50 from ST Microelectronics is selected as the secondary-side rectifier which is shown in Fig. 4-13 [57]. It has a low-profile, small footprint package: 5mm  $\times$  6mm  $\times$  1mm.

The key parameters of the FERD20U50 are shown in Table 4-3. In addition, two commercial Schottky diodes with similar ratings and packages are also shown in Table 4-3 to obtain a direct comparison between FERD and Schottky technologies. Since the forward voltage drop,  $V_f$ , and the reverse leakage current,  $I_{leak}$ , are the major performance characteristics of a rectifier,  $V_f^*I_{leak}$  is used as a figure of merit (FOM) in Table 4-2.



Fig. 4-13. Secondary-side rectifier: FERD20U50 (a) top side (b) bottom side.

Parameter	FERD20U50 ST Microelectronics	MBR2045EMFS On Semiconductor	V20PL50-M3 VISHAY
Repetitive Peak			
Reverse Voltage	50V	45V	50V
V <sub>rrm</sub>			
Forward Voltage			
Drop	0.45V	0.51V	0.51V
$I_{f}=20A, T_{J}=25^{\circ}C$		0.31 V	0.31 V
$V_{\rm f}$			
Reverse Leakage			
Current			
V <sub>r</sub> =V <sub>rrm</sub> ,	60mA	100mA	60mA
T_=125°C			
I <sub>leak</sub>			
Junction			
Capacitance	200mE	400mE	450mE
$V_r = V_{rrm}, T_J = 25^{\circ}C$	300pr	400pr	430pr
CJ			
$FOM = V_f * I_{leak}$	27mV*A	51mV*A	30.6mV*A

Table 4-2. Comparison of FERD20U50 and two Schottky diodes.

As can be seen from Table 4-2, the FERD20U50 shows performance improvement when the FOM is considered which is better by a factor of 1.89 and 1.13 compared to MBR2045EMFS and V20PL50-M3 respectively.

From Table 4-2, the FERD20U50 has low junction capacitance similar to Schottky diodes and hence it has almost zero reverse recovery charge,  $Q_{rr}$ . It can be operated at high frequency without reverse recovery loss. For the LLC DCX,  $Q_{rr}$  becomes critical only when it is operated at the above resonant frequency region. In this region, the secondary-side diodes are not turned off under ZCS condition and reverse recovery loss may occur. The LLC DCX is designed to operate mainly at the below resonant frequency region and at the resonant frequency as stated in Chapter 2.4. Therefore, having zero  $Q_{rr}$  is not a significant advantage for the rectifier performance.

#### 4.2.1. Loss calculation for secondary-side rectifiers

Power losses of a fast recovery diode can be divided into two parts:

- Conduction loss due to the forward voltage drop
- Reverse loss due to the reverse leakage current

To calculate the total power loss of each secondary-side, these components should be calculated separately. Eq. (4-14) can be used to calculate the total power loss;

$$P_{\text{sec\_diode\_loss}} = D * (V_f * I_{f\_avg} + R_{on} * I_{f\_RMS}^2) + (1 - D) * V_{rev} * I_{leak}$$
(4-14)

where D is the duty cycle of the rectifier,  $V_f$  is the forward voltage drop resulting from the average forward current  $I_{f_avg}$ ,  $R_{on}$  is the on-state resistance of the rectifier,  $I_{f_RMS}$  is the RMS value of the forward current,  $V_{rev}$  is the reverse voltage across the rectifier during off-state and  $I_{leak}$  is the reverse leakage current.

The designed LLC DCX will generally operate at the nominal input voltage and full load condition since it is cascaded with a regulated Boost PFC converter. Therefore, the power losses are calculated for this operating condition. For this operating condition, current waveform seen on each diode is shown in Fig. 4-14.



Fig. 4-14. Current waveform of each secondary-side rectifier.

As can be seen from Fig. 4-14, forward current of the rectifier changes almost sinusoidally which means the forward voltage drop also changes in time. Since it is difficult to determine the equivalent value of the forward voltage drop, average forward power dissipation versus average forward current curves of the FERD20U50, which are shown in Fig. 4-15, are utilized to determine the conduction losses. The curves are given in the manufacturer datasheet. In Fig. 4-15, the horizontal axis is the average forward current and the vertical axis is power dissipation.  $\delta$  represents the duty cycle of the diode in which it conducts the average forward current.

From Fig. 4-15, the average value of the forward current is almost equal to 8.5A and the duty cycle is equal to 0.5. Then, the power dissipation resulting from the forward voltage drop can determined as;

 $P_{\text{sec diode cond loss}} = 3.8W$ 



Fig. 4-15. Average forward power dissipation versus average forward current curves for FERD20U50 [57].



Fig. 4-16. Reverse leakage current versus applied reverse voltage for FERD20U50 [57].

To calculate the power loss during off state, reverse leakage current of the diode must be determined. Fig. 4-16 shows typical reverse leakage current values of the FERD20U50 with regard to applied reverse voltage. In center-tap configuration, the diodes see a reverse voltage that is two times of the output voltage. The maximum output voltage of the LLC DCX is specified as 12.5V previously. Then, the value of the reverse leakage current can be determined as 16mA for 125°C junction temperature. As a result, the reverse loss of the each diode can be calculated as;

$$P_{sec\_diode\_rev\_loss} = (1 - D) * V_{rev} * I_{leak}$$

$$P_{sec\_diode\_rev\_loss} = 0.5 * 25V * 16mA$$

$$P_{sec\_diode\_rev\_loss} = 0.2W$$

$$(4-15)$$

For the LLC DCX, the total power loss of the secondary-side rectifier can be calculated as;

$$P_{\text{sec\_diode\_loss}} = P_{\text{sec\_diode\_cond\_loss}} + P_{\text{sec\_diode\_rev\_loss}}$$
(4-16)

$$P_{sec\_diode\_loss} = 4W$$
Fig. 4-17 shows a breakdown of power losses of the secondary-side rectifier at the full load of nominal input voltage condition.



Fig. 4-17. Loss breakdown of the secondary-side rectifier.

# 4.3. Primary-side MOSFETs

Selecting a suitable primary-side MOSFET is not only important for improving the efficiency of an LLC resonant converter, but also it plays a critical role in the overall reliability [28]. For the selection of the primary-side MOSFET, the LLC resonant converter has three main considerations [58]:

- Achieving ZVS operation
- Reducing gate drive losses
- Avoiding from incomplete reverse recovery of the body diode

As addressed in Chapter 3.4, achieving ZVS operation is dependent on the magnetizing current  $I_{Lm}$ , the equivalent drain-source capacitance of the primary-side MOSFET  $C_{eq}$ , the dead time  $t_{dead}$  and the switching frequency  $f_{sw}$ . In order to maintain ZVS operation, the resonant tank should have sufficient inductive energy for the entire operating conditions. In addition, the gate driver signals should have sufficient dead time to allow inductive energy to charge/discharge the  $C_{eq}$  of the MOSFETs. By selecting a MOSFET with lower  $C_{eq}$ , ZVS can be achieved more easily under the same amount of inductive energy. Therefore, the dead time can be reduced. Smaller dead time results in reduced conduction losses due to the lower RMS values of currents through the converter. Therefore, the efficiency of the converter can be improved.

Selecting a power MOSFET with smaller ZVS total gate charge  $Q_{g_ZVS}$  as a primaryside switch improves the efficiency of the LLC resonant converter. With lower  $Q_{g_ZVS}$ , gate drive losses can be reduced. Also, lower  $Q_{g_ZVS}$  provides faster switching times and hence turn-off switching losses can be diminished.

Reverse recovery characteristics of the intrinsic body diode is also critical in the selection of the primary-side MOSFET. The body diode of the each primary-side MOSFET conducts during dead time intervals because of the current circulating in the resonant tank. Fig. 4-18 illustrates the time intervals (1, 2, 3, 4) in which low side MOSFET Q<sub>2</sub> or its body diode  $D_{Q2}$  conducts.

In time interval 1, the  $C_{eq}$  of  $Q_2$  is discharged completely and  $D_{Q2}$  starts to conduct the resonant tank current. In 2,  $D_{Q2}$  is forward biased by the resonant tank current. In 3,  $Q_2$  is turned on by the gate signal and the current flows through  $Q_2$  from source to drain due to its low on state resistance. In 4, the current changes its polarity and it flows through  $Q_2$  from drain to source. At the end of 4,  $Q_2$  is turned-off and the current charges the  $C_{eq}$  of  $Q_2$  to input voltage level.



Fig. 4-18. Current and voltage waveforms of low side MOSFET, Q2.

It is clear that  $D_{Q2}$  should be reverse biased sufficiently during the time interval 4 in order to avoid from stresses related to reverse recovery. Especially at light load and high switching frequencies, both magnitude and duration of the reverse bias across  $D_{Q2}$  decreases. If  $D_{Q2}$  is not recovered completely when  $Q_1$  is turned on,  $Q_2$  cannot block the reverse voltage immediately. A reverse recovery current with high di/dt flows through the device. If the reverse recovery current is large enough, the voltage induced across the channel of the MOSFET can turn on the intrinsic bipolar transistor [28]. This situation leads to the failure of the device due to the large current that will flow after the intrinsic bipolar transistor is turned on. In order to avoid from this issue, super-junction MOSFETs can be employed as primary-side switches. Vertical structure of these MOSFETs inherently prevents this type of failure [28].

For the LLC DCX, STL33N60M2 from ST Microelectronics is selected as the primary-side MOSFET [48]. The key parameters of the STL33N60M2 are shown in Table 4-3.

Parameter	STL33N60M2
Maximum Drain-Source Voltage V <sub>ds</sub>	600V
Maximum Gate-Source Voltage V <sub>gs</sub>	±25V
Gate-Source Threshold Voltage $V_{gs\_th}$	$2V\!<\!V_{gs\_th}\!<\!4V$
Typical Drain-Source Resistance R <sub>ds_on</sub>	115mΩ
Total Gate Charge Q <sub>g</sub>	45.5nC
Gate Charge ZVS Operation Q <sub>g_ZVS</sub>	27nC
Reverse Recovery Time t <sub>rr</sub>	375nsec
Reverse Recovery Charge Q <sub>rr</sub>	5.6µC

Table 4-3. The key parameters of the primary-side MOSFET: STL33N60M2.

### 4.3.1. Loss calculation for primary-side MOSFETs

The total power loss of a primary-side MOSFET can be divided into three parts: conduction loss, switching loss and gate drive loss. The conduction loss of each MOSFET can be calculated using Eq. (4-17) and (4-18);

$$P_{pri\_mos\_cond\_loss} = I_{pri\_mos\_RMS}^{2} * R_{ds\_on}$$
(4-17)

$$I_{pri\_mos\_RMS} = \frac{I_{pri\_peak}}{2}$$
(4-18)

where  $I_{pri\_mos\_RMS}$  is the primary-side MOSFET RMS current which can be estimated as half of primary-side peak current  $I_{pri\_peak}$  and  $R_{ds\_on}$  is the drain-source resistance. The STL33N60M2 has 240m $\Omega$  drain-source resistance when junction temperature is 125°C. Primary-side peak current is calculated as 2.26A. Then, the conduction loss can be calculated as;

$$P_{pri\_mos\_cond\_loss} = 0.3W$$

The LLC resonant converter achieves ZVS switching. Therefore, the turn-on loss of the primary-side MOSFETs is negligible. The turn-off loss can be estimated using Eq. (4-19) [45];

$$P_{pri\_mos\_sw\_loss} = \frac{C_{eq} * V_{in}^2 * f_{sw}}{12}$$

$$P_{pri\_mos\_sw\_loss} = 0.83W$$
(4-19)

The gate drive loss becomes critical at high switching frequencies. The gate drive loss of each MOSFET can be calculated using Eq. (4-20);

$$P_{pri\_mos\_gate\_loss} = Q_{g\_ZVS} * V_{gs} * f_{sw}$$

$$P_{pri\_mos\_gate\_loss} = 0.2W$$
(4-20)

where  $V_{gs}$  is the gate drive voltage which is selected as 15V for the LLC DCX converter.

$$P_{pri\_mos\_loss} = P_{pri\_mos\_cond\_loss} + P_{pri\_mos\_sw\_loss} + P_{pri\_mos\_gate\_loss}$$
(4-21)

$$P_{pri\_mos\_loss} = 1.33W$$

Fig. 4-19 shows a breakdown of power losses of the primary-side MOSFET at the full load of nominal input voltage condition.



Fig. 4-19. Loss breakdown of the primary-side MOSFET.

Fig. 4-20 shows a breakdown of theoretical power losses of the module at the full load of nominal input voltage condition. The total power loss is calculated as 14.84W and the estimated efficiency of the module is 93%.



Fig. 4-20. Loss breakdown of the proposed module.

# 4.4. Building Blocks of the LLC DCX Converter

The circuit of the proposed LLC DCX converter consists of five major building blocks: power stage, output current sense stage, voltage feedback loop stage, control stage and gate drive stage as shown in Fig. 4-21.



Fig. 4-21. Building blocks of the LLC DCX converter.

The circuit components of the power stage are shown in Fig. 4-22 in detail. Selection of the resonant tank components was addressed in Chapter 3 in detail. The output capacitor of the converter is determined as 3.96mF to have a 100mV peak-to-peak ripple voltage at the output. Tantalum electrolytic capacitors are employed as they have low ESR.



Fig. 4-22. Power stage of the LLC DCX converter.

As stated in Chapter 2.4, the output current sense signal is injected into the voltage feedback loop to implement the droop method. To obtain the output current sense signal, a high-side current sense amplifier IC is utilized as shown in Fig. 4-23. The output current is sensed from  $1m\Omega$  resistor and then filtered to avoid from noises. The maximum value of the current sense amplifier output signal, CS<sub>OUT</sub>, is equal to 0.85V when 17A full load current is drawn.

The output current sense signal is injected into the voltage feedback loop by using a non-inverting summer which is implemented with an op-amp as shown in Fig. 4-24. At the output of the non-inverting summer, an error amplifier and an optocoupler are employed to implement voltage feedback loop compensation and isolation. Type 2 compensation is employed. The feedback signal, FB, is obtained at the output of the optocoupler.



Fig. 4-23. Output current sense stage of the LLC DCX converter.



Fig. 4-24. Non-inverting summer and voltage feedback loop of the LLC DCX converter. The design of the voltage feedback loop is addressed in Chapter 4.5 in detail. The no-load output voltage set point of the module is arranged within the specified limits,  $\pm 0.3\%$ , by using a rheostat in the voltage divider.

NCP1395 resonant mode controller from On Semiconductor is employed as the controller [59]. The NCP1395 has a built-in voltage controlled oscillator, VCO, and produces gate drive signals by using the feedback signal at its FB pin as shown in Fig. 4-25. It provides dead time generation, minimum and maximum switching frequency setting and soft-start functions. The high side and low side gate drive output of the NCP1395 are digital signals. Therefore, these outputs cannot handle the required current for gate driving. A gate driver IC is employed in order to drive primary-side MOSFETs properly as shown in Fig. 4-25. It uses the bootstrap technique to drive high and low side MOSFET together. It receives the digital gate drive signals from the NCP1395 and turns on and off MOSFETs Q1 and Q2. Basically, the bootstrap gate driver turns of firstly  $Q_2$  with the help of  $V_{CC}$  supply. Once Q<sub>2</sub> is on, HB node turns out to be ground. The bootstrap capacitor C<sub>BOOT</sub> charges through the bootstrap diode DBOOT to VCC level. Then, the gate driver turns off Q<sub>2</sub>. In order to turn on Q<sub>1</sub>, the charge stored in C<sub>BOOT</sub> is used. The gate driver connects V<sub>BOOT</sub> node to the high side output when the dead time is finished to turn on Q<sub>1</sub>. This operation continues in a sequential manner.



Fig. 4-25. The controller and gate drive stage of the LLC DCX converter.

#### 4.5. Voltage Feedback Loop Design

To achieve closed loop stability, a compensation circuit must be inserted into the voltage feedback loop of an LLC resonant converter. The compensation circuit ensures adequate phase and gain margins by shaping the loop characteristic. For the proposed LLC DCX converter, type 2 compensation circuit, which is shown in Fig. 4-26, is employed.



Fig. 4-26. Type 2 compensation circuit.

In Fig. 4-26, the op-amp circuit transfer function has an origin pole plus a zero. The second pole is placed after the optocoupler. The transfer function equation of the compensator can be written as [60];

$$G(s) = CTR * \frac{R_{PULLDOWN}}{R_{LED}} * \frac{R_2}{R_1} * \frac{1 + \frac{1}{sR_2C_1}}{1 + sR_{PULLDOWN}C_2} = G_0 * \frac{1 + w_z/s}{1 + s/w_p}$$
(4-22)

4

where:

$$G_0 = CTR * \frac{R_{PULLDOWN}}{R_{LED}} * \frac{R_2}{R_1} = G_1 * G_2$$
(4-23)

$$G_1 = CTR * \frac{R_{PULLDOWN}}{R_{LED}}$$
(4-24)

$$G_2 = \frac{R_2}{R_1}$$
(4-25)

$$w_z = \frac{1}{R_2 C_1}$$
(4-26)

$$w_p = \frac{1}{R_{PULLDOWN}C_2} \tag{4-27}$$

In Eq. (4-23), the mid-band gain,  $G_0$ , consists of two parts: the optocoupler circuit,  $G_1$ , cascaded with the op-amp circuit,  $G_2$ . CTR is the optocoupler current transfer ratio which is specific to the selected device. It directly affects the mid-band gain of the loop and upper limit of the crossover frequency to be selected. By increasing  $R_{PULLDOWN}$ , the mid-band gain can be increased but this also means placing the high frequency pole presented in Eq. (4-23) at lower frequency. Therefore, selecting large  $R_{PULLDOWN}$  may lead to reduction of the selected crossover frequency. On the other hand, the mid-band gain can be increased by decreasing  $R_{LED}$ . The lower limit for the  $R_{LED}$  appears from the controller NCP1395. The NCP1395 can withstand maximum 10V at its FB pin. Then, the minimum value of the  $R_{LED}$  can be derived as;

$$R_{LED\_min} \ge \frac{(V_{EE} - V_{of} - V_{ol}) * R_{PULLDOWN} * CTR_{MAX}}{10}$$
(4-28)

where  $V_{EE}$  is the  $R_{LED}$  bias voltage,  $V_{of}$  is the optocoupler diode forward voltage drop,  $V_{ol}$  is the op-amp low output voltage level,  $CTR_{MAX}$  is the maximum current

transfer ratio of the optocoupler.  $R_{PULLDOWN}$  and  $R_{LED}$  are selected as 500 $\Omega$  and 1k $\Omega$  respectively for the LLC DCX converter.

The capacitor,  $C_2$ , represents the total capacitor on the emitter node of the optocoupler. The  $C_2$  consists of two parts: the added external capacitance  $C_{EX}$  from emitter to ground and the optocoupler parasitic output capacitance  $C_{OPTO}$ . These capacitors appear in parallel in the circuit:

$$C_2 = C_{EX} \mid\mid C_{OPTO} \tag{4-29}$$

 $C_{OPTO}$  plays an important role in the compensation circuit. Its effect is unavoidable. If the value of  $C_{OPTO}$  is large compared to  $C_{EX}$ , it determines the characteristic of the compensation circuit. Since it cannot be changed, it limits the placement of the high frequency pole. In this case, reduction of the selected crossover frequency or exploring new pole/zero combinations can be adopted as a solution. The parasitic output capacitance of the selected device is obtained by measuring. The measurement setup used for this purpose is shown in Fig. 4-27.



Fig. 4-27. Measurement setup for the parasitic output capacitance of an optocoupler [60].

In Fig. 4-27, DC operating point of the optocoupler is fixed with the help of resistors  $R_{PULLUP}$  and  $R_{FORWARD}$  and DC sources  $V_{BIAS1}$  and  $V_{BIAS2}$ . A signal generator is used as an AC source. The injected AC signal is measured from node A and the transferred AC signal is measured from node B. By using AC sweep, the pole introduced by the  $C_{OPTO}$  is measured as 50kHz for the selected device. The value of the  $C_{OPTO}$  can be calculated from;

$$C_{OPTO} = \frac{1}{2\pi * R_{PULLUP} * f_{opto}}$$
(4-30)

The C<sub>OPTO</sub> parameter of the selected device is determined as 7nF.

Now the transfer function of the power stage, H(s), must be extracted in order to calculate the compensator parameters. Since a practical small-signal model is not available for the LLC resonant converter, transfer function of the power stage is obtained by measuring. For this purpose, the measurement setup shown in Fig. 4.28 is implemented [61] [62].



Fig. 4-28. Setup to measure the power stage transfer function of an LLC resonant converter.

As shown in Fig. 4-28, the voltage feedback loop of the LLC resonant converter is break with  $20\Omega$  to inject a small signal. Small signal injection is done by using a signal generator. T1 is a commercial 50Hz transformer which is used to isolate the injected signal. By using an oscilloscope, the signal injected into the loop can be measured from node B whereas the resultant signal coming outside the power stage can be measured from node A. Similarly, the effect of compensation circuit on the injected signal can be measured from node C. By using a frequency sweeping signal, transfer functions of the stages can be measured as;

$$G(s) = \frac{Z}{Y} \tag{4-31}$$

$$H(s) = \frac{X}{Z} \tag{4-32}$$

Also, the open loop transfer function  $G(s) \times H(s)$  can be measured and the crossover frequency, phase and gain margin can be observed from;

$$G(s) * H(s) = \frac{X}{Y}$$
(4-33)

To measure the power stage transfer function, firstly, the converter must work properly. The measurement will be done while the converter is operating and the loop is closed. Therefore, the loop must be stable initially. Otherwise, the converter may have failure. For this purpose, a large-value capacitor can be selected for  $C_1$  to push the loop bandwidth low enough and to obtain a stable loop. The initial value of  $C_1$  can be between 100nF and 1µF.

For the LLC DCX converter,  $C_1$  is selected as 100nF initially. Other parameters are selected as:  $R_1 = 10k\Omega$ ,  $R_2 = 1k\Omega$ ,  $C_2 = 100pF$ . The transfer function of the power stage is drawn by taking multiple measurements at different frequencies as shown in Fig. 4-29.



Fig. 4-29. Bode plots of the power stage.

As can be seen from Fig. 4-29, the power stage gain crosses over the 0-dB axis at 900Hz. It has small DC gain. It has phase rotation larger than -70° above 900Hz. In order to obtain a good input rejection and a low output impedance, open loop DC gain must be large [63]. It is clear that the power stage DC gain is low. Therefore, a right compensation circuit must be employed to obtain safe gain and phase margins.

Before selecting compensator parameters, the open loop crossover frequency must be determined. In power converters, it is common to place the crossover frequency to 1/5<sup>th</sup> or 1/10<sup>th</sup> of the switching frequency. The minimum switching frequency of the LLC DCX is determined as 300kHz previously which means the crossover frequency can be 60kHz or 30kHz. However, such frequencies are very large to implement with a compensation circuit having an optocoupler and its parasitic output capacitance. In order to enlarge the crossover frequency range, the loop midband gain must be improved considerably. This is only possible by arranging the DC operating point of the optocoupler, in other words, by increasing DC currents circulating in the compensation circuit. However, this leads excessive power consumption on resistors such as  $R_{PULLDOWN}$  and  $R_{LED}$ . In order to avoid from such a situation, the crossover frequency,  $f_{crossover}$ , of the proposed LLC DCX is determined as 5kHz. It is clear that selecting a small crossover frequency means the converter output will have large undershoots and overshoots during transients since it reacts slowly. However, this feature is not so critical for an unregulated converter.

From Fig. 4-29, the power stage gain is almost equal to -14dB at 5kHz. The compensator should have 14dB gain boost at 5kHz to place the crossover frequency to the desired point. The optocoupler circuit gain is determined by the selected device and the resistor values;

$$G_1 = CTR * \frac{R_{PULLDOWN}}{R_{LED}} = 0.5 * \frac{500}{1000} = 0.25$$

Then, the op-amp circuit gain can be calculated as;

$$G_2 = \frac{G}{G_1} = \frac{10^{\frac{14}{20}}}{0.25} = 20$$

From Eq. (4-24),  $R_1$  and  $R_2$  values are selected as  $10k\Omega$  and  $200k\Omega$  respectively.

Now, the total phase rotation of the open loop transfer function should be investigated to determine how much phase boost is required at 5kHz to obtain a safe phase margin. Phase margin can be defined as how much the total phase rotation of the open loop transfer function is less than  $-360^{\circ}$  at the crossover frequency. The power stage has  $-83^{\circ}$  phase rotation and the compensator circuit has  $-270^{\circ}$  total phase rotation which means only 7° margin will be obtained. To have a 60° phase margin, the required phase boost at 5kHz can be calculated as;

$$\varphi_{boost} = -360 + 83^\circ + 270^\circ + 60^\circ = 53^\circ$$

The required phase boost can be achieved by adjusting the places of the zero and the pole. For this purpose Eq. (4-34) and Eq. (4-35) can be used [63];

$$f_p = \left(\tan(\varphi_{boost}) + \sqrt{\tan^2(\varphi_{boost}) + 1}\right) * f_{crossover}$$
(4-34)

$$f_z = \frac{f_{crossover}^2}{f_p} \tag{4-35}$$

The pole and the zero is put at 14.9kHz and 1.67kHz respectively. From Eq. (4-26) and (4-27),  $C_1$  and  $C_2$  values are determined as 450pF and 22nF respectively. From Eq. (4-29),  $C_{EX}$  is equal to 15nF. The transfer function of the designed compensator is shown in Fig. 4-30.



Fig. 4-30. Bode plots of the designed compensator.

The obtained parameters are placed into the LLC DCX compensator circuit and the open loop transfer function is measured similarly. Fig. 4-31 shows the open loop bode plots of the LLC DCX converter. As can be seen from Fig. 4-31, the crossover frequency is measured as 8kHz. The phase margin is equal to 60.5°. As shown in Fig. 4-31, the phase plot cannot be obtained for the frequencies smaller than 1kHz due to the noises in the circuit. The measurements are not accurate in this region. Because of the same reason, the gain margin cannot be measured. Transient response characteristics of the LLC DCX module are evaluated in Chapter 5 in detail.



Fig. 4-31. Open loop bode plots of the LLC DCX converter.

Important design considerations related to planar transformer, leakage inductance, primary-side MOSFETs, secondary-side rectifiers and voltage feedback loop have been described in this chapter. Building blocks of the proposed module have been provided in detail. Practical implementation of these blocks are presented.

# **CHAPTER 5**

#### **EXPERIMENTAL RESULTS**

In this chapter, performance characteristics of the proposed LLC DCX module are presented. A two-module array 400W front-end DC/DC converter and a three-module array having 2+1 redundancy configuration have been built and tested to evaluate current sharing performance of the module.

# 5.1. Test Results of Individual LLC DCX Module

In order to measure the output regulation characteristic of the module, an electronic load was used to draw the desired output current from the module and the output voltage was measured instantaneously. The measured output regulation characteristic is shown in Fig. 5-1. The output voltage is 12.55V at no load and 11.77V at full load. It changes almost linearly from no load to full load.



Fig. 5-1. Output regulation characteristic of the module.

Fig. 5-2 and Fig. 5-3 show the critical waveforms at no load and full load conditions for the nominal input voltage. As can be seen from Fig. 5-2 and Fig. 5-3, ZVS operation is achieved. The half-bridge node drops to zero before the low-side MOSFET  $Q_2$  is turned on. In Fig. 5-3, the resonant tank current,  $I_{res}$ , is almost a sinusoidal current which means the converter is operating at the resonant frequency. As stated in Chapter 3.3, the converter is operating at the desired point at full load and nominal input voltage condition.



Fig. 5-2. Critical waveforms through the module at no load:  $CH_1$  (orange) =  $I_{res}$ ,  $CH_2$  (blue) =  $V_{hb}$ ,  $CH_3$  (purple) =  $V_{gs}$  of  $Q_2$ .



Fig. 5-3. Critical waveforms through the module at full load:  $CH_1$  (orange) =  $I_{res}$ ,  $CH_2$  (blue) =  $V_{hb}$ ,  $CH_3$  (purple) =  $V_{gs}$  of  $Q_2$ .

Gate-source voltage waveform of the  $Q_2$  is shown in Fig. 5-4 in detail. Since the drain-source voltage of  $Q_2$  is already zero when the gate is supplied, the drain-gate capacitance,  $C_{gd}$ , does not sink charge. Therefore, there is no flat portion on the waveform, which is called Miller plateau. This situation also shows the converter is operating with soft-switching [64].



Fig. 5-4. Gate-source voltage waveform of the MOSFET Q<sub>2</sub>: CH<sub>1</sub> (orange) =  $I_{res}$ , CH<sub>2</sub> (blue) =  $V_{hb}$ , CH<sub>3</sub> (purple) =  $V_{gs}$  of Q<sub>2</sub>.

The critical waveforms through the converter for the maximum and minimum input voltage conditions are shown in Fig. 5-5 and Fig. 5-6 respectively. The switching frequency of the converter is 360kHz when the input voltage is 360V whereas it is 685kHz when the input voltage is 400V.



Fig. 5-5. Critical waveforms through the module at full load of minimum input voltage:  $CH_1$  (orange) = I<sub>res</sub>,  $CH_2$  (blue) = V<sub>hb</sub>,  $CH_3$  (purple) = V<sub>gs</sub> of Q<sub>2</sub>,  $CH_4$  (green) = V<sub>o</sub>.



Fig. 5-6. Critical waveforms through the module at full load of maximum input voltage:  $CH_1$  (orange) = I<sub>res</sub>,  $CH_2$  (blue) = V<sub>hb</sub>,  $CH_3$  (purple) = V<sub>gs</sub> of Q<sub>2</sub>.

The measured efficiency of the module for different load and input voltage conditions is shown in Fig. 5-7. The module reaches 89.9% maximum efficiency at full load when the nominal input voltage is supplied.



Fig. 5-7. Efficiency of the proposed module.

It should be noted that the measured efficiency at the full load of nominal voltage is considerably lower than the theoretical value calculated in Chapter 4. In Chapter 4, some power losses cannot be calculated analytically. For instance, winding losses resulting from fringing fields due to the air gap are not studied [69]. Also, winding losses resulting from the passive layer of the center-tap configuration are not included [51]. In addition, the vias between turns increase AC resistances of the windings and their effects must be analyzed [70]. In order to estimate more accurately these power losses, FEA must be applied and then transformer design can be optimized.

The LLC DCX module was also tested under transient load conditions. Output voltage response to a load step of 1A to 17A (slew rate =  $1A/\mu$ sec) is shown in Fig. 5-8. The output voltage decreases almost 750mV from no load to full load condition as it is desired. It passes momentarily below the desired output level 11.75V by a voltage of 150mV and then it recovers.



Fig. 5-8. Output voltage response to a load step of 1A to 17A:  $CH_1 = I_o$  (orange),  $CH_4 = V_o$  (green).

Output voltage response to a load step of 17A to 1A (slew rate =  $1A/\mu$ sec) is shown in Fig. 5-9. The output overshoots by a voltage of 60mV. Then, it recovers by going through a small undershoot.



Fig. 5-9. Output voltage response to a load step of 17A to 1A:  $CH_1 = I_o$  (orange),  $CH_4 = V_o$  (green).

Transient response characteristics of the module can be improved by increasing the crossover frequency of the open loop transfer function, which is implemented as 8 kHz in Chapter 4.5. For this purpose, DC gain of the open loop transfer function can be increased by changing circuit parameters. For instance, DC operating point of the optocoupler can be changed to improve DC gain of the compensation circuit. However, power consumption of the compensation circuit also increases at the same time. The trade-off should be evaluated in the design stage.

Fig. 5-10 shows the output voltage ripple at full load condition. The output voltage peak-to-peak ripple is about 105mV. It should be noted that the ripple voltage can be increased or decreased by changing the output capacitor value.



Fig. 5-10. Output voltage ripple at full load condition:  $CH_1 = I_o$  (orange),  $CH_4 = V_o$  (green).

In order to observe thermal behaviors of the circuit components, thermal imaging technique was applied. Thermal images of the module was captured at the full load and nominal input voltage condition. Two heat sinks, which are shown in Fig. 5-11, were placed on the primary-side MOSFETs and secondary-side rectifiers in order to ensure continuous safe operation of the module.

Fig. 5-12 and Fig 5-13 show thermal images of the module captured by thermal camera. The ambient temperature was 25 °C and thermal images were captured after 10 minutes operation. Fig. 5-12 shows the upper side of the module where heat sinks were placed. The highest temperature was recorded as 59.4 °C at the transformer winding. Fig. 5-13 shows the bottom side of the module. There exist some hot spots on the bottom side of the PCB due to the primary-side MOSFETs and secondary-side rectifiers which are soldered on the opposite side. The highest temperature was recorded as 83.9 °C under the secondary-side rectifiers.



Fig. 5-11. Two heat sinks used for the module.









# 5.2. Test Results of Modular Front-end DC-DC converter

### 5.2.1. Two-module 400W Front-end DC-DC converter

A two-module array 400W front-end DC/DC converter, which is shown in Fig. 5-14, has been built and tested to evaluate the current sharing performance of the module.



Fig. 5-14. Two-module array 400W front-end DC/DC converter.

The front-end DC/DC converter was loaded from no load to full load and each module's output current was measured to determine the current sharing error of the array. Current sharing error for each load condition is shown in Fig. 5-15. As shown in Fig. 5-15, the current sharing error is smaller than 10% for the output currents larger than 6A. At light load conditions, the error becomes larger than 10% due to the nonlinearity in the output regulation characteristic shown in Fig. 5-1.



Fig. 5-15. Current sharing error between two modules.

Current sharing performance of the LLC DCX module was also tested under transient load conditions. Current sharing response of the modules to a load step of 17A to 34A (slew rate =  $1A/\mu$ sec) is shown in Fig. 5-16. As shown in Fig. 5-16, the output current of the Module 1 is 8.8A initially whereas it is 8.2A for the Module 2. After the load step, both of the modules increase their output currents in a similar manner. However, the Module 1 has a larger overshoot 21.6A while it is 18.6A for the Module 2. Then, the output currents settle to their steady-state values 17.8A and 16.2A respectively.



Fig. 5-16. Current sharing response of two modules to a load step of 17A to 34A:  $CH_1 = I_o$  of Module 1 (orange),  $CH_2 = I_o$  of Module 2 (blue),  $CH_4 = V_o$  (green).

Current sharing response of the modules to a load step of 34A to 17A (slew rate =  $1A/\mu$ sec) is shown in Fig. 5-17. From Fig. 5-17, the output current of the Module 1 is 17.8A initially whereas it is 16.2A for the Module 2. After the load step, both of the modules decrease their output currents in a similar manner. However, the Module 1 has a larger undershoot 4.5A while it is 7.2A for the Module 2. Then, the output currents settle to their steady-state values 8.8A and 8.2A respectively.

As shown in Fig. 5-16 and 5-17, transient current sharing performance of the modules was tested with a half load step and there are considerable current oscillations on the output current of the Module 1. In Fig. 5-16, after the load step, the difference between the module currents reaches its maximum, 3A, while it is 1.6A at steady-state. Similarly, Module 1's output current has a larger undershoot in Fig. 5-17. As a result, droop method's dynamic current sharing performance is not as good as its steady-state performance [71].



Fig. 5-17. Current sharing response of the modules to a load step of 34A to 17A:  $CH_1 = I_o$  of Module 1 (orange),  $CH_2 = I_o$  of Module 2 (blue),  $CH_4 = V_o$  (green).

## 5.2.2. 2+1 Three-module Front-end DC-DC converter

A redundant LLC DCX module was added to the two-module front-end DC/DC converter in order to build a fault-tolerant converter. Three-module array having 2+1 redundancy configuration is shown in Fig. 5-18. The module was placed as a hot redundant unit. It will operate continuously in the array and in case of a failure it will take over loading by increasing its output power. In such a configuration, the converter can resume supply without any break.



Fig. 5-18. Three-module array having 2+1 redundancy configuration.

To observe the current sharing performance of the modules, two different tests were conducted. Firstly, 400W is drawn from the array and each module's output current is measured at steady-state to evaluate the maximum current sharing error. The results of the measurements are shown in Table 5-1.

Output current of 2+1 front-end DC/DC converter	34A
Output current of Module 1	11.7A
Output current of Module 2	10.7A
Output current of redundant module	11.6A
Maximum current sharing error	8.8%

Table 5-1. Steady-state current sharing performance of the 2+1 front-end DC/DC converter.

Secondly, in order to demonstrate the effect of a module failure on the array, the Module 1 was turned off (the input supply of the module is removed with a circuit breaker) while the output power was 400W. When the Module 1 was turned off, the Module 2 and the redundant module shared the total output power. Transient current sharing performance of the array in this situation is shown in Fig. 5-19. As shown in Fig. 5-19, at the beginning, the modules share the total output power equally. Then, the output current of Module 1 decreases to zero quickly after it is turned off. At the same time, the remaining modules increase their output currents by almost 5.9A to compensate for the gap in the supply. It should be noted that only the output current of the redundant module is shown in Fig. 5-19. The response of the Module 1 was turned off. After Module 1 is removed, the output voltage of the converter decreases almost 300mV to settle 11.77V since now each module conducts almost 17A. 2+1 three-module front-end DC-DC converter can resume power supply without any break as shown in Fig 5-20.

In this chapter, performance characteristics of the proposed LLC DCX module has been presented. Both steady-state and transient current sharing performance of the module has been demonstrated by testing a two-module array 400W front-end DC-DC converter and a three-module 400W front-end DC-DC converter having 2+1 redundancy configuration.



Fig. 5-19. Transient current sharing performance of the three-module array:  $CH_1 = I_o$  of Module 1 (orange),  $CH_2 = I_o$  of redundant module (blue).



Fig. 5-20. Output voltage response of the three-module array: CH<sub>4</sub> = Output Voltage (green).
## **CHAPTER 6**

#### **CONCLUSIONS and FUTURE WORK**

### 6.1. Conclusions

A traditional high-power front-end DC/DC converter can be replaced with an array of paralleled standardized converter modules when modular design is applied. Modular front-end DC/DC converters achieve many desirable properties: expandability of output power capacity, redundancy implementation, simplified thermal management and reduced design cost. However, in order to benefit from modular design, load current sharing must be accomplished among the paralleled modules.

In this thesis, an LLC resonant converter has been designed and implemented as an unregulated DCX module to be employed in modular front-end DC/DC converters. In order to achieve current sharing capability, the droop current sharing method was employed in the proposed module.

The droop current sharing method has been reviewed and key design parameters have been determined for the proposed LLC DCX module. To implement the droop method, voltage feedback loop of the converter and inherent gain characteristic of the LLC resonant converter topology were manipulated. This approach does not degrade the efficiency of the module. In addition, it is not affected from any resonant tank mismatch among the paralleled modules.

To design the proposed LLC DCX module, a methodical design process has been developed. The proposed method can be used to design the LLC resonant converter

topology as an DCX employing the droop current sharing method. Voltage transfer function of the topology was obtained by using FHA method and key design parameters were determined to select the circuit components of the resonant tank. The design of the proposed module was finalized by using peak gain curves and circuit analysis.

Practical design considerations related to primary-side MOSFETs and secondaryside rectifiers were addressed. In order to build a low-profile module, a planar transformer was employed in the LLC DCX module. Critical design considerations related to the planar transformer was described. To achieve high power density, the leakage inductance of the transformer was utilized as the resonant inductance of the topology. The magnitude of the leakage inductance was analyzed and important design parameters were presented.

To achieve closed loop stability, a compensation circuit was designed and implemented in the proposed module. Power plant transfer function of the LLC DCX converter was obtained through bench tests. Type 2 compensation circuit with an optocoupler was employed to reshape the loop transfer function and to achieve isolation. The circuit implementation was studied in detail.

A 500kHz 200W LLC DCX module converting 360-400VDC input to 12.5-11.75VDC output has been built and its performance characteristics has been demonstrated. The proposed module achieved desired load regulation characteristic and 89.9% efficiency at full load of nominal input voltage. Two LLC DCX modules connected in parallel shared the load current effectively. At steady-state, current sharing error of the two-module front-end DC/DC converter was found as 9.4% at full load. Dynamic current sharing performance of the droop method was evaluated and it was observed that its performance is not as good as its steady-state performance.

Three-module front-end DC/DC converter which has 2+1 redundancy configuration was implemented and both steady-state and transient current sharing performance of the proposed module was investigated. It was observed that the front-end DC/DC converter can continue to operate in case of a failure thanks to the redundant module.

A conference paper was presented at the 8th International Conference on Power Electronics, Machines and Drives (PEMD 2016) covering some of the work conducted in this thesis.

## 6.2. Future Work

The LLC DCX module presented in this thesis achieved 3.36 W/cm<sup>3</sup> (55.1 W/in<sup>3</sup>) power density and reached 89.9% maximum efficiency at full load. In addition, current sharing feature is realized effectively. While the proposed design has demonstrated good performance characteristics, some possible future works may be conducted to further improve the proposed DCX module:

- **Design optimization:** A methodical design process has been developed to select the resonant tank components of the LLC DCX module. However, the proposed design methodology does not include any optimization strategy. Basically, it provides a set of resonant tank components satisfying the required voltage gain. An optimization procedure may be developed for the proposed design method to maximize the efficiency of the DCX module.
- Transformer design optimization: A low-profile planar transformer has been implemented in the LLC DCX module. To design the planar transformer, core losses, winding losses, winding arrangement and leakage inductance has been analyzed conventionally and it is not designed optimally. At high switching frequencies, copper losses and core losses increase significantly and effect considerably the overall efficiency of the module. To achieve an optimal transformer design, the relationship between the losses and the design parameters such as switching frequency, conductor positions, number of turns, interlayer vias, core material, core geometry and air gap position has to be studied. In addition, FEA simulations should be applied to determine the losses and leakage inductance of the planar transformer.
- Synchronous Rectification: Secondary-side rectifiers are one of the major loss contributors of the design. To improve the efficiency of the module, synchronous rectification (SR) can be employed. However, it is difficult to

implement SR in the LLC resonant converter. Unlike PWM converters, driving signals of the primary-side switches cannot be applied to the secondary-side switches directly for the LLC resonant converter. Some alternative techniques has already been developed for this purpose in the literature. These techniques can be studied and applied in the proposed module to further improve the efficiency.

#### REFERENCES

[1] J. D. van Wyk and F. C. Lee, "On a Future for Power Electronics," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 1, no. 2, pp. 59-72, June 2013.

[2] S. Luo, "A review of distributed power systems part I: DC distributed power system," in *IEEE Aerospace and Electronic Systems Magazine*, vol. 20, no. 8, pp. 5-16, Aug. 2005.

[3] F. C. Lee, P. Barbosa, Peng Xu, Jindong Zhang, Bo Yang and F. Canales, "Topologies and design considerations for distributed power system applications," in *Proceedings of the IEEE*, vol. 89, no. 6, pp. 939-950, Jun 2001.

[4] C. Zhou, R. B. Ridley and F. C. Lee, "Design and analysis of a hysteretic boost power factor correction circuit," *21st Annual IEEE Power Electronics Specialists Conference*, 1990. PESC '90, San Antonio, TX, USA, 1990, pp. 800-807.

[5] F. Musavi, M. Edington, W. Eberle and W. G. Dunford, "Evaluation and Efficiency Comparison of Front End AC-DC Plug-in Hybrid Charger Topologies," in *IEEE Transactions on Smart Grid*, vol. 3, no. 1, pp. 413-421, March 2012.

[6] A. B. Bondi, "Characteristics of scalability and their impact on performance," in proceedings of the 2nd international workshop on software and performance, 2000. NY, USA, 2000, pp. 195-203.

[7] A. Birolini, *Reliability Engineering: Theory and Practice*, 7th ed. Berlin, Germany: Springer Science & Business Media, 2013, pp. 1-41.

[8] Shiguo Luo, Zhihong Ye, Ray-Lee Lin and F. C. Lee, "A classification and evaluation of paralleling methods for power supply modules," *Power Electronics Specialists Conference, 1999. PESC 99. 30th Annual IEEE*, Charleston, SC, 1999, pp. 901-908.

[9] RCP-1000 Datasheet, 2016. [Online]. Available: http://www.meanwell.com/mw\_search/RCP-1000/RCP-1000-spec.pdf

[10] IPC-300A Datasheet, 2013. [Online]. Available: https://www.meanwellweb.com/en/product-info/ac-dc-power-supply/enclosed-type/201-300-w/ipc-300/product/IPC-300A

[11] W. Feng, P. Mattavelli and F. C. Lee, "Pulsewidth Locked Loop (PWLL) for Automatic Resonant Frequency Tracking in LLC DC–DC Transformer (LLC- DCX)," in IEEE Transactions on Power Electronics, vol. 28, no. 4, pp. 1862-1869, April 2013.

**[12]** J. Y. Lee, Y. S. Jeong, H. J. Chae, K.M. Yoo, J. J. Chang, and J. H. Chang, "Two-stage insulated bidirectional DC/DC power converter using a constant duty ratio LLC resonant converter," U.S. Patent 2011/0090717A1, April 2011.

[13] Yuancheng Ren, Ming Xu, Julu Sun and F. C. Lee, "A family of high power density unregulated bus converters," in *IEEE Transactions on Power Electronics*, vol. 20, no. 5, pp. 1045-1054, Sept. 2005.

**[14]** R. V. White, "Emerging on-board power architectures," *Applied Power Electronics Conference and Exposition, 2003. APEC '03. Eighteenth Annual IEEE*, Miami Beach, FL, USA, pp. 799-804, vol.2, 2003.

[15] D. Huang, S. Ji and F. C. Lee, "Matrix transformer for LLC resonant converters," Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE, Long Beach, CA, USA, pp. 2078-2083, 2013.

[16] H. Niu, Y. Pei, X. Yang, L. Wang and Z. Wang, "Design of high power density DC Bus Converter based on LLC resonant converter with synchronous rectifier," *Power Electronics and Motion Control Conference, 2009. IPEMC '09. IEEE 6th International*, Wuhan, pp. 540-543, 2009.

[17] T. Jin and K. Smedley, "Multiphase LLC Series Resonant Converter for Microprocessor Voltage Regulation," *Conference Record of the 2006 IEEE Industry Applications Conference Forty-First IAS Annual Meeting*, Tampa, FL, pp. 2136-2143, 2006.

[18] E. Orietti, P. Mattavelli, G. Spiazzi, C. Adragna and G. Gattavari, "Current sharing in three-phase LLC interleaved resonant converter," *2009 IEEE Energy Conversion Congress and Exposition*, San Jose, CA, pp. 1145-1152, 2009.

[19] E. Orietti, P. Mattavelli, G. Spiazzi, C. Adragna and G. Gattavari, "Two-phase interleaved LLC resonant converter with current-controlled inductor," *2009 Brazilian Power Electronics Conference*, Bonito-Mato Grosso do Sul, pp. 298-304, 2009.

[20] Z. Hu, Y. Qiu, Y. F. Liu and P. C. Sen, "An interleaving and load sharing method for multiphase LLC converters," *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE*, Long Beach, CA, USA, pp. 1421-1428, 2013.

**[21]** J. Jang, S. Choi, B. Choi and S. Hong, "Average current mode control to improve current distributions in multi-module resonant dc-to-dc converters," *Power Electronics and ECCE Asia (ICPE & ECCE), 2011 IEEE 8th International Conference on*, Jeju, pp. 2312-2319, 2011.

[22] B. T. Irving and M. M. Jovanovic, "Analysis, design, and performance evaluation of droop current-sharing method," *Applied Power Electronics Conference and Exposition, 2000. APEC 2000. Fifteenth Annual IEEE*, New Orleans, LA, pp. 235-241, vol.1, 2000.

[23] Alan J. Fenn, Donald H. Temme, William P. Delaney, and William E. Courtney, "The Development of Phased-Array Radar Technology", Lincoln Laboratory Journal, Volume 12, No 2, 2000.

[24] A. K. Agrawal, B.A. Kopp, M. H. Luesse, K. W. O'Haver, "Active phased array antenna development for modern shipboard radar systems", Johns Hopkins Apl Technical Digest, Volume 22, No 4, 2001.

[25] B. Yang, "Topology investigation of front end DC/DC converter for distributed power system," Ph.D. dissertation, Virginia Polytechnic Institute and State University, 2003.

[26] J. F. Lazar and R. Martinelli, "Steady-state analysis of the LLC series resonant converter," *Applied Power Electronics Conference and Exposition, 2001. APEC 2001. Sixteenth Annual IEEE*, Anaheim, CA, pp. 728-735, vol. 2, 2001.

[27] Bo Yang, F. C. Lee, A. J. Zhang and Guisong Huang, "LLC resonant converter for front end DC/DC conversion," *Applied Power Electronics Conference and Exposition, 2002. APEC 2002. Seventeenth Annual IEEE*, Dallas, TX, pp. 1108-1112, vol. 2, 2002.

**[28]** C. Person, "Selection of Primary Side Devices for LLC Resonant Converters", M.Sc. Thesis, Virginia Polytechnic Institute and State University, 2008.

[29] D. Fu, B. Lu and F. C. Lee, "1MHz High Efficiency LLC Resonant Converters with Synchronous Rectifier," 2007 IEEE Power Electronics Specialists Conference, Orlando, FL, 2007, pp. 2404-2410.

[30] H. de Groot, E. Janssen, R. Pagano and K. Schetters, "Design of a 1-MHz LLC Resonant Converter Based on a DSP-Driven SOI Half-Bridge Power MOS Module," in IEEE Transactions on Power Electronics, vol. 22, no. 6, pp. 2307-2320, Nov. 2007.

[31] R. Ren, S. Liu, J. Wang and F. Zhang, "High frequency LLC DC-transformer based on GaN devices and the dead time optimization," *2014 International Power Electronics and Application Conference and Exposition*, Shanghai, pp. 462-467, 2014.

[32] H. Chen and X. Wu, "LLC resonant DC transformer (DCX) with parallel PWM output tight regulation," *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, Pittsburgh, PA, pp. 4742-4747, 2014.

[33] Q. Chen, J. Wang, Y. Ji and S. Liang, "Soft starting strategy of bidirectional LLC resonant DC-DC transformer based on phase-shift control," 2014 9th IEEE

Conference on Industrial Electronics and Applications, Hangzhou, pp. 318-322, 2014.

[34] J. S. Glaser and A. F. Witulski, "Output plane analysis of load-sharing in multiple-module converter systems," in *IEEE Transactions on Power Electronics*, vol. 9, no. 1, pp. 43-50, Jan 1994.

[35] C. Prasantanakorn, "Current Sharing Method for Resonant DC-DC Transformers," M.Sc. Thesis, Virginia Polytechnic Institute and State University, 2011.

[36] Technical Specification IQ4H, Rev. G, 2014. [Online]. Available: http://www.synqor.com/Datasheets/IQ4HxxxHTXxx\_Datasheet.pdf

[37] Mini Family 375V Input, Rev. 9.5, 2016. [Online]. Available: http://cdn.vicorpower.com/documents/datasheets/ds\_375vin-mini-family.pdf

**[38]** R. L. Steigerwald, "A comparison of half-bridge resonant converter topologies," Applied Power Electronics Conference and Exposition, 1987 IEEE, San Diego, CA USA, 1987, pp. 135-144.

[**39**] Film Capacitors, Metallized Polypropylene Film Capacitors (MKP), Series/Type: B32671L-B32672 Datasheet, 2016. [Online]. Available: https://en.tdk.eu/inf/20/20/db/fc\_2009/MKP\_B32671L\_672L.pdf

[40] E32/6/20/R Planar E Cores and Accessories Datasheet, 2008. [Online]. Available: http://ferroxcube.home.pl/prod/assets/e32620r.pdf

[41] H. Huang, "Designing an LLC Resonant Half-Bridge Power Converter," Texas Instrument Application Note SLUP263, 2010.

**[42]** B. Lu, W. Liu, Y. Liang, F.C. Lee, J.D. Van Wyk, "Optimal design methodology for LLC resonant converter," in Applied Power Electronics Conference and Exposition, 2006. APEC '06, pp.533-538, 2006.

**[43]** Z. Fang, S. Duan, C. Chen, X. Chen and J. Zhang, "Optimal design method for LLC resonant converter with wide range output voltage," Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE, Long Beach, CA, 2013, pp. 2106-2111.

**[44]** Xue Zhang, Wei You, Wei Yao, Shen Chen and Zhengyu Lu, "An improved design method of LLC resonant converter," Industrial Electronics (ISIE), 2012 IEEE International Symposium on, Hangzhou, 2012, pp. 166-170.

**[45]** H. Ding, "Design of Resonant Half-Bridge converter using IRS2795(1,2) Control IC," International Rectifier Application Note AN-1160.

[46] F. Musavi, M. Craciun, M. Edington, W. Eberle and W. G. Dunford, "Practical design considerations for a LLC multi-resonant DC-DC converter in battery

charging applications," 2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, FL, 2012, pp. 2596-2602.

[47] L. Dixon, "Designing planar magnetics," Texas Instrument Application Note, 2003.

[48] STL33N60M2 Datasheet, Rev. 3, 2015. [Online]. Available: http://www.st.com/content/ccc/resource/technical/document/datasheet/5e/95/33/de /53/7d/4b/d5/DM00078624.pdf/files/DM00078624.pdf/jcr:content/translations/en. DM00078624.pdf

**[49]** H. Choi, "Half-Bridge LLC Resonant Converter Design Using FSFR-Series Fairchild Power Switch (FPS<sup>™</sup>)," Fairchild Application Note, 2014.

[50] 3F4 Material Specification, 2008. [Online]. Available: http://www.ferroxcube.com/FerroxcubeCorporateReception/datasheet/3f4.pdf

[51] L. Dixon, "Eddy Current Losses in Transformer Windings and Circuit Wiring," Texas Instrument Application Note, 2003.

[52] S. Xiao, "Planar Magnetics Design For Low-Voltage DC-DC Converters," M.Sc. Thesis, University of Central Florida, 2004.

**[53]** Z. Ouyang, O. C. Thomsen and M. A. E. Andersen, "Optimal Design and Tradeoff Analysis of Planar Transformer in High-Power DC–DC Converters," in IEEE Transactions on Industrial Electronics, vol. 59, no. 7, pp. 2800-2810, July 2012.

**[54]** Z. Ouyang, O. C. Thomsen and M. A. E. Andersen, "The analysis and comparison of leakage inductance in different winding arrangements for planar transformer," 2009 International Conference on Power Electronics and Drive Systems (PEDS), Taipei, 2009, pp. 1143-1148.

[55] A. Ankoudinov, V. Rodov, "Adjustable Field Effect Rectifier," U.S. Patent 2009/0078962A1, March 2009.

[56] Rectifiers, ST Microelectronics, 2013. [Online]. Available: http://www.compel.ru/wordpress/wp-

content/uploads/2013/11/Rectifier\_presentation\_Aug2013.pdf

[57] FERD20U50 Datasheet, Rev. 3, 2015. [Online]. Available: http://www.st.com/content/ccc/resource/technical/document/datasheet/12/bb/0c/88 /9c/71/46/f6/DM00109554.pdf/files/DM00109554.pdf/jcr:content/translations/en. DM00109554.pdf

**[58]** Primary Side MOSFET Selection for LLC Topology, Rev 1.0, Infineon Application Note, 2014.

[59] NCP1395A/B Datasheet, Rev. 4, 2008. [Online]. Available: http://www.onsemi.com/pub\_link/Collateral/NCP1395-D.PDF

[60] C. Basso, *Designing Control Loops for Linear and Switching Power Supplies*. London, England: Artech House, 2012. pp. 253-308.

[61] H. Huang, "Feedback Loop Design of an LLC Resonant Power Converter," Texas Instrument Application Note SLUA582A, 2010.

**[62]** How to Measure the Loop Transfer Function of Power Supplies, Texas Instrument Application Note AN-1889, 2013.

[63] C. Basso, "The TLV431 in Switch-Mode Power Supplies loops: part II". [Online]. Available: http://cbasso.pagespersoorange.fr/Downloads/Papers/The%20TL431%20in%20loop%20control.pdf

**[64]** An introduction to LLC resonant half-bridge converter, Rev. 2, ST Microelectronics Application Note AN2644, 2008.

[65] E22/6/16/R Planar E Cores and Accessories Datasheet, 2008. [Online]. Available:

http://www.ferroxcube.com/FerroxcubeCorporateReception/datasheet/e22616.pdf

[66] M. Mu, "High Frequency Magnetic Core Loss Study," Ph.D. Thesis, Virginia Polytechnic Institute and State University, 2013.

[67] P. L. Dowell, "Effects of Eddy Currents in Transformer Windings," Proceedings IEE (UK), Vol. 113, No.8, pp.1387-1394, August 1966.

**[68]** J. Deng, S. Li, S. Hu, C. C. Mi and R. Ma, "Design Methodology of LLC Resonant Converters for Electric Vehicle Battery Chargers," in IEEE Transactions on Vehicular Technology, vol. 63, no. 4, pp. 1581-1592, May 2014.

**[69]** W. A. Roshen, "Fringing Field Formulas and Winding Loss Due to an Air Gap," in IEEE Transactions on Magnetics, vol. 43, no. 8, pp. 3387-3394, Aug. 2007.

[70] Z. Ouyang, "Advances in Planar and Integrated Magnetics," Ph.D. Thesis, Technical University of Denmark, 2011.

[71] J. Sun, "Dynamic Performance Analyses of Current Sharing Control for DC/DC Converters," Ph.D. Thesis, Virginia Polytechnic Institute and State University, 2007.

### APPENDIX

[A1] O. S. Alemdar, O. Keysan, "Design and Implementation of an Unregulated DC-DC Transformer (DCX) Module using LLC Resonant Converter," in Proc. The 8th International Conference on Power Electronics, Machines and Drives (PEMD 2016), Glasgow, U.K., April 2016.

# Design and Implementation of an Unregulated DC-DC Transformer (DCX) Module using LLC Resonant Converter

Öztürk Şahin Alemdar\*, Ozan Keysan<sup>†</sup>

\*Aselsan Inc., Turkey, osalemdar@aselsan.com.tr †Middle East Technical University, Turkey, keysan@metu.edu.tr

**Keywords:** LLC resonant converter, DC-DC transformer, current sharing, modular power converter.

#### Abstract

Traditional high-power centralized front-end DC/DC converter can be replaced with an array of paralleled standardized DC/DC transformer (DCX) modules when load current sharing is accomplished between individual modules. In this study, an LLC resonant converter is proposed as an unregulated DCX module, which has current sharing capability. Current sharing feature is implemented by using the droop current sharing method. A methodical design process is presented for the selection of the resonant tank components. A 500kHz, 100W LLC DCX module having 360-410V input and 12.5-12.1V output is designed and tested. Current sharing performance of the proposed module is demonstrated using a two-module array 200W front-end DC/DC converter.

### **1** Introduction

High efficiency, high power density, improved reliability and cost-effectiveness are the ever-present design requirements of power supplies. In order to meet these requirements, Distributed Power System (DPS) architectures are widely adopted in modern power supplies thanks to their many benefits [1, 2]. A typical DPS with intermediate bus architecture employs power factor correction (PFC) converter, front-end DC/DC converter and multiple point-of-load converters (POLs). With modular approach, these stages can be configured as an array of paralleled standardized converter modules as shown in Fig. 1. By this configuration, it is possible to achieve expandability of output power capacity, simplified thermal management, redundancy implementation and hence improved reliability.

In Fig. 1, power processing functions are distributed among the converter blocks. The front-end DC/DC converter provides an isolated low voltage distribution bus to power the non-isolated POLs which are employed for voltage level generation and regulation. Therefore, the front-end DC/DC converter can be designed as a semi-regulated or unregulated single-output DC/DC converter, which is referred to as DC/DC transformer (DCX) [3]. DCX can achieve high efficiency with high power density [4, 5]. The front-end DC/DC converter can be designed modularly by using standardized DCX modules as shown in Fig 2.



Fig. 2. Modular front-end DC/DC converter based on DCX modules.

In Fig. 2, in order to benefit from paralleling, load current sharing among the DCX modules is required. Parallel modules do not share the load current inherently due to the mismatches in the power stage and control parameters [6]. Some of the modules in the array may deliver a disproportionate fraction of the load current unless forced current sharing method is designed into the array. In a current-sharing array, modules deliver almost the same amount of power. Thus, they tend to have similar working temperatures during operation. As a result, modules have similar service lives resulting in improved reliability.

The LLC resonant converter, which is shown in Fig. 3, is an attractive topology for implementing an unregulated DCX module [7]. Primary-side switches of the LLC resonant converter can achieve zero voltage switching (ZVS) for no load to full load range. In addition, turn-off current of the primary-side switches are low. Also, secondary-side switches can achieve zero current switching (ZCS). As a result, the LLC

resonant converter can achieve high efficiency levels while operating at high switching frequencies.



Fig. 3. LLC resonant converter

Although LLC resonant converters were used as DCXs in previous studies [4, 5, 8, 9], array operation and current sharing topics were not addressed. In [10-12], current sharing methods are developed for interleaved LLC resonant converter modules. However, the proposed current sharing methods are not suitable for the design of a standardized DCX module. Design of an unregulated LLC DCX module with current sharing capability was presented in [13], but additional components were employed in the topology in order to implement the current sharing method.

In this study, an LLC resonant converter is proposed as an unregulated DC-DC transformer (DCX) module. A 500kHz, 100W LLC DCX module having 360-410V input and 12.5-12.1V output is designed. In order to realize current sharing feature, the droop current sharing method is employed in the LLC DCX module. A closed-loop control is utilized to implement the droop method actively. In addition, a design method is developed for the selection of the resonant tank components. A two-module array 200W front-end DC/DC converter is built and current sharing performance is tested.

In Section 2, the droop current sharing method for the LLC resonant converter is reviewed. Section 3 presents a closed-loop control that is employed for implementing the droop current sharing method. Section 4 provides the design method developed for the LLC DCX module. Finally, Section 5 presents the experimental results.

# **2** Droop Current Sharing Method for the LLC Resonant Converter

The proposed LLC DCX module employs the droop current sharing method, in which current sharing is achieved by load regulation characteristics of the paralleled converters [14]. Fig. 4 shows the parallel connection of two power converters to demonstrate the droop method. As shown in Fig. 4(b), in this method, current sharing among the converters is determined by either the difference between the output voltage set points ( $V_{o1}$ ,  $V_{o2}$ ) or the difference between the slopes of the load regulation characteristics ( $R_{o1}$ ,  $R_{o2}$ ) of the converters. Due to the mismatches in these parameters, power converter #1 delivers slightly more load current than power converter #2, when the output voltage is equal to  $V_o$ . In order to achieve an acceptable current sharing accuracy (i.e. the difference between the current amounts delivered by individual modules), load

regulation characteristics of the modules must be properly designed.

In order to implement the droop method, pre-selection of the output voltage set point accuracy can be adopted as



Fig. 4. (a) Parallel connection of two power converters. (b) Load regulation characteristics of the paralleled converters.

a design approach. Then, the required load regulation slope can be determined to ensure the specified current sharing accuracy. It should be noted that there is a trade-off between the slope and the load regulation range. Output voltage droop increases as the load regulation slope becomes steeper.

The desired load regulation characteristic of the LLC DCX module to implement the droop method is shown in Fig. 5.



Fig. 5. Load regulation characteristic of the LLC DCX module

The droop voltage, V<sub>d</sub>, and droop resistance, R<sub>d</sub>, are defined as;

$$V_d = V_{(NL)} - V_{(FL)} \tag{1}$$

$$R_d = V_d / I_{(FL)}$$
(2)

where  $V_{(NL)}$  and  $V_{(FL)}$  are the no load and full load output voltage respectively and  $I_{(FL)}$  is the full load output current.

Load regulation characteristics of N LLC DCX modules connected in parallel as an array, which share a total load current Io, are depicted in Fig. 6. It can be seen that the load regulation characteristics of the modules lie within the defined output voltage set point accuracy range  $\pm \Delta V_{o(SP)}$ . The module with the highest output voltage set point delivers

the highest current,  $I_{\rm H}$ , whereas the one with the lowest output voltage set point delivers the lowest current,  $I_{\rm L}$ .

The difference between the highest and the lowest module current is defined as;



(3)

Fig. 6. Load regulation characteristics of N LLC DCX modules connected in parallel

Then, the maximum relative current sharing error can be defined as [14];

$$CS_{error} = \Delta I_o / (I_o / N) \tag{4}$$

I<sub>o</sub>/N is equal to the full load current of single module;

$$(I_o/N) = I_{(FL)} \tag{5}$$

From Eq. (3), (4) and (5), the maximum relative current sharing error can be redefined as;

$$CS_{error} = 2 * \Delta V_{o(SP)} / V_d \tag{6}$$

For the array of the LLC DCX modules, the current sharing error is specified as 15%. For a good trade-off between the output voltage set point accuracy and the droop voltage, the output voltage set point accuracy is determined as  $\pm 0.25\%$ . From Eq. (6), the required droop voltage can be calculated as 0.4V when the output voltage set point is selected as 12.5V. Output voltage range of the module is arranged such that the output voltage is 12.5V at no load and 12.1V at full load. Fig. 7 shows the required load regulation characteristic of the LLC DCX module to implement the droop method with the specified current sharing error.



Fig. 7. Required load regulation characteristic for the LLC DCX module

# **3** Droop Voltage Implementation by using Voltage Feedback Loop

Inherent voltage gain characteristic of the LLC resonant converter can be manipulated to implement the droop voltage. A typical voltage gain characteristic of the LLC resonant converter having 500kHz resonant frequency is shown in Fig. 8. As can be seen from Fig. 8, the voltage gain obtained from the resonant tank decreases as the load current increases when the converter works at a fixed switching frequency either in the below or above resonant frequency region.



Fig. 8. A typical voltage gain characteristic of the LLC resonant converter

Switching frequencies of 300kHz and 750kHz are marked in Fig. 8 to demonstrate the inherent gain characteristic of the resonant tank.  $\Delta M_g$  is the difference between the voltage gain of the resonant tank at no load and full load conditions, which are  $M_{g(NL)}$  and  $M_{g(FL)}$  in Fig. 8. By selecting the operating frequency, required droop voltage can be obtained as shown in Fig. 9.



Fig. 9. Droop voltage implementation by using inherent gain characteristic

The main drawback of this approach is the operating point of the converter gets far away from the resonant frequency. The peak efficiency of the LLC resonant converter is achieved at the resonant frequency. Therefore, efficiency of the converter decreases. In addition, the droop characteristic is directly dependent on the resonant tank components. Therefore, any mismatch occurring between the resonant tanks of paralleled DCX modules results in current sharing mismatch. High gain obtained from the resonant tank makes the converter sensitive to the operating frequency. In this approach, a serious current sharing error may be occurred due to non-identical voltage gain characteristics of the paralleled modules. To solve the resonant tank mismatch issue, the droop method can be implemented actively by using the voltage feedback loop of the converter. In order to implement the droop method actively, an output current sense signal is injected into the voltage feedback loop to modify its characteristic to obtain required droop voltage as shown in Fig. 10.



Fig. 10. The block diagram of the active droop method

In Fig. 10,  $V_{OS}$  and  $I_{OS}$  are the sense signals which are proportional to the output voltage  $V_o$  and output current  $I_o$ respectively. The sum of these sense signals is compared to reference voltage  $V_{REF}$  at the error amplifier EA. Control loop ensures that the output voltage decreases as the output current increases. Control voltage  $V_c$  is the output of the EA and it is applied to the voltage-controlled oscillator VCO to determine the switching frequency  $f_{sw}$  of the converter.

In this study, the droop method is implemented by using this approach. The conversion gain of the LLC resonant converter decreases as the switching frequency is increased from the below resonant frequency region to the resonant frequency as shown in Fig 11. The LLC DCX module is designed to operate at the below resonant frequency region at no load and to operate in the close vicinity of the resonant frequency at full load. The output voltage of the module is decreased by switching frequency as the load current increases. Therefore, maximizing full load efficiency is realized by the control algorithm of the LLC DCX module. An example operating line of the designed module is marked in Fig. 11.



Fig. 11. Operating line of the LLC DCX module

As can be seen from the operating line shown in Fig. 11, the LLC DCX module operates at different frequencies determined by the load condition. The resonant frequency of the LLC DCX module is determined as 500kHz. The switching frequency range of the module is determined as 300kHz-600kHz to

implement the active droop method. Also, the nominal input voltage of the module is selected as 384V.

# 4 Design Method Developed for the LLC DCX Module

Conventionally, LLC resonant converters are designed to have line regulation and load regulation. In order to achieve these regulations, design of the resonant tank should satisfy maximum gain requirement of the application. The resonant tank consists of three passive components causing design complexity; resonant inductance  $L_r$ , resonant capacitance  $C_r$ and magnetizing inductance  $L_m$ . Two key elements are commonly used in the resonant tank design;

$$L_n = \frac{L_m}{L_r} \tag{9}$$

$$Q_e = \frac{\sqrt{Lr/Cr}}{\frac{8*n^2}{m^2}*R_L}$$
(10)

where  $L_n$  is the inductance ratio between  $L_m$  and  $L_r$ ,  $Q_e$  is the quality factor, n is the transformer turn ratio and  $R_L$  is load resistance.

 $L_n$  and  $Q_e$  determine the gain behaviour of the resonant tank with regard to the switching frequency. For different  $L_n$  and  $Q_e$ combinations, attainable peak gain of the resonant tank changes. Peak gain curves obtained from different  $L_n$  and  $Q_e$ values can be utilized in the design of the LLC resonant converter to determine the resonant tank components [15].

The LLC DCX module designed in this paper does not have load regulation. In fact, it has a predetermined output regulation characteristic to implement the droop method. In order to visualize the effect of the predetermined regulation characteristic on the selection of  $L_n$  and  $Q_e$ , a simple design methodology is developed.

Firstly, the maximum gain requirement of the module is obtained, which can be determined using Eq. (12);

$$M_{g\_max} = \frac{n*(V_0 + V_{drop})}{V_{in\_min/2}}$$
(12)

where  $V_o$  is the output voltage,  $V_{drop}$  is the voltage drop in the power stage due to power losses and  $V_{in_min}$  is the minimum input voltage.  $M_{g_max}$  changes with the output voltage of the module. Dependence of  $M_{g_max}$  on the output voltage is shown in Fig. 12 for the designed module.



Fig. 12. Dependence of Mg max on the output voltage

Since the output voltage changes with the load condition,  $M_{g_max}$  is also dependent on the load,  $R_L$ . Then, by using Eq. (10), it is simple to derive dependence of  $M_{g_max}$  on  $Q_e$ , when a  $\sqrt{Lr/Cr}$  value is chosen. For different  $\sqrt{Lr/Cr}$  values, maximum required gain versus  $Q_e$  curves can be obtained for the designed converter as shown in Fig. 13.



Fig. 13. The relationship between  $M_{g_{max}}$  and  $Q_e$  for different  $\sqrt{Lr/Cr}$  values

These obtained curves can be placed inside the peak gain curves as shown in Fig. 14 to determine  $L_n$ . Design of the converter can be done easily by selecting  $L_n$  and  $\sqrt{Lr/Cr}$ .



As can be seen from Fig. 14, the largest possible  $L_n$  value is 9 due to the maximum required gain at no load condition. After  $L_n$  is selected as 9,  $\sqrt{Lr/Cr}$  can be selected. From Fig. 14,  $\sqrt{Lr/Cr}$  can be selected as any value below 32. When  $\sqrt{Lr/Cr}$  is larger than 32, the resonant tank cannot satisfy the required gain at full load. In other words,  $Q_e$  cannot be greater than 0.34 when  $L_n$  is selected as 9 for the module.

At this stage, the aim is to select proper  $\sqrt{Lr/Cr}$  value in order to finalize the design. Selected  $\sqrt{Lr/Cr}$  affects three important design criteria. Firstly, the value of the resonant capacitor C<sub>r</sub> is determined from Eq. (13) when a value is assigned to  $\sqrt{Lr/Cr}$ . It should be noted that f<sub>o</sub> is previously selected as 500kHz.

$$C_r = \frac{1}{2\pi * f_0 * \sqrt{L_r/C_r}} \tag{13}$$

Secondly, voltage rating of the C<sub>r</sub> is determined by the selected  $\sqrt{Lr/Cr}$  value. RMS voltage of the resonant capacitor can be determined using Eq. (14);

$$V_{Cr\_RMS} = \frac{2*n*V_o + 2*I_{pri\_pk}*\sqrt{L_r/C_r} - V_{in}}{2\sqrt{2}}$$
(14)

where  $I_{pri\_pk}$  is the primary-side peak current and  $V_{in}$  is the input voltage.

 $C_r$  handles high frequency AC current circulating in the resonant tank. Before a capacitor is selected as  $C_r$ , its voltage rating has to be derated with regard to the operating frequency. For example, a 15nF metallized polypropylene film capacitor rated at 700V RMS can withstand only up to 80V RMS with a 600kHz switching frequency [16]. Therefore, voltage derating becomes a critical aspect of the design process.

From Eq. (14), it seems that smaller  $\sqrt{Lr/Cr}$  will be advantageous when the resonant capacitor's RMS voltage is considered. However, selected  $\sqrt{Lr/Cr}$  value also has impact on the primary-side current. Once  $\sqrt{Lr/Cr}$  is selected, magnetizing inductance L<sub>m</sub> becomes determined because of previously selected parameters, namely, f<sub>o</sub> and L<sub>n</sub>;

$$L_m = \frac{L_n * \sqrt{L_r / C_r}}{2\pi * f_o} \tag{15}$$

 $L_m$  directly determines the primary-side RMS current which affects the efficiency of the converter. Primary-side RMS current causes conduction loss on the primary-side switches. By assuming primary-side current has sinusoidal waveform, its magnitude can be derived as;

$$I_{pri\_RMS} = \sqrt{\frac{\left(\frac{I_{O}*\pi}{2*n}\right)^2 + \left(\frac{V_{in}/2}{2*L_{m}*2*f_{SW}}\right)^2}{2}}$$
(16)

where  $I_o$  is the output current and  $f_{sw}$  is the switching frequency of the converter.

In order to carry out the selection of  $\sqrt{Lr/Cr}$  for the designed LLC DCX module, the curves obtained from Eq. (14), (15) and (16) are plotted in Fig. 15.



Fig. 15. The selection of  $\sqrt{Lr/Cr}$ 

5 Experimental Implementation

The prototype of a 500kHz, 100W LLC DCX module with 360-410V input and 12.5-12.1V output is implemented as shown in Fig. 16. Cr is selected as 15nF and then corresponding  $\sqrt{Lr/Cr}$  value is 21.2 as shown in Fig. 15. L<sub>m</sub> is implemented as  $62\mu$ H. Leakage inductance of the transformer is used as  $L_r$ which is 6.5uH. The dimensions of the module are 104mm\*66mm\*15mm.



Fig. 16. The prototype of the LLC DCX module

The output regulation characteristic of the module achieved for the droop method is shown in Fig. 17.



Fig. 17. The output regulation characteristic of the module

The experimental waveforms when the input voltage is 384V and the output voltage is 12.1V are shown in Fig. 18. It can be seen that ZVS is achieved and the module operates in close vicinity of the resonant frequency at full load condition.



Fig. 18. Experimental waveforms; CH1: IRES, CH2: VDS of Q2, CH3: VGs of Q2

The efficiency curve of the module for different load conditions is shown in Fig 19. The converter reaches 87.5% maximum efficiency at full load. Synchronous rectification has not been implemented yet, causing efficiency reduction by 6-7%.



Fig. 19. Efficiency of the module

Two LLC DCX modules are connected in parallel to observe the current sharing performance. Current sharing errors for different load conditions are shown in Table 1. Output voltage set points of the modules are 12.52V and 12.51V.

Output Current (A)	2	4	6	8	10	12	14	16	18
CS Error (%)	0,5	1,0	1,0	0,3	0,3	0,6	0,8	0,9	0,9

Table 1. Current sharing performance of the two-module array

#### 6 Conclusion

In this paper, an LLC DCX module having current sharing capability is designed and implemented. Design and implementation of the droop current sharing method and the selection of the resonant tank components are presented. Experimental results shows that the proposed module achieves desired load regulation characteristic and 87.5% efficiency at full load. Two LLC DCX modules connected in parallel achieve 0.9% current sharing error at full load.

#### Acknowledgements

The authors wish to thank ASELSAN Inc. for the valuable support in the design and implementation of the prototypes.

#### References

- Luo, S., "A review of distributed power systems part I: DC distributed power system", [1] in IEEE Aerospace and Electronic Systems Magazine, vol.20, no.8, pp.5-16, Aug. 2005. Van Wyk, J.D.; Lee, F.C., "On a Future for Power Electronics", in IEEE Journal of
- [2] Emerging and Selected Topics in Power Electronics, vol.1, no.2, pp.59-72, June 2013.
- White, R.V., "Emerging on-board power architectures", in Applied Power Electronics Conference and Exposition, 2003, APEC '03, pp.799-804, Feb. 2003. [3]
- Huang, D.; Ji, S.; Lee, F.C., "Matrix transformer for LLC resonant converters", in [4] Applied Power Electronics Conference and Exposition (APEC), 2013, pp.2078-2083, March 2013.
- Niu, H.; Pei, Y.; Yang X.; Wang L.; Wang Z., "Design of high power density DC Bus [5] Converter based on LLC resonant converter with synchronous rectifier" in Power Electronics and Motion Control Conference, 2009. IPEMC '09, pp.540-543, May 2009.
- Luo, S.; Ye, Z.; Lin, R.; Lee, F.C., "A classification and evaluation of paralleling [6] methods for power supply modules", in Power Electronics Specialists Conference, 1999, PESC 99, pp.901-908, 1999.
- Yang, B.; Lee, F.C.; Zhang, A.J.; Guisong Huang, "LLC resonant converter for front end [7] DC/DC conversion", in Applied Power Electronics Conference and Exposition, 2002, APEC 2002, pp.1108-1112, 2002.
- [8] Ren, R.; Liu, S.; Wang, J.; Zhang, F., "High frequency LLC DC-transformer based on GaN devices and the dead time optimization", in International Electronics and Application Conference and Exposition (PEAC), 2014, pp.462-467, Nov. 2014.
- [9] Feng, W.; Mattavelli, P.; Lee, F. C., "Pulsewidth Locked Loop (PWLL) for Automatic Resonant Frequency Tracking in LLC DC-DC Transformer (LLC -DCX)", in IEEE Transactions on Power Electronics, vol.28, no.4, pp.1862-1869, April 2013.
- [10] Orietti, E.; Mattavelli, P.; Spiazzi, G.; Adragna, C.; Gattavari, G., "Current sharing in three-phase LLC interleaved resonant converter", in Energy Conversion Congress and Exposition, 2009, ECCE 2009, pp.1145-1152, Sept. 2009.

- [11] Hu, Z.; Qiu, Y.; Liu, Y.; Sen, P.C., "An interleaving and load sharing method for multiphase LLC converters", in Applied Power Electronics Conference and Exposition (APEC), pp.1421-1428, March 2013.
  [12] Jang, J.; Choi, S.; Choi, B.; Hong, S., "Average current mode control to improve current distributions in multi-module resonant de-to-dc converters", in IEEE 8th International Conference and Purpur Electronic Local Conference and Purpur Electronic Conference and Purpur Electronic Conference and Purpur Electronic Conference and Purpur Electronic Conference and Purpur Electronic Conference and Purpur Electronic Conference and Purpur Electronic Conference and Purpur Electronic Conference and Purpur Electronic Conference and Purpur Electronic Conference and Purpur Electronic Conference and Purpur Electronic Conference and Purput Electronic Conference and Purpu
- Conference on Power Electronics and ECCE Asia (ICPE & ECCE), 2011, pp.2312-2319,
- [13]
- [14]
- Conference on Power Electronics and ECCE Asia (ICPE & ECCE), 2011, pp.2312-2519, 2011. C. Prasantanakorn, "Current Sharing Method for Resonant DC-DC Transformers", M.Sc. Dissertation, Virginia Polytechnic Institute and State University, 2011. Irving, B.T.; Jovanovic, M.M., "Analysis, design, and performance evaluation of droop current-sharing method", in Applied Power Electronics Conference and Exposition, 2000, APEC 2000, pp.235-241, 2000. Lu, B.; Liu, W.; Liang, Y.; Lee, F.C.; Van Wyk, J.D., "Optimal design methodology for LLC resonant converter", in Applied Power Electronics Conference and Exposition, 2006. APEC '06, pp.533-538, 2006. "Metallized Polypropylene Film Capacitors (MKP), Series/Type: B32671L...B32672L", Jan. 2016. http://en.tdk.eu/inf/20/20/db/fc\_2009/ [15]
- [16] MKP\_B32671L\_672L.pdf