LIGHT TRAPPING MICRO AND NANOSTRUCTURES FABRICATED BY TOP DOWN APPROACHES FOR SOLAR CELL APPLICATIONS

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ABSTRACT

LIGHT TRAPPING MICRO AND NANOSTRUCTURES FABRICATED BY TOP DOWN APPROACHES FOR SOLAR CELL APPLICATIONS

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For an ultimate victory of solar energy over polluting fossil fuels, we need to decrease the cost of electricity generated from the sun. The technology based on photovoltaic (PV) solar cell is offering the most promising alternative in this energy conversion. However, this can be possible only if we can reduce the cost of solar cell fabrication and/or increase the conversion efficiency. In order to increase the performance/cost ratio of solar cells, new approaches reducing optical and electrical losses are necessary during the absorption of the light and collection of charge carriers. In this work we focused on the fabrication techniques and the application of various nanostructures on Si surface towards a better light management of the cell surface. The efficiency of a solar cell strongly depends on the properties of the interaction between the incoming light beam and the surface of the device. In order to maximize the absorption and the efficiency of the cell, various light trapping schemes have been proposed. We have applied various lithography techniques such as optical lithography, nanoimprint lithography (NIL), hole mask colloidal lithography (HCL) to generate various nano structures including nano holes patterns. After these pattern transfer process steps, either dry plasma etching or wet chemical etching techniques were

applied. For metal assisted chemical etching different metals like silver, gold, titanium were used as the catalyst of the etching. The effect of metal, metal layer thickness, process time and orientation of the wafer were studied. Structural properties of the features like hole diameter, pitch size, depth were varied and optimized. With a variety of texturing and etching process types, at the end of the study, periodic and random-introduced-periodic patterns were successfully implemented to solar cell fabrication step. The performances of the solar cells were investigated both optically and electrically.

Keywords: surface texturing with micro and nano holes, periodic patterning, reactive ion etching, metal assisted etching, nanoimprint lithography, hole colloidal lithography.

ÖZ

GÜNEŞ HÜCRE UYGULAMALARI İÇİN IŞIK HAPSEDİCİ MİKRO VE NANOYAPILARIN YUKARDAN AŞAĞI YAKLAŞIM METODLARIYLA HAZIRLANMASI

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Güneş enerjisinin, çevre kirliliğine sebep olan fosil yakıtlar karşısında nihai zaferi için güneşten üretilen elektriğin maliyetini azaltmamız gerekir. Fotovoltaik güneş hücrelerini temel alan teknoloji, bu enerji dönüşümünde en umut verici alternatifi sunmaktadır. Bununla birlikte, güneş pilinin üretim maliyetini düşürebilir ve/veya güneş hücresinin enerji dönüştürme verimliliğini arttırabilirsek bu mümkün olabilir. Güneş pillerinin performans/maliyet oranını arttırmak için, ışığın emilimi ve yük taşıyıcıların toplanması esnasında, optik ve elektriksel kayıpları azaltacak yeni yaklaşımlar gerekmektedir. Bu çalışmada, hücre yüzeyinde daha iyi bir ışık yönetimi için Si yüzeyinde çeşitli mikro ve nano yapıların üretim teknikleri ve uygulamaları üzerinde duruldu. Bir güneş gözesinin verimliliği, yüzeyin gelen güneş ışıklarıyla etkileşmesine bağlıdır. Yüzeye gelen ışığın emiliminin maksimumda olması alternatif yüzey şekilleriyle mümkündür. Hücrenin ışık emilimini ve verimini en üst düzeye çıkartmak için çeşitli ışık hapsedici yapılar önerilmiştir.Nano delik desenleri de dahil olmak üzere çeşitli mikro ve nano boyutlarda yapılar üretmek için optik litografi, nanodarbe litografisi (NIL), kolloidal delik maske (HCL) gibi çeşitli litografi tekniklerine başvurduk. Bu desen aktarım üretim adımlarından sonra reaktif iyon aşındırma (RIE) ve metal yardımlı kimyasal aşındırma (MAE) teknikleri uygulanmıştır. MAE işleminde yüzeye gümüş, altın, titanyum gibi farklı metaller buharlaştırılmıştır. Metallerin türlerine, yüzeydeki kalınlıklarına, kullanılan pulun

maruz kaldığı işlem tipine, pulun atom dizilişlerine göre oluşabilecek farklı sonuçları incelenmiştir. Maskede tanımlanmış olan değişik çap, periyot, ve derinlik değerlerine göre, tanımlanan her parametre için ayrı işlem basamakları optimize edilmiştir. Farklı çap ve periyotlardaki yüzey şekilleri, pek çok farklı kimyasal işlem süreçleriyle, düzenli ve düzenli dizilimin içinde oluşturulmuş rastgele bir dağılımla sonuçlanmıştır. Değişik derinlik ve dağılımlardaki yüzey şekilleriyle başarılı bir şekilde güneş gözeleri üretilmiştir. Üretilen gözelerin verimlilikleri optik ve elektriksel olarak incelenmiştir.

Anahtar kelimeler: mikro ve nano deliklerle yüzey şekillendirme, periyodik şekillendirme, reaktif iyon aşındırma, metal yardımlı aşındırma, nanodarbe litografi, kolloidal delik maske litografi

Dedicated to,

loving memory of my father, Emin Tekin Altınoluk,

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NOMENCLATURE

A	Absorption
a-Si	Amorphous silicon
AFM	Atomic Force Microscopy
AM1.5	Air Mass 1.5
Al	Aluminum
ARC	Antireflection coating
BCB	Benzocyclobutene
BSF	Back surface field
CB	Conduction band
c-Si	Crystalline silicon
Cz	Czochralski
CVD	Chemical Vapor Deposition
DOF	Depth of focus
Dry-HCL	Dry plasma etching and hole mask colloidal lithography
Dry-NIL	Dry plasma etching and nanoimprint lithography
DUV	Deep ultra violet
E	Energy
E_G	Energy band gap
Epifoils	Epitaxially grown silicon foils
Epifree	Epitaxy-free
FF	Fill factor
HCL	Hole mask colloidal lithography
HF	Hydrofluoric acid
ICP	Inductively Coupled Plasma
I_{SC}	Short circuit current
J	Current density
J_{mpp}	Current density at maximum power point
J_0	Dark saturation current density

J_{SC}	Short circuit current density
KOH	Potassium hydroxide
LPCVD	Low Pressure Chemical Vapor Deposition
MAE	Metal assisted chemical etching
MPP	Maximum power point
NA	Numerical aperture
N_D	Doping concentration
NIL	Nanoimprint lithography
ODTS	Octadecyltrichlorosilane
PECVD	Plasma enhanced chemical vapor deposition
PI	Polyimide
P_{mpp}	Power density at maximum power point
PS	Polystyrene
PV	Photovoltaic
R	Reflectance
RES	Resolution
R_d	Diffuse Reflectance
RIE	Reactive ion etching
RSA	Relative suface area
SEM	Scanning Electron Microscope
Si_3N_4	Silicon nitride
SiO_2	Silicon dioxide
STE	Solar Thermal Electricity
T	Transmittance
TCO	Transparent Conductive Oxide
TMAH	Tetramethylammonium hydroxide
V	Voltage
VB	Valence band
V_{mpp}	Voltage at maximum power point
V_{oc}	Open circuit voltage
Wet-HCL	Wet chemical etching and hole mask colloidal lithography
Wet-NIL	Wet chemical etching and nanoimprint lithography

CHAPTER 1

INTRODUCTION

One of the most important issues of our times is the energy demand to support our lives which are becoming more sophisticated and demanding with time. The amount of energy needed to maintain and improve the quality of our lives is increasing drastically. This energy is mostly provided by burning fossil fuels like coal, natural gas, and liquid oils that are not sustainable from several point of views. The environmental threat due to the increased CO_2 emission resulting from fossil fuels to the atmosphere is increasing to a dangerous level for the future of next generations. Moreover, the uneven distribution of these resources creates a lot of social and economic problems, which causes conflicts and even wars between different nations. We can overcome this problem by reducing the use of fossil fuels in the energy supply.

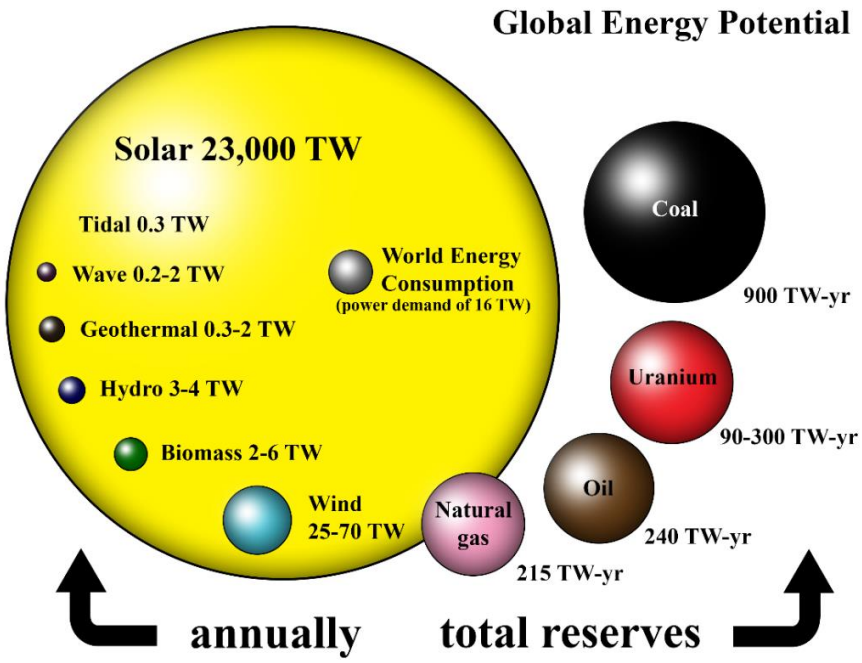


Figure 1.1 Finite (total recoverable) and renewable (yearly potential) energy reserves (in Terawatt-years) [1]

The energy resources alternative to the fossil fuels can be wind, hydro, chemical, geothermal and solar energy. Among these, solar energy represent an ultimate and most promising solution to the energy problem of the human beings. Figure 1.1 compares the known energy sources on our planet [1]. We see that sun provides us with the energy whose amount is higher than the sum of all other energy types, and is much higher than what we need to support our lives.

Solar energy composing of individual photons can be converted into electrical energy by two methods: Solar Thermal Electricity (STE) which is based on steam generation by concentrated solar radiation, and Photovoltaic (PV) which converts the energy of photons into electricity by a direct method based on a junction formed between two materials, mostly semiconductors. In recent years, PV Technologies have become favorable over STE due to their cost and applicability advantages [2]. However, for an ultimate victory over the fossil fuels, the performance/cost ratio of the PV system should be improved even further. For this purpose, we need to not only decrease the cost of manifacturing, but also increase the efficiency of the conversion as high as possible.

A solar cell is an electronic device converting sun power into electricity based on photovoltaic principles [3]. Here, the conversion process can be divided into three stages: i) absorption of the incoming photons followed by an electron-hole generation, ii) transportation of these carriers to the junction region, and finally iii) separation of them from each other with the help of a junction and forming an electrical current at the external load. First process is an optical process which requires a good light management while the other two are electronic ones which are crucially important for an efficient current generation [4]. Optical end electrical properties of a solar cell should match each other to reach an optimum operation [5]. We need to create material structures to obtain good electrical and optical properties. The efficiency of a solar cell strongly depends on the properties of the interaction between the incoming light beam and the surface of the device [6,7]. A proper surface texturing can significantly boost the light absorption, and hence electron-hole generation [8–16]. Our aim in this work is to investigate the use of some new surface structures created by advanced lithography techniques in solar cell technologies.

Surface patterning can be done either randomly or periodically [16–18]. For random patterning pyramid texturing is widely applied for standard wafer thicknesses

around 150-170 µm, but when we want to go thinner, pyramids are not good candidates[19,20]. Radial junction solar cells with holes having sizes varying from micron to sub-micron level are promising candidates on relatively thinner wafers for which pyramid texturing is not an option due to high amount of Si consumption during pyramid texturing process [21–29]. The core of this thesis is fabrication of micro and nano holes by top down approaches, reactive ion etching (RIE) [30], metal assisted etching (MAE) [31], nanoimprint lithography (NIL) [32] and hole mask colloidal lithography (HCL) [33]. According to diameter, pitch, depth values, with the details given in literature [23], we devised a design guideline. We managed to fabricate our periodic patterns properly. The second part of this study includes solar cell fabrication using these structures. We have successfully implemented these new surface structures on solar cell using standard cell fabrication methods.

1.1 Photovoltaic Energy Conversion and Solar Cells

PV power generation system is based on the direct conversion of sunlight into electricity using semiconducting materials which exhibit the photoelectric effect enabling absorption of photons and thus generation of free charge carriers and electrical current. A solar cell is the smallest unit of PV systems. When these cells are connected electrically, they create a module, which can be grouped into larger solar arrays to construct big power stations. Today there exist PV based solar energy plants with a generation power exceeding 500 MW. With more than 250 GW installation worldwide, PV systems have proven to be a reliable and sustainable alternative to other energy resources [34].

In all PV cells, light absorption initiates electrons' motion, by exciting them from the valence band to the conduction band providing free carriers needed to create of a current in the external load. Upon creation of electron-hole pair, they should be separated before they recombine, which can be achieved by a potential asymmetry formed at the junction point of two different materials. Such an asymmetric potential profile can be best formed by a p-n junction fabricated in a semiconductor by doping with different elements [35]. A typical p-n junction and its potential profile is shown in Figure 1.2 on next page.

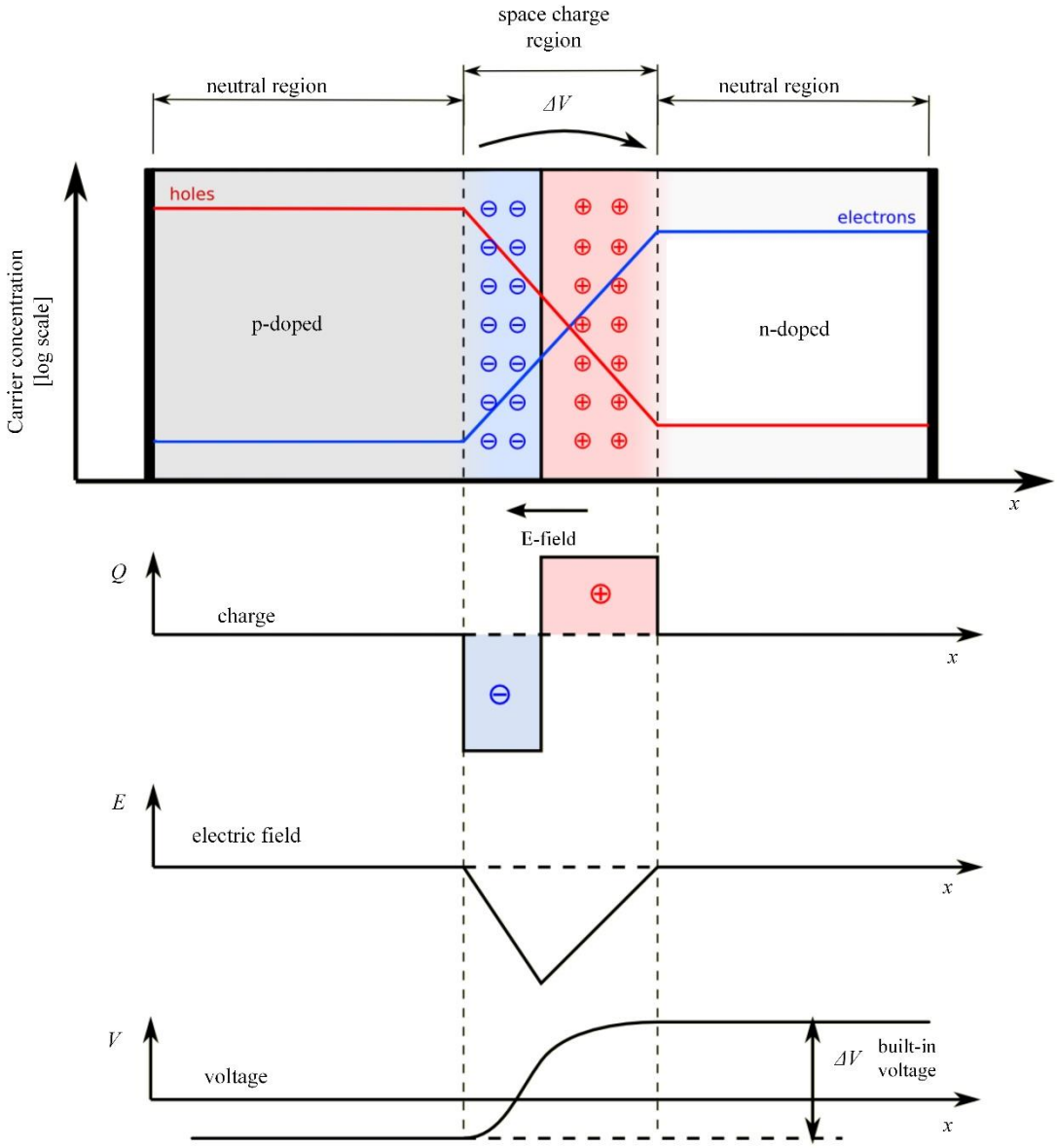


Figure 1.2 A p–n junction in thermal equilibrium under zero-bias voltage. Electron and hole concentration are depicted with blue and red lines, respectively. Gray regions are charge-neutral. Light-blue zone is negatively and light-red zone is positively charged region

Upon junction formation, electrons from negatively charged n region will diffuse towards positively charged p region where they recombine with a hole. A positively charged atom in the n-type region and a negatively charged atom in the p-type are left behind, creating an electric field. As a result of electric field, there will be a drift current towards the opposite direction of the diffused current. When drift and diffusion currents are equal, we are at the equilibrium state with a depletion region (no

free carriers) and a built in potential as a result of electric field are formed at p-n junction [36].

A typical solar cell is made up of simple p-n junction described above. Under illumination, electron-hole pairs are generated and the minority carriers (holes in n-type and electrons in p-type) diffuse to the junction where they are separated by the formed electric field and they become majority carriers. An ideal solar cell can be explained with diode equation, first introduced by Shockley written in Equation 1.1 [37]:

$$J(V) = J_0\left(e^{\frac{qV}{nk_bT}} - 1\right) - J_{ph} \tag{1.1}$$

J_0: the dark saturation current

J_{ph}: the photo-generated current density

n: the diode ideality factor

k_b: Boltzmann constant

q: elementary charge

T: the cell's temperature

For a solar cell, the current, which is generated by sunlight, flows in reverse direction with respect to forward bias (dark) diode, hence the illuminated current-voltage (*IV*) curve is shifted to negative values as depicted in Figure 1.3. The short circuit current density (Jsc) and the open circuit voltage (Voc) are obtained from the intersection of the IV curve. Maximum power density determines the current density and voltage at this operating point J_{mpp} and V_{mpp}. The basic concepts are highlighted in Figure 1.3, such as Jsc, Voc, the maximum power point (mpp) along with the corresponding combination of J_{mpp} and V_{mpp} related to the maximum generated power (P_{mpp}) as well as the fill factor (FF) which is the ratio of the squares under the *JV* curve and the product of Jsc and Voc [2].

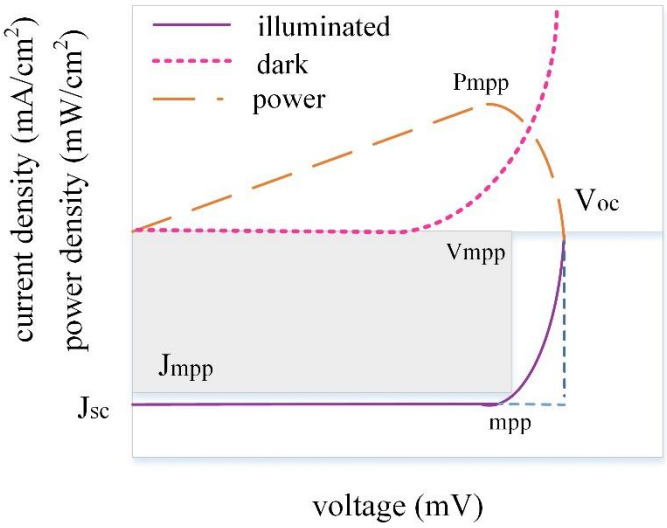


Figure 1.3 Schematic representation of current voltage (IV) characteristics of a solar cell in the dark and under illumination and the generated power per operating point

The energy conversion efficiency (η) is calculated from these parameters as:

$$\eta = \frac{P_{mpp}}{P_{in}} = \frac{J_{mpp}.V_{mpp}}{P_{in}} = \frac{J_{sc}.V_{oc}.FF}{P_{in}} \tag{1.2}$$

The single diode equation assumes a constant value for the ideality factor n. In reality the ideality factor is a function of voltage across the device. At high voltage values, when the recombination of the device is dominated by the surfaces, the ideality factor is close to one, but for lower voltages recombination in junction dominates and the ideality factor approaches two. In order to make a more accurate and realistic extraction double diode model should be taken into account. Schematic representation of a double diode model is showed in Figure 1.4 [38].

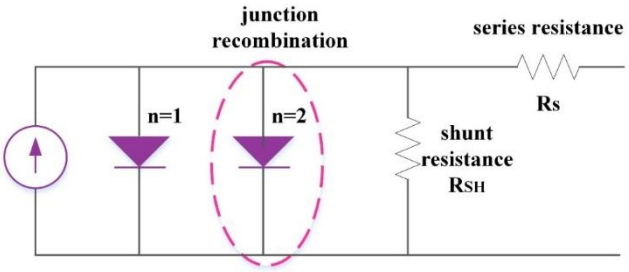


Figure 1.4 Circuit diagram of the double diode model including the parasitic series and shunt resistances

The equation of the double diode model under illumination is:

$$J(V) = J_L - J_{01}\left\{\exp\left[\frac{q(V+JR_s)}{kT}\right]-1\right\} - J_{02}\left\{\exp\left[\frac{q(V+JR_s)}{2kT}\right]-1\right\} - \frac{V+JR_s}{R_{shunt}} \tag{1.3}$$

The equation of the double diode model in the dark is:

$$J(V) = J_{01}\left\{\exp\left[\frac{q(V-JR_s)}{kT}\right]-1\right\} + J_{02}\left\{\exp\left[\frac{q(V-JR_s)}{2kT}\right]-1\right\} + \frac{V-JR_s}{R_{shunt}} \tag{1.4}$$

In both the light and dark cases the "-1" terms in the exponential are typically ignored as it makes the analysis far easier.

Under illumination:

$$J(V) = J_L - J_{01}\exp\left[\frac{q(V+JR_s)}{kT}\right] - J_{02}\exp\left[\frac{q(V+JR_s)}{2kT}\right] - \frac{V+JR_s}{R_{shunt}} \tag{1.5}$$

In the dark:

$$J(V) = J_{01}\exp\left[\frac{q(V-JR_s)}{kT}\right] + J_{02}\exp\left[\frac{q(V-JR_s)}{2kT}\right] + \frac{V-JR_s}{R_{shunt}} \tag{1.6}$$

For real case the performance of a solar cell is limited by some loss mechanisms: optical, recombination and electrical losses. These loss mechanisms are the reason of the decrease in the efficiency of a c-Si solar cell [39].

1.2 Crystalline Si Solar Cells

PV industry is overwhelmingly dominated by crystalline Si (c-Si) solar cells with efficiency values ranging from %17 to %25. Market share of this technology has increased from 80 percent to over %90 in the last 10 years [40]. Depending on the growth technique, c-Si wafers can be in mono-crystalline or multi-crystalline form [41,42]. Photo of these wafer types and cross sectional view of the cell structure are shown in Figure 1.5.

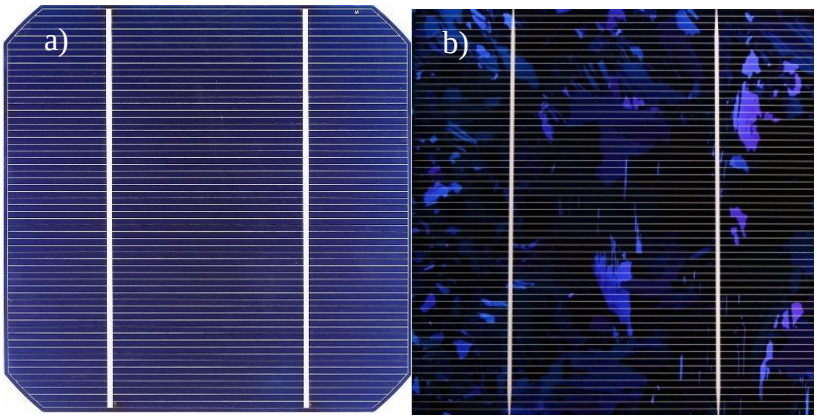


Figure 1.5 a) Mono-crystalline and b) multi-crystalline solar cells

Although depth of the p-n junction is about 0.5 µm, the thickness of a Si wafer is approximately 200 µm and 180 µm for multi-crystalline and mono-crystalline types. This thickness is needed for the handling purposes [43]. Most of the incoming light is absorbed by Si in the first 50 µm of the wafer [44]. Remaining part of the Si wafer is useless and represents waste of material which is one of the main sources of high cost in c-Si solar cell fabrication. One of the most intensively studied topics of recent investigations is on the use of thinner wafers to reduce the material cost [45–49]. However, when the wafer thickness is reduced another important problem emerges : as a poor absorber due to its indirect band gap, red and infrared part of the useful solar spectrum pass through Si wafer without being absorbed [9,50,51]. The cell is said to

be “optically thin” in this case [52–54]. In order to overcome this problem, an efficient light trapping strategy is needed, enormous amount of research groups are working on this [54–59]. Some of these approaches have been studied in this thesis work.

1.3 Optical Processes on Si Surface and Surface Texturing

When a ray of monochromatic light impinges on a flat section of semiconductor as shown in Figure 1.6, a certain amount of light, *R*, will be reflected and the remainder, T, will be transmitted into the semiconductor. The transmitted light, which can be absorbed within the semiconductor, will excite electrons from occupied low-energy states to unoccupied higher-energy states.

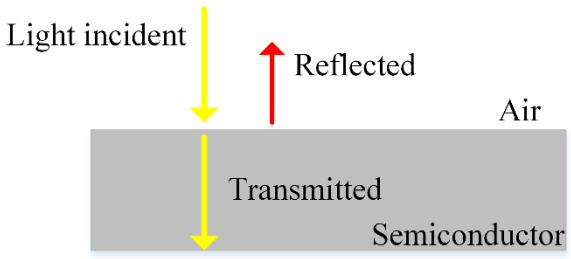


Figure 1.6 Ray of monochromatic light incident on semiconductor

The fraction of light reflected from an absorber material with a refraction index, $n_c = n - ik$, where k is the extinction coefficient for normal incidence is given by Equation 1.7 [5]:

$$R = \frac{(n-1)^2 + k^2}{(n-1)^2 + k^2} \tag{1.7}$$

Extracting the suitable values for Si depicts that for entire wavelengths involved in solar cell work, more than 30% of the incident light is reflected. This is definitely not desirable and needs to be reduced for an efficient solar cell. This problem can be solved and solar cell performance can be improved by either antireflective coatings, or creating a light trapping surface structure or both [60–65]. Due to the technological importance, a large amount of work has been devoted to light-trapping studies. Commercial single-crystalline and multi-crystalline Si solar cells all use roughened surfaces and antireflection coatings to trap more sun light within the cell

[43]. Changing surface topography with random textures can be interpreted in terms of grating with large periodicity [20,45].

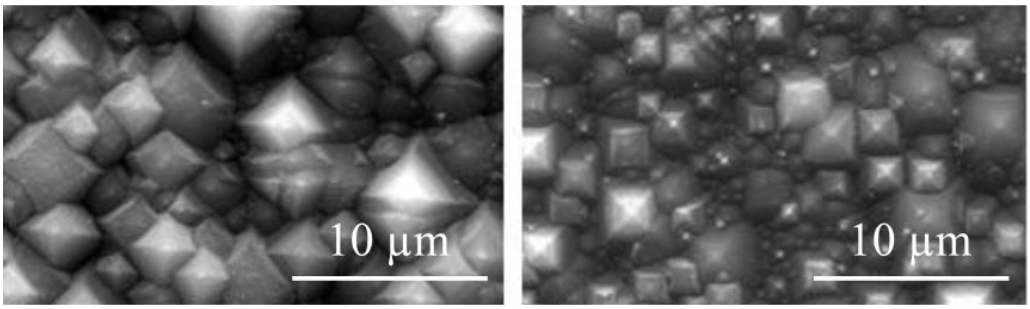


Figure 1.7 Top view of randomly textured surface obtained with pyramids after wet etching process

Random pyramids fabricated with wet etching technique on the order of several µm in size are standard for light-trapping in single crystalline silicon (c-Si) solar cells. SEM images of randomly formed pyramids on Si surface are shown on Figure 1.7. Thanks to anisotropic feature of alkaline based chemical solutions (mostly KOH based) these pyramids are created in a self- organized way. Random pyramids provide an excellent way of light trapping on thick mono-crystalline wafers [43]. However, they can't be formed on multi-crystalline wafers due to presence of different crystal domain which lifts the advantage of the anisotropic etching [43]. When we consider the optical function of the surface with pyramid formations, we see that light beam interacts with the surface more than once and thus the absorption increases as shown in Figure 1.8.

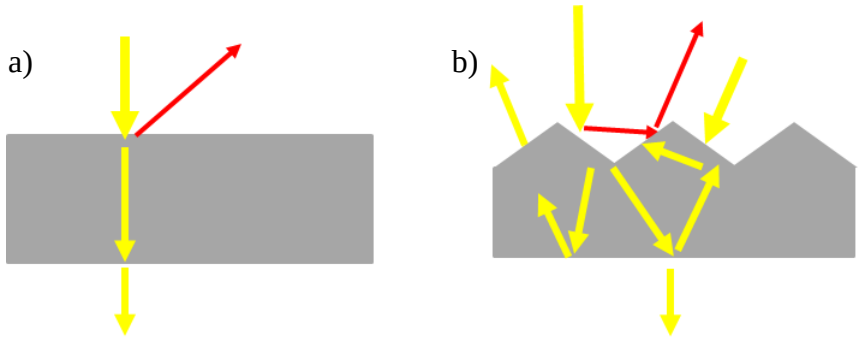


Figure 1.8 Schematic representation of a) bare, b) pyramid textured surfaces

In Figure 1.8, if the reflection coefficient of Si is R we expect to obtain an enhancement of the absorption of $(1-R^2I)/(1-RI)$ with random texturing. This enhancement obtained with pyramid texturing leads to a significant enhancement in the efficiency of the cells. Although this process is very cost-efficient, it cannot be applied to c-Si thin films or thin wafers since dimensions of the pyramid structures are comparable to the substrate thickness. For this reason, alternative methods for structuring the surface of the wafer have been studied for the thin Si wafers in recent years [29]. Many recent theoretical and numerical studies have been geared towards designing structures that can break Yablonovith (or Lambertian) limit [66] using nanostructures such as metal particles, nanorod/nanohole arrays and diffraction gratings [44,46]. Based on these studies on light-trapping characteristics, various structures like nanowires [67], nanocones [49] nanoholes [68], nanorods [69], pyramids [45], inverted pyramids [70], and plasmonic structures [52] have been fabricated and applied to solar cells. Some of these structures have been found to be useful to improve the c-Si solar cell performance [23].

According to thermodynamics of light, the intensity inside the textured material with index $n(x)$ in blackbody radiation (an opaque and non-reflective body) is larger than that of outside by the factor $n^2(x)$. The state of equilibrium between inbounding and outward-bounding radiation identifies the internal intensity.

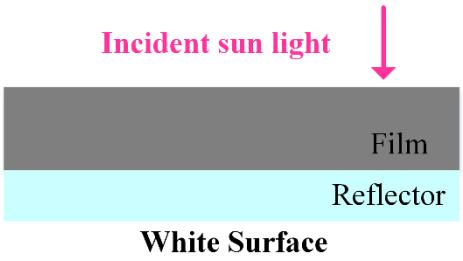


Figure 1.9 Schematic representation of a film with a white reflective back surface doubling the external intensity hence increasing the enhancement factor $2n^2$

Intensity enhancement factor of $2n^2$ gives rise to bulk absorption enhancement factor of $4n^2$, after taking into account the geometric factor, i.e. the light path enhancement represented schematically in Figure 1.9. The greatest possible value of

enhancement factor in c-Si cells for light trapping is $4n^2/Sin^2\theta \sim 50$ (Highest value for $Sin^2\theta = 1$, θ is the angle of emission cone that surrounds the cell) [6].

Parallel to theoretical studies, many experimental studies have been reported on using nanostructures for thin film PV cells [67]. C-Si nanowires, nanorods, and nanoholes etched into or grown onto Si have been tested as active layers. These cells have demonstrated generally improved performance compared to baseline PV cells, although they have seldom surpassed 15% in the solar to electrical energy conversion efficiency, much less than state-of-the-art bulk c-Si solar cells [71]. A more detailed analyses of light trapping phenomenon is given below.

1.4 Light-Matter Interaction

Light matter interaction varies depending on the size and the shape of textures. Figure 1.10 shows the light matter interaction depending on the size of the feature and light impinging on the surface.

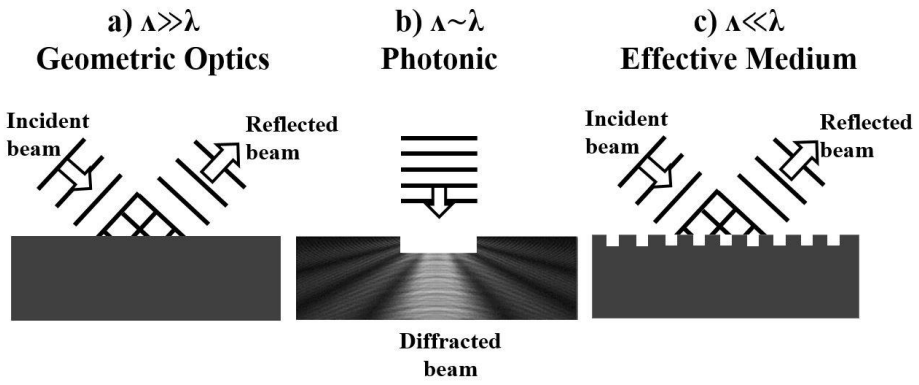


Figure 1.10 Schematic representation of the three different domains with respect to light matter interaction: a) when the feature size is larger, b) similar, c) smaller than the wavelength of the light impinging on them

When the size of the intended feature (Λ) is larger than the wave length (λ) geometrical ray optics apply [72]. When (Λ ≈ λ) wave optics/photonics apply which can be expressed by Thomas Young's famous double slit experiment. The basic expression of this experiment is diffraction/grating Equation 1.8:

$$d\left(sin\theta' + sin\theta^{i}\right) = m\lambda \tag{1.8}$$

d is the separation of the slit/grating elements, θ^{i} is the incident angle of the light, m is an intensity which is called diffraction modes at angles θ'.

Depending on the surface's periodicity (or randomness), if the dimensions of the patterns are the same, the optical properties will be the same. The schematic representation of surfaces textured with periodic and random holes is shown in Figure 1.11.

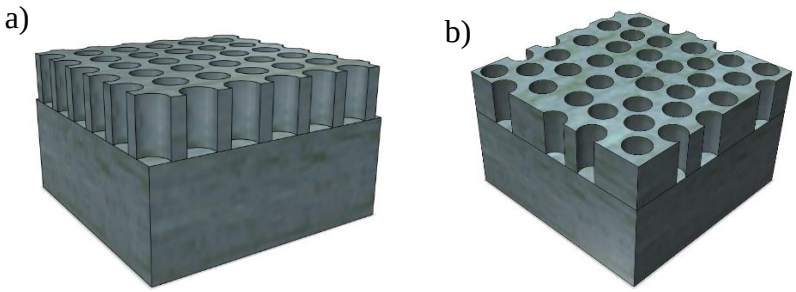


Figure 1.11 Schematic representation of a) periodic, b) random surfaces patterned with holes

For c-Si solar cells, the best way to increase energy conversion efficiency is decreasing the optical losses while considering electrical losses at the same time. This can be achieved in two ways, either light in-coupling or light trapping [59,73,74]. Increasing the amount of photons entering the photoactive layer will end up with better light in-coupling. The more the light can travel inside absorbing layer, the probability to get absorbed increases, resulting path length enhancement of light impinging and entering to the surface which is called light trapping.

When we evaluate the total optical light trapping performance of nano hole textures/nano pillars quantitatively the ultimate optical-electrical conversion capability η under the Air Mass 1.5 solar spectrum is calculated with Equation 1.9.

$$\eta = \frac{\int_{E_g}^{\infty} \frac{E_g \times I(E) \times \alpha(E)}{E} dE}{\int_{0}^{\infty} I(E) dE} \tag{1.9}$$

E_g: the bandgap energy for c-Si

E: the photon energy

$I(E)$: the solar energy density spectrum correspoding to the solar spectrum

$\alpha(E)$: absorption spectrum

For this calculation it is assumed that all photons having higher energy values than E_g, which are trapped by the absorption layer, would generate electron-hole pairs with the energy of E_g, and all generated carriers can be totally collected from contacts, with no recombination. In other words, this assumption tells us that the internal quantum efficiency is assumed to be 100% [12].

In order to evaluate and improve the performance of a solar cell, it is possible to use two important approaches for light trapping in a c-Si solar cell at weakly absorbed light. First one is absorption enhancement factor of Yablonovitch and Cody, who developed the theory of light trapping for conventional cells having thickness of many wavelengths [6]. Second one is near-bandgap optical path length factor Z_0 (multiple of cell thickness required to generate absorption equal to that found in the device) of Rand and Basore [4]. In Rand and Basore's model, they neglect a term including cell thickness and absorption coefficient. With a new expression for optical path length factor, more reliable and realistic calculations could be done [13].

1.5 Experimental Approaches

Structuring the surface of Si has attracted a lot of attention due to the increased importance in PV technology. There have been various experimental techniques to fabricate random or periodic structures on Si wafer surface [20,22,23,25]. These techniques can be classified as top-down and bottom-up approaches [35]. In the case of top-down production methods, an etching process is used to define the intended structure on the surface [75]. The bottom-up approaches, the light trapping structure is grown on the Si wafer using physical or chemical crystal growth techniques [76]. Mostly, a lithography step with an appropriate mask, which is not desirable for the ultimate commercial manufacturing, has been employed for the proof of concept [55]. As the size, and the shape get more complex, the processes become more difficult and complicated.

Fabrication techniques with top-down approaches to obtain micro and nanostructures can be accomplished using the techniques listed in Table 1.1:

Table 1.1 Fabrication techniques with top-down approaches to obtain micro and nanostructures

Method	Lithography
Template-assisted fabrication [22]	To obtain master template +
Focused ion beam milling [77]	Uniform structures +
Metal assisted etching [78]	Random - /periodic texturing +
Reactive ion etching [79]	+

(+: applied, -: not applied)

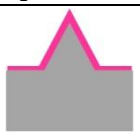
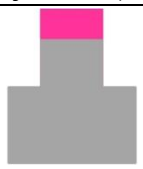
During pattern transfer, optical, nanosphere, nanoimprint (NIL), hole-colloidal lithography techniques can be used [32,33,70]. Depending on the lithography tool and mask maker's dimension criteria, one of these techniques can be selected. Also bottom-up approaches can be preferred to make surface texturing and/or deposit layers.

1.6 Why Hole Texturing?

The aim of surface texturing is to increase the absorption of light in photoactive material. Many different structures have been proposed and experimented to test their effect on the performance of thick and thin solar cells [23,40,44]. Texturing surface with holes boasts a superior solar cell results when compared with other texturing types as shown in Table 1.2 [27]. The results summarized in Table 1.2 are obtained via simulation confirmed by experimental studies with the best optimized process conditions for each type of surface texturing (Results that were shown with "*" were obtained via experiments. Optimizations include doping, dimension of features, antireflection coating, material selection for contacts and buried top contact [27].

Since this thesis is based on texturing with holes having different dimensions, we made a comparison between holes and pillars. It is possible to obtain pillars with the same mask by changing the type of the resist. A comparison between hole textures and micro pillar based structures was given in Figure 1.12 and Figure 1.13. As discussed in many papers in detail, hole based structures is more promising than micro pillar structures. It is also shown that the very high efficiency values are possible with these approaches [23,40].

Table 1.2 Comparison of the performance between radial-junction SiNH and the other types of textured solar cells [27]

Schematic of single unit	Jsc (mA/cm2)	Voc (V)	η (%)	FF (%)
 SiNH- radial-junc	66.6	0.56	27.8	74.6
 Si planar cell	~ 35	~ 0.6	~ 18	_
 *Si pyramidal cell (upright)	36.9	0.60	16.7	75.2
 *Si pyramidal cell (inverted)	40.9	0.71	24.0	82.7
 Si nanocone (SiNC)	_	_	~22.5	_
 Si nanowire (SiNW) (subsurface-junction)	_	_	~27	_
 SiNW (planar- junction)	_	_	~17.5	_
 SiNW (radial- junction)	~ 43	~ 0.52	~17	_

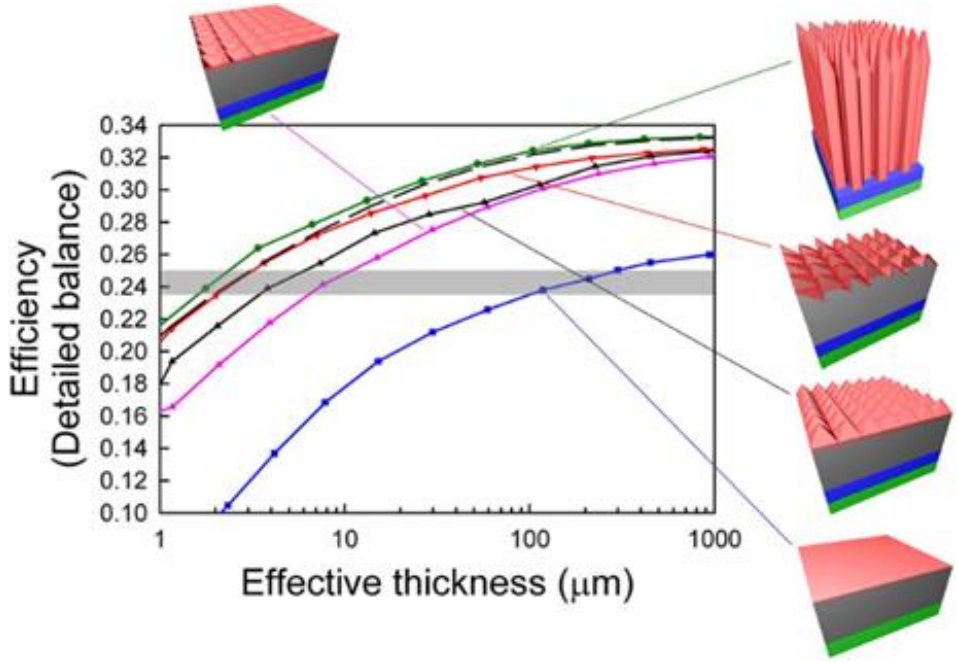


Figure 1.12 Efficiency values of thin film solar cells with different surface textures
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In Figure 1.12, it is depicted that 10 μm thick cell with correct light trapping techniques can reach the efficiency value of a thick cell which is around 200-300 μm [23].

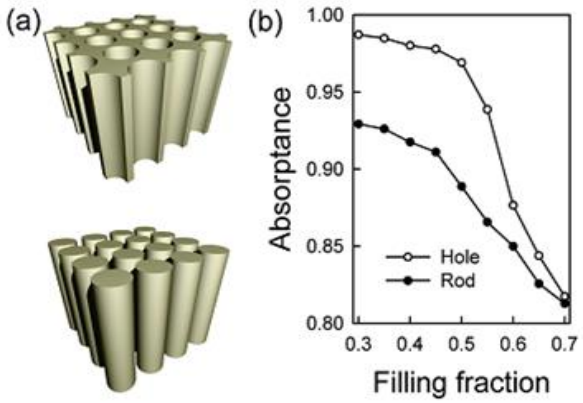

Figure 1.13 (a) Schematic representation of nanorod and nanohole textures, (b) absorption spectrum of these structures according to their filling fraction ratios
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It can be seen that hole texturing is a very promising candidate for efficient solar cell fabrication. In this thesis we have focused on the micro and nano hole structures fabricated using different pattern transfer and etching techniques such as nanoimprint lithography, RIE, MAE.

1.7 Periodic and Random Surface Structures for Light Trapping, Can Periodic Beat Random?

The introduction of light trapping was first announced by Redfield in 1974, since then many alternative ways of textures have been proposed [21]. The aim of light trapping is to enhance absorption, increase light matter interaction, and keep light inside active absorber layer resulting higher energy conversion efficiencies. As described above, standard solar cell fabrication is based on random pyramid texturing, antireflection coating (ARC) and metallic back reflector [2,4]. However, many recent studies including this thesis work focus on the periodic surface texturing [12,15,80]. When the surface is patterned with random textures, an infinite number of diffraction orders is theoretically expected. Since light can scatter into only a few diffraction orders from a grating, absorption is dominantly enhanced around the resonant wavelengths. Yielding the selectivity of a grating structure means that a more broadband absorption improvement is expected. As seen in Figure 1.10, when the size of the texture is comparable with the wavelength, the surface will act as a photonic structure. Depending on the shape, light's penetration depth will vary. It is possible to obtain more broadband absorption with respect to the periodicity. Discussions on the effectiveness of periodic structures compared to random ones are still going on. It is clear that well designed and optimized periodic structures can overperform the random structures in terms of optical performance due to the fact that light can move through the sample only a few diffraction orders [23]. However, major drawback of periodic structures is the lack of compatibility with the industrial production. A record of 25% efficiency value with periodic inverted pyramid texturing was achieved [71]. Moreover, an efficiency of 25 % was also achieved in heterojunction solar cell cells with random texturing [71]. So, while there are success stories on both sides, it seems that the efficiency race between these two approaches will continue for a while.

1.8 Thesis Organization

In this thesis, we present the results of our investigation on micro and nano hole textured surfaces on crystalline silicon wafer and their applications to solar cells.

In Chapter 1, a short introduction to solar cell, its working principle and optical processes on the cell surface with emphasis on light trapping are given. The comparison of periodic and random texturing results investigated in literature is presented.

Chapter 2 deals with surface patterning techniques followed by either wet chemical, or dry plasma etching. Metal assisted etching (MAE) and reactive ion etching (RIE) conditions are described. Optimized process parameters for a variety number of different hole and pitch sizes let us obtain different hole ratio on top of the surface, hence different optical and electrical properties.

High resolution project systems with stepper property allowed us to create submicron level of holes with desired distribution. Nanoimprint lithography (NIL) and hole colloidal lithography (HCL) techniques were used to create different surface topographies

Periodic micro and nano holes' physical and optical properties are explained in detail. For each technique possible fabrication problems could be eliminated successfully. NIL and HCL studies were conducted at IMEC under EU funded project PhotoNVoltaics.

Chapter 3 includes simulation results of hole-textured surfaces obtained by using SILVACO programme in collaboration with Prof. Dragica Vasileska from Arizona State University.

In Chapter 4, results of electrical characterization of solar cells having micro and nano holes are presented and discussed. The effects of hole diameter, pitch size, hole fraction, total surface area and hole depth are discussed.

In Chapter 5, in order to obtain better light trapping effect we made analyses with different angles. As expected the surface textured with holes had significant dependence on the angle of incidence beam. Each diameter and depth had a unique angle which gave the highest cell efficiency value.

In Chapter 6, a summary and conclusion are given and the perspectives are discussed.

CHAPTER 2

PATTERNING SI SURFACE FOR LIGHT MANAGEMENT

In order to reduce module cost and increase the efficiency of a solar cell, patterning c-Si surface is an indispensable part of solar cell technology. Texturisation of the surface can be done either by top down, or bottom up approaches. In this thesis we focused on four top down approaches: reactive ion etching (RIE) [81], metal assisted etching (MAE) [82], nanoimprint lithography (NIL) [83] and hole-colloidal lithography (HCL) [84]. Surface texturing with desired shapes could be successfully achieved with both techniques.

2.1 Patterning Si Surface by Photolithography

In order to obtain a periodic and uniform distribution of structures with specific geometries, pattern transfer is needed. The basic tool to manage pattern transfer is photolithography. After creating the patterns with desired geometries on transparent plate called mask, we can transfer them to a flat surface via optical printing process. During this printing process a photosensitive polymer, which is called as photoresist, is used to create desired pattern on the surface. When the resist is exposed to UV light, depending on being negative or positive, either the exposed part or unexposed part of the resist is dissolved in a chemical solution called developer [35].

Prior to photolithography whose process steps are shortly described in Figure 2.1, Si wafer is first cleaned using the chemical cleaning process called RCA cleaning. RCA1 is to remove organic contaminants with a solution of NH_4OH: H_2O_2: H_2O with ratio of 1:1:5. RCA2 is used to remove the metallic contaminations, with a HCl: H_2O_2: H_2O solution of ratio 1:1:7. Both cleaning steps are done at 75- 85 °C for approximately 20 min. Sometimes RCA1 could be replaced with H_2SO_4: H_2O_2 (1:1) solution at 150 °C, which is called piranha cleaning. After cleaning, wafers are kept inside an oven at temperatures above 100 °C for around 30 min in order to dehydrate the surface for a good photoresist adhesion. Photoresist is then coated onto surface by

spinning. The thickness of the resist should be as uniform as possible across the wafer. After exposing the sample to UV light through the mask, samples are dipped into the developer to obtain the desired pattern on the surface [35].

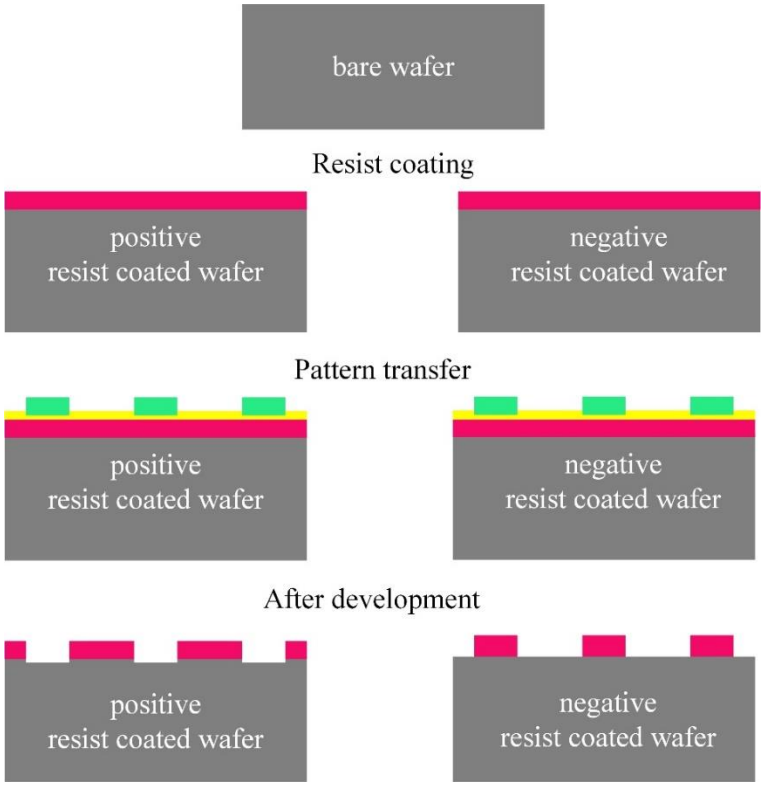


Figure 2.1 Process steps and final pattern that will be obtained at the end of photolithography using positive and negative resists

2.2 Surface Structures Generated by Reactive Ion Etching and Limits

Reactive ion etching (RIE) is a dry etching process used for selective etching of Si surface. It is a reliable technique to pattern the surface of Si which is extensively used by MEMS technology to create three dimensional structures on Si surface. The use of RIE is increasing in the PV industry. Recently, many different research groups have focused on the surface texturing by RIE [27,77]. Main benefits are very low reflection losses, the possibility of single-side texturing, reduced material loss, and reduction of chemical waste. In Figure 2.2 dry plasma etching sequence can be seen.

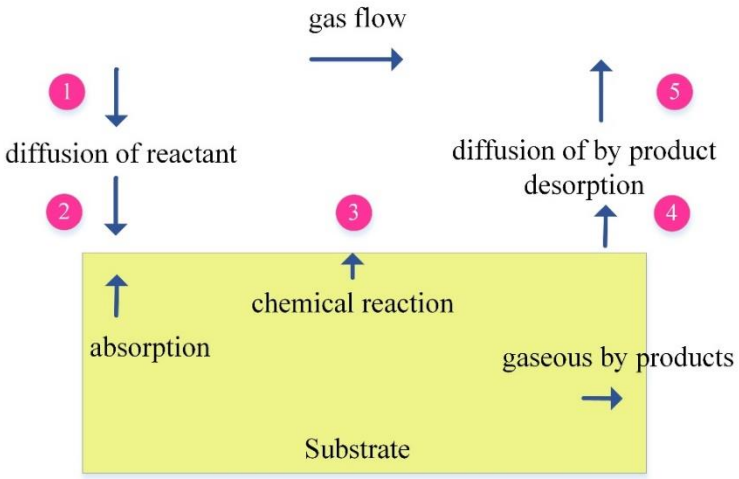


Figure 2.2 RIE Etching sequence

RIE provides very uniform surface patterns [35]. Depending on the mask pattern, desired topography can be obtained on the wafer surface. Figure 2.3 shows the schematics of rod and hole structures that can be obtained using the same mask pattern with positive and negative photoresist. Using advanced lithography techniques, we were able to obtain features with micron and submicron dimensions.

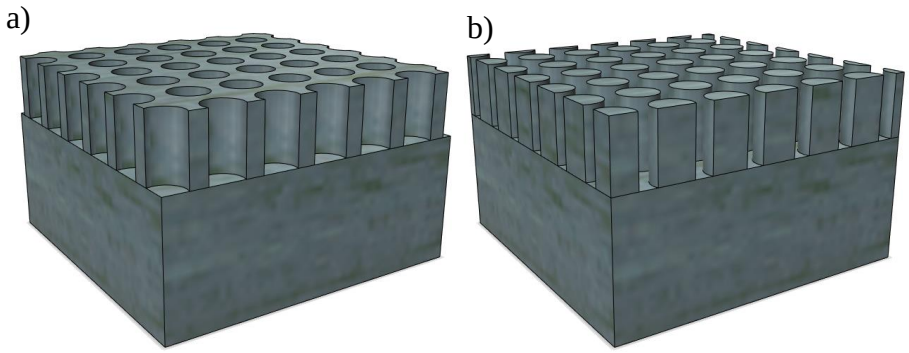


Figure 2.3 Schematic representation of RIE applied surfaces coated with a) positive and b) negative resist using the same mask and same sequence of lithography process

Simulation studies published in recent years have shown that the hole based surface is more promising than rod like structures in the PV cell performance [23]. For this reason we have focused on the analysis of micro and nano-sized hole structures and their applications to c-Si solar cells. We also looked at the effect of third

dimension, i.e., the depth of the holes, and thus the hole filling ratio on the cell performance.

RIE etching is the most promising and industrially applicable technique to make holes on the surface. A huge amount of experience has already been accumulated in MEMS technology. However, it needs to be optimized carefully as any parameter can affect the effectiveness of RIE process. Some of the process parameters could be named as; RF power level, chuck temperature, frequency, plasma composition, gas flow rates and pressure. For etching Si, CF_4 gas is used and the reactions are shown in below take place during the RIE process;

$$CF_4 \rightarrow F^* + CF_3 \tag{2.1}$$

$$CF_4 + e \Leftrightarrow CF_3 + F^* + 2e \tag{2.2}$$

$$Si + 4F^* \rightarrow SiF_4 \uparrow \tag{2.3}$$

where F^* are Fluorine atoms with electrons.

Following the chemical reactions; SiF_4 is formed which can be easily desorbed and get in gaseous form to leave the process chamber as by product. Meanwhile there is bombardment of high-energy particles resulting from DC bias [35].

Periodic patterning requires a pattern transfer step which is done with lithography process as mentioned in section 2.1. For pattern transfer we have designed a lithography mask to fabricate periodical hole arrays on Si wafer. The mask is designed to have different hole diameters and pitch (gap between holes+ diameter) sizes. Details of the dimension of photolithography mask are given in Figure 2.4. Hole dimensions and distance between the holes (gap) defined by the mask is given in Table 2.1. Vertical dimensions (depth of the holes) is defined by the duration of etching process.

Table 2.1 Dimensional constants for front surface contact mask design

Distance between square regions	2 mm
Square region dimensions	2 cm x 2 cm
Number of fingers in each square region	8
Width of finger region in each squares	200 µm

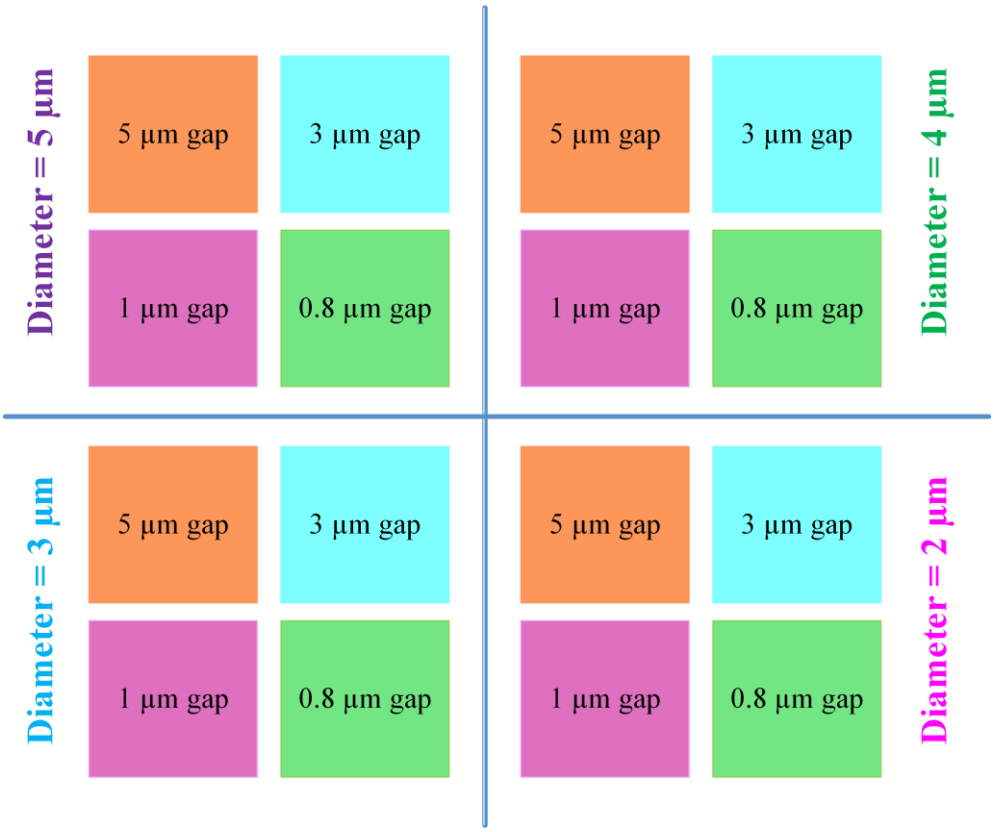


Figure 2.4 Hole dimensions and gap sizes on the photolithography mask used in this study

As shown in Figure 2.4, for optical lithography 16 different structures have been designed with L-edit programme. The spaces defined for hole textures and front contacts have been arranged in such a way that one contact mask was used for creating metal contacts. The schematic representation of textured front surface before and after metallization is shown in Figure 2.5.

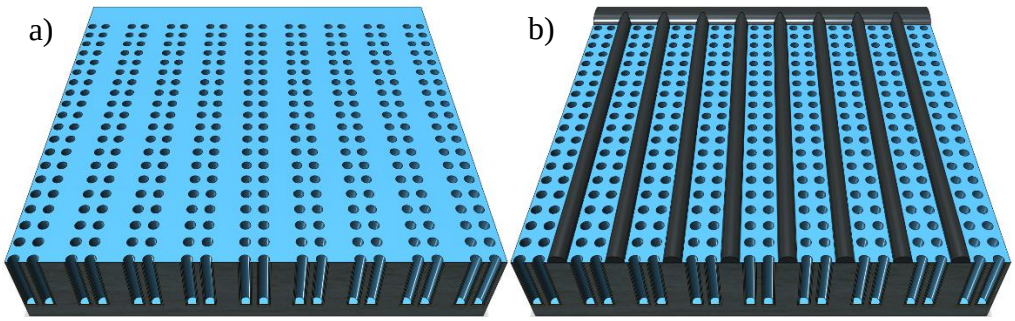


Figure 2.5 All 2 cm × 2 cm squares have 9 rectangles (2045 µm × 20000 µm), and 8 fingers (200 µm × 20000 µm) a) Before metallization b) After metallization

Metal contacts are designed to touch the flat region outside the hole structured region. Diameter and the gap between holes may not exactly be the same as defined sizes of the mask depending on illumination uniformity and development quality of lithography, but with optimization of pattern transfer we could manage to obtain exactly the same dimensions with the masks.

During pattern transfer there are some critical points that can end up with undesired results. Equation 2.4 and 2.5 represent two essential components which restrict an optical instrument: the wavelength, λ, of the illuminating light and the numerical aperture, NA, of the imaging optics. For a given wavelength, resolution is improved by increasing the numerical aperture [78]. The relationships between resolution (RES), depth of focus (DOF) and NA of the camera are given by Equation 2.4 and 2.5.

$$RES = \frac{k_1 \lambda}{NA} \tag{2.4}$$

and

$$DOF = \frac{k_2 \lambda}{(NA)^2} \tag{2.5}$$

When there is a change in λ downward, this will cause an increase in NA. k_1 and k_2 are empirically determined according to the critical dimension of designed

pattern. When these k_1 and k_2 are taken as 0.5, according to Rayleigh Criteria, it corresponds to theoretical values [79,82].

As the technology goes far beyond the expectations, with the help of extended capability of optical lithography, it is becoming possible to go smaller dimensions. Optical lithography with stepper function is a very nice representation of extended capability. In this work we have used Karl SUSS MA 56 aligner with a resolution value smaller than 0.35 µm. For stepper once the pattern is created, it can be duplicated as many times as desired. Schematics of a stepper is shown in Figure 2.6.

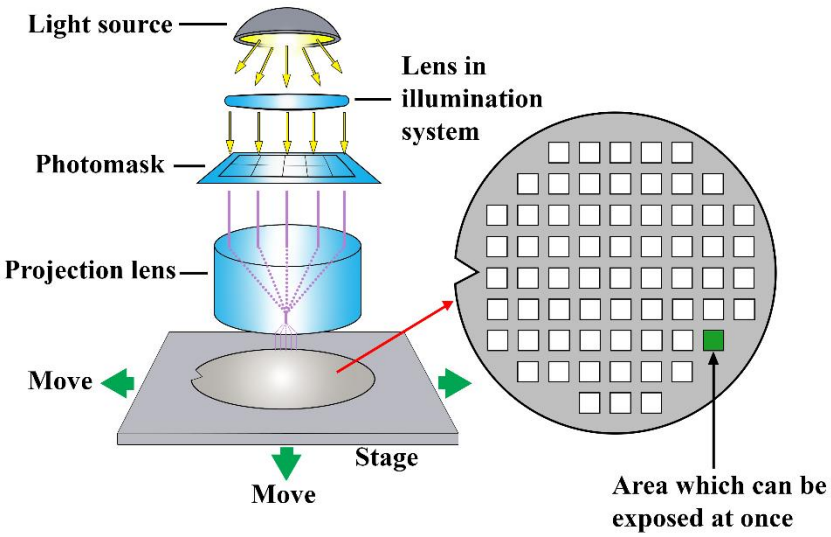


Figure 2.6 Schematic of a basic stepper tool and its components allowing us to place the designed geometry to any part of the wafer surface

As represented in Figure 2.1, the pattern on the mask (or just reciprocal pattern depending on resist type) can be transferred to wafer surface as many as desired both in vertical and horizontal axes.

Stepper aligner lets us work with 6" wafers and make patterns all over the wafer with step and repeat action. With this technique, holes (and/or any other patterns defined on mask) with submicron sizes could be fabricated. Unlike optical lithography, for stepper there is no need for exact pattern definition on the mask, only the unit cell of the pattern which can be duplicated will be enough. The dimensions also can be

altered with the wavelength of the light source depicted in system representation in Figure 2.6 [85]. For our textures with submicron level, we designed unit cells with different diameters and the map of the pattern is shown in Figure 2.7 below. The patterns can be transferred to any part of 6" wafer as many as desired.

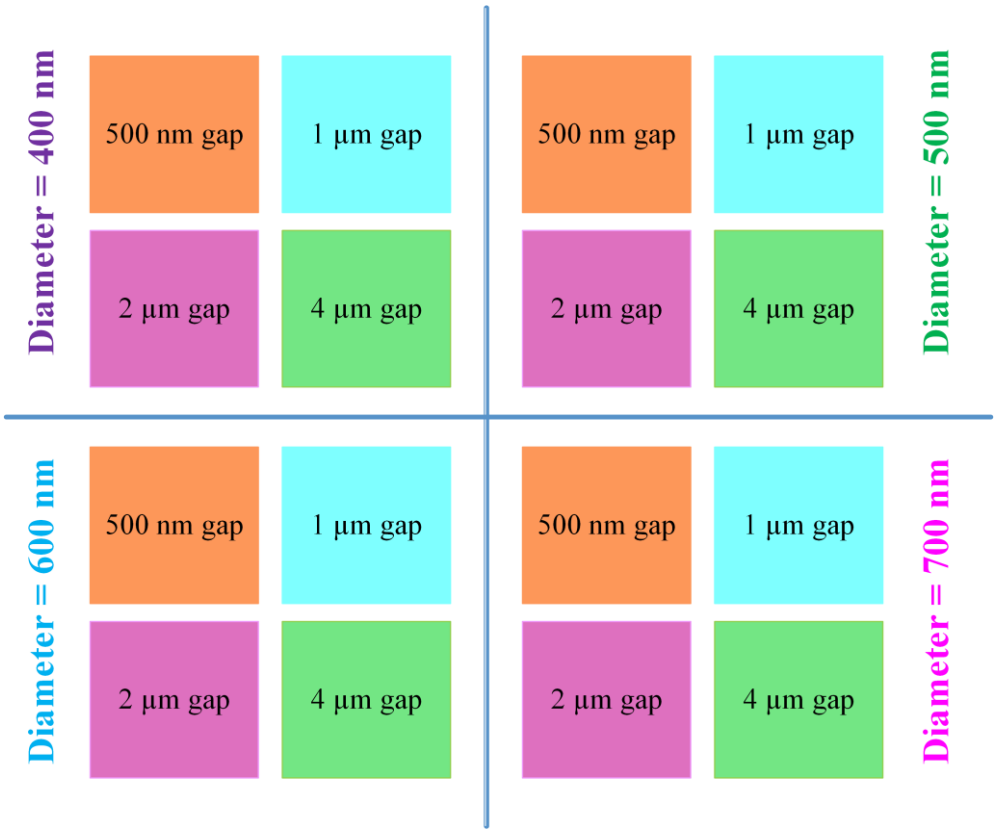


Figure 2.7 Designed mask including holes with diameters 400 nm, 500 nm, 600 nm, and 700 nm. The gaps between holes were 500 nm, 1 µm, 2 µm, and 4 µm

Following several optimization trials on dummy wafers, the images on the mask were successfully transferred. An example after photoresist development taken with microscope is shown in Figure 2.8.

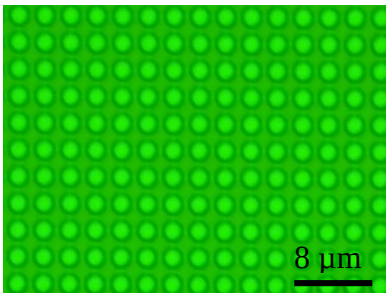


Figure 2.8 Microscope image of the structure having 2 µm diameter and 0.8 µm gap obtained after 2.5 s exposure

Checking surface after pattern transfer and development step gives us an idea about future steps. If there were an intersection between two holes as a result of overdevelopment, etching step will proceed with wrong initial parameters which will definitely end up with different morphologies rather than uniform holes.

2.2.1 Basics of Experimental Procedures

Firstly, in order to remove possible particles from the wafer surface, dehydration prebake process was conducted in a microprosessor oven at 110 °C for 10 min. After dehydration, S1805 positive photoresist was used for thin coating at 4000 rpm, followed by a soft bake at 115 °C for 1 min. After these cleaning and resist coating processes the wafer was ready for being processed in contact aligner EVG-620. Depending on wafer size, the system is prepared with necessary components. After photolithography step, dry plasma etching parameters should be defined according to the surface morphology. The size of the features, property of the resist or coated material are the important parameters to be defined for an efficient process.

We have used STS Multiplex RIE system for our dry plasma etching process. The system can etch silicon dioxide (SiO_2), silicon nitride (Si_3N_4), aluminum (Al), benzocyclobutene (BCB), polyimide (PI) with desired depths. It is also possible to etch non-plasma Si, based on Xenon Difluoride (XeF_2) gas.

During dry plasma etching process there are both physical and chemical reactions [35,77]. The process will start with SF_6 and O_2 etching, after the first step etched side wall will be protected. If previously etched surface were not protected, surface topography would end up with conical shape, rather than intended vertical deep structures. For etching cycle we have used 200 sccm SF_6 within STX Multiplex RIE

system. For side wall protection deposition of C_4F_8 with 2.5 mTorr was applied for the initial 1.5 s period of process. Untill the end of the dry plasma etching process duration, the ratio was set to 375 sccm depending on the depth of desired feature. After first 1.5 s, 35 sccm O_2 flow was initiated. Both for deposition, plasma formation, and etching sequence platen RF power of coil was set at 2200 watt. RF generator initiated with 45 Watt and finished with 35 Watt with platen power pulse. Duty cycle was 70%, 19.8 ms. Chuck temperature was +10 °C. Each cycle parameters were defined according to defined texture specifications. For deeper structures process time was kept longer when compared with shallower structures.

At the end of dry plasma etching process, we used inductively coupled plasma (ICP) to get rid of resist residues. ICP is one of the conformal cleaning technique, but this process should be carried out cautiously, not to give undesired and unexpected damages to surface. Side walls which are coated with polymerized resist during RIE process are stripped with ICP at the end of the process [86,87]. Considering our surface's physical and chemical specifications, we defined ICP conditions which finished up with resist-free surfaces. Figure 2.9 shows the image of the surface textured with RIE and cleaned with ICP.

Figure 2.9 The picture of the wafer taken after, 80 s dry etching and 30 min ICP

2.2.2 Surface Analyses of RIE Textured Structures

In this section, examples of various structures formed by RIE process are presented. The ultimate goal of this study is to understand the applicability of hole strcutures to crystalline Si solar cell technology and its advantage over other texturing

schemes. We also want to figure out the limits of RIE and other lithography techniques in patterning the surface of Si wafer. Table 2.3 shows the collection of different samples having hole diameters in between 0.8-5 μm, and pitch size in the 1.6-10 μm interval. These samples were exposed to RIE process for 160 s. We observed some differences between intended structures defined on the lithography mask and the actual patterned realized on the wafer. For example for the hole diameter of 2 μm, the actual structure ended up with a diameter of 2.198 μm, which about 10% larger than intended structure. Table 2.2 shows these differences between intended and realized structure. These variations are related to lack of detailed optimization of lithography and etching process for the structures having different diameter and pitch sizes patterned on the same mask. However, obtained dimensions are acceptable with respect to designed geometries and do not cause any problems in reaching conclusive results.

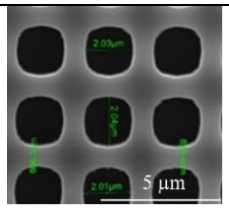
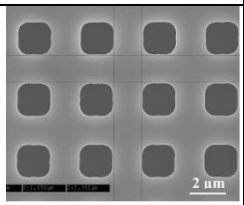
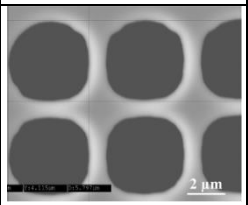
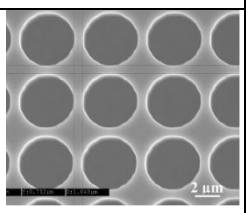
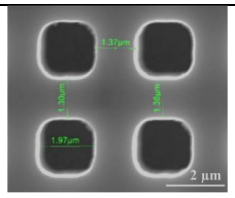
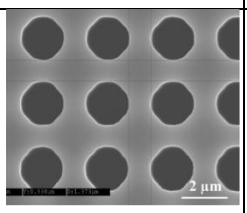
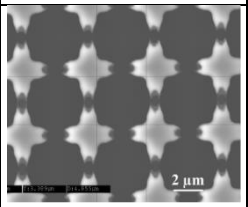
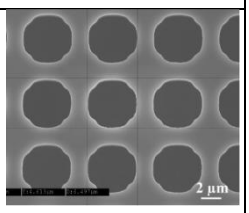
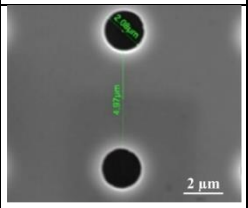
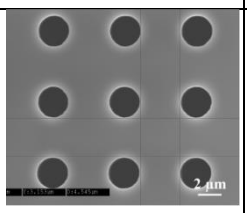
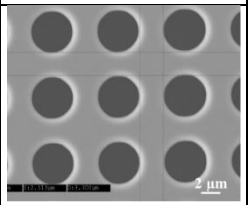
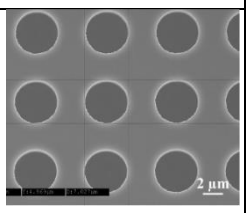
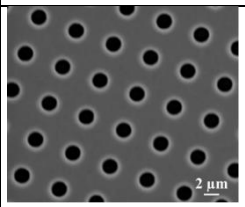
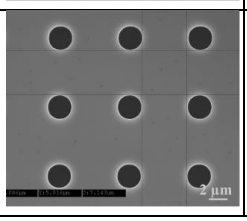
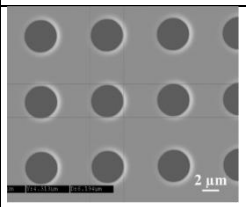
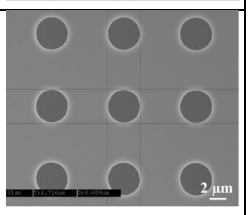
Table 2.2 Dimensions of sample patterned with 2 μm diameter and 1 μm gap

Dia: 2 x Gap: 1	Diameter (μm)	Gap between holes (μm)	Exposure time (s)	Develop time (s)
	2.29	1.45	2	50
	2.006	1.003	1.5	40
	2.053	0.909	1.5	40

For the holes having 2 μm diameter, the final diameters were changing between 2.112 μm and 2.087 μm. The gap between the holes was 0.8 μm and we measured this length as 1.675 and 1.650 μm. The diameter of the holes was smaller and the gap between them was much larger than what we expected. Holes, in fact rectangles, needed some more time for being developed to give correct sizes. For 3 μm diameter, we measured values varying between 2.910 and 2.842 μm. The gap between the holes was expected to be 3 μm and we measured this length as 3.27 and 3.15 μm for this sample. Here we could see that the period was 6 μm, which we desired, but gap between holes was aimed to be smaller and diameter to be larger. We were expecting the diameter of the holes to be 3 μm, and here the diameter was 2.93 μm. The gap between the holes was expected to be 5 μm and we measured this length as 5.08 and

5.01 µm for this sample. Some values were promising, and the ones that were larger or smaller than what we expected could be corrected with process optimizations.

Table 2.3 SEM images of samples having different diameter and gap

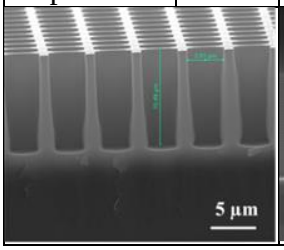
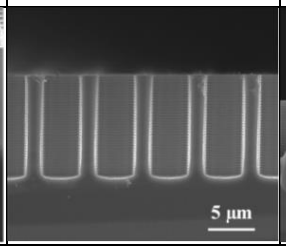
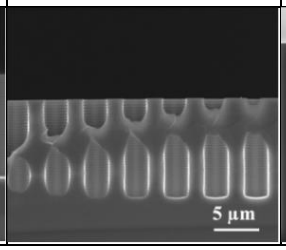
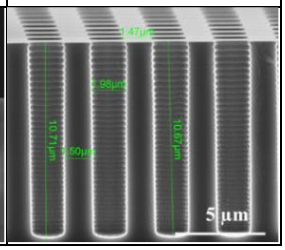
Dia / Gap	2	3	4	5
0.8				
1				
3				
5				

Wafer including 4 µm diameter holes and distances varying from 0.8 to 5 µm. The wafer was exposed to UV light for 2.5 s and developed for 38+22 s. As shown in Table 2.3, holes were close to square shape and seem to be connected to each other. The structures with these sizes couldn't be obtained as desired. SEM image of 4 µm diameter and 1 µm gap tells us the sizes of the real structure to be close to the size of our mask. We were expecting the diameter of the hole to be 4 µm, and here the diameters are changing between 4.083 and 4.115 µm. The gap between the holes was 0.8 µm and we measured this length as 0.896 and 0.875 µm. For 4 µm diameter and 3 µm gap, SEM image shows us the sizes of the real structure to be close to the size of

our mask. We were expecting the diameter of the hole to be 4 µm, and here the diameters are changing between 4.313 and 4.354 µm. The gap between the holes was 3 µm and we measured this length as 2.354 and 2.313 µm. The diameter of the holes was bigger and the gap between them was smaller than we expected. First we tried to look at the structures on the wafers without breaking them, but the depth was much bigger than the tangent of the tilt angle, for this reason the best view of the depth could be obtained after breaking the wafers and seeing the cross section of the structure. For 4 µm diameter and 5 µm gap it was obtained that the sizes of the real structure to be close to the size of our mask. For defined process sequence up to this point we could observe that, the greater the pitch size, less complicated to make patterning and etching.

The third dimension, i.e., the depth of the holes were varied by the etch time during the RIE process. The cross-sectional view of a typical hole structure is shown in Table 2.4 Here we see that well defined and vertically aligned structures can be formed. Even though the distance between two holes is very small (less than 1 µm), very high aspect ratio can be obtained. The periodic topographic features seen on the inner walls of the holes are due to the trench etching techniques used in the RIE method.

Table 2.4 Cross sectional SEM images of samples having 1 µm gap between holes, and diameter 5, 4, 3, 2 µm

Diameter	3.94	4.95	3.05	1.98
Depth	10.49	12.45	10.85	10.71
				

In order to analyze the fabricated solar cells better, a parameter called hole fraction is defined. It is the ratio of hole volume to the total volume of the wafer which is expressed in Equation 2.6.

$$\frac{\#\ of\ holes\ \times Vhole}{Vtotal}$$
$$Vhole = \pi r^2 h \tag{2.6}$$
$$Vtotal = 2 \times 2 \times thickness$$

The hole fraction of the samples we prepared in this study is displayed in Figure 2.10. We see that we cover a wide range of different hole fraction values between 5% and 60%.

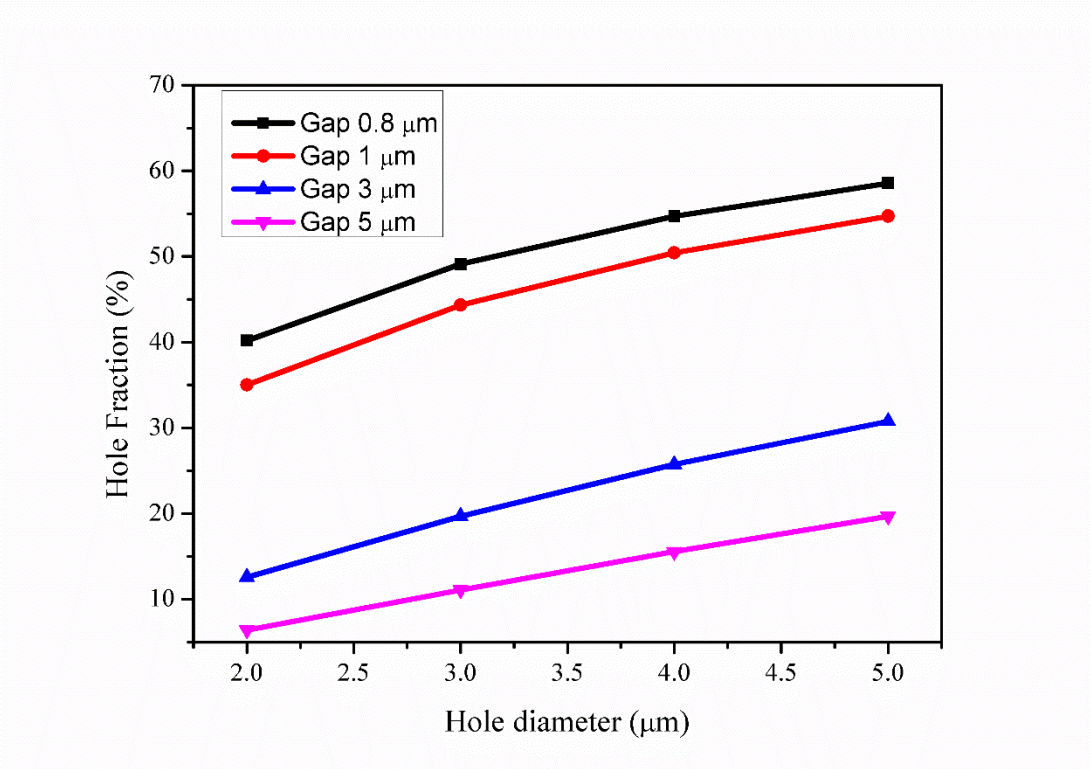
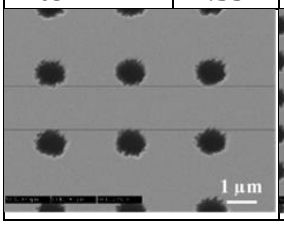
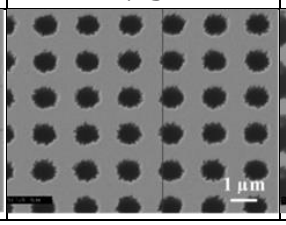
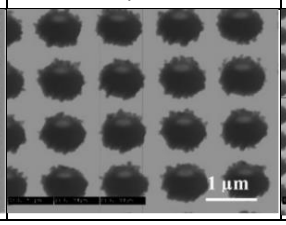
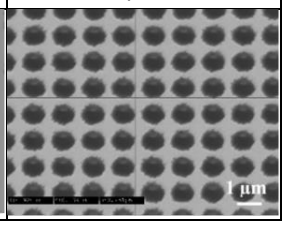


Figure 2.10 Hole diameter versus hole fraction graph for holes patterned with contact aligner

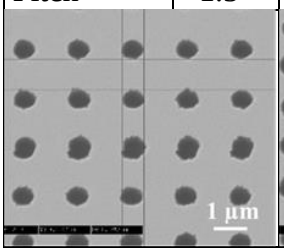
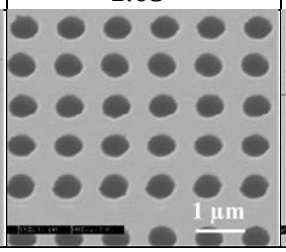
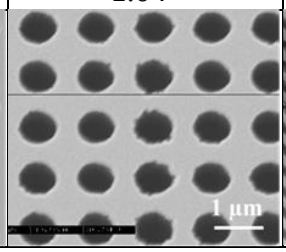
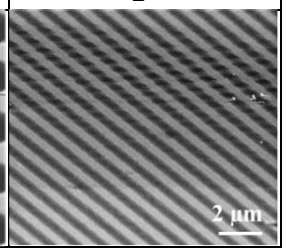
SEM images shown in Table 2.5 show us examples of hole structures obtained with RIE, including the limiting cases where nanoscale dimensions can be as low as 230 nm and 400 nm respectively. These dimensions are hardly possible to be reached with standard lithography equipment.

Table 2.5 Top view SEM images of textures obtained with stepper having diameter values between 0.63 µm and 0.93 µm

Diameter	0.93	0.78	0.63	0.92
Pitch	2.39	1.43	1.21	1.11
				

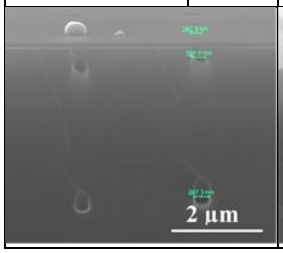
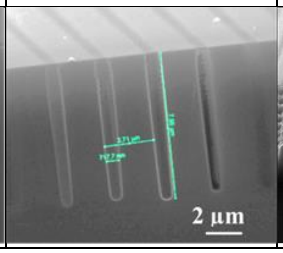
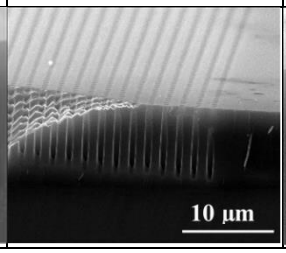
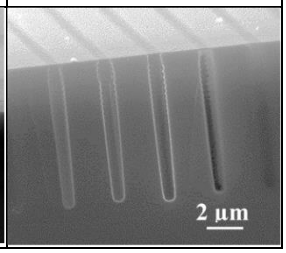
The uniformity on the surface was checked with SEM analyses obtained from different points of the surface, with maximum 10% of deviation of the dimensions we could manage to obtain desired specifications. Table 2.6 represents holes with diameter 0.6 and 0.7 µm.

Table 2.6 Top view SEM images of textures obtained with stepper having diameter values between 0.55 µm and 0.71 µm

Diameter	0.62	0.71	0.64	0.55
Pitch	1.5	1.05	1.04	1
				

As the diameter of the hole gets smaller, the process gets more complicated and difficult. One of the smallest diameters we obtained was 0.25 µm. Table 2.7 shows holes obtained with stepper and ended up with high aspect ratios.

Table 2.7 Cross sectional SEM images of textures obtained with stepper having diameter values between 0.25 µm and 0.71 µm

Diameter	0.25	0.71	0.63	0.71
Pitch	2.85	3.42	1.63	2.71
				

2.2.3 Optical Properties of Micro and Nano-Structured Surfaces by RIE

Crystalline Si is a poor absorber in the long wavelength region due to the indirect band gap structure. For this reason, we need to use thick wafer to ensure an absorption of full spectrum [2,5]. The absorption spectrum and corresponding penetration depth is shown in

Figure 2.11. We see that the thickness of the wafer is around 100 µm for a complete absorption in the infrared region. This is one of the reason for the high material cost in c-Si based PV systems.

As discussed above, the use of thin Si wafer is desirable to lower the material cost. With an efficient light trapping structure incorporated to the surface, a physically thin wafer can be made a good absorber which is said to be “optically thick”. This is possible through an appropriate texturing process.

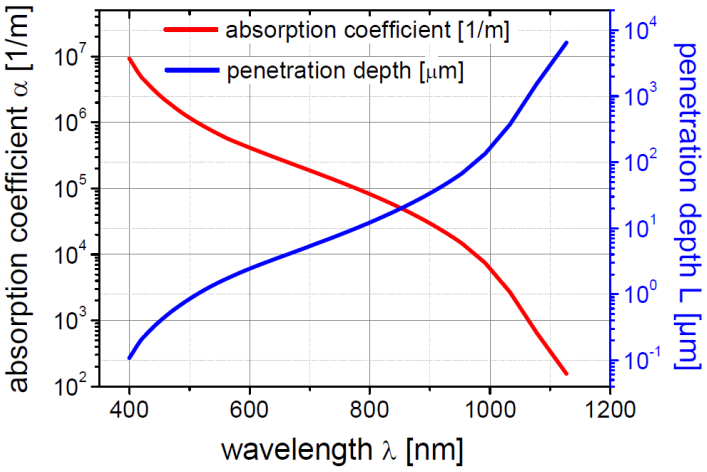


Figure 2.11 Absorption coefficient and penetration depth spectra of c-Si obtained from spectroscopic ellipsometer measurements in the 300–1000 nm wavelength range at 65°, 70°, and 75° angles of incidence

The uniform distribution of hole patterns incorporated onto the surface of Si can act as a medium with good light trapping properties [23]. In order to test this feature, we have measured the reflection of the surface patterned with different hole diameter, pitch size and depth.Figure 2.12 a) shows the reflection results of surface patterned with 4 µm diameter and 0.8 µm gap between holes having three different etching times. The longer the dry plasma etching duration is, the deeper the structures is, hence increasing optical path and ending up with lower reflection values [5]. Figure 2.12 b) shows the reflection spectra of samples with 4 µm diameter and 5 µm gap. The reflection data for the bare Si wafer and pyramid textured Si are both displayed for comparison. When we investigated these surface features by means of hole density, holes with smaller gaps will end up with surfaces having more number of holes compared to surfaces with larger gap between holes. The larger the gap values, the closer the surface profile to bare silicon surface, having reflection value close to bare silicon.

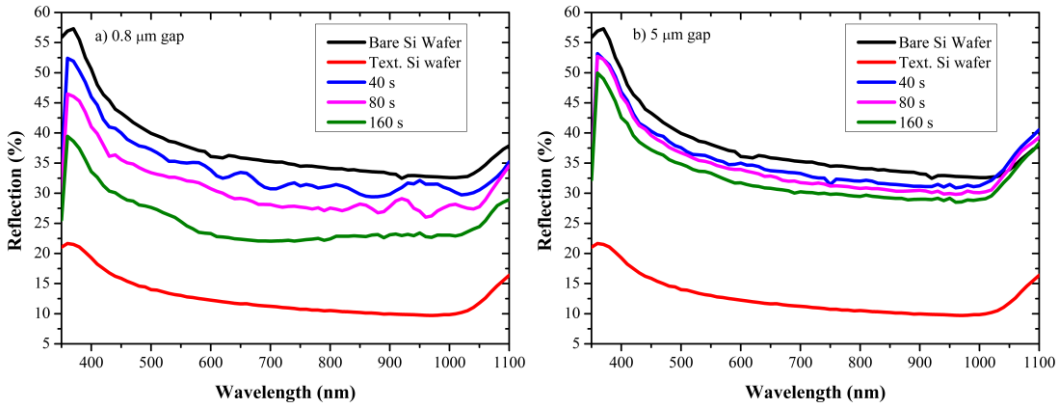


Figure 2.12 Reflection measurement comparison of surfaces textured with holes having 4 µm diameter, a) 0.8 µm and b) 5 µm gap dry etched for 40, 80, 160 s

While making optical comparisons we had three parameters namely; diameter, the gap between holes and dry plasma etching time to see the individual effects on reflection. In addition to making comparisons for constant diameter, we kept the gap constant and observed the effect of changing diameter as shown in Figure 2.13 a) We observed that the feature having the largest diameter Figure 2.13 b) (5 µm) and Figure 2.14 a) smallest gap (0.8 µm) etched for 80 s has lower reflection value when compared with holes having smaller diameter and larger gaps.

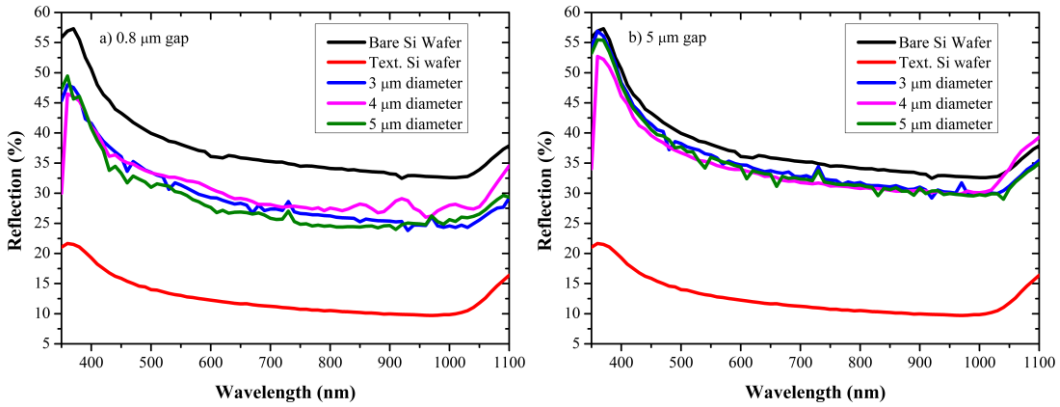


Figure 2.13 Reflection measurement comparison of surfaces textured with holes having 3 µm, 4 µm, 5 µm diameter, a) 0.8 µm and b) 5 µm gap dry etched for 80 s

When we kept diameter and dry etching time constant for samples shown in Figure 2.14 a), as in the case of constant diameter shown in Figure 2.14, 0.8 µm and 1 µm gap values were the lowest ones. For 1 µm gap we obtained around 1% less than

0.8 µm gap, this small difference was acceptable for 3 µm diameter represented in Figure 2.14 a), and the values were almost the same for 5 µm diameter plotted in Figure 2.14 b).

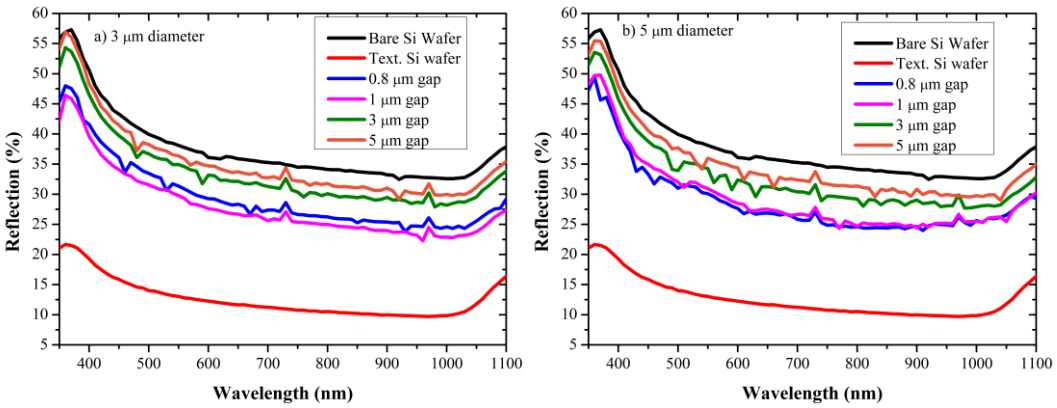


Figure 2.14 Reflection measurement comparison of surfaces textured with holes having a) 3 µm and b) 5 µm diameter with 0.8 µm, 1 µm, 3 µm and 5 µm gap dry etched for 80 s

We have observed optical information in terms of reflection depending on the hole diameter, gap, depth values, hence the distribution of holes on top of the surface. In order to make a better comparison for each periodic patterning, we have calculated their average reflection values with the formula represented in Equation 2.7 [31].

$$R = \frac{\int_{400}^{1100} R(\lambda) I(\lambda) d\lambda}{\int_{400}^{1100} I(\lambda) d\lambda} \tag{2.7}$$

Average reflection data is displayed in Figure 2.15 as a function of hole fraction. Figure 2.15 a) shows the average reflection value information obtained from surfaces patterned with 4 µm diameter, for this plot we kept diameter constant, and changed gap values and dry plasma etching duration. We had four different gap values, 0.8, 1, 3, 5 µm, and three different etching durations 40, 80, 160 s. Holes obtained with longer dry plasma etching time with deeper trench ended up with lower reflection values hence lower average reflection values. Figure 2.15 b) represents the graph of average reflection obtained with three different diameters 3, 4, 5 µm subjected to 80 s of dry plasma etching process. For each diameter we had four different gap values as

0.8, 1, 3, 5 µm. Only for one data point, Figure 2.15 b), 3 µm diameter, when the surface had 50% of hole fraction, the trend of the line changed in ascending direction.

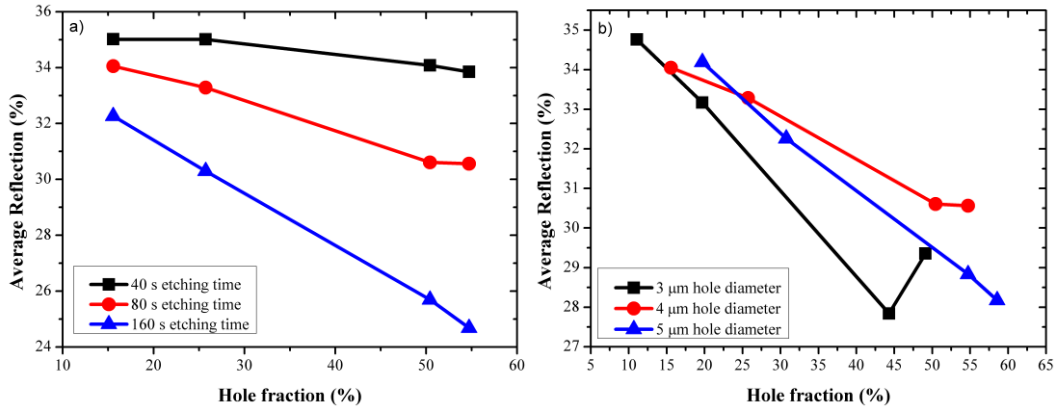


Figure 2.15 Average reflection spectra comparison depending on hole fraction of surfaces textured with a) 4 µm diameter having 0.8, 1, 3, 5 µm gap with 40, 80, 160 s etching times, b) 3, 4, 5 µm diameter having 0.8, 1, 3, 5 µm gap values with 80 s etching

For each diameter, we had four different gap values resulting in four pitch values. When we plotted AM 1.5 weighted average reflection value as a function of pitch size we obtained Figure 2.16. In Figure 2.16 a) we kept diameter constant, and changed etching duration for four different pitch sizes, Figure 2.16 b) wafer patterned with three different diameters were subjected to same dry plasma etching conditions.

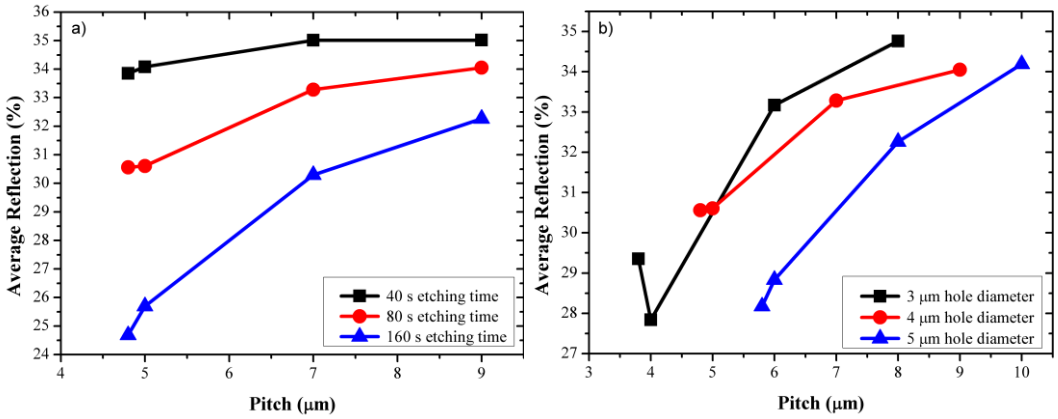


Figure 2.16 Average reflection spectra comparison depending on pitch size of surfaces textured with a) 4 µm diameter having 0.8, 1, 3, 5 µm gap with 40, 80, 160 s etching times, b) 3, 4, 5 µm diameter having 0.8, 1, 3, 5 µm gap values with 80 s etching

The trend of the data obtained from Figure 2.15 is just in the opposite direction of Figure 2.16. As the pitch size increases, the number of holes covering the surface decreases resulting in the increase of reflection values. Results shown in Fig. 2.17 and 2.18 are consistent and in agreement with the expectation of reduced reflection from the surface as the light trapping ability of the surface imporves with more hole fraction and less pitch size.

2.3 Surface Structures Generated by Metal Assisted Etching

Metal assisted etching (MAE) was first used as an electroless etching technique utilizing a discontinuous layer of metal in hydrogen peroxide (H_2O_2) and hydrofluoric acid (HF) to obtain porous Si and porous III–V compound semiconductor by Li et. al. in 2000 and 2002 in contrast to the conventional anodic etching method for porous semiconductor formation [88].

During MAE, noble metals are used to initiate local oxidation and reduction reactions. Metal such as gold (Au), platinum (Pt) and silver (Ag), deposited on the surface of a semiconductor (e.g. Si) serves as a local cathode to catalyze the reduction of oxidants (e.g. H_2O_2) producing holes. Random and periodic patterns can be obtained with the help of noble metals and appropriate chemical components. Table 2.8 summarizes comparison of MAE with other etching techniques briefly [35].

Table 2.8 Typical characteristics of three etching techniques for semiconductors [35]

	Wet etch	Dry etch	MAE
Directionality	Isotropic	Anisotropic	Anisotropic
Aspect ratio	Low	Medium	High
Ion induced damage	None	Mild to severe	None
Crystal orientation dependence	Some	Weak	Weak
Etch rate	Fast	Slow	Fast
Sidewall smoothness	Smooth	Not smooth	Smooth or rough
Chemical selectivity	Good	Poor	Depends
Cost	Low	High	Low

Huang et al. concluded that in solutions with low oxidant concentration, etching proceeds along the crystallographically preferred <1 0 0> directions, whereas

etching occurs along the vertical direction relative to the surface of the substrate in solutions with high oxidant concentrations. This was attributed to the competition of the hole injection (oxidation) and mass transport (dissolution) with respect to surface atom density. The amount of carriers (h^+) injected and consumed could regulate both the etching direction and morphology. In addition to these, the porosity increases as the wafer resistivity decreases [89].

MAE can easily be applied to form random structures as well as deterministic patterns following to lithography processes. It is relatively simple and low-cost such that all process can be carried out in a chemical lab without expensive equipment. MAE allows easy-control of various parameters (e.g., cross-sectional shape, diameter, length, orientation, doping type, and doping level). In particular, MAE enables control of the (1) orientation, (2) shape and (3) size of Si nanostructures (e.g., nanorod, nanohole) relative to the substrate. (1) Orientation of nanostructures can be altered by changing the chemistry of solution or temperature while <100> is the preferred direction at room temperature. (2) Unlike VLS-based methods that can only be used to grow wires with circular cross-sections, MAE is much more flexible and can be used to make higher surface-to-volume ratio structures. (3) MAE can be employed to fabricate straight and well-defined pores or wires with diameters as small as 5 nm or as large as 1 μm [88,90].

During MAE of Si, one of the noble metals (mainly, Au, Ag, Pt or Pd) is first deposited on the wafer and it is immersed into $HF/H_2O_2/H_2O$ solution. It is well-accepted that the chemical or electrochemical reactions occur preferentially near the noble metal. The process can briefly be summarized as follows.

- At the cathode (the metal): H_2O_2 is reduced as $H_2O_2 + 2H^+ \rightarrow 2H_2O + 2h^+$
- At the anode (the silicon substrate): The Si substrate is oxidized and dissolved. Although the reaction is controversial, there are three main models proposed for the dissolution process of Si as given below :

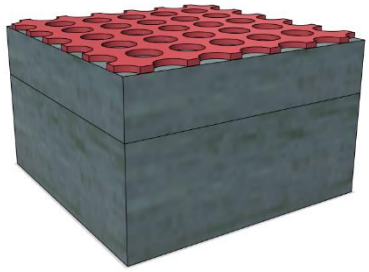
$$Si + 4h^+ + 4HF \rightarrow SiF_4 + 4H^+ \text{ or } SiF_4 + 2HF \rightarrow H_2SiF_6 \quad (2.8)$$

$$Si + 4HF_2^- \rightarrow SiF_6^{2-} + 2HF + H_2 \uparrow + 2e^- \quad (2.9)$$

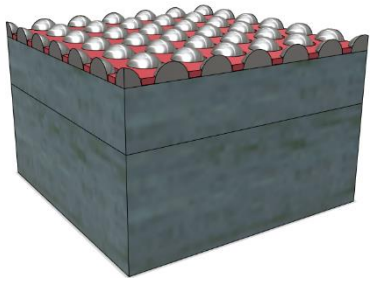
$$Si + 2H_2O \rightarrow SiO_2 + 4H^+ + 4e^- \;\&\; SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O \quad (2.10)$$

2.3.1 Metal Assisted Etching: An Alternative Technique for Surface Structuring

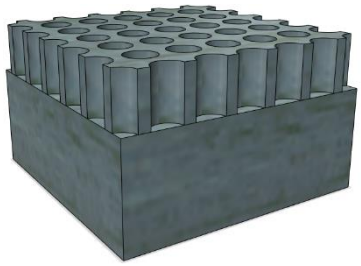
Metal assisted etching (MAE) technique is a wet etching method for fabricating random and periodic structures with the help of catalyst effect of metals. Depending on the type of patterning either periodic or random, photolithography process is required. In this study, we have obtained periodic hole texturings obtained with MAE. Prior to wet chemical etching step the wafer was subjected to optic lithography. Experimental sequence used to generate the patterns with MAE in this work is shown in Figure 2.17.



Step 1: Patterning c-Si surface was done with photolithography. The same masks used for dry etching were also used for wet etching process accelerated with metals.



Step 2: A thin layer of metal is evaporated on patterned surface and photoresist is lifted of by using aceton leaving behind the metal islands in the region where the photoresist was removed by the previous lithography step.



Step 3: MAE process was then initiated using the chemicals described above. The final step of MAE is getting rid of remaining metal. Depending on type of utilized metal, suitable chemical solution is applied to remove metal

Figure 2.17 MAE process sequence for periodic hole texturing

For periodic patterning we need to use lithography sequence regardless of the etchant type. The most critical point for MAE is defining resist thickness and removing residual resist layer in order not to remove evaporated metal layer during lift off process.

During MAE, Si under the deposited metal is etched away and therefore the metal is immersed into silicon substrate. Metal can be positioned onto silicon substrates by condensation from $AgNO_3$ solution or by deposition of Ag/Au metal using sputtering, e-beam evaporation, etc. The effects of temperature, light illumination, and solution chemistry are important parameters defining the final morphology.

2.3.2 Dependence of Etch Rate on Orientation During MAE

In principle, c-Si has an orientation dependent etch rate which is a function of the bonding energy of the surface atoms on that particular plane. {111} surface has two surfaces with atoms having one free bond ending up with a low surface energy, one with very high activation energy due to three back bonds. On the contrary, {100} surface has lower activation energy [35]. In this part of our study, we tested the orientation and having the same hole patterns went through MAE etching process as a function of etching time as shown in Table 2.9. This data is also displayed graphically in Figure 2.18. From this plot, we calculate the etch rate as 0.43 and 0.13 for (100) and (111) respectively. We see that (111) surface has significantly lower etch rate than (100) surfaces as expected from the higher bonding energy on (111) surfaces.

Table 2.9 Comparison of <1-0-0> and <1-1-1> oriented wafers coated with 25 nm Ag which were subjected to MAE

Diameter (µm)	Gap (µm)	Time (min)	Depth <1-0-0> (µm)	Depth <1-1-1> (µm)
2	1	60	23.20	4.62
2	1	45	17.8	4.21
2	1	30	13.05	4.05
3	0.8	25	11.06	3.45
3	1	18	6.46	2.91
3	3	15	6.02	1.65
3	5	12	3.77	1.15
5	0.8	6	2.86	874.4 nm
5	1	9	4.84	1.33
5	3	6	3.57	386.7 nm
5	5	3	1.75	425 nm

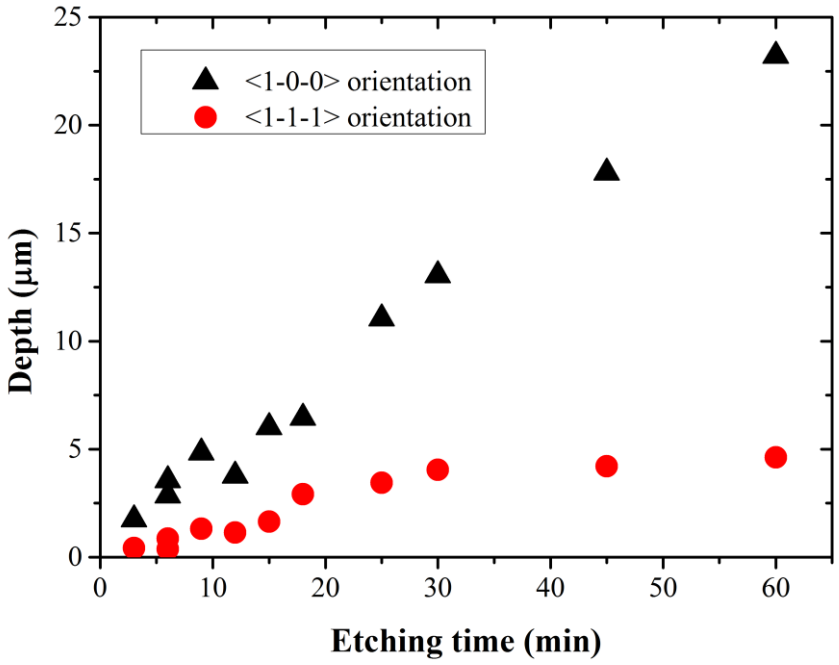
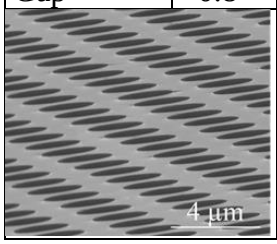
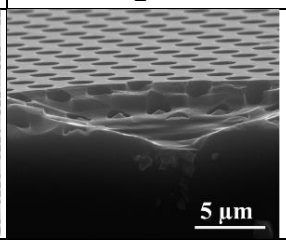
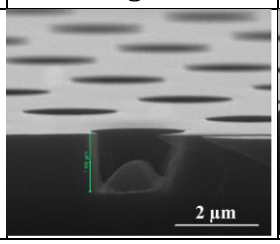
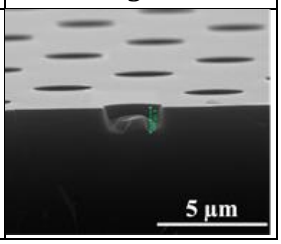


Figure 2.18 Etch rate comparison of wafers coated with 25 nm Ag having <1-0-0> and <1-1-1> orientation

When we used 25 nm Ag for MAE process on top of (111) wafers, due to low etch rate values, even after one hour etching, when we looked at their cross sectional view with SEM, we have observed that the depths were not greater than 4 µm. Table 2.10 shows the holes having same diameter, 3 µm, and 0.8 µm, 1 µm, 3 µm and 5 µm

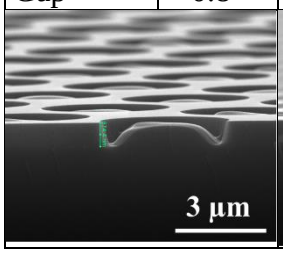
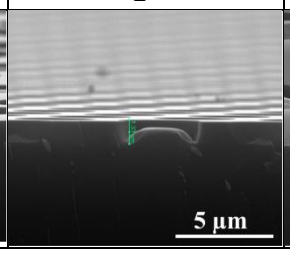
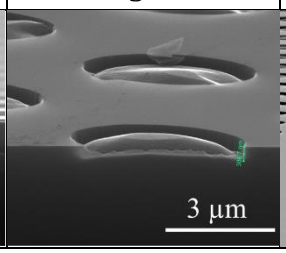
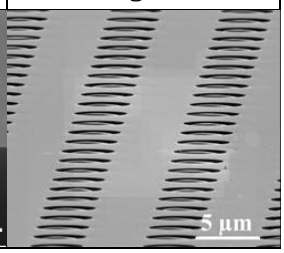
gap between holes. These samples were existing on the same wafer and subjected to same process conditions. It can be said that the uniformity of textures was perfect, but for deeper structures MAE technique was not effective for (111) wafer with aforementioned hole dimensions.

Table 2.10 SEM images of <111> oriented wafers including holes with 3 µm diameter and 0.8, 1, 3 and 5 µm gap. 25 nm Ag layer was used during MAE

Diameter	3	3	3	3
Gap	0.8	1	3	5
				

We also did MAE on <111> wafer with 5 µm diameter and four different gaps subjected to 20 min wet etching. As tabulated in Table 2.11 this wet etching duration is not enough for deep structures, also etching has initiated from side walls of the hole textures.

Table 2.11 SEM images of <111> oriented wafers including holes with 5 µm diameter and 0.8, 1, 3 and 5 µm gap 25 nm Ag layer was used during MAE

Diameter	5	5	5	5
Gap	0.8	1	3	5
				

2.3.3 Plasma Photoresist Descum

As discussed in section 2.2.1 in detail, plasma descum is a special case of oxygen plasma which is used to remove thin residual layer of photoresist following

developing step of lithography. This residual film is typically less than 1.000 Angstroms, but can interfere significantly in resolving the pattern during etching, especially if the pattern geometries are small (such as contact windows). A plasma descumming can generally remove these residues in less than a minute.

The wafers are loaded into the reactor chamber, and a plasma is established by using nitrogen. The wafers are heated during the nitrogen plasma, the nitrogen plasma is extinguished, and an oxygen plasma is established for the appropriate time, usually about one minute. Then, the system is vented to atmosphere. The sample is now ready for etching [91].

Descumming may not always be necessary or desirable depending on resist residue thickness. Therefore, a careful determination of the requirement should be made before implementing this procedure. The descumming process itself demands stringent control be maintained so as not to adversely affect the integrity of the photoresist layer or alter the pattern quality. Serious degradation in the uniformity of etching may occur.

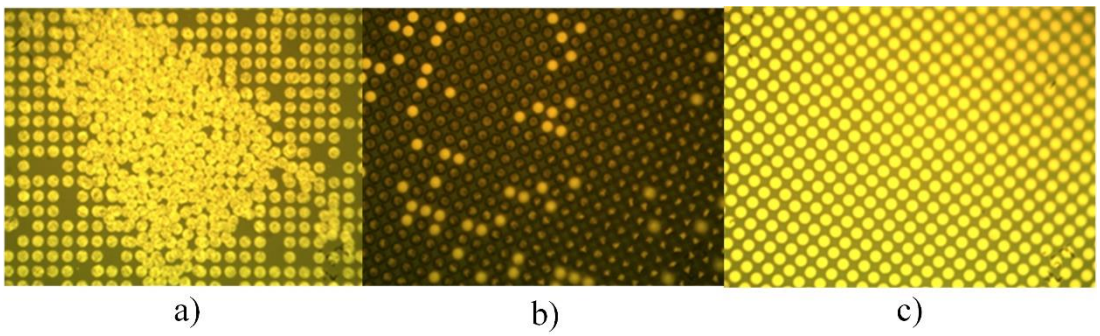


Figure 2.19 Microscope images of holes coated with 25 nm Au having 5 µm diameter and period of 6. a) with overlap, b) almost all metal is removed, c) full pattern coverage

In Figure 2.19, it can be seen that, wrong lift-off conditions will end up with undesired positions of metal layers, which will further affect the etching and final surface topography. Figure 2.19 a) surface ended up with the overlap of metal layers meaning that during lift off more than necessory resist layer was removed and during their removal metal layer was also partially removed. If we increase lift off duration, and make thinner resist layer with longer descum time, than the top surface of patterned wafer would be just like Figure 2.19 b) almost all metal was removed. Figure 2.19 c)

is a very nice representation of surface for the optimum descum and lift off process parameters from which we could manage to obtain our patterns successfully.

2.3.4 Surface Analyses of Structures Textured with MAE

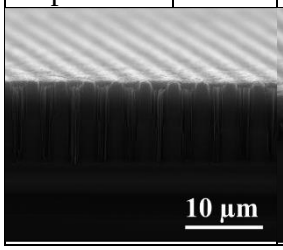
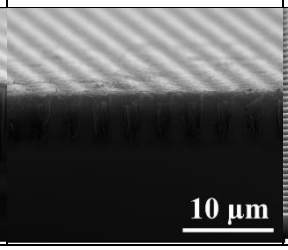
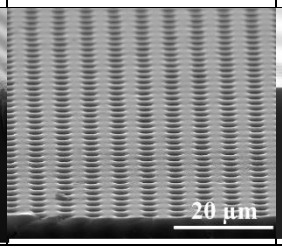
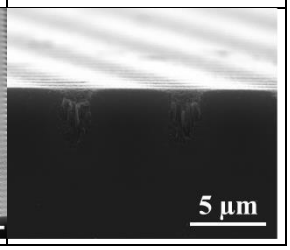
GÜNAM has recently fabricated Si nanowires and nanorods by MAE and systematically investigated their optical properties as function of their length. Solar cells in radial configuration were fabricated and tested. In particular cell structures where organic thin film was used as the top layer on the nanowires, a significant improvement in the cell efficiency was obtained compared to planar devices [92].

Most recently, GÜNAM was able to fabricate high-aspect-ratio Si nanowires on solar cells at industrial scales (156 mm x 156 mm). Surface with random and periodic patterns is limited by geometrical limitations of selected texture. Although successful demonstration of solar cells was achieved, these cells suffered from very high surface recombination due to high surface area [93]. This problem has led to lower efficiency values than standard cells. For our hole textured surfaces we tried to minimize these limitations and tried to obtain best results, whose fabrication methodology will be possible to be applied to standard solar cell fabrication.

Masks were designed with different diameter and pitch sizes, during fabrication step we could manage to control the depth of textures. During our experiments, for some cases, we varied the hole depth by the time of etching process. Depending on hole diameter, the effectiveness of chemicals to penetrate inside the holes varied. When the diameter is larger, the process will proceed quicker compared to smaller diameters. We have made comparisons with keeping some parameters constant, e.g. diameter, time.

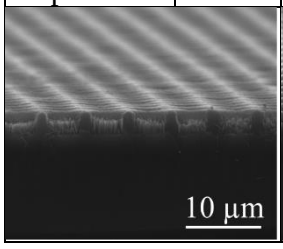
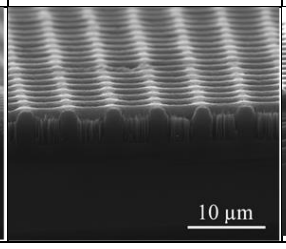
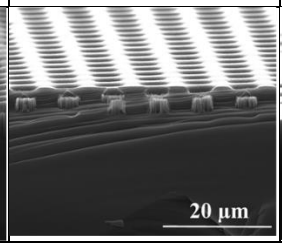
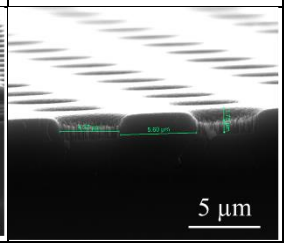
Table 2.12 given below shows an example of a sample set with different hole depth having same diameter value. SEM images of this sample set are shown in Table 2.12. We see that holes exceeding 10 μm can easily prepared by MAE. Thanks to successful lift-off process, we could manage to obtain uniform hole distribution over the whole wafer surface. Etch rate does not scale with the total area of metal catalyst, because of variation in solution based etching and possibly due to sharing of generated holes within adjacent areas.

Table 2.12 Wet etching process details and SEM images of structures including holes with 3 µm diameter and 0.8, 1, 3 and 5 µm gap

Diameter	3	3	3	3
Gap	0.8	1	3	5
Time	25	18	15	12
Depth	11.06	6.46	5.02	2.66
				

When we applied different etching times for holes with 5 µm diameter, it can be seen in Table 2.13 that depth increased with increasing etching time just as the same as we observed for holes having 2 µm, 3 µm and 4 µm diameters. Cross sectional SEM images tabulated in Table 2.13 where MAE ended up with randomly distributed nanowires inside the periodically distributed holes. The reason of these wires was the consumption of metals during chemical reaction with different rates. As reaction proceeds, metal on top of silicon surface aimed to be etched and ended up with holes, leaves the surface partially and contributes to reaction at each point of the surface with varying ratios depending on residual metal layer.

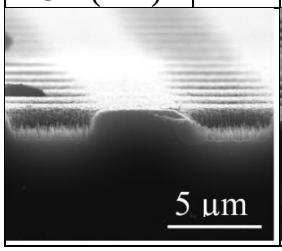
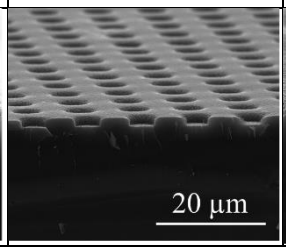
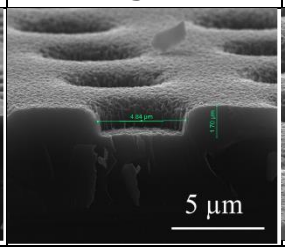
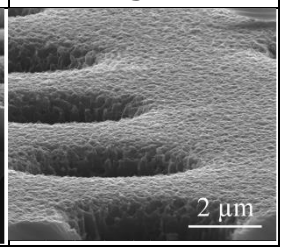
Table 2.13 Wet etching process details and SEM images of structures including holes with 5 µm diameter and 0.8, 1, 3 and 5 µm gap

Diameter	5	5	5	5
Gap	0.8	1	3	5
Time	6	9	6	3
Depth	2.86	4.84	3.57	1.75
				

During MAE, chemical reaction is not occurring just at the desired points of surface, but it also occurs on the surface which is supposed to be kept as the gap between holes. Gap between holes is also affected by the chemical containing HF, which is very reactive with Si surface which is prone to be oxidized in the solution during process. After lift-off process, metal is conformably coated on top of the holes, but when the reaction starts, metal also takes part in reaction as a catalyst. As the reaction continues the surface of hole textures is not totally covered with metal, it is behaving like a point etchant source for etching process ending up with wires. Optically perfect contribution of wires end up with electrically undesired structures such as nanowires in holes which are not easily passivated.

In order to get rid of these wires, and make surface as smooth as desired, diluted potassium hydroxide (KOH) can be applied. For samples having different pitch sizes, different time for KOH wire cleaning process was selected. For structures with larger pitch size shorter time was sufficient. As the time of KOH texturing increases, this also makes surface being etched which causes additional etching textured surface itself [94]. In the Table 2.14 below, we see that these wires are etched away and more flat and uniform hole structures are formed by this method.

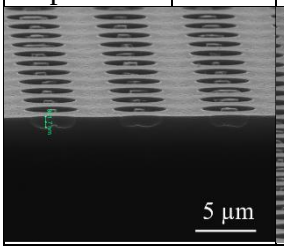
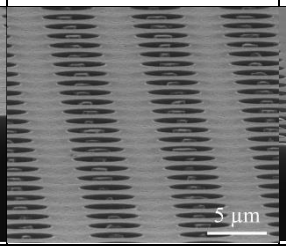
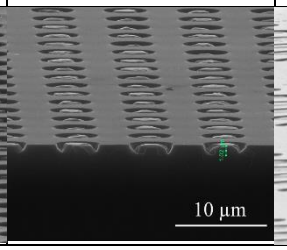
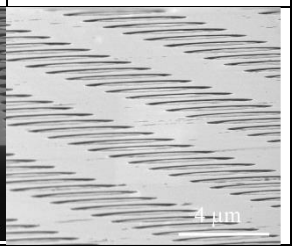
Table 2.14 Cross sectional SEM images of sample having 5 µm diameter and 10 µm pitch size. 25 nm Ag, 3 min MAE was applied to surface. a-b) 1 min KOH, c-d) 3 min KOH, (KOH: H_2O = 1:10)

Diameter	5	5	5	5
Gap	5	5	5	5
KOH (min)	1	1	3	3
				

In addition to silver, MAE was applied to surfaces coated with different metals such as gold, titanium ending up with different topographies. Table 2.15 shows top

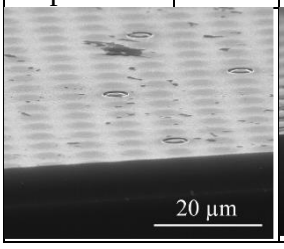
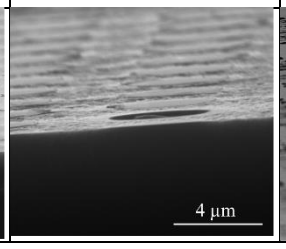
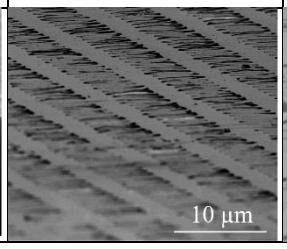
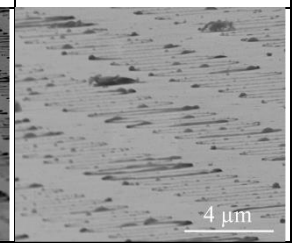
view and cross sectional SEM images of surfaces coated with 20 nm gold and etched in the same chemical solution just like as silver used MAE.

Table 2.15 Cross sectional SEM images of sample having 5 µm diameter and 3 µm gap size. 20 nm Au, 2 hours MAE was applied to surface. a-b) H_2O: HF: H_2O_2 (15:4:1), c-d) H_2O: HF: H_2O_2 (200:63:8)

Diameter	5	5	5	5
Gap	3	3	3	3
				

In some studies, to make a better contact between surface and metal, researchers suggested to use an intermediate metal layers, such as titanium, which will cause preferential material removal with desired aspect ratios [82]. Table 2.16 represents SEM analysis of the surface coated with 4 nm titanium and 20 nm gold. Reactions occuring on top of the surface gave damages to surface, the uniformity was protected but etching was not as well as we planed.

Table 2.16 Cross sectional SEM images of sample having 5 µm diameter and 3 µm gap size. 4 nm Ti and 20 nm Au, 2 hours MAE was applied to surface. a) 1 hour MAE with H_2O: HF: H_2O_2 (15:4:1), b) 2 hour with MAE H_2O: HF: H_2O_2 (15:4:1), c) 1 hour with MAE H_2O: HF: H_2O_2 (200:63:8), d) 2 hour MAE with H_2O: HF: H_2O_2 (200:63:8)

Diameter	5	5	5	5
Gap	3	3	3	3
				

Different chemical concentrations and metals were used for the same structures for comparison. Table 2.17 shows a summary of different MAE trials with different metals and hole configurations. As the time increases the depth increases, meaning there is enough chemical solution and metal in the medium ending up with etching of silicon surface.

Table 2.17 MAE process details for our hole textured surfaces coated with the same thickness of Ag and Au, etched in H_2O: HF: H_2O_2 = 200:63:8

Dia (µm)	Gap µm)	Time (min)	Depth <1-0-0> 25 nm Ag	Depth <1-0-0> 25 nm Au
2	1	60	23.20	3.31
2	1	45	17.8	2.43
2	1	30	13.05	1.12
3	0.8	25	11.06	952.1 nm
3	1	18	6.46	446.9 nm
3	3	15	6.02	243 nm
3	5	12	3.77	-
5	0.8	6	2.86	-
5	1	9	4.84	-
5	3	6	3.57	-
5	5	3	1.75	-

During our MAE experiments, we have observed that using gold ended up with shallower holes compared to silver as shown in literature [95]. For shorter wet chemical etching durations, less than 12 min, surface was almost had zero depth having surface corrugations.Figure 2.20 shows the experimental etching parameters that we have observed after making MAE with 25 nm gold and silver. The wafers that were used during this wet chemical etching study had <1-0-0> orientation.

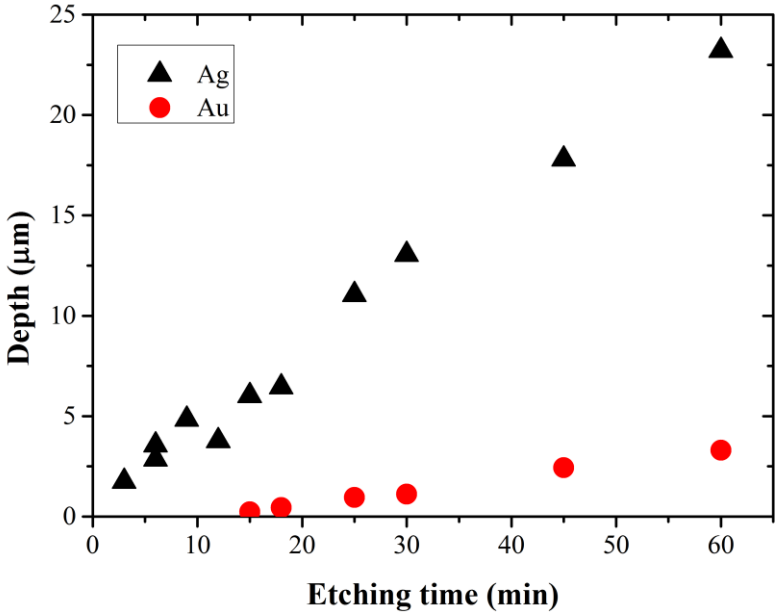


Figure 2.20 Etch rate comparison of <1-0-0> oriented wafers coated with 25 nm gold and silver

From Figure 2.20 etch rate of silver from the slope of depth/time line calculated as 0.42, where the etch rate of gold was 0.05. From the process outcomes we can conclude that deeper structures can be obtained with silver including wires inside. The wires can be removed with KOH texturing [94]. Gold assisted wet chemical etching ends up with shallower structures compared to silver assisted wet chemical etching.

2.3.5 Optical Properties of Micro and Nano Structured Surfaces Prepared by MAE

Optical properties of wet chemical etching technique applied surfaces with different surface properties such as diameter, pitch and depth were analyzed and compared. The chemical composition of the solution and temperature were kept constant. For reactions we have changed the metal thickness and the duration of reaction. As represented in section 2.3.4 in detail, SEM images let us know the textures obtained on top of the surface. Randomly distributed wires inside periodically patterned holes ended up with low reflection values, almost lower than the state of the art pyramid textured surface.

Reflection from samples with different hole diameters and gaps are shown in Figure 2.21 a) for 3 µm diameter,Figure 2.21 b) for 5 µm diameter. After lithography step, short oxygen plasma descum was applied to the surface. After that 25 nm silver

was evaporated and chemical wet etching was done for one hour. Surface textures obtained with dry plasma etching had reflection values lower than bare silicon, but higher than pyramid texturing. For MAE it can be seen that the average reflection values as low as %7 have been obtained, which was %12 for pyramid texturing. This was achieved before SiNx deposition. We can expect further reduction in reflection after SiNx deposition.

When the diameter was kept constant and gap size varied, smaller gap dimension gave the lowest reflection values. The more the number of holes on top of the surface, the more effective trap light resulting in lower surface reflection as shown in Figure 2.22.

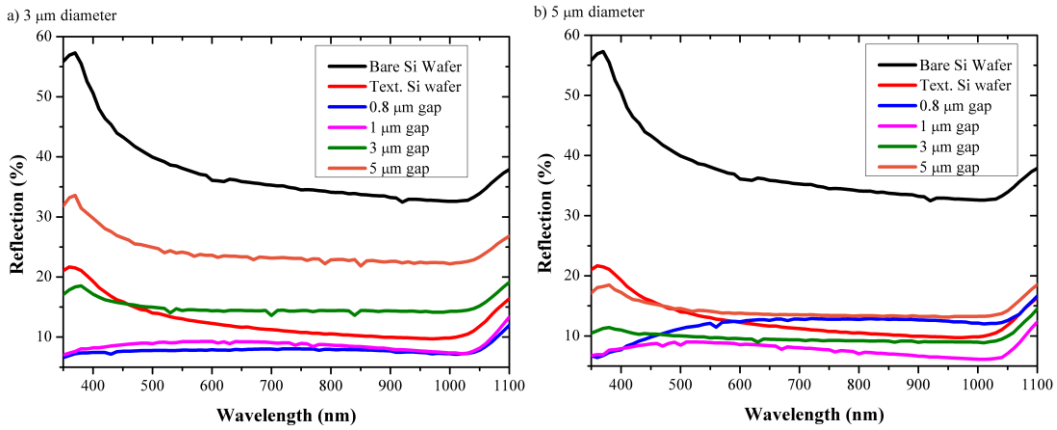


Figure 2.21 Reflection measurement of surfaces coated with 25 nm Ag, including holes with a) 3 µm diameter and 0.8, 1, 3, 5 µm gap and b) 5 µm diameter and 0.8, 1, 3, 5 µm gap

In order to make better comparison we used the same wafer coated with 25 nm gold, which was processed with the same parameters as the same as silver evaporated one. Wet chemical etching duration was also taken as 1 hour. Figure 2.21 a) shows the reflection values of samples with 3 µm diameter and for 0.8, 1, 3, 5 µm gap , Figure 2.21 b) with 5 µm diameter and for 0.8, 1, 3, 5 µm gap values.

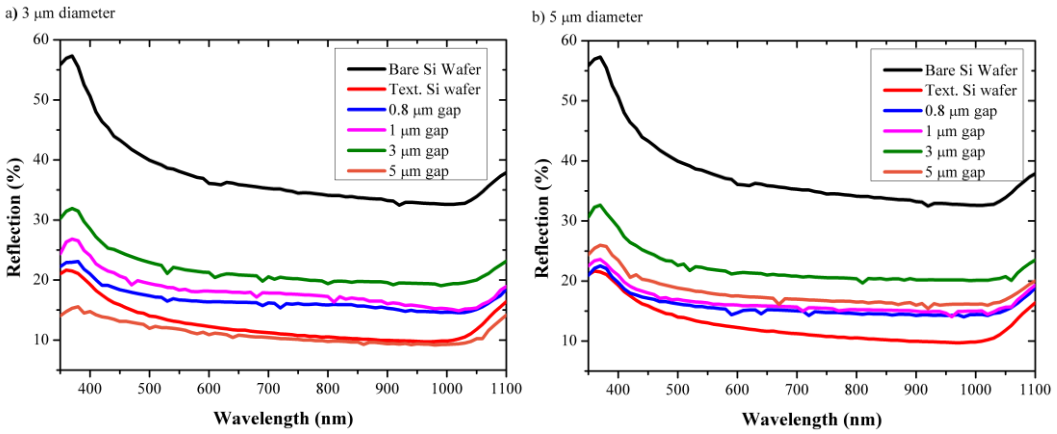


Figure 2.22 Reflection measurement of surfaces coated with 25 nm Au, including holes with a) 3 µm diameter and 0.8, 1, 3, 5 µm gap and b) 5 µm diameter and 0.8, 1, 3, 5 µm gap

Reflection measurements of MAE applied surfaces have lower values compared to RIE applied surfaces due to random nano wires inside periodically patterned holes. For optical properties these values are aimed to be achieved, and will end up with high efficiency solar cells when electrical enhancement can also be managed.

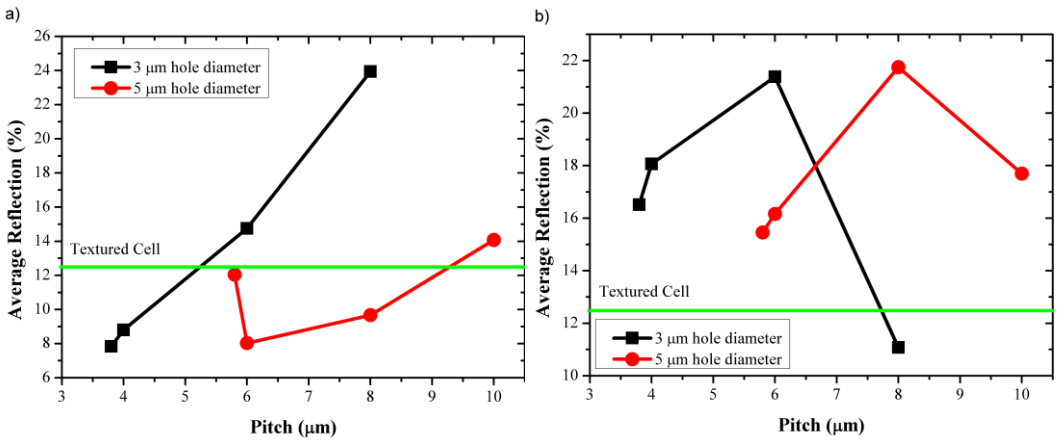


Figure 2.23 Average reflection spectra comparison depending on pitch sizes. MAE applied with a) 25 nm Ag, b) 25 nm Au

The lowest average reflections were obtained from pitch sizes of 4 µm and 6 µm as shown in Figure 2.23. These values were obtained from the surfaces coated with 25 nm silver. In addition to silver's higher etching rate than gold, we can conclude that

with the same process conditions, it is possible to obtain deeper structures including wires inside with the effective etching properties of silver.

2.4 Submicron Periodic Patterning by Nanoimprint Lithography

Surface texturing is an effective and more lasting technique in reducing reflections and improving light trapping compared anti reflection coatings. Although thin film solar cells offer the advantage of the reduced material cost, transmission losses are increased and cell performances are degraded as absorber layer become thinner. Up to now, in literature there have been many ways used for the fabrication of nanostructures as mentioned in Chapter 1, section 1.6. Patterning thinner substrates with nanoimprint litography (NIL) is one of the hottest topics of solar cell technology. Many research groups are trying to optimize their processes and increase the efficiency while decreasing the cost of the product [23].

2.4.1 Basics of Experimental Procedures

In this part of the thesis, which was conducted at IMEC, we aimed to obtain periodically arranged structures using NIL patterning, which is assumed to be one of the most promising and relatively low cost methods compared to other techniques of surface patterning [96]. For NIL process what should be done first is to design a master stamp with desired sizes and let it be produced with stepper. After obtaining master stamp, soft stamp was fabricated and pattern transfer was made.

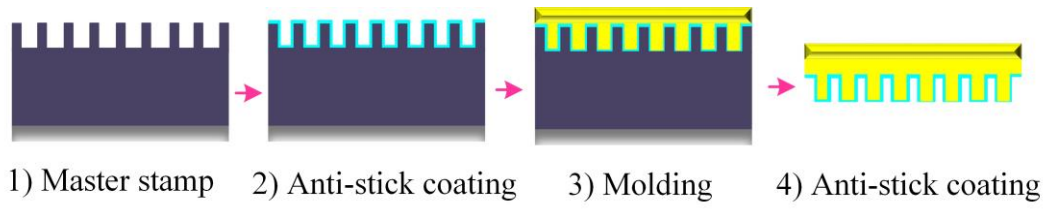


Figure 2.24 Schematic representation of soft stamp fabrication process step

Figure 2.24 briefly represents the fabrication schematic of soft stamp fabrication as:

1. Preparing master stamp (5x5): Master stamp should be cleaned for about 10 min in SPM solution (H_2O_2:H_2SO_4=1:4), 2 min H_2O: HF: HCl=20:1:1, 5 min

SPM (H_2O_2:H_2SO_4=1:4), and in between each step kept it in deionized (DI) water till resistivity value became 0.25 respectively.

2. Deposit Octadecyltrichlorosilane (ODTS): We waited for two hours at 160 ^oC, for the oven to reach the temperature, and stabilize at that level. What is crucial at this step is to take ODTS outside refrigerator for letting it get close to room temperature. During process 60 µl ODTS was used, coating lasted for one hour, and the pressure was around 2.8^{+2} mTorr.

3. Molding soft stamp: Liquid Silicone elastomer and an agent, which initiates polymerization reaction, are used for this step. Silicone elastomer has long chains, and agent creates a bridge in between these long chains, with this base-agent interaction we get long chains connected to each other with bridge-agents. The rule of thumb for this mixture is to make a mixture consisting of 10/1 ratio of liquid Silicone to agent. After making a good mixture we poured it over our master stamp and kept inside an oven which was 80 $^{\circ}C$ for two hours. In order to be able to manage pattern transfer and successful removal of soft stamp we kept it for one day, than with a careful detachment we can get our soft stamp.

4. Deposition of ODTS to our soft stamp: This step is the same as applied to our master stamp.

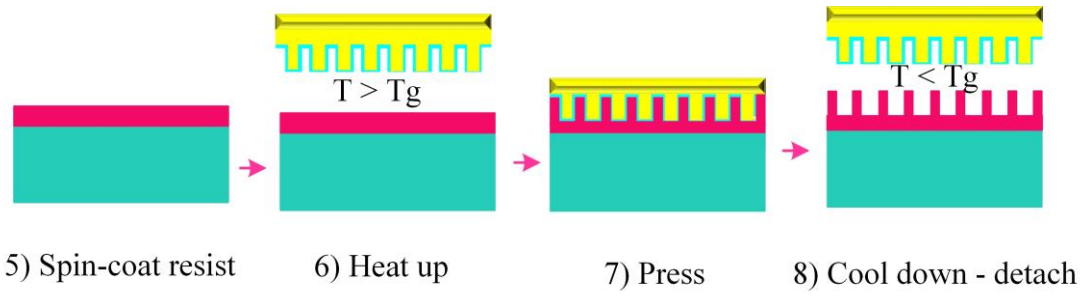


Figure 2.25 Schematic representation of imprint process step

In Figure 2.25 imprinting step is depicted. In order to make imprint, the resist should be hot enough to transfer the pattern of the master stamp. Depending on the

stamp size and the depth of the pillars, temperature and force to be applied can be defined as:

5. Resist Coating: Thickness of the resist was defined depending on the soft stamp pitch and depth sizes. MR-I 7010 positive resist was used during coating with 1000 rpm, 500 rpm acceleration with 30 s spin time.

6. Heating: In order to pattern the resist with desired features, it can take form of the master stamp when we increase the temperature.

7. Imprint: Process was done at 130 $^{\circ}$C applying 3.75 kN for two min. Before applying pressure we kept our wafer on hot bottom chuck for one min. The force to be applied depends on soft stamp volume, this value is valid for master stamps with 5x5 cm dimension.

8. Detachment: During detachment of imprint step applied force is needed to be kept constant and the time necessary for cooling down should be optimized for this step.

Regardless of etching type (either wet or dry) residual resist layer should be removed. As depicted in Figure 2.26, for dry etching oxygen plasma can be applied to dissolve the resist. Oxygen plasma is also applied to obtain a uniform resist thickness on surface

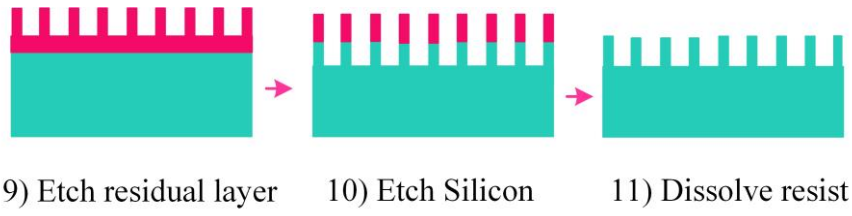


Figure 2.26 Schematic representation of pattern transfer and etching process steps for NIL method

9. Residual layer removal: A few seconds of oxygen plasma was sufficient for residual resist layer. The thickness of resist was checked and depending on the stamp size and resist thickness appropriate cleaning time was applied.

10. Etching: Either wet, or dry etching can be selected after pattern transfer.

11. Resist removal: At the end of imprinting and etching steps, the surface should be cleaned, in order not to remove any resist residues.

Above mentioned process steps are applied to all wafers during NIL process. The most crucial and only defining step is the master stamp's pitch and depth size, after these unique parameters, also etching process is crucial, as the desired depth can be varying and requires many optimizations.

For different stamps, different process parameters are required, such as resist thickness, applied force, oxygen plasma time and gas flow rates. We have worked with five different master stamps as tabulated in Table 2.18, with different pitch size, diameter and the depth of pillars which will end up with holes having the same depth of these pillars of the master stamp on resist coated wafers.

Table 2.18 Mask dimensions for master stamps

Pitch (nm)	Diameter (nm)	Depth (nm)
900	310 (*590)	150-160
800	550 (*250)	200-210
600	380 (*220)	150-200
600	240 (*360)	120-130
400	200 (*200)	100-110

(*The values for diameter are the ones that we are expecting to obtain for soft stamps)

Dimensions of stamps were checked with SEM. During soft stamp fabrication step 8 shown in Figure 2.25, detachment part is getting more complicated for shapes having smaller dimensions. Some stamp fabrications ended up with undesired dimensions, especially for larger soft stamps (10x10), for this situation, soft stamp can be created with smaller dimensions (2x2). The smaller the stamp size, the less risky for fabrication process due to easy and uniformly detachment possibility. As shown in Figure 2.27, the width of pillars (S_i), width of the holes (W_i) and the depth of these two parameters will define the resist thickness.

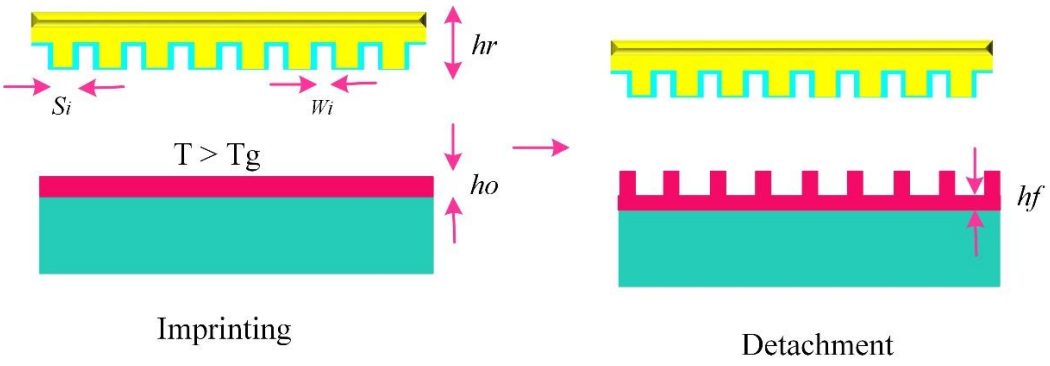


Figure 2.27 Schematic representation of residual resist layer thickness and master stamp's dimensions representation

The dimensions of master stamp gives the exact thickness of residual resist layer. From S_i and W_i, final residual resist layer thickness (*hf*) can be extracted from the initial resist thickness (*ho*) as shown in Equation 2.7 and 2.8. [97].

$$hf = ho - vhr \tag{2.7}$$

with fill factor *v*:

$$v = \frac{\sum_i Wi}{\sum_i (Si + Wi)} \tag{2.8}$$

Master stamp sizes as shown in Table 2.18 let us define resist thickness. With the correct resist coating recipe possible undesired imprinting faults during lithography step could be eliminated. In Table 2.19, depending on OBDUCAT resist data sheet, resist thicknesses for different coating recipes could be defined experimentally.

Table 2.19 OBDUCAT resist thicknesses depending on different coating recipes

Spin rate (rpm)	Acceleration (rpm)	Spin time (s)	Bake time (s)	Resist thickness (nm)
3000	500	30	60	108.5
2000	500	30	60	117.6
1500	500	30	60	131.9
1200	400	30	60	148.6
1000	500	30	60	160.8
800	200	30	60	185.3
500	100	30	60	211

When the spin rate was increased, the thinner resist layer was obtained, which would be desired for smaller pillars with smaller pitch and depth values calculated from Equation 2.8.

Each stamp with its unique specifications was optimized with NIL patterning technique and prepared for different etching methods. Depending on etching sequence desired patterns could be obtained with almost the same dimensions as the master stamp. The problematic parts of etching process was mostly related to feature sizes but more critical part was related with thinner wafers [98,99]. NIL pattern transfer and wet chemical etching combination are very challenging process sequences which need to be handled and developed for each stamp and etching type separately.

2.4.2 MAE with NIL

Patterning could be successfully applied with NIL, after pattern transfer step either wet or dry plasma etching sequence can be selected as shown in Table 2.23. As the core of this thesis is to make comparison between etching techniques combined with different patterning methods, we have combined metal assisted etching (MAE) technique with NIL patterning, which was investigated as an alternative texturing technique [100].

For MAE, our samples were coated with MRI-7010 resist, which were used during NIL patterning step, with the same conditions used for dry etching. During NIL process, before doing any etching step, what we first should do is getting rid of residual resist layer inside the holes, otherwise we won't be able to etch Si as the way we want. Undesired residual resist layers will end up with unexpected features. In order to

prevent such an undesired morphology, we have made optimizations for NIL and could manage to make successful lift off step with the help of O_2 plasma descum [87].

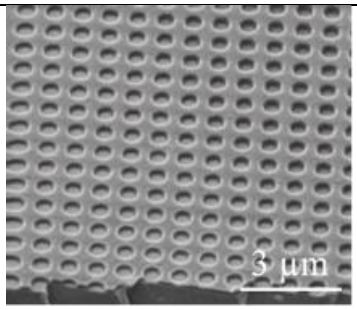
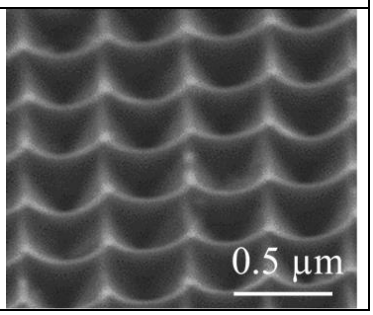
Before 25 nm Silver (Ag) evaporation, we applied 5 and 6 s of O_2 plasma descum to remove residual layer, and it can be easily said that 6 s application gave a better result than 5 s. After O_2 plasma descum, samples were coated with 25 nm Ag using thermal evaporation and ready for wet etching in a chemical mixture of H_2O : H_2O_2 : HF = 200 : 8 :63.

For MAE, process conditions could be optimized in a better way as NIL is by itself a complicated process, and when combined with MAE, experiment was more complicated as expected. The best improvement that we could manage was to make pattern transfer with NIL and obtain a uniform surface after MAE process.

2.4.3 Surface Analyses of NIL Textured Structures

After selecting the stamp and making lithography process optimizations for that stamp, etching process was optimized. Resist thickness, wet and/or dry etching conditions, residual resist layer removal vary upon stamp size. Each process step was developed and optimized and with the help of surface topography analysis we could make better process in terms of pattern transfer and etching. During dry etching step, in order to remove residual resist layer and obtain a uniform resist on top of the imprinted wafer, short O_2 plasma was applied to all surfaces, which is one of the most important process steps to proceed with correct texture parameters [99].

Table 2.20 NIL with master stamp having 800 nm pitch and 550 nm diameter

SEM image of NIL applied surface with the mask having 800 nm pitch and 550 nm diameter. Force to transfer pattern was 3.75 kN. O_2 plasma: 50 W, 50 sccm 5 s SF_6 RIE: 100 W, 30 sccm 15 s O_2 plasma: 50 W, 50 sccm 180 s	
SEM images of first NIL samples with 800 nm pitch and 550 nm diameter. Force applied was 3.75 kN. These samples were dry-etched for 45 s O_2 plasma: 50 W, 50 sccm 5 s SF_6 RIE: 100 W, 30 sccm 45 s O_2 plasma: 50 W, 50 sccm 180 s	

In Table 2.20, it can be seen that, the depth of obtained structures increased, as the etching time increased, which was expected. During dry etching what we first did was a short plasma descum depending on stamp's pillar depth and width sizes. For this sample we used master stamp having 800 nm pitch and 550 nm diameter. At the end of etching process we selected oxygen plasma cleaning, by means of surface texture either plasma cleaning, or acetone removal for resist doesn't make any changes.

When we started working with master stamp having 900 nm pitch and 310 nm diameter, we have defined new process parameters in order to proceed with desired surface patterns. Resist thickness and dry plasma etching conditions were defined after checking surface morphology with SEM tool. In Table 2.21 it can be seen that wrong detachment, and long etching duration ended up with random, undesired surface textures. Table 2.21 d) is representing the correct surface morphology with uniform expected distribution.

Table 2.21 NIL with master stamp having 900 nm pitch and 310 nm diameter

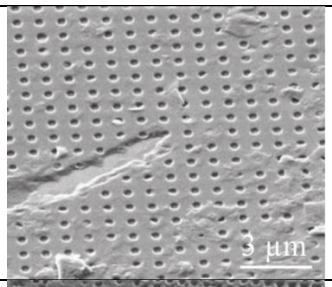
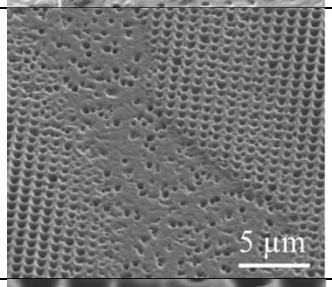
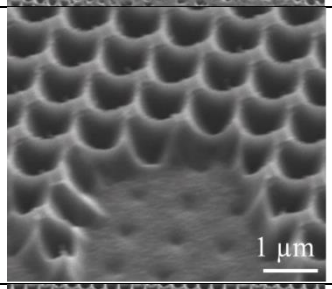
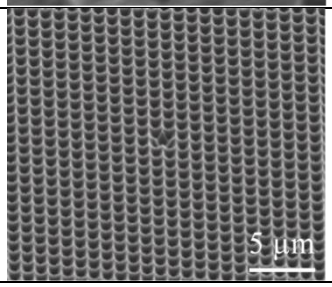
SEM image of 900 nm pitch and 310 nm diameter master stamp, some small parts of the wafer surface were patterned, and some parts were not due to either soft stamp quality or resist coating recipe. The thickness of the resist was 145 nm, and dry etching time was 30 s.	
SEM image of surface having 108 nm resist, which had the spin rate of 3000 rpm, and acceleration of 500 rpm, this sample was etched for 45 s in order to make comparisons. It can be seen that imprint process was partially achieved.	
SEM image of surface having 160 nm resist, which had the spin rate of 1000 rpm, and acceleration of 500 rpm, this sample was etched for 45 s in order to make comparisons. It can be said that during detachment very small area was wrongly removed.	
SEM image of surface having 180 nm resist, which had the spin rate of 800 rpm, and acceleration of 200 rpm, this sample was etched for 60 s. Imprint step was successfully achieved. The only problem is features are too close, additional etching may cause overlapping.	

Table 2.22 gives information about surfaces textured with the stamp having 600 nm pitch and 380 nm diameter. This stamp is relatively more challenging when compared with other stamps having larger pitch size and diameter of holes. What we did was conduct spin coating with the spin rate 800 rpm and acceleration 200 rpm ending up with 182 nm thick resist. Residual resist layer was around 20 nm which was removed with oxygen plasma and ended up with uniform resist thickness all over the surface. We aimed to use soft stamp more than once, and tried to obtain how many times we can manage to make pattern transfer with the same stamp. We could manage to use twelve times, after each imprint process we cleaned the soft stamp, but we observed some surfaces with unexpected morphology due to some resist residues left

inside soft stamp pillar, or insufficient ODTS coating of soft stamp ending up hydrophilic rather than hydrophobic.

Table 2.22 NIL with master stamp having 600 nm pitch and 380 nm diameter

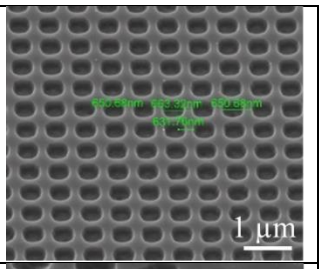
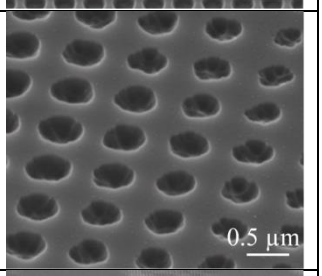
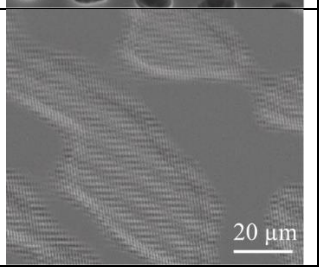
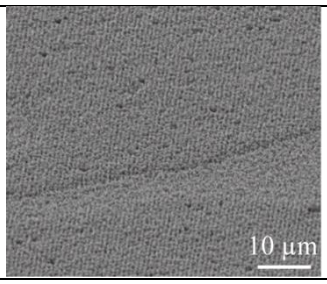
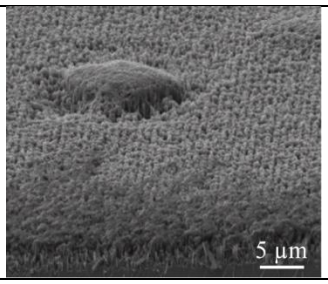
SEM image of of 600 nm pitch and 380 nm diameter sized master stamp. During lithography the spin rate was 800, and acceleration 200 rpm, this sample was etched for 15 s. This sample was the second use of the soft stamp with the predefined sizes.	
SEM image of 600 nm pitch and 380 nm diameter sized master stamp. This was the third use of the soft stamp. All dry etching process parameters were kept the same. The only difference was etching time, this wafer was etched for 45 s.	
SEM image of surface imprinted sixth time with the same master stamp. Due to either insufficient filling, or inadequate ODTS coating of soft stamp may end up with resist filled parts of the stamp which was carried to next imprinting processes.	

Table 2.23 NIL patterning and MAE with master stamp having 800 nm pitch and 550 nm diameter after 25 nm Ag evaporation

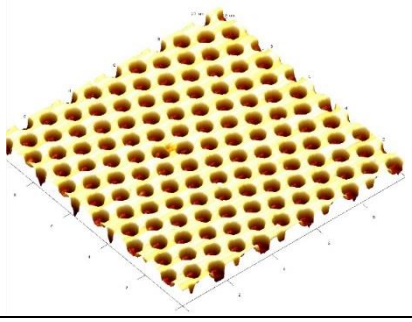
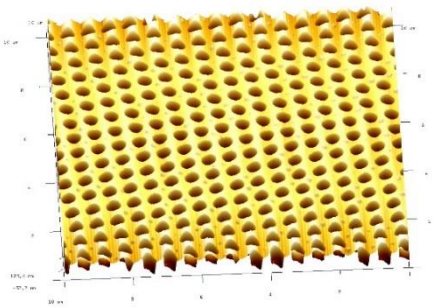
SEM data the mask having 800 nm pitch and 550 nm diameter with 3.75 kN force and 5 s O_2 plasma descum, and 3 min MAE		

We have combined NIL patterning and wet chemical metal assisted etching technique. During MAE we got the best uniformity with the stamp having 800 nm pitch and 550 nm diameter. Before lift off a short plasma descum let us end up with

successful metal coating. After checking surface coverage we initiated wet chemical etching process. Based on our experiences we selected silver to etch silicon surface. We aimed to obtain shallow depths and as uniform as possible structures. For shallow holes short etching times would be enough, we have changed etching time between 3 min to 30 min, and we obtained that 3 min of etching ended up with best uniformity. SEM image shows us a hill just in the middle of the surface, this may be due to multiple usage of soft stamp. Table 2.23 shows SEM analysis of the surface patterned with NIL and subjected to MAE.

SEM analyses gave us an idea about surface morphology, but from a limited area. When we wanted to check whole surface uniformity, we needed a more efficient way of analyzing technique. Atomic force microscope (AFM) let us check larger surface areas within shorter times compared to SEM. We obtained that we could manage to make a successful pattern transfer and define correct etching parameters ending up with desired patterns. Table 2.24 represents surface morphology of two different stamps ended up with uniform pattern. We also tried to apply different forces and the stamp with 600 nm pitch and 380 nm diameter gave better topographies with 3.03 kN.

Table 2.24 AFM analyses of surface textures obtained with two different stamps

AFM image of surface in which new stamp of sized 800-550 nm used and 3.03 kN force was applied. The less the force the better the pattern we obtain for this size. 170 nm thick resist was applied with prebake step for 30 min at 200 ˚C as told in material data sheet.	
AFM image of 600 nm pitch and 380 nm diameter sized master stamp with 3.03 kN force applied to the surface. The wafer was patterned first time with the soft stamp. Detaching from master stamp was challenging due to small sizes but seems promising.	

At the end of whole analyses we have observed that we should keep the stamp resist free. Any deterioration of the stamp would be transferred to future imprinting process. Partial removing it may have been due to inadequate ODTS coating which caused surface act as hydrophilic rather than hydrophobic.

2.5 Hole Colloidal Lithography

In order to increase the competitiveness of photovoltaics, in addition to reduced fabrication costs, high solar cell efficiencies with minimum material cost is required.. One solution suggestion for this is working with thinner c-Si substrates, however Si is an indirect bang-gap material and light absorption is not sufficient. To handle this problem different texturing methods are utilized to improve light trapping properties of the surface, and the most promising method is combining periodic and random structures together as mentioned in Chapter 1.

Introducing random textures with conformal coatings can be achieved with hole mask colloidal lithography (HCL) that enables the fabrication of plasmonic nanostructures with short range order. HCL was previously used for organic solar cells [101]. Randomly distributed textures will be combined with periodic structures, offering disordered features will be better than bare periodically textured surface morphology [102,103].

2.5.1 Basics of Experimental Procedures

The process building blocks are shown in Figure 2.28. The polystyrene beads (PS) are adsorbed on top of the surface and the etch mask is deposited. During the adsorption step, Figure 2.28 a), pattern is defined on Si surface. In order to make a conformal coating, the distribution of PS beads with the position, width and shape of the holes should be optimized. Before spreading PS beads, the surface is coated with three layers: polydiallyldimethylammonium (PDDA), poly sodium 4-styrenesulfonate (PSS), aluminum chloride hydroxide (ACH). These layers are positively charged, and after spreading negatively charged PS beads will cause an attraction between beads and the surface, which is desired. In the system, there will be a repulsive force due to same charged PS beads. With the effect of these repulsive and attractive forces the

distribution of beads will be defined. After the removal of PS beads either dry or wet etching technique can be selected [84].

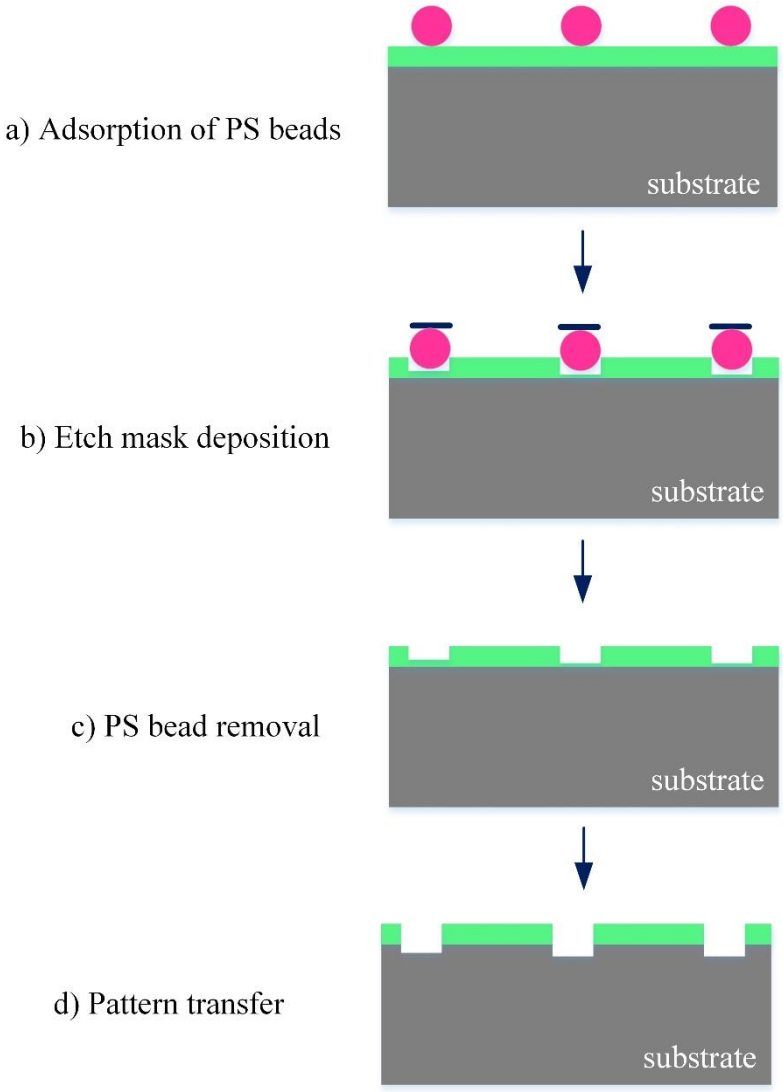


Figure 2.28. Schematic representation of HCL process: a) adsorption of beads, b) etch mask deposition, c) PS bead removal, d) pattern transfer

The bead size will define the dimension of the features that are intended to be obtained. The smaller the bead size, the easier to control on the surface coverage. When the bead size gets bigger, the probability of agglomeration gets higher, which will end up with larger unexpected features. The etch mask shown in Figure 2.28 b) is expected to be thick enough to survive during etching and thin enough to enable the bead removal. For HCL process we used samples fabricated with 1 µm ultra-thin

monocrystalline silicon layer called epifree. Epifree layer was bonded to glass, and approximately 50 nm Aluminum (Al) was deposited on top of bead covered surface as shown in Figure 2.29.

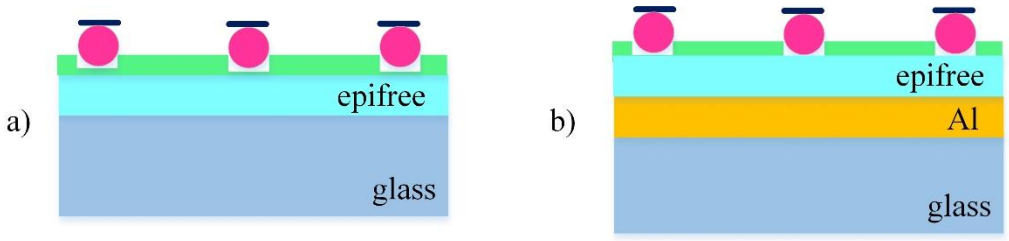


Figure 2.29 Schematic representation of substrates used for HCL having epifree layer bonded to glass, a) without Al, b) with Al

For etch mask deposition various deposition techniques can be used such as thermal evaporation, e-beam and sputtering.

2.5.2 Surface Analyses of HCL Textured Surfaces

In order to see the effect of hole colloidal lithography on surface morphology we have used different bead size and etching times. Depending on process parameters we ended up with surface covered with random holes, squares, depending on etching type pyramids with full surface coverage. Figure 2.30 depicts the surface of 1 μm epifree layer bonded to glass with Al mesh layer in between and PS beads having 270 nm bead size etched for 45 s and 35 s. As the etching time increased, the diameter of the beads increased ending up with larger features.

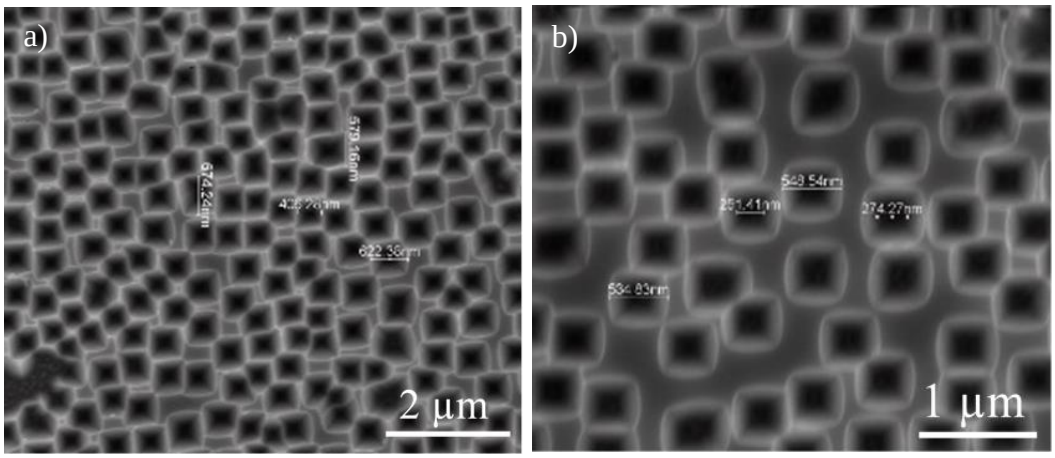


Figure 2.30 SEM image of HCL applied. The surface was 1 µm epifree layer bonded to glass with Al mesh layer in between and PS beads having 270 nm bead size. Dry etching was done for a) 45 and b) 35 s respectively

In this thesis, the diameters of the beads were varying from 270 to 510 nm. Depending on etching type (dry plasma or wet chemical anisotropic etching) and bead size process conditions were optimized. As depicted in Figure 2.30. When we change etching duration, surface has different pattern distribution. In addition to difference in depth, the gap between beads end up with smaller values (some of them have agglomeration). When we kept dry plasma etching time constant and changed the bead size, surface ended up with better coverage with larger beads as shown in Figure 2.31

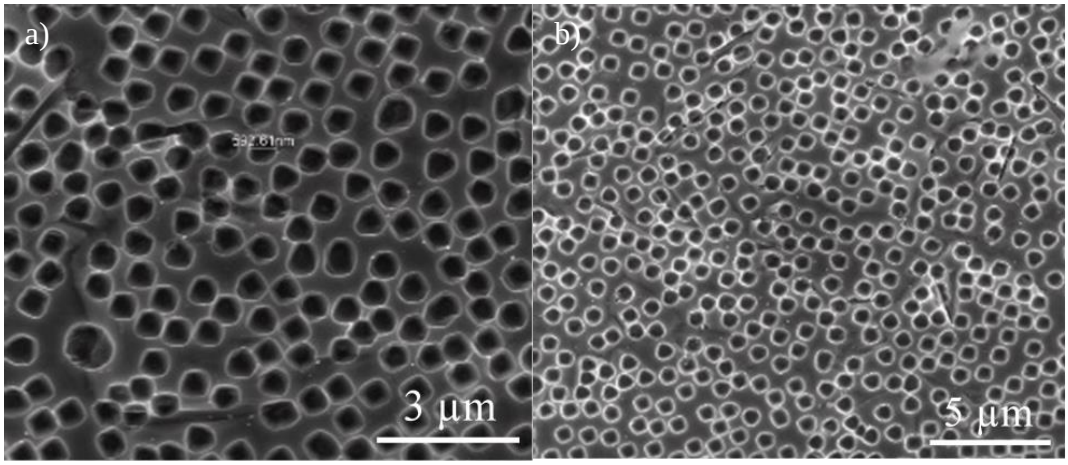


Figure 2.31 SEM image of HCL applied surfaces with 45 s dry etching. The bead sizes were a) 410 nm and b) 510 nm respectively.

When the surface was covered with smaller beads, the random distribution was not totally covering whole surface like big beads. Figure 2.32 shows dry etching results of the surface covered with 270 nm bead size.

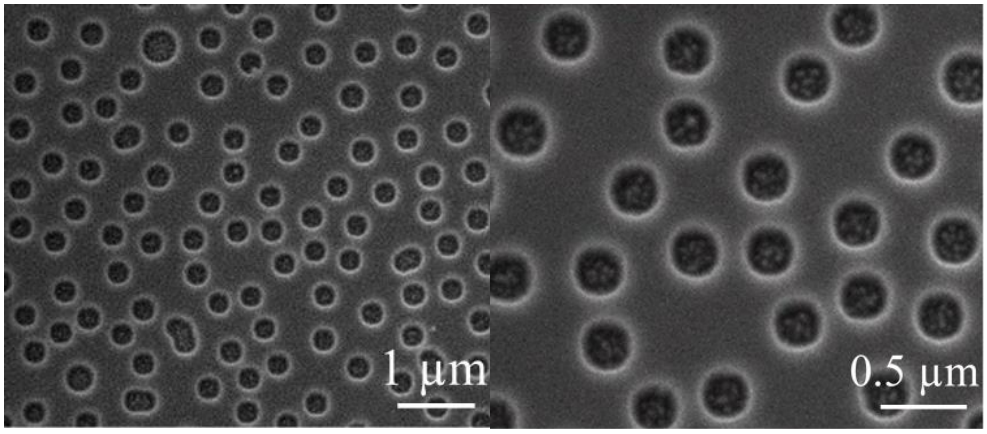


Figure 2.32 SEM image of HCL applied surfaces with 50 s dry etching, the bead size was 270 nm

HCL patterning can also be applied to thinner surfaces. The core part of this study is to work with thin wafers, epifoils. 40 µm thick epifoils were shown to be best selection for solar cell fabrication [98,99]. In Figure 2.33, it can be seen that for 510 nm bead sizes, 45 s dry etching ended up with some intersection of beads. During dry etching process we could manage to work with thin epifoils. There hadn't been any detachment, due to vacuum process step during lithography. Thanks to HCL random pattern transfer technique and well surface coverage.

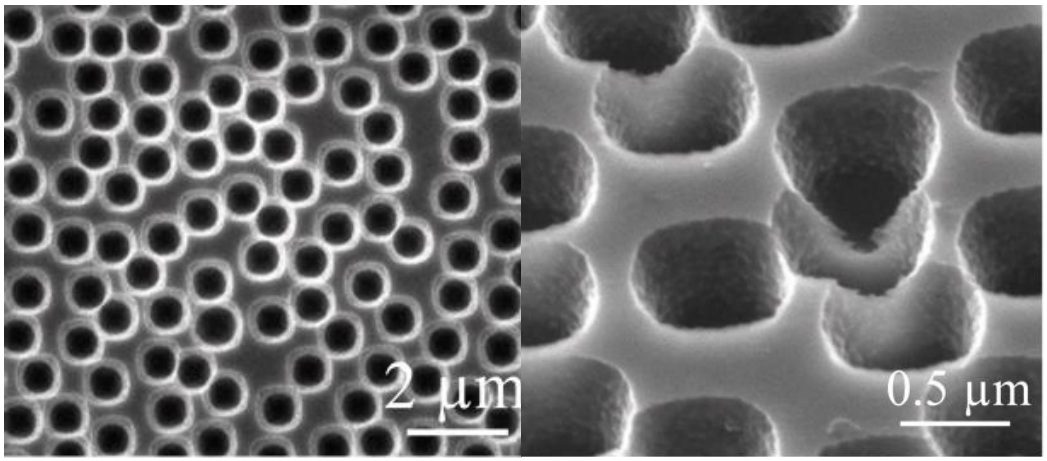


Figure 2.33 SEM image of HCL applied to 40 µm epifoils with 45 s dry etching, the bead size was 510 nm

It can be seen from SEM images that surface textures are almost similar with periodic patterning achieved with lithography based techniques. The only difference is, for HCL the position of nanostructures is depending on the bead position and diameter. Bead to bead and bead to surface reactions will differ depending on initial bead size. The defining criteria for bead size and position are defined with dry plasma etching conditions. The larger the initial bead size, the larger the final structure size. The sizes of features are depicted in Table 2.25:

Table 2.25 Initial bead sizes and final dimension of features obtained with dry plasma etching

Bead size (nm)	Etching time (s)	Final dimension (nm)	Depth (nm)
270	50	550	450
410	55	760	550
510	55	900	600

After pattern transfer with HCL either wet or dry etching techniques can be selected. During wet anisotropic etching we used tetramethylammonium hydroxide (TMAH). What we first did was to get rid of residual resist layer and initiate etching for inner side of structures using dry etching. O_2 plasma and SF_6 RIE would be the best dual action for this process. The samples were coated with OBDUCAT resist, which was thicker than NIL applied surfaces. OBDUCAT didn't use PDMS, their soft stamp

was much thinner than ours, and the size was 10x10 cm^2. Larger soft stamp size is more challenging than smaller sizes as mentioned in Chapter 2. Our dry, and wet etching recipes were:

Wet I : O_2 plasma, 50 W- 50 mTorr- 50 sccm- 20 s

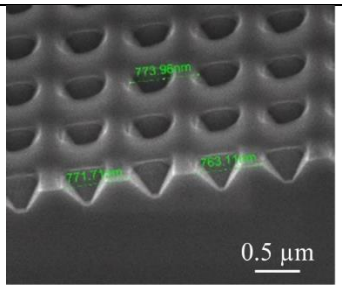
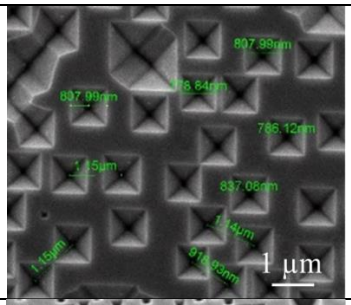
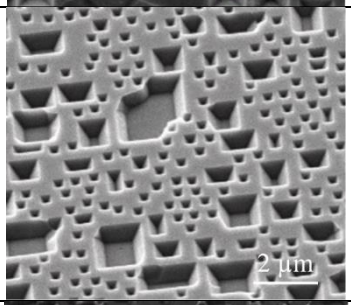
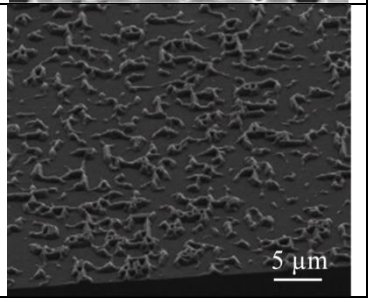
SF_6 RIE, 100 W- 100 mTorr- 30 sccm- 10 s

Wet II : O_2 plasma, 50 W- 50 mTorr- 50 sccm- 40 s

SF_6 RIE, 100 W- 100 mTorr- 30 sccm- 15 s

H_2O : TMAH = 3 : 2

Table 2.26 Wet TMAH etching comparison between NIL and HCL applied surfaces

SEM image 40 µm epifoil on mono c-Si 800 nm pitch size, with OBDUCAT resist Dry etching+ Wet I @ 60 °C , 55 s TMAH etching	
SEM image epifree on mono c-Si 630 nm bead size Dry etching+ Wet I @ 80 °C , 6 min TMAH etching	
SEM image 40 µm epifoil on mono c-Si 270 nm pitch size, with OBDUCAT resist Dry etching+ Wet I @ 60 °C , 1 min 30 s TMAH etching, 5 s O_2 plasma	
SEM image 40 µm epifoil on mono c-Si 150 nm pitch size, with OBDUCAT resist Dry etching+ Wet I @ 60 °C , 1 min 48 s TMAH etching, 5 s O_2 plasma	

When wet chemical etching results of NIL and HCL applied surfaces were compared in Table 2.26. It can be seen that insufficient etching duration ended up with almost any textures on top of the surface. NIL ended up with a very uniform distribution with full surface coverage.

TMAH at 80 °C caused 40 µm epifoils to extract, which is undesired. Lower process temperatures let us work with thinner substrates. The most difficult parts of working with thin foils were handling and processing, and when wet etching combined with these two challenges, the situation gets more complicated. For HCL, the beads and the mask could survive with the wet etching process. In Figure 2.26, wet TMAH etching comparison made between NIL and HCL samples. Insufficient etching time ended up with unexpected surface patterns. The temperature and the duration are the most crucial parameters for wet anisotropic etching method. Each pitch size for NIL and bead size for HCL ended up with different depths and distribution depending on process type and duration. Fabricated periodic and disorder introduced periodic features that are optically evaluated in section 2.4.2.

2.5.3 Comparison of HCL and NIL in Terms of Optical Properties

Both HCL and NIL patterned surfaces were well patterned when correct process conditions were defined, starting with required resist thickness, till the end of whole etching sequence. Each step was connected to each other. For NIL patterning continued with MAE technique the core part is correct lift off, after this step one can proceed with correct process conditions ending up with desired topography.

When we investigated surfaces patterned with HCL and NIL we can say that some surfaces had reflection values lower than pyramid texturing. Figure 2.34 shows the reflection values of surface patterned with NIL and 25 nm silver was coated for MAE. The stamp was having 800 nm pitch and 550 nm diameter subjected to two different wet chemical etching duration and two different oxygen plasma descum time. As the etching time increased, we can see the decrease in reflection, and 5 s of plasma descum gave the best result.

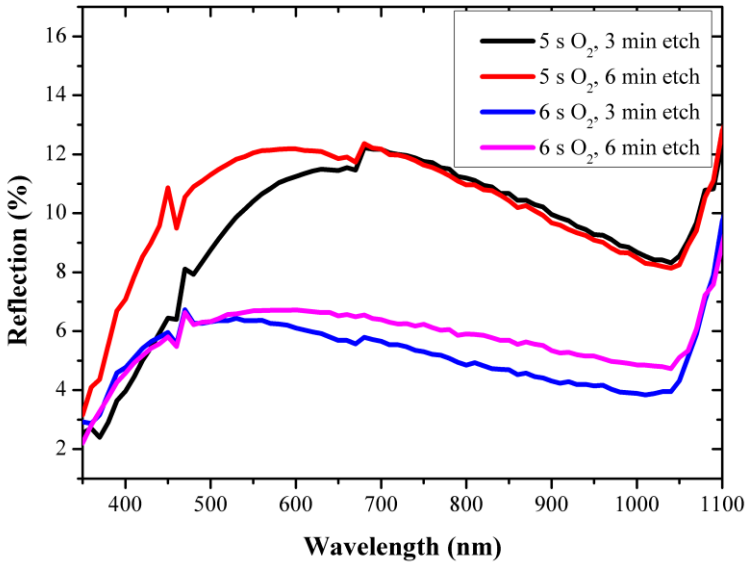


Figure 2.34 Reflection data of surface having nanostructures after 25 nm Ag evaporation and 3-6 min MAE applied with two different plasma descum time

When the coated metal layer was changed with titanium and gold, after NIL patterning, MAE step was also successfully achieved and uniform distribution was managed. The reflection values shown in Figure 2.35 were lower than pyramid texturing, but not lower than Ag assisted wet chemically etched surface.

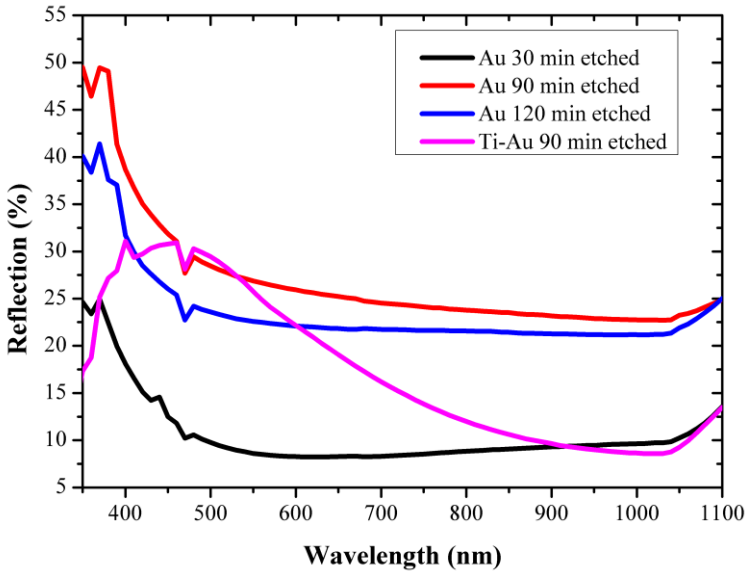


Figure 2.35 Reflection data of surface having nanostructures after 4 nm Ti and 20 nm Au evaporation and 30- 90- 120 min MAE applied with the same plasma descum time

There have been many parameters that could be changed to obtain various surface textures and pattern distribution. Depending on pattern transfer process and etching sequence, final form of textured surfaces were investigated.

Process details were analyzed depending on substrate type, bead size for HCL, stamp dimensions for NIL and either dry plasma or wet chemical etching selection. In order to define bead and pitch size of unique dimension with one expression, we used "phi" for the dimension. Table 2.27 summarizes process details and name of the samples subjected to HCL and NIL pattern transfer.

Table 2.27 Process details and wafer characteristics of the surface patterned with HCL and NIL

Wafer ID	Type	Phi (nm)	Process Details
a	epifree, Al, NIL (obducat resist)	680	40/ 50/ 180 s
b	epifree, Al, NIL(obducat resist)	680	40/ 50/ 180 s
c_1	epifree, no Al, HCL	270	100 mTorr/ 100 W/ 100 sccm – 45 s
c_2	epifree, no Al, HCL	270	100 mTorr/ 100 W/ 100 sccm – 35 s
d_1	epifree, Al, HCL	270	100 mTorr/ 100 W/ 100 sccm – 45 s
d_2	epifree, Al, HCL	270	100 mTorr/ 100 W/ 100 sccm – 35 s
e	poly Si, HCL	410	100 mTorr/ 100 W/ 100 sccm – 45 s
f	poly Si, HCL	510	100 mTorr/ 100 W/ 100 sccm – 45 s

Substrate types are divided into two groups as shown in Figure 2.29, there are aluminum and glass between thin epi layers, or not. Depending on Al abundance, after etching step removal of this intermediate Al layer was required. We have set a process matrix before starting our etching step. For the same bead sizes, depending on the available number of samples, we changed etching process time. Figure 2.36 shows the reflection data of c_1 and c_2 samples patterned with HCL, having 270 nm bead size and subjected to dry plasma etching. With the increase in etching time, lower reflection value was expected.

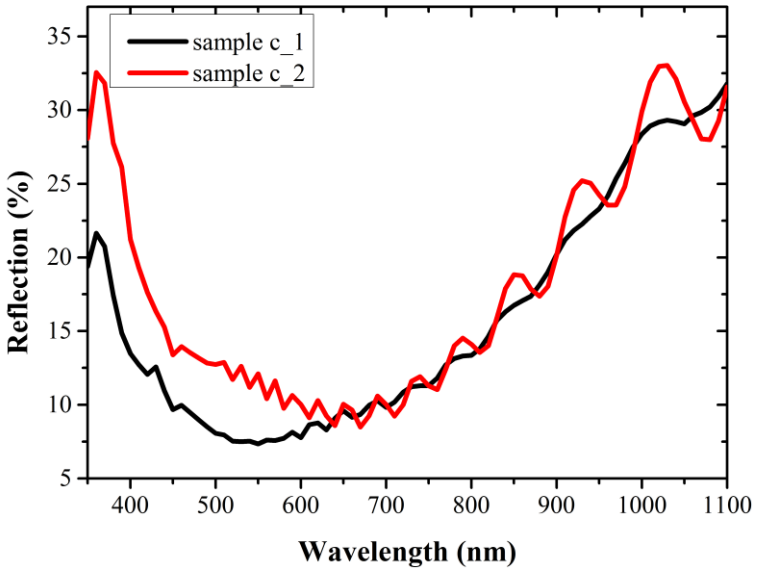


Figure 2.36 Reflectance curves of periodic nanostructures obtained with dry plasma etching

When we make a comparison between HCL and NIL patterning technique, we can conclude that NIL patterned surfaces have slightly lower reflection values. Figure 2.37 represents the reflection values of surfaces having process parameters tabulated in Table 2.27 and Figure 2.43 represents the average reflection values of the surfaces.

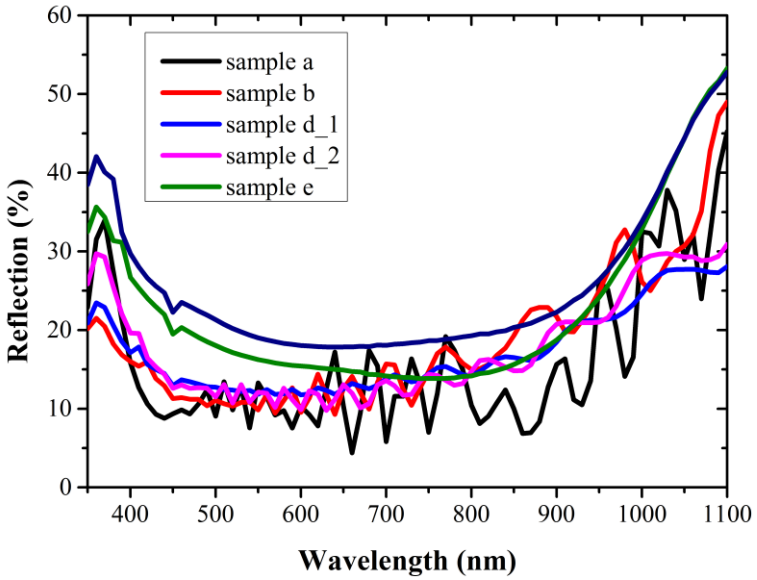


Figure 2.37 Reflectance curves of periodic nanostructures summarized in Table 2.27, obtained with dry plasma etching

When we consider the transmission values of the samples, whose process details summarized in Table 2.27, Figure 2.38 shows their transmission curves after dry plasma etching.

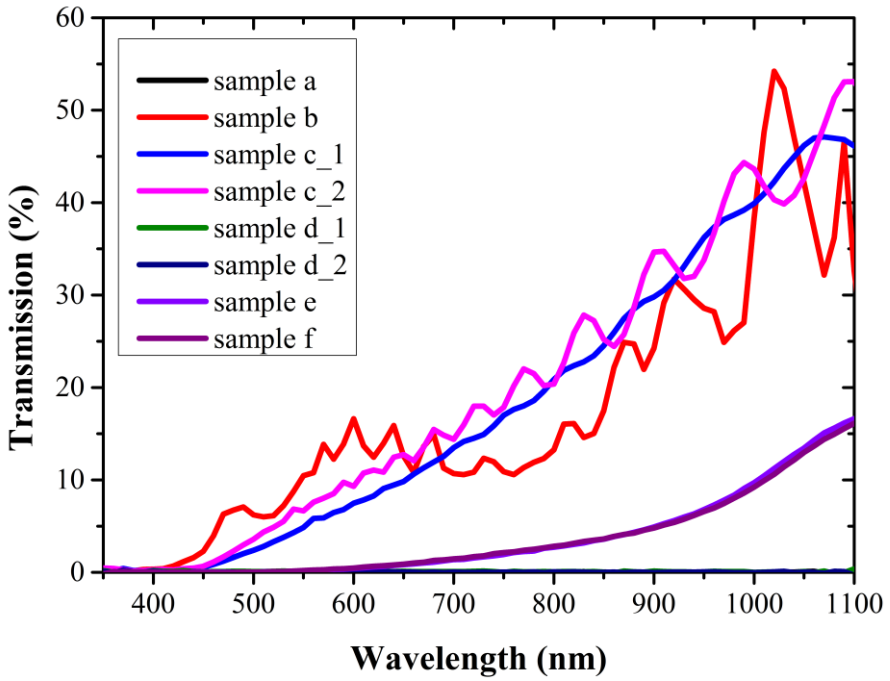


Figure 2.38 Transmission curves of periodic nanostructures summarized in Table 2.27, obtained with dry plasma etching

To summarize our optical analyses of samples patterned with NIL and HCL, which are subjected to same dry plasma etching process sequence in terms of process conditions, only the time was varied, the best optical results were obtained with NIL patterned sample, and the pitch size of the stamp was 680 nm, which corresponds to sample a in Table 2.27.

In addition to dry plasma etching, we have done wet chemical etching to surfaces patterned with NIL and HCL. The substrates that we have worked were thick and 40 µm thin epifoils bonded to glass with silicone. Both types of substrates were patterned with different bead sizes for HCL. Table 2.28 summarizes our substrates, patterned with HCL having different phi values and wet chemical etching duration.

Table 2.28 Substrate details patterned with HCL and subjected to wet chemical etching

Wafer ID	Type	Phi (nm)	Temp (°C)	Dry etching	Wet etching
p	HCL	410	60	5 s SF_6/O_2	4 min 10 s
q	HCL	510	60	X	7 min
r_1	HCL	270	60	X	8 min
r_2	HCL	270	60	X	14 min
r_3	HCL	270	60	5 s SF_6/O_2	8 min
r_4	HCL	270	60	5 s SF_6/O_2	6 min
s	Epi-HCL	270	60	5 s SF_6/O_2	1 min 30 s
t	Epi-HCL	150	60	5 s SF_6/O_2	1 min 48 s
w_1	HCL	850	80	X	6 min
w_2	HCL	850	80	X	5 min 30 s
x_1	HCL	630	80	X	6 min
x_2	HCL	630	80	X	5 min 30 s
y_1	HCL	270	X	SF_6-O_2-100 W	40 s
y_2	HCL	270	X	SF_6-O_2-100 W	45 s

Some of the samples were subjected to dry plasma etching, followed by wet chemical etching. The reason of this initial dry plasma etching was to accelerate wet etching. For HCL, we had beads on top of the surface, which were needed to be immersed in substrate resulting with etching. It can be seen that, the samples having short dry plasma etching required shorter wet etching duration. Dry plasma etching provided beads to immerse inside the surface, hence shorter duration was enough for the samples subjected to this process.

After our experiments, we have checked the uniformity of the HCL patterned surfaces, for some of the samples subjected to wet chemical etching, we could partially manage to obtain uniform distribution of intended patterns. In order to distinguish the effect of uniformity on optical performance, we have carried out reflection measurements from different parts of sample y_1 patterned with 270 nm bead and 40 s wet TMAH etching applied. As shown in Figure 2.39, almost there is 40% difference of reflection values of different parts of the sample. The effect of patterning could be seen by naked-eye also, the shiny part, having the highest reflection, had no pattern.

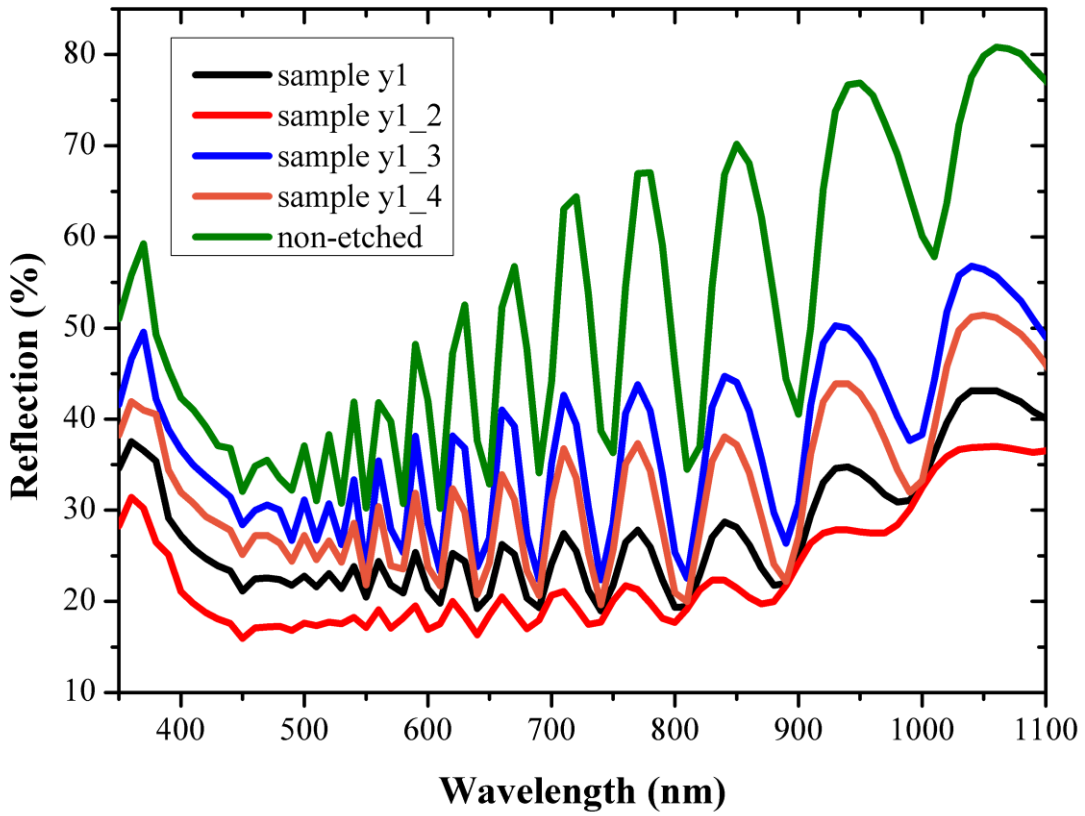


Figure 2.39 Reflection of HCL patterned sample, y_1, 270 nm bead, having 40 sec TMAH wet etching (Sample description is given in Table 2.28)

Reflection data observed from HCL applied surfaces shows us a very nice representation of Fabry-Perot interference pattern for wavelengths larger than 550 nm, which corresponds to the penetration depth of 1 µm c-Si. This means that there is an interaction with photons and the back side of the slab. The interaction between downwards wave and the upwards wave after being reflected back from the rear interface will end up with a maxima and minima in intensity [104,105]. Not all of HCL patterned samples gave this trend, sample r with the same bead size had reflection values as shown in Figure 2.40. We have applied four different etching durations for sample r, as shown in Table 2.28. We could say that 5 s of dry plasma etching followed by wet chemical etching ended up with uniform distribution and lower reflection values compared with bare wet etching sequence.

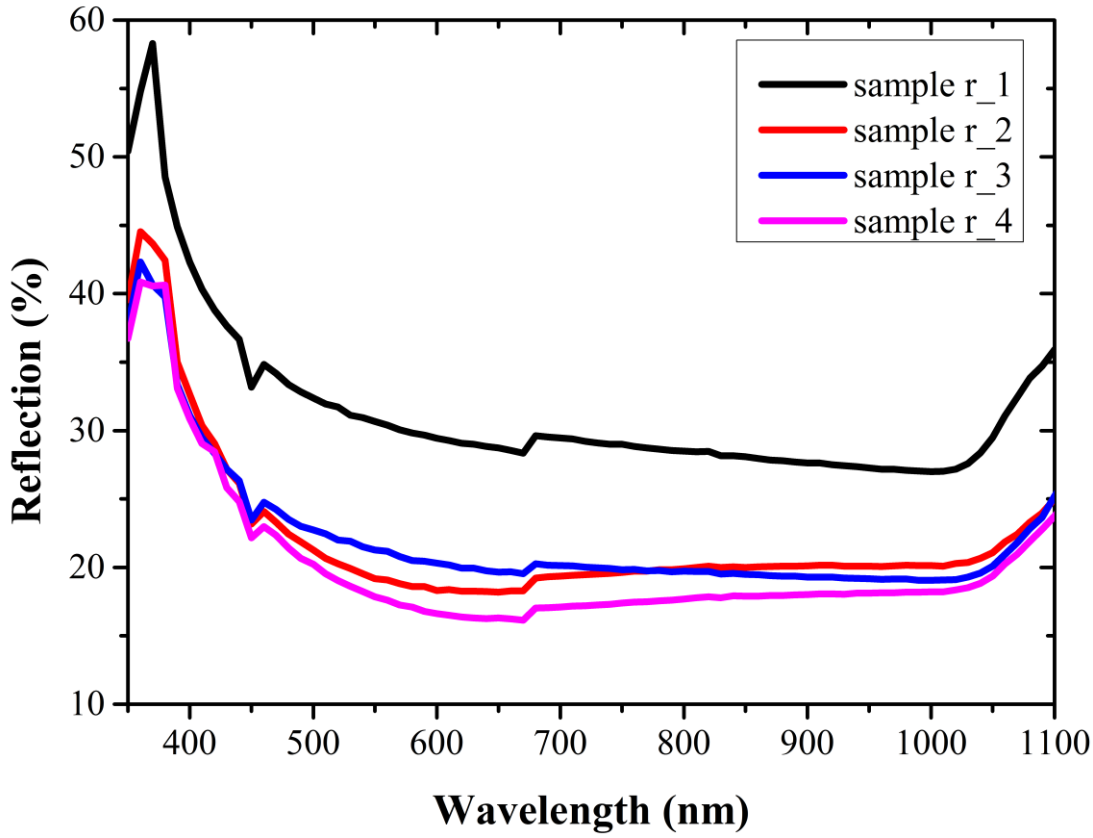


Figure 2.40 Reflection of r sample having different wet TMAH etching duration and O_2 plasma treatment

When we investigated HCL patterned sample p in terms of absorption (A), reflection (R), transmission (T), we have obtained Figure 2.41.

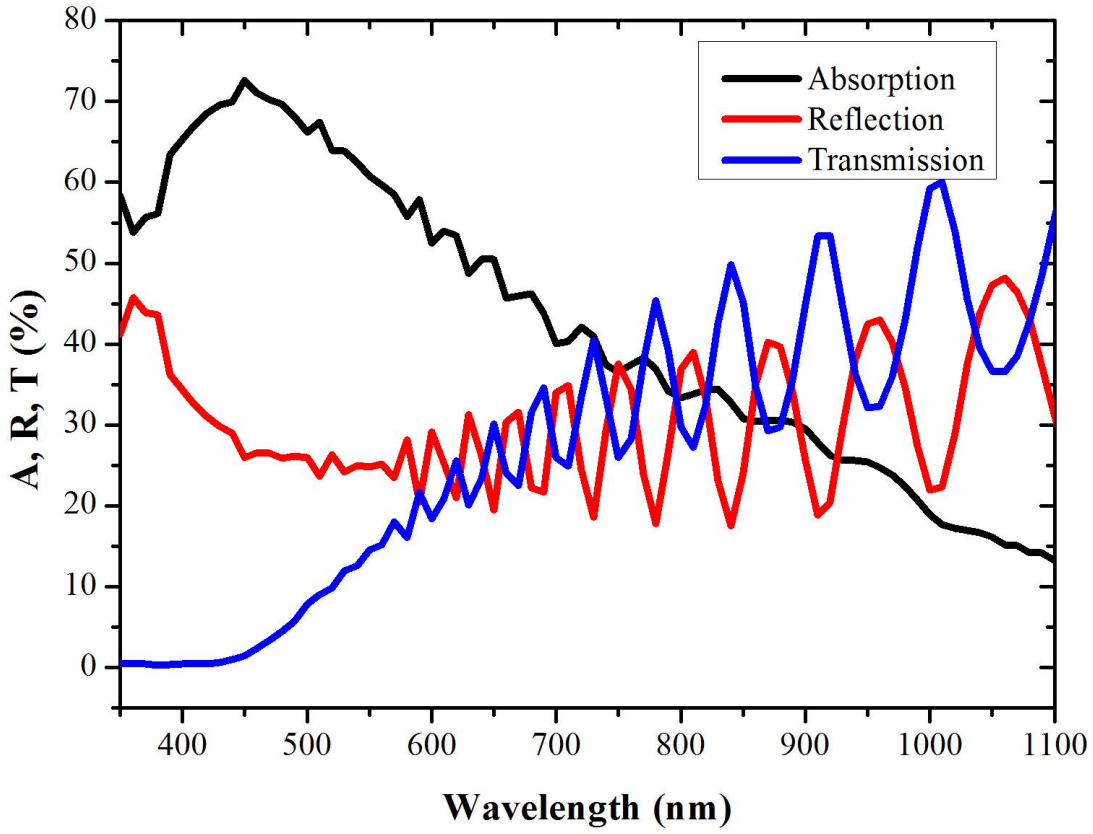


Figure 2.41 Absorption, reflection and transmission spectra of sample p with 410 nm phi

To summarize NIL and HCL patterning we have focused on three samples with the best optical performance as tabulated in Table 2.29.

Table 2.29 Wafer information patterned with HCL or NIL fabricated with wet or dry etching technique

Wafer ID	Phi (nm)	Process
D13	680	NIL – Dry etching
D15	680	NIL – Wet etching
D16	270	HCL (random) – Dry etching

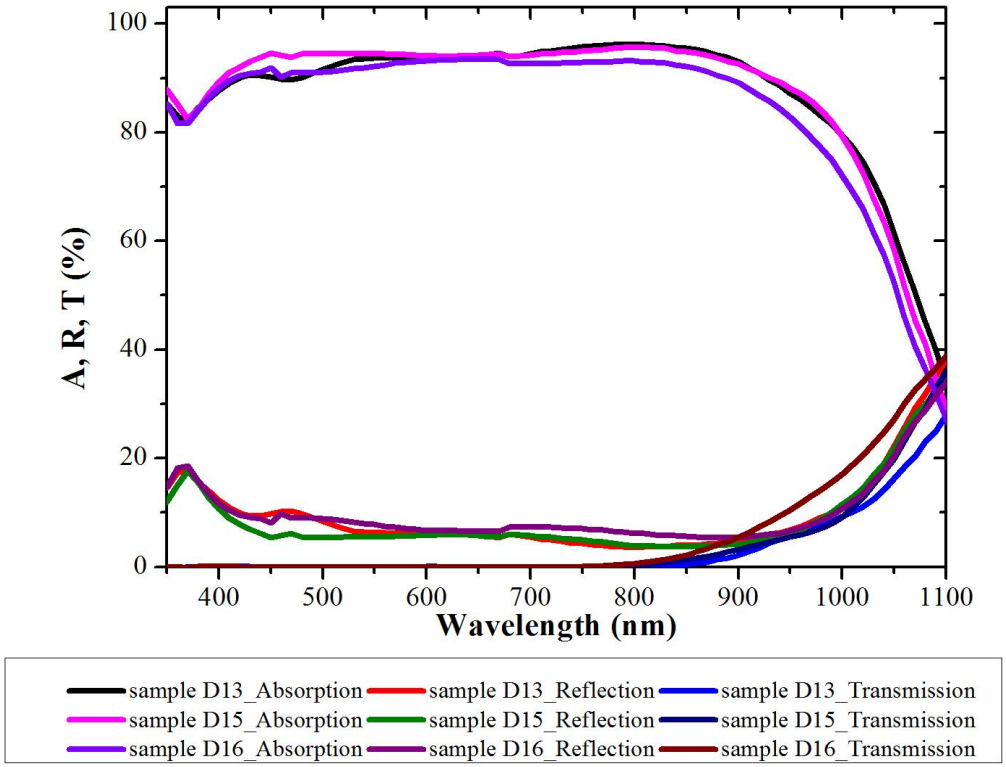


Figure 2.42 A, R, T analyses comparison of NIL and HCL patterned samples, subjected to wet and dry etching

Figure 2.42 shows the best A, R, T values of the surfaces textured with NIL and HCL. Dry and wet etching conditions were optimized depending on phi value and desired depth parameter.

To sum up we have calculated HCL and NIL textured surfaces' average reflection value to make comparison between each samples. Figure 2.43 represents the average reflection values of surfaces patterned with HCL. Sample properties were summarized in Table 2.27 and Table 2.28.

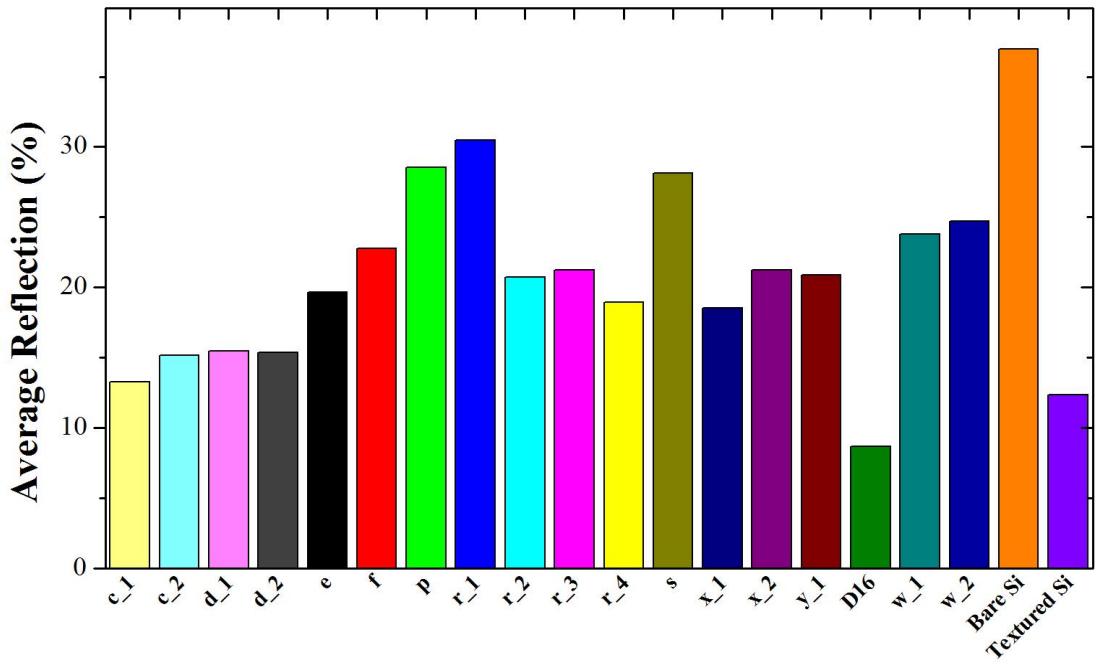


Figure 2.43 Average reflection comparison of samples patterned with HCL having different bead sizes and etching conditions

From Figure 2.43, it can be seen that D16 having 270 nm bead size, subjected to dry plasma etching and oxygen plasma descum had lower reflection values than standard pyramid textured surface.

To make a comparison between NIL patterned surfaces we have plotted average reflection values patterned with imprinting process, subjected to wet and/or dry plasma etching process. Figure 2.44 represents the average reflection values of surfaces patterned with NIL stamps having different pitch and diameter sizes with different etching parameters. The process details of samples represented here were summarized in Table 2.27 and Table 2.28.

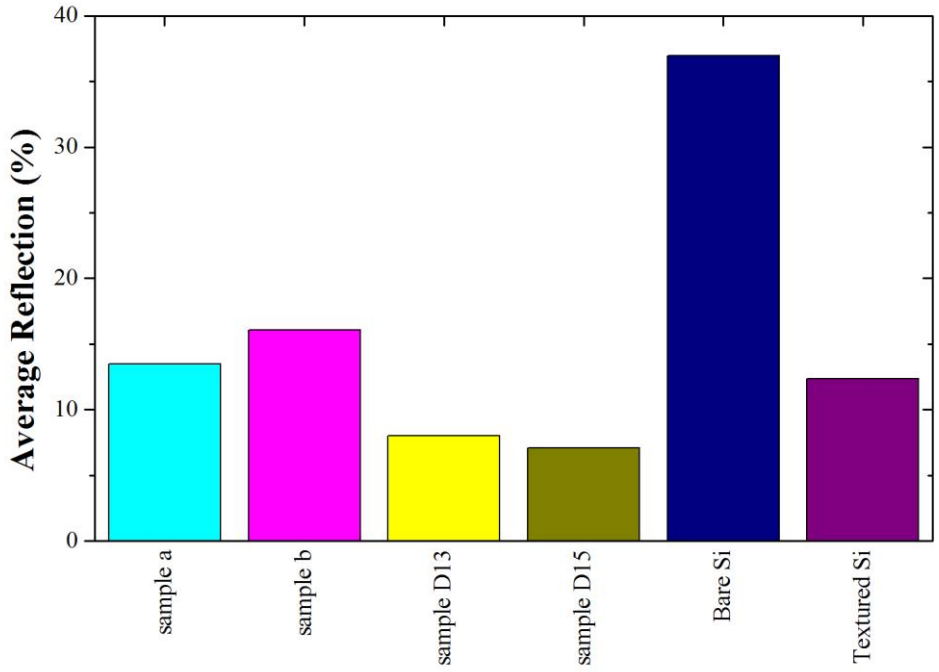


Figure 2.44 Average reflection comparison of samples patterned with NIL having different pitch sizes and etching conditions

We can see from Figure 2.44 that the lowest reflection value was obtained from the sample having 680 nm pitch size subjected to wet chemical etching, D15. D13 had also lower reflection value than standard pyramid textured surface. For NIL, both dry and wet etching process showed remarkable optical performance. With SiNx coating, these results can be further improved.

2.6 Summary of Patterning Techniques for Light Trapping on Si Surface

In this chapter we have discussed a large variety of surface topographies obtained with lithography tools having different capabilities. We have achieved periodic structures and random textures with the help of lithography based process sequences. Besides lithography, the basic experimental procedures of wet and dry etching techniques were optimized for each method.

Although there have been many research groups working on lithography-free surface texturing techniques, it is impossible to control the surface patterns obtained with random textures. The limited control on the morphology of surface will end up with insufficient light trapping. Black silicon, which is one of the most favorable studies of solar cell technology, shows perfect light in-coupling property, but poor

light trapping when compared with periodic textures. Experimental results supported with simulation studies focus on periodically patterned surface textures combined with random textures.

The most controlled micro or nano holes on the surface were obtained through lithography followed by dry plasma etching sequence. Reactive ion etching (RIE) allowed us to obtain very deep and uniform holes on silicon surface, resulting in lower reflection values compared to bare wafer. The main drawback for RIE applied wafers is the process cost. Although RIE provided us very uniform surface patterns and a good control on the topography of the surface, it is still not available for batch process during solar cell fabrication.

The other method that we have expressed in detail was metal assisted etching (MAE), which has lower process cost than RIE and available for mass production. The main drawback of MAE is the consumption of detrimental chemicals during etching step, all the reactions occur in clean room environment and the removal of metals also requires special chemical compositions. When compared with RIE method, samples prepared with metal assisted etching method has given much lower reflection due to unintentionally occurred random nano wires in periodically patterned hole textures, which ended up with light coupling and light trapping on top of the surface towards into the textured surface.

Patterning with nanoimprint lithography (NIL) followed by wet or dry etching have been tried with different pitch sizes and diameters. For each parameter we developed unique process guideline to obtain desired surface topography. Each step was conducted carefully not to end up with unintentional patterns. Different etching approaches are applied after pattern transfer, depending on substrate properties (type, thickness). Because of the handling problem of thinner substrates, glass was used as handling substrate. For dry plasma etching, the most important criterion was the pressure of the chamber, especially for thin surfaces bonded to glass. High vacuum ended up with the separation of NIL applied layer from handling substrate. For wet etching, limitations were the same. In chemical solution also bonded thin substrate might be separated from the handling glass. After defining optimum etching parameters, it was possible to obtain uniform textures with desired patterns. For NIL, we tested the multi usage of soft stamp to decrease process cost and use the time efficiently. NIL patterning followed by either dry or wet etching process sequence

gave promising results, but to be applicable for batch production in photovoltaic world, significant improvements are needed.

Hole colloidal lithography (HCL), using the direct surface self-assembly of colloids by electrostatics, followed by dry or wet etching gave the highest surface coverage ratio. Depending on bead size and etching process parameters, we could manage to obtain surface patterns with desired hole fraction. However, our topographies obtained with HCL patterning is not an effective surface texturing method. When the random textures obtained with HCL were combined with periodically patterned NIL applied surfaces, we got the most conformal patterning surfaces. For HCL, depending on the thickness of the wafer to be etched, process optimizations should be done carefully.

The advantages and disadvantages of each technique were expressed in this chapter. Each mask requires unique process optimizations to end up with desired surface patterns, if not fulfilled, process ends up with undesired surface morphology. Apart from process trials at first stage, we could manage to provide a good control over the distribution of textures with intended depths.

Disclaimer: It should be noted that the lithography part with HCL was performed at Chalmers University, while the etching step of HCL applied surfaces and NIL patterning were performed at IMEC as part of the European project PhotoNVoltaics [106].

CHAPTER 3

MODDELLING AND SIMULATON STUDIES OF SOLAR CELLS WITH PATTERNED SURFACES

Simulation studies were done with Silvaco software. Silvaco as a tool for simulation enables physical etching and depositions process, calibration of doping profiles, optical and electrical simulation for solar cell, charge resulting from holes and electrons freed by an ionizing particle and collected at a junction or contact, total dose and stress simulation. Silvaco enables both device and process simulations. Athena as a sub-modul of Silvaco lets one make 1D and 2D process simulations. The process type can be deifned by user. In order to define the structure file, user can use either Athena or Devedit tool as represented in Figure 3.1. 2D and 3D device definition can be done either with Atlas or Devedit tools. In this thesis both Atlas and Devedit were used to define our devices with hole-textured surfaces. The final plots are obtained with Tonyplot interface, which enables to analyze outcomes visually [107].

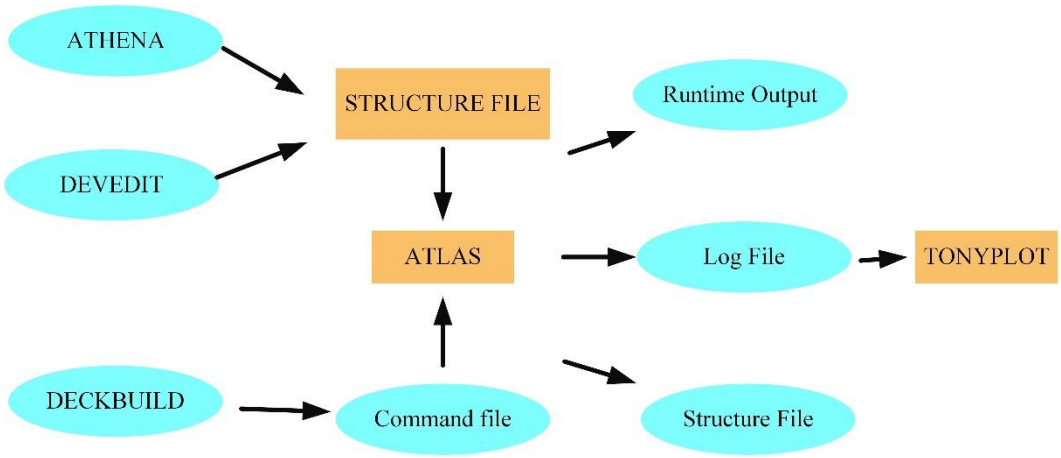


Figure 3.1 Schematic representation of SILVACO software working algorithm

3.1 Simulation Approach and Methodology

Optoelectronic devices are simulated both optically and electrically. Ray-tracing is most commonly applied method for the modelling of passive optoelectronic components. Optical ray tracing calculates the optical intensity at each grid point or at each DC bias point using the real part of refractive index. Absorption or photogeneration model, which are using the imaginary component of refractive index, calculate the new carrier generation at each grid point. The optical simulation is then followed by the electrical simulation using Luminous, S-Pisces or Blaze modules. Luminous, which is an advanced device simulator specially designed to model light absorption and photogeneration for semiconductor devices, assumes that both real and imaginary parts of the refractive index are constant. Mono-chromatic or multi-spectral sources can be simulated with Luminous.

With ray-tracing, rays originating at the external light source are traced into the device and are absorbed to form electon/hole pairs, which are subsequently detected. The parameters that were defined for simulation would define the results with ray tracing. Reverse simulation method starts with desired performance target and adopt the coden depending on outcomes. Unlike direct raytracing, in the reverse method rays originate inside the active region and traced until they exit the device. Rays can be defined depending on user either one or multiple origin points. For the common source point, interference effects can be taken into account. As long as interference is enabled, the spectral selectivity of the device structure can be analyzed by performing ray-tracing at multiple wavelengths.

The finite-difference time-domain (FDTD) method works by direct solution of Maxwell's equations in the time domain and thus explicitly accounts interference and diffraction in 1, 2 or 3 dimensions. FDTD use the same method as for ray tracing in that the emission from a set of dipoles located at user specified locations is integrated/averaged over the device.

3.2 Modelling of Solar Cells with SILVACO

Semiconductor device physics is composed of a set of fundamental equations, which were derived from Maxwell's laws.

1) Poisson's equation, shown in Equation 3.1, relates variations in electrostatic potential to local charge densities.

$$div(\varepsilon \nabla \psi) = -\rho \tag{3.1}$$

ε: local permittivity

ψ: electrostatic potential

ρ: local space charge density

2) Carrier continuity equation which is defined for holes and electrons as shown in Equation 3.2 and 3.3.

$$\frac{\partial n}{\partial t} - \frac{1}{q} div\overrightarrow{J_n} = G_n - R_n \tag{3.2}$$

$$\frac{\partial p}{\partial t} + \frac{1}{q} div\overrightarrow{J_p} = G_p - R_p \tag{3.3}$$

where:

- n and p are the electron and hole concentration
- $\overrightarrow{J_n}$ and $\overrightarrow{J_p}$ are the electron and hole current densities
- G_n and G_p are the generation rates for electrons and holes
- R_n and R_p are the recombination rates for electrons and holes
- q is the magnitude of electron charge

In some cases solving one carrier continuity equation is sufficient.

3) In order to specify physical models for J_n, J_p, G_n, G_p, R_n, R_p secondary equations are needed to be defined. The current density equations, mostly obtained with approximations to the Boltzmann Transport Equation, define the transport model. These models are:

- Drift-diffusion model
- Energy balance model
- Hydrodynamic model

The simplest and most preferred model is the drift-diffusion model as shown in Equation 3.4 and 3.5.

$$\overrightarrow{J_n} = qn\mu_n\overrightarrow{E_n} + qD_n\nabla_n \tag{3.4}$$

$$\overrightarrow{J_p} = qp\mu_p\overrightarrow{E_n} + qD_n\nabla_n \tag{3.5}$$

where:

- μ_n and μ_p are the electron and hole mobilities
- $D_n = \frac{K_B T_L}{q}\mu_n$, $D_p = \frac{K_B T_L}{q}\mu_p$ are the Einstein relationships
- $\vec{E}$=-∇_ψ is the electric field.

For our solar cell simulations ray-tracing method was used. To start ray-tracing from one point of origin the user has to specify the following parameters: coordinates of the origin of rays **X** and **Y** and wavelength **L.WAVE**. It is important that the origin be chosen in the active region of the device. Rays are not traced if the radiative recombination is zero at the ray origin.

"Reflects" parameter defines the number of reflections to be traced for each ray originating at the points X, and Y. The default value (REFLECTS=0) provides for a quick estimate of the coupling efficiency. REFLECTS>0 should be used to obtain a more accurate result. The choice of this parameter is based on a compromise between calculation time and accuracy. The maximum allowed value is REFLECTS=10. The number of reflections set to 3 or 4 is often a good choice.

The rays are assumed to be incoherent by default. This is a good approximation if the thickness of the active layer of the device is on the order of a wavelength/index. For layer thicknesses << wavelength coherent effects might be important. When the "interfere" parameter is set, the rays originating at the common source point are taken to be 100% coherent. In this case the phase information upon propagation is preserved. Phase change upon reflection is also considered. Thus, interference of rays exiting the device at the same angle is taken into account. The internal angle information is not written to the output rayfile in this case.

Although ray-tracing from one point of origin can give a reasonable estimate of optical output and angular distribution of light power, it is often desirable to

consider multiple points within the active layer of the device to obtain more accurate results. Multiple origin points can be set using the following parameters:

XMIN, XMAX, YMIN, YMAX define a rectangular area containing all origin points. XNUM and YNUM specify the number of points along x- and y- axes within the rectangular area. If XNUM is equal to 1, the x-coordinate of all origin points is set to XMIN so that the points are chosen along the line x = XMIN. Similarly, points along the specific y-line can be chosen. Ray-tracing from multiple origins is realized by repeating a single origin algorithm for each point and by adding up the normalized angular power density values thus obtained. The luminous power assigned to each source (origin) is proportional to the radiative recombination at that point. Luminous power of all sources adds up to the value obtained by integration of radiative recombination over the entire device.

3.3 Modeling of Solar Cell Structures: Expected Geometry of p-n Junction and Corresponding Carrier Generation

Solar cell is basically a p-n junction device. In order to figure out how silvaco behaves with p-n junction, we simply created a device and analyzed the effect of doping and dark IV curves as shown in Figure 3.2 and Figure 3.3. It is possible to create a p-n junction either with process tool Athena or device tool Atlas with Silvaco. In this example we have used Athena process tool, and used highly doping levels to extract the optical and electrical properties of the device. The junction depth was obtained at 650 nm from the surface which is close to real doping profile. In order to extract desired parameters we have used Luminous, which is one of the most useful tools of Silvaco, providing special parameter extraction that are unique to optoelectronics such as junction depth,concentration, temperature and electric field dependent mobilities, concentration dependent mobilities.

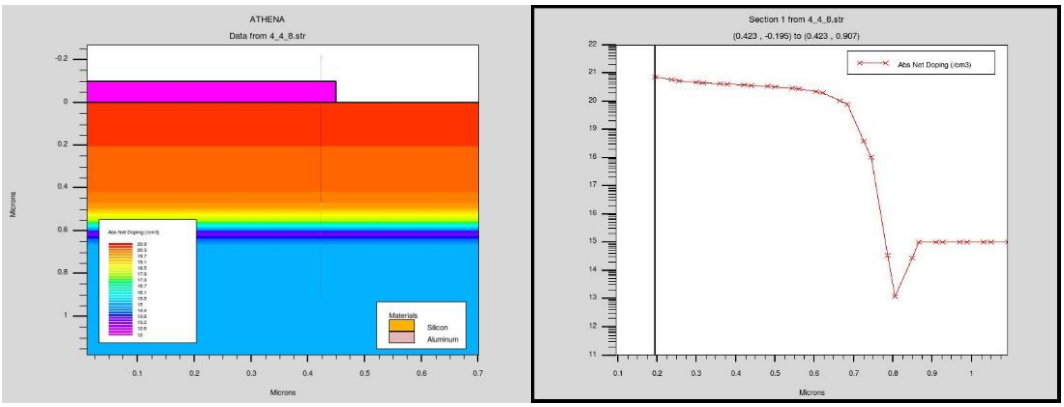


Figure 3.2 Net doping concentration profile and junction depth information of a p-n junction obtained with Athena process tool

When the simulation is finished and the output files are saved, it is possible to extract any results related to predefined and simulated structure. The output files that are saved in .str extension format lets us get related data with our device. Figure 3.3 shows dark IV characteristic of a p-n junction obtained with process tool Athena.

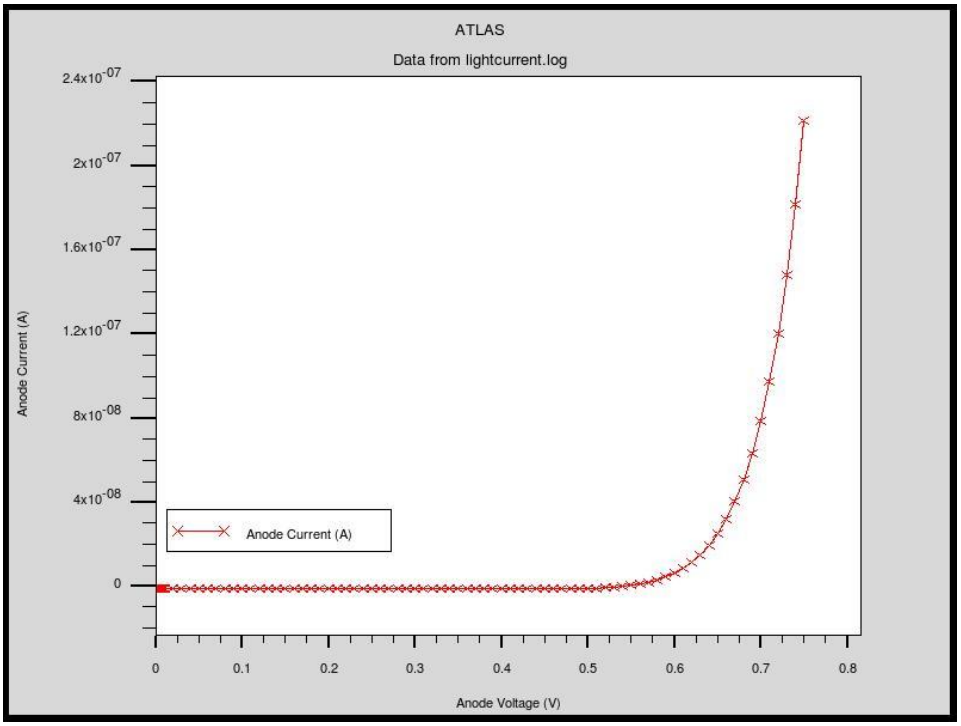


Figure 3.3 Dark IV characteristic of a p-n junction obtained with Athena process tool

3.4 Simulation of Patterned Structures

Patterning crystalline silicon surface could be done either by process or device tools of Silvaco. In order to obtain devices as close to the real case, we have used Athena process tool and defined necessory parameters which can give the best results for our textures. Depending on the models that have been defined by the user, Silvaco treats the device as occuring from grid point and make the solutions for each grid point. The most important point for defining the device is the mesh distribution. The program can adopt the mesh automatically, reducing the simulation time. At some points this mesh refinement may be helpful, but when we define textures, meshing should be dense enough to let the program beware of our textures. In Figure 3.4 3D bare and textured surfaces can be seen. With Devedit3D, it is possible to create three dimensional surfaces and Tonyplot3D enables us to plot the patterned surfaces.

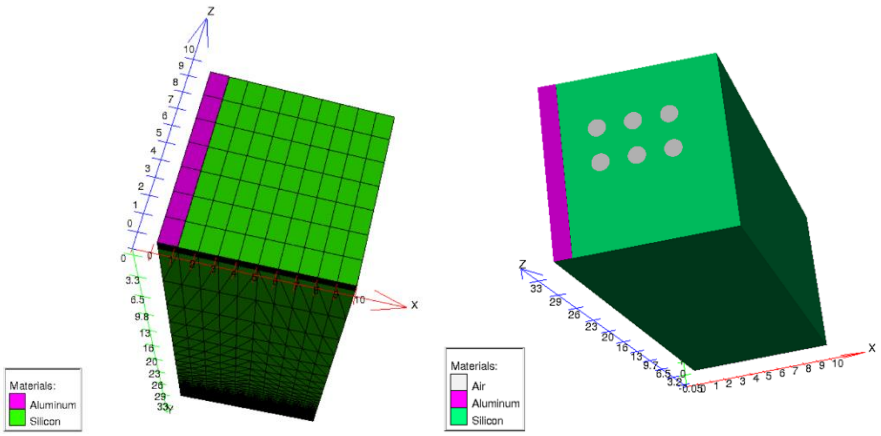


Figure 3.4 3D representation of bare and hole-textured surfaces obtained with Atlas tool

In the case of hole texturing shown in Figure 3.4, two dimensional circles can be obtained. The circles were obtained with 360 mesh points, each point corresponds to an angle and a grid point. One hole texture was defined and then multiplied depending on the dimension of holes and the gap between each hole. Once we defined the diameter and the periodicity of the holes, the depth parameter could be defined.

Table 3.1 Simulated solar cell performances of the surfaces patterned with 3 µm diameter and 1, 2, 3, 4, 5 µm gap between holes with Atlas and Luminous combination.

Diameter (µm)	Gap (µm)	Depth (µm)	Jsc (mA/cm^2)	Voc (mV)	FF	η (%)
3	1	2	24.17	630.76	83.1	12.67
3	2	2	27.02	631.24	83.09	14.17
3	3	2	30.67	632.64	83.1	16.12
3	4	2	34.16	634.24	83.09	18.00
3	5	2	37.53	635.96	83.1	19.84
Flat	-	-	26.87	521.22	79.26	11.3

Performances of the solar cells textured with 3 µm diameter and 1, 2, 3, 4, 5 µm gap holes are tabulated in Table 3.1. It can be seen that there is a direct relation between the gap and cell performance. Figure 3.5 shows the I-V curves of surfaces summarized in Table 3.1.

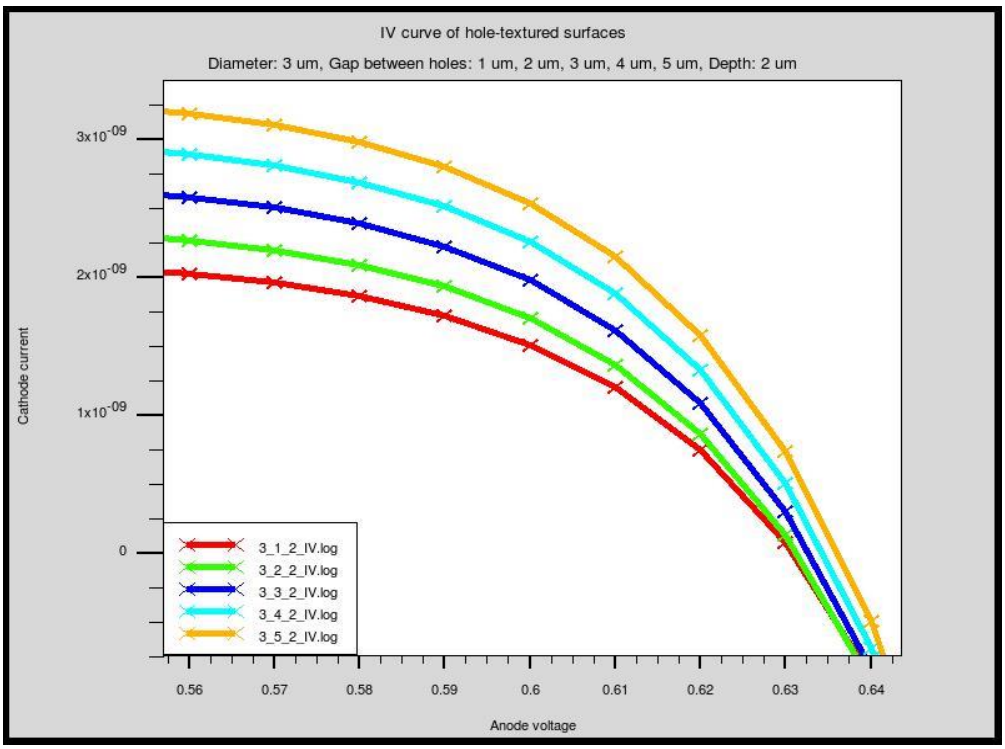


Figure 3.5 I-V curve of textured with 3 µm diameter and 1, 2, 3, 4, 5 µm gap, and 2 µm depth

For periodic hole texturing the parameters that we can change are the diameter of the holes, the gap between holes, which will define the periodicity, and the depth. In order to make better and meaningful comparisons, we kept the gap between holes and the depth constant. The solar cells were created both with process and device tool. The performances of the cells textured with holes having 1, 2, 3, 4, 5 µm diameter, 1 µm gap, and 2 µm depth are shown in Table 3.2.

Table 3.2 Simulated solar cell performances of the surfaces patterned with 1, 2, 3, 4, 5 µm diameter and 1 µm gap between holes with Atlas and Luminous combination

Diameter (µm)	Gap (µm)	Depth (µm)	Jsc (mA/cm^2)	Voc (mV)	FF	η (%)
0.5	1	2	13.58	633.96	83.34	7.17
1	1	2	15.68	632.63	83.27	8.26
2	1	2	19.94	631.32	83.17	10.47
3	1	2	24.17	630.76	83.1	12.67
4	1	2	28.06	630.32	83.02	14.68
5	1	2	31.78	630	82.96	16.61
Flat	-	-	26.87	521.22	79.26	11.3

Figure 3.6 shows the comparison of solar cell performances summarized in Table 3.2. The highest efficiency value was obtained from the surface textured with 5 µm diameter.

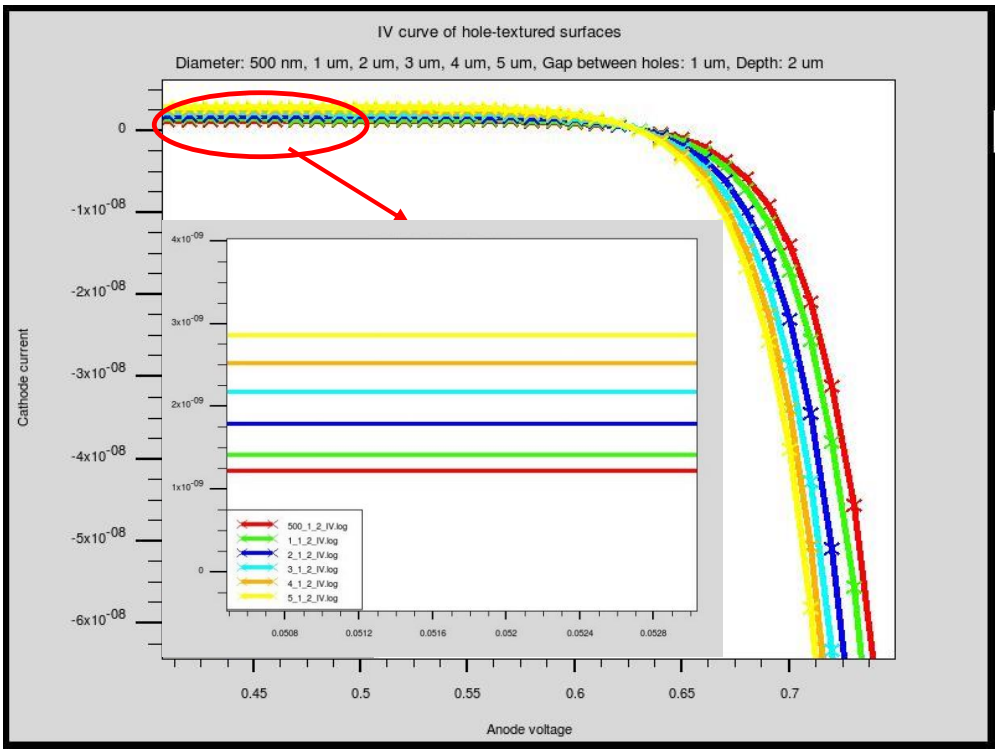


Figure 3.6 I-V curve of textured with 0.5, 1, 2 , 3, 4, 5 µm diameter, 1 µm gap, and 2 µm depth

It can be seen in Table 3.1 and Table 3.2 that the highest efficiency value was obtained with the largest gap and diameter values. In order to make a comparison depending on this information, we patterned the surface with 5 µm diameter and gap varying between 1 to 5 µm. The results represented in Table 3.3 tells us that the largest surface area (which corresponds to largest diameter and gap values) ends up with the best cell performance. For the gap value of 4 and 5 µm, the results seem to be saturated. It can be understood that, there is no need to increase the spacing between two holes.

Table 3.3 Simulated solar cell performances of the surfaces patterned with 5 µm diameter, 1 µm depth and 1, 2, 3, 4, 5 µm gap between holes with Atlas

Diameter (µm)	Gap (µm)	Depth (µm)	Jsc (mA/cm^2)	Voc (mV)	FF	η (%)
5	1	1	31.78	630	82.96	16.61
5	2	1	33.87	626.1	82.82	17.56
5	3	1	34.64	629.52	82.9	18.08
5	4	1	35.54	629.07	82.84	18.52
5	5	1	35.85	628.97	82.79	18.59
Flat	-	-	26.87	521.22	79.26	11.3

Table 3.4 shows the solar cell results obtained with the holes having holes of 3 µm diameter and 1 µm gap in between. The thickness of the p-type c-Si wafer was taken as 100 µm. The doping concentration of the absorber layer, which had a thickness value of 97.5 µm, was 5e16cm^{-3}. The back surface field was taken as 2 µm with a concentration of 5e18cm^{-3}. The emitter region was having a thickness of 500 nm with a doping concentration of 5e18cm^{-3}. For the holes having same diamater and gap were simulated for different depths.

Table 3.4 Simulated solar cell performances of the surfaces patterned with 3 µm diameter, 1 µm gap between holes and 2, 4, 8 µm depth with Atlas

Diameter (µm)	Gap (µm)	Depth (µm)	Jsc (mA/cm^2)	Voc (mV)	FF	η (%)
3	1	2	24.17	630.76	83.1	12.67
3	1	4	22.42	630.5	83.11	11.75
3	1	8	19.68	630.19	83.12	10.31
Flat	-	-	26.87	521.22	79.26	11.3

When the diameter and the gap kept constant, the depth changed, the cell performances are shown in Table 3.4. Unlike experimental results (represented in Chapter 4, Table 4.2), it was obtained that, the shallower texture gave higher efficiency. The code was developed with ray tracing method, with finite difference time domain method results can be improved and get closer to results obtained with experiments. The solar cell performances that were tabulated in Table 3.4 are graphically represented in Figure 3.7.

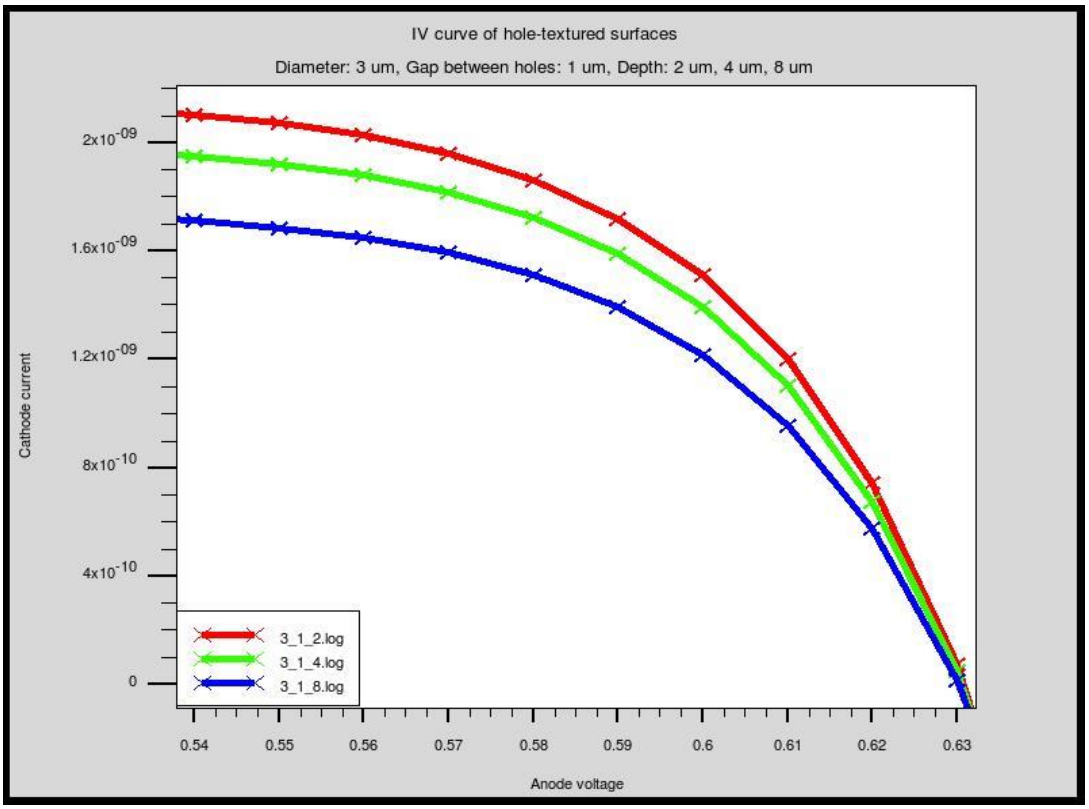


Figure 3.7 I-V curve of textured with 3 µm diameter, 1 µm gap, and 2, 4, 8 µm depth

The cell performances also depend on the thickness of the substrate. With our code we have observed that, the efficiency values increase with the increase of the thickness of the substrates, as a result of enhanced absorption. Figure 3.8 shows the efficiency values versus thickness graph. The substrate was textured with holes having 4 µm, diameter, 8 µm depth and 3, 4, 5 µm gap values.

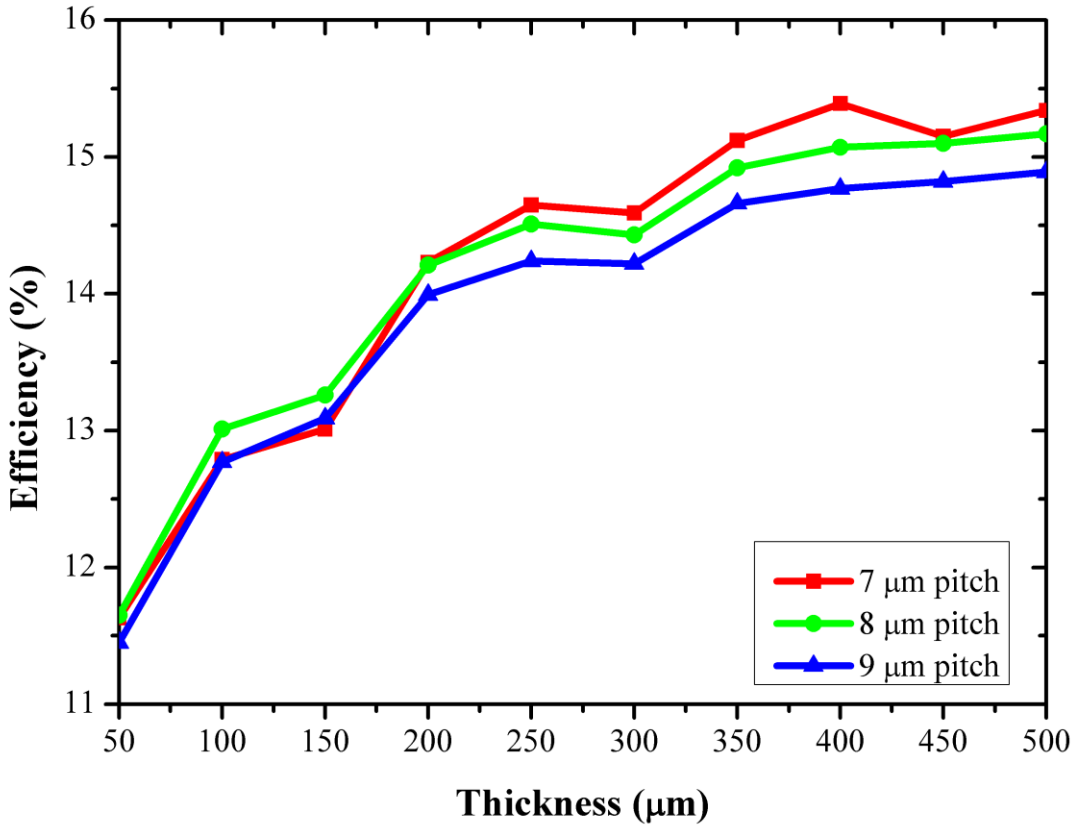


Figure 3.8 Efficiency comparison of surface textured with holes having diameter: 4 μm, pitch: 7, 8, 9 μm, depth: 8 μm

As expressed in experimental part, the effectiveness of the textured surfaces can be better seen when the analyses at different angles. The light matter interaction effect could be obtained with the simulations conducted at different angles. Solar cells charecterized with different angles were tabulated in Table 3.5. The cell was designed with the holes having diameter of 2 μm and 1 μm gap. The depth was taken as 4 μm. It can be seen that up to a certain degree, the short circuit current value was increased and after that angle started to drop, just as the same as we have obtained with the experimental results. It can be seen in Figure 3.9 that light matter interaction shows different profile with the change of incident angle.

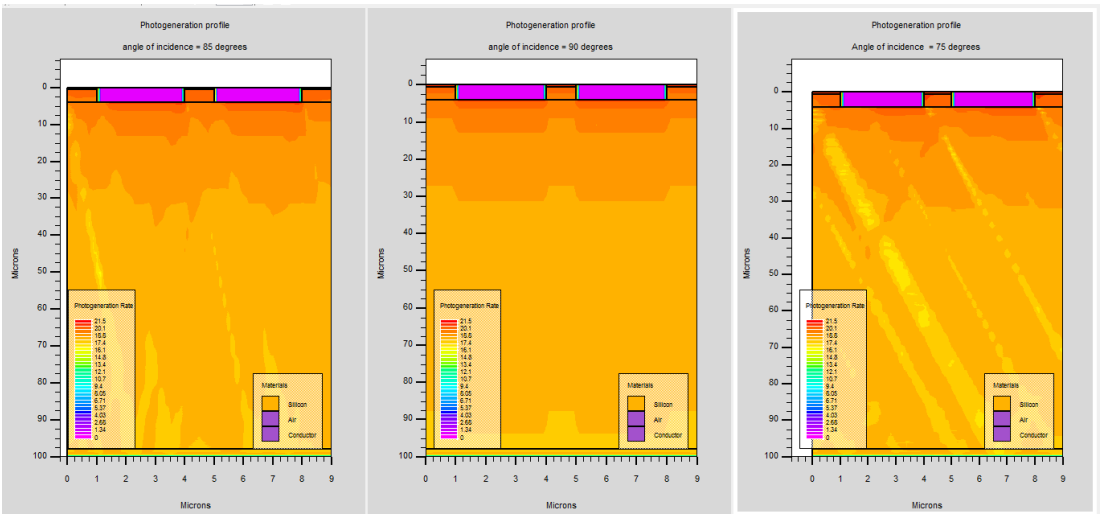


Figure 3.9 Angle resolved photogeneration rate of a hole-textured surface

Table 3.5 Angle resolved efficiency analyses of solar cells textured with holes having 2 µm diameter, 1 µm gap and 4 µm depth

Angle of Incidence	Jsc	Voc	FF	Efficiency
90	18.7	625.45	83.01	9.71
85	21.85	629.94	83.08	11.44
75	22.42	630.5	83.11	11.75
70	22.11	630.21	83.1	11.58
65	22	630.1	83.09	11.51
60	21.34	629.21	83.09	11.15
55	20.21	627.6	83.07	10.53
Flat	26.87	521.22	79.26	11.3

Upto 75 degrees there is a significant increase in short circuit current density, which directly affects the efficiency value, after 75 the values start to drop slightly. When the diameter and the depth of the hole are taken into consideration, the angle 75 corresponds to tilt angle of the sample geometrically. When the angle of the beam is set to 75 degrees, the sample can be thought to be tilted 15 degrees. The sample position is treated like a triangle.

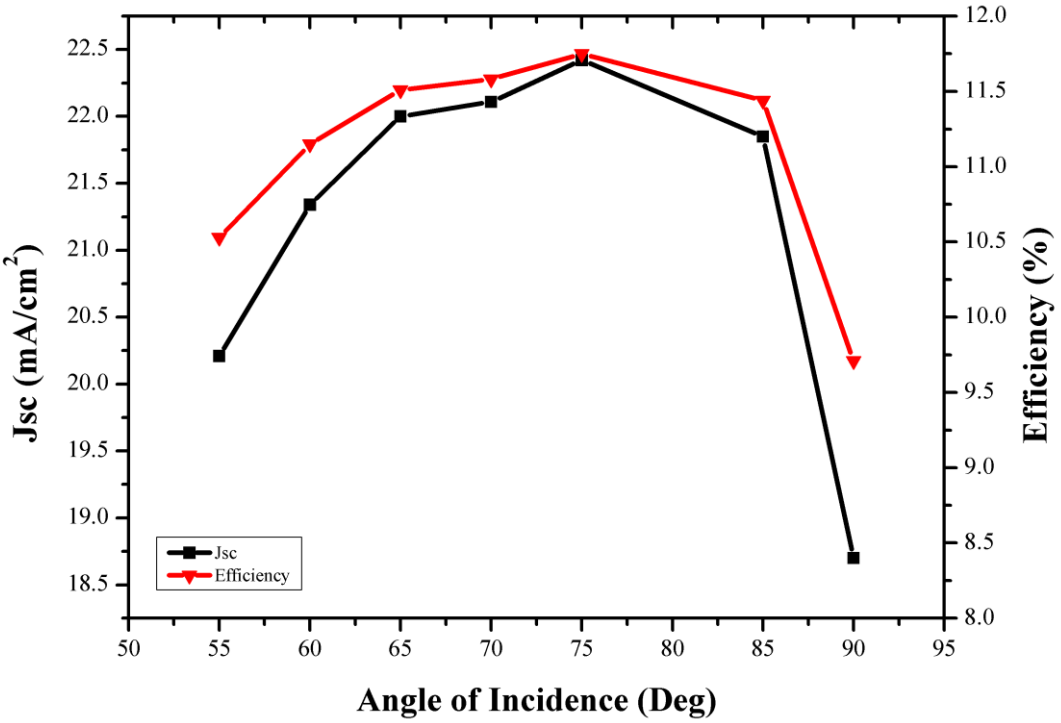


Figure 3.10 Angle of incidence effect on short circuit current density and efficiency

When textured surface (or the beam coming on to it) is tilted, the angle between sample and surface will define the hypotenuse of the triangle. The opposite side of the triangle is the depth, and the adjacent side is the diameter of the hole. The hypotenuse is sum of the square of depth and diameter of the hole. With this theory, it can be found that the tilt angle of the beam for the surface, textured with holes having 2 µm diameter and 4 µm depth, is 75 degrees. Figure 3.10 shows the effect of analyses with different angles. As shown in Table 3.5, cell efficiency is directly proportional with short circuit current density.

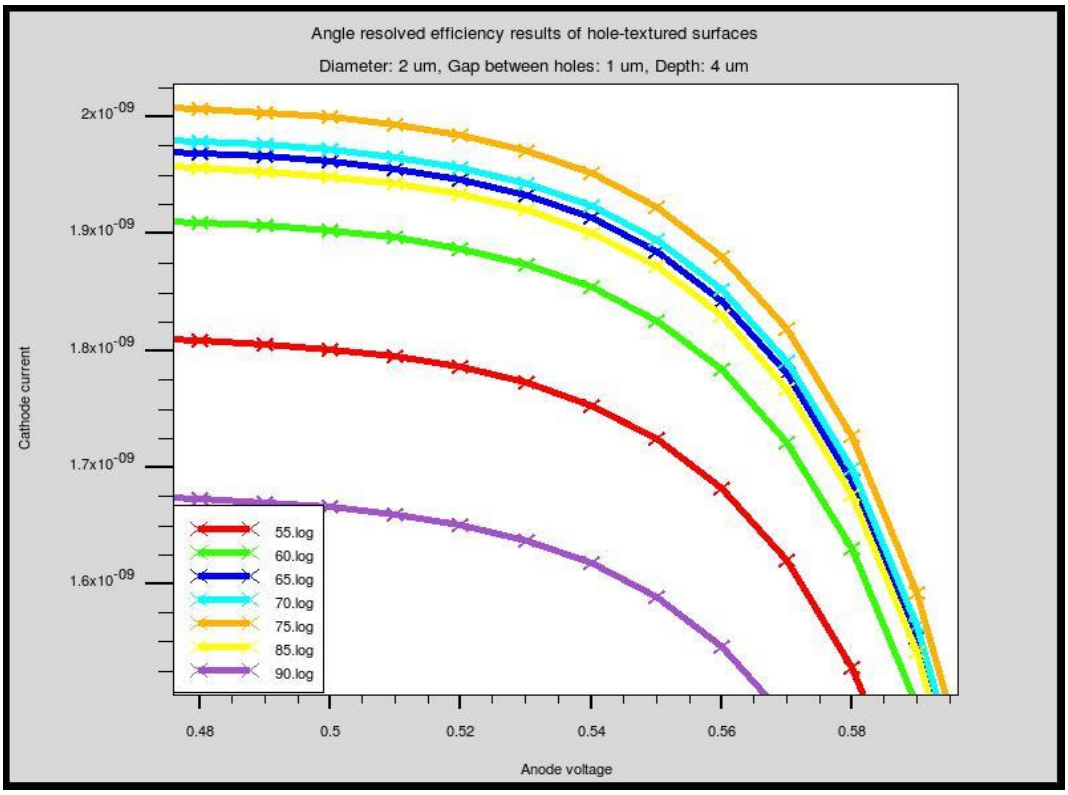


Figure 3.11 Angle resolved I-V curves of surface taxtured with holes having 2 µm diameter, 1 µm gap and 4 µm depth

Figure 3.11 shows the I-V curves of surface patterned with 2 µm diameter, 1 µm gap and 4 µm depth. The sample was simulated with different illumination angles.

The code that have been used can be improved with further optimizations, just like as experimental parameters. With Silvaco we have made the simulations of hole-textured surfaces.

In order to see the effect of light trapping, it is reasonable to make analyses with different angles, rather than beam source with straight angle. By changing the angle of the source it has been observed that each structure has its own unique behavior.

CHAPTER 4

PERFORMANCE OF SOLAR CELLS MADE ON MICRO&NANO HOLE PATTERNED Si WAFER

In previous chapters, we have discussed the application of micro and nano hole surface texturing to crystalline silicon wafer. In this chapter we present the fabrication of solar cells to procedures and main results corresponding to different surface structuring methods. For this, we have fabricated extensive amount of samples with different hole size and distribution.

4.1 Solar Cell Fabrication Experimental Procedures

Fabrication steps of a standard solar cell with aluminum back surface field (Al-BSF) is shown in Figure 4.1. Each of these steps are described briefly below.

1st Step: Fabrication sequence starts with the cleaning of p-type wafer to get rid of residuals of wafering process and to prepare the surface for the following step.

2nd Step: After cleaning step we have coated the surface with a positive photoresist (PR) to cover the whole wafer surface. Depending on the dimension of textures, each design has its own unique coating recipe.

3rd Step: Following the resist coating, photolithography is carried out to pattern PR so that opened regions will be etched during dry plasma etching or wet chemical etching whereas PR staying regions are protected.

4th Step: Depending on the pattern distribution and utilized dry plasma etching parameters, various hole dimensions for various hole depths are obtained resulting with different optical and electrical surface properties.

5th Step: After dry plasma etching, remaining PR from wafer surface is cleaned with oxygen plasma (not shown in flow chart) to continue with Phosphorous (P) diffusion.

6th Step: P diffusion is carried out at this step to obtain p-n junction.

7th Step: Following the P diffusion, SiNx is deposited by PECVD to provide surface passivation and reduce surface reflection as in the case of standard solar cell structure.

8th Step: Front and rear contacts of the cell is formed at this step where front Ag fingers are aligned to stay on un-etched regions during RIE, rear side is fully covered with Al.

9th Step: As the last step of the fabrication sequence, laser edge isolation is carried out to isolate front side of the cell from the rear side.

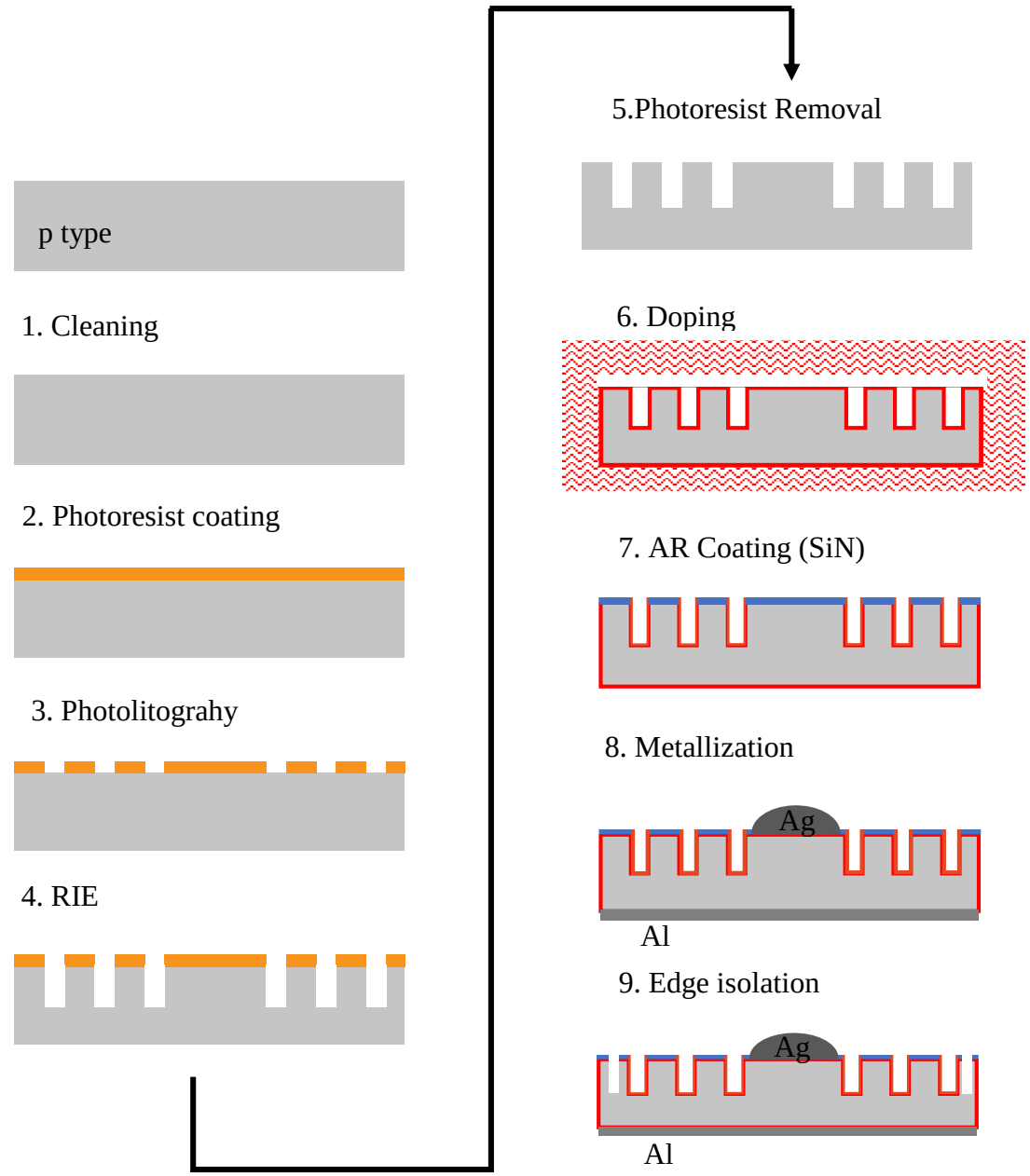


Figure 4.1 Process flow of solar cell production with micro and nano hole textured front surface

Our masks were designed in such a way that, front contacts don't intersect with the hole-textured parts of the surface. The schematic representation of a solar cell with hole patterns and front contacts is shown in Figure 4.2.

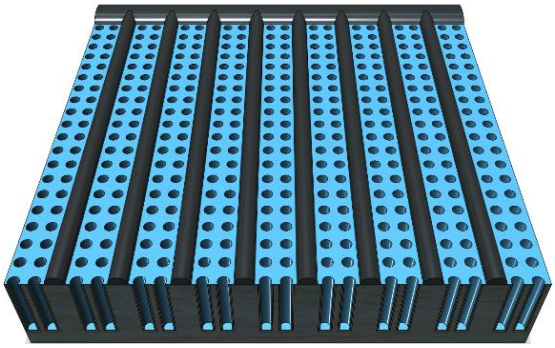


Figure 4.2 Schematic representation of hole textured solar cell with front surface contacts

After patterning step, we used one screen printing metal mask for front contacts even for different hole dimension and distribution. We kept the distance for front contacts constant which ended up with one screen printing mask.

4.2 Performances of Hole-Textured Solar Cells Obtained with Reactive Ion Etching

Solar cells fabricated with hole textured surfaces have higher efficiency values when compared with other type of textures [26]. The sizes of holes vary from micron to nano level. In literature, the solar cell fabricated with the surface patterned with 600 nm diameter and depth of holes had the efficiency value of 11.9 % [48]. When the substrate gets thinner around 10 μm, the efficiency can increase to 15.7 % with periodic nanostructures [108].

The solar cells that were fabricated with different hole diameter, pitch size and depth show different optical and electrical outcomes. Typical I-V curves of a hole textured solar cell is shown in Figure 4.3 a). Cell performance parameters are shown in the inset. It is seen that we have successfully fabricated and demonstrated solar cells on hole-textured thick wafer with expected enhancement in current [23]. We have achieved an efficiency value of 15.73 % which is the highest recorded efficiency in this type of the cell. Although it is lower than the standard cells with pyramid texturing, it is quite promising for the future applications. Standard solar cell with Al BSF have been optimized through the years and reached very mature level. With the same elaboration and optimization, similar or even higher efficiency values can be expected from the hole textured solar cells. As a first estimation, the difference from the standard

cell is somewhat expected due to the high reflection and increased surface recombination with respect to pyramid textured solar cells. Figure 4.3 b) shows the reflection spectra of the best performing cell compared with the pyramid textured and flat surface. We see that the reflection from the hole textured sample is much higher than the pyramid sample. Nevertheless, the high efficiency we have achieved from hole textured sample indicates the potential for much better performance. Surfaces patterned with periodic holes combined with random wires inside pre-patterned holes had lower reflection values than pyramid textured cells, however these optically preferable cells need some improvements in the electrical properties. Below we present the performance of the cells with hole textured surface from different point of view. Reflection value of the textured cell with the largest pitch size is close to the average reflection value of bare silicon, which is because of the dense structure of flat surfaces, rather than hole textures.

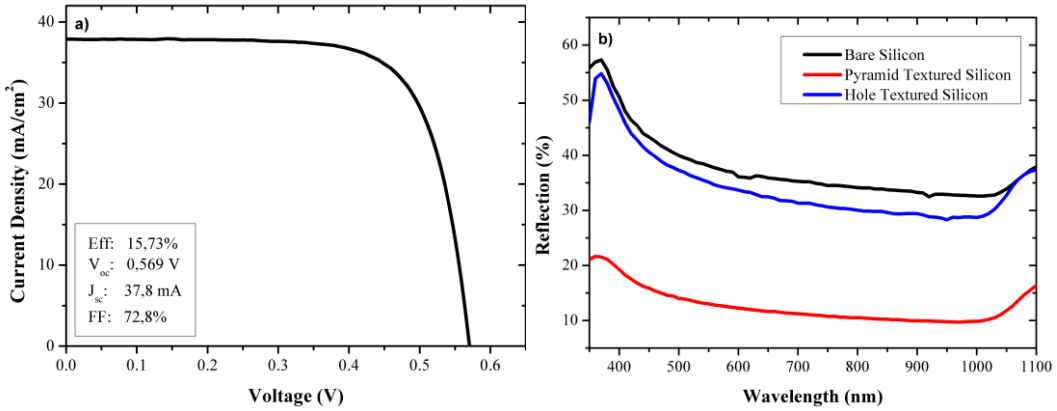


Figure 4.3 a) I-V curve of the best nano hole textured sample with hole diameter 4.1 µm, pitch size of 9.0 µm and hole depth of 12.4 µm. Inset shows the cell parameters from the I-V curve. b) Reflection spectra of the same sample compared with the bare Si and pyramid textured surface

4.2.1 Effect of Hole Diameter

Hole diameter and distribution defines the surface characteristics which determine the optical and electrical properties of corresponding solar cell. The patterning and etching techniques mentioned in Chapter 2 let us have a good control over the texturing type of the surface so that we have generated many samples with

different hole diameter and distributions. There are mainly four different diameters and four different pitch size resulting in 16 different configurations for patterning with lithography. Lithography with stepper property let us create different combinations of sizes. We designed 16 patterning masks, but depending on stepper's configuration, it is possible to change the dimensions of the pattern on mask of stepper, which is defined as reticle.

The dependence of solar cell parameters on hole diameter can be seen in Figure 4.4. The lines are drawn to show the tendency. It is hardly possible to draw very prices conclusions. However, one can figure out some general tendencies which are not absolutely deterministic. When we look at the variation of short circuit current we see that the it increases first with the increasing hole diameter, and then starts to decrease after about 3 μm hole diameter. This is a direct result of increased light trapping and absorption, which is main motivation for the surface texturing. The ability of more light trapping is improved with the hole diameter because more light can enter into the holes and trapped there. However, when the diameter of the holes exceeds certain value, the probability of bouncing back from the bottom of the hole increases. The surface becomes more reflective with increasing hole diameter, and in the extreme case, the surface approaches flat shiny surface. Hence, the short circuit current decreases with increasing hole diameter after certain value due to the increased reflection from the surface. On the other hand the open circuit voltage drops with the hole diameter as might be expected from the poor passivation of large surface area. As was discussed widely in the literature, we have the dilemma between optical and electrical properties: good collection of photons by an efficient light trapping, but high recombination losses due to the poor passivation at the surfaces. FF of a cell gives information about the series resistance and shunt resistance of the device. We see that FF drops with increasing hole diameter, which is a result of increased overall resistance of the device due to the large hole fraction at the surface.

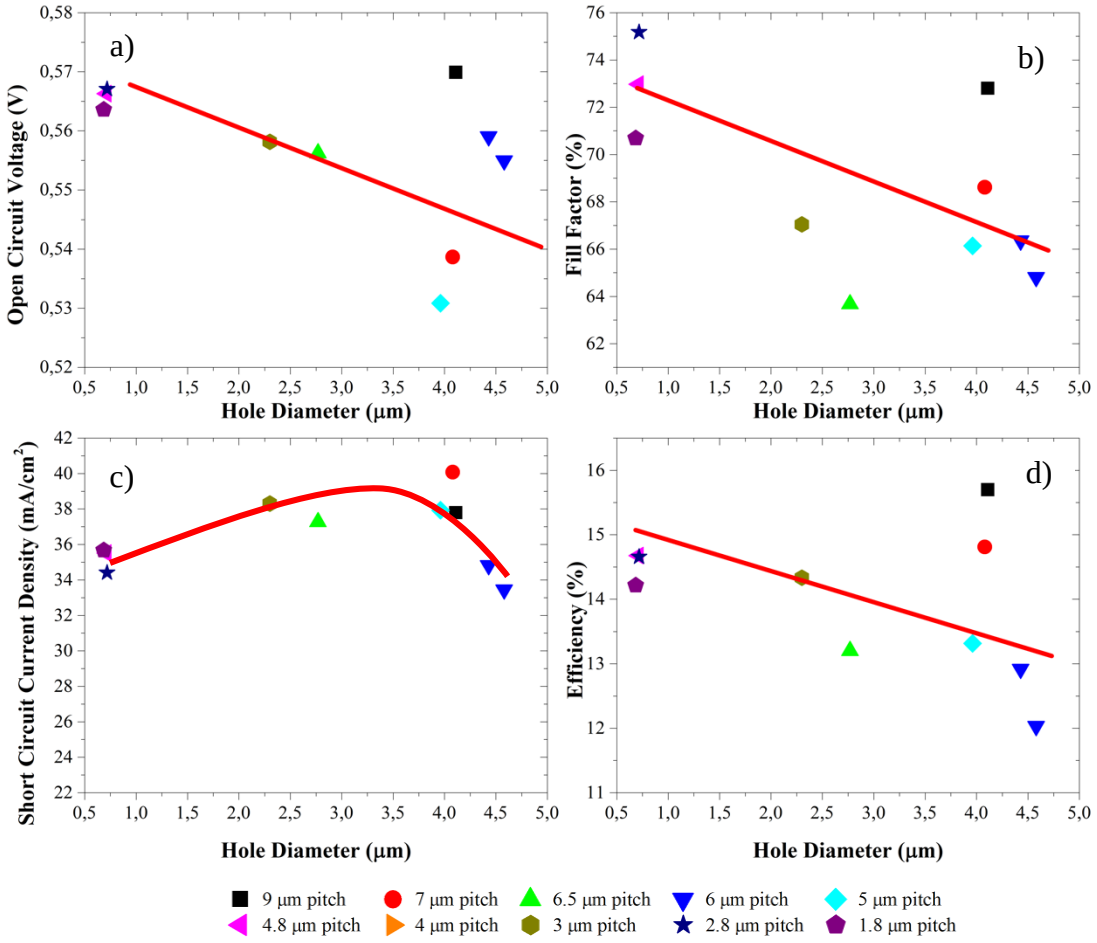


Figure 4.4 Solar cell parameters, a) open circuit voltage, b) fill factor, c) short circuit current density, d) efficiency depending on the hole diameter with different pitch values, solid lines are given to guide the eye

For hole textures having diameter less than 800 nm, which was the critical value for electron beam lithography based patterning, we made the pattern transfer with stepper which provides features below the diffraction limits of the optical lithography system. We were able to generate holes with diameter of 600 nm in this way. It is also interesting to note that these dimensions are at the border between ray optics and wave optics. For this reason, we present the results of the cells in this region separately.

Typical I-V curves of two different diameters in the wave optics regime are shown in Figure 4.5 below. Corresponding solar cell parameters are displayed in Table 4.1. To make a better comparison we kept the gap between holes constant, 1 µm. Holes having 600 nm and 700 nm were compared with each other. It can be seen that, 600

nm of diameter gave significantly better cell efficiency when compared with 700 nm, which leads to a 20% higher a short circuit current in the sample with 600 hole diameter than the sample with 700 nm. The open circuit voltage remained the same for these two samples, indicating that the junction formation and recombination losses are similar. The difference in the cell performance is remarkable and needs to be investigated. This is a problem of solving Maxwell equation for these two device configurations, which requires a special study with this purpose

Table 4.1 Comparison between 600- 700 nm diameter and 1 µm gap having the same RIE conditions and stepper patterning.

Structure Diameter-Gap	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	η (%)
600 nm- 1 µm	533.3	36.3	69.7	13.5
700 nm- 1 µm	534,1	30,7	72,6	11,9

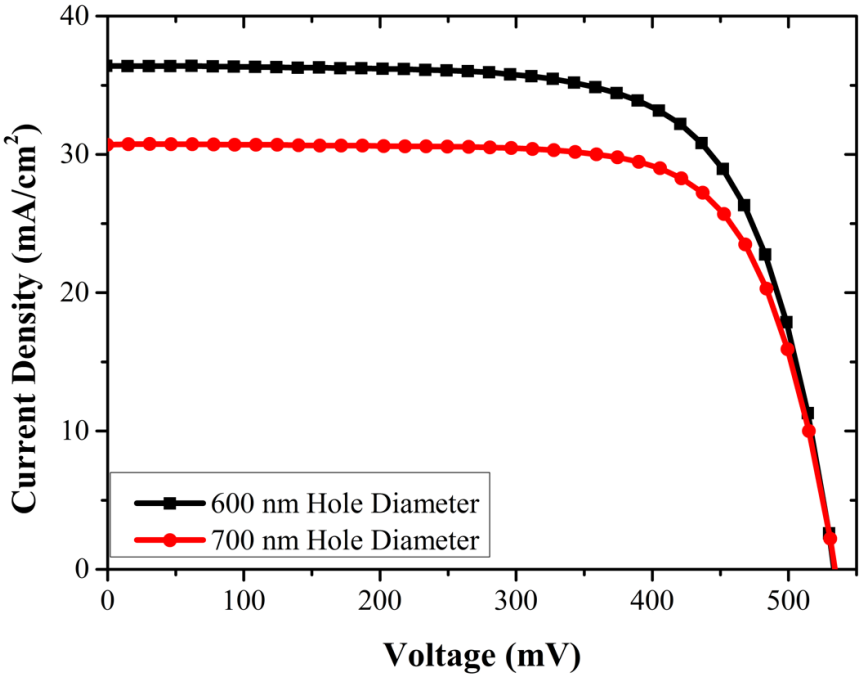


Figure 4.5 I-V curve of nano-hole textured surfaces with 600 nm and 700 nm diameter and 1 µm gap between holes

4.2.2 Effect of Pitch Size

The pitch size, which is the periodicity of the pattern, increases with the increase of either diameter, or the gap between holes. As the diameter of the holes increases, the photocurrent generation for a single unit will be enhanced.

Increase in the pitch size indicates an enhanced contribution of the radial junction solar cells patterned with holes [27]. For the solar cells that were fabricated with different pitch sizes are represented in Figure 4.6 in terms of open circuit voltage (Voc), fill factor (FF), short circuit current density (Jsc) and efficiency (η).

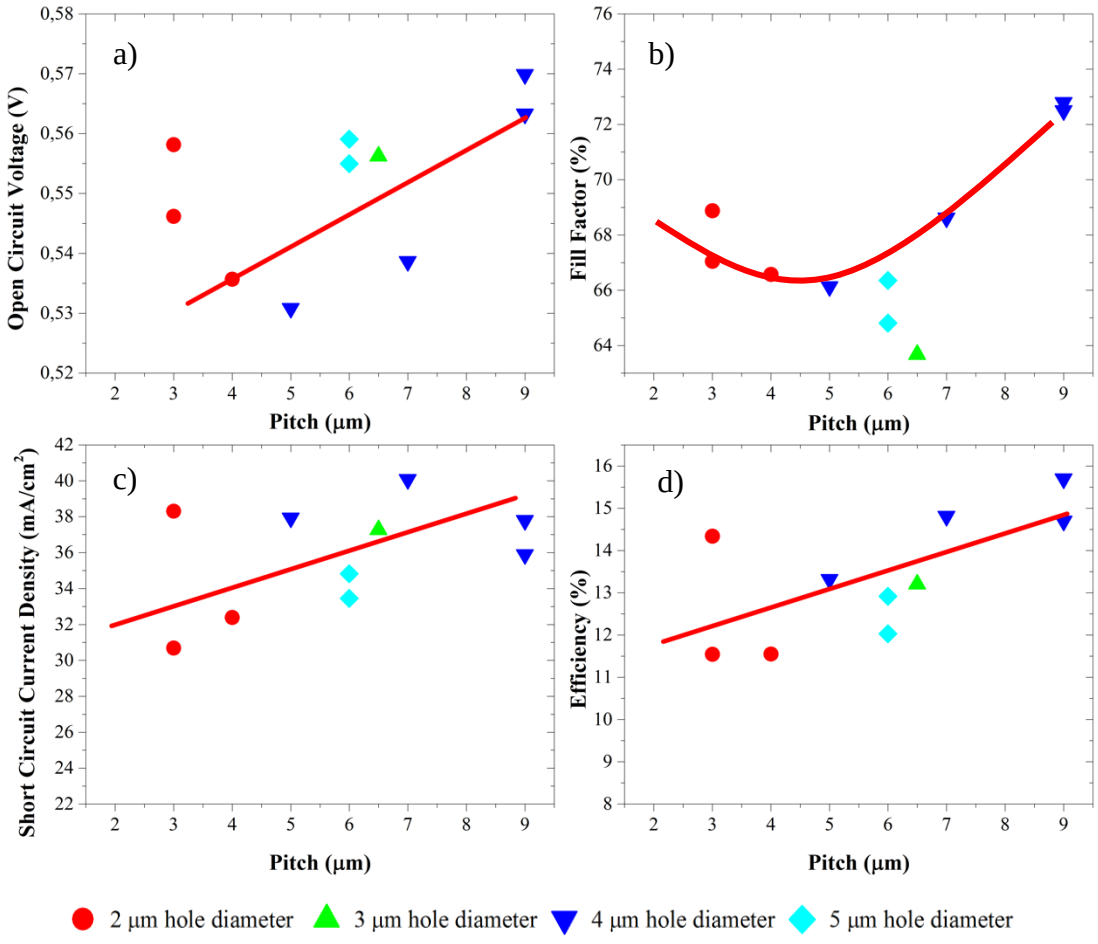


Figure 4.6 Solar cell parameters, a) open circuit voltage, b) fill factor, c) short circuit current density, d) efficiency depending on pitch size with different hole diameters, solid lines are given to guide the eye

For 2 µm diameter increasing pitch degraded both Voc and Jsc of the solar cells. Reduction in Voc could be related to increased surface roughness. It is apparent

that applied passivation recipes for whole fabrication sequence is not suitable to fully cover such small features on the surface of the wafer. The results represented here were obtained from the wafer patterned with different pitch sizes. In order to obtain better doping, passivation and metallization results, and specific fabrication parameters should be defined and used. Unlike 2 µm diameter holes, considering 4 µm diameter holes, increasing pitch size improves cell performance.

4.2.3 Effect of Hole Fraction and Total Surface Area

As given in Chapter 2, hole fraction (HF) is defined as the ratio of the hole volume to the total material volume including the holes, which is calculated with the Equation 4.1.

$$HF = \frac{Volume\ of\ holes}{Total\ volume} = \frac{np\pi^2 h}{L^2 h} = \frac{n\pi r^2}{L^2} \tag{4.1}$$

For the calculation of total hole volume represented in Equation 4.1, number of holes (n) on the given topography was multiplied with the volume of one hole. The height (h)value was taken the same for holes, and for total surface patterned with holes, for that reason h could be eliminated. Figure 4.7 shows the parameters of radius (r), pitch size (p) and length of one side (L) for hole textured surface.

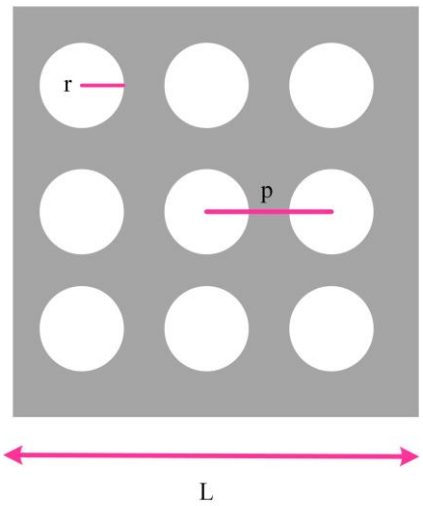


Figure 4.7 Schematic representation of radius (r), pitch (p) and length of one side (L)

When we relate the area of holes to the surface area, we can define the relative surface area (RSA), which is the ratio of the total surface area to the area of the flat and non textured surface, as expressed in Equation 4.2.

$$RSA = \frac{L^2 + 2n\pi rh}{L^2} \tag{4.2}$$

Variation of the cell parameters with the hole fraction is shown in Figure 4.8 below. The light trapping action of the holes are clearly seen from the variation of short circuit current with hole fraction shown in Figure 4.8. The amount of short circuit current increases initially for small hole fraction and reaches a maximum value of about 38 mA/cm^2 which is remarkably high. It then starts to drop with increasing hole fraction. This is expected from the increased recombination with a large surface area of the holes. As discussed above, there are two competing mechanisms here: one is the efficient light trapping and the absorption, the other one is the recombination losses at the surface of the hole area. It seems that for low hole fraction values, the light trapping dominates the general behavior of the variation, while for large hole fractions recombination losses determines the changes in the short circuit current. As for the efficiency, we have obtained quite promising values. The best efficiency we have obtained is 15.73% which is highest value recorded in the literature so far for thick crystalline solar cells fabricated on p-type crystalline silicon wafers with standard solar cell fabrication techniques. On the other hand, high performing cells are those with low hole fraction values. We observe a degradation with increasing HF and surface area especially for large values. When we have investigated the same data as a function of total surface area, it was obtained that the degradation effect was stronger. This is indeed expected due to the fact that large surface area generated after the etching process causing high surface recombination losses and thus reduced efficiency. However, the drop in the efficiency is not that drastic. We observe high values even for high HF and surface areas. This is showing the success of the approach and the way we have produced the cell. It is clear that one can reach much higher values with a good surface passivation which needs to be studied and optimized carefully, which is not the core of this thesis. Optimization of the antireflection coating is another parameter that can improve the measured cell efficiency even further. In Figure 4.8,

solar cell parameters obtained with different distribution of holes, hence different hole fractions. Open circuit voltage and fill factor drop with the increase in hole fraction. For short circuit current density and efficiency that drop was obtained after 0.3 value of hole fraction.

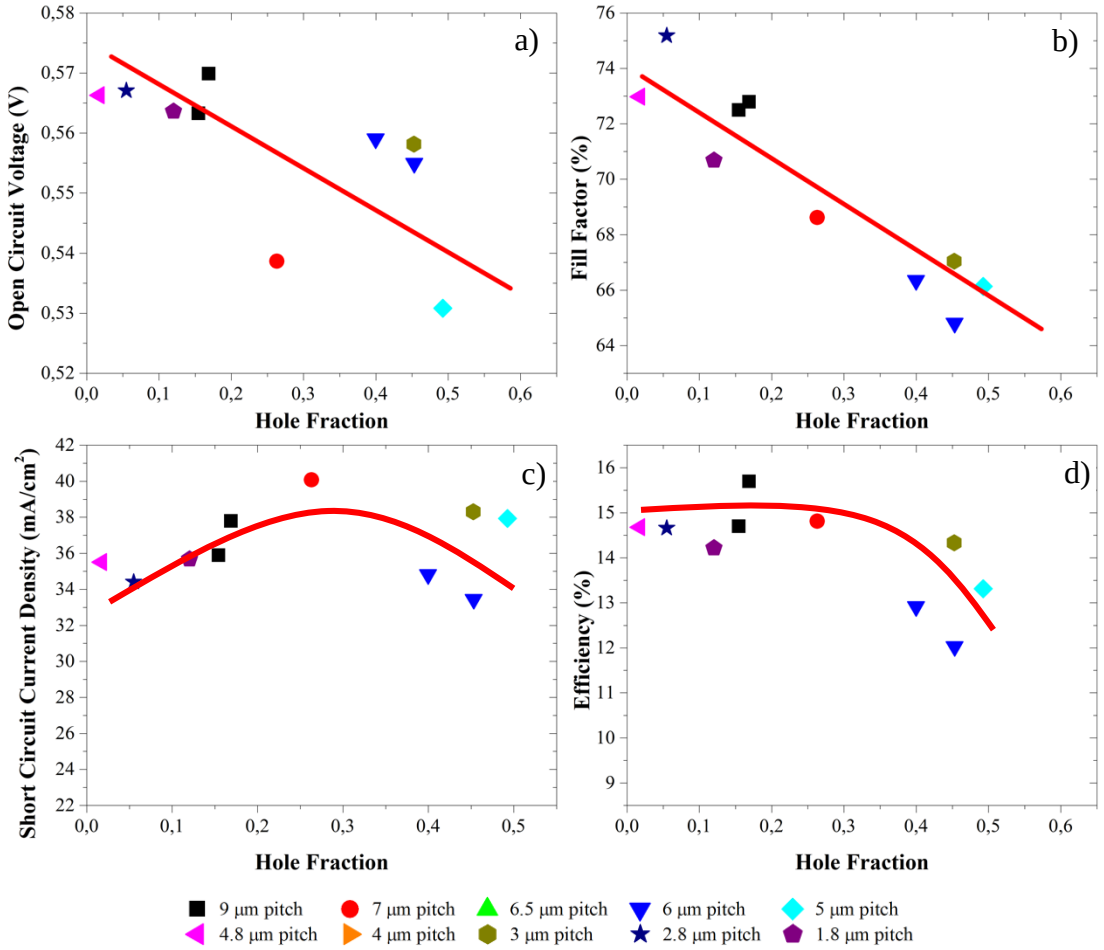


Figure 4.8 Solar cell parameters, a) open circuit voltage, b) fill factor, c) short circuit current density, d) efficiency depending on relative surface area, solid lines are given to guide the eye

4.2.4 Effect of Hole Depth

Fabricated solar cells having holes with different diameter, period and depth values have much lower reflection values when compared to bare silicon as explained in detail in Chapter 2. Regardless of pattern transfer method and etching type. The surface can be patterned with electron beam, nanoimprint, nano sphere, hole colloidal lithography. After patterning, surface is textured by wet or dry etching sequences. All

techniques described in Chapter 2 have been used to create periodic textures, later randomness could be introduced to system if desired. Optical characterization of surfaces with different hole diameter, distribution and depth were analyzed in detail, and it was obtained that lower reflection values are attainable.

The average reflection value differ for different topographies. For the same diameter and pitch sizes, etching with different durations were conducted, hence resulting in different depths. The highest efficiency solar cell performance device was obtained with the mask having hole diameter of 4 µm and 5 µm gap. When etching duration was increased, deeper structures were obtained. Deeper structures resulted with lower reflections, which provides more efficient light trapping effect. Average reflection data for three different hole depths with 4 µm diameter and different pitch values is shown in Figure 4.9.

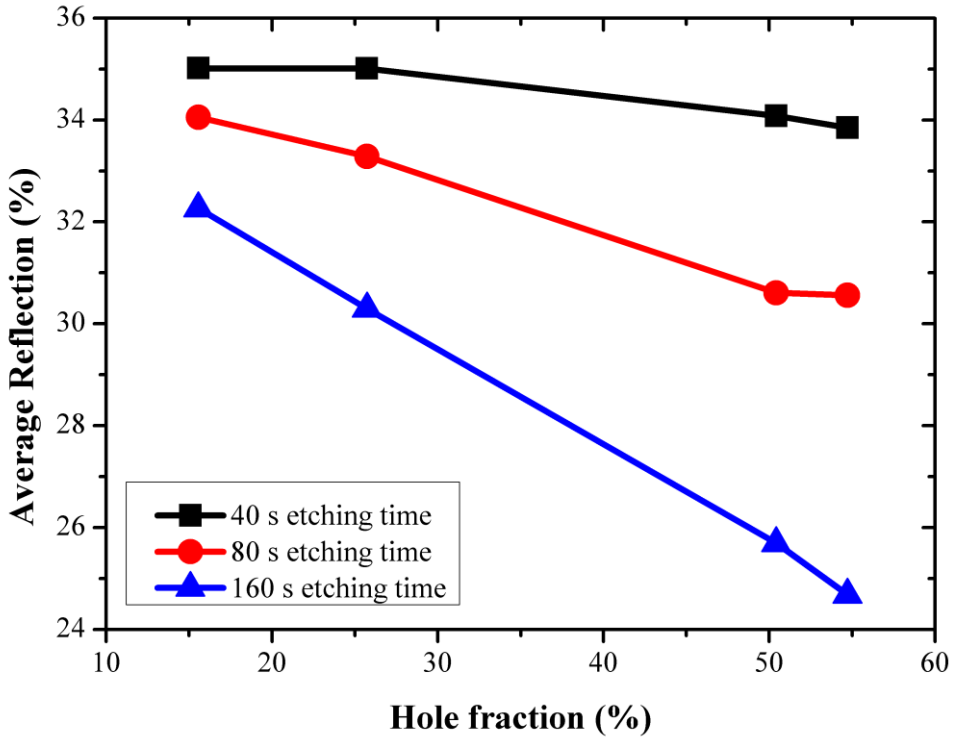


Figure 4.9 Average reflection comparison of hole textured surfaces with 4 µm diameter and four different pitch values subjected to dry plasma etching

The depth of the holes can be easily controlled with the etching time. For the dry plasma etching system which was used for RIE process, vertically etched deep

trenches can be formed by a special method which has been developed for MEMS applications. However, for standard RIE systems and chemical etching techniques like metal assisted etching, there exist limitations on the vertical wall formations

J-V curves of three different samples with three different hole depths are shown in Figure 4.10. It can be seen that highest efficiency was obtained from the structure subjected to longest etching duration, hence the deepest trench having 12.4 µm depth. The most significant increase is observed in the short circuit current, which is a result of good light trapping.

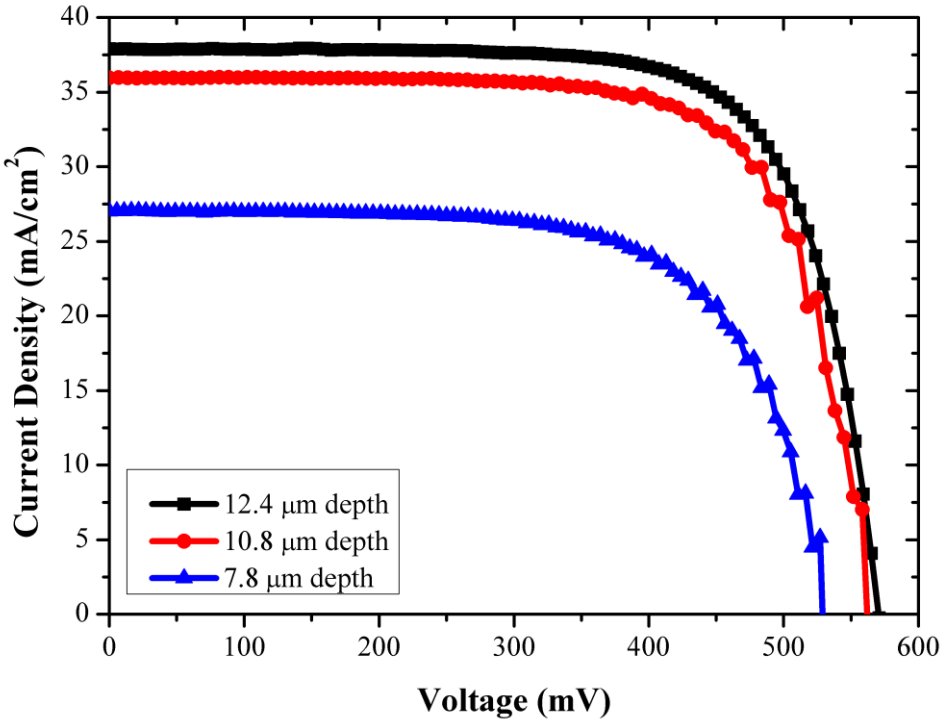


Figure 4.10 IV characteristics of solar cells patterned with 4 µm diameter and 5 µm gap subjected to three different dry plasma etching duration

The solar cell performances as a function of hole depth, extracted from the J-V measurements are summarized in Table 4.2. In this study, dry plasma etching conditions were kept the same, except for the etching duration. In Table 4.2, surface patterns obtained with wet chemical etching was also added for comparison.

It can be seen that the efficiency value can be as high as 15.7%, which was achieved with micro-hole textured surface [109]. This result was achieved with 525 µm thick wafer. The improvement in the efficiency is clearly a result of increase in the

short circuit current due to the efficient light trapping. The short circuit current and the efficiency increase with increasing the hole depth. We also see that the Voc values are relatively high compared to the expectations from such systems. It is quite remarkable that Voc remains the same with increasing hole depth, which contradicts with the expectation of higher recombination when the surface area is increased. This indicates that the surface passivation is remarkably well and other losses are more effective than the surface passivation in this case.

Table 4.2 Performance of periodic hole-patterned solar cells using reactive ion etching

Etching Technique	Dia (μm)	Gap (μm)	Depth (μm)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	η (%)
RIE	4	5	7.8	527.7	27.0	67.5	9.6
RIE	4	5	10.8	563.3	35.9	72.5	14.7
RIE	4	5	12.4	569.9	37.8	72.8	15.7
RIE	0.6	4	8	529.1	33.7	53.7	9.6
MAE	3	0.8	3	504.6	24.2	69.9	8.5

The MAE sample tabulated in was coated with 25 nm silver and etched for one hour. We see that this sample is not performing well compared to the ones prepared with RIS. Significantly low Jsc value is a result of poor carrier collection due to the randomly distributed nano wires inside of periodic holes.

4.3 Solar Cell Textured with Metal Assisted Etching

Solar cells, which were subjected to wet chemical etching, were also analyzed. Samples were subjected to MAE for one hour. Each surface textured with same diameter and different gap values was subjected to same wet chemical etching conditions. Some representative J-V curves obtained from the samples with varying gap distance between holes are shown in Figure 4.11. These samples have the same hole diameter and pitch size. The smaller gap distance corresponds to larger surface area, and higher HF. It is clearly seen from this plot that cell performance is improved

with larger gap distance. This is a result of increase both in the open circuit voltage and short circuit current which are tabulated in Table 4.3.

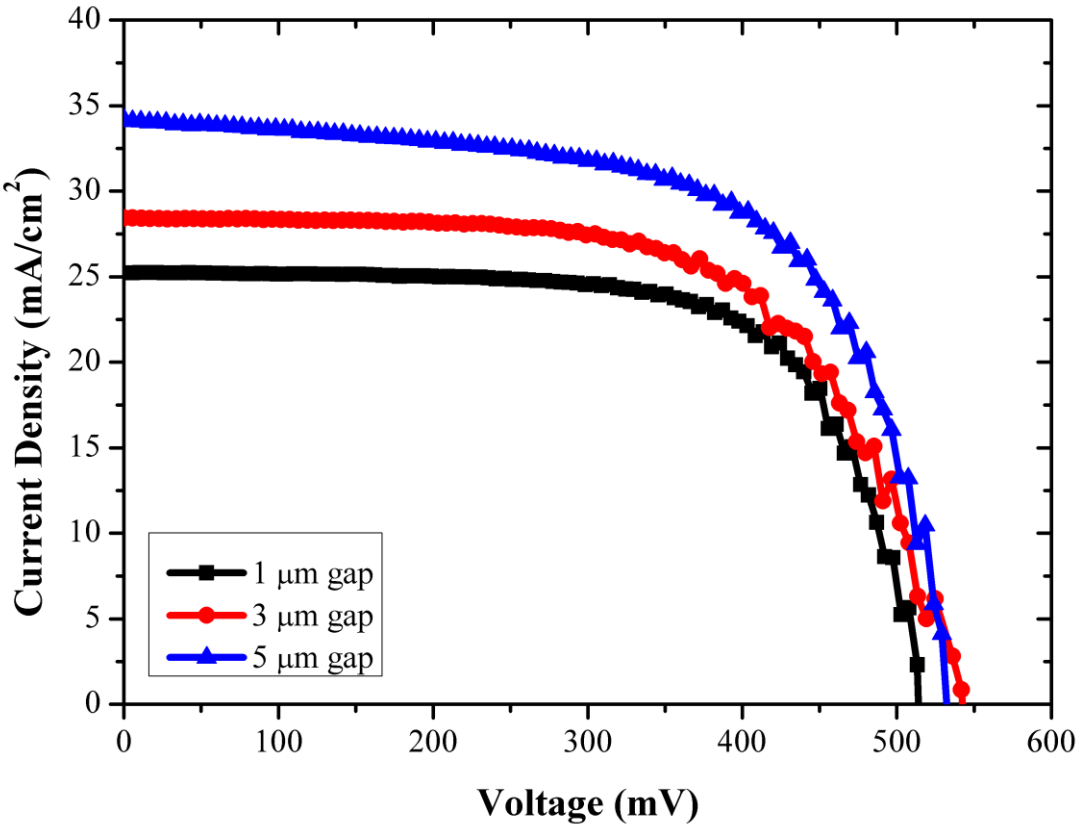


Figure 4.11 Current density versus voltage graphs of samples with 5 µm diameter and 1, 3, 5 µm gap subjected to one hour MAE

Table 4.3 MAE applied to the surface with 5 µm and 1, 3, 5 µm gaps having the same etching parameters

Diameter: 5 µm	Depth (µm)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	η (%)
1 µm gap	17.48	512.1	25.2	69	8.9
3 µm gap	19.32	531.6	28.4	64.1	9.6
5 µm gap	23.04	531.8	34.1	63.7	11.5

Solar cell performance values obtained with MAE were not as high as RIE patterned surfaces. This is mainly due to unexpected nanowire formation inside micro

hole textures. These nanowires reduces both Voc and Isc values due to the extremely large surface area which is quite defected. The resultant structures can be seen from the SEM pictures shown in Figure 4.12. The nanowires inside the holes ended up with promising results from optical view, but final structure is not good for electrical performance of the cell. It seems to be hard to passivate such complicated surfaces.

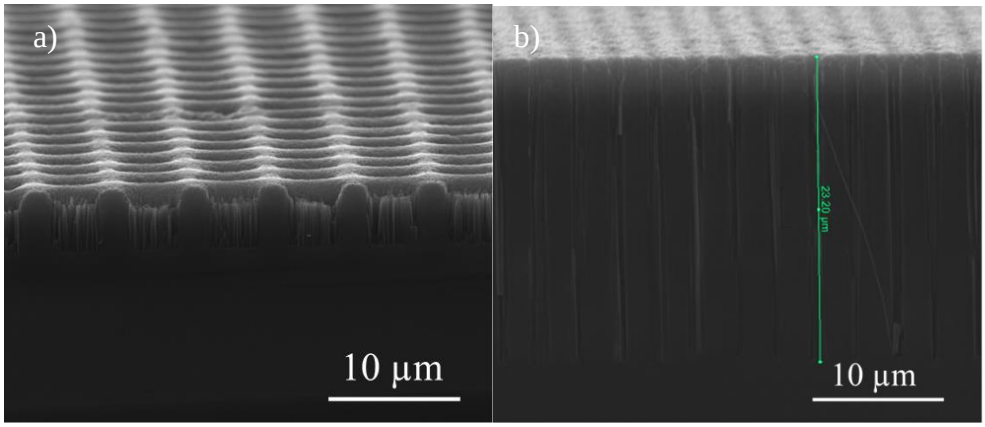


Figure 4.12 SEM images of samples textured with MAE. a) 9 min etching, b) 60 min etching

4.4 Passivation of Hole Textured Surfaces

It is generally accepted that the surface passivation is the crucial step when the surface is textured with micro and nano structures. Large surface area is expected to cause higher recombination losses, which acts against the optical gains that might be obtained due to the effective light trapping. The effect of surface recombination losses is mostly seen as a drop in the open circuit voltage, which can also affect the short circuit current. This study deals with surface structuring with several patterning and etching techniques. In all cases, the surface area which is exposed to chemical and physical processed is increased. The surface is inevitably damaged during these processes. If a proper passivation technique can not be developed, such a large area surface will deteriorate the electrical performance of the cell with high recombination losses. This is generally observed throughout this study.

The passivation effect on solar cell performances was studied with standard technique used in the c-Si solar cell production. We have performed SiNx deposition

using PECVD system of GÜNAM, which is routinely used in the cell fabrication. In order to see the optical effect of the SiNx layer, reflection measurements of textured surface were compared with SiNx deposited textured surfaces. Reflection spectra from these samples are shown in Figure 4.13. Average reflection as a function of gap between the holes are shown in Figure 4.14. We see that the reflection increases with the increasing gap distance and decreases drastically as a result of anti-reflection effect of SiNx.

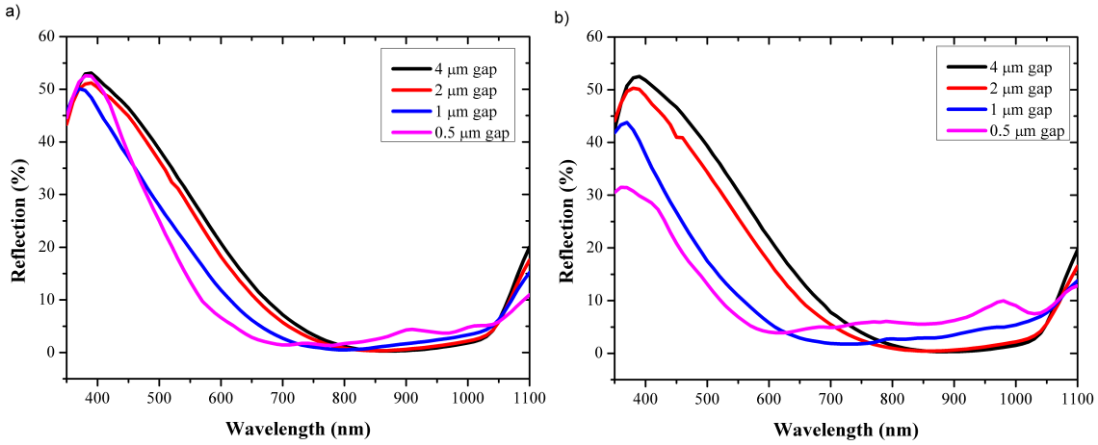


Figure 4.13 Reflection spectra of samples coated with SiNx with the diameters of a) 600 and b) 700 nm. The gap between holes is 500 nm, 1 µm, 2 µm, 4 µm

Figure 4.14 shows the average reflection values for 600 nm and 700 nm diameter of holes before and after SiNx coating. As seen in Figure 4.14, application of SiNx layer reduces average reflection of both samples having diameter of 600 nm and 700 nm samples where smaller the gap ends with lower the reflection.

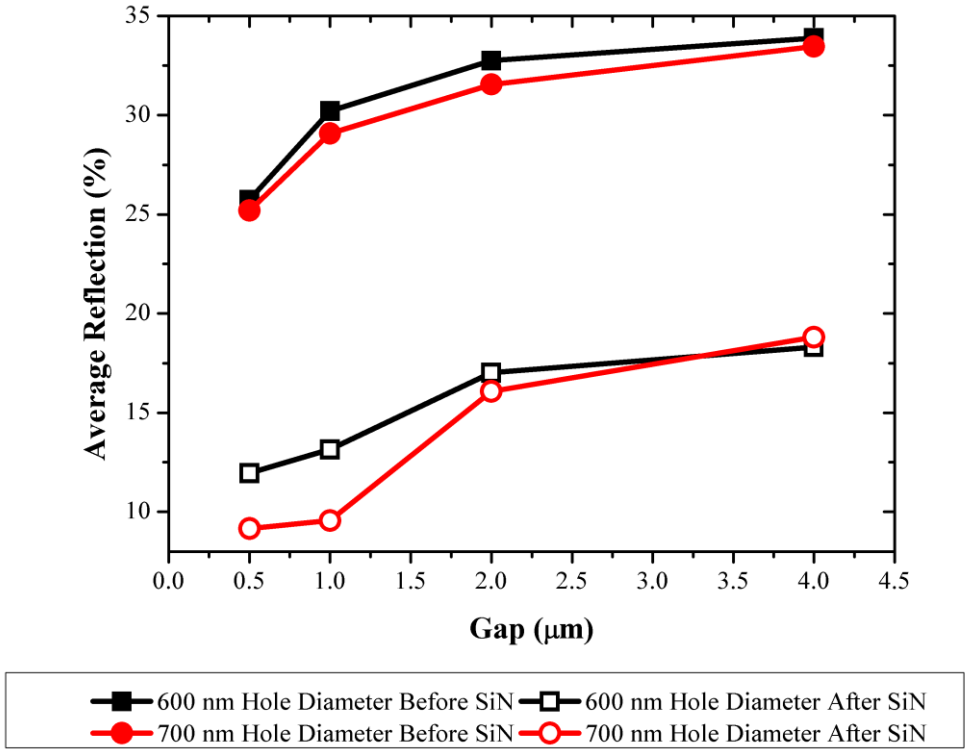


Figure 4.14 Average reflection spectra of samples having 600 nm and 700 nm diameter before and after SiNx coating

For all passivation studies, standard nitride coating recipe was applied to hole textured surfaces. In order to obtain better optical performance, hence electrical performance, patterned surfaces can be subjected to special passivation process optimizations.

CHAPTER 5

ANGULAR DEPENDENCE OF CELL PERFORMANCE

There have been used standard solar cell characterization parameters, i.e. AM 1.5 illumination, 25 °C medium temperature, the angle of the simulated sunlight beam's hitting directly on top of the surface without any tilt angle relative to the surface, but these conditions do not meet rational status, they only represent a small portion of realistic, actual conditions in which a solar cells and panels work. Characterization techniques should be considered depending on the medium of the cell, the intensity and incidence angle of the sunlight, physical location of the cell according to the duration of a day and climate. Standard photovoltaic modules are ground fixed, and the sun's position is changing in time depending on earth's movement, so angle resolved performance analysis is the only way to obtain correct values of the cell performance. All solar cell results obtained with standard cell characterization techniques represent the performance only for that specific conditional case.

In order to make better analyses, close to realistic cases as much as possible, standard characterization techniques should be enhanced. The best and easily applicable solution for research and industry is varying the angle between sample and the incident beam. Photovoltaic properties of a cell vary depending on the effect of light matter interaction. To see the effect of light trapping, the characterization techniques should be favorable. Better cell results have been obtained with different light trapping schmes, even better ones can be obtained with improved characterization techniques.

5.1 Importance of Incidence Angle for Patterned Surfaces

The characterization of a solar cell, either optically or electrically, strongly depends on its material quality and surface morphology. These chemical and physical

parameters will define the performance of a cell. The aim of surface texturing with a variety of surface patterns is to achieve optically and electronically desired solar panels.

As the core of this thesis is surface texturing with micro and nano holes using different patterning and etching techniques, we have analyzed our solar cells with non-zero illumination. We have obtained the effect of hole texturing with respect to standard cell characterization conditions. Depending upon the diameter, distribution and the depth of the holes, surface exhibits different optical and electrical properties. In order to see the effect of hole textured c-Si surface on cell performance, it is more necessary to analyze the surface at variable angles. The relative incident angle has been varied between 0° to 45° in orthogonal axes. The results show a % 3 improvement in average electrical power output normalized with respect to normal incidence power output of textured surfaces. The hole patterning was achieved with electron beam lithography and subjected to dry plasma etching. Afterwards standard solar cell fabrication steps, explained in Chapter 2, were applied. The optical and electrical characterizations of the surfaces patterned with different hole diameter and distribution were done with standard test conditions. In order to see the effect of patterning on light matter interaction we developed an effective way of characterization.

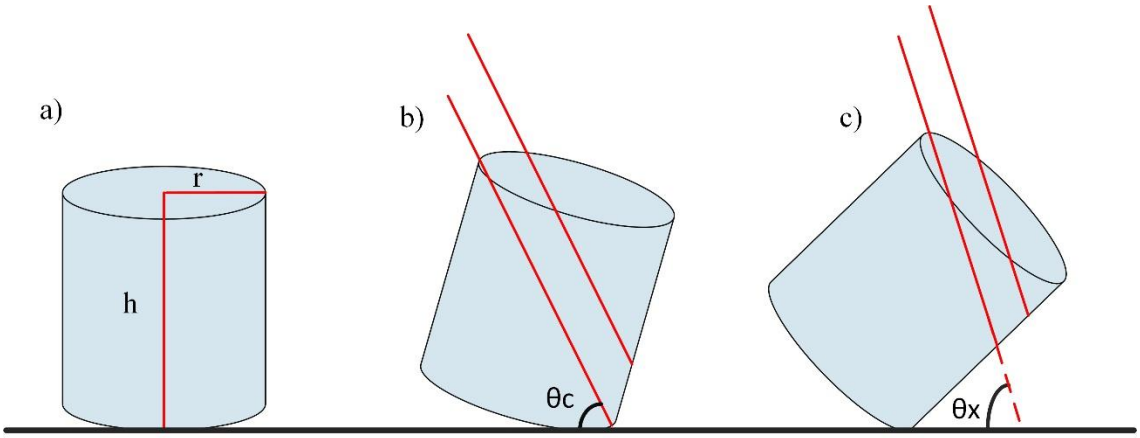


Figure 5.1 Schematic representation of a cylinder under a) direct sun light, no tilt angle, b) (θ_c) critical angle, c) $(\theta_x > \theta_c)$ bigger than the critical angle

We take into consideration that if any light enters the hole textured surface with an angle rather than 0° as shown in Figure 5.1 a) then this light bounces back and forth between the walls of the hole.

The diameter of the holes, spacing between two holes will affect the penetration depth of light. The penetration depth of the maximum wavelength of the solar spectrum is equal to the minimum spacing between two etched holes [110]. The diameter and the depth of the hole texture define the distance traveled by a light ray at each point of incidence on the wall, but after a critical angle(θ_c) schematically represented in Figure 5.1 b), the texture starts shadowing itself, Figure 5.1 c), hence there would be no generation on shadowed side walls. The angles larger than ($\theta_x > \theta_c$) will end up with lower electrical performances when compared with smaller angles [111].

5.2 Experimental Setup for Angular Dependence Measurements

Angle-resolved characterization of a solar cell can be done in two ways: first, changing the angle of the illumination source (which is not available for most of the characterization set ups), second, the sample could be tilted with respect to the incident light beam. Based on measured short circuit current density and efficiency values at different angles, it is possible to determine the combination of hole diameter and depth that will end up with the best cell performance. For hole textured surfaces, each measurement was conducted as function of the relative incident angle between the solar cell and the light source. As represented in Figure 5.2, during our cell characterization we managed to change the incident angles with tilting the sample rather than changing the angle of simulated sunlight beam.

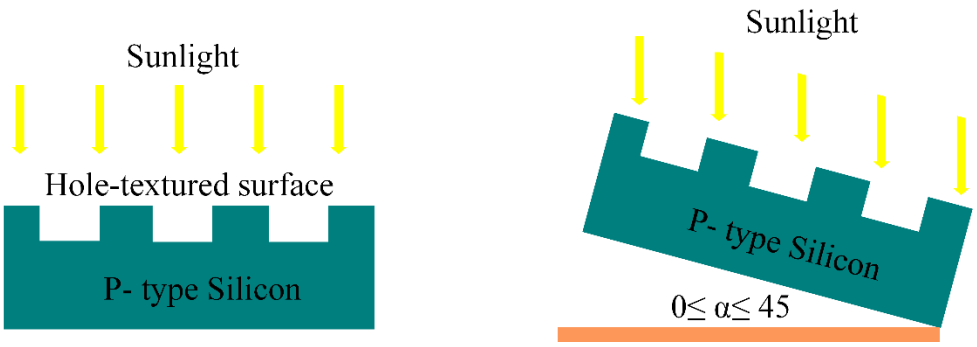


Figure 5.2 Schematic representation of angle-resolved measuring setup

In order to achieve characterization of our hole textured surfaces we have designed a special back contact. Our setup has a fixed back contact, for this reason we weren't able to change the angle of sample with moving bottom contact, with the help of our design we could manage to make analyses.

5.3 Results of Experimental Measurements of Angular Dependence

Solar cells that we fabricated on silicon surface having different distribution of holes were analyzed with angles varying in between 0° to 45°. Our results demonstrate that each depth corresponds to a certain angle at which maximum efficiency can be obtained. Angle-resolved efficiency analysis is one of the best techniques to see the effect of light trapping. Hole-texturing, due to the concave and periodic structure of hole shape, the effect of characterizing with different angles let us see the effect of light trapping. Hole texturing surfaces showed higher increase in Jsc and efficiency values compared to randomly etched surfaces, conical-like hillocks that were randomly distributed across the entire solar cell surface characterized with different angles as shown in Figure 5.3 [111].

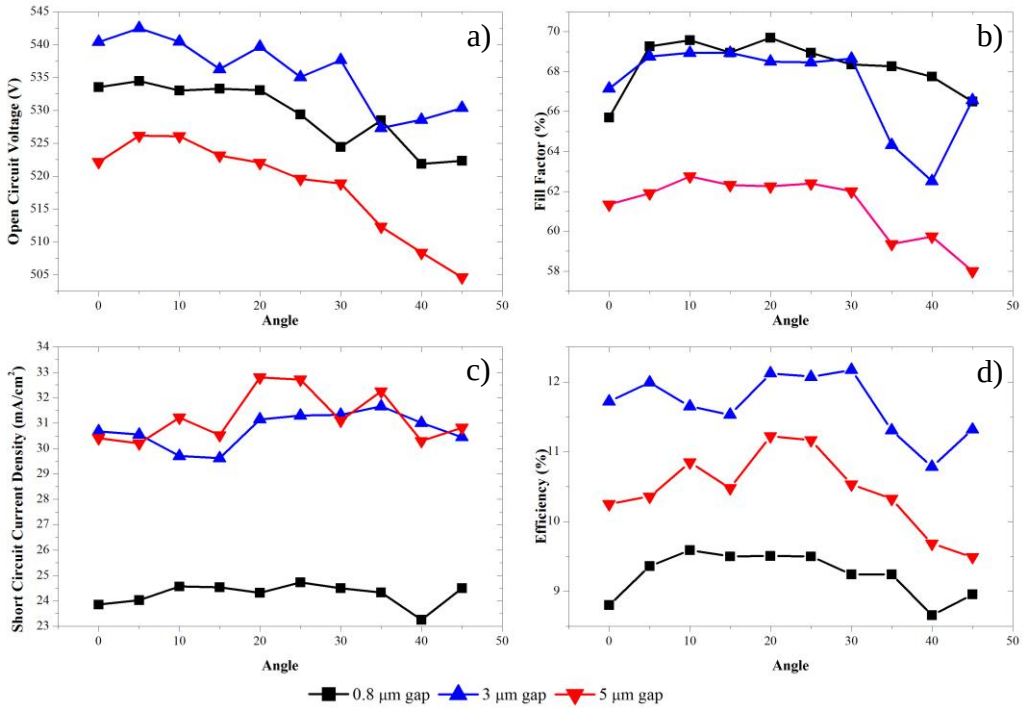


Figure 5.3 Solar cell performances: a) open circuit voltage, b) fill factor, c) short circuit current density, d) efficiency, obtained from the surface with 4 µm diameter 0.8, 1, 3, 5 µm gap, 7.8 µm depth, fabricated with dry plasma etching, between 0° to 45°

Figure 5.3 shows the solar cell performance comparison of samples having diameter of 4 µm and gap of 0.8, 1, 3, 5 µm. The measurement were done between 0° to 45°. For the samples having 1 µm and 3 µm gap, the increase in short circuit current continued 20° and 15°. The depth of the sample for 5 µm gap had the depth of 7.8 µm checked with cross sectional images obtained with scanning electron microscope images. From the depth and the diameter, the angle was calculated as 25°.

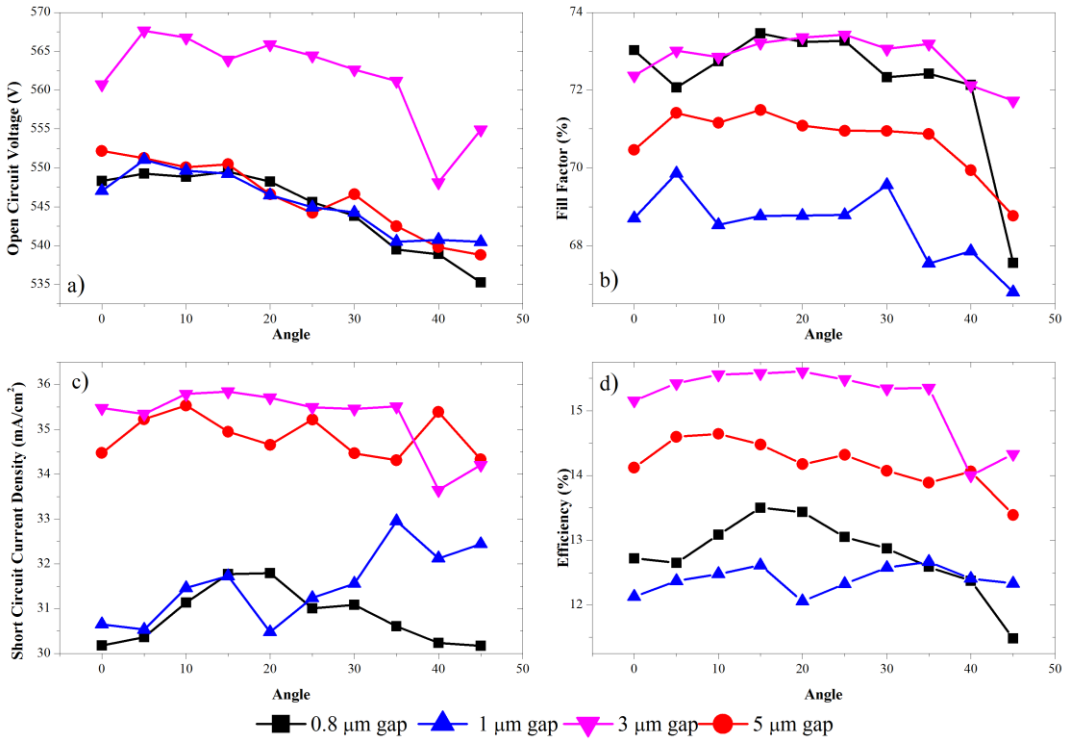


Figure 5.4 Solar cell performances: a) open circuit voltage, b) fill factor, c) short circuit current density, d) efficiency, obtained from the surface with 4 µm diameter 0.8, 1, 3, 5 µm gap, 10.8 µm depth, fabricated with dry plasma etching, between 0° to 45°

Figure 5.4 has the same diameter and gap values just as represented in Figure 5.3. The only difference is the duration of dry plasma etching process. For this sample, the time is 40 s longer than process time of samples in Figure 5.3. The structures were around 2 µm deeper. For 0.8 µm of gap showed an increase up to 20° and then started to decrease which is 15° for 1 µm gap. For 3 µm gap value, after 35° there starts the drop.

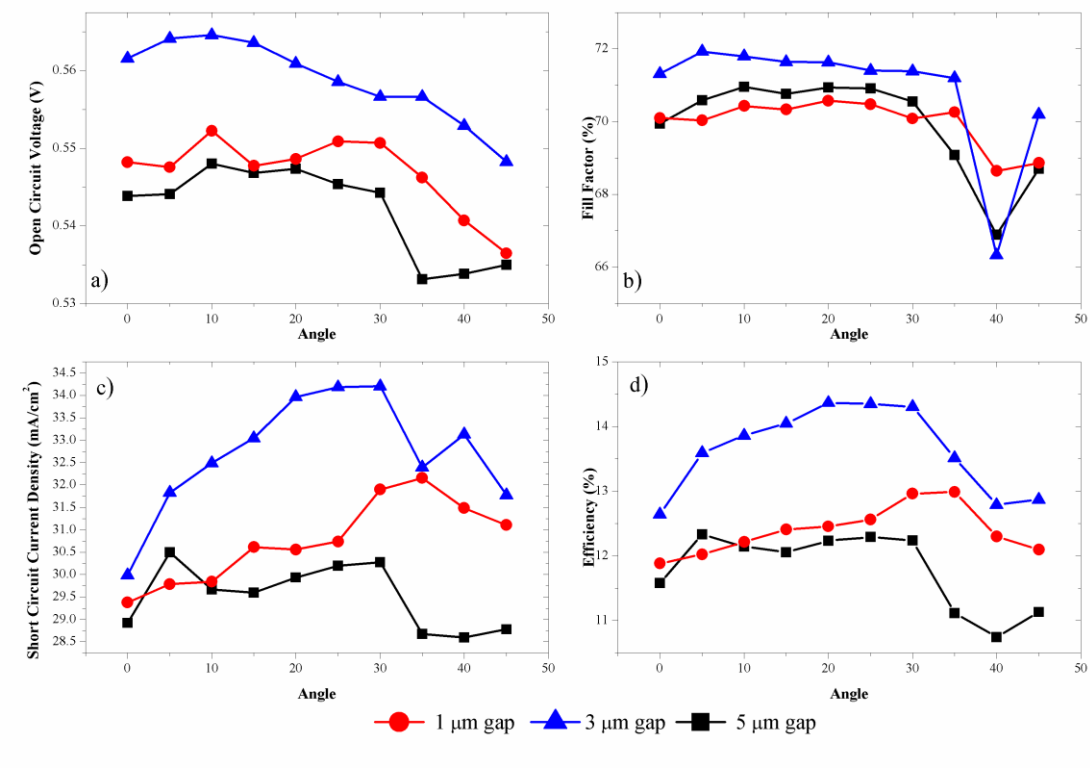


Figure 5.5 Solar cell performances: a) open circuit voltage, b) fill factor, c) short circuit current density, d) efficiency, obtained from the surface with 4 µm diameter 1, 3, 5 µm gap, fabricated with dry plasma etching, between 0° to 45°

When the process time kept too long, which ended up with a depth value of 13 µm, the increase in short circuit current and efficiency could be obtained for the sample having 4 µm diameter and 3 µm gap shown in Figure 5.5. The comparison between other samples patterned on the same wafer, subjected to the same process parameters also shown in Figure 5.7.

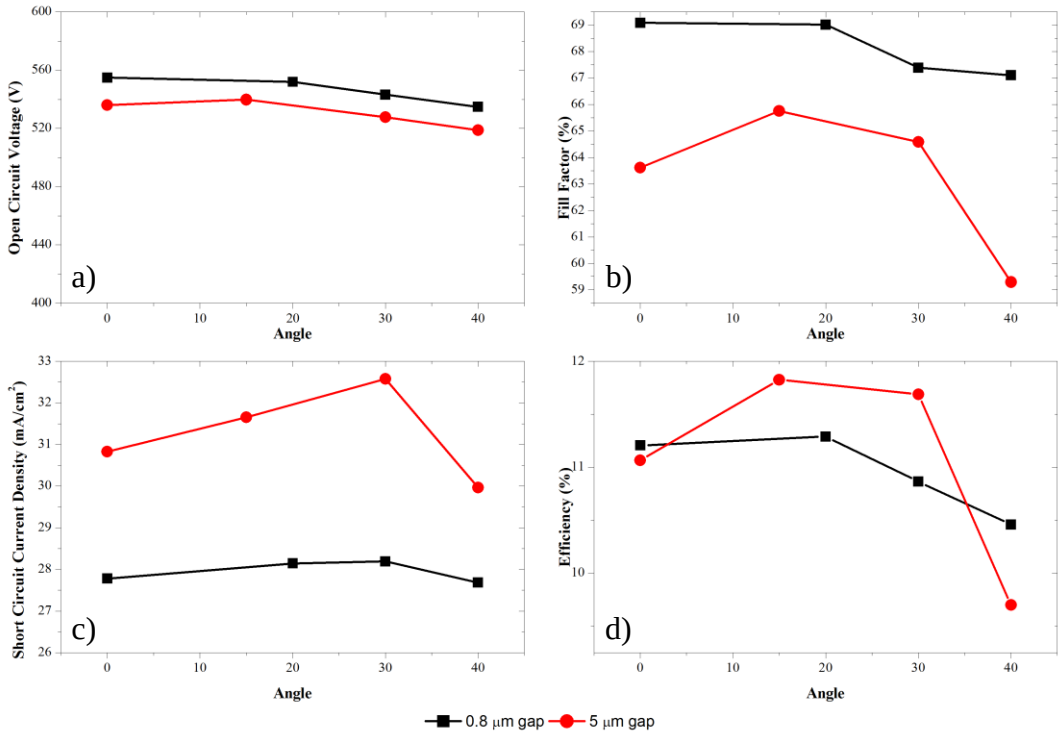


Figure 5.6 Solar cell performances: a) open circuit voltage, b) fill factor, c) short circuit current density, d) efficiency, obtained from the surface with 2 µm diameter 0.8, 5 µm gap, fabricated with dry plasma etching, between 0° to 45°

The samples with different depth, whose solar cell performances shown in Figure 5.6, had different angles. The angles corresponding to depth values are tabulated inTable 5.1.

Table 5.1 The depth and the diameter of the samples were the same which were compared in Figure 5.6

Diameter (µm)	Gap (µm)	Depth (µm)	Angle°
2	0.8	2.9	30
2	5	3.2	25

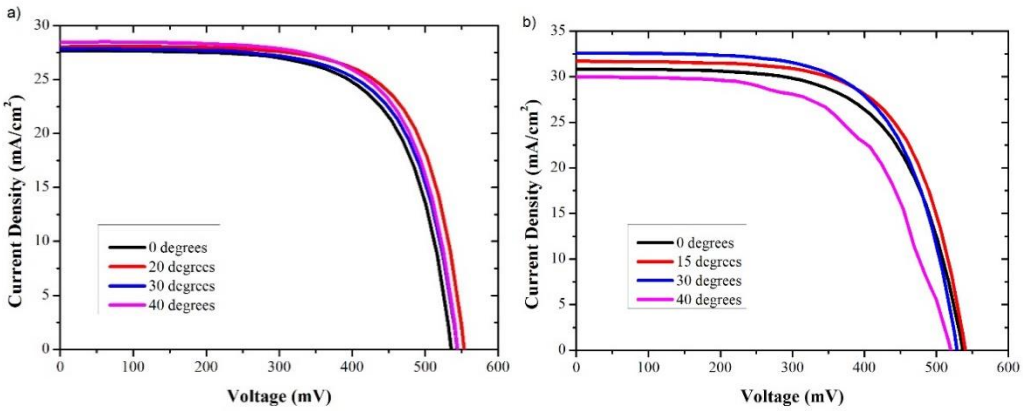


Figure 5.7 Open circuit voltage versus short circuit current density comparison for solar cell performances obtained from the surface with 2 µm diameter: a) 0.8 µm gap, b) 5 µm gap fabricated with dry plasma etching

The depth of the texture depends on its dimension. As shown in Figure 5.7, surface patterned with the same diameter and different gap values will give the highest efficiency value at different angles.

CHAPTER 6

CONCLUSIONS AND FUTURE PERSPECTIVES

In this PhD thesis work, we have investigated structuring the surface of crystalline Si solar cell using top down approaches, patterned with lithography tools having different capabilities. During patterning; optical lithography, nanoimprint, hole colloidal lithography were used. Following the surface patterning with these lithography techniques, suface of c-Si wafer was structured with both dry and wet etching processes. A large variety of pattern dimension and distribution were obtained through process optimizations. We finally fabricated solar cells on some of these surfaces to see their effect on the solar cell performance. Although lithography is not a preferred technique in industrial solar cell manufacturing, it is still the only way of obtaining periodical structures which can be favorable in certain cases. It is also useful for the proof of concept studies.

We have successfully generated periodic structures with the help of lithography techniques mentioned above. Final topography of the surface is determined by the dimension and distribution of hole textures and etching duration. We have achieved to obtain dimensions ranging from wave optic regimet (less than micron) to micro-scale ray optic sytems, which provides a unique platform to study the optical effects of two different rgimet simultanously. Process parameters have been optimized for a good control over the structures and thus optical performance. For instance, the longer etching time leads to deeper holes on the surface, which provided lowest reflection from the surface. When the hole coverage of surface was small, the reflection approaches bare silicon.

Surface patterns obtained using metal assisted etching exhibited better optical performance than those obtained with dry plasma etching. This was because MAE introduced additional nanostructures inside the holes that make the reflection even lower. During MAE experiments, we used metals like gold, silver, titanium as the catalyst for the etching process. The difference in their etch rate ended up with different

depths even for the same process duration. After numerous experimental trials, silver was obtained to be the best metal in terms of process efficiency and resultant optical performance when compared with other metals. However, poor electrical property due to increased surface area and damage is a common problem for all MAE applied samples used for solar cell fabrication. An effective surface passivation method should be developed for a good solar cell performance after MAE.

Nanoimprint lithography process parameters were optimized for different master stamps. When compared with other lithography techniques, the requirements for successful patterning more than once are more complicated, but following an optimization study, we have obtained a maximum number of thirteen. The effective cleaning of master stamps, sufficient silane coating and correct resist thickness led to succesful formation of desired shapes. For thick wafers (~500 μm), the process steps were easier, but when the substrates get thinner (~40 μm), each process step should be carried out in a special way. Thin substrates need to be bonded to another thick substrate. During the imprinting step, a force was applied to make pattern transfer, this force also cause a stress on bonded layers. The thinner the layer is, the more difficult to handle and proceed with it.

Similarly, hole colloidal lithography was performed over both thick and thin substrates using the direct surface self-assembly of beads by the electrostatic force. The attractive force of beads to the surface, and the repulsive force between each other lead to surface assembly of the beads. For thinner layers, the challenges for this technique were similar like nanoimprint process. Especially during wet chemical etching, the beads ended up with more random distribution than expected. In order to improve etchings, beads were immersed and process initiated with dry plasma etching. After a short plasma etching step, wet chemical etching steps were conducted safely.

Hole textured silicon surfaces have been characterized for their optical properties. As expected, the reflection from the surface is reduced drastically by the introduction of hole texturing with respect to the flat Si surface. The degree of reduction depends on the density and the depth of the hole patterns.

Finally solar cells have been fabricated on various hole textured surfaces. The best performing solar cell showed an efficiency value of 15.7%, which is best reported value in the literature so far. This result demonstrates the potential of the use of hole patterning in the solar cell fabrication. The efficiency of the cells increased with

increasing hole depth as a result of improved light trapping leading to higher short circuit current. This result is a direct proof of the light trapping effect of the hole texturing. We epxect to improve the performance values even better with a proper passivation technique.

Table 6.1 Performance of patterned surfaces with NIL, RIE and MAE

Texturing	Jsc (mA/cm^2)	Voc (mV)	FF (%)	η (%)
*900 nm Dry-NIL	15.3	435	72	4.8
*600 nm Dry-NIL	15.4	403	56	3.5
*Dry-HCL	17.2	444	58	4.5
RIE	37.8	569.9	72.8	15.7
MAE	24.2	504.6	69.9	8.5
Flat	20.9	564.9	75.8	9

(*Results are taken from [99])

Table 6.1 summarizes solar cell performances obtained with different patterning and etching tecniques. Solar cell fabrication techniques and the substrate thicknesses were different for the structures fabricated with NIL and HCL. It can be seen that the best performance was obtained from the surface patterned with micro holes subjected to dry plasma etching. This result is not surprizing as RIE is a mature and well behaving technique. Other lithography techniques have not been optimized yet and we can expect to improve them with a more detailed study of optimization.

The angle of incidence is an important factor for the solar cell performance, which has not been studied yet. In most cases the solar modules are fixed on the ground and sun's motion through the day makes the angle of incidence quite variable. In particular, if the surface has three dimensonal structures, like the ones we generated in this study, the angle of incidence might have a significant effect on the solar cell performance. We have shown that the performance of the cell is strongly depending on the angle of incidence of the light. In some cases, the maximum power point is located at an angle different than the normal direction.

The performances of solar cells can be improved with better passivation techniques. Especially nano wires inside the micro holes require extra process optimization. The successful passivation can be achieved with more conformal coating

with atomic layer deposition. We have applied standrd SiNx passivation in this study. With different types of material coatings the results can be improved. Especially, use of Al_2O_3 can be quite promising and applicable to the hole textures produced in this work.

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EDUCATION

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Mersin University	Electrical and Electronics Engineering	M.S.	Turkey	2005-2007
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WORK EXPERIENCE

Institution	Title	Subject	Dates
IMEC- Belgium	Visiting Scholar	PhotoNVoltaics, European Union 7th Framework Program	15/12/2014-15/06/2015
Arizona State University	Visiting Scholar	Simulation studies of textured solar cells	01/04/2014-01/09/2014
The Scientific and Technological Research Council of Turkey, 1001 Project- TÜBİTAK 107E153	Project Assistant	Therapeutic Capacitive Micromachined Ultrasound Transducers with Diamond Membranes	31/12/2007-31/12/2010
PEGAS-EMO	Project Engineer	System designer	01/06/2004-01/09/2007

AREAS OF EXPERTISE

Micro electro mechanical systems, material processing and characterization at micro and nano scale, surface texturing, process optimization, solid state electronic devices, solar cells, nanoimprint lithography, hole colloidal lithography, reactive ion etching, simulation, silvaco, design, production and development of textured surfaces for efficient and low-cost solar cells.

PUBLICATIONS IN JOURNALS

1. Serra H. Altınoluk, Hande E. Çiftpınar, Olgu Demircioğlu, Rasit Turan, Periodic micro hole texturing with metal assisted chemical etching for solar cell applications: dependence of etch rate on orientation, Cogentphys, under revision.
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REFEERED CONFERENCE PAPERS

1. Serra H. Altınoluk, Hande E. Çiftpınar, Olgu Demircioğlu, Fırat Es, Gulsen Baytemir, Orhan Akar, Akın Aydemir, Adem Saraç, Tayfun Akın, Raşit Turan, Light trapping by micro and nano-hole texturing of single-crystalline silicon solar cells, 6th International Conference on Silicon Photovoltaics, Silicon PV 2016, Energy Procedia 00 (2016), http://dx.doi.org/10.1016/j.egypro.2016.07.081
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3. Serra H. Altınoluk, Hande E. Çiftpınar, Olgu Demircioğlu, Fırat Es, Gulsen Baytemir, Orhan Akar, Akın Aydemir, Adem Saraç, Tayfun Akın, Raşit Turan, Micro and nano-hole texturing single crystalline silicon wafer for solar cell applications: effects of hole diameter and distribution, Materials Research Society 2016, Phoenix, poster presentation.