PHASE LOCKED DIELECTRIC RESONATOR OSCILLATOR DESIGN
AND FABRICATION FOR RECEIVER SYSTEMS

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
MIDDLE EAST TECHNICAL UNIVERSITY

BY
REMZİ KÖKSAŁ

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF MASTER OF SCIENCE
IN
ELECTRICAL AND ELECTRONICS ENGINEERING

AUGUST 2016
Approval of the thesis:

PHASE LOCKED DIELECTRIC RESONATOR OSCILLATOR DESIGN AND FABRICATION FOR RECEIVER SYSTEMS

submitted by REMZİ KÖKSAL in partial fulfillment of the requirements for the degree of Master of Science in Electrical and Electronics Engineering Department, Middle East Technical University by,

Prof. Dr. Gülbin Dural Unver
Dean, Graduate School of Natural and Applied Sciences

Prof. Dr. Tolga Çiloğlu
Head of Department, Electrical and Electronics Engineering

Prof. Dr. Sencer Koç
Supervisor, Electrical and Electronics Engineering Dept., METU

Examining Committee Members:

Prof. Dr. Şimşek Demir
Electrical and Electronics Engineering Dept., METU

Prof. Dr. Sencer Koç
Electrical and Electronics Engineering Dept., METU

Prof. Dr. Özlem Aydınlı Çivi
Electrical and Electronics Engineering Dept., METU

Assistant Prof. Fatih Koçer
Electrical and Electronics Engineering Dept., METU

Associate Prof. Asım Egemen Yılmaz
Electrical and Electronics Engineering Dept., AU

Date: 24.08.2016
I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

Name, Last name : Remzi KÖKSAL
Signature :
Oscillators play an important role in transmitters and receivers. In these systems, stable frequency source and low phase noise are critical for system performance. In radio frequencies, phase locked dielectric resonator oscillators are one of the best options in terms of cost, dimension, and performance. These oscillators are widely used in systems such as RADAR, electronic warfare, and communication. In this thesis, design methodology of phase locked dielectric resonator oscillator is given, an oscillator at 8 GHz is designed, produced and measured. The oscillator output power at the design frequency is measured to be 13 dBm, and the phase noise drops down to -134 dBc/Hz at 1 MHz offset.

This thesis contains the details of the design, simulation, and fabrication procedure of a low phase noise phase locked dielectric resonator oscillator.

Keywords: Phase locked dielectric resonator oscillator, phase noise
ÖZ

ALMAÇLAR İÇİN FAZ KİLİTLEMELİ DİELEKTRİK REZONATÖRLÜ OSİLATÖR TASARIMI VE GERÇEKLENMESİ

Köksal, Remzi
Yüksek Lisans, Elektrik ve Elektronik Mühendisliği Bölümü
Tez Yöneticisi : Prof. Sencer Koç
Ağulos 2016, 95 sayfa

Osilatörler alma gönderme sistemlerinde önemli bir rol oyanlar. Bu sistemlerde sabit osilasyon kaynakları ve düşük faz gürültüleri, sistem performansı bakımından önemlidir. Radyo dalga frekanslarında, faz kilitleme döngülü dielektrik resonator osilatörler fiyat boyut ve performans açısından en iyi seçeneklerden biridir. Bu osilatörler RADAR, elektronik harp ve haberleşme alanlarında sıkça kullanılmaktadır. Bu tezde, faz kilitleme döngülü dielektrik resonatorun tasarım yöntemi verilmiş ve 8 GHz frekansında bir osilatör tasarlanmıştır, üretilmiş ve ölçülmüştür. Tasarlanan osilatörün çıkış gücü 13 dBm ve osilasyon frekansından 1MHz uzaklıkta faz gürültüsü -134dBc/Hz olarak ölçülmüştür.

Bu tez çalışması, düşük faz gürültülü faz kilitleme döngülü dielektrik resonator osilatör için tasarım, benzetim ve gerçekleme yöntemlerini içermektedir.

Anahtar kelimeler: faz kenetlemeli dielektrik rezonatörlü osilatör, faz gürültüsü
to the memory of my father
ACKNOWLEDGEMENTS

I would like to thank Prof. Sencer Koç for his guidance and support throughout this thesis study.

I would like to thank Şebnem Saygın, Mustafa Akkul, Hakkı İlhan Altan, Halil İbrahim Atasoy, Taylan Eker for their valuable suggestions and support throughout this study. Moreover, I wish to my appreciation to Onur Ö zgür and Arda Özgen for their great effort during the mechanical design of the module.

I would like to thank ASELSAN Inc. for allowing me to use their facilities for design, fabrication and measurement.

Finally, I want to express my deepest gratitude to my lovely family for supporting and encouraging me.
TABLE OF CONTENTS

ABSTRACT ................................................................................................................ v
ÖZ .............................................................................................................................. vi
ACKNOWLEDEGEMENTS ...................................................................................viii
TABLE OF CONTENTS ........................................................................................ ix
LIST OF TABLES .................................................................................................... xii
LIST OF FIGURES .................................................................................................xiii
LIST OF ABBREVIATIONS .................................................................................. xvi
1. INTRODUCTION .................................................................................................. 1
   1.1. Motivation of the Thesis ................................................................................ 1
   1.2. Brief Historical Background ......................................................................... 2
   1.3. Thesis Overview ............................................................................................ 2
2. PHASE NOISE IN OSCILLATORS ...................................................................... 5
   2.1. Introduction ................................................................................................... 5
   2.2. Phase Noise Models ...................................................................................... 6
   2.3. Local Oscillator Phase Noise Considerations for Receiver Systems .......... 8
3. DIELECTRIC RESONATOR .............................................................................. 11
   3.1. Introduction ................................................................................................... 11
   3.2. Dielectric Resonator Design by Using EM Solver ...................................... 16
   3.3. Coupling of the resonator ............................................................................ 21
   3.4. Resonator Frequency Tuning ...................................................................... 25
      3.4.1 Metal Tuning Screw ................................................................................... 26
3.4.2 Dielectric Tuning Screw

4. OSCILLATOR DESIGN

4.1 Oscillator Theory

4.2 Negative Resistor Oscillator Design

4.2.1 Active Device with Feedback

4.2.2 Resonator

4.2.3 Oscillation Matching

4.3 DRO Design and Simulations

4.3.1 Series Feedback DRO

4.3.2 Parallel Feedback DRO

4.4 Varactor Tuned DRO

5. PHASE LOCKED LOOP DESIGN

5.1 PLL Blocks

5.1.1 Sampling Phase Detector

5.1.2 Loop Filter

5.1.3 Acquisition Circuit

5.2 PLL Design for Voltage Controlled DRO

5.3. Phase Noise Contributions

6. MEASUREMENT RESULTS

6.1 Phase Noise Measurements

6.2 Output Power

6.3 PLL Performance

6.4 Thermal Measurement Tests

7. CONCLUSION
LIST OF TABLES

TABLES

Table 3.1 Comparison of resonator with respect their properties ......................... 12
Table 3.2 Resonant frequency, quality factor and insertion loss with respect to
diameter ...................................................................................................................... 19
Table 3.3 Resonant frequency, quality factor and insertion loss with respect to height
.................................................................................................................................... 20

As expected and seen Table 3.2 and 3.3, resonant frequency increases when
dimension of the resonator decreases. Variation of resonant frequency with respect to
dimensions are shown graphically in Figure 3.7 and Figure 3.8 ......................... 20
Table 3.4 Resonant frequency, quality factor and insertion loss with respect to
distance between DR and microstrip line ................................................................. 24
Table 4.1 Tuning Range with respect to length of TLs ............................................ 53
Table 6.1 Frequency Offset vs. Phase Noise .............................................................. 82
Table 6.2 Temperature Performance for Multiplication factor 80 ............................. 88
Table 6.3 Temperature Performance for Multiplication factor 40 ............................. 89
LIST OF FIGURES

FIGURES
Figure 2.1 Phase Noise Spectrum of Leeson’s’ Model (figure a is for low Q, figure b is for high Q)................................................................................................................ 7
Figure 2.2 Phase Noise Modulated with input Signals ................................................ 9
Figure 4.1 Linear Feedback System........................................................................... 29
Figure 4.2 Microwave network.................................................................................. 30
Figure 4.3 Location of Poles and time domain behaviors................................. 31
Figure 4.4 Change of location of poles in oscillators (start-up to steady state condition .................................................................................................................................... 31
Figure 4.5 Main Oscillator Topology......................................................................... 32
Figure 4.6 Series Feedback of RF Transistor with transmission line and inductor (biasing is not shown).................................................................................................................. 38
Figure 4.7 Parallel Feedback of RF Transistor with transmission line (biasing is not shown)......................................................................................................................................... 38
Figure 4.8 Input and Output Stability Circles ............................................................ 39
Figure 4.9 Resonator active device and matching network (bias is not shown)....... 41
Figure 4.10 Single Stub Matching Network .......................................................... 42
Figure 4.11 Series Feedback Transistor Scheme .................................................... 43
Figure 4.12 Stability Factor of Series Feedback Amplifier .................................... 44
Figure 4.13 S parameters of Series Feedback Amplifier (dB)................................... 44
Figure 4.14 Dielectric Resonator and unstable Amplifier ..................................... 45
Figure 4.15 Output Impedance................................................................................ 45
Figure 4.16 DRO Schematic .................................................................................. 46
Figure 4.17 Output Impedances plus Source Impedances ....................................... 46
Figure 4.18 Output Power Simulation (dBm).......................................................... 47
Figure 4.19 Parallel Feedback DRO ........................................................................ 48
Figure 4.20 Output Impedance................................................................................ 48
Figure 6.2 Designed PLDRO Module................................................................. 80
Figure 6.3 Inside view of the PLDRO Module ..................................................... 80
Figure 6.4 Phase Noise Measurement............................................................... 82
Figure 6.5 Fundamental Oscillator Signal ......................................................... 83
Figure 6.6 Fundamental frequency and its harmonics ........................................ 84
Figure 6.7 Varactor tuning voltage at steady state.............................................. 85
Figure 6.8 Varactor tuning voltage at out of locking range ................................ 85
Figure 6.9 Varactor voltage vs time (case abruptly decrease in reference frequency) ........................................................................................................ 86
Figure 6.10 Varactor voltage vs. time (case abruptly increase in reference frequency) .......................................................................................................... 87
Figure 6.11 Varactor Tuning Voltage Vs Temperature with multiplication factor 80 ............................................................ 89
Figure 6.12 Tuning Voltage Vs Temperature with multiplication factor 40 .......... 89
**LIST OF ABBREVIATIONS**

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DR</td>
<td>Dielectric Resonator</td>
</tr>
<tr>
<td>DRO</td>
<td>Dielectric Resonator Oscillator</td>
</tr>
<tr>
<td>PLDRO</td>
<td>Phase Locked Dielectric Resonator Oscillator</td>
</tr>
<tr>
<td>PLL</td>
<td>Phase Locked Loop</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>SRD</td>
<td>Sampling Recovery Diode</td>
</tr>
<tr>
<td>SPD</td>
<td>Sampling Phase Detector</td>
</tr>
<tr>
<td>VCO</td>
<td>Voltage Controlled Oscillator</td>
</tr>
<tr>
<td>Q</td>
<td>Quality Factor</td>
</tr>
<tr>
<td>I.L</td>
<td>Insertion Loss</td>
</tr>
<tr>
<td>K</td>
<td>Rollet Stability Factor</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuit</td>
</tr>
<tr>
<td>VHF</td>
<td>Very High Frequency</td>
</tr>
<tr>
<td>HF</td>
<td>High Frequency</td>
</tr>
</tbody>
</table>
CHAPTER 1

INTRODUCTION

1.1. Motivation of the Thesis

Oscillators are essential for communication systems, digital systems, and instrumentation. In communication systems, carrier frequency is formed by oscillators, and frequency up down converters also use oscillators. In digital electronics, clock circuitry is implemented by oscillators. Thus, in electronic world oscillators are vital components.

Properties of oscillators are significant for system performance. For communication applications, the most important property of oscillator is phase noise; for example, excessive phase noise might degenerate receiver performance. Output power is also critical since output power of oscillator must be high enough to drive mixer or amplifier. In addition to that for both analog and digital circuit, frequency of oscillation must remain constant for short and long period of time, phase locked loop is generally used to stabilize frequency of oscillation. In general sense, phase noise, output power level, and stability of oscillation frequency are main concern of oscillators.

In microwave frequencies, type of resonator is one of the most critical consideration for low phase noise, cost, dimension, and producibility. Planar transmission lines resonators are preferable in terms of cost and mass production, however its quality factor might not be sufficient for low phase noise. Dielectric resonators could be good choice in terms of quality factor, and its dimension. Moreover, dimension of dielectric resonator is lower than cavity resonators despite their quality factors are similar. On the other hand, dielectric resonator oscillator might not be suitable for high volume production, since dielectric resonator oscillator requires post fabrication tuning. In
spite of disadvantages of dielectric resonator, it is convenient to use in terms of its quality factor, cost, and dimension.

Dielectric resonator oscillators are widely used in today’s electronic warfare, missiles, RADARs and communication systems. In this thesis, design methodology of dielectric resonator oscillator integrated with phase locked loop is explained step by step, and design is verified by measurements. Main aim of the thesis is to gain perspective on design of phase locked dielectric resonator oscillator.

1.2. Brief Historical Background

First time, in 1939 Robert D. Richthmer conducted a study showing that unmetallized dielectric structures have resonator properties similar to metallic cavities [1]. He also showed that, dielectric resonators can radiate due to boundary conditions between air and dielectric material. These results are used to develop dielectric resonators and dielectric resonator antennas. In the late 1960s dielectric resonators used as a resonator in waveguide filters [2]. In today’s technology dielectric resonators can be produced in any shape and any physical properties such as small dielectric loss, controllable dielectric constant, and controllable thermal coefficients. Today’s technology allows us to use dielectric resonators in microwave applications such as oscillators, filters, and antennas [3]. Dielectric resonators are being used in oscillators since 1970 [4]

1.3. Thesis Overview

This thesis focuses on design and construction of phase locked dielectric resonator oscillator (PLDRO) which is fabricated and measured to verify design. In this part, thesis overview is given for each chapter.

In chapter 2, fundamentals of noise in electrical circuits is given briefly, then phase noise models are summarized. Effects of phase noise on system performance are mentioned in this section.
In chapter 3, general properties of resonators are introduced, and design considerations of dielectric resonator (DR) by using an electromagnetic solver are explained. Additionally, coupling mechanism of DR is mentioned and mechanical tuning methods for resonant frequency is given.

In chapter 4, firstly fundamentals of oscillators is given. Secondly, negative resistance method for microwave oscillators is explained and oscillation conditions related with this method are given. Thirdly, design techniques and algorithms of DRO by using harmonic balance and linear simulation tool is also given in this part. Finally, varactor tuned DRO design considerations is mentioned.

In chapter 5, basics of PLL is mentioned, and PLL components which are used in this work are explained. In addition to that by assuming linear behavior, PLL performance of DRO is simulated in time domain. Effects of PLL to the output phase noise is also given in this chapter.

In chapter 6, measurement results of prototype are given by considering thermal variations.

In chapter 7, the work is summarized, and future works are stated in conclusion.
CHAPTER 2

PHASE NOISE IN OSCILLATORS

2.1. Introduction

In this part of the thesis; basics of noise and phase noise are explained briefly. Electrical circuits are composed of resistors, and transistors which can be regarded as noise generators in circuits. In resistors, electrons move in random directions with directly proportional to temperature, and noise in resistor can be modelled as thermal or white noise [5]. For transistors or diodes, noise is generated due to energy levels of carriers in p-n junctions, this noise is called as shot noise and can be modelled by a Poisson process. In addition to that field effect transistors generate noise due to impurities in conductive channel, this noise is frequency depended due to gate capacitance and is called 1/f noise or flicker noise. Furthermore, inductors and capacitors can be regarded as noiseless elements, however their parasitic resistance generates noise. Even if capacitors and inductors are assumed as noiseless, spectral density of noise is affected by capacitor and inductor due to frequency response of these elements [5].

Oscillators are also composed of resistors, transistors, and resonators. Resistors and transistors are noise generators in oscillator, and generated noise is shaped in frequency domain due to frequency response of resonators. Output of an oscillator could be written as

\[ y(t) = (A + \tilde{a}(t)) \sin(\omega t + \theta(t)) \]  

(2.1)

where \( A \) is amplitude, \( \tilde{a} \) is noise in amplitude with zero mean, and \( \theta(t) \) is phase noise.
Noise of an oscillator is critical for some applications, for example probability of correct detection in receiver highly depends on phase noise of local oscillator. In digital world, jitter noise may have catastrophic effects on clock or information signal.

Phase noise of an oscillator can be modelled in terms of quality factor, noise figure, output power and corner frequency of flicker noise which is examined in next section.

### 2.2. Phase Noise Models

Spectral purity of an oscillator, quantified in terms of phase noise is the most critical parameter for RF, wireless communication and digital electronic systems so prediction of phase noise is required to satisfy desired phase noise. Many models have been developed to predict phase noise.

The most well-known phase noise model is Leeson’s model which was proposed in 1966. This model is based on linear time invariance feedback approach and model is in good agreement for LC resonators. Leeson’s phase model can be written as [6]

$$
L(\Delta f) = 10 \log \left( \frac{\frac{FkT}{2P_{out}}}{fo} + \left( \frac{fc}{fcQ_L} \right)^2 \left( 1 + \frac{fc}{fo} \right) \right) \tag{2.2}
$$

where $F$ is noise figure, $fc$ is corner frequency of flicker noise, $P_{out}$ is output power in watt, $Q_L$ is loaded quality factor of resonator, and $k$ is Boltzmann constant.

In spectrum, Leeson’s model basically can be observed as in Figure 2.1. For low $Q$ oscillators spectrum is observed as in Figure 2.1.a whereas for high $Q$ oscillator phase noise is observed as in Figure 2.1.b
Other phase noise model is Razavi’s model, this model is also based on linear assumptions. In contrast to Leeson’s model, this model can predict phase noise of inductorless CMOS differential ring oscillators. Razavi’s phase model can be written as [7]

\[ L(\Delta f) = 10 \log \left\{ \frac{8}{3} \frac{kT}{P_{out}} \frac{f_0}{\Delta f} \right\}^2 \]  

(2.3)

Another phase noise model is Hajimiri’s model which is based on linear time variant assumptions based on integral equations [8]. Non-linear model is also available which is developed by Alper Demir. Demir’s model is purely mathematical and CAD oriented, and it can be described by one dimensional differential equation [9]. Readers who are interested in those model refer to inside papers [6] [7] [8] [9].
2.3. Local Oscillator Phase Noise Considerations for Receiver Systems

All receivers use one or more local oscillator to convert carrier frequency to intermediate frequency before signal is demodulated. In ideal case, these frequency conventions should not distort to signal and all information on the signal could be recovered, whereas in real world both mixer and local oscillator distort the signal and limit the receiver’s ability to recover signal. Mixer degradations could be minimized by proper design whereas phase noise of local oscillator could not be decreased except by improving oscillator performance. Mainly, frequency modulated or phase modulated signal degraded due to phase noise of oscillator, and bit error rates also are increased by phase noise. Thus for proper receiver operation phase noise specification should be clearly defined [10].

For communication applications, channel noise and phase noise degrade the signal to noise ratio so in signal constellation diagram random distribution is observed around signal points. If noise is too high and signal constellation diagram has too many signal points such as 256QAM, false detections would be observed.

For RADAR and electronic warfare applications, except for desired input signal, interference signals might also be detected by receiver. All received signals are modulated by phase noise of local oscillator as shown in Figure 2.2. If power level of interference signal is high, desired signal might be under the modulated phase noise of interference, and weaker signal might not be detected. Thus, noise floor of receiver is increased by phase noise of interference signals.
Besides the phase noise, local oscillator which is constructed by PLL might have spurious signals on phase noise. If spurious is in video bandwidth, probability of false detection increases.

To conclude, local oscillator phase noise and mixer performance effect the overall performance of receiver. Phase noise of a local oscillator is main concern for high performance receivers.
CHAPTER 3

DIELECTRIC RESONATOR

3.1. Introduction

Resonator is a frequency selective network which resonates at particular frequencies. In microwave, they are used in filters, oscillators, and antennas which require frequency selective networks. There are many types of microwave resonators so selection of the resonator is a critical point before designing oscillator. Which resonator should be used, can be determined with respect to application and requirements, In Table 3.1 some properties of resonators are given [11].

Quality factor of a resonator is a critical parameter since noise performance of an oscillator and bandwidth of a filter depends on quality factor. Quality factor can be defined as [11]

$$Q = \omega \frac{\text{average energy stored}}{\text{energy loss/second}}$$  (3.1)

This expression indicates that if losses in resonator increases quality factor decreases, and if coupling of resonator increases, average energy stored in resonator diminish so Q decreases. Thus, to ensure high quality factor; microwave losses and coupling should be low as possible; however, without coupling, there is no power transfer between a resonator and a feedline. To obtain maximum power transfer, the resonator must be matched to the feedline at the resonant frequency. In practice a resonant circuit is invariably coupled to other circuitry, which will always have the effect of lowering the overall, or loaded Q of the circuit. [11].

Loaded quality factor can be defined as
\[ Q_L = \frac{\omega_r}{3\text{dB BW}} \]  

(3.2)

where \( \omega_r \) is resonant frequency.

For oscillator applications, \( Q_L \) and coupling should be high enough for low phase noise and sufficient coupling.

Dimension and cost are also critical parameters as quality factor. In this work, dielectric resonator is selected because its quality factor is high enough at microwave frequencies and it is generally smaller in cost, size, and weight than an equivalent metallic cavity, and can very easily be incorporated into microwave integrated circuits and coupled to planar transmission lines [11].

Table 3.1 Comparison of resonator with respect their properties

<table>
<thead>
<tr>
<th>Type of Resonator</th>
<th>Quality Factor</th>
<th>Dimension</th>
<th>Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cavity Resonator</td>
<td>High</td>
<td>Large</td>
<td>Low</td>
</tr>
<tr>
<td>Microstrip Resonator</td>
<td>Low</td>
<td>Small</td>
<td>Low</td>
</tr>
<tr>
<td>Coaxial Resonator</td>
<td>Moderate</td>
<td>Moderate</td>
<td>Low</td>
</tr>
<tr>
<td>Dielectric Resonator</td>
<td>High</td>
<td>Moderate</td>
<td>Moderate</td>
</tr>
<tr>
<td>Ferrite YIG Resonator</td>
<td>High</td>
<td>Small</td>
<td>Moderate</td>
</tr>
<tr>
<td>LC Resonator</td>
<td>Very Low</td>
<td>Small</td>
<td>Low</td>
</tr>
</tbody>
</table>

Dielectric resonator is a disc shaped dielectric material which is composed of Ba (Ca Ta Mg Zr) oxide. Its dielectric constant is 10 to 120 and its temperature coefficient of resonant frequency (\( \tau_f \) (ppm/°C, 25° to 60°C) is between -3 and +9 which is quite reasonable for oscillator applications; and its unloaded quality factor is 3000 to 35000
depending on its operation frequency and dielectric constant [12]. Dielectric resonator is also used for band pass tunable filters and dielectric resonator antennas (DRA).

For oscillator applications usually TE$_{01\delta}$ resonant mode is used. Analytical solution of dielectric resonator is given below [11].

Since dielectric constant of resonator is much higher than dielectric constant of air, walls of resonator act as an open boundary. For simplicity of analytical analysis, PMC side wall and dielectric boundary for top and bottom surface can be assumed. Geometry of resonator is shown in Figure 3.1

![Figure 3.1 Geometry of DR](image)

For TE$_{01}$ circular dielectric waveguide mode $E_z = 0$ and $H_z$ must satisfy the wave equation

$$ (\nabla^2 + k^2)H_z = 0 \quad \text{(3.3)} $$

$$ k = \sqrt{\varepsilon_r}k_0 \quad \text{for} \ |z| \leq \frac{L}{2} \quad \text{and} \quad k = k_0 \quad \text{for} \ |z| \geq \frac{L}{2} $$

The solution of (3.3) has circular symmetry, so solution of $H_z$ is Bessel function of first kind since $H_z$ is finite at $r = 0$. Since TE$_{01}$ mode is considered, index of Bessel function is zero. Thus, solution of $H_z$ is given as
\[ H_z = H_0 J_0(k_c r) e^{\pm j \beta z} \]  \hspace{1cm} (3.4)

where \( k_c^2 = k^2 - \beta^2 \)

Due to PMC boundary condition \( H_z \) must be zero at \( r = a \)

so; \( J_0(p_{01}) = 0 \) \( (p_{01} = 2.405) \) and \( k_c = \frac{p_{01}}{a} \)

Since \( \partial E / \partial \phi = 0 \)

\[ E_\phi = \frac{j \omega \mu_0}{k_c^2} \frac{\partial H_z}{\partial r} \]  \hspace{1cm} (3.5)
\[ H_r = -\frac{j \beta}{k_c^2} \frac{\partial H_z}{\partial r} \]  \hspace{1cm} (3.6)

By substituting \( H_z \); \( E_\phi \) and \( H_r \) can be found as

\[ E_\phi = \frac{j \omega \mu_0 H_0}{k_c} J'_0(k_c r) e^{\pm j \beta z} \]  \hspace{1cm} (3.7)
\[ H_r = \frac{\pm j \beta H_0}{k_c} J'_0(k_c r) e^{\pm j \beta z} \]  \hspace{1cm} (3.8)

for \( |z| \leq \frac{L}{2} \), propagation constant can be written as

\[ \beta = \sqrt{\varepsilon_r k_0^2 - k_c^2} \]  \hspace{1cm} (3.9)

Propagation constant is real valued in dielectric.

In air region \( (|z| \geq \frac{L}{2}) \) propagation constant will be imaginary so it is convenient to write
\[ \alpha = \sqrt{k_c^2 - k_0^2} \quad (3.10) \]

From symmetry, the \( H_z \) and \( E_\varphi \) field distributions for the lowest-order mode will be even functions about \( z = 0 \). Thus the transverse fields for the \( \text{TE}_{01\delta} \) mode can be written for \( |z| < L/2 \) as

\[
E_\varphi = A J_0(k_c r) \cos(\beta z) \quad (3.11)
\]

\[
H_r = \frac{\pm j \alpha B}{\omega \mu_0} J_0(k_c r) \sin(\beta z) \quad (3.12)
\]

for \( |z| > L/2 \) fields can be written as

\[
E_\varphi = B J_1'(k_c r) e^{-\alpha |z|} \quad (3.13)
\]

\[
H_r = \frac{\pm j \beta A}{\omega \mu_0} J_0'(k_c r) e^{-\alpha |z|} \quad (3.14)
\]

where \( A \) and \( B \) are unknown amplitude coefficients. In (3.14), the \( \pm \) sign is used for \( z > L/2 \) and \( z < -L/2 \), respectively.

Tangential electric fields must be continue at top and bottom boundary, and tangential magnetic fields must be continue at \( z = \pm L/2 \). Thus by equating (3.11) and (3.13) at \( z = \pm L/2 \), and by equating (3.12) and (3.14) at \( z = \pm L/2 \) unknown amplitude coefficients \( A \) and \( B \) reduce so wave characteristic equation can be written as

\[
\tan \frac{\beta L}{z} = \frac{\alpha}{\beta} \quad (3.15)
\]

For resonant frequency, equation (3.15) can be solved numerically as a function of dielectric constant and dimensions of the resonator [11]. However, this equation is an approximate solution since fringing fields are ignored; moreover, in practice dielectric resonator is enclosed by a module cavity whose dimensions also affects the resonant
frequency. Thus, to obtain more accurate solution, a numerical EM solver should be used.

![Figure 3.2 Magnetic field intensity around dielectric resonator](image)

Magnetic field around dielectric resonator is shown in Figure 3.2. Due to fringing fields around side walls, resonator can be coupled to microstrip line. Coupling ratio can be adjusted by changing distance between DR and microstrip. If that distance is decreased, coupling increases; whereas loaded quality factor decreases.

### 3.2. Dielectric Resonator Design by Using EM Solver

In this part of the thesis, numerical solution of the dielectric resonator coupled to microstrip line is explained. Since analytical solution of dielectric resonator in module cavity is not possible, numerical solution is required. In this work CST is used for EM solutions.

Simulation environment of DR coupled to microstrip is given in Figure 3.3 and Figure 3.4. In these figures; there are two microstrip lines; the long length transmission line is the feedline of the resonator, and short one is required for electronic tuning of the resonant frequency. Varactor diode will be coupled through the short length microstrip line; by tuning the varactor bias voltage, resonant frequency of DR can be tuned within 10MHz.
There is a tuning screw above the DR, which is necessary for mechanical tuning of the resonant frequency. By changing the height of the tuning screw, resonant frequency can be varied a several hundred MHz’s. Distance between DR and carrier of the module also affects the resonant frequency and quality factor.

Figure 3.3 Numerical solution environment

Figure 3.4 Cross-section view of simulation setup

Resonant frequency of uncovered DR can be found approximately [13].

\[ f_{GHz} = \frac{34}{a \sqrt{\varepsilon_r}} \left( \frac{a}{L} + 3.45 \right) \]  

(3.16)
where \( a \) is the radius of DR in mm, \( L \) is the height of DR in mm, and \( \varepsilon_r \) is dielectric constant of the DR.

In addition to that, height range of DR should be 35% to 45% of the resonator’s diameter; otherwise, other modes of the resonator could close near \( \text{TE}_{015} \) mode. [14]

As a starting point, equation (3.16) could be used; however, this equation is very crude and it is valid for no metallic cavity enclosure. For this reason, actual resonant frequency is higher than approximation (3.16) [13]. Thus, by using (3.16) radius of DR is selected as 3.875mm and height of DR is selected as 3.05mm that corresponds to 7.5GHz for (3.16) whereas, according to EM solver, actual resonant frequency of this DR is approximately 8GHz due to metal enclosure and tuning screw. Scattering parameters of DR are shown in Figure 3.5 and Figure 3.6.
In simulation tool, tuning could be useful to satisfy desired resonant frequency, quality factor and insertion loss. In Table 3.2 and Table 3.3, resonant frequency, quality factor and insertion loss are shown with respect to radius and height.

Table 3.2 Resonant frequency, quality factor and insertion loss with respect to diameter

<table>
<thead>
<tr>
<th>Diameter(mm)</th>
<th>Resonant Frequency(GHz)</th>
<th>Loaded Q</th>
<th>Insertion loss(dB) at resonance</th>
</tr>
</thead>
<tbody>
<tr>
<td>7.65</td>
<td>8.1055</td>
<td>4050</td>
<td>-7.37</td>
</tr>
<tr>
<td>7.70</td>
<td>8.0710</td>
<td>4030</td>
<td>-7.19</td>
</tr>
<tr>
<td>7.75</td>
<td>8.0385</td>
<td>4400</td>
<td>-6.85</td>
</tr>
<tr>
<td>7.80</td>
<td>8.0060</td>
<td>4000</td>
<td>-7.22</td>
</tr>
<tr>
<td>7.85</td>
<td>7.9735</td>
<td>3800</td>
<td>-7.03</td>
</tr>
</tbody>
</table>

Figure 3.6 $S_{21}$ of Dielectric Resonator; diameter 7.75mm and height 3.05mm
Table 3.3 Resonant frequency, quality factor and insertion loss with respect to height

<table>
<thead>
<tr>
<th>Height (mm)</th>
<th>Resonant Frequency (GHz)</th>
<th>Loaded Q</th>
<th>Insertion loss (dB) at resonance</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.95</td>
<td>8.1145</td>
<td>4050</td>
<td>-6.98</td>
</tr>
<tr>
<td>3.00</td>
<td>8.0760</td>
<td>4250</td>
<td>-7.00</td>
</tr>
<tr>
<td>3.05</td>
<td>8.0385</td>
<td>4400</td>
<td>-6.85</td>
</tr>
<tr>
<td>3.10</td>
<td>8.0005</td>
<td>4200</td>
<td>-7.26</td>
</tr>
<tr>
<td>3.15</td>
<td>7.9650</td>
<td>4200</td>
<td>-7.32</td>
</tr>
</tbody>
</table>

As expected and seen in Table 3.4 and 3.5, resonant frequency increases when dimension of the resonator decreases. Variation of resonant frequency with respect to dimensions are shown graphically in Figure 3.7 and Figure 3.8

![Figure 3.7 Resonant frequency with respect to diameter](image)

Figure 3.7 Resonant frequency with respect to diameter
As shown in Table 3.2 and Table 3.3, there is no specific relationship between dimension and quality factor. Quality factor and insertion loss mainly depend on length between resonator and microstrip line; these are examined in next section.

3.3. Coupling of the resonator

In this part of the thesis, coupling mechanism between microstrip line and DR with TE$_{01\delta}$ mode will be explained. Magnetic field intensity of the TE$_{01\delta}$ mode is perpendicular to the microstrip plane so that the magnetic lines of the resonator link with those of the microstrip line as shown in Figure 3.9 [15]. In other words, magnetic field lines of microstrip line is compatible with magnetic field lines of TE$_{01\delta}$ mode. Thus, coupling ratio is related to magnetic field interaction between DR and microstrip. If distance between microstrip line and DR decreases, magnetic field interaction increases so coupling ratio increases. Magnetic field interaction in simulation environment is shown in Figure 3.10. In Figure 3.10 microstrip line is excited at resonant frequency, at that frequency DR has interaction to microstrip line.
In Figure 3.11 lumped element model of DR is shown. According to this model, interaction is shown as a transformer with coupling ratio ‘n’.

In this model; quality factors and resonant frequency can be calculated as
Linear microwave solvers such as AWR and ADS use lumped element DR model for designing resonator; however this model is less accurate since module cavity environment is not modelled in these solvers. In this work; to analyze DR, EM solver is used, and oscillator is designed by using extracted numerical results in harmonic balance solver.

\[
Q_u = R \sqrt{\frac{C}{L}} \quad Q_e = \frac{R}{n^2} \sqrt{\frac{C}{L}} \quad Q_L = \frac{1}{1+n^2} \sqrt{\frac{C}{L}}
\]

\[
f_0 = \frac{1}{\sqrt{LC}}
\]

In EM solver, effects of distance between DR and microstrip is studied as show in Table 3.6 Resonant frequency, quality factor and insertion loss with respect to distance between DR and microstrip are observed as in Figure 3.12. As expected, by decreasing of this distance, quality factor is decreased.
Insertion loss is also affected by coupling, and it can be written as

\[ I. L = -20\log\left(1 - \frac{Q_L}{Q_u}\right) \]  

(3.19)

Theoretical insertion loss is a little different than solver result since metal enclosure and microstrip line also have loss, and radiation loss is also present.

Table 3.6 Resonant frequency, quality factor and insertion loss with respect to distance between DR and microstrip line

<table>
<thead>
<tr>
<th>Distance between DR and m.strip</th>
<th>Resonant Frequency(GHz)</th>
<th>Loaded Q</th>
<th>Insertion loss(dB) at resonance</th>
<th>Theoretical insertion loss dB</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.35</td>
<td>8.0395</td>
<td>2970</td>
<td>-4.73</td>
<td>-3.1</td>
</tr>
<tr>
<td>3.85</td>
<td>8.0395</td>
<td>3300</td>
<td>-5.77</td>
<td>-3.5</td>
</tr>
<tr>
<td>4.35</td>
<td>8.0385</td>
<td>4400</td>
<td>-6.85</td>
<td>-5</td>
</tr>
<tr>
<td>4.85</td>
<td>8.038</td>
<td>5000</td>
<td>-9.27</td>
<td>-6</td>
</tr>
<tr>
<td>5.35</td>
<td>8.0375</td>
<td>5050</td>
<td>-12.2</td>
<td>-6.1</td>
</tr>
</tbody>
</table>

Figure 3.12 Quality Factor versus distance between DR and feedline
3.4. Resonator Frequency Tuning

Resonant frequency of DR might not be exactly the same as simulation solution since any variation on radius, height and dielectric constant of DR can cause change in resonant frequency as mentioned in section 3.2. As a result of those, tolerances of the resonator should be as low as possible. In addition to that temperature variation has also effect on resonant frequency. Thus; to ensure desired resonant frequency, tuning screw should be used.

The operation of the tuning mechanism can be explained by the perturbation principle. For any small change in cavity volume or any small change in tuning screw, electric and magnetic energies in cavity also change; and assuming $\Delta V$ is small in Figure 3.13, resonant frequency changes according to (3.20) and (3.21) [16]

\[ \frac{\omega - \omega_0}{\omega} \approx \frac{\int_{V_0} (\mu |H_0|^2 - \varepsilon |E_0|^2) \, dv}{\int_{V_0} (\mu |H_0|^2 + \varepsilon |E_0|^2) \, dv} \] (3.20)

\[ \frac{\omega - \omega_0}{\omega} \approx \frac{\Delta W_m - \Delta W_e}{W_m + W_e} \] (3.21)

where $\Delta W_m$ and $\Delta W_e$ are the changes in the stored magnetic energy and electric energy, respectively, after the shape perturbation, and $W_m + W_e$ is the total stored energy in the cavity. These results show that the resonant frequency may either
increase or decrease depending on where the perturbation is located and whether it increases or decreases the cavity volume. [16]

In section 3.4.1 and 3.4.2, change in resonant frequency by using metal and dielectric tuning screw is examined.

3.4.1 Metal Tuning Screw

In this section, resonant frequency of DR with respect to location of metallic screw will be explained.

By bringing the metal screw close to the dielectric resonator as shown in Figure 3.14, the resonant frequency of the TE$_{01\delta}$ mode is modified from the value given by (3.21). Above DR, magnetic fields are dominant due to mode of DR so change in magnetic energy causes increase in resonant frequency. In Figure 3.15, scattering parameters of DR are shown and in Figure 3.16 change in resonant frequency can be observed graphically.

Figure 3.14 Tuning Screw and DR location
3.4.2 Dielectric Tuning Screw

Dielectric screw can also be used as tuning element. By bringing the dielectric screw close to the dielectric resonator, the resonant frequency of the TE_{01δ} mode is modified. In contrast to metallic screw, change in magnetic energy causes decrease in resonant frequency. In Figure 3.17 change in resonant frequency can be observed graphically.

Figure 3.15 S parameters with respect to change in tuning screw

Figure 3.16 Location of tuning screw vs. resonant frequency
According to simulation results, metallic screw has more effect on tuning resonator. For metallic screw 78MHz tuning is observed; whereas, for dielectric screw 8MHz tuning is achieved; moreover other hybrid modes is observed. In this work, metallic tuning screw is used since it is more effective on tuning and easy to handle.

![Figure 3.17 Location of tuning screw vs. resonant frequency](image)

Figure 3.17 Location of tuning screw vs. resonant frequency
4.1 Oscillator Theory

Oscillator is a nonlinear device which converts DC power to RF signal. In contrast to amplifiers, oscillators are based on instability of circuits. The basic operation of oscillators can be examined as linear feedback network. In Figure 4.1, mathematical model of an oscillator is given.

In Figure 4.1, $V_i(\omega)$ is input of the circuit, $A(\omega)$ is gain, and $H(\omega)$ is transfer function of the feedback system and, $V_o(\omega)$ is output of the system. In oscillators, input corresponds to noise in the system, $H(\omega)$ corresponds to resonator of oscillator.

![Figure 4.1 Linear Feedback System](image)

By considering Figure 4.1 output of oscillator can be written as

$$A(\omega) [V_i(\omega) + H(\omega) V_o(\omega)] = V_o(\omega) \quad (4.1)$$

$$V_o(\omega) = \frac{A(\omega)}{1 - A(\omega)H(\omega)} V_i(\omega) \quad (4.2)$$

In (4.2), output of the feedback system is given.
If $A(\omega)H(\omega)$ is 1 at a particular frequency, denominator of (4.2) becomes zero, thus non-zero output power can be observed at that specific frequency. This is referred to Nyquist or Barkhausen criterion which is used to design oscillators [17].

In microwave, $A(\omega)$ and $H(\omega)$ could be modified in terms of reflection coefficients. By considering Figure 4.2, reflected and incident signals can be written as

$$b_1 = b_s\Gamma_1 + b_s\Gamma_1^2\Gamma_s + b_s\Gamma_1^3\Gamma_s^2 + \cdots \quad (4.3)$$

$$\frac{b_1}{b_s} = \frac{\Gamma_1}{1-\Gamma_1}\Gamma_s \quad (4.4)$$

Notice that equations (4.2) and (4.4) are in similar form. As a result of that; if $\Gamma_1\Gamma_s$ is 1, denominator of (4.4) is zero. Thus, "$\Gamma_1\Gamma_s = 1$" gives non-zero incident and reflected power at particular frequency that is unstability or oscillation condition for microwave networks. To design RF oscillators this condition is widely used. That method is called negative resistance method which is examined in the next section.

Above analysis are based on linear model, whereas oscillation mechanism is nonlinear. Thus linear analysis might not be sufficient to examine oscillators. In oscillators, location of poles is not steady due to nonlinearity. For start-up condition, poles of (4.4) must have a positive real part-complex conjugate pair as shown in Figure 4.3.e so that in time domain, magnitude of the oscillation grows up as shown in Figure 4.3.b. If
poles do not have positive real parts as in Figure 4.3.d, oscillation decays down as shown in Figure 4.3.a and steady state oscillation could not be observed.

Magnitude of oscillation cannot grow up to infinity, magnitude of output waveform is limited by saturation of the active device; at steady state condition, poles close to imaginary axes as shown in Figure 4.4 and stable oscillator behavior is observed as in Figure 4.3.c and 4.3.f.

Thus; to guarantee oscillations, roots of $1 - A(\omega)H(\omega)$ must be a complex conjugated pair with positive real parts, thus oscillation condition states that
Equations (4.5) and (4.6) are called the start-up conditions for an oscillator.

In conclusion; oscillator design is based on unstability of the circuit. As long as denominator of the output satisfy oscillation conditions at a specific frequency, non-zero output can grow-up due to noise in circuit. To obtain steady state oscillation, initial complex conjugate poles must be on the right half plane.

4.2 Negative Resistor Oscillator Design

In section 4.1 how oscillation can be occurred is explained. To design an oscillator, linear feedback approach can be a starting point; however in some cases, only linear feedback approach may not be sufficient due to nonlinear nature of the active device. To guarantee building up of an oscillation, start up conditions must also be satisfied as stated in (4.5) and (4.6).

In this section, negative resistance method will be explained; this method is convenient to use to design oscillators in microwave frequencies. RF oscillators mainly consist of a resonator, an active device, and a matching network which is shown in Figure 4.5.

![Figure 4.5 Main Oscillator Topology](image)
In Figure 4.5, the resonator is a frequency selective network which determines oscillation frequency; unstable active network is required to obtain negative resistance. Finally, a matching network is required to satisfy oscillation conditions and to maximize oscillation output power.

In section 4.1 expression (4.4) states that to observe nonzero reflected and incident power, denominator of network equation should be zero at oscillation frequency, thus at steady state \( \Gamma_r \Gamma_{\text{in}} \) should be 1. Since reflection coefficient of a resonator always lower than 1 (\( |\Gamma_r| \leq 1 \)) due to passive behavior, \( |\Gamma_{\text{in}}| \) must be higher than 1. If input reflection coefficient is higher than 1, \( R_{\text{in}} \) must be negative, that is called negative resistor method.

In below expressions, it is shown that why \( R_{\text{in}} \) is negative valued.

Consider reflection between resonator and active device.

\[
z_{\text{in}} = R_{\text{in}} + jX_{\text{in}}
\]  
(4.7)

where \( R_{\text{in}} \) is resistance of \( z_{\text{in}} \) and \( X_{\text{in}} \) is reactance of \( z_{\text{in}} \)

To provide oscillation, \( |\Gamma_{\text{in}}| \) is

\[
|\Gamma_{\text{in}}| = \left| \frac{z_{\text{in}} - z_0}{z_{\text{in}} + z_0} \right| \geq 1
\]  
(4.8)

where \( z_0 \) is characteristic impedance and it is positive and real for lossless transmission line.

Expression (4.8) reduces to
\[ |R_{in} + jX_{in} - z_0| \geq |R_{in} + jX_{in} + z_0| \] \hspace{1cm} (4.9)
\[ R_{in}^2 - 2R_{in}z_0 + z_0^2 + x_{in}^2 \geq R_{in}^2 + 2R_{in}z_0 + z_0^2 + x_{in}^2 \] \hspace{1cm} (4.10)

Expression (4.10) reduces to

\[ 0 \geq R_{in}z_0 \] \hspace{1cm} (4.11)

Since \( z_0 \) is positive. \( R_{in} \) must be negative to satisfy (4.11)

\[ R_{in} \leq 0 \] \hspace{1cm} (4.12)

Now consider oscillation condition at steady state and examine impedances.

\[ \Gamma_r \Gamma_{in} = 1 \] \hspace{1cm} (4.13)
\[ \frac{z_r - z_0}{z_r + z_0} \frac{z_{in} - z_0}{z_{in} + z_0} = 1 \] \hspace{1cm} (4.14)

where \( z_r \) is impedance of the resonator

\[ z_r = R_r + jX_r \] \hspace{1cm} (4.15)

Expression (4.15) reduces to

\[ z_r z_{in} - z_{in} z_0 - z_0 z_r + z_0^2 = z_r z_{in} + z_{in} z_0 + z_0 z_r + z_0^2 \] \hspace{1cm} (4.16)
\[ z_r + z_{in} = 0 \] \hspace{1cm} (4.17)

Expression (4.17) states that

\[ R_{in} + R_r = 0 \] \hspace{1cm} (4.18)
\[ X_{in} + X_r = 0 \] \hspace{1cm} (4.19)
Equations (4.18) and (4.19) are impedance conditions to provide steady state oscillation.

Note that if $\Gamma_r \Gamma_{in}$ is 1; $\Gamma_{out} \Gamma_s$ is also 1 as shown below.

$$\Gamma_r = \frac{1}{\Gamma_{in}} = \frac{1 - s_{22} \Gamma_s}{s_{11} - \Delta \Gamma_s}$$  \hspace{1cm} (4.20)$$

$$\Gamma_{out} = \frac{1 - \Delta \Gamma_r}{s_{22} - \Delta \Gamma_r} = s_{22} + \frac{s_{12} s_{12} \Gamma_r}{1 - s_{11} \Gamma_r}$$  \hspace{1cm} (4.21)$$

where $\Delta = s_{11} s_{22} - s_{21} s_{12}$

From (4.20) and (4.21) it can be shown that

$$\Gamma_r \Gamma_{in} = \Gamma_{out} \Gamma_s$$  \hspace{1cm} (4.22)$$

Thus, oscillation condition $\Gamma_r \Gamma_{in} = 1$ is also valid for output terminating port so both input and output terminating ports are oscillating.

For start-up condition as mentioned in part 4.1 poles must have a complex conjugated pair with positive real part, as a result of that $\Gamma_r \Gamma_{in}$ must be higher than 1

$$\Gamma_r \Gamma_{in} > 1$$  \hspace{1cm} (4.23)$$

By using similar calculation as in expressions (4.13) to (4.17). Expression (4.23) reduces to

$$z_{in} + z_r < 0$$  \hspace{1cm} (4.24)$$

As a result of (4.24), at start up condition impedances must satisfy

$$R_{in} + R_r < 0$$  \hspace{1cm} (4.25)$$
\[ X_{in} + X_r = 0 \]  \hspace{1cm} (4.26)

\[ |R_{in}| > R_r \]  \hspace{1cm} (4.27)

Note that \( R_{in} \) is not constant due to non-linearity. By assuming \( |R_{in}| \) decreases linearly up to building of oscillation, to maximize output oscillator power \( R_{in} \) should be, \([18]\)

\[ \left| \frac{R_{in}}{3} \right| = R_r \]  \hspace{1cm} (4.28)

To summarize, for microwave oscillators impedances must satisfy

\[ X_{in}(\omega_0) = -X_r(\omega_0) \quad \text{or} \quad X_{out}(\omega_0) = -X_s(\omega_0) \]

and

\[ |R_{in}(\omega_0)| > R_f(\omega_0), \quad \left| \frac{R_{in}(\omega_0)}{3} \right| \approx R_f(\omega_0) \]  \hspace{1cm} (4.29)

\[ |R_{out}(\omega_0)| > R_s(\omega_0), \quad \left| \frac{R_{out}(\omega_0)}{3} \right| \approx R_s(\omega_0) \]  \hspace{1cm} (4.30)

where \( \omega_0 \) is resonant frequency.

A design procedure for two port oscillators could be summarized as follows.

1. Design a resonator which resonates at the oscillation frequency. Note that type of resonator, quality factor and coupling ratio are important for cost, output power, and phase noise.
2. Design an unstable active network at oscillation frequency. Using series or parallel feedback could be useful to satisfy unstability. Make sure \( R_{in} \) is negative.
3. By using (4.29) and (4.30) design an oscillating matching network.
4.2.1 Active Device with Feedback

In section 4.2 general consideration about microwave oscillator design is explained. In this section, active device for oscillators is discussed.

To provide negative resistance, an active device is required. Generally in microwave; PIN diodes, RF transistors, and amplifiers are used to achieve oscillation. Selection of active device is important. Firstly, the active device must operate at the oscillation frequency that means scattering parameters should be suitable for unstability. Secondly, for phase noise consideration, noise figure and flicker noise of the active device should be as low as possible. Thirdly, P1dB and large signal parameters of oscillator are required for non-linear simulation.

To observe unstability of the active device; Rollet stability factor, stability circles, and scattering parameters of the active device with feedback should be used. If Rollet stability factor (K) is lower than 1, active device is potentially unstable; whereas, if K is higher than 1 device is unconditionally stable; for amplifier application, Rollet stability factor must be higher than 1 and (|Δ| < 1). Rollet stability factor can be expressed as

\[
K = \frac{1-|s_{11}^2|-|s_{22}^2|+|Δ^2|}{2|s_{21}s_{12}|}
\]  

(4.31)

Series or parallel feedback could be used to obtain unstability. Usually for series feedback, a transmission line or an inductor is connected to base or source of a transistor as shown in Figure 4.6. Similarly for parallel feedback; a transmission line or a resonator network could be connected between gate and drain as shown in Figure 4.7. By tuning length of transmission line or inductance, negative resistance and unstability could be achieved.
Another point is stability circles; by using stability factor, these circles are plotted on Smith chart. Stability circle gives which load value is unstable or stable, if unstable load value is selected, active device will oscillate otherwise it will not. In Figure 4.8 output stability circles is shown, shaded areas show stable load values. By selecting unstable area on Smith chart, desired load for oscillation can be determined.
Scattering parameters $S_{11}$ and $S_{22}$ could also be used for stability analysis. For example, consider input or output reflection coefficient for oscillator condition as shown in expression (4.32). If $|S_{11}|$ or $|S_{22}|$ is greater than 1, $|\Gamma_{\text{in}}|$ or $|\Gamma_{\text{out}}|$ can also be greater than 1 so active device gives negative resistance.

\[
|\Gamma_{\text{in}}| = |s_{11} + \frac{s_{21}s_{12}\Gamma_s}{1-s_{22}\Gamma_s}| > 1 \quad \text{and} \quad R_{\text{in}} < 0 \quad (4.32)
\]

Thus, feedback network could be designed so that $|S_{11}|$ is greater than 1; also to provide sufficient gain for starting conditions; $s_{21}$ should be higher than 1 at resonant frequency.

For phase noise consideration; type of transistor, noise figure and flicker noise of active device are critical. Unfortunately, many transistor suppliers do not provide flicker noise data, however type of transistor and noise figure might give information about noise.

In RF systems, output power of an oscillator could be critical to drive mixer or amplifier. Saturation power of an active device must be large enough for sufficient output power. Furthermore, large signal parameters are useful to simulate output...
power. Harmonic balance simulators can simulate output power and harmonics. If large signal parameters are not available, these parameters can be measured and modeled. For example; by using load-pull variations and power sweep measurement, these parameters can be extracted. For Agilent devices, large signal parameters can be measured as X-parameter which is a kind of large signal parameter that is suitable for non-linear simulation. In addition to that if large signal simulation is available, linear approximation in expression (4.28) is not necessarily used, and output power could be simulated in terms of load variation, and optimum load which gives maximum power can be found.

In conclusion, feedback network design is a key point to obtain negative resistance. Moreover, selection of active device plays an important role on phase noise and output power.

### 4.2.2 Resonator

As mentioned in section 3, resonator is one of the most critical part for oscillator design. Properties and type of resonators have strong effects on phase noise and operation frequency. For example; for Harley and Colpits oscillators, lumped element LC network can be used as a resonator. Crystal oscillators are used to generate clock or reference signal, and piezoelectric crystal resonator is used. These oscillators are usually used in HF and VHF. Above 3GHz, usually planar transmission line resonators, hairpin resonators, dielectric resonators, cavity resonators, tube resonators, YIG resonators and optical resonators etc. are preferred. Thus according to application and requirement, appropriate resonator should be chosen. In addition to that by using IC technology, high Q factor capacitor resonator could be constructed in microwave frequencies, these resonators are used in packed VCOs which are available in market.

As mentioned in section 3, in this work, firstly analytical analysis methods are used to determine approximate dimensions of dielectric resonator than numerical EM solver is used for fine tuning. After the resonator is designed, results are extracted to harmonic
balance simulator than negative resistance behavior is observed by changing feedback parameters. When enough negative resistance is observed, matching network can be designed to satisfy oscillation conditions. In the next section, oscillation matching network design is considered.

### 4.2.3 Oscillation Matching

In part 4.2.1 and 4.2.2 general design approach for active devices and resonators are given by considering simulation tools; after unstable amplifier and resonator are designed, suitable impedances must be loaded to output of the active device so that oscillation conditions are achieved. Matching network is final synthesis point for oscillator design, and it is the most critical part for a success design. Consider Figure 4.9; for unstable operation, $R_{out}$ is negative at resonant frequency. If it is necessary, value of $R_{out}$ could be changed from positive to negative by tuning length of transmission lines ($\theta_1$, $\theta_2$ and $\theta_3$) so that desired $R_{out}$ can be achieved.

![Figure 4.9 Resonator active device and matching network (bias is not shown)](image)

To achieve oscillation condition impedances must be $|R_{out}(\omega_0)| > R_s(\omega_0)$ and $X_{out}(\omega_0) = -X_s(\omega_0)$. After $R_{out}$ and $X_{out}$ are calculated or simulated, suitable impedance matching is designed according to (4.29) and (4.30). Infinitely many
solution can be found to construct oscillating matching network; however for simple design, single stub matching network is sufficient to resolve this problem. In Figure 4.10 matching network is shown.

![Figure 4.10 Single Stub Matching Network](image)

For single matching load, $Z_s$ can be calculated as

$$Z_s = R_s + jX_s = Z_{o2} \frac{(Z_o / \tan(\theta_{o1})) + jZ_{o2}\tan(\theta_{o2})}{Z_{o2} + j(Z_o / \tan(\theta_{o1})) + \tan(\theta_{o2})}$$  \hspace{1cm} (4.33)$$

and (4.33) reduces to

$$Z_s = R_s + jX_s = Z_{o2} \frac{(Z_o Z_{o1} - Z_o Z_{o2} \tan(\theta_{o1}) \tan(\theta_{o2})) + j[Z_o Z_{o2} \tan(\theta_{o2})]}{[Z_o Z_{o2} + j[Z_o (Z_{o1} \tan(\theta_{o1}) + Z_{o2} \tan(\theta_{o1})]}}$$  \hspace{1cm} (4.34)$$

$Z_{o1}, Z_{o2}, \theta_{o1},$ and $\theta_{o2}$ must be designed according to oscillation conditions which are given in (4.29) and (4.30). In addition to that to adjust harmonics and maximize output power, $R_s$ might be tuned as long as expression (4.29) is valid.

In next section, DRO design and simulation considerations are given for both parallel and series feedbacks.
4.3 DRO Design and Simulations

4.3.1 Series Feedback DRO

Practical DRO design is explained by using a microwave simulator which is AWR design environment for this part. In this thesis, a series feedback DRO is designed manufactured and measured; simulation results which are given in this section are based on produced DRO.

As a first step, transistor with series feedback is constructed as shown in, and all practical elements are taken into consideration for good realization, for example bondings and jumper pads are included in simulation. For biasing, self-bias topology is used since it is less sensitive to resistance variations. In this work, length of series feedback which is shown in Figure 4.11 is approximately 90 degree at resonant frequency. By tuning length of series feedback lines, stability factor and scattering parameters are settled as shown in Figure 4.13. As a starting design point; $S_{11}$ and $S_{22}$ set at value greater than 1 at resonance frequency because oscillation is based on amplification of reflected and incident signal. To decouple DC from output, a thin film capacitor is used.

Figure 4.11 Series Feedback Transistor Scheme
After unstable amplifier is designed, EM solution of dielectric resonator is imported from CST to AWR as one port s-parameter box; then this extracted one port resonator is connected to gate of transistor as shown in Figure 4.14. Then real and imaginary part of output impedance $z_{out}$ is plotted as shown in Figure 4.15, and real part of $z_{out}$ must be negative for oscillation.
According to (4.29) and (4.30), an oscillation matching network is designed as shown in Figure 4.16. In this figure for oscillation matching network, a single stub network is used, in addition to that a 15dB coupler is designed for sampling of output signal so that phase detector of PLL could compare output and reference signal.
To investigate oscillation condition $R_{out}(\omega_0) + R_s(\omega_0)$ and $X_{out}(\omega_0) + X_s(\omega_0)$ are plotted in Figure 4.17. As a result of that $R_{out}(\omega_0) + R_s(\omega_0) < 0$ and $X_{out}(\omega_0) + X_s(\omega_0) = 0$
If large signal parameters of active device are available, output power and harmonics can be simulated by harmonic balance simulator. In Figure 4.18 simulation result is shown. Results are quite close to measured results, output power was measured as 13.6 dBm. Measurement results will be given in more detail in part 6.

![Figure 4.18 Output Power Simulation (dBm)](image)

**4.3.2 Parallel Feedback DRO**

In this part, parallel feedback DRO design is explained by AWR design environment. Both series feedback and parallel feedback design algorithm are the same. In contrast to series feedback DRO, this oscillator is not produced and measured; so for simplicity, bondings and jumpers are not modelled. Moreover, ideal LC are used for oscillation matching.

In Figure 4.19, schematic of parallel feedback DRO is shown. For this topology of resonator, resonator network acts as a very narrow band stop filter; in other words, at resonant frequency power propagate through resonator with minimum loss.
For unstability, by changing length of transmission lines, $R_{out}$ is adjusted as negative, as shown in Figure 4.20.

Figure 4.20 Output Impedance

In Figure 4.20, output impedances are measured as $X_{out}(\omega_0) = -35$ $\Omega$ and $R_{out}(\omega_0) = -110$ $\Omega$; so matching network could be designed as $X_s(\omega_0) = -35$ $\Omega$ and $R_{out}(\omega_0) < -110$ $\Omega$
In Figure 4.21, ideal matching network is given, inductance of the inductor can be calculated as

$$j \omega_0 L = jX_s(\omega_0) = j35 \, \Omega$$  \hspace{1cm} (4.35)

$$L \approx 0.7 \, \text{nH}$$  \hspace{1cm} (4.36)

where $\omega_0$ is oscillation frequency 8GHz.

Furthermore, as shown in Figure 4.22 output power can be plotted as a function of the load impedance $R_s$. For this simulation, maximum power transfer is obtained at $R_s = 60 \, \Omega = 0.545 |R_{out}(\omega_0)|$ this shows that assumption in (4.28) is not necessarily used if nonlinear simulation is available.
All in all, for DRO design, appropriate dielectric resonator should be designed by using EM solver; then by using unstable amplifier, output impedances should be measured so that oscillating matching network is designed with respect to (4.29) and (4.30). Moreover, nonlinear simulator has advantage to visualize load variations. In next section, voltage controlled dielectric resonator oscillator design is discussed.

4.4 Varactor Tuned DRO

Frequency of free running oscillators shift with respect to temperature, aging, and time. For this reason; depending on application, frequency of oscillation is controlled by phase locked loops. To provide frequency control, oscillators are integrated with frequency controlled units.

In this work, to control frequency, a varactor diode is used. Varactor diode is a unilateral device, and in accordance with the applied voltage its capacitance decreases. For typical LC resonator, varactor diode is directly connected on LC resonator, whereas for this work a thin film varactor diode is connected to the transmission line as shown in Figure 4.23, its tuning voltage is applied on inductor choke. When capacitance of varactor is changed, effective capacitance of dielectric resonator is slightly changed then resonant frequency is shifted with respect to applied voltage. Furthermore, as shown in Figure 4.23 length of transmission lines ($\theta_1$ and $\theta_2$) which are connected to varactor are critical since effect of varactor diode vary with respect to length of $\theta_1$ and $\theta_2$. In practice $\theta_1$ and $\theta_2$ are generally selected as 90 and 180 degree; respectively [19]. In this work, effects of $\theta_1$ and $\theta_2$ are simulated as shown in Figure 4.24 to Figure 4.27 length of these lines affects the range of tuning frequency. As an example, for $\theta_1$ and $\theta_2$ are 90 degree, tuning range of resonant frequency is very limited and its behavior is nonlinear as shown in Figure 4.25 since when $\theta_2$ is 90 degree, short circuit is presented at resonator coupling point. For $\theta_1=90$ and $\theta_2=180$ degree, 8.4MHz tuning is obtained and its characteristic is almost linear as shown in Figure 4.24. For PLL applications, linearity of resonant frequency with respect to varactor voltage might be critical.
Length between dielectric resonator and transmission line which is connected to varactor is also important for tuning. When coupling between the transmission line and resonator is increased, tuning range also increases. However, when this occurs loaded quality factor decreases so phase noise becomes worse.
Figure 4.25 Freq. vs Tuning Capacitance for θ1=90 θ2=90

Figure 4.26 Freq. vs Tuning Capacitance for θ1=180 θ2=90

Figure 4.27 Freq. vs Tuning Capacitance for θ1=135 θ2=135
In Table 4.1, a comparison is given with respect to the lengths of transmission lines.

Table 4.1 Tuning Range with respect to length of TLs

<table>
<thead>
<tr>
<th>$\Theta_1$ (degree)</th>
<th>$\Theta_2$ (degree)</th>
<th>Tuning Range (MHz)</th>
<th>Frequency Behavior w.r.t voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>90</td>
<td>180</td>
<td>8.4</td>
<td>Linear</td>
</tr>
<tr>
<td>90</td>
<td>90</td>
<td>0.3</td>
<td>Non-linear</td>
</tr>
<tr>
<td>180</td>
<td>90</td>
<td>2.9</td>
<td>Linear</td>
</tr>
<tr>
<td>135</td>
<td>135</td>
<td>7.6</td>
<td>Linear</td>
</tr>
</tbody>
</table>

In conclusion, effects on voltage control tuning range is given and voltage controlled DRO is designed, so designed DRO could be used as VCO in phase locked loop. In the next section, design considerations of PLL and PLDRO are given.
CHAPTER 5

PHASE LOCKED LOOP DESIGN

5.1 PLL Blocks

Phase locked loop (PLL) is a feedback system which controls and synchronizes output phase with respect to input phase. In other words, by using PLL, phase of output is locked to phase of input. When phase and frequency control is critical, PLL is widely used in applications such as frequency synthesizer, transmitters, receivers, modulators, demodulators, oscillators, symbol synchronization, carrier and clock recovery. Basic building blocks of PLL which are shown in Figure 5.1 composed phase detector, frequency divider or multiplier, loop filter, and voltage controlled oscillator.

![Figure 5.1 Basic PLL Blocks](image)

In Figure 5.1, loop filter $H(s)$ is a low pass filter. Assuming that the output frequency of the VCO depends linearly on the tuning voltage of the VCO, the transfer function of the VCO can be written as $\frac{K_{vco}}{s}$.

Relation between phase and frequency of the VCO can be written as
\[ V \text{tune}(t)K \text{vco} + 2\pi fi = 2\pi f_o = \frac{d}{dt} \theta_o(t) \]  
\[(5.1)\]

where \(fi\) is frequency of the VCO when \(V \text{tune}\) is zero, \(f_o\) and \(\theta_o\) are output frequency and phase of the VCO, respectively.

Actually, PLL is a nonlinear system but it can be characterized as linear system; by assuming that phase error \(\theta_e(s)\) is sufficiently small, and frequency changing of the VCO with respect to tuning voltage is linear.

In Laplace domain, transfer function of the PLL which is given in Figure 5.1 can be written as

\[ \theta_e(s) = \theta_i(s) \frac{K_d}{1 + \frac{K_d K \text{vco} H(s)}{N}} \]  
\[(5.2)\]

where \(K_d\) is gain of phase detector, \(N\) is frequency scaling factor of the frequency divider.

Basically, for proper operation phase error must be zero at steady state. By using final value theorem, steady state behavior of phase error can be observed as

\[ \lim_{t \to \infty} \theta_e(t) = \lim_{s \to 0} s \theta_e(s) \]  
\[(5.3)\]

In addition to that loop design must be carefully designed since if denominator of (5.2) is zero, or phase margin is small; PLL tends to oscillate or does not work properly. Thus, to satisfy stable operation, phase margin and loop filter bandwidth should be designed so that phase margin should be between 45\(^\circ\) and 60\(^\circ\), and filter bandwidth should be smaller than 1/10 of the phase detector frequency channel spacing [20].
In next sections, all PLL building blocks which are used in this study are explained. For phase locked dielectric resonator oscillator (PLDRO); a step recovery diode and schottky diodes are used as phase detector and frequency multiplier. An active low pass filter is used as loop filter; and voltage controlled DRO is used as VCO. In addition to that for acquisition behavior a triangular wave generator is used.

5.1.1 Sampling Phase Detector

A phase detector compares two sinusoidal signal at its input and generates an error signal. If there is a phase difference between them, this error signal can be used to drive the VCO after low pass filtering.

In digital based PLLs; XOR gates, flip flops and digital phase comparators are used, whereas for analog phase detectors mixers are widely used. In microwave applications, both analog and digital phase detectors are used; however to use digital phase detector, frequency of microwave signal must be divided before digital phase detection.

In this thesis; analog phase detector is used as sampling phase detector which consists of a step recovery diode (SRD) and schottky diode pair as shown in Figure 5.2.

SRD whose characteristic is given in Figure 5.3 can generate sharp narrow pulses at reference frequency. Thus in frequency domain, impulses or combs can be obtained up to 20 GHz which determines working range of the detector. To conclude, SRD can multiply referans signal up to 20 GHz [21] [22].
As shown in Figure 5.2 capacitors between SRD and schottky diode act as a switch which turns on and off by the pulse generated by the SRD. The series pair of schottky diode are used to detect phase error between frequency of VCO and combs of input reference.

The overall circuitry of phase detector is shown in Figure 5.4. Balun transformer is used for impedance matching and is also used for isolation between referans signal and SRD. Capacitors and resistor between transformer and SRD are used for termination and tune circuit for microwave frequency. Furthermore, 50ohm resistor between microwave input and schottky diode is used for microwave termination. Phase error signals are buffered and balanced with variable resistor as shown in Figure 5.4 [21].
In this work, digital phase detector is not used since it requires frequency divider whose noise floor limits phase noise and it is not more economical than sampling phase detector [21].

5.1.2 Loop Filter

In this thesis, a second order active low pass filter is used as loop filter shown in Figure 5.5. Sweep acquisition circuitry is integrated with loop filter; but for low phase errors, its loading effect could be ignored.

Gain and bandwidth of loop filter is critical parameter for loop filter design since if gain and bandwidth of filter increases PLL could lock more quickly, however due to damping factor of the system, PLL might become unstable.

Other point is that the signal at the input of the loop filter is not pure, it may also contain referans signal, its harmonics and intermodulation of all IF signals and, harmonics due to nonlinearity of SRD. To avoid undesired effects, all unwanted signals must be attenuated by low pass filter. Thus bandwidth of loop filter should be
as low as possible; also for noise immunity, bandwidth of the filter should be considered.

Transfer function of the designed loop filter can be written as

\[ H(s) = \frac{1 + s C_1 R_2}{s C_1 R_1} \frac{1}{1 + s C_2 R_3} \]  

(5.4)

Transfer function of filter is shown in Figure 5.6 and Figure 5.7. For this design, bandwidth of filter is not sufficient to lock error frequency which is higher than about 1 kHz because when error frequency is higher than 1 kHz, it is attenuated by loop filter and error becomes out of lock-in range. However; acquisition sweep circuit which is explained in the next section helps to reduce frequency error so that it is in lock in range.
Figure 5.6 Gain of Loop Filter

Figure 5.7 Loop Filter Transfer Function Angle
5.1.3 Acquisition Circuit

Frequency of the VCO and reference oscillator might be very different at startup of the system, or frequency of phase error could be far away from bandwidth of loop filter, so phase error is suppressed by loop filter, for this case PLL is out of lock-in range. The process of attaining lock is called as acquisition.

When phase error is high, tuning voltage of the VCO is swept by acquisition circuitry. During sweeping, frequency of VCO is changed; when frequency of phase error is in bandwidth of loop filter, phase error is amplified, and loop filter become more dominant then acquisition circuit.

For digital PLLs, digital discriminator and charge pumps are widely used for acquisition. For this design, triangular sweep circuit is used. Square wave or exponential wave for sweeping is not recommended [23] since this type of sweep rate is much too fast to lock. In addition to that sinusoidal sweep which is achieved by Wien bridge oscillator is also not recommended due to its temperature sensitivity [23].

For this design a comparator and an integrator are used to create triangular sweep. Comparator circuit creates square wave, then square wave is transformed to triangular wave by integrator. Schematic of acquisition circuitry is shown in Figure 5.8.

In Figure 5.8, Op-Amp U1, R1, R2 and capacitor are components of loop filter, in addition to that these components are also used for acquisition circuitry as an integrator. Moreover, Op-Amp U2 is used as comparator; resistors R3 and R4 are positive feedback of acquisition, and R5 resistor is used to create constant current source. Design and analysis methodology of the acquisition circuitry will be given below.
To analyze and design acquisition circuitry, assume that phase error is high. In this case amplitude of phase error signal can be ignored since when phase error increases, beat voltage of sampling phase detector decreases.

Firstly, consider comparator operation. Assume that $V_{2+} > V_{2-}$, $V_{02} = V_{cc}$; In this case, $I_{sv}$ can be written as

$$I_{sv} = \frac{V_{o2} - V_{1-}}{R_5} = \frac{V_{cc}}{2R_5}$$  \hspace{1cm} (5.5)

Note that this current is constant and positive. Whereas for $V_{2+} < V_{2-}$ the current will be constant and negative.

Voltage and current relation of capacitance can be written as

$$I_{sv} = C \frac{dV_c}{dt} = \frac{V_{cc}}{2R_5}$$  \hspace{1cm} (5.6)
Output of op-amp U1 can be written as follow

\[ V_{01} = V_{1-} - I_{sv} R_2 - V_c \]  \hspace{1cm} (5.7)

By substituting (5.5) and (5.6) in to (5.7). Expression (5.7) can be reduced as

\[ V_{01} = \frac{V_{cc}}{2} - \frac{V_{cc}}{2R_5} R_2 - V_c \]  \hspace{1cm} (5.8)

By differentiating (5.8), equation (5.9) can be obtained.

\[ \frac{dV_{01}}{dt} = -\frac{dV_c}{dt} = -\frac{V_{cc}}{2R_5 C} \]  \hspace{1cm} (5.9)

Then, \( V_{01}(t) \) can be written by integrating (5.9)

\[ V_{01}(t) - V_{01}(0) = \int_0^t \frac{dV_c}{dt} \, dt = -\frac{V_{cc}}{2R_5 C} \, t \]  \hspace{1cm} (5.10)

(5.9) shows that output of op-amp U1 is linearly decreased when \( V_{02} = V_{cc} \). On the other hand, \( V_{2+} \) voltage also diminishes with \( V_{01} \). When \( V_{2+} < V_{2-} = V_{cc}/2 \) state of comparator is changed and \( V_{02} \) suddenly becomes \( V_{ss} \) (\( V_{ss} \) is zero in our case). Then \( V_{01} \) becomes a linearly increasing function of time. Assume that at time \( t_1 \) state of comparator is change. To determine \( t_1 \), \( V_{2+} \) can be written as

\[ V_{2+}(t) = V_{02} \frac{R_3}{R_3 + R_4} + V_{01} \frac{R_4}{R_3 + R_4} \]  \hspace{1cm} (5.11)

\[ V_{2+}(t) = V_{cc} \frac{R_3}{R_3 + R_4} + \left( V_{01}(0) - \frac{V_{cc}}{2R_5 C} \, t \right) \frac{R_4}{R_3 + R_4} \text{ for } t < t_1 \]  \hspace{1cm} (5.12)
\( V_{01}(0) \) can be regarded as \( V_{cc} \) for rail to rail op-amp operation. In addition to that \( V_{2+} \) reduces to \( \frac{V_{cc}}{2} \) at \( t_1 \), \( V_{2+} \) can be written as

\[
V_{2+}(t_1) = \frac{V_{cc}}{2} = V_{cc} \frac{R_3}{R_3 + R_4} + \left( V_{cc} - \frac{V_{cc}}{2R_5 C} t_1 \right) \frac{R_4}{R_3 + R_4}
\]  

(5.13)

Finally, decreasing duration of triangular wave can be found as

\[
\Delta t = t_1 = \frac{(R_3 + R_4) R_5 C}{R_4}
\]

(5.14)

Similarly rise time of triangular wave is equal to \( \Delta t \). Thus, frequency of triangular sweeping can be written as

\[
f_{\text{sweep}} = \frac{1}{2 \Delta t}
\]

(5.15)

Another important design consideration is the hysteresis of comparator, \( V_{02} \) should also must be considered, and resistor \( R_4 \) must be larger than resistor \( R_3 \) for consistent hysteresis of comparator [23].

For proper operation, sweep frequency should not be too high, otherwise loop filter could not catch phase error. On the other hand, if sweep frequency is too low, locking time of PLL might be too long. In this work, sweep frequency is selected around 40-50 Hz which is a reasonable value for proper operation of loop filter. Furthermore, resistor \( R_5 \) should be high as possible to isolate loop filter and acquisition, since constant current \( I_{sv} \) might affect loop filter operation even though amplitude of phase error is high.

By ignoring the loading effect of phase error, the sweep circuit is simulated by a spice simulator, triangular waveform solution can be seen in Figure 5.9
In conclusion, if bandwidth of loop filter is not sufficient for phase error, acquisition could be required. Actually, acquisition can be regarded as coarse tuning and, loop filter can be regarded as fine tuning for PLL systems. In next section overall designed PLL blocks which is integrated with DRO, is explained with simulation results.

5.2 PLL Design for Voltage Controlled DRO

In this section, designed PLDRO is explained by considering design methodology and PLL simulation results. In this work, reference signal oscillator is given externally in PLDRO module. Reference signal is amplified by op-amp to drive sampling phase detector, then phase error is proceeded by loop filter as tuning voltage of DRO. Output signal is sampled by a 15dB coupler for feedback. Block diagram of PLDRO is given in Figure 5.10.
According to block diagram phase error can be written as

$$\theta_e(s) = k_p (N\theta_i(s) - \theta_o(s))$$  \hspace{1cm} (5.16)

where $N$ multiplier is factor of phase detector and $k_p$ is half of beat voltage of sampling phase detector [23].

Loop equation can be written as in equation (5.17) and it reduces to (5.18) in terms of phase error and input phase.

$$\theta_e(s) H(s) \frac{k_{vco}}{s} = \theta_o(s) = N\theta_i(s) - \frac{\theta_e(s)}{k_p}$$  \hspace{1cm} (5.17)

$$\frac{\theta_e(s)}{\theta_i(s)} = \frac{N k_p}{1 + \frac{k_{vco} k_p H(s)}{s}}$$  \hspace{1cm} (5.18)

where $k_{vco}$ (rad/volts) is frequency change with tuning voltage of DRO.
To observe performance of PLDRO, transfer function of phase error and denominator must be examined.

By substituting designed numerical values of designed loop filter and DRO. Expression (5.18) can be rewritten as in equations (5.19) and (5.20).

\[
\frac{\theta_e(s)}{\theta_1(s)} = \frac{N k_p}{1 - \frac{k_{vco} k_p}{s} \frac{1+sC_1R_2}{sC_1R_1} \frac{1}{1+sC_2R_3}} \tag{5.19}
\]

By substituting \(N, k_p, k_{vco}, R_1, R_2, R_3, C_1\) and \(C_2\), phase error can be written as

\[
\frac{\theta_e(s)}{\theta_1(s)} = \frac{16}{1 - \frac{2 \pi 1600000}{s} \frac{1+s 1.8 \times 10^{-4}}{s 4 \times 10^{-5}} \frac{1}{1+s 4 \times 10^{-7}}} \tag{5.20}
\]

Transfer function of (5.20) can be plotted as in Figure 5.11.

![Figure 5.11 TF of phase error with respect to input phase](image-url)
Amplitude transfer function graph shows that phase error is attenuated for frequencies below 10 kHz so loop filter works properly up to 10 kHz, otherwise acquisition circuit becomes dominant than loop filter. Angle transfer function graphs shows that phase error with respect to input phase is zero for the lowest frequencies.

To observe stability of the PLL system loop gain can be written and plotted as given in (5.21) and Figure 5.12.

\[
\text{Loop Gain} = \frac{k_{vco}k_pH(s)}{s}
\]  

(5.21)

Figure 5.12 Loop Gain

Graphs in Figure 5.12 are used to determine phase margin of PLL. From graphs phase margin is observed to be about 95 degree which is quite far away from unstability, so it can be concluded that designed PLL system is stable.
In (5.2) phase error is observed with respect to reference phase, in similar way output phase could also be written with respect to input phase as in (5.22) whose transfer function is plotted as Figure 5.13.

\[
\frac{\theta_o(s)}{N\theta_i(s)} = \frac{k_p k_{vco} H(s)}{s + k_p k_{vco} H(s)}
\]  

(5.22)

Figure 5.13 Transfer Function of output phase

Graph in Figure 5.13 shows low pass characteristic with gain 1. This means that output phase is the same as input phase when frequency of phase error closes to zero.

To observe time domain or transient behavior of designed PLDRO, spice simulation is performed. In simulation tool, behavioral model of sampling phase detector and DRO are used. In addition to that to observe acquisition behavior, performance of acquisition circuitry is also included in model. Linearized time domain model of PLDRO is shown in Figure 5.14. In this design tuning voltage of DRO is between 0 volts and 10 volts.
For the first case of simulation, frequency of the reference oscillator is selected so that PLL locks at the half of tuning voltage of DRO. For this case tuning voltage of DRO must be 5V as long as DRO is lock. Figure 5.15 shows tuning voltage as a function of time. Since initial phase error is small, acquisition is not effective.
As a second case, frequency of reference oscillator is selected so that PLL locks at 8V. In this case, at starting, phase error is too high so triangular wave acquisition performed up to 15msec. When phase error becomes sufficiently small, the loop filter becomes effective.
As a third case, frequency of reference oscillator is selected so that PLL locks at 2V. Figure 5.17 shows the tuning voltage in time. At starting acquisition is effective when phase error is small enough loop filter sets tuning voltage at 2V.

![Figure 5.17 Tuning voltage of DRO for locking 2V case](image)

As the final case, frequency of reference oscillator is selected so that frequency range of DRO and input phase are very different; in other words, PLL cannot locks oscillator between 0 and 10V tuning range. In this case, tuning voltage is swept by acquisition circuit as triangular wave as shown in Figure 5.18 and, so PLL is out of lock in range, and PLDRO is not work properly.
To conclude, all simulation results show that as long as input reference signal selected properly, PLL block could achieve lock. Moreover, when frequency characteristics of DRO changes due to aging or temperature variation, PLL can lock DRO frequency as long as phase error is in lock in range.

5.3. Phase Noise Contributions

Phase noise of oscillators mainly depend on quality factor of resonator and noise characteristics of active device as in Lesson noise model. On the other hand, when a PLL is used, overall phase noise does not only depend on phase noise of DRO but also it is affected by PLL due to close loop nature. Thus, phase noise of PLDRO consists of phase noise of DRO, reference oscillator, sampling phase detector, loop filter, regulators and resistors. Each noise contribution can be calculated by referring output. Additive noise contributions of DRO, filter, SPD and reference signal are shown in Figure 5.19.

Figure 5.18 Tuning voltage of DRO for unlock case
For simplicity, it can be assumed that phase noise of each contributor is additive, and uncorrelated so output referred noise contribution of each element can be calculated as

\[
\sigma_{\text{ref-osc}} = \Phi_{\text{ref-osc}}(N \frac{k_p k_{\text{vco}} H(s)}{s + k_p k_{\text{vco}} H(s)}) \quad (5.23)
\]

\[
\sigma_{\text{SPD}} = \Phi_{\text{SPD}}(N \frac{k_p k_{\text{vco}} H(s)}{s + k_p k_{\text{vco}} H(s)}) \quad (5.24)
\]

\[
\sigma_{\text{DRO}} = \Phi_{\text{vco}} \left( \frac{s}{s + k_p k_{\text{vco}} H(s)} \right) \quad (5.25)
\]

\[
\sigma_{\text{filter}} = \Phi_{\text{filter}} \left( \frac{k_{\text{vco}} H(s)}{s + k_p k_{\text{vco}} H(s)} \right) \quad (5.26)
\]

Expression (5.23) to (5.26) show that phase noise is effected by loop filter characteristic, frequency multiplier factor N and tuning range \(k_{\text{vco}}\) of DRO. As an example, the output referred noise of reference oscillator has a low pass characteristics, whereas the output referred noise contribution of VCO, displays a high pass characteristics is observed as show in Figure 5.20. In Figure 5.20, transfer function of (5.25) is plotted as blue line, and transfer function of (5.23) (for N=1) is plotted as red line. If multiplier factor N is increased, phase noise contribution of reference signal is increased by 20log(N).
Phase noise of PLDRO can be written in terms of output referred noise contributions as in expression (5.27)

\[ \sigma_{\text{PLDRO}} = \sqrt{\sigma^2_{\text{ref osc}} + \sigma^2_{\text{SPD}} + \sigma^2_{\text{DRO}} + \sigma^2_{\text{filter}} + \sigma^2_{\text{other contributions}}} \quad (5.27) \]

Thus phase noise could be written as

\[ \text{P.N} = 20\log(\sigma_{\text{PLDRO}}) \quad (5.29) \]

To reduce phase noise of a closed loop system, loop filter bandwidth and frequency multiplier factor \( N \) must be carefully selected. In this work, loop filter bandwidth is selected by considering both PLL performance and noise contributions.

In this work, phase noise of VCO (DRO) and input oscillator are measured separately and, based on measured results, output referred noise contributions calculated by
(5.23) and (5.25) then total phase noise is calculated by expression (5.27). Results are given in Figure 5.21.

In Figure 5.22, overall theoretical phase noise and measured phase noise could be observed. Results are similar. Reasons of small differences might be due to parasitic capacitance of PCB board and regulators.
Figure 5.22 Phase Noise

Theoretical Total Phase Noise
Measured Phase Noise

Offset Frequency (Hz)

dBc/Hz
In this chapter measurement results are given. Phase noise, output power, and thermal variation tests are necessary to determine performance of oscillators. Figure 6.1, the measurement setup is shown. For reference signal, a signal generator is used. To measure phase noise and output power a spectrum analyzer is used. To characterize oscillator with thermal variations a hot-cold plate is used, and to observe varactor tuning voltage, an oscilloscope is used.

In Figure 6.2, designed PLDRO module is shown. PLDRO module has two RF ports, one of them is DRO output, and other port is input port of reference signal. In Figure 6.3;inside view of the module is shown, in PCB, there are regulators, op-amps,
transformers, and sampling phase detector. In RF part of the figure; dielectric resonator, transistor, microstrip lines, microstrip coupler, thin film packed varactor and capacitors can be seen.

Figure 6.2 Designed PLDRO Module

Figure 6.3 Inside view of the PLDRO Module
6.1 Phase Noise Measurements

Phase noise of the PLDRO was measured by spectrum analyzer which has phase noise measurement option. Screen view of spectrum analyzer is shown in Figure 6.4 and phase noise is shown in Table 6.1.

Phase noise of this design is similar to commercial modules. For example, for X-band commercial PLDROs, phase noise at 1MHz offset varies between 130dBc/Hz to 140dBc/Hz, phase noise at 100 kHz offset varies between 110dBc/Hz to 120dBc/Hz. For lower frequency offsets, phase noise mainly depends on phase noise of reference signal as mentioned in section 5.3.

On the other hand, spurious noise is observed in phase noise as seen in Figure 6.4. Reasons of these spurious might be PLL circuits, since when PLL loop is broken some of these spurs disappear. Moreover, while constructing regulator circuits small undesired oscillations were observed. Then by tuning peripheral capacitance of regulators, undesired operation was prevented so one of the reason might be due to regulator circuitry. Furthermore, around 35kHz offset a small peak is observed in phase noise measurements, reason of that could be undesired or parasitic pole or zero in PCB, another reason could be due to internal frequency response of op-amp or regulator circuitry.

In the next section, power measurement of PLDRO is given.
Figure 6.4 Phase Noise Measurement

Table 6.1 Frequency Offset vs. Phase Noise

<table>
<thead>
<tr>
<th>Frequency Offset</th>
<th>Noise level (dBc/Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 Hz</td>
<td>-71.4 dBc/Hz</td>
</tr>
<tr>
<td>100 Hz</td>
<td>-80 dBc/Hz</td>
</tr>
<tr>
<td>1 kHz</td>
<td>-91.3 dBc/Hz</td>
</tr>
<tr>
<td>10 kHz</td>
<td>-92.7 dBc/Hz</td>
</tr>
<tr>
<td>100 kHz</td>
<td>-104 dBc/Hz</td>
</tr>
<tr>
<td>1 MHz</td>
<td>-134 dBc/Hz</td>
</tr>
</tbody>
</table>
6.2 Output Power

In this part, power measurements and harmonics are discussed. In this setup to protect spectrum analyzer from excessive power a 13 dB attenuator is connected to output, and power is measured as -0.44 dBm as shown in Figure 6.5. By adding attenuator and cable loss, power output is measured to be about 13 dBm. Output power measurement is the same as simulation result which is given in section 4.3.1. This power is usually sufficient to drive mixers, otherwise a low noise amplifier could be added in module to increase output power level.

Harmonics of oscillator measured as -22dBc for 2\textsuperscript{nd} harmonic and -41dBc for 3\textsuperscript{rd} harmonics which is shown in Figure 6.6. In this design, no filter is used to suppress harmonics.

Figure 6.5 Fundamental Oscillator Signal
6.3 PLL Performance

In this part of the thesis, PLL performance is evaluated. At steady state or during lock, varactor tuning voltage must be a DC value as shown in Figure 6.7 for this case PLDRO output frequency is constant, and output frequency is an integer multiple of the frequency of reference signal. If PLL is out of lock-in range or reference signal is switch off, PLL acquisition circuitry works and triangular search is observed as seen in Figure 6.8
Figure 6.7 Varactor tuning voltage at steady state

Figure 6.8 Varactor tuning voltage at out of locking range
PLL performance is also evaluated when an abrupt change in the frequency of reference signal occurs. In Figure 6.9 frequency of reference is decreased and increased, respectively. When frequency is suddenly changed, firstly acquisition circuit becomes dominant and linear search is observed then during linear search phase error diminishes and loop filter tune to varactor voltage. PLL reaches steady state in 5 ms to 25 ms for sudden changes. Behavior of tuning voltage is also similar to simulation results which is given in section 5.2

In next section, PLDRO performance with respect to temperature variation is given.

Figure 6.9 Varactor voltage vs time (case abruptly decrease in reference frequency)
6.4 Thermal Measurement Tests

Frequency of oscillators shift due to aging and temperature variations and the PLL should be able to compensate these changes, provided that such changes remain in the lock-in range of the PLL.

For temperature variation setup, a constant reference is provided to PLDRO, and varactor tuning voltage, phase noise, output power and frequency are observed. Results are tabulated in Table 6.2 and Table 6.3. In these tables reference signal is selected such that multiplication factor of SRD is 80 and 40, respectively. In Figure 6.11 and Figure 6.12 temperature vs. tuning voltage is given graphically. Results show that PLL can compensate temperature variations up to 45°C, which may not be adequate for local oscillator applications. On the other hand, by increasing electronic tuning range of oscillator, temperature performance can be improved. To achieve this, location of transmission line connected to varactor diode should be adjusted so that electronic tuning range is increased; however, loaded quality factor of resonator might decrease, and phase noise might become worse. Another solution could be using a varactor diode
which is more sensitive to changes in capacitance. Another solution could be
increasing voltage range of PLL above than 10volts. Furthermore tuning voltage does
not change linearly with temperature as shown in Figure 6.11 and Figure 6.12, this
could be also solved by adjusting the length of the transmission line which is connected
to the varactor diode.

It is observed that the output power and phase noise are only slightly affected by
change in temperature. However, this observation could be due to measurement error
since calibrations, cable and connector loss might change with time.

Table 6.2 Temperature Performance for Multiplication factor 80

<table>
<thead>
<tr>
<th>Temp C°</th>
<th>Frequency of Reference (MHz)</th>
<th>Frequency of PLDRO (MHz)</th>
<th>Varactor Tuning Voltage (V)</th>
<th>Output Power (dBm)</th>
<th>Supply Voltage (V)</th>
<th>Supply Current (mA)</th>
<th>Phase Noise dBC/Hz @ 1MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>100.74</td>
<td>8059.2</td>
<td>0.7</td>
<td>13.6</td>
<td>12V</td>
<td>88mA</td>
<td>-131</td>
</tr>
<tr>
<td>15</td>
<td>100.74</td>
<td>8059.2</td>
<td>1.87</td>
<td>13.6</td>
<td>12V</td>
<td>88mA</td>
<td>-132</td>
</tr>
<tr>
<td>25</td>
<td>100.74</td>
<td>8059.2</td>
<td>2.86</td>
<td>13.55</td>
<td>12V</td>
<td>88mA</td>
<td>-134</td>
</tr>
<tr>
<td>30</td>
<td>100.74</td>
<td>8059.2</td>
<td>3.93</td>
<td>13.55</td>
<td>12V</td>
<td>88mA</td>
<td>-133</td>
</tr>
<tr>
<td>40</td>
<td>100.74</td>
<td>8059.2</td>
<td>7.4</td>
<td>13.5</td>
<td>12V</td>
<td>88mA</td>
<td>-134</td>
</tr>
<tr>
<td>45</td>
<td>100.74</td>
<td>8059.2</td>
<td>9.5</td>
<td>13.45</td>
<td>12V</td>
<td>88mA</td>
<td>-132</td>
</tr>
</tbody>
</table>
Figure 6.11 Varactor Tuning Voltage Vs Temperature with multiplication factor 80

Table 6.3 Temperature Performance for Multiplication factor 40

<table>
<thead>
<tr>
<th>Temp C°</th>
<th>Frequency of Reference (MHz)</th>
<th>Frequency of PLDRO (MHz)</th>
<th>Varactor Tuning Voltage (V)</th>
<th>Output Power (dBm)</th>
<th>Supply</th>
<th>Phase Noise dBc/Hz @ 1MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>201.48</td>
<td>8059.2</td>
<td>0.6</td>
<td>13.6</td>
<td>12V 108mA</td>
<td>-134</td>
</tr>
<tr>
<td>15</td>
<td>201.48</td>
<td>8059.2</td>
<td>1.94</td>
<td>13.6</td>
<td>12V 107mA</td>
<td>-133</td>
</tr>
<tr>
<td>25</td>
<td>201.48</td>
<td>8059.2</td>
<td>3.45</td>
<td>13.55</td>
<td>12V 107mA</td>
<td>-134</td>
</tr>
<tr>
<td>30</td>
<td>201.48</td>
<td>8059.2</td>
<td>4.87</td>
<td>13.55</td>
<td>12V 107mA</td>
<td>-134</td>
</tr>
<tr>
<td>40</td>
<td>201.48</td>
<td>8059.2</td>
<td>9.52</td>
<td>13.45</td>
<td>12V 106mA</td>
<td>-133</td>
</tr>
</tbody>
</table>

Figure 6.12 Tuning Voltage Vs Temperature with multiplication factor 40
CHAPTER 7

CONCLUSION

7.1 Summary of the work

In this thesis, design and fabrication of the PLDRO is given. As mentioned in chapter 2, phase noise of an oscillator plays an important role for system performance since phase error has a strong effect on proper detection.

In chapter 3 and 4, design considerations of DR and DRO are given, respectively. In these chapters it is mentioned that cavity volume, tuning screw, and tolerances should take into consideration for a success design. Furthermore, design steps of a DRO are given, these design steps can be used for all type of microwave oscillators. In chapter 5, PLL design for DRO is given by considering optimum noise and locking time.

Measurement results of PLDRO is given in chapter 6. Output power at the 8 GHz is measured to be 13 dBm, and the phase noise drops down to -134 dBC/Hz at 1 MHz offset.

The object of this work is to gain perspective on design of PLDRO to RF engineer. Researchers and engineers who are interested in DRO and PLDRO could use this work as a design guide since those designs were given not only by considering theoretical bases but also considering practical and computer aided design methodology.
7.2 Future Work

In this study, know-how is gained about design of PLDRO. For further studies, PLDRO design will progress, and experiences gained in this work will be used to design and produce commercial PLDRO.

Measurement results showed that voltage range of PLL is not sufficient to compensate temperature variation up to 45°C changes. To set operating temperature between -20°C and 70°C which is usable range for commercial PLDROs [24], electrical tuning range must be increased from 2MHz to 5-10 MHz. To achieve this, length of transmission line which is connected to varactor diode should be tuned, additionally varactor diode and its transmission line should be close to DR. Another solution is that increasing PLL voltage range with respect to operating temperature of varactor.

Phase noise of oscillator can also be improved. Decreasing distance between DR and microstrip lines could reduce phase noise of DRO. Moreover, in this design regulator circuitries had problematic as mentioned in section 6.1, using low noise and stable regulators will help to reduce phase noise. PLL circuitry has also effects on phase noise; in next prototypes PLL loop bandwidth and loop gain will be designed by considering both noise performance and locking performance.

In addition to 8GHz PLDRO, different frequencies will be also designed. RF part of module will be modified such that all RF elements will be locates on printed substrate instead of metal carrier, and printed substrate will has tuning pads to reconfigure for different oscillation frequency and to provide post fabrication tuning.
REFERENCES


