COMPARATIVE DESIGN OF MILLIMETER WAVE RF-MEMS PHASE SHIFTERS

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COMPARATIVE DESIGN OF MILLIMETER WAVE RF-MEMS PHASE SHIFTERS

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ABSTRACT

COMPARATIVE DESIGN OF MILLIMETER WAVE RF-MEMS PHASE SHIFTERS

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Phase shifters are widely used for electronic beam steering for various antenna applications. This thesis presents design and comparison of 3 different 3-bit transmission type phase shifters, which are switch-line, Distributed MEMS Transmission Line (DMTL) and triple stub phase shifters, realized with capacitive contact Radio Frequency (RF) Micro-Electro-Mechanical Systems (MEMS) switches for Ka-Band applications. For the design of switch-line phase shifter reducing the sensitivity of the electrical performance to the fabrication tolerances and by this way increasing the yield is targeted by minimizing the air-bridges used in the design. In order to achieve this, new Coplanar waveguide (CPW) T-junction and CPW bend structures are designed. For DMTL phase shifter design, a new method based on using circuit models is used instead of the conventional DMTL phase shifter for reducing the computational work and for preventing to obtain an inapplicable design, because of the dimensions, with the conventional method. In this thesis also a triple stub phase shifter is designed with the motivation of reducing the number of control bits. Comparisons of these phase shifters are done in terms of their insertion/return losses, maximum phase errors, bandwidths at 35 GHz, pull-in voltages of the switches used in the designs, layout dimensions of the phase shifters and number of control bits of the phase shifters. DMTL phase shifter is the most favourable phase shifter in terms of its low loss, small size and low pull-in voltage. Whereas switch-line phase shifter shine outs only with its large bandwidth. Compared with DMTL and switch-line phase shifters,

triple stub phase shifter is only favourable in terms of its layout dimensions.

Keywords: RFMEMS, phase shifter, DMTL, triple stub, switch-line phase shifter

ÖZ

MİLİMETRE DALGA'DA KARŞILAŞTIRMALI RF-MEMS FAZ KAYDIRICI TASARIMI

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Haziran 2016 , 65 sayfa

Faz kaydırıcılar birçok anten uygulamasında ışın demetinin yönlendirilmesinde kullanılmaktadır. Bu tez Ka-bant uygulamaları için sığal RF MEMS anahtarlar ile gerçekleştirilen 3 farklı iletim tarzlı faz kaydırıcının; hat-seçme, Dağıtılmış MEMS iletim hattı (DMİH) ve 3lü saplamalı faz kaydırıcılar; tasarım ve karşılaştırmasını içermektedir. Hat-seçmeli faz kaydırıcının tasarım sürecinde elektriksel performansın üretim toleranslarına hassasiyetini en aza indirgemek ve buna bağlı olarak üretim verimini arttırmak hedeflenmiştir. Bunun için yeni eşdüzlemsel dalga kılavuzu (EDK) T-bileşim ve EDK dirsek tasarlanmıştır. DMİH faz kaydırıcı tasarımında geleneksel tasarım yönteminden farklı olarak devre modellerinin kullanılmasını temel alan yeni bir yöntem kullanılmıştır. Bunun nedeni sayısal yükü azaltmak ve geleneksel yöntem sonucunda ortaya çıkabilecek uygulanamaz tasarımları engelleme isteğidir. Ayrıca bu tezde kontrol sayısını azaltmak hedeflenerek yeni bir 3lü saplamalı faz kaydırıcı tasarımı yapılmıştır. Tasarımı yapılan faz kaydırıcıların karşılaştırmaları 35 GHz'de araya girme/geri dönüş kayıpları, en yüksek faz hatası, bant genişliği, tasarımlarda kullanılan anahtarların uyarım voltajları, faz kaydırıcıların serim boyutları ve kontrol sayıları göz önüne alınarak yapılmıştır. DMİH faz kaydırıcı tasarımı düşük kayıp ve boyutları ile öne çıkarken hat-seçmeli faz kaydırıcı geniş bant özelliği ile öne çıkmaktadır. DMİH ve hat-seçmeli faz kaydırıcı tasarımları ile karşılaştırılıdığında 3lü saplamalı faz kaydırıcı tasarımı sadece küçük serim boyutları ile öne çıkmaktadır.

Anahtar Kelimeler: RFMEMS, faz kaydırıcı, DMİH, 3lü saplama, hat seçmeli faz kaydırıcı

To my family

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I want to reserve my family's place. I would like to show my gratitude to my mother Aysun Kobal, my father Selami Kobal and my brother İlyas Kobal for their 25 years support. They deserve this success more than anybody. I also would like to thank my niece Ela Kobal for being joy of my family.

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LIST OF ABBREVIATIONS

GaAs	Gallium arsenide
MEMS	Micro-Electro-Mechanical Systems
CPW	Coplanar waveguide
SPDT	single-pole-double-throw
SPST	single-pole-single-throw
NI	National Instruments
HFSS	High Frequency Structure Solver
DMTL	Distributed MEMS Transmission Line
MIM	metal-insulator-metal
MAM	metal-air-metal

CHAPTER 1

INTRODUCTION

Controlling events is the biggest desire of the human beings through out the history of man kind. Starting with Nikola Tesla, they started to learn wireless control which ease their life. Wireless control trials started with single, simple antennas and in today's world, simple antennas evolve into antenna arrays. Biggest advantage of antenna arrays compared to the single antennas is with antenna arrays, main beam can be directed to a specific direction with beam steering.

Beam steering is very crucial for some cases like tracking an object or in a short range communication system in order to increase the quality of the communication. This steering can be mechanical, which is carried out with motors that change the positions of the antennas, or it can be electrical, which is realized with phase shifters that change the angle of the main beam. Mechanical beam steering is simple compared to the electrical beam steering since only motors are needed. However, because of the fact that steering is mechanical, it is slower than electrical beam steering. Furthermore, this mechanical movement introduces noise to the system. In order to minimize the noise introduced by the movement of the antennas, rotation must be smooth. Both mechanical and electrical beam steering techniques can be used depending on the requirements of the application. For applications like tracking a fast object or daily life communication systems, fast beam steering is required. That is why electrical beam steering with phase shifters is preferred for these applications.

Phase shifters are composed of variable or reconfigurable tools. Reconfigurability can be achieved by electromechanical movement or using semiconductor, ferrimagnetic or ferromagnetic materials. Depending on which method is chosen, phase shifters

can be categorized as analog and digital. Analog phase shifters' working principle is based on controlling phase shift by changing the applied voltage. Whereas digital phase shifters work by stimulating the corresponding bits with voltage. Phase shift can be obtained by stimulating necessary bits.

Analog phase shifters can be realised with ferrimagnetic, ferromagnetic or semiconductor materials. Ferrimagnetic and ferromagnetic phase shifters are based on inducing the magnetic anisotropy of the material by applying a DC voltage to a coil wrapped around this material. Amount of phase shift can be controlled with the applied DC voltage. Because of its high resistivity and significant amount of anisotropy at microwave frequencies, ferrimagnetic materials are prefered instead of ferromagnetic materials. There are several examples of ferrite phase shifters in the literature [1, 2]. Origin of ferrite phase shifters leans on 1950s but today there are still new researches held on this topic [3]. Main drawback of ferrite phase shifter is the power consumption on the coils: in order to create magnetic field inside the ferrite, current must be fed to the coil which results in extra power consumption [4]. Furthermore, switching time of ferrite phase shifter is slow compared to the phase shifters realised with semiconductor materials, in the order of 100 μ-seconds [4]. Besides all, ferrite phase shifters are still used in specific applications which needs high RF power.

Digital phase shifters designed on semiconductor materials, such as gallium arsenide (GaAs), shine out with their fast switching times [5] and small surface areas [6, 7]. However, these phase shifters cannot handle high RF power compared to the ferrite phase shifters. In addition to these, fabrication on GaAs is expensive since GaAs is an expensive material. Silicon is another semiconductor that can replace GaAs. Compared to the phase shifters designed on GaAs, phase shifters designed on silicon have higher insertion losses [8] but fabrication is cheaper.

RF-MEMS (Radio Frequency Micro-Electro-Mechanical System) technology is recently an attractive technology used for digital phase shifter design. Low loss, low cost and suitability for integrated fabrication are the three main properties of this technology which make RF-MEMS attractive. RF-MEMS is based on the electromagnetic actuation and physical movement of the structures. By using this property, switches or variable capacitors can be designed and used in various phase shifter designs: switch

elements can be used for guiding the signal into different channels whereas variable capacitors can be used for loading the transmission line by changing the characteristic impedance and phase velocity of the transmitting wave. Both of these two structures are based on capacitance change: as it can be seen from Figures 1.1 - 1.2, capacitive contact RF-MEMS switches have two different capacitance values for up and down cases [10].

Various phase shifters can be designed with RF-MEMS switches and variable capacitances. These phase shifters can be gathered under the titles of transmission type phase shifters and reflection type phase shifters. For reflection type phase shifters, mainly couplers are used with two ports terminated with structures offering variable reflection controlled by bias voltage [11, 12]. For constant phase shifter designs, mostly reflection type phase shifters are used. In order to obtain constant phase characteristics, two couplers cascaded back to back [13] or other structures, like all-pass structure [14], are used.

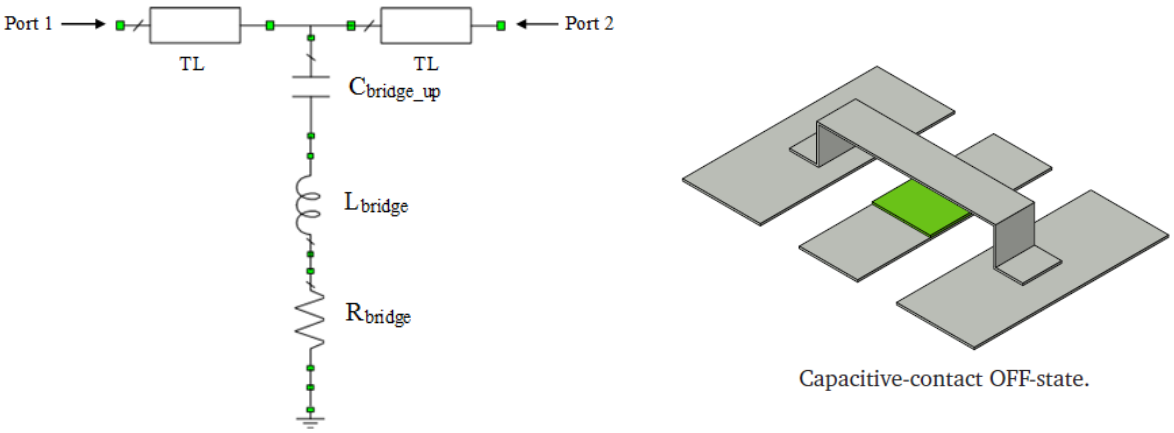
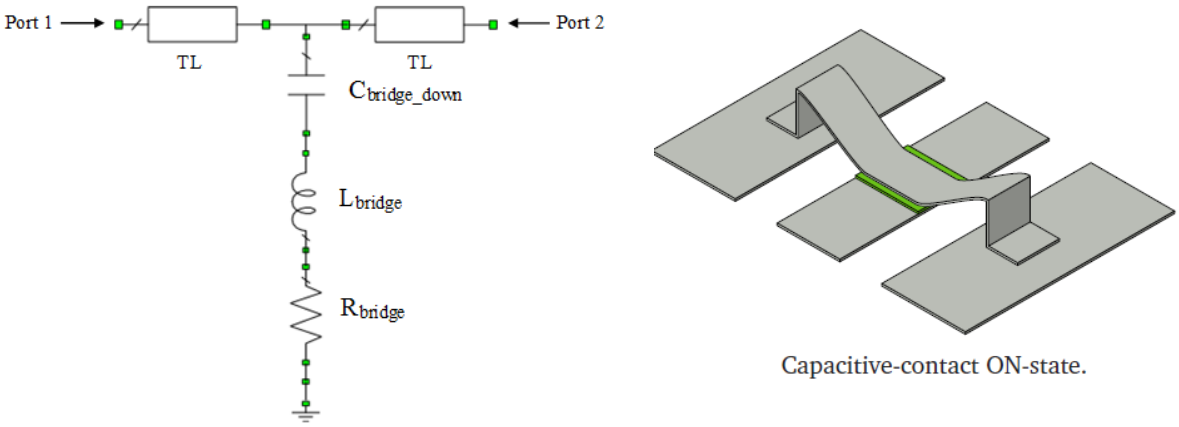


Figure 1.1: (a) Circuit model and (b) schematic projection of a switch in up position [9].

Switch-line [15–17] and distributed MEMS transmission line (DMTL) [18–20] phase shifters are two most common examples of transmission type phase shifters. Switch-line phase shifters are basically composed of two single-pole-double-throw (SPDT) switches and two transmission lines between the switches. SPDT switches are responsible for directing the wave into one of its outputs. By switching between two



(a) (b)

Figure 1.2: (a) Circuit model and (b) schematic projection of a switch in down position [9].

transmission lines with different length, relative phase shift can be obtained. This type of phase shifters is also an example of true-time delay phase shifters since relative phase shift is obtained by transmission line length difference. DMTL phase shifter is also an example of true-time delay phase shifters. DMTL phase shifter working principle is based on loading the transmission line: Switches, or in other words unit cells, used in DMTL phase shifter are not used for ensuring isolation between its two ports instead they are used as variable capacitors. Previously it is discussed that RF-MEMS switches have two different capacitance values for their up and down states which are parallel connected to the transmission line. If the necessary up/down ratio for the unit cells are calculated, relative phase shift between up and down states can be obtained by changing the phase velocity of the propagating wave by the unit cell.

Using stubs in the phase shifters is not a new concept but they are mainly used in switched line phase shifters for loading one of the transmission lines [21]. Triple stub circuit topology theoretically can convert any impedance connected as a load to one of its port to any input impedance of the other port with infinitely many stub length combinations. By using this property, RF-MEMS phase shifter can be designed with this circuit topology by changing the stub lengths effectively with RF-MEMS switches. Because of the fact that triple stub phase shifter has two ports, it is also an example for transmission type phase shifter. However, it is not a true-time delay phase shifter since working principle of this phase shifter does not depend on length difference.

Instead, it depends on resonance.

RF-MEMS phase shifters cannot handle RF power as much as ferrite phase shifters. Reason behind this is the charging of the switches: if swithces are charged, they will stuck in down position. If the charging effect is disregarded, RF-MEMS phase shifter still cannot handle power as much as ferrite phase shifters because of the dielectric breakdown. However; in order to improve power handling of the RF-MEMS phase shifters, specific researches are done [22–24]. In terms of switching time, RF-MEMS phase shifter has much successful performance than ferrite phase shifters.

In this thesis comparative design of switch-line, DMTL and triple stub phase shifters on a 500 μm thick glass substrate is carried out in details. Objectives of this thesis work is to find the optimum 3-bit phase shifter design which:

- operates at 35 GHz.
- has minimum insertion loss.
- has minimum return loss.
- occupies minimum area.
- has switching elements whose pull-in voltages are lower than 25 V.
- has a maximum phase error better than 5 %.
- has minimum number of controls.
- needs minimum computational work.

Glass substrate is chosen because of the fabrication process flow, which is going to be explained in details in Chapter 2.4. Since this process flow is repeatable and suitable only for glass, glass is chosen as the substrate for the designs.

Antenna array size is inversely proportional with the phase resolution criteria for scanning a specific sector. In most of the antenna applications, 3- or 4-bit phase shifters are used. In order to decrease computational work of this thesis and knowing that designing 4-bit phase shifters are nothing but repeating the procedures which are going to be discussed in the upcoming chapters, 3-bit is chosen at the beginning of this thesis work. 35 GHz center frequency is chosen for decreasing the sizes of both antennas and phase shifters. Furthermore, 35 GHz is sufficient for short-range communication systems.

Throughout each phase shifter design, coplanar waveguide (CPW) is used as the transmission line instead of microstrip line since with the fabrication process discussed in the Chapter 2.4, opening and coating vias is not possible. That is why ground plane must be on the same level with the signal line so in order to use the process flow discussed in Chapter 2.4, using CPW is obligatory. Characteristic impedance of a CPW depends on the:

- dielectric characteristic of the substrate on which CPW is designed.
- thickness of the substrate.
- electrical performance of the conductor layer outspread on the substrate.
- thickness of the conductor layer.
- space between the ground plane and signal line.
- width of the signal line.
- design frequency.

Dielectric constant (ε_r), thickness and tangent loss ($tan\delta$) of the substrate (t_{subs}), conductivity (σ) and thickness (t_{cond}) of the conductor layer are fixed values knowing that glass substrate and gold are used for the fabrication. These fixed values are tabulated in Table 1.1.

Table 1.1: Fixed values for the glass substrate and the gold used in the design of the phase shifters.

PARAMETER	VALUE
ε_r	4.6
$tan\delta$	0.015
t_{subs}	500 μm
σ	$3 \times 10^7 S/m$
t_{cond}	1 μm

Switch-line and DMTL phase shifters discussed in this thesis are designed on systems with different characteristic impedances. In order to find the dimensions of the CPWs with these characteristic impedances, formulations presented in Equation 1.1 [25] are used. However, these formulations do not include radiation loss. Most of the travelling wave in a CPW propagates in air between signal line and ground plane so increasing the spacing between ground plane and signal line will result in an increase in the insertion loss due to the increase in the radiation loss. So for finding the di-

mensions of the optimum CPW with minimum radiation loss, simulations are held in Ansys HFSS.

$$
\begin{aligned}
Z_{ch} &= \frac{Z_0}{2 \times \sqrt{\varepsilon_{eff}} \times \left[\frac{K(k_1)}{K(k_1')} + \frac{K(k_2)}{K(k_2')} \right]} \\
Z_0 &= 120 \times \pi \\
\varepsilon_{eff} &= \frac{\varepsilon_r + 1}{2} \\
K(k), K(k') &\text{ are the complete elliptical integrals of the first kind}
\end{aligned}
\tag{1.1}
$$

Design of each phase shifter which are compared in this thesis are investigated in separate chapters. In Chapter 2, design of building blocks of a 3-bit switch-line phase shifter are discussed. Also the details of the fabrication process developed at METU-MEMS Research and Application Center is given in this chapter. Novel design procedure of a 3-bit DMTL phase shifter is discussed in Chapter 3. In Chapter 4, mathematical design of a 3-bit triple stub phase shifter is contended. Comparisons of the expected results belonging to these phase shifter are done in Chapter 5. Future works of this thesis are also shared in this chapter.

CHAPTER 2

SWITCH-LINE PHASE SHIFTER

2.1 Introduction

In this chapter a 3-bit switch-line phase shifter which is designed at 35 GHz on a 500 μm thick glass substrate (ε_r=4.6, tanδ=0.015 at 35 GHz) is presented. For the design, coplanar waveguide (CPW) structure is used as the transmission medium. Each bit of the phase shifter, whose layout is shown in Figure 2.1, consists of 2 single-pole-double-throw (SPDT) switches and 2 transmission lines with different lengths: one of these transmission lines is the reference line and its length is constant for each bit and the other transmission line is chosen in order to obtain the relative phase with respect to the reference line.

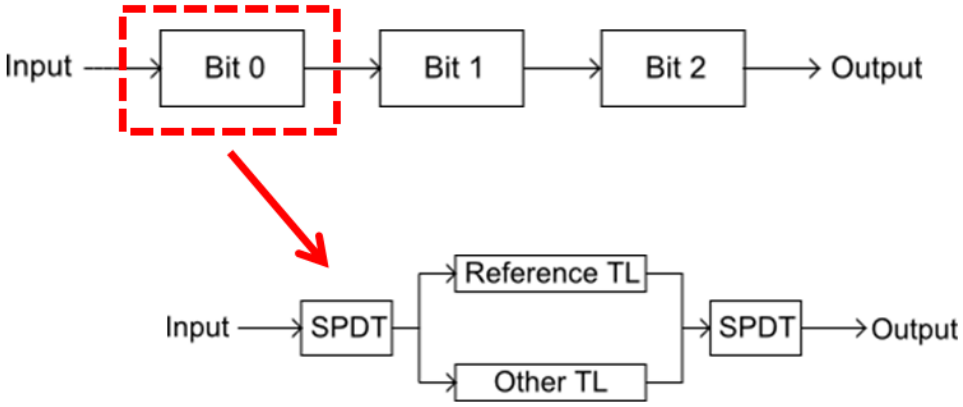


Figure 2.1: Layout of a 3-bit switch-line phase shifter.

Any directional change on CPW means a discontinuity. CPW discontinuities in the SPDT switches might introduce a potential difference between the ground planes and

cause undesired modes to propagate down the transmission line. In order to prevent such detrimental effects, one typically uses air-bridges at CPW discontinuities. These air-bridges, however, cause an increased return/insertion loss due to their parasitic capacitance. To mitigate the effect of air-bridges on the RF performance, the switch design uses a minimum number of air-bridges with proper impedance compensation. By this way, it is aimed to have electrical performance less sensitive to the fabrication tolerances.

In this chapter, design of SPDT switches, each bit of the phase shifter, and fabrication process are investigated deeply.

2.2 SPDT Switch Design

Figure 2.2 illustrates a schematic view of the SPDT switch. The switch employs a CPW structure as the transmission medium, and comprises a CPW T-junction followed by right-angled CPW bends. Series metal-insulator-metal (MIM) capacitors isolate the output ports in terms of their DC bias. Two RF MEMS switches operating in opposite states set the path of the signal among the two output ports.

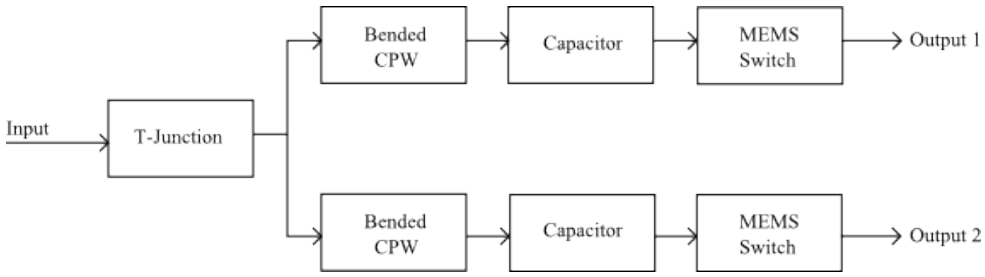


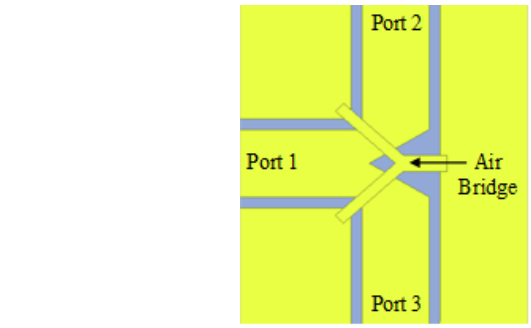
Figure 2.2: Illustration of the SPDT switch and its components.

2.2.1 CPW T-Junction

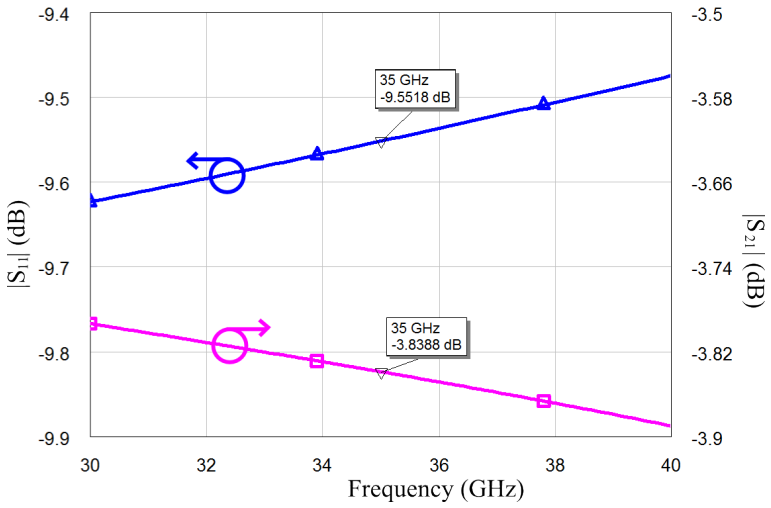
As it was stated in the introduction section of this chapter, air-bridges are needed at the CPW discontinuities. In [26] a T-junction with 3 air-bridges are proposed. Decreasing the number of air-bridges is one of the main targets of this design. That is why a new T-Junction design is performed.

Figure 2.3a shows the layout of the designed CPW T-junction. The design employs a Y-shaped bridge not only to minimize the capacitive area over the CPW signal trace, but also to reduce the electrical sensitivity of the junction on fabrication tolerances in an effort to improve the process yield. Impedance matching sections as well as the reduced capacitive overlap improve the return and insertion losses of the junction.

Figure 2.3b presents the simulated S-parameters of the designed junction terminated in 50 Ω reference impedance. The junction presents 9.55 dB return loss and 3.84 dB insertion loss at 35 GHz. These values are very close to those of an ideal lossless junction (9.54 dB and 3.52 dB respectively). When utilized in the SPDT switch, one of the junction output ports will be open circuited during the operation since the RF MEMS switches, which will be discussed shortly, will operate in opposite states.



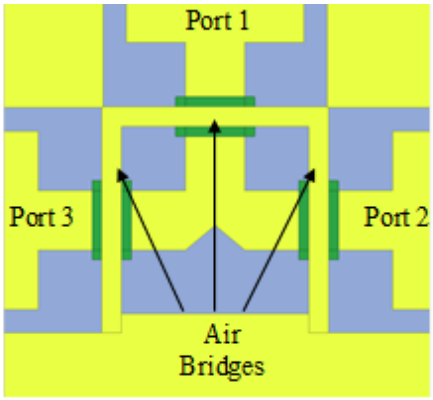
(a)



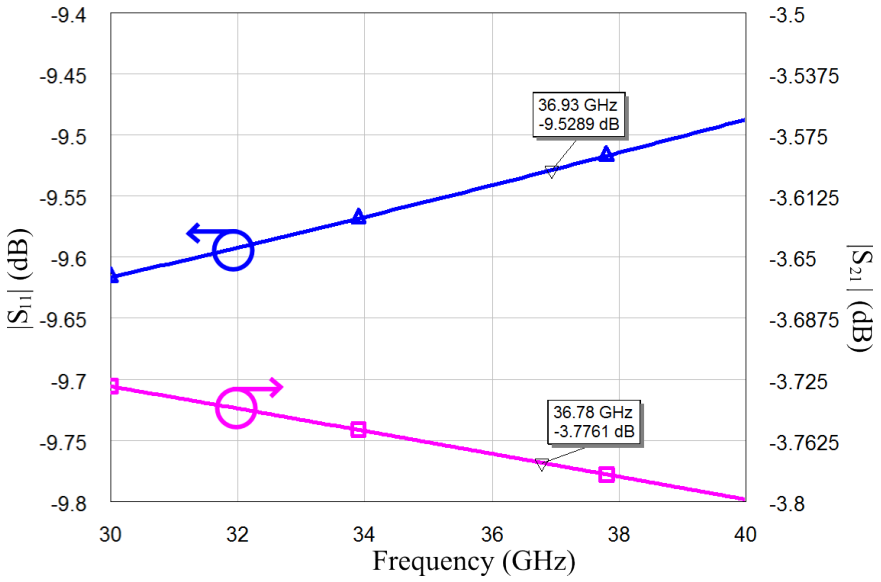
(b)

Figure 2.3: (a) Top view and (b) simulated $|S_{i1}|$ of the designed CPW T-junction with one air-bridge.

After finalizing the design, area of the Y-shaped air-bridge is calculated as approximately 17634 μm^2. According to the results of the previous fabrications done in METU-MEMS Research and Application Center, great amount of bending in the vertical axis of the bridge after the releasing step of the fabrication process is expected which will result in electrical performance degradation. On the ground of this knowhow, a new T-junction with three air-bridges is designed. Layout and expected S-parameters of the new design are presented in Figure 2.4a and Figure 2.4b respectively.



(a)



(b)

Figure 2.4: (a) Top view and (b) simulated $|S_{i1}|$ of the designed CPW T-junction with three air-bridges.

According to the simulation results, expected return loss and insertion loss are respectively 9.53 dB and 3.78 dB. It is beneficial to remind one more time that return loss of an ideal lossless T-junction is 9.55 dB whereas its insertion loss is 3.52 dB.

Design of this T-junction is held in HFSS. After several simulations, final dimensions are found and tabulated in Table 2.1.

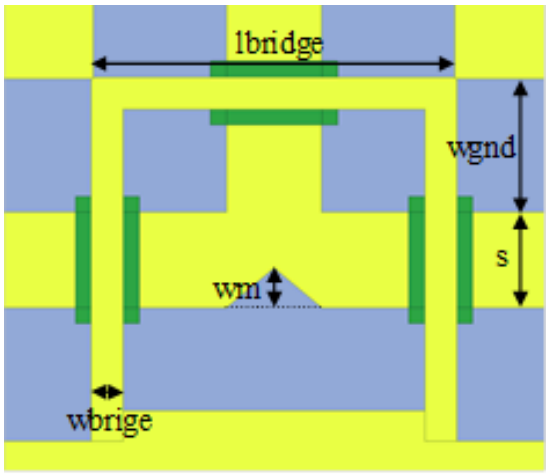


Figure 2.5: Notations used for the dimensions of the designed T-junction with 3 air-bridges.

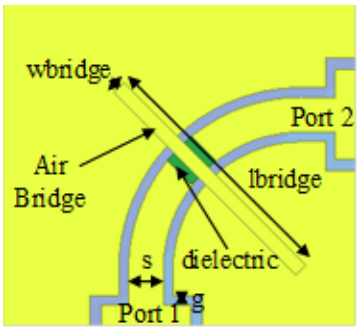
Table 2.1: Dimensions of the designed T-junction with 3 air-bridges

Parameter	Value (μm)
lbrdige	228
wgnd	85
s	60
wm	25
wbridge	20

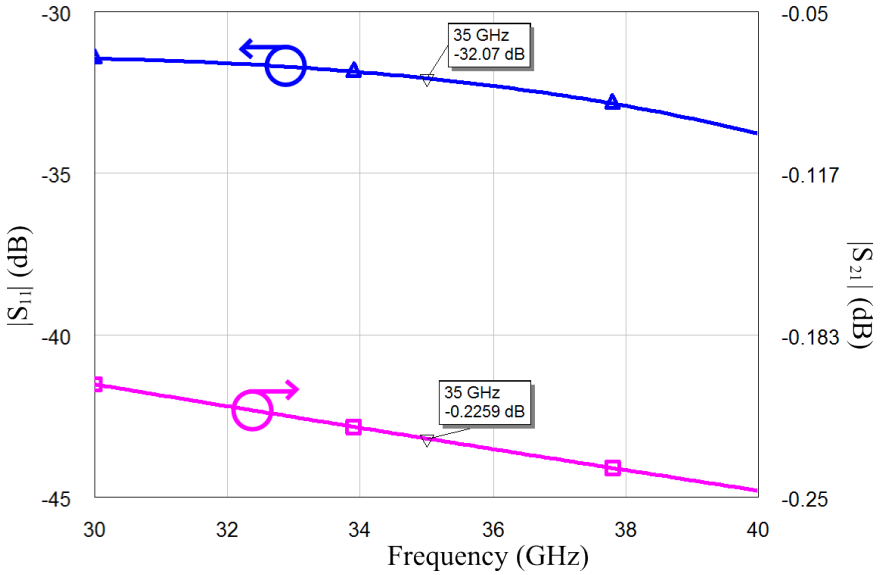
For the ports, a CPW which has 180 μm signal width with 24 μm signal-ground opening is used in order to pass from high-Z system to 50 Ω system. No transition is designed between these two systems.

2.2.2 CPW Bend

In [26] a 90° bended CPW structure with two air-bridges is proposed. In the proposed design, air-bridges are put in front of the ports. In order to decrease the number of air-bridges, a CPW bend with one air-bridge is designed. In the designed bend, air-bridge is placed onto the middle of the structure as it can be seen from Figure 2.6a.



(a)



(b)

Figure 2.6: (a) Top view and (b) simulated $|S_{i1}|$ of the designed CPW bend.

Similar to the design of T-junction, simulations for CPW bend are held in HFSS in order to find the optimum dimensions for minimum insertion loss. Dimensions for the final design is tabulated in Table 2.2. With respect to these dimensions, expected results show that designed CPW bend offers 0.22 dB insertion loss and 32 dB return

loss. 0.22 dB insertion loss corresponds to 95 % transmission. For the return loss case, 32 dB return loss provides a good matching.

Table 2.2: Dimensions of the designed 90° CPW bend

Parameter	Value (μm)
wbridge	15
lbridge	522
s	70
g	20

Length labelled as "lbridge" in the schematic presented in Figure 2.6a is not the overall length of the suspending part of the bridge. If the lengths of the anchors of the bridge are subtracted, overall bridge length, which is 97 μm, can be obtained. If the length of the bridge is chosen too long, it will have an inductive effect on the $|S_{11}|$. In other words, return loss of the design will increase which will also cause an increase in the insertion loss. With the simulations held in HFSS, optimum bridge length is found.

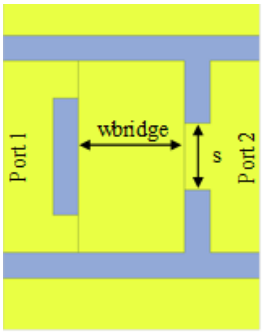
2.2.3 Series MIM Capacitor

MIM capacitors are crucial for providing DC isolation. If MIM capacitors are not inserted to the design, it would be impossible to excite switches one by one since signal line is used for excitation and it is common for all switches. Some of the air-bridges could also be pulled-down if the applied voltage is higher than their pull-in voltages. In order to prevent these scenario, series MIM capacitors are designed and inserted to the design.

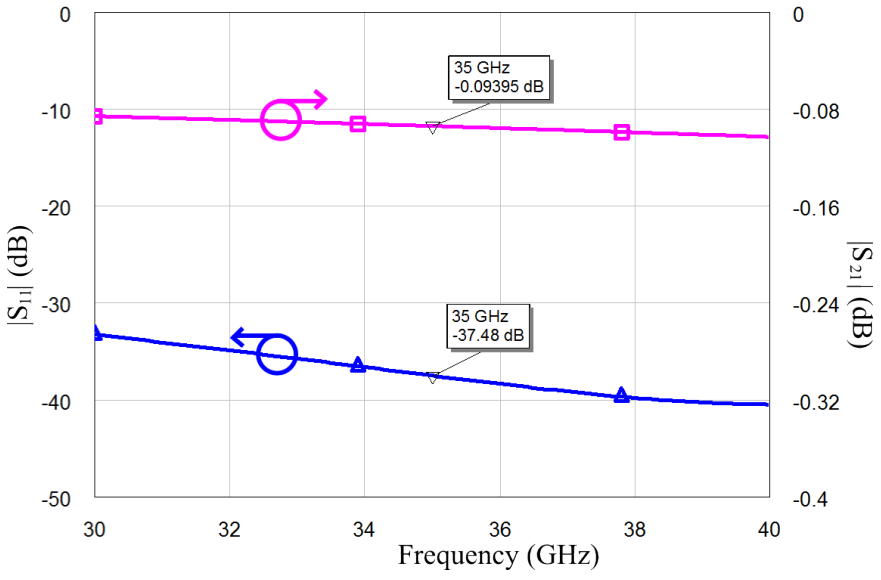
For isolation capacitor, 1.2 pF is chosen as the starting point. Necessary dimensions are calculated by using the nominal capacitance formula, which is shown in Equation 2.1.

$$
\begin{aligned}
C &= \varepsilon \times \frac{\text{Conductor Area}}{\text{Distance Between the Conductors}} \\
\varepsilon &= \varepsilon_0 \times \epsilon_r \\
\text{Conductor Area} &= s \times wbridge \\
\text{Distance Between the Conductors} &= t_d
\end{aligned}
\tag{2.1}
$$

In Equation 2.1 ε_0 represents the free space permittivity, ε_r represents the dielectric constant, *wbridge* represents the bridge width which is also shown in Figure 2.7a, s represents the signal line width and t_d represents the dielectric thickness. As a dielectric, silicon-nitrate, which has dielectric constant 7, is used.



(a)



(b)

Figure 2.7: (a) Top view and (b) simulated $|S_{i1}|$ of the designed series MIM capacitor.

Minimum insertion loss is aimed and iterative simulations are performed in HFSS. For this condition which is equivalent to minimum return loss, optimum s value is searched for. According to the simulation results, *wbridge* is found as 100 μm and s is found as 62 μm. These dimensions lead to a capacitance value which approximately equals to 1.23 pF. For the transitions at the ports, a CPW with signal width equals to 180 μm and signal-ground opening equals to 24 μm is chosen. Expected $|S_{i1}|$ of the series MIM capacitor are presented in Figure 2.7b. According to these results, approximately 0.094 dB insertion loss is expected from the MIM capacitor. In other words, more than 97 % of the propagating wave can pass to the other port of the capacitor. That is to say RF wise this capacitor design can assumed to be non-existent while it provides DC isolation.

2.2.4 RF-MEMS Capacitive Switch Element

The SPDT switch configuration employs two RF-MEMS switch elements operating at opposite states. For these switch elements, capacitive-contact RF-MEMS switches are designed similar to the ones in [9] using HFSS. Layout of the designed switch is given in Figure 2.8 and dimensions of the switch are tabulated in Table 2.3.

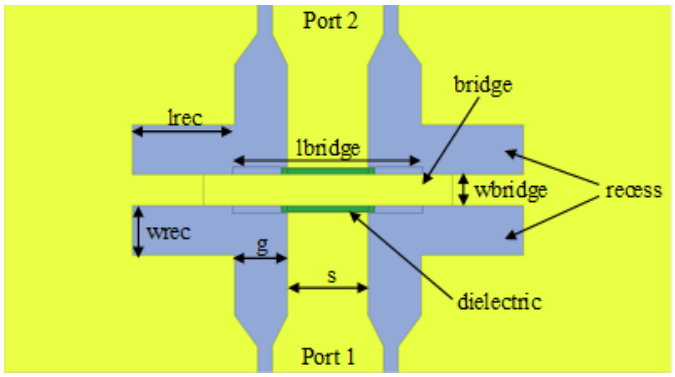


Figure 2.8: Layout of the designed capacitive-contact RF-MEMS switch.

For 50 Ω transitions at the two ports, again a CPW with a signal width 180 μm and a signal-ground opening 24 μm are used. By using the dimensions given in Table 2.3, expected characteristics of the switch are found and shown in Table 2.4 and tabulated in Table 2.4. According to these results, designed RF-MEMS switch offers an

Table 2.3: Dimensions of the designed capacitive-contact RF-MEMS switch

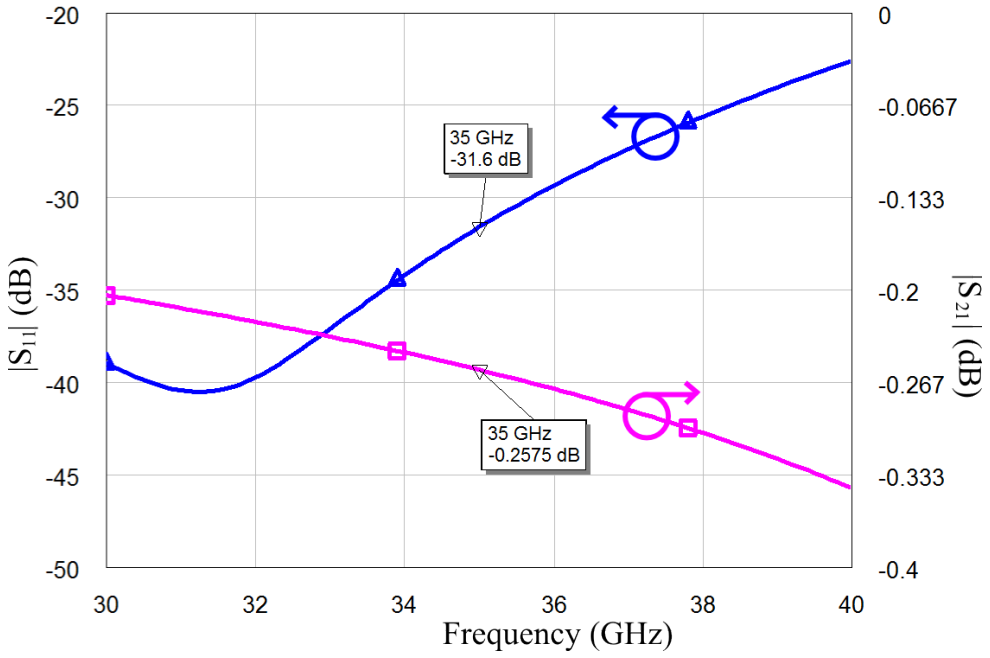
PARAMETER	VALUE (μm)
lrec	165
wrec	80
lbridge	307
wbridge	50
g	86
s	130

isolation better than 52 dB at 35 GHz. In other words, only 0.00063 % of power is transmitted to the other port when the switch is in down position. For the up case, 31.6 dB return and 0.25 dB insertion losses show that this switch design has a good input matching while 94 % power transmission is provided.

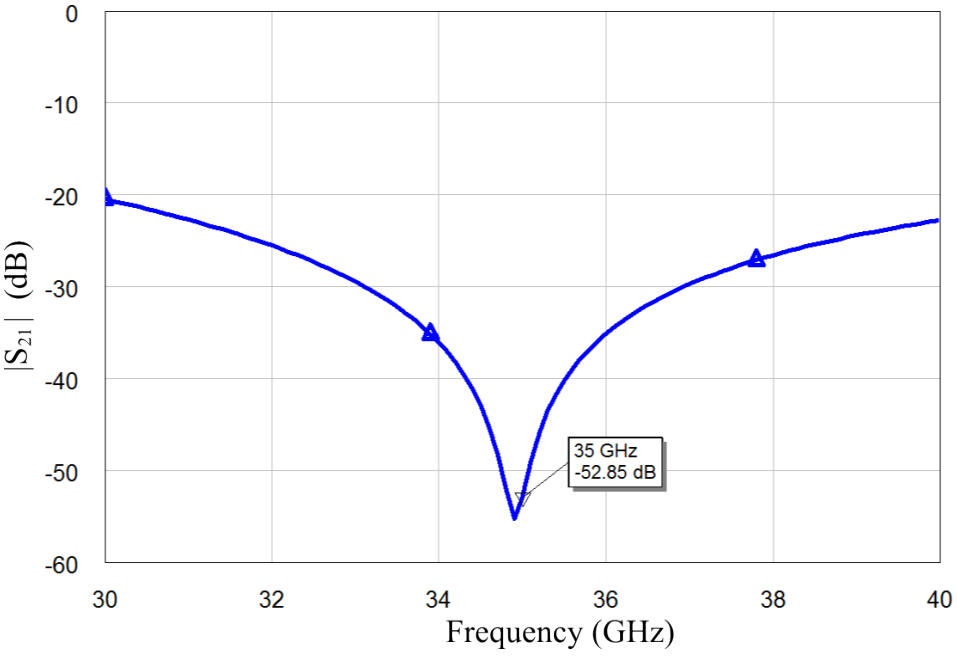
Table 2.4: Expected characteristics of the designed capacitive contact RF-MEMS switch.

CHARACTERISTIC	VALUE (dB)
Isolation	52.85
Insertion loss	0.26
Return loss	31.6

Proposed switch is different than the switch designs in [10]. In this design, four recesses are introduced next to the anchors of the bridge. These recesses are used for inductive tuning of the switch. In other words, they are responsible for tuning the isolation characteristic of the switch and obtaining maximum isolation at the desired frequency. Also with this improved design, controlling the bridge length is targeted for both decreasing the pull-in voltage of the switch and minimizing the vertical bending in the bridge.



(a)



(b)

Figure 2.9: Expected (a) insertion, return losses and (b) isolation characteristics of the designed capacitive contact RF-MEMS switch.

2.2.4.1 Mechanical Analysis of the RF-MEMS Switches

Fixed-fixed beams, i.e. switches, used in the design do not have a single conductor layer. It is in a multilayer configuration where one conductor layer is placed between two silicon-nitrate layers as can be seen from Figure 2.10. More detailed information about the fabrication will be given in the upcoming sections.

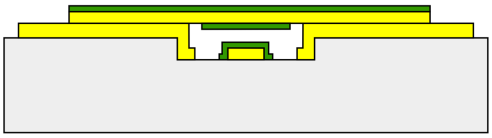


Figure 2.10: Section of a fixed-fixed beam.

If the technology parameters are known, pull-in voltage of a single layer fixed-fixed beam can be estimated with the following equation [27]:

$$V_{PI} = (1 - \gamma_1\gamma_2) \times \sqrt{\frac{4 \times (Ac_{PI} + Bc_{PI}^3) \times \sqrt{h} \times (h - c_{PI})^{3/2}}{\varepsilon_0 \times \left(1 + 0.42 \times \frac{h}{w_{bridge}}\right)}}$$

$$A = 2 \times \left[\frac{\tilde{E}}{3}\left(\frac{\pi}{t_{bridge}}\right)^4 \times \frac{t^3}{4} + \frac{\pi^2}{4lbridge} \times \sigma \times t\right] \tag{2.2}$$

$$B = \frac{\pi^4}{8l_{bridge}^4} \times \tilde{E} \times t$$

$$\gamma_1 = 1.1454 \times \left(1 - 0.8894 \times e^{1.0874\times10^{-2}\times h\times l_{bridge}\times t}\right)$$

$$\gamma_2 = e^{\frac{(\gamma^2)^{0.3115}}{E\times t}\times 4.0552\times10^3\times\left(l_{bridge}-100\times10^{-6}+0.06724\right)}$$

In Equation 2.2, c_{PI} is the central deflection of the beam when pull-in occurs, ε_0 is the permittivity of vacuum, $\tilde{E}$ is the modulus, l_{bridge} is the length, w_{bridge} is the width, t is the thickness, σ is the residual stress along length of the beam, h is the height of the beam from the signal line. As it was stated earlier, fixed-fixed beams used

in the design of the phase shifter have multilayer. That is why Equation 2.2 must be modified. Instead of t, $\tilde{E}$ and σ effective values for these can be calculated and inserted back to the equation. In [27], Equation 2.3 is derived for calculating these effective values for an n-layer fixed-fixed beam which is visualized in Figure 2.11 but they assumed that only the top layer of the beam is conductor while other layers are all dielectric.

$$
\begin{aligned}
t_{eff} &= 2 \times \sqrt{\frac{\sum_{i=1}^{n} \tilde{E}_i w_i \left(Z_i^3 - Z_{i-1}^3\right)}{\sum_{i=1}^{n} \tilde{E}_i w_{bridge_i} t_i}} \\
\sigma_{eff} &= \sum_{i=1}^{n} \frac{\sigma_i t_i w_i}{t_{eff} w_{bridge}} \\
E_{eff} &= \sum_{i=1}^{n} \frac{\tilde{E}_i t_i w_i}{t_{eff} w_{bridge}}
\end{aligned}
\tag{2.3}
$$

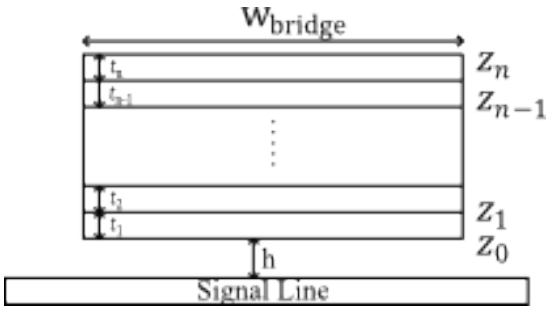


Figure 2.11: Section of an n-layer fixed-fixed beam with different widths of layers.

Assuming that there is no deflection in the beam and using the technology parameters of METU-MEMS Application and Design Center, which are tabulated in Table 2.5, effective thickness, residual stress and modulus are calculated and shown in Table 2.5.

By using these calculated values, pull-in voltage for the switch is estimated as approximately 23 V. It is essential to state one more time that these calculated pull-in values are just estimation and in the used formula, conductor layer is assumed to be at the very top. However, for the switch used in the phase shifter design conductor layer is in the middle.

Table 2.5: Technology parameters, dimensions of the three layers of the fixed-fixed beam and effective Young's Modulus, residual stress and thickness calculated from these values.

Parameters	Layer 1	Layer 2	Layer 3
Young's Modulus ($\tilde{E}$) (GPa)	295	78	295
Residual Stress (σ) (MPa)	30	80	30
Thickness (t) (μm)	0.1	1.0	0.1
Width w_{brdige} (μm)	50	50	50
Effective Young's Modulus ($\tilde{E}_{eff}$) (GPa)	111.7		
Effective Residual Stress (σ_{eff}) (Mpa)	60.2		
Effective Thickness (t_{eff}) (μm)	1.4		

2.2.4.2 Effect of the Switch Dimensions on the Pull-In Voltage

Dimensions of the switch directly affect the pull-in voltage of the switch as it can be seen from Equation 2.2. In order to observe the effect of dimension changes on the pull-in voltage of a switch, various pull-in calculations are done for different switch dimensions. These calculations are tabulated in Table 2.6.

Table 2.6: Calculated pull-in voltages for different switch dimensions.

Dimension	Value (μm)	Pull-In Voltage (V)
wbridge	50	23.2
lbridge	300	
wbridge	100	23.2
lbridge	300	
wbridge	50	33.5
lbridge	100	
wbridge	50	18.9
lbridge	200	

Calculated pull-in voltages in Table 2.6 show that changes in the width of the bridge have no effect on the pull-in voltage. However, changes in the length of the bridge directly affect the pull-in voltage: bridge length and pull-in voltage are inversely proportional. In Chapter 2.2.4, it was stated that recesses are introduced to the switch design in order to control the bridge length. In other words; by changing the recess dimensions, bridge length and correspondingly pull-in voltage can be set to a desired value.

Power handling of a switch is related with the pull-in voltage of that switch: switches with higher pull-in voltages are capable of handling more power. However, increasing the pull-in voltage decreases the life time of a switch due to the failure based on charging effect. So it can be summarized as follows: increasing the bridge length of a switch increases the pull-in voltage and power handling of the switch whereas it decreases the life time of the switch.

2.2.5 Expected Results of the SPDT Switch

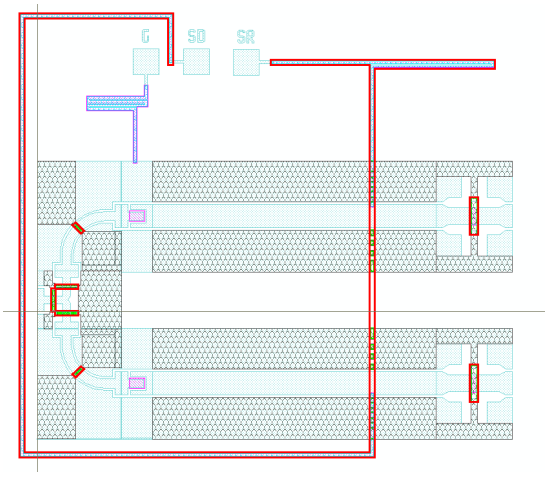
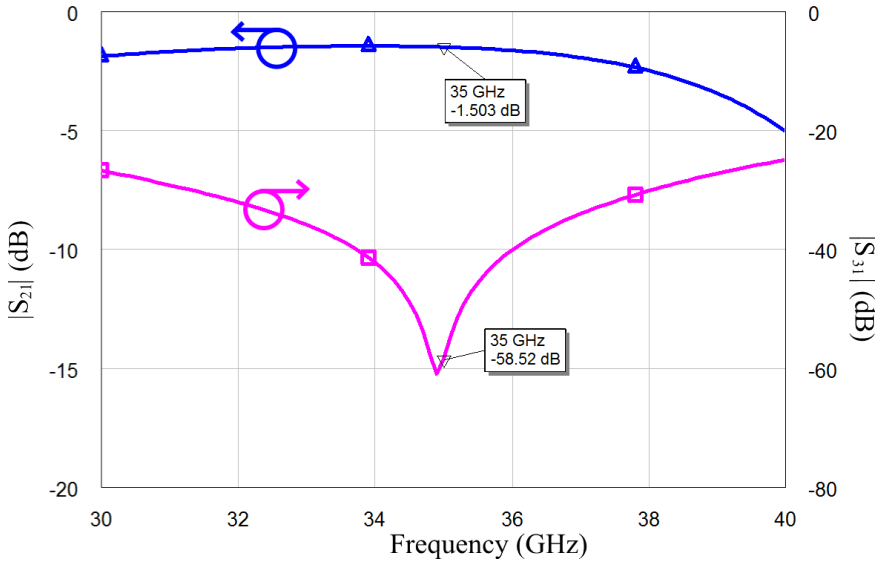


Figure 2.12: Layout of the designed SPDT switch from the wafer.

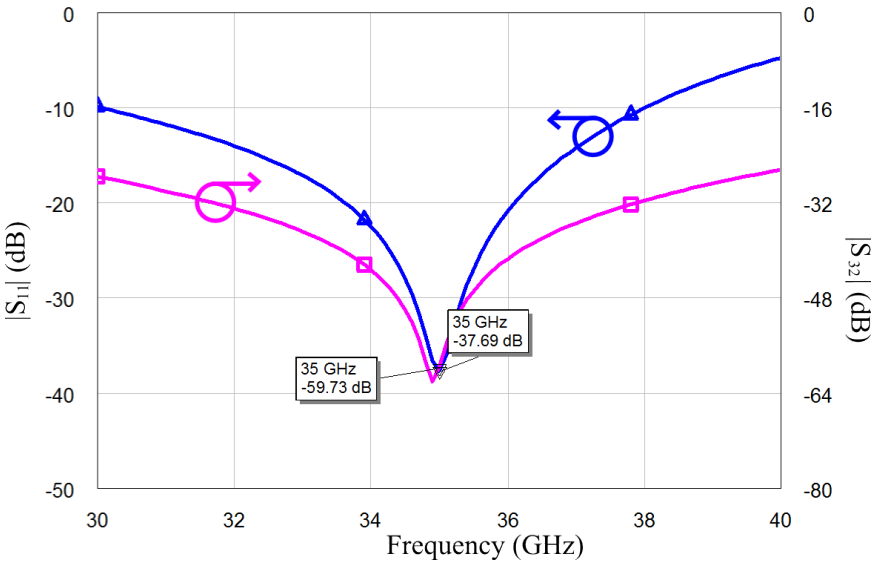
The performance of the SPDT switch is simulated in NI Microwave Office AWR Design Environment by cascading individual S-parameters of each building block presented in the earlier sections. Figure 2.13 shows the obtained simulation results.

One observes from Figure 2.13b that the designed SPDT switch exhibits a tuned

performance at 35 GHz owing to the limited isolation bandwidth of the RF-MEMS switch elements and quarter-wave transmission line sections (for translating the virtual short impedance of the switch elements at down-state to an open circuit). In particular, the switch provides 37 dB return loss, 1.5 dB insertion loss and 58 dB isolation at 35 GHz. According to 20 dB return loss and 30 dB isolation criteria, the bandwidth around 35 GHz is limited to 2.5 GHz and 7.5 GHz respectively.



(a)



(b)

Figure 2.13: $|S_{i1}|$ of the designed SPDT switch.

2.3 Expected Results of the Overall Phase Shifter

After completing the design and obtaining expected results of SPDT switch, overall 3-bit switch-line phase shifter design is started. As it is stated in the Introduction section of this chapter, each bit of the phase shifter consists of two SPDT switches connected back-to-back and two transmission lines with different lengths on the two branches of the SPDT switches as it can be seen from Figure 2.14.

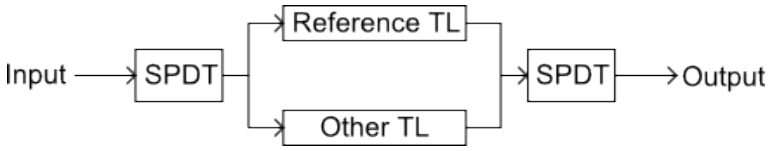


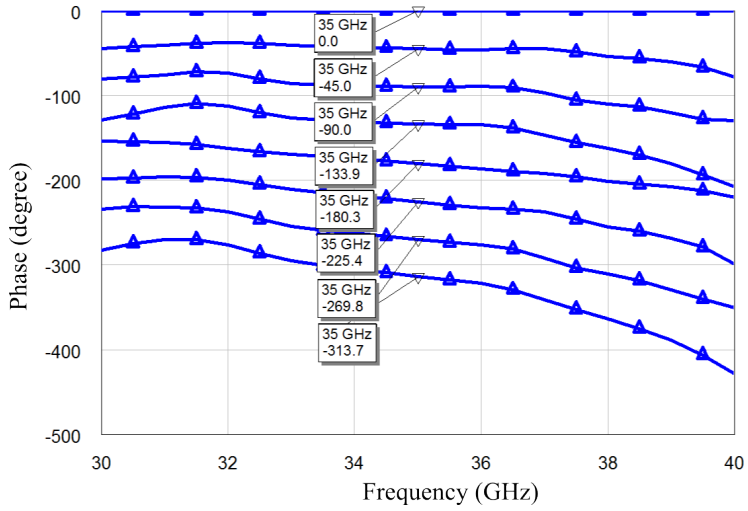
Figure 2.14: Illustration of one of the bits of the switch-line phase shifter.

As the reference transmission line, CPW with length 100 μm is chosen for all of the bits. In order to find length differences of the transmission lines for all three bits, iterative simulations are held in NI AWR. With the help of these simulations, necessary length differences are found and tabulated in Table 2.7.

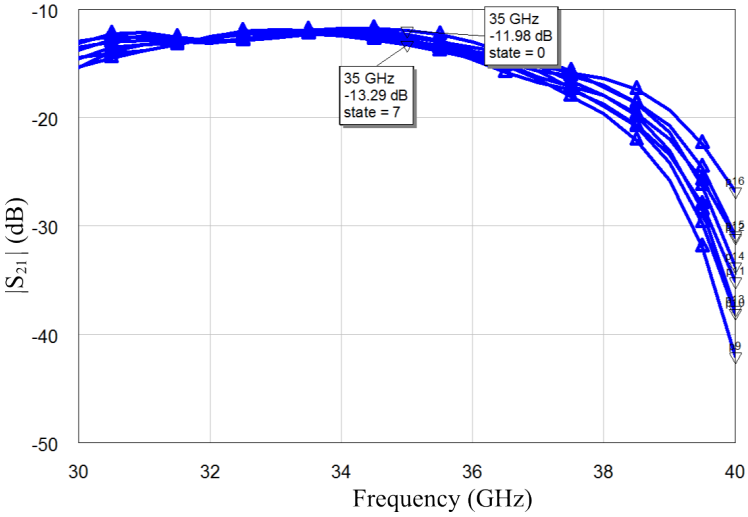
Table 2.7: Transmission line differences for all of the bits of the 3-bit switch-line phase shifter.

Bit	Length Difference (μm)
Bit 0	755
Bit 1	1410
Bit 2	2704

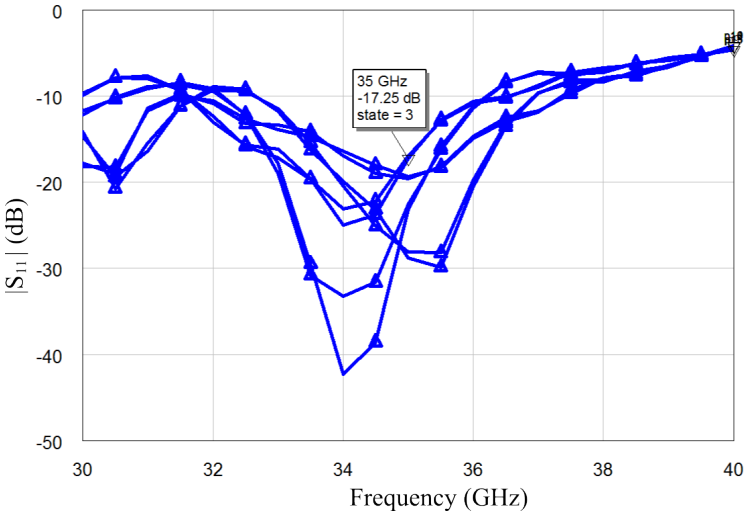
According to the simulation results, which are shown in Figure 2.15, for the worst case expected insertion and return losses are 13.3 dB and 17.25 dB respectively. For the return loss, there is approximately 1.6 GHz bandwidth around 35 GHz if 15 dB return loss is the limit. Bit error of the overall phase shifter is expected to be better than 0.8 % at 35 GHz according to the phase performance of the phase shifter which is shown in Figure 2.15a. From the same figure, true-time delay characteristic of the designed phase shifter also can be seen in 32-36.5 GHz band. Furthermore, with this switch-line design, 4.65 GHz bandwidth can be defined at 35 GHz center frequency for an operation with maximum 10 % phase error.



(a)



(b)



(c)

Figure 2.15: Expected (a) phase performance and (b), (c) $|S_{i1}|$ of the designed 3-bit switch-line phase shifter.

2.4 Fabrication

The phase shifter will be fabricated using an in-house surface micromachining processes developed at METU-MEMS Research and Application Center. Figure 2.16 presents a summary of the flow of the phase shifter fabrication process. A silicon and a glass wafers are required for the phase shifter fabrication. Firstly, a Si_xN_y layer is deposited on the silicon wafer, followed by a Au sputtering process. Afterwards, a second Si_xN_y layer is deposited and all of the layers are patterned to obtain MEMS bridges. Secondly, the glass wafers are etched to form 1.3 μm deep recesses. Then, Cr-Au layers are sputtered and patterned to obtain CPW traces. As a final step a Si_xN_y layer is deposited and patterned to have a dielectric layer under the MEMS bridge. Then the silicon and glass wafers are bonded by a Au-Au thermocompression bonding. The silicon wafer is etched away following the bonding step. At this step the RF MEMS bridges are formed and suspended. This process flow is slightly changed version of the flow presented in [28].

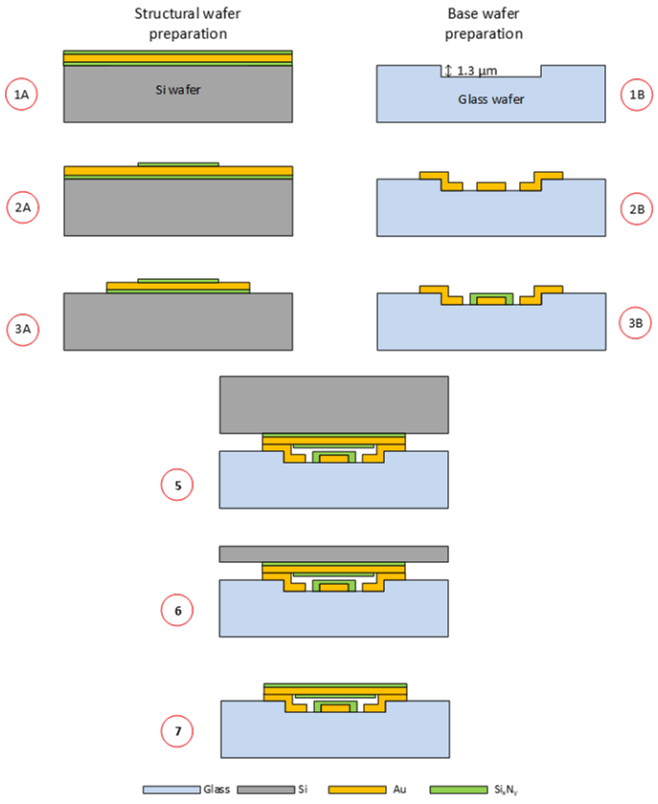
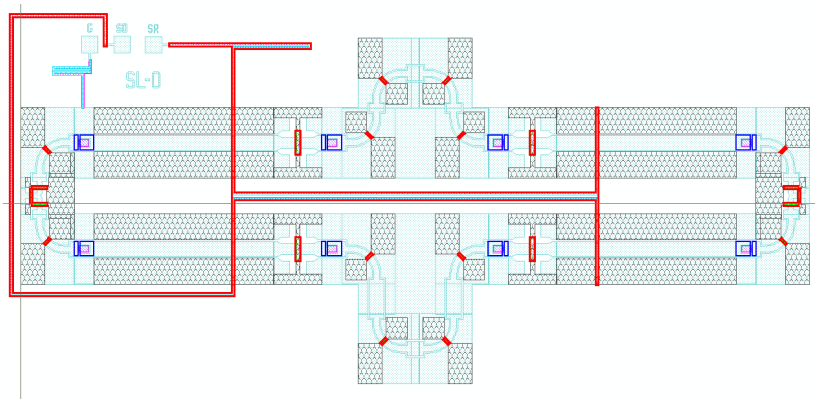
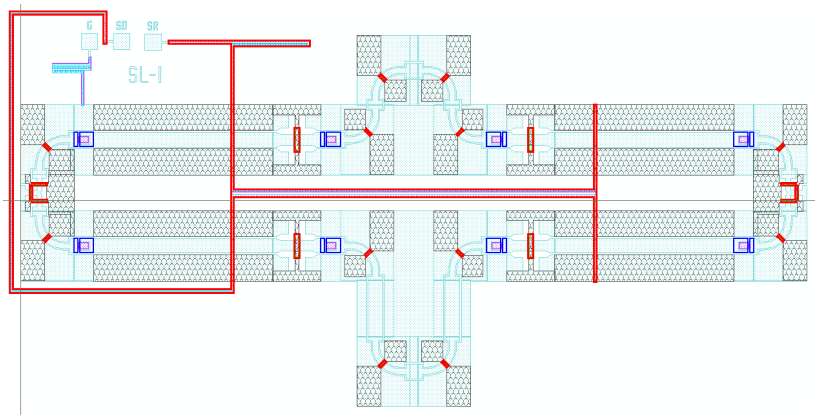


Figure 2.16: Schematic description of the fabrication process.

Designed 3-bit switch-line phase shifter has not fabricated yet. However, layouts are prepared and sent to METU-MEMS Research and Application Center. Layouts of the all bits are shared in Figure 2.17.



(a)



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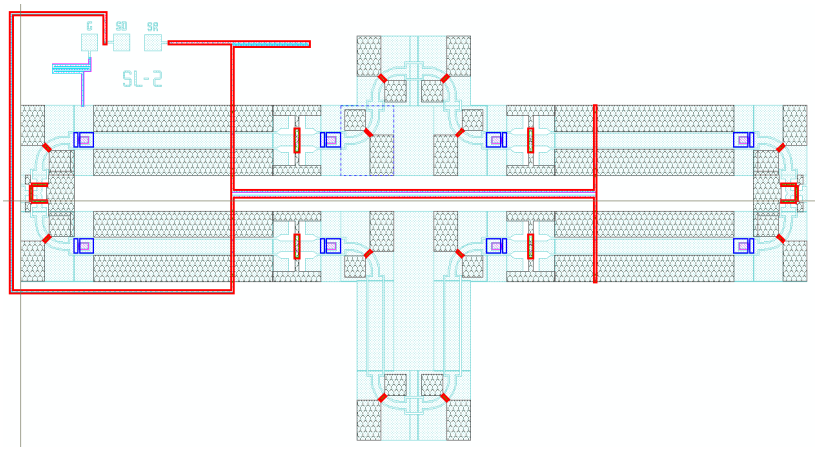
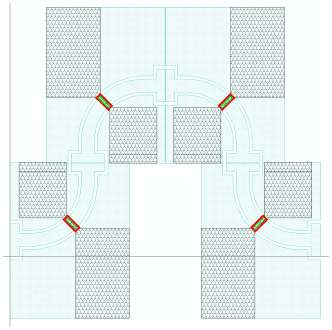


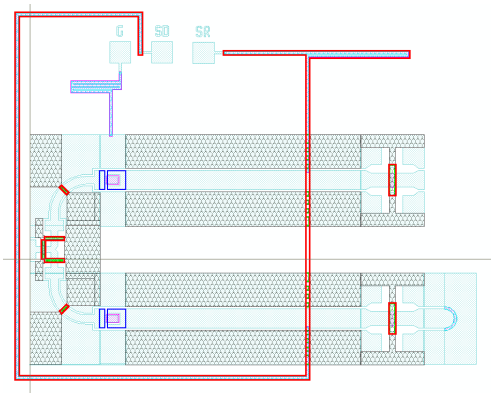
(c)

Figure 2.17: Layouts of the (a) first, (b) second and (c) third bits of the designed switch-line phase shifter.

After fabrication; if there is a mismatch between the expected and measured results, some test structures are designed and placed to the wafer in order to back-process the reason of the failure. Some of these structures are given in Figure 2.18.



(a)



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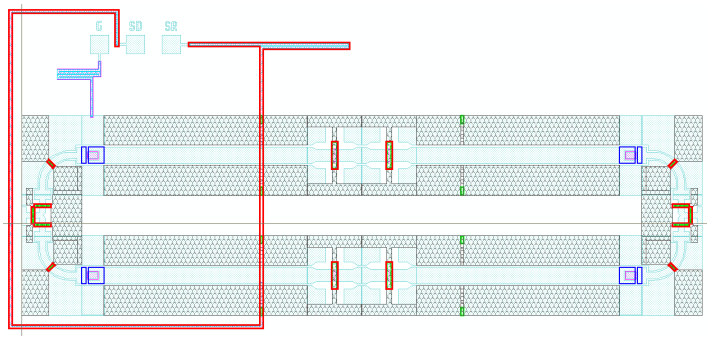


(c)

Figure 2.18: Layouts of (a) CWP bend test structure, (b) one port terminated with match load SPDT switch and (c) two SPDT switches cascaded back-to-back.

2.5 Conclusion

For RF-MEMS phase shifter design, switch-line phase shifter topology is chosen in the first place because of its minimum number of switches compared to other digital phase shifters considered. By this way dependency of electrical performance on the fabrication is aimed to be minimized. However in the final stage, after optimizing each building block, expected insertion loss is observed to be too much. According to the simulation results, 13.3 dB insertion loss is expected which makes this design unfavourable. This much of insertion loss also contradicts with the low-loss expectations from the RF-MEMS structures. In any case, in order to use this phase shifter in a transmitter, a gain block is also needed for compensation.

Another drawback of this design is its dimension: length of the 3-bit switch-line phase shifter is in the orders of mm. Other phase shifter topologies, like DMTL phase shifters, can be designed with smaller dimensions.

Besides all of these negative sides, there are superior performance parameters. This phase shifter offers maximum 0.8% bit error at 35 GHz. Furthermore, 4.65 GHz bandwidth can be defined for an operation with maximum 10% phase error.

Using microstrip transmission lines instead of CPW, can decrease both insertion loss and the dimensions of the structure. For example, use of microstrip will eliminate need for air-bridges. This would lead to a lower insertion loss. Also it is easier to bend microstrip lines. So length of the overall design could be minimized by bending the quarter wavelength transmission lines used in the SPDT switch. With the fabrication process discussed in Chapter 2.4, opening and coating vias are not possible. That is why, design is not repeated by using microstrip transmission lines instead of CPW.

In the interest for comparing electrical performance of switch-line phase shifter with an another phase shifter topology, a 3-bit DMTL phase shifter is designed. Design procedure and expected results of the design are discussed in the upcoming chapter.

CHAPTER 3

DISTRIBUTED MEMS TRANSMISSION LINE (DMTL) PHASE SHIFTER

3.1 Introduction

Expected insertion loss of the 3-bit switch-line phase shifter discussed in the previous chapter is too much compared to the insertion loss of DMTL phase shifters presented in [29–31]. Because of this, a new 3-bit DMTL phase shifter is designed in order to compare their performances.

In this chapter a novel 3-bit DMTL phase shifter designed for Ka-Band applications is presented. Designed phase shifter has comparable expected results with the ones proposed in [29–31]. This DMTL phase shifter is designed to operate at 35 GHz on a 500 μm thick glass substrate (ε_r=4.6, tanδ=0.015 at 35 GHz) like the one introduced in Chapter 2. In the same way, coplanar waveguide (CPW) structure is used as the transmission medium for the design. This design consists of 3 bits each having different number of capacitive contact, shunt RF MEMS switches, which are going to be called unit cell after this point. Each bit has different unit cells but every unit cells in a bit are identical. By taking the simulation results into consideration, it is decided to have 2 unit cells in the first bit, 4 unit cells in the second bit and 8 unit cells in the third bit.

In the following parts of this chapter, unit cell designs of each bit is investigated deeply. The same fabrication process discussed in Chapter 2.4 is used for this design therefore fabrication process is not discussed in this chapter.

3.2 Design

In order to decrease the burden of the computational work, every unit cell is designed separately using circuit models in National Instruments (NI) AWR Design Environment. Moreover, the number of unit cells in a bit is chosen at this point according to the maximum phase that a unit cell can provide under certain dimension limitations. These dimension limitations are set considering the fabrication limitations.

On the basis of the dimensions found with the simulations held in NI AWR, 3D electromagnetic simulations are performed in Ansys High Frequency Structure Solver (HFSS) for confirming the dimensions. After completing the design of each unit cell in Ansys HFSS, these cells are cascaded for observing the expected overall DMTL phase shifter characteristics.

Design process of the phase shifter is continued with the mechanical analysis and design of the package. More detailed information is given in the following parts.

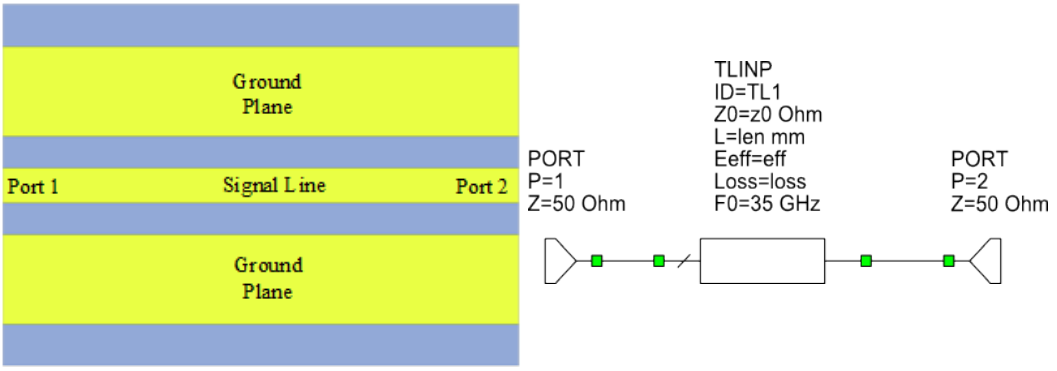
3.2.1 Unit Cell Design

For the transmission line, CPW is used. Dimensions of this CPW is decided before starting the design of the phase shifter. In order to find the optimum dimensions, parametric sweep property of the Ansys HFSS is used and the case with the maximum signal width with the minimum insertion loss is chosen.

Signal width of the chosen CPW is 192 μm while the signal-ground opening is 179 μm. Characteristic impedance and the attenuation constant of the CPW with the given dimensions are 87.1 Ω and 90 dB/m respectively. These values can be obtained with the formulas presented in [25]. Collin's approach does not include radiation loss. In order to find a better approximation for the attenuation constant, 3 CPWs having the same signal width and signal-ground openings but different lengths are simulated in HFSS and then by using these results and the optimization toolbox of the NI AWR, optimizations are performed. 3D model and the black-box model of one of these transmission lines are shown in Figure 3.2.

Line length shown as "len" in Figure 3.1b is kept constant and the other parameters

are used as optimization parameters. According to these simulations, characteristic impedance, attenuation constant and relative effective dielectric constant, which is labeled as "eff" in Figure 3.1b, are found as 87.6 Ω, 160 dB/m and 2.73 respectively.



(a) (b)

Figure 3.1: (a) 3D model and (b) transmission line model of a CWP .

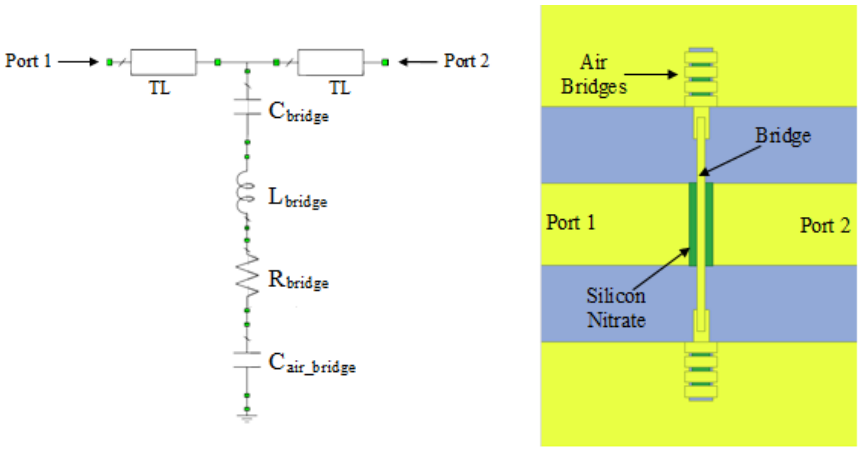
Capacitive contact, shunt RF MEMS switches can be modelled with two transmission lines (TL) and 2 capacitances, 1 inductance, and 1 resistance connected parallel to these TLs as shown in Figure 3.2a [10]. C_{bridge} depends on the state of the bridge and the width of the bridge whereas L_{bridge} and R_{bridge} depends on the type of the conductor and the distance between the anchors. Air bridges are introduced to the nominal switch in order to achieve the necessary up/down ratio for the required angular difference in the S_{21} of the two states by using the fact that air bridges act as extra capacitors (metal-air-metal (MAM) capacitor).

In order to calculate capacitance of the bridge when it is in up-state and the capacitance of the MAM capacitors, following equation is used [32]:

$$C = \varepsilon_0 \left[1.15 \frac{s\, w_{bridge}}{h_{equ}} + 2.8 \left(\frac{s + w_{bridge}}{h_{equ}} \right) \times \left(\frac{t}{h_{equ}} \right)^{0.222} + 4.12\, h_{equ} \left(\frac{t}{h_{equ}} \right)^{0.728} \right] \tag{3.1}$$

$$h_{equ} = h_{bridge} + \frac{t_d}{\varepsilon_r}$$

In Equation 3.1; ε_0 represents the free space permittivity, s represents the signal line



(a) (b)

Figure 3.2: (a) Circuit model and (b) top view of the fixed-fixed beam.

width, w_{bridge} represents the bridge width, t represents the thickness of the conductor, h_{brdige} represents the height of the bridge from the dielectric, t_d represents the thickness of the dielectric under the bridge and ε_e represents the dielectric constant. For the capacitance calculation of the air bridges, w_{bridge} parameter is changed with l_{mam} which represents the overall length of the MAM capacitor as it can be seen from Figure 3.3.

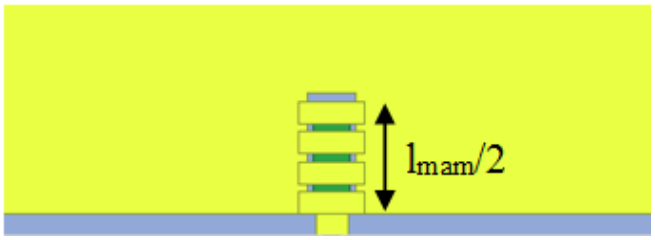


Figure 3.3: Top view of a MAM capacitor in one of the unit cells.

l_{mam} is the overall MAM capacitor length. This capacitor is implemented symmetrically as two capacitors with $l_{mam}/2$ lengths to the two anchors of the fixed-fixed beam. There are 9 μ spacing between the air bridges. Those openings are left intentionally in order to increase the stiffness of the bridges. By this way minimum bending on the bridges is expected after the fabrication. 9 μm is much smaller than the wavelength

at the design frequency. That is why no effect on electrical performance is expected.

Parameters other than w_{bridge} and l_{mam} are kept constant throughout the design. These constant values are tabulated in Table 3.1.

For the calculation of the bridge when it is in down-state, nominal capacitance formula, Equation 3.2, is used.

$$\begin{aligned} C &= \varepsilon \times \frac{\text{Conductor Area}}{\text{Distance Between the Conductors}} \\ \varepsilon &= \varepsilon_0 \times \epsilon_r \times \text{Correction factor} \\ \text{Conductor Area} &= s \times w_{bridge} \\ \text{Distance Between the Conductors} &= t_d \end{aligned} \tag{3.2}$$

When the bridge is in down-state, some air is left between the dielectric and the bridge due to the rough surface of the silicon-nitrate layer. This prevents the perfect contact so that's why a correction factor is needed in Equation 3.2. According to the previous switch fabrication results, that correction factor is found as 0.37 [9].

Inductance and resistance values of the bridge are found from the previous designs of the RF MEMS group in the department. These values are taken as the initial values. Initial values for capacitance values are also calculated for an initial w_{bridge} and l_{mam} values. After assigning an initial value to the TL shown in Figure 3.2a, all of these values are inserted to the circuit constructed in NI AWR and then by using the opti-

Table 3.1: Constant values throughout the DMTL phase shifter design.

Parameters	Values
Characteristic Impedance (Z_0)	87.6 Ω
Attenuation Constant (α)	160 dB/m
Signal Width (W)	192 μm
CPW Slot Width (G)	179 μm
Conductor Thickness (t)	1 μm
Bridge Height (g_0)	1 μm
Dielectric Thickness (t_d)	0.3 μm
Dielectric Constant (ε_r)	7
Free Space Permittivity (ε_0)	8.854×10^{-12} F/m

mization tool box of this program, optimum values are found for w_{bridge}, l_{bridge}, r_{bridge}, l_{mam} and TL length which satisfies the necessary phase shift. Afterwards, 3D simulations of the unit cells are performed with HFSS by using the dimensions found with NI AWR. Obtained simulation results are imported back to NI AWR for observing the overall bit characteristics. It is seen that expected results from the simulations held in NI AWR do not match with the simulation results from HFSS. After back processing, it is seen that the characteristic impedance of the transmission lines in the unit cells are found much higher than the value taken at the very beginning of the design. In order to decrease the overall characteristic impedance of the unit cell, it is decided to increase the capacitance, in other words to load the transmission line more. This can be done in two ways: increasing the bridge width or increasing the MAM capacitor lengths. Increasing the bridge width may cause bending in the bridge. That is why this option is not chosen. By increasing the MAM capacitor lengths, 3D simulations are repeated in HFSS and after a few iterations desired insertion phase characteristics are obtained. Dimensions of each unit cells, before and after the iterations, are tabulated in Table 3.2.

Table 3.2: Dimensions of each unit cells, before and after the iterations

	Unit Cell 0		Unit Cell 1		Unit Cell 2	
Parameter	Before (μm)	After (μm)	Before (μm)	After (μm)	Before (μm)	After (μm)
w_{bridge}	37	37	37	20	20	20
l_{bridge}	400	400	400	400	400	400
l_{mam}	250	334	240	312	214	358
l_{tl}	550	550	607	607	728	728
s	192	192	192	192	192	192
g	179	179	179	179	179	179

3.2.2 Mechanical Analysis of the Fixed-Fixed Beams

For the mechanical analysis of the fixed-fixed beams of the DMTL phase shifter, technology parameters and formulations described in Chapter 2.2.4.1 are used. Assuming that there is no deflection in the beam and using the technology parameters of METU-MEMS Application and Design center, effective thickness, residual stress

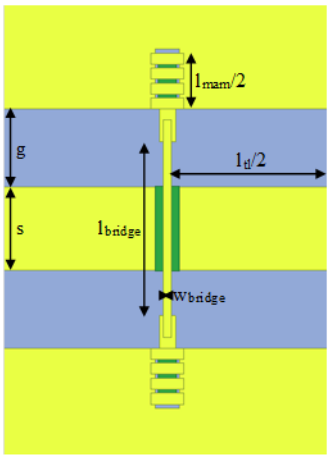


Figure 3.4: Top view of a unit cell.

and modulus are calculated and shown in Table 3.3.

Table 3.3: Dimensions of the three layers of the fixed-fixed beam and effective Young's Modulus, residual stress and thickness calculated from these values.

PARAMETERS	LAYER 1	LAYER 2	LAYER 3
Thickness (t) (μm)	0.1	1.0	0.1
Width w_{brdige} (μm)	37	37	37
Effective Young's Modulus ($\tilde{E}_{eff}$) (GPa)	111.7		
Effective Residual Stress (σ_{eff}) (Mpa)	60.2		
Effective Thickness (t_{eff}) (μm)	1.4		

From these calculated values, pull-in voltages for 3 different fixed-fixed beams are estimated. It is essential to state one more time that these calculated pull-in values are just estimation and in the utilized formulation, conductor layer is assumed to be at the very top. However, for the switches used in the phase shifter design conductor layer is in the middle. Estimated pull-in voltages for 3 different fixed-fixed beams used in the unit cells are tabulated in Table 3.4.

Table 3.4: Estimated pull-in voltages for the 3 switches used in the unit cells.

Switch Number	Pull-In Voltage (V)
Switch ♯1	16.4
Switch ♯2	16.4
Switch ♯3	16.4

3.3 Fabrication

The phase shifters are planned to be fabricated using an in-house surface micromachining processes developed at METU-MEMS Research and Application Center. More detailed information about the fabrication is given in Chapter 2.4.

Designed phase shifters have not been fabricated yet but their mask sets for production are prepared and produced in METU-MEMS Research and Application Center. Layouts of the first, second, third bits and the overall DMTL phase shifter are presented in 3.5 - 3.8.

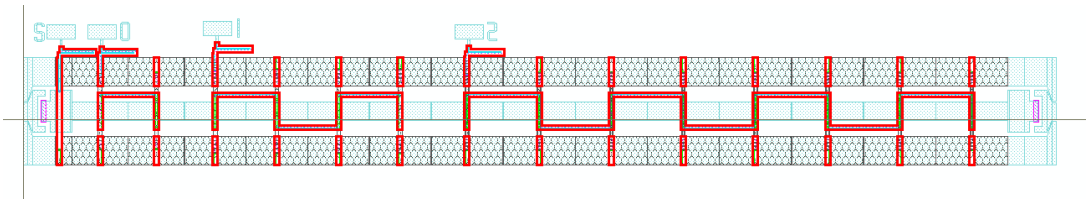


Figure 3.5: Layout of the overall 3 bit DMTL phase shifter.

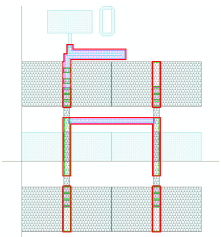


Figure 3.6: Layout of the first bit of the DMTL phase shifter.

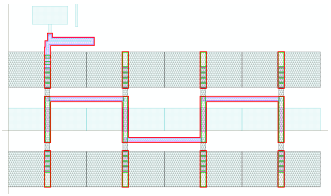


Figure 3.7: Layout of the second bit of the DMTL phase shifter.

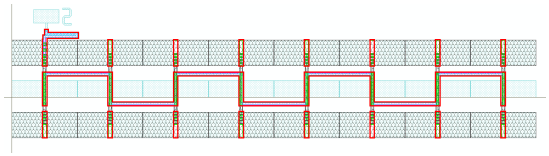


Figure 3.8: Layout of the third bit of the DMTL phase shifter.

3.4 Expected Results

Demonstration of the designed 3-bit phase shifter is shown in Figure 3.9. The cascaded 3D electromagnetic simulation results of the unit cells are inside the black boxes labelled as “Bit 0”, “Bit 1” and “Bit 2”. After connecting every designed part, expected phase characteristics are obtained and shown in Figure 3.10. From Figure 3.10, it can be seen that the maximum expected phase error is around 1.3% at 35 GHz. Expected insertion loss and return loss for all of the states are visualized in Figure 3.11. From those graphs, at 35 GHz maximum expected insertion loss is 3.7 dB. Furthermore, designed DMTL phase shifter offers maximum return loss around 14 dB which means only 4 % of the incident power returns.

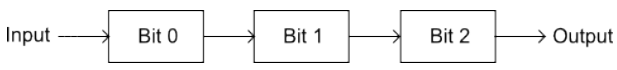


Figure 3.9: Black box model of the 3-bit DMTL phase shifter.

True time-delay characteristics of the DMTL phase shifter can be seen from Figure 3.10. On the basis of this characteristics, 2.69 GHz bandwidth can be defined for an operation with maximum 10% phase error at 35 GHz center frequency.

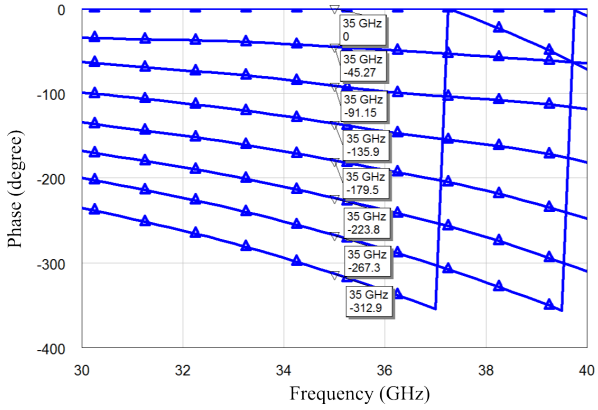
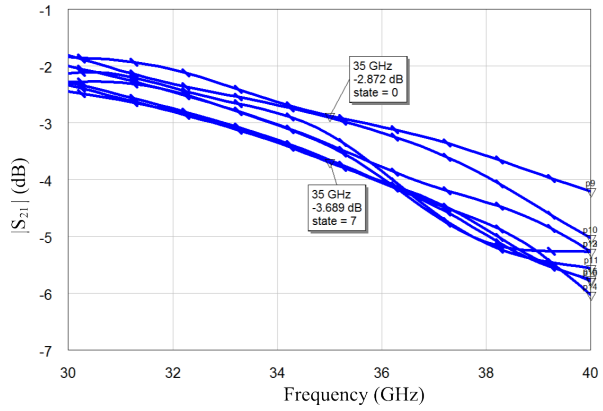
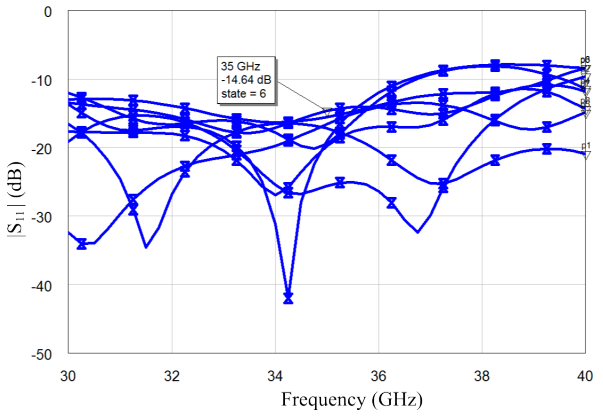


Figure 3.10: Expected phase characteristic of the designed 3-bit DMTL phase shifter.



(a)



(b)

Figure 3.11: Expected (a) insertion and (b) return loss characteristics of the designed 3 bit DMTL phase shifter.

3.5 Conclusion

In this chapter design of a 3-bit DMTL phase shifter is presented. For this phase shifter, capacitive contact, parallel RF-MEMS switches are utilized for loading the transmission line. The transmission lines are CPW. Consecutive design steps are perfomed in NI AWR and Ansys HFSS. This methodology and the individual steps are discussed in detail in the previous sections. Fabrication steps are also discussed.

According to the simulation results, expected pull-in voltages for the RF-MEMS switches are below 20 V. Furthermore, expected insertion loss is better than 3.7 dB whereas expected return loss is better than 14 dB. With these expected results, maximum expected phase error is 1.3% at 35 GHz.

This design has not been fabricated yet but mask layouts of the individual bits and the overall 3-bit phase shifter are prepared and sent to the METU-MEMS Research and Application Center.

On the basis of the simulation results, it is seen that this DMTL phase shifter offers a better performance in terms of insertion loss and pull-in voltages compared to the switch-line phase shifter discussed in Chapter 2. Both DMTL and switch-line phase shifters are examples of true time delay phase shifters.

For comparing these phase shifter topologies with an another transmission type shifter, a 3-bit triple stub phase shifter is designed. Details of this design is discussed in the following chapter.

CHAPTER 4

TRIPLE STUB PHASE SHIFTER

4.1 Introduction

In the previous chapters, design of two 3-bit true time-delay phase shifters, which are switch-line and DMTL phase shifters, are investigated. In order to compare true time-delay phase shifters' performances with another transmission type phase shifter, a 3-bit triple stub phase shifter is designed at 35 GHz.

Using stubs for loading a transmission line and designing a phase shifters is prevalent. There are mainly two types of applications: In the first one, stubs are mainly used in a switch-line phase shifter topology for loading one of the transmission lines [21]. In the other application stubs with switches, which are responsible for changing the effective length of the stubs, are connected series to the propagation path [33] are used. In [34] and [35] Dr. Unlu proposes phase shifter applications of a triple stub topology. It was demonstrated that with 32 control bits, 10° phase resolution, which corresponds to 5-bit, with 0.64° phase error can be achieved. However, that much number of control bits is not feasible for implementation.

In this chapter design of a 3-bit triple stub phase shifter is discussed on the basis of [34] and [35]. 3-bit is chosen in order to decrease the number of control bits. Also the other designs discussed in the previous chapters are also 3-bit. Design is limited with the development of a MATLAB script in order to find the necessary stub lengths and the solution of this script. 3D modelling of this phase shifter is not completed and it is left as a future work.

4.2 Design

Triple stub circuit topology is actually nothing but an extension of the conventional double stub loaded-line phase shifter. This topology, which is pictured in Figure 4.1, is very well known for its ability for making impedance transformation theoretically to any impedance. This transformation comes up with infinitely many solutions. In other words, input impedance of the port 1 or 2 can be transformed to any impedance by changing the stub lengths. With two different length sets, differential phase shift could be obtained.

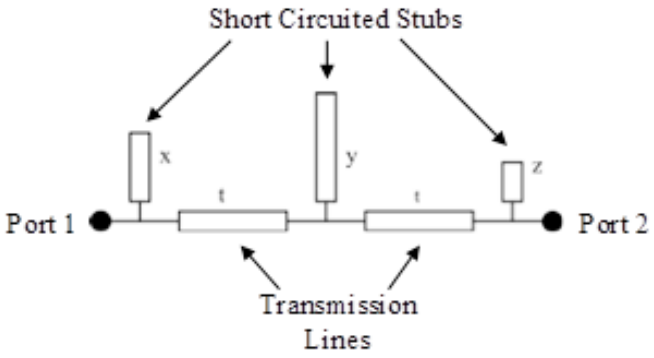


Figure 4.1: Schematic of the triple stub topology where x, y, z and t are the corresponding lengths.

In order to design a 3-bit phase shifter with the circuit schematic shown in Figure 4.1, S-parameters of the overall structure is needed. For easing the calculations, ABCD parameters of the triple stub topology is found in the first place. From the calculated ABCD parameters, S-parameters are calculated by using the necessary transformations.

In the upcoming section, ABCD parameter calculation and S-parameter extraction from the ABCD parameters are investigated deeply.

4.2.1 ABCD and S-Parameter Calculation of the Triple Stub Circuit Topology

For the first step of the design, type of the transmission line is chosen as CPW since with the fabrication process discussed in Chapter 2.4, fabrication of microstrip transmission line is not possible. Reason for this restriction is discussed in Chapter 2.5.

ABCD parameter calculation of the triple stub circuit topology starts with calculating the ABCD parameters of each individual short circuited stubs and the transmission lines between the stubs.

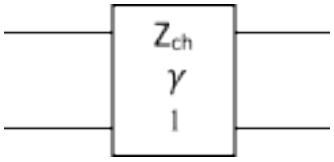


Figure 4.2: Schematic a two port transmission line with characteristic impedance Z_{ch}, propagation constant γ and length l.

ABCD parameter of a two port transmission line with characteristic impedance Z_{ch}, propagation constant γ and length l can be represented as follows:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} cosh(\gamma l) & Z_{ch} \times sinh(\gamma l) \\ \frac{sinh(\gamma l)}{Z_{ch}} & cosh(\gamma l) \end{bmatrix}$$

If an unknown load with impedance Z_L is connected to one of the ports of these transmission line as shown in Figure 4.3, input impedance can be represented as Equation 4.1.

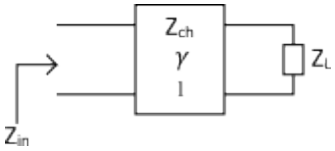


Figure 4.3: Schematic an unknown load with impedance Z_L is connected to one of the ports a transmission line.

$$Z_{in} = Z_{ch} \times \frac{Z_L + Z_{ch} \times tanh(\gamma l)}{Z_{ch} + Z_L \times tanh(\gamma l)} \tag{4.1}$$

Input impedance of the short circuited stubs with lengths x, y and z shown in Figure 4.1 are calculated with Formula 4.1 by equating Z_L to zero since they are short circuited. Calculated input impedances are tabulated in Table 4.1.

Table 4.1: Input impedances of the short circuited stubs shown in Figure 4.1.

Stub	Input Impedance (Z_{in})
x	$Z_{in,x} = Z_{ch} \times tanh(\gamma x)$
y	$Z_{in,y} = Z_{ch} \times tanh(\gamma y)$
z	$Z_{in,z} = Z_{ch} \times tanh(\gamma z)$

If a load with impedance Z is connected in parallel as shown in Figure 4.4, ABCD parameter of the system can be expressed as follows:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \frac{1}{Z} & 1 \end{bmatrix}$$

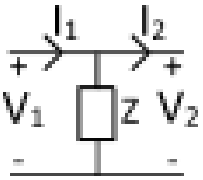


Figure 4.4: Schematic of a load with impedance Z parallel connected to a transmission line.

After calculating the ABCD parameters of each short circuited stubs and transmission lines between them, ABCD parameter of the overall triple stub topology is calculated by multiplying previous matrices. Insertion loss/phase and return loss are the main concerns of 3-bit triple stub phase shifter. That is why only S_{11} and S_{21} are computed with Equations 4.2, 4.3.

$$S_{11} = \frac{A + \frac{B}{Z_0} - C \times Z_0 - D}{A + \frac{B}{Z_0} + C \times Z_0 + D} \tag{4.2}$$

$$S_{21} = \frac{2}{A + \frac{B}{Z_0} + C \times Z_0 + D} \tag{4.3}$$

4.2.2 Search Algorithm

Search algorithm is a totally automatized MATLAB script. Script accepts operating frequency, insertion and return loss limits from the user. Then scripts initiates initial lengths for the short circuited stubs while obeying insertion and return loss criteria and it calculates S-parameters from ABCD parameters of the triple stub circuit topology using the formulas discussed in the previous subsection. In order to decrease computational work, length of the transmission lines between the stubs kept constant at $\lambda/5$. With predefined steps script searches for the necessary stub lengths for 45° phase resolution assuming that maximum stub length is $\lambda/2$. Reason for this can be explained with Smith Chart: take into considerations the two impedances with same magnitudes but opposite phases shown in Figure 4.5.

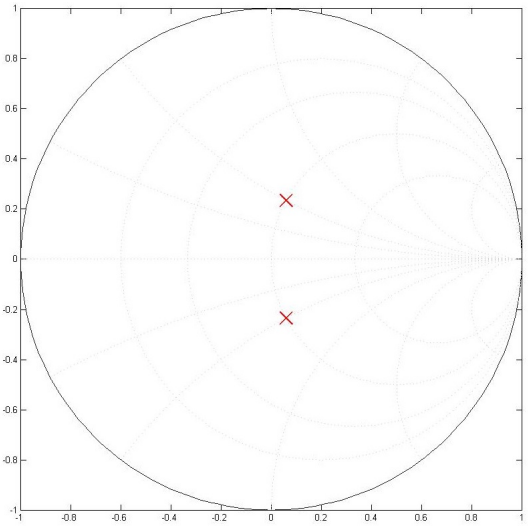


Figure 4.5: Two impedances with same magnitudes but different phases shown on a Smith Chart.

These two impedances have same phase but one of them is lagging and the other one is leading. Accepting that only absolute phases of the input impedance of the stubs are important for the design of the phase shifter, these two impedances are same in terms of their phases. That is why maximum stub length is taken as $\lambda/2$ at the center frequency.

Outcomes of the search algorithm are the reference case stub lengths and stub lengths corresponding to 45° phase resolution for all of the reference cases.

4.2.3 Processing the Outcomes of the Search Algorithm

Obtained reference stub lengths and corresponding stub lengths for necessary phase resolution are analysed with an another MATLAB script in order to find the optimum solution set. With optimum solution set, minimum number of control bits is implied. According to the result of the new script, with combination of 7 different lengths for first stub, 5 different lengths for second stub and 7 different lengths for third stub, which equals to 16 controls, a 3-bit triple stub phase shifter can be designed.

Expected phase performance of the designed triple stub phase shifter with 16 controls is shown Figure 4.6. According to these results, maximum expected phase error is approximately 3.55 % at 35 GHz. In the search algorithm, maximum phase error is set as 5 %. So this results prove the success of the search algorithm. For an operation with maximum 10 % phase error, 0.12 GHz bandwidth can be defined around 35 GHz on the basis of the expected phase characteristic of the triple stub phase shifter.

Triple stub phase shifter is not a true time-delay phase shifter as it was stated before. This can be also seen from Figure 4.6 since in the given graph, there is no constant slope area.

Expected return loss of the designed phase shifter is shared in Figure 4.7. According to these results, for the worst case expected maximum return loss is 17.7 dB. Expected insertion loss characteristic of the designed phase shifter is not given since during the design procedure transmission lines are assumed to be lossless. In other word, propagation constant (γ) is purely imaginary. Inserting loss to the design will not effect the phase characteristic of the design so much. If an effect is observed, it can be eliminated during the 3D electromagnetic design of the phase shifter.

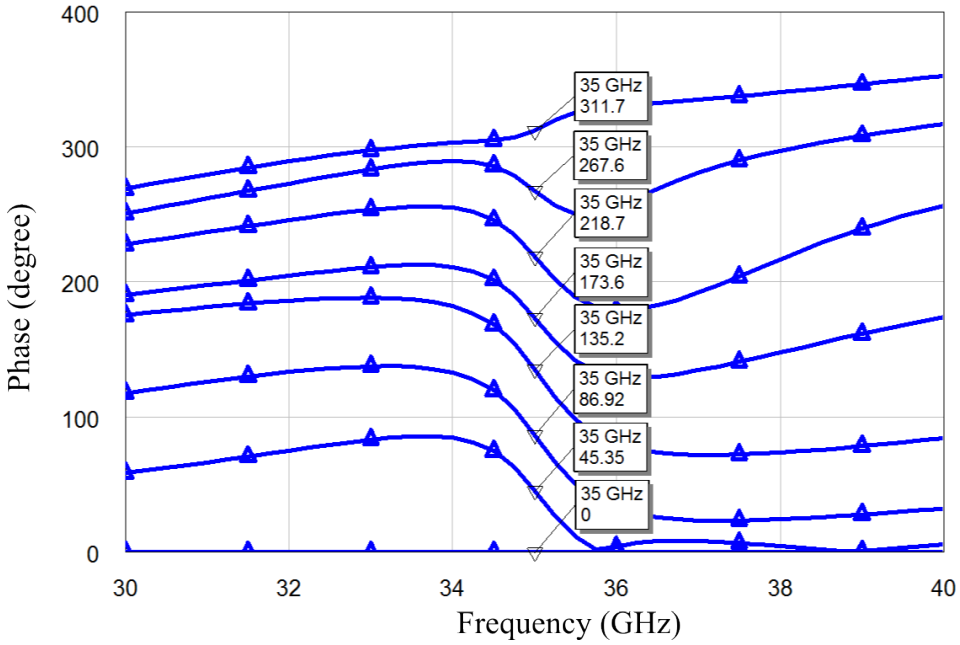


Figure 4.6: Expected phase characteristic of the designed 3-bit triple stub phase shifter.

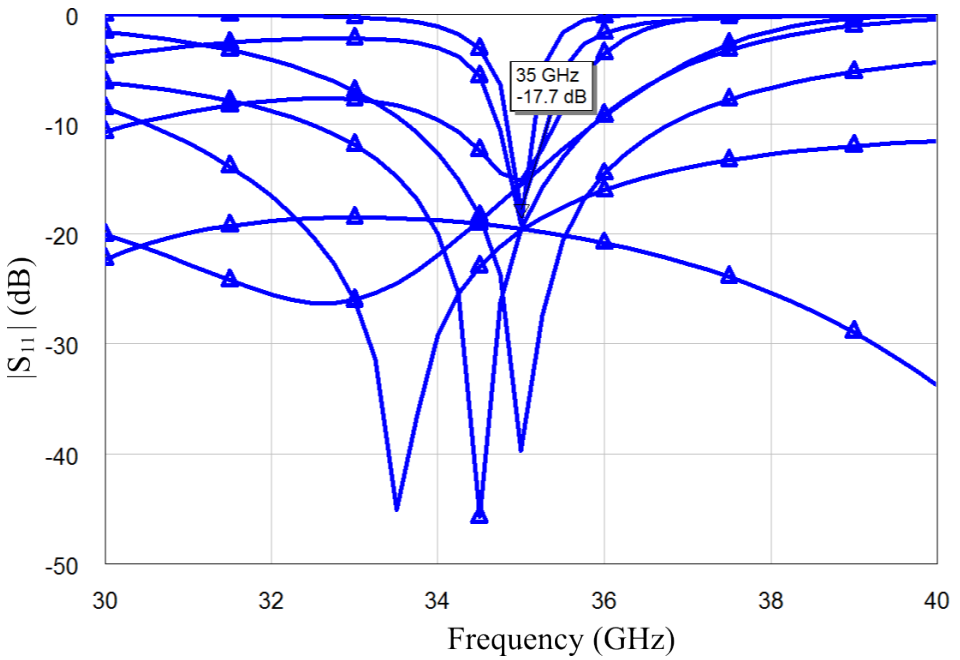


Figure 4.7: Expected return loss characteristic of the designed 3-bit triple stub phase shifter.

4.3 Conclusion

In this chapter, mathematical design of a 3-bit triple stub phase shifter at 35 GHz is discussed. For the design a MATLAB script is written. This script accepts frequency, insertion and return loss limits from the user and computes reference stub lengths and stub lengths needed for 45° phase resolution for these reference cases. Then with an another MATLAB script, outcomes of the previous script is investigated and the case which needs minimum number of control is chosen.

According to the results of the MATLAB scripts if the lengths of the transmission lines between the stubs are fixed to $\lambda/5$ at the design frequency, with 16 control bits triple stub phase shifter which has 45° phase resolution can be obtained. For control unit, capacitive contact RF-MEMS switches which are similar to the ones discussed in Chapter 2.2.4 will be used. Expected results show that design offers 17.7 dB return loss and 3.55 % phase error at 35 GHz. In terms of phase error, this design is behind the design presented in [34] but still 0.12 GHz bandwidth can be defined at 35 GHz center frequency for an operation with maximum 10 % phase error. Expected insertion loss characteristic of the design is not shared since during the design, transmission lines are assumed to be lossless. If an effect of loss on the phase characteristic is observed, it can be eliminated during the design of the building blocks by changing the transmission lengths.

Design has not been finalized yet. Transmission line, T-junction, RF-MEMS capacitive contact switch designs and fabrication are left as future work.

CHAPTER 5

CONCLUSION

In this thesis, 3-bit switch-line, DMTL and triple stub RF-MEMS phase shifter designs are introduced, investigated, and compared.

For the switch-line phase shifter main motivation is to use minimum number of air-bridges. During the design of the SPDT switches, this motivation is watched over. In order to decrease the number of the air-bridges, a novel T-junction is designed with a "T" shaped bridge. After finalizing the electromagnetic simulations of the T-junction, area of the bridge is calculated approximately as 17634 μm^2. According to the experience obtained by the previous fabrications done in METU-MEMS Research and Applications Center, it is impossible to release this bridge without any bending. Bending of the air-bridge directly effects the electrical performance of the design. That is why a new T-junction with three air-bridges, like the one proposed in [26], is designed. For the CPW bend design, which is also a part of the SPDT switch design, a structure with one air-bridge located at the middle of the design is used. All of this effort for minimizing the air-bridges is for decreasing the dependency of the electrical performance of the overall phase shifter to the fabrication tolerances and increasing the yield. SPST switch, which is a capacitive contact RF-MEMS switch, is designed with additional recess which are used for inductive tuning. With this improved design, reducing the bridge length is targeted for both decreasing the pull-in voltage of the switch and minimizing the vertical bending in the bridge. According to the expected results, designed 3-bit switch-line phase shifter is well behind the switch-line phase shifters in the literature in terms of loss characteristics. Actually, this situation contradicts with RF-MEMS technology's low-loss characteristic. Reason behind this

situation is the examples in the literature mostly uses microstrip transmission lines as a transmission medium. Due to the reasons discussed in Chapter 2.5, microstrip transmission lines cannot be used in the switch-line phase shifter design discussed in this thesis. Comparing with the switch-line phase shifter implemented with CPW in [36], designed phase shifter has comparable loss and phase characteristics.

For the design of 3-bit DMTL phase shifter, a different procedure than the conventional design procedure is used. Conventional design procedure starts with choosing Bragg frequency, at which power transmission is stopped or in other words at which characteristic impedance equals to zero. Bridge widths are calculated at the end of this procedure so at the end there is a probabailty to have an unfeasible design because of the bridge lengths. Details of this design procedure is discussed in [37]. In the proposed DMTL phase shifter design in Chapter 3, decreasing computational work is aimed and each bit of the phase shifter is designed separately in NI AWR by using the circuit models of the MEMS switches, or unit cells. According to the circuit models obtained,3D electromagnetic simulations of each unit cells are performed in Ansys HFSS. After completing the designs of unit cells, expected results of the cells are exported from Ansys HFSS into NI AWR in order to observe expected phase and loss characteristics of the overall design. Knowing that DMTL phase shifters presented in [29, 30] have package loss which increase the overall insertion loss, it would be better to compare the designed DMTL phase shifter with the one presented in [31]. In terms of phase and loss characteristics, offered DMTL phase shifter design has comparable characteristics with [31] while having less computational work.

Using triple stub circuit topology as a phase shifter is not a new concept [38]. In this thesis a 3-bit triple stub phase shifter is designed with ideal CPWs. For this design, a MATLAB script which computes necessary short circuited stub lengths for 45° phase resolution with respect to the reference cases, which are generated automatically, by calculating first ABCD parameters and then S-parameters of the triple stub topology while regarding the return and insertion loss criterion defined by the user. 3D electromagnetic design of the triple stub phase shifter has not been finalized yet.

5.1 Comparison of the Switch-Line, DMTL and Triple Stub Phase Shifters

High actuation voltage is one of the problems of RF-MEMS technology. Through out the design of the switches used in both switch-line and DMTL phase shifters, keeping pull-in voltages below 25 V is targeted. Pull-in voltage is directly proportional to the length of the bridge. In order to decrease the length of the capacitive contact RF-MEMS switch used in the switch-line phase shifter, additional recesses are introduced to the design as it was discussed earlier. However, for a good isolation, length of the bridge cannot be reduced under a certain value. For the switches used in the DMTL phase shifter, isolation is not an important characteristic so lengths of the bridges can be changed without any lower limit. If the up-down ratio of the switch is not sufficient, additional switch can be inserted series to the other switches. With these considerations, designs are accomplished and the expected pull-in voltages of switches are tabulated in Table 5.1. Freedom in changing the length of the switches used in DMTL phase shifter can also be seen from this table since expected pull-in voltages of the unit cells are lower than the RF-MEMS switch of the switch-line phase shifter. For triple stub phase shifter, switch is not designed. That is why triple stub phase shifter is not included to this part of the comparison.

Table 5.1: Expected pull-in voltages for the switches used in switch-line and DMTL phase shifters.

Switch		Pull-In Voltage (V)
Switch-Line	RF-MEMS Switch	23
DMTL	Unit Cell 0	16.4
	Unit Cell 1	16.4
	Unit Cell 2	16.4

First "M" in MEMS stands for "micro". So topologies designed by MEMS technology must be small. If the dimensions of the switch-line and DMTL phase shifters, which are also tabulated in Table 5.2 are investigated, it can be seen that switch-line phase shifter is beyond being small. Dimension of the DMTL phase shifter is also larger than the conventional phase shifters in the market [39] but still it is smaller approximately 20 times than the switch-line phase shifter.

Table 5.2: Layout dimensions of the switch-line and DMTL phase shifters.

Phase Shifter	Length (mm)	Width (mm)
Switch-Line	40.0622	5.3705
DMTL	11.135	1.5705

After this point, triple stub phase shifter design is included to the comparisons. In terms of number of control bits, switch-line and DMTL phase shifters have equal values which equals to three. However, triple stub phase shifter has 13 control bits as it can be seen from Table 5.3. RF-MEMS phase shifters are driven by a special driver circuit which is specifically designed for this purpose. Since control bits do not drawn any current from the source, in other words there is no power consumption, having 3 or 13 control bits do not have any difference. Having 13 control bits may only have drawback of designing 13 bias lines which also cover a great amount of space in the layout.

Table 5.3: Control bits number of the switch-line and DMTL phase shifters.

Phase Shifter	Number of Control Bits
Switch-Line	3
DMTL	3
Triple Stub	16

For the comparison of electrical performances of the designed phase shifter, Table 5.4 is prepared with the expected results. According to these results, switch-line phase shifter offers the best performance in terms of maximum phase error whereas again switch-line phase shifter has the maximum expected insertion loss for the worst case. DMTL phase shifter offers better insertion loss compared to the switch-line phase shifter. Maximum phase error of the DMTL phase shifter can be decreased during the measurements by increasing the bias voltage since DMTL phase shifter is based on loading the transmission line and increasing bias voltage means increasing the loading of the line. However, if the bias voltage is increased too much, switches can be charged and stucked in down position. Increasing the bias voltage of the switch-line phase shifter switches improves the maximum phase error in a small range since these switches are used for mainly isolation and for the isolation better than 20 dB, there will be no significant change.

Table 5.4: Expected loss and phase characteristics of the switch-line, DMTL and triple stub phase shifters for the worst case.

Characteristics	Switch-Line	DMTL	Triple Stub
Insertion Loss (dB)	13.3	3.7	Not calculated
Return Loss (dB)	17.25	14	17.7
Maximum Phase Error (%)	0.8	1.3	3.55

Triple stub phase shifter cannot be compared with the other phase shifter topologies in terms of insertion loss because of the fact that up to the point triple stub design is carried out, transmission lines are assumed to be lossless. So insertion loss of the design is only caused by the reflection loss.

In order to define a bandwidth for the designed phase shifters, 10 % phase error is chosen as the limit for the frequency performances of these designs. Phase error for 45° state usually determines the maximum phase error of the overall phase shifter. For switch-line, DMTL and triple stub phase shifter designs, bandwidths are calculated from the expected phase performances for 45° and tabulated in Table 5.5.

Table 5.5: Bandwidths of the switch-line, DMTL and triple stub phase shifter for an operation with maximum 10 % phase error.

Phase Shifter	Bandwidth (GHz)
Switch-Line	4.65
DMTL	2.69
Triple Stub	0.12

In the light of these information, DMTL phase shifter is seemed to be the best option for a 3-bit phase shifter designed with MEMS technology since only expected phase error and bandwidth is behind switch-line phase shifter with only little differences. Only point that must be considered for this topology is that the DMTL phase shifter has so many switches and design is so sensitive to the variances in the switches. Because of this, electrical performance depends on the fabrication tolerances which results a decrease in the yield knowing that fabrication is not uniform through out the wafer.

5.2 Future Work

Design of the triple stub phase shifter is not finalized. Transmission line, T-junction, RF-MEMS capacitive contact switch, which is going to be used as control element, designs are left as future work. During the design of the triple stub phase shifter, transmission lines are assumed to be lossless. That is why effect of the loss parameter on the phase characteristics is not known. This effect will investigated as future work.

Layouts of switch-line and DMTL phase shifters' bits are prepared with test structures. Furthermore, they are placed on a 4 inch wafer, which is shown in Figure 5.1, and prepared for fabrication. Designed wafer will be fabricated with a process flow developed by RF-MEMS group. However, due to excessive busyness in METU-MEMS Research and Application Center, fabrication of switch-line and DMTL phase shifters is left as future work.

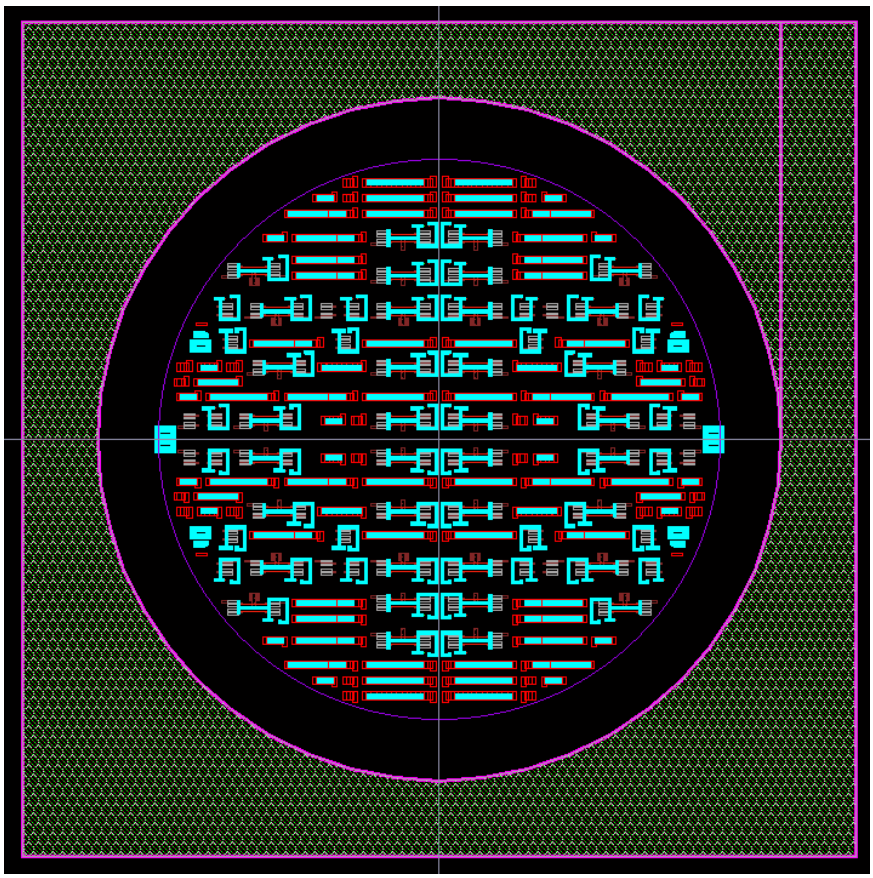


Figure 5.1: Layout of the full 4 inch wafer.

REFERENCES

[1] C. R. Boyd Jr, "A dual-mode latching reciprocal ferrite phase shifter," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 18, no. 12, pp. 1119–1124, 1970.

[2] B. Lax, K. J. Button, and L. M. Roth, "Ferrite phase shifters in rectangular wave guide," *Journal of Applied Physics*, vol. 25, no. 11, pp. 1413–1421, 1954.

[3] F. A. Ghaffar and A. Shamim, "A partially magnetized ferrite ltcc-based siw phase shifter for phased array applications," *Magnetics, IEEE Transactions on*, vol. 51, no. 6, pp. 1–8, 2015.

[4] W. E. Hord, "Microwave and millimeter-wave ferrite phase shifters," *Microw. J*, vol. 32, pp. 81–94, 1989.

[5] Y. Jingshi, "A novel mmic 3 phase-state lc switched-filter phase shifter," Ph.D. dissertation, 2003.

[6] D.-H. Shin, J.-C. Jeong, S.-M. Moon, I.-b. Yom, and D.-W. Kim, "Compact ku-band gaas multifunction chip for satcom phased arrays," in *Microwave Conference (EuMC), 2015 European*. IEEE, 2015, pp. 1471–1474.

[7] E.-Y. Lin, C.-C. Huang, S. Tang, C.-C. Su, and Y.-H. Wang, "A 36 ghz four-bit tunable all-pass phase shifter using 0.15-?? m gaas technology," in *TENCON 2015-2015 IEEE Region 10 Conference*. IEEE, 2015, pp. 1–4.

[8] M.-D. Tsai and A. Natarajan, "60ghz passive and active rf-path phase shifters in silicon," in *Radio Frequency Integrated Circuits Symposium, 2009. RFIC 2009. IEEE*. IEEE, 2009, pp. 223–226.

[9] C. Cetintepe, "Development of mems technology based microwave and millimeter-wave components," *MSc, Electrical-Electronics Eng., Middle East Technical University (METU), Ankara*, 2010.

[10] G. M. Rebeiz, *RF MEMS Theory, Desgin and Technology*. New York: Wiley, 2003.

[11] C.-S. Lin, S.-F. Chang, C.-C. Chang, and Y.-H. Shu, "Design of a reflection-type phase shifter with wide relative phase shift and constant insertion loss," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 55, no. 9, pp. 1862–1868, 2007.

[12] K. Miyaguchi, M. Hieda, K. Nakahara, H. Kurusu, M. Nii, M. Kasahara, T. Takagi, and S. Urasaki, "An ultra-broad-band reflection-type phase-shifter mmic with series and parallel lc circuits," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 49, no. 12, pp. 2446–2452, 2001.

[13] A. Kuzubasli, "Design of an x-band 3-bit rf mems constant phase shifter," *MSc, Electrical-Electronics Eng., Middle East Technical University (METU), Ankara*, 2016.

[14] K. Khoder, M. Le Roy, and A. Pérennec, "An all-pass topology to design a 0–360 continuous phase shifter with low insertion loss and constant differential phase shift," in *Microwave Conference (EuMC), 2014 44th European*. IEEE, 2014, pp. 1556–1559.

[15] S. Omran, M. Rahim, and T. Masri, "Beam-forming network using switch-line phase shifter," in *Applied Electromagnetics, 2007. APACE 2007. Asia-Pacific Conference on*. IEEE, 2007, pp. 1–5.

[16] G. Yang, Z. Ying-bin, B. Lu, and Q. Ran, "Design and modeling of 4-bit mems switched-line phase shifter," in *Electronics, Communications and Control (ICECC), 2011 International Conference on*. IEEE, 2011, pp. 798–801.

[17] P. Anand, S. Sharma, D. Sood, and C. Tripathi, "Design of compact reconfigurable switched line microstrip phase shifters for phased array antenna," in *Emerging Technology Trends in Electronics, Communication and Networking (ET2ECN), 2012 1st International Conference on*. IEEE, 2012, pp. 1–3.

[18] C. Guclu, C. Cetintepe, O. A. Civi, S. Demir, and T. Akin, "35 ghz phased array antenna using dmtl phase shifters," in *2010 10th Mediterranean Microwave Symposium*, 2010.

[19] J. S. Hayden and G. M. Rebeiz, "Very low-loss distributed x-band and ka-band mems phase shifters using metal-air-metal capacitors," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 51, no. 1, pp. 309–314, 2003.

[20] J.-J. Hung, L. Dussopt, and G. M. Rebeiz, "Distributed 2-and 3-bit w-band mems phase shifters on glass substrates," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 52, no. 2, pp. 600–606, 2004.

[21] S.-Y. Eom, "Broadband 180 bit phase shifter using a $\lambda/2$ coupled line and parallel $\lambda/8$ stubs," *Microwave and Wireless Components Letters, IEEE*, vol. 14, no. 5, pp. 228–230, 2004.

[22] C. D. Patel and G. M. Rebeiz, "An rf-mems switch for high-power applications," in *Microwave Symposium Digest (MTT), 2012 IEEE MTT-S International*. IEEE, 2012, pp. 1–3.

[23] B. D. Jensen, Z. Wan, L. Chow, K. Saitou, K. Kurabayashi, and J. L. Volakis, "Integrated electrothermal modeling of rf mems switches for improved power handling capability," in *Wireless Communication Technology, 2003. IEEE Topical Conference on*. IEEE, 2003, pp. 10–11.

[24] H. Sedaghat-Pisheh, R. Mahameed, and G. M. Rebeiz, "Rf mems miniature-switched capacitors with pull-down and pull-up electrodes for high power applications," in *Microwave Symposium Digest (MTT), 2011 IEEE MTT-S International*. IEEE, 2011, pp. 1–4.

[25] R. E. Collin, *Foundations for Microwave Engineering*, 2nd ed. New York: Wiley, 2001.

[26] R. N. Simons, *Coplanar waveguide circuits, components, and systems*. John Wiley & Sons, 2004, vol. 165.

[27] M. Nie, Q.-A. Huang, W. Li, and H. Rong, "An in-situ technique for measuring young's modulus and residual stress of each layer for multi-layer film," in *Solid-State Sensors, Actuators and Microsystems, 2005. Digest of Technical Papers. TRANSDUCERS'05. The 13th International Conference on*, vol. 1. IEEE, 2005, pp. 836–839.

[28] C. Cetintepe, E. S. Topalli, S. Demir, O. A. Civi, and T. Akin, "A fabrication process based on structural layer formation using au–au thermocompression bonding for rf mems capacitive switches and their performance," *International Journal of Microwave and Wireless Technologies*, vol. 6, no. 05, pp. 473–480, 2014.

[29] N. S. Barker and G. M. Rebeiz, "Distributed mems true-time delay phase shifters and wide-band switches," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 46, no. 11, pp. 1881–1890, 1998.

[30] J. Luikui, W. Qun, T. Kai, H. Xunjun, Y. Guohui, and F. Jiahui, "A wafer-scale packaging for rf dmtl phase shifter," in *Microwave Conference, 2008 China-Japan Joint*. IEEE, 2008, pp. 640–643.

[31] S. Dey and S. K. Koul, "10–35-ghz frequency reconfigurable rf mems 5-bit dmtl phase shifter uses push-pull actuation based toggle mechanism," in *Microwave and RF Conference (IMaRC), 2014 IEEE International*. IEEE, 2014, pp. 21–24.

[32] A. K. Goel, *High-Speed VLSI Interconnections*, 2nd ed. New York: Wiley, 2007.

[33] J.-H. Park, H.-T. Kim, W. Choi, Y. Kwon, and Y.-K. Kim, "V-band reflection-type phase shifters using micromachined cpw coupler and rf switches," *Microelectromechanical Systems, Journal of*, vol. 11, no. 6, pp. 808–814, 2002.

[34] M. Unlu, "Novel impedance tuner, phase shifter and vector modulators using rf mems technology," *PhD., Dept. of Electrical and Electronics, Middle East Technical University, Ankara*, 2009.

[35] M. Unlu, S. Demir, and T. Akin, "Triple stub circuit topology as simultaneous insertion phase, amplitude and impedance control circuit for phased array applications," *Microwaves, Antennas & Propagation, IET*, vol. 6, no. 13, pp. 1399–1406, 2012.

[36] Z. Wang, Z. Liu, and X. Li, "A ka-band 3-bit rf mems switched line phase shifter implemented in coplanar waveguide," in *Solid-State and Integrated Circuit Technology (ICSICT), 2010 10th IEEE International Conference on*. IEEE, 2010, pp. 1450–1452.

[37] K. Topalli, Ö. A. Civi, S. Demir, S. Koc, and T. Akin, "A monolithic phased array using 3-bit distributed rf mems phase shifters," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 56, no. 2, pp. 270–277, 2008.

[38] M. Unlu, S. Demir, and T. Akin, "A 15–40-ghz frequency reconfigurable rf mems phase shifter," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 61, no. 8, pp. 2865–2877, 2013.

[39] *TGP2102 Product Data Sheet*, TriQuint Semiconductor, Texas, 5 2008.

[40] *ANSYS Electronics Desktop Online Help*, ANSYS Inc., Canonsburg, PA 15317, 12 2015.

APPENDIX A

USING LUMPED PORT EXCITATION FOR HFSS SIMULATIONS AND ITS EFFECT ON THE SIMULATION RESULTS

Wave port and lumped port excitations are the two most common excitation structures of HFSS. Before simulating the structure constracted in HFSS, excitation structure must be chosen and for this differences between these structures have to be knwon. Wave port represents an external surface from where a signal enters or exits the geometry whereas lumped port represents an internal surface [40]. With wave port, the excitation is applied to a cross-sectional area. On the other hand, with lumped port, the excitation is applied to a point.

There is no certain judgement on which excitation structure gives more accurate results. According to the measurement results of the previous fabrications done in METU-MEMS Research and Application Center, it is seen that expected results obtained by simulations done with lumped port excitation fit measurement results better. That is why all of the simulations discussed in this thesis done with lumped port excitation.

For lumped port excitation of a structure having CPW as a transmission line, a 2D rectangular shape must be created between the signal line and the ground planes. Also the ground planes of the CPW must be connected behind the lumped port. After this point integration line of the port must be specified. An example of a lumped port is shown in Figure A.1 with a red rectangle. There is no specific dimension limits for the conductor part that is combining the two ground planes behind the lumped port. However, setting the width of the conductor too small may disturb the currents

flowing through it and effect the simulation results. Setting the width of the conductor too big has no effect on the simulation in terms of the expected results but since this conductor also will be mashed, computational work will increase. It is seen that setting the width of the conductor to the width of the signal line, which is labelled as s in Figure A.1, is sufficient.

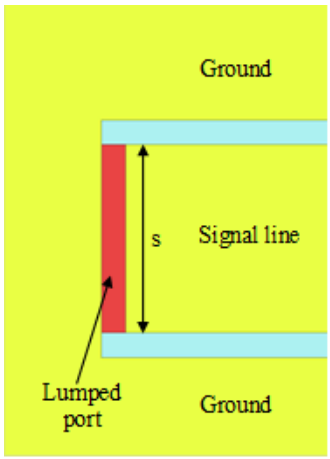


Figure A.1: Schematic of a lumped port excitation.

Another important point that must be regarded for lumped port excitation is the dimensions of the lumped port. Dimension labelled as l of the lumped port shown in Figure A.2 directly equals to the width of the signal line.

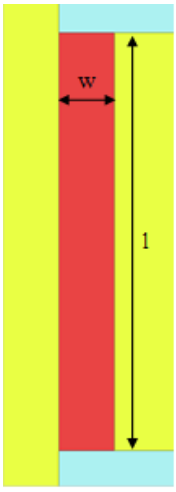


Figure A.2: Dimensions of a lumped port.

Dimension labelled as w of the lumped port shown in Figure A.2 is not constant. Some formulations related to this dimension exist but none of them is certain. Optimum way to find dimension w is to make iterative simulations with a CPW by changing w and examining S_{11} on a Smith Chart. These iterations must be continued until a part of a circle whose center is at the center of the Smith Chart is observed like the one shared in Figure A.3.

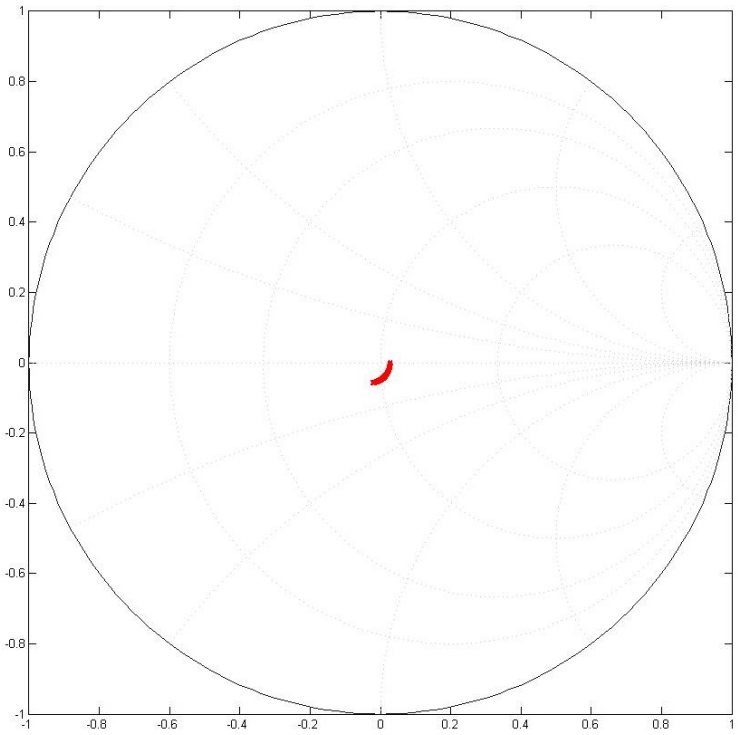


Figure A.3: S_{11} of a CPW simulated with lumped port.

Lumped port is actually a lumped element for exciting the device [40]. So simulations done with lumped port excitation includes the effect of the lumped port. In order to extract this effect, lumped ports are modelled in NI AWR as transmission lines using the procedure discussed in Chapter 3.2.1. Obtained transmission line models are then extracted from the simulation results for obtaining more realistic expected results.