DESIGN AND IMPLEMENTATION OF VARIABLE FREQUENCY SINE WAVE OUTPUT BUCK-BOOST INVERTER

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ABSTRACT

DESIGN AND IMPLEMENTATION OF VARIABLE FREQUENCY SINE WAVE OUTPUT BUCK-BOOST INVERTER

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Conventional inverters have pulse-width-modulated output with a fundamental component at the desired frequency and magnitude. These converters are usually buck type and therefore the DC link voltage limits the maximum 3-phase output voltage magnitude. As a consequence, in motor drive applications field weakening is essential after a certain frequency of operation, as it becomes impossible to preserve the rated flux level. In renewable energy applications similar problems arise. When the DC link voltage falls, the rated output voltage at rated frequency is no longer achievable. Therefore, the energy available cannot be extracted from source. Some techniques are used to increase output voltage such as over-modulation. However over-modulation causes harmonics to increase and different problems arise. Thus there are two important issues to be studied for DC to AC conversion; obtaining sinusoidal output and boosting input voltage. Various studies on this topic are searched and analyzed. A method is proposed, implemented and tested. The results show that proposed method enables operation at rated frequency with THD being lower than 5% even if DC-link voltage is %26 lower than nominal voltage.

Keywords: Buck-Boost Inverter, Sinusoidal Drive, Sine Wave Inverter

ÖZ

DEĞİŞKEN FREKANSLI ÜÇ FAZ SİNUS DALGA ÇIKIŞLI ALÇALTAN-YÜKSELTEN EVİRİCİ TASARIMI VE UYGULANMASI

Şener, Yunus

Yüksek Lisans, Elektrik ve Elektronik Mühendisliği

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Şubat 2016, 209 sayfa

Geleneksel eviriciler çıkışlarında temel frekansı ve genliği elde edecek şekilde darbe genişlik modülasyonu kullanırlar. Bu çeviriciler genellikle "buck" tipindedir ve bu nedenle DC bara gerilimi maksimum 3 faz çıkış gerilimini limitler. Bunun sonucunda, motor sürücü uygulamalarında belli bir frekansın üzerinde manyetik alanın zayıflaması kaçınılmaz olur. Yenilenebilir enerji uygulamalarında da benzer sorunlar gözlenir. DC bara gerilimi düştüğünde anma geriliminde çalışması imkansız hale gelir, bu da enerji olsa bile kullanılamamasına sebep olur. Çıkış gerilimini artırmak için aşırı modülasyon gibi bazı teknikler kullanılmaktadır. Fakat aşırı modülasyon harmoniklerin artmasına sebep olur ve bu da başka sorunlara neden olur. Bu nedenle DC-AC uygulamalarında önemli iki konu bulunmaktadır. Birincisi sinus dalga çıkışı elde etmek, ikincisi ise çıkış gerilimini yükseltebilmektedir. Bu konu üzerine yapılmış olan çalışmalar incelenmiş ve analiz edilmiştir. Bir metod geliştirilip, uygulanmış ve test edilmiştir. Sonuçlar, geliştirilen metodun giriş gerilimi anma değerinden %26 daha düşük olsa bile, çıkışında %5 THD değerinden daha düşük bir seviyede çalışabildiğini göstermektedir.

Anahtar Kelimeler: İndiren-Yükselten Çevirici, Sinüs Sürücü, Sinüs Dalga Evirici

To My Precious Fiancé

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TABLE OF CONTENTS

LIST OF TABLES

TABLES

LIST OF FIGURES

FIGURES

LIST OF ABBREVATIONS

CPLD	(Complex Programmable Logic Device)
ESR	(Equivalent Series Resistance)
IGBT	(Insulated Gate Bipolar Transistor)
IPM	(Intelligent Power Module)
PWM	(Pulse-width Modulation)
PFC	(Power Factor Correction)
RMS	(Root Mean Square)
THD	(Total Harmonic Distortion)
UPD	(Unity Power Factor)
UPS	(Uninterruptable Power Supply)

CHAPTER 1

INTRODUCTION

1.1. Inverters for Variable Frequency Variable Voltage Output

Most of the motors used in industry are AC motors. To control torque and speed of these motors, variable frequency AC source is required. To obtain variable frequency, inverters are used to drive motors. Grid voltage is rectified to obtain DC voltage and inverter is used to obtain AC voltage. Also nowadays, alternative power sources such as solar and wind power are finding widespread application. Solar cells produce DC voltage and inversion is required to connect them to the grid. Wind power sources also require rectification and inversion to connect them to the grid unless they operate as induction generators or synchronous generators. With increasing demand of inversion, more research on inversion techniques is done.

In conventional motor drive or inversion technique, full bridge (shown at Figure 1-1) for single phase and for three phase (shown at Figure 1-2) for 3 phase applications are used. In Figure 1-1 and Figure 1-2 MOSFETs are considered as switches which may be replaced with other switching elements such as IGBT, GTO or thyristors. In Figure 1-1, when switches S1 and S4 are in conduction, positive voltage is applied to load, and when switches S2 and S3 are in conduction, negative voltage is applied to load. Thus by opening and closing the switches a PWM waveform with a fundamental component at desired frequency and magnitude is formed at the output. Different methods are used for producing PWM waveform; alternatively a square wave output may be produced. In square wave application, switching is done at the desired output frequency. In this method distortion is very high and large filters are required to smooth the output waveform. Its advantage is the low switching frequency thus low power dissipation. Multilevel inverters which are composed of

multi stage full bridge circuits, are also used to decrease distortion and losses caused by switching [1].

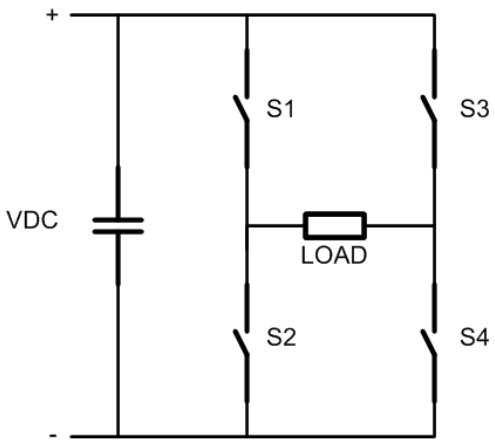


Figure 1-1 Single Phase Full Bridge Configuration

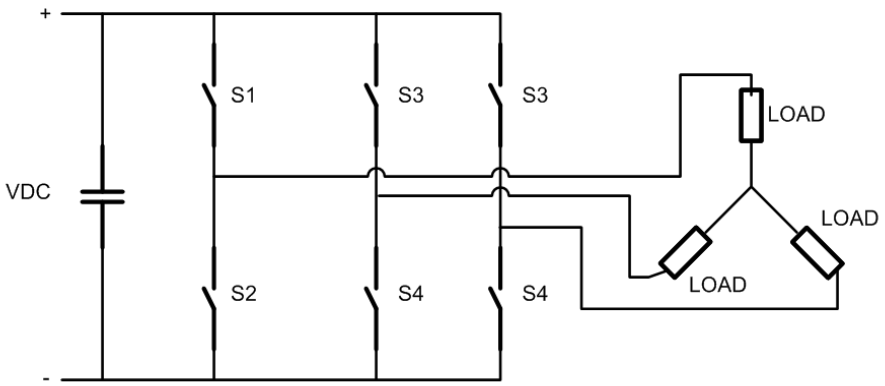


Figure 1-2 Three Phase Full Bridge Configuration

In PWM method, switching is done with higher frequency than the output frequency. Ratio of switching frequency to the output frequency is called frequency modulation index (m_f). When m_f increases, distortion in the output voltage waveform decreases since it is easier to filter high frequency components but switching losses increase. In Figure 1-4, harmonic spectrum of PWM waveform is shown when m_f is fifteen. The

waveform has fundamental component and harmonics. By using low-pass filters at the output, harmonics are filtered to obtain sinusoidal waveform. In Figure 1-3, an example of PWM waveform is shown. Its fundamental component is shown with red waveform.

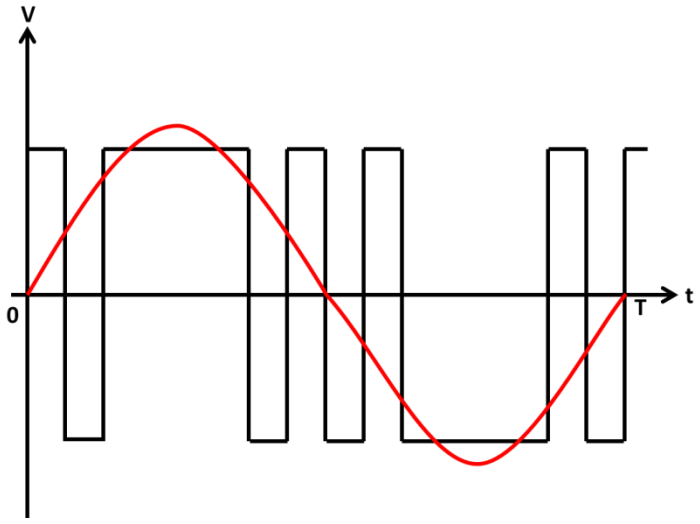


Figure 1-3 PWM Waveform(Black) and Fundamental Voltage Waveform(Red)

Amplitude modulation index(m_a) is another factor which effects the PWM waveform and fundamental output voltage magnitude. m_a is the ratio of magnitude of reference signal and magnitude of carrier signal. To obtain higher voltage levels at the output, m_a is increased. If m_a is greater than one, it is called overmodulation. Square wave operation is reached when m_a is too high.

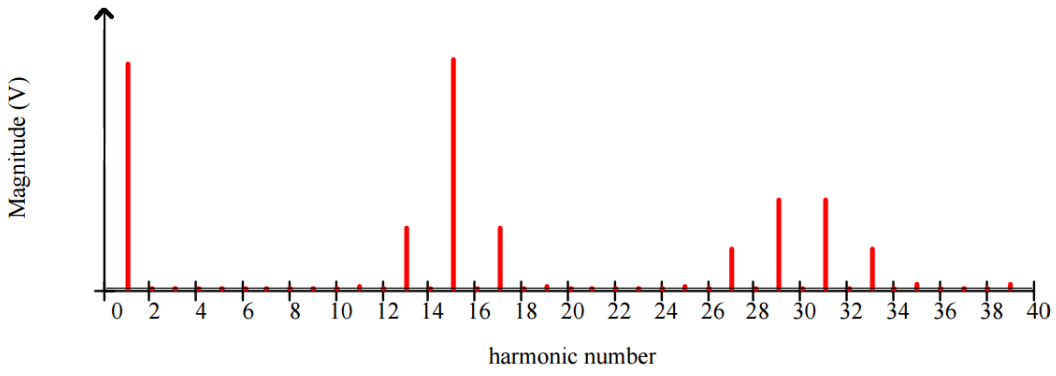


Figure 1-4 Harmonic Spectrum of Sinusoidal PWM at m_f=15

Even if PWM technique is used for conventional inversion technology, distortion at the output occurs since high voltage is switched continuously. Switching causes harmonics at the output. These harmonics lead to losses and reduction of torque in motors. To show that losses increase when a motor is driven with PWM, three induction machines (2 poles, 4 poles and 6 poles) with rated power 5.5kW are driven to compare motor core losses. Each motor is driven with a PWM output inverter and with a sine wave by connecting to grid. For same loads, core losses of motors are calculated. The core losses are shown in Table 1-1. When a motor is driven with PWM output, losses are higher with respect to a motor driven by sine wave.

Table 1-1 Core Loss Comparison of Grid and Inverter Fed Motor

	Core Loss of Inverter Connected Machine	Core Loss of Grid Connected Machine	Increase in losses due to PWM source
2 pole	304,87W	149,41W	155,46W
4 pole	271,83W	198,80W	73,03W
6 pole	195,82W	161,37W	34,35W

It is known that motor no-load core loss increases when it is driven by a PWM output ASD [2], [3], [4]. The effect of PWM supply on motor performance has always been of interest. In general it is known from measurements under no-load condition that the core loss of the motor increases when supplied by a PWM source. The core loss is found to decrease as the carrier frequency of the inverter increases. On the other hand the inverter circuit loss increases with increasing switching frequency. Depending on the drive carrier frequency, the losses of the converter can be greater than the core loss of the motor. [5]

PWM drives also may cause problems with the motor insulation. This is because the voltage that appears across the winding is composed of pulses, with a desired fundamental frequency. These pulses may cause high frequency currents to flow over the bearings and cause their rapid deterioration. Furthermore, they may cause a resonance to occur with the cable and insulation capacitances of the motor insulation, causing an underdamped oscillation. As a consequence much higher voltages may appear on the winding insulation than it is designed for. These increased stresses on the insulation may cause early failure of the insulation. Sometimes reactors are placed at the output of the inverter to alleviate this problem. As a consequence motor terminal voltage becomes less than rated value and may result in operating the motor at an operating point where it is efficiency is lower [6]. As a consequence losses of the motor are higher and it may be necessary to de-rate the motor. [5]

Alternatively some methods are developed which uses DC voltage to produce sine wave output. For example in Figure 1-5, conventional method is shown, grid voltage is rectified to obtain a DC voltage and it is switched and filtered to obtain sinusoidal voltage at output [7]. In Figure 4-3, alternative method is shown [7]. In this method DC voltage is used to obtain full wave rectified output waveform and in each half cycle this waveform inverted to obtain sine wave at the output. Various alternative single phase topologies are analyzed in Chapter 2. Three phase application of these alternative topologies are analyzed in Chapter 3 and Chapter 4.

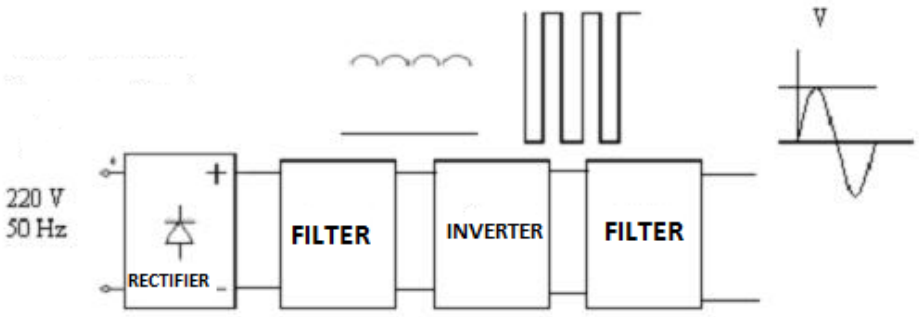


Figure 1-5 Conventional Method for Inversion

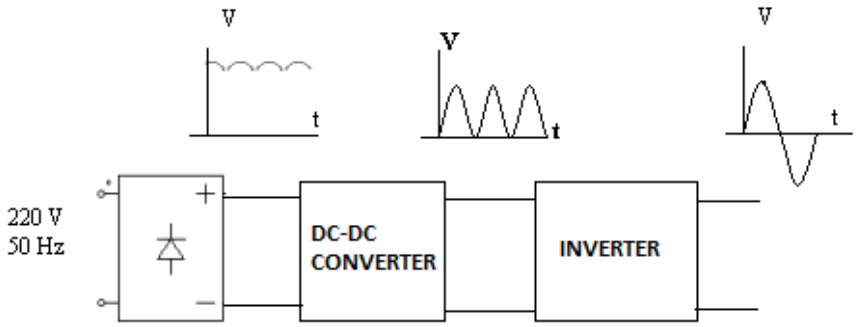


Figure 1-6 Alternative Method for Inversion

The discussion here raises the question of how to obtain a sinusoidal output at the inverter output. This can be achieved by filtering the PWM output of an PWM modulated inverter. Alternatively circuit configurations which may produce a sinusoidal output may be considered. The issue here is to make sure that the total loss of the inverter and the motor remains less than the conventional arrangement. Further considerations are the cost and size of the alternative inverter configurations. If an advantageous inverter configuration which satisfies the requirements is possible, that would certainly be very attractive for industry. Another issue which is worth considering is the boost capability of an inverter, which is discussed in section 1.2.

1.2. Benefits of Boosting Input Voltage

Due to voltage fluctuations in the grid or low voltage levels of battery fed systems, input voltage may decrease to value which is not enough to obtain desired output voltage. In that condition classical method is to use overmodulation. By using overmodulation fundamental component of AC signal is increased. However, this results to higher harmonic components. Even if over-modulation is used, boosting is limited and cannot be higher than RMS value of square wave [8].

Boosting capability eliminates harmonic problem and output voltage can be boosted any level up to component limits. In other words, it is dependent on components

used, by using higher voltage and current limited switches, inductors and capacitors voltage boost level can be increased.

In motor drive applications, wider constant torque region can be obtained by boosting output voltage since field weakening is avoided. This allows motors to operate at rated conditions even if input voltage of inverter decreases below its nominal level.

Nowadays, electrical vehicles are of great interest. In such an application, using an inverter with boosting capability increases the capability of these vehicles by utilizing battery for lower voltage levels. Battery cells must be connected to obtain required minimum operating voltage. Boosting stage allows operation at lower input voltages; therefore series connected battery cells can be decreased which allows smaller battery package. An example of state of charge for li-ion batteriy is shown for different discharge rates in Figure 1-7. “1C” in the figure refers to 15A, “2C” refers to 30A and other discharge rates can also be calculated in the same way. For example; if the system is designed for “1C” discharge and minimum voltage of 3V each cell, there is 15% energy left which cannot be used which is shown with dashed red lines in Figure 1-7. If boosting is available, energy left in the battery can also be used which increases utilization of battery.

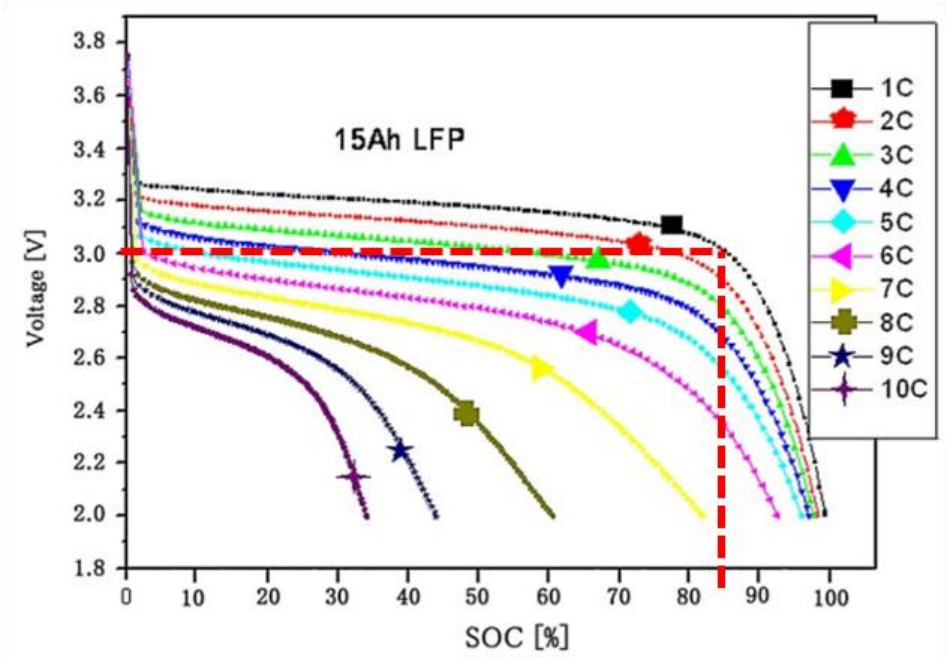


Figure 1-7 State of Charge of Li-İon Batteries at Different Discharge Rate

UPS systems may also benefit from this property. Since some of these systems are supplied by battery, ability to use lower voltage level without over-modulation will help UPS system to supply power with less harmonic content.

Solar powered systems also usually require boosting. Irradiation level may change due to weather conditions. Output current and output voltage level of solar cell is dependent on irradiation. When irradiation decreases, output voltage may decrease down to a value which is not enough for inverter to operate. By using boosting this issue can be solved. Similar problem may occur in wind powered systems since its power is also dependent on weather conditions. Although available energy is very low, this energy can be supplied to grid by boosting voltage up to required level. Voltage versus current and voltage vs power graph of a commercial solar cell for different irradiance values are shown in Figure 1-8. Solar cells are connected in series to increase voltage level and in parallel to increase current level. Voltage level which draws maximum power decreases nearly 10% when irradiance decreases from 1000W/m^2 to 600W/m^2. For lower values of irradiance, this difference in the voltage level also increases. If voltage level at maximum power is less than the minimum

voltage that inverter can operate, it will result panel to work at a point where its efficiency is not maximum. If open-circuit voltage level is less than the minimum voltage that inverter can operate, then no power can be extracted from solar cell. If boosting is possible, the inverter can operate to draw maximum power from solar cell in wider range. Typical irradiance level measured at different points of Earth in July is shown in Figure 1-9. For example; if a system located at 45° north is designed for minimum irradiance level of 600W/m^2, then nearly 5% solar energy cannot be extracted from panel. By using boosting this energy level which cannot be extracted form panel can be decreased.

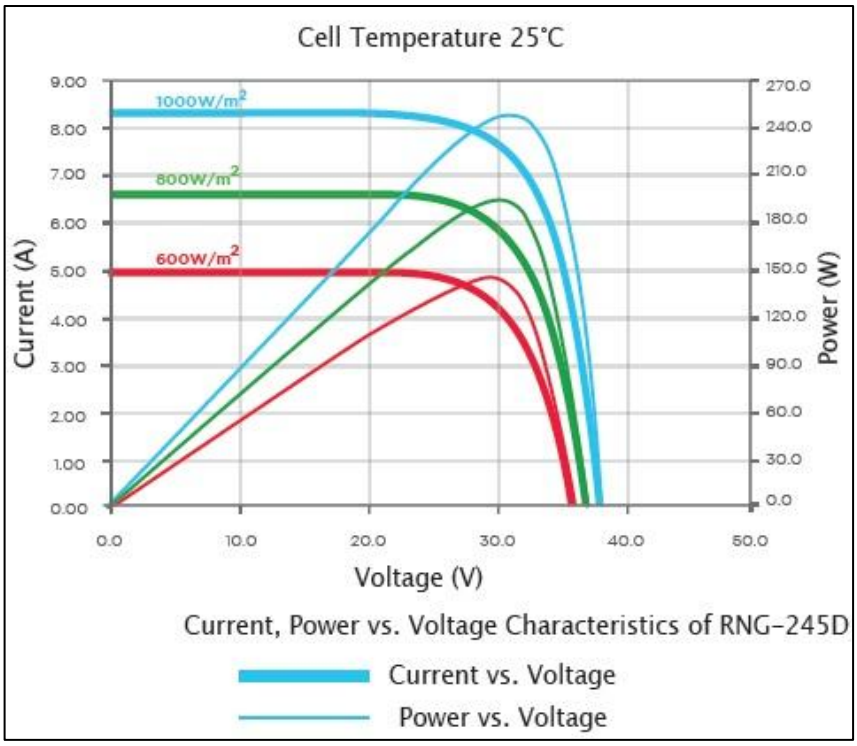


Figure 1-8 Voltage vs Current and Voltage vs Power Graph of a Commercial Solar Cell

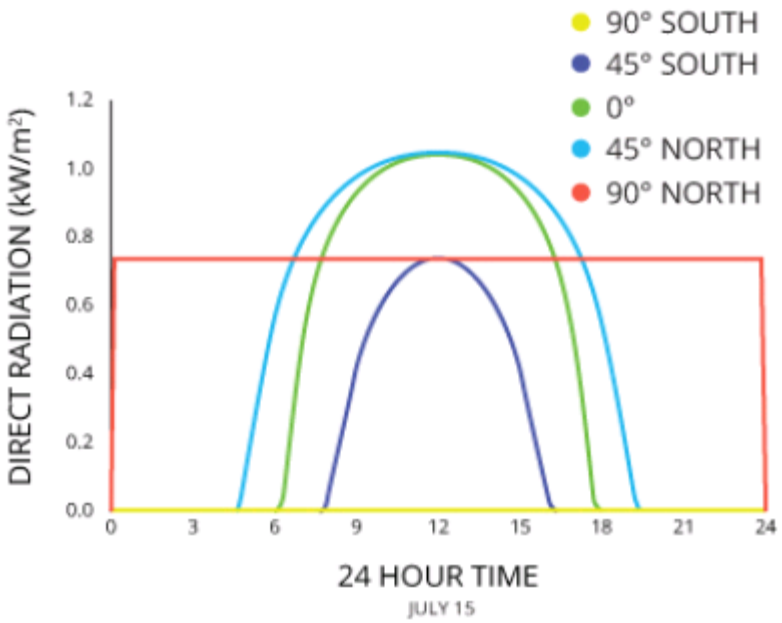


Figure 1-9 Irradiance Levels at Different Points of Earth in July

Boosting capability is also very important parameter for inversion. Therefore attention is paid to this parameter throughout this study.

1.3. Aim of Thesis

Importance of sine wave output and boosting capability is described in sections 1.1 and 1.2. Aim of the thesis is to design a three phase inverter with variable frequency and variable output voltage. Sine wave output and boosting capability are the main concerns while designing the inverter. Various single phase topologies in the literature which produce sine wave output are analyzed first to understand operating principles, advantages and disadvantages of them. Motor driving is one of the objectives of this study. Since motors generate power while braking, some modifications are proposed for these topologies to transfer power from output to DC link to investigate the possibility of using these circuits in a motor drive application. These single phase topologies are compared according to ratings of their components and their cost. Topologies are classified according their boosting capability also. Topologies without boosting capability are modified to obtain three phase output and

compared with classical inversion method. Topologies with boosting capability are also modified to obtain three phase output. An inversion method with boosting capability is also proposed and compared with other topologies with respect to component ratings. The proposed topology is further analyzed to compare efficiency and cost with classical method which contains boost converter in front of three phase full bridge and filter at the output.

1.4. Scope of Thesis

The thesis consists of seven chapters. This chapter gives basic information about aim of thesis and advantages of sine wave output and boosting.

Second chapter is about research done in the literature for producing single phase sine wave. The topologies are described, evaluated and compared.

Third chapter describes sine wave output topologies for three phase output without boosting capability. This chapter covers modifications of single phase topologies to obtain three phase output. These modified topologies for three phase output are described, evaluated and compared.

Forth chapter describes topologies for three phase output with boosting capability. In this chapter, first modifications of single phase topologies for three phase application are described. Then a topology is proposed with sine wave output and boosting capability. Lastly modified topologies and proposed topology are evaluated and compared.

In fifth chapter, design and implementation of proposed topology(non-inverting buck-boost inverter) is described.

In sixth chapter, test results of implemented design are given.

Last chapter is the conclusion of the thesis.

CHAPTER 2

SINGLE PHASE TOPOLOGIES

There are several studies in the literature which use DC voltage for obtaining pure sine wave at the output. Most of these studies are done for photovoltaic applications in which input supply voltage is much smaller than low voltage grid system voltage level (380Vrms line to line). All of these studies which are described in this chapter are done for single phase application [7], [9], [11], [12], [13]. Although aim of the thesis is to produce three phase output, these single phase topologies are analyzed to see their operation and feasibility of three phase application. Feasible topologies for three phase application are modified to obtain three phase output which are described in Chapter 3 and Chapter 4.

Each single phase topology in the literature, is evaluated according to suitability of input and output voltage levels, feasibility of two way power flow (when motors are the load, they may operate as generators during breaking thus this energy must be supplied back to DC bar) and components required. Input and output voltage levels are analyzed to determine voltage ratings of switches and capacitors used in each topology. Since motor drive is aimed, two way power flow of these topologies are analyzed. Some modifications are done to allow two way power flow if possible. Lastly the topologies are compared with each other and with classical method according to component ratings and total cost while operating with same input voltage, output power and output voltage.

Voltage and current ratings of components used in these topologies are analyzed first. By using these ratings, costs of each topology is calculated to compare them.

2.1. Boost DC-AC Converter (Topology A)

Block diagram and output voltage waveforms of Boost DC-AC Converter are shown in Figure 2-1 and in Figure 2-2 [9]. In the topology two boost converters are used which generate sine waves out of phase with same offset DC voltage. Since DC offset voltages are same for both output voltages of converters, difference of the output voltages is a sine wave.

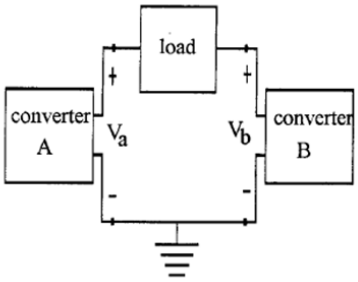


Figure 2-1 Block Diagram of Boost DC-AC Converter

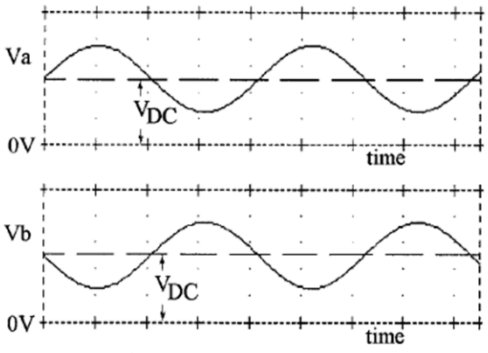


Figure 2-2 Output Voltage Waveforms of Boost DC-AC Converters

Circuit diagram of this topology is given in Figure 2-3 [9]. Figure “a” in Figure 2-3 shows one leg of the converter, Figure “b” in Figure 2-3 shows both legs.

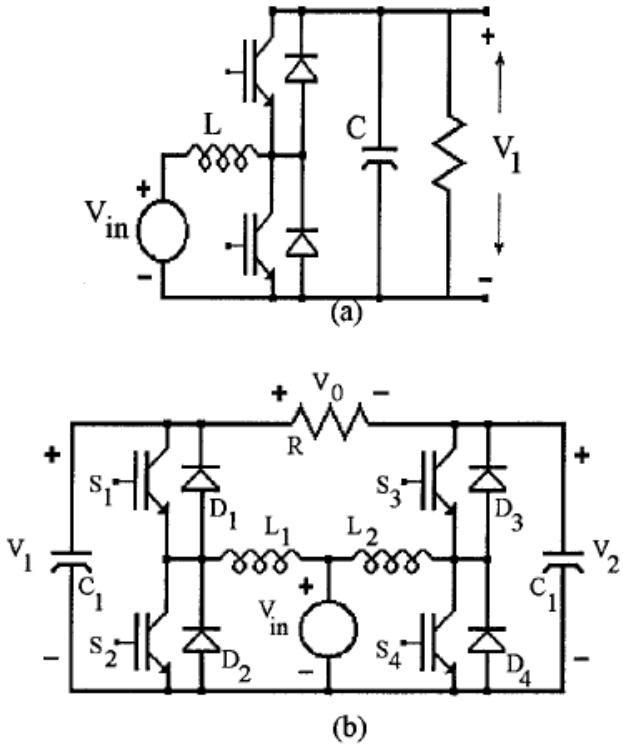


Figure 2-3 Circuit Diagram Boost DC-AC Converter

In Figure 2-4, V_a voltage waveform is shown [9]. V_a voltage has DC offset about 225V and 180V peak to peak AC voltage where input voltage is 96V. V_a waveform is not pure sine however V_b is not pure sine either thus when the difference of them are taken output waveform becomes more symmetrical. In Figure 2-5 V_{ab} is shown for open loop control [9].

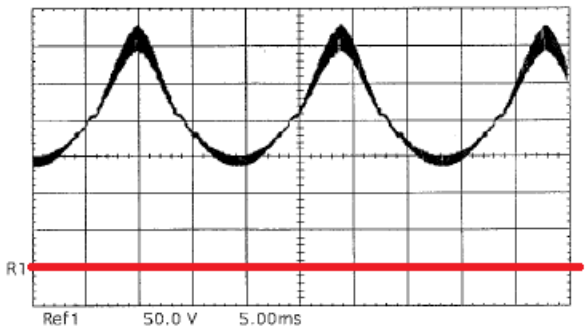


Figure 2-4 V_a Voltage Waveform with Open Loop Control

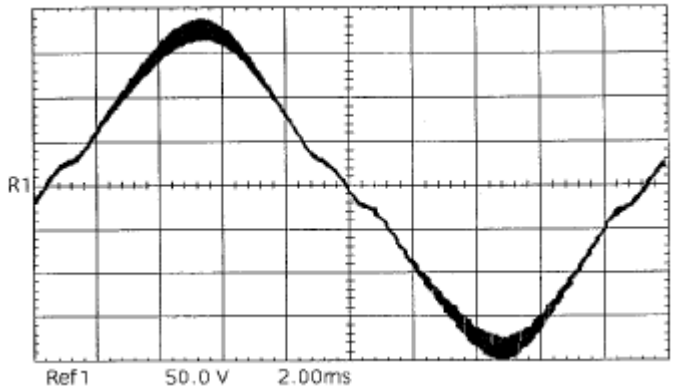


Figure 2-5 Output Voltage Waveform (V_{ab}) with Open Loop Control

2.1.1. Two Way Power Flow

The topology is appropriate for two way power flow. In Figure 2-3,b the circuit diagram is shown and in Figure 2-6 reverse power flow path is shown. Inductor current increases in the reverse direction when S1 is on and it decreases when S2 is on. It can transfer power from output to input DC bus.

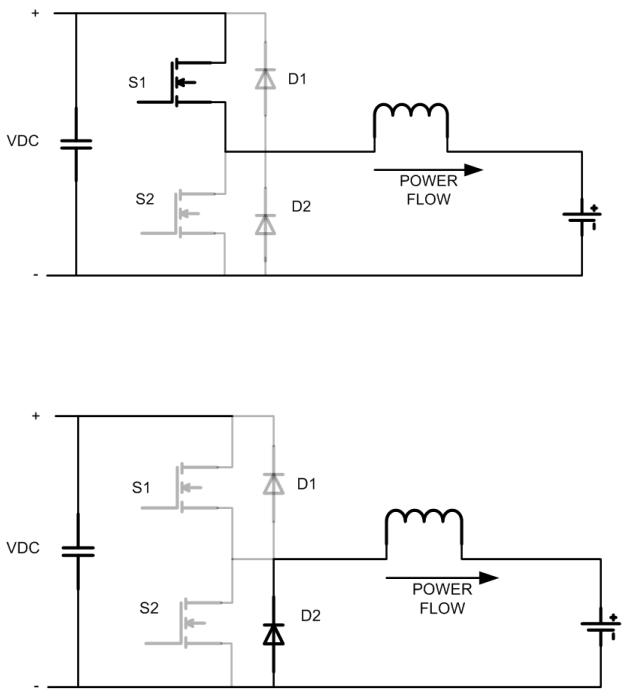


Figure 2-6 Reverse Power Flow Paths of the Boost Converter

2.1.2. Component Requirements

Voltage ratings of capacitors and switches are related to peak voltage over them. Output voltage swings between positive peak and negative peak. Thus peak to peak voltage is twice peak voltage. Output of boost topology is always higher than input voltage. Thus minimum output voltage can be taken as V_{in}. When twice peak voltage is added to input voltage, peak voltage is obtained.

$$V_{max} = V_{in} + V_{outrms} * 2 * \sqrt{2} \qquad (2.1)$$

If ripple is ignored, inductor current is maximum at peak voltage. If output of one converter is at maximum, output of other converter is at minimum. This is due to 180° phase shift. Minimum voltage is assumed to be V_{in} for calculating voltage stresses. Since output voltage is at maximum, output current is at maximum. Output current is obtained by dividing output power by output voltage.

$$I_{out} = \frac{P_{out}}{V_{out}} \quad (2.2)$$

Inductor current of converter whose output voltage is equal to input voltage, is equal to output current (No loss is assumed). Thus regenerated power is equal to input voltage multiplied by output current.

$$P_{Regenerated} = I_{out} * V_{in} \quad (2.3)$$

Total power supplied by one converter is equal to output power plus regenerated power by other converter.

$$P_{Total} = P_{Regeneated} + P_{Out} \quad (2.4)$$

Inductor current is equal to input current in boost topology, thus inductor current is calculated by dividing input power to input voltage. When losses are ignored, input power is equal to output power.

$$I_{Lmax} = \frac{P_{Total}}{V_{in}} \quad (2.5)$$

$$I_{Lmax} = \frac{P_{Regenerated}}{V_{in}} + \frac{P_{out}}{V_{in}} \quad (2.6)$$

$$I_{Lmax} = I_{out} + \frac{P_{out}}{V_{in}} \quad (2.7)$$

$$I_{Lmax} = \frac{P_{out}}{V_{out}} + \frac{P_{out}}{V_{in}} \quad (2.8)$$

Drawbacks of this topology:

1. Requirement of switches and output capacitor which must withstand higher voltage level than output peak to peak AC voltage plus input voltage. This is due to boost topology; output voltage must be always greater than input voltage.

2. Circulating currents may occur if output DC offset voltages differ from each other. According to load characteristic it may break down the system.
3. Power rating of one converter must be at least twice of output power since while one converter is supplying power other one regenerates power.

2.2. Flyback Inverter (Topology B)

Block diagram of flyback inverter is shown in Figure 2-7 and its circuit diagram is shown in Figure 2-8 [10].

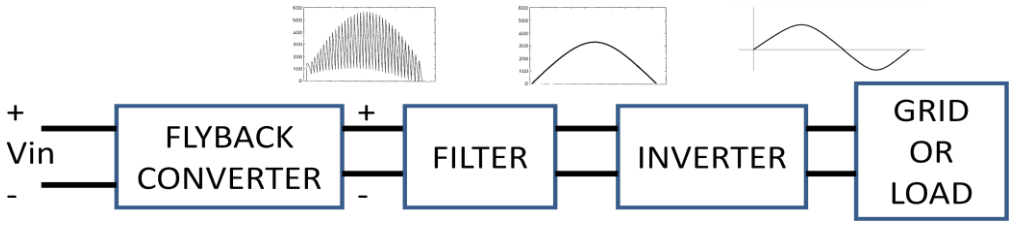


Figure 2-7 Block Diagram of Flyback Inverter

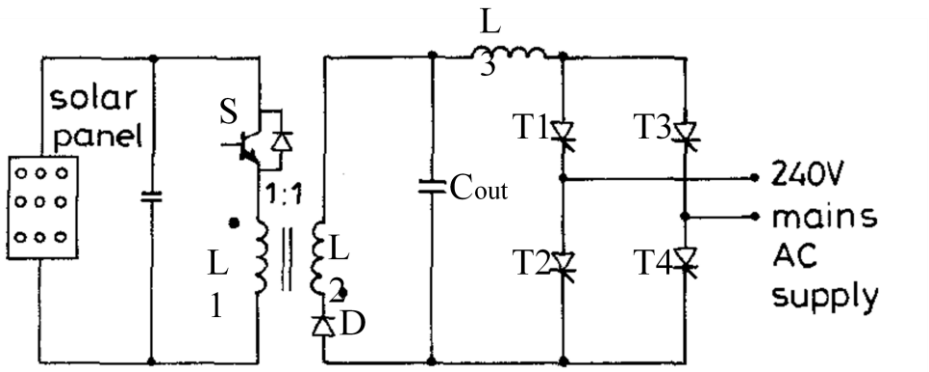


Figure 2-8 Circuit Diagram of Flyback Inverter

In the topology, flyback converter is used to regulate output current instead of output voltage. In Figure 2-9 output current waveform is shown and in Figure 2-10, voltage waveform of flyback output capacitor is shown [10]. Ripple voltage is nearly 400V at output capacitor. Output current is filtered by an inductor.

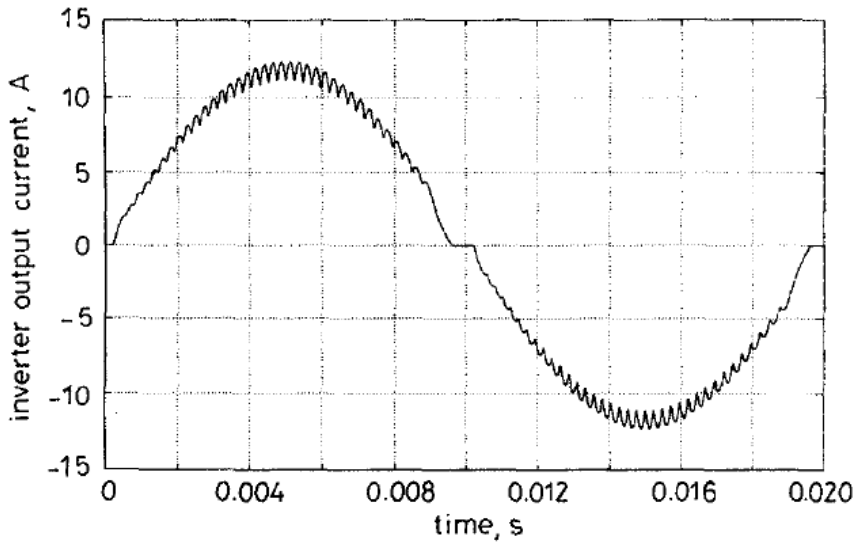


Figure 2-9 Output Current Waveform of Flyback Inverter

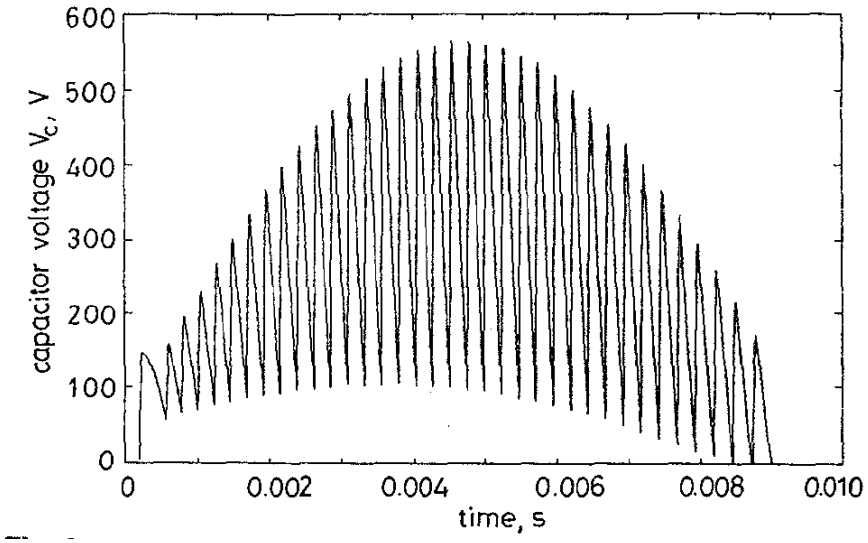


Figure 2-10 Output Capacitor Voltage Waveform of Flyback Inverter

2.2.1. Two Way Power Flow

This topology must be modified for two-way power flow. Diode D shown in Figure 2-8 must be replaced with a switch. Diodes must be added parallel to thyristors T1, T2, T3 and T4. Excess power passes through diodes parallel with thyristors to C_{out},

then it is transferred to input by the transformer. Figure 2-11 shows reverse power path. T1 and T4 are assumed to be on.

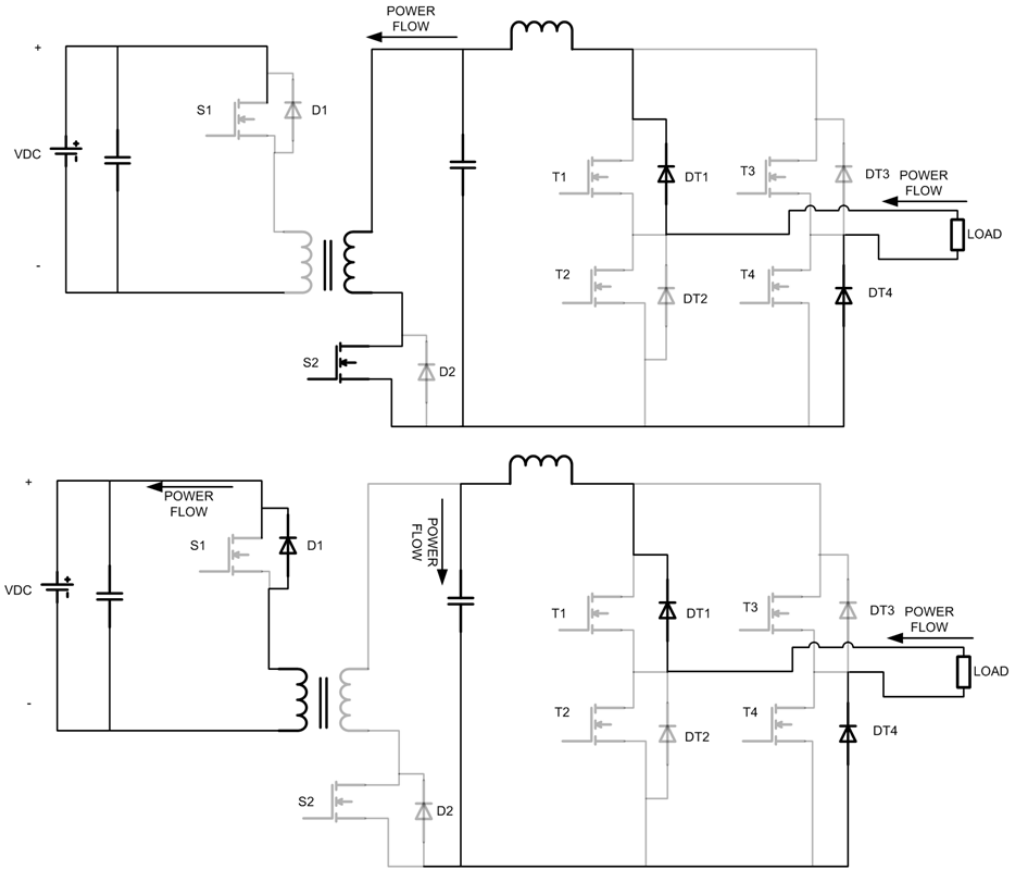


Figure 2-11 Reverse Power Flow Paths of Flyback Inverter

2.2.2. Component Requirements

Capacitor peak voltage is equal to output peak voltage plus ripple. Ripple can be assumed to be equal to output peak voltage. 1 capacitor is required.

$$V_{Cmax} = V_{outrms} * 2 * \sqrt{2} \quad (2.9)$$

Fast switch voltage ratings are equal to output voltage plus input voltage in flyback topology (1:1 turns ratio is assumed at transformer). 2 fast switches are required.

$$V_{FastSWmax} = V_{in} + V_{outrms} * 2 * \sqrt{2} \quad (2.10)$$

Slow switch voltage ratings are equal to output peak voltage. 4 slow switches are required.

$$V_{SlowSWmax} = V_{outrms} * 2 * \sqrt{2} \quad (2.11)$$

Inductor current rating is equal to output current rating (Ripple is ignored). 1 inductor is required.

$$I_{Lmax} = I_{out} \quad (2.12)$$

Transformer power rating is equal to output power (Zero loss is assumed). 1 transformer is required.

$$P_{Transformer} = P_{out} \quad (2.13)$$

Drawbacks of this topology:

1. Topology requires switch and capacitor voltage ratings more than required output voltage.
2. Topology requires both flyback transformer and inductor.
3. If load of the system is a machine, even if current does not contain very large value of ripple, phases of machine will see high frequency voltage components which results in harmonic torques and harmonic losses.

2.3. Single-Stage Boost Inverter (Topology C)

Block diagram of single stage DC-AC converter for photovoltaic systems is shown in Figure 2-12 [11]. Circuit diagram is shown in Figure 2-13 [11]. The circuit is capable of both boosting and inversion.

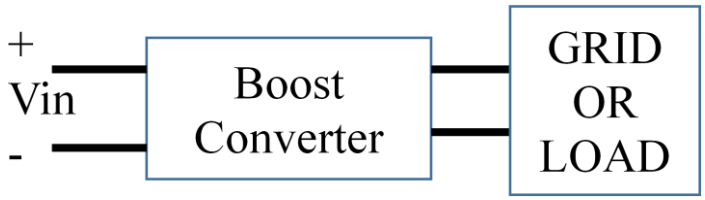


Figure 2-12 Block Diagram of Single-Stage Boost Inverter

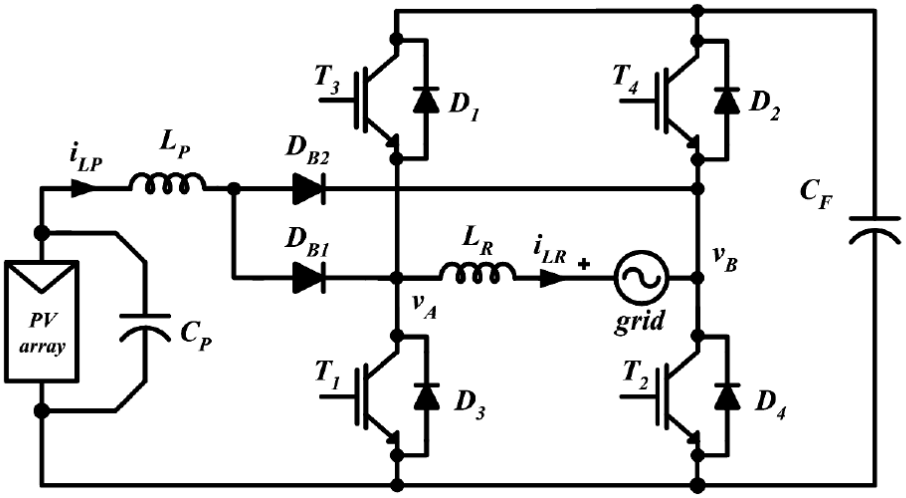


Figure 2-13 Circuit Diagram of Single-Stage DC-AC Inverter

Operating modes are shown in Figure 2-14 and Figure 2-15 [11]. In Figure 2-14 boosting modes are shown. If either T_1 or T_2 is on, L_p charges and when they are both off, L_p discharges on output capacitance.

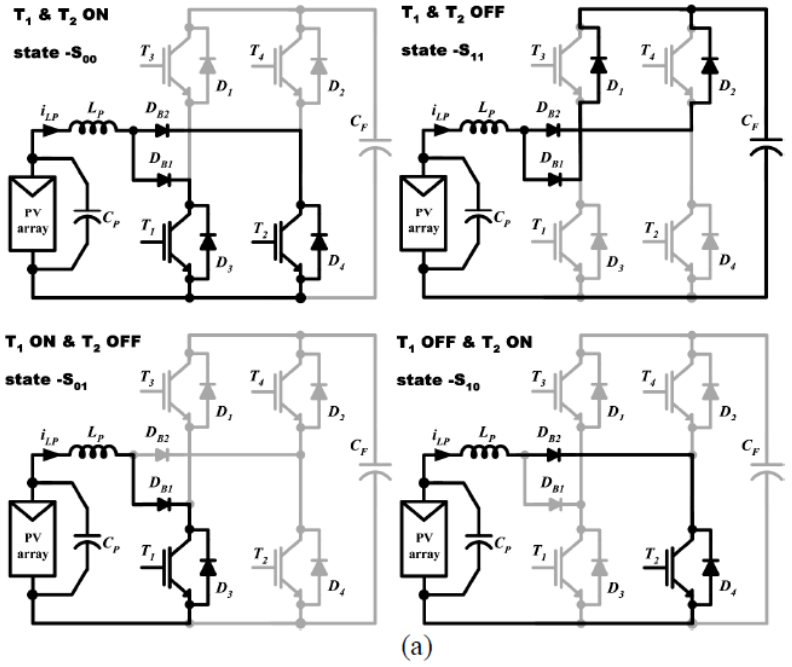


Figure 2-14 Current Paths in Boosting Mode

In Figure 2-15bridge modes are shown [11]. According to states of T_1, T_2, T_3 and T_4, load plus L_r sees 0, V_{CF} or $-V_{CF}$.

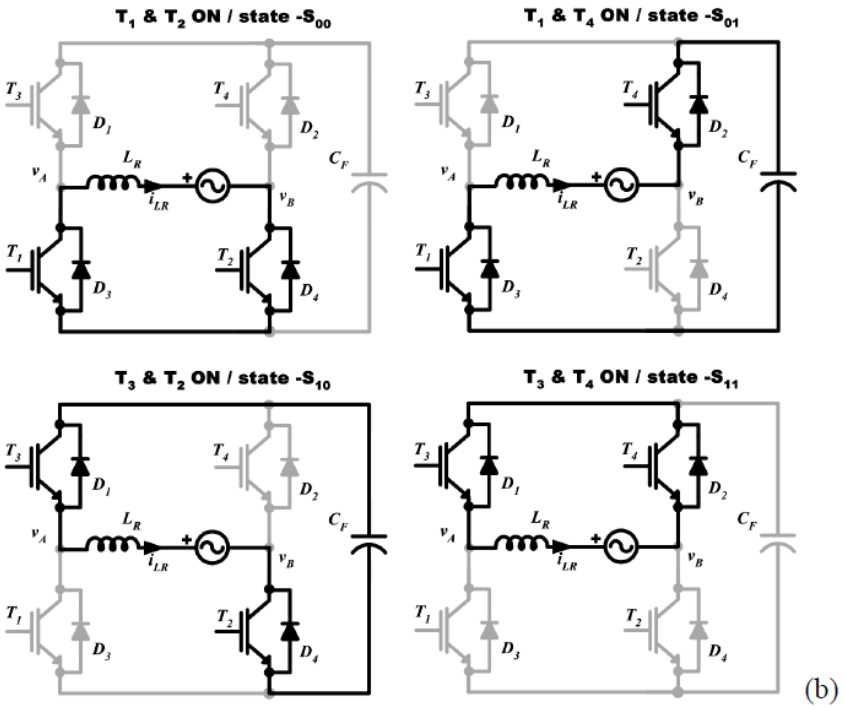
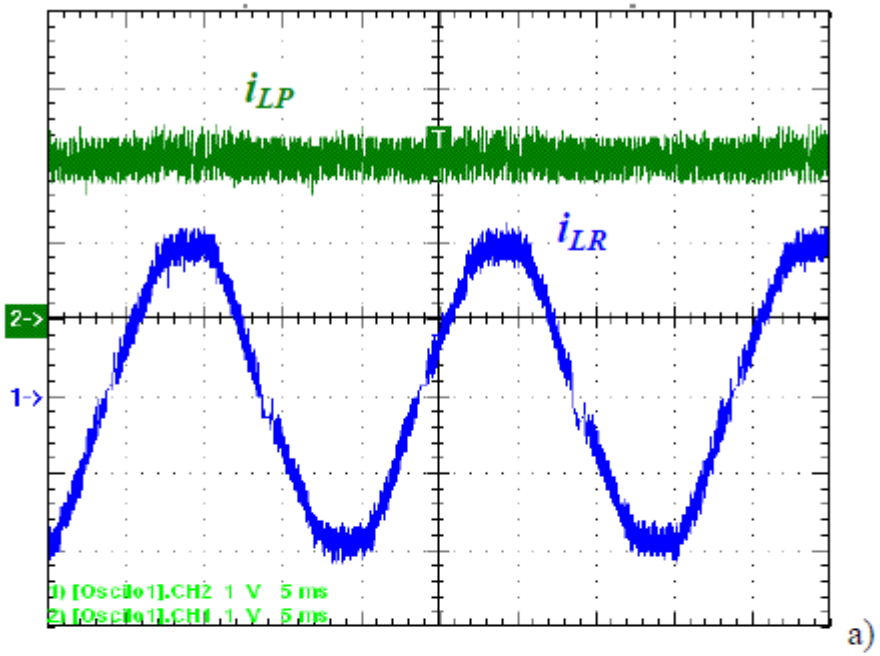


Figure 2-15 Current Paths in Bridge Modes

By using this topology, two stages of converter and inverter is decreased to one. In Figure 2-16, boost inductor current is shown with green, output current is shown with blue and grid voltage is shown with pink waveform [11]. Advantage of this topology is reducing the switch count.



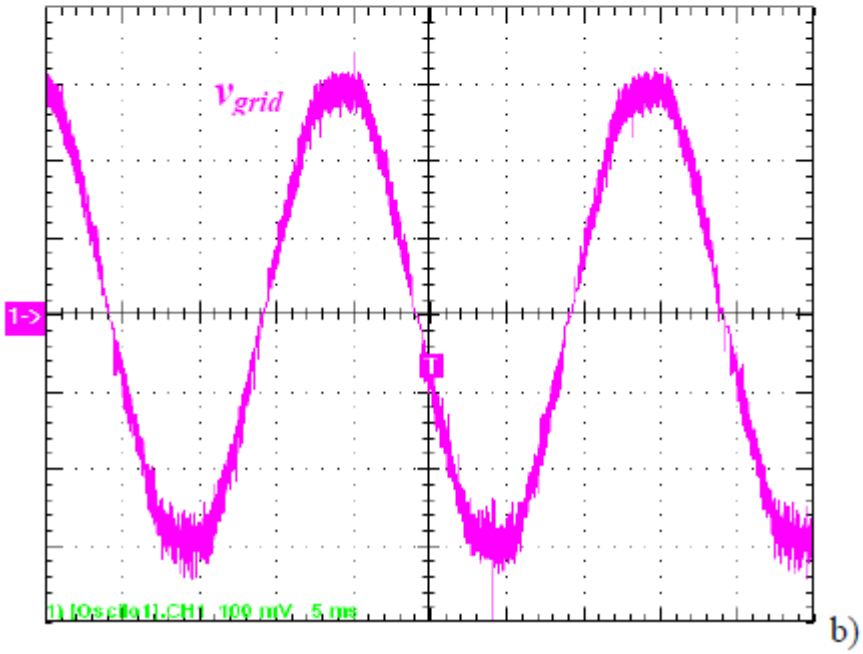


Figure 2-16 a) Output Current and Boost Inductor Current Waveforms b) Grid Voltage Waveform

2.3.1. Two Way Power Flow

This topology is not appropriate for two-way power flow. Diodes DB1 and DB2 which are shown in Figure 2-13, block reverse power flow.

2.3.2. Component Requirements

One capacitor is required. It must withstand input voltage plus output peak voltage. [11]

$$V_{Cmax} = V_{in} + V_{outrms} * \sqrt{2} \tag{2.14}$$

Four fast switches are required; their voltage rating is equal to capacitor voltage rating.

$$V_{SWmax} = V_{in} + V_{outrms} * \sqrt{2} \tag{2.15}$$

One inductor with current rating I_{outrms} is required since output current passes over it. (Zero loss is assumed, output voltage is assumed to be constant at a value V_{outrms}, ripple current is ignored)

$$I_{LR} = I_{outrms} \tag{2.16}$$

One inductor with current rating equal to input current is required. Input current can be calculated by dividing output power to input voltage. (Zero loss is assumed, output voltage is assumed to be constant at a value V_{outrms}, and ripple current is ignored)

$$I_{LP} = \frac{P_{out}}{V_{in}} \tag{2.17}$$

Drawbacks of this topology:

1. Requirement of storage capacitance which must stand output peak voltage plus input voltage.
2. Two way power flow is not possible with this configuration.

2.4. Single Stage Buck Boost Inverter For Solar Power Extraction (Topology D)

Block diagram for single stage DC-AC converter for photovoltaic systems is shown in Figure 2-17 [12]. Circuit diagram is shown in Figure 2-18 [12]. This topology is combination of boost and inverting topologies. For generating positive half cycle boost topology is used and for producing negative half cycle inverting topology is used. Neutral point being at zero voltage is advantage of this topology.

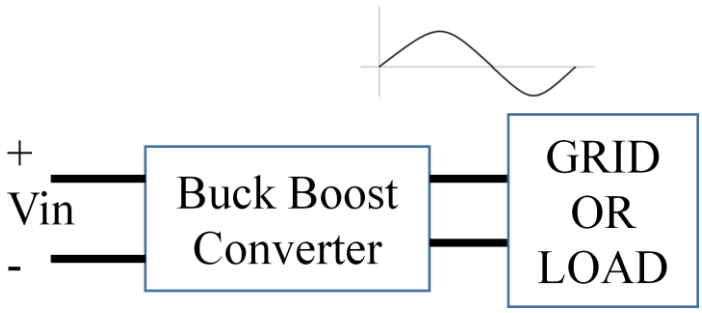


Figure 2-17 Block Diagram of Novel Single Stage DC-AC Buck Boost Inverter

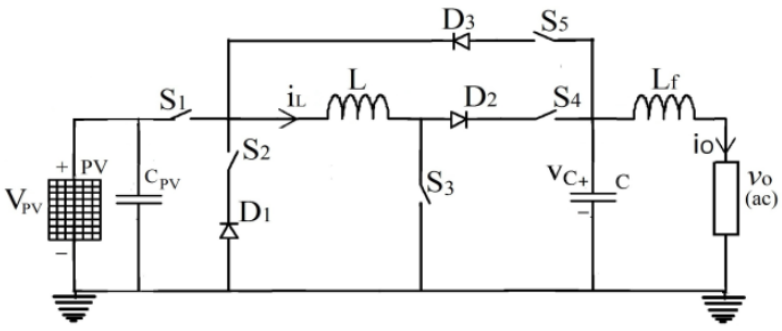


Figure 2-18 Circuit Diagram of Novel Single Stage DC-AC Buck Boost Inverter

Operating modes are shown in Figure 2-19 [12]. (a) and (b) are current paths for positive half cycle. (c) and (d) are current paths for negative half cycle.

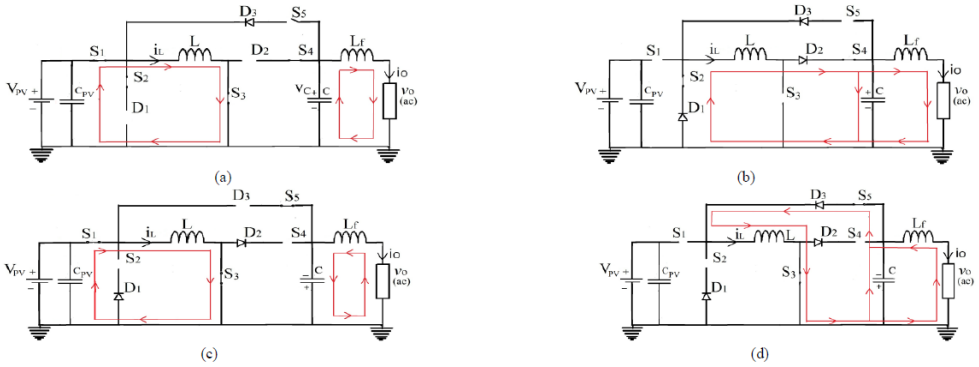
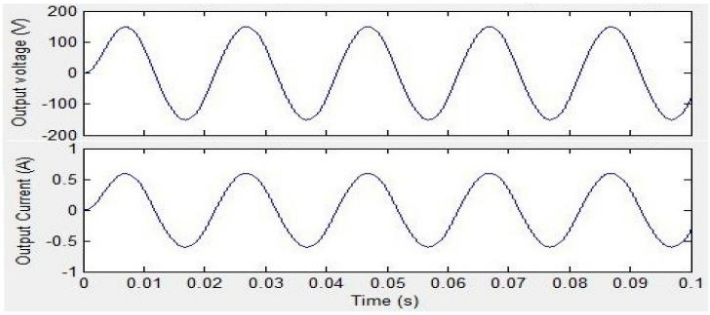
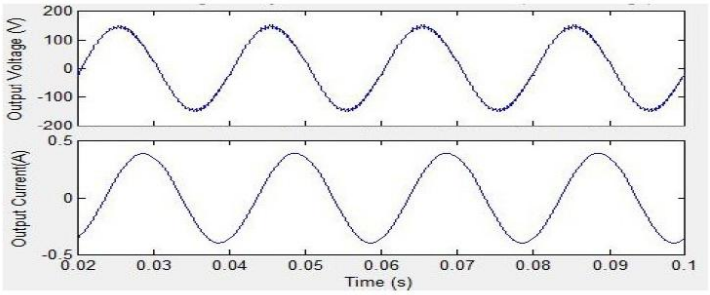


Figure 2-19 Current Path during different modes of operation: (a) Mode 1 for positive half cycle when S_1 and S_3 are ON (b) Mode 2 for positive half cycle when S_1 and S_3 are OFF (c) Mode 3 for negative half cycle when S_1 is ON (d) Mode 4 for negative half cycle when S_1 is OFF

In Figure 2-20, simulated output voltage and current waveforms are shown [12]. (a) shows resistive load waveforms. (b) shows inductive load waveforms.



(a)



(b)

Figure 2-20 a) Simulated Voltage and Current Waveforms for R Load, b) Simulated Voltage and Current Waveforms for RL Load

2.4.1. Two Way Power Flow

This topology must be modified for two-way power flow. A switch must be added parallel to diodes D_3 and S_5, a switch must be added parallel to diodes D_2 and S_4, a switch must be added parallel to diodes S_2 and D_1, a diode must be added parallel to S_1 and a diode must be added parallel to S_3 which are shown in Figure 2-18. Modified circuit is shown in Figure 2-21. The current path will be similar to the one in Figure 2-19 but in the opposite direction.

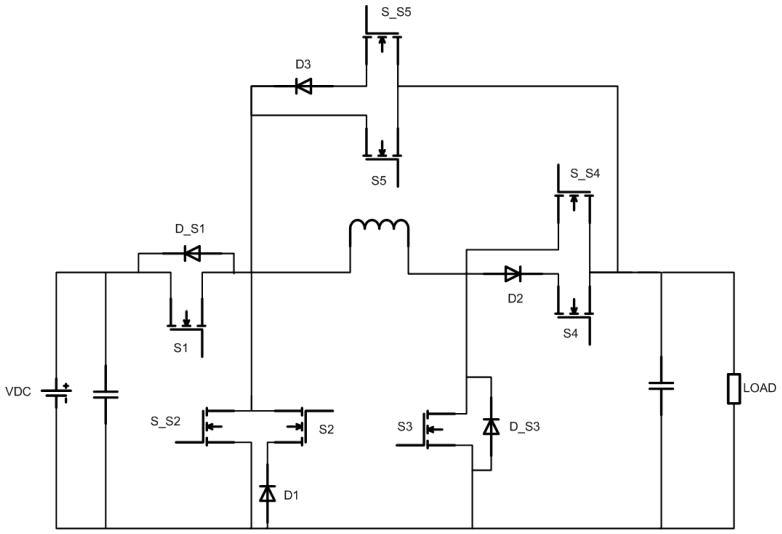


Figure 2-21 Modified Circuit for Two Way Power Flow

2.4.2. Component Requirements

One capacitor is required. It must withstand positive and negative output peak voltage.

$$V_{Cmax} = \pm V_{outrms} * \sqrt{2} \tag{2.18}$$

Five fast switches are required. During negative cycle operation S1 and S5 must withstand input voltage plus output peak voltage. S_S2 must withstand input voltage. S_S4 and S_S5 must withstand output peak voltage during positive cycle operation.

$$V_{S1max} = V_{in} + V_{outrms} * \sqrt{2} \tag{2.19}$$

$$V_{S5max} = V_{in} + V_{outrms} * \sqrt{2} \tag{2.20}$$

$$V_{S\_S2max} = V_{in} \tag{2.21}$$

$$V_{S\_S4max} = V_{outrms} * \sqrt{2} \tag{2.22}$$

$$V_{S\_S5max} = V_{outrms} * \sqrt{2} \quad (2.23)$$

Three slow switches are required. During positive cycle S3 must withstand output peak voltage. During negative cycle S2 and S4 must withstand output peak voltage.

$$V_{S2max} = V_{outrms} * \sqrt{2} \quad (2.24)$$

$$V_{S3max} = V_{outrms} * \sqrt{2} \quad (2.25)$$

$$V_{S4max} = V_{outrms} * \sqrt{2} \quad (2.26)$$

One inductor is required. Inductor current is at maximum value when output voltage is at negative peak. Inductor current can be calculated by equation 2.27. I_{outrms} can be calculated by dividing output power to output voltage. 1-D term is equal to input voltage divided by output voltage. Replacing I_{outrms} and 1-D term, results in equation 2.28. (Zero loss is assumed, output voltage is assumed to be constant at a value V_{outrms}, ripple current is ignored)

$$I_L = \frac{I_{outrms}}{1-D} \quad (2.27)$$

$$I_L = \frac{P_{out}*(V_{in}+V_{outrms})}{V_{in}*V_{out}} \quad (2.28)$$

Drawbacks of this topology:

1. Output capacitor must withstand both positive and negative polarities thus electrolytic capacitors cannot be used.
2. Switch count is relatively higher with respect to similar topologies.

2.5. Novel Bidirectional DC-To-AC Inverter (Topology E)

Block diagram of Novel Bidirectional DC-to-AC Inverter is shown in Figure 2-22 [13]. Circuit diagram is shown in Figure 2-23, a. In this method buck converter is

used to produce half-wave of a sine and it is inverted to obtain a pure sine wave at the output. Reference, capacitor and output voltages are shown in Figure 2-23, b.

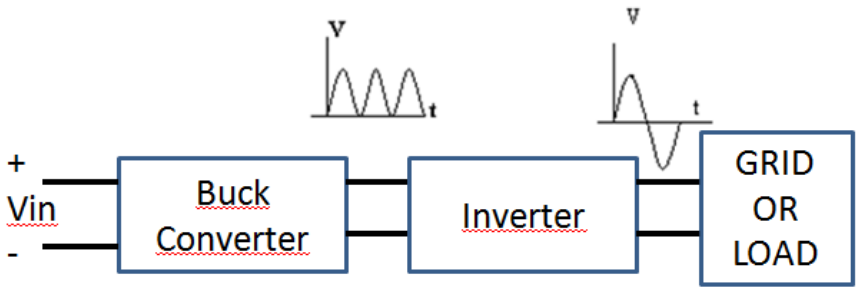


Figure 2-22 Block Diagram of Bidirectional DC-To-AC Inverter

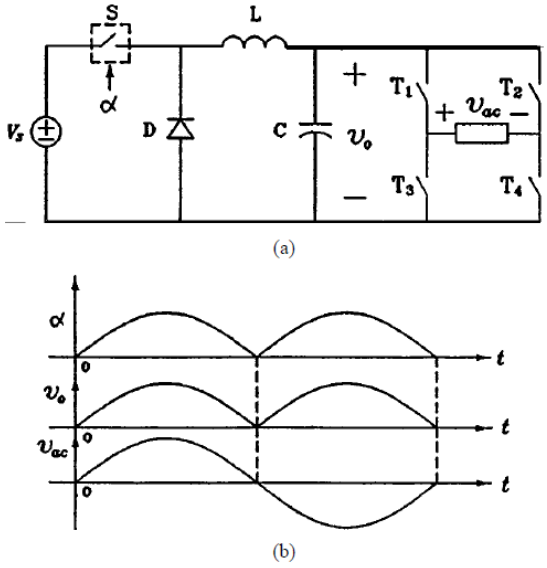


Figure 2-23 Circuit Diagram of Bidirectional DC-To-AC Inverter (a), Waveforms (b)

Full wave rectified sine waves are produced. Load is fed positive cycle when T1 and T4 are on. Load is fed negative cycle when T2 and T3 are on. This study is similar to research done by Ertan[7] in the sense of producing output. Main difference between research done by Ertan[7] and study on Novel Bidirectional DC-to-AC Inverter [13] is the operating voltage. Converter researched by Ertan[7], uses voltage levels about

low voltage grid system. And the converter researched in the study of "Novel Bidirectional DC-to-AC Inverter[13]" uses voltage levels about battery voltage.

2.5.1. Two Way Power Flow

Two way power flow is possible with this topology by adding a switch parallel to diode D in Figure 2-23, a. Modified circuit diagram is shown in Figure 2-24 assuming S1 and S4 are on.

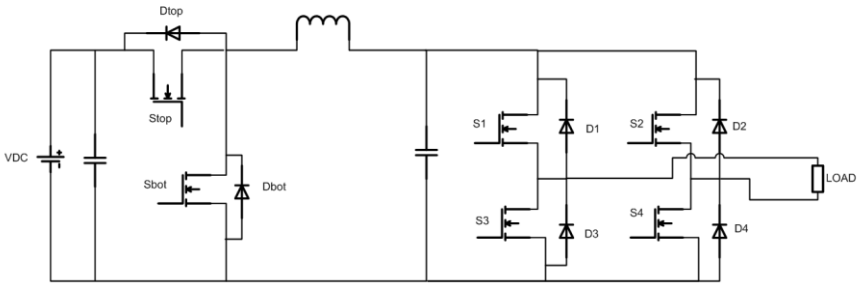


Figure 2-24 Circuit Diagram for Two Way Power Flow

In Figure 2-25 and Figure 2-26 reverse power flow paths are shown.

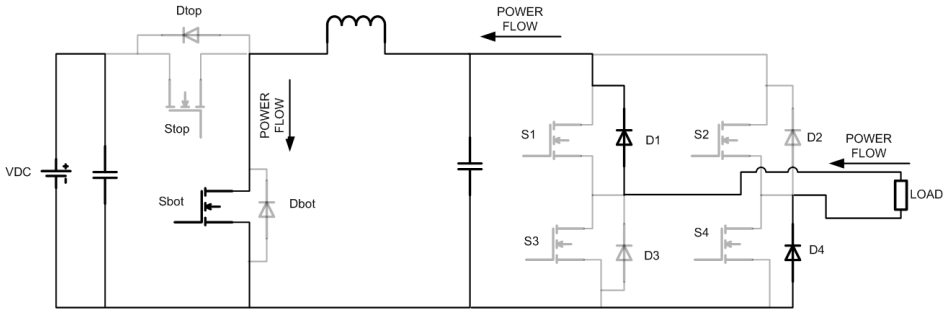


Figure 2-25 Reverse Power Flow Path(Sbot is conducting)

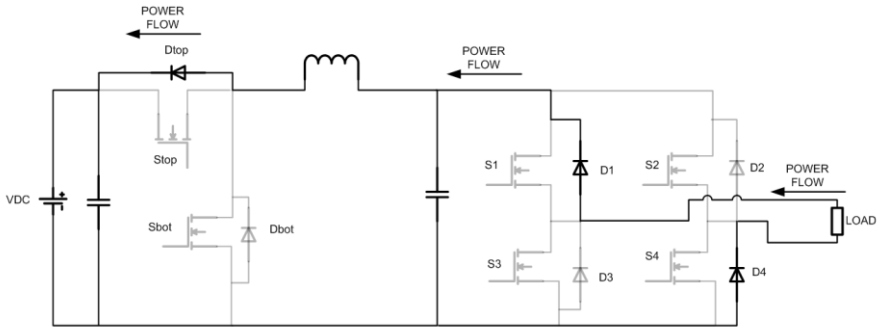


Figure 2-26 Reverse Power Flow Path (Dtop is conducting)

2.5.2. Component Requirements

One capacitor is required. It must withstand positive output peak voltage.

$$V_{Cmax} = V_{outrms} * \sqrt{2} \tag{2.29}$$

Two fast switches are required. These switches are used in buck stage and oust withstand input voltage.

$$V_{Sfastmax} = V_{in} \tag{2.30}$$

Four slow switches are required. These switches are used at inversion stage and they must withstand output peak voltage

$$V_{Sslowmax} = V_{outrms} * \sqrt{2} \tag{2.31}$$

One inductor with current rating I_{outrms} is required since output current passes through this inductor. (Zero loss is assumed, output voltage is assumed to be constant at a value V_{outrms}, and ripple current is ignored)

$$I_L = I_{outrms} \tag{2.32}$$

Drawback of this topology:

1. Output voltages higher than input voltage cannot be obtained.

2.6. Comparison of Topologies

The topologies are modified to be appropriate for two way power flow and required switch counts are revised. Table 2-1 is formed to compare previous studies done, table contains maximum switch and capacitor voltages, requirement of fast and slow switches for three phase application and circuit diagram of that topology. In the table by V_{out}, phase to neutral rms voltage is referred. For ease of calculation DC output with magnitude V_{outrms} is assumed at the output and drawing current I_{outrms}.

Flyback Converter shown in Table 2-1 assumed to have transformer with 1:1 turns ratio [10].

Table 2-1 Voltage and Current Ratings of Topologies

	Switch Voltage	**Capacitor Voltage**	**Inductor Current**
A) BOOST DC-AC	$V_{in}+V_{outrms}*2\sqrt{2}$ (4 fast switches)	$V_{in}+V_{outrms}*2\sqrt{2}$ (2 capacitors)	$P_{out}/V_{in}+$ P_{out}/V_{outrms} (2 inductors)
B) FLYBACK	$V_{in}+V_{outrms}*2\sqrt{2}$ (2 fast switches) $V_{outrms}*\sqrt{2}$ (4 slow switches)	$V_{outrms}*2\sqrt{2}$ (1 capacitor)	I_{outrms} (1 inductor) Additional Flyback Transformer
C) SINGLE STAGE BOOST	$V_{in}+ V_{outrms}*\sqrt{2}$ (4 fast switches)	$V_{in}+ V_{outrms}*\sqrt{2}$ (1 capacitor)	I_{outrms} (1 inductor) P_{out}/V_{in} (1 inductor)
D) SINGLE STAGE BUCK-BOOST	$V_{in}+V_{outrms}*\sqrt{2}$ (2 fast switches) V_{in} (1 fast switch) $V_{outrms}*\sqrt{2}$ (2 fast switches,3 slow switches)	$\pm(V_{outrms}*\sqrt{2}\,)$ (1 capacitor)	$P_{out}*(V_{in}+ V_{outrms})$ / $(V_{in} * V_{outrms})$ (1 inductor)
E) BUCK+ INVERTER	V_{in}(2 fast switches) $V_{outrms}*\sqrt{2}$ (4 fast switches)	$V_{outrms}*\sqrt{2}$ (1 capacitor)	I_{outrms} (1 inductor)
F) CLASSICAL (Single Phase Full Bridge Inverter)	V_{in}(4 fast switches)	$V_{outrms}*\sqrt{2}$ (1 capacitor)	I_{outrms} (1 inductor)

When Table 2-1 is observed, topology with minimum stress on switches and capacitor is to be topology E. It has also minimum count of fast switches but it cannot boost the input voltage.

Topology B is similar with topology E. They both have converter stage plus inverter stage. Topology B may be considered as isolated version of topology E. By changing transformer turns ratio in flyback transformer, input voltage can be boosted but it may increase the switch and capacitor stresses. Since topology B requires transformer, more losses occur due to leakage inductance. Leakage inductance causes some of power not to be transferred from primary to secondary side, therefore snubbers are required not to overstress switches. Also in the study another inductance is needed for topology B to filter output current.

Topology C and D are similar. They do not require extra inverting stage. These two topologies are able to boost input voltage. Topology C is not appropriate for two way power flow.

Topology A requires two converters thus it requires two inductances and two capacitances which doubles the cost of inductors and capacitors. Its switch and capacitor voltage ratings are the highest according to compared topologies. Its only advantage is being able to boost input voltage.

2.6.1. Cost Evaluation

To calculate costs of materials, Burkart and Kolar's cost models are used[14]. Each component cost model depends on ratings of that component.

Capacitor Cost Model

In equation 2.33, cost model for electrolytic capacitor is shown. b_{ELCO} and c_{ELCO} are fixed parameters which are shown in Table 2-2, Cr is capacitance value in uF and U_r is voltage rating of capacitor. In equation 2.34, cost model for film capacitor is given.

a_{film}, b_{film} and c_{film} are fixed parameters which are shown in Table 2-2, C_r is capacitance value in uF and U_r is voltage rating of capacitor.[14]

$$\sum ELCO = b_{ELCO}U_r + c_{ELCO}C_rU_r^2 \quad (2.33)$$

$$\sum film = a_{film} + b_{film}U_r + c_{film}C_r \quad (2.34)$$

Table 2-2 Capacitor Cost Calculation Parameters

	a_x	b_x	c_x
ELCO		$1.437 \cdot 10^{-3}$ €/V	$24.757 \cdot 10^{-9}$ €/µF V²
Film	-1.022 €	$54.956 \cdot 10^{-3}$ €/V	$2.426 \cdot 10^{-3}$ €/µF
X2 305 V	-0.025 €		0.155 €/µF
Y2 300 V	0.073 €		2.604 €/µF

Inductor Cost Model

Inductor cost is evaluated in two parts, core cost and winding cost. In equation 2.35, cost calculation formula is shown. Parameters are looked from Table 2-3. Parameters with €/kg are multiplied by weight of corresponding material. Parameters with €/unit are simply added in the equation. [14]

$$\sum L = \sigma_{core,x}W_{core} + \sigma_{wdg,x}W_{wdg} + \sum_{mat,x}^{fc} + \sigma_{lab,x}W_{wdg} + \sum_{lab,x}^{fc} \quad (2.35)$$

Table 2-3 Inductor Cost Calculation Parameters

Core type:	**High flux ferrite**	**Amor-phous**	**Nanocris-talline**	**High Si steel**	**GOES**
$\sigma_{\text{core},x}$ (€/kg)	5.5	16.0	23.0	12.0	2.5
Winding type:	**Solid round**	**Flat**	**Foil**	**Litz**	
$\sigma_{\text{wdg},x}$ (€/kg)	10.0	10.0	20.0	$\frac{15.0}{\frac{A_{\text{strand}}}{\text{mm}^2}+0.45}$	
$\Sigma^{\text{fc}}_{\text{mat},x}$ (€/unit)	1.0	2.0	2.0	1.0	
$\sigma_{\text{lab},x}$ (€/kg)	7.0	21.0	14.0	7.0	
$\Sigma^{\text{fc}}_{\text{lab},x}$ (€/unit)	2.0	4.0	2.5	2.0	
Ξ_L (%)			25.0		

Since inductor cost model is based on weight of core and winding. To compare costs, weights of core and winding must be found for given inductance L and current rating of inductor. By using equation 2.36 core area and winding are product is obtained. Assuming A_{core} and A_{wdg} equal and square, core volume and winding volume is found. Mass is obtained by multiplying material density with volume.

$$A_{core} * A_{wdg} = \left(\frac{L * I^2 * 10^4}{B_m * K_u * K_j}\right)^{1.16} \tag{2.36}$$

Switch Cost Model

Switch cost model consists of chip area and package cost[14]. Chip area is calculated according to equation 2.38 for 1200V transistors and 2.39 [21][22]. for 600V transistors. After calculating chip area, by using Table 2-4 for parameters, cost is calculated.

$$\sum SC = \left(\sum_n \sigma_{chip,x(n)} A_{chip,n}\right) + \sum pack, x \tag{2.37}$$

Table 2-4 Silicon Cost Calculation Parameters

Chip technology:	Si T&FS IGBT	Si NPT IGBT	Si PiN diode	SiC Schottky diode	Si CoolMos
$\sigma_{chip,x}^{600\,V}$ (€/cm²)	5.52	7.22	2.46	46.24	4.48
$\sigma_{chip,x}^{1200\,V}$ (€/cm²)	6.57	6.65	4.46	86.47	
Package type:	**TO-247-3**	**SOT-227**	**Module (23.2 cm²)**	**Module (29.9 cm²)**	**Module (37.6 cm²)**
$\Sigma_{pack,x}$ (€/unit)	0.55	8.10	7.62	10.01	15.06

$$A_{T,1200V}(I_N) = 0.95\,\frac{mm^2}{A} * I_N + 3.2mm^2 \tag{2.38}$$

$$A_{T,600V}(I_N) = 0.47\,\frac{mm^2}{A} * I_N - 0.32mm^2 \tag{2.39}$$

2.6.2. Cost Comparison

To make cost comparison some assumptions are done.

- V_{in}=310V (Single phase full bridge is applied)
- V_{out}=220Vrms
- P_{out}=3.3kW
- L=1mH
- C=47uF Electrolytic capacitor is used except for single stage buck boost topology.
- Si T&FS IGBT are used as switches and current rating is twice of required for safety margin.
- Slow switch(Switching at 50Hz) cost are taken 40% of fast switch.[15]

For each topology switch, capacitor and inductor cost are calculated and shown on Table 2-5.

Table 2-5 Costs of Single Phase Topologies

	Switch Cost	Capacitor Cost	Inductor Cost	Total Cost
A) BOOST DC-AC	13.5€	2.67€	74.56€	**90.73€**
B) FLYBACK	9.4€	2.41€	28.4€+13.4€	**53.61€**
C) SINGLE STAGE BOOST	6.76€	1.34€	28.4€+18.3€	**54.8€**
D) SINGLE STAGE BUCK-BOOST	19.39€	33.16€	37.28€	**89.83€**
E) BUCK+ INVERTER	5.94€	0.56€	28.4€	**34.9€**
F) CLASSICAL FULL BRIDGE + FILTER	6.6€	0.56€	28.4€	**35.56€**

Cheapest method is topology E. Its only disadvantage is not being able to boost input voltage. Topology E is further analyzed in Chapter 3 to obtain three phase output by modifying single phase topology. Topology B is also explained in Chapter 3 as an alternative to topology E.

Topology A and Topology D are further analyzed in Chapter 4 to obtain three phase output by modifying single phase topology. Topology C is not analyzed since two way power flow is not possible.

2.7. Summary

In this chapter, topologies which produce pure sine wave at the output are evaluated. The topologies are compared according to the ratings of components, cost of inverter, and ability of transferring power in two ways. In next chapters, topologies which are appropriate for three phase application will be further analyzed. In Chapter 3, topology E described in section 2.5 will be analyzed further for three phase application. In Chapter 4, topology A and D will be analyzed further for three phase application.

CHAPTER 3

THREE PHASE TOPOLOGIES WITHOUT BOOST CAPABILITY

As discussed earlier the aim of this study is to seek inverter topologies which are capable of producing a sine wave output. The desired topology of course should have comparable efficiency to classic H bridge topology, should have similar or lower cost and in addition it is desirable to have boosting capability, which helps to extend constant torque region in vector controlled motor drives or in renewable energy applications reduce storage element cost. This chapter concentrates on obtaining a 3-phase sinus output waveform utilizing the single-phase inverter topologies discussed in the previous chapter to find out the possibility of using there of them to achieve the purpose.

The investigation starts with Topology E which produces full wave rectified sine wave waveform, by using a buck converter and followed by a full bridge stage to fold back sine wave as described in Chapter 2 (Figure 3-1) The reason why this topology is further investigated here is that it appears to have many of the desirable properties as compared to other single-phase inverter circuits discussed in Chapter 2.

Four different variations of the basic topology are proposed to obtain three-phase sine wave output. They are first evaluated according to switch ratings and counts of inversion stage. A topology which requires less switch count is selected to compare with classical way of inversion.

One topology which directly produces sine-wave output stage is compared with classical way of inversion in terms of efficiency of the inverter and THD of output voltage waveform. Then one topology with lower switch voltage ratings is compared with classical way of inversion in terms of efficiency of the inverter.

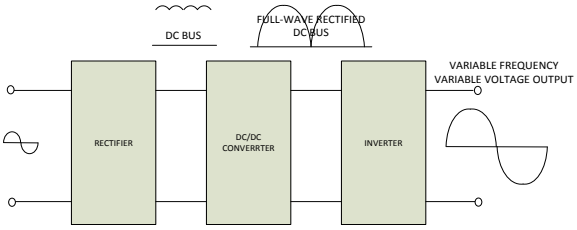


Figure 3-1 Block Diagram of Topology E

3.1. Three Isolated Converters

The simplest way to obtain three phase sine wave is to use three converters which is described in topology E for each phase. However, isolation of the converters is required since a short circuit path is created if they are not isolated. This short circuit path will be described in detail. Isolation can be maintained by three ways: using isolation transformer at the output, using isolated DC/DC converter or using isolated DC link voltages(by using 3 isolated PFC or input power transformer).

3.1.1. The Operation Principle

The circuit diagram of three converters is shown in Figure 3-2. Three converters are used to produce one phase and they are tied from middle point of one half of full bridge. Other half of full bridge is connected to load.

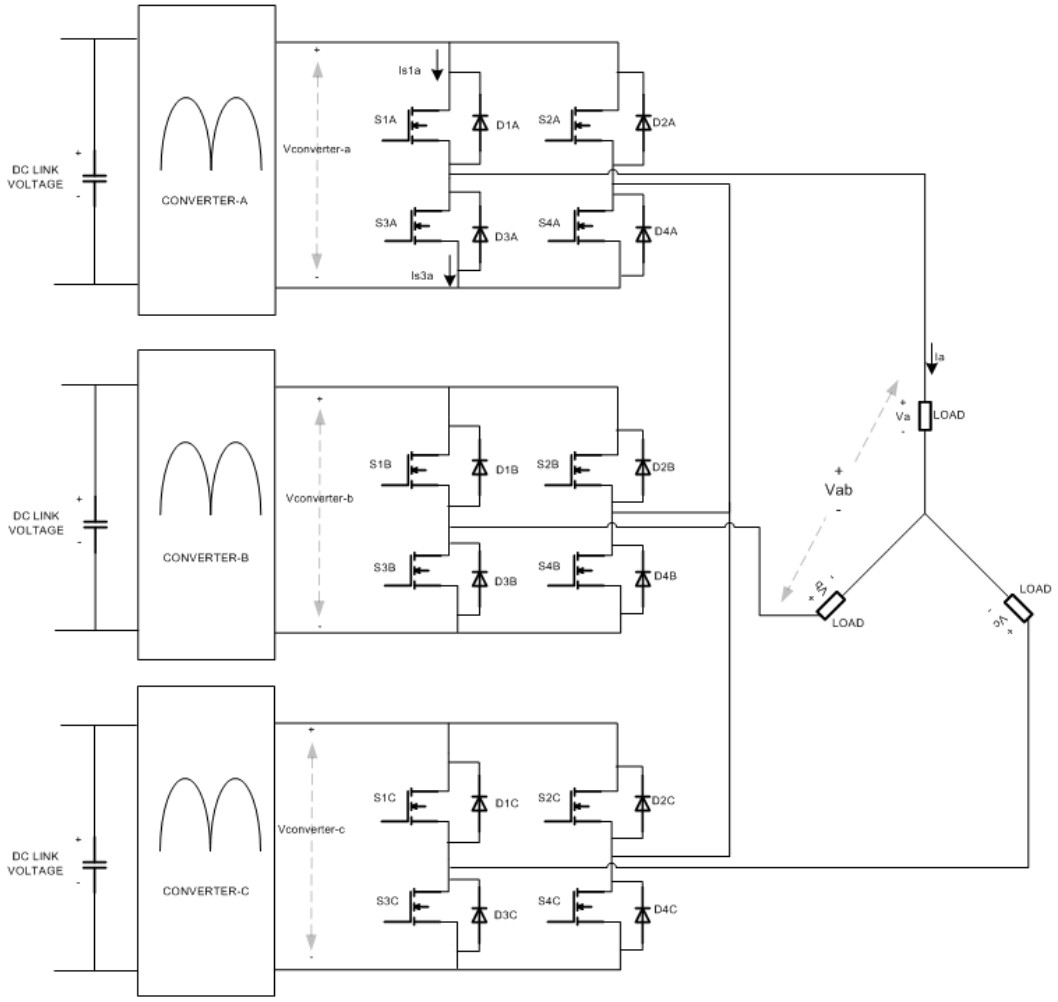


Figure 3-2 Circuit Diagram of Three Isolated Converters

Waveforms of Converter-A voltage, Converter-B voltage, Converter-C voltage, phase voltages V_a, V_b, V_c and line to line voltage V_{ab} are shown in Figure 3-3.

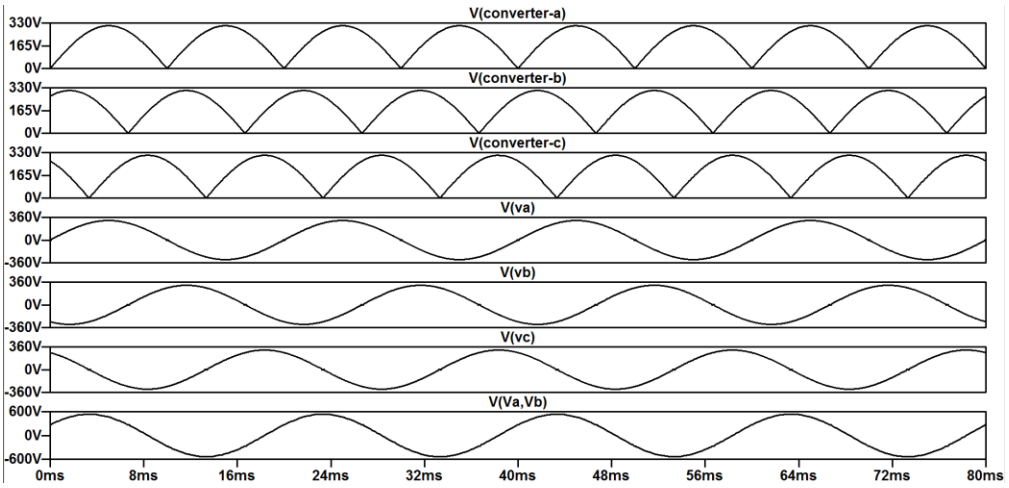


Figure 3-3 Waveforms of Converter-A voltage, Converter-B voltage, Converter-C voltage, phase voltages V_a, V_b, V_c and line to line voltage V_{ab} respectively from top to bottom

Waveforms of Converter-A voltage, phase voltage Va, switch current of S1A, switch current of S2A, switch current of S3A, switch current of S4A and load current of phase A are shown in Figure 3-4. For phase A, current waveforms are shown in Figure 3-4. For one half cycle S1A and S4A conducts and for one half cycle S2A and S3A conducts. The other phases are delayed version of phase A. Fullwave rectified waves are inverted to produce sine waves. The period for each supply is T/2 since it is full wave rectified of sine wave. The converter output voltages are delayed by T/3 time where T is period for desired frequency at the output.

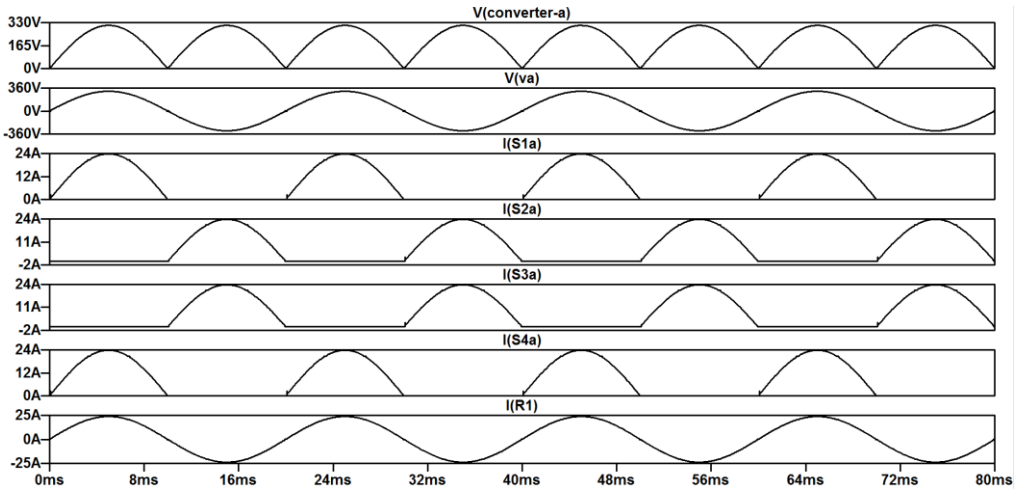


Figure 3-4 Waveforms of Converter-A voltage, phase voltage V_a, switch current of S1A, switch current of S2A, switch current of S3A, switch current of S4A and load current of phase A respectively from top to bottom

The switches shown in Figure 3-2 may be slow switches. For resistive load switching is done at zero voltage and zero current. For inductive load switching is done at zero voltage but not at zero current.

Table 3-1 Switching Time of Inversion Stage Switches

TIME	**0 to 3.333m**	**3.333m to 6.667m**	**6.667m to 10m**	**10m to 13.333m**	**13.333m to 16.667m**	**16.667m to 20m**
Conducting Switches of Phase A	S1A,S4A	S1A,S4A	S1A,S4A	S2A,S3A	S2A,S3A	S2A,S3A
Conducting Switches of Phase B	S2B,S3B	S2B,S3B	S1B,S4B	S1B,S4B	S1B,S4B	S2B,S3B
Conducting Switches of Phase C	S1C,S4C	S2C,S3C	S2C,S3C	S2C,S3C	S1C,S4C	S1C,S4C

3.1.2. Short Circuit Problem

Closer inspection reveals that unless the individual converters are isolated the arrangement given in Figure 3-2 has no practical value. This problem is illustrated in Figure 3-5. Individual converters switch independently to produce a sinus output voltage, as described in Table 3-1. Therefore, for example there comes an instant whereby switches S4A, S2B, S4C are in conduction and a short circuit occurs as shown by the thick solid current flow path in Figure 3-5. And different short circuit paths are created in different times. This finding suggests that individual converters must be electrically isolated from each other if the arrangement in Figure 3-2 is used for producing three-phase output. Isolation can be achieved in several manners;

- A power frequency input transformer can be used.

- An output transformer can be used for each converter.
- An isolated converter topology may be used for producing the full-wave rectified waveform.

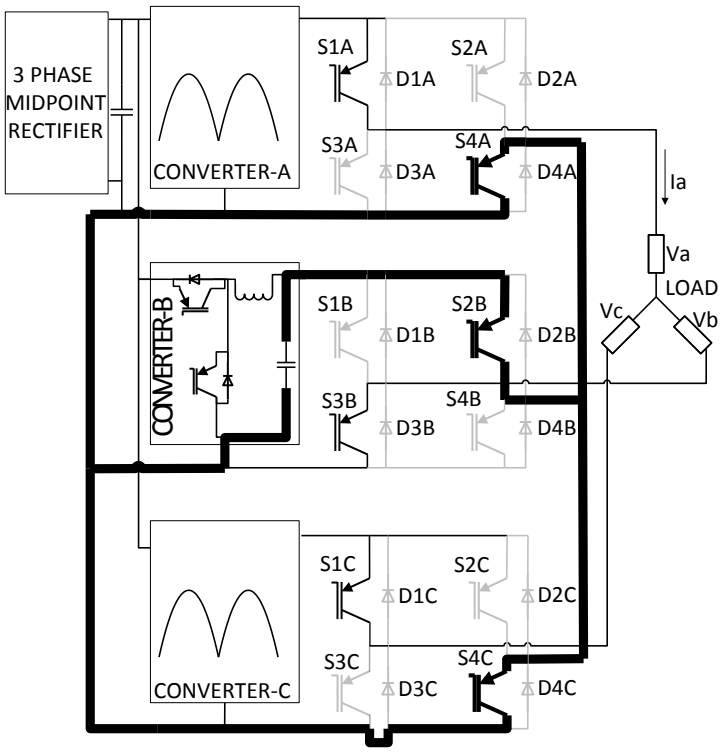


Figure 3-5 Short Circuit Path in Buck Converters

Each of these solutions has serious drawbacks. For example, if power frequency transformers are used on the input side the size of the resulting converter would be very large as well as its volume and the cost would seriously increase.

In solution (b) the output transformer is subject to variable frequency output and this would require a special transformer and the size of this transformer would be large as well.

The only practical solution for obtaining isolation appears to be using a converter topology employing a high frequency transformer, which provides the required isolation. For example flyback converter may be used for this purpose which is the modified version of topology B described in Chapter 2. Figure 3-6 illustrates how the

short circuit path is avoided using such a converter topology. As illustrated in this figure, the transformer before the inversion stage provides the required electrical isolation and prevents a short circuit.

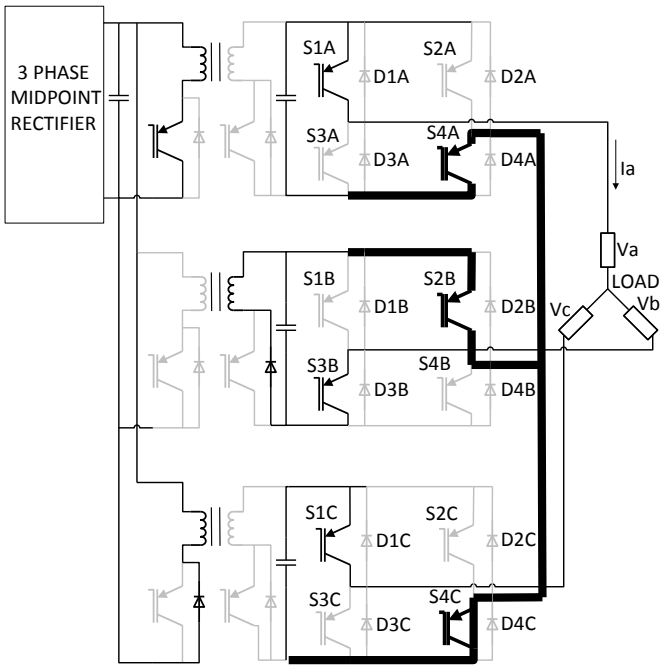


Figure 3-6 Flyback Converter Avoids Short Circuit Path

If flyback converter is to be used then converter may also have boost capability. It is possible to obtain higher output voltage by adjusting transformer turns ratio.

3.1.3. Switch Ratings

In this topology, phase voltages are obtained by using three converters and inversion stage. Voltage ratings of switches at the converter stage and inversion stage are equal to peak output voltage level of phase voltage.

3.1.4. Loss and Efficiency Analysis

Loss and efficiency analysis for this topology is done in section 3.9. The advantage of this topology is the ability to operate from lower input voltage. It requires isolation of the converters. In efficiency analysis it is assumed that they are fed from isolated supplies.

3.2. Two Isolated Converters

Three phase sine waves are delayed by T/3 from each other. By using open delta connection, three phase sine waves can be obtained by two sine waves which are delayed by T/6. In this section, two converters of topology E are used. By using two converters which produce V_{ac} and V_{bc}, three phase sine wave can be obtained.

3.2.1. Operation Principle

Positive terminal of V_{ac} is connected to phase A, positive terminal of V_{bc} is connected to phase B and negative terminals of the output stage of converters are connected to phase C. Therefore, with two converters which produce full wave rectified sine waves, three phases can be obtained. The circuit diagram of this output topology is shown in Figure 3-7. The converters must be isolated because of same reason which is described in section 3.1. Waveforms of Converter-A voltage, Converter-B voltage line to line voltages Vab, Vbc, Vca are shown in Figure 3-8. Waveforms of Converter-A voltage, Converter-B voltage, load current of phase A, switch current of “S1A, S4A”, switch current of “S2A, S3A” are shown in Figure 3-9. Fullwave rectified waves are inverted to produce sine waves.

The switches shown in Figure 3-7 may be slow switches. Switching is done at zero voltage but not at zero current.

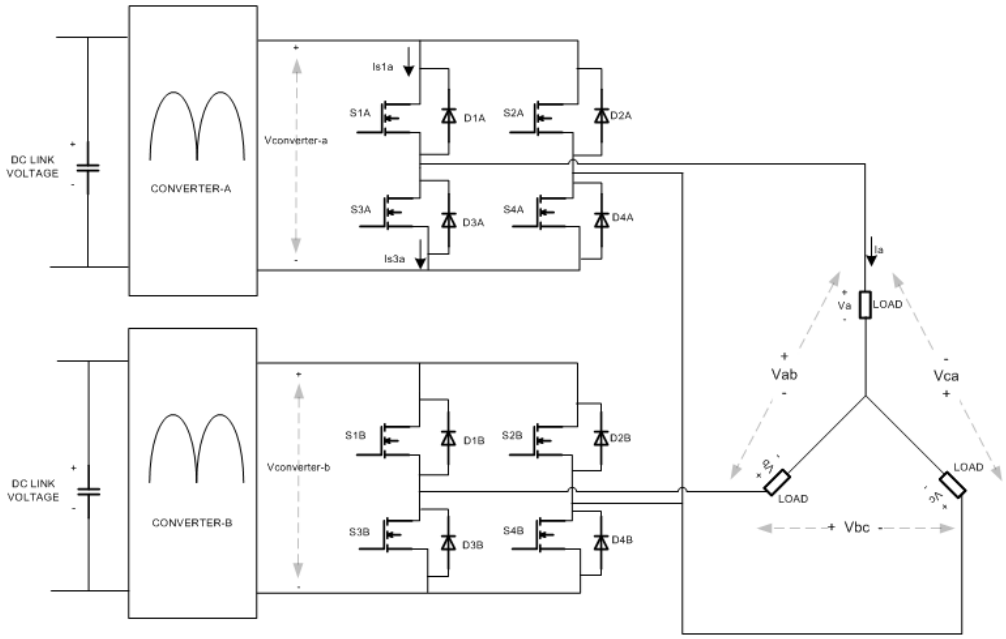


Figure 3-7 Circuit Diagram of Two Isolated Converters

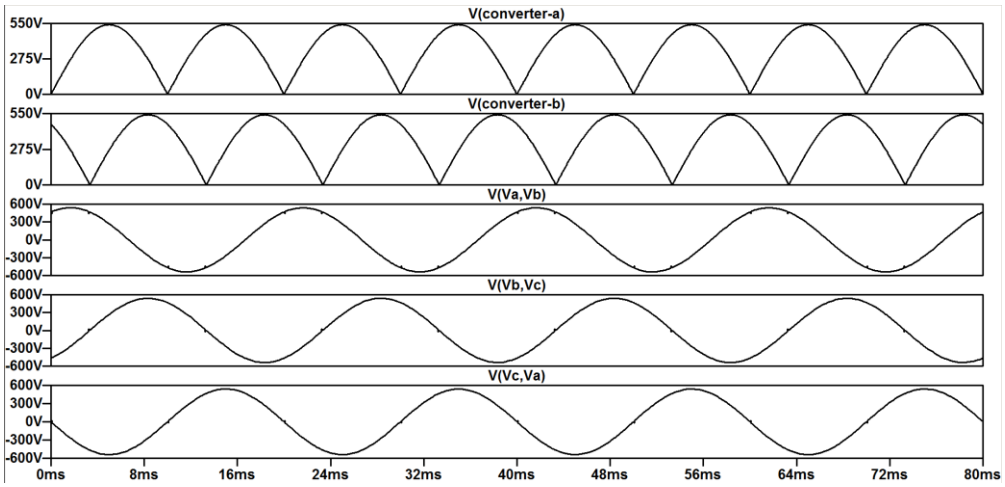


Figure 3-8 Waveforms of Converter-A voltage, Converter-B voltage line to line voltages V_{ab}, V_{bc}, V_{ca} respectively from top to bottom

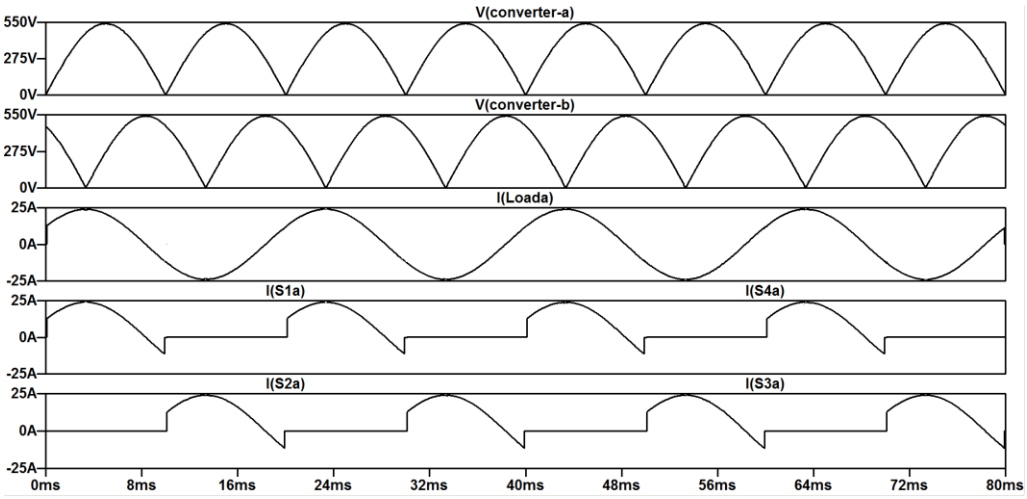


Figure 3-9 Waveforms of Converter-A voltage, load current of phase A, switch current of "S1A,S4A" and switch current of "S2A,S3A" respectively from top to bottom

Table 3-2 Switching Time of Inversion Stage Switches

TIME	0 to 3.333m	3.333m-4.5m	5m-8.333m	5m-10m	10m-13.333m	13.333m-14.5m	14.5m-18.333m	18.333m-20m
Conducting Switches of Converter A	S1A S4A	S1A S4A	S1A S4A	D1A D4A	S2A S3A	S2A S3A	S2A S3A	D2A D3A
Conducting Switches of Converter B	S2B S3B	D1B D4B	S1B S4B	S1B S4B	S1B S4B	D2B D3B	S2B S3B	S2B S3B

3.2.2. Short Circuit Problem

This topology also requires isolation of the converters. The reason is same with previous topology which is described in section 3.1. For example, at an instance switch S4A and S2B conduct as shown in Table 3-2 and creates a short circuit path.

3.2.3. Switch Ratings

In this topology, phase voltages are obtained by using two converters and inversion stage. Voltage ratings of switches at the converter stage and inversion stage are equal to peak output voltage level of line to line voltage.

3.3. Two Nonisolated Converters

Topologies described in sections 3.1 and 3.2 require isolation of the converters. Isolation requires additional components and its disadvantages are described in section 3.1.2. In this section, a topology which does not require isolation is proposed and analyzed.

3.3.1. The Operation Principle

This topology requires two converters, which produce waveforms in the form of full wave rectification of two phases of three phase system. In Figure 3-10, connections of the converters to phases are shown. Each interval positive terminal of one converter is connected to one phase, positive terminal of other converter is connected to one phase and negative terminals of both converters is connected to one phase.

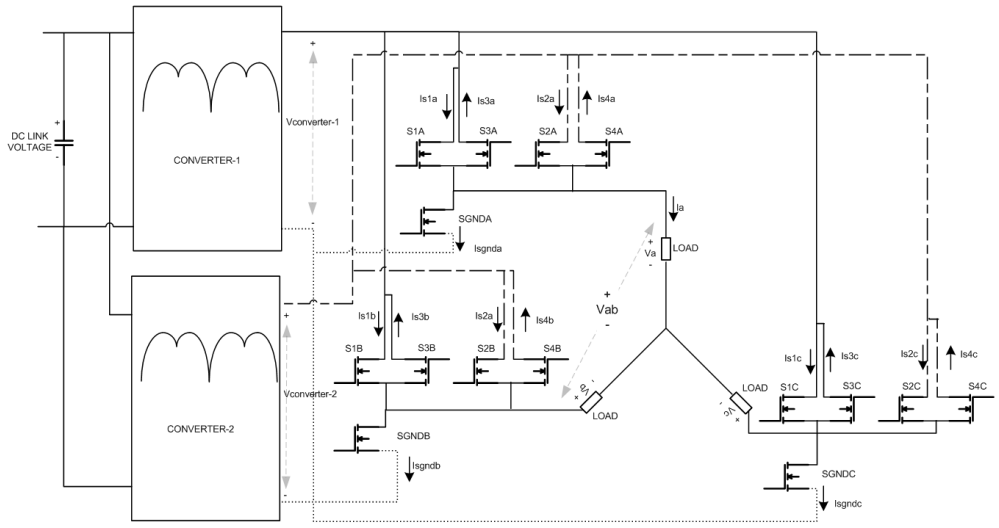


Figure 3-10 Circuit Diagram of Two Nonisolated Converters

Waveforms of Converter-1 voltage, Converter-2 voltage, phase voltages V_a, V_b, V_c and line to line voltage V_{ab} respectively from top to bottom are shown in Figure 3-11. Phase voltage are not sinusoidal, the phase voltage waveforms are shown with respect to negative terminal of DC link. The phase voltage waveforms contain "twin peaks". Although phase voltages are not sinusoidal, line to line voltages are sinusoidal. For each phase there are five switches, two of the switches are connected to positive output terminal of converter-1, two of the switches are connected to positive output terminal of converter-2 and one switch is connected to negative terminals of both converters. Switches connected to positive output terminals of converters must not contain internal body diode since they must block reverse current path.

Output phases are connected to converters through five switches to obtain waveforms shown in Figure 3-11. Although phase voltages do not seem to be sinusoidal, line to line voltages become sinusoidal. To illustrate, phase voltage V_a, load current of phase A, switch current of S1A, switch current of S3A, switch current of S2A, switch current of S4A and switch current of SGNDA are shown in Figure 3-12 . S1A and S3A are both connected to converter-1, the only difference is the conducting way. S1A conducts from converter to load and S3A conducts from load to converter.

Same thing is true for S2A and S4A. S2A and S4A are both connected to converter-2, the only difference is conducting way. S2A conducts from converter to load and S4A conducts from load to converter.

The switches shown in Figure 3-10 may be slow switches. Switching is done at zero voltage but not at zero current.

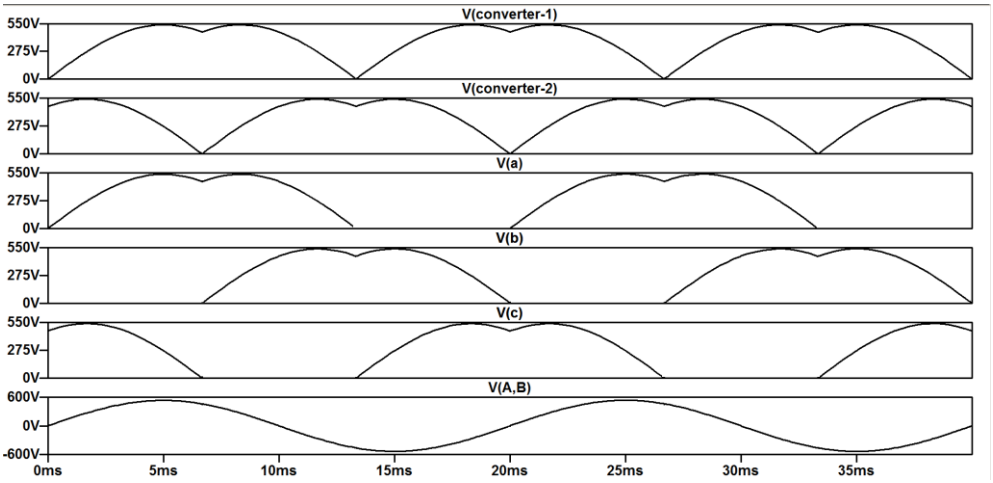


Figure 3-11 Waveforms of Converter-1 voltage, Converter-2 voltage, phase Voltages V_a, V_b, V_c and line to line voltage V_{ab} respectively from top to bottom

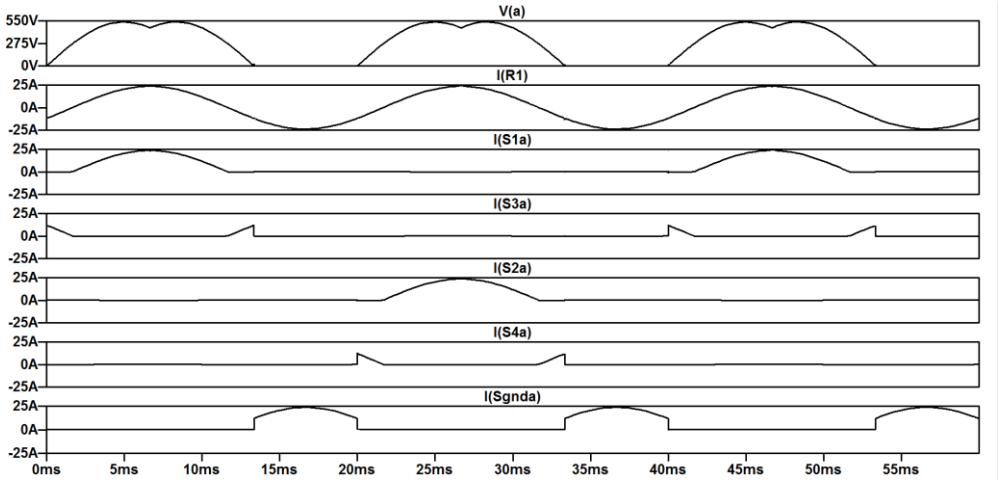


Figure 3-12 Phase voltage V_a, load current of phase A, switch current of S1A, switch current of S3A, switch current of S2A, switch current of S4A and switch current of SGNDA respectively from top to bottom

Table 3-3 Switching Time of Inversion Stage Switches of Phase A

TIME	0 to 1.667m	1.667m to 11.667m	11.667m to 13.333m	13.333m to 20m	20m to 21.667m	21.667m to 31.667m	31.667m to 33.333m	33.333m to 40m
Conducting Switches of Phase A	S3A	S1A	S3A	SGNDA	S4A	S2A	S4A	SGNDA

As it can be observed in Figure 3-12 , switches connected to positive terminal of the converters conduct in one period and does not conduct in one period. Thus, they conduct once each two period. However, the switch connected to negative terminals conducts each period.

3.3.2. Switch Ratings

In this topology, phase voltages are obtained by using two converters and inversion stage. Voltage ratings of switches at the converter stage and inversion stage are equal to peak output voltage level of line to line voltage.

3.4. Three Non-Isolated Converters

The topology described in section 3.3, i.e. “two non-isolated converters” requires many switches at its output stage. In Figure 3-11, it is observed that three phase sine waves can be obtained by using three converters which produce V(a), V(b) and V(c) voltage waveforms with twin peaks as in the figure. Note that in this case the stage which is used to invert the half wave DC bus voltage to obtain sine-wave output can be removed saving 4 switches in each phase. Therefore, it is decided to investigate a topology which synthesizes sine wave using a DC bus with “twin-peak” repetitive voltage pulses is investigated in this section.

Thus converter output voltage waveforms are similar for the topology described in this section and the topology described in section 3.3.

3.4.1. The Opereation Principle

This method requires three DC/DC converters. Output terminal of each converter is tied to one phase. In Figure 3-13, block diagram of this topology is shown.

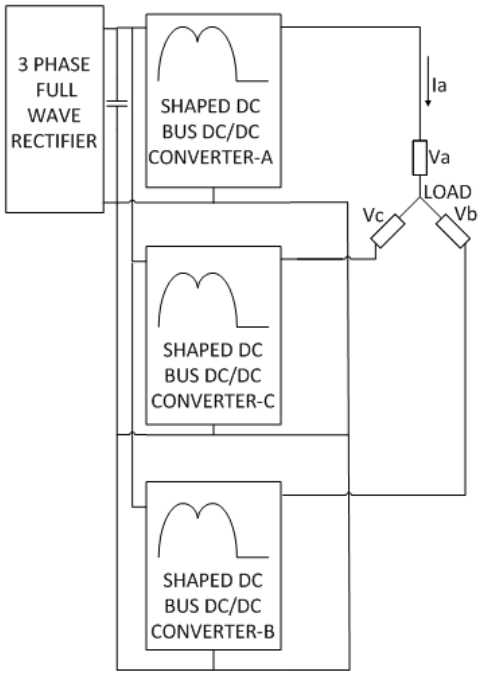


Figure 3-13 Block Diagram of Three Non-Isolated Converters

The converters are made to follow reference signal to obtain three phase output. Output voltage waveforms of converters are shown in Figure 3-14. Each converter operates during 2T/3 time where T is fundamental output period.

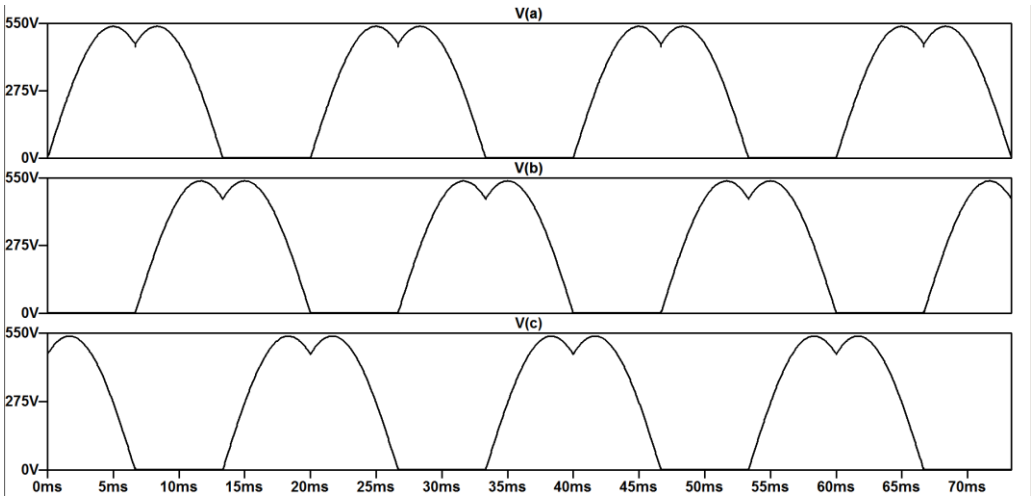


Figure 3-14 Output Voltages Waveforms of Converters

Phase a, phase b and line to line voltage V_{ab} is shown in Figure 3-15. As it can be observed from the figure, sine wave V_{ab} is generated by using two converters whose outputs are shown with V(a) and V(b). Line to line voltages are shown in Figure 3-16. Three phase sine wave is generated by three converters.

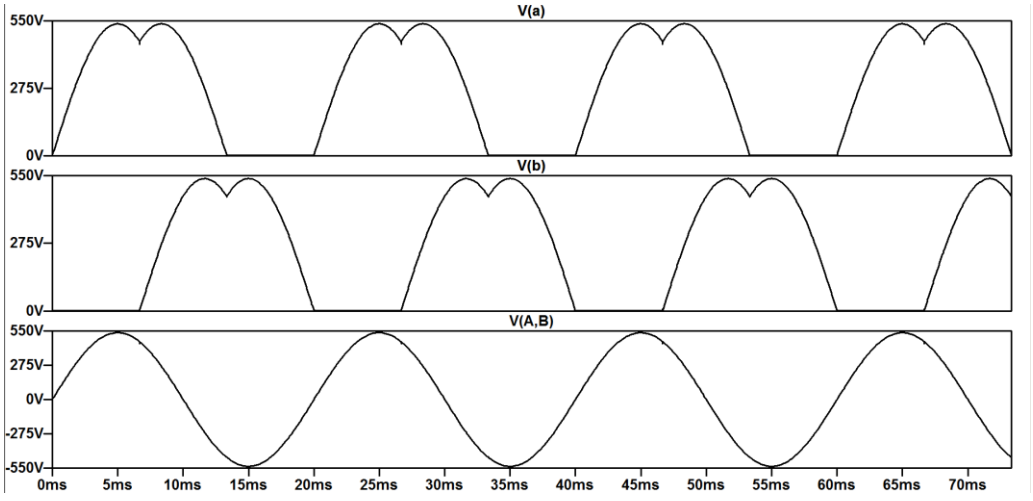


Figure 3-15 Phase A Output Voltage, Phase B Output Voltage and V_{ab} Line to Line Voltage Waveforms

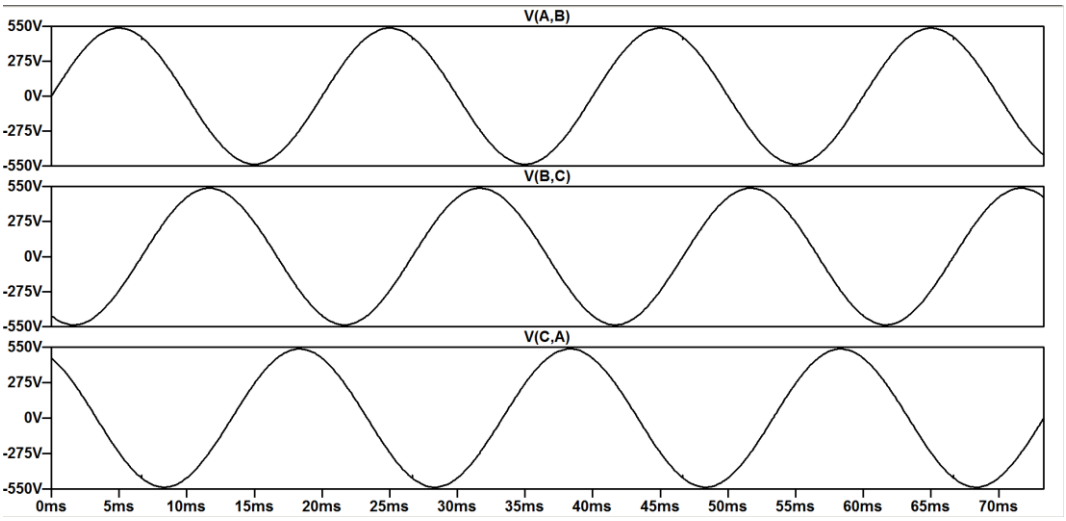


Figure 3-16 Line to Line Voltage Waveforms

Circuit diagram of this topology is shown in Figure 3-17. Three buck converters are used to create three phase waveform. It is very similar to classical full bridge with LC filter except position of the capacitor. In classical method capacitor is tied delta or Y to output phases, in this method capacitors are tied between phases and negative terminal of input. Six fast switches are required in total.

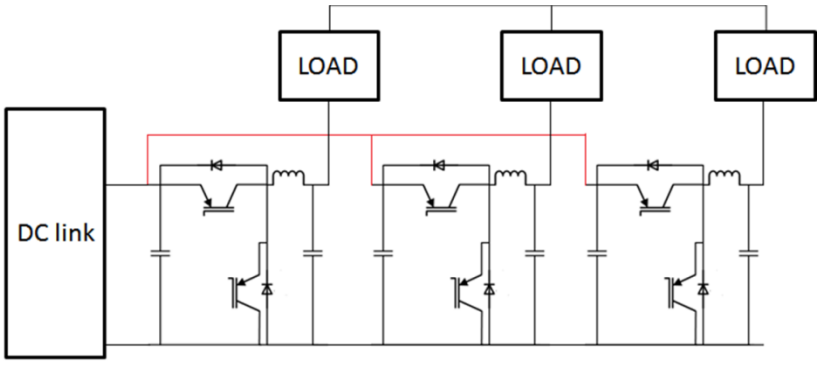


Figure 3-17 Circuit Diagram of Three Buck Converters

3.4.2. Switch Ratings

In this topology, phase voltages are obtained by using three converters. Voltage ratings of switches at the converter stage are equal to peak output voltage level of line to line voltage. Additional inversion stage is not required.

3.4.1. Loss and Efficiency Analysis

Loss and efficiency analysis for this topology is done in section 3.8. The advantage of this topology is that it does not require additional inversion stage.

3.5. Comparison of Switch Requirements

All topologies contain buck converter if we discard the need of isolation. In Table 3-4 fast switch count and voltage ratings of those switches are shown. And in Table 3-5, inversion stages are compared according to switch count, switch voltages, switch currents and zero voltage switching. Switches referred in Table 3-5 are slow switches. V_{outrms} is phase voltage.

Table 3-4 Required Fast Switch Quantities

	Switch Quantity	Switch Voltages
Three Isolated Converters	6	$V_{outrms}*\sqrt{2}$
Two Isolated Converters	4	$V_{outrms}*\sqrt{6}$
Two Non-isolated Converters	4	$V_{outrms}*\sqrt{6}$
Three Non-isolated Converters	6	$V_{outrms}*\sqrt{6}$

Table 3-5 Required Slow Switch Ratings

	Switch Quantity	Switch Voltages	Switch Currents	Zero Voltage Switching
Three Isolated Converters	12	$V_{outrms}*\sqrt{2}$	$I_{outpeak}$	Yes
Two Isolated Converters	8	$V_{outrms}*\sqrt{6}$	$I_{outpeak}$	No
Two Non-isolated Converters	15	$V_{outrms}*\sqrt{6}$	$I_{outpeak}$	Yes
3 Non-isolated Converters	0			

When we observe Table 3-4 and Table 3-5, three Isolated Converters have less voltage on switches, thus it will decrease the switching losses on fast switches. Its disadvantage is the requirement of the isolation.

Two Isolated Converters seems to decrease fast switch count but it also requires isolation. To isolate converter stage must be changed, additional components are required and losses increase.

Two Non-isolated Converters seems to be appealing since it decreases fast switch count and does not require isolation but additional fifteen slow switches required in the inversion stage makes it unprofitable.

Three Non-isolated Converters does not require inversion stage, but the topology is very similar to classical full bridge and LC filter added at the output. The difference is capacitor connection of the filter.

Three Non-isolated Converters seem to be optimum thus further analysis and simulations are done to compare three Non-Isolated Converters and classical method(three phase full bridge) plus LC filter.

3.6. Simulation and Loss Calculation Method

To calculate losses “LT-Spice 4” simulation program is used. Simulated circuit diagram is shown in Figure 3-18. During simulations input voltage switches and diodes are kept constant, only capacitor and inductor values are changed.

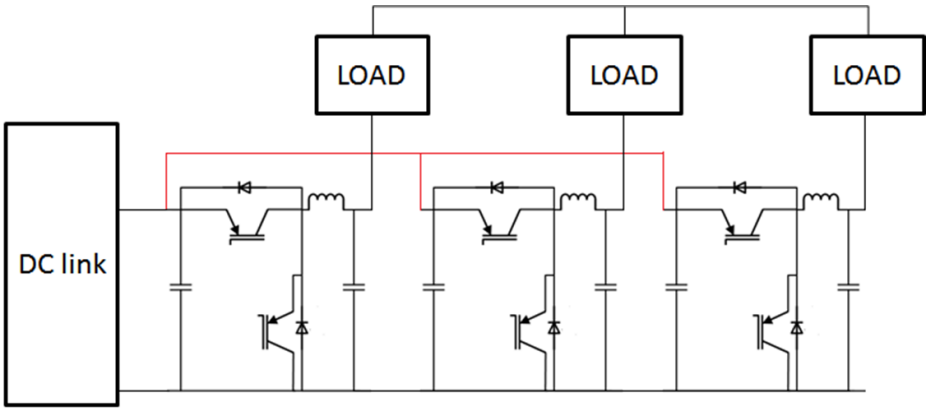


Figure 3-18 Simulated Circuit Diagram for Three Non-Isolated Converters

3.6.1. Capacitor Loss Calculation

Various capacitor manufacturers are searched and dissipation factor of capacitors are analyzed. For low ESR capacitors, dissipation factor is mostly given to be lower than 0.1%. Since they are similar, one of them is chosen and used in the simulations.

For capacitor (C1) TDK B3236 series capacitor parameters are simulated. Capacitor ESL and ESR, and dissipation values are looked from a manufacturer. Table 3-6 shows capacitor capacitance, ESR at 100Hz, self-inductance.

Dissipation Factor=DF=ESR/XC=0.001 at 100Hz

For example: ESR at 10kHz of 10uF capacitance is calculated by multiplying ESR value at 100Hz by 100. Thus ESR at 10kHz equals to 480mΩ.

Table 3-6 Capacitor Parameters

C(uF)	ESR(mΩ)	Lself(nH)
10	4,8	195
15	4,1	195
20	4,3	195
25	5,2	220
30	4,8	220
40	6,6	225
50	6	225

3.6.2. Inductor Loss Calculation

For inductor (L3), model with hysteresis loss is used. This model defines the inductance by its core parameters. Spice program uses "Nonlinear Transformer Model for Circuit Simulation"[16]. In this model Coercive force (H_c Amp-turns/meter), Remnant flux density (B_r Tesla), Saturation flux density (B_s Tesla) define core material parameters. Gap length (L_g) defines gap length in meters, N defines the turn number, A defines core area in m^2, L_m defines magnetic length. R_{ser} is equivalent series resistance of the inductor. For required current level, typical core area, gap area, magnetic length and turn number is calculated and they are changed for different simulations.

ESR value is calculated by multiplying resistance per unit length by turn number and mean turn length.

B_s,B_r and H_c values are looked from datasheet.

3.7. Filter Design for Simulation

In this section, filter design will be explained. First LC product is calculated to satisfy THD of output voltage. Then inductor current relationship with capacitor is calculated. Filter values are calculated for minimum loss and minimum cost.

3.7.1. LC Product Calculation

Output Voltage is 310Vp for one phase. If %1.5 percent ripple is allowed then ripple is 4.65Vp. The supply is switching with constant frequency at 10kHz. In their paper, Michael Salcone and Joe Bond show that maximum ripple occurs at 50% duty cycle and ripple value is calculated by equation 3.1[17]. LC product is shown on equation 3.2.

$$\Delta V_{D=0.5} = \frac{V_{bus}}{(32*L*C*f^2)} \quad (3.1)$$

$$L * C = 3.63 * 10^{-8} \quad (3.2)$$

3.7.2. Inductor Current Calculation

In Figure 3-19, output voltage waveform, output current waveform and output capacitor current waveform of one converter are shown. Inductor current is equal to sum of output current and capacitor current. As it can be observed, at T/3 inductor current becomes maximum. Period T=20ms in Figure 3-19.

Capacitor current at T/3 can be calculated as:

$$I_C = C * \frac{dV_C}{dt} \quad (3.3)$$

Voltage waveform for 0 to T/3 can be defined by

$$Vc = 540 * sin\left(\frac{2*\pi*t}{T}\right) \quad (3.4)$$

$$\frac{dVc}{dt} = 540 * \frac{2*\pi}{T} sin\left(\frac{2*\pi*t}{T}\right) \quad (3.5)$$

If T=20ms;

$$\frac{dVc}{dt}\left(\frac{T}{3}\right) = -84.823k \quad (3.6)$$

There is a breakpoint at T/3, for slightly higher values than T/3 dv/dt=84.823k. Then current rating for inductor is equal to;

$$I_{Lmax} = I_{outpeak} + 84.823k * C \quad (3.7)$$

$I_{outpeak}$ is equal to 11.78A for 5.5kW output at 380V line to line voltage.

$$I_{Lmax} = 11.78 + 84.823k * C \quad (3.8)$$

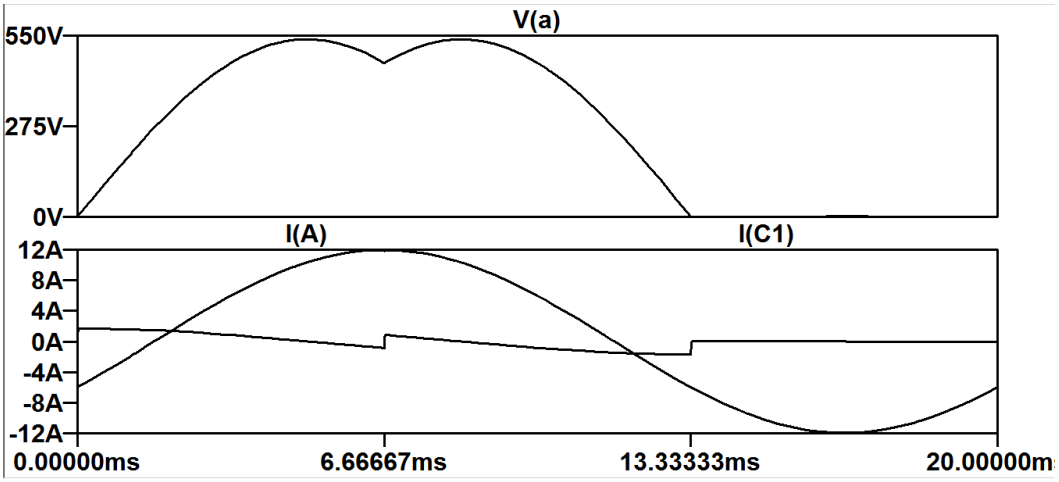


Figure 3-19 Output Voltage Waveform

3.7.3. Commercial, Minimum Cost, Minimum Loss Filter

Three types of LC filter are evaluated. Some commercial filters are searched through internet. Minimum cost and minimum loss filter values are calculated.

3.7.3.1. Commercial Filters

Inverter output filters for 5.5kW are searched in the internet and 3 parts are found:

REO Inductive Components CNW M 933 / 12 / IP (12A, 4,9mH 1,1uF 7,2kg)

Danfoss 130B2411 (17A,3.1mH 10uF 150W dissipation)

SHAFFNER FN 5040-17-83 (17A, 3.1mH 10uF 115W dissipation)

3.7.3.2. Minimum Cost Filter

Cost calculation method is described in Chapter 2. Inductor cost is dependent on inductance and current rating. Amorphous core and solid round wire is assumed to be used. In equation 2.3, cost calculation formula for inductor is shown. Parameters are looked from Table 2-3. Since inductor cost model is based on weight of core and winding. To compare costs, weights of core and winding must be found for given inductance L and current rating of inductor. By using equation 2.4 core area and winding are product is obtained. Assuming A_{core} and A_{wdg} equal and square, core volume and winding volume is found. Mass is obtained by multiplying material density with volume. Inductor cost with respect to inductance and current is shown in equation 3.9.

$$Inductor\ Cost = 21.28 * L^{0.87} * I^{1.74} + 3 \quad (3.9)$$

In equation 2.2, cost model for film capacitor is given. Film capacitor is assumed to be used. Capacitor cost with respect to capacitance in uF is shown in equation 3.10.

$$Capacitor\ Cost = 31.9516 + 2.426 * 10^{-3} * C \quad (3.10)$$

$$Total\ Cost = 21.28 * L^{0.87} * I^{1.74} + 3 + 31.9516 + 2.426 * 10^{-3} * C \quad (3.11)$$

Peak inductor current with respect to capacitance is calculated in equation 3.8. LC product is shown in equation 3.2. L and I values in equation 3.11 are replaced as functions of capacitance. Thus total cost is obtained as a function of capacitance. By sweeping capacitance value between 1uF and 10mF, cost graph with respect to capacitance is obtained and shown in Figure 3-20. Minimum cost occurs at 123uF and 294uH which results in 41.53€ for one phase. For 100uF capacitance, inductance value is 363uH and cost is 41.6€ for one phase.

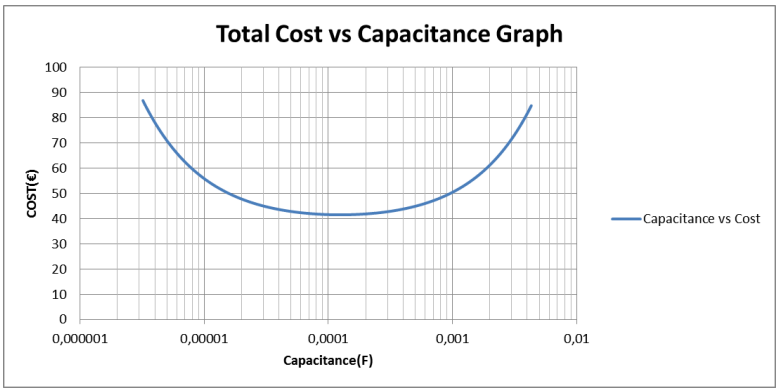


Figure 3-20 Total Cost vs Capacitance Graph

3.7.3.3. Minimum Loss Filter

To obtain minimum loss filter parameters, MATLAB program is used. Since output voltage is not constant, losses are not always constant. Thus assuming switching frequency is 10kHz, one period(20ms for 50 Hz operation) is divided into parts of 100us. In each switching cycle, output voltage value, output current value, capacitor mean current value, inductor mean current value, inductor ripple current value and capacitor current value are calculated. Power loss is integrated for one period and average power loss is found for one period. For a LC value, total loss is calculated. L and C values are swept and minimum loss filter values are found.

Inductor loss can be divided into core loss and copper loss. Core Loss is formulated by approximating values shown in core loss graph for 10kHz[18].

Inductor current has two components, low frequency component and high frequency component. Low frequency components are formed by load and capacitor. High frequency component is due to switching. For a switching cycle inductor current may be assumed to be triangular current which is formed of DC current at a value equal to low frequency component plus ripple current. Power loss of triangular current on a resistor is given by 3.12.

$$\text{Copper Loss} = R * \left[I_{DC}^2 + \frac{I_{AC}^2}{12}\right] \quad (3.12)$$

Capacitor loss is calculated similar to inductor copper loss; its current has DC and AC components.

Total capacitor and inductor loss for one phase is swept with respect to inductance value and it is shown in Figure 3-21.

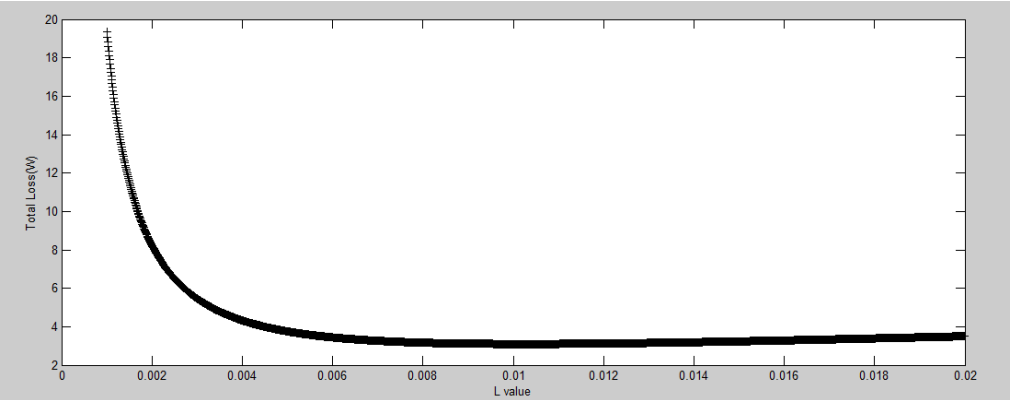


Figure 3-21 Total Loss vs Inductance Graph

Minimum Loss is obtained at 10.1mH and 3.52uF. Price of minimum Loss Filter is 82€.

3.8. Simulation Results of Three Non-isolated Converters and Classical Inverter with Filter

Different capacitor values and inductor values are simulated. 9 simulations are done at total and results are shown in Table 3-7.

In Table 3-7;

- Pout: three phase output power
- Pin: three phase input power
- Converter Efficiency: This values is three phase efficiency of the converter and equals to output power divided by input power
- Lloss: three phase inductor loss

- Closs: three phase capacitor loss
- THD: 1000 harmonic component of 50Hz are calculated and THD is found.

9 different simulations are done:

Three non-isolated converters, classical inverter with delta connected filter, classical inverter with star connected filter for minimum cost LC filter.

Three non-isolated converters, classical inverter with delta connected filter, classical inverter with star connected filter for minimum loss LC filter.

Three non-isolated converters, classical Inverter with delta connected filter, classical inverter with star connected filter for commercial LC filter.

Table 3-7 Simulation Results of Topologies with Different Filter Types

	Simulation	C(uF)	L(mH)	Pout (W)	Pin (W)	η(%)	Lloss (W)	Closs (W)	THD (%)
Minimum Loss Filter	3 Non-Isolated	3,52	10,1	5506,2	5615,7	98,1	6,09	0,13	1,75
	Classical Inverter with Delta filter	3,52	10,1	5747,1	5553,2	98,6	9,26	0,6	1,63
	Classical Inverter with Star filter	3,52	10,1	5399,8	5478	98,6	8,87	1,65	1,51
Minimum Cost Filter	3 Non-Isolated	100	360	5521,8	5770,2	95,7	24,18	62,21	0,86
	Classical Inverter with Delta filter	100	360	5575,2	5969,6	93,4	24,9	121,2	1,45
	Classical Inverter with Star filter	100	360	5493,3	5705,8	96,3	23,28	43,11	1,32
Commercial Filter	3 Non-Isolated	10	3,2	5526,9	5649,9	97,8	10,32	1,37	1,04
	Classical Inverter with Delta filter	10	3,2	5540,5	5660,3	97,9	9,3	2,22	1,23
	Classical Inverter with Star filter	10	3,2	5471,2	5588,9	97,9	8,82	0,81	1,19

In the simulations, L*C product is same for minimum cost and minimum loss filters. Commercial filter L*C product is slightly smaller. For same L*C product, it is observed that increasing L value decreases losses. This is due to decreasing of ripple current. When ripple current decreases, losses also decrease. Minimum cost filter contains least amount of inductance, thus its ripple current and losses are higher. Minimum loss filter contains highest amount of inductance, and its losses are lower than other simulated filters. Increasing inductance value also worsens the transient response since current cannot change quickly. When Table 3-7 is observed, commercial filter values seem optimum, its THD is less, efficiency is high enough and fundamental voltage is higher.

When the topologies are compared for same type of filter, they show similar results. It is hard to say one of them is better than others. Three non-isolated converters seem to have less THD for same filter values except minimum loss. Its efficiency seems to be slightly lower. Fundamental voltages are similar.

3.9. Efficiency Comparison of Simulated Topologies

Since three non-isolated converters did not show much better characteristic than classical method, additional analysis is done on three isolated converters which is described in section 3.1. The aim is to see the losses to decrease when input voltage is lower. Table 3-8 shows efficiencies of simulated topologies. It is seen that three isolated converters does not increase efficiency.

Table 3-8 Efficiency Comparison of Topologies

Topology	**Efficiency (%)**
Three Non-Isolated Converters	97,8
Classical Method with LC filter tied in delta configuration	98,3
Classical Method with LC filter tied in Y configuration	98,3
Three Isolated Converters	97,4

Power loss of each component of three isolated converters and classical inverter with filter is examined and compared. It is assumed that input supplies of three isolated converters are isolated. Circuit diagram for one phase of three isolated converters is shown in Figure 3-22. Power loss of each component is shown in Table 3-9. Simulations are done for three phase, however in Table 3-9, power and loss values are shown for one phase. Total loss can be calculated by multiplying the values in the table by three.

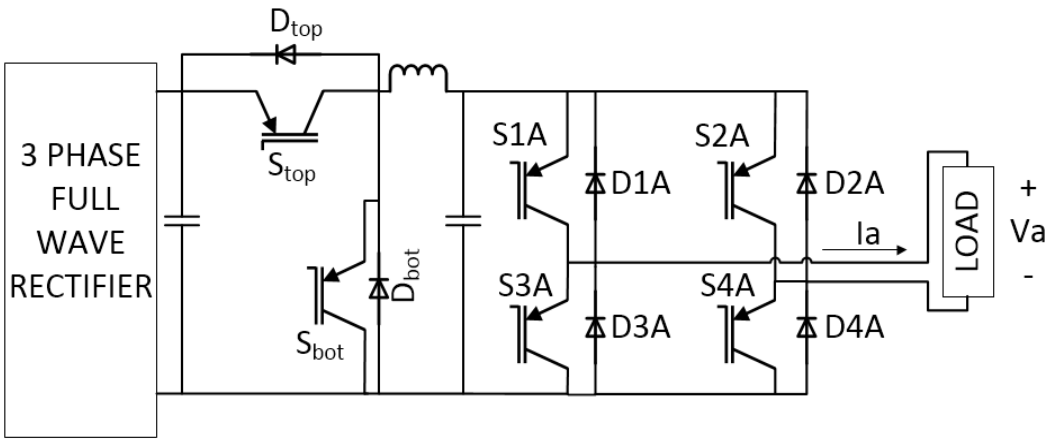


Figure 3-22 One Phase of Three Isolated Converters

Table 3-9 Power Loss of Each Component of Simulated Topologies for One Phase

Component	Three Isolated Converters (W)	Full Bridge + LC Filter (W)
IGBTTop	25,05	23
DTop	0	0,1
IGBTBottom	0,6	12
DBottom	2	0,4
Lcoreloss	1,2	1,63
Lculoss	1,5	0,22
DFW	0	-
C1	0,3	1,01
IGBT1	4,45	-
D1	0	-
IGBT2	4,45	-
D2	0	-
IGBT3	4,45	-
D3	0	-
IGBT4	4,45	-
D4	0	-
Total	48,45	38,36
Output Power	1785,2	1850,6
Input Power	1833,6	1889,2

Although switching losses decrease with Three Isolated Converters, conduction losses added by output stage which is 17,8W, makes total loss more than classical method.

3.10. Summary

In Chapter 2, it is shown that topology E is beneficial for producing single phase sine wave output. In this chapter, it is aimed to obtain three-phase output using the same concept with topology E. Different methods are proposed to obtain three-phase and these are compared. The results show that using topology E for three phase application is not more beneficial than using the classical bridge topology. Efficiency of classical bridge topology is measured to be 0.5% higher with respect to simulation results.

This is because; benefits of topology E for single phase cannot be obtained by three phase application of that topology. In single phase application of topology E, fast switching switch count is decreased. Reduction in fast switch count decreases switching losses and cost. However, in three phase application fast switching switch count cannot be decreased. The “three non-isolated converters” do not require slow switches, however comparison between “three non-isolated converters” and classical method show that this circuit is not beneficial in terms of efficiency and distortion at the output voltage. Two of the topologies considered require isolation, where it is found that isolation increases component count and cost and decreases efficiency. And “two non-isolated converters” require many switches at its inversion stage which complicates the control of switches and increases the total cost thus this topology is not preferable. Therefore, benefits obtained by single phase application cannot be obtained by three phase application of topology E.

In this chapter it is observed that if boosting is not required, classical method of inversion with filter at the output is enough to meet requirements. Other alternative topologies with boosting capability which are described in chapter 2 are further analyzed in next chapter to evaluate their three phase application.

CHAPTER 4

THREE PHASE TOPOLOGIES WITH BOOST CAPABILITY

One aim of this thesis is boosting capability. As discussed in chapter 1, boosting is required in many areas. Therefore this chapter focuses on the possibility of using the single-phase topologies with boosting capability described in Chapter 2, to obtain three-phase output.

Single phase topologies which are described in Chapter 2 are modified to obtain three phase output. One topology which is capable of producing sine wave and boosting is also proposed in this chapter. First, topologies are evaluated according to their component ratings. Then two topologies are further investigated to calculate and compare their cost and efficiency.

4.1. Boost DC-AC

Operating principle of Boost DC-AC topology is described in section 2.1. Figure 4-1 shows the block diagram of boost DC-AC converter. Three phase block diagram is shown in Figure 4-2. Three converters each producing sine wave 120° away from each other are used. Difference between single phase and three-phase, is the quantity of converters and phase difference between them.

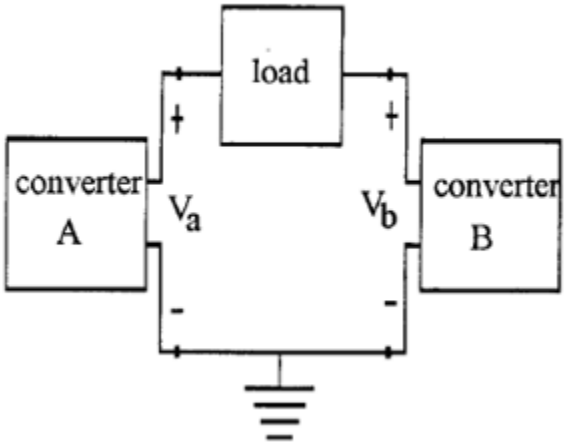


Figure 4-1 Block Diagram of Single Phase Boost DC-AC

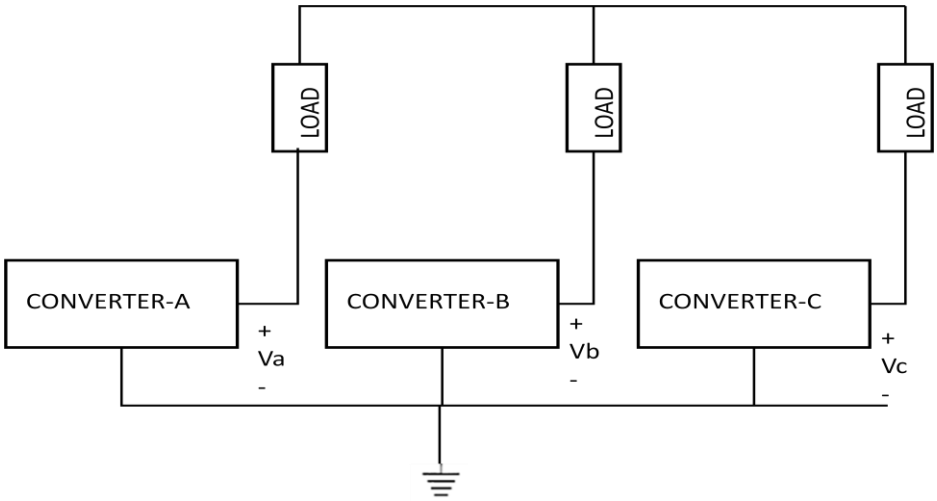


Figure 4-2 Block Diagram of Three Phase Boost DC-AC

4.1.1. Component Requirements

Calculations for voltage and current ratings are described in Chapter 2.

Three capacitors with voltage rating higher than input voltage plus twice output peak voltage is required.

Six fast switches with voltage rating higher than input voltage plus twice output peak voltage is required.

For one phase peak voltage is equal to input voltage plus twice output peak voltage and peak output current passes when output voltage is at maximum value.

$$I_L = \frac{I_{out}}{1-D} \qquad (4.1)$$

$$I_{outpeak} = \frac{P_{out}}{3*V_{outrms}} * \sqrt{2} \qquad (4.2)$$

$$1 - D = \frac{V_{in}}{V_{in}+2*V_{outrms}*\sqrt{2}} \qquad (4.3)$$

$$I_{Lmax} = \frac{P_{out}*\sqrt{2}*(V_{in}+2*V_{outrms}*\sqrt{2})}{3*V_{outrms}*V_{in}} \qquad (4.4)$$

$$I_{Lmax} = \frac{P_{out}*4}{3*V_{in}} + \frac{P_{out}*\sqrt{2}}{3*V_{outrms}} \qquad (4.5)$$

Three inductors with current rating equal to value calculated at equation 4.5 (Zero loss is assumed, output voltage is assumed to be constant at a value V_{outrms}, ripple current is ignored)

4.2. Single Stage Buck Boost

Operating principle of Single Stage Buck Boost topology is described in section 2.4. Figure 4-3 shows the block diagram of this topology. Figure 4-4 shows the modified circuit diagram of one phase to obtain two way power flow. Modifications to obtain three phase are shown in Figure 4-5 [12]. Three converters each producing sine waves 120° away from each other are used. The circuit produces both positive and negative half of sine wave.

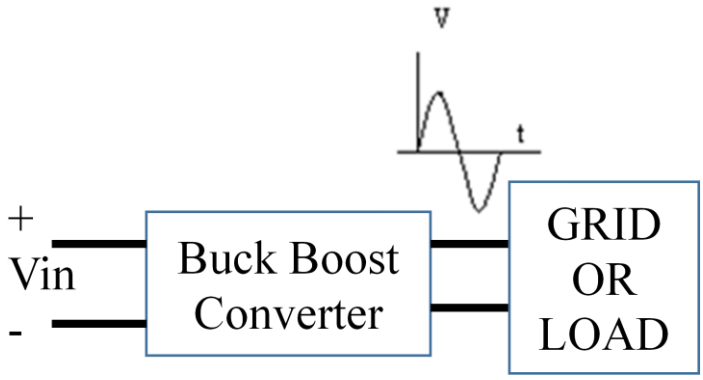


Figure 4-3 Block Diagram of Single Stage DC-AC Buck Boost Inverter

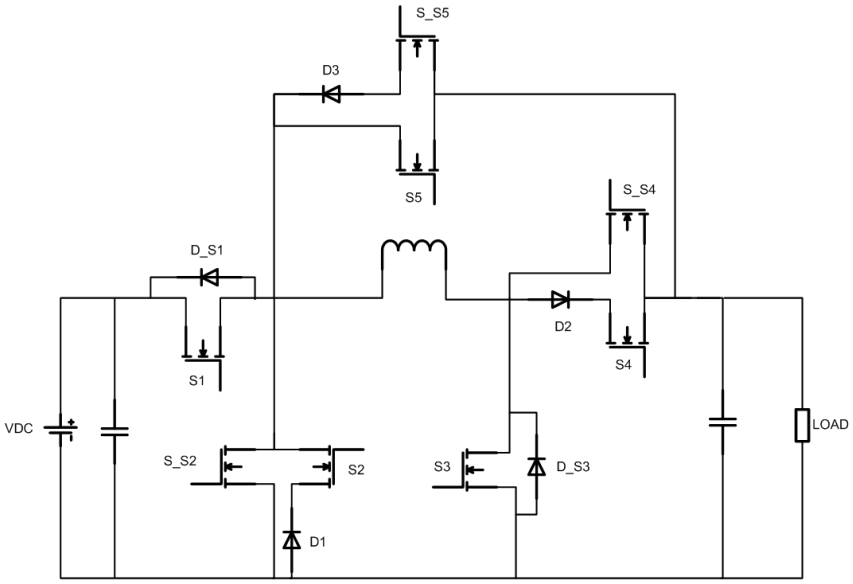


Figure 4-4 Modified Circuit Diagram for Two Way Power Flow

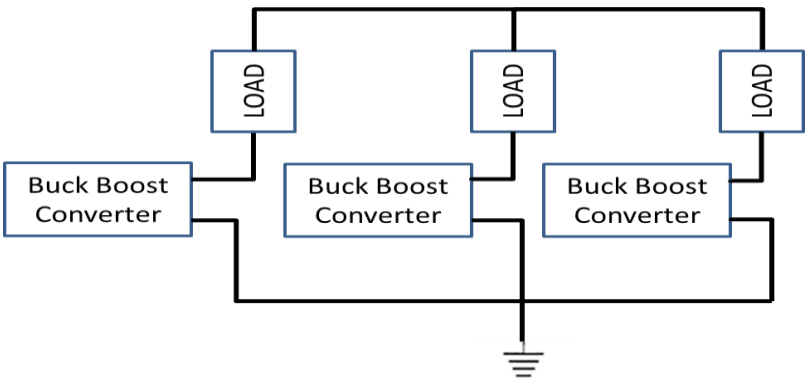


Figure 4-5 Three Phase Modification of Single Stage DC-AC Buck Boost Inverter

4.2.1. Component Requirements

Three capacitors with voltage rating higher than output peak voltage.

Six fast switches with voltage rating higher than input voltage plus output peak voltage.

Three fast switches with voltage rating higher than input voltage.

Six fast switches with voltage rating higher than output peak voltage.

Nine slow switches with voltage rating higher than output peak voltage.

Three inductors with current rating equal to the value calculated at equation 4.6. (Zero loss is assumed, output voltage is assumed to be constant at a value V_{outrms}, ripple current is ignored)

$$I_{Lmax} = \frac{P_{out}*\sqrt{2}*(V_{in}+V_{outrms}*\sqrt{2})}{3*V_{outrms}*V_{in}} \quad (4.6)$$

4.3. Classical Method (Boost Converter + Full Bridge)

Three phase inverter with boost capability can be obtained by using boost converter and full bridge. The block diagram of this topology is shown in Figure 4-6. Input voltage is first boosted to obtain required minimum voltage for full bridge. Then by applying sinusoidal PWM to full bridge and filtering by LC filter, three phase sine waves are obtained.

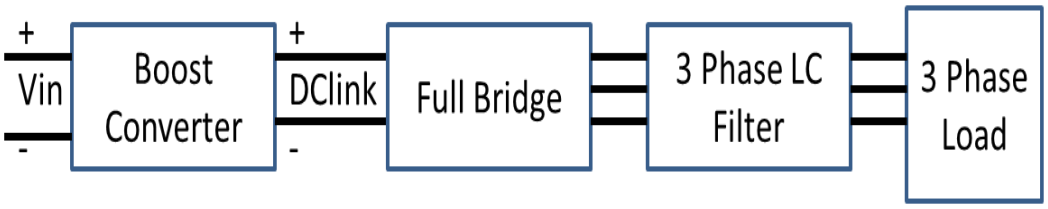


Figure 4-6 Block Diagram of Boost Converter and Full Bridge

4.3.1. Component Requirements

Three capacitors with voltage rating higher than output peak voltage, one capacitor with voltage rating higher than DC link voltage are required.

Eight fast switches with voltage rating higher than DC link voltage are required.

Three inductors with current rating equal to output peak current and one inductor with current rating equal to output voltage divided by input voltage are required. (Zero loss is assumed, output voltage is assumed to be constant at a value V_{outrms}, ripple current is ignored)

4.4. Non-Linear Sliding-Mode Control of Three-Phase Buck-Boost Inverter

Three inverting buck-boost converters are used to obtain 3 phase sine waves [19]. The block diagram of this topology is shown in Figure 4-7.

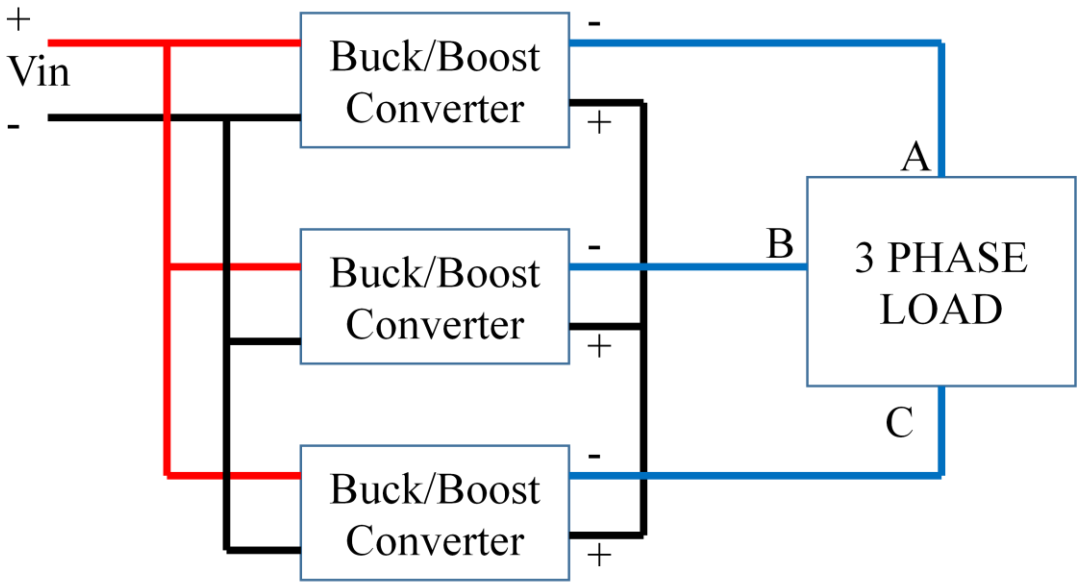


Figure 4-7 Block Diagram of Inverting Buck-Boost Converter

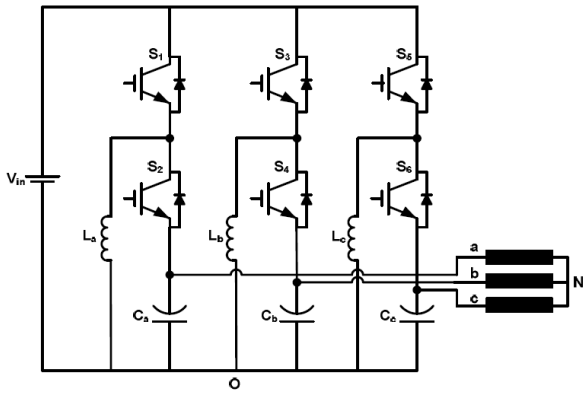


Figure 4-8 Circuit Diagram of Inverting Buck-Boost Converter

The circuit diagram of this topology is shown in Figure 4-8. Output voltages of converters are modulated to obtain three phase sine waves.

4.4.1. Component Requirements

Three capacitors with voltage rating higher than output peak voltage are required.

Six fast switches with voltage rating higher than input voltage plus output peak voltage are required.

Inductor current rating for single phase inverting buck-boost converter is derived in Chapter 2. For three phase, maximum inductor current is calculated according to equation 4.7.

$$I_{Lmax} = \frac{P_{out}*\sqrt{2}*(V_{in}+V_{outrms}*\sqrt{2})}{3*V_{in}*V_{outrms}} \quad (4.7)$$

Three inductors with current rating equal to maximum current calculated by equation 4.7 are required. (Zero loss is assumed, output voltage is assumed to be constant at a value V_{outrms}, ripple current is ignored)

4.5. Non-inverting Buck Boost Converter (Proposed Method)

The block diagram of three phase non-inverting buck boost converter is shown in Figure 4-9. Detailed description of operating principle of this topology is described in Chapter 5. In this section only component ratings are given to make comparison.

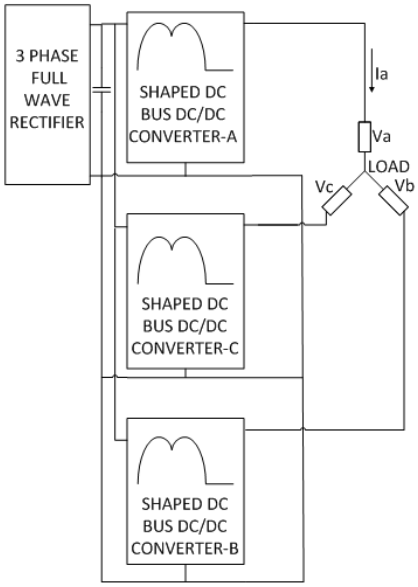


Figure 4-9 Block Diagram of Non-inverting Buck-Boost Converter

4.5.1. Component Requirements

Three capacitors with voltage rating higher than line to line output peak voltage are required.

Twelve fast switches with voltage rating higher than maximum of input voltage or line to line output peak voltage, are required.

Three inductors with current rating equal to output peak current divided by 0.8 is required.

4.6. Comparison of Topologies

Table 4-1 is formed to make comparison easier, it includes switch and capacitor voltages and inductor currents in terms of output voltage (V_{out}), output power (P_{out}) and input voltage (V_{in}).

V_{out} is the RMS values of phase voltage, P_{out} is three phase total output power and V_{in} is input voltage.

Table 4-1 Component Ratings of Topologies with boosting Capability

	Switch Voltage	Capacitor Voltage	Inductor Current	Fast SW	Slow SW
Boost DC-AC [9]	$V_{out}*2*\sqrt{2}+ V_{in}$ (6 fast switches)	$V_{out}*2*\sqrt{2}+V_{in}$ (3 capacitors)	$4*P_{out}/(3V_{in})+$ $\sqrt{2}*P_{out}/(3V_{out})$ (3 inductors)	6	
Single Stage Buck Boost [11]	$V_{in}+ V_{out}*\sqrt{2}$ (6 fast switches) V_{in} (3 fast switch) $V_{out}*\sqrt{2}$ (6 fast switches,9 slow switches)	$\pm V_{out}*\sqrt{2}$ (3 capacitor)	$\sqrt{2}*(P_{out}/3)*$ $(V_{in}+V_{out}*\sqrt{2})/$ $(V_{in}*V_{out})$ (3 inductors)	15	9
Inverting Buck Boost [19]	$V_{in}+ V_{out}*\sqrt{6}$ (6 fast switches)	$V_{out}*\sqrt{6}$ (3 capacitor)	$\sqrt{2}*P_{out}/3*$ $(V_{in}+V_{out}*\sqrt{6})/$ $(V_{in}*V_{out})$		
Boost Converter + Full Bridge + LC filter	V_{in} (2 fast switches) V_{DClink} (6 fast switches)	V_{DClink} (1 capacitor) $V_{out}*\sqrt{6}$ (3 capacitors)	P_{out}/V_{in} (1 inductor) $P_{out}*\sqrt{2}/(3*V_{out})$ (3 inductors)	8	
Non-Inverting Buck-Boost (Proposed Method)	$Max(V_{in}, V_{out}*\sqrt{6})$ (12 fast switches)	$V_{out}*\sqrt{6}$ (3 capacitor)	$P_{out}*\sqrt{2}$ / $(3*0.8*V_{in})$ (3 inductors)	12	

Some assumptions are done values in Table 4-1 are replaced with these assumption. Table 4-3 is formed with following assumptions. These assumptions are shown in Table 4-2.

Table 4-2 Power and Voltage Assumptions

V_{in}	500V
P_{out}	5500W
V_{out}	220Vrms
V_{DClink}	600V

Table 4-3 Component Ratings of Topologies with Boosting Capability

	Switch Voltage	**Capacitor Voltage**	**Max Inductor Current**	**Fast SW**	**Slow SW**
Boost DC-AC [9]	1120V (6 fast switches)	1120V (3 capacitors)	26.45A (3 inductors)	6	
Single Stage Buck Boost [11]	810V (6 fast switches) 500V (3 fast switch) 310V (6 fast switches,9 slow switches)	±310V (3 capacitors)	19.1A (3 inductor)	15	9
Inverting Buck Boost	1040V (6 fast switches)	540V (3 capacitors)	24.58A (3 inductors)	6	
Classical Boost Converter + Full Bridge + LC filter	600V (8 fast switches)	600V (1 capacitor) 540V (3 capacitors)	11A (1 inductor) 11.79A (3 inductors)	8	
Proposed Method (Non-Inverting Buck-Boost)	540V (12 fast switches)	540V (3 capacitor)	12.73A (3 inductors)	12	

When Table 4-3 is observed, voltage and current ratings of Boost DC-AC topology are much higher than ratings of other topologies. It is designed for input voltages lower than input voltage assumption which is made in this chapter.

Single Stage Buck Boost topology seems proper according to its voltage and current ratings; however it requires fifteen fast and nine slow switches for three phase application. Requirement of high switch count makes this topology not preferable.

Inverting Buck-Boost topology requires less switch count however high voltage ratings of capacitors and switches make it not preferable.

Classical method and proposed method seems close to each other, classical method requires additional capacitor and inductor for boost part, whereas proposed method requires more switches than classical method. Cost and efficiency analysis should be done to make comparison between these two methods.

4.6.1. Efficiency Analysis of Proposed Topology and Classical Method

To compare efficiencies of classical method and proposed method, simulations are done. To make simulations first capacitance and inductance values are calculated.

Non-Inverting Buck-Boost Converter Inductor and Capacitor Calculation

Non-inverting Buck-Boost Converter operates as buck converter when V_{out} is less than V_{in} and it operates as boost converter when V_{out} is higher than V_{in}.

Voltage ripple is higher in boost mode thus capacitor value can be calculated according to boost mode.

$$\Delta V = \frac{V_{in} * I_{outpeak} * D * T}{2 * C * V_{outpeak}} \qquad (4.1)$$

Ripple voltage equation is given at equation 4.1. D being duty cycle is assumed to be maximum 20%. Peak output current is equal to 11.9A, period is 100uS, output peak voltage is equal to 540V, and input voltage is equal to 500V. Ripple voltage is assumed to be 10V. Then required capacitance is calculated to be 11uF. For commercial value it is approximated to 10uF.

$$\Delta I_L = \frac{V_{in} * D * T}{2 * L} \qquad (4.2)$$

ΔI_L is assumed to be 20% of output current which is 11.9A. Then L is equal to 2.1mH. Required core area, magnetic length, gap, turn number and cost is calculated and shown in Table 4-4.

Table 4-4 Calculated Inductor Values for Non-inverting Buck Boost Converter

Ac	4.73 cm^2
Lm	12.30 cm
ResrL	0.013 Ω
lg	0.091cm
TurnN	57
Cost	21.83€

Non-inverting Buck-Boost Converter Simulation Results

Circuit diagram simulated for buck-boost converter is shown in Figure 4-10. The circuit diagram shows one phase of inverter namely phase A. Inverter contains three of this circuit except shown capacitors C1, C2 and C3. All capacitors are shown in Figure 4-10, they are delta connected.

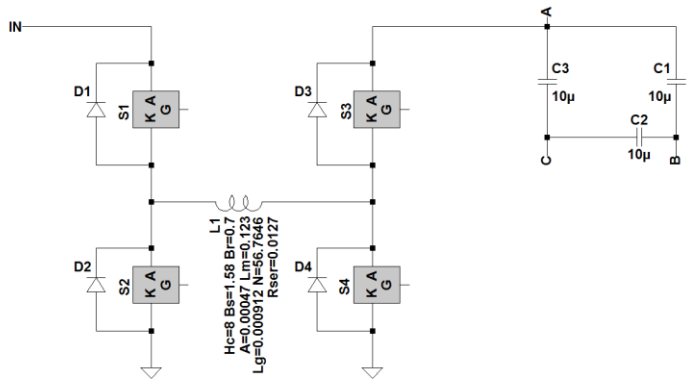


Figure 4-10 Circuit Diagram of Non-inverting Buck-Boost Converter

Phase A voltage waveform, inductor current of L1 and phase current of phase A are shown in Figure 4-11. When V_{out} is less than 80% of input voltage, buck mode is used by making S3 conduct and disconnecting S4, otherwise buck-boost mode is used. Figure 4-12 shows phase voltage of A and B and line to line voltage of V_{ab}. Simulation results are shown in Table 4-5.

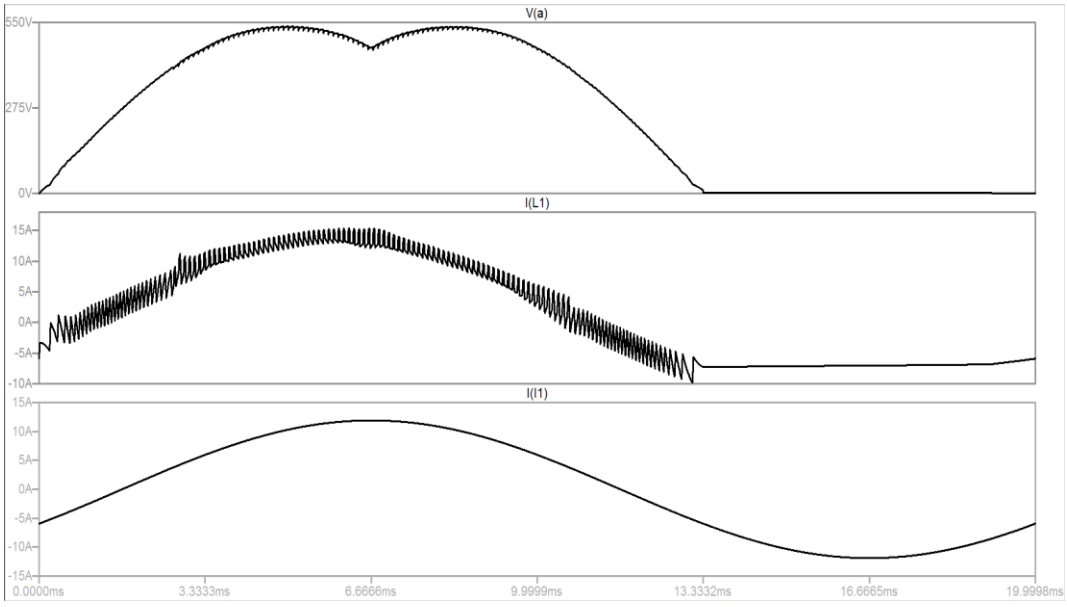


Figure 4-11 Phase A voltage, Inductor Current and Output current Waveform

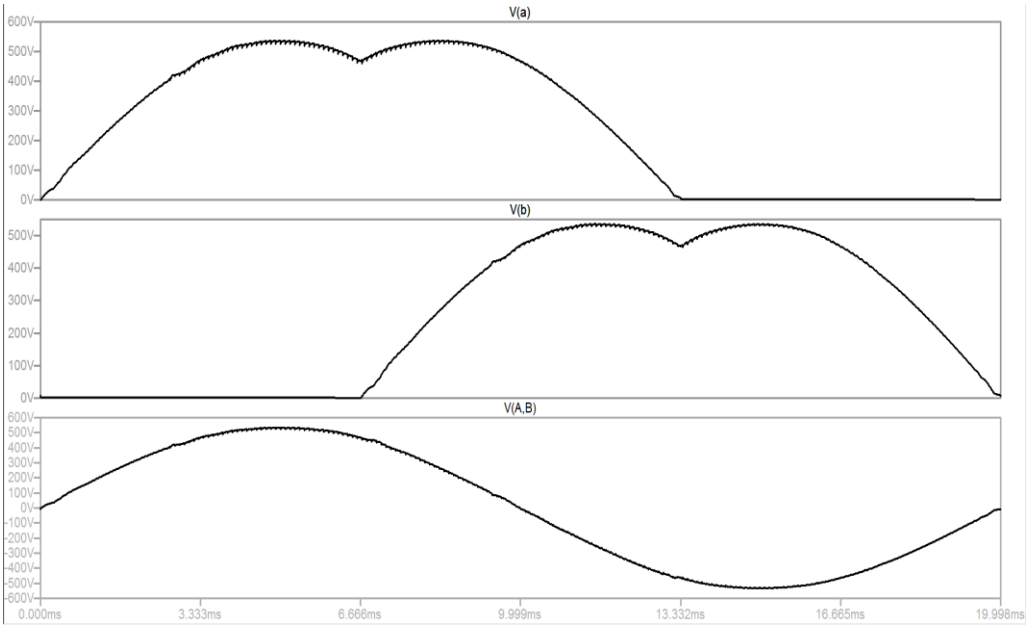


Figure 4-12 Phase A and B voltages and Line to Line Voltage V_{ab}

Table 4-5 Simulation Results of Non-Inverting Buck Boost Converter

Simulation		Non-inverting Buck-Boost
Capacitor Values	C(F)	10u
	ESR(Ω)	480m
	ESL(H)	195n
Inductor Values	ESR(Ω)	0,013
	L(H)	2.1m
Converter Values	Pout(W)	5522,10
	Pin(W)	5718,23
	Lloss (W)	2,82
	Closs (W)	3,80
	S and D losses (W)	189,51
	Switching Frequency	10k
	η (efficiency)	0,97
	THD(%)	0,79

Classical Method (Boost Converter + Full Bridge + LC filter) Inductor and Capacitor Calculation

Boost converter and full bridge component requirements are calculated separately, then added.

Boost Converter Inductor and Capacitor Calculation

Ripple voltage equation is given at equation 4.3. D being duty cycle is assumed to be maximum 20%. Peak output current of boost converter is equal to 9.6A, period is 100uS, DC link voltage is equal to 600V, and input voltage is equal to 500V. Ripple voltage is assumed to be 10V. Then required capacitance is calculated to be 7.63uF. For commercial value it is approximated to 10uF.

$$\Delta V = \frac{V_{in} * I_{out} * D * T}{2 * C * V_{DClink}} \quad (4.3)$$

$$\Delta I_L = \frac{V_{in} * D * T}{2 * L} \quad (4.4)$$

ΔI_L is assumed to be 20% of output current which is 9.6A. Then L is equal to 2.7mH. Required core area, magnetic length, gap, turn number and cost is calculated and shown in Table 4-6.

Table 4-6 Calculated Inductor Values for Buck-Boost Converter

Ac	4.04 cm^2
Lm	11.37 cm
ResrL	0.019 Ω
lg	0.082 cm
TurnN	66
Cost	18.5€

Full Bridge Inductor and Capacitor Calculation

Ripple voltage equation is given at equation 4.5. Period is 100 uS, input voltage is equal to 500V. Ripple voltage is assumed to be 10V. Capacitance value is taken 10uF in order to make capacitance equal with other topologies. Then L is equal to 1.88mH.

$$\Delta V = \frac{V_{in} * T^2}{32 * L * C} \qquad (4.5)$$

Required core area, magnetic length, gap, turn number and cost is calculated and shown in Table 4-7.

Table 4-7 Calculated Inductor Values for Output Filter of Classical Method

Ac	4.43 cm^2
Lm	11.91 cm
ResrL	0.012 Ω
lg	0.087cm
TurnN	54
Cost	20.38€

Boost Converter and Full Bridge Simulation Results

Simulation results of boost converter and full bridge are shown in Table 4-8. For each component losses are shown in the table.

Table 4-8 Simulation Results of Classical Method

Simulation		Full Bridge	Boost
Capacitor Values	C(F)	10u	10u
	ESR(Ω)	480m	480m
	ESL(H)	195n	195n
Inductor Values	ESR(Ω)	0,012	0,019
	L(H)	1.88m	2.7m
Converter Values	Pout(W)	5524,60	5662,70
	Pin(W)	5663,10	5744,10
	Lloss (W)	2,91	2,46
	Closs (W)	2,01	7,83
	S and D losses (W)	133,58	71,11
	Switching Frequency	10k	10k
	η (efficiency)	0,98	0,99
	THD(%) (1000 harmonic components of 50Hz)	0,27	

4.6.2. Cost Analysis of Proposed Topology and Classical Method

For each topology cost analysis is done. According to ratings of capacitors, inductors and switches, costs are calculated by using cost models.

Non-Inverting Buck-Boost Inverter Cost

Inductor Cost is calculated in previous section and it is 21.83€. Capacitor cost is calculated according to cost model and it is 28.68€. Switch cost is calculated according to cost model and it is 2.349€.

Boost Converter Cost

Inductor Cost is calculated in previous section and it is 18.5€. Capacitor cost is calculated according to cost model and it is 28.68€. Switch cost is calculated according to cost model and it is 1.9€.

Full Bridge + Filter Cost

Inductor Cost is calculated in previous section and it is 20.83€. Capacitor cost is calculated according to cost model and it is 28.68€. Switch cost is calculated according to cost model and it is 2.246€.

4.6.3. Cost Comparison of Proposed Topology and Classical Method

For each topology component costs are shown in Table 4-9. Total cost of buck-boost converter is 179.72€ whereas total cost of boost converter plus full bridge is 212.99€. It is seen that proposed topology decreases component cost.

Table 4-9 Cost Comparison of Proposed Topology and Classical Method

	Switch Cost	Capacitor Cost	Inductor Cost	Total Cost
Non-inverting Buck-Boost	28.188€	86.04€	65.49€	179.72€
Boost Converter	3.8€	28.68€	18.5€	50.98€
Full Bridge	13.48€	86.04€	62.49€	162.01€
Boost+Full Bridge	17.28€	114.72€	99.77€	212.99€

4.6.4. Overall Comparison of Proposed Topology and Classical Method

Table 4-10 shows efficiency and cost of Non-inverting Buck-Boost Converter and Classical Method (Boost Converter + Full Bridge + Filter). Non-inverting Buck-Boost converter is more efficient than classical method and it is cheaper.

Table 4-10 Efficiency and Cost Comparison of Non-Inverting Buck-Boost Converter and Classical Method

	Non-inverting Buck-Boost Converter	Boost Converter + Full Bridge + Filter
n	0,97	0,96
Cost	179.72€	212.99€

4.7. Summary

In this chapter, topologies with pure sine wave output and boosting capability are analyzed. It is found that topologies which are mainly designed for solar power applications are not appropriate for grid connected operation since their voltage rating of switches and capacitors increases when input voltage increases. In this chapter, a topology is proposed to obtain sinusoidal output and boosting capability. Topologies are first compared according to ratings of required components. According to this comparison, it is found that component ratings of two topologies are more appropriate for defined operating conditions. These two topologies which are proposed topology and classical topology are further analyzed to compare efficiency and cost of these topologies. Classical method consists of boost converter, full bridge and filter at the output. The results show that proposed method is nearly 1% more efficient and nearly 15% cheaper than classical topology for defined operating conditions. Therefore, the proposed topology is implemented to observe its operation which is described in chapter 5.

CHAPTER 5

DESIGN AND IMPLEMENTATION

In this chapter, design and implementation process of non-inverting buck boost inverter is described in detail. In Chapter 4, three phase topologies with boosting capability were discussed. First, the topologies were compared according to component ratings and component counts. It was found that each topology has some advantages and disadvantages. Some of them are designed for lower input voltages such as solar power applications and they are not appropriate for grid connected operation since component rating becomes relatively high. Thus two of the topologies which are more appropriate for given conditions, are chosen to compare their efficiencies and cost. One of them is the proposed topology which will be described in detail in this chapter, and the other one is the conventional method to use boost converter in front of three phase full bridge with a LC filter at the output of full bridge to obtain sine wave. Simulations and cost calculations which are described in Chapter 4, show that proposed method is cheaper and more efficient than the classical topology with a boost stage followed by an three-phase bridge.

In this chapter, design for specific requirements is described for the proposed topology in detail. Block diagram of proposed topology is shown in Figure 5-1. The inverter is fed from DC supply to form three-phase voltage. In the proposed topology, the DC voltage stage is followed by a power stage, control stage (voltage transducer is part of the control stage) and software which runs to manage the control stage.

In this chapter, first the power stage of proposed topology will be described. The operation of the circuit and ratings of component are described. Secondly control stage is explained. In control stage, microcontroller selection, CPLD (Complex

Programmable Logic Device) requirement and CPLD operation are described. Operation of CPLD will be explained in section 5.3.2. Thirdly, the control software is described with a flowchart in section 5.4. Lastly, obtaining DClink voltage is described in section 5.5.

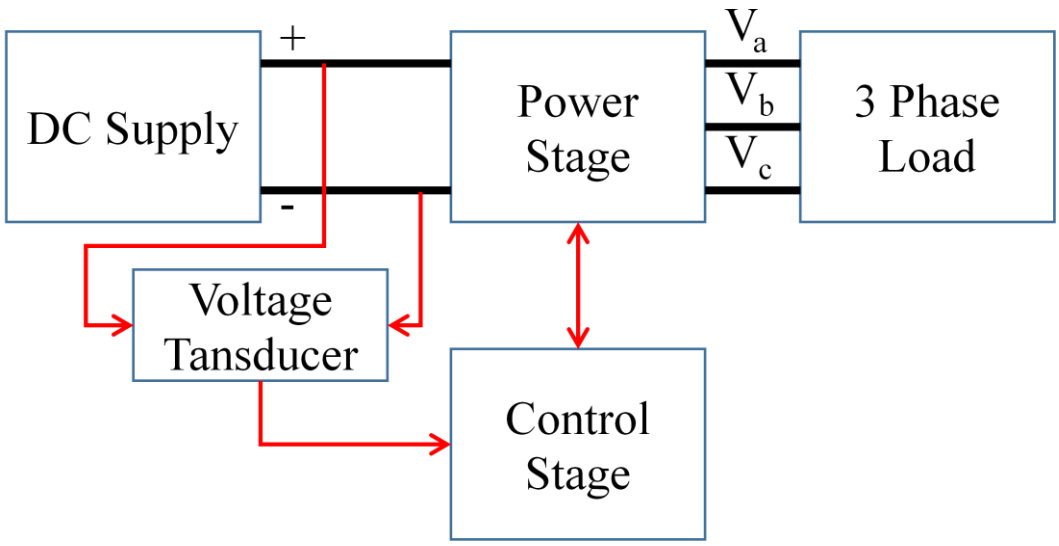


Figure 5-1 Block Diagram of Proposed Topology

5.1. Design Requirements

The main goals of the design are to produce pure sine wave at the output and to boost input voltage when necessary. Input voltage range, output voltage, output power and frequency range is shown in Table 5-1. Power stage and control stage are designed to operate in these conditions. Output voltage can be set between 10Hz to 75Hz. Rated operating frequency is 50Hz. Rated voltage at rated frequency is 380V. For lower frequencies output voltage level is decreased to achieve V/f control. For higher frequencies output voltage is constant and equal to rated voltage. This design is done for maximum 380Vrms line to line. Higher output voltage level can also be obtained by replacing switches and capacitors with higher voltage rated components. Since output voltage level is decreased for lower frequencies, output power is also decreased assuming inverter supplies rated current. Application of V/f is the design

criteria. It is selected to be V/f controlled to be able to drive an induction machine at different frequencies. Inverter can also operate at constant output voltage by updating software however in this design it is V/f controlled.

Table 5-1 Design Requirements for Operation

V_{in} (V DC)	400-540
V_{out} (Vrms line to line)	380 when f≥50 380*f/50 when f<50
P_{out} (W)	2500 when f≥50 2500*f/50 when f<50
Frequency (Hz)	10-75

5.2. Power Stage Design

In this section, design of power stage is explained. First operation principle of power stage is described. Three phase voltage generation by using three converters and operating modes of the converters are described in that section. Then component selection criteria are described.

5.2.1. Operation Principle

In Figure 5-2 block diagram of power stage is shown. It consists of 3 non-inverting buck boost converters. Positive terminal of each converter is tied to one phase and negative terminals are tied to each other. The block diagram is same with the topology described in section 3.4. The difference between topologies described in

this chapter and in section 3.4, is the converter stage. Buck converter is used in section 3.4 and non-inverting buck boost converter is used in this section.

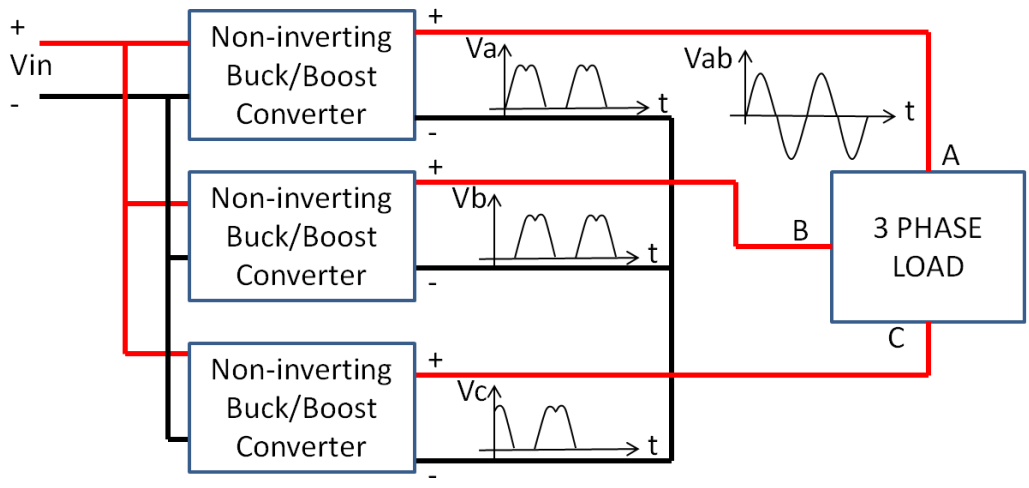


Figure 5-2 Block Diagram of Power Stage

Obtaining three phase sine waves by using three converters is described in section 3.4. This issue will be briefly revised again in this section. Three converters are made to follow reference signals to obtain output voltage waveforms which are shown in Figure 5-3. Each converter operates 2T/3 time where T is fundamental output period. Voltage waveforms are delayed by T/3.

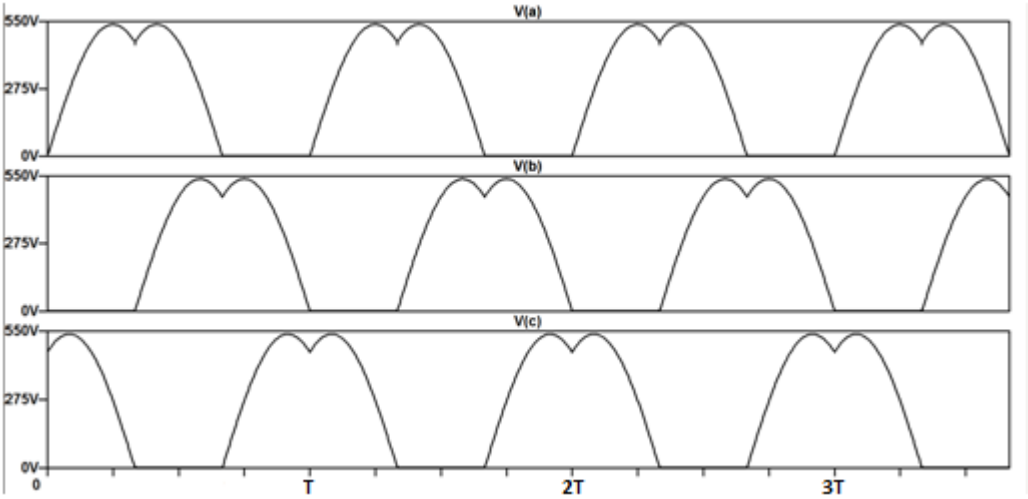


Figure 5-3 Output Voltage Waveforms of Converters

Phase a, phase b and line to line voltage V_{ab} are shown in Figure 5-4. As it can be observed sine wave V_{ab} is generated by using the converters whose outputs are shown with V(a) and V(b).

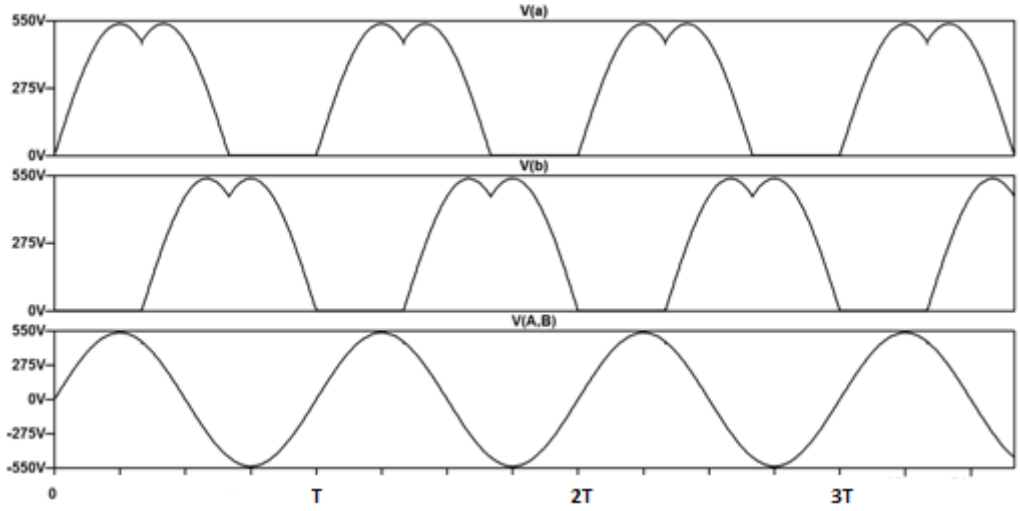


Figure 5-4 Phase A, Phase B and Vab Voltage Waveforms

Three non-inverting buck boost converters are used to produce three voltage waveforms which are shown in Figure 5-3. The circuit diagram of power stage for one phase is shown in Figure 5-5. Non-inverting buck boost topology requires 4 switches. This circuit can operate in three different modes; buck, boost and buck-boost. The way these modes are employed in this study are discussed in section 5.2.1.1, 5.2.1.2 and 5.2.1.3.

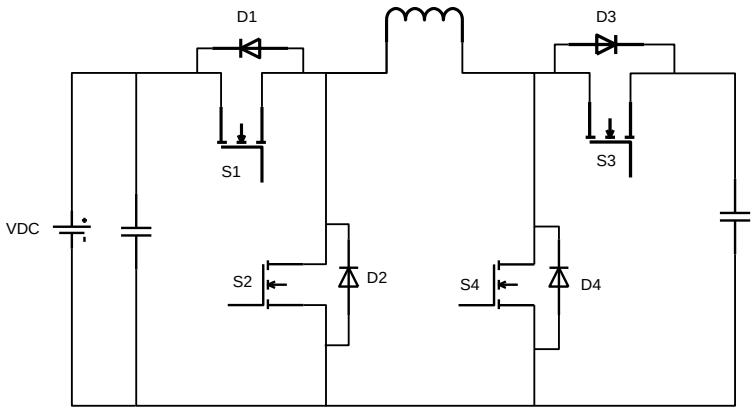


Figure 5-5 Circuit diagram of one converter for one phase

Circulating currents may occur when power supplies are operated in parallel. In this design each converter operates individually, therefore circulating currents do not occur, however, unbalanced currents may occur if load is not balanced or output voltage levels of individual phase converters are different.

5.2.1.1. Buck Mode Operation

During buck mode operation, S3 is always conducting, S4 is not conducting and S1 and S2 are switched to obtain regulation. Buck mode switch states are shown in Figure 5-6. Transfer ratio of buck mode is shown in equation 5.1 [20]. "Duty1" is the ratio of time of S1 conducting over period.

$$V_{out} = Duty1 \times V_{in} \tag{5.1}$$

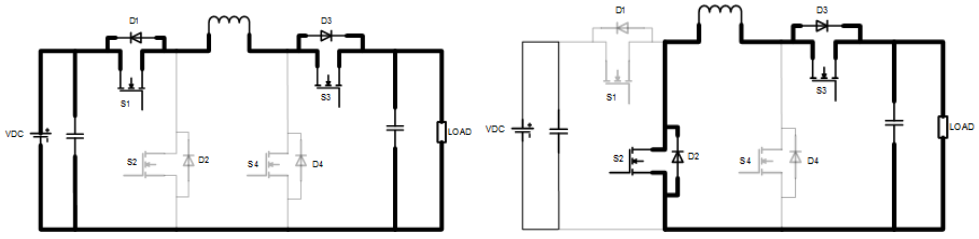


Figure 5-6 Buck Mode Operation

5.2.1.2. Boost Mode Operation

During boost mode operation, S1 is always conducting, S2 is not conducting and S3 and S4 are switched to obtain regulation. Boost mode switch states are shown in Figure 5-7. Transfer ratio of boost mode is shown in equation 5.2 [20]. "Duty2" is the ratio of time of S4 conducting over period.

$$V_{out} = \frac{V_{in}}{1-Duty2} \tag{5.2}$$

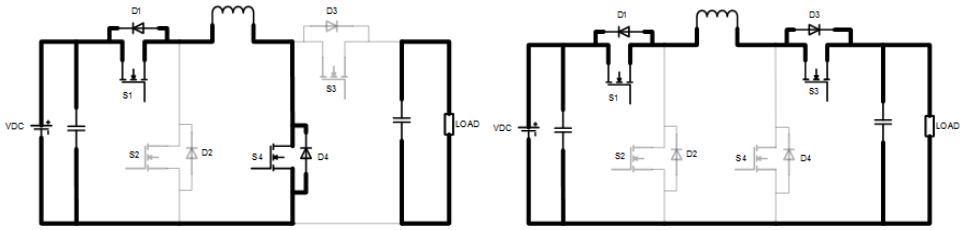


Figure 5-7 Boost Mode Operation

5.2.1.3. Buck-Boost Mode Operation

Ideally buck mode and boost mode would be enough to obtain output voltage lower or higher than input voltage. However, output voltage level equal to input voltage cannot be achieved by these two modes because of voltage drop over switches and power losses on components. Buck-Boost mode enables operation when output voltage is equal to input voltage; therefore buck boost mode is used. In buck boost mode, all switches are switched. Switching period can be divided into 3 states for buck boost operation. Switch states are shown in Table 5-2. During State 1, S1 and S4 are conducting and voltage over inductor is equal to input voltage. Current path is shown in Figure 5-8.

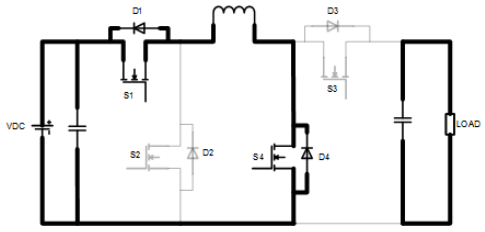


Figure 5-8 Buck-Boost Operation State 1

During State 2, S1 and S3 are conducting; voltage over inductor is equal to difference between input voltage and output voltage. Current path is shown in Figure 5-9.

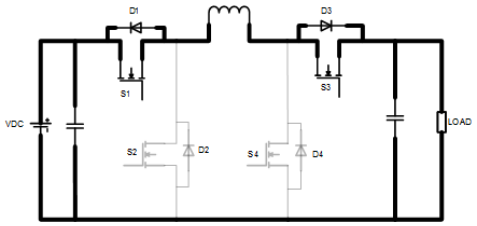


Figure 5-9 Buck-Boost Operation State 2

During State 3, S2 and S3 are conducting; voltage over inductor is equal to negative of output voltage. Current path is shown in Figure 5-10.

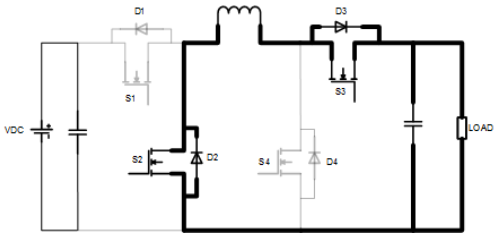


Figure 5-10 Buck-Boost Operation State 3

Table 5-2 Switch States during Operation Modes

	State 1	**State 2**	**State 3**
S1, D1	ON	ON	OFF
S2, D2	OFF	OFF	ON
S3, D3	OFF	ON	ON
S4, D4	ON	OFF	OFF
VL	V_{in}	V_{in}-V_{out}	-V_{out}

In Figure 5-11 and Figure 5-12, inductor current waveform is visualized according to voltage over its terminals. Switching states are shown for a switching period. Output voltage is higher than input voltage in Figure 5-11. Since output voltage is higher than input voltage, voltage over inductor is negative thus current decreases in state 2. Output voltage is lower than input voltage in Figure 5-12. Since output voltage is lower than input voltage, voltage over inductor is positive thus current increases in state 2. Input to output transfer ratio can be calculated by using inductor voltage time area.

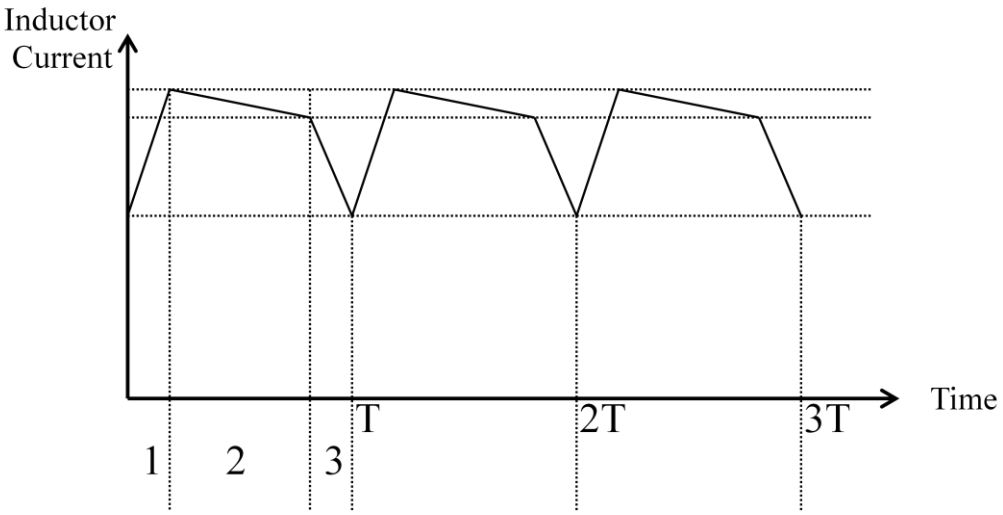


Figure 5-11 Inductor current waveform when output voltage is higher than input voltage

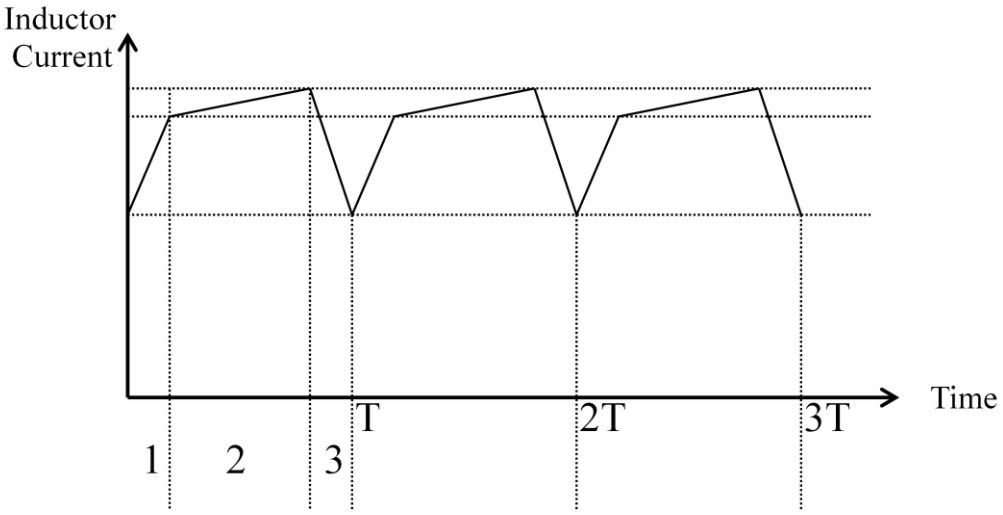


Figure 5-12 Inductor current waveform when output voltage is lower than input voltage

5.2.1.4. Determination of Transfer Ratio during Buck-Boost Mode

Duty1 is described as time of State 1 plus State 2 over period. It may be regarded as duty cycle of S1 and S2. Duty2 is described as time of state 1 over period. It may be regarded as duty cycle of S3 and S4. Voltage time area (VTA) mode is used to calculate transfer ratio. Inductor current waveform is shown in Figure 5-11 and Figure 5-12 and voltage over inductor in different states are shown in Table 5-2. Voltage time area(VTA) of State1, State2, State3 are shown in equations 5.3, 5.4, 5.5 respectively. VTA over a period is equal to zero. 3 equations are added and equated to zero in equation 5.6.

$$VTA_{State1} = Duty2 \times V_{in} \tag{5.3}$$

$$VTA_{State2} = (Duty1 - Duty2) \times (V_{in} - V_{out}) \tag{5.4}$$

$$VTA_{State3} = (1 - Duty2) \times (-V_{out}) \tag{5.5}$$

$$0 = Duty2 \times V_{in} + (Duty1 - Duty2) \times (V_{in} - V_{out}) + (1 - Duty1) \times (-V_{out}) \tag{5.6}$$

$$0 = Duty1 \times V_{in} + (1 - Duty2) \times (-V_{out}) \tag{5.7}$$

Equation 5.7 shows transfer ratio of input to output. It is dependent on both duty cycles Duty1 and Duty2. In the design, Duty1 is kept constant during buck-boost mode operation and Duty2 is changed to regulate output voltage.

5.2.1.5. Mode Transition

Ideally buck mode and boost mode would be enough to obtain output voltage lower and higher than input voltage. However due to losses, it is not possible to obtain output voltage equal to input voltage in buck mode. When input voltage level and output voltage level are close, buck boost mode operation is required since desired

output voltage cannot be obtained by buck mode nor boost mode. In this design only two modes are used which are buck mode and buck-boost mode. Boost mode is omitted to decrease mode transition and make controller simple. Since required boosting ratio is lower than 35% this can be achieved by buck-boost mode. Boost mode can also be used in designs where boost ratio is higher than 50%.

Voltage threshold of mode transitions must be determined. This threshold can be anything, however making it too low will increase current ripple in the inductor. Thus it must be chosen as high as possible. Voltage drops over components and dead time between switching will cause converter to obtain lower voltage than input voltage in buck mode. It is assumed that buck converter operates successfully at 80% duty cycle thus voltage threshold is determined as 80% of input voltage. In other words, for a given time if output voltage value is less than 80% of input voltage, buck mode is used. Otherwise buck-boost mode is used. In buck mode output voltage to input voltage ratio determines the duty cycle(namely Duty1 in this chapter). In buck-boost mode Duty1 is kept constant at 80%, and Duty2 is set to regulate voltage.

5.2.2. Capacitor and Inductor Selection

In this section, method of choosing values of capacitance and inductance is described. Inductor peak current changes when capacitor changes. Thus a relationship between capacitance and peak inductor current is formed first.

5.2.2.1. Capacitance and Inductor Relationship

The topology is based on three converters which creates waveforms delayed by 120° to obtain three phase sine waves.

Assuming there is a supply whose output is in the shape of phase A voltage. Phase A voltage waveform is shown with V(a) in the top of Figure 5-13. There is a capacitor connected between output terminals. This capacitor is charging and discharging every cycle. Its current waveform is shown as I(C1) with red color in Figure 5-13.

Load current waveform is shown as I(A) with blue color in Figure 5-13. Total current supplied is the sum of load current and capacitor current and it is shown in the bottom of Figure 5-13.

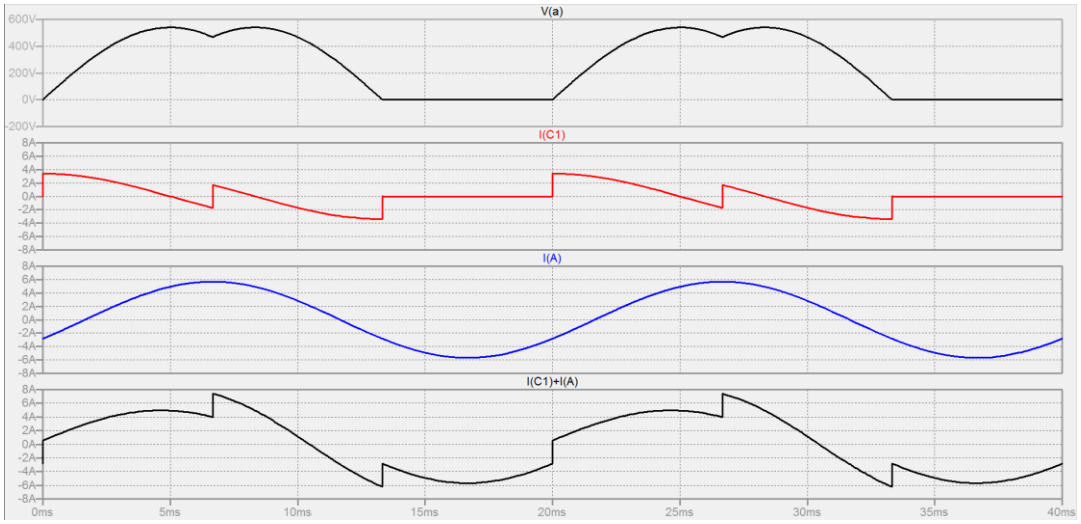


Figure 5-13 Phase A voltage, current, capacitor current, supply current

Maximum value of the current which must be supplied is in the break point of voltage waveform. Capacitor current value can easily be calculated assuming that it is supplied by sine wave. Breakpoint is at T/3.

$$V(t) = V_{outpeak} * \sin(wt - T/3) \tag{5.6}$$

$$I_c(t) = C * \frac{d(V(t))}{dt} \tag{5.7}$$

$$I_c(t) = C * w * V_{outpeak} * cos(wt - T/3) \tag{5.8}$$

I_c at breakpoint:

$$I_{cpeak} = \frac{C*w*V_{outpeak}}{2} \tag{5.9}$$

The current which must be supplied is equal to capacitor current plus load current. Since inductor of the converter does not conduct during Duty2 of period. Inductor current is higher and it is shown at equation 5.10.

$$I_{Lmax} = \frac{I_{out} + \frac{C*w*V_{peak}}{2}}{(1-Duty2)} \quad (5.10)$$

In equation 5.5 relationship of duty cycles with voltages is shown. It is said that Duty1 is equal to 0.8 for buck-boost operation. At the breakpoint output voltage is sin(60°)*Voutpeak.

$$(1 - Duty2) = \frac{0.8*Vin}{V_{outpeak}*\frac{\sqrt{3}}{2}} \quad (5.11)$$

Replacing (1-D2) term into equation 5.10 and replacing output voltage product with output current by output voltage, equation 5.12 is obtained.

$$I_{Lmax} = \frac{P_{out}}{0.8*V_{in}} + \frac{C*w*\sqrt{3}*(V_{outpeak})^2}{0.8*V_{in}} \quad (5.12)$$

Maximum inductor current increases when capacitance increases. Increasing capacitance decreases voltage ripple which results in better THD. Increasing maximum inductor current causes losses to increase since switches are turned on and off with higher current and inductor copper loss increases. Simulations are done to choose capacitance and inductance value. Simulations are done by using LT SPICE 4. Modeling components for simulation is described in section 3.5.1.

5.2.2.2. Capacitor

Inductor value is kept constant and capacitance value changed to observe ripple and losses. Ripple voltage and loss values for different capacitor values are shown in Table 5-3. Capacitance versus voltage ripple is shown in Figure 5-15 and capacitance versus loss graph is shown in Figure 5-14. Capacitance versus cost graph is shown in Figure 5-16.

Table 5-3 Ripple and Loss Values for Different Capacitors

Capacitance(uF)	Ripple(V)	Loss(W)
1	277	157
5	58	161
10	30	165
20	17	182
50	9	242
100	8,5	354

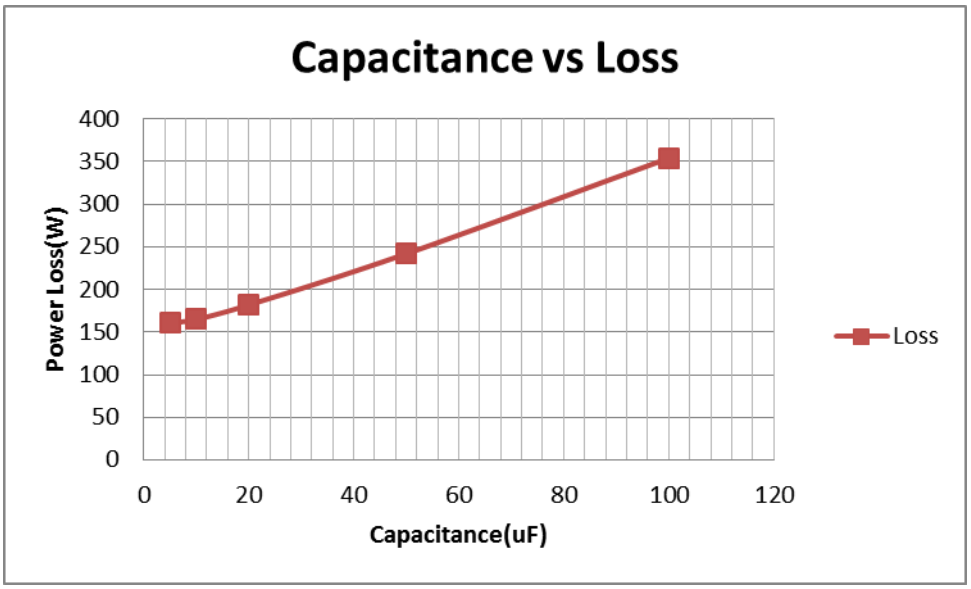


Figure 5-14 Capacitance versus Filter Loss Graph

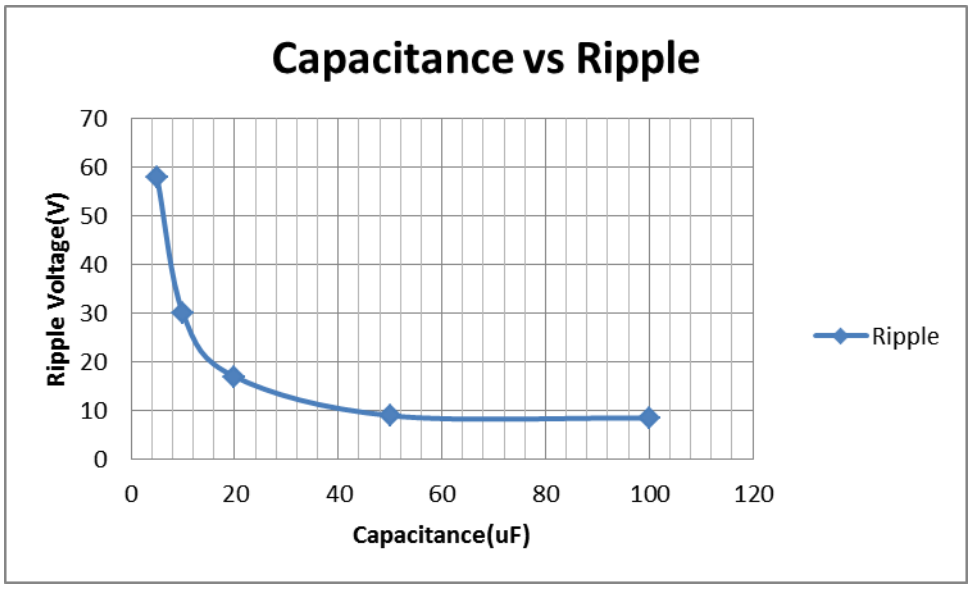


Figure 5-15 Capacitance versus Ripple Graph

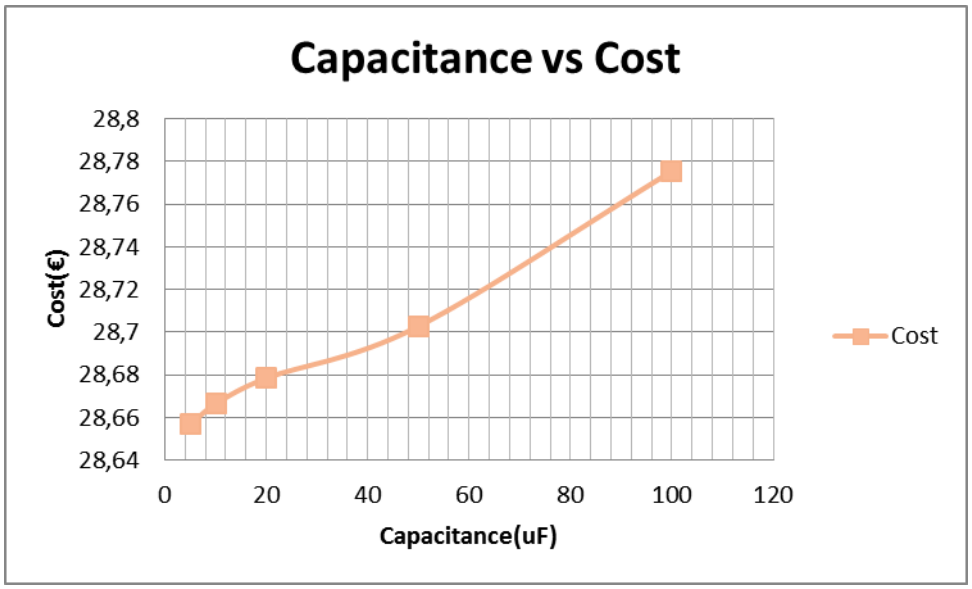


Figure 5-16 Capacitance versus Cost Graph

Increasing capacitance decreases voltage ripple but increases loss. Cost does not change significantly in this range. 20uF capacitance is decided to be used because its voltage ripple is low enough to operate inverter lower than 5% THD; this result is obtained by simulation.

5.2.2.3. Inductor

After capacitance value is selected, simulations are done for different inductance values. Increasing inductance value decreases current ripple thus it decreases losses, however it also increases size of inductor thus it increases cost. Cost and loss values for different inductor values are shown in Table 5-4. Loss values are obtained by simulation and cost values are obtained by cost models described in section 2.6.1. Inductance versus inductor cost is shown in Figure 5-17 and inductance versus power loss graph is shown in Figure 5-18.

Table 5-4 Ripple and Loss Values for Different Inductance

Inductance(mH)	Cost(€)	Loss(W)
0,1	10	251
0,5	11	212
0,7	12	191
1	14	182
2	21	173
3	33	165

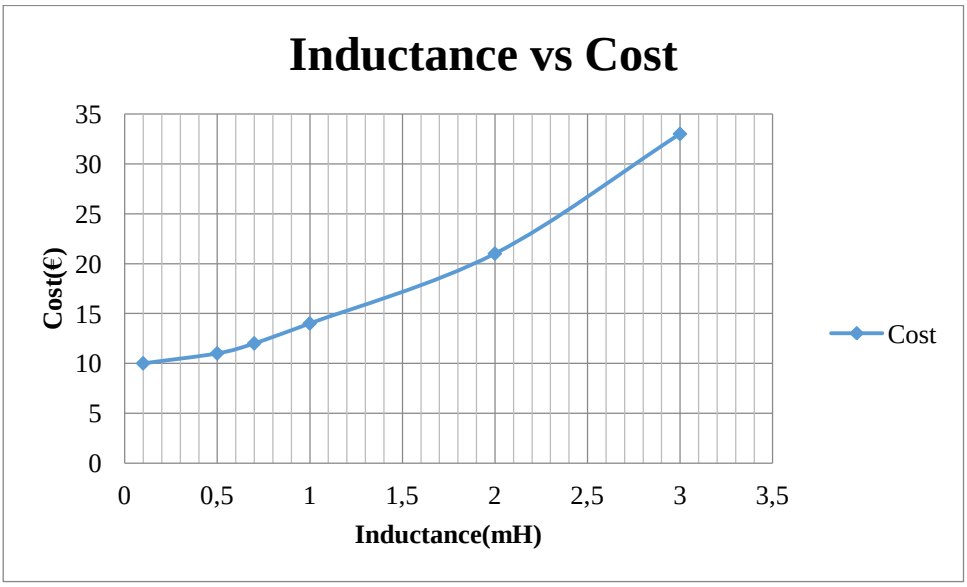


Figure 5-17 Capacitance versus Inductance Graph

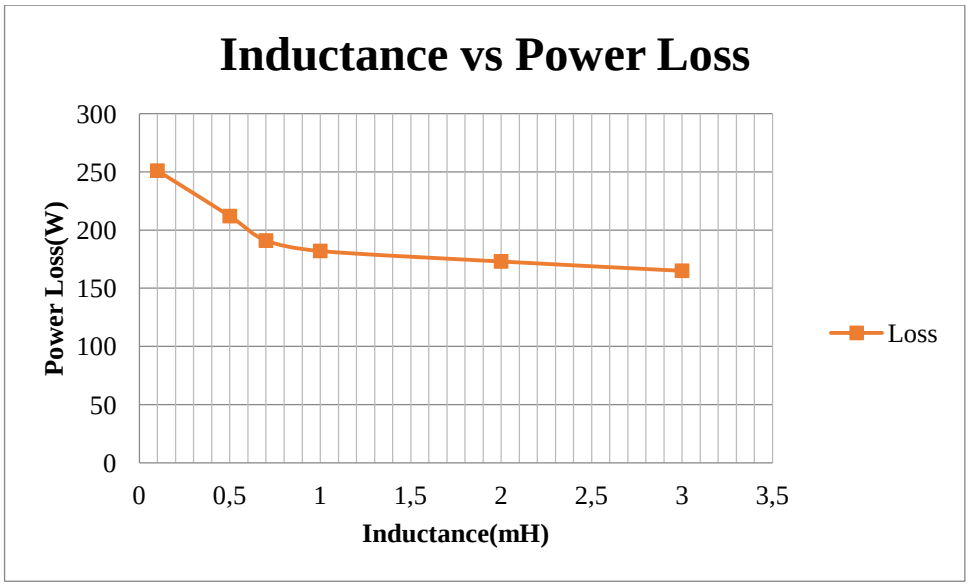


Figure 5-18 Capacitance versus Inductance Graph

Increasing inductance value decreases losses thus increases efficiency however it also increases size and cost. Inductance is chosen to be 700uH. N27 material E core is used to form inductor. In Table 5-5, inductor parameters are shown. In simulation results, inductor peak current is observed to be close to 20A. Thus inductor must have saturation current higher than 20A. Inductance is designed to have saturation current 25A and current limit is put to 20A to avoid inductor saturation. Current limiting is explained in section 5.3.

Table 5-5 Inductor Parameters

l_e (Effective magnetic path length)	149 mm
A_e (Effective Core Area)	683 mm^2
g (gap length)	3 mm
A_L (Inductance factor; $A_L = L/N^2$)	379nH
N (Turn Number)	43
Saturation Current	25A

5.2.3. Switch Selection

PM50RL1A120 IGBT(1200V, 50A) module is used which contains three phase full bridge with common input. It contains total of 6 switches. This switch is preferred because it has internal gate drive and protection circuit. These aspects allow quick prototyping.

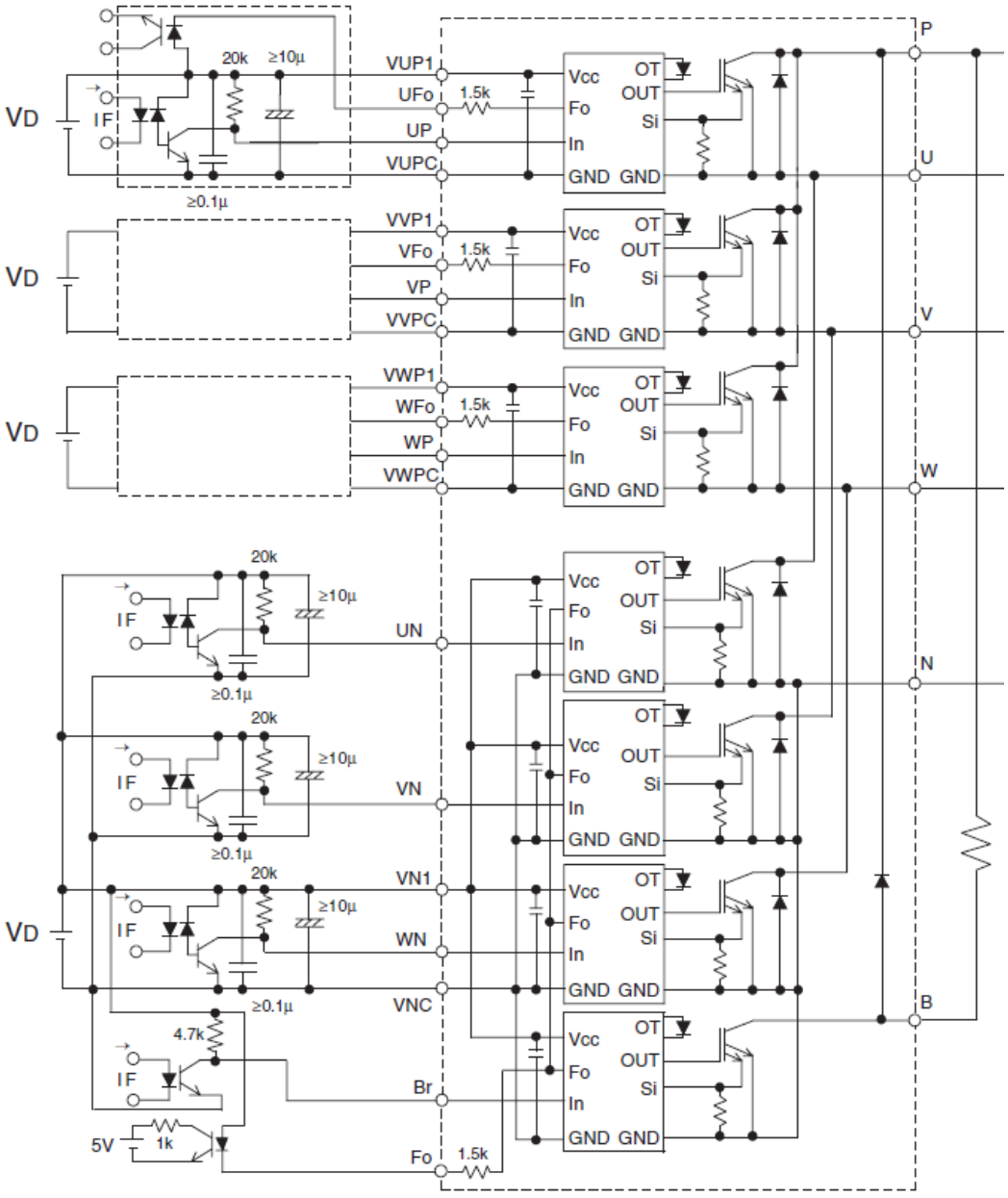


Figure 5-19 Application Example Circuit of PM50RL1A120 module [23]

Application Example Circuit of PM50RL1A120 module is shown in Figure 5-19. Power input terminals are P positive and N negative terminal. U, V and W are midpoints of IGBTs. To drive top switches, 3 isolated converters are required to supply control circuit of gate drivers. To drive bottom switches, 1 isolated converter is required to supply control circuit of gate drivers. Signal input of gate drivers are driven by optocouplers to isolate power stage and control stage. In this design 12 switches are required.

Power pin connection diagram is shown in Figure 5-20. Inductors of converters and input capacitor and output capacitors are also shown in Figure 5-20. Total of 4 PM50RL1A120 IGBT modules are used to implement 3 buck-boost converters. One module is used in the input side of converters (S1 and S2 according to Figure 5-5). Output terminals (midpoint of two IGBTs) are connected to the inductors of each converter. Since the module contains common input (top IGBTs are connected to same bus), output stage of converters require different modules. Thus 3 different modules are used at the output stages. Only one phase of the module is used at the output.

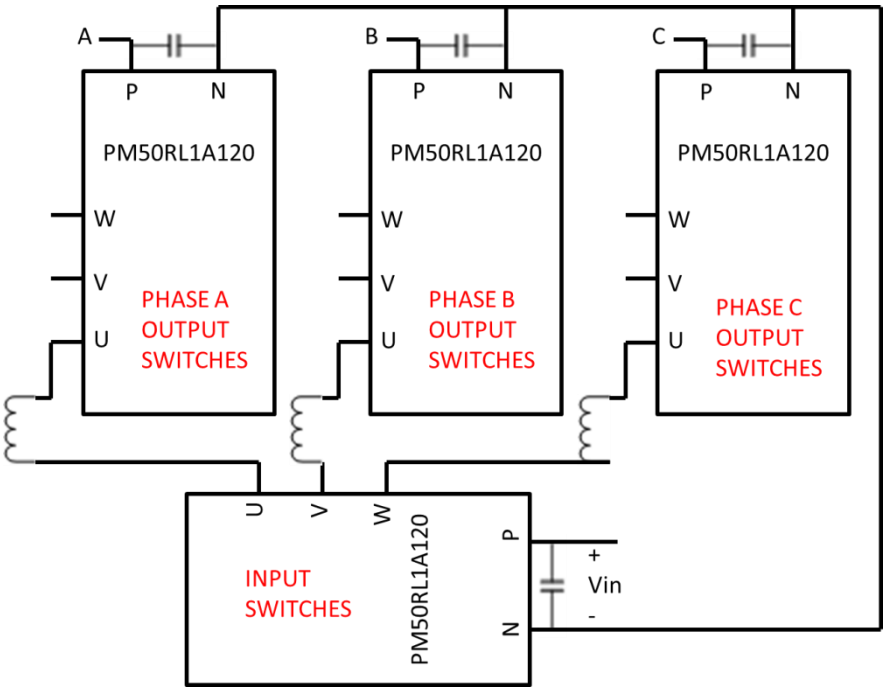


Figure 5-20 Connection Diagram of Power Terminal of IGBT Modules

5.2.3.1. Isolated Supplies

IGBT modules contain internal gate drive however they require isolated supplies for their gate drive circuitry. 7 isolated supplies are used to supply gate drive circuitry of IGBT modules. 3 of them are used to supply input side top switches, 3 of them used to supply output side top switches. One supply is used to supply all bottom switches since negative terminals of all modules are connected. TMR 2-4813WI (TRACO Power Company) is used for generating isolated 15V which is nominal voltage of gate drive circuitry.

5.2.3.1. Optocouplers

Optocouplers are used to transfer signals from control stage to power stage. HCPL-0466(AVAGO Technologies) is used for this purpose. For each switch, one optocoupler is used. Small (PCB) printed circuit boards(in size of IGBT module) which contain optocouplers are put over IGBT modules to make signal path shorter between IGBT modules and optocouplers. The PCB is shown in Figure 5-29.

5.3. Control Stage Design

In this section, design of control stage is explained. Control stage has two main objectives. First one is to produce PWM signals for all switches according to the input voltage. There are 12 IGBTs which must be driven where each two IGBTs are switched complementary. To drive all switches, 6 independent PWM signals are required. Thus the microcontroller must have at least 6 PWM outputs. Second objective is to protect the power stage. Inductors must not saturate thus current limit is needed for inductors. Over-voltage protection is required for output since converter is able to boost the voltage. Operation must be stopped when DClink voltage is not within 380V and 600V. To achieve all these objects of control stage, a block diagram is prepared. In Figure 5-21, block diagram of control circuit is shown.

Power stage is fed from a DC link. DC link voltage is measured by voltage transducer LV-25P (LEM). This transducer is isolated voltage transducer. It is used to isolate power stage and control stage. Output of the voltage transducer is read by ADC port of microcontroller. DC link voltage is used to calculate the duty cycles of switches at the output stage and for "disable" operation when input voltage is not within set limits. According DC link voltage level, microcontroller produces 6 PWM signals which is described in section 5.4.

One I/O port of the microcontroller is used for output over-voltage protection. Output voltage terminals are connected to resistive voltage divider through diodes. Maximum of three output voltages is conducted through diodes. This voltage is divided by resistors and compared with over-voltage limit. When output voltage of a phase exceeds the threshold, microcontroller stops operation of inverter and disables switching.

Four I/O ports of microcontroller are used for ON/OFF and output frequency setting. Software of microcontroller will be explained in section 5.4.

CPLD is used to generate IGBT gate signals. It has three objectives:

a) Forming complementary signals of PWM signals coming from the microcontroller,
b) Current protection of inductors used in converters
c) Obtaining dead time between complementary PWM signals of the switching IGBT's.

Use of CPLD is essential because selected microcontroller cannot produce 12 PWM signals. And also, limiting inductor current of converters cannot be performed in microcontroller since microcontroller is operating sequentially. Interrupt option could be used, however in case two inductor current of converters exceed the threshold, microcontroller can limit only one of them and it would cause overcurrent problems. CPLD operates as logic circuit and handles all signals at the same time.

Operation of CPLD is described in section 5.3.2. Instead of CPLD, FPGA can also be used. Main point is the ability of parallel processing.

Inductor current value of each converter is sensed by Hall Effect sensors. Current values are compared with current limits and if current limit is exceeded, a signal is sent to CPLD to turn off required switch. Current limits are set to 20A. Determination of limits is explained in section 5.2.2.3.

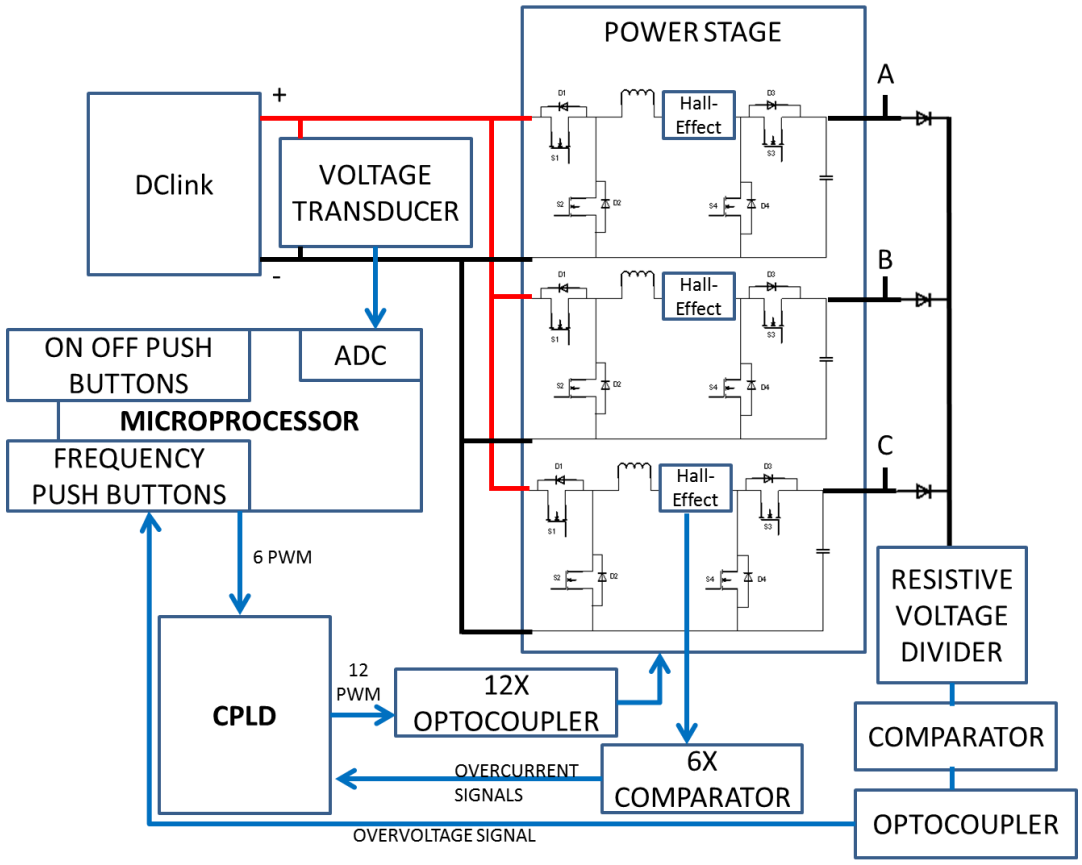


Figure 5-21 The Block Diagram of Control Stage

5.3.1. Microcontroller Selection

Power stage contains 6 complementary switches (2 complementary for each phase). Thus 6 complementary or 12 independent PWM ports are required. Since CPLD is used in the design, forming complementary signals is done in CPLD. Thus the microcontroller requires at least 6 independent PWM output ports, 6 I/O ports and 1

ADC port. dsPICDEM 1.1 Development Board is used since it contains a microcontroller which satisfies the required ports. It contains DSPIC30F6014(Microchip) microcontroller and peripheral components for different purposes . The development board also contains a linear regulator to regulate microcontroller bias voltage to 5V and it is supplied by a voltage level higher than 8V. On development board there are 4 push button switches connected to microcontroller. These switches are used to enable and disable inverter and to increase and decrease frequency. Development board also contains terminals connected to each pin of microcontroller; connections are done by using these terminals. Software which runs on microcontroller is explained in section 5.4. The development board is shown in Figure 5-22.

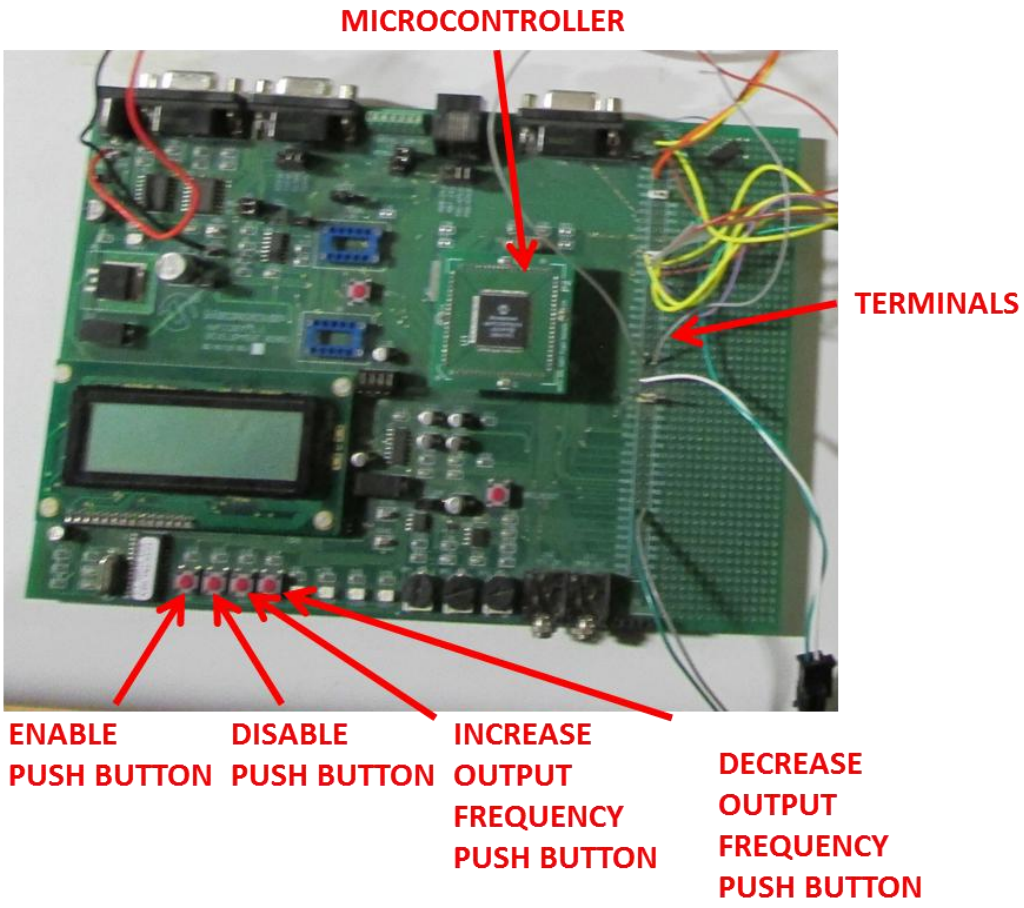


Figure 5-22 The Development board of microcontroller

5.3.2. Complex Programmable Logic Device (CPLD)

CPLD is used to generate IGBT gate signals for the power stage. Its objectives are explained in section 5.3.

CPLD can be programmed by programming languages such as Verilog and VHDL. In this design logic circuit is designed in Xlinx software. Xlinx software converts the logic circuit to Verilog language. CPLD logic circuit for one phase is shown in Figure 5-23. AND gates, OR gates, SR flip flops and counters are used. For each phase 2 PWM signals, 2 inductor current signals of converter and one "zero signal" are input to CPLD and 4 PWM signals are output which are sent to gates of IGBTs of the corresponding phase.

According to PWM signal coming from microcontroller and inductor current threshold signals coming from comparators, gate signals of IGBT's are produced.

When inverter is disabled, "zero signal" is sent from microcontroller. "Zero signal" disables switching and turns off all switches except S3 which is shown in Figure 5-5. S3 is turned on to transfer the energy generated by motor even if inverter is disabled.

When inverter is enabled and inductor currents do not exceed their threshold levels, CPLD only doubles the signal quantity coming from microcontroller. 6 PWM signals generated by microcontroller are received and CPLD generates inverses of these signals and produces 12 PWM signals. Another purpose of using CPLD is to set dead time between turning off and turning on of two switches. Counters are used to set 3uS dead time which is higher than maximum turn of time used IGBT. Maximum turn of time given in the datasheet is 2.8uS.

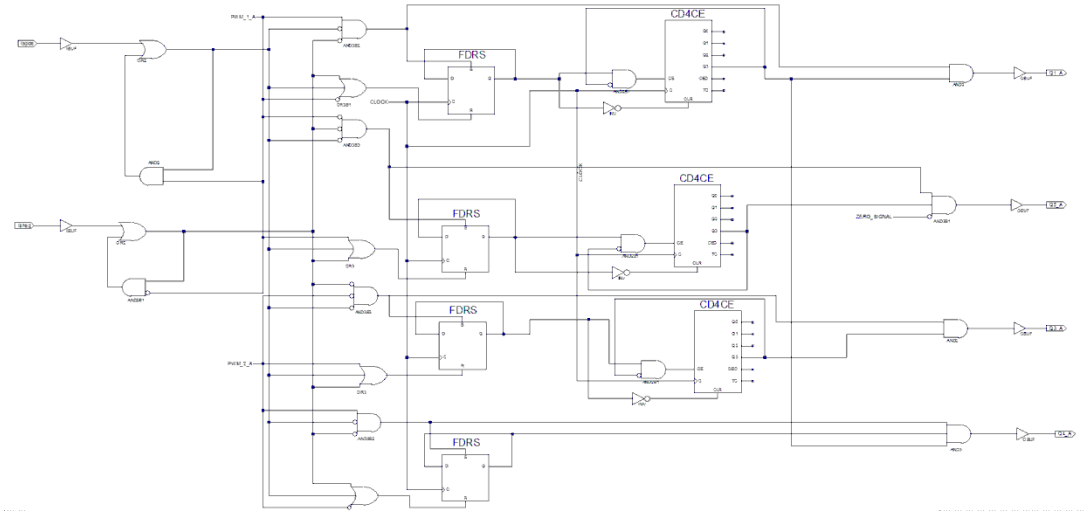


Figure 5-23 CPLD Logic Circuit for one phase

When inverter is enabled and one or more inductor current exceeds current threshold, CPLD turns off the switch or switches related, to decrease current level. Current threshold can be exceeded in both ways positive and negative. Positive current is defined as current flowing from the input to the output.

Exceeding positive current threshold is caused by S1 and S4 switches according to mode of operation. During the buck operation, it is caused by S1. Current path of converter in buck mode is shown in Figure 5-6. During buck-boost operation it may be caused by S1 or S1 and S4, the current paths are shown in Figure 5-9 and Figure 5-8, respectively. When positive current threshold is exceeded, S1 and S4 are turned off for that switching period. Signal path which turns off S2 via the logic sequence in the CPLD is shown in Figure 5-24.

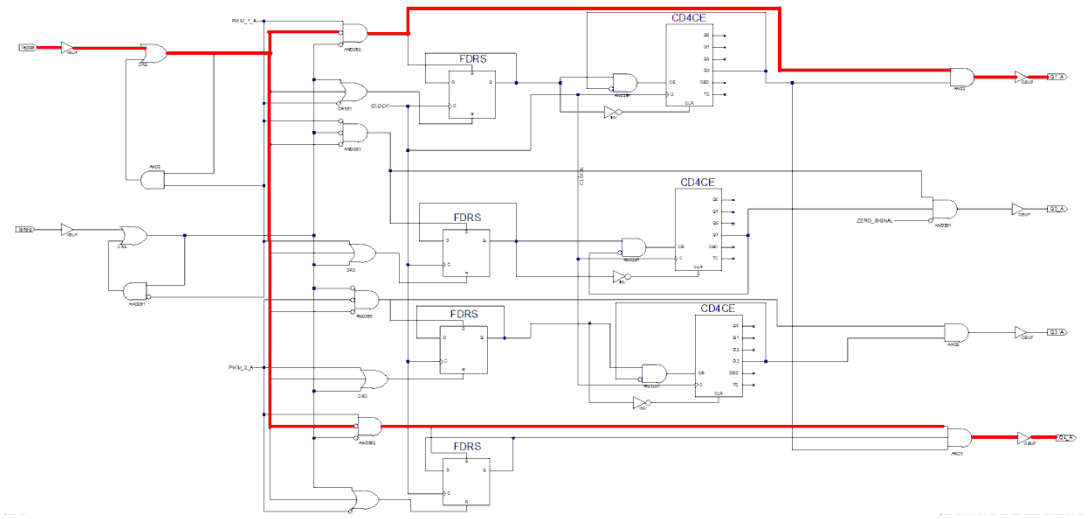


Figure 5-24 Signal Path which turns off S1 and S4 when positive current threshold is exceeded

Exceeding negative current threshold is caused by S2 and S3 switches. Current path of converter in this state is shown in Figure 5-10. If negative threshold is exceeded, only S2 is turned off. S3 cannot be turned off since load inductance will cause breakdown of S3. When S2 is turned off, inductor currents feed input capacitors and its current decreases. Signal path which turns off S2 is shown in Figure 5-25.

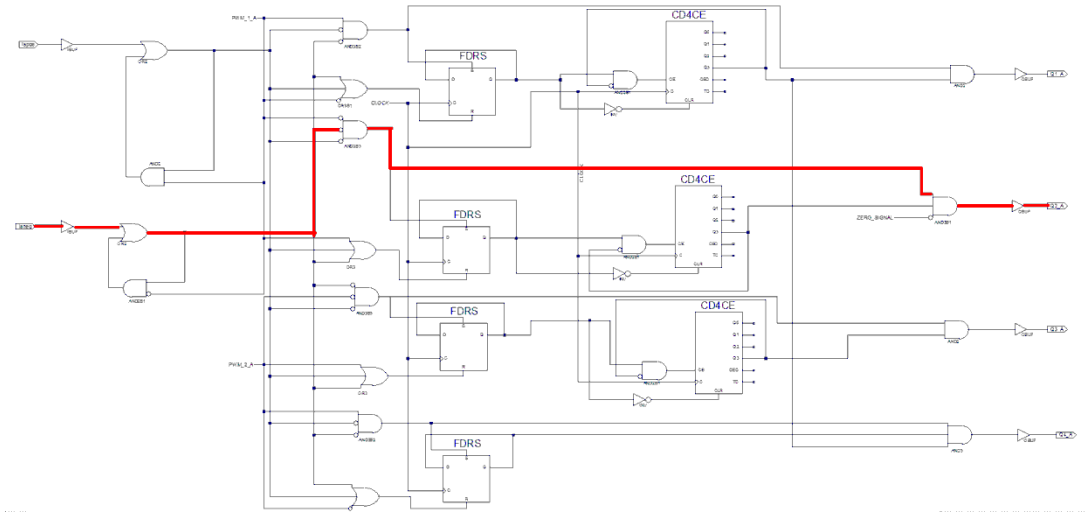


Figure 5-25 Signal Path which turns off S1 and S4 when positive current threshold is exceeded

5.3.3. Hall Effect Sensors and Comparators

Hall Effect sensors are used to measure inductor current. Total of 3 Hall Effect sensors are used in the power circuit. Hall Effect sensors are shown in Figure 5-21. They are placed between inductor and switches S3 and S4. Hall Effect devices produce voltage signal which is proportional to current passing through this device. This voltage is compared with preset values standing for current limits. 2 comparators are used for each hall-effect sensor where one compares with positive threshold and one compared with negative threshold. When positive current threshold is exceeded, a signal is formed and sent to CPLD meaning that related phase inductor current exceeded the positive threshold. Similar action is taken for negative threshold. Total of 6 signals are sent to CPLD, positive and negative for each phase. Current limits are determined by simulations. Simulation results are shown in Chapter 6. Positive current threshold is set to 20A and negative current threshold is set -20A.

5.4. Software Design

Software described in this section runs on the microcontroller. Main objective of the software is to produce PWM signals. In the application here voltage feedback from the output is not used. The system is feedforward controlled and the duty cycles are set according to DC link voltage level. Thus it is necessary to read DC link voltage through an ADC port. Output frequency can be changed during operation; two push buttons are used to increase and decrease the output frequency. Two push buttons are used to enable and disable to inverter. Software reads the “states” of these push buttons. Software consists of two parts which are the main function and the time interrupt function parts. Reading input voltage and switch states are done in main function part. PWM signal generation is performed in the time interrupt function part.

Figure 5-26 shows the flowchart of the main function part.

Block 1 in Figure 5-26, disables the inverter. When microcontroller is first energized, inverter starts at disabled mode.

Block 2 in Figure 5-26, sets the default values for variables used in the software. These default values are the output frequency which is set to 10Hz and switching frequency which is set to 10kHz. Output frequency can be changed by push buttons but switching frequency is always constant.

Block 3 in Figure 5-26, enables the time interrupt. When time interrupt is enabled, microcontroller interrupts repeatedly within set period. Its period is changed and set if frequency setting push buttons are pressed. When timer interrupt occurs, software goes to time interrupt function.

Block 4 in Figure 5-26, reads the states of enable and disable push buttons.

Block 5 in Figure 5-26, checks the state of disable push button. If disable push button is pressed it disables the inverter at block 6 and goes to block 4 again. When inverter is disabled, a signal named “zero signal” is sent to CPLD which turns off switching.

Block 7 in Figure 5-26, checks the state of inverter and enable push button. If state of inverter is “disabled”, the software goes to block 6. If enable push button is pressed or state of inverter is “enabled”, the software goes to block 8.

Block 8 in Figure 5-26 reads the DC link voltage level by ADC.

Block 9 in Figure 5-26 reads the states of output frequency setting push buttons.

Block 10 in Figure 5-26 checks the state of frequency increase push button. If frequency increase push button is pressed, software goes to block 11. Otherwise software goes to block 12.

Block 11 in Figure 5-26, increases output frequency by 1Hz. Maximum frequency which can be set is 75Hz.

Block 12 in Figure 5-26, checks the state of frequency decrease push button. If frequency decrease push button is pressed, software goes to block 13.

Block 13 in Figure 5-26, decreases output frequency by 1Hz. Minimum frequency which can be set is 10Hz.

Finally software returns to block 3 and updates the period of time interrupt if output frequency is changed.

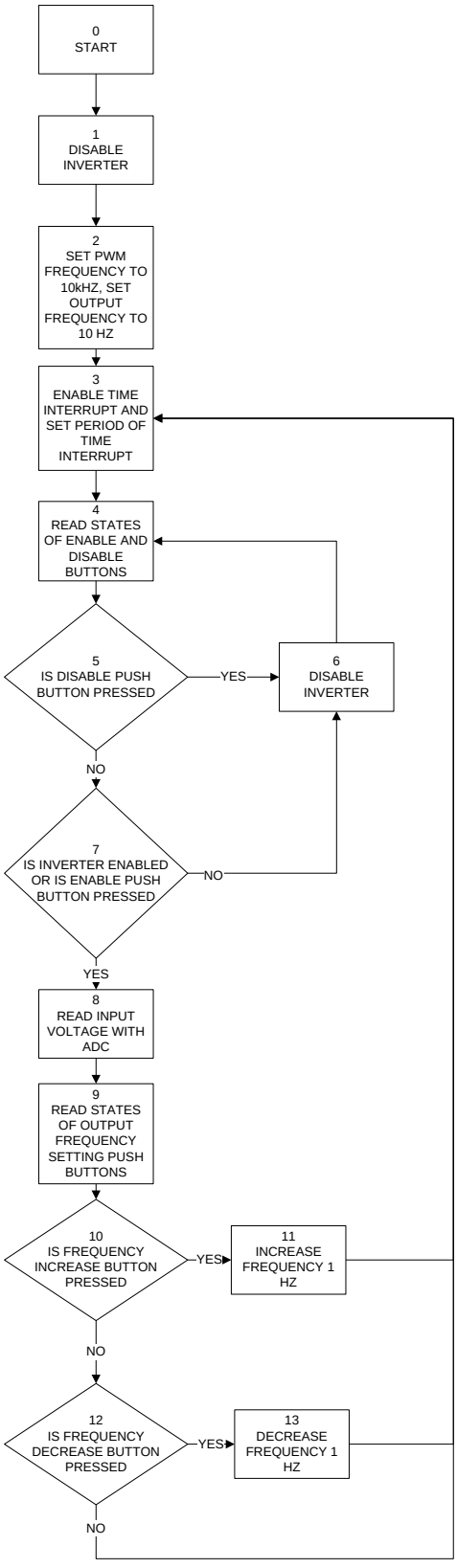


Figure 5-26 Flowchart of main function

Time interrupt is set according to the output frequency setting. Period of output voltage is divided into 100 steps. For example, if period is 20mS, for each 200uS interval an interrupt signal is generated. There is a variable called “time step” in time interrupt function. This variable is increased for every time step, until it reaches 100. When it reaches 100, the variable is set to 0.

A lookup table is generated for sine values of three phases corresponding to every step. Figure 5-27 shows flowchart of the time interrupt function.

Block 14 in Figure 5-27, checks the state of inverter. If inverter is not enabled or output overvoltage signal is generated, software goes to block 16.

Block 15 in Figure 5-27, checks the DC link voltage level. If DC link voltage is between 380V and 600V, input voltage is proper. If input voltage is not within set limits, software goes to block 16. If input voltage is within set limits, software goes to block 17.

Block 16 in Figure 5-27, disables the inverter.

Block 17 in Figure 5-27, calculates desired output voltage levels for each phase. Output voltage peak value is determined according to frequency. The voltage level is determined to keep V/f ratio constant at 380Vrms line to line over 50 Hz for frequencies lower than 50Hz, and 380Vrms line to line is set for the output peak value for frequencies greater or equal to 50Hz. Desired voltage levels for that instant, are calculated by using output voltage peak value and lookup table which holds the sine values corresponding to that time step.

Block 18 in Figure 5-27, calculates the duty cycles of switches. Duty cycles are formulized in section 5.2. By using DC link voltage level and desired output voltage level, required duty cycles are determined.

Block 19 in Figure 5-27, sets the calculated duty cycles to PWM ports of the microcontroller.

Block 20 in Figure 5-27, increases “time step” by 1.

Block 21 in Figure 5-27, checks the value of “time step”. If it is equal to or greater than 100, “time step” variable is set to zero. At the end of time interrupt, software returns to main function.

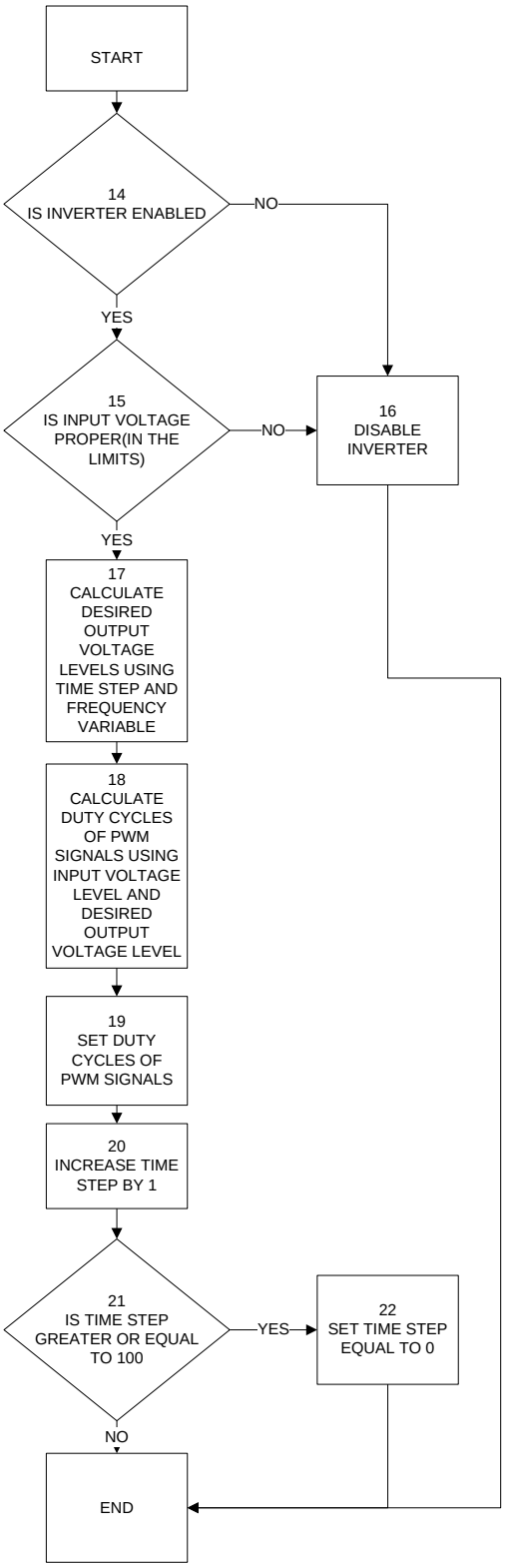


Figure 5-27 Flowchart of time interrupt function

5.5. Obtaining DClink Voltage

To obtain DC link voltage, grid connected 3 phase AC source is used. Nominal phase voltage of grid is 220V and nominal frequency is 50Hz. Variac is used to set input voltage level. 3 phase full bridge is used to rectify AC voltage and feed DC link capacitors. 3 phase thermic magnetic shelter is added for overcurrent protection. A mechanical switch which is parallel to 1kΩ resistor is used to charge DC link capacitors. Switch is initially made not conducting manually. Capacitors are charged over 1kΩ resistor. After capacitors are charged, switch is made conducting manually. Block diagram of DC link is shown in Figure 5-28.

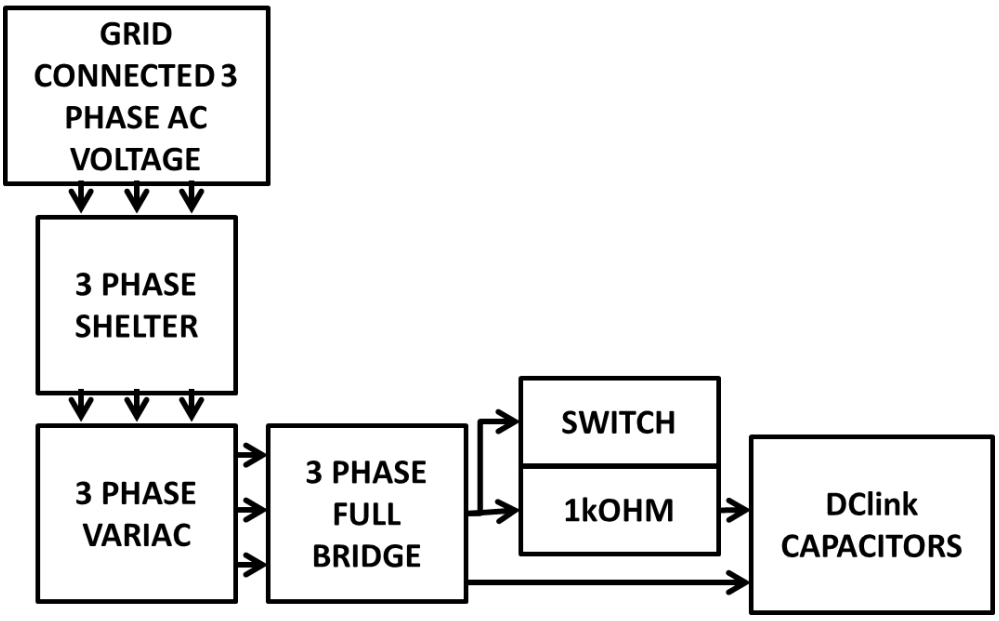


Figure 5-28 Block Diagram of DC link

5.5.1. Capacitance Value Calculation

DC link capacitance value is calculated first. Maximum voltage ripple at DC link occurs at minimum voltage which is 400V for the system. DC link is charged 6 times in one period when it is fed from 3 phase full bridge rectifier. Capacitor current voltage relationship is shown in equation 5.13. Capacitor is discharged with output power. Capacitor current is obtained by dividing output power to input voltage. It is

assumed that capacitor discharges maximum 25V. Period of grid is 20mS, one sixth of it is used as Δt. These values are put to equation 5.13 and equation 5.14 is obtained.

$$I_C = C * \frac{\Delta V}{\Delta t} \tag{5.13}$$

$$\frac{2500}{400} = C * \frac{25}{(20m/6)} \tag{5.14}$$

$$C = 833uF \tag{5.15}$$

Calculated capacitance value is 833uF. 330uF capacitances are used for DClink. By connecting two of them series and five of them parallel, 825uF of equivalent capacitance is obtained which is shown in equation 5.16.

$$C_{eq} = \frac{330uF}{2} * 5 \tag{5.16}$$

Rectifier circuit is simulated with 825uF capacitance to see voltage ripple at maximum power and minimum input voltage. Simulated ripple voltage turned out to be 17V which is less than 25V assumption. Voltage ripple is smaller because discharging time is smaller than the assumption.

5.5.2. Charging Resistor Calculation

Time constant for RC network is shown in equation 5.17. It is assumed that steady state voltage is reached at 5τ time. Charging time is aimed to be less than 10s. Resistor value needs to be less than 2.424kΩ which is calculated by inequality 5.18. 1kΩ is used as charging resistor.

$$\tau = R * C \tag{5.17}$$

$$5 * R * C < 10 \tag{5.18}$$

$$R < 2424.24\Omega \tag{5.19}$$

5.6. Summary

In this chapter design of the proposed topology is explained. First the power stage is designed. The power stage is designed to achieve two goals; obtaining sinusoidal output voltage and boosting input voltage. Components are chosen to allow designed inverter to operate from 400V to 540V DC input voltage, from 10Hz to 75Hz output frequency and supply rated power of 2.5kW at rated 50Hz output frequency operation. Power stage is simulated to verify the system operation. Simulation results are explained in Chapter 6 to make comparison with actual test results. Simulations are done for different input voltages to verify boosting capability. Resistive and inductive load simulations are done to observe the THD of the output voltage and the efficiency of the converter for different output frequencies. After boosting capability and producing sine wave output capability is verified with simulation, control stage is designed to meet the requirements from the converter.

The control stage of the converter is designed to achieve three main goals; to generate PWM signals of IGBT's according to DC link voltage level, to achieve over-voltage protection and over-current protection. Components are chosen to satisfy these goals.

Thirdly the software stage is designed to produce the gate signals to IGBT's to achieve the desired output voltage. The output frequency setting and enable-disable operation is achieved by the software.

Finally, obtaining the DC link input voltage to the system is described. In the experiments the test circuit is designed with a variable voltage AC input obtained from a three-phase variac. This is followed by a diode rectifier to obain the DC bus voltage supplying the power stage. To adjust DC link Voltage AC input voltage is adjusted.

The design is implemented to verify the design of the converter and observe its performance during operation. Tests are conducted to observe boosting capability

and producing sine wave output capability. Test procedure and test results are explained in Chapter 6.

In Figure 5-29, the implemented power stage of the converter is shown. In this figure box numbered 1 show the IGBT module used in the input side. Box numbered 2 shows the inductors used in the converter. Box numbered 3 shows the IGBT modules used in output side. Box numbered 4 shows the output capacitors. Box numbered 5 shows input filter capacitances. Box numbered 6 shows DC-link capacitors. Box numbered 7 shows 3 phase full bridge rectifier and DC-link charging circuit.

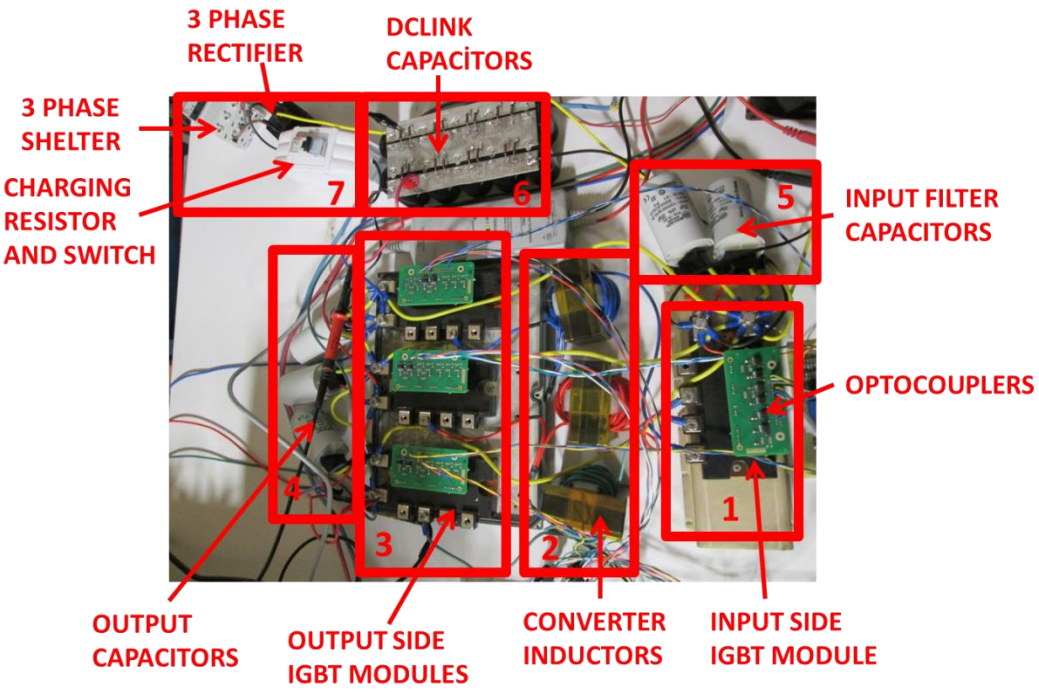


Figure 5-29 The Power Stage

CHAPTER 6

TESTS AND RESULTS

Design of the proposed topology is described in Chapter 5. In this chapter, simulation and test results are explained and compared to verify operation of the proposed topology. Tests in this chaptercan be grouped into 4 parts. First with no load tests, inductor current, inductor voltage, switch voltage and capacitor voltage waveforms are obtained and are presented. Experiments performed are repeated also in the simulation software and their results are compared. Operation of inverter is explained and the design process is verified by this study.

Secondly, tests are performed while the implemented converter is operating at steady-state conditions. In this investigation the efficiency and the THD of the converter output are analyzed for the designed DC link voltage range (400V-540V), for the designed output frequency range and for different resistive and inductive loads.

Thirdly, the performance of the converter is tested while the load is suddenly switched “on” and “off”. This is called the transient operation. The transient-operation test waveforms are obtained for different DC link voltages at rated output frequency. Lastly an induction motor (3.5kw, 4 pole, 1400 rpm) is driven by the designed converter and the performance of the converter with this type of load is tested. The efficiency of the converter is measured and output waveform THD is measured while driving the test induction motor.

6.1. No-Load Tests

These tests are done to show voltage and current waveforms and operating principle of the converter. The test results are also compared with simulation results to verify reliability of simulation results. Test equipment is described in section 6.1.1. No load tests are done with two DC link voltage level. First DC link voltage is set to 540V which is nominal grid voltage and waveforms are observed. By these tests operation at nominal input voltage is verified. Then DC link voltage is set to 400V which is the minimum voltage that converter is designed to operate and waveforms are observed. By these tests boosting capability is verified. By no load tests, effect of voltage ripple in DC link voltage is minimized. Also software updates the level of DC link in each two switching cycle. For example, DC link voltage level is updated each 400uS for 50Hz operation.

6.1.1. Test Equipment

VARSAN VARIAC: This equipment is used to supply power stage. Input voltage level is set by this equipment.

INSTEK GPS-3303: This equipment is used to supply control circuit. Two channels are used. 8V is used to supply control circuit and 24V is used to supply isolated converters which are used for gate drive circuit.

Agilent Technologies MSO-X 3024 Oscilloscope: This device is used to obtain voltage and current Waveforms. Two 100:1 voltage probes, one differential probe and 1 current probe is attached.

Agilent Technologies N2790A 100MHz differential Probe: This probe is used as voltage probe. It was necessary for measuring switching waveforms.

FLUKE i30S AC/DC current Clamp: This device is clamped over cable to measure current waveform.

6.1.2. 540V DC link Voltage Operation

A three phase bridge rectifier fed from variac is used to obtain the desired DC link voltage. First DC link capacitors are charged by charging resistor. After the capacitors are charged, charging resistor is bypassed by a switch manually. In this document test results obtained only at 50 Hz are presented. Test results obtained for other frequencies are not presented but they are summarized in the tables where the THD value of output voltage and RMS value of output voltage is given. To make comparison both test results and simulation results are shown consecutively.

All voltage measurements are done relative to negative terminal of DC-link unless it is specified. From Figure 6-1 to Figure 6-32, odd numbered figures show test results and even numbered figures show simulation results.

6.1.2.1. No Load Three Phase Output Voltages at 50Hz

Output voltage waveforms of the designed converter are shown in Figure 6-1 and Figure 6-2. These waveforms show how three phase voltage waveform is obtained by the three converters. In the figure, yellow colored waveform is phase A output voltage, green colored waveform is phase B output voltage and blue colored waveform is phase C output voltage. Pink colored waveform is line to line voltage V_{ab} and orange colored waveform is line to line voltage V_{bc}.

In Figure 6-1, Figure 6-2, output voltages of converters are in same axis to show phase difference between converters. Each converter makes switching action two third of period and only two converters are switching at the same time.

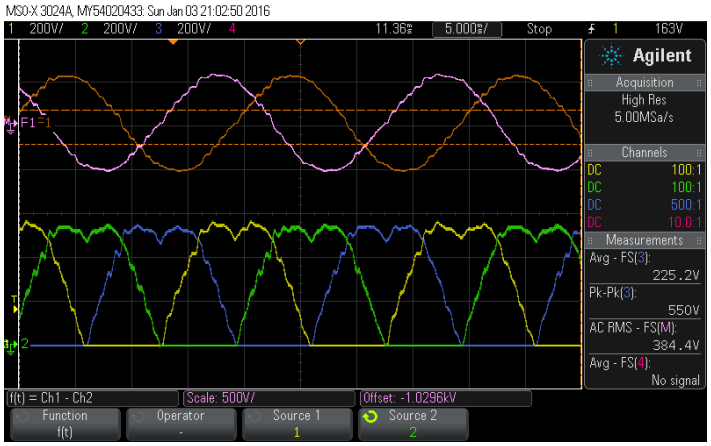


Figure 6-1 Phase Voltages (A:yellow, B:green, C:blue) and Line to Line Voltages (V_{ab}:pink, V_{bc}:orange) obtained by Test Results

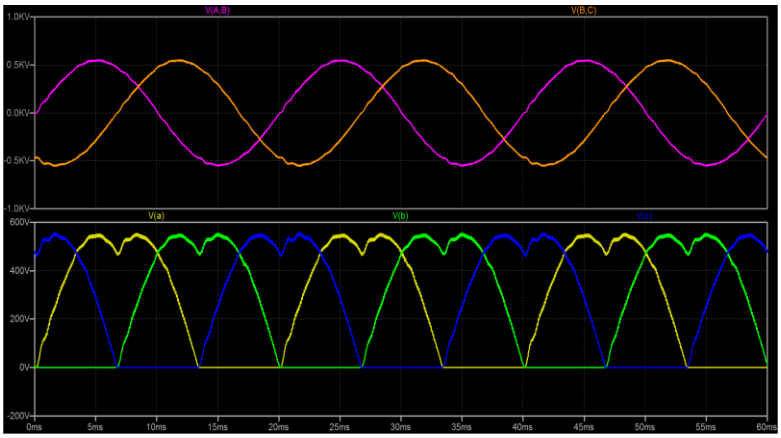


Figure 6-2 Phase Voltages (A:yellow, B:green, C:blue) and Line to Line Voltages (V_{ab}:pink, V_{bc}:orange) obtained by Simulation Results

Some oscillations are observed at output voltages of converters which is also seen on line to line voltages in test results. These oscillations are similar to voltage ripple, however they are called oscillations since they are caused by oscillations in inductor current. Inductor current waveforms are shown in next section. Possible reasons for oscillations in inductor current are also described in next section.

Waveforms are also observed for 10Hz, 30Hz and 75Hz operation. THD and RMS value of output line to line voltage are shown in Table 6-1. Current and voltage

waveforms of test results and simulation results are similar in terms of shape and magnitude.

6.1.2.2. Inductor Current Waveforms

Inductor current waveforms are observed to show current ripple in buck mode and buck boost mode. When mode transition occurs, shape of inductor current changes. Change of shape will be shown in the figures. Inductor current ripple values will be discussed in section 6.2 with steady state load tests.

Since converters are identical, only phase "a" inductor current is shown. From Figure 6-3 to Figure 6-12, phase A output voltage with yellow color, DC link voltage with blue color and phase A inductor current with magenta color are shown. Figure 6-3 and Figure 6-4 show voltage and current waveforms for one cycle. Phase "a" voltage and DC link voltage are on same axis to show where mode transition occurs. Remaining figures are obtained by zooming in these waveforms.

When phase a voltage waveform is observed in Figure 6-3, there are points where slope of output voltage changes discreetly. These points are called breakpoints and they are shown in the figure.

Figure 6-3 Phase A Voltage(yellow), DC link Voltage(blue) and Phase A Inductor Current(magenta) obtained by Test Results

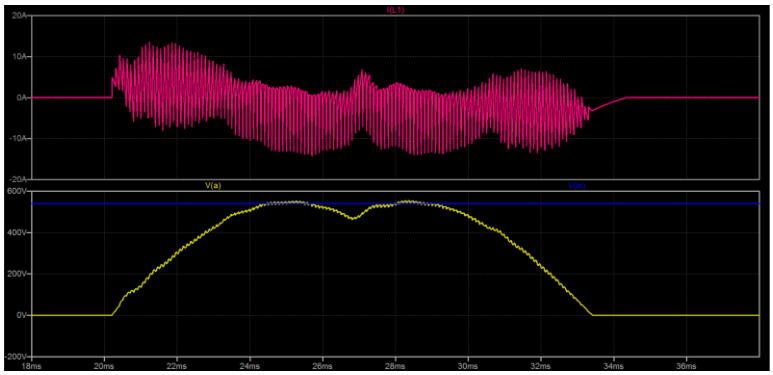


Figure 6-4 Phase A Voltage(yellow), DC link Voltage(blue) and Phase A Inductor Current(magenta) obtained by Simulation Results

There is a low frequency component in inductor current waveform. This component is defined as oscillation. Oscillation in inductor current is higher in test results with respect to simulation; this may be because duty cycle changes in continuous way in simulation while it changes in the designed circuit at every time step which is determined by capability of the microcontroller. These oscillations also affect the output voltage waveform. For 50Hz operation duty cycles are updated every other switching cycle. For lower frequency operation, they are updated less frequent which also causes higher overshoot and undershoot in inductor current and results in higher THD. These oscillations can be damped if current mode control of inductor is used. The design was focused on operation of topology and no attention was paid to control aspects. Designing control loop is a work which must be focused on later. Another reason for these oscillations is the breakpoints at output voltage waveform. Capacitor current varies with derivative of its voltage. There are three breakpoints in voltage waveform which are shown in Figure 6-3. In these breakpoints, capacitor current changes suddenly, this results inductor current to increase and decrease suddenly and cause oscillations in inductor current. THD values of 75Hz operation is worse than 50Hz operation, this is caused by higher rate of voltage change occurs when frequency increases. The capacitors are tied between phase voltages and the negative terminal of DC link. If capacitors are connected in “Δ” or “Y” configuration, voltage over capacitors will be sinusoidal and no breakpoints at capacitor voltage will occur. Since capacitor voltage is sinusoidal, no sudden change

of capacitor current occurs. Thus inductor current does not overshoot or undershoot which decreases oscillations at inductor current and at output voltage. This would solve oscillation problem however it requires sensing the output voltages. When one converter is in non-switching state, S3 and S4 switches of that converter are required to conduct at the same time to connect that phase to ground with a non-inductive path. If inductive path occurs such as in this design, it causes spikes at output voltage waveform of other phases and causes breakdown of switches. Sensing output voltage is essential to conduct S3 and S4 switches at the same time, because output capacitor must be fully discharged before S3 and S4 are made conducting. Otherwise capacitor is discharged through low impedance path and large amount of current may pass over switches which may be harmful for switches and capacitor. In this design, since output voltages are not sensed, capacitors could not be connected in "Δ" or "Y" configuration.

Beginning of switching for phase "a" converter is shown in Figure 6-5 and Figure 6-6. In these figures converter is operating in buck mode since output voltage is less than 80% of DC link voltage. Inductor current shape is similar to buck converter in continuous conduction mode.

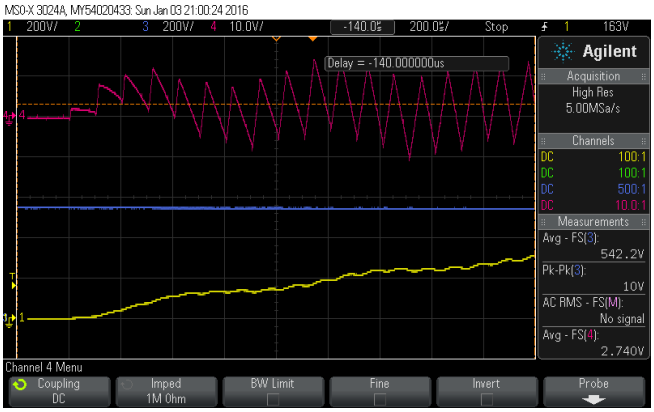


Figure 6-5 Phase A Voltage(yellow), DC link Voltage(blue) and Phase A Inductor Current(magenta) obtained by Test Results

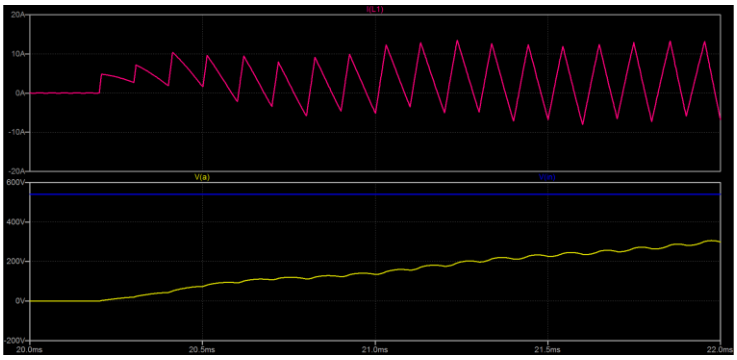


Figure 6-6 Phase A Voltage(yellow), DC link Voltage(blue) and Phase A Inductor Current(magenta) obtained by Simulation Results

When output voltage is higher than 80% of DC link voltage which is 432V when DC link is 540V, the converters switch to operation in buck-boost mode. Inductor current changes its shape form triangular to trapezoidal. Change of shape of inductor current when mode transition occurs, is shown in Figure 6-7 and Figure 6-8.

Figure 6-7 Phase A Voltage(yellow), DC link Voltage(blue) and Phase A Inductor Current(magenta) obtained by Test Results, Transition from buck to buck boost mode

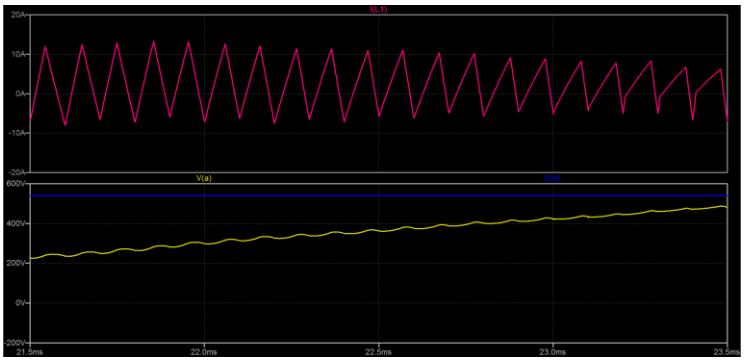


Figure 6-8 Phase A Voltage(yellow), DC link Voltage(blue) and Phase A Inductor Current(magenta) obtained by Simulation Results

At the break point of output voltage waveform which is shown in the middle according to time scale in Figure 6-3, output capacitor starts to charge suddenly from discharging, which results in inductor current to increase. This state is shown in Figure 6-9 and Figure 6-10. This also causes to oscillations in inductor current as can be traced from Figure 6-9. Mean current of inductor overshoot and undershoots. Oscillations in inductor current also cause oscillations at the output voltage as it can be traced from Figure 6-3.

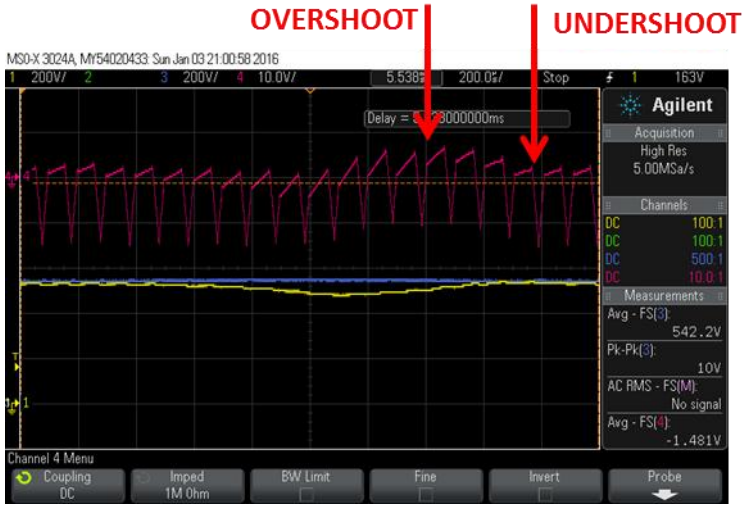


Figure 6-9 Phase A Voltage(yellow), DC link Voltage(blue) and Phase A Inductor Current(magenta) obtained by Test Results

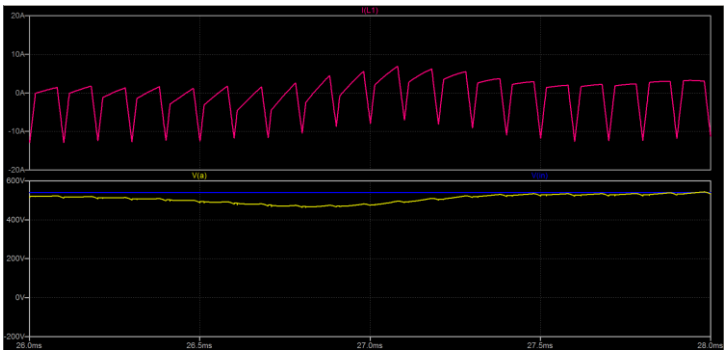


Figure 6-10 Phase A Voltage(yellow), DC link Voltage(blue) and Phase A Inductor Current(magenta) obtained by Simulation Results

When output voltage decreases to a level lower than 80% of DC link voltage, the converter starts to operate at buck mode again. Inductor current is in buck mode. Mode transitions are shown in Figure 6-11 and Figure 6-12.

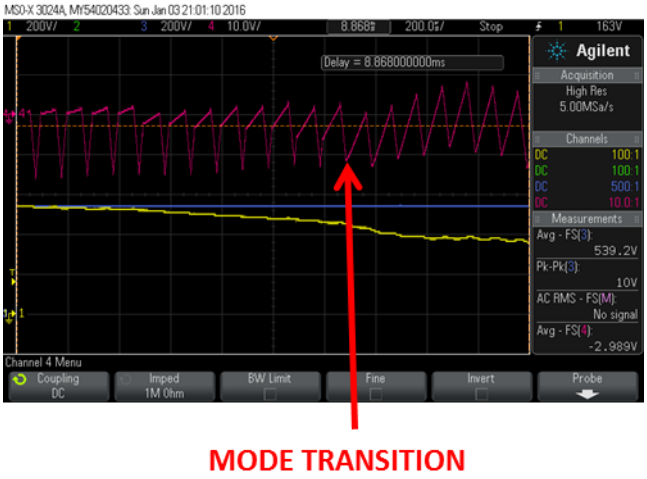


Figure 6-11 Phase A Voltage(yellow), DC link Voltage(blue) and Phase A Inductor Current(magenta) obtained by Test Results, Transition from buck-boost to buck mode

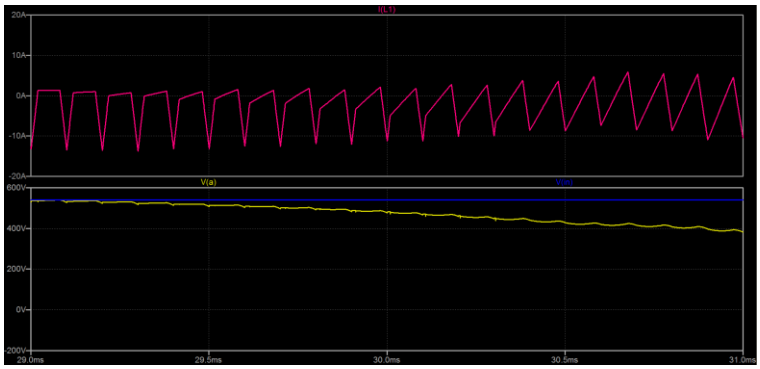


Figure 6-12 Phase A Voltage(yellow), DC link Voltage(blue) and Phase A Inductor Current(magenta) obtained by Simulation Results

If oscillations on inductor current are discarded, test and simulation results are similar with respect to inductor current shape and magnitude in different operating modes. As described in section 6.1.2.1., the tests are also conducted for different frequencies. Oscillations on output voltage waveforms are caused by overshoot and undershoot of inductor current. For lower frequencies, overshoot and undershoots of inductor current are higher due to increase in time step. For higher frequencies, they are higher due to higher slew rate of output voltage waveform.

6.1.2.3. Voltage Waveforms of S1 and S2 Switches

Circuit diagram of the converter is shown in Figure 5-5. Voltage across collector and emitter of S2 are shown in figures from Figure 6-13 to Figure 6-22 with blue colored waveform. Voltage over collector and emitter of S1 is not shown but it can be obtained by subtracting blue colored waveform from DC link voltage. In these figures DC link voltage is shown with green color, output voltage is shown with yellow color and inductor current is shown with magenta color. As described in previous section, S1 and S2 are switching for 2/3 of a period. Figure 6-13 and Figure 6-14 show waveforms for one period. These waveforms are presented to show switch voltage rating are appropriate and variation of “duty1” as described in section 5.2. DC link voltage and output voltage waveforms are shown to emphasize when mode

transition occurs. Inductor current waveform is shown to observe current waveform in different states of S1 and S2.

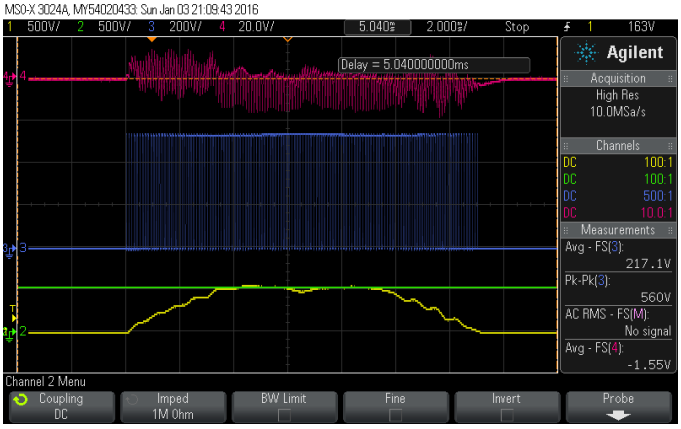


Figure 6-13 Phase A Voltage(yellow), DC link Voltage(green), Voltage Waveform across S2(blue) and Phase A Inductor Current(magenta) obtained by Test Results

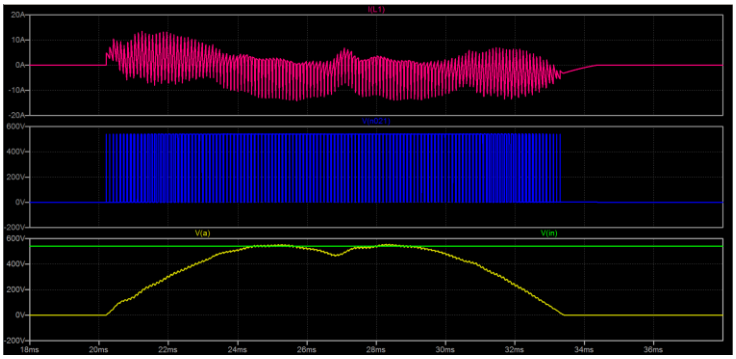


Figure 6-14 Phase A Voltage(yellow), DC link Voltage(green), Voltage Waveform across S2(blue) and Phase A Inductor Current(magenta) obtained by Simulation Results

The designed converter starts operating in buck mode, duty cycle “duty1” increases to obtain higher voltage level at the output. Figure 6-15 and Figure 6-16 show starting point of switching.

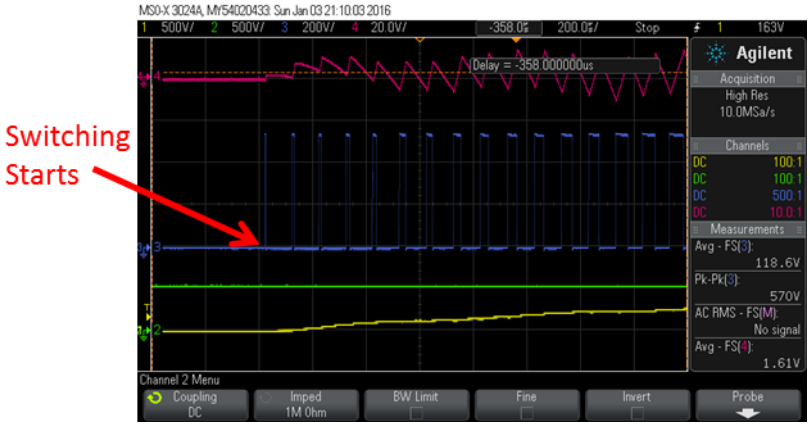


Figure 6-15 Phase A Voltage(yellow), DC link Voltage(green), Voltage Waveform across S2(blue) and Phase A Inductor Current(magenta) obtained by Test Results

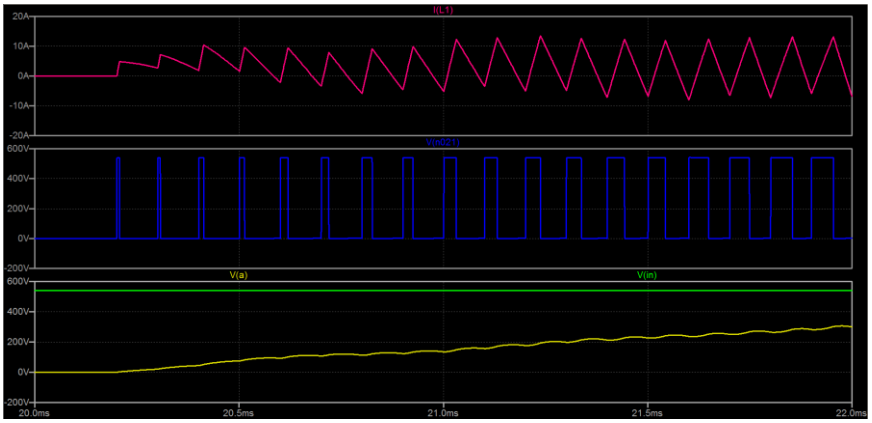


Figure 6-16 Phase A Voltage(yellow), DC link Voltage(green), Voltage Waveform across S2(blue) and Phase A Inductor Current(magenta) obtained by Simulation Results

In buck-boost mode, duty cycle “duty1” for switches S1 and S2 is constant and 80%. Obtaining desired voltage level is done by output switches S3 and S4. Constant duty cycle operation for “duty1” is shown in Figure 6-17 and Figure 6-18.

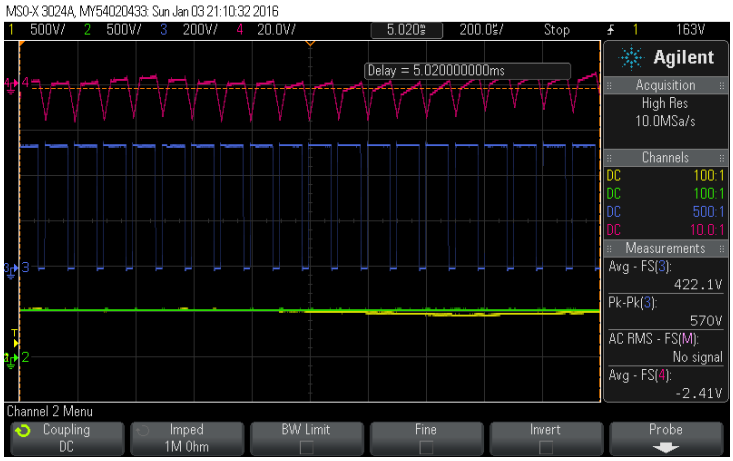


Figure 6-17 Phase A Voltage(yellow), DC link Voltage(green), Voltage Waveform across S2(blue) and Phase A Inductor Current(magenta) obtained by Test Results

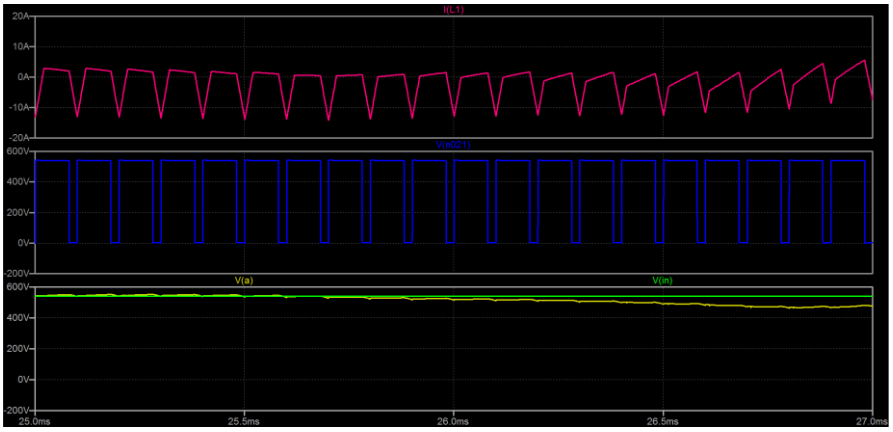


Figure 6-18 Phase A Voltage(yellow), DC link Voltage(green), Voltage Waveform across S2(blue) and Phase A Inductor Current(magenta) obtained by Simulation Results

When output voltage decreases below 80% of DC link voltage, converter starts operating at buck mode again, duty cycle “duty1” for switches S1 and S2 starts decreasing. Mode transition is shown in Figure 6-19 and Figure 6-20.

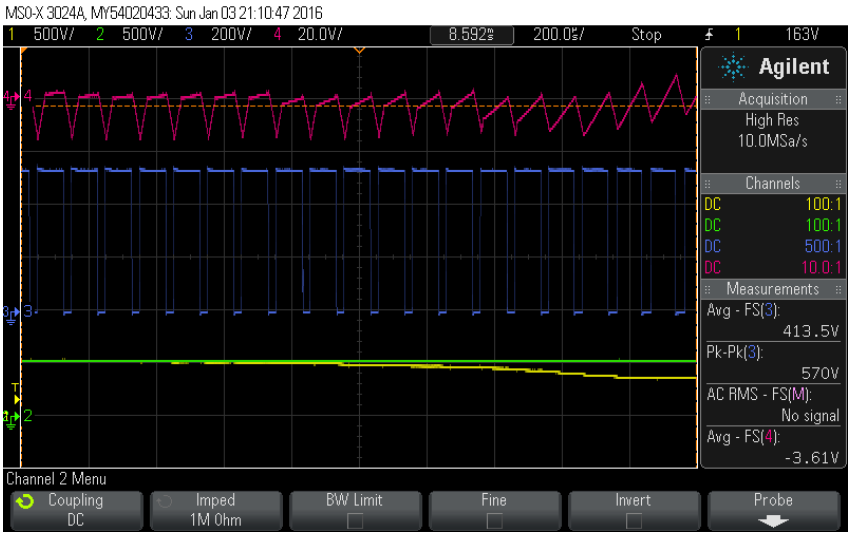


Figure 6-19 Phase A Voltage(yellow), DC link Voltage(green), Voltage Waveform across S2(blue) and Phase A Inductor Current(magenta) obtained by Test Results

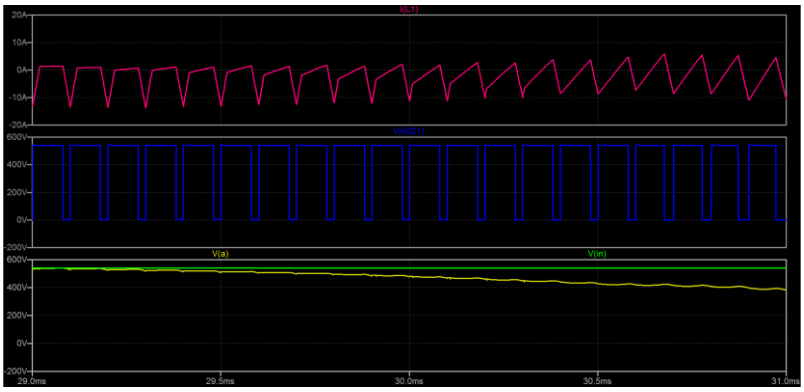


Figure 6-20 Phase A Voltage(yellow), DC link Voltage(green), Voltage Waveform across S2(blue) and Phase A Inductor Current(magenta) obtained by Simulation Results

Duty cycle “duty1” for switches S1 and S2 decreases to 0 and switching stops. These waveforms are shown in Figure 6-21 and Figure 6-22.

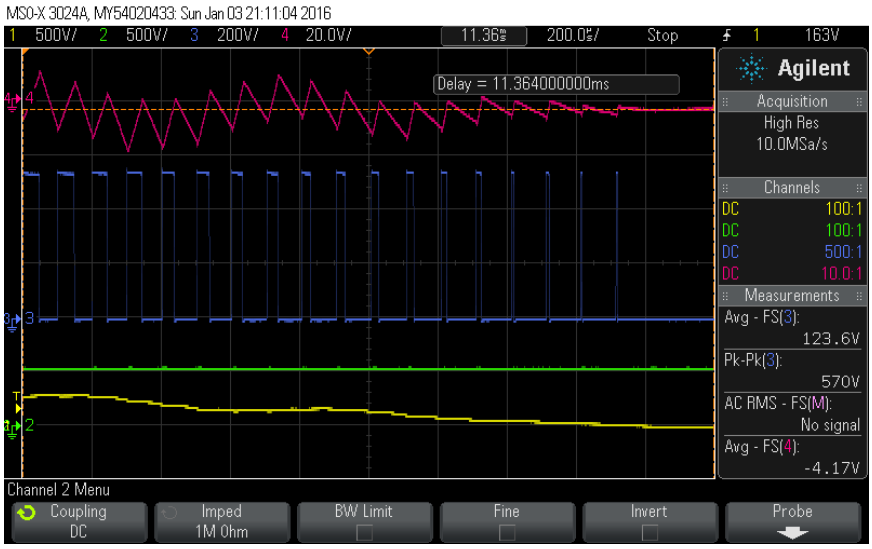


Figure 6-21 Phase A Voltage(yellow), DC link Voltage(green), Voltage Waveform across S2(blue) and Phase A Inductor Current(magenta) obtained by Test Results

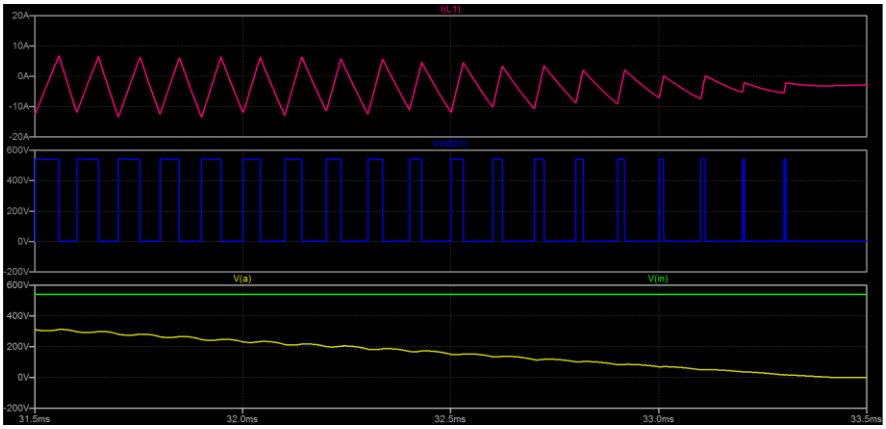


Figure 6-22 Phase A Voltage(yellow), DC link Voltage(green), Voltage Waveform across S2(blue) and Phase A Inductor Current(magenta) obtained by Simulation Results

Maximum voltage over S1 and S2 is equal to DC link voltage. In these tests, maximum voltage seen on S1 and S2 is equal to 540V. Switch voltage ratings are 1200V which is nearly double of required value. Switches are chosen in that manner because of two reasons; they have internal gate drive which eases the control and for future work where higher DC link voltages will be tested.

6.1.2.4. Voltage Waveforms of S3 and S4 Switches

Circuit diagram of the converter is shown in Figure 5-5. Voltage across collector and emitter of S4 are shown in figures from Figure 6-23 to Figure 6-30 with blue colored waveform. Voltage over collector and emitter of S3 is not shown but it can be obtained by subtracting blue colored waveform from output voltage. In these figures output voltage is shown with yellow color and inductor current is shown with magenta color. As described in previous section, S3 and S4 are switching in buck-boost mode. Figure 6-23 and Figure 6-24 show waveforms for one period. These waveforms are presented to show switch voltage rating are appropriate and variation of "duty2" as described in section 5.2.

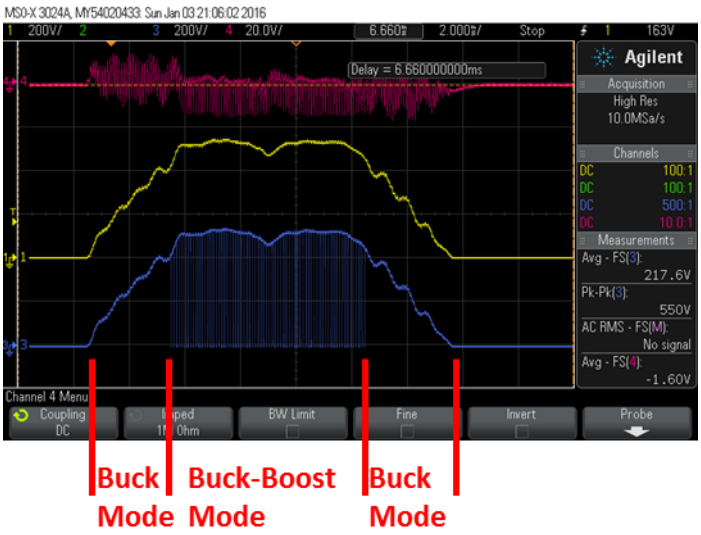


Figure 6-23 Phase A Voltage(yellow), Voltage Waveform across S4(blue) and Phase A Inductor Current(magenta) obtained by Test Results

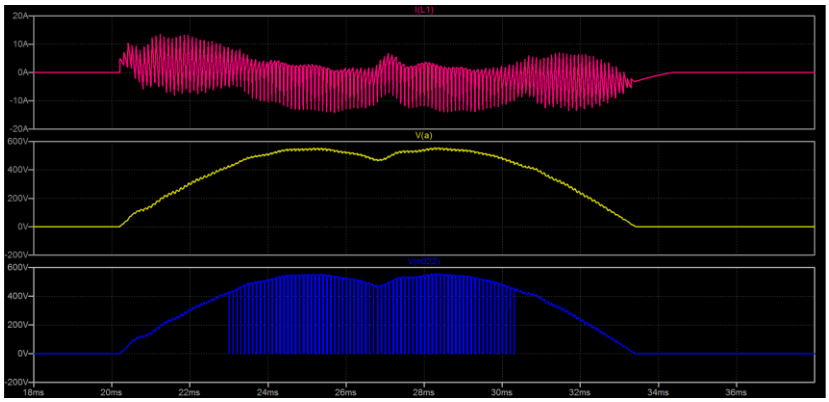


Figure 6-24 Phase A Voltage(yellow), Voltage Waveform across S4(blue) and Phase A Inductor Current(magenta) obtained by Simulation Results

While converter operates in buck mode, S3 is on and S4 is off. When output voltage is higher than 80% of DC link voltage, S3 and S4 start switching. Figure 6-25 and Figure 6-26 show starting point of switching.

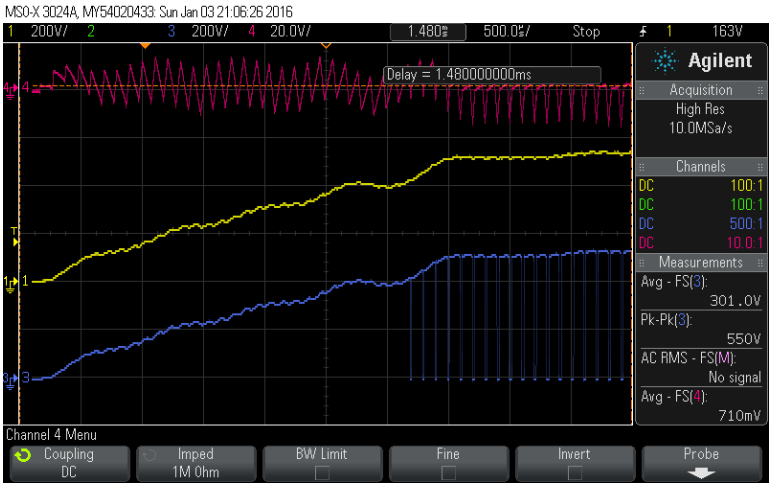


Figure 6-25 Phase A Voltage(yellow), Voltage Waveform across S4(blue) and Phase A Inductor Current(magenta) obtained by Test Results

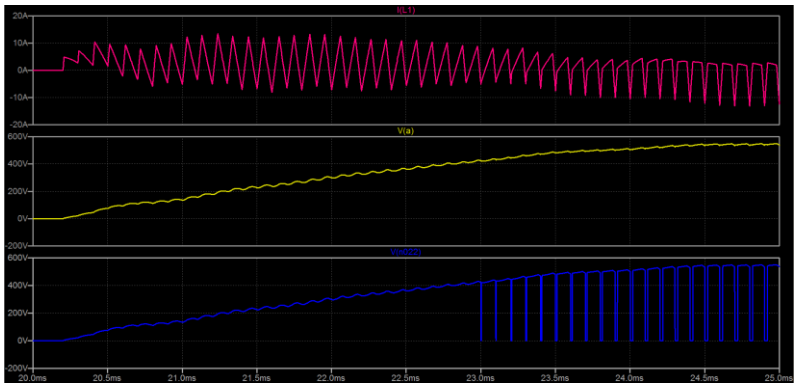


Figure 6-26 Phase A Voltage(yellow), Voltage Waveform across S4(blue) and Phase A Inductor Current(magenta) obtained by Simulation Results

To obtain higher output voltage, on time off S4 must be increased. In Figure 6-27 and Figure 6-28 on time of S4 is higher for higher output voltages. When S4 is conducting, inductor current increases with applied DC link voltage to its terminals.

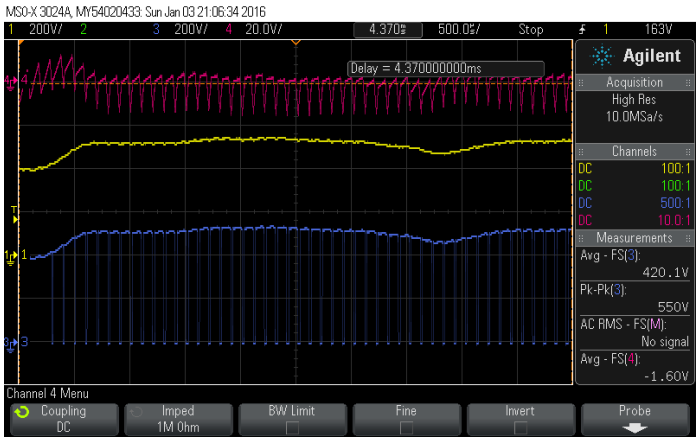


Figure 6-27 Phase A Voltage(yellow), Voltage Waveform across S4(blue) and Phase A Inductor Current(magenta) obtained by Test Results

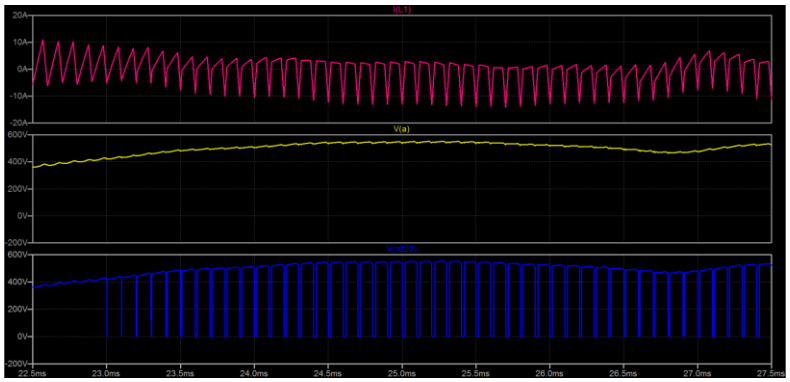


Figure 6-28 Phase A Voltage(yellow), Voltage Waveform across S4(blue) and Phase A Inductor Current(magenta) obtained by Simulation Results

When output voltage decreases below 80% of DC link voltage, converter starts operating at buck mode again, S3 is conducting and S4 is off. Mode transition is shown in Figure 6-29 and Figure 6-30.

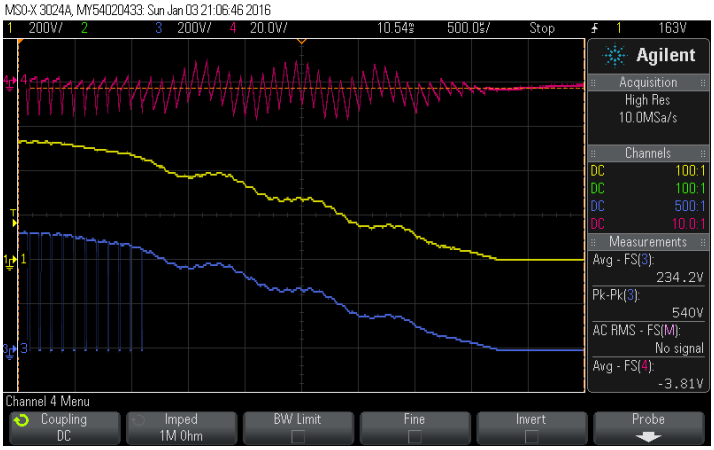


Figure 6-29 Phase A Voltage(yellow), Voltage Waveform across S4(blue) and Phase A Inductor Current(magenta) obtained by Test Results

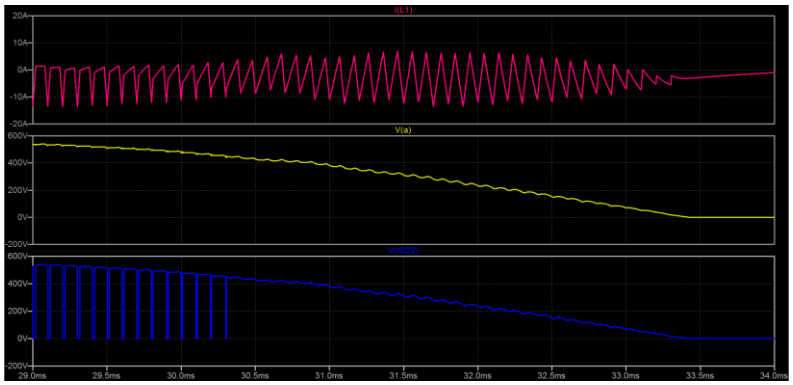


Figure 6-30 Phase A Voltage(yellow), Voltage Waveform across S4(blue) and Phase A Inductor Current(magenta) obtained by Simulation Results

In these tests, maximum voltage seen on S3 and S4 is equal to 540V. Switch voltage ratings are 1200V which is nearly double of required value. Switches are chosen in that manner because of two reasons; they have internal gate drive which eases the control and for future work where higher output voltages will be tested. DC link voltage and output voltage waveforms are shown to emphasis when mode transition occurs. Inductor current waveform is shown to observe current waveform in different states of S3 and S4.

6.1.2.5. Inductor Voltage Waveforms

Voltage over inductor is shown in Figure 6-31 and Figure 6-32 with blue color. In these figures output voltage is shown with yellow color, DC link voltage is shown with green color and inductor current is shown with magenta color. Voltage over inductor is the difference of voltage at midpoint of switches S1, S2 and voltage at midpoint of switches S3 and S4. These waveforms are shown to give insight about maximum voltage rating of inductor. The value is the equal to maximum of DC link voltage and output voltage. In these tests they are equal and 540V.

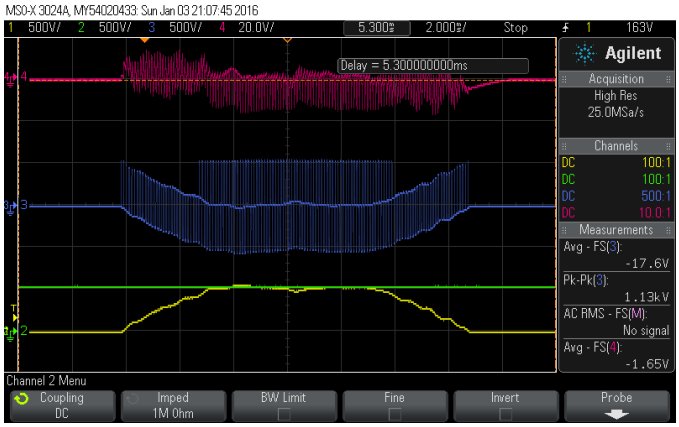


Figure 6-31 Phase A Voltage(yellow), DC link Voltage(green), Phase A Inductor Voltage Waveform(blue) and Inductor Current(magenta) obtained by Test Results

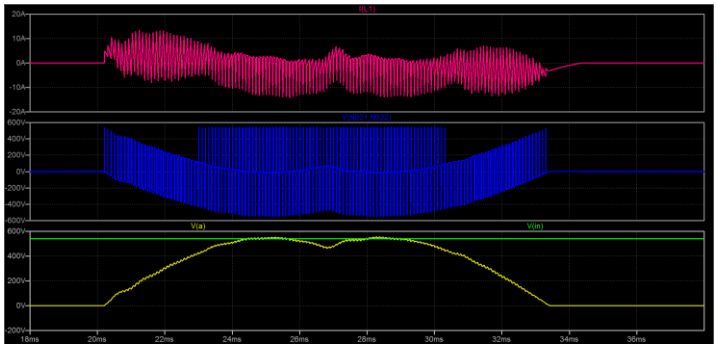


Figure 6-32 Phase A Voltage(yellow), DC link Voltage(green), Phase A Inductor Voltage Waveform(blue) and Inductor Current(magenta) obtained by Simulation Results

6.1.2.6. No Load Test and Simulation Results Comparison at 540V DC link Voltage

Current and voltage waveform shapes are similar in test and simulation results and show that simulation is reliable for generating current and voltage waveforms. In this section, THD of output voltage waveform and RMS value of line to line voltage are also presented for different frequencies.

In Table 6-1, THD of output voltage waveform and RMS value of line to line voltage are shown for different frequencies in tests results and simulation results. THD

values are higher in test results; the reason is described in section 6.1.2.2. Oscillation in inductor current also causes oscillation at the output voltage which results in higher distortion at the output voltage. Simulation is affected less with this phenomenon.

Table 6-1 Comparison of No-Load Tests at 540V DC link Voltage

	THD of line to line voltage V_{ab}		RMS values of line to line voltage V_{ab} (V)	
	Test Results	Simulation Results	Test Results	Simulation Results
75 Hz	4,17%	2,34%	379,7	383,8
50 Hz	3,87%	1,53%	379,8	384,1
30 Hz	4,21%	2,43%	219,5	228,2
10 Hz	4,52%	3,49%	72,3	74,3

RMS values of line to line voltage are slightly higher in simulation results. However this is not an important criterion since output voltage is not sensed and can be increased or decreased by trimming transfer function.

6.1.3. 400V DC link Voltage Operation

A three phase bridge rectifier fed from variac is used to obtain the desired DC link voltage. First DC link capacitors are charged by charging resistor. After capacitors are charged, charging resistor is bypassed by a switch manually. To shorten test time, waveforms are only obtained for 50Hz operation. For operation of other frequencies

THD value of output voltage and RMS value of output voltage is given. To make comparison both test results and simulation results are shown consecutively. These tests are conducted to show boosting capability of topology.

All voltage measurements are done relative to negative terminal of DC-link unless it is specified. From Figure 6-33 to Figure 6-62, odd numbered figures show test results and even numbered figures show simulation results.

6.1.3.1. No Load Three Phase Output Voltages at 50Hz

Output voltage waveforms of converters are shown in Figure 6-33 and Figure 6-34.These waveforms show how three phase voltage waveform is obtained by three converters. In figures, yellow colored waveform is phase A output voltage, green colored waveform is phase B output voltage and blue colored waveform is phase C output voltage. Pink colored waveform is line to line voltage V_{ab} and orange colored waveform is line to line voltage V_{bc}.

In Figure 6-33 and Figure 6-34, output voltages of converters are in same axis to show phase difference between converters. Each converter makes switching action two third of period and only two converters are switching in the same time

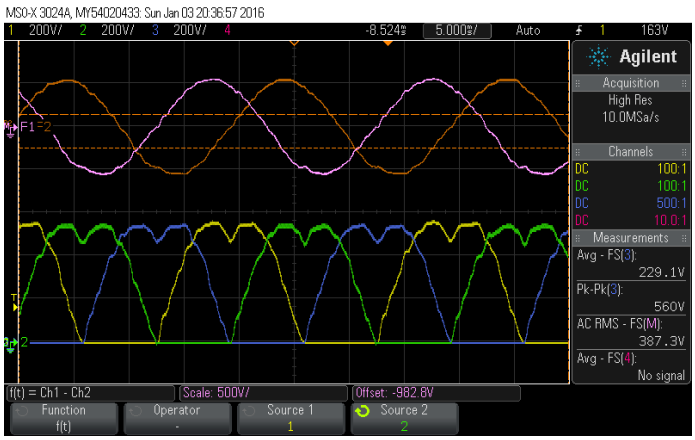


Figure 6-33 Phase Voltages (A:yellow, B:green, C:blue) and Line to Line Voltages (V_{ab}:pink, V_{bc}:orange) obtained by Test Results

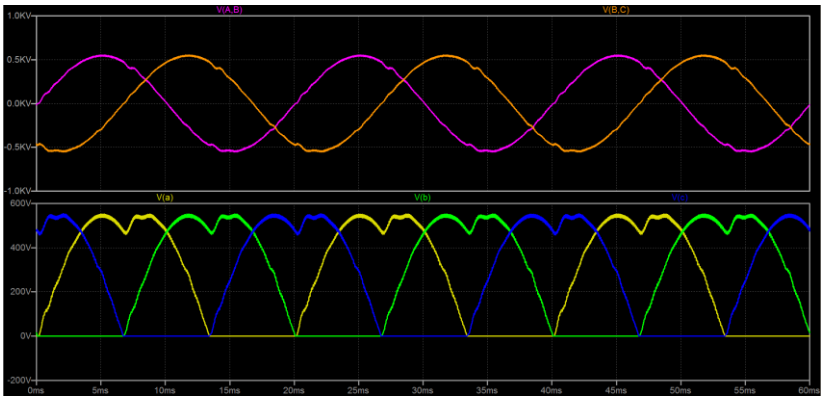


Figure 6-34 Phase Voltages (A:yellow, B:green, C:blue) and Line to Line Voltages (V_{ab}:pink, V_{bc}:orange) obtained by Simulation Results

Some oscillations are observed at output voltages of converters which are also seen on line to line voltages in test results. These oscillations are caused by oscillations in inductor current. Inductor current waveforms are shown in next section. Possible reasons for oscillations in inductor current are described in 6.1.2.2. It is also observed that oscillations are higher when converters are operating at 540V DC link voltage with respect to 400V DC link voltage.

Waveforms are also observed for 10Hz, 30Hz and 75Hz operation. THD and RMS value of output line to line voltage are shown in Table 6-2. Current and voltage waveforms of test results and simulation results are similar in terms of shape and magnitude.

6.1.3.2. Inductor Current Waveforms

Inductor current waveforms are observed to show current ripple in buck mode and buck boost mode. When mode transition occurs, shape of inductor current changes. Change of the shape will be shown in the figures. Inductor current ripple values will be discussed in section 6.2 with steady state load tests.

Since converters are identical, only phase “a” inductor current is shown. From Figure 6-35 to Figure 6-42, phase A output voltage with yellow color, DC link voltage with

blue color and phase A inductor current with magenta color are shown. Figure 6-35 and Figure 6-36 show voltage and current waveforms for one cycle. Remaining figures are obtained by zooming in these waveforms. Oscillation in inductor current is higher in test results with respect to simulation; the reason is explained in section 6.1.2.2. Inductor current ripple values will be discussed in section 6.2 with steady state load tests.

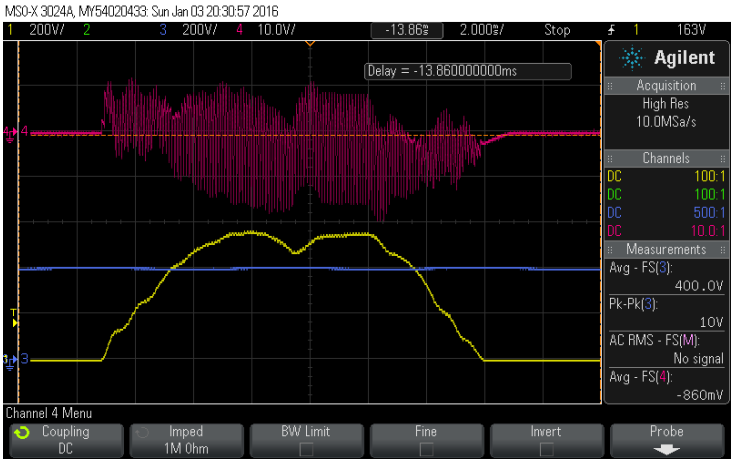


Figure 6-35 Phase A Voltage(yellow), DC link Voltage(blue) and Phase A Inductor Current(magenta) obtained by Test Results

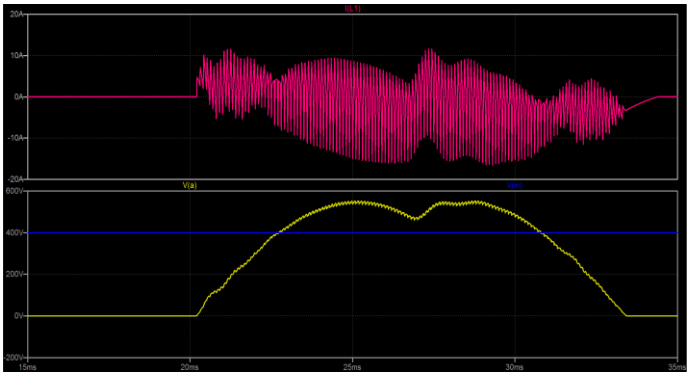


Figure 6-36 Phase A Voltage(yellow), DC link Voltage(blue) and Phase A Inductor Current(magenta) obtained by Simulation Results

Beginning of switching for phase “a” converter is shown in Figure 6-37 and Figure 6-38. In these figures converter is operating in buck mode since output voltage is less

than 80% of DC link voltage. Inductor current shape is similar to buck converter in continuous conduction mode.

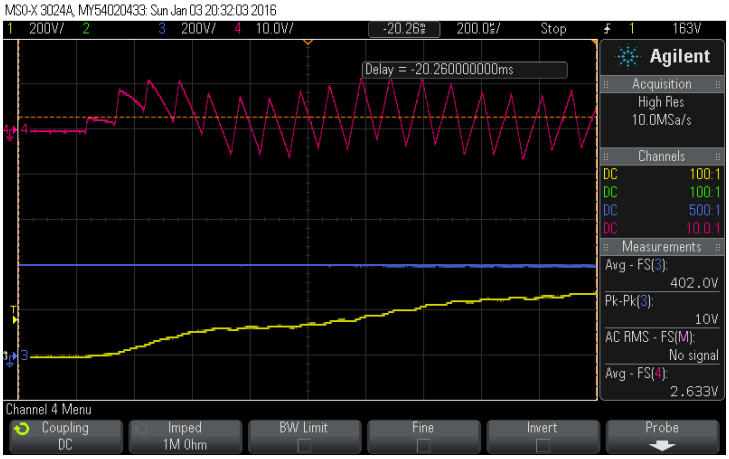


Figure 6-37 Phase A Voltage(yellow), DC link Voltage(blue) and Phase A Inductor Current(magenta) obtained by Test Results

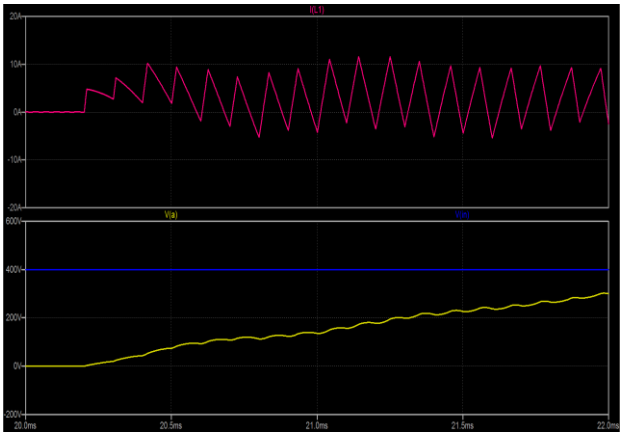


Figure 6-38 Phase A Voltage(yellow), DC link Voltage(blue) and Phase A Inductor Current(magenta) obtained by Simulation Results

When output voltage is higher than 80% of DC link voltage which is 320V when DClink is 400V, converters operate at buck-boost mode. Inductor current changes its shape form triangular to trapezoidal. Change of shape of inductor current when mode transition occurs, are shown in Figure 6-39 and Figure 6-40.

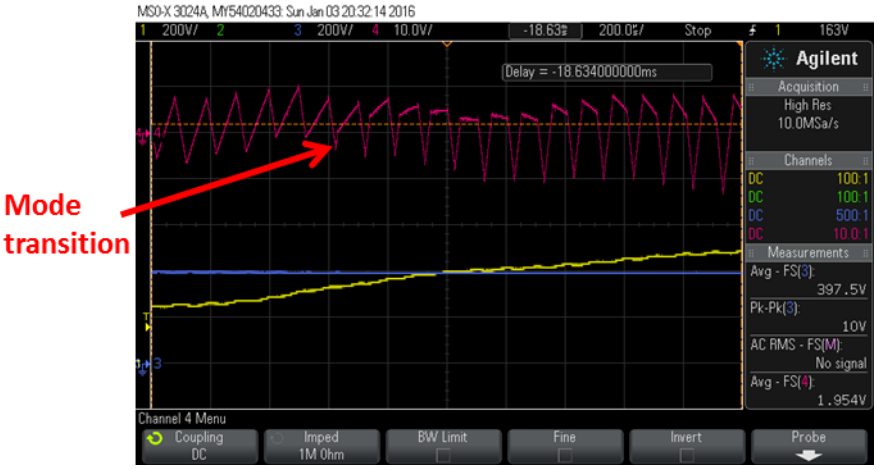


Figure 6-39 Phase A Voltage(yellow), DC link Voltage(blue) and Phase A Inductor Current(magenta) obtained by Test Results

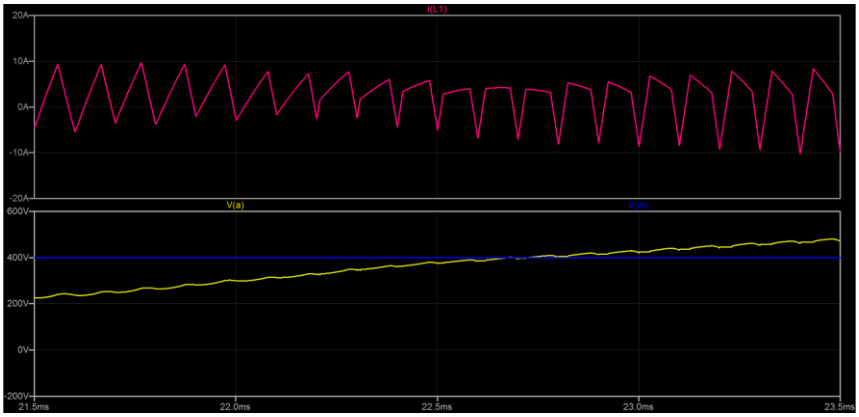


Figure 6-40 Phase A Voltage(yellow), DC link Voltage(blue) and Phase A Inductor Current(magenta) obtained by Simulation Results

When output voltage decreases to level lower than 80% of DC link voltage, converter starts to operate at buck mode again. Inductor current shape is similar to inductor current at buck converter. Mode transitions are shown in Figure 6-41 and Figure 6-42.

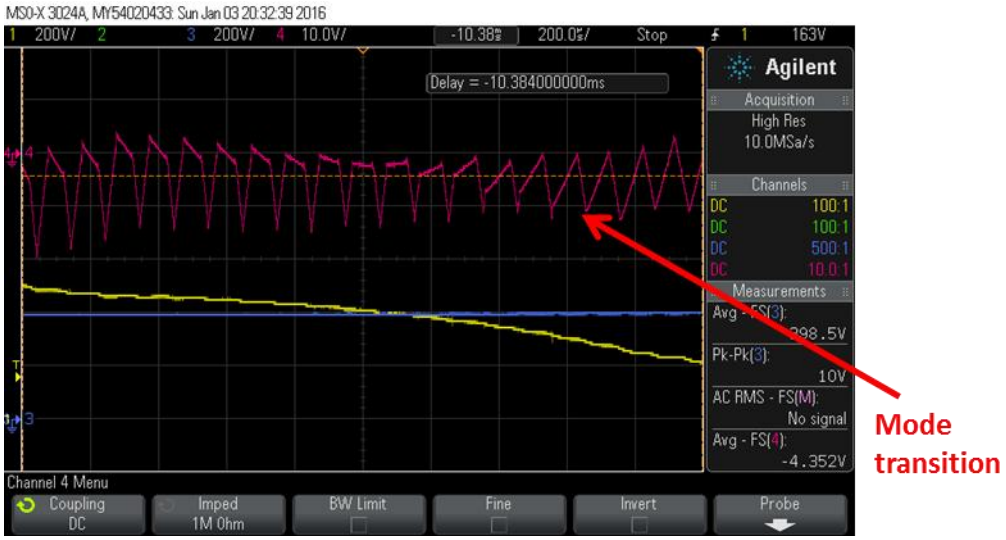


Figure 6-41 Phase A Voltage(yellow), DC link Voltage(blue) and Phase A Inductor Current(magenta) obtained by Test Results

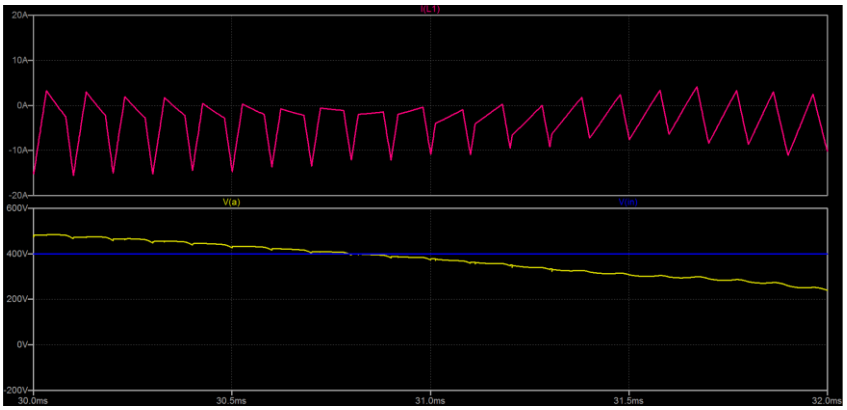


Figure 6-42 Phase A Voltage(yellow), DC link Voltage(blue) and Phase A Inductor Current(magenta) obtained by Simulation Results

6.1.3.3. Voltage Waveforms of S1 and S2 Switches

Circuit diagram of the converter is shown in Figure 5-5. Voltage across collector and emitter of S2 are shown in figures from Figure 6-43 to Figure 6-52 with blue colored waveform. Voltage over collector and emitter of S1 is not shown but it can be obtained by subtracting blue colored waveform from DC link voltage. In these figures DC link voltage is shown with green color, output voltage is shown with

yellow color and inductor current is shown with magenta color. As described in previous section, S1 and S2 are switching for 2/3 of a period. Figure 6-43 and Figure 6-44 show waveforms for one period. These waveforms are presented to show switch voltage rating are appropriate and variation of “duty1” as described in section 5.2. DC link voltage and output voltage waveforms are shown to emphasis when mode transition occurs. Inductor current waveform is shown to observe current waveform in different states of S1 and S2. Maximum voltage over S1 and S2 is equal to DC link voltage. In these tests, maximum voltage seen on S1 and S2 is equal to 400V which is lower than switch ratings.

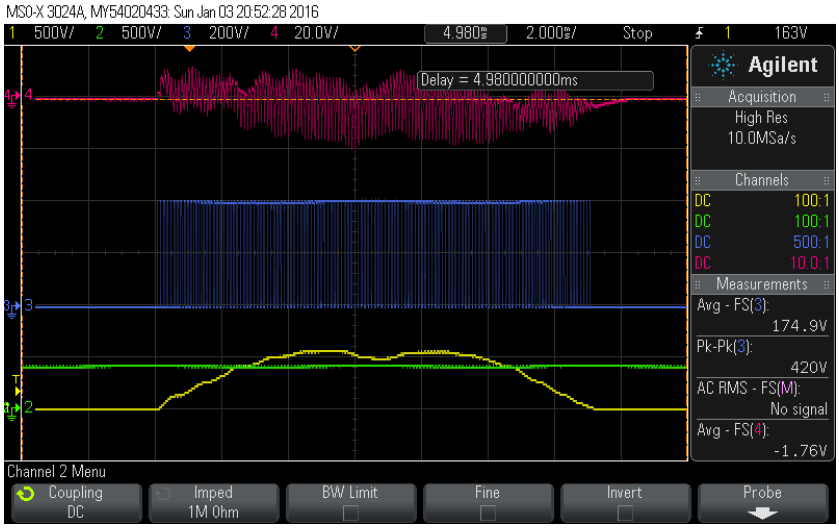


Figure 6-43 Phase A Voltage(yellow), DC link Voltage(green), Voltage Waveform across S2(blue) and Phase A Inductor Current(magenta) obtained by Test Results

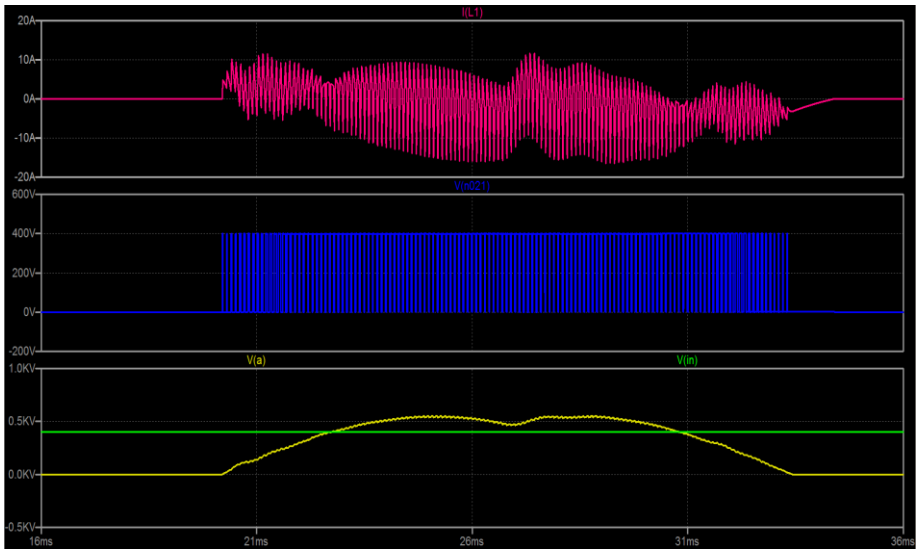


Figure 6-44 Phase A Voltage(yellow), DC link Voltage(green), Voltage Waveform across S2(blue) and Phase A Inductor Current(magenta) obtained by Simulation Results

The designed converter starts operating in buck mode, duty cycle "duty1" increases to obtain higher voltage level at the output. Figure 6-45 and Figure 6-46 show starting point of switching.

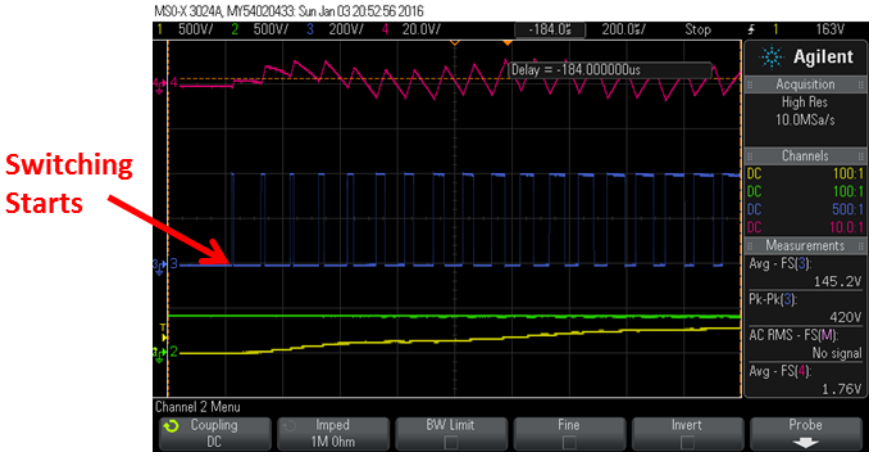


Figure 6-45 Phase A Voltage(yellow), DC link Voltage(green), Voltage Waveform across S2(blue) and Phase A Inductor Current(magenta) obtained by Test Results

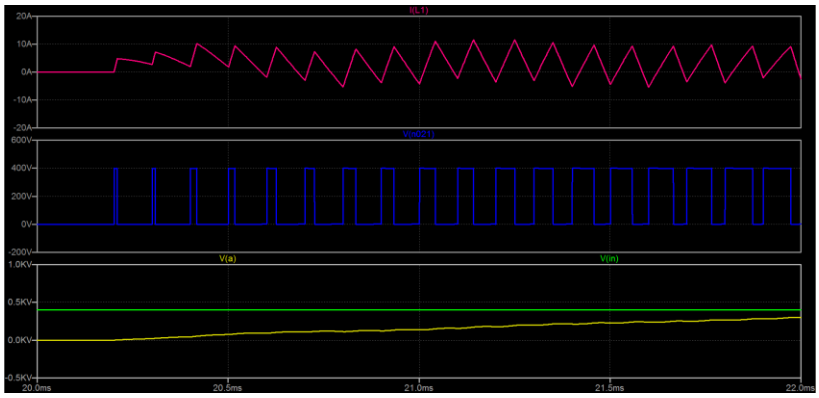


Figure 6-46 Phase A Voltage(yellow), DC link Voltage(green), Voltage Waveform across S2(blue) and Phase A Inductor Current(magenta) obtained by Simulation Results

In buck-boost mode, duty cycle “duty1” for switches S1 and S2 is constant and 80%. Obtaining desired voltage level is done by output switches S3 and S4. Constant duty cycle operation for “duty1” is shown in Figure 6-47 and Figure 6-48.

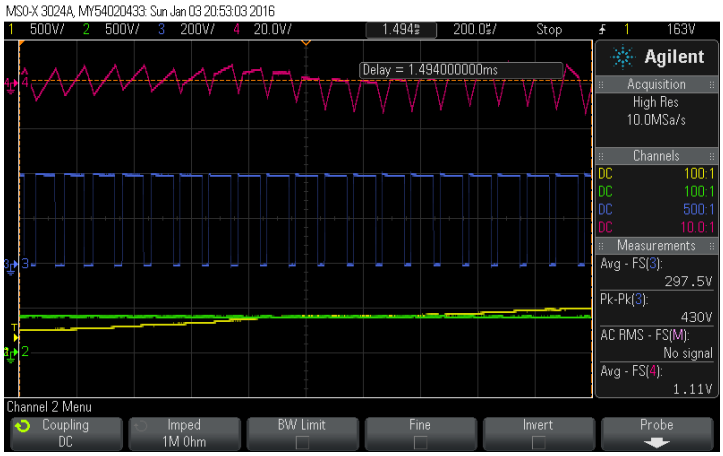


Figure 6-47 Phase A Voltage(yellow), DC link Voltage(green), Voltage Waveform across S2(blue) and Phase A Inductor Current(magenta) obtained by Test Results

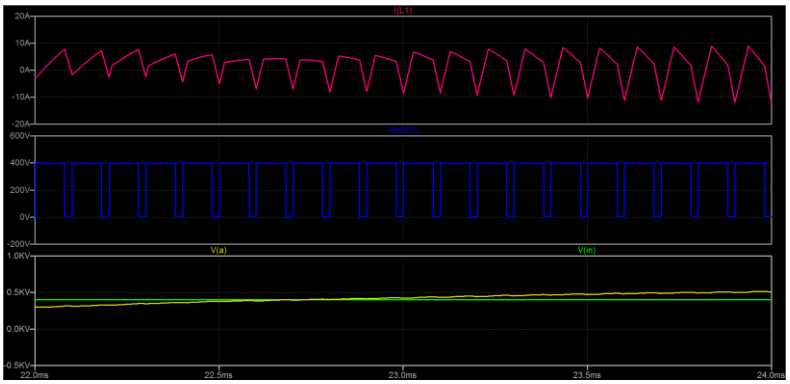


Figure 6-48 Phase A Voltage(yellow), DC link Voltage(green), Voltage Waveform across S2(blue) and Phase A Inductor Current(magenta) obtained by Simulation Results

When output voltage decreases below 80% of DC link voltage, converter starts operating at buck mode again, duty cycle “duty1” for switches S1 and S2 starts decreasing. Mode transition is shown in Figure 6-49 and Figure 6-50.

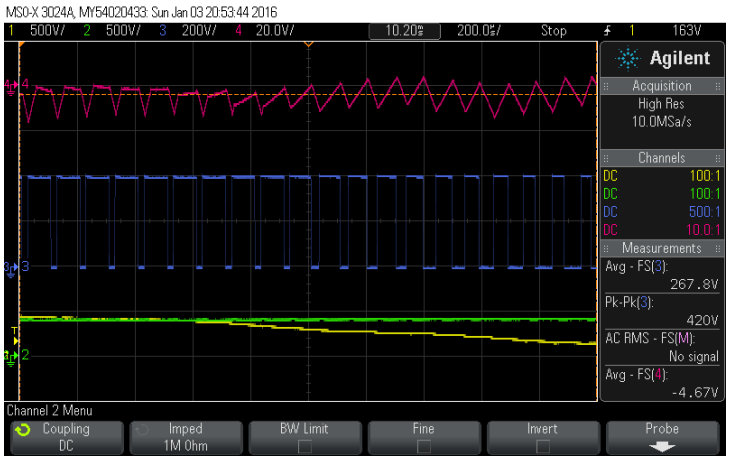


Figure 6-49 Phase A Voltage(yellow), DC link Voltage(green), Voltage Waveform across S2(blue) and Phase A Inductor Current(magenta) obtained by Test Results

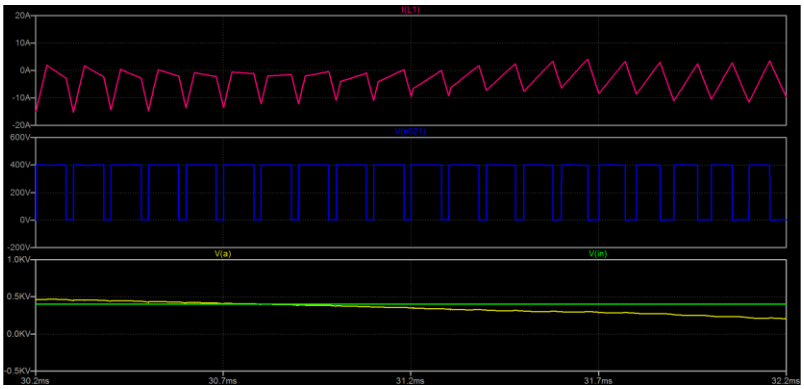


Figure 6-50 Phase A Voltage(yellow), DC link Voltage(green), Voltage Waveform across S2(blue) and Phase A Inductor Current(magenta) obtained by Simulation Results

Duty cycle for switches S1 and S2 decreases to 0 and switching stops. These waveforms are shown in Figure 6-51 and Figure 6-52.

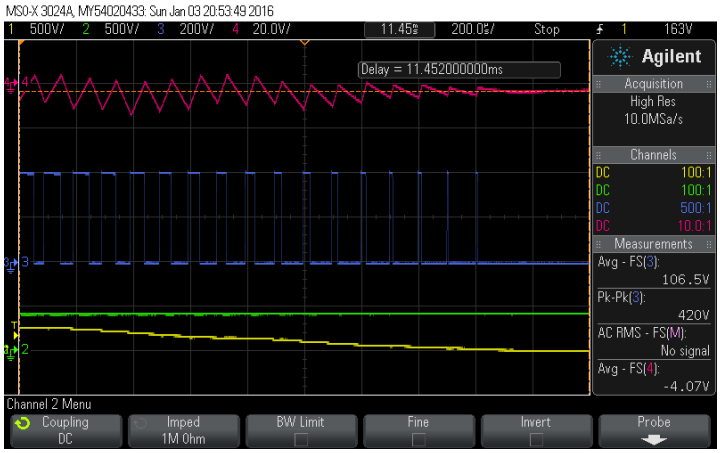


Figure 6-51 Phase A Voltage(yellow), DC link Voltage(green), Voltage Waveform across S2(blue) and Phase A Inductor Current(magenta) obtained by Test Results

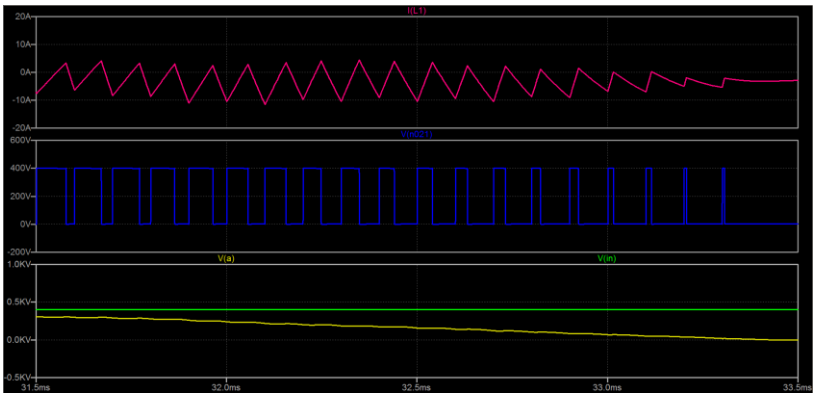


Figure 6-52 Phase A Voltage(yellow), DC link Voltage(green), Voltage Waveform across S2(blue) and Phase A Inductor Current(magenta) obtained by Simulation Results

6.1.3.4. Voltage Waveforms of S3 and S4 Switches

Circuit diagram of the converter is shown in Figure 5-5. . Voltage across collector and emitter of S4 are shown in figures from Figure 6-53 to Figure 6-60 with blue colored waveform. Voltage over collector and emitter of S3 is not shown but it can be obtained by subtracting blue colored waveform from output voltage. In these figures output voltage is shown with yellow color and inductor current is shown with magenta color. As described in previous section, S3 and S4 are switching in buck-boost mode. Figure 6-53 and Figure 6-54 show waveforms for one period. These waveforms are presented to show switch voltage rating are appropriate and variation of “duty2” as described in section 5.2. In these tests, maximum voltage seen on S3 and S4 is equal to 540V which is same with the results obtained by operation with 540V DClink voltage. This is expected since voltage seen over switches S3 and S4 is equal to maximum output voltage and does not depend on DC link voltage. DC link voltage and output voltage waveforms are shown to emphasis when mode transition occurs. Inductor current waveform is shown to observe current waveform in different states of S3 and S4.

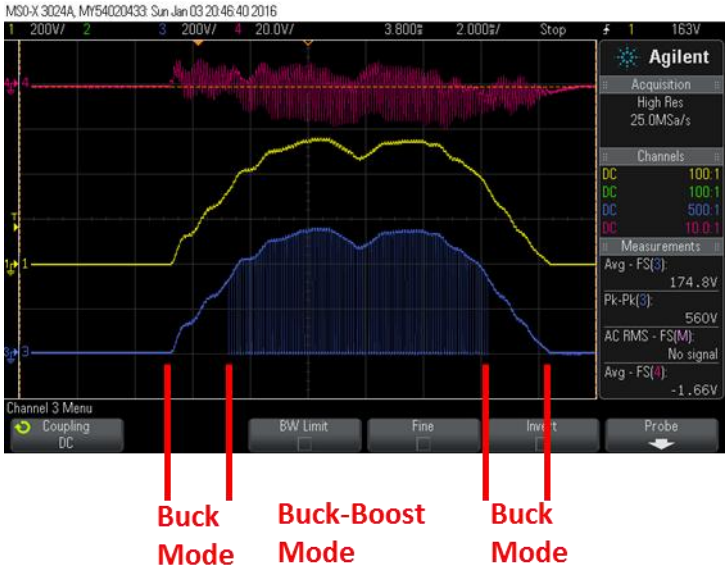


Figure 6-53 Phase A Voltage(yellow), Voltage Waveform across S4(blue) and Phase A Inductor Current(magenta) obtained by Test Simulation Results

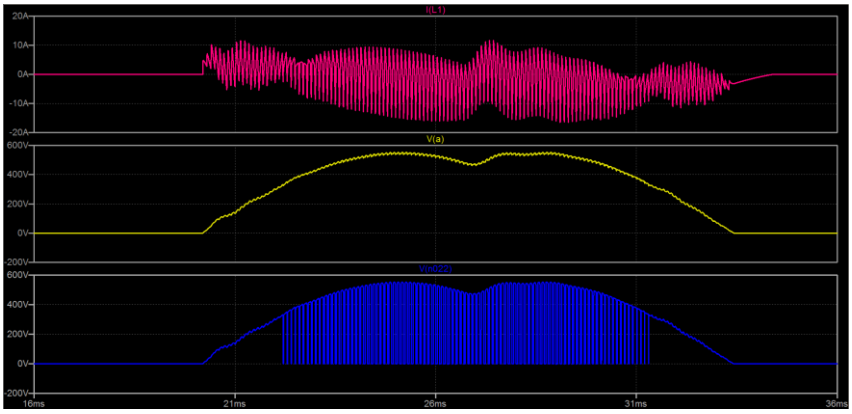


Figure 6-54 Phase A Voltage(yellow), Voltage Waveform across S4(blue) and Phase A Inductor Current(magenta) obtained by Simulation Results

While converter operates in buck mode, S3 is on S4 is off. When output voltage is higher than 80% of DC link voltage, S3 and S4 star switching. Figure 6-55 and Figure 6-56 show starting point of switching.

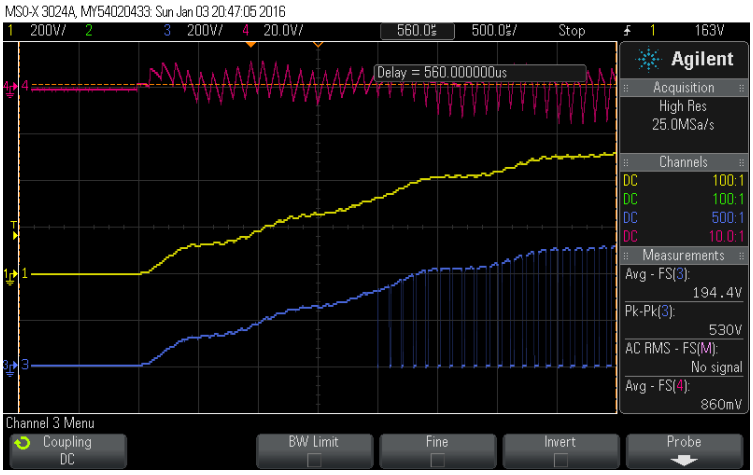


Figure 6-55 Phase A Voltage(yellow), Voltage Waveform across S4(blue) and Phase A Inductor Current(magenta) obtained by Test Results

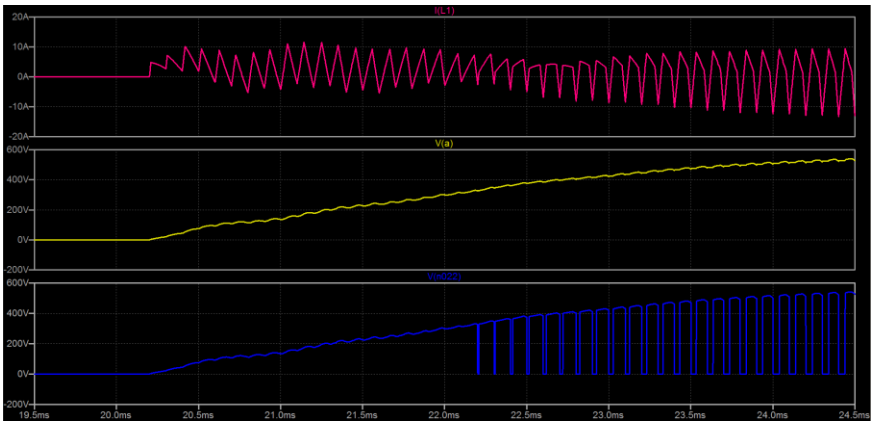


Figure 6-56 Phase A Voltage(yellow), Voltage Waveform across S4(blue) and Phase A Inductor Current(magenta) obtained by Simulation Results

To obtain higher output voltage, on time off S4 must be increased. In Figure 6-57 and Figure 6-58 on time of S4 is higher for higher output voltages. When S4 is conducting, inductor current increases with applied DC link voltage to its terminals.

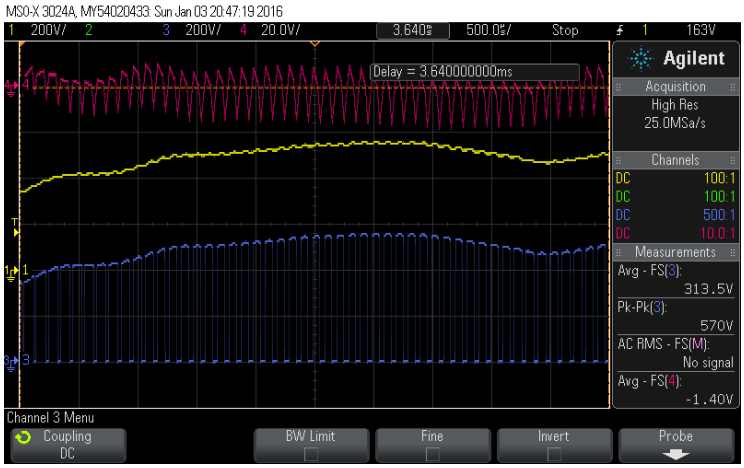


Figure 6-57 Phase A Voltage(yellow), Voltage Waveform across S4(blue) and Phase A Inductor Current(magenta) obtained by Test Results

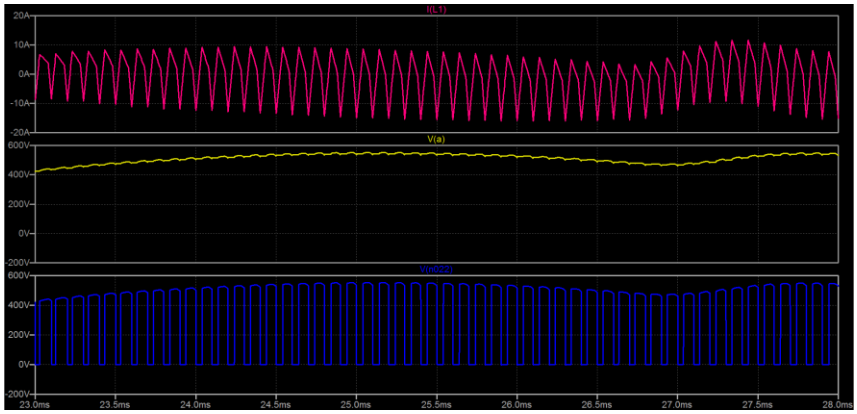


Figure 6-58 Phase A Voltage(yellow), Voltage Waveform across S4(blue) and Phase A Inductor Current(magenta) obtained by Simulation Results

When output voltage decreases below 80% of DC link voltage, converter starts operating at buck mode again, S3 is conducting and S4 is off. Mode transition is shown in Figure 6-59 and Figure 6-60.

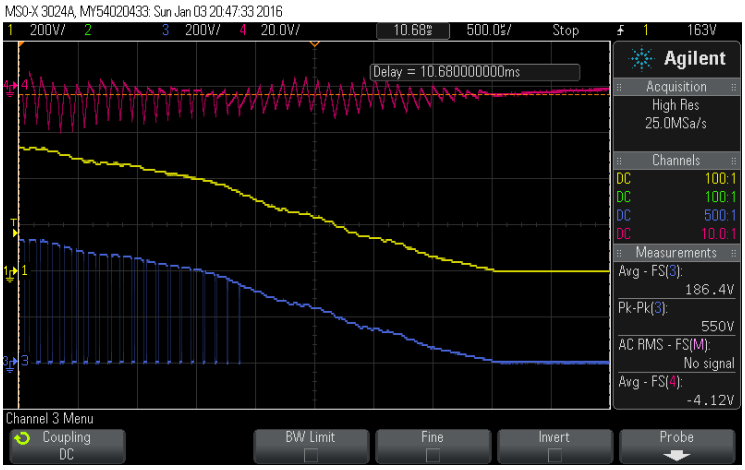


Figure 6-59 Phase A Voltage(yellow), Voltage Waveform across S4(blue) and Phase A Inductor Current(magenta) obtained by Test Results

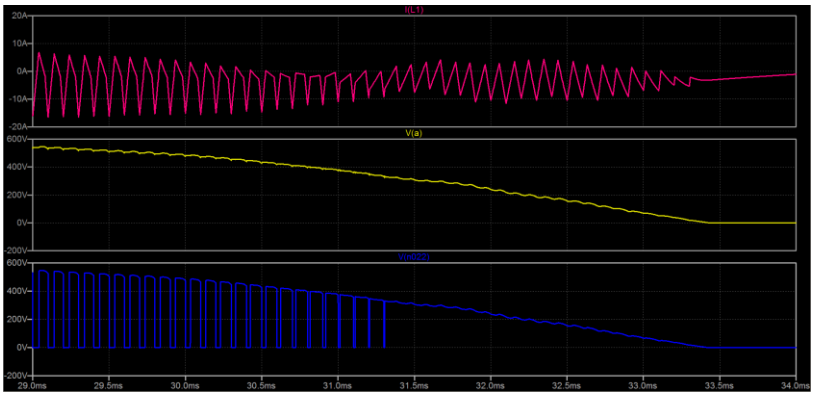


Figure 6-60 Phase A Voltage(yellow), Voltage Waveform across S4(blue) and Phase A Inductor Current(magenta) obtained by Simulation Results

6.1.3.5. Inductor Voltage Waveforms

Voltage over inductor is shown in Figure 6-61 and Figure 6-62 with blue color. In these figures output voltage is shown with yellow color, DC link voltage is shown with green color and inductor current is shown with magenta color. Voltage over inductor is the difference of voltage at midpoint of switches S1, S2 and voltage at midpoint of switches S3 and S4. These waveforms are shown to give insight about maximum voltage rating of inductor. The value is the equal to maximum of DC link

voltage and output voltage. In these tests, it is equal to maximum output voltage and 540V.

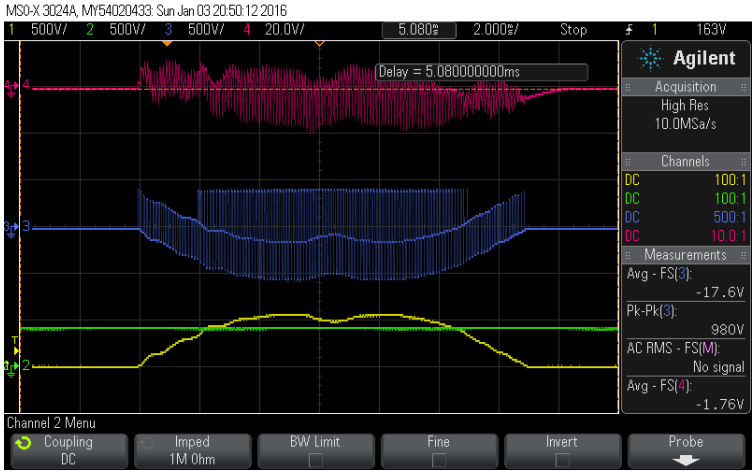


Figure 6-61 Phase A Voltage(yellow), DC link Voltage(green), Phase A Inductor Voltage Waveform(blue) and Inductor Current(magenta) obtained by Test Results

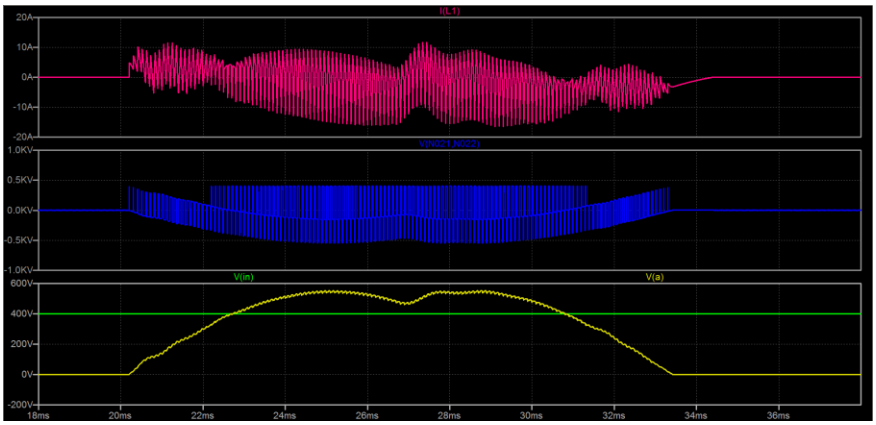


Figure 6-62 Phase A Voltage(yellow), DC link Voltage(green), Phase A Inductor Voltage Waveform(blue) and Inductor Current(magenta) obtained by Simulation Results

6.1.3.6. No Load Test and Simulation Results Comparison

Current and voltage waveform shapes are similar in test and simulation results and show that simulation is reliable for generating current and voltage waveforms. In this

section, THD of output voltage waveform and RMS value of line to line voltage are also presented for different frequencies.

In Table 6-2, THD of output voltage waveform and RMS value of line to line voltage are shown for different frequencies in tests results and simulation results. THD values are higher in test results; the reason is described in section 6.1.2.2. Oscillation in inductor current also causes oscillation at the output voltage which results in higher distortion at the output voltage. Simulation is affected less with this phenomenon.

Table 6-2 Comparison of No-Load Tests at 400V DC link Voltage

	THD of line to line voltage Vab		RMS values of line to line voltage Vab (V)	
	Test Results	Simulation Results	Test Results	Simulation Results
75 Hz	3,97%	2,34%	379,8	381,7
50 Hz	3,34%	1,75%	379,8	382,2
30 Hz	4,06%	2,02%	218,6	228,1
10 Hz	4,63%	3,72%	71,7	75,1

RMS values of line to line voltage are slightly higher in simulation results. However this is not an important criterion since output voltage is not sensed and can be increased or decreased by trimming transfer function.

6.1.4. Summary of No Load Tests

Waveforms obtained by simulation and tests are very similar with respect to shape and magnitude. Obtaining three phase sine waves by three converters is explained first. Voltage and current waveforms are shown for different operating modes. Oscillations are observed in test results and solution is proposed to solve this problem. Boosting capability is verified by 400V DC link voltage tests.

6.2. Steady State Tests

By doing steady state tests, measuring THD and efficiency is aimed. These tests are conducted at 4 different output frequencies which are 10Hz, 30Hz, 50Hz and 75Hz. The tests are repeated for 540V and 400V DC link voltage. V/f is applied at the output. From 10Hz to 50Hz output voltage varies linearly but from 50Hz to 75Hz output voltage is constant and equal to the voltage at 50Hz. Loads are described at Table 6-3. Units are "Watt(W)" for resistive loads and "Volt-Ampere(VA)" for inductive loads. For each output frequency four resistive and four inductive tests are done. Resistive test results are also compared with simulation results to verify reliability of simulation.

Table 6-3 Test Load Power at Different Frequencies

Frequency (Hz)	25% Load (W or VA)	50% Load (W or VA)	75% Load (W or VA)	100% Load (W or VA)
75	625	1250	1875	2500
50	625	1250	1875	2500
30	375	750	1125	1500
10	125	250	375	500

In sections 6.2.2 and 6.2.3, efficiencies are calculated by subtracting rectifier loss thus give the efficiency of inverter only. To calculate rectifier losses, DC link is loaded by resistor drawing different amount of power. Three phase input power measured is measured by three phase wattmeter. Output power of DC link is calculated by multiplying mean output voltage with mean output current. Rectifier loss when DC link voltage is 540V is shown in Table 6-4. Rectifier loss when DC link voltage is 400V, are shown in Table 6-5. According to power drawn from 3 phase AC source, rectifier loss is estimated and subtracted from input power to calculate inverter efficiency.

Table 6-4 Rectifier Losses When DC link Voltage is set to 540V

DC link Voltage (V)	Three Phase Input Power (W)	Power Drawn from DC link (W)	Rectifier Loss (W)
537,2	2540	2433,51	106,48
538,7	2040	1971,64	68,35
542,2	1675	1610,33	64,66
542,2	1325	1268,74	56,25
538,7	1120	1072,01	47,98
542,0	790	753,38	36,62
537,2	655	617,78	37,22
539,2	530	501,45	28,54
541,2	400	378,84	21,16
540,2	260	244,37	15,63
540,2	133	122,68	10,32

Table 6-5 Rectifier Losses When DC link Voltage is set to 400V

DC link Voltage (V)	Three Phase Input Power (W)	Power Drawn from DC link (W)	Rectifier Loss (W)
399,0	2770	2653,35	116,65
400,0	2080	1992,00	88,00
397,5	1690	1621,80	68,20
402,5	1420	1364,47	55,52
402,5	1140	1098,82	41,17
400,0	800	768,00	32,00
401,5	650	626,34	23,66
399,5	520	503,37	16,63
401,5	385	373,39	11,60
399,0	265	255,36	9,64
400,0	135	128,47	6,53

6.2.1. Test Equipment

VARSAN VARIAC: This equipment is used to supply power stage. Input voltage level is set by this equipment.

INSTEK GPS-3303: This equipment is used to supply control circuit. Two channels are used. 8V is used to supply control circuit and 24V is used to supply isolated converters which are used for gate drive circuit.

HIOKI 3184 DIGITAL POWER HI TESTER: This equipment is used to measure input power.

HIOKI 3194 MOTOR/HARMONIC HI TESTER: This equipment is used to measure output power and THD.

6.2.2. Resistive Test Results

Resistive tests are done to observe efficiency of inverter and THD of output voltage at different conditions. Inductor current ripple values at resistive load are explained. Also comparison between classical method is done by simulation results.

Steady state resistive test results for 400V DC link voltage are shown in Table 6-6 and for 540V DC link voltage are shown in Table 6-7. In the tables for different frequencies and loads, DC link voltage, input power, output power, efficiency, voltage distortion, current distortion and voltage magnitude at fundamental frequency are shown.

Table 6-6 Resistive Test Results at 400V DC link Voltage

Frequency (Hz)	V_{in}(V)	P_{in}(W)	P_{out}(W)	n(%)	V_{THD}(%)	I_{THD}(%)	V_{outf}(Vrms)
75	403	2623	2474,7	94,3	2,68	3,11	369,52
75	401	1992	1869,6	93,9	4,12	3,33	373,59
75	401	1389	1249,1	89,9	3,97	3,86	377,28
75	400	756	624,18	82,6	4,06	4,1	381,33
50	399,1	2623	2455,9	93,6	2,68	2,66	369,62
50	402,6	2102	1961,4	93,3	2,83	2,71	372,93
50	401,5	1329	1185,1	89,2	3,08	2,78	375
50	398,4	756	634,4	83,9	3,18	3,07	379,3
30	398	1502	1440,4	95,9	2,56	2,34	211,41
30	400	1145	1101,5	95,6	2,83	1,96	215,34
30	401,5	788	748,71	95,0	2,99	2,27	217,32
30	402	399	373,28	93,6	3,47	2,94	218,82
10	399,4	624	542,04	86,9	9,45	8,97	58,937
10	402,5	409	367,38	89,8	5,38	4,77	66,17
10	401,9	280	250,2	89,4	4,29	3,61	68,5
10	397,5	161	140,02	87,0	3,68	2,77	76,41

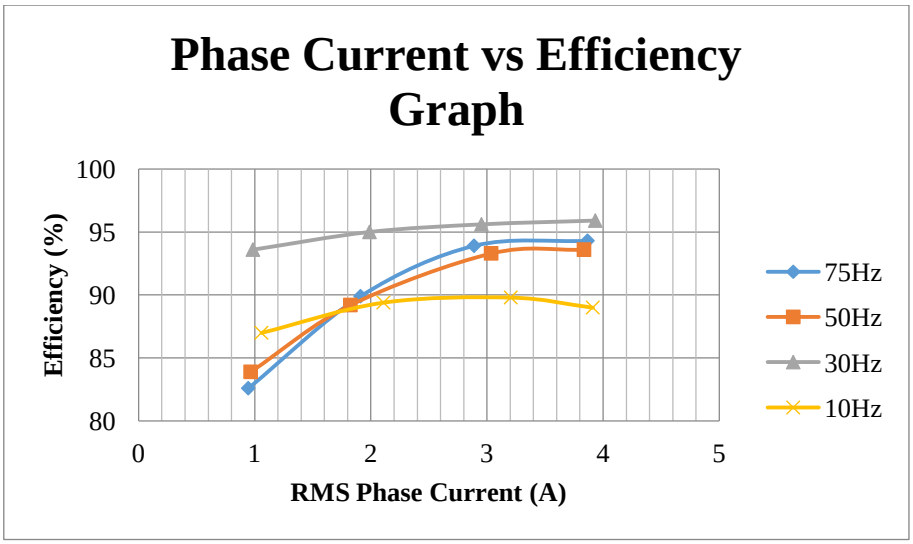


Figure 6-63 Phase Current vs Efficiency Graph at 400V DC link

In Figure 6-63, efficiency of inverter is drawn with respect to phase current at different frequencies. At rated current efficiencies are lower for 10Hz this is because output power is lower. Switching losses decrease slightly while output power is one fifth of rated power at 50Hz. Thus efficiency becomes less at 10Hz. Efficiencies of 75Hz and 50Hz are similar since their output voltage magnitude is same. Efficiencies at 30Hz are better. This is because switching losses decrease since output voltage magnitude is decreased to three fifth of rated voltage.

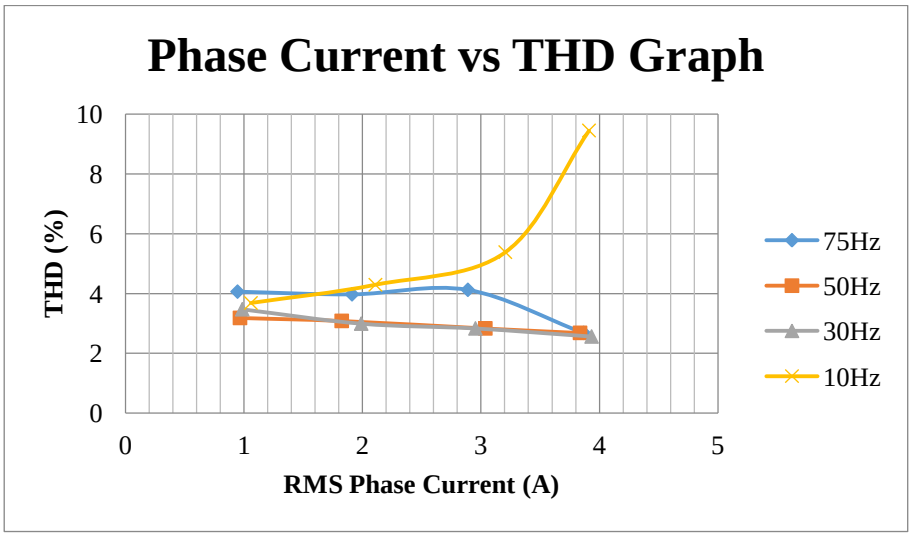


Figure 6-64 Phase Current vs THD Graph at 400V DC link

In Figure 6-64, THD of output voltage is drawn with respect to phase current at different frequencies. THD values are worse at 10 Hz and 75 Hz; this is because system is optimized for 50 Hz operation. At 10 Hz, time step is large and output takes shape of stepped voltage waveform. At 75 Hz, voltage slope is higher, thus it is harder to follow reference signal.

Table 6-7 Resistive Test Results at 540V DC link Voltage

Frequency(Hz)	V_{in}(V)	P_{in}(W)	P_{out}(W)	n(%)	V_{THD}(%)	I_{THD}(%)	V_{outf}(Vrms)
75	538,7	2630	2511,5	95,5	3,3	3,39	372,08
75	535,2	2012	1888,5	93,9	3,88	3,71	375,04
75	537,2	1354	1259,5	93,0	4,31	3,74	378,13
75	539,2	733	624,83	85,2	4,26	4,14	379
50	538,7	2690	2560,8	95,2	3,17	3,25	372,78
50	537,2	2112	1991,8	94,3	3,38	3,34	375,04
50	542,7	1294	1190,1	92,0	3,57	3,18	375,96
50	540,6	743	637,58	85,8	3,79	3,41	379
30	519	1585	1491,7	94,1	3,44	2,45	215,12
30	527,1	1193	1109,1	93,0	3,73	2,64	215,11
30	538,1	823	746,76	90,7	3,18	2,63	217,61
30	541,2	449	374,46	83,4	3,91	3,13	218,83
10	535,7	572	502,28	87,8	12,89	11,6	56,553
10	537,7	399	361,29	90,5	7,14	6,35	65,69
10	535,6	280	245,59	87,7	6	5,22	68,2
10	530	171	140,79	82,3	4,77	3,85	76,67

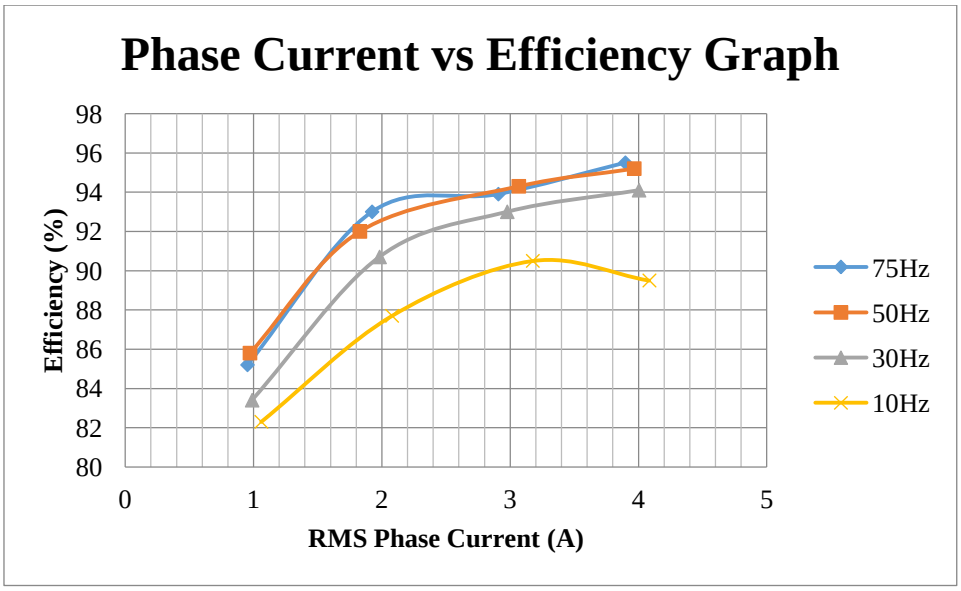


Figure 6-65 Phase Current vs Efficiency Graph at 540V DC link

In Figure 6-65, efficiency of inverter is drawn with respect to phase current at different frequencies. At rated current efficiencies are lower for 10Hz this is because output power is lower. Switching losses decrease slightly while output power is one fifth of rated power at 50Hz. Thus efficiency becomes less at 10Hz. Efficiencies of 75Hz and 50Hz are similar since their output voltage magnitude is same. Efficiencies at 30Hz are also worse than efficiencies of 50Hz and 75Hz. When DC link voltage was 400V, efficiency results for 30Hz were better. This result could not be achieved when DC link voltage is 540V. This is because switching losses of S1 and S2 is higher when DC link voltage is 540V. Since output power is less at 30Hz with respect output power at 50Hz, measured efficiencies at 30Hz became less.

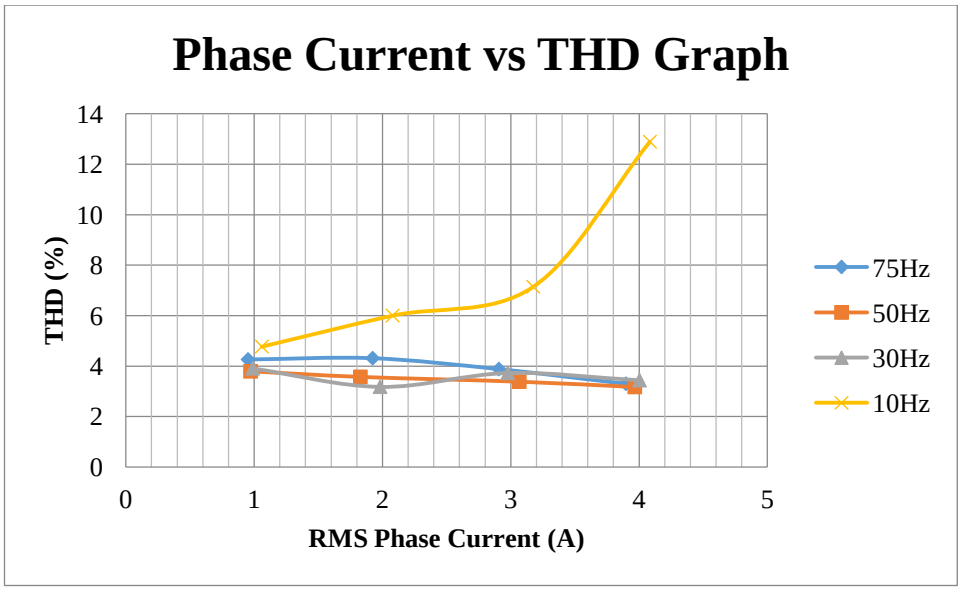


Figure 6-66 Phase Current vs THD Graph at 400V DC link

In Figure 6-66, THD of output voltage is drawn with respect to phase current at different frequencies. THD values at 30Hz, 50Hz and 75Hz are similar. THD values are worse at 10 Hz; this is because system is optimized for 50 Hz operation. At 10 Hz, time step is large and output takes shape of stepped voltage waveform.

6.2.2.1. Comparison of Simulation and Test Results

All resistive load tests are also simulated to verify reliability of simulation. Table 6-8 and Table 6-9 are formed to make comparison between test results and simulation results. Efficiencies of test results are higher in test results.

Table 6-8 Test Results and Simulation Results Efficiency Comparison for 400V DC link Voltage

		Test Results	Simulation Results	Difference
Frequency(Hz)	P_{out}(W)	n(%)	n(%)	%
75	2500	94,3	93,8	0,5
75	1875	93,9	93,1	0,8
75	1250	89,9	89,2	0,7
75	625	82,6	81,7	0,9
50	2500	93,6	92,9	0,7
50	1875	93,3	92,6	0,7
50	1250	89,2	88,1	1,1
50	625	83,9	81,8	2,1
30	1500	95,9	95,2	0,7
30	1175	95,6	94,9	0,7
30	750	95,0	94,1	0,9
30	375	93,6	92,8	0,8
10	500	86,9	85,3	1,6
10	375	89,8	88,6	1,2
10	250	89,4	87,9	1,5
10	125	87,0	85,8	1,2

Table 6-9 Test Results and Simulation Results Efficiency Comparison for 540V DC link Voltage

		Test Results	Simulation Results	Difference
Frequency(Hz)	P_{out}(W)	n(%)	n(%)	%
75	2500	95,5	94,8	0,7
75	1875	93,9	93,5	0,4
75	1250	93,0	92,6	0,4
75	625	85,2	83,8	1,4
50	2500	95,2	94,6	0,6
50	1875	94,3	93,7	0,6
50	1250	92,0	91,5	0,5
50	625	85,8	83,5	2,3
30	1500	94,1	93,6	0,5
30	1175	93,0	92,4	0,6
30	750	90,7	89,3	1,4
30	375	83,4	81,9	1,5
10	500	87,8	85,3	2,5
10	375	90,5	89,3	1,2
10	250	87,7	85,2	2,5
10	125	82,3	80,1	2,2

Maximum difference is at calculated efficiencies are 2.1% for 400V DC link voltage and 2.5% for 540V DC link voltage. Although the results are not exact, the relationship between output frequency and output power is same with test results. Simulation can be used to compare two different configurations to evaluate which one is more efficient.

6.2.2.2. Current Ripple and Maximum Inductor Current

In Table 6-10, inductor current ripple and maximum inductor current values are given at different frequencies while inverter is loaded with rated current. Maximum inductor current occurs at 75Hz as it was discussed in Chapter 5. Its value is 19A and it is less than positive current level threshold which was discussed in Chapter 5.

Table 6-10 Current Ripple and Maximum Inductor Current at Different Frequencies

Frequency	Inductor current ripple at 400V DC link voltage (A)	Inductor current ripple at 540V DC link voltage (A)	Maximum inductor current at 400V DC link voltage (A)	Maximum inductor current at 540V DC link voltage (A)
75 Hz	22	16	19	16
50 Hz	22	16	18	12
30 Hz	12	18	13	17
10 Hz	10	12	7	8

It is observed that inductor current ripple is nearly 4 times of maximum load current. Maximum load current is 5.35A which is the peak value of rated current. Ripple can be decreased by two ways. First method is using an inductor with larger inductance value; however this increases cost and size of inductor. Another method is to optimize the voltage threshold where mode transition occurs between buck mode and buck-boost mode. This is an issue which will be investigated in future work.

6.2.2.3. Efficiency Comparison Between Proposed Topology and Classical Method

In Chapter 4, efficiency comparison was done between proposed topology and classical method. Classical method consists of boost converter to increase input voltage, full bridge to produce PWM waveform and LC filter to decrease THD of output voltage. This comparison is repeated for designed circuit at rated power at rated frequency. Efficiencies obtained by test results and simulation results are given

for the designed circuit and efficiencies obtained by simulation results are given for classical method in Table 6-11.

Table 6-11 Efficiency Comparison

DC link Voltage	Efficiency obtained by test results of designed circuit	Efficiency obtained by simulation results of designed circuit	Efficiency obtained by simulation results of classical Method
400V	93,6%	92,9%	92,1%
540V	95,2%	94,6%	93,7%

According to simulation results, proposed method increases efficiency with respect to classical method.

6.2.3. Inductive Test Results

Steady state inductive test results for 400V DC link voltage are shown in Table 6-12 and for 540V DC link voltage are shown in Table 6-13. In the tables for different frequencies and loads, DC link voltage, input power, output power, efficiency, voltage distortion, current distortion and voltage magnitude at fundamental frequency, apparent power and power factor are shown. Inductive load tests are done to show THD values of output voltages. Efficiencies are lower than resistive load tests as expected since output power is less with respect to resistive load.

Table 6-12 Inductive Test Results at 400V DC link Voltage

Frequency (Hz)	V_{in} (V)	P_{in} (W)	P_{out} (W)	N (%)	V_{THD} (%)	I_{THD} (%)	V_{outf} (Vrms)	S_{out} (VA)	P.F
75	402	718	598	83,3	4,98	2,82	380,99	2455,6	0,24
75	402,5	437	320,6	73,4	5,07	3,33	382,76	1891,2	0,17
75	399	591	481,7	81,5	4,7	1,39	382	1252,2	0,38
75	400	513	394,9	77,0	4,29	1,93	382,16	624,8	0,63
50	399	1275	1166,8	91,5	3,45	1,19	376,34	2441	0,48
50	399	989	877,2	88,7	3,19	1,29	377,49	1795	0,49
50	398,5	718	622,4	86,7	3,2	1,28	378,82	1248,5	0,50
50	398,8	407	328,17	80,6	3,49	1,26	382,34	677,48	0,48
30	397	690	644,2	93,4	4	1,17	216,57	1462,4	0,44
30	398,9	493	451,6	91,6	3,72	1,18	217,96	1162,7	0,39
30	402,9	349	314,25	90,0	3,88	1,29	218,78	727,01	0,43
30	399,5	202	173,32	85,8	3,83	1,19	219,45	350,26	0,49
10	401	202	157,71	78,1	6,61	2,24	68,47	497	0,32
10	400,9	174	150,3	86,4	6,47	2,16	70,35	368,1	0,41
10	399,5	125	115,98	92,8	6,22	2,44	71,05	220,01	0,53
10	400	64	58,29	91,1	5,37	2,29	71,47	108,02	0,54

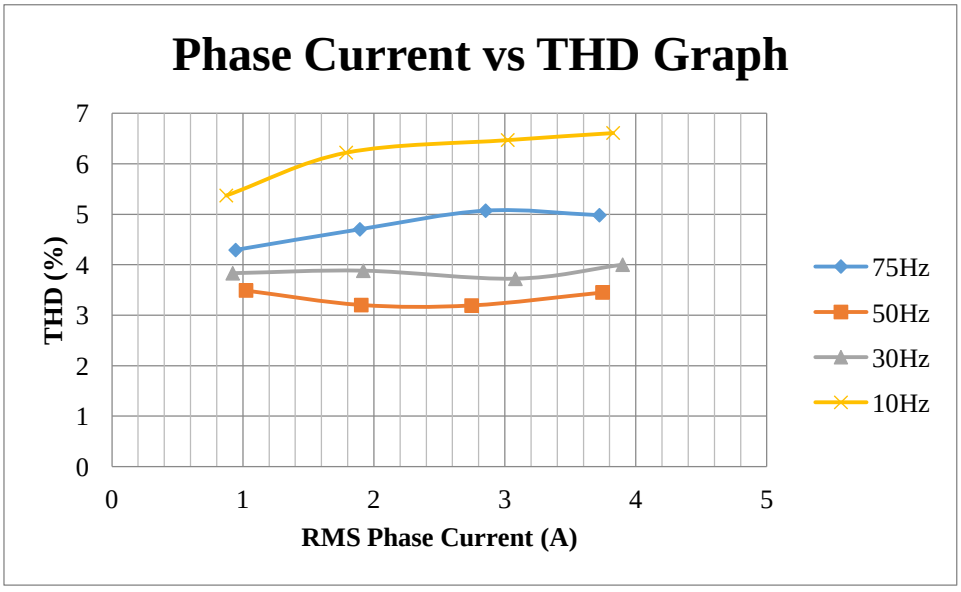


Figure 6-67 Phase Current vs THD Graph at 400V DC link

In Figure 6-67, THD of output voltage is drawn with respect to phase current at different frequencies. THD values are worse for 10Hz, 30Hz and 75Hz, this is because system is optimized for 50Hz operation. At 10 Hz, time step is large and output takes shape of step. This is also observed at 30Hz operation. At 75Hz, voltage slope is higher, thus it is harder to follow reference signal.

Table 6-13 Inductive Test Results at 540V DC link Voltage

Frequency (Hz)	V_{in} (V)	P_{in} (W)	P_{out} (W)	N (%)	V_{THD} (%)	I_{THD} (%)	V_{outf} (Vrms)	S_{out} (VA)	P.F
75	540,2	713	613,3	86,0	5,56	3,28	381	2505,5	0,24
75	542,2	432	325,1	75,3	5,75	2,21	382	1921,5	0,17
75	540,7	577	483,8	83,8	4,47	1,85	382,42	1256,5	0,39
75	540,7	499	394,9	79,1	4,29	1,93	379	624,8	0,63
50	540,2	1254	1162,9	92,7	4,48	1,77	378,64	2456,7	0,47
50	539,2	993	896,9	90,3	4,06	1,78	379,36	1829,8	0,49
50	538,7	714	624,5	87,5	3,98	1,81	381,17	1258,7	0,50
50	539,6	397	324,65	81,8	4,42	1,76	380,52	670,9	0,48
30	541,7	744	656,7	88,3	4,41	1,39	218,16	1489,9	0,44
30	543,6	532	454,5	85,4	4,18	1,35	218,67	1171,2	0,39
30	537,7	389	314,53	80,9	4,21	1,26	219,1	727,83	0,43
30	541,7	235	174,42	74,2	4,45	1,24	219,8	352,75	0,49
10	538,7	205	154,38	75,3	8,35	2,84	68,02	485,48	0,32
10	537,6	180	149,95	83,3	8,55	2,68	70,12	364,92	0,41
10	541,7	133	115,51	86,8	8,19	3,05	70,9	219,69	0,53
10	541,7	67	57,9	86,4	7,06	2,58	71,66	107,34	0,54

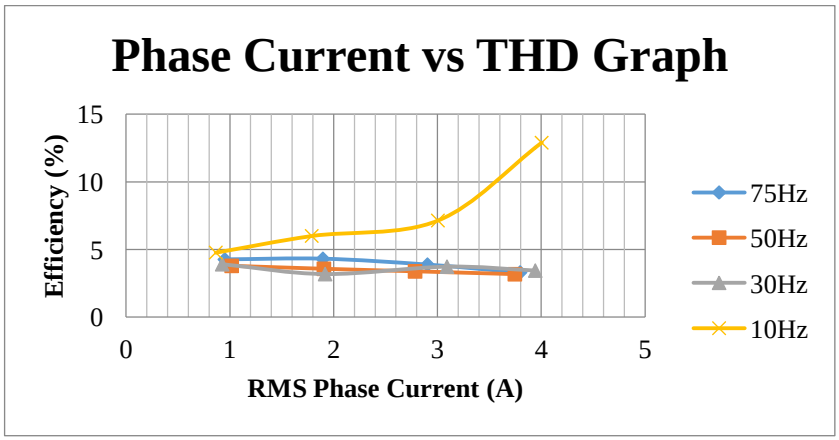


Figure 6-68 Phase Current vs THD Graph at 400V DC link

In Figure 6-68, THD of output voltage is drawn with respect to phase current at different frequencies. At 10 Hz, time step is large and output takes shape of step which increases the distortion. THD at other frequencies are similar and less than 5%.

6.3. Transient Tests

These tests are done to observe transient response during load step. For 400V and 540V DC link voltage, 0% to 100% and 100% to 0% load step is applied while inverter is operating at rated frequency. Mechanical switch is used to connect and disconnect load manually.

6.3.1. Test Equipment

VARSAN VARIAC: This equipment is used to supply power stage. Input voltage level is set by this equipment.

INSTEK GPS-3303: This equipment is used to supply control circuit. Two channels are used. 8V is used to supply control circuit and 24V is used to supply isolated converters which are used for gate drive circuit.

Agilent Technologies MSO-X 3024 Oscilloscope: This device is used to obtain voltage and current Waveforms. Two 100:1 voltage probes, one differential probe and 1 current probe is attached.

Agilent Technologies N2790A 100MHz differential Probe: This probe is used as voltage probe. It was necessary for measuring switching waveforms.

FLUKE i30S AC/DC current Clamp: This device is clamped over cable to measure current waveform.

6.3.2. Resistive Load Step

In this section, resistive load step response is analyzed. In the figures, line to line voltage V_{ab} is shown with pink color and load current I_{ab} is shown with magenta color. In Figure 6-69, 0% to 100% load step voltage and current waveforms are shown when DC link voltage is 400V. No distortion occurs at the output voltage waveform.

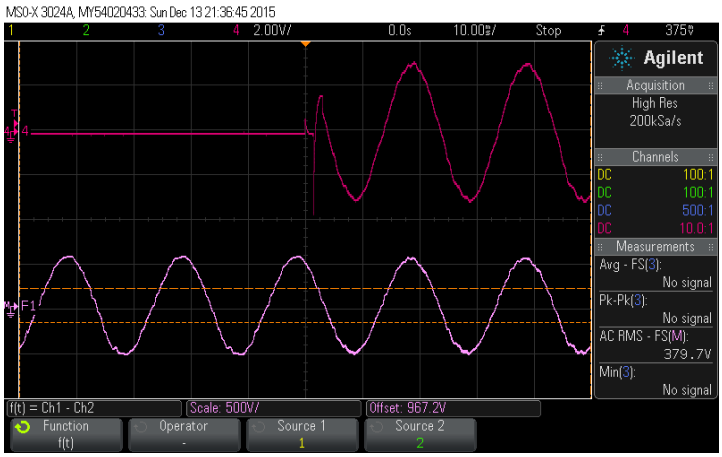


Figure 6-69 0% to 100% Resistive Load Step at 400V DC link

In Figure 6-70, 100% to 0% load step voltage and current waveforms are shown when DC link voltage is 400V. No distortion occurs at the output voltage waveform.

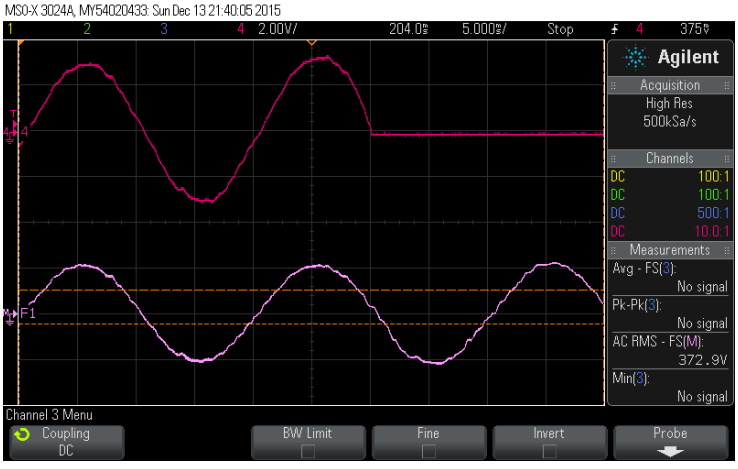


Figure 6-70 100% to 0% Resistive Load Step at 400V DC link

In Figure 6-71, 0% to 100% load step voltage and current waveforms are shown when DC link voltage is 540V. No distortion occurs at the output voltage waveform.

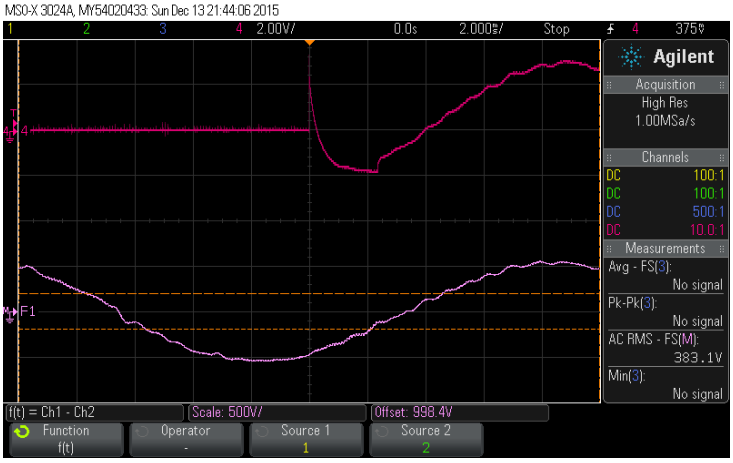


Figure 6-71 0% to 100% Resistive Load Step at 540V DC link

In Figure 6-72, 0% to 100% load step voltage and current waveforms are shown when DC link voltage is 540V. No distortion occurs at the output voltage waveform.

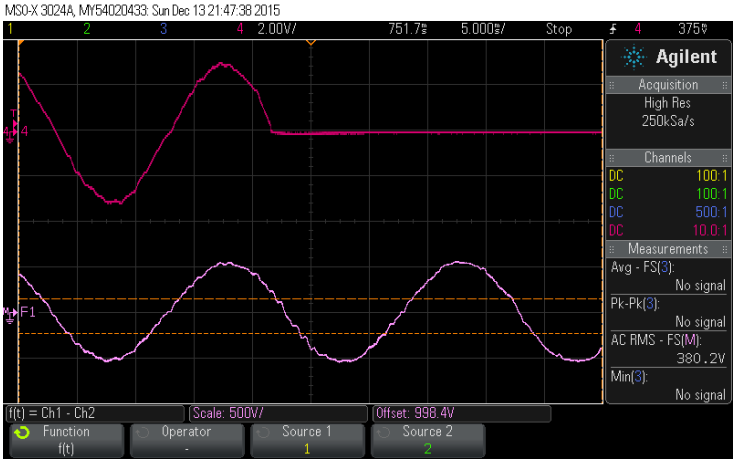


Figure 6-72 100% to 0% Resistive Load Step at 540V DC link

Inverter continues to operate successfully when resistive load step is applied when it is operated from 400V or 540V DC link voltage.

6.3.3. Inductive Load Step

In this section, inductive load step response is analyzed. In the figures, line to line voltage V_{ab} is shown with pink color and load current I_{ab} is shown with magenta color.

In Figure 6-73, 0% to 100% load step voltage and current waveforms are shown when DC link voltage is 400V. No distortion occurs at the output voltage waveform.

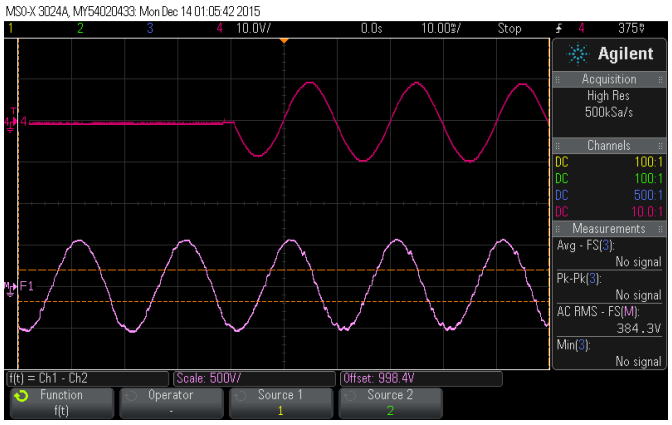


Figure 6-73 0% to 100% Inductive Load Step at 400V DC link

In Figure 6-74, 100% to 0% load step voltage and current waveforms are shown when DC link voltage is 400V. No distortion occurs at the output voltage waveform.

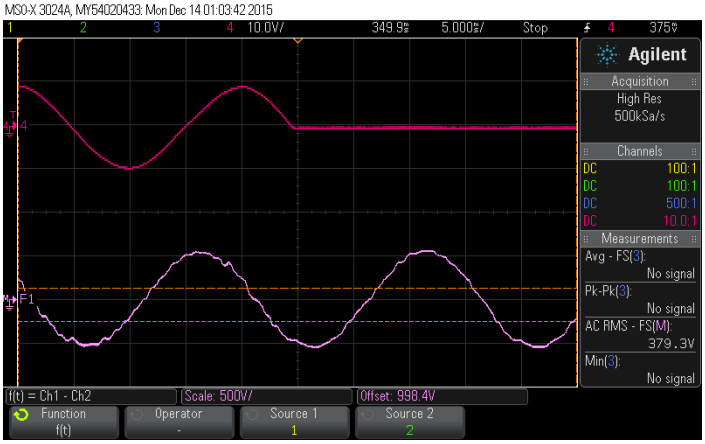


Figure 6-74 100% to 0% Inductive Load Step at 400V DC link

In Figure 6-75, 100% to 0% load step voltage and current waveforms are shown when DC link voltage is 540V. No distortion occurs at the output voltage waveform.

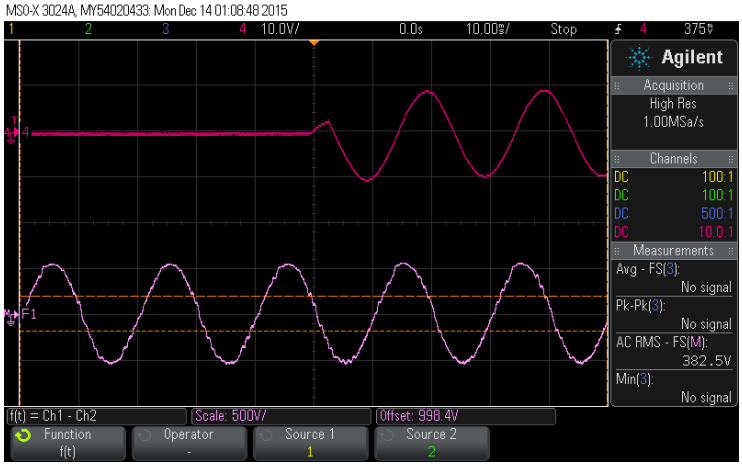


Figure 6-75 100% to 0% Inductive Load Step at 540V DC link

In Figure 6-76, 100% to 0% load step voltage and current waveforms are shown when DC link voltage is 540V. No distortion occurs at the output voltage waveform.

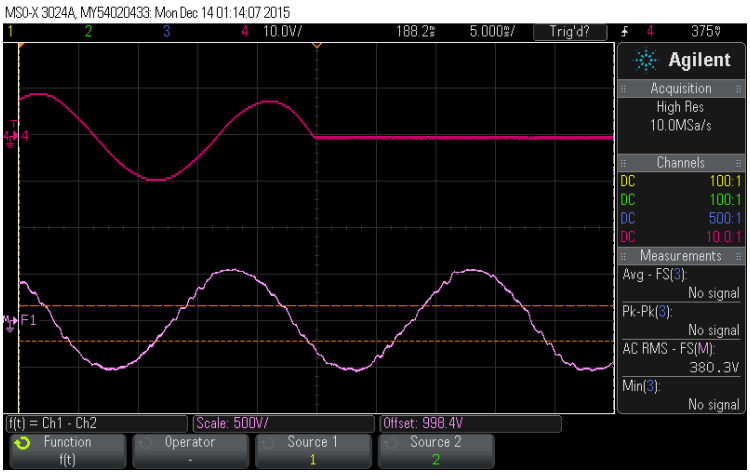


Figure 6-76 100% to 0% Inductive Load Step at 540V DC link

Inverter continues to operate successfully when inductive load step is applied when it is operated from 400V or 540V DC link voltage.

6.4. Motor Tests

An induction motor is driven to observe THD and efficiency of inverter at different frequencies. Motor is started at 10Hz and speed is increased by increasing frequency. Then motor is loaded with DC generator.

6.4.1. Test Equipment

VARSAN VARIAC: This equipment is used to supply power stage. Input voltage level is set by this equipment.

INSTEK GPS-3303: This equipment is used to supply control circuit. Two channels are used. 8V is used to supply control circuit and 24V is used to supply isolated converters which are used for gate drive circuit.

HIOKI 3184 DIGITAL POWER HI TESTER: This equipment is used to measure input power.

HIOKI 3194 MOTOR/HARMONIC HI TESTER: This equipment is used to measure output power and THD.

SIEMENS KB5-6: This equipment is induction motor which is used as load. This motor has 4 pole and output power is 3.5kW. Rated frequency is 50Hz, rated speed is 1400 rpm. Rated power factor at rated power is 0.8.

6.4.2. Motor Test Results

Induction motor used in the tests has 3.5kW rated output power. Inverter is capable of supplying 2.5kVA, thus the motor could not be loaded at full power. Motor is loaded such that inverter is operating at rated current. For 50Hz operation inverter is overloaded.

In Table 6-14, operating frequency, input power, output power, efficiency of inverter, voltage distortion, current distortion, apparent power and speed of the motor data is given when DC link voltage is 400V.

Table 6-14 Motor Test Results at 400V DC link Voltage

Frequency (Hz)	P_{in} (W)	P_{out} (W)	N (%)	V_{THD} (%)	I_{THD} (%)	S_{out} (VA)	Speed (rpm)
50	1342	1187,1	0,88	4,04	10,14	2881,4	1479
30	547	484,5	0,89	4,39	4,77	1467,8	885
10	474	403,7	0,85	10,46	9,55	522,77	251,5

Voltage distortion is measured less than 5% while inverter is operating at 50Hz and 30Hz. Voltage distortion at 10Hz is higher as it is explained in resistive and inductive load tests.

In Table 6-15, operating frequency, input power, output power, efficiency of inverter, voltage distortion, current distortion, apparent power and speed of the motor data is given when DC link voltage is 540V.

Table 6-15 Motor Test Results at 540V DC link Voltage

Frequency (Hz)	P_{in} (W)	P_{out} (W)	N (%)	V_{THD} (%)	I_{THD} (%)	S_{out} (VA)	Speed (rpm)
50	1326	1175,6	0,89	4,83	10,16	2912,4	1479
30	573	469,4	0,82	5,41	5,27	1491,5	885
10	482	417,05	0,87	12,1	9,82	518,41	251,5

Voltage distortion is measured less than 5% while inverter is operating at 50Hz Distortion values at other frequencies can be decreased by optimizing software for operation at that frequency.

The proposed method is also compared with classical method. A commercial inverter is used to drive same motor at same load and total losses are compared. The equate operating conditions, commercial inverters is also operated at 10kHz switching frequency. Commercial inverter which is used in the tests, do not contain boost stage and filter at the output. Motor is loaded by a DC generator and its power is measured. The test results are shown in Table 6-16. Efficiency of commercial inverter is measured to be higher than proposed method as expected since it does not contain boost stage and filter at the output, however total loss of the system i.e motor and inverter configuration is higher for classical method. Efficiency of the system is measured to be low because motors are not loaded with rated power. THD of proposed method is measured to be much better. In case a filter is used at the output of the classical invertere topology, the proposed topology would prove to be more advantageous.

Table 6-16 Motor Test Results at 540V DC at 50Hz Output Frequency

	P_{in} (W)	P_{out} (W)	P_{gen} (W)	Efficiency of Inverter (%)	Total Loss (W)	Efficiency of System (%)	V_{THD} (%)
Proposed Method	1390	1175,6	738	84,57	652	53,09%	4,83
Full Bridge	1443	1314	741	91,00	702	51,35%	49,5

6.5. Summary and Conclusions

The results show that the inverter is operating successfully under resistive and inductive loads and when it is driving an induction motor.

Voltage THD is lower than 5% for rated frequency (50Hz) and it is lower than 6% except operation at 10Hz. THD at 10Hz operation is higher because software is not optimized for 10Hz. Voltage steps in reference signal are constant for all frequencies. For better THD, reference values must be set individually for each frequency. By optimizing for each operation frequency, THD at 10Hz operation can also be made

less than 5%. THD values measured with resistive and inductive load tests, is higher than simulation results. This is due to oscillation in inductor current and solution is proposed for this problem.

Efficiency is higher than 82.3% for all resistive loads less than rated power. At rated power efficiency is 95.2% for resistive load at 540V DC link voltage and 93.3% for resistive load at 400V DC link voltage. Efficiency increases when output power increases. Thus it can be foreseen that increasing output power will increase the efficiency. Efficiency results are compared with simulation results and values are close to each other. During the tests feed forward constant voltage estimated from V/f is applied for output which results in less output voltage when frequency is low. Since voltage thus power is lower, efficiency at 10Hz is measured to be low with respect to other tested operation frequencies. If output voltage could be kept constant for different frequencies, efficiencies at different operating frequencies would be closer to each other. Since power decreases when loaded with inductive load, efficiencies of inductive load are measured to be lower with respect to resistive load.

Output voltage decreases when output current increases. Load regulation is 2.6% at rated frequency. Feedback from output voltage levels is required to be used to improve load regulation.

Output voltage is observed for load steps. Inverter operates successfully during 0% to 100% and 100% to 0% load steps, undershoot and overshoot is not noticeable. There is no change at output voltage waveform except magnitude decreases slightly.

The implemented inverter is capable of driving an induction motor at different speeds. To improve drive performance current control can be added to the system. As described in chapter 1, motor test results show that core losses decrease when motor is supplied with sinusoidal waveform instead of PWM waveform.

CHAPTER 7

CONCLUSION

Starting point of this study was to design an inverter with pure sine wave output. Benefits of pure sine wave output over PWM output are discussed in Chapter 1. To achieve pure sine wave output, various topologies in the literature with sine wave output are analyzed to understand operation principles of them which were described in Chapter 2. These topologies described in Chapter 2 which are alternative to classical inversion approach are designed for single phase output and they are mainly designed for solar power applications. These topologies are analyzed according to ratings and costs of components assuming that they are supplied with rectification of single phase grid voltage. Another criteria which was focused on, is two way power flow ability which is important for driving motors. The topologies are divided into two groups; topologies without boosting capability and topologies with boosting capability. To calculate component ratings, topologies are assumed to be supplied from grid. Component ratings of topologies in the literature which were designed for solar power applications are calculated to be higher since they are designed for boosting and operate more efficient at lower input voltage. Topology E (Novel Bidirectional DC-To-AC Inverter) described in Chapter 2 which contains buck converter stage followed by an inverter stage, is observed to be beneficial for single phase operation. This topology is not capable of boosting; however special attention is paid to this topology because this topology decreases the required fast switch count and only needs extra slow switches with respect classical single phase full bridge. In this topology only two switches are switched at high frequency in the buck converter stage. Four switches in the inverter stage are switched with output voltage frequency. Furthermore these switches operate at zero voltage crossing and therefore they are virtually lossless, only conduction losses appear on swithces. Since fast switching switch count is decreased, switching losses are decreased and efficiency of this

arrangement is higher with respect to single phase full bridge. Topology E is designed for producing single phase output. Since aim of this study is to produce three-phase output, some modifications are done to topology E to obtain three-phase output. Four different modified versions of this topology are proposed and compared with classical full bridge topology. Two of these modified topologies (three isolated converters and two isolated converters) need isolation because short circuit path occurs during switching. Isolation requires additional components thus increases cost and decreases efficiency. One of modified topologies (two non-isolated converters) requires many switches at inversion stage which hardens the control of switches and increases cost. One of modified topologies (three non-isolated converters) seemed better than others because it did not require extra slow switches; only 6 fast switches are required at buck converter stage. This topology is compared with classical three phase full bridge with LC filter at the output. The cost values are same because it is assumed that topologies contain same filter, however efficiency of three non-isolated converters is measured to be 97.8% whereas efficiency of classical method is measured to be 98.3%. The results show that benefits of topology E (described in Chapter 2) obtained in single phase applications is not obtained in three phase applications because fast switching switch count cannot be decreased in three phase application. After obtaining this result, this study is continued by evaluation of topologies with boosting capability.

Advantages of boosting capability were discussed in Chapter 1. In Chapter 4, sine wave output topologies with boosting capability are analyzed. Single phase topologies which are described in Chapter 2, are modified to obtain three phase output. A topology which is capable of producing sine wave output and capable of boosting the voltage is also proposed. Topologies in the literature and proposed topology are compared according to ratings of components and cost. As described earlier, topologies described in Chapter 2, are mainly for solar power applications. Component ratings are calculated to be higher in topologies which are designed for solar power applications, with respect to the proposed topology and the classical method. Classical methods consist of using boost converter, three phase full bridge and LC filter at the output. The proposed topology and classical method are

compared according to cost and efficiency. According to the simulation results, the proposed topology increases efficiency nearly 1% with respect to classical method for analyzed power and voltage values. The results may differ for different power and voltage ratings. Size of the inductor in the proposed method and output stage of classical method are close to each other. Current rating is slightly higher in proposed method, however inductor used in the boost converter is eliminated. Although switch counts increase in the proposed method, elimination of boost converter stage is estimated to decrease total cost nearly 15% as compared to the classical arrangement (boost stage + three-phase bridge + filter). One disadvantage of the proposed topology is that it cannot operate at unity power factor since it requires DC voltage in input side. In the classical approach boost converter on the input side may be also used to obtain power factor correction (PFC). Adding a PFC stage to proposed method will increase cost of the inverter and decrease total efficiency of the system. Thus the usage of proposed method is proper when unity power factor operation is not a requirement. The proposed topology can easily be used in systems which are directly supplied with DC source such as battery powered systems or solar powered systems.

According to the results obtained by cost analysis and efficiency analysis in Chapter 4, the proposed topology show some benefits over efficiency and cost with respect to classical method under tested operating conditions. To observe the operational performance of the proposed topology and analyze feasibility of the proposed topology, the proposed topology is designed and implemented. The proposed topology is designed to supply 2.5kW at rated output frequency (50Hz) and to obtain 380Vrms (line to line) voltage at the output. It is also designed for operation between 10Hz to 75Hz output frequency. While designing the inverter, the focus was on the operation of the power stage at variable output frequency and variable DC link voltage. The designed circuit is for feedforward operation (DC link voltage is measured to calculate duty cycles of switches. In other words the controller has no output voltage feedback, therefore the voltage output of the inverter falls with increasing load.

The inverter is tested for different output frequencies, different DC link voltages and with different loads. According to test results, proposed topology produces three phase sine wave output whose THD is less than 5% at rated frequency. Objective of producing sine wave output is satisfied and proven by test results. To improve THD, there are issues to be studied later which are described in the future work section.

Another objective of this study was to design a circuit with good boosting capability. It is observed that inverter is able to operate when the DC bus voltage is 26% (400V) less than nominal voltage (540V) which is minimum operating voltage of designed inverter. By redesigning power components, operation at lower input voltages can also be achieved.

The designed and implemented circuit is observed to satisfy the two goals of this study, which are having a sine wave output and capability of operation under reduced DC link voltage levels. However improvements are needed, which are discussed in the future work section.

Issues to be studied in future work:

- Load Regulation: To improve load regulation voltage feedback from output must be added to system. In Chapter 5, software design is explained. Calculation time for time interrupt function is measured to be 100uS. When the inverter operates at 75Hz, duty cycles are reprogrammed each 133.33uS. Duration left for the main function is 33.33uS which is enough to make an ADC reading for input voltage and to read switch states. If control loop for voltage feedback is operated in microcontroller, it will require additional calculation time. Therefore, either duration for reprogramming duty cycles must be increased or microcontroller must be replaced by another whose capacity is better. If duration for reprogramming duty cycles increases, distortion at the output will also increase.
- Efficiency: To increase efficiency, inductance value must be increased; however it increases the size and cost of inductor.

- THD: Inductor current control must be added to the feedback loop to decrease oscillations in the inductor current and the output voltage. Another method is the change of configuration of output capacitors which also requires voltage feedback from output.
- Operating Output Frequency Range: Capacitor at the output limits frequency range since it is charged and discharged continuously each cycle. Smaller capacitance value can be used to operate inverter in higher frequencies, however, THD of output voltage also increase when capacitance value is decreased.
- Maximum Output Voltage Level: Inverter can operate at higher output voltage by increasing voltage rating of capacitors which will allow inverter to drive motors without field weakening.
- Boosting Ratio: By redesigning the circuit, the inverter can operate at lower DC bus voltages.
- MPPT (Maximum Power Point Tracking): MPPT can be achieved by adding output current control to the proposed topology. Supplied current to grid or load, can be adjusted to draw maximum power from power source

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