DESIGN OF AN X-BAND 3-BIT RF MEMS CONSTANT PHASE SHIFTER

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Approval of the thesis:

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ABSTRACT

DESIGN OF AN X-BAND 3-BIT RF MEMS CONSTANT PHASE SHIFTER

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This thesis presents a 3-bit 180° constant phase shifter design implementing Co-Planar Waveguide (CPW) and RF MEMS variable capacitors with ±1.8% accuracy at 10 GHz and ±5.8% maximum peak error between 9-11 GHz. The phase shifter with minimum phase errors is determined by considering exemplary circuit simulations of different phase shifter types designed with a novel in-house RF MEMS fabrication process [1] parameters. Due to its wide-band characteristics and CPW compatibility, the selected topology is the reflect-type phase shifter employing RF MEMS capacitor banks and 3-dB couplers. Phase shifts are provided by the change in the reflection phase of RF MEMS capacitor banks. At first, a 2-bit 90° phase shifter is designed to cover 0°-90° phase shifts. Successive addition of two 2-bit phase shifters allows to obtain a 3-bit operation up to 180° phase shift.

The capacitor bank design includes various configurations of RF MEMS capacitors, and they are compared to provide minimum phase errors between 9-11 GHz. The

design procedure is managed while having regard to the in-house novel RF MEMS fabrication technique [1] and its design rules. Two different options are considered for the design of 3-dB couplers, namely regular Branch-Line Coupler (BLC) and Double Branch-Line Coupler (DBLC), comparing their bandwidths which are defined by phase difference and power imbalance between coupled and thru ports. Circuit simulations suggest to use a miniaturized double branch-line coupler (M-DLBC) implementing CPW Lines shortened with lumped air-bridge capacitors, and therefore this coupler and RF MEMS capacitor banks are modelled and simulated by using a 3D Electromagnetic (EM) solver software. The proposed 3-bit phase shifter provides phase shifts with a ±1.8% accuracy at 10 GHz and ±5.8% maximum peak error between 9-11 GHz. The mechanical parameters such as spring constant and pull-in voltages of RF MEMS bridges used in the phase shifter are also calculated.

Keywords: Phase Shifter, RF MEMS, CPW, X band, Double Branch Line Coupler

ÖZ

X-BANT 3-BİT RF MEMS SABİT FAZ KAYDIRICI TASARIMI

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Bu tez çalışması, 10 GHz'de ±1.8% doğruluğunda ve 9-11 GHz bandında en fazla ±5.8% hataya sahip, Eşdüzlemsel Dalga Klavuzu (EDK) ve RF MEMS değişken sığaç yapılarını kullanan bir 3-bit 180° sabit faz kaydırıcı tasarımı sunmaktadır. En az hataya sahip faz kaydırıcı, farklı faz kaydırıcı çeşitlerinin yenilikçi bir kurum-içi üretim parametreleri [1] ile tasarlanmış, örnek devre benzetimleri incelenerek belirlenmiştir. Daha geniş bant aralığı sunması ve EDK uyumlu olması sebebiyle, seçilen topoloji RF MEMS sığaç bankaları ve 3-dB bağlayıcıları kullanan yansıtmalı faz kaydırıcı olmuştur. Faz basamakları, RF MEMS sığaç bankasının yansıma fazındaki değişikliklerle sağlanmıştır. Öncelikle, 0°'den 90°'ye kadar faz farkı verebilen 2-bit faz kaydırıcı tasarlanmıştır. Bu faz kaydırıcılardan iki tanesinin arka arkaya eklenmesiyle, 3-bit ile çalışan 180° faz kaydırıcı elde edilmiştir.

Sığaç bankası tasarımı, farklı RF MEMS sığaç düzenlemelerini içermektedir ve bunlar 9-11 GHz aralığında en az faz hatası vereni bulmak üzere karşılaştırılmıştır. Tasarım

süreci, yenilikçi üretim tekniği [1] ve tasarım kuralları göz önünde bulundurarak yürütülmüştür. 3-dB bağlayıcı için normal Branş-Hatlı Bağlayıcı (BHB) ve Çiftli Branş-Hatlı Bağlayıcı (ÇBHB) olmak üzere iki seçenek, bağlı ve direk çıkışları arasındaki faz farkı ve güç dengesizliği tarafından belirlenen bant genişlikleri karşılaştırılarak incelenmiştir. Devre benzetimleri, hava-köprü sığaçları ile kısaltılmış EDK hatlarını kullanan, Küçültülmüş Çiftli Branş-Hatlı Bağlayıcı (K-ÇBHB)'yı öne çıkarmış, bu bağlayıcı ve RF MEMS sığaç bankası 3 boyutlu olarak Elektromanyetik (EM) çözücü yazılımında modellenmiş ve benzetimleri yapılmıştır. Sunulan 3-bit faz kaydırıcı, 10 GHz'de ±1.8% doğruluk ve 9-11 GHz bandında en fazla ±5.8% hatalı faz kaymaları sağlamaktadır.

Anahtar Kelimeler: Faz Kaydırıcı, RF MEMS, EDK, X bant, Çift Branş-Hatlı Bağlayıcı

Dedicated to my family…

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CHAPTER 1

INTRODUCTION

Wireless systems, which can be integrated in all kind of "things" together with various sensors, receive a world-wide attention these day and this trend is named as "Internet-of-Things". Portable GPS devices help people to navigate themselves while smartphones employ new protocols for improved communication delighting users with superior multimedia functions. Consumer electronics, even home appliances such as thermostats and coffee machines, are equipped with wireless communication modules like Wi-Fi or Bluetooth. Growing interest in these trends pushes the manufacturers to pay their attention to miniaturization and low-power integration of wireless communications keeping the cost minimized. All these advancements direct the attention of industry and research organizations to RF sections with compact-sized, low-cost, high performance to meet tight specifications with minimum battery usage [2].

RF MEMS (Radio Frequency Micro-Electro-Mechanical Systems) has been an advancing technology area which has an increasing attention from both the industry and the universities. RF MEMS has various solutions which have the potential to address the needs of device manufacturers mentioned [3]–[6]. Although it is a recent technology compared to its semiconductor counterparts, successful applications of RF MEMS devices such as microwave and millimeter-wave radars, smartphone transceivers, satellite and instrumentation systems are exemplified in the literature [7].

This thesis focuses on design of microwave components with an intention to exploit superior properties of the RF MEMS technology. In next section, some of these properties are overviewed.

1.1. An Overview of RF MEMS Switches

Radio Frequency (RF) waves correspond to electromagnetic waves of which frequencies are in the range from 300 MHz to 300 GHz in the electromagnetic spectrum. The intersection of Radio Frequency (RF) and Micro-Electro-Mechanical Systems (MEMS) research areas is about devices and systems which are microfabricated and to operate in RF region [8]. In this region, the devices and components are placed on and connected with planar transmission lines, which are coplanar waveguide (CPW) lines or micro-strip lines. As they are small in size and relatively low-cost enabling monolithic integration with other components, RF MEMS attracts researchers and engineers. In the last decades, RF MEMS switches and phase shifters have been developed with promising characteristics such as low-insertion loss and low DC-power consumption [9].

One of the most important properties of RF MEMS is reconfigurability and it enables the system to adjust itself to circumstances and provides automaticity. This reconfigurability is mainly provided by RF MEMS switches [2], [10]–[21] and tunable capacitors [22]–[25]. Especially, RF MEMS switches are preferred due to their superior performances such as low insertion loss and high isolation, over Field Effect Transistors (FET) and PIN diodes [7].

Due to their low-loss microwave and millimeter-wave applications, MEMS actuated shunt switches have been developed. These switches employ a thin metal membrane bridge which is suspended over the center conductor which serves as the signal trace as in Figure 1.1. The bridge has anchors on the ground conductors and fixed at either one or two ends. By applying a DC voltage, an electrostatic force is generated between the bridge and the signal trace beneath it which results in pull-down of the bridge on

the dielectric surface preventing DC-short but forming an RF low-impedance path to ground [26].

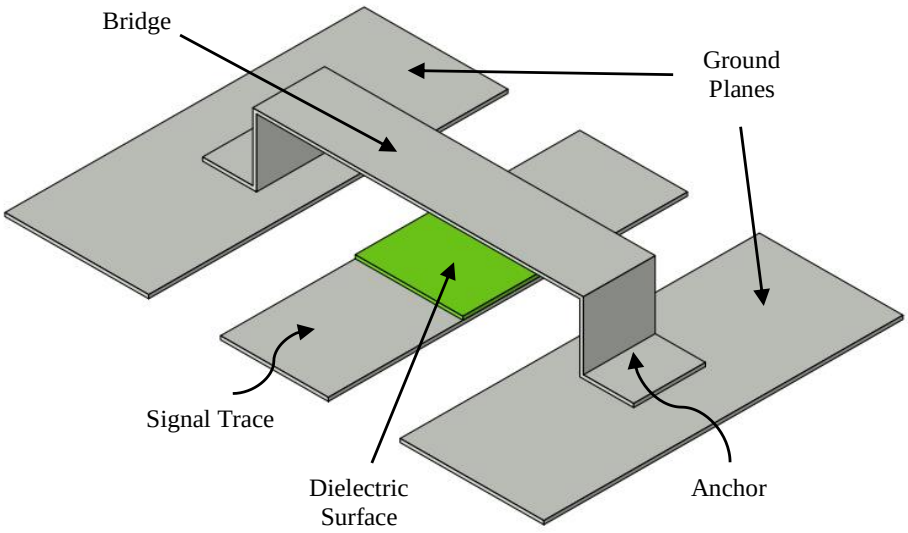


Figure 1.1. 3D view of a typical RF MEMS capacitive, shunt switch [2].

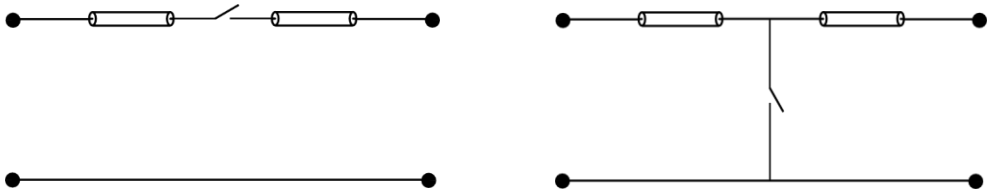
While the structure may seem simple, increasing the frequency of operation requires more exhaustive design procedure and robust fabrication conditions to fulfill the performance specifications.

RF MEMS switches found in the literature may be divided into three main groups regarding to their circuit configurations, contact types and actuation mechanisms.

1.1.1. Circuit Configuration Types

As one can predict, RF MEMS switches enable passing or blocking the signals propagating in a transmission line which they are placed on. For monolithic and planar fabrication approaches, CPW transmission lines and microstrip lines are generally preferred. RF MEMS switches can either connect transmission lines together allowing

signal to pass in series configuration or couples the signal to the ground for blocking in shunt configuration [8]. These circuit configuration types are shown in Figure 1.2.

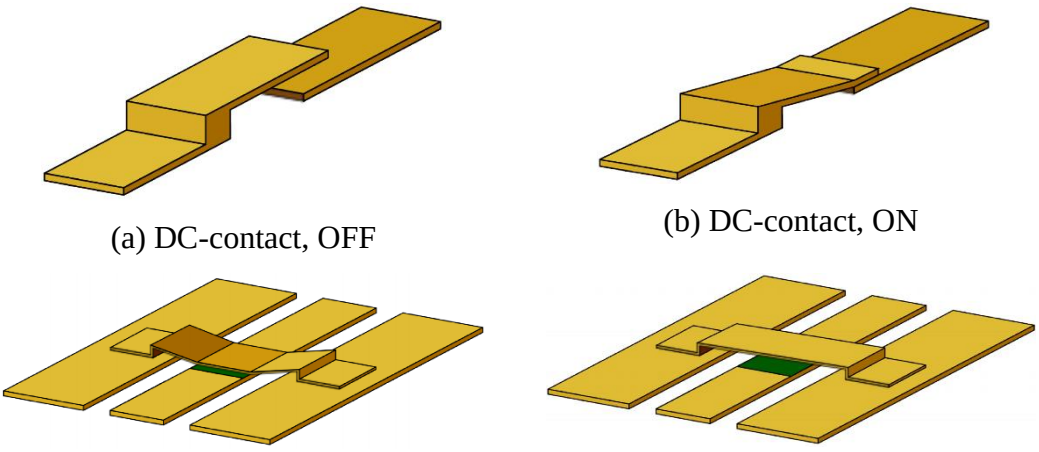


(a) (b)

Figure 1.2. RF MEMS switch circuit configurations: (a) Series and (b) Shunt.

For CPW lines, shunt configuration is preferred mainly due to simplicity in fabrication process. The METU RF MEMS process is also optimized for fabrication of switches in shunt configuration [2].

1.1.2. Contact Types



(a) DC-contact, OFF (b) DC-contact, ON

(c) Capacitive contact, OFF (d) Capacitive contact, ON

Figure 1.3. DC and capacitive contact RF MEMS switches [8].

Besides their circuit configurations, RF MEMS switches can be classified into two groups according to the type of contact between the signal trace and the suspending MEMS-bridge. Two main types are DC-contact and capacitive-contact switches as they given in Figure 1.3.

1.1.3. Actuation Mechanisms

RF MEMS technology employs micrometer sized movable parts to switch between ON and OFF states, and provides functionality in RF domain. These parts can be actuated by different mechanisms. Main examples of these mechanisms are electrostatic, piezoelectric, electrothermal and magnetic actuation. In the digital world small chip size, fast response time and power consumption are the most common desired properties. As the electrostatic actuation mechanism provides these properties, it is the most favored [2]. Thus, only electrostatic actuation mechanism is of interest in this thesis.

DC and capacitive contact switch mechanisms shown in Figure 1.3 are examples of the electrostatic actuation mechanism. MEMS cantilevers or bridges can be pulled down with an application of a DC voltage difference between the signal trace and the ground plane. For shunt switches, the bridge itself is connected to the ground. The electric field created between the signal trace and the bridge results in a force on the bridge and after a certain potential difference the bridge collapses. This is known as *pull-in* phenomenon and the minimum potential difference is called as *pull-in voltage (V_{pi})* [7]. If a potential difference equal or greater then V_{pi} is applied, the bridge will collapse and the DC-contact, the series switch will be in ON but capacitive-contact, shunt switches will be in OFF state as indicated in Figure 1.3.

1.2. An Overview of Phase Shifters

Phased arrays employ electronic, mechanical, or material switches to change the phase of individual radiating elements across an antenna enabling the radiated beam to steer. Communication and radar systems incorporating phased arrays will enable greater efficiency, higher data rates and increase access between greater numbers of links. [9]

Phase shifters are one of the key components of the active phased arrays which use transmit/receive (T/R) module for modern radar applications [27]. In Figure 1.4, the typical schematics of T/R module for X-band phased array antenna is shown. Note that the path in the middle implements a phase shifter and an attenuator which are reciprocals and allow to use the module in both transmit and receive modes. In [28], a multiple antenna receiver for the phased array operating at higher frequencies is also described. CMOS phase shifters have been also presented in the literature [27-31].

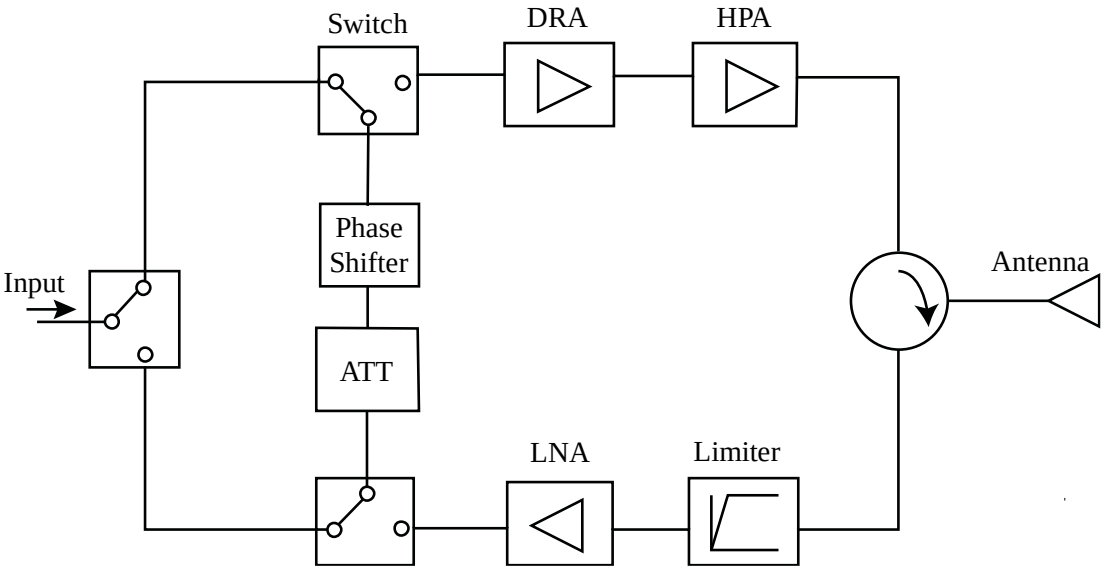


Figure 1.4. Typical schematic of T/R module for X-band [27].

RF MEMS phase shifters are elaborated in this study, as they provide superior performances such as low insertion loss and high isolation, over Field Effect Transistors (FET) and PIN diodes [7].

1.3. Motivation of Dissertation

Advanced material and microfabrication techniques have enabled Integrated Circuits (ICs) to operate frequencies above 5 GHz [30]. These advancements facilitate the monolithic integration of lumped and distributed elements. Integration of MEMS and CMOS components is also much easier thanks to novel microfabrication techniques.

METU RF MEMS Group has been involving in almost all areas related to RF MEMS field. Throughout the years, many qualified researchers have contributed to this area in both theory, design and fabrication. Especially, RF MEMS capacitive, shunt switches on co-planar waveguides have been extensively studied in the group [2],[31],[8]. Recently, RF MEMS switches have been zero-level [8] and wafer-level [32] packaged and microwave characterization of these packaging approaches have been performed.

In this dissertation, an upper-level design approach is employed to satisfy design specifications given in next section. That is, novel RF MEMS switches, of which design and fabrication techniques developed by METU RF MEMS [33], are implemented as variable and fixed capacitors to build couplers and tuneable capacitor banks to obtain a digital phase shifter with maximum phase accuracy.

1.4. Design Objectives and Organisation of the Thesis

The main objective of this thesis is to design a digital constant phase shifter which employs RF MEMS technology developed previously and satisfies design specifications given in Table 1.1. Another goal is to review phase shifter topologies and discuss their characteristics to be able to decide which one suits for the given project.

Table 1.1. Specifications for phase shifter designed in the thesis.

Specification	**Value**
Operation	3-bit
Input/Output Port Type	CPW, On-wafer
Frequency Band	9-11 GHz
Phase Accuracy Error at 10 GHz	±2% (each bit)
In-band Peak Phase Error	±8% (per bit)
Insertion Loss	Not Specified
Size Limitation	Not Specified

Following this introduction chapter, Chapter 2 reviews various digital phase shifters with circuit designs and simulations for each. At the end of that chapter, simulation results are compared and their suitability for design specifications in Table 1.1 are discussed.

Chapter 3 includes different capacitor bank implementations as reflective terminals to be connected to the coupler. Again, ideal designs and simulations are conducted for three designs. Design-3 is chosen to be best candidate due to lower phase errors and modelled in EM simulator.

Chapter 4 explains the design methodology for 3-dB, quadrature hybrid coupler. This chapter features regular branch-line coupler (BLC), double stage branch-line coupler (DBLC) and their miniaturized configurations with RF MEMS capacitors. They are first designed with ideal components and simulated. After comparison of their performances, M-DBLC with the widest bandwidth, is modelled in EM simulator.

Lastly, Chapter 5 investigates the integration of coupler and capacitor bank EM models and overall performance of designed phase shifter is also discussed. In Chapter 6, conclusion and future work are given.

CHAPTER 2

REVIEW OF DIGITAL PHASE SHIFTER TOPOLOGIES

This chapter deals with analysis and design of common phase shifter topologies. Sections 2.1-2.3 introduce classifications of phase shifters and compare them in terms of their fabrication techniques, operation and response over frequency. Sections 2.3-2.8 describe various phase shifter topologies and also include design examples with in-house fabrication standards. Finally, Section 2.9 evaluates phase shifter performances with interpretation of simulation results and discusses their suitability for design specifications. It concludes that reflect-type phase shifter which employs RF MEMS capacitor banks is the most promising topology.

2.1. Introduction to MEMS Phase Shifters

Microwave and millimeter-wave phase shifters play essential roles in phased array antennas for telecommunications and radar applications. They are currently compromised of ferrite materials, PIN diodes, or FET switches [7]. Although they provide prominent solutions, they have various drawbacks. Main advantages and disadvantages of these systems are listed in Table 2.1.

Due to the fact that FET-based phase shifters can be integrated with amplifiers on the same chip which means lower assembly cost, they have been used extensively in modern phased arrays [7]. However, they cannot compete with the loss performance of the RF MEMS-based phase shifters and the main reason for this low loss characteristics is that MEMS switches have very low series resistance [31].

Table 2.1. Some advantages and disadvantages of phase shifters.

System	Advantages	Disadvantages
Ferrite Phase Shifters	Excellent performance, High RF power handling, Low insertion loss	Expensive fabrication, High DC power consumption, High weight
Solid-state Phase Shifters	Monolithic integration, Low power consumption	High RF loss
PIN diodes	Low loss operation at mm-wave frequencies	High DC-power consumption

2.2. Analog Phase Shifters vs. Digital Phase Shifters

There are two basic designs of phase shifters in terms of changing the phase shift: The analog and digital phase shifters. The analog phase shifter provides a continuously variable phase shift, from 0° to 360°, and it employs generally varactor diodes. Digital phase shifters are useful for a discrete set of phase delays. Switches are usually used for digital operation. Here, it should be noted that the performance of phased array antenna is directly related to the number of bits employed, and most systems require a 3-bit or a 4-bit design for higher scanning solutions [7].

The main advantage of the digital phase shifter over its analog counterparts is the reduction of the area of the device for the same amount of phase shift. However, the resolution of phase steps decreases as a penalty for the gain in the area [31]. If high resolution is desired, the number of bits increases and so the fabrication complexity.

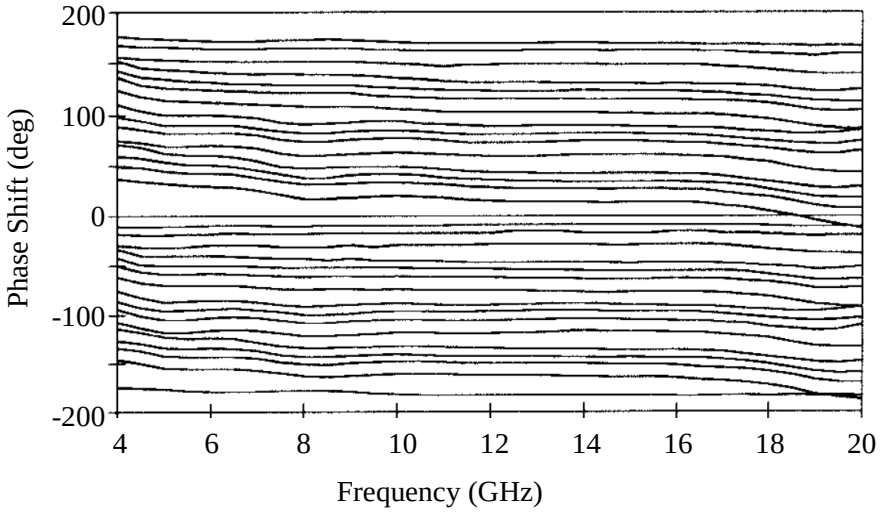
2.3. Introduction to Digital Phase Shifters

According to their phase shift response over frequency, digital phase shifters can be classified in two categories,

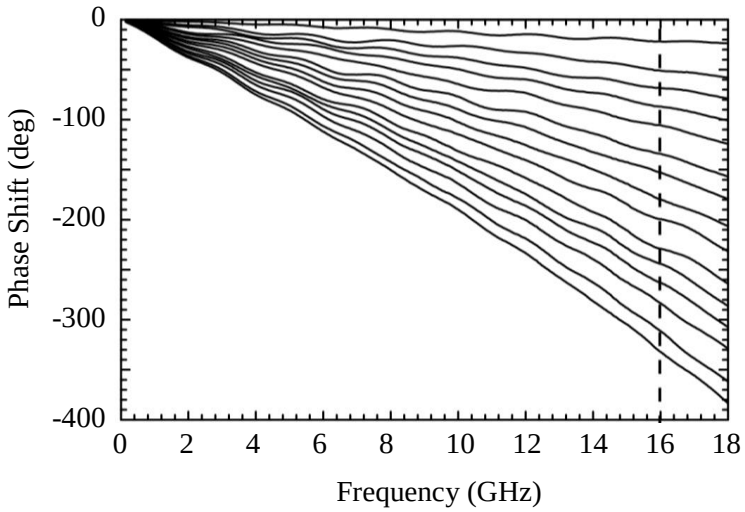
(a) Constant phase versus frequency,

(b) Linear phase versus frequency.

Examples of these categories are given in Figure 2.1. In [34], a 6-bit MMIC phase shifter is described with the best reported performance levels over the 6 to 18 GHz band. As shown, it has a flat phase shifts over frequency with certain RMS errors.



(a) MMIC 6-bit phase shifter with constant-phase versus frequency [34].



(b) DMTL phase shifter with linear-phase versus frequency [35].

Figure 2.1. Phase shifter types in terms of response over frequency.

For DMTL phase shifters such as the study presented in [35], the response usually increases linearly with the frequency as shown in Figure 2.1(b). This type of phase shifters are dominant in true-time-delay phased arrays. Applications especially that require a wide bandwidth, can be easily implemented using switched delay lines [7].

Constant-phase designs are generally used for signal processing in radar applications, wideband communication systems and components (SSB mixers, vector modulators, balanced amplifiers, etc.), and high-precision instrumentation systems [7].

MEMS switches are one of the best candidates to use in digital-constant phase shifters which results in lower loss phase shifters at any frequency, and especially from 8 to 100 GHz. Thus, an increasing interest has grown in the research and industry communities and various phase shifters [6,9,35,36] have been developed. Moreover, as MEMS switches have very small up-state capacitances, they provide a wider band performance than when similar designs implements solid-state devices. MEMS phase shifters also enable a considerable reduction in the DC power for large phased arrays, especially in receive-only systems. Lastly, MEMS switches can be fabricated directly with the antenna element which enables low-cost phased arrays [7].

In the following sections, digital phase shifters and their characteristics are reviewed. A simple and ideal example for each type is designed at 10 GHz and corresponding results are given.

2.4. Switched-Line Phase Shifters (SLPS)

Switched delay-line implementations are shown in Figure 2.2. Every delay bit is implemented separately, and an N-bit phase shifter is constructed by cascading several bits of different values. The phase delay is obtained by switching in the required number of bits. For example, if a 90° phase shift is needed, then only bit #2 is switched in the circuit. However, if a 225° phase shift is required, then bits #1 and #3 are used. The phase shift increases linearly with frequency as expected from all delay-line techniques with minimal transmission line dispersion [7].

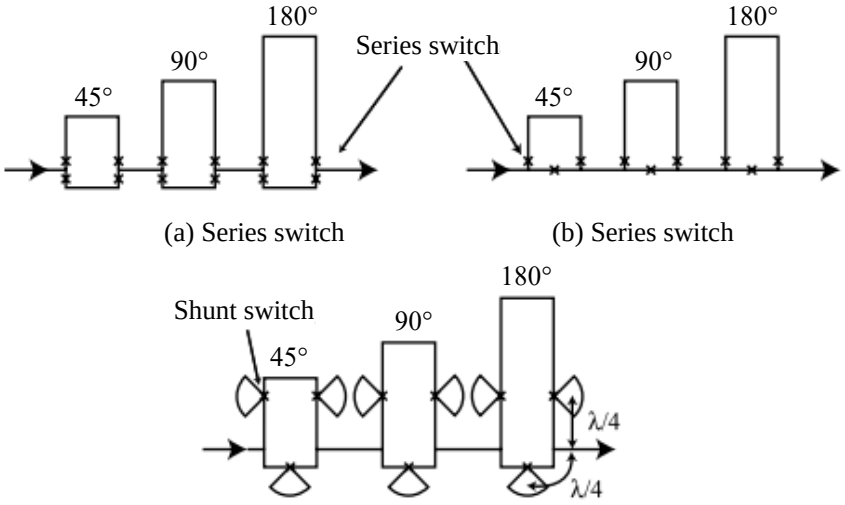


Figure 2.2. Switched-line phase shifters. Series and shunt switch implementations.

An ideal SLPS employing 22.5°, 45° and 90° electrical length transmission lines and ideal *Single Pole, Double Throw (SPDT)* switches are designed in Figure 2.3. As seen from the frequency response simulations of this design in Figure 2.4, the phase shift is not constant over the frequency but rather increases linearly with it. In addition, shunt-switch implementations are used only in a microstrip design. Although series-switch implementation on CPW is possible, due to size considerations and limited bandwidth, switched-line phase shifters are not suitable for constant phase shifters [7].

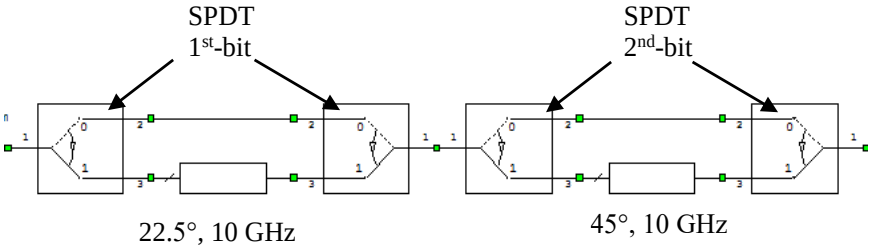


Figure 2.3. First two bits of a SLPS implementing ideal SPDT switches.

Table 2.2. Design parameters for switched-lines.

Electrical Length	W	G	L
22.5°	240 μm	30 μm	1124 μm
45°	240 μm	30 μm	2248 μm
90°	240 μm	30 μm	4496 μm

In Table 2.2, design parameters for 22.5°, 45° and 90° CPW lines are listed. The materials used are 500μm-thick glass substrate with $\varepsilon_r = 4.6$ and gold conductor lines with $\sigma = 3.10^7$ Siemens, which are METU RF MEMS process parameters [2].

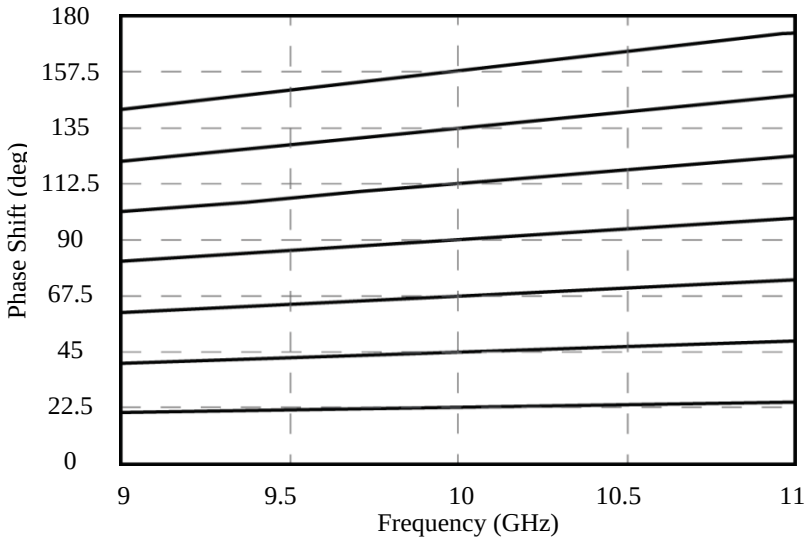


Figure 2.4. The phase shift performance of an ideal SLPS designed at 10 GHz.

2.5. Reflect-Line Phase Shifters (RLPS)

An example of N-Bit shunt switch, reflect-line phase shifter is shown in Figure 2.5. The bandwidth, defined by reflection coefficient and phase shift versus frequency, for an N-bit phase shifter is significantly smaller than a standard 50-Ω coupler. Moreover,

it is dependent on the phase delay. This is because the coupler is reactively terminated with a different reactance for every phase step.

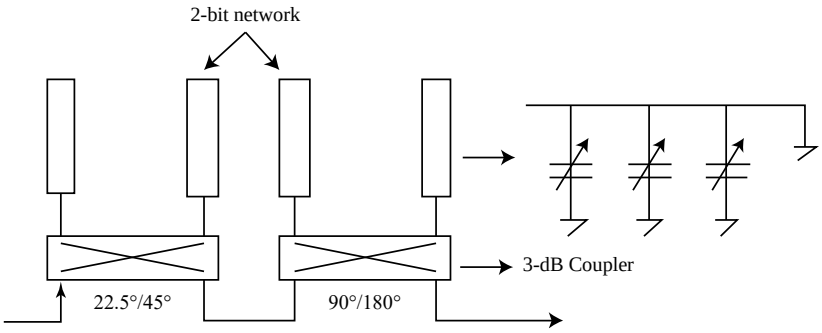


Figure 2.5. A 4-bit RLPS cascading two 2-bit RLPSs.

As the reflective circuit employs transmission lines, the phase shift will be dependent on the frequency and their application providing constant-phase over frequency is difficult. Even though ideal SPDT switches and with RF-MEMS switches with zero insertion loss and perfect isolation, the response is not constant through the frequency as a result of the nature of the transmission line. This can be clearly seen from the phase shift performance presented in Figure 2.7.

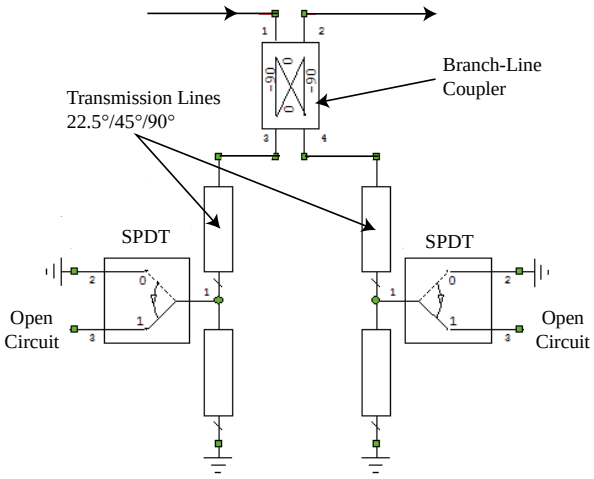


Figure 2.6. Ideal 3-bit reflect-line phase shifter design with ideal SPDT switches.

For couplers, ideal branch-line coupler with 35.4Ω and 50Ω 90°-lines are used. These transmission line are to be realized with CPW lines fabricated with same METU RF MEMS parameters as in switched-line phase shifter design in previous section. Design parameters for CPW lines are tabulated in Table 2.3.

Table 2.3. Design parameters for ideal branch-line coupler.

Parameter	W	G	L
35.4Ω	377 μm	10 μm	4481 μm
50Ω	240 μm	30 μm	4496 μm

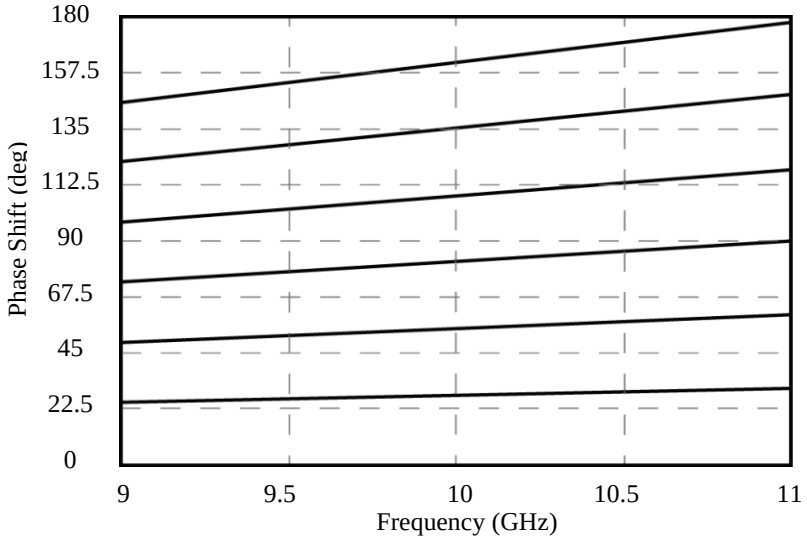


Figure 2.7. The phase shift performance of an ideal RLPS designed at 10 GHz.

2.6. Loaded-Line Phase Shifters (LLPS)

Loaded-line phase shifters work based on the idea that is to load a transmission line with two different impedances and use a midsection matching network. A concept designed with the fabrication materials is presented in Figure 2.8. The matching network ensures that the phase shifter is matched to Z_0 for both loading conditions.

The phase difference between the two different loads can be accurately controlled by the value of the loading impedances. Loaded-line phase shifters result in excellent response for small phase delays (11.25°, 22.5°, and 45°). A 90°-phase shift is not practical because the design results in a very narrowband response [7]. The bandwidth is generally defined by the frequency range where the phase shift is within ±2° from the design value and the reflection coefficient is less than -20 dB.

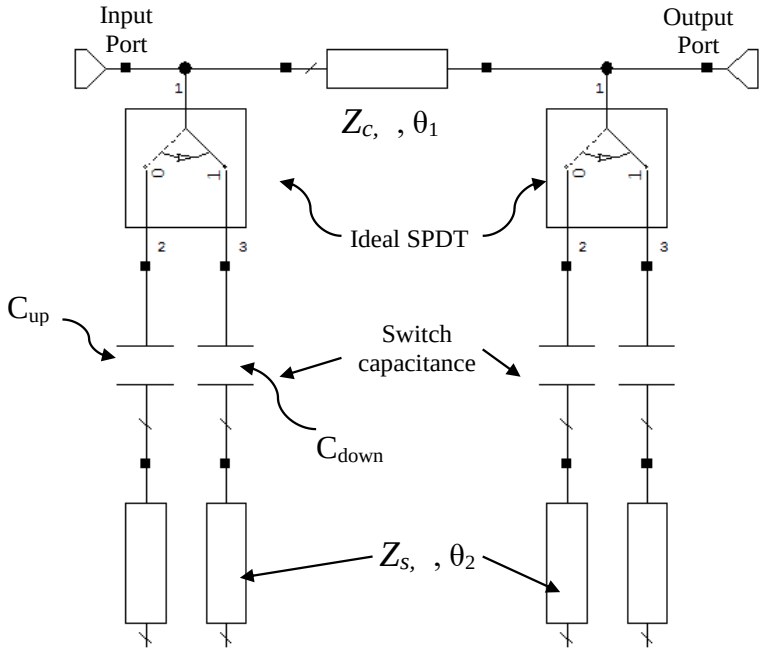


Figure 2.8. Designed loaded-line phase shifter in X-band.

Design parameters for loaded-line phase shifter are given in Table 2.4 and Table 2.5. The values are found following the same approach presented in [7].

Table 2.4. Design parameters for loaded-line phase shifter.

Parameter	**Value**	**Parameter**	**Value**
Z_c	52.4Ω	θ_1	69.5°
Z_s	30.3Ω	θ_2	18.6°
C_{up}	70.5 fF	C_{down}	1510 fF

Table 2.5. Design parameters for CPW-lines used in LLPS design.

Parameter	W	G	L
52.4Ω	200 μm	30 μm	3470 μm
30.3Ω	442 μm	5 μm	920 μm

The performance of designed LLPS is given in Figure 2.9. Since loaded-line phase shifters mostly employ DC-switches and they result in very narrow-band response for 45° and 90°. Moreover, 30.3Ω CPW line is hard to implement. Thus, this topology is not a good candidate for design satisfying error specifications.

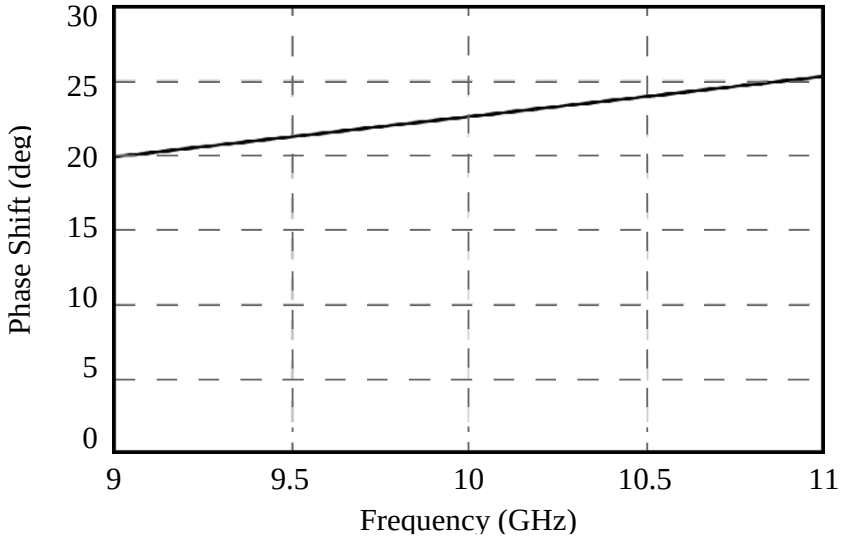
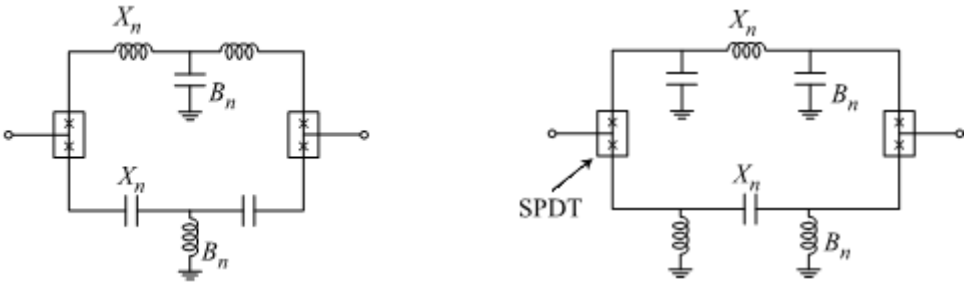


Figure 2.9. Loaded-line phase shifter to provide 22.5° designed at 10 GHz.

2.7. Switched Network (High-Pass/Low-Pass) Phase Shifters

A very common switched-network phase shifter is the low-pass/high-pass filter configuration as shown in Figure 2.10. The low-pass filter results in a phase delay while the high-pass filter results in a phase advance as one can expect. The input/output impedances of both filters are designed to be Z_0 at the design frequency. The capacitors and inductors can be implemented using lumped elements, transmission lines, or a combination of both.



(a) T-network (b) π-network

Figure 2.10. Switched filter phase shifter topologies [7].

The low-pass/high-pass filter networks are switched using SPDT (Single-Pole, Double Throw) switches. With ideal SPDT switches, a wide-band response is possible. However, although SPDT switches can be implemented with shunt MEMS switches, λ/4 lines are required to transform short circuit into open circuit. However, the capacitive, shunt, RF-MEMS switches used in SPDT insert different phases for up and down states. Thus, the phase shift between the networks deviates from the expected results. In order to observe this effects, a switched network example is designed to provide 45° at 10 GHz. The effect of phase insertion can be seen in the phase shift performance simulations given in Figure 2.11. Due to the difference in up/down state phase insertions, the phase shift deviates from 45°.

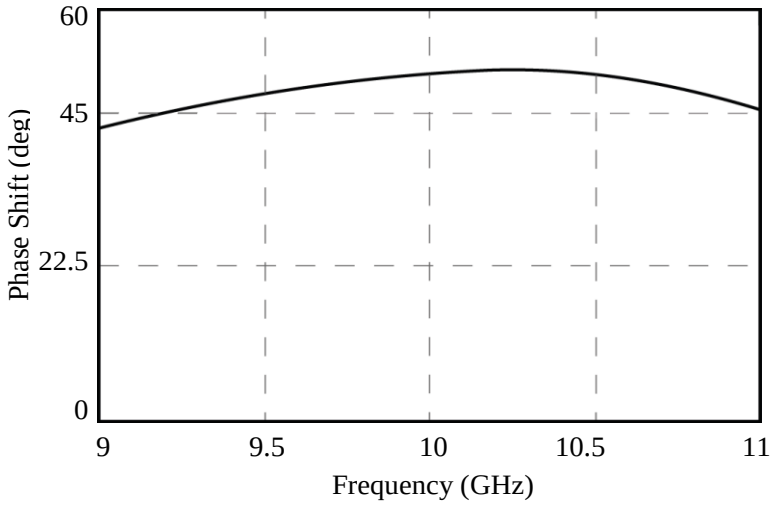


Figure 2.11. Deviation in phase shift of a switched network.

2.8. Switched Capacitor-Bank Phase Shifters

The switched capacitor-bank phase shifter design is based on a quadrature 3-dB coupler and a reflection-type phase shifter as shown in Figure 2.12. The reflection phase due to a capacitive load is given in Equation (2.1) [7]. Note that $|X_c| \ll Z_0$ is assumed.

$$\phi = \pi + 2\tan^{-1}\left(\frac{|X_c|}{Z_0}\right) \quad for\ (X_c \le 0) \tag{2.1}$$

where $X_c = -j/(w_0 C)$ and C is the bridge capacitance depending on its state.

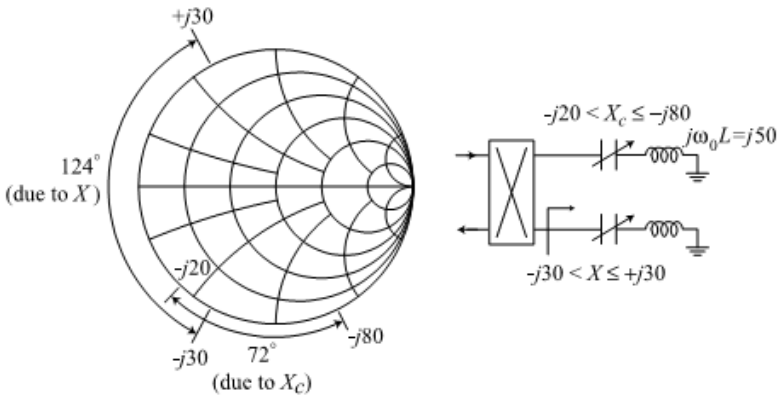


Figure 2.12. Reflection coefficient of a phase shifter and inductive tuning [7].

Here it should be noted that the bandwidth is limited by the 3-dB coupler to around $\pm$15% due to the reactive loading at the output ports. The phase shift can be increased if an inductance is placed in series with the bridge. The inductance is chosen so as to resonate with the average value of the bridge capacitance so that it spans a wider range of the reflection coefficient for the same *down-to-up capacitance ratio (DUR).*

From the forgoing analysis, the only problem with the switched capacitor-bank phase shifter seems to be the bandwidth limitation of the coupler. However, it may be solved

using several phase shifting stages in cascade. As an example, the design in [38] uses two stages cascaded to obtain a very wide-band frequency response.

2.9. Comparison and Conclusion

In previous sections, various kinds of phase shifters are reviewed and their characteristics are exemplified with ideal circuit designs. Among them, those implementing distributed systems like transmission lines usually provide linear phase shifts which changes with frequency. Although constant phase delays may be obtained employing different configuration of these systems, 3-bit operation with eight phase shift steps requires complex design in addition to very large sizes due to transmission lines which yields high fabrication cost.

In Section 2.8, switched-capacitor bank phase shifters are seen to be a potential candidate because a single variable capacitor can provide a desired phase shift at the center frequency. After a literature survey conducted on reflected-type phase shifters employing switched capacitor-banks rather than transmission lines, it has been concluded that the study in [38] has the design purposes which are most parallel to the project specifications and the idea of cascading, which is not recent, is a good starting point. Moreover, the materials and fabrication techniques used are also feasible in METU-MEMS facilities. METU RF MEMS Group has previous studies and fabricated switches which have similar capacitances and they are, indeed, more successful in terms of controllability. Thus, a reflected-type phase shifter which is consist of 3-dB couplers terminated by RF MEMS capacitor banks is selected to be studied in this thesis.

CHAPTER 3

DESIGN OF RF MEMS DIGITAL CAPACITOR BANKS

This chapter elaborates upon the first building block of the phase shifter, which is reflect terminals providing different shifts in the phase of the reflection coefficient Γ. For this purpose, single or multiple variable reactive elements, capacitors or inductors, can be employed to change the phase. If this change is properly adjusted, phase shift steps between reflection coefficients are obtained.

Using MEMS fabrication methods, variable capacitors (tunable capacitors) and capacitor-banks are fabricated and reported in the literature [34]–[39]. The capacitance of the bank can be tuned either in analog or digital manner. Analog tunable capacitors allow continuous tuneability of capacitance value, theoretically, into any value in the range. While digital tunable capacitors can provide only discrete capacitance values, they are often preferred due to their design and fabrication simplicity.

3.1. Introduction to RF MEMS Digital Capacitor Banks

Generally, digital tuneable capacitors generally employ RF MEMS switches with fixed capacitors and actuating these switches different capacitance values are obtained. In this study, however, the switch itself is a variable capacitor of which the capacitance is switched between up and down states resulting in small and large values, respectively. As shown in Figure 3.5, a RF MEMS switch has two capacitance value depending on the position of the bridge, that is, a low-capacitance, C_{up}, and a high-capacitance, C_{down}.

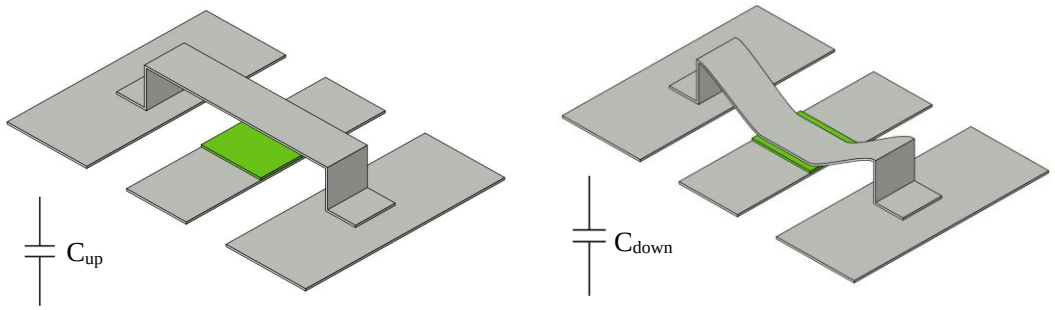


Figure 3.1. Using RF MEMS switch as variable capacitor.

The gap change is attributed to the change in the capacitance as the area remains same, theoretically, DUR (down-to-up ratio) can be calculated as follows,

$$C_{up} = \frac{\varepsilon_0 A}{(\frac{t_D}{\varepsilon_D} + g)} \tag{3.1}$$

$$C_{down} = \varepsilon_{D,eff}\varepsilon_0 \frac{A}{t_D} \tag{3.2}$$

$$DUR = \frac{C_{down}}{C_{up}} = 1 + \varepsilon_D \frac{g}{t_D} \tag{3.3}$$

where

ε_0 : The permittivity of free-space,

ε_D : Relative permittivity of dielectric layer,

$\varepsilon_{D,eff}$: Effective relative permittivity at down state

A : Area of the bridge on the signal trace,

t_D : Thickness of the dielectric layer

g : Height of the air gap.

Typical values used in METU RF MEMS process are $\varepsilon_D = 7$ and $t_D = 0.3\ \mu m$, $g = 1.2\ \mu m$ [1,7]. However as the bridge does not uniformly contact to the dielectric,

the effective relative permittivity, ε_D is degraded by a factor of 0.37 resulting in $\varepsilon_{Deff} = 2.59$ which is explained in [31] and [2]. Using typical values above, DUR is calculated as 10.73.

$$\Gamma_L = \frac{Y_0 - Y_L}{Y_0 + Y_L} \tag{3.4}$$

$$Y_L = j\omega C \tag{3.5}$$

$$\Gamma_L = \frac{Y_0 - j\omega C}{Y_0 + j\omega C} \tag{3.6}$$

$$|\Gamma_L| = 1, \qquad \angle\Gamma_L = \tan^{-1}\frac{-2Y_0\omega C}{Y_0^2 - \omega^2 C^2} \tag{3.7}$$

As shown in Equation (3.7), $\angle\Gamma_L$ is the phase of the refrection coefficient when a transmission line with Y_0 admittance is loaded with a capacitor, *C*. The phase shift θ, is equal to the difference between the phases of the reflection coefficient at initial and final states of bridges.

$$\theta = \angle\Gamma_f - \angle\Gamma_i \tag{3.8}$$

$$\theta = \tan^{-1}\frac{-2Y_0\omega C_f}{Y_0^2 - \omega^2 C_f^2} - \tan^{-1}\frac{-2Y_0\omega C_i}{Y_0^2 - \omega^2 C_i^2} \tag{3.9}$$

Using trigonometrical equality in Equation (3.10),

$$\tan^{-1}A - \tan^{-1}B = \tan^{-1}\frac{A - B}{1 + AB} \tag{3.10}$$

Equation (3.9) can be rewritten as,

$$= \tan^{-1}\left(\frac{-2Y_0\omega\left(\frac{C_f}{Y_0^2 - \omega^2 C_f^2} - \frac{C_i}{Y_0^2 - \omega^2 C_i^2}\right)}{1 + \frac{4Y_0^2\omega^2 C_f C_i}{(Y_0^2 - \omega^2 C_f^2)(Y_0^2 - \omega^2 C_i^2)}}\right) \tag{3.11}$$

Equation (3.11) shows that phase shift heavily depends on the frequency. However, according to the project specifications given in previous sections, constant phase shift steps are also desired.

For a single phase shift step, these two requirements, $\theta \; and \frac{\theta}{d\omega} = 0,$ can be simultaneously satisfied by choosing *DUR*, a fabrication parameter, and the up-state capacitance C_u. Nevertheless, for *N* phase steps *2N* requirements are to be satisfied over 9-11 GHz. For different phase steps, required increase in total capacitance values may be obtained with different combinations of bridge position. That is, by cascading the bridges one and after, capacitances become in parallel combination as shown in Figure 3.2.

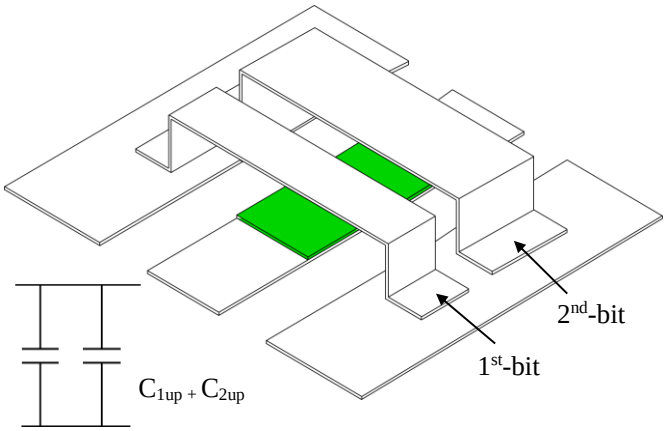


Figure 3.2. RF MEMS Variable capacitors with multiple bridges.

In Figure 3.2, two bridge is cascaded as an example. The number of bridges can be increased depending of the number of bits and phase step sizes. However, as the number of bits increased, it becomes harder to find the capacitance values which gives accurate and constant phase shift over a wide bandwidth. The reason for that is although one can choose the upstate capacitances of bridges, the height of the bridges and so *DUR* has to be chosen a single value due to the process limitations. Moreover,

the phase shift-capacitance relation calculated for *DUR*=10 at 10 GHz shown in Figure 3.3 is not linear and the change in the phase shift decreases at higher bits.

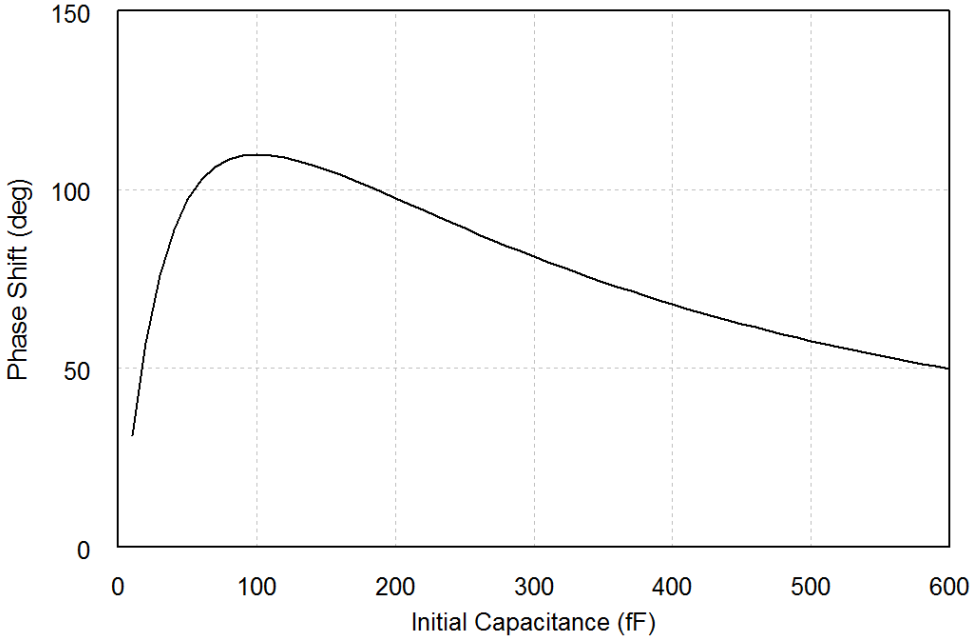


Figure 3.3. Phase Shift vs. Initial Capacitance.

3.2. Design of 2-Bit Capacitor Banks

After reviewing RF MEMS switches as variable capacitors, three alternative designs are presented in this section.

3.2.1. Design-1: Identical Sub-capacitors

In order to satisfy the design specifications, the operation should be 3-bit. This can be satisfied by cascading two stages which individually employ four sub-capacitors. Firstly, one can investigate the effect of non-linearity in Figure 3.3 by trying identical sub-capacitors. In Figure 3.4, a capacitor formed by an RF MEMS bridge is divided into four capacitors and $C_{11} = C_{12} = C_{13} = C_{14} = C_u$ is choosen.

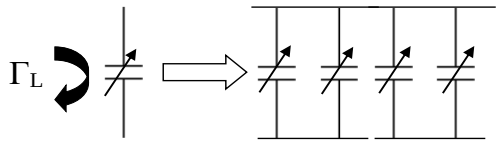


Figure 3.4. RF MEMS Variable Capacitor Bank.

As previously mentioned, $\theta \; and \frac{d\theta}{d\omega} = 0$, can be satisfied for a single phase step, θ, by tuning C_u and *DUR.* The phase shift in reflection coefficient is optimized for 90° when all four bridges are pulled down providing $4C_d$. After optimization, $C_u = 34.4\, fF \; and \; DUR = 5.84$ are found.

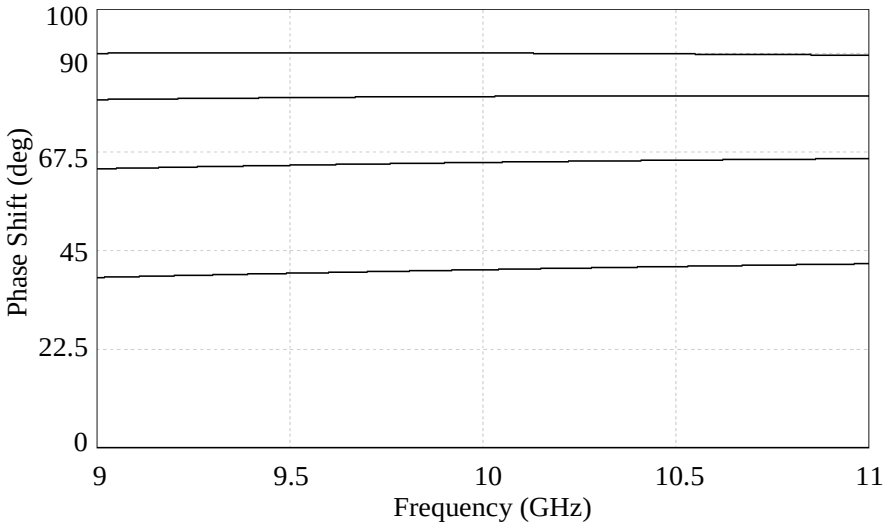


Figure 3.5. Phase shift steps over frequency with identical sub-capacitors, C_u.

The corresponding results are shown in Figure 3.5. Pulling down all bridges, *i.e.* state 11, results in 90° however actuating them one by one does not provide 22.5° as the increase in capacitance is not linear as shown in Table 3.1. If all phase steps are set as a goal in the optimization, it stacks with inaccurate results since the number of variables is not enough to find a solution.

In Design-1, the airgap height is calculated as 0.56 μm. The minimum capacitance needed is $C_u = 34.4\ fF$ which corresponds to bridge widths of 25.9 μm over 100μm-width signal trace. Although narrow bridges require a meticulous microfabrication, it is still in the limits of METU RF MEMS microfabrication standards.

Table 3.1. Position of the bridges and capacitance provided in Design-1.

State	**B1**	**B2**	**B3**	**B4**	**Capacitance (fF)**	**Ratio**	**Phase Shift (°)**
00	Up	Up	Up	Up	137.6	1.00	Reference
01	**Down**	Up	Up	Up	304.3	2.21	40.6
10	**Down**	**Down**	Up	Up	470.9	3.42	65.1
11	**Down**	**Down**	**Down**	Up	637.5	4.63	80.1
100	**Down**	**Down**	**Down**	**Down**	804.1	5.84	90

3.2.2. Design-2: Different Sub-capacitors

In order to find a results satisfying all phase step requirements, each capacitor in Figure 3.2 is defined as a separate variable: $C_{11},\ C_{12},\ C_{13},\ C_{14}$ and *DUR* is set as 10.73 corresponding to typical height of airgap, 1.2 μm. Then eight optimization goals, *i.e.* $\theta\ and\ \frac{d\theta}{d\omega} = 0$ for each phase step, are defined. The optimization results are listed in Table 3.2 where down-state capacitors are written in bold and corresponding phase shift is drawn in Figure 3.6. Although peak-to-peak phase error is large as 9.6°, this design still satisfies the project specifications.

Table 3.2. Optimized Capacitance values in Design-2.

State	C_1 (fF)	C_2 (fF)	C_3 (fF)	C_4 (fF)	Peak Error (°)	Phase Shift (°) At 10 GHz
00	12.0	19.3	41.0	182.6	-	Reference
01	**136.3**	19.3	41.0	182.6	0.1	22.5
10	**136.3**	**219.2**	41.0	182.6	0.8	45.1
11	**136.3**	**219.2**	**465.8**	182.6	2.3	67.5
100	**136.3**	**219.2**	**465.8**	**2074.3**	4.5	90.1

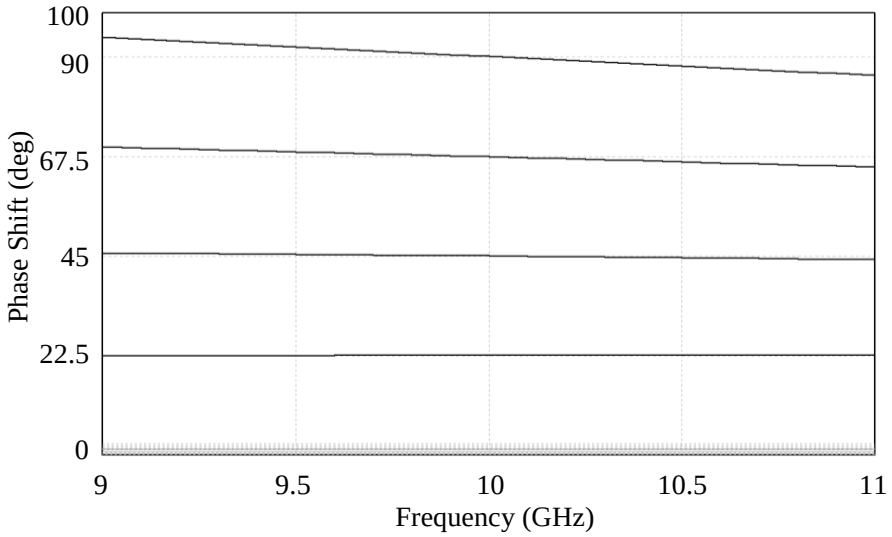


Figure 3.6. Phase shift steps with different sub-capacitors.

Design-2 employs a minimum capacitance of $C_{1u} = 12\ fF$. This capacitance value requires a bridge width of 17.8 µm placed over a signal trace which has a width of 100 µm. Due to fabrication limits, the bridge may not be precisely fabricated as it is narrower than 20 µm. Moreover, the parallel plate area is as small as 17800 μm^2 which requires a high pull-in voltage which is not desired.

3.2.3. Design-3: Different Sub-capacitors and a Fixed Capacitor

In order to overcome fabrication complexity in Design-2, alternative capacitor bank is designed in Figure 3.7. In this design, one of the RF MEMS capacitors is turned into a fixed, Metal-Insulator-Metal capacitor (MIM). Three bridges are used to provide 2-bit operation.

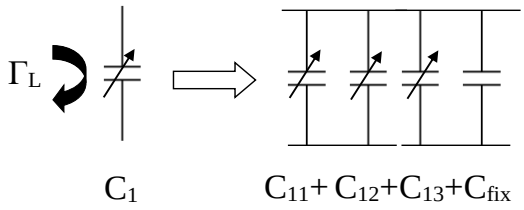


Figure 3.7. RF MEMS variable capacitor bank with a fixed capacitor.

In this design, the state definitions are changed as in Table 3.3. Unlike the previous designs, pulling down of each bridge corresponds to different states providing an extra 22.5° phase shift and when all bridges are collapsed 90° phase shift is obtained. MIM-bridge provides a fixed capacitance in all states which leads a decrease in *DUR* and linearization of phase shift over the frequency band between 9 and 11 GHz.

Table 3.3. Actuation states of the bridges in Design-3.

Actuated Bridge	State	Phase Shift at 10 GHz
MIM	000	0°
MIM, 1st Bridge	001	22.5°
MIM, 2nd Bridge	010	45°
MIM, 3rd Bridge	100	67.5°
MIM, All 3 Bridges	111	90°

In Table 3.4, optimized capacitor values are tabulated. There are accuracy errors in each state, however, it is still within the specification limits with enough margins.

Table 3.4. Optimized Capacitance values in Design-3.

C_1 (fF)	**C_2 (fF)**	**C_3 (fF)**	**C_{fix} (fF)**	**Peak Error (°)**	**Phase Shift (°) At 10 GHz**
8.3	19.1	35.7	63.7	-	Reference
88.7	19.1	35.7	63.7	0.8	22.6
8.3	204.6	35.7	63.7	1.7	45.1
8.3	19.1	382.8	63.7	1.4	68.2
88.7	204.6	382.8	63.7	0.5	89.5

Looking into phase shift response given Figure 3.8, the peak error in the first stage is 0.8°. This error is in the limits of design specifications which is defined as 1.8°. The letters on the graph Figure 3.8 indicate the actuation of the bridges, *e.g.* UDU means only the second bridge is collapsed.

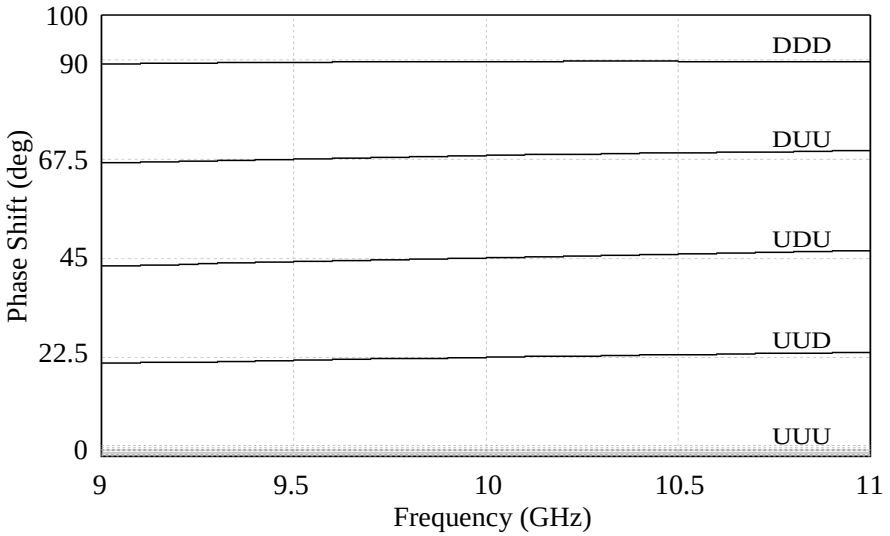


Figure 3.8. Phase shift response of MEMS capacitors and a fix capacitor.

In Design-3, C_1 is the smallest capacitor and has a capacitance of 8.3 fF when it is not actuated. This requires 11.6 μm bridge width over 100 μm signal trace. However, as 11.6 μm may not be precisely fabricated, bridge width of 23.2 μm over 50 μm signal trace should be preferred. Still, small parallel plate area of 11600 μm^2 may result in a high pull-in voltage [2].

3.3. Design of Most Significant Bit (MSB)

This section investigates the design of MSB which is responsible for an additional 90° phase shift. When this capacitor is cascaded with the capacitor bank designed in Section 3.2, the overall system will be able to provide phase shifts between 90° and 180°. For realization of this bit, two designs are proposed.

3.3.1. Cascading a MSB Capacitor with Design-2

MSB capacitor can be realized with a single RF MEMS capacitor shown in Figure 3.1. Using $\frac{C_{down}}{C_{up}} = DUR = 10.73$ and Equations 4.9-4.11, $C_{MSBu} = 34.9\ fF$ is found. The phase shift in the reflection coefficient due to this capacitor is given in Figure 3.9. The phase error is 4.3° at 9 and 11 GHz. Note that the slope of phase shift is positive in contrast to the response of Design-2 as seen in Figure 3.6.

For realization of MSB capacitor of 34.9 fF, 51.8 μm bridge over 100 μm signal trace can be used. As it has relatively high capacitance, it is easier to fabricate and pull down by electrostatic force.

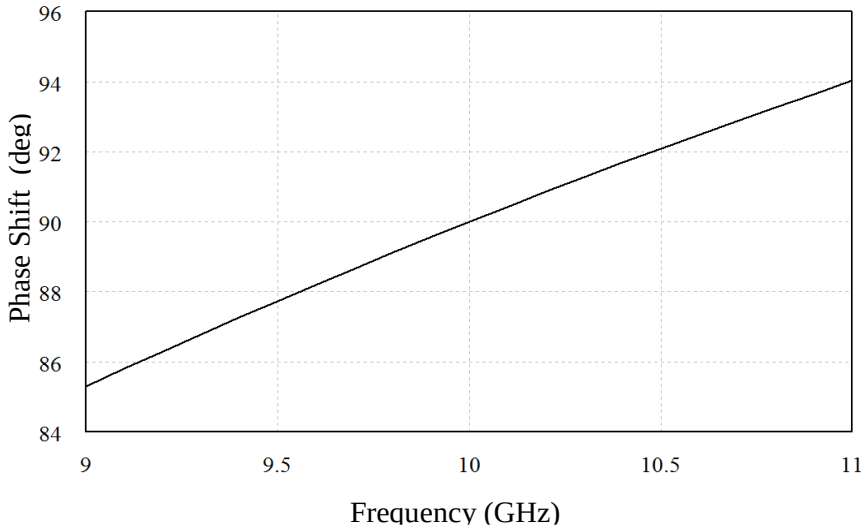


Figure 3.9. Phase shift in the reflection coefficient of MSB capacitor.

The sum of the phase shifts in the reflection coefficients of digital capacitor bank and MSB capacitor is given in Figure 3.10. As seen, the slopes of phase shifts due to capacitor bank and MSB capacitor cancels each other and provides flat response. The maximum peak error is 4.5° in 90° and 112.5° phase step which is still in the error limits of the project defined as ±8%. The phase errors almost completely cancels each other in 180°.

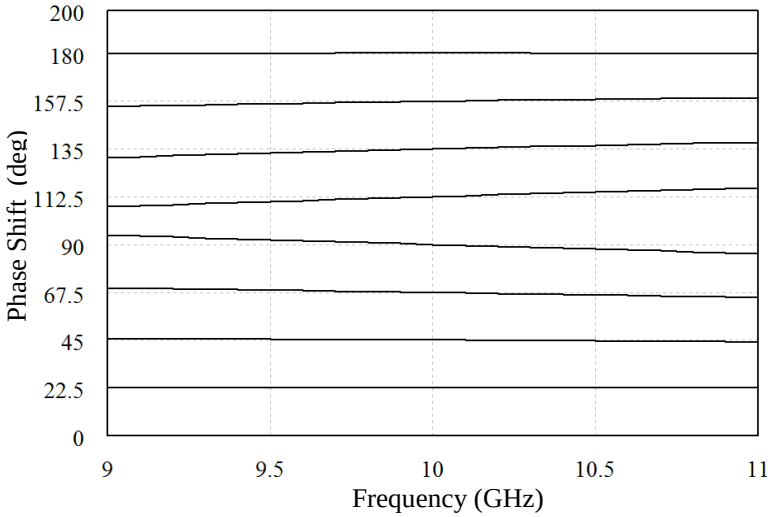


Figure 3.10. Sum of the phase shifts due to capacitor bank and MSB capacitor.

3.3.2. Cascading Two Identical Capacitor Banks in Design-3

An alternative way of realizing MSB is cascading two identical capacitor banks given in Design-3. This is because Design-3 is very successful in providing 90° phase shift as shown in Figure 3.8. In Figure 3.11, the total phase shift in the reflection coefficients of capacitor banks are given.

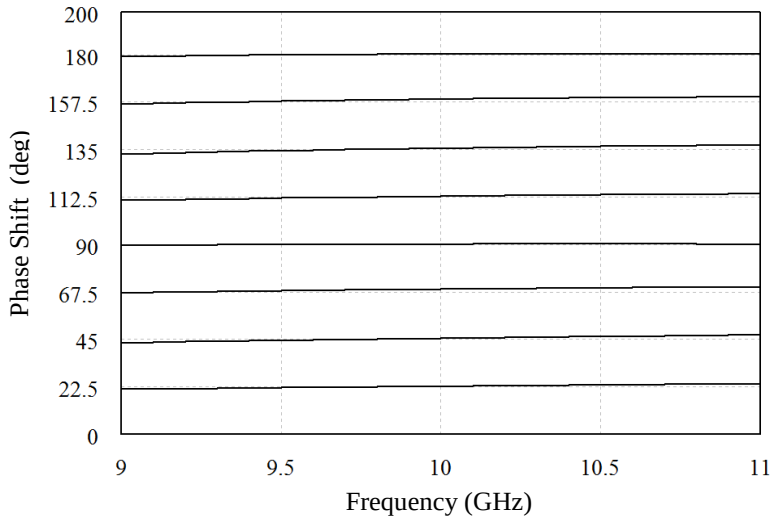


Figure 3.11. The total phase shift when two capacitor banks are cascaded.

The maximum accuracy error of 1.25° occurs in 67.5° phase step as expected from Table 3.4. Nevertheless, this error is close but within the limits of ±2% accuracy specification. Note that this phase step, however, can also be realized when 22.5° and 45° phase steps are provided separately. In this case, total accuracy error is smaller than 0.7°. This is one of the main advantage of cascading two capacitor banks.

3.3.1. Comparison of Designed Capacitor Banks

In Section 3.2, three design examples are presented. In Design-1, equal capacitors are used and these capacitances are optimized for 90°. However, it is failed to provide 22.5° in each bit. Thus, it is not an even proper candidate for the project.

Design-2 employs four different capacitors and it is quite successful in providing desired phase shifts when the bridges are collapsed one after another. For its disadvantages, it requires a narrow bridge for the smallest capacitor and the largest capacitor is too large which may have to be realized with two sub-capacitors.

In Design-3, a fixed capacitor replaces one of the bridges and the operation states are realized by collapsing each bridge separately. As an advantage, the number of actuation paths will be one less. In addition, each bridge is separately actuated and the errors due to non-uniform capacitive contact will not be cumulated. On the other hand, it employs a very small capacitance of 8.3 fF which is hard to fabricate and pull down.

Note that 3-bit operation to provide 180° phase shift is provided by MSB designs in Section 3.3. Comparing Figure 3.10 and Figure 3.11, both designs satisfy the specifications but cascading two identical capacitor banks with a fixed capacitor results in a better performance. Moreover, design of a single stage compromising a coupler and a capacitor bank will be enough as the cascaded stages are identical. Together with the advantages of Design-3, cascading two capacitor banks is a better approach.

3.4. Modelling and Simulations of RF MEMS Capacitor Banks

After deciding the capacitor bank and MSB circuits, RF MEMS structures are designed and simulated in this section. Using Equations 4.1-4.3, the bridge widths can be calculated for each capacitor. Utilizing the advantage of employing identical capacitor banks for both lower bits and MSB, designing and optimizing RF MEMS structures once will be sufficient. In Table 3.5, calculated widths of the ideal bridges are given. Note that these values are estimated assuming ideal capacitors. However, a bridge resistance and an inductance will accompany the capacitance created.

Table 3.5. Capacitance values and calculated bridge widths for Design-3.

State	**C_1**	**C_2**	**C_3**	**C_{fix}**
C_{up} (fF)	8.3	19.1	35.7	63.7
W_b (μm)	24.7	56.7	106.0	17.6

In Figure 3.12 and Figure 3.13 electromagnetic (EM) models of the capacitor bank designed in Section 3.2.3 are given. For the sake of simplicity, glass substrate is not shown. Yellow regions represent gold plates forming co-planar waveguide (CPW) structure. Five bridges are placed on the CPW and three of them are connected to bias lines. As the fixed capacitor was implemented in air-bridge, it would require a wide bridge, which would have very low spring constant. Thus, it is realized as MIM-capacitor. Other design parameters are listed in Table 3.6.

Table 3.6. Model parameters for Design-3.

Explanation	**Parameter**	**Value**
Width of signal of transmission line	W0	115 μm
Width of gap of transmission line	G0	10
Width of signal under bridges	W	50 μm
Width of gap under bridges	G	50 μm
Height of airgap	Hbrid	1.2 um
Thickness of dielectric layer	t_d	0.3 um
Relative permittivity of dielectric layer	ε_d	7
Effective permittivity of dielectric layer	$\varepsilon_{d,eff}$	2.59
Relative permittivity of substrate	ε_{subs}	4.6

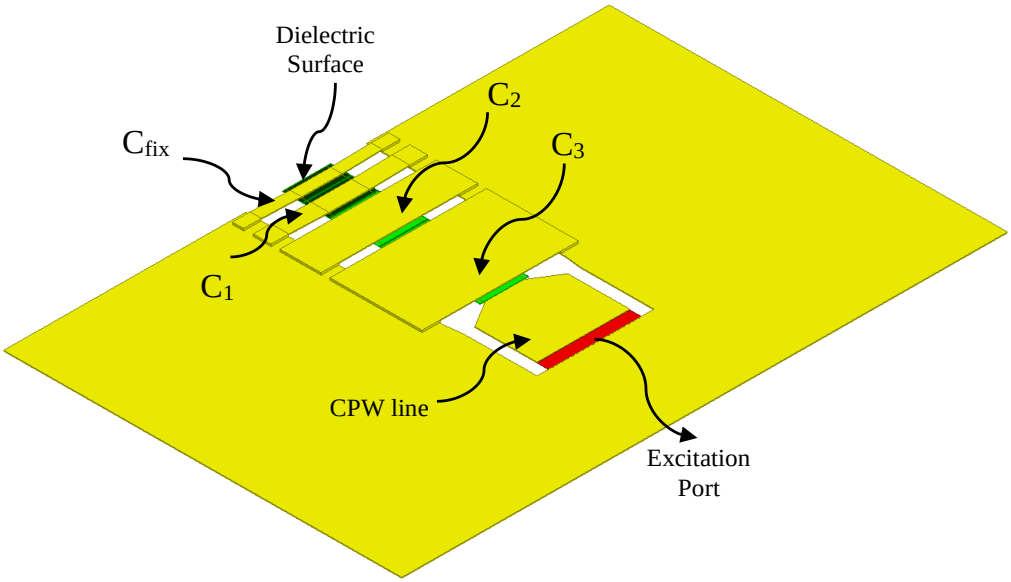


Figure 3.12. 3D-view of EM model of the capacitor banks in Design-3.

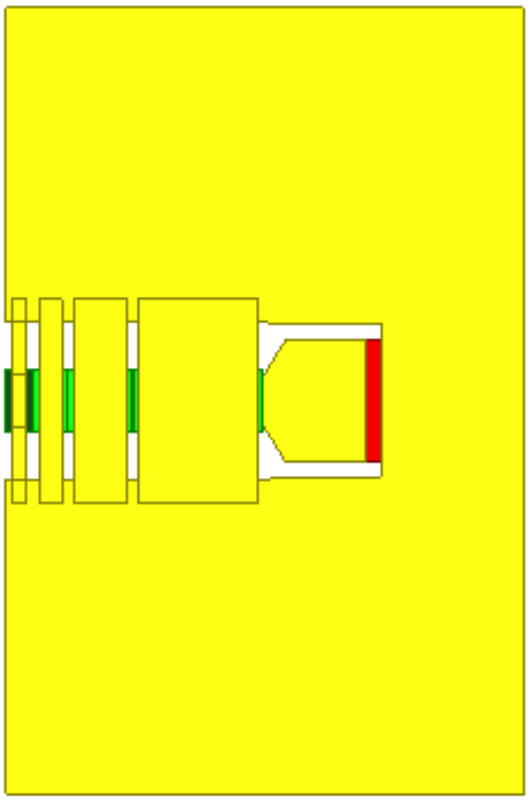
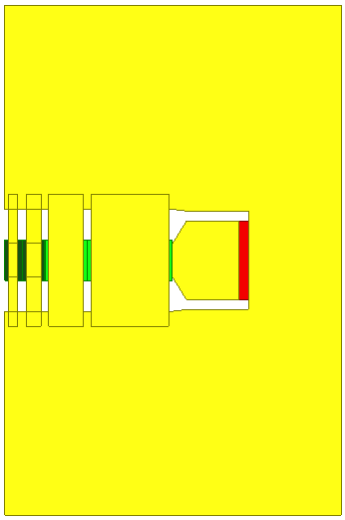
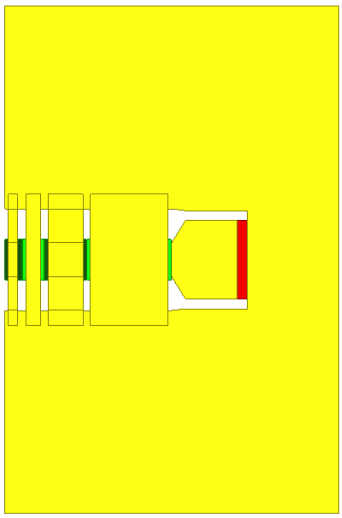


Figure 3.13. Top view of capacitor bank at reference state.

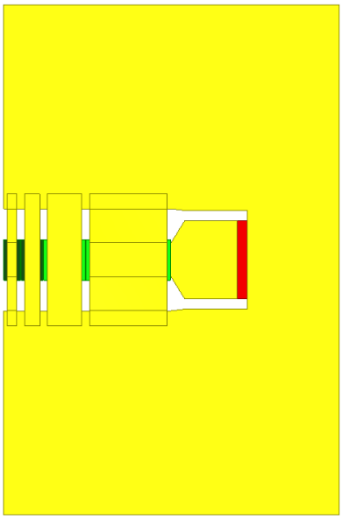
In order to realize the operation principle given in Table 3.3, bridges are configured as in Figure 3.14 and they provide a phase shift in the reflection coefficient seen by the excitation port with respect to that of the reference state at which all the bridges are up as shown in Figure 3.13. Note that the dielectric layers under bridges which are pulled-down are defined and colored differently as their effective permittivity decreases by a factor of 0.37 due to non-uniform capacitive contact.



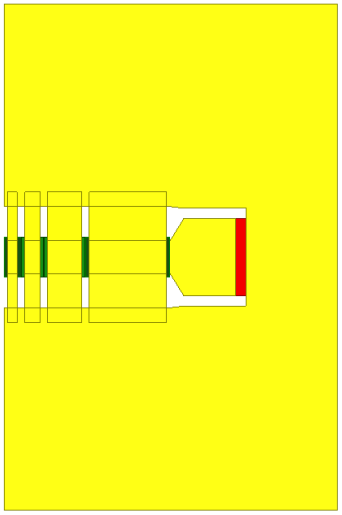
(a) 22.5° phase step



(b) 45° phase step



(c) 67.5° phase step



(d) 90° phase step

Figure 3.14. Operation principle and bridge states of capacitor bank.

After simulating EM model with ideal bridge widths given in Table 3.5, an optimization for non-ideal capacitors is performed in EM simulator. Down-to-up capacitance ratio (*DUR)* is calculated as 10.4 which is degraded by a factor of 0.96 due to parasitic bridge resistance and inductance. Optimized parameters resulting in best performance are listed in Table 3.7.

Table 3.7. Optimized bridge widths for non-ideal capacitors.

State	**C_1**	**C_2**	**C_3**	**C_{fix}**
C_{up} (fF)	6.63	15.3	29.5	74.73
W_b (μm)	21.3	51.5	109.6	15.3

Simulation results of EM model of the optimized capacitor bank is given in Figure 3.15. They are also consistent with the circuit design results of Design-3 given in Figure 3.8.

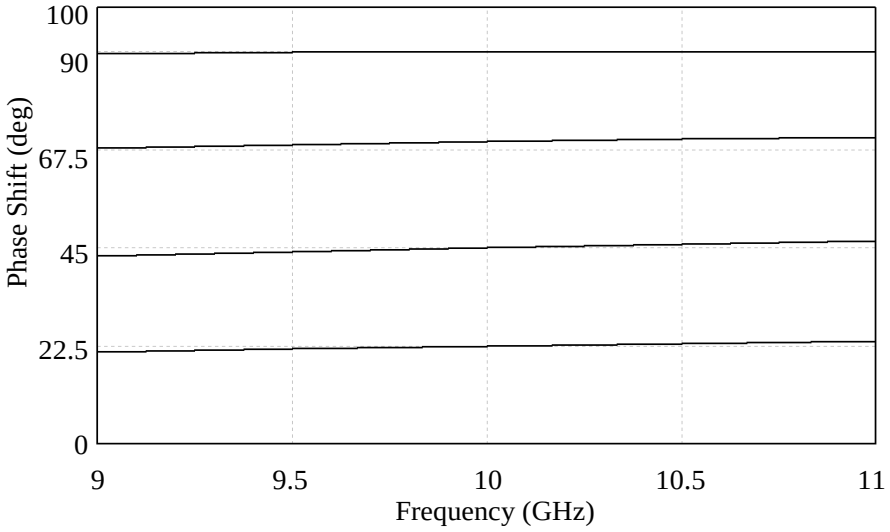


Figure 3.15. Phase shift performance of 3D EM capacitor bank model.

The phase errors of simulated model are listed in Table 3.8 and simulation results indicate that capacitor bank is quite successful in providing required reflection phase

delays. However, the capacitor bank has an accuracy error of 2.7% (written in bold) at 67.5° phase step, which violates 2% maximum accuracy error specification. Fortunately, this phase step can also be obtained as 22.5°+45° when two stage is cascaded. Moreover, another optimization after integration can also be conducted if needed.

Table 3.8. Phase errors of simulated EM model of Design-3.

Phase Step	**9 GHz**	**10 GHz**	**11 GHz**	**Accuracy Error**	**Peak Error**
22.5°	21.08°	22.44°	23.60°	-0.3%	4.9%
45°	43.00°	44.97°	46.50°	-0.1%	3.3%
67.5°	67.71°	69.32°	70.31°	**2.7%**	4.2%
22.5°+45°	64.08	67.41	70.1	-0.1%	3.9%
90°	89.42°	89.90°	89.79°	-0.1%	-0.2%

According to simulation results in Table 3.8, 2-bit operation with low accuracy and peak errors is obtained. When two stages consisting of the capacitor bank and ideal coupler are cascaded, design specification will also be satisfied for greater phase steps since Design-3 proposes very successful 90°-phase shift as most significant bit. Note that this is the most important advantage of Design-3 mentioned in previous section. The errors due to the non-idealities of the coupler will be investigated in next chapter.

3.5. Mechanical Parameters of RF MEMS Capacitor Banks

The spring constant and the pull-in voltage are the most important mechanical parameters for MEMS bridges which significantly affects the phase shifter performance. Thus, it is valuable to calculate these parameters. For this mechanical analysis parts, the parameters which are specific to the fabrication process are obtained

from [1]. Using Equation 3.12-3.10 [39], spring constants, normalized pull-in deflections and pull-in voltages of all bridges are found and given in Table 3.9.

$$k_{linear} = 32W_b\zeta E\ \frac{1}{\left(\frac{L}{t}\right)^3} + \frac{48}{5}\frac{\sigma}{\left(\frac{L}{t}\right)} \tag{3.13}$$

$$k_{quad} = \frac{4096}{175}W_b\zeta\frac{E}{\left(\frac{L}{t}\right)^3 t^2}, \tag{3.14}$$

$$\zeta \triangleq \frac{1}{\alpha^3-2\alpha^2+2}, \alpha \triangleq \frac{\mathrm{W}}{\mathrm{L}} \tag{3.15}$$

where σ is the residual stress, W is the width of the signal line, and L and t represent the length and total thickness of the bridge, respectively.

The normalized pull-in deflection is found using Equation 3.16.

$$\begin{aligned} y_{npi} = &\left(5\sqrt{\beta^2\eta^4 - 2\beta\eta^2 + 5} + \sqrt{\beta}(\beta\eta^3 + 5\eta)\right)^{\frac{2}{3}} \\ &+ \sqrt{\beta}\eta\left(5\sqrt{\beta^2\eta^4 - 2\beta\eta^2 + 5} + \sqrt{\beta}(\beta\eta^3 + 5\eta)\right)^{\frac{1}{3}} \\ &+ \frac{\beta\eta^2 - 5}{\left(5\sqrt{\beta^2\eta^4 - 2\beta\eta^2 + 5} + \sqrt{\beta}(\beta\eta^3 + 5\eta)\right)^{\frac{1}{3}}} \end{aligned} \tag{3.17}$$

$$v_{npi} = \sqrt{\beta y_{npi}^3 + y_{npi}}\ (\eta - y_{npi}) \tag{3.18}$$

$$V_{PI} = v_{npi}\sqrt{\frac{2g^3k_{linear}}{wW\varepsilon_0}}$$

$$\eta \triangleq 1 + \frac{t_D}{g\varepsilon_D}, \beta \triangleq g^2 \frac{k_{linear}}{k_{quad}}, \tag{3.19}$$

Table 3.9. Mechanical parameters of the bridges

W_b(µm)	L(µm)	W (µm)	k_{linear} (N/m)	k_{quad} (N/m)	y_{npi}	V_{PI} (V)
24.7	194	50	93.96	6.71	0.35	53.97
56.7	194	50	215.7	15.40	0.35	53.97
106.0	194	50	403.24	28.79	0.35	53.97

Table 3.9 presents the mechanical parameters for the bridges. As seen, the normalized pull-in deflections and voltages are the same for all bridges. This is not surprising because Equation 3.20-3.10 do not contain W_b term. This is also expected since both spring constant and electrostatic force depend on W_b which cancels each other at the equilibrium state [31]. The pull-in voltages are 53.97 Volts for all bridges which can be a high voltage for driving circuit which makes the digital operation more difficult. Fortunately, the bridge lengths do not affect the capacitance values provided by them and using longer bridges with 300 µm would result in a pull-in voltages below 30 Volts without significant degradations in the phase shifter performance.

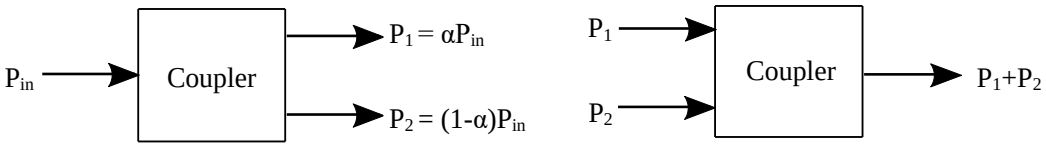
CHAPTER 4

DESIGN OF QUADRATURE HYBRID COUPLER

This chapter establishes four different types of coupler designs and compares their coupling performances. In previous chapter, RF MEMS capacitor banks are designed with an approach to minimize phase errors assuming the couplers are ideal which means they have no contribution to overall phase error. In reality, however, the couplers should be very carefully designed in terms of both power imbalance and phase difference between coupled and thru ports. Thus, this chapter is reserved for a brief review of couplers, and various coupler designs.

4.1. Introduction to Couplers

Power dividers and directional couplers are passive microwave components. They can be used for power division or power combining as shown in Figure 4.1.



(a) Power division with a ratio of α. (b) Power combining.

Figure 4.1. Configurations of couplers.

When used for power division, an input signal is divided into two or more output signals. On the other hand, a power combiner configuration of coupler accepts two or more input signals and combines them at the output signal of more power.

A coupler which has three or more ports is ideally lossless. Indeed, three-port networks are in the form of T-junctions and power dividers while four-port networks take the form of directional couplers and hybrids. Directional couplers can provide arbitrary power division and hybrids have usually equal power division (3 dB) with a 90° or a 180° phase difference.

A general s-matrix of a directional coupler is given in Equation (4.1).

$$S = \begin{bmatrix} 0 & 0 & T & C \\ 0 & 0 & C & T \\ T & C & 0 & 0 \\ C & T & 0 & 0 \end{bmatrix} \tag{4.1}$$

In this matrix, T is the transmission term found by

$$T = -j * (L_X * \sqrt{1 - C_F^2}) \tag{4.2}$$

and C is the coupling term given by

$$C = L_X * C_F \tag{4.3}$$

where

$$L_X = 10^{-\frac{|\alpha|}{20}}, \qquad C_F = 10^{-\frac{|\gamma|}{20}} \tag{4.4}$$

and α corresponds to the excess loss, which is ideally zero, and γ is the coupling ratio in dB.

Then a lossless, quadrature hybrid has the following parameters, $\alpha = 0, \gamma = 3, L_X = 1, C_F = \sqrt{0.5},\ T = -j\sqrt{0.5}\ and\ C = \sqrt{0.5}$ resulting in the following matrix,

$$S_Q = \begin{bmatrix} 0 & 0 & -j\sqrt{0.5} & \sqrt{0.5} \\ 0 & 0 & \sqrt{0.5} & -j\sqrt{0.5} \\ -j\sqrt{0.5} & \sqrt{0.5} & 0 & 0 \\ \sqrt{0.5} & -j\sqrt{0.5} & 0 & 0 \end{bmatrix} \tag{4.5}$$

As seen from S_Q matrix given in Equation (4.5), an input power incident at the port 1 is equally divided into port 3 and port 4 with a 90° phase difference.

4.2. Coupler Specifications

In this thesis, 3dB-coupler is employed to divide the input power with a 90° phase difference, which can also be called as "quadrature hybrid". As a constant-phase operation over the frequency band is aimed, it is the most important that the coupler operates in a wideband which lies between 9 GHz and 11 GHz.

The input and output ports of the phase shifter will be co-planar waveguide (CPW). Thus, the transmission lines are better to be CPW-based so that there is no need for microstrip-to-CPW transition which may limit the bandwidth. As indicated in the design specifications, high phase accuracy (±2%) and peak phase error (±8%) in the frequency band is aimed. The coupler, of course, is also an error source that should be carefully designed. At this point, main goal is to divide input power equally with 90° phase difference, although it can be lossy and the power level drops more than 3 dB. On the other hand, there is no size limitation, power handling and insertion loss are free parameters which enables satisfying accuracy specifications. The coupler specifications to be satisfied in the frequency band are listed in Table 4.1.

Table 4.1. 3dB-coupler specifications to be designed in this thesis.

Specification	Value
Power Division Imbalance	< 0.5 dB
Phase Difference Error	270°±1°
Input/Output Port Type	CPW

4.3. Design of Wideband Quadrature Hybrids as 3-dB Coupler

4.3.1. Branch-Line Coupler (BLC)

Branch-line coupler (BLC) is a fundamental component in planar microwave-integrated circuit that has many applications in devices including phase shifters, vector modulators, amplifiers, and mixers. Its prior features such as compact size and high-performance which are highly desired in many communication systems [40].

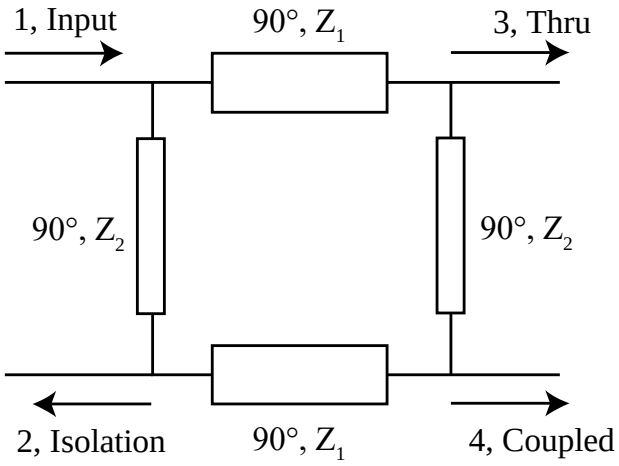


Figure 4.2. Schematics of an ideal branch-line coupler.

A typical ideal branch-line coupler design is given in Figure 4.2. It is comprised of four quarter-wave length transmission line (TL) at the center frequency and two of them have Z_0 characteristic impedance while the others have $Z_0/\sqrt{2}$. Here, $Z_2 = Z_0 = 50\Omega$ and $Z_1 = \frac{50}{\sqrt{2}}\Omega$ are chosen.

Considering that all ports are matched to 50Ω, the scattering matrix of an ideal BLC is given in matrix (4.6):

$$S_Q = \begin{bmatrix} 0 & 0 & -j1\sqrt{2} & -1\sqrt{2} \\ 0 & 0 & -1\sqrt{2} & -j1\sqrt{2} \\ -j1\sqrt{2} & -1\sqrt{2} & 0 & 0 \\ -1\sqrt{2} & -j1\sqrt{2} & 0 & 0 \end{bmatrix} \quad (4.6)$$

From above scattering matrix, it can be said that the input power is evenly divided between ports 3 and 4 with a 90° phase shift. No power is transmitted to port 2, which is named as *isolated port*. The directivity is ideally infinity at the center frequency.

The response of an ideal BLC designed at the center frequency of 10 GHz is presented in Figure 4.3 and Figure 4.4. The graph shows the input power is divided into two output ports, thru and couple, with an equal 3dB split at the center frequency. In Figure 4.3, the loss from input to the couple port is around 3 dB (dashed line) in the frequency band, however that of thru port (solid line) increases to 3.6 dB.

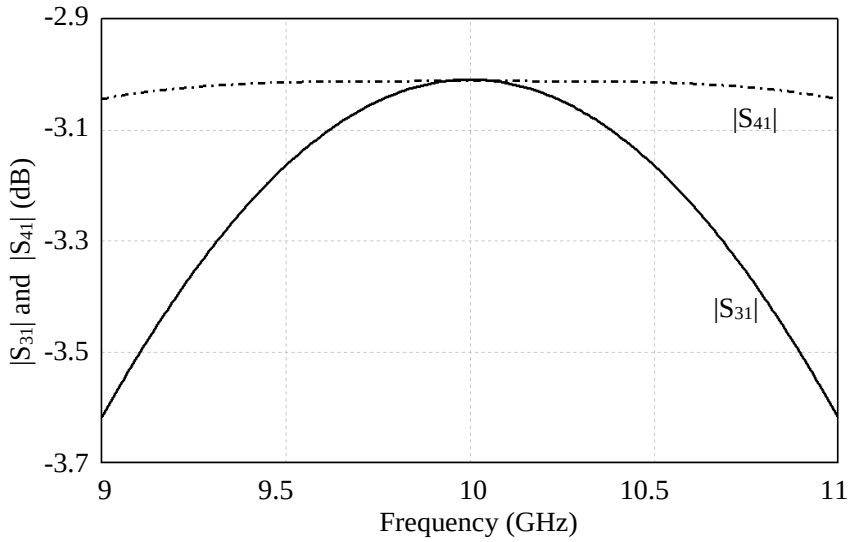


Figure 4.3. The power division performance of ideal BLC between 9-11 GHz.

As presented in Figure 4.4, both return loss and isolation are better than 14 dB in the frequency band between 9 and 11 GHz. The maximum phase shift error is 1.2° between 9 and 11 GHz. These results, even in ideal case, do not satisfy the coupler specifications listed in Table 4.1.

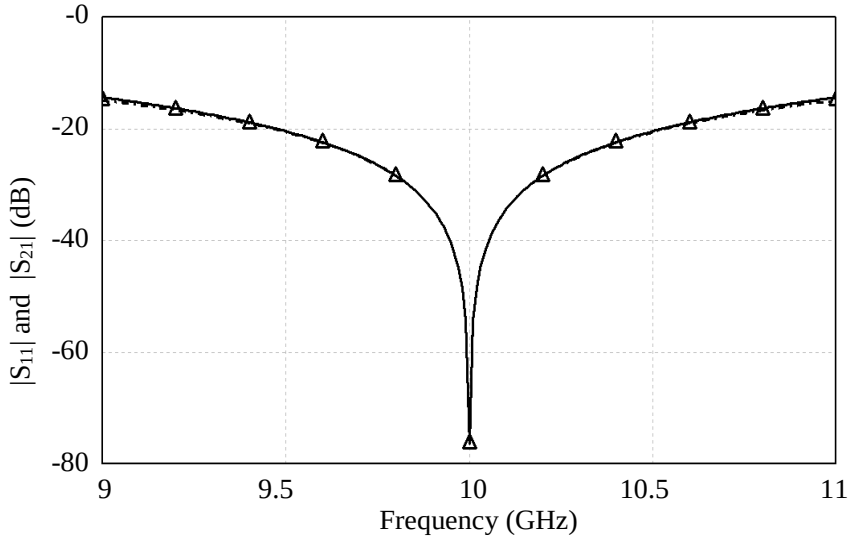


Figure 4.4. The return loss (solid line) and isolation (triangles) of ideal BLC.

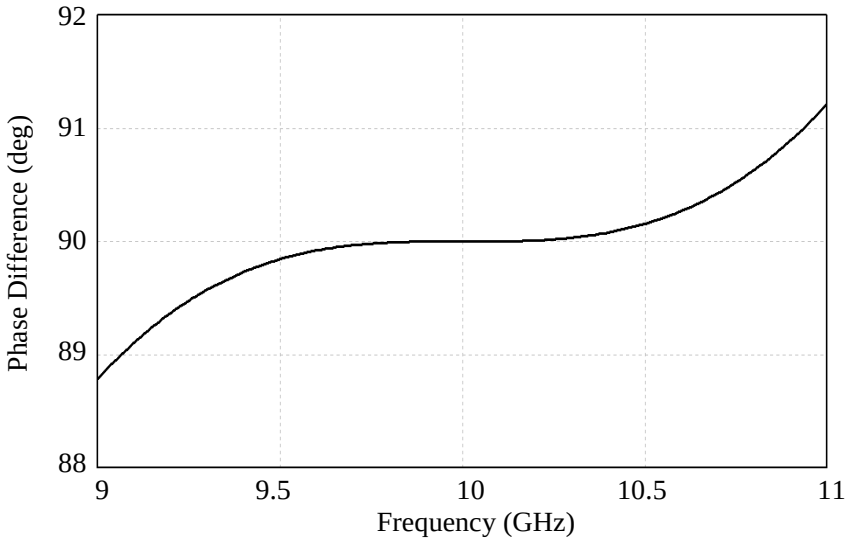


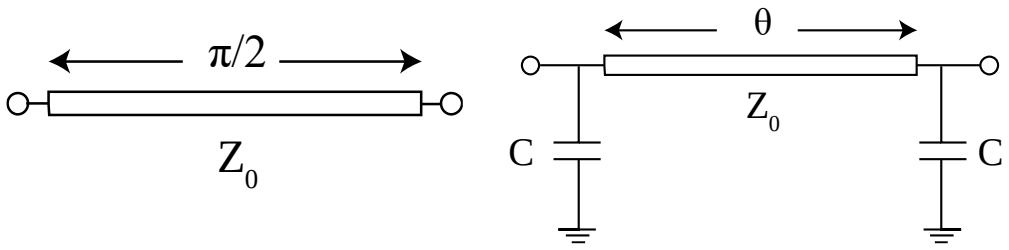
Figure 4.5. The phase difference between thru and couple ports of ideal BLC.

Here, it is important to note that as seen in Figure 4.5, BLC is a phase error source. First, the aim is to reduce the phase error by broadening the bandwidth. However, the reflective terminals will also introduce error and the method to mitigate this problem can also be the optimization of overall phase shifter with iteration rather than optimizing each components. That is, it may also then be possible to cancel errors by introducing intuitional errors into the performance of the components.

4.3.2. Miniaturized Branch Line Coupler (M-BLC)

As shown in Figure 4.2, the branch-line coupler has four quarter wavelength at the designed frequency and they occupy a large area resulting in high fabrication costs, especially when gold is used as the conductor. However, today's devices require compact and low-cost components accompanying high performance [40]. Thus, it is better to take this trend into consideration even if there is no size limitation as a specification.

A size-reduction method for hybrid couplers is proposed in [41] which employs short high-Z TLs and shunt lumped capacitors. Although there are several other techniques for size-reduction such as presented in [30-32], this method is quite compatible with CPW and capacitive-shunt switch fabrication. Hence, this miniaturization techniques will be exploited using the equivalent line models given in Figure 4.6.



(a) Standard λ/4 line. (b) π-model equivalent line.

Figure 4.6. Miniaturization of a typical transmission line [40].

Examining the equivalence of the circuits in Figure 4.6 (a) and (b), the admittances are found in Equation (4.7):

$$Y_a = \frac{1}{jZ_0}\begin{bmatrix}0 & 1\\ 1 & 0\end{bmatrix} \text{ and } Y_b = \begin{bmatrix}\frac{cos\theta}{jZsin\theta} + j\omega_0 C & \frac{1}{jZsin\theta}\\ \frac{1}{jZsin\theta} & \frac{cos\theta}{jZsin\theta} + j\omega_0 C\end{bmatrix} \tag{4.7}$$

where Z_0, Z, θ and ω_0 are the characteristic impedance of the quarter-wavelength line, the characteristic impedance of the high-Z TL, the electrical length of it and the angular frequency, respectively.

As they are equivalent circuits, the following equations are to be satisfied.

$$Z = \frac{Z_0}{sin\theta} \text{ and } C = \frac{cos\theta}{\omega_0 Z_0} \tag{4.8}$$

Equation (4.8) indicates that there are two free parameters to choose and the others are found using the formula. As an example, choosing $Z_0 = 50\Omega, \theta = 60°$ and then Eqn. 3.8 results in $Z_1 = 57.7\Omega, C_1 = 159.2\, fF$. However, it should be noted that the lumped-capacitor is designed at the center frequency ω_0 and hence, it causes to narrower bandwidth. In order to see this effect, 50Ω and 35.4Ω quarter wavelength transmission lines are shortened to equivalent lines with electrical lengths of $\theta = 30°$ and $\theta = 60°$. The corresponding parameters are listed in Table 3.2 and 3.3 considering glass substrate with $\varepsilon_r = 4.6$.

Table 4.2. Parameters for equivalent lines for 50Ω, 90°-transmission line.

Electrical Length (°)	**Length (μm)**	**Characteristic Impedance (Ω)**	**Capacitance (fF)**
$\theta = 90°$	4420	50	-
$\theta = 60°$	2720	57.74	159.2
$\theta = 30°$	1407	100	275.7

Table 4.3. Parameters for equivalent lines for 35.4Ω, 90°-transmission line.

Electrical Length (°)	**Length (μm)**	**Characteristic Impedance (Ω)**	**Capacitance (fF)**
$\theta = 90°$	4580	35.36	-
$\theta = 60°$	3003	40.82	225.1
$\theta = 30°$	1487	70.71	389.8

Using the parameters in Table 4.2 and Table 4.3, it is possible to decrease the area approximately by a factor of 8. However, the bandwidth gets narrower and the error in phase-shift significantly increases with miniaturization as seen in Figure 4.7.

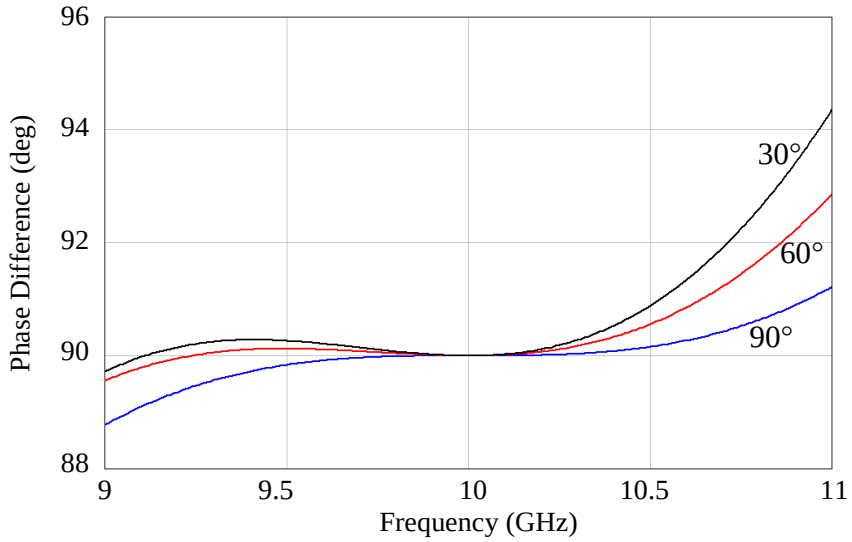


Figure 4.7. The phase difference dependence on θ values.

Due to the fact that the bandwidth defined by phase accuracy and peak error is the most important parameter of designed phase shifter, it is better not to reduce the transmission length. Moreover, for low phase shift steps such as 22.5°, even without any size reduction, the bandwidth is not wide enough to satisfy 20% bandwidth specification as shown in Figure 4.5. Thus, another approach is proposed to for a wider bandwidth in the following section.

4.3.3. Double Stage Branch Line Coupler (DBLC)

Because of the bandwidth considerations described in the previous section, a different method is employed for a wide-band phase shift performance. This method implements an extra branch-line section added to conventional BLC in Figure 4.2. Again, all TL lengths are normally λ/4 as shown in Figure 4.8. This topology is called as *"Double Branch-line Coupler"* and will be abbreviated as *"DBLC"* through this thesis.

Although their physical dimensions are larger compared to a conventional hybrid, multi-stage structures are often used to achieve wider bandwidths [44].

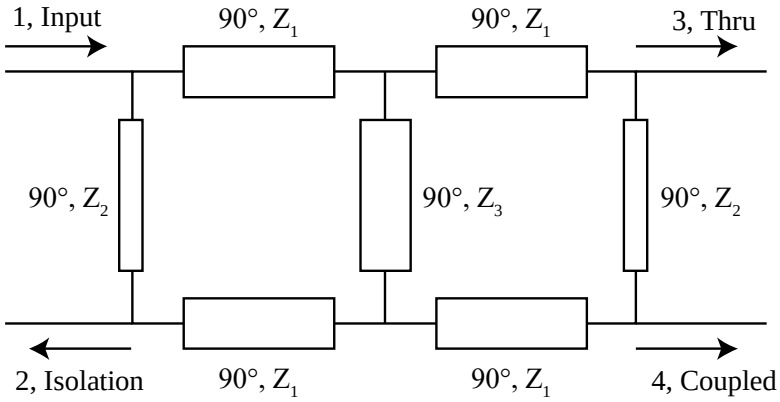


Figure 4.8. Schematics of an ideal double branch-line coupler (DBLC).

In this topology, the relation between the characteristic impedances of λ/4 transmission lines are given in Equation (4.9).

$$Z_2 = Z_0\left(1+\sqrt{2}\right) \; and \; Z_3 = \sqrt{2}\,\frac{Z_1^2}{Z_0} \tag{4.9}$$

Note that for a typical $Z_0 = 50\Omega$ system, $Z_2 = 120.7\Omega$ is fixed. However, Z_3 can be found from Equation (4.9) once Z_1 is set as a design parameter. The dependence of phase shift performance on Z_1 is given in Figure 4.9. As seen, phase error is minimum when the characteristic impedances, $Z_1 = Z_3 = \frac{50}{\sqrt{2}} = 35.4\Omega$ are choosed.

Another advantage of choosing Z_1 and Z_3 equal is the simplicity in modeling because T-junction, designed in following section of this chapter, will be more successful in connecting them with less mode disturbance at the nodes, as shown in Figure 4.16 (a).

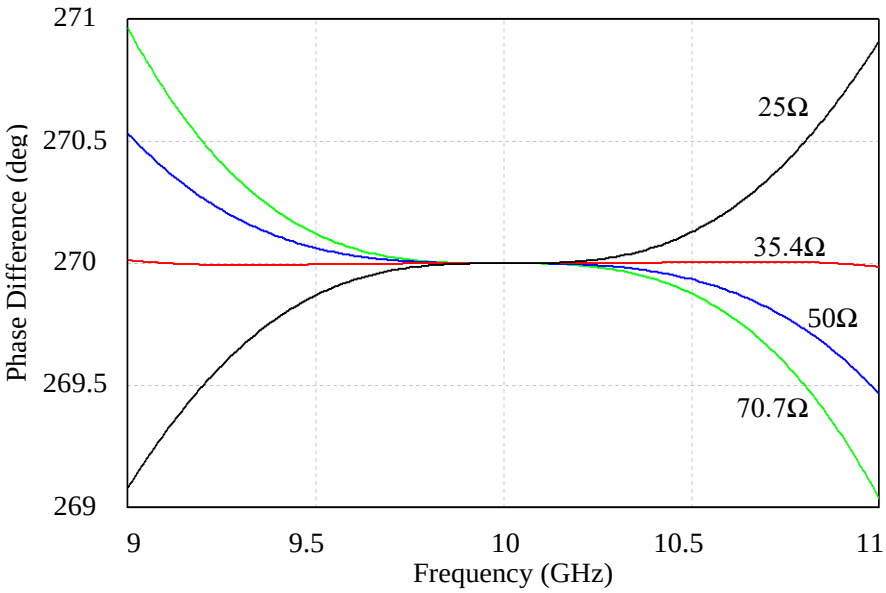


Figure 4.9. Phase shift performance of DBLC for different Z_1 values.

When Z_1 and Z_3 are chosen to be equal to 35.4Ω, phase error is low as 0.02° which is negligible. This is a very significant improvement when compared to the single BLC of which phase shift performance is given in Figure 4.5.

In Figure 4.10, the ratio of the powers transmitted to coupled and thru ports are given. The power imbalance between the output arms is below 0.5 dB in the bandwidth. Nevertheless, this imbalance should be noted as an error source contributing to accuracy and peak phase errors of overall phase shift design.

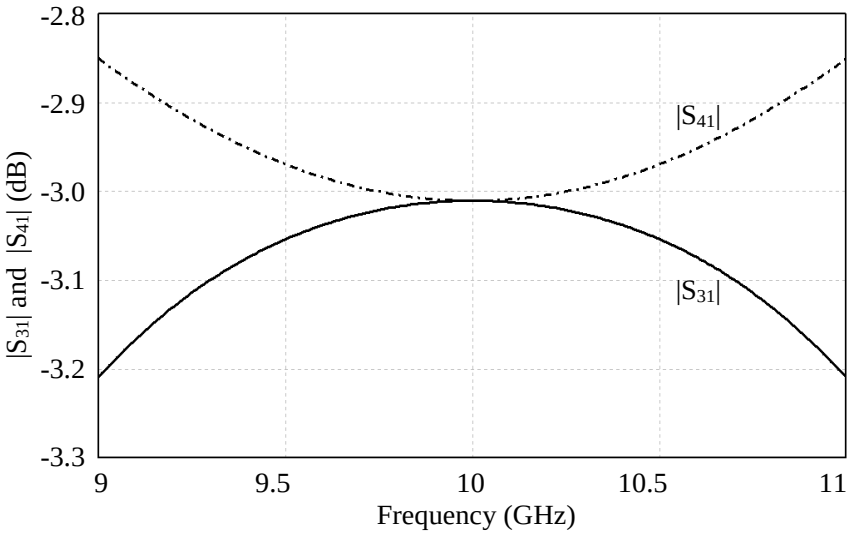


Figure 4.10. The power division performance of ideal DBLC between 9-11 GHz.

The return loss (solid line) and isolation (triangles) of ideal DBLC is given in Figure 4.11 and they are both better than -22 dB in the frequency band which are also quite superior over single BLC in addition to phase accuracy.

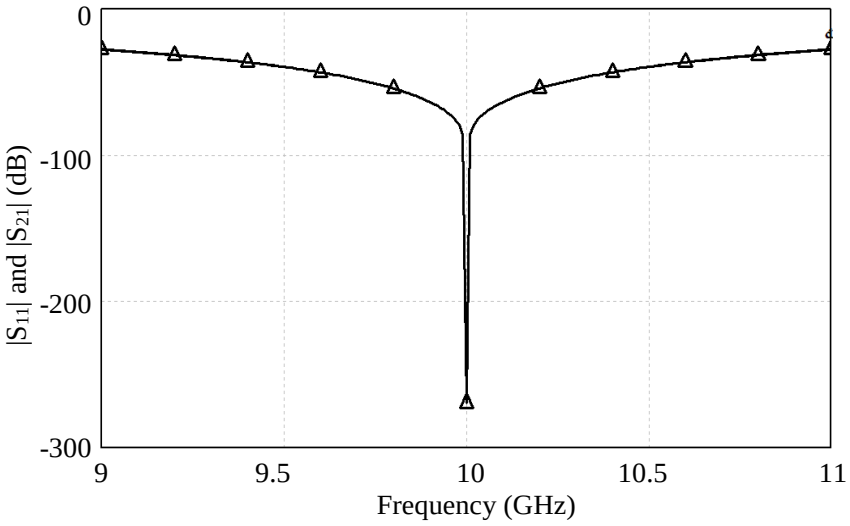


Figure 4.11. The return loss (solid line) and isolation (triangles) of ideal DBLC.

4.3.4. Miniaturized Double Stage Branch Line Coupler (MDBLC)

The DBLC shown in Figure 4.8 can also be miniaturized replacing λ/4 lines by high-Z lines using previous approach mentioned in Section 4.3.2. In this case, 4500-μm transmission lines having the characteristic impedance of 35.4Ω and the electrical length of 90° are shortened to 2293-μm/41.5Ω transmission lines using 164 fF RF MEMS bridge capacitances. Note that this parameters are different from those in Table 4.3 because the width of signal trace and gaps are changed. In order to extend the bandwidth, the electrical lengths for Z_1=35.4Ω is selected as 60°. The corresponding results are given in Figure 4.12. The maximum phase shift error is 0.7° and power imbalance is 0.5 dB between 9 and 11 GHz.

Note that although Z_3 is also 35.4Ω, it cannot be reduced as it has to have the same length as 120.7Ω transmission lines at the right and left branches. This is because of the implementation of the branch-line coupler will be in a rectangular shape as shown in Figure 4.15. Again, 120.7Ω transmission lines have to have air bridges to connect both ground planes to avoid mode disturbance. Thus, it will also be reduced by air bridge capacitors but it should be as minimum as possible.

Here, it should be noted that the electrical lengths of the lines are adjusted in a way that the phase error and the power imbalance is minimum. However, designed branch-line couplers are assumed to be lossless and the total loss due to conductor loss and dielectric loss will also significantly affect the phase response. Thus, they should also be optimized after electromagnetic (EM) model simulations. Moreover, another optimization can also be performed after integration with the reflective terminals to reduce the errors and increase the phase shift performance.

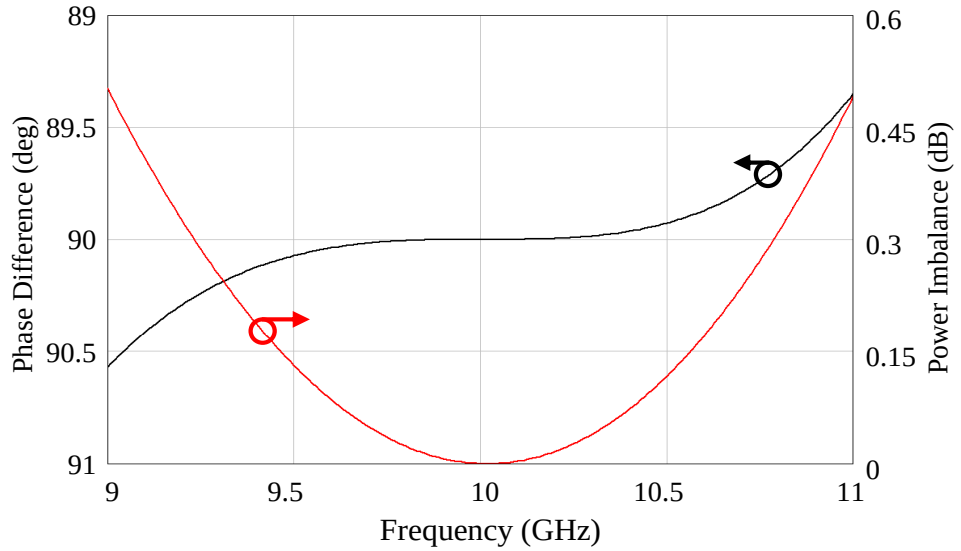


Figure 4.12. The phase difference and power imbalance ports of M-DBLC.

Return loss, isolation and coupling performance of M-DBLC is plotted in Figure 4.13. As seen, both return loss and isolation are better than -21 dB in the frequency band. Power division between coupled and thru is almost equal to -3.38 dB at the center frequency and maximum imbalance is lower than 0.5 dB in 9-11 GHz.

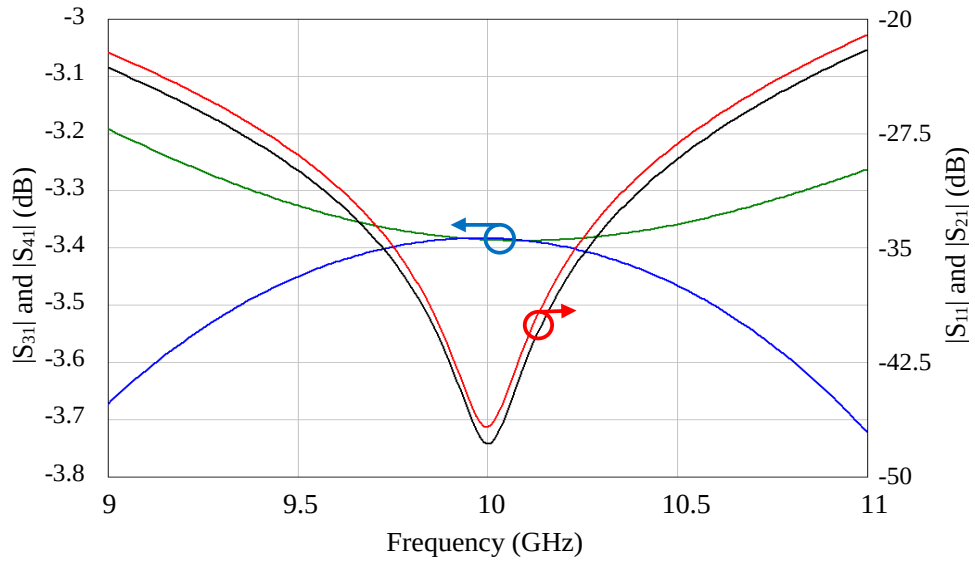


Figure 4.13. Return loss, isolation and coupling performance of M-DBLC.

4.3.5. Comparison of Designed Couplers

In previous sections, four types of branch-line couplers (BLC) are designed and their performances are compared in Table 4.4. It is seen that adding an extra branch to regular BLC results in a wider bandwidth defined by the phase error or the power imbalance.

Table 4.4. Performance comparison of lossless BLC designs between 9-11 GHz.

Coupler Type	**Maximum Phase Error (°)**	**Maximum Power Imbalance (dB)**	**Total Conductor Length (mm)**
BLC	1.2	0.7	17.8
Miniaturized BLC	2.9	0.8	11.4
Double BLC	0.5	0.5	31.3
Miniaturized DBLC	0.7	0.5	27.6

Note that transmission lines implemented in designed couplers are assumed to be lossless. In a more realistic case, the transmission lines are lossy and even if the power balance is conserved, the phase error increases.

Here, there is a trade-off between the sources of phase error. That is, if DBLC is preferred rather than regular BLC, the phase error is decreased but the total conductor loss increases which means the phase performance may be affected. Thus, miniaturization of DBLC becomes more important and M-DBLC is to be chosen.

4.4. 3D Modelling and Electromagnetic (EM) Simulations of Coupler

In previous sections, various branch-line couplers are designed with ideal transmission lines and their performances are compared. As mentioned, due to its wide-band characteristics, Miniaturized Double Branch Line Coupler (M-DBLC) is preferred for the design.

In this section, the transmission lines with miniaturization capacitances are modelled in EM simulator. Figure 4.14 represents 3D EM model of M-DBLC designed in Section 4.3.4. Transmission lines are implemented using co-planar waveguides (CPW) rather than microstrip line to avoid microstrip-to-CPW transition which introduces extra design step and so extra error. Moreover, METU RF MEMS capacitive, shunt switches have been developed for CPW lines.

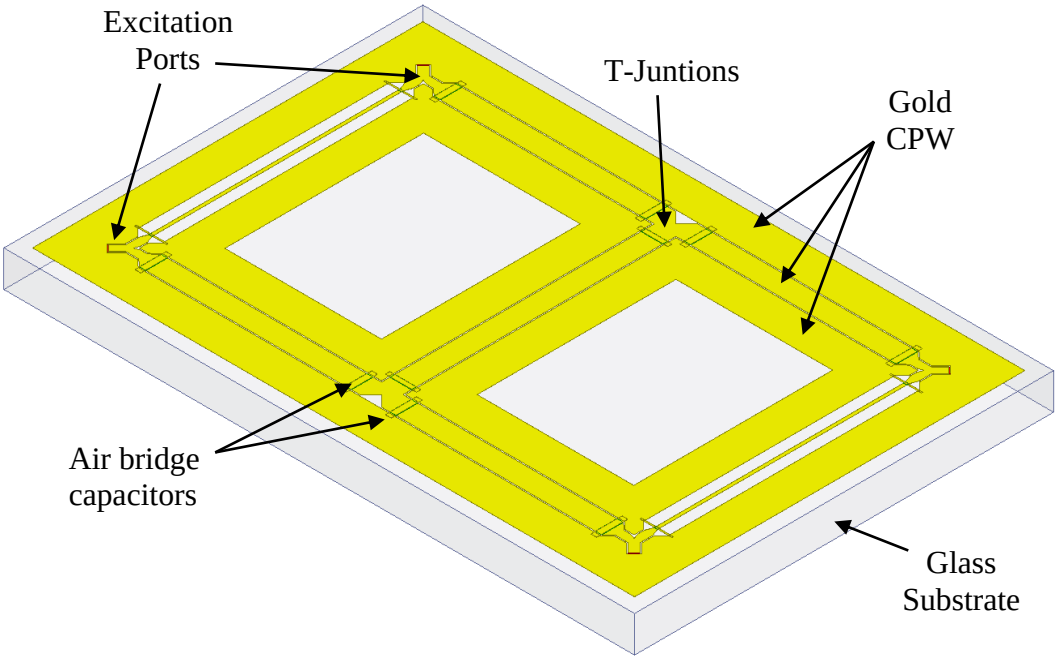


Figure 4.14. EM model of Miniaturized Double Branch Line Coupler (M-DBLC).

As a design objective, materials are chosen to be compatible with METU RF MEMS process. 500μm-thick glass substrate with $\varepsilon_r = 4.6$ and gold conductor lines with $\sigma = 3.10^7$ Siemens [2] are employed to create CPW lines, Z_1, Z_2 and Z_3 as shown in Figure 4.15. At each ends of transmission lines, fixed capacitors are placed for both connecting ground lines on each side and miniaturization. Employing lumped-elements to reduce distributed-line lengths limits the bandwidth but it decreases the loss which is a significant phase error source. Thus, capacitance values are to be optimized for wide-bandwidth with minimum phase errors.

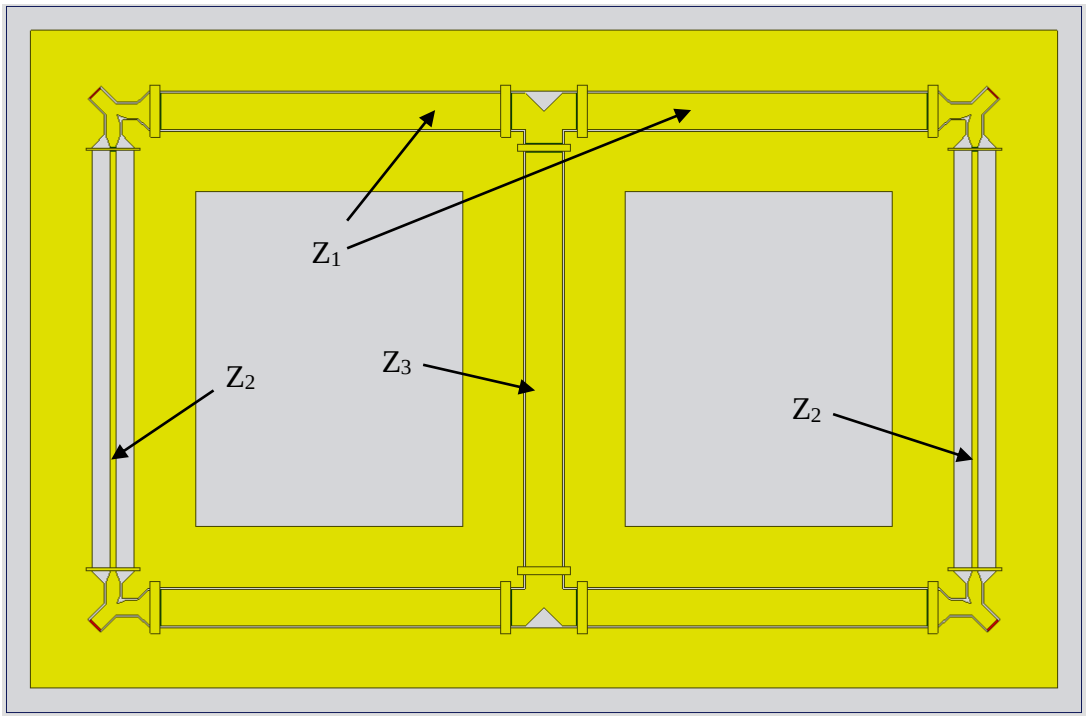
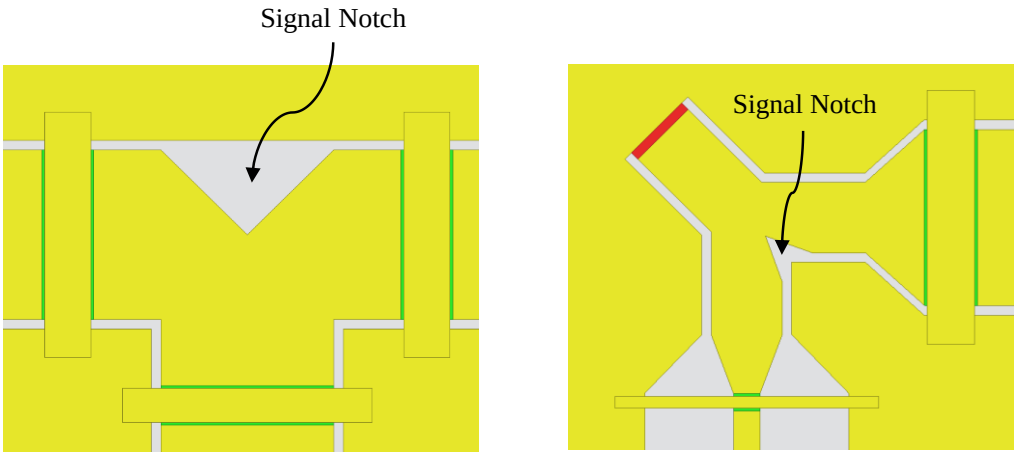


Figure 4.15. Top view of miniaturized double branch line coupler model.

In implementing double branch-line couplers with CPW lines, the major challenge is that $Z_2 = 120.7\Omega$ lines require very narrow signal traces with wide gaps in opposite to

$Z_3 = 35.4\Omega$ which is formed by wide signal traces and narrow gaps. At the port corners, these lines connects to each other with Y-junctions which directly affects the modes. Thus both T-junctions and Y-junctions shown in Figure 4.16 require extra meticulous design.



(a) T- junction. (a) Y-junction.

Figure 4.16. EM model of designed transmission line junctions.

As directly connecting these contradictory lines causes mode conversion at the junctions and so power loss, a similar approach to T-junctions developed in [8] is followed. That is, they are both connected to 50Ω-lines first with transitions and then the junction. In this design, however, the loading effect of air bridges are not tried to be minimized as the case in [8], but rather used for miniaturization of transmission lines. Again, notches are recessed into signal traces entering the junctions to preserve signal width in the direction of ports and thru-lines. The physical dimensions of the notches are determined by parametric optimizations in Ansoft HFSS™ v11. Most important design parameters of M-DBLC are listed in Table 4.5.

Table 4.5. Model parameters for M-DBLC.

Explanation	**Parameter**	**Value**
Signal Width (120.7Ω)	W120	45 μm
Gap Width (120.7Ω)	G120	150 μm
Air Bridge Width (120.7Ω)	Wab	20 μm
Line Length (120.7Ω)	L120	3705 μm
Signal Width (35.4Ω-Z_1)	W35	300 μm
Gap Width (35.4Ω-Z_1)	G35	17 μm
Line Length (35.4Ω-Z_1)	L35	3055 μm
Air Bridge Width (35.4Ω-Z_1)	Wab35	80 μm
Signal Width (35.4Ω-Z_3)	W35mid	300 μm
Gap Width (35.4Ω-Z_3)	G35mid	16 μm
Air Bridge Width (35.4Ω-Z_3)	Wab35mid	60 μm
Signal Width (50Ω-ports)	W50	120 μm
Gap Width (50Ω-ports)	G50	16 μm
T-junction Notch Width	ir35	150 μm
T-junction Notch Length	irr35	150 μm
Y-junction Notch Width	ir	40 μm
Y-junction Notch Length	irr	50 μm
Height of airgap	Hbrid	1.2 μm
Thickness of dielectric layer	t_d	0.3
Relative permittivity of dielectric layer	ε_d	7
Relative permittivity of substrate	ε_{subs}	4.6

As seen in Table 4.5, despite of the fact that Z_1 and Z_3 are both 35.4Ω-lines, they do not have equal design parameters as Z_3 must have to same length with 120.7Ω-lines placed on left and right most branches to preserve rectangular geometry as mentioned in previous section.

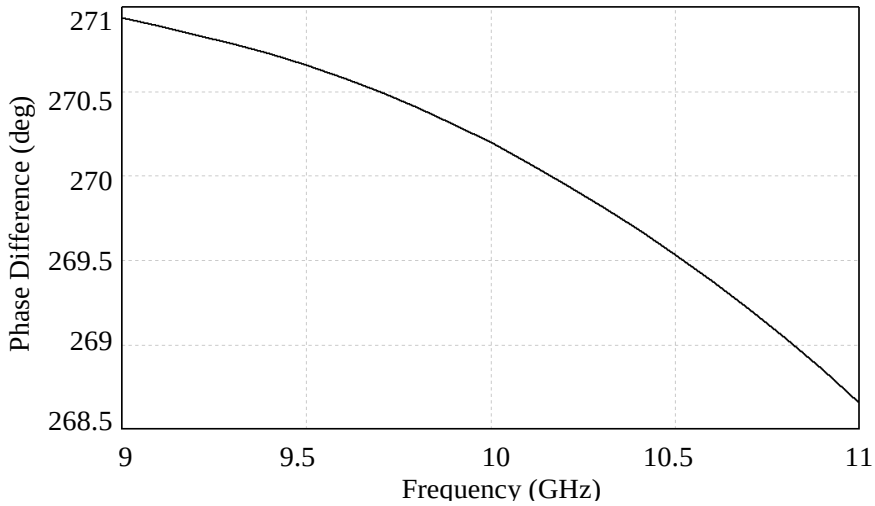


Figure 4.17. Phase difference between coupled and thru ports of M-DBLC.

In Figure 4.17, phase difference between the output arms of the coupler is given. Although the performance is not as good as the ideal design due to parasitic bridge capacitances and losses (dielectric loss and conductor loss), it still satisfies the design specifications. Furthermore, the slope of the phase difference over frequency is negative which is opposite to that of capacitor bank and this is advantageous because they cancel each other and decrease peak error at 9 and 11 GHz.

The power division between coupled and thru ports is given in Figure 4.18. Maximum power imbalance is 0.3 dB around 9 GHz and lower than 0.15 dB in 75% of the frequency band. Both power levels are about - 4.4 dB due to conductor and dielectric losses in addition to non-optimal return loss and isolation. Here, however, it should be noted that the optimization goal is set to obtain 90° phase difference between coupled and thru with minimum phase error and power imbalance.

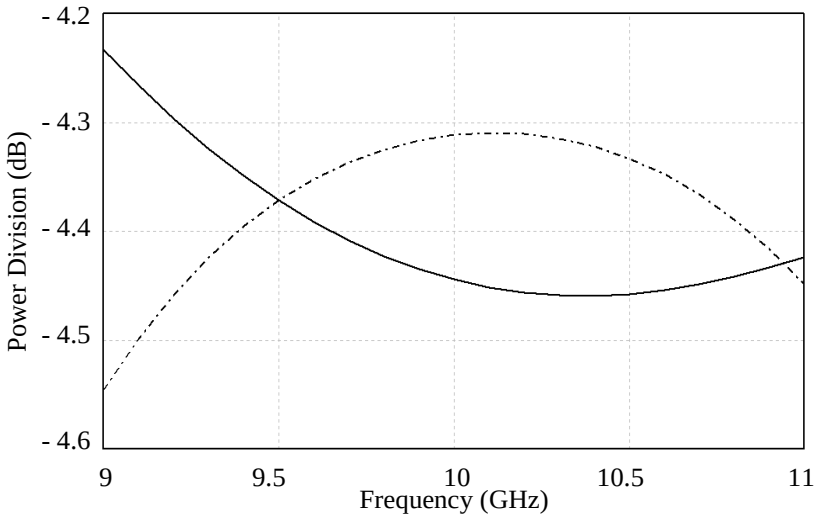


Figure 4.18. Power division between couple (solid) and thru (dashed) ports.

Figure 4.19 presents return loss (solid line) and isolation (dashed line) performance of the M-DBLC. Non-ideality of designed transmission lines and mode conversion on the junctions, which are not completely prevented, result in a frequency shift between return loss and isolation dips. Nevertheless, they are both better than -25 dB in the frequency band which causes negligibly small degradation in cascading performance.

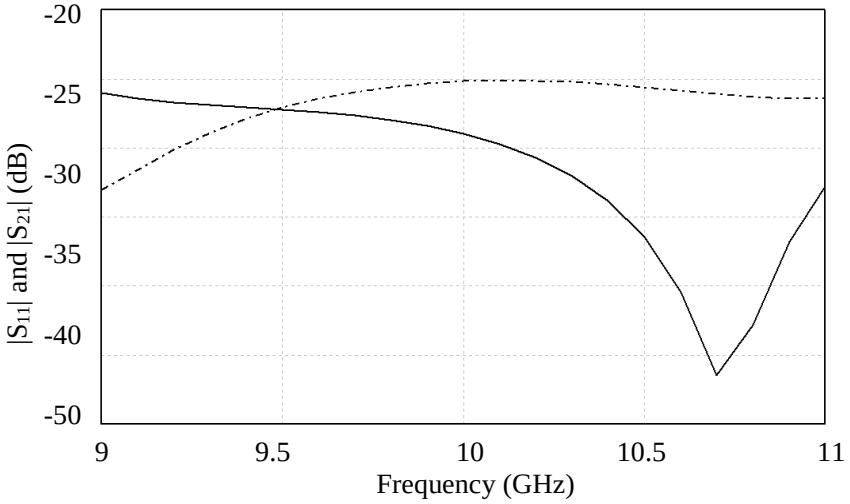


Figure 4.19. Return loss (solid) and isolation (dashed) of M-DBLC.

CHAPTER 5

INTEGRATION OF THE BUILDING BLOCKS AND 3-BIT 180° PHASE SHIFTER

Previous chapters establish 3-dB coupler and reflect terminal designs as two building blocks of reflect-type phase shifter while this chapter explains the integration of these blocks. Section 5.1 describes matching problems encountered in direct integration of them. Section 5.2 proposes a solution for this problem and presents a successful 2-bit 90° phase shifter with further optimizations. Finally, Section 5.3 deals with successive addition of two 2-bit phase shifters and by doing so, 3-bit phase shifter 180° phase shift which fully satisfies design specifications is obtained.

5.1. 2-bit 90° Phase Shifter

In this section, the coupler (M-DBLC) designed in previous chapter is directly terminated by RF MEMS capacitor bank (Design-3) as shown in Figure 5.1. The phase of output power incrementally shifts by 22.5° at each state with respect to that at reference state where no bridge is actuated, *i.e.* all capacitors are state up-state.

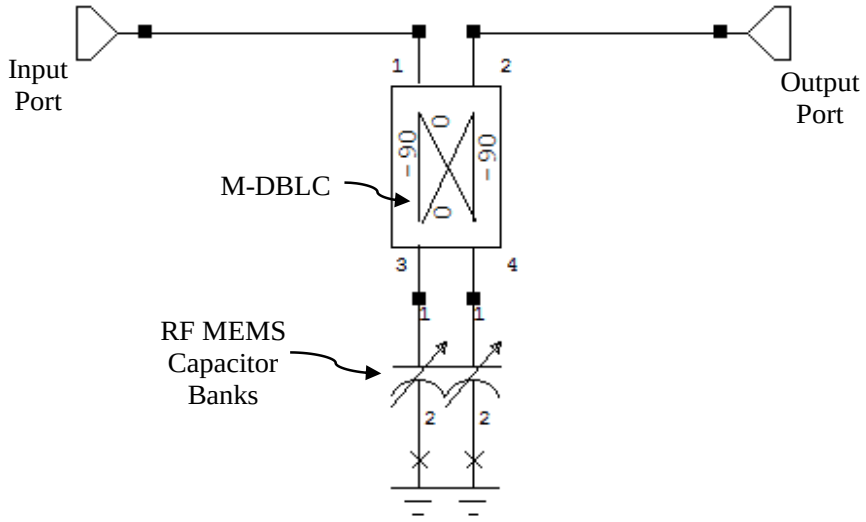


Figure 5.1. 2-bit 90° RF MEMS phase shifter.

Figure 5.2 presents the phase shift performance of implemented 2-bit phase shifter. As shown, it fails to provide any of the phase delays accurately. The accuracy error and peak error at each state is listed in Table 5.1. As seen from the table, both accuracy and peak error are much higher than allowed by the design specifications given in Table 1.1 in the introduction chapter.

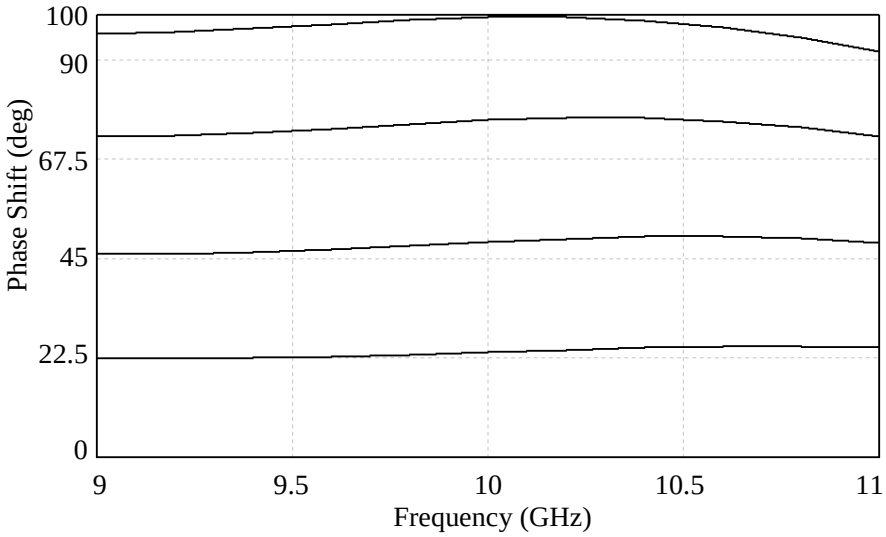


Figure 5.2. Phase shift performance of 2-bit 90° phase shifter.

Table 5.1. Phase errors of 2-bit phase shifter.

Phase Step	9 GHz	10 GHz	11 GHz	Accuracy Error	Peak Error
22.5°	22.28	23.82	24.8	5.9%	10.2%
45°	45.83	48.3	48.54	7.3%	7.9%
67.5°	72.51	76.24	72.72	12.9%	7.7%
22.5°+45°	68.11	72.12	73.34	6.8%	8.7%
90°	95.78	99.44	92.07	10.5%	6.4%

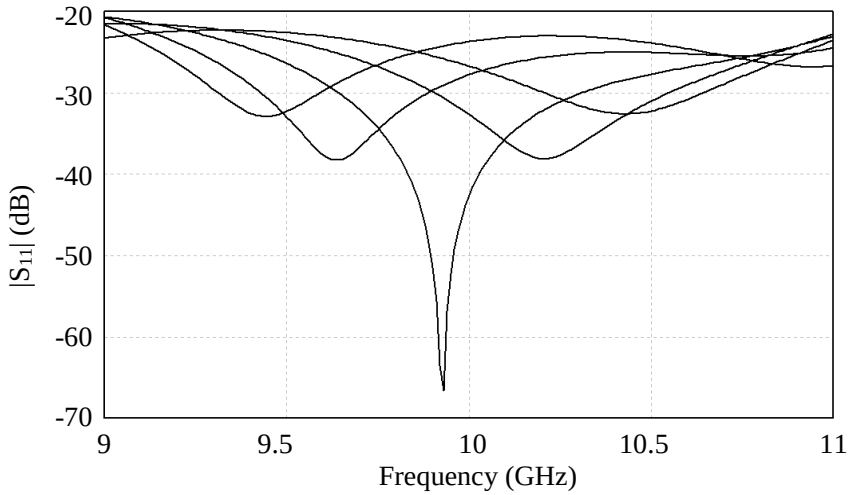


Figure 5.3. Return loss of 2-bit phase shifter for all states.

The return loss and insertion loss of 2-bit phase shifter for all states are given in Figure 5.3 and Figure 5.4, respectively. The return loss is better than -20 dB in all cases which allows successfully cascading two phase shifters for 3-bit operation. However, the phase shifter is quite unsuccessful at 90° phase delay which means it cannot be used as MSB either. The results state clearly that the building blocks, which separately work very well, are not capable of providing desired phase shifts together.

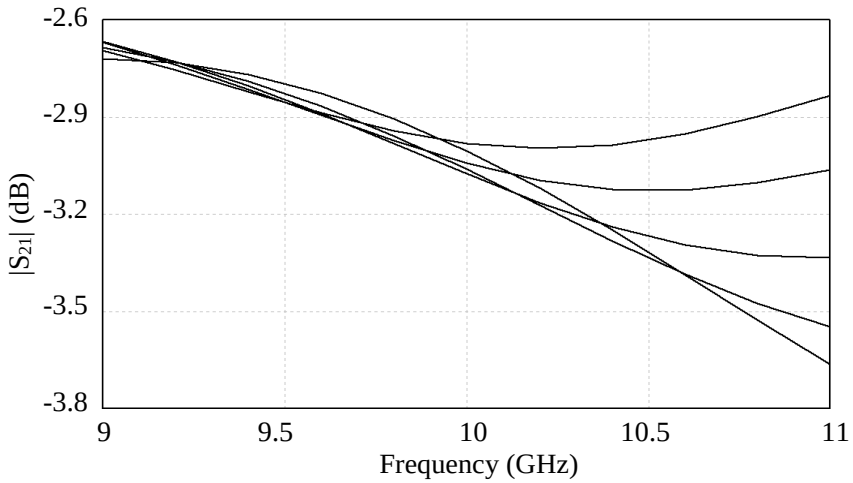


Figure 5.4. Insertion loss of 2-bit phase shifter for all states.

The problem has already winked in Section 2.8 which investigates the switched-capacitor bank phase shifters. As stated, the bandwidth is limited by the 3-dB coupler to around $\pm$15% due to the reactive loading at the output ports. The input impedance of the capacitor bank dramatically changes at different states due to capacitive loading. Thus, an impedance matching network is needed to mitigate the phase error problem.

5.2. Further Optimizations with Impedance Matching

The input impedance seen by the coupler ports can be simply changed with insertion of identical transmission lines between the coupler and the capacitor bank. The schematics of proposed solution is given in Figure 5.5. The length and characteristic impedance of this transmission line is optimized using AWR Microwave Office™ 2006 with optimization goals set to minimize phase errors especially at 22.5°.

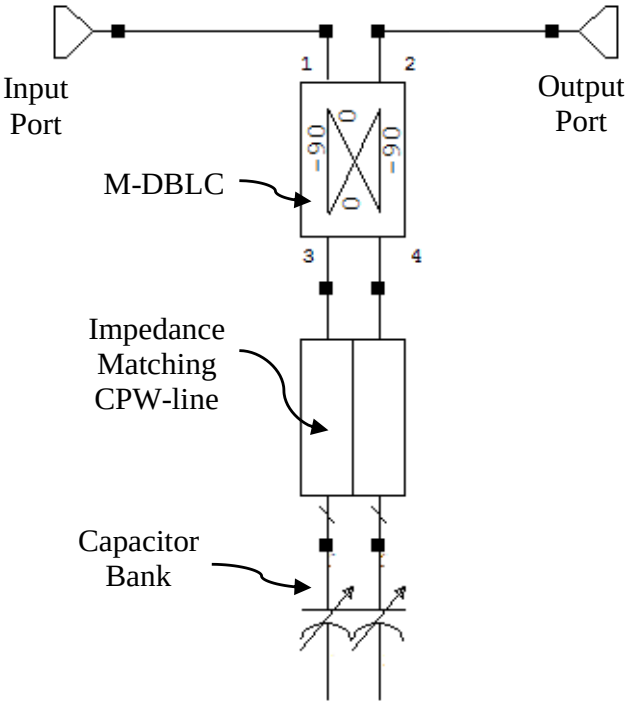


Figure 5.5. Implementation of CPW lines for impedance matching.

Optimization results show that implementing 47Ω-transmission lines with 49.5° electrical length before the capacitor bank optimizes the impedance seen by the coupler. Thus, a CPW line with parameters in Table 5.2 is designed as impedance matching network.

Table 5.2. Design parameters of CPW line employed for impedance matching.

Parameter	**W**	**G**	**L**
Value	310 μm	30 μm	2478 μm

Figure 5.6 shows the performance of 2-bit phase shifter with impedance matching transmission line. As seen, the errors significantly decreases due to wider bandwidth provided by the coupler. The phase shift is a bit lower around 11 GHz than expected for 45° and 90° steps, however, it still satisfies the design specifications. The accuracy and phase errors are given in Table 5.3.

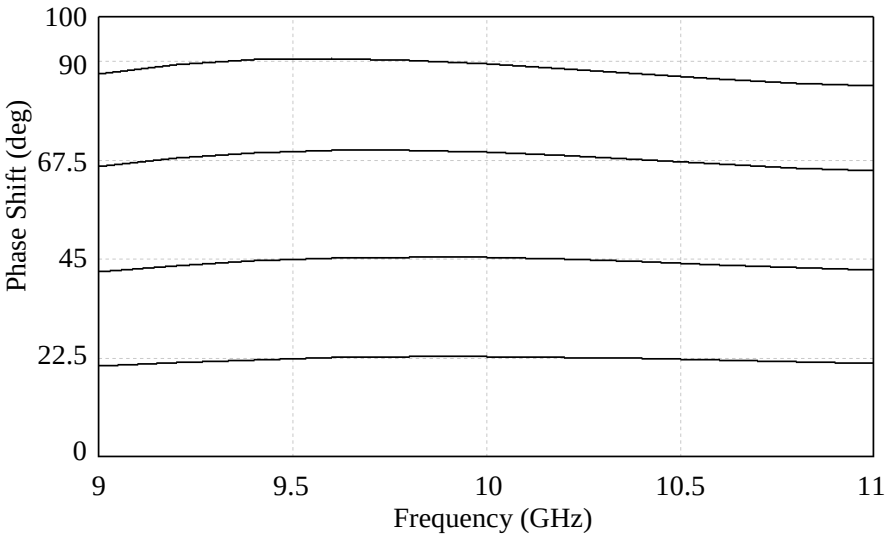


Figure 5.6. Performance of 2-bit phase shifter with impedance matching.

Table 5.3. Phase errors of 2-bit phase shifter after impedance matching.

Phase Step	**9 GHz**	**10 GHz**	**11 GHz**	**Accuracy Error**	**Peak Error**
22.5°	20.62	22.77	21.26	1.2%	-5.5%
45°	41.97	45.31	42.31	0.7%	-6.0%
67.5°	65.98	68.87	64.98	2.0%	-2.3%
22.5°+45°	62.59	68.08	63.57	0.9%	-5.8%
90°	87.12	89.52	84.29	-0.5%	-3.2%

The accuracy error is maximum 2% at 67.5° phase step. As mentioned before, however, the accuracy error is lower than 1.2% for all states when this step is realized by 22.5°+45° in 3-bit operation. The cascading performance significantly depends on the return loss of 2-bit phase shifter. Thus, the return loss is better than -21 dB for all states in the frequency band as shown in Figure 5.7. In Figure 5.8, the insertion of the phase shifter is presented. It is also better than -2.95 dB in the band. Compared to Figure 5.4, impedance matching also decreases the insertion loss.

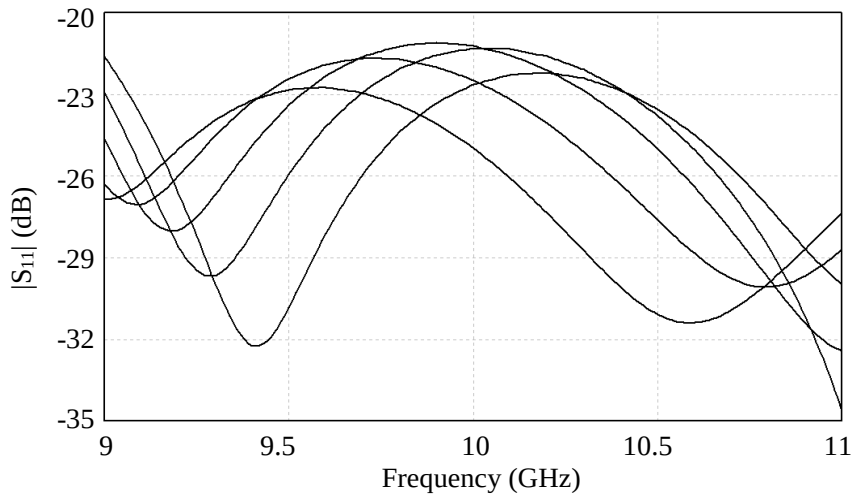


Figure 5.7. Return loss of 2-bit phase shifter after impedance matching.

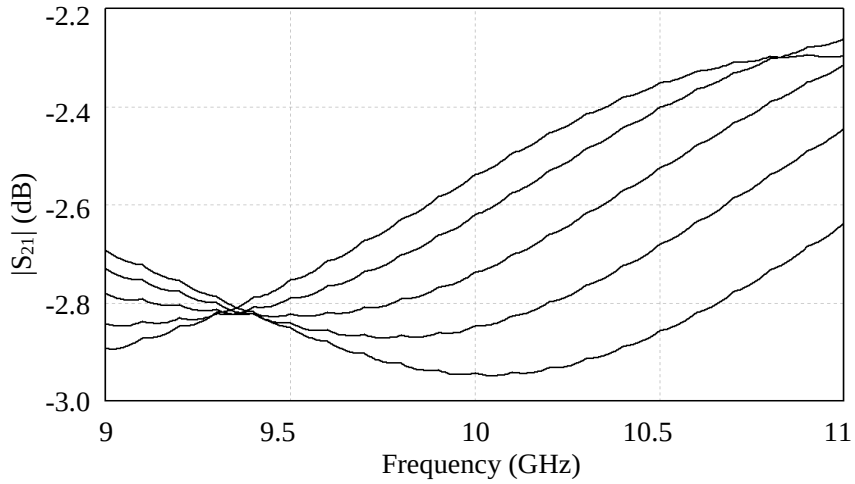


Figure 5.8. Insertion loss of 2-bit phase shifter after impedance matching.

5.3. 3-bit 180° Phase Shifter

In Figure 5.9, it is schematically shown that two 2-bit 90° phase shifter are cascaded to obtained 3-bit 180° phase shifter. The simulation results for this phase shifter are given in Figure 5.10. As shown, the phase steps are quite successful in lower bits and the error at 11 GHz increases in upper bits. This is mainly because the impedance

matching CPW line is optimized for minimum peak error in 22.5°. Fortunately, the percentage error is also low at higher phase delays.

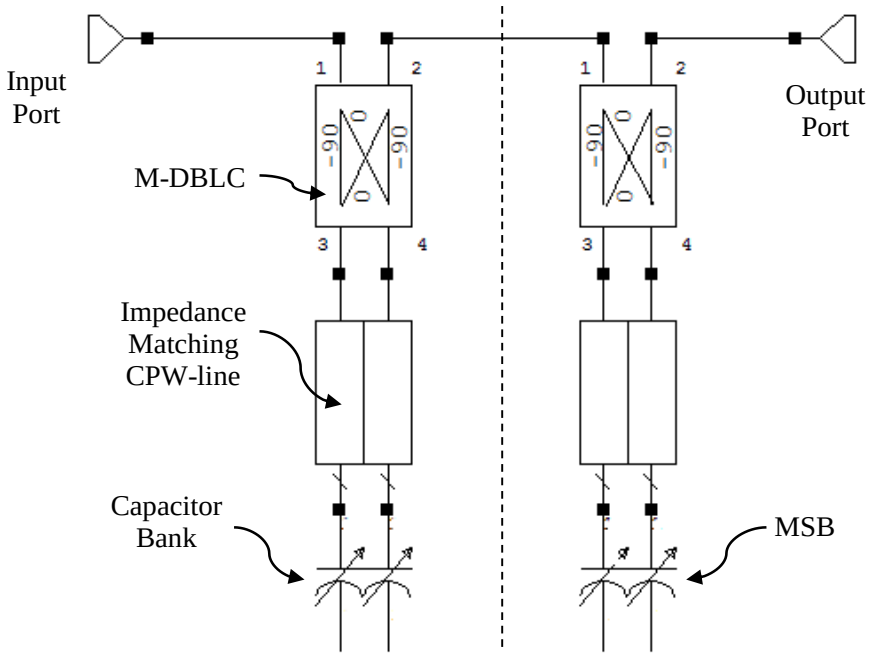


Figure 5.9. 3-bit 180° phase shifter.

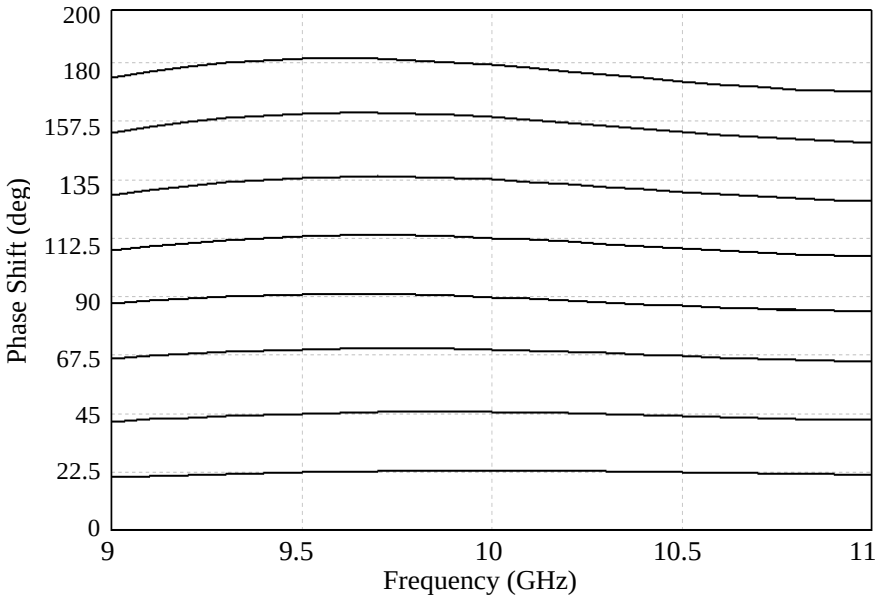


Figure 5.10. Performance of 3-bit phase shifter after impedance matching.

The accuracy and peak errors are tabulated in Table 5.4. When this table is compared to phase errors of 2-bit phase shifter given in Table 5.3, it is seen that the increase in the phase errors are insignificant. Moreover, some errors are even better such as peak error of 45° state. Only exception is the significant increase in accuracy error at 22.5° state. However, it is still below 2% accuracy error limit. The maximum accuracy error of 1.8% occurs at this state and maximum peak error is 5.8% at 45°. Finally, simulation results show that designed 3-bit phase shifter successfully operates with all accuracy and peak error values satisfy the design specifications given in Table 1.1.

Table 5.4. Phase errors of 3-bit phase shifter.

Phase Step	**9 GHz**	**10 GHz**	**11 GHz**	**Accuracy Error**	**Peak Error**
22.5°	20.57	22.9	21.31	1.8%	-5.3%
45°	41.92	45.53	42.37	1.2%	-5.8%
67.5°	65.98	69.65	65.01	3.2%	-2.3%
22.5°+45°	62.49	68.43	63.68	1.4%	-5.7%
90°	87.14	89.76	84.29	-0.3%	-3.2%
112.5°	107.7	112.5	105.5	0.0%	-4.3%
135°	129.1	135	126.6	0.0%	-4.4%
157.5°	153.1	159	149.3	1.0%	-2.8%
180°	174.3	179	168.7	-0.6%	-3.2%

The return loss of designed 3-bit phase shifter is given in Figure 5.11. It is better than -18.6 dB for all eight states in the frequency band. This states that the phase shifter can safely be used in 50Ω systems as it is matched.

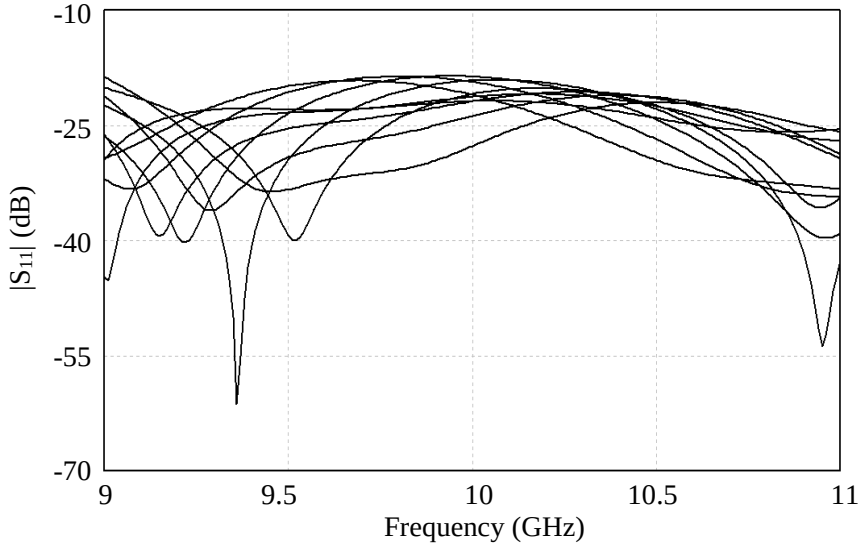


Figure 5.11. Return loss of 3-bit 180° phase shifter.

Figure 5.12, lastly, shows the insertion loss of the phase shifter which is a critical performance merit for most implementation. As seen, the insertion loss is better than -5.86 dB at all states. More importantly, maximum insertion loss variance is lower than 1 dB among phase steps.

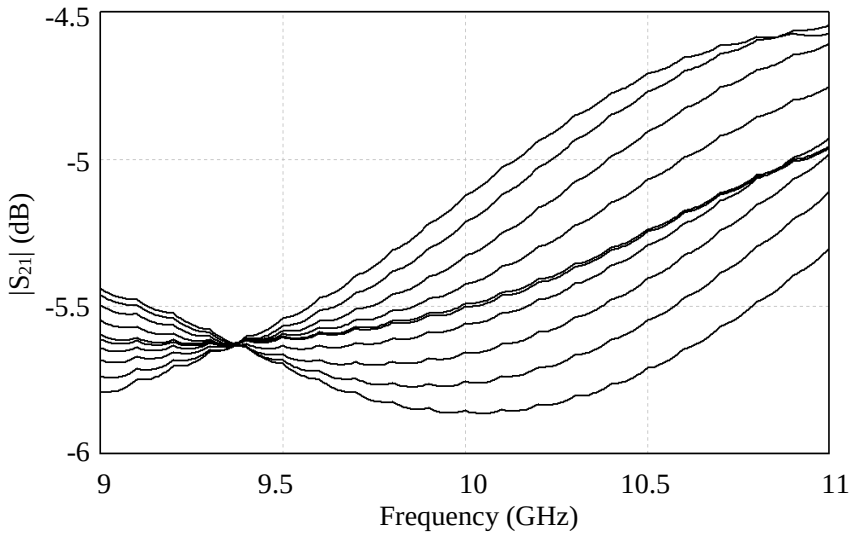


Figure 5.12. Insertion loss of 3-bit 180° phase shifter.

5.4. Sensitivity of Designed Phase Shifter to Process Variations

This section deals with the sensitivity of the phase shifter designed in this thesis to variations in the fabrication process. Especially, process variations have been experienced in the fabrication of RF MEMS bridges [2], [8], [31]. These variations result in structures with incorrect geometrical parameters. Thus, it is valuable to investigate how the phase shifter performance is affected by the process variations in the dimensions.

As one can expect, the most vulnerable part of the phase shifter is RF MEMS capacitor bank which is responsible for shifts in the reflection phase. The capacitance values at up-state and down-state of the bridge are significantly susceptible to variations in dimensions causing high phase errors, especially, in lower phase steps.

Among geometrical parameters, relative error due to variations is much higher in smaller dimensions, namely, the height and the width of the bridge while the percentage changes in greater dimensions such as bridge length can be neglected for simplicity. For this reason, sensitivity of the phase shifter performance to bridge widths and heights are discussed in next subsections.

5.4.1. Sensitivity of Phase Shifter to Bridge Widths

As Equations (3.1) and above(3.2) suggest, the area of the parallel plate capacitor formed by the bridge and the signal trace is directly proportional to the bridge width, W_b. Neglecting the variations in bridge length L_b, any variation in W_b changes the up-state and down-state capacitance with the same ratio which is clearly indicated by Equation (5.1) and (5.2).

$$\Delta C_{up} = \frac{\varepsilon_0 L_b}{(\frac{t_D}{\varepsilon_D} + g)} \Delta W_b \,, \qquad \Delta C_{down} = \frac{\varepsilon_{D,eff} \varepsilon_0 L_b}{t_D} \Delta W_b \tag{5.1}$$

$$\frac{\Delta C_{up}}{C_{up}} = \frac{\Delta C_{down}}{C_{down}} = \frac{\Delta W_b}{W_b} \tag{5.2}$$

However, down-to-up capacitance ratio *DUR* remains the same as both relative changes in down-state and up-state capacitances are equal which cancel each other.

For the sake of simplicity, the variations in bridge width is defined as percentage error in W_b. Figure 5.13 shows accuracy errors occurring at 10 GHz for 22.5° and 45° phase shifts due to variation in the width of the first bridge, W_{b1}. The errors in higher bits are not shown here as they are all lower than 0.1° which is negligible. As shown, 0.2° accuracy error occurs per 1% variation in $W_{b1.}$ This means that a variation higher than 2.5% (0.6 μm) will result in the violation of design specifications. However, the higher bits are not significantly affected by this change. This is a very useful advantage of Design-3 in which the bridges are actuated separately to provide the corresponding phase shift as the variation in one bridge does not affect the other phase steps.

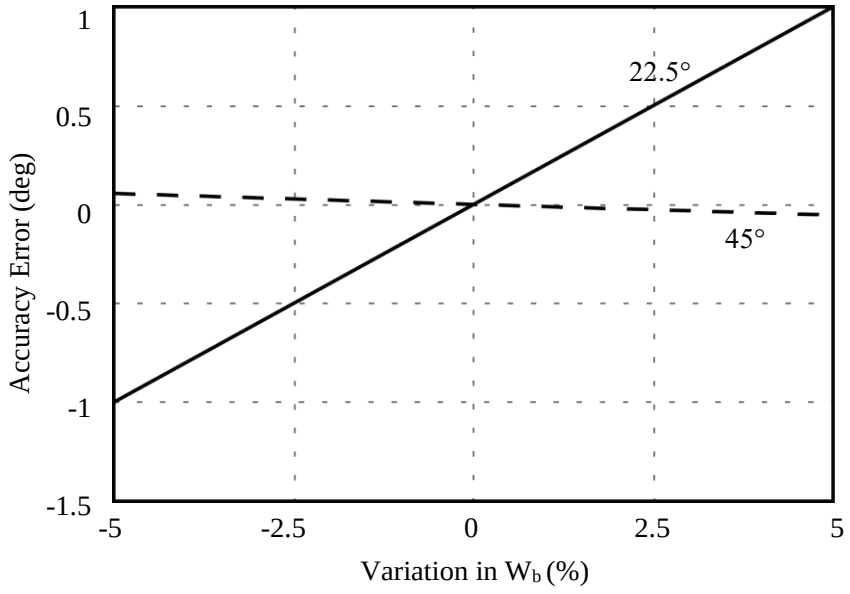


Figure 5.13. Accuracy errors at 22.5° and 45° steps due to variations in $W_{b1.}$

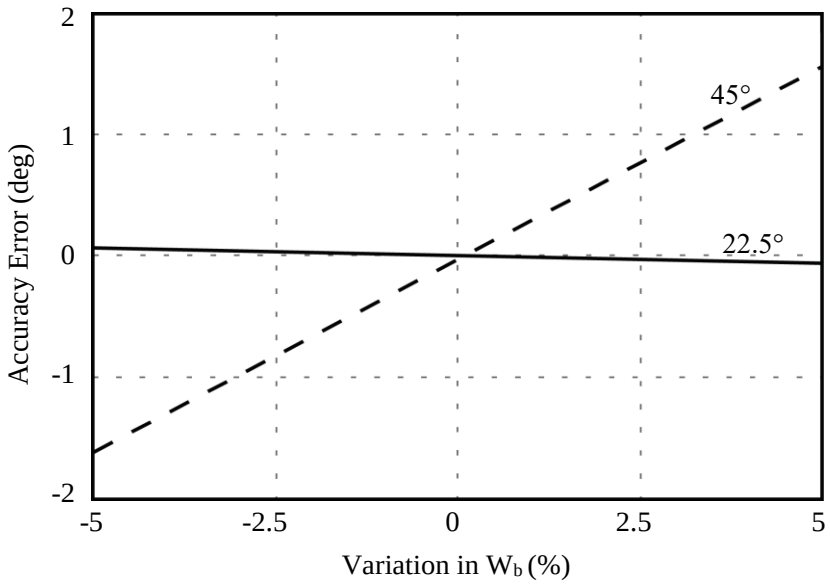


Figure 5.14. Accuracy errors at 22.5° and 45° steps due to variations in W_{b2}

Figure 5.14 presents the sensitivity to variations in the width of the second bridge which is responsible for providing 45° phase shift. Again, there occurs an accuracy error of 0.32° per 1% variations in the second bridge width at 45° phase step which means variations higher than 2.8% (1.6 μm) will violates the design specifications. Fortunately, 22.5° phase step is negligibly affected by this variations.

5.4.2. Sensitivity of Phase Shifter to Bridge Heights

One of the common process variations is the unexpected changes in the bridge height, *g*, due to stress and degradation of the spring constant [2], [8], [31]. These variations directly affects the up-state capacitance ratio and *DUR* as down-state capacitance remains the same.

$$C_{up,2} = \frac{\varepsilon_0 A}{(\frac{t_D}{\varepsilon_D} + g_{ni})} = C_{up}, 1 \frac{(\frac{t_D}{\varepsilon_D} + g_i)}{(\frac{t_D}{\varepsilon_D} + g_{ni})} \tag{5.3}$$

$$C_{down} = \varepsilon_{D,eff}\varepsilon_0 \frac{A}{t_D} \tag{5.4}$$

where g_i represents the ideal bridge height of 1.2 μm and g_{ni} is the non-ideal bridge heigh.t. Because bridges are placed very close to each other, dimensional variations in bridge heights are assumed to be equal. As shown in Equation (5.3) and (5.4), up-state capacitance changes with non-ideal bridge height (g_2) however down-state capacitance is not affected from this change. Thus, the effect of the bridge height to the response is not as significant as that of the bridge width as shown in Figure 5.15.

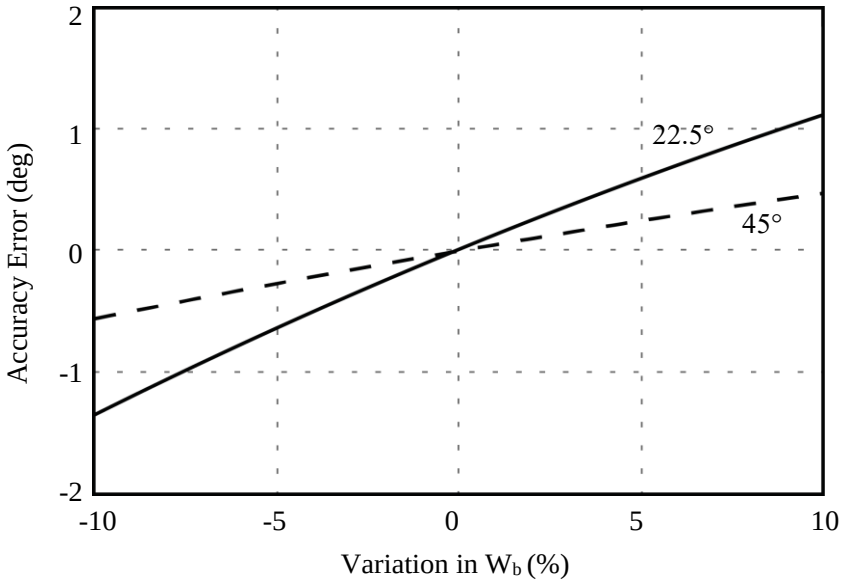


Figure 5.15. Effect of variations in all bridge heights to the performance.

Figure 5.15 shows that an approximate accuracy error of 0.06° occurs per 1% change in the bridge height and one can say that if the variation in all bridge heights are larger than 7.5% (0.1μm), the design specifications are not satisfied.

CHAPTER 6

CONCLUSIONS AND FUTURE WORK

This thesis presents an X-band, 3-bit 180° constant phase shifter based on RF MEMS technology with certain design specifications. These specifications state that phase shifter should employ CPW lines and have a maximum accuracy error of ±2% at each bit and ±8% peak error per bit. Design procedure of the phase shifter is divided into four parts.

First, several phase shifter topologies are reviewed and compared to find most promising solution. Some of the phase shifters are mostly preferred for linear phase shifting applications as they employ distributed systems providing the phase shift. Few of them are not compatible with RF MEMS capacitive, shunt switches or hard to implement with CPWs. As a result of circuit simulations, reflect-type phase shifters which offer up to ±15% bandwidth are elaborated in this thesis. These phase shifters implement 3-dB couplers and reflective terminals. Cascading two 2-bit 90° phase shifters, a 3-bit 180° phase shifter can be obtained.

Secondly, a reflective terminal which provides variable reflection phase is to be designed as the first building block. RF MEMS capacitor banks which employ electrostatically actuated MEMS bridges are designed. Various bridge and actuation configurations are simulated and compared. Among them, Design-3 consisting of a fixed MIM capacitor with three variable capacitors offers minimum accuracy error and phase error. This design is modelled with RF MEMS switches on CPW lines and simulated in Ansoft HFSS^{TM} v11. The model is able to provide 0°-90° reflection

phases in a 2-bit operation with a maximum accuracy error of 0.3% and peak error of 4.9% in 9-11 GHz.

After design of the reflective terminal, Branch-Line Coupler (BLC) topologies are investigated for the second building block. As the circuit simulations show that BLC is unable to provide the required bandwidth to cover 9-11 GHz, Double Branch-Line Coupler (DBLC) is designed instead. Employing seven 90°-lines, however, DBLC suffers from conductor and dielectric losses which degrades the phase delay performance in addition to size and cost considerations. A miniaturization approach using air-bridges as MEMS capacitors, which are originally to connect ground planes, is followed to reduce line lengths. Miniaturized DBLC (M-DBLC) is designed in ideal circuit schematics and then modelled and optimized in 3D EM solver, Ansoft HFSS^{TM} v11. Proposed model successfully divide the input power with an imbalance of 0.3 dB and 1.4° phase error between coupled and thru ports.

EM models of two building blocks are integrated to obtain a 2-bit 90° phase shifter. Directly terminating M-DBLC with RF MEMS capacitor bank in Design-3 results in an erroneous phase shifter which cannot be used especially in 90° phase step also preventing the implementation of most-significant bit. This is because the dramatic changes in the impedance seen by the coupler. This problem is mitigated with insertion of an impedance matching transmission line in between. After optimization of this line, 2-bit phase shifter with maximum accuracy error of 1.2% and peak error of 6% is obtained. This phase shifter is also successful in terms of return loss and insertion loss which are found to be better than -21 dB and -2.56 dB, respectively. Cascading two of these phase shifters, 3-bit 180° phase shifter is finally obtained. This phase shifter has a maximum accuracy error of 1.8% and peak error is 5.8%, which meets the design specifications stated at the beginning of the research. The return loss states and the insertion of the phase shifter is better than -18.6 dB and -5.86 dB, respectively for all states in 9-11 GHz frequency band.

Presented results can be improved or extended further with the following future works:

- Employing different impedance matching transmission line for the first and second 2-bit phase shifters for better matching
- Developing microfabrication techniques to bias MEMS bridges which are placed very close to each other
- MEMS fabrication and measurement results of designed models

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