X-BAND HIGH POWER GAN POWER AMPLIFIER DESIGN AND IMPLEMENTATION

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ABSTRACT

X-BAND HIGH POWER GaN POWER AMPLIFIER DESIGN AND IMPLEMENTATION

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High frequency power amplifiers play a crucial role in design, development and overall performance of wireless communication systems. Demanding requirements of the power amplifiers require improvements in output power, efficiency and bandwidth. GaN devices attract high frequency power amplifier designers due to the superior material characteristics of GaN. In this thesis, a power amplifier operating at X-band is designed and realized using a GaN discrete bare die transistor. It provides over 15 W output power and 30% PAE in continuous wave(CW) operation and 20 W output power and 40% PAE in pulsed operation. Moreover, AM/AM and AM/PM measurements are also done for both operation modes to better understand nonlinearities of GaN devices and compare CW and pulsed modes. Furthermore, pulse phase stability and spectrum behavior of the PA are also measured to evaluate the PA from a system point of view. Nonlinear and EM simulations are performed using CST Microwave Studio and AWR Microwave Office together with the nonlinear model provided by the supplier of the transistor die.

Keywords: Power Amplifier, X-band, Electromagnetic modelling, Amplifier Characterization.

ÖZ

X-BANT YÜKSEK GÜÇLÜ GaN GÜÇ YÜKSELTEÇ TASARIMI VE GERÇEKLENMESI

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Mikrodalga frekanslarda çalışan güç yükselteçler kablosuz haberleşme sistemlerinin tasarımı ve geliştirilmesi sırasında en kritik elemanlardan birisi olarak karşımıza çıkar. Günümüz sistemlerinde artan performans gereksinimleri, güç yükselteçlerin özellikle çıkış güçleri, verimlilikleri ve bant genişliklerinde iyileştirme ve geliştirme ihtiyacını ortaya çıkarmaktadır. GaN yarı iletken malzemeler üstün elektriksel özellikleri sayesinde, güç yükselteç konusunda araştırmacıların ilgisini çekmektedir. Bu çalışmada, X-bant içinde çalışan bir güç yükselteç GaN ayrık transistor kullanılarak tasarlanmış ve gerçeklenmiştir. Tasarlanan güç yükselteç sürekli çalışma modunda 15 W çıkış gücü ve 30% verimlilik, darbeli çalışma modunda 20 W çıkış gücü ve 40% verimlilik sağlamıştır. Güç yükseltecin doğrusallıktan ne kadar uzaklaştığını daha iyi anlamak için AM/AM ve AM/PM davranışları da hem sürekli çalışma hem darbeli çalışma modları için ölçülmüştür. Ayrıca, güç yükseltecin darbe faz kararlılığı ve frekans spektrumu da güç yükselteci sistem bakış açısıyla değerlendirmek amacıyla ölçülmüştür. CST Microwave Studio ve AWR Microwave Office yazılımları elektromanyetik simülasyonlar için transistor modeliyle birlikte kullanılmıştır.

Anahtar Kelimeler: Güç Yükselteç, X-bant, Elektromanyetik Modelleme, Yükselteç Karakterizasyonu.

To Derya and Deniz,

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CHAPTER 1

INTRODUCTION

1.1 MICROWAVE POWER AMPLIFIERS

Microwave power amplifiers are devices that converts DC power into significantly high microwave power by generating high frequency, large voltage and current waveforms. They are one of the indispensable parts of high frequency systems including radars [1-3], commercial wireless communication tools such as cell phones, microwave heating devices [4,5] etc. Starting from 1900s, the need of microwave power is compensated by firstly magnetrons and then travelling wave tube amplifiers(TWTA) and klystrons all of which benefit from the movements of electrons in low pressure space [6,7]. By the invention of silicon bipolar three terminal transistors in 1960s, solid-state devices have become dominant actors in development of amplifiers due to their ease of implementation and higher degree of reliability. Research and development on wide variety of semiconductor materials including GaAs, InP, SiC and GaN provides the usage of solid state devices in high frequency regions of signal spectrum [8]. Moreover, improvements in semiconductor industry have led to discoveries of new production methods offering smaller, more reliable, more efficient devices that are easy to use, easy to package and cost effective.

Although TWTAs are still the primary choice for very high power-kW to MW range-amplifiers, promising semiconductor technologies offer high power density and have become candidates for TWTA replacements. Whereas GaAs devices which have become popular after 1980s provide approximately 1 W/mm at around 10 GHz, GaN transistors having considerable amount of research efforts all over the world offer >5

W/mm power density around 10 GHz. The rise in power density of semiconductor devices indicates that solid-state transistors will defeat TWTAs in high microwave power industry in near future.

1.2 WHAT GAN OFFERS

In the early 1990s, researchers have found that Gallium Nitride solid-state devices have promising material properties such as large energy bandgap, high electron mobility and high saturated electron velocity by the help of which the devices offer very high power density [9]. High energy bandgap refers high breakdown electric field on device drain-source channel enabling larger voltage swings during operation. Figure 1.1 summarizes the cut-off frequency versus voltage breakdown relationship for different type of semiconductor technologies. It can be concluded from the graph that very larger voltages can be applied to drain of GaN materials at very high frequencies.

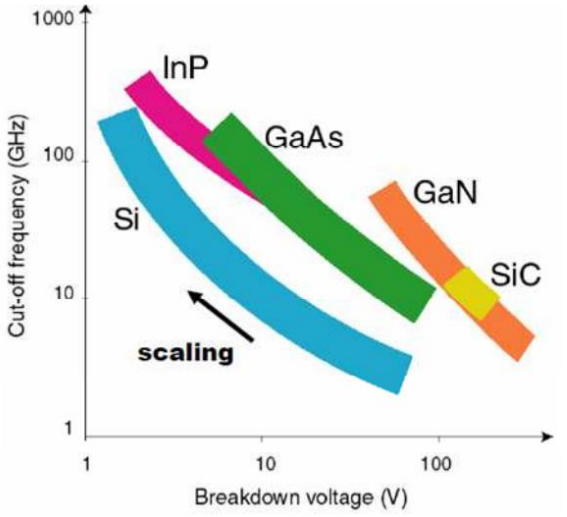


Figure 1.1 Voltage breakdown and cut-off frequency for different semiconductor materials [10].

Figure 1.2 gives information about the power density values provided by different semiconductor technologies. It can be observed that GaN devices have the highest power density among the other technologies for a given drain voltage.

High drain voltage operation allows lower current values which results in higher drain impedances. Since the ease of and bandwidth of the matching are determined by the ratio of two impedances that will be matched, GaN devices offer simpler matching networks and wider fractional bandwidths. Although aim of the power amplifier design is to obtain as much as power possible, due to the power dissipation on device channel, higher channel temperature is seen on channels of GaN devices. Therefore, cooling of the power amplifiers is significantly important in GaN power amplifiers [11].

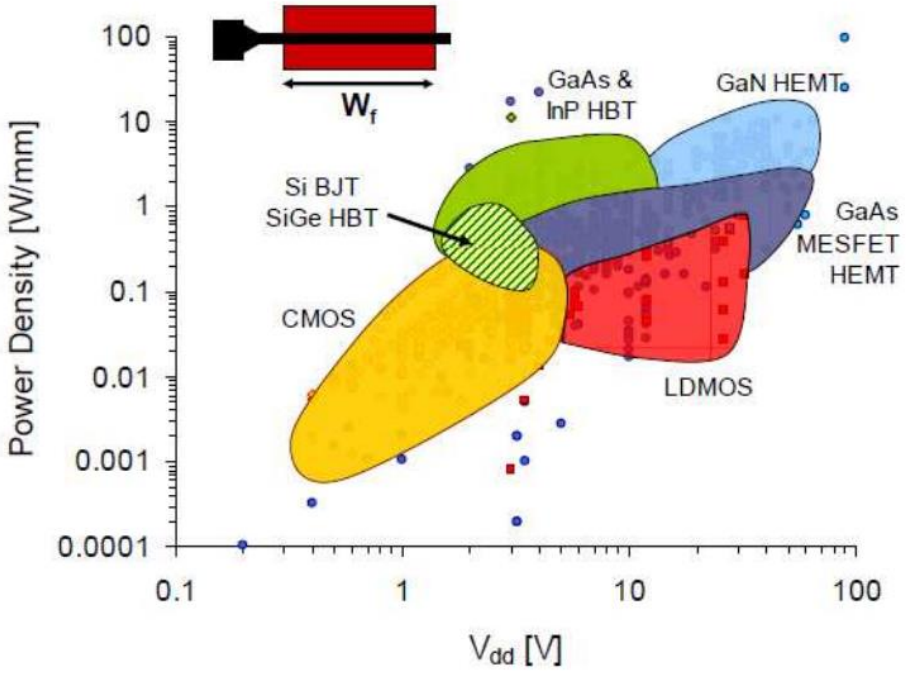


Figure 1.2 Output power vs frequency for state of the art semiconductor devices [10].

1.3 OUTLINE OF THE THESIS

The exciting features of GaN semiconductor material make it ideal for high frequency high RF power applications. In this work, it is aimed to design a power amplifier using a discrete GaN transistor and to evaluate its electrical performance and nonlinear characteristics from both device and system point of view.

In Chapter 2, basic parameters to evaluate electrical performance, some fundamental concepts to understand nonlinear behavior of power amplifiers and some issues related to PA operational conditions in a system are discussed.

In Chapter 3, a typical process to design and realize a microwave power amplifier is explained in a step by step manner. Therefore, Chapter 3 constitutes a design guide for a typical high frequency PA. This chapter also includes an introductory information on some fabrication issues to have a more reliable PA.

In Chapter 4, using the basis constructed in Chapter 2 and Chapter 3, an X-band high power amplifier is designed utilizing a nonlinear transistor model to illustrate the process defined in Chapter 3. This chapter also underlines the impotance of 3D accurate electromagnetic modelling to have a first pass design. Chapter 4 ends with the linear and nonlinear simulation results to be compared with the measurement results which is given in Chapter 5. In Chapter 5, results of various linear and nonlinear measurements are given to evaluate the performance of both GaN material and constructed PA at microwave frequency region. By the end of this chapter, the reader will have an idea on advantages and drawbacks of GaN semiconductor technology for PA applications.

Lastly, Chapter 6 summarizes the thesis and gives information about the future works to be done.

CHAPTER 2

POWER AMPLIFIER FUNDAMENTALS

Power amplifier is one of the most crucial components used in modern wireless communication systems including but not limited to mobile communication, radar, electronic warfare, satellite communication, medical imaging applications. Since requirements that must be satisfied by a power amplifier differs significantly from one application to another, different performance parameters must be optimized for each application.

Generally, power amplifier is a device that uses DC power to increase the power level of an incoming signal which is defined in a specific frequency band. More specifically, microwave power amplifiers are devices that operate in microwave frequency regime of radio frequency spectrum so that they are intended to use in high frequency applications.

Due to the fact that the primary aim of using a power amplifier is obtaining high power levels dictated from the application specifications, most of the time power amplifiers are used in large-signal conditions. Large-signal operation drives the transistors into nonlinear regions so that a distorted replica of incoming signal is obtained at the output of the power amplifier. Therefore, it is important to define how PA distorts the meaningful signal.

In addition to performance parameters, there are also stability issues, biasing effects and different operation modes that must be considered during PA design process.

In this chapter, basic performance parameters, distortion parameters are defined and classes of amplifiers, stability issues and operation modes for power amplifiers are also presented.

2.1 BASIC PARAMETERS

In Figure 1, basic power amplifier operation is shown using a simplified energy flow diagram. The mathematical relationship between output power and input power of the amplifier can be expressed as:

$$P_{out}(t) = G(t) \times P_{in}(t) \tag{2-1}$$

$P_{out}(t)$: $Output\ power\ in\ Watts$

$P_{in}(t)$: $Intput\ power\ in\ Watts$

$G(t)$: $Power\ Gain\ in\ \frac{Watts}{Watts}$

Since power levels that must be handled in applications ranges from micro-Watts to Mega-Watts, power is usually expressed in dB scale referenced to 1 mW. Therefore, the above relationship between input power, output power and power gain can be expressed in dB scale as follows:

$$P_{out,dBm} = G_{dB} + P_{in,dBm} \tag{0-1}$$

$P_{P_{out,dBm}}(f)$: $Output\ power\ in\ dBm\ as\ a\ function\ of\ frequency$

$P_{in,dBm}(f)$: $Input\ power\ in\ dBm\ as\ a\ function\ of\ frequency$

$G_{dBm}(f)$: $Power\ Gain\ in\ dB\ as\ a\ function\ of\ frequency$

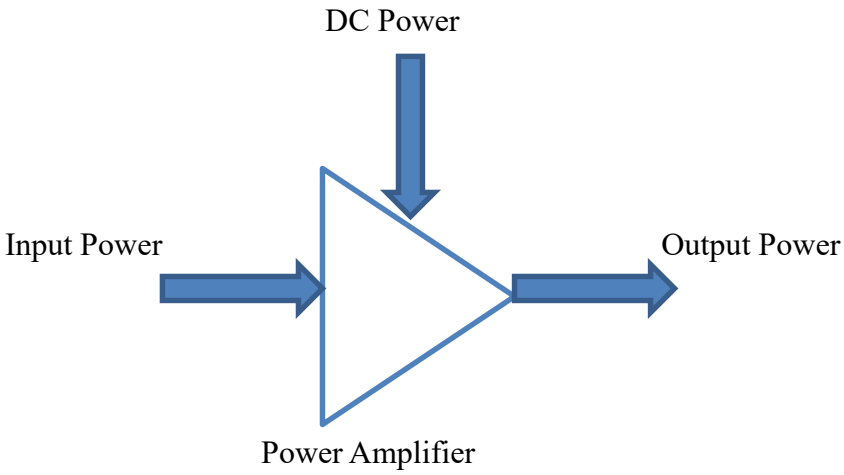


Figure 2.1 Basic operation of a power amplifier.

From equation (2-2), it is understood that as input power increases, output power increases continuously. However, this is not the case in practice since when high input power is applied, the amplifier saturates due to nonlinear behavior of the amplifier and gain compression occurs. This phenomenon is graphically depicted in Figure 2.2 for a typical amplifier. As it is seen, as input power increases and goes from small signal excitation region to large signal excitation region, power gain starts to compress.

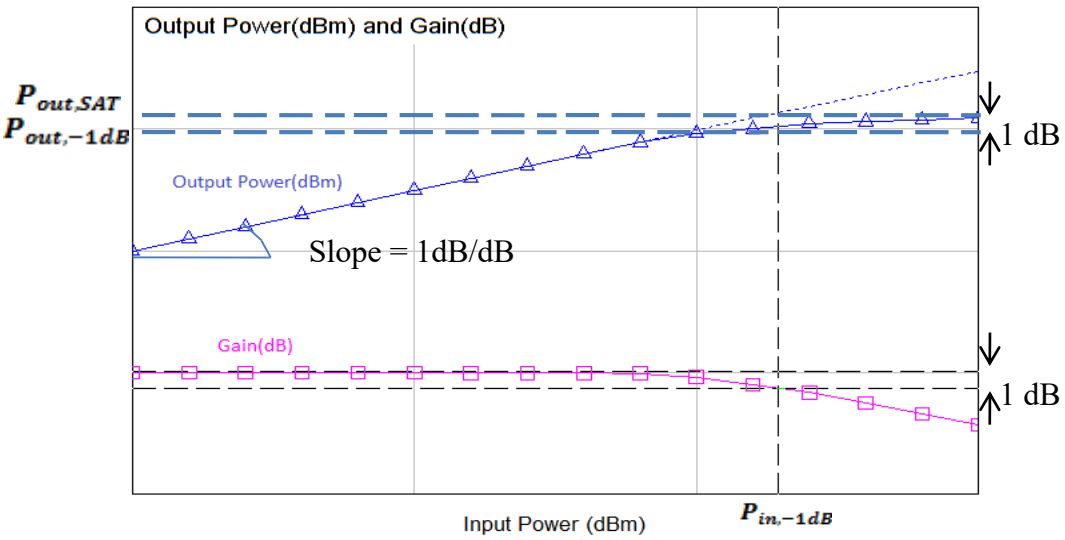


Figure 2.2 Input power, output power and power gain relation of a typical amplifier.

Two figure-of-merits called -1 dB compression output power level, $P_{out,-1\ dB}$, defined as the output power level deviated 1 dB from the ideal linear behavior and corresponding input power level, $P_{in,-1dB}$, are used to characterize the compression behavior of any amplifier. These parameters are also depicted in Figure 2 for a typical amplifier. The relationship between input power and output power at exactly 1 dB compression can be expressed in mathematical form as follows:

$$P_{out,dBm} = (G_{dB} - 1) + P_{in,dBm} \tag{2-3}$$

The other important parameter to characterize a power amplifier is saturation output power level, $\boldsymbol{P_{out,SAT}}$, which represents the maximum output power that can be extracted from an amplifier. As it is seen Figure 2.2, as input power increases, the output power reaches its 1 dB compression point and if input power increases further, output power saturates and reaches its maximum value. In general, power amplifiers are driven in large signal condition to obtain its saturated output power level.

As it is stated above, microwave power amplifiers convert provided DC power into microwave signal power but since some loss occurs during this conversion process, power amplification is not a perfectly efficient operation. Therefore, as a figure-of-merit for a power amplifier, drain/collector efficiency is defined as follows:

$$\eta = \frac{P_{out}}{P_{DC}} \tag{2-4}$$

To extract most of the available power from a power amplifier, the device needs to be driven with high input power levels so that input power level becomes comparable with output power and provided DC power. Therefore, another parameter, called "power added efficiency", is defined to take into account the contribution of input power in equation (2-5). Figure 2.3 shows output power, gain and efficiency parameters as a function of input power.

$$\eta_{add} = \frac{P_{out} - P_{in}}{P_{DC}} \tag{2-5}$$

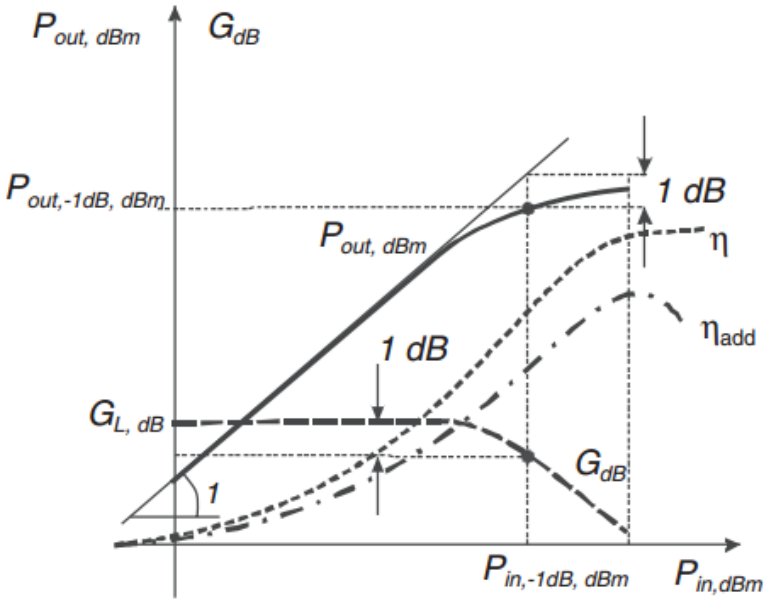


Figure 2.3 Relationship between efficiency parameters, output power, gain and input power for a typical amplifier [12].

2.2 DISTORTION PARAMETERS

Since power amplifiers operate at large signal region, output signal of a power amplifier is a distorted replica of input signal. The distortion occurs since voltage and current at the output of amplifier are clipped due to the intrinsic physical limitations of the semiconductor device. If operation of a power amplifier is modeled using a third order power series approximation, output voltage of the amplifier can be expressed as a function of input voltage as follows:

$$V_o = a_1 \times V_{in} + a_2 \times V_{in}^2 + a_3 \times V_{in}^3 \tag{2-6}$$

When the input signal is a single tone excitation;

$$V_{in} = A \times \cos(2\pi f t) \tag{2-7}$$

Output voltage will have the following form:

$$V_o = a_2 \frac{A^2}{2} + A \times \left(a_1 + \frac{3}{4} a_3 A^2\right) \times \cos(2\pi f t) + a_2 \frac{A^2}{2} \cos(2 \times 2\pi f t) + a_3 \frac{A^3}{4} \cos(3 \times 2\pi f t) \tag{2-8}$$

As it is seen in equation (2-8), even if power amplifier is excited by a single tone signal, DC, fundamental, second and third harmonic components are generated at the output. Input power and harmonic power components, assuming unit reference impedances, can be calculated using equation (2-8) as follows:

$$P_{in} = \frac{A^2}{2} \tag{2-9}$$

$$P_{out,f} = \frac{A^2}{2} \times \left(a_1 + \frac{3}{4} \times a_3 \times A^2\right)^2 \tag{2-10}$$

$$P_{out,2f} = a_2^2 \times \frac{A^4}{8} \tag{2-11}$$

$$P_{out,3f} = a_3^2 \times \frac{A^6}{32} \tag{2-12}$$

The power of fundamental component is a function of complex constants a_1 and a_3 together with input signal amplitude. In Figure 2.4, it is shown that $\frac{a_3}{a_1}$ must be smaller than zero to observe the compression characteristic of the amplifier.

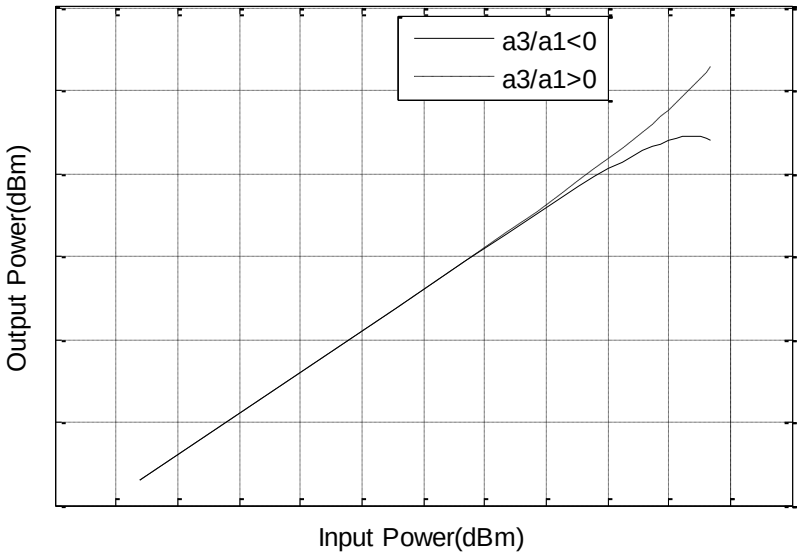


Figure 2.4 Fundamental output power for different parameter sets.

2.2.1 HARMONIC DISTORTION

As it is seen in equation (2-8), in addition to fundamental component, harmonic components are also generated by a PA as a response to single tone excitation. Harmonic distortion is measure of how much power generated at harmonic frequencies referenced to fundamental component power. According to harmonic distortion definition, n^{th} harmonic distortion, HD_{nf} , is defined as follows:

$$HD_{nf} \triangleq \frac{P_{out,nf}}{P_{out,f}} \tag{2-13}$$

Therefore, for a third order power series approximation, harmonic distortion for second and third harmonic components can be calculated using harmonic powers given in equation (2-10), equation (2-11) and equation (2-12) as follows:

$$HD_{2f} = \frac{P_{out,2f}}{P_{out,f}} = \frac{(a_2^2 * \frac{A^4}{8})}{\frac{A^2}{2} * \left(a_1 + \frac{3}{4} * a_3 * A^2\right)^2} = \frac{(a_2^2 * \frac{A^2}{4})}{\left(a_1 + \frac{3}{4} * a_3 * A^2\right)^2} \tag{2-14}$$

$$HD_{3f} = \frac{P_{out,3f}}{P_{out,f}} = \frac{a_3^2 * \frac{A^6}{32}}{\frac{A^2}{2} * \left(a_1 + \frac{3}{4} * a_3 * A^2\right)^2} = \frac{a_3^2 * \frac{A^4}{16}}{\left(a_1 + \frac{3}{4} * a_3 * A^2\right)^2} \tag{2-15}$$

In addition to harmonic distortion parameter defined for each harmonic component, Total Harmonic Distortion(THD) is defined as follows:

$$THD = \frac{\sum_{n=2}^{\infty} P_{out,nf}}{P_{out,f}} \tag{2-16}$$

In Figure 2.5, power levels of fundamental, second and third harmonic components are shown as a function of input power. Harmonic distortion parameters, HD_{2f} and HD_{3f} , are also shown graphically. As input power level increased, second and third harmonic power levels get closer to fundamental power level so that harmonic distortion increases.

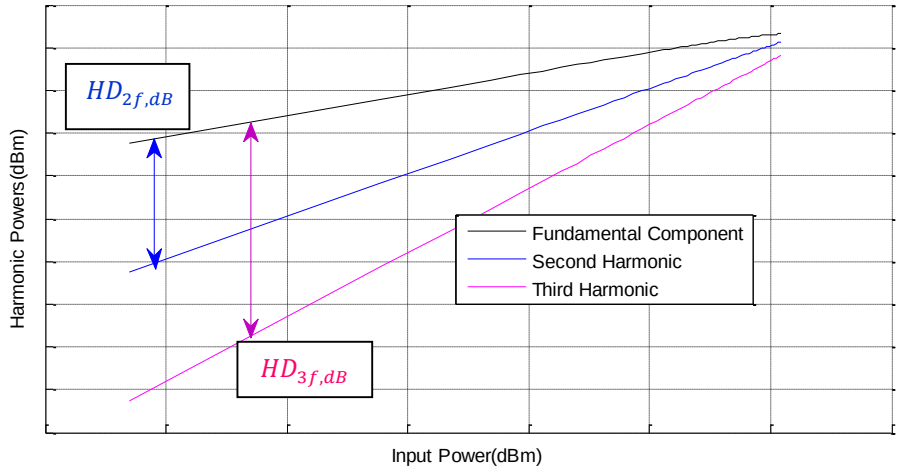


Figure 2.5 Fundamental, second and third harmonic powers as a function of input power.

2.2.2 AM/AM AND AM/PM

The third order power series approximation given in equation (2-6) defines a memoryless operation for a PA so some nonlinear effects cannot be seen using this approximation. In mathematical form, input and output signals of a PA can be expressed as follows:

$$V_{in}(t) = A(t) \times \cos(2\pi f t + \Phi(t)) \tag{2-17}$$

$$V_{out}(t) = G[A(t)] \times \cos(2\pi f t + \Phi(t) + \theta[A(t)]) \tag{2-18}$$

where;

$$G[A(t)]: Gain, nonlinear\ function\ of\ input\ signal\ amplitude,$$

$$\theta[A(t)]: phase\ change\ inserted\ by\ PA, nonlinear\ function\ of\ input\ signal\ amplitude.$$

The nonlinear behavior of gain is called as AM/AM and nonlinear behavior of phase change is called AM/PM conversions. The nonlinear behavior in amplitude is mainly due to the nonlinear transconductance and the nonlinear behavior of phase is primarily due to nonlinear behavior of internal capacitors and inductors included in the transistor model. The AM/AM and AM/PM curves for a typical power amplifier are shown in Figure 2.6.

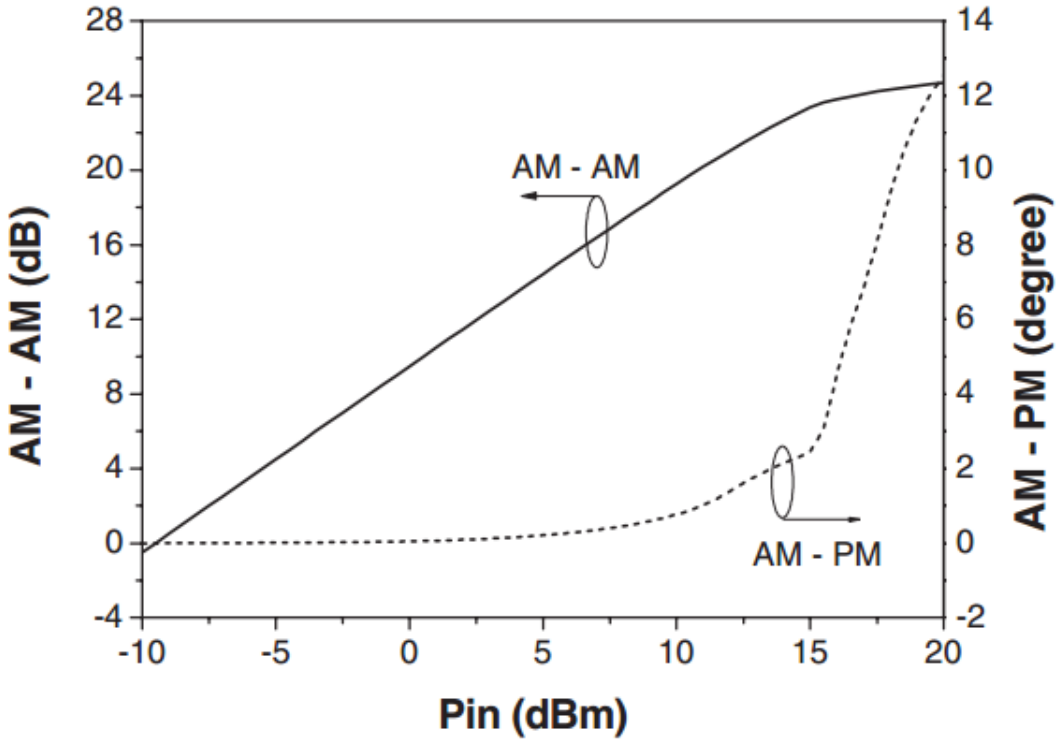


Figure 2.6 AM/AM and AM/PM characteristics of a typical PA [12].

Nonlinear, input drive dependent AM/AM and AM/PM characteristics are not desirable behaviors in communication systems since they directly affect the constellation diagram of a system. Moreover, in phased array systems, AM/PM conversion may dangerously effect the antenna beamforming ability so that the system performance degrades from expected.

2.3 POWER MATCHING

The power level that can be extracted from a transistor is determined by size of transistor and the technology used to produce the transistor. However, to extract all of the power available from transistor, output matching network of the transistor is needed to be designed carefully. In Figure 2.7, IV curves of a typical transistor are shown together with a bias point and three different load lines. Since load impedance of a transistor is defined as follows:

$$R_L = \frac{V_{ds}}{I_{ds}} \tag{2-19}$$

If Figure 2.7 is analyzed, it is seen that when full swing is generated for both voltage and current around the chosen bias point, maximum power is obtained from the transistor. Otherwise, all of the available power is extracted from the transistor cannot be extracted from the transistor. This condition is called as power matching so output matching network must be designed such that it allows full swing for both voltage and current waveforms.

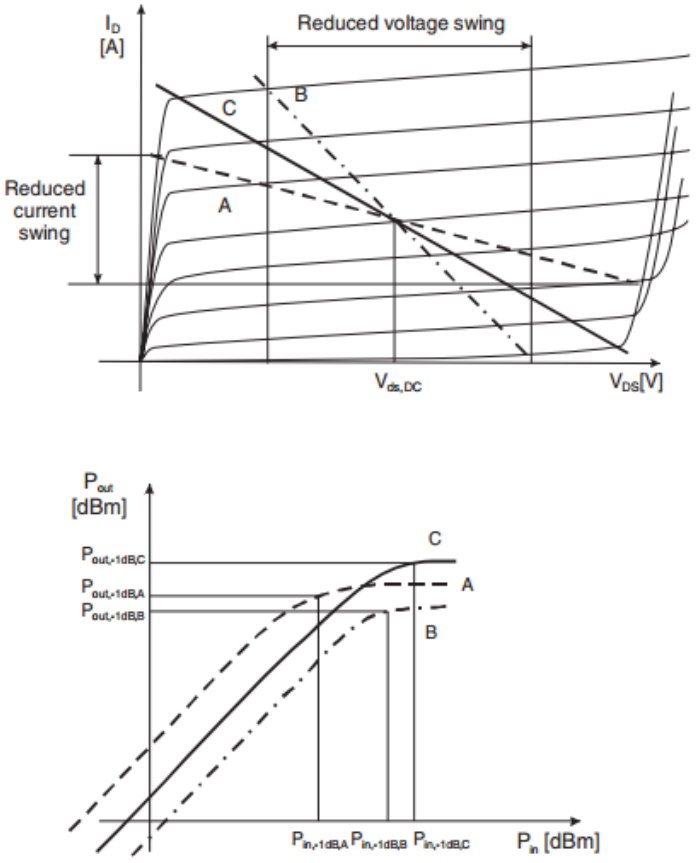


Figure 2.7 Different load lines and corresponding input/output power behaviors [12].

2.4 CLASSES OF AMPLIFIERS

Amplifiers are classified according to DC bias points and resulting current conduction angle (Φ). In Figure 2.8, drain current is shown as a function of both drain and gate voltages and resulting typical drain current waveforms are shown in Figure 2.9. Choice

of class of operation is a design decision depending on the efficiency, linearity and output power requirements of PA and significantly affects the amplifier performance. As in almost all engineering decisions, there is trade-off between efficiency, linearity and output power when choosing class of operation. Simply, as conduction angle decreases efficiency increases but linearity also falls down or vice versa. As it is seen in Figure 2.10, Class AB operation has highest output power, good linearity and moderate level of efficiency.

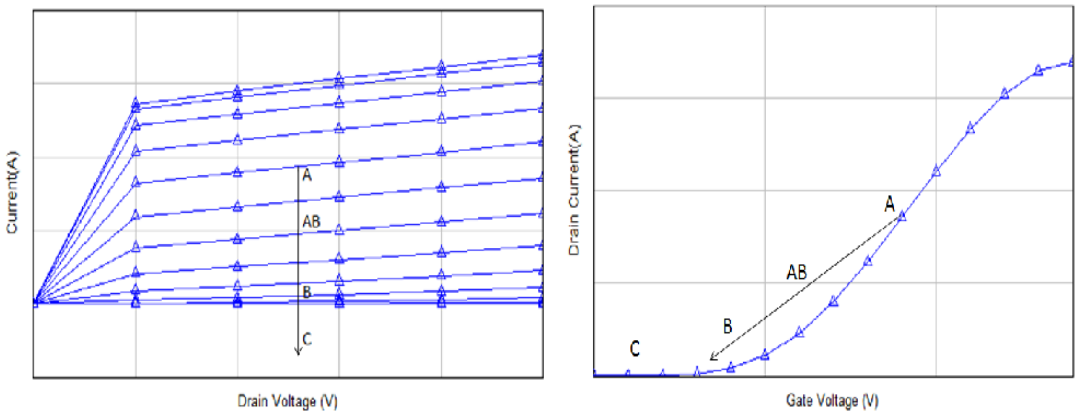


Figure 2.8 Drain current as a function of drain and gate voltages.

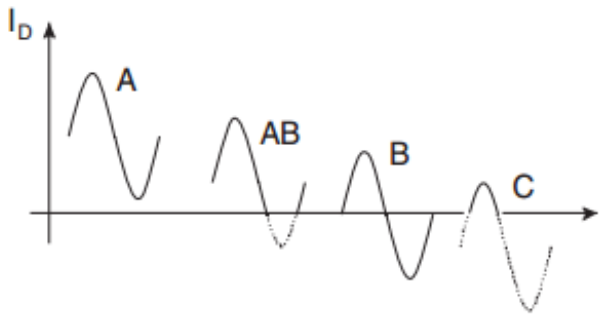


Figure 2.9 Drain current conduction angle for different bias classes [12].

In addition to classes defined by bias points, there are also another group of operation classes defined by harmonic terminations and dynamic conditions. There classes

include Class D, Class E, Class F modes and their analysis requires derivation of multi-harmonic voltage and current waveforms [13].

In literature, extensive analysis of all classes is done and their comprehensive comparison can be found [14].

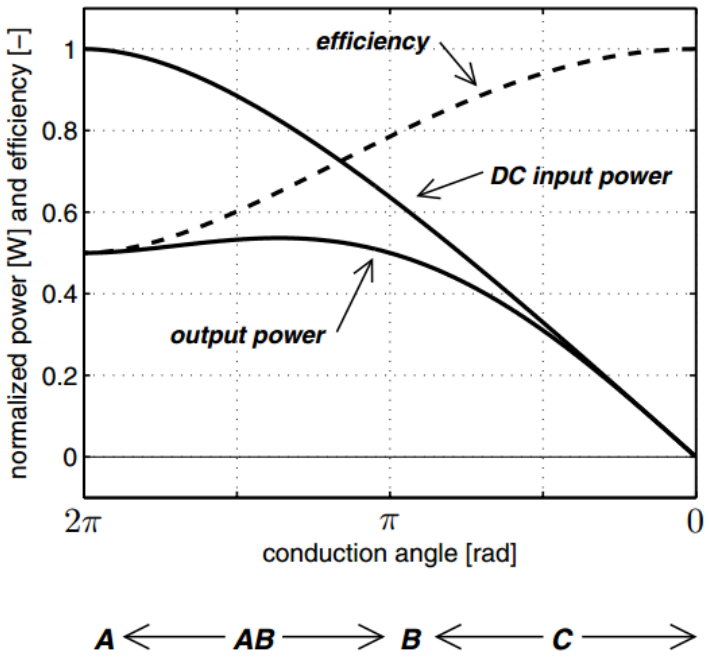


Figure 2.10 Output power, efficiency and DC power as a function of conduction angle [15].

2.5 STABILITY

The first and most important thing expected from a power amplifier is not to oscillate. Due to the internal feedback mechanism inside transistors, part of the output signal may be fed back to input side and if actual input signal and feedback signal may somehow have same phases then they will sum up and create oscillations. This process is created intentionally in oscillator circuits but for an amplifier it is hazardous and degrades the performance. Therefore, after the choice of class of operation, stability analysis on transistor must be done and a stability network must be designed if necessary.

When a circuit is unstable, the signal increases unlimitedly and drives the active devices into large signal operation or saturation. A power amplifier must be unconditionally stable meaning stable at all frequencies and at all source-load impedances. Out of the interested band must also be concerned when stability analysis is done since in operation one cannot know all incoming signals-out of band signals may also come- and impedances seen by amplifier. If an oscillation occurs following problems may be seen in circuit [16]

- The active device will be driven into saturation and circuit design will not be valid anymore since the circuit operates at a large signal condition at a frequency,
- Circuit will work noisier in the case of oscillation,
- Probably, unwanted large signal operation will damage the active device.

To investigate whether a transistor is possibly unstable, there are several methods one of which is called as *μ-factor*. *μ-factor* is an easy to analyze since the designer have to look at only one parameter to decide whether the active device is stable or not. The necessary and sufficient condition for stability for *μ-factor* is:

$$\mu = \frac{1-|s_{22}|^2}{|s_{11}-\Delta s_{22}^*|+|s_{21}s_{12}|} > 1 \tag{2-20}$$

$$where;$$

$$\Delta = s_{11}s_{22} - s_{12}s_{21} \tag{2-21}$$

Therefore, the designer must calculate *μ-factor* at all frequencies from zero frequency to much higher frequencies of interested band and add a stability network if necessary. In this work, *μ-factor* is used in design process to look at stability issues in the circuit.

Another important point about stability and *μ-factor* is that larger values of μ means a more stable circuit but as μ gets larger, maximum available gain(MAG) that can be obtained from the active device decreases. Therefore, in the interested band *μ-factor* must be large enough to ensure a stable operation but small enough to obtain high gain from the device. Out of band *μ-factor* may be much larger to have more stable

operation. In Chapter 4, some simulations will be presented to show the relation between *μ-factor* and MAG.

2.6 LOAD PULL TECHNIQUE

Load pull is a technique that is used to find the optimum impedances to be seen at drain and/or gate of the active device to minimize or maximize one or more of the performance parameters of an amplifier. This operation is realized using impedance tuner by which any impedance defined on Smith Chart can be obtained, ideally. The performance parameter might be output power for a power amplifier or efficiency to design a high efficiency power amplifier. The parameters that will be optimized might be different at gate and drain. For instance, the designer may want to maximize by controlling the impedance at drain side and want to maximize small signal gain by using the impedance at gate side. A typical load pull setup is shown in Figure 2.11 as a block diagram. There are two impedance tuners one which is located at output side and the other is placed at input side of the transistor. Basically, the tuner has to control the fundamental frequency component by covering almost all points on Smith Chart. In more advanced setups, the tuner can control one or more harmonics simultaneously.

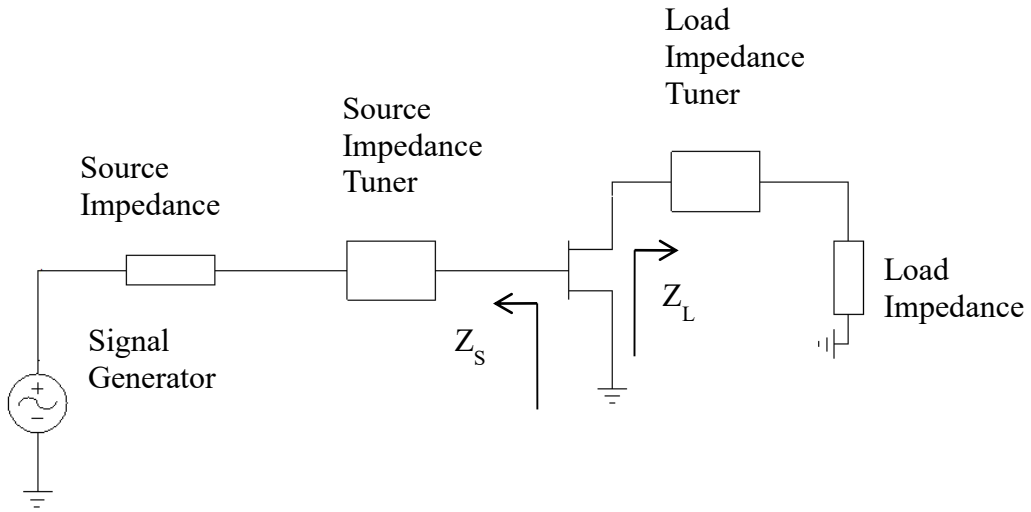


Figure 2.11 Load pull simulation or measurement technique block diagram.

Load pull data can be obtained by both nonlinear simulations or using load pull measurements. If nonlinear model is available for the transistor what will be used, then

modern CAD tools provide load pull simulations using built-in impedance tuner blocks. If nonlinear model is not available, then the designer has to set up a test bench to perform load pull measurements.

After the load pull simulations or measurements, the designer obtains load pull contours defined on Smith Chart and the optimization parameter- output power, efficiency, gain etc- is constant on those contours meaning that the impedances on a specified contour provide same performance. In Figure 2.12, two samples of tuner impedance points on Smith Chart are presented. On the Smith Chart a, it is pointed out by the impedance points that the tuner will travel along almost whole Smith Chart whereas on the Smith Chart b the tuner will focus on a smaller area defined by impedance points. In Figure 2.13, results of two sample load pull simulations are shown. The red curves represent the output power contours and blue curves represent the efficiency contours. As it is seen that the curves are located at slightly different regions so that maximum efficiency and maximum output power cannot be obtained simultaneously. The “X” points at the center of all contours depict the maximum output power and maximum efficiency values.

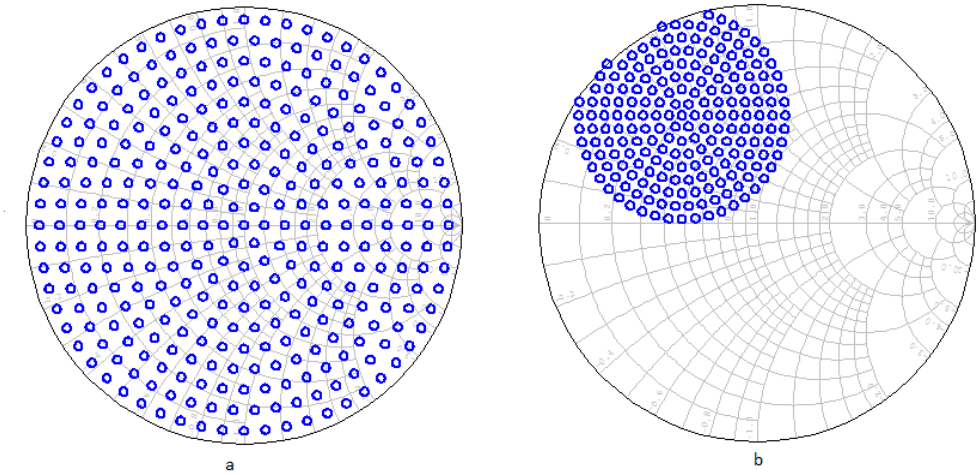


Figure 2.12 The impedance points which the tuner will travel on.

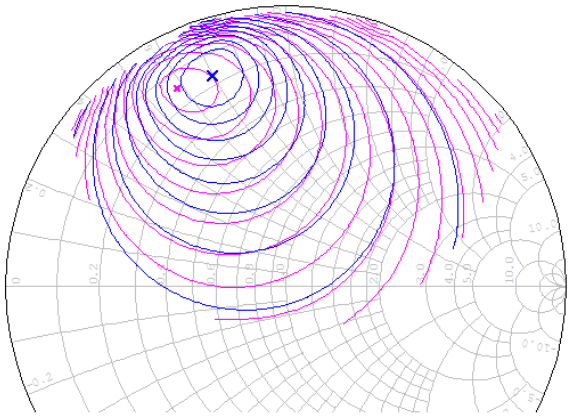


Figure 2.13 A sample load pull measurement result for efficiency and output power optimization.

Since transistors are bilateral devices and assuming they are completely unknown to the designer at the beginning of design, load pull process must be an iterative process. The designer should start with tuning the load impedances and then he should tune the source impedance by applying the previously found optimum load impedance. However, several iterations of same load/source pull tuning must be done since applied source(load) impedances probably change the optimum load(source) impedance point. After several iterations, impedances points will converge to optimum locations on Smith Chart.

2.7 CW AND PULSED OPERATION MODES

In wireless communication applications like radar, power amplifiers may basically work in two operation modes one of which is continuous wave (CW) and the other one is pulsed mode. In CW operation, both of input RF signal and supply voltage of amplifier is always ON. In pulsed operation, one of input RF signal and supply voltage or both of them are ON in predefined times and OFF in the other times.

In Figure 2.14, CW operation is simply presented by a block diagram. As it is seen, input RF signal and supply voltage of the amplifier is always ON and output signal is an amplified replica of input signal.

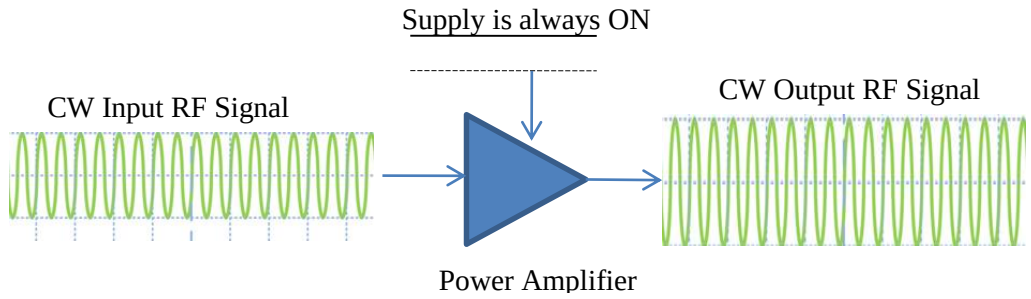


Figure 2.14 CW Operation of PA.

There are three techniques to have a pulsed PA operation. In the first technique, input RF signal is a CW signal and supply voltage of the PA is modulated meaning that it is continuously opened and closed so that an amplified and pulsed output RF signal will be obtained. First technique is presented in Figure 2.15.

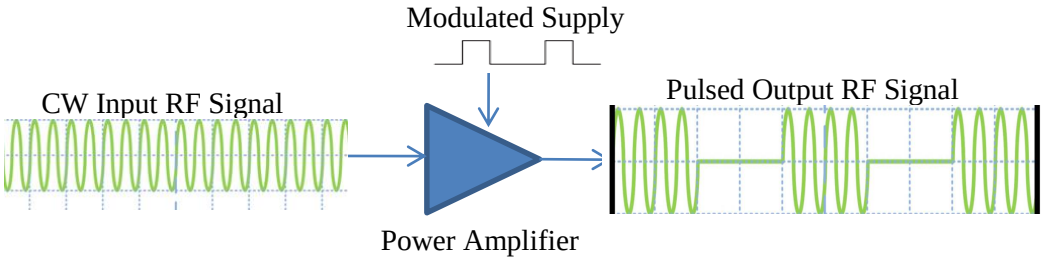


Figure 2.15 Pulse operation with only supply modulation.

In second pulse operation technique, supply voltage of the PA is always ON and input RF signal is modulated so that again an amplified and pulsed output RF signal is obtained. This technique is presented in Figure 2.16.

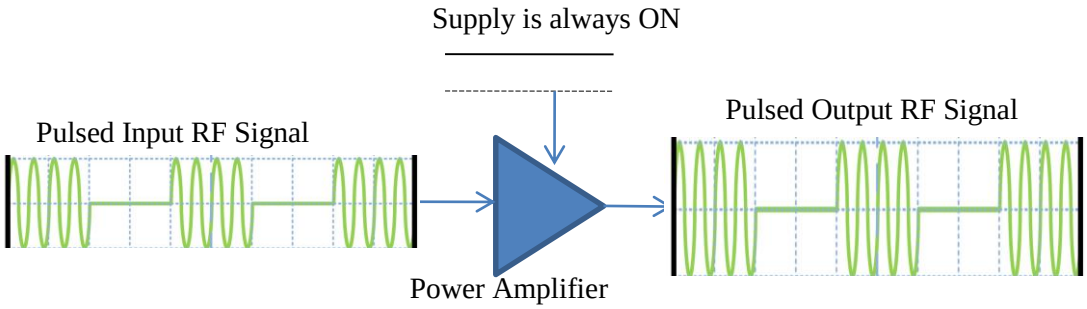


Figure 2.16 Pulse operation with only input RF signal modulation.

In the last technique, both of input RF signal and supply is modulated simultaneously so that an amplified and pulsed RF signal is obtained at the output of the PA. This technique is presented in a block diagram in Figure 2.17.

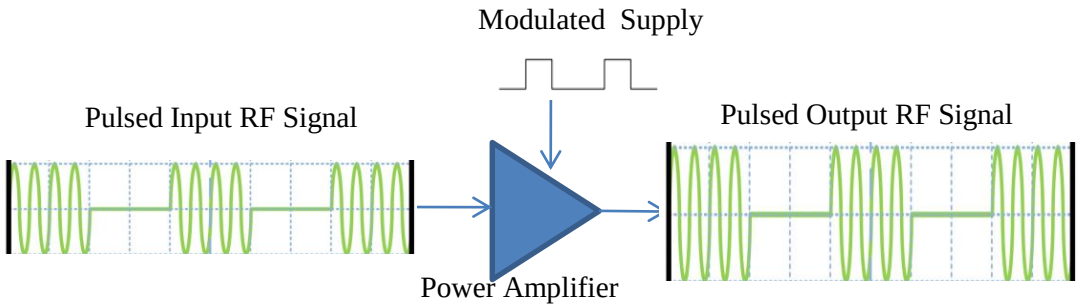


Figure 2.17 Pulse operation with both input RF signal and supply modulation.

There are some parameters related to pulsed operation. The first parameters that need to be defined are pulse width(PW) and pulse repetition interval(PRI). PW means the amount of time that PA will be ON or operate. PRI means the total amount of time that PA will be ON or operating and OFF or non-operating. These parameters are depicted graphically on Figure 2.18. There are also duty cycle and pulse repetition frequency parameters that are closely related to PW and PRI as follows:

$$PRF = \frac{1}{PRI} \tag{2-22}$$

$$duty\ cycle(\%) = \frac{PW}{PRI} * 100 \tag{2-23}$$

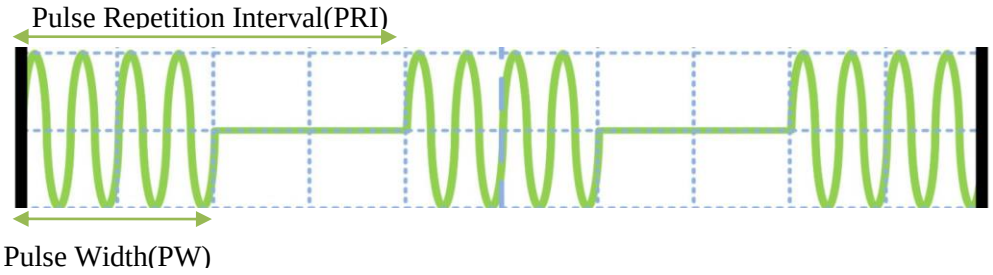


Figure 2.18 Pulse parameters.

Obviously, the last pulse operation technique is more complex than the others but it is a more efficient and more spectrum friendly technique. It requires a more complex

circuitry because the designer needs to implement a supply modulation circuit that can handle voltage and current levels that PA requires and can also satisfy the timing requirements such as rise and fall times of pulse, minimum/maximum PWs and PRIs. In addition, input RF signal must also be modulated which means designer needs to have a fast RF switch or a RF modulator circuitry.

The second pulse operation technique requires only RF signal modulation and its supply voltage is always ON. However, since its supply is always ON, the PA always draws current from the supply so that more DC power is used by PA.

In Figure 2.19, envelope of a typical RF pulse seen at the output of PA is shown. Output of a supply modulation circuit is a second order RLC network and sudden current changes during rise and fall times which results in ringing on supply voltage. This possibly small ringing on supply voltage also modulates the output RF signal and there will be frequency components f_r (frequency of ringing) away from the center frequency. The first pulse operation technique, because of previously described ringing issue, is not spectrum friendly.

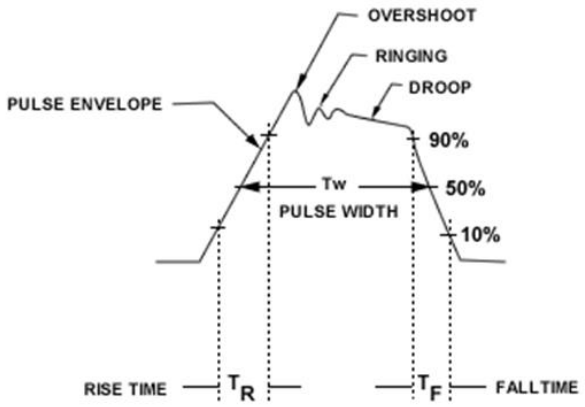


Figure 2.19 Typical PA output pulse envelope shape.

2.8 COMPARISON OF SEMICONDUCTOR MATERIALS FOR PAs

In any application satisfying requirements of PA needs careful selection of semiconductor material and technology. In addition to electrical performance requirements, there may be some other requirements on environmental conditions like temperature or overall PA cost. Therefore, semiconductor technology must be chosen such that it addresses all environmental, economic and electrical performance requirements.

Nowadays, PAs that will be mass-produced largely designed using silicon (Si) and gallium arsenide(GaAs) based semiconductor materials. In addition, wide bandgap materials such as gallium nitride(GaN) and silicon carbide(SiC) are also developed by research centers and some semiconductor materials and they provide performance advantages at microwave frequencies whereas their cost is still relatively high.

On Table 2.1, some properties of semiconductor materials are presented [17]. Energy bandgap is the required energy to transfer one electron from valence band to conduction band and wider bandgap implies larger operating voltages resulting in high power densities. Large operating voltage also results in large load impedances which makes matching network design process easier. As power density levels on devices are increased, heat generation is also increased so designer needs to have higher thermal conductivity to effectively move away the generated heat. High mobility implies low ON resistance on transistor channel and low ON resistance results in low loss. Moreover, high substrate resistance means a good insulator and it decreases substrate losses.

Table 2.1 Comparison of Semiconductor Materials.

Property	Si	GaAs	GaN	SiC	InP
Electron Mobility ($cm^2 V^{-1}.s^{-1}$)	1500	8500	1000	900	5400
Hole Mobility ($cm^2 V^{-1}.s^{-1}$)	450	400	350	120	200
Energy Bandgap(eV)	1,12	1,42	3,2	3,23	1,35
Saturated Drift Velocity(10^7 cm/s)	1	2	1,8	0,80	2
Thermal Conductivity(W/cm.°C)	1,40	0,45	1,7	4,90	0,68
Dielectric Constant	11,90	12,90	14	10	8
Substrate Resistance(ohm)		>1000	>1000	<20	>1000

CHAPTER 3

HIGH FREQUENCY POWER AMPLIFIER DESIGN

In previous chapter, fundamental parameters and operation of PAs are described to understand the what and how PAs do. In this chapter, from definition of requirements to prototyping, fundamental steps for the realization of PA will be discussed.

PA design is a multi-step procedure any of which affects significantly the final performance of PA. If any one of these steps is not done carefully and meticulously, the designer will spend so much time on iterations, going back and re-designing the problematic parts.

Moreover, since this work is mainly about the high frequency PA design, high frequency circuit modeling and simulations will also be discussed in this chapter. To have a first-pass-design PA, meaning a PA that works without or small amount of post-tuning, the designer needs to spend significant time on circuit modeling and electromagnetic (EM) simulations.

Prototyping of PA requires some special considerations to have a more reliable operation. Therefore, as a final topic some prototyping issues will be discussed in this chapter.

3.1 DESIGN PROCESS

PA design process starts with definition of requirements and ends with a PA which is validated to show that it satisfies the requirements defined initially. In Figure 3.1, PA design process is divided into basic steps to give an idea about the PA design journey. In following subheadings main steps will be discussed in more detail.

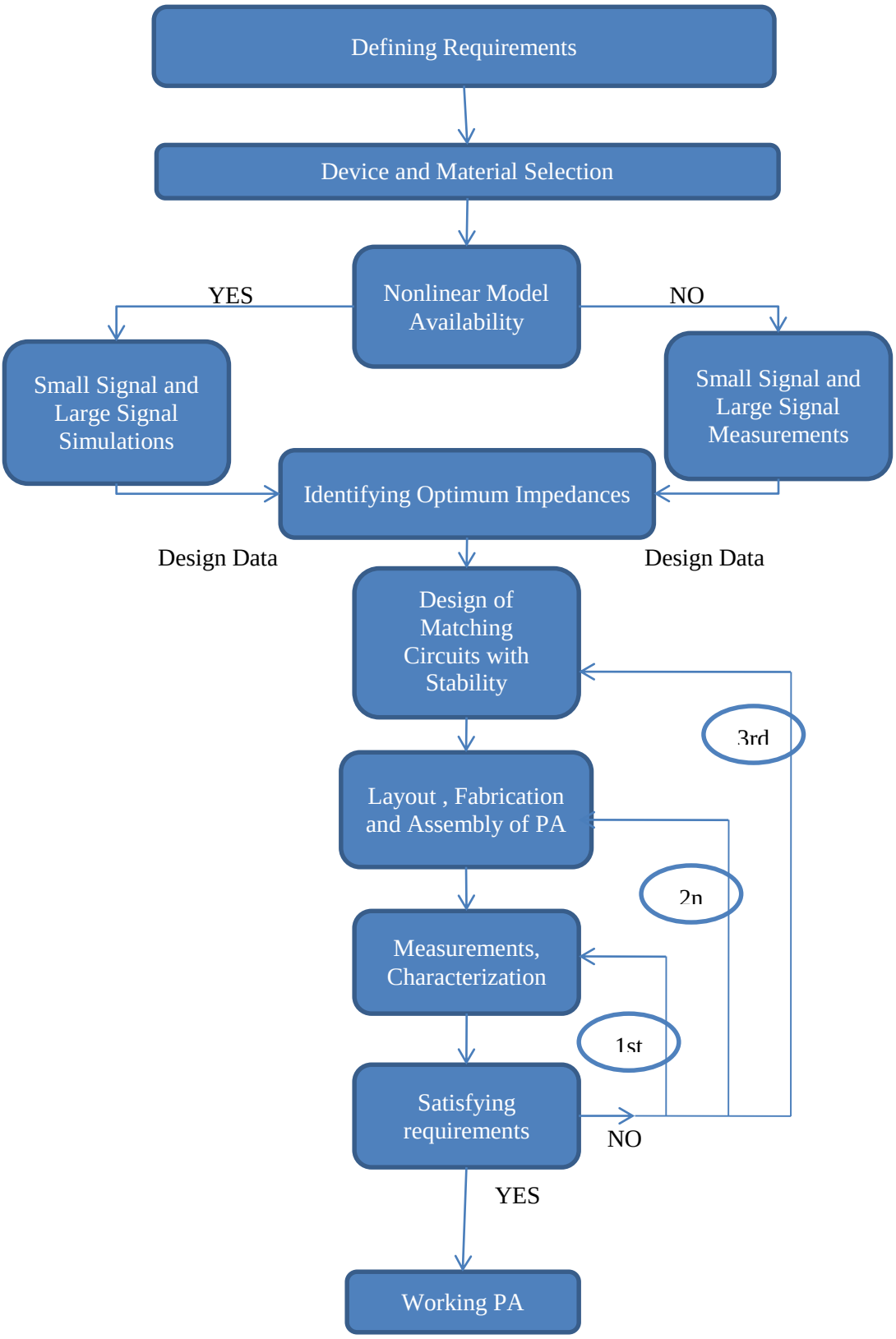


Figure 3.1 PA design process as a block diagram.

3.1.1 REQUIREMENTS

As it is defined in Chapter 2, there might be some performance requirements such as output power, efficiency, bandwidth, gain or parameters related to linearity that are expected to be satisfied by the PA. In addition to electrical performance requirements, there may be some constraints on final mechanical size of the constructed PA. Moreover, for operating ambient temperature or operating case temperature range, there may be some values so that some thermal precautions have to be taken to have a reliable operation. At the very beginning of the design, these requirements must be defined and finalized carefully since they will setup a base for the rest of the design process. All of the design decisions such as technology and material selection, mechanical housing construction and even measurement setup structure will depend on the requirements of the PA.

3.1.2 DEVICE AND MATERIAL SELECTION

Focus of this thesis work is *hybrid* microwave power amplifier so that device and material selection includes two decisions one of which is semiconductor material, technology and device selection and the other one is PCB material selection.

As a first step, the active device, the transistor, which will be used, must be chosen such that it is able to provide expected output power, efficiency, gain and linearity requirements as well as other reliability related requirements. In Chapter 2, some semiconductor materials and some of their parameters are presented and compared. Using those parameters and looking at transistors that semiconductor manufacturers offer the designer must choose a proper device. For instance, if high power density is required GaN devices might be solution with relatively high cost. If the power requirement is relatively low but cost is the primary concern, a GaAs device might be good choice. In addition, upper limit of operation frequency of transistors must be also examined whether their operation band coincides with the project center frequency and bandwidth or not.

Moreover, PCB material selection is the second primary choice before working on design. On Table 3.1, some PCB materials and their characteristics are given to compare them. Dielectric constant of the substrate material determines the

characteristic impedance of a microstrip line together with height of the substrate. As dielectric constant becomes larger, same characteristic impedance can be synthesized using a narrower microstrip line. For instance, wide transistors with high output power need to see low load impedances to microstrip lines with low characteristic impedance must be used at matching circuits. When a PCB material with high dielectric constant is chosen, those lines will be easier to realize. Furthermore, loss tangent affects the dielectric losses introduced by substrate material. As loss tangent decreases, lower loss will be introduced.

Thermal conductivity of the material is an important parameter since the dissipated energy on matching circuits will be converted to heat which needs to be transferred to *cold plate* as efficient as possible. As thermal conductivity of material increases, thermal resistance will decrease and the temperature difference between bottom metal and top metal of circuit will decrease meaning the heat transfer becomes more efficient.

Since the active device and PCB will be mounted on a mechanical body and significant amount of heat is generated during operation, thermal expansion in mechanical body and PCB will occur. Therefore, thermal expansion coefficients of both materials used to construct mechanical body and PCB must be well-matched not to have mechanical damage on PCB.

In addition to substrate material used in PCBs, conductor materials on substrate are also important to build PAs since they will also introduce loss on matching circuits. Therefore, conductor stack-up must be chosen carefully to decrease the loss.

As a final note, before starting to a PA design, the designer must look for PCB manufacturers to find out available materials, production tolerances and design rules of manufacturer not to design a circuit being not realizable.

Table 3.1 Some substrate materials and their properties.

	Substrate Materials			
Property	**Alumina**	**RT/Duroid 5880**	**RT/Duroid TMM10i**	**RT/Duroid 4003C**
Dielectric Constant	9,9	2,2	9,8	3,55
Dielectric Loss(Loss Tangent)	0,0001	0,0009	0,0020	0,0027
Thermal Conductivity(W/mK)	26,6	0,2	0,76	0,64
Coefficient of Thermal Expansion(ppm/°C)	8,2	X=31, Y=48,Z=237	X=16, Y=16,Z=20	X=11, Y=14,Z=46

3.1.3 DESIGN DATA GATHERING AND CIRCUIT DESIGN

To start the design of circuit blocks of a PA, the designer needs to analyze, measure/simulate the transistor to gather design data such that the S-parameters, stability factor, optimum impedances, maximum available power and gain from the device.

Some semiconductor manufacturers provide nonlinear models using which the designer can make small signal and large signal simulations. By using nonlinear model and simulation results the designer can get all the information and data, assuming the model is accurate enough, required for the design.

If nonlinear model of the transistor is not available, the designer must measure all the small signal and large signal data needed for the PA design. Although measuring the device is much more time consuming than simulating the device, the designer will know that the data obtained by measurements are correct. In addition, during measurements, the designer can generate the environmental conditions same as the operating conditions of PA, so that final performance of the PA will be better estimated.

Therefore, if a transistor nonlinear model is proven to be accurate then PA design process will be easier and shorter for the designer.

When the designer has the data then matching circuits, stability network, gate and drain bias network could be designed. Functions of circuit blocks will be explained in following sections. Since this thesis work is about design of microwave PAs, high frequency electromagnetic simulations will also be discussed later.

3.1.4 FABRICATION AND MEASUREMENT

When the design of all circuit blocks are finalized, layout must be constructed and mechanical structure of the PA must also be considered. Layout of the circuits will determine the dimensions of the mechanical structure so if there is size limitation in requirements then layout must be drawn accordingly.

Using the size and shapes of the generated PCB layouts, a mechanical housing must be designed. However, in addition to size and shapes, thermal effects and size of the waveguide structures generated inside the mechanical structure must also be considered. Size of waveguide must be arranged such that any of the waveguide modes should not be excited not to lose energy.

If PCBs and mechanical housing are fabricated, then all of the components will be assembled to construct the PA. After assembly of the PA, test setups must be formed to measure the performance of the PA. The measurement parameters will be determined by the requirements identified at the very beginning of the design process. There is not a unique, universal PA measurement setup so structure of the test setup, measurement devices to be used will be determined by the designer and the parameters that will be measured. Moreover, one must be careful when constructing the setup and need to estimate the power levels at each node on each element in the setup not to burn out any of the devices due to high DC and RF power flow. Most probably, cooling will be necessary in the setup during measurements not to damage the PA because of excessive temperature values.

It is expected and desired that the PA satisfy the all requirements. If PA does not satisfy the requirements, then the first thing to do is finding out the reason why PA does not

work as expected and trying to make the PA satisfy the requirements by post-tuning on circuits which is a process generally done by using gold disks to make small modifications on matching circuits to work as expected. However, post-tuning works only for small performance shifts from the expected performance parameters, which is mainly caused by PCB manufacturer tolerances and assembly tolerances. If the problem is not solvable by post-tuning, then re-designing the layout or re-designing the matching circuits will be unavoidable. Since re-designing, re-fabrication and re-assembly is a time-consuming and costly process, the designer needs to spend time on modeling and simulations to have a PA that works in first run.

3.2 DESIGN METHOD

There are several methods to design the matching circuits to build a PA. In order to design matching circuits, the designer needs large-signal data of the active device since the PA will operate under large-signal drive.

If nonlinear, large-signal model or large-signal measurement data are not available then the designer may calculate load pull contours of the transistor by using the method described in [18]. By using this calculated, approximate load pull data, matching circuits can be designed.

The other method that could be used when large-signal model or data is not available is using the load line method [19]. In this method, the designer needs to define voltage and current waveforms on drain-source channel of the transistor using the DC bias voltage, current and resulting load line and then calculate the optimum load impedance that will be shown to transistor to have the power match condition, which is described in Chapter 2. The problem of load-line method is that the calculated optimum load impedance is defined on the current source plane of the transistor. In Figure 3.2, a simple model for a FET device is presented. By load line method, optimum load impedance is calculated at DS plane so the designer needs to translate this impedance D'S' plane by de-embedding device output resistance g_{ds} and output capacitance C_{ds}. At microwave frequencies, as wavelength decreases, device parasitic components also become critical since they will generate another plane D''S'' which is the plane that the designer can reach physically. The parasitic network shown in Figure 3.2,

consisting parasitic inductance, capacitance and resistance seen on device output, will also translate the impedance seen at D'S' to another impedance at D''S'' so the designer needs to model the parasitic components at the output of the device to calculate Z_L'' which is the actual optimum impedance from the designer perspective. Therefore, load line method cannot be used directly at microwave frequencies, where wavelength is comparable with active device physical size, due to the parasitic components and requires modeling of parasitic components network.

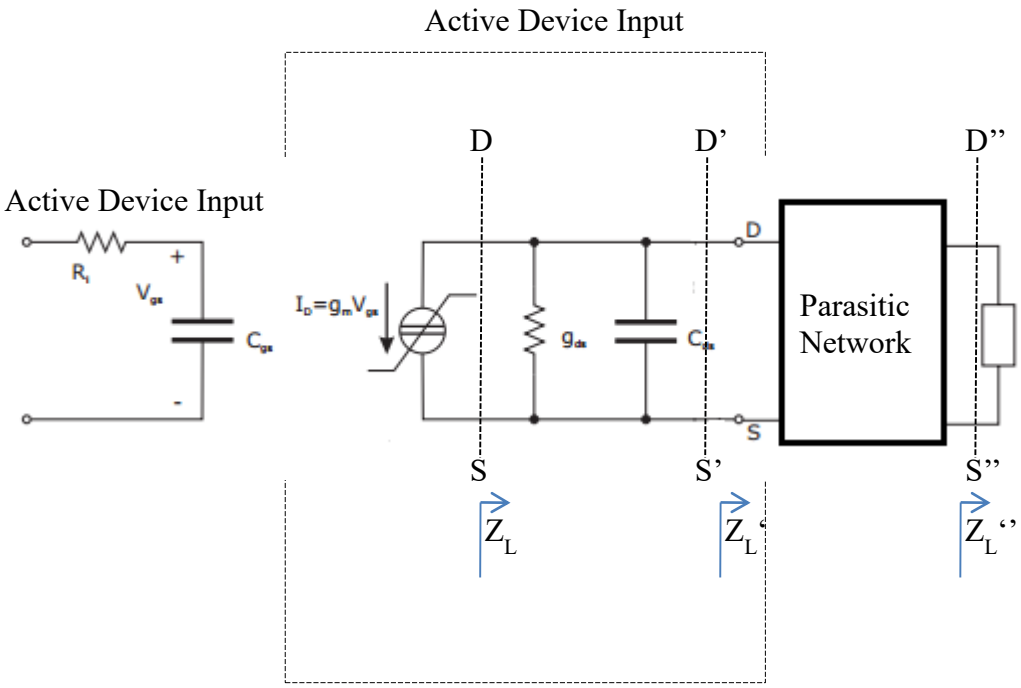


Figure 3.2 FET simple device model with parasitic elements.

If a nonlinear model is not available but the designer is able to do large-signal load-pull measurements, then the data obtained from the measurements could be used to design matching networks.

In this thesis work, nonlinear model of the transistor is available and used for the PA design. The nonlinear model provides small-signal, large-signal and load-pull simulations using a CAD tool so optimum impedances can be obtained directly in simulation environment. In addition, using a nonlinear model, a complete amplifier circuit with all circuit blocks can be constructed and simulated for output power,

efficiency, both small signal and large signal gain. Therefore, availability of a nonlinear model greatly simplifies the design process and reduces the design cycle time significantly.

In Figure 3.3, a load pull simulation schematic constructed in a modern CAD tool is presented. As it is seen on the figure, there are two impedance tuners one of which is used to tune the load impedance of the transistor and the other is used to tune the source impedance of the transistor. Moreover, the tuners can be used for first, second and third harmonic impedances simultaneously. The tuners are used iteratively to find both optimum load and source impedances to be shown to the transistor. Furthermore, the tuner can be used to find optimum impedances for any of the PA parameters such as output power, efficiency or gain. For example, in one application, the designer may want to find the optimum load impedances for maximum output power and in another application, the designer may want to tune efficiency of the PA.

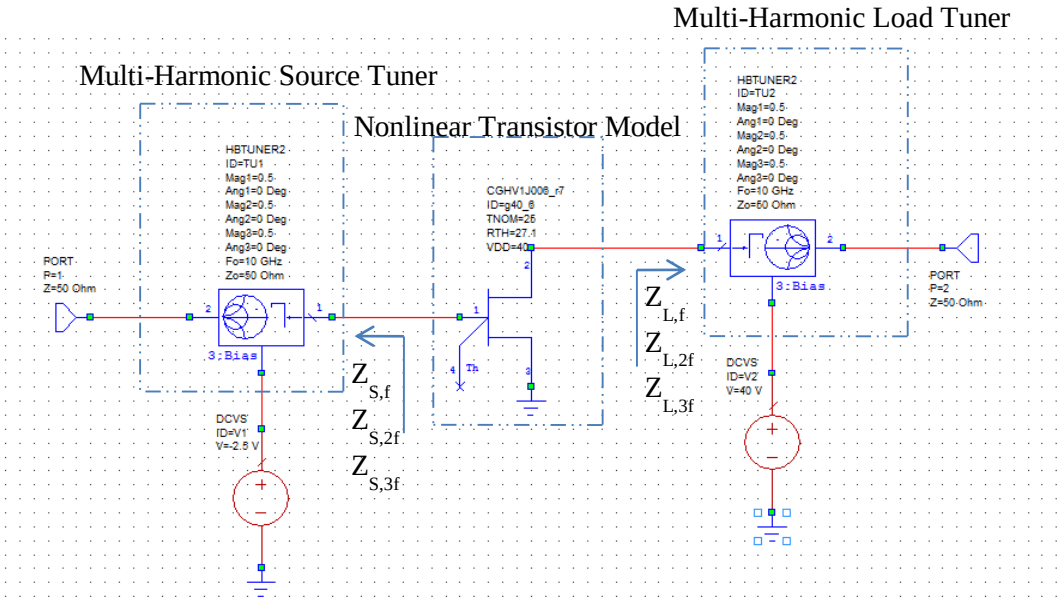


Figure 3.3 Load pull simulations in a modern CAD tool.

3.3 CIRCUIT BLOCKS

A PA device can be divided into meaningful circuit blocks to better understand the internal dynamics of a PA. Figure 3.4 represents the basic circuit blocks involved in a typical PA. The circuit diagram and their placement on the schematic is not unique

for an amplifier design but it is usually used topology for high frequency PA designs. This topology is also used for the PA designed as a part of this thesis work.

At output side of a PA, there is an output matching network to transfer the load impedance, usually 50 ohms, into optimum impedance seen by the transistor and a drain bias network to apply the drain bias voltage. These two network blocks, output matching network and drain bias network, can be integrated and may both match the impedances and bias the transistor. In this case, bias network will be a part of the output matching network. However, in this work, they are treated as different circuit blocks to explain the functions of each one.

At the input side of PA, there is a stability network in addition to input matching network and gate bias network. As explained in Chapter 2, stability network is designed such that it provides unconditionally stable operation for PA.

At each side of the PA, there are DC block capacitors that block the DC component of the both incoming and outgoing signals and only let RF signals to propagate.

In this section, each component represented in the block diagram of a typical PA in Figure 3.4 will be explained in more detail.

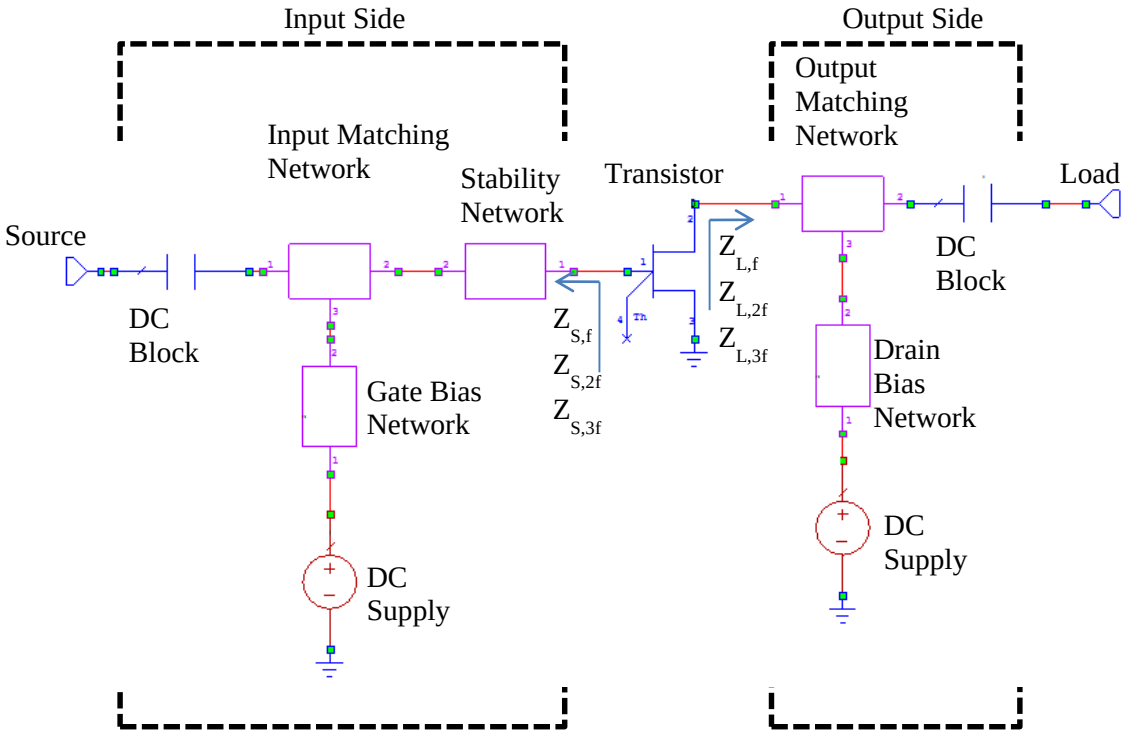


Figure 3.4 A typical PA circuit with all blocks.

3.3.1 STABILITY NETWORK

To obtain a PA device which is unconditionally stable at all frequencies and at all impedances seen by transistor, the designer, most probably, needs to add a stability network to the circuit. In Figure 3.5, two different stability network topologies are shown. Due to the ease of implementation using microstrip circuits, the stability network topology shown in the Figure 3.5-a is chosen in this work.

Equivalent series impedance of the RC network can be formulated as follows:

$$Z_{eq} = \frac{R}{1+w^2*R^2*C^2} - j\frac{w*R*C}{1+w^2*R^2*C^2} \quad (3\text{-}1)$$

Real part, resistance, of this equivalent impedance will add loss to the input side of the PA. Since transistors usually have higher gain at low frequencies and available gain decreases as frequency increases, transistor needs high resistance at lower frequencies and lower resistance as frequency increases to provide stability. As it is seen in equation (3-1), resistance decreases as frequency increases meaning reactance of the

capacitor gets closer to short. This is what PA needs due to available gain-frequency relationship. Therefore, proper choice of R and C in stability network provides unconditionally stable operation.

In reality, as frequency increases, physical sizes of circuit elements will become comparable with wavelength and all circuit elements will behave as distributed elements. The proposed R-C network will be designed and realized using distributed resistance and capacitance which will have parasitic components around actual elements. For instance, both of the R and C will have inductances and additional shunt capacitances. The parasitic inductances and actual capacitance C may resonate and constitute an open circuit at the interested frequency band. This will cause that only the series resistance is effective so very high loss will occur which is not acceptable. In short, the circuit elements must be carefully modeled to see the effects of parasitic components and actual high frequency behavior of the network.

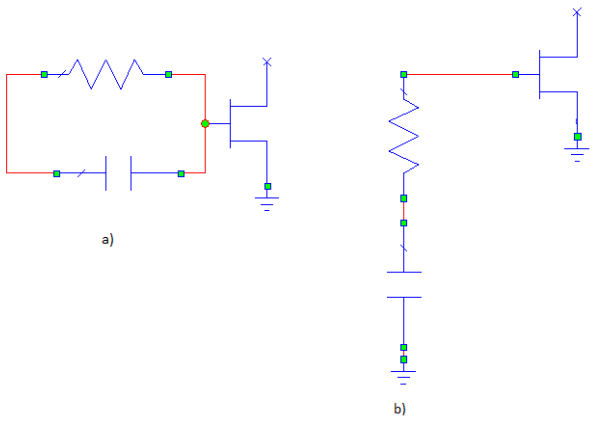


Figure 3.5 Stability network topologies.

3.3.2 MATCHING NETWORKS

Both of the input and output matching networks are responsible for realizing the optimum impedances, which are determined by load pull data, at gate and drain of the active device. In addition to optimum impedances, the designer needs to have low loss matching elements in order not to lose power at the output or input stage. Since lumped elements are not usable at microwave frequencies due to their physical sizes,

distributed elements such as series transmission lines, short or open stubs are used as matching elements.

Using single stub or double stub lossless matching networks are one way to match the complex impedances each other. They can be easily realized using microstrip series lines and stubs One section of single stub matching network cannot provide wideband matching so a multi-section network must be used to obtain impedance matching over a wide bandwidth. In Figure 3.6, an open, single stub matching network is shown and in equation (3-2) its input impedance is formulated.

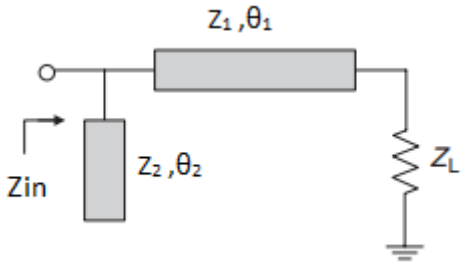


Figure 3.6 Single, open stub matching network.

$$Z_{in} = -j * Z_2 * \cot\theta_2 + Z_1 * \frac{Z_L + j * Z_1 * tan\theta_2}{Z_1 + j * Z_L * tan\theta_2} \quad (3\text{-}2)$$

Secondly, quarter wavelength transformers can be used as impedance matching elements as shown in Figure 3.7. There are several ways such as Binomial and Chebyshev methods to calculate the characteristic impedances of the quarter wavelength lines which match the two impedances to each other. To obtain a wide bandwidth matching performance, one must use multi-section quarter wavelength impedance transformer. Quarter wave length matching techniques are analyzed analytically in literature [20]. In Figure 3.7, a four section impedance transformer is presented. The problem with quarter wavelength matching technique is that this method is used to match real impedances. Most of the time, the impedances on gate and drain sides of a transistor has both nonzero imaginary and real parts so quarter wavelength impedance transformation is not directly applicable to matching network design of a PA.

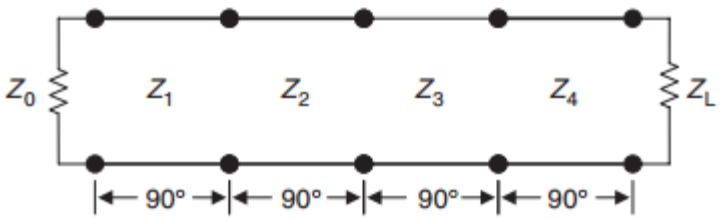


Figure 3.7 A quarter wavelength four section impedance transformer.

Another problem for both of the matching methods explained above is that they assume constant input and output impedances at all frequencies. However, the optimum impedance of a PA slightly changes across the interested frequency band. Therefore, if a wideband matching is required, the designer must monitor the impedance transformation along the matching network for whole frequency band. As a general approach, quarter wavelength transformers and low pass type matching networks are used together to realize the required impedance matching in the interested frequency band.

In addition, when high RF output power is needed, wide gate periphery devices are chosen. As a result, source and load impedances of the transistors become extremely low. For instance, as will be shown in Chapter 4, the transistor, that will be used as the active device of this thesis work, has an optimum load impedance whose real part is 2 ohms. To match 2 ohms to 50 ohms, the output matching network will have an impedance transformation ratio 1:25 which is a significantly challenging to match over a wide bandwidth.

3.3.3 BIAS NETWORK

If bias network elements are not used as matching elements then input impedance of the bias network must be very high, ideally open circuit, compared to 50 ohms to isolate the bias network from matching circuits at high frequencies. For low frequency amplifiers, bias networks can be designed using RF chokes. At microwave frequencies, bias networks are designed using λ/4 transmission lines.

In Figure 3.8, lumped element gate and drain bias networks are presented. Decoupling capacitors provide RF short circuit at gate and drain bias points and RF chokes transformers the RF short circuit to RF open circuit. The electrical length between decoupling capacitor and RF choke must be as short as possible in order not to shift RF short impedance. Therefore, the designer should do the RF bias network design on Smith Chart to observe the location of Z_bias impedance.

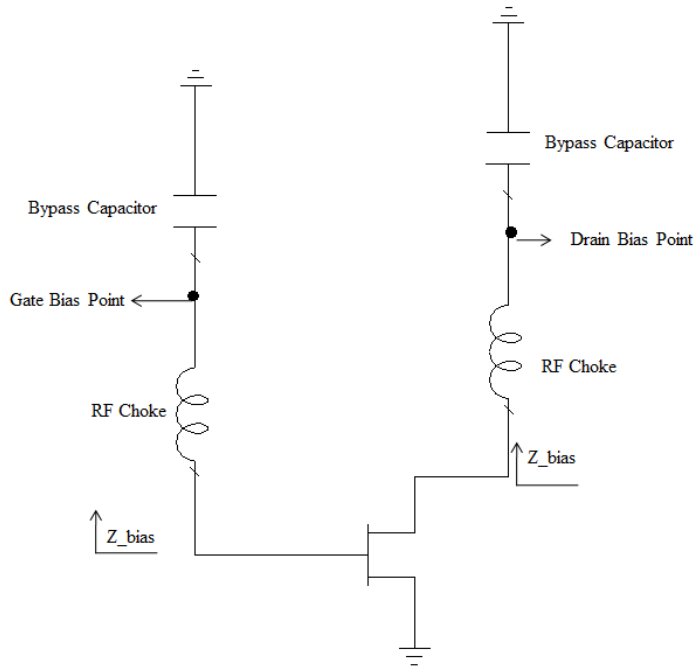


Figure 3.8 A typical lumped element gate and drain bias networks.

In Figure 3.9, a bias network synthesized using λ/4 transmission lines and decoupling capacitors that provides short circuit (very low impedance) at the gate/drain bias point. In theory, due to the decreasing impedance behavior of an ideal capacitor with increasing frequency, it is expected that the capacitor provides very low impedance values - close to short circuit region of the Smith Chart- at the bias points. However, since capacitors are not ideal and they always have complex electrical model including inductors and resistors, they have some resonance frequencies decreasing usable range of frequency spectrum.

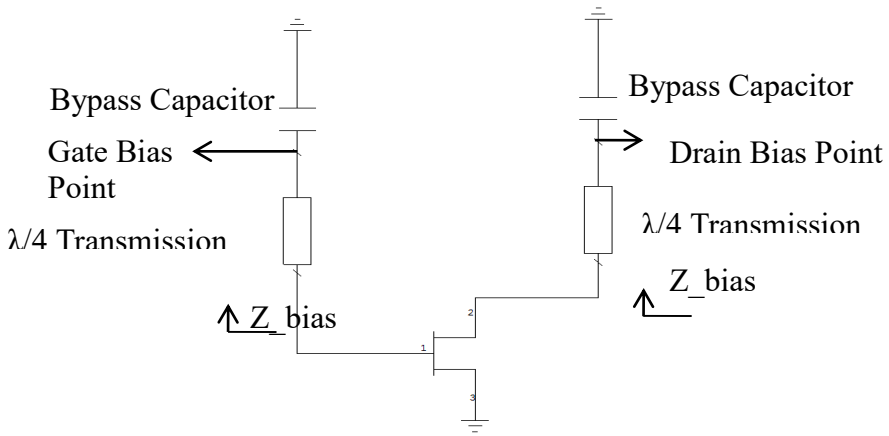


Figure 3.9 A typical distributed bias network with short circuit capacitor.

In Figure 3.10, a wideband distributed element bias network is shown. As it is seen, λ/4 radial stub provides a wideband short circuit at the biasing point and λ/4 transmission line transforms the short circuit to open circuit of Smith Chart. Since radial stub provides the short circuit, a close bypass capacitor is not needed anymore. However, to decouple the circuit from the supply, a decoupling capacitor will provide a better supply performance if sudden current change occurs. Typical input impedance of a distributed element bias network simulated in a CAD tool is presented in Figure 3.11. As it is seen, the bias network provides high input impedance between 8-12 GHz frequency band.

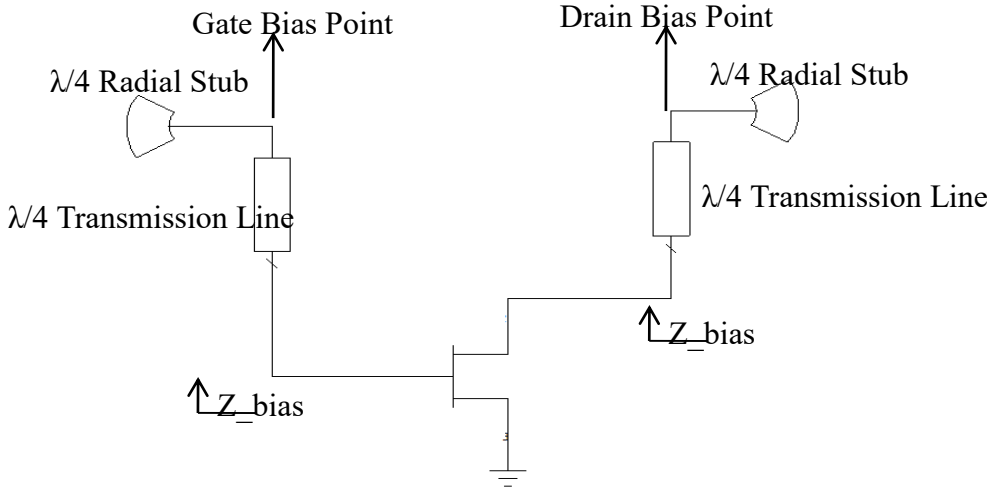


Figure 3.10 A typical distributed bias network with radial stub.

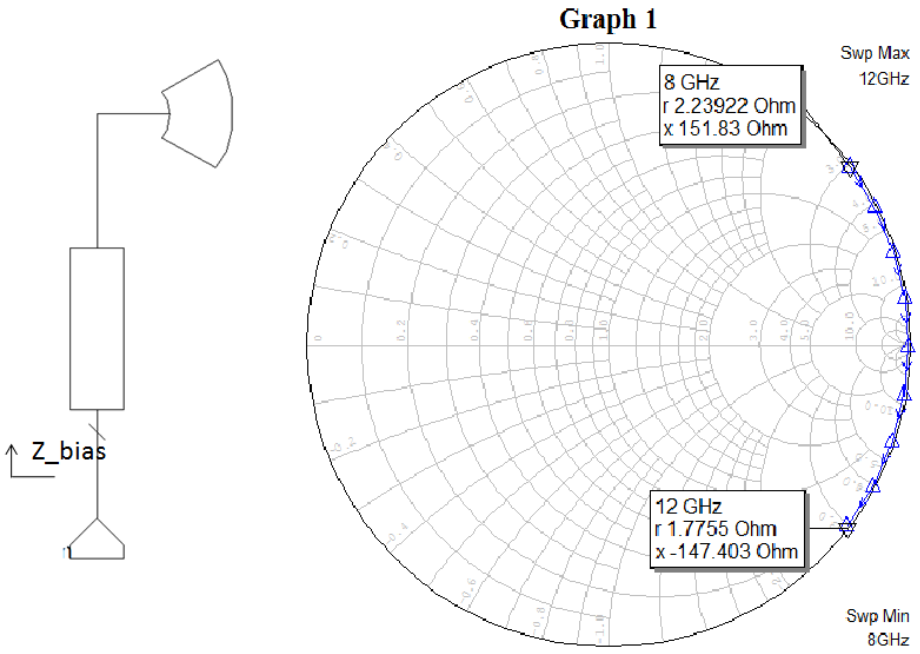


Figure 3.11 Input impedance of a distributed biasing network.

3.4 FABRICATION CONSIDERATIONS

In addition to electrical design of a PA, prototyping must also be considered during the design to obtain a reliable operation. There are several issues such as metal housing, thermal precautions, attachment of active device and PCBs to housing and RF connectors to be used.

Design of metal housing is important since it electrically isolates the PA from other interference signals, transfers the heat generated by PA and provides an infrastructure to mount the PA, supply circuits, RF connectors to build a complete PA module. Most commonly used housing material is aluminum since it is cheap, easy to process mechanically and light weight. In addition, it has both relatively good electrical and thermal conductivity. Most of the time, aluminum is plated through a gold layer or a silver layer but there is also a nickel seed layer in between [21]. In Figure 3.12, a typical thermal stack-up is presented. Metal housing transfers the heat to cold plate through surface touch and screws. As thermal conductivity of metal housing material

increases meaning lower thermal resistance, the heat is transferred faster so equilibrium temperature of transistor junction becomes lower. In addition to thermal conductivity (thermal resistance), density of the housing material is also important since higher density materials provide larger thermal capacitance so that heat transfer becomes faster. However, weight of the total module will increase if a higher density housing material is chosen. For instance, copper has higher thermal conductivity and higher density then aluminum but it is more expensive and results in heavier PA module. Therefore, the choice of metal housing material is application dependent.

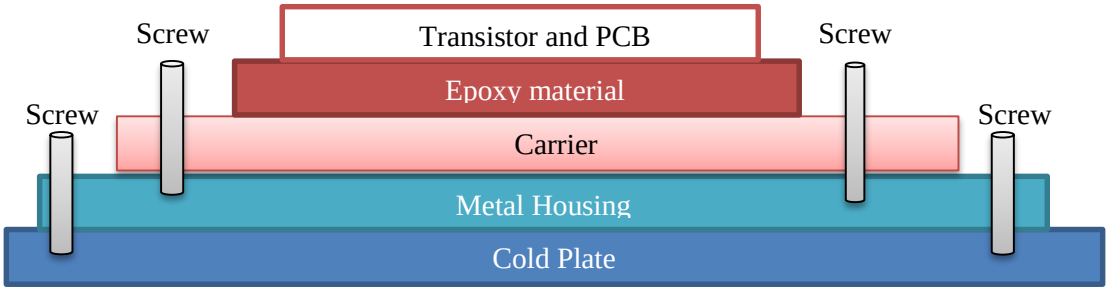


Figure 3.12 Typical thermal stack-up.

Active devices and PCBs must be mounted to metal housing using epoxy materials and metal carries. Metal carriers are optional parts since transistors and PCBs can be directly attached to metal using thermal and conductive epoxy materials. However, metal carriers provide production and maintenance flexibility since they form a separate part of a PA module together with transistors and PCBs. For instance, when an active device is burnt out on a metal carrier, that metal carrier can be mounted off, active device is replaced or a new metal carrier can be mounted on to housing.

Epoxy materials as chemical adhesives that provide both electrical and thermal conductivity. Transistors in die form and metal backed PCBs are epoxied directly onto metal housing or metal carriers. Electrical conductivity provides grounding to active devices whereas thermal conductivity provides low thermal resistance between semiconductor and back side metal. In addition to electrical and thermal conductivity, epoxy materials should provide some degree of flexibility since thermal expansion coefficients of semiconductor materials and metals usually do not match with each other. Therefore, as power dissipation increases, the generated heat will increase as in

the case of a PA and thermal expansion will occur in both metal and semiconductor material. When thermal expansion is significantly different, due to the mechanical stress, mechanical breaks will occur on semiconductor material. Flexible epoxy material will form an interface between semiconductor and metal to decrease the level of mechanical stress.

Cold plate must also be cooled using an active cooling method such as air or fluid flow. Since cold plates also have finite thermal capacitance, their ability to *stay cold* is restricted to a finite time. If they are not cooled, the temperature of cold plate and junction of semiconductor will have same temperature or even cold plate high temperature so that heat flow will not occur between transistor junction and cold plate and transistor will be burnt out in a very short time.

CHAPTER 4

X BAND GaN HYBRID MIC POWER AMPLIFIER DESIGN

In Chapter 2 and Chapter 3, fundamental parameters and concepts defined for a PA, typical design process of a PA, various circuit blocks and fabrication concerns are discussed.

In this chapter, using the basis constituted in previous chapters, an X-band GaN PA will be designed step by step. Starting with the definition of requirements, a complete PA will be constructed using both small-signal and large-signal simulations as a demonstration to previous chapters.

In addition to high frequency circuits, a drain voltage pulsing method and a circuit topology will also be discussed.

4.1 DEFINITION OF REQUIREMENTS

The following requirements are expected to be satisfied by the PA. These requirements will be the basis for each design decision in the other PA design steps.

Table 4.1 PA Requirements

Parameter	**Requirement**
Frequency Band	9-11 GHz
Output Power	20 W
PAE	30%
Small Signal Gain	10 dB

4.2 DEVICE AND MATERIAL SELECTION

In accordance with the requirements defined above, Cree's CGHV1J025D GaN discrete transistor die is chosen as the active device. The manufacturer also provides a nonlinear model for the device so load-pull simulations can be done using one of commercially available electromagnetic simulation tool.

Total gate length of the CGHV1J025D is 5 mm and specified power density of the device is around 5 W/ mm. Therefore, it can provide approximately 25 W output power with 10 dB power gain in 9-11 GHz frequency band. However, these values are measured using on-wafer measurements so they do not include any circuit loss. A photo of the transistor is shown in Figure 4.1.

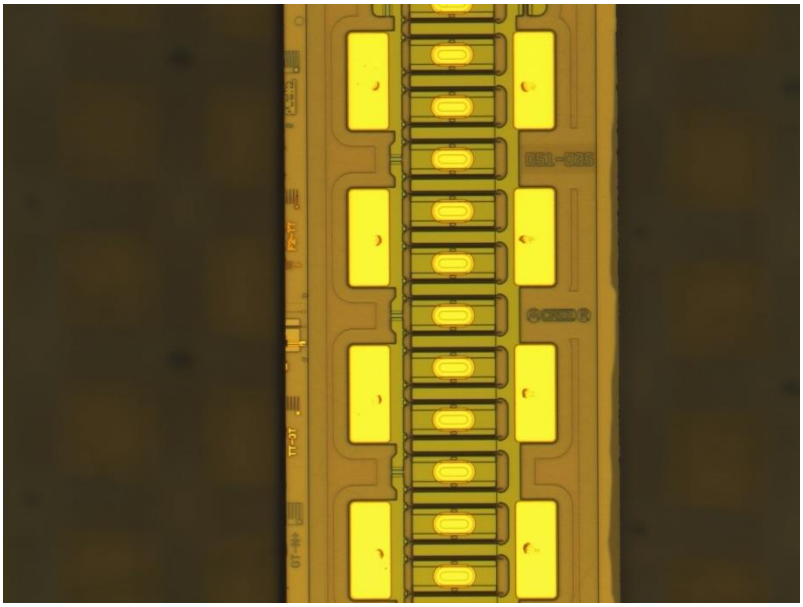


Figure 4.1 Photo of the CGHV1J025D GaN Transistor Die.

In addition to the active device, a substrate material to build the matching circuits must be chosen. In order not to lose available gain and available power that the active device can provide, a substrate material with low loss tangent should be used. Moreover, thermal conductivity is another important parameter since high temperatures might occur on substrate materials due to the high RF power levels and circuit losses.

High dielectric constant materials give the opportunity to design smaller size circuits which result in smaller final PA size. Therefore, a relatively large dielectric constant material with low loss tangent and high thermal conductivity would be a good choice. As a result, alumina is chosen to be the substrate material that has the properties shown in Table 4.2.

Table 4.2 Alumina Material Properties

Parameter	Value
Dielectric Constant	9.7
Loss Tangent	0.0002
Thermal Conductivity(Watts/m°K)	26.9
Thickness	5 mil

4.3 TRANSISTOR ANALYSIS USING NONLINEAR MODEL

Availability of the nonlinear model of the transistor greatly simplifies the design procedure since DC analysis, stability analysis and load pull simulations can be done directly on a commercially available CAD tool.

4.3.1 DC ANALYSIS

DC simulation result in the form of transistor drain IV curves is presented in Figure 4.2. As it is seen on the Figure, knee voltage of the transistor is around 8 V and breakdown voltage of the transistor is approximately 125 V. Although, to have a voltage swing between 8 V and 125 V, the designer must choose the drain voltage quiescent point in the middle of those voltages but due to the thermal reasons and to stay away from the breakdown region, 40 V is chosen to be drain quiescent point. As indicated in Chapter 1, Class AB operation is a good compromise between output power, efficiency and linearity so 40 V drain voltage and 240 mA drain current are chosen bias parameters which are also suggested in the datasheet of the transistor.

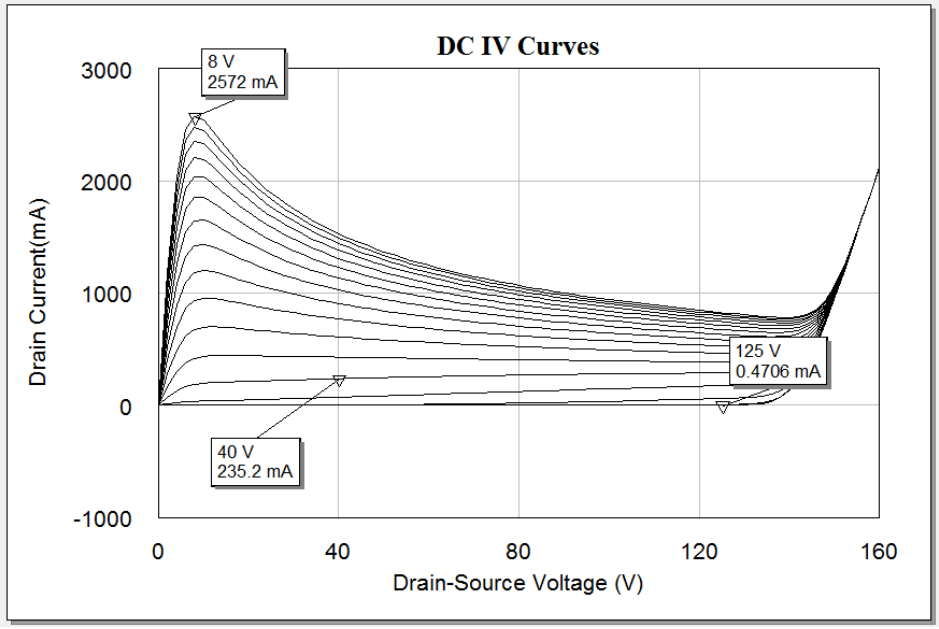


Figure 4.2 IV Curves of the transistor.

4.3.2 STABILITY ANALYSIS

Stability is one of the first issues to analyze at the beginning of PA design. Since, S-parameter response of the device is function of the bias points, stability factors must be simulated at the operating bias conditions.

In Figure 4.3, μ-factor and MAG are drawn as a function of frequency. Stability analysis must be done from very low frequencies to very high frequencies to observe potentially unstable regions. Since μ-factor is a geometrical stability criterion, as it becomes larger circuit becomes more stable. However, there is an inverse proportionality between μ-factor and MAG so that μ-factor must be close to 1 in the frequency band of interest but as large as possible out of band to have high gain and to prevent out of band oscillations. As it is seen on Figure 4.3, the active device is stable above 11.7 GHz and unstable otherwise. Therefore, a stability circuit must be designed to have unconditional stability at all frequencies.

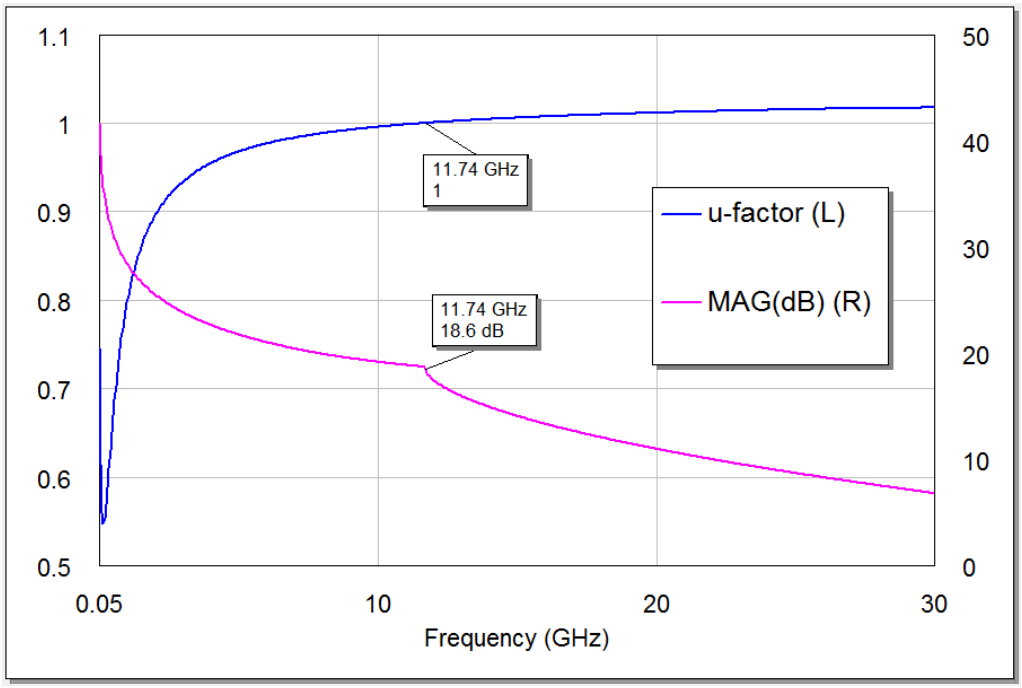


Figure 4.3 μ-factor and maximum available gain.

Stability networks provide unconditional stability at all frequencies by introducing resistance to matching network. The value of the resistance needed by the active device to have unconditional stability can be found using the stability circles. In Figure 4.4, input stability circles of the active device are presented. In this case, the stability circles imply that the device is unstable inside the stability circles and stable at the other parts of the Smith Chart. To have stability at all frequencies, stability circles must be pushed out of the Smith Chart. The real parts of the values shown by markers located on the Figure show the required resistance value to have unconditional stability at the frequency that marker shows. As it is seen, the device needs more resistance at lower frequencies and low resistance at higher frequencies. From another perspective, it can be said that by adding the required series resistances, the impedance values that the active device can see at its input side will be restricted to the safe regions of the Smith Chart.

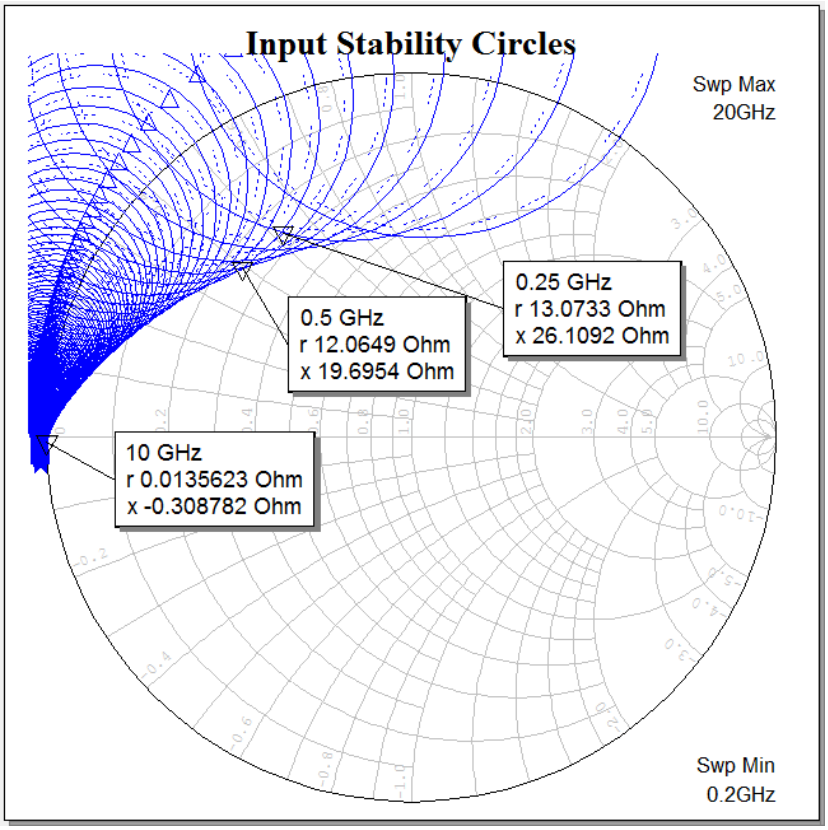


Figure 4.4 Input stability circles.

4.3.3 LOAD PULL AND SOURCE PULL SIMULATIONS

Load pull and source pull simulations are essential design steps in PA design procedure since they construct a basis for the design of matching networks. Generally, at the load side of a PA, load pull simulations are done to find optimum impedances for the highest possible output power whereas at the source side of a PA, source pull simulations are done to find the optimum impedances for the highest possible gain.

In Figure 4.5, results of load pull simulations at 10 GHz are shown as load pull curves for the maximum output power. As it is seen, the active device can provide approximately 44.2 dBm output power when it sees 2.5+7.2*i ohm load impedance. However, this impedance level is only valid for 10 GHz meaning that at the other frequency points it will slightly change.

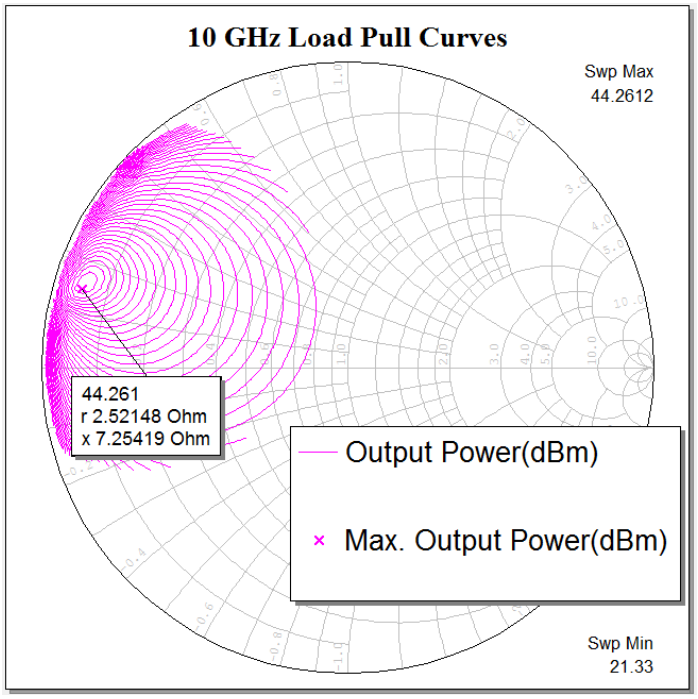


Figure 4.5 Load pull contours at 10 GHz.

In Figure 4.6, results of source pull simulations at 10 GHz are shown as load pull curves to maximize the small signal gain of the amplifier. As it is seen, the active device can provide approximately 18 dB small signal gain when it sees 0.3-ohm source impedance which is very close to short circuit point of the Smith Chart. However, this impedance level is only valid for 10 GHz meaning that at the other frequency points it will slightly change.

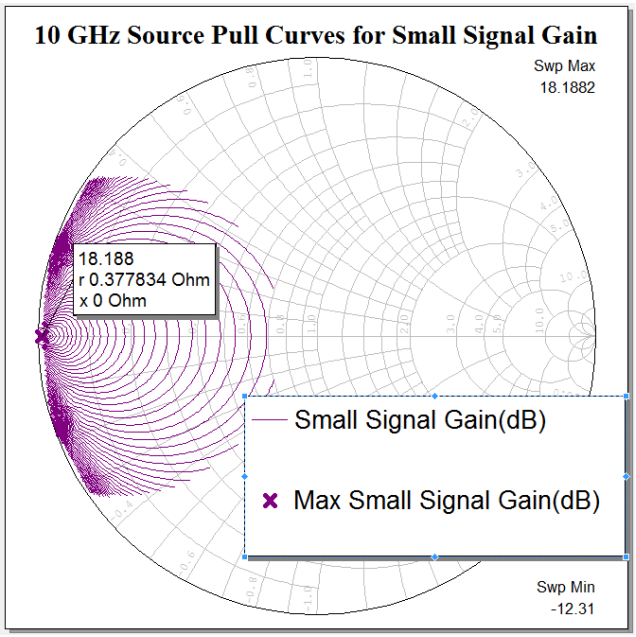


Figure 4.6 Source pull contours at 10 GHz.

In Figure 4.7, optimum impedances at the input and output of the active device are shown on the Smith Chart. Although, optimum source impedances do not change, optimum load impedances differ from each other at each frequency point.

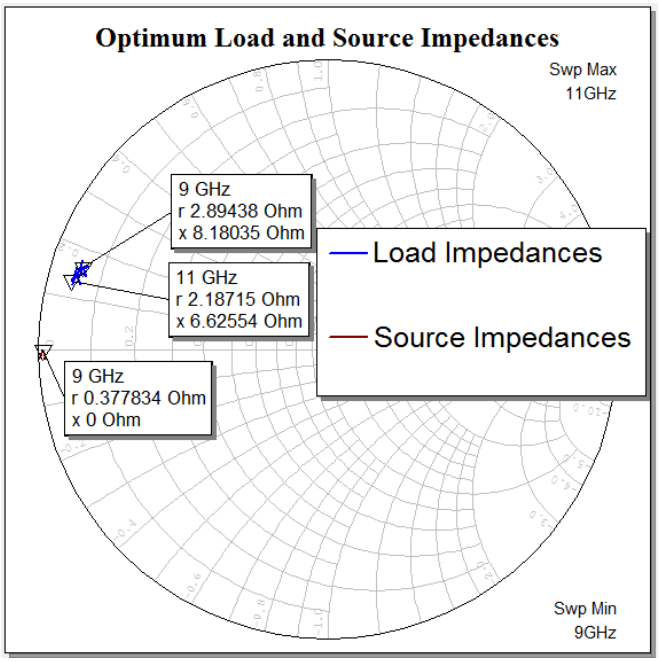


Figure 4.7 Optimum load and source impedances in 9-11 GHz frequency band.

In simulation environment, using a lossless multi-frequency impedance tuner, optimum load and source impedances at each frequency point is shown to the active device. The resulting output power and small signal gain obtained from the transistor is shown in Figure 4.8. As it is seen, the output power is around 44 dBm and small signal gain is between 18 dB and 16.5 dB. However, these results do not include any mismatch or any propagation loss which will be introduced by matching networks. Stability network will also introduce an additional loss to have unconditional stability so small signal gain will be significantly lower than source pull results.

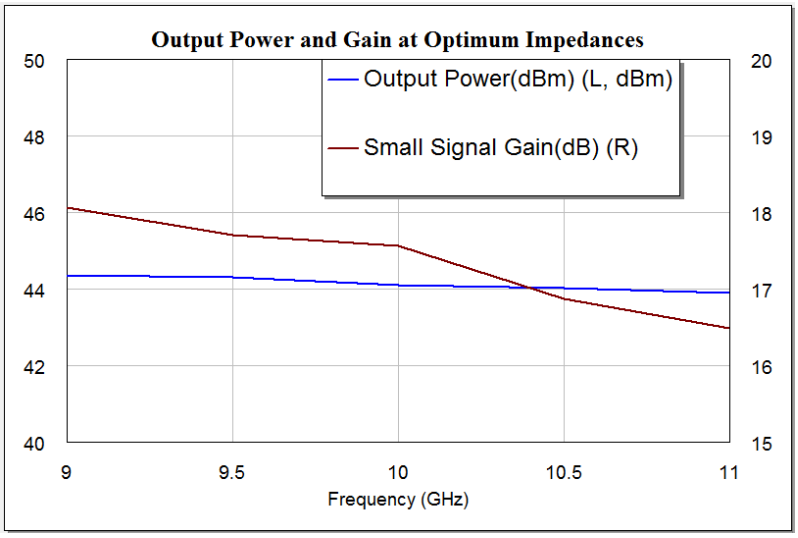


Figure 4.8 Output power and small signal gain obtained as a result of load/source pull simulations.

4.4 BOND WIRES

In hybrid microwave circuits, bond wires are used to carry electromagnetic waves between different substrates. In hybrid power amplifier circuits, bond wires are used between transistor die and matching network substrates to provide connection. In Figure 4.9, a 3-dimensional bond wire model for the connection of matching network and drain pads of the active device is presented.

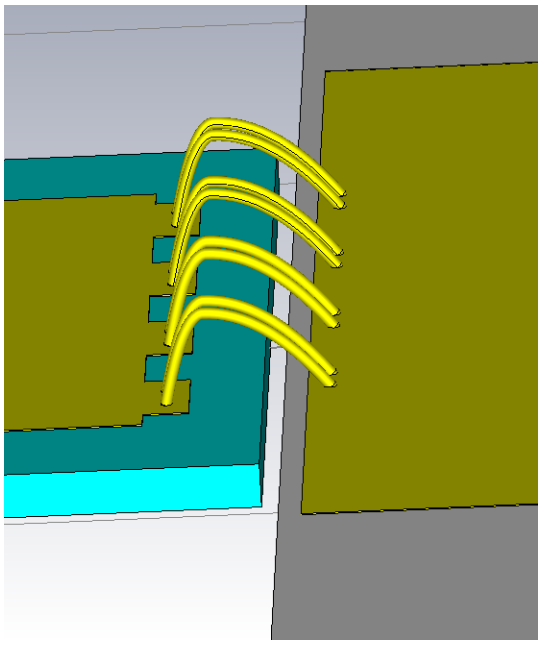


Figure 4.9 3D Bond wire model.

Bond wires behave as very narrow microstrip lines whose substrate material is mostly vacuum so that they are microstrip lines that have very high characteristic impedances. As shown in Figure 4.7, optimum load and source impedances are very close to short circuit region of the Smith Chart so that bond wires- high characteristic impedance lines- transforms those optimum impedances significantly on the Smith Chart. As a result of this transformation, not only impedance points changes but also the designer loses some of the available bandwidth since optimum impedance points spread out.
On Figure 4.10, optimum load impedances looking into the matching network and shifted optimum load impedances due to bond wires are shown together. As it is seen, even small length of bond wires greatly impacts the location of optimum impedances. Therefore, bond wires must be thought as matching network elements being a part of the impedance matching networks since their use is unavoidable in hybrid microwave circuits. The markers in the Figure 4.9 placed on both curves show that the bond wires shifted the impedance values by 13° in terms of their phase.

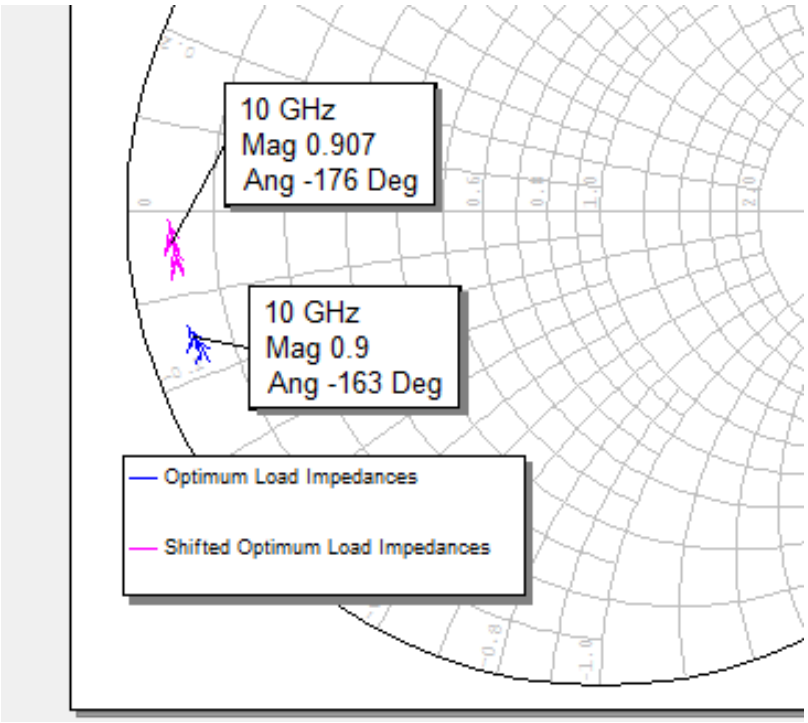


Figure 4.10 Optimum load impedances and shifted optimum load impedances by bond wires.

4.5 STABILITY NETWORK DESIGN

As it is shown in section 4.3.2 the transistor is potentially unstable for the frequencies below 11.7 GHz so it is needed to add a stability network providing unconditional stability for all frequencies. It is important to be conscious of the fact that since an intentional loss is introduced to the PA to stabilize, the stability network should provide highest gain together with unconditional stability. Therefore, it is necessary to monitor the maximum available gain with a stability factor not to lose to control the introduced loss level at the frequency band of interest. The proposed ideal circuit for unconditional stability, which is a simple, parallel connected RC circuit, is shown in Figure 4.11.

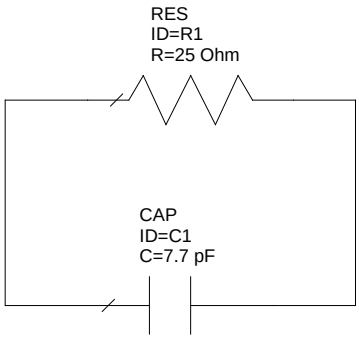


Figure 4.11 Proposed ideal stability network.

The stability factor and maximum available gain is also shown in Figure 4.12. However, the circuit elements used in the proposed network are ideal and the network does not contain any parasitic elements. The actual model of the network includes parasitic inductances, parasitic capacitances and resistances for each element and between elements and ground layer. The inductors and capacitors generate resonant frequencies that may cause high loss. Therefore, actual 3D model is needed to construct and the circuit must be simulated to include all parasitic effects and to see actual circuit response.

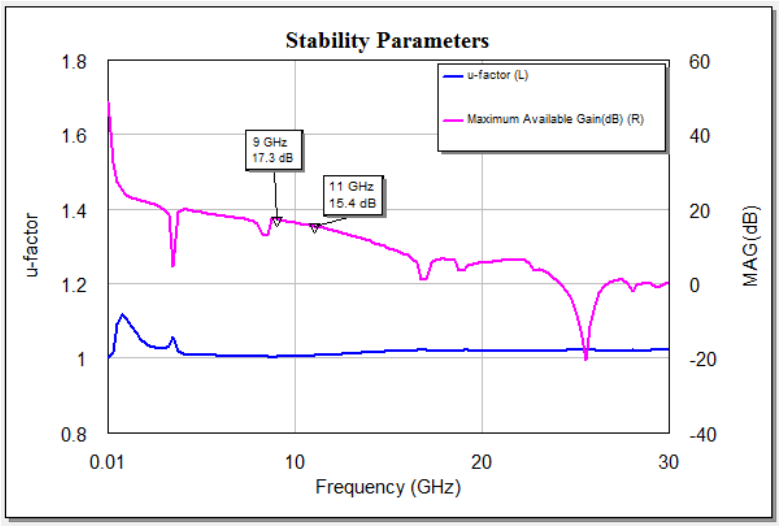


Figure 4.12 u-factor and maximum available gain with ideal network.

The constructed 3D model of the proposed ideal network is shown in Figure 4.13. Instead of ideal capacitor and resistor, thin film capacitors and resistor used. The

bottom sides of the capacitors are attached to the microstrip line using conductive epoxy material and connected the upper sides are connected to circuit using bond wires. The resistor is modeled as a thin film resistor with 50 ohm/square sheet resistance value. Gate bond wires between stability network and transistor die is also included in the stability network model to have a better accuracy.

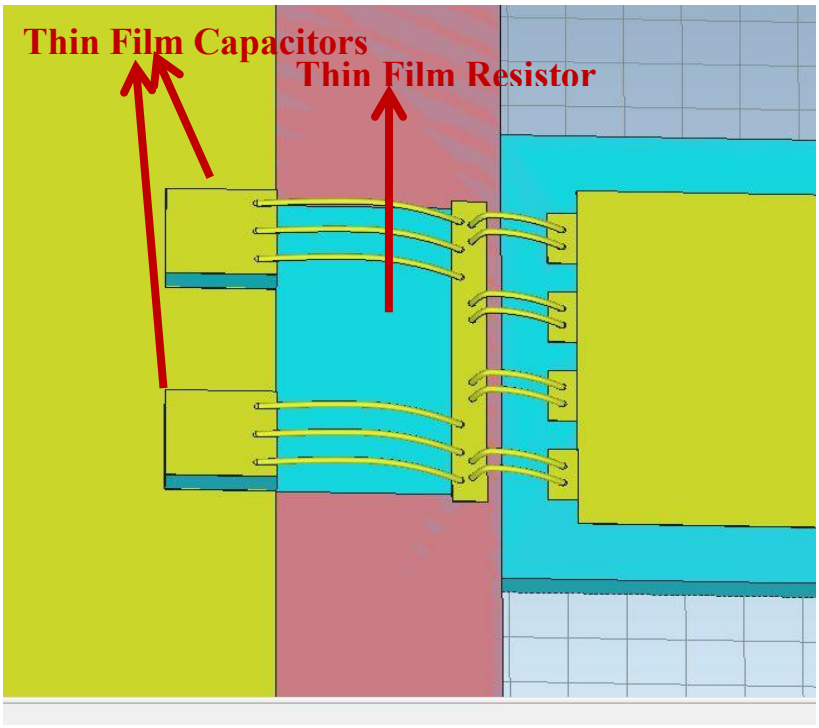


Figure 4.13 3D model of stability network.

The u-factor and maximum available gain with the 3D electromagnetic simulation result is shown in Figure 4.14. It should be noted that the model shown in Figure 4.13 is an optimized model for to have a u-factor greater than 1 for all frequencies and relatively higher gain values. It is seen that maximum available gain is higher than 14 dB in 9-11 GHz band u-factor is greater than 1 everywhere. The optimization is done by changing capacitor values and tuning the number and length of bond wires than connect the upper side of the capacitors. It is also observed that the maximum available gain value is lower out of the band which is the result of optimization work. After the optimization, the total capacitance value becomes 1.6 pF and resistance value becomes 25 Ohm.

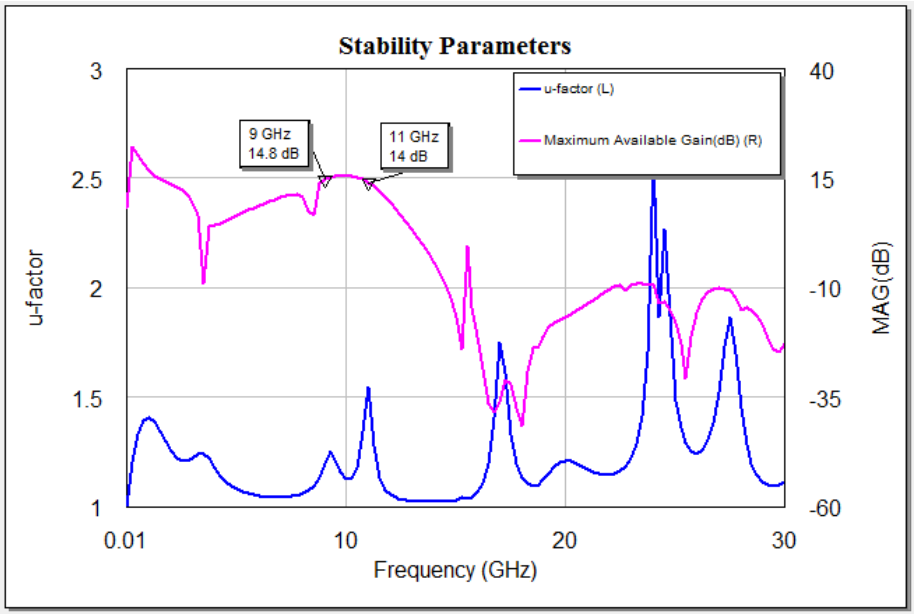


Figure 4.14 Stability network result with 1.6 pF capacitance value.

Figure 4.15 shows the result of another simulation using total capacitance of 9.1 pF. It is seen that although the transistor is unconditionally stable, maximum available gain drops down to 7 dB level due to the shift of a resonance frequency occurring in circuit response. Figure 4.15 also points out the importance of the careful stability network design not to introduce higher loss than needed in the circuit.

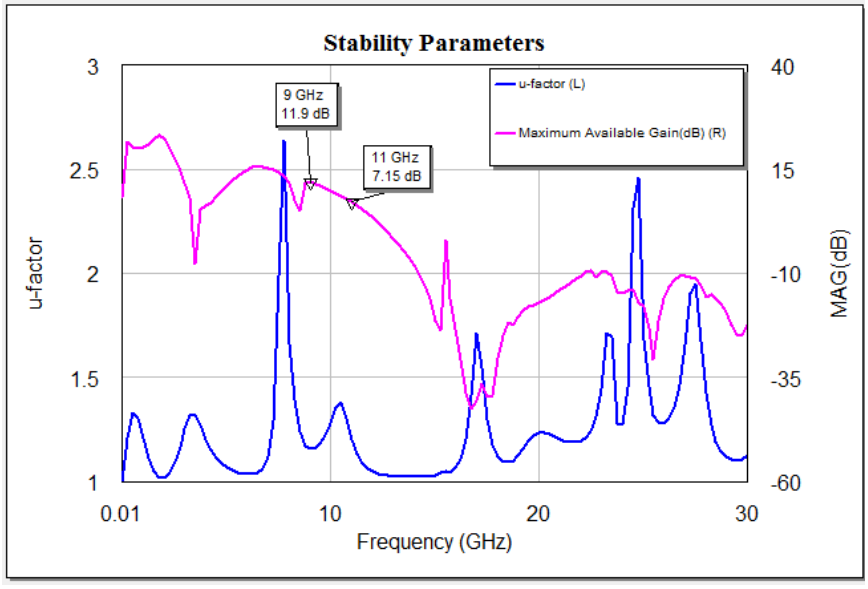


Figure 4.15 Stability network result with 9.1 pF capacitance value.

4.6 INPUT MATCHING NETWORK DESIGN

Based on the source pull simulations done in previous sections, an input matching network is designed using microstrip circuits. The schematic view of the input matching network is shown in Figure 4.16. It is seen that the stability network designed in previous section is also included in the input matching network since it transforms the impedance in addition to its stabilization duty. Therefore, the stability network must be thought as a part of the input matching circuit.

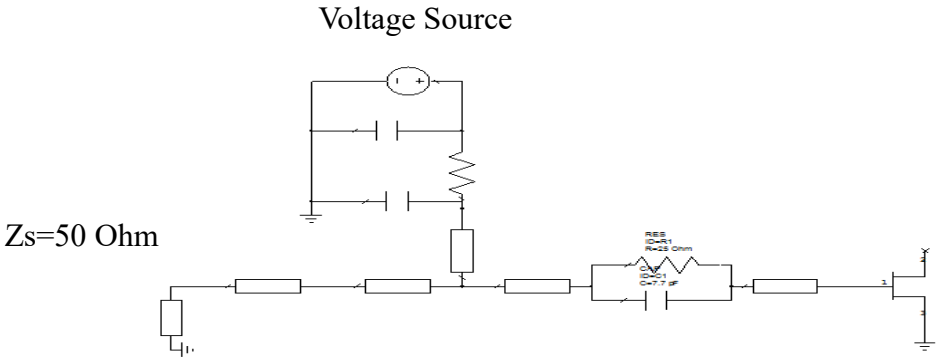


Figure 4.16 Schematic view of input matching network.

The 3D electromagnetic model of the input matching network including bond wires, stability network and gate bias circuit is shown in Figure 4.17. It should be noted that gate bond wires are also assumed to be a part of the input matching network.

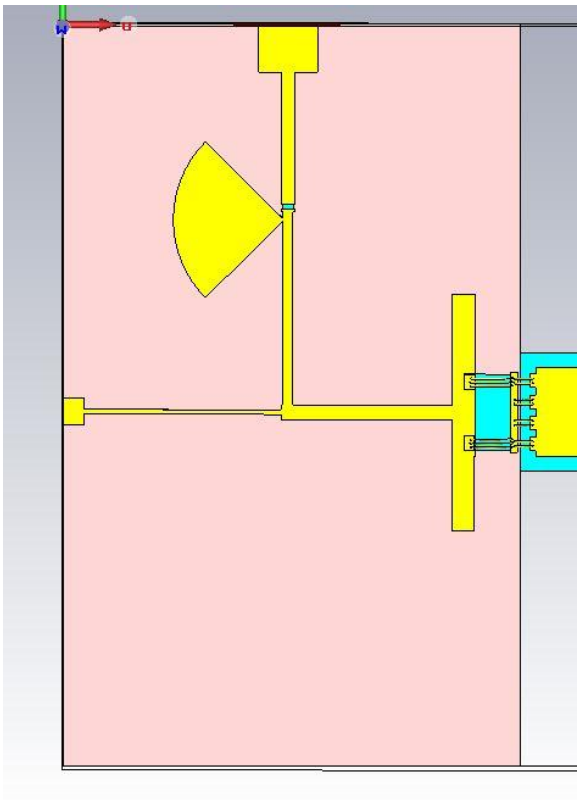


Figure 4.17 3D electromagnetic model of the input matching network.

Using the constructed 3D electromagnetic model, the input matching circuit is simulated and tuned to compensate the differences between electromagnetic simulations and ideal circuit simulations. The impedances that is shown to the gate pads of the transistor is shown in Figure 4.18 together with optimum source impedances found by source-pull simulations. As it is seen there is a remarkable difference between locations of two impedance sets. However, the optimum impedances are so close to short point of the Smith Chart that they cannot be obtained for a relatively large bandwidth of 9-11 GHz. As a result of this difference, the small signal gain and input return loss of the PA will be worse than expected as will be shown in Section 4.8.

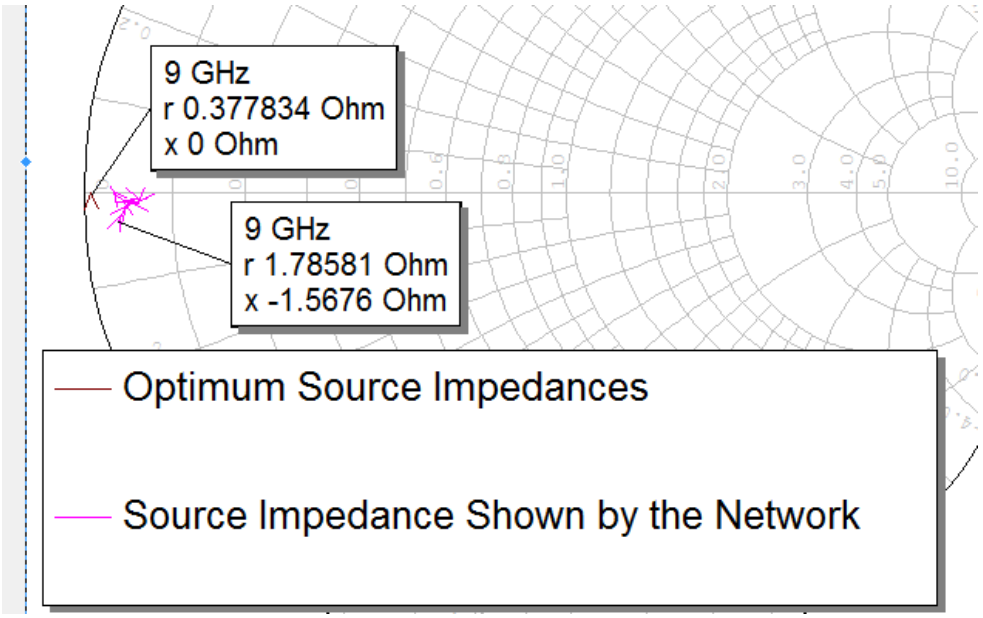


Figure 4.18 Response of simulated and tuned input matching network.

4.7 OUTPUT MATCHING NETWORK DESIGN

The proposed schematic structure for the output matching network is shown in Figure 4.19. Drain bias network is also included in the output matching network since it will be a significant part of the layout of the network.

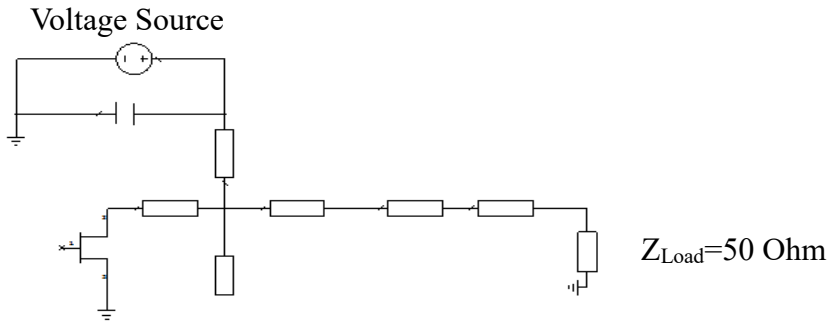


Figure 4.19 Schematic view of output matching network.

3D electromagnetic model that belongs to schematic shown above is given in Figure 4.20. It should be noted that drain bond wires connecting alumina substrate and the transistor is also included to the model.

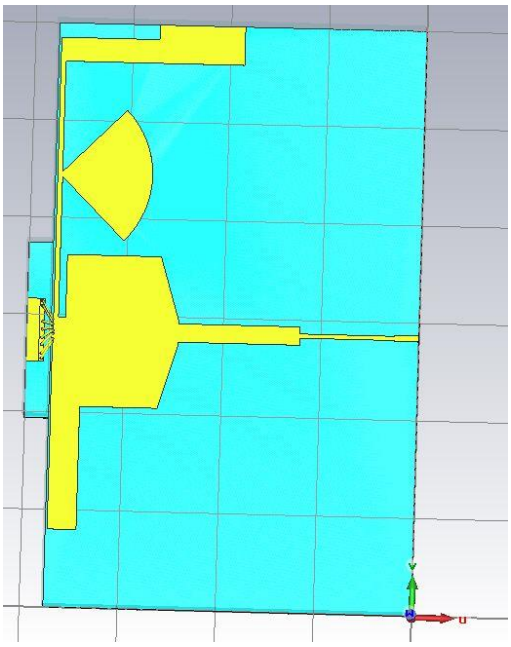


Figure 4.20 3D electromagnetic model of the output matching network.

The impedances shown to the drain of the transistor and obtained from both load simulations and simulations of electromagnetic model are shown together in Figure 4.21. It is seen that ideal impedances and impedances coming from electromagnetic simulations are almost identical to each other so the it is can be said that electromagnetic model of the output matching network provides power matching at the drain of the transistor.

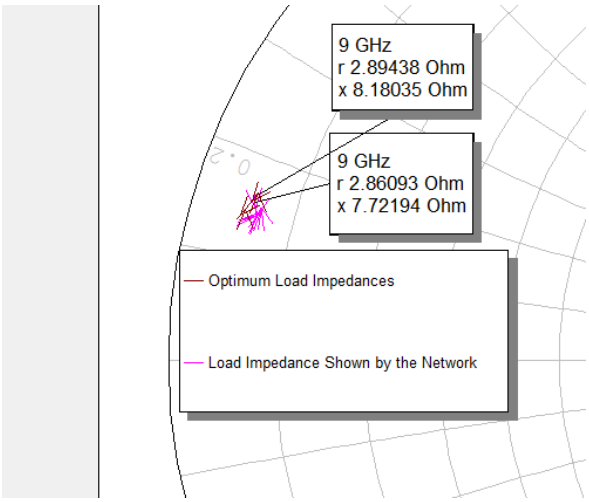


Figure 4.21 Response of simulated and tuned output matching network.

4.8 SIMULATOIN RESULTS

When the design process of the matching networks, stability and bias networks are finished, the circuit blocks are connected to each other to simulate the complete PA. The nonlinear model of the transistor provides the capability of realizing nonlinear simulations such as output power, harmonic distortion, AM/AM and AM/PM.

Small signal simulation results of the PA are given in Figure 4.22 showing that gain of the amplifier is above 11.9 dB at the frequency band of interest. Moreover, output return loss value of the PA is better than -10 dB and input return loss is varying between -5 dB and -10 dB. As shown in Figure 4.18, input matching network cannot provide the required matching at the gate side of the transistor so the input return loss simulation is relatively poor.

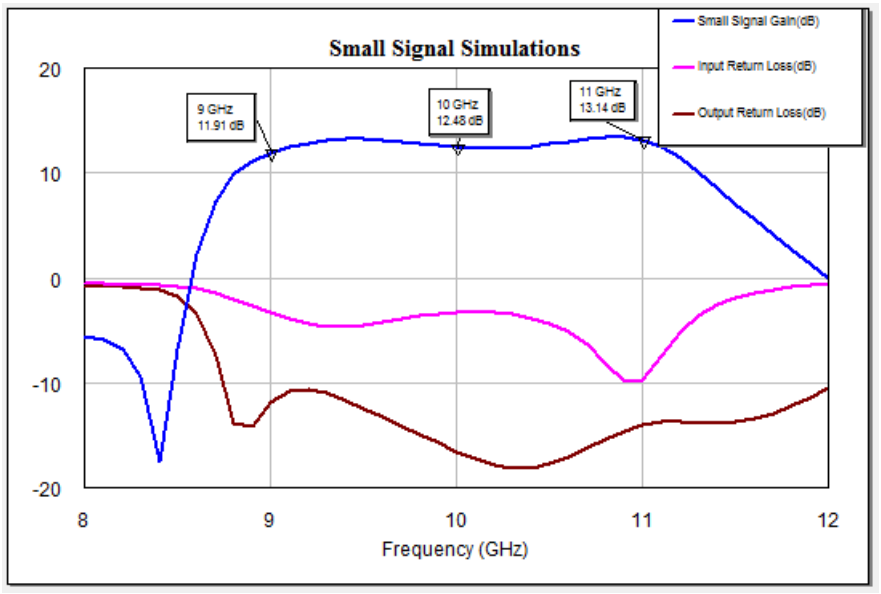


Figure 4.22 Simulated small signal parameters.

Figure 4.23 represents output power, PAE (%) and power gain measurements together. It is seen that output power is better than 43 dBm (20 W), PAE is better than 33% and power gain is better than 6 dB between 9 GHz and 11 GHz. During those measurements, input power is kept constant at 37 dBm for all frequencies. When power gain and small signal gain is compared using Figure 4.21 and Figure 4.22, the PA is saturated more than 6 dB.

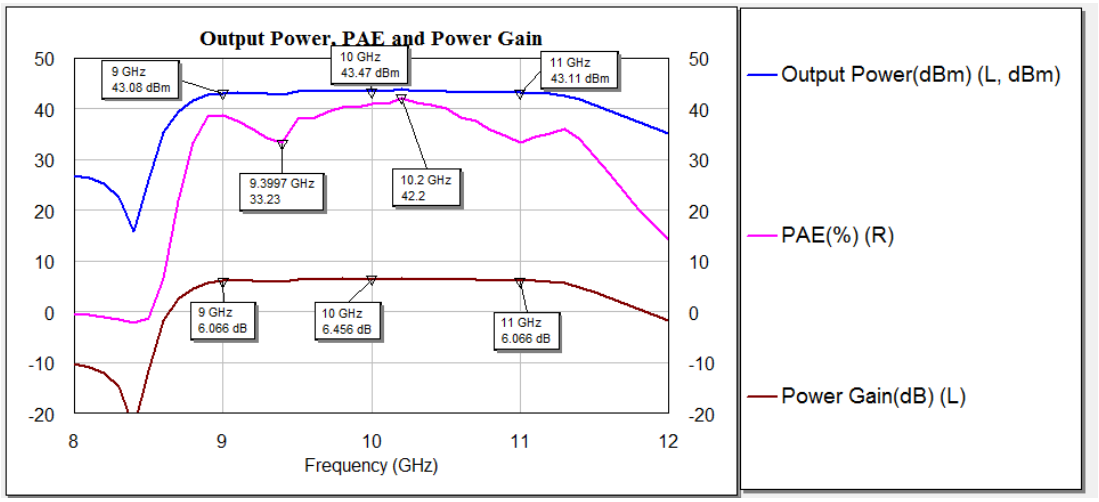


Figure 4.23 Simulated output power, PAE (%) and power gain at 37 dBm input power.

The simulation results to extract the other nonlinearity parameters AM/AM and AM/PM characteristics are shown in Figure 4.24. The 6 dB saturation level observed in previous graphs can also be observed in Figure 4.24. Moreover, the AM/AM curve of the PA has a negative slope for all input power levels. The reason for this behavior is explained by the material characteristics of the GaN. When AM/PM behavior is examined, it is seen that 7° variation in simulations is observed between linear and nonlinear regions.

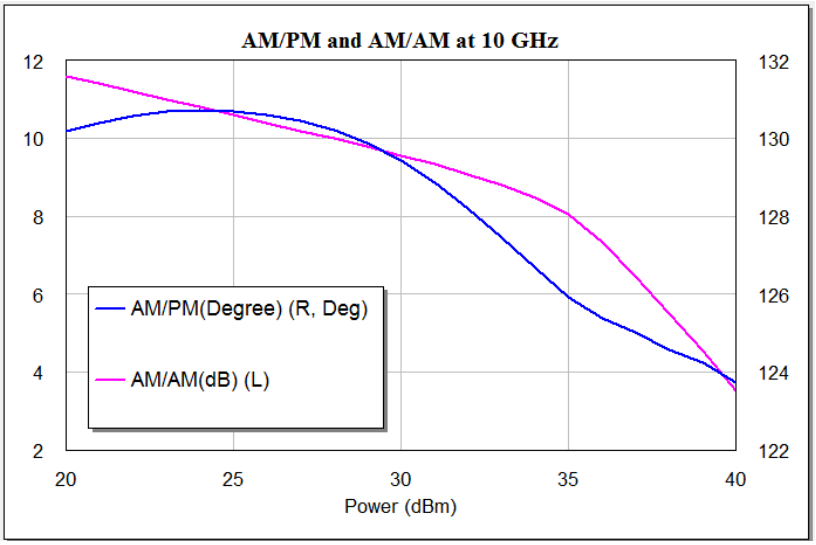


Figure 4.24 Simulated AM/AM and AM/PM curves of the PA at 10 GHz.

Harmonic distortion is another parameter that gives information about the nonlinearity level of the PA. Generated second harmonic level for the 10 GHz fundamental frequency is shown in Figure 4.25. Using the definition given in equation (2-13) the second harmonic distortion, $HD_{2nd,dB}$, can be calculated as follows:

$$HD_{2nd,dB} = 43.46 - 12.18 = 31{,}28 \text{ dBc}$$

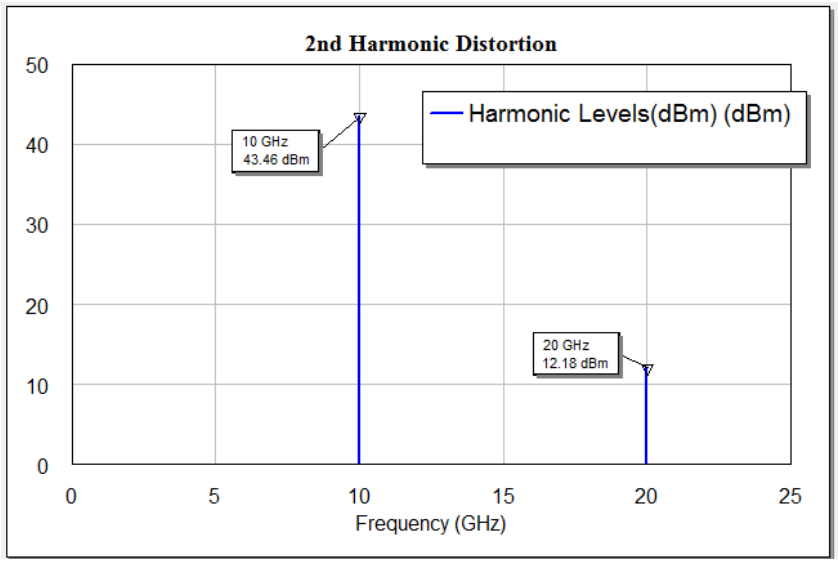


Figure 4.25 Simulated 2nd harmonic distortion.

CHAPTER 5

REALIZATION AND MEASUREMENTS

In Chapter 4, a microwave hybrid PA is designed using a GaN discrete transistor and alumina substrate material by using a nonlinear transistor model which is capable of doing both large signal and small signal measurements.

In this Chapter, the designed PA in Chapter 4 is fabricated and tested to observe the electrical performance parameters of the PA and to compare the simulation and measurement results. Measurement method and measurement setup are described in detail to give a better idea about the PA measurement setups. Measurement results are also discussed in detail to better characterize and understand the behavior of GaN PA.

The PA is measured under both CW and pulsed operating conditions. For each operation mode, PA is biased in Class AB and Class B operating regions to observe the performance change under different DC bias points. Basically, output power, gain and efficiency parameters of the PA are measured for each operation mode and bias point. Moreover, to characterize the nonlinearity of the PA better, AM/AM and AM/PM behaviors are also measured. In addition, output signal spectrum of the PA is also measured to compare spectral properties of different operation modes.

5.1 PROTOTYPING

Designed matching networks are fabricated on alumina substrate using thin film technology. In addition to matching networks, a mechanical housing is also designed

to build the PA. The picture of the fabricated PA is shown in Figure 5.1 and Figure 5.2.

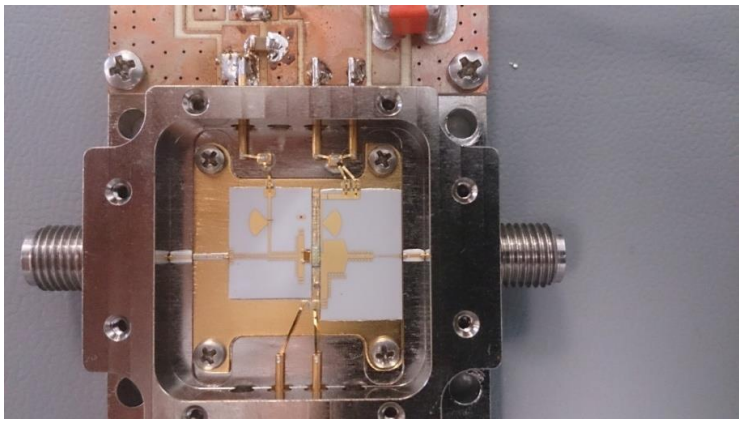


Figure 5.1 Fabricated PA.

The bias circuit which is able to generate pulsed drain voltage is also assembled on to the mechanical housing as seen on Figure 5.2.

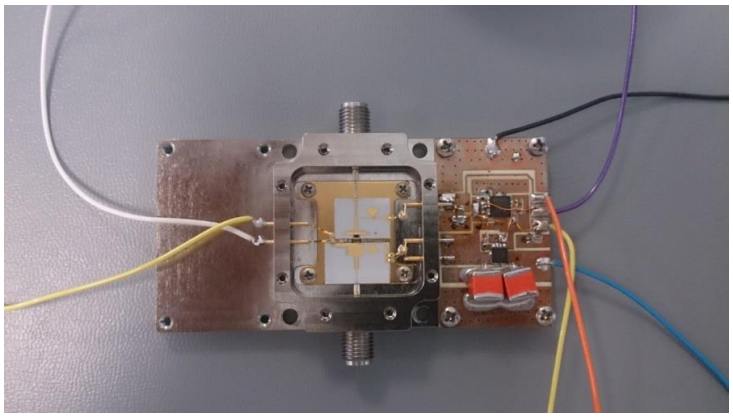


Figure 5.2 Fabricated PA with pulse bias circuit.

As a result of the mechanical structure, a thermal stack-up similar to shown in Figure 3.12 is obtained. A temperature sensor is also placed as close as possible to the transistor die to better monitor the base temperature of the die.

5.2 DESCRIPTION OF MEASUREMENT SETUP

The measurement setup is shown as a block diagram in Figure 5.3. In addition to the PA, a network analyzer (NA) to measure the S-parameters, a driver amplifier to

provide the required input power to the PA and an attenuator to protect the NA from any high power damage are used.

The NA is capable of doing both CW and pulsed mode measurements since it has internal RF pulse sources. Therefore, both CW and pulsed measurements are done using the same measurement setup under both small signal and large signal drive. In this setup, S-parameters can be measured as a function of input power at a predefined frequency between A' and B' planes as shown in Figure 5.1. Since phase and amplitude response of driver amplifier, PA and attenuator block is obtained at each input power level, output power, gain and AM-AM and AM-PM characteristics can be inferred from the results.

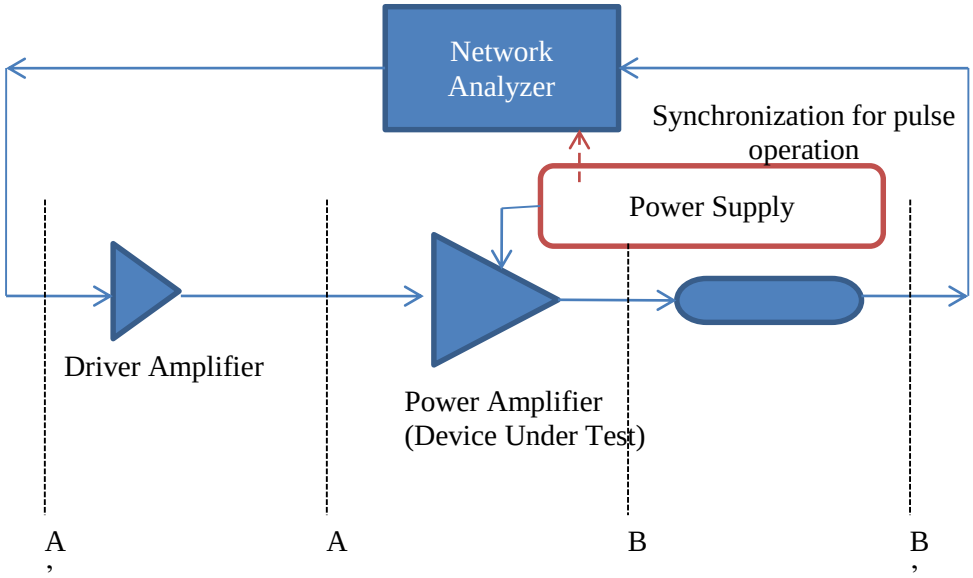


Figure 5.3 The measurement setup of fabricated PA.

However, the results obtained from the test fixture shown in Figure 5.3 include data of driver amplifier, PA and attenuator so by de-embedding the characteristics of driver amplifier and attenuator by using the measurements done by setups shown in Figure 5.4 must be eliminated from the complete block to obtain the characteristics of only PA.

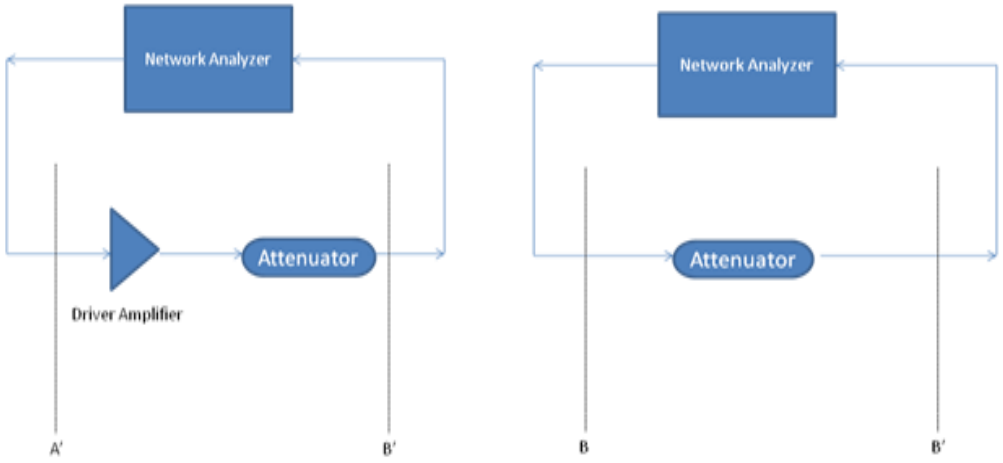


Figure 5.4 The measurement setup of fabricated PA.

Picture of the measurement setup is shown in Figure 5.5. In addition to measurement devices, there are also cooling equipment to prevent the temperature to reach excessive levels for the PA.

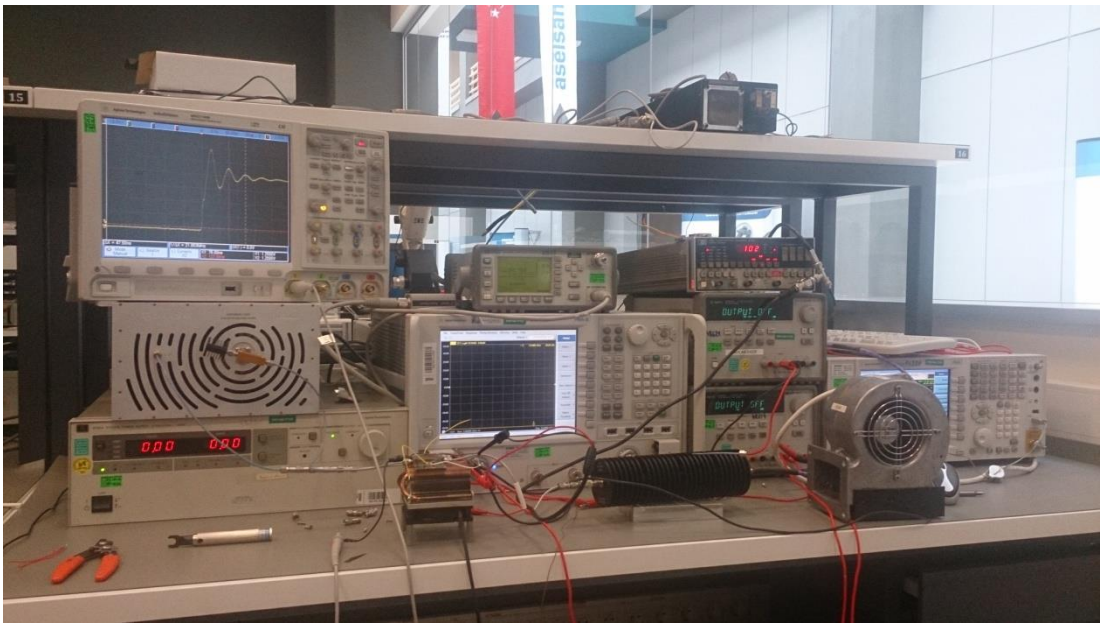


Figure 5.5 The measurement setup of fabricated PA.

5.3 CW FUNDAMENTAL MEASUREMENTS

In CW mode, the drain and gate bias voltages as well as RF input signal are applied continuously to the fabricated PA. During the CW measurements, the PA is biased in Class AB mode whose quiescent drain current is between Class A and Class B modes drain bias currents. Table 5.1 summarizes the bias parameters of Class AB CW mode measurements. As it is seen on the table, the gate bias voltage that generates 240 mA drain current a little differs from the simulation model supplied by the manufacturer. That difference is most probably due to the production tolerances of semiconductor device.

Table 5.1 Class AB Bias Voltage and Current Values

Class AB Bias Conditions		
Gate Voltage(V)	**Drain Voltage(V)**	**Drain Bias Current(mA)**
-2.64	40	240

As a first step, the PA is measured under small signal conditions to validate that whether the PA works as expected and is stable or not. If the PA is not stable then small signal gain might be lower, drain current might have ripples, sudden changes and even the PA could burn out due to the instability. Figure 5.6 represents the small signal measurement result of the PA under CW operation mode. It is observed that the PA does not have any stability problem and works as expected. However, the small signal gain is a little lower than the simulation result. The reason of this performance variation is most probably matching network loss which is not accurately simulated using EM simulators. Moreover, the PA package includes RF connectors, some microstrip lines which also introduce additional loss. This additional loss is measured and included in results but the transitions between matching networks and microstrip lines could cause mismatch loss due to imperfect 50 ohm characteristics.

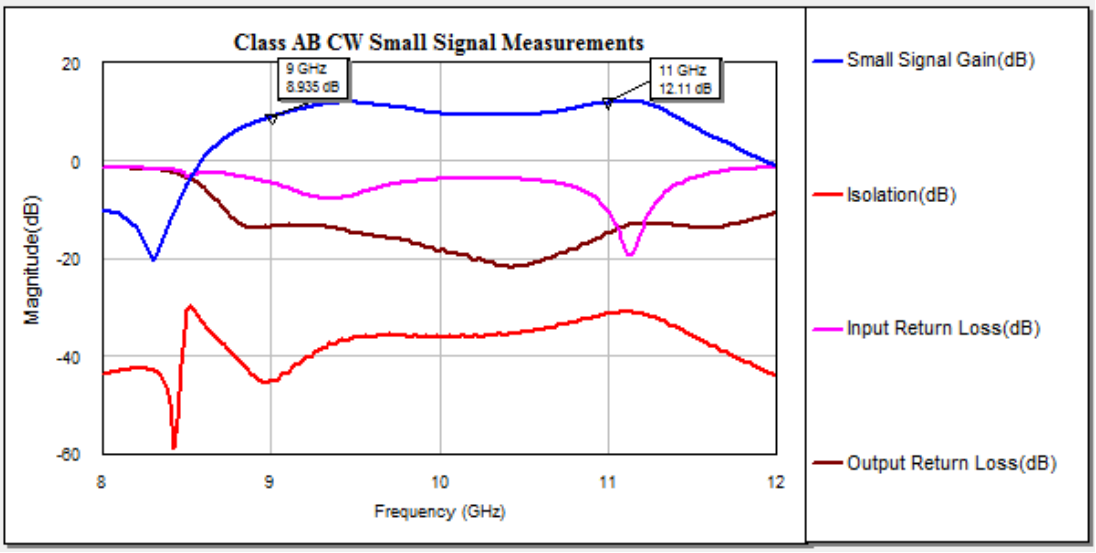


Figure 5.6 Small signal S-Parameters of the fabricated PA in CW Class AB mode.

In Figure 5.7, output power levels at each measurement frequency are shown as a function of input power level. It is seen that measured output power is between 42.15 dBm and 43.9 dBm. The minimum output power level in the operation band is a little lower than the simulation results. However, in simulations, effect of the increased case(junction) temperature is not considered. During nonlinear the measurements, the base plate temperature of the transistor die is read around 75°C-80°C using the sensor which is located as close as possible to the transistor die. The high base plate temperature value is one the possible reasons of the difference of simulated and measured output power levels.

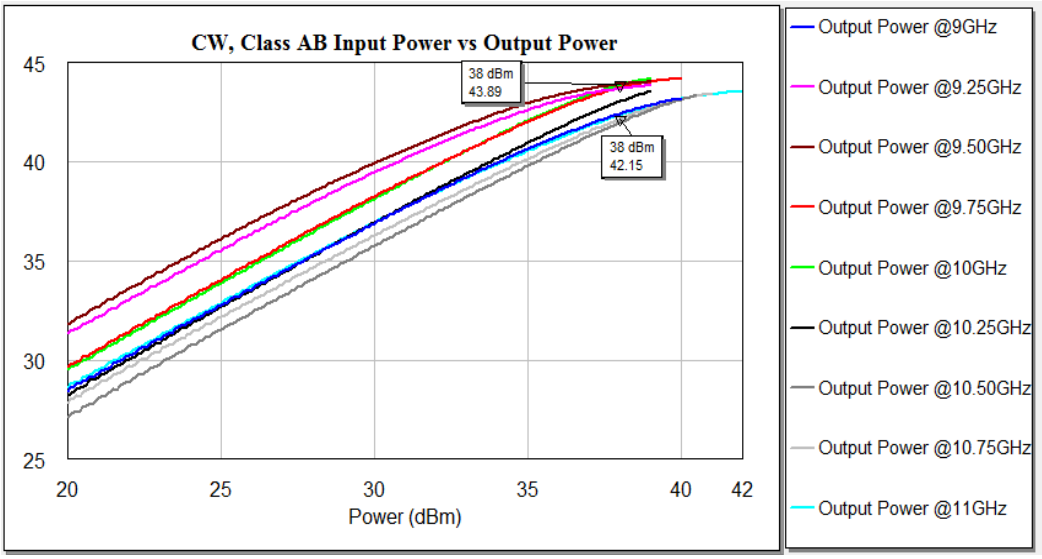


Figure 5.7 Output power as a function of input power for different frequency points.

Power-Added Efficiency(PAE) and Drain Efficiency(DE) measurements are given in Figure 5.8 and Figure 5.9, respectively. It is seen that PAE values are between 28% and 42% whereas DE varies between 40% and 53% in the band of interest. The huge difference between PAE and DE is caused by low power gain seen at large signal operation. At large signal operation, input power becomes comparable to output power and injected DC power so it lowers the PAE value.

If an efficient and high gain driver stage is added to the fabricated PA then without increasing the injected DC power, PAE value can be increased by high power gain values.

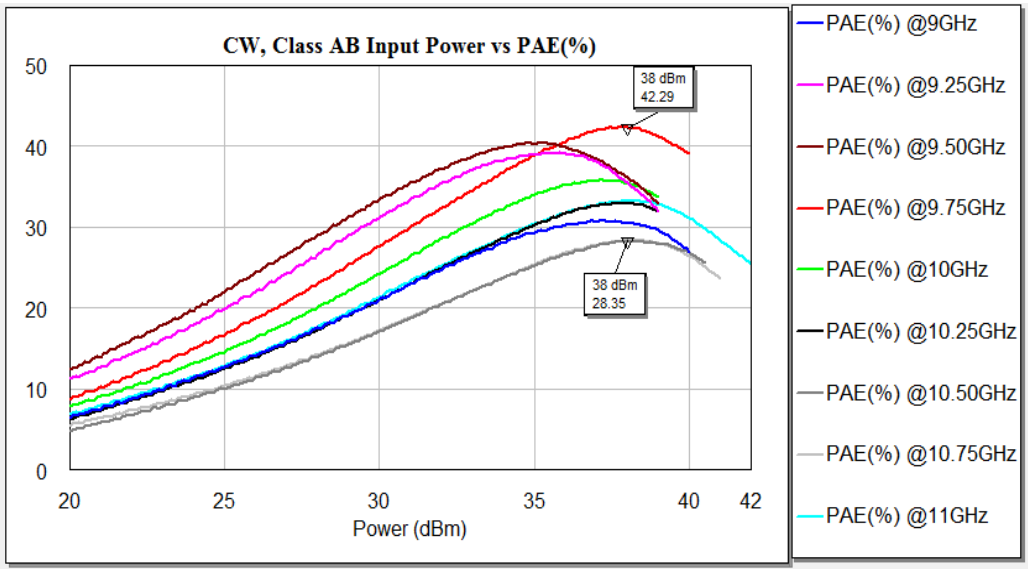


Figure 5.8 PAE as a function of input power for different frequency points.

The high temperature seen on the base plate of the die is again the main reason of the low PAE values. Due to the high temperature, both output power and power gain values decrease so thus the PAE gets lower. Therefore, a more powerful cooling method providing lower base plate temperature level will improve output power, power gain and efficiency characteristics of the PA.

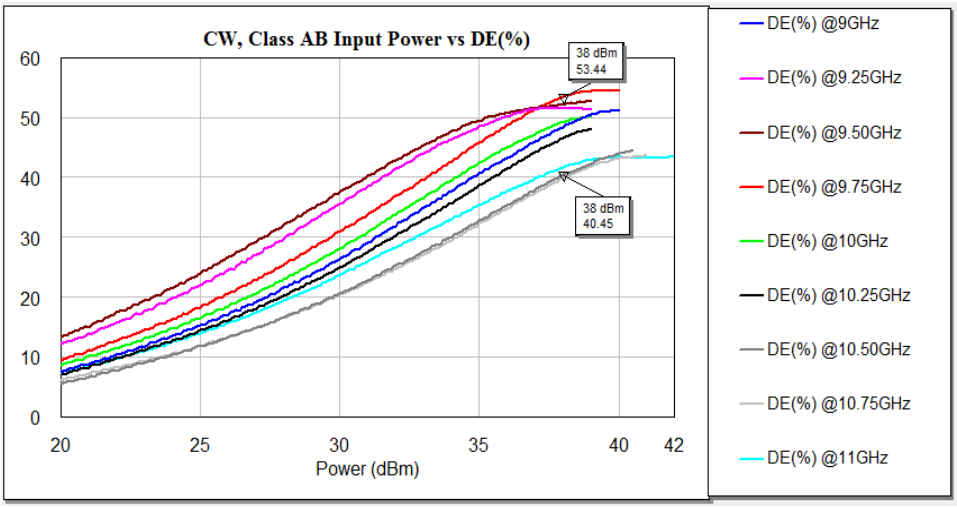


Figure 5.9 DE as a function of input power for different frequency points.

AM/AM and AM/PM characteristics mentioned in Chapter 2 are the other two behavior of the PA. In Figure 5.10, AM/AM behavior of the PA is shown for each frequency point. It is seen that, gain of the amplifier decreases continuously not only after the P_{1dB} point of the PA. This behavior is one of the fundamental characteristics of the GaN amplifiers. Therefore, it is hard to define a P_{1dB} point and gain compression level since the gain decreases for subsequent input power point so saturation output power level must be used instead of compression level and P_{1dB} to define the PA behavior.

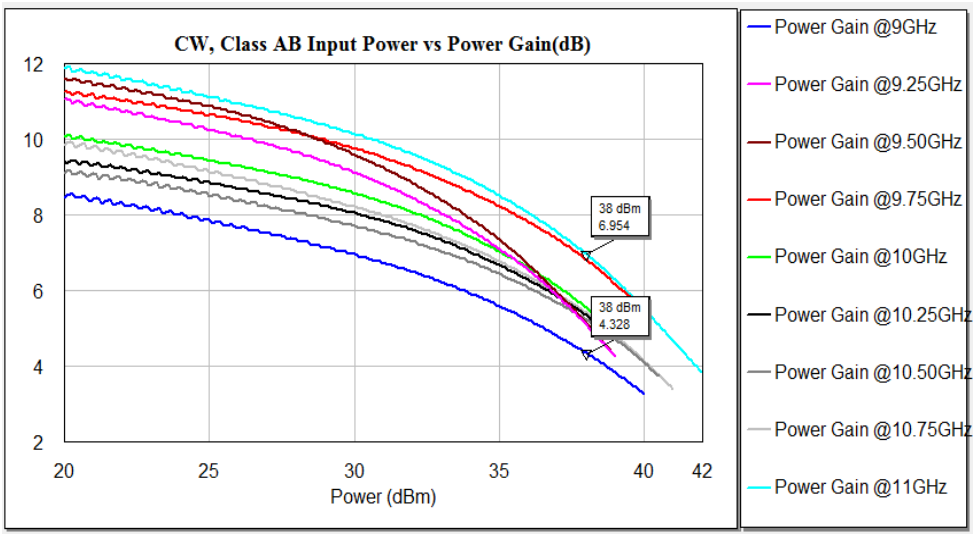


Figure 5.10 Power gain(AM/AM) as a function of input power for different frequency points.

AM/PM behavior of the PA is given in Figure 5.11 at each measurement frequency. To observe the behavior in more detail, AM/PM characteristic at 10 GHz is given alone in Figure 5.12. It is seen that insertion phase changes slightly as the PA goes into deep saturation.

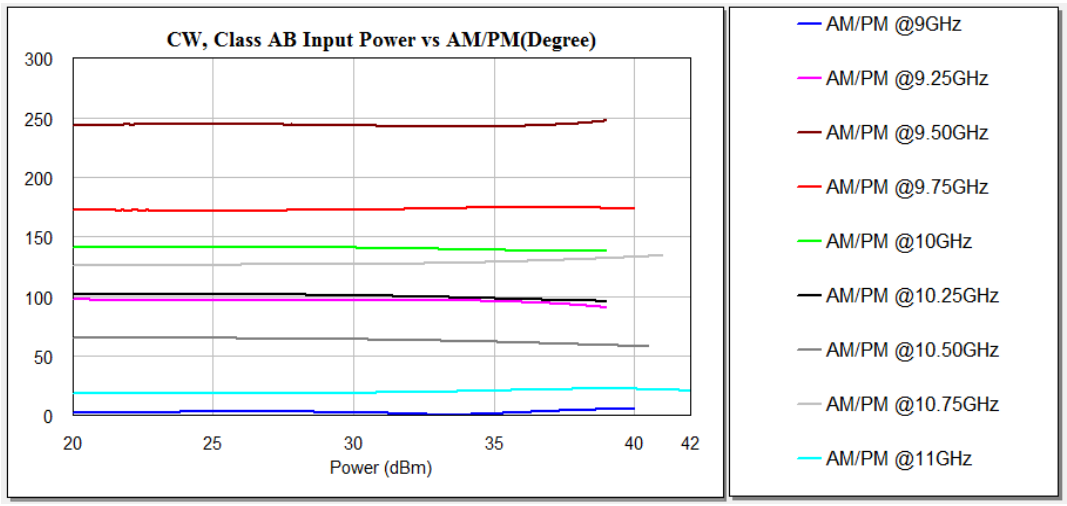


Figure 5.11 AM/PM characteristics at different frequency points.

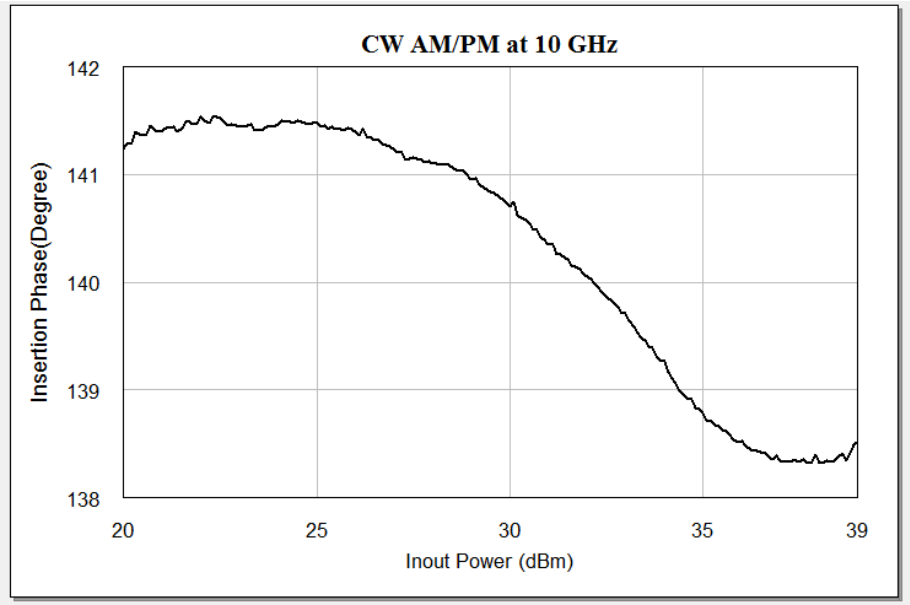


Figure 5.12 AM/PM Characteristics at 10 GHz.

Usually, in a communication system, the PA is expected to work under constant input power conditions across the frequency band of interest. In Figure 5.13 and Figure 5.14 output power, PAE and DE measurement results are given at a constant 38 dBm input power level. It is seen that output power is above 42 dBm with a maximum value of approximately 44 dBm. PAE is above 30% and DE is above 40% across the frequency band.

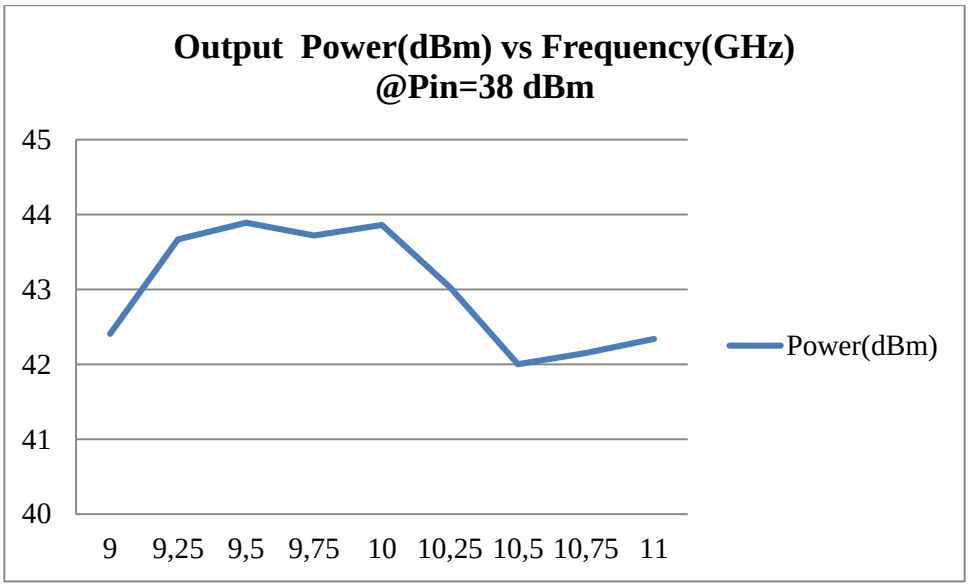


Figure 5.13 Output Power at constant Input Power.

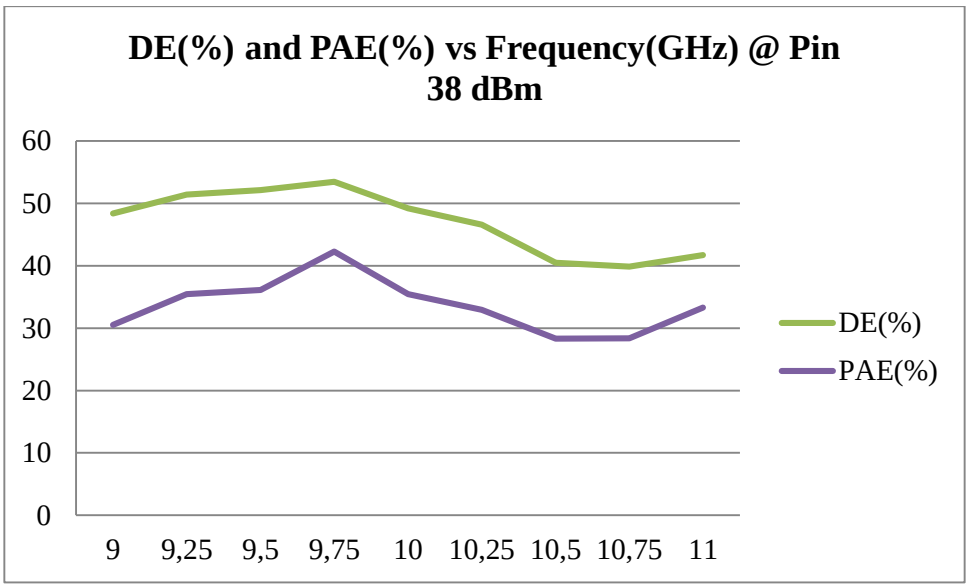


Figure 5.14 DE and PAE at constant Input Power.

5.4 PULSED FUNDAMENTAL MEASUREMENTS

During the pulsed measurements, both drain voltage and RF input signal is provided as pulsed signals. The biasing conditions and pulse parameters are given in Table 5.2. The PA is biased in Class AB mode and duty cycle of the pulse is 10%. The measured

current is the average of instantaneous drain current so the actual bias current is around 240 mA which is same as the CW measurement bias point.

Table 5.2 Class AB Bias Voltage and Current Values under Pulsed Operation

Class AB Bias Conditions				
Gate Voltage(V)	**Drain Voltage(V)**	**Drain Current(mA)-Average**	**Pulse Width(us)**	**Period(us)**
-2.64	40	24	50 us	500 us

The pulsed drain voltage of the PA is measured and given in Figure 5.15. As it is seen the drain voltage has overshoots at both rising edge and falling edge of the voltage waveform. However, the voltage level and switching times are observed as expected. The ringing at the beginning and end of the waveform will cause distortion at the pulse spectrum and this distortion will be shown in following sections.

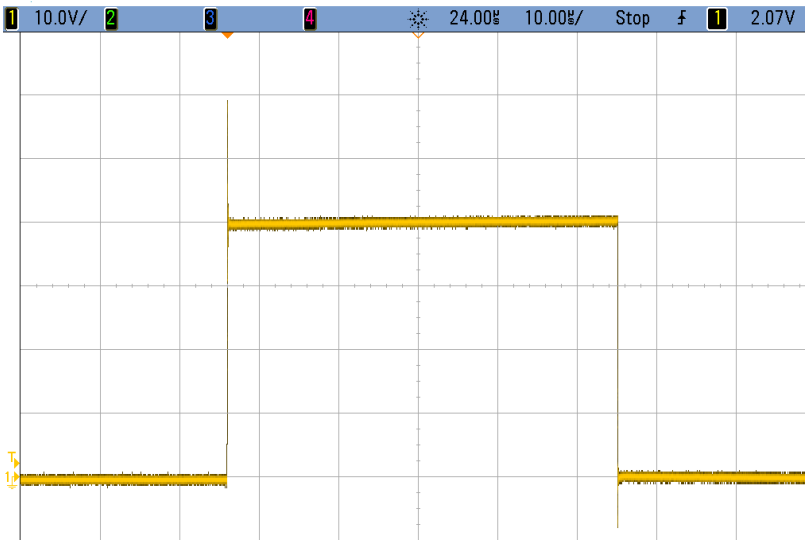


Figure 5.15 Pulsed drain voltage.

Using a peak power analyzer device, peak output power level when both the drain voltage and RF input signal is ON is observed. The shape of the output power level envelope is given in Figure 5.16. The RF pulse width is slightly narrower than the

drain voltage ON time to have a clean pulse shape at the output. As it is seen the power level is around 44 dBm at the beginning of the pulse and it drops down to 43.9 dBm level at the end of the pulse.

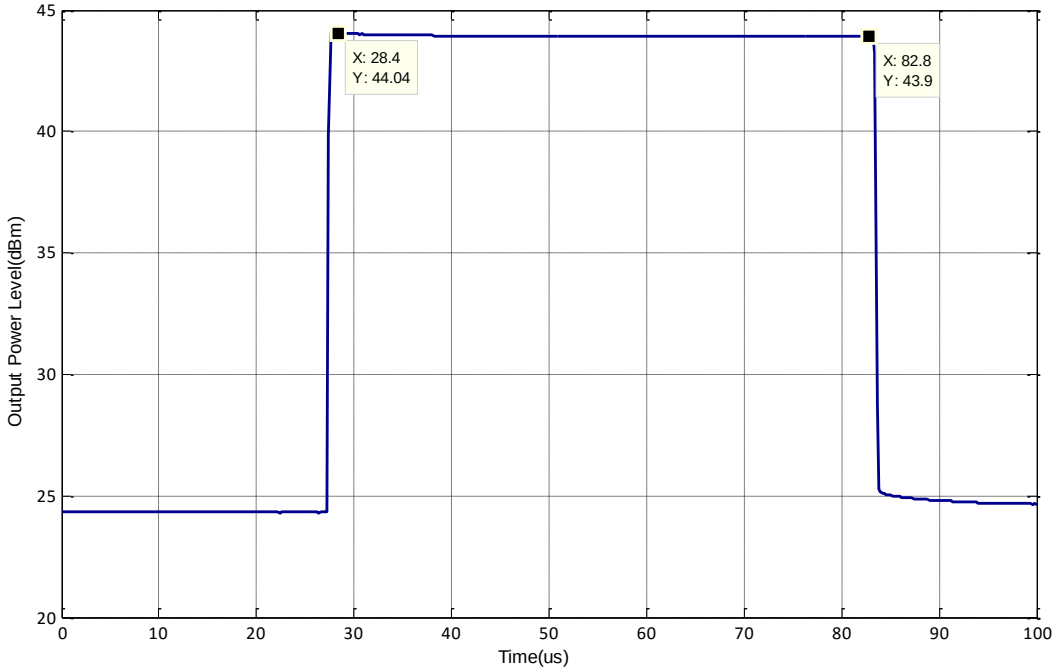


Figure 5.16 Output Power Envelope of RF output signal.

The decrease in peak power level in pulsed operation is called as “Pulse Amplitude Droop”. Pulse amplitude droop is an undesired behavior seen in pulsed operation since the average power and the total energy transmitted by antenna will be lower than expected. The main reasons of the pulse droop decreasing power generation capability and power gain due to the increase in temperature during the On time of pulse. In this work, the droop is measured as 0.1 dB which is an acceptable value as is it seen in Figure 5.17. There are several methods [22] proposed to decrease the pulse amplitude droop such as increasing drain bias current in time along with pulse width to compensate the power gain reduction but the complexity of amplifier biasing circuits will be increased by additional controls.

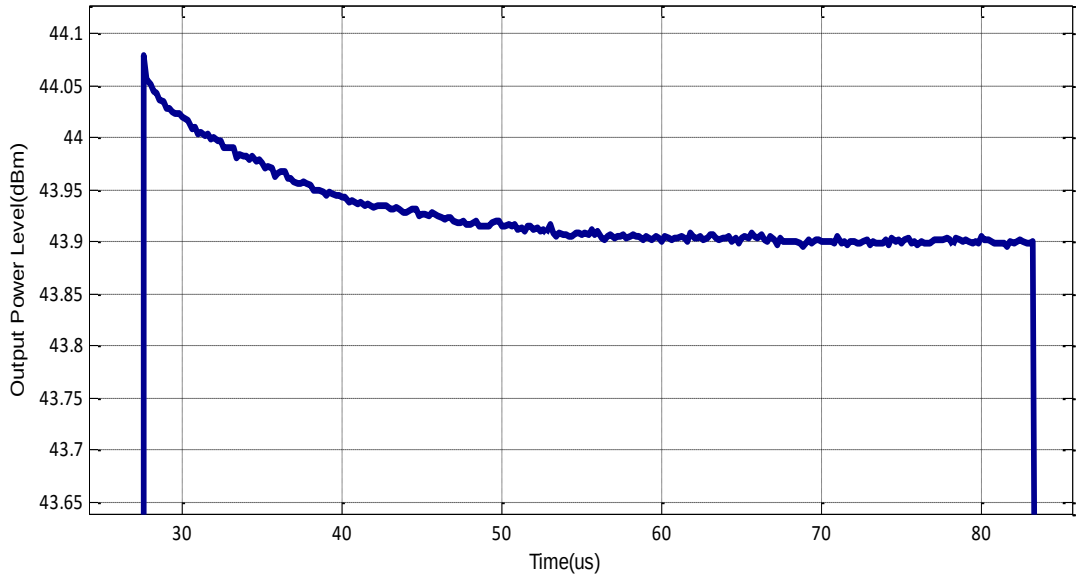


Figure 5.17 Pulse amplitude droop along the pulse width.

The S-Parameters measured under pulsed drive is shown in Figure 5.18. It is observed that small signal gain of the amplifier is slightly higher than the CW drive case. The reason for the increase in the gain is the lower temperature values occurred on the base plate of the transistor die. Since the amplifier works only in 10% duty cycle, the average dissipated power will be approximately 1/10 of the CW operation power dissipation. In transient point of view, base plate of the temperature increases when the pulse in ON whereas the temperature decreases when the pulse is OFF since there is not any power dissipation on the active device. As a result, the average temperature of the base plate will be lower in pulsed operation.

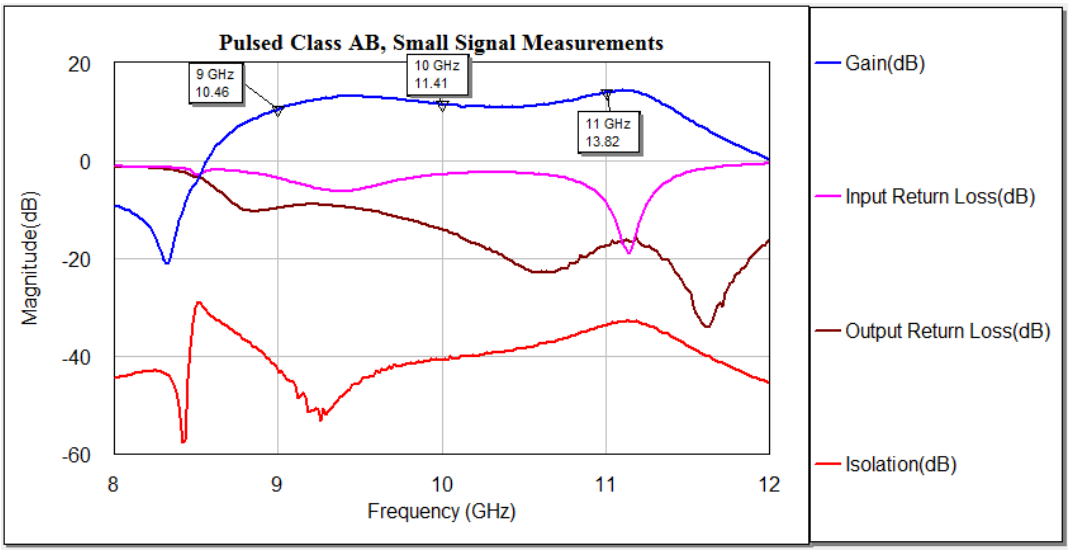


Figure 5.18 Small signal parameters in pulsed mode operation.

In Figure 5.19, output power at each measurement frequency point as a function of input power. It is seen on the graph that the output power level varies between 43.1 dBm and 44.4 dBm across the frequency band of interest. When it is compared to the CW output power measurements, it is observed that the pulsed mode operation provides better than 1 dB improvement in output power. The reason for that improvement is again lower average junction temperature during the operation.

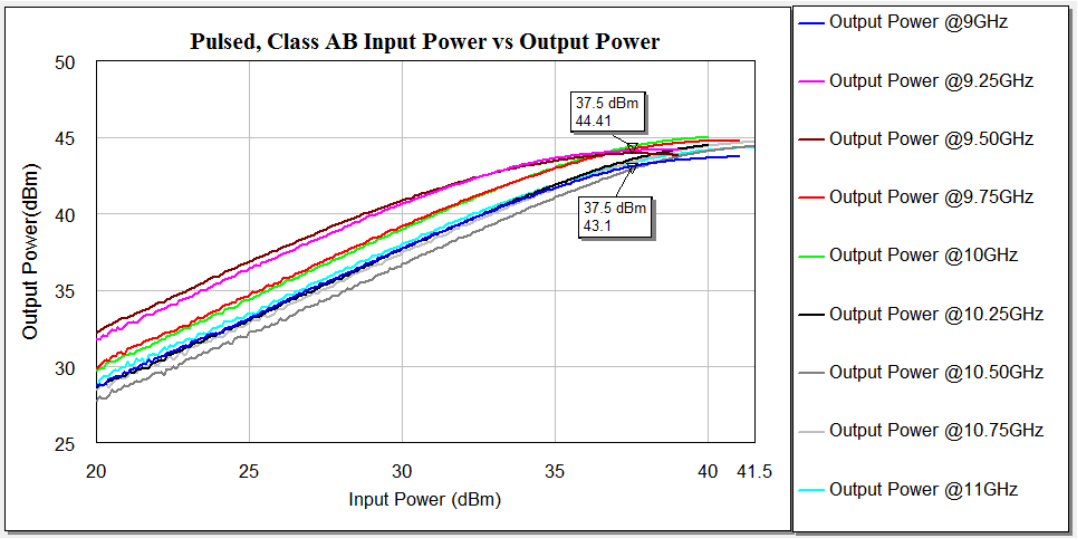


Figure 5.19 Pulsed output power as a function of input power for different frequency points.

Power-Added Efficiency (PAE) and Drain Efficiency (DE) measurements under pulsed drive are given in Figure 5.20 and Figure 5.21, respectively. It is seen that PAE values are between 43% and 55% whereas DE varies between 52% and 52% in the band of interest. The efficiency values under pulsed drive are remarkably higher than the CW case. The reason for this improvement is that lower required input power level and higher output power due to lower temperature values.

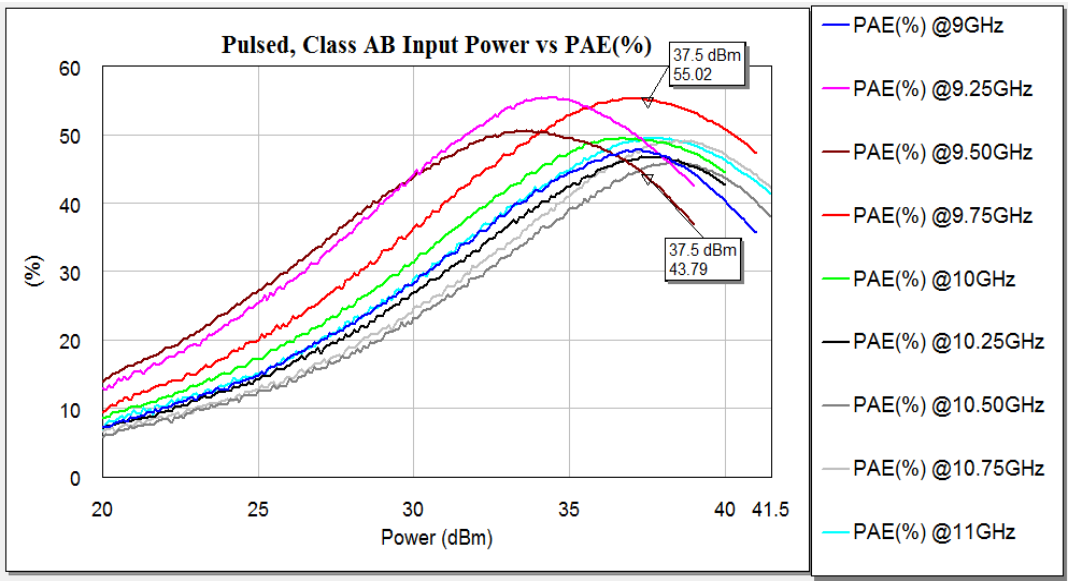


Figure 5.20 Pulsed PAE (%) as a function of input power for different frequency points.

The PAE and DE values are closer to each other in pulsed measurement since higher power gain obtained in pulsed mode. The input power becomes less comparable to output power and injected DC power so it becomes less effective in PAE calculations.

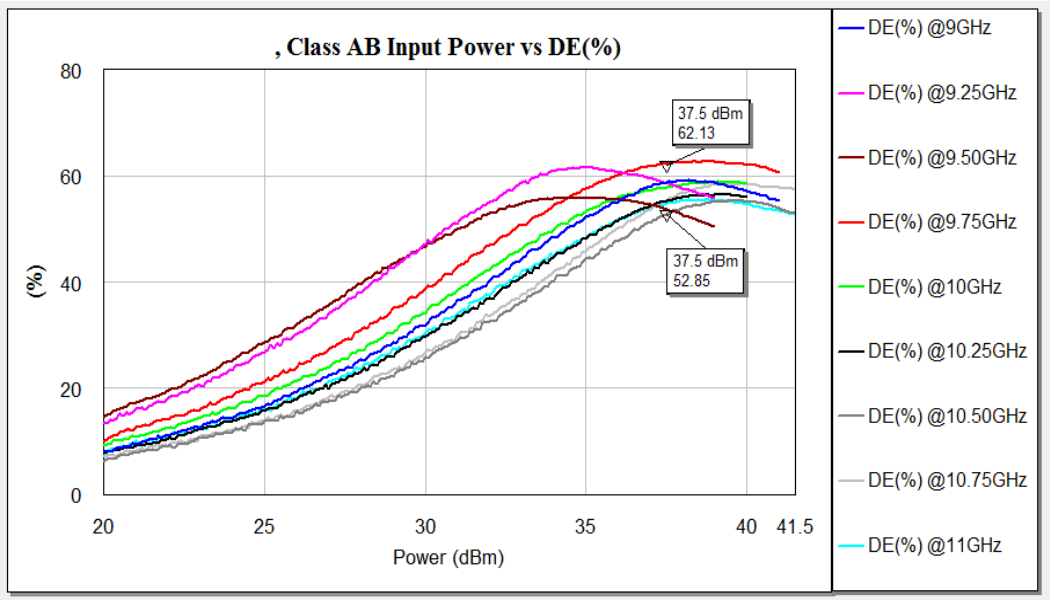


Figure 5.21 Pulsed DE (%) as a function of input power for different frequency points.

In Figure 5.22, AM/AM behavior of the PA is shown for each frequency point. The power gain values at saturation region of the PA have a minimum of 7 dB and a maximum of 10.1 dB.

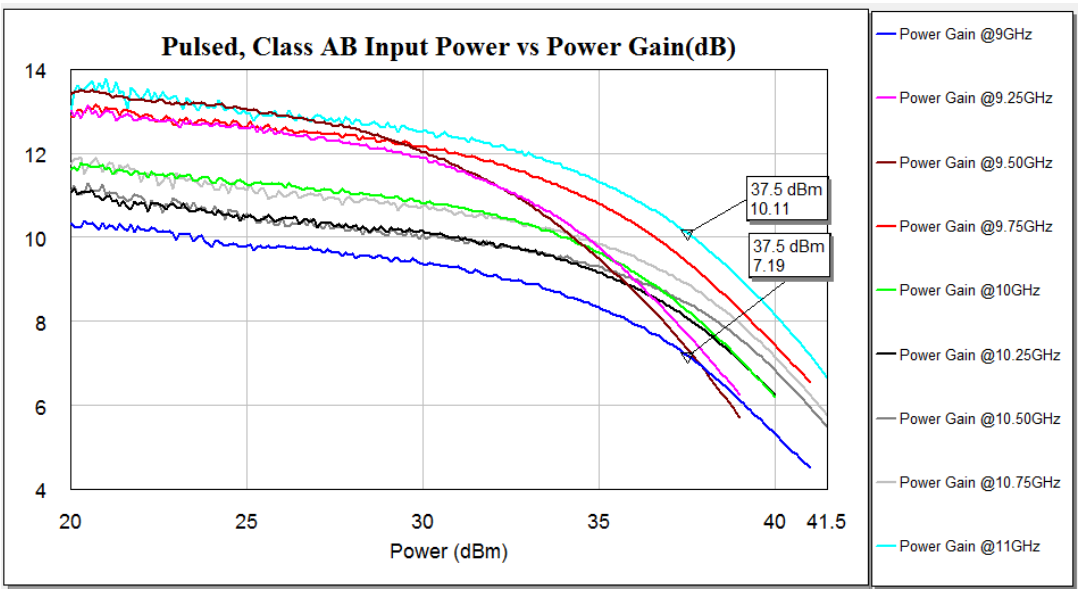


Figure 5.22 Pulsed power gain as a function of input power for different frequency points.

In Figure 5.23, AM/PM behavior of the PA is shown for each frequency point with respect to input power. The insertion phase of the PA changes slightly as the nonlinearity increases with input power level.

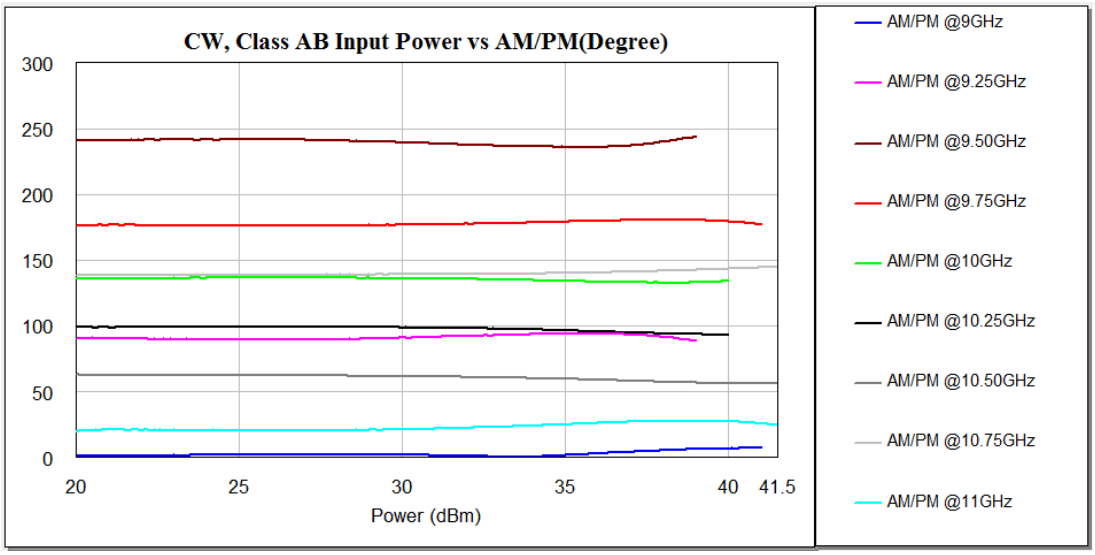


Figure 5.23 Pulsed AM/PM characteristics as a function of input power for different frequency points.

In Figure 5.24, AM/PM characteristic of the PA at 10 GHz is given in more detail. It is seen that although the absolute value of the phase is imperceptibly differs from the CW AM/PM measurement, the behavior of the insertion phase as a function of input power remains unchanged. The small difference in absolute value of the phase between pulsed and CW measurements are probably due to the higher temperature values seen on both active device and passive elements such as microstrip circuits and RF connectors.

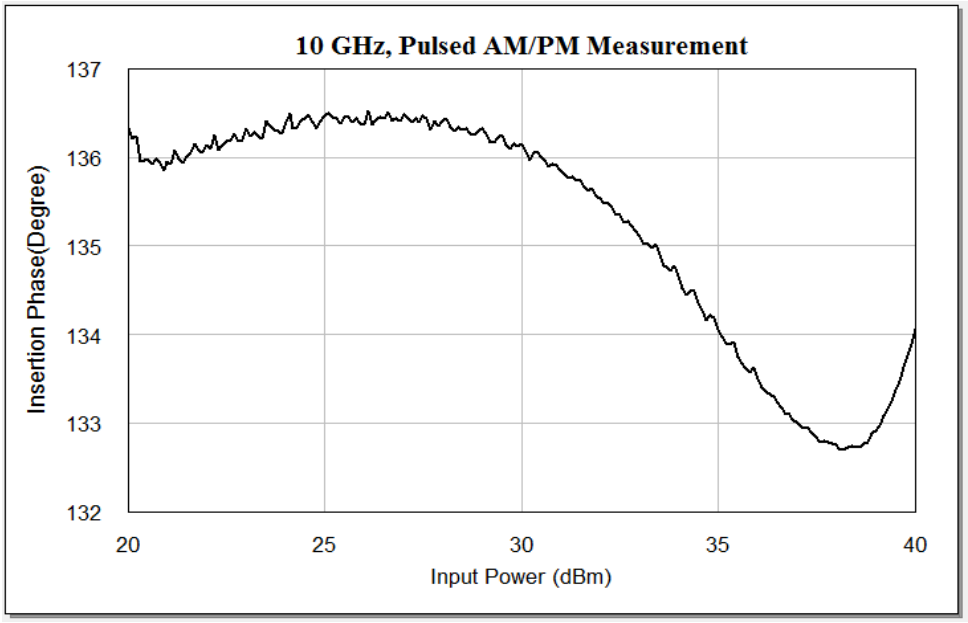


Figure 5.24 Pulsed AM/PM characteristics at 10 GHz.

When the input power level is kept constant at 37.5 dBm across the frequency band of the PA, the power at the output of the PA is obtained as in the Figure 5.25. As it is seen, the minimum value of the power is around 43 dBm and maximum value is around 44.5 dBm.

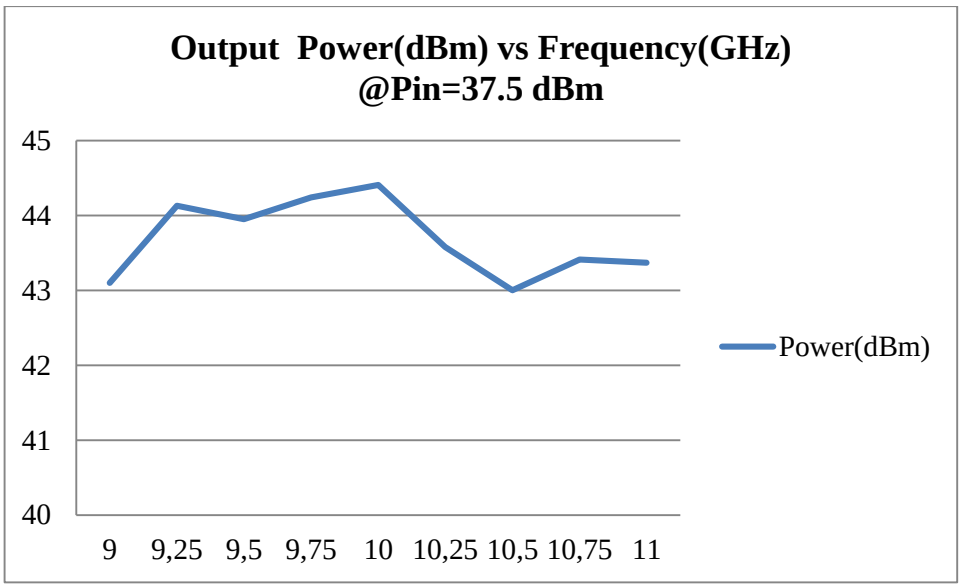


Figure 5.25 Output power versus frequency at 37.5 dBm input power.

When the input power level is 37.5 dBm, the measured DE and PAE values are shown in Figure 5.26. It is observed that both in terms of output power and efficiency parameters, the PA works significantly better in pulsed operation.

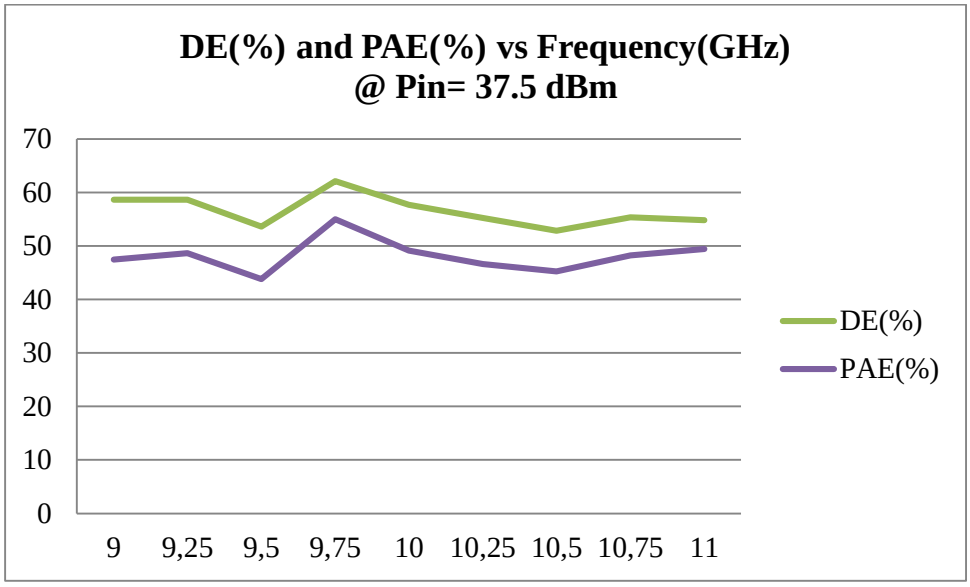


Figure 5.26 DE (%) and PAE (%) versus frequency at 37.5 dBm input power.

5.5 PULSE PHASE STABILITY MEASUREMENTS

In pulsed applications, such as radars in defense systems, the insertion phase of the power amplifier during the pulsed is expected to stay constant since the phase change will deteriorate communication performance of the system. Moreover, the insertion phase values of subsequent pulses in a pulse burst are also expected to be same for all pulses. However, mostly due to the thermal transient events on semiconductor and passive circuit elements seen when the pulse is ON, there will be phase change along the RF pulse. In addition, since the power amplifiers are not memory-less devices, there may be pulse-to-pulse phase changes in a pulse burst.

Using time domain pulse measurement capability of the network analyzer device in the measurement setup, ten subsequent pulses are positioned on the time axis of the network analyzer as shown in Figure 5.27. In the Figure, there are ten pulses having 100 us pulse width and 509 us pulse period. Six different data sets as shown in Figure 5.27 are captured and saved as data points with respect to time. It is aimed that the six

data sets are independent from each other by shutting down all the system after each measurement and waiting for a while to provide independence between measurements. The measurement frequency is set to 10 GHz for all time domain measurements and the PA works in nonlinear region.

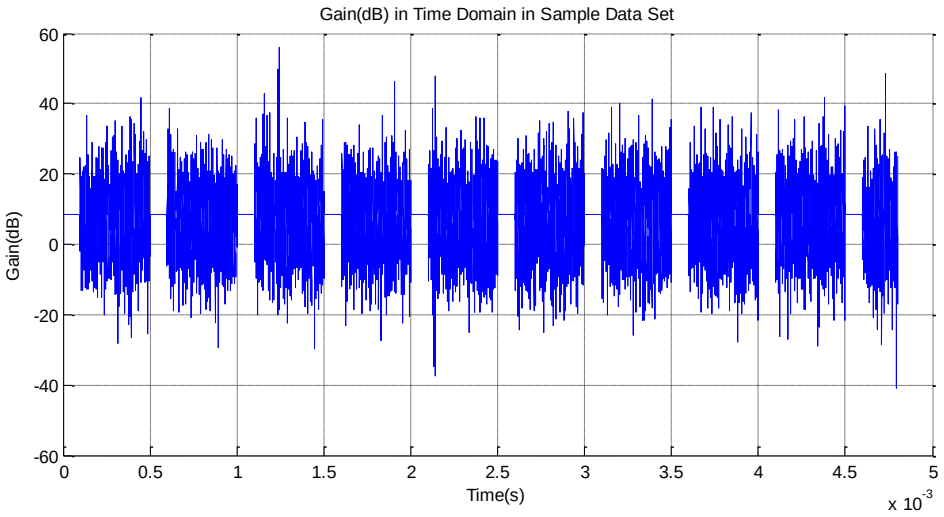
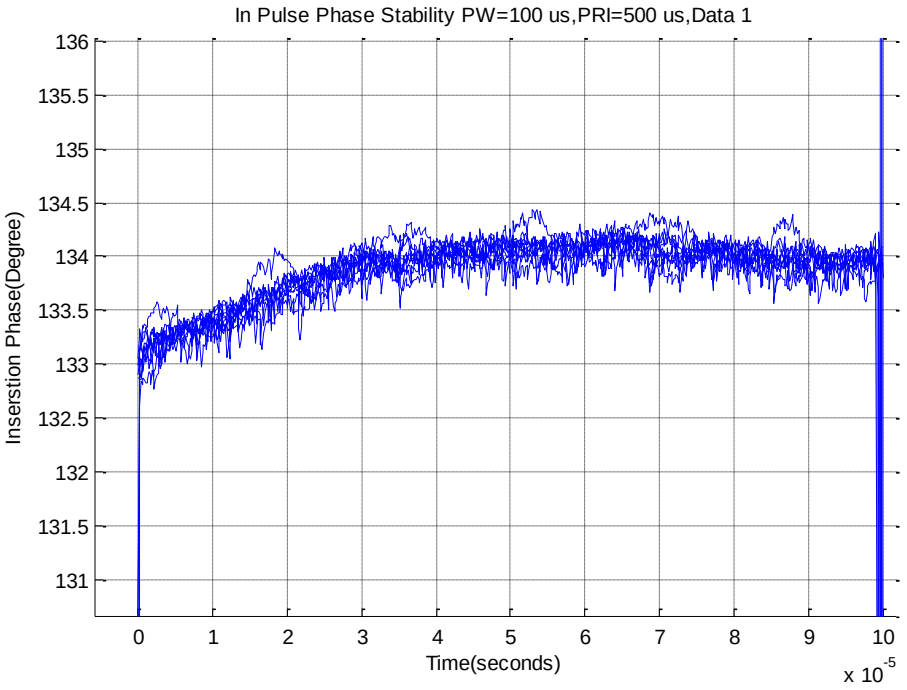


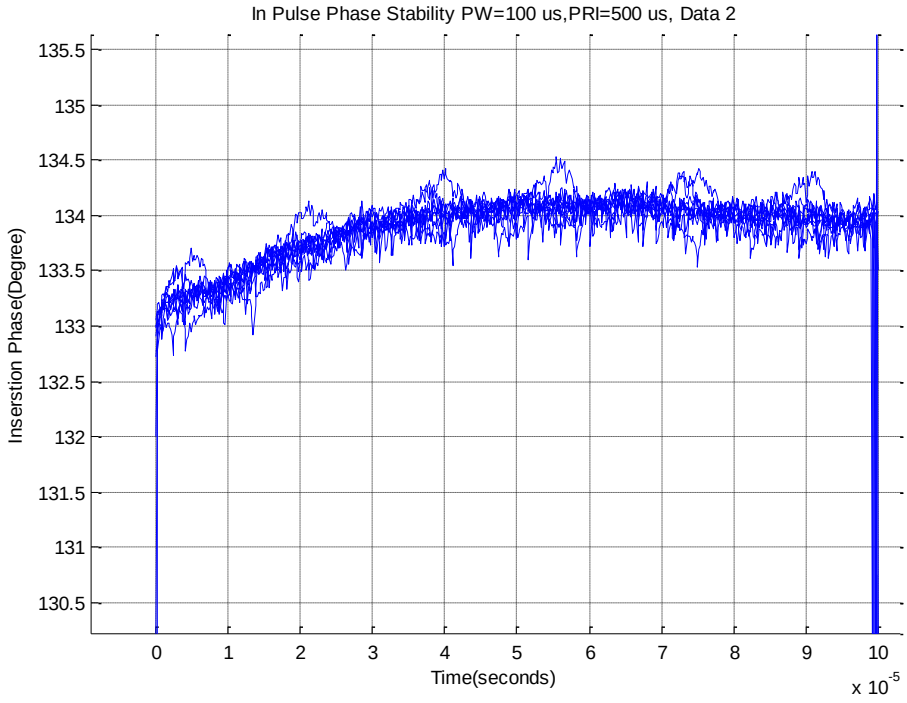
Figure 5.27 A sample time domain pulse data set.

In Figure 5.28 and Figure 5.29, all ten pulses in a dataset is drawn on top of each other. This means that, for instance in Figure 5.28, only ON times of ten pulses of dataset 1 are drawn together. Figure 5.28, 5.29 and 5.30 point out that phase change during the ON time of pulses are around 1-1.5° and all pulses are almost identical to each other.

In Figure 5.28 through 5.30, it is seen that there are some ripples on the phase values of the signal during the pulse. However, if the ripple behavior is examined in detail, it is observed that there is not a periodic structure. In addition, averaging and smoothing functions of the network analyzer is closed during the time domain pulse measurements and the relative phase change during the ripple is around 0.25° so the fluctuations on phase are ignorable.

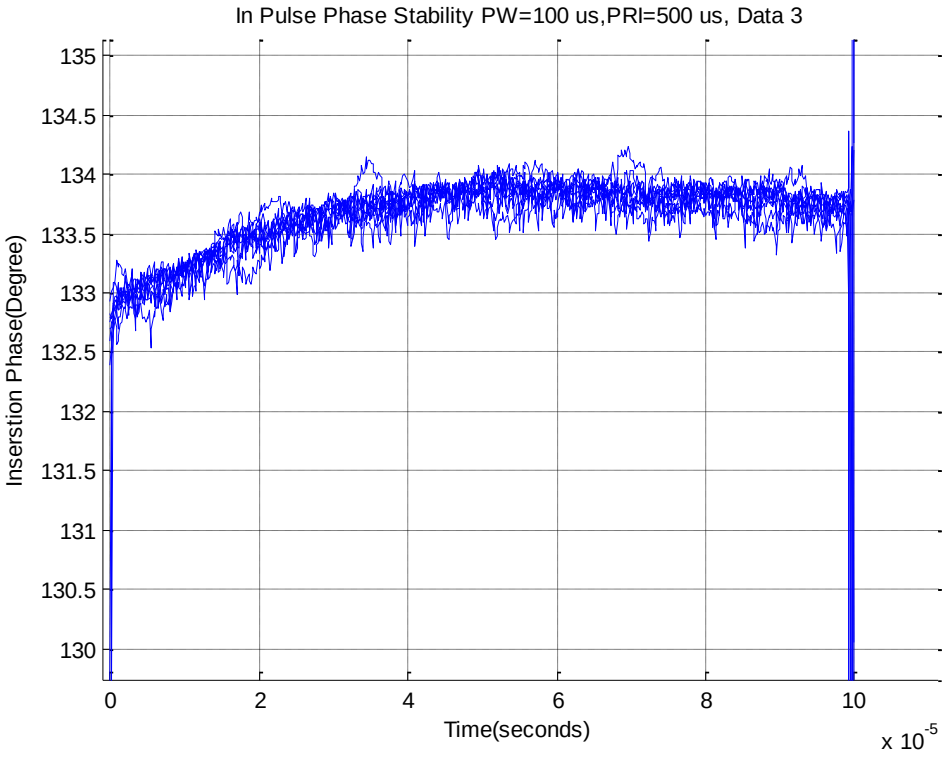


a)

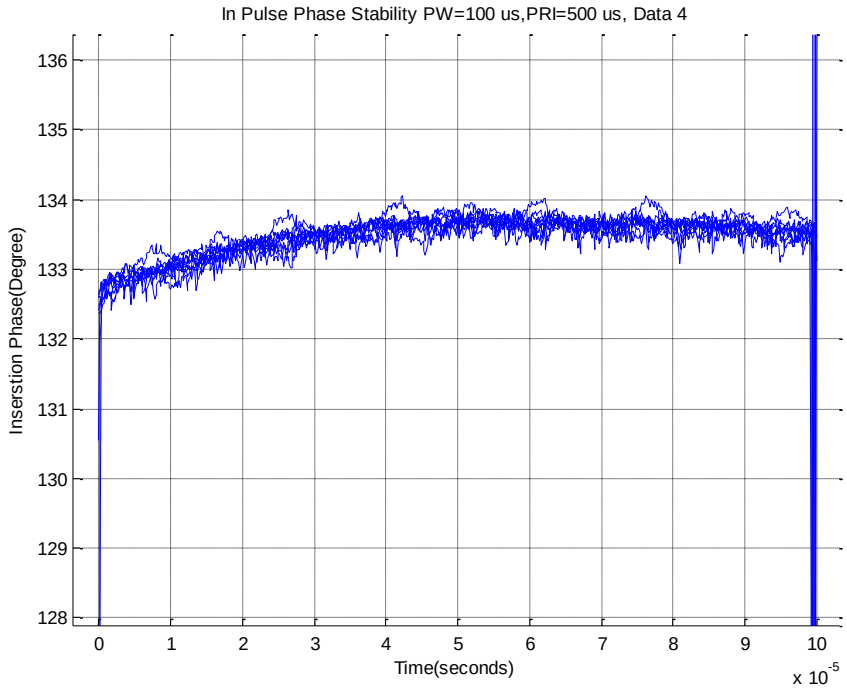


b)

Figure 5.28 Phase values of ten pulses of data sets 1 and 2.

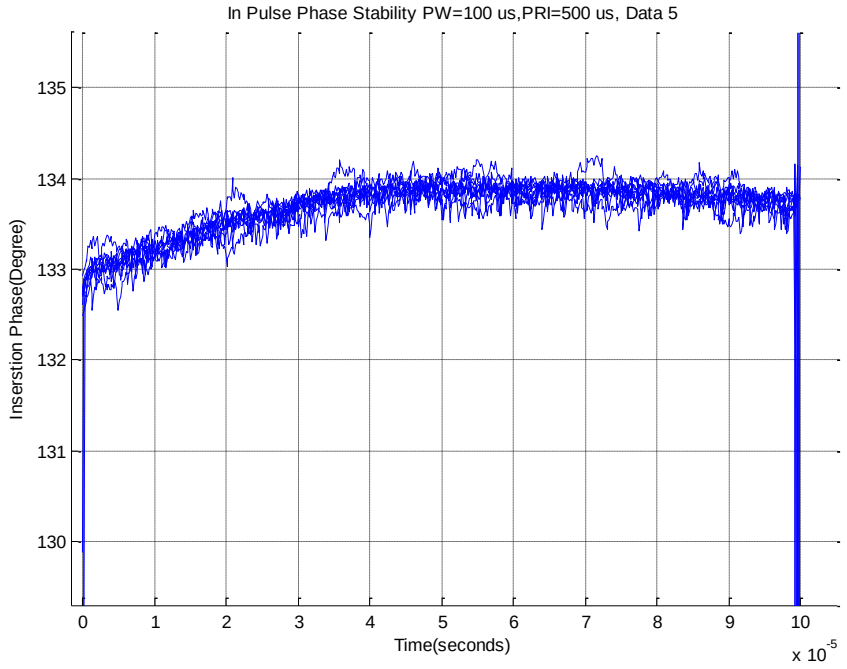


a)

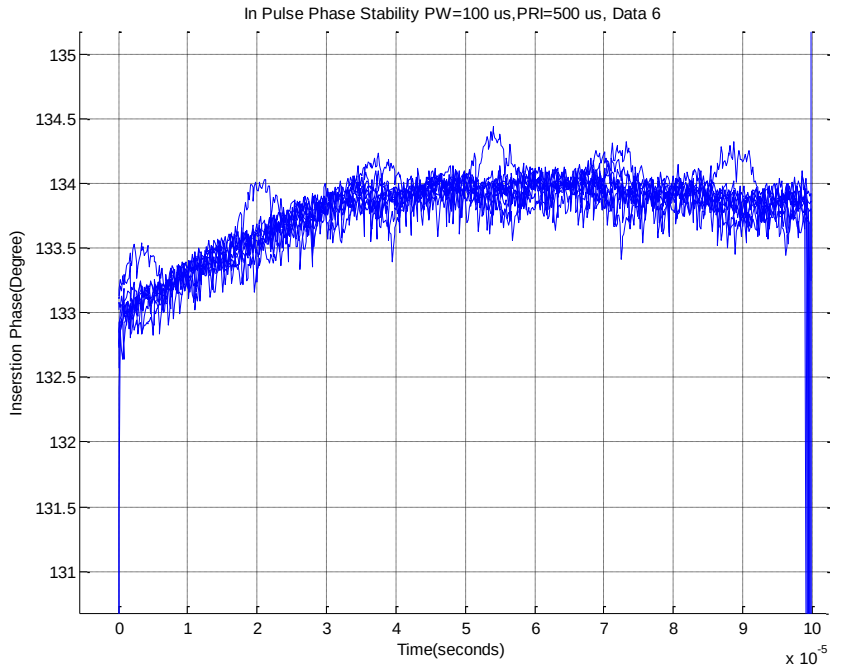


b)

Figure 5.29 Phase values of ten pulses of data sets 3 and 4.



a)



b)

Figure 5.30 Phase values of ten pulses of data sets 5 and 6.

In Figure 5.31, insertion phase of the 50th us of each pulse on each dataset are shown with respect to pulse number. Each of the curves with different colors corresponds to one dataset and one dataset has 10 points being 50th us of each of ten pulses in a dataset. The figure shows that pulse to pulse phase variation is less than 1° and phase of each dataset is consistent with other datasets.

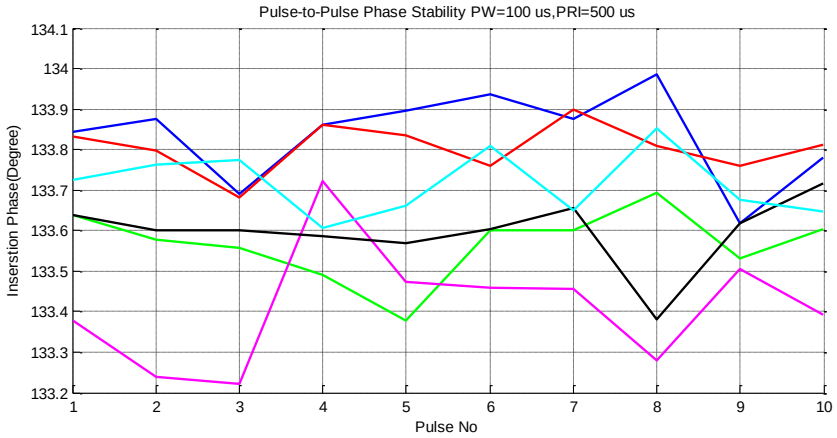


Figure 5.31 Pulse-to-pulse phase change for all datasets.

5.6 SPECTRUM MEASUREMENTS

In this section, frequency spectrum of different drive conditions will be compared and the things that alter the spectrum will be explained.

In this spectrum measurements, the PA is used under pulsed operation conditions. As explained in Chapter 2, there are three ways to realize a pulsed mode operation. In this measurement, the pulsed operation modes shown in Figure 2.12 and Figure 2.13 in which only supply modulated and both supply and RF signal modulated, respectively.

The pulsed RF signal can be expressed in mathematical form as follows:

$$S(t) = rect\left(\frac{t}{\tau}\right) x \, \mathrm{A}\cos(2 \times pi \times f_c \times t) \qquad (5\text{-}1)$$

where;

$$rect\left(\frac{t}{\tau}\right): rectangular\ signal\ with\ time\ width\ of\ \tau\ and\ with\ period\ T,$$

$$f_c: RF\ frequency.$$

Equation (5.1) points out that a pulsed RF signal can be expressed as a multiplication of a rectangular signal and a continuous sinusoidal signal. Then, in frequency domain, the resultant expression of the pulsed RF signal can be calculated as follows:

$$S(f) = \tau sinc(f\tau) \times \left\{\frac{A}{2}[\delta(f - f_c) + \delta(f + f_c)]\right\} \quad (5\text{-}2)$$

$$S(f) = \frac{\tau A}{2}[sinc\big((f - f_c)\tau\big) + sinc((f + f_c)\tau) \quad (5\text{-}3)$$

Which is a convolution of a sinc function with two impulses and the convolution operator gives rise to two frequency shifted sinc functions at f_c and $-f_c$. However, the S(f) function is only the envelope of the frequency domain expression of a pulse train. The period of the rectangular pulses will also be effective in calculation of frequency domain definition and the total transformation can be expressed graphically as shown in Figure 5.32.

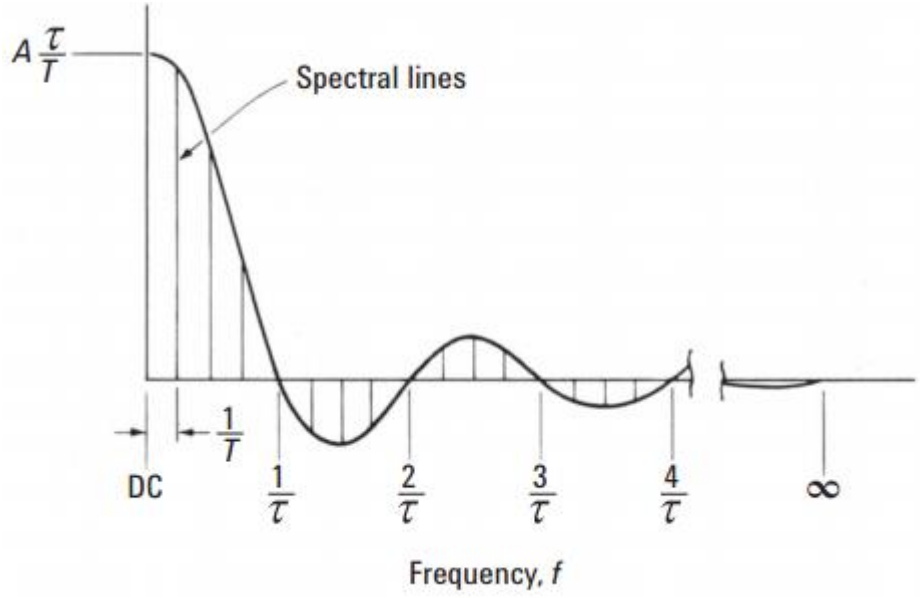


Figure 5.32 Frequency spectrum of a rectangular pulse train.

When the signal shown in Figure 5.32 is convolved with frequency response of a continuous RF signal, the obtained ideal frequency spectrum of a pulsed RF signal will be as shown in Figure 5.33. The PRF parameter is equal to the frequency of pulse train.

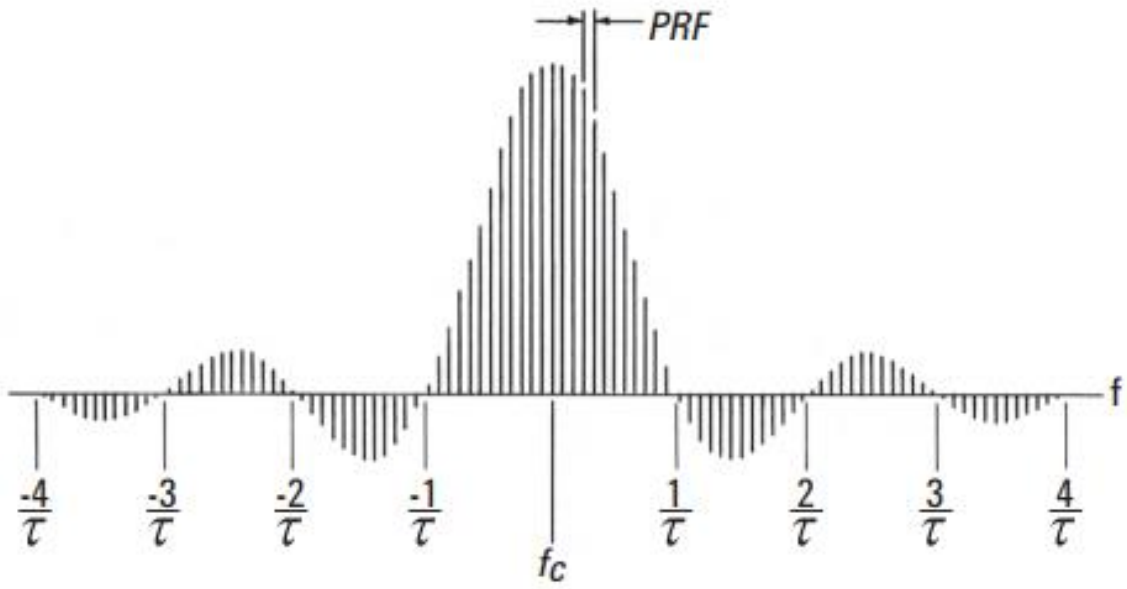


Figure 5.33 Frequency spectrum of an ideal RF pulse train.

The output signal spectrum of the PA driven in pulsed mode is shown in Figure 5.34. The RF pulse has 100 us pulse width and 1 ms pulse period. The 100 us pulse width corresponds to spectrum nulls occurring at $f_c \pm n\frac{1}{PW}$ (n=1,2,3,4) and the first two nulls are shown in Figure 5.34 using markers. The nulls occur 10 kHz and 20 kHz away from the 10 GHz carrier frequency as expected.

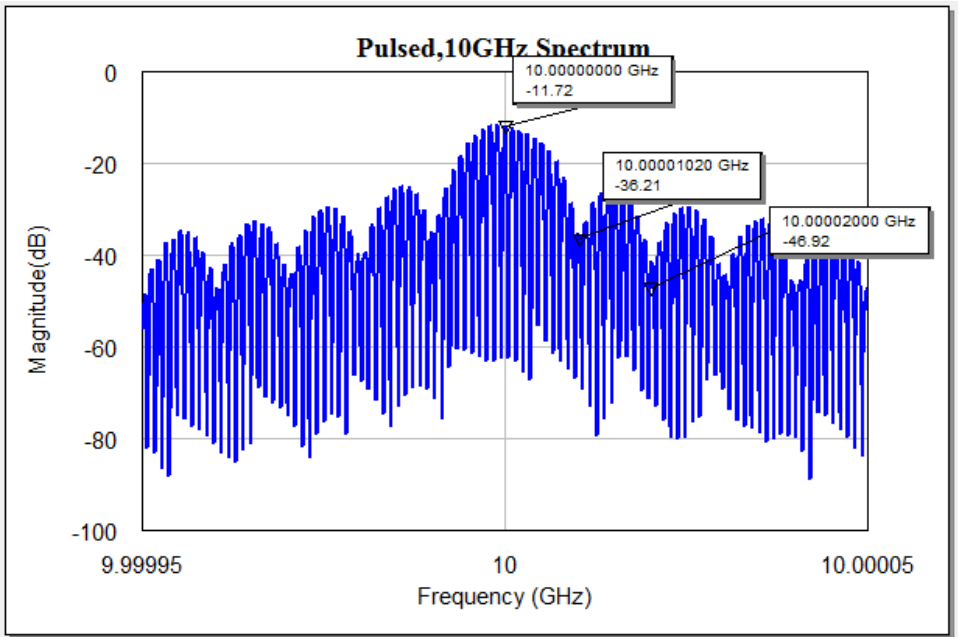


Figure 5.34 Frequency spectrum of measured RF pulse.

Figure 5.35 shows the rising edge of the pulsed drain voltage having signal ringing on top of the signal due to the high order RLC system occurring on the route of drain current. The inductance on the current route is generated due to the parasitic effects of PCB lines or other conductors that current passes through. The step response of high order RLC system to a sudden current change during the rising edge of the pulse causes the ringing on the voltage waveform. The ringing function R(t) can be expressed mathematically as follows:

$$R(t) = A \times \cos(2 \times pi \times f_r \times t) \times \exp(-\frac{t}{RC}) \qquad (5\text{-}4)$$

The R(t) function also affects the output signal of the PA as a multiplication factor to the equation (5-4). The ringing frequency, f_r , can be read by the help of x-axis cursors from the Figure 5.35 as 20 MHz. It can be concluded that if the RF signal coincides with the ringing on the drain voltage then there will be frequency components at $f_c \pm f_r$.

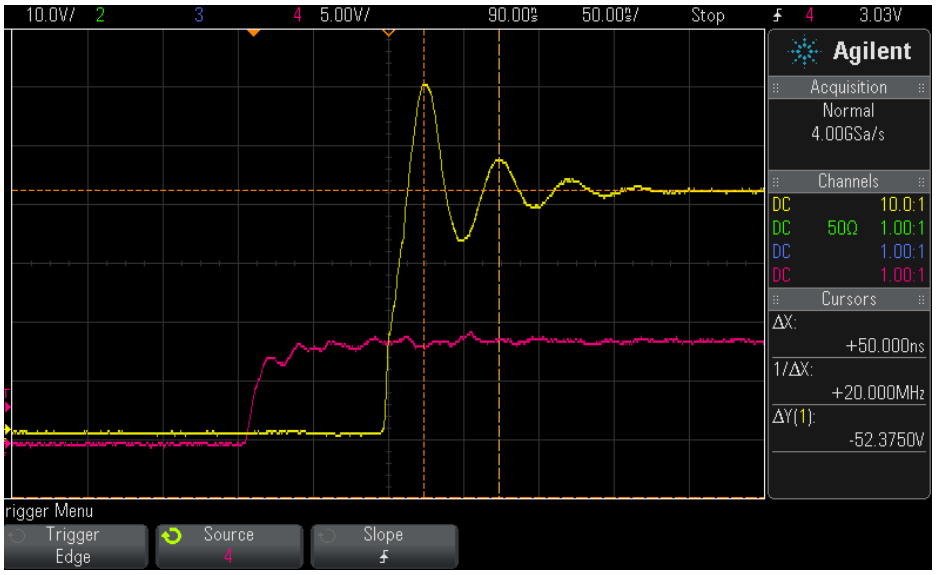


Figure 5.35 Rising edge of the drain voltage waveform with ringing on it.

In practical applications, in order not to coincide the RF signal and drain voltage ringing, two time delays at rising edge and falling edge of the drain voltage waveform are set as shown in Figure 5.36. In other words, width of the drain voltage is kept wider than the pulsed RF signal and RF signal is positioned such that voltage ringing and RF signal are not seen at the same time on the PA.

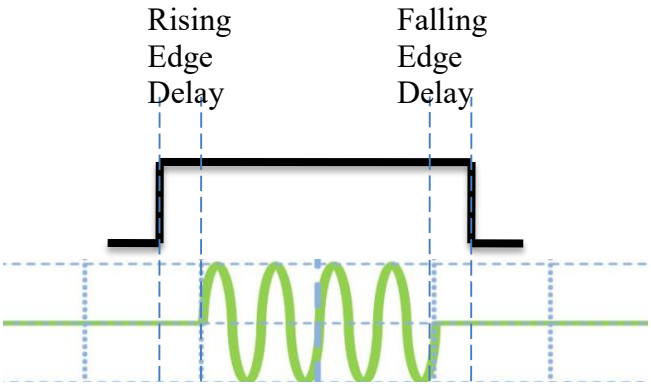


Figure 5.36 Timing of voltage waveform and RF input signal in a typical pulsed RF PA application.

When the timing shown in Figure 5.36 is applied in the measurement, the spectrum of the PA output signal becomes as shown in Figure 5.37. It should be noted that the

frequency span in Figure 5.37 is 100 MHz so that the sinc behavior of the pulse spectrum cannot be differentiated since frequency width of the sinc lobs is 10 kHz.

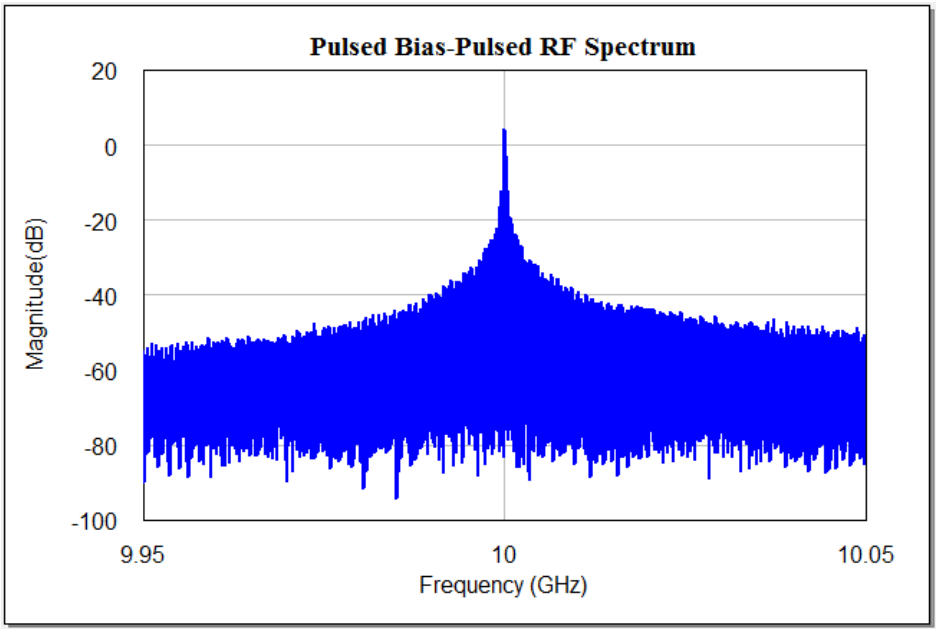


Figure 5.37 100 MHz frequency spectrum of a pulsed RF-pulsed bias PA application.

When the input RF signal is applied continuously and only the drain voltage is modulated according to the pulse parameters, the voltage ringing and the RF signal will be present at the same time. Therefore, it is expected to see frequency components 20 MHz away from the carrier RF frequency 10 GHz. Figure 3.38 shows the resulting spectrum of CW RF input signal and modulated drain voltage applied to the constructed PA. It is seen that there are small frequency components 20 MHz away from the 10 GHz due to the multiplication effect of voltage ringing on the drain voltage waveform. Although, amplitude of the unwanted frequency components, they may degrade -for instance- the system performance of pulsed radar receivers.

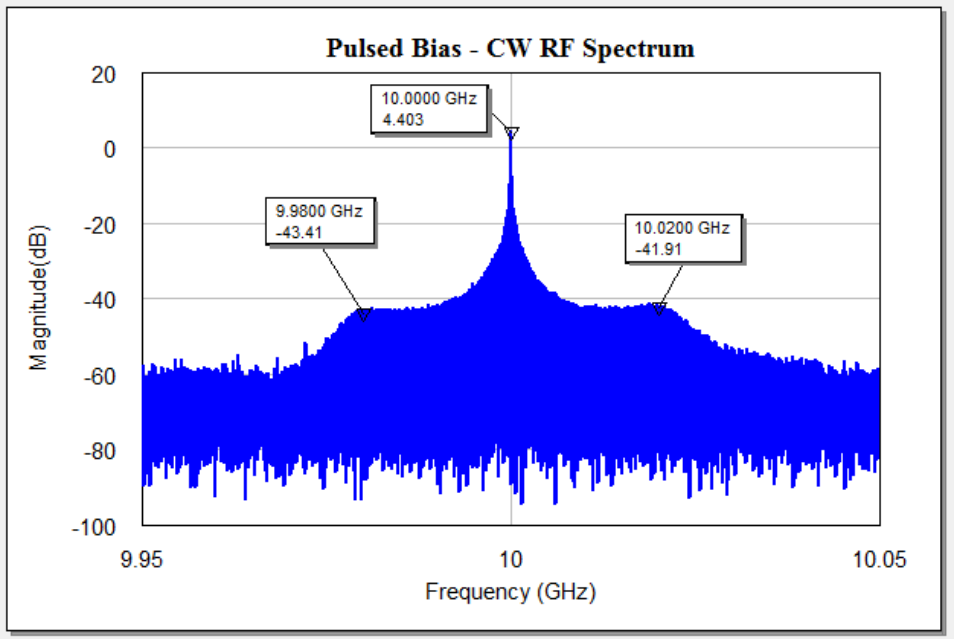


Figure 5.38 Spectrum of CW RF input and modulated drain voltage application.

5.7 DISTORTION MEASUREMENT

Another characterization parameter of a PA is harmonic distortion which is described in Chapter 2. Second harmonic distortion, HD_{2nd}, of the PA designed and constructed for this work is measured and shown in Figure 5.39.

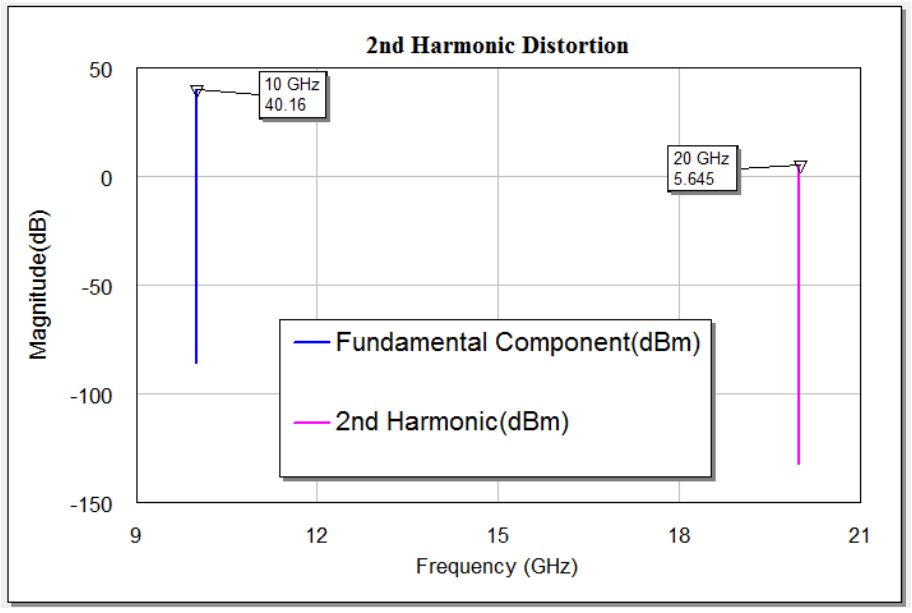


Figure 5.39 Second harmonic distortion measurement.

Since harmonic distortion is a ratio defined for harmonic components and fundamental component, the second harmonic distortion is expressed in dBc scale as follows:

$$HD_{2nd,dBc} = P_{out,2nd,dB} - P_{out,1st,dB} = 5.645 - 40.16 = -34.52\ dBc$$

5.8 GROUP DELAY MEASUREMENT

Group delay is an important parameter that indicates the propagation velocity difference of an electromagnetic wave inside a medium for each frequency component. Especially in systems having some kind of amplitude or phase modulation, group delay directly effects the system bit error rate performance. For a given instantaneous bandwidth, B, if the group delay is large, then each frequency component arriving at receiver channel will have significantly different phase angles so that during the demodulation of the signal, the message will not be reconstructed correctly.

Power amplifiers are usually the last system component before the antenna, so its contribution to the group delay of transmitter chain would eventually designates the transmitter's group delay characteristic. Since GaN material is a relatively new technology, it is important to observe group delay characteristic of power amplifiers that are fabricated using GaN semiconductor devices.

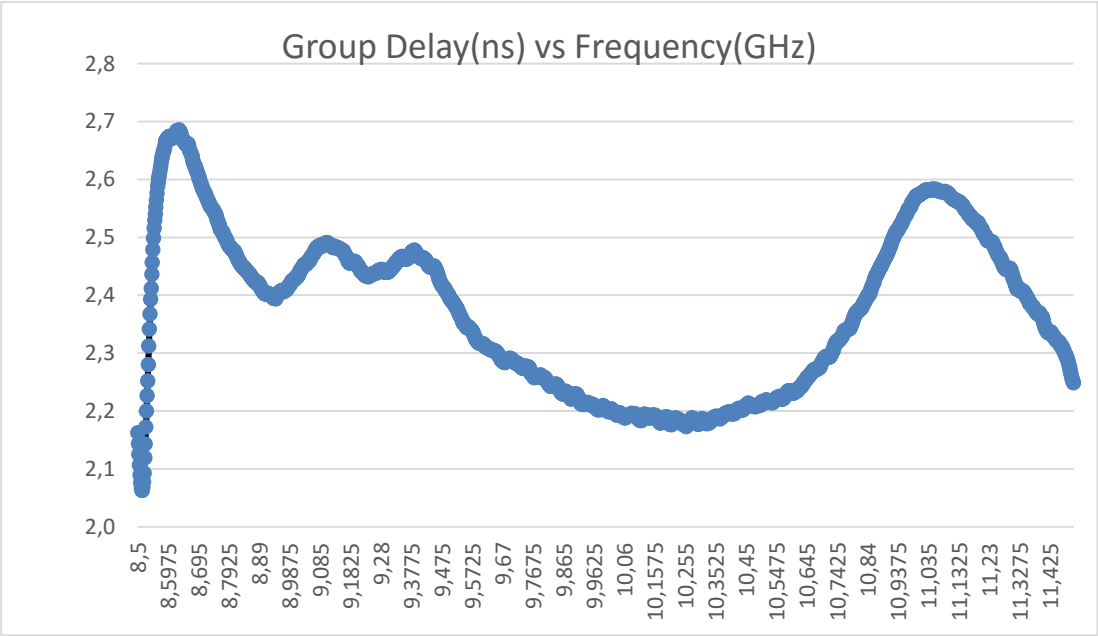


Figure 5.40 Group delay measurement of the constructed PA.

Figure 5.40 represents group delay measurement of the constructed PA. The measurement is taken for 8.5 GHz-11.5 GHz frequency band which is a little larger than the operation band (9 GHz-11 GHz) of the PA. It is seen that the maximum value of delay difference is observed as around 400 ps. However, group delay difference becomes larger out of the PA band since matching networks behave as bandpass filters whose propagation constant values degrade out of the band.

CHAPTER 6

CONCLUSION

Microwave power amplifiers are utilized in almost all high frequency wireless communication systems and have great impact on overall system performance. Since power amplifiers mostly operate in deeply nonlinear operation conditions, consume relatively large amount of system power budget, generate significantly large amount of heat they must be carefully designed and fabricated to have a reliable and cost effective system.

GaN as a semiconductor material having large energy band gap, high electron mobility and high thermal conductivity offers high power density devices, which are ideal candidates for development of high power microwave power amplifiers. The purpose of this thesis work is performance evaluation of a microwave power amplifier, designed and fabricated using GaN technology, for future wireless systems, including but not limited to radar, 5G, medical imaging and microwave heating, which are the typical high frequency applications that need high power amplifier devices

In Chapters 1 and 2, a comprehensive introduction on GaN material and descriptions of some behavioral and operational concepts related to power amplifiers are presented. The design process of the power amplifier is explained in Chapter 4 in great detail using the theoretical basis given in Chapter 3. Chapter 5 presents various measurement results, which illustrate that the fabricated PA works as expected. The measurements are done for both pulsed and CW operation modes to observe the performance deviation between two operation modes. It is seen that power amplifier provides better than 18 Watts of output power in CW mode and better than 20 Watts of output power in pulsed operation mode. In addition to output power measurements, AM/AM and

AM/PM behaviors are also measured to quantify the introduced nonlinearity by the power amplifier for both CW and pulsed modes. Moreover, frequency content of the output signal of the amplifier are also examined. Frequency response of two different pulsed operation methods are compared in terms of spectral efficiency. Pulse-to-pulse and in-pulse phase variation are two parameters that affect the performance of the systems operating in pulsed modes. Those two parameters are also measured for the constructed power amplifier to better define its behavior in pulsed systems. Furthermore, group delay measurement is also done utilizing the fabricated PA for the evaluation of usage in systems that use amplitude and phase modulation techniques.

As a conclusion, for the systems that require high RF output power, GaN technology is ideal the candidate for the future systems. However, it should also be noted that while providing high power density devices, GaN materials do not provide significant efficiency improvement so that the generated heat by the PA is remarkably increased. Therefore, reliability problems might occur if thermal management is not proper. Furthermore, the fabricated PA does not have a strongly linear operation region as it is observed in AM/AM measurements so that GaN based power amplifiers are not proper for the use in the systems which are expected to operate linearly. In pulse-phase stability measurements it is observed that pulse-to-pulse and in-pulse phase variations are ignorable which is another advantage of GaN material for pulsed systems.

Since GaN technology and GaN based microwave power amplifiers are still in development stages, there are variety of topics that must be studied in future. Firstly, since the RF output power level is high, the dissipated power on the GaN PA will also be high. Therefore, efficiency enhancement techniques such as multi-harmonic matching networks, envelope tracking, Doherty technique should be applied using GaN semiconductor devices. Moreover, those techniques to improve the efficiency of the amplifier should be tried to be developed for wideband applications. Secondly, the AM/AM distortion issue of the GaN devices must be handled with using power amplifier linearization techniques to make GaN transistors usable for linearity required applications. Furthermore, thermal management of the high power amplifiers is

another topic that must be studied extensively to improve the both device and system reliability.

GaN technology can be evaluated for millimeter wave applications such as 5G phased array systems, automative radars and imaging systems. Especially for high volume applications such as phased arrays, system on a chip (SoC) solutions that can be developed utilizing GaN material. For instance, MMICs having a PA, high power switch, high input power survivable low noise amplifiers on a single chip might be a good solution for future phased array systems.

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