DESIGN AND REALIZATION OF A 0.5-5 GHZ CASCADED FEEDBACK AMPLIFIER

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ABSTRACT

DESIGN AND REALIZATION OF A 0.5-5 GHZ CASCADED FEEDBACK AMPLIFIER

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Wideband amplification is one of the most examined study areas in microwave engineering. In this thesis work, 2-stage amplifier operating in decade bandwidth of 0.5-5 GHz is designed, simulated and demonstrated using two different discrete transistors. Designed amplifier is based on cascaded feedback amplifier concept. In order to flatten the gain of the designed amplifier, feedback topology is applied to both stages. Primarily, first stage is designed and demonstrated with flat gain of 7.8±1.2 dB and minimum return loss of 8.2 dB. After the second stage is designed, cascaded structure is formed and fabricated. Designed cascaded feedback amplifier has a flat gain of 17.1±1.8 dB and minimum return loss of 8 dB. Also, converting the schematic design of the amplifier into EM analysis in order to make a realistic simulation is explained in details in this thesis study.

Keywords: Broadband amplifier, cascaded amplifier, feedback amplifier

ÖZ

0.5-5 GHZ ARDIŞIK BAĞLI GERİBESLEMELİ YÜKSELTEÇ TASARIMI VE GERÇEKLENMESİ

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Geniş bantlı yükseltme, mikrodalga mühendisliğinde en çok çalışılan alanlardan biridir. Bu tez çalışmasında, farklı ve ayrık iki transistor kullanılarak 0.5-5 GHz frekans bandında çalışan 2 katlı bir yükselteç tasarlanmış, benzetimi yapılmış ve gerçeklenmiştir. Tasarımı yapılan yükselteç, ardışık bağlı geribeslemeli yükselteç mimarisine dayanmaktadır. Tasarlanan yükseltecin kazancını düzleştirebilmek için iki kata da geri-besleme uygulanmıştır. Öncelikle ilk katın tasarımı yapılmış ve kazancı 7.8±1.2 dB, geri dönüş kaybı da minimum 8.2 dB olacak şekilde gerçeklenmiştir. İkinci kat da tasarlandıktan sonra ardışık yapı oluşturulmuş ve üretilmiştir. Gerçeklenen yükseltecin kazancı 17.1±1.8 dB ve minimum geri dönüş kaybı 8 dB'dir. Ayrıca, gerçekçi bir benzetim yapmak amacıyla şematik tasarımından devrenin elektromanyetik tasarımına geçiş ayrıntılı bir şekilde anlatılmıştır.

Anahtar kelimeler: Geniş bantlı yükselteç, seri bağlı yükselteç, geribeslemeli yükselteç

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LIST OF ABBREVATIONS

RF: Radio Frequency

DC: Direct Current

TWT: Travelling-Wave Tube

PAE: Power added efficiency

SiGe: Silicon-Germanium

BJT: Bipolar Junction Transistor

GaAs: Gallium-Arsenide

FET: Field-Effect Transistor

TWDA: Travelling-Wave Distributed Amplifier

EM: Electromagnetic

VSWR: Voltage Standing Wave Ratio

E-HEMT: Enhancement Mode High Electron Mobility Transistor

P-HEMT: Pseudomorphic High Electron Mobility Transistor

PCB: Printed Circuit Board

SMD: Surface Mount Device

SMA: SubMiniature Version A

CHAPTER 1

INTRODUCTION

1.1. RF Amplification

Amplifier is an electronic circuit that amplifies the input signal by using DC energy and transfers the increased signal to the output. In a wireless communication system, RF signal propagates to receiving antenna through the medium, mostly air. During the propagation, the signal attenuates considerably. In order to make a successful communication, power of the received signal must be greater than the sensitivity of the receiver. To achieve this, it is common to place a power amplifier at the output stage of the transmitter. Similarly, receiver systems get weak signals. To process these weak signals, there are amplifiers at the input stage of receiver architectures. So, amplification is one of the key stages of microwave systems.

Microwave amplifiers were based on tube structure such as travelling wave tubes (TWT) and klystrons in early years with very limited applications. Since 1970, solid state technology made a huge progress, so most RF amplifiers are made of solid-state devices such as SiGe BJTs, GaAs FETs etc. [1] Solid-state microwave amplifiers are low cost and high-performance products that may be realized easily.

During the substantial developments in technology, specifications of amplifiers became more challenging. For this reason, amplifiers are one of the main research areas for designers in order to satisfy the requirements. Necessities for today's microwave systems differ from case to case. Some systems require wideband

operation while some need noise figure to be as low as possible, and some others are used for high power applications. So, researchers are trying to improve the amplifier structures in order to get the required specifications such as bandwidth, linearity, efficiency, size etc. Numerous circuit techniques and topologies were developed in order to increase the performance of the amplifiers for specific applications.

Broadening the bandwidth of the amplifier is one of the vital goals of amplifier topologies. The most common circuit methods for implementing wideband amplification are [2]:

a. Reactively matched circuit
b. Balanced circuit
c. Travelling wave distributed circuit
d. Feedback circuit

Each technique has its own advantages and disadvantages. Feedback amplifier configuration is one of the structures that increase the bandwidth of amplifier and has outstanding stability performance. Feedback topology is also a cost-effective way to achieve a flat gain over increased bandwidth.

1.2. Feedback Amplifiers

The main principle in feedback amplifier is to combine a portion of the output signal of the amplifier with the input signal by simply forming a feedback line from output to input of the amplifier. Basically, all electronic components with power gain (vacuum tubes, transistors) are considered as nonlinear devices. Using feedback structure, some trade-offs between gain and bandwidth are examined in these nonlinear devices.

Design of an amplifier for a narrow bandwidth may be straightforward according to the desired requirements. For example, designing the input and output matching networks with reactive components are easy for narrow bandwidth. However, as

the desired bandwidth increases, reactive matching networks may fail to satisfy the input and output return loss requirements over the desired bandwidth. Also, compensation of the gain using reactive matching networks gets more difficult. So, negative feedback techniques are used to overcome these problems.

Feedback amplifiers have many significant advantages. They may have satisfactory input and output return losses over the desired bandwidth. Also, stability is improved by applying feedback topology. Moreover, it is a low-cost application compared to other broadband amplifier topologies.

However, gain of the amplifier is reduced by applying feedback topology. Also, its output power is decreased and noise figure is increased due to the used components at the feedback line.

1.3. Outline of the thesis

This thesis is planned as follows: In Chapter 2, wideband amplification structures are given briefly. Advantages and disadvantages of broadband amplifier topologies are discussed, and theoretical formulations are given for some broadband amplifier topologies. Also, feedback topology is mentioned briefly, which is the starting point of this work.

In Chapter 3, theoretical formulations about feedback topology and design process of proposed cascaded feedback amplifier is explained in detail. Schematic and EM simulation phases are given and results are discussed. Fabrication process, measurements and comparisons are also given in this chapter.

Finally, conclusion and possible future studies are given in Chapter 4.

CHAPTER 2

WIDEBAND AMPLIFIERS

An ideal microwave amplifier should have a flat gain and satisfy input and output matching over the desired bandwidth [1]. Maximum power transfer is achieved by a conjugate matching network, but it can typically be done over a narrow bandwidth. While the bandwidth of the amplifier is increased by applying some methods, gain and return loss of the amplifier are expected to decrease.

In this chapter, some of the broadband amplifier topologies are discussed briefly. Theoretical expressions are given and feedback concept is introduced.

2.1. Motivation for Wideband Amplification

Amplifier is one of the most critical active circuitry in microwave systems. As the qualifications for wireless systems get more challenging, their sub-systems, especially amplifiers are required to satisfy more stringent specifications.

Virdee states that narrow bandwidth is demanded by systems such as communication receivers, and moderate bandwidth is required by commercial radar receivers. But he adds that electronic warfare and optical communication systems need wide bandwidths for unknown emitter frequency and high data-rate [2]. With the massive development of electronic warfare, optical communication and instrumentation systems, wideband systems are preferred by designers. So, broadband amplification techniques came into prominence.

Extra careful consideration and new difficulties are introduced by wideband amplifiers [8]. These difficulties may be sorted as:

a. Generally, $|S_{21}|$ of an active device reduces by 6 dB/octave and $|S_{12}|$ increases with the frequency with the same ratio, as it is seen in Figure 1 [12].
b. S_{11} and S_{22} parameters also vary significantly with frequency, their frequency variations are critical for designing matching circuits.
c. Noise figure and VSWR parameters are likely to get poorer as the frequency and operational bandwidth increase. In case of a wideband design, all these parameters should be considered at the same time and some trade-offs are inevitable.

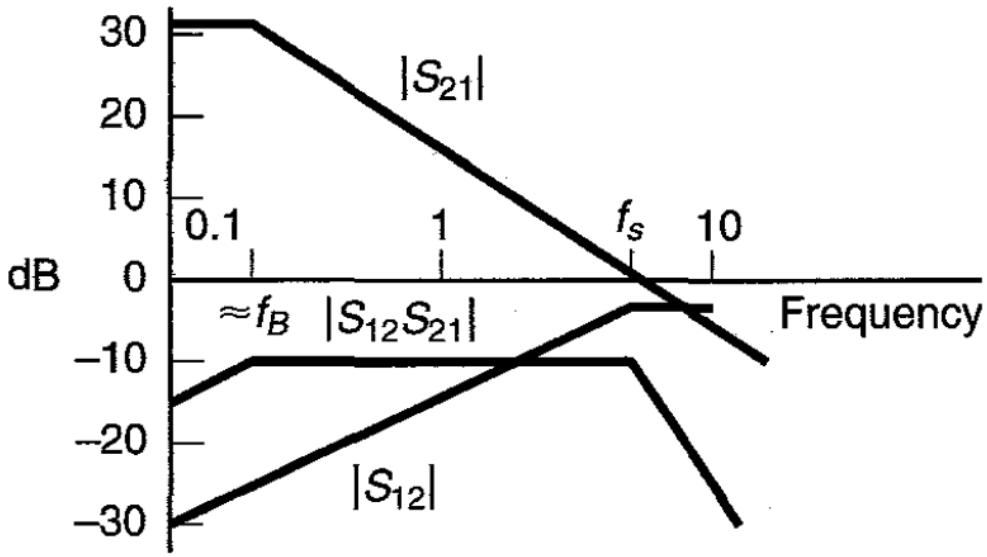

Figure 1 Frequency behavior of $|S_{21}|$, $|S_{12}|$ and $|S_{12}.S_{21}|$

2.2. Wideband Design Techniques

Motivation for wideband amplifier design and its difficulties are given in the previous section. In order to solve these problems, designers came up with different wideband design techniques, most popular of which may be listed as:

a. Reactively matched circuit
b. Balanced circuit
c. Travelling wave distributed circuit
d. Negative feedback circuit

Each circuit technique has advantages and disadvantages over each other. One must choose the design topology considering the system requirements and specifications.

These techniques are discussed in the following sections.

2.2.1. Reactively Matched Circuit

Reactively matched circuit which is illustrated in the Figure 2, also known as lossless matched topology, takes its name from the reactive components that compose the input and output matching networks of the amplifier [2]. It is known that the gain of the transistors is higher at the lower frequencies. As the frequency increases, gain is decreased. Reactive components at the input and output matching network produce reflections at the lower frequency, so that the gain is tried to be compensated and flattened.

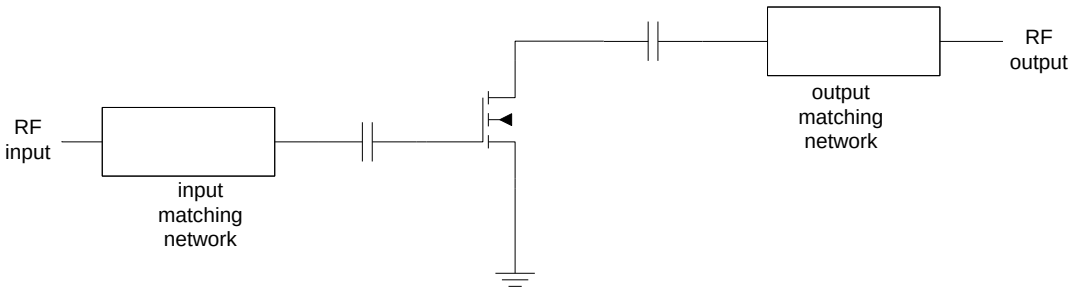

Figure 2 Reactively Matched Circuit

Input matching network design plays an important role for the minimum noise figure and maximum gain, while output matching network provides the power added efficiency (PAE) and maximum output power.

First reactively matched power amplifier was designed by Tserng, et al. [9] , which was a 2-18 GHz amplifier with the PAE of 8-15% and 200 mW output power.

Matching the amplifier for a small bandwidth is not a difficult task for designers. As the bandwidth increases, matching gets harder and some reductions in performance becomes inevitable.

2.2.2. Balanced Circuit

Balanced topology is a good preferable solution for input/output VSWR and gain flatness problems in broadband amplification. In Figure 3, balanced topology is illustrated with 3-dB hybrid couplers at input and output of the circuit.

It was mentioned that reactively matched topology may have some return loss problems at some part of the frequency spectrum, because of its gain-flattening technique. But in the balanced structure, this problem is eliminated perfectly by using hybrid couplers, which would cancel out the reflected signal naturally.

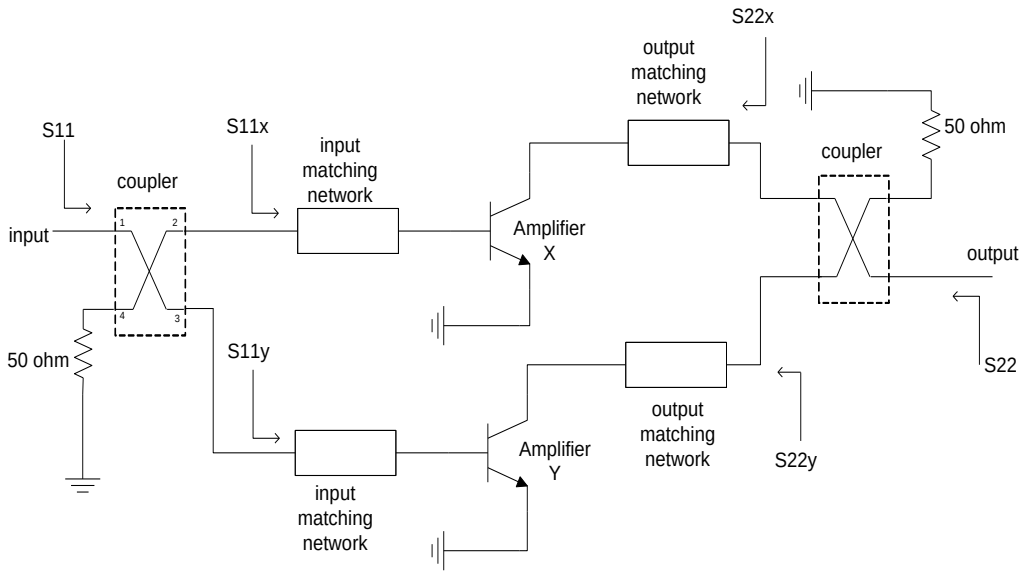

Figure 3 Balanced Amplifier Topology

For hybrid coupler block, it is common to use the 3-dB Lange coupler and 3-dB branch-line coupler. Also, it is possible to use 2-way Wilkinson power divider and a quarter wave line added at the end of one of its branches. The S-parameter matrix of the coupler is given as [13];

$$[S] = \begin{bmatrix} 0 & \frac{e^{\frac{-j\pi}{2}}}{\sqrt{2}} & \frac{e^{-j\pi}}{\sqrt{2}} & 0 \\ \frac{e^{\frac{-j\pi}{2}}}{\sqrt{2}} & 0 & 0 & \frac{e^{-j\pi}}{\sqrt{2}} \\ \frac{e^{-j\pi}}{\sqrt{2}} & 0 & 0 & \frac{e^{\frac{-j\pi}{2}}}{\sqrt{2}} \\ 0 & \frac{e^{-j\pi}}{\sqrt{2}} & \frac{e^{\frac{-j\pi}{2}}}{\sqrt{2}} & 0 \end{bmatrix}$$

If the coupler is used as a divider-combiner by terminating the 4th port with the characteristic impedance, S matrix would become

$$[S] = \begin{bmatrix} 0 & \frac{e^{\frac{-j\pi}{2}}}{\sqrt{2}} & \frac{e^{-j\pi}}{\sqrt{2}} \\ \frac{e^{\frac{-j\pi}{2}}}{\sqrt{2}} & 0 & 0 \\ \frac{e^{-j\pi}}{\sqrt{2}} & 0 & 0 \end{bmatrix}$$

According to this, if an incident signal a_1 is applied to port 1 of hybrid coupler with $a_2 = a_3 = 0$, it is seen at the output ports that

$$b_2 = {a_1\, e^{\frac{-j\pi}{2}}}\Big/{\sqrt{2}} \quad \text{and} \quad b_3 = {a_1\, e^{-j\pi}}\Big/{\sqrt{2}}$$

It is seen clearly that there is a 90^0 phase difference between the branches. For combiner version, incident signals a_2 and a_3 that have the same magnitude but phase difference of 90^0 (i.e. $a_3 = a_2\, e^{j\pi/2}$) are applied to port 2 and 3, and the output at port 1 would be seen as

$$b_1 = \frac{e^{\frac{-j\pi}{2}}}{\sqrt{2}}\left(a_2 + a_3\, e^{-j\pi/2}\right) = \frac{e^{-j\pi}}{\sqrt{2}}(2a_2)$$

Therefore, if two amplifiers at the two branches of the topology in Figure 4 have the same input return loss, the reflected signals from the amplifiers would have the same magnitudes and phase difference of 90^0. When these two signals are combined at the hybrid coupler at the input, their phase difference becomes 180^0 and the two signals cancel each other. Consequently, perfect matching is achieved at the input of the hybrid coupler theoretically. The same calculations are also valid for the output return loss of the topology [13].

It is possible to mention the advantages of the balanced structure as

a. Output power is nearly 3 dB higher than one of the amplifiers itself, because two outputs are combined.
b. Even if the return loss of single amplifier is poor, huge enhancements are possible by the help of the hybrid couplers. So, it is easier to design broadband amplifier with less consideration of VSWR.
c. They are simply cascadable due to the isolation effect of hybrid device.

Disadvantages of balanced topology may be stated as

a. Bandwidth of the whole circuit is limited by the bandwidth of the hybrid coupler. Bandwidth is said to be about 50% of the center frequency practically. For larger bandwidths, multisection Wilkinson topologies should be considered [14].
b. Due to the two active device usage, the total circuit consumes more DC power and has larger size.

2.2.3. Travelling Wave Distributed Circuit

Distributed amplifier concept dates back to the 1940s with the usage in wideband vacuum tube amplifiers [1]. Ultra wide bandwidths are seen to be possible with

this structure. Capacitance and transconductance of conventional electronic valve are studied out by W.S Percival to determine the bandwidth of the amplifier [3]. He separated the input and output capacitance of the valve from their transconductance and absorbed them into artificial transmission lines [2]. So, bandwidth is limited by the cut-off frequency of the artificial lines. Later on, Ginzton [4] and Horton [5] studied this topology and demonstrated the distributed amplifier. Then, Moazzam and Aithison introduced a dual-fed single stage distributed amplifier in which the input and output ports have reactive terminations [6]. This structure improves the gain and efficiency over conventional TWDA. Analyses and simulation results of Moazzam and Aithison state that cascaded single stage distributed amplifier topology may have a flat response with 9.5 dB gain up to 5 GHz, nearly the same gain of four stage conventional TWDA. Liang and Aithison then developed the topology into cascade of n single-stage distributed amplifier, by simply excluding idle drain and gate termination except from first and last stages [7]. Flat gain of 20 dB is achieved by their simulation results with this topology.

In Figure 4, conventional travelling wave distributed amplifier circuit is shown.

In conventional TWDA, input signal propagates forward through the gate line. As each transistor receives some part of the signal and amplifies by its transconductance, they deliver the amplified signal to the drain line. While the amplified signals travel through the drain line in forward direction, they add up and amplitude of the total output signal becomes higher. Performance of the TWDA structure is highly dependent on this in-phase adding.

During the propagation through the drain line, some imperfections give rise to reflections. In order these reflected signals not to corrupt the travelling output wave, a termination resistance (R_d) is placed at the other end of the drain line.

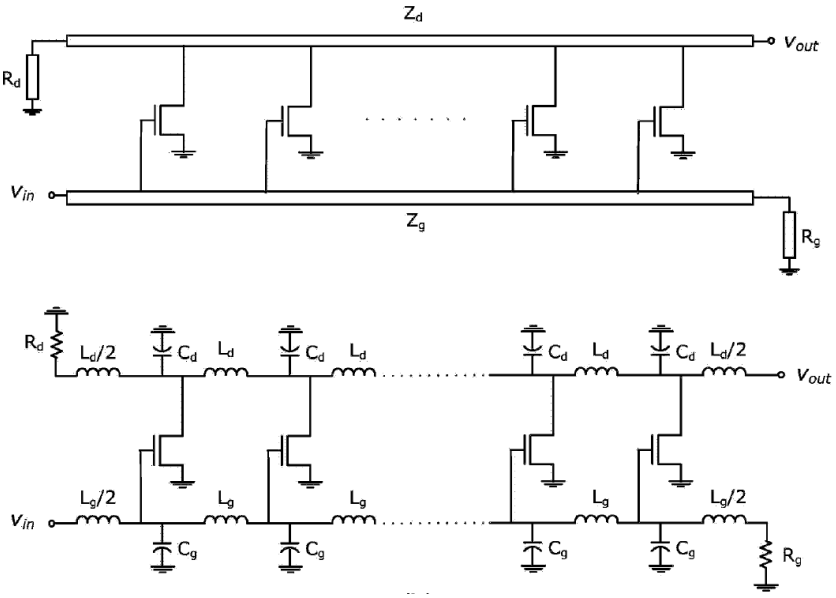

Figure 4 Conventional TWDA Configuration

Because input and output transmission lines eliminate the capacitance of the FETs, bandwidth of the amplifier is mostly determined by these artificial transmission lines. If the characteristic impedance of the lines does not change considerably as the frequency is changed, the amplifier still operates and this determines the bandwidth of the amplifier.

Virdee calculates the gain of conventional TWDA structure by using the generic amplifier model which is shown in Figure 5 [2]. In this calculation, basically, the FET is taken as lossless and other elements such as package parasitics are omitted for a simple calculation. Gate and drain transmission lines are formed as lumped elements (L_d and L_g) as seen in Figure 5. Load and source terminations are 50Ω.

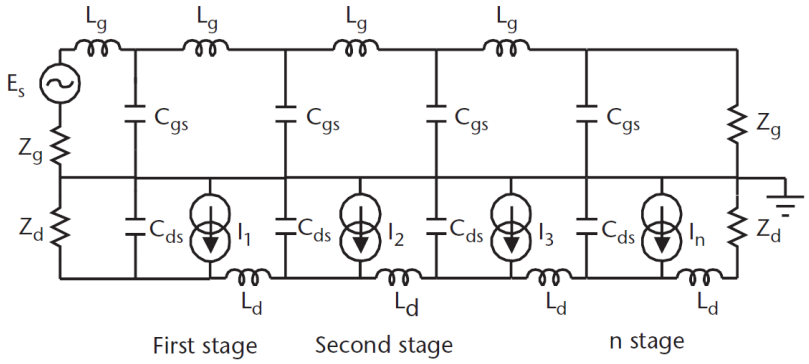

Figure 5 n-section TWDA (equivalent model)

If FET current generators have magnitudes of I_1, I_2, .. I_n, total current in the load is found by superposition of the drain line currents as [2]:

$$I_d = \frac{1}{2}\left\{I_1\, e^{-jn\beta_d} + I_2\, e^{-j(n-1)\beta_d} \ldots I_n\, e^{-j\beta_d}\right\}$$

E_s generates voltages of V_1, V_2,… V_n across each gate capacitors. So, if V_{in} is the voltage across the input terminal of the amplifier, we get

$$V_1 = V_{in}\ e^{-j\beta_g}$$

$$V_2 = V_{in}\, e^{-2j\beta_g}$$

$$V_n = V_{in}\, e^{-jn\beta_g}$$

We know that;

$$I_1 = g_m\, V_1\ ,\ \ I_2 = g_m\, V_2\ ,\ldots,\ I_n = g_m\, V_n$$

Also, the following expression becomes true because of the lossless consideration of FETS;

$$|V_1| = |V_2| = |V_n| = |V_{in}| \text{ and } |I_1| = |I_2| = |I_n| = |I_{in}|$$

So,

$$I_d = \frac{1}{2}\, V_{in}\, g_m \left\{e^{-j(n\beta_d+\beta_g)} + e^{-j((n-1)\beta_d+2\beta_g)} \ldots\ e^{-j(\Delta\beta_d+n\beta_g)}\right\}$$

Above equation may also be written as;

$$I_d = \frac{1}{2}\, V_{in}\, g_m \left\{\frac{1 - e^{-j+1n(\beta_d+\beta_g)}}{1 - e^{-j\Delta(\beta_d-\beta_g)}}\right\} e^{-j((n+1)\beta_d+\beta_g)}$$

For a matched line, V_{in} can be expressed as $E_s/2$. So;

$$|I_d| = \frac{1}{4}\, E_s\, g_m \left|\frac{\sin\frac{n}{2}(\beta_d - \beta_g)}{\sin\frac{1}{2}(\beta_d - \beta_g)}\right|$$

Therefore, forward gain may be expressed as; [2]

$$G = \frac{{E_s}^2}{4Z_d} = \frac{{g_m}^2 Z_d Z_g}{4} \left(\frac{\sin \frac{n}{2}(\beta_d - \beta_g)}{\sin \frac{1}{2}(\beta_d - \beta_g)} \right)^2$$

The expression inside the sine function can reduce to n^2 in the limiting situation of $\beta_g \rightarrow \beta_d$. So, forward gain expression can be reduced to;

$$G = \frac{1}{4} n^2 {g_m}^2 Z_d Z_g$$

It is clearly seen that the gain expression of TWDA topology is not a function of frequency up to the cut-off frequency of the artificial lines. This equation of ideal case tells us that the increment of the number of the stages "n" would not limit the gain of the amplifier, but in practice the real expression is different. If the artificial line losses are taken into consideration, the gain expression becomes [10];

$$G = \frac{1}{4} {g_m}^2 Z_d Z_g \left(\frac{e^{-A_g n} - e^{-A_d n}}{A_g - A_d} \right)^2$$

where A_g and A_d are the gate and drain line attenuations, respectively.

The optimum number of the stages in maximum available gain equation is calculated with finding the maxima point of the gain formula by differentiating and equating it to zero as [11];

$$N = \frac{\ln \frac{A_d}{A_g}}{A_d - A_g}$$

The relation between the number of stages and the gain of the conventional TWDA structure is seen in Figure 6 [2].

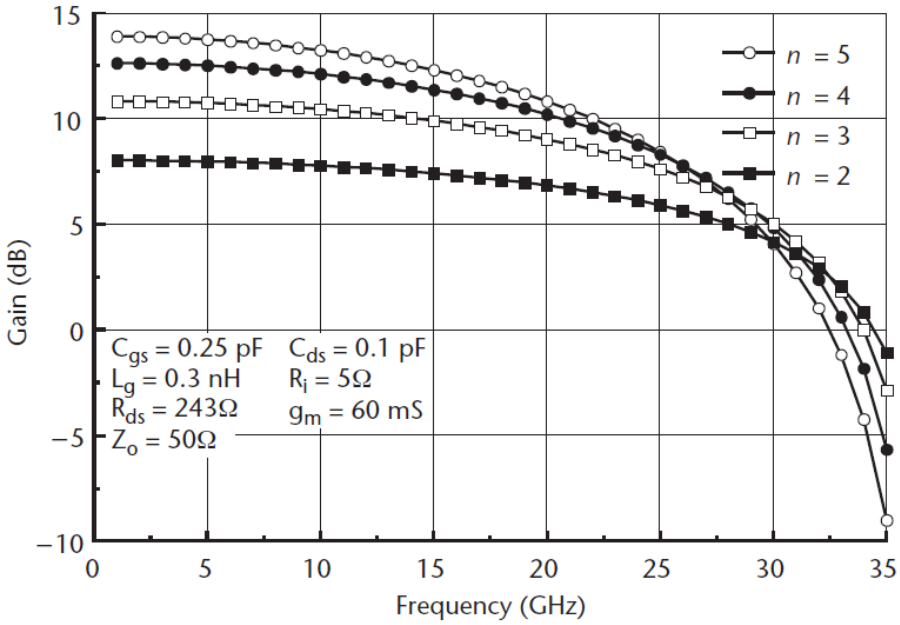

Figure 6 TWDA Gain vs. Number of Stages

As it is shown in Figure 6, gain increment does not change much as the number of stages is more than 5. This is because the gate line attenuation is too high after the 4^{th} and 5^{th} stage. So, there is a tiny signal for the transistors after the 4^{th} and 5^{th} ones to amplify. Another reason is that keeping the phases coherent becomes more difficult as the number of stages grows, and out-of-phase signals do not contribute to the output signal.

Advantages of travelling wave distributed amplifier may be listed as:

a. Satisfactory input and output return losses.
b. Wide bandwidths may be achieved.
c. Good reverse isolation and stability.

Disadvantages of travelling wave distributed amplifier are:

a. Phase coherency is the biggest problem.
b. Each active device receives less input power than the previous one because of gate line attenuation.

c. Gain is limited because of gate line attenuation and practical difficulties of phase equalization. Also, as the number of stages increases, total size of the circuit increases, too.
d. Failure in one stage would affect the total response drastically.

2.2.4. Feedback Circuit

Basic schematic of an amplifier with feedback structure is shown in Figure 7 [8]. In this topology, feedback is generated by a RLC circuit. Capacitor is used for DC blocking, inductor and resistor are used for adjusting the gain level and bandwidth.

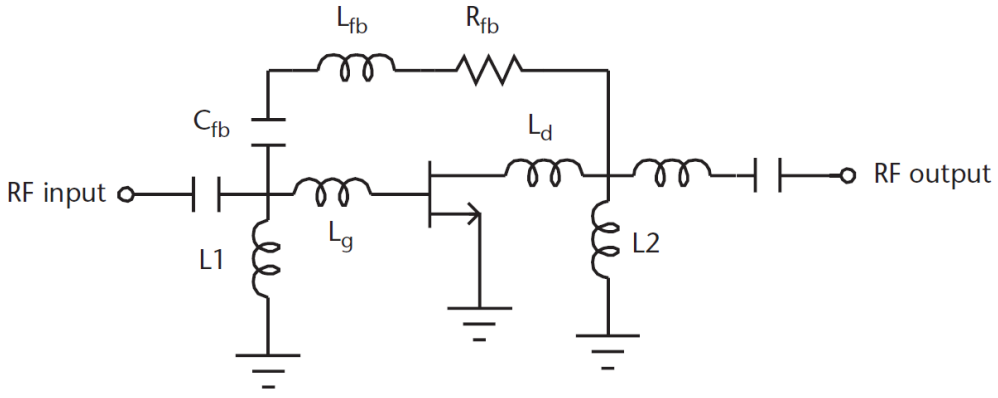

Figure 7 Amplifier with Feedback

It was mentioned that the amplifier gain is decreased as the operating frequency increases, which means gain is generally higher in the lower part of the operation frequency of the amplifier. In order to make some improvements in the gain flatness, gain at the lower frequency needs to be decreased while keeping the high frequency response unchanged. This is the main purpose of the inductive components at the feedback path. Since impedance of inductors is directly proportional to the frequency, it has higher impedance value at high frequencies and vice versa. Therefore, at lower frequencies, some part of the output signal is delivered to the input by feedback path, interferes and decreases the gain. At higher frequencies, since the impedance of feedback path is high, output signal

cannot be delivered to input considerably, which is the main goal of feedback topology.

Advantages of feedback amplifiers are listed as;

a. Since the gain is reduced, operation bandwidth is increased by the same ratio considering the gain-bandwidth product remains the same.
b. It is a cheap solution for achieving flat gain response.
c. Stability of the amplifier increases remarkably.

Drawbacks of this topology are;

a. Higher noise figure because of the resistive elements in the feedback path.
b. Output power is decreased.

CHAPTER 3

THEORY AND DESIGN OF CASCADED FEEDBACK AMPLIFIER

Flat gain and satisfactory input and output return loss are parameters that are becoming harder to realize as the bandwidth increases, as mentioned in previous chapter. In order to overcome these problems, feedback amplifier concept is developed by Black [8]. Feedback topology is preferable for its good return loss, flat gain and increased stability over a wide bandwidth.

In this chapter, theory of feedback amplifiers is explained in details. Simulation phase for designed amplifiers are given step by step, and measurement results are shown. Differences between simulation and measurement results are explained. In order to make realistic simulations, electromagnetic analysis of the circuit is also shown in details.

3.1. Theory of Feedback Amplifiers

A basic schematic for feedback amplifier was given in Figure 7 [8]. In this schematic, L_{fb}, C_{fb} and R_{fb} components form the feedback line. In this schematic, the inductor in the drain (L_d), the inductor in the gate (L_g) and the inductor in the feedback line (L_{fb}) may be tuned to increase bandwidth of the amplifier [9]. As the frequency increases, impedance of the inductor in the feedback line (L_{fb}) increases and effect of the feedback decreases. The capacitor in the feedback line (C_{fb}) operates as a DC block between gate and drain lines. Also, C_{fb} controls the

bandwidth of the amplifier with L_{fb} while the resistor in the feedback line (R_{fb}) adjusts the gain.

General topologies of feedback structure are shown in Figure 8 [8].

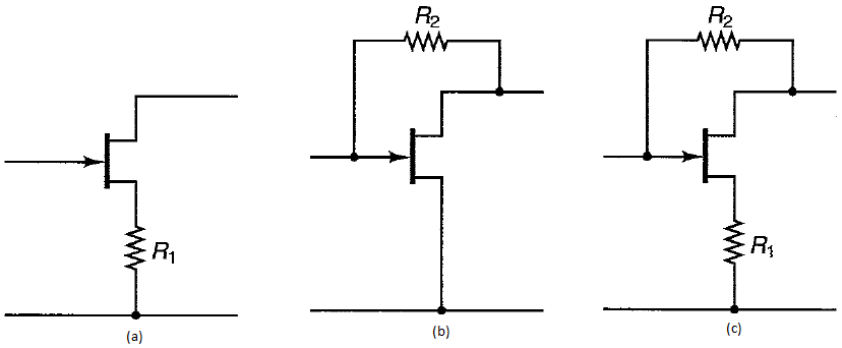

Figure 8 (a) FET with series feedback (b) FET with shunt feedback (c) FET with series-shunt feedback

If the equivalent circuit of FET is considered and parasitic elements are neglected, the equivalent circuit of Figure 8 may be expressed as in the Figure 9 [8].

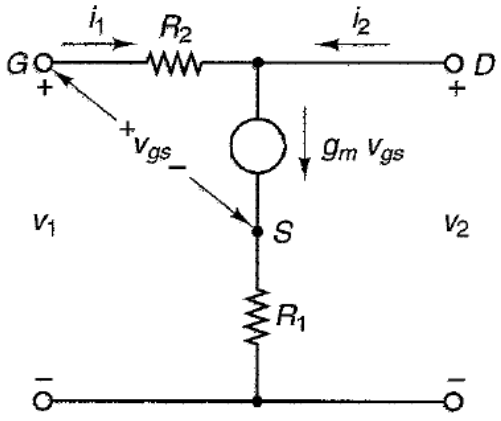

Figure 9 Series-shunt feedback with equivalent model of FET

According to this circuit, the admittance matrix of this structure becomes:

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} \dfrac{1}{R_2} & -\dfrac{1}{R_2} \\ \dfrac{g_m}{1+g_m R_1} - \dfrac{1}{R_1} & \dfrac{1}{R_2} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}$$

These Y-parameters can be easily converted into S-parameters by simply applying conversion identities [13], so we get:

$$S_{11} = S_{22} = \frac{1}{D}\left(1 - \frac{g_m Z_0^2}{R_2(1 + g_m R_1)}\right)$$

$$S_{21} = \frac{1}{D}\left(\frac{-2g_m Z_0}{1 + g_m R_1} + \frac{2Z_0}{R_2}\right)$$

$$S_{12} = \frac{2Z_0}{DR_2}$$

where

$$D = 1 + \frac{2Z_0}{R_2} + 1 - \frac{g_m Z_0^2}{R_2(1 + g_m R_1)}$$

If perfect input and output matching is considered ($S_{11} = S_{22} = 0$), then

$$1 + g_m R_1 = \frac{g_m Z_0^2}{R_2}$$

Above equation can be also expressed as

$$R_1 = \frac{Z_0^2}{R_2} - \frac{1}{g_m}$$

So that, S_{21} and S_{12}can also be expressed as

$$S_{21} = \frac{Z_0 - R_2}{Z_0}$$

$$S_{12} = \frac{Z_0}{Z_0 + R_2}$$

Above equations proves that S_{21} is a function of characteristic impedance and shunt feedback resistor in the feedback line. Hence, gain of the amplifier may be adjusted by changing the R_2 resistor.

Also, shunt topology in Figure 8b can be examined by simply making $R_1 = 0$ at the above equations. Hence, we get

$$g_m = \frac{R_2}{Z_0^2}$$

Also, considering S_{21} is a negative number, equation of S_{21} above can be written as

$$R_2 = Z_0(1 + |S_{21}|)$$

If A_v is taken as the voltage gain of a basic shunt feedback topology as in Figure 10, then output voltage and input current can be written as

$$v_o = A_v v_1$$

$$i_1 = \frac{v_1 - v_o}{R_2}$$

So that,

$$R_{in} = \frac{v_1}{i_1} = \frac{R_2}{1 - A_v}$$

If R_{in} is considered as characteristic impedance of RF circuits (50 Ω), it is seen that above two equations of R_2 and R_{in} are same.

In the case of series-shunt feedback, if value of g_m is high enough, the following equation can be written

$$R_1 R_2 \approx Z_0^2$$

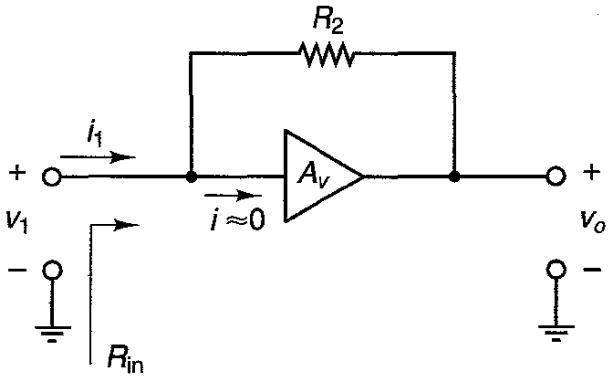

Figure 10 Shunt feedback

As all topologies, feedback topology has advantages and disadvantages. Advantages of feedback structure can be listed as;

a. Bandwidth of the amplifier is increased.
b. It is a cheap and easy solution for broadband amplification.
c. It has good matching and flat gain over a wide bandwidth.
d. It provides increased stability.

Disadvantages of the feedback structure can be sorted as;

a. Due to the resistive element in feedback line, noise figure is increased.
b. Gain and output power of the transistor is decreased in order to increase the bandwidth.
c. Extra care should be taken with the bias network. Especially for cascaded structures, it is a good idea for each stage to have its own bias network, which increases complexity.

3.2. Designing Cascaded Feedback Amplifier

Transistor choice is one of the most important points in the design of an amplifier. In this thesis, a 2-stage feedback amplifier is designed using NI AWR Design Environment. Since the gain of the transistors change with frequency massively, gain flattening is achieved by applying feedback to both transistors in the design.

Two transistors of Avago Technologies are used. Brief information about these transistors is given in the next sub-section. Then, schematic and EM Structure designs are explained in details.

3.2.1. ATF541M4

ATF541M4 is a low noise, small packaged and single supply enhancement-mode high electron mobility transistor (E-HEMT) with high linearity. Basic parameters of ATF541M4 are shown in Table 1 [16].

Table 1 Key parameters of ATF541M4

	Unit	Minimum	Typical	Maximum
Threshold Voltage	V	0.18	0. 36	0.52
Transconductance	mmho	230	398	560
Gain	dB	15.5	17.5	18.5
Noise Figure	dB	-	0.5	0.9
OIP3	dBm	29	31.5	-
P1dB	dBm	-	20	-

In order to make realistic simulations, S parameters files which are provided by Avago Technologies in "s2p" format should be used. S parameters file is not generated from the computational design. Vendors measure the S parameters of the product, apply mathematical de-embedment procedure and finally provide the data file to the customers. So, design with S parameters files is expected to give realistic S parameters simulation results.

The supplier gives the S parameters files for different drain voltages and drain current. Designer must use the S parameter file of relevant bias point. In this study, ATF541M4 is planned to be biased at 3V at drain and 0.6V at gate with 60 mA drain current. If the drain current of the demonstrated design would be different from the bias point of the used S parameter file, it can be adjusted by slowly changing the gate voltage.

3.2.2. ATF34143

ATF34143 is a high-dynamic range, low noise, pHEMT with small sized package. It is biased with -0.5V at gate and 4V at drain consuming about 60 mA. Basic parameters of ATF53143 are shown in Table 2. [17].

Table 2 Key parameters of ATF54143

	Unit	Minimum	Typical	Maximum
Threshold Voltage	V	-0.65	-0.5	-0.35
Transconductance	mmho	180	230	-
Gain	dB	16	18.5	19
Noise Figure	dB	-	0.5	0.8
OIP3	dBm	33	35.8	-
P1dB	dBm	-	21.4	-

Since the S parameters files are generated by measurements, some unwanted effects such as package parasitics are also included, which means that there is no reason to add the parasitic elements to the transistor.

3.2.3. Using the Conical Inductor

Choking inductor is a vital point in amplifier design. Especially in broadband applications, this element requires extra care for not being a resonant component between the operating frequencies. Ordinary inductors are not suitable for 0.5-5 GHz design, so a conical inductor of ATC (ATC506WLSM2R00) is used. Insertion loss and return loss graphs of this component are given in Figure 11 [18].

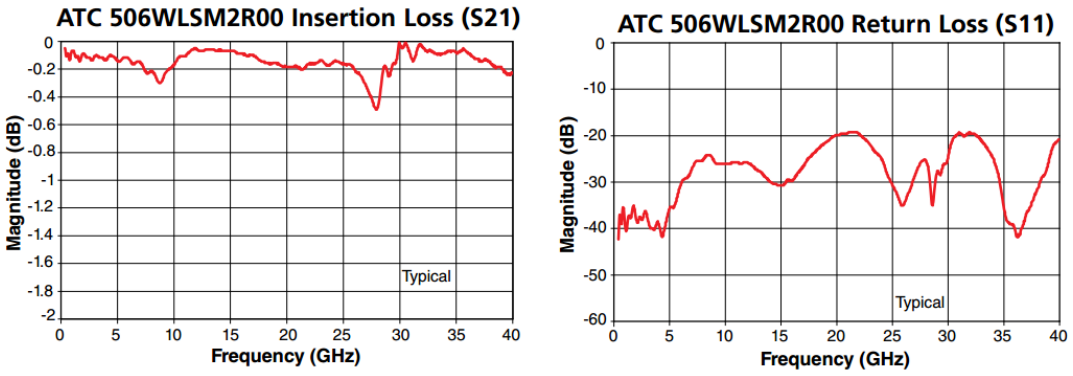

Figure 11 S_{21} and S_{11} of Conical Inductor

Since two transistors are used in the final design, their gate and drain voltages are set and connected individually in the schematic design tool of AWR. So, 4 conical inductors for are required for the two transistors used.

An important point for using conical inductors is their method of generating S parameter model. S parameter files of conical inductors are generated by using a shunt configuration, as seen in Figure 12 [19].

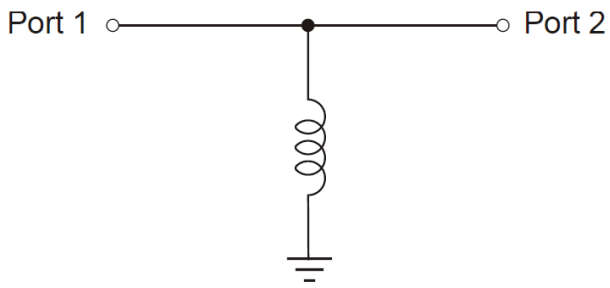

Figure 12 Shunt Configuration

Therefore, subcircuit of the conical inductors that are created by S parameters data file must be connected as a series element to the DC block capacitor during simulations as illustrated in Figure 13 since it is already measured in shunt configuration.

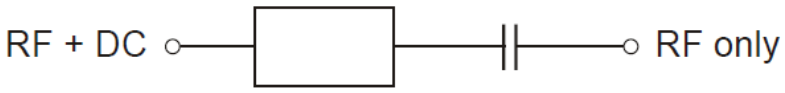

Figure 13 True connection of S parameter file of conical inductors

3.2.4. Schematic Design of the First Stage

Bias point and the DC current level are some of the most crucial and underrated step in an amplifier design. So, first phase for designing an amplifier is determining the proper biasing point of the transistors. Once it is determined, the relevant S parameters file is used. For ATF541M4 transistor, 3V drain voltage with 60 mA current is used.

S parameters file is imported to AWR schematic design tool as shown in Figure 14.

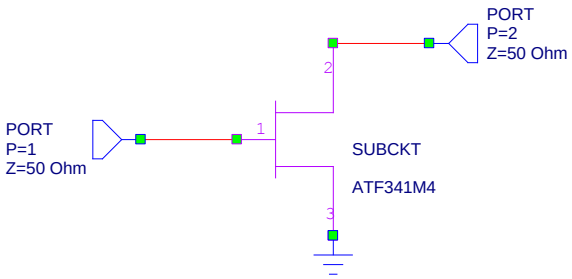

Figure 14 S Parameter Model of ATF541M4

S parameters simulation results are given in Figure 15.

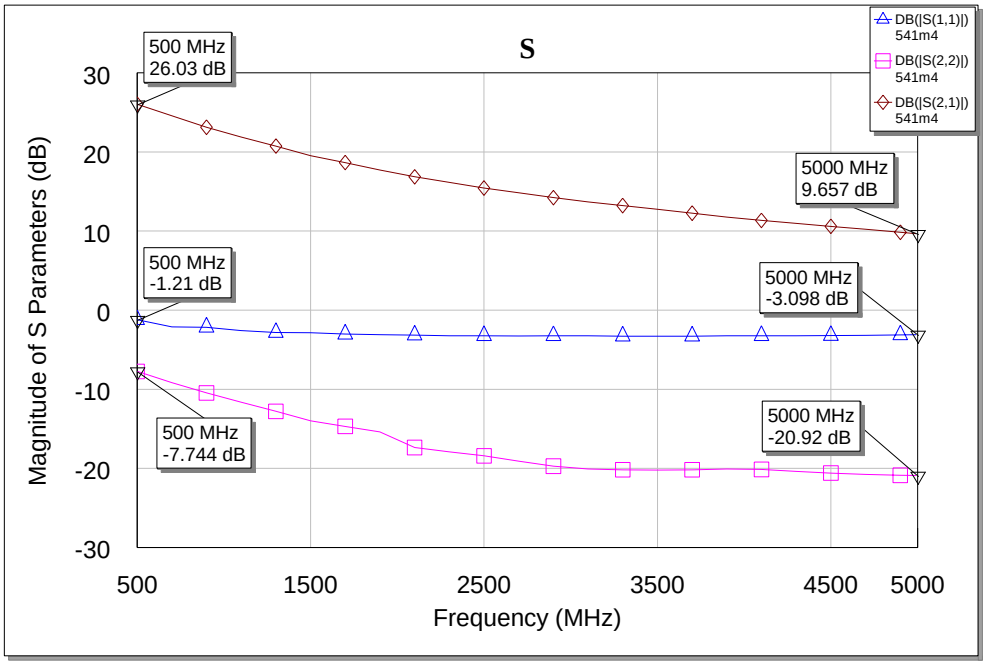

Figure 15 S parameter results of model

As it is clearly seen, gain is decreased from 26 dB to 9.6 dB as the frequency increases. Negative feedback circuitry takes the role of gain equalization at this point. For starting point, source and feedback resistors are selected as 10 Ω and 250 Ω respectively, as shown in Figure 16.

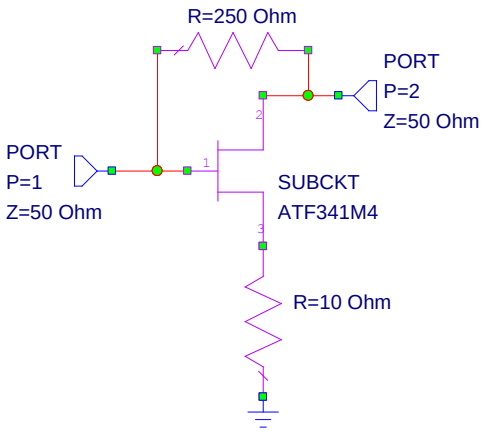

Figure 16 Feedback topology with initial values

S parameters simulation results of transistor with feedback are given in Figure 17.

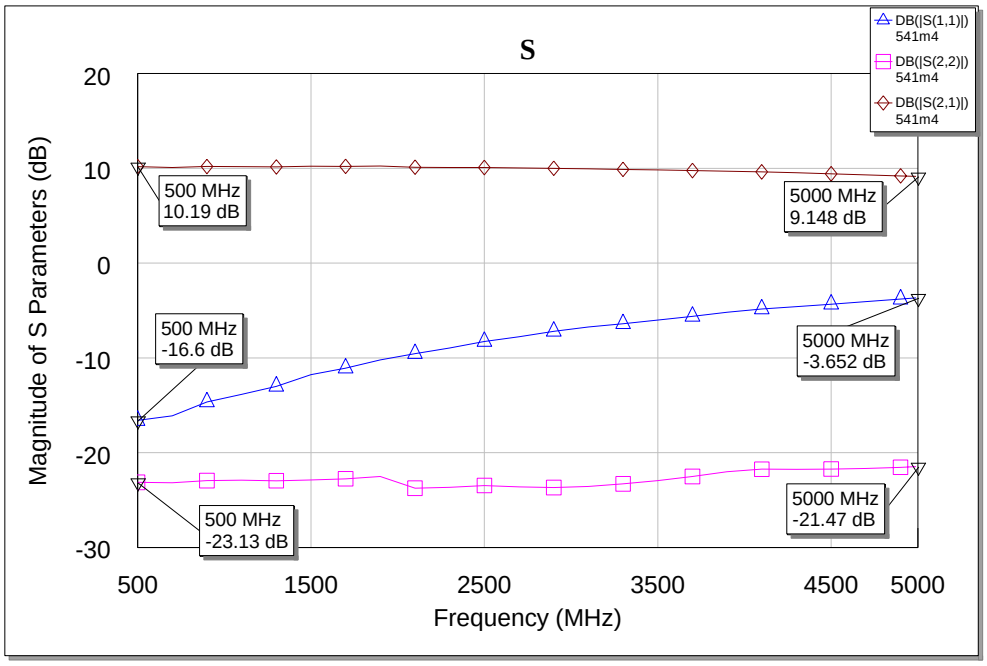

Figure 17 S parameter analysis of feedback topology

As it is seen, gain is equalized by feedback circuitry according to the previous results. Maximum and minimum values of S_{21} are nearly 10.19 dB and 9.148 dB respectively, which is considered to be flat as compared to the previous results.

So, next step is to match the impedance of the input and output ports to the characteristic impedance of the system. For initial steps of impedance matching, Smith Chart analysis is very useful. In Figure 18, S_{11} and S_{22} results of Figure 17 are given in the Smith Chart.

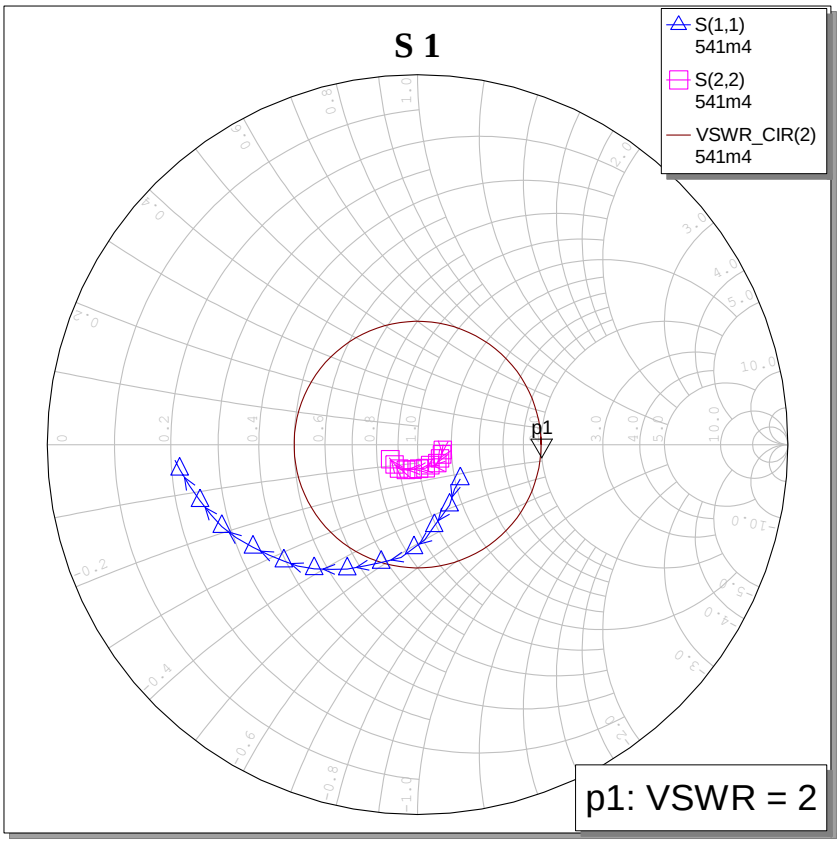

Figure 18 Smith Chart analysis of feedback topology

As it is seen both from Smith Chart and rectangular graph, output matching is quite satisfying. So, it is logical to start adding the matching network elements to the input side and to the feedback circuitry.

When the Smith Chart results are examined, it can be seen that inductive and resistive components in series would shrink the S_{11} through the center of the Smith Chart because S_{11} is at the bottom half of the chart. A resistor in series is added to the input of the circuit. Besides, some microstrip lines and junction elements

which are inductive elements are added for input and output of the transistor, as given in Figure 19. These T-junctions also act like transmission lines just like microstrip lines.

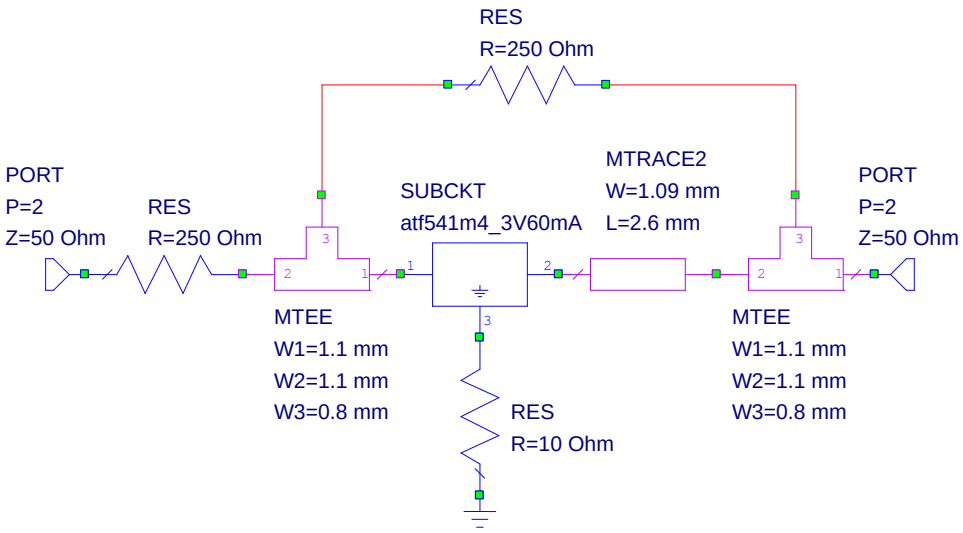

Figure 19 Microstrip lines, tees and lumped components

At first, initial values are assigned as the resistor values, line and junction lengths and widths. Then, the values are tuned by watching the Smith Chart. Results of the schematic in Figure 19 are given in Figure 20. As it is seen in the chart, inductive and resistive elements moved the input return loss to the center. Both S_{11} and S_{22} are inside the VSWR 2:1 circle, which is an acceptable level in an amplifier design.

A small inductor is added to the input of the transistor for matching. Also, transmission lines are added to the feedback path of the circuit, as it is seen in Figure 21. Besides there are two source pins of the transistor, but subcircuit file in the simulation has one source port. So, two parallel transmission lines are connected to the source pin of the subcircuit file for proper simulation. In the same manner, the feedback resistor at the source pin is doubled. Component values are tuned, as in the previous step.

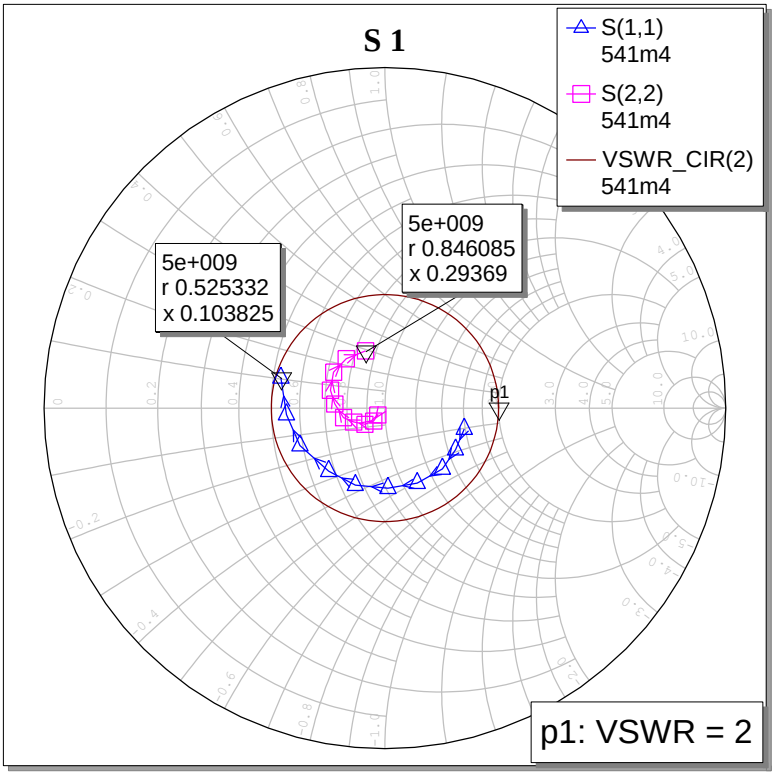

Figure 20 Smith Chart analysis

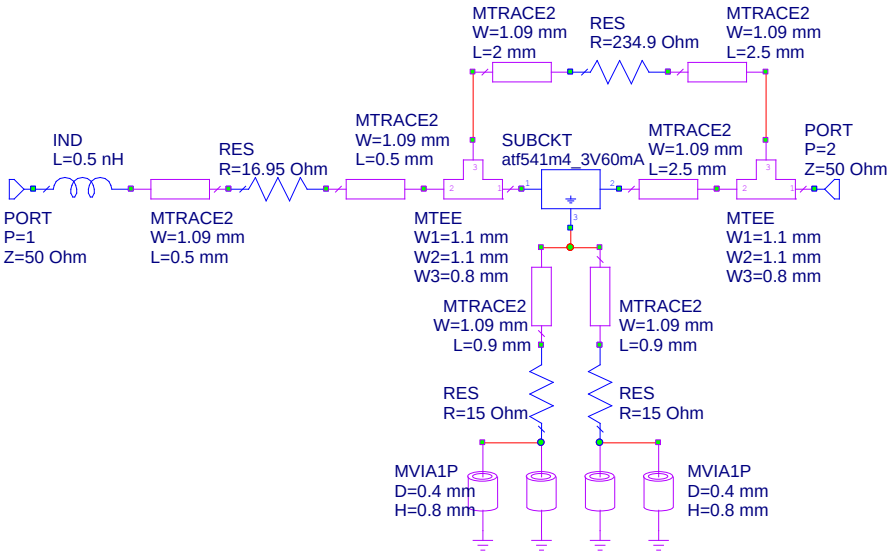

Figure 21 Schematic with input matching network

An important issue is that; a component could not be connected to ground without an inductive element. Here, ground connections are made through vias with a hole diameter of 0.4 mm and pad width of 0.8 mm. Ground connections without vias in simulations may misguide the designer and unpleasant surprises may occur in the real world demonstration. So, design using vias would be more realistic.

Smith Chart analysis of the schematic in Figure 20 is given in Figure 21.

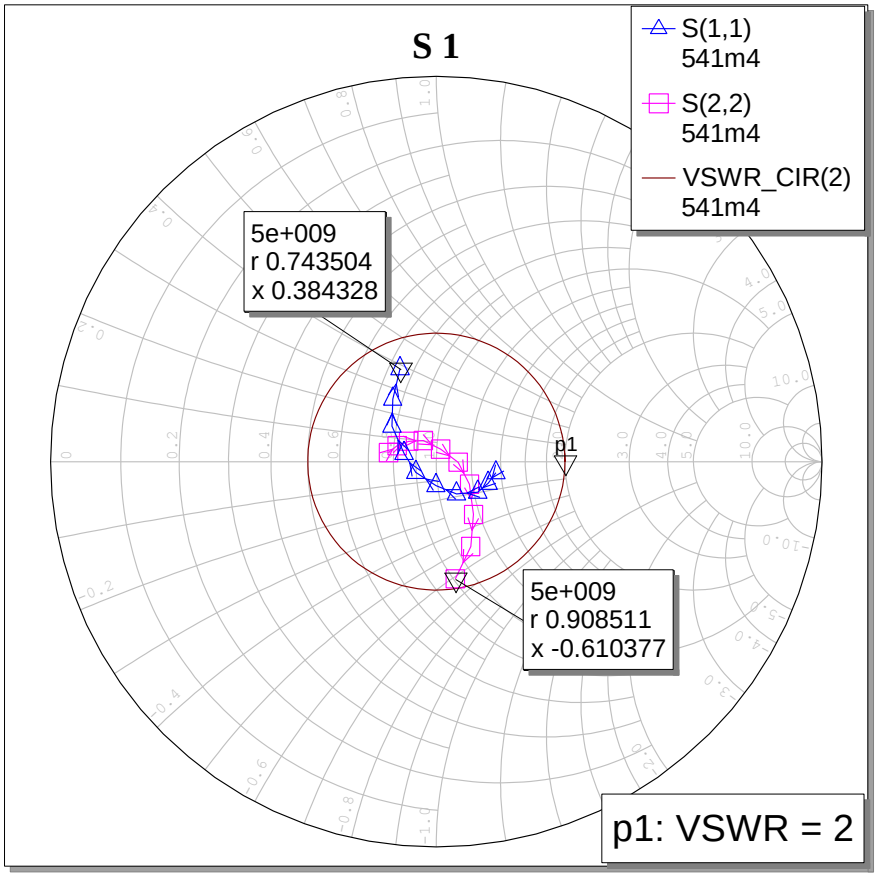

Figure 22 Smith Chart analysis

As it is seen in Figure 22, return losses get their maximum values at the highest frequency, but it is still inside the VSWR 2:1 circle.

The input return loss analysis in Figure 22 states that a small capacitor in shunt would move the return loss at upper frequencies to the center of the Smith Chart.

Finally for the schematic design of first stage, a small shunt capacitor at the input is added with its footprint pads. Transmission lines with characteristic impedance of 50Ω, which do not affect the return loss analysis considerably, are added to the input and output ports as seen in Figure 23.

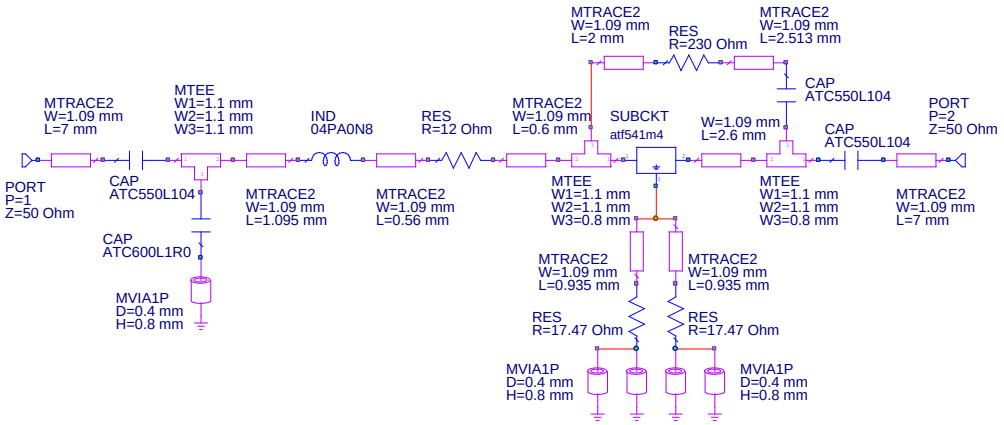

Figure 23 Final schematic for first stage

Another important point is that, lumped elements must be replaced by their S parameter data files which are provided from various suppliers. Especially using the S parameter models of capacitors and inductors may prevent the designer from unexpected situations. S parameter models of DC blocks at the input and output, the inductor and the capacitor at the input are used in the schematic.

Input and output return losses for the final configuration are shown plotted on a Smith Chart in Figure 24. As it is clearly seen, return losses are inside the VSWR 2:1 circle, most of the points are very close to the center of the chart.

Besides, it is seen that the output return loss in Smith Chart at 5 GHz is moved closer to the center of the chart compared to the previous analysis. Lower frequencies are also closer to the center than previous analysis, which means return loss of the design is satisfactory.

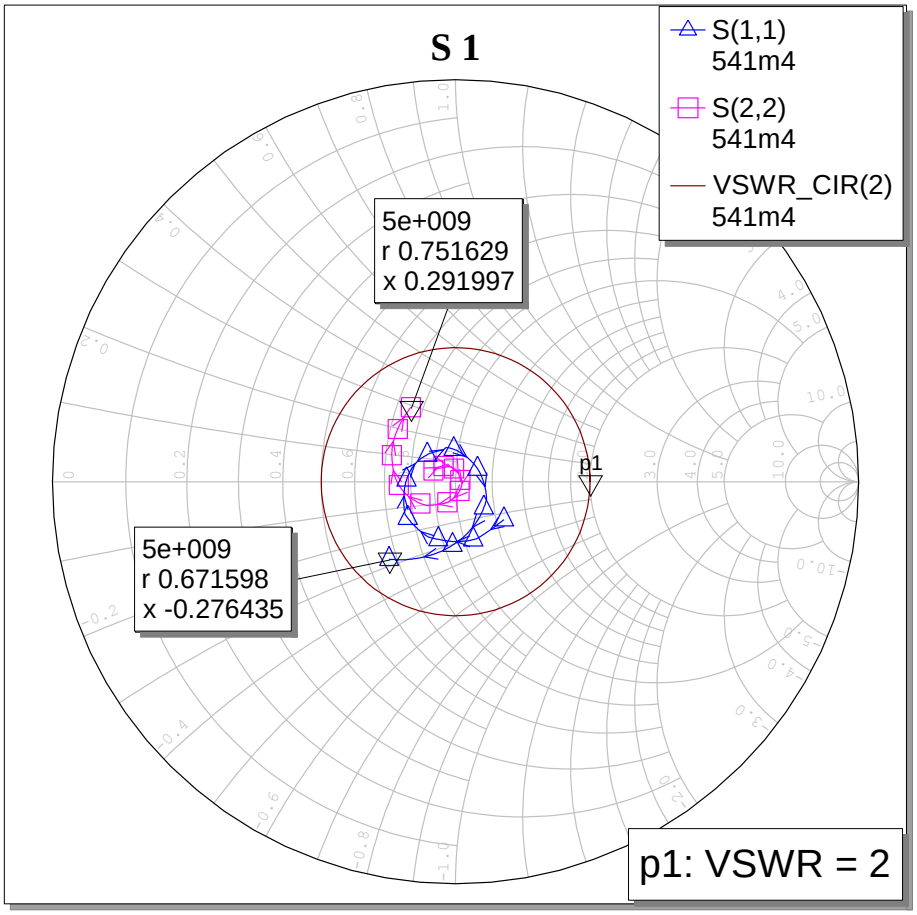

Figure 24 Smith Chart Analysis

Assigning random values to component parameters and using an optimizer tool would be a method for achieving the goals of the amplifier, but it would be an inappropriate engineering approach and take considerable simulation time. Instead, assigning logical values to the component parameters by tuning makes the optimizer very fast and accurate. After the element values are tuned manually while observing the graphs until reasonable results are obtained, optimizer can be used in order to get a better result. In this step, Simplex Optimizer tool is used over the frequency range of 0.5-5 GHz with the constraints below:

- $|S_{11}|$ and $|S_{22}| < -15$ dB
- $8 \text{ dB} < |S_{21}| < 10$ dB

This schematic analysis would give the idea of starting point of electromagnetic (PCB) analysis. So, achieving the optimizer goals fully would not be necessary at this point.

After the optimization, S_{11}, S_{22} and S_{21} of the final schematic in rectangular form are given in Figure 25.

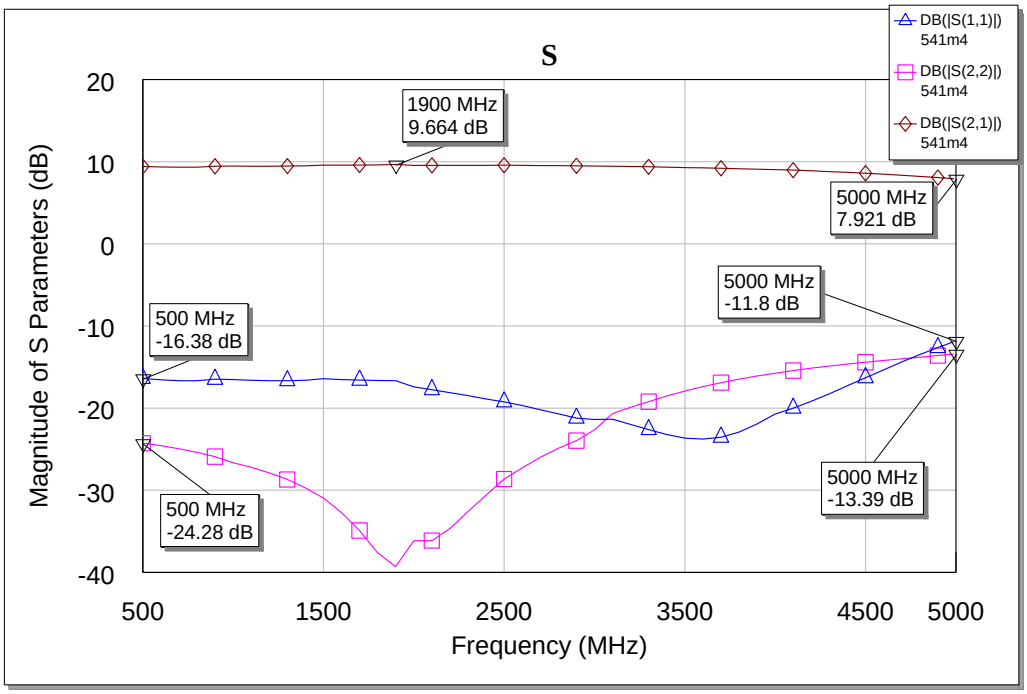

Figure 25 S parameters of final schematic

As seen from the figure, gain of the full circuit is between 9.6 dB and 7.92 dB. Return losses of the amplifier is below -15 dB for most of the bandwidth and may be up to -11.8 dB maximum, which is satisfactory for a schematic analysis.

For an amplifier design, stability is a consideration that must be checked at every critical step. Stability of an amplifier may be examined analytically or graphically using stability circles on Smith Chart. In this design, stability is considered analytically by μ-parameter that can be introduced as [15]:

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - S_{11}^{*}\Delta| + |S_{12}S_{21}|} \quad \text{where}$$

$$\Delta = S_{11}S_{22} - S_{21}S_{12}$$

For unconditional stability condition, the criteria below must be satisfied:

$$\mu > 1$$

Stability analysis is given below in Figure 26.

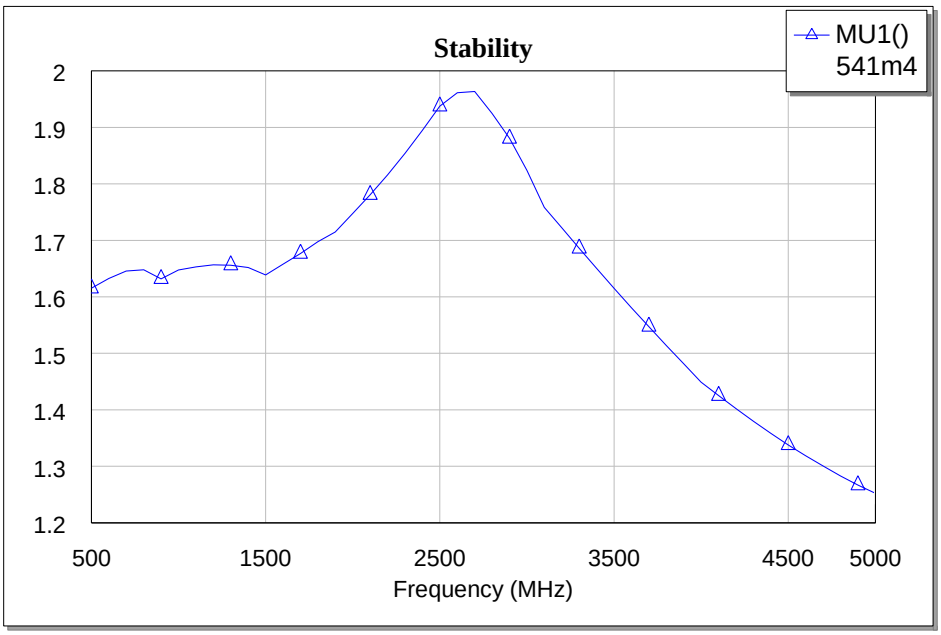

Figure 26 Stability Analysis

According to the stability analysis, because the μ parameter is greater than 1 at every point, the designed schematic is unconditionally stable.

3.2.5. EM Structure Design of First Stage

Once a satisfactory schematic simulation is obtained, electromagnetic simulations are run. Schematic simulation result gives the designer a rough answer about matching topology and component values, such as line width and lumped element

values and give an idea whether the proposed design is feasible or not. Schematic simulator generates and uses the S-parameter file of each element (lumped elements, transmission lines etc.) and then unites them to give the answer. But it cannot solve the mitering/ tapering effects, electromagnetic coupling between separate transmission lines which is a vital point in operation of a circuit in real life. To make a realistic simulation, EM simulation using the S parameters of all discrete components is run as a whole-PCB simulation.

All of the microstrip elements should be replaced with its electromagnetic equivalent, and then the whole PCB should be analyzed at one time in order to take the couplings between different lines into account. Lumped component values may change by optimization from the previous schematic analysis as the EM analysis proceeds.

Schematic simulator takes the S-parameter data of the EM Structure, and then combines this information to make its own schematic calculations with other elements.

Replacing the transmission lines is started from the element nearest to the transistor, the input tee. The input tee is substituted with its EM model which is created by EM Structure tool of AWR, and put back to the schematic as seen in Figure 27.

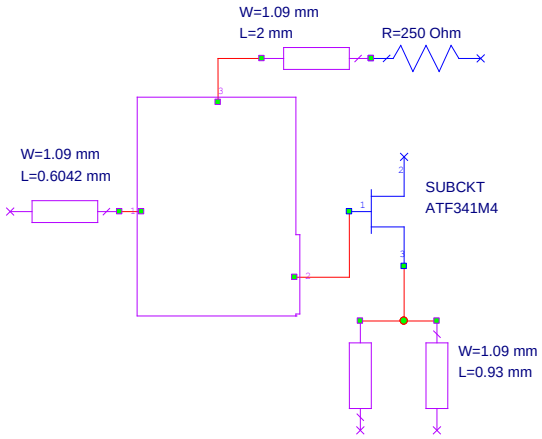

Figure 27 Part of the schematic with replaced EM subcircuit of input tee

Result of this substitution is seen in Figure 28. Small changes occur as a result of this substitution, which is normal and more realistic as compared to the schematic analysis.

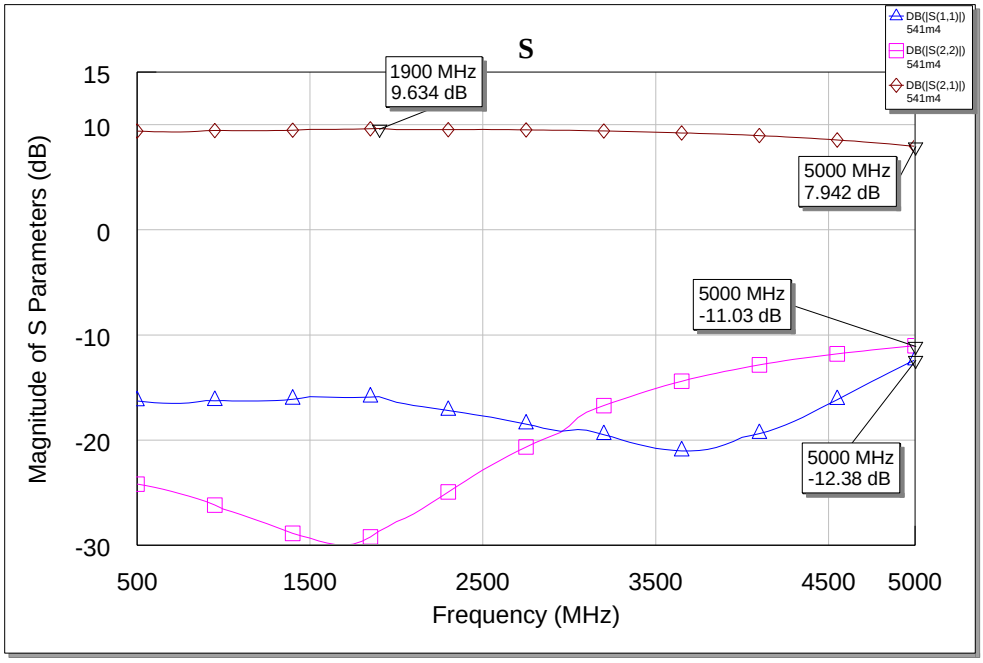

Figure 28 S parameter analysis

Feedback path and pads of discrete components are added to the EM Structure, and replaced with their schematic model in Figure 29. It is important that the gaps between transmission lines are equal to the footprints of SMD components, so that, this would be a more realistic simulation that considers the coupling effects between the lines than using random gaps. In high frequency designs, lumped components with 0402 or 0201 package size are preferred because their parasitic effects are less than components with 0603 or bigger package size. In this study, lumped elements with 0402 package size are used since they are easier to assemble to the PCB than 0201 size. Length of a lumped component with 0402 size package is nearly 1 mm, and width is 0.6 mm. The gap between its pads is

nearly 0.6 mm. So, 0.6 mm gaps are left between the transmission lines where lumped components will be assembled.

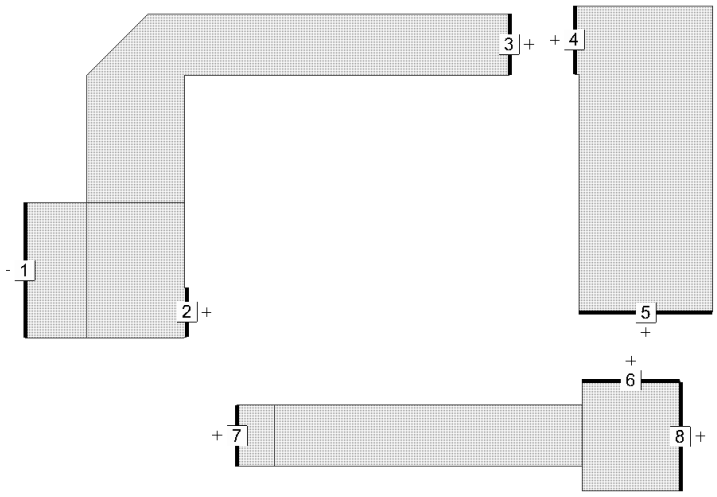

Figure 29 EM Structure of feedback path and transmission lines

AWR generates a subcircuit of EM structure after evaluating it. For this reason, discrete elements must be connected to the correct nodes of this subcircuit, which is a critical step for accurate simulation. AWR gives the opportunity of seeing the subcircuit as a projection of the EM structure, as seen in Figure 30.

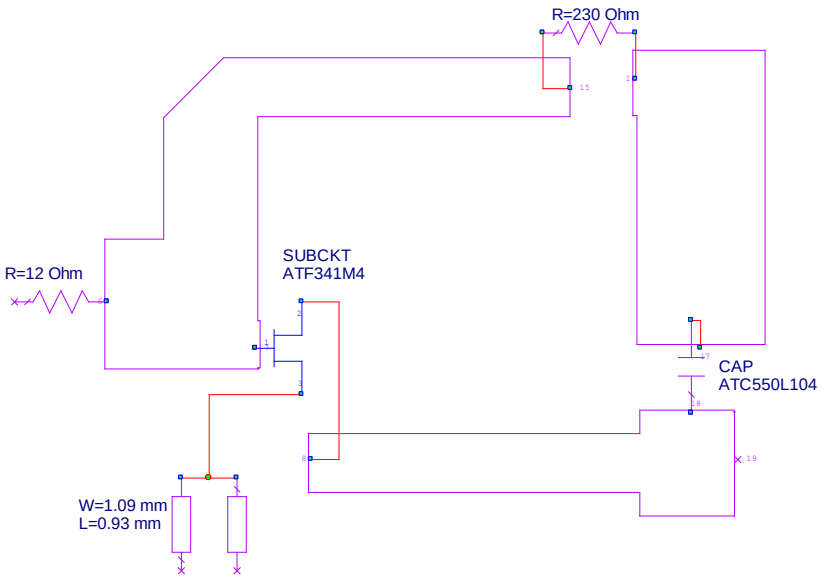

Figure 30 Part of the schematic with imported EM Structure

Replacing the schematic elements with EM subcircuits affects the S parameter analysis. So, tuning/optimizing the values after every substitution may be necessary. Results of the upper schematic after tuning are given in Figure 31.

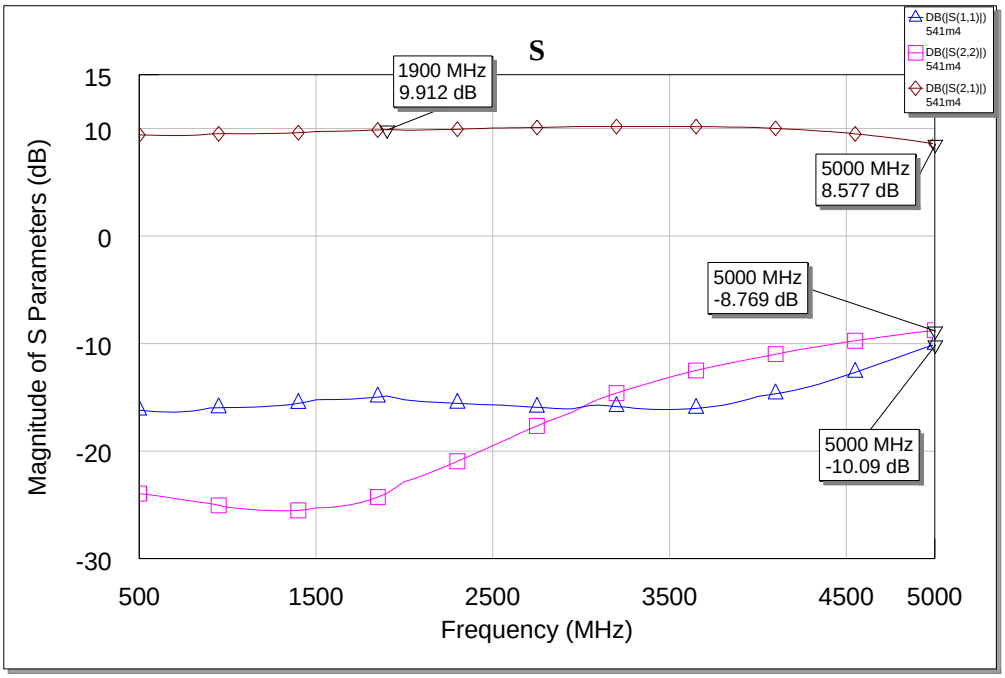

Figure 31 S Parameter Analysis

As it is seen, the results are still acceptable considering the rest of the schematic.

All other elements are replaced with EM models, and after tuning the final circuit is formed. Footprint of whole EM structure is shown in Figure 32.

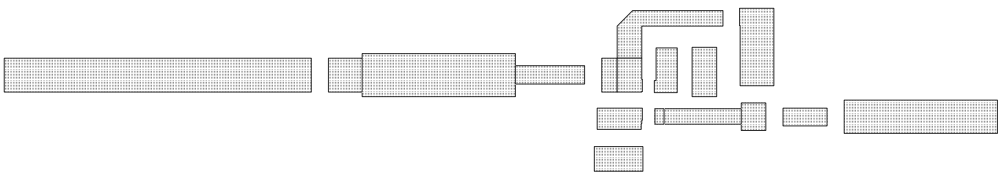

Figure 32 EM Structure of whole circuit

The final circuit which contains all discrete elements and EM structure is split for clear display. Input section is given in Figure 33.

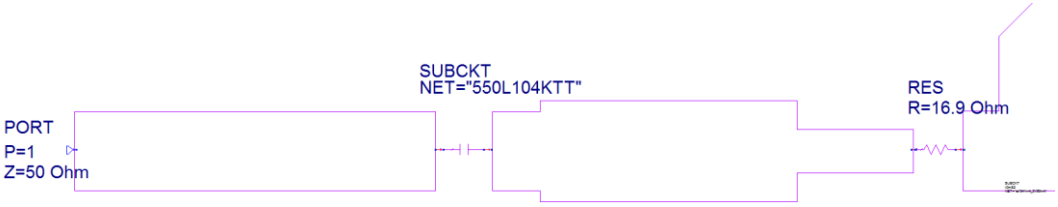

Figure 33 Input Section

Medium section that contains the feedback path, transistor pads and vias is given in Figure 34.

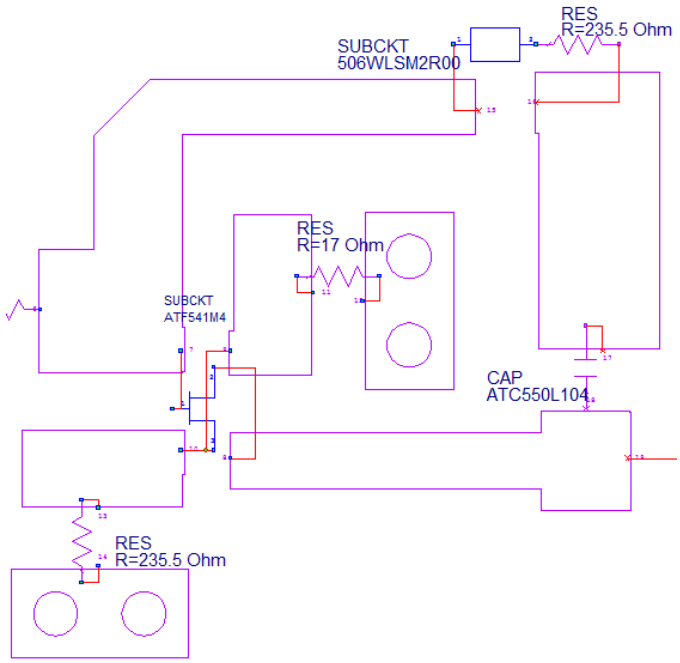

Figure 34 Medium Section

Finally, the output section is given in Figure 35.

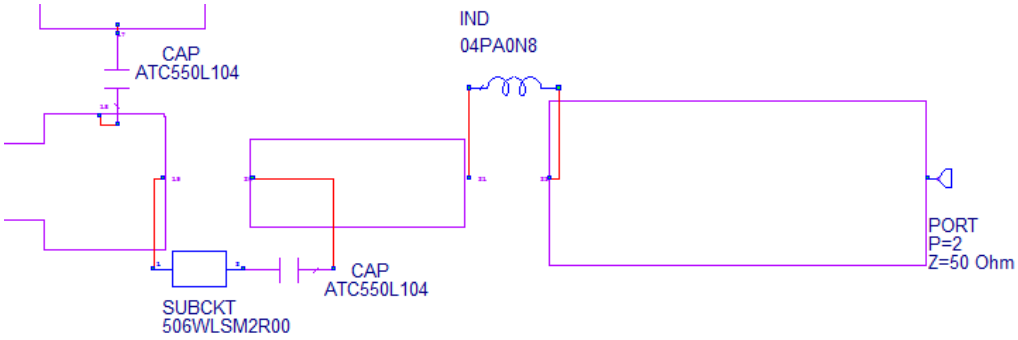

Figure 35 Output Section

Meshing is one of the most important steps in an EM analysis. The smaller the meshes, the more accurate and realistic the results are. As the meshing gets smaller, simulation time increases considerably. Maximum frequency in this design is 5 GHz, whose wavelength in the selected substrate is nearly 3.26 cm. So, 0.04 mm of grid size is considered to be accurate. In Figure 36, Figure 37 and Figure 38, close up views of meshed geometry are given.

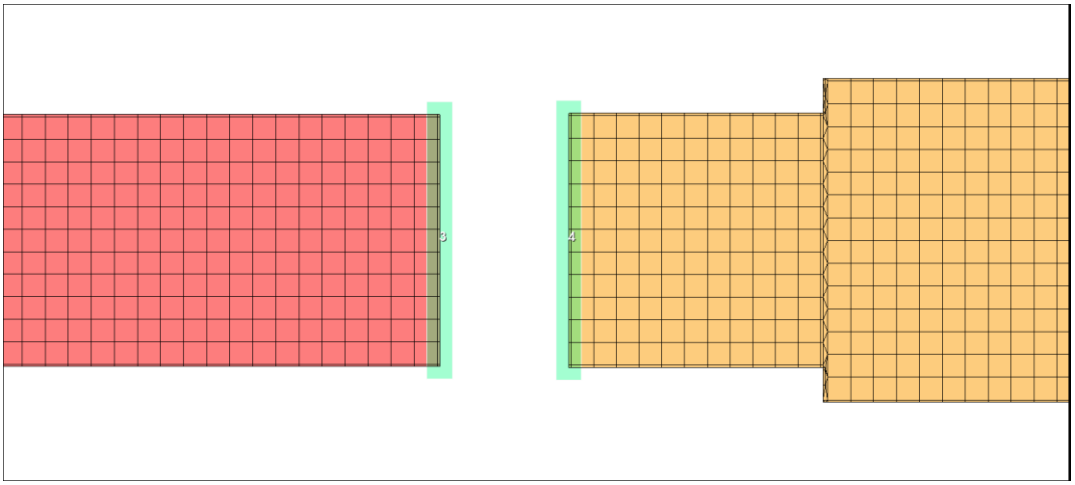

Figure 36 Meshing example in the circuit-1

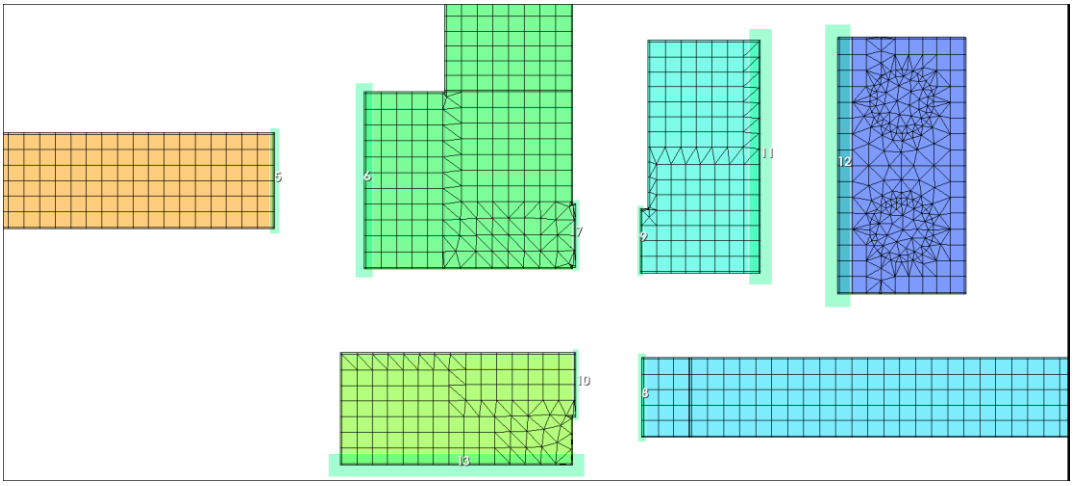

Figure 37 Meshing example in the circuit-2

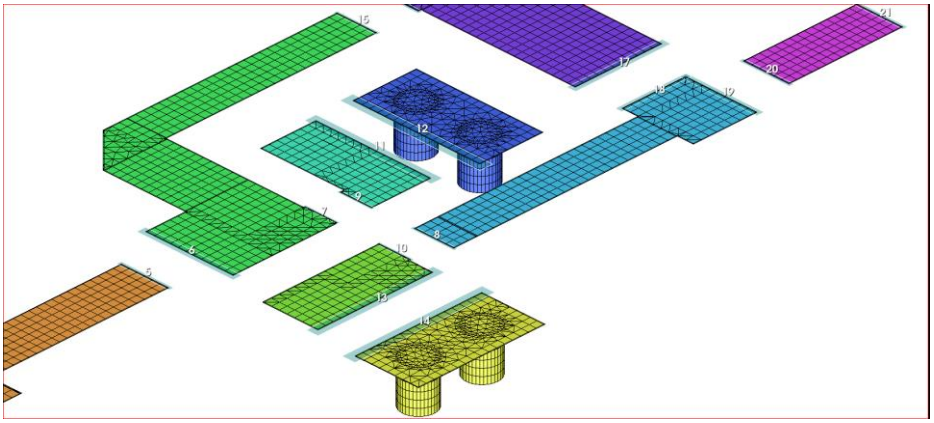

Figure 38Meshing example in the circuit-3

As seen in Figure 36, Figure 37 and Figure 38, meshes are bigger at flat and continuous sections. But they get smaller at the sections of discontinuity and rapid changes in order to model these segments better. For example circular vias, pad ends and the interstage sections of different lines are are smaller and denser as compared to the other flat transmission line sections.

Gain (S_{21}) analysis of full schematic that is formed by Figure 33, Figure 34 and Figure 35 is given in Figure 39.

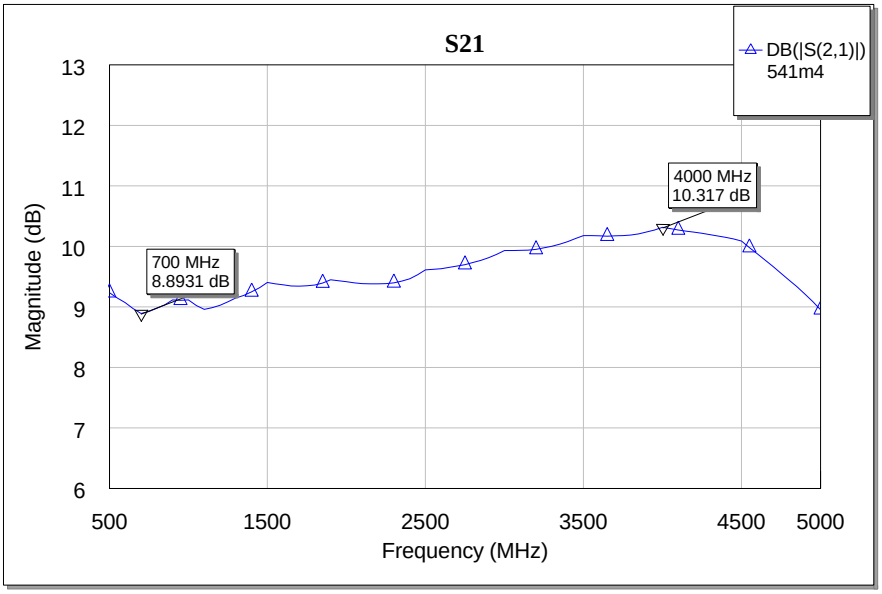

Figure 39 Gain analysis of full schematic with EM structure

As seen from the graph, S_{21} changes between 8.9 dB and 10.3 dB throughout the whole band, which is satisfactory. Return loss graphs are given in Figure 40.

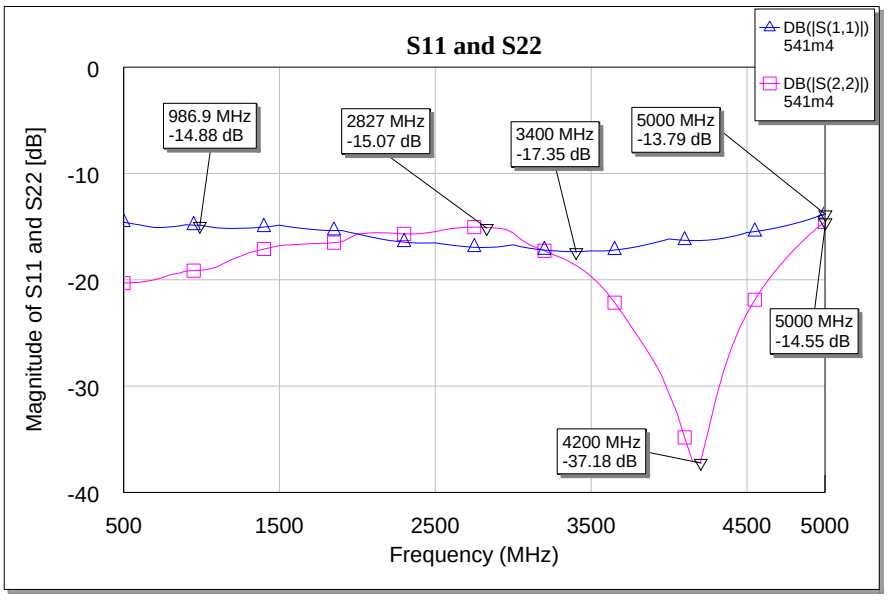

Figure 40 Return loss analysis of full schematic with EM structure

From Figure 40, input and output return losses may be considered as satisfactory. Maximum input and output return losses are 14.55 dB and 13.79 dB, respectively, but they are above 15 dB at the most of the band.

Stability analysis is shown in Figure 41.

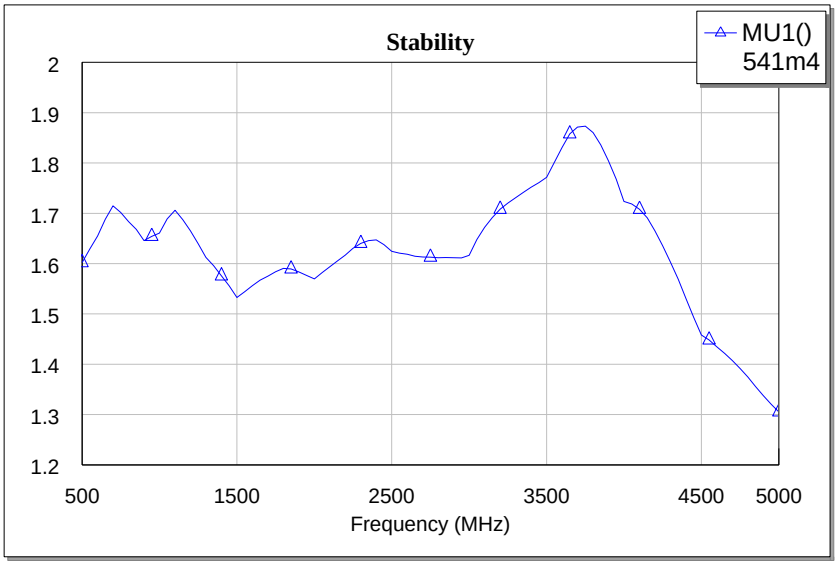

Figure 41 Stability analysis of full schematic with EM structure

Considering the stability analysis, the design is said to be unconditionally stable because μ parameter is greater than 1 over full band.

Since all S parameters are quite satisfactory and the design is unconditionally stable, the amplifier can be fabricated.

3.2.6. Fabrication of the First Stage

PCB design phase is conducted by AWR Microwave Office Layout Tool. Performing an EM analysis provides the designer big convenience, because all the critic transmission lines are generated at that step, which are ready to use in PCB design.

Layout is generated as below in Figure 42.

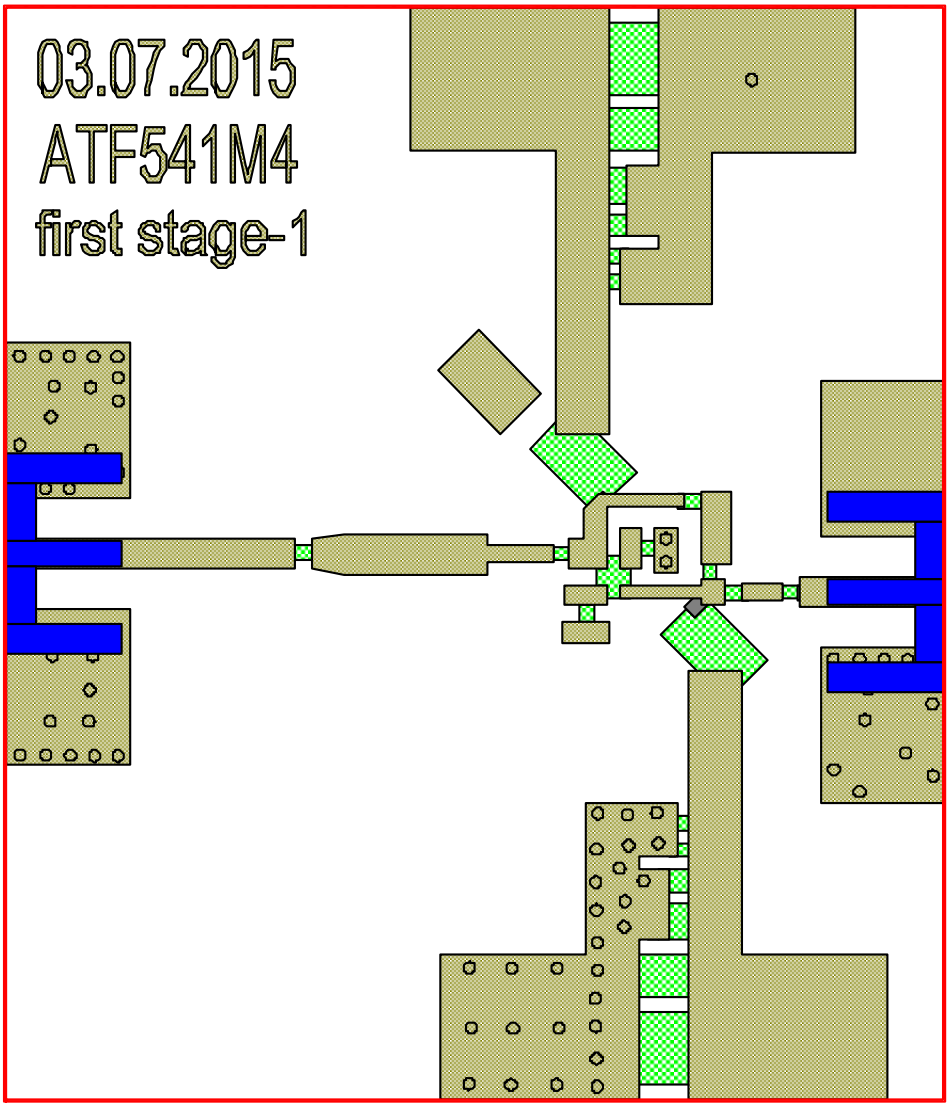

Figure 42 Layout of the first stage

The blue regions are footprints of SMA connectors which will be soldered to the input/output transmission lines and ground pads. Also, gaps for decoupling capacitors of different physical packages (0402, 0603, 1206 etc.) are considered between the voltage line and ground pads. Moreover, the gaps of conical inductors are designed to be suitable for different packages in case there will a need for a different conical inductor.

In Figure 43, close view of the center of the PCB is given.

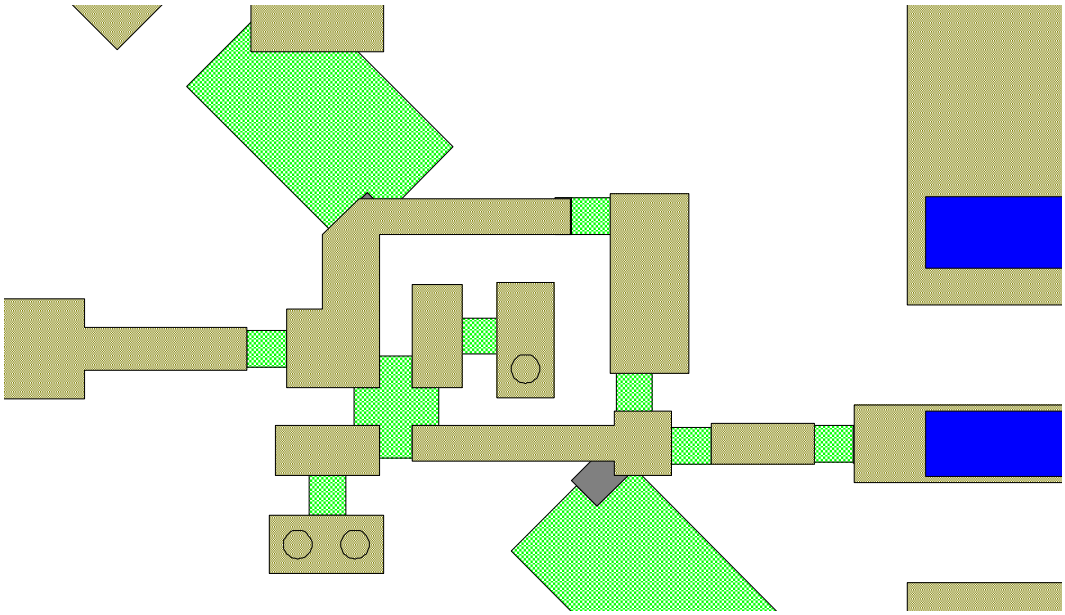

Figure 43 Close view of the center of the layout

As it is seen from the layout, minimum line width is limited with the minimum width of the discrete elements. Also, gaps between the pads are adjusted considering the physical dimensions of lumped elements with 0402 package size. So that, soldering the elements to their pads would be easy.

The layout is fabricated on Rogers 4003 substrate with 20 mil height. Picture of fabricated PCB with assembled elements are given in Figure 44.

The PCB is 3.2 cm as long and 3.8 cm as wide. The height of the PCB is 20 mils. Therefore, a metal plate is assembled to the bottom of the PCB to increase its mechanical strength, so that, unpleasant accidents such as breaking the PCB during measurements are avoided.

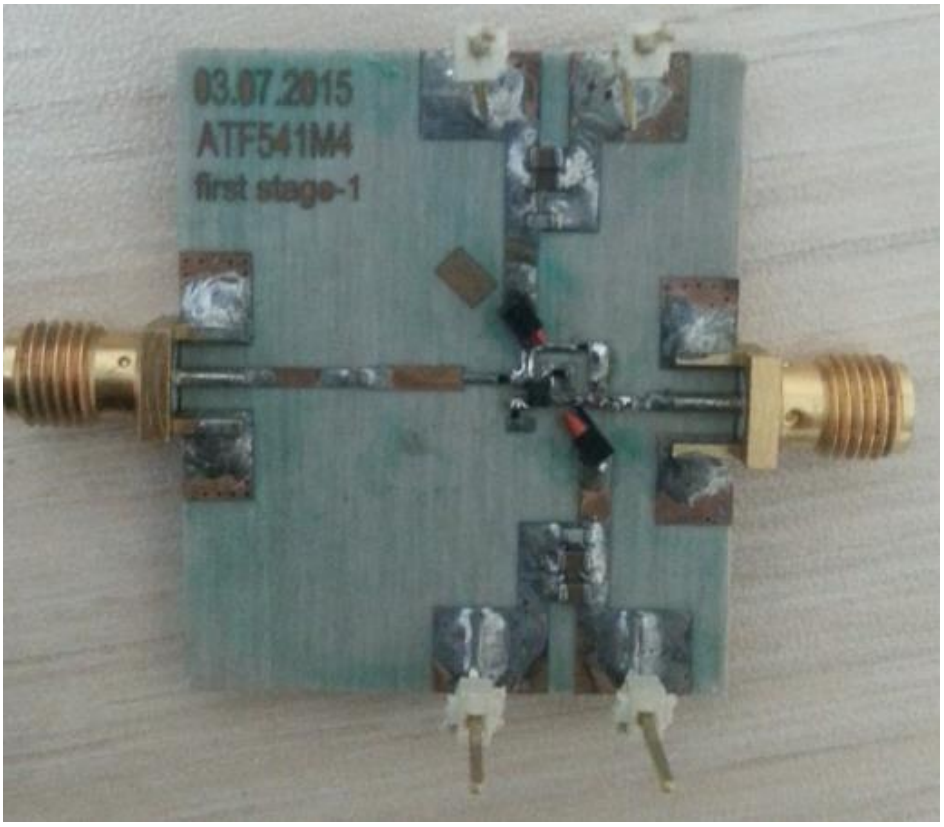

Figure 44 Fabricated PCB of first stage

3.2.7. Measurement of the First Stage

After the amplifier is fabricated, first step for making measurements is applying the DC voltage. During simulation phase, 3V drain voltage and 60 mA drain current is considered, and S parameter file of the specified ratings is used.

For normal biasing, 0.6V gate voltage would produce 60 mA drain current, as expressed in the datasheet. But, since there are resistors at the source pins of the transistor, there would be less current for 0.6V gate voltage. For this reason, drain current should be adjusted to 60 mA by changing the gate voltage.

First, drain voltage is applied and no current is observed. Then 0.6V gate voltage is applied, and the drain voltage is seen as nearly 25 mA, as expected. By increasing the gate voltage, the drain voltage is observed to increase. At 1.02V

gate voltage, the drain current is read as 60 mA, and the transistor biased successfully.

S parameter measurement is made with Agilent N5230A PNA-L Network Analyzer. After making calibrations for 0.5-5 GHz, the amplifier is connected to the network analyzer and the measurement result is given in Figure 45.

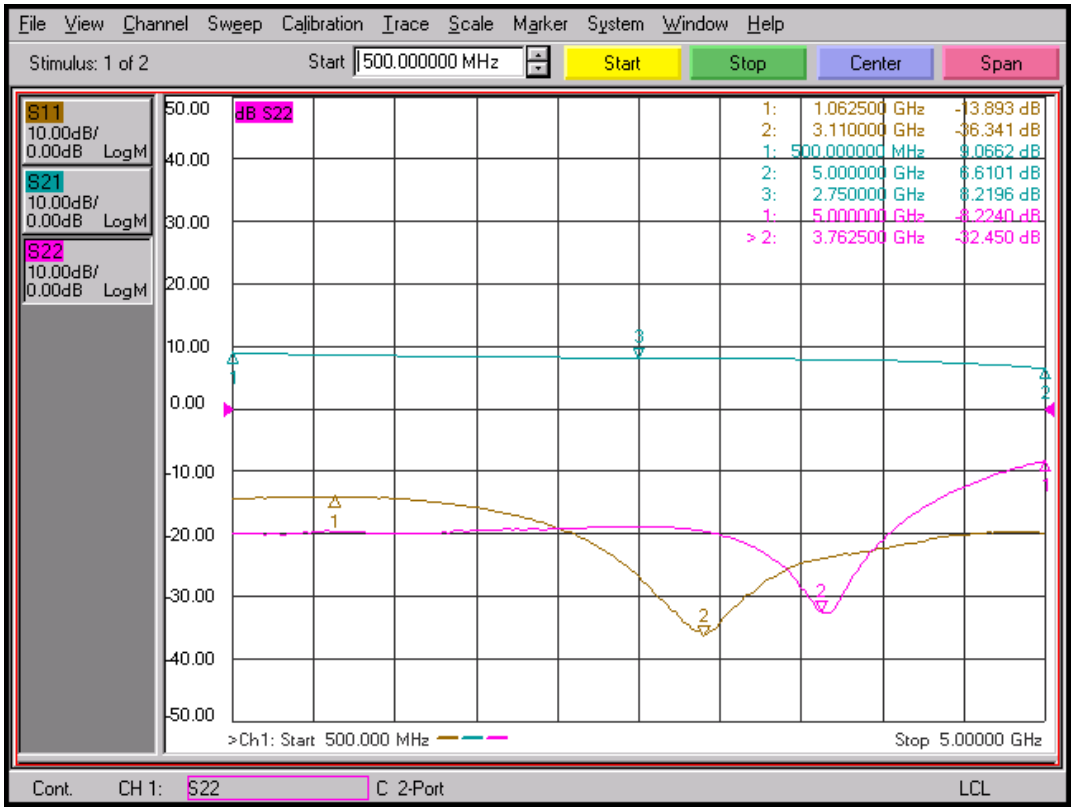

Figure 45 S parameter measurement screen

As it is seen from the measurement, gain level is nearly 9 dB at 500 MHz, and decreases as the frequency increases, as expected from the simulations. Also, input and output return losses are below -15 dB for most of the bandwidth, which is quite similar with the simulation results.

In Figure 46 and Figure 47, measured and simulated gain and return loss parameter is compared in same graphs.

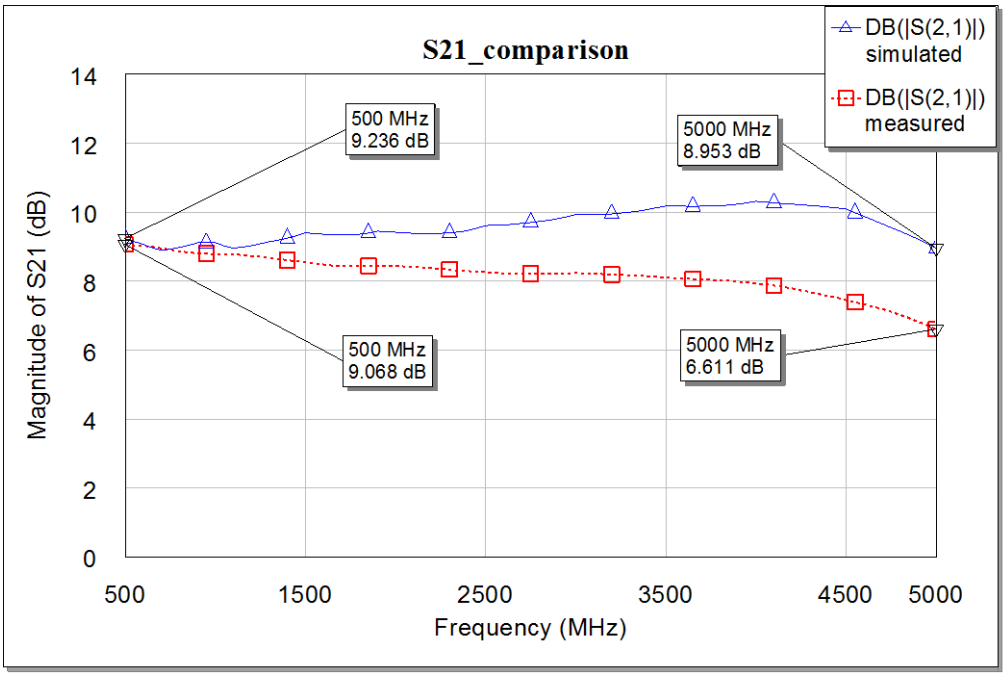

Figure 46 Gain comparison of simulation and measurement

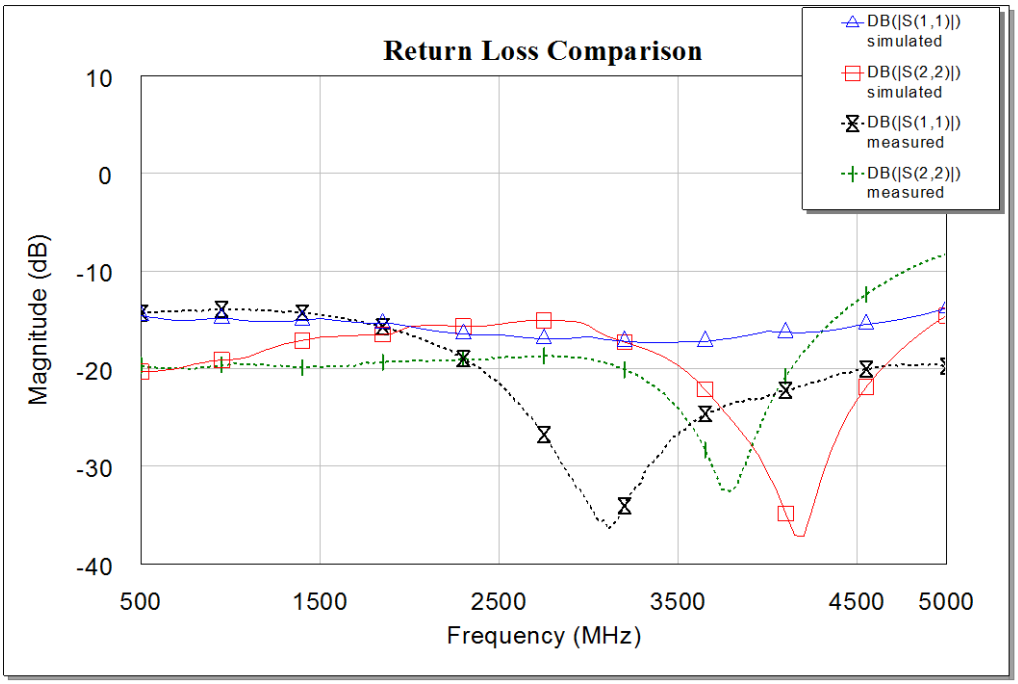

Figure 47 Return loss comparison of simulation and measurement

According to comparison of simulated and measured gain parameter, there is nearly 0.2 dB difference at 500 MHz, and nearly 2.3 dB difference at 5 GHz. The difference between simulated and measured increases as the frequency increases, which is expected. The effect of parasitic elements and component tolerances are directly proportional with increased frequency.

As seen from return loss comparison graph, simulated and measured values are quite similar. Measured input and output return loss values are smaller than simulated values at low frequencies. As the frequency increases, it is seen that measured values are greater than simulated values, which is expected considering the same reasons with gain comparison graph.

After the S parameter measurement is finished, basic stability test is applied. Same DC voltages are applied to the amplifier, input connector is terminated with 50 ohm, and output of the circuit is connected to the spectrum analyzer. No signal between 100 MHz and 18 GHz frequency spectrum is observed. So, the fabricated amplifier is considered as stable.

3.2.8. Schematic Design of the Second Stage

At the second stage of the cascaded feedback amplifier, ATF34143 of Avago Technologies is selected as the active device. Design procedure is same as the first stage.

First, S parameter file of the transistor with appropriate bias point is imported to AWR Schematic Tool. Bias point of the transistor is selected as 4V drain voltage and 60 mA drain current as expressed in the datasheet of the transistor. Gate voltage should be adjusted during measurements to tune the drain current as 60 mA, as in the measurement of the first stage. S parameters are analyzed which are shown in Figure 48.

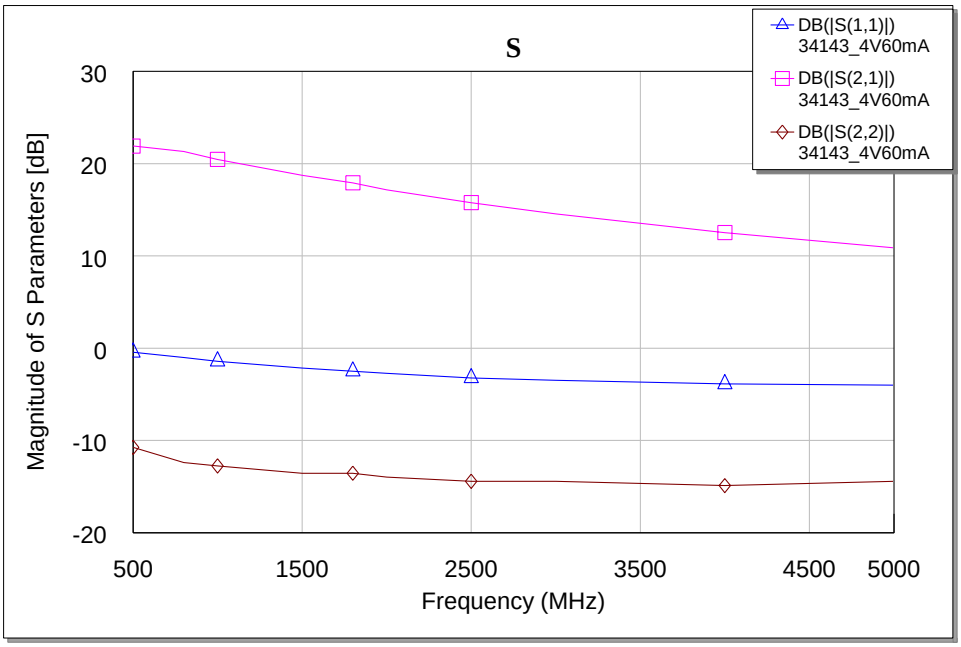

Figure 48 S parameters of ATF34143

As it is observed from the S parameters analysis, gain of the transistor decreases as the frequency increases, as expected.

In order to equalize the gain, feedback topology is applied as in the first stage design. Feedback and source resistors are tuned and selected as 450 and 7 ohms, respectively, as given in Figure 49.

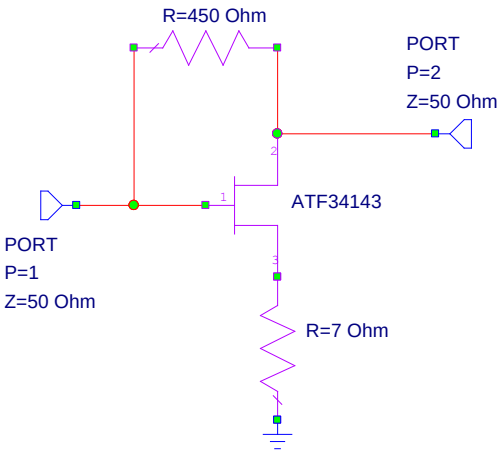

Figure 49 Feedback topology applied to ATF34143

S parameter analysis after feedback topology is shown in Figure 50.

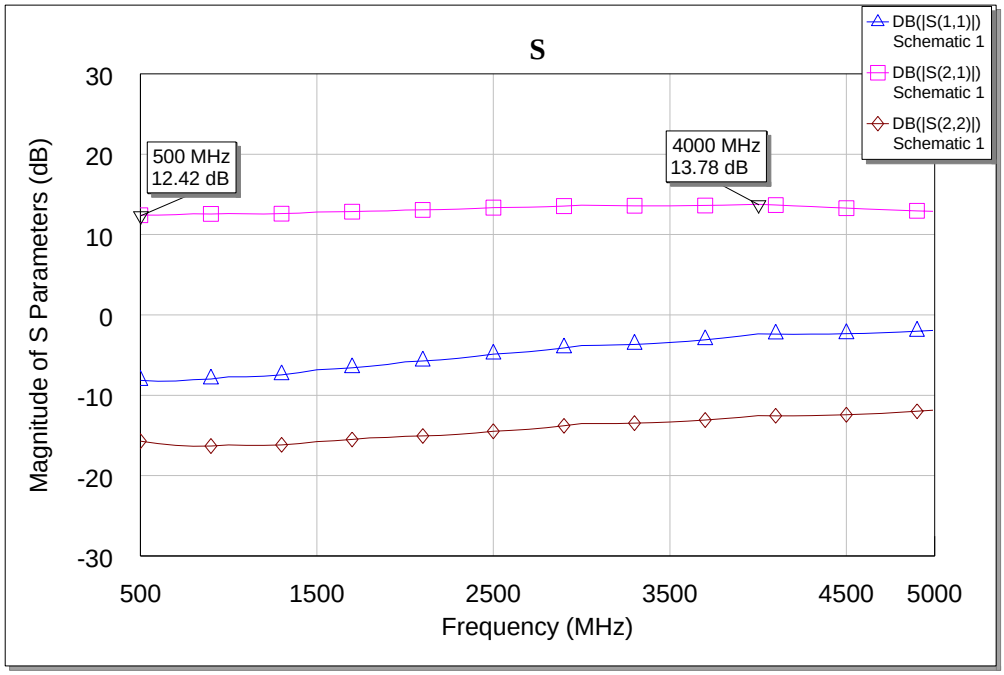

Figure 50 S parameters of ATF34143 with feedback

As it is observed from the graph, gain is well equalized according to the previous simulation. After that, input and output matching networks should be designed considering the stability.

Smith Chart results are given in Figure 51. According to the Smith Chart, output return loss is inside the VSWR 2:1 circle, but input return loss is poor.

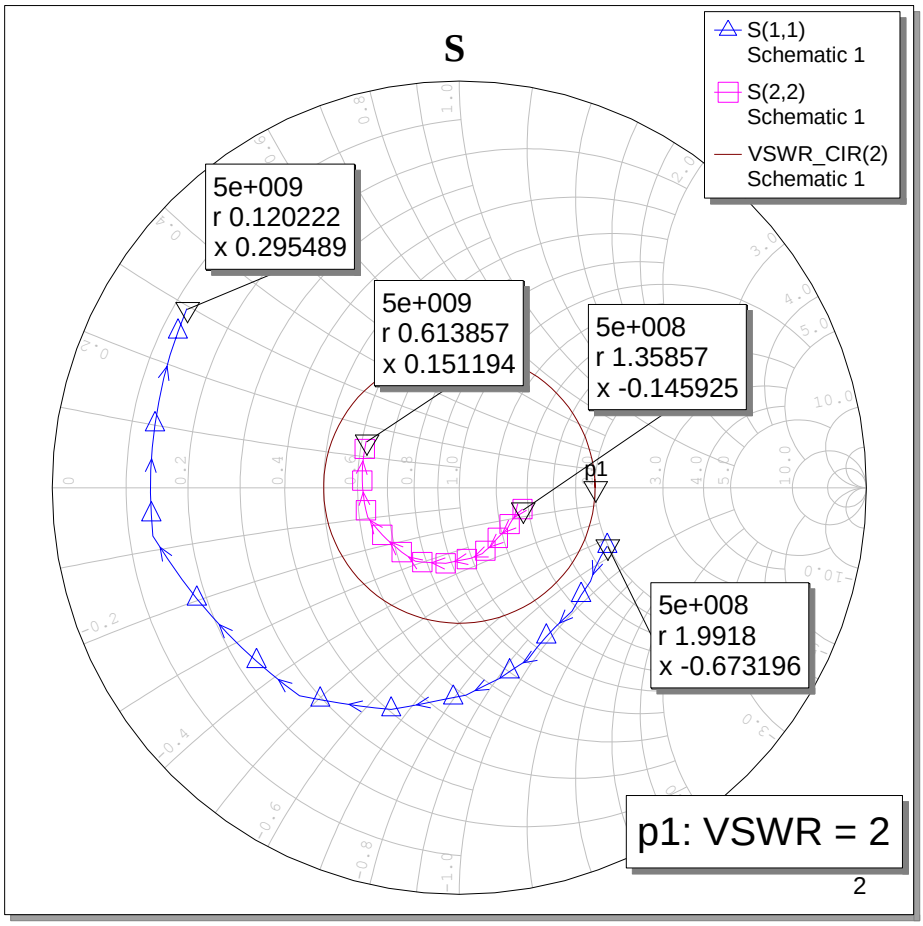

Figure 51 Smith Chart analysis of feedback topology

As in the first stage amplifier, a resistor is placed at the input of the amplifier to shrink input return loss to the center. Also, pads and transmission lines between the components are added to the schematic. These pads and transmission lines are inductive elements. So, the need for inductive elements for input return loss at lower frequencies is met. Values of the lumped elements and parameters of transmission lines are tuned manually by observing the Smith Chart. The schematic and its Smith Chart analysis are constituted in Figure 52 and Figure 53, respectively.

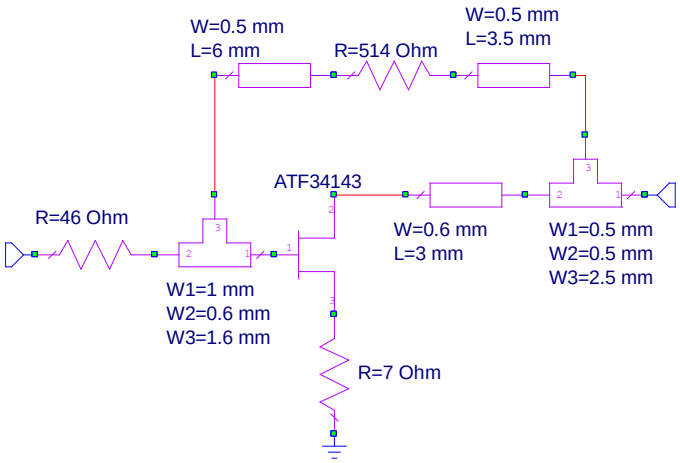

Figure 52 Schematic with transmission lines and lumped elements for matching

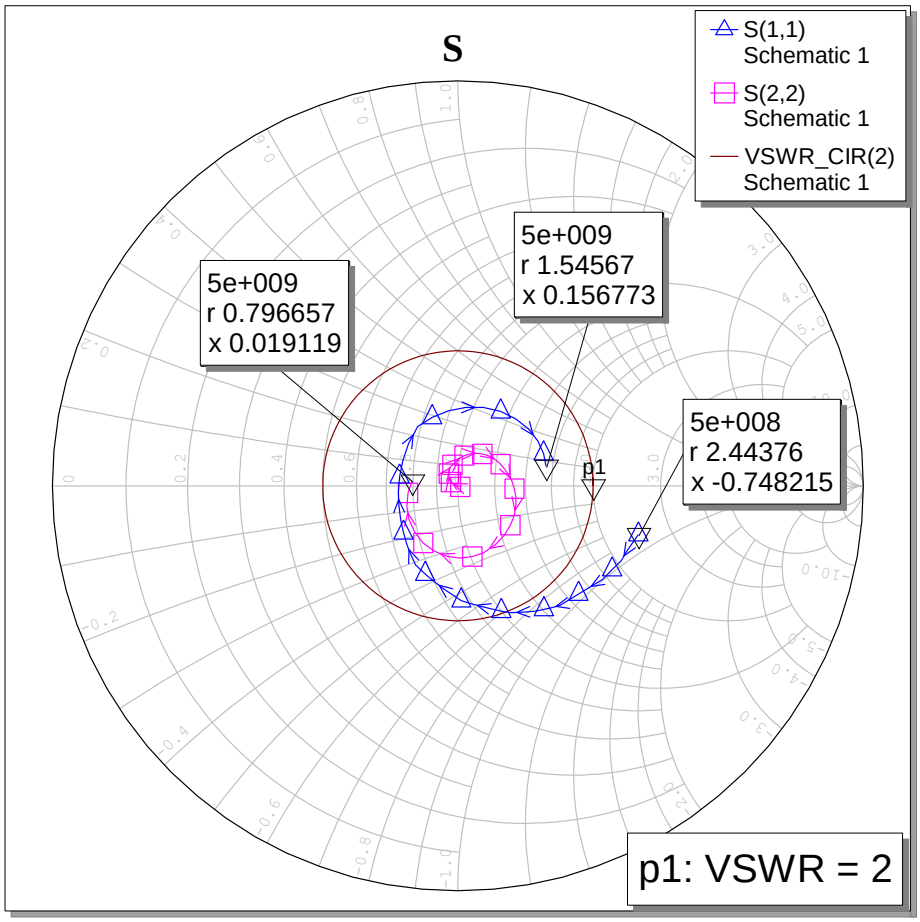

Figure 53 Smith Chart analysis

Output matching seems quite good, but input matching still needs to be enhanced. According to the Smith Chart, capacitive elements in series and inductive element in shunt is needed. So a highpass filter topology is applied to the input side of the amplifier. Element values are tuned manually and the schematic given in Figure 54 is created.

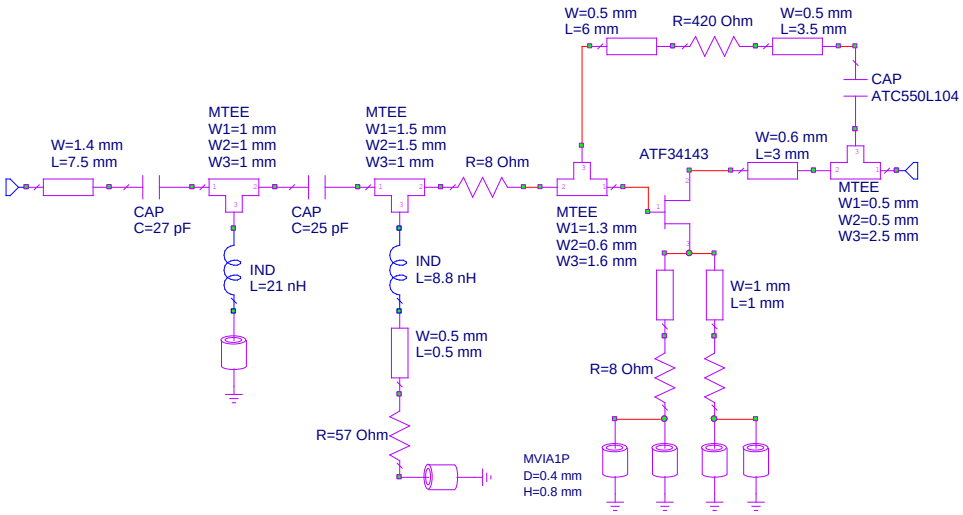

Figure 54 Schematic with added input matching network

Smith Chart analysis of this schematic is shown in Figure 55. As it is seen, input matching is enhanced, but output return loss became poorer. According to Smith Chart, a capacitive element in series and an inductive element in shunt can move the output return loss towards the center of the chart.

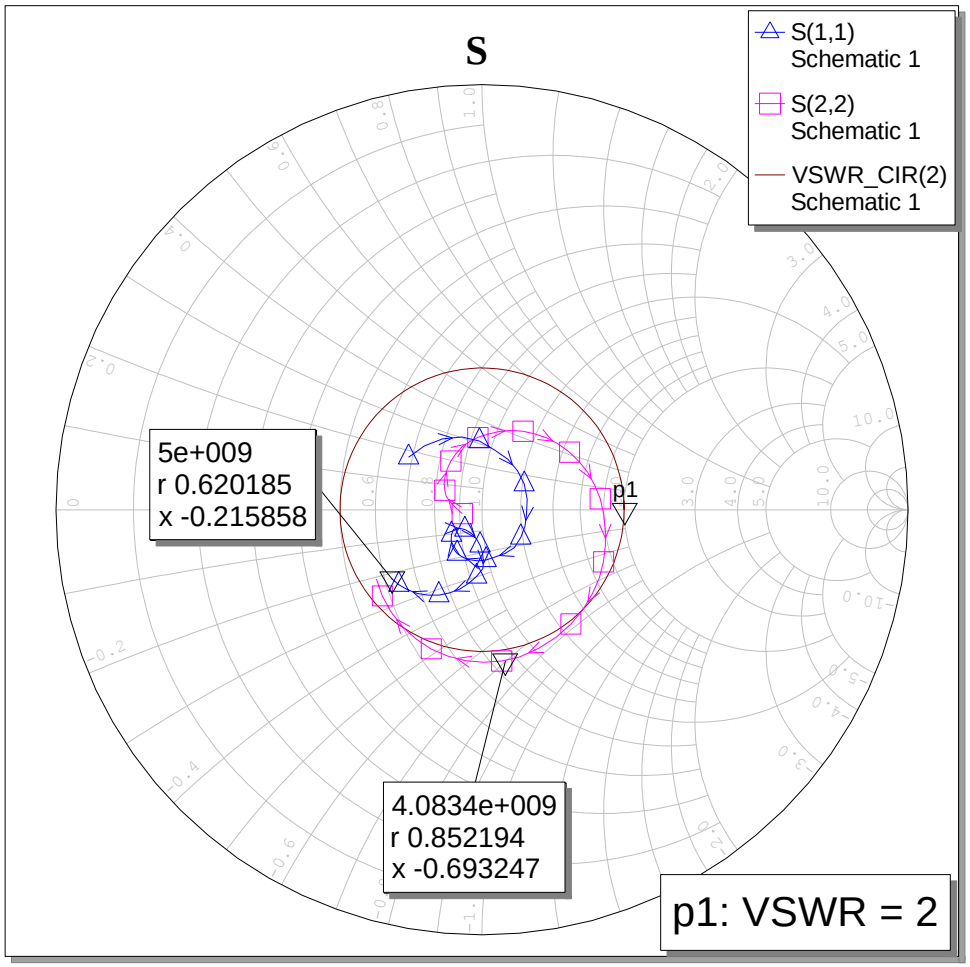

Figure 55 Smith Chart analysis

So, finally, a highpass output matching network is added to the output of the schematic, tunings are applied and final form of the schematic is formed as seen in Figure 56.

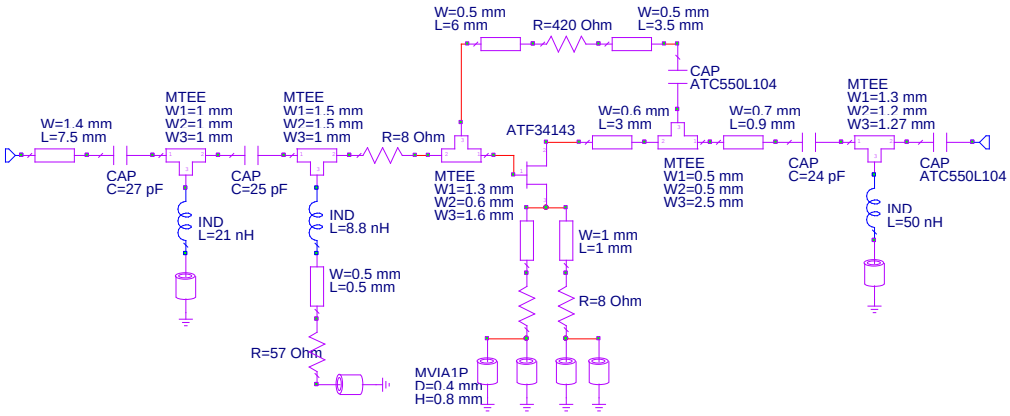

Figure 56 Final form of schematic of the second stage

Smith Chart analysis of this schematic is given in Figure 57.

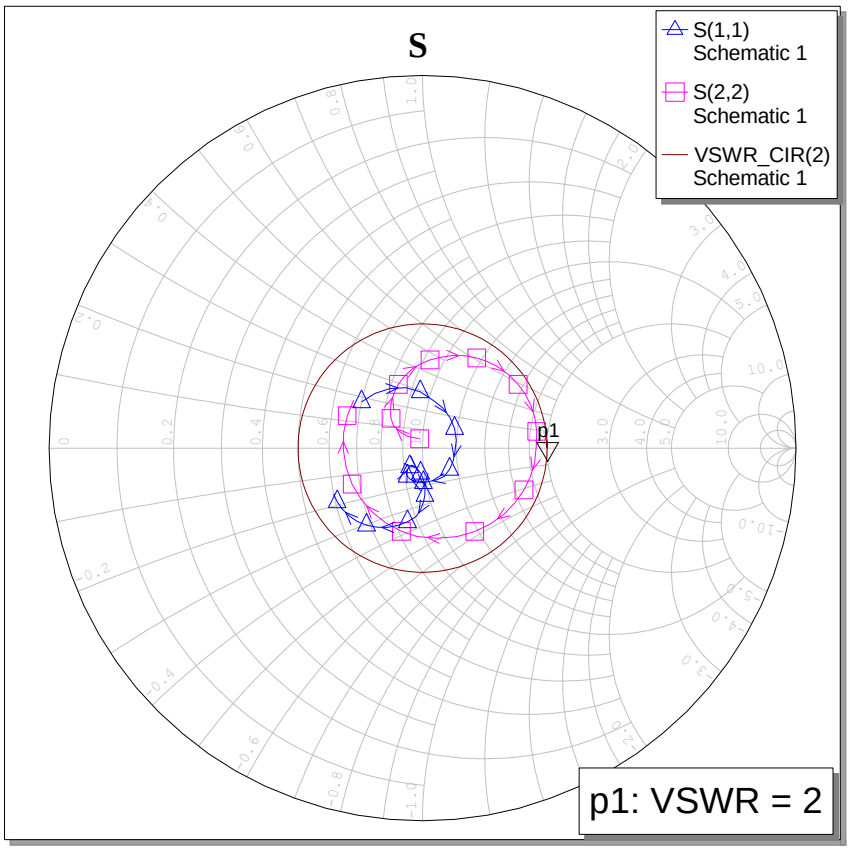

Figure 57 Smith Chart analysis

As it is seen from the chart, input and output return loss are both inside the VSWR 2:1 circle. Rectangular form of the Smith Chart above is shown in Figure 58.

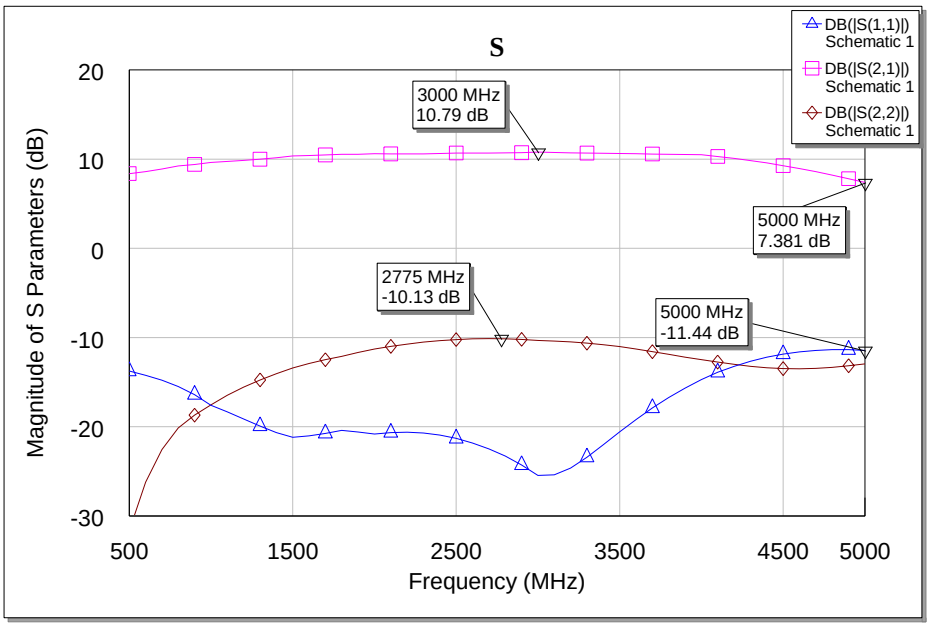

Figure 58 S parameters of schematic of the second stage

In Figure 58, gain is considered to be equalized according to the first step. Input return loss is below 15 dB for most of the bandwidth, and output return loss may be considered to be satisfactory. Stability analysis is given in Figure 59.

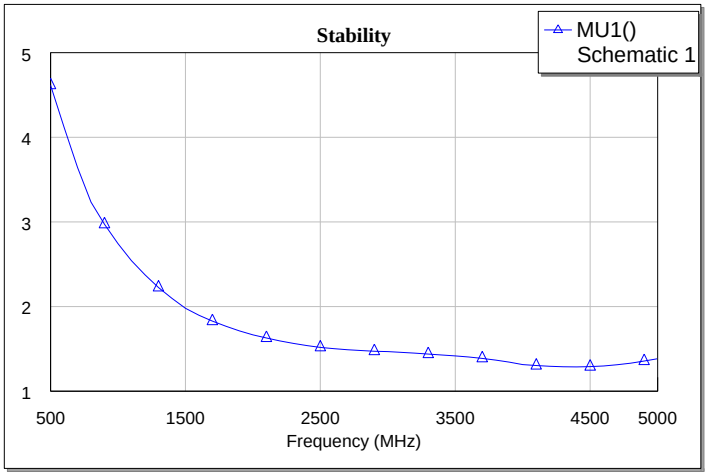

Figure 59 Stability analysis

According to this result, the design is considered to be unconditionally stable because μ parameter is greater than 1 over full band. After these results, EM analysis can be examined.

3.2.9. EM Structure Design of the Second Stage

As in the design of the first stage, substituting the transmission lines with their EM equivalents is started from the element nearest to the transistor. The feedback paths, lumped element pads and input and output tees are created as an EM Structure in the EM tool of AWR as shown in Figure 60. Again, Rogers RO4003 substrate with 20 mil thickness is used, and grid size is taken to be 0.04 mm.

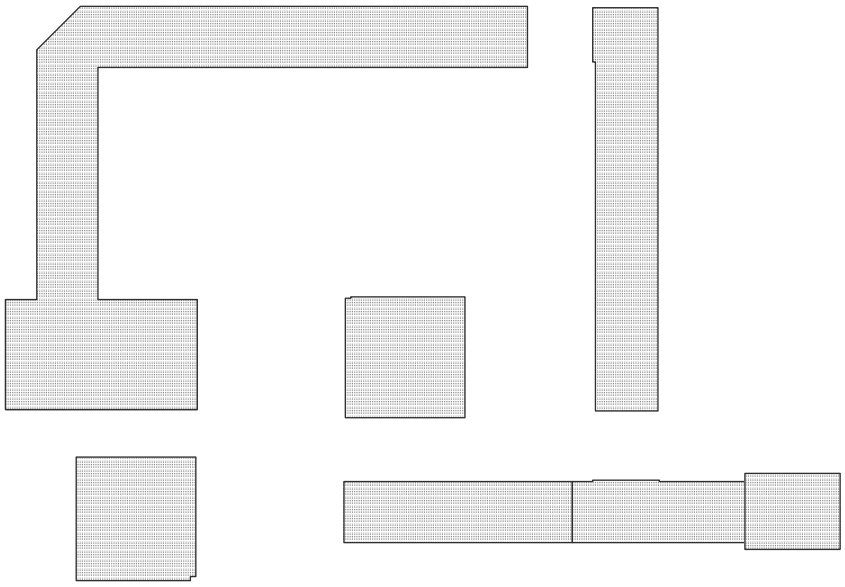

Figure 60 EM models of transmission lines and tees near to the transistor

After creating the EM structure, it is extracted as a subcircuit into the schematic, tunings are made and the schematic is shown in Figure 61.

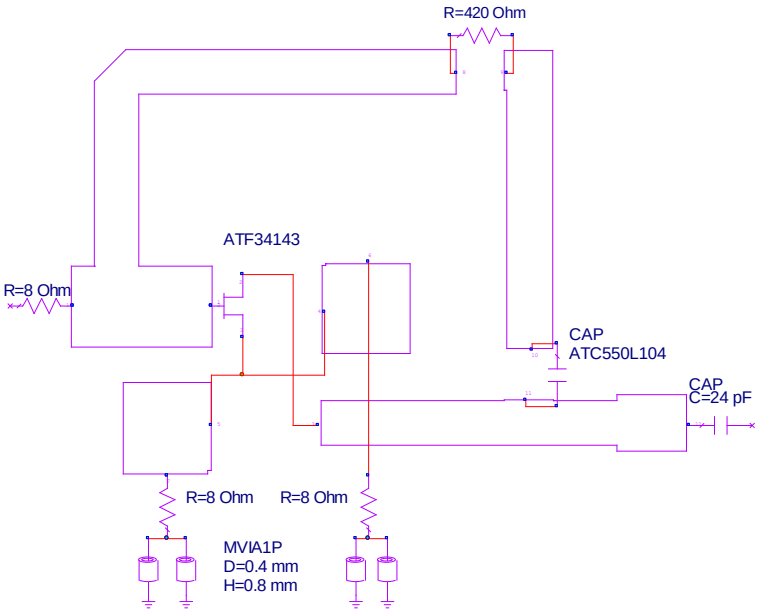

Figure 61 Part of the schematic with EM structure

Schematic analysis with the EM subcircuit above gives the S parameter analysis in Figure 62. Small differences are observed, but it is not critical considering the other elements to be optimized.

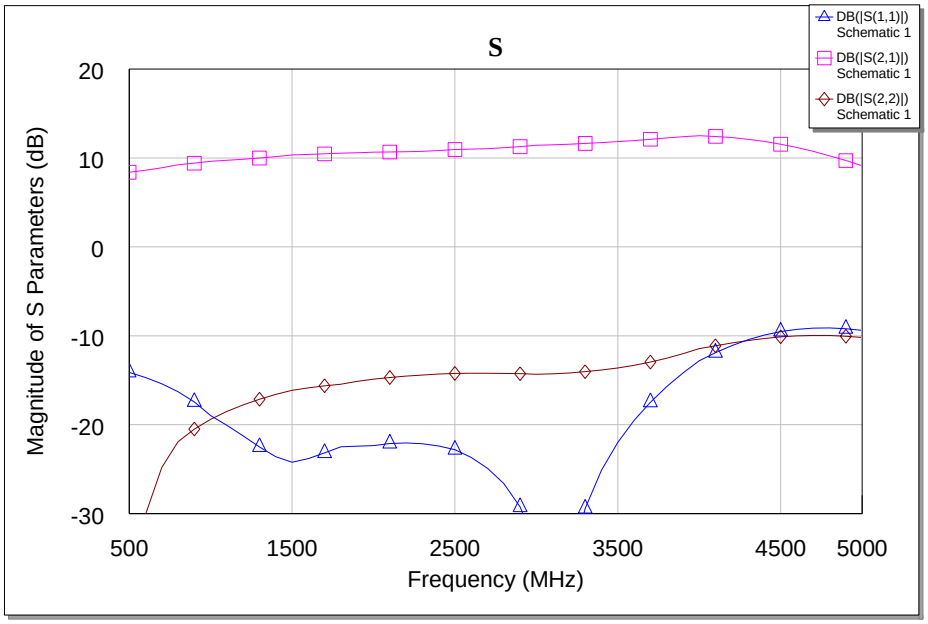

Figure 62 S parameter analysis

When all of the pads, vias and tees are replaced by their EM equivalent and extracted into schematic analysis as subcircuit, lumped elements and transistor are connected to the relevant nodes, final optimization is run with the same goal at the first stage, and final schematic is formed as it is seen in Figure 63 and Figure 64. The circuit is divided into two parts and given in two figures for clarity.

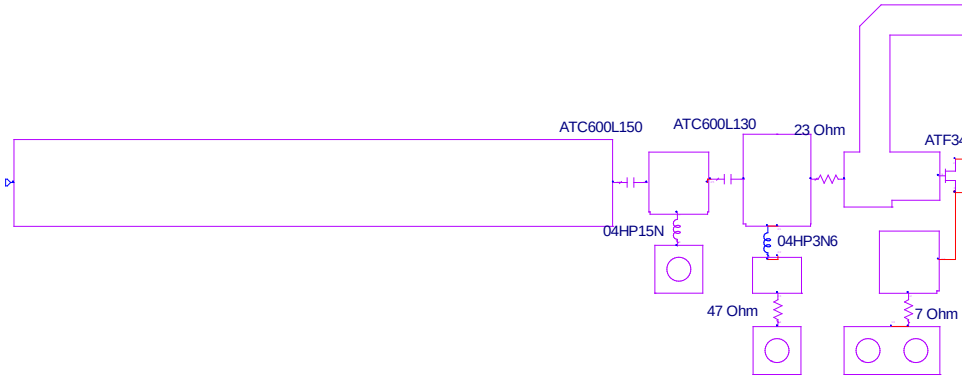

Figure 63 Input side of the second stage

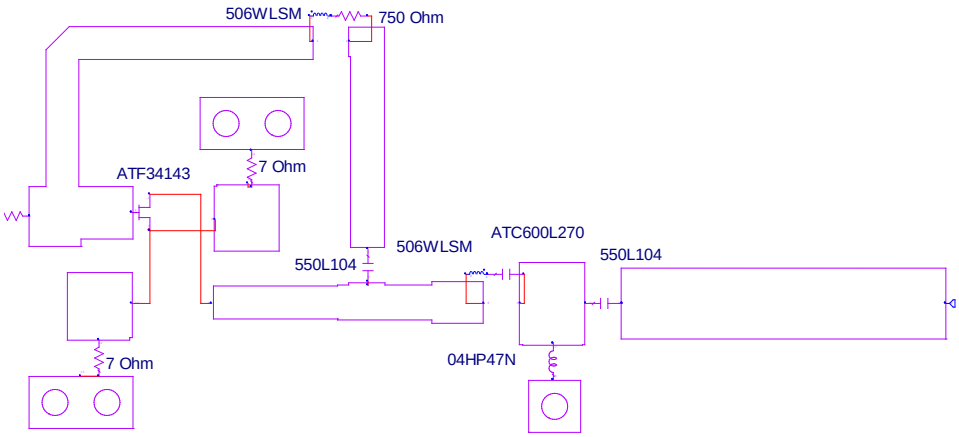

Figure 64 Output side of the second stage

After the optimization of whole circuit, all capacitors and inductors are replaced with their S parameters models. Resistors do not need to be replaced by their models at these frequencies, so that they are left as ideal resistors. It is also

important that, for final analysis, S parameters of DC blocks and conical inductors are used in the appropriate nodes, which would increase the accuracy of the simulation.

EM simulations are run using 0.04 mm grid size, which results in a simulation time that can be considered as fast and accurate. After all of the simulations are completed with satisfactory results, simulation is run again with 0.01 mm mesh size, and no considerable change is observed.

Some meshing examples are given in Figure 65. Again, grids become dense at the points of discontinuity.

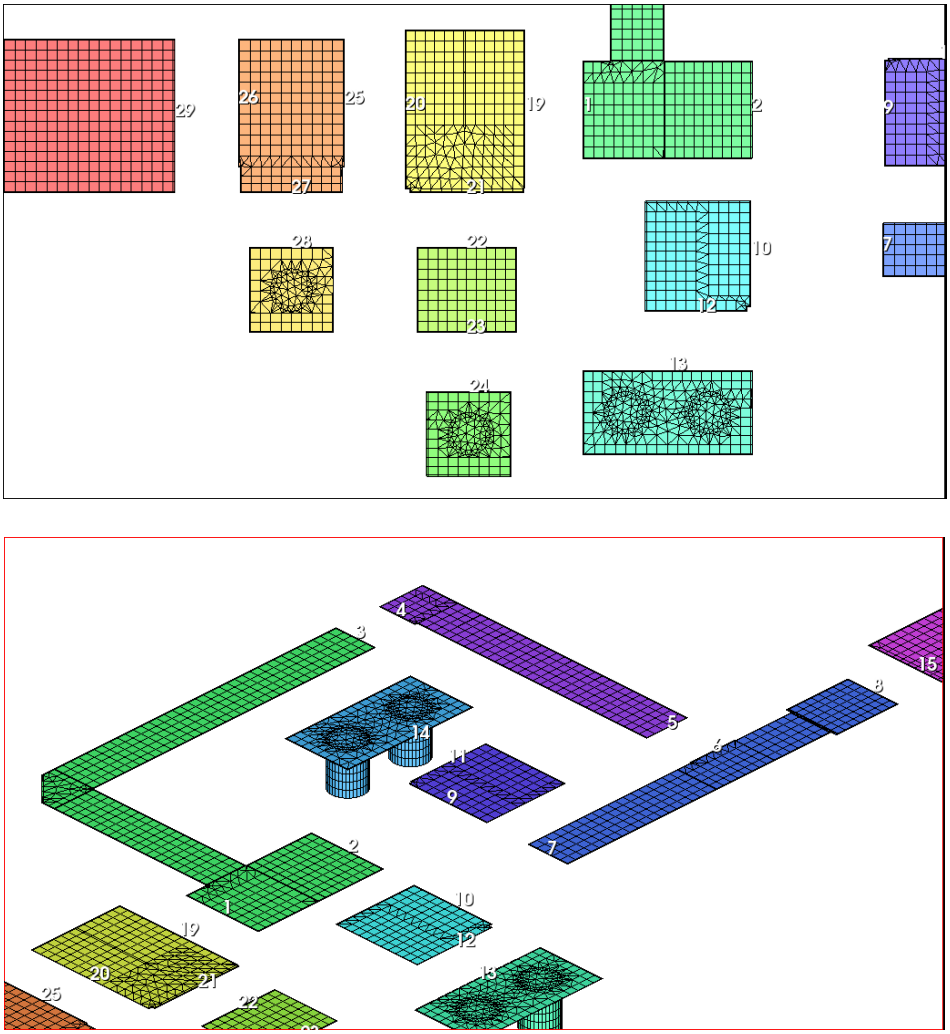

Figure 65 Some meshing examples of second stage

After completing the final optimization, the final design gives the S_{21} result that is shown in Figure 66.

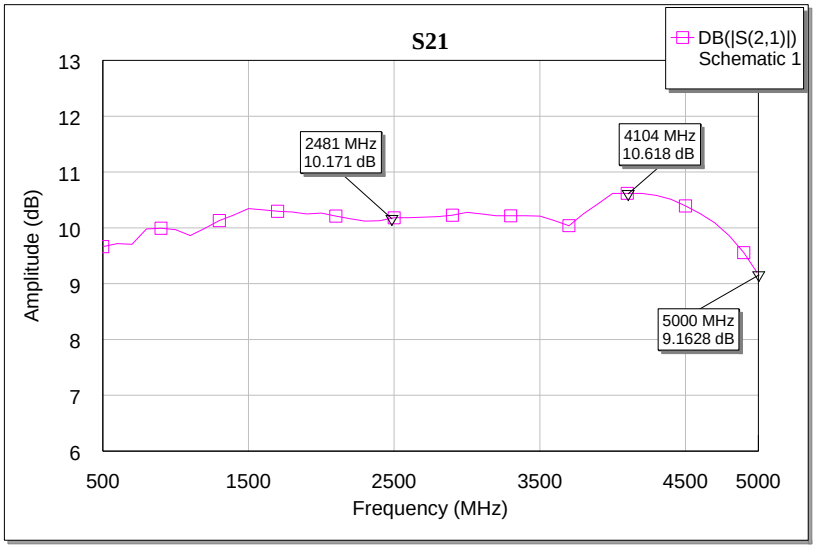

Figure 66 Gain analysis of second stage

According to the S_{21} analysis, gain varies between nearly 10.6 dB to 9.1 dB over full band. It is close to 10 dB for most of the bandwidth. Return loss analysis of final design is shown in Figure 67.

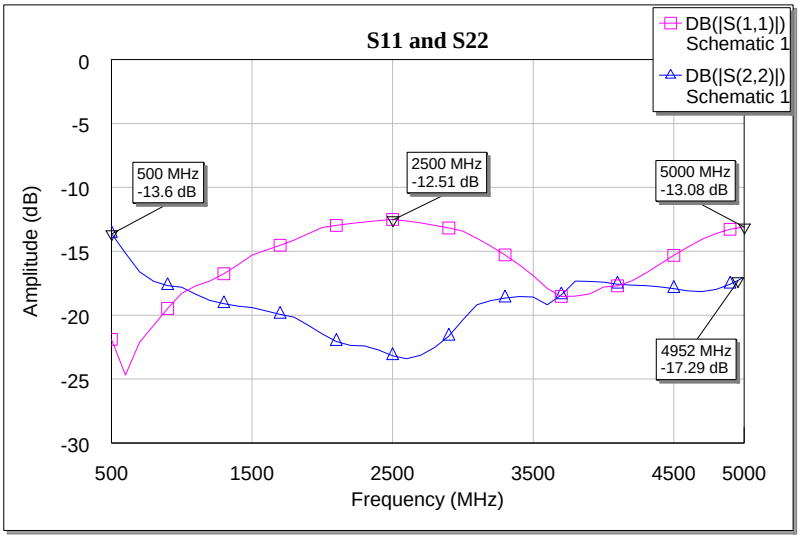

Figure 67 Return loss analysis of second stage

According to the simulation, maximum level of S_{22} and S_{11} is -12.5 dB and -13.6 dB respectively, and they are generally below -15 dB over the full band, which is satisfactory.

Stability analysis is shown in Figure 68.

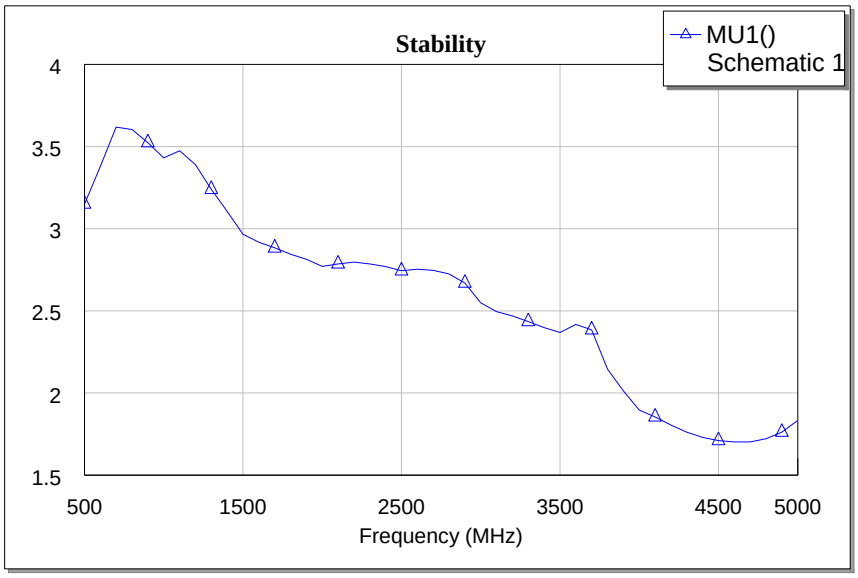

Figure 68 Stability analysis of second stage

According to the stability simulation, since μ parameter is greater than 1 for full band, designed amplifier is unconditionally stable.

After design of the second stage, these amplifiers can be cascaded and final cascaded feedback amplifier circuit may be formed.

3.2.10. Design of the Cascaded Feedback Amplifier

Since input and output of both stages are matched to 50 ohms, designed amplifiers can be cascaded easily without any need of interstage matching. First and second stages that contain their EM structure data are cascaded as seen in Figure 69.

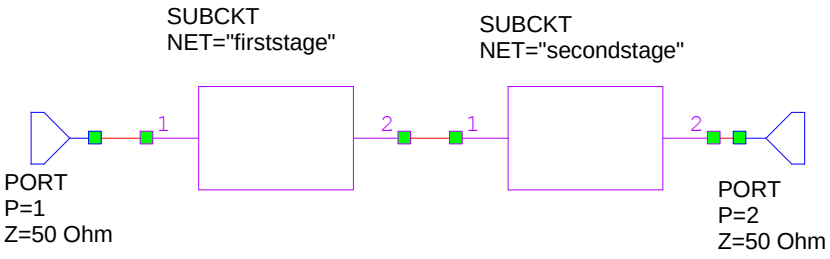

Figure 69 Cascading the first and second stage

Gain simulation of the cascaded feedback amplifier schematic including EM structure is given in Figure 70.

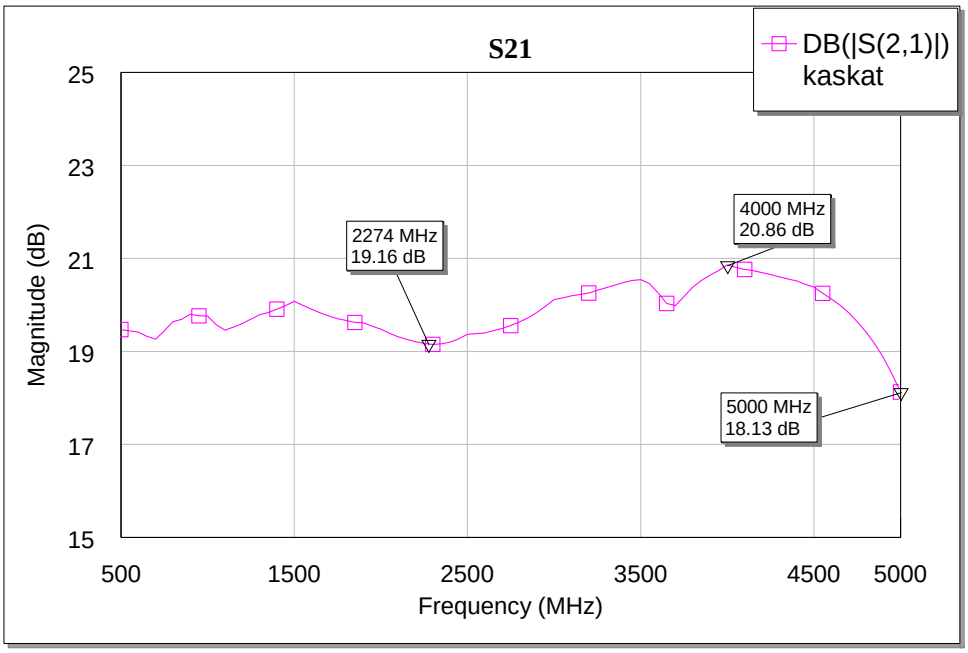

Figure 70 Gain analysis of cascaded feedback amplifier

According to the gain analysis, S_{21} changes between 20.8 dB and 18.1 dB, which is considered as satisfactory.

Return loss analysis of cascaded feedback amplifier is given in Figure 71.

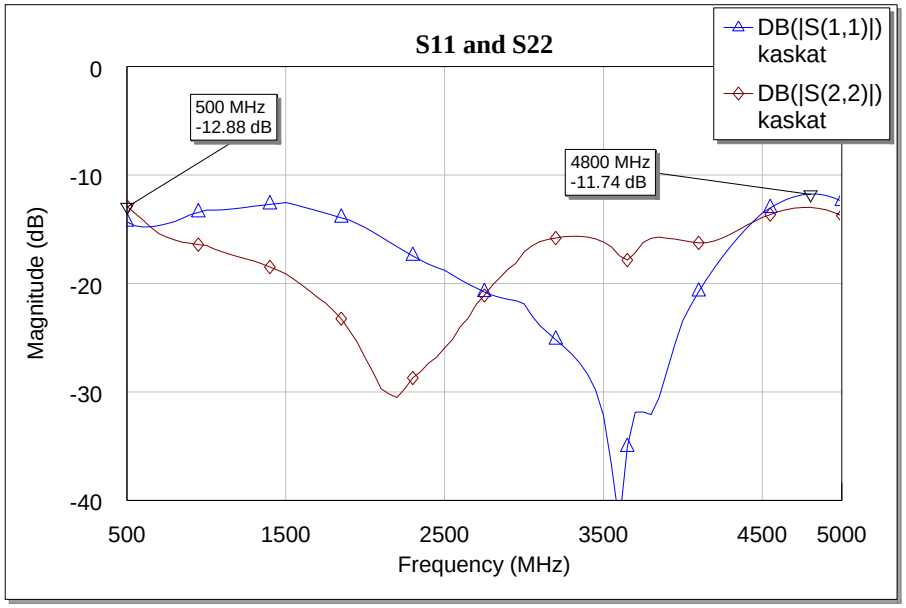

Figure 71 Return loss analysis of cascaded feedback amplifier

According to the return loss analysis, S_{11} and S_{22} have maximum points of -12.8 dB and -11.7 dB. At most of the bandwidth, they are below -15 dB, which is quite good. Stability analysis is shown in Figure 72.

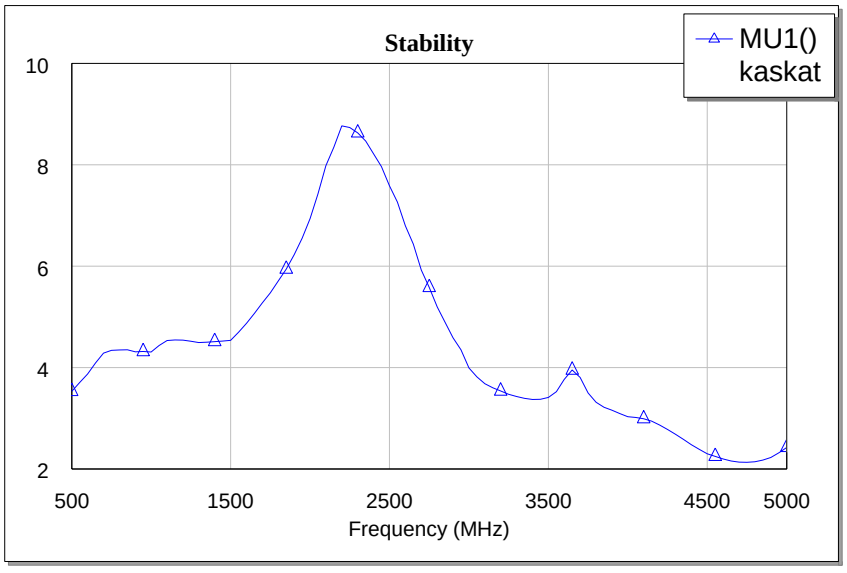

Figure 72 Stability analysis of cascaded feedback amplifier

Since μ parameter is greater than 1 at desired bandwidth, design is considered as unconditionally stable.

Since EM analyses are completed successfully, next step is PCB design.

3.2.11. Fabrication of the Cascaded Feedback Amplifier

Since the EM analyses results are satisfactory, transmission lines and pads should be used as is. Layout of the first stage was designed at previous section, so the second stage should be connected to the output of the first stage. Designed layout of the cascaded feedback amplifier circuit is illustrated in Figure 73.

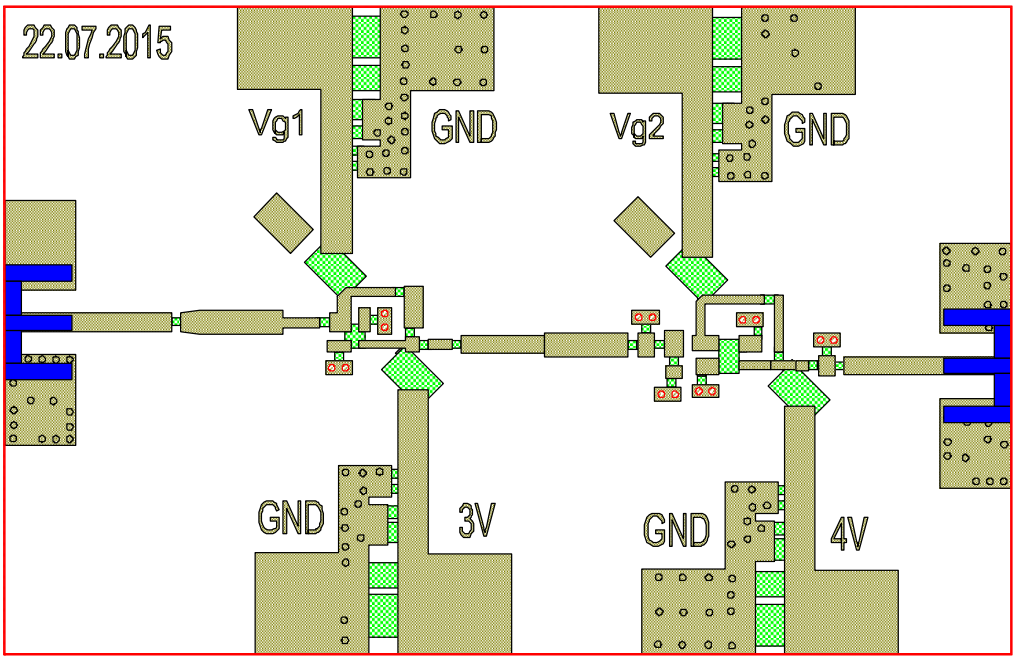

Figure 73 Layout of cascaded feedback amplifier

As in the previous layout design, DC bias traces are designed considering decoupling capacitors of different packages. These traces are deliberately designed to be larger than the size of the chosen conical inductors to ensure that a larger inductor can fit if needed. Also, ground pads are filled with vias in order to

get a proper ground. According to this layout, the fabricated PCB is given in Figure 74.

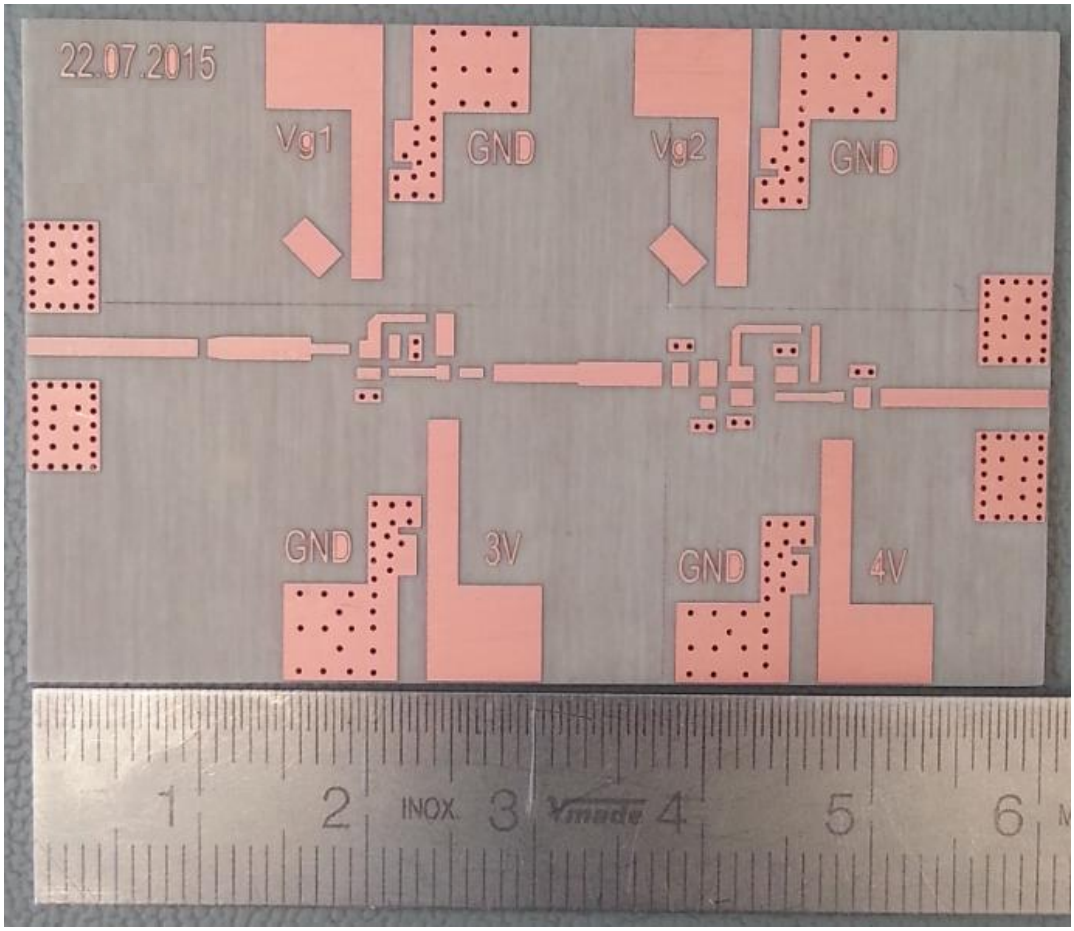

Figure 74 PCB of designed cascaded feedback amplifier

The PCB is 6 cm as long and 3.9 cm as wide. Since the height of the PCB is 20 mils which is very thin, a metal plate is soldered to the bottom of the PCB to increase its mechanical strength, so that, unwanted accidents such as breaking the PCB while using torque wrench to connect the SMA connectors are avoided.

After mounting the SMD components, decoupling capacitors, SMA connectors and DC terminals, final form of the PCB is given in Figure 75.

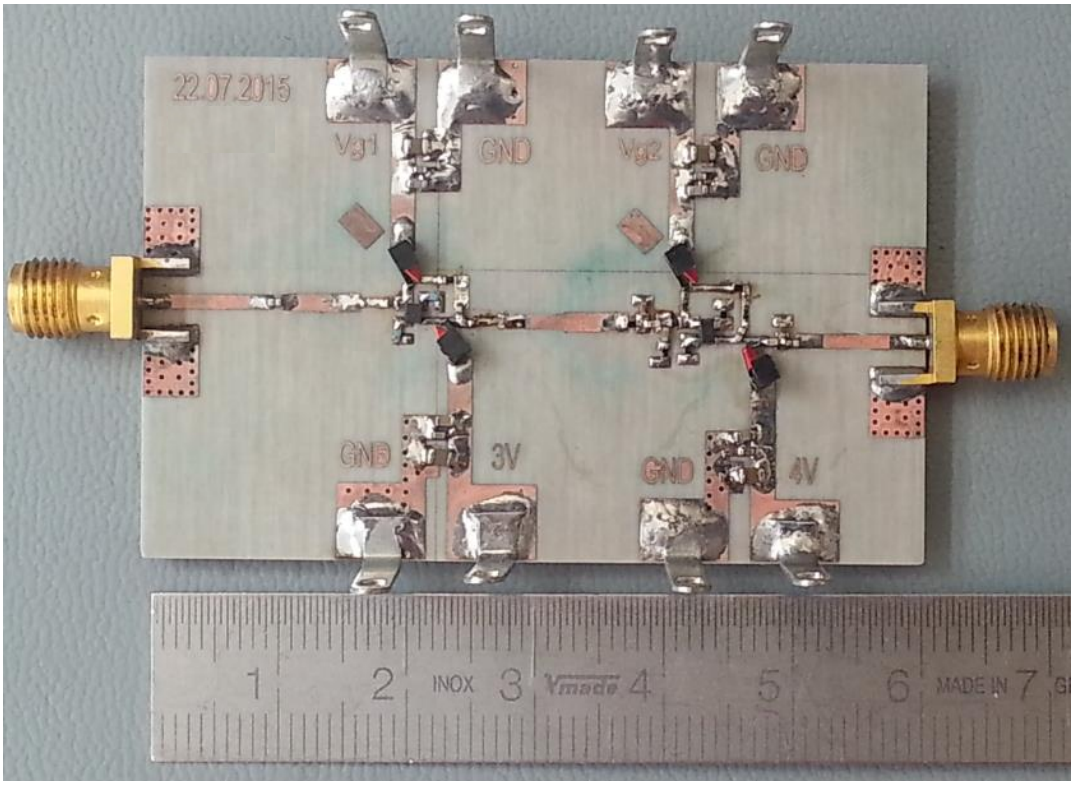

Figure 75 Assembled cascaded feedback amplifier

3.2.12. Measurement of the Cascaded Feedback Amplifier

Bias point of the first stage is known from the first trial. Drain of the second stage is connected to 4V, and gate is connected to -0.5V using DC voltage sources. Since there are feedback elements at the source of the second stage, similarly in the first stage, gate voltage should be changed observing the drain current. 60 mA which is the current of the used S parameter data file is seen at -0.2V gate current. Finally, second stage is biased and cascaded feedback amplifier is ready for S parameters measurement.

After making two-port calibration, cascaded feedback amplifier is connected to network analyzer and S parameters results are given in Figure 76.

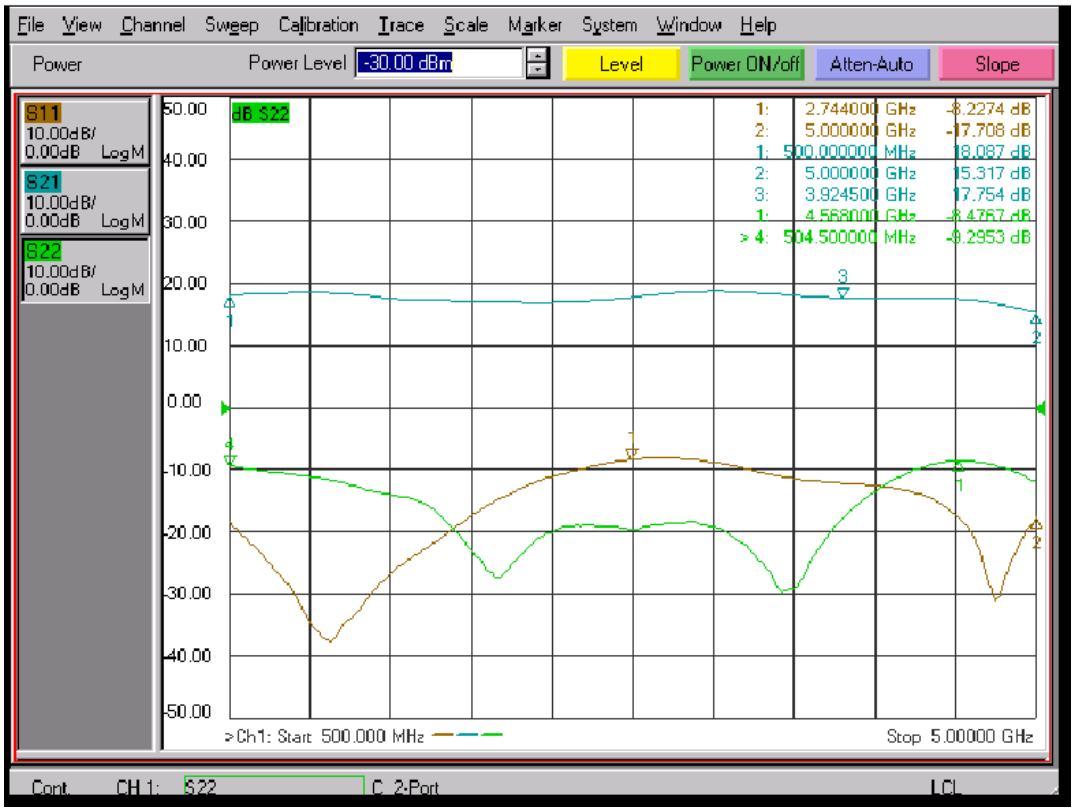

Figure 76 S-parameters Measurement of Cascaded Feedback Amplifier

The measurement results show that the designed cascaded feedback amplifier is quite satisfactory. It has a flat gain around 17.1 dB between 0.5-5 GHz. Maximum and minimum gain values are 18.9 dB and 15.3 dB respectively. S_{11} parameter is below -15 dB for most of the band, as in the simulations. At 2.744 GHz, S_{11} has its highest value of -8.227 dB. S_{22} parameter is also below -15 dB for most of the band. At 4.558 GHz, S_{22} parameter has its maximum value of -8.4767 dB.

Simulated and measured gain data are given in the same graph in Figure 77.

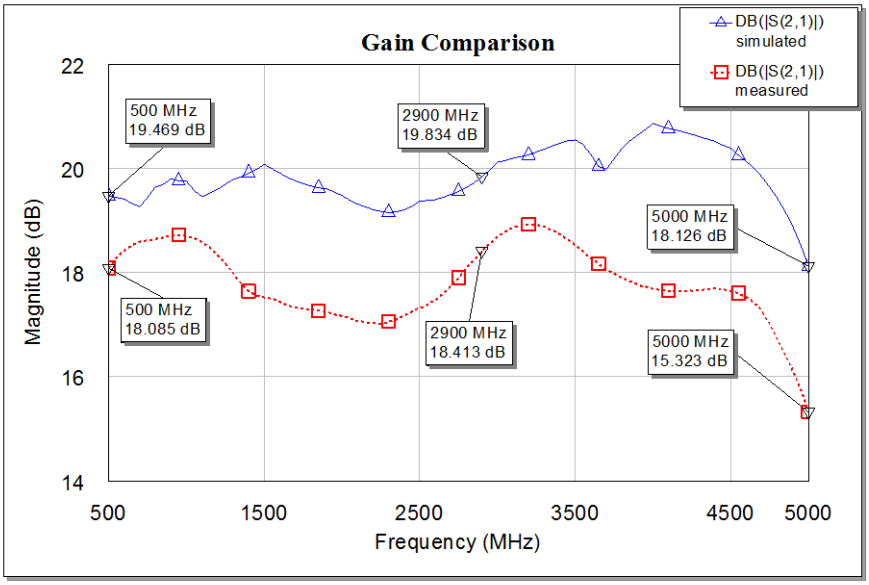

Figure 77 Gain comparison of simulation and measurement

According to the comparison graph, measured data follow the simulated data with nearly 1.5 dB below. The greatest difference, which is nearly 2.8 dB, is at the maximum frequency, as expected.

Return loss comparison of simulated and measured data is given in Figure 78.

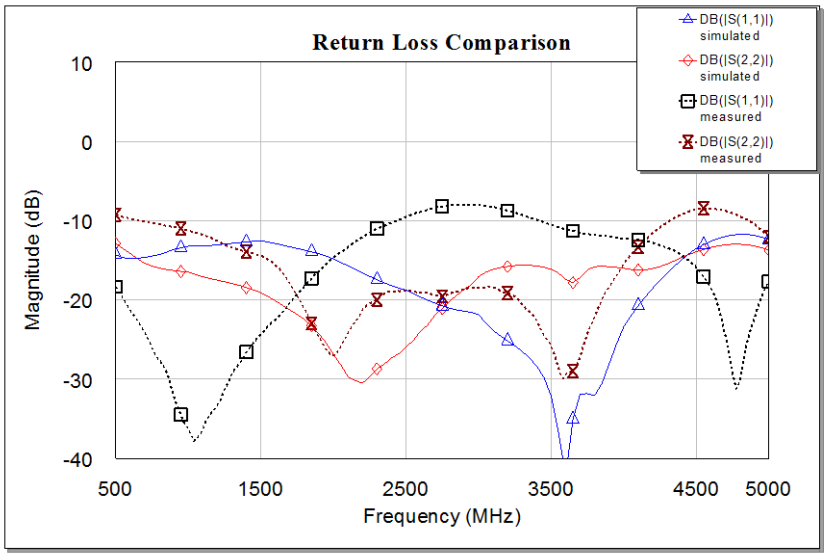

Figure 78 Return loss comparison of simulation and measurement

As it is seen from the compared data, both simulated and measured data are lower than -10 dB over most of the band. Small variations of component values and parasitic elements may cause a big difference between return loss simulation and measurement below -10 dB at these frequencies. So, the difference between measurement and simulation in Figure 78 is acceptable.

These results show that the designed cascaded feedback amplifier has acceptable return loss values with satisfying gain over the decade bandwidth of 0.5-5 GHz. Simulation and measurement results are quite similar. Main causes for the differences between simulation and measurements can be listed as:

- Tolerances of the lumped components
- Tolerances of the active devices
- Effects of the soldering
- Effects of the PCB fabrication

CHAPTER 4

CONCLUSION AND FUTURE STUDIES

In this thesis work, a cascaded feedback amplifier for decade frequency band of 0.5-5 GHz is designed, fabricated and measured. Design process of 2-stage feedback amplifier is explained step by step. In order to achieve a flat gain, feedback topology is used for both transistors.

Needs for today's RF technology are getting increased and changing according to the application. Increased bandwidth is one of these necessities, which comes with various design problems. Wideband amplification is one of the emphasized research areas for microwave systems. Broadband amplification may be achieved using several methods, such as reactive matching, balanced, distributed and feedback methods.

Feedback amplifiers are well-known for achieving wide-band operation, which has advantages and disadvantages as other methods. Feedback amplifiers have satisfying input and output return losses over a wide frequency range. Gain flattening is another important advantage of feedback topology with unconditional stability. For disadvantages, it is well-known that gain of the active device is reduced in order to increase the bandwidth. Besides, noise figure of feedback amplifiers are not low due to the resistive components in the feedback line. Also, applying feedback to a transistor may cause unpleasant results due to some reasons such as undesired couplings between input and output lines. Schematic analysis may mislead the designer in this regard. For this reason, EM analysis would provide more realistic results, which is another aim of this study.

4.1. Summary of Work

In the study, first of all, the first stage is designed using ATF541M4 transistor of Avago Technologies in AWR Design Environment and design process is explained in detail step by step. For a flat gain, resistive negative feedback circuit is applied to transistor at the expense of increase in noise figure. All microstrip lines, tees and pads are replaced with their equivalent EM structure equivalents and final tunings are applied to the design. Gain of the first stage is between 8.9 dB and 10.3 dB, and return losses are better than approximately -14 dB in the simulations. First stage is then fabricated on a 20 mil Rogers 4003 substrate and S parameters are measured using a calibrated Agilent N5230A PNA-L Network Analyzer after setting the appropriate bias point. According to the S parameter measurements, first stage has a flat gain between 9 dB and 6.6 dB. Input return loss is higher than 14 dB approximately for the full band, and also output return loss is higher than 15 dB for most of the band. Gain and return losses decrease as the frequency increases, which is often experienced during an RF amplifier design.

Then, second stage is designed using ATF34143 transistor of Avago Technologies. Again, design steps are given in detail. After satisfactory schematic analyses, all microstrip lines and pads are replaced by their EM structure equivalents and final tunings are applied. According to EM analysis, gain of the first stage varies between 9.15 dB and 10.6 dB for full-band. Input return loss is greater than 12.5 dB, and output return loss is greater than 13 dB. After satisfactory results of second stage design, two stages are cascaded and final design of the cascaded feedback amplifier is formed. Gain of the simulated amplifier varies between 20.86 dB and 18.13 dB. Return losses are greater than 11 dB for full-band, and greater than 15 dB for most of the band. For all simulations, stability of the amplifier is considered. After satisfactory S parameter simulation results, cascaded feedback amplifier is fabricated, assembled and measured using network analyzer. Gain of the fabricated amplifier is between 18.9 dB and 15.3

dB. Maximum input and output return losses are 8.2 and 8.4 dB, respectively, which is quite acceptable. Also, return losses are seen to be higher than 10 dB for most of the 0.5-5 GHz bandwidth. For a final step, input of the cascaded feedback amplifier is terminated with 50 ohm, and output of the amplifier is connected to a spectrum analyzer and frequency band of 10 MHz-18 GHz is observed. No signal is observed at the output of the amplifier down to -80 dB, which means that designed amplifier does not oscillate.

According to final measurements, simulation and demonstrated results are seen to be parallel and satisfactory. Main reasons for the differences between simulations and measurement results are tolerances of the used components, layout and fabrication effects and effects of some components such as SMA connectors that are not modeled in the simulations. All of these effects decrease the gain and return losses, as expected.

4.2. Future Studies

For future work, noise figure of the designed cascaded feedback amplifier may be taken into consideration. If flat gain is achieved without resistive feedback elements, noise figure would be lower. Besides, in order to enhance the input and output return losses, balanced topology may be applied. Furthermore, a metal housing may be considered for the amplifier in order not to be effected by unwanted signals in the environment.

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