ONLINE APPLICATION OF SHEM TO GRID-CONNECTED INVERTERS WITH VARIABLE DC LINK VOLTAGE BY PARTICLE SWARM OPTIMIZATION

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ABSTRACT

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In this thesis, online selective harmonic elimination method (SHEM) has been applied to a voltage source converter (VSC) based grid-connected three-phase two-level inverter with variable DC link input voltage eliminating 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, and 19^{th} harmonics in the output voltage. The switching angles of SHEM are given by a set of nonlinear transcendental equations. Particle swarm optimization (PSO) algorithm is used for the solution of this equation set, and this algorithm is implemented in the field-programmable gate array (FPGA) for a fast and online calculation of switching angles in real time without using a lookup table. FPGA is used as the main and sole controller in the implemented voltage source inverter (VSI) to provide gating signals for IGBTs.

In applications where input DC link voltage varies in a wide range, usage of lookup table for switching angle sets might be disadvantageous due to discretization of modulation index values, large lookup table storage, and infeasible region

of solution space, which are investigated in detail in the thesis, with explanatory examples. The effects of PSO algorithm parameters on searching performance are also elaborated. FPGA implementation of PSO algorithm for solution of SHEM equation sets is described in detail. A 1.6 kVA, 380 V, three-phase VSI is successfully implemented and tested in the laboratory. Hardware co-simulation, computer simulation, and experimental results have shown that SHEM can be successfully applied online for the control of grid-connected inverters.

Keywords: Online Selective Harmonic Elimination Method (SHEM), Grid Connected Inverter, Variable DC Link Voltage, Particle Swarm Optimization (PSO), Field-Programmable Gate Array (FPGA)

ÖZ

ŞEBEKEYE BAĞLI DEĞİŞKEN DA BAĞ GERİLİMLİ EVİRGEÇLERE
PARÇACIK SÜRÜ OPTİMİZASYONU İLE
ÇEVRİMİÇİ SHEM UYGULANMASI

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Bu tez çalışmasında, çevrimiçi seçici harmonik eliminasyon metodu (SHEM) gerilim kaynaklı çevirgeç (GKÇ) temelli, şebekeye bağlı ve değişken DA bağ giriş gerilimine sahip üç faz iki seviyeli evirgece uygulanmış ve evirgecin çıkış gerilimindeki 5., 7., 11., 13., 17. ve 19. harmonikler yok edilmiştir. SHEM anahtarlama açıları lineer olmayan transandantal denklemler halinde ifade edilir. Parçacık sürü optimizasyonu (PSO) algoritması bu denklem kümesinin çözümü için kullanılmış ve bu algoritma, anahtarlama açılarının hızlı ve çevrimiçi bir şekilde gerçek zamanlı olarak başvuru tablosu kullanılmadan hesaplanabilmesi için alanda programlanabilir kapı dizisinde (FPGA) uygulanmıştır. FPGA, uygulanmış olan gerilim kaynaklı evirgeçteki IGBT'lerin anahtarlama sinyallerinin sağlanması için ana ve tek kontrolcü olarak kullanılmıştır.

Giriş DA bağ geriliminin geniş bir aralıkta değiştiği uygulamalarda, anahtar-

lama açısı kümeleri için başvuru tablolarının kullanılması, modülasyon indeksi değerlerinin ayrıklaştırılması, büyük başvuru tablolarının depolanması ve çözüm uzayının uygulanamaz bölgesi nedeniyle elverişsiz olabilir. Bu tezde bu nedenler açıklayıcı örneklerle birlikte detaylı olarak incelenmiştir. PSO algoritmasının değişkenlerinin arama performansı üzerindeki etkileri de ayrıca ayrıntılandırılmıştır. SHEM denklem kümelerinin çözümü için PSO algoritmasının FPGA üzerinde uygulanması detaylı olarak açıklanmıştır. 1.6 kVA, 380 V, üç faz gerilim kaynaklı bir evirgeç başarıyla gerçekleştirilmiş ve laboratuvar ortamında test edilmiştir. Donanımla birlikte simülasyon sonuçları, bilgisayar simülasyonu sonuçları ve deney sonuçları SHEM'in çevrimiçi olarak şebekeye bağlı evirgeçlerin kontrolü için başarıyla uygulanabileceğini göstermektedir.

Anahtar Kelimeler: Çevrimiçi Seçici Harmonik Eliminasyon Metodu (SHEM), Şebekeye Bağlı Evirgeç, Değişken DA Bağ Gerilimi, Parçacık Sürü Optimizasyonu (PSO), Alanda Programlanabilir Kapı Dizisi (FPGA)

To my family

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TABLE OF CONTENTS

LIST OF TABLES

TABLES

LIST OF FIGURES

FIGURES

NOMENCLATURE

α_k	Switching Angle
β	Inertia Weight
δ	Load Angle
γ	Modulation Index Penalty
μ	Angle Constraint Penalty
ω	Grid Frequency
ω_{ff}	Feed-forward Component of the Grid Frequency
$\omega t_{a,\,b,\,c}$	PLL Information of the Grid Voltage
φ	Sum of Cognition and Social Factors
θ	Phase Angle
C	LCL Filter Capacitance
c_1	Cognition Factor
c_2	Social Factor
C_{dc}	DC Link Capacitance
d	Dimension of the Problem Space
D	Reverse Diode of Switching Semiconductor
f	Fitness Value of the Particle
f_1	Frequency of the Fundamental Component
f_c	Converter Switching Frequency
f_{res}	LCL Filter Resonant Frequency
$gbest_i$	Global Best Fitness of the i^{th} Particle
I	RMS Current From Inverter to Grid
$i_{a,\,b,\,c}$	Grid Current
I_{dc}	DC Link Current
i_{L1}	Inverter-Side LCL Filter Current
i_{L2}	Grid-Side LCL Filter Current
i_{ph}	Photo-Current Source
K	Constriction Factor

k_i	Integral Constant of PI Control
k_p	Proportional Constant of PI Control
L_1	Inverter-Side LCL Filter Inductance
L_2	Grid-Side LCL Filter Inductance
M	Modulation Index
$pbest_i$	Personal Best Fitness of the i^{th} Particle
P_G	Grid-Side Active Power
P_I	Inverter-Side Active Power
P_{in}	Inverter Input Active Power
P_{out}	Inverter Output Reactive Power
Q_G	Grid-Side Reactive Power
Q_I	Inverter-Side Reactive Power
Q_{out}	Inverter Output Reactive Power
R	Total Reactor Loss Resistance
$rand$	Random Number
R_p	PV Cell Shunt Resistance
R_s	PV Cell Series Resistance
s	Swarm Size
t	Time Frame
T	Switching Semiconductor
T_{igbt}	Temperature of the IGBT
$U_{max}1$	Highest Permanent Catenary Voltage
$U_{max}2$	Highest Non-Permanent Catenary Voltage
$U_{max}3$	Highest Long-Term Catenary Overvoltage
$V_{\alpha,\beta}$	α and β Component of the Voltage
$v_{a,b,c}$	Grid Voltage
v_{AB}	Inverter Line-to-Line Output Voltage
v_{An}	Inverter Midpoint Output Voltage for Leg A
V_{CE}	IGBT Collector-Emitter Voltage
V_{dc}	DC Link Voltage
$V_{d,q}$	D and Q Component of the Voltage
$\hat{V_f}$	Peak Value of the Fundamental Line-to-Neutral Inverter Output Voltage
v_i	Velocity of the i^{th} Particle

V_I	Line-to-Neutral Inverter RMS Voltage
V_G	Line-to-Neutral Grid RMS Voltage
V_{max}	Maximum Velocity
$V_{rms,l-l}$	Line-to-Line RMS Voltage
$V_{rms,l-n}$	Line-to-Neutral RMS Voltage
X	Reactor Reactance
x_i	Position of the i^{th} Particle
X_{max}	Dynamic Range of the Particle

LIST OF ABBREVIATIONS

AC	Alternating Current
ADC	Analog-to-Digital Converter
ANN	Artificial Neural Network
CMT	Clock Management Tile
CSI	Current Source Inverter
DAC	Digital-to-Analog Converter
DC	Direct Current
DFF	D Flip Flop
DLL	Delay Locked Loop
DSP	Digital Signal Processor
FFT	Fast Fourier Transform
FIR	Finite Impulse Response
FPGA	Field-Programmable Gate Array
GA	Genetic Algorithm
GUI	Graphical User Interface
HDL	Hardware Description Language
IGBT	Insulated-Gate Bipolar Transistor
I/O	Input/Output
JTAG	Joint Test Action Group
LFSR	Linear Feedback Shift Register
LUT	Lookup Table
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MPPT	Maximum Power Point Tracking
MULT	Multiplier
PCB	Printed Circuit Board
PI	Proportional-Integral
PLL	Phase Locked Loop
PRNG	Pseudo Random Number Generator

PSO	Particle Swarm Optimization
p.u.	Per-Unit
PV	Photovoltaic
PWM	Pulse-Width Modulation
RAM	Random Access Memory
RMS	Root Mean Square
SHEM	Selective Harmonic Elimination Method
SiC	Silicon Carbide
SPI	Serial Peripheral Interface
STATCOM	Static Synchronous Compensator
TDD	Total Demand Distortion
THD	Total Harmonic Distortion
TLL	Three-Phase Line-to-Line
TLN	Three-Phase Line-to-Neutral
TRNG	True Random Number Generator
UPS	Uninterruptible Power Supply
VHDL	VHSIC HDL
VHSIC	Very High Speed Integrated Circuit
VLSI	Very Large Scale Integrated
VSC	Voltage Source Converter
VSI	Voltage Source Inverter

CHAPTER 1

INTRODUCTION

1.1 Overview

It is a basic fact that the human civilization is living in an era in which energy resources are regarded as the most important asset of the planet. The need for finding energy resources in order to compensate the ever-increasing energy consumption of people has driven several nations to seek new and alternative ways of supplying energy for their industry and household, especially in the 21^{st} century.

Fossil fuels have been the primary source of energy until the end of last century. Over 79 % of the primary resources of energy consumed in the world consists of fossil fuels. 57.7 % of this amount is utilized for the transportation sector, which is rapidly decreasing. It is predicted that the fossil-based oil, coal, and gas reserves will run out in the next ten decades by the World Energy Forum [1]. It has become a must to utilize alternative energy resources for highly efficient energy conversion with low emission due to concerns about increasing oil prices, fossil fuel deficit, global warming, and damages to environment and ecosystem [2]. Worldwide renewable energy resources other than hydroelectric energy has exceeded 480 gigawatts by 2012 due to the growth in their installed capacity. This generation of power compensates 5.2 % of the worldwide electricity consumption, and half of the newly installed generation capacity consists of this power [3].

Although the focus for supplying energy in more efficient ways has been on the

resource side recently, the conversion of energy resources to electrical energy, which is injected into the power grid to be used by industry and household, highly depends on the efficiency of the power converter. Implementing a robust and stable power converter is very essential for increasing the cumulative efficiency of the system. Energy resources have fluctuated and unpredicted features, which is not preferable for power grid operators. Therefore, power electronics has an important role for obtaining more controllable and robust energy production and reducing system costs. Moreover, more advanced control methods and configurations for power electronic converters are needed due to new challenges and considerations in alternative energy conversion [4].

Along with the demands of renewable energy resources, their conversion and distribution to the power grid, power converters also play an essential role in driving motors. Several topologies and control methods have been investigated in the literature to build efficient motor drives, and the research for developing the conversion process always continues. With the advance of new generation of semiconductors such as Trench 4 insulated-gate bipolar transistors (IGBTs), long lifetime, high reliability, high operating temperatures, and reduced switching losses can be achieved [5]. Silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) and diodes are examples of other new semiconductor families, with which it is possible to design and implement high density power modules operating with low switching losses at high junction temperatures [6]. These new generation of semiconductors contribute to the desire for low switching power losses in power converters in a revolutionary way.

The control of power converters has become more important and interesting due to emerging microcontroller technologies. The ever-increasing computing power and speed of microcontrollers enables engineers to implement algorithms in real time easily, which was once recognized as impossible due to complexity and high computing power demand of algorithms in the past. By utilizing the features of fast and powerful microcontrollers such as field-programmable gate arrays (FPGAs), one can apply various control methods to implement efficient, robust, dynamic, and reliable conversion process, which will bring about new possibilities and horizons for power electronics and alter its history.

1.2 Switch-Mode Inverters

Inverters are basically DC-to-AC converters and widely used for variable-speed AC motor drives, uninterruptible power supplies, induction heating, and many other industrial applications. DC sources such as batteries, solar cells, or fuel cells can be inputs to inverters, and the duty of the inverter is to convert this DC input voltage to a symmetric AC output voltage with specified magnitude and frequency. Although the output voltage waveform of an inverter should be sinusoidal ideally, it is non-sinusoidal due to certain harmonics caused by the switching action of semiconductors in practice. Low and medium power applications can be implemented with square-wave or quasi-square-wave voltages, but high power applications require lowly-distorted sinusoidal voltages. By utilizing high-speed power semiconductor devices and several advanced switching techniques, the harmonic contents of the non-sinusoidal output voltage can be minimized or reduced considerably [7].

Inverters can be classified according to different features. When classified by the number of phases, single-phase inverters and three-phase inverters are the two main categories. In general, pulse-width-modulation (PWM) control signals are used to generate AC output voltage; however, there are many other switching methods in the literature. Inverters are called as voltage source inverter (VSI) if their input is a DC voltage source, or current source inverter (CSI) if their input is a DC current source [8].

The VSIs can be categorized into three general categories:

- *Pulse-width-modulated inverters:* For these inverters, the AC output voltage magnitude and frequency is controlled by the inverter by utilizing PWM for semiconductor switches since the input DC voltage is constant in magnitude.
- *Square-wave inverters:* For these inverters, the AC output voltage magnitude is controlled by altering the input DC voltage. The frequency of the output voltage is determined by the inverter control method, and the output voltage has square-wave waveform.

- *Single-phase inverters with voltage cancellation:* If the inverter is single-phase inverter, the output voltage magnitude and frequency can be controlled with voltage cancellation method although the input DC voltage is constant, and the switching technique is not PWM. These inverters have the properties of the previous two inverters; however, their utilization area is not as wide as others [8].

Figure 1.1 summarizes the classification of the inverters. In some applications, which will be discussed in the next chapter, the input DC link voltage to the inverter is variable throughout the course of operation, and this requires a dynamic control approach for the switches in the inverter if the output harmonic content is desired to be low. Several control methods have been investigated in the literature and implemented in the industry, and one of these methods, which is selective harmonic elimination method, will be introduced in the next section.

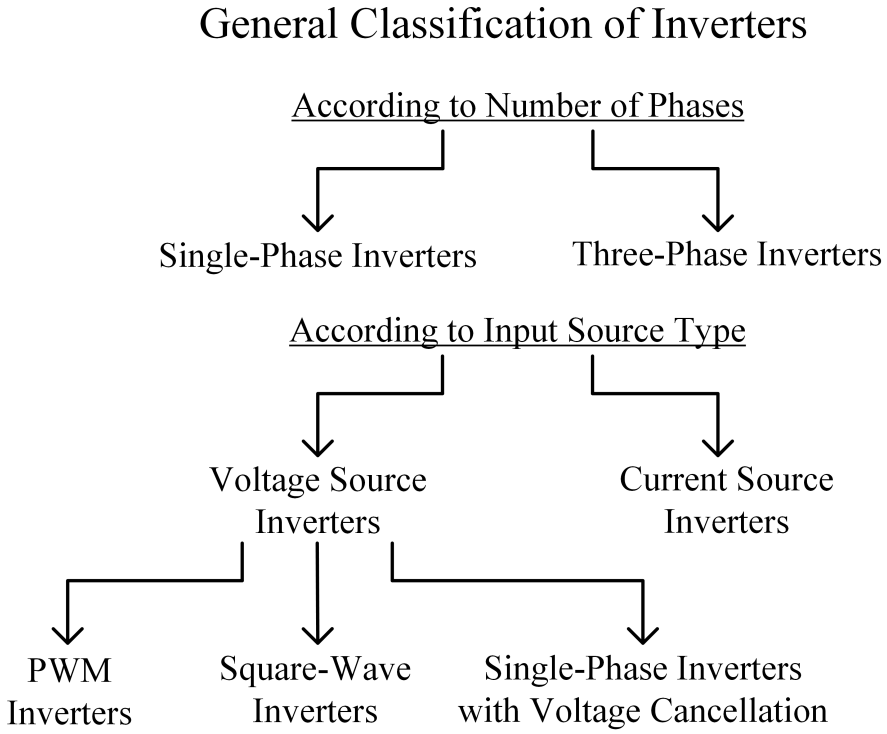


Figure 1.1: General Classification of Inverters

1.3 Selective Harmonic Elimination Method

1.3.1 Application Areas

Selective harmonic elimination method (SHEM) combines square-wave switching and PWM switching to control the fundamental output voltage. Moreover, it is possible to eliminate specific harmonics in the output voltage of the inverter via selection of specific notch angles in the switching pattern of the semiconductors. Each notch in a half-cycle provides one degree of freedom so that one notch is used for the control of fundamental, and the others are used for cancelling the undesirable lower-order harmonics. The higher-order harmonics can be filtered by a small filter. By utilizing very large scale integrated (VLSI) circuits and microcontrollers, SHEM can be implemented for inverters without making the switching frequency and switching losses very high. Figure 1.2 shows an example application of SHEM to a two-level VSI in order to control the fundamental and eliminate two harmonics [8].

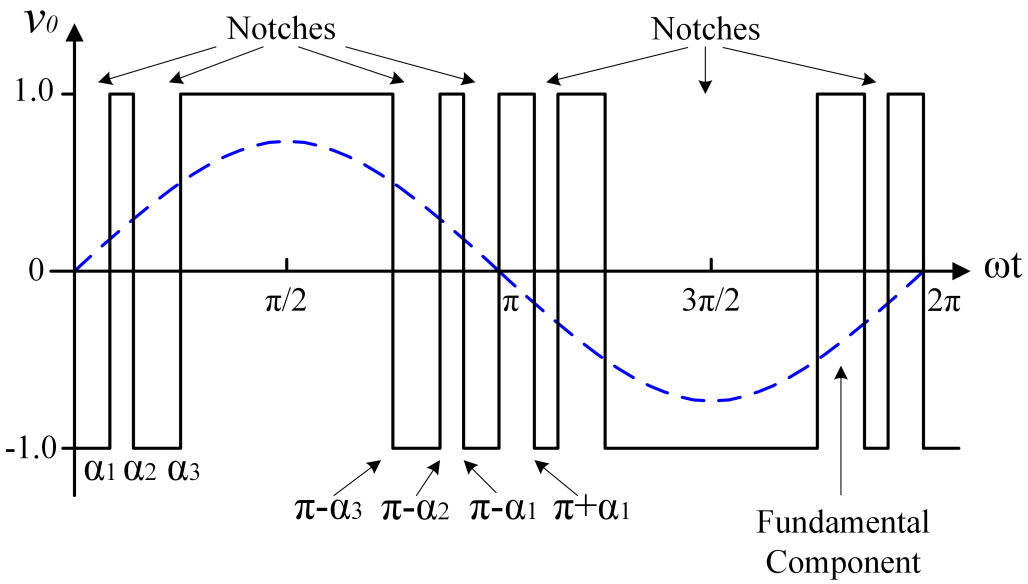


Figure 1.2: Application of SHEM to Two-Level VSI

The use of two-level inverters is disadvantageous due to high switching losses at high switching frequencies for high-power and high-voltage applications. There-

fore, switching semiconductor devices should be used with series or parallel combinations to handle high voltages and currents. Multilevel inverters are found to be effective for high-power high-voltage applications since the power rating can be increased by increasing the number of voltage levels and thereby using switching semiconductors with lower voltage ratings. By this way, higher output voltage levels can be reached with lower harmonic content without use of transformers between the inverter and the grid. Figure 1.3 depicts the typical output voltage of a nine-level multilevel inverter [7].

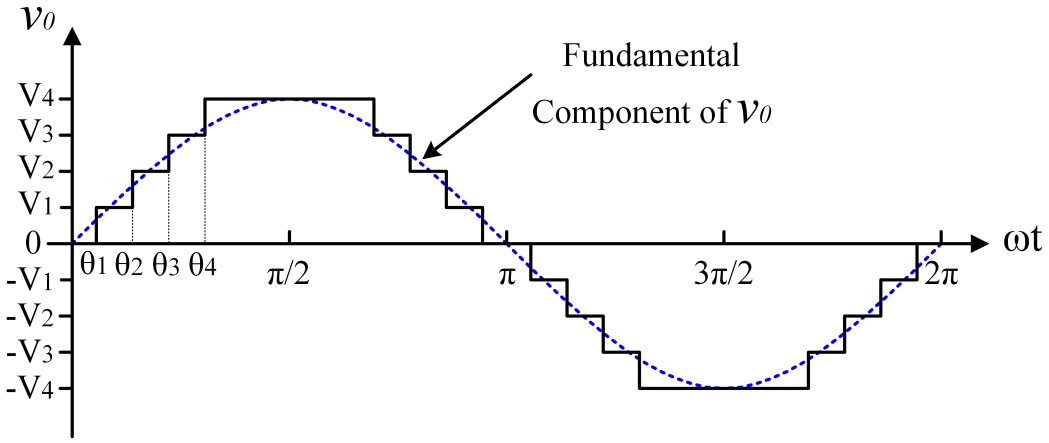


Figure 1.3: Output Voltage of Nine-Level Multilevel Inverter

SHEM can also be applied to multilevel inverters. As can be seen from Figure 1.3, the selection of switching angles, θ_1, θ_2, θ_3, θ_4, affects the shape of the output voltage waveform. Moreover, the magnitudes of fundamental output voltage and harmonics in this waveform can be controlled by selecting the switching angles deliberately, which makes it possible to eliminate lower-order harmonics just as in the case of selecting notch angles for two-level inverters. As the number of voltage levels increases, more switching angles and, in turn, more degrees of freedom are acquired so that more harmonics can be eliminated. By this way, filtering requirements in the output connection are reduced considerably.

Both two-level and multilevel inverter topologies have been implemented in a wide range of applications in the industry. Reactive power control in utility sys-

tems is an example of these applications. An inverter can generate a controlled reactive current and operate as a static synchronous compensator (STATCOM) in the steady-state. By this way, it can either generate or consume reactive power from the grid according to the demands of the grid operator. The harmonic content in the inverter output can be reduced with SHEM; thus, the efficiency of the system can be improved [7]. In [9], a two-level three-leg voltage-source converter (VSC) was designed and implemented for a medium-size distribution-type STATCOM application. 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, 19^{th}, 23^{rd}, and 25^{th} harmonics in the output voltage are eliminated by SHEM. Another STATCOM application with SHEM has been presented in [10]. In this research, a 154-kV ±50-MVAr transmission STATCOM was designed and implemented to realize compensation of reactive power, regulation of terminal voltage, and stability of power system. The implementation includes five 10.5-kV ±12-MVAr cascaded multilevel converter modules with five series-connected H-bridges in each phase for each module operating in parallel. SHEM technique is utilized to determine five switching angles which eliminate 5^{th}, 7^{th}, 11^{th}, and 13^{th} harmonics by keeping the harmonic distortion of the line-to-neutral output voltage at minimum. Therefore, there is no need to utilize a larger series filter reactor at the output.

1.3.2 Algorithms Used for SHEM Equations

In both cases of two-level inverter and multilevel inverter, it is necessary to solve a set of nonlinear equations in order to find the switching angles of SHEM. These equations consist of mainly sinusoidal terms, and the number of equations in the set equals the number of switching angles. Although using more switching angles eliminates more harmonics, the complexity of the problem increases as the number of switching angles increases, and finding the solution set becomes very hard via conventional methods. In order to solve this set of nonlinear equations, there has been two general groups of techniques presented in the literature.

The first group includes iterative methods such as Newton-Raphson method. Iterative methods are affected by the choice of initial points in general, and divergence of the algorithm is possible. Although Newton-Raphson method is

fast, it can only find one solution set [11]. In [12], the roots of the equation set is found by using MATLAB function *fsolve*, which relies on a Gauss-Newton method with a mixed quadratic and cubic line search method. Homotopy algorithm is another approach, applied in [13–16]. The authors in [17–20] proposed other iterative numerical techniques whereas in [21], the Walsh function-based analytical technique is adopted. In [22] and [23], theories of resultants and of symmetric polynomials were used to characterize the existence of solutions for each modulation index value and then to solve polynomial equations obtained from transcendental equations. Modulation index is defined as the ratio of the output voltage to the input voltage of the converter multiplied by a constant. For some infeasible modulation index values, SHEM equations does not have a solution set. The iterative methods do not offer optimum solutions for infeasible modulation index values, which may be problematic for implementations working for a continuous range of modulation index values.

The second group takes the selective harmonic elimination problem as an optimization problem, and the solution is sought with evolutionary search algorithms. Evolutionary search algorithms have been found to be effective in solving various problems in industry in recent years. These algorithms allow the solution of the problem to be found more easily than analytical methods, and in some cases, where the analytical methods cannot be applied, they are the only way to reach a feasible solution. These algorithms can find the global optimum solution if certain harmonics can be completely eliminated, or they can offer optimum notch angles if a feasible solution cannot be found. Some of the notable evolutionary search algorithms applied to the problem include genetic algorithm (GA) [24–26], particle swarm optimization (PSO) [11, 27, 28], ant colony optimization [29], bee algorithm [30], and bacterial foraging algorithm [31]. Figure 1.4 below summarizes the algorithms used for solution of SHEM equations.

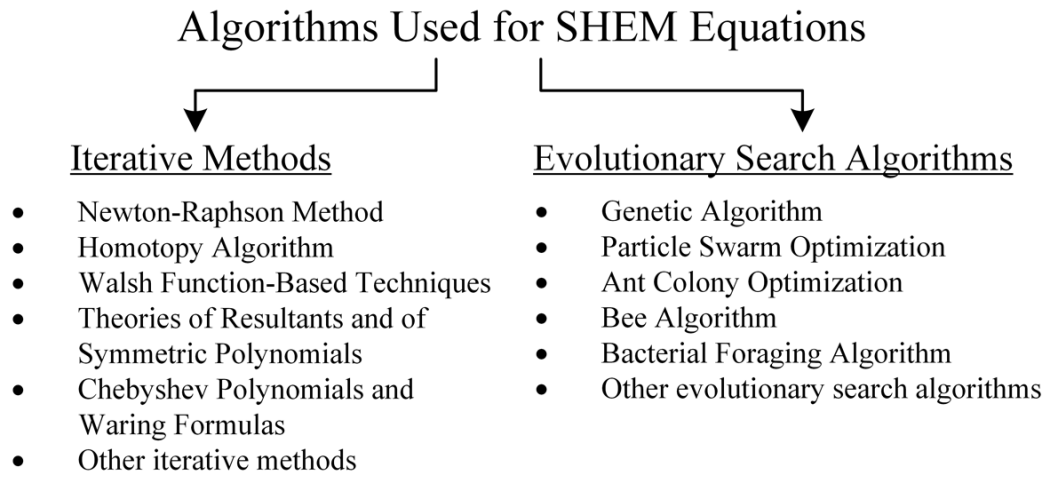


Figure 1.4: Algorithms Used for Solution of SHEM Equations

1.3.3 Offline and Online Applications

Almost all of the aforementioned methods require heavy computing which may not be realized in a fast and effective way unless a microcontroller whose clock frequency is considerably high is utilized. Therefore, in practice, SHEM switching angle sets have been solved for by one of the aforementioned methods beforehand and then stored as a lookup table in the microcontrollers up to now. In [9] and [10], for example, the switching angles are solved by a hybrid algorithm which combines the genetic algorithm and the gradient-based steepest descent method. Genetic algorithm is utilized to determine proper initial points whereas these initial points are processed by the steepest descent method to find the global optimum in a fast way. Obtained values of switching angles for different modulation index values are stored as a lookup table in the microcontroller.

Although storing the switching angle sets for different modulation index values in the microcontroller is effective, the use of discrete modulation index values may lead to some disadvantages in some cases, resulting in nonoptimum commutations. Moreover, significant amount of memory is needed in the microcontroller if the number of stored lookup tables is increased [32]. There is also possibility that the solutions might be missing for some problems, and interpolation techniques may be required [33]. This problem has led the researchers to search for

online application of SHEM in an effective way.

As mentioned before, solving the equations for switching angles require heavy computing effort. In [33], the authors used the generalization ability of artificial neural network (ANN) to circumvent this problem. The GA is used to calculate switching angles beforehand for different DC source values, and then the ANN is used to train the controller to determine the switching angles for different DC sources in real-time at each phase of the multilevel inverter. By this way, the ANN replaces the lookup table and introduces its inherent capability to generalize the solution space into the problem with proper training.

Another approach for online application of SHEM is investigated in [32]. The authors proposed an analytical procedure for computation of all pairs of valid switching angles used in pattern generation in five-level H-bridge cascaded inverters. The proposed procedure allows fully analytical calculation of switching angles using Chebyshev polynomials and Waring formulas. It is asserted in the research that due to its limited complexity, the procedure can be easily implemented in real time using digital signal controller, programmable logic device or FPGA. However, elimination of only one harmonic is investigated in the research. Although it has been asserted that the procedure can be extended to multiple harmonic elimination, this has been left as a future work, and it is not known yet how the procedure will perform when it is applied to multiple harmonic elimination.

1.4 Scope of the Thesis

Within the scope of this thesis, SHEM has been applied in real time to find optimum switching angles with the application of particle swarm optimization, eliminating 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, and 19^{th} harmonics in the output voltage of a grid-connected inverter with a variable DC link input voltage. The PSO algorithm has been implemented in the FPGA, which has been used as the main and sole controller in order to provide gating signals for IGBTs utilized in the inverter.

The outline of this thesis is given as follows:

In Chapter 2, the problem definition is given for offline application of SHEM. Inverters with variable DC link voltage are investigated in two different applications, photovoltaic and traction applications. It is shown that the modulation index values for inverters with variable DC link voltage varies in a wide range. The disadvantages of offline calculation of SHEM switching angles and then storing the angle sets in the microcontroller as lookup tables are shown by investigating discretization of modulation index values, lookup table storage requirement, and infeasible region of solution space.

In Chapter 3, particle swarm optimization algorithm is elaborated. The mindset behind evolutionary search algorithms are introduced, and their common features are mentioned along with their advantages over traditional iterative methods. Then, PSO algorithm is introduced, and its process flow is given along with equations used in the algorithm. SHEM patterns are elaborated in detail, and the application of PSO algorithm to the cost function of the formulated SHEM problem is shown. Finally, the effects of parameters in the PSO algorithm on the solution of the problem are investigated along with related data and figures.

In Chapter 4, FPGA implementation of online SHEM by PSO algorithm is elaborated. An overview of FPGAs is given along with its structure and application areas, merits of using FPGAs, a general design flow used for projects with FPGA, and features of fixed-point arithmetic. Then, the implemented VHDL code for FPGA is investigated for each of the modules used in the code, which are PSO, PLL, dead-time modules and ADC, DAC, and protection codes. The workflow of the PSO module is investigated along with related diagrams, and the theories of concepts utilized for the algorithm are given.

In Chapter 5, simulations of the grid-connected inverter system with online application of SHEM in Simulink platform are discussed along with figures and tables. Simulation of implemented VHDL code in ISim platform and its hardware co-simulation are elaborated with the results acquired from the calculation of SHEM switching angles in real time. Finally, experimental results are given for the implemented grid-connected three-phase two-level inverter with necessary

figures, tables, and data.

In Chapter 6, a summary of the work done for the thesis is given with some predictions and suggestions for future work.

In Appendix A, the related schematics of the grid-connected inverter drawn in ISIS platform and its PCB design drawn in ARES platform of Proteus Professional software are given.

Finally in Appendix B, the list of laboratory equipments used during the tests conducted on the inverter can be found.

CHAPTER 2

PROBLEM DEFINITION

In this chapter, the problems of offline SHEM application will be discussed. As mentioned in the previous chapter, implementing SHEM switching angles as a lookup table for different modulation index values in the microcontroller has some disadvantages which affect the normal operation of the inverter. The incentives for seeking online application of SHEM can be summarized as variable DC link voltage of single-stage inverters, discretization of modulation index values, lookup table storage requirement, and infeasible region of SHEM solution space.

2.1 Variable DC Link Voltage

As introduced in the previous chapter, inverters convert the DC input voltage to a symmetric AC output voltage with controllable magnitude and frequency. The simplest form of an inverter is a single-phase half-bridge inverter. As shown in Figure 2.1, the upper and lower semiconductors in this arrangement are switched so that they connect $+V_{dc}/2$ or $-V_{dc}/2$ to the output, whose reference is taken as the midpoint of the input capacitors. Therefore, the DC input voltage is converted to the AC output voltage which alternates between positive and negative. Single-phase full-bridge inverters and three-phase full-bridge inverters are derived from this configuration by adding additional legs of semiconductors as shown in Figure 2.2 and Figure 2.3 [8].

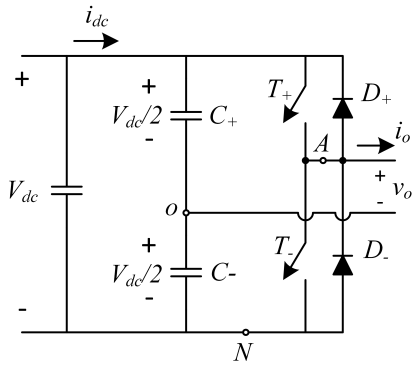


Figure 2.1: Single-Phase Half-Bridge Inverter

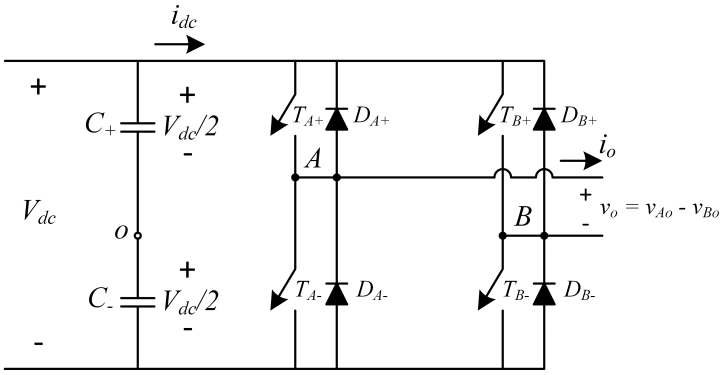


Figure 2.2: Single-Phase Full-Bridge Inverter

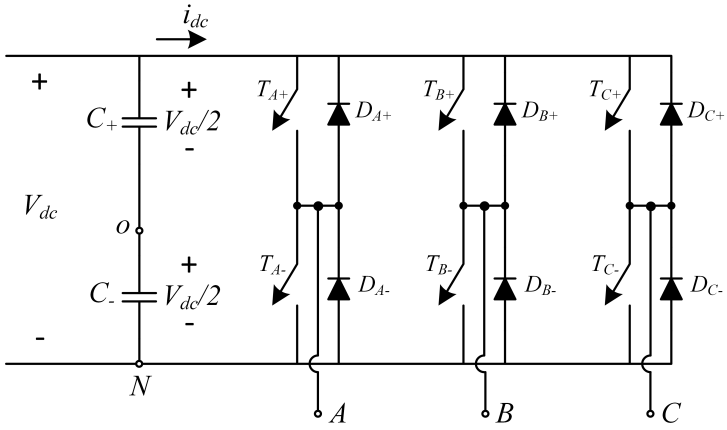


Figure 2.3: Three-Phase Full-Bridge Inverter

Modulation index is defined as the ratio of the output voltage to the input voltage of the inverter multiplied by a constant, which is specific to the topology and control method of the inverter. By changing the modulation index, the fundamental output voltage can be controlled, and, in turn, active and reactive power flow can be controlled according to the demands. Therefore, the changes to the input DC link voltage directly affects the operation of the inverter, and the control loop has to take care of these changes in order to provide stable and robust service.

In some applications where the input voltage is not high enough to supply the DC-AC inverter, an additional DC-DC boost converter stage is used between the supply and the inverter. By adjusting the duty cycle of this converter, the DC link voltage can be held at a constant value, thus relieving the inverter control of taking care of variable input voltage. However, two-stage inverters have lower power conversion efficiency, higher cost, and lower reliability since the chance of component failure is higher with respect to the single-stage converter [34].

A variable DC link voltage at the input to a single-stage inverter causes the modulation index value to be variable, and this results in different switching angle sets if SHEM is used as the control method. Therefore, all of these angle sets should be stored for discretized values of modulation index in the microcontroller beforehand so that the inverter can handle the input DC link voltage variations. This requirement causes the discretization, storage, and solution space problems for modulation index values, which will be explained later in this chapter.

Two of the applications where the input DC voltage changes according to the conditions outside the inverter are introduced briefly as follows.

2.1.1 Photovoltaic Applications

Photovoltaic (PV) power generation has a large share of installed capacity along with the wind power as one of the fast-developing renewable energy resources. As can be seen from Figure 2.4, the worldwide PV power generation reached the fastest growth rate of installed capacity at 60 % between 2007 and 2012 and

at 40 % only in 2012. It is foreseen that the cost of PV systems will continue decreasing in the future, which will make it possible for the grid-connected PV systems to compete with other renewable energy systems [3].

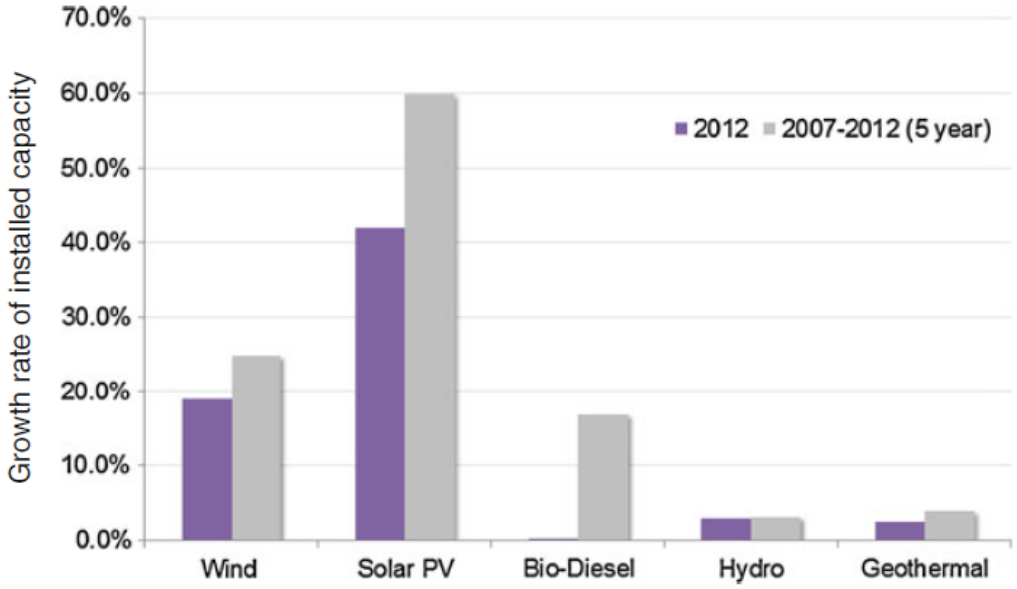


Figure 2.4: Worldwide Growth Rate of Installed Capacity for Different Renewable Technologies in 2012 and between 2007 and 2012 [3]

The solar energy is immensely affected by the environmental conditions such as irradiance level and ambient temperature, which makes it essential for a grid-connected PV power system to transfer and convert the solar energy efficiently and reliably. This system has to harvest the maximum power from the PV panels for changing environmental conditions, to operate with grid synchronization, and to comply with grid connection requirements. PV panels are the basic building blocks of a PV system, in which they are connected to a grid-connected inverter for power conversion. They consist of PV cells connected in series and parallel to achieve increased output voltage and current levels, respectively. If the total DC link voltage is low, a DC-DC boost converter may be needed to increase this voltage to a sufficient input voltage level for the inverter [4].

PV cells may be made of various materials such as mono- and poly-crystalline silicon, or cadmium telluride, amorphous silicon, copper indium gallium selenide for thin-film cells. However, the selection of material does not affect the oper-

ating principle of the PV technology, which is based on the photovoltaic effect. This effect converts the sunlight to an electromotive force, creating a DC current when the PV cell is short-circuited. This short-circuit current depends on the solar irradiance level and the ambient temperature. Figure 2.5 shows the electrical circuit equivalent of a PV cell, where i_{ph} is the photocurrent source, with which a diode is connected in parallel, R_p is the shunt resistance, and R_s is the series resistance [4].

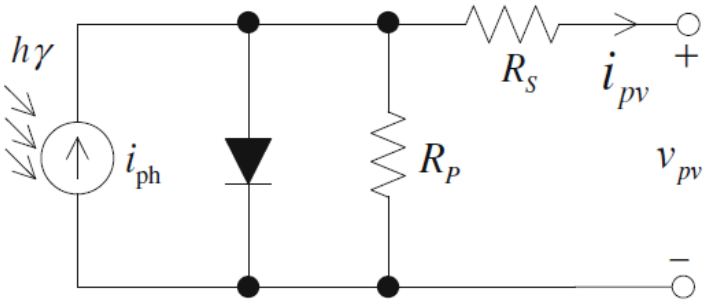


Figure 2.5: PV Cell Electrical Equivalent Circuit [4]

The electrical I-V and P-V characteristics of a PV panel are not linear and depends on the ambient conditions, as can be seen from Figure 2.6 for (a) various solar irradiance levels at 25°C and (b) various ambient temperatures at 1000 W/m^2. A maximum power point tracking (MPPT) algorithm is needed to extract the most of the solar energy and convert it from the PV panels because of their non-linear characteristics and environmental dependency [4].

As can be observed from Figure 2.6, the maximum power point (MPP) voltage should be the operating input voltage of the grid-connected inverter, and it is dependent on the solar irradiance and ambient temperature. Solar irradiance does not affect the MPP voltage as much as ambient temperature does. If the inverter is a two-stage one with a DC-DC boost converter, this converter takes care of the MPP voltage variation by adjusting its duty cycle to harvest the maximum power from the PV panel and to increase the PV output DC voltage to a level which exceeds the peak grid voltage, making the DC link voltage of the DC-AC inverter invariable [35]. However, for single-stage inverters, the input voltage of the inverter should be high enough to inject power to the grid. For this

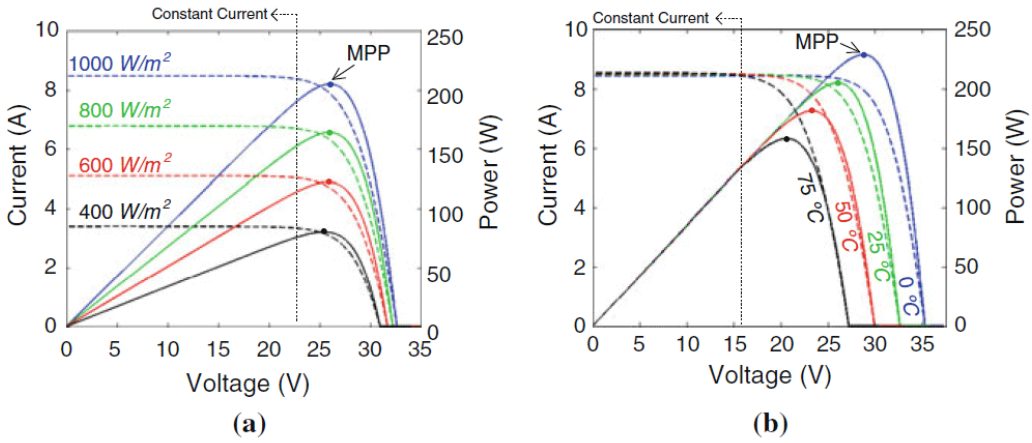


Figure 2.6: I-V and P-V Characteristics of a PV Panel [4]

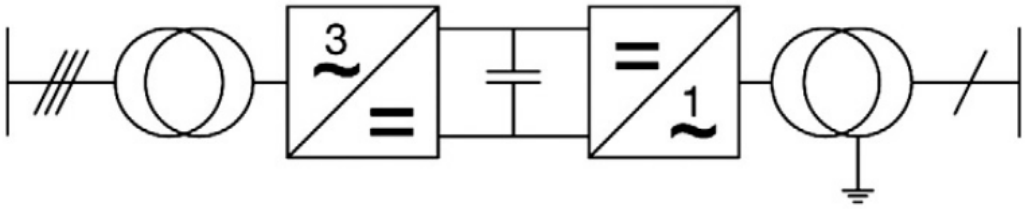
reason, a PV string is created with series-connected PV panels. The variation of MPP voltage against changing solar irradiance and ambient temperature for an example PV field, which consists of 20 thin-film solar panels in two parallel strings rated at 1600 W, is shown in Table 2.1 below. As can be seen from this table, the variation of voltage caused by the ambient temperature is so high that it varies between 584 V and 786 V. As explained before, this causes a wide variation of modulation index values for the inverter, and this means that a wide range of switching angles should be stored as a lookup table in the microcontroller if the control method is chosen as SHEM for the single-stage inverter.

Table 2.1: Variation of MPP Voltage Against Changing Solar Irradiance and Ambient Temperature

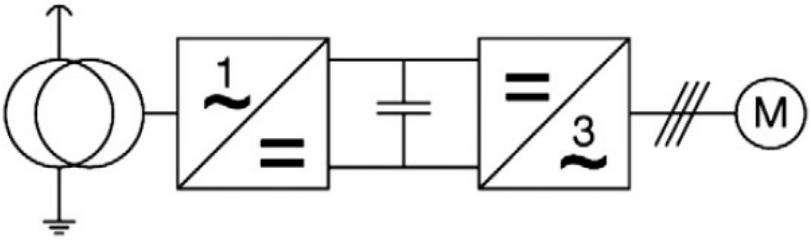
	200 W/m²	**400 W/m²**	**600 W/m²**	**800 W/m²**	**1000 W/m²**
−10 °C	747.6 V	777.1 V	784.7 V	785.8 V	783.6 V
10 °C	706.5 V	736.6 V	745.0 V	746.7 V	745.0 V
30 °C	665.6 V	696.3 V	705.5 V	707.8 V	706.6 V
50 °C	624.9 V	656.3 V	666.3 V	669.1 V	668.4 V
70 °C	584.4 V	616.5 V	627.3 V	630.8 V	630.6 V

2.1.2 Traction Applications

Railways are the most energy-efficient land-based means of transport, and the most efficient way to deliver the required power to electric motors used in railways is via an electric power supply system alongside the railway tracks. Railway power supply systems are either AC or DC systems. The AC railway power supply system is summarized in Figure 2.7, where the upper image (a) illustrates a railway power supplying converter which converts three-phase AC public grid electricity to single-phase AC railway network electricity, whereas the lower image (b) depicts a vehicle unit converter which delivers the energy from the single-phase AC railway network to three-phase AC traction motor. The AC systems can either be operated at the same public grid frequency or at a different frequency which is normally lower. DC systems, however, require only the second conversion where the electricity from the DC supply is converted to three-phase electricity to be delivered to AC traction motor [36].



(a) Railway Power Supplying Converter



(b) Vehicle Unit Converter

Figure 2.7: AC Railway Power Supply System [36]

There are several different standards for the contact line voltages for both AC and DC railway systems. Electricity is delivered to the trains in different ways, often via an overhead contact line called the catenary. The catenary is actually a geometrical shape in mathematics, namely it is the shape of a cord hanging freely

from two fixed points. The physical catenary goes above the actual overhead contact line. Therefore, it is normal to denote the entire system of conductors hanging from the poles alongside the railway line as the catenary system [36]. Railway locomotives and other units are supplied with the electrical energy acquired from the catenary, which makes it possible for them to operate without a prime mover. Utilization of AC motors for electric traction is advantageous since it has higher power-to-weight ratio than diesel or steam powered traction. Moreover, faster acceleration can be achieved via electric traction [37].

The standard EN 50163 is related to supply voltages of traction systems for railway applications [38]. AC systems have voltages ranging from 15 to 25 kV (at 16.7 or 50-60 Hz) and are usually found in long distances or routes with heavy traffic. DC systems, on the other hand, are generally utilized for trams, suburb trains, and medium distances. Light rail and metro services can use either aerial catenaries or third rail, with operating voltages ranging from 600 to 1500 V. Higher power applications require catenary voltages up to 3 kV [39]. The supply voltages of traction systems are summarized in Table 2.2, and Figure 2.8 shows the maximum value of the catenary voltage according to the duration, where Zone C is for overvoltages between highest long-term overvoltage U_{max3} and highest non-permanent voltage U_{max2}, Zone D is for U_{max2}, and Zone E is for highest permanent voltage U_{max1} [37, 38].

As can be seen from Table 2.2 and Figure 2.8, the catenary voltage of the traction system may change considerably between lowest non-permanent voltage and highest non-permanent voltage. For a DC traction system, this causes the input voltage of the DC-AC inverter to fluctuate considerably, which is the same situation as that seen for PV applications, explained in the previous section. If the inverter output harmonics are to be eliminated via SHEM, the requirement that a large lookup table of switching angles should be stored in the microcontroller of the inverter is again necessary for changing values of the modulation index.

Table 2.2: Nominal Voltages and Their Permissible Limits for Traction Systems

Traction system	Lowest non-permanent voltage (U_{min2}) (V)	Lowest permanent voltage (U_{min1}) (V)	Nominal voltage (U_n) (V)	Highest permanent voltage (U_{max1}) (V)	Highest non-permanent voltage (U_{max2}) (V)
600 V DC	400	400	600	720	800
750 V DC	500	500	750	900	1000
1.5 kV DC	1000	1000	1500	1800	1950
3 kV DC	2000	2000	3000	3000	3000
15 kV AC, 16.7 Hz	11000	12000	15000	17250	18000
25 kV AC, 50 Hz	17500	19000	25000	27500	29000

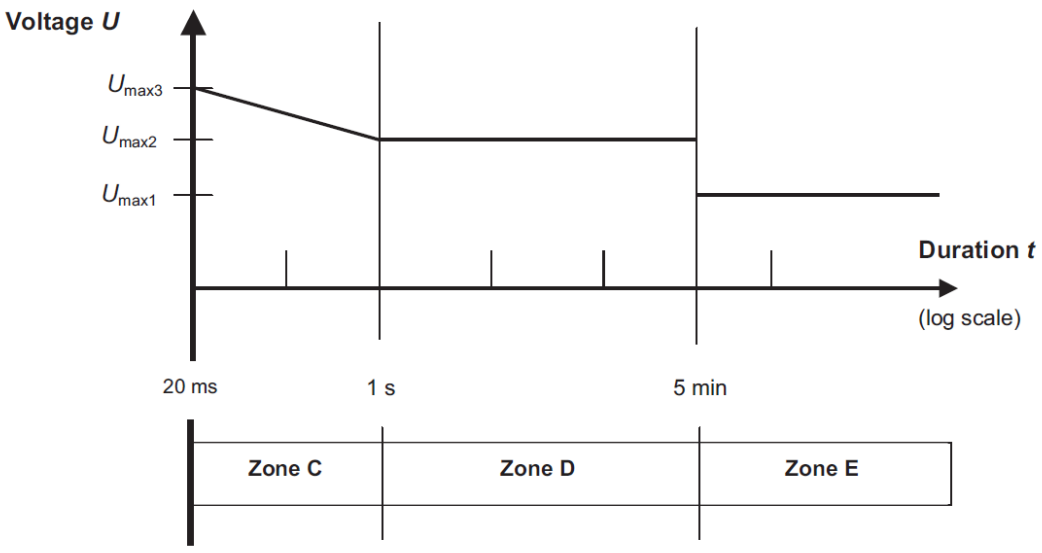


Figure 2.8: Maximum Value of the Catenary Voltage According to the Duration [38]

2.2 Discretization of Modulation Index

When implemented in a microcontroller as a lookup table, SHEM switching angles for discretized modulation index values are stored as it is not possible to reach a continuous range due to the nature of digital control. For example, in [10], 150 steps of modulation index values are used from −50-MVAr- to +50-MVAr-reactive-power control, and the optimum values of switching angles are found for these modulation index values to be stored in a 150 × 5 lookup table.

The modulation index value is generally found by a control loop as the output of a PI controller. The value found has to be rounded to a value stored in the lookup table if it is not exactly stored. Therefore, a slightly different value of modulation index than the value, which is required by the control loop, has to be used. Since the application of switching angles stored for this modulation index value will bring about a different fundamental voltage than the required voltage and non-eliminated lower-order harmonics at the inverter output, the active and reactive power injected to the grid and the total harmonic distortion will be different than desired values.

This phenomenon can be summarized in a simple example. Figure 2.9 shows a three-phase two-level inverter for a PV application in which the input DC link voltage changes between 600 V and 800 V. Assuming SHEM is used for the control method with a lookup table of modulation index values, let us consider only 10 values of modulation index are stored along with the switching angles that eliminate the 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, and 19^{th} harmonics. This requires storing a lookup table of 10 × 7 switching angles in the microcontroller as shown in Table 2.3.

This inverter structure can be simplified in a single-line diagram where the power flow is defined from the AC inverter output voltage to the AC grid through the filter reactor. Figure 2.10 illustrates single-phase active and reactive power flow in this single-line diagram, where V_I is the line-to-neutral RMS voltage at the inverter side, V_G is the line-to-neutral RMS voltage at the grid side, δ is the load angle, I is the RMS current flowing from inverter to grid, R is the total loss

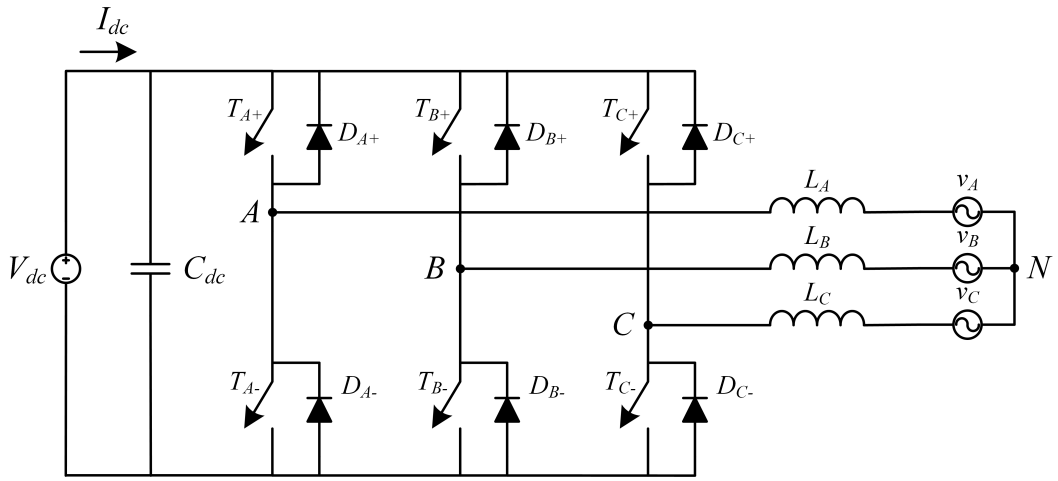


Figure 2.9: Circuit Diagram of Three-Phase Two-Level Inverter

Table 2.3: Example Lookup Table for Switching Angles for Different Modulation Index Values

Modulation index	$\alpha_1(^\circ)$	$\alpha_2(^\circ)$	$\alpha_3(^\circ)$	$\alpha_4(^\circ)$	$\alpha_5(^\circ)$	$\alpha_6(^\circ)$	$\alpha_7(^\circ)$
0.10	$\alpha_{1,1}$	$\alpha_{1,2}$	$\alpha_{1,3}$	$\alpha_{1,4}$	$\alpha_{1,5}$	$\alpha_{1,6}$	$\alpha_{1,7}$
0.20	$\alpha_{2,1}$	$\alpha_{2,2}$	$\alpha_{2,3}$	$\alpha_{2,4}$	$\alpha_{2,5}$	$\alpha_{2,6}$	$\alpha_{2,7}$
0.30	$\alpha_{3,1}$	$\alpha_{3,2}$	$\alpha_{3,3}$	$\alpha_{3,4}$	$\alpha_{3,5}$	$\alpha_{3,6}$	$\alpha_{3,7}$
0.40	$\alpha_{4,1}$	$\alpha_{4,2}$	$\alpha_{4,3}$	$\alpha_{4,4}$	$\alpha_{4,5}$	$\alpha_{4,6}$	$\alpha_{4,7}$
0.50	$\alpha_{5,1}$	$\alpha_{5,2}$	$\alpha_{5,3}$	$\alpha_{5,4}$	$\alpha_{5,5}$	$\alpha_{5,6}$	$\alpha_{5,7}$
0.60	$\alpha_{6,1}$	$\alpha_{6,2}$	$\alpha_{6,3}$	$\alpha_{6,4}$	$\alpha_{6,5}$	$\alpha_{6,6}$	$\alpha_{6,7}$
0.70	$\alpha_{7,1}$	$\alpha_{7,2}$	$\alpha_{7,3}$	$\alpha_{7,4}$	$\alpha_{7,5}$	$\alpha_{7,6}$	$\alpha_{7,7}$
0.80	$\alpha_{8,1}$	$\alpha_{8,2}$	$\alpha_{8,3}$	$\alpha_{8,4}$	$\alpha_{8,5}$	$\alpha_{8,6}$	$\alpha_{8,7}$
0.90	$\alpha_{9,1}$	$\alpha_{9,2}$	$\alpha_{9,3}$	$\alpha_{9,4}$	$\alpha_{9,5}$	$\alpha_{9,6}$	$\alpha_{9,7}$
1.00	$\alpha_{10,1}$	$\alpha_{10,2}$	$\alpha_{10,3}$	$\alpha_{10,4}$	$\alpha_{10,5}$	$\alpha_{10,6}$	$\alpha_{10,7}$

resistance of the reactor, X is the reactance of the reactor, P_I and Q_I are the inverter-side active and reactive powers whereas P_G and Q_G are the grid-side active and reactive powers. If it is assumed that R is much smaller than X, the active and reactive power flow are governed by Equation 2.1, Equation 2.2, and Equation 2.3 [9]. For this inverter, the modulation index is given as in Equation 2.4 where V_{dc} is the input DC link voltage.

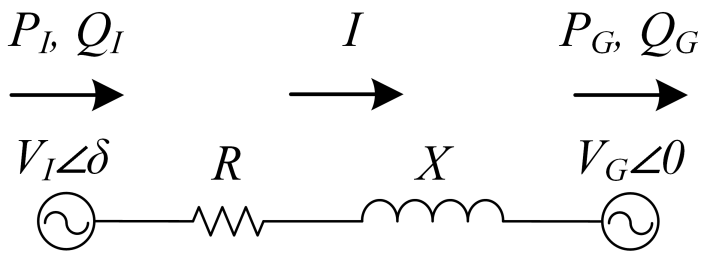


Figure 2.10: Single-Line Diagram of the Three-Phase System

$$P_I = P_G = \frac{V_I V_G}{X} \sin\delta \tag{2.1}$$

$$Q_I = V_I \frac{V_I - V_G \cos\delta}{X} \tag{2.2}$$

$$Q_G = V_G \frac{V_I \cos\delta - V_G}{X} \tag{2.3}$$

$$M = \frac{\pi V_I \sqrt{2}}{2V_{dc}} \tag{2.4}$$

Assuming that it is desired the inverter does not inject any active or reactive power to the grid, which is a three-phase grid at 400 $V_{rms,l-l}$ and 50 Hz, the RMS value of the fundamental voltage at one leg of the inverter should be equal to the RMS value of the line-to-neutral voltage of the grid, 220 $V_{rms,l-n}$, and the power angle between these two voltage vectors should be zero. Assuming the power angle is kept at zero by a separate controller and the reactive power is desired to be kept at zero, if the input DC link voltage is 752 V, for example, the required modulation index value will be 0.65, which will bring about the worst error. Since there is no defined switching angle set for this value, it will be rounded to 0.7 and the angle set corresponding to this value will be applied in the controller. For this value of modulation index, the fundamental output voltage will be 237 $V_{rms,l-n}$ instead of 220 $V_{rms,l-n}$. Thus, although the active power will be kept at zero by the power angle controller, the injected reactive power at the grid side will be 1188 VAr per phase instead of zero. Moreover, this

error will increase if a lower value of reactance is used. Considering a lookup table of 100 × 7 switching angles, the error in the reactive power corresponding to the worst error in the modulation index (0.005) will decrease to 118 VAr per phase for a DC link voltage of 746 V. Therefore, discretization of modulation index values results in an error in the reactive power flow of the inverter, and a lookup table with finer values of modulation index should be used, which results in the need for larger storage area allocation in the microcontroller.

Same approach can also be used for a multilevel inverter. In this case, unequal DC link voltages of separate H-bridges affect all of the SHEM equations [33]. This is not the case for two-level inverter since the DC link voltage term is not present in the SHEM equations, which will be investigated in the next chapter, except the one that controls the fundamental voltage. Therefore, using a different switching angle set only affects the fundamental voltage and, in turn, reactive power. For multilevel inverter, however, since all of the equation set is affected, the lower-order harmonics will not be completely eliminated for a rounded value of modulation index; therefore, the total harmonic distortion will also be higher along with the erroneous reactive power being injected into or consumed from the grid.

2.3 Lookup Table Storage

In practice, more than 10 sets of switching angles are stored to make the range of modulation index values more continuous. However, because of the nature of digital control, only a limited number of angle sets can be stored in the microcontroller. Although storing more angle sets decreases the error caused by the discretization, this requires more storage area to be used in the microcontroller. For example, storing the 10 × 7 lookup table of Table 2.3, in which the resolution of switching angles is defined to be 32-bit in the microcontroller, consumes 280 bytes of memory whereas storing a 100 × 7 lookup table consumes 2.73 kB of memory. Moreover, if we want to eliminate one more harmonic from the output voltage, one more switching angle has to be inserted in one angle set, making the table size 100 × 8. This increase brings about 400 bytes of extra usage

in the microcontroller. For lookup tables consisting of more discretized values of modulation index and more switching angles to eliminate more lower-order harmonics, the size of the lookup table will be larger.

An advantage of online application of SHEM over offline application with lookup table is that no lookup table is required for calculation of switching angles. This advantage is of course compensated by increased calculation workload. Nevertheless, this calculation workload does not increase linearly as the number of harmonics to be eliminated increases if evolutionary search algorithms are used for online application of SHEM. As it will be explained in the next chapter, evolutionary search algorithms can solve the corresponding equation set by a concept of parallel searching realized by the individuals of the population. An increase in the number of harmonics to be eliminated results in more calculation workload for the fitness value of the switching angle set; however, the number of individuals in the population of the evolutionary search algorithm does not have to increase linearly, and even the same number of individuals can solve higher order equation sets if parameters of the algorithm are selected carefully.

2.4 Infeasible Region of Solution Space

Both for two-level and multilevel inverters, the SHEM equations are nonlinear transcendental equations with sinusoidal terms. The equation set is solved for switching angles which produce the desired modulation index and eliminate specified number of harmonics. Modulation index takes values between 0 and 1, and a solution fulfilling the constraints can be found for most of this range. However, there is a small region of this range in which there is no feasible solution set, namely, there is no switching angle set which fulfills all of the constraints. For a two-level three-phase inverter controlled with 7 SHEM switching angles which eliminate 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, and 19^{th} harmonics in the output line-to-neutral voltage, this region can be seen clearly in Figure 2.11 below. In this figure, it can be seen that some switching angles start to converge each other after 0.9 modulation index, which causes the corresponding notches in the output voltage waveform of the inverter to perish. Moreover, if harmonic content of this

waveform is investigated, it can be seen that the lower-order harmonics are not completely eliminated since it is not possible, as shown in Figure 2.12.

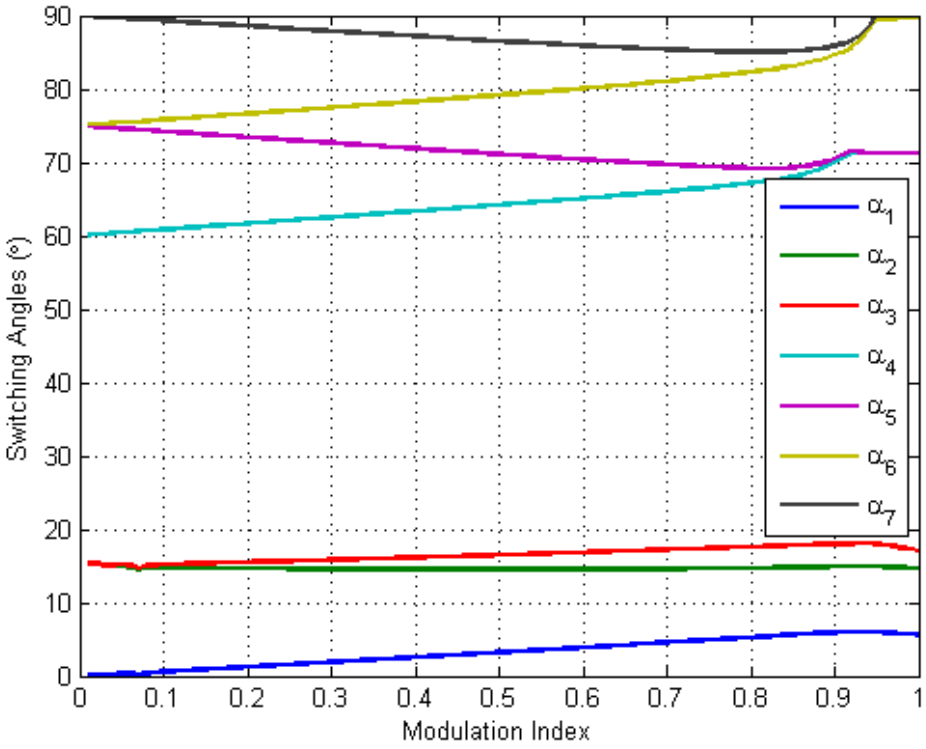


Figure 2.11: Switching Angles vs Modulation Index Graph for the VSI

If SHEM is desired to be applied online, modulation index should be limited at the boundary of this region or some new switching angle sets should be offered for infeasible values, which will increase the continuity of the solution space and stability of the inverter operation. If a lookup table is to be used, the missing solution space can be filled with angles found for a different configuration of the problem. Instead of configuring the problem to minimize the individual harmonics, the total harmonic distortion at the inverter output voltage can be taken as the parameter to be minimized. However, this means a change of characteristics at the feasible region boundary, and it should be taken care of by selecting switching angles carefully in order to make the transition smooth.

Evolutionary search algorithms have distinct advantages over iterative methods at this point. As it will be explained more in detail in the next chapter, these algorithms search the solution space thoroughly, and they do not get trapped

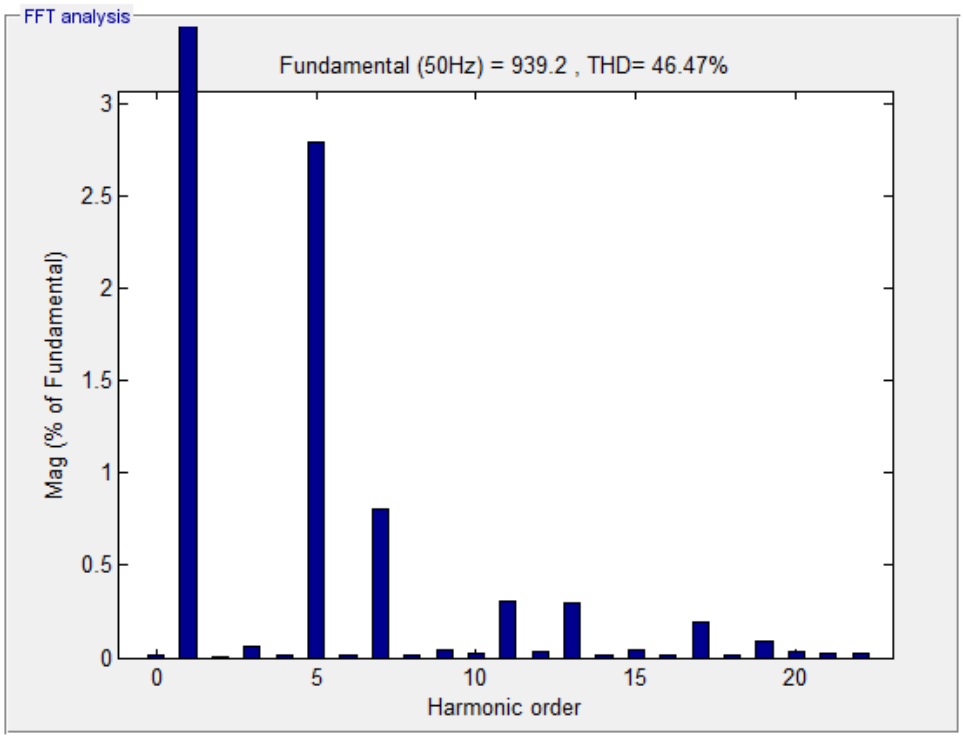


Figure 2.12: FFT Analysis of the Output Voltage Waveform with M=0.95

in local minima. Although traditional iterative algorithms require good initial points for the algorithm to converge, evolutionary algorithms can generally find the solution set even with a random initial population. Iterative algorithms fail to suggest switching angle sets for infeasible region of solution space; however, evolutionary algorithms manage to find a solution set for such regions. Although this solution does not eliminate specified harmonics since it is not possible, it minimizes these harmonics and is the best solution set that can be used for the specified modulation index. This brings about continuity and smooth transition in the solution space. If the parameters of the evolutionary algorithm are set carefully, the solution set can be found much faster than it is found via iterative methods, which makes online application of SHEM more feasible.

CHAPTER 3

APPLICATION OF PARTICLE SWARM OPTIMIZATION TO SHEM

3.1 Evolutionary Search Algorithms

Large-scale engineering problems often require mathematical optimization to reach the best case in which the cost is minimized. However, these problems are rarely easy to solve with conventional mathematical methods. The difficulties associated with these optimization problems have brought about the development of alternative solutions. NP-hard problems with many variables and nonlinear cost functions cannot be solved by linear programming and dynamic programming techniques generally, and only local optima can be achieved in many cases. This caused researchers to investigate evolutionary algorithms to find global optimum for nonlinear problems [40].

Evolutionary algorithms are stochastic search methods based on the processes inspired by evolution and/or social behaviour of species in the nature, for example, the way how ants find the shortest way to food source and the way how birds migrate via shortest route to their destination. In order to solve complex optimization problems in a fast and robust manner, several evolutionary algorithms have been developed to mimic the efficient behaviour of these species in the nature [40]. Although all of the possible candidate solutions can be evaluated to find the optimum one for a small search space, it is very impractical to do so for a large search space. At this point, the developed evolutionary algorithms have been found to be more effective than traditional search algorithms [41].

Evolutionary algorithms are processes that operate on a set of candidate solutions, which are individuals in a population. Each individual is actually an encoded form of the candidate solution. The population is generated with a random or heuristic approach at first, and each individual is evaluated with a fitness function in order to assess its candidacy for a potential global solution. This fitness function is a quantitative information in the algorithm [41]. The main ingredients of evolutionary algorithms can be summarized as a population consisting of individuals with assigned fitness values via a fitness function, exchange of information in the neighbourhood of an individual, evolution of the population or generational replacement, encoding of the solution, history of the individual, improvement of the individual, and introduction of noise and perturbation in the population [42]. Figure 3.1 below shows the location of evolutionary algorithms with respect to other deterministic and non-deterministic procedures [41].

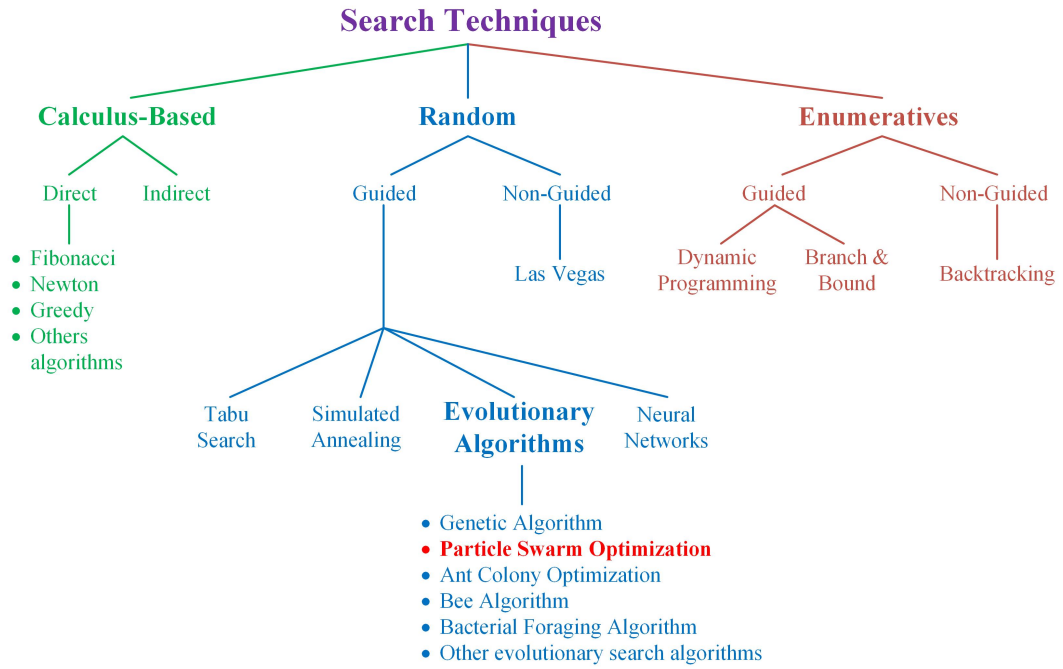


Figure 3.1: Search Techniques Tree

The advantages of evolutionary computation can be summarized briefly as follows.

- *Conceptual simplicity:* Without using a gradient information, the algo-

rithm converges to a global optimum with only initialization, iterative evolution, and selection with particular fitness value.

- *Broad applicability:* Any problem which can be formulated as a cost function to be optimized can be solved via evolutionary algorithms, which makes these algorithms applicable for many problems in different areas.

- *Hybridization with other methods:* Traditional optimization algorithms such as steepest descent method can be combined with evolutionary algorithms. In these applications, the gradient-based methods can be used after evolutionary algorithms find good starting points for fast implementation. These algorithms can also be used with neural networks, fuzzy systems and many other systems.

- *Parallelism:* One of the most important features of evolutionary algorithms is that the individuals in a population operate in parallel to find the global optimum solution; therefore, these algorithms can reach the solution much faster than traditional optimization algorithms.

- *Robust to dynamic changes:* Traditional optimization algorithms might require a restart if they get stuck in a local minimum; therefore, they are not robust to dynamic changes. On the other hand, the individuals in the evolutionary algorithms can be adapted to new environmental situations in a fast and easy manner. Thus, it is generally not needed to restart the algorithm at all.

- *Solving problems that have no solutions:* Evolutionary algorithms are very advantageous for problems for which there is no human experience. Although "artificial intelligence solves problems, they do not solve the problem of how to solve problems". However, evolutionary algorihms give a method for solving "the problem of how to solve problems" [41].

Genetic algorithm (GA) was the first evolutionary algorithm introduced in the literature. It was based on the principle of 'survival of the fittest' and the evolution process via reproduction. GAs have been widely used for many applications because of their efficient applicability to large problems, they often

require longer solution times than other evolutionary algorithms [40]. These algorithms include evolutionary programming, genetic programming, ant colony optimization, particle swarm optimization, differential evolution, biogeography-based optimization, cultural algorithms, opposition-based learning, simulated annealing, tabu search, artificial fish swarm algorithm, group search optimization algorithm, shuffled frog leaping algorithm, firefly algorithm, bacterial foraging optimization algorithm, artificial bee colony algorithm, gravitational search algorithm, harmony search algorithm, and some others [43].

3.2 Particle Swarm Optimization

Particle swarm optimization (PSO) is a stochastic population-based optimization technique developed by Dr. Russell Eberhart and Dr. James Kennedy in 1995 [44]. It is inspired by bird flocking, fish schooling, herd behaviour of land animals, and swarming behaviour of insects. PSO has many similarities with other evolutionary algorithms such as being initialized with a random or heuristic population and searching the solution by updating the population. On the other hand, there are no crossover or mutation operators in PSO, and no new population is created through evolution. In PSO algorithm, the particles are candidate solutions, and they search the problem space by pursuing the current optimum particles via cognitive and social interaction. It has been used in many areas recently instead of other algorithms because it finds the optimum solutions in a faster and cheaper way with a small number of parameters to adjust [40,41].

In a population of birds, fish or insects, one individual can affect the others by finding a more desirable path to the goal. However, each particle needs some level of "craziness" or randomness in their movement in order to escape local minima and explore the search space thoroughly [41]. For example, each bird can identify the bird at the best location and speed towards it using a velocity depending on its current position. Then, each bird can explore the search space locally with its cognitive intelligence, and this process continues until the desired destination is reached. Birds learn from both their own experience and the experience of other birds, which corresponds to local and global searches, respectively [40].

The coordinates of the particle associated with its best fitness value it has acquired so far is called the personal best location (*pbest*). The location with the best fitness value the population has reached altogether is called the global best location (*gbest*). The particle updates its velocity towards its *pbest* and *gbest* locations in each time frame. The total acceleration terms corresponding to local and global searches are weighted by separate random numbers [45].

The original process flow for the PSO algorithm is as follows.

1. A population of particles is initialized with random or heuristic positions on d dimensions in the problem space.

2. For each particle, the fitness function to be optimized is evaluated in d variables.

3. The current position of the particle is compared with its *pbest* via fitness function evaluation. If the current fitness value is better than the previous fitness value corresponding to the previous *pbest*, *pbest* is updated to the current location in d-dimensional space.

4. The current position of the particle is compared with the *gbest* via fitness function evaluation. If the current fitness value is better than the previous global best fitness value, *gbest* is updated to the current location in d-dimensional space.

5. The velocity and position of the particle is updated according to Equation 3.1 and Equation 3.2, respectively:

$$v_i(t+1) = \beta v_i(t) + c_1 \times rand \times (pbest_i(t) - x_i(t)) + c_2 \times rand \times (gbest(t) - x_i(t)) \tag{3.1}$$

$$x_i(t+1) = x_i(t) + v_i(t+1) \times \Delta t \tag{3.2}$$

6. Until a sufficiently good fitness value or maximum number of time frames is reached, the process is repeated from step 2 [41, 45].

β, on the right hand side of Equation 3.1, is the inertia weight that controls how much the current velocity will be dominant on the new calculated velocity. c_1 and c_2 are the cognition and social factors, respectively. They are the acceleration constants which update the velocity of a particle towards *pbest* and *gbest*. These coefficients are usually set to 2. *rand* is a random number between 0 and 1 and gives the particle its explorative capability over the search space. The first term on the right hand side corresponds to diversification whereas the second and third terms correspond to intensification in the search procedure. The velocity of the particles on each dimension are usually limited to a maximum velocity V_{max} in order not to go beyond the limits of the search space [41]. In later works, the use of a constriction factor has been found to be beneficial to guarantee the convergence of the PSO algorithm. This constriction factor can be incorporated into the velocity equation as follows:

$$v_i(t+1) = K \times [\beta v_i(t) + c_1 \times rand \times (pbest_i(t) - x_i(t)) + c_2 \times rand \times (gbest(t) - x_i(t))] \tag{3.3}$$

$$K = \frac{2}{|2 - \varphi - \sqrt{\varphi^2 - 4\varphi}|}, \ where \ \varphi = c_1 + c_2, \ \varphi > 4 \tag{3.4}$$

Typically, φ is set to 4.1 and the constant multiplier K is thus 0.729. V_{max} is limited to X_{max}, the dynamic range of each variable on each dimension, as a rule of thumb to acquire better results [45]. The basic flowchart of PSO is as shown in Figure 3.2 [41].

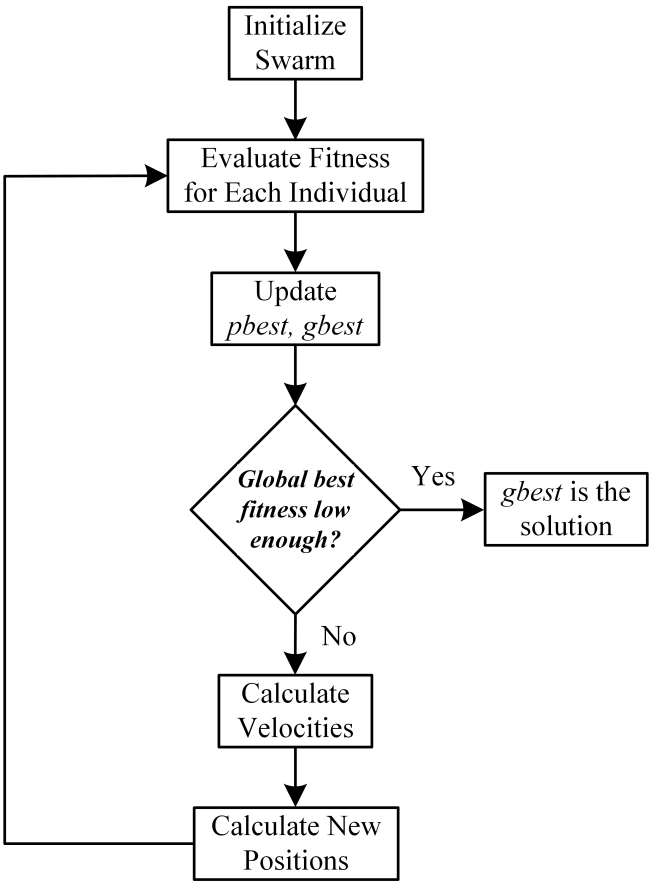


Figure 3.2: Basic Flowchart of PSO

3.3 Problem Formulation

In this thesis work, a three-phase two-level grid-connected inverter has been investigated and implemented for a PV application with online application of SHEM by PSO algorithm. The circuit diagram of the inverter is shown in Figure 3.3 whereas specifications of the inverter and the components used in the circuit are given in Table 3.1. PSO requires formulation of cost function to evaluate the fitness values of each particle at each time frame. Therefore, SHEM equations should be defined and put into a format so that each particle can be assigned a real fitness value. After determining the cost function, defining the boundaries of the solution space, generating an initial population of swarms in this solution space, and setting PSO parameters, the algorithm is ready to seek a feasible global optimum for the optimization problem under consideration.

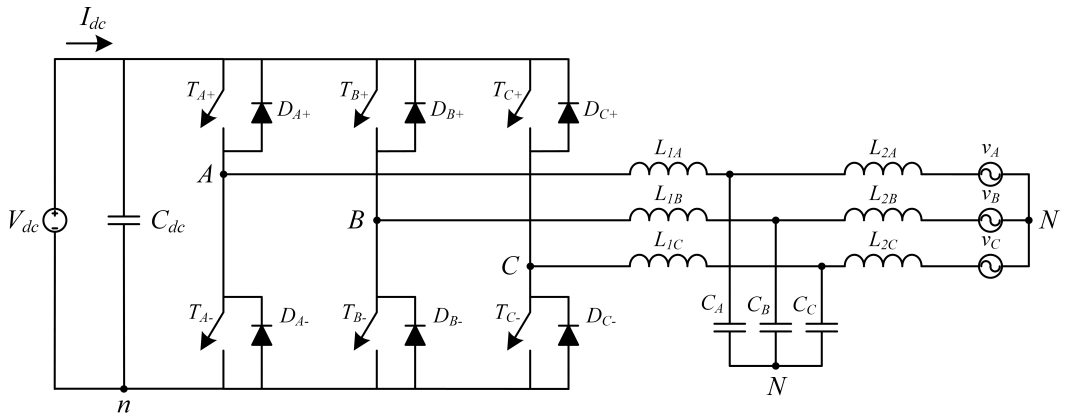


Figure 3.3: Three-Phase Two-Level Grid-Connected Inverter

Table 3.1: Specifications of the Inverter and Components

DC Link Voltage, V_{dc}	600 - 900 V
DC Link Current, I_{dc}	3 A_{max}
DC Link Capacitor, C_{dc}	40 μF
IGBT Maximum V_{CE} Voltage	1200 V
LCL Filter Inductors, L_{1A}, L_{1B}, L_{1C}	15 mH
LCL Filter Inductors, L_{2A}, L_{2B}, L_{2C}	15 mH
LCL Filter Capacitors, C_A, C_B, C_C	20 μF
Grid Specification	Three-Phase 380 V_{l-l}, 50 Hz
Rated Power	1.6 kVA

3.3.1 SHEM Patterns

For three-phase inverters, there are several harmonic elimination patterns available, which are shown in Figure 3.4. Three-phase line-to-line technique (TLL) is based on the elimination of harmonics directly in the line-to-line converter voltage whereas three-phase line-to-neutral techniques (TLN1 and TLN2) are based on the elimination of harmonics in line-to-neutral converter output voltage. The difference between the TLN1 and TLN2 techniques is that the total number of harmonics eliminated in TLN1 technique is even while it is odd in TLN2 technique. All triplen harmonics are not present in a three-phase three-wire system; therefore, there is no need to eliminate them [46, 47].

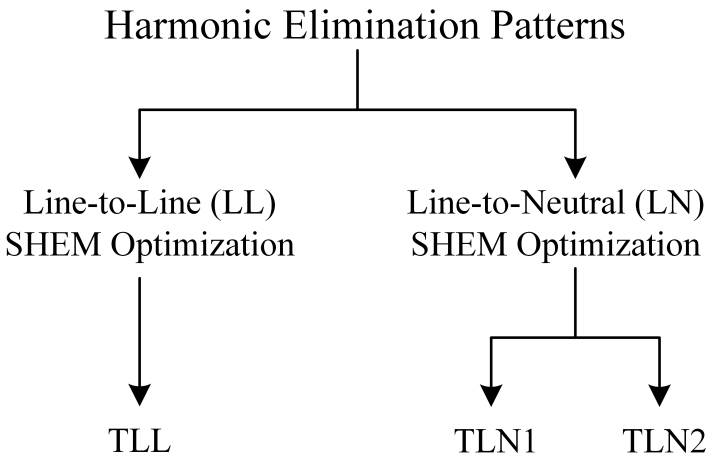


Figure 3.4: Harmonic Elimination Patterns for Three-Phase Inverters

The Fourier expansion of the converter voltage is as given in Equation 3.5.

$$v(t) = a_0 + \sum_{n=1}^{\infty} a_n \cos(n\omega_0 t) + b_n \sin(n\omega_0 t) \tag{3.5}$$

where

$$a_0 = \frac{1}{T} \int_{t_0}^{t_0+T} v(t)\,\mathrm{d}t \tag{3.6}$$

$$a_n = \frac{2}{T} \int_{t_0}^{t_0+T} v(t) \cos(n\omega_0 t)\, \mathrm{d}t \tag{3.7}$$

$$b_n = \frac{2}{T} \int_{t_0}^{t_0+T} v(t) \sin(n\omega_0 t)\, \mathrm{d}t \tag{3.8}$$

If the output voltage is an odd quarter-wave symmetric waveform, then the following simplification can be made:

$$a_0 = 0 \tag{3.9}$$

$$a_n = 0 \tag{3.10}$$

$$b_n = 0,\ if\ n\ is\ even \tag{3.11}$$

$$b_n = \frac{8}{T} \int_{0}^{T/4} v(t) \sin(n\omega_0 t)\, \mathrm{d}t,\ if\ n\ is\ odd \tag{3.12}$$

3.3.1.1 TLN1 Technique

As can be seen from the line-to-neutral voltage in Figure 3.5, there are odd number of notch angles present in the waveform, which results in elimination of even number of total harmonics via SHEM since one notch angle is used to control the fundamental component [46, 47].

b_n is found for odd harmonics by using Figure 3.5 and Equation 3.12:

$$b_n = \frac{4}{n\pi} \frac{V_{dc}}{2} \left[-1 - 2 \sum_{k=1}^{N} (-1)^k \cos(n\alpha_k) \right] \tag{3.13}$$

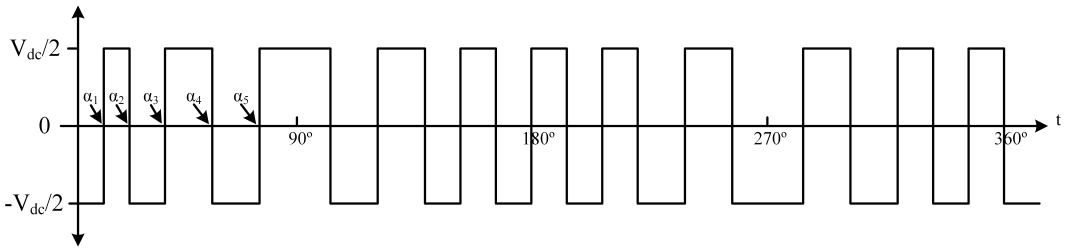


Figure 3.5: Line-to-Neutral Voltage for TLN1 Technique

If the fundamental component is set to a predetermined value and the (N-1) harmonics are set to zero, the following equation set is obtained with N equations and N variables.

$$\begin{bmatrix} 2\cos(\alpha_1) & -2\cos(\alpha_2) & \cdots & 2(-1)^{N+1}\cos(\alpha_N) \\ 2\cos(5\alpha_1) & -2\cos(5\alpha_2) & \cdots & 2(-1)^{N+1}\cos(5\alpha_N) \\ \vdots & \vdots & \ddots & \vdots \\ 2\cos(x\alpha_1) & -2\cos(x\alpha_2) & \cdots & 2(-1)^{N+1}\cos(x\alpha_N) \end{bmatrix} = \begin{bmatrix} 1+\frac{\pi b_1}{2V_{dc}} \\ 1 \\ \vdots \\ 1 \end{bmatrix} \tag{3.14}$$

where

$$x = 3N - 2 \tag{3.15}$$

$$0 < \alpha_1 < \alpha_2 < \ldots < \alpha_N < \frac{\pi}{2} \tag{3.16}$$

Converter switching frequency, f_c, is expressed as

$$f_c = (2N+1)f_1 \tag{3.17}$$

where f_1 is the frequency of the fundamental component.

The equation set 3.14, 3.15, and 3.16 should be solved simultaneously to obtain a solution set. Since N equations are nonlinear, they cannot be solved with

analytical methods. Iterative methods and evolutionary search algorithms are needed.

3.3.1.2 TLN2 Technique

As can be seen from the line-to-neutral voltage in Figure 3.6, there are even number of notch angles present in the waveform, which results in elimination of odd number of total harmonics via SHEM since one notch angle is used to control the fundamental component [46, 47].

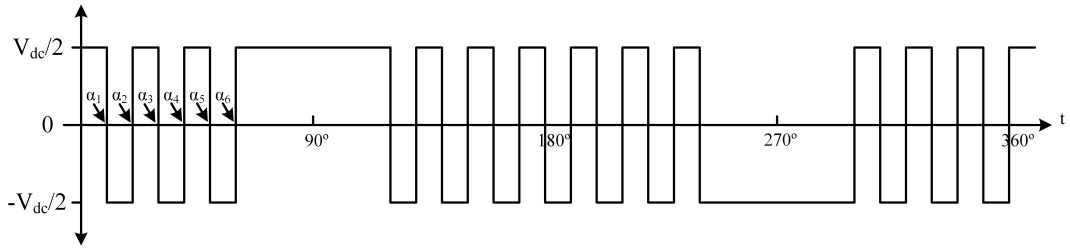


Figure 3.6: Line-to-Neutral Voltage for TLN2 Technique

b_n is found for odd harmonics by using Figure 3.6 and Equation 3.12:

$$b_n = \frac{4}{n\pi}\frac{V_{dc}}{2}\left[1 + 2\sum_{k=1}^{N}(-1)^k \cos(n\alpha_k)\right] \tag{3.18}$$

If the fundamental component is set to a predetermined value and the (N-1) harmonics are set to zero, the following equation set is obtained with N equations and N variables.

$$\begin{bmatrix} 2\cos(\alpha_1) & -2\cos(\alpha_2) & \cdots & 2(-1)^{N+1}\cos(\alpha_N) \\ 2\cos(5\alpha_1) & -2\cos(5\alpha_2) & \cdots & 2(-1)^{N+1}\cos(5\alpha_N) \\ \vdots & \vdots & \ddots & \vdots \\ 2\cos(x\alpha_1) & -2\cos(x\alpha_2) & \cdots & 2(-1)^{N+1}\cos(x\alpha_N) \end{bmatrix} = \begin{bmatrix} 1 - \frac{\pi b_1}{2V_{dc}} \\ 1 \\ \vdots \\ 1 \end{bmatrix} \tag{3.19}$$

where

$$x = 3N - 1 \tag{3.20}$$

$$0 < \alpha_1 < \alpha_2 < \ldots < \alpha_N < \frac{\pi}{3} \tag{3.21}$$

Converter switching frequency, f_c, is expressed as

$$f_c = (2N + 1)f_1 \tag{3.22}$$

where f_1 is the frequency of the fundamental component.

3.3.1.3 TLL Technique

Line-to-line converter voltage, which has odd quarter-wave symmetry, is depicted in Figure 3.7 for TLL technique.

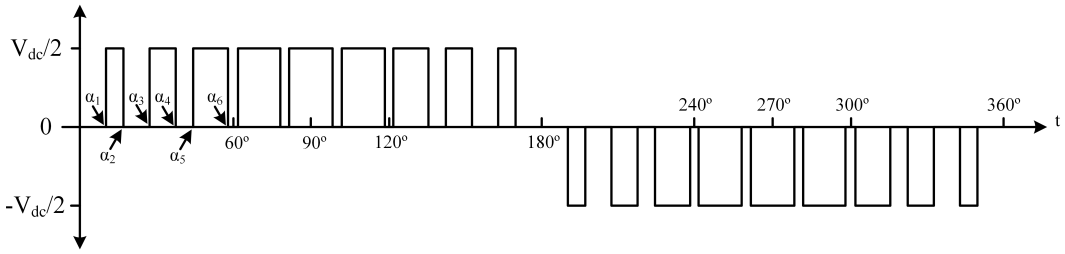


Figure 3.7: Line-to-Neutral Voltage for TLL Technique

b_n is found for odd harmonics by using Figure 3.7 and Equation 3.12:

$$b_n = \frac{4}{n\pi}\frac{V_{dc}}{2}\left[\sum_{k=1}^{2N}(-1)^{k+1}\cos(n\alpha_k)\right],\ N\ is\ even \tag{3.23}$$

If the fundamental component is set to a predetermined value and the (N-1) harmonics are set to zero, the following equation set is obtained with N equations and N variables.

$$\begin{bmatrix} \cos(\alpha_1) & -\cos(\alpha_2) & \cdots & -\cos(\alpha_{2N}) \\ \cos(5\alpha_1) & -\cos(5\alpha_2) & \cdots & -\cos(5\alpha_{2N}) \\ \vdots & \vdots & \ddots & \vdots \\ \cos(x\alpha_1) & -\cos(x\alpha_2) & \cdots & -\cos(x\alpha_{2N}) \end{bmatrix} = \begin{bmatrix} \frac{\pi b_1}{2V_{dc}} \\ 0 \\ \vdots \\ 0 \end{bmatrix} \tag{3.24}$$

where

$$x = 3N - 1 \tag{3.25}$$

$$0 < \alpha_1 < \alpha_2 < \ldots < \alpha_N < \frac{\pi}{3} \tag{3.26}$$

The first 60° interval of the switching pattern is found by solving 3.24, 3.25, and 3.26, and the last 60° interval of the half cycle is the same as the first 60° interval. The 60° to 120° interval is acquired by folding the first and last 60° intervals around the 60° to 120° points. α_{N+1} and α_{2N} are obtained by folding symmetry [46, 47].

Although maximum obtainable fundamental converter voltage is 1 p.u. peak for 1 p.u. DC link voltage in TLN1 and TLN2 techniques, it is 0.85 p.u. peak for 1 p.u. DC link voltage in TLL technique. This reduction in fundamental voltage is a disadvantage of TLL technique. Hence, TLN1 and TLN2 techniques are preferred when implementing SHEM [46, 47].

3.3.2 Cost Function of the Problem

For the three-phase two-level grid-connected inverter under consideration, TLN1 technique is selected in order to eliminate six harmonics, specifically 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, and 19^{th}, which brings about a switching frequency of 750 Hz according to Equation 3.17. These are the lowest-order harmonics present in the output voltage waveform of the inverter since even order harmonics are not present if an odd quarter-wave symmetric pattern is used, and all triplen

harmonics are eliminated automatically in a three-phase three-wire system. For this system, the equation set to be satisfied is as follows:

$$b_1 = \frac{4}{\pi}\frac{V_{dc}}{2}\left[-1-2\sum_{k=1}^{7}(-1)^k\cos(\alpha_k)\right] = \hat{V_f} \tag{3.27}$$

$$b_5 = \frac{4}{5\pi}\frac{V_{dc}}{2}\left[-1-2\sum_{k=1}^{7}(-1)^k\cos(5\alpha_k)\right] = 0 \tag{3.28}$$

$$b_7 = \frac{4}{7\pi}\frac{V_{dc}}{2}\left[-1-2\sum_{k=1}^{7}(-1)^k\cos(7\alpha_k)\right] = 0 \tag{3.29}$$

$$b_{11} = \frac{4}{11\pi}\frac{V_{dc}}{2}\left[-1-2\sum_{k=1}^{7}(-1)^k\cos(11\alpha_k)\right] = 0 \tag{3.30}$$

$$b_{13} = \frac{4}{13\pi}\frac{V_{dc}}{2}\left[-1-2\sum_{k=1}^{7}(-1)^k\cos(13\alpha_k)\right] = 0 \tag{3.31}$$

$$b_{17} = \frac{4}{17\pi}\frac{V_{dc}}{2}\left[-1-2\sum_{k=1}^{7}(-1)^k\cos(17\alpha_k)\right] = 0 \tag{3.32}$$

$$b_{19} = \frac{4}{19\pi}\frac{V_{dc}}{2}\left[-1-2\sum_{k=1}^{7}(-1)^k\cos(19\alpha_k)\right] = 0 \tag{3.33}$$

where $\hat{V_f}$ is the peak value of the fundamental line-to-neutral voltage at the inverter output, V_{dc} is the input DC link voltage, b_n is the peak value of the n^{th} harmonic where $n = \{5, 7, 11, 13, 17, 19\}$, and α_k is the switching angle to be found where $k = \{1, 2, 3, 4, 5, 6, 7\}$.

Equation 3.27 can be rearranged in such a way that the right hand side of it is made zero. Defining the modulation index as

$$M = \frac{\pi\hat{V_f}}{2V_{dc}} \tag{3.34}$$

and rewriting the equations after simplifications, the following equation set is acquired:

$$T_1 = -1 - \left[2\sum_{k=1}^{7}(-1)^k \cos(\alpha_k)\right] - M = 0 \tag{3.35}$$

$$T_5 = -1 - \left[2\sum_{k=1}^{7}(-1)^k \cos(5\alpha_k)\right] = 0 \tag{3.36}$$

$$T_7 = -1 - \left[2\sum_{k=1}^{7}(-1)^k \cos(7\alpha_k)\right] = 0 \tag{3.37}$$

$$T_{11} = -1 - \left[2\sum_{k=1}^{7}(-1)^k \cos(11\alpha_k)\right] = 0 \tag{3.38}$$

$$T_{13} = -1 - \left[2\sum_{k=1}^{7}(-1)^k \cos(13\alpha_k)\right] = 0 \tag{3.39}$$

$$T_{17} = -1 - \left[2\sum_{k=1}^{7}(-1)^k \cos(17\alpha_k)\right] = 0 \tag{3.40}$$

$$T_{19} = -1 - \left[2\sum_{k=1}^{7}(-1)^k \cos(19\alpha_k)\right] = 0 \tag{3.41}$$

The cost function of the problem, and consequently, the fitness value of a switching angle set can be formulated by squaring the left hand sides of the equation set 3.35 – 3.41 and summing them as shown in Equation 3.42 below.

$$f = \mu(\gamma\, T_1^2 + T_5^2 + T_7^2 + T_{11}^2 + T_{13}^2 + T_{17}^2 + T_{19}^2) \tag{3.42}$$

where γ is the modulation index penalty and μ is the angle constraint penalty. It has been found that using a penalty for the first term in the fitness function, which concerns the modulation index constraint, helps the particles to satisfy the constraint for changing modulation index values in a better way. Another important constraint for the equation set 3.35 – 3.41 is

$$0 < \alpha_1 < \alpha_2 < \alpha_3 < \alpha_4 < \alpha_5 < \alpha_6 < \alpha_7 < \frac{\pi}{2} \tag{3.43}$$

A penalty approach is used for particles that do not obey this constraint, and their fitness function is multiplied by the angle constraint penalty. Therefore, they have higher fitness values, and the other particles do not tend to go towards

them. The fitness function has a minimum value of zero if switching angles found from the algorithm satisfy all the conditions in the equation set 3.35 – 3.41 and the angle constraint in Equation 3.43. By squaring the terms, all cost function terms are made non-negative; consequently, any solution set that does not satisfy the conditions will make the cost function have a positive value. Therefore, this cost function can be assigned as a fitness value to any particle in the PSO algorithm, and it can be deduced that any particle with a low fitness value will have a better switching angle set that is close to satisfying the conditions. A particle with zero fitness value will be the global solution of the problem.

Since the switching angles have to be found in a range between 0° and 90°, the particles that desire to go beyond this region with a high velocity should be prevented for the sake of finding feasible solutions. A part of the algorithm consists of this control which checks if any particle desires to go beyond the limits and sets the position value of that particle as the upper or lower boundary. The current velocity of this particle is also clamped to fit the boundary constraints since it affects the velocity of next time frame according to Equation 3.1.

The initial population of the swarm can be generated in different ways, which affect the performance of the algorithm immensely. An initial approach would be to distribute the particles in the [0°, 90°] region randomly. Although the particles incline to converge to the solution in this case, the speed of convergence is found to be slow. It has been seen that, setting only one particle as the solution of a previous problem, in which the modulation index was different than the current one, helps the solution be found with a faster speed rather than distributing all of the particles randomly. The solution space is not very wide for two-level inverters with SHEM as the control method since only the first equation in the equation set 3.35 – 3.41 changes due to changing modulation index and all the others are set to zero all the time. By setting one particle as the solution of a previous problem, the particles do not lose time for searching the solution space where the solution does not exist, and they directly go towards the feasible region.

3.3.3 Results of the PSO Algorithm

The PSO algorithm code used in this thesis is written in MATLAB environment. It is an improved version of the code developed by Donckels, which needed some changes for efficient FPGA implementation [48]. This code is applied to the problem upon the cost function formulation with the parameters shown in Table 3.2 below.

Table 3.2: PSO Algorithm Default Parameters

Parameter	**Symbol**	**Value**
Inertia weight	β	1
Cognition factor	c_1	2.8
Social factor	c_2	1.3
Constriction factor	K	0.729
Swarm size	s	250
Number of time frames	t	200
Modulation index penalty	γ	100
Angle constraint penalty	μ	10

Initially, some of these parameters have been found by a trial-and-error approach, and some of them are set as the suggested values by authors who investigated the algorithm in the literature. It has been seen the solutions found for changing values of modulation index have very low fitness values and satisfy all of the constraints with high performance. Table 3.3 shows the switching angle sets found for different modulation index values by the PSO algorithm code run on MATLAB software.

In Figure 3.8, the decadic logarithm of the fitness value of the switching angles given in Table 3.3 are shown for different values of modulation index. As can be seen, for a specific range ([0.9, 1]) of modulation index values, the minimum fitness value that can be reached is considerably high compared to other regions, meaning that there is no solution satisfying all of the constraints completely here. However, the solution corresponding to this nonzero fitness value is the best one to be used for the specified modulation index, which supports the argu-

ments presented for infeasible region of solution space presented in Section 2.4 of Chapter 2.

Table 3.3: Switching Angle Sets Found for Different Modulation Index Values by the PSO Algorithm

Modulation index	$\alpha_1(^\circ)$	$\alpha_2(^\circ)$	$\alpha_3(^\circ)$	$\alpha_4(^\circ)$	$\alpha_5(^\circ)$	$\alpha_6(^\circ)$	$\alpha_7(^\circ)$
0.10	0.477	14.509	14.917	60.827	74.184	75.775	89.284
0.20	1.231	14.690	15.541	61.657	73.419	76.620	88.571
0.30	1.861	14.558	15.809	62.490	72.634	77.437	87.867
0.40	2.516	14.490	16.124	63.332	71.860	78.271	87.177
0.50	3.187	14.476	16.469	64.188	71.101	79.133	86.510
0.60	3.867	14.507	16.830	65.071	70.367	80.038	85.887
0.70	4.555	14.584	17.204	66.014	69.690	81.032	85.355
0.80	5.248	14.704	17.590	67.152	69.202	82.259	85.061
0.90	5.921	14.877	17.987	69.878	70.349	84.638	85.886
0.95	5.939	14.890	17.933	69.237	69.242	88.774	89.267

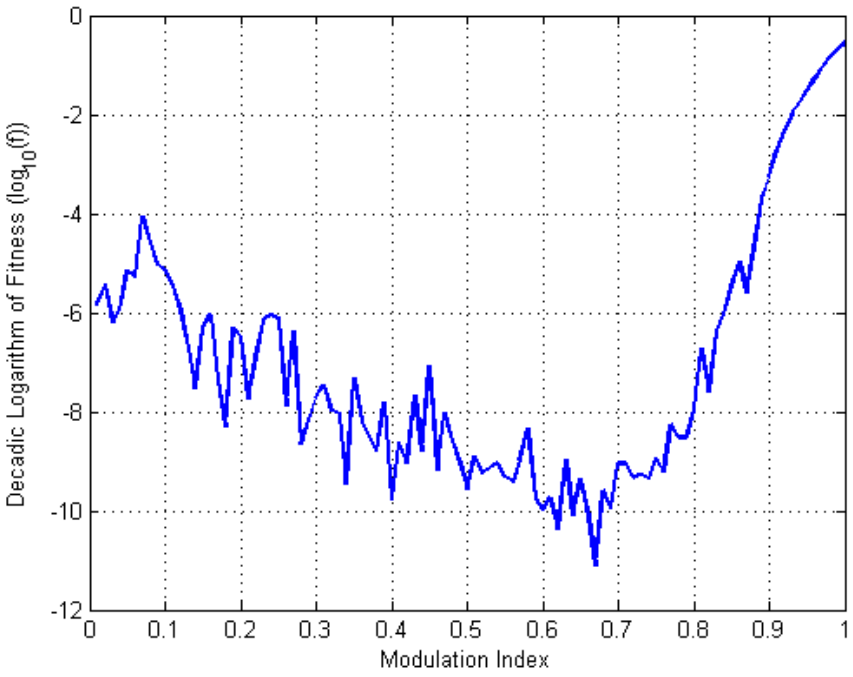


Figure 3.8: Decadic Logarithm of Fitness vs Modulation Index

3.3.4 Effects of Algorithm Parameters on the Solution

A further study has also been conducted to see the individual effects of the parameters on the convergence, speed, and performance of the algorithm. In order to compare the effects of parameters in equal circumstances, two modulation index values for which a solution to the equation set 3.35 – 3.41 exists are selected. For example, as can be seen from Figure 3.8, modulation index values of 0.6 and 0.8 have definitely solutions. The study is conducted in such a way that the modulation index change is from 0.8 to 0.6, and the solution of the former value is used as one of the individuals in the algorithm for the solution of the latter value. Although this individual has a fitness value 9.55×10^{-7} for 0.8 modulation index, it has a fitness value of 4 for 0.6 modulation index. The other individuals are generated randomly in the MATLAB environment and can be expected to have higher fitness values. Therefore, the algorithm has to decrease this global fitness value by finding the solution for the new modulation index.

For all of the tests conducted, one parameter is changed in a predetermined range, and the others are kept constant at the default values shown in Table 3.2. Then, the resulting global fitness value is saved, and the relation between the corresponding parameter is shown in the related figure. The fitness value is shown with its decadic algorithm since its variation is in a wide range. For the test related with the modulation index penalty, the target fitness value is set at 10^{-9}, and the number of time frames elapsed to reach this value is observed. The angle constraint penalty is not tested in this study since the effect caused by the variation in this parameter is seen to be very little compared to other parameters. Since the random search is at the heart of the PSO algorithm, slightly fluctuating results are acquired at each run of the algorithm; however, the trends in the graphs can be easily seen with the help of a moving average filter. In the following figures, both the actual and filtered data are shown to illustrate these trends resulting from the changes in parameters.

3.3.4.1 Inertia Weight

Figure 3.9 below shows the decadic logarithm of the global fitness acquired after the algorithm runs against different inertia weights between 0.05 and 2. As can be seen from the figure, an inertia weight of 0.6 gives the lowest fitness values in a specified number of time frames. For inertia weight values lower than 0.4 and higher than 1, the algorithm is not able to reach a solution since the corresponding fitness values are too high.

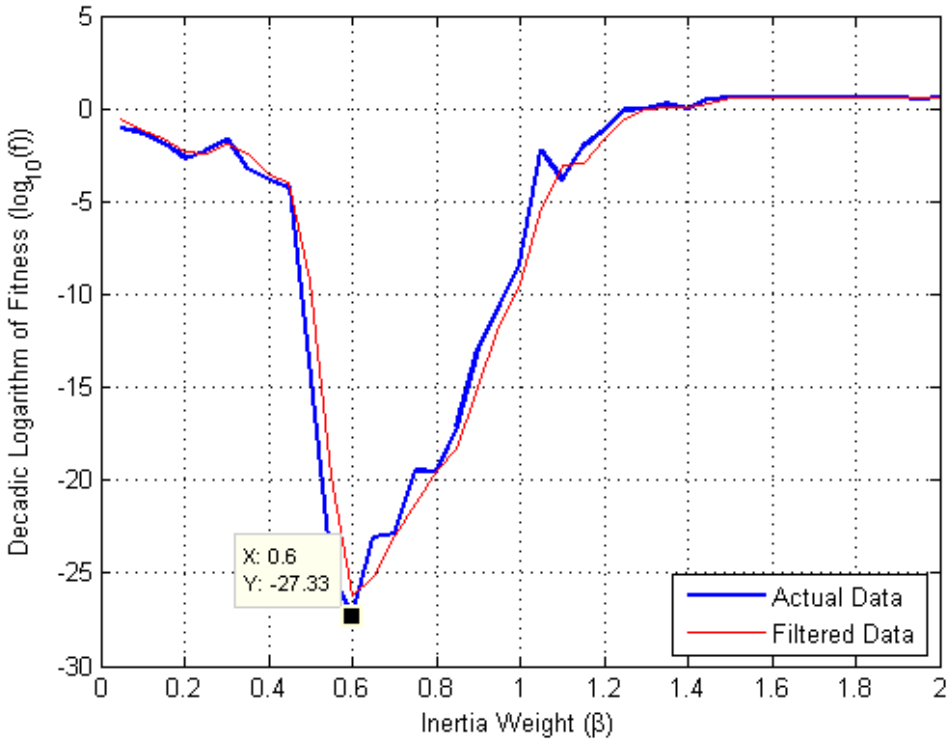


Figure 3.9: Decadic Logarithm of Fitness vs Inertia Weight

3.3.4.2 Cognition Factor

Figure 3.10 below shows the decadic logarithm of the global fitness acquired after the algorithm runs against different cognition factors between 0.1 and 4. Since it is suggested that the φ value, which is the sum of cognition and social factors in Equation 3.4, is selected to be greater than 4, the corresponding social factor is adjusted according to the changes in the cognition factor. If a constriction factor is used in the algorithm, φ is suggested to be set at 4.1; therefore, the sum of cognition and social factors is kept constant at 4.1 in this test. As can be seen from the figure, cognition factors between 2 and 2.5 give the lowest fitness values in a specified number of time frames.

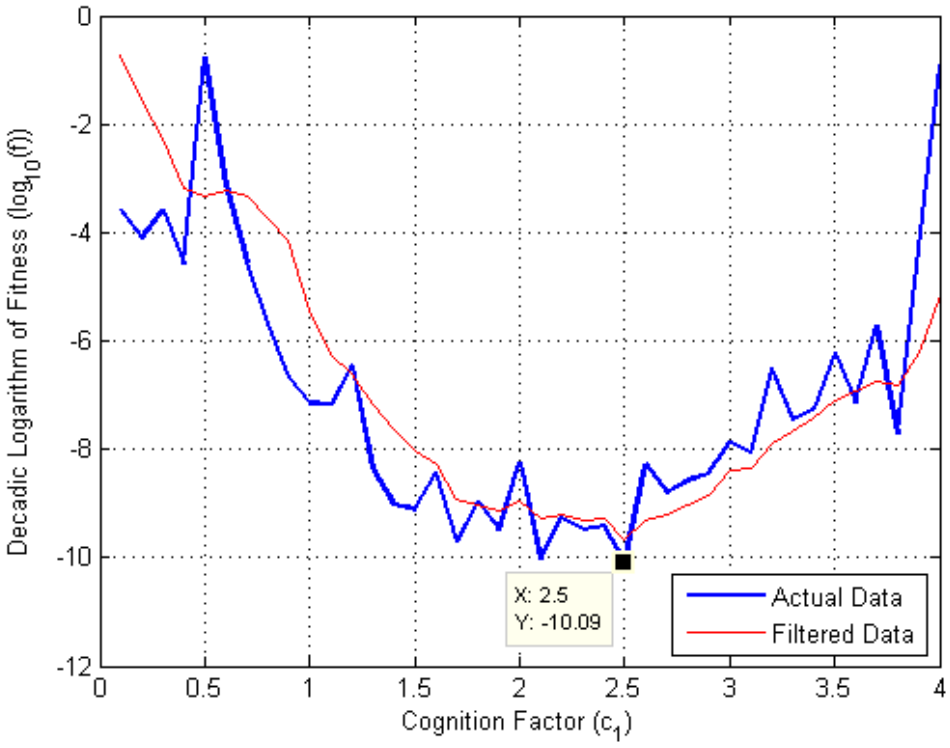


Figure 3.10: Decadic Logarithm of Fitness vs Cognition Factor

3.3.4.3 Social Factor

Figure 3.11 below shows the decadic logarithm of the global fitness acquired after the algorithm runs against different social factors between 0.1 and 4. This test is also conducted under the assumption that the sum of cognition and social factors is kept constant at 4.1. As can be seen from the figure, social factors between 2 and 2.5 give the lowest fitness values in a specified number of time frames.

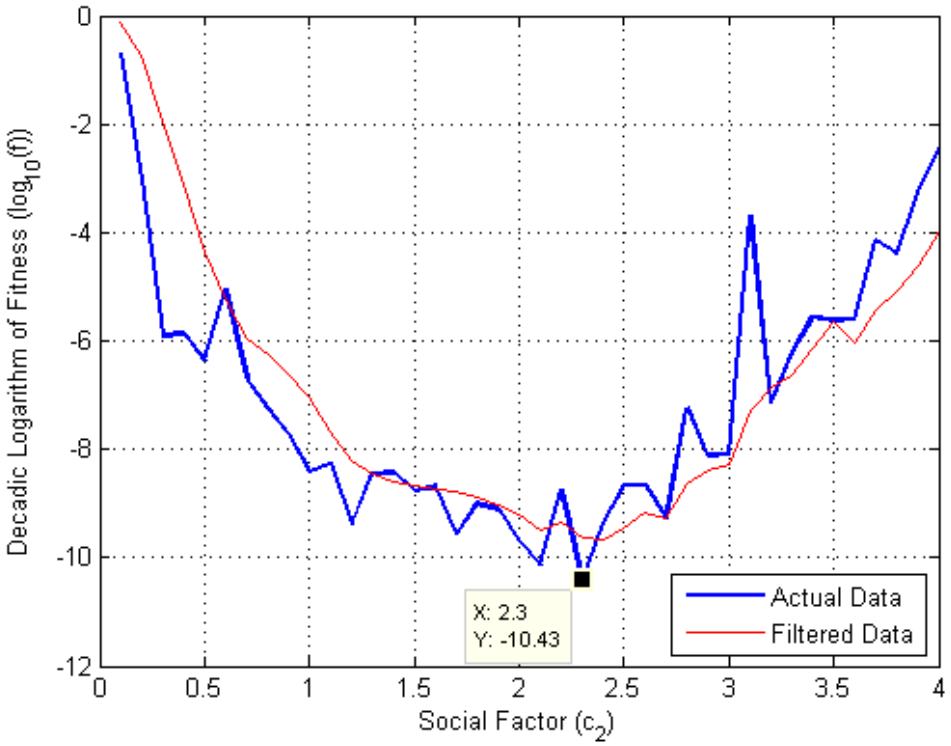


Figure 3.11: Decadic Logarithm of Fitness vs Social Factor

3.3.4.4 Swarm Size

Figure 3.12 below shows the decadic logarithm of the global fitness acquired after the algorithm runs against different swarm sizes between 50 and 2000. As can be seen from the figure, higher values of swarm size give lower fitness values in a specified number of time frames. However, using a high value of swarm size means more calculations should be done for assigning fitness values to each individual in the swarm in a specified number of time frames, and this increases the total time in which the algorithm completes. It can be seen that the results keep improving after swarm size of 250, but the changes in the corresponding switching angle set will be very little in practice. Therefore, a set corresponding to a global fitness value of 10^{-9} can be assumed to be the solution of the problem, and it is not necessary to use bigger swarm sizes in the algorithm.

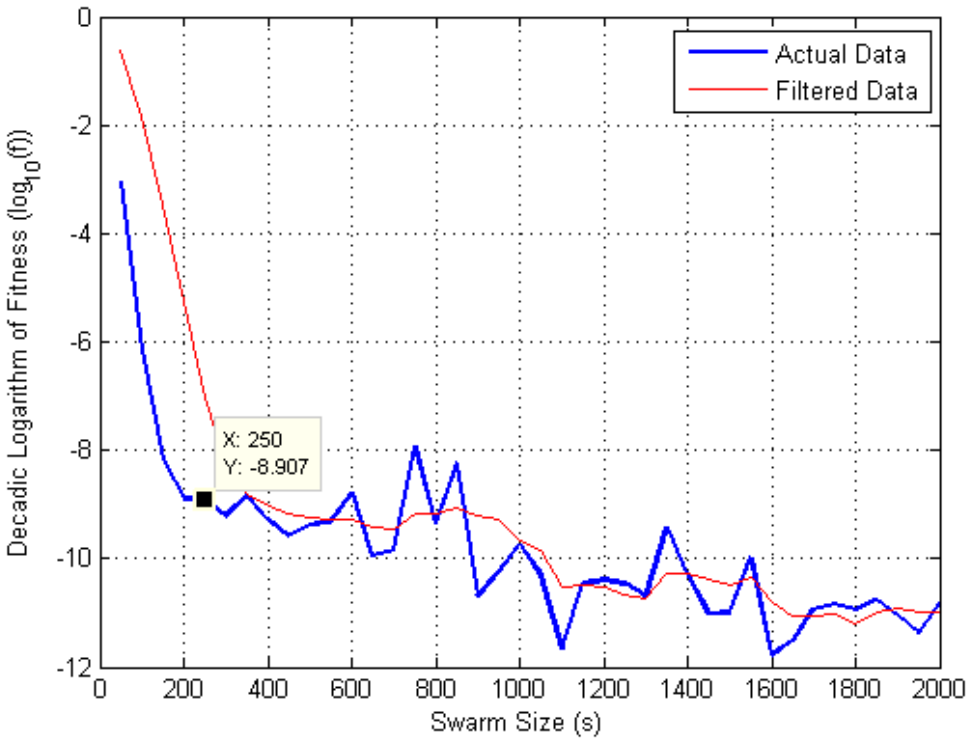


Figure 3.12: Decadic Logarithm of Fitness vs Swarm Size

3.3.4.5 Number of Time Frames

Figure 3.13 below shows the decadic logarithm of the global fitness acquired after the algorithm runs against different number of time frames between 10 and 400. As can be seen from the figure, 200 time frames gives a fitness value of 10^{-9}, which is an acceptable value for the resulting switching angle set to be the solution of the problem. If the number of time frames is increased beyond 200, the solution keeps getting better but the changes in the corresponding switching angles are very little. Therefore, it is not necessary to use higher numbers of time frames in order not to increase the total time in which the algorithm completes.

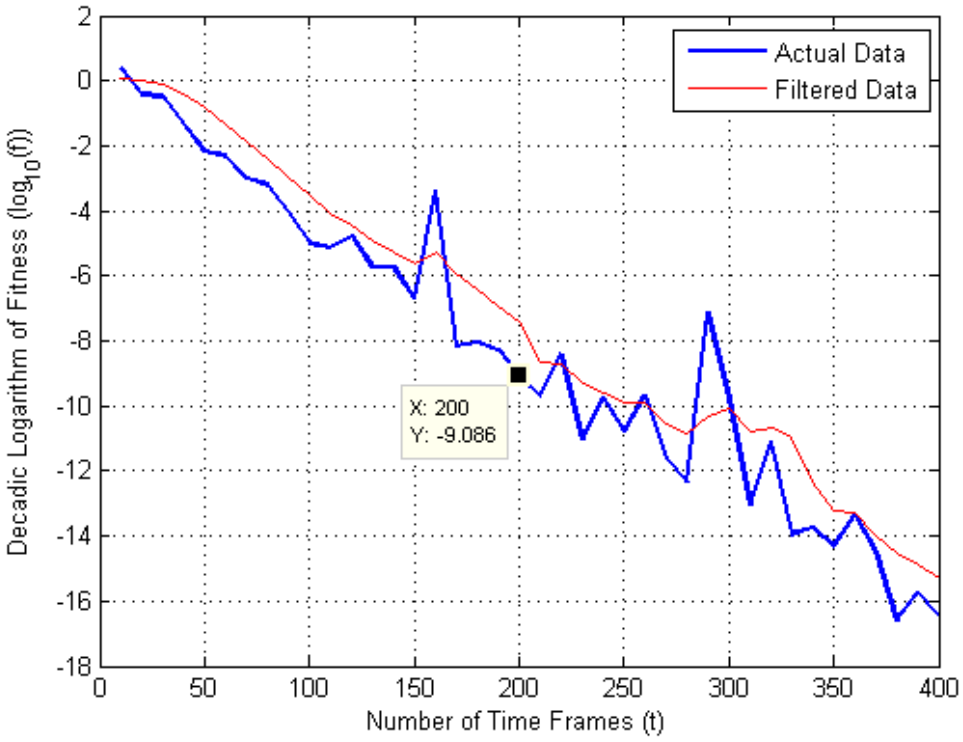


Figure 3.13: Decadic Logarithm of Fitness vs Number of Time Frames

3.3.4.6 Modulation Index Penalty

Figure 3.13 below shows the number of time frames elapsed to reach the global fitness value of 10^{-9} against different values of modulation index penalty between 1 and 400. Using a penalty coefficient of 1 means no penalty is incurred for the first term in Equation 3.42. As can be seen from the figure, this requires very high number of time frames to reach the desired fitness value. However, starting from a penalty coefficient of 10, the number of time frames required decreases drastically from values around 2500 to values around 250. Using higher values of the penalty coefficient does not result in more decrease in the time frames; therefore, any coefficient higher than 10 can be used for the algorithm to find the best switching angle set that fits the new modulation index value.

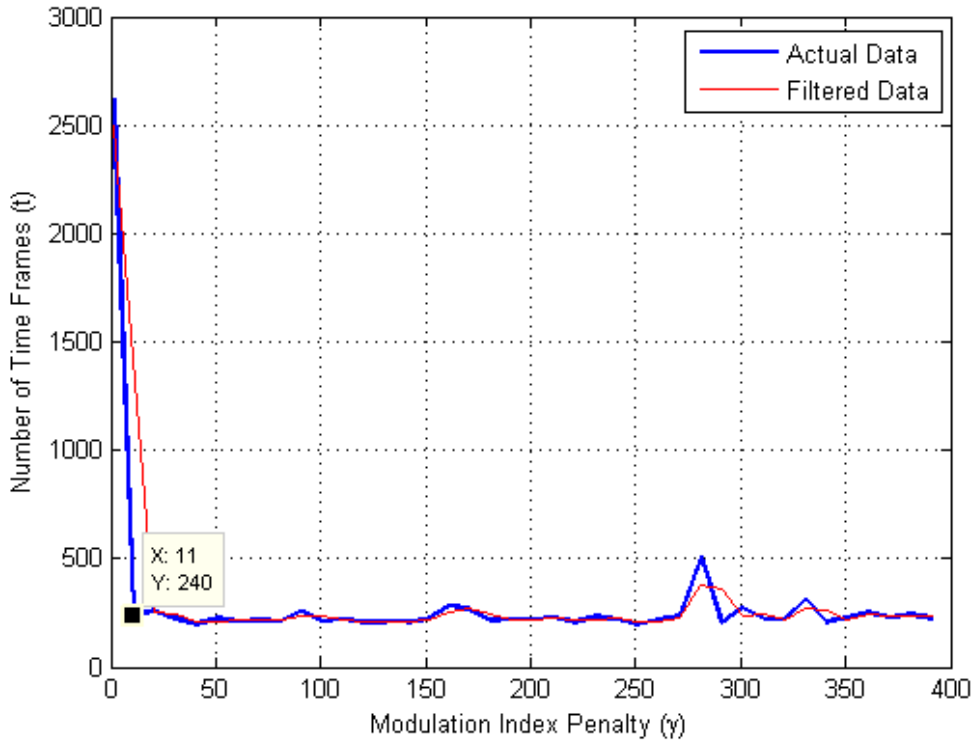


Figure 3.14: Time Frame vs Modulation Index Penalty

CHAPTER 4

FPGA IMPLEMENTATION OF ONLINE SHEM

Field programmable gate arrays (FPGAs) have drawn attention of power conversion industry in recent years because of their suitability for systems which require complex computation and fast processing time. In order to implement online application of SHEM, a powerful computing device that can handle huge lookup table and RAM operations at a very fast speed is needed since the control action is necessary to be taken in a time less than or equal to one period of grid voltage. For the grid-connected two-level three-phase inverter implementation in this thesis, FPGA is selected as the sole controller along with an analog-to-digital converter (ADC) microchip. In this chapter, the FPGA implementation of online SHEM by PSO algorithm will be investigated in detail.

4.1 Overview of FPGAs

4.1.1 Structure and Application Areas

FPGA mainly consists of combinatorial logic blocks distributed between arrays of flip-flops. For combinatorial blocks, the current state of the outputs are dependent only on the current state of the inputs. Several logic blocks can be generated from basic combinatorial blocks. Clocking is very important for FPGA blocks since the propagation delay between the inputs and outputs of a block should be within one clock period to avoid unstable results. FPGA modules consist of both programmable logic blocks, static Random Access Memory (RAM), Delay Locked Loops (DLLs), and Phase Locked Loops (PLLs). FPGA

chips can also easily be interfaced to other electrical components and signals. Figure 4.1 below shows the internal structure of a generic FPGA [49].

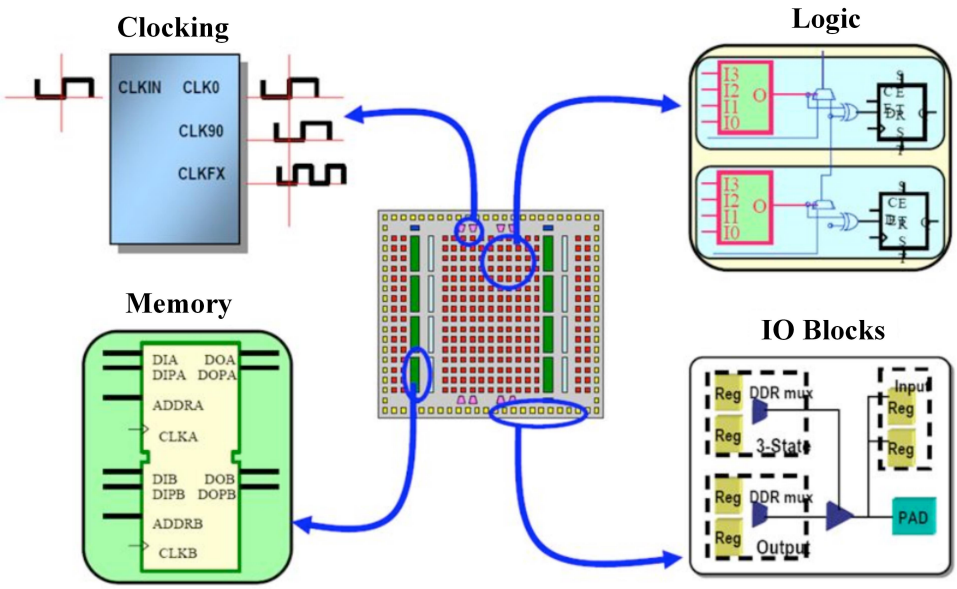


Figure 4.1: Internal Structure of a Generic FPGA [49]

Although FPGAs were only capable of having peripheral interfaces to main processors in the past, they can realize complex and demanding processes such as arithmetic architectures easily today [50]. FPGA is more advantageous than other analog and digital controllers since it can realize control algorithms quasi-instantaneously [51]. Utilization of FPGAs for motion control and power conversion has been popular for industrial applications recently. FPGAs have been used for PWM inverters, power-factor correction [52], DC/DC resonant converters [53], multilevel converters [54], matrix converters [55], soft switching [56], STATCOM [9,10,57], brushless DC motors, induction machine drives, switched reluctance machine drives, fuzzy logic control of power generators, and speed measurement [58,59]. FPGAs can also be used along with DSPs in applications where DSP realizes control blocks and FPGA realizes complex calculations. On the other hand, all control operations can be integrated into a single FPGA module to simplify operations [50].

4.1.2 Merits

FPGAs are not designed for particular operations, and the written code is not dependent on the hardware. Therefore, they can be configured to perform specific operations which traditional controllers cannot handle. Easier and shorter design flows, low-power requirement, and higher logic block density are some of the other notable advantages of FPGAs [59]. Even traditional controllers such as DSPs can be integrated as a core inside FPGAs. When compared to each other, resources of FPGAs outweigh those of other controllers [50].

Parallelism is the most important advantage for FPGAs over DSPs. Hardware operations can be realized concurrently in FPGAs. Figure 4.2 shows a finite impulse response (FIR) filter realized in conventional DSP device and FPGA. Although it takes 256 loops to process consecutive operations in DSPs, the calculations can be realized in 256 parallel operations in one clock cycle in FPGAs. Therefore, FPGAs can reach higher computation power than DSPs [49].

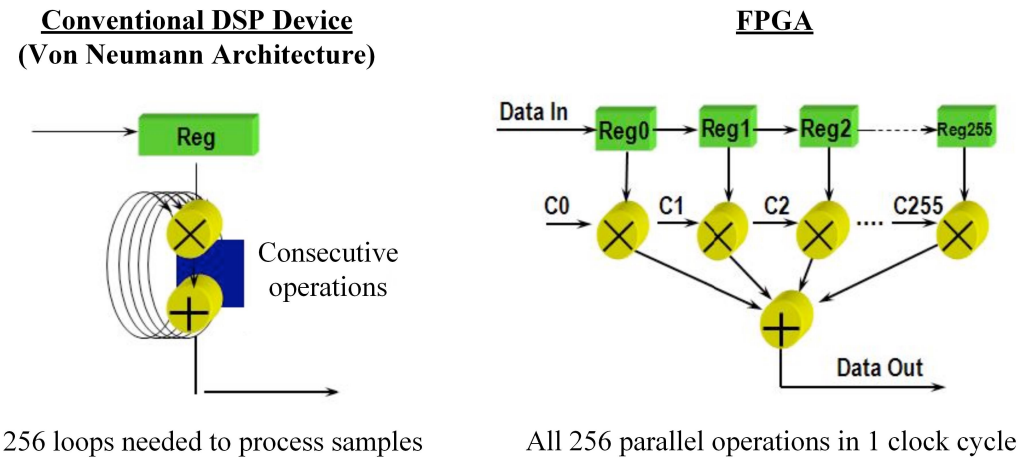


Figure 4.2: FIR Filter Comparison between DSP and FPGA [49]

The flexibility for trading off between area and speed is another advantage of FPGAs. Figure 4.3 shows how speed and cost optimization can be done in FPGAs by choosing more parallel or more serial operations [49].

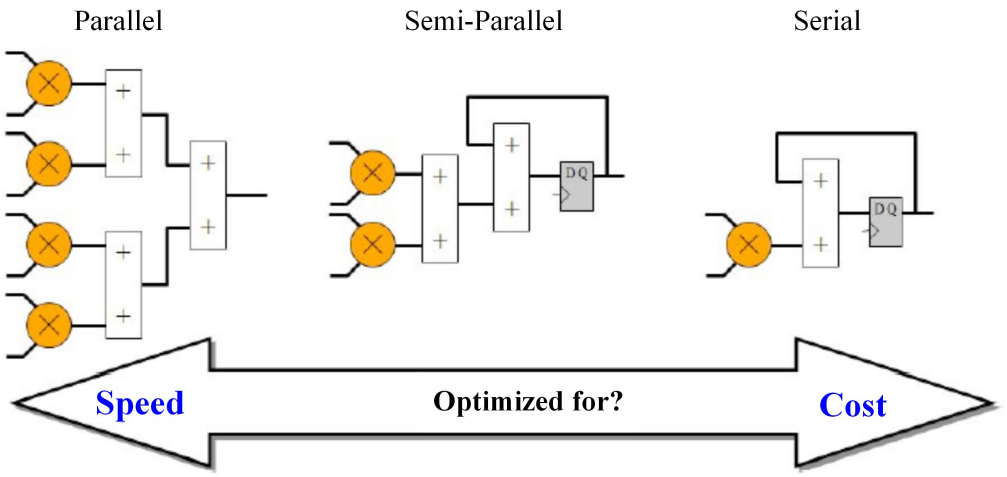


Figure 4.3: Speed/Area Trade-off in FPGAs [49]

4.1.3 Design Flow

The steps taken to turn initial ideas into final hardware in FPGAs can be called as the design flow. The designer needs to translate the design into hardware by using the software tools produced by FPGA vendors. The steps of design flow can be summarized as follows [49]:

- *Design entry*: In this step, the ideas about the design are transformed into software representation using Hardware Description Languages (HDLs). Main HDLs used by designers are Verilog and Very High Speed Integrated Circuit HDL (VHDL). HDLs does not work with sequential coding but they work with concurrent statements.

- *Synthesis*: The synthesis tool generates a netlist by using basic combinatorial logic blocks for specific FPGA model upon getting HDL code. Some advanced optimization tools can also be applied to enhance the timing performance and decrease propagation delays for the design.

- *Place and route*: The placer places the logic blocks according to the netlist and the router interconnects these blocks by considering the timing constraints. The system clock frequency is very essential in the design, and it depends on an optimized routing process.

- *Bit stream generation*: FPGAs are programmed by receiving a bit stream, and it is created in a single file once the place and route operation is over [49].

In this design flow, the first step requires the effort of the designer, and the others are realized by the software packages offered by FPGA vendors. Moreover, using abstract blocks and schematics for the design entry has been popular for designers recently. These blocks can also be simulated by some software packages, and hardware co-simulation between the computer and the FPGA module is also possible. The connection can be made via a Joint Test Action Group (JTAG) or Ethernet connection. This enables the designer to see the real system clock frequency and possible errors in the design entry [49].

4.1.4 Fixed-Point Arithmetic

In FPGA designs, high performance operations can be realized via fixed-point representation although floating point design can also be used. Table 4.1 shows some examples of fixed-point arithmetic using two's complement representation of signed numbers with three integer bits and three fractional bits [49].

Table 4.1: Examples of Two's Complement Signed Fixed-Point Arithmetic

Digit Worth						**Decimal Value**
$-(2^2)$	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	
-4	2	1	0.5	0.25	0.125	
0	0	0	0	0	1	0.125
0	0	0	0	1	0	0.25
1	0	1	0	0	0	-3.0
1	1	0	0	0	1	-1.875
1	1	1	1	1	1	-0.125

The main advantage of fixed-point arithmetic is that the bus widths can be shortened according to the resource requirements in the FPGA. As more and more operations are realized on a signal, its width increases and it will be full

of useless precision information. More importantly, timing constraints may not be satisfied for a system with wide buses. Therefore, the width of the buses are controlled via truncation and rounding. In truncation, useless fractional bits are dropped in the signal bus whereas in rounding, a '1' bit is added to the most significant bit of the ones to be dropped before truncation, which is explained in Figure 4.4 below [49].

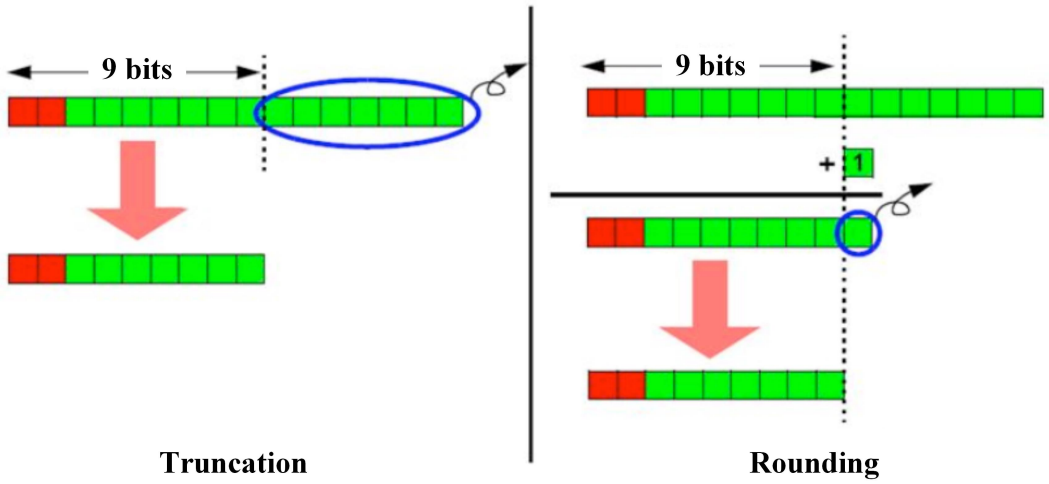


Figure 4.4: Truncation vs Rounding in Fixed-Point Representation [49]

4.2 Implemented FPGA Code

In this thesis work, particle swarm optimization is applied to SHEM equations to find the switching angle set that eliminates the 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, and 19^{th} harmonics at the output voltage of a VSI with variable DC link voltage input. This application is implemented in an FPGA as a real-time calculation, which makes it possible to update switching angle sets for changing values of input DC link voltage without using a lookup table. This work is applied on a VSI which is implemented for a PV application. For FPGA module, XEM6010-LX150 USB 2.0 integration module of Opal Kelly is used. This module contains Xilinx Spartan-6 XC6SLX150-2FGG484 FPGA with the specifications listed in Table 4.2 [60].

In this section, the FPGA modules used in the coding will be elaborated. The

schematic of the VSI control blocks implemented in FPGA is depicted in Figure 4.5. FPGA calculation results acquired from hardware co-simulation and the waveforms acquired from experimental work for the VSI will be given in the next chapter.

Table 4.2: Specifications of XEM6010-LX150 Module

Feature	**XEM6010-LX150**
Slice Architecture	4 6-LUT, 8 DFF
Slices	23,038
DFFs	184,304
Distributed RAM	1,355 kB
Block RAM	4,824 kB
MULT/DSP	180
Memory Controller Block	Yes
PLLs	Yes (6 CMT)
On-Board Memory Banks, Width	128 MB DDR2 One, x16
Peak Memory Bandwidth	10 GB/s

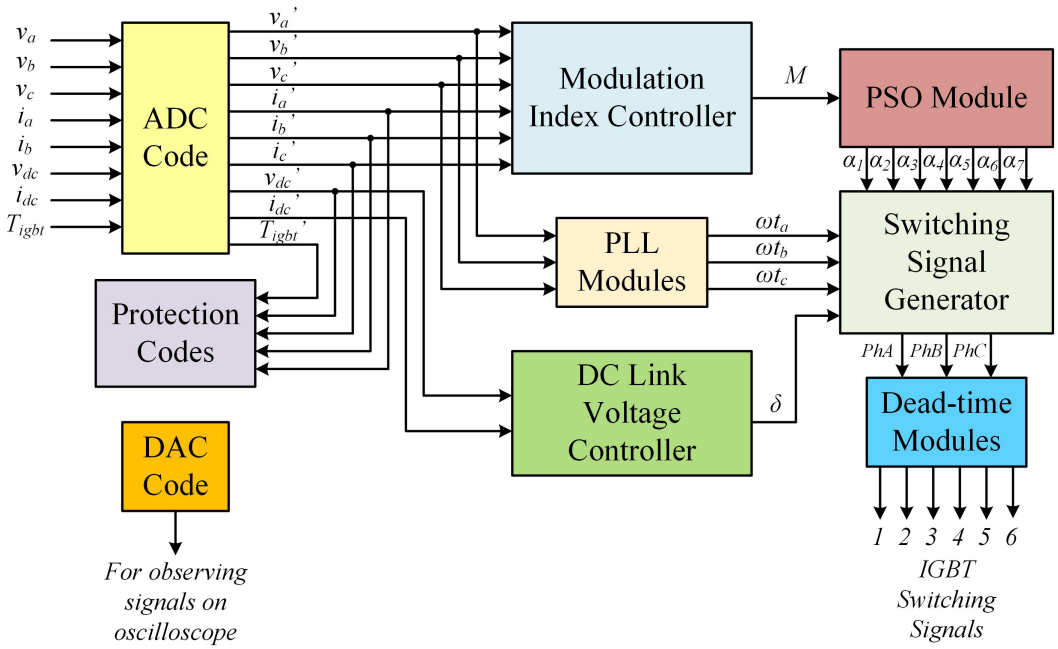


Figure 4.5: Schematic of the VSI Control Blocks Implemented in FPGA

4.2.1 PSO Module

As explained in the previous section, high-performance applications can be realized sufficiently by using enough bits in fixed-point representation. Therefore, fixed-point library is extensively used in the VHDL code written for this application. VHDL is selected instead of Verilog language in this work since it is a strongly typed language, has the ability to define custom types, has natural coding style for asynchronous resets, and logical statement endings are clearly marked. On the other hand, Verilog is a weakly-typed language, has no sensitivity lists, no support of custom types, has confusing signal declarations, confusing language conventions for beginners, and reduced support for asynchronous signals [61].

The main advantage of FPGAs over conventional DSPs is to exploit parallelism, and it is used wherever it is possible in the written code. As can be remembered from Equation 3.42 generated for the cost function of the SHEM switching angles, there are 49 cosine terms for elimination of six harmonics. For these cosine terms, a lookup table is used for cosine values of angles, and the RAM module corresponding to this lookup table has been replicated 49 times for all the cosine results to be acquired concurrently at one clock cycle. If it is considered that there are at least 250 particles in the swarm, and each of them requires 49 cosine terms to calculate the fitness value resulting from the cost function, exploitation of parallelism is essential to achieve fast calculation of desired switching angles.

The PSO algorithm needs two random numbers between 0 and 1 to update the velocities of individual particles and, in turn, to realize random searching of particles in the search space, as given in Equation 3.1. For this reason, a random number generation should be used in VHDL. A random number generator is designed to create a sequence of numbers without any pattern. There are two main methods used to generate random numbers, which are true random number generators (TRNGs) and pseudo random number generators (PRNGs). TRNGs use measurements from random physical phenomenon to generate random numbers. PRNGs, on the other hand, uses mathematical algorithms to generate random number sequences with long periods by using an initial "seed".

For this thesis work, PRNG is implemented. PRNGs generate random number sequences which repeat itself after some point; therefore, they are not completely random. The maximum period of the sequence is set by the initial seed. As the length of this initial seed increases, longer random sequences can be created [62].

A linear feedback shift register (LFSR) is a sequential shift register which produces binary random numbers with a determined periodic sequence. LFSRs can generally be implemented in a more optimized way than other methods in the FPGAs. The outputs of some registers are XORed to provide input for the next register, and the last register gives feedback for the XORs. The specific position of XOR inputs are called "taps" and the position of the taps determine the number of random numbers in the sequence. Figure 4.6 shows a diagram of an eight bit LFSR. In the VHDL code, a 12-bit LFSR is used. This LFSR produces pseudo-random numbers in a sequence which repeats itself after $2^{12} - 1 = 4095$ numbers if a certain tap setting, which yield the maximum length of sequence for the given registers, is used. According to this, the taps are taken from the 1^{st}, 4^{th}, 6^{th}, and 12^{th} registers [63].

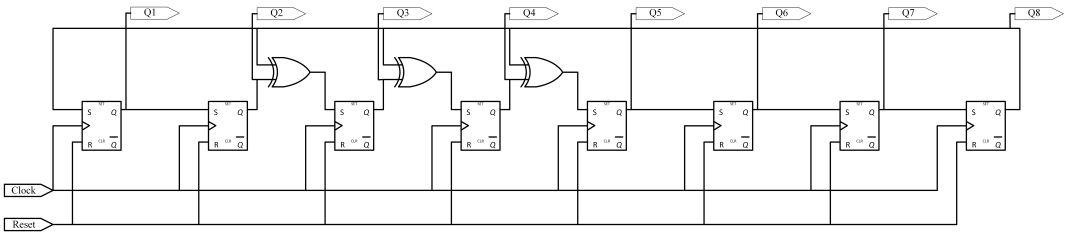


Figure 4.6: Diagram of an 8-bit LFSR

During the hardware co-simulation, it has been found that the FPGA code is working at 10 MHz clock frequency without any calculation errors, and the RAM blocks used in the modules can be run at 30 MHz clock frequency at most. These frequencies are the best ones at which propagation time does not affect the running processes; otherwise, if clock frequencies are increased, the calculations for fitness and velocity of the particles cannot be finished in the given period of time. As found in Section 3.3.4 of Chapter 3, a swarm consisting of 250 particles with 200 time frames gives satisfactory results for the PSO algorithm. During implementation of PSO, one time frame is realized in two sections. In the first

section, the fitness value of each particle, in other words, the cost function value of each switching angle set is calculated at each rising edge of 10-MHz clock. Moreover, personal best switching angle set of each particle is kept in memory along with its fitness value, which helps to compare the qualification of each particle with its personal historical record. The global best switching angle of the current time frame is also kept in memory and updated at each rising edge of the clock upon the comparison of stored fitness value of the particle with that of others. After 250 clock cycles, the personal best value of each particle and the global best value of the current time frame is decided.

At this point, the calculation of velocity for each particle can start since *pbest* and *gbest* is known for each of them. The velocity vector has a length of 7 since there are 7 angles to be found, and the velocity should be calculated for each of them. At each rising edge of clock, all 7 components of the velocity vector of one particle are calculated concurrently, and its position in the next time frame is found. The velocity is also updated according to the situation in which the particle goes beyond the boundaries of the problem. After another 250 clock cycles, the next time frame with new positions of each particle is generated, and one iteration is thus complete in 500 clock cycles or 50 μs. If 200 time frames are used for the algorithm, the switching angle set that eliminates the specified harmonics is found in 10 ms. Figure 4.7 below summarizes the mindset behind the PSO implementation in the VHDL code.

As mentioned in the previous chapter, the initialization of the swarm can be done randomly or by utilizing the constraints defined for the problem. According to Equation 3.43, the switching angles should be found in an increasing order with the next angle being bigger than the previous one. According to this condition, it is useless to search the first switching angle near 90° or the last switching angle near 0°. Therefore, the range [0°, 90°] has been divided into 7 segments, and each segment is divided into 250 sections linearly. If the swarm is initialized with this lattice structure, shown in Figure 4.8, the performance of the algorithm increases considerably.

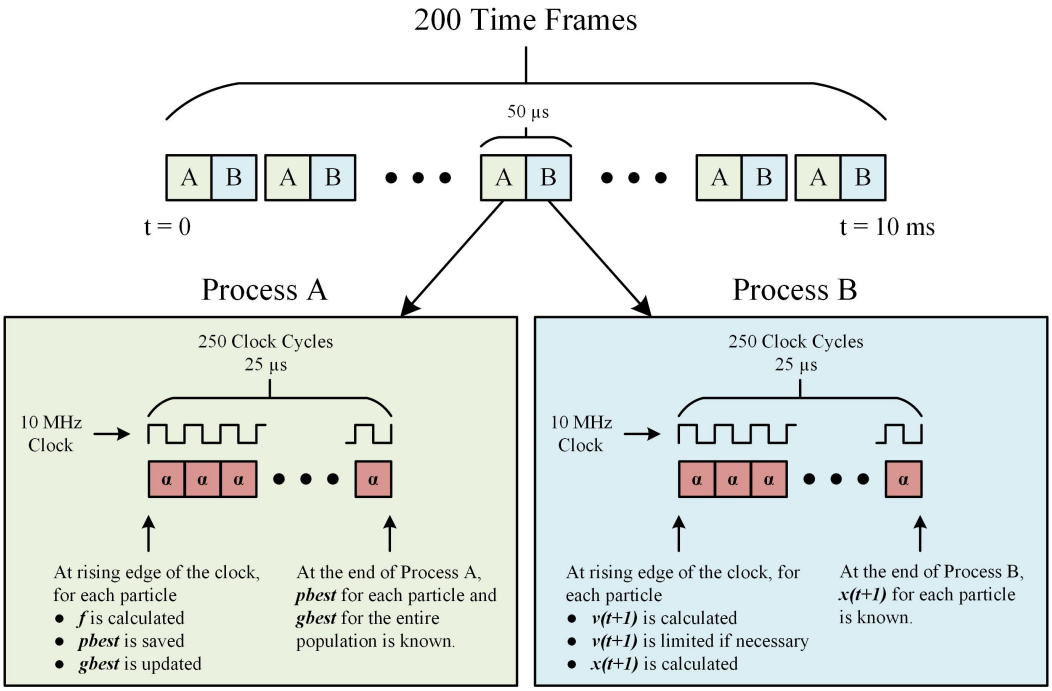


Figure 4.7: Mindset Behind the PSO Module in the VHDL Code

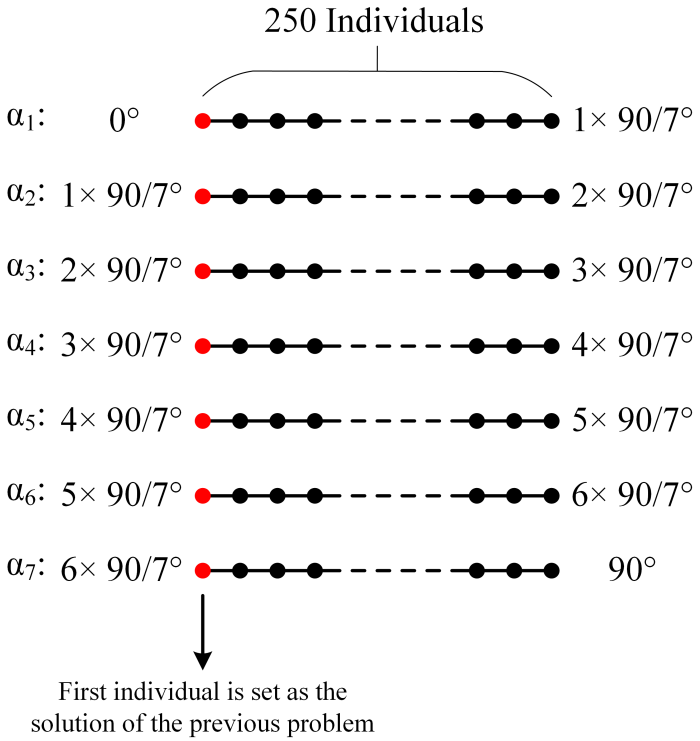


Figure 4.8: Lattice Structure Used for Initialization of the Population

The PSO module written in VHDL is synthesized and implemented, and its programming file is generated on a computer. Table 4.3 shows the device utilization summary report for only this module taken from the Xilinx ISE Design Suite software. The program gives the area constraint ratio for this code as 12 %, which is an indicator of how much area is used in the FPGA just for PSO module.

Table 4.3: Device Utilization Summary Report for PSO Module

Slice Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	5080	184304	2 %
Number of Slice LUTs	8142	92152	8 %
Number of Fully-Used LUT-FF Pairs	2652	37683	7 %
Number of Bonded IOBs	24	338	7 %
Number of Block RAM/FIFO	84	268	31 %
Number of BUFG/ BUFGCTRL/BUFHCEs	2	16	12 %
Number of DSP48A1s	105	180	58 %

If the VHDL code is synthesized as a whole with other modules included, the device utilization summary report is as given in Table 4.4 with an area constraint ratio of 41 %. As can be seen from this ratio, it can be deduced that there is still much space in the FPGA, which makes it possible to eliminate more than six harmonics in the output voltage waveform of the inverter. However, the limitation for the number of harmonics to be eliminated online by the FPGA results from the number of DSP48A1s, which are basically modules that concern multiplication operations in the FPGA. As can be seen in Table 4.4, these modules are used up to 98 % in the FPGA implementation, and there is not much DSP48A1 module left for another harmonic to be eliminated in real time. One solution under these circumstances might be not to eliminate extra

harmonics in real time but to eliminate them with a lookup table. Moreover, the place and route settings in Xilinx ISE Design Suite can be adjusted for cost and speed trade-off in the FPGA.

Table 4.4: Device Utilization Summary Report for Entire VHDL Code

Slice Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	9920	184304	5 %
Number of Slice LUTs	32794	92152	35 %
Number of Fully-Used LUT-FF Pairs	5031	37683	13 %
Number of Bonded IOBs	57	338	16 %
Number of Block RAM/FIFO	104	268	38 %
Number of BUFG/ BUFGCTRL/BUFHCEs	3	16	18 %
Number of DSP48A1s	177	180	98 %

4.2.2 PLL Module

Since the implemented VSI is working as grid-connected, it is necessary to detect the phase and frequency of the grid in order to control the power flow. The phase locked loop (PLL) is a method to obtain phase and frequency information of the grid, which was first described in 1923 and 1932 [64]. Figure 4.9 shows the diagram of a three-phase synchronous reference frame PLL. The phase voltages v_a, v_b, v_c are acquired from the line voltages, and the stationary reference frame of the phase voltages are transformed via the Clark and Park transformations into a reference frame locked to the grid frequency. The angle θ is acquired by integrating the output of the PI control, which is the frequency command ω^*. If this frequency is the same as the grid frequency, the direct and quadrature axis voltages V_d and V_q become DC values depending on the value of θ. The error

between the direct axis reference voltage V_d^* and V_d is eliminated by setting V_d^* equal to zero with the help of the closed loop feedback. Therefore, the PLL output is synchronized with the grid voltage [65].

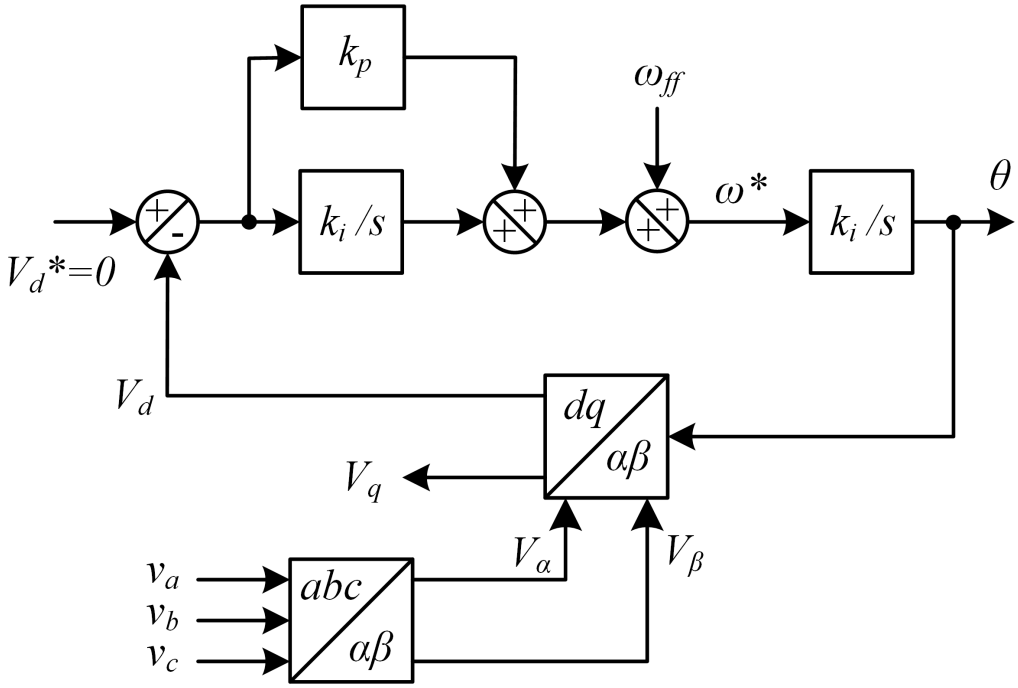


Figure 4.9: Three-Phase Synchronous Reference Frame PLL Diagram

The PI control for PLL is realized as a discrete-time control in the microcontrollers since continuous-time conditions cannot be realized digitally. The sampling time for PLL control loop is selected as 20 μs, corresponding to 50 kHz frequency. This is accomplished by getting the results from the PLL module at every 200 cycles since it is also fed by 10 MHz clock. The PLL module is also replicated for other two phases, thus realizing PLL of each phase separately. Figure 4.10 below shows the acquired PLL output for one of the phases along with the measured grid voltage to illustrate the performance of the implemented PLL code.

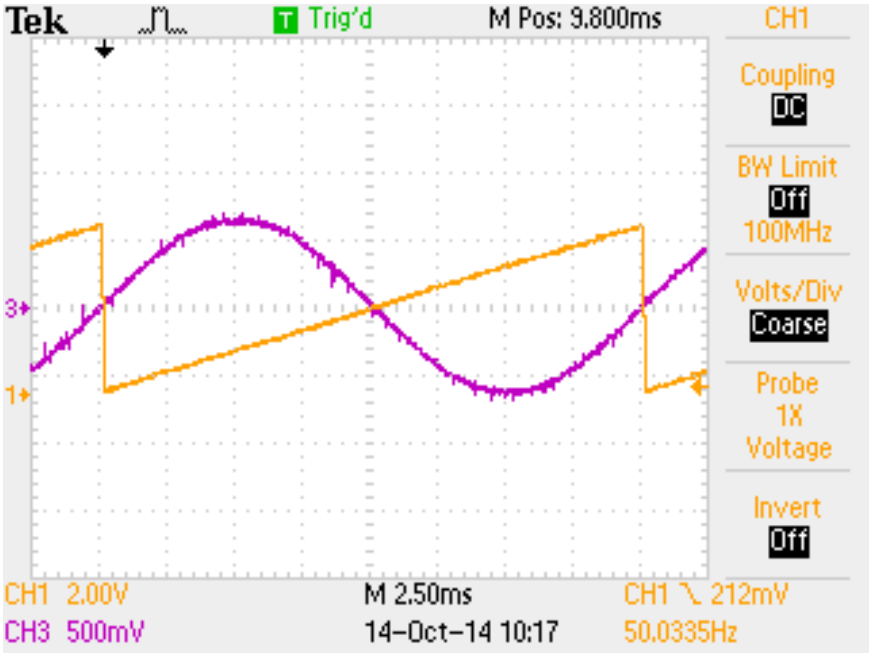


Figure 4.10: Acquired PLL Output from the Implemented FPGA Code

4.2.3 Modulation Index and DC Link Voltage Control Modules

Modulation index controller is a simple PI controller which tries to decrease the error between the desired and generated reactive powers. The reactive power generated by the inverter is calculated in this module by utilizing the instantaneous p-q theory [66]. The PI controller output is the modulation index value required for the inverter to inject the desired reactive power to the grid, and it is fed to the PSO module for generation of SHEM switching angles.

Active power control is realized by controlling the load angle δ in Equation 2.1. The error between measured and desired input DC link voltages is fed to a PI controller to determine the load angle. This control block also takes the measured input DC current to calculate the power input to the inverter for information.

The calculated SHEM switching angles, PLL module outputs for each phase, and the load angle information is fed to the switching angle generator. This block compares the switching angles with the PLL output modified by the load angle so that it is decided whether the output of one switching leg will be high or low

at any instant for each phase. If the output of one leg is high, the upper switch in this leg will be turned on, and the lower switch will be turned off. If it is low, the switching will be vice versa. This phase switching information is finally fed to the dead-time module which adds the required dead-time between upper and lower switching signals and distributes each signal to the corresponding switching semiconductor.

4.2.4 Dead-time Module

In practice, semiconductor switches have finite turn-off and turn-on times. When the upper or lower switch in one leg of the converter is turned off at the specified switching angle, the other one in the same leg is turned on with a delay, which is called a dead-time and conservatively chosen to avoid a "shoot-through" or cross-conduction current through the leg [8]. This dead-time is chosen to be 5 μs in the implemented code, and it can be clearly seen in Figure 4.11 below which shows the generated switching signals for the upper and lower switches in one leg.

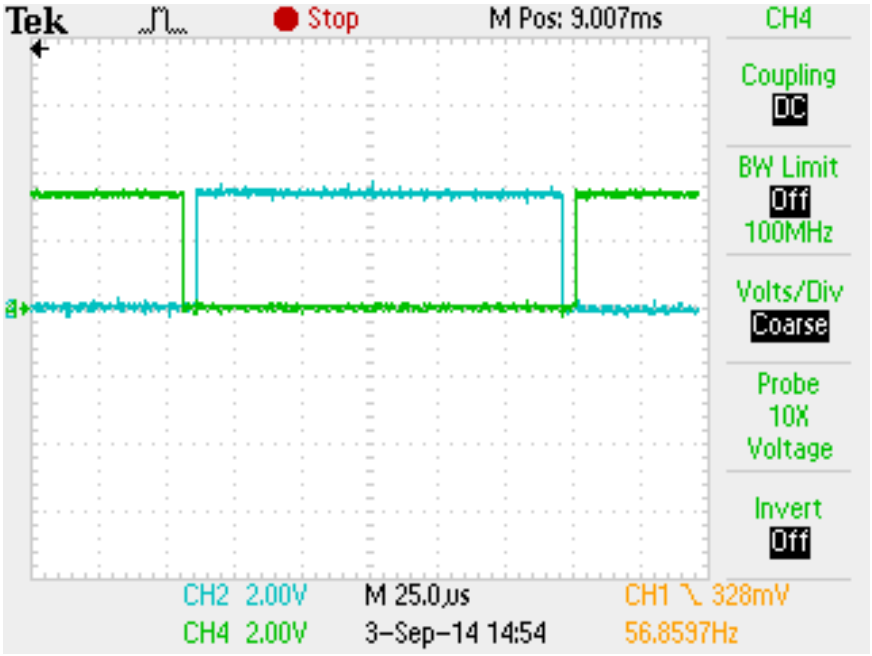


Figure 4.11: Implemented Dead-time between Upper and Lower Switching Signals

4.2.5 ADC and DAC Code Processes

This section and the next section concerns the processes devoted to other tasks in the VHDL code. Processes can be thought of consecutive code instructions realized at the rising or falling edges of the system clock. They are not separate modules but code snippets implemented in the main module and other modules.

The control of the inverter is realized by the FPGA, which is the sole controller in the inverter along with an analog-to-digital converter (ADC) microchip. The FPGA handles online SHEM application along with other control loop operations, so there is no need to use an extra DSP microcontroller. By this way, design complexity is simplified, and system costs are reduced. However, there is still need to include an ADC microchip in order to digitize analog signals for processing. For this microchip, ADC128S102 of Texas Instruments has been used. It is an 8-channel and 12-bit ADC which can have sampling rates from 500 ksps to 1 Msps. It is based on a "successive-approximation register architecture with an internal track-and-hold circuit" [67]. In order to send the converted signals from the analog side to the digital side through the isolation barrier on the printed circuit board (PCB), a digital isolator, ADUM2401 of Analog Devices, is used [68]. Digital-to-analog converters (DACs) are also included on the PCB to trace the variables in the FPGA code on the oscilloscope. For this purpose, AD5621 of Analog Devices is used as a 12-bit DAC [69].

One significant merit of FPGA coding is that it is not necessary to include any ADC, DAC or serial peripheral interface (SPI) library in the code as it is done for a DSP. The programmers are free to write their own protocol according to the needs of the ADC or DAC microchips used. Definition of digital buses with high number of bits is allowed in VHDL, and this fact is utilized in the ADC code written. The input serial data is taken for all eight inputs and stored into a 124-bit bus during data acquisition. At the end of this, the signals are extracted from the bus at once and converted to fixed-point representation to be used in the calculations. The converted signals for the inverter are three phase voltages, two line currents, input DC link voltage and current, and temperature information supplied from the switching device used. DAC code is also written

with a simplistic approach in VHDL without requiring any complex libraries.

4.2.6 Protection Code Process

In order to operate the grid-connected inverter in a safe manner, several protection measures were taken and implemented in the FPGA code. When some faulty condition occurs, the code interrupts the power conversion by pulling all of the switching signals to low and turning off the switches.

For current limit, temperature limit, and input DC link voltage limit, the protection code is implemented such that if the limits are exceeded constantly for 100 μs, the switching is interrupted for 10 s, and it starts again after this duration. Another measure taken for safe operation is to start switching of each leg at the zero crossings of the grid phase voltages consecutively. By this way, large start-up currents are prevented since large initial voltages are not applied to the output filter abruptly at the start of operation.

Another protection measure was taken for any wrong calculation that may result from the PSO algorithm. Although the PSO code is run for several modulation index values successfully, a part of the code checks if the condition specified in Equation 3.43 is satisfied or not for the resulting switching angles, and if any angle is bigger than the consecutive angle, the switching is interrupted. Moreover, the next calculation does not include this wrong angle set as one of its particles but that resulting from a correct calculation for another modulation index value; therefore, the algorithm is not trapped around the wrong switching angle set. The same procedure is applied if the resulting fitness value is found to be relatively high. This means that the algorithm has somehow trapped around a local minimum; thus, the initial population is forced not to include the wrong angle set but that resulting from a correct calculation for another modulation index value.

CHAPTER 5

RESULTS

In this chapter, the simulation and experimental results of the thesis work will be presented along with related figures, tables, and data. The chapter will be divided in two parts, first of which will be devoted to simulation results in which ISim simulations of the written FPGA code, real time hardware co-simulation of this code with XEM6010-LX150 FPGA module of Opal Kelly, and Simulink simulations of the three-phase two-level grid-connected inverter with variable DC link input will be presented. In the second part, the experimental results of the implemented grid-connected inverter will be given.

5.1 Simulations

5.1.1 ISim Simulations of FPGA Code

In order to generate the bit stream which is required for programming the flash memory of the FPGA, Xilinx ISE Design Suite program is used. The program includes an internal simulator called ISim which makes it possible to simulate the VHDL code written by configuring a testbench file which supplies the necessary input signals to the module in which the VHDL code is placed. The clock signals can be configured for any frequency specified by the programmer; however, this choice of system frequency is totally for simulation purposes and is subject to change according to the specifications of the real FPGA module. Therefore, system frequency is generally determined after hardware co-simulation. The testbench file can include non-synthesizable signal types and mathematical

functions such as trigonometric functions which can only be realized as lookup tables in the synthesizable code.

With the help of the ISim simulator, PSO module, PLL module, modulation index control code, and DC link voltage control code in the VHDL code were simulated clock by clock, and the errors were corrected. The other codes for ADC, DAC, and dead-time were tested with hardware co-simulation experimentally. ISim simulations were beneficial for PSO module at most because seeing the correct algorithm flow in the code was at utmost importance for the success of the thesis work.

Figure 5.1 shows a screenshot of the ISim simulator, in which it can be seen that all the signals and variables in the code can be traced clock by clock. The global best fitness value of the population in the PSO algorithm and the global best individual, namely, the best switching angle set that eliminates the specified harmonics can also be traced in the simulator. This is depicted in Figure 5.2 in which the gradual decrease in the global best fitness value (red) and consequent changes in global best switching angles (blue) are shown. Both values are represented in unsigned decimal representation of fixed-point numbers in order to notice the change easily. It is seen that the algorithm finds the switching angles for new modulation index value with specified PSO parameters successfully.

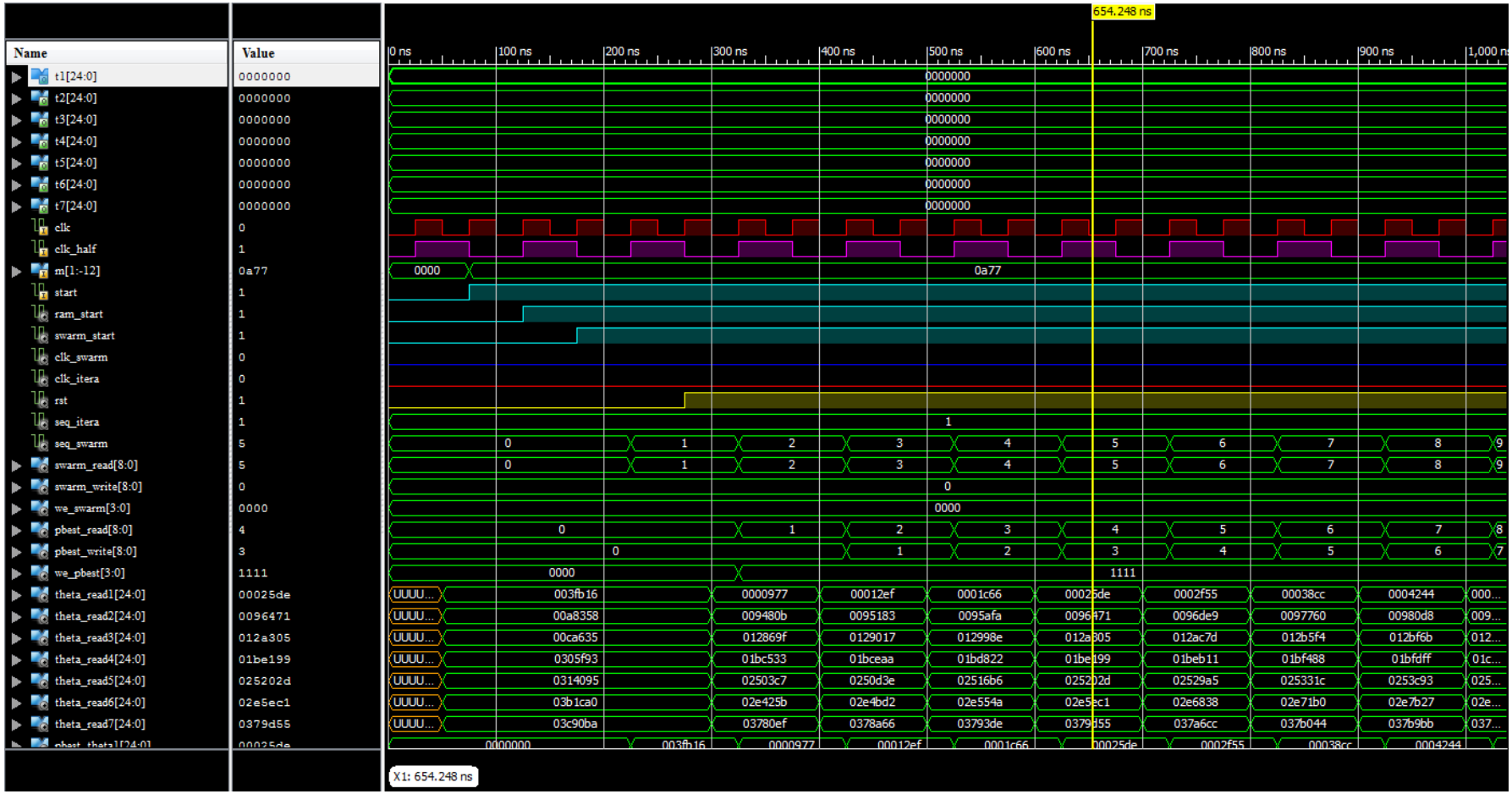


Figure 5.1: Screenshot of the ISim Simulator

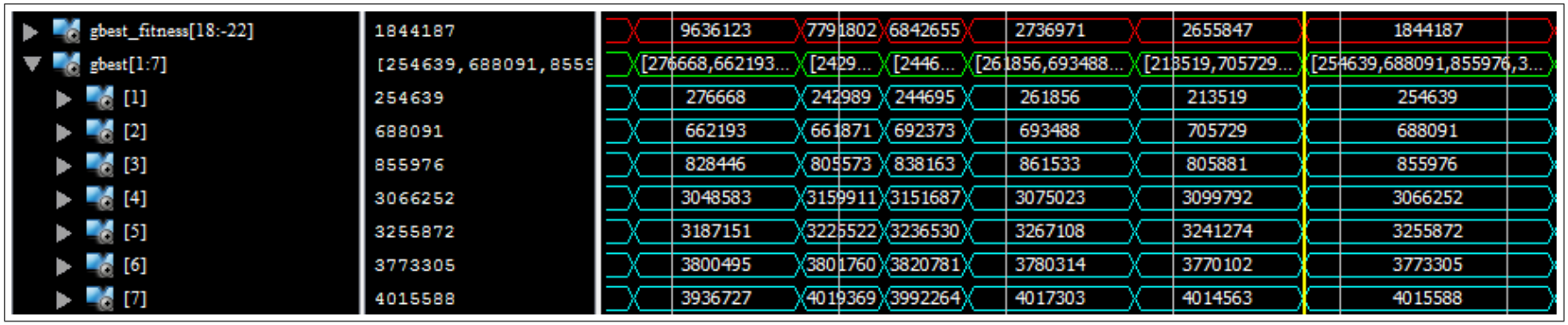


Figure 5.2: Gradual Decrease in Global Best Fitness and Consequent Changes in Switching Angles

5.1.2 Hardware Co-simulation of FPGA Code

Opal Kelly allows the tracing and changing values of signals used in the FPGA code with an interface called FrontPanel. This interface also allows programming the flash memory of the FPGA module and adjusting its clock settings. While the code is running in the FPGA, critical parameters, such as PI control parameter and limits, can be adjusted in real time, and the results can be seen directly on the system. This makes the design and implementation process easier and decreases the time allocated for testing considerably. Figure 5.3 below shows the FrontPanel interface.

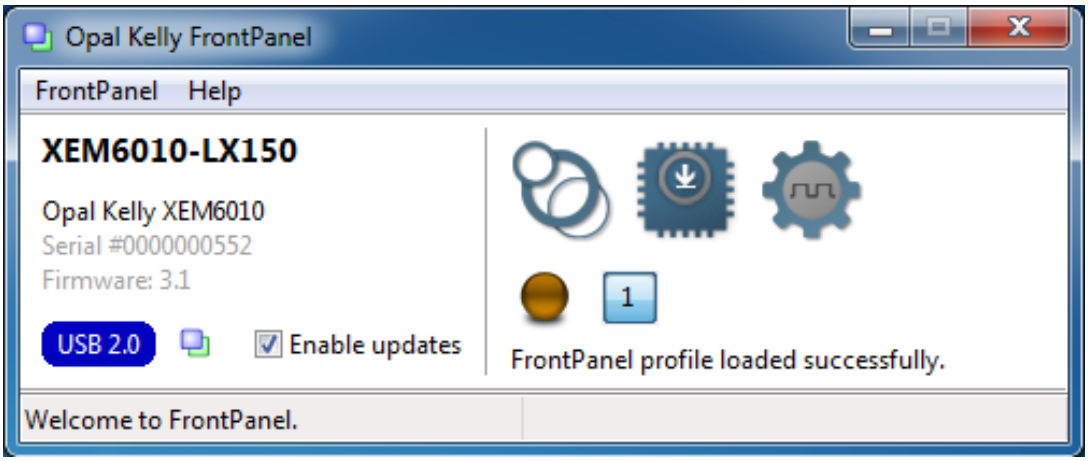


Figure 5.3: Opal Kelly FrontPanel Interface

Hardware co-simulation is very important in the sense that limits of the system clock frequency can only be seen in real time. During the simulation, the maximum system clock frequency was found to be 10 MHz, and the RAM blocks used in the modules could work at frequencies up to 30 MHz. These frequencies are the boundaries at which propagation time does not affect the running processes. If clock frequencies are increased, the calculations for fitness and velocity of the particles cannot be finished in the given period of time. Figure 5.4 shows the graphical user interface (GUI) implemented for observing and controlling the signals in the code. In this interface, the switching signals can be started and stopped, the relay at the output of the inverter can be controlled, and PI parameters of controllers can be adjusted. Several other parameters, such as switching angles and power calculation results, can be observed in separate interfaces.

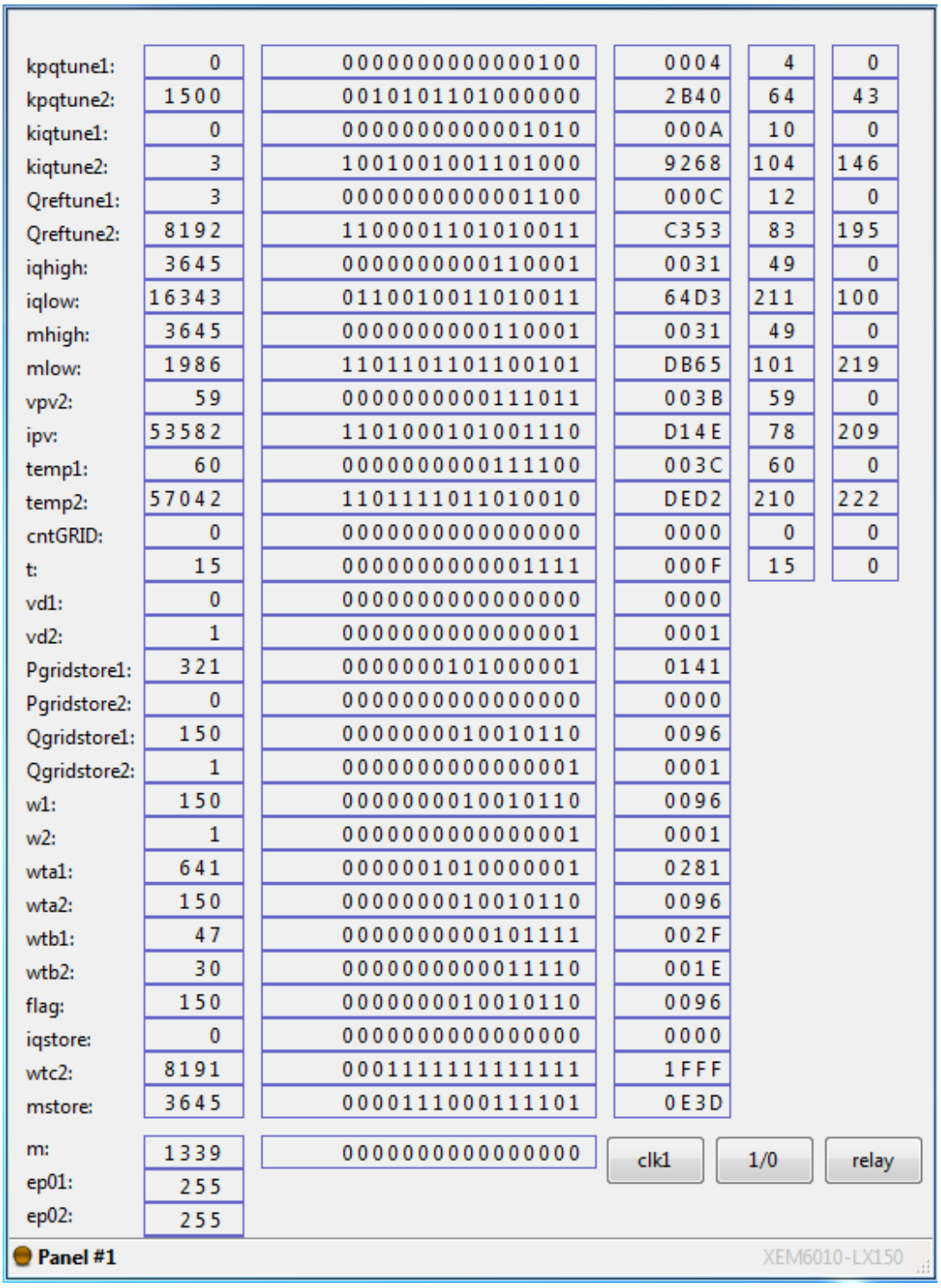


Figure 5.4: Implemented GUI for Observing and Controlling Signals

Table 5.1 below presents the switching angles which were found by the PSO algorithm running in the FPGA in real time and acquired via the FrontPanel interface. In this table, the modulation index is changed from 0 to 0.95, and the corresponding global fitness value is shown along with the switching angles. In the implemented PSO code, the fraction part of the fitness value is stored as a 22-bit vector, which gives a resolution of 2^{-22}. However, the LFSR used for pseudo-random number generation is 12-bit, which limits the resolution of the search algorithm. Thus, fitness values on the order of minimum 10^{-7} are achieved in the FPGA code although values on the order of 10^{-9} were possible to achieve with the MATLAB PSO code as can be remembered from Chapter 3 Section 3.3.4. Nevertheless, achieved fitness values from the FPGA implementation can be accepted to be satisfactory, and the resulting switching angle sets can be regarded as valid solutions for SHEM operation. The infeasible region of the solution space can also be observed from the results as the modulation index gets closer to 1.

In order to illustrate the performance of online application of SHEM in real time, the PSO module in the FPGA is given a sharp step change of modulation index from 0.1 to 0.9 and the resulting changes in the switching angles are observed on the oscilloscope through the DACs on the inverter. In this experiment, 180° is set to 5 V at the DAC output because this was the best setting which illustrated the changes in switching angles. Since 12-bit DACs are used on the inverter and 360° is defined as a 24-bit fixed-point logic vector, the last 11 bits of this vector could not be shown on the oscilloscope. The importance of this is that although the switching angles seem to reach steady state much earlier than the given 10-ms algorithm period, the search for the optimum set actually continues on a higher resolution in the FPGA code. Figures 5.5 – 5.11 depict the consequent changes in the switching angles where the blue signal shows the window in which the algorithm starts and stops, and the magenta signals are the switching angles whose values in degrees are marked on them. As can be seen from the figures, the algorithm successfully finds the new switching angle set in accordance with Table 5.1, with only small discrepancies caused by voltage measurement errors.

Table 5.1: Switching Angles Found from Hardware Co-simulation

Modulation index	$\alpha_1(^\circ)$	$\alpha_2(^\circ)$	$\alpha_3(^\circ)$	$\alpha_4(^\circ)$	$\alpha_5(^\circ)$	$\alpha_6(^\circ)$	$\alpha_7(^\circ)$	Fitness
0	0.2493	15.7299	15.7450	60.0205	75.0755	75.1126	89.9834	2.3842×10^{-7}
0.10	0.5413	14.6059	15.0185	60.8055	74.2343	75.7945	89.2893	1.2159×10^{-5}
0.20	1.2174	14.6774	15.5243	61.6366	73.4394	76.6187	88.5831	2.3842×10^{-7}
0.30	1.8639	14.5832	15.8383	62.4810	72.6492	77.4407	87.8685	1.1921×10^{-6}
0.40	2.5440	14.5221	16.1884	63.3469	71.8430	78.2928	87.1697	2.4080×10^{-5}
0.50	3.1544	14.6122	16.4289	64.1677	71.1103	79.1146	86.5212	1.8597×10^{-5}
0.60	3.8429	14.5104	16.8160	65.0482	70.3910	80.0027	85.9159	7.1526×10^{-7}
0.70	4.5554	14.5901	17.2189	66.0119	69.6945	81.0345	85.3590	1.9073×10^{-6}
0.80	5.2526	14.7281	17.6156	67.1384	69.1861	82.2752	85.0532	1.9073×10^{-6}
0.90	5.8949	14.8653	17.9233	70.0526	70.5724	84.4271	85.7674	2.4891×10^{-4}
0.95	6.0575	14.9571	18.0922	74.9765	75.3163	86.6707	87.6171	7.4458×10^{-4}

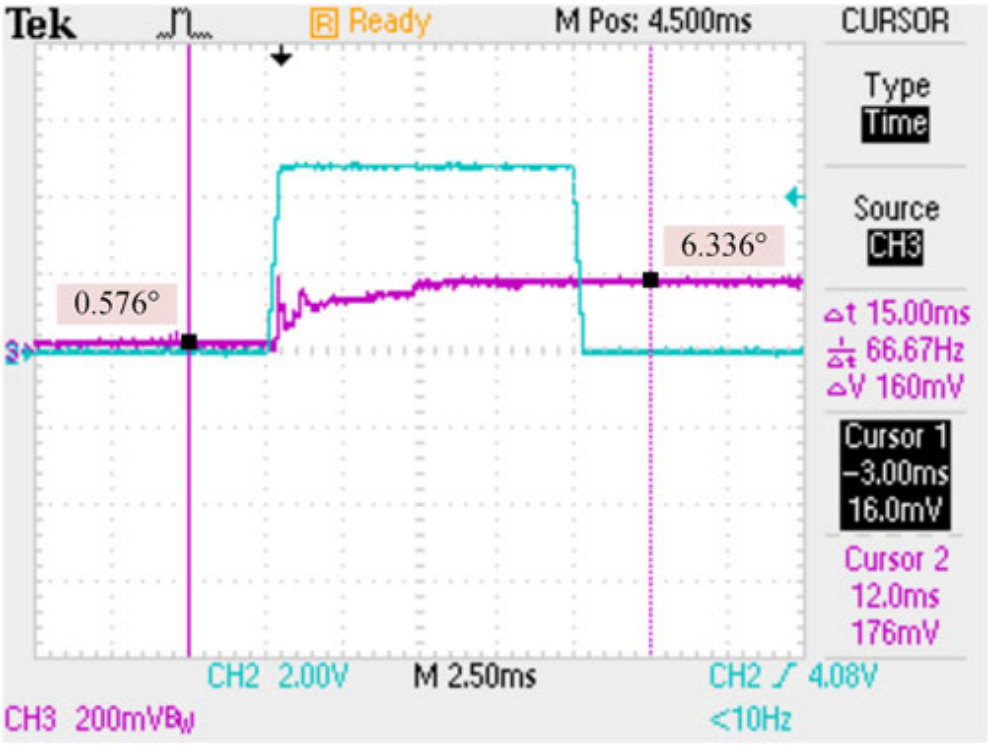


Figure 5.5: Online Change in Switching Angle α_1

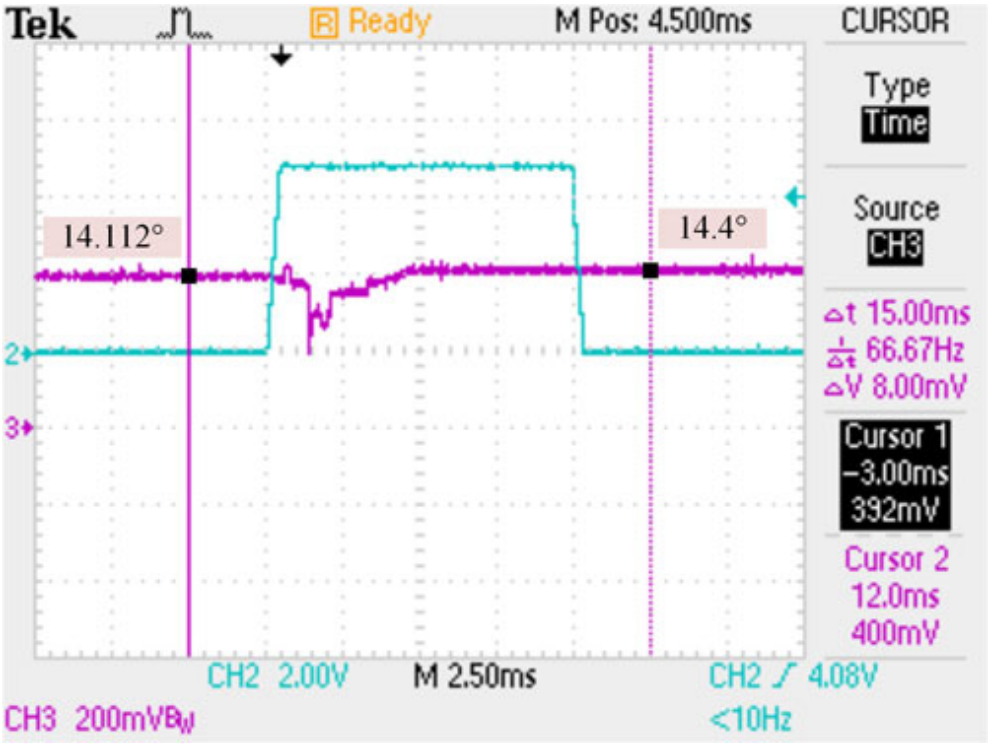


Figure 5.6: Online Change in Switching Angle α_2

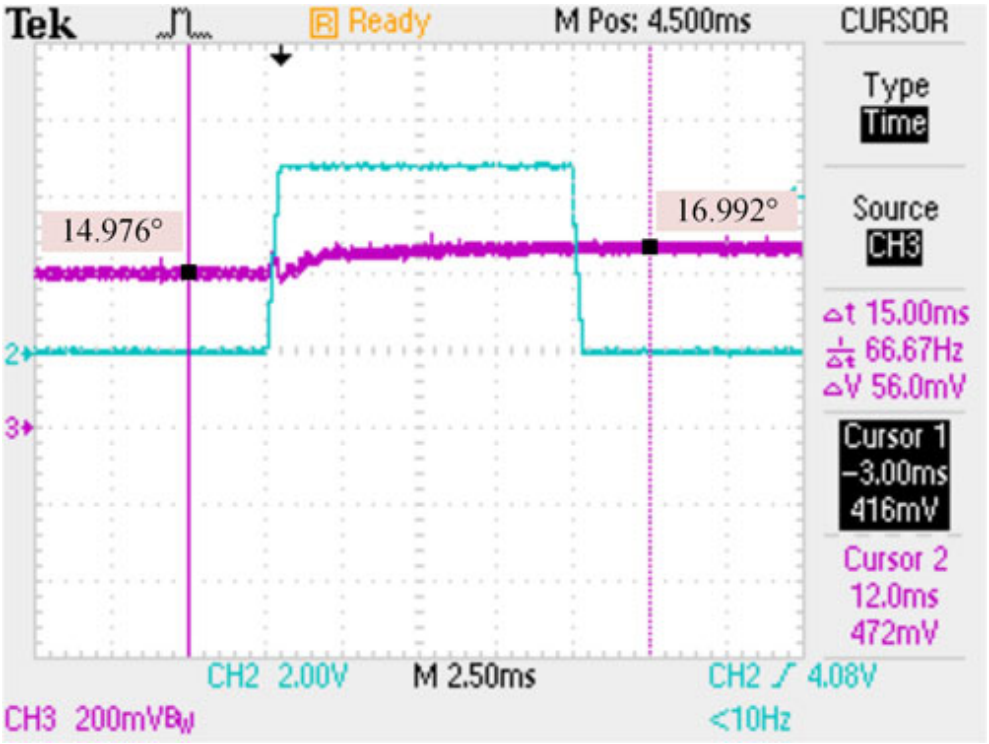


Figure 5.7: Online Change in Switching Angle α_3

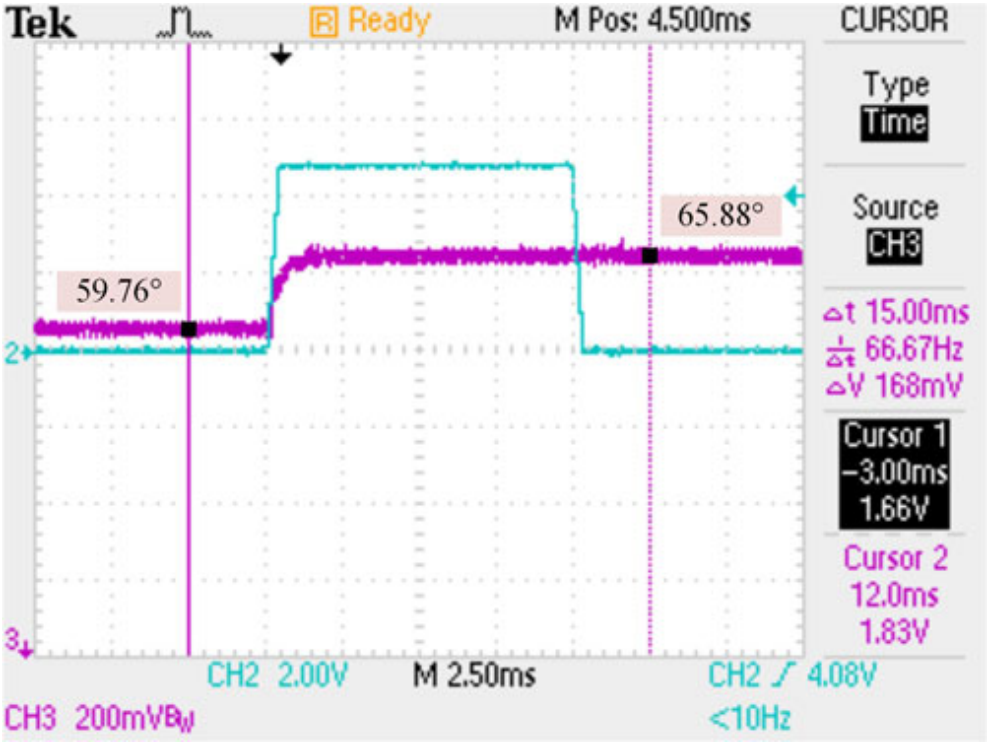


Figure 5.8: Online Change in Switching Angle α_4

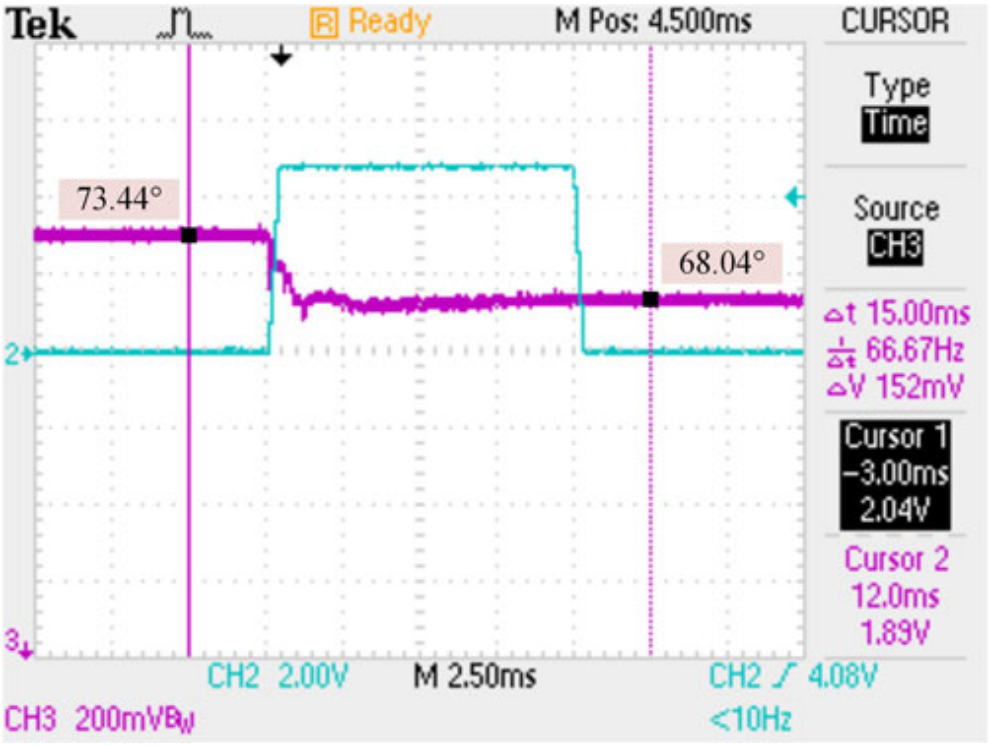


Figure 5.9: Online Change in Switching Angle α_5

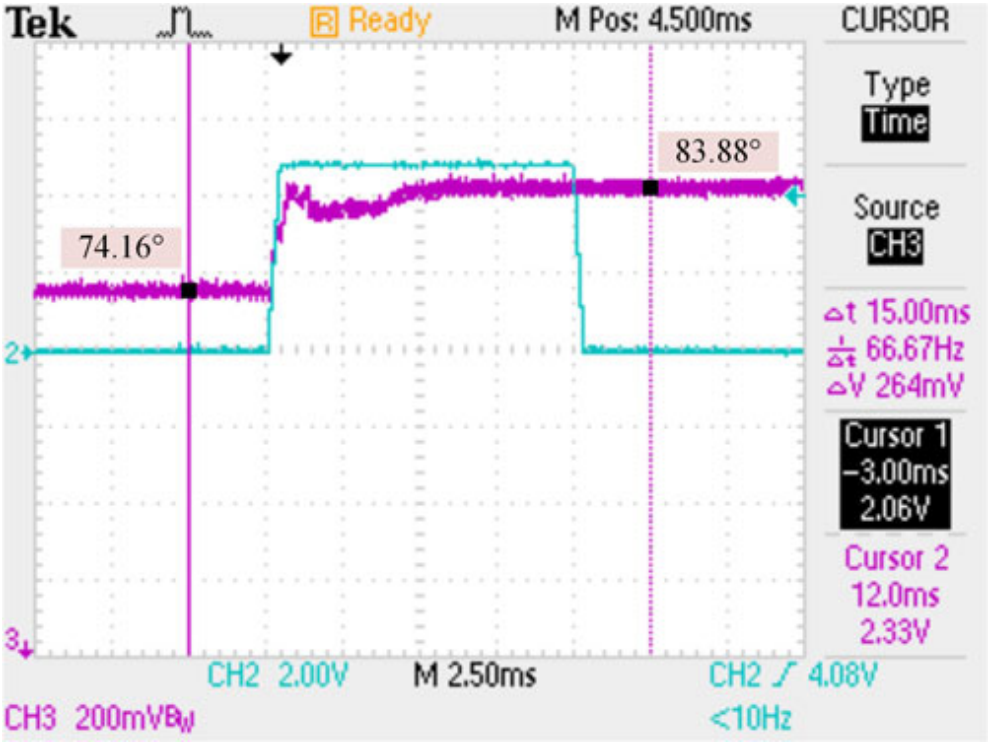


Figure 5.10: Online Change in Switching Angle α_6

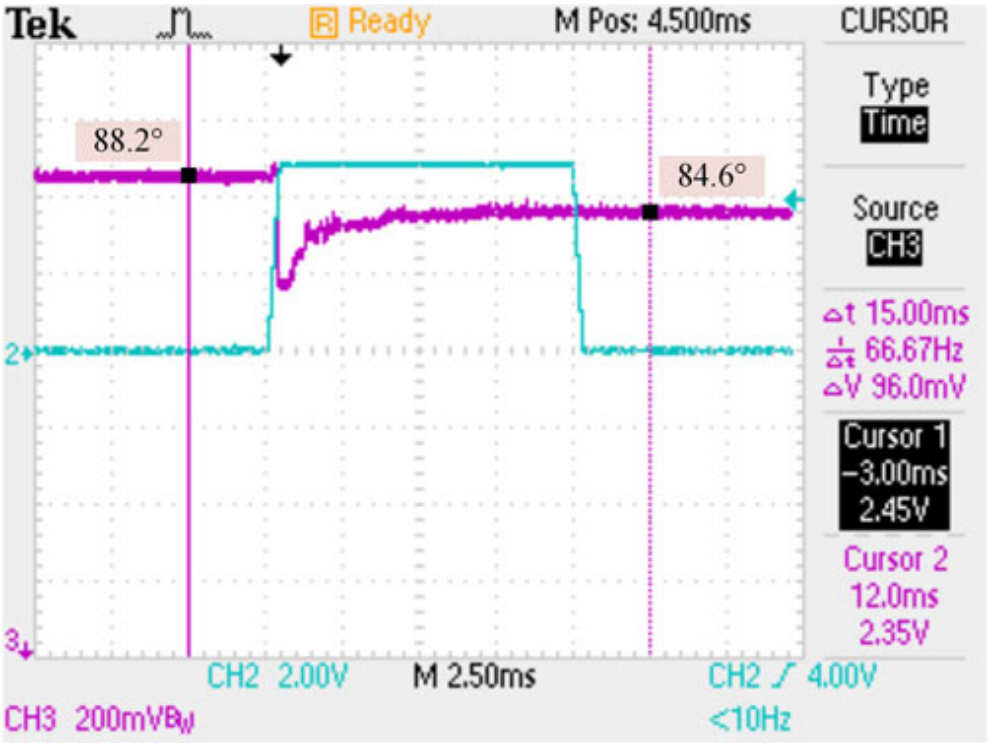


Figure 5.11: Online Change in Switching Angle α_7

5.1.3 Simulink Results

The circuit diagram of the three-phase two-level grid-connected inverter is shown again in Figure 5.12, and the specifications of the inverter and the components used in the circuit are repeated in Table 5.2. The circuit is simulated in the Simulink environment on the computer.

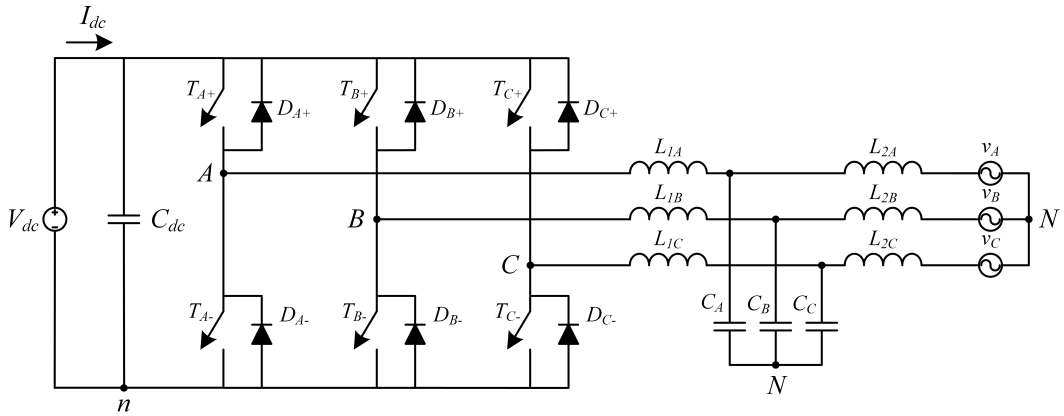


Figure 5.12: Three-Phase Two-Level Grid-Connected Inverter

Table 5.2: Specifications of the Inverter and Components

DC Link Voltage, V_{dc}	600 - 900 V
DC Link Current, I_{dc}	3 A_{max}
DC Link Capacitor, C_{dc}	40 μF
IGBT Maximum V_{CE} Voltage	1200 V
LCL Filter Inductors, L_{1A}, L_{1B}, L_{1C}	15 mH
LCL Filter Inductors, L_{2A}, L_{2B}, L_{2C}	15 mH
LCL Filter Capacitors, C_A, C_B, C_C	20 μF
Grid Specification	Three-Phase 380 V_{l-l}, 50 Hz
Rated Power	1.6 kVA
Switching Frequency	750 Hz

Simulink environment is part of the MATLAB software in which the PSO algorithm code is written. One of the most valuable aspects of simulating the circuit in Simulink is that this PSO code can be integrated in the simulation easily as a function block. Therefore, a complete simulation of the control loops can be realized in the software. Figure 5.13 shows the solver parameters used for the simulation whereas Figure 5.14 depicts the diagram of the circuit simulated in the Simulink environment. In this diagram, "PLL" blocks implement PLL for all three phases, "PQ" block makes calculations for instantaneous active and reactive powers, and the MATLAB function "PSO Algorithm" block, seen on the top right part of the figure, integrates the PSO code written in MATLAB language into the Simulink simulation. The calculated angles are then fed to "Leg A", "Leg B", and "Leg C" blocks which create the related switching signals for the IGBTs.

This simulation is done for a PV application, in which the MPPT voltages of the series-connected string of panels changes drastically with temperature as can be remembered from Section 2.1.1 of Chapter 2. In order to show new SHEM switching angles are found for changing values of input DC link voltage, three cases are investigated in which the temperature of the panels are changed from -10 °C (Case I) to 25 °C (Case II) at 3 seconds and then to 60 °C (Case III) at 5 seconds in the simulation. The corresponding input DC voltages become 825 V, 750 V, and 690 V in these cases. The rated inverter power is 1600 W.

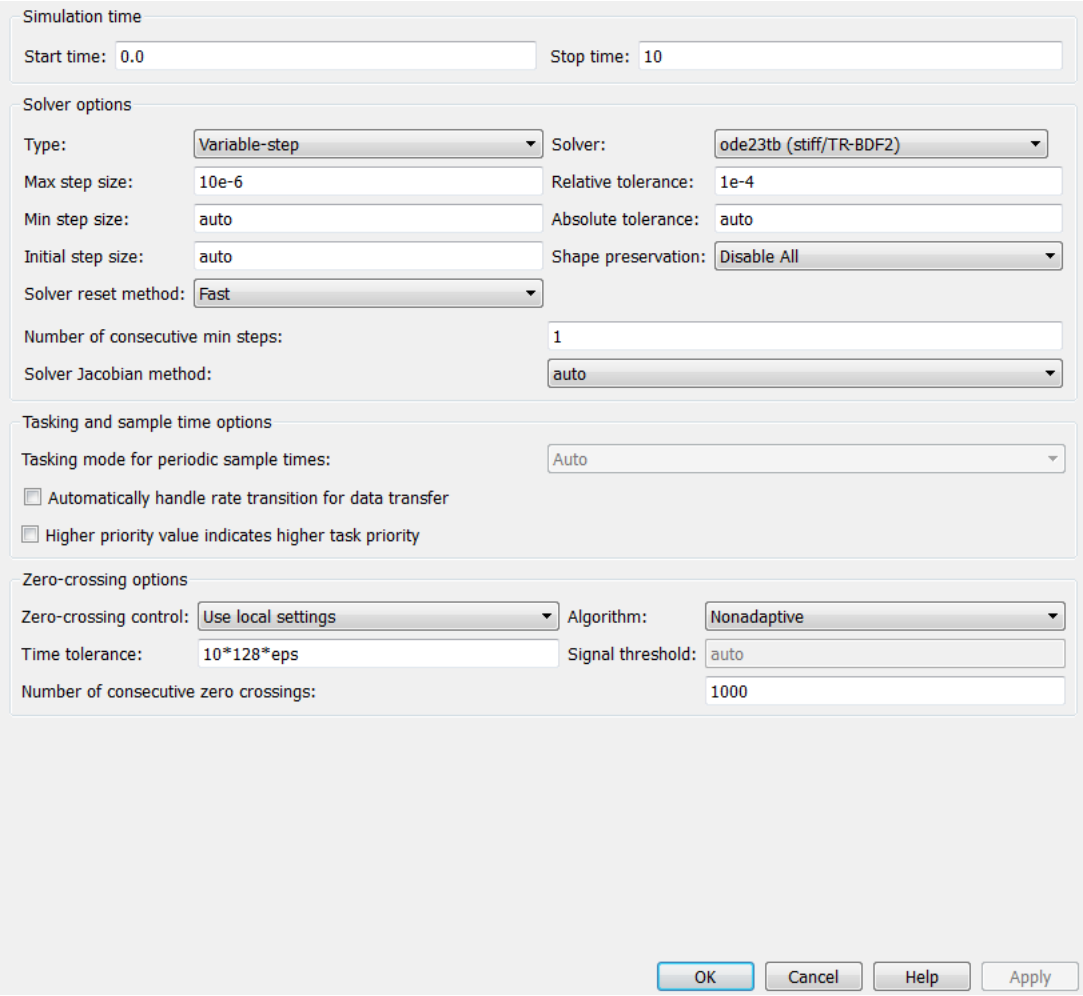


Figure 5.13: Solver Parameters for Simulink Simulation

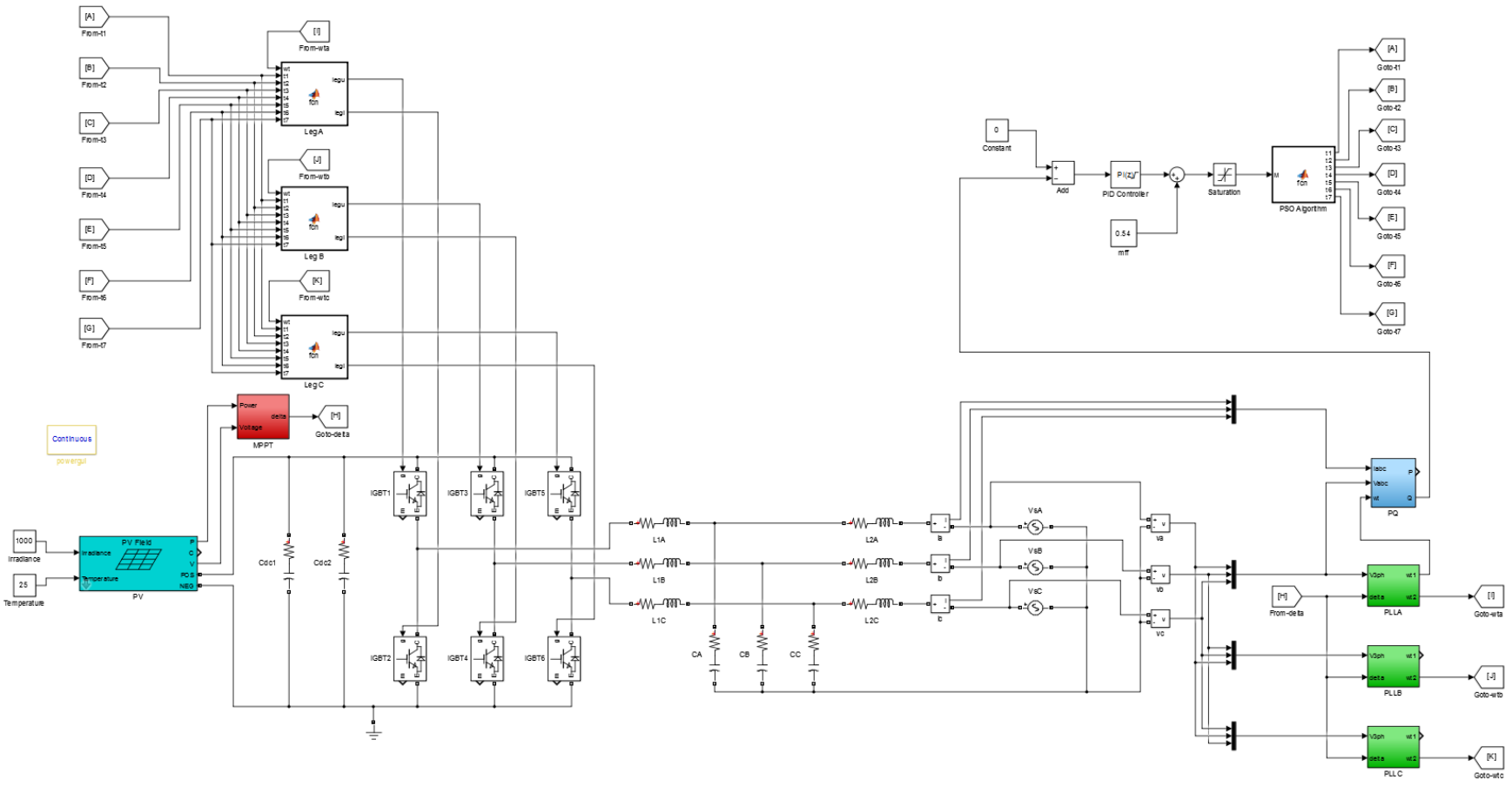


Figure 5.14: Diagram of the Circuit Simulated in Simulink

5.1.3.1 Grid Voltage and PLL Output

Figure 5.15 shows the three-phase grid voltage and the PLL output for phase A, B, and C. As can be seen from the figure, the implemented PLL block successfully finds the zero-crossings of the grid voltage.

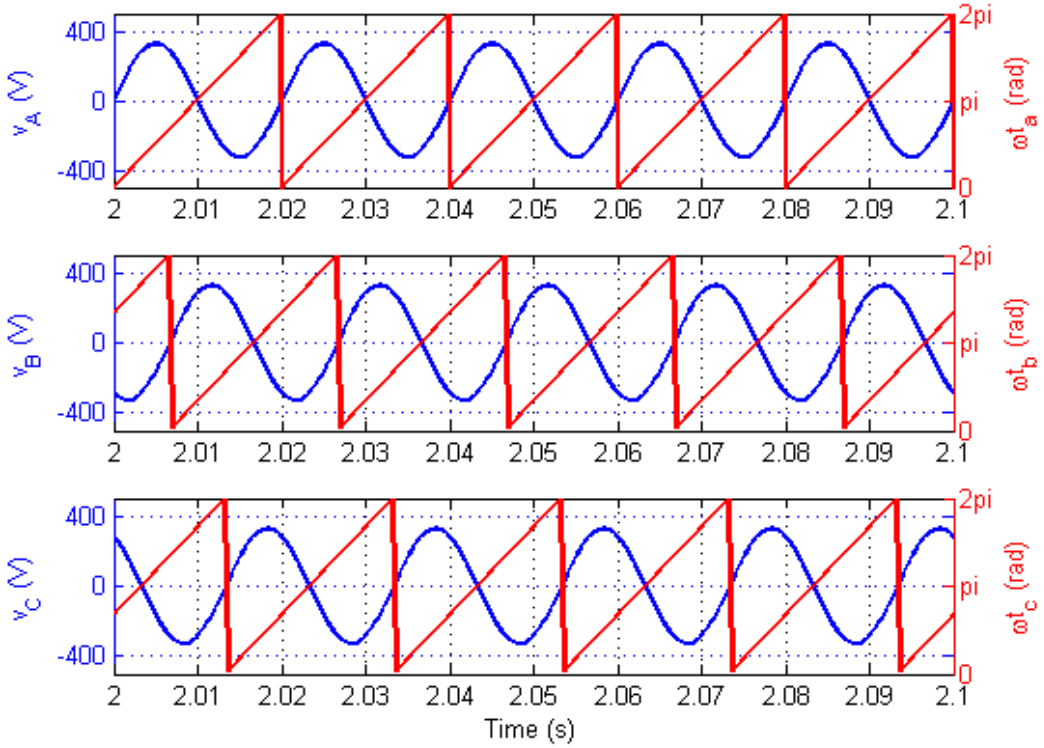


Figure 5.15: Three-Phase Grid Voltage and PLL Output for Each Phase (Simulink)

5.1.3.2 Input DC Link Voltage

Figure 5.16 shows the changes in the input DC link voltage whereas Figure 5.17 shows the voltage ripple in this voltage for all three cases. As can be seen from the figures, the input voltage changes at 3 and 5 seconds of the simulation to reflect the temperature change in the solar simulator, and the voltage ripple is not more than 20 V in all cases.

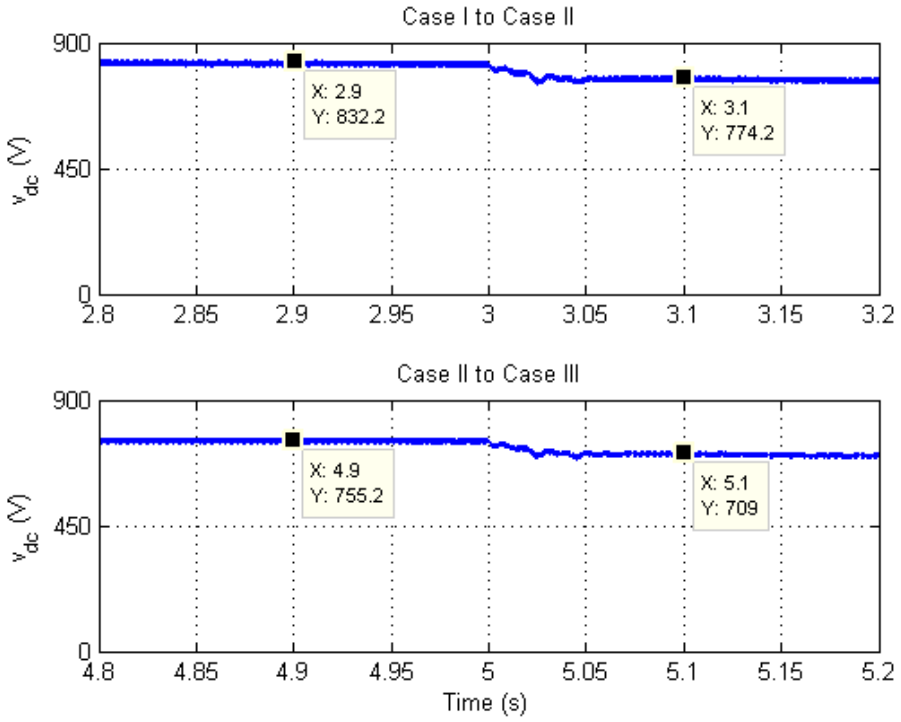


Figure 5.16: Changes in Input DC Link Voltage of the Inverter (Simulink)

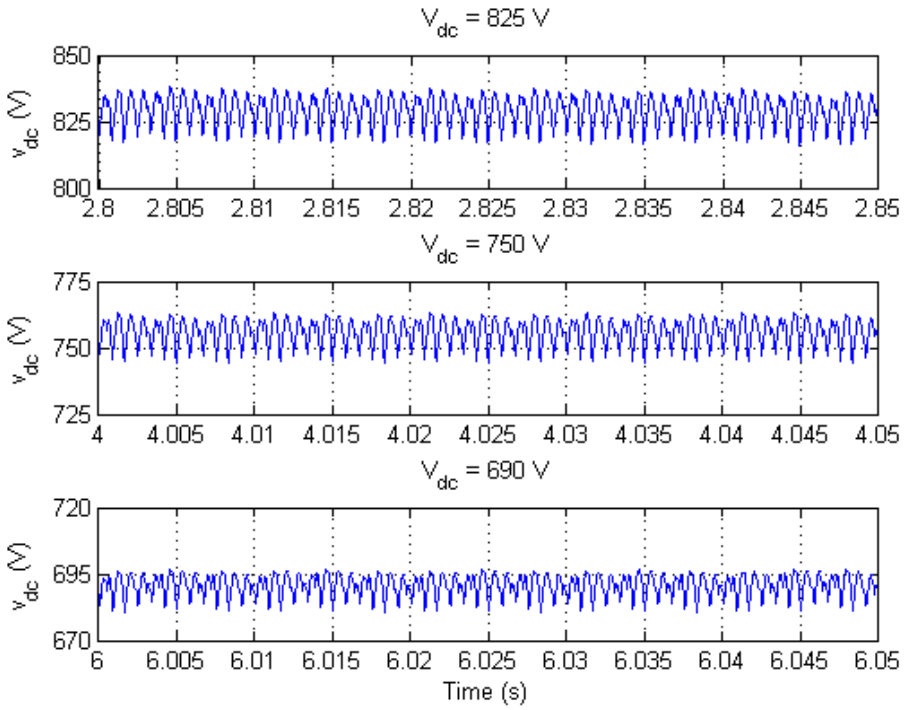


Figure 5.17: Input DC Link Voltage Ripple of the Inverter (Simulink)

5.1.3.3 Modulation Index and Switching Angles

Figure 5.18 shows the changes in the modulation index while Figure 5.19 and Figure 5.20 shows the corresponding change in the set of switching angles found by the PSO algorithm according to the changes in the input DC link voltage. As can be seen from the figures, the control loop that tries to keep the output reactive power at zero finds the modulation index value that minimizes the reactive power error in less than 40 ms, and the switching angles are calculated and updated at each period of the grid voltage in this duration by the PSO algorithm function block.

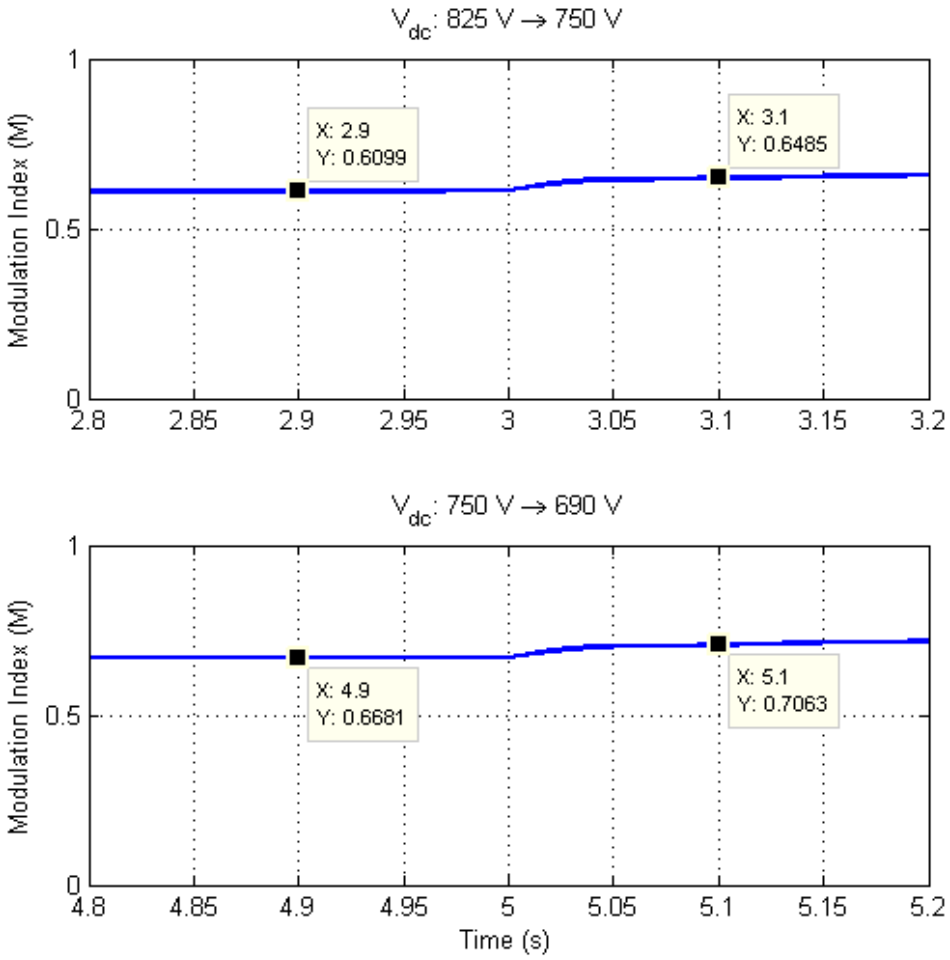


Figure 5.18: Changes in Modulation Index of the Inverter (Simulink)

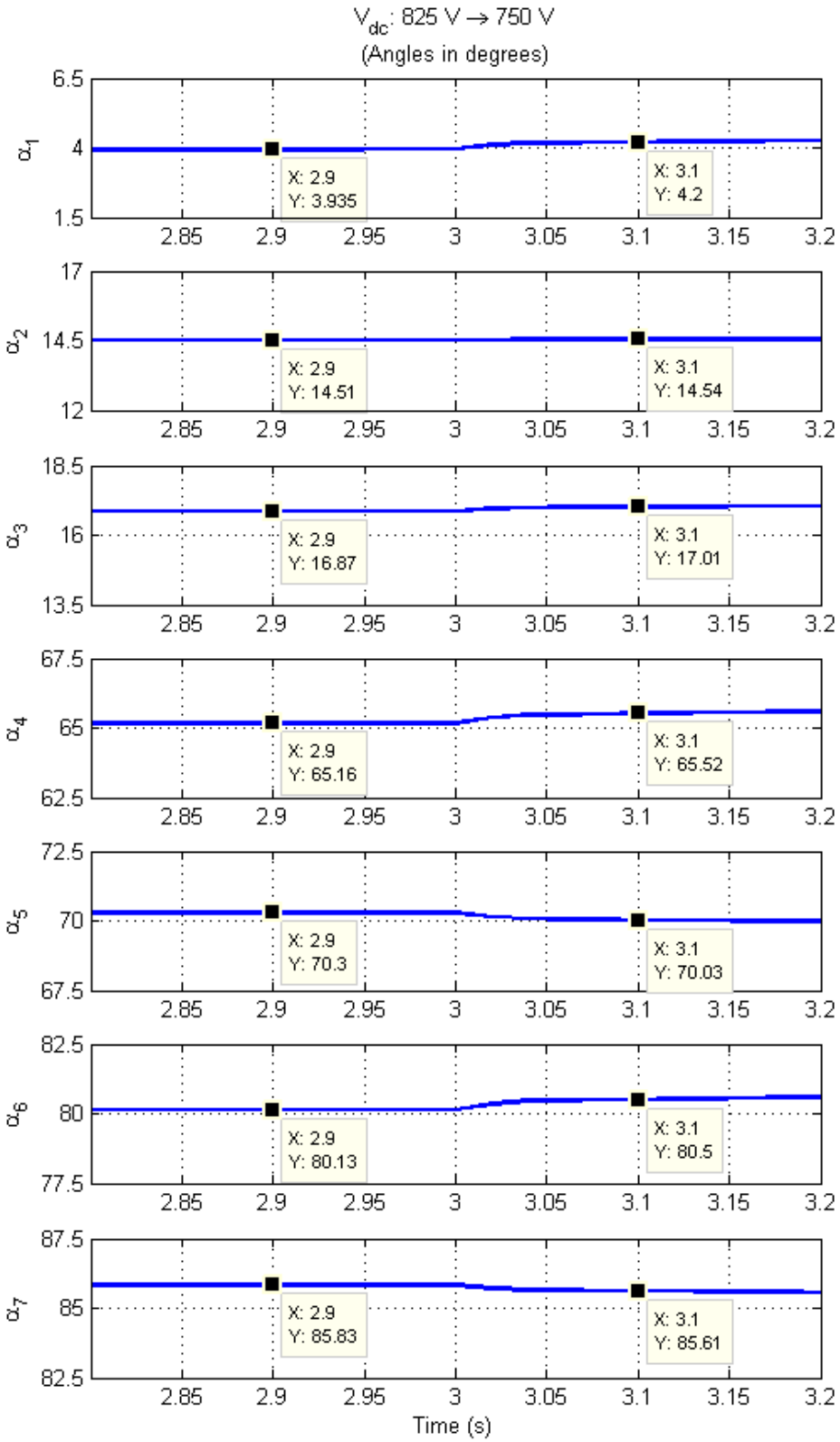


Figure 5.19: Changes in Switching Angles (Case I to Case II) (Simulink)

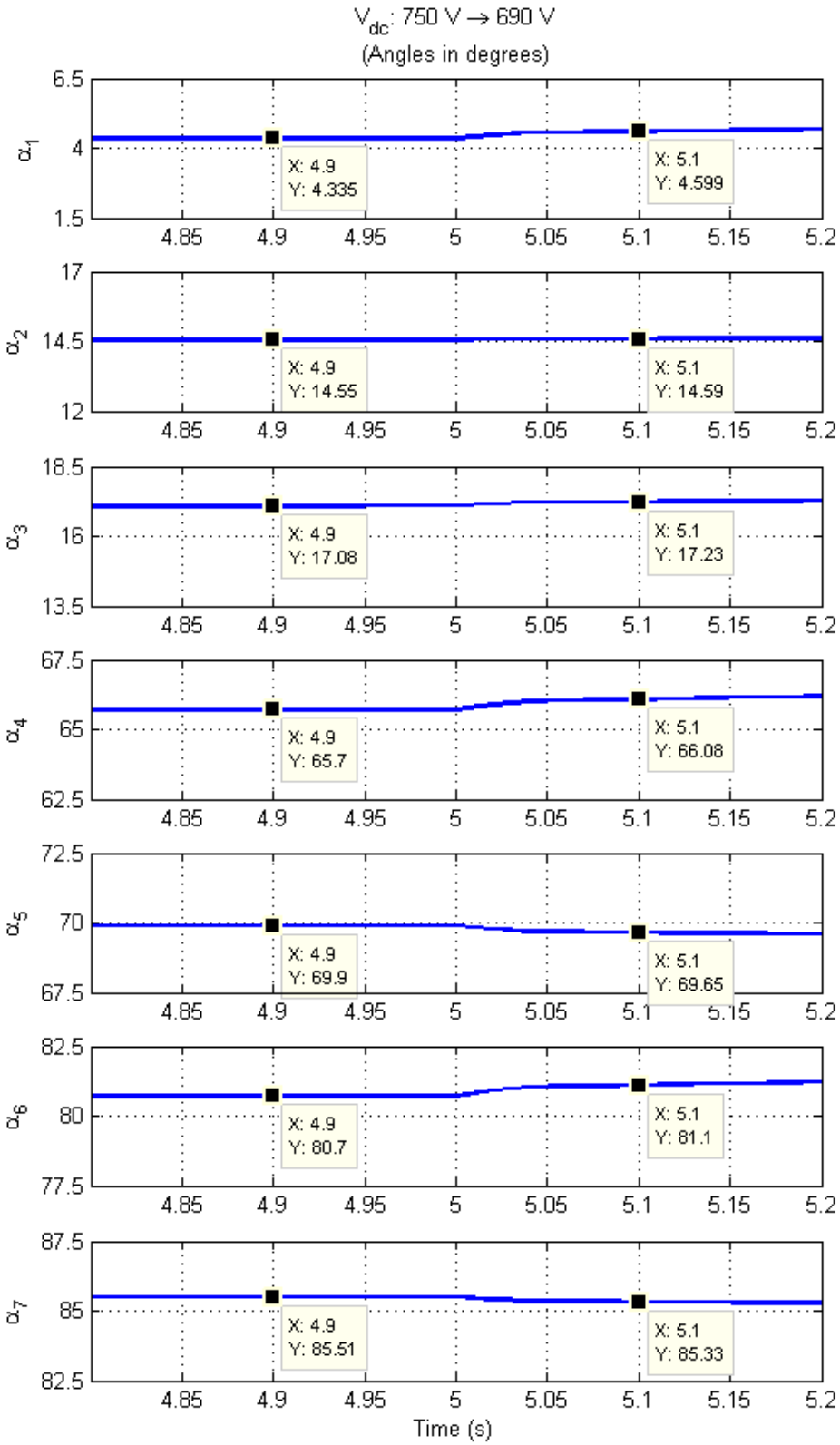


Figure 5.20: Changes in Switching Angles (Case II to Case III) (Simulink)

5.1.3.4 Inverter Output Voltage

Figure 5.21 shows the inverter midpoint output voltage for Leg A (v_{An} in Figure 5.12) while Figure 5.22 shows the inverter line-to-line output voltage (v_{AB}) for all three cases. The FFT analysis of the inverter midpoint output voltage is included in Figure 5.23 since the selected SHEM pattern is TLN1 technique, which eliminates 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, and 19^{th} harmonics in the line-to-neutral output voltage. Figure 5.24, Figure 5.25, and Figure 5.26 show that the specified lower-order harmonics are consequently eliminated in the line-to-line inverter output voltages for each case.

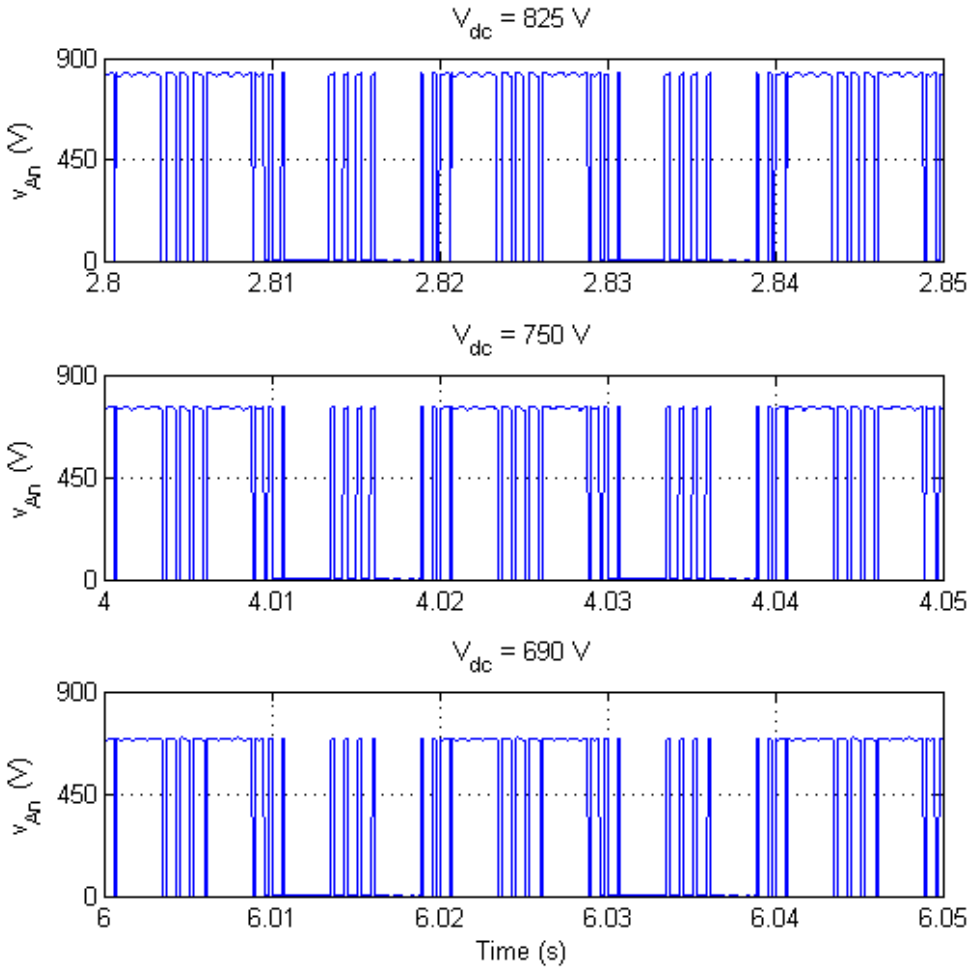


Figure 5.21: Inverter Midpoint Output Voltage for Each Case (Simulink)

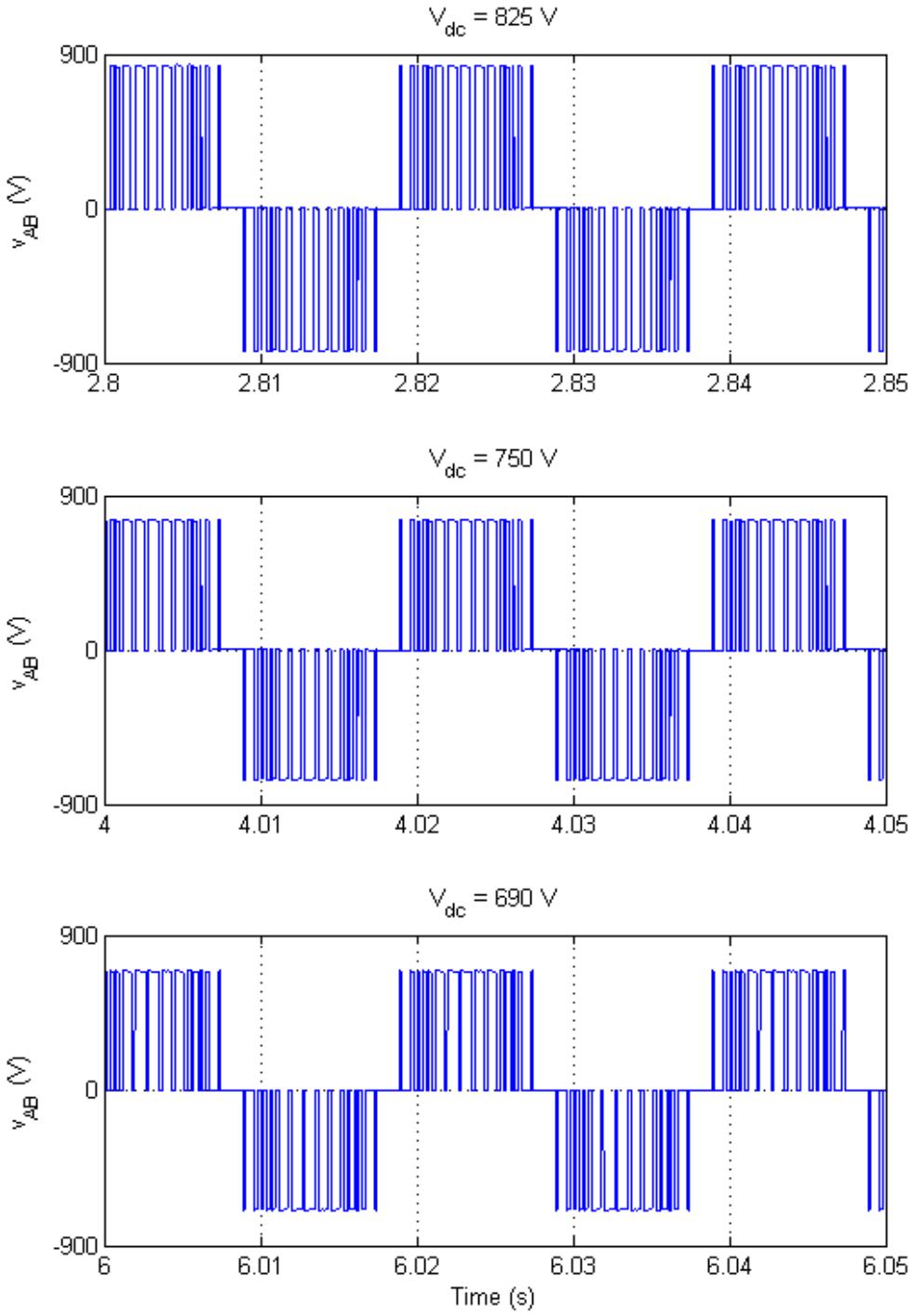


Figure 5.22: Inverter Line-to-Line Output Voltage for Each Case (Simulink)

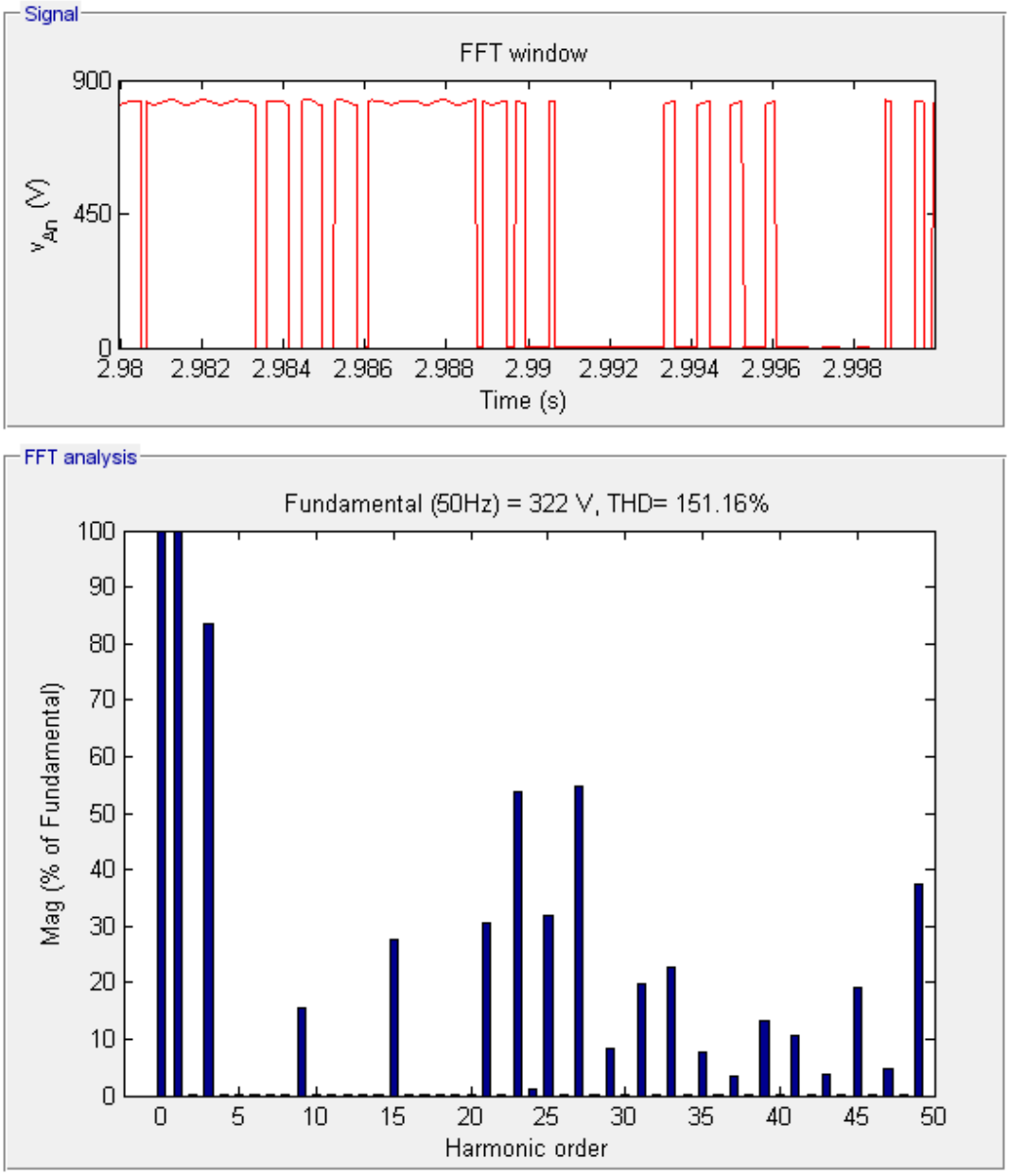


Figure 5.23: FFT Analysis of the Inverter Midpoint Output Voltage for Case I (Simulink)

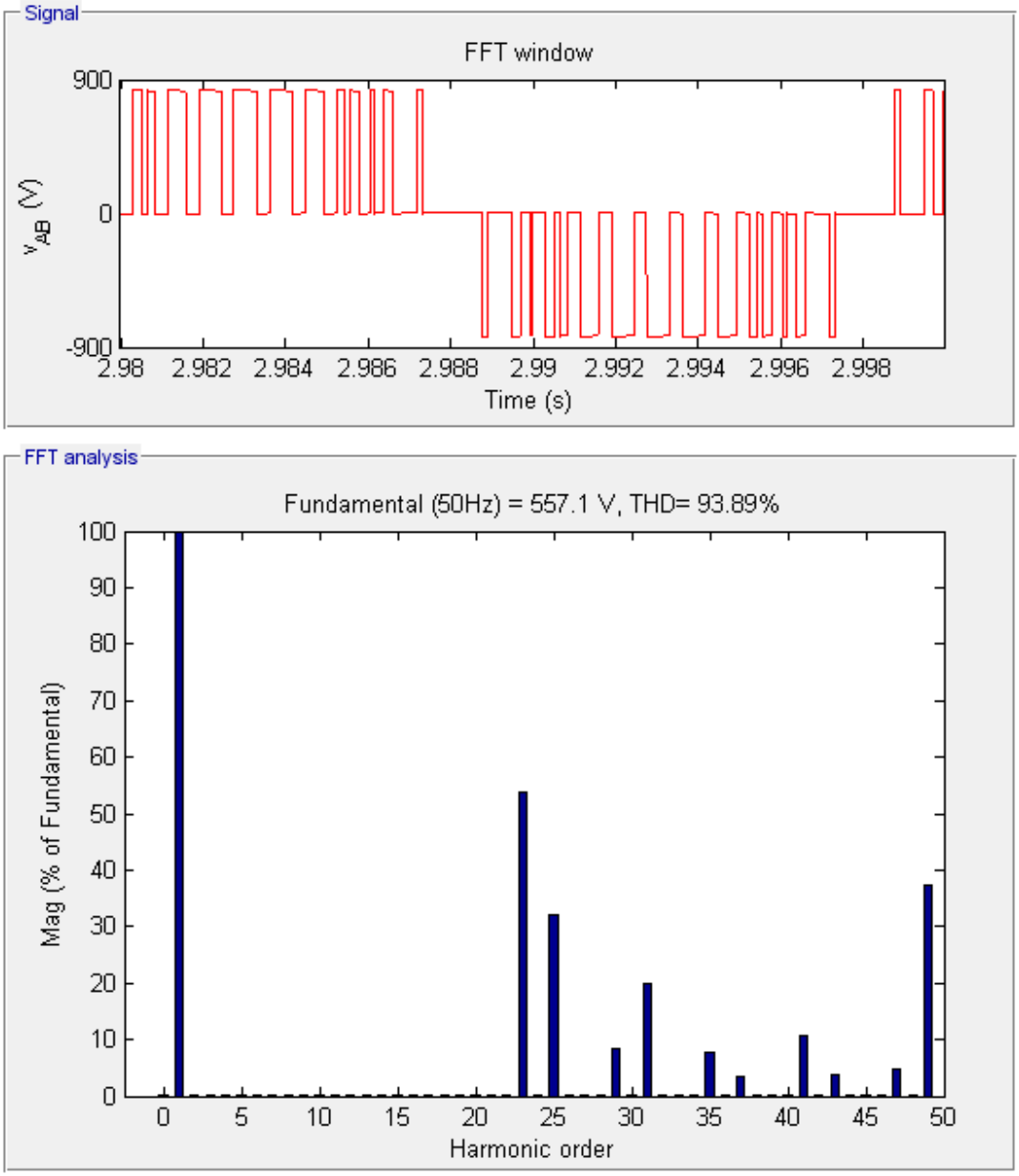


Figure 5.24: FFT Analysis of the Line-to-Line Output Voltage for Case I (Simulink)

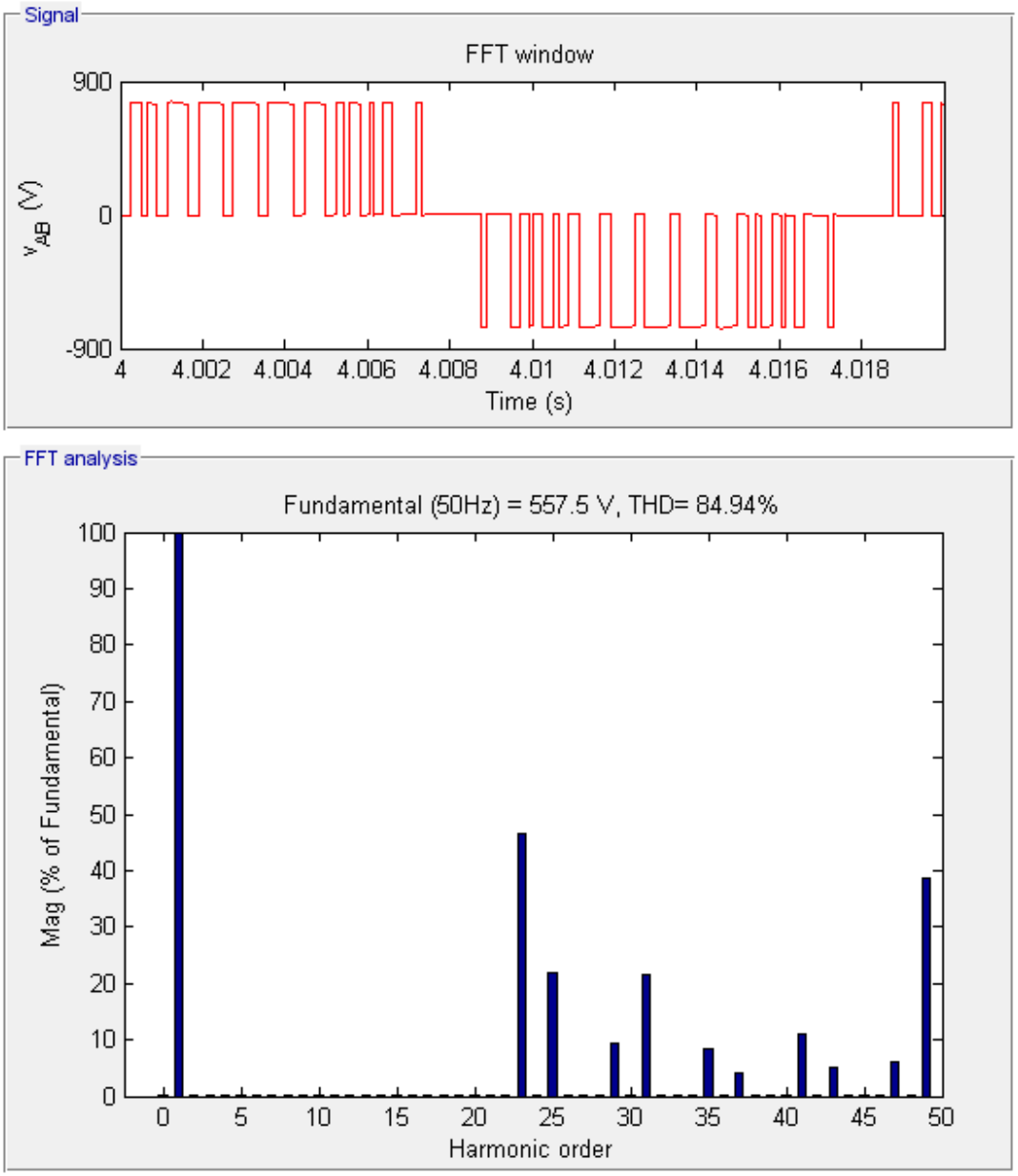


Figure 5.25: FFT Analysis of the Line-to-Line Output Voltage for Case II (Simulink)

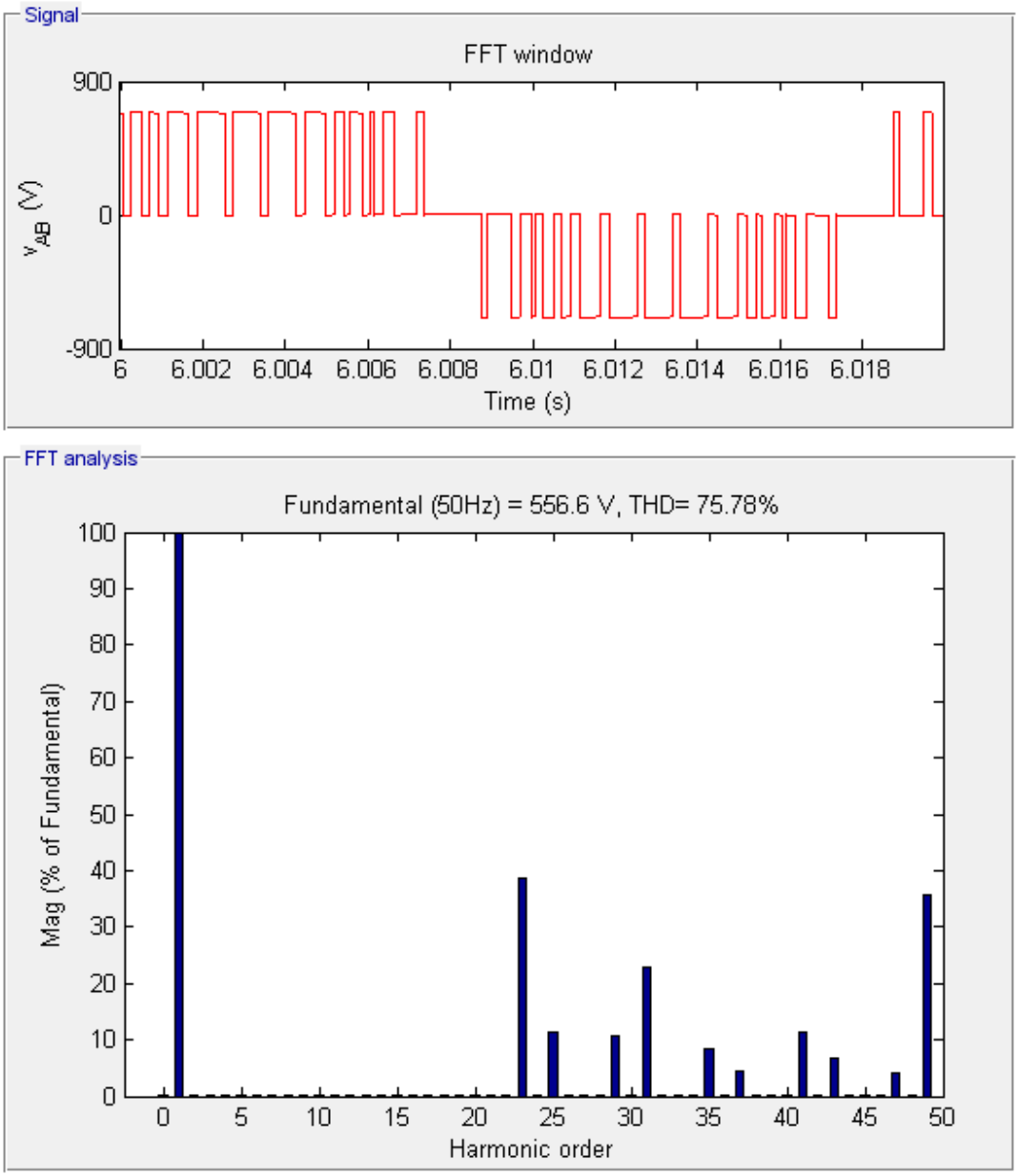


Figure 5.26: FFT Analysis of the Line-to-Line Output Voltage for Case III (Simulink)

5.1.3.5 Inverter and Grid Side Output Currents

Figure 5.27 shows the inverter-side current (i_{L1A}), and Figure 5.28 shows the grid-side current (i_{L2A}) for all three cases. Figure 5.29 shows the FFT analysis of the inverter-side current. The FFT analyses of the grid current in all of the cases, depicted in Figure 5.30, Figure 5.31, and Figure 5.32, show that the specified lower-order harmonics are eliminated and at least minimized successfully. As can be seen from these figures, the utilized LCL filter damps the high-order harmonics successfully. Although the total demand distortion (TDD) is below 5 %, there are some non-eliminated harmonics around the 5^{th} and 7^{th} harmonics in the analyses. These harmonics are related with the resonant frequencies of the LCL filter, which are calculated as in Equation 5.1 and Equation 5.2 [70]. If the calculations are done with the component values presented in Table 5.2, these frequencies come out to be 290.58 Hz and 410.94 Hz, respectively. Although the harmonic analyses of the inverter line-to-line output voltage show nearly absent low-order harmonics, very low 5^{th} and 7^{th} voltage harmonics present in the waveforms might be amplified to show their effects on the line current since the resonant frequencies of the filter come out to be around them.

$$f_{res1} = \frac{1}{\sqrt{L_2 C}} \tag{5.1}$$

$$f_{res2} = \frac{1}{\sqrt{\frac{L_1 L_2}{L_1 + L_2} C}} \tag{5.2}$$

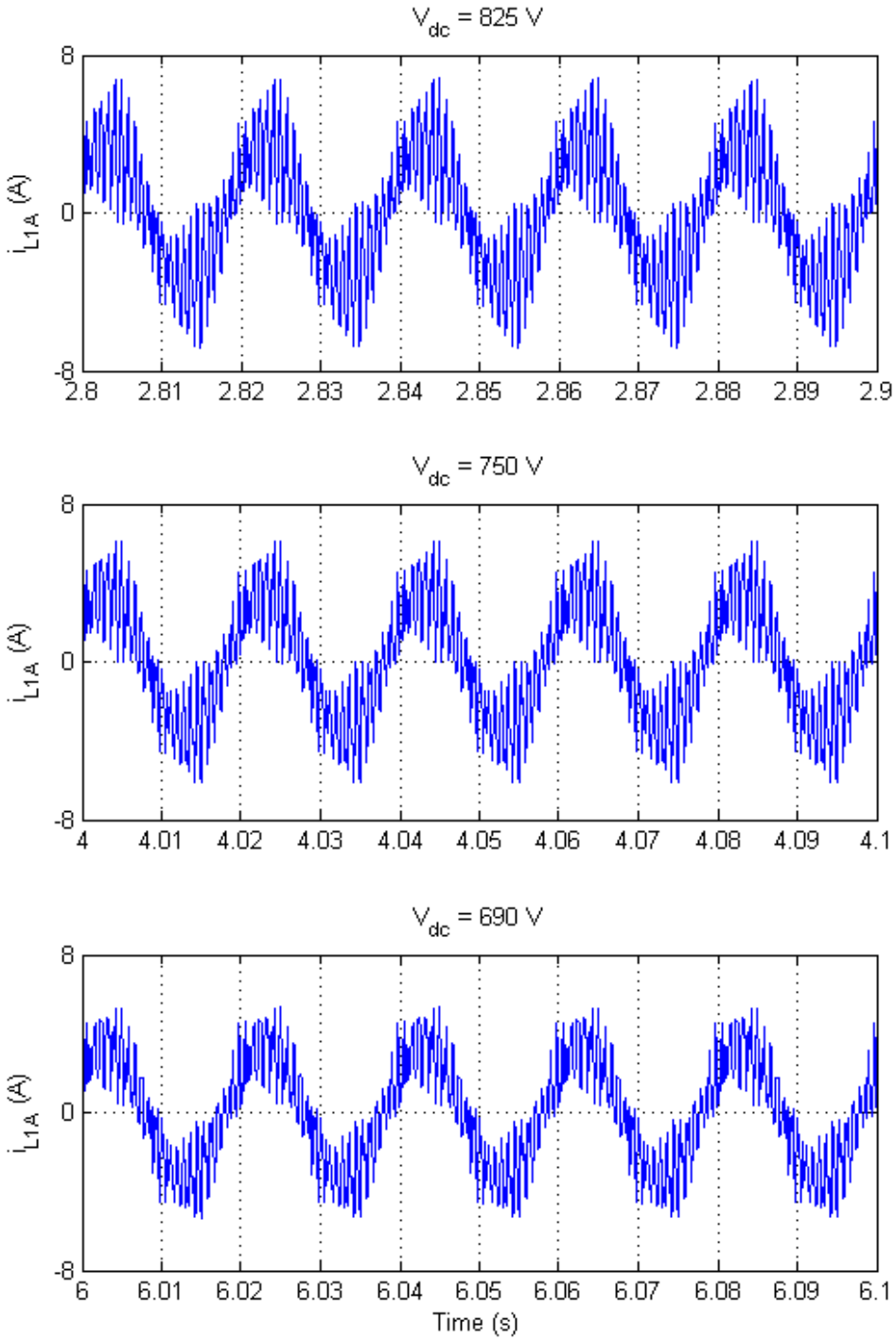


Figure 5.27: Inverter-Side Current for Each Case (Simulink)

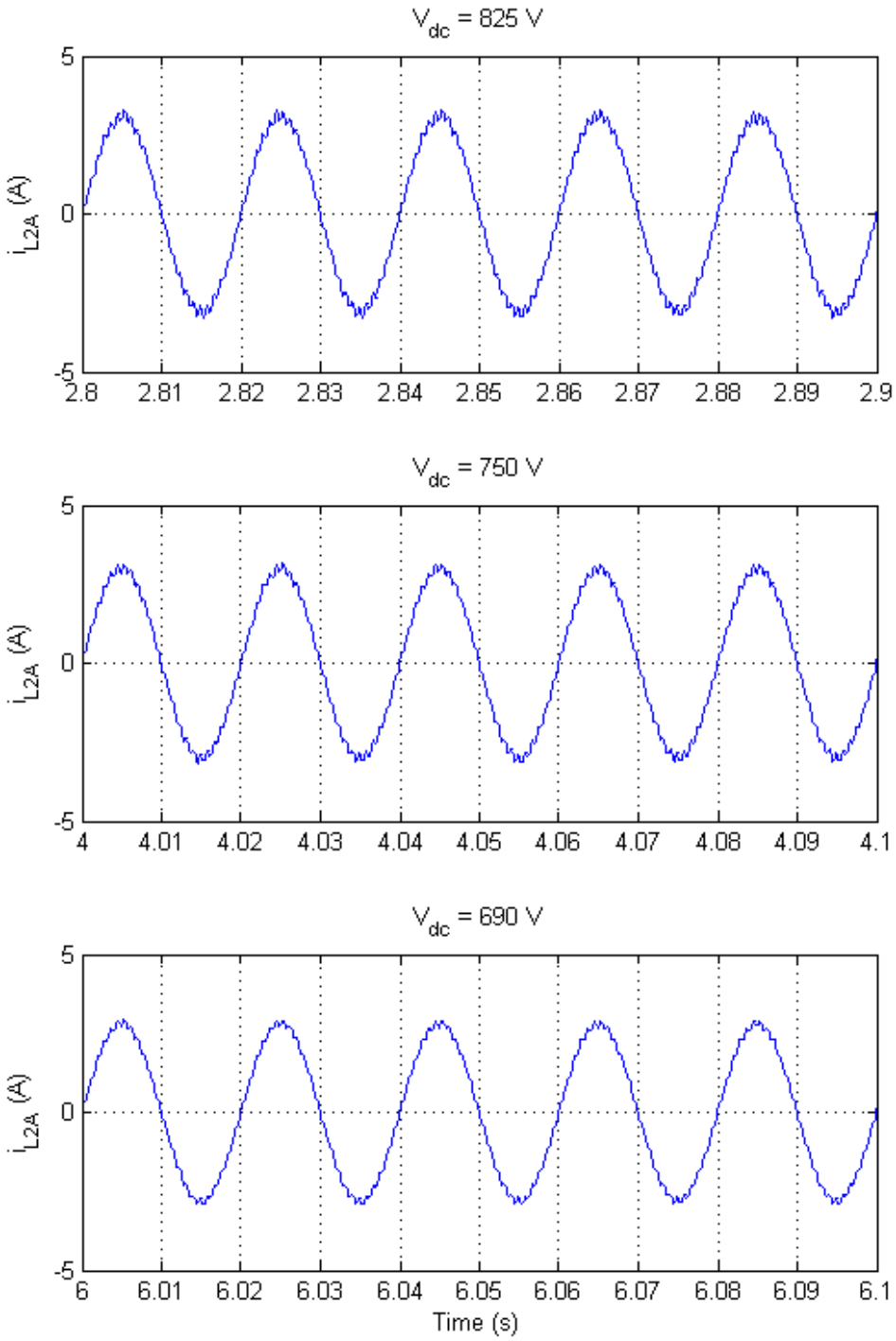


Figure 5.28: Grid-Side Current for Each Case (Simulink)

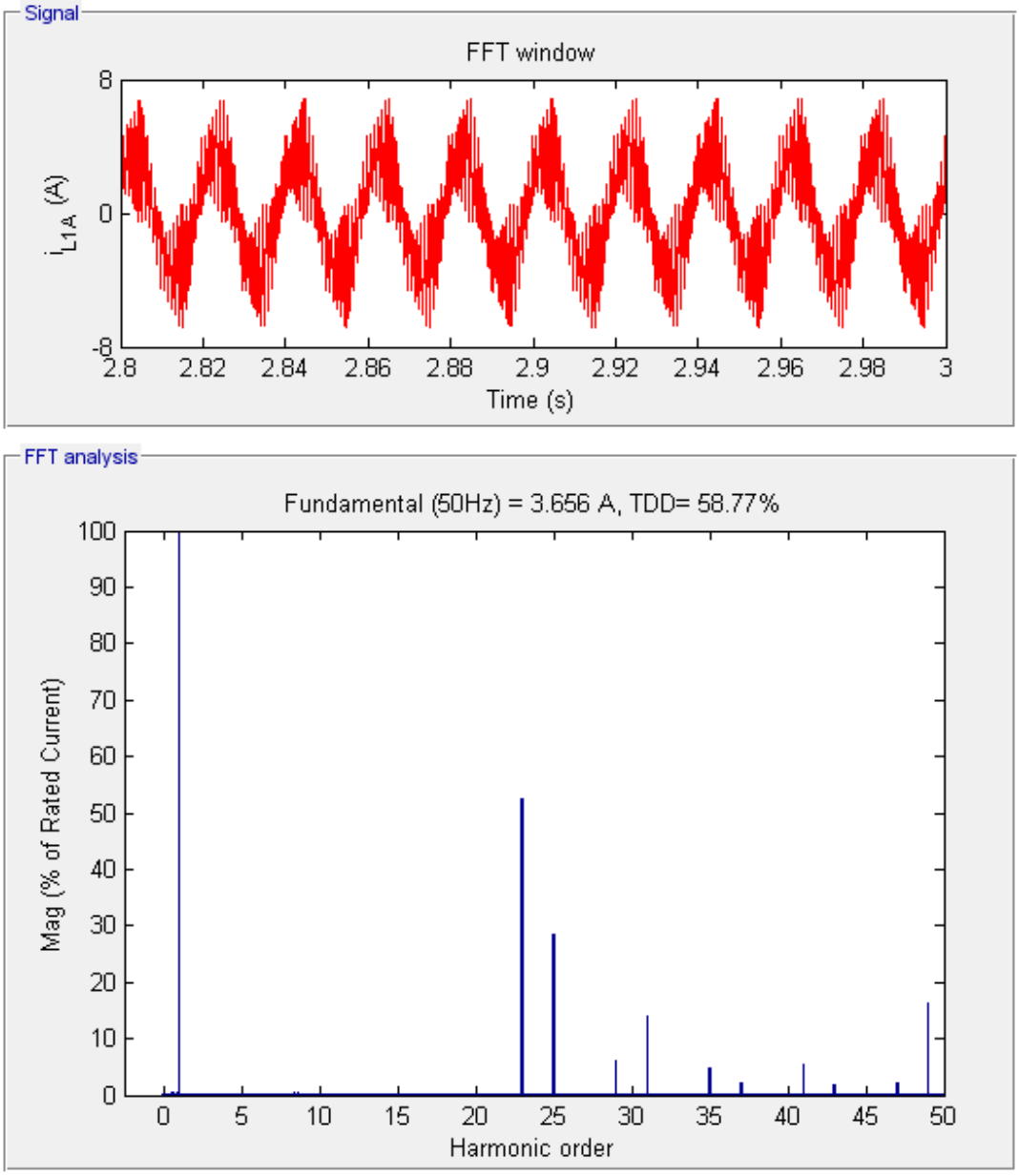


Figure 5.29: FFT Analysis of the Inverter-Side Current for Case I (Simulink)

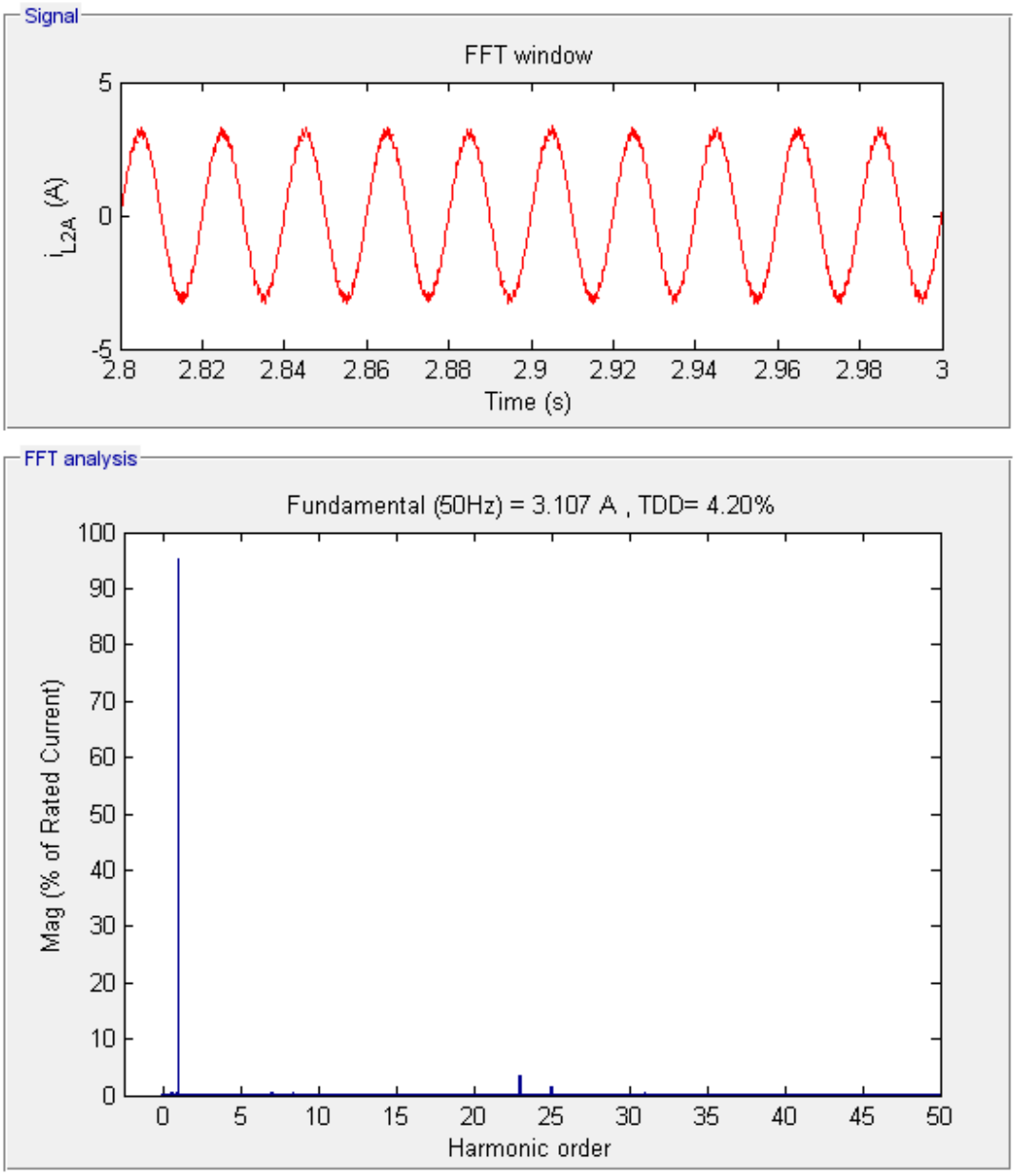


Figure 5.30: FFT Analysis of the Grid-Side Current for Case I (Simulink)

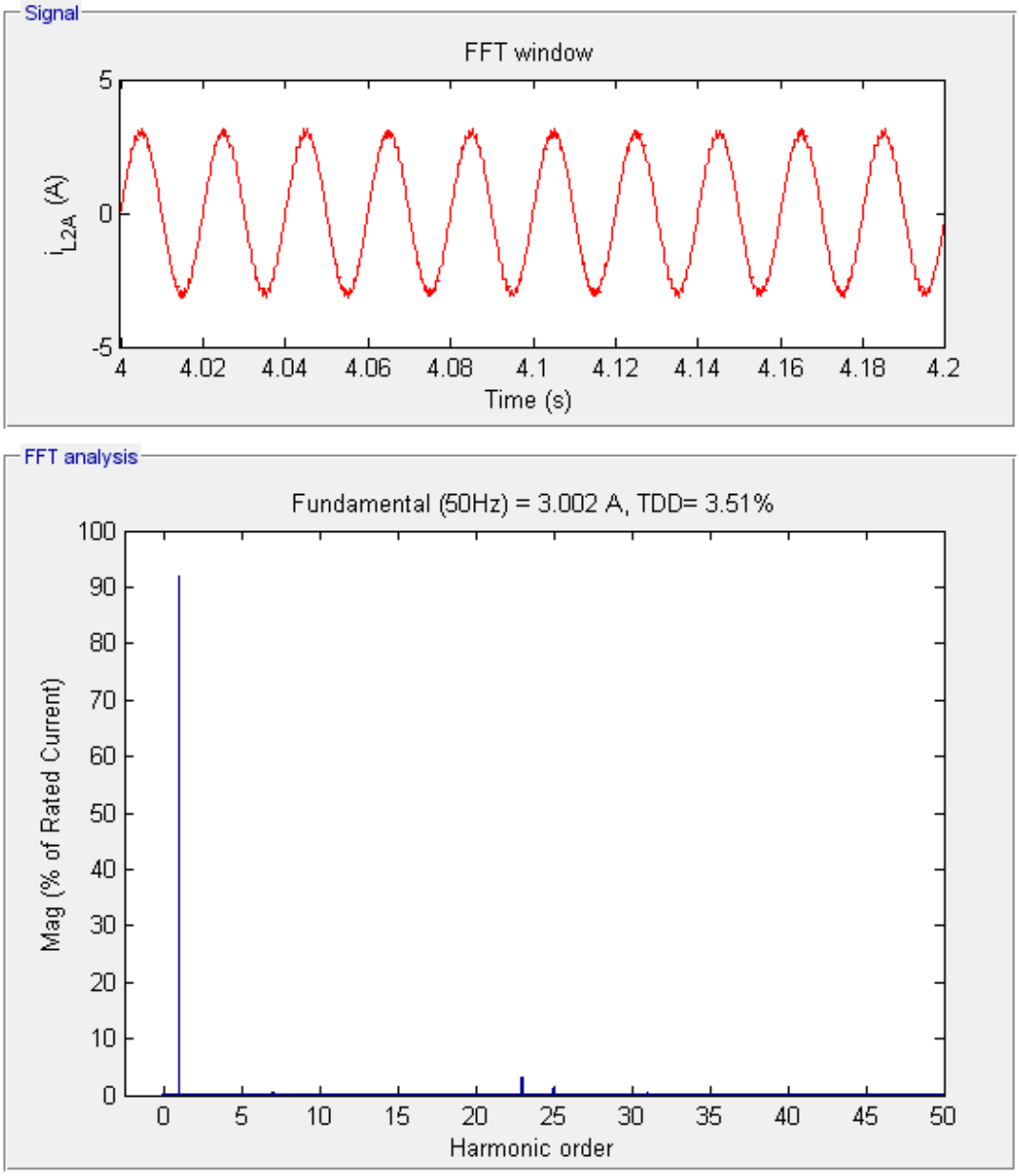


Figure 5.31: FFT Analysis of the Grid-Side Current for Case II (Simulink)

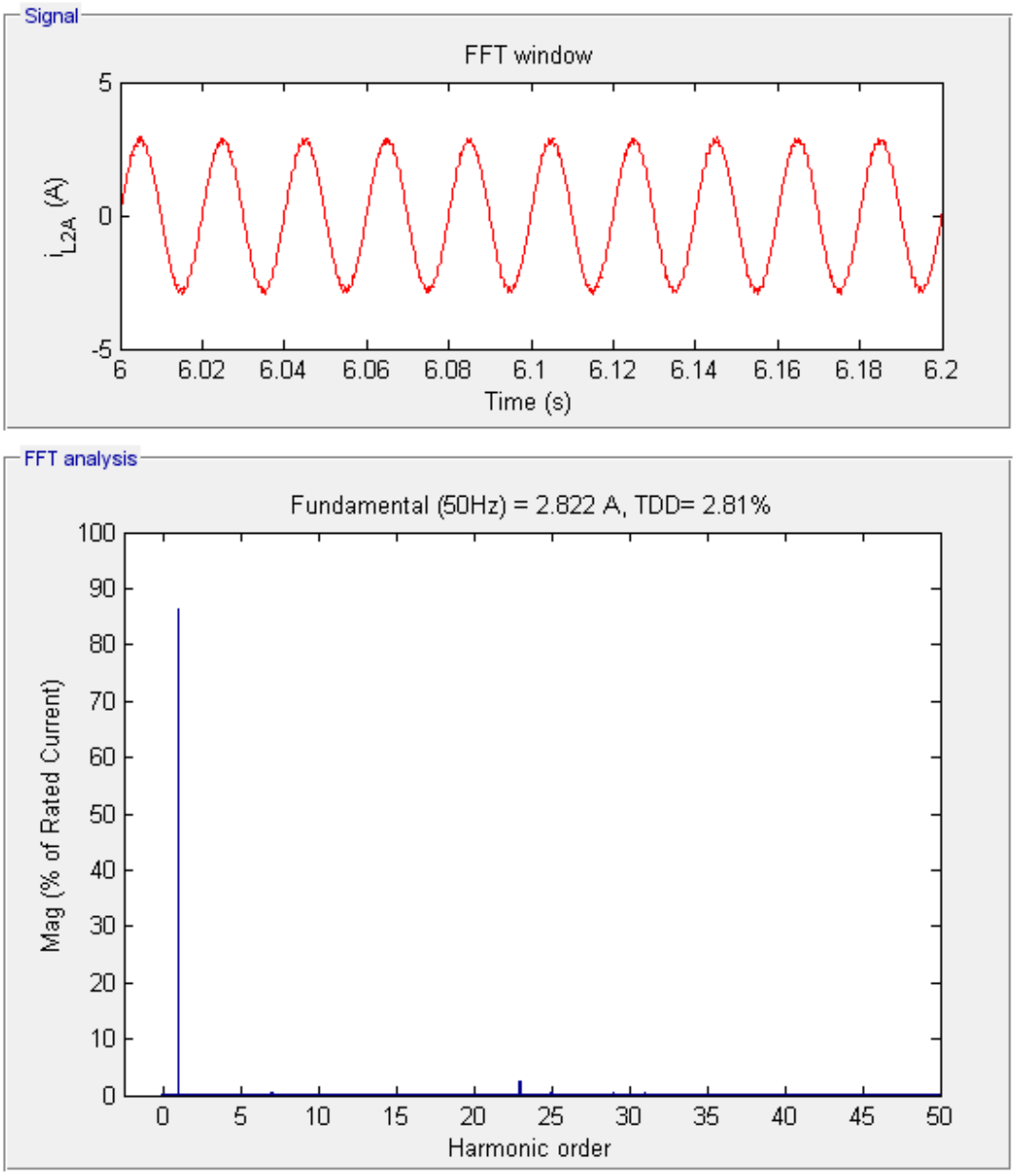


Figure 5.32: FFT Analysis of the Grid-Side Current for Case III (Simulink)

5.1.3.6 Input and Output Power of the Inverter

Figure 5.33 shows the instantaneous active power at the input side of the inverter. The power output of the simulator reflects the temperature change and decreases as the temperature increases. Figure 5.34 and Figure 5.35 show the total active power and reactive power at the grid frequency injected to the grid by the inverter. As can be seen from the figures, there are some undershoots in the output active and reactive powers, but the controller compensates these undershoots well in less than 0.05 s. The efficiency of the inverter can be calculated to be around 97 %.

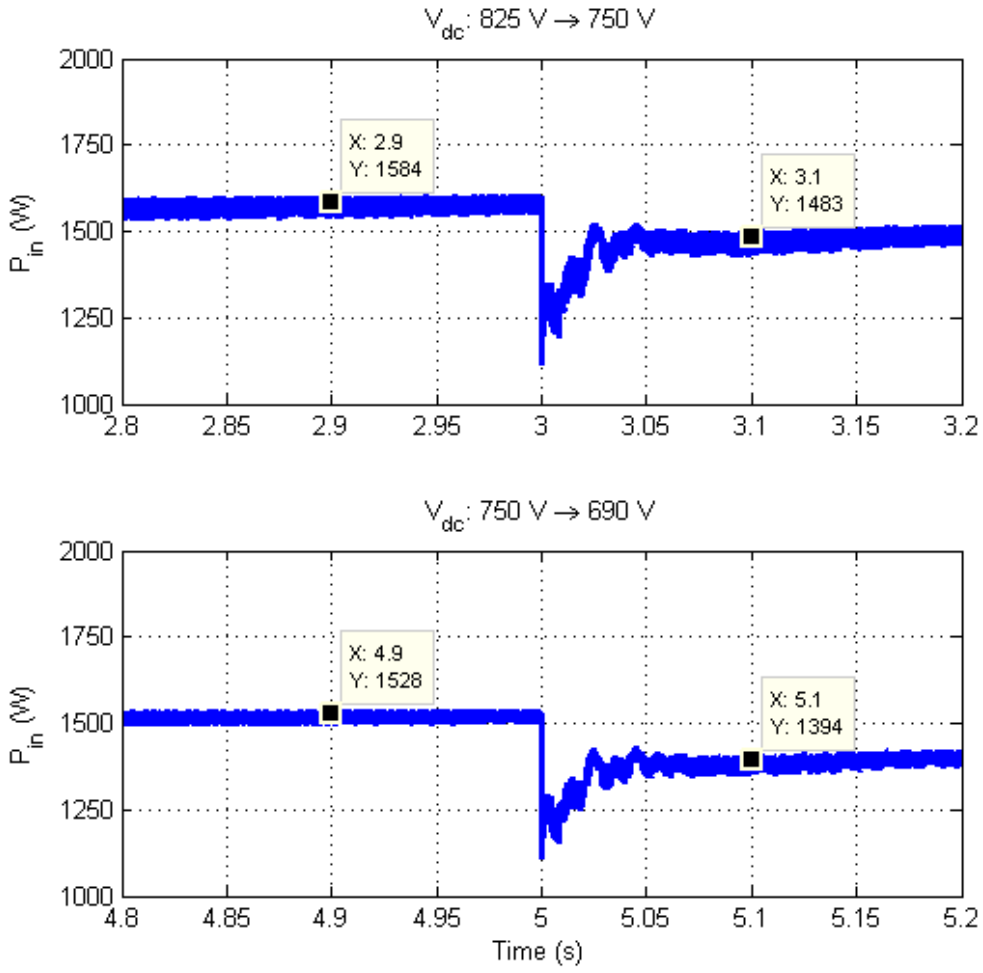


Figure 5.33: Changes in Active Power Input of the Inverter (Simulink)

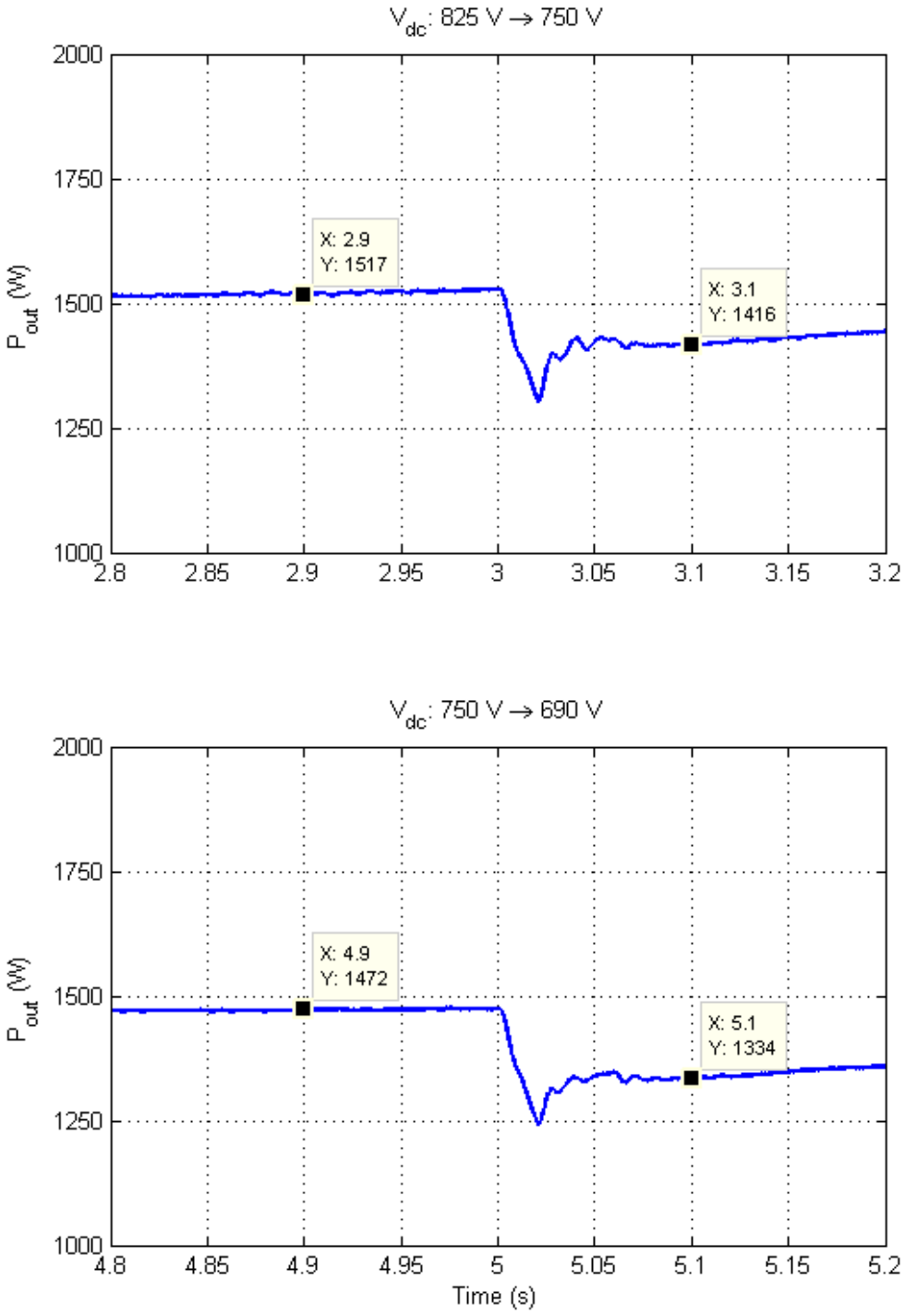


Figure 5.34: Changes in Active Power Output of the Inverter (Simulink)

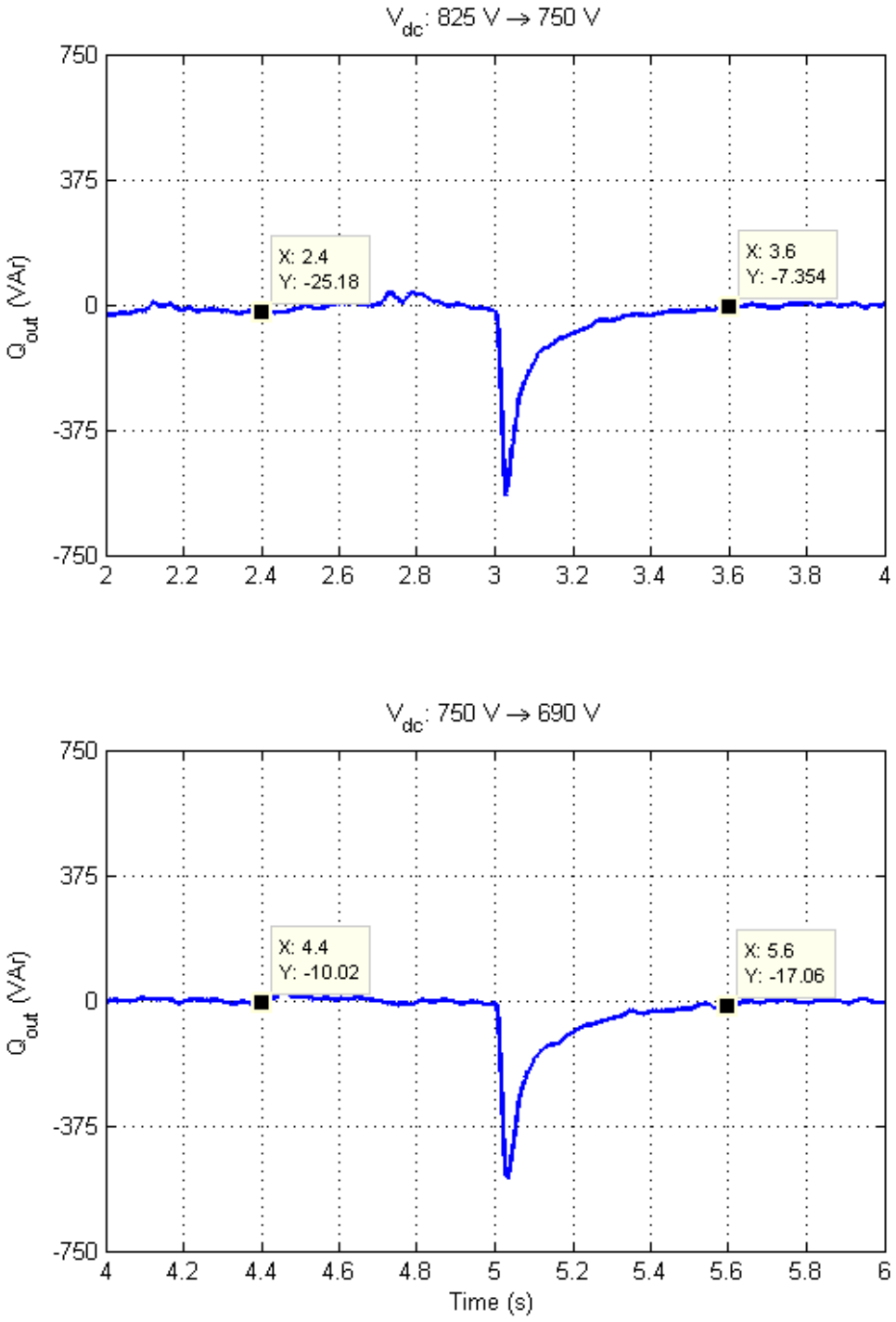


Figure 5.35: Changes in Reactive Power Output of the Inverter (Simulink)

5.2 Experimental Results

The simulated grid-connected inverter is implemented on a PCB and tested in the laboratory within this thesis work. For PCB design, Proteus Professional software is used. The related schematics of the circuit drawn in ISIS platform and its PCB design drawn in ARES platform are given in Appendix A. Figure 5.36 shows the close-up photograph of the implemented PCB whereas Figure 5.37 shows the test setup in the laboratory. The list of laboratory equipments used during the tests conducted on the inverter can be found in Appendix B.

For the grid-connected inverter, the same experimental procedure used for the simulations is applied. The solar simulator is configured so that it supplied three different DC output voltages according to the changes in the temperature. The simulator is configured as a solar panel string rated at 600 W_{mppt} and 667 V_{mppt} at 0°C. Although the rated power of the designed inverter is 1600 W, simulated solar panels are configured for lower MPPT power and voltage because of the problems encountered during circuit operation. The temperature of the panels is changed from 0°C (Case I) to 30°C (Case II) and then to 60°C (Case III). The corresponding maximum power point voltages are 667, 614, and 560 V, respectively, which are supplied as the input to the inverter. In the following subsections, the results acquired from the tests conducted will be given.

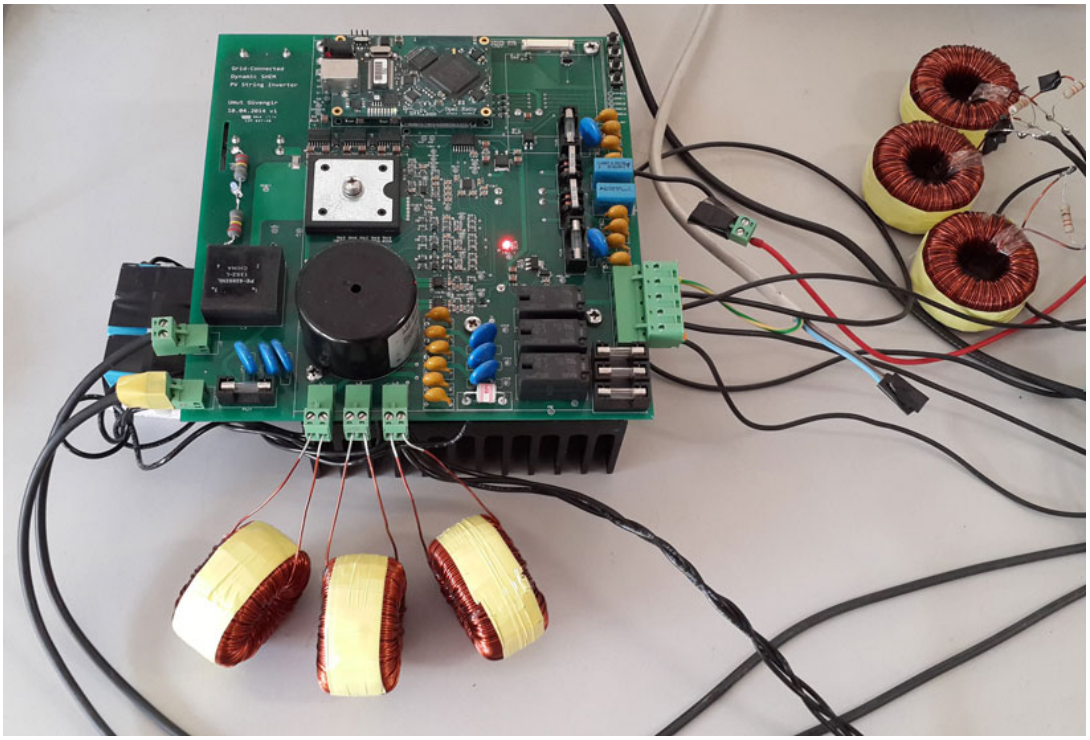


Figure 5.36: Close-up Photograph of the Implemented PCB

Figure 5.37: Test Setup in the Laboratory

5.2.1 Grid Voltage and PLL Output

Figure 5.38 shows the three-phase grid voltage and the PLL output for phase A, B, and C. The measured voltage has a considerable switching noise on it because of a problem in the differential amplifier circuit; however, the calculations are not affected due to the digital filter implemented in the FPGA code. Therefore, the PLL module successfully finds the zero-crossings of the grid voltage.

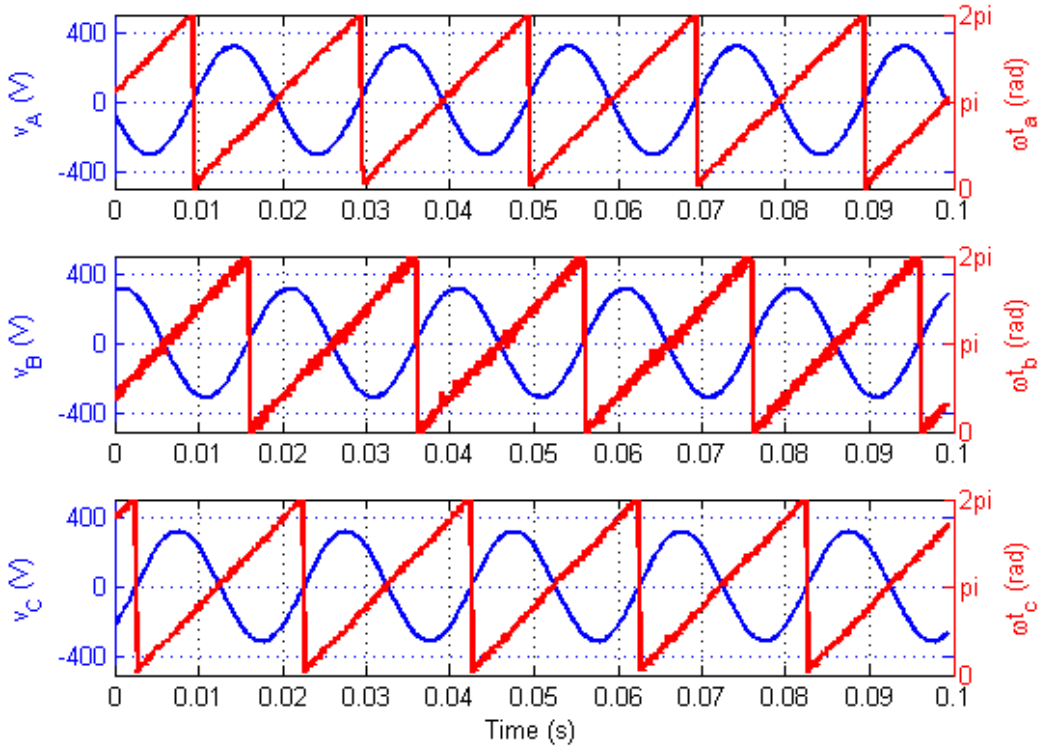


Figure 5.38: Three-Phase Grid Voltage and PLL Output for Each Phase (Experimental)

5.2.2 Input DC Link Voltage

Figure 5.39 shows the changes in the input DC link voltage whereas Figure 5.40 shows the voltage ripple in this voltage for all three cases. As can be seen from the figures, the DC link voltages are less than the MPPT voltages since the inverter showed better performance in the constant current region of the solar simulator. The input DC link voltage ripple is observed to be around 20 V.

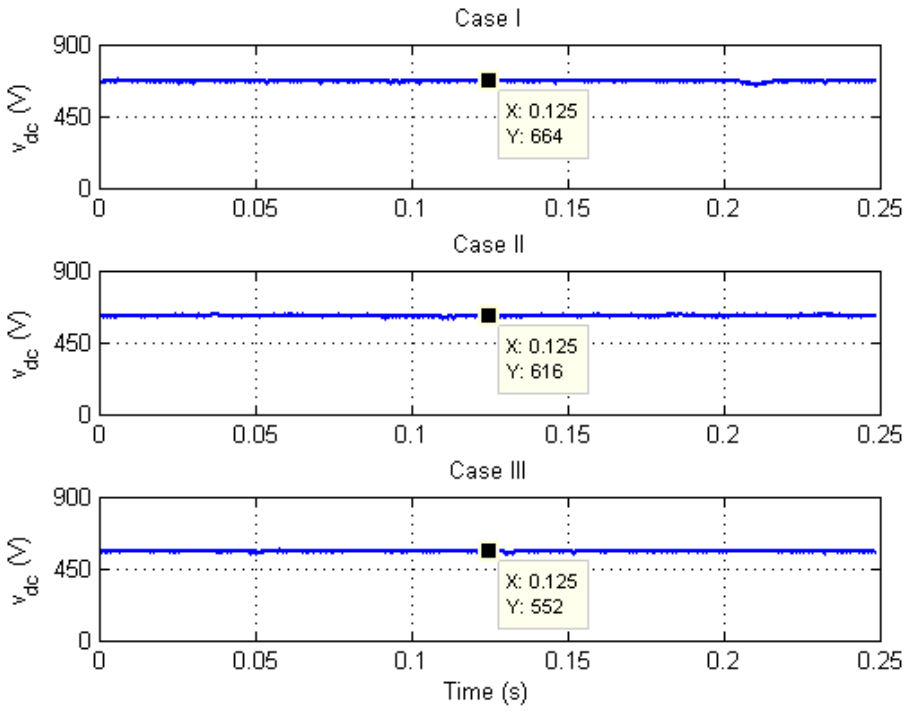


Figure 5.39: Input DC Link Voltage of the Inverter (Experimental)

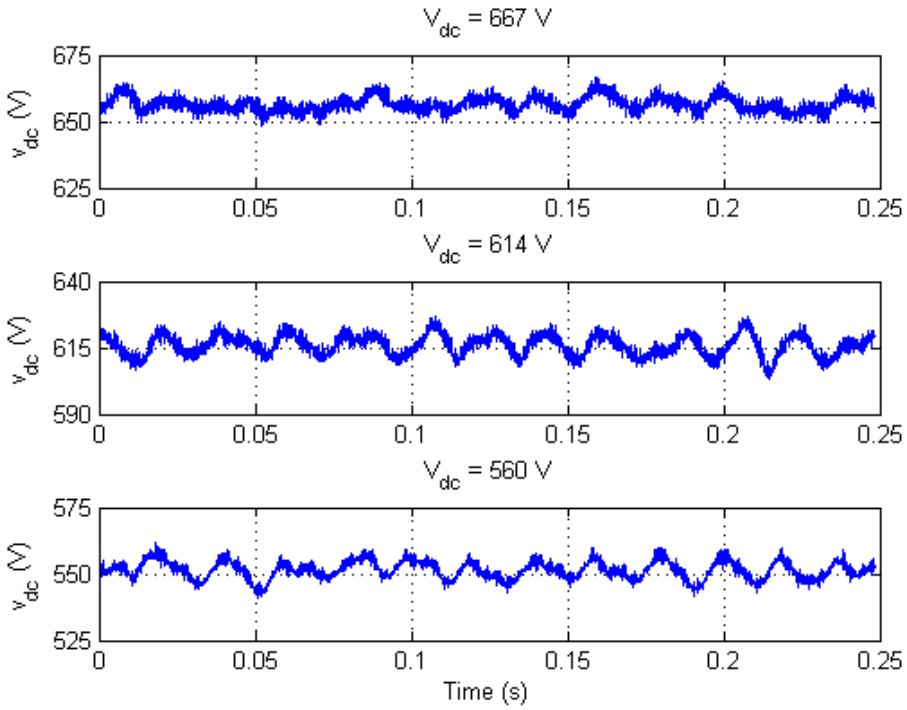


Figure 5.40: Input DC Link Voltage Ripple of the Inverter (Experimental)

5.2.3 Modulation Index and Switching Angles

Table 5.3 shows the modulation index values and the corresponding sets of switching angles found by the PSO module in the FPGA code for each case. These data are acquired from the FrontPanel GUI interface implemented for tracing and controlling the signals in the code, as investigated in Section 5.1.2. During the experiments, it was seen that the modulation index is updated by the PI controller to counter the reactive power error successfully; however, the controller requires more parameter tuning for faster response.

Table 5.3: Switching Angles Found by PSO Module of FPGA for Each Case

Case	**I**	**II**	**III**
V_{dc} (V)	667.5	613.8	560.0
P_{in} (W)	608.1	559.2	510.2
M	0.724	0.808	0.862
$\alpha_1(^\circ)$	4.751	5.314	5.678
$\alpha_2(^\circ)$	14.625	14.741	14.814
$\alpha_3(^\circ)$	17.328	17.646	17.828
$\alpha_4(^\circ)$	66.300	67.282	68.363
$\alpha_5(^\circ)$	69.531	69.194	69.409
$\alpha_6(^\circ)$	81.336	82.391	83.383
$\alpha_7(^\circ)$	85.258	85.062	85.246

5.2.4 Inverter Output Voltage

Figure 5.41 shows the inverter midpoint output voltage for Leg A (v_{An}) while Figure 5.42 shows the inverter line-to-line output voltage (v_{AB}) for all three cases. The FFT analysis of the inverter midpoint output voltage is again included in Figure 5.43 to show how TLN1 technique eliminates 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, and 19^{th} harmonics in the line-to-neutral output voltage. The FFT analyses of the line-to-line inverter output voltage show that the specified harmonics are eliminated successfully, depicted in Figure 5.44, Figure 5.45, and Figure 5.46.

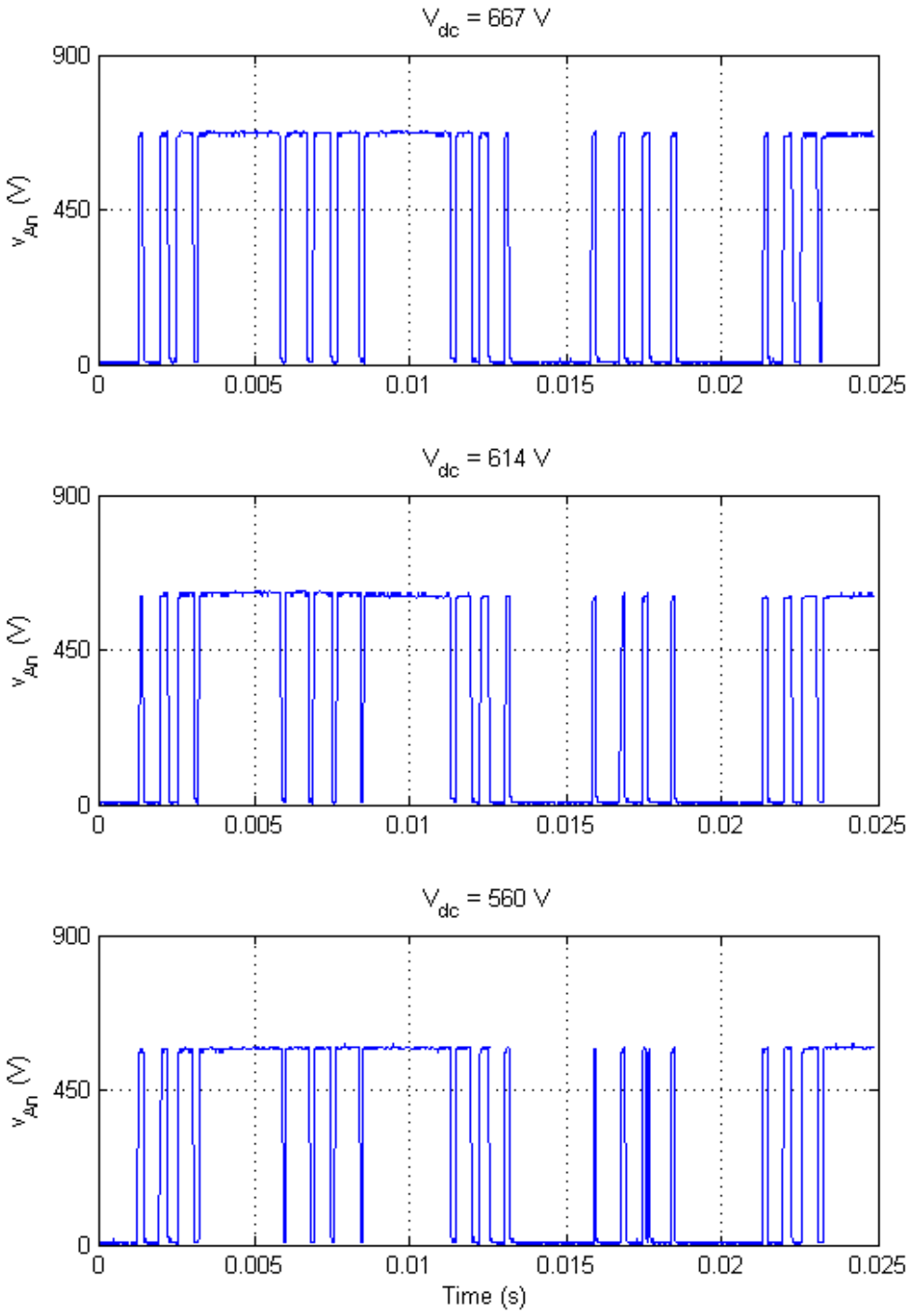


Figure 5.41: Inverter Midpoint Output Voltage for Each Case (Experimental)

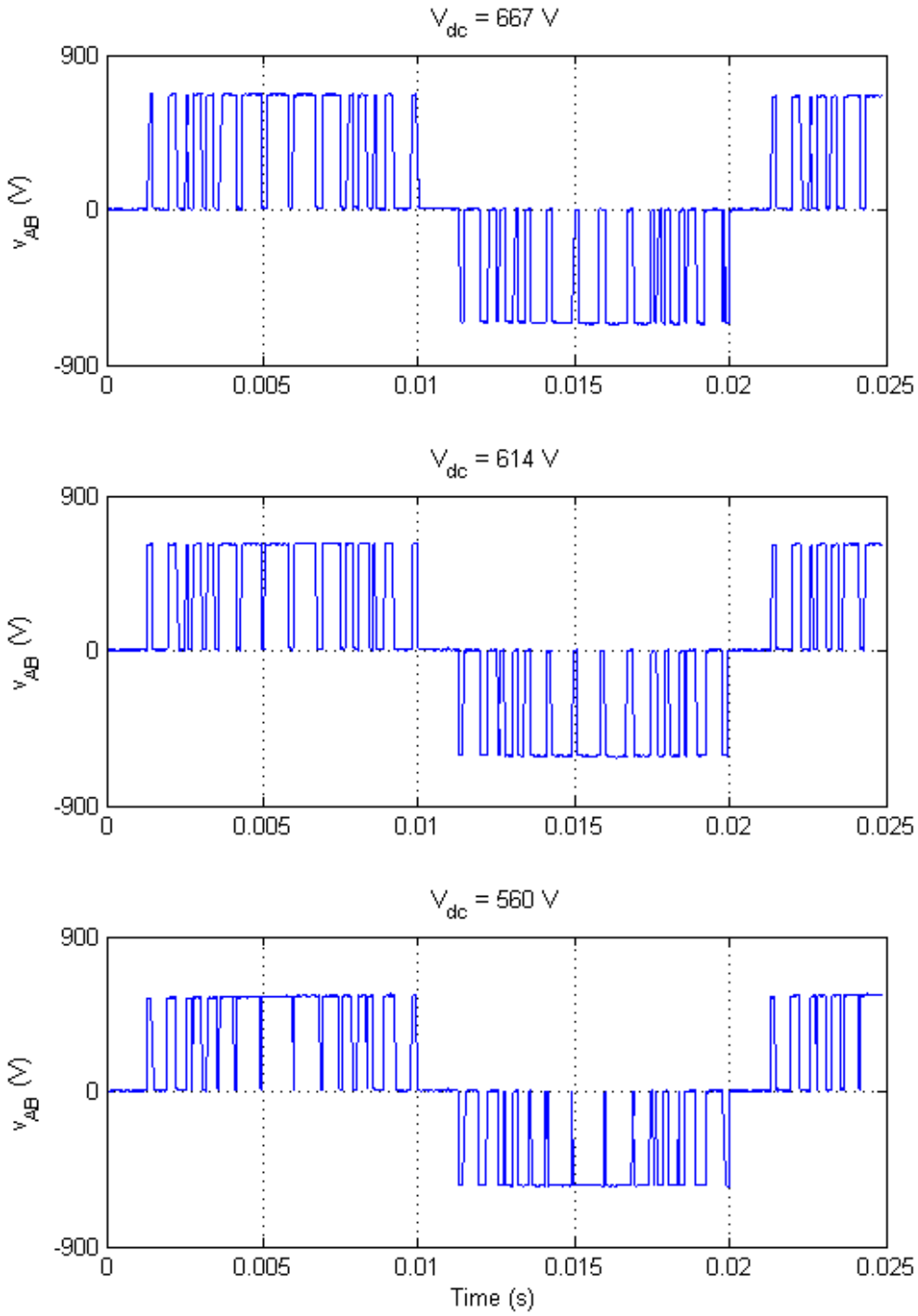


Figure 5.42: Inverter Line-to-Line Output Voltage for Each Case (Experimental)

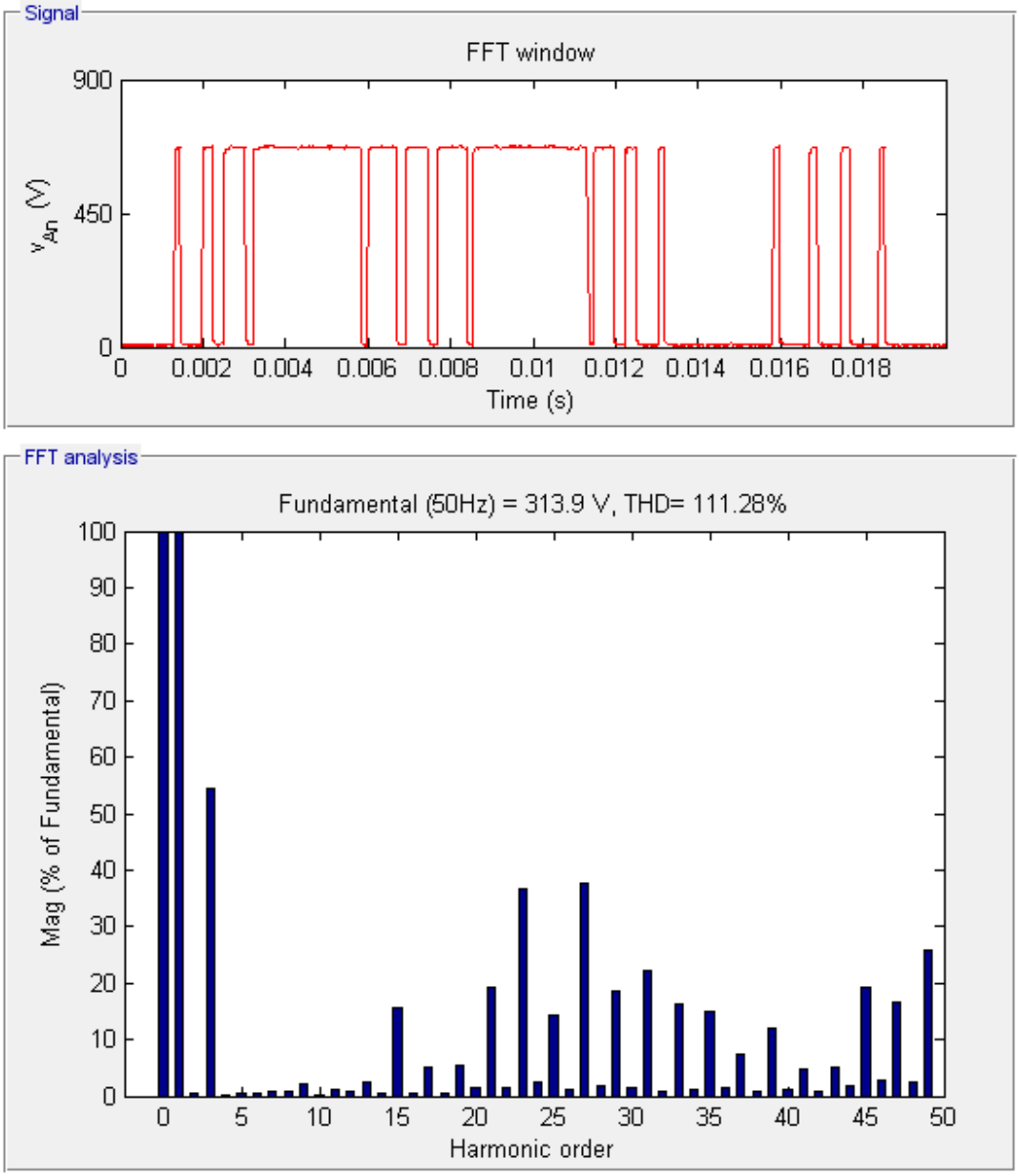


Figure 5.43: FFT Analysis of the Inverter Midpoint Output Voltage for Case I (Experimental)

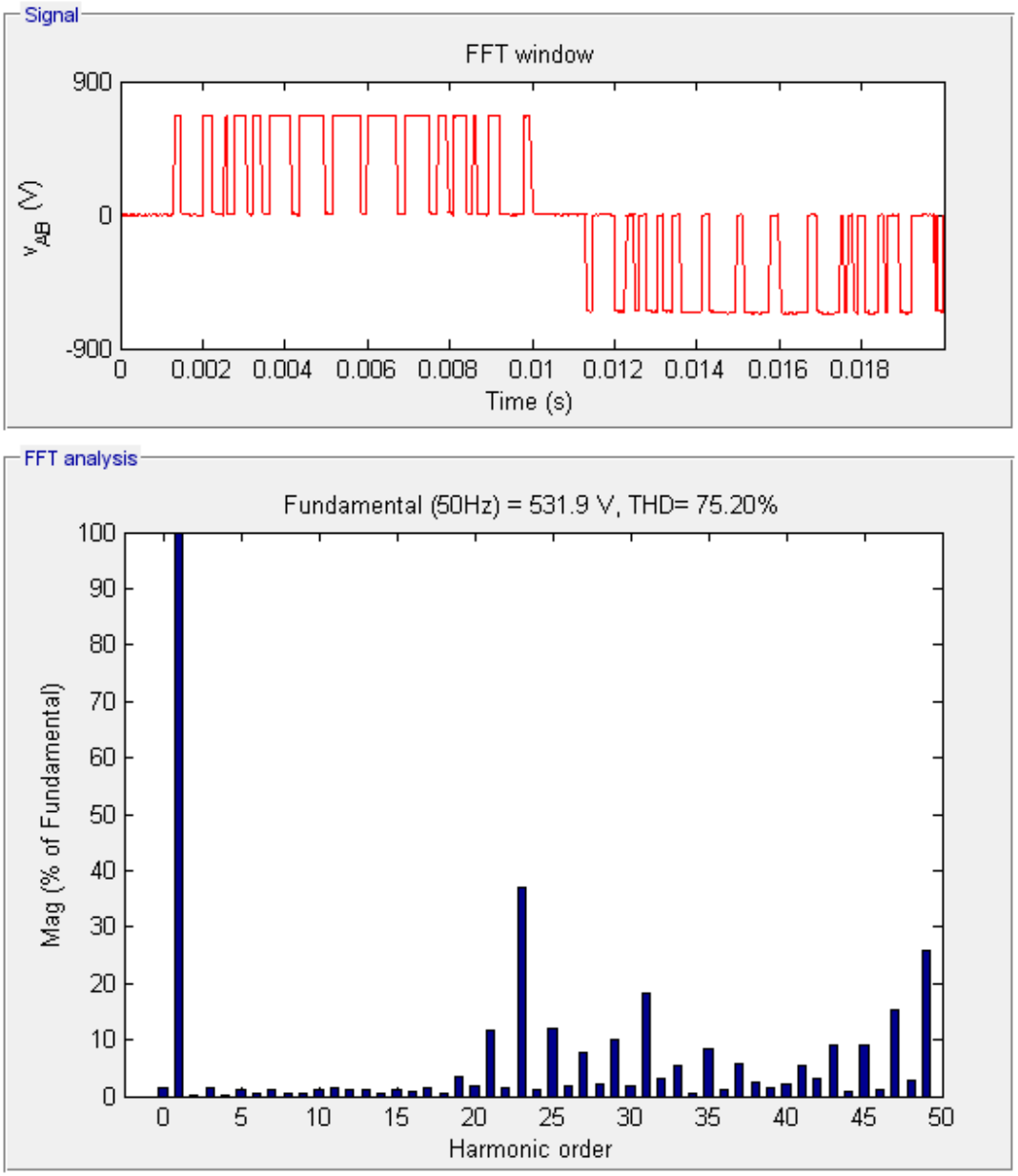


Figure 5.44: FFT Analysis of the Line-to-Line Output Voltage for Case I (Experimental)

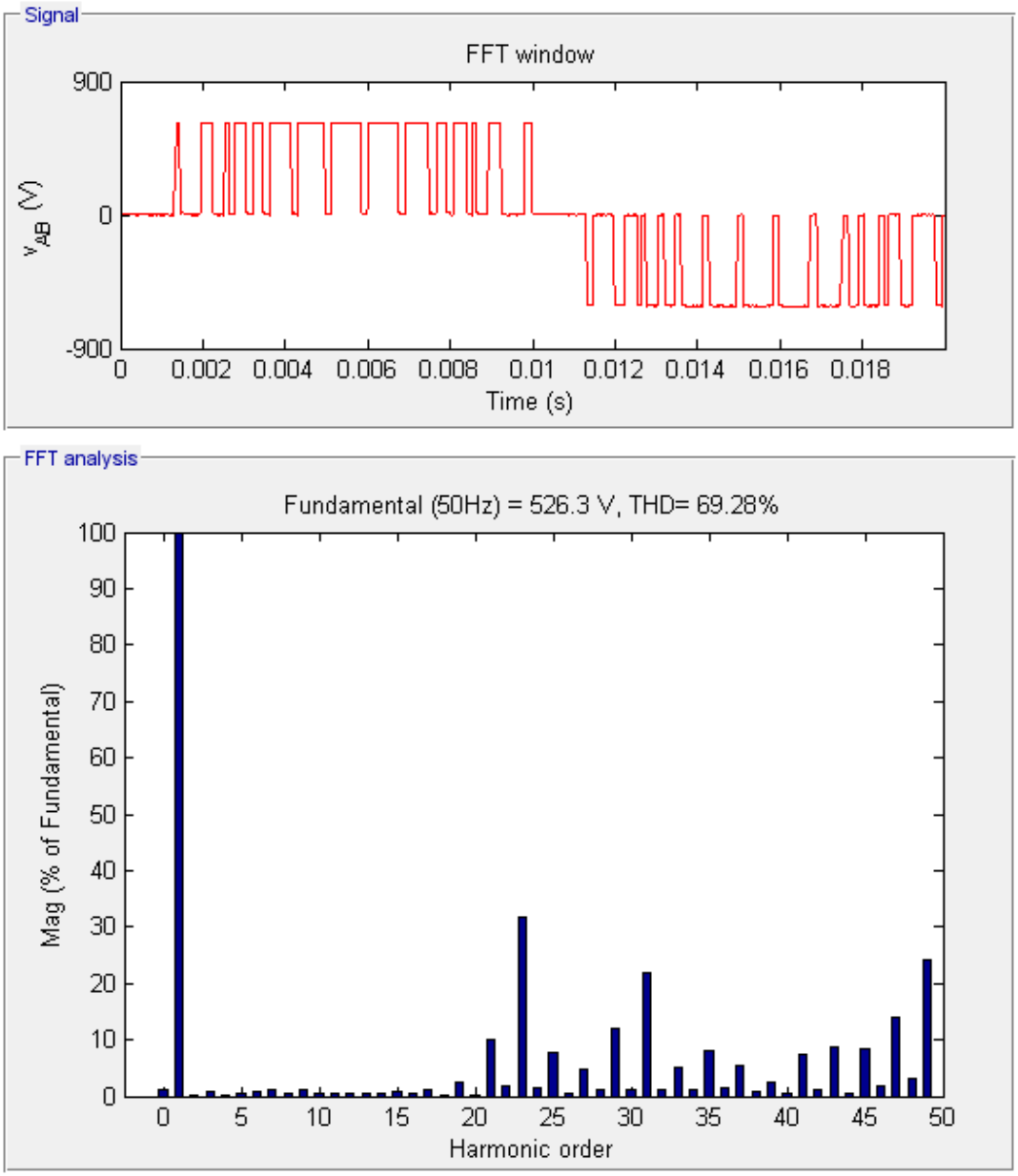


Figure 5.45: FFT Analysis of the Line-to-Line Output Voltage for Case II (Experimental)

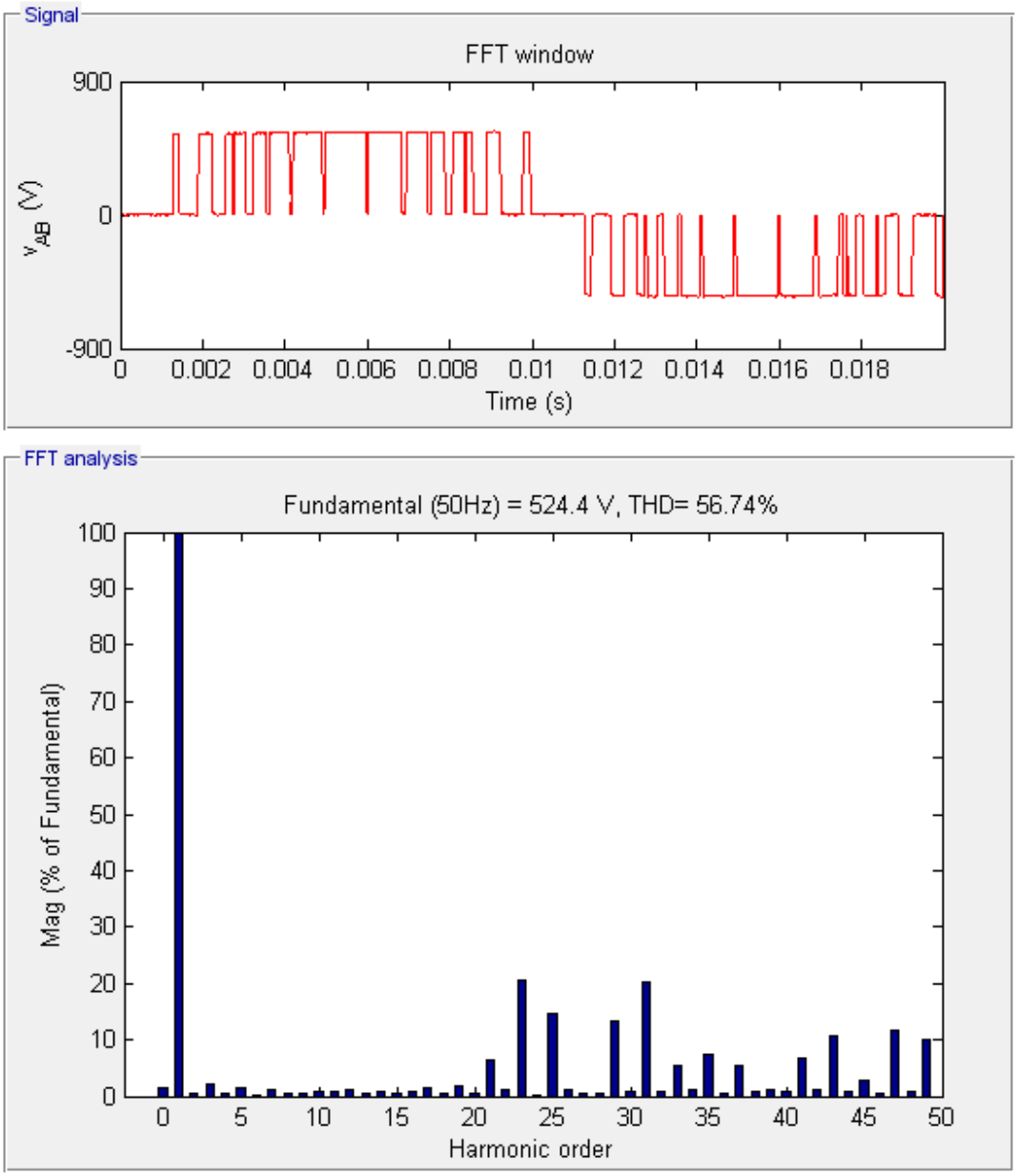


Figure 5.46: FFT Analysis of the Line-to-Line Output Voltage for Case III (Experimental)

5.2.5 Inverter and Grid Side Output Currents

During the several tests conducted in the laboratory of TÜBİTAK MAM Ankara Branch, it has been realized that the grid voltage contains too much 5^{th} and 7^{th} harmonics due to the uninterruptible power supply (UPS) connected at the main distribution box of the building. Since the resonant frequencies of the LCL filter used at the output of the inverter coincide with these harmonics as found from the simulations, the circuit operation was limited to low power levels for the tests conducted. Therefore, inverter and grid side output current data could not be acquired successfully in the laboratory.

For this reason, it has been decided that the inverter should be tested at a laboratory where harmonics caused by the UPS are low. Since a passive filter is already installed in the electrical machines and power electronics laboratory in our department, the grid voltage contains much less harmonics caused by the UPS and consequently has low THD values. Moreover, the capacitance of the capacitor in the LCL filter has been decreased to 16 μF so that the resonant frequencies do not coincide with low-order harmonics. The effect of these improvements can be seen from the harmonic analysis of the grid-side LCL filter current when the inverter is idle from Figure 5.47 and Figure 5.48, which are recorded in the TÜBİTAK laboratory and the department laboratory, respectively.

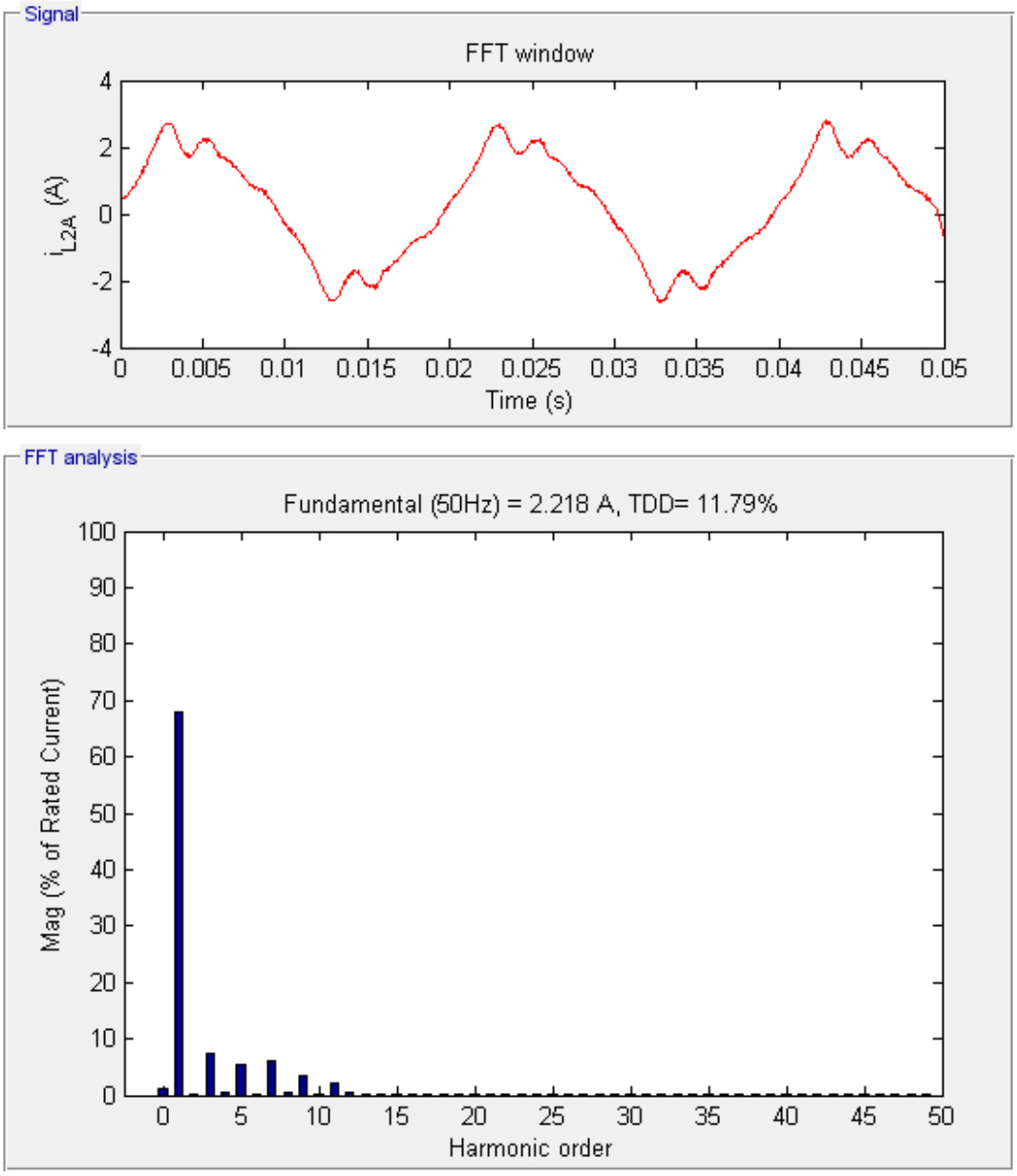


Figure 5.47: Grid-Side LCL Filter Current Recorded in TÜBİTAK Laboratory When the Inverter is Idle (Experimental)

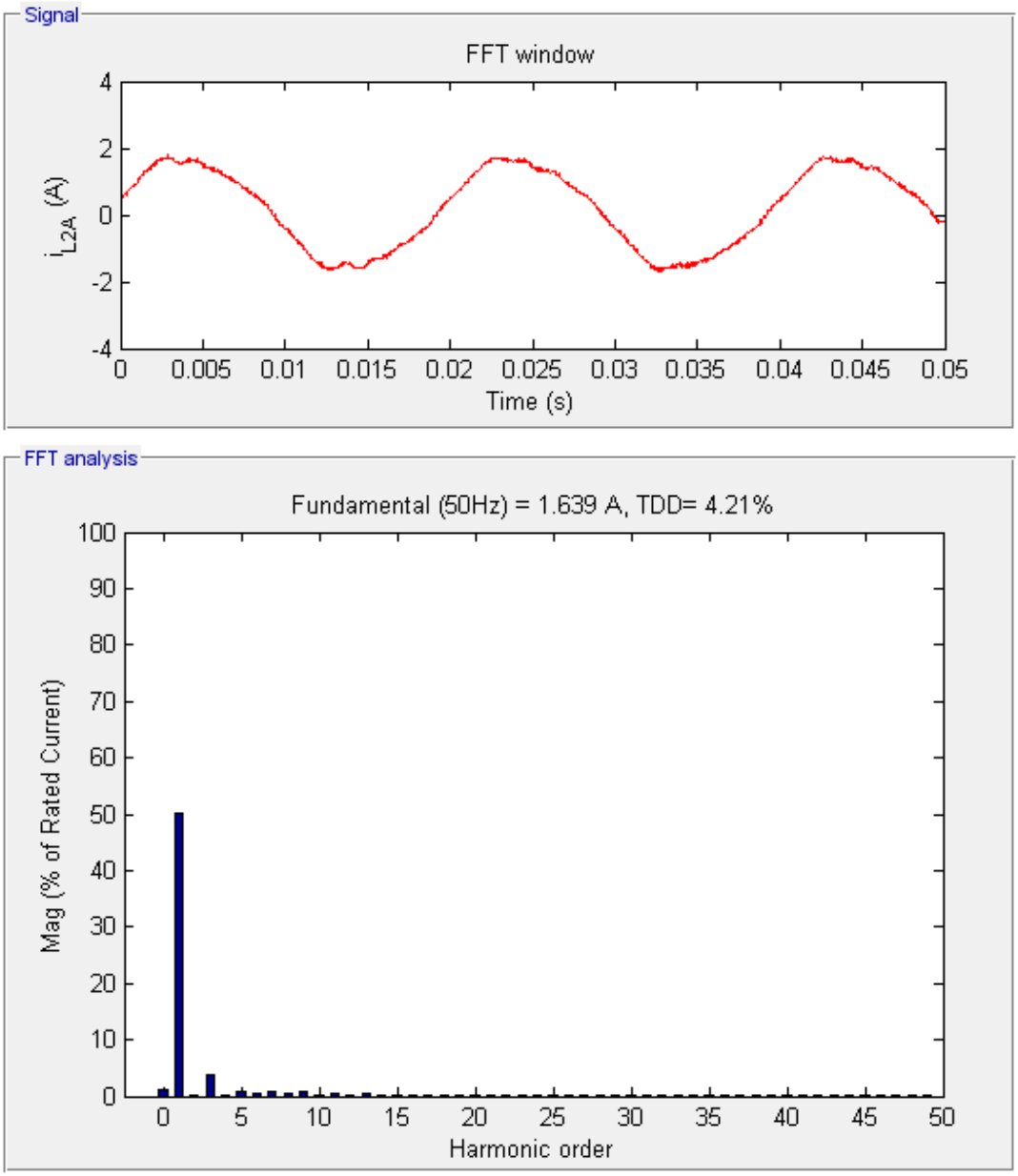


Figure 5.48: Grid-Side LCL Filter Current Recorded in Department Laboratory When the Inverter is Idle (Experimental)

Due to the operation of nonlinear loads like arc and ladle furnaces of the heavy-industry plants, power electronics equipment, and other adverse effects originated by the consumers, sinusoidal waveforms of current and voltage are distorted and they include harmonics whose frequencies are at multiples of the fundamental frequency [71, 72]. The corner frequencies of the LCL filter used in the inverter are too low that they coincide with these low-order harmonics caused by UPS and other background harmonics, and the inverter is sinking low-order harmonics from the grid, which results in amplification of the harmonics in the grid current. Therefore, it is necessary to conduct a careful design of LCL filter to optimize the performance of the inverter. One solution is to increase the grid-side inductance and capacitance of the LCL filter to damp these harmonics; however, this requires using very large filter components due to low switching frequency. Another solution is to increase the switching frequency of the inverter, which helps to decrease the filter requirement. The second solution is more effective since usage of nonlinear loads connected to the common point of coupling is very common and it is very hard to find a grid in which low-order harmonics are absent. The LCL filter design has been investigated in the literature extensively, and it is necessary to use a complete design procedure, such as the one presented in [73], to achieve better and reliable performance. The implemented control loop can also be upgraded to a better controller to provide more stable and fast response in the future as described in [74].

The inverter was tested in the department laboratory with two strings of 22 thin-film solar panels rated at 1600 W at two different apparent power levels, 650 VA and 1000 VA. The inverter-side current and the grid-side current for both power levels are shown in Figure 5.49 and Figure 5.50, respectively. Figure 5.51 and Figure 5.52 show the FFT analyses of the inverter-side current whereas Figure 5.53 and Figure 5.54 show the FFT analyses of the grid-side current for both power levels, respectively. As can be seen from the figures, a TDD value of 11.56 % could be achieved for the grid-side current in the laboratory.

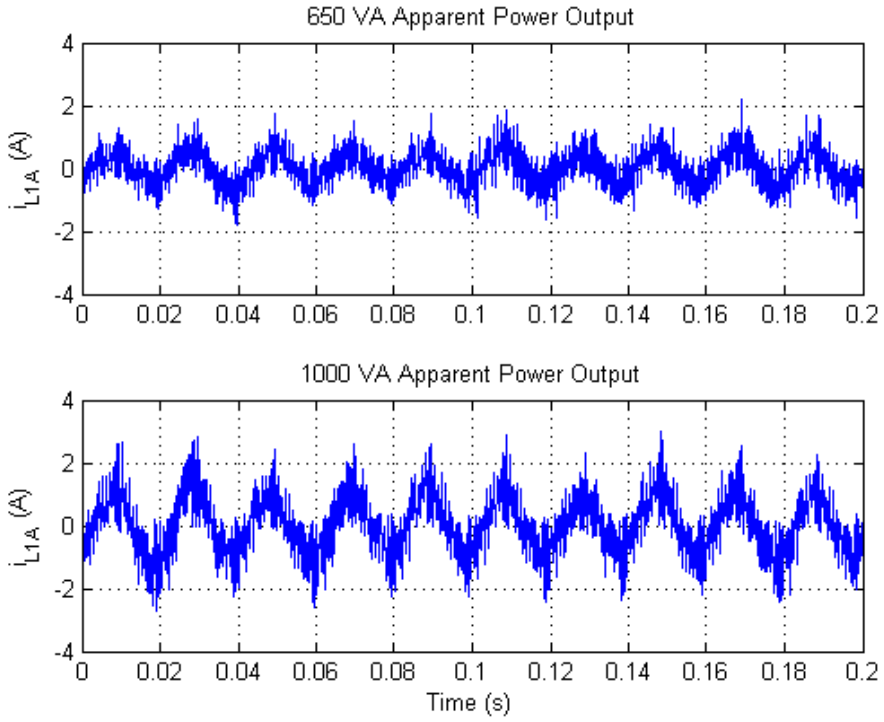


Figure 5.49: Inverter-Side Current for Different Power Outputs (Experimental)

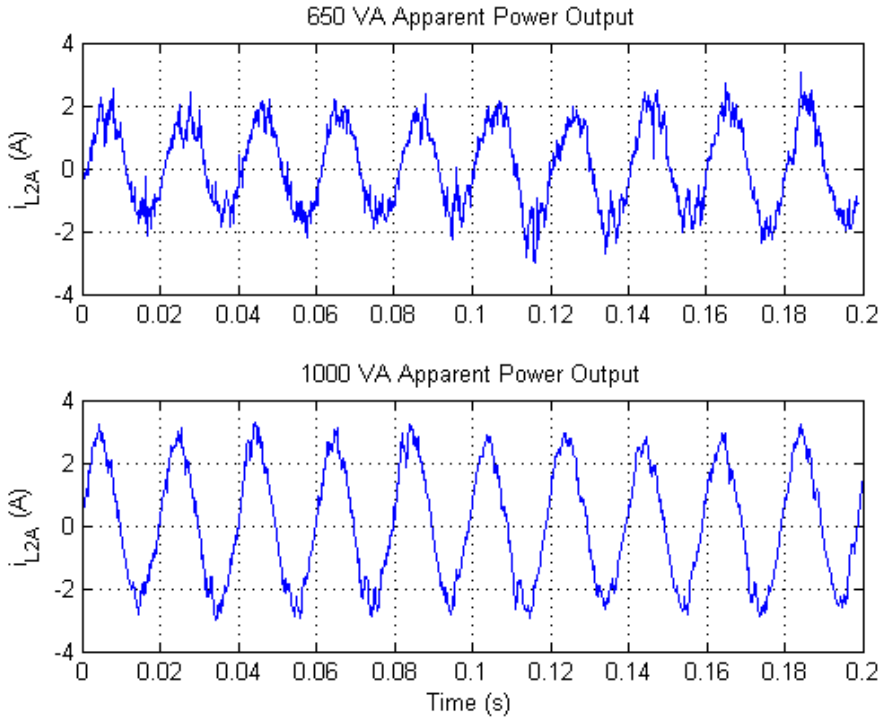


Figure 5.50: Grid-Side Current for Different Power Outputs (Experimental)

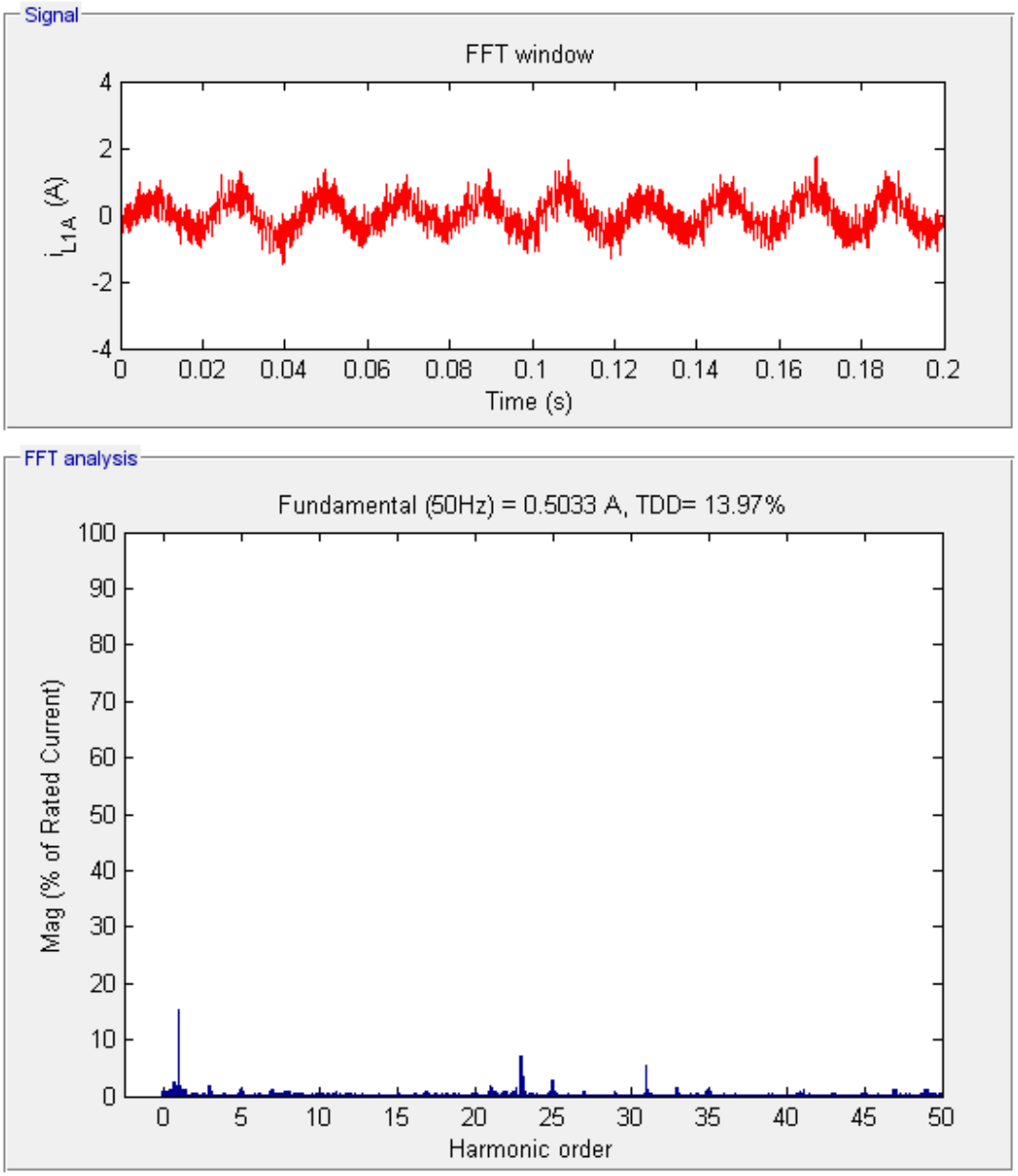


Figure 5.51: FFT Analysis of the Inverter-Side Current for 650 VA Output (Experimental)

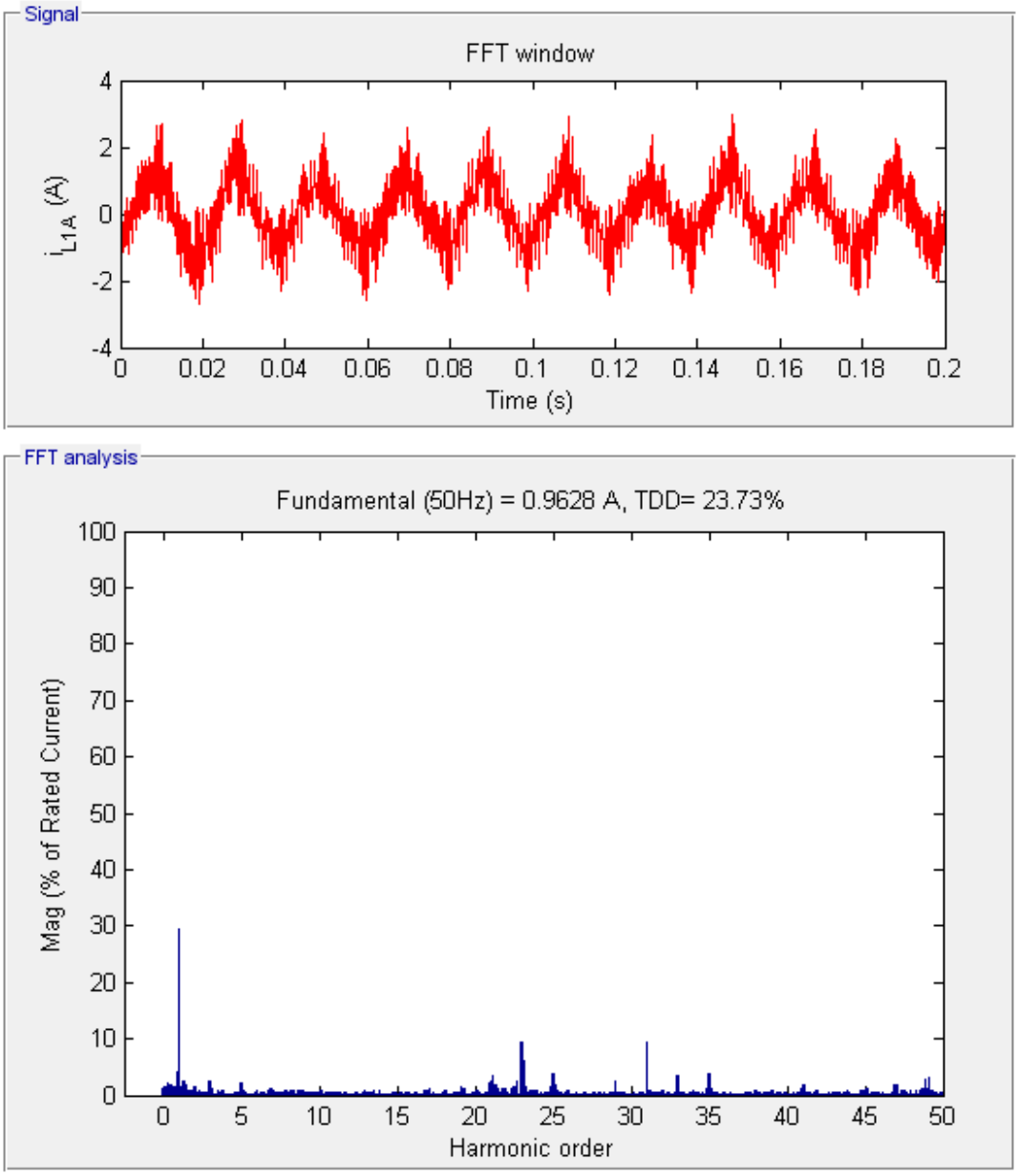


Figure 5.52: FFT Analysis of the Inverter-Side Current for 1000 VA Output (Experimental)

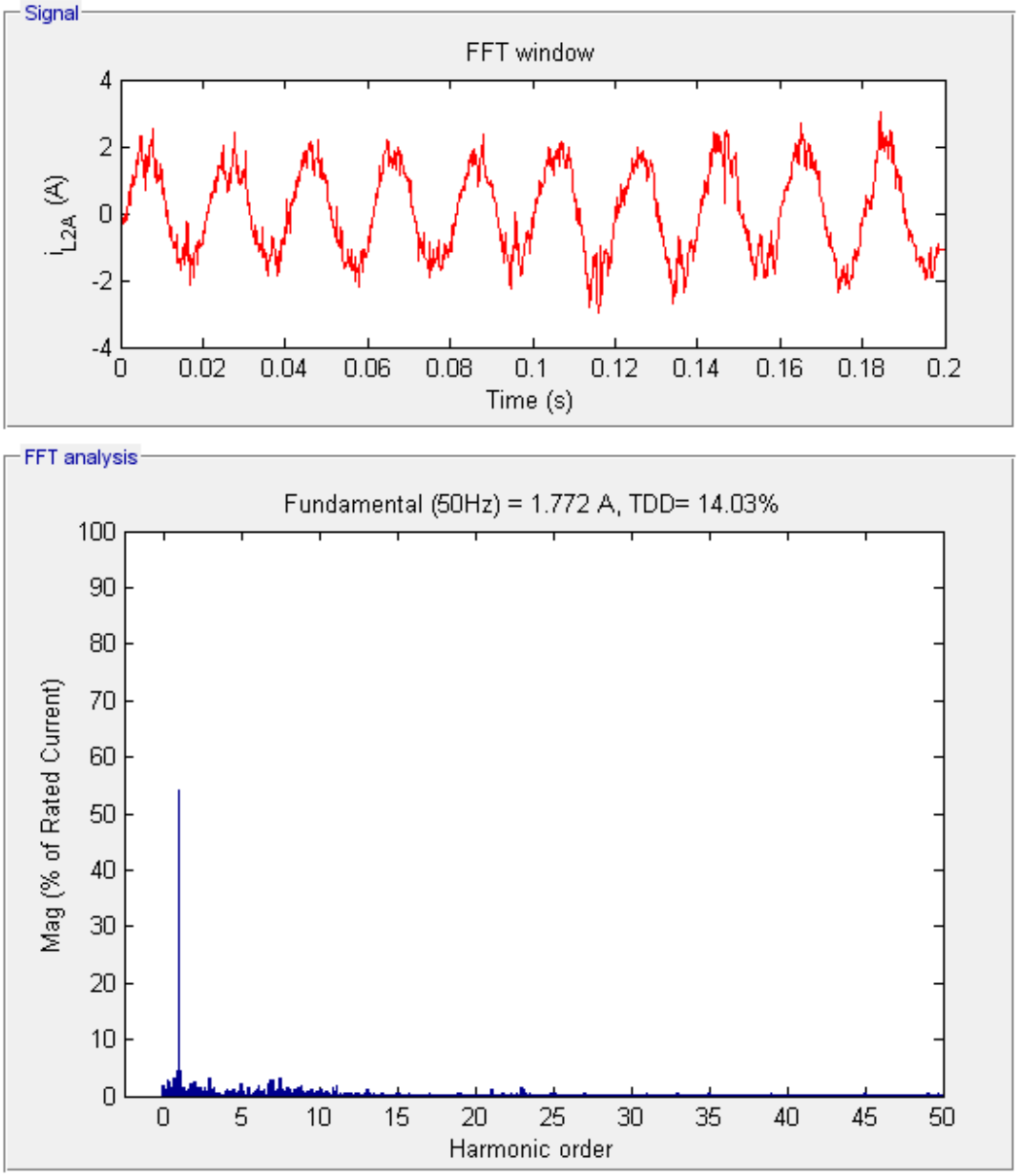


Figure 5.53: FFT Analysis of the Grid-Side Current for 650 VA Output (Experimental)

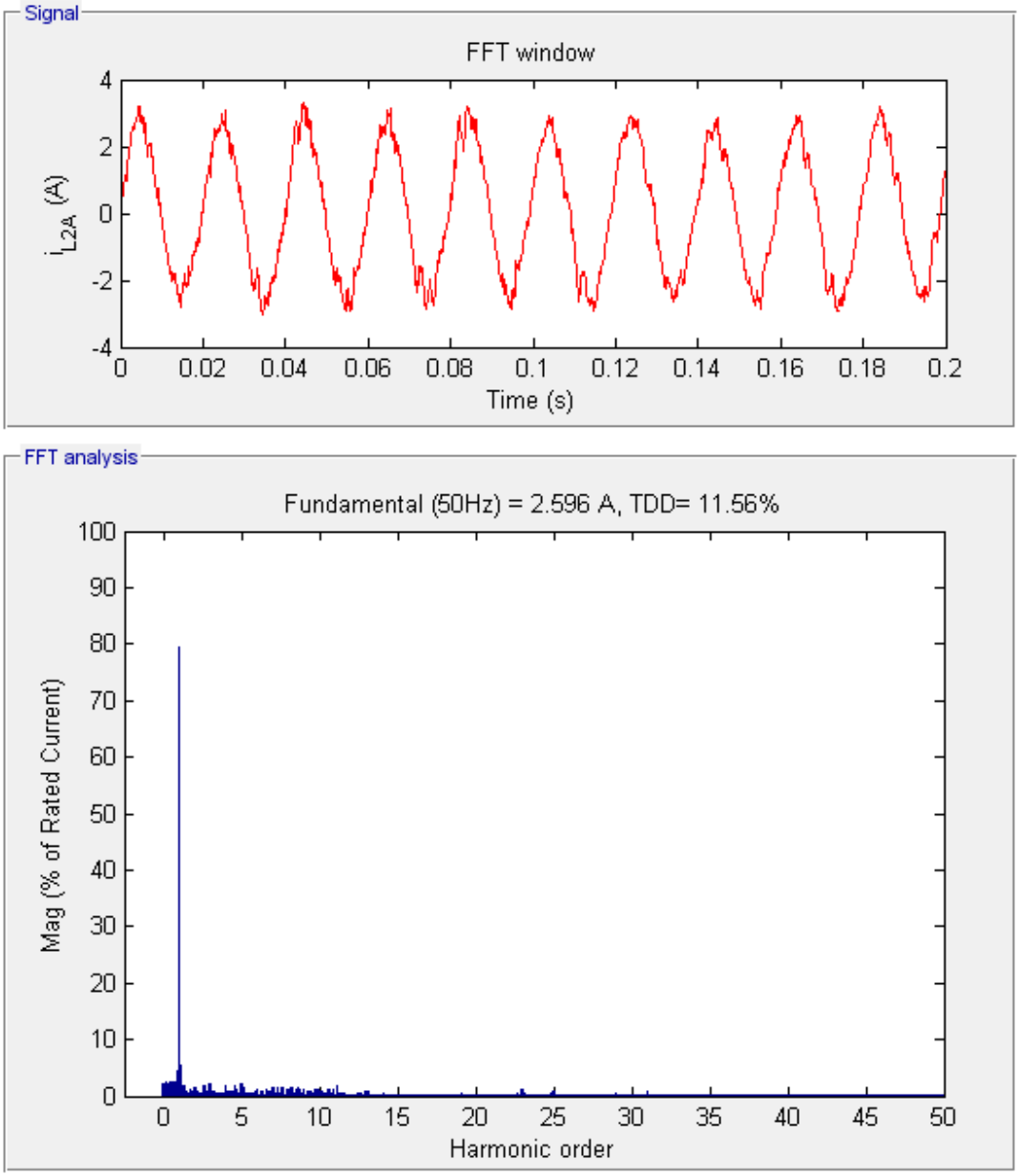


Figure 5.54: FFT Analysis of the Grid-Side Current for 1000 VA Output (Experimental)

5.2.6 Input and Output Power of the Inverter

The input power to the inverter was supplied by the solar simulator during the experiments in the TÜBİTAK laboratory, and the maximum power that can be supplied by the simulator was 608.1 W, 559.2 W, and 510.2 W for V_{dc} = 667 V (Case I), V_{dc} = 614 V (Case II), and V_{dc} = 560 V (Case III), respectively. Figure 5.55 shows the total apparent, active, and reactive power output of the inverter for all three cases with reactive power control set at Q_G=0 whereas Figure 5.56 shows these powers with reactive power control set at Q_G=500 VAr being injected into the grid. The reactive power shown is related to the fundamental output current, and the control loop manages to find the modulation index that make this reactive power zero or 500 VAr at the maximum power point of the solar panels. The efficiency of the inverter can be calculated to be 87 % with given input and output active power figures.

(a) Case I (b) Case II (c) Case III

Figure 5.55: Total Apparent, Active and Reactive Output Power of the Inverter (Q_G=0 VAr) (Experimental)

(a) Case I (b) Case II (c) Case III

Figure 5.56: Total Apparent, Active and Reactive Output Power of the Inverter (Q_G=500 VAr) (Experimental)

CHAPTER 6

CONCLUSION

Energy resources generally have fluctuated and unpredicted features, and it is necessary to supply the grid with a nearly sinusoidal output current with low total demand distortion conforming to the standards. This requires using sophisticated control methods to achieve more efficient and reliable energy conversion. Selective harmonic elimination method (SHEM) is a switching method which controls the fundamental output voltage of the inverter and eliminates specified lower-order harmonics at the same time by introducing notches in the waveform at deliberate times. Utilization of low switching frequency due to this method results in low switching losses, which is very important for the efficiency of high-power converters. Although the advantages of applying SHEM are prominent, there are also considerable disadvantages. SHEM equations are highly nonlinear, and finding the switching angle set that eliminates the specified harmonics becomes harder as the number of harmonics increases. A myriad of iterative and evolutionary algorithms have been investigated in the literature for solution of SHEM equations, which have been mentioned in Chapter 1. Being more effective than others or not, each of these methods are successful at finding the correct solution set in their own reference frames.

For applications with variable DC link voltage, a high number of solution sets should be found since the modulation index is also variable. Until recent years, finding these solutions and storing them as lookup tables in the microcontrollers in advance has been the only way to utilize SHEM for inverters. However, offline application of SHEM requires the use of discretized values of modulation

index, high storage area for lookup table, and careful inspection for the solution space where no feasible solution can be found for the SHEM equations. These drawbacks of offline application of SHEM have driven researchers to seek ways for online application in real time. With the advance of ever-increasing computing power and speed of emerging microcontroller technologies, implementation of complex search and optimization algorithms in real time has become possible and feasible. By utilizing these fast and powerful microcontrollers, it is not too hard to implement efficient, robust, dynamic, and reliable power conversion process. In this thesis work, SHEM equations have been solved in real time for switching angles that eliminate 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, and 19^{th} harmonics in the output voltage of a grid-connected inverter under variable DC link input voltage. The inverter topology is a two-level three-phase voltage source inverter, and the online application of SHEM is realized by implementing particle swarm optimization (PSO) algorithm in an FPGA controller, successfully.

Among several SHEM patterns available for two-level three-phase inverters, TLN1 technique is selected for the SHEM problem using PSO algorithm. PSO algorithm could also be applied to other techniques considering different number of harmonics to be eliminated. After formulating the cost function of the problem, the switching angle sets were found by the PSO algorithm. In the current application, global best solution was found with 10^{-9} fitness value and 250 individual particles in 200 time frames. Although a penalty coefficient has been used for infeasible candidate solutions to get rid of them in the PSO algorithm, this approach is not efficient since the knowledge about the search space acquired by these candidate solutions is lost during the search process. Implementing a heuristic function for these infeasible candidate solutions would help to redirect the corresponding particles to the feasible solution space instead of eliminating them, which would decrease the total solution time considerably in the future. Although the parameters used in the implementation stage were set by using default values and some trial-and-error approach, their separate effects on the problem were also investigated. However, the individual parameters might have effects on each other and there may be considerable coupling between them. Therefore, the effects of parameters can be assessed by a more extensive test in

the future. PSO algorithm has several advantages over genetic algorithm as discussed in the thesis; however, there are many other evolutionary algorithms in the literature that can be applied for the SHEM problem. The resulting fitness values and total solution times can be compared to observe which algorithm is more efficient than the others.

The PSO algorithm code was implemented in the FPGA as a module and online application of SHEM was successfully tested with ISim simulation on the computer and hardware co-simulation between the computer and FPGA module. With the parameters used in the PSO module, new switching angles can be found in a total time of 10 ms. Although the PSO module uses 12 % of the FPGA resources, other modules implemented for operation of the inverter increase this figure to 41 % and use nearly all of the multiplier blocks available. Therefore, only six harmonics could be eliminated online at this point. Selection of more optimized parameters, rewriting inefficient parts of the FPGA code, and use of higher resolution random number generation may result in shorter solution times and higher system frequencies for FPGA, which makes it possible to eliminate more harmonics online in less than 10 ms in the future. In this application, the utilized FPGA module does not have enough resources; however, a more advanced FPGA module can be selected by considering the characteristics of the power converter application, the cost of the FPGA module, and its resources. Therefore, the PSO algorithm parameters can be selected so that the FPGA resources are utilized in a better way.

Although the simulation results for the entire system can be regarded to be successful, there were some important points noted during the experimental work for future studies. First of all, the online application of SHEM is successfully realized with the real-time implementation of PSO algorithm in the FPGA module. Although the PSO module was successfully tested for different modulation index values, the modulation index controller, which tries to make reactive power error zero, was not as successful as the PSO module, and it gave a late response to the reactive power error. This may be related with the calculation of instantaneous reactive power in the FPGA module affected with the noise seen on the measured grid voltage. This noise problem is attributed to the differential am-

plifier circuit used for measurement although it has not been correctly addressed. Nevertheless, the implemented digital filters were found to be beneficial, and the normal circuit operation could be observed to some extent. Another important point was that the circuit operation was randomly interrupted by the current limit protection code. When the current waveforms were investigated at these moments, it was seen that one of the phase currents built up to large values in the positive or negative direction. This problem may be caused by a faulty switching in normal conditions; however, the switching waveforms were closely inspected for any problems, and necessary counter measures were taken in the FPGA code for wrong switching angle sets.

It can be observed from the results acquired in the experimental work that careful design of LCL filter is the key to the optimized performance for VSIs. The output filter used for the inverter was observed to sink low-order harmonics caused by nonlinear loads connected to the common point of coupling such as uninterruptible power supplies. It is necessary to increase the switching frequency of the inverter by adding more switching angles in the output voltage waveform of the inverter, some of which may be eliminated online. It is very essential to design the LCL filter by using guidelines in the literature in order to inject a nearly sinusoidal output current conforming to the standards with low TDD into the grid in the future.

The 1.6 kVA, 380 V, three-phase inverter was successfully simulated in Simulink with online application of SHEM. TDD values as low as 2.81 % were acquired for the grid current, and the implemented control loop was shown to reach steady state in less than 0.05 s. The inverter efficiency was calculated to be 97 % in the simulations. The inverter was designed, implemented, and tested in the TÜBİTAK MAM Ankara Branch laboratory with a solar simulator and in the electrical machines and power electronics laboratory in our department with solar panels. The inverter could be tested at power levels from 500 VA to 1000 VA in the laboratories because of the aforementioned problems, and TDD values of 11.56 % could be achieved for the grid current. The inverter efficiency was calculated to be around 87 % from the experimental results. The online application of SHEM to grid-connected inverters with variable DC link

voltage by implementing PSO algorithm in the FPGA module in real time was successfully shown to complete in 10 ms as can be seen from ISim simulations and hardware co-simulation results presented. In the future, the mindset of this research can be applied to other topologies and applications, such as multilevel inverters and STATCOMs, for which SHEM can be applied.

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APPENDIX A

PCB SCHEMATICS DRAWN IN PROTEUS PROFESSIONAL

The PCB design of the grid-connected inverter is realized in the Proteus Professional software. This software consists of two platforms, the ISIS platform in which the circuit schematics of the inverter is drawn and the ARES platform in which the PCB layout of the circuit is drawn.

The input protection components, IGBT module, output LCL filter, and current measurement components are shown in Figure A.1.

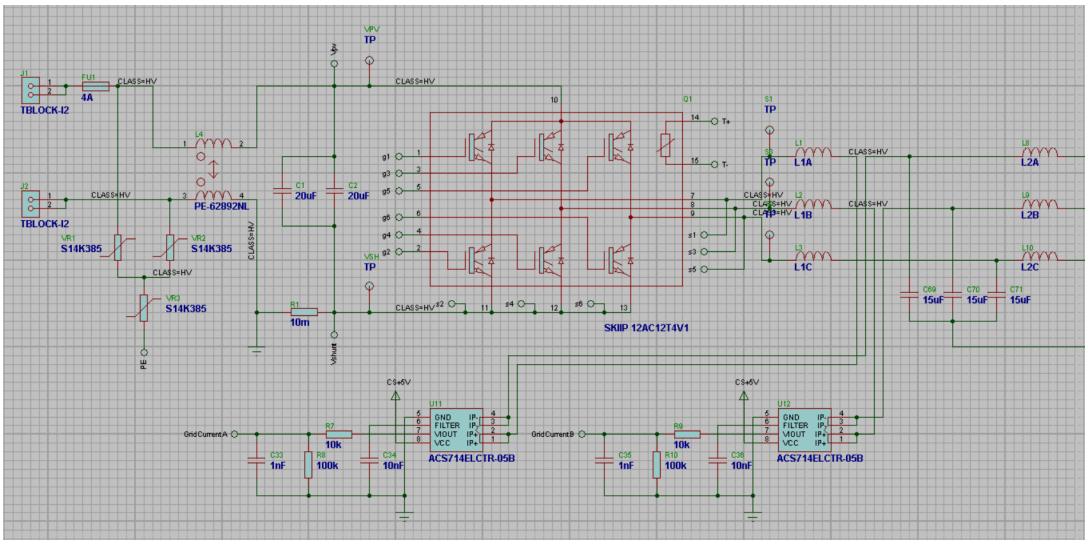

Figure A.1: Input Protection, Inverter, and Current Measurement Components

Output common-mode filter and output protection components are shown in Figure A.2.

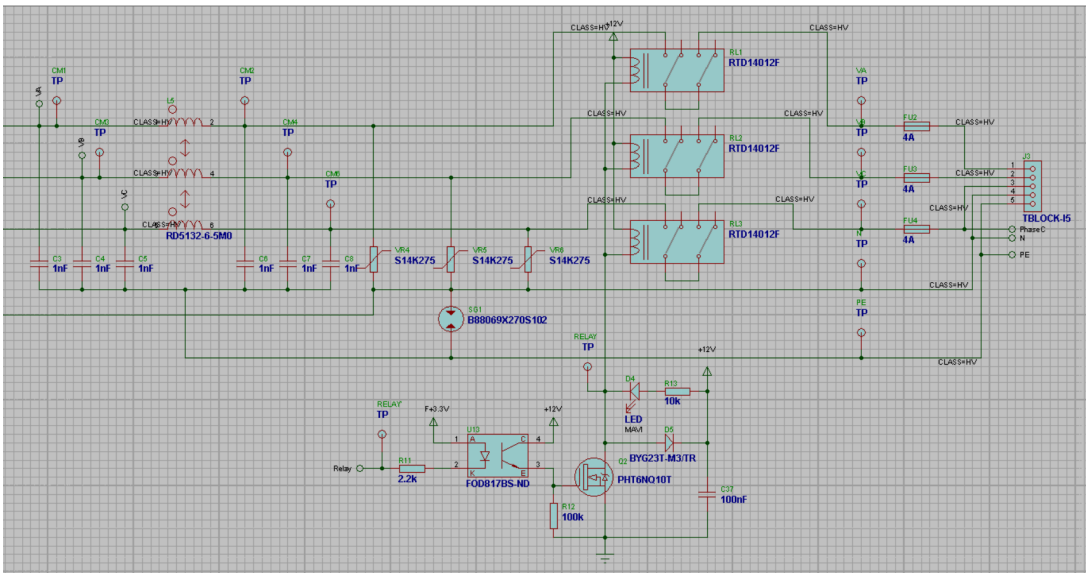

Figure A.2: Output Common-Mode Filter and Protection Components

Gate driver components for the IGBT module are shown in Figure A.3.

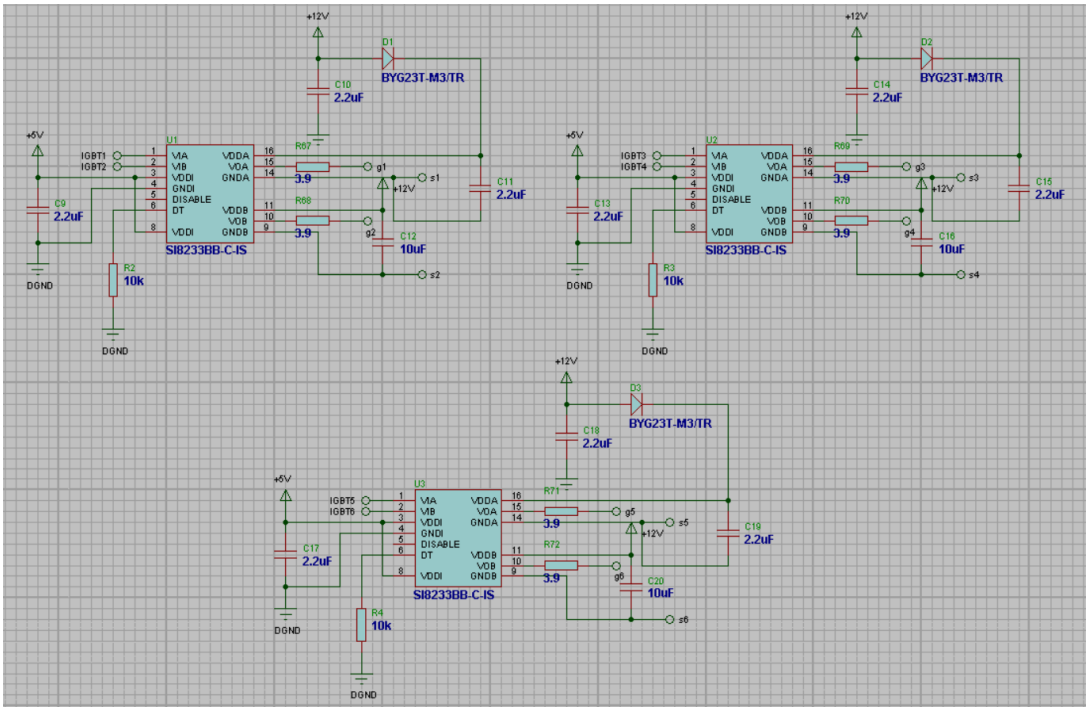

Figure A.3: Gate Driver Components

ADC, ADC isolator, and DAC circuit components are shown in Figure A.4.

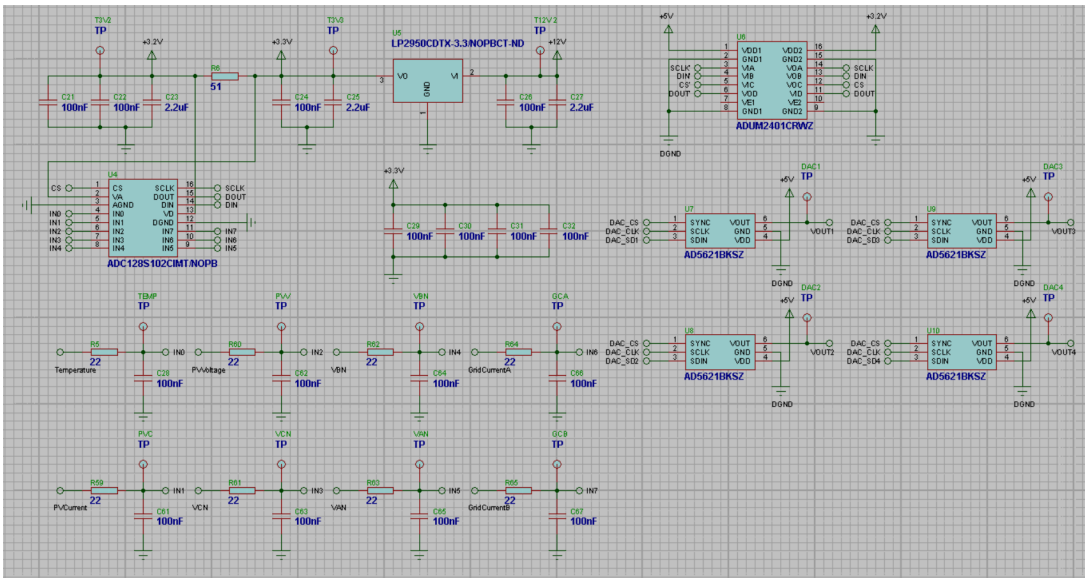

Figure A.4: ADC, ADC Isolator, and DAC Components

Input DC voltage and current, IGBT temperature, and output line-to-neutral voltage measurement circuit components are shown in Figure A.5.

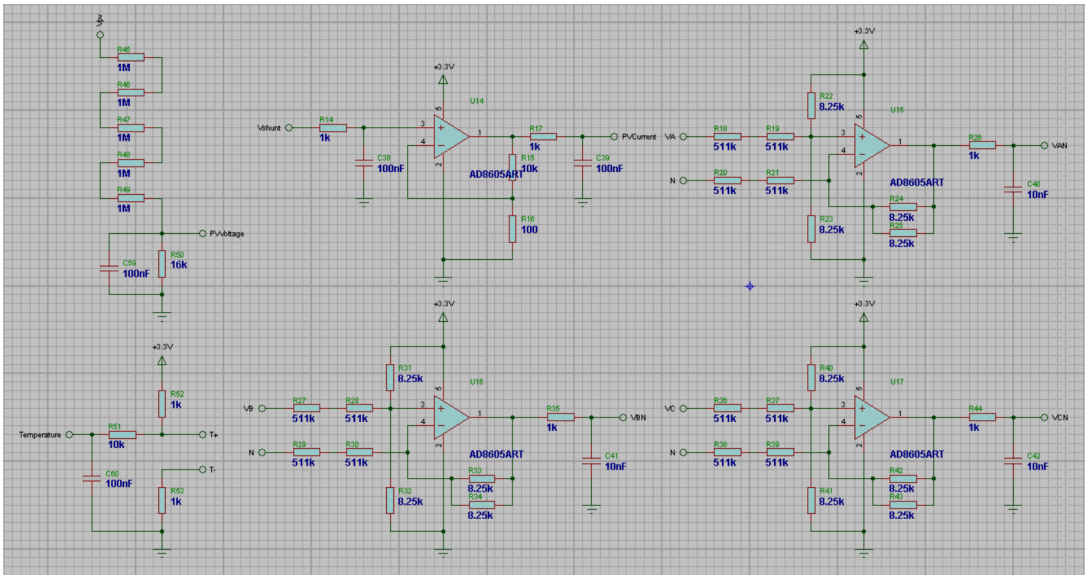

Figure A.5: Measurement Circuit Components

Power supply components are shown in Figure A.6.

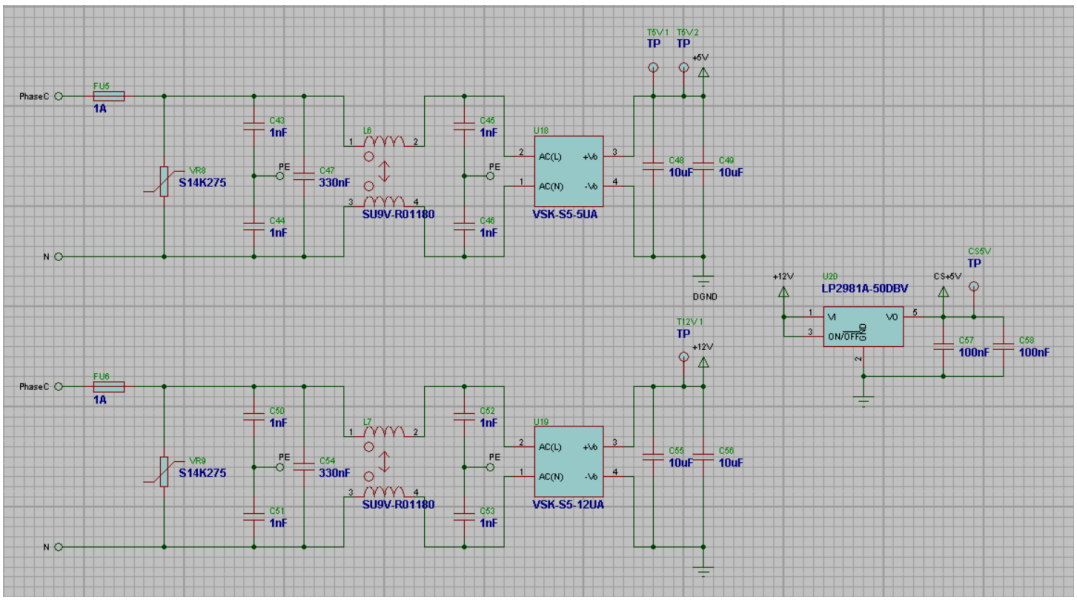

Figure A.6: Power Supply Components

FPGA, LED display, and other circuit components are shown in Figure A.7.

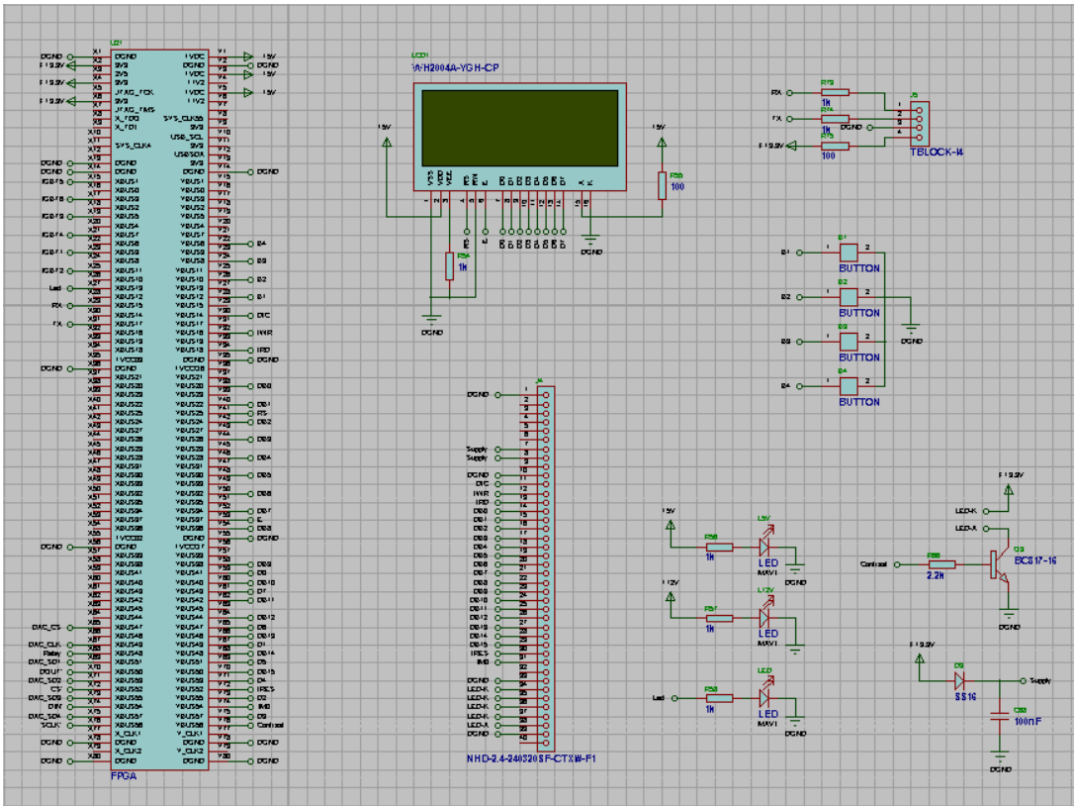

Figure A.7: FPGA and Other Circuit Components

Finally, PCB layout drawn in ARES platform is shown in Figure A.8.

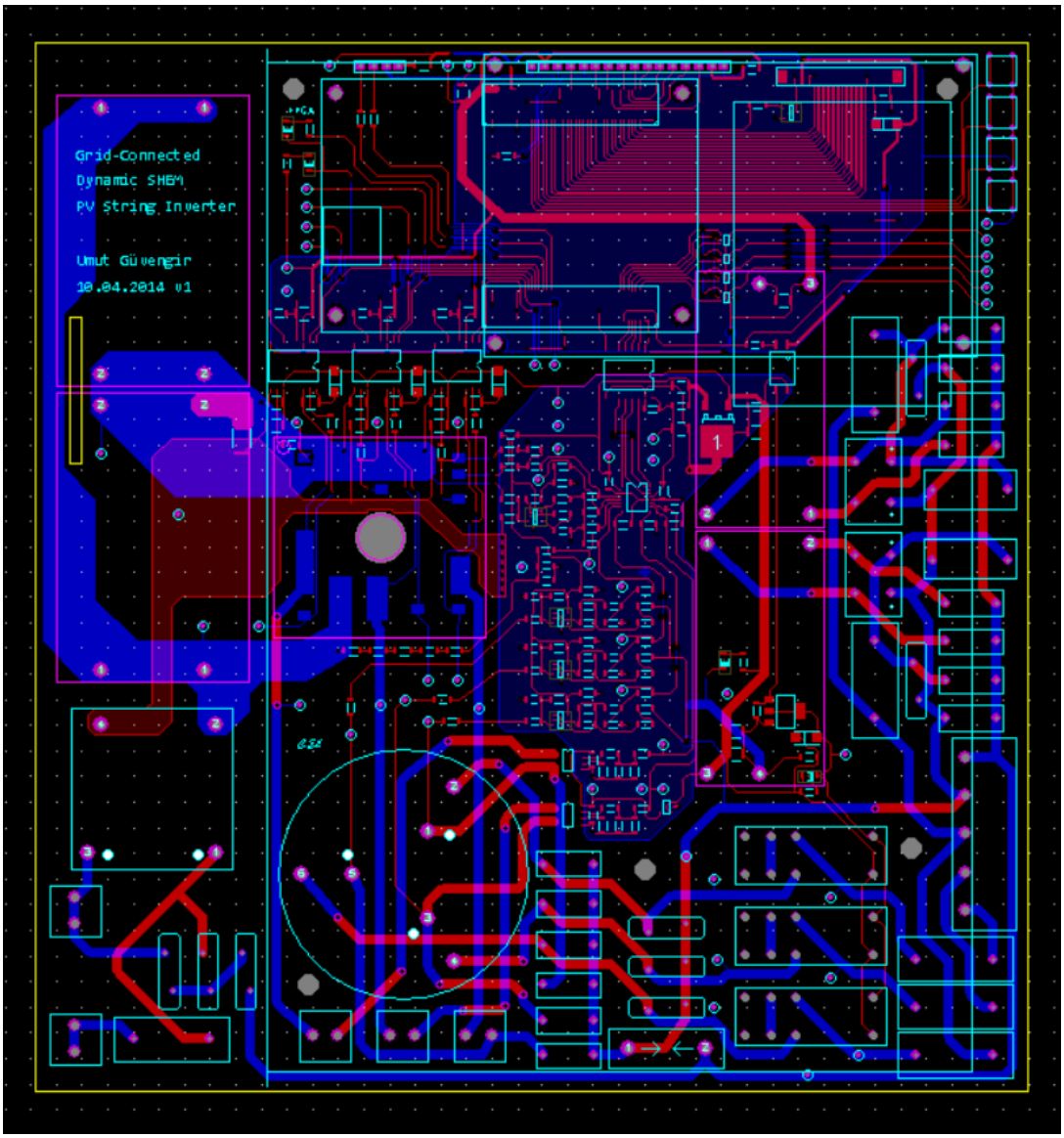

Figure A.8: PCB Layout Drawn in ARES Platform

APPENDIX B

LABORATORY EQUIPMENT USED FOR TESTS

- Chroma 62150H-1000S Programmable DC Power Supply with Solar Array Simulation
- Fluke 289 True-RMS Industrial Logging Multimeter
- Instek GPR-16H50D Power Supply
- PMK PHV1000 High Voltage Passive Probe
- RayTek ThermoView Ti30 High-Performance Thermal Imager
- Siemens SENTRON PAC4200 Power Monitoring Device
- Textronix A622 AC/DC Current Probe
- Textronix P2220 Voltage Probe
- Textronix P5050 Voltage Probe
- Textronix TPS2014 Digital Storage Oscilloscope
- Varsan Three-Phase Variac