A VERSATILE 5th ORDER SIGMA-DELTA MODULATION CIRCUIT FOR MEMS CAPACITIVE ACCELEROMETER CHARACTERIZATION

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ABSTRACT

A VERSATILE 5th ORDER SIGMA-DELTA MODULATION CIRCUIT FOR MEMS CAPACITIVE ACCELEROMETER CHARACTERIZATION

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With the significant developments in capacitive MEMS inertial sensors, tons of studies in the literature trying to enhance the performance parameters of MEMS capacitive accelerometer systems such as linearity, noise floor and bandwidth further has emerged. However, all the studies are conducted on a certain reference point, which is mainly the properties of the accelerometer sensor that alter a lot in the design of the high performance interface readout circuit. The designed interface circuits usually adopt high dependence on the accelerometer parameters and little variations on the accelerometer sensor due to fabrication impurities may result in the stability collapse of the whole system. Even though the advanced fabrication procedures allow the fabrication of the accelerometers with negligible tolerance and high yield, a precisely characterization extracted

circuit is required to qualify the fabricated accelerometer sensor. Such a circuit can propose data readout from capacitive accelerometer of a wide range and high tolerance.

This thesis presents the design of a highly coherent accelerometer characterization circuit. The major duty of front end compatibility to variety of sensor with no need to be redesigned is sustained by the use of simple voltage-mode approach. A mixed-signal loop consisting of 2 analog and 3 programmable digital filters is constructed for ΣΔ modulation. PDM voltage output is supplied back to the accelerometer electrodes to end up with closed-loop circuit, increasing the linearity, bandwidth and range of the system in a great sense. The proposed system is simulated in MATLAB Simulink Environment with two different sensors. The system is found out to have 35 μg/√Hz noise floor, nearly quarter of which is caused by the accelerometer.

Keywords: MEMS accelerometers, versatile front-end, electromechanical feedback, capacitance sensing, sigma-delta modulator.

ÖZ

KAPASİTİF MEMS İVMEÖLÇER KARAKTERİZASYONU İÇİN ÇOK YÖNLÜ 5 DERECELİ SIGMA-DELTA MODÜLASYON DEVRESİ

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Kapasitif MEMS ataletsel algıyacıların gelişimiyle, kapasitif MEMS ivmeölçer sistemlerinin çizgisellik, gürültü taban ve bant genişlik gibi performans parametrelerinin daha da arttırılması için literatür de tonlarca araştırma çıkmıştır. Yalnızca yapılan araştırmalar tek referans noktası olan ve yüksek performanslı algılayıcı devrelerin tasarımını çok değiştiren sensör özellikleridir. Tasarlanan geçirici devreler ivmeölçer parametrelerine yüksek bağımlılık gösterir ve ivmeölçer parametrelerindeki ufak değişiklikler bile sistemin stabilite temelli çöküşüne sebep olabilir. Gelişmiş üretim tekniklerinin az tolerans ve yüksek verimlilikle ivmeölçer üretimi sağlamasına rağmen üretilmiş aygılayıcıların kalifiye edilmesi için detaylıca karakterize edilmiş devrelere ihtiyaç vardır. Bu tür

devreler geniş yelpazede ve yüksek toleransta ivmeölçerlerden bilgi aktarılmasını sağlayabilir.

Bu tez çok uyumlu ivmeölçer karakterizasyon devresi önermektedir. Temel görev olan değişik aygılayıcılarla tekrar tasarım aşaması gerektirmeden uyum sağlama basit voltaj-okuma yöntemi ile yapılmaktadır. ΣΔ modülasyonu elde edilmesi için 2 seviyeli analog ve 3 seviyeli sayısal filtrelerden oluşan karışık sinyalli döngü kurulmuştur. Nabız yoğunluk modülasyonlu voltaj çıkışı kapalı döngü oluşturmak için tekrardan ivmeölçere beslenerek, sistemin çizgiselliği, bant genişliği ve çalışma aralığı büyük ölçüde geliştirilmiştir. Önerilen sistem MATLAB Simulink ortamında simule edilmiş ve gürültü tabanı 35 μg/√Hz olarak bulunmuştur.

Anahtar kelimeler: MEMS ivmeölçerler, uyumlu ön-cephe, elektro-mekanik geri besleme, kapasitans algılama, sigma-delta modülatör.

To my father, Dr. Bəxşeyiş Əsgərov

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CHAPTER 1

INTRODUCTION

From the beginning of the humankind history till the modern age, the major measurement of reference that had always evolved has been the speed. For illustration, even the data streaming rate that we were adopting as fast 10 years ago, would now push the patience limits of most people. This evolution in technology has been initiated with the revolution of shrinking the size of the electronic components. While number of components fitted to a certain area was increased, the number of functions to be conducted grew accordingly leading to a speed boost. A device that promises to exceed the limit and increase the number of functions from several to all needed is forecasted to be Micro-Electro Mechanical Sensors (MEMS).

As the name itself narrates, MEMS are micro-sized transducers and systems mainly manipulating mechanical elements and electrical signals from the corresponding components in an application specific manner. MEMS technology utilizes advanced micro-fabrication techniques and processes for the fabrication of devices with the sizes ranging from sub micrometers to several millimeters, which may include several systems at once. The miniature size enables mass production in a single run, decreasing fabrication per system cost enormously.

The evolution procedure from the micromachining to manipulating matter at atomic scale has been initiated by the electronic circuit industry back in 1950s'.

The goal back then of fabricating smaller devices for small cost still remains with further improvements of making the devices with lower power consumption and greater strength, which in term describes all the main advantages that the MEMS technology has gained over the classical methods. Such a development has offered unique opportunities in material design particularly in biological interfaces.

Counting down the advantages with the imposed tenders merely reflects the diversity of applications and the market development this technology has been through. Figure 1.1 shows the level that the MEMS devices has penetrated to civilian programs with the applications fields and forecasted market distribution in next 5 years [1].

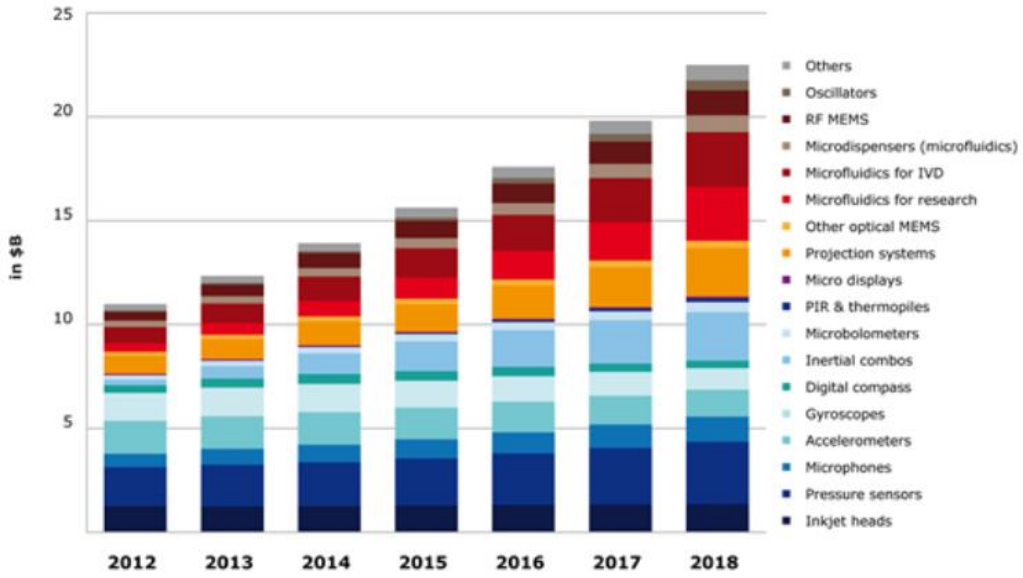


Figure 1.1: Application fields and forecasted market distribution of MEMS [1].

As the ancestor of the MEMS fabrication, the micro electronic industry kept up the pace in development. The increased properties in the transducers tailored the requirements of the electronic interfaces in a high degree. For example, the readout circuits of MEMS inertial sensors have independently passed a whole duration of enhancement to top the inertial and navigation grade requirements for

MEMS IMU systems. The boost in the electronic circuit designs resulting in a high performance interfaces has led to an era where the total system performance was limited with mechanical elements.

Through the enhancement continuum of the readout electronics, the certain reference frame on which the optimization of the electronics components was conducted is the mechanical properties of the IMU inertial sensors. While proceeding towards a high performance interface, the sensors parameter tolerances are shrinking. Even though it is the expected trade-off in developing technologies, batch micromachining factories or wide-range interest institutes would love to work with a single readout that can be used to characterize nearly all the capacitive fabrication. Therefore, easy readout electronics applicable to wide range of sensors is a hot topic nowadays, and corresponding goal was adopted in this thesis work.

1.1 Assortment of Accelerometers

In a world where the reference speed changes unimaginably on every aspect frame, the measurement of this change rate, namely acceleration is a very honorable duty fulfilled by accelerometers. Figure 1.2 shows the possible aspect frames and the required major properties accordingly [2].

MEMS accelerometer gained much interest due to its recent developments and is one of the top 4 shareholders in the MEMS market. Their ease of use, low-cost and small size makes them favorite in the run with their counterparts.

MEMS accelerometers are generally used to convert the physical dislocation of the suspended proof mass, which depends on the implied acceleration to another physical domain to be interfaced with the electronic circuit. Therefore, the two alterable constraints, namely the converted domain and the interface circuit can be used to categorize the accelerometers accordingly.

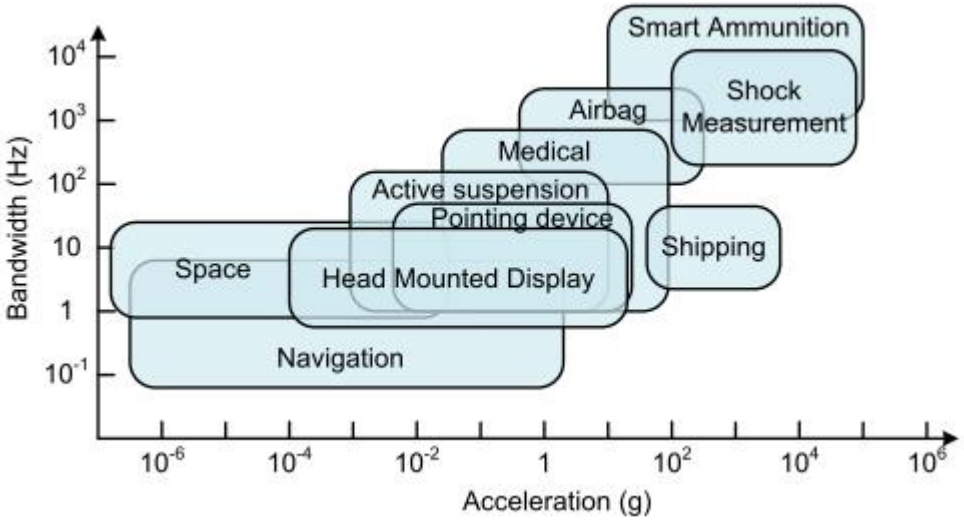


Figure 1.2: Application oriented accelerometer characterization [2].

1.1.1 Assortment by Conversion

As earlier described, several methods can be used to transfer the acceleration deduction from the displacement to sensing domain. The possible conversions to sensing domain, in term characterize the MEMS accelerometer type [3]:

1) Piezoresistive
2) Capacitive
3) Tunneling
4) Resonant
5) Thermal
6) Optical
7) Electromagnetic
8) Piezoelectric

Known as the first micromachined and commercialized accelerometer, piezoresistive operate on the basic principle of resistance change [4-5]. When the external acceleration is applied to piezoresistive accelerometer, the dislocation of the proof mass in reference to the support frame leads to the change in the length

of suspension beams, which by changing its stress profile directly affects the resistance embedded. The change in the resistance can be scanned by simple resistive bridge, and thus the acceleration change can be computed thereby. Even though simple fabrication process and easily applicable electronics make them shine with their simplicity, highly temperature dependence and low sensitivity repels them for industrial applications.

Keeping the line, piezoelectric material can be used to fabricate device where the imposed force would result in an accumulated electrical charge. The induced charge can be directly coupled to a transistor to be read out as acceleration [6]. Piezoelectric accelerometer's high bandwidth and good resolution enable their utilization in shock measurements.

Electromagnetic accelerometer, as the name itself depicts require the placement of magnetic coils on the proof mass and supporting frame separated by a certain air gap. While the external acceleration is applied, due to the distance change between the still coils the mutual inductance would be altered. A simple circuit can be utilized to compute the acceleration [7].

Optical accelerometers combine the properties of optics and MEMS in a single device to provide higher sensitivity and better reliability. The utilization of the optical power instead of electrical, exploits electromagnetic interference immunity [8]. However, the fabrication of such devices is still challenging and hard-integration nature limits their applications.

Another method that has been used to depict acceleration from the external applied force is beam resonant frequency shifting. Called as resonant accelerometers, the devices rely on the shift of the beam resonant frequencies caused by the inertial force to axial force transfer [9]. Special techniques like differential resonance matching can be used to suppress thermal mismatches and nonlinearities to achieve high resolution and very good stability [10-11]. Even though, the small bandwidth of such devices limits their application highly.

One of the inputs of the nature, namely temperature is another measure for acceleration. The inverse proportionality of the temperature flux to the distance between the heat source and the heat-sink can compute a measure for acceleration, the force that alters the described [12]. The placement of two temperature sensor and deduction thereby can give sub-μg performances [13].

Tunneling accelerometer use the tunneling current forced between the top and bottom electrodes to compute the acceleration. In the existence of the inertial force, the approaching moving electrode establishes a small current in a short distance. The induced current can be used in a closed loop to counteract the movement by applying the desired voltage to the electrodes, improving the range of the system. Externally applied voltage can easily be used to measure the acceleration [14].

Last but not the least; capacitive transduction is another approach in MEMS accelerometers for proof mass deflection measurement. Known as the most widely used method, capacitive transduction relies on the change in the capacitance embedded between the proof mass and the support frame. The existence of external acceleration forces the proof mass to dislocate, altering the gap between the two capacitance sensing electrodes. Their simple structure and numerous advantages associated with noise performance and low frequency response enable their application in large-volume automotive market [15] and inertial-grade navigation [16].

1.1.2 Assortment by Interface

With the transfer in physical domain, the converted data has to be transferred into electrical domain to be processed and computed thereby. Several methods can be used to electrically deduce the acceleration from the displacement of the mechanical element inside the accelerometer:

1.1.2.1 Open Loop

In open loop operation, the raw physical variation data acquired from the accelerometer is processed and the respective data is outputted by the readout circuitry. These types of interfaces measure the absolute change due to acceleration and lack a feedback loop, yielding a simple design. However, operating the accelerometer package in open loop introduces some serious obstacles, namely linearity and operation range. The function between the input acceleration and the electronic output is highly nonlinear. Furthermore, due to pull-in voltage concept in the MEMS systems, the capacitance variation among the electrodes to be processed is finite, limiting the operation range of the accelerometer system.

1.1.2.2 Closed loop

Inclusion of some modification into the readout circuit guides the conduction of closed loop operation. The conduction of the electromechanical feedback neutralizes the motional fluctuations of the proof mass inside the accelerometer, which significantly increases the operation range of the system. Moreover, as the movement is counteracted in closed loop operation, the effect of the nonlinear function is largely suppressed and the linearity improves considerably [17]. It is also worth to note that for having a reliable closed loop operation the open loop gain of the system should be high enough. A strongly closed loop would in turn lead the overall system to be independent of the small variations in the open loop. The conventional improvements in closed loop operation are true; however, system cannot be fully utilized because of the non-linearity between the mechanical feedback force and the electrical feedback voltage [18]. Furthermore, introduction of closed loop to the accelerometer draws noteworthy stability issues. The reinforcement of the closed loop for having a high noise performance puts the circuit into stability criteria, illustrating the trade-off between the noise and the stability [19]. It is important that with the variations in the sensor

parameters due to the changes in the surrounding environment the system would not sacrifice from the stability margin or performance value. If not, the system becomes highly dependent on the fabrication parameters, as the results of which the system lacks robustness. Accordingly, to avoid these types of consequences several readout architecture including ADC, PID utilization and sigma-delta modulation are being reported in the literature [20-26].

1.2 Overview of Capacitive MEMS Accelerometer Readout Circuits

Readout intended electronic circuit design for capacitive MEMS accelerometers has always been a state-of-art issue. As described, topologies with different approaches have been proposed to extract data in high performance. The main trend has shifted to designing closed-loop circuit for future-intended applications.

1.2.1 Digital Feedback Circuits in Literature

The implementation of digital feedback containing loops evolved in response to the lack of stability in closed-loop readouts. Firstly, *Boser et al.* have proposed fourth-order sigma-delta interface architecture with a very high performance. The electronic filter implemented after the mechanical sensor acts like a noise shaper and overall system rejects the in-band quantization noise efficiently. Figure 1.3 shows the total system designed, where the electronic filter parameters were altered by tuning the constant factors on the loop. Interface also promises good linearity, however, stability plays the role of limiting factor. The system truly illustrates the trade-off between the noise performance and the stability [20].

Keeping the line, *Raman et al.* have reported an unconstrained architecture with a proportional based controller. In this architecture for systematic design of high order sigma-delta force-feedback loops two degree of freedom is introduced and stability can be designed independent of the performance. Flexible design and analysis is a strong point, but the system lacks reinforced open loop gain. Once

calibrated with initial sensor parameters, high performance noise data can be acquired. However, with the variations in sensor parameters due to the change in the environment the same results can no longer be observed. As the architecture is sensitive to the tolerances in sensor parameters, it cannot be called as a robust design [21].

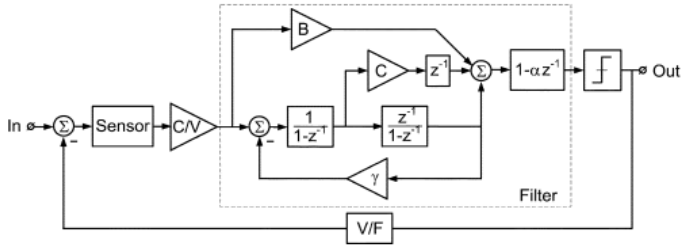


Figure 1.3: Fourth-order electromechanical sigma-delta loop [20].

For extended linearity, dynamic range and bandwidth *Land et al.* have proposed a digital PID-type controller for accelerometers. The analog data by the utilization of flash A/C is converter into digital environment, where it gets processed by an integral based controller. In this design, the conduction of the control in digital environment induces serious mismatches and noise, because of separate A/D (flash ADC) & D/A conversions. Moreover, the design cannot be analytical solved or designed with the well-known procedures [22].

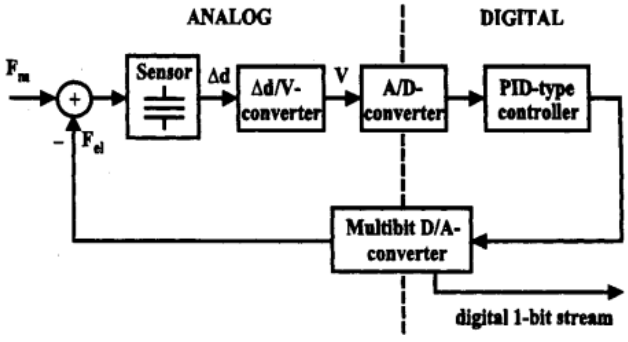


Figure 1.4: Electromechanical closed loop with PID control [22].

1.2.1.1 Fifth-order ΣΔ Modulation

The evolution of sigma delta modulator has run in parallel with the wireless telecommunication systems, as primary role in speed boost is played by such modulators. These key devices supply the systems with high efficiency, wide bandwidth and application specific adjustment features. Several features of described modulators, such as order augmentation became the priority components in fast data rate for wireless telecommunication applications. Furthermore, the application in modern mobile technology required another key feature of low power consumption, a goal set to be satisfied.

A study was carried by *Matsukawa et al.* on conventional continuous-time sigma-delta analog-to-digital converters for lowering the power consumption. They have implemented their phenomenon of fifth-order, 3-bit and single feedback ΣΔ ADC on 110 nm CMOS process. The achievements of the proposed circuit are supplied by single-opamp resonator, ringing-relaxation filter and passive resistor adder. Figure 1.5 shows the block diagrams of conventional ΣΔ ADC and the proposed structure, respectively.

To demonstrate the advantages brought by the designers, the pros of every step must be considered. Firstly, the designers have replaced the resonators in the conventional sigma-delta loop with so called “versatile single-opamp resonator”. Such an improvement reduces the number of opamps implemented in high-order circuits, greatly reducing the power consumption and the phase delay. Furthermore, another unique point about the single-opamp resonator is that it can realize a perfect transfer function lacking first order Laplace term, alterable second-order transfer function of the numerator and calibration easy structure with the use of independent resistor values.

The other two innovations proposed are ringing-relaxation filter and passive resistor adder, enabling the reduction of gain bandwidth product of the very first

opamp for suppressing the interference caused by feedback DAC and signal addition with negligible power consumption, respectively [23].

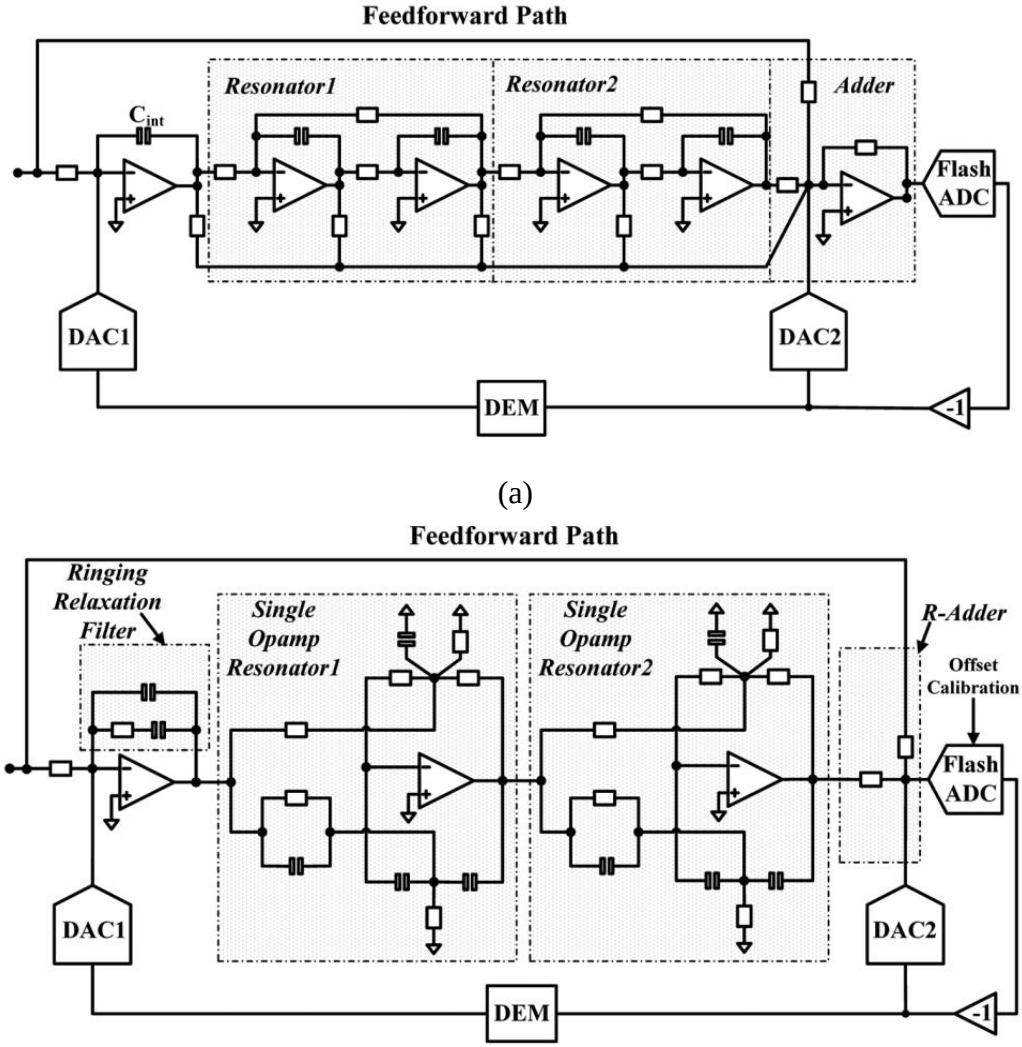


Figure 1.5: Block diagram of (a) conventional 5th order CT ΣΔ ADC, (b) proposed 5th order CT ΣΔ ADC [23]

The proposed loop was fabricated in 110 nm CMOS process corresponding to 0.32 mm^2 chip area. With 10 MHz input signal bandwidth and application of 1.1 V, 68.2 dB SNR and 62.5 dB SNDR were presented as a result. Although the finites are sufficient for stabilizing the modulator and limiting the power consumption (FoM = 0.24pJ/conv.), the system has serious concerns in terms of

harmonic distortion suppression. In relation to the concerns, the system cannot acquire high resolution measurement. Successful application of the topic can be related to the systems with low oversampling ratio only.

Another development on high-order sigma-delta converters, serving the same goal of broadband wireless telecommunication was accomplished by *Lu et al.* They have proposed a continuous-time low-pass sigma-delta modulator including seven-phase clocking scheme. The ultimate purpose of boosting the SNDR of the circuit, claimed by most wireless technology developers is conducted by the use of multi-bit quantization, consequently multi-bit feedback DAC. This method attracts attention because when utilized SNDR improvement can be achieved over wide bandwidth without increasing the sampling frequency. Figure 1.6 shows the system architecture of the mentioned ΣΔ modulator circuit [24].

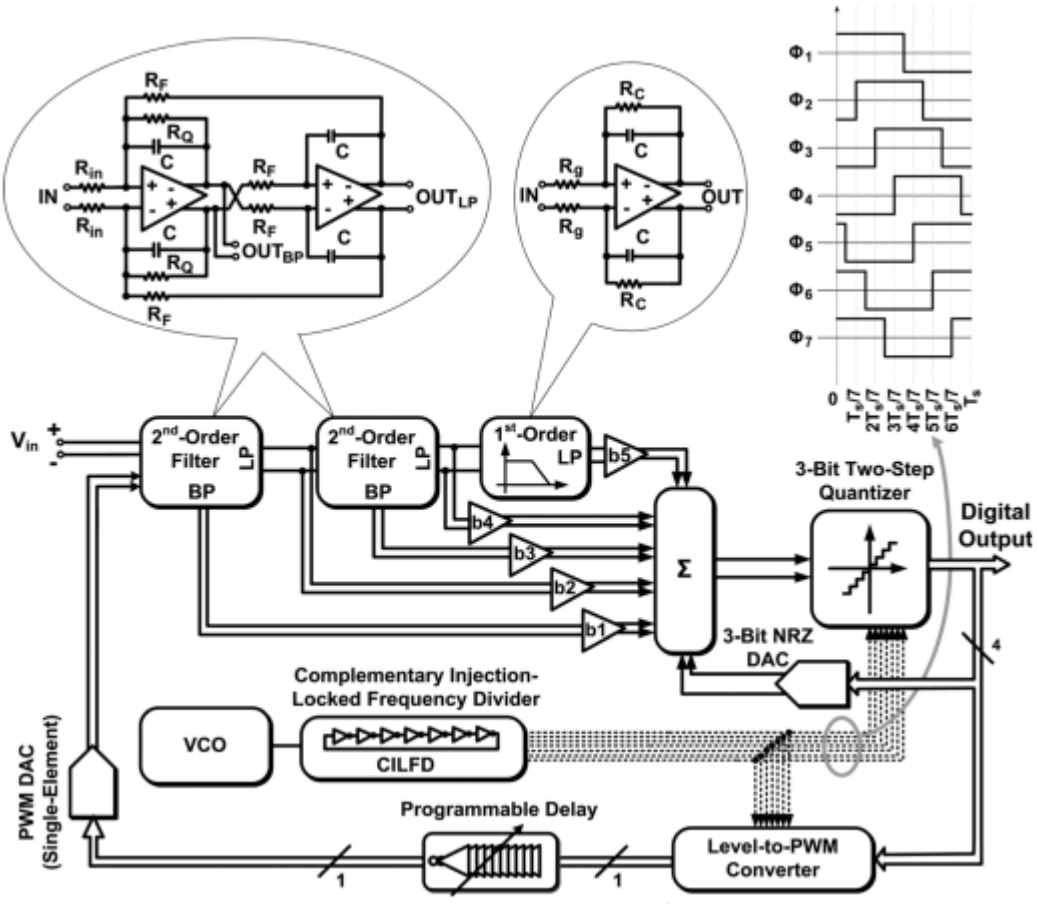


Figure 1.6: System architecture of the proposed 5th order CT modulator [24].

In pursuing an effective design, the author's main goal was to prevent DAC element matching issues altogether by using a multi-bit single-element DAC. Accordingly, the circuit includes a 3-bit quantizer and a single-element DAC that actualizes 3-bit feedback via time-based operation. In this sense, an on-chip voltage controlled oscillator and a complementary injection-locked frequency divider were employed for low-jitter clock generation, for procurement of precise timing signals and clock jitter to attain high SNDR.

For real life illustration and assessment of the circuit, the modulator fabricated in a standard 0.18 μm CMOS process with a die size of 2.6mm^2 was fetched into a test setup with 25 MHz bandwidth and 1.8 V supply. Nonlinearities from the element mismatch were successfully suppressed and a peak SNDR of 67.7 dB was observed. However, the drawback of the design can be directly observed as the power consumption. The power consumption of the circuit is 48mW, 56% of which is dissipated in the modulator block. In accordance with its bandwidth the FoM can be calculated as 484 fJ/bit, which is two times larger than [23]. Technology scaling in time can enhance the power efficiency of the design though. Furthermore, technology scaling can also cure the necessity for accurate digital timing circuitry. Overall, it is promising way with complex and power consuming design, expected to be an applicative product with development of technology scaling [24].

The alternative advantage of modulation realization through precision lacking components suits the sigma-delta converters at the cost effective converter mission for audio application. Choice of a five order modulator with good linearity discrete components can supply the minimum requirements for 20 bit dynamic range with 64 oversampling ratio, such that was designed by *Ritoniemi et al*. They have designed a sigma-delta modulation loop with extricable/addible integrators. The addition or removal of integrators is conducted through switch capacitors for stabilization of high-order sigma-delta loop. The whole system is made to be a stable high-order modulator with limited input range. Figure 1.7 shows the block diagram of the described loop [25].

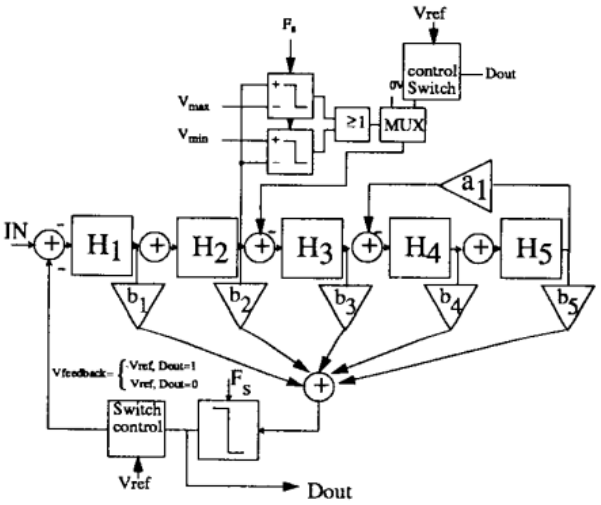


Figure 1.7: Block diagram of the fifth order sigma-delta modulator [25].

The unstable operation in the loop is suppressed by initial detection at the output of the second integrator. With the excision of the voltage above the allowed range, an additional feedback is added to the input of the third integrator. The feedbacks are organized so that the integrator voltages are always limited to the allowed range for stable operation [25]. Even though a stable operation is preserved, the system has several drawbacks in terms of noise, chip area complexity. With every alteration in the circuit, the gain of the resultant integrators should be calibrated accordingly, forbidding a settled operation. Also use of excessive capacitor increase the kT/C noise together with the chip area.

Last but not the least, the fifth order architectures are also utilized in sensor interfaces similar to the prospect of this thesis. A closed-loop mixed signal architecture aiming to achieve technical parameters required for tactical grade was proposed by *Dong et al.* The designed circuit is an ultra-high precision fifth-order sigma-delta loop, whereas the five time integration of the signal is divided between the analog and digital parts respectively as two and three. The major aim of the designers was to decrease the dependence of the loop of manufacturing errors and to optimize the accelerometer in terms of several parameters. Figure 1.8 shows the system architecture proposed [26].

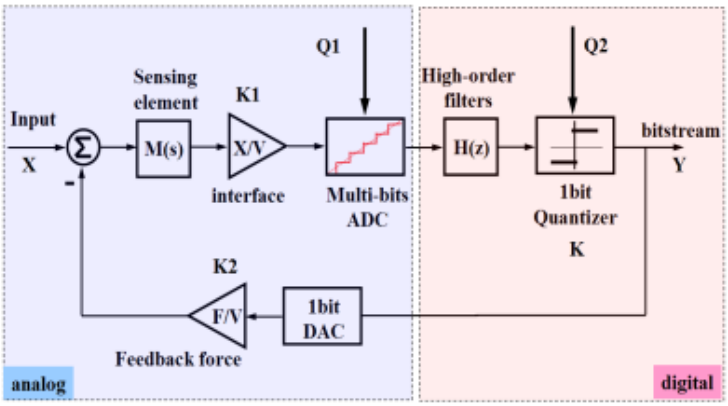


Figure 1.8: System architecture of 5th order closed-loop proposed by [26].

Utilization of the accelerometer as an analog integrator in the loop yields the system as an electro-mechanical sigma-delta modulator, which is discussed in chapter 3. Nevertheless, to give an insight the circuit converts the analog data to digital environment for controlled processing and fetches back the signal for electro-mechanical feedback. The proposed system is very similar to the one in the thesis work; however, it was fabricated by CMOS process. Designated fabrication lacks the vision of batch testing and concentrates more on long-term stability by use of high-performance mechanical devices. The results obtained by the group are charming, and enable utilization of MEMS accelerometer is tactical missions. With the full range input of 15 g and bandwidth of 300 Hz, the noise level observed was as 1.7 $\mu g/\sqrt{Hz}$ with 100 mW power consumption. Such an architectural structure is widely proposed in the literature [36-39].

1.2.2 ΣΔ Modulation Circuits in METU

Capacitive MEMS accelerometer interface design has always been a major interest for METU-MEMS Research Group. While chronologically analyzing, the second-order sigma-delta readout designed by Reha Kepenek is observed as the first manuscript, a M.Sc. thesis that started it all. Figure 1.5 shows the block diagram of the system proposed by Reha.

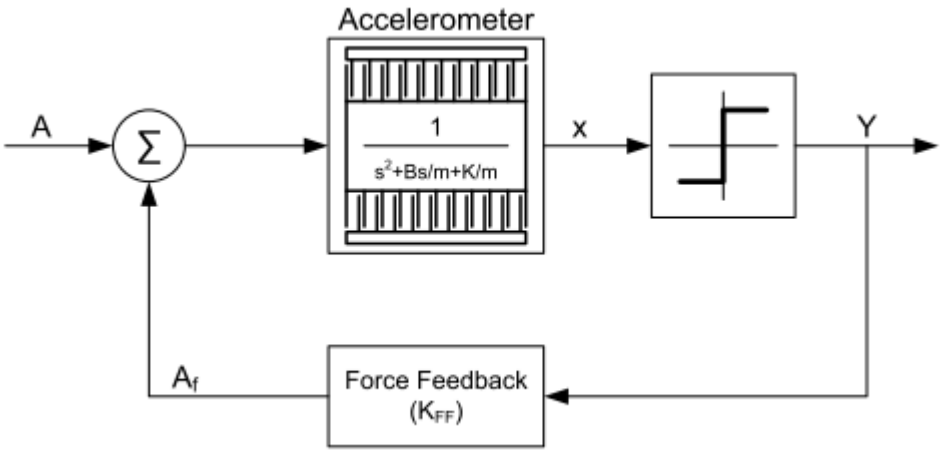


Figure 1.9: Block diagram of 2nd order sigma-delta loop [2].

In the system proposed, the second-order low pass characteristic of the MEMS accelerometer is employed as consecutive noise shaper. Applying the output signal of the accelerometer to a quantizer yields a pulse-density modulated signal, directly related to the input signal in second order and further fed back to the accelerometer for counteracting the dislocation of the proof mass. Keeping the proof mass in the null position and applying digital electromechanical feedback provides the system with enlarged range and enhanced linearity.

Using the sigma-delta readout circuit for the closed loop, low noise test results were observed. The readout mashed with the MEMS accelerometer performed at an operational range of around ±18.5 g on tests, in which the promised high linearity was verified. The noise floor of the total system was measured to be 86 μg/√Hz and a bias drift of 74 μg was sustained [2].

The research was further enhanced, and Ugur Sonmez implemented a modified sigma-delta loop. In his M.Sc. thesis Ugur presents a fourth-order unconstrained topology as electromechanical closed loop to improve the accelerometer system in aim of navigation grade applications. Figure 1.6 shows the topology presented by Ugur Sonmez.

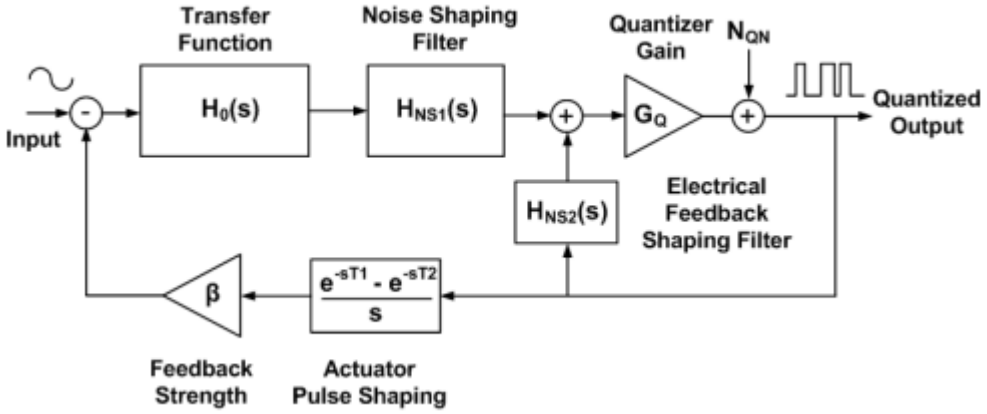


Figure 1.10: Block diagram of 4th order unconstrained sigma-delta loop [27].

In the system proposed, an additional second order electronic filter was employed in series with the second-order low pass characteristic of the MEMS accelerometer to end up with fourth order electromechanical loop. The duty of noise shaping was shifted from the mechanical element inside the loop to the electronic circuit, which can be implemented with more ease. The system shows an exceptional performance and knocks on the doors of navigation grade.

Tested together with the MEMS capacitive accelerometer fabricated in METU-MEMS facilities, 5.95 μg/√Hz, 6.4 μg bias drift, 131.7 dB dynamic range and up to ± 37.2 g full scale range were observed as performance parameters. The positive effect of the increasing the order of the loop in a controlled manner can be obviously seen as the research report 25 fold improvement [27].

Following the trend, Osman Samet Incedere took the competition to the further edge of designing the similar system with much less power consumption. He has also included a PI controller in his loop to increase the open loop gain and ensure the stability of the total system. Figure 1.7 shows the block diagram of the low power, high performance sigma-delta loop.

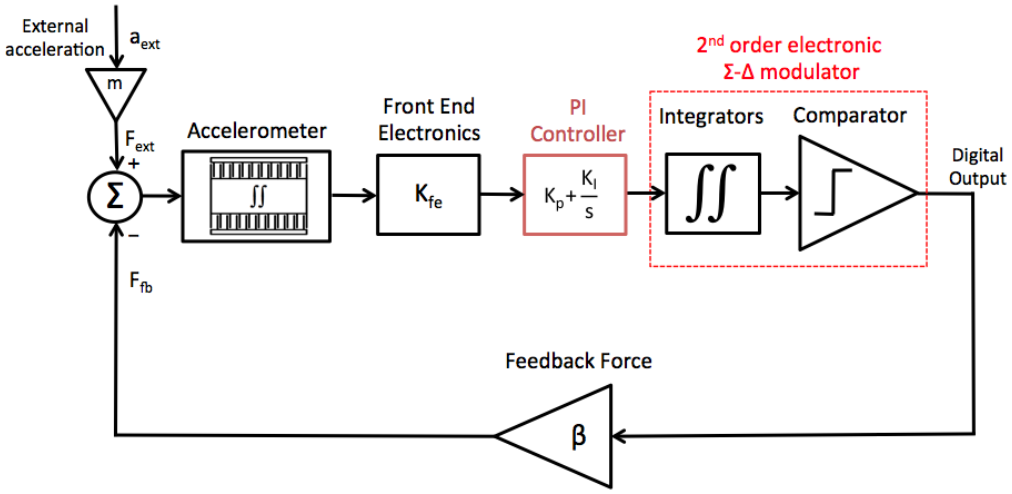


Figure 1.7: Block diagram of analog PI included 4th order sigma-delta loop [28].

As a part of the research, a PI controller was included in the loop to serve guarantee the stability. PI controller increases the open loop gain of the system, which in term decreases the fluctuation in the proof mass location, resulting in a better linearized output. The designed system is highly controllable through the digital blocks inside the ASIC, which makes its application possible for several purposes. It is noteworthy that the system designed dissipates less than 2 mW to yield performance parameters like 5.3 μg/√Hz noise floor, ± 19.5 g full scale range and 128.5 dB dynamic range. For the simulative convergence of the listed results, a mechanical sensor with $3.5x10^{-6}$ F/m sensitivity, 9.5 pF rest capacitance, 2.32 kHz resonant frequency and 4.6 μg/√Hz Brownian noise was employed [28].

1.3 Objectives and Outline of the Thesis

The designed interface circuits usually adopt high dependence on the inertial sensor parameters and little variations on the sensor due to fabrication impurities may result in the stability collapse of the whole system. Even though the advanced fabrication procedures allow the fabrication of the MEMS inertial

sensors with negligible tolerance and high yield, a precisely characterization extracted circuit is required to qualify the fabricated sensor. Such a circuit can propose data readout from sensors, such as capacitive accelerometer of a wide range and high tolerance. Therefore, the design of stable multipurpose readout electronics to be utilized by large-scale MEMS fabricators for capacitive accelerometer characterization was adopted as the goal during this research. For the successful fulfillment of the goal, several features were assigned as checkpoints in reference to the top level:

1. The main objective of this work is to design a readout that can be interfaced with various accelerometers, independent of their mechanical properties and still high resolutions should be achieved. The readout should be fetched without the need to be redesigned with wide range of sensors (sub-g to 100g) with high linearity and good noise performance.
2. Circuitry content of the loop should be chosen from discrete components, without any need for CMOS fabrication.
3. The open loop gain of the loop should be chosen with care in order to match stability condition in high-order sigma delta electromechanical loops.
4. Total loop order should be increase further than four, to observe the advantages that quantization noise improvement presents in terms of resolution.
5. A simple transduction approach should be chosen to be interfaced with different mechanical characteristics. Furthermore, the system should be well understood on theory for integrated test analysis.

The thesis consists of 4 chapters. After brief information about MEMS, overview of the work done till completion of this thesis is given in Chapter 1. Objectives and outline of the thesis conclude the first chapter.

Chapter 2 includes detailed information about the crucial components in the loop. Several details corresponding to sigma-delta converters are described. The

specific application of ΣΔ converters, namely electromechanical feedback details are presented afterwards. In this chapter, some information about the utilized MEMS capacitive accelerometer is also presented.

Chapter 3 gives the specific work proposed in the scope of the thesis. The specific application of ΣΔ converters, namely electromechanical ΣΔ modulation details are presented firstly. The proposed structure is in detail analyzed at low-level. The MATLAB model and corresponding simulations endorsing the proposed theory are presented together with the electronic circuit to be tested.

Chapter 4 illustrates the work shown for the intake of test results. Divided into two parts called open-loop and closed-loop, the chapter includes the setups and packages prepared together with the test results. At the end of every section, comments are included for clear understanding. The third section of the chapter includes general discussion about the applicability of the loop.

Finally, Chapter 5 summarizes the works done in the scope of this thesis, providing information about the feasibility of the approach and suggesting a possible future work.

CHAPTER 2

THEORETICAL BACKGROUND OF THE LOOP

This chapter presents the principles of crucial components in the sigma-delta loop. Section 2.1 exploits the equations of the accelerometer for the successful transaction of the research. The extraction of the transfer function for the accelerometer is conducted, while the utilized mechanical parameters are given at the end of the section. Up next, Section 2.2 presents the basic understanding of sigma-delta converters together with the related concepts such as noise shaping, oversampling and demodulation. Related adaptation of sigma-delta converter, namely electromechanical sigma-delta loop is further discussed with order isolation.

2.1 Capacitive MEMS Accelerometer

The first component content that we face in the loop is the capacitive MEMS accelerometer. The capacitive MEMS accelerometer designed in METU-MEMS research group and employed as the mechanical sensing element in the scope of this research, is lateral-comb like structure with a suspended proof-mass reacting to the external acceleration [29]. In response to the inserted force to the structure, the proof mass deflects a certain distance from its null position depending on the parameters like its own mass, spring constant, damping coefficient. Dislocation results in the change of well-defined gap between the comb-like micromachined structures that can be sensed as a capacitance change respectively. Figure 2.1

illustrates the mechanical sensor, in order words the accelerometer structure. For a clarified understanding, the simple model of the accelerometer is embedded inside the figure.

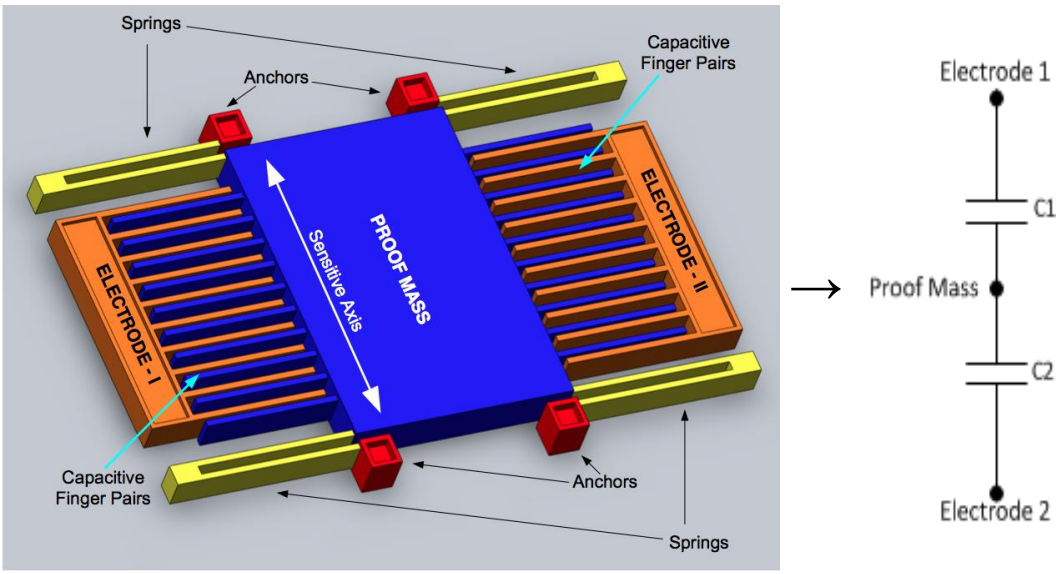


Figure 2.1: Capacitive MEMS accelerometer structure and its simplified view

The illustrated capacitance between the electrodes and the proof mass is employed by the capacitive finger pairs. Every single pair can be thought as a capacitor. Processing several finger pairs with their poles intersecting at the exact same node yields the capacitance that directly proportional to the number of the pairs. Moreover, further interaction of the pairs among themselves supplements total capacitance value and decreases the sensitivity, which will show later. To be formulated, the total capacitance is written as

$$C_{1,2} = \frac{N.\varepsilon_0.A}{d_1} + \frac{(N-1).\varepsilon_0.A}{d_2} \qquad (2.1)$$

In the equation, N is single-sided number of the finger, ε_0 is the permittivity of the air, A is the overlap area of a single finger pair, d_1 is the gap corresponding to the paired fingers and d_2, called as anti-gap, is the gap between the plates with further interaction as discussed above. For better understanding, Figure 2.2 shows

an illustration of the comb-like structure and dimensional parameters [2].

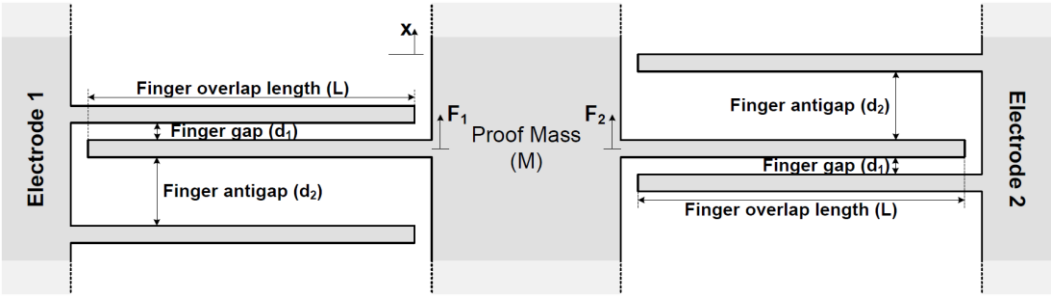


Figure 2.2: A zoomed view showing the dimensional parameters of the capacitive finger pairs inside capacitive MEMS accelerometer [2].

As a movement is forced on the proof mass by the existence of acceleration, the gap is thereby also forced to change. If the displacement of the proof mass from its null is taken as x, equation (2.1) can be upgraded to

$$C_{1,2} = \frac{N.\varepsilon_0.A}{d_1 \pm x} + \frac{(N-1).\varepsilon_0.A}{d_2 \mp x} \tag{2.2}$$

It is noteworthy that the accelerometer is transverse structural vise. Therefore, the capacitance values given in Equation 2.2 prior to Figure 2.1 operate in a differential logic, meaning that while one increase the other one decreases. This property will be further utilized for readout purposes.

Assuming that the displacement of the proof mass is small compared to the gap and anti-gap, the Taylor expansion can be applied to Equation 2.2 to extract displacement dependent and independent terms.

$$C_1 = \frac{N.\varepsilon_0.A}{d_1} + \frac{(N-1).\varepsilon_0.A}{d_2} + \left[\frac{N.\varepsilon_0.A}{{d_1}^2} - \frac{(N-1).\varepsilon_0.A}{{d_2}^2}\right]x \tag{2.3}$$

Further terms of the Taylor expansion are neglected. Note that assuming negligible dislocation is not a bad argument, because employment of electromechanical feedback with even second order system is quite enough to counteract the movement of the proof mass so that the displacement level is kept

unnoticeable. In Equation 2.3, the first term that is independent of acceleration is equal to Equation 2.1 and called rest capacitance. The second term in the equation is displacement dependent term and can be utilized to find the sensitivity of the accelerometer. By simply differentiating Equation 2.3, we find

$$\frac{\partial C_1}{\partial x} = \frac{N.\varepsilon_0.A}{{d_1}^2} - \frac{(N-1).\varepsilon_0.A}{{d_2}^2} \tag{2.4}$$

The absence of a displacement term shows that the capacitance is linear in the systems with proper feedback. Furthermore, Equation 2.4 illustrates the negative effect of the anti-gap to the sensitivity. Therefore, the anti-gap should be designed big enough to yield with a reasonable sensitivity.

Last but not the least; the sensitivity expression can be used to calculate electrostatic pulling force. It's an important parameter in the closed loop system and calculated by the use of applied voltage (V) and capacitive sensitivity. Making use simple equation

$$F_{FB} = \frac{1}{2}.\frac{\partial C}{\partial x}.V^2 \tag{2.5}$$

By simply inserting Equation 2.4 for sensitivity,

$$\begin{aligned} F_{FB} &= \frac{1}{2}.\left[\frac{N.\varepsilon_0.A}{{d_1}^2} - \frac{(N-1).\varepsilon_0.A}{{d_2}^2}\right].V^2 \\ &= \frac{\varepsilon_0.A.V^2}{2}.\left[\frac{N}{{d_1}^2} - \frac{(N-1)}{{d_2}^2}\right] \end{aligned} \tag{2.6}$$

With the calculation of the force feedback, the necessity for the position control can be interpreted by simple law of physics:

$$F = m.a_{ext} \tag{2.7}$$

As described in the earlier section, in the closed loop systems the actuation strength is used to find the disturbance in the position control, which can be further utilized to extract the acceleration

2.1.1 Transfer Function

For the proper modeling of the accelerometer system, a transfer function defining the mechanical element should be extracted. A proper model for the capacitive MEMS accelerometer is usual defined as mass-spring-damper. Figure 2.3 shows a simple mass-spring-damper system.

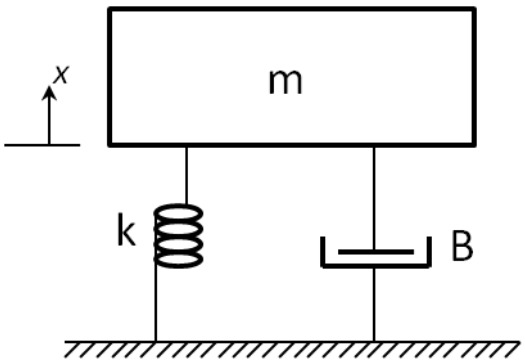


Figure 2.3: Simple mass-spring-damper structure.

Combining the equations of motion for the accelerometer and mass-spring-damper system,

$$F = m.a_{ext} = m.\ddot{x} + \beta.\dot{x} + K.x \tag{2.8}$$

In Equation 2.8, m is the mass of the suspended proof mass, x is the displacement, β is the damping coefficient and K is the spring constant. Applying Laplace transform and forming the equation for the transfer function of the accelerometer,

$$H(s) = \frac{1}{s^2 + \frac{\beta}{m}s + \frac{K}{m}} \tag{2.9}$$

Constructing an analogy for second order systems and Equation 2.9 results in a set of equations as,

$$\omega_0 = \sqrt{\frac{K}{m}} \tag{2.10}$$

$$Q = \frac{\sqrt{K.m}}{\beta} \tag{2.11}$$

Therefore, it can be concluded that the quality factor and the resonance frequency of the accelerometer which define the performance over the spectrum are highly dependent on the mechanical parameters of the sensor. Table 1 show the utilized accelerometer's mechanical parameters included in the scope of this thesis work.

Table 2.1: Mechanical properties of the accelerometers used in this research.

Design Parameters	**Sensor-1**	**Sensor-2**
Structural Thickness (μm)	35	35
Proof Mass (kg)	2.66 x 10^{-7}	1.27 x 10^{-7}
Spring Constant (N/m)	56.3	165
Damping Coefficient ($N.m/s$)	9.1	4.3
Resonance Frequency (Hz)	2495	-
Capacitive Gap (μm)	2	3
Capacitive Anti-Gap (μm)	7	10
Finger Length (μm)	155	230
Brownian noise ($\mu g/\sqrt{Hz}$)	6	6.6
Rest Capacitance (pF)	10.4	8

2.2 Sigma-Delta Modulation

Even though the discovery of Sigma-Delta modulation leans back to 70's [30], the widespread application came up to be fancy with the innovative developments in VLSI technology. Sigma-delta modulation supplies a unique property of high resolution digitalization for analog carriers with frequency much less than the sampling frequency. The logical conclusion can be carried that for applications

such as sensor interfaces, characterization systems and audio filtering where input low frequency signal is to be processed with high dynamic range and flexibility, ΣΔ converter would turn out to be the most cost effective modulation, providing up to 21 bit resolution [31]. Implementation of such a filtering inherently offers primary advantages such as linearity and robust operation. Furthermore, making of use the general trade-off between the accuracy and the speed, high performance can be achieved without the dependency to the analog component properties [32]. The described feature will be deeply utilized in the scope of the thesis. Figure 2.4 shows the basic block diagram of a first-order ΣΔ modulator.

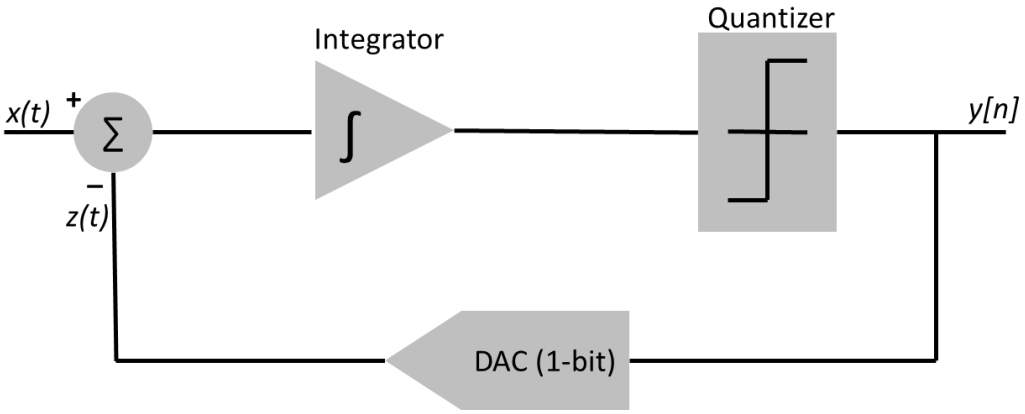


Figure 2.4: Simplified block diagram of a first-order ΣΔ modulator.

As illustrated, the loop consists of an integrator, a quantizer and a 1-bit digital to analog converter. The analog input, *x(t)* is initially feed to an integrator conducting the sigma operation, else to say the summation. This function enables the system to be independent of the rate of change in the input signal. The attained signal is afterwards feed to a quantizer, where an absolute value of 1 or -1 is produced as a digital output of *y[n]*. The output is thereafter converted to a analog signal of *z(t)* through a 1-bit DAC.

The nature of the feedback forces the average of *z(t)* signal to be equal to *x(t)*, forwarding the difference as an input to the integrator. The difference between these signals is called the quantization noise, and it will be further discussed in

coming section. Figure 2.5 shows a sample input-output graph for first-order ΣΔ modulator [33].

The input-output graph clearly illustrates that when the average mean of the input signal is above zero, the quantizer outputs positive signal more, and vice versa. Furthermore, it can also be seen that when the input signal is around zero, the output oscillates, going back and forth between the positive and negative maximum. To finalize, observing that output shows long durational positive digital signal at maximum of the analog input, and long durational negative digital signal at the minimum of the analog input seal the deal of understanding.

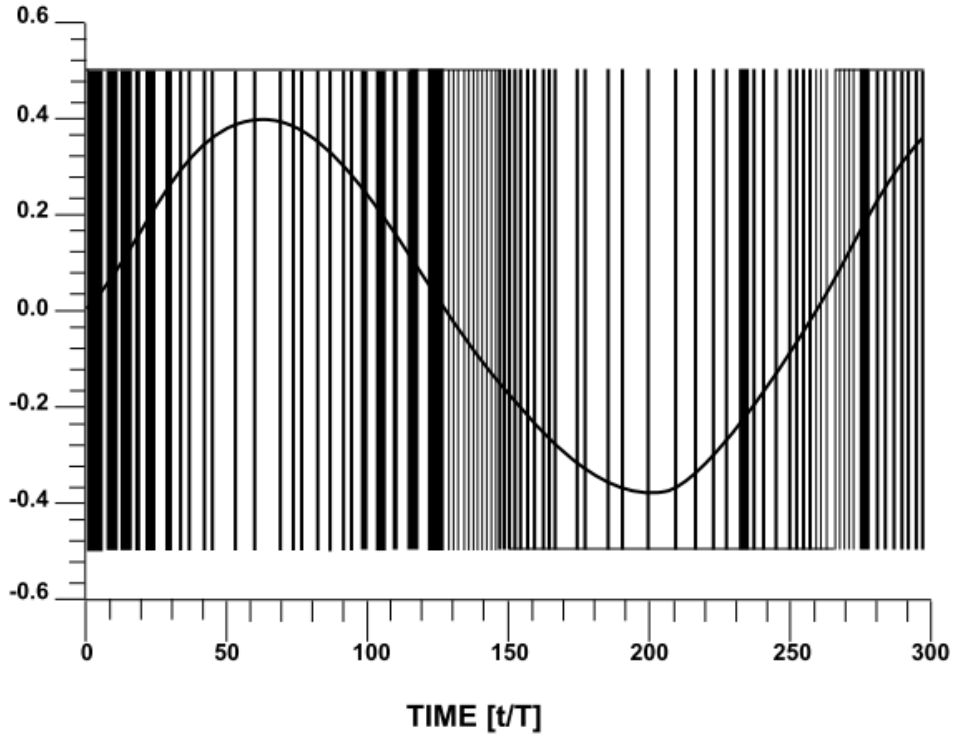


Figure 2.5: Basic input-output graph for 1st order ΣΔ modulator [33].

In the resuming subsections of this section, the basic concepts about the ΣΔ modulator are presented. The concepts of quantization noise and the effect of oversampling, noise shaping asset of the modulator and decimation are discussed for clear understanding about the ΣΔ modulator.

2.2.1 Quantization Noise and Oversampling

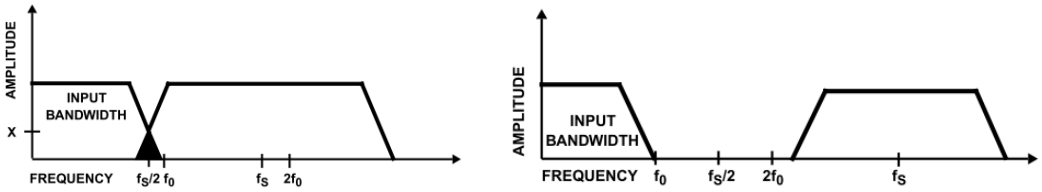
Making use of digitalization in the circuit always introduces a big obstacle of quantization noise for the designer. As the digitalizing system always responses according to the encoded bits, an irrelevant signal can cause an unintended output change, which is called quantization noise. Even though the quantization noise is random, it can be visualized as white noise and its RMS voltage can be calculated as:

$$e_{RMS}^2 = \frac{1}{q}\int_{-\frac{q}{2}}^{\frac{q}{2}} e^2.de = \frac{q^2}{12} \tag{2.12}$$

$$e_{RMS} = \frac{q}{\sqrt{12}} \tag{2.13}$$

In Equation 2.12 and 2.13, e_{RMS} notates RMS quantization voltage and q notates the LSB of the quantizer.

Remembering that ΣΔ employs an oversampled ADC logic, oversampling concept should be immerged somehow for the extraction of frequency dependent components about the quantization noise. It is no secret that while a signal is sampled, its input spectrum is copied and mirrored to multiples of the sampling frequency. When the sampling frequency is not chosen larger than the Nyquist frequency (twice the signal frequency), the signal spectrum and the mirrored spectrum intersect, which is a big sampling violation called aliasing. Figure 2.6 (a) shows the described undersampled spectrum, which causes distortion on the output signal that is recovered from the digitized data. On the other hand, the conduction of the sampling at a much greater frequency than the Nyquist frequency avoids the aliasing, and is called oversampling. Figure 2.7 (b) shows the oversampled signal spectrum [34].



(a) (b)

Figure 2.6: (a) Undersampled and (b) Oversampled signal spectrums [34].

Referring Figure 2.6, the Oversampling Ratio (OSR) is defined as:

$$OSR = \frac{f_s}{2.f_0} \tag{2.14}$$

In Equation 2.14, f_s is the sampling frequency and f_0 is the bandwidth of the signal.

As the noise spectral power of the quantized data is hold till the half of the sampling frequency, a basic integration with bandwidth boundaries would yield:

$$e_{RMS}^{in-band} = \frac{q}{\sqrt{12}}\sqrt{\frac{2.f_0}{f_s}} = \frac{e_{RMS}}{\sqrt{OSR}} \tag{2.15}$$

In Equation 2.15, $e_{RMS}^{in-band}$ notates the in-band quantization noise voltage and it's obvious that the increased oversampling ratio decreases the in-band quantization noise. This is a general feature that oversampling converters maintain and make them so fancy in the modern world. Figure 2.7 shows the described oversampled noise spectrum [33].

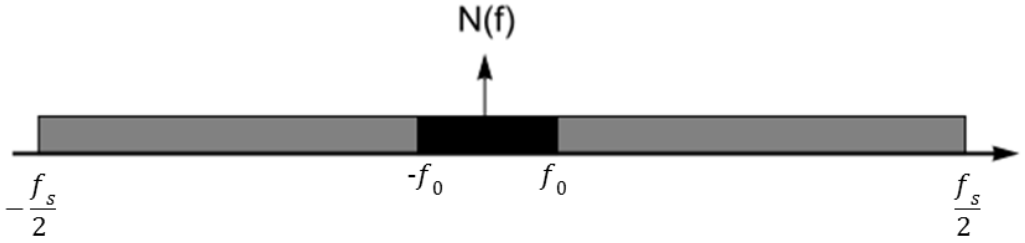


Figure 2.7: Noise spectrum for an oversampled ADC [33].

2.2.2 Noise Shaping

The positive effect of the oversampling compared to Nyquist converters is safely transferred to sigma-delta modulators. The existence of an integrator however, provides the designer with an alternate response. Figure 2.8 illustrates first order sigma-delta modulator in s-domain.

Note that in Figure 2.8, the quantizer is simple shown as a quantization noise source and integrator is modeled as a perfect one.

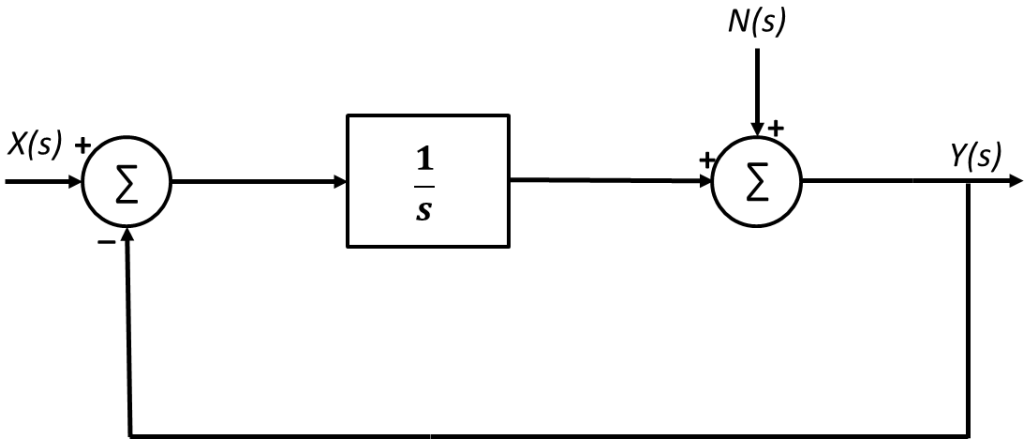


Figure 2.8: s-domain sigma-delta modulator.

Addition of an integrator to the loop introduces an extra frequency dependent term to the spectral noise density equation because the integrator plays subtraction role in the noise loop. Through the calculation shown in [35], the in-band quantization noise voltage for first order sigma-delta modulator can be presented as:

$$e_{\sum\Delta}^{in-band} = e_{RMS}\frac{\pi}{\sqrt{3}}\left(\frac{2f_0}{f_s}\right)^{\frac{3}{2}} \tag{2.16}$$

Analyzing Equation 2.16 through replacement of Equation 2.14, the inverse proportionality between the oversampling ratio and the in-band quantization

noise is proven, meaning that increasing the oversampling ratio decreases the in-band quantization noise significantly (9dB per two factor) in sigma-delta modulators. At this point, the effect caused by insertion of an additional integrator to the looping can be further analyzed. Implementation of a second order sigma-delta modulator yields an in-band quantization noise of:

$$e_{2-\sum\Delta}^{in-band} = e_{RMS}\frac{\pi^2}{\sqrt{5}}\left(\frac{1}{OSR}\right)^{\frac{5}{2}} \tag{2.17}$$

Equation 2.17 clearly illustrates the positive effect of integrator addition in quantization noise suppression. 9dB noise suppression per OSR doubling in single order modulator is now enhanced to 15dB with a single integrator addition. So interpreting for addition of several integrators, we conclude with the equation:

$$e_{M-\sum\Delta}^{in-band} = e_{RMS}\frac{\pi^M}{\sqrt{2M+1}}\left(\frac{1}{OSR}\right)^{\frac{(2M+1)}{2}} \tag{2.18}$$

Referencing Equation 2.18 M corresponds to the order of the ΣΔ modulator, in other words the number of the integrating functions inside the loop. Further increase in the loop order leads to a better noise suppression performance, which clearly illustrates the noise shaping property of ΣΔ modulators. Figure 2.9 shows the in-band noise characteristics swept across the sampling frequency for ΣΔ modulator having M number of integrators.

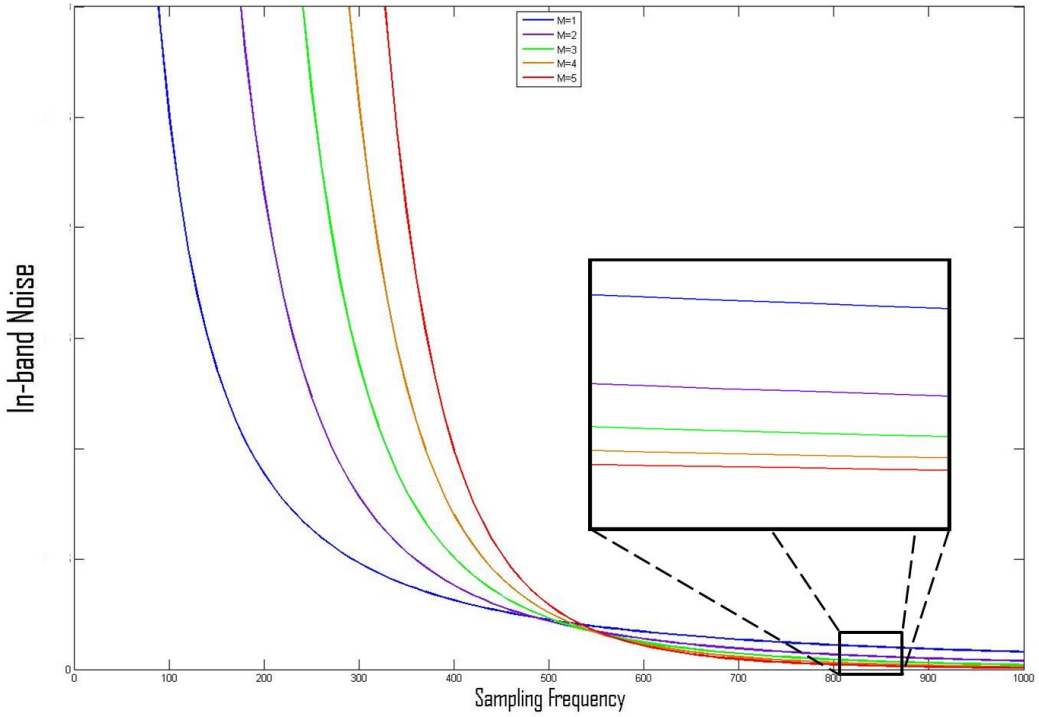


Figure 2.9: Noise shaping characteristic for 1st to 5th order ΣΔ modulator.

Referring to Figure 2.9, it is obvious that the in-band noise voltage has a low-pass filter characteristic. The effect of the sigma-delta loop shaping the noise observed at the output is to be considered. Extracting the transfer function for the input and the noise in reference to Figure 2.8 is crucial in observing the noise shaping. Using the superposition theorem and neglecting the N(s), we observe the loop transfer function as:

$$Y(s) = \frac{1}{s}(X(s) - Y(s)) \tag{2.19}$$

$$\frac{Y(s)}{X(s)} = \frac{1}{s+1} \tag{2.20}$$

It is obvious that the loop shows a low pass characteristic for the input signal. For input signal at low frequencies, which is the case for sensor interfaces, the input signal is transferred directly to the output. Flipping the loop and now letting X(s) be zero for the extracting of noise transfer function (NTF(s)), we observe:

$$Y(s) = N(s) - \frac{1}{s}Y(s) \tag{2.21}$$

$$\frac{Y(s)}{N(s)} = \frac{s}{s+1} = NTF(s) \tag{2.22}$$

The noise transfer function of the loop, (NTF(s)) is found out to have a high-pass characteristic. It can be concluded that the utilization of ΣΔ modulator with oversampling causes the quantization noise to spread over the wide sampling spectrum and the in-band noise spectrum to decrease. Simply, the ΣΔ modulator pushes the noise to high frequencies, which is afterwards filtered, discussed in detail in coming subsection.

2.2.3 Digital Filtering

With the acquisition of oversampled digitized data, the feedback is supplied for the system stabilization. However, for the successful readout of the input-referred output, digital filtering step is a crucial component. Digital filtering step carries a big importance because at this very step the noise spread across the sampling bandwidth and shaped by the ΣΔ modulation is filtered-out. Furthermore, digital filtering converts the 1-bit high-frequency sampled data to a feasible frequency range, with a high resolution output. Digital filtering step has two major duties:

1) Removal of the shaped excess quantization noise:

With the major goal of oversampled ΣΔ modulation conducted, namely shaping the quantization noise by transferring the most content of the noise to high frequencies, a step before the output readout has a major duty of the cutting out the out-of-band noise. Such a duty can be conducted by a simple low-pass filter with a sharp cut-off, which limits the frequency content of the input and the noise transferred to the output, and also helps to improve the resolution at the output. Figure 2.10 shows the resultant noise distribution.

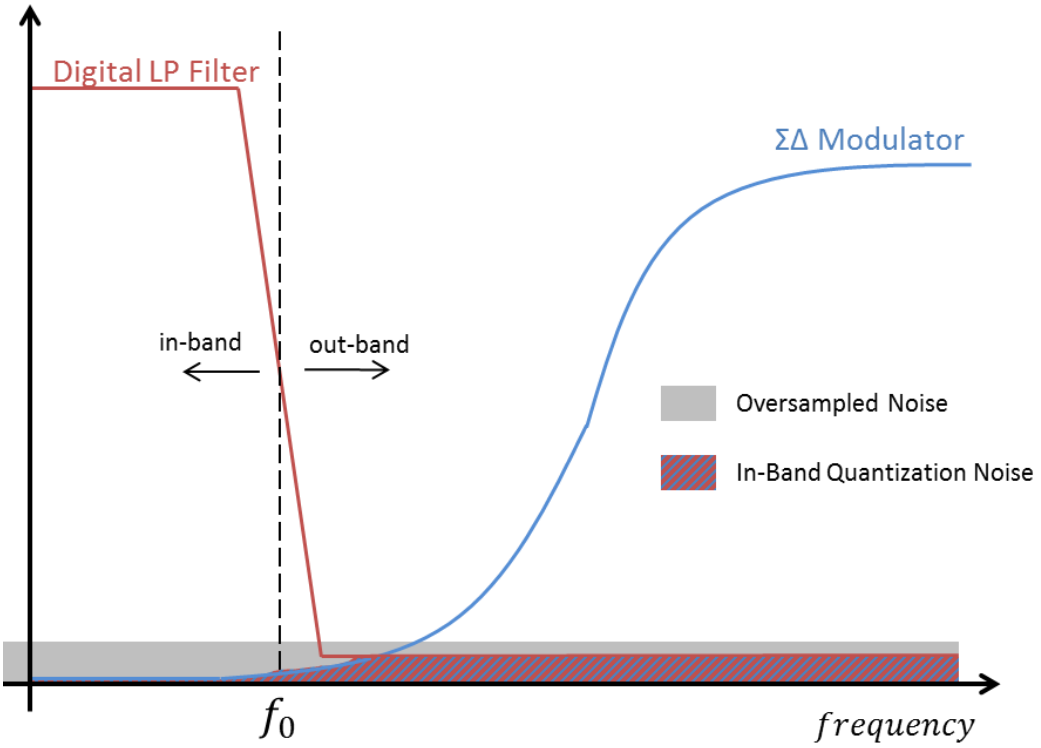
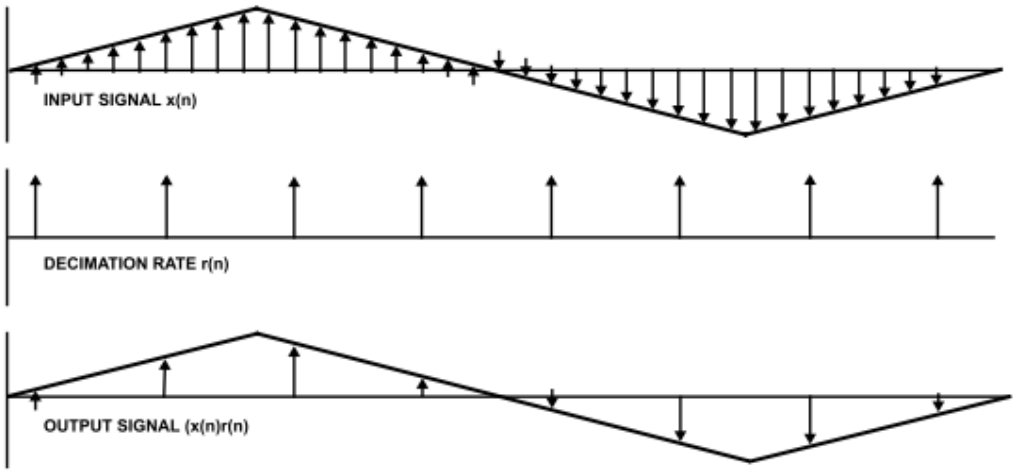


Figure 2.10: In-band noise after low-pass filtering.

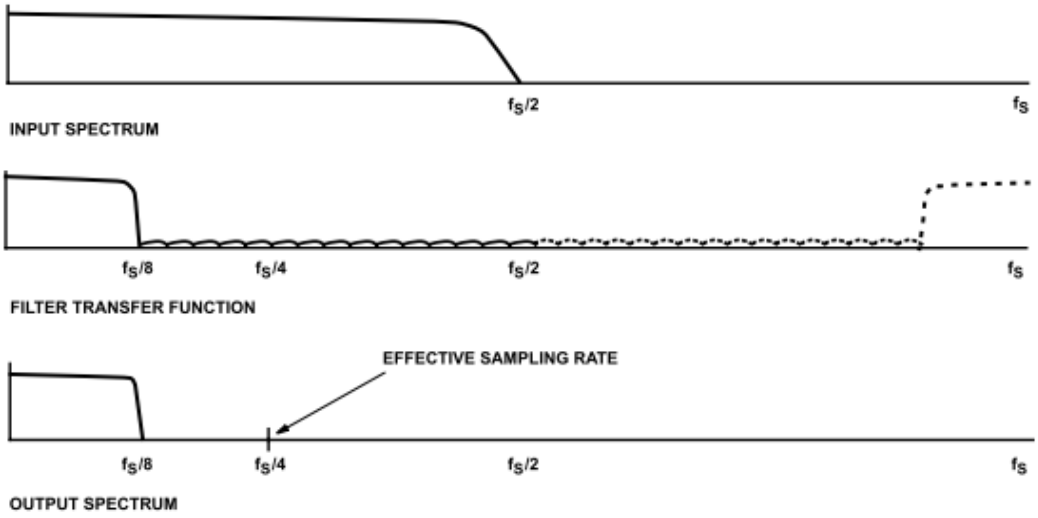
Note that the high frequency gain of the low-pass filter changes the noise observed in a great manner. Hence, a low-pass with a very sharp cut-off characteristic and nearly zero high frequency gain should be implemented, which a separate state-of-art issues itself.

2) Sample rate reduction (Decimation):

The advantages of sampling the input with a frequency much higher than the Nyquist frequency are obvious, as discussed. However, referring the sampling theorem, for the non-distortional reconstruction of the input signal, the sampling frequency should be twice the input frequency. In decimation step, the oversampled data rate is decreased to a reasonable rate with the suppression of redundant data, which is an extensive load for digital data processing, storage and transmission [33]. Figure 2.11 shows the decimation in time domain and frequency domain [34].



(a)



(b)

Figure 2.11: Illustration of decimation in (a) time domain, and (b) frequency domain [34].

It can be concluded that for the state-of-art implementation of the ΣΔ modulator, the related concept presented in this chapter should be implemented with the edge knowledge, therefore understood correctly.

CHAPTER 3

DESIGN AND SIMULATIONS OF ΣΔ MODULATOR CIRCUIT

The basic principle of the feedback, creating a signal pretty close to the input can be utilized with the accelerometer in a manner that the movement of the accelerometer is always kept at zero. The theory is called electromechanical feedback, and is a wide spread concept in inertial sensors. The concept of the electromechanical ΣΔ modulation is explained in the first section of the chapter together with the deficiencies of the low-order modulator and the need for the high-order modulator will be supported. This section also includes the system architecture of the proposed loop in the thesis. Every black box in the circuit will be clarified with the corresponding design parameters and the specific simulations will be discussed. Finally total system simulation yielding the expected parameters is to be conducted. The versatile nature of the loop is also simulated by creating a space for 5 different parameters of the accelerometer.

3.1 Electro-Mechanical ΣΔ Modulation Circuit

The advantages of employing a ΣΔ modulation circuit have been clarified. Keeping the line, the emphasis that the capacitive MEMS acceleration sensor, called the accelerometer can also be excited, meaning that the location of the

proof mass can be altered proportional to the sensor sensitivity and the voltage applied to the electrodes has been gained. Mashing these advantages in a single system called electromechanical ΣΔ modulation is a brilliant idea, proposing priceless advantages like increased linearity, enhanced bandwidth and boosted dynamic range.

3.1.1 Second-Order Electro-Mechanical ΣΔ Modulation

The basic implementation of the electro-mechanical ΣΔ modulation is the second-order loop. Figure 3.1 shows the second-order electro-mechanical ΣΔ modulation circuit.

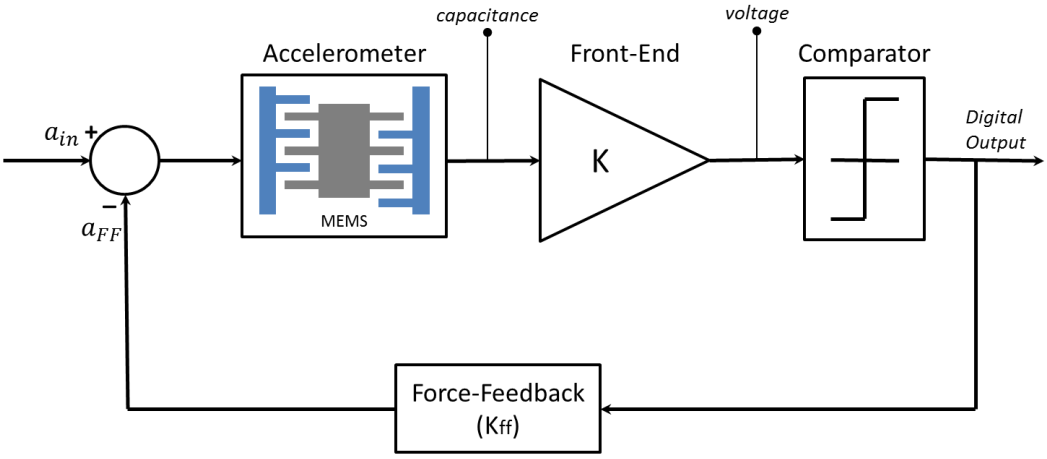


Figure 3.1: Block diagram of second-order electro-mechanical ΣΔ modulator circuit.

In the second order system, the mission of two-order integration is accomplished by the accelerometer in the loop. The second order low-pass transfer function of the accelerometer shapes the quantization noise, and integrates the difference with the inputted acceleration and the force-feedback force. The difference in the accelerometer causes some displacement in the accelerometer, resulting in gap change between the comb-like electrodes. The described change is generates an alternate capacitance value at the output of the accelerometer. The capacitance

change is sensed by the front-end electronics and converted to voltage, as an electronic interface value. The resultant voltage is feed to a comparator accordingly, where a PDM signal is achieved, defining the polarity for the force-feedback. As a principle in the sigma-delta converters, the force-feedback tries to suppress the motion of the proof mass by the application of a potential to corresponding electrodes. Note that the digital output is an oversampled signal, and the whole procedure described happens in a tick of a second.

Similar to its ancestor, sigma-delta modulator, electro-mechanical ΣΔ modulator also shapes the quantization noise, spreads the noise across the sampling bandwidth. However, the quantization noise shaping is now dependent on the accelerometer parameters, as the sensor is utilized as the integrator of the loop. In the following case, the limited DC gain in pre-quantization integration step of the loop (accelerometer + front-end) is a serious obstacle in designing high-performance circuit. Figure 3.2 graphically illustrates the limited DC gain problem and associated noise characteristic.

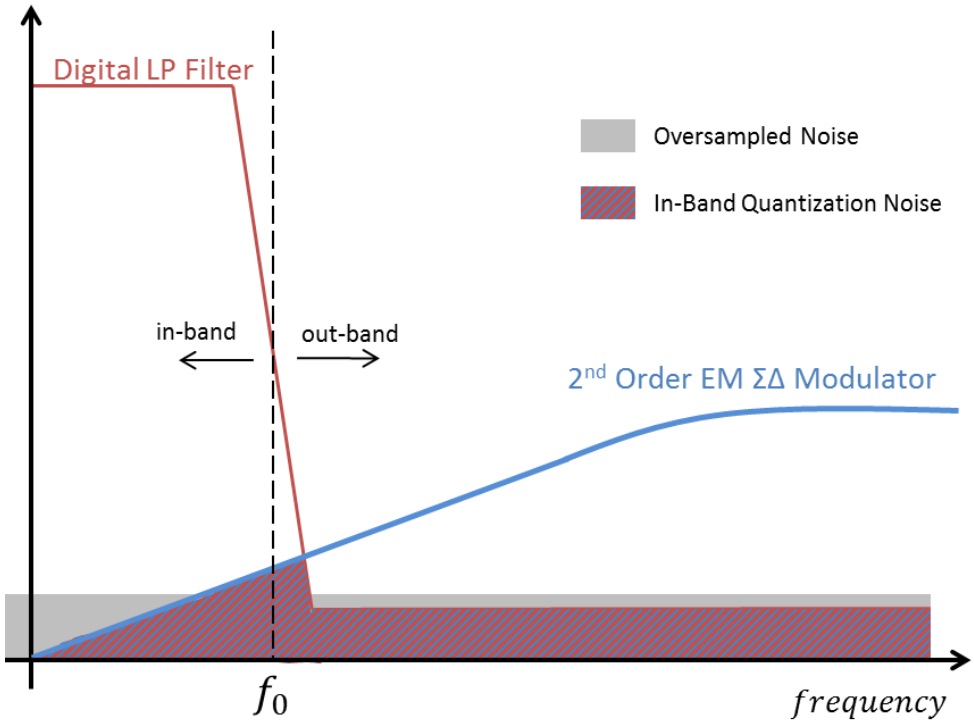


Figure 3.2: Noise characteristic of the 2nd order electro-mechanical ΣΔ modulator.

The low-pass characteristic of the integration step can be improved to overcome the obstacle though. However, for the solution of the problem a big sensor with large proof mass and small springs have to be designed. The conduction of such a design violates the general logic of MEMS, wandering away from the advantages of the micromachining such as small-scale and cost efficient fabrication.

In addition, the limited DC gain of the accelerometer introduces a huge problem called ‘dead-zone’, observed when only the accelerometer is utilized as the integrator in the loop. Dead-zone is referred to a problematic acceleration input range, in scope of which the external acceleration does not cause any changes at the output. The main reason of this happening is that during the application of slight DC external acceleration in steady-state condition, the inadequate accelerometer DC gain cannot cause enough fluctuations for altering the oscillating voltage inside the loop, fed to the quantizer. Therefore, only sign dependent quantizer does not alter the output stream. In top level, the accelerometer has a proportional displacement, causing only a DC change at the input of the quantizer, thereby no reflection to the output.

The further development of the loop should be considered through the electronic interface circuitry. First and the most promising step for further improvement is increasing the order of the loop by addition of extra integrators electronically.

3.1.2 High-Order Electro-Mechanical ΣΔ Modulation

It is obvious that remaining dependent on the accelerometer as the low-pass noise shaping characteristic supplier is highly unwise. Even though the modern micromachining technologies empower the fabrication of high performance mechanical structure with negligible tolerances, the current situation requires an external involvement to the loop for a high performance system. Keeping the trend, the proposed design may be extended in a way that the major problem of fumbling several sensors in a run can be overcome. For the batch fabricators, as the mechanical properties such as stress differ in the outer limits of the die, and

the interface circuit designs specifically aim for the high performance of accelerometers with dedicated mechanical parameters, the accelerometers showing little divergence in the mechanical parameters are thrown away. Hence, for the wide spread application the design circuit should be suitable for interface connection with sensors of different parameters.

The major logic of increasing the number of the integrators in the circuit is stimulating the low-pass characteristic of the loop. Immerging extra integrators with the perfectly characterized electronic properties, which is relatively easy to conduct in digital domain will suppress the low DC gain and help shaping the noise characteristics of the circuit, as explained in sub-section 2.2.2. Furthermore, cascaded electronic integrator connection overcomes the dead-zone problem because of the stimulated DC gain boost in pre-quantization steps of the loop. Figure 3.3 shows the block diagram for M order electro-mechanical ΣΔ modulator circuit.

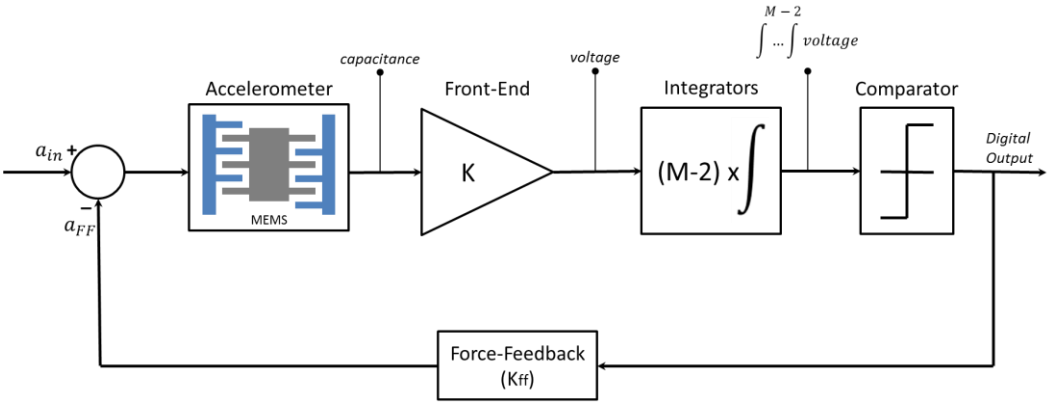


Figure 3.3: Block diagram of an M order electro-mechanical ΣΔ modulator circuit.

As previously described, the accelerometer adds two integrations to the loop. Therefore, for the design of an M order electro-mechanical sigma-delta loop, M-2 number of electronic integrators should be implemented.

The implementation of extra electronic integrator forces the designer to face with a new concern of stability. With the increase in the count of the integrators in the loop, noise characteristic improves trading off from the stability edge. The stability of the circuit deteriorates with the straightforward augment of the electronic integrators, because the loop gain is not enhanced thereby. Hence, the addition of extra integrators after the desired quantization noise shaping achievement is nonsense and the number of the electronic integrators should be chosen wisely. By desired quantization noise shaping statement, the suppression of the quantization noise down to non-primary noise source is meant.

It is noteworthy that the exact model extraction of the integrator in electronic domain is more feasible than adaptation of a mechanical integrator. Controllable electronic integrators can be utilized as noise shapers, where the trade-off between the noise and the stability can be played accordingly. Moreover, PI controllers can be adopted as an integrator for supplying alongside boost to the loop gain.

Last but not the least; a chief development that can be emerged is employing additional controllable integrators in digital domain [36-38]. Digital domain integration offers the system a whole new concept of adaptive control. Digital domain control though requires the adaptation of an Analog-to-Digital Converter (ADC), which introduces a secondary quantization noise. Luckily, the sigma-delta modulation and linear calculation techniques can also be used to shape the secondary quantization noise (ADC quantization noise), opening a new prospect design for us [26].

3.2 Proposed System Architecture

To fulfill the objectives of the thesis, a 5^{th} order electro-mechanical $\Sigma\Delta$ modulator circuit is proposed. The two order of integration to the loop is supplied in analog domain by the mechanical accelerometer sensor, where the remaining 3 order of integration is conducted in digital domain by the processor unit of the

FPGA. The use of digital filter enables critical loop parameter swap at any time, helping the designer to employ adaptive control. However, for the integration to take place in digital domain the voltage output from the front-end should be converter to digital domain. Extra employment of an ADC introduces an addition quantization noise source, which should be taken care of. That is exactly why the loop order was increased while the fourth-order modulation was also enough for suppression of in-band quantization noise. Furthermore, for adaptation of the front-end with the wide range of sensors require the circuit should be approached in a simple manner and the requirements on analog circuitry should be relaxed somehow. Figure 3.4 shows the block diagram of the versatile 5^{th} order ΣΔ modulator circuit proposed for capacitive MEMS accelerometer characterization.

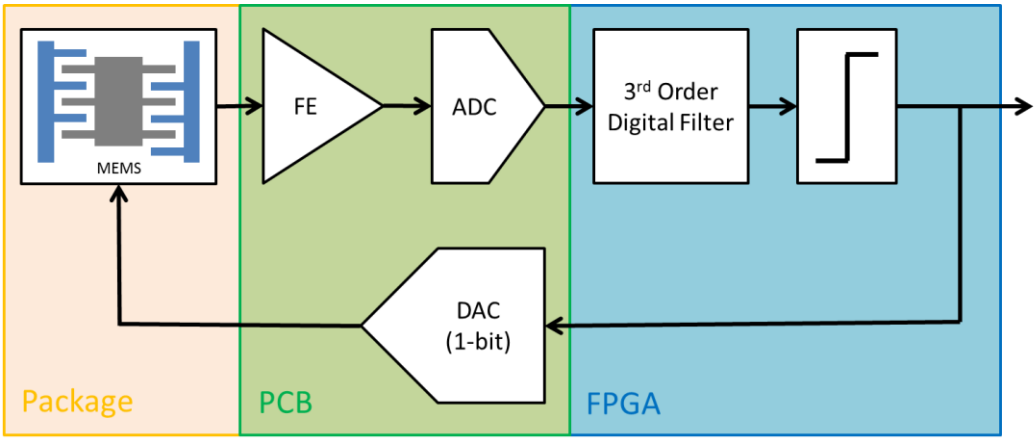


Figure 3.4: Block diagram of the proposed versatile 5^{th} order ΣΔ modulator circuit.

The accelerometer is a mechanical sensor reacting to external acceleration by deflecting from its initial position. The dislocation causes the embedded capacitances inside the sensor to change, which can be sensed through several transductions. In the proposed structure, voltage-mode approach is utilized for sensing the voltage change in the proof mass of the sensor. The voltage change is amplified by the front-end electronics, which is adaptive to wide range of sensors because of its simplicity. For the process of the analog signal in the digital

domain, Analog-to-Digital Converter (ADC) is employed. Oversampling nature of ΣΔ modulators allows design relaxation in analog chain, resulting in the use of 7-bit ADC to be sufficient. However, hiring a low-bit ADC imposes a secondary quantization error that can also be shaped by ΣΔ modulator through linear techniques, meaning that the conversion resolution need is suppressed thereby. The acquired digital data is supplemented in digital domain, where the integrator parameters are adapted accordingly. Furthermore, digital filters are also used to supply proportional gain to the system for loop stability. The choice of triple integration in the FPGA is made for shaping the ADC quantization noise and increasing system resolution. Lastly the signal is quantized and converted to Pulse-Density Modulated (PDM) form. Note that electrostatic force linearization nature of the oversampled PDM output is exploited as the feedback to the accelerometer. Well adaptation of the sigma-delta with time multiplexing enables the use of the same electrode at sense and feedback phases. Therefore, the dislocation of the accelerometer is counteracted by the PDM signal, increasing the linearity and the range of the system in a great sense.

Also note that the implementation is conducted on 3 different platforms. The accelerometer is placed in a package. A minimum size package slightly larger than the accelerometer sensor and containing at least 3 pins is sufficient. The package containing the sensing element is mounted on a PCB, which contains the discrete components of the front-end circuit and the ADC. The PCB is mounted on the FPGA evaluation board through which the data streaming and switch is compiled. Coming subsections will in deep analyze the parts of the proposed loop.

3.2.1 Voltage-mode readout

The acceleration data extraction method from the accelerometer is much different than the accustomed ones. The designs conducted all over the world address the individual needs of special sensors. The adaptation of the circuit with wide range

of range sensors is not a design issue for most designers. However, for the foundries with mass manufacturing, the versatility of the circuit that enables its use for characterizing all sensors in a run is relatively newly desired property. Acknowledging this as a goal, a front-end circuit that can adapt to variety of sensor without the need to be redesigned is designed.

In accustomed circuits, the front-end capacitance to voltage conversion amplifier is switch-capacitor and operates by charge integration logic in capacitive circuit. Even though the conventional implementation of these circuits with CMOS technology is effective and controllable with PLL's and clock generators, switch-cap circuits are not easy to be implemented with discrete components on a PCB. In the proposed design, the main logic is the readout of the middle voltage change in the accelerometer due to the charge sharing concept. To emphasize the judgment of the voltage-mode readout, the sensing node voltage is calculated impedance and charge vise. Figure 3.5 shows the simplified view of the excited accelerometer as the embedded capacitors.

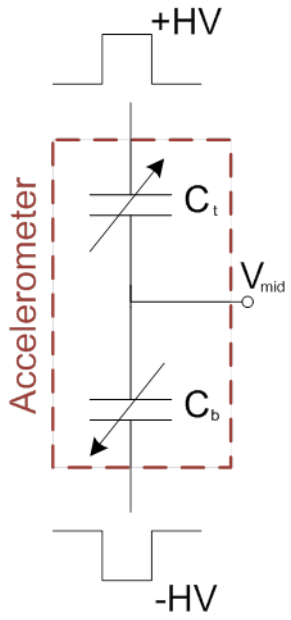


Figure 3.5: Illustration of an excited capacitive accelerometer with the sense out node marked as V_{mid}

Impedance vise:

Knowing that the impedances for the capacitors are $\frac{1}{s.C_t}$ and $\frac{1}{s.C_b}$ respectively, the voltage accumulated on the bottom capacitance can be written as

$$V(C_b) = \frac{\frac{1}{sC_b}}{\frac{1}{sC_b} + \frac{1}{sC_t}} * 2HV = \frac{C_t}{C_t + C_b} * 2HV \tag{3.1}$$

Therefore, V_{mid}voltage can be computed as

$$V_{mid} = -HV + 2HV \frac{C_t}{C_t + C_b} \tag{3.2}$$

Charge vise:

Leaning on the basic principle that the charge in every moment is the same in the circuit, charge conservation can be written as

$$2HV \frac{C_t . C_b}{C_t + C_b} = (V_{mid} - (-HV))C_b \tag{3.3}$$

In Equation 3.3, the charge stored in the series capacitance array is referenced equal to the total charge in the bottom electrode. Dividing both sides by C_b and making simple math yields

$$V_{mid} = -HV + 2HV \frac{C_t}{C_t + C_b} \tag{3.4}$$

It is obvious that charge vise V_{mid} calculation as in Equation 3.4 and impedance vise V_{mid} calculations as in Equation 3.2 yield the same result. It can be concluded that if properly excited, the proof mass node of the accelerometer can be inherently utilized as voltage output for the capacitive sensing readout. It should be noted that V_{mid} is an s-free and strongly displacement dependent voltage conversion node. As the capacitance of the top and the bottom accelerometer capacitances are strongly dependent with displacement, it is obvious that the V_{mid} node perfectly suits for the displacement to voltage conversion duty specifications. Furthermore, with the application of the electro-

mechanical feedback assuming that the displacement of the accelerometer mass is much smaller than the gap, the voltage response can be concluded as linear. It is also noteworthy that V_{mid} yields 0V when top and bottom capacitances are the same. As shown in [37], the middle voltage linear sensitivity on the displacement can be written as

$$V_{mid}(x) = HV\frac{\partial C/\partial x}{C_0}.x \tag{3.5}$$

In Equation 3.5, x is the displacement of the accelerometer, C_0 is the rest capacitance, HV is the high voltage applied to excite the accelerometer, and $\partial C/\partial x$ is the accelerometer's sensitivity which is independent of the displacement as shown in sub-section 2.1. Figure 3.6 shows the deflection of the bottom and the top capacitance for 10 step 1 g acceleration inside sensor-2.

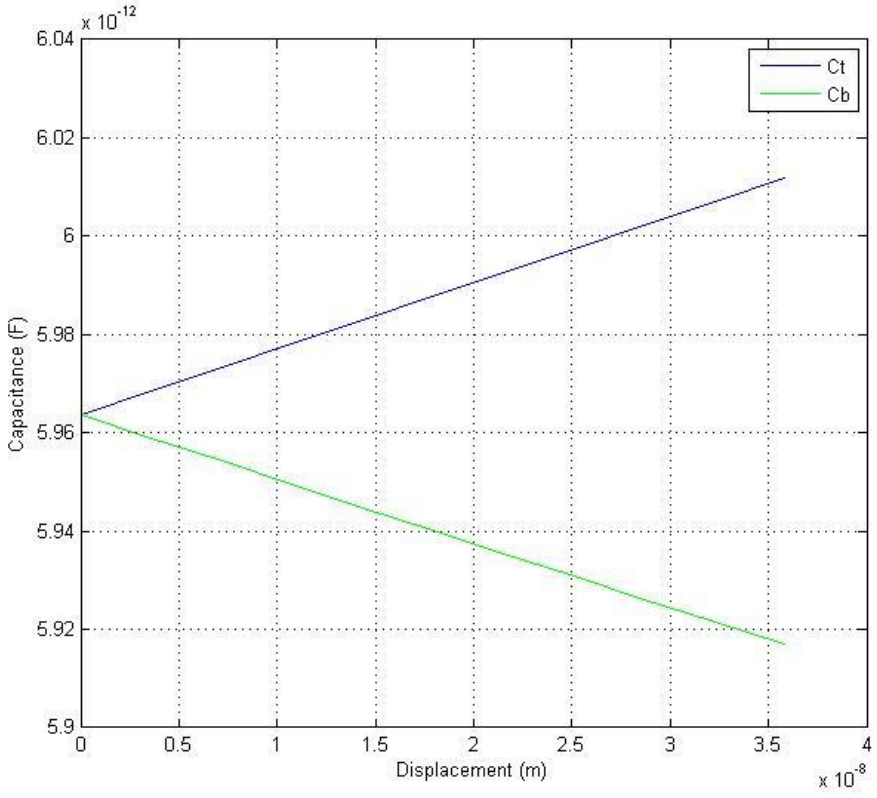


Figure 3.6: Capacitance changes of sensor-2 according to applied 10 stepped 1g acceleration.

The open loop model of the system was constructed in MATLAB Simulink environment and all the simulations were preceded thereby. Figure 3.7 shows the model constructed in Simulink Environment.

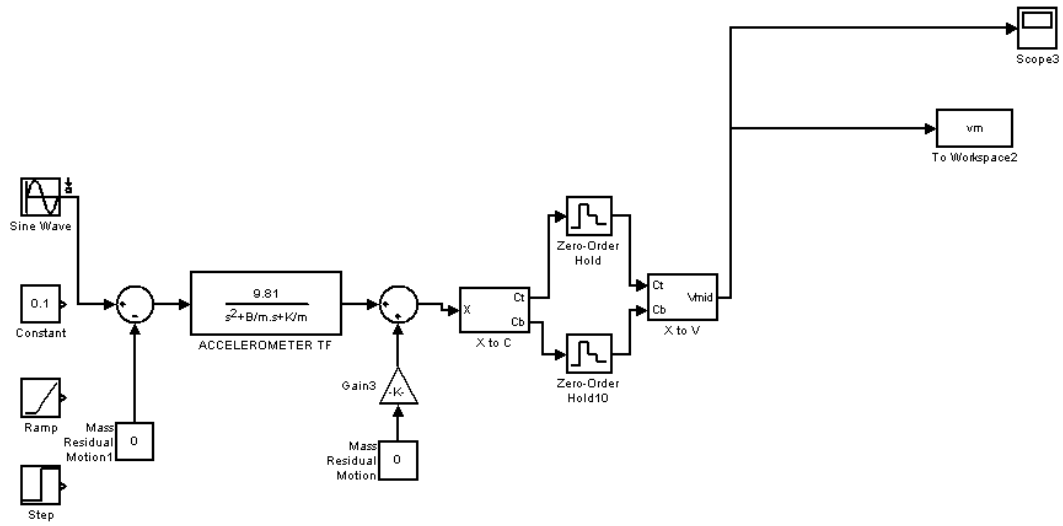


Figure 3.7: Open-loop front-end model in MATLAB Simulink Environment.

As one of the test signals, 1g amplitude 100Hz acceleration was applied for observation of the scale factor. The scale factor was found to be 71.7 mV/g in the system. Figure 3.8 shows the voltage response of the accelerometer according to the model constructed in MATLAB.

Note that a big issue in utilization of the accelerometer as displacement to voltage converter is the effect of the parasitic capacitance seen from the proof mass when the accelerometer is connected for sensing. In described condition, the proof mass voltage degrades from Equation 3.4 and becomes

$$V_{mid} = -HV + 2HV\frac{C_t}{C_t + C_b + C_p} \tag{3.6}$$

Prior to the parasitic capacitance coupling in the loop, discrete component of the voltage pre-amplified employed to supply amplification of the accelerometer voltage should be placed close to the accelerometer package.

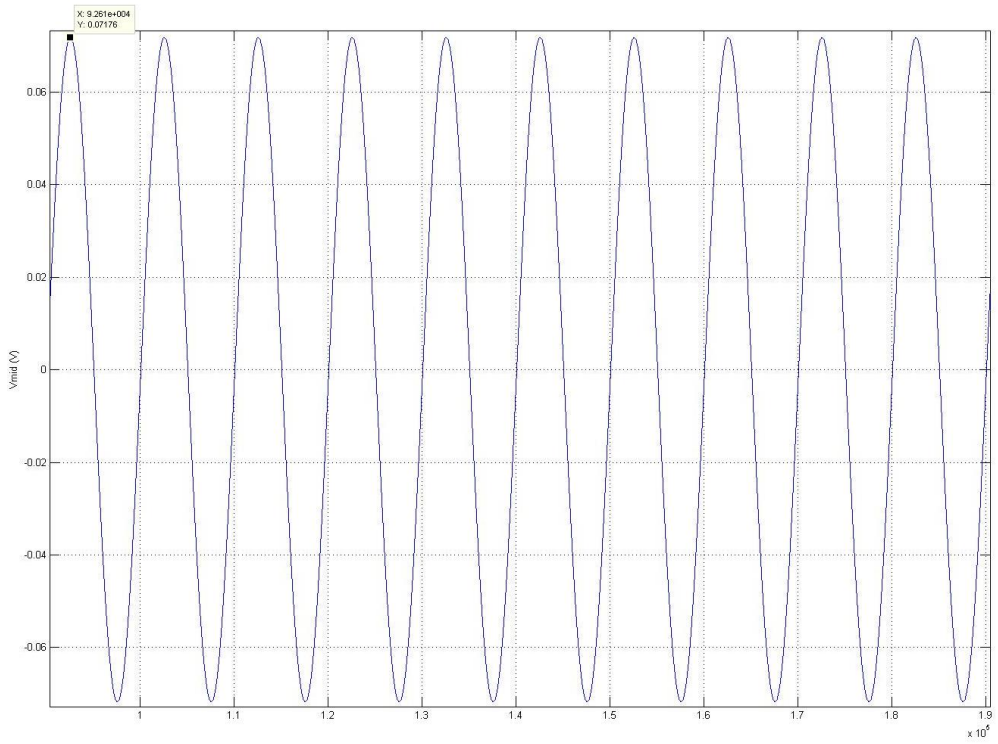


Figure 3.8: Simulated voltage output of the accelerometer according to the applied 2g peak-to-peak acceleration.

3.2.2 Pre-Amplifier

For the system stability and sealing the effect of the parasitic capacitance in the accelerometer voltage generation, a pre-amplifier circuit was employed. The input of the voltage mode amplifier is connected to the proof mass node of the accelerometer, and uses the capacitive feedback to boost the voltage generated by the accelerometer. An OPAMP with small W/L ratio transistors is used to minimize the input capacitance and hence, capacitive loads are employed for settling at limited sense period. The charge of the capacitors in the amplification phase is reset at the same time when the reset function is applied to the accelerometer sensor. Figure 3.9 shows the schematic of the voltage amplifier employed in the front-end.

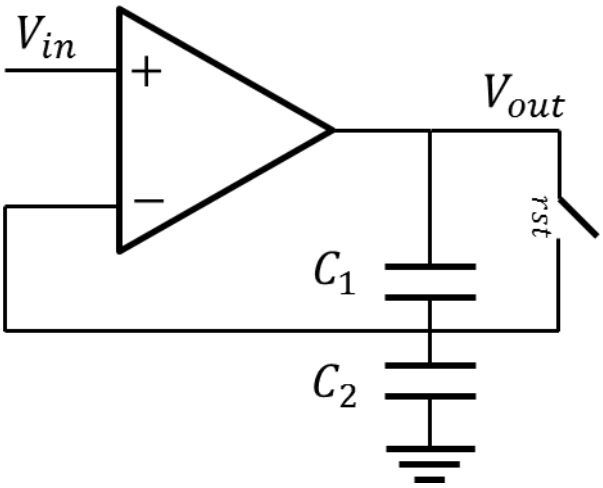


Figure 3.9: Schematic view of capacitive voltage pre-amplifier.

Referring to Figure 3.9, the voltage gain of the capacitive voltage pre-amplifier is calculated as

$$A_v = \frac{V_{out}}{V_{in}} = \frac{C_1 + C_2}{C_1} \tag{3.7}$$

Note that in contrast with the charge-mode pre-amplifier, the gain of the pre-amplifier stage has no dependency to sensor capacitance value, which exploits freedom degree of the proposed system. Furthermore, with the omission of charge injection concept, which is a huge concern in switch-capacitor circuit, the proof mass of the accelerometer is not accelerated during the sense phase. This is a huge advantage of voltage-mode amplifier application, boosting the rectification error and linearity of the total system extremely.

3.2.3 Readout Switching and Timing

The engagement of ΣΔ modulator for readout of inertial sensors offers a unique property of time multiplexing, which can be adapted for the use of the accelerometer electrodes for sensing and actuating. However, for such application

the time diagram of the phases should be carefully designed. Figure 3.10 shows the time diagram designed for the system.

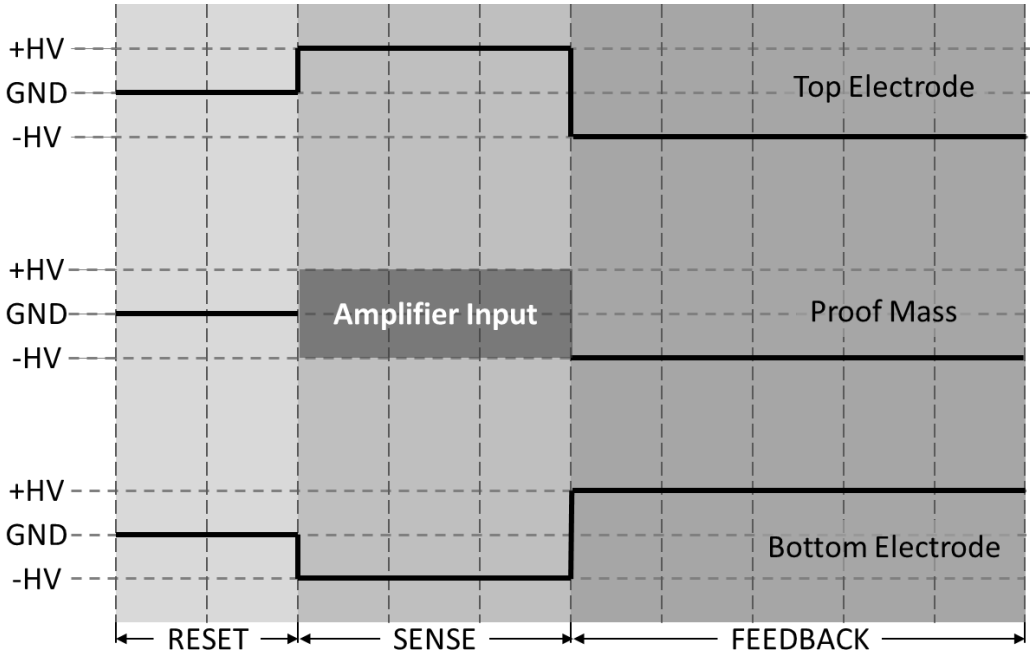


Figure 3.10: Timing diagram for accelerometer electrodes.

In the reset phase, all the electrodes of the accelerometer are intentionally short circuited to the ground to reset the embedded capacitors. This phase is chosen to be 20% of the total time.

In the sense phase, as illustrated in Figure 3.5 the top electrode is instantaneously supplied with positive voltage, where the bottom electrode is supplied with negative. The reason for this trigger is to excite the embedded capacitors inside the accelerometer. On the other hand, the proof mass electrode is connected to the pre-amplifier input for sensing the voltage as in Equation 3.5.

In the last phase of the system, according to the decision on the latter parts of the loop, the proof mass voltage together with one of the electrodes is pulled to some high voltage. The other electrode is pulled to the opposite voltage to counteract the motion of the proof mass. Note that according to the example given, prior to being pulled towards the bottom electrode, the proof mass has dislocated towards

the top electrode. The feedback phase is chosen to be half of the cycle duration for definite application of force feedback.

In contrast to the extremely complicated timing diagrams of traditional switch capacitor readouts, the employed timing diagram is very easy. The clock generating circuit needs to produce only three clocks with simple edge and transactions. Furthermore, the circuit does not need the integrate phase, which is used to buy some time for the capacitors to converge the flowing charge in switching mode front-end applications.

3.2.4 ADC & Digital Filtering

In reference to the obvious reasons discussed, the computed voltage by the accelerometer and the front-end needs to be further integrated. Conduction of such a duty in digital domain allows inclusive control of the loop parameters which are dependent on the considered integrators. Before diving to the digital domain though, the approach for the domain conversion should be further discussed. The use of ADC for this purpose is inevitable. The choice of a discrete ADC is a hard job, simplified by the oversampling and sigma-delta utilization. A 7-bit Flash ADC is used as the conversion tool in the proposed design. However, a low precision ADC presents additional quantization noise alongside, which needs to be suppressed for high resolution system. ΣΔ modulator noise shaping advantage is also used for ADC quantization noise. Therefore, the loop order selection altered at the digital domain is chosen in dependence to the ADC quantization noise.

The presentation of an ADC to the loop introduces extra quantization noise to the system as discussed. Converting the proposed design to an s-domain representation, a noise source can be placed instead of ADC in the loop. The noise source is placed after the front-end and before the digital integrators. Figure 3.11 shows the s-domain illustration of the proposed characterization circuit architecture.

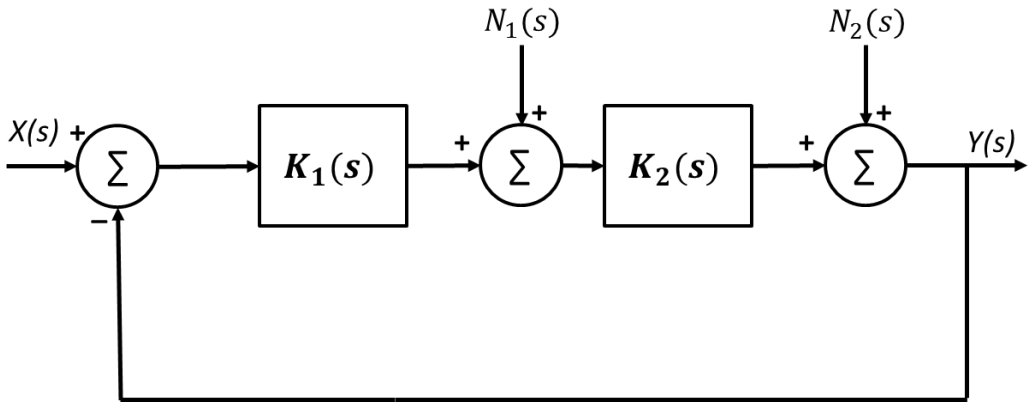


Figure 3.11: Simplified s-domain illustration of the proposed circuit

In Figure 3.11, $K_1(s)$ and $K_2(s)$ are the low-pass characteristic functions of analog and digital integrations respectively, and $N_1(s)$ with $N_2(s)$ are placed according to ADC and ΣΔ quantization noises. Extracting transfer functions of the system yields

$$\frac{Y(s)}{X(s)} = \frac{K_1(s)K_2(s)}{1 + K_1(s)K_2(s)} \tag{3.8}$$

$$\frac{Y(s)}{N_1(s)} = \frac{K_2(s)}{1 + K_1(s)K_2(s)} \tag{3.9}$$

$$\frac{Y(s)}{N_2(s)} = \frac{1}{1 + K_1(s)K_2(s)} \tag{3.10}$$

Equations 3.8, 3.9 and 3.10 show the transfer function for input, ADC quantization noise and ΣΔ quantization noise respectively. Remembering that integrators in the loop have low-pass characteristic, it is obvious that input and ΣΔ quantization noise transfer functions shows the same characteristic defined before, namely low-pass and high-pass respectively. However, ADC quantization noise transfer function is observed having a band-pass characteristic, where the filter structure is dependent on the order ratio of the analog and digital integrators. Therefore, the count of digital filter can be used to shape the quantization noise coming from the ADC. The solid assessment of two order of

integration in analog domain enables visualization of the noise shaping caused by swapping the loop order in digital domain. Figure 3.12 shows rough noise shaping characteristic for N number of hired digital integrators.

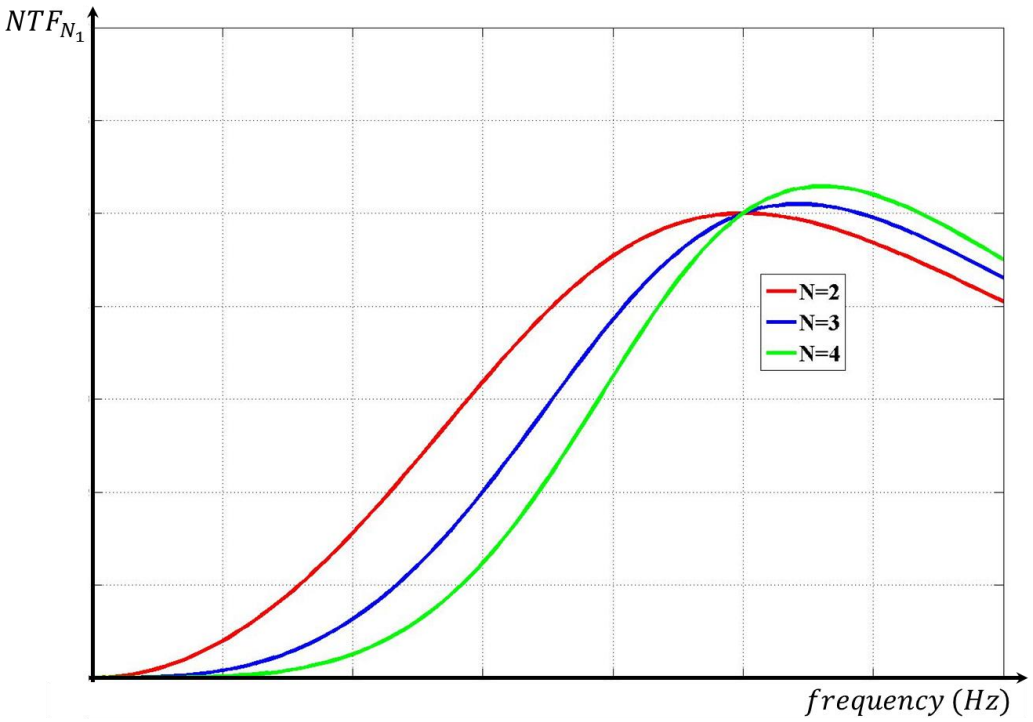


Figure 3.12: Rough illustration of ADC quantization noise shaping by the N order digital filter of the proposed loop.

It can be concluded referring Figure 3.12 that even though twice integration in the digital domain is enough for sigma-delta quantization noise suppression, 2nd order digital filters would fall short in shaping ADC quantization noise. Therefore, 3rd order digital integrator is employed in the FPGA.

3.3 System Level Simulations

For the observation of the proposed theory, conduction of system level simulations is crucial. The system level simulations were carried in SIMULINK environment of MATLAB on the base of system parameter's alterations and

visualization of output and corresponding system definitions. To define the versatile nature of the proposed loop, accelerometers with interchanged structural parameters were simulated in a step-by-step fashion. Else to say, for different parameters of the accelerometer connected to the loop, the effect of rest capacitance, sensitivity change on crucial parameters such as velocity random walk, settling time was observed. However, to conduct the simulations, a top level model of the whole loop needs to be designed. Figure 3.13 shows the MATLAB Simulink model constructed for versatile 5^{th} order electromechanical ΣΔ modulator.

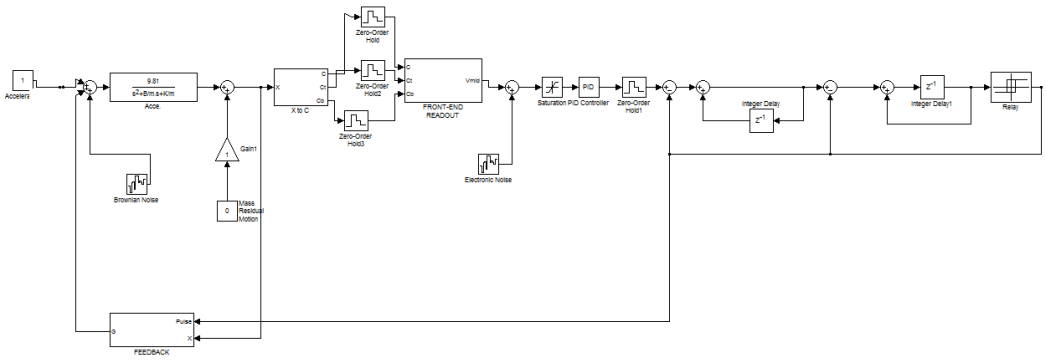


Figure 3.13: MATLAB Simulink model for the proposed ΣΔ modulator.

As in Figure 3.13, the accelerometer is modeled as in sub-section 2.1.1. The accelerometer is a single transfer function that generates displacement according to the applied acceleration value. At this entry node, Brownian noise is inserted as a fluctuation on the applied acceleration. The displacement output of the accelerometer is summed up with mass residual motion, and fetched as an input to voltage mode readout and electromechanical feedback force generator. To count the differences of the simulation model from the original model it should be firstly noted that one of the integrators in digital domain is designed as PI controller and the gain stage (pre-amplifier) is simulated through the proportional gain of the controller. PI is also placed for the additional gain need for stability of the loop to be supplied. For initial observation of the proper operation of the

model, a sample 1g signal is applied and output bit stream is observed. Figure 3.14 shows a sample output bitstream with the application of 1 g acceleration to SENSOR-2.

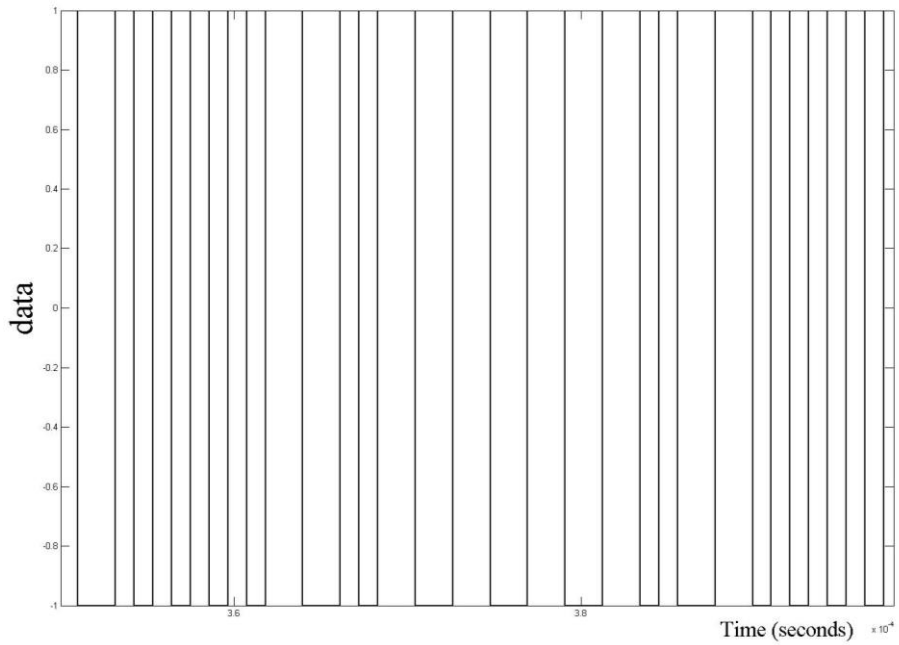


Figure 3.14: Output bitstream for 1g application in closed-loop to SENSOR-2.

As the result may seem a little awkward in terms of scientific expression, the changing pattern of the pulse width explains much. When the time frame of the data was widened, it was observed that the same pattern showed itself repeatedly throughout the whole time spectrum. That combined with the ramping power spectrum at the output; to be shown later in this chapter proofs the proper operation of the sigma-delta loop.

For observation of the versatility of the proposed design, all the noise sources except the self-induced were killed and several simulations were carried with SENSOR-1 taken as a reference. The main goal was to see whether the circuit can maintain stable operation with same altered mechanical parameters, affecting the accelerometer output from minor to major scales. To provide a reference, SENSOR-1with the original parameters was simulated. Table 3.1 shows the results obtained for SENSOR-1 simulations.

Table 3.1: MATLAB Simulink simulation results for SENSOR-1.

Mechanical Inputs					
Gap	2 μm	Anti-gap	7 μm	# fingers	352
Mechanical Outputs					
Mass	266 ng	Q factor	0.42	Spring c.	56.28 N/m
Rest Cap.	10.4 pF	Cap. sensitivity	3.75 μF/m	Range	10.66 g
PID Parameters					
Proportional Gain	1		Integral Gain	1000	
Electrical Outputs					
VRW	$1.6\mu g/\sqrt{Hz}$	Scale factor	47 mV/g	Settling time	1 ms

It is noteworthy that on all the simulations to be discussed in this chapter, the sampling frequency, in other words the frequency of the digital clock was taken as 1MHz. The time period of the clock signal was used to apply feedback and to extract digital data from the decimated output of sigma-delta converter in MATLAB Simulink environment.

As a proof to the proper operation of the loop, a 1 V 100 Hz signal, deducing 1g 100 Hz acceleration was applied to the loop and the resulting feedback voltage was monitored. Figure 3.15 shows the applied signal together with the feedback voltage on the same scale. It is obvious that one can see a slight voltage difference between the applied and induced voltage. Even though this difference may seem a threat for stable operation, actually it is not. It is the induced quantization noise of the system, an inevitable nature of digitization.

Even though the main goal of the research is to observe the operation of the readout circuit for accelerometers with wide range of mass or rest capacitance for example, the correlated nature of these structural parameters remain as an

obstacle in parameter sweep analysis. As rest capacitance, sensitivity, spring constant and in terms, quality factor are dependent on several properties, they were defined as mechanical output of the accelerometer system and observed in accordance with electrical outputs. Therefore, in resuming simulations the change will be implemented on spacing and number of fingers inside the accelerometer leading to changes in mechanical parameters of the structure and figures corresponding to electrical results will be discussed.

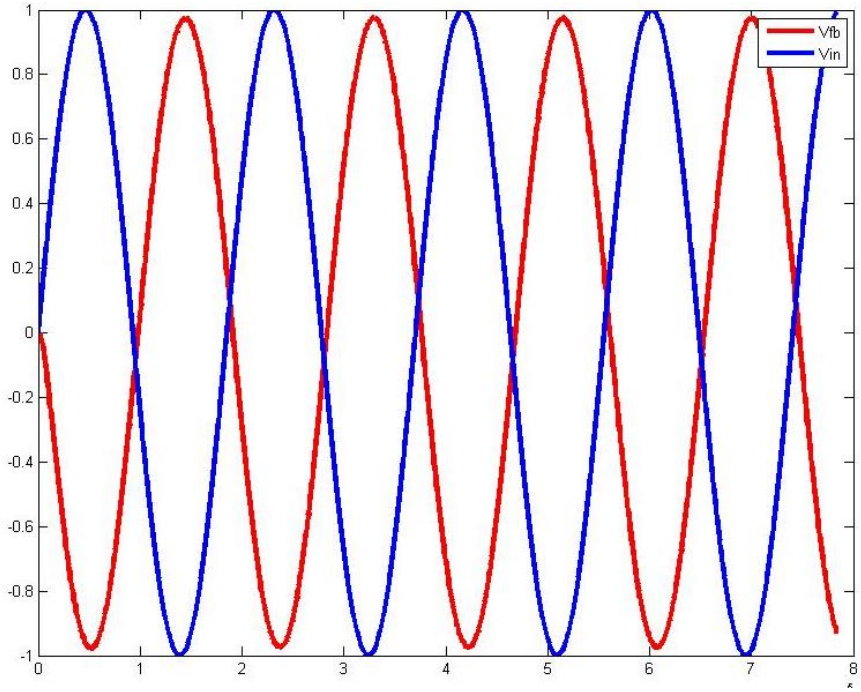


Figure 3.15: Transient simulation of SENSOR-1 with 1g 100Hz input.

In the first phase of alternative simulation conduction, the focus was maintained on gap between the fingers. The gap spacing was increased from 2 micrometers to 2.3 micrometers. A minor change was made intentionally for observation of changes on electrical outputs. Table 3.2 summarizes the simulation parameters and obtained results. Figure 3.16 shows the power spectral density of the defined accelerometer setup and Figure 3.17 shows the step response of the loop with described parameters.

Table 3.2: MATLAB Simulink results for increased gap SENSOR-1.

Mechanical Inputs					
Gap	2.3 μm	Anti-gap	7 μm	# fingers	352
Mechanical Outputs					
Mass	266 ng	Q factor	0.307	Spring c.	56.28 N/m
Rest Cap.	9.34 pF	Cap. sensitivity	2.72 μF/m	Range	7.83 g
PID Parameters					
Proportional Gain	1		Integral Gain	1000	
Electrical Outputs					
VRW	$1.77\mu g/\sqrt{Hz}$	Scale factor	65.2 mV/g	Settling time	1 ms

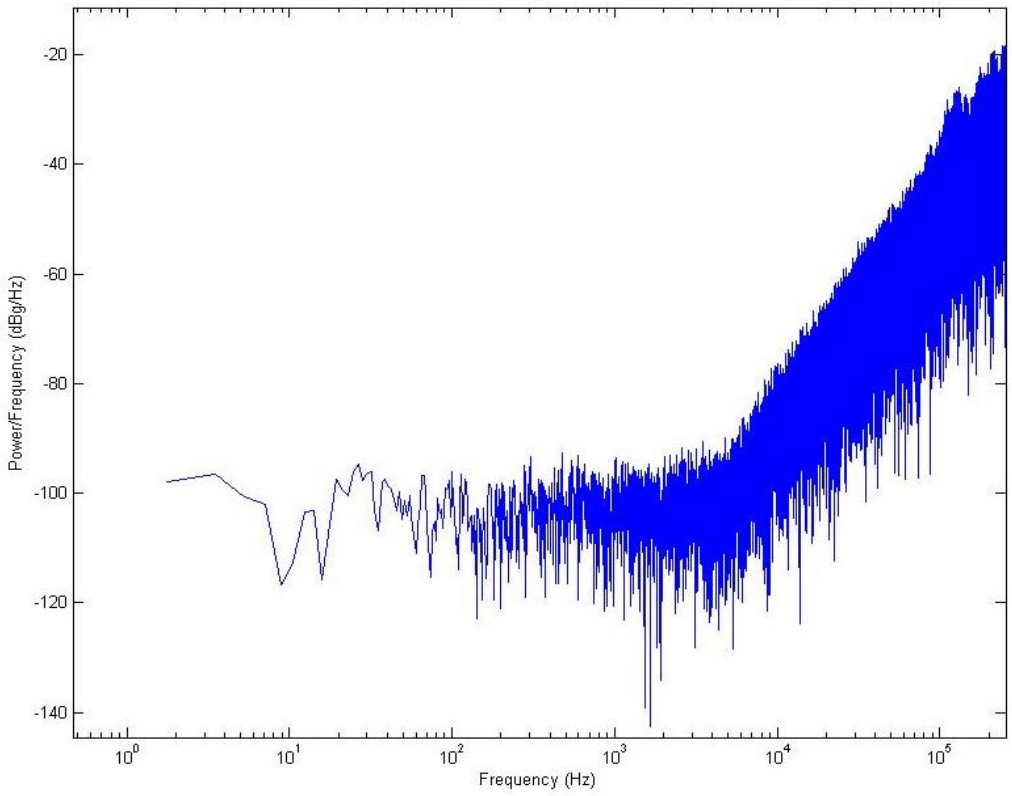


Figure 3.16: PSD for increased gap SENSOR-1 simulation.

The slight increase in the spacing of the capacitive fingers changes the rest capacitance and capacitive sensitivity of the accelerometer, which in accordance alters the range and the scale factor of the system drastically. Note that there was no need for changing the controller parameter for stable operation and the system reacted in similar time with the reference. Furthermore, the bottom floor on PSD was concluded as -104.5 dBg/Hz, yielding a noise floor of approximately 8 $\mu g/\sqrt{Hz}$.

In the second phase of alternative simulation conduction, the focus was shifted to the finger count. The number of capacitive fingers was decreased from 352 to 100. This dramatic change was intentionally applied for illustration of stable operation even under large changes of mechanical outputs. Table 3.3 summarizes the simulation parameters and obtained results. Figure 3.17 shows the power spectral density of the defined accelerometer setup and Figure 3.18 shows the step response of the loop with described parameters. Furthermore, Figure 3.19 shows the settling time tuning with the controller parameters its described setup.

Table 3.3: MATLAB Simulink results for decreased fingered SENSOR-1.

Mechanical Inputs					
Gap	2.3 μm	Anti-gap	7 μm	# fingers	100
Mechanical Outputs					
Mass	235 ng	Q factor	0.6505	Spring c.	56.28 N/m
Rest Cap.	4.11 pF	Cap. sensitivity	1.2 μF/m	Range	3.9 g
PID Parameters					
Proportional Gain	1	Integral Gain	1000		
Electrical Outputs					
VRW	9 $\mu g/\sqrt{Hz}$	Scale factor	131.5 mV/g	Settling time	2.2 ms

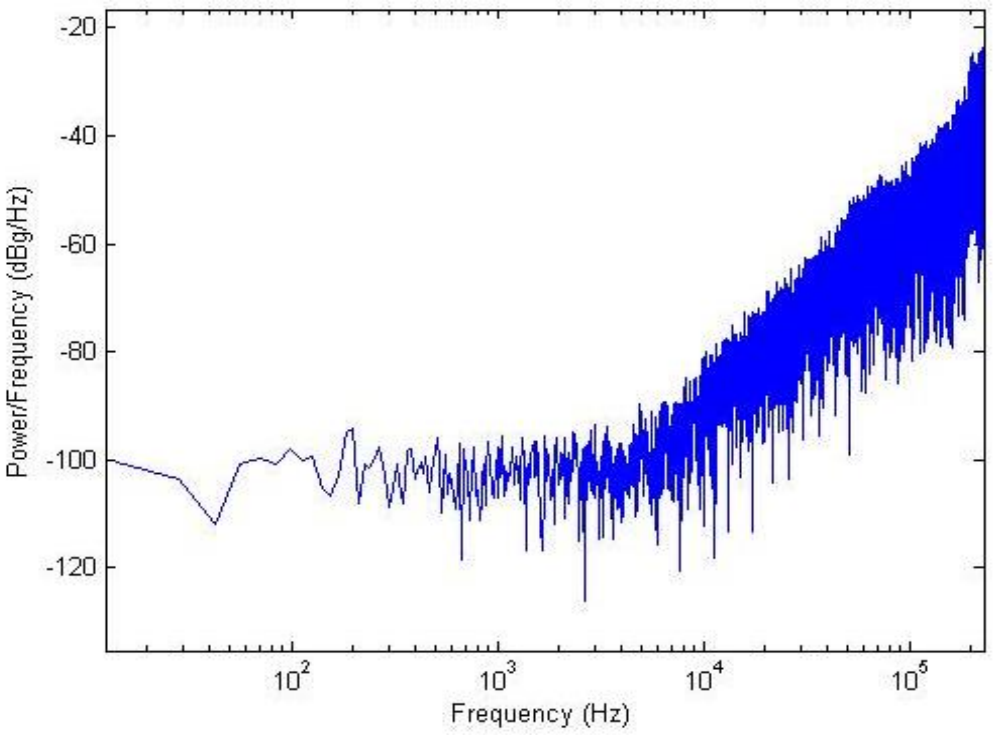


Figure 3.17: PSD for decreased fingered SENSOR-1 simulation.

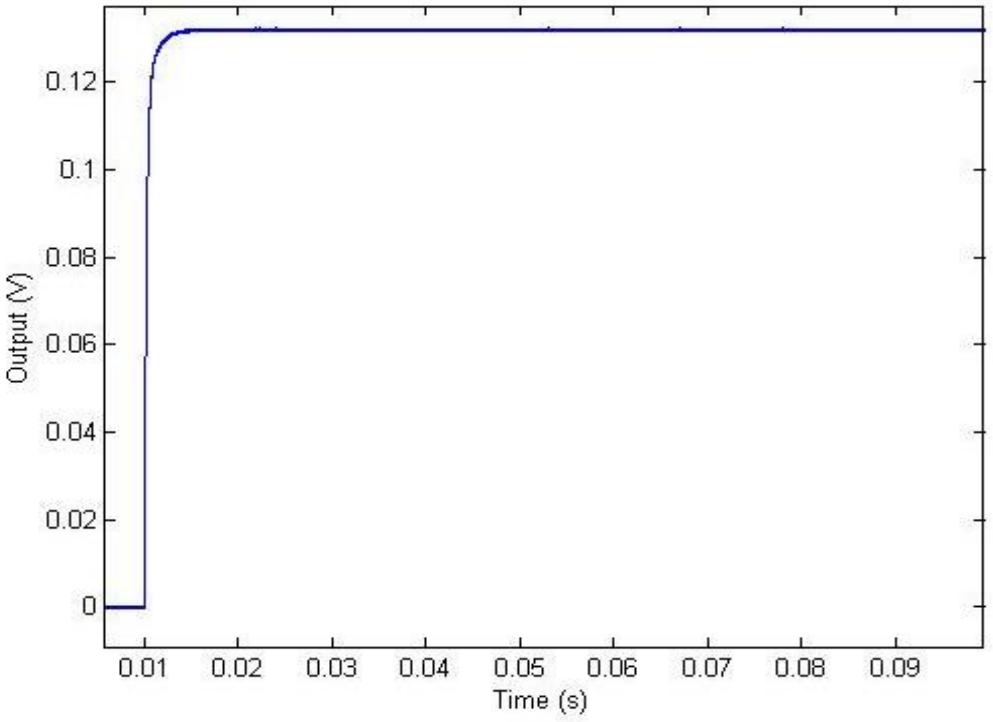


Figure 3.18: Step response for decreased fingered SENSOR-1 simulation.

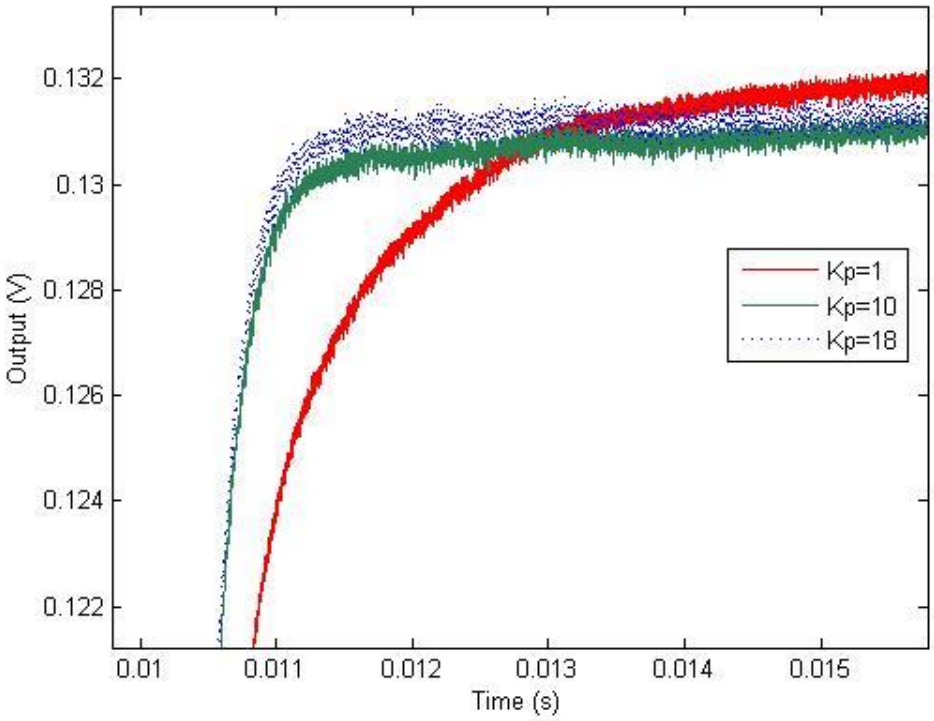


Figure 3.19: Step response dependency on proportional gain for decreased fingered SENSOR-1 simulation.

The decrease in the capacitive finger on the other side has a major effect on the defined mechanical outputs. Nearly all the mechanical outputs has dramatically decreased, limiting the range to only 3.9 g. These mechanical parameter changes operated with the same controller parameters as before yielded a stable operation with high scale factor of 0.1315 V/g. The observation on the PSD results in a noise floor of -100 dBg/Hz, which is close to the calculated velocity random walk. Last but not the least, the jump in the settling time of the system is related with the doubling of quality factor. For shortening the response time, the proportional gain of the controller can be increased. Referring Figure 3.19, the settling time can be decreased down to 1 millisecond with proportional gain of 10 and to 0.9 milliseconds with the proportional gain of 18 supplied by the controller.

In the third phase of alternative simulation conduction, a completely different accelerometer model was simulated. The major purpose was to observe the operation of the circuit for high range accelerometers. The sensor parameters used in this stage was labeled as the ones belonging to SENSOR-X. Table 3.4 summarizes SENSOR-X parameters and obtained results. Figure 3.20 shows the power spectral density of the defined accelerometer setup for SENSOR-X and Figure 3.21 shows the step response of the loop with described parameters.

Table 3.4: MATLAB Simulink results for SENSOR-X.

Mechanical Inputs					
Gap	1 μm	Anti-gap	4 μm	# fingers	424
Mechanical Outputs					
Mass	320 ng	Q factor	0.048	Spring c.	56.28 N/m
Rest Cap.	38 pF	Cap. sensitivity	28 μF/m	Range	67.65 g
PID Parameters					
Proportional Gain	1		Integral Gain	1000	
Electrical Outputs					
VRW	11.4 $\mu g/\sqrt{Hz}$	Scale factor	7.8 mV/g	Settling time	5 ms

From the results acquired, it can be concluded that even for a wide range sensor with completely different set of mechanical parameters such as quailty factor of 0.048, the system can operate properly without a need to re-arrange the controller parameters. Even though the settling time is higher and the response starts to change fashion, the system can still successfully decode on a small scale factor of 7.8 mV/g and deduce noise floor of -96 dBg/Hz.

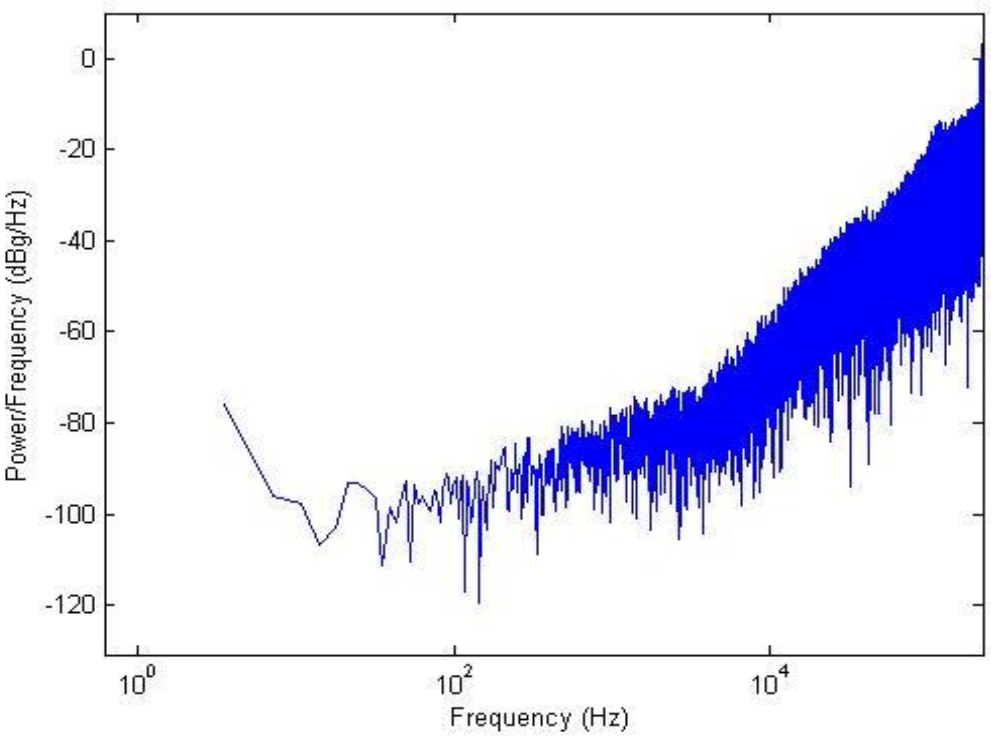


Figure 3.20: PSD for SENSOR-X simulation.

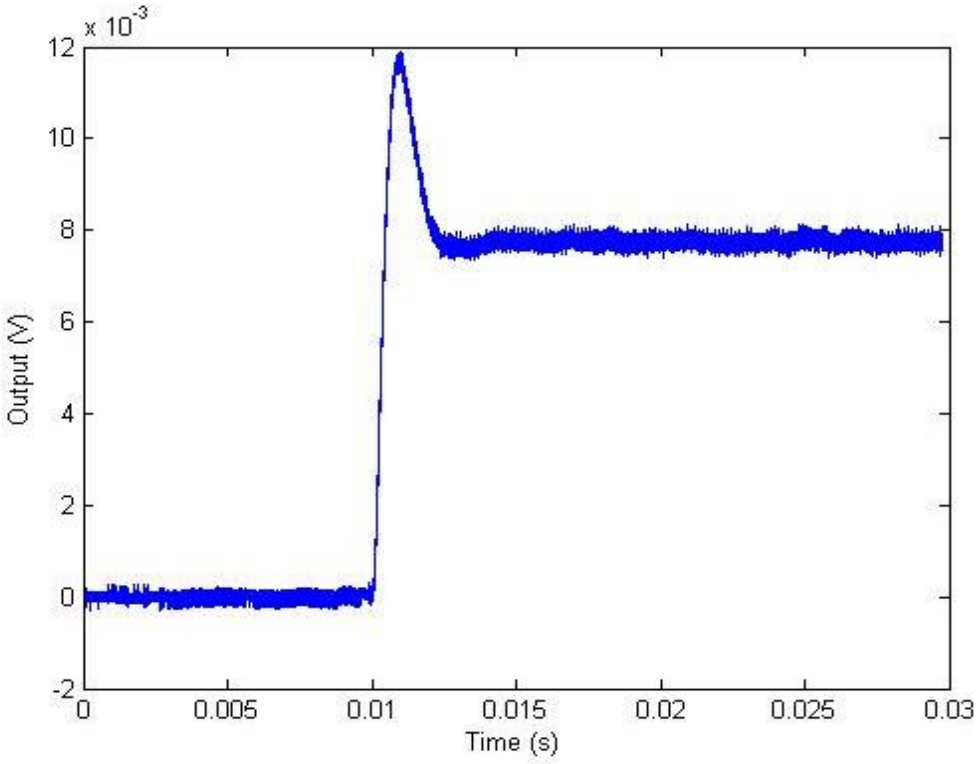


Figure 3.21: Step response for SENSOR-X simulation.

In the last phase of alternative simulation conduction, the focus was shifted to the accelerometer with a chance of real time testing. The accelerometer called MEMS-4 was simulated on the same simulation setup with changing any controller parameters. MEMS-4 accelerometer also had totally different structural parameters such as structure thickness, whereas all of them were inputted to a simulation. Table 3.5 summarizes the concerning simulation parameters of MEMS-4 and obtained results. Figure 3.22 shows the power spectral density of the defined accelerometer setup with MEMS-4 and Figure 3.23 shows the step response of the loop with described parameters.

Table 3.5: MATLAB Simulink results for MEMS-4.

Mechanical Inputs					
Gap	3 μm	Anti-gap	9 μm	# fingers	456
Mechanical Outputs					
Mass	71 ng	Q factor	0.49	Spring c.	18.4 N/m
Rest Cap.	6 pF	Cap. sensitivity	1.32 μF/m	Range	14.2 g
PID Parameters					
Proportional Gain	1		Integral Gain	1000	
Electrical Outputs					
VRW	8.5 $\mu g/\sqrt{Hz}$	Scale factor	23.6 mV/g	Settling time	$\leq$ 1ms

Application of the proposed circuit to a physical sensor with different mechanical parameters has resulted with good results as one can observe. An even smaller settling time than other simulations, together with moderate scale factor and appreciable noise of -100 dBg/Hz has been achieved.

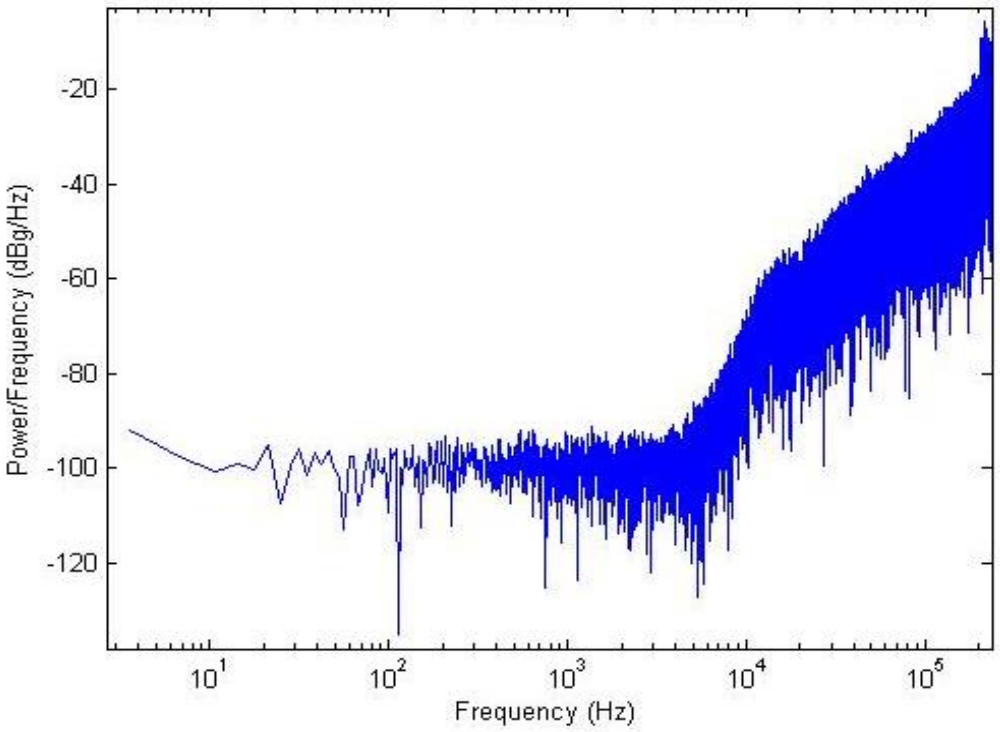


Figure 3.22: PSD for MEMS-4 simulation.

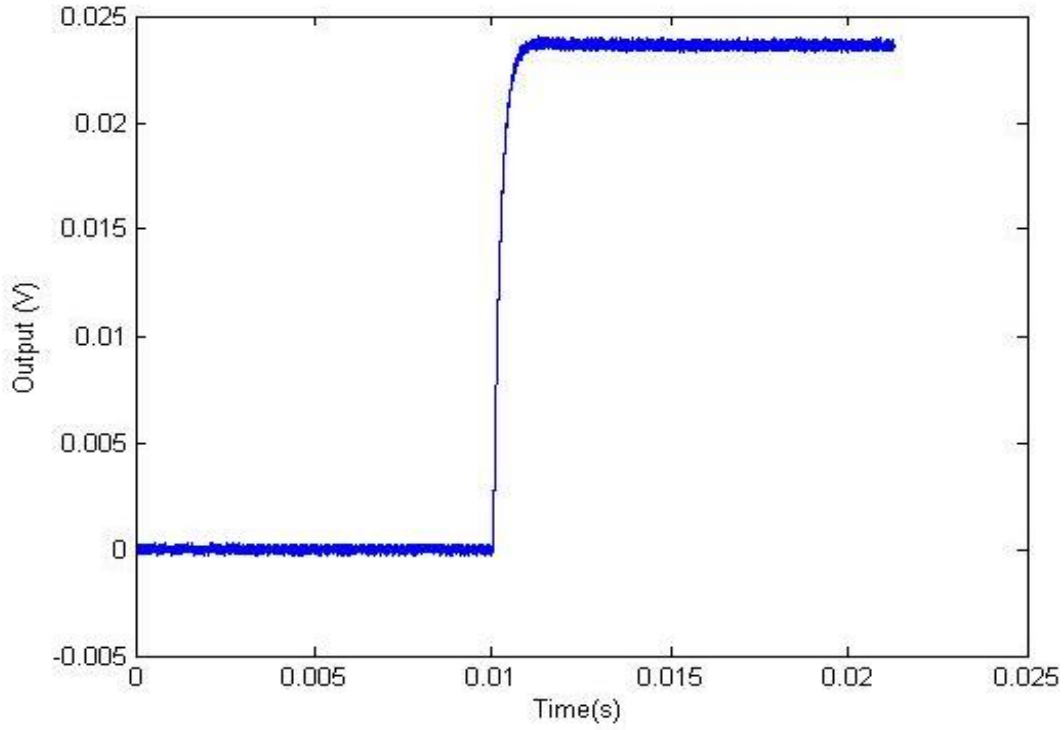


Figure 3.23: Step response for MEMS-4 simulation.

It should be noted that the complex nature of the design limits the parametric sweep in reference to mechanical output parameters. For instance, the extraction of rest capacitance range where the system is stable cannot be conducted independently because charge-integration method is not used. Therefore, we are not referencing the rest capacitance to any other capacitance which would induce a range. However if we were to do such a research, one would have to sweep according to the basic parameters of gap, anti-gap and etc.; which in terms would not yield a solid results because of many other parameters dependence on them. If we had any method to change the rest capacitance only though, the open loop gain would be affected only as shown in sub-section 3.2.1. To sum up, the correlation of the parameters limits the spectral research, relying on the operational check with the mechanical parameters of a specific device.

Further simulations are conducted on the system for estimation of the noise floor. Note that in these simulations the Brownian noise coming from the accelerometer and the electronic noise, which has relatively increased compared to previous system with the utilization of discrete components are included in the loop. Figure 3.24 shows the power spectral density for the whole system with all the noise sources included.

The noise floor of the system was found as 89 dBg/Hz, corresponding to 35.5 $\mu g/\sqrt{Hz}$ total noise. It is obvious that the system total noise has increased compared to the previous designs conducted at METU [27-28]. Table 3.6 shows the estimated noise sources of the system.

Note that 35.5 $\mu g/\sqrt{Hz}$ is expected noise value because of discrete components employment. Furthermore, ADC quantization noise is not properly shaped by the digital domain filters. The proportional and integral gains can be further adjusted for ADC quantization noise shaping and can be further decreased to 2 $\mu g/\sqrt{Hz}$.

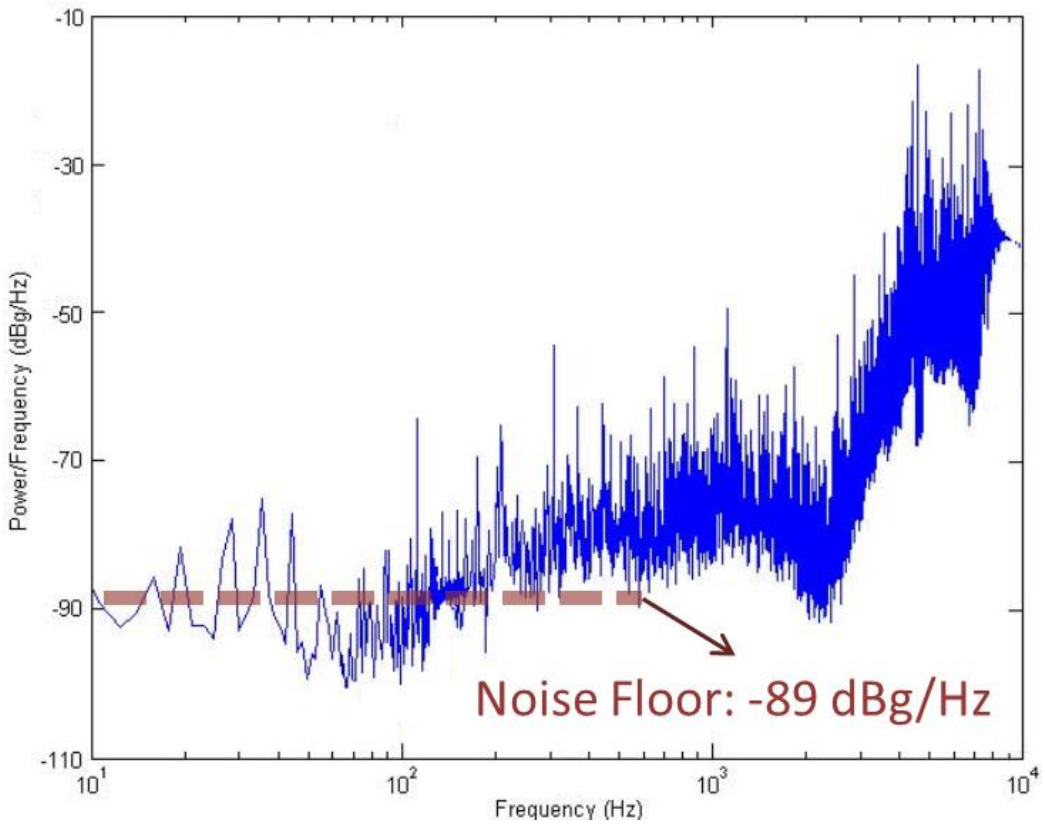


Figure 3.24: PSD for discrete front-end 5th order electromechanical ΣΔ modulator circuit simulated.

Table 3.6: Estimated noise distribution in the system.

Noise Source	***Estimated Value***
Brownian Noise	6.6 $\mu g/\sqrt{Hz}$
Electronic Noise	100 $\mu V/\sqrt{Hz}$
ΣΔ Quantization Noise	1 $\mu g/\sqrt{Hz}$
ADC Quantization Noise	7 $\mu g/\sqrt{Hz}$
Feedback Voltage Noise	1 $\mu V/\sqrt{Hz}$
Total Noise:	**35.5 $\boldsymbol{\mu g/\sqrt{Hz}}$**

3.3.1 Model Versatility Simulations

Even though the simulations conducted for certain fabricated accelerometers and the sensors with similar mechanical parameters show successful operation of the circuit, the scan of the mechanical parameter range to be operated by the circuit should be extracted for the complete verification of the versatile nature of the loop. For the defined purpose, minimum and maximum values of mechanical parameters, namely rest capacitance, capacitive sensitivity, quality factor, mass and spring constant was defined by interpreting the controllable operation of the circuit. The extreme values were thereafter meshed in a variable space, yielding 32 possible mechanical sensors with on the edge mechanical parameters. It is noteworthy that during the extraction of the extreme values all the mechanical parameters were assumed to be uncorrelated; in other words, the prospect of defined sensors fabrication with the modern manufacturing techniques was neglected. Table 3.7 shows 32 different accelerometer models to be simulated for the sake of versatility.

The simulation model extracted for the accelerometer readout loop in the previous sub-section was not altered in dependence to the change in the mechanical parameters. The only notable difference of the loop is that the electromechanical feedback voltage is multiplied with constant at the ratio of defined capacitive sensitivity to the calculated capacitive sensitivity. The described change should have been employed for the system feedback to settle correctly with the corresponding input.

As observed in Table 3.7, the maximum and minimum values of 5 different parameters for the accelerometers were distributed in a digital fashion. The rest capacitance was assigned as the most significant parameter in a wide range from 1 pico-farad to 10 nano-farads. Note that the defined range includes majority of the acceleration sensors to be reported in the literature [2-5].

Table 3.7: Mechanical parameters of 32 different accelerometer models.

Label	Capacitance (F)	Sensitivity (F/m)	Quality Factor	Mass (g)	Spring constant (N/m)
Sensor-1	10×10^{-13}	10×10^{-9}	0.01	10×10^{-9}	0
Sensor-2	10×10^{-13}	10×10^{-9}	0.01	10×10^{-9}	250
Sensor-3	10×10^{-13}	10×10^{-9}	0.01	10×10^{-7}	0
Sensor-4	10×10^{-13}	10×10^{-9}	0.01	10×10^{-7}	250
Sensor-5	10×10^{-13}	10×10^{-9}	1	10×10^{-9}	0
Sensor-6	10×10^{-13}	10×10^{-9}	1	10×10^{-9}	250
Sensor-7	10×10^{-13}	10×10^{-9}	1	10×10^{-7}	0
Sensor-8	10×10^{-13}	10×10^{-9}	1	10×10^{-7}	250
Sensor-9	10×10^{-13}	10×10^{-7}	0.01	10×10^{-9}	0
Sensor-10	10×10^{-13}	10×10^{-7}	0.01	10×10^{-9}	250
Sensor-11	10×10^{-13}	10×10^{-7}	0.01	10×10^{-7}	0
Sensor-12	10×10^{-13}	10×10^{-7}	0.01	10×10^{-7}	250
Sensor-13	10×10^{-13}	10×10^{-7}	1	10×10^{-9}	0
Sensor-14	10×10^{-13}	10×10^{-7}	1	10×10^{-9}	250
Sensor-15	10×10^{-13}	10×10^{-7}	1	10×10^{-7}	0
Sensor-16	10×10^{-13}	10×10^{-7}	1	10×10^{-7}	250
Sensor-17	10×10^{-9}	10×10^{-9}	0.01	10×10^{-9}	0
Sensor-18	10×10^{-9}	10×10^{-9}	0.01	10×10^{-9}	250
Sensor-19	10×10^{-9}	10×10^{-9}	0.01	10×10^{-7}	0
Sensor-20	10×10^{-9}	10×10^{-9}	0.01	10×10^{-7}	250
Sensor-21	10×10^{-9}	10×10^{-9}	1	10×10^{-9}	0
Sensor-22	10×10^{-9}	10×10^{-9}	1	10×10^{-9}	250
Sensor-23	10×10^{-9}	10×10^{-9}	1	10×10^{-7}	0
Sensor-24	10×10^{-9}	10×10^{-9}	1	10×10^{-7}	250
Sensor-25	10×10^{-9}	10×10^{-7}	0.01	10×10^{-9}	0
Sensor-26	10×10^{-9}	10×10^{-7}	0.01	10×10^{-9}	250
Sensor-27	10×10^{-9}	10×10^{-7}	0.01	10×10^{-7}	0
Sensor-28	10×10^{-9}	10×10^{-7}	0.01	10×10^{-7}	250
Sensor-29	10×10^{-9}	10×10^{-7}	1	10×10^{-9}	0
Sensor-30	10×10^{-9}	10×10^{-7}	1	10×10^{-9}	250
Sensor-31	10×10^{-9}	10×10^{-7}	1	10×10^{-7}	0
Sensor-32	10×10^{-9}	10×10^{-7}	1	10×10^{-7}	250

The second bordered parameter was the capacitive sensitivity of the accelerometer, limited between 10 nano-farads per meter and 1 micro-farad per meter. Several reasons such as direct dependence of the electromechanical feedback on the capacitive sensitivity, unnatural uncorrelated parametric sweep and the will of simulation conduction without notable changes on the model are causing the deficient range defined for the capacitive sensitivity. The quality factor of the sensor, which would only affect the damping as the other two parameters defining it are set to a minimum or maximum, was assigned was assigned in a wide scope, ranging from 0.01 to 1. The fourth parameter limited for the observation of the system bounds is the mass. The limits for the mass were defined on the fact that the sensor is a micromechanical one, from 10 nano-grams to 1 microgram. Finally, the least significant parameter was defined as spring constant, having a huge range lasting from 0 to 250 newtons per meter.

On the base of the extracted space for the accelerometer structures, the closed-loop accelerometer readout loop simulations were conducted. It should be pointed out that the main emphasis of the loop was taken as the stability; in other words, the loop was aimed to be operated with the altered mechanical parameters of the accelerometer. The parameters swept for the stable operation of the loop were the integral and proportional gain of the PI controller enrolled as a single order integrator. Another parameter that could be swept is the sigma-delta gain; however, there was no need as its gain has a short range. The sigma-delta gain employed by second-order integrators was calculated as 0.67, and was always kept constant throughout the simulations.

During the conduction of the simulations, the output measurements referenced for the qualification of the loop were chosen as scale factor, measurement range, settling time, corner frequency and velocity random walk. The scale factor and the settling time of the system according to various mechanical parameters were mined from the step response. For some conditions where the scale factor was so high that the observable output saturated, a more moderate input was applied, and the proportionality vision was utilized for the forecast of the scale factor. On the

other hand, the operation range was calculated with a simple equation including the feedback voltage, mass and sensitivity. The bandwidth of the system was simply observed through the frequency where the scale factor was decreased 3 dB. Last but not the least, the velocity random walk was calculated by the use of power spectrum. The match of the result was certified also using the Allan Variance technique. Table 3.8 shows the simulation results obtained for controller parameter tuned 32 different accelerometer models.

The statement for the tuning of the proportional and integral gain, aiming the stable operation of the loop, cannot be cited for every single condition. The main reason is the correlation that altered parameters have in reference to the loop. However, main patterns can be highlighted in adjustment of the PI parameters. The most significant reference is the open-loop gain, which is affected by several parameters. If treated in an uncorrelated fashion, spring constant does not affect the open loop gain. However, when the spring constant is raised while the mass of the sensor is at its minimum, the proportional gain needs to be raised in several occasions. The main reason for the gain boost is the amplification in the first-order term of the second-order filter, namely the accelerometer, which is spring constant divided by the mass, and it needs to be tracked with DC gain. As it can be imposed from the previous statement, this type change does not happen in the models where the mass is at its maximum, except it is affected by other parameters. To wrap up the mass effect on the PI parameters; when the mass of the sensor is raised to its maximum, a higher gain boost is needed for the electromechanical feedback to counteract big body. Furthermore, as the increase in the mass also decreases the dynamic response of the loop, a more moderate integral gain is enough to keep the circuit stable. The third parameter, namely quality factor sweep does not require notable change in the gain parameters. Nevertheless, more responsive nature of a high quality factor accelerometer allows intensification of the proportional gain, which in terms decreases the settling time of the circuit

Table 3.8: Simulation results for the loop with various accelerometer models.

Label	PG	IG	S.F. (mV/g)	Range (g)	Settling time (ms)	Band (Hz)	VRW (µg/√Hz)
Sensor-1	10	10K	8.65	0.7645	3.5	1300	200
Sensor-2	10	10K	8.2	0.7645	28	40	1000
Sensor-3	150	1K	870	0.0076	4	800	5.6
Sensor-4	150	1K	627	0.0076	12	90	141
Sensor-5	50	10K	8.5	0.7645	1.27	1000	280
Sensor-6	60	10K	4.2	0.7645	1.7	750	5000
Sensor-7	150	1K	860.4	0.0076	4.4	850	4
Sensor-8	150	1K	610	0.0076	1.5	780	66
Sensor-9	1	10K	23.2	76.45	1.2	800	7.07
Sensor-10	5	10K	23.4	76.45	1.35	500	112
Sensor-11	40	1K	2300	0.7645	1.5	780	8.91
Sensor-12	40	1K	2100	0.7645	2.5	420	12.5
Sensor-13	2	10K	23.38	76.45	1	770	8
Sensor-14	2	10K	23.5	76.45	1.7	430	44.66
Sensor-15	40	1K	2310	0.7645	1.3	760	8
Sensor-16	40	1K	2270	0.7645	1.8	800	5
Sensor-17	500K	1M	9	0.7645	1.23	720	7.94
Sensor-18	600K	1M	4.68	0.7645	1.5	400	10
Sensor-19	1.5M	0.5M	860	0.0076	2.5	830	6.3
Sensor-20	1.5M	0.5M	605	0.0076	10	100	100
Sensor-21	750K	100K	8.8	0.7645	1	720	6.3
Sensor-22	600K	1M	4.24	0.7645	1.15	700	10
Sensor-23	2M	1M	865.2	0.0076	2	720	8
Sensor-24	2M	1M	646.7	0.0076	1.17	750	11.2
Sensor-25	10K	1M	23.67	76.45	1	800	9
Sensor-26	80K	1M	19.3	76.45	1.4	630	10
Sensor-27	500K	100K	2320	0.7645	1.3	740	5.95
Sensor-28	500K	100K	2238	0.7645	1.9	480	17.7
Sensor-29	20K	100K	23.5	76.45	0.9	810	7.94
Sensor-30	15K	100K	11.43	76.45	1.25	650	11.2
Sensor-31	500K	100K	2317	0.7645	1.1	750	10
Sensor-32	500K	100K	2247	0.7645	1.25	750	5.62

A major boost in the capacitive sensitivity of the accelerometer increases the open-loop DC gain, because the gain of the front-end is directly proportional to the capacitive sensitivity as shown in Equation 3.5. To account for the sensitivity increase, the proportional gain of the PI should be decreased. Note that if the electromechanical feedback is forced to generate a voltage accordingly, a small decrease would be enough to keep up the loop stable. Last but not the least, the most significant parameter affecting the loop is the rest capacitance of the accelerometer. Referencing Equation 3.5, the rest capacitance of the inversely proportional with the open-loop gain of the loop, and wide range of sweep forces the designer to increase the proportional gain of the controller to encounter for it. The integral gain is also raised in a moderate fashion to keep up with the pace and keep the loop running.

When the correlation between the parameters is encountered for, the system operation shown in Table 3.8 collapses. The reason for some of the previously described tuning features not to match is caused by the insuppressible correlation inside the loop.

After the observation of the stable operation of the loop with the tuned controller parameters, the uncorrelated circuit was qualified. It is clear that as the circuit provides a quantized output, a low-pass filter was employed for the extraction of several parameters. The low-pass filter was designed to have a unity gain and wide bandwidth for output not to be affected by it. Referring to Table 3.8, it is obvious that some parametric changes do not affect the observed output. For example, increase spring constant from 0 to 250 does not change the operation range of the accelerometer, which is independently controlled. On the other hand, described change does drastically affect the bandwidth of accelerometer loop, which has all its parameters at minimum. The increase in the spring constant is reflected as a large integral term to the accelerometer, which in absence of controllable features increases the response time. Furthermore, having a large spring constant with small mass forces the system to a high noise state. These features are seen in several simulation couples, but the most significant

bandwidth disturbance is observed in the first two couple of sensors, and the enormous noise increase is observed in transactions from Sensor-1 to Sensor-2 and from Sensor-5 to Sensor-6. Accordingly, Figure 3.25 shows the power spectral density for Sensor-2.

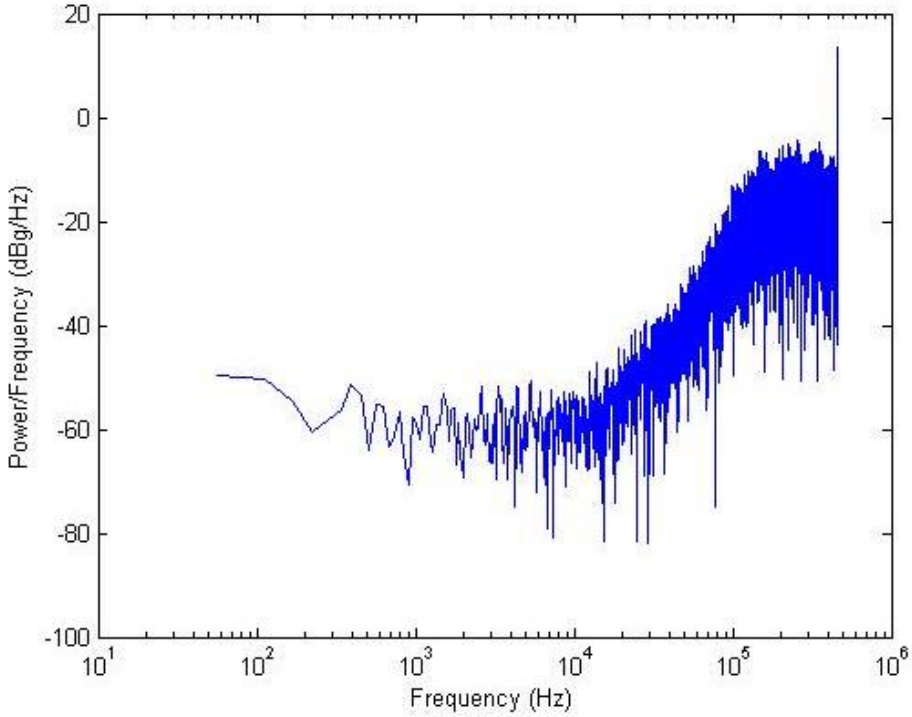


Figure 3.25: Power spectral density for Sensor-2.

In transaction between the first two couple of sensors, where the mass of the accelerometer has been pulled from minimum to maximum, the scale factor boost can be observed. Such an increase in the scale factor, which ultimately leads to a decrease in the operation range, illustrates the trade-off between the scale factor and the operation range. Taking the scale factor conversion further, the sensitivity can also be pulled from minimum to the maximum value to adopt additional boost of the scale factor. The sensors 11, 12, 15, 16, 27, 28, 31 and 32, having such architecture, respond to a single g application with an average voltage of 2.2. Even with their limited operation range, such design has shown the best noise characteristics. Figure 3.26 shows the power spectral density for Sensor-32.

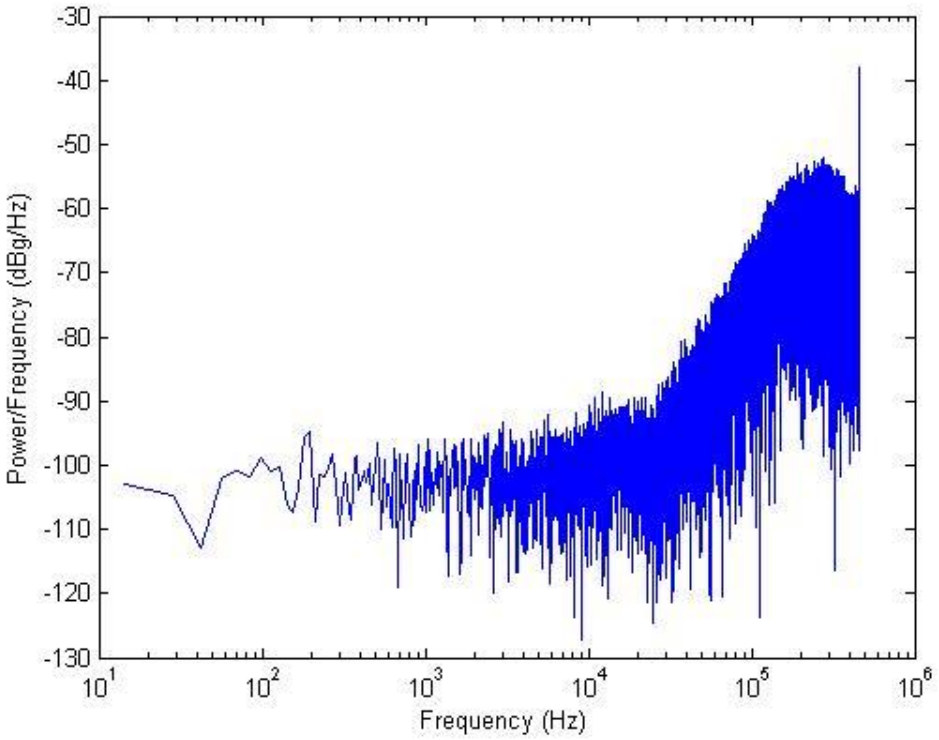
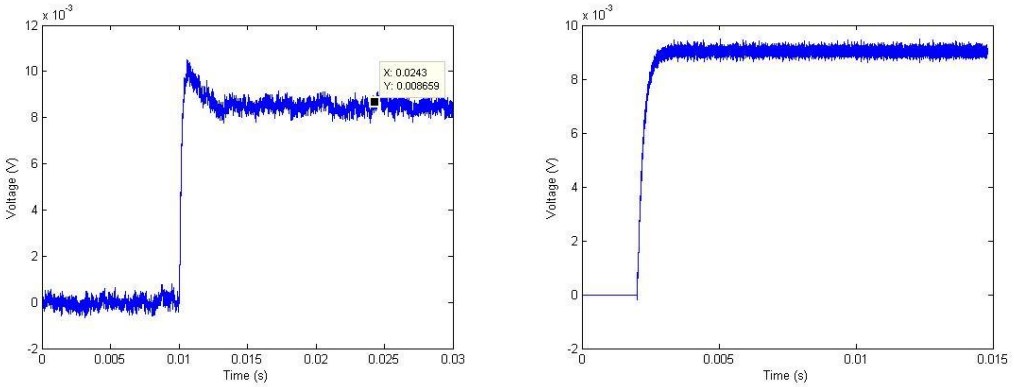


Figure 3.26: Power spectral density for Sensor-32.

The quality factor sweep in the simulations has also affected the output characteristics. In the first phase of the simulations, where the minimum values were mostly interpreted, the quality factor change from minimum to maximum causes a massive increase in the noise density, because of the miscues in the loop. However, it's positive effect on the response time increase system bandwidth, and even suppresses the huge bandwidth loss, observed when the spring constant is pulled up. In the second phase of the simulations, the quality factor does minor effect on the noise; on the other hand, its increase supplies the system with extra 650 Hz of bandwidth as observed in transaction from Sensor-20 to Sensor-24.

Finally, the reflection of the rest capacitance sweep between its defined maximum and minimum can also be observed through conducted simulation. Referencing Sensor-1 and Sensor-17, it can be clearly seen that the increase of rest capacitance leads to reduced settling time, wider bandwidth and suppressed

noise floor. Even though such an application should be supplied with high gains from the controller, a more stable operation makes it worth it. It should note that as the parametric space approaches its maximum, because of the decrease in affection different parameter impose on the circuit, the circuit becomes more stable and operates with the desired output characteristics. Figure 3.27 shows the step-response for Sensor-1 and Sensor-17.



(a) (b)

Figure 3.27: Step-response illustration for (a) Sensor-1 and (b) Sensor-17.

CHAPTER 4

TEST SETUP AND RESULTS

The logic behind the quote ‘To have a great idea, have lots of them’ by great thinker Thomas Edison is in fact a major reference proving that theory worth nothing until it is suited for some application. As in every related field, a theory defined in terms of equation and unknown parameters come to be familiar after initial testing, and an understanding leading to replacement of unknowns with real life components ease the deal of successful application. On the other hand, application specific may require the use of an alternative route, meaning that few alterations on a well-established design and possible explanation with few initial tests may yield in an innovative theory. This chapter illustrates the procedure of preparing the right setup for the according tests, the acquired results in open-loop system and the struggles in achievement of closed-loop system. Finally the chapter is finalized with the discussion about the results and their prospective.

4.1 Open-Loop Tests

4.1.1 Test Setup

The validation of the any proposed engineering theory is dependent on the test results, which is acquired through the use of a test setup. The pre-said

automatically employs a major importance on test setup, and its dedicated design with care is crucial for successful results.

One of the major differences of the proposed design compared to the previous designed circuits in METU-MEMS facilities was the continuous-time voltage mode sense-out of the acceleration. Referring to sub-section 3.2.1 where it is described in details; while triggered with opposite voltage through different electrodes after being grounded totally, the accelerometer should be able to generate a voltage at the proof mass electrode reflecting the displacement according to the acceleration. Figure 4.1 shows the accelerometer connected with the pre-amplifier for voltage mode readout. Figure 4.2 shows the package prepared with the containing components. It should be noted that the package shown in Figure 4.2 was prepared with 16-pin package and glass substrate that was previously prepared by gyroscope group. Similar operational amplifier circuit comprising glass substrate was altered in few ways by laser cuts and connections through conductive epoxy and ball bonding. Conducted changes enabled pre-designed glass substrate use for defined testing purposes.

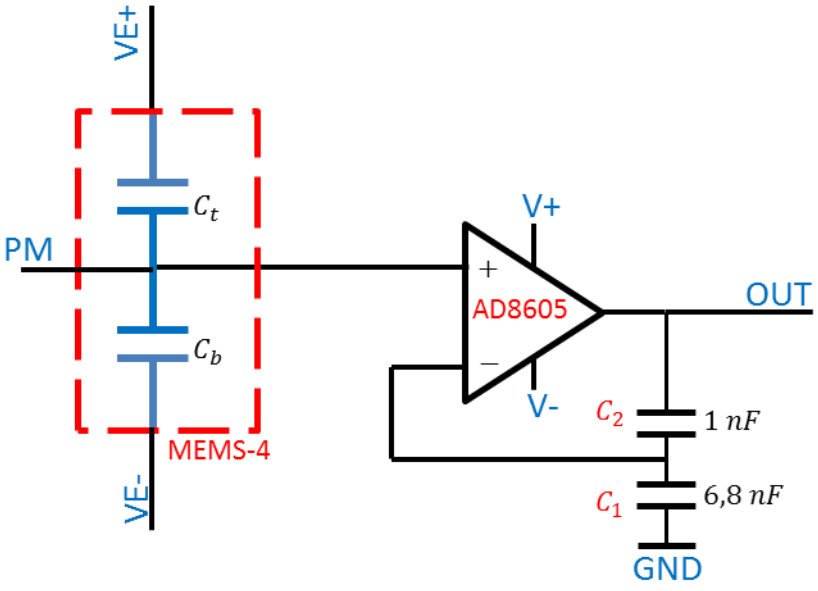


Figure 4.1: Circuit schematic of voltage-mode sensing test.

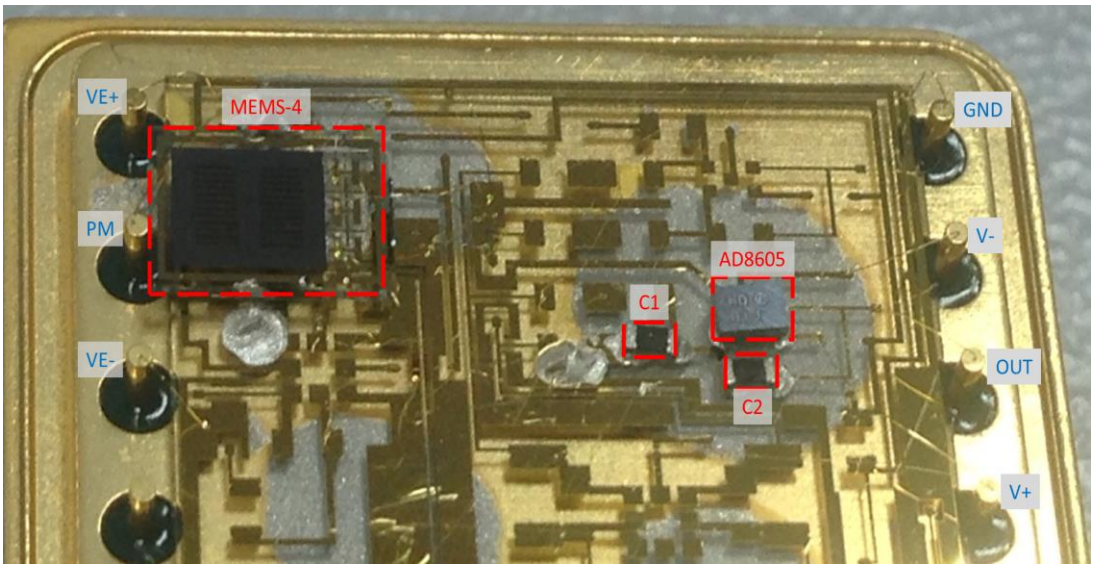


Figure 4.2: Package prepared for voltage-mode acceleration sensing test.

Last but not the least; the test setup would not be complete without proper power supplying units. For the defined purpose, firstly all the electrodes including the proof mass of the accelerometer was grounded in parallel with short-circuiting C1 and C2 capacitors for charge flushing. Afterwards, the top electrode was excited to 3.3V and the bottom electrode to -3.3V. In this condition, if there were a displacement present in the accelerometer, a sudden burst of voltage at the proof mass electrode would be observed. Therefore, the accelerometer was tilted 90 degrees for proof mass to deflect and enable observation of an observable voltage at proof mass node.

For the operation amplifier supply, a maximum saturation voltage of 3.3V was directly applied. The negative supply node of the amplifier was grounded. Note that it is an obstacle in observing negative voltages under negative acceleration, which is not a problem as negative acceleration is not the issue in this step.

4.1.2 Results and Comments

For verification of the acquired results in the open-loop test, two packages including the same components and MEMS-4 were prepared, labelled as *Pack_A* and *Pack_B*. Some prerequisite test for checking out correct connections were conducted with success. Figure 4.3 shows the results obtained for voltage-mode sensing tests together with the applied signals. Referring the figure, it can be observed that as soon as positive and negative electrodes are excited with +3.3V and -3.3V respectively, the proof mass generates a voltage, which is further amplified and outputted by the operational amplifier. On the other hand, referring to Equation 3.5 it can be concluded that the accelerometer would generate approximately 70 mV at proof mass with reasonable deflection of nearly 100nm under 1g acceleration. With the resulting voltage of the proof mass fetched to the pre-amplifier with the moderate gain of 7.8, an output voltage of 0.54V can be observed under perfect conditions.

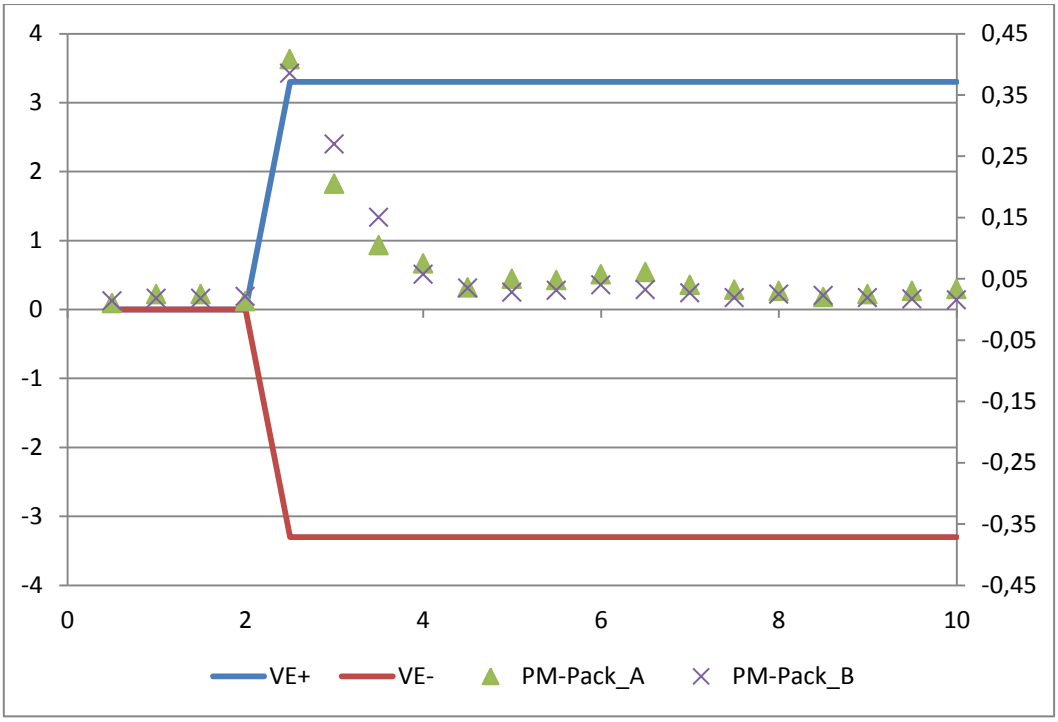


Figure 4.3: Open-loop voltage-mode front-end circuit test results.

There is a certain difference between the expected value and the measured one, mainly caused by the parasitic connections and the tolerance of the components. Referring to Equation 3.6 which highlights the major degradation of the proof mass voltage with the increase in the parasitic capacitance, it can be concluded that such a voltage difference in this parasitic rich test setup is very realistic.

It can also be concluded that in terms of time, the accelerometer generates the full range of the proof mass voltage in nearly 0.5 milliseconds in open-loop. After the voltage is generated by the dynamic current flowing within the rise time of the triggering signals, the accelerometer cannot hold the accumulated charges. As the middle electrode of the accelerometer is read continuous time and even having contact with the amplifier in sense phase, is the main reason for charge leakage.

4.2 Closed-Loop Tests

4.2.1 Test Setup

Some sort of verification of the theory with initial tests in open-loop raises further interest in conduction of the closed-loop tests and fully verification. For the conduction of the closed-loop analysis, the initial package prepared needed to be modified. Keeping the line with the theory, connection between a moderate ADC and the output of the front-end is required. The output of the ADC with I^2C protocol is fetched into the FPGA, where the digital signal is processed as proposed. Figure 4.4 shows the package prepared for the closed-loop test, whereas Figure 4.5 shows the circuit of it.

The extra added component to the package is the ADC, namely ADS1013. Note that even though the circuit was proposed to be conducted on a PCB, a design on a glass substrate inside a multi-connectional package allowed the alteration that would be present in the design. With the solid verification of the results, the whole system may be transferred into a PCB with defined discrete components.

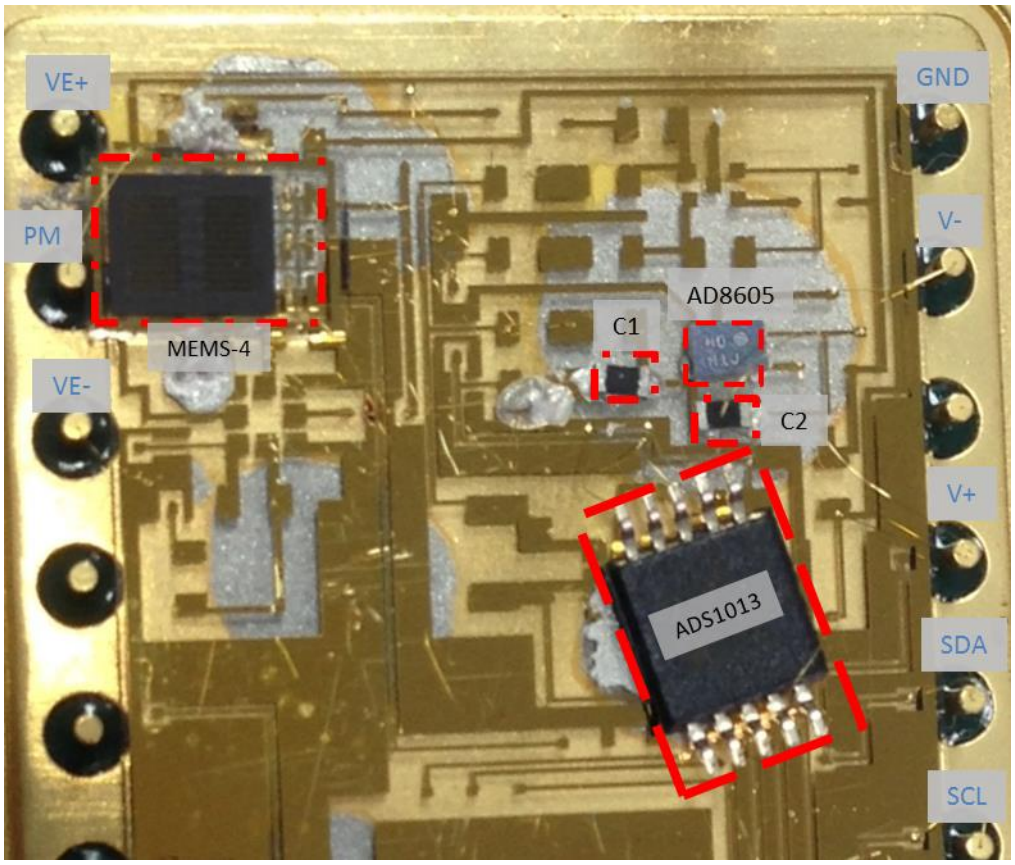


Figure 4.4: Package prepared for closed-loop acceleration sensing tests.

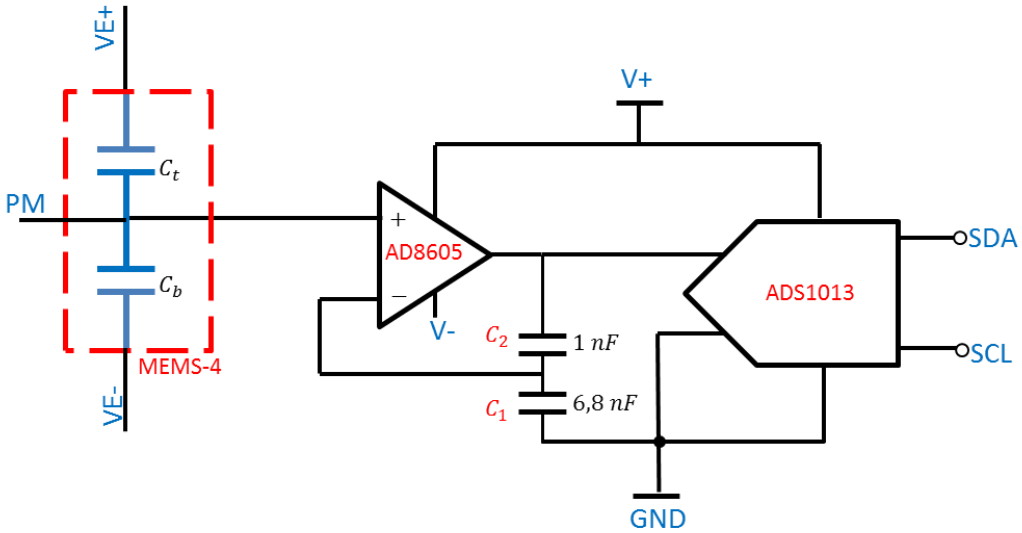


Figure 4.5: Circuit schematic of the analog front-end for closed-loop tests.

For the successful conduction of the closed-loop tests, a power supply output with an uncontrolled noise must be filtered out. For the purpose, a regulating PCB including LT1762 regulator was utilized. The regulated voltages were inputted into a connection PCB, where the contact with the accelerometer package was enabled. The output coming from the I^2C interface of the analog-to-digital converter inside the package is fed to the FPGA, to be processed in the connected PC. Software was prepared for intake and triple integration of the signal. The resulting pulse density modulated digital signal is afterwards fetched to the accelerometer electrodes with the direct connection between the FPGA and the connection PCB. Figure 4.6 shows the described test setup with the entire component labelled. Note that with the settlement of all the components, the PCB's can be jammed up in a compact one and directly connected to the FPGA.

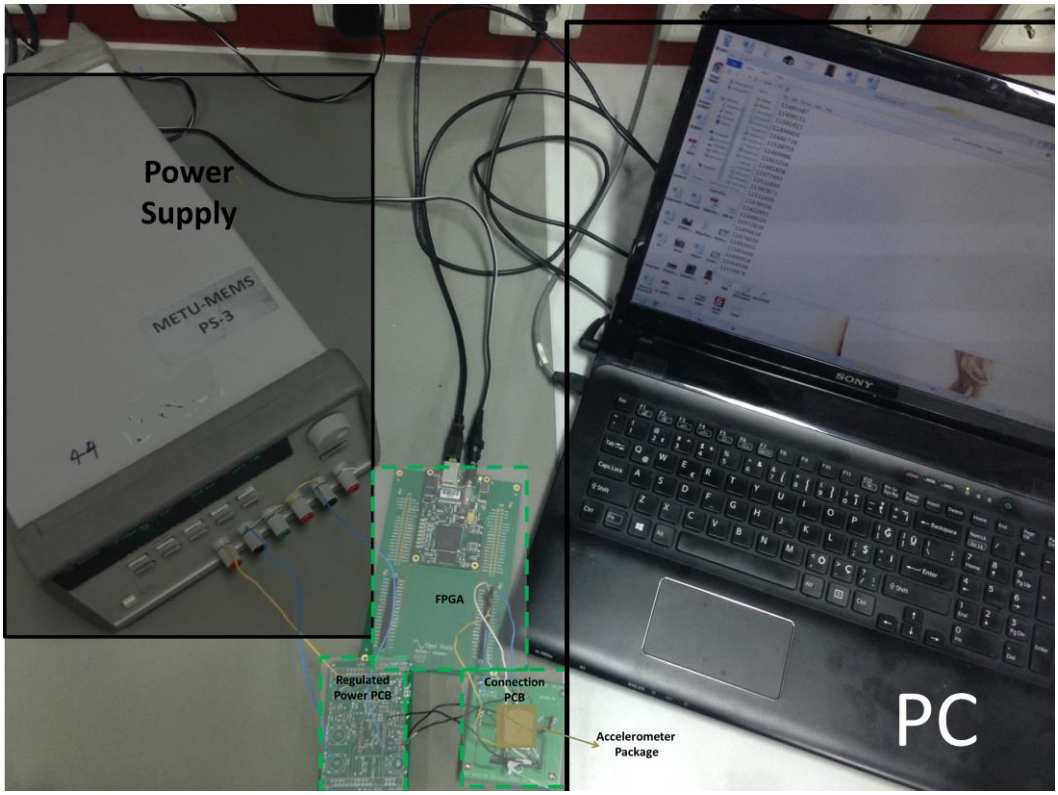


Figure 4.6: Versatile accelerometer test setup.

4.2.2 Results and Comments

Even though the test setup was effectively built, the test conducted in the closed-loop did not resume the trend. To certify, at the PDM output a signal proportional to the applied acceleration could not be read. With that said, a feedback voltage counteracting the accelerometer could not be achieved and the accelerometer would always saturate the output at applied accelerations. Several reasons could be encountering such an issue due to the complexity of the loop and the reliability of the test setup. It should be also noted that the 3300 sample rate of the bonded analog-to-digital converter inside the package is a huge obstacle in increasing the digital frequency to the desired ones. Such an issue may be the source for digital correlation in the designed software, and reason for the collapse of the system. Nevertheless, on some trials under zero acceleration some data could be scanned. It is noteworthy that the observation of these data does not verify the rightful operation of the circuit. The results are not reliable, but nevertheless worth discussion. Assuming a moderate scale factor, the acquired results can be used to sketch an Allan variance graph for deduction of the potential noise floor. Figure 4.7 shows the possible AlaVar curve.

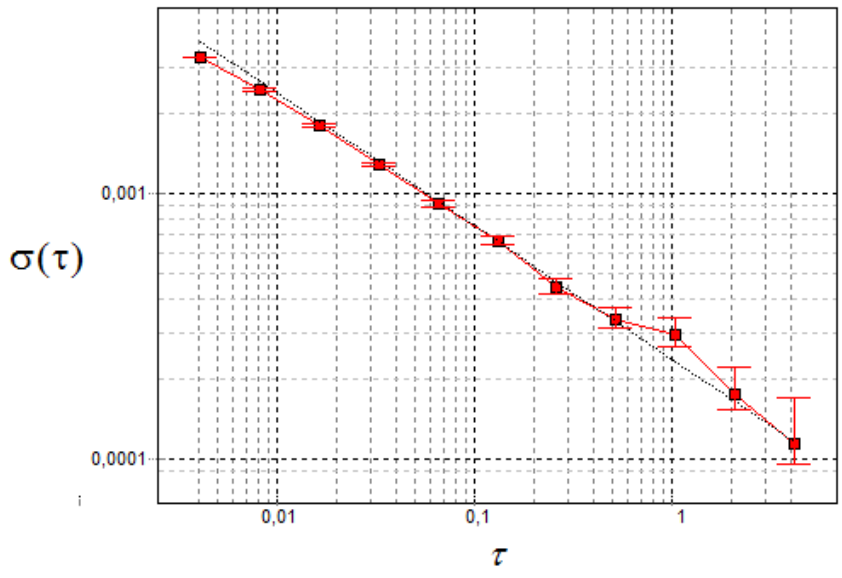


Figure 4.7: AlaVar curve for the acquired results of MEMS-4 with assumed scale factor.

Referring Figure 4.7, a velocity random walk of 236 μg/√Hz can be concluded. This amount of random walk leads to approximately 330 μg/√Hz of noise floor, which is much diverged from the proposed one. Scale factor may be assumed to be 10 times larger, which would lead to the proposed result. However, that quantity of the scale factor, nearly half of the originally seen bitstream would limit the system in terms of dynamic range, which is certainly something we do not desire to exist. Furthermore, many problems can be caused by the complex and unreliable nature of the connections through single cables and unsealed ungrounded interface. The closed loop test setup should be further optimized and a single PCB should be produced including all the interfaces and voltage generation. An optimum result can be achieved in that manner.

We also observe that the Alavar curve observed in Figure 4.7 does not entirely show the characteristics of an accelerometer loop, lacking a minimum point to deduce the bias instability and several other slopes for other noise source conclusion. This also questions the reliability of the result.

4.3 Feasibility of the Proposed Loop

The deficiency for adequate test results showing the desired operation of the circuit requires a proper explanation to the matter. Even though the simulation results have proven the robustness property of the circuit, some extra discussion should be presented about the applicability. Firstly, for the discrete component application of the circuit, a well-designed high voltage switching control unit should be employed. The fumble of contact switching between the accelerometer and the front-end amplifier leads the accelerometer to saturate. The contact point draws further attention for the operation with high sensitive sensors. Furthermore, the choice of the discrete components is also a crucial step for the architecture operation. The operational amplifier of the pre-amplifier should have negligible input capacitance, and its bandwidth should be corresponding with the desired

operation frequency. Consequently, the analog-to-digital converter bandwidth should also be wide enough to operate with the desired frequency.

Zooming out of the package, the post important reference for readout of low noise is the PCB. A single PCB including the power regulators, FPGA card and operating unit should be designed with grounded substrate, in order to restrict the noise coupling. A carefully designed and component mounted PCB can be used long-time, whereas the readout of every accelerometer sensor could be conducted by only placing package including the bonded sensors.

Last but not the least, the interface with the computer and the software should be carefully designed for high performances. Modern data acquisition devices can be used through defined interfaces, meshed with the software to supply the system with the controller and the sigma-delta integrators.

CHAPTER 5

SUMMARY AND CONCLUSIONS

On the scope of the conducted research, a simplified design of highly versatile circuit for characterization of capacitive inertial sensors is focused on. The design would enable readout of accelerometer with various mechanical parameters by just packaging the accelerometer alone and making the corresponding connection to the front-end. The summary of the work can be given as follows:

1. With the possession of simply versatile front-end, the designed readout circuit can be matched with wide range of sensors, intended form sub-g to 100g measurements. Proposed modulator circuit can considerably decrease the sensitivity to manufacturing tolerance. It perfectly suits the market requirements of batch manufacturing facilities.
2. The front-end of the circuit is designed with discrete components. No CMOS process is required, which suppresses the need for packaging and glass substrate design, intended for solid matching between the mechanical sensor and the CMOS circuitry.
3. Implementation of non-mechanical integrators of the loop in digital domain presents the adaptive control logic to the system. Simultaneously

controlled digital loop parameters can be used to save the system form stability crashing, which is a moderate problem in high-order circuits.

4. The complex mixed-signal structure is simplified by the use of linear techniques to build a representative model in a simulation environment. The operation the circuit in MATLAB Simulink platform is confirmed, and corresponding analyses are conducted thereby
5. Linearized model is furthermore utilized for detailed emphasis of the noise shaping concept. By the use of linear techniques, double quantization noise shaping is accomplished as high-pass and band-pass characteristics for ΣΔ and ADC quantization noises respectively.
6. The total noise of the system is calculated as 35.5 μg/√Hz, mainly contributed by the ADC quantization noise and the electronic noise caused by the employment of discrete IC components.

To conclude, design of a versatile electro-mechanical ΣΔ modulator goal was achieved in the research. The relatively high noise in the system can be suppressed further by the implementation of Correlated-Double Sampling (CDS) in PCB and exact forecasting the digital filter parameters in the FPGA. In fact, the non-mechanical noise of the system can be suppressed down to sub-μg levels, outperforming classical macro electromechanical quartz sensor in cost, robustness and noise.

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