DESIGN OF HIGH POWER WAVEGUIDE LIMITER

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ABSTRACT

DESIGN OF HIGH POWER WAVEGUIDE LIMITER

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Microwave limiters are protector structures. Microwave limiters protect the receiver circuits from high power microwave signals. Receiver circuits of radar systems are able to process the signals with low level amplitude. This situation results in usage of very sensitive circuit blocks. These sensitive circuit blocks, such as LNAs, are protected from high power signals by limiters. The causes of the undesired microwave signals with high level amplitude can be transmitter to receiver leakage and high power microwave short pulses coming from outside as an enemy attack. Transmitter leakages are predictable threats because transmitted signal timing is known. However threats from outside is unpredictable because the time of threat cannot be known. Outside threats can cause problem in the radar system at any time. In order to protect receiver channel of radar system, low response time high power microwave limiter must be used. In this study, two critical points are aimed. The limiter, which can handle the signals with kW power levels, and which have low response time is aimed. Two different single stage waveguide limiters, whose operating frequency bands are 9.4-10 GHz, are designed with two different high power pin diodes. Linear/Nonlinear measurements of waveguide limiters are performed. Then these two single stage limiters are connected in cascade and the resulting two stage waveguide limiter is measured. In order to increase the sensitivity and the response speed of the waveguide limiter, the waveguide detector is designed

with the Schottky diode. The limiters are measured with the WG detector. Circuit designs and simulations are performed using AWR® and CST®.

Keywords: Waveguide, Pin Diode, High Power, Low Response Time, Limiter, Schottky Diode, Detector

ÖZ

DALGA KILAVUZU YAPILI YÜKSEK GÜÇ LİMİTLEYİCİ TASARIMI

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Mikrodalga sınırlayıcılar koruyucu yapılardır. Devrelere zarar verebilecek yüksek güçte sinyallerin sisteme girişini engellemektedir. Radar sistemlerinin almaç devreleri genellikle çok düşük seviyedeki işaretleri işleme yeteneğine sahiptirler, bu da yarı-iletken malzemelerle oluşturulan çok hassas devre blokları kullanmayı gerektirir. Bu hassas devre elemanlarının girişine ulaşan yüksek güçte işarete karşı hasar görmeden dayanabiliyor olması gerekmektedir. Yüksek güçteki işaretlerin sebepleri; göndermeç kanalı ile almaç kanalı arasındaki izolasyonun yetersiz olması ve çok kısa darbe genişlikli yüksek güçlü işaret yayını yapabilen tehditler olabilir. Göndermeç kaynaklı tehditler zamanlama açısından daha kontrol edilebilir tehditlerdir. Fakat dış kaynaklı tehditlerin zamanlama açısından kontrol edilebilmesi mümkün değildir. Tehdit her an çalışmakta olan radar sisteminde problem yaratabilir. Almaç kanalını yakabilecek bu durumlardan koruyabilmek için düşük cevap zamanlı yüksek güç sınırlayıcılar kullanılmalıdır. Bu çalışmada sınırlayıcı tasarımı yapılırken iki kritik nokta hedeflenmiştir. İlk olarak gücü kW mertebesindeki işaretleri sınırlayabilen dalga kılavuzu sınırlayıcı tasarımı, ikinci olarak tasarlanan sınırlayıcının cevap verme süresini kısaltma amaçlanmıştır. Yüksek giriş gücüne dayanıklı “pin” diyotlar ile 9.4-10 GHz bandında çalışan dalga kılavuzu tek aşamalı iki farklı sınırlayıcı tasarlanmıştır. Tasarlanan dalga kılavuzu sınırlayıcıların doğrusal ve doğrusal olmayan ölçümleri yapılmıştır. Sonrasında iki farklı sınırlayıcı art arda takılarak oluşturulan iki aşamalı sınırlayıcı ölçümleri yapılmıştır. Tasarlanan sınırlayıcıların hassasiyetini ve cevap verme hızını arttırmak için “Schottky” diyot ile aynı bantta çalışan dalga kılavuzu detektör tasarlanmış ve sınırlayıcıların detektörle birlikte ölçümleri yapılmıştır. Devre tasarımları ve benzetimleri AWR® ve CST® kullanılarak yapılmıştır.

Anahtar Kelimeler: Dalga Kılavuzu, Pin Diyot, Yüksek Güç, Düşük Cevap Zamanı, Sınırlayıcı, “Schottky” Diyot, Detektör

To my family

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CHAPTER 1

INTRODUCTION

1.1. REVIEW OF LITERATURE

High power limiters has a vital role in modern radars; interference threats, high power microwave (HPM) pulse attacks, ultra wideband (UWB) pulse attacks, and TX/RX isolation problems are the main causes of compulsory high power limiter usage in radar systems [1]. Radio and radar receivers are expected to be capable of processing signals with very small amplitudes, necessitating the use of very sensitive circuit blocks that can contain fragile semiconductors [2].

High power limiters are generally used as a receiver protector device in military applications. The warfare field can include undesired high power interference signals. Such high power signals can saturate or even burns out the receiver structure.

Moreover, peak power of transmitted signals to an antenna may be in the order of kilowatts to megawatts [3]. Such high power transmission necessitates good isolation of the receiver side. In most of the applications, a circulator is used for isolating the transmitter and the receiver; however, even a small impedance mismatch of the antenna can cause a significant power transfer to the receiver side in the transmission period, which can damage or even burn out the receiver [4].

In addition to antenna mismatch problem which causes leakage to receiver, TX signal which is reflected from platform can be at dangereous power level for RX. However in pulsed working systems, the timings can be adjusted according to transmit and receive time to eliminate confliction time between TX and RX. This kind of high power problems are predictable.

HPM signal is the high power microwave signal and UWB signal is the ultra wideband signal. HPM signals are relatively narrow, less than 10% instantaneous bandwith [5]. HPM signals usually have rise time less than 10 nS and pulse width around 100 nS respectively [6]. In compare to HPM signals, UWB signals have very short rise time in the order of picoseconds and pulse width around few nanoseconds. The frequency spectum of UWB pulses relatively larger than HPM signals and UWB pulses have an instantenous bandwith larger than 25% [5]. UWB pulses whose power levels are high can cause big problems for receivers. It is difficult to have response time shorter than pulse width of UWB pulses for protector devices.

1.1.1. Front-Door Protection Sub Groups

All of the threats that are mentioned above enters the receiver of the system through its normal input, in other words the front door. Because of that, the protection devices which protect these systems are named as front-door protection devices. The front-door protection devices can be divided into sub groups according to the behaviour and the technology on which they are based on. These are clamping and crowbaring devices. Clamping and crowbaring are the main limiting mechanisms of the limiting device. Other classifications are still possible such as active and passive devices according to switching on mechanism of the device [7].

Clamping and Crowbaring

Clamping and crowbaring are the two main types of techniques utilized for the design of the limiters.

The main mechanism of limiting in clamping limiters is the impedance change experienced in the clamping structure during the high power pulse application. As the pulse exceeds the threshold level of the limiter, conduction starts and the pulse is clamped to a safe level. Low impedance path between the signal line and the ground is provided by clamping response. Top of the pulse envelope is clipped off and the pulse amplitude is reduced to proper levels (i.e. levels appropriate for safe reception for a receiver circuitry). Diode limiters and Metal Oxide Varistors (MOVs) are examples of clamping devices.

Crowbaring device uses switching mechanism. High power pulse, which exceeds a threshold level, triggers the conduction of the crowbaring device. Crowbaring device short circuits the pulse to ground potential and the level of RF voltage becomes zero (and current becomes maximum). The disadvantage of the crowbaring devices is the longer recovery time compared to clamping devices. The main reason for this disadvantage is its much lower impedance at the time of high power pulse application. Flow of substantially large surge currents remaining in the device is accomplished by crowbaring device [7]. In general, larger voltages and currents can be handled without breakdown problem compared to clamping devices. Gas Discharge Tubes (GDTs) are the example of the crowbaring devices.

Passive and Active Protection Devices

According to activation style, protector devices can be grouped as passive and active limiters [8]. Passive protection devices are self-activated limiters; limiting is performed without any requirement of external control signals or power supply. Most of the protector devices are passive. On the other hand, active protection devices require external control signals or power supply. Indeed, active protection devices can be considered as switches. Active protection devices have faster response time compared to passive protector devices. Faster response time results in smaller amount of energy to be transferred to the protected structure. Actually, the need of external signal or power supply can be considered as drawback of active limiters compared to passive limiters. Undamaged passive limiters provide protection even if the radar system does not operate.

Diode Limiters

The use of semiconductor diodes for limiting microwave power has been widely discussed [9-14]. There are a variety of different diode limiters. The first type is HF application of the LF technique of two diodes shunting a tranmission line [15-17]. The most of diode limiters clamp the pulse with fast rise times [17-19]. Doping of intrinsic region between P and N regions can be changed to adjust threshold level. The junction capacitance of diode must be low to use it at high frequencies.When the junction of the doped area is faced with pulse, the energy of the portion of high power pulse is converted to heat. If the diode limiter is exposed to high power pulse, it might be destroyed.

At the microwave frequency applications, pin diode limiting mechanism is not similar to mechanisms experienced in clipping diode usage. Pin diode shows lower resistance for higher power pulses [20-21]. It destructs the impedance matching mechanism and reflects high power signals, whereas clipping diodes clips the peaks of the waveform. Besides, the reflection coefficient exerted to the high power pulse is a function of the amplitude of the pulse, unlike the shunting mechanism of crowbaring techniques.

1.2. OUTLINE OF THESIS

In Chapter 2, PIN diode limiter fundamentals and general properties are described. Single stage and two stage limiter topologies are shown and explained. Design parameters and performance characteristics are presented.

In Chapter 3, first, diode selection for the limiter and detector design is explained. Besides, in this chapter, the simulations and modelling of the semiconductor devices and the structure cavities are presented together with the results and applications of the results.

In Chapter 4, fabrication of the WG detector and WG limiter are explained and shown. The mechanical structures of these two devices are shown and how these devices are produced is explained. Next, the linear, nonlinear and transient measurements regarding the fabricated limiters are presented together with the corresponding simulations. Also, the discrepancies are noted and explained in this chapter.

In Chapter 5, future works and brief conclusion are given.

CHAPTER 2

PIN DIODE LIMITER BACKGROUND

A simple limiter comprises a pin diode and RF choke inductor, both of which are in shunt with transmission line as it is shown in Figure 2.1. RF choke inductor is used for DC return of pin diode.

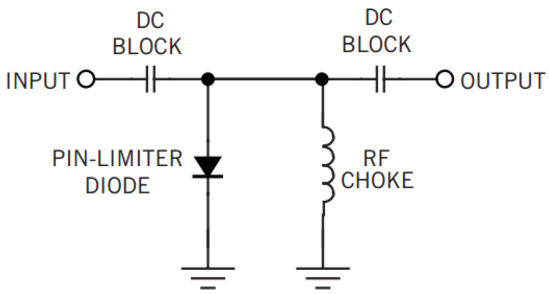

Figure 2.1: Basic Topology of Single Stage Pin Diode Limiter [2]

Pin diode is a kind of RF resistor whose resistance is lowered with increasing incident power. Without large input signals, the impedance of the limiter is at its maximum, resulting in insertion loss of typically less than 0.5 dB [2]. When the large power signal is presented to the input, impedance of the diode is lowered, and mismatch occurs resulting in higher reflection coefficient. Limiter shows linear AM-AM behaviour below the threshold level. Above threshold level, limiter shows an increasing insertion loss when the input signal power gets higher. A typical plot of output signal level vs input signal level is shown in Figure 2.2.

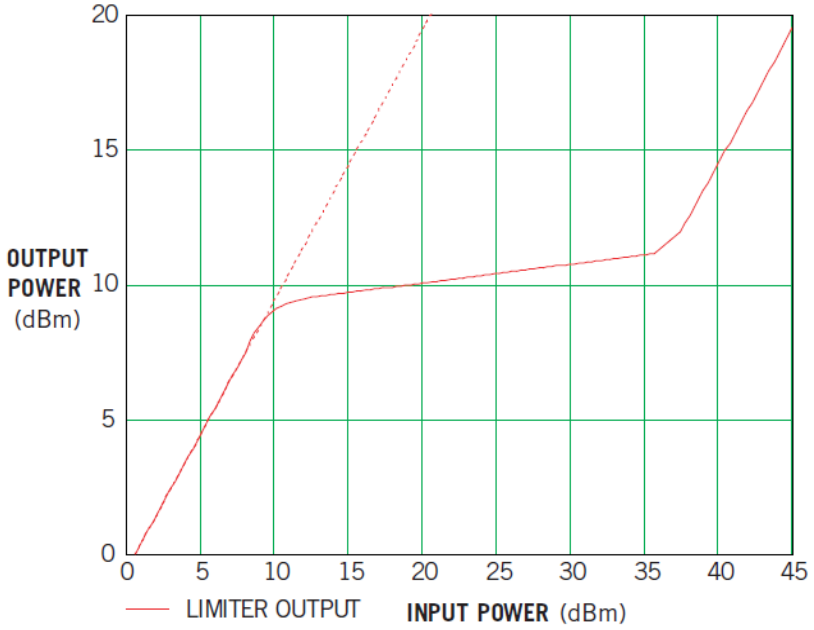

Figure 2.2: Example Pin Diode Limiter Response to Illustrate Linear and Nonlinear Regions of Pin Diode Limiter [2]

Since the limiter diode at low impedance state reflects the incident high power signal, the total power dissipation on the limiting diode is lowered (mainly dependent on the serial resistance of the diode). In Figure 2.3, generalized protector network, which has n number of shunt connected diodes is shown.

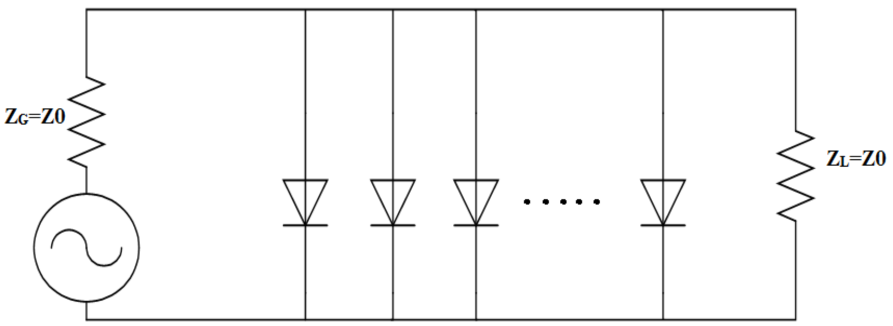

Figure 2.3: Generalized Protector Network Including N Number of Pin Diodes

Isolation of protector network is

$$\frac{\mathrm{P_A}}{\mathrm{P_L}} = \left(1 + \mathrm{n}\frac{\mathrm{Z_0}}{2\mathrm{R}}\right)^2 \xrightarrow[\mathrm{Z_0} \gg \mathrm{R}]{} \frac{\mathrm{n^2 Z_0^2}}{4\mathrm{R}^2} \tag{2-1}$$

where;

P_A : incident power

P_L : power reaching load

Z_0 : line impedance

n : number of diodes

R : resistance of diode at given forward bias.

If $Z_0/R >> 1$, isolation level $P_A/ P_L >>1$. When this condition is satisfied, the power P_d absorbed by each diode is approximately;

$$\frac{P_d}{P_A} \cong \frac{4R}{n^2 Z_0} \tag{2-2}$$

When $Z_0 / R >>1$, the diodes can protect receivers against incident power levels P_A much greater than the diode burnout power P_b since most of the incident power is reflected [22]. Also, inreasing the section of limiter diodes increases the isolation. On the other hand, insertion loss is traded off for the increased receiver protection which limits the number of diodes.

A single stage limiter can typically produce 20 to 30 dB isolation, depending on the input signal frequency and the charactesistics of the diode [2]. In the cases which requires much more isolation, the stage of the limiter can be inceased. Such kind of imiters are multi-stage limiters.

Two stage limiter is composed of two pin diode which have different power handling. More powerful diode is called ‘coarse’ diode and the other diode is called ‘cleanup’ diode. The schematic of two stage limiter is shown in Figure 2.4. The cleanup diode is the diode with the thinner I layer compared to coarse diode. Diameter of the P region can be larger for a coarse diode whose I region is thicker to have same capacitance value with cleanup diode [2]. Larger diameter of coarse diode results in a diode whose series resistance is lower than series resistance of the cleanup diode so that the isolation of the coarse limiter can be larger than the isolation of the cleanup limiter. Besides, low insertion loss is observed at coarse limiter under low level input signal conditions compared to cleanup limiter. Moreover, thermal resistance of the coarse diodes can be lower than thermal resistance of the cleanup diodes [2].

The cleanup diode is put λ/4 away from the coarse diode. When the high power signal reaches limiter, cleanup diode is turned on and its impedance is lowered. The reflection begins from the cleanup diode and standing wave is created with voltage minumum on the low impedance cleanup diode. Away λ/4 from claenup diode, voltage maximum occurs on coarse diode. Large voltage forces charge carriers into I layer and the impedance of coarse diode begins to become lower.

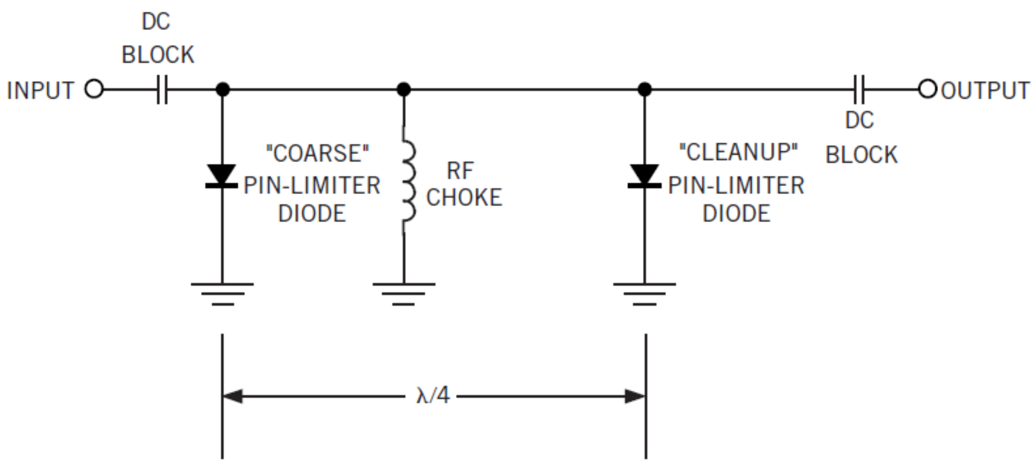

Figure 2.4: Basic Topology of Two Stage Pin Diode Limiter [2]

Transition of coarse diode from high impedance to low impedance takes time. If this time can be decreased, spike leakage level and response time which is the time to get flat leakage decrease. Flat leakage and spike leakage are shown in Figure 2.5.

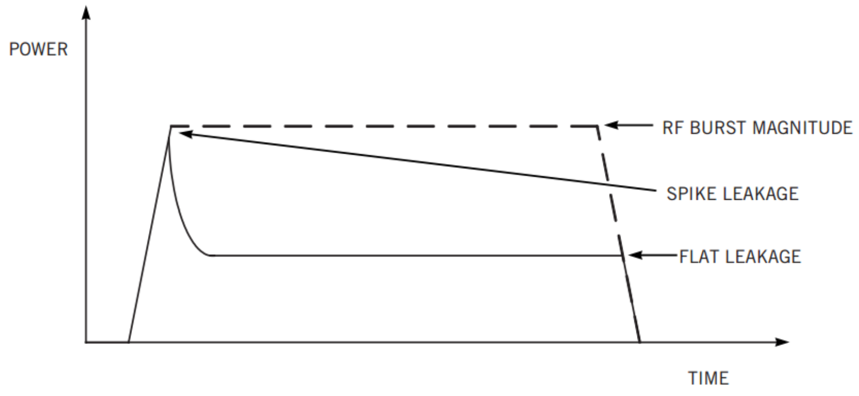

Figure 2.5: Example Time Domain Response of Basic Pin Diode Limiter Which Shows Spike Leakage and Flat Leakage [2]

The Schottky diode detector can be used to decrease state transition time of pin diode. When the small portion of RF signal power is detected to bias coarse diode, coarse diode can change its high impedance state to low impedance state faster. The schematic of Schottky detector biased two stage limiter is shown in Figure 2.6.

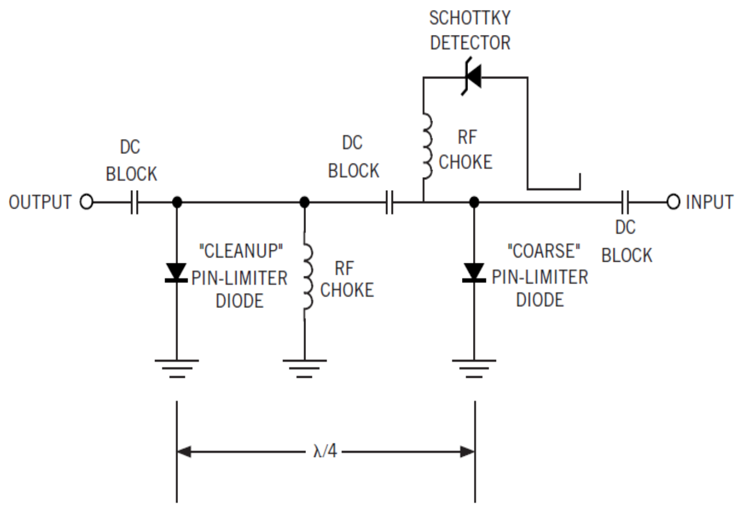

Figure 2.6: Basic Topology of Two Stage Limiter with Schottky Detector [2]

CHAPTER 3

WAVEGUIDE DETECTOR AND WAVEGUIDE LIMITER DESIGN

3.1. WAVEGUIDE DETECTOR DESIGN

A WG detector is designed to detect portion of RF power which passes through WG in 9.4-10 GHz frequency band. Sensing the level of RF power is important to bias pin diode of WG limiter. Increasing input power results in increased detected voltage and faster turning on of pin diode. In general, Schottky diode is used for designing detectors because of its fast turn on and off.

Bias voltage of limiter pin diode must be negative at a sufficient level to turn the pin diode on because in the waveguide structure the anode of pin diode is going to be DC ground. When the detected negative voltage is at cathode of pin diode, pin diode is going to be forward biased. DC return path of pin diode is completed via the Schottky diode. Cathode of Schottky diode is connected to the coupling loop mechanism inside the waveguide via transmission line. The coupling loop is mainly the DC path for the currents induced on the Schottky diode and the pin diode. This creates DC return for Schottky diode. The functional diagram of Schottky diode detector biased pin diode limiter is shown in Figure 3.1.

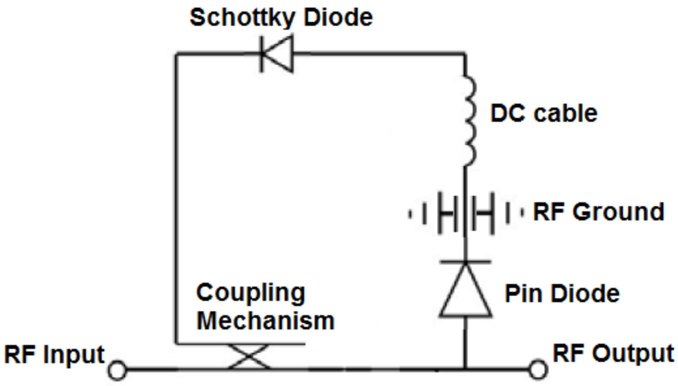

Figure 3.1: Functional Diagram of Schottky Detector Biased Pin Diode Limiter

3.1.1. Schottky Diode Selection

Schottky diode is also known as a detector diode. For a proper detection, the response time of detector diode should be lower than the period of the signal, which is directly related to the junction capacitance of the detector diode. Operation frequency of WG detector is going to be in X-Band and the Schottky diode of the detector should be selected accordingly.

Another important parameter of Schottky diode is the sensitivity (TSS – Tangential Signal Sensitivity). The dynamic range of the detector is related to the sensitivity figure of the diode itself. The selected Schottky diode to design WG detector is MSS20,046-T86 which is a product of Aeroflex/Metelics. The electrical parameters of the chosen Schottky diode are summarized in Table 3.1. The package of the chosen Schottky diode is pill package which can be used in coaxial structures. The package of chosen diode is shown in Figure 3.2. Package parasitic values of chosen Schottky diode are shown in Figure 3.3.

Table 3.1: Electrical Parameters of Selected Schottky Diode

Model	C_T MAX (pF)	T_{SS} TYP (dBm)	RV MIN (Ω)	RV MAX (Ω)	γ TYP (mV / mW)	Frequency MAX (GHz)
MSS20,046-**T86**	0.28	-59	2000	6000	8000	18
Test Conditions	f=1 MHz V_R=0 V	f= 10 GHz		P_{IN}=-30 dBm		R_L= 1 MΩ

Figure 3.2: Selected Schottky Diode whose Package is Proper for Usage in Coaxial Structures

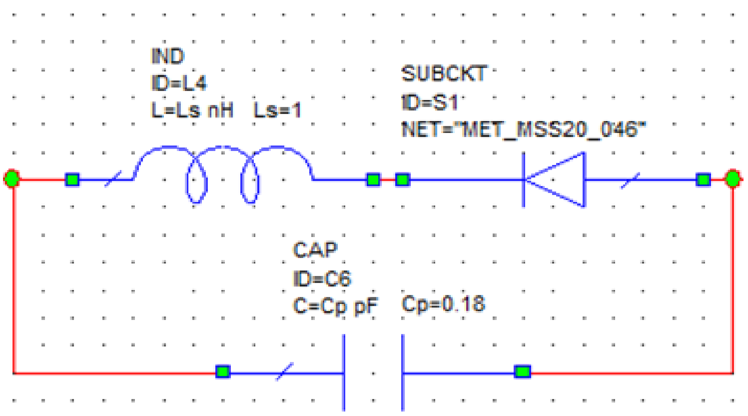

Figure 3.3: Lumped Model of Selected Schottky Diode with Package Parasitic Values

3.1.2. Coupling Loop in WG

In WG there must be a transition to coaxial structure which includes Schottky diode. Since the aim of WG detector is detecting small portion of RF power, light coupling is already enough for proper operation. TE_{10} mode is dominant mode in WR90 in 9.4-10 GHz frequency band. Time varying magnetic field inside coupling loop is the source of current which goes to coaxial structure. The direction of magnetic field is same with direction of propagation and the plane of coupling loop is perpendicular to propagation direction of RF signal. Coupling loop in WR90 WG and coaxial part is shown in Figure 3.4. The location of coupling loop is near the side wall of WG. At this location E-field strength is low because of tapered strength of E-field. The reasons of this location selection are not to disturb E-Field so much and to get light coupling. The radius of coupling loop is crucial parameter for adjusting coupling. By changing the radius of coupling loop, different coupling values can be acquired. The effect of coupling loop radius on detected voltage is going to be shown in simulation results.

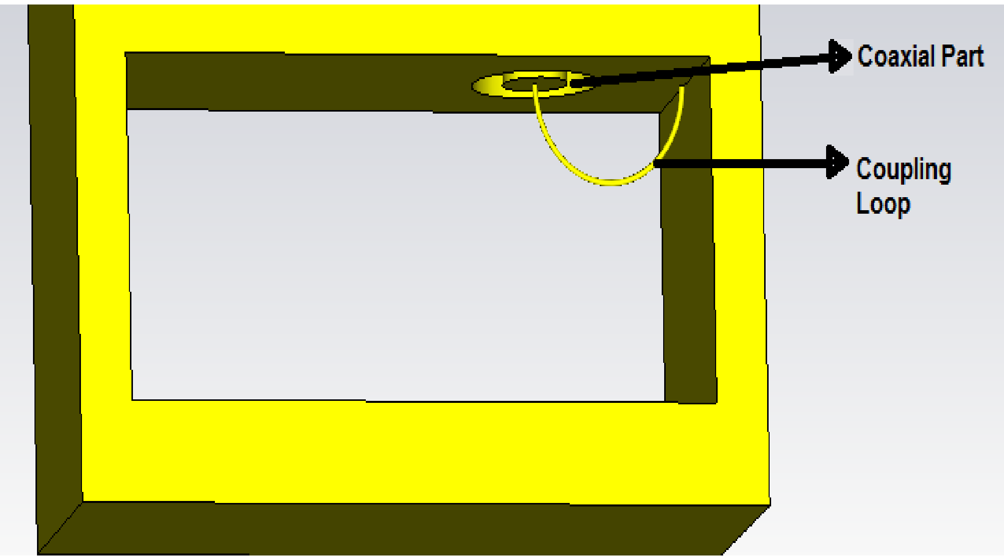

Figure 3.4 : Representation of Coupling Loop inside of WG Detector

3.1.3. Schottky Diode Impedance Matching in Coaxial Structure

In coaxial structure, impedance matching of the diode is simulated in AWR MWO. As it is seen in Figure 3.5, already modeled Schottky diode MSS20-046 in AWR, package parasitic taken from datasheet, DC return inductor L3, load capacitor CL, load resistance RL and two coaxial parts composes the detector schematic.

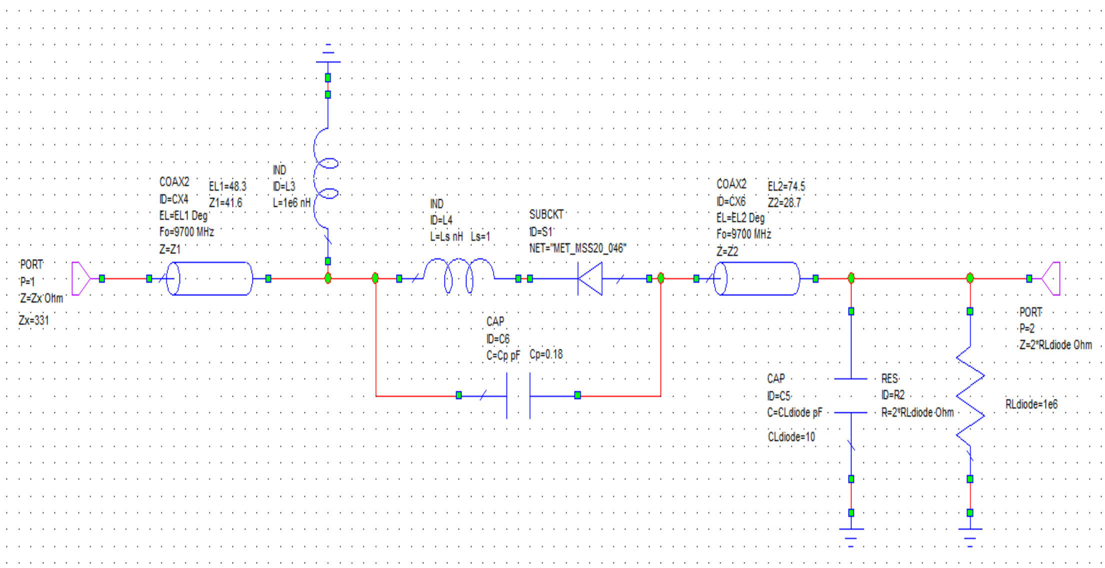

Figure 3.5: AWR Schematic which Shows Schottky Detector in Coaxial Structure with Load Capacitor and Resistor

The coaxial line just after the coupling loop accomplishes impedance matching of coupling loop impedance to input impedance of Schottky diode. The next coaxial line is mainly utilized for the mechanical requirements because load capacitor and resistor cannot be mounted directly on chosen Schottky diode. This coaxial line carries the detected DC current from the Schottky diode to the load capacitor and resistor at the end of the coaxial line. The length and impedance of coaxial parts are tuning parameters to get optimum impedance matching in 9.4-10 GHz frequency band. The length and impedance values of coaxial parts which give optimum impedance matching, package parasitic values, load capacitor value and load resistor value are shown in Table 3.2. Also, simulation result which shows the impedance matching is shown in Figure 3.6. (The detailed descriptions of the physical structures will be also presented throughout the discussion on the co-simulation sub sections).

Table 3.2: Schottky Detector Components' Values in AWR

Impedance of Coaxial Part 1 (Ω)	Elect. Length of Coaxial Part 1 (degree)	Impedance of Coaxial Part 2 (Ω)	Elect. Length of Coaxial Part 2 (degree)	Diode Package Capacitance (pF)	Diode Package Inductance (nH)	Load Capacitor (pf)	Load Resistance (Ω)
41.6	48.3	28.7	74.5	0.18	1	10	1M

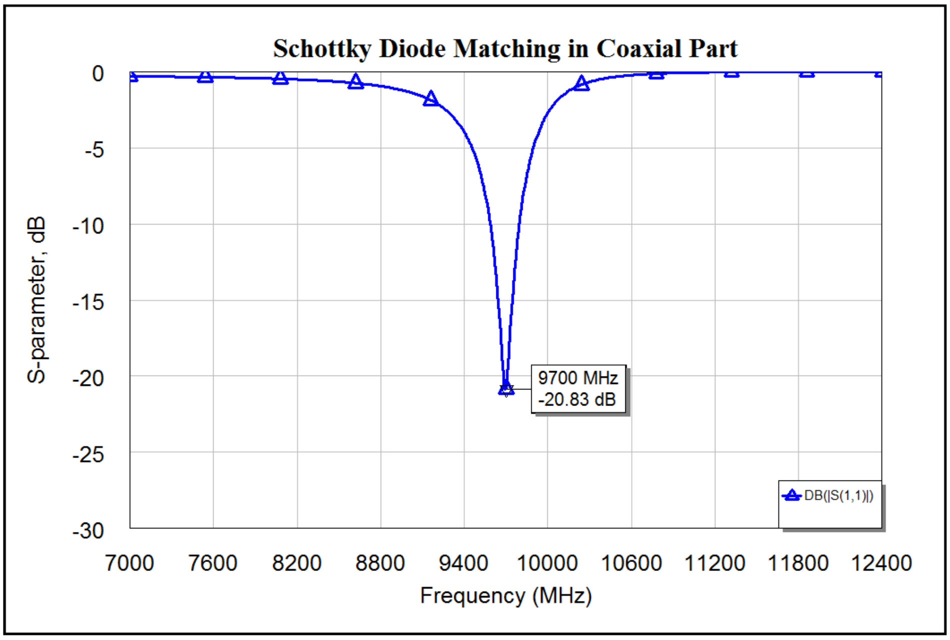

Figure 3.6: AWR Simulation Result which Shows Return Loss of Schottky Detector in Coaxial Structure

Impedance matching is tuned to center frequency of 9.7 GHz as shown in Figure 3.6. Impedance matching is made in the 9.7 GHz centered 200 MHz band above 10 dB return loss. The impedance change of input port does not affect the matching center frequency but affects the value of return loss. The observation of not having effect on matching center frequency reduces the importance of coupling loop impedance calculation. The coupling loop impedance is calculated roughly with impedance calculator to be 331 Ω.

After linear simulation, nonlinear simulation is performed. The aim of nonlinear simulation is to show increment of the detected voltage when the input power is increased. The nonlinear simulation result is shown in Figure 3.7. Transient analysis cannot be made in AWR MWO. Transient analysis simulations are made in CST and the results are going to be shown in the subsequent part. Steady state response is observed in AWR MWO.

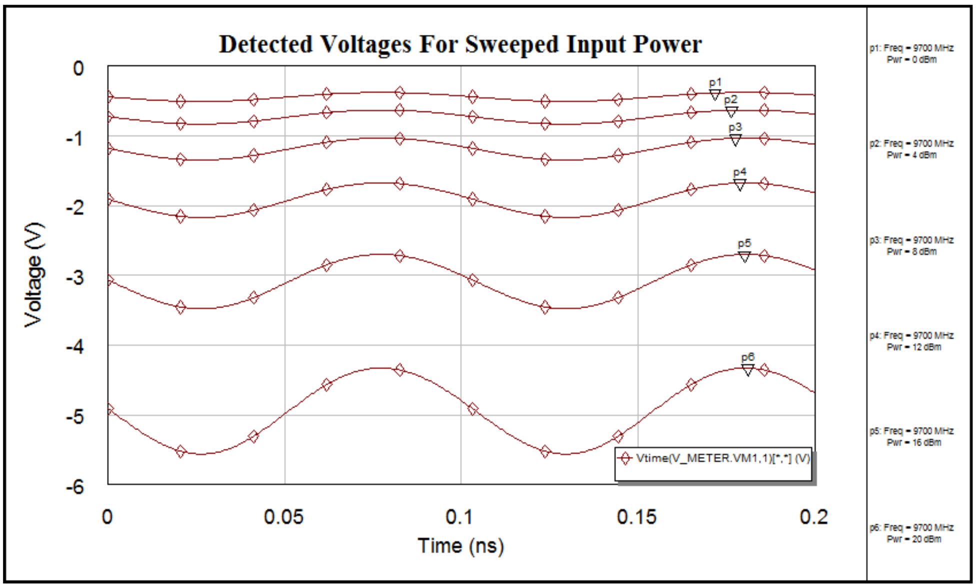

Figure 3.7: AWR Simulation Result which Shows Detected Voltages of Schottky Detector for Different Input Power Levels

The amount of ripple, which can be seen from Figure 3.7, is dependent on RC structure at output. When the load capacitor value gets smaller the ripple increases because low pass filter attenuation at low frequencies becomes lower. Increasing the value of load capacitor decreases the ripple however the time to reach steady state gets longer. Note that longer response time is worse than high ripple for detector biased limiter application, since fast limiting is desired.

3.1.4. 3D EM simulations of WG detector

After performing ideal simulations in AWR MWO to understand the effects of the detector components on the simulation results basically, realistic simulations should be made. CST is a tool which can make 3D EM simulation. Also, CST provides co-simulation tools which combine 3D structures with lumped components. The whole WG detector structure is drawn in CST as it is shown in Figure 3.8.

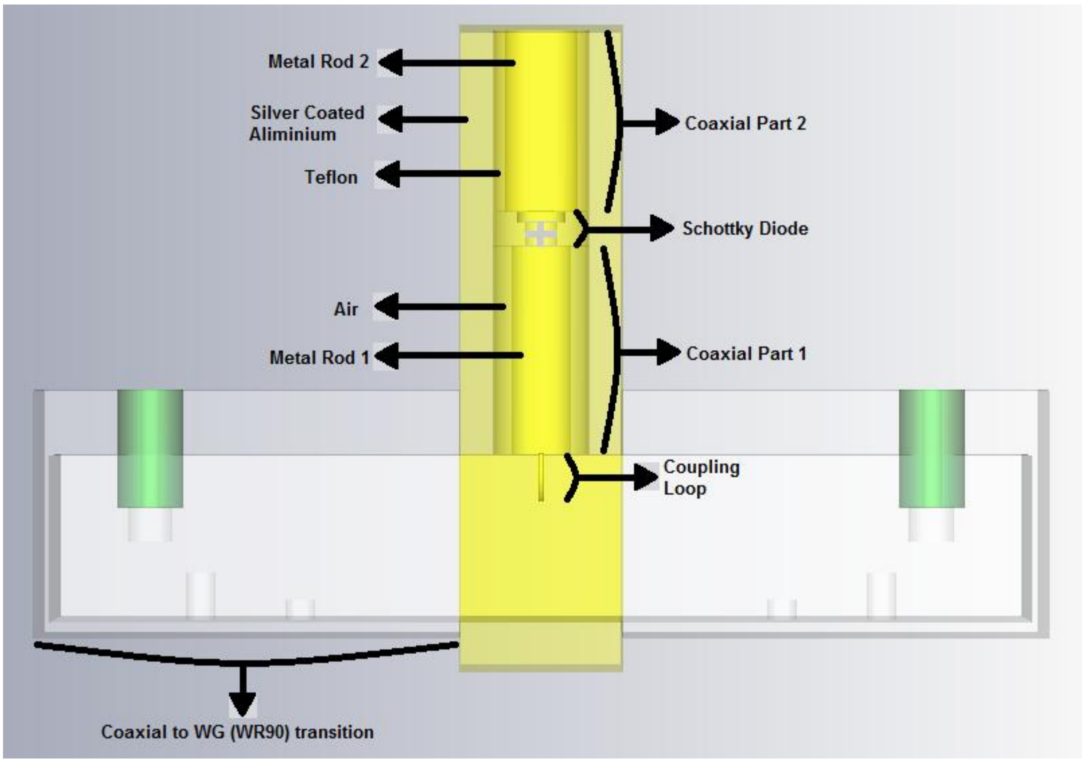

Figure 3.8: Side View of WG Detector in CST

CST can make time domain simulation with TEM mode input and output port. Otherwise it cannot make time domain simulation. Coaxial to WG (WR90) transitions at input and output are required to make time domain analysis. This transition converts TE_{10} mode of WG to TEM at input and output ports. WG to coaxial part transition is performed with coupling loop. Coaxial structure has three stage; coaxial part 1, Schottky diode and coaxial part 2. As explained earlier, coaxial part 1 is responsible for impedance matching between input of the diode and the coupling loop structure. Schottky diode package is drawn according to the dimensions from the respective datasheet. Coaxial part 2 is responsible for carrying output current of Schottky diode to the surface of outer metal. Load capacitor and load resistor can be mounted between end of the coaxial part 2 and the outer metal (silver coated aluminum) which is at ground potential. As seen in Figure 3.9, coaxial part 1 is filled with air and coaxial part 2 have dielectric material which is Teflon. The reason for not selecting air as dielectric filler for coaxial part 2 is that Teflon is solid and this solidness helps the whole coaxial structure to be fixed inside the metal body.

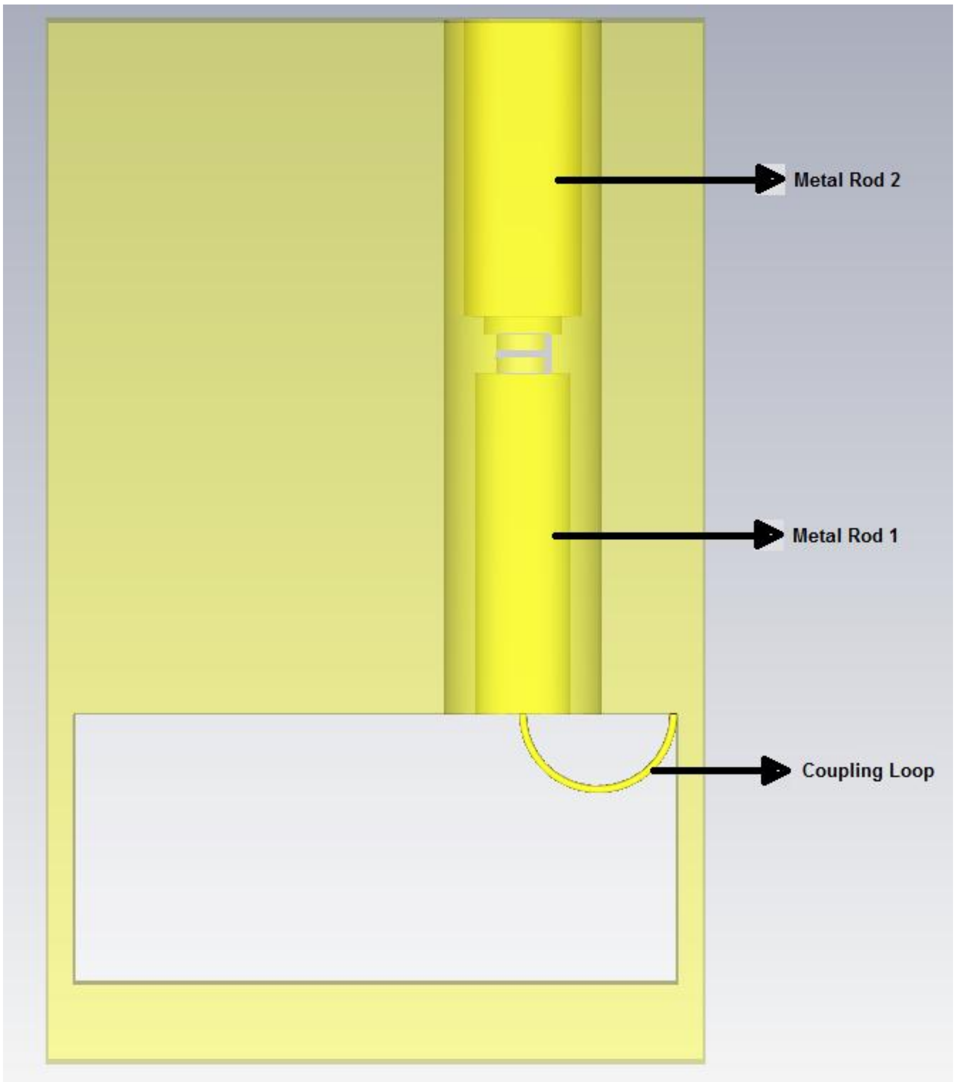

Figure 3.9: Cross Sectional View of WG Detector in CST

Metal rod 1 is the center metal of coaxial part 1 and metal rod 2 is the center metal of coaxial part 2. It was already explained that the length and the impedance of coaxial part 1 and 2 are tuning parameters of 3D EM simulation. EM simulation starts with the initial values which are taken from the AWR simulations. However realistic EM simulation does not give the same results as that found from the AWR simulations at the beginning. Here it can be observed that tuning is required for appropriate results. Also note that CST 3D EM simulation is slower compared to the ideal AWR simulations increasing the tuning times.

The ports of whole structure are shown in Figure 3.10. Port 1, Port 2 and Port 4 are CST defined waveguide ports. However, Port 3 is CST defined discrete port. Lumped model of the diode including spice model can be introduced to CST by discrete Port 3. Discrete port is crucial for co-simulation which combines lumped components and 3D structures. The schematic of co-simulation is shown in Figure 3.11. Tuned values of coaxial parts' lengths and impedances and the values of lumped components are shown in Table 3.3.

Table 3.3: Schottky Detector Components' Values in CST

Impedance of Coaxial Part 1 (Ω)	Electrical Length of Coaxial Part 1 (degree)	Impedance of Coaxial Part 2 (Ω)	Electrical Length of Coaxial Part 2 (degree)	Half-Loop Radius (mm)	Diode Package Inductance (nH)	Load Capacitor (pF)	Load Resistance (Ω)
29.97	150.24	11.9	187.36	2.85	1	10	1M

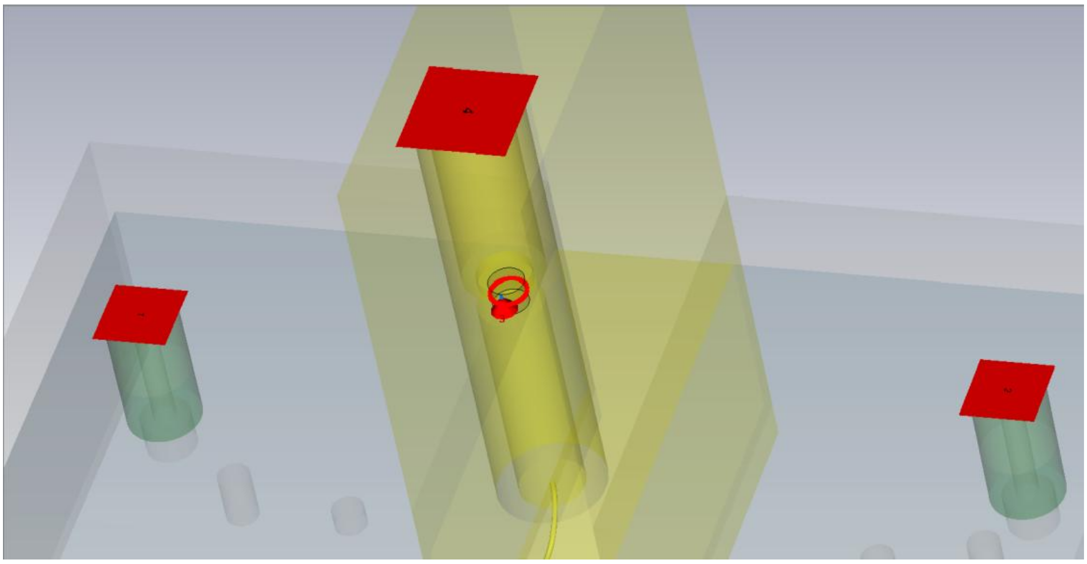

Figure 3.10: Representation of WG Detector Ports in CST

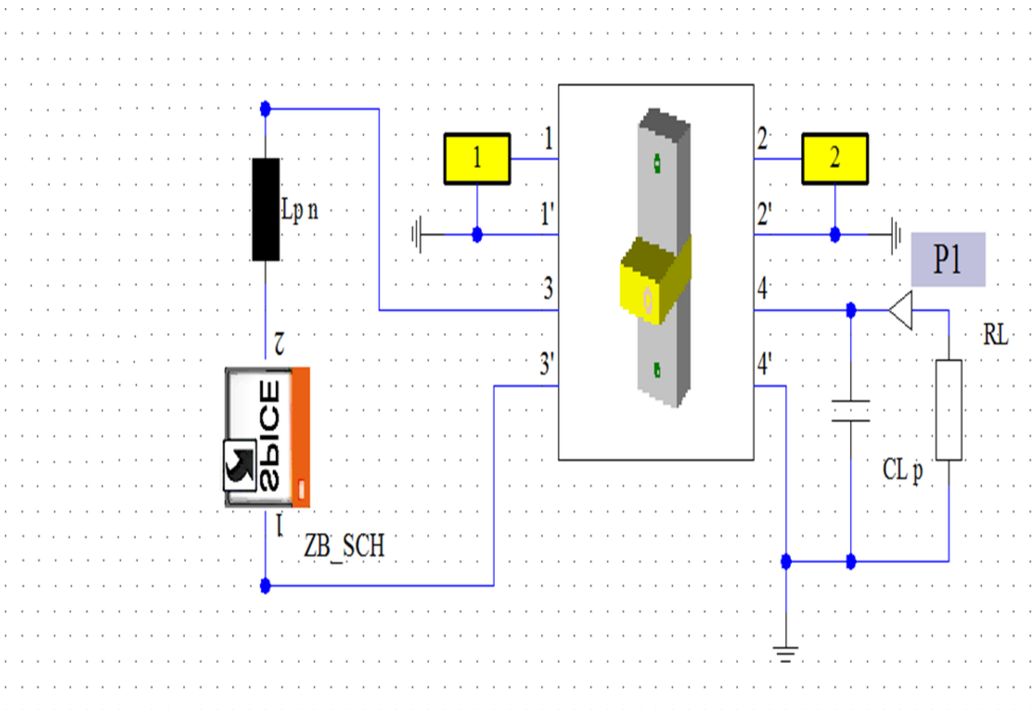

Figure 3.11: CST Co-Simulation Schematic which Shows Combination of 3D Structures and Lumped Components of WG Detector

3D EM co-simulation results are shown in Figures 3.12- 3.15. In the Figures 3.12 and 3.13, the transient time domain response is analyzed. Effect of the input power and the load capacitor are shown in Figure 3.12. When the input power is increased from 59 dBm to 65 dBm, the detected voltage increases from 2.9V to 13V at tenth nanosecond. Transient analysis is stopped at tenth nanosecond because longer simulation takes longer time to wait. 10 ns is sufficient time to get desired results from the transient analysis. Also, the other parameter, the load capacitor value, is decreased from 20 pF to 10 pF. It is observed that lower value of the load capacitor results in higher ripple and lower time to reach steady state. In Figure 3.13, the effect of coupling loop radius is shown. When the coupling loop area is increased, the detected voltage increases. These results show us the WG detector structure is working and it can detect portion of RF input power. In addition to nonlinear time domain simulations, linear S-parameter simulation is done. S-parameter simulation results are shown in Figure 3.14 and Figure 3.15.

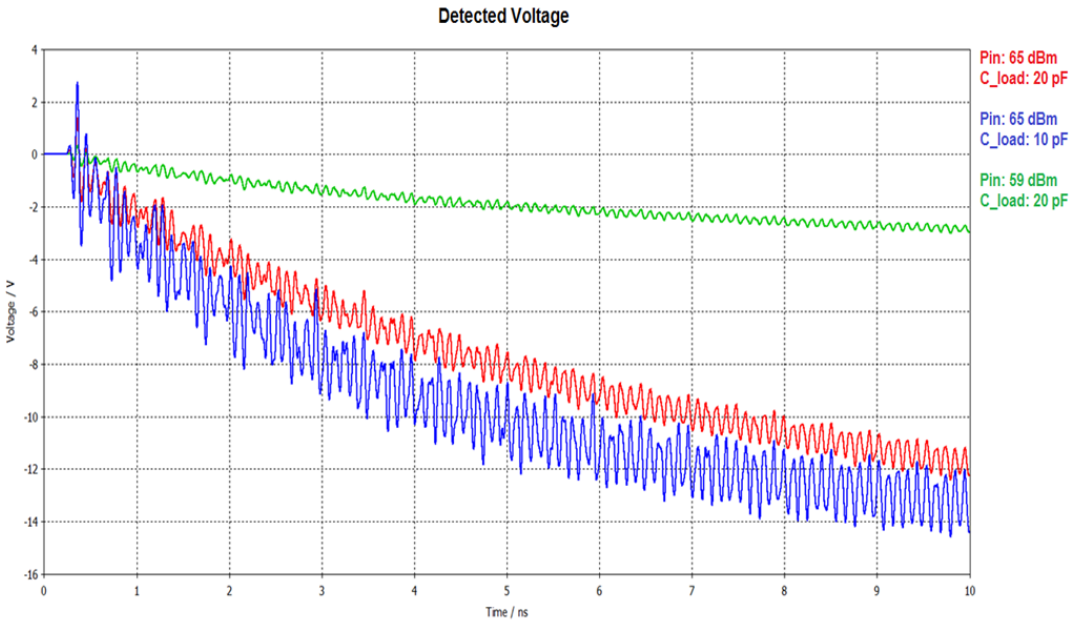

Figure 3.12: CST Simulation Result which Shows Effect of Input Power Level and Load Capacitor On Detected Voltage

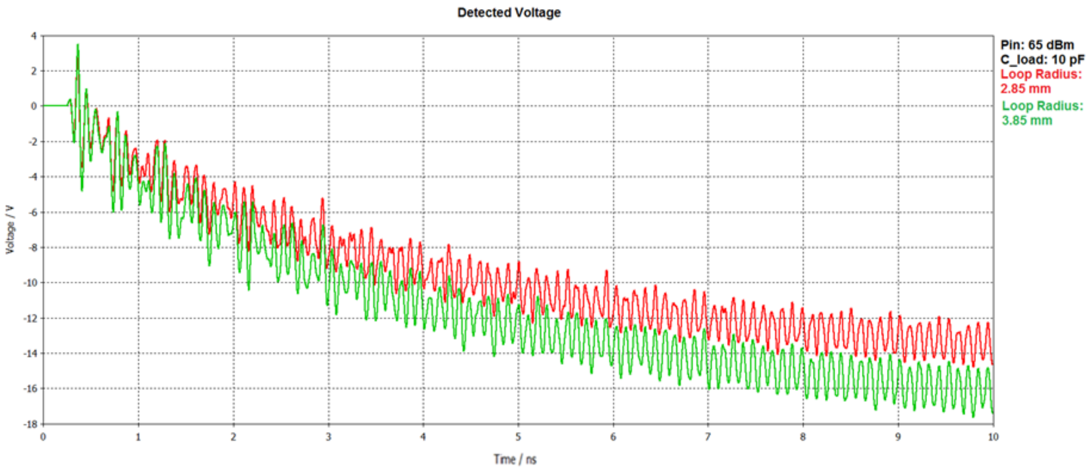

Figure 3.13: CST Simulation Result which Shows Effect of Coupling Loop Radius On Detected Voltage

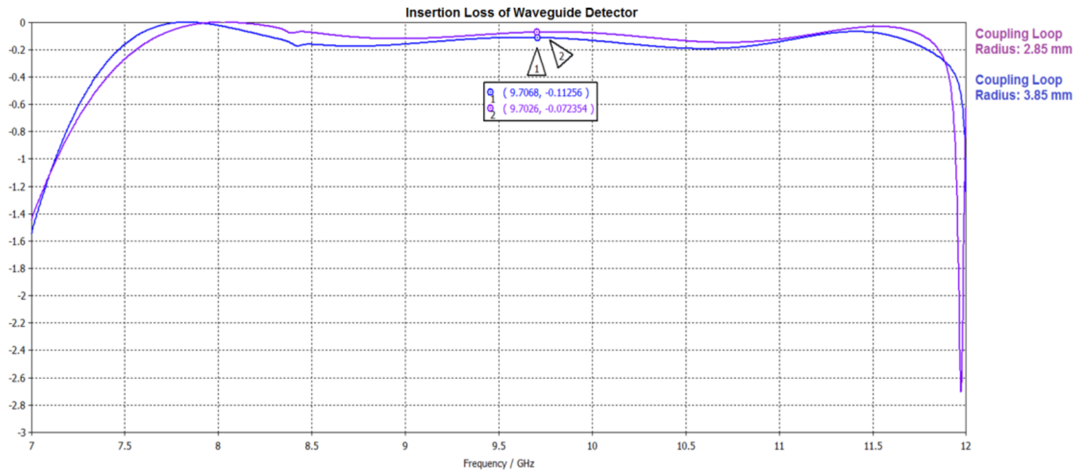

Figure 3.14: CST Simulation Result which Shows Coupling Loop Radius Effect on Insertion Loss of Waveguide Detector

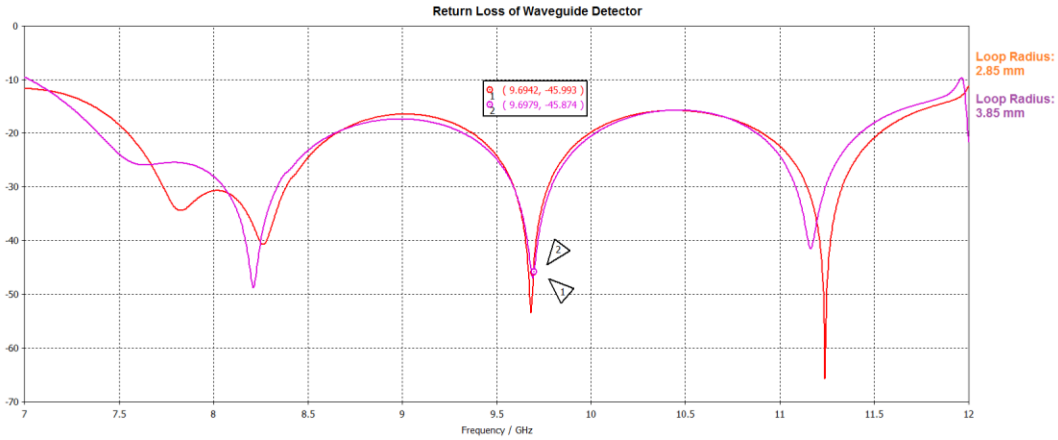

Figure 3.15: CST Simulation Result which Shows Return Loss of Waveguide Detector

Insertion loss of the WG detector is 0.072 dB and return loss of the WG detector is below 45 dB at 9.7 GHz when the coupling loop radius is 2.85 mm.

$IL = 10 \times \log(|S_{21}|^2)$

$RL = 10 \times \log(|S_{11}|^2)$

$(|S_{21}|^2) + (|S_{11}|^2) = 1$

It should be noted that, 45 dB of RL would require much lower IL (lower than 0.072 dB, since lossless simulation is made) to be exercised in the simulation. But the result shows us that the coupled power into the detector loop increases the insertion loss of the structure. This observation can be justified by changing the above notation.

$(|S_{31}|^2) + (|S_{21}|^2) + (|S_{11}|^2) = 1$

But note that the third port in the EM simulation is a lumped port and calculating S31 in the simulator would cause meaningless results. According to S_{21} and S_{11} results, the coupled power can be easily inferred to be as 17.82 dB provided that a third fictitious port is used in the calculations.

In Figures 3.14 and 3.15, the results are also simulated for coupling loop radius of 3.85 mm. From the simulations, it is clear that the coupling value is increased to 15.92 dB together with an increase of the IL value (to 0.11 dB). Same comment was made after the transient time domain simulations. Both linear and nonlinear simulations results show the effect of coupling loop clearly.

3.2. WAVEGUIDE LIMITER DESIGN

Waveguide limiter is the structure which combines waveguide and pin diode. The pin diode placement in WG is the main problem of WG limiter design. Post coupling mechanism is crucial to put pin diode in WG and it provides transition between waveguide mode and coaxial mode. Post coupling mechanism will be analyzed with simulators. In fact, pin diode is put in coaxial structure which resonates in desired band. Low power signal response of the waveguide limiter is like bandpass filter response and in contrast, high power signal response is like bandstop filter response. When the input power level is increased, S_{11} and S_{21} interchange at 9.7 GHz is the main purpose of the WG limiter design. Pin diode ON and OFF states are used to create this interchange.

Here, single stage post coupled pin diode WG limiter is designed to operate in 9.4-10 GHz frequency band; the desired bandwidth is 600 MHz. AWR MWO and CST 3D EM simulators are used to make ideal and realistic linear simulations.

3.2.1. Pin Diode Selection

Pin diode selection is the starting point in design. Since high power limiting is desired; the pin diode, which has high power survivability, should be chosen. High power handling of pin diode is related to dissipated power on it. Low power dissipation requires low series resistance. In high power limiter applications, series resistance is the key parameter while selecting pin diode. In addition to high power specification, the speed of transition from OFF state to ON state is important too.

When the high power pulse enters the receiver, pin diode limiter should react rapidly. However, higher power survivability results in slower transition between ON and OFF states because of junction capacitance of pin diode, which also affects the operating frequency range of the device. The junction capacitance of the pin diode should be selected according to the operating frequency in X-band. In addition to junction capacitance; the package parasitic capacitance and inductance affect the upper level of operating frequency.

The pill packaged pin diode is selected for coaxial structure. In order to observe power handling performance and response time of pin diode limiter, two pin diodes are chosen. These diodes are product of Aeroflex/Metelics. Their part numbers are MLP7120-T86 and MLP7110-T86. T86 code is package code of pin diodes. MLP7120 pin diode is tougher compared to MLP7110 pin diode. Their electrical and RF characteristics are shown in Table 3.4 and the package of diodes is shown in Figure 3.16.

Table 3.4: Electrical Characteristics of Selected Pin Diodes

	V_B, V	C_j, pF	R_s, Ω	R_s, Ω	τ, ns	Θ_{jc}, $^{O}C/W$	Θ_{jc}, $^{O}C/W$
Condition	IR=10uA	V_R=0V F=1MHz	IF=10mA F=1GHz	IF=1mA F=1GHz	IF=10mA IR=6mA	1uS pulse	CW
MLP7120	120-180	0.2	1.5	3.5	50	1.2	40
MLP7110	45-75	0.2	1.5	4	10	15	80

Table 3.5: RF Characteristics of Selected Pin Diodes

	Max. P_{PEAK} (dBm)	Threshold (1dB Limiting) (dB)	$P_{leakage}$ (dBm)	I.L. (dB)	CW P_{in} (W)	Recovery Time (ns)
MLP7120	60	20	39	0.1	5	50
MLP7110	53	15	27	0.1	3	20

Figure 3.16: Selected Pin Diode whose Package is Proper for Usage in Coaxial Structures

As can be seen in Figure 3.16, it can be attached to center metal of the coaxial structure with conductive epoxy easily. According to information taken from datasheet, package parasitic capacitance is 0.18 pF and package parasitic inductance is 0.45 nH. Modeling of the pin diode for ON and OFF states is described in subsequent parts. Also, polarity of the diode can be shown from its package. Anode of pin diode is wide side and the cathode is on the other side.

3.2.2. Pin Diode Modeling

Modeling of the pin diode with lumped components is necessary to make linear simulation. Lumped components of the pin diode model are package parasitic capacitance Cp, package parasitic inductance Ls, junction capacitance Cj and series resistance Rs. The schematic, which is composed of lumped components of pin diode, is shown with components' values in Figure 3.17. Pin diode ON and OFF states represented with low and high resistance value of Rs in linear simulations. Cp value is omitted in CST EM simulation because the package of the diode is drawn and the drawn package already models this capacitance.

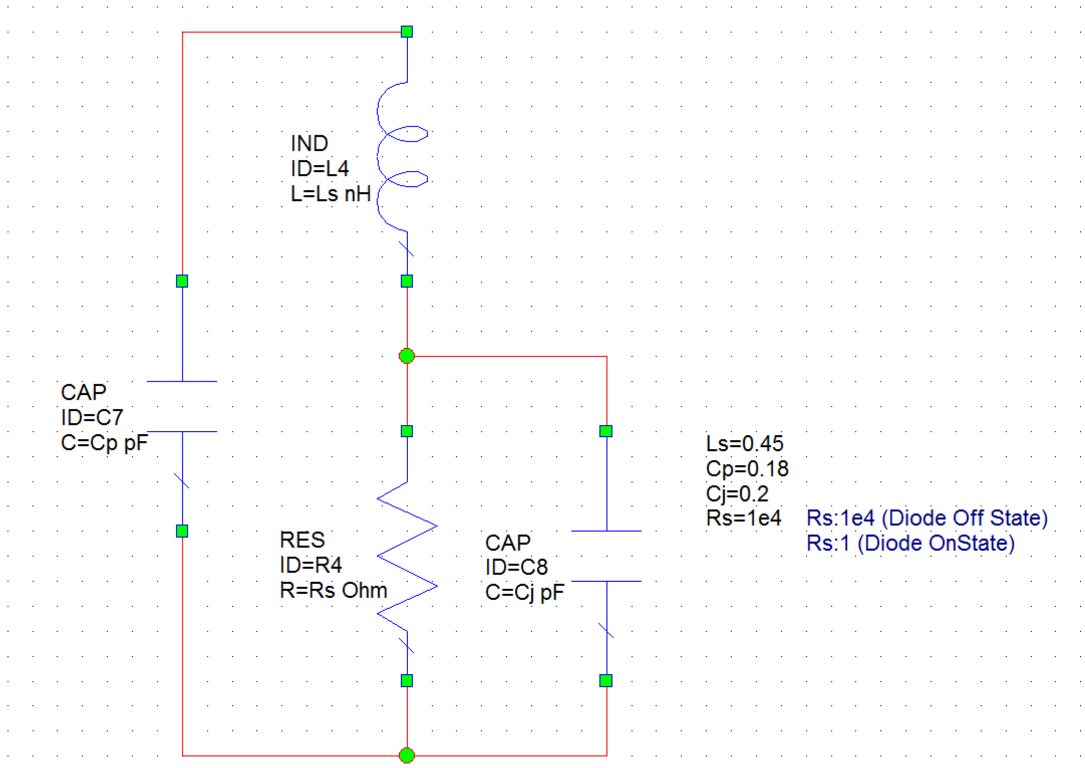

Figure 3.17: AWR Schematic which Shows Lumped Model of Pin Diode

3.2.3. Reduced Height Waveguide Modeling

Reduced height waveguide is used to make better impedance transition between WR90 WG and the coaxial structure which includes the pin diode. Reducing the height of the WG results in reduced impedance of WG. The formula which is used for waveguide impedance calculation is shown in equation 3-1 where λ_G is the guided wavelength of WG, λ_0 is the wavelength in the vacuum, b is the height of WG and a is the broader wall width of the waveguide.

$$Z_0 = 2 \times \sqrt{\frac{\mu_0}{\varepsilon_0}} \times \frac{\lambda_G}{\lambda_0} \times \frac{b}{a} \tag{3-1}$$

In addition to waveguide impedance calculation, there are formulations to model the transition between WR90 to reduced height waveguide. The WR90 WG to reduced height WG transition is shown in Figure 3.18, and its equivalent circuit is shown in Figure 3.19. The formulations by Marcuvitz to calculate the admittance value B, which is shown in Figure 3.19, are shown in equations 3-2, 3-3 and 3-4 [23].

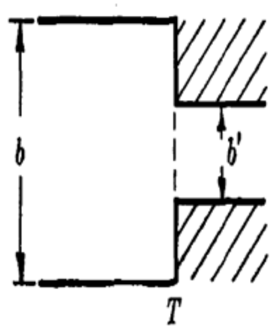

Figure 3.18: Side View of Reduced Height WG [23]

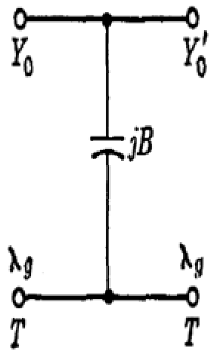

Figure 3.19: Equivalent Circuit of Reduced Height WG [23]

$$\frac{Y_0}{Y_0'} = \frac{b'}{b} = \alpha = 1 - \delta \tag{3-2}$$

$$A = \left(\frac{1+\alpha}{1-\alpha}\right)^{2\alpha} \frac{1+\sqrt{1-\left(\frac{b}{\lambda_G}\right)^2}}{1-\sqrt{1-\left(\frac{b}{\lambda_G}\right)^2}} - \frac{1+3\alpha^2}{1-\alpha^2} \tag{3-3}$$

$$\frac{B}{Y_0} \approx \frac{2b}{\lambda_G}\left[\ln\left(\frac{1-\alpha^2}{4\alpha}\right)\left(\frac{1+\alpha}{1-\alpha}\right)^{1/2(\alpha+1/\alpha)} + \frac{2}{A}\right] \tag{3-4}$$

These formulas are inserted to AWR MWO as global definitions to be made calculation of admittance B value. The calculations are made automatically by AWR MWO while b′ value varies. The AWR MWO schematic which shows the parameters of the reduced height WG model is shown in Figure 3.20.

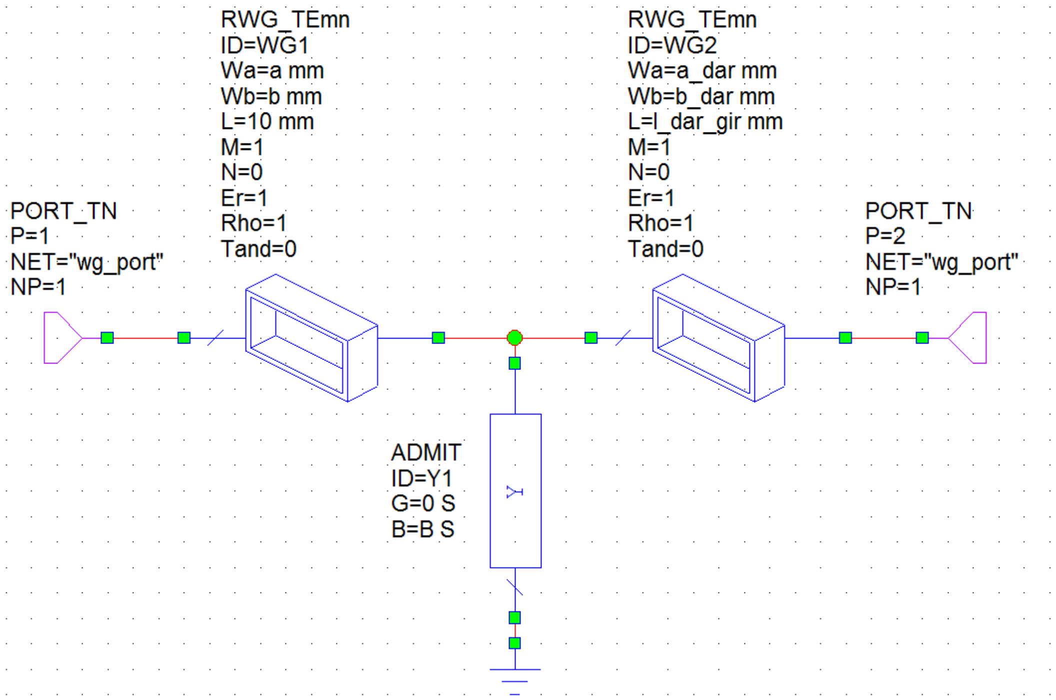

Figure 3.20: AWR Schematic which Shows the Reduced Height WG Model

3.2.4. Modeling of Centered Solid Inductive Post in Rectangular WG

In WG limiter design, centered solid inductive post enables transition between modes of waveguide and coaxial structure. TE_{10} to TEM transition is made by solid inductive post, in other words by post coupling. Similar to reduced height waveguide modeling, there are formulations to model centered solid inductive post in rectangular WG by Marcuvitz [23]. The modeling is done without considering the coaxial structure. Cross sectional view, top view and equivalent circuit are shown in Figure 3.21, Figure 3.22 and Figure 3.23; however these figures are general representations of solid inductive post which is not at the center of WG. If x equals to a/2 in top view of solid inductive post, centered solid inductive post can be imagined easily. Reactance values X_b and X_a are calculated with the equations 3-5, 3-6, 3-7 and 3-8.

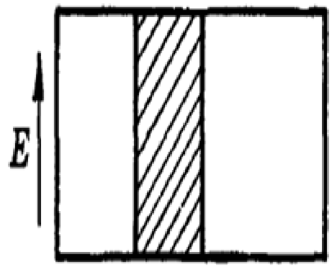

Figure 3.21: Cross Sectional View of Inductive Post in WG [23]

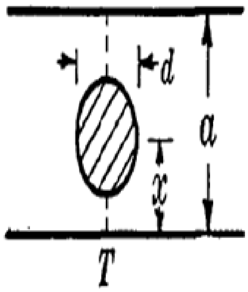

Figure 3.22: Top View of Inductive Post in WG [23]

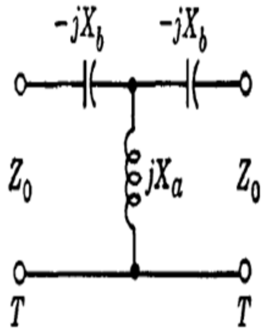

Figure 3.23: Equivalent Circuit of Inductive Post in WG [23]

$$\frac{X_a}{Z_0} = \frac{X_b}{2Z_0} + \frac{a}{2\lambda_G}\left[S_0 - \left(\frac{\pi d}{2\lambda}\right)^2 - \frac{5}{8}\left(\frac{\pi d}{2\lambda}\right)^4 - 2\left(\frac{\pi d}{2\lambda}\right)^4\left(S_2 - 2S_0\frac{\lambda^2}{\lambda_G^2}\right)^2\right] \tag{3-5}$$

$$\frac{X_b}{Z_0} = \frac{a}{\lambda_G}\frac{\left(\frac{\pi d}{a}\right)^2}{1+\frac{1}{2}\left(\frac{\pi d}{\lambda}\right)^2\left(S_2+\frac{3}{4}\right)} \tag{3-6}$$

$$S_0 = \ln\frac{4a}{\pi d} - 2 + 2\sum_{n=3,5,\ldots}^{\infty}\left[\frac{1}{\sqrt{n^2-\left(\frac{2a}{\lambda}\right)^2}} - \frac{1}{n}\right] \tag{3-7}$$

$$S_2 = \ln\frac{4a}{\pi d} - \frac{5}{2} + \frac{11}{3}\left(\frac{\lambda}{2a}\right)^2 - \left(\frac{\lambda}{a}\right)^2\sum_{n=3,5,\ldots}^{\infty}\left[\sqrt{n^2-\left(\frac{2a}{\lambda}\right)^2} - n + \frac{2}{n}\left(\frac{a}{\lambda}\right)^2\right] \tag{3-8}$$

These formulas are inserted to AWR MWO as global definitions to calculate easily reactance values X_a and X_b while d value which is diameter of post varies. The calculations are defined in AWR as equations. The AWR MWO schematic which shows the parameters is shown in Figure 3.24.

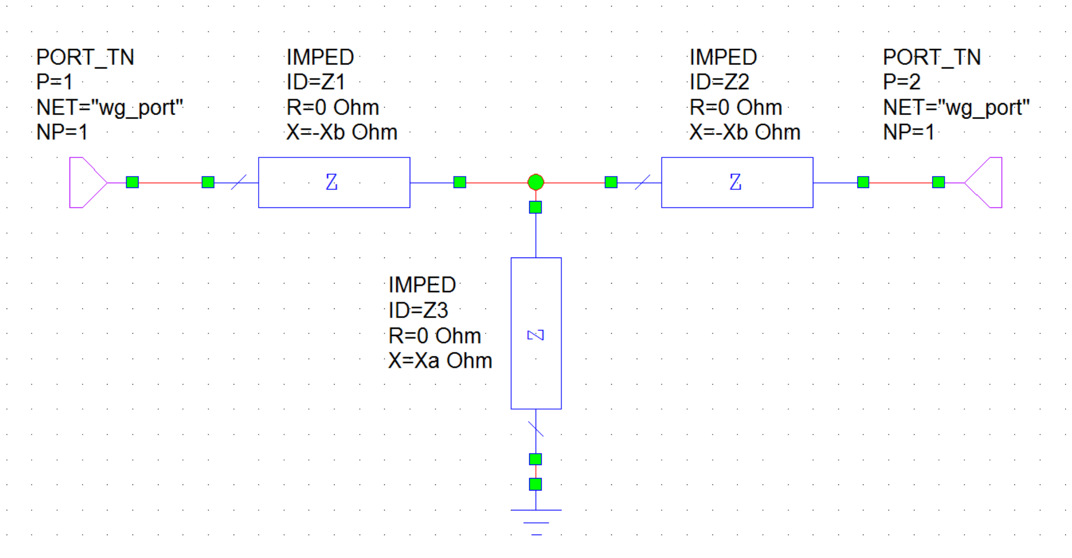

Figure 3.24: AWR Schematic which Shows Model of Solid Inductive Post in WG

3.2.5. Post Coupled Pin Diode Waveguide Limiter in AWR

After modeling of pin diode, reduced height waveguide and centered solid inductive post are completed; the whole structure is drawn in AWR MWO as can be seen in Figure 3.25.

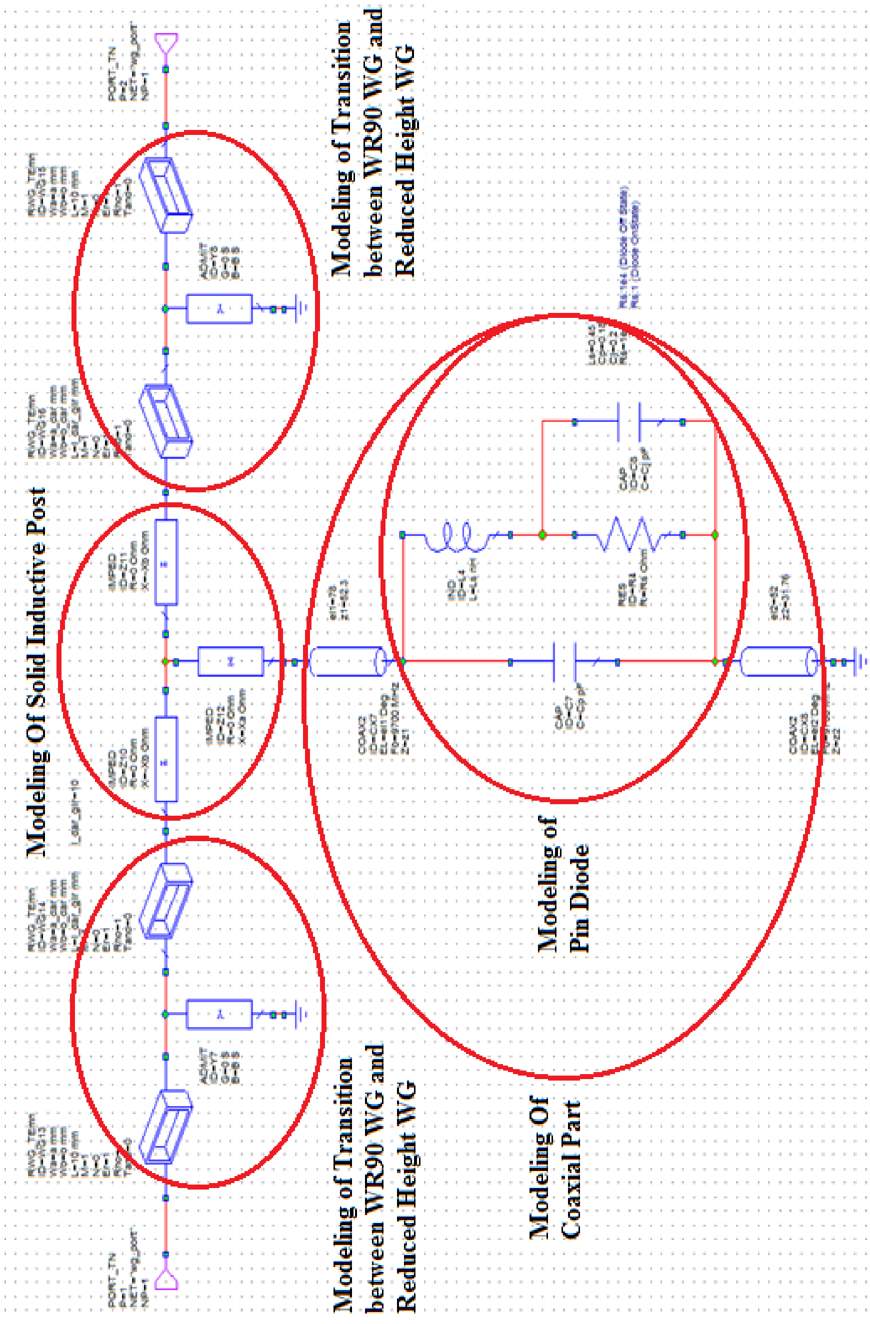

Figure 3.25: AWR Schematic of Post Coupled Pin Diode WG Limiter

The post coupled pin diode WG limiter is simulated to get linear frequency response. The simulations are performed at ON and OFF states of pin diode. As mentioned in earlier parts of this chapter, series resistance Rs of pin diode determines the state of pin diode. When it is set to high resistance, which can be considered as open, post coupled pin diode limiter is not at limiting state. When it is set to low resistance, which can be considered as short, post coupled pin diode limiter is at limiting state. When the Rs of pin diode acts like open, junction capacitance C_j in parallel with Rs begins to have an effect on resonating structure with the pin diode package parasitic capacitance C_p and inductance L_s. When the Rs of pin diode acts like short, C_j does not have any effect on resonating structure and only package parasitic capacitance and inductance creates resonating structure. With the help of the coaxial transmission lines, frequency of resonance is tuned to desired frequency band 9.4-10 GHz. In simulation results; bandpass response is desired when R_s acts like open, bandstop response is desired when R_s acts like short.

There are two coaxial lines in the schematic which is shown in Figure 3.25. Impedance and length of these lines; which are el1, z1, el2, z2; are tuning parameters after selecting fix values for height "b_dar" and length "l_dar_gir" of reduced height waveguide, and for diameter "d" of inductive post. The parameter values which give optimum response are shown in Table 3.6. The simulation results are shown in Figure 3.26 and Figure 3.27 and the results seem to be acceptable as the first step into the design. Pin diode OFF state simulation result is shown in Figure 3.26. The response is similar to bandpass response with good return loss in desired band. Pin diode ON state simulation result is shown in Figure 3.27. The response is similar to bandstop response. S_{21} and S_{11} responses of post coupled pin diode WG limiter interchange in same band when the diode state is changed.

Table 3.6: WG Limiter Components' Values in AWR

a,a_dar (mm)	b (mm)	b_dar (mm)	l_dar_gir (mm)	d (mm)	el1 (degree)	z1 (Ω)	el2 (degree)	z2 (Ω)
22.86	10.16	6	10	2.5	78	52.3	52	31.76

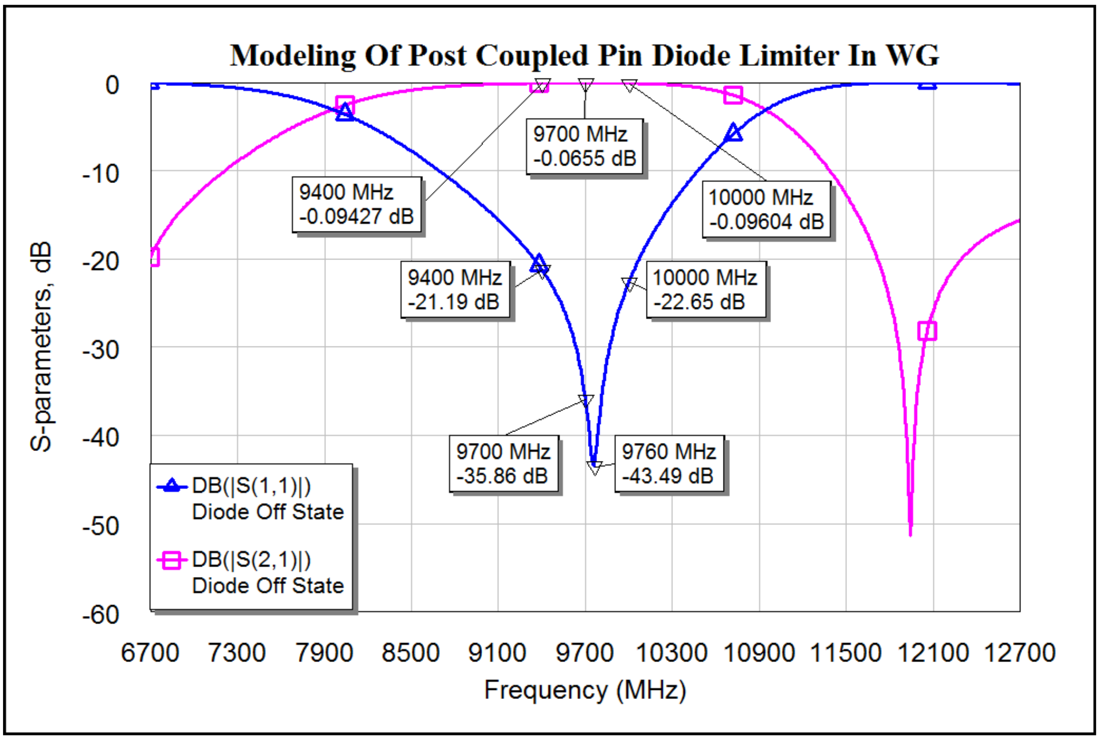

Figure 3.26: AWR Simulation Result which Shows S-parameter Of Limiter at OFF State

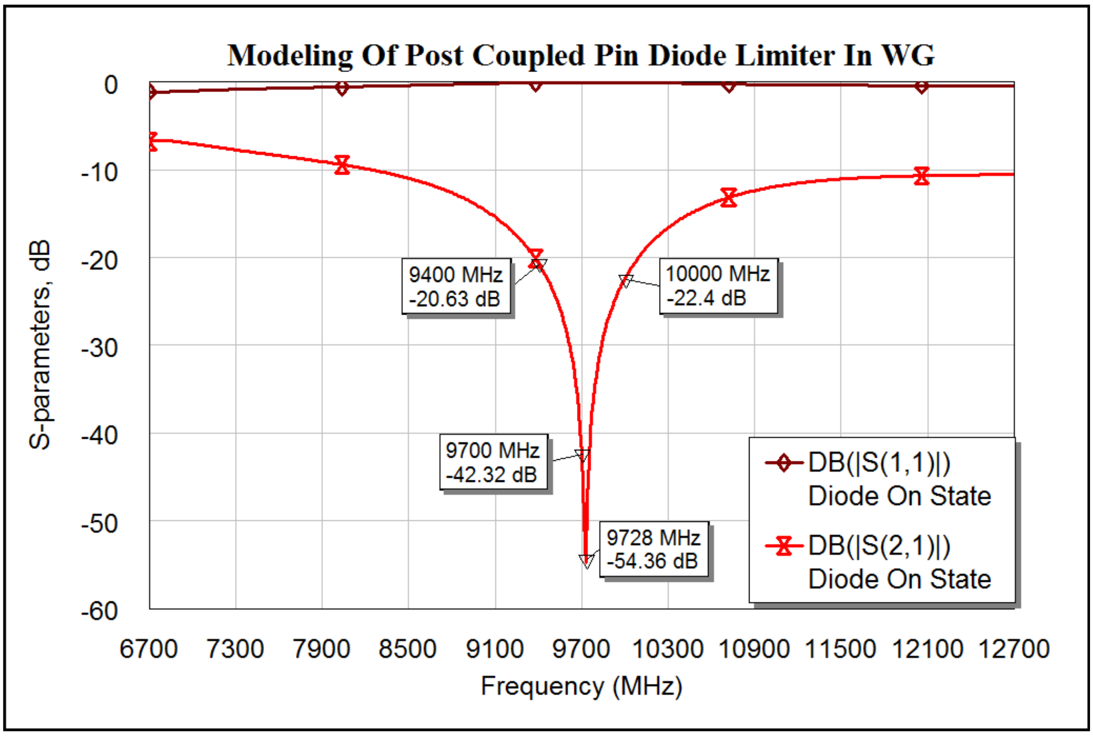

Figure 3.27: AWR Simulation Result which Shows S-parameter Of Limiter at ON State

3.2.6. Post Coupled Pin Diode Waveguide Limiter in CST

After performing ideal linear simulations in AWR MWO, realistic 3D EM linear simulations should be performed before production of the mechanical structures. CST co-simulation tool is used to simulate whole structure including the lumped model of pin diode. Lumped pin diode model is defined in co-simulation via discrete port. Whole structure, which is drawn in CST, is shown in Figure 3.28.

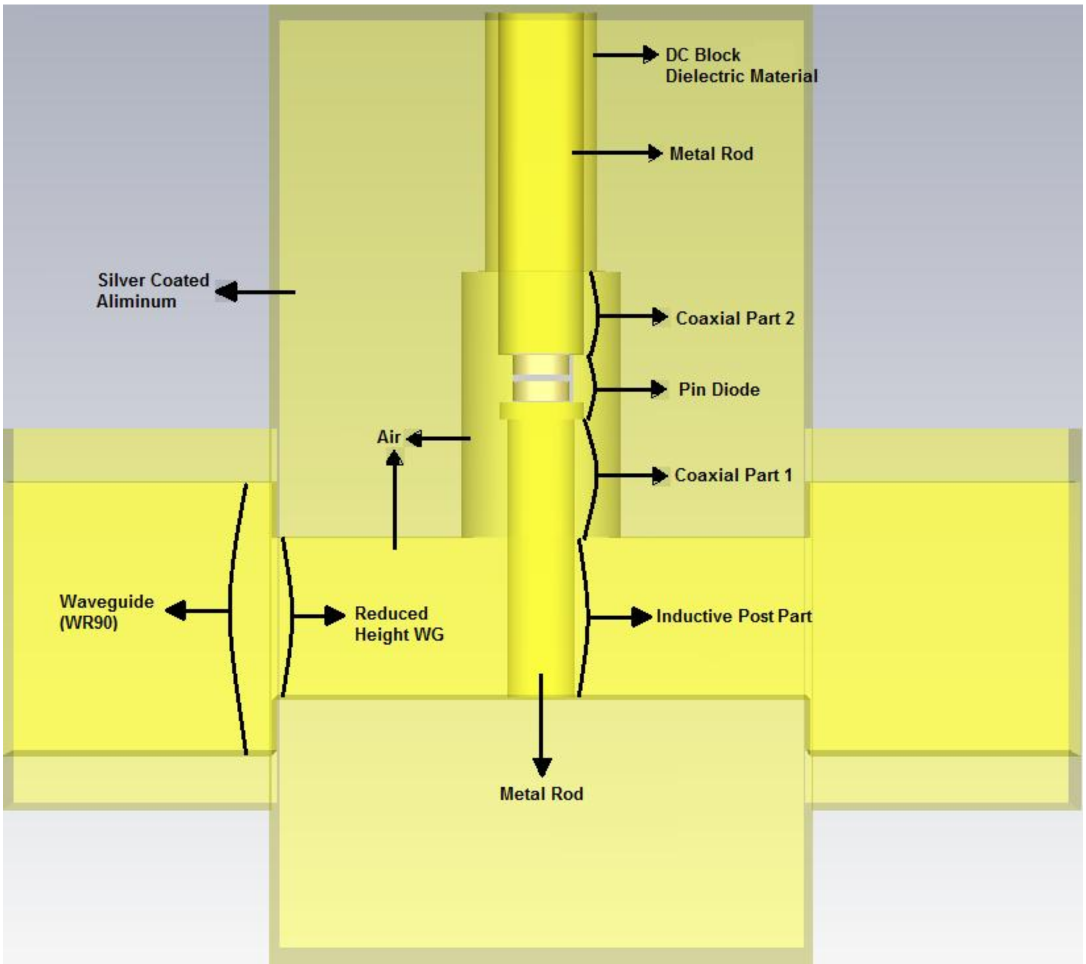

Figure 3.28: Side View of WG Limiter in CST

As can be seen in Figure 3.28; WR90 waveguide, reduced height waveguide, inductive post, coaxial parts and pin diode compose the waveguide limiter. In order to bias pin diode, DC block material PVDF (heat shrinkable tube) is used. Its 0.2 mm thickness is sufficient to create big capacitive effect which shows RF ground effect. In design of WG limiter, silver coating is preferred because of its low loss nature for microwave signals. Conductivity of silver is 6.3e7 S/m and conductivity of gold is 4.1e7 S/m. Silver is better than gold for low loss performance.

The ports of waveguide limiter are shown in Figure 3.29. There are three ports. Port 1 and Port 2 are input and output ports which are defined as waveguide port in CST. Port 3 is discrete port which is used for pin diode lumped modeling. The co-simulation schematic which combines 3D structure with lumped components is shown in Figure 3.30. Since the pin diode package is drawn and the capacitive effect of package can be created by CST, package capacitance of pin diode is not put on schematic.

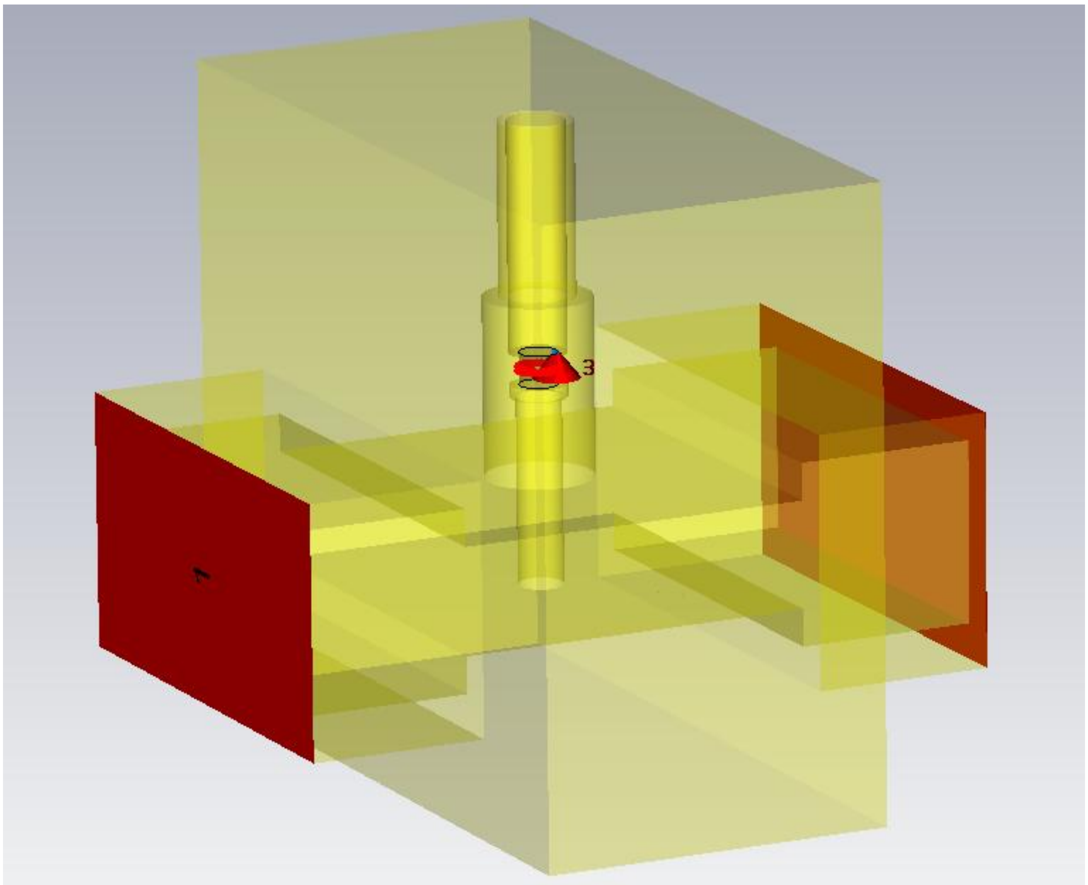

Figure 3.29: Representation of WG Limiter Ports in CST

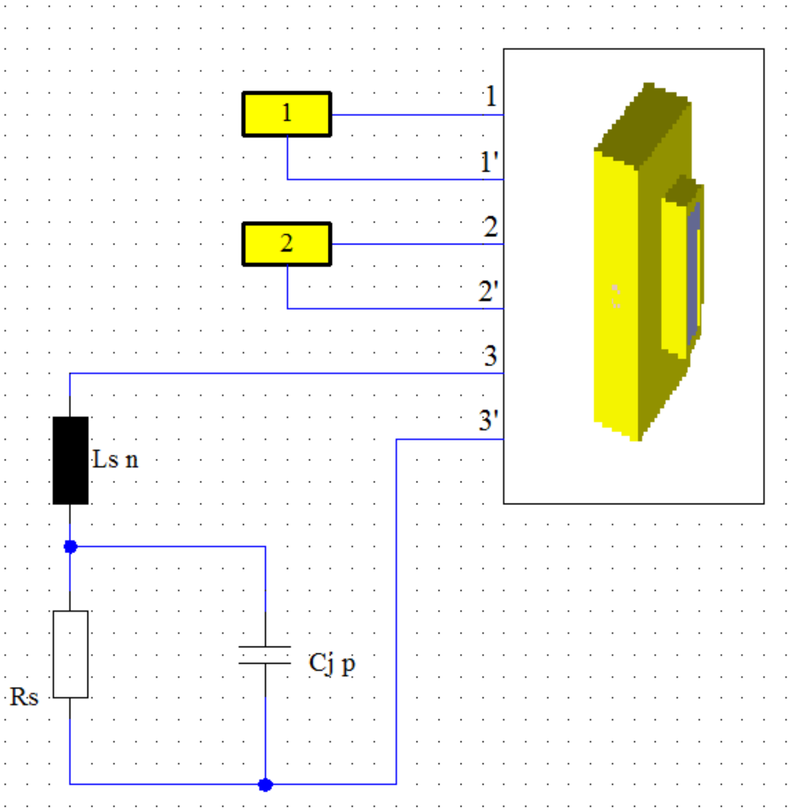

Figure 3.30: CST Co-Simulation Schematic which Shows Combination of 3D Structures and Lumped Components of WG Limiter

At the beginning, parameter values of the WG limiter are taken from AWR MWO which gives desired simulation results. However the taken values are tuned in CST. Height and length parameter of the reduced height waveguide remain same with AWR MWO simulation but impedance and length of the coaxial parts are changed slightly. After tuning process is completed, co-simulation shows the desired results. The final values of parameters in CST are shown in Table 3.7. Simulation result for pin diode OFF state is shown in Figure 3.31 and ON state is shown in Figure 3.32.

Table 3.7: WG Limiter Components' Values in CST

a,a_dar (mm)	b (mm)	b_dar (mm)	l_dar_gir (mm)	d (mm)	el1 (degree)	z1 (Ω)	el2 (degree)	z2 (Ω)
22.86	10.16	6	10	2.5	51.26	52.49	36.11	37.69

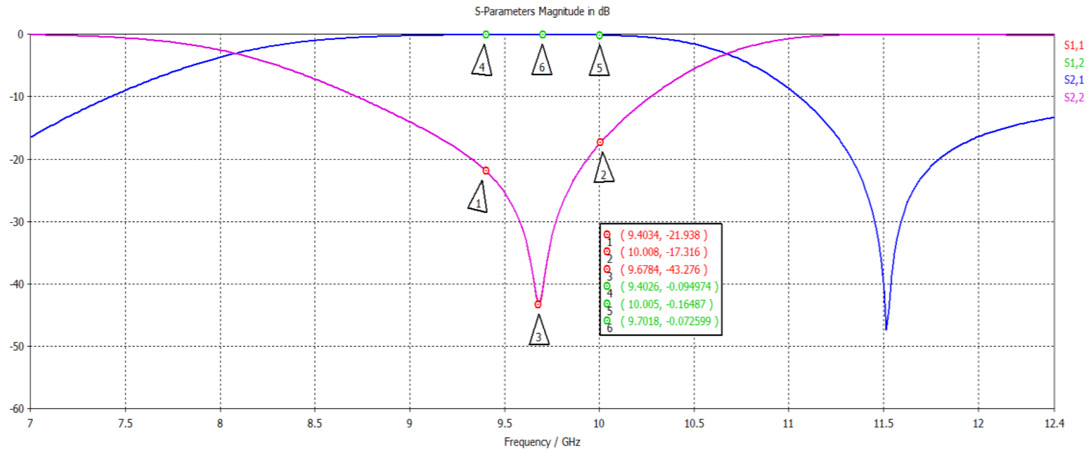

Figure 3.31: S-parameter of WG Limiter OFF State in CST

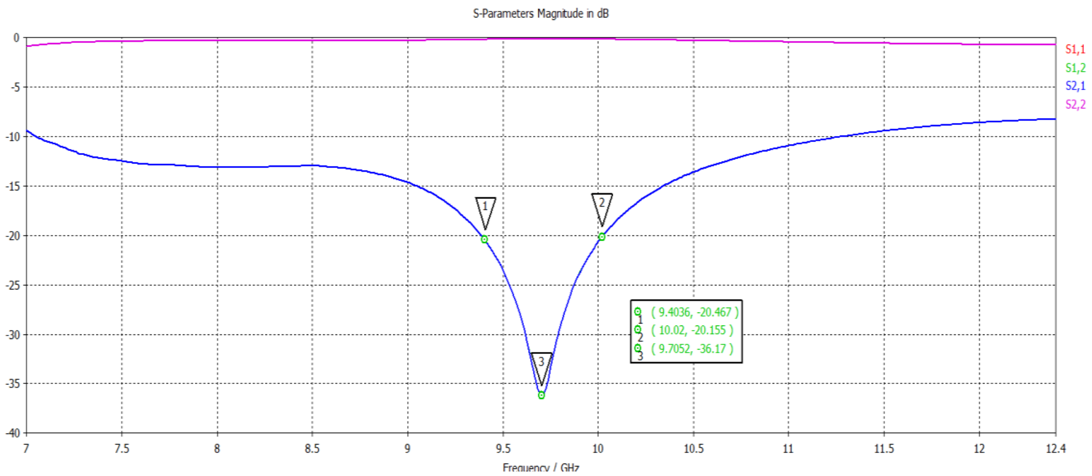

Figure 3.32: S-parameter Of WG Limiter ON State in CST

AWR and CST simulation results for both of the pin diode states are compared. The comparison graph for OFF state pin diode limiter is shown in Figure 3.33. AWR and CST simulation results get closer to each other after slight tuning is made in CST. Due to realistic simulation in CST, the impedance matching bandwidth is narrower and insertion loss is higher than AWR simulation result. The frequency difference of return loss notches is about 90 MHz. This difference is not abnormal because of tuning process. Notch of return loss can be tuned by slightly changing the coaxial parts’ length and impedances.

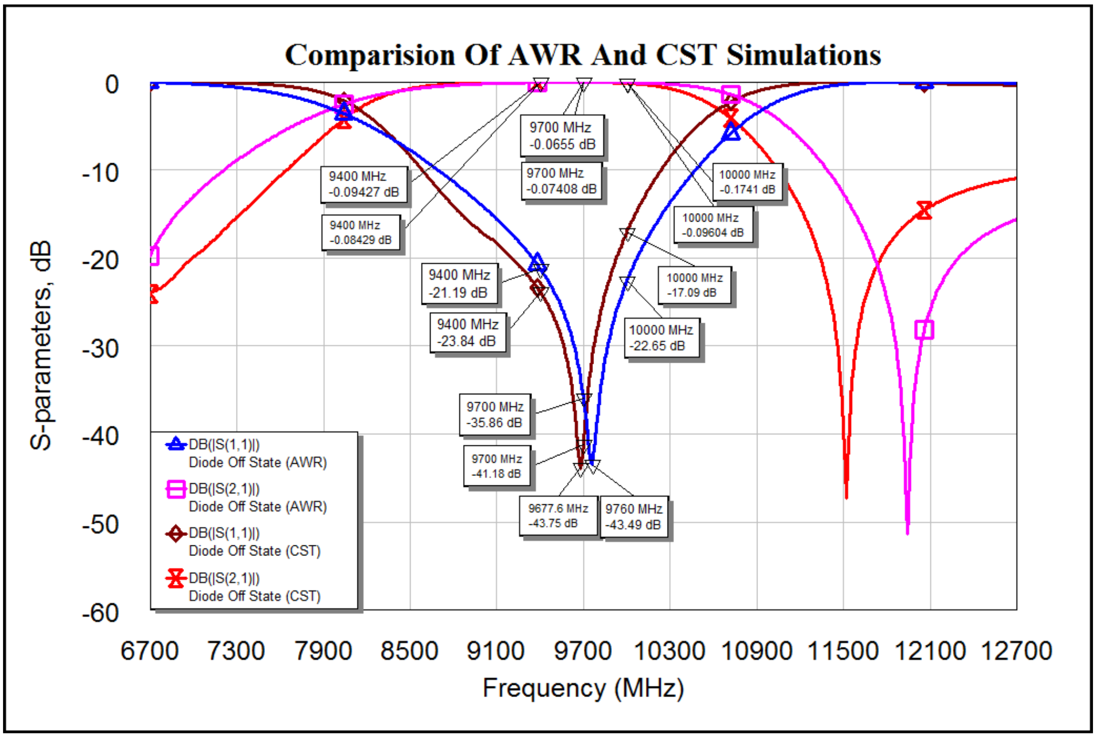

Figure 3.33: Comparison between AWR and CST Simulations of Limiter at OFF State

The comparison graph for ON state of pin diode is shown in Figure 3.34. Isolation level of pin diode limiter in AWR simulation is higher. The reason of this difference is that CST simulation is more realistic and it results in higher loss.

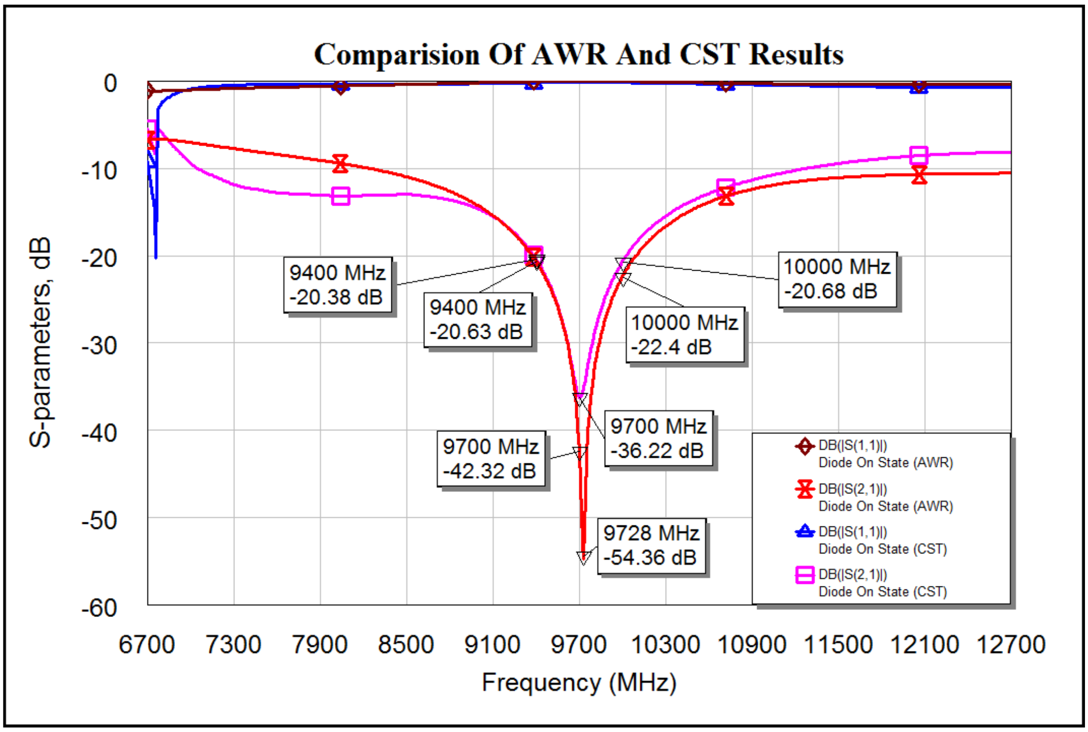

Figure 3.34: Comparison between AWR and CST Simulations of WG Limiter at ON State

3.2.7. Combining WG Limiter and WG Detector in AWR MWO

After design of the WG limiter and the WG detector are completed, the effect of detector on limiter is analyzed in AWR MWO via nonlinear simulation. When the coupled power is increased, detected voltage level increases so that the sensitivity of pin diode limiter increases with increasing bias voltage. Pin diode limiting level gets higher for same input power level. The schematic which combines detector and limiter is shown in Figure 3.35. The simulations are performed for different coupling values and input power is swept from -20 to 60 dBm. Large signal S-parameters are acquired as the result of the simulations; simulation results are shown in Figure 3.36. Some of the points in the simulations are not completed because of a convergence problem of the simulator. The transparency of the resultant curves in the graph is because of this problem.

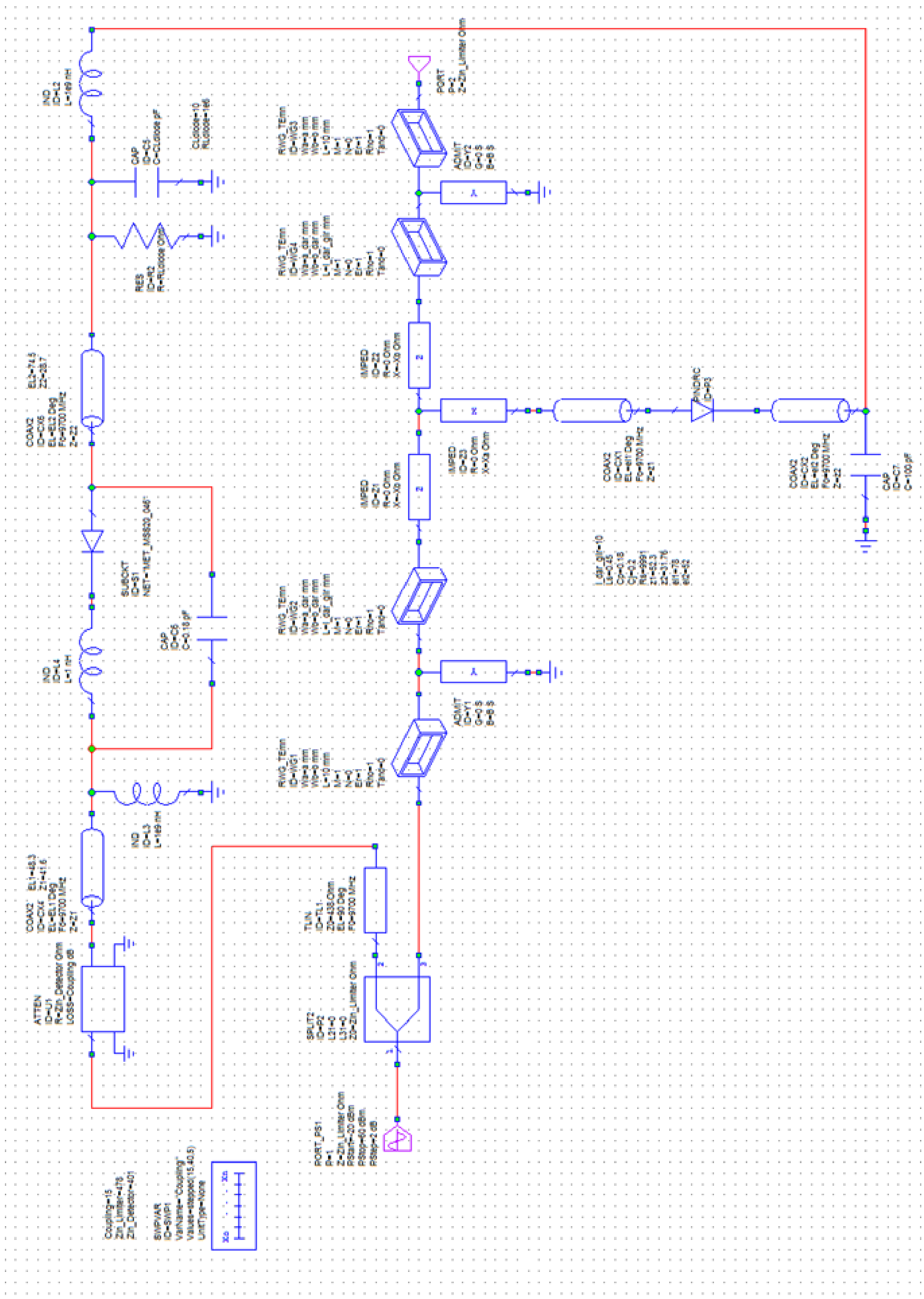

Figure 3.35: AWR Schematic which Combines Limiter and Detector

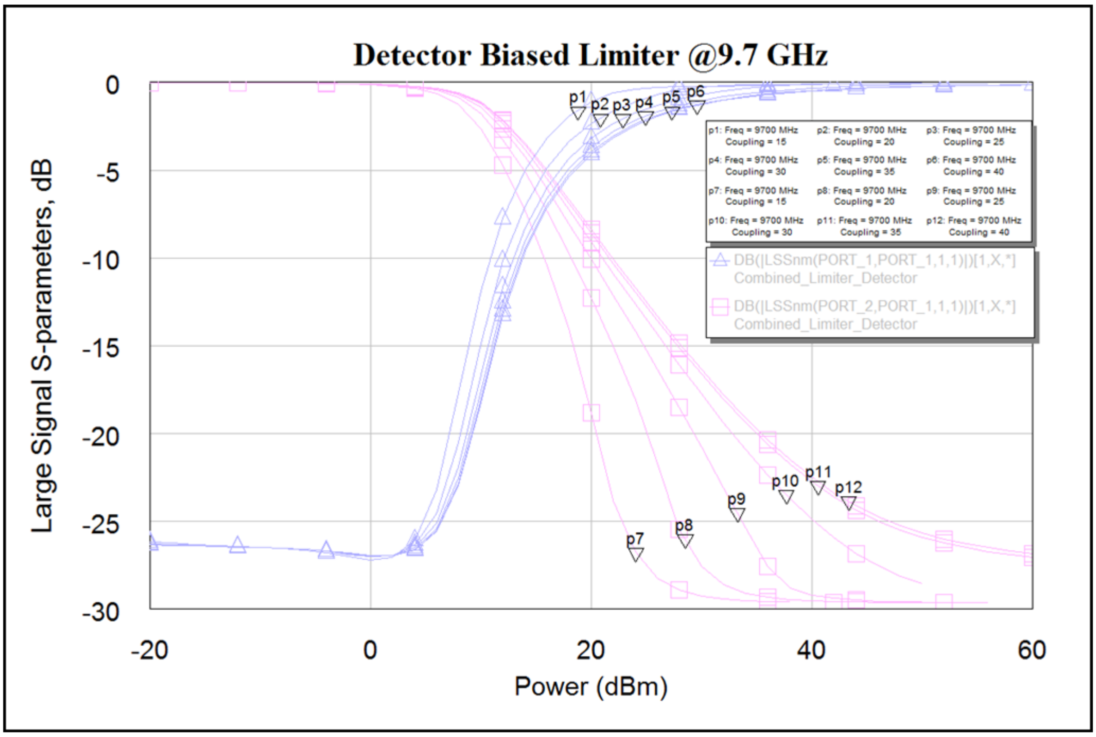

Figure 3.36: AWR Simulation Result which Shows Large Signal S-parameter of Detector Biased Limiter

CHAPTER 4

WAVEGUIDE LIMITER AND WAVEGUIDE DETECTOR FABRICATIONS AND MEASUREMENTS

In Chapter 3, the waveguide detector and the waveguide limiter are designed, their simulation results are shown and desired simulation results are acquired. WG detector and WG limiter are mechanical devices because of the nature of WG. 3D EM simulations are performed to clarify the dimensions of mechanical components. Also, mechanical tolerances are considered in EM simulations. In other words, EM simulations are the last effort to determine the dimensions and end of the design procedure before fabrication of the devices. According to 3D step files, which are exported from CST, the devices are prepared for manufacturing in mechanical CAD software. The produced components will be shown and how the structures are made will be explained in this chapter. After the explanations on the basic fabricated parts, the fabrication of WG detector and WG limiter are going to be shown and explained. After fabrication part, linear and nonlinear measurements of the WG detector and the WG limiter, and the measurement setup requirements are going to be shown and explained.

4.1. FABRICATION OF WG DETECTOR AND WG LIMITER

4.1.1. Fabrication of WG Detector

The purpose of the WG detector is to bias the WG limiter. WG detector must be adaptable to WG limiter. The mechanical structures are manufactured according to this requirement. All of the produced components are shown in Figure 4.1.

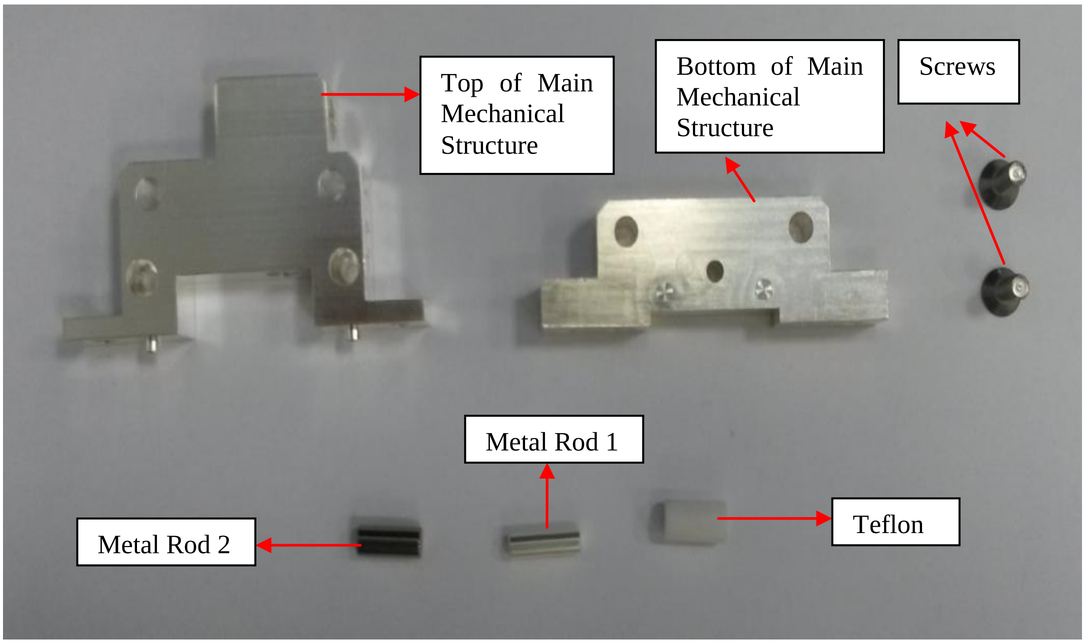

Figure 4.1: Produced Components of WG Detector

Metal rod 1 and 2 are the center metal of coaxial part 1 and 2, which are shown in design chapter. Metal rod 2 is put inside of dielectric material Teflon. As mentioned in earlier chapter, the reason for not selecting air as dielectric filler for coaxial part 2 is that Teflon is solid and this solidness helps the whole coaxial structure to be fixed inside the metal body. Metal rod 2 with dielectric material Teflon, Schottky diode and metal rod 1 are shown in Figure 4.2. Schottky diode is attached to metal rod 1 and metal rod 2 with conductive epoxy. The whole coaxial part; whose components are metal rod 1, Schottky diode and metal rod 2; is inserted to hole as shown in Figure 4.3 and Figure 4.4.

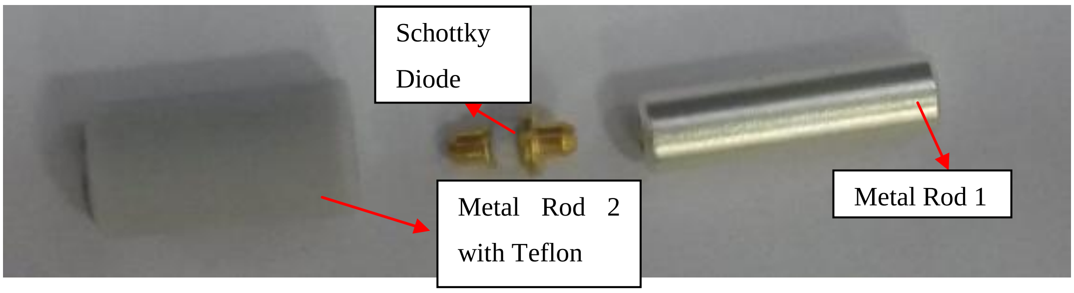

Figure 4.2: Coaxial Part Components

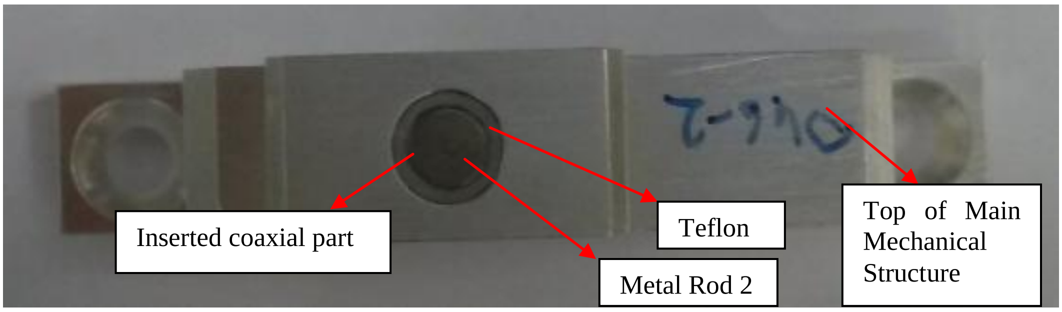

Figure 4.3: Top View of Inserted Coaxial Part

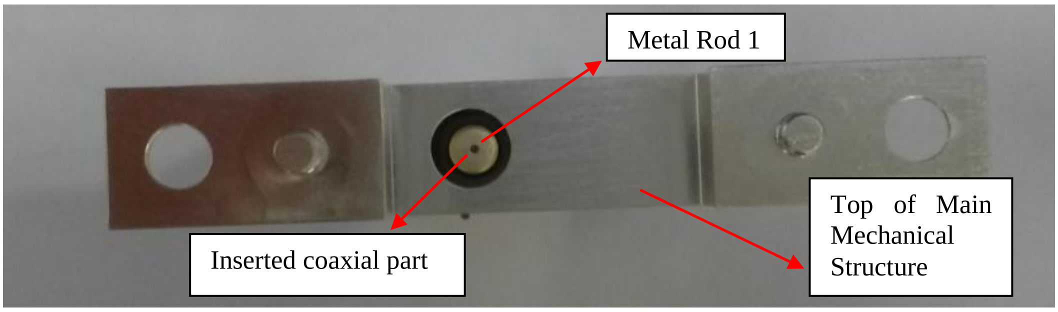

Figure 4.4: Bottom View of Coaxial Part

After insertion of whole coaxial part to hole is completed, one side of the coupling loop is attached to metal rod 1 and the other side is attached on inner surface of top main mechanical structure with conductive epoxy as shown in Figure 4.5.

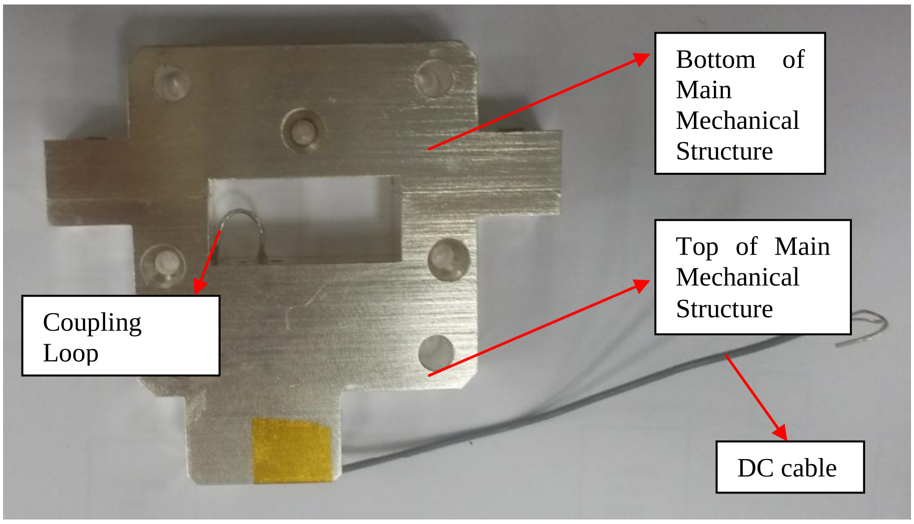

Figure 4.5: Cross Sectional View of WG Detector

After attachment of the coupling loop is completed; lumped components, which are capacitor and resistor, are attached to end of the coaxial part 2 with conductive epoxy. In order to transfer the detected voltage to pin diode limiter for biasing, dc cable is attached on end of the coaxial part 2 with conductive epoxy too. The pictures are shown in Figure 4.6 and Figure 4.7.

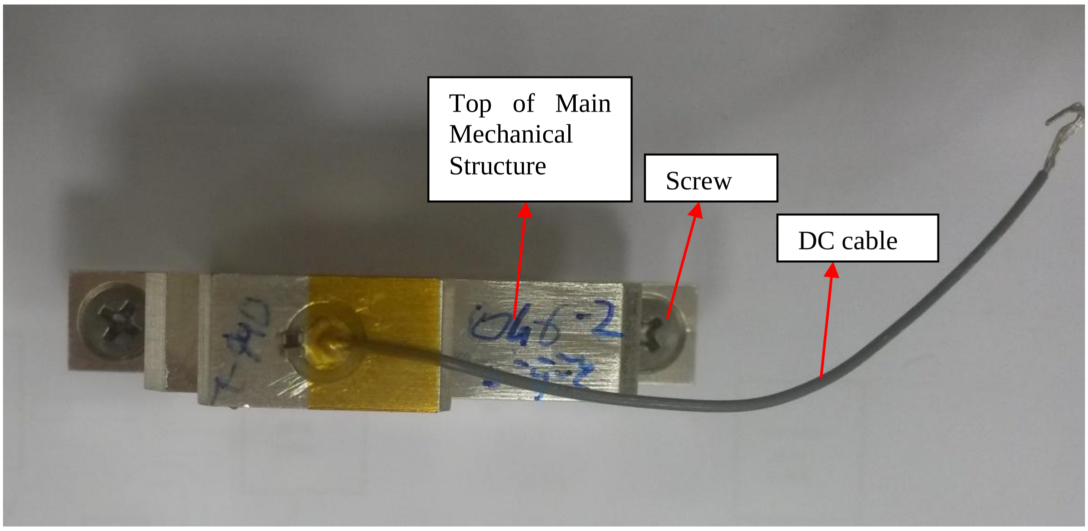

Figure 4.6: Top View of WG Detector

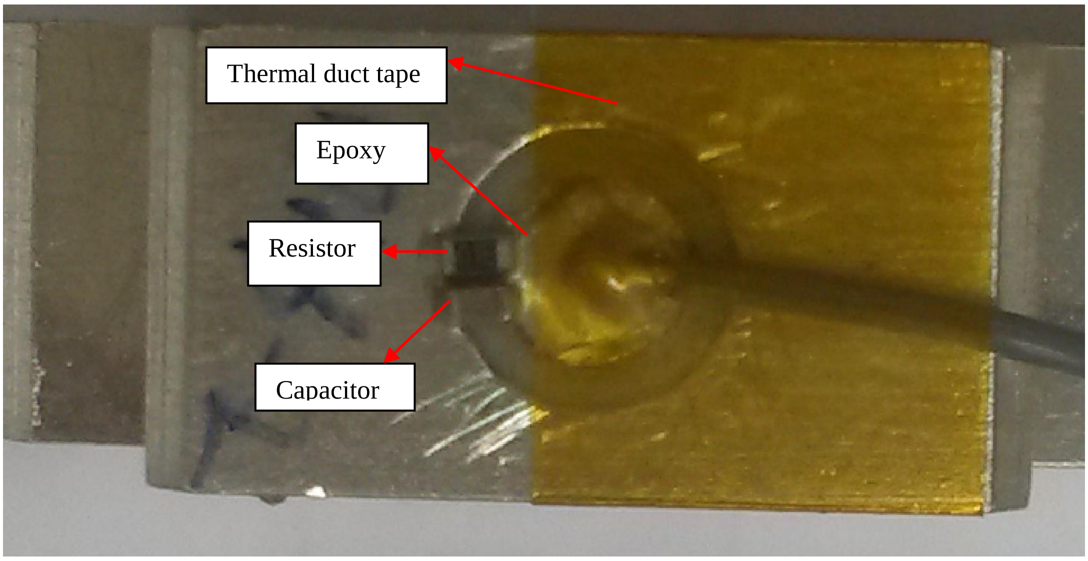

Figure 4.7: Zoomed Top View of WG Detector

4.1.2. Fabrication of WG Limiter

All of the components of the WG limiter are shown in Figure 4.8. In the bottom view of the main mechanical structure, step of the reduced height WG can be seen. The cylindrical hole for the coaxial part can be seen in the top view of the main mechanical structure. Metal rod 1 includes both the inductive post and the coaxial part 1, which are described in the design chapter. Metal rod 1 has a threaded section which enables mechanical movement for tuning the electrical performance. Also, “sliding ground” can be used for tuning process. Metal rod 2 is the center metal of the coaxial part 2 which is described in the design chapter. Heat shrinkable tube is used to coat metal rod 2 for DC blocking.

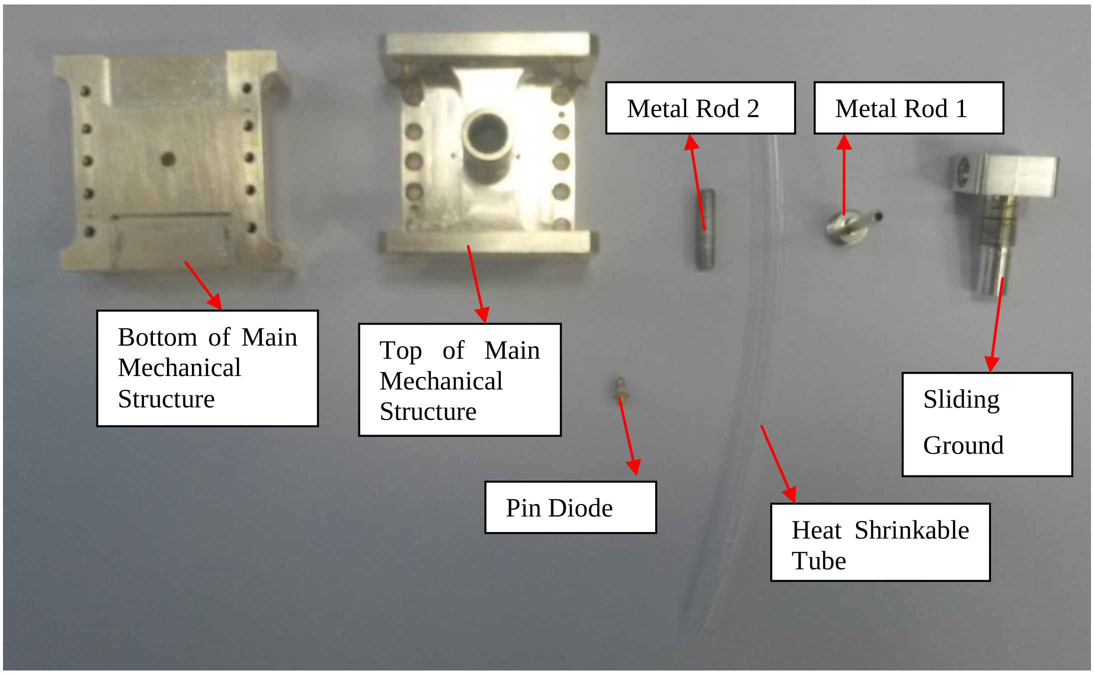

Figure 4.8: Produced Components of WG Limiter

Metal rod 1 and sliding ground are screwed to mechanical structures as shown in Figure 4.9. After screwing Metal rod 1 to bottom mechanical structure; metal rod 1, pin diode and metal rod 2 which is coated with tube are attached with conductive epoxy as shown in Figure 4.10.

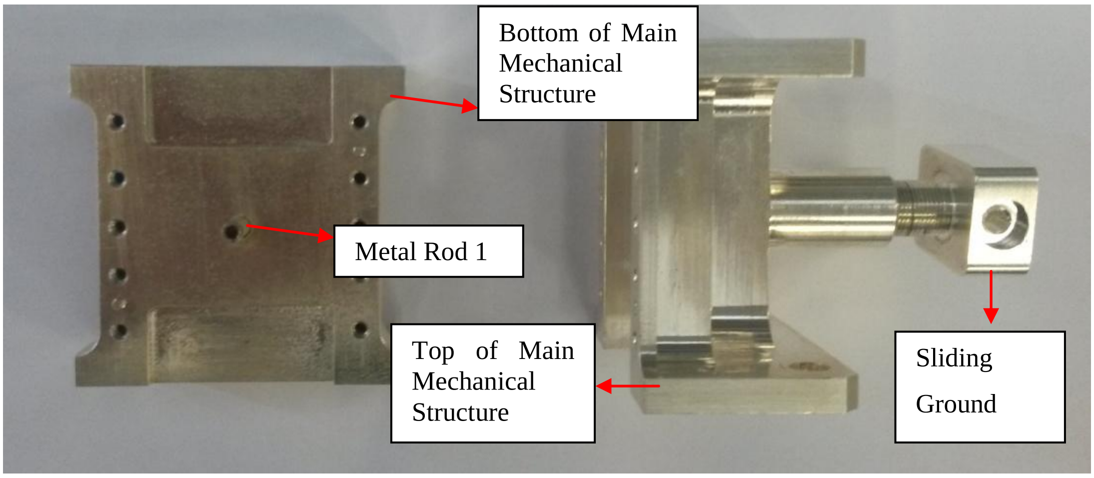

Figure 4.9: Top and Bottom Parts of WG Limiter

The coaxial part is composed of metal rod 1, 2 and diode as shown in Figure 4.10. Since metal rod 1 has screwing function, the length of coaxial part 1 can be tuned. However this screwing affects the length of coaxial part 2. When the coaxial part 1 length is increased, the length of coaxial part 2 decreases. In addition to this screwing, independent screwing is necessary for tuning of coaxial part 2. Sliding ground can slide around of the metal rod 2, which is center metal of coaxial part 2. Sliding ground is independent screwing which enables tuning of coaxial part 2. When coaxial part 1 length is increased, sliding ground should be screwed backward to keep the length of coaxial part 2 fixed. Namely, two independent screwing mechanisms are designed for tuning of WG limiter.

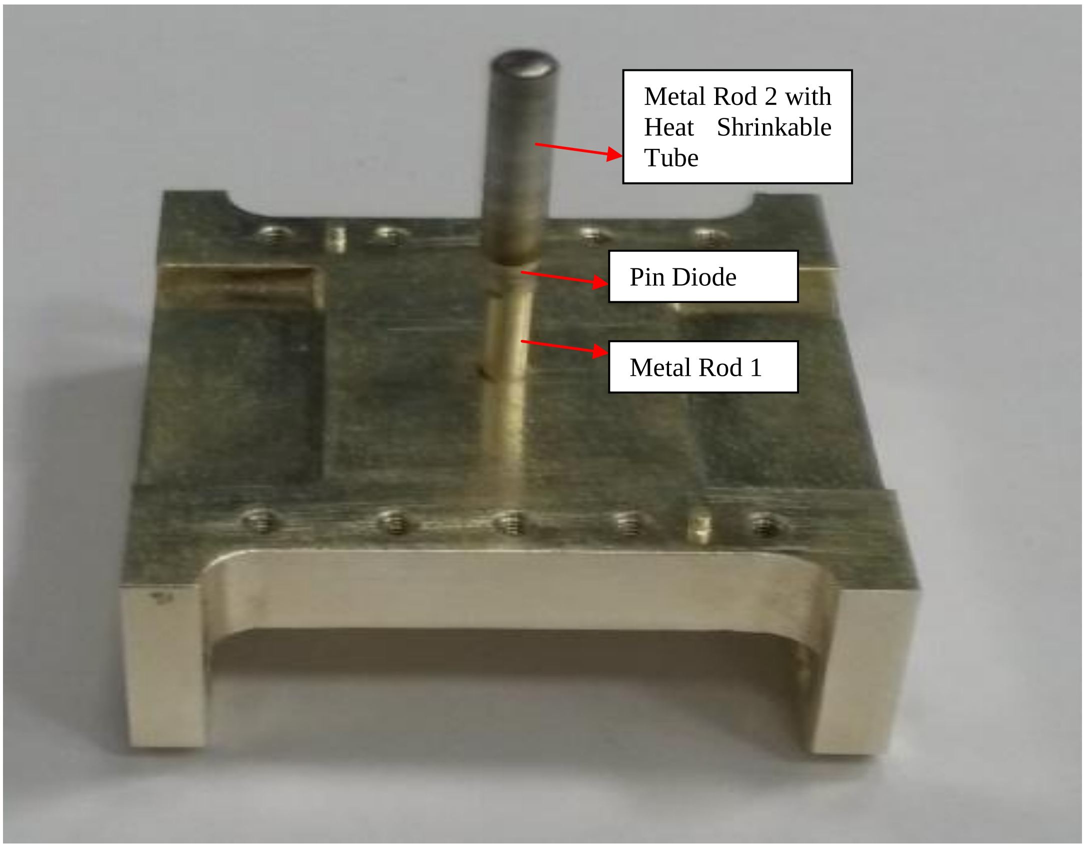

Figure 4.10: Coaxial Part of WG Limiter

After all integration is completed, WG limiter is shown in Figure 4.11. For safety purposes, metal duct tape is used to prevent possible RF leakages during the high power measurements. DC cable is attached to the top of coaxial part 2 with conductive epoxy to get detected voltage from WG detector.

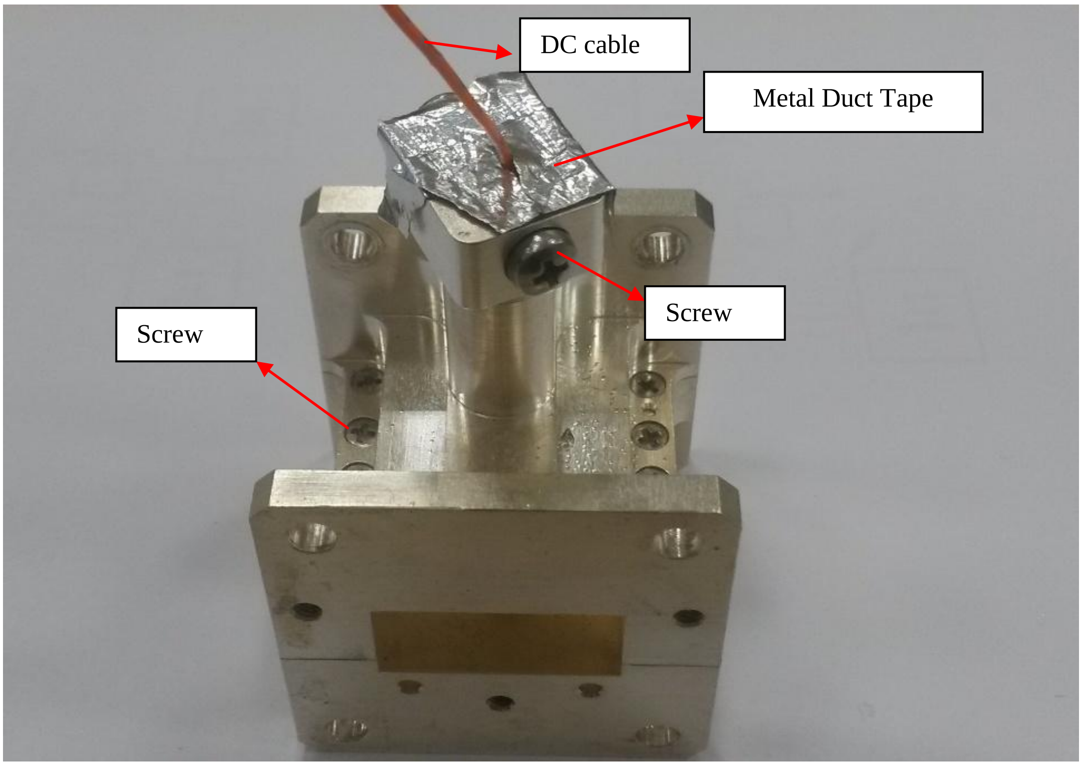

Figure 4.11: WG Limiter whose Fabrication is Completed

4.2. MEASUREMENTS OF WG DETECTOR AND WG LIMITER

After fabrication process is completed, devices are measured under small signal and large signal conditions. Insertion loss, isolation level, high power limiting level and response time are the crucial parameters for evaluating the measurement results. Measurement results of the limiters having different diodes and the limiters with and without the detector are compared.

4.2.1. Small Signal S-Parameter Measurements

First of all, small signal S-parameters of the WG limiters are measured with using network analyzer to observe the insertion loss of the WG limiters with different diodes which are MLP7110 and MLP7120. Linear measurements of the WG limiters are made for both states of pin diode. After single stage limiters' measurements are completed, the WG limiter with MLP7120 pin diode and the WG limiter with

MPL7110 pin diode are connected in cascade. The linear measurements of two stage WG limiter are performed. Then WG detector is connected to WG limiter, the added insertion loss by WG detector is observed and from added loss the coupling in WG detector is calculated.

4.2.1.1. Measurements of WG Limiter with MLP7120 Pin Diode

Small signal S-parameters of WG limiter with MLP7120 pin diode are shown in Figure 4.12 and Figure 4.13. These responses are acquired after tuning process. Coaxial parts’ lengths are adjusted for optimum performance. In Figure 4.12, OFF state response is shown. Return loss values are higher than 14 dB in 9.4-10 GHz frequency band and higher than 20 dB at the center of the band. The insertion loss values are under 0.62 dB in 9.4-10 GHz frequency band and under 0.46 dB at the center of the band. In Figure 4.13, the ON state response is shown. WG limiter is biased to turn on the pin diode. The S-parameters of the WG limiter is measured at bias currents 2 mA, 5 mA and 7 mA. As it seen in figure, insertion loss of the limiter gets higher when the current is increased. Insertion loss or isolation value is less than 20 dB in 9.4-10 GHz frequency band, is less than 28 dB at the center of the band. The interchange off the S_{11} and S_{21} is shown in the graphs when the pin diode state is changed.

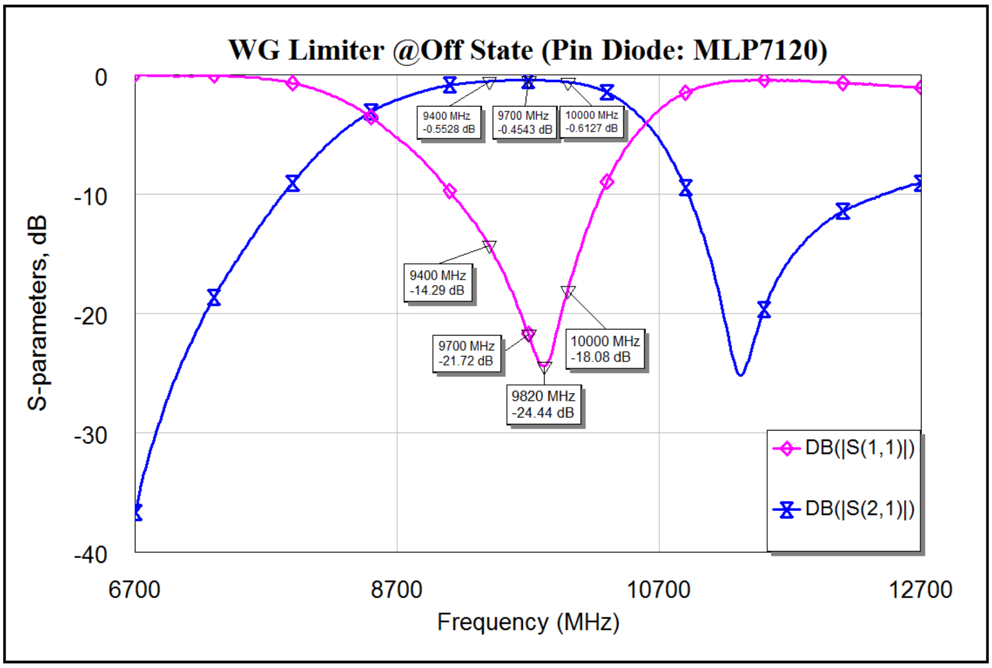

Figure 4.12: S-parameter Of WG Limiter with MLP7120 Pin Diode at OFF State

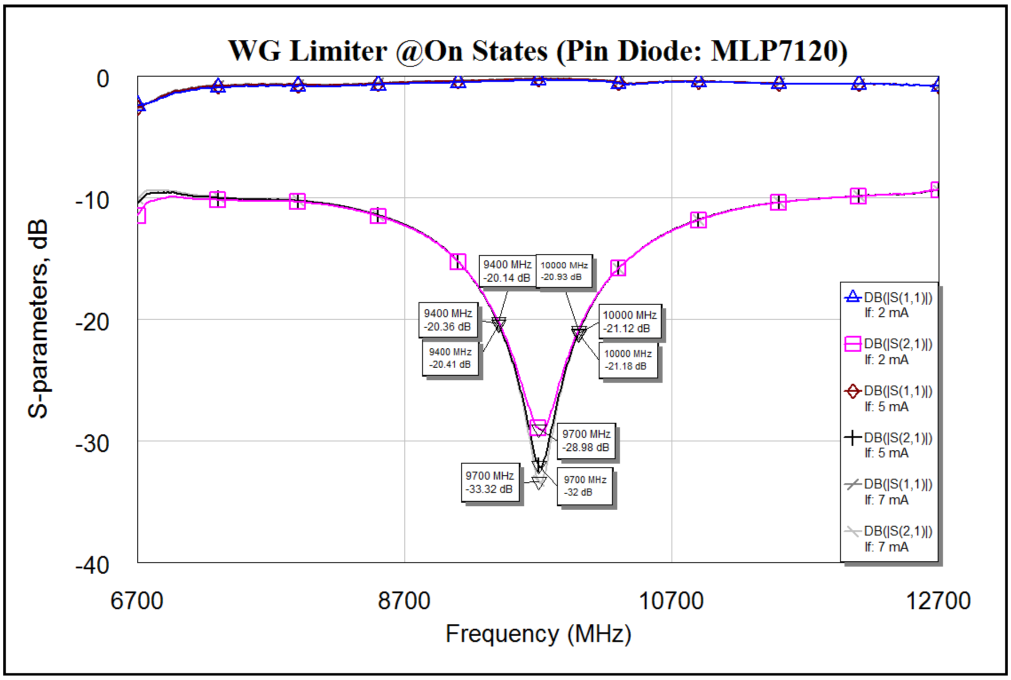

Figure 4.13: S-parameter Of WG Limiter with MLP7120 Pin Diode at ON State

4.2.1.2. Measurements of WG Limiter with MLP7110 Pin Diode

Small signal S-parameters of WG limiter with MLP7110 pin diode are shown in Figure 4.14 and Figure 4.15. Like WG limiter with pin diode MLP7120, these responses are acquired after tuning process. Coaxial parts’ lengths are adjusted for optimum performance. In Figure 4.14, OFF state response is shown. Return loss values are higher than 12 dB in 9.4-10 GHz frequency band and higher than 16 dB at the center of the band. The insertion loss values are under 0.58 dB in 9.4-10 GHz frequency band and under 0.44 dB at the center of the band. In Figure 4.15, the ON state response is shown. WG limiter is biased to turn on the pin diode. The S-parameter of the WG limiter is measured at bias currents 2 mA, 5 mA and 7mA. As it is seen in figure, like the WG limiter with MLP7120 diode, insertion loss of the limiter gets higher when the current is increased. Insertion loss or isolation value is less than 16 dB in 9.4-10 GHz frequency band, is less than 25 dB at the center of the band. The interchange of the S_{11} and S_{21} is shown in the graphs when the pin diode state is changed.

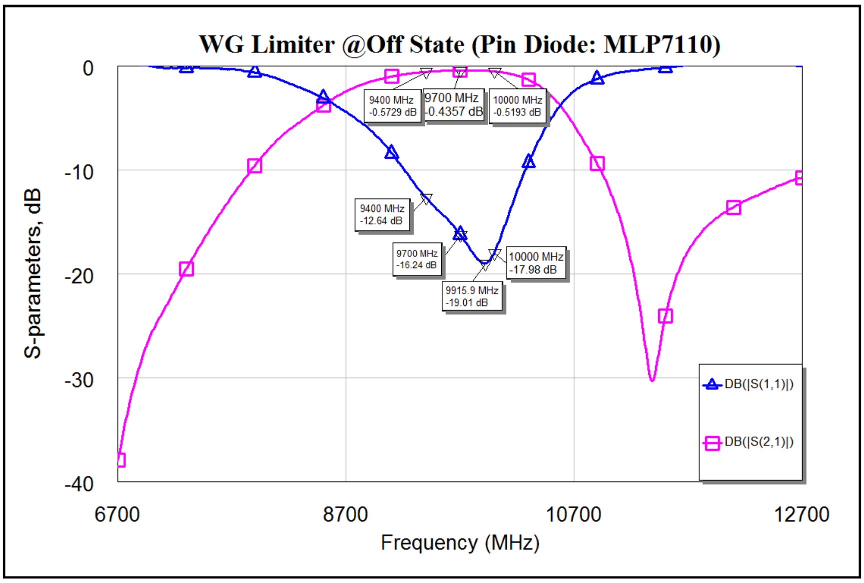

Figure 4.14: S-parameter Of WG Limiter with MLP7110 Pin Diode at OFF State

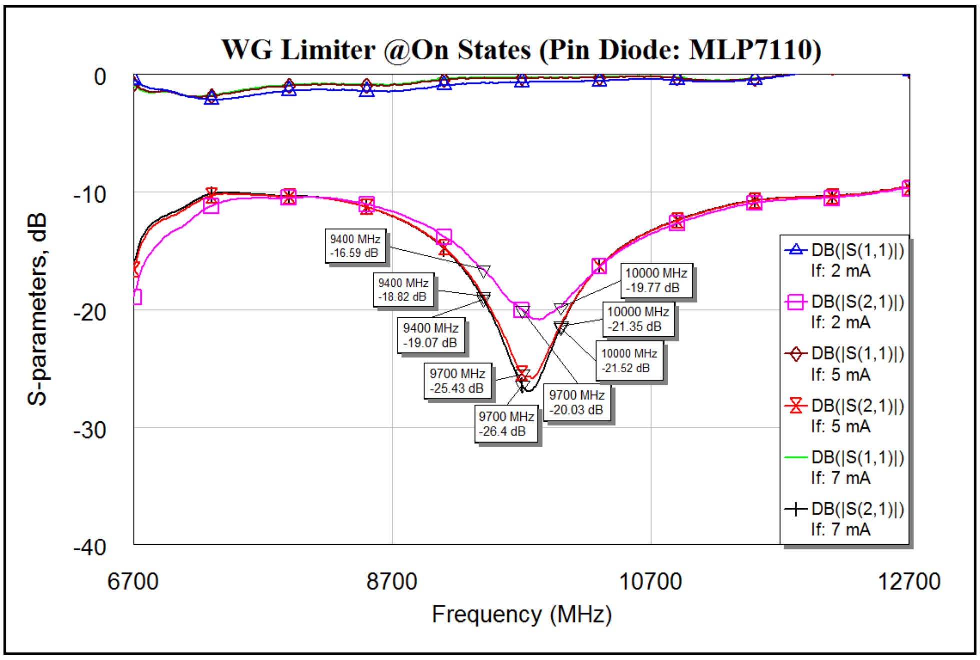

Figure 4.15: S-parameter Of WG Limiter with MLP7110 Pin Diode at ON State

4.2.1.3. Comparison between Simulations and Measurements

In Figure 4.16 and Figure 4.17, the measurement results of the WG limiters with MLP7120 and MLP7110 diodes; the CST simulation result are shown in the same graphs for the cases in which the pin diode state is ON and OFF. Measurement results, where diode is in OFF state, show that insertion loss is greater and bandwidth is narrower in comparison to the simulation results. Insertion loss and impedance matching bandwidth of the WG limiters with MLP7120 and MLP7110 pin diodes are close to each other. The WG limiter with MLP7120 has a better impedance matching than that of WG limiter with MLP7110 diode. Due to ideal components in the simulations, matching results of the measurements are worse, as expected. For the diode ON state, WG limiter with MLP7120 diode has better isolation than the one with MLP7110 diode. Isolation levels of the measurements are worse than simulation results, as expected.

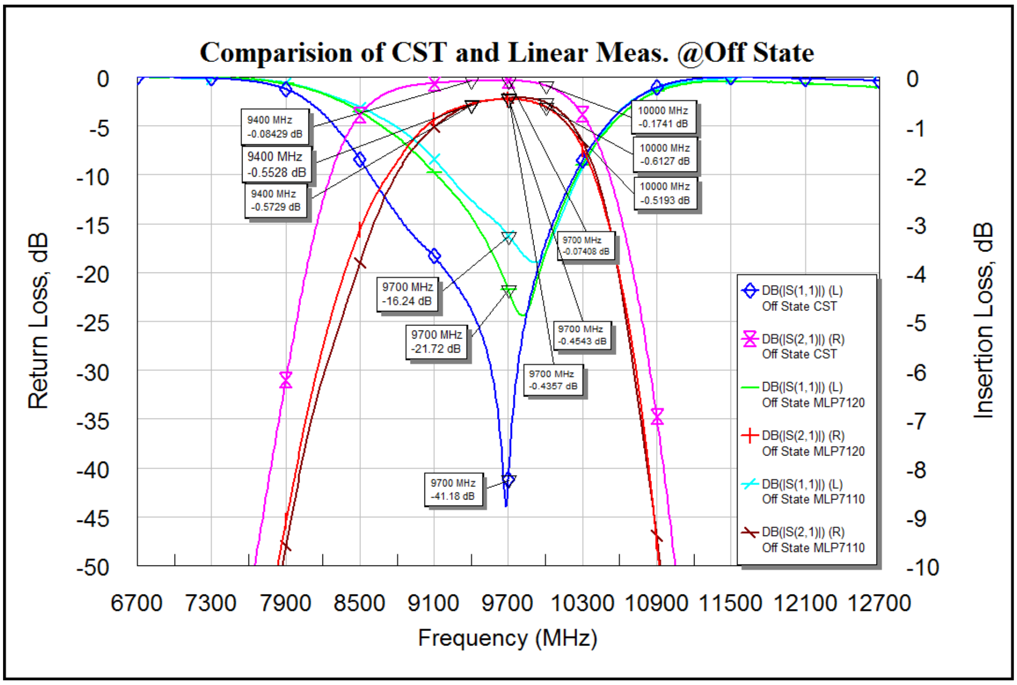

Figure 4.16: Comparison of CST Simulation and Measurements at OFF State

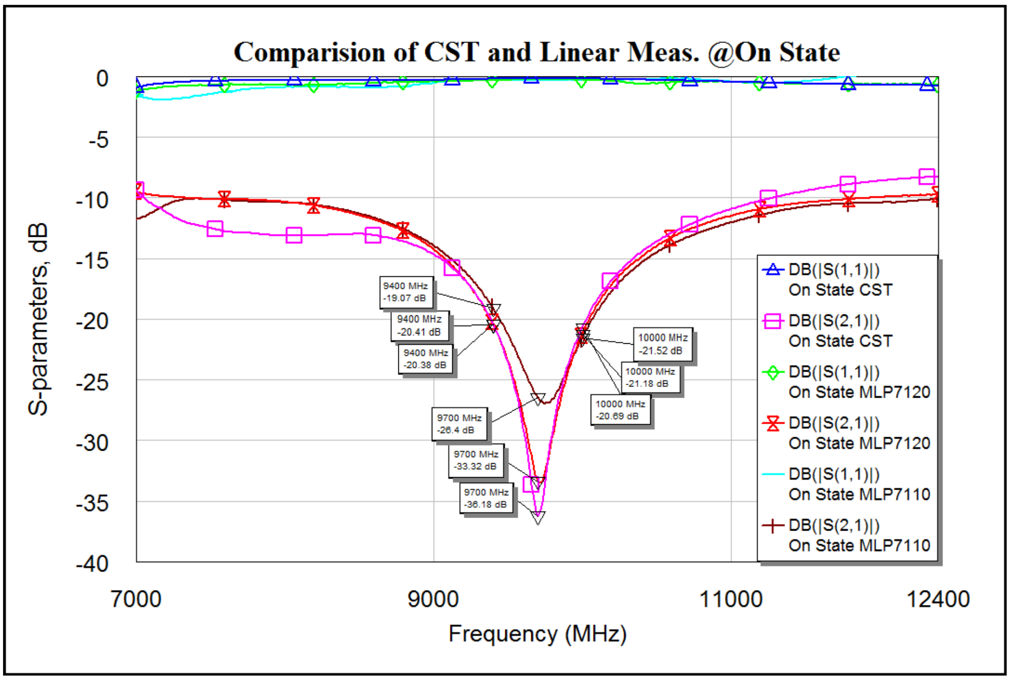

Figure 4.17: Comparison of CST Simulation and Measurements at ON State

4.2.1.4. Measurements of Two Stage WG Limiter

In Figure 4.18, the WG limiters and the WG detector are cascade connected. Small signal S-parameters of two stage WG limiters with MLP7110 and MLP7120 pin diodes are shown in Figure 4.19 and Figure 4.20. Tuned WG limiters are directly connected and post-connection tuning is not performed.

Actually, main purpose of the thesis was to understand the single stage limiters. After the observation of good impedance matching performances of single stage limiters, the performance of two stage WG limiter is examined. Electrical distance is important between the WG limiters for good impedance matching results for two stage limiter. As mentioned earlier, at the beginning, this parameter is not taken into consideration. In Figure 4.19, OFF state response is shown. Return loss values are higher than 13 dB in 9.4-10 GHz frequency band and higher than 18 dB at the center of the band. The insertion loss values are less than 1.4 dB in 9.4-10 GHz frequency band and under 0.84 dB at the center of the band. In Figure 4.20, the on state response is shown. Two stage WG limiter is biased to turn on the pin diodes. The S-parameter of the two stage WG limiter is measured at bias current 9 mA. Insertion loss or isolation level is less than 30 dB in 9.4-10 GHz frequency band and above 54 dB at the center of the band. The discontinuity occurs at S_{21}. The reason of this can be unwanted mode in WG. If this can be eliminated, isolation will be less than 40 dB in 9.4-10 GHz frequency band. There will be an effort to get rid of this problem. The interchange off the S_{11} and S_{21} is shown in the graphs when the pin diode state is changed.

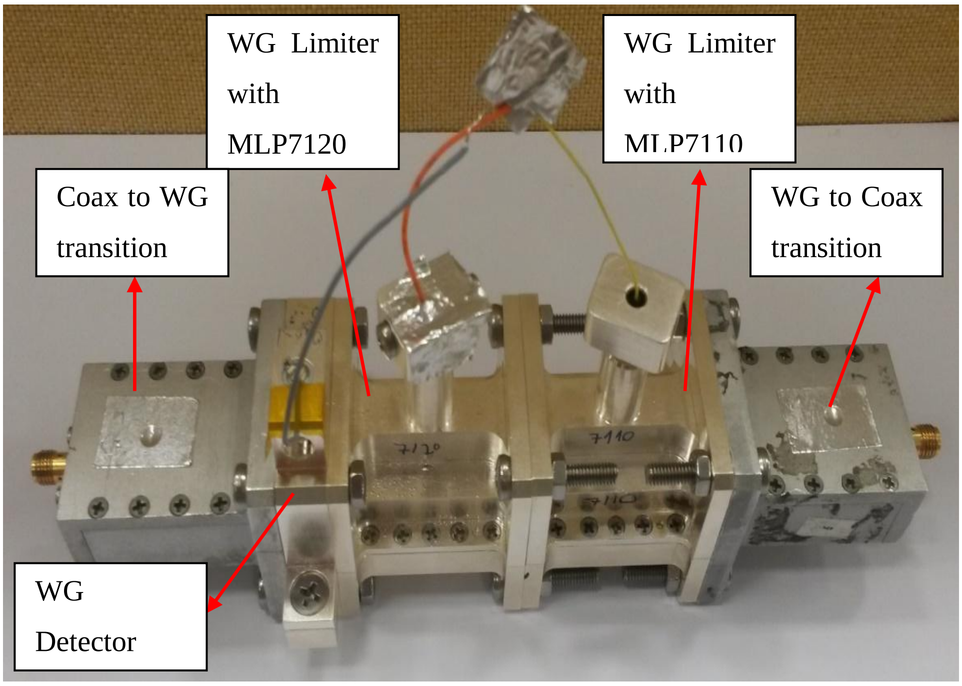

Figure 4.18: Two Stage WG Limiter with WG Detector

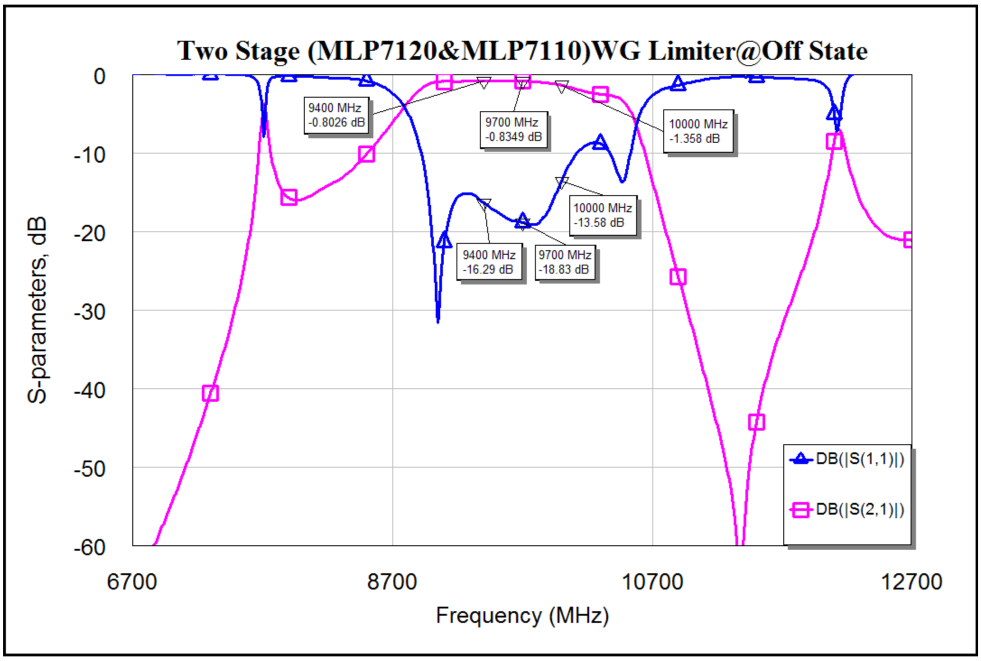

Figure 4.19: S-parameter Measurement of Two Stage WG Limiter at OFF State

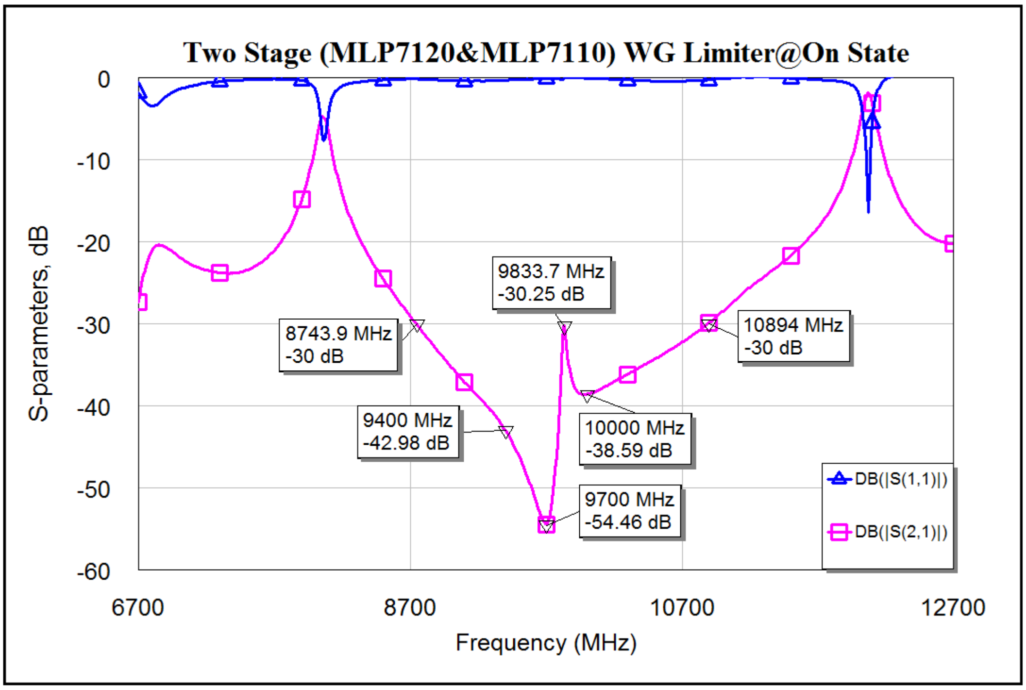

Figure 4.20: S-parameter Measurement of Two Stage WG Limiter at ON State

4.2.1.5. Measurement of WG Detector

Single stage WG limiter with pin diode MLP7120 is measured with and without WG detector and it is shown in Figure 4.21. The difference between insertion losses equals to insertion loss of WG detector. Difference is about 0.05 dB at the center frequency. The length of WG detector is not long to see this loss. Reason of this loss is coupling loop mechanism. Coupling level can be calculated from this loss value 0.05 dB. The coupling is calculated as 19.4 dB.

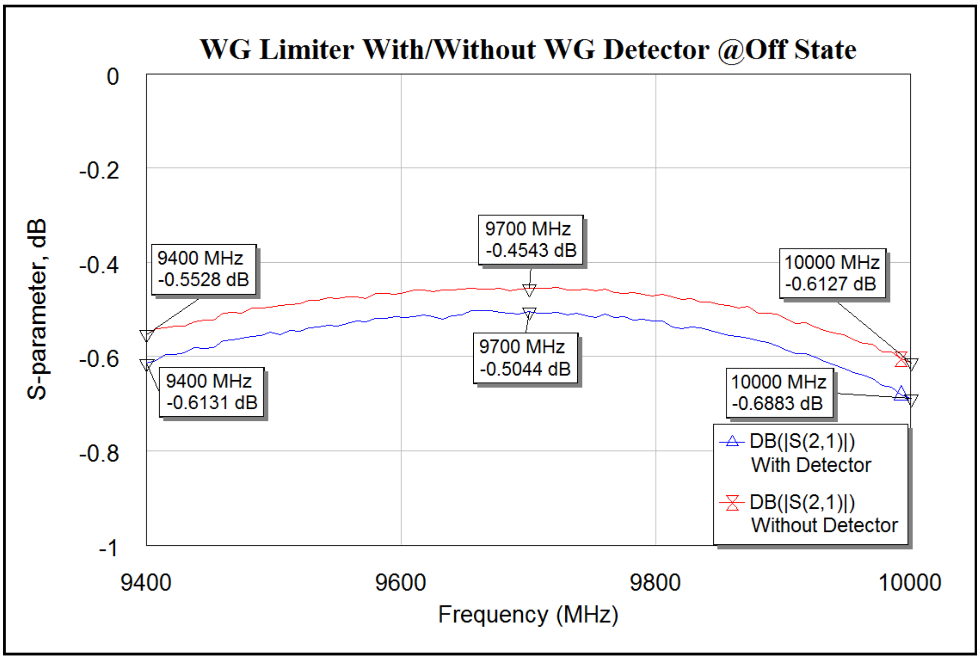

Figure 4.21: S-parameter Measurement of WG Limiter with/without WG Detector

4.2.2. Large Signal Measurements

After the linear measurements, high power nonlinear measurements of WG limiters with different diodes are performed. WG detector measurements, which show detected voltage level with varying input power, are made. Also, high power nonlinear measurements are made for the case that WG limiter is with WG detector. Effect of WG detector on WG limiter is observed. High power measurements are performed at two setups. Necessary measurement device and driving amplifiers cannot be found always in ASELSAN. The reason of establishing two setups is because of this problem. At the first setup maximum input power is about 45 dBm with duty cycle of 10%. Almost all of the measurements are performed at the first setup. At the second setup TWTA is used for about 62 dBm power levels with duty cycle 5%. The pictures of first setup are shown in Figure 4.22, Figure 4.23 and the pictures of second setup are shown in Figure 4.24, Figure 4.25.

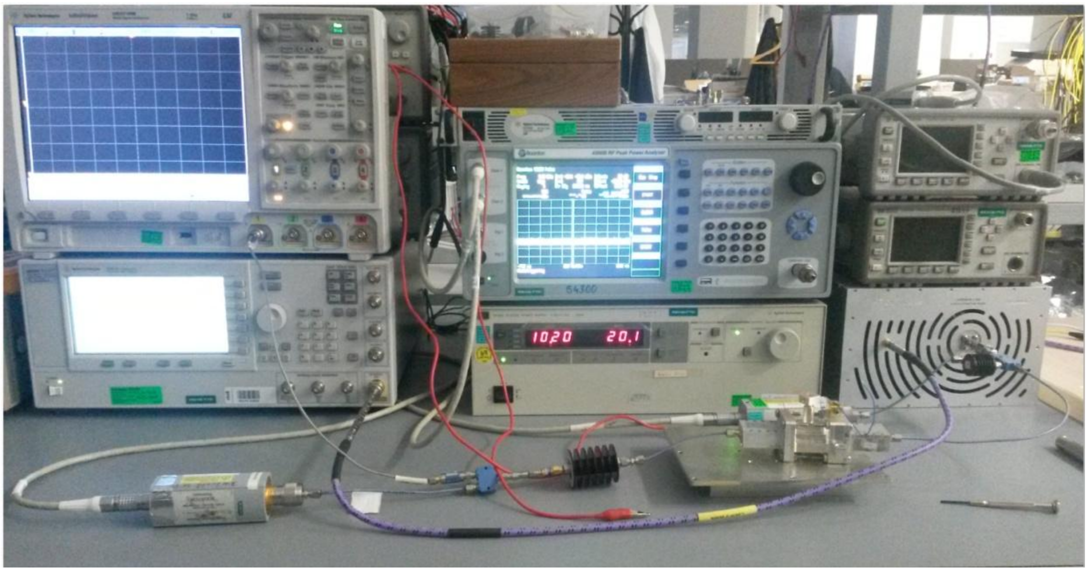

Figure 4.22: The Picture Of First Setup

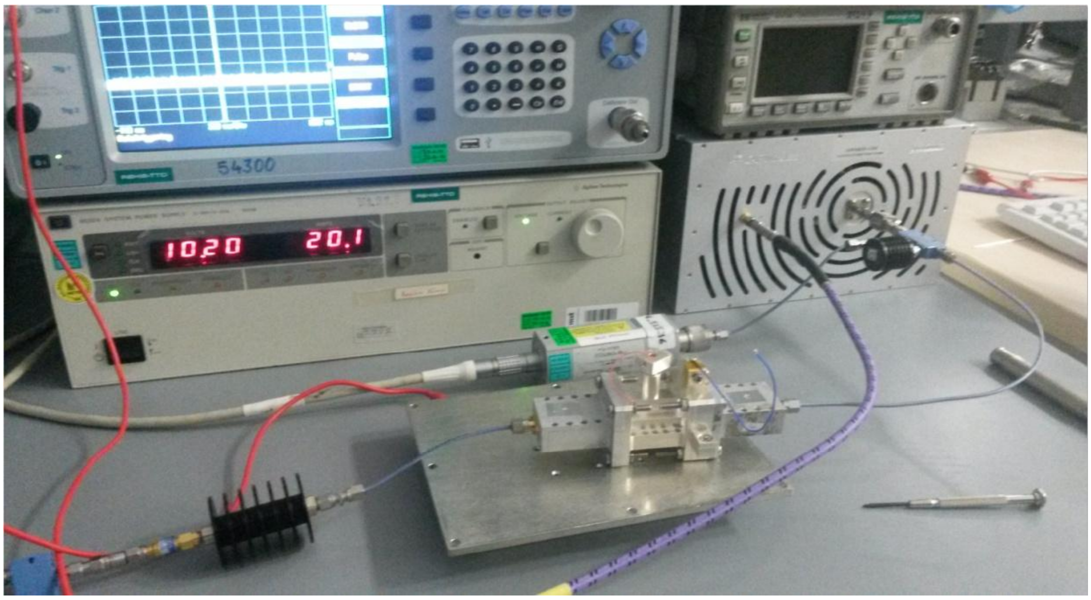

Figure 4.23: D.U.T at First Setup

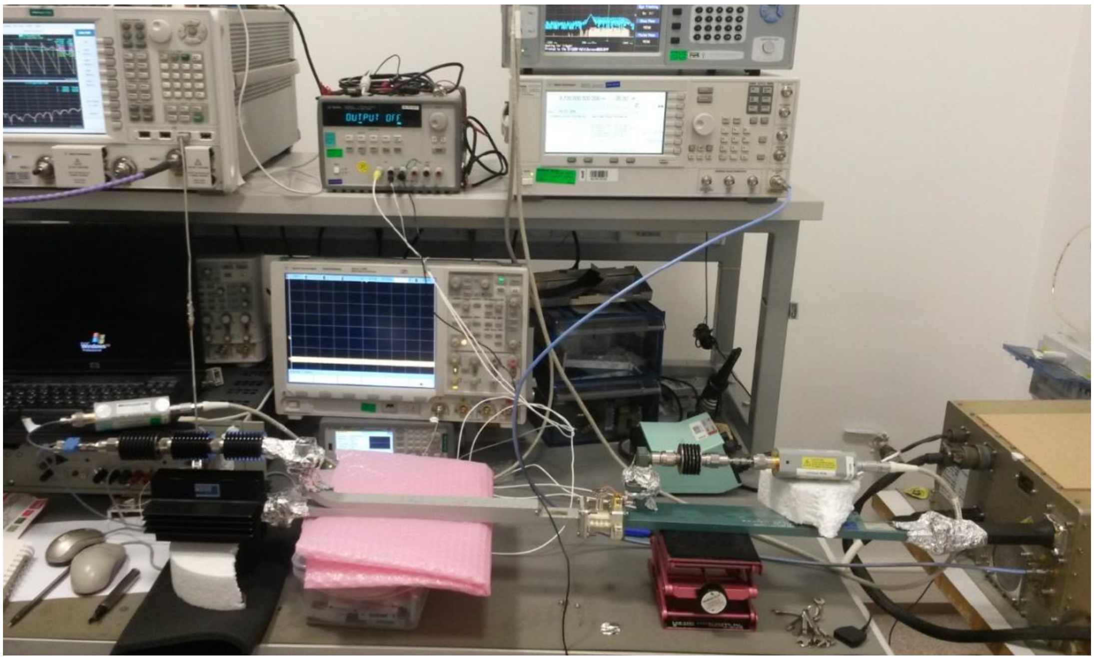

Figure 4.24: The Picture Of Second Setup

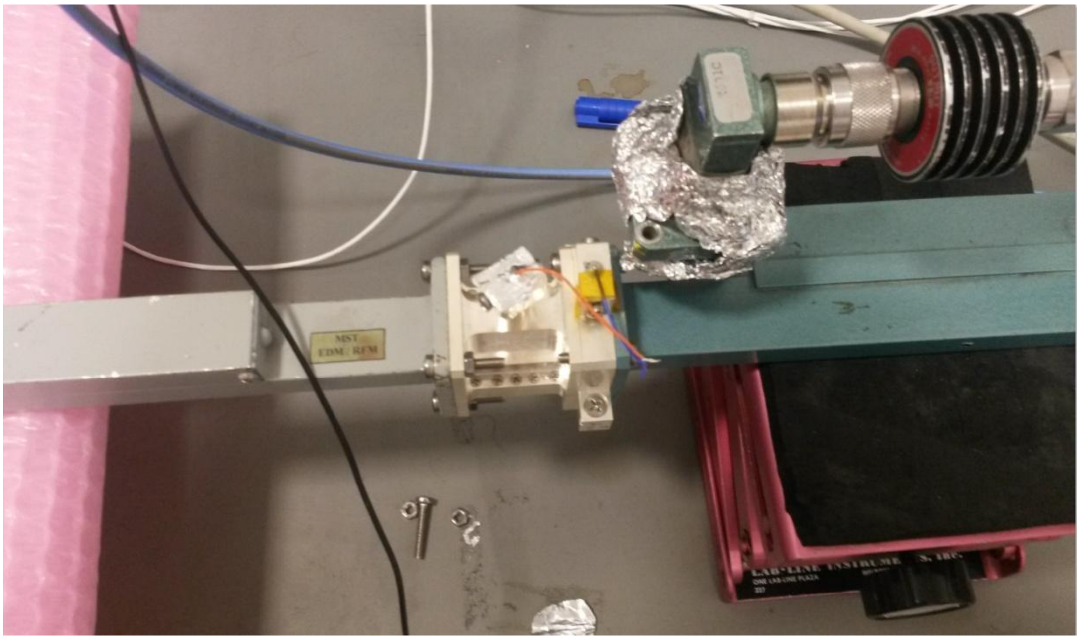

Figure 4.25: D.U.T at Second Setup

4.2.2.1. Measurements of WG limiter with MLP7120 Pin Diode

Limiting value of WG limiter with pin diode MLP7120 and without/with detector is measured at first setup at five different frequencies with power sweeping between approximately 10 and 45 dBm. The results are shown in Figure 4.26 and Figure 4.27.

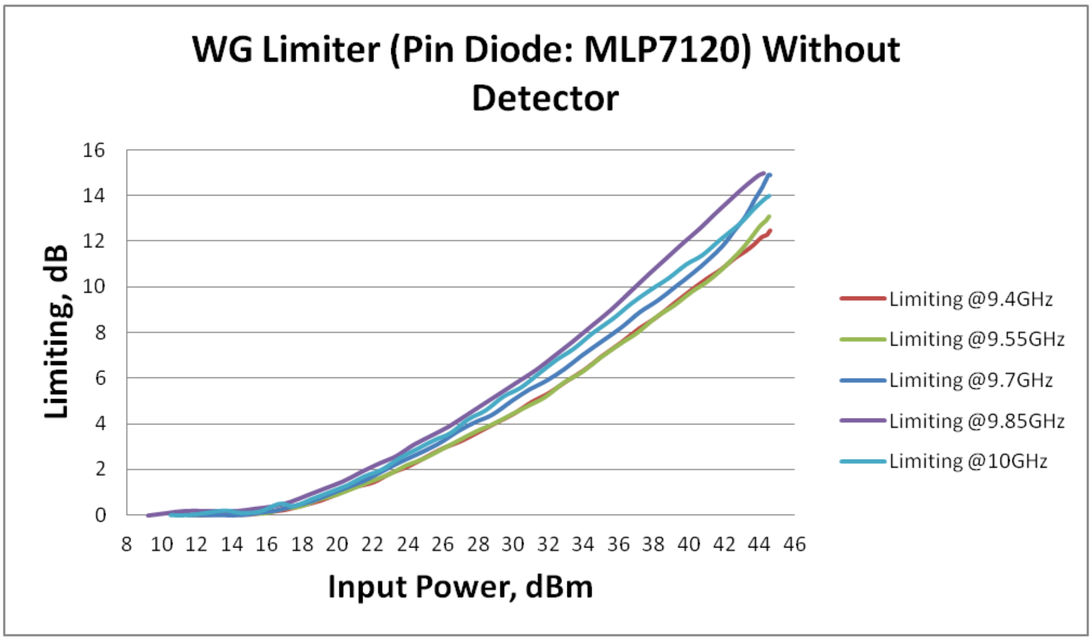

Figure 4.26: Nonlinear Measurements of WG Limiter with MLP7120 Pin Diode

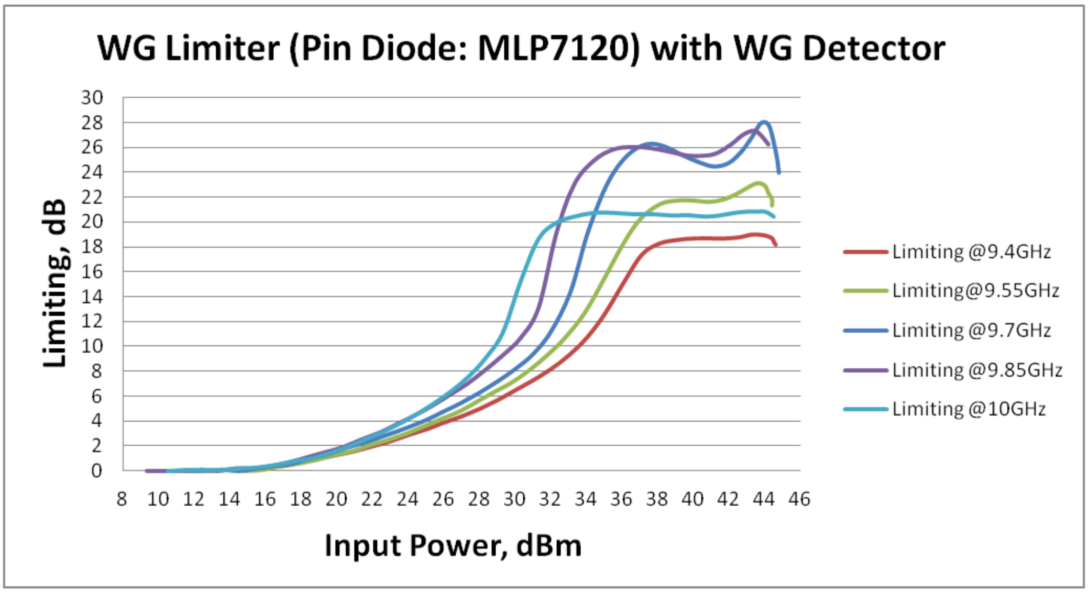

Figure 4.27: WG Detector Biased WG Limiter with MLP7120 Pin Diode Nonlinear Measurements

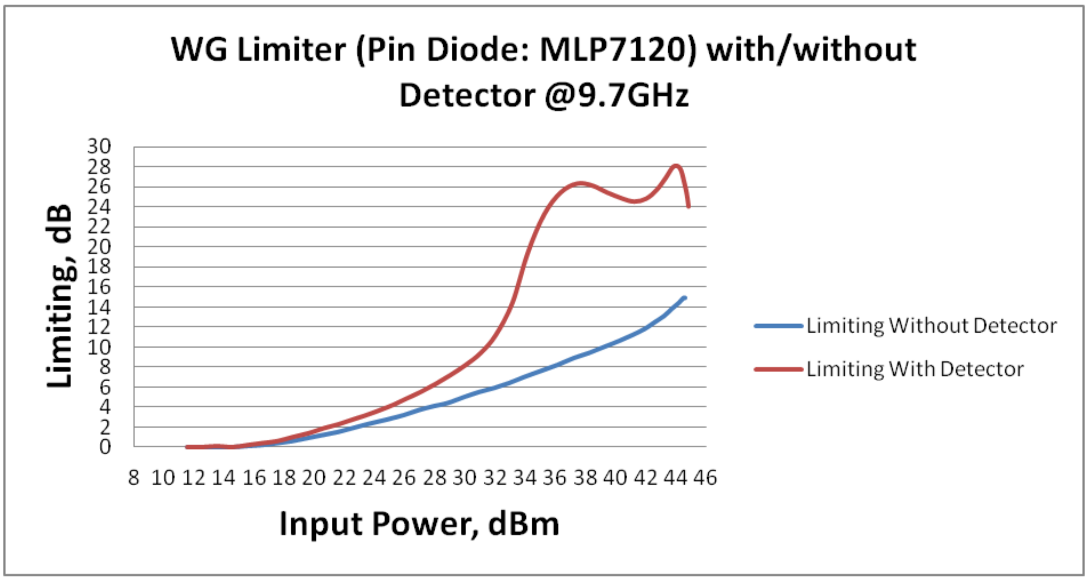

Figure 4.28: Comparison of WG Detector Biased and Not Biased WG Limiter with MLP7120 Pin Diode at 9.7 GHz

In the case of “without detector”, whose results are shown in Figure 4.26, when the input power is increased the limiting gets higher. Limiting value observed at the center frequency is higher than the limiting values measured at other frequencies; which is like the linear results. When the 45 dBm input power is given to WG limiter without detector, approximately maximum 32 dBm flat leakage occurs at the output in 9.4-10 GHz frequency band, at 9.7 GHz approximately maximum 30 dBm flat leakage occurs. The result of WG limiter with WG detector is shown in Figure 4.27. When the 45 dBm power comes to WG limiter without detector approximately maximum 26 dBm flat leakage occurs at the output in 9.4-10 GHz frequency band, at 9.7 GHz approximately maximum 19 dBm flat leakage occurs.

With the WG detector, the limiting values get higher and maximum limiting is acquired for lower input power levels as shown in Figure 4.28. There is a rippling response of limiting as shown in Figure 4.28. The cause for this behavior is predicted to be due to the reverse breakdown mechanism experienced in the Schottky diode. Analysis on the behavior is left as a future work.

In order to give higher input power to the WG limiter with pin diode MLP7120, the second setup is used. However, the Schottky diode of WG detector is damaged due to the high power at the input terminals. New WG detector with smaller coupling loop is produced and then the measurements continue with this WG detector. The smaller coupling loop greatly decreases the coupled power and the sensitivity of the Schottky detector. The results of TWTA measurements at 9.7 GHz with/without WG detector whose coupling loop is smaller are shown in Figure 4.29. In the case of “without detector”, limiting value reaches 22 dB with input power 60 dBm. At 60 dBm, the pin diode maximum limiting value is acquired which is shown in datasheet as 21 dB. Beyond 60 dBm input power, limiting value gets lower. Beyond 62 dBm TWTA gave VSWR error because all the power is reflected back to TWTA in this limiting level. The high power isolator must be used to make measurements with input power which is higher than 62 dBm. This is also left as a future work. In the case of “with detector”, the limiter/detector assembly is tested up to 54 dBm input power; which is shown in Figure 4.29. It should be noted that the reverse breakdown mechanism in the Schottky detector is experienced at 54 dBm input power level. Beyond this power level, the Schottky diode was expected to be impaired and the experiment had been ended at this power level. Besides, the reflection is much better in the "with detector" case and the possibility of TWTA breakdown due to return power from the limiter is higher. However, maximum limiting value of WG limiter with detector is observed as approximately 26 dB at input power of 50 dBm.

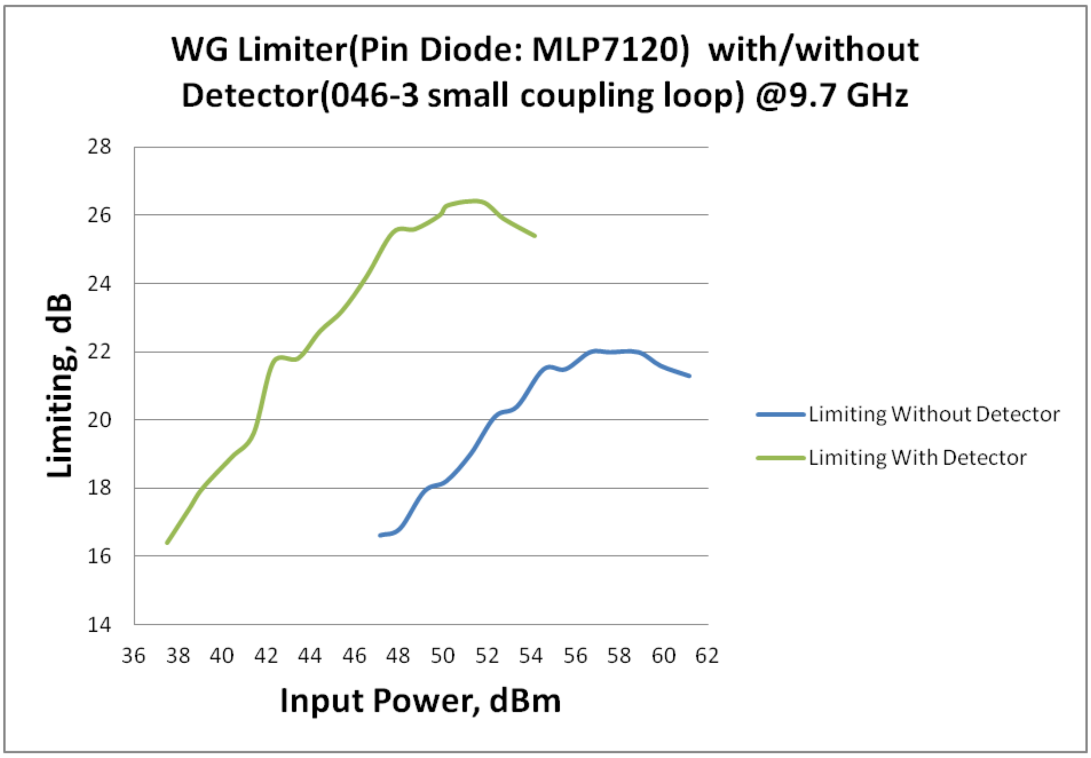

Figure 4.29: TWTA measurements of WG Detector Biased and Not Biased WG Limiter with MLP7120 Pin Diode at 9.7 GHz

To observe the coupling loop effect on limiting values, the WG limiter with pin diode MLP7120 is measured with different WG detectors. The result are shown in Figure 4.30. Detector1 have bigger coupling loop than Detector2. As it is observed in graph, WG limiter with Detector2 reaches its maximum limiting value approximately at input power 38 dBm. WG limiter with WG Detector1 reaches maximum limiting value at lower input power level which is approximately 33 dBm. However beyond 39 dBm, limiting values are getting closer. Bigger coupling loop results in higher voltage detection compared to other detector's detected voltage at same level input power and turning on of pin diode of limiter occurs at lower power levels.

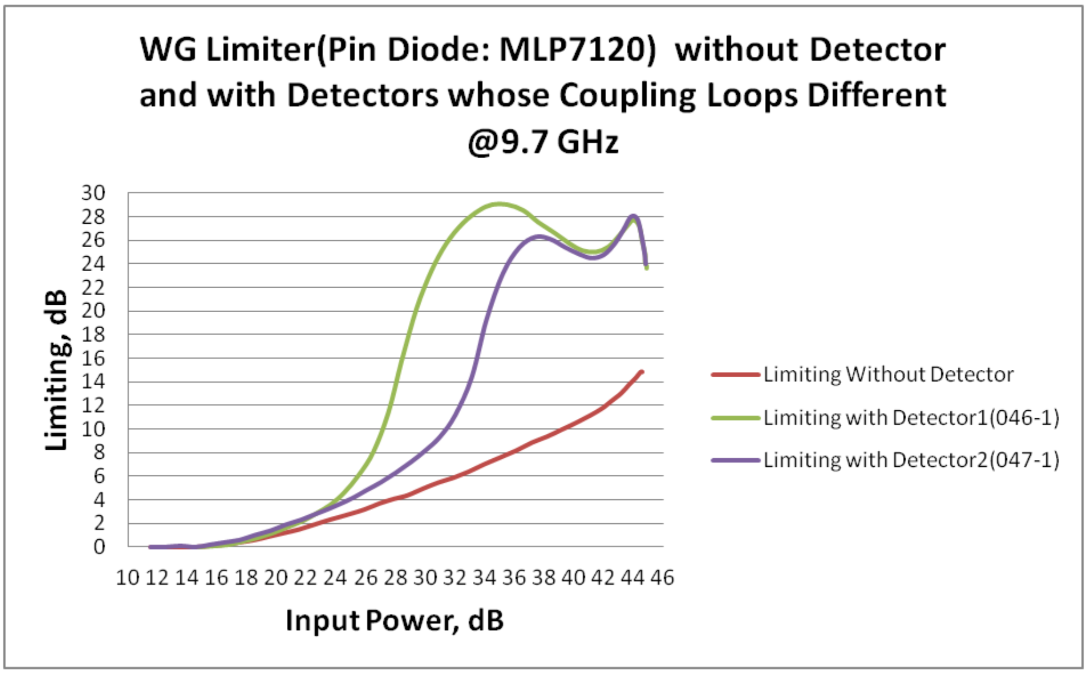

Figure 4.30: Coupling Loop Radius Effect on Limiting Values

4.2.2.2. Measurements of WG limiter with MLP7110 Pin Diode

MLP7120 is more powerful and less sensitive diode than MLP7110 diode as mentioned in pin diode selection part. After making measurements with MLP7120, WG limiter with pin diode MLP7110 is measured at 9.7 GHz. The results are shown in Figure 4.31. The higher sensivity of MLP7110 can be seen from results compared to MLP7120.

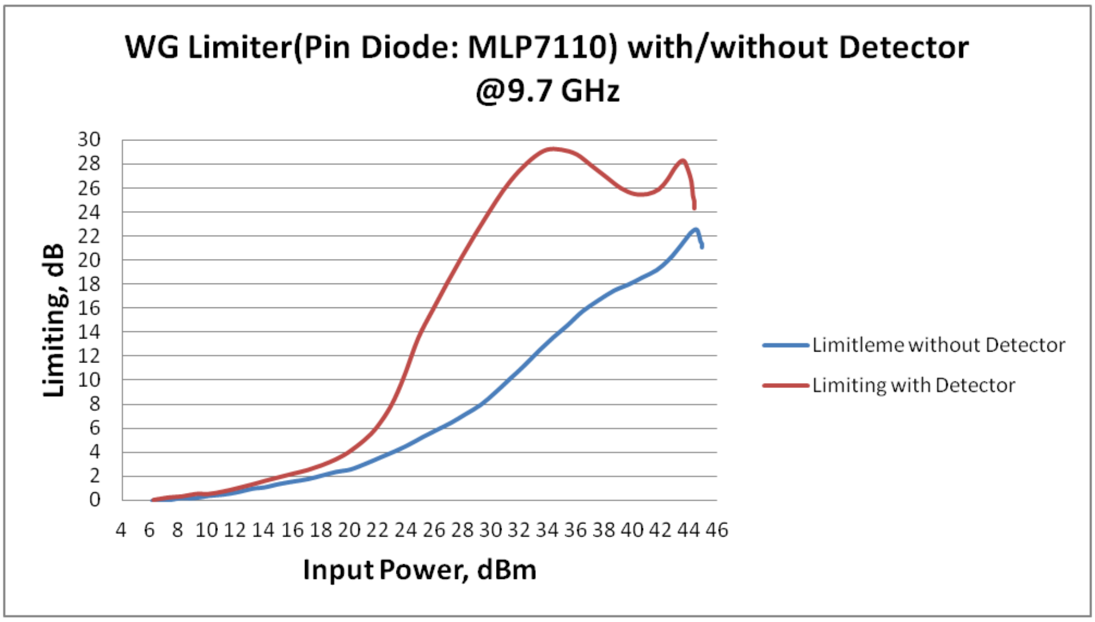

Figure 4.31: Comparison of WG Detector Biased and Not Biased WG Limiter with MLP7110 Pin Diode at 9.7 GHz

In the "without detector" case of MLP7110 pin diode limiter; as the input power is increased, limiting becomes higher. When the 45 dBm input power is given to WG limiter without detector maximum 23 dBm flat leakage occurs approximately at the output, at 9.7 GHz. In the "with detector" case of MLP7110 pin diode limiter, when 45 dBm of power comes to WG limiter without detector maximum 19 dBm flat leakage occurs at the output at 9.7 GHz approximately. The maximum limiting value of 29 dBm is acquried at about 35 dBm input power. The ripple characteristic is again seen in this diode justifying our suspicions on the reverse breakdown of Schottky diode.

4.2.2.3. Comparisons of WG Limiter Measurements

The measurement results of all of the limiter types are shown in Figure 4.32 including the two stage limiter with WG detector measurement only. From the results it can be deduced that; first of all, WG limiters' pin diodes are getting more sensitive when they are biased with WG detector which detects voltage directly proportional to input power; secondly, MLP7110 pin diode is more sensitive than MLP7120 pin diode because the slope of limiting value is higher and it has same limiting value with MLP7120 diode for lower power levels as expected. In the two stage WG limiter case, limiting value reaches 37 dB at the input power 33 dBm because both of the pin diodes are in action for limiting. Beyond 37 dBm of input power, limiting values of all limiters with detector are converging to similar values.

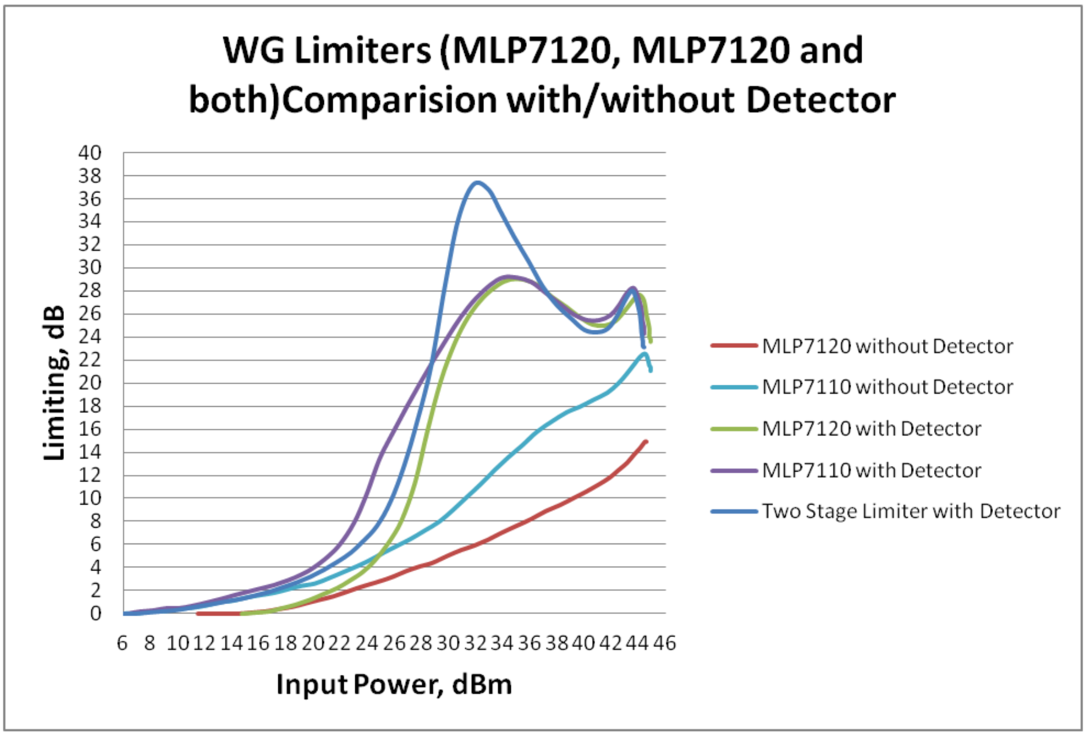

Figure 4.32: Comparison of WG Detector Biased and Not Biased WG Limiters with MLP7110 and MLP 7129 Pin Diodes at 9.7 GHz

4.2.3. Oscilloscope Measurements

After making high power measurements for all of the cases with peak power analyzer, spike leakeage level and response time of WG limiters are measured for all the cases. Results are shown in Figure 4.34. All of the limiting value measurements were done with peak power analyzer however the detector of peak power analyzer is not fast enough to see spikes at the output of WG limiters. Spike leakage and response time measurements are done with oscilloscope and fast detector at first setup, and there is 31.7 dB attenuation between output of the WG limiter and input of the selected detector (Krytar 202A). Attenuator is put in front of the fast detector to prevent it from high power damage.

Krytar 202A detector is used to see spike leakeage which occurs in narrow time duration. Detected voltage vs. input power measurement of fast detector Krytar 202A is shown in Figure 4.33. The input power is swept between -16 and 21 dBm as seen in Figure 4.33.

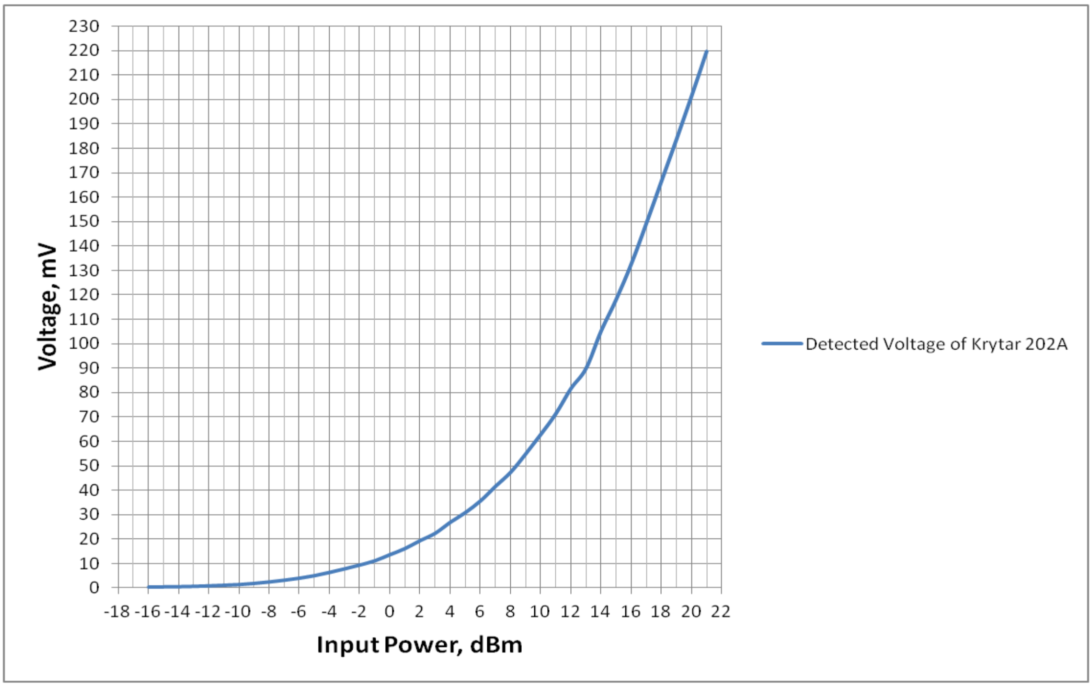

Figure 4.33: Output Voltage Measurement of Fast Detector Krytar202A

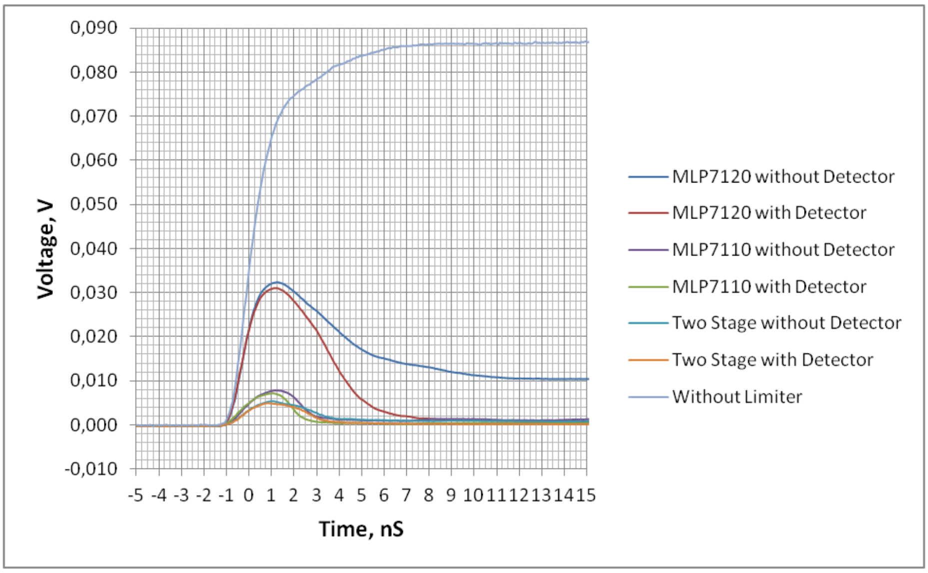

Figure 4.34: Output Voltage/Response Time Measurement of WG Detector Biased or Not Biased WG Limiter with MLP7120 or MLP7110 Pin Diode

After measurements, spike levels and response times of the WG limiters are tabulated and shown in Table 4.1.

Table 4.1: Response Time and Spike Leakage Levels of WG Limiters

WG Limiters	Response time (nS)	Spike Level (dBm) @ P_{in}~44.7 dBm
WG Limiter with MLP7120 without Detector	~8	~36.7
WG Limiter with MLP7120 with Detector	~6	~36.6
WG Limiter with MLP7110 without Detector	~3	~29.7
WG Limiter with MLP7110 with Detector	~2.6	~29.6
Two Stage Limiter without Detector	~3	~25.6
Two Stage Limiter with Detector	~2.9	~25.6

The effect of detector is observed best on WG limiter with MLP7120 pin diode. More sensitive pin diode MLP7110 have shorter response time and lower spike level compared to MLP7120. Response time of two stage limiter so close to limiter with MLP77110. Spike leakege level is minumum at two stage limiter as expected because two diodes are acting. From comparison of single stage limiters, it can be deduced that, response time and spike leakeage are inversely proportional with each other.

The response time of limiter with MLP7120 can be shortened. In the case of WG detector biased WG limiter, DC cable is used to transmit detected voltage to pin diode of limiter. The length of this cable is crucial to speed up the pin diode limiter. However DC cable length cannot be shortened so much because of mechanical limititations. If DC length cannot be shortened, delay can be given to RF path between WG detector and input of the WG limiter while keeping DC cable length same.

To test the case, a delay of approximately 5 ns is applied to the RF path between the detector and the limiter using coaxial cable. The screenshot of the result on the oscilloscope is shown in Figure 4.35. The detected voltage level and power level of spike at the its peak point are about 19 mV and 36 dBm in the without detector case. In the case of with detector, spike level is about 15 mV~33.5 dBm and in this case RF is delayed. It was observed that the spike level is decreased by giving delay to RF. Also, the time of peak point decreases by 0.42 ns. It can be inferred from the measurements that if the delay is increased, the amplitude of the spike power becomes smaller. However, note that applying 1 ns delay requires 30 cm lentgh in air. Accomplishing a meaningful delay may require some other techniques like dielectric filling or changing waveguide modes. However it should be appreciated that applied delay may cause serious loss problems, making it unfeasable in applications.

Figure 4.35: Comparison of WG Limiter without WG Detector and RF Delayed WG Limiter with WG Detector

Finally, WG detector performance is measured. Detected voltage is shown for two cases. Detector output is floating in one case, and in the other case, it is connected to the pin diode of WG limiter. Figure 4.36 shows the measurement of output voltage versus the applied input power. Note that, the output voltage is clipped by the pin diode at its knee voltage (approximately 0.86V).

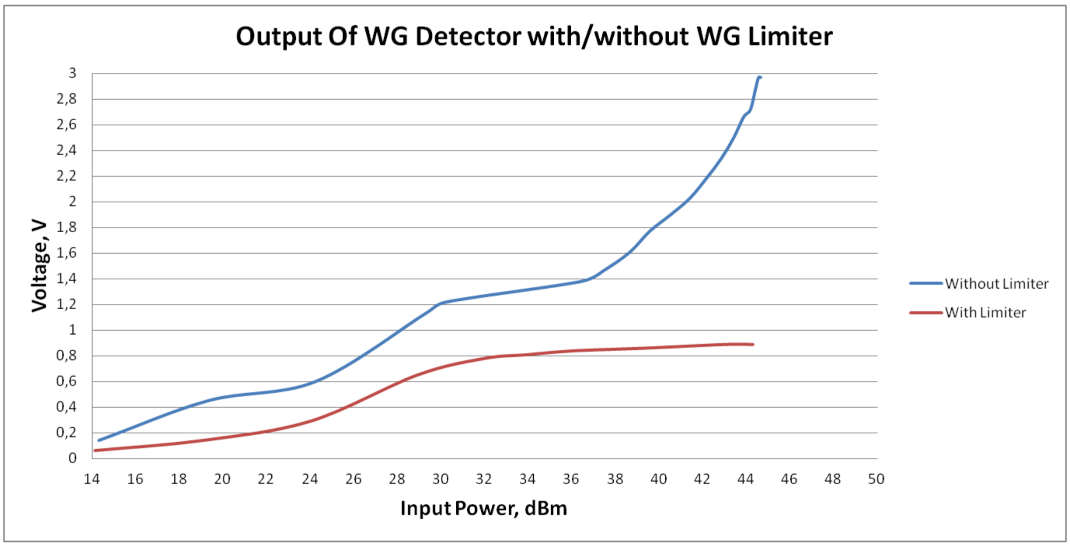

Figure 4.36: Detected Voltage Measurement with/without WG Limiter

CHAPTER 5

CONCLUSION AND FUTURE WORKS

In this thesis study, high power WG limiter are investigated. Several topologies are analyzed; post coupled pin diode WG limiter topology is chosen for implementation. High power limiting is one of the main purposes of the thesis, therefore high power pin diodes are chosen. Another major purpose is to reduce the response time of WG limiters. At this point, the detector which biases the pin diode of WG limiter is recommended for reducing response time and increasing the sensitivity.

In this thesis, two single stage WG limiters which have different diodes and WG detectors having different coupling loops are designed, fabricated and measured.

Design process of WG limiter began with AWR MWO simulations. Diodes and 3D structures are modeled before making simulations in AWR MWO. 3D WG limiter modeling is done with formulations.

WG limiter pin diode parameters are key parameters of design to match the structure in desired bandwidth of 9.4-10 GHz. After getting good results from simulations on impedance matching, design continues with 3D EM simulations in CST. The whole structure is drawn in CST and S-parameter simulations are performed. Co-simulation is made to combine lumped model of diode and 3D structure. To sum up, impedance matching is the main aim of ideal and 3D EM simulations. To put pin diode in WG, impedance matching of pin diode and manipulating S_{11} and S_{21} responses according to diode ON and OFF state are the goals of the WG limiter design process.

Similarly, design process of WG detector began with modelling in AWR MWO. Spice model of Schottky diode is used and impedance matching of this diode in coaxial structure is analyzed in AWR MWO. In addition to linear simulations, nonlinear simulations is performed which shows the detected output voltages. After ideal simulations in AWR MWO, the 3D structure is drawn in CST and co-simulation is performed. The most important part of WG detector is the coupling loop whose radius affects the detected voltage. By using the spice model of Schottky diode in CST, nonlinear transient time domain simulations are performed.

After these design steps and optimizations in CAD, fabrication of the limiters and detectors are completed; and linear/ nonlinear measurements are made. Network analyzer is used to get S-parameter of the devices and tuning is made during this measurements. The band of the WG limiters are adjusted to 9.4-10 GHz at ON and OFF states of the pin diode. Insertion loss and return loss values are measured. Insertion loss of the WG limiters is below 0.5 dB for both of the diodes in the 9.4-10 GHz frequency band. Isolation value of WG limiter with diode ON state is between 25 and 30 dB at the center frequency of operation. Besides, linear measurements of the WG detector are made. In these measurements coupling loop radius is tweaked for plausible IL values, which is also a measure of coupling value. Next, nonlinear measurements are performed. Power sweep up to 61 dBm is applied with the help of TWTA and up to 46 dBm with the help of driver amplifier. Limiting values of the WG limiters are measured with these power settings. Limiting values up to 30 dB are acquired. It is observed that usage of WG detector increases the sensivitiy of the WG limiter and lowers the response time of the WG limiter. Effect of coupling loop on limiting values is observed. It is also observed that the effect of the WG detector can be increased to get rid of spike leakage by giving RF delay between WG limiter and WG detector.

The maximum power levels and duty cycle limits of WG limiters are not investigated. The reason is that there is not any other pin diode to continue the measurements. These measurements will be performed as future work after getting ordered diodes. Besides, the reason of the ripple at the limiting value graphs will be investigated in detail as future work. Moreover, geometry of the composed structure which includes both detector and limiter can be changed to reduce to DC bias cable length and to increase RF path. This change results in increasing detector effectiveness. Mechanical structures which have proper geometry will be produced and the measurements are made as future works. Also, the distance between the pin diodes of two stage WG limiter are not taken into account at the beginning of the design. According to proper distance between diodes, two stage WG limiter structure will be designed and manufactured.

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