# DESIGN AND REALIZATION OF HIGH POWER LOW LOSS COMBINERS

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submitted by **GONCA SUNA** in partial fulfillment of the requirements for the degree of **Master of Science in Electrical and Electronics Engineering Department, Middle East Technical University** by,

Prof. Dr. Canan Özgen
Dean, Graduate School of **Natural and Applied Sciences** _____

Prof. Dr. Gönül Turhan Sayan
Head of Department, **Electrical and Electronics Engineering** _____

Prof. Dr. Nevzat Yıldırım
Supervisor, **Electrical and Electronics Engineering Dept., METU** _____

Prof. Dr. Şimşek Demir
Co-Supervisor, **Electrical and Electronics Engineering Dept., METU** _____

**Examining Committee Members:**

Prof. Dr. Canan Toker
Electrical and Electronics Engineering Dept., METU _____

Prof. Dr. Nevzat Yıldırım
Electrical and Electronics Engineering Dept., METU _____

Prof. Dr. Şimşek Demir
Electrical and Electronics Engineering Dept., METU _____

Prof. Dr. Gülbin Dural
Electrical and Electronics Engineering Dept., METU _____

Dr. Tuncay Erdöl
ASELSAN Inc. _____

**Date:** **25/11/2013**

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Name, Last name : Gonca SUNA

Signature :

## ABSTRACT

DESIGN AND REALIZATION OF HIGH POWER LOW LOSS COMBINERS

Suna, Gonca

M.S., Department of Electrical and Electronics Engineering

Supervisor: Prof. Dr. Nevzat Yıldırım

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In recent high power microwave systems, power generation is commonly achieved by combining a bunch of transistor amplifier. Regarding the efficiency of power combining operation, insertion loss of the combiner is a critical parameter. In this thesis, several low loss power combiners, namely, microstrip Wilkinson combiner in 6-18 GHz frequency range, suspended stripline branchline couplers in 16.5-17.5 GHz frequency range and finally, planar probe coaxial waveguide combiners in 8.5-11.5 GHz and 15.5-17.5 GHz frequency ranges are investigated and implemented. It is shown that planar probe coaxial waveguide combiner has much lower loss compared to the other ones. Therefore, 8 identical 2 W power amplifiers are combined using planar probe coaxial waveguide combiners of two different operating frequency bands to get 15 W outputs in both 8-12 and 15-18 GHz frequency ranges successfully.



Keywords: Power Combiner, Planar Probe, Coaxial Waveguide, Combining Efficiency

# ÖZ

YÜKSEK GÜÇLÜ VE DÜŞÜK KAYIPLI BİRLEŞTİRİCİLERİN TASARIMI VE GERÇEKLENMESİ

Suna, Gonca
Yüksek Lisans, Elektrik ve Elektronik Mühendisliği Bölümü
Tez Yöneticisi: Prof. Dr. Nevzat Yıldırım

Kasım 2013, 129 sayfa

Son yıllardaki yüksek güçlü mikrodalga sistemlerinde, güç üretimi yaygın olarak belirli sayıda transistör yükseltecin çıkış güçlerinin birleştirilmesi ile elde edilmektedir. Güç birleştirme işleminin verimliliğinde birleştirici kaybı önemli bir değişkendir. Bu tezde, 6-18 GHz frekans aralığında mikroşerit Wilkinson birleştirici, 16.5-17.5 GHz frekans aralığında askıda şerit hatlarla bağlaç tipi birleştirici ve son olarak, 8.5-11.5 GHz ve 15.5-17.5 GHz frekans aralıklarında eş-eksenel ortamda düzlemsel problu birleştirici olmak üzere çeşitli düşük kayıplı güç birleştiriciler incelenmiş ve gerçeklenmiştir. Eş-eksenel ortamda düzlemsel problu birleştirmenin diğerlerine kıyasla daha az kaybı olduğu gösterilmiştir. Bu nedenle, 8 adet 2 W'lık özdeş yükseltecin çıkış güçleri eş-eksenel ortamda düzlemsel problu birleştiricilerle birleştirilmiş, 8-12 GHz ve 15-18 GHz frekans aralıklarında 15 W çıkış gücü başarı ile elde edilmiştir.

Anahtar Kelimeler: Güç Birleştirici, Düzlemsel Prob, Eş-eksenel Dalga Kılavuzu, Birleşim Verimliliği

*To my family*

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# CHAPTER 1

# INTRODUCTION

In microwave systems, the system scenario may require high output power. In this case, high-output power modules must be built to operate in microwave frequency range. The oldest solutions for this requirement are microwave tubes. The most commonly used one is the traveling wave tube amplifier, which was introduced as a concept in 1942 and suggested to be used as an amplifier in 1947 by Kompfner [1]. In his article, Kompfner describes his technique and its usage as an amplifying device. Amplifying occurs by the help of a beam of electrons and a helix shaped structure.

In following years, solid state monolithic microwave integrated circuit (MMIC) technology has developed. Using this technology, power amplifiers for microwave frequencies were designed and produced. Sizes of these devices were on the order of millimeters and the output powers are generally less than 10 Watts per device. Using only one single device as a solution for high power (hundreds of Watts in microwave frequencies) requirement was not feasible. However, this usage was considered for many applications which do not require more than tens of Watts in microwave frequencies. Modules including MMIC devices were much smaller than the ones using traveling wave tube amplifiers (TWTAs). Despite the size advantage, the output power levels of MMICs per device were not appropriate for most of the transmitters. Therefore, an assigned number of identical MMIC amplifiers can be employed by combining the outputs of those units to achieve more power than a single MMIC die could supply. Different types of power combiners

were developed in the literature and have been used for combining MMIC amplifier outputs. In this thesis, several examples of power combiners are described, designed and built for various microwave frequency bands. Among them, the most efficient combiners are selected and used to build power amplifier modules of 10-20 Watts output for two frequency bands, 8-12 GHz and 15-18 GHz. Power combiner devices could be also used for combining a number of TWTA outputs; only for the case when more than a few kilowatts are needed, which is out of the scope of this thesis.

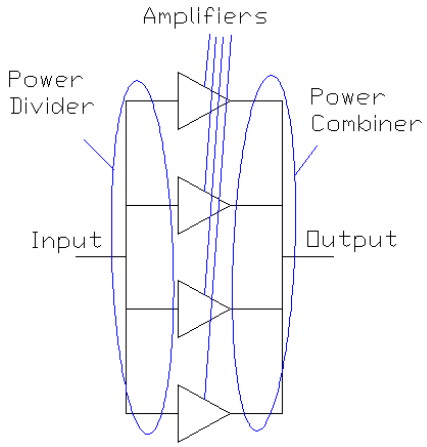



**Figure 1.1:** A conceptual power combining system

In Figure 1.1, a conceptual power combining system is shown. In this figure, there is a power divider at the input stage after the input port. Power is applied from input and divided by four, using the power divider. Outputs of this power divider are

used for feeding the four amplifiers. There is a power combiner at the output stage. Amplifier outputs are combined by the power combiner and fed to the output.

There are a few main types of couplers which have been used widely in power combining structures since the introduction of solid state power amplifier (SSPA**)** concept. These are Wilkinson, branchline, rat-race and coupled line couplers. The combiners are mainly defined by Pozar in [2].

Wilkinson introduced a divider of hybrid type in 1970 [3]. He described the structure of a divider which can divide the input into a randomly selected number of parts. Each resulting part is identical, i.e. has the same signal magnitude and phase. Resistive elements can also be added between branches to obtain good isolation between the output parts.

The simplest and most widely used version of this kind is a 2-way Wilkinson divider. The schematic of the divider is given in Figure 1.2. In this divider, there are two output and one input ports. The input signal splits into to two at a junction. The resulting two branches of this junction are identical and have a length of quarter wavelength (QWL) at the center frequency of operation. While each port has 50 Ω reference impedance, the characteristic impedance of these lines must be 70.7 Ω, i.e. √2 times the reference characteristic impedance. The QWL branches are for impedance matching of two parallel-connected outputs at the junction. Each QWL line is connected to one output with reference 50 Ω via 50 Ω lines. There is also a resistive element in the structure. A 100 Ω (twice the reference impedance) resistance is connected between the endpoints of the two QWL lines. This resistor supplies good isolation between two outputs in case of imperfect 50 Ω loads. In reverse, when the structure is used as a combiner, unevenly fed powers from the inputs will be dissipated on this resistor. Hence, the power transfer between the input ports is obstructed and any damage on the devices is prevented.

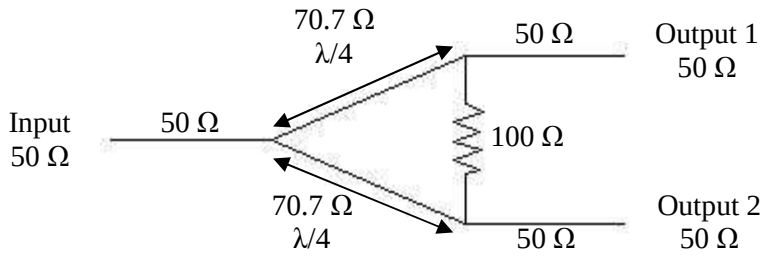



**Figure 1.2:** Schematic of a 2-way Wilkinson divider

Another widely used type of combiner is the branchline coupler. This is a type of $90^o$ hybrid coupler; since the input is divided into two parts with equal magnitude but $90^o$ phase difference. An example schematic of a branchline coupler is given in Figure 1.3. There are two output ports, one isolated port and one input port. These ports are connected with a network which includes four QWL lines as seen in Figure 1.3. When the reference characteristic impedance is 50 Ω, the line which connects two output ports is 50 Ω and the line which connects the input and the isolated ones is also 50 Ω. The other two QWL lines have 35.4 Ω characteristic impedance; i.e. the reference characteristic impedance 50 Ω divided by √2. The isolated port is terminated with a load of impedance equal to the reference characteristic impedance; 50 Ω in the case of Figure 1.3. In this case, when power is applied from the input, it splits into two parts and transferred to the outputs. The signals at the outputs have the same magnitude. In terms of phase, the signal at Output 2 is lagging the signal at Output 1 by $90^o$.

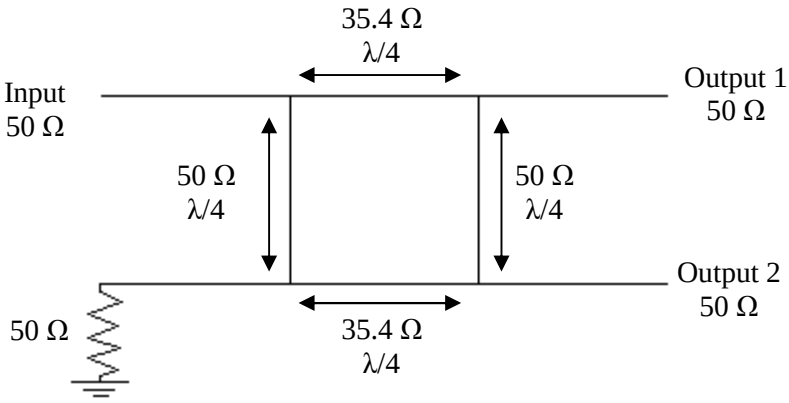



**Figure 1.3:** Schematic of a 2-way branchline coupler

Rat-race coupler is also a very common type of combiners. The operation is similar to the branchline coupler, except the phase difference between the outputs; it is $180^{o}$ instead of $90^{o}$. There are two output ports, one isolated port and one input port. The ports are connected to the center ring formed by four line sections consisting of three QWL and one ¾ wavelength sections as shown in Figure 1.4.

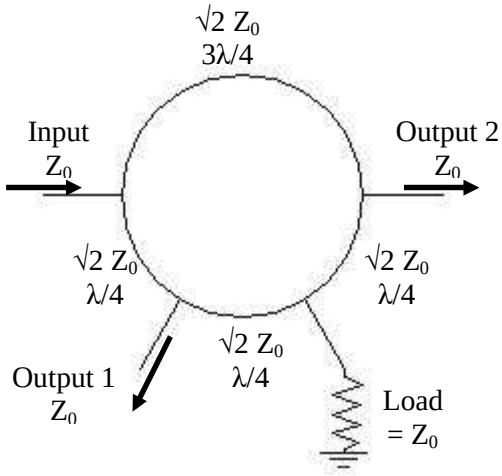



**Figure 1.4:** Schematic of a 2-way rat-race coupler

In this configuration, the rat-race coupler divides the signal to Output 1 and Output 2. The signal magnitudes are equal. In terms of insertion phase, the signals at the two outputs are $180^o$ out of phase. This operation is used in special applications like mixer and phase shifter circuits.

Coupled line couplers are also widely used types of combiners. The explanatory circuit is given in Figure 1.5. There are two QWL transmission lines which are coupled in a selected method. In most coupled line structures, the lines are closely spaced and they are coupled through the fringing fields in their edges. The circuit is examined by even and odd mode approaches. In each analysis, the two coupled transmission lines are modeled as an equivalent transmission line. The characteristic impedances of the equivalent transmission lines are calculated as $Z_{0e}$ and $Z_{0o}$ respectively for even and odd mode. The inequality of impedances is due to different boundary conditions used between the lines where the coupling occurs. In

the circuit in Figure 1.5, Output 1 is the direct port, Output 2 is the coupled port and the isolated port is terminated with load impedance $Z_0$. For equal split of the input signal to the two outputs, $Z_{0e}*Z_{0o}$ must be equal to $Z_0^2$ where $Z_0$ is the reference characteristic impedance of the all four ports. Furthermore, the phase difference between the two ports is $90^o$.

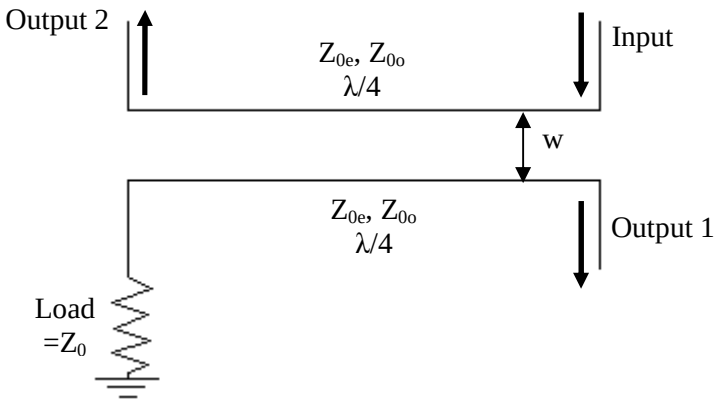



**Figure 1.5:** Schematic of a 2-way coupled line coupler

In 1979, Russell reviewed various types of combiner which can be used in solid state power amplifier (SSPA) modules in his paper [4]. In the paper, firstly, the common combiner types are mentioned. Then, different structures are described in terms of combining steps: corporate (multi step) and N-way (single step).

Corporate combiners are grouped into two: chain type and tree type. In chain combiners, couplers are used in cascade form. In each step, power travels from input to outputs by coupling. In spite of easy construction of the chain approach, additional combining losses could be a disadvantage. Insertion losses of all the couplers will be accumulated in stages and thus, combining efficiency will decrease. A schematic is of this type is given in Figure 1.6.

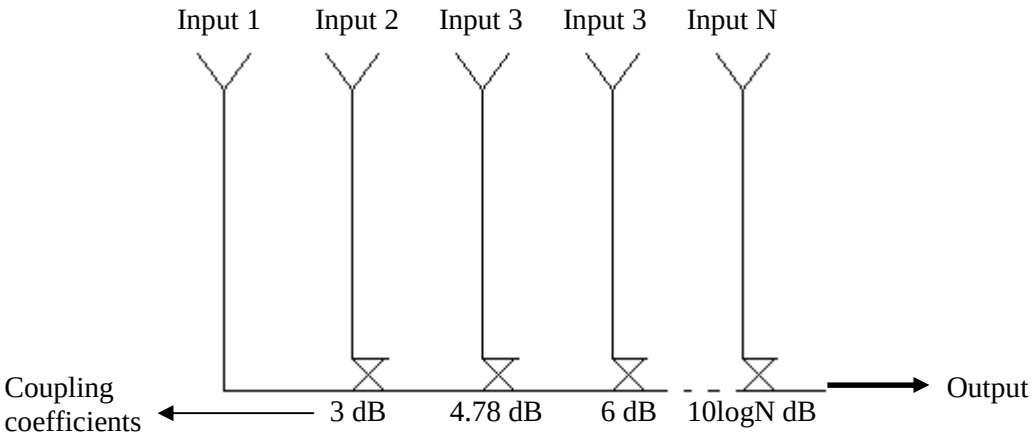



**Figure 1.6:** Schematic of a chain combiner with N inputs

Tree combiners are more widely used corporate combiners in microwave modules. In tree combiners, the circuit is formed at a few steps because 2-way combiners are used at each step. At the end, for N stages, $2^N$-1 adders are used. In Figure 1.7, the schematic for a 4-way tree combiner is given. Similar to chain

combiners, these combiners have the disadvantage of the accumulation of insertion loss due to combiners at each stage.

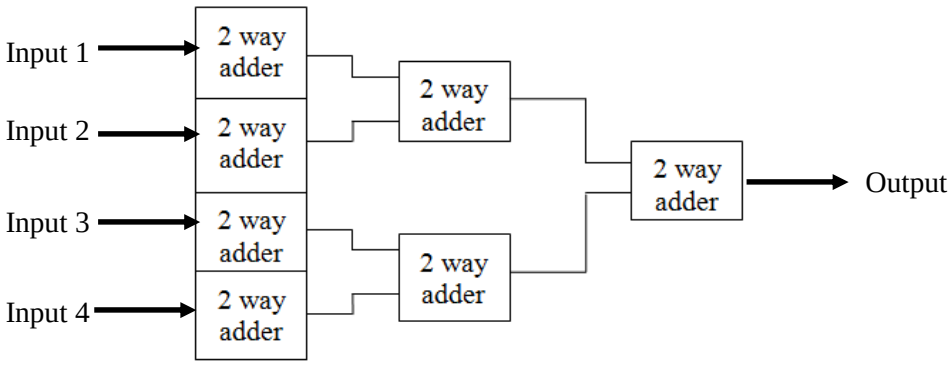



**Figure 1.7:** Schematic of a tree combiner with four inputs

In Russell's paper [4], the second main type, N-way combiners are defined as devices which combine the required number of inputs at a single step. They are also grouped by the method of combining as non resonant combiners and cavity combiners.

Non-resonant N-way combiners use the technology in corporate combiners, except the connections are arranged for N inputs in N-way symmetry. The inputs are placed radially and power is combined at a transmission line junction connected to all branch transmission lines. One example for this type is Wilkinson's combiner

with N inputs [3]. In N>2 case, the isolation resistors must be placed evenly between the branches and this brings a difficulty for producing the circuit. Another approach may be the usage of radial transmission lines for combiner branches, which is studied in [5].

Resonant N-way combiners use the electromagnetic (EM) wave modes in the structure. The powers achieved by the amplifiers are transferred to air medium such as the combination of their fields generates the EM mode in the combining structure. In case of even feeding, combination of powers will transform into the desired mode in the structure and transferred to the output.

Resonant N-way combiners have the advantage of minimized dielectric and conductor loss due to combining in air medium. Because of this advantage, this technique has become popular in recent years and there has been many studies using different combining structures. In some studies, power is combined in rectangular waveguide (RWG) ([6]-[10]). This medium has the disadvantage of limited bandwidth, due to the cutoff frequency of RWG. As a solution, combining in coaxial waveguide (CWG) was investigated, which has TEM mode operation with no cutoff frequency. In this case, assuming matching circuits are wideband, bandwidth is only limited by the input amplifiers. In [21], [22], power is transferred to CWG through a finline array. In these combiners, amplifiers are inside the combining medium, which brings difficulty in production and heat removal. In [13]-[22], this power transfer is made by using probe arrays. Amplifiers are connected at inputs of the array inside the combiner. There is one probe for each input in the array which is inserted into combining medium. Power from amplifiers are radiated through these probes and combined in air CWG medium.

In power combining systems, combining efficiency depends on differences between combined signals and the loss introduced by the combiner. Ideally, maximum efficiency is obtained when all combined signals are equal in magnitude

and phase and the combiner has no insertion loss. The characteristics (magnitude and phase) of input signals depend on MMIC characteristics and they are often not controllable. In addition to matching each arm as much as possible in terms of magnitude and phase, combiners are selected to have low insertion loss.

Depending on the requirements and limitations of applications, certain techniques of power combiner design are more suitable than others to obtain lower insertion loss and preferred in critical applications. In this thesis, combiners are designed and built for comparison of this property in microwave bands using three different techniques as summarized below. In order to compare their performances, response at 17 GHz is taken as reference, since it is included in all design frequency bands.

1) Microstrip Wilkinson combiner:

The first combiner is designed to investigate the effect of microstrip line usage in a combiner. For this purpose, a wideband 8-way microstrip divider, seen in Figure 1.8, was designed and built at 6-18 GHz band. The circuit is formed as a Wilkinson divider without the isolation resistors. Inputs are placed at the edges of an octagon. The material cladding used for transmission lines is Rolled copper. The input return loss of the produced combiner came out to be better than 10 dB over the 6-18 GHz band while the best match is about 20 dB at 17 GHz. The ideal insertion loss is 9.03 dB per branch and the measured insertion loss in the operating frequency band came out to be around 10 dB. In order to use as a comparison criterion with other power combiner techniques, the insertion loss added by the combiner is measured at the best match frequency (17 GHz) and the average insertion loss of branches came out to be 10.5 dB; thus the loss added by the combiner is found to be about 1.5 dB. Both conductor loss and dielectric loss are effective in microstrip lines.

**Figure 1.8:** View of the prototype microstrip Wilkinson combiner

2) SSS branchline coupler:

Another technique to be investigated is the suspended substrate stripline (SSS) technique. For this investigation, a 4-way divider using SSS structure, seen in Figure 1.9 was designed and built at 16.5-17.5 GHz frequency band. The circuit is formed using 2-way branchline couplers in two steps. The input return loss of the produced combiner came out to be better than 19 dB. The ideal insertion loss is 6 dB and the insertion loss in operating band came out to be around 7 dB.

At 17 GHz, the return loss came out to be 22 dB, the average insertion loss of branches came out to be 6.9 dB; thus the loss added by the branches is measured as 0.9 dB, better than microstrip, as expected. In SSS, mainly conductor loss is effective due to thin suspended substrate dielectric.

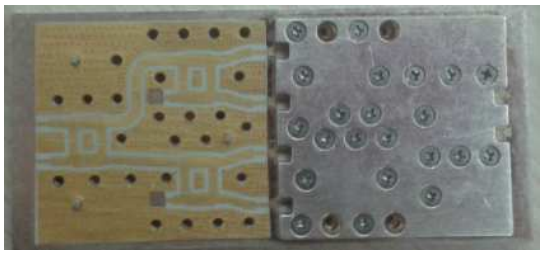


**Figure 1.9:** View of one prototype planar probe CWG combiner

3) Planar probe coaxial waveguide combiner:

The main focus of this thesis is to examine the technique of using coaxial waveguide (CWG) structures with planar probes in power combining in expectation of less combiner loss ([16], [18]). For this purpose, 8-way planar probe CWG combiners are designed and built in 8.5-11.5 and 15.5-17.5 GHz bands. Picture of one of the prototypes is shown in Figure 1.10. The input return losses of the produced combiners came out to be better than 12 dB. The ideal insertion loss is 9.03 dB and the insertion loss in operating band for both bands came out to be around 9.5 dB.

For the combiners operating at 15.5-17.5 GHz, at 17 GHz, the return loss came out to be 16 dB, the average insertion loss of branches came out to be 9.5 dB; thus the loss added by the combiner came out to be 0.5 dB.

Among these combiners, the lowest insertion loss is achieved by the planar probe CWG combiner. This is expected because both dielectric loss and conductor loss are minimized in the media where EM propagation occurs. After observing this

result, this type of combiner is selected to be used in an amplifier module where 2 W output MMIC elements are combined. Two modules were built and tested for 8-12 GHz and 15-18 GHz bands successfully with output powers of approximately 15 watts.


**Figure 1.10:** View of one of the prototypes for planar probe CWG combiner

# CHAPTER 2

## DESIGN AND REALIZATION OF A 6-18 GHZ 8-WAY MICROSTRIP WILKINSON COMBINER WITH CIRCULARLY PLACED INPUTS

In this thesis, the first combining technique which will be investigated is the usage of microstrip lines. Microstrip is the most widely used type of transmission line in commercial and military applications, due to its ease of fabrication and assembly. In order to investigate this technique, an 8-way Wilkinson power combiner is designed using microstrip lines as its branches. In this design, the cladding is selected and input positions are organized such that the best possible performance is achieved using microstrip technique. In other words, the performance degradation will be due to microstrip transmission technique; not due to unnecessary line connections caused by design. Hereby, the combiner will be a good reference for investigating the limitations of microstrip technique.

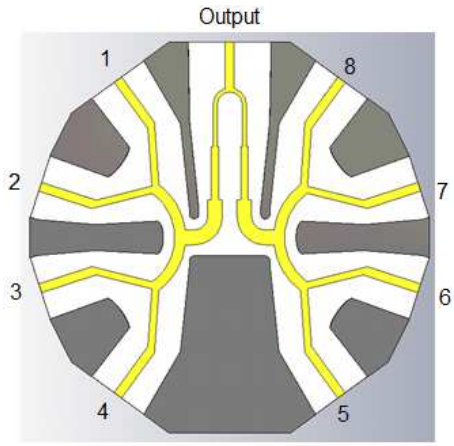



**Figure 2.1:** Layout of the 8-way microstrip Wilkinson combiner

For this combiner, with the layout in Figure 2.1, inputs 1 to 8 are placed at the edges of a planar octagon-like shape. A similar study was presented by Rector in [23]. Input lines are combined in binary logic; i.e. two branches are combined at each step. Combined branches travel to the center of the octagon in an 8-way symmetry. Thus each input path has the same electrical length from input port to the center. From the center, combination of inputs 1-4 and 5-8 are carried to output port as two parallel branches. At output port they are combined and this is the last binary step of the combination.

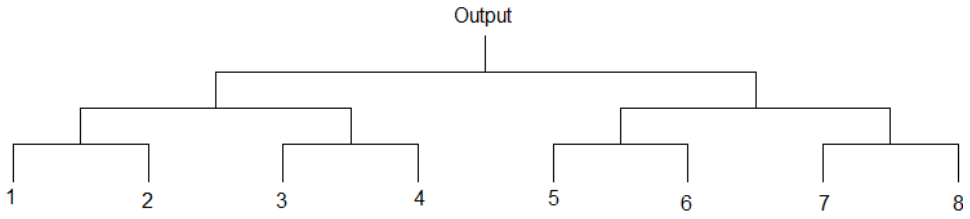



**Figure 2.2:** An 8-way binary combiner where the inputs are on a straight line

The configuration of branches allows much smaller electrical lengths compared to the case more often used, where the inputs are placed on a straight line, as seen in Figure 2.2. In the straight line case in Figure 2.2, the inputs at the edges (1 and 8) are the farthest, and usually more than necessary far from the output. Because of this distance, the branches between 1 and 8 to output must be long transmission lines. However, it is necessary to obtain matching of input path electrical lengths, thus the insertion phases. Thus, the path lengths of other nearer inputs (from inputs 2-7 to output) must be the same as the length of the longest path (from inputs 1 and 8 to output). For instance, the path from input 4 to the output turns out to be much longer than the actual distance between input 4 and the output. As microstrip loss increases with line length, this excessive length brings excessive loss. The branch loss, equal for all branches, is determined by the farthest input path.

In the design of this combiner, different from conventional configuration (Figure 2.2), these unnecessarily long paths are avoided. The inputs are placed in a circular symmetry (Figure 2.1). Actual distance from the output to input port is the same for all 8 inputs. Path lines are short and equal to each other. Thus the insertion

loss is determined by the short common path and becomes much smaller compared to conventional configuration (Figure 2.2). This will minimize the insertion loss which can be achieved by microstrip, to be used for comparison. If the output connector was placed at the center, even shorter lines would be achieved, however this is not considered and output is carried to outer boundary where the inputs are placed, in order to have more practical connection.

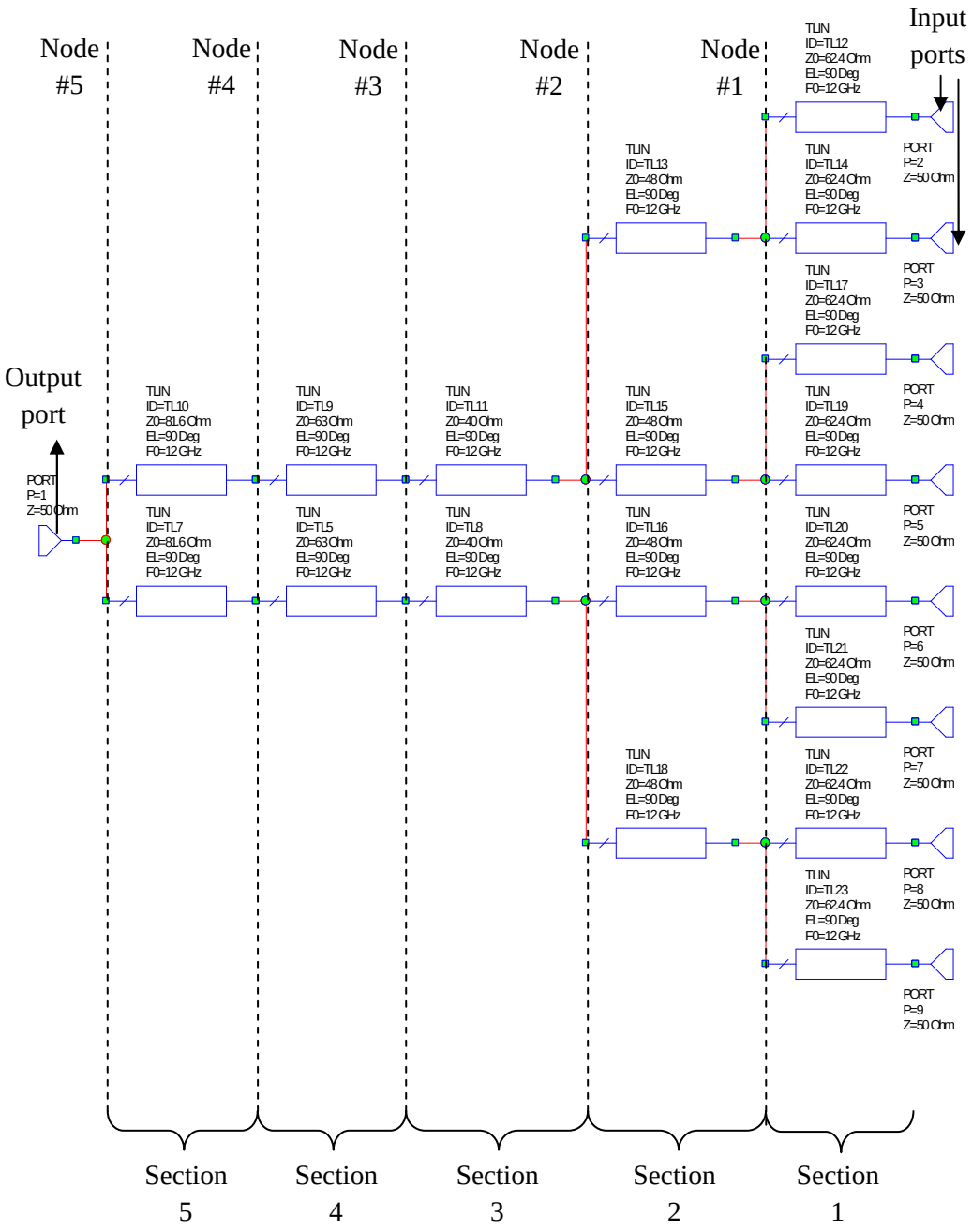



**Figure 2.3:** Schematic of the 8-way microstrip Wilkinson combiner

The schematic of the combiner with the layout in Figure 2.1 is given in Figure 2.3. This schematic can be divided into 5 sections numbered in the figure. Each section is composed of a number of transmission lines with equal impedance. The sections are separated by node group lines which are also numbered in Figure 2.3. For targeted operation, voltages generated on node points are examined in order to help simplifying the design procedure. The combiner is assumed to be evenly fed from its 8 inputs. The schematic is electrically symmetric; thus when one of the node groups is selected, nodes forming that group are electrically the same. In other words, all nodes in a selected node group will carry the same voltage. Using this property, a node group can be treated as a single node. This means the lines between two node groups (a section) become lines between two nodes, i.e. parallel connected lines. Thus, each section can be represented as a single transmission line equivalent to the lines of that section. This approach removes all parallel connections and transforms the circuit into pure series form, as given in Figure 2.4.

In Figure 2.4, which is obtained by simplifying Figure 2.3, the combiner turns out to be a multistage QWL matching structure between 6.25 and 50 Ω. In the design, the available theory for multistage QWL matching was used. Using this theory and AWR Microwave Office® as a linear simulation tool, the impedance values are optimized for the targeted bandwidth.

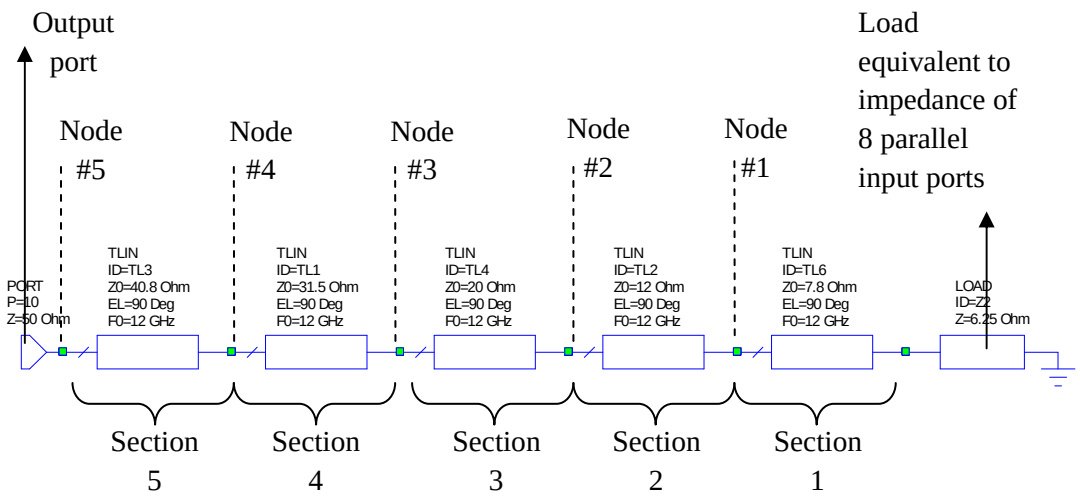



**Figure 2.4:** Schematic of the 8-way microstrip Wilkinson combiner in series form

In this design, a 5-section circuit was found sufficient to obtain the frequency band. Initial values are selected using the approach in [2]. Afterwards, the impedance values are optimized in AWR Microwave Office® in order to obtain a smoother frequency response. From sections 5 to 1, the characteristic impedances are selected as 40.8, 31.5, 20, 12 and 7.8 Ω, respectively.

The linear simulation result of the schematic is seen in Figure 2.5. The output return loss ($S_{11}$) is simulated as better than 20 dB. The ideal insertion loss ($S_{21}$) is 9.03 dB and the insertion loss in operating band came out to be around 9.05 dB, thus the loss added by the combiner came out to be 0.02 dB. In linear simulation, the conductor and dielectric losses are not considered, insertion loss arises only from mismatch loss; thus the observed value is very low.

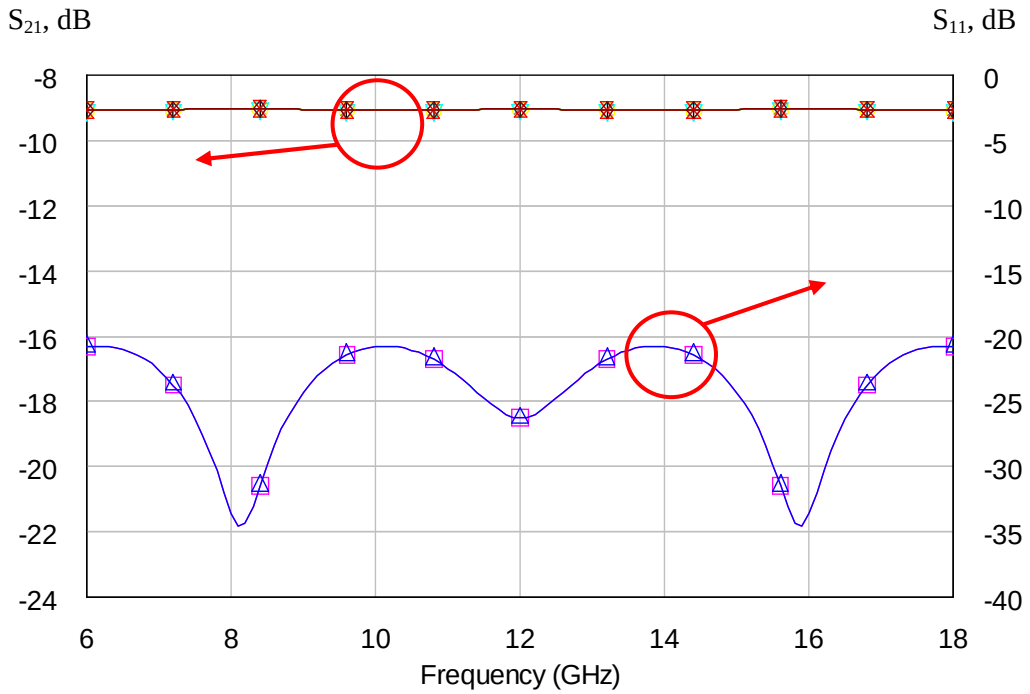



**Figure 2.5:** Linear simulation result of the impedance transformation circuit

At the next step, the actual schematic (Figure 2.3) is obtained by calculating the equivalent characteristic impedances. When the schematic is determined, the layout seen in Figure 2.6, is drawn and simulated in 3D EM software of CST Microwave Studio®. RO3003 is picked as the substrate with relative dielectric constant 3. The height of the substrate is 0.254 mm. The substrate is cladded by 17 micron thick rolled copper and no other cladding is applied afterwards. Some impedance and length values needed to be optimized to approach the ideal response. The deviations from calculated impedances were due to closely spaced walls between the lines. The need of placing these walls was to improve isolation and

avoid cavity resonance in the overall structure. However, to keep the combiner compact enough, some of the walls needed to be placed very close to the transmission lines (Figure 2.6). This affects the effective dielectric constant throughout the lines; because at side wall boundaries the fields are not negligible but forced to obey the wall boundary conditions. Thus, both calculated impedances and electrical lengths are changed, and this brings the need of optimization.

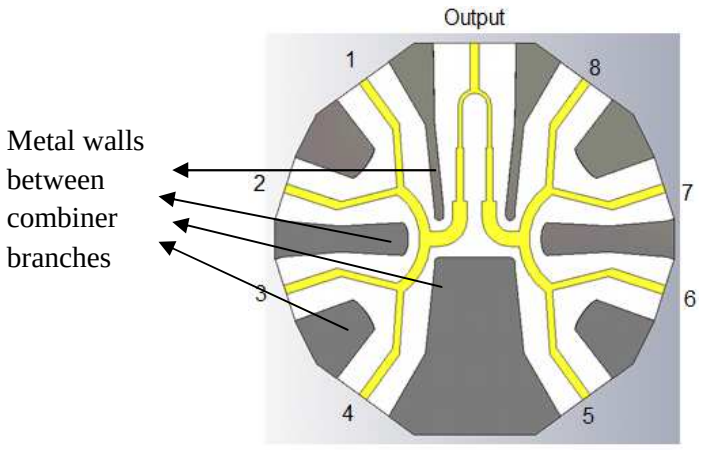



**Figure 2.6:** Metal walls in 8-way microstrip Wilkinson combiner

The 3D simulation result for the optimized values is given in Figure 2.7. The output return loss is seen as better than 19 dB. The ideal insertion loss for 8-way

comibners is 9.03 dB and the insertion loss in operating band came out to be around 9.25 dB, thus the loss added by the combiner is 0.25 dB per branch.

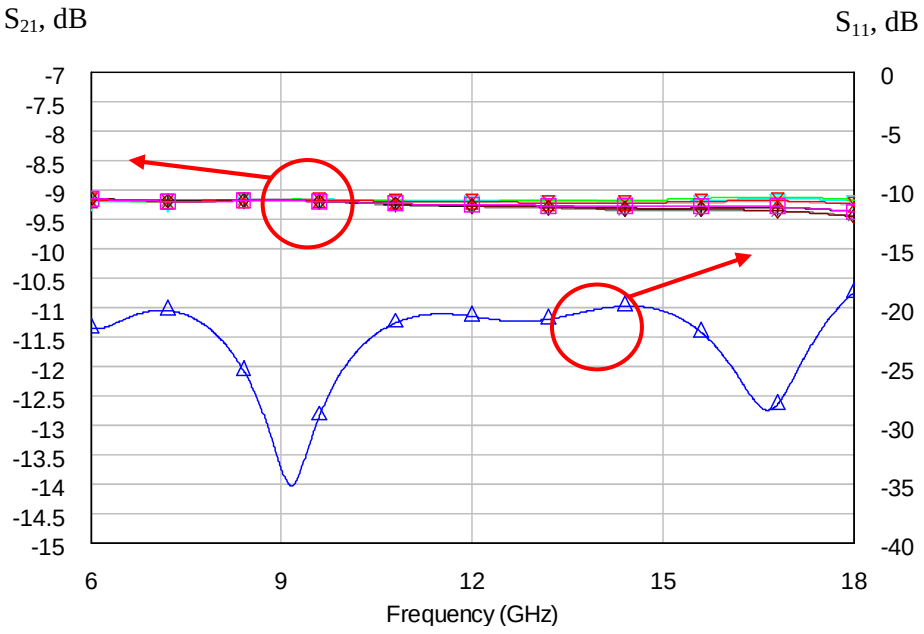



**Figure 2.7:** 3D simulation result of the 8-way microstrip Wilkinson combiner

The measurement result of the manufactured combiner is given in Figure 2.8. On the return loss trace, there are repeating notches due to non-ideal transition junctions. This characteristic caused increase on the return loss at periodic points;

overall return loss is seen as better than 10 dB. In microstrips, losses are due to both conductor loss and dielectric loss. As expected, insertion loss between input of one branch and the output is about 10 dB, getting closer to 9.5 dB near the lower edge of the band and about 10.5 dB near the upper edge of the frequency band. Therefore, extra introduced loss of the combiner is less than 1.5 dB in the frequency band. This value is better when compared to the other microstrip 8-way binary combiners of which inputs are placed on a straight line. These results could be taken as the attainable best ones that can be obtained by a microstrip combiner, since path lengths for conductors are minimized. The results will be used while comparing by the other combining techniques, SSS combiner and planar probe CWG combiner. After comparison, it was seen that microstrip combining has the lowest loss among the three techniques.

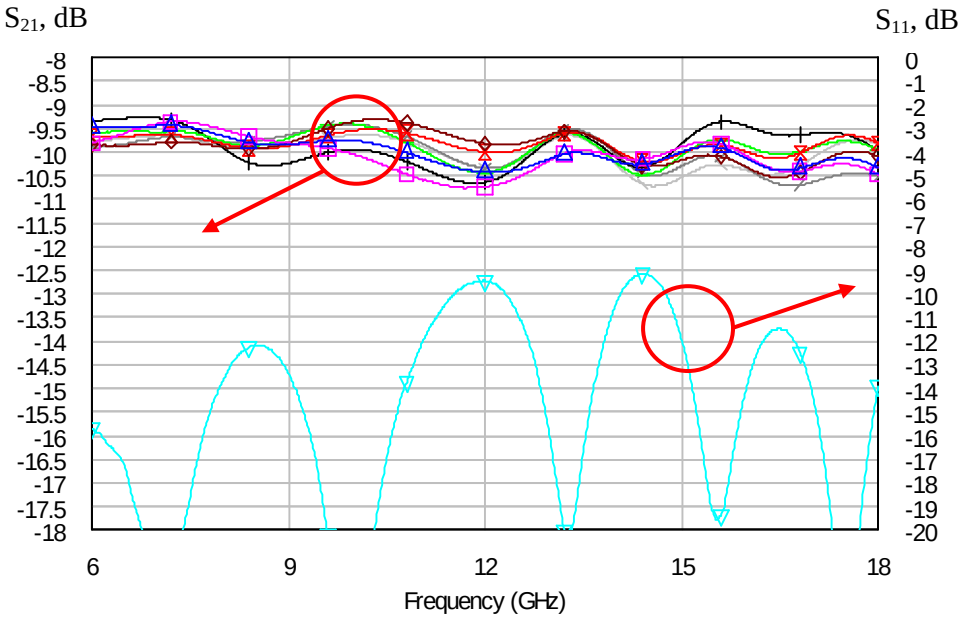



**Figure 2.8:** Measurement result of the 8-way microstrip Wilkinson combiner

# CHAPTER 3

## DESIGN AND REALIZATION OF A 4-WAY SUSPENDED SUBSTRATE STRIPLINE BRANCHLINE COUPLER

After the conventional microstrip line technique, another low-loss one, the SSS technique will be investigated. In this technique, transmission lines are constructed such that a copper sheet is placed on a dielectric substrate, where the dielectric substrate is suspended in air and the air is enclosed by metal walls. The usage of air medium decreases the dielectric loss, which is the reason of expecting lower loss than microstrip line technique. In order to investigate this technique, a 4-way branchline coupler is designed by suspended substrate striplines.

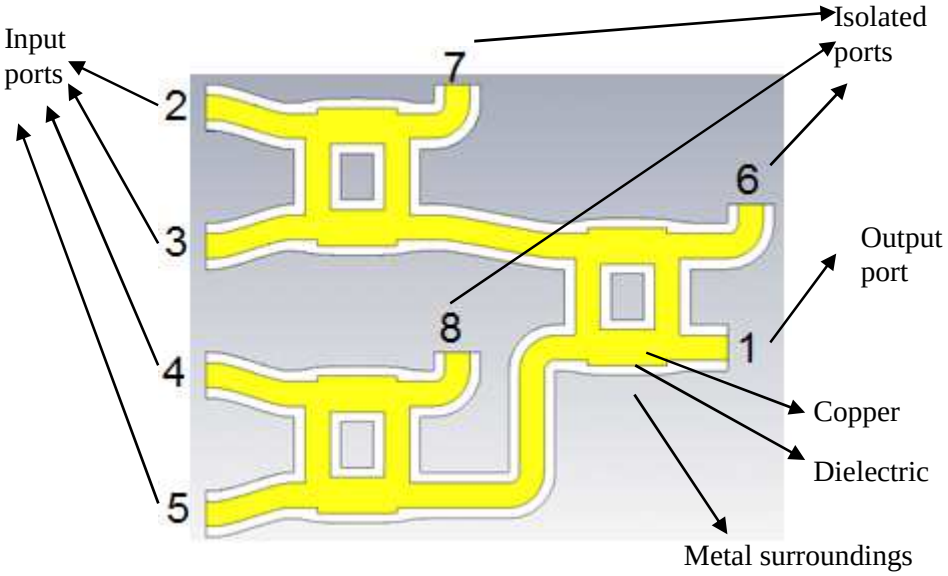



**Figure 3.1:** Top view of the 4-way SSS branchline coupler

The board layout of this combiner is shown in Figure 3.1. There are four input ports and three isolated ports which are terminated by a well-matched load. In order to minimize dielectric losses, transmission lines are made up by SSS structures. In this structure, seen in Figure 3.1, effective dielectric constant is reduced by placing the substrate between top and bottom air layers which have 0.5 mm thickness each. This brings both longer wavelength and the need for longer lines, but also brings wider lines. Change in width is more significant than change in line lengths. Thus, decrease in loss due to width increment will be more significant; rather than the increase in loss due to length increase. This results in less copper loss. In addition, the fields tend to propagate in TEM mode, where the line on the

substrate acts equivalent to the center coax conductor. This similarity is due to the surface currents on the inner metal walls, and the dielectric used by EM waves is mostly air. The average dielectric loss is reduced compared to a fully-loaded dielectric case. Furthermore, when the inner plating of the walls is chosen from good conductors like gold and silver, the conductor loss will also be reduced.

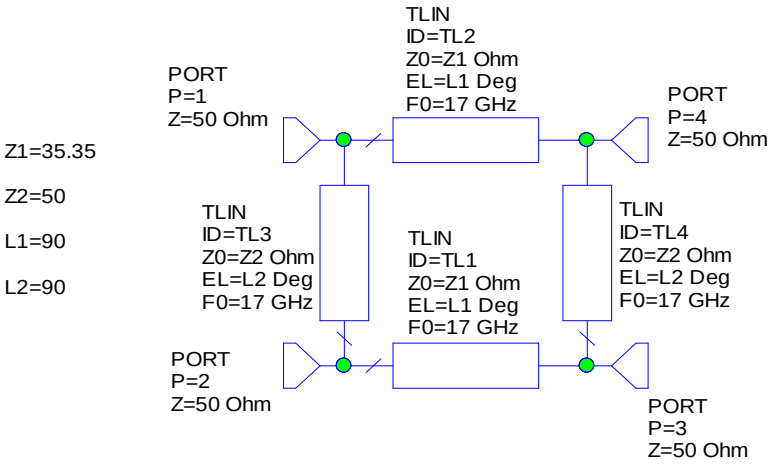



**Figure 3.2:** 2-way branchline coupler circuit

The technique is applied in a branchline coupler circuit. A 4-way coupler is designed by using 2-way couplers in cascade, where two branches are combined at a time. First, the 2-way branchline coupler schematic, seen in Figure 3.2, is created to use as a starting block. A branchline coupler in general is a 4-port network. In addition to the input port there are two output ports and an isolated port. The ports

are connected via four transmission lines and all ports are assumed to be terminated by known reference characteristic impedance Z0. In the schematic shown in Figure 3.2, the line between ports 1 and 2 and the line between ports 3 and 4 has characteristic impedance equal to the known reference characteristic impedance. The line between ports 1 and 4 and the line between ports 2 and 3 have characteristic impedance equal to $1/\sqrt{2}$ of the known reference characteristic impedance. The length of each four transmission line is equal to QWL at the center frequency. For this configuration, when Port 1 is the input port, Port 3 and Port 4 are the output ports and Port 2 is the isolated port. The power magnitude of signals reaching ports 3 and 4 are the same and equal to the half of the power at Port 1. However, in terms of phase, the signal at Port 3 is lagging the signal at Port 4 by $90^{o}$. In theory, no signal is transferred to the isolated port, Port 2.

The linear simulation result of the circuit is shown in Figure 3.3. The input return loss is better than 25 dB. The ideal insertion loss is 3.01 dB and the insertion loss in operating band is seen around 3.03 dB, thus the loss added by the combiner is seen as 0.02 dB. The 4-way coupler circuit will be formed by placing two 2-way couplers at the input of another one. This final form is not designed and only simulated in linear simulation software.

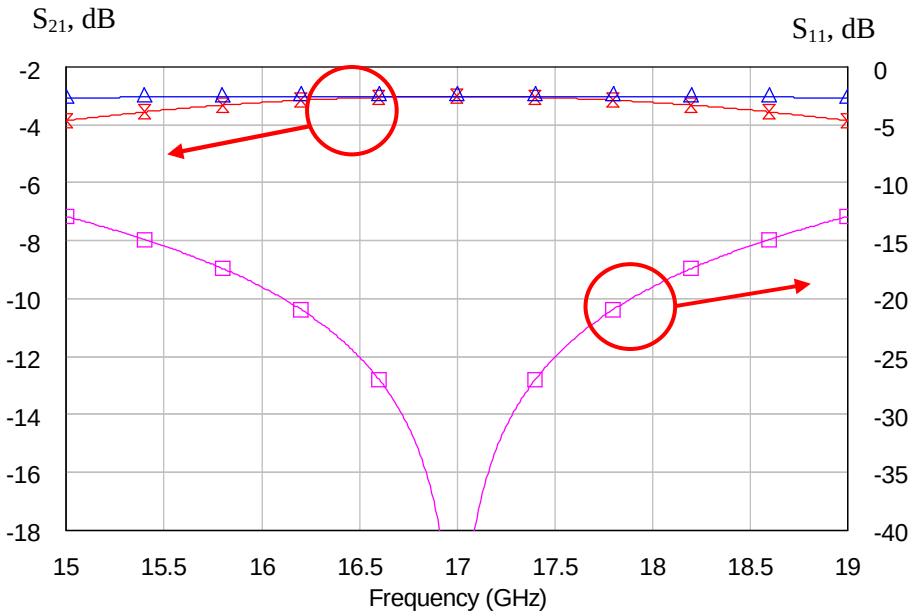



**Figure 3.3:** Linear simulation result of the 2-way branchline coupler

The 3D model of the final form is constructed in CST Microwave Studio® by using the impedances of the schematic (Figure 3.2). The substrate is picked as RO3003 with relative dielectric constant 3. The height of the substrate is 0.254 mm. 0.508 mm of air is left on both top and bottom sides of 0.254 mm-thick substrate. The substrate cladding is copper of 17 micron thickness and no other cladding is applied afterwards. The transmission lines are closely placed near narrow sidewalls to avoid possible undesired mode excitations. The width of these narrow channels

where the lines are placed is 2.5 mm, that is QWL at 30 GHz which is sufficiently far from the upper edge of the band.

The close sidewalls will change the effective dielectric constant, because at side wall boundaries the fields are not negligible, but forced to obey the wall boundary conditions. Instead of theoretical calculation, the line widths and lengths are found by sweeping related parameters in 3D simulation in order to obtain required values. The final layout of 4-way combiner can be seen in Figure 3.4, where 6 is the output port, 2, 3, 4, 5 are the input ports and 1, 7, 8 are the isolated ones.

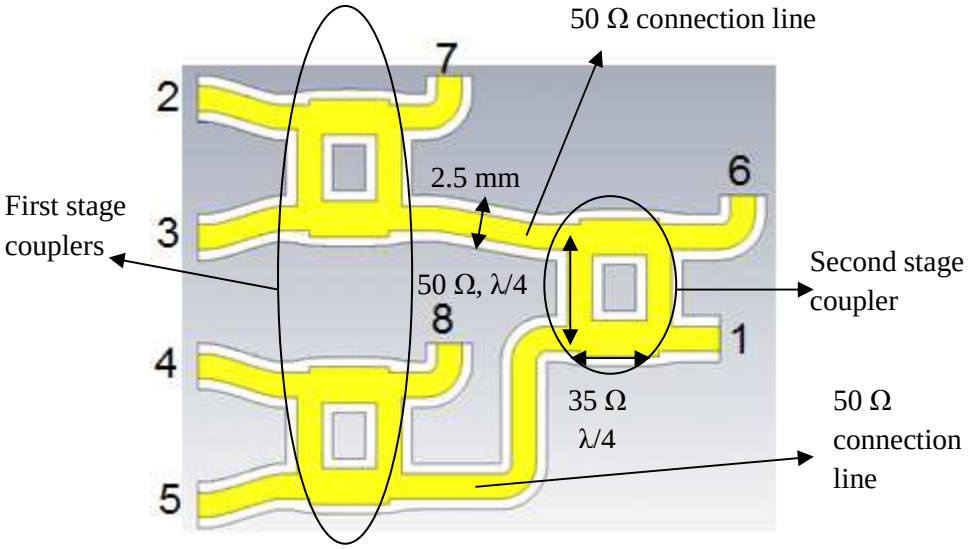



**Figure 3.4:** Final layout of the 4-way SSS branchline coupler

In the simulation, all isolated ports are terminated by 50 Ω loads. The 3D simulation result of this layout is given in Figure 3.5. The input return loss is better than 22 dB. The ideal insertion loss is 6 dB while combining 4 inputs and the insertion loss in operating band is around 6.25 dB, thus the loss added by the combiner is seen as 0.25 dB.

In 3D simulation using CST Microwave Studio®, the walls surrounding the transmission lines are made up by perfect electric conductor (PEC). In the production of the structure, walls cannot be placed next to the substrate edge, which requires cutting away some parts of the substrate layer. This is not desirable because it damages the integrity of the substrate board and complicates correct alignment of transmission lines with respect to air. In production, the substrate board is kept as a single layer and squeezed between top and bottom metals. The ground effect near transmission lines is achieved by placing closely spaced metal plated via holes near all transmission line edges. There are also 3 guide pins added to the metal body and pin holes added to the substrate, in order to provide correct positioning of the combiner substrate board. The pins and via holes are shown in Figure 3.6.

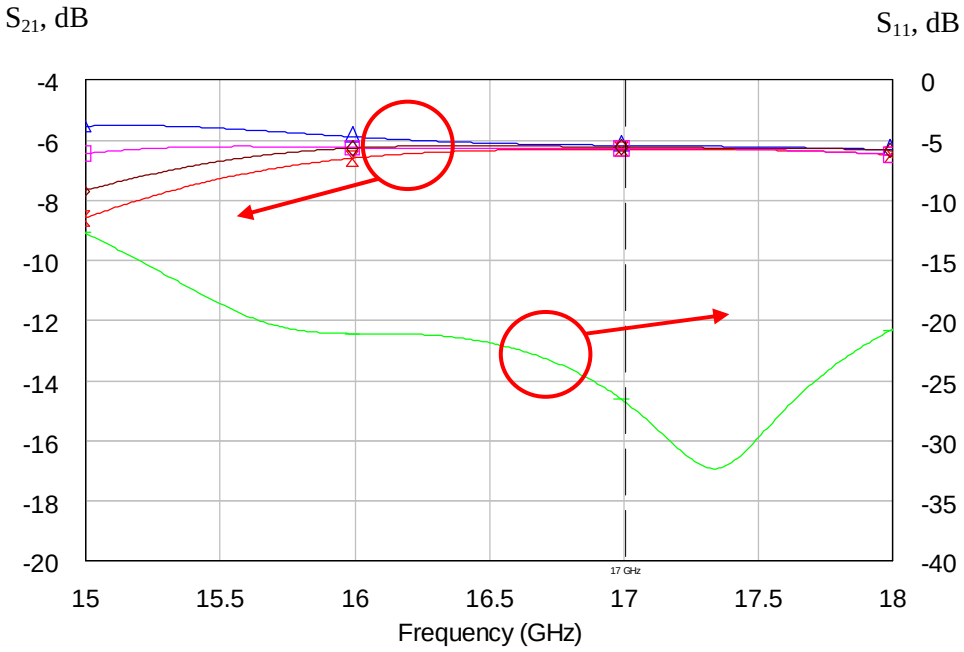



**Figure 3.5:** 3D simulation result of the 4-way SSS branchline coupler

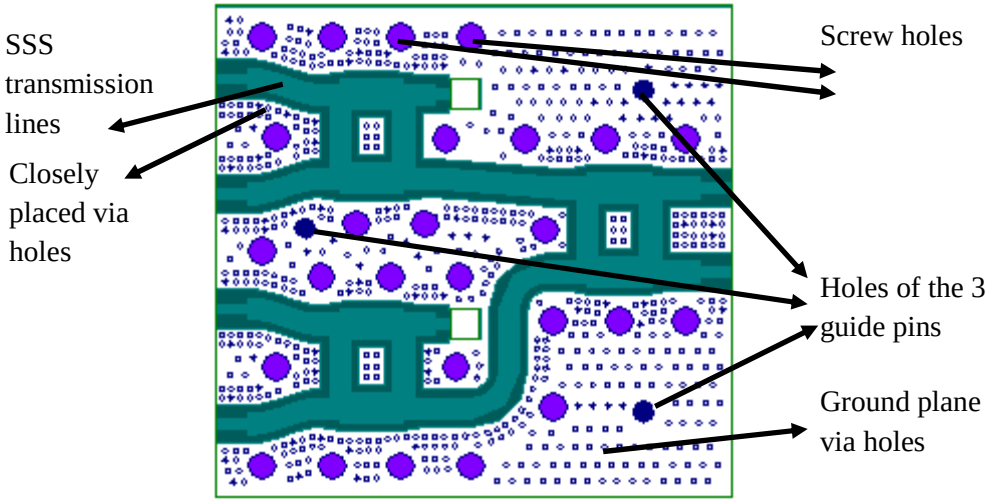



**Figure 3.6:** Via and pin positioning of the SSS combiner substrate board

The isolated ports are terminated by 10 dB attenuators, which brings 20 dB return loss, so well matching at isolation ports. For sure, other terminals of the attenuators should be left open. This method is chosen instead of using a 50 ohm resistor, because ethe return loss of 10 dB attenuator is measured to be higher than the available 50 ohm resistor.

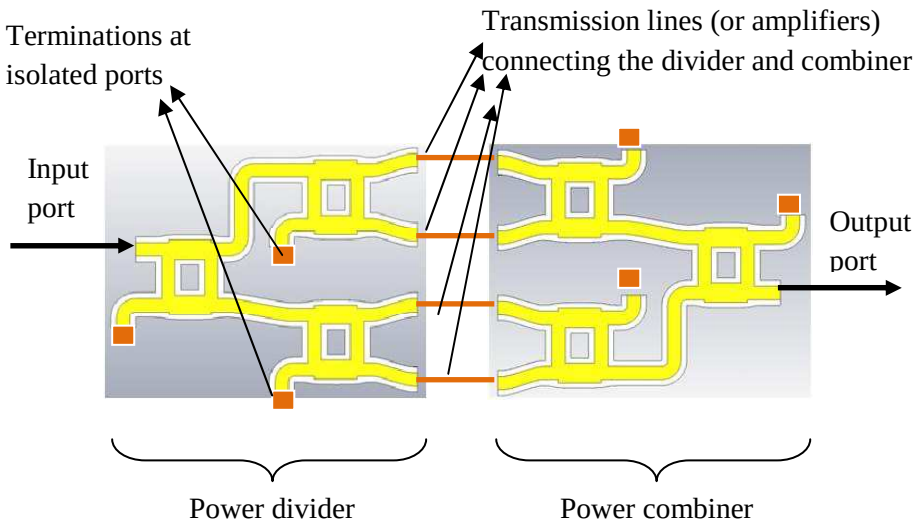



**Figure 3.7:** Combining circuit by 4-way SSS branchline coupler

There is an asymmetry in the layout, which needed to be given in a fixed order while combining in order to maintain input ports evenly spaced. The power is first divided by this coupler and the coupler feeds amplifiers connected to four branches; then amplifier outputs are combined by an identical coupler. The total paths followed by each branch, as seen in Figure 3.7, are physically and electrically equal. Thus, the total phase shift introduced by the structure for each branch will be the same. The length difference between coupler outputs may still cause amplitude imbalance at the input and power loss at the output. However, the insertion loss caused by length difference is negligibly small; thus, amplitude imbalance is neglected in this design.

The measurement result of the produced combiner is given in Figure 3.8. The curves are observed to be consistent with the ones obtained by 3D simulation. The input return loss came out to be better than 19 dB. In SSS loss, losses are due to both conductor loss and dielectric loss, mostly due to conductor loss because dielectric loss is minimized. As expected, insertion loss between one input branch and the output came out to be about 6.8 dB, getting to close to 6.7 dB near the lower edge of the band and about 6.9 dB near the upper edge of the band. Therefore, extra introduced loss of the combiner came out to be less than 0.9 dB in the frequency band. With respect to microstrip loss at the same band, these values are lower. This is expected because in SSS, dielectric loss is not as effective as in microstrip case. However, at the same frequency band, better insertion loss characteristics are achieved by the combiners designed by planar probe coaxial waveguide (CWG) technique described next.

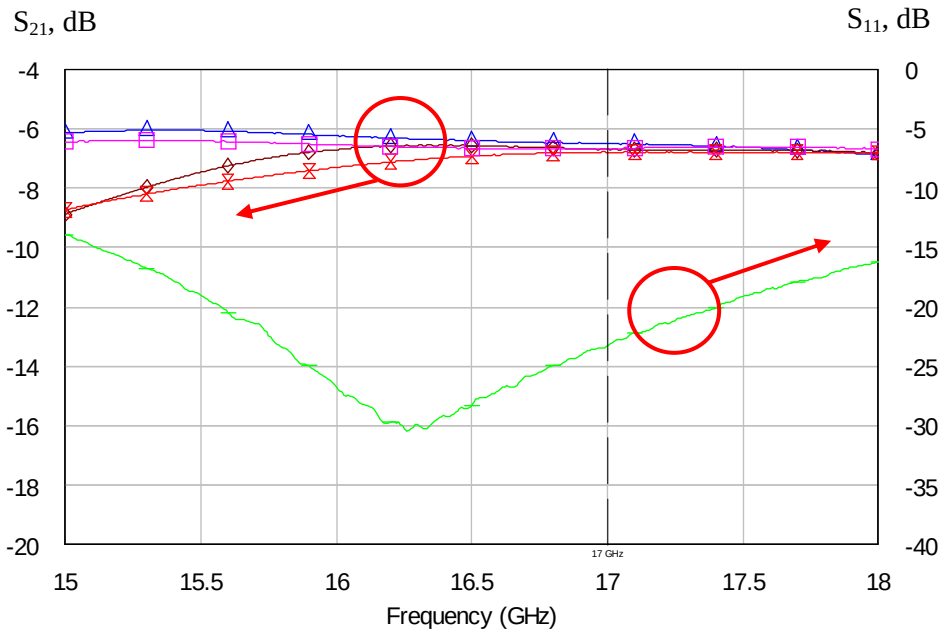



**Figure 3.8:** Measurement result of the 4-way SSS branchline coupler

# CHAPTER 4

## QUALITATIVE DESCRIPTION AND DESIGN METHODS OF PLANAR PROBE COAXIAL WAVEGUIDE COMBINERS

The introductory papers on planar probe CWG combiner are listed in [16] and [18]. The operation principles presented are summarized below. The design steps used in this thesis are also defined qualitatively.

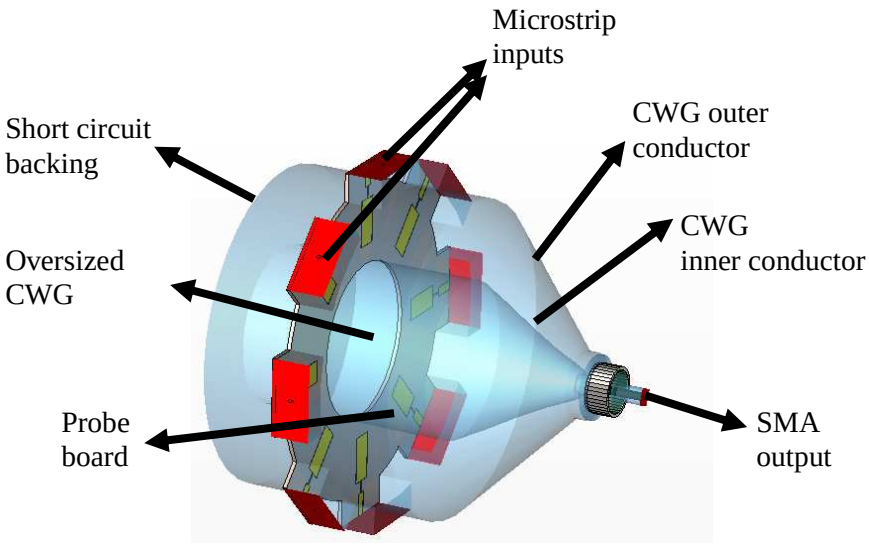



**Figure 4.1:** Conceptual picture of a planar probe CWG combiner

Figure 4.1 shows a conceptual picture of an 8-way planar probe CWG combiner. The combiner structure can be coarsely defined as a cylindrical oversized waveguide with the inputs placed on the side surface in axial symmetry and the output placed on the top. Power combining takes place within the oversized waveguide which is then tapered to match a standard SMA connector.

In Figure 4.2, a top view of the input plane is given and the ports are numbered for an 8-way combiner. The output is shown as number 0, and it is oriented orthogonal to the viewpoint of the illustration.

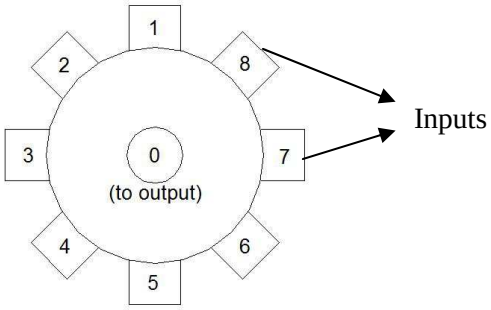



**Figure 4.2:** Ports of an 8-way planar probe coaxial waveguide combiner

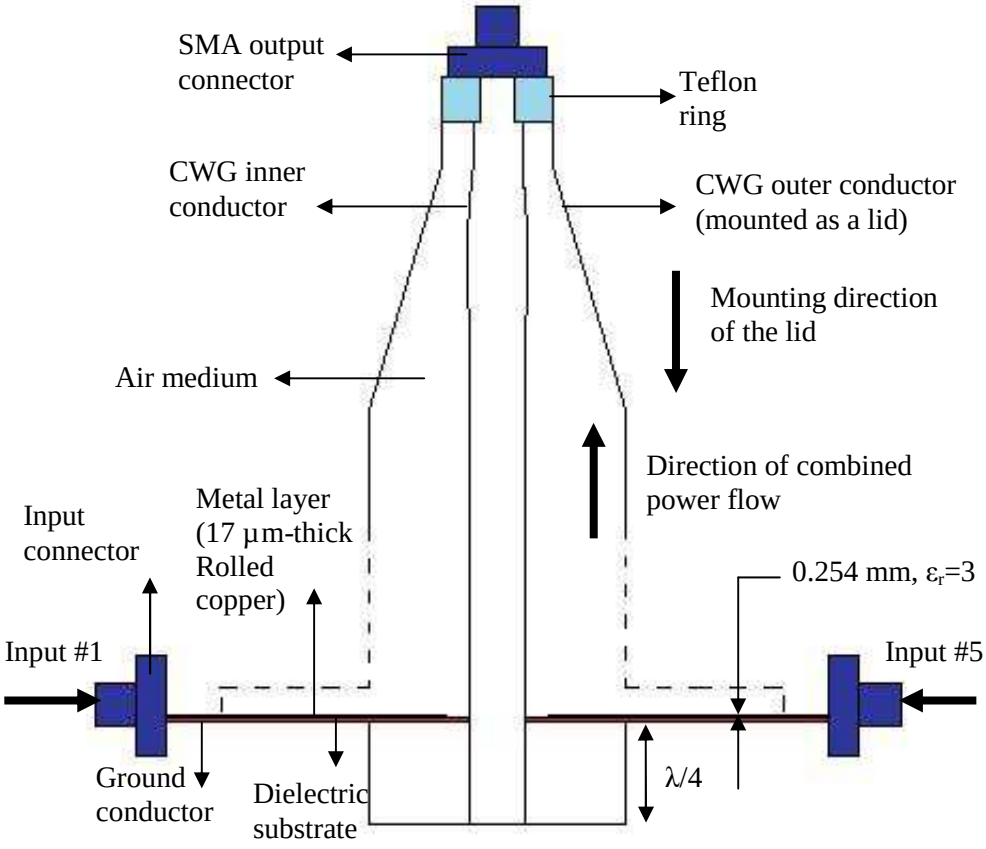



**Figure 4.3:** Longitudinal cross section of a planar probe CWG combiner

Longitudinal cross section of the structure is shown in Figure 4.3. In this cross section, only two inputs standing on opposite sides are seen. The output of the combiner is seen at the top. After mounting, an air-filled CWG cylinder is obtained, with a dielectric substrate board near the bottom surface. Power transferred by the

inputs radiated from the substrate and flew toward to the output, in the direction illustrated in Figure 4.3.

In planar probe CWG power combiner, oversized coaxial line dimensions should be reduced to standard SMA dimensions at the CWG matching block by tapering. For the ease of assembly, the outer conductor of the taper is mounted as a lid (Figure 4.3). In [18], an analytic approach is described how the taper is designed. The approach does not take evanescent modes into consideration. On the other hand, highly accurate 3D EM simulation tools (CST®, HFSS®) are available, so the analytic approach is not preferred in the design procedure.

The overall design is divided into three main blocks to ease the design procedure. In Figure 4.4 and Figure 4.5, the design blocks are shown.

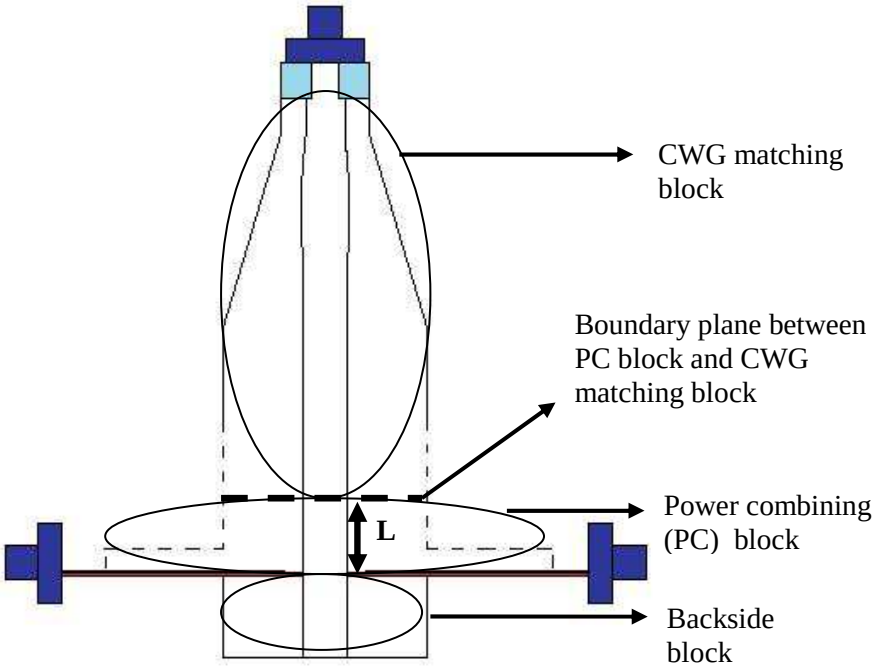



**Figure 4.4:** Design blocks in longitudinal cross-section view

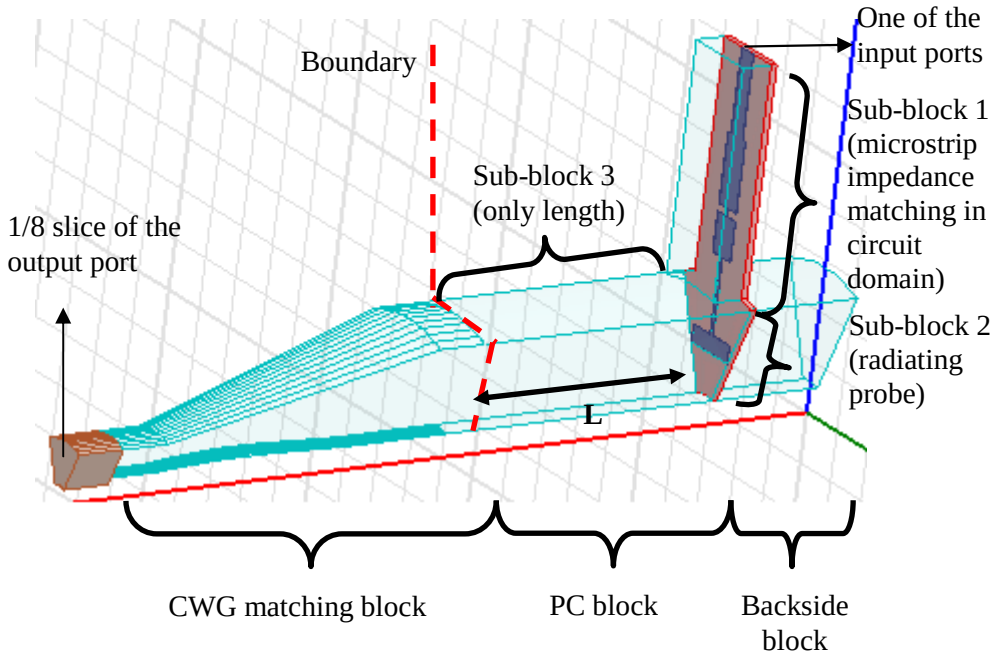



**Figure 4.5:** Design blocks in 3D slice view

The simplest block is the backside block, the ending part of the combiner. It is the CWG section positioned between short circuit (SC) backing and the substrate board. The backside block prevents power traveling to the opposite direction of the output.

Another block is the power combining (PC) block. PC block includes the inputs, the dielectric substrate board and part of the CWG on top of the board. In this block, power is fed to the substrate board and radiated into the CWG where the combination occurs. Selection of L depends on the selected design method.

PC block is divided into 3 sub-blocks as shown in Figure 4.5. Sub-block 1 is formed by the input feed lines which are stepped for impedance matching. They are placed on a dielectric substrate, thus forming a microstrip structure. Sub-block 2 is formed by the radiating probes which are the extensions of input feed lines and placed on the same plane of the substrate board (Figure 4.6). Axially symmetric inputs stand on the edges of the circular planar substrate board. Sub-block 3 is the oversized CWG section of length L. The length L should be high enough to allow the decaying of evanescent fields arising in the power combining structure.

Details of Sub-block 1 and Sub-block 2 are shown in Figure 4.6 and Figure 4.7. In microstrip input matching section, input power is transferred to probes. In radiation section, this power is exposed to CWG medium.

The last block before the output of the combiner is the CWG matching block (Figure 4.4, Figure 4.5). The function of this block is to transfer the combined power to the output while supplying impedance match to the output connector. The shape of this block is generally conical; because the dimensions of the PC block (~λ/4) are much greater than the output connector dimensions and the CWG matching block must be a tapered transition.

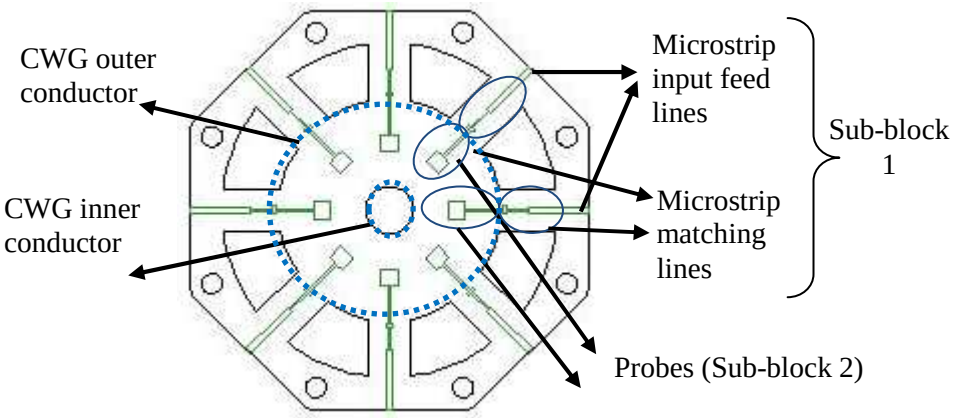



**Figure 4.6:** Layout of the dielectric substrate board

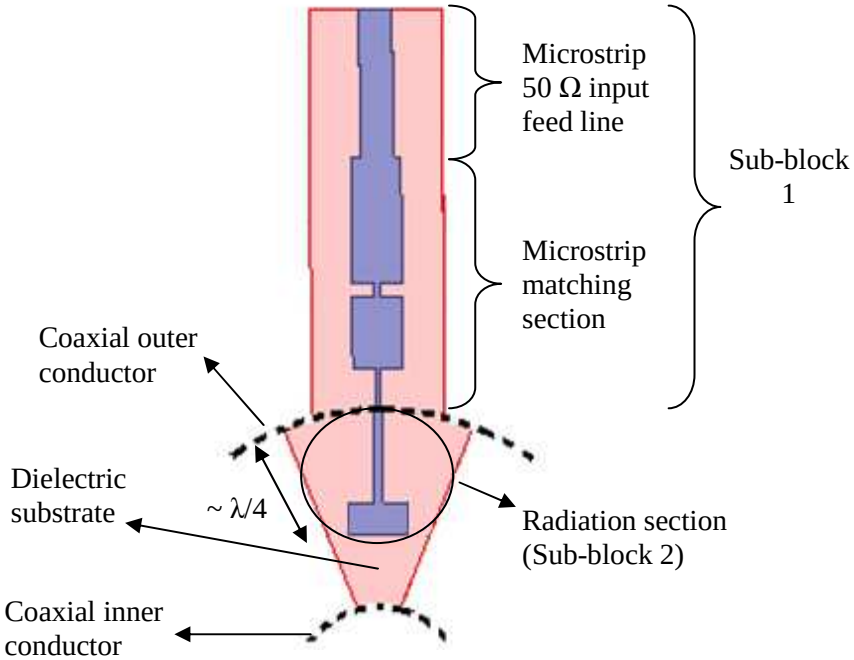



**Figure 4.7:** Input feed structure

In order to apply and investigate this technique ([16], [18]), which is the main focus of this thesis; designs are carried on for two frequency bands: 8.5-11.5 GHz and 15.5-17.5 GHz. Two different methods are found for design and they are both realized.

## 4.1 Design of Backside Block

For both methods selected for planar probe CWG combiner design, the backside block (Figure 4.5), which is the first block to be determined, the approach is the same. The backside section is in an oversized CWG structure which is ended in a short circuit metal wall placed at λ/4 (QW) distance from the plane of probe, in the opposite direction to the output. Thus, an open circuit appears at probe location leading to maximum electric field which allows more efficient power transfer from the probe to the coaxial medium. In Figure 4.8, standing wave E-field lines in the structure are shown with arrows. The sizes of arrows are proportional to field strength. The maximum E-field planes are shown in with blue dashed lines, one of which is coinciding with the substrate plane, as desired.

The probe length should be about QW length for efficient radiation (Figure 4.7). Therefore, the oversized coaxial inner and outer radii are selected to accommodate the probes.

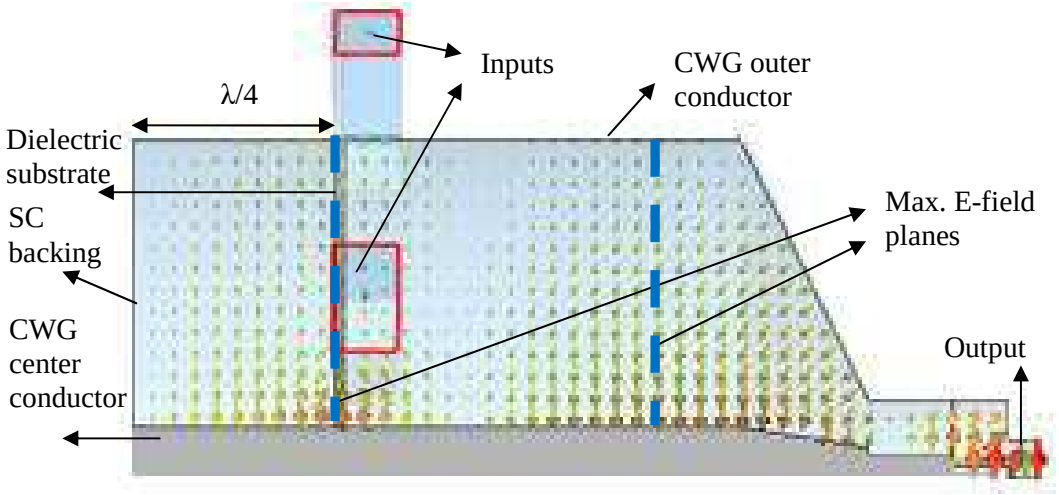



**Figure 4.8:** Example longitudinal e-field distribution in planar probe CWG combiner

The distance between inner and outer conductors is limited by in order to prevent unexpected and undesired mode propagations. It is important to guarantee a single mode operation for efficient power transfer. In this aspect, the combiner is thought as a union of eight identical evenly fed channels. The channels can be thought as the 1/8 slices of a cylinder (Figure 4.5). In each channel, fields propagate from one input to the output independently. The channel lateral cross-section dimensions are chosen small compared to wavelength. The largest cross-section is the one in the oversized coaxial; thus its radii are kept small.

## 4.2 Design of PC Block and CWG Matching Block

Design of the remaining parts use different approaches in the two methods:

### 4.2.1 Sub-block Method

In this method, PC block and CWG matching block (Figure 4.4, Figure 4.5) are designed separately. CWG matching block is a tapered CWG (Klopfenstein taper) which can be treated in exact analytic manner. PC block is designed by three separate sub-blocks. Sub-block 1, the microstrip input feed section has capacitive and inductive line segments. Sub-block 2, being also a part of the input circuit which extends into the CWG is in 2-step planar form. This block acts like an antenna converting input power into EM propagation in CWG. Sub-block 3 is a uniform CWG piece whose length is L (Figure 4.9). The length L is selected such that all evanescent modes decay sufficiently.

The PC block is modeled as seen in Figure 4.9. In this model, only 1/8 slice of the whole structure is simulated. The sides of this model are terminated with PMC boundary, due to electrical symmetry. The top and bottom surfaces are terminated with PEC boundary which corresponds to the metal in the structure. The oversized coaxial port is terminated by a load equal to $8*Z_{ch}$, where $Z_{ch}$ is the characteristic impedance of the oversized coaxial, such that the parallel of 8 slices result in $Z_{ch}$, thus no reflection is seen from that port.

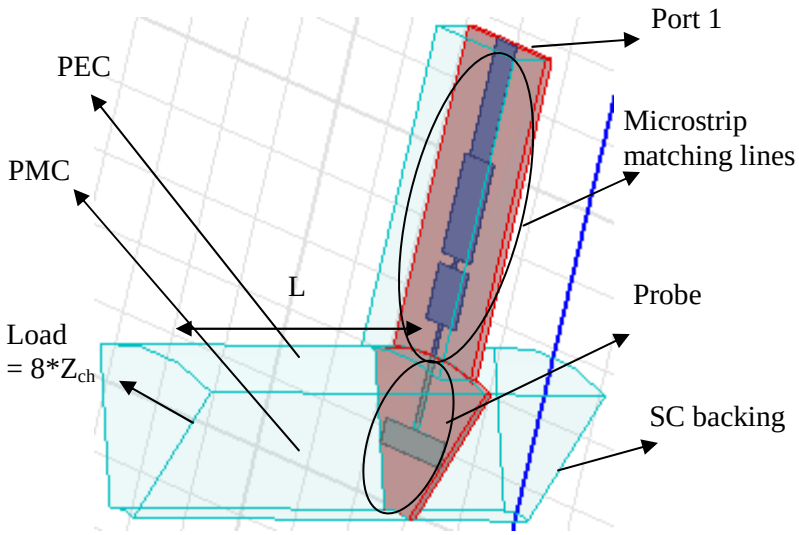



**Figure 4.9:** Simulation model of PC block for sub-block method

The boundary plane that separates PC block and CWG matching block is clarified in Figure 4.4 and Figure 4.5. The characteristic impedance at that plane is fixed at the beginning as $Z_{ch}$, since it is only determined by the radii and the radii are fixed when designing the backside block. In design of each sub-block, a load $Z_{ch}$ is placed at that boundary. This means, after backside block dimensions are fixed, PC block and CWG matching block are isolated from each other in design.

In this method, blocks and sub-blocks of the structure go through the following design flow:

- **Step 1:** Sub-block 2 of PC block is optimized independent from other blocks in HFSS® (3D simulation).

- **Step 2:** Sub-block 1 of PC block is optimized with respect to Sub-block 2 of PC block, in AWR Microwave Office® (linear simulation).

- **Step 3:** Sub-block 3 of PC block (only length) is optimized with respect to Sub-block 1 and Sub-block 2 of PC block in HFSS® (3D simulation).

- **Step 4:** CWG matching block is designed independent from other blocks (theoretically).

**Step 1:**

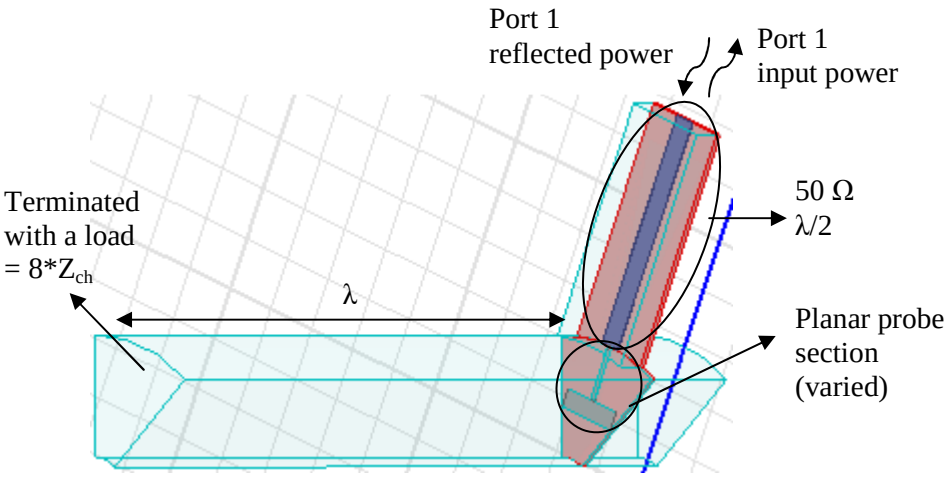



**Figure 4.10:** Simulation block for planar probe section design

Since it is the most critical part in the combiner, Sub-block 2 of PC block is the first one to be designed. A 50 Ω microstrip line of half wavelength is used to feed the radiating probe (Sub-block 2). Then, the probe dimensions (lengths and widths of steps) are swept by observing reflection coefficient ($S_{11}$). In this sweep, 50 Ω line is used as Sub-block 1 (Figure 4.10). In sub-block 3, L is selected equal to one wavelength. After sweeps, the $S_{11}$ traces are plotted with respect to frequency and observed on Smith chart. The probe dimensions giving the trace closest to the center are selected; thus, the probe design is completed.

**Step 2:**

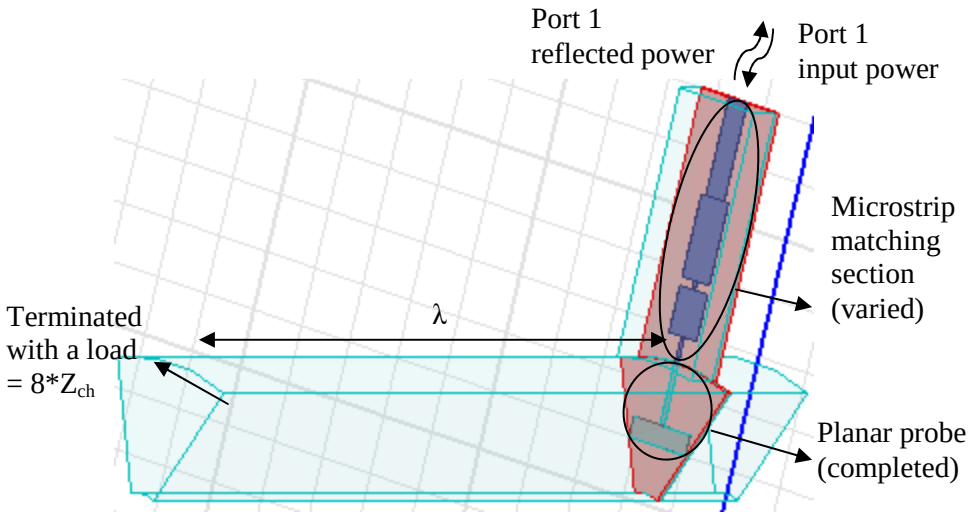



**Figure 4.11:** Simulation model of PC block in sub-block method

After fixing Sub-block 2 of PC block, the 50 Ω line is replaced by a better matching circuit to minimize $S_{11}$ seen at Port 1 (Figure 4.11). The selected probe is

placed in the structure. L is selected as λ and the oversized coaxial is terminated with $8*Z_{ch}$. The microstrip matching lines supply reactive matching on Smith chart of the probe impedance to 50 Ω input. The matching lines can be thought as capacitors and inductors using short length approximation. Reflected power is observed at the input port on Smith chart. The matching section is designed as consecutively placed inductors and capacitors which carry the probe impedance to the center of Smith chart in a few steps.

**Step 3:**

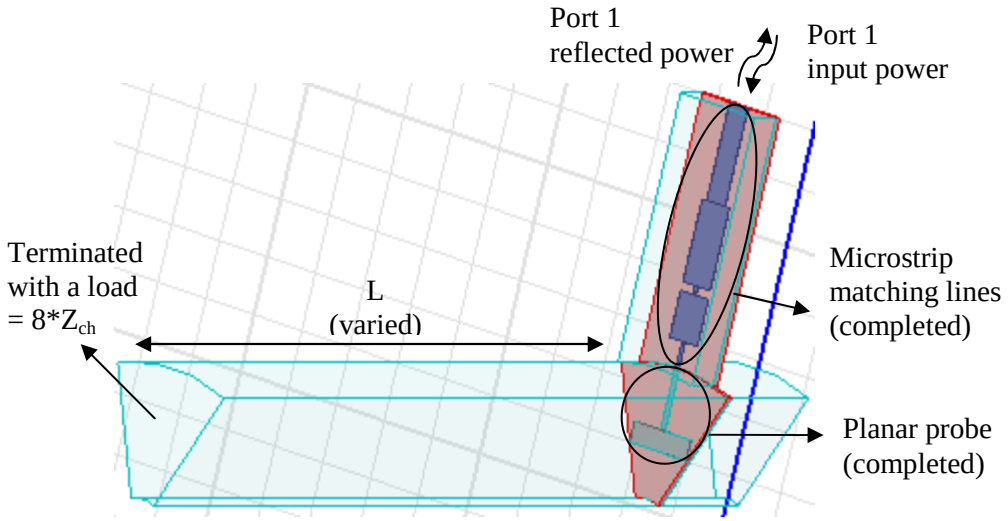



**Figure 4.12:** Simulation model of PC block in sub-block method

At Step 3, oversized waveguide length L length is swept and $S_{11}$ is monitored (Figure 4.12). The shortest possible length that maintains the same $S_{11}$ trace is selected. If oversized coaxial waveguide (OCW) were selected shorter, the fields from probes would not be settled in TEM mode. Therefore, a load $Z_{ch}$ cannot be used in the designs and this spoils the independency of the two sub-blocks, so does the main logic of this method.

**Step 4:**

As the last step, the CWG matching block is theoretically designed as a Klopfenstein taper which transforms $Z_{ch}$ to 50 Ω impedance of the SMA output (Figure 4.13). The taper is selected for strictly wide band and well matching. The PC block impedance may not give the sufficiently less return loss at all frequencies; CWG matching block must be a smooth transformation of that impedance to the output to avoid further mismatch loss.

When the PC and CWG parts are cascaded (Figure 4.5), the combiner structure becomes complete.

The advantage of this method is to be able to design each block separately and more quickly due to systematic approach.

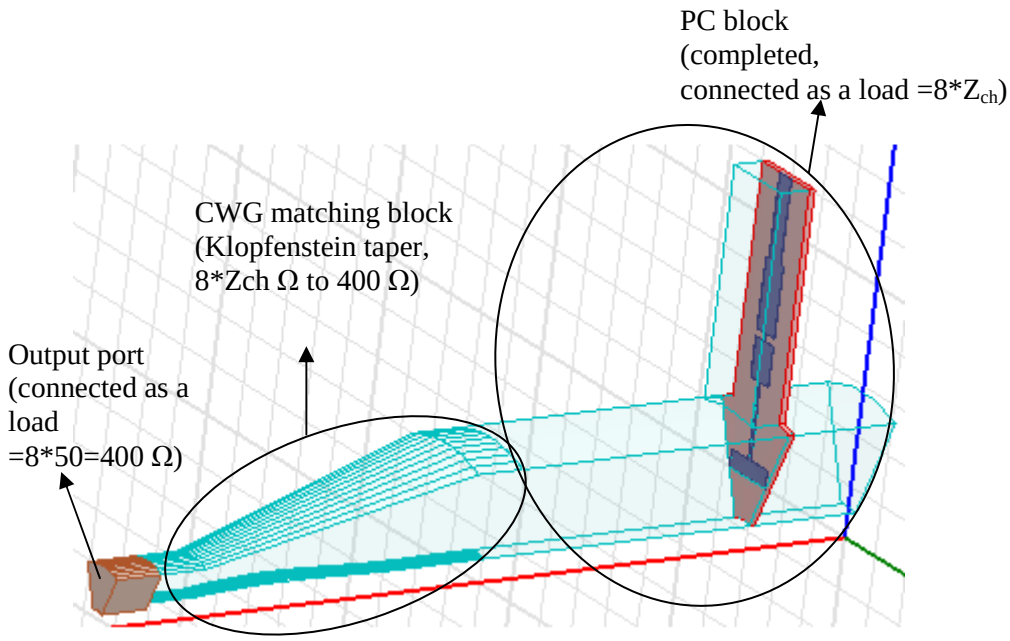



**Figure 4.13:** Design view of CWG matching block for sub-block method

### 4.2.2 Optimization Method

In the previous approach, the tapered section of CWG is designed as a Klopfenstein taper, which sets the tapering length to get the desired bandwidth. Moreover, this taper is placed at a distance L from the substrate. The length of the taper and L are the largest dimensions of the structure; thus they determine the total length. The total length can be reduced by optimizing the whole structure at a time. In this approach, this optimization is applied. As a result, 2 cm decrease in total

length and 0.15 dB decrease in average insertion loss (due to decrease in length) was achieved.

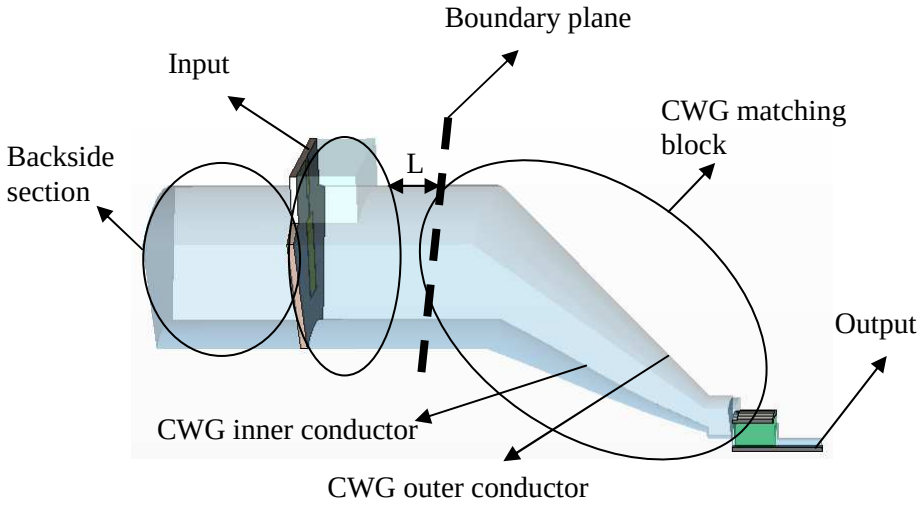



**Figure 4.14:** Design view of the whole structure for optimization method

In this method, blocks and sub-blocks of the structure (Figure 4.14) go through the following design flow:

- **Step 1:** Sub-block 1 and Sub-block 2 are selected to be single stage lines with equal width.

- **Step 2:** Sub-block 1 and Sub-block 2 are optimized together in CST Microwave Studio® (3D simulation). The length of Sub-block 3 of PC block is selected to be 0.5 mm.

(In this step, in order to speed up the design, sweeps for Sub-block 1 can be carried out in AWR Microwave Office®, using extracted Sub-block 2 sweep results obtained from CST Microwave Studio®.)

- **Step 3:** CWG matching block is optimized with respect to PC block in CST Microwave Studio® (3D simulation, whole structure).

- **Step 4:** If necessary, Sub-block 1 and Sub-block 2 are optimized to be stepped lines in CST Microwave Studio® (3D simulation, whole structure).

**Step 1:**

Planar probe and microstrip matching were selected as simple as possible in the beginning. The probe was selected as a single stage probe with width, wp and length, lp. The microstrip matching section was selected as a single stage line with width, wp and length, lt (Figure 4.15).

The input (Port 1) is directly connected to the microstrip line with width, wp; thus, the port impedance $Z_{in}$ depends on wp. In 3D simulations, this input is fed by the impedance $Z_{in}$. This impedance is automatically calculated during each simulation in CST Microwave Studio® and the port reference is set to the calculated value.

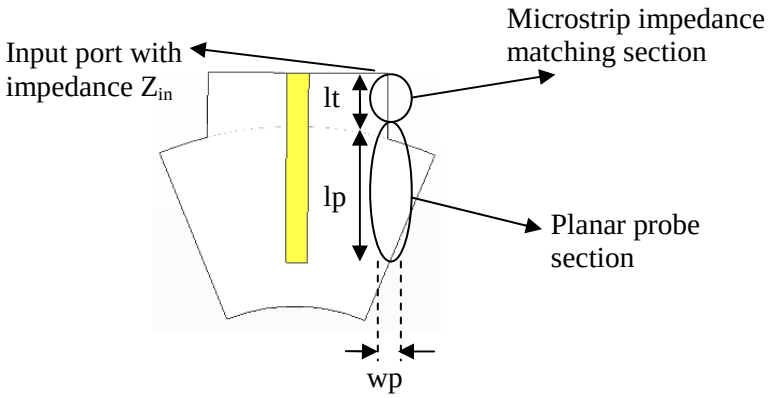



**Figure 4.15:** PC probe and microstrip matching sections

**Step 2:**

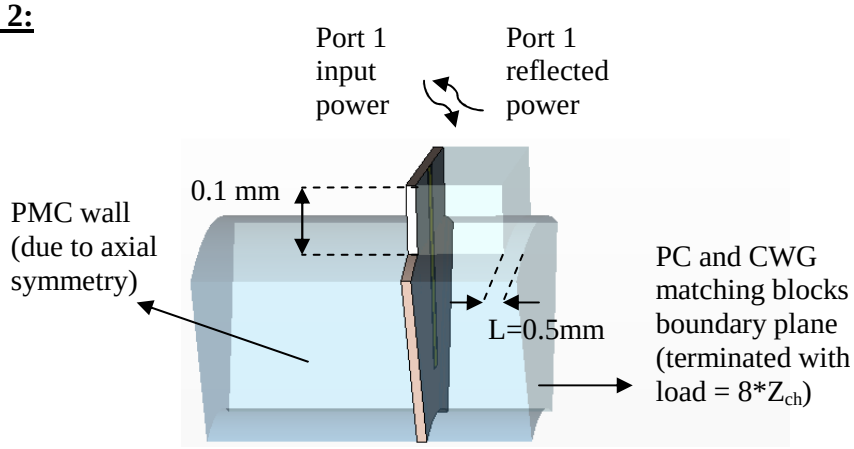



**Figure 4.16:** PC block view for optimization method

The simulation block, given in Figure 4.16 is similar to the one in the previous method. In this method, after the backside section, the first designed block is PC block. In this model, only 1/8 slice of the whole structure is simulated. The sides of this model are terminated with PMC boundary, due to electrical symmetry. The top and bottom surfaces are terminated with PEC boundary which corresponds to the metal in the structure. The oversized coaxial port is terminated by a load equal to $8*Z_{ch}$, where $Z_{ch}$ is the characteristic impedance of the oversized coaxial, such that the parallel of 8 slices result in $Z_{ch}$ (96.5 Ω).

In order to speed up the design process, sweeps of Sub-block 2 and Sub-block 1 are executed in different simulation tools; but they are still investigated together when selecting the dimensions.

Sub-block 2 is simulated in CST Microwave Studio® (3D simulation). Oversized waveguide length L is selected as 0.5 mm and the input port length is 0.1 mm in 3D simulations. Instead of 1/8 slice, ¼ slice of the structure is simulated in this method. The reason is the 3D simulation program (CST®) allows only Cartesian boundary condition assignment. This slice includes 2 input ports, 2 probes and ¼ of the output port. A load equal to $4*Z_{ch}$ (where $Z_{ch}$ is the characteristic impedance of oversized coaxial) connected to oversized waveguide boundary port instead of $8*Z_{ch}$. By these configurations, wp and lp are swept.

The sweep results of 3D software are extracted as S-parameter blocks and imported to AWR Microwave Office® (linear simulation). The schematic in this software is shown in Figure 4.17. This extraction has two functions: sweep for Sub-block 1 is done here more quickly, and sub-blocks of PC block are integrated in this tool.

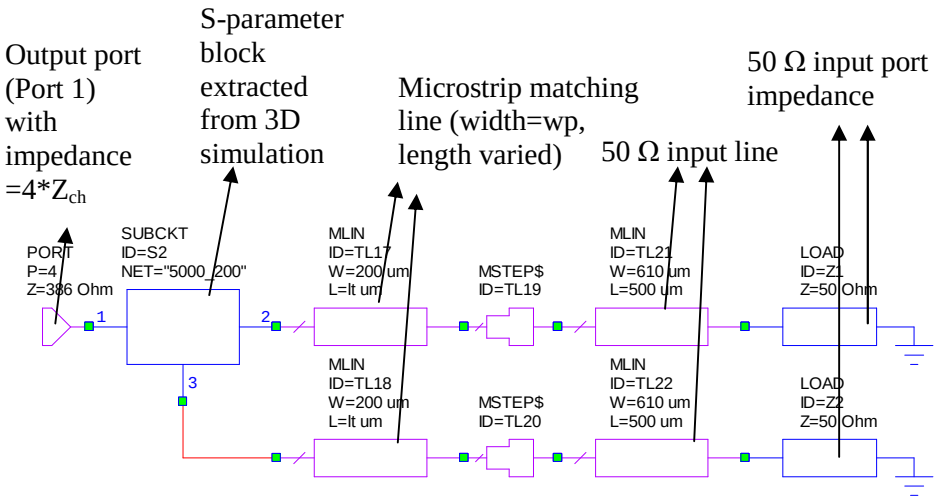



**Figure 4.17:** Linear simulation schematic for PC block in optimization method

In linear simulation, the microstrip matching line length except 0.1 mm length portion is swept. The $S_{11}$ traces with respect to frequency are observed on Smith chart with reference to $4*Z_{ch}$. The probe width (with respective probe and microstrip lengths) which makes the frequency impedance curve points closest to each other is selected. lp and lt are determined according to wp. This will lead to a wideband response. The place of this curve on Smith Chart does not need to be exactly in the center (Figure 4.18).

In this step, the parameters wp, lp and lt are swept as combinations and the best combination is selected. The two types of simulations do not belong to different steps. CST Microwave Studio® is used because probe part must be simulated in 3D tools. AWR Microwave Office® is only used to speed up the sweeps of microstrip part, which can be modeled linearly. When the best combination is found, the PC block design is completed.

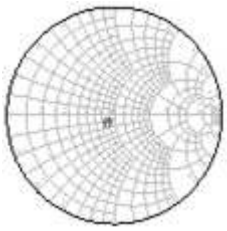


**Figure 4.18:** Impedance of optimized PC block for X-band seen from input

**Step 3:**

The tapered CWG matching block is designed in 3D simulation software as seen in Figure 4.19. The model is ¼ slice of the whole combiner. Previous blocks cannot be changed by terminations to be used in CWG matching block design. Whole structure must be simulated in order to consider all field distributions. The two inputs are terminated by 50 Ω. Structure is fed by the output (Port 1) with impedance being $4*Z_{ch}$.

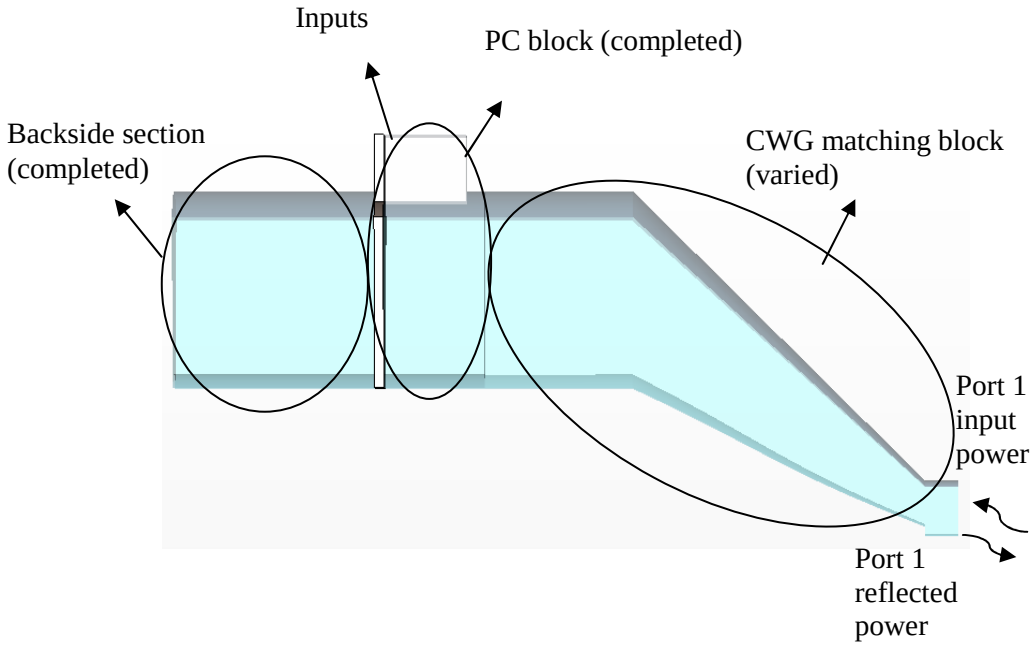



**Figure 4.19:** CWG matching block design view

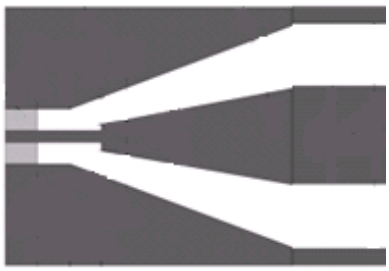
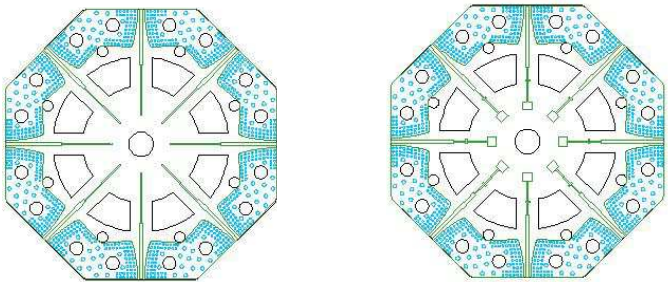


**Figure 4.20:** A sample structure of CWG matching block

In order to design the CWG matching block, a suitable structure is picked at first (Figure 4.20). For example, two linear tapers are placed with two step discontinuities between them. As initial values, lengths of the tapers are set to 0.5 mm. Then, the lengths are increased and the radii of step discontinuities are swept while monitoring $S_{11}$. The process is guided by observing the effect of each increment. The aim of the process is to bring $S_{11}$ trace to the center on Smith chart. The shortest possible lengths reaching this goal are selected, which completes the CWG matching block design.

The combiner design has also been completed at the same time with the CWG matching part design, unless a further optimization of probes are needed.

**Step 4:**



(a) (b)

**Figure 4.21:** 1-stage and 2-stage designed board versions for the same case

As stated at the beginning of the optimization method, the planar part is selected as single-stage lines in order not to increase the number of optimization parameters. However, this may be the cause of thin probes which have the risk of spark occurrence in high power case. This situation can be prevented by designing the probe in two steps: a narrow step at the input part and a wide step at the tip part. If needed, after mechanical dimensions are fixed, this second optimization is considered to have 2-stage probe. Microstrip matching section (Sub-block 1 of PC block) is also optimized. 1-stage and 2-stage version probe boards of one combiner are shown in Figure 4.21 (a) and (b), respectively.

In this thesis, the best combiner performance was achieved by the optimization method. This method has the possibility of selecting shorter dimensions; thus, the insertion loss of the combiner is decreased due to this fact. With respect to sub-block method, 2 cm decrease in longitudinal size and nearly 0.15 dB decrease in insertion loss per branch are achieved. Optimization method allows stretching the limits of the dimensions presented by the sub-block (systematic) method.

Power amplifier modules are built using the combiners designed by this method. In these combiners, a further optimization is applied to probe as explained above to obtain a higher power device.

# CHAPTER 5

# DESIGN AND REALIZATION OF PLANAR PROBE COAXIAL WAVEGUIDE COMBINER BY THE SUB-BLOCK METHOD

An 8 way planar probe CWG power combiner is designed by a systematic method which divides the whole structure in several sub blocks to have flexibility by certain design rules. In this chapter, details of the design procedure will be given for all sub-blocks.

## 5.1 Backside Block Design

The first step is to determine the inner and the outer radii of oversized CWG. Difference between the two radii and the 1/8 portion of outer perimeter are both equal to ¼ of the wavelength at center frequency (Figure 5.1). The distance from the back metal and the probe board is also fixed to ¼ of wavelength at center frequency.

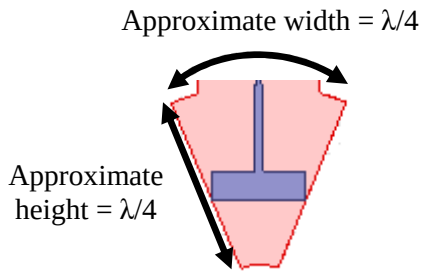



**Figure 5.1:** One probe portion of the oversized CWG for sub-block method

## 5.2 Power Combining Block Design

As the first step, substrate material is selected as Rogers RO5880 for the probe board. One of the reasons for selecting this material was the low $\varepsilon_r$=2.2. An $\varepsilon_r$ value close to 1 will be compatible to the air-filled CWG. Thus the probe board will not introduce much disturbance to field flow in CWG. Moreover, the low $\varepsilon_r$ will provide wide microstrip lines; reducing copper loss and heating caused by it. Another reason was the good copper peel strength; which will increase stability of the copper pattern on RO5880.

Before beginning probe impedance simulations, the window dimensions at the point where each probe is hung into the oversized coaxial, which can be seen in Figure 5.2, should also be determined. This window is not normally a part of coaxial medium and has a risk of coupling undesired modes. Keeping the window dimensions small compared to wavelength will prevent coupling.

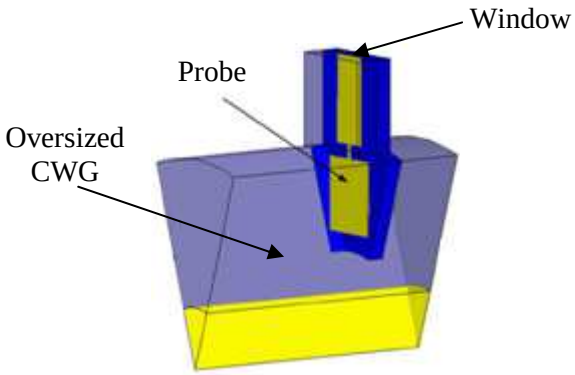



**Figure 5.2:** Rectangular window through which one probe is inserted

In Figure 5.3, the dimensions of this window are named as h is the height and W0 is the width. h is selected as 5 times the substrate height and W0 is selected as 5 times the line width; in order to include microstrip mode fields in the port. The substrate is 0.254 mm thick RO5880 with $\varepsilon_r$=2.2, resulting a 50 Ω line width of 0.77 mm. Thus, for all designs, h is selected as 1.27 mm and W0 is selected more than 3.85 mm.

The window should be wide enough so microstrip matching section can fit. For Ku-band, W0=3.85 mm is found appropriate. For X-band, W0 is scaled considering possible stub lengths will be more than Ku-band case. The scale factor is the 1.65, which is the ratio of center frequency wavelengths for the two bands.

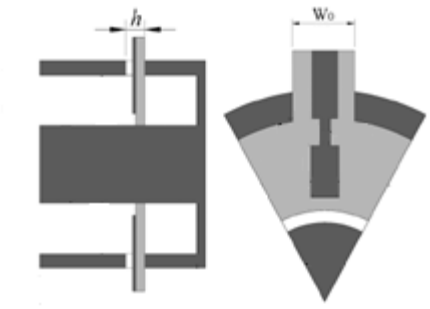



**Figure 5.3:** Backside section dimension parameters for sub-block method

After these initial selections, 3D model for PC block can be constructed. In PC block, Sub-block 2 is designed first since it is the most critical section.

### 5.2.1 Sub-block 2 design

Sub-block 2 is the section which includes the radiating probes. The enclosure of the probes requires numerical techniques for field calculation. Instead of complex calculations, accurate 3D simulation tools of HFSS® are used.

In 3D simulations, probe dimension parameters are swept and probes with the best performance are selected. In Figure 5.4, probe parameters are shown and named. The probes are designed in two stages with different widths for more flexible design.

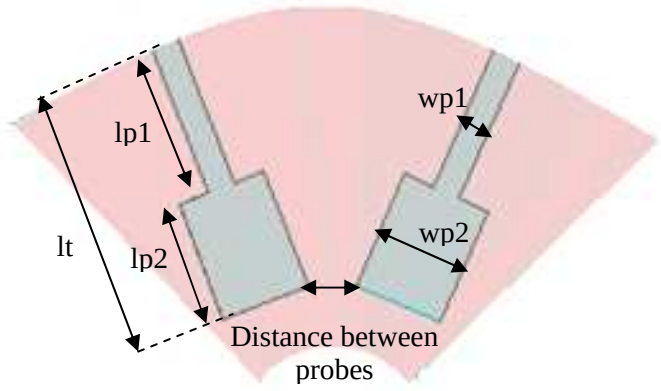



**Figure 5.4:** Dimension parameters of probes

Before the trials, limits are determined for these parameters. These limits are selected in order to minimize spark risk at the tip of probes or between probes.

Tips of the probes are open circuited; thus the highest voltages on probes are expected at the tips. This may cause high electric field between tips and CWG center conductor; thus sparks. The exact estimation of spark risk using simulation is not possible. Instead, in order to minimize this risk, wp2 was maximized and lt was minimized. Maximized wp2 will minimize voltage per length at probe tips. Using this aspect, the wide stage of the 2-stage probe is placed at the tip and the narrow stage is connected to microstrip input. Minimized lt will increase the distance between probe tip and CWG center conductor; thus decrease the electric field between them.

Sparks can also occur between two adjacent probes. Although the desired operation is even mode, there will be differences between input signals in reality. Thus difference voltages will appear at adjacent probe edges, which will create nonzero E-field and sparks. In order to minimize this risk, distance between probes (Figure 5.4) should be maximized. However, exact estimation of this risk is not possible. Instead, several values are selected to be used in simulation sweeps, which are listed in Table 5.1.

**Table 5-1:** Selected values for distance between probes

| **Frequency band (GHz)** | 8.5 –11.5 | 8.5 –11.5 | 15.5 – 17.5 | 15.5 – 17.5 |
|---|---|---|---|---|
| **Distance between probes (mm)** | 1 | 1,4 | 0,8 | 1 |

After these selections, lt is swept in HFSS®. For each lt, wp2 is calculated from the distance between probes. In order to balance the low impedance due to wp2, wp1 is selected very narrow. Two options are determined for wp1 as 0.3 mm and 0.6 mm. Thus, for each band; for each lt-wp2-wp1 combination, a separate 3D model is prepared. For each model, a parameter sweep for lp1 is made; since it is the only parameter left for the probe.

Before starting simulations in HFSS®, meshing reliability is important, since fields in the structure cannot be well-defined. For efficient meshing, each sub area is meshed with a different local mesh size. Moreover, adaptive meshing cycles are applied to the whole structure. A denser meshing will provide more accurate results, however the needed computer memory will increase thus the simulation will be slower. Instead of a very dense meshing, acceptable mesh sizes are selected for faster simulation (Figure 5.5). Only sub-block 2 is densely meshed (especially the narrow probe stage) because it is the most critical and undefined part of the structure.

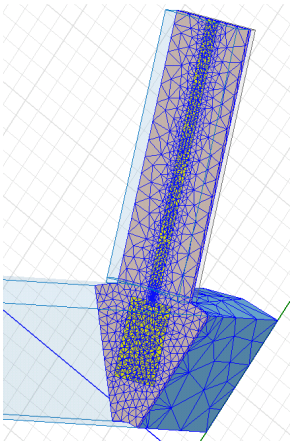


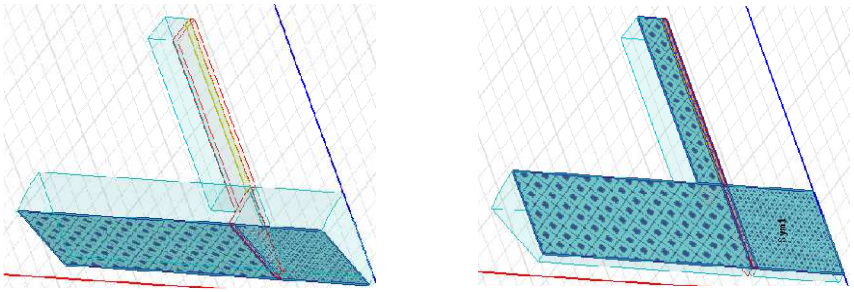
**Figure 5.5:** Meshing view for the PC block

In order to check the reliability of meshing, trials are made for each mesh size. For each sub area, mesh size is compared with an overly meshed case (very dense meshing). The two cases gave exactly the same result according to impedance curves on Smith Chart; thus simulation proceeded with the selected meshing.

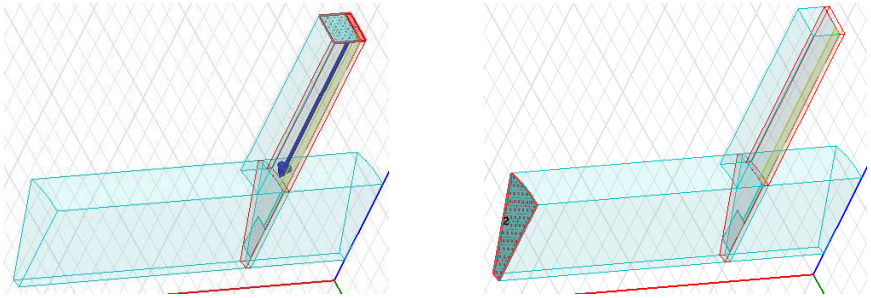
After mesh determination, boundary conditions (BC) are determined for simulation model. For simulation, 1/16 slice of the PC block is used (Figure 5.6). This slice is one probe portion (1/8 slice) divided by two from the symmetry axis of the probe. This is the smallest possible portion of PC block; thus with appropriate BCs, this will give the smallest solution matrix and result in fastest simulation.

The selected BCs are shown in Figure 5.6 (a) and (b). At the surface that separates the probe from the adjacent probe (Figure 5.6 (a)), perfect magnetic conductor (PMC) BC is used; since tangential H field is 0 due to axial symmetry. At the symmetry plane of probe (Figure 5.6 (b)), magnetic symmetry BC is selected, since the probe is electrically symmetric around its longitudinal axis.

There are 2 ports in the model in Figure 5.6; microstrip input side is Port 1 (c) and oversized CWG side is Port 2 (d). Port 2 is terminated with the automatically calculated impedance; which is the oversized CWG characteristic impedance ($Z_{ch}$) multiplied by 16. This means CWG side is assumed perfectly matched. Reflection coefficients at Port 1 are observed on Smith Chart, taking the automatically calculated port line impedance (impedance of half microstrip) as reference impedance. The line from probe to Port 1 is 50 Ω microstrip.

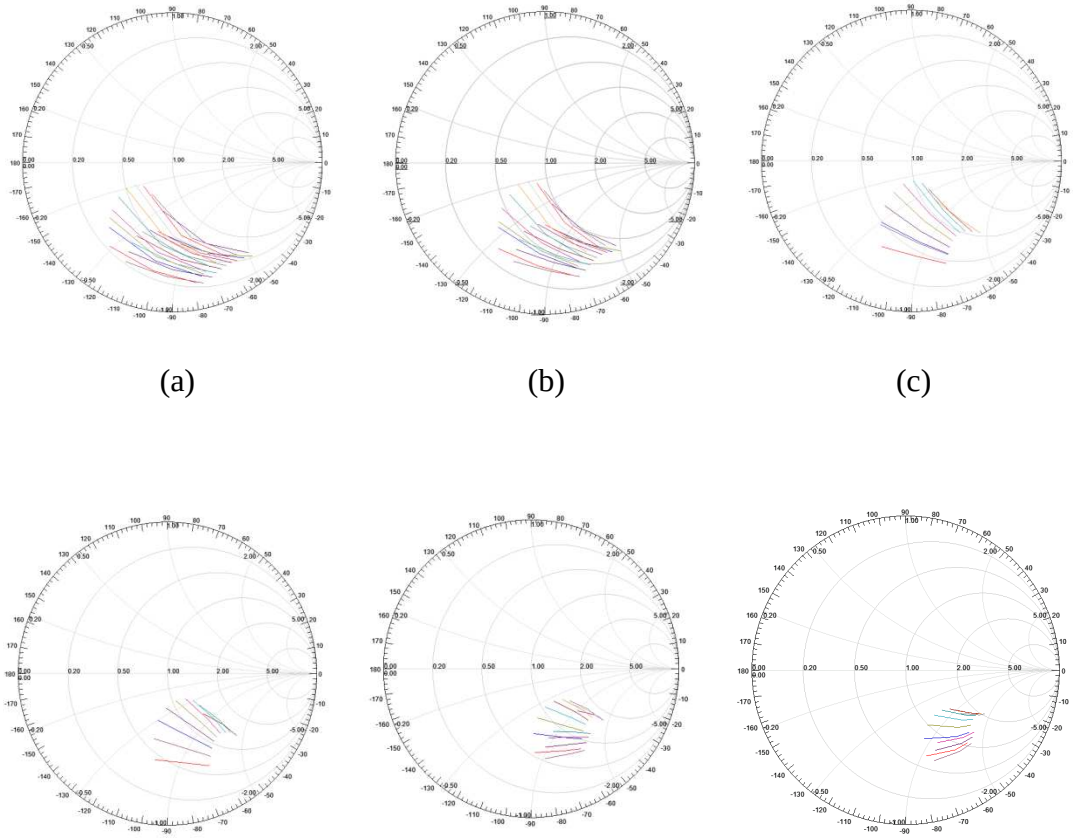


(a) (b)



(c) (d)

**Figure 5.6:** Boundary conditions for 3D PC block simulation



(a) (b) (c)

(d) (e) (f)

**Figure 5.7:** Sweep results for lt values

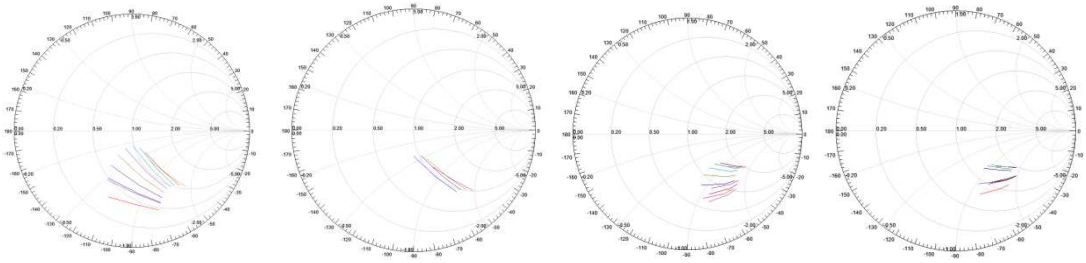
The parameters are investigated one at a time. At each step, all the parameters other than the one being investigated are fixed. For each value of the parameter which is investigated, all possible combinations of other parameters are simulated. Using these cumulative graphs, best value for the investigated parameter is selected. For each parameter, two possible values are selected.

The first sweeping is made for lt. In Figure 5.7, X-band sweep results for different lt values are given; graphs (a) to (f) correspond to lt=3.5 to 6 mm with 0.5 mm steps. For each lt, all other parameters are swept; resulting in a cumulative of possible impedances which can be reached with that lt value. As lt increases, the curves become less frequency dependent (more wideband) and closer to chart center. Thus, high lt is better for matching, while low lt is better for reducing spark risk. For lt in X-band, 4.5 mm and 6 mm are selected to be used as alternatives in parameter combinations.

**Table 5-2:** Selected lt values and lt-wp1 combinations

| | **(a)** | **(b)** | **(c)** | **(d)** |
|---|---|---|---|---|
| **lt (mm)** | 4,5 | 4,5 | 6 | 6 |
| **wp1 (mm)** | 0,3 | 0,6 | 0,3 | 0,6 |

After selecting lt values, wp1 is swept. The sweep parameter combinations are given in Table 5-2 and respective sweep results are given in Figure 5.8. For lower wp1, better and more wideband matching is achieved. However, low wp1 will increase heating for copper probes. In this case, for a high lt value (high spark risk but better matching) a low wp1 value can be selected (worse matching but less heating) for balancing the advantages. From Table 4-2, (a) and (d) are selected to be used in further sweeps.



(a) (b) (c) (d)

**Figure 5.8:** Results for wp1 sweep for combinations in Table 5-2

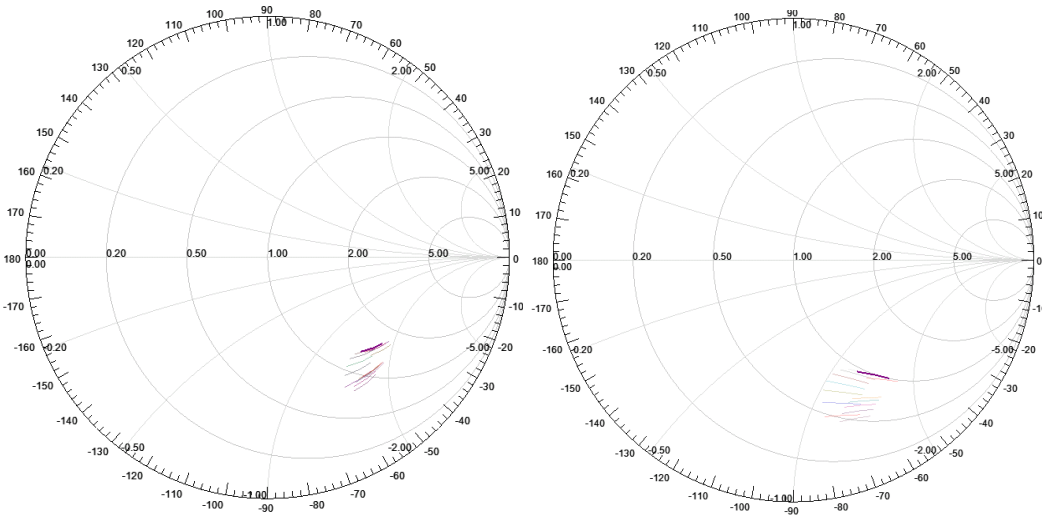
At the next step, wp2 values are selected. These are calculated from the lt values in Table 5-2 and distance between probes in Table 5-1. For each frequency band, 4 combinations of wp1-wp2 and lt are obtained, as listed in Table 5-3.

**Table 5-3:** Selected wp2 values for lt-wp1 combinations

| | **8.5 – 11.5 GHz** | | | | **15.5 – 17.5 GHz** | | | |
|---|---|---|---|---|---|---|---|---|
| | (a) | (b) | (c) | (d) | (e) | (f) | (g) | (h) |
| **wp1 (mm)** | 0,6 | 0,3 | 0,6 | 0,3 | 0,6 | 0,3 | 0,6 | 0,3 |
| **wp2 (mm)** | 1,86 | 3,1 | 0,99 | 2,23 | 0,94 | 1,69 | 0,73 | 1,47 |
| **lt (mm)** | 6 | 4,5 | 6 | 4,5 | 3,6 | 2,7 | 3,6 | 2,7 |

After the combinations in Table 5-3 are determined, lp1 is swept for each combination. For low and high limits of lp1, probe impedance is far from center and more dependent on frequency. At a certain value between upper and lower lp1 limits, the impedance is least dependent on frequency and the probe impedance gets closest to the center. This means the probe will provide better and more wideband matching.

In Figure 5.9 (a) and (b), lp1 sweep results are given for parameter combinations (e) and (h) from Table 5-3, respectively. For each graph, lp1=2.1 is selected since it gives the best matching (the bold curve nearest to the center).



(a) (b)

**Figure 5.9:** Results for lp1 sweep for combinations (e) and (h)

For both bands and parameter combinations; an lp1 value is selected using this approach. The final parameter combinations for both bands are given in Table 5-4, where the values are in millimeters. The probe impedance curves with respect to frequency for each selected parameter combination are given in Figure 5.10. As observed, better matching is obtained in 15.5-17.5 GHz band ((e), (f), (g), (h)) because the operating bandwidth (%12) is narrower than the other band, 8.5-11.5 GHz (%30).

**Table 5-4:** Determined probe dimensions for the sub-block method

| | **8.5 – 11.5 GHz** | | | | **15.5 – 17.5 GHz** | | | |
|---|---|---|---|---|---|---|---|---|
| | **(a)** | **(b)** | **(c)** | **(d)** | **(e)** | **(f)** | **(g)** | **(h)** |
| **wp1 (mm)** | 0,6 | 0,3 | 0,6 | 0,3 | 0,6 | 0,3 | 0,6 | 0,3 |
| **lp1 (mm)** | 3,5 | 3,5 | 3,5 | 3,5 | 2,1 | 2,1 | 2,1 | 2,1 |
| **wp2 (mm)** | 1,86 | 3,1 | 0,99 | 2,23 | 0,94 | 1,69 | 0,73 | 1,47 |
| **lt (mm)** | 6 | 4,5 | 6 | 4,5 | 3,6 | 2,7 | 3,6 | 2,7 |

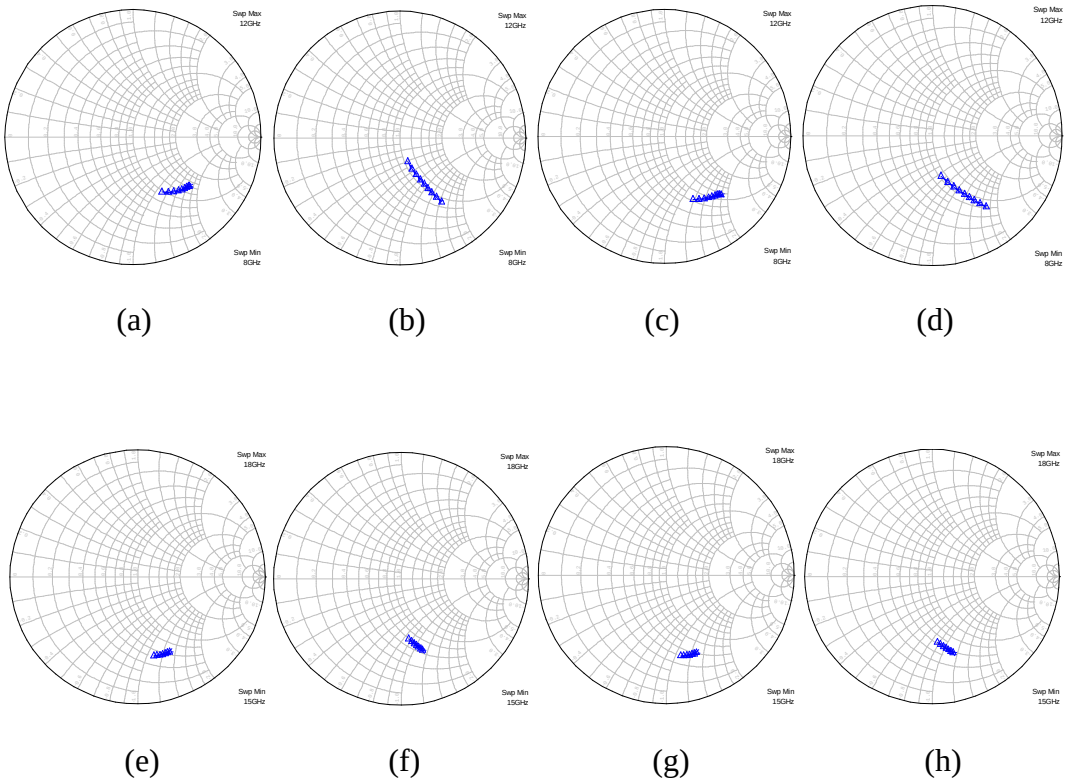



**Figure 5.10:** Selected probe impedance graphs for the sub-block method

### 5.2.2 Sub-block 1 design

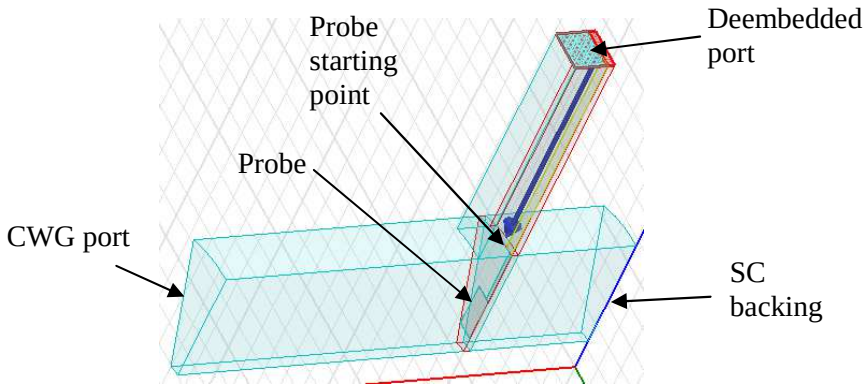



**Figure 5.11:** 3D simulation view for 1/16 slice of sub-block 2

For each parameter combination in Table 5-4 for Sub-block 2, there is a simulated 3D model in HFSS® (Figure 5.11). The simulation blocks are extracted as S-parameter blocks to AWR Microwave Office®, where Sub-block 1 will be designed. However, since 3D model includes half of the transmission lines, the extracted blocks are connected in parallel in AWR Microwave Office®, in order to obtain full transmission line at the microstrip port.

In 3D simulations, microstrip port is deembedded as in Figure 5.11. Thus, impedance seen at the deembedded port is the impedance seen from the probe starting point.

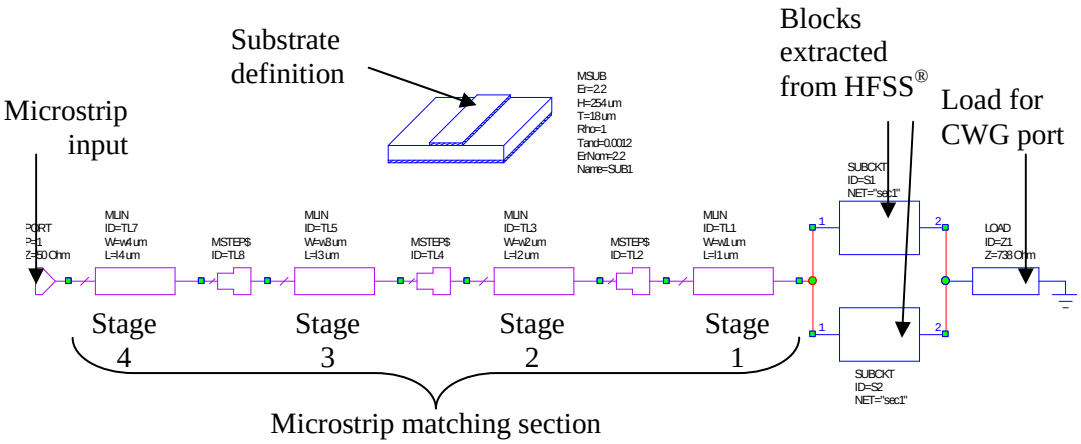



**Figure 5.12:** Schematic of microstrip matching for sub-block method

In Figure 5.12, one of the schematics in AWR Microwave Office® is given. There are four stages in the microstrip matching section. The layout of these sections is given in Figure 5.13 and their effects to input impedance on Smith chart are given in Figure 5.14. The design is for the probe combination (a) from Table 4-4; however the others are done in the same logic.

The places of stages in the layout are from 1 to 5 starts from the probe to the 50 Ω input. In Figure 5.14, impedances seen from transition points are given. (a) is the impedance seen from the start of stage 1. (b) to (e) are impedances seen from the end of stages 1 to 4, respectively. The matching stages act similar to lumped elements, from short length approximation approach (SLA).

The probe impedance is shown in Figure 5.14 (a). As all probe combinations, the impedance is in the capacitive half of Smith chart. The first matching line, stage 1 is a narrow line, which acts like an inductor from SLA. This stage brings the

impedances towards the upper (inductive) half of Smith chart (b). The center frequency is on real axis, high frequency points are on inductive side and low frequency points are in capacitive side. The reason is, for high frequency points stage 1 is electrically longer and inductance with respect to SLA is more.

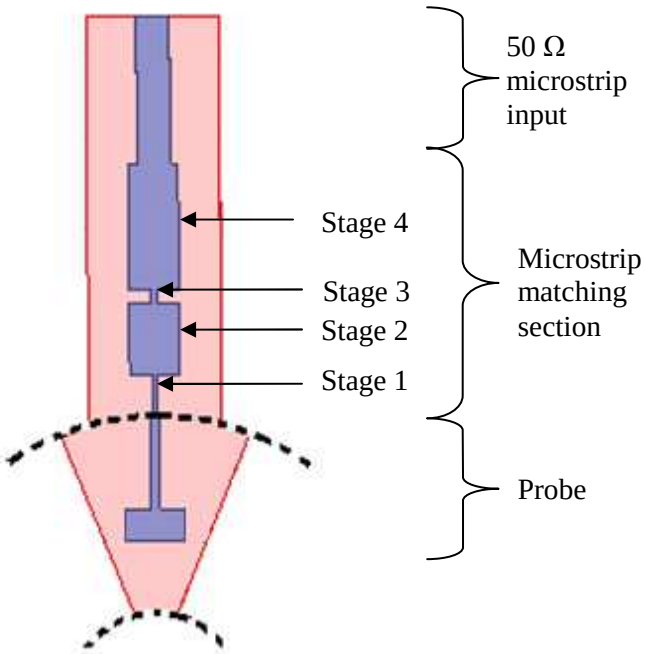
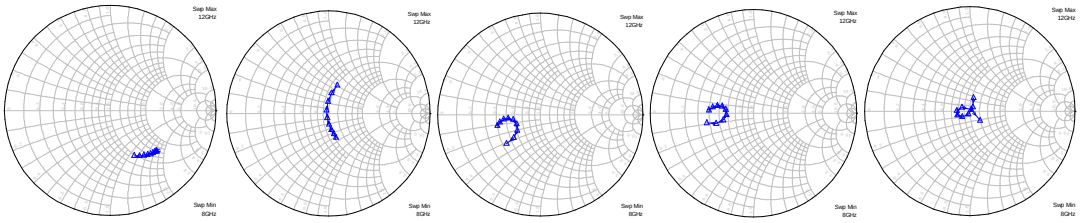



**Figure 5.13:** Microstrip matching stage layout for sub-block method

Stage 2 is a line segment wider than 50 Ω lines; thus acts as a capacitance form SLA. This stage brings impedance in (b) back to capacitive side. Similar to stage 1, the capacitance effect will be stronger for high frequency points. This will bring a curvature to impedance line, bringing the frequency points closer, as in (c).

Stage 3 is a narrow line with inductive effect. This section brings the impedance curve center to real axis (d). The impedances of different frequencies are close to each other, which means wideband response. The points are all close to the center of the curve on real axis. The center corresponds to a real impedance value; it can be assumed that all frequencies are brought to that impedance. In stage 4, there is a QWL transformer to bring this real impedance to 50 Ω. The final shape of the impedance curve is seen in (e).



(a) (b) (c) (d) (e)

**Figure 5.14:** Microstrip matching stage impedance graphs for sub-block method

Design with this sub-block method has input connectors which can be easily connected to the board by squeezing the substrate between connector pin and ground. The inputs are required to be in coplanar line type to use these types of connectors. Thus, a coplanar to microstrip transition on RO5880 substrate is designed. The layout and simulated input return loss (better than -20 dB) of this transition is given in Figure 5.15 and Figure 5.16, respectively.

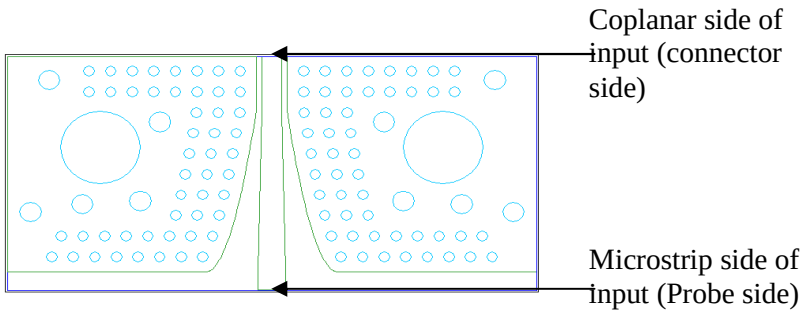



**Figure 5.15:** Layout of coplanar line transition for sub-block method

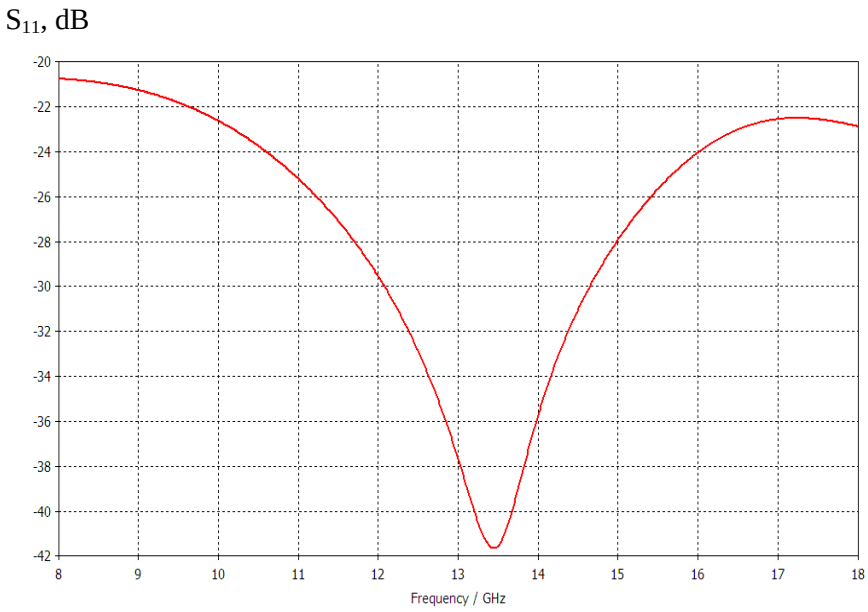



**Figure 5.16:** Simulation result of coplanar line transition for sub-block method

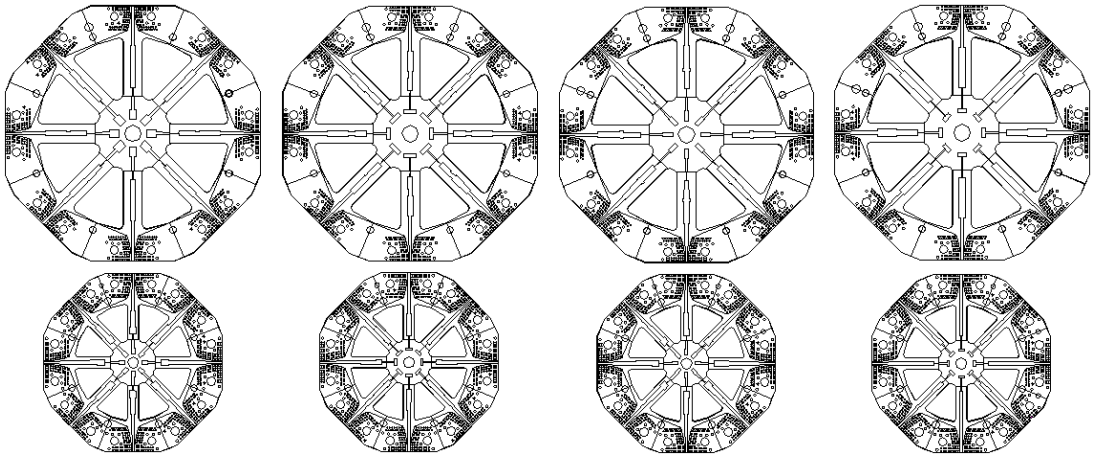


**Figure 5.17:** Final board layouts for sub-block method

The substrate boards that carry the probes and the microstrip matching circuits are integrated with the coplanar-microstrip transition and a single board is produced for each probe configuration. The final layouts of these boards are seen in Figure 5.17, where the top four boards are for 8.5 – 11.5 GHz band and the bottom four boards with smaller radii are for 15.5 – 17.5 GHz.

### 5.2.3 Sub-block 3 design

Sub-block 3 is a uniform oversized CWG segment with length L (Figure 5.18). This length is adjusted to have pure TEM mode at the end of the distance L from the probe board. Thus, a load equal to $Z_{ch}$ (characteristic impedance of CWG) can be placed with no difference in $S_{11}$ (reflection from Port 1 in Figure 4.39). Ideally, for $L=\lambda$ this can be obtained. However, a shorter L may provide the same effect and this value is set by trials.

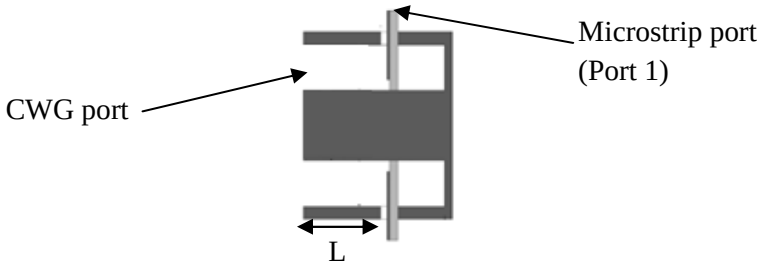
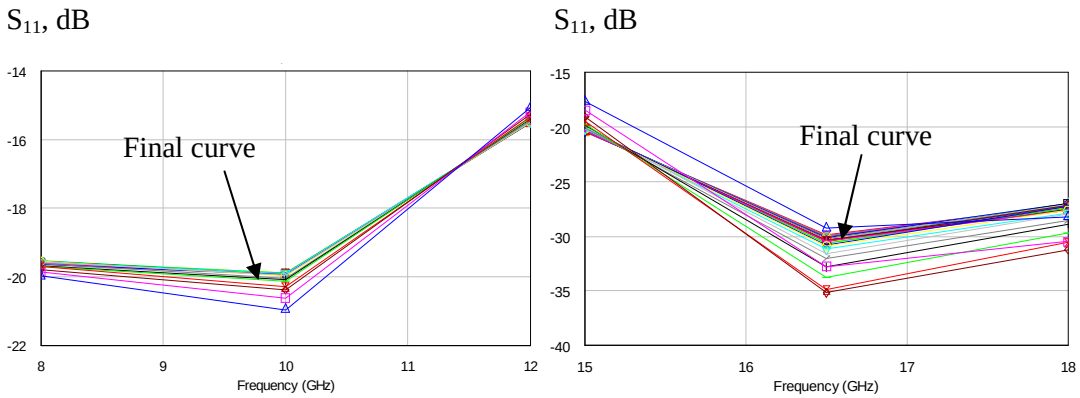



**Figure 5.18:** Distance of oversized coaxial part

In the simulations for finding L, the parameter was swept. For 8.5 – 11.5 GHz band, L is swept from 0.5 mm to 15 mm with 0.5 mm steps and $S_{11}$ values for 8 GHz, 10 GHz and 12 GHz are plotted in Figure 5.19 (a). For 15.5 – 17.5 GHz band, L is swept from 1.8 mm to 18 mm with 0.3 mm steps and $S_{11}$ values for 15 GHz, 16.5 GHz and 18 GHz are plotted in Figure 5.19 (b).

For both bands, the L value at which the $S_{11}$ curve is converged to the final shape (for the highest value of L) is selected. The minimum L is found as 9 mm for X-band and 11 mm for Ku-band.




(a) (b)

**Figure 5.19:** Results for sweep of oversized coaxial length for sub-block method

Minimum L turned out to be higher for high frequency band. This can be explained from the similar behavior of the probes with monopole antennas. Thus, the distance that modes are settled for the probe (L) is expected to behave similar

with frequency to the distance that modes are settled for monopole antenna (Rayleigh distance).

### 5.3 Coaxial Waveguide Matching Block Design

After parameter L is determined, the Klopfenstein tapers are designed in both frequency bands. The Klopfenstein taper is a coaxial structure with curved inner and outer conductors. As the curvature changes, from the ratio of the radii, the characteristic impedance changes according to a special nonlinear function [24]. In the design in this thesis, the outer cylinder radius of the taper is determined to be linearly tapered. This will be the inner surface of the lid to be placed on top of probe array; the linear taper choice is due to the difficulty of processing an inner surface with a nonlinear function.

Then, according to the function of impedance through the taper, the respective inner radius values were calculated using the design approach in [25]. These formula based calculations are made with the help of MATLAB®. In this calculation, the function determines matching value while the length determines the lower cutoff frequency. In this design, -25 dB output return loss of taper section matching was obtained from 92 Ω (oversized CWG) to 50 Ω (output). The length of taper for 8.5 – 11.5 GHz band is calculated as 20 mm and the length for 15.5 – 17.5 GHz band as 12 mm. In order to prevent sudden impedance transitions, 2 mm straight CWG line segments are placed at both ends of the Klopfenstein taper (Figure 5.19 and Figure 5.20).

At the output end of the taper, before reaching the connector seal, a Teflon disk is placed. This disk supplies accurate alignment between the lid and the center conductor. The final shapes of the tapers in both bands are shown in Figure 5.19 and Figure 5.20.

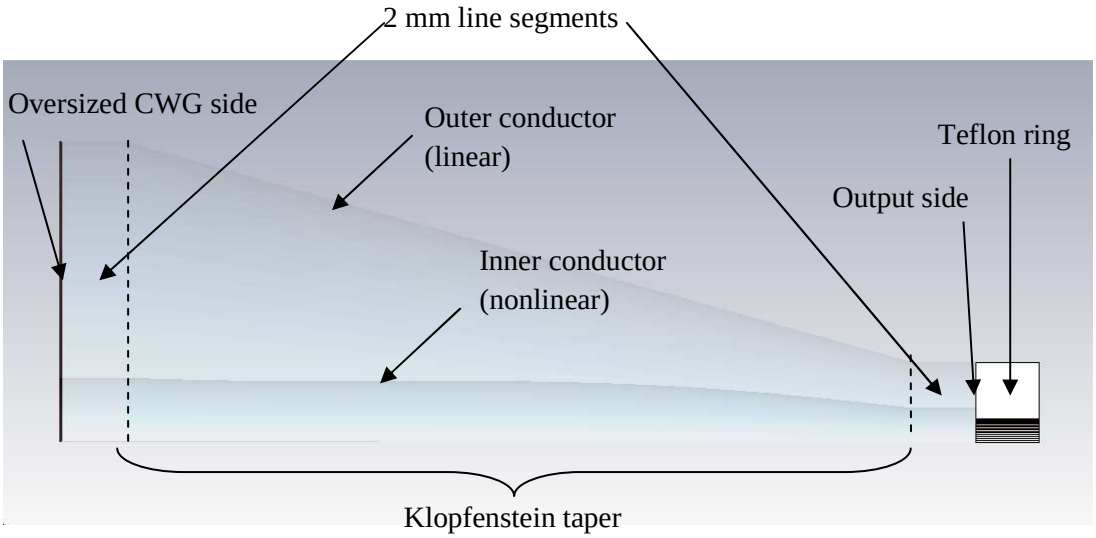



**Figure 5.19:** Final shape of taper for sub-block method in X-band

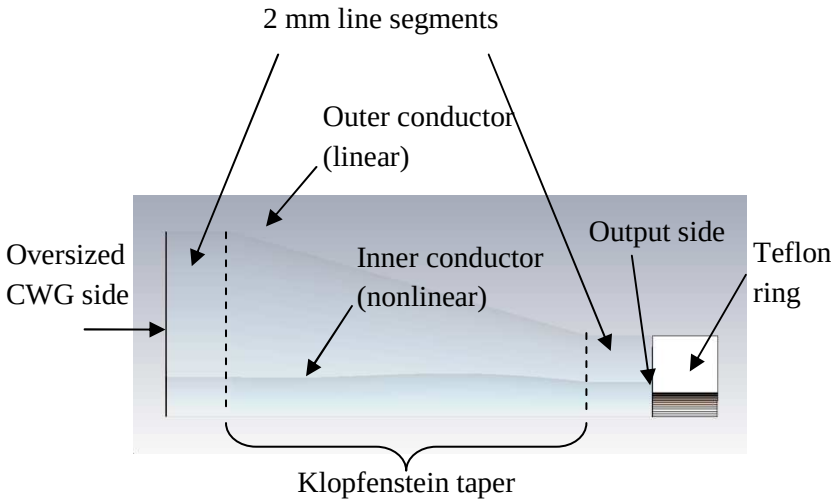



**Figure 5.20:** Final shape of taper for sub-block method in Ku-band

## 5.4 Completion

After all parameters of structures are determined, all parts of the path are simulated together once more in a 3D simulation program for all combinations in both frequency bands. The $S_{11}$ results for 8.5 – 11.5 GHz band are shown in Figure 5.21 and results for 15.5 – 17.5 GHz band are shown in Figure 5.22.

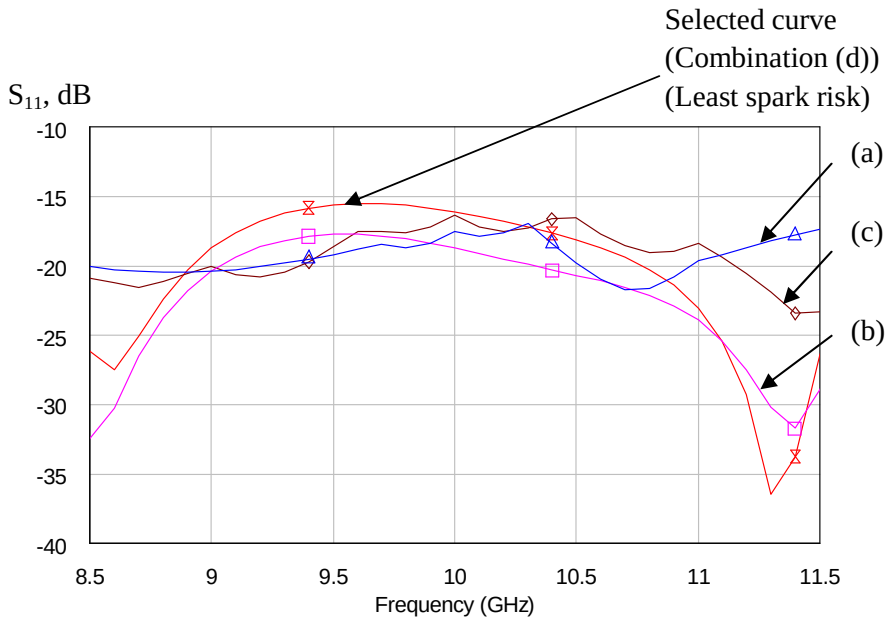



**Figure 5.21:** Simulation results at X-band for sub-block method

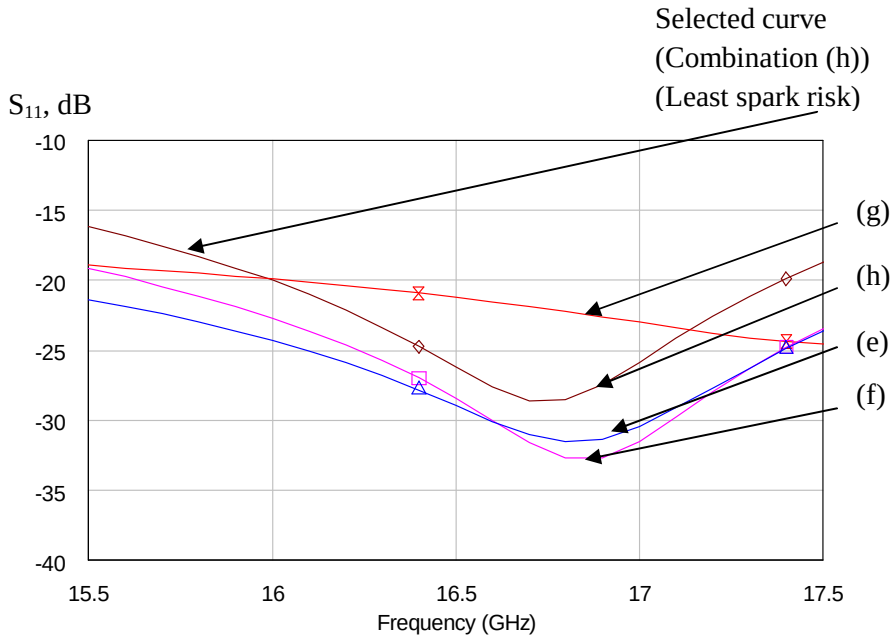



**Figure 5.22:** Simulation results at Ku-band for sub-block method

The graphs are for the 8 probe alternatives listed in Table 5-4. In Figure 5.21, curves are for combinations (a) to (d). In Figure 5.22, curves are for combinations (e) to (h). For both frequency bands, it can be seen that from (a) to (d) and (e) to (h), the achieved minimum output return loss value gets worse. On the other hand, risk of sparking decreases (between tip of the probe and coaxial center conductor or between two adjacent probes).

After production of all possibilities, design with the least spark risk is measured and sufficiently low return loss (better than 12 dB) was observed. Thus; for usage in modules, combination (d) is selected for X-band and combination (h) is selected for Ku-band.

## 5.5 Realizations of Combiners Designed by Sub-block Method

For the sub-block method, the combiners are produced with coaxial input and SMA output connectors. Probe array boards are produced for four different types of probes. The prototype views of version 4 designs for X-band and Ku-band are given in Figure 5.25 (a) and (b), respectively. The measurement results for these designs are given in Figure 5.23 for X-band and Figure 5.24 for Ku-band. For both bands, the responses are observed as close to the expected values and the ripple magnitudes are also within an acceptable range of 1 dB. The output reflection loss is better than -12 dB and the average insertion loss is less than 0.8 dB per branch. This loss includes the total connector loss at input and output which can be up to 0.4 dB which is not included in 3D simulation.

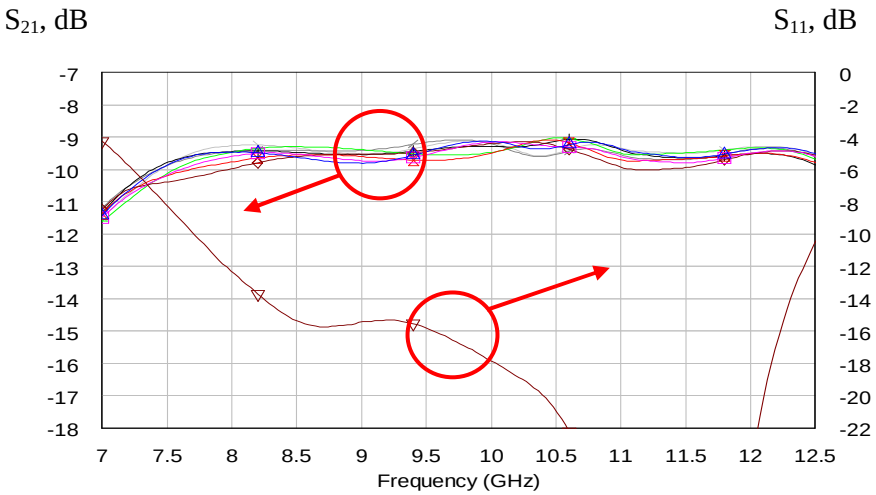



**Figure 5.23:** Measurement for X-band version 4 design in sub-block method

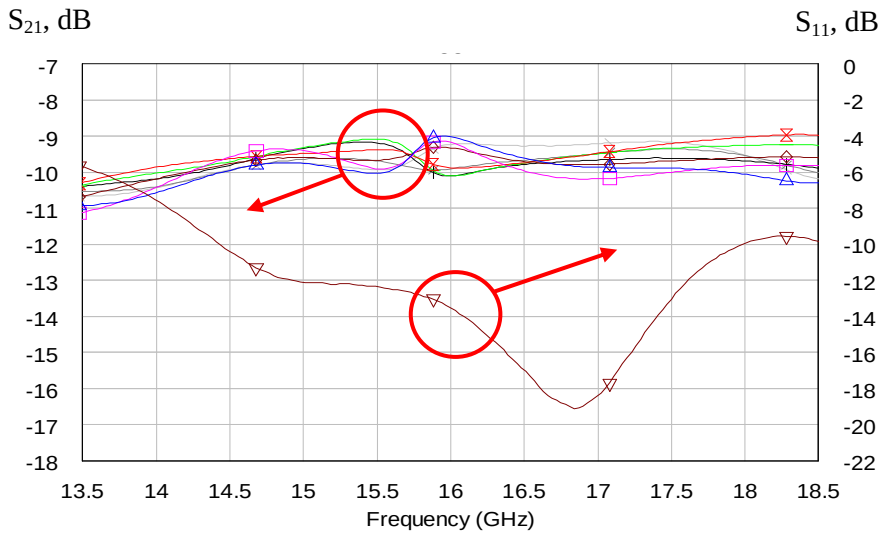



**Figure 5.24:** Measurement for Ku-band version 4 design in sub-block method

(a) (b)

**Figure 5.25:** Prototype combiner views for sub-block method version 4 designs

In the design, the most high-power handling, but the worst output return loss was expected for version 4 designs. However; after these designs are manufactured and measured, return loss was seen to be sufficiently low in the operation bands. In this case, the other versions do not have much advantage compared to the version 4. Assembly of other versions was not made. Version 4 design is used as the reference when comparing sub-block method with other methods. In the 15 W power amplifier module, optimization method designs which have slightly better performance were used.

# CHAPTER 6

# DESIGN AND REALIZATION OF PLANAR PROBE COAXIAL WAVEGUIDE COMBINER BY THE OPTIMIZATION METHOD

In sub-block method, each block was designed in a systematic and mostly theoretical way. In that method size of the combiners was not taken as a critical parameter. Each sub-block was selected sufficiently large to be on the safe side in satisfying the design goals. After finishing this design, ways of reducing combiner dimensions were investigated.

An optimization method is introduced for this purpose. In this method, design will be carried out as a flow starting from the inputs and leading to the output. At each step, one more block is added and the simulation includes all previous blocks. Due to use of optimization, matching line and CWG lengths can be minimized. This provides advantage both in terms of size and loss. In this chapter, design details of this method will be given.

## 6.1 Backside Block Design

Radii of oversized CWG are calculated from dimensions of one probe portion (Figure 6.1). In optimization method, these dimensions are selected equal to standard rectangular waveguide (RWG) dimensions which are used at the related frequency band. This is due to avoid the risk of breakdown or undesired modes. Since these designs will be the improved versions of the sub-block method designs, standard values are selected in order to be on the safe side. The selected waveguides

are WR-90 for 8.5 – 11.5 GHz and WR-62 for 15.5 – 17.5 GHz and the radii are calculated accordingly.

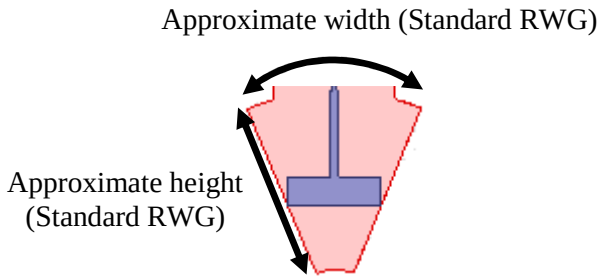



**Figure 6.1:** One probe portion of the oversized CWG for optimization method

However, according to port simulations in AWR Microwave Office®, the approximate widths are likely to generate higher order modes. In order to prevent this, inner radius is reduced to 2 mm for both bands. Outer radius is calculated from adding the standard RWG height to 2 mm.

## 6.2 Power Combining Block Design

At the beginning, window dimensions through which probes are inserted into CWG (Figure 6.2) should be selected. The dimensions are selected through 3D simulations in CST Microwave Studio® by observing higher order mode excitations.

The width of this window is selected as 4 mm and the height is selected as 2.25 mm for both bands.

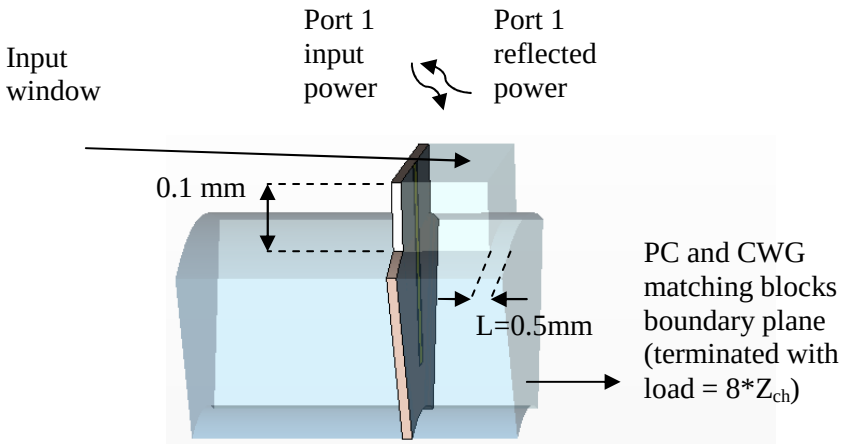



**Figure 6.2:** PC block simulation view for optimization method

The substrate is selected as 0.254 mm thick RO3003 with rolled copper (RD) cladding. Copper-dielectric interface is much smoother compared to more commonly used electrodeposited (ED) cladding. This property decreases the path length where the current flows; thus conductor loss is reduced. RO3003 has a dielectric constant of 3.3, which will not disturb the field flow in CWG much. It also has an advantage compared to the sub-block method design, due to its relatively high dielectric constant will provide shorter lines in the microstrip matching and coplanar transition sections; leading to smaller combiner dimensions.

With these materials and terminations, the length and width combinations of probes are simulated. The parameters for probe and microstrip matching are shown in Figure 6.3. In CST Microwave Studio®, wp and lp are swept while lt=0.5 mm.

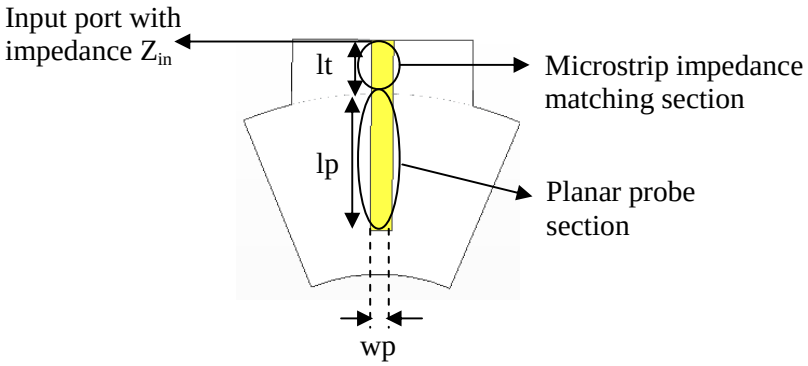



**Figure 6.3:** PC probe and microstrip matching section parameters for optimization method

After these simulations, the results are extracted from CST Microwave Studio® transferred to AWR Microwave Office®. In Figure 6.4, the schematic is seen for ¼ slice of the combiner. The oversized coaxial port is named Port 1 and connected to a port with impedance equal to $4*Z_{ch}$ (where $Z_{ch}$ is the characteristic impedance of oversized CWG). Microstrip ports of extracted blocks are connected to microstrip matching lines with width wp and adjustable length.

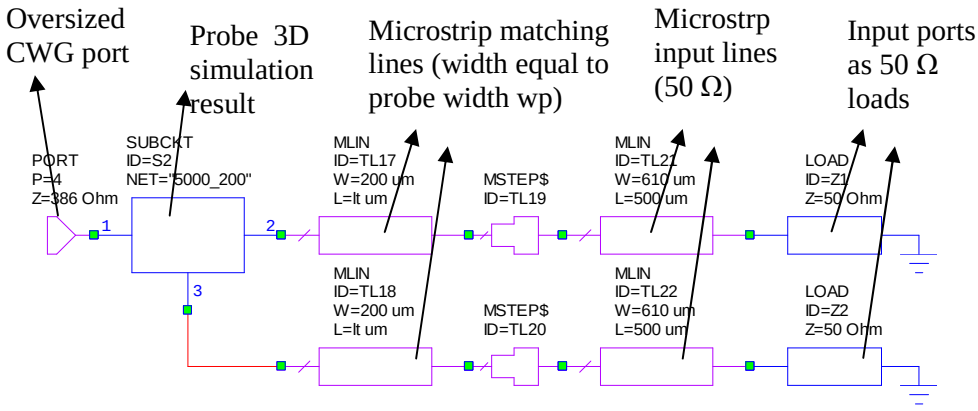



**Figure 6.4:** Example schematic for microstrip matching simulation for optimization method

In AWR Microwave Office®, for each wp-lp combination, the extracted S-parameter block is placed, width of the matching line is set to wp and length of the matching line is tuned. The goal is to obtain the most wideband impedance response, i.e. to bring impedance curve points closest to each other.

For 15.5 – 17.5 GHz band, several probe combinations and obtained impedance curves with optimized microstrip matching lines are shown in Figure 6.5 (a) to (l). (a) to (c) are for wp=0.2 mm and lp=5-6-7 mm; (d) to (f) are for wp=0.4 mm and lp=5-6-7 mm; (g) to (i) are for wp=0.61 mm and lp=5-6-7 mm and (j) to (l) are for wp=1 mm and lp=5-6-7 mm, respectively.

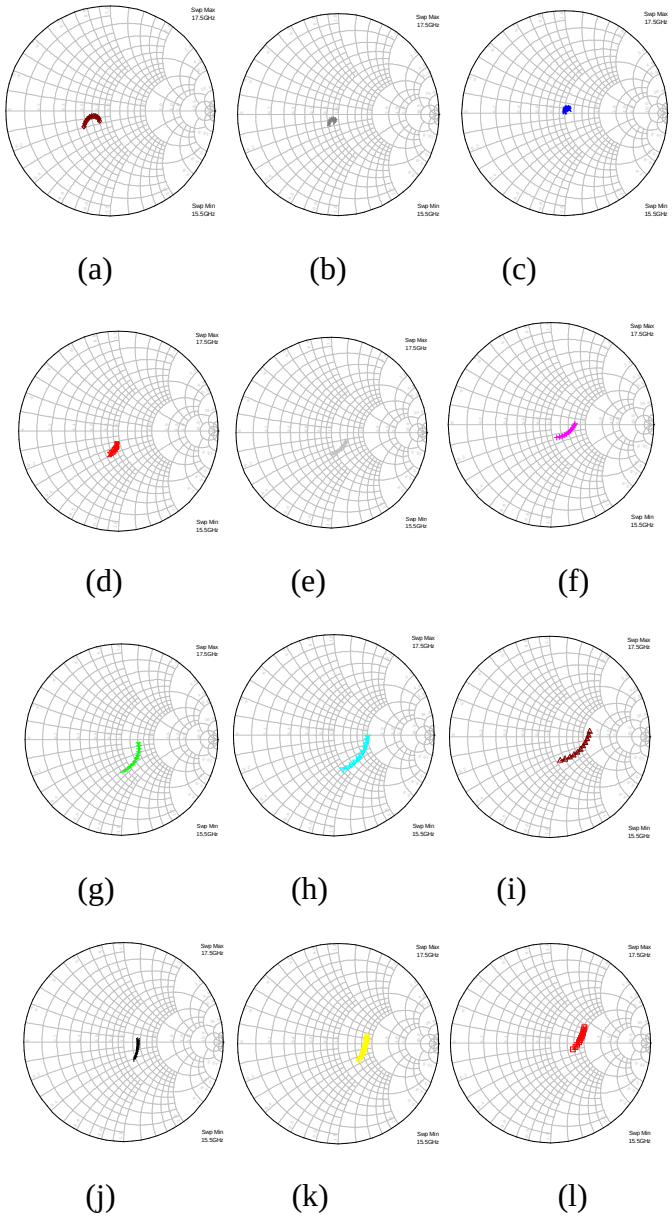



**Figure 6.5:** PC block simulation results for optimization method

In the simulations, as seen in Figure 6.5, decrease of wp and increase of lp resulted in more wideband response. wp is selected as 0.2 mm for both bands while lp is selected as 9.34 mm for 8.5 – 11.5 GHz and 4.8 mm for 15.5 – 17.5 GHz.

### 6.3 Coaxial Waveguide Matching Block Design

For selected PC blocks of each band, a CWG matching structure is modeled. This structure is composed of linear tapers and step discontinuities, as seen in Figure 6.6. The matching taper is connected to the cross section starting 0.5 mm away from the input window, which is the boundary plane between PC block and CWG matching block (Figure 6.2). Thus, the coaxial taper circuitry has a function to match the impedance of PC block the 50 Ω output.

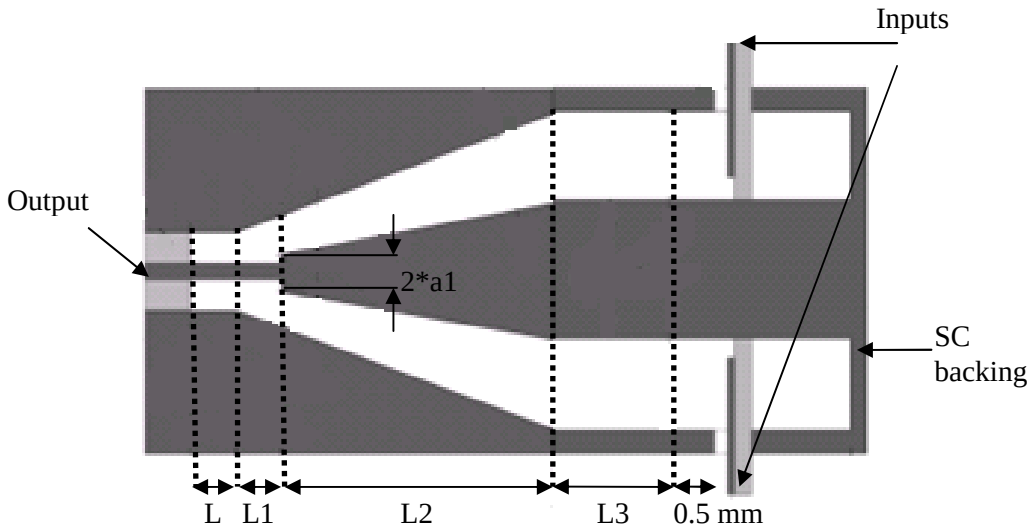



**Figure 6.6:** CWG matching block parameters for optimization method

At the end of the taper, before connecting the center conductor to SMA pin, a Teflon ring is placed. After the outer lid is connected to the main body, this ring is placed tightly between the end of the lid and the center conductor. This helps to correctly align inner and outer conductors with respect to each other, which is highly critical for appropriate CWG operation. The location of this ring is shown in Figure 6.7.

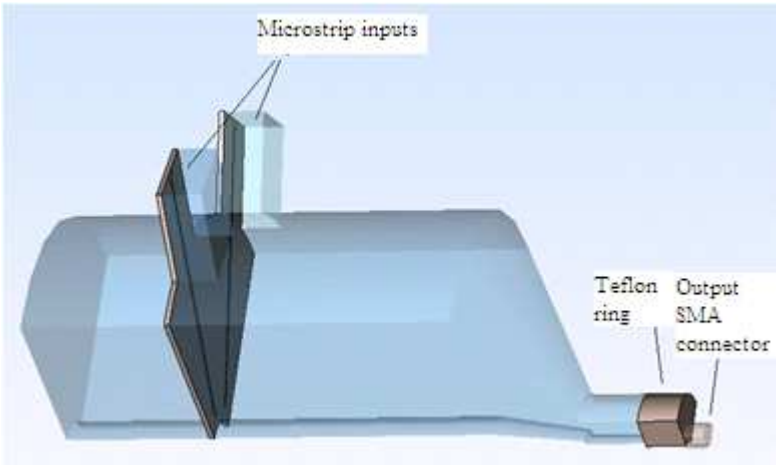



**Figure 6.7:** Location of the Teflon ring for optimization method simulation

The CWG matching part is initially modeled as L=L1=L2=L3=0.5 mm. After the initialization, a separate simulation for each parameter is made by incrementing its value. For each frequency band, the movement (impedance change) caused by each parameter increment is observed. These are used while parameter

tuning for impedance matching. The overall dimension parameters and selected values are given in Table 6-1.

**Table 6-1:** Selected parameter values for optimization method design

| **BW (GHz)** | ***a (mm)*** | ***b (mm)*** | ***W0 (mm)*** | ***h (mm)*** | ***Wh (mm)*** | ***Lr-Lp (mm)*** |
|---|---|---|---|---|---|---|
| 8.5 - 11.5 | 2 | 12,16 | 4 | 2,25 | 0,2 | 4,61 |
| 15.5 - 17.5 | 2 | 9,9 | 4 | 2,25 | 0,2 | 3,71 |
| | ***Wp (mm)*** | ***Lp (mm)*** | ***L4 (mm)*** | ***L3 (mm)*** | ***L2 (mm)*** | |
| 8.5 - 11.5 | 0,2 | 9,34 | 7,5 | 14 | 4,5 | |
| 15.5 - 17.5 | 0,2 | 4,8 | 4,54 | 2,53 | 4,8 | |

## 6.4 Completion

With the above parameters of the structure, the overall view and simulation results of final designs for X-band and Ku-band are shown in Figure 6.8 and Figure

6.9, respectively. The $S_{11}$ is seen better than 20 dB and the insertion loss introduced by the combiner is seen less than 0.2 dB per branch.

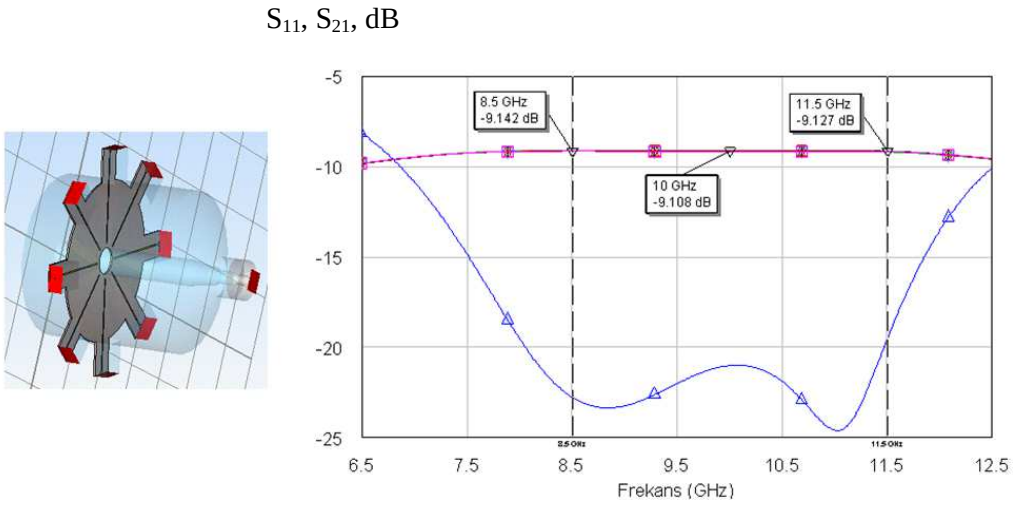



**Figure 6.8:** 3D simulation view and results at X-band for optimization method

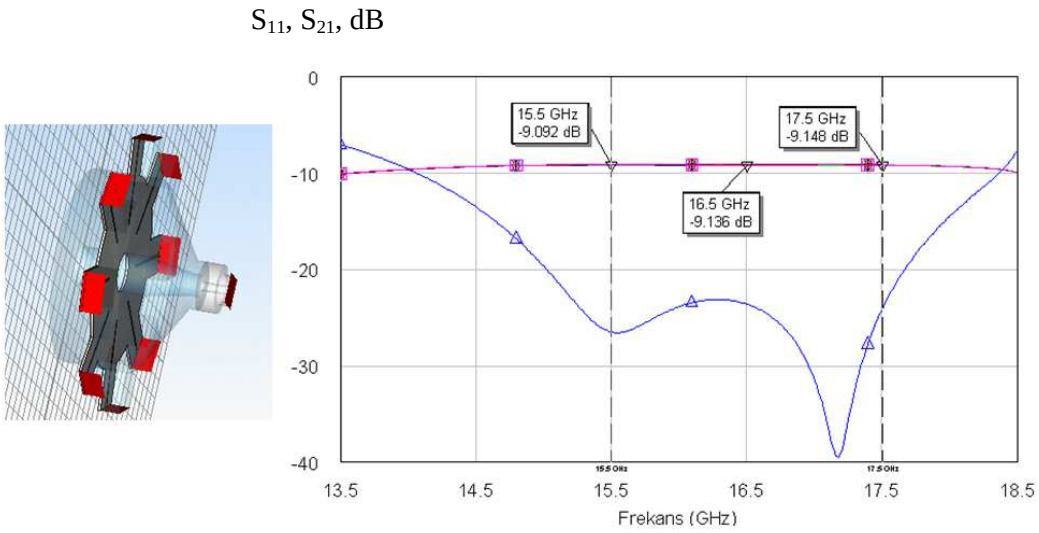


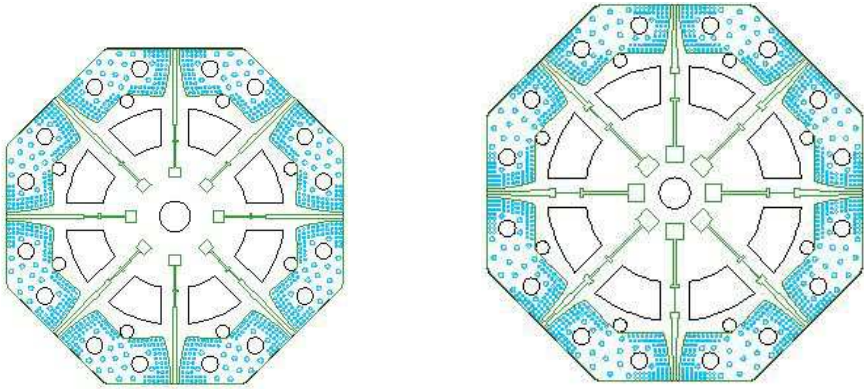

**Figure 6.9:** 3D simulation view and results at Ku-band for optimization method

## 6.5 Second Optimization for Probes

After completing the design, an alternative probe structure is considered. The aim of this alternative is to obtain a suitable structure for more output power. The most critical change that should be made is to reduce the risk of sparks at the tip of the probes. This can occur under high power between the tip of the probe and oversized CWG center conductor. In order to reduce that risk, the tip of the probe should be designed as wider and further away from the CWG center conductor as possible.

For this purpose, a two-stage probe is modeled with the stage connected to microstrip is thinner than the stage at the tip (Figure 6.10). Microstrip matching section is selected as a multistage microstrip. Probe and microstrip matching section

dimensions are swept. The widest and shortest probe which can be matched using a multistage microstrip circuit is selected for both bands. The layouts for these new probe types are given for X-band and Ku-band in (a) and (b) of Figure 6.10, respectively. These layouts include the coplanar to microstrip matching lines for coplanar input connectors, similar to sub-block method.



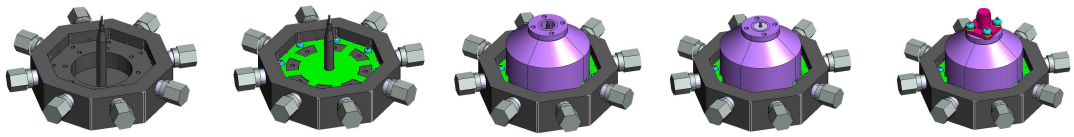
(a) (b)

**Figure 6.10:** Probe layouts after second probe structures for optimization method

## 6.6 Realizations of Combiners Designed by Optimization Method

For the optimization method, firstly the single stage versions were produced using SMA input and output connectors. The integration steps of the sub mechanical

parts are shown in Figure 6.11 (a) to (e). As seen from the figure, the center conductor of coaxial path, the base part carrying the probe board and the back short are produced as a single mechanical piece (a). The reason to include inner cylindrical conductor to the backside part is to reduce aligning problems that can occur while integrating two separate pieces of the thin cylinder. The probe board is then attached on this part using conductive epoxy in microstrip ground surfaces (b). After the board is placed, the top lid is placed which includes outer cylinders of tapered and stepped coaxial parts (c). Then, the Teflon ring at the end is placed tightly; this also ensures aligning of the lid with respect to the center conductor (d). Lastly, the SMA connector of the output port is attached (e).



(a) (b) (c) (d) (e)

**Figure 6.11:** Assembly of combiners designed by optimization method

The mechanical bodies was produced both with gold and silver plated samples. The aim of this plating selection is to reduce insertion loss of the combiners as much as possible. Since the waves, after combining in front of the probe board, travel in the air-filled coaxial line path and the currents flow on inner and outer cylindrical surfaces of the coaxial line path, the loss will be mostly occur on this path. The dielectric loss will be very low because of air medium. The conductor loss

can be minimized by using good conductors on inner surfaces of coaxial path. In order to be able to compare the performance of both, silver and gold plated mechanical paths are produced and integrated with probe board and the input/output connectors. The outer view of these parts is given in Figure 6.12.

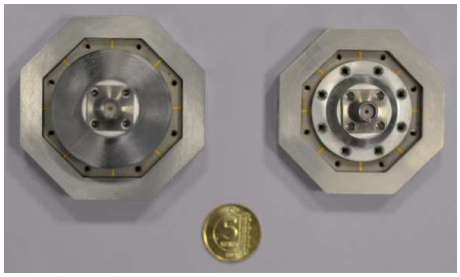
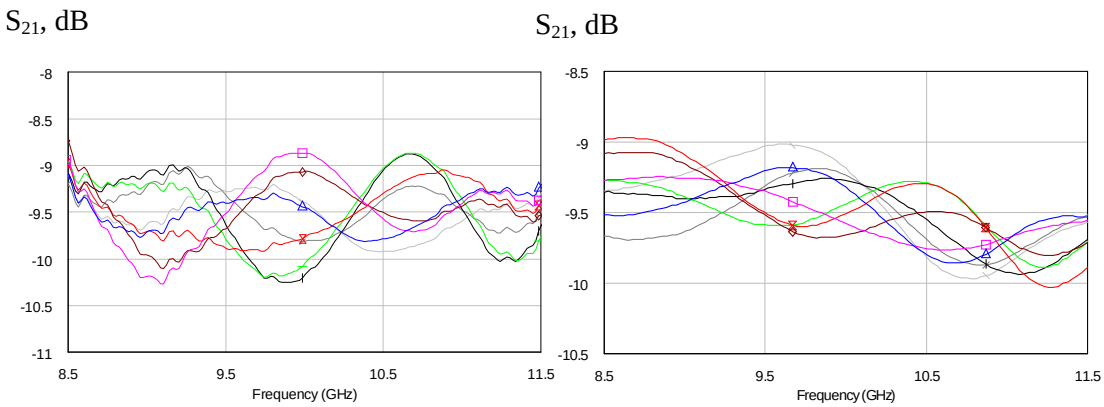


**Figure 6.12:** Outer view of mechanical parts for optimization method designs

In this optimization method design, one of the aims was to observe the effects of different connector, plating and probe types. In order to compare the input connector type, two combiners designed for 8.5-11.5 GHz band are used. The combiners are both designed by single stage probes and silver plating. Insertion losses of these combiners are shown in Figure 4.61. Graph (a) has SMA connectors connected through seals mounted on input walls and graph (b) has coplanar input connectors with the probe board squeezed between its terminals.

When Figure 6.13 is observed, the average insertion loss (between different inputs and different frequencies) is the same for both. The more significant difference is the frequency and magnitude of the ripples on insertion loss traces.

These ripples are formed because of non-ideal input terminations and poor isolation characteristics of the combiner. For the case of SMA connectors, the mounting of the seal is more complex and difficult to repair. This can be due to mounting process of the seal to input walls with epoxy of the seal itself. Any reflection caused by this non-ideality is transferred to other input ports because of poor isolation and the reflected power travels similarly inside the combiner. For all inputs these multiple reflected waves cancel each other at certain frequencies while they are added at other frequencies. This effect causes ripples on insertion loss characteristics. For SMA, risk of reflection was more, which will cause higher magnitude ripples, as observed in Figure 6.13 (a).

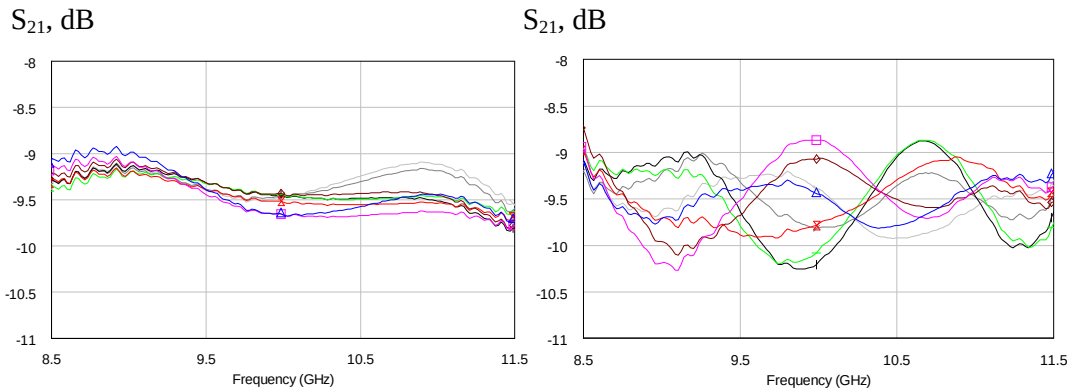



(a) (b)

**Figure 6.13:** Branch insertion loss graphs for connector type comparison

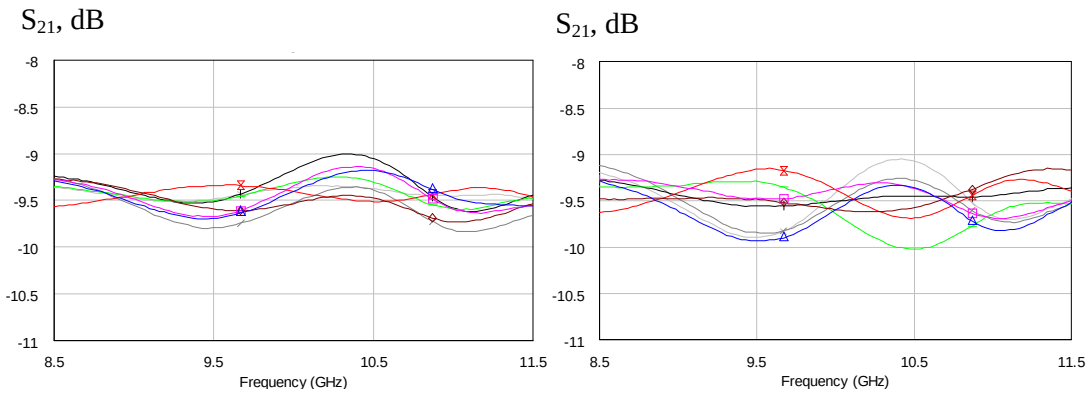
Difference between silver and gold plating are given in Figure 6.14 and Figure 6.15, all for 8.5-11.5 GHz frequency band. In Figure 6.14, the combiners belong to the design with the single stage probes and SMA input connectors. In Figure 6.15, the two-stage probe structure design is used with coplanar input

connectors. In both figures, the graphs on the left side are for gold plating and the graphs on the right side are for silver plating.




(a) (b)

**Figure 6.14:** Branch insertion loss graphs for plating type comparison (SMA connectors)

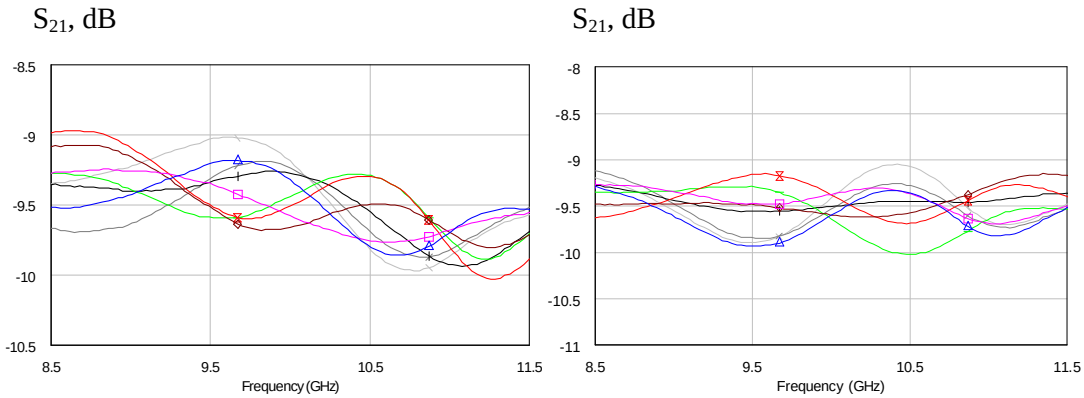



(a) (b)

**Figure 6.15:** Branch insertion loss graphs for plating type comparison (CPL connectors)

The main idea of comparing silver and gold plating types was to observe the effect on insertion loss. Since the path followed by the combined power is mostly the inner walls of the coaxial lids the loss is mainly determined by the plating on these walls. The average loss is very low and approximately the same for both plating types. The difference is, similar to input connector comparison, the ripples on insertion loss traces. The ripples for silver plating are more significant compared to gold plating. It is known that these ripples generally originate from non-idealities in the structure. Since silver plating is more prone to be damaged with environmental conditions, one of the reasons may be corruption of plating material. Another reason may be tiny mistakes in locating the probe board on silver surface. There is no certain control mechanism in the structure and the colors of the substrate and the plating are very close which makes the detection of errors more difficult than other cases.

The last comparison is between single-stage and two-stage probes for the design at 8.5-11.5 GHz with silver plating and coplanar input connectors, shown in Figure 6.16. The graph on the left belongs to the design with a single-stage thin probe with the appropriate matching lid above. The graph on the right belongs to the design with a two-stage wide-tip probe and its own matching lid. It can be observed that there is no significant difference in average insertion loss with respect to frequency or ripple characteristics on the traces. So an advantage of designing the probe with a single stage could not be observed. This information is used when selecting the type of combiner to use at output stage in power combining experiments. In this case it is more convenient to use a two-stage probe which provides both good matching and wide edge for the tip for the probe. The selected combiners and their responses for power combining modules will be presented in the next section of this chapter.




(a) (b)

**Figure 6.16:** Branch insertion loss graphs for probe stage number comparison

# CHAPTER 7

# POWER AMPLIFIER MODULES USING PLANAR PROBE COAXIAL WAVEGUIDE COMBINERS

## 7.1 Description of the Building Blocks for the Power Amplifier Modules

For the first experiment on power combining performance of the combiner designs, a basic power amplifier driver block is designed and produced with ~2 W output power. The amplifier block is designed to work in 6-18 GHz frequency band. Thus, this block could be used to examine the performance of both 8.5 – 11.5 GHz and 15.5 – 17.5 GHz combiner designs. In each feed block, there are two separate paths with the same layout. In the module, there are two combiner structures. 4 feed blocks are used to feed the 8 parallel branches of combiners. Feed blocks and the combiners are connected on a single metal carrier body, which also has the function of cooling the module. On this mechanical body, as the first step a combiner is used as a divider. The module input is divided into 8 equal parts and carried to feed block inputs via bendable amplitude and phase matched coaxial cables. These signals are amplified separately in the 8 channels of 4 feed blocks. Power at the output of each channel is then carried to the second combiner. At the output of this combiner, the power value is measured to be evaluated.

In Figure 7.1, the layout of a feeding amplifier block is shown. At the output of each channel, shown with number 3 on the figure, TGA2510 amplifiers with 6-18 GHz operating frequency band and 2.8 W output power are used.

In order to prevent power combining loss which can occur due to phase and amplitude imbalance, elements shown with number 1 and 2 are used. In Figure 7.1, the element shown with number 1 has the function of phase shift up to 180 degrees with 6 steps each shifting 30 degrees. The elements shown with number 2 are used for amplitude adjustment. This gives 0-4 dB amplitude adjusting range with 1 dB steps to each of the channels. The sufficiency of this much tuning option is also verified in a linear simulation program, similar to the adjustment of the insertion phases.

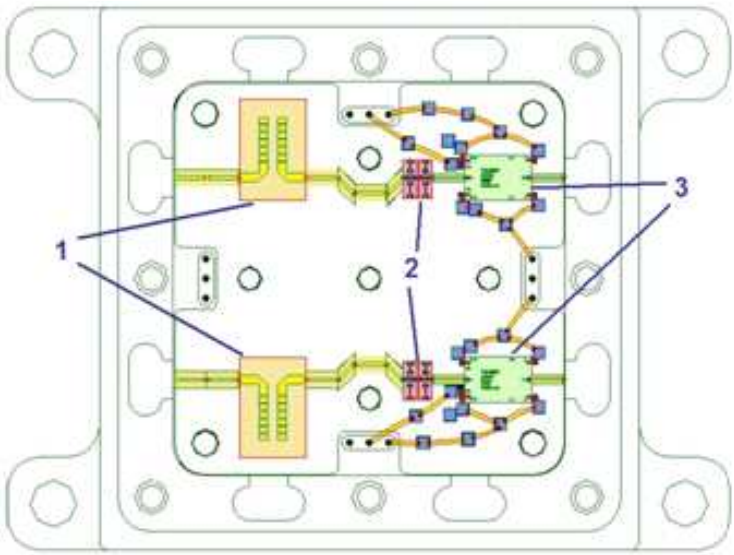



**Figure 7.1:** Layout of the feeding amplifier blocks

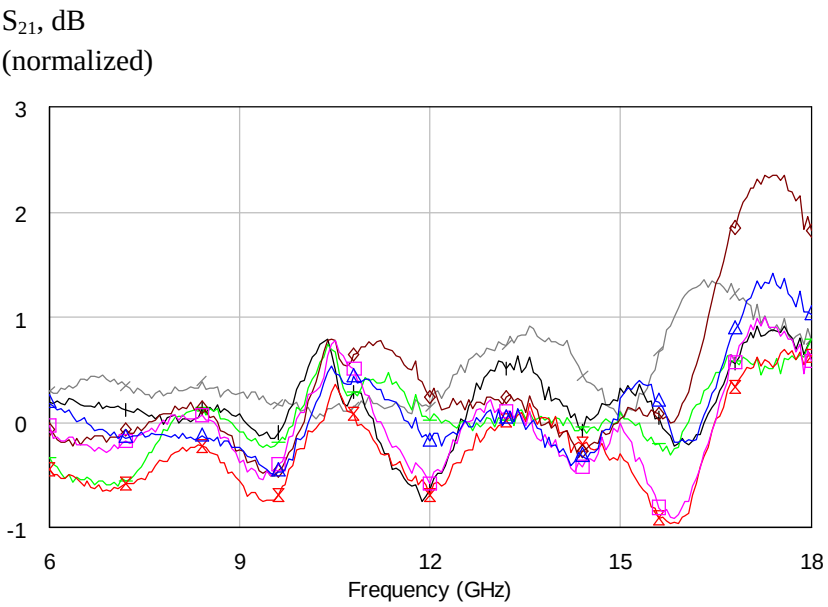



**Figure 7.2:** Small-signal gain differences of feed amplifier channels

Before the integration of the feed blocks to the amplifier module, S parameters of all 8 channels in small-signal operation are measured. The total 8 amplifying channels for 8 combiner inputs packaged in separate modules are all measured in the linear region. In order to obtain efficiency in power combining, the differences in gain and phase values are important rather than the actual values. Thus, for each channel, the gain and phase differences are plotted with respect to one of the channels selected as a reference. The gain difference plot (in dB) and the phase difference plot (in degrees) are given in Figure 7.2 and Figure 7.3, respectively.

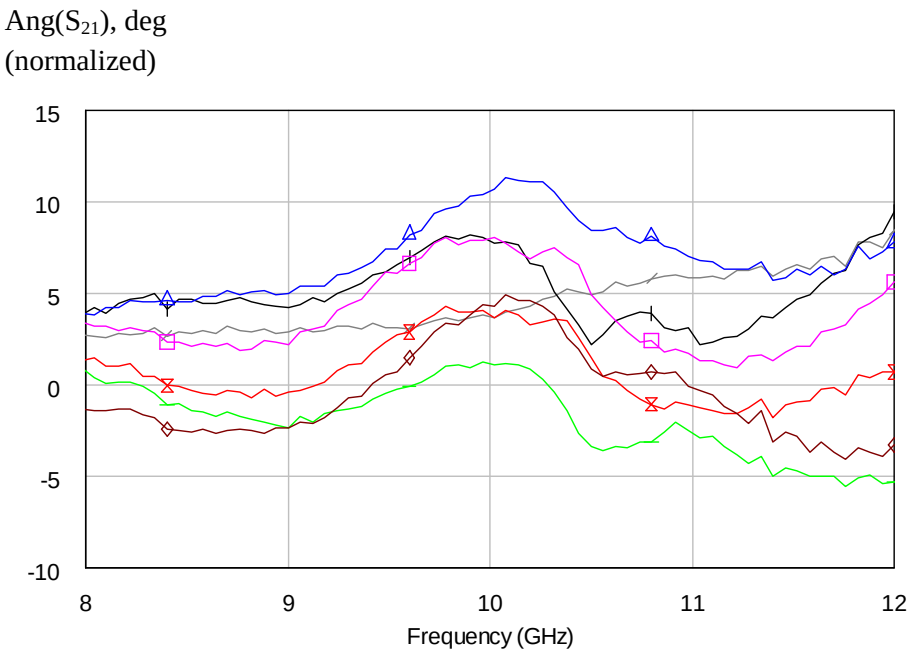



**Figure 7.3:** Small-signal insertion phase differences of feed amplifier channels

At center frequency, the gain imbalance between branches is within ~ 1 dB and the phase imbalance is within ~ 10 degrees according to the measurements. For that frequency, these limits are both acceptable limits for efficient combining of the channel output powers. According to the gain plots, the gain difference could be decreased at the upper side of the frequency band using the wideband attenuator. However, in this case the difference in the rest of the band will be increased. In order to obtain acceptable response in the larger portion of the frequency band, no adjustments are made using the selectable attenuator. According to the phase plots, the limits are acceptable for all frequencies in operation band. The adjustment steps

are 30 degrees, moreover the phase shift value is not constant in the frequency band; thus no phase adjustments are made between amplifier channels as well.

In the power amplifier modules, the combiners and driving blocks are placed on a metal block which carries the elements and helps heat removal. The building elements are integrated on this metal blocks via flexible SMA cables with 3.5 inches length.

## 7.2 8-12 GHz Power Amplifier Module Structure and Measurement Results

For constructing the 8-12 GHz power amplifier, the combiners that will be used in dividing the input power and combining amplifier channel outputs are selected at first. The combiner used at input is a silver plated two-stage probe combiner with coplanar input connectors. The passive response of this combiner is given in Figure 7.4.

For the output, the gold plated version of the input combiner is used. The usage of two-stage probe combiner at output is due to the wide probe edge in this probe structure. This property decreases the failure risk due to spark creation at the output probe tips under high power. The passive response of the output stage combiner is given in Figure 7.5.

The view of 8-12 GHz power amplifier module can be seen in Figure 7.6.

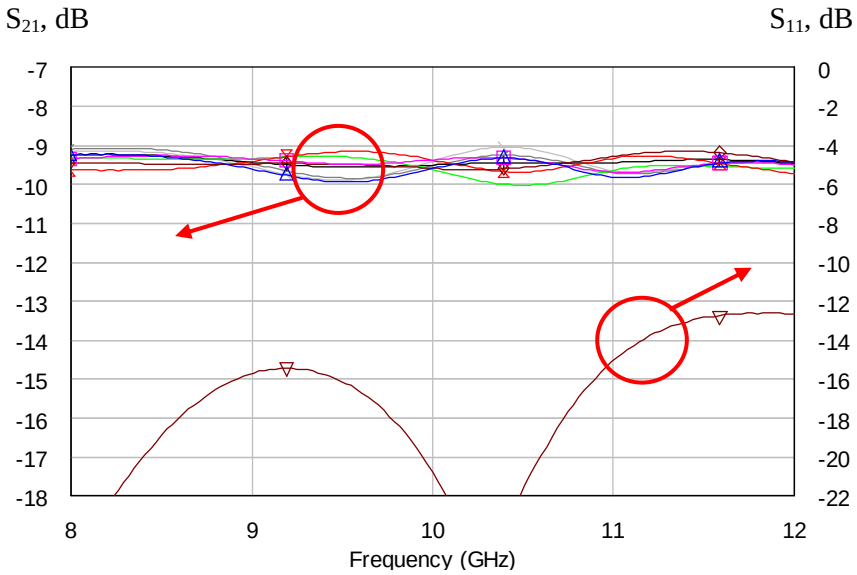



**Figure 7.4:** Input combiner passive response for X-band module

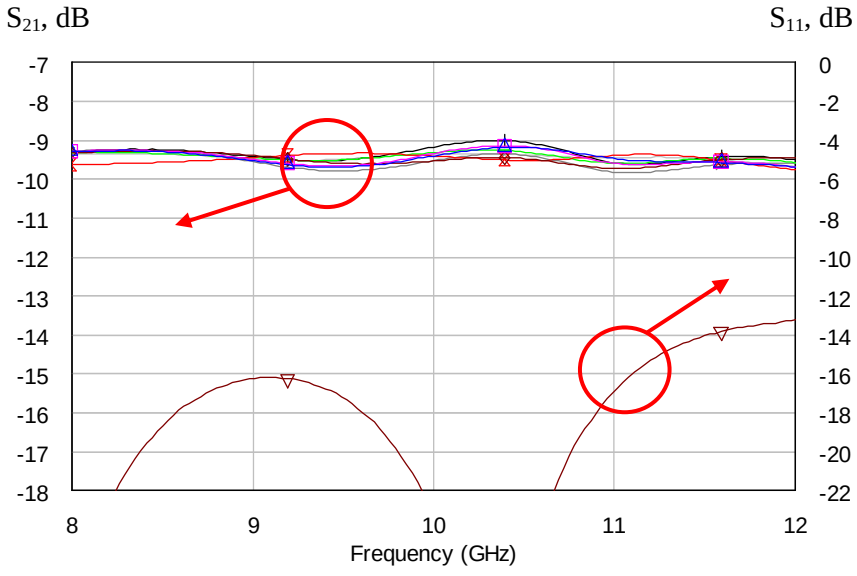



**Figure 7.5:** Output combiner passive response for X-band module

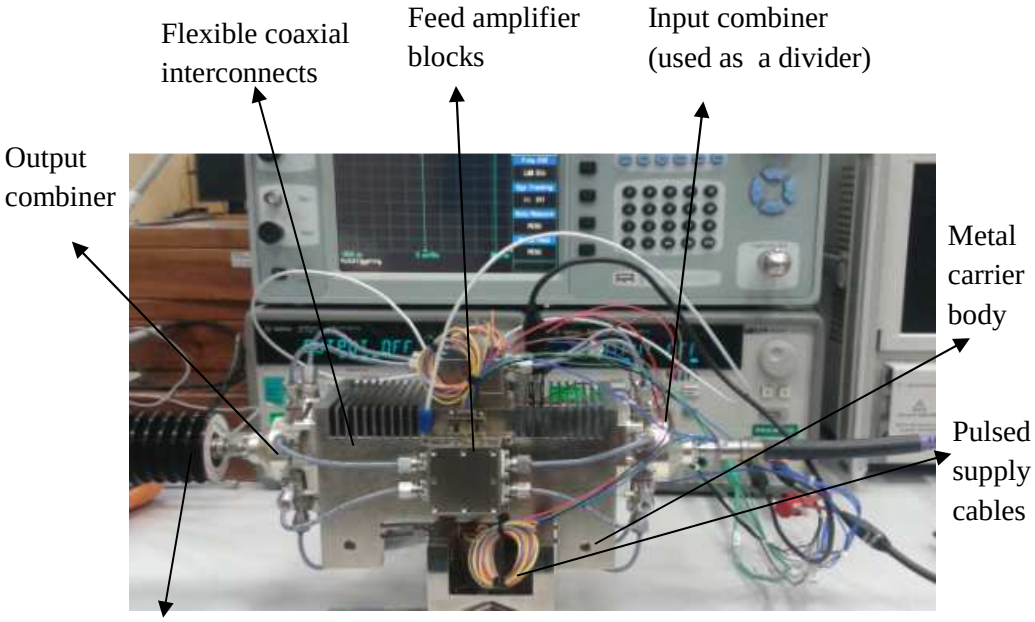



**Figure 7.6:** View of 8-12 GHz power amplifier module

The output power values of the module are measured in the 4 dB compression point for 0,5 GHz frequency steps. The measurements are made at 10% duty cycle with 10 µs pulse width. The results are plotted in Figure 7.7. In the figure, a curve for expected output power is also added. This power is calculated from the average of output powers for 8 amplifier channels and the insertion loss of the output combiner.

The measured and expected values are close according to the plots. Expected value is calculated as below:

| | | | | | | |
|---|---|---|---|---|---|---|
| Feed channel output power at P4dB (~34 dBm) | + | 9 dB (ideal 8-way combining) | – | Loss introduced by combiner per branch (~0.5 dB) | – | Cable loss (~0.3 dB) |

The calculated combining efficiency is around 90%. There is ~1.5dB difference at some frequencies. This difference is partly due to assumption of equal channel outputs as the average of 8 channels. There is an amplitude difference which will cause the combined power to defect from the expected value.

Moreover, the compression effects are not included in the expected power calculations. According to the individual amplifier channel measurements, although the linear region gains are similar, the channel compression points are not all equal to the compression point of the module at those frequencies. As the compression level increases, the insertion phase starts to increase rapidly and cause phase difference between channels. This phase difference result in less effective combination of channel output powers.

Lastly, some of the decrease in power might be caused because the isolation values of the output combiner are not ideal and there is no isolator at channel outputs. At high compression points, the output impedance of amplifiers are not ideal. Thus, the load impedances of each amplifier are affected by the output impedance of adjacent amplifiers. This will change amplifier load impedance at high power and deviate amplifier characteristics from the expected values which are measured under ideal load conditions.

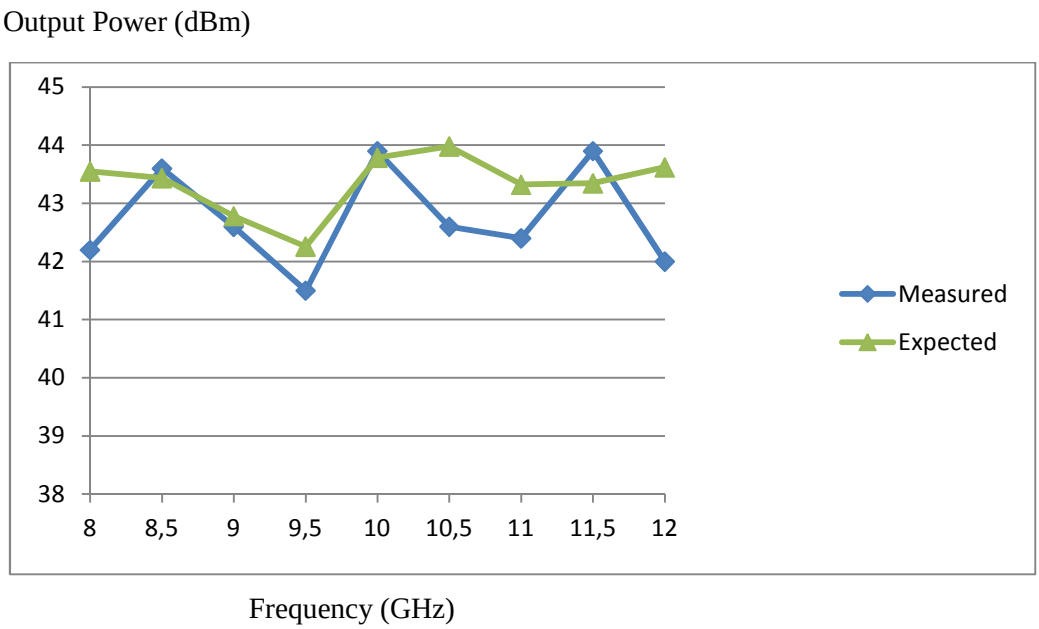



**Figure 7.7:** Expected and measured output powers at P4dB for X-band module in dBm

### 7.3 15-18 GHz Power Amplifier Structure and Measurement Results

In this amplifier, similar to the 8-12 GHz case, the input combiner is selected as single-stage thin probe silver plated design with coplanar input connectors, while the output combiner is selected as the two-stage probe version of the same combiner mechanics, however in this case gold plated mechanic is used for output because of availability drawbacks. However, the gold plated structures are generally preferred due to better symmetry of input insertion losses. The response of the input combiner is given in Figure 7.8 and the response of output combiner is given in Figure 7.9.

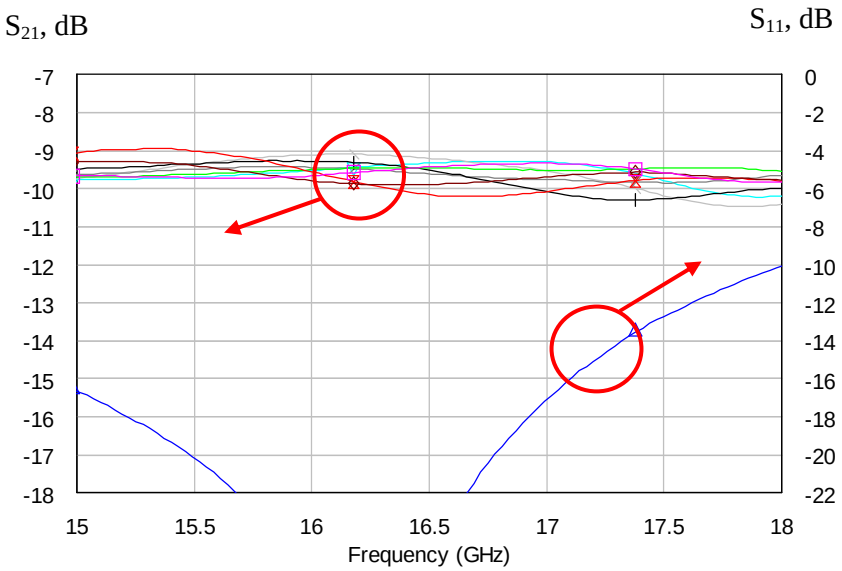



**Figure 7.8:** Input combiner passive response for Ku-band module

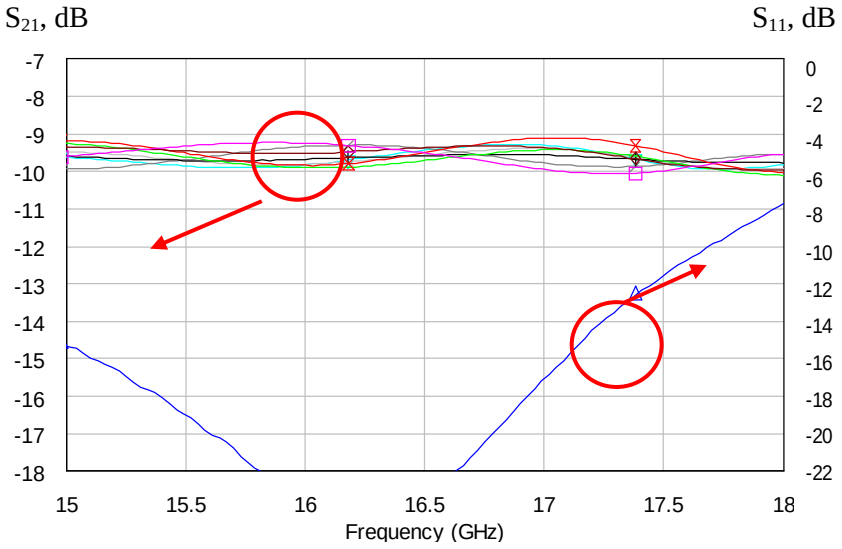



**Figure 7.9:** Output combiner passive response for Ku-band module

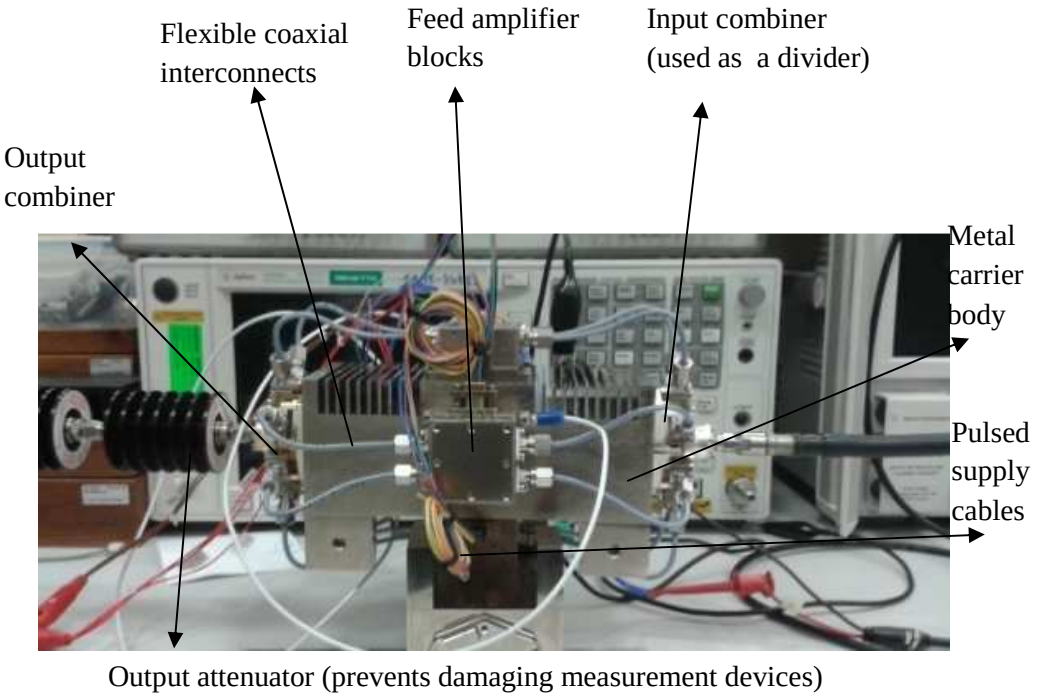



**Figure 7.10:** View of 15-18 GHz power amplifier module

The view of the module and measured output power levels (in dBm) for this module are given in Figure 7.10 and Figure 7.11, respectively. The measurements are made at 10% duty cycle with 10 µs pulse width. The calculated combining efficiency is around 80%.

The expected values are calculated and deviations from expected values could be explained from the same ideas presented for 8-12 GHz module. At some points, expected power is below the measured value. The reason might be that most of the channel outputs are more than the average assumed output value. Moreover

the values may have increased in the output impedance conditions set by the combiner, which could not be estimated.

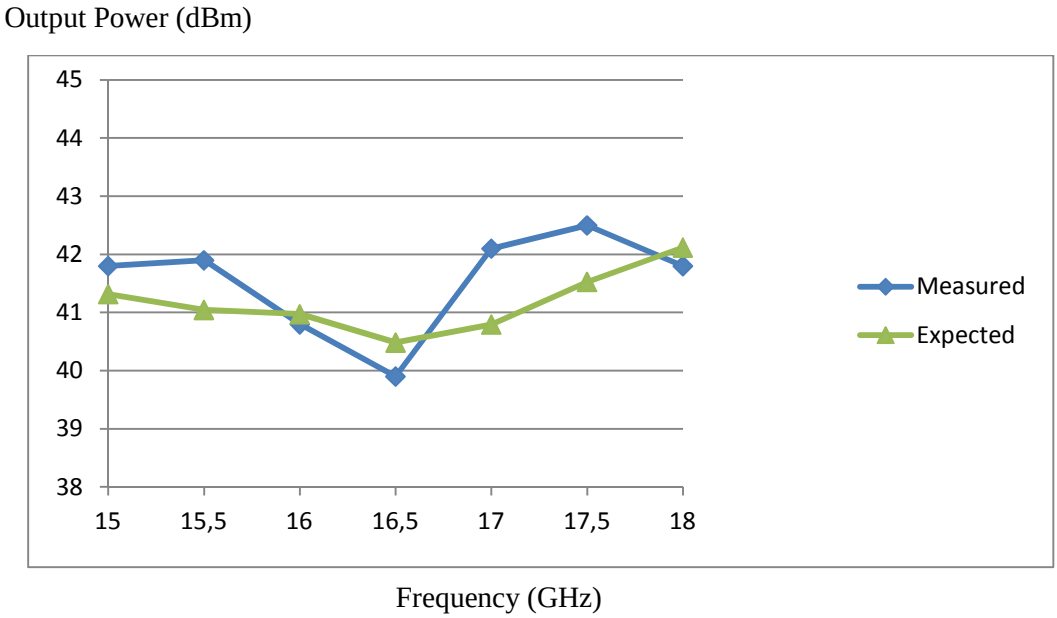



**Figure 7.11:** Expected and measured output powers at P4dB for X-band module in dBm

# CHAPTER 8

# CONCLUSION

In this thesis, several low loss power combining techniques are investigated for comparison. For the 8-way microstrip Wilkinson combiner, insertion loss is low compared to cascaded combiners with the same total number of arms. However, because of dielectric and conductor losses, insertion loss remains high compared to SSS branchline and planar probe CWG combiners. For the SSS branchline combiner, dielectric loss is minimized due to usage of air medium. Moreover, low $\varepsilon_r$ means wide copper lines which decrease conductor loss. Lengths of lines are also increased with low $\varepsilon_r$; but this increase is less effective on insertion loss than the widening of lines. The lowest insertion losses are observed for the planar probe coaxial waveguide (PPCWG) combiners. This is partly due to transmission in air medium, which minimizes the dielectric loss. Part of the improvement in insertion loss is due to currents flowing in CWG inner surfaces. These surfaces are both very wide and plated with good conductor metals. These properties decrease the resistivity of transmission lines and thus the conductor loss.

For all combining techniques, insertion loss calculated by the simulation software is very low. The difference between measured value and simulated value can be explained differently for different techniques. For the planar probe CWG combiner, the loss value is close to the simulation result except the ripples which cause differences in branches. The difference is caused by non ideal connector impedances and imbalance among branches due to production tolerances which could not be modeled in the software. For SSS combiner, the extra loss is partly due

to the non ideal boundary conditions in the actual combiner. Via holes may not give exactly the same response with the perfect electrical walls. Part of the loss is due to more resistive lines in actual combiner because of the skin effect. The skin depth is very low at the design frequency which needs closely spaced mesh on the metal which the software could not support. A similar effect exists for the microstrip combiner. In this case the skin depth is also very low at the end of the frequency band and metal loss is more dominant in this structure; thus the weakness of modeling causes more difference between simulated and measured results.

Since the best performance is obtained with planar probe CWG combiners, power amplifier modules are built with these combiners in order to test power combining operation. Two modules are built in 8-12 GHz and 15-18 GHz bands. Output powers of the modules are about 15 W. Combining efficiency came out to be approximately 85%.

Finally, power handling test is applied using TWTA at 10 GHz. It is seen that all probes in PPCWG designs can operate up to 2 kW without spark occurrence. Thus, each probe turned out to be handling 250 W power. This experiment leads to the conclusion that, if necessary power inputs can be supplied from input terminals and cooling is maintained, powers up to 2 kW can be achieved by using PPCWG combiners.

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