A LOW-POWER CAPACITIVE INTEGRATED CMOS READOUT CIRCUITRY FOR HIGH PERFORMANCE MEMS ACCELEROMETERS

A THESIS SUBMITTED TO
GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
MIDDLE EAST TECHNICAL UNIVERSITY

BY

OSMAN SAMET İNCEDERE

IN PARTIAL FULLFILLMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF MASTER OF SCIENCE
IN
ELECTRICAL AND ELECTRONICS ENGINEERING

SEPTEMBER 2013

Approval of the thesis:

A LOW-POWER CAPACITIVE INTEGRATED CMOS READOUT CIRCUITRY FOR HIGH PERFORMANCE MEMS ACCELEROMETERS

submitted by **OSMAN SAMET İNCEDERE** in partial fulfillment of the requirements for the degree of **Master of Science in Electrical and Electronics Engineering Department, Middle East Technical University** by,

Prof. Dr. Canan Özgen
Dean, Graduate School of **Natural and Applied Sciences** _____

Prof. Dr. Gönül Turhan Sayan
Head of Department, **Electrical and Electronics Engineering** _____

Prof. Dr. Tayfun Akın
Supervisor, **Electrical and Electronics Eng. Dept., METU** _____

Dr. Selim Eminoğlu
Co-Supervisor, **Mikro-Tasarım San. ve Tic. Ltd. Şti.** _____

Examining Committee Members:

Assoc. Prof. Dr. Haluk Külah
Electrical and Electronics Eng. Dept., METU _____

Prof. Dr. Tayfun Akın
Electrical and Electronics Eng. Dept., METU _____

Dr. Selim Eminoğlu
Mikro-Tasarım San. ve Tic. Ltd. Şti. _____

Assoc. Prof. Dr. Barış Bayram
Electrical and Electronics Eng. Dept., METU _____

Assoc. Prof. Dr. Kıvanç Azgın
Mechanical Eng. Dept., METU _____

Date: 03.09.2013

I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

Name, Last Name: Osman Samet İncedere

Signature:

ABSTRACT

A LOW-POWER CAPACITIVE INTEGRATED CMOS READOUT CIRCUITRY FOR HIGH PERFORMANCE MEMS ACCELEROMETERS

Osman Samet İncedere

M.Sc., Department of Electrical and Electronics Engineering

Supervisor : Prof. Dr. Tayfun Akın

Co-Supervisor : Dr. Selim Eminoğlu

September 2013, 79 pages

This thesis presents a low power capacitive integrated CMOS readout circuitry for high performance MEMS accelerometers. It proposes a linearized model of the complete closed loop accelerometer system, which makes easier of designing and analyzing the system. Designed readout circuitry offers low noise, wide dynamic range and high linearity system with very low power consumption. Designed readout circuit includes proportional integral (PI) controller circuit, which significantly decreases the proof mass deflection of the accelerometer resulting in high linearity and high immunity to sensor parameter changes. Designed system also suppresses the readout circuit noise in a significant amount and this noise suppression allows designing very low power readout circuits without degrading the noise performance of the system. Readout circuit provides highly programmable digital controller circuit, which allows controlling of all digital timing signals, bias currents and voltages, and power consumptions of analog blocks, front-end circuit gain, gain coefficients of PI controller and sigma-delta modulator gain. Designed readout circuit also offers optional external timing signals and optional external voltage reference. The readout circuit is implemented using 0.35 um process. Circuit level and system level simulations are performed in Cadence and MATLAB Simulink environments respectively. The simulations guarantee stability and proper operation of the accelerometer system. As a sensing element, accelerometer having the

specifications of $3.5x10^{-6}$ F/m sensitivity, 9.5 pF rest capacitance, 2.32 kHz resonant frequency and 4.6 μg/√Hz Brownian noise, is used. Simulation results show that system has 5.3 μg/√Hz noise level at the output, ± 19.5 g full scale range, 128.5 dB dynamic range and 1.8 mW power consumption with 3.3 V supply voltage.

Keywords: MEMS accelerometers, low noise electronics, closed-loop accelerometer systems, capacitive readout circuit, sigma-delta modulator.

ÖZ

YÜKSEK PERFORMANSLI MEMS İVMEÖLÇERLER İÇİN
DÜŞÜK GÜÇ TÜKETİMLİ KAPASİTİF TÜMLEŞİK CMOS OKUMA DEVRESİ

İncedere, Osman Samet
Yüksek Lisans, Elektrik ve Elektronik Mühendisliği Bölümü
Tez Yöneticisi : Prof. Dr. Tayfun Akın
Ortak Tez Yöneticisi : Dr. Selim Eminoğlu

Eylül 2013, 79 sayfa

Bu tez yüksek performanslı MEMS ivmeölçerler için düşük güç tüketimli kapasitif tümleşik CMOS okuma devresi sunmaktadır. Bu tez kapsamında kapalı devre ivmeölçer sistemleri için doğrusal model önerilmektedir. Bu doğrusal model sistem analizini ve tasarımını kolaylaştırmaktadır. Tasarlanan okuma devresi çok düşük gürültülü, geniş dinamik aralığa ve yüksek doğrusallığa sahip sistemi, düşük güç tüketimiyle sunmaktadır. Tasarlanan okuma devresi ivmeölçerin hareketini azaltmayı sağlayan oransal-integral denetleyici içermektedir ve ivmeölçerin az hareket etmesi yüksek doğrusallığı ve sensör değişkenlerine bağlılığın azalmasını sağlamaktadır. Tasarlanan sistem ayrıca okuma devresi gürültü seviyesini büyük ölçüde bastırmaktadır ve bu, sistem performansının düşmesine sebep olmadan düşük gürültülü okuma devresi tasarlamaya olanak sunmaktadır. Okuma devresi bütün sayısal zamanlama sinyallerini, analog devrelerin kutuplama akım ve voltaj değerlerini, ve güç tüketimini, ön uç devresinin kazancını, oransal-integral denetleyicinin kazanç katsayılarını ve sigma-delta modülatör devresinin kazancını kontrol etmeye olanak sağlayan oldukça yüksek programlanabilir özelliğe sahip sayısal denetleme devresi içermektedir. Ayrıca, tasarlanan okuma devresi isteğe bağlı olarak çip dışından sayısal zamanlama sinyallerinin ve referans voltajının kullanılmasını sağlamaktadır. Okuma devresinin tasarımı 0.35 um CMOS teknolojisinde geliştirilmiştir. Devre düzeyinde ve sistem

düzeyinde simülasyonlar sırasıyla Cadence ve MATLAB Simulink programlarında yapılmıştır. Simulasyonlar ivmeölçer sisteminin kararlılığını ve düzgün çalışmasını teyit etmiştir. İvmeölçer olarak $3.5x10^{-6}$ F/m hassasiyetli, hareketsiz halde 9.5 pF kapasiteye sahip, 2.32 kHz yankılama frekansında ve 4.6 μg/√Hz Brownian gürültüsüne sahip bir ivmeölçer kullanılmıştır. Simulasyon sonuçları 5.3 μg/√Hz çıkış gürültü seviyesi, ± 19.5 g giriş aralığı, 128.5 dB dinamik aralık ve 3.3 V güç kaynağı ile 1.8 mW güç tüketimi olduğunu göstermiştir.

Anahtar kelimeler: MEMS ivmeölçerler, düşük gürültülü elektronik, kapalı devre ivmeölçer sistemleri, kapasitif okuma devresi, sigma-delta modulator.

To my family

ACKNOWLEDGEMENTS

I would like to express my gratitude towards my advisor Prof. Dr. Tayfun Akın for his supervision and guidance throughout this study. I would like to thank Dr. Selim Eminoğlu for his endless support and trust through my graduate life.

I would like to thank Burak Eminoğlu and Uğur Sönmez for their technical guidance and sharing their knowledge and experience at every stage of this study.

I also would like to thank all of the colleagues at Mikro-Tasarım, Nusret Bayhan, Mehmet Ali Gülden, Suhip Tuncer Soyer, Murat Işıkhan, Serhat Koçak, Siner Gökhan Yılmaz, Mithat Cem Boreyda Üstündağ, Özge Turan, Cem Yalçın, Mehmet Akdemir, Murat Aktürk and Emine Aytekin for their invaluable friendship and support during this work.

I would like to thank my previous colleagues at Mikro-Tasarım, Çağlar Altıner, Yiğit Uygar Mahsereci and Celal Avcı for their friendship and providing a pleasant working environment.

I would like to express my gratitude towards to TUBİTAK for their support of my M.Sc. study with their scholarship.

Last but not least, I would like to give my special thanks to my mother, my father and my brother for their endless trust, encouragement and patience in every moment of my life. I would like to thank my grand mother for her endless love and interest on me throughout my life. Without their invaluable support, I would not achieve this success.

TABLE OF CONTENTS

LIST OF TABLES

TABLES

LIST OF FIGURES

FIGURES

CHAPTER 1

INTRODUCTION

Micro-Electro-Mechanical Systems (MEMS) is a technology using the techniques of microfabrication to obtain the miniaturized mechanical or electro-mechanical devices or structures. The physical dimensions of MEMS devices can vary in the range of below one micron to a few millimeters. Similarly, MEMS devices have different type of structures. While some types contain simple structure without any moving element, some of them include very complex electromechanical system with multiple moving elements controlled by integrated electronic circuitry. One of the main criteria defining a structure or a device as a MEMS device is that there should be some parts in the miniaturized structure, which achieve some type of mechanical functionality even if these parts cannot be movable parts [1].

MEMS offer several advantages, which makes it one of the most promising technologies of 21th century. Firstly, MEMS provides devices that can be produced with a combination of many different fields seen unrelated previously. Biology and microelectronics are one of the important examples of the interdisciplinary nature of MEMS technology. Secondly, MEMS offers high performance and reliable components and devices due to its batch fabrication techniques. Thirdly, cost, size and weight of the MEMS devices are significantly low, which allows them very commonly used in industrial and consumer products. Lastly, manufacturing of products by MEMS cannot be made any other techniques [2].

The history of MEMS lays into the early of 1950's. Over the half-century, MEMS has gradually been out of the subject that is only researched in R&D laboratories and it has found a place in everyday products. Especially, in the mid-1990's MEMS devices began to commercialize and appeared in lots of commercial products and applications. Size of MEMS market has grown excessively after 1990's and today it exceeds 10 billion dollar per year. It is predicted that MEMS market will continue to increase its size and reaches a size of 20 billion dollar in three years. Figure 1.1 illustrates the MEMS market distribution according to application areas from 2010 to 2016 [3].

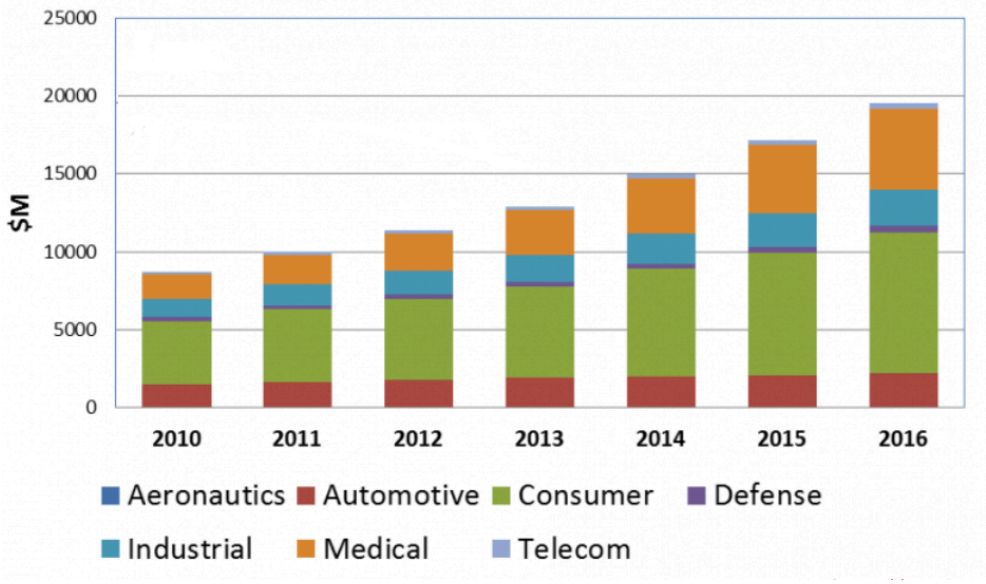

Figure 1.1: MEMS market distribution according to applications in 2010-2016 [3].

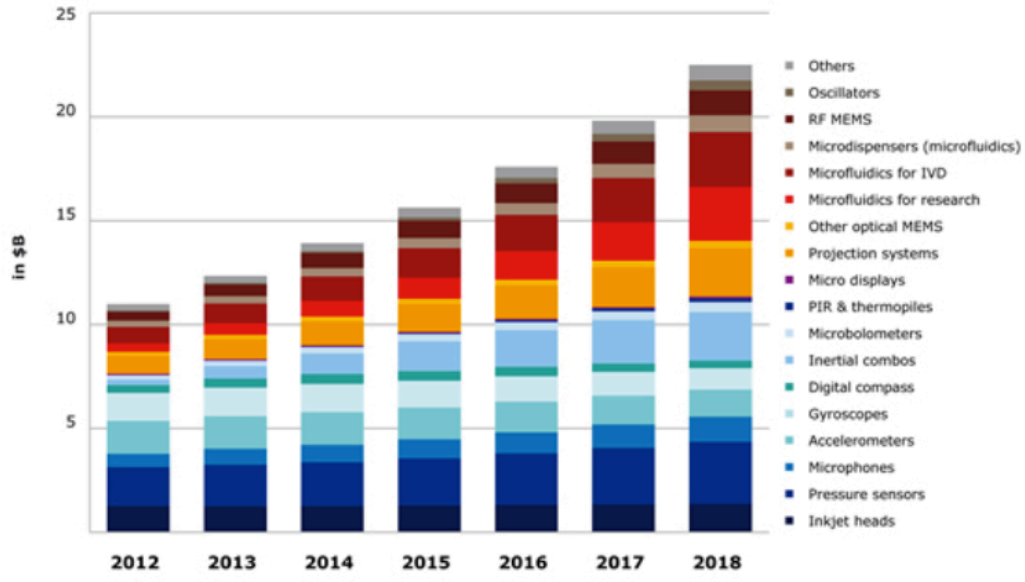

Figure 1.2: MEMS market distribution according to devices in 2012-2018 [4].

MEMS market offers a very wide range of products from different application areas that meet the needs of customers. Figure 1.2 shows the MEMS market distribution according to devices between 2012 and 2018 [4]. As it is clear from the figure that a large variety of MEMS devices are extensively used in the market and accelerometers have a big place in the market along with the pressure sensors.

Inertial sensors, including accelerometer and gyroscope, are one of the most significant types of MEMS devices. MEMS accelerometers are very demanding and quite popular due to their low-power, low-cost, small size and reliable operation. They have the second largest sales volume after pressure sensors [2].

The first MEMS accelerometer was designed in 1979 in Stanford University. However, MEMS accelerometers were used as products for large volume applications after 15 years later from the first design. Automotive airbag sensors are one of the first commercial devices using MEMS accelerometers. All today's cars use MEMS accelerometer in the airbag. MEMS accelerometers are not limited to automotive applications. The application of them covers very broad spectrum such as navigation and guidance system, biomedical applications for activity monitoring, tracking and monitoring mechanical shock, earthquake detection, automotive industry, image stabilization, microgravity measurement in space, tilt sensing and animal tracking [5] [6] [7].

Performance of accelerometers can be measured according to the parameters such as operation range, bandwidth, resolution, linearity and offset and performance requirements of accelerometers change with the applications that they are used. For example, navigation grade accelerometers should have a resolution in the range of μg. However, in ballistic and impact sensing application, resolution is not that critical. 1g resolution is quite enough. Nevertheless, operation range should be in the range of 10000 g. Figure 1.3 shows the application areas of MEMS accelerometers and their required specifications [8].

In the scope of this thesis work, a capacitive type MEMS accelerometer is used and studied. An accelerometer system is composed of two main parts: the sensor and the readout electronics. The capacitive sensor itself reacts to external acceleration with a capacitance change. This capacitance change should be converted into an electrical quantity to measure the acceleration input. Electronic readout circuits are used to perform this conversion. Acceleration sensitivity and range as well as the output noise are main important parameters for an accelerometer. For portable applications power dissipation becomes also very important parameter, especially for systems that run on batteries. In this thesis, a low-power programmable integrated CMOS readout circuit is designed and implemented for capacitive type MEMS accelerometers. Due to the programmable features of this new readout circuit, it becomes easy to interface various capacitive MEMS accelerometers.

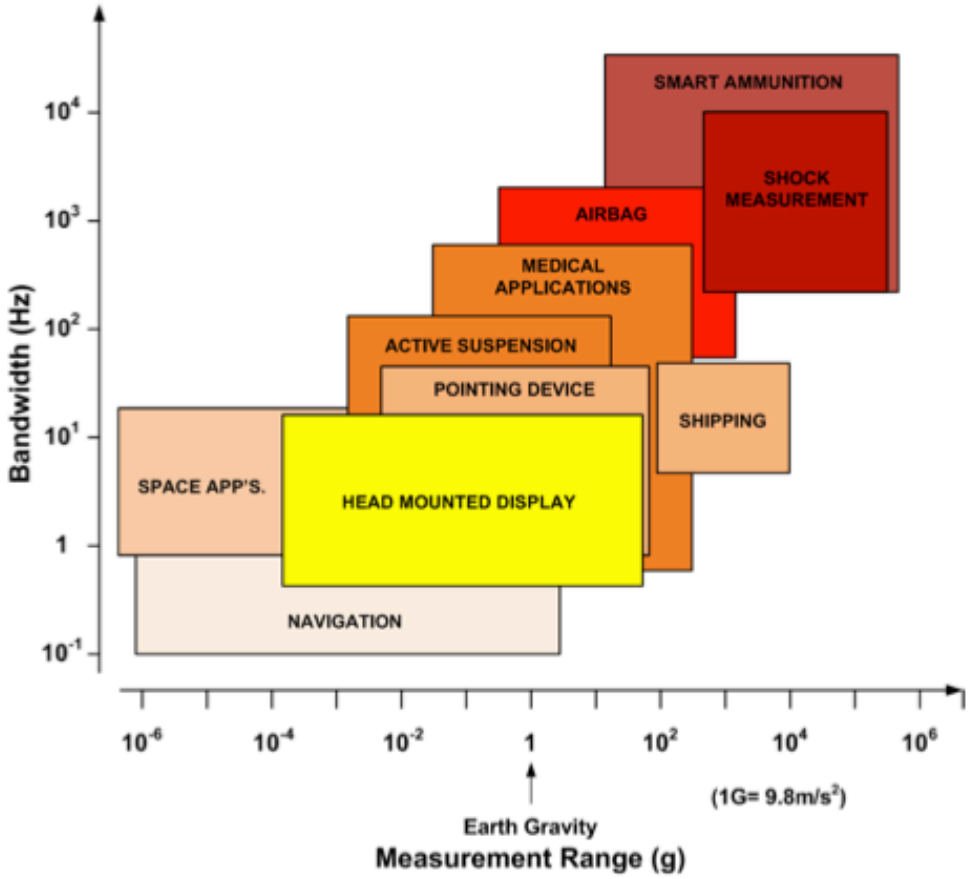

Figure 1.3: MEMS Accelerometer Applications and their required specifications [8].

1.1 Classification of Accelerometers by Sensing Mechanism

MEMS accelerometers can be classified according to their sensing mechanism:

1) Capacitive
2) Piezoresistive
3) Piezoelectric
4) Hall effect
5) Magnetoresistive
6) Heat transfer

Capacitive accelerometers sense the capacitance change as name suggests. When external force is applied to the accelerometer, proof mass changes its position and the

capacitance value between proof mass and electrode fingers is altered. Change in capacitance is then detected by electronic circuit.

Piezoelectric accelerometers make use of piezoelectric effect that is defined as generation of electrical potential due to the stress applied on materials such as crystals. Electrical charge is created when external acceleration is applied and this charge can be detected with an electronic circuitry to obtain acceleration information. Piezoresistive accelerometers work with the principle of measuring the electrical resistance of a material when external acceleration is applied to it. In Hall effect type accelerometers, voltage variations created due to the change in the magnetic field around the accelerometer are measured. Magnetoresistive accelerometers measure changes in resistance due to magnetic field. They are very similar to the Hall effect accelerometers. The difference between them is that magnetoresistive accelerometers measure resistance instead of measuring voltage. In heat transfer accelerometers internal changes in heat transfer are measured because of acceleration. [9].

As a summary, there are several ways of implementing MEMS accelerometers. Capacitive type accelerometers have significant advantages compared to other types of accelerometers. Firstly, they offer simple structure and therefore, low fabrication cost. Moreover, they have the features of high sensitivity, high reliability and low power consumption along with low noise, low nonlinearity, high immunity to temperature changes, and low bias drift. Due to these advantages, capacitive accelerometers are very commonly used in consumer applications [10].

1.2 Classification of Accelerometers by Readout Circuit

Readout circuits can mainly be classified into two categories, which are open loop and closed loop electronics.

1.2.1 Open Loop Electronics

Open loop electronics is a simple way of converting the capacitance between accelerometer electrodes and proof mass into electrical voltage. As name suggests, complete system is open loop, which means there is no feedback mechanism in the system. Open loop system requires a basic and simple electronic circuit design, which is the main advantage of it and since the electronic circuitry is simple, it has also low readout circuit noise.

However, there are some major drawbacks of this type of interface circuit. Firstly, it has highly non-linear input-output characteristic due to large deflection of proof mass. Secondly, dynamic range of open loop systems is very low because proof mass and electrode fingers can stick to each other easily at high acceleration input levels and also high acceleration input levels result in high nonlinearity. Therefore, dynamic range of the

open loop systems is limited. Thirdly, the bandwidth of open loop systems is restricted with the bandwidth of accelerometer. There is no way to change the bandwidth of the system. Lastly, open loop systems have high bias drift and temperature sensitivity due to large deflection of proof mass.

1.2.2 Closed Loop Electronics

In closed loop electronics, contrary to open loop electronics there is a feedback mechanism in the system. Electromechanical feedback force counteracting to external force is applied to accelerometer electrodes by the readout circuit in order to be able to minimize the proof mass displacement. Therefore, nonlinearity problem encountered in the open loop system is significantly reduced. Small proof mass displacement in closed loop systems also reduces the bias drift, temperature sensitivity and dependence on sensor parameters. Moreover, dynamic range of the system can be increased in a significant amount by using high feedback voltage. Furthermore, closed loop electronics provides an opportunity to change output bandwidth. On the other hand, closed loop systems have very complex readout circuit compared with open loop electronics and this complexity brings higher noise contribution. However, readout electronic noise can be suppressed with a careful design.

Closed loop electronics can also be divided into two sub-categories according to feedback type that is applied. These are analog and digital feedback types. In analog feedback electronics, acceleration input is converted into analog voltage and this voltage is given back to accelerometer electrodes as feedback. Analog feedback type electronics are much easier to design and implement compared with digital feedback type electronics. However, linearity of analog feedback electronics is not good enough due to non-linear relation between feedback voltage and force. Furthermore, analog feedback electronics give analog output and it should be converted into the digital domain with a high resolution ADC to be able to process acceleration data. The need for high resolution ADC increases the cost, size and complexity of external electronics.

Due to the drawbacks of analog feedback electronics mentioned above, digital feedback electronics are much more preferable. In digital feedback electronics, acceleration input is converted into digital output and this digital output is given back to accelerometer electrodes as feedback. In general, a sigma-delta modulator inside readout electronics performs digitization operation. Digitization of feedback significantly improves the linearity of the system by linearizing the relation between feedback voltage and force. It is explained in detail in Section 3.2. Since digital feedback electronics has digital output, it does not require any usage of ADC in external electronics, which simplifies the design of PCB. The system that is the combination of accelerometer and digital feedback electronics including sigma-delta modulator is called as electro-mechanical sigma-delta modulator [11].

1.3 Accelerometer Readout Circuits at METU

At METU, first MEMS accelerometer study began in 2003 with silicon-on-insulator designs and designed accelerometers were fabricated by MemsCap Company. Then, MEMS accelerometers started to be fabricated in METU-MEMS [13]. With the fabrication process at METU-MEMS, there was a need for high performance readout circuits to be able to convert acceleration data into electrical domain. Such a readout circuit was designed by Reha Kepenek as part of his M.Sc. thesis [12].

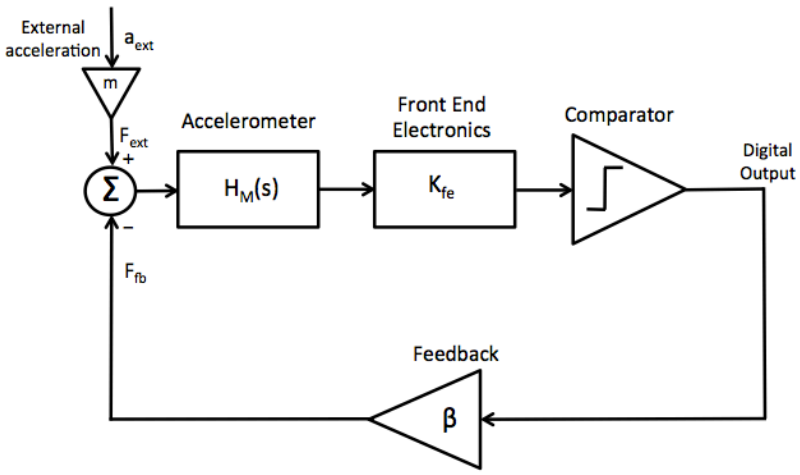

Figure 1.4: Block diagram of the closed loop system architecture used in [12].

In his work, a simple second order electro-mechanical sigma delta modulator is designed. Figure 1.4 shows the block diagram of the closed loop system architecture used in this work. Accelerometer, which in fact has a mechanical low-pass second order transfer function, is used as a loop filter for sigma-delta modulation. With this structure, it was achieved 153 μg√Hz noise level, 96 dB dynamic range with an accelerometer having < 5 μg√Hz mechanical noise level and readout circuit had power consumption of 16 mW. However, designed system had a problem with high noise level, dead zone problem (system does not respond to low level acceleration input) and high power consumption. High noise level was entirely dominated by quantization noise because accelerometer used as a loop filter had very low DC gain. Therefore, quantization noise was not shaped well by the accelerometer and determined the output noise level.

After this work, Uğur Sönmez designed a new readout circuit as part of his M.Sc. thesis [13]. In his work, he used an unconstrained fourth-order electro-mechanical sigma-delta modulator as readout circuitry, which is introduced by J. Raman [14]. Figure 1.5 shows the block diagram of the closed loop system architecture used in his work. The main difference between these two previous studies is that Uğur Sönmez added a 2nd order

electronic sigma-delta modulator to the system. High DC gain integrators in the sigma-delta modulator compensate the low gain of the accelerometer. As a result, quantization noise is suppressed very well in low-frequency band. Also, this structure eliminates the dead zone phenomena seen in the previous work. According to test results, he achieved 5.95μg√Hz noise level and 131.7 dB dynamic range with an accelerometer having 4.6 μg√Hz mechanical noise level and readout circuit had power consumption of 16.7 mW. It is apparent that he made a significant improvement in noise level and dynamic range of the system.

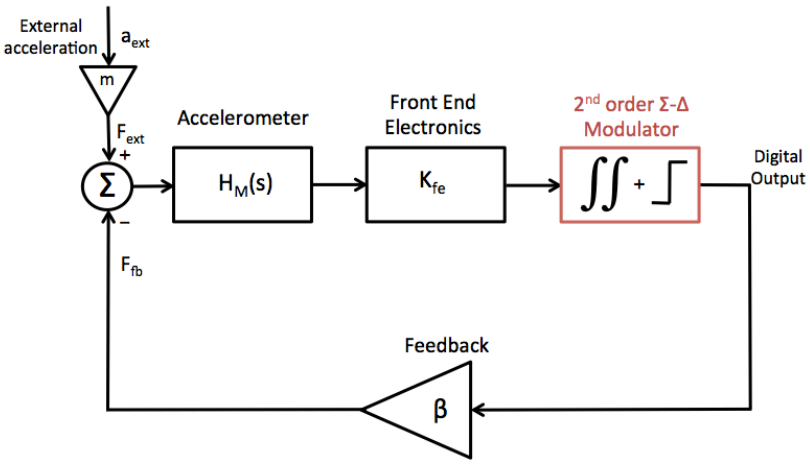

Figure 1.5: Block diagram of the closed loop system architecture used in [13].

1.4 Research Objectives and Thesis Organization

This research aims to have better performance than the electro-mechanical sigma-delta accelerometer system previously designed in METU [13]. In order to be able to have much better design, readout circuit should have the following features:

1. The primary objective of this thesis work is to produce low-power readout circuitry. Previous work [13] had a power demand of 16.7 mW. This work aims to have power consumption lower than 2 mW.
2. Open loop gain of the system should be increased to have better linearity and higher immunity to sensor parameter changes.
3. Readout circuit noise and sigma-delta quantization noise should be sufficiently suppressed that total output noise level is determined by Brownian noise of the accelerometer.
4. A linearized model of the complete system should be developed to predict the stability of the system and make system analyses easier.
5. The readout circuit is designed with many programmable features so that this readout can be used with various capacitive accelerometers with different

electrical and mechanical properties. The programmable features, such as the input reference capacitor selection, the biasing, the gain and the timing of the analog blocks in the readout can be configured and programmed through a serial programming interface with the help of an integrated digital controller circuit.

Organization of this thesis is as follows:

Chapter 2 explains the principles of sigma-delta modulation and basic concepts such as oversampling, noise shaping and demodulation. After giving the fundamental principles and concepts of sigma-delta modulation, its application on accelerometer systems, which are called as electro-mechanical sigma-delta modulators are explained.

Chapter 3 gives the architecture of the designed system in this work. Complete linearized model of the system is also developed in order to make analyses easier and predict system stability. Lastly, system level analysis is done and simulation results are given.

Chapter 4 tells about the implementation of the readout circuit design. It begins with the readout circuit architecture. Then, all the building blocks of the readout circuit will be explained in detail and top-level integration will be given.

Chapter 5 summarizes the works done in the scope of this thesis.

CHAPTER 2

PRINCIPLES OF SIGMA-DELTA MODULATION

This chapter presents the principles of sigma-delta modulation. Section 2.1 gives the basics of sigma-delta modulators. The concepts of oversampling, noise shaping and demodulation are explained. This section mainly focuses on electronic sigma-delta modulators. Section 2.2 mentions about electro-mechanical sigma-delta modulators and how accelerometer is adapted for sigma-delta modulation. Brief explanation about second order and high order systems is given.

2.1 Sigma-Delta Modulators

Sigma-delta modulation is a quite popular and an efficient way of obtaining high-resolution signals and it is generally used in low bandwidth analog to digital converter applications. In data converters, there is always a trade-off between resolution and signal bandwidth. This trade-off is in favor of resolution in sigma-delta data converters. In other words, resolution is increased at the cost of lowering signal bandwidth. Oversampling and noise shaping are two concepts that are used in sigma-delta modulators in order to be able to achieve high-resolution signals.

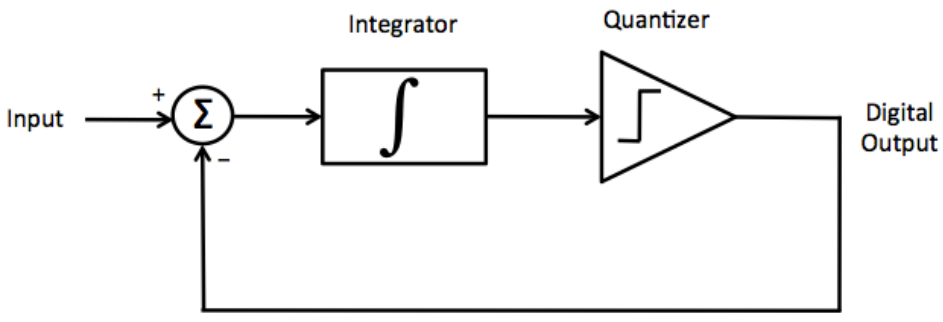

Figure 2.1: Basic block diagram of Σ-Δ modulator.

Figure 2.1 shows the basic block diagram of Σ-Δ modulator. It includes an integrator and a quantizer block. This type of Σ-Δ modulator is called as first-order Σ-Δ modulator**.** Σ-Δ modulators are named as according to the number of integrators they include. For instance, if a Σ-Δ modulator has two integrators, it is called as second-order Σ-Δ modulator.

What Σ-Δ modulator mainly does that it converts input signal into high frequency (oversampled) digital output signal whose average is proportional with the input. Quantizer is a non-linear block as its nature. It takes input, compares the input with a reference voltage and converts the difference voltage to digital output. In general, one-bit quantizers are preferred in Σ-Δ modulators since they have simple implementation and have well-defined two level outputs.

Analysis of Σ-Δ modulators are quite difficult due to including a non-linear element, quantizer. However, quantizer can be represented as an additive noise source as in Figure 2.2.

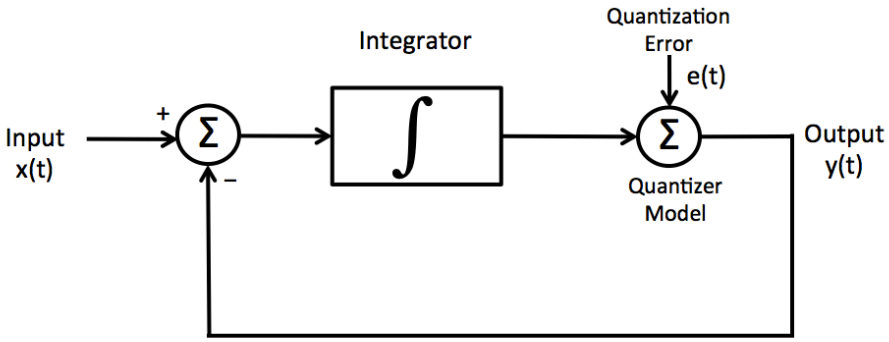

Figure 2.2: Basic block diagram of a Σ-Δ modulator with a quantizer model.

Equation 2.1.1 expresses the quantization error introduced into the system [15].

$$e_{rms}^2 = \frac{1}{\Delta}\int_{-\Delta/2}^{\Delta/2} e^2\, de = \frac{\Delta^2}{12} \tag{2.1.1}$$

where Δ is the quantization step size. Notice that quantization error is actually a white noise source because it has equal probability to have a value between –Δ/ 2 and Δ/ 2.

2.1.1 Oversampling

Sampling a signal with a sampling frequency with a much higher value than the twice of the signal bandwidth (Nyquist frequency) is called as oversampling. Σ-Δ ADCs are also named as oversampling ADCs due to its higher sampling rate compared with signal bandwidth. Oversampling increases the resolution and decreases the in-band noise. The ratio of sampling frequency and signal bandwidth is defined as oversampling ratio that is stated in Equation 2.1.1.1.

$$M = \frac{f_s}{2f_B} \tag{2.1.1.1}$$

where f_s is the sampling frequency and f_B is the signal bandwidth.

Power spectral density of quantization noise distributed uniformly over the sampling frequency can be expressed as follows.

$$N_e(f) = \frac{e_{rms}^2}{f_s} = \frac{\Delta^2}{12.f_s} \tag{2.1.1.2}$$

In-band quantization noise is, therefore, can be written as in Equation 2.1.1.3.

$$e_{B,rms}^2 = \int_{-f_B}^{f_B} N_e(f)\ df = \frac{\Delta^2.2f_B}{12.f_s} = \frac{\Delta^2}{12.M} \tag{2.1.1.3}$$

where $e^2_{B,rms}$ is in-band rms noise power, and f_B is signal bandwidth.

Figure 2.3 illustrates the effect of oversampling on quantization noise with a graphical interpretation to understand more clearly.

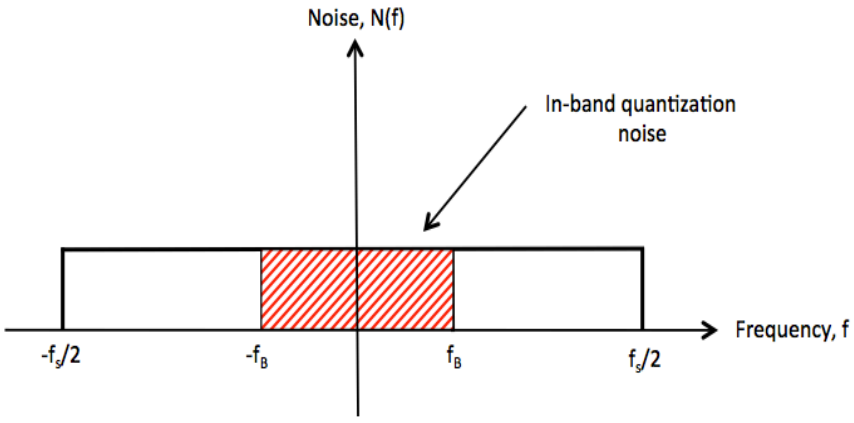

Figure 2.3: Effect of oversampling on quantization noise.

It is obvious that oversampling ratio is an important parameter to decrease quantization noise. Doubling the oversampling ratio leads to 3 dB decrease in in-band quantization noise and 0.5 bit increase in resolution.

2.1.2 Noise Shaping

Noise shaping as name suggests shapes the quantization noise by pushing most of in-band noise to high frequency band. Integrators in Σ-Δ modulators are used for noise shaping purpose.

Integrator in Figure 2.2 has a discrete transfer function of $H(z) = 1/(z-1)$. Noise transfer function is defined as the ratio of output voltage and quantization noise as Equation 2.1.2.1 states.

$$NTF = \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)} = 1 - z^{-1} \tag{2.1.2.1}$$

where Y(z) is the output and E(z) is the quantization noise. By inserting $z = e^{jwT}$ into the equation above, Equation 2.1.2.2 can be derived [11].

$$NTF(jw) = 2\sin(wT/2)\,.\,e^{-j(wT-\pi)/2} \tag{2.1.2.2}$$

Magnitude of noise transfer function can be written as in the following way.

$$|NTF(jw)| = 2|\sin(wT/2)| = 2|\sin(\pi f/f_s)| \tag{2.1.2.3}$$

Equation 2.1.2.4 expresses the output noise power spectral density.

$$N_y(f) = |NTF(jw)|^2 . N_e(f) \tag{2.1.2.4}$$

By replacing $|NTF(jw)|^2$ with its equivalent expression, Equation 2.1.2.5 is easily obtained.

$$N_y(f) = 4|\sin(\pi f/f_s)|^2\,.N_e(f) \tag{2.1.2.5}$$

It is clear from Equation 2.1.2.5 that quantization noise is shaped by a high pass transfer function. Figure 2.4 illustrates the noise-shaping characteristic of this first-order modulator [16].

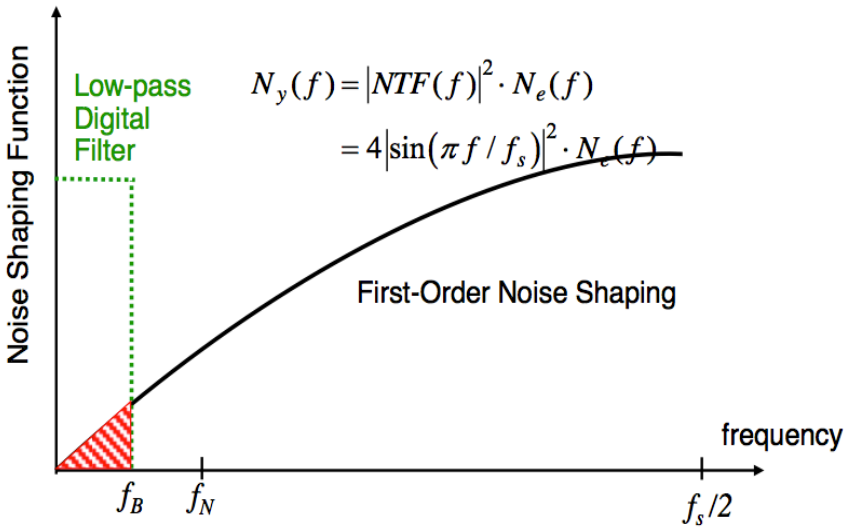

Figure 2.4: First-order noise shaping graph [16].

Total shaped quantization noise at the output can be calculated by integrating the output noise power spectral density over bandwidth. The result is shown in Equation 2.1.2.6 [16].

$$e_{B,rms}^2 = \int_{-B}^{B} N_y(f)\, df = \int_{-f_s/2M}^{f_s/2M} \frac{\Delta^2}{12.f_s}.4|\sin(\pi f/f_s)|^2\, df$$

$$e_{B,rms}^2 \cong \frac{\pi^2.\Delta^2}{3.M^3.12} \qquad (2.1.2.6)$$

Equation 2.1.2.6 points out that noise shaping has a significant impact on quantization noise. Doubling oversampling ratio leads to 9 dB decrease in in-band quantization noise and 1.5 bit increase in resolution of first order Σ-Δ modulators.

Equation 2.1.2.6 can be extended to more general form including the order of Σ-Δ modulator [17].

$$e_{B,rms}^2 = e_{rms}^2 \cdot \frac{\pi^{2N}}{M^{2N+1}.(2N+1)} \qquad (2.1.2.7)$$

where $e^2_{B,rms}$ is total shaped quantization noise at the output, e^2_{rms} is quantization noise introduced into the system as shown in Equation 2.1.1, N is the modulator order and M is the oversampling ratio. Equation 2.1.2.7 stresses the fact that

increasing the modulator order dramatically degrades the in-band quantization noise.

Figure 2.5 shows the effect of Σ-Δ modulator order on quantization noise along with oversampling ratio [12].

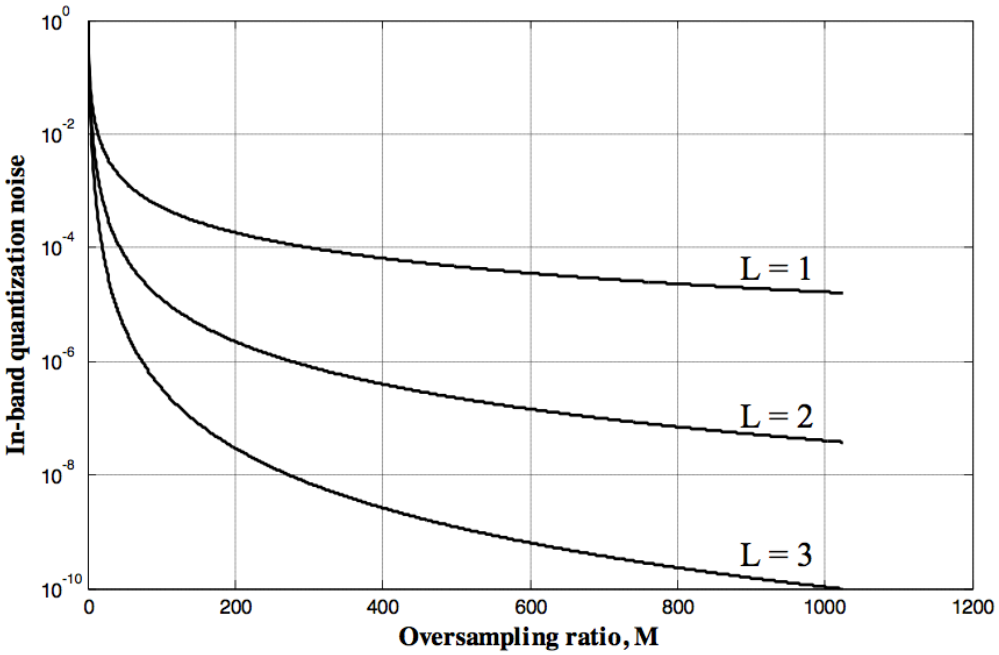

Figure 2.5: Effect of the Σ-Δ modulator order and oversampling ratio on in-band quantization noise [12].

2.1.3 Demodulation

Σ-Δ modulators have 1-bit digital bit stream that has to be processed through filtering to obtain meaningful output. Digital bit stream includes all frequency components from 0 Hz to sampling frequency (f_s). Therefore, it includes the input at low-frequency band along with the quantization noise distributed all over the sampling frequency band. In previous section, it is explained that quantization noise is shaped and most of the noise is pushed out to high frequency band. In order to be able to extract input signal, a low-pass filter is needed. Hence, excessive noise components are thrown out.

Low-pass filter only decreases the bandwidth and it does not change the sampling rate. Sampling rate can be decreased down to the Nyquist rate without any input information loss. Decreasing sampling rate is called as decimation. A decimation stage is used after low-pass filtration. It removes the unnecessary data and data processing, therefore, will be much easier.

Figure 2.6 shows the demodulation block diagram and Figure 2.7 shows the graphical representation of digital low-pass sinc filter [10].

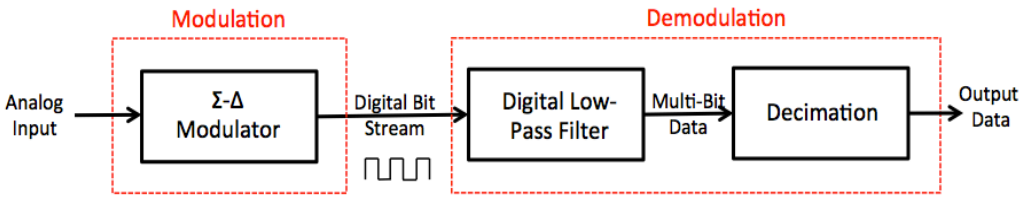

Figure 2.6: Demodulation process.

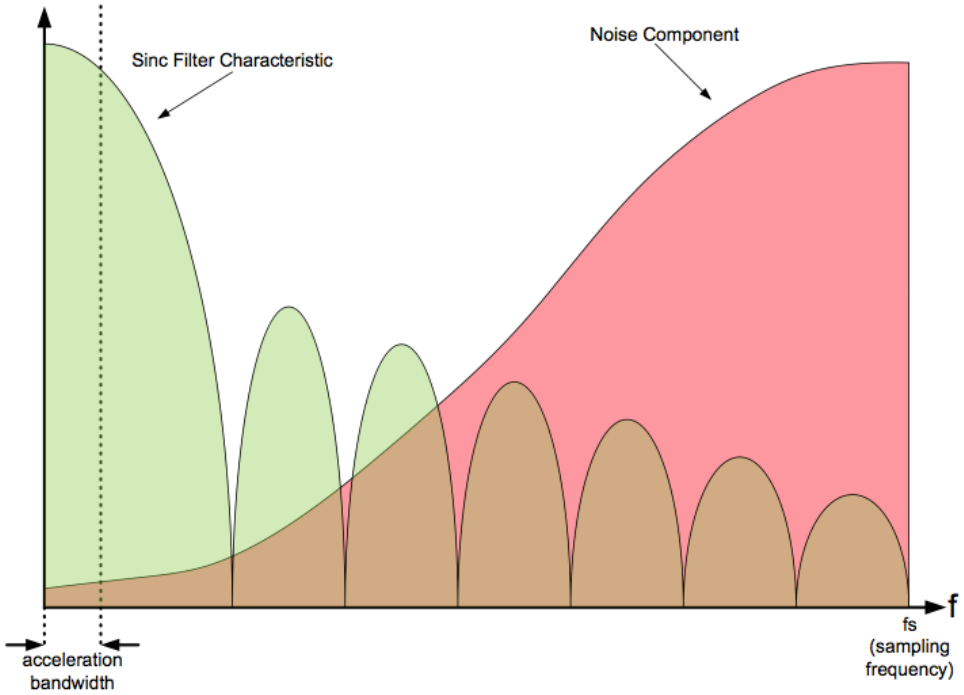

Figure 2.7: Digital low-pass sinc filter [10].

2.2 Electro-mechanical Sigma-Delta Modulators

In Section 2.1, it is discussed about the fundamental concepts of electronic sigma-delta modulators and it is expressed that sigma-delta modulators are used for low-frequency applications because input signal is oversampled in order to be able to obtain high-resolution signal at the output. It is also shown that sigma-delta modulators include integrators or low-pass filtering elements to shape the quantization noise and therefore, it is suppressed in low-frequency band.

Sigma-delta modulation is well suited for any capacitive sensing MEMS accelerometers since input (acceleration) bandwidth is, in general, limited to a few kHz and accelerometer can be used as a low-pass filtering element for sigma-delta modulation.

2.2.1 Capacitive MEMS Accelerometer

In this section, capacitive MEMS accelerometer that is used in this thesis will be explained. Capacitive accelerometers sense the inertial acceleration applied on it and reacts to this acceleration by changing its position. Position change results in capacitance change between accelerometer and electrodes. Therefore, this type of accelerometers is referred as capacitive accelerometers.

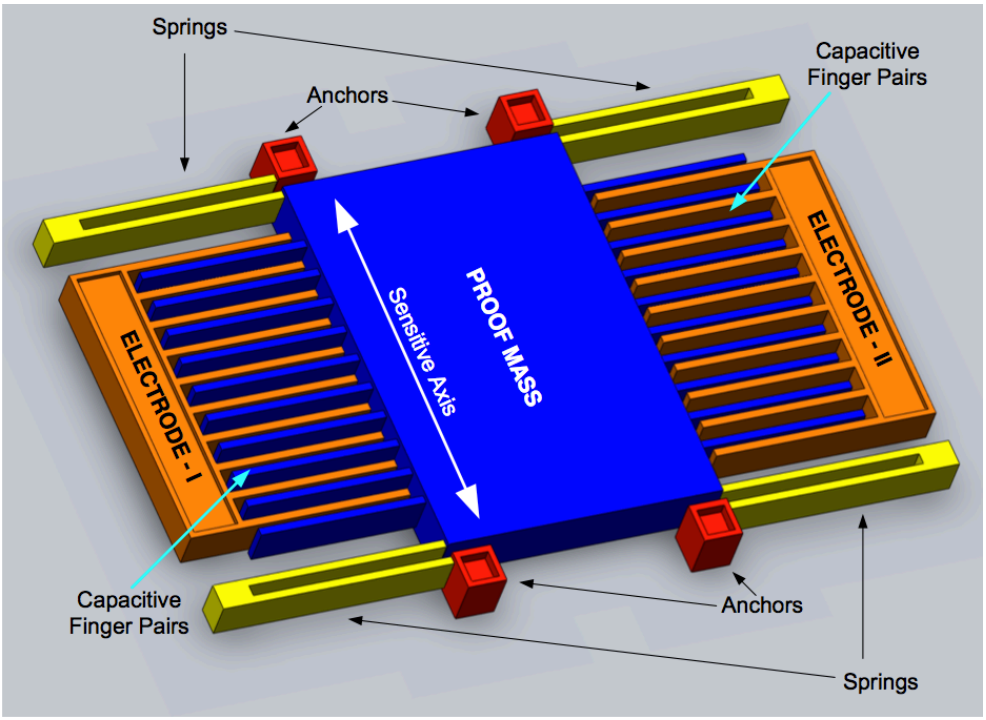

Figure 2.8: Model of a capacitive MEMS accelerometer [10].

Figure 2.8 illustrates the model of capacitive MEMS accelerometer that is used in this thesis [10]. Moving or sensing element of an accelerometer is called as proof mass. Proof mass has a finger type structure that increases the capacitive sensitivity of accelerometer. Deflecting of proof mass from its rest position forms capacitive difference between proof mass fingers and electrode fingers as seen in Figure 2.8.

Capacitive accelerometers can be modeled as a second-order mass spring damper system as in Equation 2.2.1.1 [18].

$$F = ma = m.\frac{d^2x}{dt} + \beta\frac{dx}{dt} + Kx \tag{2.2.1.1}$$

where F is the applied force, m is the proof mass, a is the applied acceleration, β is the damping coefficient, K is the spring constant and x is the proof mass position deflection. Equation 2.2.1.2 gives the resulting transfer function between acceleration and position.

$$H_{acce}(s) = \frac{1}{s^2 + (\beta/m)s + K/m} \tag{2.2.1.2}$$

Equations 2.2.1.3 and 2.2.1.4 define the resonance frequency and quality factor of second-order accelerometer system.

$$w_{res} = \sqrt{\frac{K}{m}} \tag{2.2.1.3}$$

$$Q = \frac{\sqrt{K.m}}{\beta} \tag{2.2.1.4}$$

The capacitance of single capacitive finger pair can be written as in Equation 2.2.1.5.

$$C = \frac{\varepsilon_0 \,.A}{d - x} \tag{2.2.1.5}$$

where ε_0 is the permittivity of the air, A is the capacitive area of the finger, d is the gap between proof mass and electrode fingers and x is the amount of proof mass deflection.

Equation 2.2.1.6 gives the total capacitance between one electrode and proof mass fingers.

$$C_{1,2} = \frac{N \,.\varepsilon_0 \,.A}{d_1 \mp x} + \frac{(N-1).\varepsilon_0 \,.A}{d_2 \pm x} \tag{2.2.1.6}$$

where C_1 is total capacitance formed between proof mass and electrode-1, C_2 is total capacitance formed between proof mass and electrode-2, N is the finger number of each electrode, d_1 is finger gap distance and d_2 is finger anti-gap distance. Smaller distance between fingers is called as gap distance and larger one is called as anti-gap distance.

C_1 and C_2 are equal to each other when proof mass is at its rest position. (No acceleration applied). However, when proof mass is deflected into positive x-direction, C_1 decreases and C_2 increases, and vice versa. This capacitance difference between C_1 and C_2 is then sensed with the electronic circuitry.

Table 2.1 gives the parameters of the MEMS accelerometer used in this thesis [10].

Table 2.1: Parameters of the MEMS accelerometer used in this thesis [10].

Parameter	Value
m	263.9 ug
K	56.3 N/m
β	8.5 N.s/m
Number of fingers	351
d_1	2 um
d_2	7 um
h	35 um
L	140 um
w_{res}	14.58 krad/s
Q	0.455
C_{rest}	9.5 pF

2.2.2 2nd Order Electro-Mechanical Sigma-Delta Modulators

In previous section, it is explained that accelerometer has a second-order mechanical low-pass filter characteristic. Hence, it is possible to use accelerometer as a loop filter for sigma-delta modulation. Such systems are called as 2nd order electro-mechanical sigma-delta modulators. In the literature, there are so many reported studies making use of 2nd order EM Σ-Δ modulators. Figure 2.9 illustrates the block diagram of 2nd order EM Σ-Δ modulator. As it is shown in the figure that acceleration is input to the system and it is detected by the accelerometer. Accelerometer reacts to this input by moving its proof mass position. Position change is then sensed by readout electronics and converted to electrical potential difference. Comparator block compares this potential difference with a reference voltage and gives output. According to the digital output value, feedback force is applied to the electrodes of the accelerometer to keep proof mass stationary.

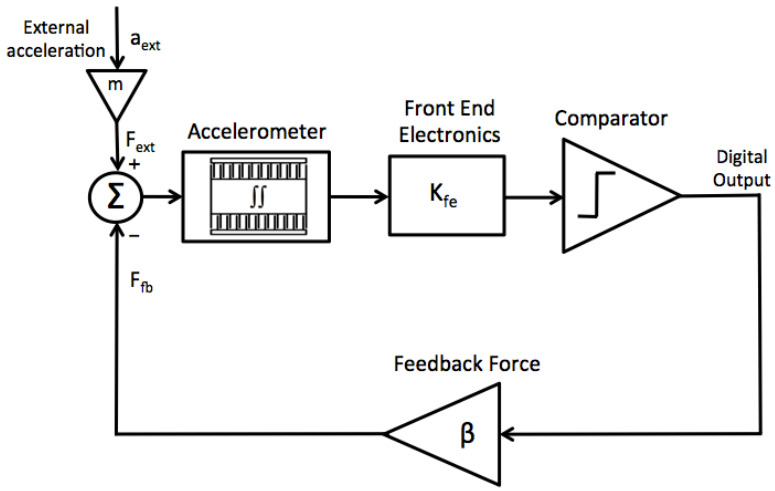

Figure 2.9: Block diagram of a 2nd order electro-mechanical sigma-delta modulator.

Quantization noise of 2nd order EM Σ-Δ modulators is shaped by the accelerometer transfer function. However, accelerometer is a mechanical low-pass filter with very low DC gain. Therefore, quantization noise cannot be shaped and suppressed well by low DC gain accelerometer, which will result in high quantization noise at the output. As a solution to this problem, an accelerometer that shows a good low-pass filter characteristic can be designed. In order to do this, mass of the accelerometer should be increased very much and spring constant should be extremely small. Fabrication of such an accelerometer is very difficult and costs very much. Size of this accelerometer would also be too big. Hence, it is not a good idea to change accelerometer parameters for obtaining low quantization noise. To resolve this problem, a high order EM Σ-Δ modulator should be used instead of 2nd order EM Σ-Δ modulator.

2.2.3 High Order Electro-Mechanical Sigma-Delta Modulators

High order EM Σ-Δ modulators are formed with additional electronic integrators that are cascaded to second order mechanical sensing element. As a naming convention, if one integrator stage is cascaded to the accelerometer, it is called as third order EM Σ-Δ modulator. Two order already comes from the accelerometer. Figure 2.10 shows the basic block diagram of a high order Σ-Δ modulator. In the figure, an Nth order electronic sigma-delta modulator is added to the system and complete system is called as (N+2)th order EM Σ-Δ modulator.

Additional electronic integrators along with the accelerometer form the loop filter. Electronic integrators compensate the low gain of the accelerometer and therefore, quantization noise can be suppressed at low frequencies. The number of additional integrators can be specified according to desired quantization noise level. For instance,

assume that quantization noise is the most dominant noise source of a second-order system. It is very reasonable to increase the order of system until quantization noise does not make so much contribution to output noise level compared with other noise sources. After that level, there is no meaning to add more integrators to the system. In contrast, stability of the system can suffer with additional integrators. However, system stability can be checked with the linearized model of the system explained in Chapter 3 and non-linear model simulations.

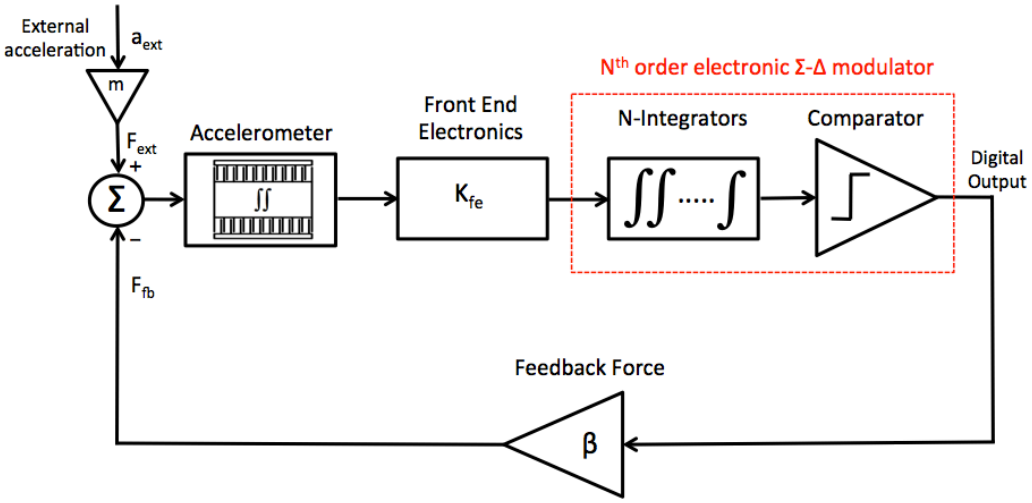

Figure 2.10: Block diagram of a high order electro-mechanical sigma-delta modulator.

CHAPTER 3

DESIGN AND ANALYSIS OF ELECTRO-MECHANICAL SIGMA-DELTA ACCELEROMETER SYSTEM

This chapter presents the design and analysis of electro-mechanical sigma-delta accelerometer system that is implemented in this thesis work. It begins with introduction section. In this section, it is briefly talked about the system architecture and advantages of the proposed structure. Section 3.2 gives the linearized model of the EM Σ-Δ accelerometer system. In Section 3.3, analysis and simulation results of the designed system are given.

3.1 Introduction

In previous chapter, it is talked about that second order EM Σ-Δ modulators depend strongly upon the accelerometer filter characteristic for quantization noise suppression. However, designed accelerometers have very low DC gain and do not exhibit good low-pass filtering characteristic. It is mentioned that accelerometers should have extremely large mass and very small spring constant to be able to obtain good filter characteristic, which results in expensive and big size systems. High order systems are offered to eliminate this problem. Additional integrators cascaded to the accelerometer help obtaining better low-pass filter characteristic and decrease the dependence on accelerometer parameters. Hence, high order systems relax the design of MEMS accelerometer.

In the literature, there are so many reported high order EM Σ-Δ modulator studies [14] [19-22]. All of these studies take advantage of improved noise shaping of high order systems. However, most of them lacks of strong system open loop gain. High noise performance can still be acquired with these systems. Nevertheless, change in accelerometer parameters because of variation in environment conditions does not allow obtaining same results. These systems cannot be called as robust systems. It is not

desirable to get different results with different environment conditions. Hence, robustness is an important parameter in accelerometer systems.

Figure 3.1 shows the block diagram of electro-mechanical sigma-delta accelerometer system implemented in this thesis work. System architecture employs a PI controller differing from the high order systems in the literature. Basically, PI controller makes the open loop gain of the system very high. Therefore, it lets us to design a robust system. High open loop gain also provides higher dynamic range, better linearity and bias instability due to very small deflection of proof mass from its rest position.

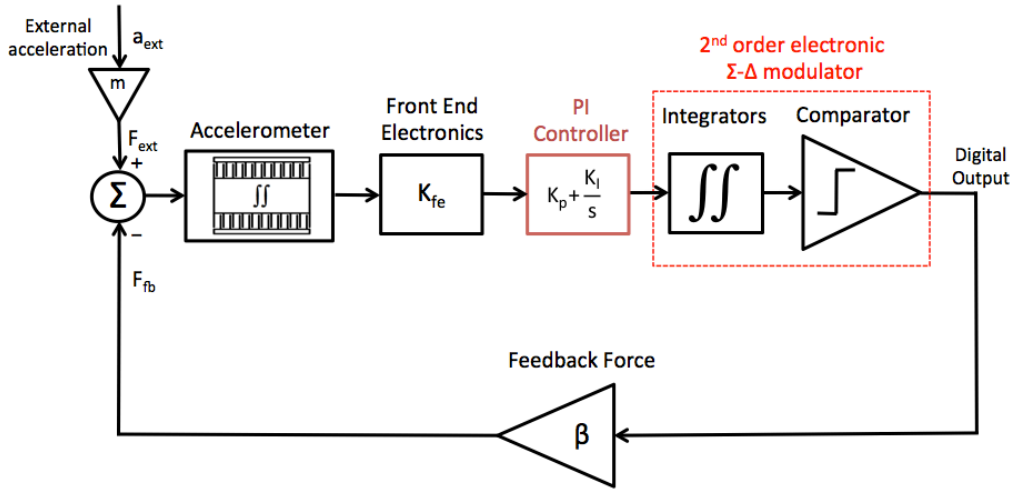

Figure 3.1: Block diagram of electro-mechanical sigma-delta accelerometer system implemented in this thesis work.

In this chapter, a linearized model of the complete system is also constituted, which makes system design and analysis much simpler. Especially stability of the system can easily be analyzed and estimated correctly with this model. Previous works on the stability of electro-mechanical sigma delta modulator system depends on either non-linear model simulations in environments such as MATLAB Simulink or complex mathematical analyses that are difficult to apply. Linearized model given in this chapter provides an opportunity to designers to know stability limit and margin of the system and determine the design according to this information.

One of the main aims of this thesis is to design a low-power readout circuit. Spring-softening effect that will also be described in this chapter allows designers to design low-power circuits. Spring-softening effect helps suppressing the readout circuit noise and therefore, current of the readout can be decreased without degrading the noise performance of the system.

3.2 Linearized Model of Electro-mechanical Σ-Δ Accelerometer System

Sigma-delta modulation is quite popular technique that is used in closed loop accelerometer systems. There are some important reasons using Σ-Δ modulation. These reasons can be written as follows.

1. Electrostatic feedback force has a non-linear characteristic. Σ-Δ modulation linearizes the electrostatic feedback force.
2. Σ-Δ modulation digitizes the output of the system. Accelerometer data can be extracted easily by using a simple digital low-pass filter. In analog output case, there will be a need to use an external ADC to digitize the output. Therefore, Σ-Δ modulator simplifies the external electronic.
3. Σ-Δ modulation, as its nature, introduces very low noise contribution to the system due to high oversampling and noise shaping.

In this section, it will be described in detail how Σ-Δ modulation linearized the electrostatic force.

3.2.1 Linearization of Electrostatic Feedback Force

To have a deeper understanding of the effect of Σ-Δ modulator on linearization of electrostatic feedback force, we need to look at the feedback network of the accelerometer system. Voltage to force has a non-linear relation in capacitive type MEMS accelerometers. This relation is expressed as:

$$F_{fb} = \frac{1}{2} \cdot \frac{dC}{dX} \cdot V^2 \tag{3.2.1.1}$$

where, F_{fb} is the electromechanical feedback force, dC/dX is the capacitance variation with respect to displacement and V is the feedback voltage.

Assume that Σ-Δ modulator is taken out of the system in Figure 3.1. In that case, the complete system will turn into the system as in Figure 3.2. This is actually a closed loop system with analog feedback. Assume also that loop gain of the system is sufficiently large enough that feedback force counterbalances the external force. Equation 3.2.1.2 shows the relation between external force and feedback force.

$$F_{ext} = F_{fb} = m \, . \, a_{ext} \tag{3.2.1.2}$$

In that case, the feedback voltage, which is also the output of the system, is proportional to the square root of the applied acceleration. It is expressed in Equation 3.2.1.3 that clearly points out that analog feedback systems suffer from high nonlinearity.

$$V_{out} = \sqrt{\frac{2 \,.\, m \,.\, a_{ext}}{dC/dX}} \qquad (3.2.1.3)$$

To solve nonlinearity problem there should be a nonlinear block which functions to linearize the feedback. Two major modulation techniques can be used in the feedback path for linearization, which are pulse density modulation (PDM) and pulse width modulation (PWM). In PDM, which is nothing but a Σ-Δ modulation, input voltage is converted into the high frequency digital pulses whose density corresponds to the amplitude of the input voltage. In PWM, input voltage is converted into the high frequency digital pulses whose width corresponds to the amplitude of the input voltage.

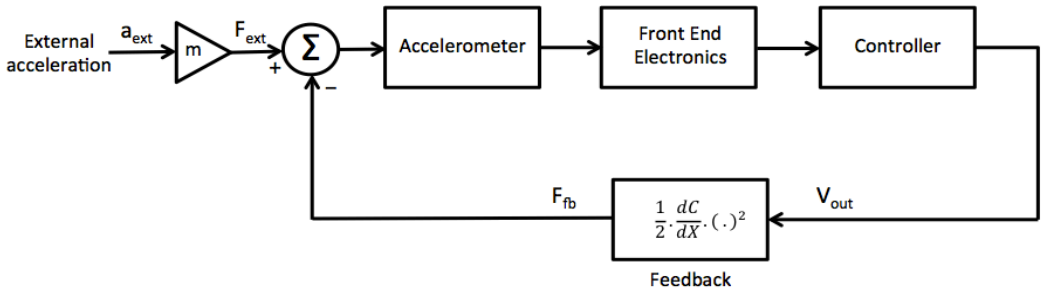

Figure 3.2: System block diagram of closed loop system with analog feedback.

Both of the modulators have very straightforward circuit implementation. However, due to finite rising and falling times of pulses, especially at high frequencies, PWM has worse linearity when compared with PDM. In PDM, nonlinearity is not observed since rising and falling times occur at each pulse [18]. Therefore, PDM is more preferable than PWM because of better linearity.

As explained in Section 2.1.3, demodulation of Σ-Δ modulator can be realized with a low-pass filter and decimation stage. Since decimation stage is only for purpose of removing extra data, demodulation can only be represented with a low-pass filter. Low pass filter averages the digital bit stream and gives an output proportional to input of Σ-Δ modulator.

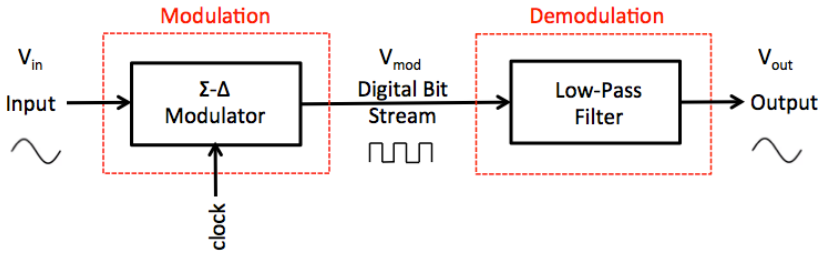

Figure 3.3: Σ-Δ modulation and demodulation process.

Figure 3.3 illustrates Σ-Δ modulation and demodulation process. Assuming that low-pass filter has a gain of unity at its pass band, input and output relation can be expressed as follows:

$$\langle V_{mod} \rangle = V_{out} = k_{mod} \, . V_{in} \tag{3.2.1.4}$$

where V_{in} is the input voltage, $<V_{mod}>$ is the average of modulator output composed of ***unity*** amplitude digital pulses, V_{out} is the output voltage and k_{mod} is the gain coefficient between input and output. If digital pulses have amplitude any other than unity, input-output relation should be scaled with that amplitude.

In Equation 3.2.1.4, input-output relation is just modeled with gain coefficient k_{mod}. Actually, this relation is correct under the assumption that modulator clock frequency is much higher than input bandwidth. If input bandwidth is close to the modulator clock frequency, then phase difference will be observed between input and output signals. However, by making sure that modulator clock frequency is high enough, modulator can be modeled as a gain block as in Equation 3.2.1.4 [23].

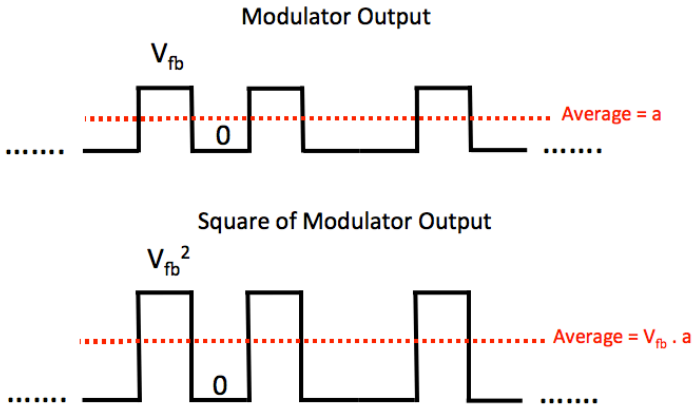

Figure 3.4: Effect of squaring Σ-Δ modulator output.

Figure 3.4 illustrates an example of Σ-Δ modulator output and square of this output. Modulator output has a pulse stream alternating between V_{fb} (constant feedback voltage) and 0V. If this output is squared, the same pulse stream is obtained, but alternating between V_{fb}^2 and 0V as shown in Figure 3.4. Let's say that average of the modulator output is *a*, which is a value between 0 and V_{fb}. Then, average of the squared modulator output will be $V_{fb}.a$. It is apparent that squared output is also linearly related with the input. Therefore, Σ-Δ modulator can be used for the purpose of linearization.

In figure 3.5, electromechanical feedback block, which has a square relation between input and output, is placed after Σ-Δ modulator.

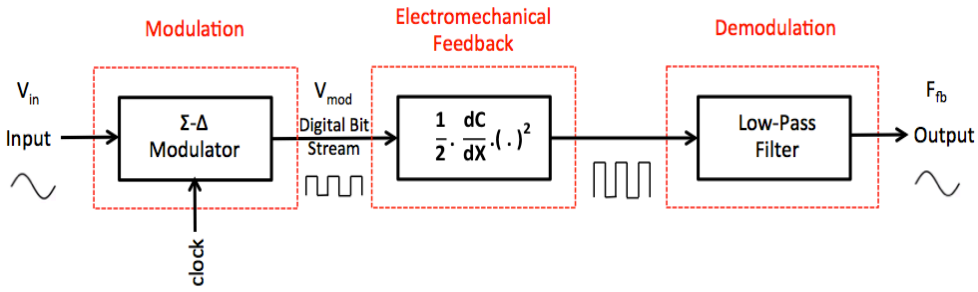

Figure 3.5: Σ-Δ modulation with electromechanical feedback.

Equation 3.2.1.5 and 3.2.1.6 shows the relation of average of modulator output and its square in Figure 3.5, respectively. Here, modulator output alternates between V_{fb} and 0V.

$$\langle V_{mod} \rangle = k_{mod} \,.V_{fb} \,.V_{in} \tag{3.2.1.5}$$

$$\langle V_{mod}^2 \rangle = k_{mod} \,.V_{fb}^2 \,.V_{in} \tag{3.2.1.6}$$

Equation 3.2.1.7 shows the relation between modulator input and output of low pass filter in Figure 3.5.

$$F_{fb} = \frac{1}{2}.\langle V_{mod}^2 \rangle \,.\frac{dC}{dX} \,.\, c \,.V_{in} = \frac{V_{fb}^2}{4} \,.k_{mod} \,.\frac{dC}{dX} \,.V_{in} \tag{3.2.1.7}$$

Since feedback force is not applied continuously, it is added a term, *c*, representing the ratio of feedback cycle duration to complete system cycle duration. It will be assumed as 0.5 (50% of complete cycle) in later calculations. In above equation, since k_{mod} and V_{fb}^2 are constant terms, square term in feedback is linearized with the help of Σ-Δ modulator.

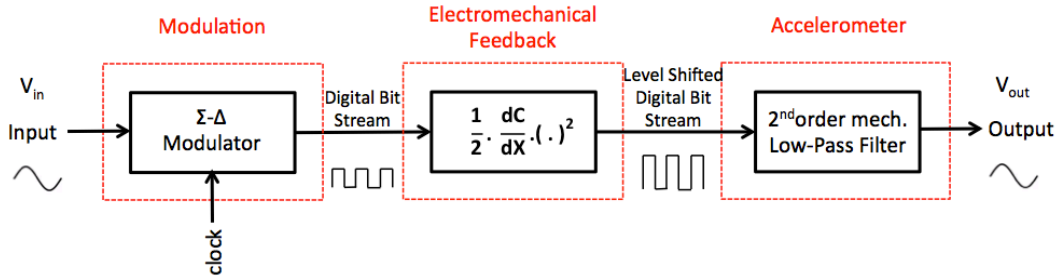

Figure 3.6: Σ-Δ modulation with electromechanical feedback and accelerometer.

Instead of using an external low-pass filter, accelerometer that is already a second order mechanical low-pass filter can be used. Figure 3.6 shows the feedback structure using accelerometer as a low-pass filter.

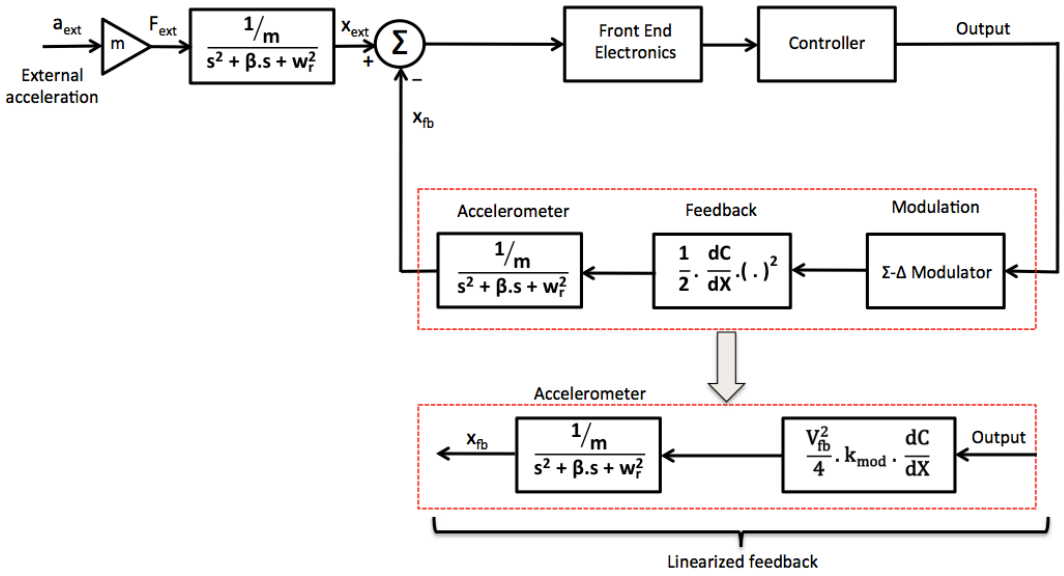

Figure 3.7: Electro-mechanical sigma-delta accelerometer system with linearized feedback [23].

Figure 3.7 illustrates the block diagram of electro-mechanical sigma-delta accelerometer systems with linearized feedback. Notice that accelerometer block in feed forward path is moved into the input and feedback paths. Therefore, linearized feedback structure in Figure 3.6 is obtained. Since the other blocks such as front-end and controller circuits are

linear-time-invariant (LTI) blocks, the analytical design and analysis of the complete system can easily be made using well-known LTI techniques.

3.2.2 Effect of Capacitance Sensitivity (dC/dX) on Feedback Force

In previous section, $\frac{dC}{dx}$ is accepted as if it is a constant term. In fact, in varying gap capacitive MEMS accelerometer, there is nonlinearity in capacitance sensitivity. In Section 2.2.1, capacitance expression is obtained in Equation 2.2.1.6. Capacitance sensitivity of the accelerometer is obtained by taking the derivative of capacitance with respect to displacement. Equation 3.2.1.1 shows capacitance sensitivity expression.

$$\frac{dC_{1,2}}{dx} = \pm\frac{N\,.\,\varepsilon_0\,.\,A}{(d_1 \mp x)^2} \mp \frac{(N-1).\,\varepsilon_0\,.\,A}{(d_2 \pm x)^2} \tag{3.2.1.1}$$

It is very clear from Equation 3.2.1.1 that sensitivity changes nonlinearly with proof mass position. However, since proof mass deflection is very small in closed loop systems, in general x = 0 is assumed for calculation of capacitance sensitivity. Therefore, Equation 3.2.1.1 turns out to following linear equation.

$$\frac{dC_{1,2}}{dx} \cong \pm\frac{N\,.\,\varepsilon_0\,.\,A}{d_1^2} \mp \frac{(N-1).\,\varepsilon_0\,.\,A}{d_2^2} \tag{3.2.1.2}$$

Equation 3.2.1.2 implies that sensitivity highly depends on gap spacing of the fingers. Smaller gap spacing results in higher sensitivity, which is an important result for designing the sensor.

Although zero proof mass displacement assumption seems very reasonable, it, in fact, does not characterize the actual relation very well. This assumption completely removes the displacement effect of capacitance sensitivity. Equation 3.2.1.1 can be extended using Taylor series expansion around x=0. The result is shown in Equation 3.2.1.3. First two terms of Taylor series expansion are included in the equation, which converges to actual relation very closely. First term is constant term and second term is the first order displacement term. Therefore, it is obtained a linear approximation of nonlinear displacement dependency of capacitance sensitivity.

$$\frac{dC_{1,2}}{dx} \cong \pm\frac{N.\,\varepsilon_0\,.\,A}{d_1^2} \mp \frac{(N-1).\,\varepsilon_0\,.\,A}{d_2^2} + 2.\left(\frac{N.\,\varepsilon_0\,.\,A}{d_1^3} + \frac{(N-1).\,\varepsilon_0.\,A}{d_2^3}\right).\,x \tag{3.2.1.3}$$

Although feedback force equations are, for simplicity, written for one electrode actuation in Section 3.2.1, both of the electrodes are actuated. While one of the electrodes is being actuated with the Σ-Δ modulator output, the other one is being actuated with the inverse

of the Σ-Δ modulator output. If the average of modulator output is denoted by $<V_{mod}>$, then the average of the inverse of modulator output can be written as follows:

$$\langle \overline{V}_{mod} \rangle = \frac{V_{fb}}{2} - \langle V_{mod} \rangle \tag{3.2.1.4}$$

Modulator output alternates between V_{fb} and 0V, and feedback cycle is assumed as 50% of the complete cycle. Square of the inverse output average is expressed as in Equation 3.2.1.5.

$$\langle \overline{V}^2_{mod} \rangle = \frac{V^2_{fb}}{2} - \langle V^2_{mod} \rangle \tag{3.2.1.5}$$

Total feedback force applied to proof mass can be written as follows;

$$F_{fb} = \frac{1}{2} . \left(\frac{dC_1}{dx} . \langle V^2_{mod} \rangle + \frac{dC_2}{dx} . \langle \overline{V}^2_{mod} \rangle \right) \tag{3.2.1.6}$$

Total feedback force is the combination of forces applied by two electrodes to the proof mass of sensor. If Equations 3.2.1.3 and 3.2.1.5 are combined with Equation 3.2.1.6, Equation 3.2.1.7 is obtained.

$$F_{fb} = \left(\langle V^2_{mod} \rangle - \frac{V^2_{fb}}{4} \right) . \left(\frac{N . \varepsilon_0 . A}{d_1^2} - \frac{(N-1) . \varepsilon_0 . A}{d_2^2} \right) + \frac{V^2_{fb}}{2} . \left(\frac{N . \varepsilon_0 . A}{d_1^3} + \frac{(N-1) . \varepsilon_0 . A}{d_2^3} \right) . x \tag{3.2.1.7}$$

Equation 3.2.1.7 shows the exact feedback force relation of varying gap capacitive accelerometers. As it is clear from the equation above that feedback force is composed of three components, which are sigma-delta modulator output, proof mass displacement and a constant term referred as force offset.

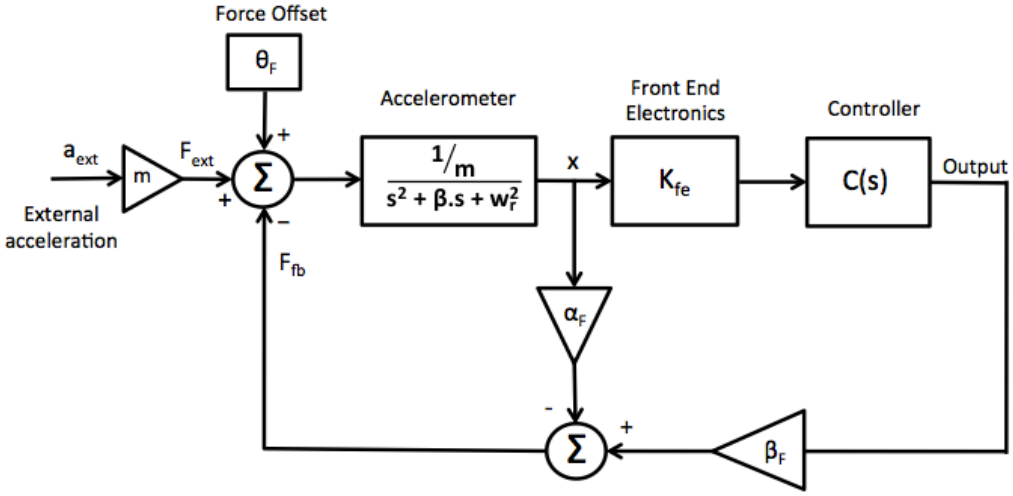

Figure 3.8: Complete linearized model of the electro-mechanical sigma-delta accelerometer systems.

Figure 3.8 illustrates the complete linearized model of the electro-mechanical sigma-delta accelerometer systems. Here, output to force relation is expressed with coefficient β_F. $\langle V^2_{mod} \rangle$ is replaced with its equivalent expression while defining β_F in Equation 3.2.1.8. Displacement dependency of feedback force is modeled as a displacement feedback with the coefficient α_F illustrated in Equation 3.2.1.9. Displacement dependency of feedback force is also called as spring softening effect [24]. α_F term has an effect of decreasing the spring constant of the accelerometer. That's why, it is referred as spring softening effect. Force offset is added to the input directly with the coefficient θ_F as shown in Equation 3.2.1.10.

$$\beta_F = \frac{V_{fb}^2}{2} . k_{mod} . \left(\frac{N . \varepsilon_0 . A}{d_1^2} - \frac{(N-1) . \varepsilon_0 . A}{d_2^2} \right) \tag{3.2.1.8}$$

$$\alpha_F = \frac{V_{fb}^2}{2} . \left(\frac{N . \varepsilon_0 . A}{d_1^3} + \frac{(N-1) . \varepsilon_0 . A}{d_2^3} \right) \tag{3.2.1.9}$$

$$\theta_F = \frac{V_{fb}^2}{4} . \left(\frac{N . \varepsilon_0 . A}{d_1^2} - \frac{(N-1) . \varepsilon_0 . A}{d_2^2} \right) \tag{3.2.1.10}$$

In the complete linearized model, there is an important point to stress to avoid confusing. For simplicity, accelerometer block is moved back to the feed-forward path again. It will not disrupt the feedback linearization. Feedback signal is still passing through accelerometer (mechanical low-pass filter).

3.3 Analysis and Simulations of the Electro-mechanical Sigma-Delta Accelerometer System

Up to now, it is explained how Σ-Δ modulator linearizes the electrostatic feedback force and how capacitance sensitivity affects the electrostatic feedback force. It is also obtained a linearized model of the complete system as shown in Figure 3.8, which allows the analysis of complete system very simple.

Open loop gain of the complete system in Figure 3.8 can be written as follows:

$$A_{OL}(s) = \frac{1/m}{s^2 + \beta s + w_r^2} . (K_{fe}. C(s). \beta_F - \alpha_F) \tag{3.3.1}$$

Here, C(s) term, controller action, is not defined yet. Let's assume that it is decided to use a proportional controller with gain coefficient K_p. However, in proportional controller systems, there is always a steady error at the output [25]. Steady state error in accelerometer systems leads not to keeping the proof mass stationary adequately. This causes to degradation in linearity and dynamic range and it also decreases the temperature immunity of the sensor, which results in poor bias instability. Steady state error can be decreased by increasing the open loop gain of the system (increasing K_p). Nevertheless, stability problem occurs in that case. There will be 180^0 phase delay before open loop gain of the system reaches 0dB gain, which means unstable system.

A proportional-integral (PI) controller will be used instead of proportional controller. Integral action will completely eliminate the steady state error and corresponding unwanted results. System stability is assured by adjusting the proportional and integral gain coefficients. Transfer function of the PI controller in s domain can be expressed as in Equation 3.3.2.

$$C(s) = K_p + \frac{K_I}{s} \tag{3.3.2}$$

By placing Equation 3.3.2 into Equation 3.3.1, open loop gain of the system with PI controller is obtained.

$$A_{OL}(s) = \frac{1/m \,.\, (K_{fe}. K_p. \beta_F - \alpha_F). \left(s + \frac{K_{fe}. K_I. \beta_F}{K_{fe}. K_p. \beta_F - \alpha_F}\right)}{s^3 + \beta s^2 + w_r^2 s} \tag{3.3.3}$$

Closed loop response of the system to the external force can be expressed in Equation 3.3.4.

$$A_{CL}(s) = \frac{1/m \,.\, K_{fe}.K_p.\left(s + \frac{K_I}{K_p}\right)}{s^3 + \beta s^2 + \left(w_r^2 - \frac{\alpha_F}{m} + \frac{K_{fe}.K_p.\beta_F}{m}\right)s + \frac{K_{fe}.K_I.\beta_F}{m}} \tag{3.3.4}$$

Front-end gain coefficient, K_{fe}, includes displacement to capacitance conversion ($K_{C/X}$) and voltage to capacitance conversion ($K_{V/C}$) as shown in the equation below.

$$K_{fe} = K_{C/X}.K_{V/C} \tag{3.3.5}$$

In Equations 3.3.3 and 3.3.4, some of the coefficients are selectable due to high programmability of the readout circuit. Voltage to capacitance conversion is derived in Equation 4.2.1.12 and it can be adjusted by changing integration capacitance (C_{int}) of the front-end circuit. C_{int} is a programmable capacitance adjusted between 0.5 pF and 15.5 pF with steps of 0.5 pF. Feedback coefficient, β_F, can be changed by Σ-Δ modulator gain coefficient, k_{mod} and feedback voltage. (See Equation 3.2.1.8). k_{mod} is altered with feedback capacitances of Σ-Δ modulator that are also programmable and can be adjusted between 100 fF and 1.5 pF. Proportional-integral controller coefficients, K_p and K_I are also selectable and they can be set to any desired value with proper combination of capacitance values. (See Section 4.3)

3.3.1 Stability Analysis and Simulation Results

Thanks to the obtained linearized model of the EM Σ-Δ accelerometer system, stability can be analyzed easily and it is checked using bode plot approach. For this, open loop transfer function obtained in Equation 3.3.3 is used. Along with stability analysis, transient response of the system to the step input is also obtained by using the closed loop transfer function in Equation 3.3.4.

To be able to check the accuracy of the linearized model analyses, system level simulations should also be performed. In SPICE-type simulators, simulation of electro-mechanical Σ-Δ modulators requires very long computational time and enormous amount of computer memory due to oversampling nature of Σ-Δ modulators. Instead of them, system level simulations are done in environments such as MATLAB-Simulink. Non-linear models of the designed blocks are simulated and results are obtained. Figure 3.9 shows the MATLAB-Simulink simulation setup of the complete system.

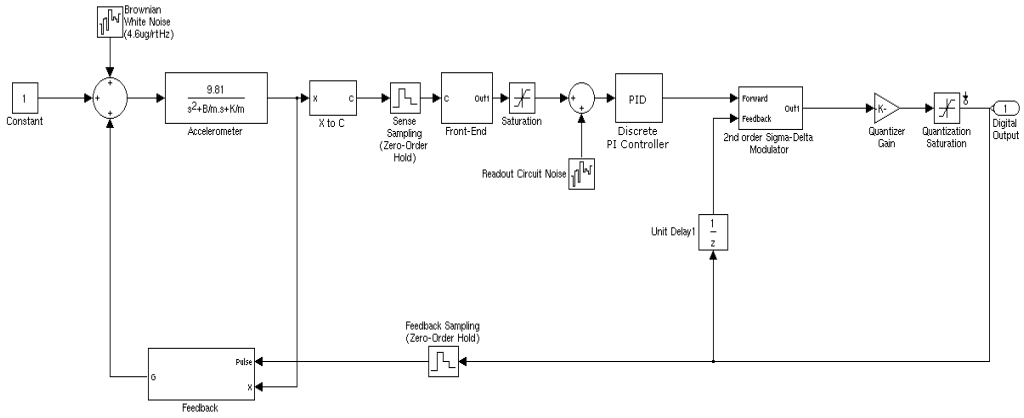

Figure 3.9: MATLAB-Simulink simulation setup of the complete system.

Figure 3.10 gives the Bode-plot analysis result of the designed system. Design parameters are selected such that phase margin is aimed to have around 60^0 for optimum settling time. Phase margin of the system is obtained as 62.2^0. Proportional and integral controller parameters are selected as K_p=1 and K_I =4500.

Figure 3.11 gives the step response of the system with using linearized model. As seen in the figure, settling time of the system is expected to be around 2 msec. Another point to stress here is that no steady state error is observed in the response of the system due to PI controller.

Figure 3.12 gives MATLAB-Simulink simulation result of the system to the step input using the model in Figure 3.9. Note that linearized model result perfectly matches with the simulation result of MATLAB-Simulink, which shows the accuracy of the obtained linearized model of EM Σ-Δ accelerometer system in Figure 3.8.

To see the effect of change in PI controller parameters and compare the linearized model result and MATLAB-Simulink simulation result in another case, K_I parameter is increased excessively to the value 25000. It is expected that increase in integrator parameter K_I degrades the system stability. The same simulations carried out with actual design parameters are done with new K_I value. The results are shown in Figures 3.13, 3.14 and 3.15. The phase margin is obtained as approximately 8^0, which is very close to the stability limit. System output is ringing as seen in Figures 3.14 and 3.15. Linearized model gives almost the same result again compared with the MATLAB-Simulink simulation result.

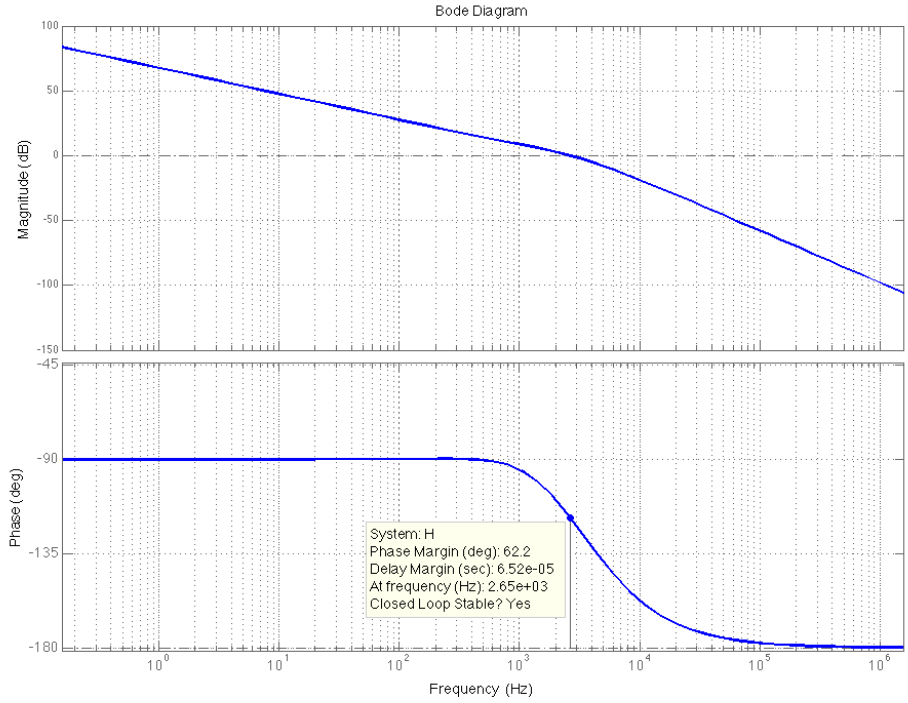

Figure 3.10: Bode plot analysis of the system (K_p=1 and K_I =4500).

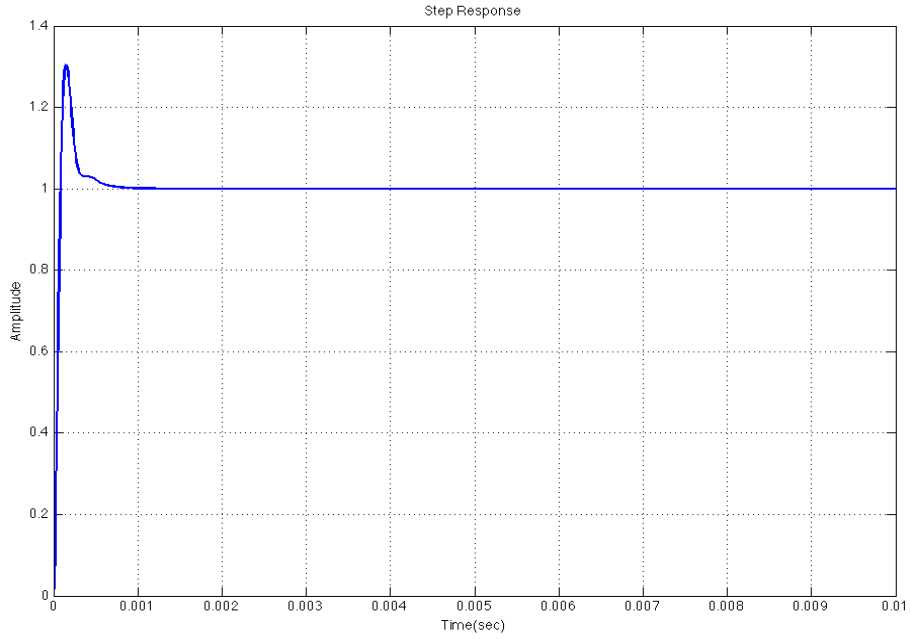

Figure 3.11: Step response of the system using linearized model (K_p=1 and K_I =4500).

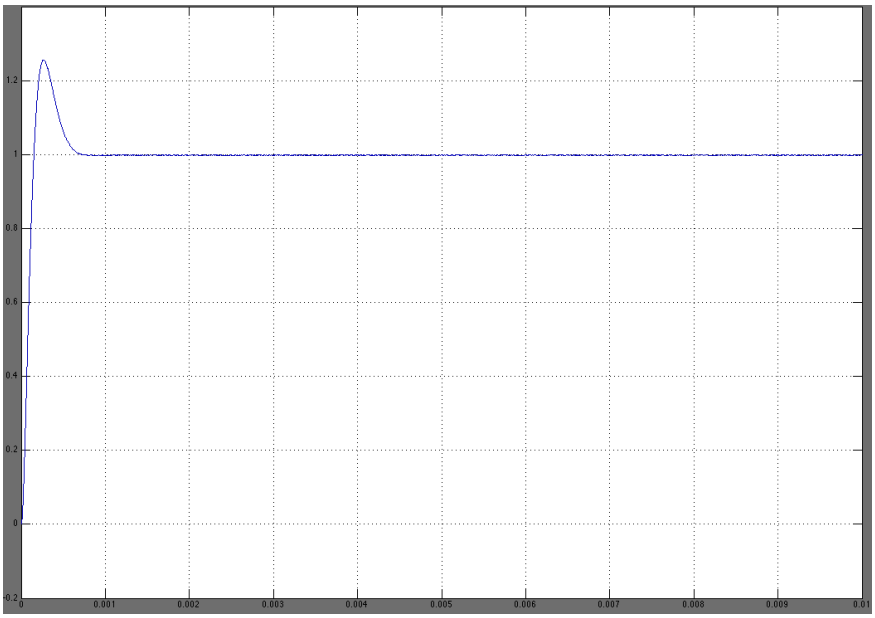

Figure 3.12: Step response of the system using MATLAB-Simulink model (K_p=1 and K_I =4500).

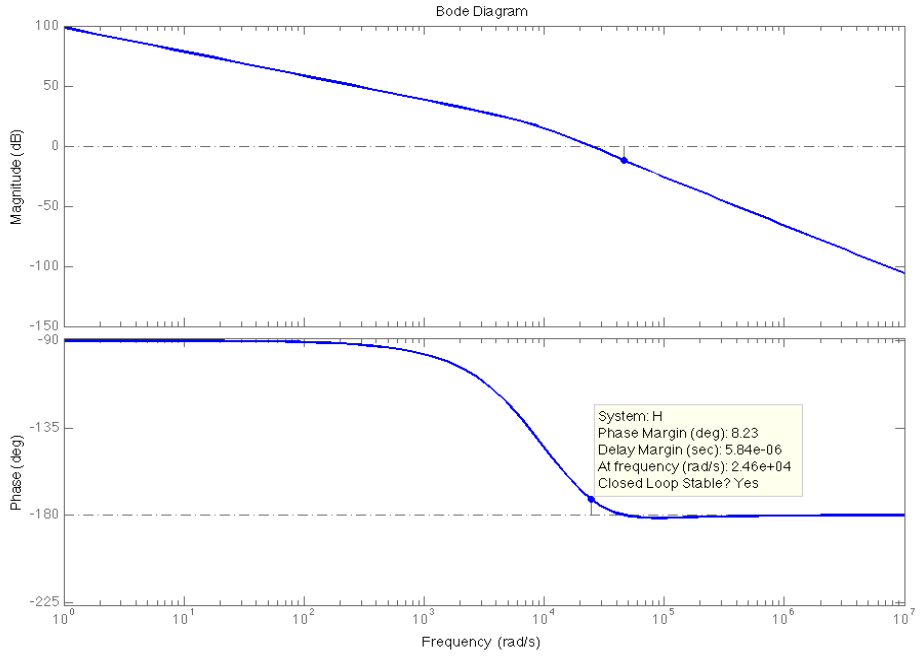

Figure 3.13: Bode plot analysis of the complete system (K_p=1 and K_I =25000).

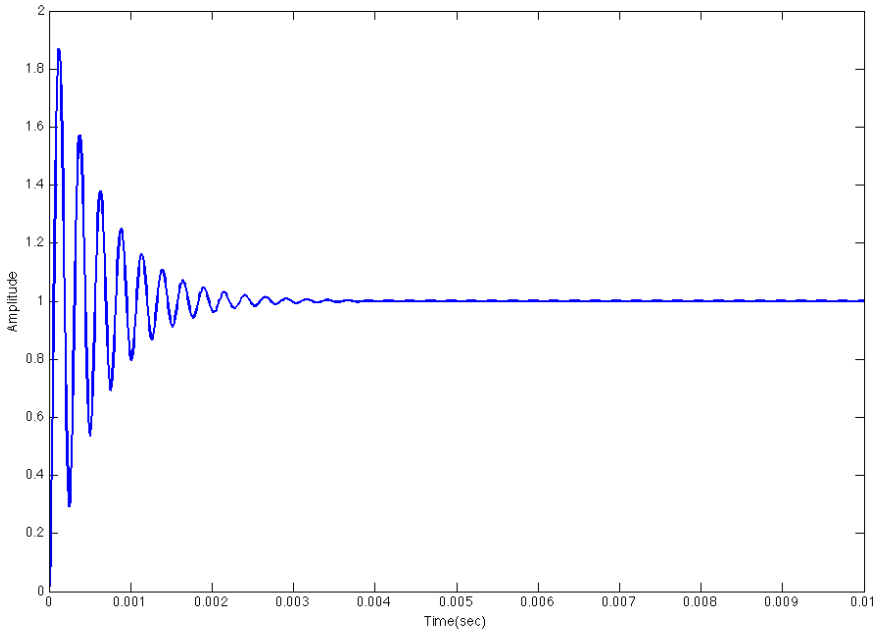

Figure 3.14: Step response of the system using linearized model (K_p=1 and K_I =25000).

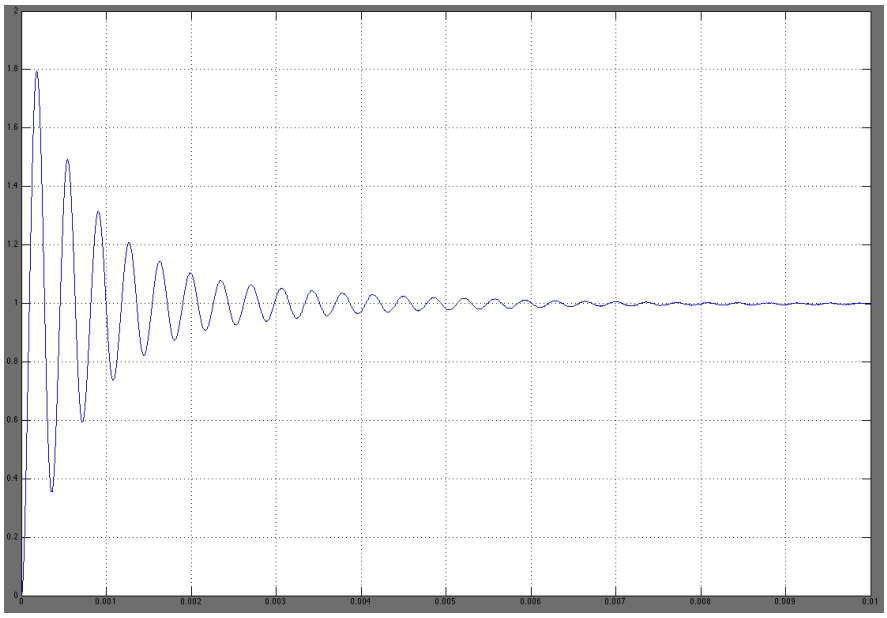

Figure 3.15: Step response of the system using MATLAB-Simulink model (K_p=1 and K_I =25000).

3.3.2 Noise Analysis and Simulation Results

There are mainly four types of noise sources in the system. In this section, these noise sources will be analyzed and noise simulation results will be given.

3.3.2.1 Brownian Noise

Brownian noise is one of the primary noise components of the system and is caused by the mechanical motion of the accelerometer. Equation 3.3.2.1.1 gives Brownian noise of the accelerometer in terms of acceleration [20].

$$a_{n,brownian} = \frac{\sqrt{4k_B TB}}{m} \quad (m/s^2\sqrt{Hz}) \tag{3.3.2.1.1}$$

where k_B is Boltzmann's constant, T is temperature, B is damping coefficient and m is the mass of accelerometer.

3.3.2.2 Readout Circuit Noise

Readout circuit noise is mainly composed of the noise components of front-end circuit and the PI controller circuit. The integrator of PI controller suppresses sigma-delta modulator circuit noise by its high DC gain. Therefore, it is not included in the calculation of readout circuit noise. Front-end circuit noise at the output is given in Equation 3.3.2.2.1 [26].

$$v_{n,fe} = v_{in} \cdot \sqrt{\frac{C_s + C_p}{C_{int}} \cdot \frac{2\pi f_u}{f_s}} \quad (V\sqrt{Hz}) \tag{3.3.2.2.1}$$

where v_{in} is the input referred noise of front-end OTA, C_s is the accelerometer sense capacitance value, C_p is the parasitic capacitance at the input of OTA, f_u is the OTA's unity gain frequency and f_s is the sampling frequency.

The PI controller circuit noise can also be calculated in a similar way since the circuit architectures of front-end and PI controller circuits are quite similar. Its noise contribution is added to front-end circuit noise and total readout circuit noise is calculated.

3.3.2.3 Quantization Noise

Quantization noise of the system comes from the quantizer error of the Σ-Δ modulator. In Section 2.2.3, it is explained that quantization noise is suppressed with additional electronic integrators in high order EM Σ-Δ modulators. In this work, it is used a second order electronic Σ-Δ modulator after PI controller for the purpose of quantization noise suppression. The integrator of PI controller also suppresses the quantization noise in addition to two integrators in the Σ-Δ modulator. Therefore, quantization noise decreases to the value very lower than the values of Brownian noise and readout circuit noise.

3.3.2.4 Feedback Voltage Noise

Feedback voltage noise is injected into the system at the feedback cycles of the system. Its acceleration equivalent noise is given as follows [27]:

$$a_{n,fb} = \frac{v_{n,fb}.V_{fb}}{m}.\frac{dC}{dx} \quad (m/s^2\sqrt{Hz}) \tag{3.3.2.4.1}$$

where $v_{n,fb}$ is the feedback voltage noise, V_{fb} is the feedback voltage. It is clear from the equation above that feedback noise increases with the feedback voltage. In fact, at high feedback voltage values, this noise source can dominate all the noise sources and therefore, it should be taken care of especially at high voltage.

Figure 3.16 shows the linearized model of the closed loop system including all noise sources.

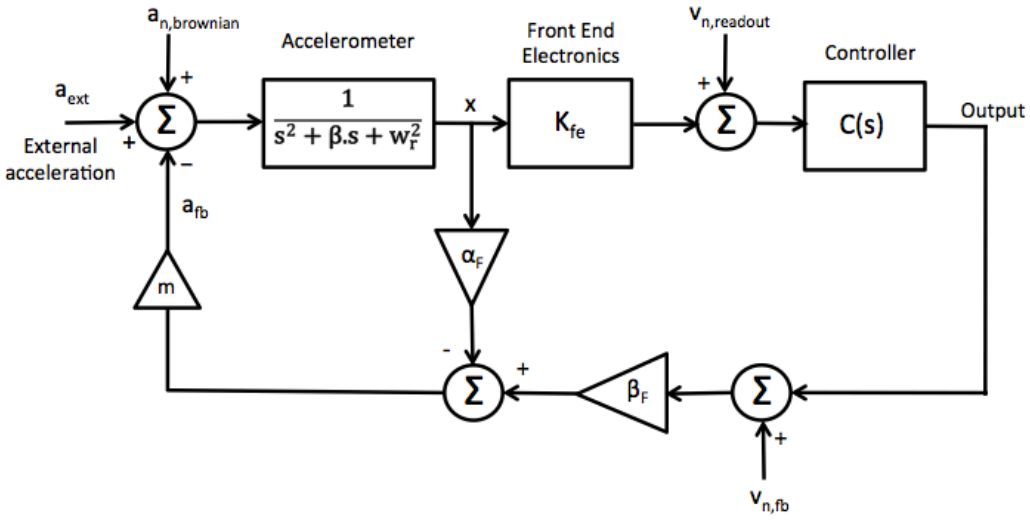

Figure 3.16: Linearized model with noise sources included.

The noise at the output of the system due to readout noise can be written as in the following equation.

$$v_{n,out} = v_{n,readout} \cdot \frac{1}{K_{fe}} \cdot \frac{1}{\beta_F} \cdot (s^2 + \beta s + w_r^2 - \frac{\alpha_F}{m}) \quad (3.3.2.1)$$

In Equation 3.3.2.1, spring softening effect is clearly observed. α_F has an effect of decreasing the spring constant or resonant frequency. Defining effective resonant frequency $w_{r,eff} = w_r^2 - \alpha_F / m$, it can be reduced down to zero by adjusting α_F. As seen in Equation 3.2.1.9, α_F can be adjusted by changing the feedback voltage. Effective resonant frequency of the accelerometer that is used in this thesis work is reduced to zero with the feedback voltage of 7.6V. Equation 3.3.2.2 shows the equation resulting with zero effective resonant frequency.

$$v_{n,out} = v_{n,readout} \cdot \frac{1}{K_{fe}} \cdot \frac{1}{\beta_F} \cdot (s^2 + \beta s) \quad (3.3.2.2)$$

$s^2 + \beta s$ term has actually a high-pass filter characteristic. Therefore, readout circuit noise at low-frequency band can be suppressed in a significant amount. Spring softening effect helps to design very low power readout electronics without degrading the performance of the system.

The complete system is simulated including all the noise sources in MATLAB-Simulink environment with the model shown in Figure 3.9. Table 3.1 gives the expected noise values of the designed system.

Table 3.1: Expected noise value of the system

Noise Sources	**Noise Value**
Brownian Noise	4.6 μg√Hz
Readout Circuit Noise	1 μV√Hz
Feedback Voltage Noise	100 nV√Hz
Quantization Noise	<1 μg√Hz
Total Output Noise	**5.3 μg√Hz**

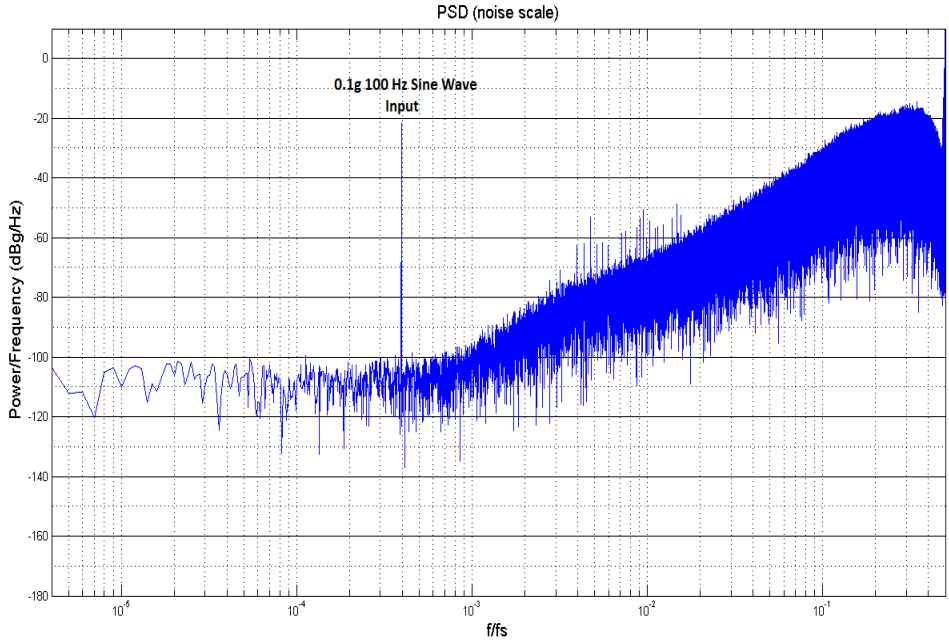

Figure 3.17: Power Spectral Density (PSD) of the designed accelerometer system simulated in MATLAB-Simulink.

Figure 3.17 illustrates the PSD noise result of the designed accelerometer system simulated in MATLAB-Simulink. It has a noise floor of -105.5 dBg/Hz, which is equivalent to 5.3 μg√Hz noise at the output. Output noise is mostly dominated by Brownian noise component. Since Brownian noise is injected into the system at the input, it is directly observed at the output.

To see the effect of spring softening on noise level, the simulations are also done with 5V and 10V feedback voltages instead of 7.6V. The results show 8.9 μg√Hz noise level for 5V feedback voltage and 10.1 μg√Hz noise level for 10V feedback voltage. Readout circuit noise starts to affect the noise performance of the complete system when feedback voltage changes from the voltage level of 7.6V.

CHAPTER 4

READOUT CIRCUIT IMPLEMENTATION

In previous chapter, system level design of EM Σ-Δ accelerometer systems was explained. A linearized model was developed in order to analyze the system behavior and simulation results of the designed system were given. This chapter will mainly focus on the circuit implementation of the blocks shown in Figure 3.1. Section 4.1 gives the designed readout circuit architecture. Section 4.2-4.6 talks about the individual blocks of the readout circuits in detail. Finally, Section 4.7 explains the top-level integration of the designed readout circuitry.

4.1 Readout Circuit Architecture

Figure 4.1 shows the architecture of the designed readout circuit. It is obvious from the figure that readout circuit has five main parts: namely front-end circuit, proportional-integral controller, second order sigma-delta modulator, bias generator and digital controller.

Front-end circuit is the core element of the readout circuit. It actually works as an interface between accelerometer and readout electronics. It mainly converts the capacitance change between accelerometer electrodes and proof mass to the electrical potential difference. A proportional-integral (PI) controller follows the front-end circuit. It is used to control the stability of the system and for increasing the system open loop gain resulting in higher linearity, wider dynamic range and higher immunity to accelerometer parameter changes.

Second-order sigma-delta modulator is used after PI controller stage. It includes two electronic integrators and a comparator. It functions to filter and suppress the quantization noise and produces one-bit digital output. Then, according to the digital

output value, feedback voltage is applied to the electrodes of the accelerometer. Level of the feedback voltage is adjusted with the high voltage level shifters.

Digital controller produces the necessary timing signals of front-end circuit, PI controller and second order sigma-delta modulator. Besides creating the required timing signals, it controls the programmable features of the readout circuit such as gain of the front-end circuit, K_p and K_I values of PI controller, gain of sigma-delta modulator, bias generator voltages and currents, sampling time, power consumptions of front-end circuit, PI controller and sigma-delta modulator and reference capacitor selection.

Bias generator creates the necessary currents and voltages of the readout circuitry. It mainly includes a bandgap reference, and programmable current and voltage DACS.

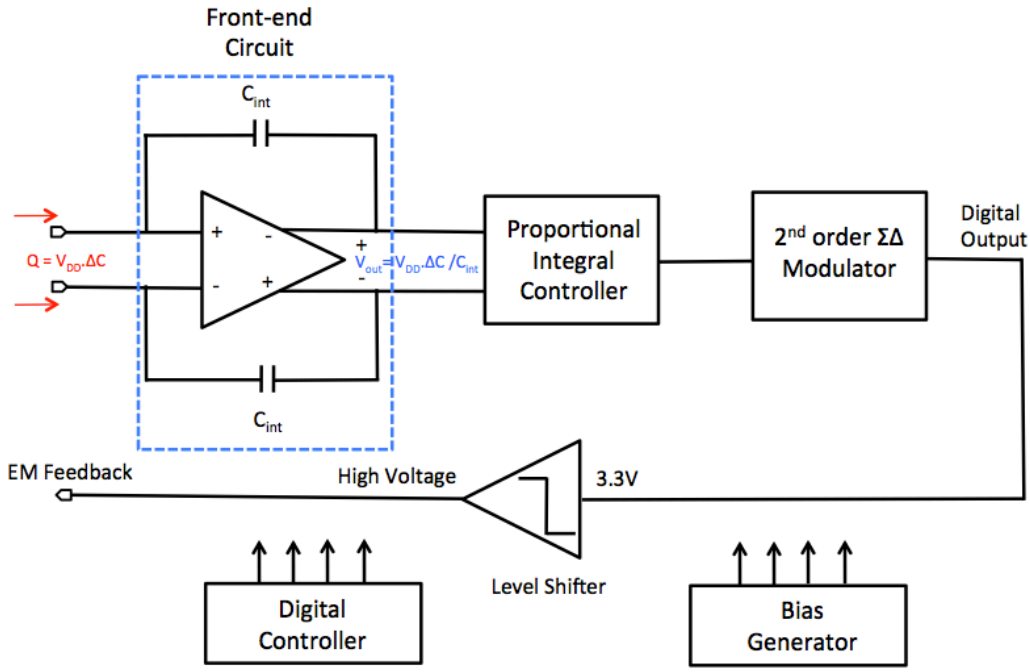

Figure 4.1: Architecture of the designed readout circuit

4.2 Front-End Circuit

The front-end circuit is the first stage of the readout circuit. This stage basically converts the capacitance between electrodes and proof mass fingers to the electrical potential difference. Besides that, it includes high voltage control switches to apply feedback voltage to accelerometer electrodes.

In the circuit implementation, fully differential type structure is preferred due to several advantages over its single ended counterpart. These advantages can be summarized in the following way [28].

- Increased immunity to external noise (less common mode or power supply noise)
- Increased voltage swing
- Reduced even order harmonics

Figure 4.2 shows the fully differential front-end circuit, which is implemented with switched-capacitor circuit. It employs a fully differential folded cascode operational transconductance amplifier (OTA), reference capacitors (C_{ref1}, C_{ref2}), correlated double sampling (CDS) capacitors, integration capacitors and CMOS switches controlling the charge flow.

CDS capacitances are used to reduce the low frequency components of noise (1/f noise) and offset created at the inputs of the OTA.

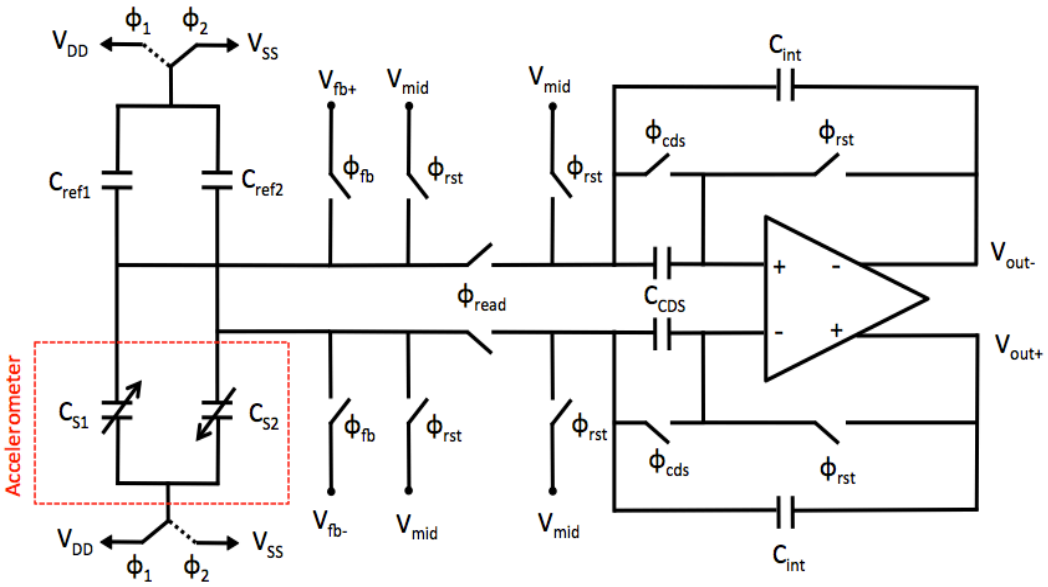

Figure 4.2: Front-end circuit diagram

4.2.1 Operation of C/V conversion

Figure 4.3 illustrates the timing diagram of front-end circuit in order to have better understanding of how capacitance to voltage conversion happens. Assume that ϕ_{cds} switches are on which means correlated double sampling operation is not performed. This is due to making the analysis easier. Timing of the front-end circuit can be separated into three phases. These are reset, integration, and feedback phases. Reset phase starts with changing ϕ_{rst} from low to high level. In this phase, integration capacitances (C_{int}) are fully discharged and OTA is in buffer configuration. Input and output voltages are set to mid-point (V_{mid}) voltage. Accelerometer electrodes are also discharged in this phase.

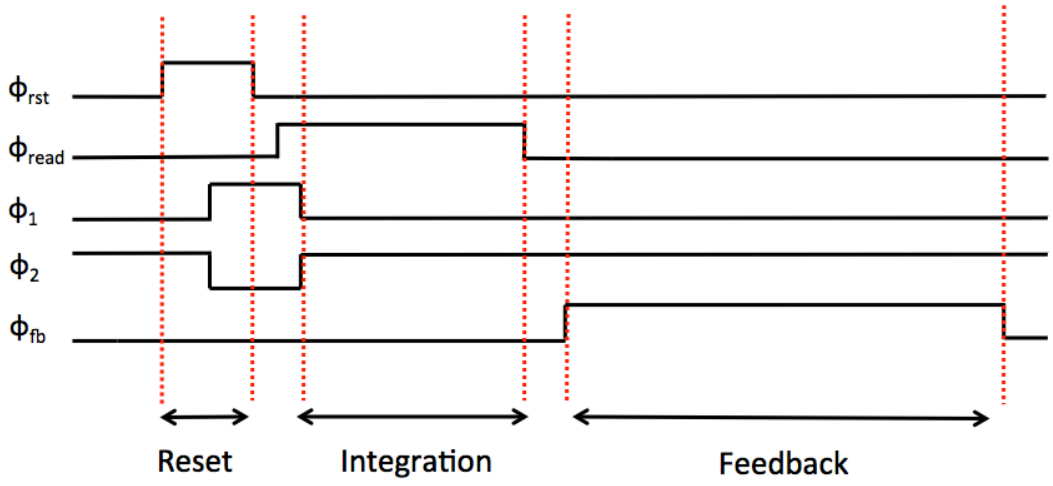

Figure 4.3: Timing diagram of front-end circuit

When reset operation is completed, ϕ_{read} switch connecting the accelerometer and OTA changes to ON position. This switch functions to prevent the OTA from high electrical discharge of accelerometer electrodes. Notice that electrical connection between accelerometer and OTA is established in only integration phase. In reset and feedback phases, this connection is broken off.

Integration phase begins with changing the state of ϕ_1 and ϕ_2 from high to low and low to high, respectively. In this state, OTA is removed from buffer configuration and is set to the integration configuration. In order to understand how charge integration happens, charges on the reference, accelerometer sense and integration capacitances should be written before and after ϕ_1 and ϕ_2 switches change their state.

Initial charge (before ϕ_1 and ϕ_2 switches change their state) on the positive and negative input nodes of OTA can be expressed respectively as follows:

$$Q_{init1} = (V_{mid} - V_{ss}).C_{ref1} + (V_{mid} - V_{dd}).C_{s1} \quad (4.2.1.1)$$

$$Q_{init2} = (V_{mid} - V_{dd}).C_{ref2} + (V_{mid} - V_{ss}).C_{s2} \quad (4.2.1.2)$$

Since reset phase is active before integration phase, input nodes of the OTA are set to the mid-point voltage. Final charge (after ϕ_1 and ϕ_2 switches change their state) on the positive and negative input nodes of OTA can be expressed respectively as follows:

$$Q_{final1} = (V_+ - V_{dd}).C_{ref1} + (V_+ - V_{ss}).C_{s1} + (V_+ - V_{out-}).C_{int} \quad (4.2.1.3)$$

$$Q_{final2} = (V_- - V_{ss}).C_{ref2} + (V_- - V_{dd}).C_{s2} + (V_- - V_{out+}).C_{int} \quad (4.2.1.4)$$

where V_+ is the positive input voltage, V_- is the negative input voltage, V_{out+} is the positive output voltage and V_{out-} is the negative output voltage of the OTA after charge integration.

According to the charge conservation principle, initial and final charges must be equal to each other. Equations 4.2.1.5 and 4.2.1.6 govern this relation.

$$Q_{init1} = Q_{final1} \quad (4.2.1.5)$$

$$Q_{init2} = Q_{final2} \quad (4.2.1.6)$$

Due to the fact that OTA has very high DC gain, positive and negative input voltages will be the same common voltage. Therefore, it can be expressed as in Equation 4.2.1.7.

$$V_+ = V_- = V_{in} \quad (4.2.1.7)$$

Equations 4.2.1.5 and 4.2.1.6 turn into the following expressions by combining the Equations 4.2.1.1 to 4.2.1.4 and 4.2.1.7. Reference capacitors C_{ref1} and C_{ref2} are chosen equal and they are expressed with C_{ref} in Equations 4.2.1.8 and 4.2.1.9.

$$\begin{aligned}&(V_{mid} - V_{in} + V_{dd} - V_{ss}).C_{ref} \\ &= (V_{in} - V_{mid} + V_{dd} - V_{ss}).C_{s1} + (V_{in} - V_{out-}).C_{int}\end{aligned} \quad (4.2.1.8)$$

$$\begin{aligned}&(V_{mid} - V_{in} + V_{dd} - V_{ss}).C_{ref} \\ &= (V_{in} - V_{mid} + V_{dd} - V_{ss}).C_{s2} + (V_{in} - V_{out+}).C_{int}\end{aligned} \quad (4.2.1.9)$$

If Equation 4.2.1.8 is subtracted from Equation 4.2.1.9, Equation 4.2.1.10 is obtained.

$$V_{out+} - V_{out-} = \frac{(V_{in} - V_{mid}).(C_{s1} - C_{s2}) + (V_{dd} - V_{ss}).(C_{s1} - C_{s2})}{C_{int}} \quad (4.2.1.10)$$

V_{in} voltage is dependent on reference and accelerometer sense capacitors. Equation 4.2.1.11 expresses this relation.

$$V_{in} = V_{mid}.\frac{3.C_{ref} - (C_{s1} + C_{s2})/2}{C_{ref} + (C_{s1} + C_{s2})/2} \quad (4.2.1.11)$$

By choosing $C_{ref} = (C_{s1} + C_{s2})/2$, V_{in} voltage is equated into the V_{mid} voltage. Therefore, Equation 4.2.1.10 simplifies to the following equation.

$$\Delta V_{out} = \frac{(V_{dd} - V_{ss}).(\Delta C_s)}{C_{int}} \quad (4.2.1.12)$$

where $\Delta V_{out} = V_{out+} - V_{out-}$, $\Delta C_s = C_{s1} - C_{s2}$.

Equation 4.2.1.12 summarizes the relation between the sense capacitors of accelerometer and differential output voltage of front-end circuit. As it is apparent from this equation that differential capacitance difference is converted into the differential output voltage. $(V_{dd} - V_{ss})/C_{int}$ is the gain of the front-end circuit.

Reference capacitors and integration capacitors in the front-end circuit have a selectable feature. One can select reference capacitors from 1 pF to 31 pF with 1pF steps. In the same way, integration capacitors can be selected from 500 fF to 15.5 pF with 500 fF steps. Therefore, gain of the front-end circuit can be adjusted in a flexible way.

The last phase of front-end circuit is the feedback phase. Differential output voltage of the front-end circuit is processed throughout the other blocks of the readout circuit and feedback voltage is applied to the electrodes of the sensor according to the output of the comparator which is the last stage of the readout circuit. Before starting to apply feedback voltage, ϕ_{read} switches will be off to disconnect the accelerometer and OTA. Then, ϕ_{fb} switches will be on and feedback phase begins. After feedback phase finishes, the next cycle will start again with reset phase.

4.2.2 Operational Transconductance Amplifier (OTA)

OTA is the most important analog block used in the readout circuit. It significantly affects the power consumption, speed and noise of the complete system. Therefore, it needs to be taken care of while designing.

Since blocks in the readout circuit such as front-end, PI controller and integrators in the sigma-delta modulator have switched-capacitor implementation, there is no need to use low output impedance OPAMPs. OTAs are more suitable to drive capacitive loads and have easier implementation.

Front-end circuit employs fully differential p-input folded cascode OTA as shown in Figure 4.4. The reason why folded cascode topology is selected is that it can easily be used in buffer configuration. It has also wider input common range and higher output swing when compared with telescopic structure. In terms of power, it has moderate power consumption. On the other hand, it has some disadvantages. It has lower open-loop gain, higher noise and lower slew rate compared with telescopic structure [29].

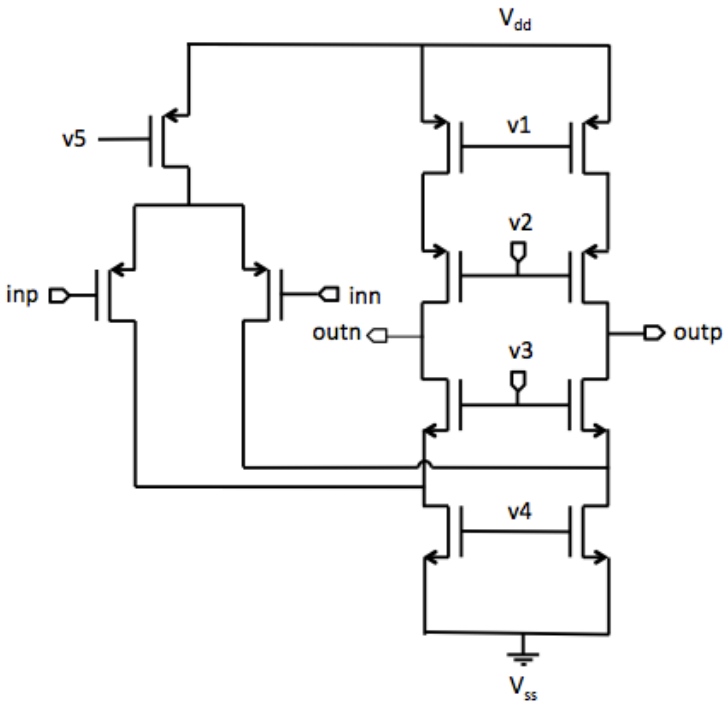

Figure 4.4: Schematic of fully differential folded cascode OTA [29].

Power consumption is the primary concern in designing the OTA because this thesis aims to implement a low-power readout circuit. However, decreasing power consumption results in higher noise and lower speed. There is a multiple trade-off between these three performance parameters.

Section 3.3.2 tells that spring softening effect can suppress readout electronic noise at low-frequency band. Therefore, it is possible to decrease the power to some extent

without considering the increase in noise level. However, speed limitation steps in here. Speed of the front-end OTA, in other words settling time, is the major factor defining the sampling frequency of the system. For deeper understanding of why it is the limiting factor on sampling frequency, mathematical expressions showing the dependencies of settling time will help a lot.

Equation 4.2.2.1 shows time constant relation of front-end circuit in integration phase [29].

$$\tau_{int} = \frac{C_L.C_{eq} + C_L.C_{int} + C_{eq}.C_{int}}{G_m.C_{int}} \quad (4.2.2.1)$$

where τ_{int} is time constant coefficient, C_L is capacitance load at the output, C_{eq} is the total capacitance at the input, C_{int} is the integration capacitance and G_m is the transconductance value of OTA.

Equation 4.2.2.2 expresses the equivalent total input capacitance.

$$C_{eq} = C_{ref} + C_s + C_{in} \quad (4.2.2.2)$$

where C_{ref} is the reference capacitance, C_s is the sense capacitance of the accelerometer and C_{in} is the input capacitance (gate and parasitic capacitances) of the OTA.

Load capacitance of the output has quite lower value than C_{eq} and C_{int}. Therefore, it is a reasonable assumption to examine time constant expression for the case $C_L = 0$. By inserting this into the Equation 4.2.2.1, following simple result is obtained.

$$\tau_{int} = \frac{C_{ref} + C_s + C_{in}}{G_m} \quad (4.2.2.3)$$

Equation 4.2.2.3 stresses that settling time of front-end circuit depends upon the accelerometer sense and reference capacitances, and G_m of the OTA. Accelerometer that is used in this thesis work has quite high sense capacitances and this leads to long settling time. This explains the reason why front-end circuit primarily determines the sampling frequency of the system.

Low sampling frequency can cause stability problems in complete system. In Section 3.2.1, it is mentioned that if sampling frequency of the system is not high enough than the input frequency of the sigma delta modulator, there will be additional phase shift between input and output. This phase shift may be sufficiently large enough that it can make the system unstable. Hence, settling time of the front-end OTA cannot be very long.

The only way to decrease settling time is to increase G_m of the OTA. Equation 4.2.2.4 shows G_m expression of the OTA [30].

$$G_m = \sqrt{2.\mu_p.C_{ox}.\left(\frac{W}{L}\right)_{in}.I_D} \quad (4.2.2.4)$$

Current and W/L ratio of the input transistors can be increased to obtain higher G_m. Increase in W/L ratio can be considered as a first option for higher Gm to have a low-power circuit. It can be increased up to a certain point because excessive increase of W/L ratio makes the chip size bigger and increases gate capacitances too much. Hence, it is a good design approach to primarily increase W/L ratio of input transistors up to a certain point and then to increase the current to obtain desired settling time.

In fully differential amplifiers, output common mode voltage is highly susceptible to mismatches and parameter variations of the transistors and it can easily drop/jump into the negative/positive supply voltages. In order to stabilize output common mode voltage, there is a need to use a common mode feedback (CMFB) circuit which functions to sense the output common voltage and compare it with a reference voltage. Then, it gives feedback by adjusting one of the bias voltages of the amplifier and sets the output common voltage to the reference voltage [31].

There are two different types of common mode feedback circuits. They are continuous CMFB and switched-capacitor CMFB. Continuous CMFB is more suitable for continuous time circuits and switched-capacitor CMFB is more suitable for discrete time circuits. Since the readout circuit that is implemented in this thesis work consists of switched-capacitor circuits (discrete time), it is more convenient to use a switched-capacitor CMFB circuit. The switched-capacitor CMFB has several advantages over continuous CMFB. Firstly, it consumes far less power than the continuous CMFB circuit that requires continuous bias current. Switched-capacitor CMFB circuit consists of only capacitors and switches that do not require any bias current. Secondly, continuous CMFB circuit adds extra poles to the output nodes that affect the frequency response of differential amplifier and can lead to stability problems. Nonetheless, the SC-CMFB circuit does not introduce extra poles. It only increases the load at the output, which does not cause any stability problems [32].

Figure 4.5 illustrates the schematic of SC-CMFB circuit that is used in the OTA. In Figure 4.5, V_{cmref} is the reference common mode voltage, V_{outp} is the positive output voltage of OTA, V_{outn} is negative output voltage of OTA, $V_{biasref}$ is the reference bias voltage and V_{bn} is the bias voltage of OTA. Equation 4.2.2.5 defines the output common mode voltage.

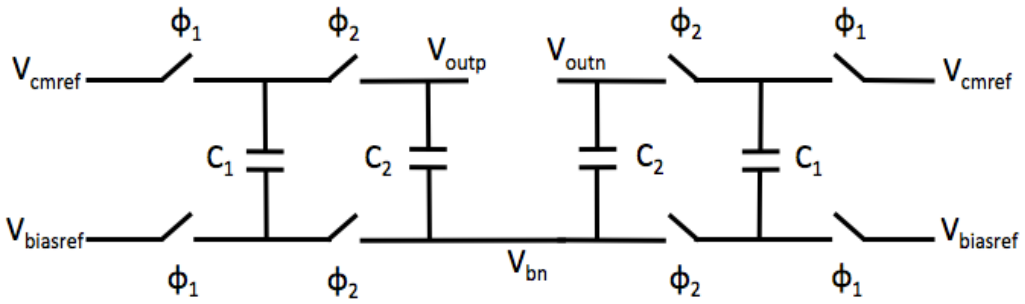

Figure 4.5: Schematic of switched-capacitor common mode feedback circuit.

$$V_{cm} = \frac{V_{outp} + V_{outn}}{2} \tag{4.2.2.5}$$

SC-CMFB circuit uses two non-overlapping clocks, namely, ϕ_1 and ϕ_2. In ϕ_1 phase, C_1 capacitors are charged to $V_{cmref} - V_{biasref}$ voltage. In ϕ_2 phase, C_1 and C_2 capacitors are connected in parallel. In this phase, output common voltage (V_{cm}) is sensed and changed by $V_{biasref} - V_{bn}$. Equation 4.2.2.6 shows the approximate output common voltage expression [32].

$$V_{cm} \cong V_{cmref} + V_{biasref} - V_{bn} \tag{4.2.2.6}$$

If output common mode voltage (V_{cm}) decreases to the value lower than reference voltage (V_{cmref}) due to any reason, the bias voltage (V_{bn}) also decreases and this leads to decrease in currents of nmos transistors. Therefore, V_{cm} increase. It is apparent that there is a negative feedback mechanism in CMFB that keeps output common mode voltage at the desired reference voltage.

Figure 4.6 shows AC simulation results of the designed front-end OTA. The DC gain is measured as 94 dB and phase margin is measured as 61^0. DC gain is kept high in order to minimize the gain error.

Figure 4.7 shows the noise simulation result of the designed front-end OTA. The circuit achieves 7.9 nV√Hz input referred thermal noise floor and 2.7 μV√Hz input referred flicker noise. The flicker noise seems to be high, but it is cancelled with CDS capacitances.

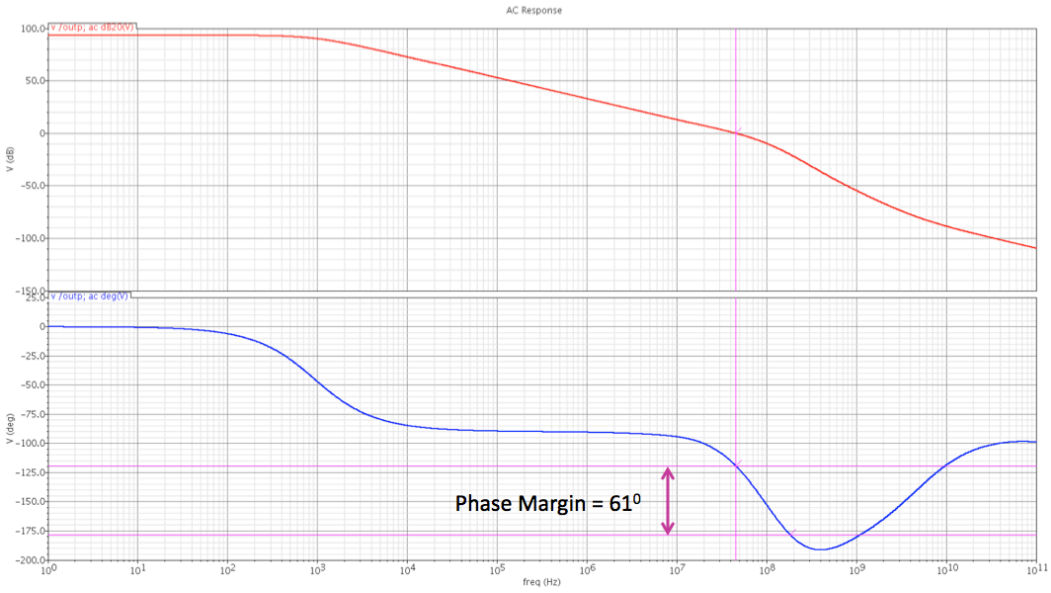

Figure 4.6: AC simulation results of the front-end OTA.

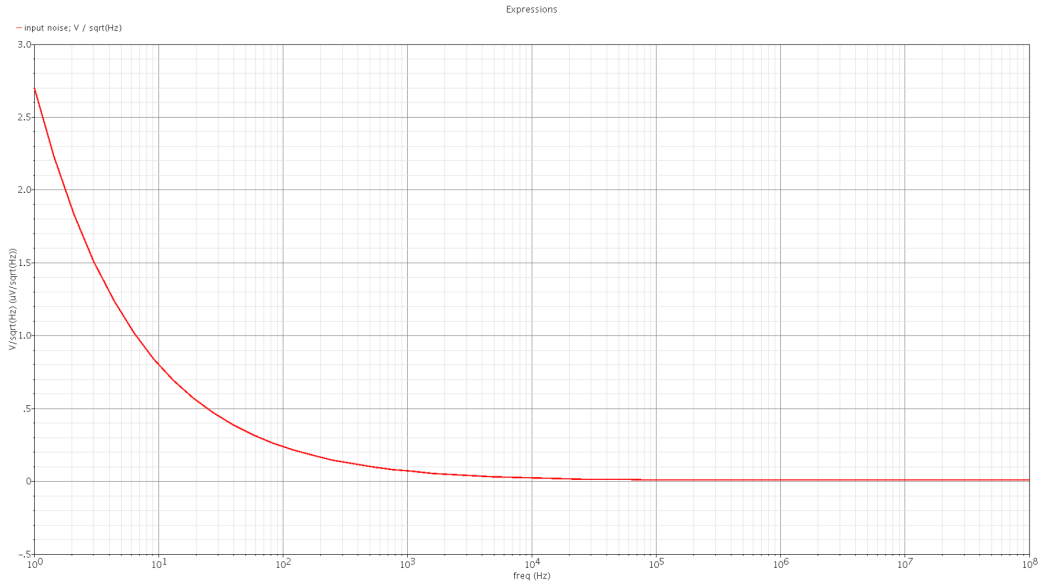

Figure 4.7: Noise simulation result of the front-end OTA.

Table 4.1 summarizes the simulation results of the designed OTA, and Figure 4.8 illustrates the layout of the front-end OTA. It was drawn fully symmetric in order to minimize the input referred offset voltage. The effect of common-mode noise and even-order nonlinearity is also suppressed with symmetric layout [29].

Table 4.1: Simulation results of the OTA used in front-end circuit.

Parameter	**Value**
Power Consumption	**676 µW**
DC Gain	94 dB
Bandwidth (at 1pF load)	1.1 KHz
Gain Bandwidth Product (at 1pF load)	44 MHz
Phase Margin (at1pF load)	61^0
Input referred flicker noise (1/f) at 1Hz	2.7µV√Hz
Input referred thermal noise floor	7.9 nV√Hz

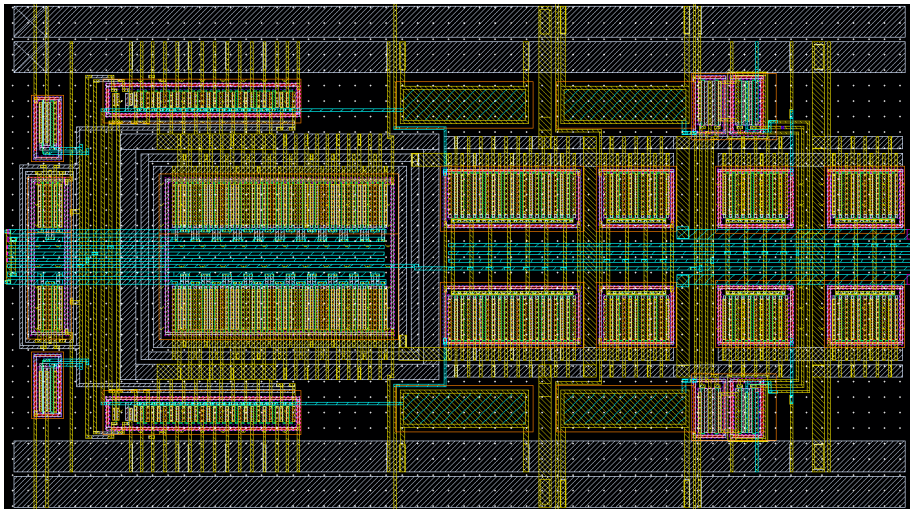

Figure 4.8: Layout of the front-end OTA. It measures 170 µm in height and 290 µm in width in a 0.35 µm CMOS technology.

4.3 Proportional-Integral (PI) Controller Circuit

Front-end circuit is succeeded by PI controller circuit, which has a transfer function as in the following equation.

$$H(s) = K_p + \frac{K_I}{s} \tag{4.3.1}$$

where K_p is the proportional gain coefficient and K_I is the integral gain coefficient. Figure 4.9 illustrates the circuit implementation of PI controller and Figure 4.10 shows the required timing diagram.

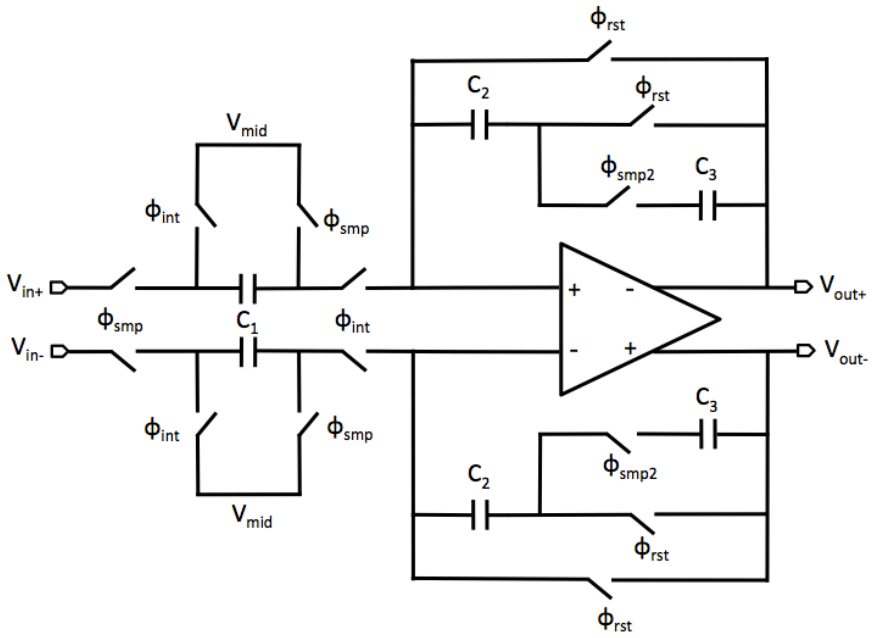

Figure 4.9: Proportional Integral (PI) controller circuit diagram.

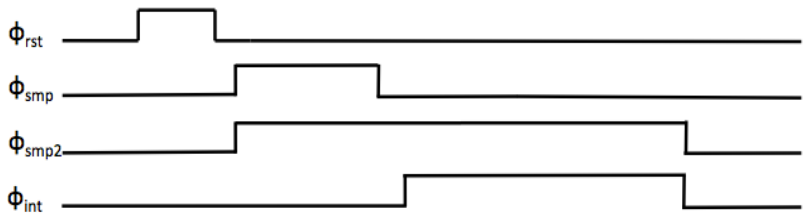

Figure 4.10: Timing diagram of PI controller circuit diagram.

Operation of PI controller starts with ϕ_{rst} phase. In this phase, OTA is forced into the buffer configuration and C_2 capacitors are discharged. After ϕ_{rst} switches change their state from high to low, ϕ_{smp} and ϕ_{smp2} go into high. At that instant, input voltage of PI controller, which is also the output of front-end circuit, begins to be sampled on C_1 capacitors. Sampling operation is performed during ϕ_{smp} phase. Charges accumulated on C_1 capacitors can be expressed as in Equations 4.3.2 and 4.3.3.

$$Q_{samp+} = (V_{mid} - V_{in+}).C_1 \tag{4.3.2}$$

$$Q_{samp-} = (V_{mid} - V_{in-}).C_1 \tag{4.3.3}$$

where Q_{samp+} is the charge on C_1 in the positive input branch and Q_{samp-} is the charge on C_1 in the negative input branch.

After sampling operation is completed, integration phase starts with ϕ_{int}. In this phase, sampled input voltages on C_1 capacitors are integrated into the capacitors C_2 and C_3. Assume that C_3 is initially discharged. According to charge conservation principle, total charge in sample phase will be equal to the total charge in integration phase. Equations 4.3.4 and 4.3.5 show the total charge in integration phase.

$$Q_{int+} = (V_+ - V_{mid}).C_1 + (V_+ - V_{out+}).\frac{C_2.C_3}{C_2 + C_3} \tag{4.3.4}$$

$$Q_{int-} = (V_- - V_{mid}).C_1 + (V_- - V_{out-}).\frac{C_2.C_3}{C_2 + C_3} \tag{4.3.5}$$

where V_+ and V_- is the positive and negative input voltages of OTA in integration phase, respectively. Since OTA used in PI controller circuit has very high open loop gain, it will equate the input voltages V_+ and V_-. If the equations from 4.3.2 to 4.3.5 are combined, Equation 4.3.6 is obtained.

$$\Delta V_{out} = \left(\frac{C_1}{C_2} + \frac{C_1}{C_3}\right).\Delta V_{in} \tag{4.3.6}$$

It can be inferred from above equation that output voltage that is proportional to capacitance ratios is acquired. At the beginning of the next cycle, capacitors C_2 are discharged with ϕ_{rst} phase while preserving the charges on capacitors C_1. Then, new input voltages are sampled and integrated again. Equation 4.3.7 states the differential output voltage of PI controller at the end of two cycles.

$$\Delta V_{out} = \frac{C_1}{C_2}.\Delta V_{in} + \frac{C_1}{C_3}(\Delta V_{in} + \Delta V_{in,prev}) \tag{4.3.7}$$

Equation 4.3.7 can be extended into more generalized form. Equation 4.3.8 gives the output voltage at the end of N cycles.

$$\Delta V_{out}(N) = \frac{C_1}{C_2}.\Delta V_{in}(N) + \frac{C_1}{C_3}.\sum_{i=1}^{N} \Delta V_{in}\,(i) \tag{4.3.8}$$

It is clear from the equation above that output voltage is consisted of two terms, which are proportional and summation terms. Summation operation is nothing but simply integration in discrete time circuits. Therefore, the circuit in Figure 4.9 successfully implements a proportional integral action.

Equation 4.3.9 expresses output to input transfer function of Equation 4.3.8 in z-domain.

$$\frac{V_{out}}{V_{in}}(z) = \frac{C_1}{C_2} + \frac{C_1}{C_3}.\frac{z}{z-1} = \frac{C_1}{C_2} + \frac{C_1}{C_3}.\frac{z^{1/2}}{z^{1/2} - z^{-1/2}} \tag{4.3.9}$$

where $z = e^{jwT_s}$, w is input frequency and T_s is the sampling time. If $z = e^{jwT_s}$ is replaced into the Equation 4.3.9, following result is obtained.

$$\frac{V_{out}}{V_{in}}(e^{jwT_s}) = \frac{C_1}{C_2} + \frac{C_1}{C_3}.\frac{e^{jwT_s/2}}{e^{jwT_s/2} - e^{-jwT_s/2}} \tag{4.3.10}$$

Since $\sin x = \frac{e^{jx} - e^{-jx}}{2j}$, Equation 4.3.10 turns into the Equation 4.3.11.

$$\frac{V_{out}}{V_{in}}(e^{jwT_s}) = \frac{C_1}{C_2} + \frac{C_1}{C_3}.\frac{e^{jwT_s/2}}{2j\sin\left(\frac{wT_s}{2}\right)} \tag{4.3.11}$$

By rearranging the terms in Equation 4.3.11, the result in Equation 4.3.12 is derived.

$$\frac{V_{out}}{V_{in}}(e^{jwT_s}) = \frac{C_1}{C_2} + \frac{C_1}{C_3}.\frac{1}{jwT_s}.\frac{wT_s/2}{\sin(wT_s/2)}.e^{jwT_s/2} \tag{4.3.12}$$

At low input frequencies, $\sin(wT_s/2) \cong wT_s/2$ and $e^{jwT_s/2}$ can be approximated to 1. Equation 4.3.13 gives the approximate input output transfer function.

$$\frac{V_{out}}{V_{in}}(e^{jwT_s}) \cong \frac{C_1}{C_2} + \frac{C_1}{C_3}.\frac{1}{jwT_s} \tag{4.3.13}$$

Proportional gain coefficient K_p and integral gain coefficient K_I can be inferred easily from the equation above. Equations 4.3.14 and 4.3.15 show K_p and K_I values respectively.

$$K_p = \frac{C_1}{C_2} \tag{4.3.14}$$

$$K_I = \frac{C_1}{C_3 . T_s} \tag{4.3.15}$$

K_p and K_I values can be adjusted freely by selecting the capacitance values of C_1, C_2 and C_3. K_I also depends on the sampling time of the system. Actually, it is an expected result because sampling time defines how many summation operations occur in a certain time. If sampling time decreases, there will be more summation operations in that certain time and vice versa.

PI controller includes a fully differential folded cascode amplifier with switched capacitor common mode feedback circuit as in front-end. In terms of speed, PI controller OTA does not drive as much capacitive load as front-end OTA drives. Therefore, speed is not that critical performance criterion of PI controller OTA while designing. Power consumption of the OTA is minimized in such a way that noise performance is not degraded very much. Also, open loop gain of the OTA is kept high in order to reduce gain errors of PI controller.

Figure 4.11 and Figure 4.12 show AC and noise simulation results of PI controller OTA respectively. Table 4.2 gives the summary of simulation results.

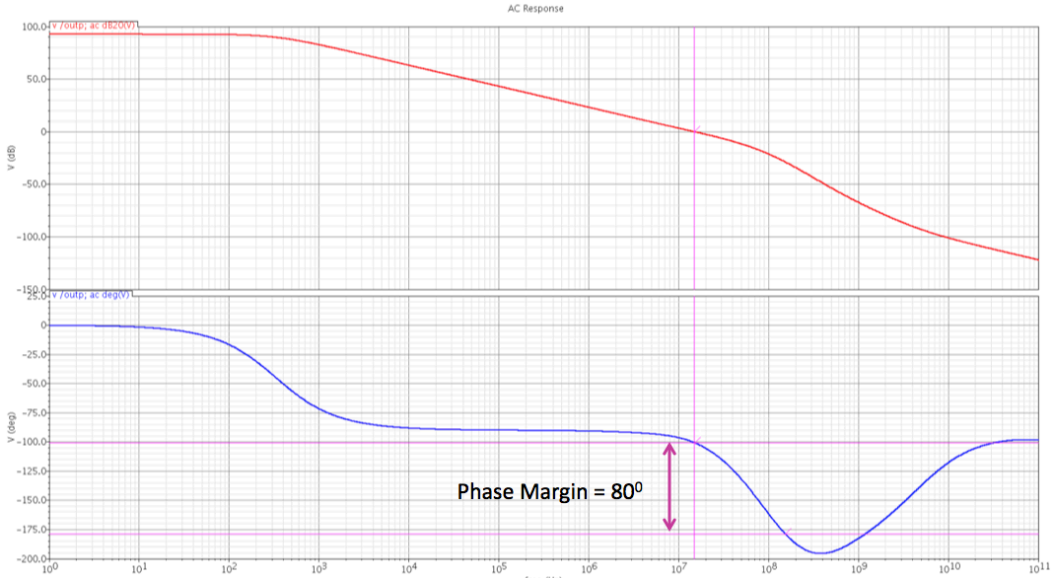

Figure 4.11: AC simulation results of PI controller OTA.

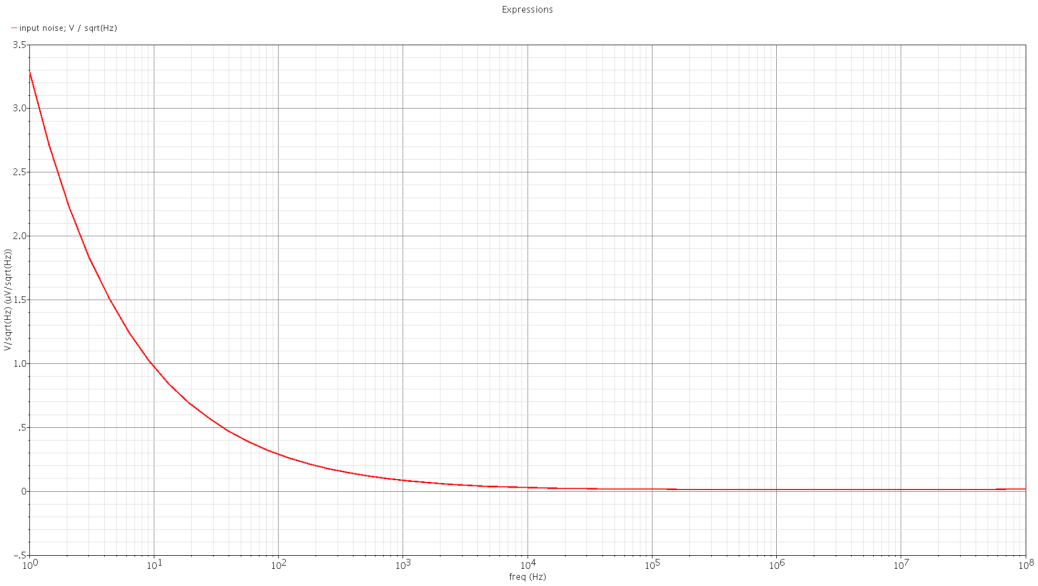

Figure 4.12: Noise simulation result of PI controller OTA.

Table 4.2: Simulation results of the OTA used in PI controller.

Parameter	**Value**
Power Consumption	**236 µW**
DC Gain	93 dB
Bandwidth (at 1pF load)	600 Hz
Gain Bandwidth Product (at 1pF load)	14.4 MHz
Phase Margin (at1pF load)	80^0
Input referred flicker noise (1/f) at 1Hz	3.3 µV√Hz
Input referred thermal noise floor	13.5 nV√Hz

4.4 Second Order Sigma-Delta (Σ-Δ) Modulator Circuit

Second order Σ-Δ modulator includes two integrators and a 1-bit comparator. Figure 4.13 shows the topology of the Σ-Δ modulator that is used in the readout circuit. In figure 4.13, the coefficients A and B are the feed-forward gain coefficients of integrator-1 and integrator-2, respectively. Coefficients C and D are called as feedback gain coefficients.

Input signal passes through two integrators and according to the accumulated signal at the output of second integrator, comparator generates digital outputs. Digital outputs are then given as feedback to the inputs of the integrators. The circuit implementation of second order Σ-Δ modulator is quite straightforward.

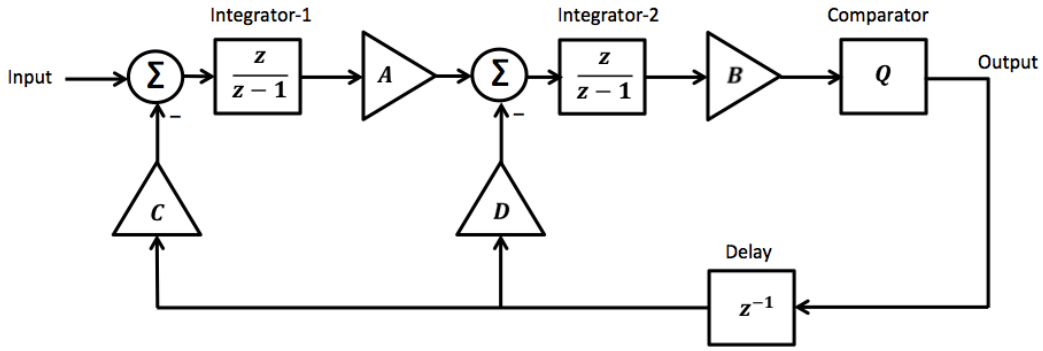

Figure 4.13: Block diagram of second order Σ-Δ modulator.

4.4.1 Integrator Circuit

As in front-end and PI controller circuits, integrator circuit is also implemented in discrete time. Figure 4.14 illustrates the schematic view of the integrator circuit. It has two differential inputs as shown in the figure. V_{in} inputs are connected to the PI controller output and V_{fb} inputs are connected to the output of the comparator in order to constitute the block diagram in Figure 4.13.

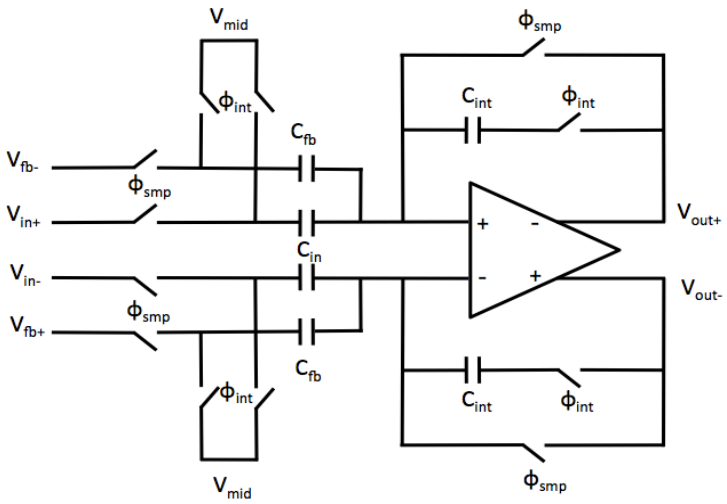

Figure 4.14: Schematic view of integrator circuit.

Operation of the integrator circuit is simple. There are two phases, which are sample and integration. In sample phase, differential input voltages are sampled on the capacitors C_{in} and C_{fb}. In integration phase, charges on these capacitors are integrated into the capacitors C_{int}.

Equation 4.4.1.1 expresses the differential output voltage of the integrator. Derivation of Equation 4.4.1.1 is very similar to the derivation of PI controller output voltage given in Equation 4.3.9. Hence, it is not derived again.

$$\Delta V_{out}(N) = \frac{C_{in}}{C_{int}} . \sum_{i=1}^{N} \Delta V_{in}(i) - \frac{C_{fb}}{C_{int}} . \sum_{i=1}^{N} \Delta V_{fb}(i) \qquad (4.4.1.1)$$

Equation 4.4.1.1 can be converted into the z-domain easily as in Equation 4.4.1.2.

$$\frac{V_{out}}{V_{in}}(z) = \left(\frac{C_{in}.V_{in} - C_{fb}.V_{fb}}{C_{int}}\right) . \frac{z}{z-1} \qquad (4.4.1.2)$$

Figure 4.15 shows the schematic view of Σ-Δ modulator integrators with electronic feedback from the comparator outputs. Figure 4.16 shows the associated timing diagram of these integrators.

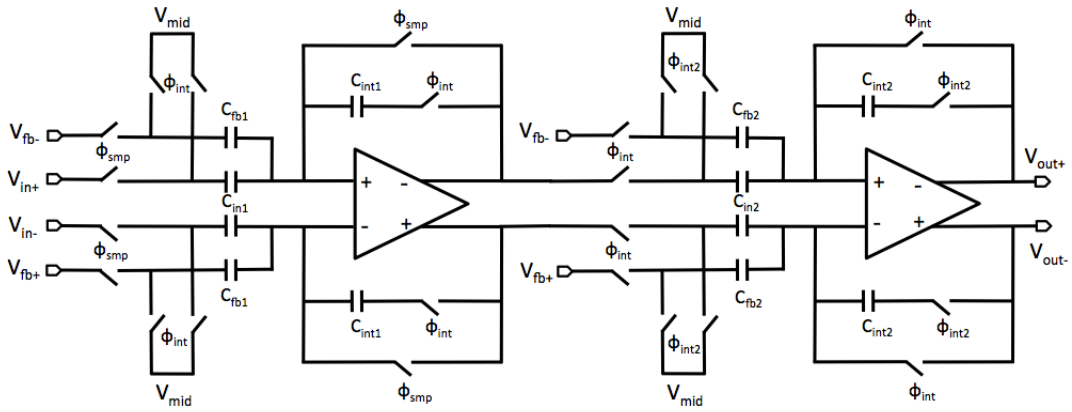

Figure 4.15: Schematic view of Σ-Δ modulator integrators with electronic feedback

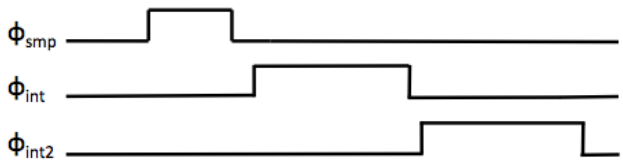

Figure 4.16: Timing diagram of Σ-Δ modulator integrators

According to the timing diagram in Figure 4.16, while first integrator is transferring the charges on input capacitors to the integration capacitors (C_{int1}) in integration phase (ϕ_{int}), second integrator begins to sample C_{int1} voltage on C_{in2} capacitors and feedback voltage on C_{fb2} at the same time. After ϕ_{int} phase finishes, integration phase of second integrator (ϕ_{int2}) begins and corresponding output voltages are obtained.

There is an important point here to notice. Second integrator output is forwarded to the comparator and comparator generates digital output. However, this digital output is given as feedback to the integrators in the next cycle. Hence, there is one cycle delay in the feedback path. This delay is also represented with its z-domain equivalent in Figure 4.13.

The gain coefficients A, B, C and D in Figure 4.13 can be expressed as in the equations from 4.4.1.3 to 4.4.1.6. Capacitance values are selected in order to obtain desired gain coefficient.

$$A = \frac{C_{in1}}{C_{int1}} \tag{4.4.1.3}$$

$$B = \frac{C_{in2}}{C_{int2}} \tag{4.4.1.4}$$

$$C = \frac{C_{fb1}}{C_{int1}} \tag{4.4.1.5}$$

$$D = \frac{C_{fb2}}{C_{int2}} \tag{4.4.1.6}$$

OTAs used in Σ-Δ modulator integrators are the same as in PI controller circuit since the specifications of these circuits are quite similar. Therefore, a new OTA was not designed in Σ-Δ modulator integrators.

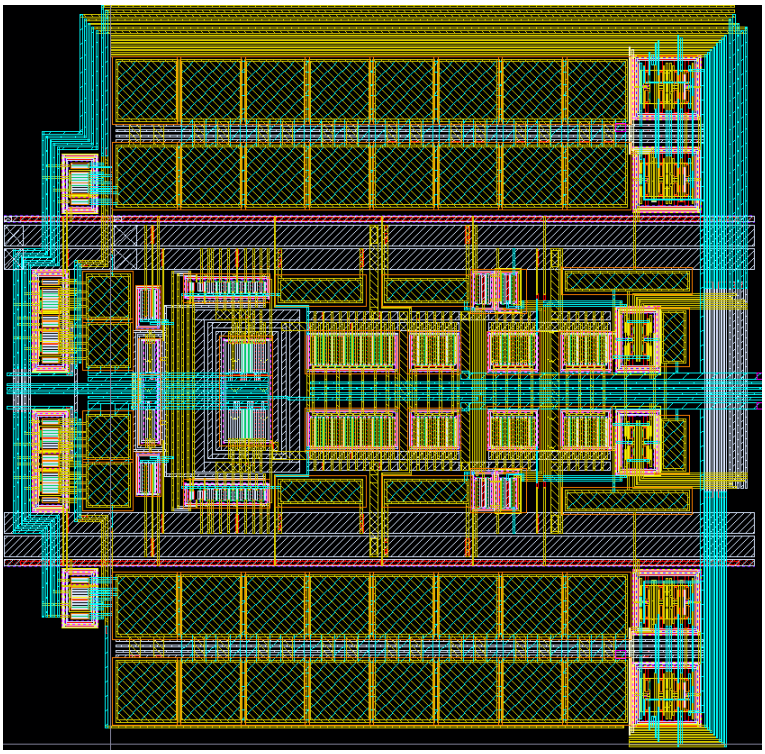

Figure 4.17: Layout of the integrator. It measures 360 μm in height and 365 μm in width in a 0.35 μm CMOS technology.

Figure 4.7 shows the layout of the designed integrator. It has also a symmetrical layout. Integrator OTA is placed between the power rails, and capacitors and switches are put above the power rails as seen in Figure 4.7.

4.4.2 Dynamic Latched Comparator

The final stage of the 2nd order Σ-Δ modulator is 1-bit comparator. The comparator samples the output of the second integrator and converts it to the digital output. It keeps output voltage until the next sample.

While choosing the type of comparator and designing it, there are some performance parameters that are taken care of. Speed, gain, power dissipation and offset are the important ones. In the Σ-Δ modulator, a dynamic latched comparator topology is selected due to its zero static power consumption, high speed, and full swing digital output level. Nonetheless, dynamic latched comparators suffer from the high input referred offset voltage. Using a preamplifier stage in front of the dynamic latched comparator can reduce offset voltage in considerable amount. However, there is no need to use a preamplifier in sigma-delta modulators because the integrators used before the comparators suppress the input offset voltage.

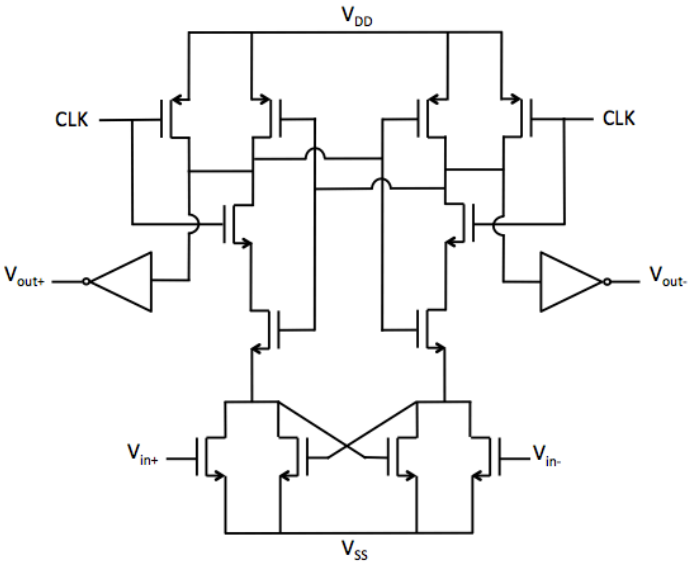

Figure 4.18: Schematic view of dynamic latched comparator.

Figure 4.18 shows the dynamic latched comparator circuit that is used in the Σ-Δ modulator. It includes two back-to-back inverters constituting the latch and it needs a clock signal. When the clock signal goes to low, the outputs of the comparator are set to low voltage. At the rising edge of the clock, the comparison operation begins. Back-to-back inverters provide positive feedback converting the small voltage difference at the inputs of the comparator to the full swing digital output.

4.5 Bias Generator

Bias generator produces all the bias voltages and currents of the readout circuit. It includes four main parts, which are bandgap voltage generation, reference current generation, current DACs and voltage DACs. It totally generates 6 bias voltages and 4 bias currents for the OTAs used in the readout circuit.

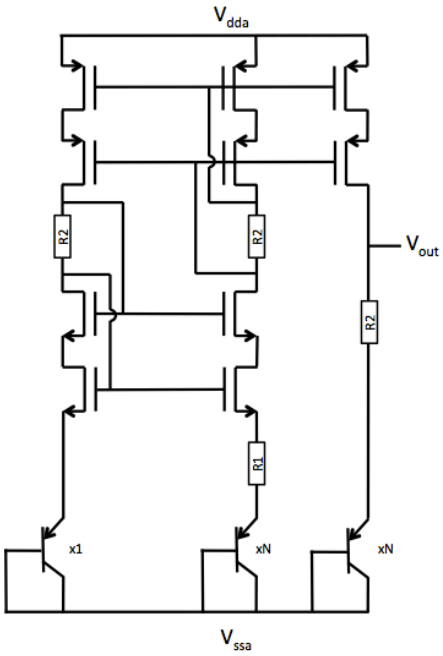

Figure 4.19: Schematic view of bandgap generation circuit [29].

Bandgap generation produces a temperature and supply independent voltage for the reference generation block. As name suggests, bandgap generation block produces a voltage around 1.2 V, bandgap energy of the Silicon. Bandgap circuits in the literature needs two components. These are the negative temperature coefficient base-emitter voltage of BJT and the positive temperature coefficient voltage. These two voltages then add up with the right coefficients to build a temperature independent voltage. Positive temperature coefficient voltage is generally created from the current that is proportional to absolute temperature (PTAT) and a resistor.

In Figure 4.19, currents flowing through all the branches are same and proportional to absolute temperature. The value of the PTAT current is determined with the BJT multiplier factor, N, and the resistance, R1. The current flowing through the branches can be written as [29]:

$$I_{branch} = \frac{V_t \ln N}{R_1} \tag{4.5.1}$$

where, I_{branch} is the branch current, V_t is the thermal voltage, N is the BJT multiplier factor, and R_1 is the resistance. The output voltage can be found as;

$$V_{out} = V_{BE} + V_t \ln N \frac{R_2}{R_1} \tag{4.5.2}$$

where, V_{out} is the output voltage of the bandgap generation block, V_{BE} is the base-emitter voltage of , N is the diode multiplier, R_1 and R_2 are the resistances. When the derivative of Equation 4.5.2 w.r.t. temperature is taken, base-emitter voltage brings negative component, and thermal voltage brings positive component. With the right R_1, R_2, and N, temperature independent voltage is obtained, and it is close to the bandgap energy of the Silicon. In this thesis work, 1.213 V of bandgap voltage is obtained. In case of any failure in bandgap generation, bias generator also allows using external bandgap voltage. Therefore, the rest of the circuit will not be affected and will work properly.

After the temperature independent bandgap voltage is generated, this voltage is used for reference current generation. Reference current will be used to obtain necessary bias voltages and currents. Reference current generated by this circuit is 1uA. Reference current is then mirrored to be used in current and voltage DACs.

Bias generator includes 4 current DACs and 6 voltage DACs, which can be programmed by digital controller with 5-bit selection. Current DACs have a range of 1 µA and 31 µA with 1µA steps. Voltage DACs have a range of 0.1 V and 3.3 V with approximately 100 mV steps.

4.6 Digital Controller

The digital controller generates all the timing signals of the readout circuit that are necessary for proper operation. It also allows adjusting bias currents and voltages of the readout circuit, and changing programmable features of the readout circuit such as gain of the front-end circuit, K_p and K_I values of PI controller, gain of sigma-delta modulator, sampling time reference capacitor selection, optional external timings and optional bandgap reference voltage.

Figure 4.20 shows the block diagram of the digital controller that is implemented in this thesis. Digital controller is consisted of three main blocks, which are serial programming interface, digital memory and timing generator.

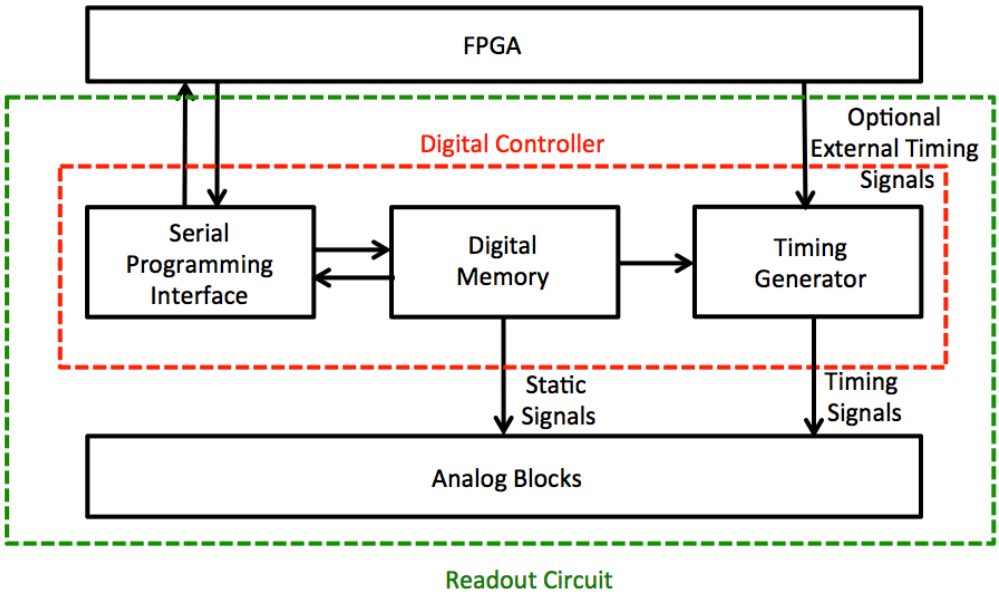

Figure 4.20: Digital controller block diagram

4.6.1 Serial Programming Interface

The serial programming interface provides the communication of the chip with external electronics such as FPGA. It uses 4-wire communication. Serial data input, serial clock and active low enable signal are input wires and serial data output is the output wire.

The communication type used in this serial programming interface is address-based communication, which means that it needs address information writing to the memory or reading back from the memory.

Figure 4.21 shows the 15-bit register content of the serial programming interface circuit. It includes 8 bit data, 6-bit address and 1 bit read/write registers.

14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
W/R	address<5:0>						data<7:0>							

Figure 4.21: Serial programming interface register table

To be able to communicate properly with the chip, FPGA should send data from least significant bit (LSB) to most significant bit (MSB). Figure 4.22 shows the serial interface timing diagram. At each time, 8-bit data, 6-bit address data and 1 bit read/write data are sent to chip (write mode) or sent back from the chip to the FPGA (read mode). Hence, one communication period lasts 15 clock cycles. The enable signal goes low when communication starts and it remains low until the end of communication.

There are two modes in communication, which are read and write modes. Chip understands in which mode it is working by looking at the last bit of the serial data. If the last bit is zero, read mode is active and vice versa. In read mode, 8-bit data bits are don't care bits. Only address bits and W/R bit should truly be specified to get back the memory data. Read data is sent serially from serial data output wire. In write mode, one should also send 8-bit data correctly along with the address bits and W/R bit.

An important point is that chip samples the serial data at the rising edge of the serial clock. Therefore, FPGA should change the serial data at the falling edge of the serial clock.

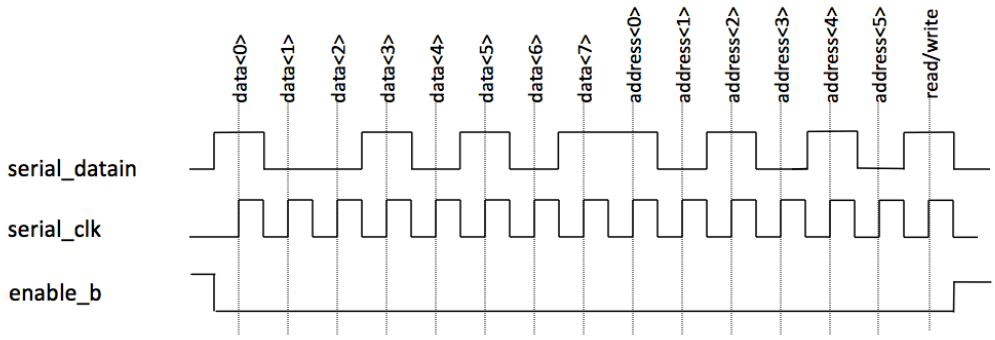

Figure 4.22: Serial interface timing diagram

4.6.2 Digital Memory

Digital controller includes 51 bytes register type digital memory, which stores the control bits related with timing generator, bias generator and programmable features of the readout circuit. Digital memory has a structure that provides opportunity to read the contents of it through the serial programming interface to the external world.

4.6.3 Timing Generator

The readout circuit needs total 14 digital timing signals and their complements. Timing generator block produces these timing signals. It provides high flexibility to obtain desired signals. Figure 4.23 shows one period of a timing signal along with system clock.

Rising and falling edges of a timing signal can be adjusted freely in timing generator. Rising edge of the signal is determined by 8-bit memory data that is represented with set count in the figure below. Similarly, falling edge of the signal is determined by another 8-bit data that is represented with reset count. As a result, timing signals can be tuned with one clock cycle precision. In addition to this, timing signals can be toggled. One bit memory is reserved for toggling operation. Therefore, a timing signal is controlled with 17 bits.

Line count defines the period of timing signals. In other words, it specifies the sampling time of the readout circuit. 8-bit data is reserved for line count in the memory.

Timing generator circuit also allows external timing signals to be used in the readout circuit instead of timing signals generated inside the chip. This is due to any possible problem causing digital controller not to work properly. In that case, external timing signals can be used to make readout circuit still work.

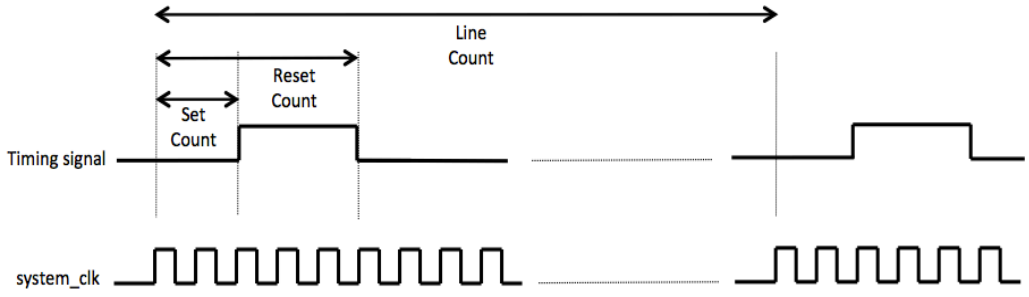

Figure 4.23: Illustration of a timing signal.

Figure 4.24 shows the layout of digital controller. Digital controller occupies 2100x480 μm^2 area. The layout is composed of three main sub-blocks. The first one is the serial programming interface, which is placed at the top in the given layout. The second one is the digital memory, which is the large array placed in the middle of the layout. The last one is the timing generator placed at the bottom of the layout.

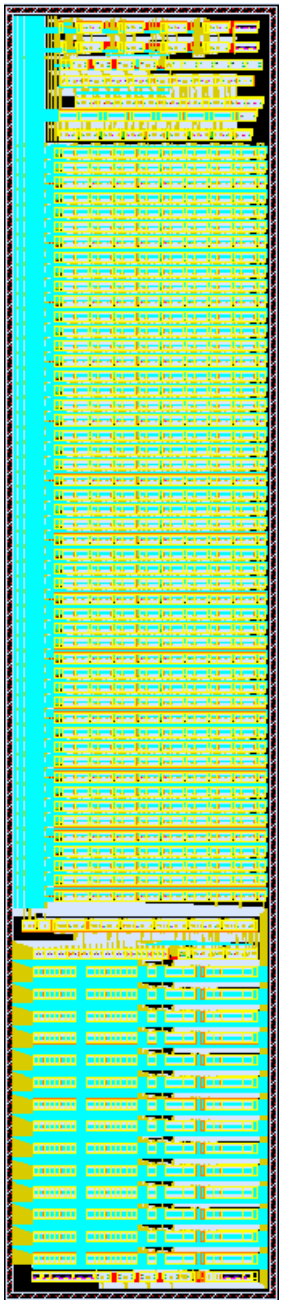

Figure 4.24: Digital controller layout. It measures 2100 µm in height and 480 µm in width in a 0.35 µm CMOS technology.

4.7 Top Level Integration

Individual layouts of the designed readout circuit blocks are combined to have a top-level layout. Figure 4.25 shows the floor plan of top-level layout. As it is obvious from the figure that digital controller is placed at the bottom side of the chip and it lays from one end to the other end. It occupies most of the chip area due to the fact that high programmability requires plenty of memory space. At the topside, front-end circuit, PI controller, second-order sigma-delta modulator and bias generator are placed from left to right.

The chip measures 2900x1900 µm in 0.35 µm CMOS process and includes total of 42 pads, three of them are not used. Table 4.3 shows the pad list of the designed readout circuit. Timing signals of readout circuit can also be driven externally in case of any failure in internally generated timing signals. 14 digital test signal pads are placed into the pad layout for this purpose. 3 analog signal pads are also used for similar purpose. 4 pads are used for the communication of the chip with external world. The chip has one system clock pad, one reset pad and two digital output pads. Accelerometer interface is provided by three pads. These pads are Acce_Pos and Acce_Neg used to drive positive and negative electrodes of the accelerometer, and Proof_Mass_Drive used to drive proof mass of the accelerometer. Rests of the pads are power supply and ground pads. They are separated with digital, analog and high voltage power pads.

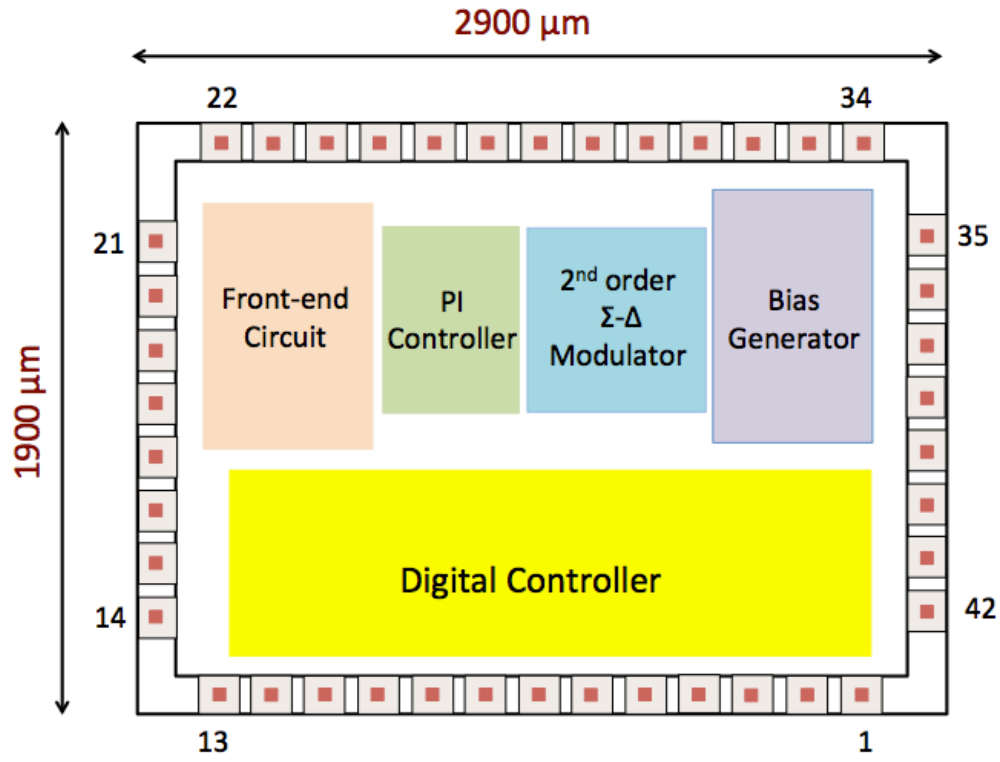

Figure 4.25: Floor plan of top-level layout

Table 4.3: Pad list of the designed readout circuit.

Pad Number	***Pad Name***	***Pad Number***	***Pad Name***
1	Digital_Test_0	22	Acce_Pos
2	Digital_Test _1	23	Acce_Neg
3	Digital_Test _2	24	Proof_Mass_Drive
4	Digital_Test _3	25	High Voltage Supply
5	Digital_Test _4	26	High Voltage Ground
6	Digital Supply	27	High Voltage Ground
7	Digital Ground	28	Analog Supply
8	Digital Ground	29	Analog Ground
9	Digital_Test _5	30	Analog Ground
10	Digital_Test _6	31	Pad_vdd
11	Digital_Test _7	32	Pad_gnd
12	Digital_Test _8	33	Analog Signal
13	Digital_Test _9	34	Analog Signal
14	Digital_Test _10	35	Not used
15	Digital_Test _11	36	Not used
16	serial_datain	37	Analog Signal
17	s_latch	38	Digital Output -
18	serial_clk	39	Digital Output +
19	system_clk	40	sdout
20	rstb	41	Digital_Test _12
21	Not used	42	Digital_Test _13

Figure 4.26 shows the top-level layout of the designed readout circuit chip. The chip measures 1900 µm in height and 2900 µm in width in a 0.35 µm CMOS process. The given layout is drawn according to floor plan given in the Figure 4.25.

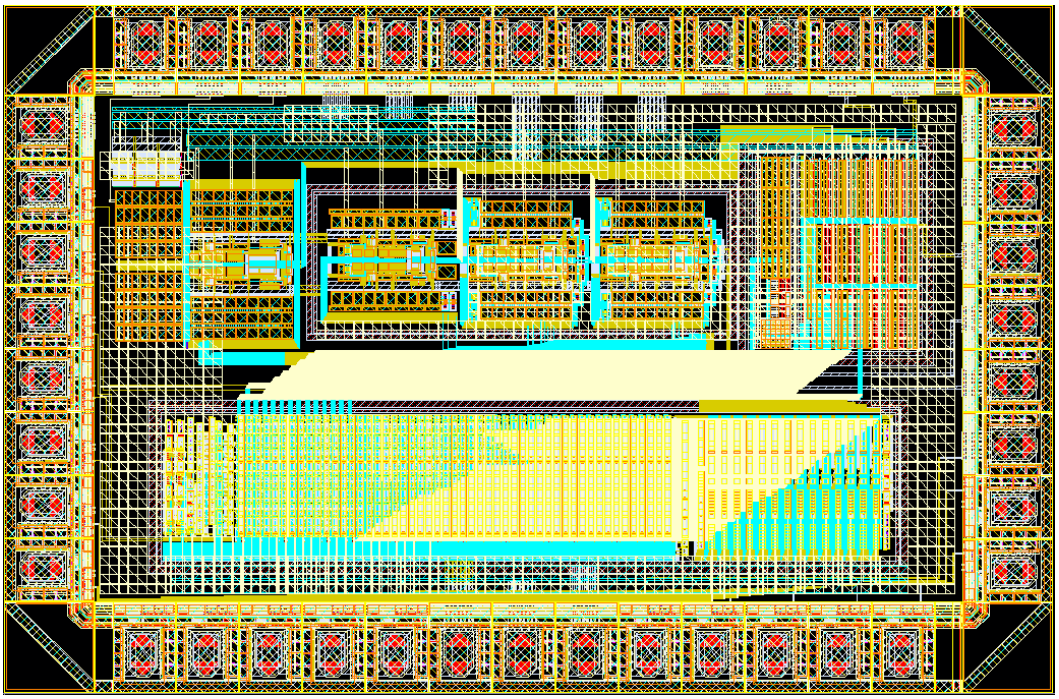

Figure 4.26: Top-level layout of the designed readout circuit chip. The chip measures 1900 μm in height and 2900 μm in width in a 0.35 μm CMOS process .

CHAPTER 5

SUMMARY AND CONCLUSIONS

The research conducted in this thesis focuses on the design of a low-power and programmable capacitive CMOS integrated readout circuit for high performance accelerometers with various electrical and mechanical properties. The results of this work can be summarized as follows:

1. The readout circuit designed in this thesis work consumes 1.8 mW power using a 3.3 V supply voltage. When compared with the previous work [13], the power consumption is decreased to about $1/9^{th}$ of the power consumption of the previous work.
2. The readout circuit is designed to have many programmable features allowing to control the gain, biasing, and timing of various analog blocks in the chip, making this readout chip suitable for a various capacitive accelerometer sensors with a wide range of sense capacitance values from 1pF to 31 pF.
3. A linearized model, which completely matches with the simulation results of the non-linear MATLAB-Simulink model, has been developed. Stability and noise of the system can easily be analyzed using this linearized model.
4. The immunity of the system to sensor parameter changes and the linearity of the system are increased due to the high open loop gain provided by this readout circuit utilizing a PI controller.
5. The output noise of the system is simulated as 5.3 μg√Hz using the accelerometer with the parameters given in Table 2.1. It has been found that the output noise is dominated by the Brownian noise of the accelerometer. The readout circuit noise and the quantization noise are suppressed down to the Brownian noise level.
6. The input range of the system is calculated as ±19.5g, assuming the accelerometer parameters given in Table 2.1. This result corresponds to a dynamic range of 128.5 dB.

7. It should be noted that the readout circuit developed in this thesis provides similar noise and dynamic range values with a fraction power of the previously developed readout circuits, in addition to several programmable features simplifying overall system integration.

REFERENCES

[1] MEMS and Nanotechnology Exchange, "What is MEMS technology?," https://www.mems-exchange.org/MEMS/what-is.html, last access: 19.08.2013

[2] PRIME Faraday Partnership, "An Introduction to MEMS," Wolfson School of Mechanical and Manufacturing Engineering, Loughborough University, 2002.

[3] P. Doe, "Consumer markets drive MEMS scaling and efforts to cut development time," http://www.semi.org/en/node/39781, last access: 20.08.2013

[4] Yole Devolopment Market Research and Strategy Development Company, "Status of MEMS Industry 2013," http://www.i-micronews.com/reports/Status-MEMS-Industry-2013/1/384/, last access: 22.08.2013

[5] N. Yazdi, F. Ayazi, and K. Najafi, "Micromachined Inertial Sensors," Proc. of the IEEE, Vol. 86, No 8, pp. 1640-1659, August 1998

[6] F. Chollet and H. Liu, "A (not so) short Introduction to MEMS," ver. 5.0, 2012. http://memscyclopedia.org/introMEMS.html

[7] M. Andrejašic, "MEMS Accelerometers," Faculty for mathematics and physics Department of Physics, University of Ljubljana, March 2008.

[8] M. Kraft, "Micromachined Inertial Sensors State of the Art and a Look into the Future", University of Southampton.

[9] SENSR, "Practical guide to Accelerometers," http://www.sensr.com/pdf/practical-guide-to-accelerometers.pdf, last access: 22.08.2013.

[10] Ilker E. Ocak, "A Tactical Grade MEMS Accelerometer," PhD. Thesis, Middle East Technical University, 2010.

[11] M. Lemkin, B. E. Boser and D. Auslander, J. H. Smith, "A 3-axis force balanced accelerometer using a single proof-mass," International Conference on Solid State Sensors and Actuators, TRANSDUCERS 1997, vol.2, June 1997, pp. 1185.

[12] Reha Kepenek, "Capacitive CMOS Readout Circuits for High Performance MEMS Accelerometers," MSc. Thesis, Middle East Technical University, 2008.

[13] Uğur Sönmez, "Capacitive CMOS Readouts for High Performance MEMS Accelerometers," MSc. Thesis, Middle East Technical University, 2011.

[14] J. Raman, P. Rombouts, and L. Weyten, "An Unconstrained Architecture for Systematic Design of Higher Order ΣΔ Force-Feedback Loops," IEEE Transactions on Circuits and Systems, vol. 55, July 2008 pp.1608-1614.

[15] Richard Schreier and Gabor Temes, "Understanding Delta-Sigma Data Converters," IEEE Press Piscataway, NJ, 2005 pp. 50-53.

[16] University of Berkeley, “Oversampled ADCs,” Lecture Notes for ECE 247, Department of Electrical and Computer Engineering. [Online]. Available: http://inst.eecs.berkeley.edu/~ee247/fa07/files07/lectures/L26_f07.pdf

[17] Steven R. Norsworthy, Richard Schreirer and Gabor C. Temes, ”Delta-Sigma Data Converters Theory Design and Simulation,” IEEE Press Piscataway, NJ, 1997 pp. 141-163.

[18] Jiangfeng Wu and L. Richard Carley,”Electromechanical-Modulation With High-Q Micromechanical Accelerometers and Pulse Density Modulated Force Feedback,” IEEE Transactions on Circuits and Systems, vol. 53, issue 2, February 2006, pp. 274-287.

[19] B.V. Amini, R. Abdolvand and F. Ayazi, "A 4.5-mW Closed-Loop Micro-Gravity CMOS SOI Accelerometer," Solid-State Circuits, IEEE Journal of, vol.41, no.12, pp.2983, 2991, Dec. 2006

[20] V.P. Petkov and B.E. Boser, ” A Fourth-Order ΣΔ Interface For Micromachined Inertial Sensors,” Journal of Solid State Circuits, vol. 40, August 2005 pp. 1602-1609.

[21] Y.T. Liu, X.W. Liu, Y.Wang and W.P. Chen, ” A sigma–delta interface ASIC for force-feedback micromachined capacitive accelerometer,” Analog Integrated Circuits and Signal Processing, vol. 72, issue 1, December 2011 pp. 27-35.

[22] Yufeng Dong, M. Kraft, W. Redman-White, "Higher Order Noise-Shaping Filters for High-Performance Micromachined Accelerometers," Instrumentation and Measurement, IEEE Transactions on, vol.56, no.5, pp.1666, 1674, Oct. 2007

[23] Burak Eminoglu, “Weekly Progress Report be110724,” Vol. 135, Middle East Technical University, 2011.

[24] Gang Zhang, “Design and Simulation of a CMOS MEMS Accelerometer,” MSc. Thesis, Carnegie Mellon University, 1998.

[25] Ogata, Katsuhiko, “Modern Control Engineering,” Englewood Cliffs, NJ, Prentice Hall, 1990.

[26] H. Külah, J. Chae, N. Yazdi, and K. Najafi, ”Noise Analysis and Characterization of a Sigma-Delta Capacitive Microaccelerometer,” Journal of Solid State Circuits, vol. 41, issue 2, Feb. 2006, pp. 352 - 361.

[27] U. Sönmez, H. Külah, and T. Akın, ” A Flexible 4th-Order Σ-Δ Micro Accelerometer with 6 ug/√Hz Resolution and 130 dB Dynamic Range,” METU MEMS, 2011.

[28] Texas Instruments, ”Fully-Differential Amplifiers,” Application Report, Jan. 2002.

[29] Behzad Razavi, ”Design of Analog CMOS Integrated Circuits,” McGraw Hill, Singapore 2001.

[30] Paul R. Gray, Paul J. Hurst, Stephen H. Lewis and Robert G. Meyer ”Analysis and Design of Analog Integrated Circuits,” 5th Ed., John Wiley & Sons, Inc., United States of America 2009.

[31] C. Bula and M. Jimenez,“Practical Considerations for the Design of Fully Differential OTAs with SC- CMFB,” IEEE Latin American Symposium on Circuits and Systems, 2010.

[32] O.Choksi and L.Carley,“Analysis of switched-capacitor common-mode feedback circuit,” IEEE Trans. on Circuits and Systems II: Analog and Digital Signal Processing, vol. 50, no. 12, pp. 906–917, Dec. 2003.