COMPARISON OF CRYSTAL SI SOLAR CELLS FABRICATED ON P-TYPE AND N- TYPE FLOAT ZONE SILICON WAFERS

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
MIDDLE EAST TECHNICAL UNIVERSITY

BY

MAKBULE BİLGEN

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF MASTER OF SCIENCE
IN
PHYSICS

SEPTEMBER 2013

Approval of the Thesis:

COMPARISON OF CRYSTAL SILICON SOLAR CELLS FABRICATED ON P-TYPE AND N-TYPE FLOAT ZONE SILICON WAFERS

submitted by **Makbule Bilgen** in partial fulfillment of the requirements for the degree of **Master of Science in Physics Department, Middle East Technical University** by,

Prof. Dr. Canan Özgen _____
Dean, Graduate School of **Natural and Applied Sciences**

Prof. Dr. Mehmet Zeyrek _____
Head of Department, **Physics**

Prof. Dr. Raşit Turan _____
Supervisor, **Physics Dept., METU**

Examining Committee Members:

Prof. Dr. Mehmet Parlak _____
Physics Dept., METU

Prof. Dr. Raşit Turan _____
Physics Dept., METU

Prof. Dr. Nizami Hasanlı _____
Physics Dept., METU

Assist. Prof. Dr. Alpan Bek _____
Physics Dept., METU

Assist. Prof. Dr. Kadir Ertürk _____
Physics Dept., NKU

Date: 02.09.2013

I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

Name, Last Name: Makbule Bilgen

Signature :

ABSTRACT

COMPARISON OF CRYSTAL SI SOLAR CELLS FABRICATED ON P-TYPE AND N-TYPE FLOAT ZONE SILICON WAFERS

Bilgen, Makbule

Master of Science, Department of Physics

Supervisor : Prof. Dr. Raşit TURAN

September 2013, 91 pages

Solar cells are traditionally fabricated on p-type Si substrates due to the high electron diffusion length in p-type substrate. However, high quality float zone silicon wafers provide higher carrier life time for holes in the n-type substrates, making it possible to fabricate high efficiency solar cells in this type of substrate. Superior properties of n-type substrates have created a tendency towards fabrication of n-type solar cells in photovoltaic market technology considerably. It is even forecasted that photovoltaic (PV) industry will completely shift from p-type systems to n-type systems in the near future.

This technology shift leads to new research activities related to production steps since it should be optimized to get better performance of solar cells.

In this work, we have focused on the development of solar cells based on n-type substrate. Several different routes have been followed and compared with each other. Comparison was made between solar cells fabricated on n- and p-type substrates having a good quality. The conditions yielding high solar cell efficiency was studied in this direction. Both the fabrication and characterization of solar cells were carried out at METU-GÜNAM facilities

Keywords: n-type solar cell, p-type solar cell, float zone silicon wafer, photovoltaic technology

ÖZ

P VE N-TİPİ FLOAT ZON Sİ DİLİMLER ÜZERİNDE ÜRETİLMİŞ GÜNEŞ GÖZELERİNİN KARŞILAŞTIRILMASI

Bilgen, Makbule

Yüksek Lisans, Fizik Bölümü

Tez Yöneticisi : Prof. Dr. Raşit TURAN

Eylül 2013, 91 sayfa

Yüksek elektron difüzyon uzunluğu nedeni ile güneş gözeleri geleneksel olarak p-tipi alttaş üzerinde üretilir. Ancak, yüksek kaliteli float zon silisyum dilimler n-tipi alttaşlarda da yüksek verimli güneş gözelerinin üretilmesini sağlar. N-tipi alttaşların daha iyi özelliklere sahip olması nedeni ile fotovoltaik market, teknoloji araştırmalarını n-tipi alttaşlar kullanarak güneş gözesi üretmek üzerine yönlendirmiştir. Bu araştırmalar sonucunda fotovoltaik teknolojinin p-tipi alttaşlar yerine tamamen n-tipi alttaşlara döneceği bile öngörülmektedir.

Güneş gözelerinden daha yüksek verim elde edebilmek için bu teknoloji değişimi yeni üretim teknikleri ve araştırma alanları ortaya çıkarmıştır.

Bu çalışmada n-tipi alttaş kullanılarak farklı yollardan üretilen güneş gözelerinin kıyaslaması yapıldı ve üretim stepleri optimize edilmeye çalışıldı. Daha sonra ise n-tipi ve p-tipi güneş gözeleri float zon dilimler üzerinde üretilerek karşılaştırıldı. Bu yöntemle daha yüksek verimli güneş gözelerinin elde edilmesini sağlayan şartlar araştırıldı. Güneş gözelerinin üretim ve karakterizasyonu ODTÜ-GÜNAM tesislerinde gerçekleştirildi.

Anahtar kelimeler: n-tipi güneş gözesi, p –tipi güneş gözesi, float zon silisyum dilim fotovoltaik teknoloji

To my mom and dad

ACKNOWLEDGMENTS

I would like to express my deepest thanks to my supervisor Prof. Dr. Raşit Turan for his advice, guidance, help and patience. I would also like to thank him for giving me an opportunity to work in his research group.

I would like to thank Fırat Es for all his guidance, valuable advice and help throughout my thesis studies, and for his friendship and support since the first day that I joined the group. Specially thanks to Emine Hande Çiftpınar for her endless support and great friendship. Discussions with her, morning gossip accompanied by coffee in the early hours of the day have been indispensable for me. I would also like to thank Demircioğlu Couple for all their endless support and sincere friendship. I would like to thank Serim Kayacan İlday for her friendly support, Mete Günöven for his help and support, Gülsen Baytemir, Bilge Can Yıldız, Burcu Barutçu and Engin Özkol and for their friendship. I would like to thank all LAB 118 friends and GÜNAM technicians. I would also like to thank İbrahim Güllü and Doğan Mansuroğlu for their beautiful friendship and support. Other special thanks goes to Zehra Aras, thank you for being such an invaluable friend.

I would like to express my endless thanks and gratitude to Selçuk Bilmiş for his endless academic and technical support, patience and great friendship. Without him, that master period would be more difficult.

I would also like to thank Prof. Dr. Bayram Tekin, who has been a milestone for my education life, for his encouragement, advice and patience.

Finally, I would like to express my deepest gratitude to my family. Nothing would be easy without their love, support and patience. I am also thankful to my husband for his encouragement and endless patience during this period.

TABLE OF CONTENTS

LIST OF TABLES

TABLES

LIST OF FIGURES

FIGURES

LIST OF ABBREVIATIONS

AM1.5G	Air Mass 1.5 Global
Fz	Float Zone
Cz	Czochralski
E_C	Conduction Band Energy
E_V	Valance Band Energy
eV	Electron Volt
KOH	Potassium Hydroxide
IPA	Iso Propyl Alcohol
DI water	Deionized water
Si	Silicon
e-	Electron
h+	Hole
E field	Electric field
SC	Semiconductor
PECVD	Plasma Enhanced Chemical Vapor Deposition
AR	Anti Reflective
BSF	Back Surface Field
SEM	Scanning Electron Microscope

CHAPTER 1

INTRODUCTION

It is a well-known fact that energy is one of the most important issues all over the world. The main source of energy is fossil fuels such as coal, oil or natural gas. However, the most important problem is that these resources are limited and they do not have sustainability in the presence of increasing energy consumption. Increasing demand also give rise to economic problems since unit price of electrical energy is also increasing. Moreover, the conventional fossil energy is detrimental to our natural life because it leads to global warming considerably due to the rate of carbon dioxide emission.

No one can deny that this problem can be tackled through renewable energy source such like solar energy, wind energy, geothermal energy, etc. However, solar energy attracts more attention among the other alternative energy resources since it is clean, abundant and accessible everywhere easily. For this reason, solar energy, in particular photovoltaic (PV) technology is considered to be a promising alternative to conventional sources. Solar energy conversion systems are proven to be a reliable means of generating electricity and heat for domestic and industrial usage.

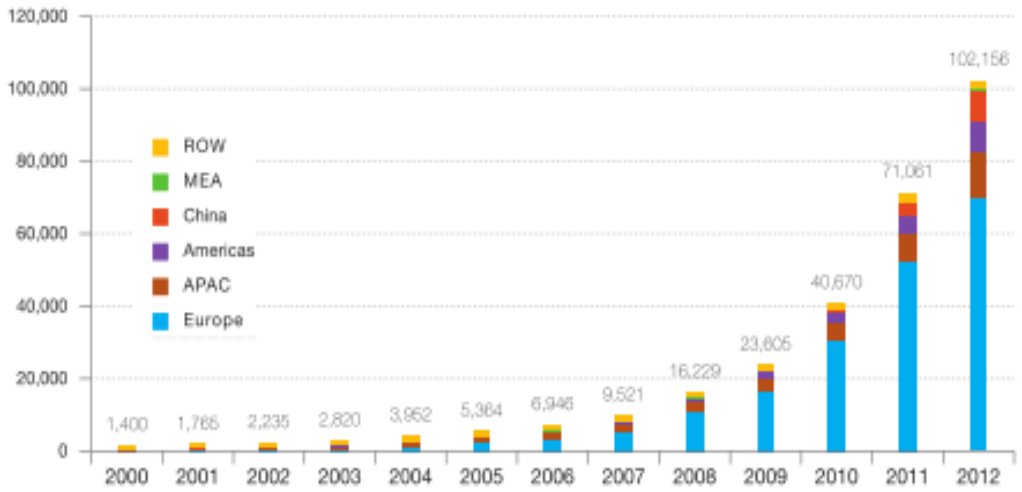


Figure 1. 1 Evolution of Global PV cumulative installed Capacity 2000-2012 (MW) [1]

Nowadays, with the lower cost and higher efficiency, PV technologies are becoming more competitive and gaining more attention especially in developed countries.

To illustrate the enhancement in the PV activities, Figure 1.1 shows the amount of installed PV systems globally. We see that the total PV power exceeded 100 GW at the end of 2012, which represents a significant amount in the power generation.

1.1. Historical Perspective of Photovoltaic Technology

Photovoltaic technology dates back to 19th century. In 1839, Edmund Becquerel realized the photovoltaic effect when he performed an experiment related to electrolytic cell [2, 3]. He firstly showed that materials can respond to the light by generating electric current. Then, photovoltaic effect in solid selenium was observed by William Adams and Richard Day in 1876 [2, 3].Charles Fritts designed first photovoltaic device which was made by using two different metals and by placing selenium between the metals [4]. Then, Grohndal observed the photovoltaic effect in copper-cuprous oxide films [2, 3]. At beginning of the 1900s, Walter Schottky and Neville Mott put forward a theory related to metal-semiconductor barrier [2]. In the following years, many experiments and research were carried out.

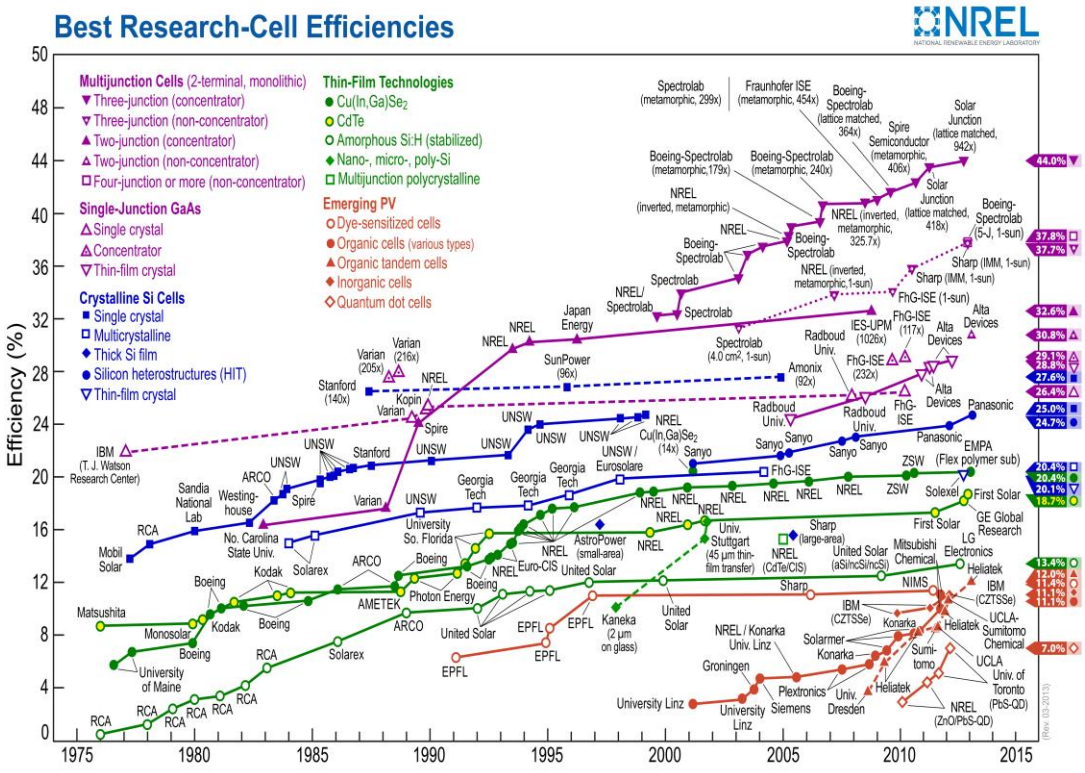


Figure 1. 2: NREL's cell efficiency graph[5]

During 1950s, formation of p-n junction was performed in silicon when the properties of silicon were discovered. Then, in 1954, the first silicon solar cell was produced by L. Pearson, C.S. Fuller and D.M. Chapin in BELL Labs.

Efficiency of that solar cell was nearly 6% [2]. In 1954, p-n junction which formed other elements was manufactured, but silicon dominated all the market technology and this case is still continuous. The number of research conducted in solar energy has been increased especially after the oil-crisis in 1973. For this reason, huge budget has been allocated by government of countries for research.

To reduce the cost and improve the efficiency, alternative materials and methods have been tried through research projects around the world. Thin film materials like amorphous silicon, organic solar cells and III-V semiconductors have been studied to obtain lower cost and/or higher efficiency in solar cells. Figure 1.2 shows the distribution of efficiencies obtained with different material and device systems.

1.2. Photovoltaic Market

Although different photovoltaic technologies based on new material systems have been developed through the years, the oldest technology, that is, crystalline silicon technology has still prevailed in the commercial market due to its superior properties described in section 2.1. Commercial market share of different PV technologies is given Figure 1.3

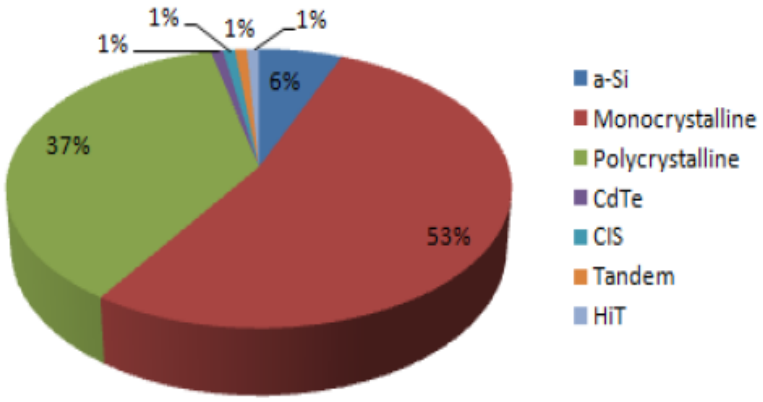


Figure 1. 3: Commercial market shares of photovoltaic technologies[6]

We see the share of c-Si technology is almost 90 % in today's PV market [7]. On the other hand, the level of maturity and development are of interest for the future development. Figure 1.4 compares the efficiency values achieved by the technology today and the maximum achievable values. We see that Si technology has been so developed that it has approached the theoretical limits, while for other technologies, there is a significant

difference between theoretical values and the experimental results [5]. Most of the research activities are focusing on the reduction of carrier loss after the generation.

Solar cell technologies are commonly classified as three main categories. They are called as first, second and third generation solar cells.

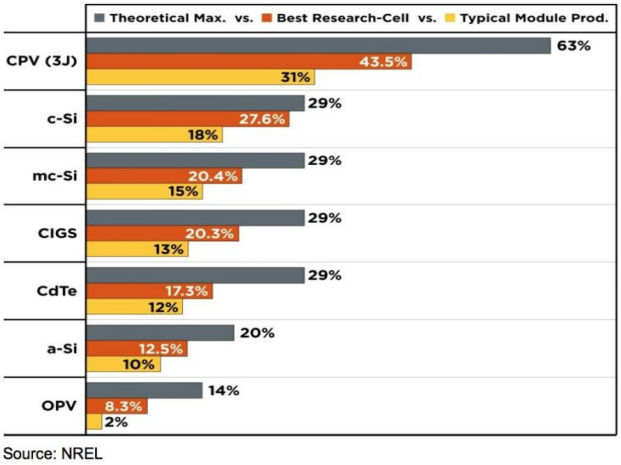


Figure 1. 4: Calculated and recorded solar cell efficiency [5]

The solar cells based on crystalline Si are called first generation solar cells. It is often made of mono crystalline or multi-crystalline silicon wafer cut from the ingots grown by Czochralski and cast growth techniques, respectively. A picture of these cells is shown in Figure 1.5. When we compare mono crystalline silicon and multi-crystalline silicon solar cells we see that the former provides high efficiency because the latter has grain boundaries which cause conductivity degradation. This affects the performance of multi-crystalline silicon solar cell negatively. In mono crystal solar cells, the conduction takes place without any obstacle that leads to higher conversion efficiency. Mono crystalline silicon solar cell technology has reached 25% cell efficiency at lab level. At the same time, the improvement in the wafer growth technology, cost of crystalline silicon solar cells is being lowered, and consequently, crystalline solar cells are securing their dominant position in the commercial market.

In order to move towards more efficient systems, new ideas and approaches are being developed in recent years. One of the most important approaches is to switch from p-type based technology to n-type based solar cell systems. It is well known that n-type Si has better electronic properties due to the higher carrier life time. However, technological difficulties in the solar cell fabrication on n-type wafers have prevented them from being the major technology. As a result, in spite of its rather poor electronic properties, the whole PV industry has been organized according to the requirements of the p-type based solar cell fabrication.

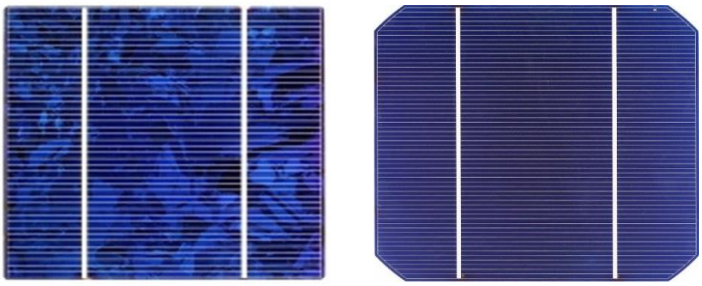


Figure 1. 5: Industrial multi-crystalline solar cell and single crystalline solar cell

In recent years, some new ideas have been implemented to make n-type based cell production more feasible. This has created huge amount of attraction and resulted in increased R&D and production activities. It is even predicted that, the technology will evolve to a mature and superior level so that the PV industry will completely shift from p-type systems to n-type systems in the near future. Figure 1. 6 shows a projection of the market share for these two technologies, made by mono-Si. From this projection, we see that the market will be dominated by n-type material by mono-Si.

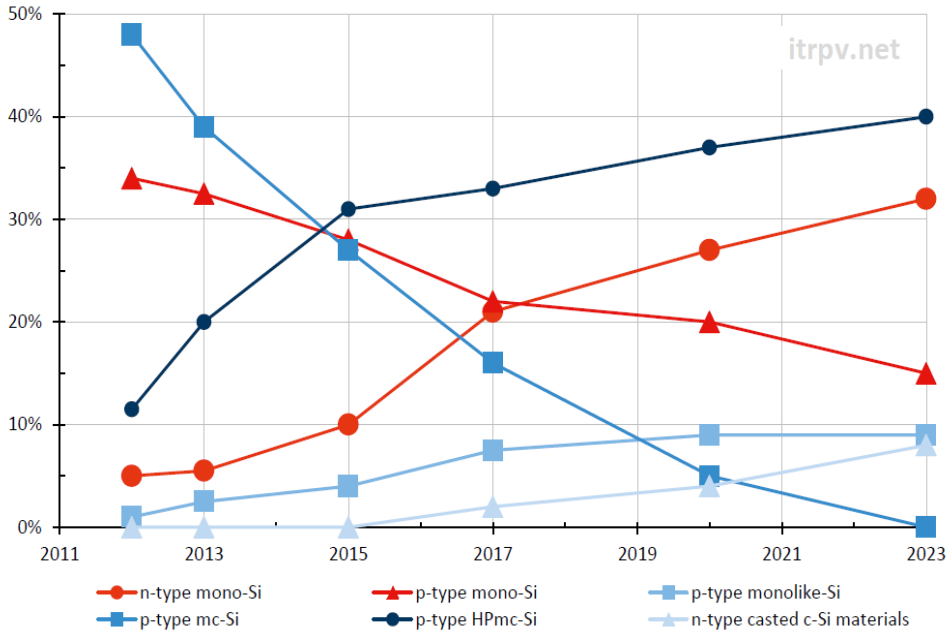


Figure 1. 6: Estimation of market share for p-type and n-type based solar cells [7]

This technology shift requires extensive research activities. New production steps should be designed and optimized to achieve the best conditions. In this work, we have focused on the development of solar cells based on n-type substrate.

Our work represents first attempts carried out at GÜNAM facilities. Several different routes have been followed and compared with each other. We have been able to demonstrate the feasibility of n-type solar cells.

Other technologies based on so called second generation and third generation have not been outside the scope of this study. Just to give short information. Solar cells in the form of thin films are called second generation solar cells.

They have usually lower efficiency compared to the first generation solar cells, but relatively cheaper technology [8]. Thin film systems have lost their market position due to the cost reductions in the c-Si cell technology.

A variety of new material and cell designs is called third generation solar cells. They are expected to have higher efficiencies. However, most of these new systems are still in the R&D level, and far from the industrial application. Many of these approaches have little chance for a commercial success.

1.3. **Summary of the thesis**

The main aim of this study is to understand and optimize the fabrication steps n-type solar cells and compare it with conventional p-type solar cells. This work is expected to form the technology know-how in GÜNAM. This thesis consists of five chapters. First one is an introduction which provides general information on photovoltaic technology.

Chapter 2 presents the basic properties of wafer growth techniques**,** semiconductors and type of semiconductors as well as the fundamental concepts of photovoltaic technology.

Chapter 3 consists of the main experimental part of the cell production. All production steps are covered in this chapter. In addition, theory, experiment and experimental results of each process steps are also discussed in details.

In chapter 4, solar cells produced by different approaches are characterized by means of I-V measurements, quantum efficiency measurements and SunsVoc measurements. In addition, performance of these solar cells is compared her

In chapter 5, this thesis is concluded with a short summary by taking all results into consideration.

CHAPTER 2

AN OVERVIEW OF MATERIALS AND DEVICES WITH IMPORTANCE FOR SOLAR CELL APPLICATIONS

2.1. Float Zone and Czochralski Crystal Silicon Wafer Growth

Although germanium was mostly used as the semiconductor material at the beginning of the solid state devices fabrication in 1950s, after a short period of time, silicon has started to be used instead of germanium due to the superior properties of silicon such as band gap, abundance, thermally grown silicon dioxide. Therefore, silicon has become the major material in solid state devices fabrication. For example, germanium has a low band gap (0.67 eV) which leads to higher leakage current and its oxide is water soluble which is undesirable in solid state device technology and it is less abundant which affects cost of devices. Other semiconductor compounds have similar problems. In contrast to other materials, silicon has a quite suitable band gap (1.12 eV) for room temperature device applications and its oxide that grows thermally is an excellent insulator, which is highly needed for integrated circuit technology [9]. Moreover, silicon is more abundant. When taken all these important properties in to the consideration, silicon crystal is easily seen to be superior for integrated circuit production. Having this impact on the micro electronic circuit industry, the growth of high quality Si single crystal becomes an important issue both scientifically and technologically.

To obtain purified single crystal silicon, two major technologies are widely used: Czochralski growth and float zone growth. The former one is suitable for mass production while the latter one yields higher purity material with slightly higher cost.

SiO_2, pure form of sand called as quartzite, is used as a raw material in order to obtain silicon crystal. It is placed in a furnace with carbon in the form of coke, coal and wood ships and a number of reactions start in the furnace at high temperature [10]. The overall reaction is given by (2.1) [10].

$$SiC\ (solid) + SiO_2\ (solid) \rightarrow Si\ (solid) + Si0\ (gas) + CO\ (gas) \qquad (2.1)$$

Silicon produced in this process is called as metallurgical grade silicon (MGS). It is not pure enough to be used in solar cells or other electronic devices due to high impurity content.

In order to purify it further, it is pulverized and is reacted with hydrogen chloride (HCl), so that trichlorosilane ($SiHCl_3$) in gas form is obtained as follows

$$Si\ (solid) + 3HCl\ (gas) \rightarrow\ SiHCl_3(gas) + H_2\ (gas) \tag{2.2}$$

Pure solid Si is then obtained by fractional distillation using H_2 as given in the following reaction:

$$SiHCl_3(gas) + H_2\ (gas) \rightarrow Si(solid) + 3HCl\ (gas) \tag{2.3}$$

This final product is called electric grade silicon (EGS).The EGS is a polycrystalline material with reduced impurity level. The amount of impurities is nearly in the parts-per-billion range (1ppb = 5 $x10^{13}cm^{-3}$) [9, 10].

The Czochralski method is based on crystallization from the melt, that is, it is solidification from the melt at the interface. The EGS is melted in a crucible which is made up of quartzite at high temperature. Then, the oriented seed crystal is placed in a seed holder. Next, oriented seed crystal is immersed into the melt and seed holder is started to rotate (counter clockwise). In the meantime, crucible is also rotated (clockwise). When the part of the seed crystal is dipped into the melt, seed is pulled out of the melt by using seed holder slowly [10]. During this process, solidification occurs at the interface as shown in the Figure 2. 1. In this way, Si ingot is formed that has same orientation with seed crystal. Pull rate is an important parameter in this technique, since it affects defect formation. Another important factor is the ambient control which is obtained by argon gas which prevents oxidation and evaporation from the melt.

Upon ingot production, wafers are cut from the ingot using rotating diamond saw or more usually using wire saw.

In this process, dopant atoms, phosphorous or boron atoms can be added into the melt in order to obtain n-type or p-type single crystal, respectively. Doping concentration is related to amount of dopant atoms added to the solution.

The Czochralski method is an effective way obtaining the single crystal wafers in large scales. However, the disadvantage of this technique is that single crystal wafers include oxygen impurities considerably since the crucible is made up of SiO_2, which deteriorates the device performance. Oxygen impurities give rise to reducing the minority carrier lifetime [11]. Therefore, it results in reduction of current, voltage and efficiency directly. To get rid of this problem, float zone wafer growth technique has been developed. Using this method, Si wafers that have lower impurities (such as oxygen and carbon) concentration can be obtained.

Float zone technique is considered to be better technique in terms of the material quality. It is, however, more expensive than Czochralski technique. For this reason, Czochralski wafers dominate the commercial market today.

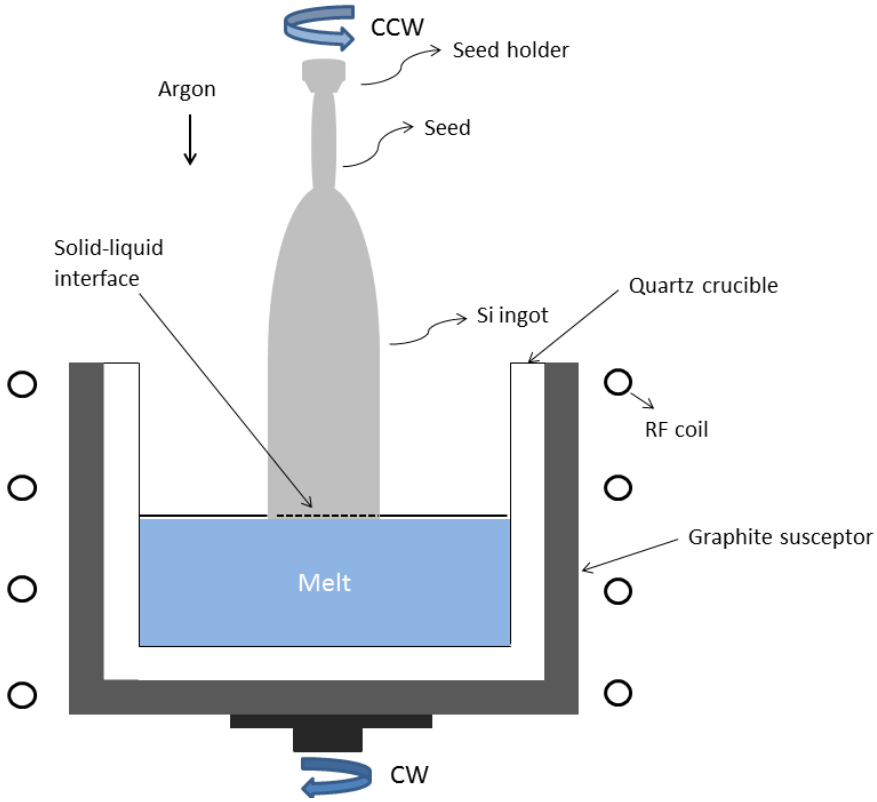


Figure 2. 1: Schematic diagram of Czochralski crystal growth [11]

In the float zone process which illustrated in Figure 2.2, a poly-crystal rod is heated by a RF coil to produce single crystal wafers. The rod is suspended freely without any contact with the crucible, which provides the lower contamination than Cz silicon wafer. The oriented seed is held bottom of the poly-crystal rod and RF heats the rod from bottom to the top. During the heating process, a small zone is molten when the RF passes along the rod. Impurities are disposed to staying in molten region and thus impurities are considerably removed to end of the rod. Since heating is started from the bottom which is placed oriented seed crystal, orientation of molten regions converts into the orientation of seed crystal and molten region becomes solid as a high purity single crystal. Then, by removing end part of the resultant ingot, we obtained purified single crystal ingot. To obtain further purification, melting-solidification cycle is repeated. In the final step the ingot is sliced by saw into the wafers [10, 11].

When the solar cell is produced from Fz single crystal wafer, efficiency of the cell can reach nearly 25% [12]. Fz crystal wafer has an advantage considerably when compared to Cz.

However, the price is high and the diameter of produced wafer is limited to the restriction resulting from the production technique.

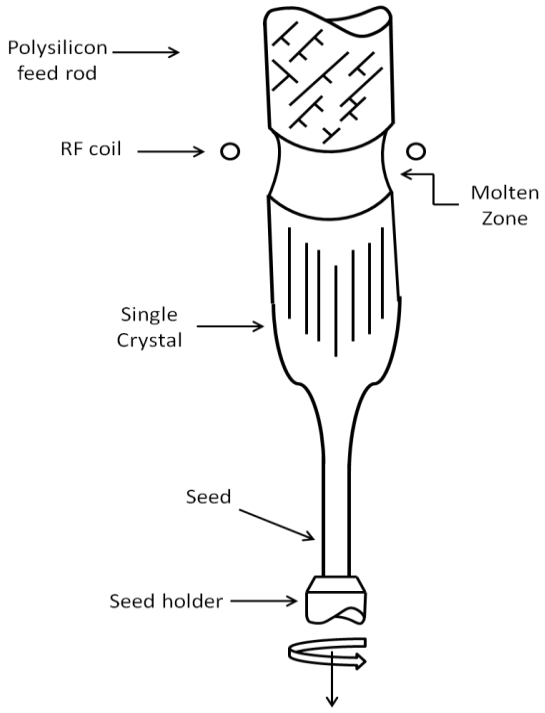


Figure 2. 2 : Schematic diagram of Float-zone crystal growth [11]

2.2. Type of semiconductors

Two main material categories exist with respect to electrical conductivity: conductors and insulators. However, there is another material class that acts as insulators at T=0 K and with increasing temperature, they become thermally activated and act as conductors. It is a characteristic behavior in terms of electrical conductivity and this type of materials are called as semiconductors. They are important in electronic industry since their electrical properties can be controlled by doping or by thermal and optical means.

Semiconductors are called as intrinsic semiconductors if they are not doped intentionally. They are called as extrinsic semiconductors if they are doped with impurity elements which make them p-type or n-type. This property can be expressed using thermodynamical variable called Fermi Level (in the thermodynamic terminology it is called chemical potential). Fermi level is defined as the highest occupied energy level of electrons at T=0 K. If it is inside the electronic band which must be allowed, this material is defined as metal. If Fermi level is inside the forbidden gap at T=0 K, it is defined as insulator. The band which is above of the Fermi level is called conduction band, the band which is below is called valance band. The region between valance band and conduction band is called as forbidden gap which has a very important impact on industrial applications.

2.2.1. Intrinsic Semiconductors

Intrinsic semiconductors can be interpreted with the help of band theory as mentioned above. At T=0 K, valance band is filled by electrons and conduction band is completely empty. There exists a forbidden gap called as band gap. The most familiar semiconductors are silicon and germanium from the group IVA of periodic table (Figure 2.3). Silicon is the most important semiconductor for microelectronic and solar cell applications.

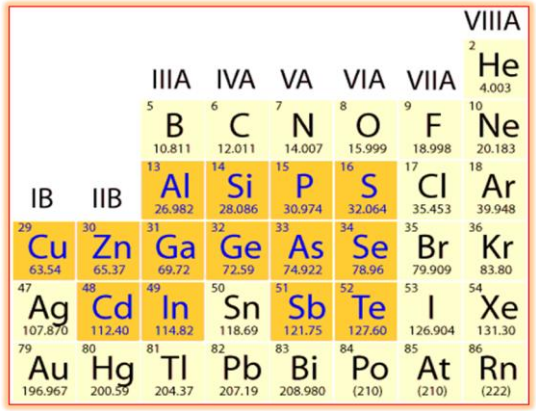


Figure 2. 3: Place of some semiconductors on periodic table

Using elements of groups IIIA and VA of periodic table, compound semiconductor materials like GaAs can be synthesized More semiconductors can be obtained when using elements of IIB and VIA such as ZnS and CdS.

Since isolated silicon atoms have four valance electrons ([Ne] $3s^2p^2$) when they form a crystal structure, each silicon atom is bonded covalently to others, where 4 valence electrons are shared with other 4 neighbors. This makes Si a stable and robust material. When an electron residing in the valance band is excited thermally or optically, it makes transition into the conduction band. (see Figure 2.4)

In the case of optical excitation, only photons whose energy is greater than the band energy can excite an electron to the conduction band. Any semiconductor based optical detection system including the solar cell must satisfy this condition for photo current generation.

Electrons are relatively free in the conduction band. They move around and, if a potential exists, they can be directed to the outside world to generate current. In the case of thermal generation, electrons receiving enough thermal energy can be excited to the conduction band where they can move freely. The thermal energy is provided by the lattice vibration of the atoms.

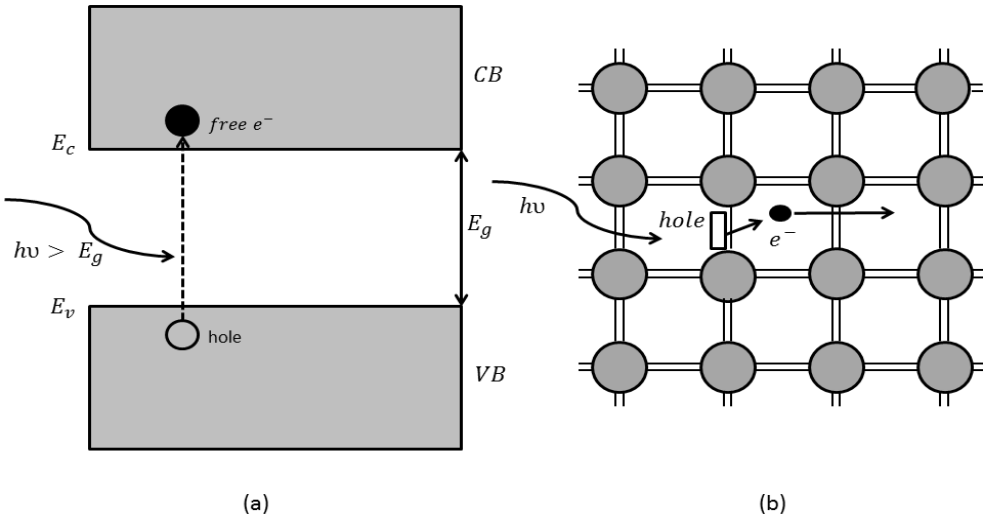


Figure 2. 4 : Energy band diagram of electrical conduction (a), electron bonding diagram of electrical conduction (b) in intrinsic silicon after excitation

The conductivity of a semiconductor is determined by the free electrons and holes in the conduction and valance band, respectively. The conductivity of intrinsic semiconductor is defined as

$$\sigma = n|e|\ \mu_e + p|e|\ \mu_h \tag{2.4}$$

Where the p and n are the number of holes and electrons per cubic meter, respectively. μ_e and μ_h are the mobility of electron and hole, respectively.

However, for intrinsic semiconductors, corresponding to each free electron, holes are created and it is expressed by as

$$n = p = n_i \tag{2.5}$$

Where n_i is the carrier concentration of the intrinsic semiconductor. Thus, (2.4) becomes,

$$\sigma = n_i|e|(\mu_h + \mu_e) \tag{2.6}$$

2.2.2. Extrinsic Semiconductors

Semiconductor device technology is based on control conduction by chemical doping which converts an intrinsic material to extrinsic one. In an extrinsic semiconductor, the conduction is controlled by electrons and holes provided by the dopant atoms.

In the case of Si crystal, each atom has four valance electrons and they bond covalently to the neighboring silicon atom. If an element of group V of periodic table, such as arsenic (As), phosphorus (P) and antimony (Sb) is added as impurity atom into the silicon crystal, four valance electrons are bonded with silicon, fifth electron is left without bonding. That electron stays around the region of impurity atoms and it becomes free easily for a while since the binding energy of fifth electron is so small.

This can be expressed by perspective of band theory. Each fifth electron of impurity atoms which is bound to silicon loosely occupies energy state located forbidden band, around the conduction band. When they gain the required the energy to reach conduction band, they become free electron and jump into the conduction band. Room temperature is sufficient to excite these electrons and this makes it possible the transitions into the conduction band. This type of impurity atoms is called as donor since electrons are donated by excitations through these impurity atoms (Figure 2.5).

In the case of group V doping, since the density of free electrons in conduction band is much greater than density of holes in valance band ($n \gg p$), (2.4) becomes,

$$\sigma = n|e|\,\mu_e \tag{2.7}$$

This type of materials is defined n-type semiconductor. In addition, it is clear that the majority charge carriers are electrons and minority charge carriers are holes. As for Fermi level, it is shifted upwards because donor states is close to the conduction band, but its exact position depends on temperature and concentration of impurity atoms.

If an element of group IIIA of periodic table like boron (B) is doped into the silicon crystal, the opposite effect occurs compared to n-type semiconductors. Impurity atoms have three valence electrons at this time and they share these electrons with silicon atoms. However, one bond is deficient in terms of electron, that is, it is a hole. Electrons of adjacent atoms can displace the hole since it is bound to dopant atom, but binding energy is so small. The hole moves into the crystal from further away the impurity atom by this way. This motion can be generalized to all impurity atoms. Therefore, motion of holes is observed at most.

It can be also explained by band theory. The energy level of these type materials is between conduction band and valance band, close to valance band. The level is called acceptor state since impurity atoms is called acceptor atoms due to acting as electron acceptor. Electrons in valance band can be excited to the thermal excitation and make a transition into acceptor level rather than conduction band. Thus, missing electrons, i.e., holes, increases in the valance band.

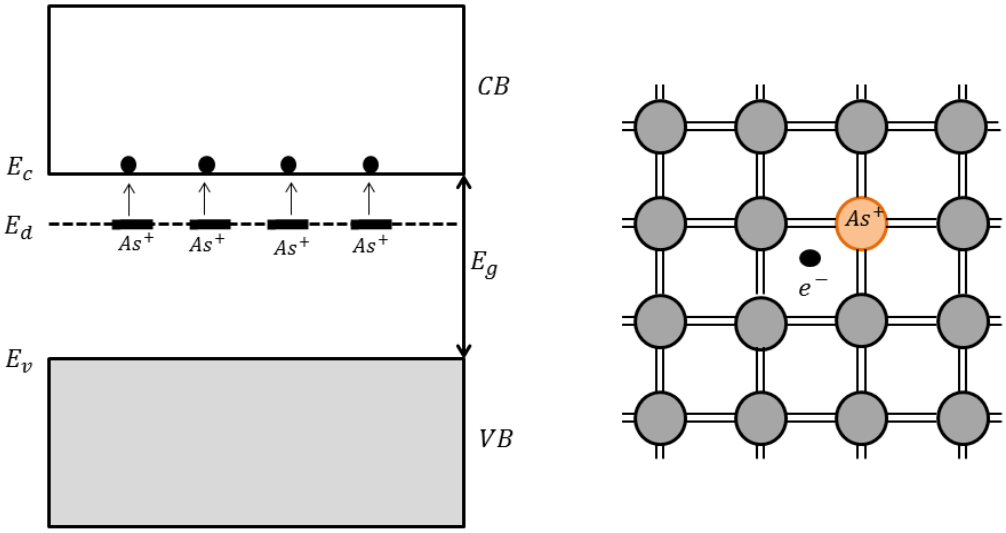


Figure 2. 5: Energy band diagram of n-type semiconductors (a), electron bond structure of n-type semiconductors (b)

When the compare between the number of free electrons and holes, it is clear that majority charge carriers are holes and minority charge carriers are electrons. This type of materials is called p-type semiconductor (Figure 2.6)

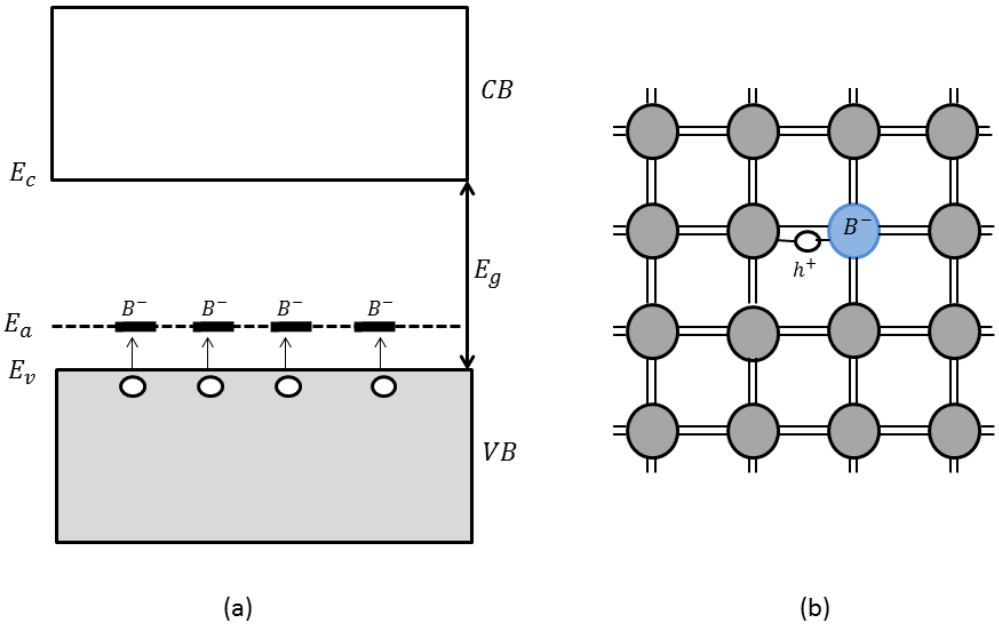


Figure 2. 6: Energy band diagram of p-type semiconductors (a), electron bond structure of p-type semiconductors (b)

Fermi level of p-type semiconductor is the forbidden gap, but it is near the acceptor level. Its exact location is determined by temperature and concentration of acceptor atoms. In addition, for p- type material, conductivity is defined by (2.8) due to $p \gg n$

$$\sigma = p|e|\,\mu_h \tag{2.8}$$

2.3. P-n junction

The operation of almost all semiconductor electronic materials is based on p-n junction. It is also fundamentally important for solar cell operations.

When an n-type material and p-type material are brought together, electron diffuse from n-type region to the p-type region and holes diffuse from p-type region to the n-type region, which results from the concentration gradient.

Although the regions are neutral originally, flow of charge carriers leads to formation of a region, including opposite charged ions. This region is called depletion region. It is apparent that there is internal electric field inside the depletion region from the positive ions to the negative ions, called as built in electric field.

Contrary to diffusion, drift current has always opposite direction, i.e., holes drift into the p region and electrons drift into the n region due to the built in electric field. At equilibrium, diffusion and drift current of charge carriers will be balanced, so that total net current is equal to zero. There is potential difference in p type and n type region at equilibrium. It is called as built in potential.

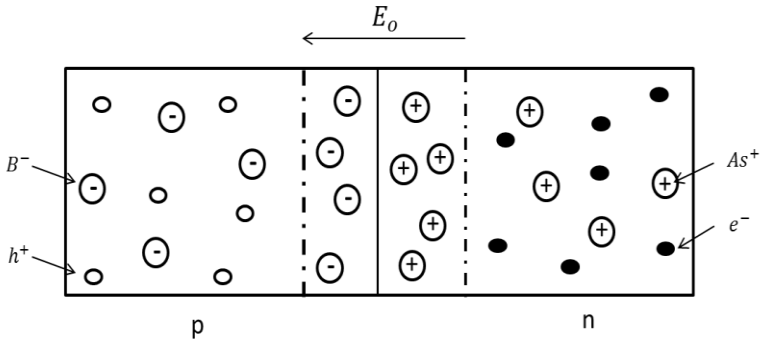


Figure 2. 7: Simple schematic of p-n junction

When the forward bias (positive potential to p-side compared to n-side) is applied to the junction, it disturbs the equilibrium. The applied voltage is directly dropped across the depletion region because the voltage dropped across the neutral region is negligible. Therefore, it reduces the built in potential since it affects directly built in electric field.

For this reason, diffusion current increases considerably and the number of majority carriers increases in bulk region. Therefore, net current flow increases. When the reverse bias is applied to the junction, potential at the junction increases. Therefore diffusion current is even reduced.

From the perspective of energy band diagram, when the p-n junction forms, (Figure 2.8) Fermi levels of them must be aligned at equilibrium. In addition to this, the energy bands are bent since vacuum level must be continuous (Figure 2.9).

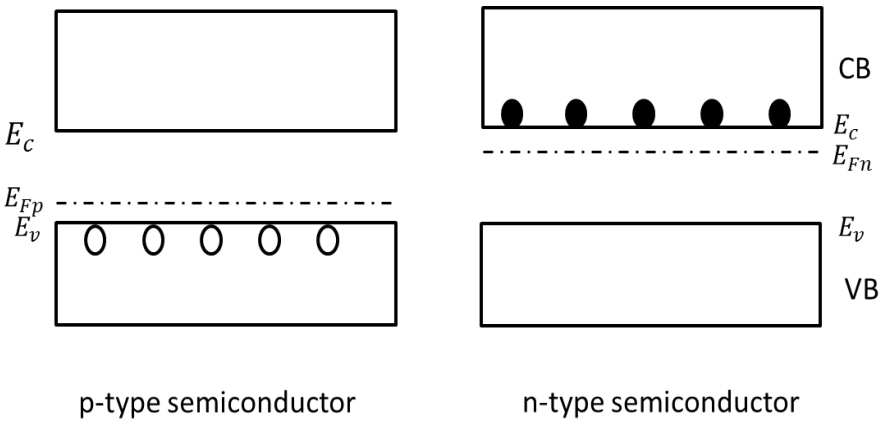


Figure 2. 8 : Band diagram of isolated p-type and n-type semiconductor

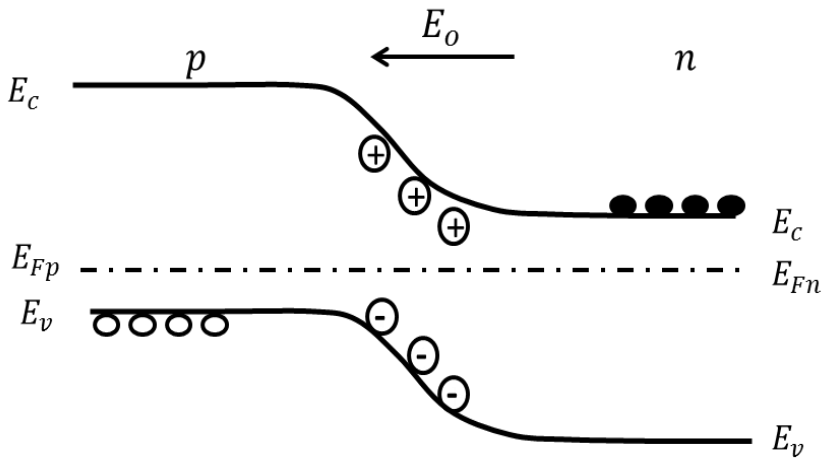


Figure 2. 9: Band diagram of a p-n junction when the two semiconductors are in contact

2.4. Fundamental concepts of photovoltaic technology

2.4.1. Solar Irradiation

Outside the surface of the earth's atmosphere, the solar irradiation is $1367\ \mathrm{W/m^2}$. However, the real value differs slightly since distance between Earth and Sun changes because of the elliptical orbit off the Earth around the Sun. When these are taken into consideration, the average value of irradiance outside the Earth's atmosphere is determined as $1353\ \mathrm{W/m^2}$, which is defined as solar constant. This is not the case when the radiation passes the atmosphere. Sunlight is attenuated considerably, which can result from scattering and absorption by air molecules.

Air mass is a parameter defined as the path length which light travels through the atmosphere and it is given as

$$Air\ mass = \frac{1}{\cos\theta} \tag{2.9}$$

Where θ is the angle between vertical axis and position of the sun. When the incoming light comes along the surface normal, the condition is called as AM0 condition, whereas it is called as AM1.5 condition for the light coming with an angle of 48^{o}. AM1.5 condition is also named as AM1.5G where "G" stands for "global". It means that both direct and diffuse radiation is taken into account. When the spectrum of AM1.5G is normalized, incident power gives $1000\ \mathrm{W/m^2}$.

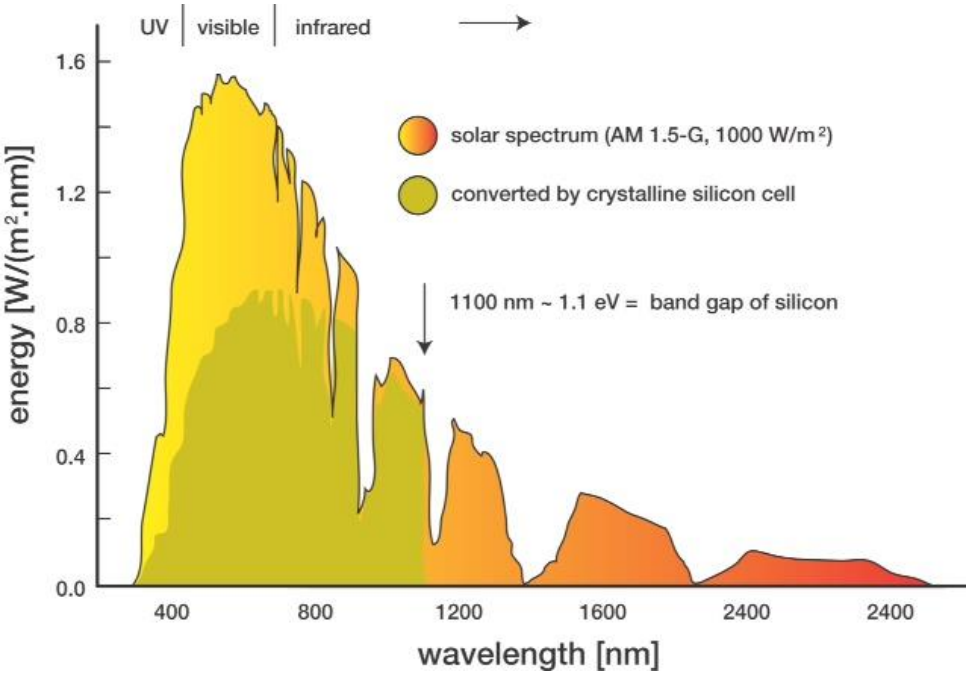


Figure 2.10: Solar irradiation at AM1.5G [13]

2.4.2. Photovoltaic cell parameters

As a p-n junction diode, a solar cell displays the same behavior as a simple p-n junction diode since its mechanism is based on p-n junction. Therefore, the total current of solar cell is expressed by a diode characteristic as given by.

$$I_d = -I_{ph} + I_0\left(e^{\frac{qV}{kT}} - 1\right) \tag{2.10}$$

Where I_d is total current of the solar cell, I_0 is the reverse saturation current, I_{ph} is the photocurrent which is generated under illumination, k is the Boltzmann constant, Vis the applied voltage and T is the temperature.

Under an illumination, I-V curve shifts in the negative voltage direction. Conventionally, I-V curve of the solar cell is characterized using 4th quadrant. I-V curve of a solar cell is given by Figure 2.11. Basic solar cell parameters that can be extracted from the I-V curve are as follows:

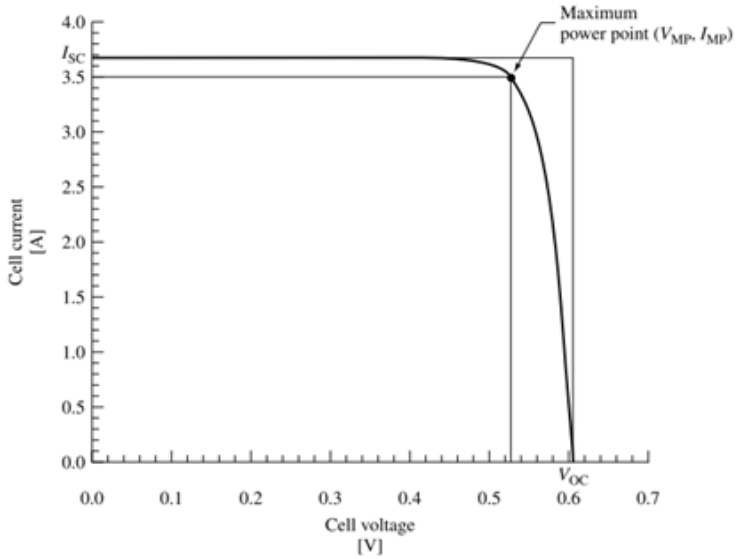


Figure 2. 11: I-V curve of solar cell

Open Circuit Voltage (V_{oc}):

While the current flowing over the surface is zero, difference in voltage between the terminals of the cell is called open circuit voltage. V_{oc} is nearly 0.65-0.70V in high efficiency Si solar cells [14, 15].V_{oc} can be found intersection point of I-V curve with the the horizontal axis.

Short Circuit Current (I_{sc}):

While the voltage difference is zero at the terminals of the cell, the current flowing along the cell is called short circuit current. I_{sc} can be found from the intersection point of the I-V curve with the vertical axis.

Maximum Power Point Voltage (V_{MP}):

The voltage at which the solar cell generates the maximum power is called as maximum power point voltage. V_{MP} is equal to V_{oc} in an ideal solar cell.

Maximum Power Point Current (I_{MP}):

It is defined as the current at which the maximum power is obtained. For an ideal cell, I_{MP} is equal to I_{sc}.

Fill Factor (FF):

The ideal I-V curve of the solar cell must be rectangular since V_{MP} is equal to V_{oc} and I_{MP} is equal to I_{sc} for ideal cell. However, I-V curve of cell deviates from the rectangular shape due to some losses, which is characterized by another parameter called fill factor. Fill factor (FF) is defined as

$$FF = \frac{V_{MP} \times I_{MP}}{V_{oc} \times I_{sc}} \tag{2.11}$$

Efficiency :

The ratio of output power to input power is the definition of efficiency for a solar cell. The input power of the sunlight can be found from the light intensity multiply by surface area. For a standard measurement system, the input power is set to be $1000 W/m^2$ which corresponds to AM1.5 condition described above. Efficiency of cell can be calculated as

$$\eta = \frac{P_{out}}{1000 W/m^2 \times (surface\ area)} \tag{2.12}$$

Where P_{out} is defined as maximum output power and η is efficiency of solar cell.

Shunt Resistance:

Shunt resistance is defined as resistivity against the leakage currents along the p-n junction. It is a measure of the leak current present at the junction across the device area. Shunt resistance must be high in order to prevent leakage current. It can be calculated from slope of I-V curve at V = 0.

$$R_{SH} = \frac{1}{\frac{dI}{dV}}, \quad \text{at } V = 0 \tag{2.13}$$

Low shunt resistance value affects the cell efficiency directly in negative way and it results from production steps

Series Resistance:

Series resistance can be defined the total resistance of the device. It is the sum of different resistive components like, bulk resistance of semiconductor and metal contact resistance. It is an important parameter, since series resistance affects directly solar cell performance. Higher series resistance deteriorates the performance of the cell. For ideal solar cells, series resistance is zero clearly.

CHAPTER 3

PRODUCTION STEPS OF N-TYPE AND P-TYPE Si SOLAR CELLS

In thıs section, the process steps which are performed during the production of p type and n type float zone silicon wafer will be introduced. The aim of process and theory of that will be discussed in this chapter. All the process steps needed to fabricate a solar cell is shown in the flow chart below,

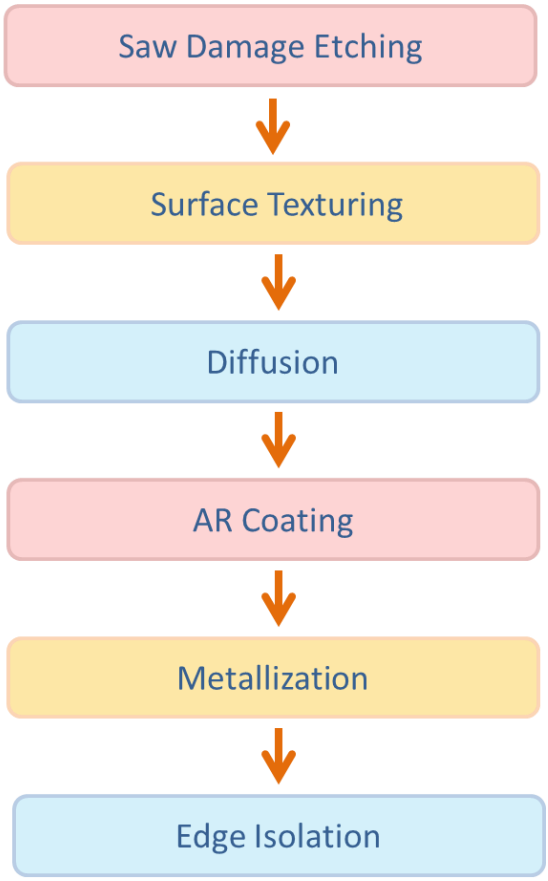


Figure 3. 1: Flow chart of production steps for n-type and p-type solar cells

3.1. Saw Damage Etching:

3.1.1. Aim of Saw Damage Etching

Reducing the reflection on the surface is an essential process in order to increase the efficiency of the solar cell via reducing optical losses. The most effective way of reducing the reflection from the surface and increasing the absorption of the light is to texture the surface and coating it with an anti-reflective layer that also contributes to the electrical passivation of the surface.

It is known that initial surface morphology is not good enough due to the damages created by the wafering process which is usually done by wire sawing. This damaged surface should be cleaned and polished before any other process. Therefore, before the texturing, wafers are processed with an alkaline chemical etching called as saw damage etching. This process makes the surface of the wafer flat and ready for the further texture etching. The saw damage etching is often performed using highly concentrate potassium hydroxide (KOH) solution.

3.1.2. Experiment

In this study, we used boron doped p type and phosphorous doped n type doped wafers produced by float zone technique. Wafers have (100) crystallographic direction, thickness nearly $200\mu m, 1-5\ \Omega$cm electrical resistivity.

Saw damage etching of the as-cut silicon wafers was done by a mixture of KOH and DI water (1 unit KOH and 5 units DI). In this step, a heater and a thermocouple were used to control the temperature. A magnetic stirrer enabled us to obtain homogenous solution.

In this study, as cut wafers were dipped in the KOH solution at 80°C for 1 min., 2 min., 4min. and 6min., respectively in order to remove the surface defects. Then, wafers were cleaned in DI water and dried by N_2. We have optimized the etching process through a series of systematic solution.

3.1.2.1. Reflection Measurement

Reducing reflection from the surface is a crucial for an efficient cell operation. It is important to control the effectiveness of anti-reflective layers. During the fabrication steps, the reflection of the samples is measured after each of the saw damage etching, texturing and anti-reflective thin film covering steps.

The reflection setup consists mainly of light source, chopper, integrating sphere, monochromator, diaphragm & lens, photodetector (UV enhanced Silicon) and lock-in amplifier; as can be seen below Figure 3.2.

Monochromator has input slit and output slit. Output slit of monochromator is attached to a detector and the input slit is attached to the integrating sphere. Integrating sphere is used since textured wafers have both specular and diffuse reflection. It provides to collect all of them. Chopper is placed in front of the lamp, which provides modulation of the light beam. The light beam is focused onto the reflection sample port of the integrating sphere with the help of lenses and a diaphragm. The alignment of the components is important, because the spot size should be smaller than the port size at the reflection port. This can be checked using a piece of paper. When no sample is placed, all light should exit the sphere from this sample port, which would minimize the dark signal. Dark signal should be minimized for better signal to noise ratio.

Two measurements were carried out in order to determine total reflection of sample before the reflection measurement of samples. One is performed by calibration disk. Calibration disk is a reference sample used for complete reflection. The other is done without any sample, which is called as dark measurement. Total reflection of sample is calculated by (3.1).

$$\text{total reflection} = \frac{\text{Measured} - \text{Dark}}{\text{Calibration} - \text{Dark}} \tag{3.1}$$

At the reflection port, the sample is placed at the angle of 8 degrees, so that the specularly reflected light does not leave the sphere from the entrance port, but strikes the inside of the sphere instead. Therefore total reflection is measured (diffuse + specular reflection).

3.1.3. Results of Etching Experiments

We have performed a series of experiments to determine the best surfaces for solar cell production. We studied effect of etch duration by holding the samples in the solution. The resultant surfaces were characterized using SEM and optical reflection measurements.

As seen in Figure 3.3, the surface of bare wafer has saw damage considerably. Samples held in the KOH solution for 0.5 min. and 1 min. have still porous surface so that these time periods were not enough to remove damage from the surface. Sample held in KOH solution for 2 min. has a better surface for solar cell applications despite the roughness left on the surface. Although samples held in KOH solution for 4min. and 6 min. have shiny surfaces, they are not suitable for solar cell due to reduced thickness. Thinner wafers result in reduced absorption of light and they are difficult to handle during production process.

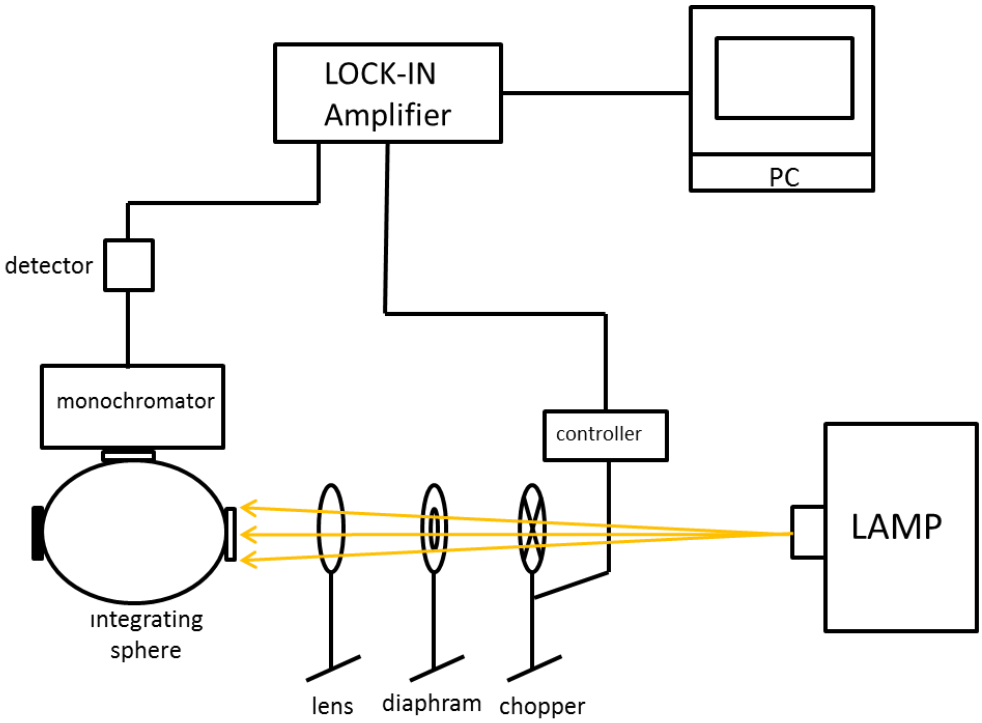


Figure 3. 2: Schematic of reflectance measurement setup

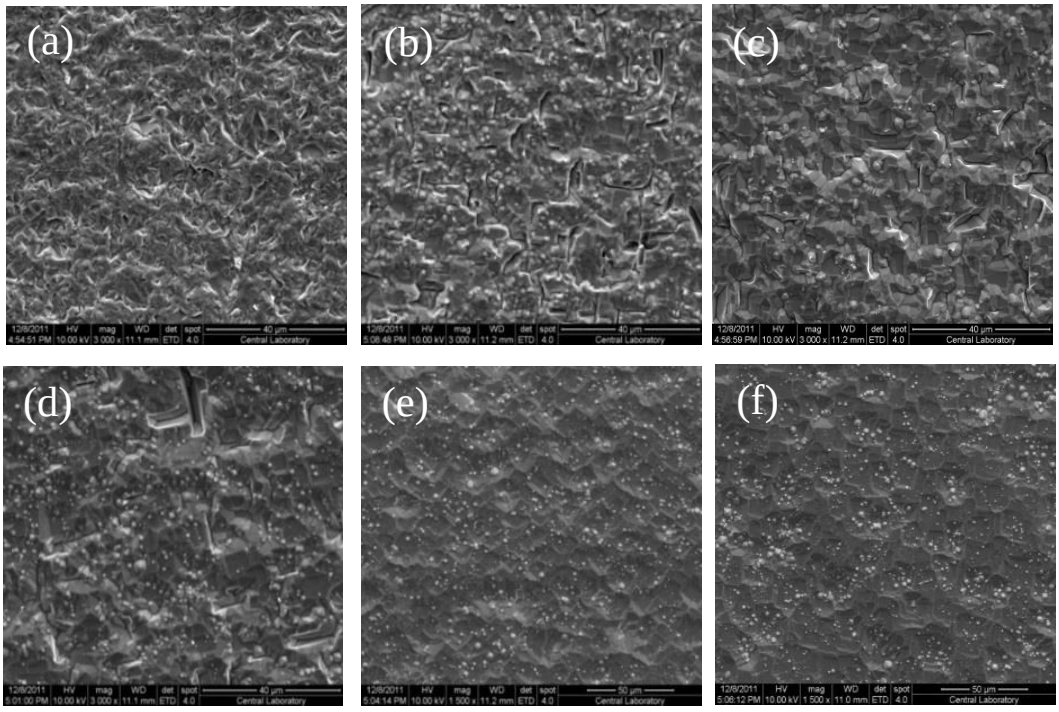


Figure 3. 3: SEM images of bare wafer (a), 0.5min. in KOH (b), 1 min. in KOH (c) ,2 min. in KOH (d), 4 min in KOH (e), 6 min. in KOH (f)

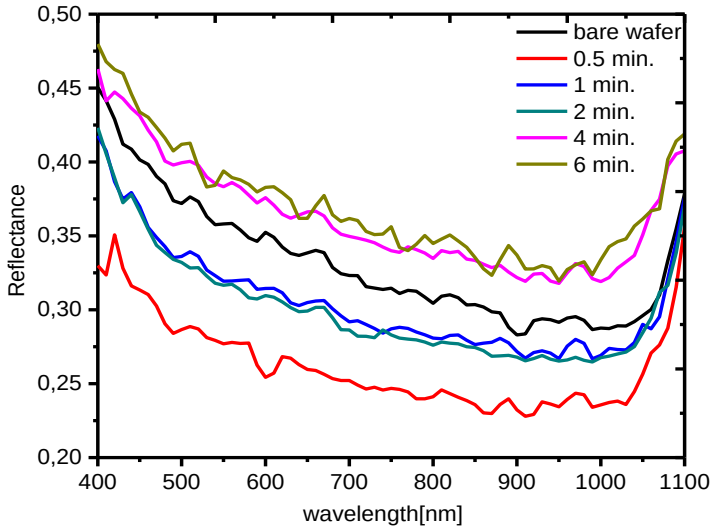


Figure 3. 4: Reflection measurement results of different samples

According to the results shown in Figure 3.4, 0.5 min KOH sample results in lowest reflection among the other samples. However, surface of this sample was not suitable for the texturing process because it needs smooth surface to properly form the pyramids. Therefore, 2 min. KOH process is determined to be optimum for our studies.

3.2. Surface Texturing for Lower Reflection

3.2.1. Theory of texturing

Reduction of the surface reflectance is of a great importance in maximizing the energy conversion efficiency by a solar cell. Reducing reflection will enhance the absorption and creation of electron-hole pairs in the active region of the solar cell, and thus improve the conversion efficiency. One of the techniques that reduce the reflection is to texture the surface of the cell in such a way that the interaction of the light beam with the surface is increased. In principle, texturing should enhance the current output of the solar cell substantially. Therefore, texturing is an important process that should be carried out during the solar cell fabrication.

The aim of texturing is to create a new surface morphology on the silicon wafer that provides multiple light interactions with the cell surface. For single crystalline and wafer-based solar cells, it can be achieved by anisotropic etching using an alkali solution which forms pyramidal shapes on the surface of the silicon wafer. These pyramids are formed randomly on the surface of the silicon due to the etch rate differences of KOH solution for different crystal orientation.

Potassium hydroxide (KOH) has been used to make three dimensional shapes on Si surface and bulk. It is the major chemical etchant material of microelectromechanical systems (MEMS) technology. KOH is highly anisotropic with the extremely low etch rate for (111) plane. When applied to a Si wafer having an initial surface orientation of (100), the surface will ultimately be covered with pyramids having 111 surfaces only. In order to improve the quality of the surface, KOH is used with with isopropyl alcohol (IPA) and deionized water (DI) solution.

Anisotropic etching of the silicon in that solution occurs by means of the following mechanism [16].

$$\text{Si} + 4\text{OH}^- \rightarrow \text{Si(OH)}_4 + 4\text{e}^- \tag{3.2}$$

In this process, etch rate of potassium hydroxide on the (100) and (111) plane is of determining role. During the texturing process, (1 0 0) oriented mono-crystalline wafer is etched in a mixture of KOH, IPA and water with a very high rate until all surfaces become (111) plane. In this way, pyramids on the surface of the wafer are formed as illustrated in Figure 3.5.

Etch rate of KOH solution for silicon substrate;

$$etch\ rate\ (1\ 0\ 0)\ plane / etch\ rate\ (1\ 1\ 1)\ plane\ = 600/1$$

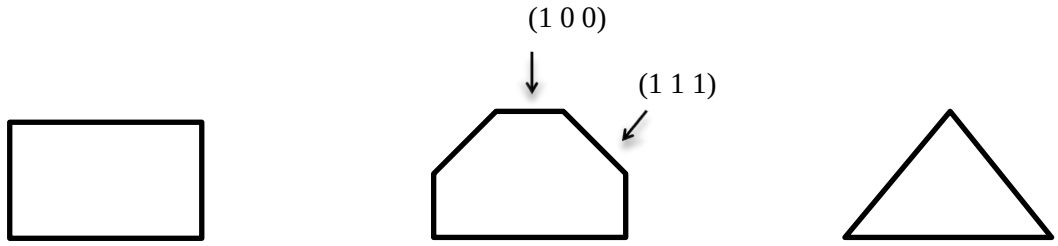


Figure 3. 5: Process of anisotropic etching for (10 0) oriented silicon wafer

The shape of the new surface contributes to increasing the optical length of the light as shown in Figure 3.6. As can be seen in Figure 3.6, the number of reflection on the surface of the wafer and the generation of electron-hole pairs are increased dramatically in this way.

(a) (b)

Figure 3. 6: Reflection of incident light beam from smooth surface (a), from textured surface

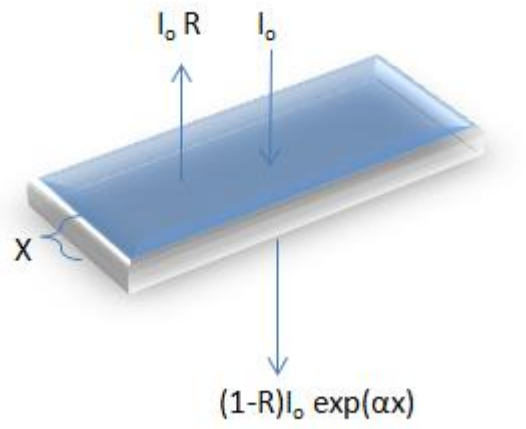


Figure 3. 7: Reflection and transmition of incident light in semiconductor

The amount of optical gain by surface texturing can be calculated as follows: When a beam of photons having an energy E and intensity I_o enter the material and travels a thickness x, (Figure 3.7) the amount of light absorbed by the material is determined by Beer-Lambert law:

$$\frac{dI}{dx} = -\alpha I \tag{3.3}$$

Where α is the absorption coefficient. The solution of this equation is found from

$$I(x) = I(0)e^{-\int \alpha \, dx} \tag{3.4}$$

For uniform α; the equation becomes,

$$I(x) = I(0)e^{-\alpha x} \tag{3.5}$$

For this reason, it can be said that the total reflectivity of the surface is reduced from IR to IR^2 by pyramidal structure formed after the texturing process (0<R<1) as shown in Figure 3.8.

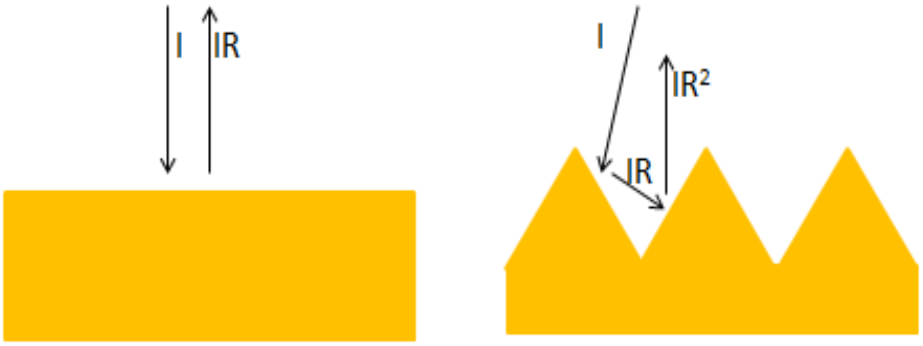


Figure 3. 10: Intensity of reflected light beam

3.2.2. Experimental Procedures

In this step, saw damage etched wafers have been used as sample. On the contrary saw damage etching process, the solution has been prepared as dilute solution relatively.

Texturing of the silicon wafers were done within a 20 liter tank by mixing KOH, DI water and IPA. In this process, thermocouple, heater and magnetic stirrer are used for the control of temperature, setting the desired temperature value and obtaining homogeneous mixture, respectively.

The mixture ratio of KOH, DI water, IPA in the solution, the etch duration and the temperature are all crucially important in reaching the best condition on the surface.

We studied and optimized the solution composition. For this purpose we varied the process parameters as summarized in the table below.

We see that a large number of experiments have been carried out in this experiment. In choosing the process parameters listed in Table 3.1, we analyzed the data available in the literature and considered the physical-chemical properties of the solution. For instance, we know that the IPA is not effective when the temperature is above its boiling point (82.5°C). We also know that KOH solution does not work at temperatures below 70°C. Form the data available in the literature, the concentration of KOH and IPA should not exceed %4 and %15 respectively [17].

Table3. 1: Variables of texturing process

Variables	Lower Limit	Upper Limit
KOH concentration (wt %)	2	4
IPA concentration (wt %)	10	15
Time (min)	35	50
Solution temperature (°C)	75	80

Wafers were first exposed to 1:20 HF: DI solution in order to eliminate the natural oxide on the surface of them, then they were rinsed by DI. Then, they were immersed in to the etch tank for the desired period of time. After all of these processes, they were cleaned by DI again and dried by N_2. During the experiments, speed of mechanical stirrer was constant at 220 rpm.

3.2.3. Results of Texturing Experiments

Figure 3.9 shows SEM images of the process, including 2 wt % KOH and 10 wt % IPA at 75°C for 35 min., 40min., 45 min., 50 min. as seen in the Figure 3.9, 35 minutes is not enough for formation of pyramids since surface is just started for this duration. Pyramids start to be formed at 40 minutes and 45 minutes, but the reflection from the surface is still far from the desired conditions for these samples. As for 50 minutes, pyramids formed on the surface, but their distribution is not homogenous.

Figure 3.10 shows SEM images of the process, including 2 wt % KOH and 15 wt % IPA at 75°C for 35 min., 40min., 45 min.,50 min. We see from these figures that increasing the amount of IPA is worsening the pyramid formation.

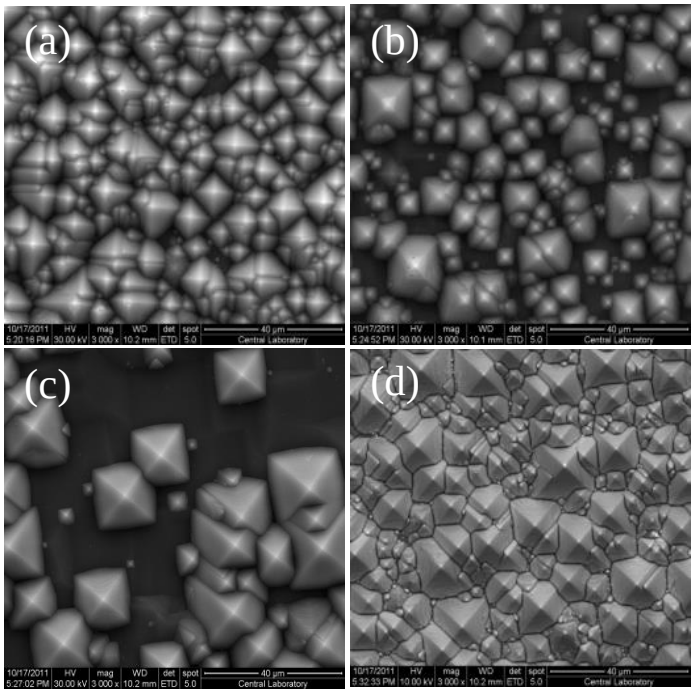


Figure 3. 11: SEM images of samples textured in 2 wt % KOH and 10 wt % IPA solution at 75°C for 35 min. (a), 40 min. (b), 45 min. (c) ,50 min. (d)

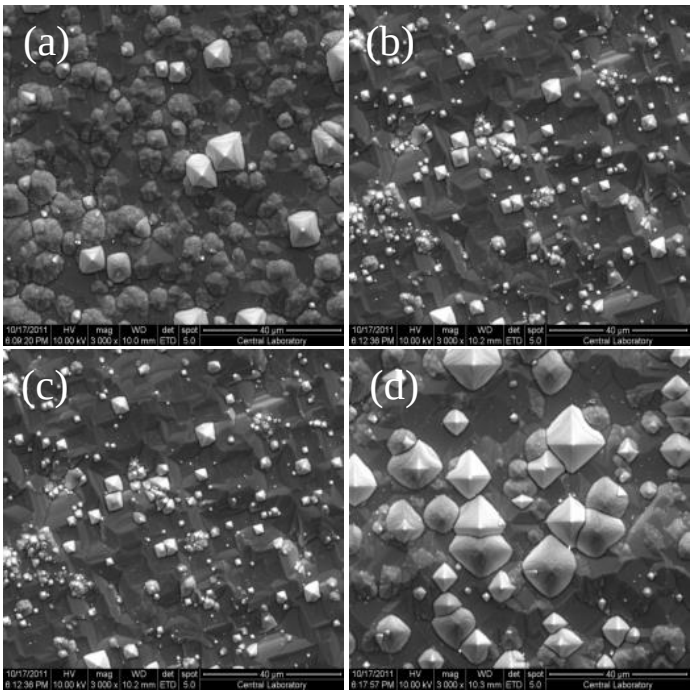
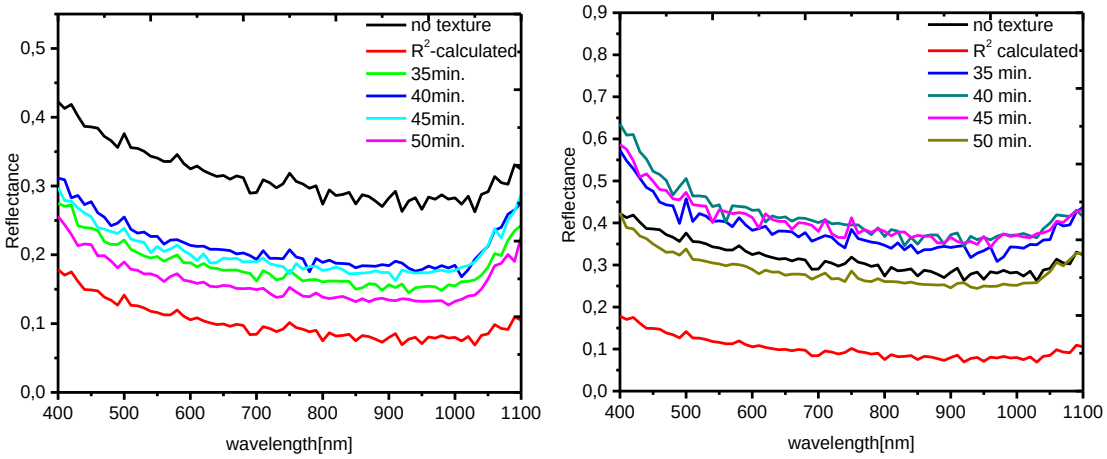


Figure 3. 10: SEM images of samples textured in 2 wt % KOH and 15 wt % IPA solution at 75°C for 35 min. (a), 40 min. (b), 45 min. (c) ,50 min. (d)



(a) (b)

Figure 3.11: Reflection measurement results of samples textured in 2 wt % KOH and 10 wt % IPA solution (a) and in 2 wt % KOH and 15 wt % IPA solution (b) at 75°C for different time periods.

As seen the Figure 3.11, solutions, including 2 wt % KOH-10 wt % 10 IPA and 2 wt % KOH and 15 % IPA do not provide good results in terms of reflection. Samples which belong to both solutions are far away from expected result.

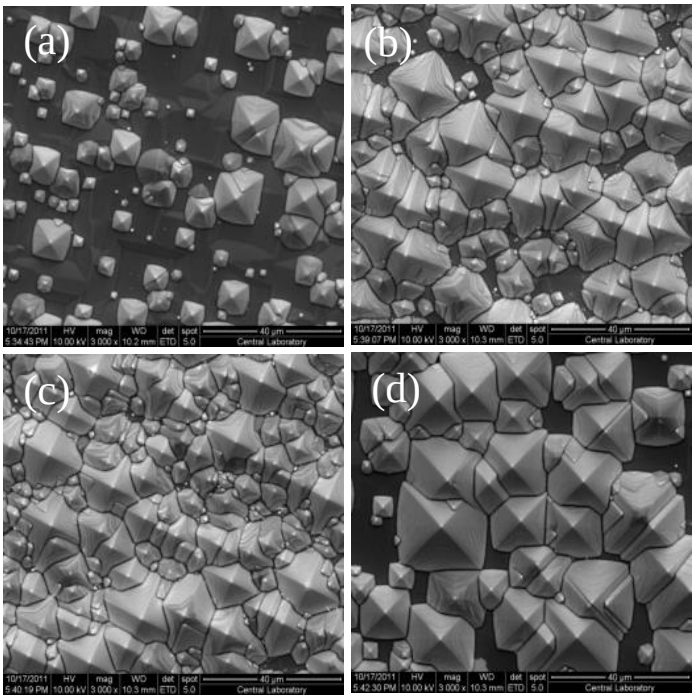


Figure 3. 12: SEM images of samples textured in 3 wt % KOH and 10 wt % IPA solution at 75°C for 35 min. (a), 40 min. (b), 45 min. (c) , 50 min. (d)

Figure 3.12 shows SEM images of the process, including 3 wt % KOH and 10 wt % IPA at 75°C for 35 min., 40min., 45 min., 50 min. It is apparent that 35 minutes and 40 minutes are not enough to form shape like pyramids. Pyramids started to be formed at 45 minutes along the whole surface.

Figure 3.13 shows that higher rate of IPA in solution deteriorates the surface quality compared to results of Figure 3.10. It is observed that pyramids could not start to form in solution, including 3 wt % KOH and 15 wt % IPA at 75°C for 45 min. and 50 min.

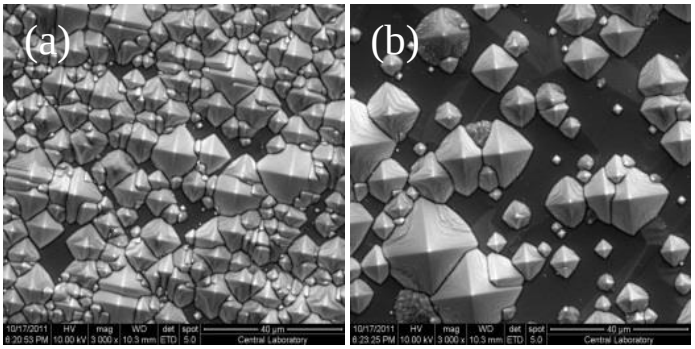
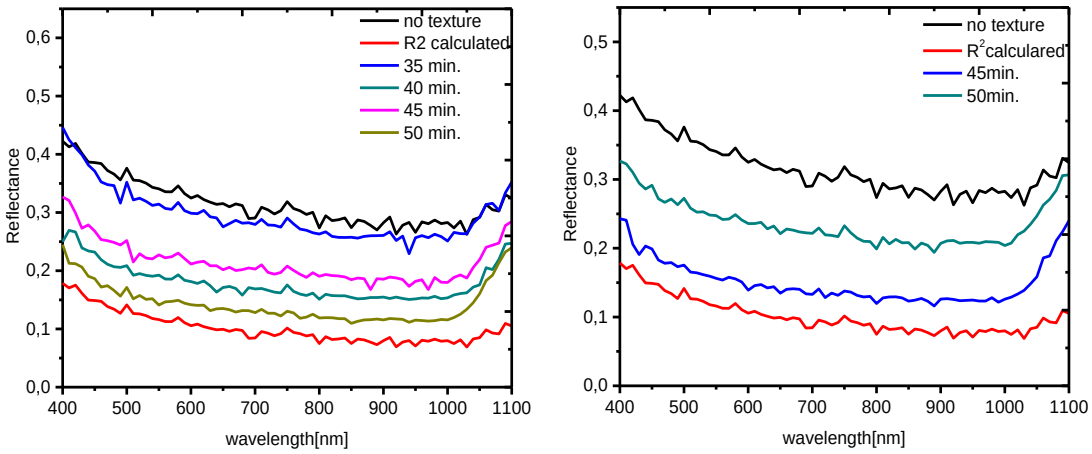


Figure 3. 13 : SEM images of samples textured in 3 wt % KOH and 15 wt % IPA solution at 75°C for 45 min. (a), 50 min. (b)



(a) (b)

Figure 3. 14: Reflection measurement results of samples textured in 3 wt % KOH and 10 wt % IPA solution (a) and in 3 wt % KOH and 15 wt % IPA solution (b) at 75°C for different time periods.

In Figure 3.14, better results have been obtained in terms of reducing reflection when the etch-time was increased. However, when the amount of IPA in solution was increased, reflection from the surface increased since surface of the wafer has lost homogeneity. According to these results, it is concluded that the amount of IPA has affected directly surface morphology and the shape of pyramids.

Figure 3.15 shows SEM images of the process, including 3 wt % KOH and 10 wt % IPA at 80°C for 35 min., 40min., 45 min., 50 min. It is clear that pyramids started to grow on top of each other at 35 min. and 45 min. since reaction occurs faster due to the increased temperature. As for 45 min. and 50 min., pyramidal shapes on the surface could not be preserved. Therefore, increase in temperature affects quality of the surface negatively.

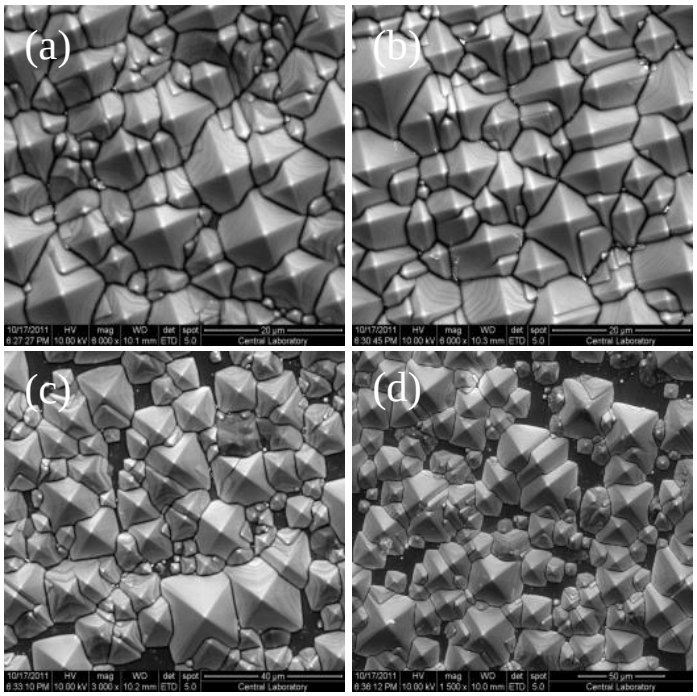


Figure 3. 15: SEM images of samples textured in 3 wt % KOH and 10 wt % IPA solution at 80°C for 35 min. (a), 40 min. (b), 45 min. (c) , 50 min. (d)

Figure 3.16 shows SEM images of the process, including 4 wt % KOH and 10 wt % IPA at 75°C for 35 min., 40min., 45 min., 50 min. It can be expressed that solution behaves aggressively because pyramidal shapes on the surface were annihilated by solution after the 45 minutes. On the contrary to this, pyramids could not be formed on the whole surface by that solution at 35 and 40 minutes.

According to Figure 3.17a, increasing process temperature increased the deviation from the R^2. Similarly as seen Figure 3.17b, increasing KOH concentration also increased the deviation from R^2. is the theoretical limit of surface reflectance

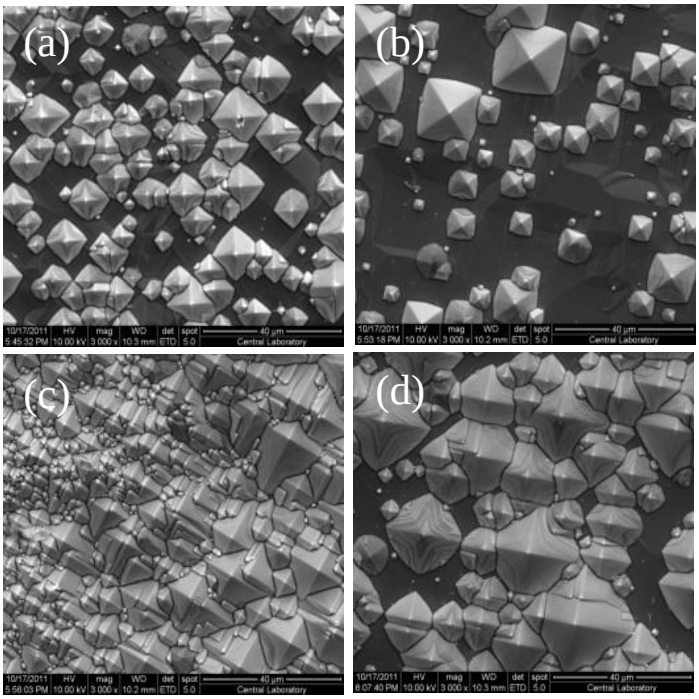


Figure 3.16: SEM images of samples textured in 4 wt % KOH and 10 wt % IPA solution at 75°C for 35 min. (a), 40 min. (b), 45 min. (c) ,50 min. (d)

Taking all SEM and Reflection measurement results into account, it could be said that optimum process temperature is 75°C and optimum KOH concentration is between 3-4 wt % with optimum IPA concentration is 10 wt %. Optimum etch time is found to be 45 minutes.

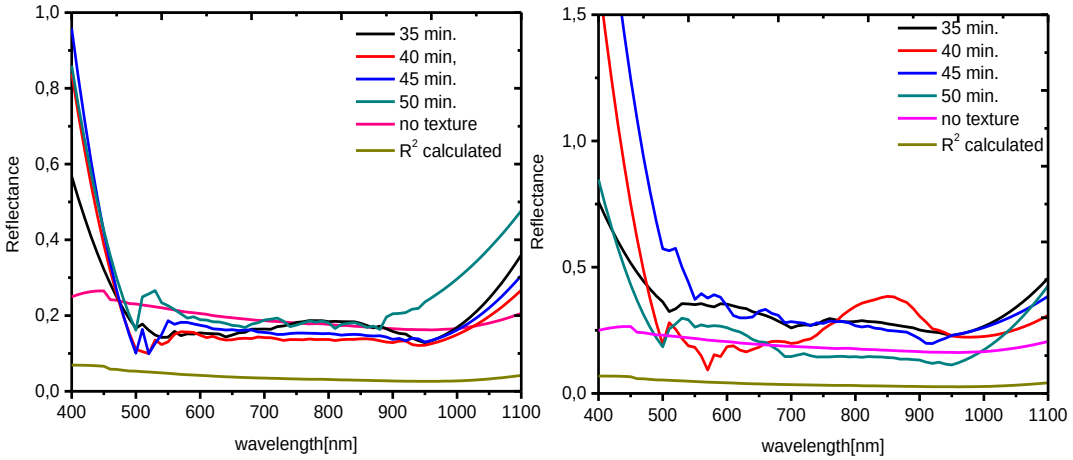


Figure 3.17: Reflection measurement results of samples textured in 3 wt % KOH and 10 wt % IPA solution at 80°C for different time periods (a) and in 4 wt % KOH and 10 wt % IPA solution (b) at 75°C for different time periods.

3.3. Diffusion

3.3.1. Theory

In principle, conversion of the energy in photovoltaic systems stems from separation of the charges. Therefore, formation of p-n junction plays an important role in order to separate electrons and holes generated by light.

Doping is a way to create p-n junction in a semiconductors. It is done by placing dopant atoms like boron or phosphorus into the Si lattice at high temperatures. For this purpose, chemical sources in vapor form are commonly used.

At high temperatures, dopant atoms released from the source diffuse into the semiconductor, and replace the Si atoms substitionally. The diffusion process is driven by differences in concentration of dopant atoms. A thin layer of p (or n) region is formed on the surface of the n (or p) type of the substrate.

In this way, a p-n junction forms at the transition region between oppositely doped regions. The diffusion process is usually expressed by a diffusion constant given in square meters per second and depends on temperature exponentially.

Due to the importance of the process in solar cell production, we would like to give a short review of the diffusion theory here.

There are two main approaches that have been put forward to describe the diffusion process. One is the atomic theory which is related to vacancy and interstitial diffusion. The other one is Fick's continuum theory which solves the Fick's equation.

3.3.1.1. Atomistic Approach

Diffusion from atomistic perspective is migration of atoms randomly in a solid material. Actually, it can be thought as movement of dopant atoms in lattice by means of vacancies or interstitials.

At low temperature host atoms occupy the lattice site. With rising temperature, the lattice atoms vibrate and break bonds and leave the lattice site. A neighboring dopant atom moves into that vacancy site at the same time. It is called as vacancy diffusion.

If atom that is an interstitial position moves into another place that is not a lattice site. This is called as interstitial diffusion. (Figure 3.18)

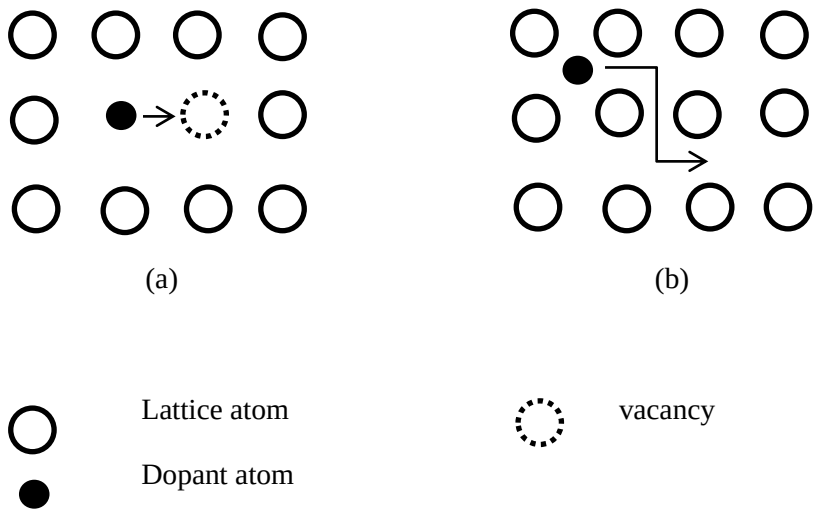


Figure 3.18: Atomic diffusion mechanism. (a) vacancy diffusion mechanism. (b) interstitial mechanism

3.3.1.2. Fick's Laws of Diffusion

Fick's law of diffusion is the continuum approach which is based on concentration gradient of the particles in medium. This approach is useful to describe the standard diffusion processes like to ones used in semiconductor technologies. The diffusion takes place when there is a difference in concentration of atoms between two regions. When this condition occurs a particle flux from the high concentration region to low concentration region is observed. J stands for diffusion flux [18]. A more detailed description of the diffusion based on the Fick's laws is given below.

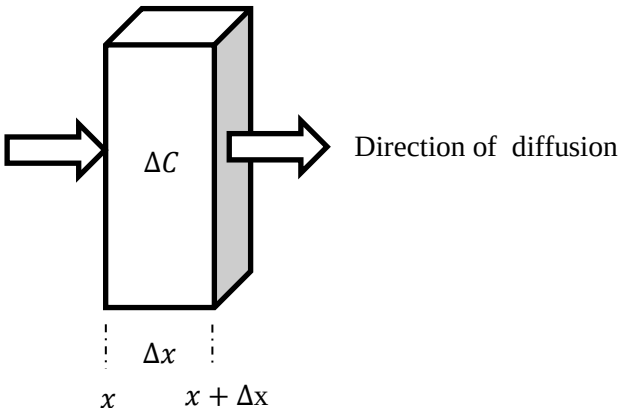


Figure 3.19: Diffusion along the thin plate

Diffusion is analyzed under two situations, one of which is the steady state diffusion, that is, diffusion does not depend on time. In this case, it is assumed that differences of concentration , ΔC, at the interval Δx that is so small. Thus; concentration gradient can be defined as,

$$\frac{\Delta C}{\Delta X} = \lim_{\Delta X \to 0} \frac{C(X + \Delta X) - C(X)}{\Delta X} \tag{3.6}$$

$$\frac{\Delta C}{\Delta X} = \frac{C(X + \Delta X) - C(X)}{X + \Delta X - X} \tag{3.7}$$

$$\frac{\Delta \mathrm{C}}{\Delta \mathrm{X}} = \frac{\mathrm{dC}}{\mathrm{dX}} \tag{3.8}$$

Flux is directly proportional to concentration gradient. Therefore, diffusion flux can be defined by,

$$\mathrm{J} = -\mathrm{D}\frac{\mathrm{dC}}{\mathrm{dX}} \tag{3.9}$$

This equation is known as Fick's fist law. D is diffusivity which is proportionality constant and unit of that is m^2/s. C is the carrier concentration. Basically, concentration gradient leads to diffusion is the driving force since dopant atoms tend to move from high concentration region to low concentration region.

The other one is non-steady state diffusion which means that diffusion depends on time. Using continuity equation, Fick's second law is obtained at this time.

$$\frac{\partial \mathrm{C}}{\partial \mathrm{t}} = -\frac{\partial \mathrm{J}}{\partial \mathrm{x}} = \frac{\partial}{\partial \mathrm{x}}\left(\mathrm{D}\frac{\partial \mathrm{C}}{\partial \mathrm{x}}\right)$$

If the diffusion constant does not depend on x, we obtain the (3.9).

$$\frac{\partial \mathrm{C}}{\partial \mathrm{t}} = \mathrm{D}\frac{\partial^2 \mathrm{C}}{\partial \mathrm{X}^2} \tag{3.10}$$

This expression becomes meaningful when considering boundary conditions. To solve this equation, initial and boundary conditions have essential role. Therefore, two important situations should be taken into consideration. One of them is constant surface concentration diffusion. The other one is constant total dopant diffusion. Of the two cases, the former can be thought that the source is held constant concentration on the surface of semiconductor during the process. The latter can be thought that there is a finite source and it is deposited on the surface of semiconductor and then all dopant atoms diffuse into the semiconductor during the process.

Constant Surface Concentration:

The boundary conditions,

$$C(x,0) = 0, C(0,t) = C_S, C(\infty,t) = 0$$

The differential equations can be solved by using Fourier transformation. (steps of solution are given Appendix A).

The result of (3.10) is obtained in the form of complementary error function.

$$C(x,t) = C_s \operatorname{erfc}\left(\frac{x}{2\sqrt{Dt}}\right) \tag{3.11}$$

Constant Total Dopant Diffusion:

Boundary conditions,

$$\int_0^\infty C(x,t)dx = Q, \quad C(\infty,t) = 0$$

The result of (3.10) is obtained depending on exponential function

$$C(x,t) = \frac{Q}{\sqrt{\pi\, Dt}} e^{\frac{-x^2}{4Dt}} \tag{3.12}$$

In semiconductor technologies, diffusion process is usually done in two steps, one of which is pre-deposition step and other one of which is drive-in step.

Dopant atoms diffuse into the surface of the semiconductor in pre-deposition step and they create the constant surface concentration condition. Then, the next step is the drive-in at which the dopant atoms penetrate deep into the semiconductor with a high temperature annealing. This case corresponds to the constant total dopant condition.

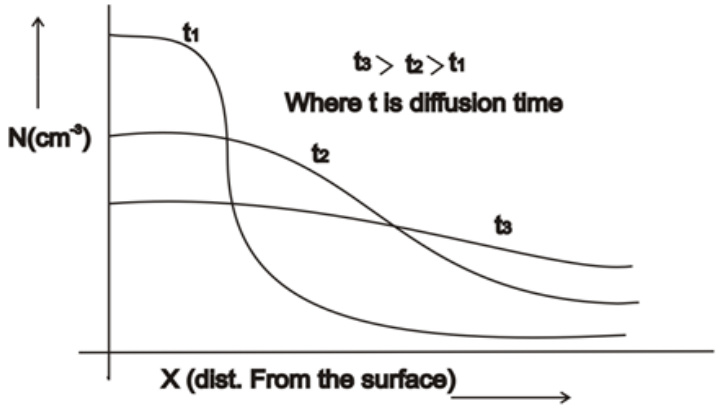


Figure 3.20: Concentration distribution of drive in diffusion [19]

3.3.2. Experimental details of diffusion process for n-type and p-type solar cells production

Diffusion of dopant atoms is carried out in a quartz tube furnace at high temperature (Figure 3.21). Semiconductor wafers are placed in furnace and they are exposed to gas mixture, including dopant atoms. Boron is preferred for p-type doping while phosphorus is preferred for n-type doping generally since these elements have higher solubility in silicon. BCl_3 is mostly used as a liquid source for p-type doping, whereas $POCl_3$ is used as source for n-type doping. For example, during the phosphorus diffusion, these reactions take place in a furnace [10]. (3.13 and 3.13)

$$4POCl_3 + 3O_2 \rightarrow 2P_2O_5 + 6Cl_2 \quad (3.13)$$

$$2P_2O_5 + 5Si \rightarrow 4P + 5SiO_2 \quad (3.14)$$

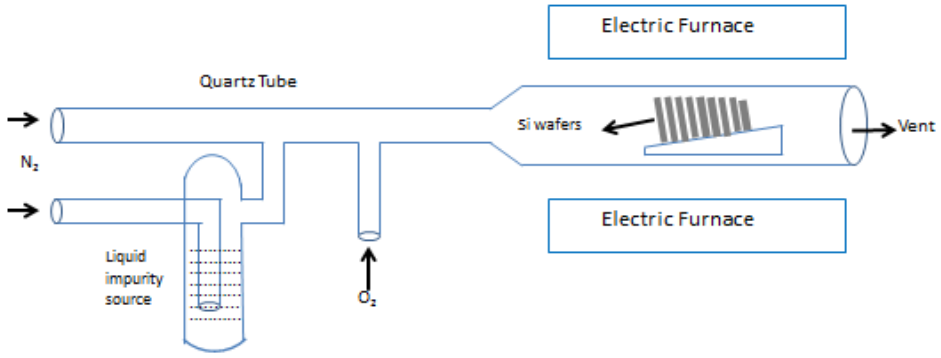


Figure 3. 21: The schematic diagram of quartz tube furnace system for doping process

Phosphorus is released by means of this way and it diffuses into the silicon wafer.

3.3.3. Production Approaches for n-type Solar Cells: Results of Experiments

Solar cell based on p-type crystalline silicon is more common in market technology since fabrication of p-type solar cell is performed easily and the needed knowhow has been reached up to now. However, solar cell based on n-type crystalline silicon is attracting a lot of attention in recent years because of its potential for higher efficiency values resulting from higher minority carrier lifetime and higher tolerance to metallic impurities. Efficiency values exceeding 20% have already been obtained with n-type solar cells.

However, there are some difficulties in fabrication process of n-type crystalline silicon. For example, boron (B) doping is necessary to form p layer and it is highly difficult process [20, 21]. Getting rid of these difficulties is needed to improve n-type crystalline silicon solar cell technology. In this work we aimed to generate knowledge and methodology for the fabrication of n-type solar cells. We also processed p-type solar cells in a similar fashion for comparison.

Production of p-type solar cell has been standardized in industry, which provides sufficiently high efficiencies. However, for n type solar cell, there is not a standard process resulting in high efficiency values for large area applications.

Therefore, in this work, different production methods have been performed to produce n-type solar cell. In this section, the formation of p-n junction will be covered. The doping process will be discussed in detail.

Firstly, fabrication of p-type solar cell process has been done by using standard fabrication processes.

Then, corresponding to this, the same process has been done to the n-type crystalline silicon. P-n junction formation is studies on these samples. Flow chart of the standard fabrication steps are shown in Figure 3.22 (a). In this process double side textured p-type wafers were used and they were doped with phosphorus (P) in doping furnace. . Then, p-n junction was obtained in each wafer. Doping type and level is determined by the measurement of sheet resistances on the both surface of doped wafers and type of surfaces of wafers using four-point probe. Both surface of the p-type wafers showed an average resistivity of 50Ω/□ after the diffusion. It means that double side textured wafers were doped with impurity atoms.

However, doping both surfaces is not desirable. We need to make one side of the wafer p-type. This condition is achieved after the back side metallization is completed. Also the back side should be doped heavily to reduce the recombination. So called back surface field (BSF) must be created to prevent recombination of minority carrier at rear surface. Since metallization of the rear side is done by aluminum, which is a dopant for Si, it converts n doped region into p-type after the firing process which enables Al atoms to diffuse into the crystalline silicon from the back side [22]. By this way, the structure of n-p-p+ is obtained to produce p-type solar cell. In the metallization section, this process will be described in a more detailed way. To produce solar cell based on n type crystalline silicon, different ways have been followed in order to obtain high efficiency from solar cell since formation of p-n junction is difficult relatively.

The first approach is the standard process of p-type wafer. It was thought to be a useful process for also n-type wafers.

Figure 3.22 (b) shows the flow chart of the standard process and cross section of wafer. N-type wafers are first doped with phosphorus like the process of p-type wafers. The sheet resistances of the both surfaces of wafers are checked after diffusion process. In our experiments, we obtained resistivity values around 50Ω/□, showing that wafers were properly doped. However, p-n junction could not be obtained because the types of wafers were n-type and substrate doped with phosphorus resulting in n-type. Therefore, to obtain p-n junction, rear surface of doped wafers have been covered with Al paste and fired. By this way, p-n junction is obtained. In 1st approach, p-n junction is close to the rear contact.

Al is not preferable in metallization of n-type materials since Al belongs to IIIA group of periodic table and it can convert n-type region into p-type region by means of diffusion. Therefore, metallization is also a difficult step in n-type solar cell production. Silver (Ag) has been applied as an alternative to Al in metallization process in rest of this study.

However, properties of silver are not suitable for creation of back surface field at rear surface. For this reason, it was decided to obtain p-n-n$^+$ in rest of the study when the positive effect of BSF on the efficiency of solar cell is taken into consideration [20].

To form p-n-n+, the production steps of the second approach is shown in the Figure 3.23. N-type wafers have been doped with boron. After doping process, the doping types of both sides of the wafers were checked and both sides were measured to be p-type. Then, resistances of both sides have been measured by using four point probe. The average resistance results are shown in Figure 3.24.

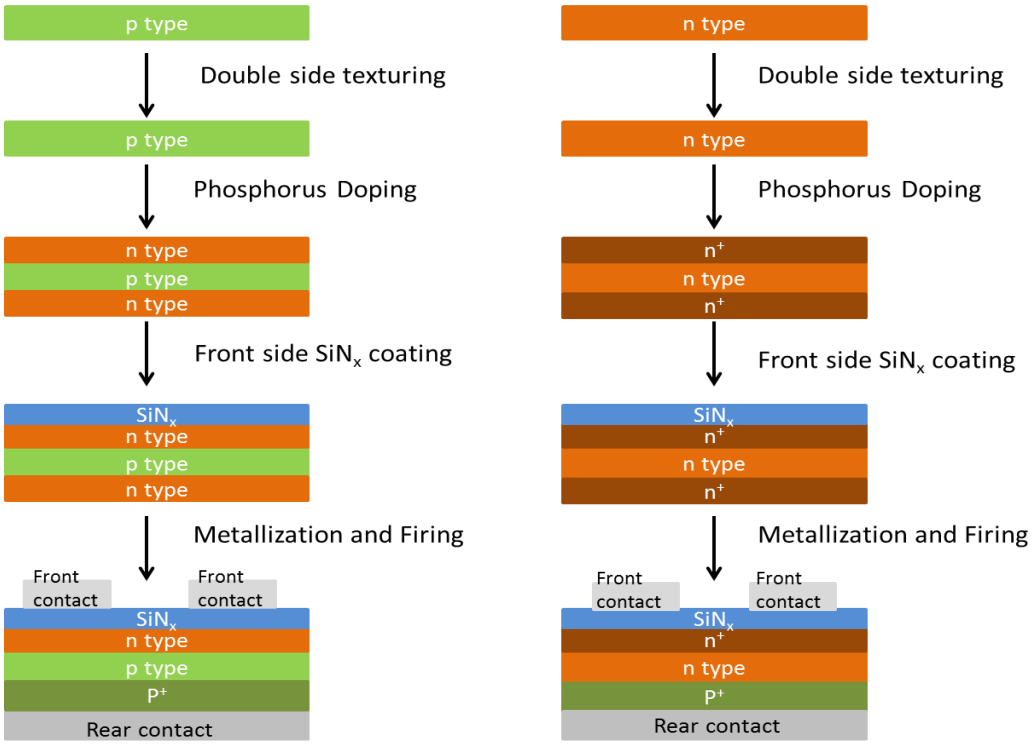


Figure 3.22: Process Flow of 1st approach for p-type wafers (a), n-type wafers (b)

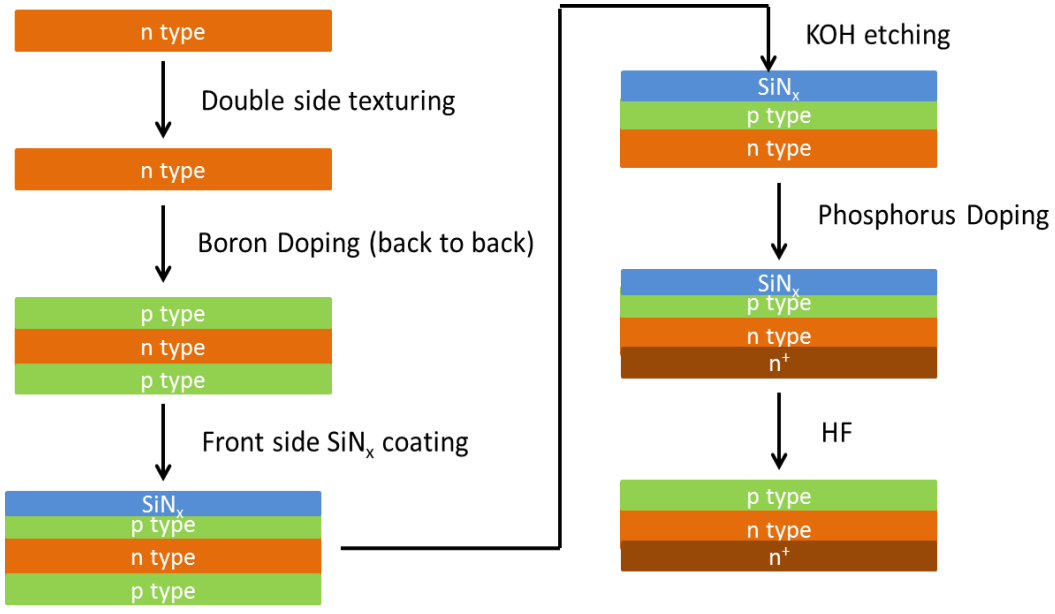
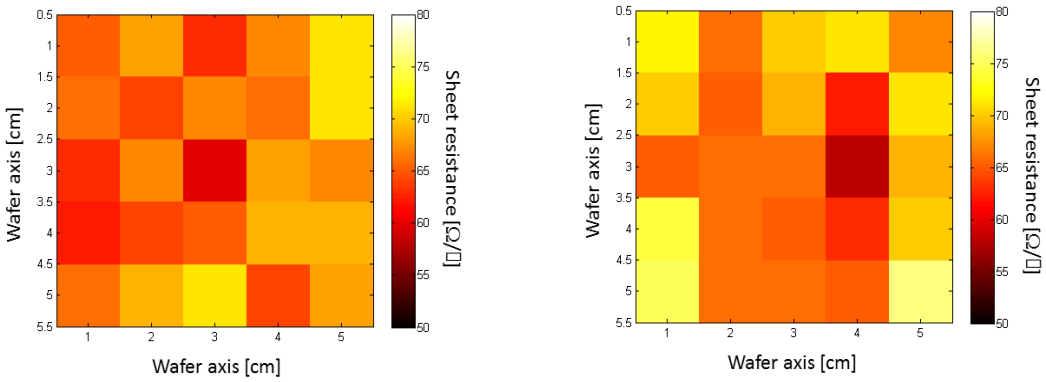


Figure 3. 23: Process Flow of 2nd Approach

Boron doped silicon wafers are desired to have sheet resistance values about 60Ω/□ in literature [23]. As seen in Figure 3.24, in this work, the resistance of front and rear sides of doped wafers were measured to be approximately 65 and 70 Ω/□, respectively.

To prevent negative effect of parasitic junction and to create n+ layer, p-type layer at the rear side of the wafer is needed to be etched by using KOH solution, at high temperature ~80°C. Therefore, to preserve front surface of wafers during etching, silicon nitride has been deposited by plasma enhanced chemical vapor deposition (PECVD) and then etching in KOH solution at 80°C, but for different time periods 30 seconds, 60 seconds, 120 seconds and 240 seconds was applied. This work has been done to optimize the etching duration in solution.



(a) (b)

Figure 3. 24: Sheet resistance values mapping of front side of n-type wafers (a), rear sides of n-type wafer (b)

After that, the type of back side of the wafers has been checked and the resistances of back sides have been measured from different regions. The results of sheet resistances are shown in Figure 3.25.

As seen Figure 3.25, resistance increased for 30 seconds and 60 seconds processes, and reached a constant value around 150-160 Ω/□ for120-240 seconds samples. Up to 120 seconds, we still have a p layer at the back side of wafers. However, when p-layer was completely etched from the back surface, a constant resistance value was reached.

Then, to obtain p-n-n+, back sides of these wafers have been doped with phosphorus again. Then, silicon nitride on front sides of the doped wafers was removed using HF solution and the sheet resistance measurements were done from both sides of wafers. The results of sheet resistance measurement for 30 and 60 seconds samples are shown Figure 3.26.

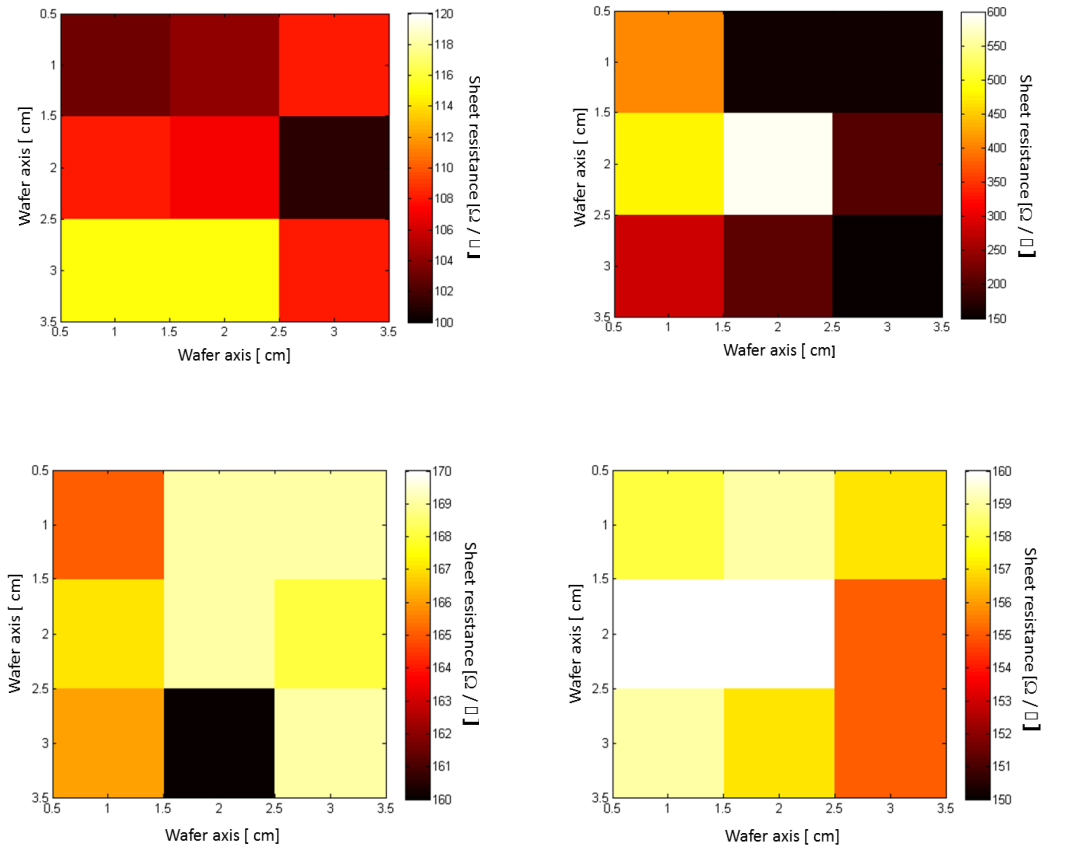


Figure 3. 25: Sheet resistance values mapping of back sides of n-doped wafers after KOH solution in (a) 30 sec., (b) 60 sec., (c) 120 sec., (d) 240 sec.

Figure 3.27 also shows the results of sheet resistance measurement for 120 and 240 seconds samples. Figure 3. 26 and Figure 3. 27 have shown that silicon nitride prevented the front side of wafers from doping and chemical solution since the sheet resistance of front side of wafers remained same after etch experiment constant. rear side of the wafers doped with phousphorus.

As a result, we observed that samples held in solution for 120 sec. and 240 sec. have shown best results clearly since they have lower resisitance values. It means that 120 sec. and 240 sec. samples have been doped highly, which is desirable for BSF formation.

After these processes, metallization on the front and back surface of the wafers was performed through thermal evaporation without anti-reflective coating in order to measure I-V characteristics both dark and under illumination. These measurements are necessary to understand diode characteristic of p-n junction. Therefore, results of these measurement enabled us to decide about duration of samples in KOH solution.

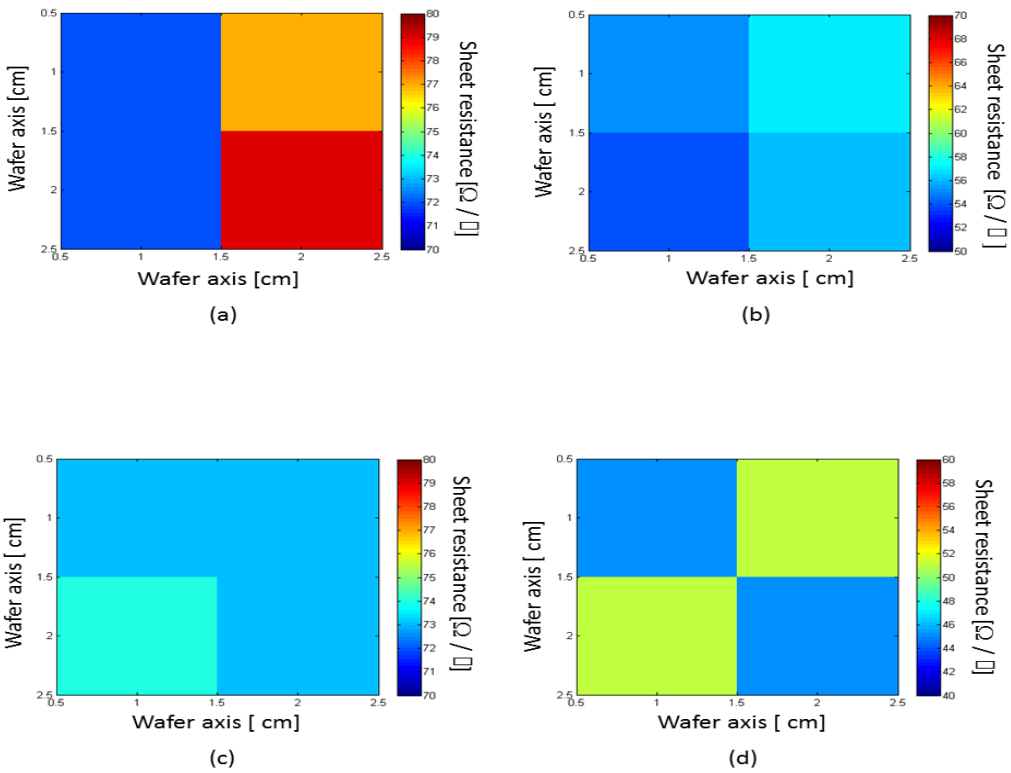


Figure 3. 26: Sheet resistance mapping of front side (a) and rear side (b) of sample for 30 seconds. Sheet resistance mapping of front side (a) and rear side (d) of sample for 60 seconds

Figure 3.28 (a) shows results of dark I-V measurement of samples before annealing. Figure 3.28 (b) shows resuts of dark I-V measurement of samples after annealing at 300°C. We see that all samples exhibit some rectification expected from a p-n junction diode. However, we also see that all samples show better rectificiations indicating better diode properties. After annealing, diode characteristics of junction started to be degraded. The reason for this can be the silver diffusion into the junction during the annealing. Silver has a high diffusivity in Si, that can easily reach the junction region and thus increase the leakage current.

Next, I-V measurement of samples performed under illumination. Table 3.2 shows the results of I-V measurement of under illumination before annealing. It is clearly shown that sample holding 120 sec. in solution have the best results. According to all of these results, the optimum duration in KOH solution of wafers has been determined nearly 120 seconds for 2nd approach.

I-V measurement of samples was done after the annealing at 300°, but there occurred a metallization problem that will be discussed in the metallization section.

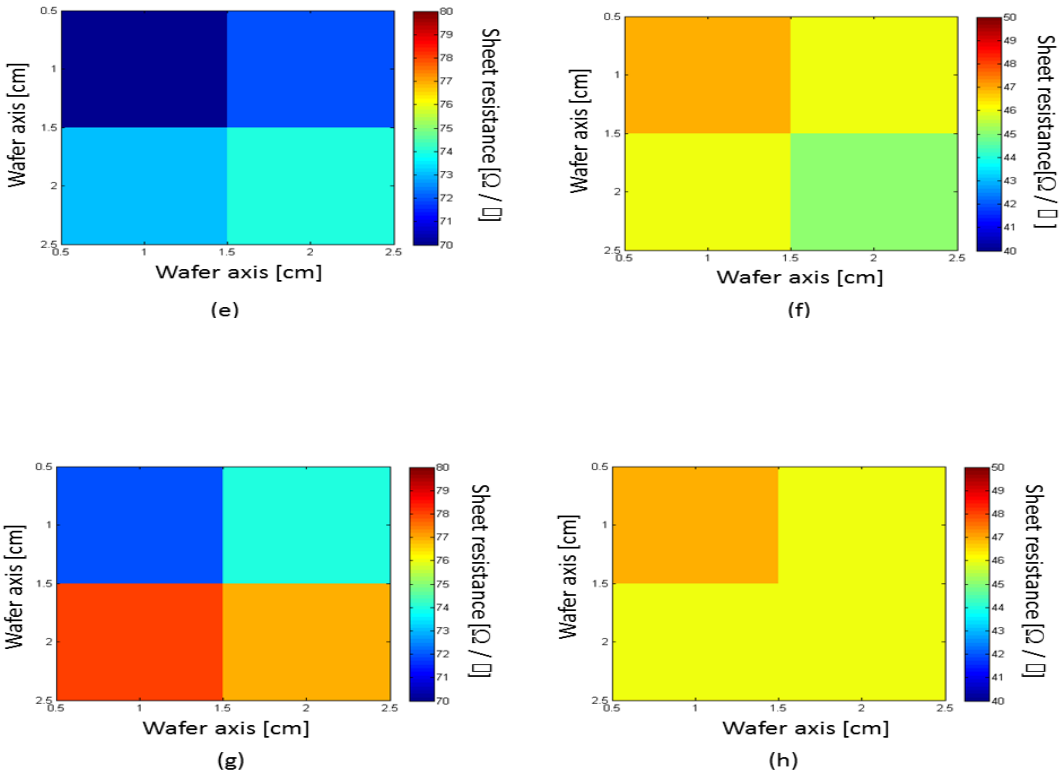
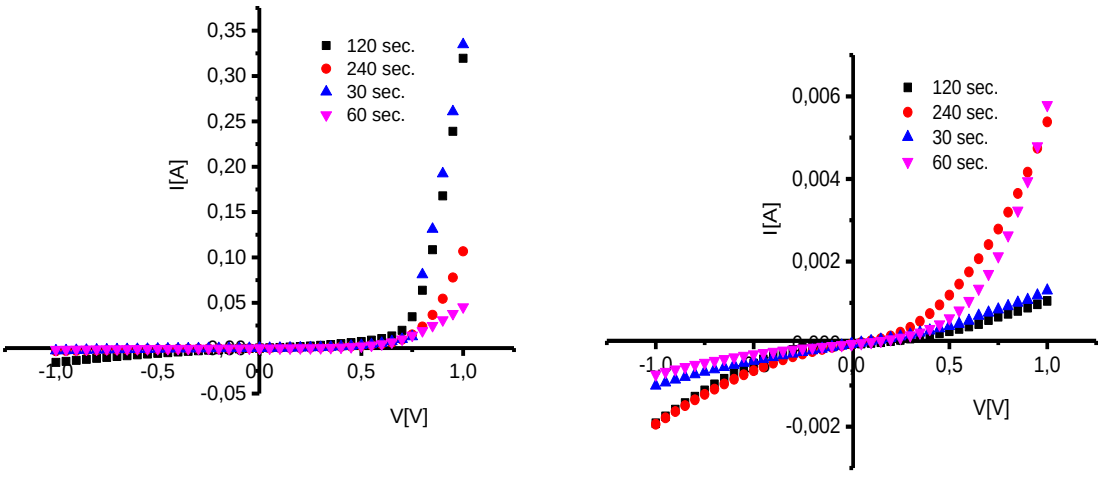


Figure 3. 157: Sheet resistance mapping of front side (e) and rear side (f) of sample for 120 seconds. Sheet resistance mapping of front side (g) and rear side (h) of sample for 240 seconds



. Figure 3. 28 : Results of dark I-V measurement (a) before and after annealing (b)

Table 3. 1: Results of I-V measurement under illumination of samples

Samples	Isc[A]	Voc[V]	Jsc [mA/cm^2]	Cell Eff.[%]	Fill Factor[%]	R at Voc	R at Isc	Cell area[cm^2]
30 sec.	**0.046**	**0.49**	**17.33**	**4.47**	**46.98**	**3.68**	**132.44**	**2.26**
60 sec.	**0.05**	**0.55**	**22.04**	**6.71**	**49.37**	**2.89**	**115.29**	**2.4**
120 sec.	**0.049**	**0.56**	**25.14**	**9.19**	**59.10**	**2.31**	**931.11**	**1.95**

The 3rd approach is shown Figure 3.29. Firstly, silicon nitride on the back side of the wafers was deposited by PECVD to prevent back side from boron doping. Then, front side of the wafers was doped with phosphorus. Next step was to remove the silicon nitride layer from the back side. A new silicon nitride layer was then deposited on the front side of wafers to protect front surface against phosphorus doping in the next step. Then, the back side of wafers was doped with phosphorus and then silicon nitride on the front surface was by a HF solution. By this way, p-n-n+ structure was obtained. The sheet resistance results of the structure were approximately same as the 2nd approach. Sheet resistance of the front and back side of the wafers was nearly 70 Ω/□ and 50 Ω/□, respectively.

The 4th approach is slightly different from 3rd. It is seen clearly when compared to Figure 3.29 and Figure 3.30. Front side of the wafers was protected by silicon nitride against phosphorus doping since back surface of wafers has been doped with phosphorus in this process.

As seen Figure 3.29, next steps are removing silicon nitride from front surface and deposition silicon nitride on the back surface of wafers before the boron doping. Then, boron doping was done and silicon nitride was removed from the back side of wafers. The structure of p-n-n+ has also been obtained by this way.

Although process flows of 3rd and 4th approaches seem similar, there is a small difference between doping sequences. In the 3rd approach Boron doping was carried out before the phosphorous diffusion, whereas phosphorous doping was carried out prior to Boron doping in the 4th approach. Since boron and phosphorous doping were carried out at ~1000°C and ~850°C respectively, comparison of these two approaches enabled us to see the effect of temperature on the junction depth.

As a final trial, we followed a 5th approach which is different from other approaches considerably. Figure 3.31 shows flow chart of this approach. Doping process is done differently in this approach. Wafers were doped with boron by putting them back-to-back. We expect that back-to-back configuration protects the both side of the wafers from doping. After the doping process, to create effect BSF on the back side, silicon nitride was deposited on to front side of wafers and then back side of wafers was doped with phosphorus. Next, silicon nitride was removed the front side of wafers. Thus, p-n-n+ was obtained as seen Figure 3.31. Sheet resistance of both sides of wafers showed nearly the same values.

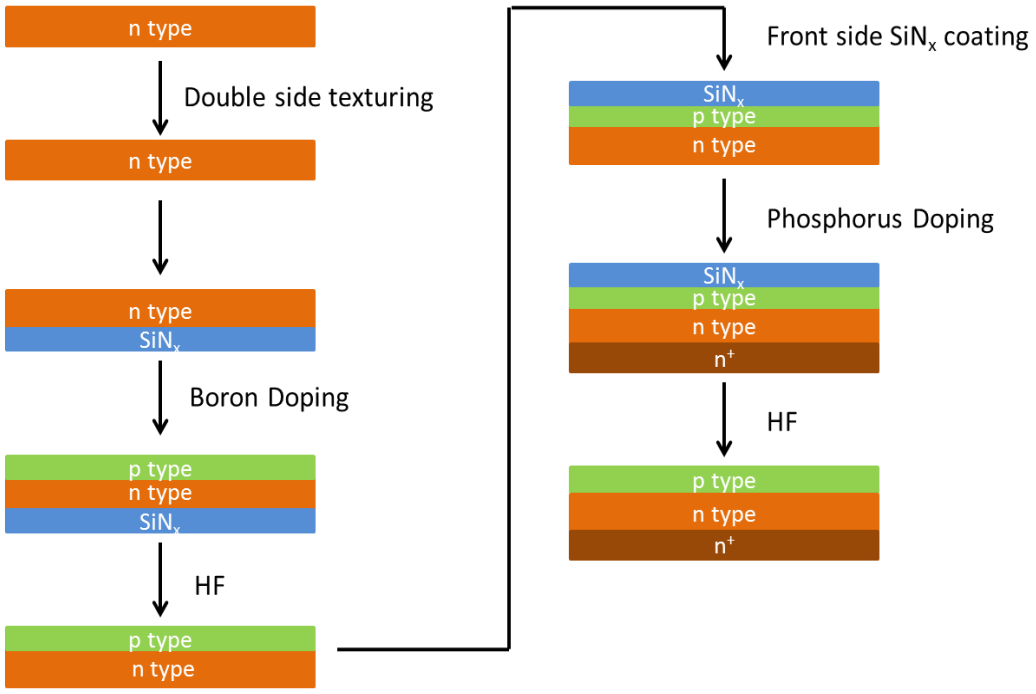


Figure 3. 29: Process Flow of 3rd Approach

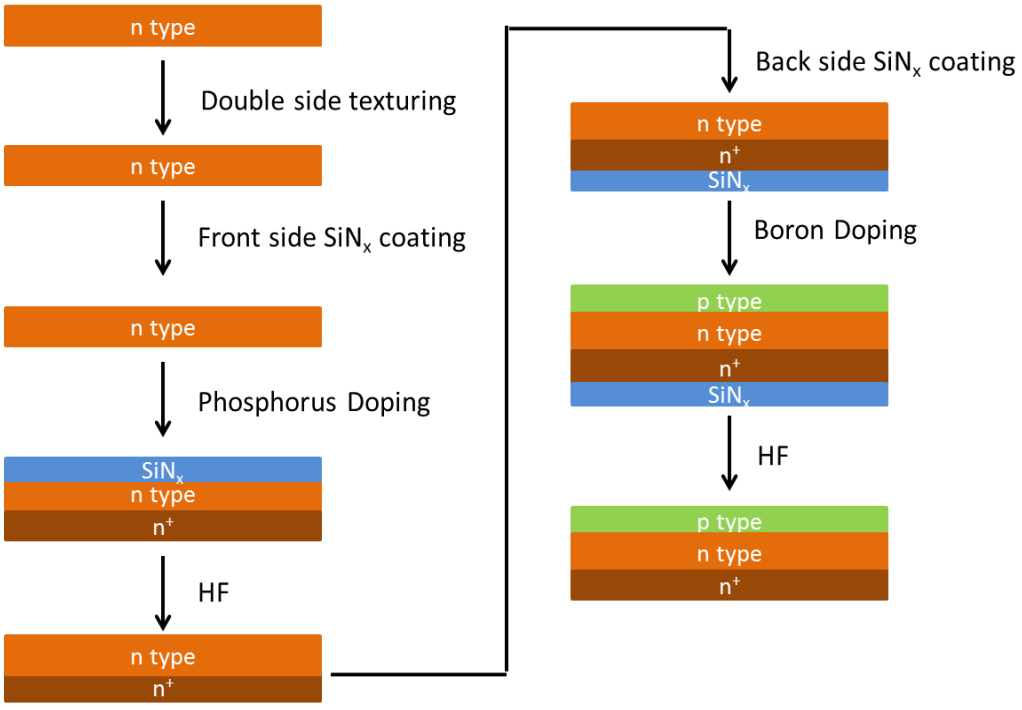


Figure 3. 30: Process Flow of 4th Approach

Considering all different approaches described above, we see that nearly same sheet resistance values were obtained for both front and back surface of the wafers except for the 1st approach.

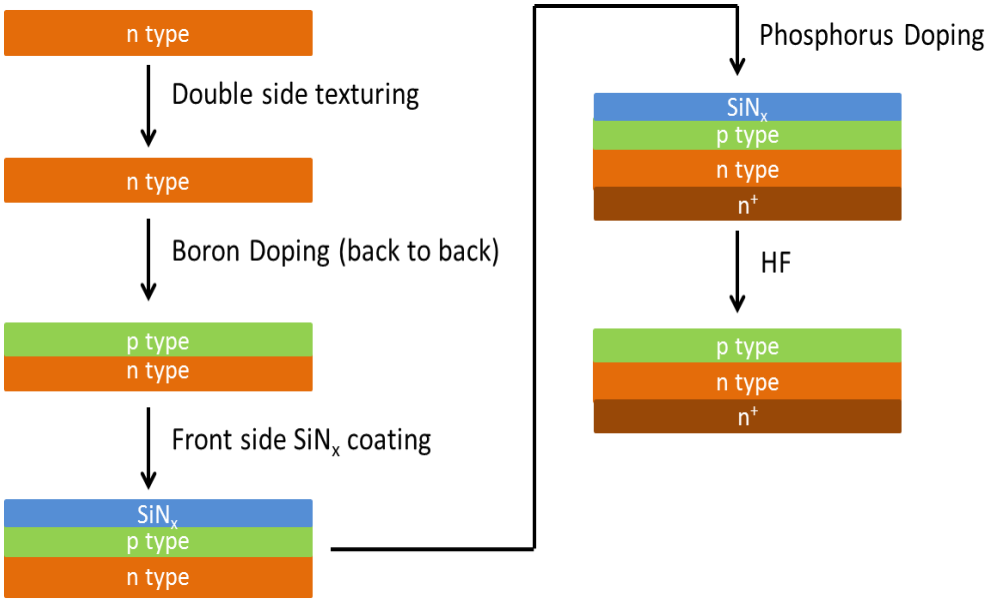


Figure 3. 31: Process Flow of 5th Approach

3.4. Antireflective Coating

3.4.1. Theory

It is a well-known fact that the efficiency of a solar cell depends strongly on the number of photons that absorbed by a cell. Therefore, the reduction of reflection on the front surface of the cell is crucial for en efficient energy conversion. Thanks to antireflective (AR) coatings available today, the reduction of the reflection is easily obtained in today's PV industry. In addition to the AR functionality, these thin films provide also electrical passivation on the surface by saturating the defect states on the surface.

Moreover, with the help of hydrogen present in the environment, coming from process gases SiH_4 and NH_3, bulk passivation of Si wafer is also enhanced. Finally, AR coatings also provide a protection from the environmental damages originated from dusts, moisture, etc.

When dealing with optical behavior of a surface we need to consider the dielectric constant of the material under consideration. It is well know that the reflection and absorption on a material surface is described using the dielectric constant which is given below,

$$\sqrt{\varepsilon_s} = n_s - ik_s \tag{3.15}$$

In (3.15), n_s is the refractive index, k_s is the absorption index and ε_s is the dielectric constant.

The reflectance is determined by the differences in refractive index between two materials as given in the equation below,

$$R = \left(\frac{n_0 - n_s}{n_0 + n_s}\right)^2 \tag{3.16}$$

When the material is coated with antireflective coating thin film which has refractive index n_1, (3.16) becomes [2],

$$R = \frac{(n_0 - n_s)^2 + \left(\frac{n_0 n_s}{n_1} - n_1\right)^2 \left(\tan\frac{2\pi n_1 d_1 \cos\theta_1}{\lambda}\right)^2}{(n_0 + n_s)^2 + \left(\frac{n_0 n_s}{n_1} + n_1\right)^2 \left(\tan\frac{2\pi n_1 d_1 \cos\theta_1}{\lambda}\right)^2} \tag{3.17}$$

Where $\theta_1$is the angle between the normal and the incident light, λ is the wavelength of the incident light, $d_1$is the thickness of the antireflective coating thin film. The minimum reflection of a normal incident ($\theta = 0$) is satisfied when the (3.17) is satisfied

$$n_1 = \sqrt{n_0 n_s} \tag{3.18}$$

that leads to the following relation between thickness and the wavelength;

$$d_1 = \frac{\lambda}{4n_1} \tag{3.19}$$

When this condition is satisfied we obtain the best condition to obtain a minimum reflection from the surface. So the thickness of the AR coating is easily found for a particular wavelength in the light spectrum. We see that the thickness and the refractive index of the coated film are important parameter in designing the best performing solar cells. With this simple consideration we can now calculate the desired thickness and refractive index of an antireflective coating film for silicon.

Refractive index of silicon n_s, is 3.44 and that of air, n_0, is 1 at 600 nm nearly. When the incident light comes, the refractive index of antireflective coating film for silicon can be obtained as

$$n_1 = \sqrt{3.44} = 1.85 \tag{3.20}$$

Since the solar spectrum converted by crystalline silicon solar cell has a peak 600 nm nearly as seen Figure 2.10, optimization is done with respect to that wavelength. For this reason, thickness of AR layer is calculated from the above expression, assuming wavelength of incident light is 600 nm. Then, thickness is found as,

$$d_1 = \frac{600}{4 \times 1.85} = 81 \text{ nm} \tag{3.21}$$

The reflectance of bare silicon on the front surface and silicon with antireflective coating film as a function of wavelength is shown in Figure 3.32.

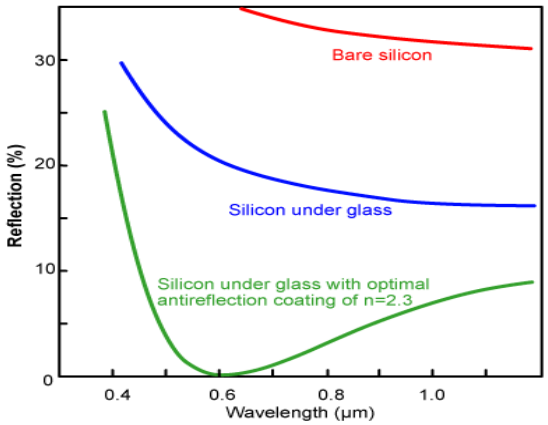


Figure 3. 32: The reflectance graphs of bare silicon and coated by anti-reflective thin film [24]

The reflectance of the silicon with an antireflective film is seen to have a minimum value at 600 nm. In today's PV industry, silicon nitride (Si_3N_4) is commonly used as an AR layer due to its superior optical and electrical properties. It is preferred because the refractive index of it is nearly 2.0. Moreover, refractive index of it can be varied by changing gas flow ratio.

3.4.2. Experiment

Silicon nitride is used as an antireflective coating layer on the front surface of the wafer in this part of the work since it provides good AR behavior and passivation of the surface.

To form a Si_3N_4 layer on Si surface, silane and ammonia are reacted chemically and this reaction leads to formation of silicon nitride through the following reaction as shown (3.22).

$$3SiH_4 + 4NH_3\ 4NSi_3N_4 + 12H_2 \quad (3.22)$$

Si_3N_4 is deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD) system in GÜNAM. The schematic diagram of the system is shown in Figure 3.33. Main process parameters are pressure, deposition temperature, and the total flow rate of the gases. In this work, these parameters are determined by process temperature: 380°C, pressure: 1000 mTorr and total gas flow: 1600 sscm (SiH_4:200/NH_3:1400).

In addition, the most important property of silicon nitride as a dielectric layer in PV technology is its refractive index that can be varied depending on the ratio of reactants. This gives us a chance of controlling the optical and electrical properties of the film easily. Figure 3.35 shows the dependence of refractive index on the gas flow ratios for a given wavelength.

We see that when the ratio of silicon increases, refractive index also increases. Therefore, silicon rich films give rise to higher refractive index. Optical and electrical properties of silicon nitride can then be controlled easily by means of changing the rate of the gas flow.

Thickness is also important parameter for dielectric layer, since it affects both optical and electrical properties. For solar cell application, refractive index of Si_3N_4 and thickness of that optimize nearly 2 and 80nm, respectively.

3.4.3. Experimental Results for Si_3N_4 Ar Coating

Silicon nitride has been mostly used as passivation layer and anti-reflective coating in PV industry [20, 26]. In recent years, silicon nitride and silicon dioxide stack layers have also been applied for n-type solar cells [27]. For this reason, in this study, silicon nitride has been used alone for p-type solar cell, but both silicon nitride and silicon nitride-silicon dioxide stack layer have been tried for passivation of the surface and for reduction of the reflection for n-type solar cell (Figure 3.36).

To produce n-type solar cell, front and back surface of some samples were only coated with silicon nitrate layer, whereas that of some samples were coated with silicon nitrate-silicon dioxide stack layers.

The reason why passivation layer covered on both sides of wafers is that both surfaces need passivation so that higher lifetime values could be reached.

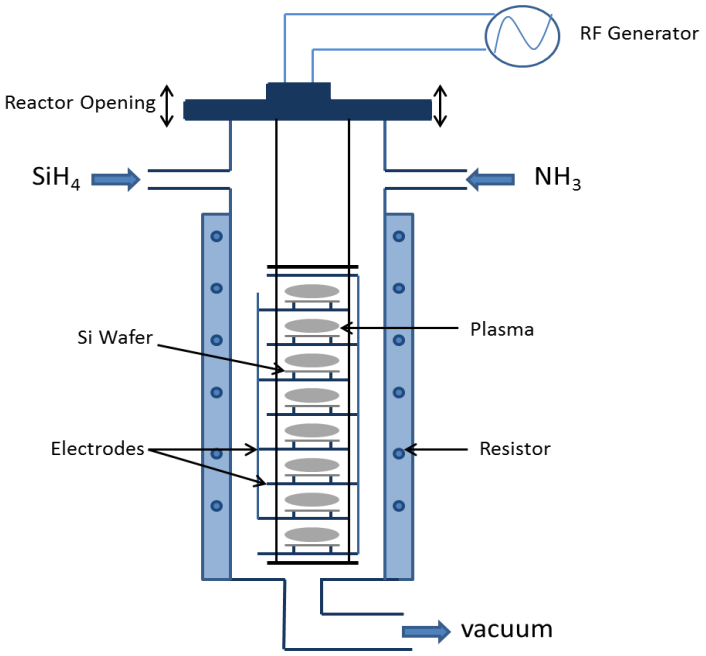


Figure 3. 33: Schematic diagram of PECVD system.

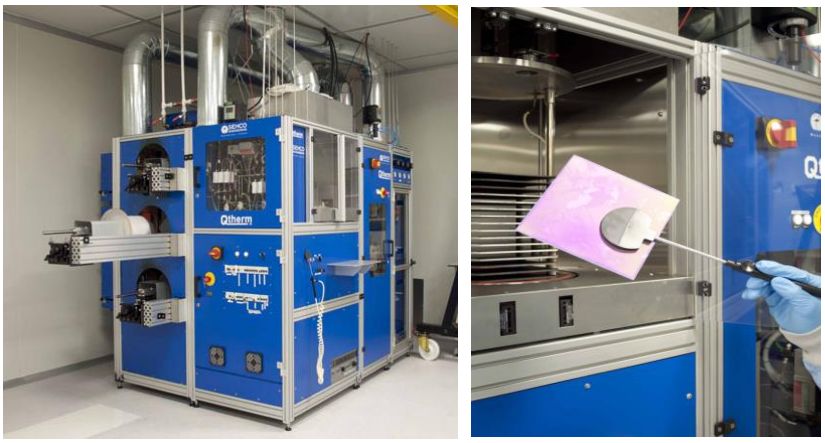


Figure 3. 34: Images of diffusion furnace and PECVD system used in GÜNAM

N-type solar cells, passivation of both sides are needed. However, for p-type solar cells, back surface is covered with Al which is used to create BSF. For this reason back surface passivation is not possible. However, in recent years, techniques fabricating back surface passivation have been developed. These techniques are outside of the scope of this study.

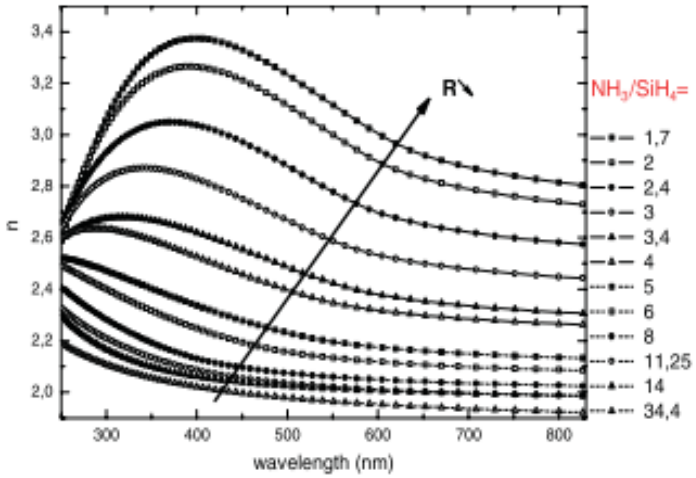


Figure 3. 35: Dependence of refractive index of SiN_x on the gas flow ratio for a given wavelength [25]

.

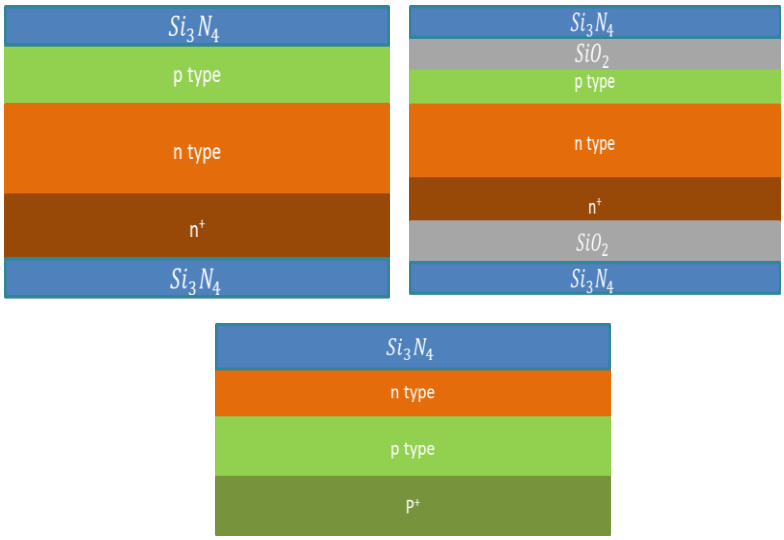


Figure 3. 36: Cross sectional view of both n-type and p-type wafers after the anti -reflective coating process

After the coating process, reflection measurements were done for p-type and n-type wafers to observe anti-reflective properties. The results of reflection measurement are shown in Figure 3.37, where we see that the reflection from the surface to very low values, which is desirable for the absorption enhancement.

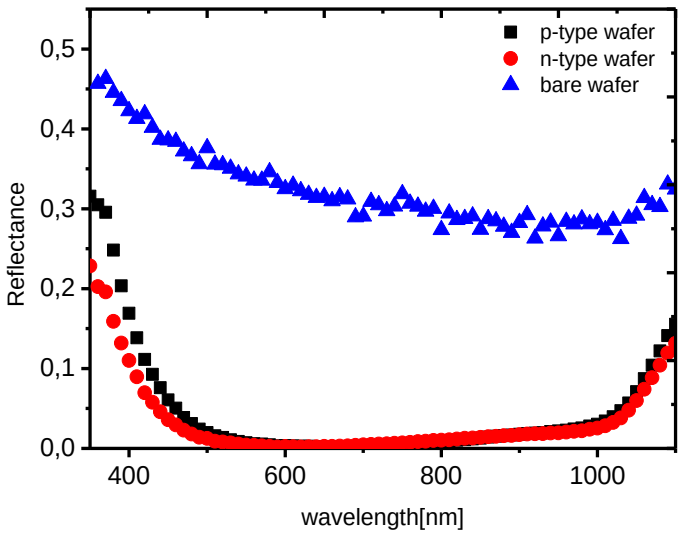


Figure 3. 37: Reflectance measurement results of p-type and n-type doped wafer

3.5. Metallization

3.5.1. Theory of Metal Semiconductor Contacts

In a solar cell, charges are separated in p-n junction by means of the electric field. Metallization is needed to collect the separated charges and pass them into the external load. Therefore, both surfaces of the semiconductor require metal contacts.

There are several ways to form metal films over the surface of the semiconductor such as thermal evaporation, screen printing etc. In solar cell industry, screen printing is generally preferred for its lower cost and suitability for mass production.

When a metal film is formed over the semiconductor, two types of contacts can be formed, namely, rectifying and non-rectifying contacts. The rectifying type junctions are called Schottky junction while the non-rectifying ones are called Ohmic contacts. This property is determined by the difference in the work functions of semiconductor and metal. The work function of a material is defined as the energy difference between the vacuum level and Fermi level.

When a metal and semiconductor junction forms, the Fermi level of them should be aligned at equilibrium in order to satisfy continuity equation. Assume that a semiconductor with a work function is $q\Phi_s$ is brought into a contact with the metal having the work function of $q\Phi_m$.

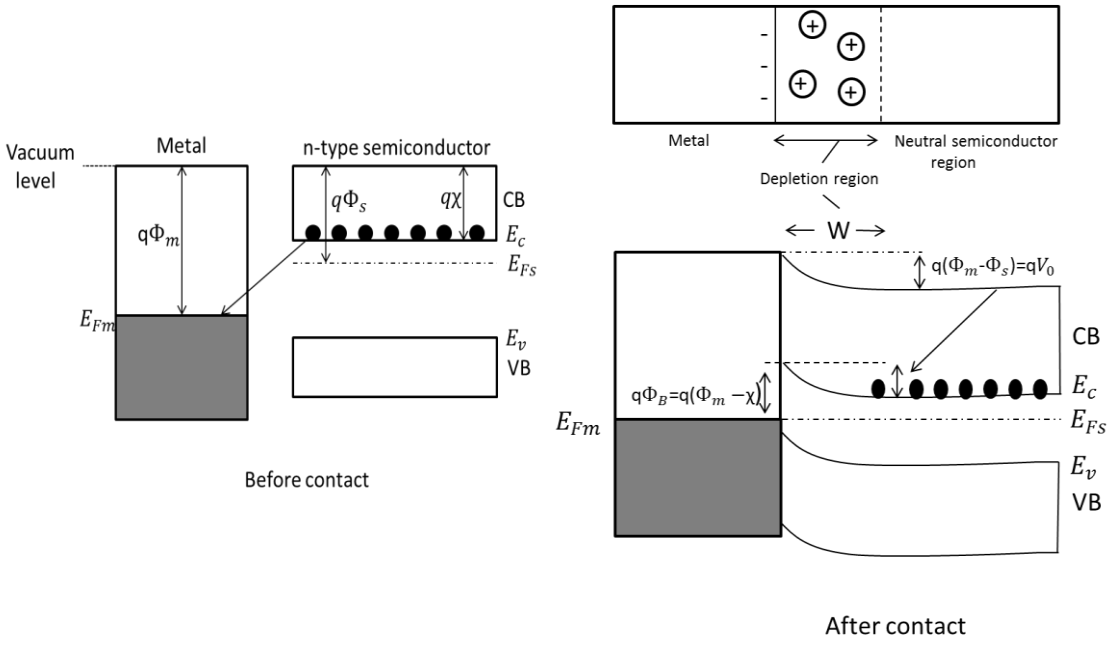


Figure 3. 38: Schottky junction formation

If work function of semiconductor is lower than that of metal, a potential barrier called as Schottky barrier is formed at the junction. This situation is illustrated in the Figure 3.38.

As shown in the figure, upon formation of metal semiconductor junction, difference in work functions leads to flow of charges, creating depletion region in the semiconductor side. This charge flow continues until Fermi levels of them are aligned at the same position. This leads to a charge transfer between two sides and formation of a dipole system. As a result, an electric field is developed which manifest itself as band bending in the conduction and valence bands of the semiconductor as shown in Figure 3.38.

The height of potential barrier is defined as $_{\mathrm{m}} - \chi$. Electron affinity ($\mathrm{q}\chi$) is defined as the energy from the bottom of the conduction band to the vacuum level. In addition, the contact potential at equilibrium is called as build-in potential, V_o.

When applied the forward bias, built-in potential is lowered and electrons from semiconductor move into the metal easily, since more electrons are present.

When a reverse bias is applied, built-in potential is higher than that under the zero bias. Electrons in the semiconductor do not move into the metal easily since there are few carriers when semiconductor is connected to positive terminal.

Therefore, very little current called as reverse saturation current is observed. The current flow is illustrated in Figure 3.39.

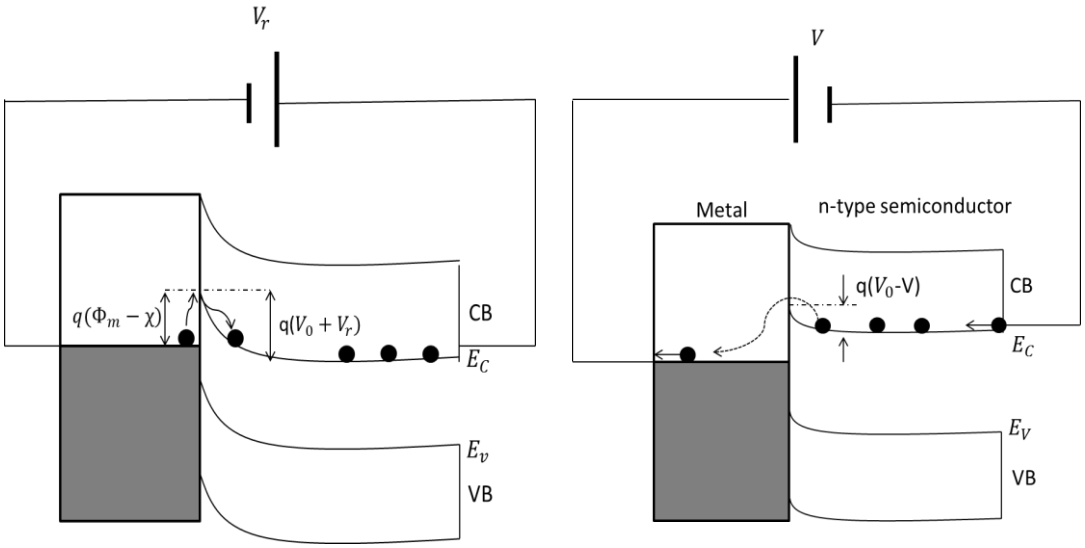


Figure 3. 39: Reverse and forward biased Schottky junction

The formation of Schottky junction is not preferable for photovoltaic devices. Ohmic contact is desirable since it has a negligible contact resistance.

An example for an Ohmic junction between n-type semiconductor and a metal is shown Figure 3.40. Note that, to satisfy this condition, the work function of metal should be lower than the work function of the semiconductor.

However, this condition is usually not obtained in a standard process needed for industrial applications. For this reason, a heavily doped region is formed to have an Ohmic contact.

Fortunately, the Schottky barrier can be overcome by increasing the doping concentration in the semiconductor, since higher doping concentration reduces the width of depletion region and leads to easy tunneling current.

A low contact resistance is then obtained even though a Schottky barrier still exists at the junction. In this type metal semiconductor contacts, no depletion region is formed when the Fermi levels of metal and semiconductor are aligned. However, heavy doping is not desirable because of high recombination rate that degrades the cell efficiency.

This problem is partly solved using new approaches like selective emitter technology. The determination of the contact resistance between semiconductor and metal layer is important to understand the junction and identify the quality of the metal junctions of the solar cell. For this purpose, Transmission Line Method (TLM) is commonly used.

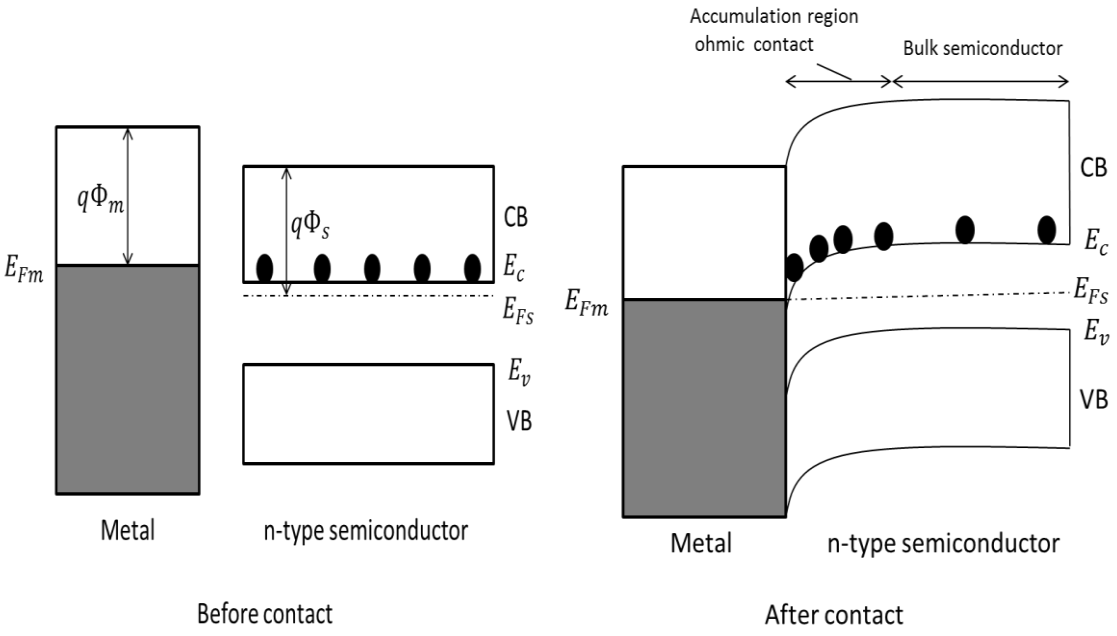


Figure 3. 40: Ohmic contact formation

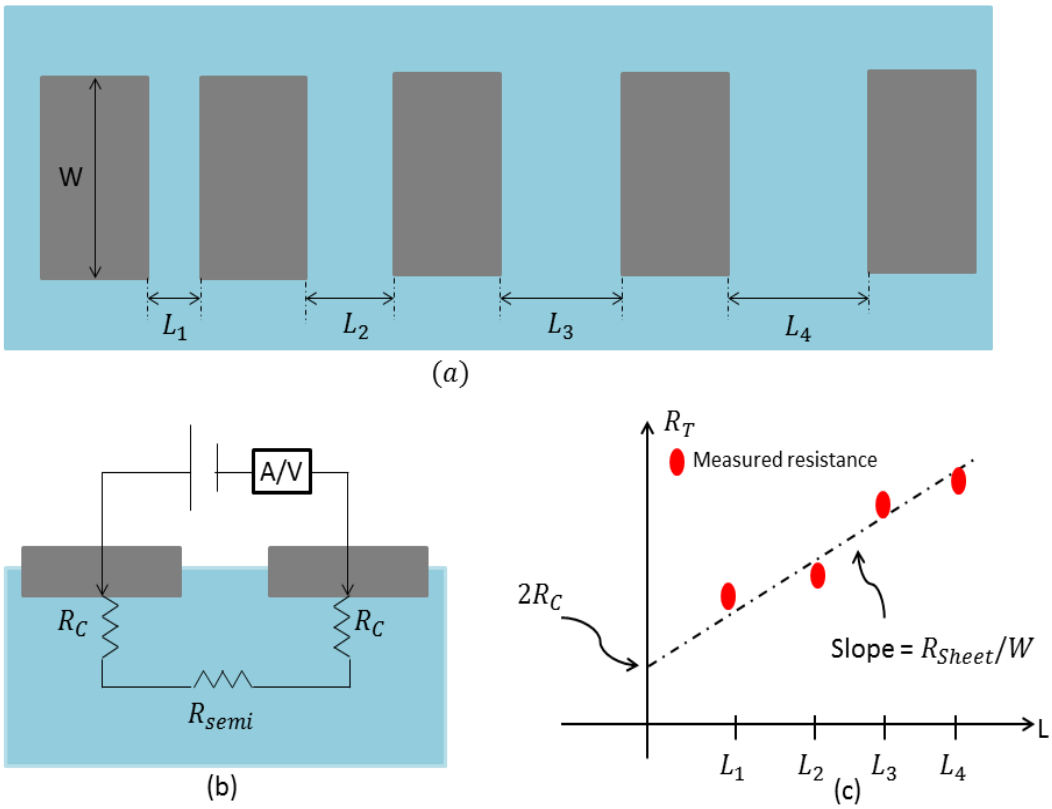


Figure 3. 41: top view of the TLM mask (a), cross section area of total resistance (b), curve of TLM (c)

3.5.1.1. Contact Resistance Measurement Using Transmission Line Method (TLM)

TLM is an effective way of determining the contact resistance of metal semiconductor junction. To use TLM method, firstly, the special pattern shown in Figure 3.41 (a) is printed on the wafer using a screen printer with a metal mask having the desired opening defining the desired geometry. The metal bars have varying gaps that facilitate formation of regions with different resistances. The contact resistance is determined as follows, first, I-V curves are measured between the adjacent metal contacts. Then, total resistances are found from the I-V curves [28]. The measured total resistance for any interval is defined as,

$$R_T = R_{semi} + 2R_C \tag{3.23}$$

In (3.23), R_{semi} corresponds to the resistance of semiconductor between two metal contacts and R_C is the contact resistance which results from the formation metal and semiconductor. The semiconductor resistance can be written as,

$$R_{semi} = R_s \frac{L}{W} \tag{3.24}$$

In (3.24), R_s is the sheet resistance of semiconductor, L is the distance between adjacent metal contacts and W is the length of the metal bar. When (3.24) is inserted into the (3.23), (3.23) becomes,

$$R_T = R_s \frac{L}{W} + 2R_C \tag{3.25}$$

When L goes on zero, (3.25) becomes,

$$R_T = 2R_C \tag{3.26}$$

When the graph of R_T of each adjacent contact versus L is plotted and the data are fitted the

linear curve, contact resistance can be found at the intersection point of the fitted line with the y-axis as shown in the Figure 3.41.

3.5.2. Screen Printing as a Method of Metallization

Screen printing is a commonly used for metallization in PV technology. It is far preferable way since it allows low cost and mass production. For p type solar cell, aluminum (Al) is used in order to coat the rear side of the cell since Al converts n type layer formed after the doping into the p type layer again. Moreover, it is convenient in order to create back surface field (BSF), which reduces recombination at the rear side of the solar cell. Therefore, back side of the wafer is fully coated by a paste with Al. For front side of the p type solar cell, silver (Ag) is used rather than aluminum, since n type layer formed by P requires not to be contacted with Al with a low contact resistance.

Moreover, the design of the front metal contact is different from back side, such that it should allow solar cell to absorb the maximum light because light enters into the cell from front side. With the busbars and fingers, H-bar patterns is prevalent generally as shown in figure 3.42.

On the other hand, h-bar pattern mask and Ag paste are used both rear and front side of the wafer for n-type wafer. The reason is that if the rear side of the wafer covers with Al, p-n-n+ structure loses the property of BSF. For this reason, the rear side is coated with Ag instead of Al.

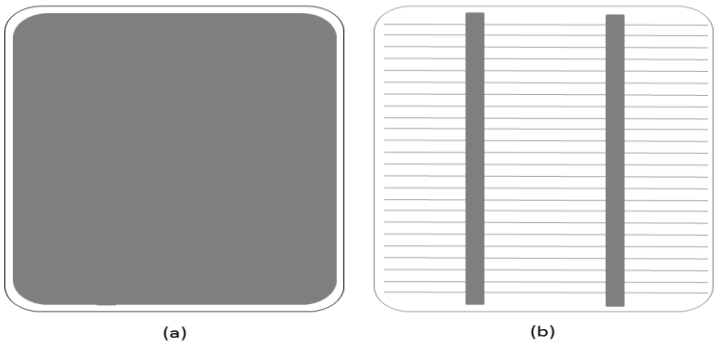


Figure 3. 42: Aluminum mask for back side of wafer (a), silver mask for both sides of the wafer (b)

As mentioned above, the resistance of the metal and its contact resistance are important for an efficient cell operation. These parameters strongly depend on the geometry of the printed fingers and busbars. Fingers and busbars should be designed to obtain lowest resistance. At the same time, the total area of the printed metal should be small to have lowest shadowing effect.

For this reason, the ratio between the width and height of the finger, called aspect ratio should be optimized to minimize the resistivity and to reduce shadow effect. As seen in the figure 3.43, the width of the finger should be small for less shadowing effect. However, the cross sectional area of finger should be large to obtain the maximum conductivity. Therefore, the height of the finger should be high. When these conditions are taken into the consideration, aspect ratio should be as high as possible with smallest width. When these conditions take into consideration, the optimum ratio, aspect ratio, is determined and it is defined as (3.27).

Aspect ratio can vary nearly from 0.30 to 0.20 in screen printing method [29]. To increase the aspect ratio even further, double printer is also considered.

$$\text{Aspect ratio} = \frac{\text{height}}{\text{width}} \tag{3.27}$$

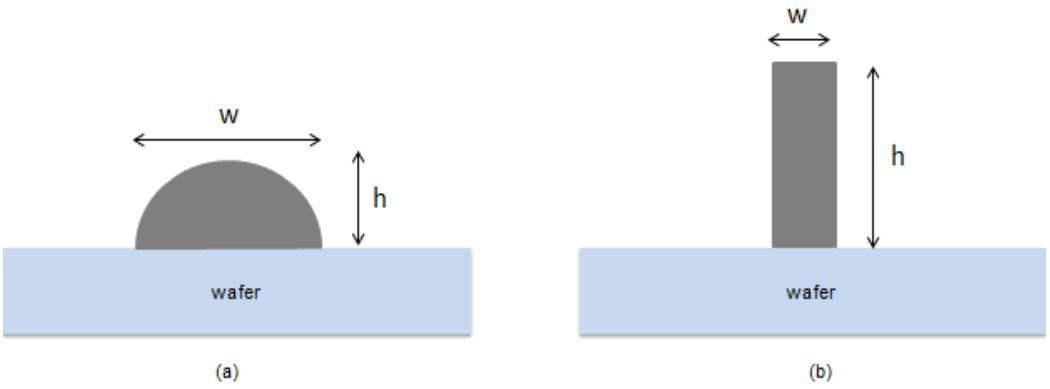


Figure 3. 43: Cross section area of screen printed line in real case (a), in ideal case (b)

In this work, ASYS X1 SL model screen printer, shown in Figure 3.44 has been used as a printer in GUNAM laboratory.

Then, solar cells are exposed to firing process through belt furnace at high temperature to diffuse metal into the silicon wafer on both side of the cell.

Belt furnace used in this study consists of seven heating zones. However, it is found that three zones are enough to obtain sufficiently good results. The belt speed is adjustable for optimization [29]. In this work, three zones have been used.

The temperature of zone 2 has been set to 850°C while temperature of zone 1 has been set to 700°C-750°C. Contrary to zone 1 and 2, zone 3 was adjusted to a lower temperature. Different metallization pastes have different properties and for this reason, temperature profile of them can vary slightly. Firing furnace that was used in this work is shown in the Figure 3.44.

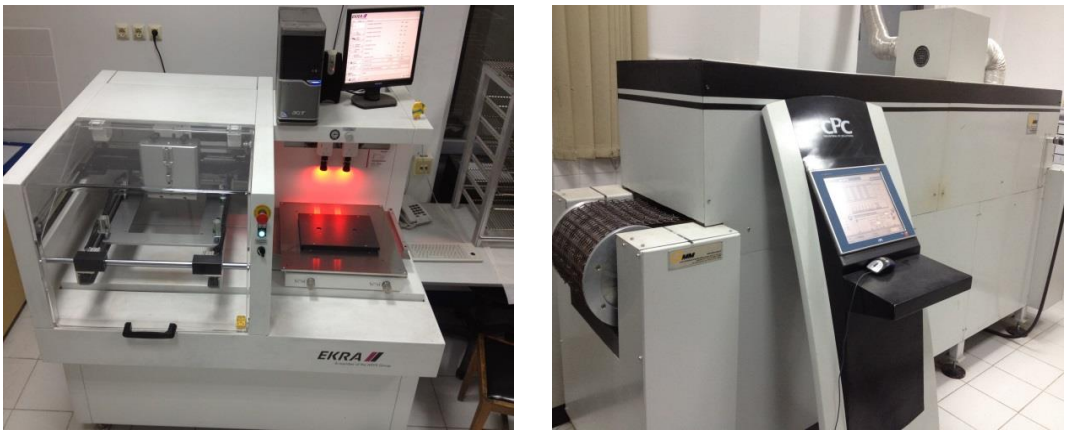


Figure 3. 44: Images of screen printer and firing furnace

3.5.3. Edge Isolation

When the textured wafers are doped in diffusion process, both the front surface of wafers and back surface of the wafers are doped with dopant atoms, as well as edges of the wafers. For p-type solar cells, although Al converts n-type region into p^+ region on the back surface of the doped wafer by means of firing process after the metallization, it cannot prevent the current at the edge of the wafers. Similarly, although using silicon nitrate enables us to protect the surface of the wafers in diffusion process for n-type solar cells, it cannot prevent the edges from doping. Therefore, electron hole pairs separated from p-n junction can flow the edges and recombine without achieving metal contacts, which causes shunt currents that is detrimental for performance of the cell. To prevent shunt currents, edge isolation is performed by several methods such as laser scribing, chemical edge isolation or plasma edge isolation.

In our laboratory, laser scribing has been used. Laser scribing creates a deep groove of 20-30 μ m along the periphery of the cell that provides the isolation of the front side from the back side [30]. This technique is routinely used in the production line today as it is suitable for the mass production.

3.5.4. Metallization Results

After the formation of p-n junction for n-type wafer, we found that silver affects diode characteristic of the junction negatively after the annealing. This results from silver diffusion through the junction. To test the quality of Ag contact we performed TLM analysis, from which we calculated the value of contact resistances as described in section 3.5.1.1.

Some samples were only coated with silicon nitrate layer whereas some samples were coated with silicon nitrate-silicon dioxide stack layers. Then, TLM patterns were formed on those

two types of samples. In addition, bare wafers were also patterned with the same TLM masks to be used as reference group. Cross sectional views are shown in Figure 3.45.

A 75 nm thick Silicon nitrate was deposited by PECVD, when needed 10-15 nm thick silicon dioxide layers were grown by dry oxidation nearly at 950°C.

These samples were fired for different transition velocities changing from 90mm/s to 70mm/s while zone temperatures were kept constant. Temperature of zone 1 and zone 3 is at 750°C and that of zone 2 is at 830°C.

The results of contact resistance are given in Table3.3. According to Table 3.3, for type 1 samples, 80mm/s transition velocity gave the lowest contact resistance value among other transition velocities. For type 2 samples, 90mm/s transition velocity gave the lowest contact resistance value among others. Lower contact resistance results in better metallization quality. For this reason, 80 mm/s could be accepted as optimum transition velocity for type1 samples whereas 90mm/s could be accepted for type 2 samples.

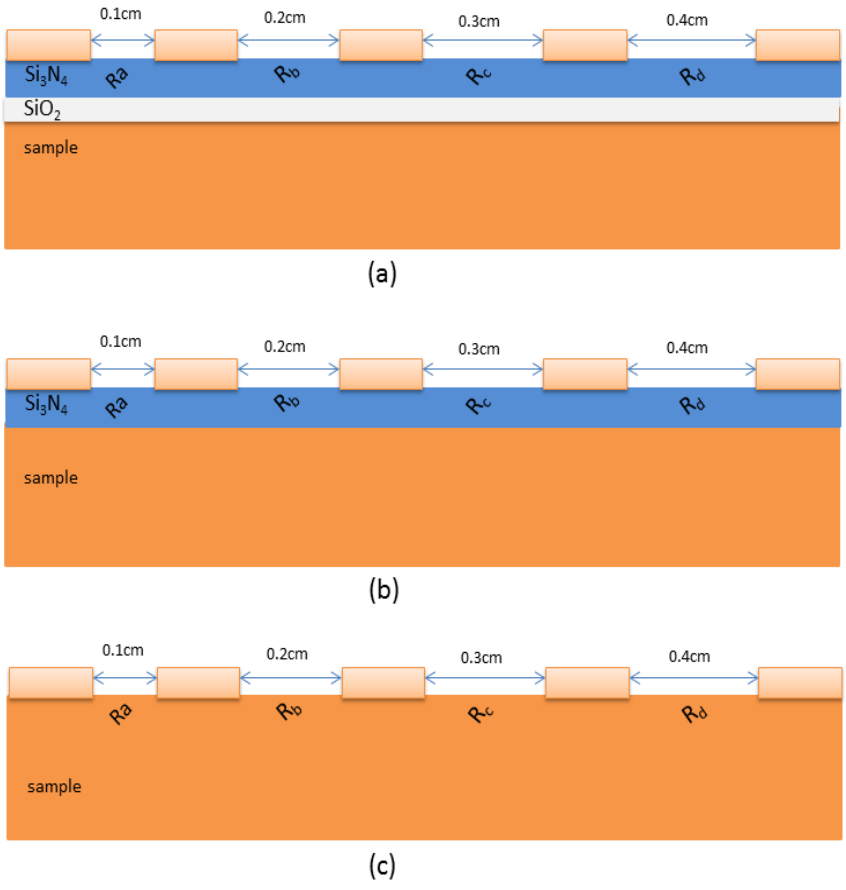


Figure 3. 45: Design of samples for TLM measurement type 1 (a), type 2 (b), type 3 (c)

Table 3. 2 : Results of contact resistance at different transition velocity.

Velocity(mm/s)	R_{C1} (Ω)	R_{C2} (Ω)	R_{C3} (Ω)	R_{C4} (Ω)	R_{C5} (Ω)	$R_{C\ AV}$(Ω)
90(type1)	3.9	2.5	1.84	2	2.18	2.48
90(type2)	1.76	1.4	1.5	1.54	1.65	1.57
90(type3)	1.65	1.57	1.5	1.45	1.48	1.53
80(type1)	2.2	1.57	1.62	1.78	1.7	1.77
80(type2)	3	2.3	1.88	1.71	1.7	2.11
80(type3)	1.5	1.39	1.44	1.29	1.35	1.39
70(type1)	3.03	1.95	1.59	1.93	2.1	2.12
70(type2)	4.2	1.39	1.39	1.43	1.61	2.0
70(type3)	1.4	1.40	1.42	2.83	1.85	1.78

Metallization of samples was done by taking into consideration these results. Images of sample after metallization and edge isolation are given below in Figure 3.46.

To observe the effect of edge isolation on solar cell, solar cell was analyzed by thermal camera which shows the hot points resulting from the excessive shunt current. A DC bias is applied to observe this effect. The thermal images of samples can be seen in Figure 3.49.

As seen Figure 3.47 (a), high temperature of edges of the solar cell indicated the leakage current before the edge isolation. After edge isolation, Figure 3.47 (b), high temperature at the edges was no longer observable. Hot spot shown as HS1 in Figure 3.47 (b) was resulted from rupture at some point along a finger. The relatively lower temperature after edge isolation deduced that edge isolation could be successfully carried out.

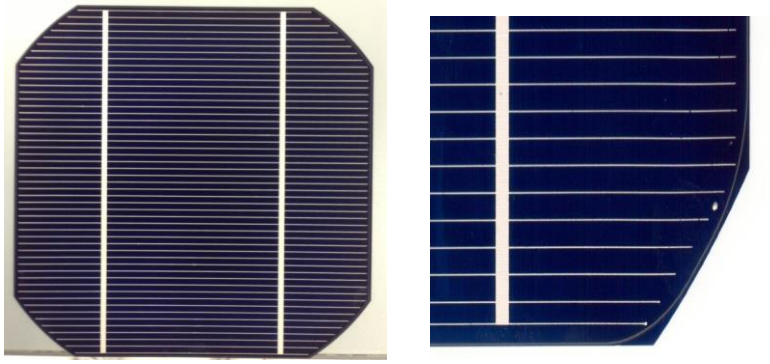


Figure 3. 46: Images of sample after metallization (a), and edge isolation (b)

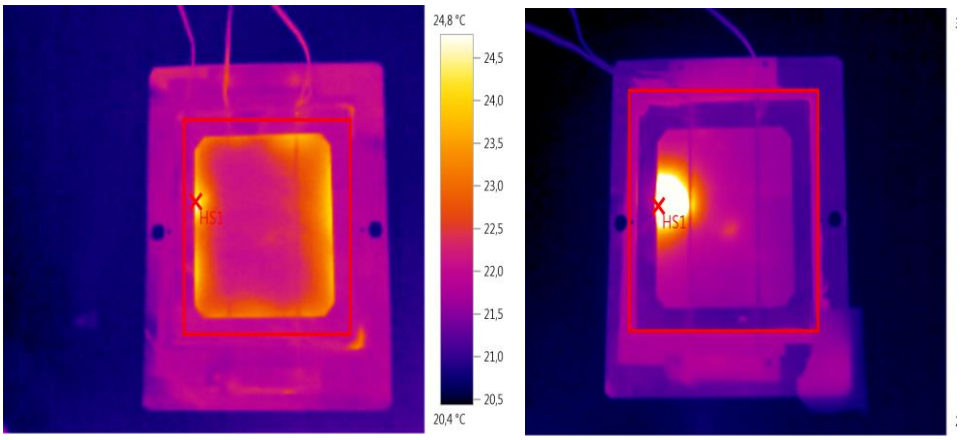


Figure 3. 47: Thermal camera images of sample before edge isolation (a), after edge isolation (b)

CHAPTER 4

PERFORMANCE OF N-TYPE SOLAR CELLS PRODUCED WITH DIFFERENT APPROACHES

4.1. I-V Characteristics of Solar Cells

4.1.1. Experimental Setup

Electrical characteristics of solar cells were determined by I-V measurement under illumination and dark. Dark I-V measurement was done by Keithley Sourcemeter connected to the PC. The connection of sample and sourcemeter is provided by two probes, one of which is connected to the front fingers of solar cells. The other one is connected to the copper plate which is in touch with the back side of samples. The I-V measurement under illumination was performed with a Solar Simulator manufactured by Quick Sun. Solar Simulator includes a flash lamb adjusted to the AM1.5G. Experimental setup is given below Figure 4.1.

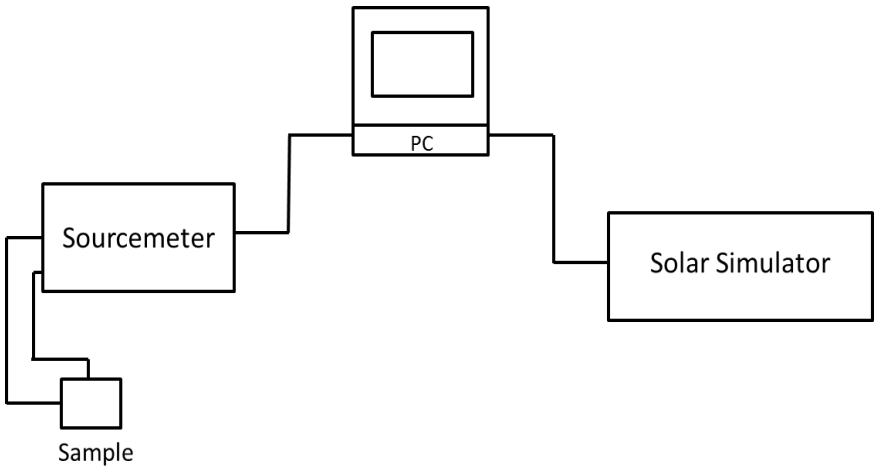


Figure 4. 1: Schematic of I-V characterization setup

In addition to I-V curves, solar simulator gives the values of efficiency, fill factor, open circuit voltage, short circuit current, current density etc. of solar cell by means of snapshot of the software of solar simulator.

4.1.2. Experimental Results

In this study, p-type solar cells and n-type solar cells including five different approaches were produced. Next, for n-type solar cells, two different combinations of passivation layers were used to obtain better performance. Then, metallization was done by using screen printer to all types of wafers and all wafers were exposed to the firing process and edge isolation process as well.

After all these steps, electrical characterizations and performances of all solar cells produced different way were studied by measuring I-V curve under illumination and dark.

Dark I-V measurement was performed using Keithley Source meter to understand diode characteristics of samples. Results of dark I-V measurement of samples with Si_3N_4 are given below Figure 4.2.

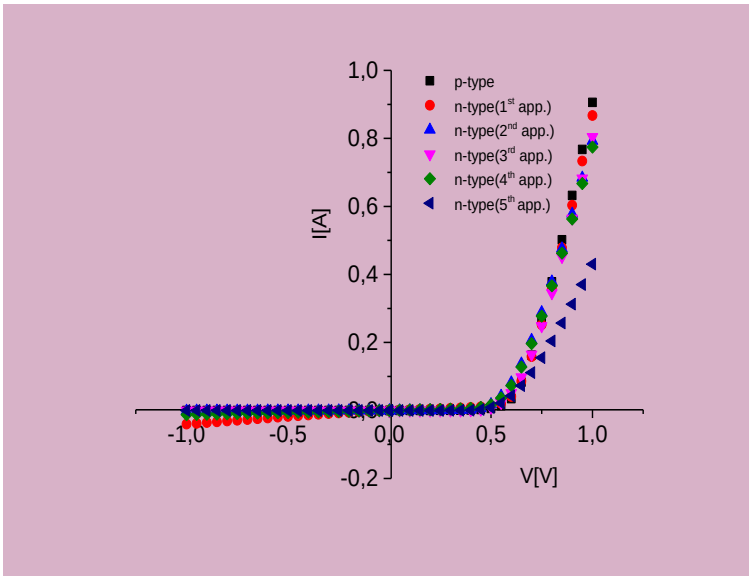


Figure 4. 2: Results of dark I-V measurement of samples passivated with only Si_3N_4

According to Figure 4.2, all samples with Si_3N_4 display typical diode behavior. It means that processes of formation of p-n junction were done successfully. This is a promising result for solar cell applications.

Results of dark I-V measurement for the samples with Si_3N_4-SiO_2 stack layer are given in Figure 4.3. As seen from this figure, we have also obtained diode characteristics in this case.

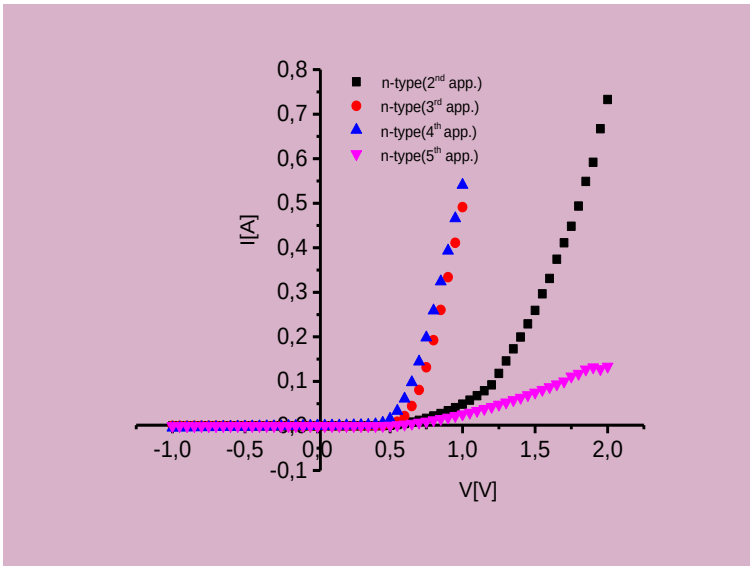


Figure 4. 3: Results of dark I-V measurement of samples double sides passivated with stack layer

Under the illumination, these results of solar cells used as passivation layer only Si_3N_4 are given by Figure 4.2.

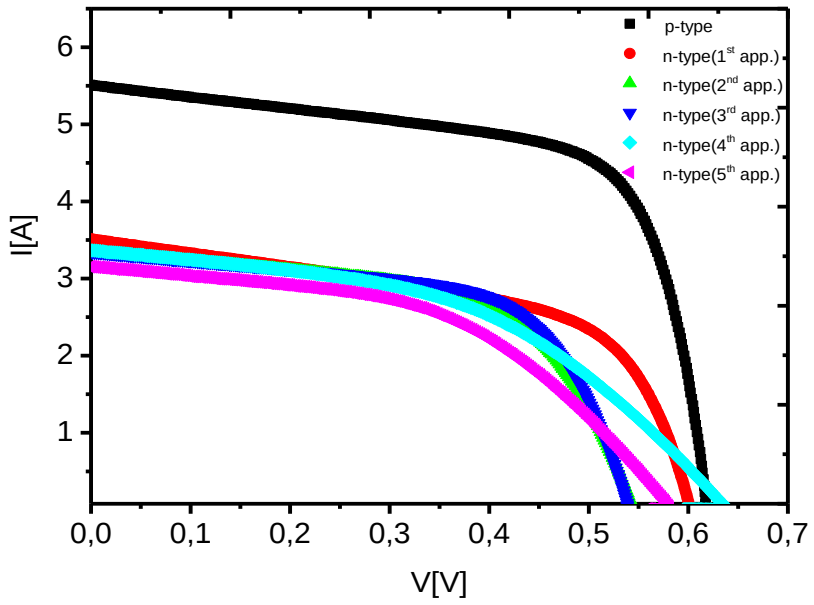


Figure 4. 4: Results of I-V measurement of samples passivated with Si_3N_4

From Figure 4.4, we see that p-type solar cell has a better performance when compared to n-type solar cells of I-V curves. The values of open circuit voltage and short circuit current are better results for p-type solar cell with respect to n-type solar cells. N-type solar cells have relatively lower open circuit voltages and short circuit current values. This is somewhat expected because the technology based on p-type wafer is well established and controlled. N-type Si needs to be studied and optimized to reach the level that p-type technology has reached.

I-V measurement of solar cells with $SiO_2 - Si_3N_4$ passivation stack layer was done under illumination. The results of this measurement are given in Figure 4.5.

It is clear that I-V curves of all samples and the values of open circuit voltage and short circuit current of each samples seem to be same nearly, except one sample produced by 5th approach.

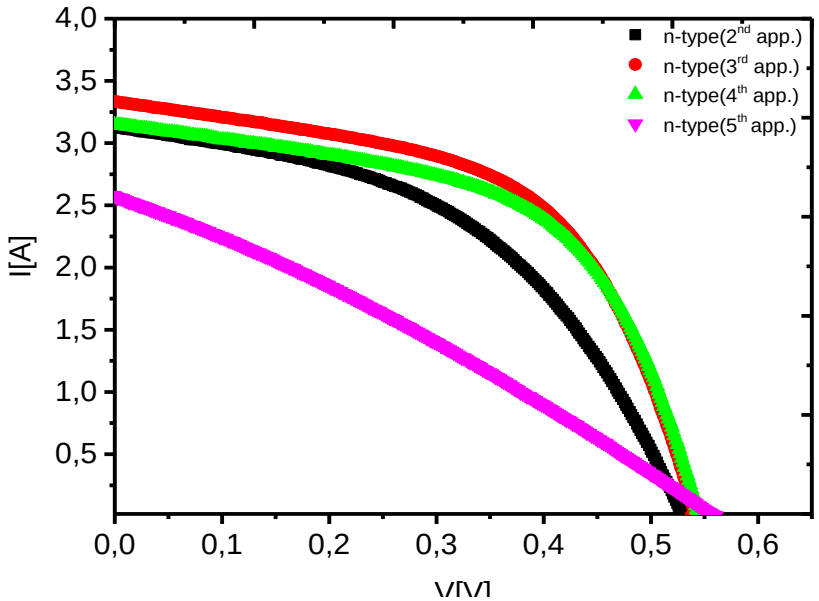


Figure 4. 5: Results of I-V measurement of samples double sides passivated with SiO_2- Si_3N_4

Other parameters obtained from solar simulator are given Table 4.1. From Figure 4.4, Figure 4.5 and Table 4.1, it can be deduced that better performance both p-type and n-type solar has been obtained when only silicon nitride is used as passivation layer.

It is clearly seen that p-type sample has good performance and the value of open circuit voltage and current density are compatible with today's solar cell industry. Fill factor of p-type solar cell is almost comparable with the solar cell produced by industry. Shunt resistance value seems to be negative, which results from properties of solar simulator. Solar simulator can give negative results for shunt resistance value when the shunt resistance value is high enough. Therefore, it can be said that shunt resistance of p-type sample is almost ideal.

As for series resistance value of p-type sample, it is close to zero. The lower series resistance results in higher performance of solar cell and so the value of p-type sample is promising to obtain better performance for solar cell efficiency. However, it could be reduced even more when metallization is enhanced.

Table 4. 1: Result of I-V measurement by solar simulator

Sample	Isc[A]	Voc[V]	Jsc [mA/ cm^2]	Cell Eff.[%]	Fill Factor[%]	R_{sh}	R_S	Cell area[m^2]
p-type	4.98	0.62	33,2	15.83	77.06	30.48	0.009	0.015
n-type (1stapp.)	3.26	0.57	31,65	12.21	67.2	1.47	0.017	0.0103
n-type (2nd app.) with Si_3N_4	3.27	0.51	31,74	10.9	66	6.72	0.023	0.0103
n-type (2nd app.) with Si_3N_4+SiO_2	3.04	0.51	29.51	8.0	52	2.26	0.046	0.0103
n-type (3rdapp.) with Si_3N_4	3.21	0.51	31.16	11.3	70.7	11.37	0.019	0.0103
n-type (3rd app.) with Si_3N_4+SiO_2	3.05	0.52	29.61	9.9	63	18.18	0.029	0.0103
n-type (4thapp.) with Si_3N_4	3.13	0.62	30.38	10.2	52	7.83	0.073	0.0103
n-type (4thapp.) with Si_3N_4+SiO_2	3.22	0.51	31.26	9.5	58	3.06	0.031	0.0103
n-type (5thapp.) with Si_3N_4	3.05	0.57	29.61	9.18	53	3.84	0.067	0.0103
n-type (5thapp.) with Si_3N_4+SiO_2	2.53	0.61	24.56	4.5	30	0.32	0.196	0.0103

For n-type samples, as shown Table 4.1, it is seen obviously that performance of them is relatively lower than that of p-type solar cell. When looked at the open circuit values of n-type solar cells, the values are far away from the desirable value since open circuit value varies from 0.62 to 0.65 in high efficiency solar cells. Shunt resistance values of n-type wafers are also not high enough to prevent the leakage current. Lower shunt resistance values may have resulted from the leakage through the junction and lower quality of edge isolation.

From the results displayed in Table 4.1, series resistance values of n-type solar cells are also higher that of p-type solar cell. In order to analyze the effect of series resistance on solar cell performance, solar cells were divided into smaller pieces and I-V measurement was done again for each pieces. This is because effect series resistance decreases with decreasing area, due to the lower amount of current that flows to the contacts.

This process was applied to all samples and some remarkable results of them are found as shown in Figure 4.6. It is observed that n-type samples with SiO_2-Si_3N_4 stack layer show a positive response to decreasing area of the cell.

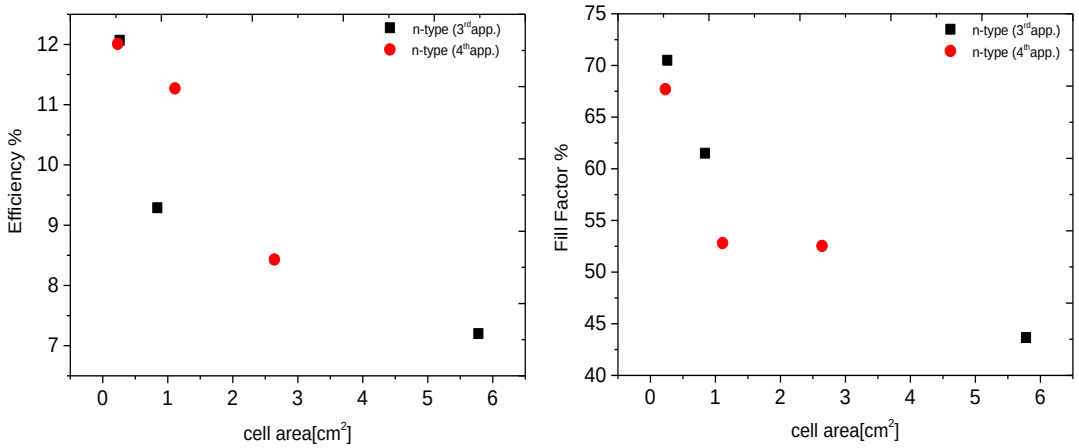


Figure 4. 6: Effect of cell area on efficiency and fill factor

Table 4. 2: Results of SunsVoc Measurement

samples	Jsc	Voc	Pseudo Cell Efficiency	Fill Factor
p-type	0.035	0.618	17.79	0.822
n-type (1st app.)	0.032	0.613	14.11	0.708
n-type (2nd app.) with Si_3N_4	0.032	0.554	13.63	0.756
n-type (2nd app.) with Si_3N_4 -SiO_2	0.032	0.539	13.33	0.761
n-type (3rd app.) with Si_3N_4	0.032	0.553	13.56	0.754
n-type (3rd app.) with Si_3N_4 -SiO_2	0.032	0.539	13.64	0.779
n-type (4th app.) with Si_3N_4	0.032	0.559	13.91	0.765
n-type (4th app.) with Si_3N_4 -SiO_2	0.032	0.549	13.75	0.770
n-type (5th app.) with Si_3N_4	0.032	0.545	13.59	0.767
n-type (5th app.) with Si_3N_4 -SiO_2	0.032	0.566	14.71	0.799

Figure 4.6 shows that reduction of the series resistance increases performance of the solar cells. Since it is directly related to quality of metallization, SunsVoc measurement was performed to the all samples to obtain pseudo cell efficiency. Cell efficiency could be calculated by eliminating series resistance of metal via SunsVoc measurement. Results of SunsVoc measurement are given Table 4. 2.

As can be seen in the Table 4.2, results of all I-V measurement exhibits clearly that metallization plays an important role in improvement of solar cell performance. It can be said that better results can be obtained by improving metallization for all samples. As given Figure 3.49 in section 3.5.4, the rupture of metal fingers is observed by image of thermal camera after the edge isolation. Consequently, to improve the performance of both type solar cells, it required to optimize the metallization process such as firing temperature, and laser parameter in edge isolation process.

4.2. Quantum Efficiency Measurement

Quantum efficiency is a quantity showing the performance of a cell as a function of the wavelength and it is defined as the ratio of the number of charge carriers which are collected by solar cell to the number of incident photons. Quantum efficiency (QE) is directly related to absorption of material and performance of charge collection of solar cell. Ideal shape of quantum efficiency is a rectangle with %100 efficiency, but the shape of quantum efficiency of solar cell is far away from the rectangular shape, since recombination affects the quantum efficiency directly as seen the figure 4.8. External quantum efficiency and internal efficiency are different from each other. In external quantum efficiency, optical losses are taken into consideration like reflection, whereas in internal quantum efficiency, the effect of reflected light is not included in the measurement.

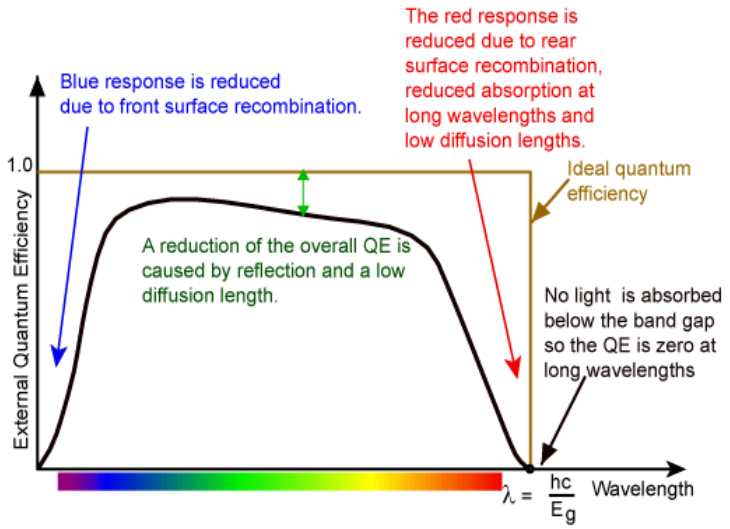


Figure 4. 8: Quantum efficiency of ideal and real silicon solar cell [31]

Photons having short wavelength are absorbed at the front of solar cell and thus charge carriers are generated in the vicinity of front surface of the cell. Therefore, these carriers can be exposed to surface recombination. For this reason, quantum efficiency is affected by surface recombination at the front surface short wavelength. Lower surface recombination velocity can increase the quantum efficiency [31]. As for long wavelength, quality of back surface field affects the quantum efficiency since long wavelength reaches the rear surface of solar cell without being absorbed by Si. The thickness of the wafer is important for the effectiveness of the back side. For thinner wafer, increasıng optical path in the solar cell might be important.

4.2.1. Quantum Efficiency Setup

Quantum efficiency setup consists mainly of halogen light source, chopper, monochromator, current amplifier and lock-in as shown in the Figure 4.9. Light is modulated with a chopper and separated into different wavelength with the help of monochromator and focused into the sample by a lens. The sample cell produces a photocurrent under this illumination. The part of the photocurrent which has the same modulation frequency as the chopper frequency is measured by the lock-in amplifier, for each wavelength. The number of charge carriers is deduced from this photocurrent (A) by dividing it into the charge of one electron. Similarly, the number of incident photons is measured using a photodetector (UV enhanced Silicon) with a known detectivity (A/W). The measured photocurrent (A) is divided by this detectivity and the energy of a single photon at that wavelength, to give the number of incident photons. The ratio of the number of electrons to the number of photons gives the external quantum efficiency.

4.2.2. Quantum Efficiency Results

Results of quantum efficiency measurement are displayed in Figure 4.10. From Figure 4.10(a), we see that p-type solar cells have considerably better results when compared to n-type samples. Firstly, quantum efficiency result of n-type sample produced by 1^{st} approach shows that n+-n-p+ structure is not enough to inject charge carriers to obtain good performance. Although results of other n-type samples produced by 2^{nd}, 3^{rd}, 4^{th} and 5^{th} approaches are nearly the same, 5^{th} approach seems to be slightly better. However, decrease in quantum efficiency is observed at short wavelength. It indicates that front surface recombination is effective, which results from inadequate surface passivation. In Figure 4.10 (b), it is seen that n-type sample produced by 5^{th} approach has better result among the other n-type samples double side passivated with Si_3N_4-SiO_2.

When taken into consideration Figure 4.10, difference in quantum efficiency between n-type samples double side passivated with Si_3N_4-SiO_2 stack layer and n-type samples double side passivated with only Si_3N_4, it can be said that stack layer provides better surface passivation at short wavelength especially.

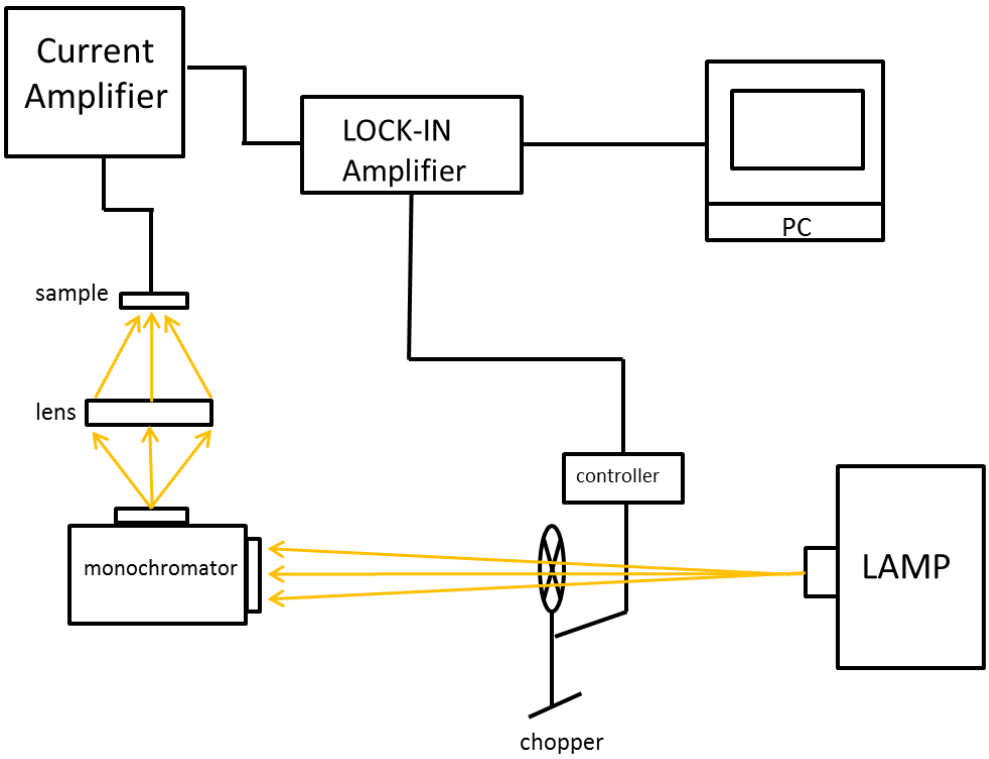
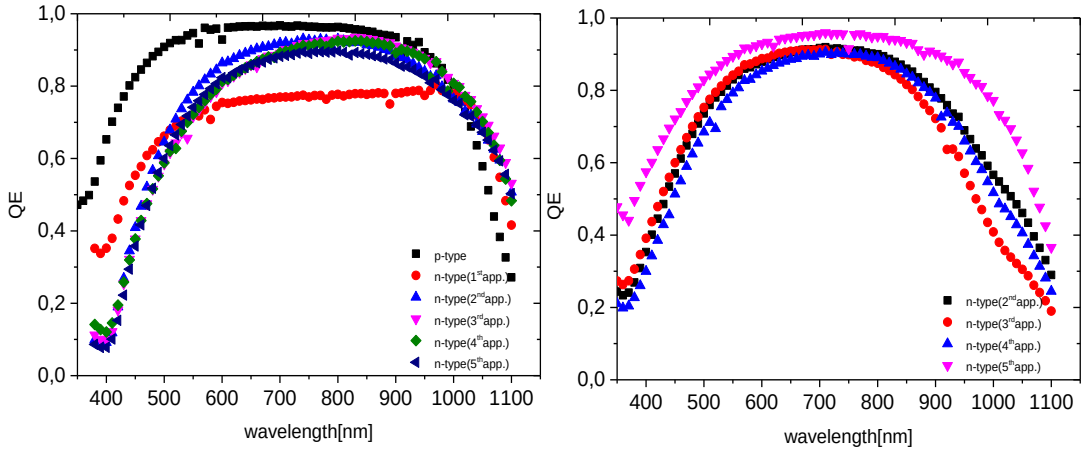


Figure 4. 10: Schematic of quantum efficiency measurement setup



(a) (b)

Figure 4. 11: Results of quantum efficiency measurement of double sides passivated samples (a) with Si_3N_4, (b) with Si_3N_4-SiO_2

The effect of passivation on external quantum efficiency for n-type samples can be observed in Figure 4.11. As shown the Figure 4.11, although front surface recombination is observed

on samples, better passivation for n-type samples is obtained by Si_3N_4-SiO_2 stack layers at short wavelength especially. The remarkable result is observed for n-type samples produced by 5th approach. For p-type emitter, it has already known fact that Si_3N_4-SiO_2 stack layer provides better passivation. Thus, it is expected result.

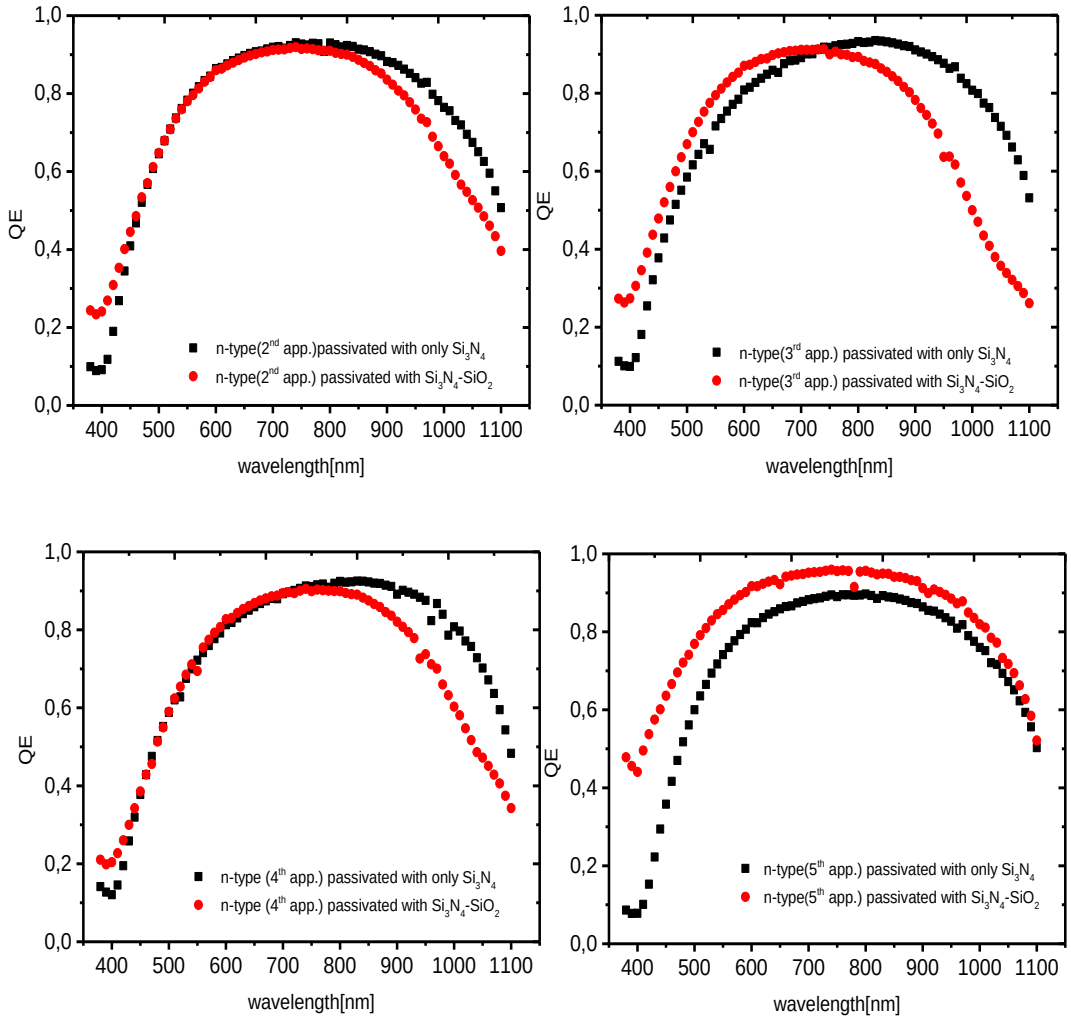


Figure 4. 12: Comparison the quantum efficiency results between n-type samples produced by 2nd, 3rd, 4th and 5th approach but different passivated

Quantum efficiency measurement is also performed from the back side of samples. The results of quantum measurement from the back side of the samples are given Figure 4.12. From Figure 4.12 (a), the n-type sample produced by 5th approach is relatively outstanding among the n-type samples double sides passivated with only Si_3N_4. At long wavelength, the measured loss is related to front surface recombination as measured from the front surface measurements.

Figure 4.12 (b) gives the quantum efficiency results from the back side of n-type samples double side passivated with Si_3N_4-SiO_2 stack layers. It can be seen obviously that the remarkable efficiency has 5th approach, but passivation layers of other samples are far away from the desirable properties

In SunsVoc experiment, by eliminating the metallization effect, n-type sample produced by 5th approach had the best values in terms of efficiency as can be shown Table 4.2. Results of SunsVoc measurement are consistent with these quantum efficiency results.

I-V measurement gave different results in terms of performance of samples since metallization and firing process affect directly. It is clear that metallization needs to be improved for this technology.

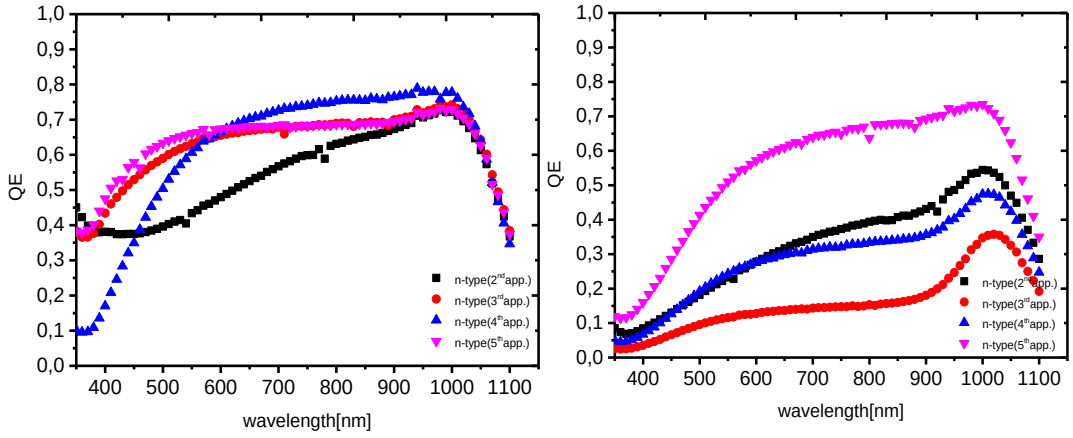


Figure 4. 13: Results of quantum efficiency measurement of double sides passivated samples (a) with Si_3N_4, (b)with Si_3N_4-SiO_2

CHAPTER 5

CONCLUSION

The majority of commercial solar cell is based on crystalline silicon technology, which results from well-known technology of silicon and its abundance. Solar cells are mostly produced by using p-type substrate in the photovoltaic market. However, in recent years, solar cells based on n-type substrate are considered to be alternative way of fabrication of high efficiency solar cells due to the superior properties of n-type material. There are several advantages of n-type silicon when compared to p-type silicon. Firstly, it is a well-known fact that n-type silicon has more tolerance for metallic impurities such as Fe, which probably leads to higher diffusion length of minority carriers. Also, since p-type silicon is doped with boron, it contains boron-oxygen complexes, which cause light induced degradation and affects minority carrier lifetime negatively.

However, fabrication steps of solar cell based on n-type silicon are more difficult than p-type silicon. First problem is the boron diffusion process. It requires higher temperature than phosphorus diffusion. Other problem is the passivation of p-layer. Since silicon nitride includes positive fixed charges, it is not adequate for passivation of emitter region of n-type solar cell. Contrary to p-type cells, Si_3N_4 passivation contains positive charges that prevent the accumulation of charges causing higher surface recombination. Silicon dioxide is suggested for passivation because it is a good material for p-type layer, but its growth takes a longer time. Another problem is metallization of n-type solar cell. Creation of BSF is also difficult compared to p-type.

The aim of this research was to fabricate p-type and n-type silicon solar cells on float zone silicon wafers and compare their performance of them. The reason why float zone wafer was used is that wafers grown by float zone technique has high purity since growth process does not include crucible.

For solar cell production, both n-type and p-type oriented single crystalline silicon wafers (100) were used. Thickness of wafers was nearly $180\mu m$.

To produce the p-type solar cell, in GUNAM laboratory, conventional process steps used in the industry today were used. These experimental steps consist of saw damage etching, texturing, phosphorus diffusion, anti-reflective thin film coating, metallization, firing and edge isolation for p-type solar cell production.

Saw damage etching process had to be optimized firstly. Since saw damage etching results in a homogenous surface, it has a great importance and effect on the following texturing process. Then, texturing process was optimized to enhance the absorption and to reduce the

reflection. It enhances the current output of solar cells directly. Optimized values for both process were determined for both p-type and n-type wafers.Different approaches were tried to produce n-type solar cell since the fabrication of n-type cells has not an industry standard process yet.

In the first approach, the standard p-type solar cell process was applied to the n-type solar cell production as the first approach where aluminum rear contact was formed. By means of this way n^+-n-p^+ structure was formed. In addition, new process methodologies were developed to form p-n-n^+,structure. The second approach included KOH etching process to etch p doped layer from the back side of the wafer. The third and fourth approach were almost similar, but the only difference between them was phosphorous and boron doping sequence. Phosphorous doping was performed after the boron doping in third approach. As for the fourth approach, boron doping was done by placing the wafers back to back in this approach.

After p-n-n+ structures were formed by different approaches, anti-reflective coating was deposited on all wafers. However, due to p-type emitter, deposited silicon nitrate was not a suitable passivation layer. For this reason, two different passivation layer structures were applied on solar cells. First one was a double side passivation only with silicon nitride, the other one was double side passivation with silicon dioxide and silicon nitride stack layer.

Then, silver grid structure was screen printed on front side of the all passivated wafers. Aluminum was screen printed on the rear side of the p-type and n-type produced in first approach, whereas silver grid structure was screen printed on the rear side of the rest of the n-type wafers produced by 2^{nd}, 3^{rd}, 4^{th} and 5^{th} approaches.

Then, to determine the performance of solar cells, I-V measurement under dark and illumination, and quantum efficiency measurement were performed and results of them was analyzed.

According to results of these measurements, p-type solar cell was far superior to n-type solar cells in terms of performance. Considering the fact that we are studying this system for the first time, these results might be expected. However, the results are far from showing the expected advantage of the n-type cells. When results of quantum efficiency are taken into consideration, it was seen that double side passivation with silicon nitride and silicon dioxide stack layer was more effective to passivated the surfaces for n-type cells. However, the effect of BSF was not sufficient for n-type cells passivated with stack layer, which results in lower efficiency.

The solar cell performance was determined with I-V measurements, where we generally observed lower performance from the n-type cells. We identified that the metallization is the main reason for this low performance. Low shunt resistance values and high series resistance values indicated that silver grids could not suitable for n-type solar cells. In literature, silver-aluminum grid structure is screen printed on the front surface of high efficiency n-type cells. However, in this study, only silver grid structure was used. It may affect the quality of metallization.

For further research, metallization should be optimized for n-type solar cells. The suitable material and grid structure should be found. In addition, edge isolation can be seen as another problem for n-type cells. Parameters of edge isolation should be optimized.

REFERENCES

[1] M. P. Gaëtan Masson, Marie Latour, Manoël Rekinger, Ioannis-Thomas Theologitis, "Global Market Outlook For Photovoltaics Until 2015" European Photovoltaic Industry Association, 2011.

[2] J. Nelson, *The Physics of Solar Cells*, 1st ed. London, England: Imperial College Press, 2003.

[3] "PVCDROOM." [Online]. Available: http://pvcdrom.pveducation.org/MANUFACT/FIRST.HTM. [Accessed: 15-Aug-2013].

[4] "Photovoltaic Timeline." [Online]. Available: http://inventors.about.com/od/timelines/a/Photovoltaics.htm. [Accessed: 15-Aug-2013].

[5] W. Future, E. Summit, and A. Dhabi, "Renewable Energy : Capturing the Potential" 2013.

[6] M. Z. Hussin, A. Yaacob, R. A. Rahman, Z. M. Zain, S. Shaari, and A. M. Omar, "Monitoring results of Malaysian Building Integrated PV Project in Grid-connected Photovoltaic system in Malaysia" Energy and Power, vol. 2, no. 3, pp. 39–45, May 2012.

[7] I. T. Roadmap, "International Technology Roadmap for Photovoltaic (ITRPV) Results 2012" March, 2013.

[8] "Different Generations of Solar Cells" [Online]. Available: http://org.ntnu.no/solarcells/pages/generations.php. [Accessed: 10-Aug-2013].

[9] S. M. Sze, *VSLI Technology*, 2nd ed., M. Hill, Ed. India: McGraw-Hill Education Pvt Limited, 1983.

[10] S.M. Sze, *Semiconductor Device: Physics and Technology*, 2nd ed.: John Wiley and Sons, 2002.

[11] "PVCDROOM." [Online]. Available: http://pveducation.org/pvcdrom/manufacturing/float-zone-silicon. [Accessed: 07-Aug-2013].

[12] T. Clausen, J. Vedde, L. Jensen, A. Nielsen, O. Andersen, T. L. Larsen, and A. M. Jorgensen, "Thin silicon solar cells fabricated on cost optimized float zone silicon," 3rd World Conference on Photovoltaic Energy Conversion 2003 Proceedings, vol. 2, 2003.

[13] “Solar Spectrum.” [Online]. Available: http://www.zianet.com/daystar/Spectrum.html. [Accessed: 05-Aug-2013].

[14] “Open Circuit Voltage” [Online]. Available: http://pveducation.org/pvcdrom/solar-cell-operation/open-circuit-voltage. [Accessed: 01-Aug-2013].

[15] Industrially Feasible Rear Side Concept for N-Type Silicon Solar Cells Approaching 700 mV of Voc” 25th European Photovoltaic Solar Energy Conference and Exhibition, 2010.

[16] H. Park, S. Kwon, J. S. Lee, H. J. Lim, S. Yoon, and D. Kim, “Improvement on surface texturing of single crystalline silicon for solar cells by saw-damage etching using an acidic solution” Solar Energy Materials and Solar Cells, vol. 93, no. 10, pp. 1773–1778, 2009.

[17] D.L. King and M.E. Buck, "Experimental Optimization of an Anisotropic Etching Process for Random Texturization of Silicon Solar Cells," in *22nd IEEE Photovoltaics Specialist Conference*, 1991, pp. 303-308.

[18] W. D. Callister, “Materials Science and Engineering” Materials Science and Engineering A, vol. 29, pp. 499–504, 2009.

[19] “Concentration Distribution of Drive in” [Online]. Available: http://cnx.org/content/m36703/latest/?collection=col11170/latest. [Accessed: 13-Jul-2013].

[20] A. R. Burgers, R.C.G. Naber, A.J.Carr, P.C.Barton, L.J.Geerligs, Xiong Jingfeng, et al., "19.5% Efficient N-type Si Solar Cells Made In Production" in *25th European Photovoltaic Solar Energy Conference and Exhibition 5th World Conference on Photovoltaic Energy Conversion*, Valencia, 2010

[21] “N-type silicon solar cell with Al back junction : results and modeling ” [Online]. Available: http://www.sintef.no/project/Foxy/Publications/NREL n-type cells 060724.pdf. [Accessed: 10-Aug-2013].

[22] D. Saynopva, V. Mihailetchi, L. Geerligs et al., "Comparison of High Efficiency Solar Cells on Large Area N-type and P-type Silicon Wafers with Screen Printed Aluminum Alloyed Rear Junction" in *33rd IEEE Photovoltaic Specialists Conference*, 2008.

[23] A. Edler, J. Jourdan, V. D. Mihailetchi, R. Kopecek, R. Harney, D. Stichtenoth, T. Aichele, A. Grochocki, J. Lossen, T. S. Böscke, and H. Krokoszinski, “Screen Printed n-type Silicon Solar Cells for Industrial Application” in 25th European Photovoltaic Solar Energy Conference, 2010, pp. 1446–1448.

[24] “Anti-Reflective Coating” [Online]. Available: http://pveducation.org/pvcdrom/design/anti-reflection-coatings. [Accessed: 02-Jul-2013].

[25] J.-F. Lelièvre, J. De la Torre, A. Kaminski, G. Bremond, M. Lemiti, R. El Bouayadi, D. Araujo, T. Epicier, R. Monna, M. Pirot, P.-J. Ribeyron, and C. Jaussaud, “Correlation of optical and photoluminescence properties in amorphous SiN_x:H thin

films deposited by PECVD or UVCVD" *Thin Solid Films*, vol. 511–512, pp. 103–107, 2006.

[26] R. C. G. Naber, N. Guillevin, A. R. Burgers, L. J. Geerligs, A. W. Weeber, "ECN N-type Silicon Solar Cell Technology" in *34th IEEE PVSC*, Philadelphia, 2009, pp. 990-992.

[27] J. Schmidt and M. Kerr, "Surface passivation of silicon solar cells using plasma-enhanced chemical-vapour-deposited SiN films and thin thermal SiO_2 / plasma SiN stacks" *Vacuum*, vol. 16, pp. 164–170, 2001.

[28] Ms. Thesis , L. Shi, *Contact Resistance Study on Polycrystalline Silicon Thin Film Solar Cells on Glass*: The University of New South Wales, 2008.

[29] Ms. Thesis, O. Demircioğlu, *Optmization of Metallization in Crystalline Silicon Solar Cells*: Middle East Technical University, 2012.

[30] Ms. Thesis, F. Es, *Fabrication and Characterization of Single Crystalline Silicon Solar Cells*: Middle East Technical University, 2010.

[31] "Quantum Efficiency" [Online]. Available: http://pvcdrom.pveducation.org/CELLOPER/QUANTUM.HTM. [Accessed: 01-Jul-2013].

APPENDIX A

SOLUTION OF FICK'S SECOND LAW

In this section, Fick's second law (3.10) which is given as

$$\frac{\partial C}{\partial t} = D\frac{\partial^2 C}{\partial x^2}\ , \tag{A.1}$$

will be solved for the boundary conditions

$$C(x,0) = 0, \quad C(0,t) = C_S, \qquad C(\infty,t) = 0\ , \tag{A.2}$$

where C_S is a constant. This differential equation can be solved by using Fourier transformation as shown below.

Since we are working on the line [0,∞)

$$C(x,t) = 0 \qquad \text{when } x < 0\ . \tag{A.3}$$

Let's do a Fourier transform in the x coordinate.

$$\tilde{C}(q,t) = \frac{1}{\sqrt{2\,\pi}}\int_{-\infty}^{\infty} C(x,t)e^{iqx}dx \tag{A.4}$$

Whose inverse transform is

$$C(x,t) = \frac{1}{\sqrt{2\,\pi}}\int_{-\infty}^{\infty} \tilde{C}\,(q,t)e^{-iqx}\,dq\,. \tag{A.5}$$

When (A.3) is used, (A.4) reduces to,

$$\tilde{C}(q,t) = \frac{1}{\sqrt{2\,\pi}} \int_0^{\infty} C(x,t) e^{iqx} dx \,. \tag{A.6}$$

Both sides of the equation (A.1) are multiplied by e^{iqx} and $\frac{1}{\sqrt{2\pi}}$ and integrated from zero to infinity with respect to x then we get

$$\frac{\partial}{\partial t}\left(\frac{1}{\sqrt{2\,\pi}} \int_0^{\infty} C(x,t) e^{iqx} dx\right) = \frac{D}{\sqrt{2\,\pi}}\left(\int_0^{\infty} \frac{\partial^2 C(x,t)}{\partial x^2} e^{iqx} dx\right). \tag{A.7}$$

The right hand of side of (A.7) can be manipulated as

$$\frac{\partial^2 C(x,t)}{\partial x^2} e^{iqx} = \frac{\partial^2}{\partial x^2}\left(C(x,t) e^{iqx}\right) - 2\frac{\partial}{\partial x}\left(C(x,t)\frac{\partial}{\partial x} e^{iqx}\right) + C(x,t)\frac{\partial^2}{\partial x^2} e^{iqx} \tag{A.8}$$

Since we have,

$$\frac{\partial}{\partial i} e^{iqx} = iq e^{iqx} \tag{A.9}$$

$$\frac{\partial^2}{\partial x^2} e^{iqx} = -q^2 e^{iqx} \,. \tag{A.10}$$

Then, after integration by parts, (A.7) can be written as follows;

$$\frac{\partial}{\partial t}\tilde{C}(q,t) = \frac{D}{\sqrt{2\pi}}\left(\frac{\partial}{\partial x}\left[C(x,t)\, e^{iqx}\right]_0^{\infty} - 2\left[C(x,t) iq\, e^{iqx}\right]_0^{\infty}\right) - q^2 D\, \tilde{C}(q,t)\,, \tag{A.11}$$

Where we used (A.6). Using the boundary conditions (A.2), we get

$$\frac{\partial}{\partial t}\,\tilde{C}(q,t) - \frac{2Diq}{\sqrt{2\pi}} C_S = -q^2 D\, \tilde{C}(q,t). \tag{A.12}$$

This is now an ordinary differential equation which can be solved in following way: First, we multiply (A.12) with an arbitrary integrating function $\mathrm{f(t)}$ which obeys

$$\frac{1}{\mathrm{f(t)}}\frac{\partial \mathrm{f(t)}}{\partial \mathrm{t}} = \mathrm{q^2 D}\,. \tag{A.13}$$

Therefore, (A.12) reads as,

$$\frac{\partial}{\partial \mathrm{t}}\left[\mathrm{f(t)}\tilde{\mathrm{C}}(\mathrm{q,t})\right] = \frac{2\mathrm{Diq}}{\sqrt{2\pi}}\mathrm{C_S f(t)}\,. \tag{A.14}$$

Note that, (A.14) can be written as,

$$\frac{\partial}{\partial \mathrm{t}}\,\tilde{\mathrm{C}}(\mathrm{q,t}) + \frac{1}{\mathrm{f(t)}}\frac{\partial \mathrm{f(t)}}{\partial \mathrm{t}}\tilde{\mathrm{C}}(\mathrm{q,t}) = \frac{2\mathrm{Diq}}{\sqrt{2\pi}}\mathrm{C_S f(t)}\,. \tag{A.15}$$

And (A.13) guarantees that (A.15) is equivalent to (A.12). The solution of (A.13) is

$$f(t) = f_0 e^{q^2 Dt}\,, \tag{A.16}$$

where f_0 is an integration constant. Putting (A.16) into (A.15), we get

$$\frac{\partial}{\partial \mathrm{t}}\left[\mathrm{e^{q^2 Dt}}\,\tilde{\mathrm{C}}(\mathrm{q,t})\right] = \frac{2\mathrm{Diq}}{\sqrt{2\,\pi}}\mathrm{C_S}\;\mathrm{e^{q^2 Dt}}\,. \tag{A.17}$$

To obtain $\tilde{C}(q,t)$, (A.17) is integrated with respect to t;

$$\int_0^{\mathrm{t}} \frac{\partial}{\partial \mathrm{t}}\left[\mathrm{e^{q^2 Dt}}\,\tilde{\mathrm{C}}(\mathrm{q,t})\right]\mathrm{dt} = \frac{2\mathrm{Diq}}{\sqrt{2\,\pi}}\mathrm{C_S}\;\int_0^{\mathrm{t}} \mathrm{e^{q^2 Dt}}\mathrm{dt}\;. \tag{A.18}$$

From (A.18), $\tilde{C}(q,t)$ is found as

$$\tilde{C}(q,t) = \tilde{C}(q,0)e^{-q^2Dt} + \frac{2i}{q\sqrt{2\pi}}C_S \; - \frac{2i}{q\sqrt{2\pi}}C_S \; e^{-q^2Dt} . \tag{A.19}$$

We still have to find $\tilde{C}(q,0)$. To do this, let t=0 in (A.5), to obtain

$$C(x,0) = 0 = \frac{1}{\sqrt{2\pi}}\int_{-\infty}^{\infty} \tilde{C}\,(q,0)e^{-iqx}\,dq\,, \tag{A.20}$$

which constraints $\tilde{C}(q,0)$ as

$$\tilde{C}(q,0) = 0\,. \tag{A.21}$$

Then, (A.19) can be written as

$$\tilde{C}(q,t) = \frac{2i}{q\sqrt{2\pi}}C_S\,\left(1 - e^{-q^2Dt}\right). \tag{A.22}$$

By putting (A.22) into (A.5) , $C(x,t)$ is found as

$$C(x,t) = \frac{i}{\pi}C_S\,\left(\int_{-\infty}^{\infty}\frac{1}{q}(1 - e^{-q^2Dt})e^{-iqx}dq\,\right). \tag{A.23}$$

Before we simplify this expression, let us check that whether (A.23) satisfies the boundary conditions or not. The second boundary condition in (A.2) is

$$C(0,t) = \frac{i}{\pi}C_S\,\left(\int_{-\infty}^{\infty}\frac{1}{q}(1 - e^{-q^2Dt})dq\,\right), \tag{A.24}$$

where the integral can be found with the help of Mathematica as,

$$\int_{-\infty}^{\infty} \frac{1}{q}\left(1 - e^{-q^2 Dt}\right)dq = -i\,\pi \quad . \tag{A.25}$$

Therefore, the boundary condition is satisfied

$$C(0,t) = C_S \ .$$

Further simplify the expression (A.23), let us expand e^{iqx} and drop the cosine term since it gives an odd integral

$$C(x,t) = \frac{i}{\pi} C_S \left(\int_{-\infty}^{\infty} \frac{1}{q}(-i)\sin qx\left(1 - e^{-q^2 Dt}\right)dq \right). \tag{A.26}$$

By using Mathematica the integration of (A.26) can be found as

$$C(x,t) = C_S \left(1 - \operatorname{erf}\left(\frac{x}{2\sqrt{Dt}}\right)\right) , \tag{A.27}$$

where erf (x) is the error function. The result can also be written in the form of the complementary error function as below

$$C(x,t) = C_s \operatorname{erfc}\left(\frac{x}{2\sqrt{Dt}}\right) . \tag{A.28}$$