INTEGRATED CIRCUIT DESIGN FOR FLIP-CHIP BONDED CAPACITIVE MICROMACHINED ULTRASONIC TRANSDUCERS

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
MIDDLE EAST TECHNICAL UNIVERSITY

BY

MOHAMMAD MAADI

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF MASTER OF SCIENCE
IN
ELECTRICAL AND ELECTRONICS ENGINEERING

SEPTEMBER 2013

Approval of the thesis:

INTEGRATED CIRCUIT DESIGN FOR FLIP-CHIP BONDED CAPACITIVE MICROMACHINED ULTRASONIC TRANSDUCERS

Submitted by **MOHAMMAD MAADI** in partial fulfillment of the requirements for the degree of **Master of Science in Electrical and Electronics Engineering Department, Middle East Technical University** by,

Prof. Dr. Canan Özgen
Dean, Graduate School of **Natural and Applied Sciences** _____

Prof. Dr. Gönül Turhan Sayan
Head of Department, **Electrical and Electronics Engineering** _____

Assoc. Prof. Dr. Barış Bayram
Supervisor, **Electrical and Electronics Eng. Dept., METU** _____

Examining Committee Members:

Prof. Dr. Cengiz Beşikçi
Electrical and Electronics Engineering Dept., METU _____

Assoc. Prof. Dr. Barış Bayram
Electrical and Electronics Engineering Dept., METU _____

Prof. Dr. Tayfun Akın
Electrical and Electronics Engineering Dept., METU _____

Assoc. Prof. Dr. Haluk Külah
Electrical and Electronics Engineering Dept., METU _____

Dr. Murat Tepegöz
Mikrosens Elektronik San. ve Tic. A.Ş. _____

Date: **02.09.2013**

I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

Name, Last name: Mohammad Maadi

Signature:

ABSTRACT

INTEGRATED CIRCUIT DESIGN FOR FLIP-CHIP BONDED CAPACITIVE MICROMACHINED ULTRASONIC TRANSDUCERS

Maadi, Mohammad

M. Sc., Department of Electrical and Electronics Engineering

Supervisor: Assoc. Prof. Dr. Barış Bayram

September 2013, 176 pages

In previous decades, the applications of ultrasound technologies in medical imaging and therapeutic systems have significantly increased. In conventional ultrasound systems, the transducer array is separated from the electronic instrumentation with multicore physical cabling. However, connection cables make the system too bulky and degrade the receive sensitivity in ultrasound 3D imaging applications because of the capacitance of long cables. The interface electronics for phased array ultrasound systems (imaging or therapeutic) use the ultrasound transducer array to steer a focused beam over the volume being fired or imaged with eliminating bulky cables. Among the available types of ultrasound transducers, CMUTs (capacitive micromachined ultrasonic transducers) are particularly interested because they do not suffer from self-heating effects in comparison with their piezoelectric counterparts. Hence, the integration of CMUTs with front-end electronics can be used in high power and continuous wave (CW) applications such as high intensity focused ultrasound (HIFU).

The aim of this study is to design highly flexible and programmable transmit beam-former ASIC using a HV 0.35 μm CMOS technology to be flip-chip bonded to a 4X4 CMUT array for ultrasound therapeutic applications. However, proposed IC can be used as a transmitter circuitry in color Doppler 3D imaging applications. In our designed chip, each CMUT element is provided by an 8-bit shift register, an 8-bit comparator, a one-shot circuit with adjustable pulse width, a programmable pulse train generator and a high voltage pulser circuit. The interface electronics can generate two types of outputs with programmable focusing delays to 16 ultrasound transducer elements in different modes: The first mode is

for generating single pulses in which the one-shot circuits adjust the width of the pulses from a few nanoseconds to 650 ns with enough resolution for different operating frequencies of ultrasound transducer. The second one has been considered for generating controllable pulse trains. The frequency of the generated pulse trains can be selected using digitally controlled oscillator (DCO) with three 5-bit digitally controlled delay elements (DCDE), frequency down conversion (FDC) circuit and combinational logics. In DCDE circuit depending on the 5-bit digital input vector, 32 different delay settings in the range of 5 to 50 ns can be obtained. For easy prediction of the DCDE delay time for a given digital input vector, we tried to generate a monotonic delay behavior with ascending binary input patterns in different small areas. Since, the stability of designed DCO-DCDE circuit is very important, the circuit was designed stable in -10% VDD and in 25, 50 and 75 ℃ temperatures variations. The temperature variation values for 25 to 50 ℃ and 25 to 75 ℃ are less than 5%. Furthermore, the circuit showed less than 5% variation for -10% supply reduction. The average power consumption of designed 5-bit DCDE with two buffers is 165 and 844 µw when the circuit generates delays of 21 ns (for generating 20 MHz pulse trains when the digital input vector is 11111) and 1.54 ps (for generating 650 GHz pulse trains when the digital input vector is 00000), respectively. To have a better resolution for the frequency of the pulse trains, we added frequency down conversion (FDC) circuit to DCO-DCDE. The output of the FDC circuit can be selected using an 8X1 multiplexer to generate 256 different pulse train frequencies in the range of 1 to 10 MHz with good resolution. Single pulse and pulse train modes are separated from each other by a 1X2 demultiplexer. At final stage the amplitudes of single pulses or pulse trains are increased up to 45 V using high voltage (HV) pulsers with THKOX module. The outputs of these pulsers are connected to flip-chip bonding pads and then the top electrodes of the CMUTs. When the magnitude of the pulses is 45 V, the rise and fall time of the output signals are 5 and 8 ns for 2.5 pF capacitive loads, respectively. The slew rate and figure of merit of the circuit at V_{HV} = 45 V is 1.89 V/µs and 0.51 ns/(µm.V), respectively. These kinds of circuits have dramatic power consumptions. Our designed HV pulser circuit consumes 51.66 mw for 45 V output signals. Using an external control system like FPGA, the 8-bit global counter can be incremented from 1 to 256 so that each pulser circuit fires correspondent CMUT element when its stored shift register value is identical with the value of global counter.

In the frame of this research, a different kind of ultrasound therapeutic interface electronics for 16X16 CMUT array has been designed in HV 0.35 µm CMOS technology. The proposed ASIC includes the same driver (LV) circuitry but 90 V high voltage pulsers with HVTHKOX module.

ÖZ

FLİP-ÇİP YAPIŞTIRMALI KAPASİTİF MİKROÜRETİLMİŞ ULTRASONİK ÇEVİRGEÇLER İÇİN ENTEGRE DEVRE TASARIMI

Maadi, Mohammad

Yüksek Lisans, Elektrik ve Elektronik Mühendisliği Bölümü

Tez Yöneticisi: Doç. Dr. Barış Bayram

Eylül 2013, 176 sayfa

Son on yıllarda ultrason teknolojilerinin medikal ve terapatik sistemlerdeki kullanımı kayda değer miktarda artmıştır. Geleneksel ultrason sistemlerinde çevirgeç dizisi elektronik ölçüm sisteminden çok damarlı fiziksel kablolar ile ayrılır. Fakat bağlantı kablolaları sistemi hantal yapmakta ve 3 boyutlu görüntüleme sistemlerinde alıcı hassasiyetini kabloların uzun olmasından dolayı düşürmektedir. Faz dizisi ultrason sistemlerinde (görüntüleme ve ya terapatik) elektronik arayüzü ultrason verici dizisinde hantal kablolar yerine görüntülenecek veya ateşelencek hacimde bir noktaya odaklanmak için kullanılır. Varolan ultrason vericilerinden CMUT'lar (Capacitive Micromachined Ultrasonic Transducers) diğer pizoelektrik eşdeğerleriyle kıyaslandığında kendini ısıtma etkisi olmadığından özellikle ilginçtir. Bu yüzden CMUT'ların arayüz elektroniği ile entegrasyonu yüksek yoğunlukta odaklanmış yüksek güç sürekli dalga uygulamalarında kullanılabilir.

Bu çalışmanın amacı oldukça esnek ve programlanabilir bir iletilen dalga şekillendirici ASIC'i 0.35 µm yüksek voltaj CMOS teknolojisi kullanarak flip-çip şeklinde 4x4'lük CMUT dizisine ultrason terapatik uygulamalar için bağlanacak şekilde tasarlamaktır. Fakat önerilen entegre devre 3 boyutlu renkli Doppler uygulamalarında verici olarak da kullanılabilir. Tasarlanan devremizde her CMUT elemanını süren 8-bit ötelemeli kaydedici, 8 bit kıyaslayıcı ve ayarlanabilir darbe genişliğine sahip tekli darbe üreteci, programlanabilir darbe katarı üreteci ve bir adet yüksek voltaj darbe devresi vardır. Arayüz elektroniği programlanabilir odaklanma gecikmesine sahip çıktıları 16 adet ultrason vericiye farklı modlarda sunabilir. İlk mod tekli darbeler içindir. Bu modda tekli darbe üreteci darbenin genişliğini bir kaç nano saniyeden 650ns'ye kadar ultrason vericinin farklı çalışma

frekansları için yeterli çözünürlükte ayarlar. İkinci mod kontrol edilebilir darbe katarları üretmek için düşünülmüştür. Üretilen darbe katarının frekansı 3 adet 5-bit sayısal olarak kontrol edilen gecikme elemanı (SOKEGE), frekansı aşağı çeviririci (FAÇ) ve mantık devrelerine sahip sayısal olarak kontrol edilen bir osilatör (SOKEO) ile ayarlanır. SOKEGE devresinde 5-bitlik sayısal girdi vektörüne bağlı olarak 32 farklı gecikme ayarı 5'ten 50ns'ye kadar elde edilebilir. Belirli bir sayısal girdi vektörünün SOKEGE gecikmesini kolayca tahmin etmek için, monoton bir gecikme davranışını farklı küçük alanlarda azalan ikili girdi örüntüleri şeklinde yaratmaya çalıştık. Tasarlanan SOKEO -CDE devresinin kararlılığı çok önemli olduğundan, devre %10 VDD değişimi ve 25,50 ve 75°C sıcaklık değişimlerinde kararlı olacak şekilde tasarlanmıştır. 25'ten 50 °C'a ve 25'ten 75 °C'a olan sıcaklık değişim değerleri %5'ten küçüktür. Ayrıca devre, devre giriş voltajındaki %10'luk bir azalmaya %5'ten küçük bir değişim ile cevap vermiştir. Tasarlanan iki tamponlu 5 bit SOKEGE devresinin ortalama güç harcaması 21 ns (20MHz'lik darbe katarı üretmek için sayısal girdi vektörü 11111) ve 1.54ps (650GHz'lik darbe katarı üretmek için sayısal girdi vektörü 00000) gecikme için sırasıyla 165 ve 844 µW'tır. Darbe katarlarının frekansının çözünürlüğünü iyileştirmek için SOKEO- SOKEGE'ye frekansı aşağı çevirici (FAÇ) devre eklenmiştir. FAÇ devresinin çıktısı 8x1'lik çoklayıcı kullanarak 256 farklı darbe katarı frekansı 1'den 10MHz'e kadar iyi çözünürlükte elde edilebilir. Tekli darbe ve darbe katarı modları birbirinden 1x2'lik ters-çoklayıcı ile ayrılır. Son aşamada tekli darbenin veya darbe katarının genlikleri THKOX modülü ile yüksek voltaj darbe üreteci kullanarak 45 V'a yükseltilir. Bu darbe üreteçlerinin çıktıları flip-çip bağlantı pedleri üzerinden CMUT'ların tepe elektrotlarına bağlanır. Darbenin genliği 45V iken çıktı sinyallerin çıkma ve düşme zamanları 2.5pF'lik kapasitif yükler için sırasıyla 5 ve 8ns'dir. V_{HV} = 45 V iken devrenin eğimi ve erdem değeri sırasıyla 1.89 V/µs and 0.51 ns/(µm.V)dir. Bu tarz devrelerin olağanüstü güç tüketimi vardır. Tasarladığımız Yüksek Voltaj darbe üreteci devresi 45V'luk girdi sinyallerine karşılık 51.66mW harcar. FPGA gibi harici bir kontrol sistemi kullanarak 8bitlik global sayaç 1'den 256'ya kadar artırılır ve her darbe üreteci devre ilgili CMUT elemanını kendi ötelemeli kaydedicisinde saklanan değer'e denk geldiğinde ateşler.

Bu araştırma kapsamında 16x16'lık CMUT dizisi için farklı bir ultrason terapatik arayüz elektroniği Yüksek Voltaj 0.35 µm CMOS teknolojisi için tasarlanmıştır. Önerilen devre, HVTHKOX modülü ile aynı sürücüye (LV) fakat 90 V yüksek voltaj darbe üretecine sahiptir.

To my parents, family and lovely fiancée

ACKNOWLEDGEMENTS

This work is in part supported by the Scientific and Technological Research Council of Turkey (TUBITAK), under grant number of 110E072.

Hereby, I would like to give my best thanks to my thesis Supervisor, Assoc. Prof. Dr. Baris Bayram for all his support and guidance during this project.

I would also express my gratitude to Serra Altınoluk, Serdar Görümlü, Parisa Sharif, Nasim Esmailzadeh, Berker Peköz, Fatih Akyürek, Işık Can, Sedat Doğru and Nicasio Maguu in ULTRAMEMS Research Group who helped me a lot to continue with this research by providing a nice research environment.

I should not forget to thank Dr. Oğuz Altun for his guidance and friendly attitude during the discussion that we had for controlling the IC before sending to fabrication.

I would also thanks to my friends in Middle East Technical University, second dormitory (Yurt.2) and my beloved hometown URMIA who helped me a lot to have a friendly atmosphere during this study.

I would also express my thanks to my friends in Night Driving Club (NDC) who helped me a lot to increase my motivation and insight in all aspects of my life.

In the end, I would like to give my special thanks to my parents, mother and father in law, family and lovely fiancée who helped me emotionally during my life and studies in METU.

TABLE OF CONTENTS

APPENDICES

LIST OF FIGURES

FIGURES

LIST OF TABLES

TABLES

CHAPTER 1

INTRODUCTION

The ultrasound systems technology with a broad variety of applications for real-time 3D imaging and therapeutic medical purposes has been quickly growing during last decades. The advances in Micro Electromechanical Systems (MEMS) and Microelectronics technologies allowed the combinations of microfabricated devices with integrated circuits and bring great advances for medical applications in our daily life. MEMS technology has found commercial achievement in miniaturized structures, sensors, actuators, and microelectronics with a great demand in medical applications. Some of these applications are related with medical imaging (sonography) and therapy. Ultrasound imaging and therapeutic is becoming an important tool in modern medicine technologies for achieving high resolution and high sensitivity systems. These technologies can be used for 3D medical imaging (colored or black and white images) inside patient's bodies using sound waves and echoes or therapeutic applications such as detection of cancer cells, cleaning body from cancer cells by firing them, breaking of kidney stones and etc. Ultrasound technology can also be used in nondestructive testing of structures and products, detection of the objects, obstacles and measuring the distances between them, cleaning, mixing and to accelerating chemical processes.

Medical imaging applications consist of transmitter and receiver systems. The transmitter sends an acoustic wave and from the sound reflected back to the receiver, images are formed. Acoustic waves are sent using ultrasound transducers. These transducers show a mechanical response after they are excited with electrical signals. In imaging applications, the reflected waves make mechanical displacement on transducers and generate electrical signals and subsequently images are formed. On the other hand, in therapeutic applications ultrasound transducers are excited with high energy signals. These signals are harmless while they pass through tissues to inside of the body. In recent clinical applications, high intensity focused ultrasound (HIFU) systems are used for ultrasound transducers based on PZT-8 and PZT-4 (piezoelectric materials) in the range of 1 to 4 MHz [1].

Although, there are many efforts have been done to design and implement ultrasound transducers for medical imaging applications, there are a few works which try to improve the performance of interface electronics required to be used together with ultrasound transducers for CMUT therapeutic applications.

This thesis aims to design flexible and fully controllable beam-former interface electronics of CMUT transducers for ultrasound therapeutic applications. This chapter gives an introduction on the ultrasound transducers motivation and required beam-form generator with a focus on capacitive micromachined ultrasonic transducers (CMUTs) systems. Section 1.1 describes the fundamentals of ultrasound waves by providing some simple definitions. Section 1.2 continues this chapter by providing an overview around the micromachined ultrasound transducers (MUTs) with each subsection describing the piezoelectric micromachined ultrasound transducers (PMUTs) and capacitive micromachined ultrasonic transducers (CMUTs). Section 1.3 explains the typical beam-form generator for micromachined ultrasonic transducers (MUTs) with each subsection discussing the specific design considerations for most commonly available piezoelectric micromachined ultrasound transducers (PMUTs) and capacitive micromachined ultrasonic transducers (CMUTs). Section 1.4 continues this chapter by giving an extensive list of goals and achievements to be considered by this research and Section 1.5 ends this chapter by providing the outline of the thesis including a summary of contents of each chapter.

1.1 Ultrasound Fundamentals

The sounds beyond the human hearing range (20 to 20000 Hz) are called ultrasound. Figure 1.1 shows the diagram of the ultrasound waves. As shown in this figure, the acoustic spectrum has been divided into three ranges of frequencies. Also, the ultrasound range of frequencies itself consist of three regions. Acoustic waves can be used in medical imaging for image formation and medical therapy for detection, firing and cleaning.

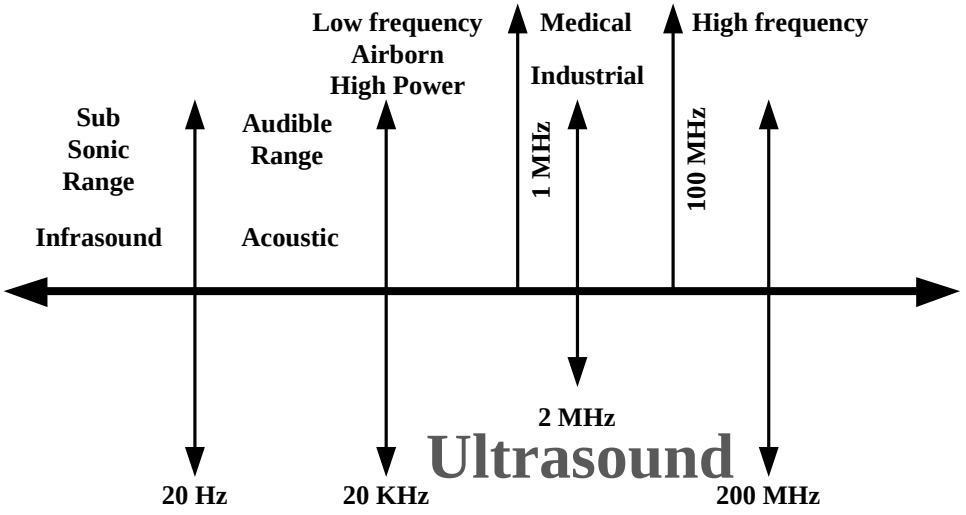


Figure 1.1 Spectrum of the acoustic wave.

Both of ultrasonic and light travel in the form of waves but unlike the light waves which can travel in an empty space (vacuum), elastic medium like liquid or solid is needed for travelling of ultrasound waves. The velocity of ultrasound can be calculated by having the

values of wave length (λ), material sound velocity (C) and the frequency (f) or period of time (T) by $\lambda = C \times T$. The value of the velocity in a perfectly elastic material at a given pressure and temperature is constant.

1.2 Micromachined Ultrasound Transducers (MUTs)

For high frequency medical acoustic imaging and therapeutic applications, the reduction in size of the transducers is limited by the process of fabrication [2]. Micromachined ultrasound transducers (MUTs) enable the fabrication of complete phased array devices at low cost. In fact, a single micromachined ultrasound transducer is composed of a large number of microscopic elements. Since ultrasound transducers are fabricated in array structure, groups of ultrasound elements can be used as a phased array.

As shown in Figure 1.2, the micromachined ultrasound transducer (MUT) includes a circular silicon nitride membranes suspended on heavily doped silicon substrate. When a voltage (ac or dc) is applied between the substrate and the membrane, the membrane is attracted by the electrostatic forces toward the substrate. If the membrane is excited using AC voltages at its operating frequency, large displacement and significant ultrasound waves are generated. In reverse mode, if the membrane is biased correctly and is excited with ultrasound waves at its operating frequency, significant detection currents are generated. Since the dimensions of the membranes are in microns and the values of the residual stress are in hundreds of MPa's, micromachining is considered as a good method for the fabrication of ultrasound transducers.

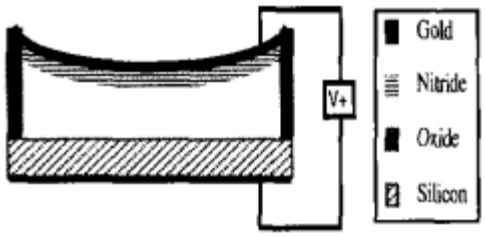


Figure 1.2 Schematic of one element of a MUT [3].

Figure 1.3 shows a typical example of a fully micromachined ultrasound transducer. As can be observed, each micromachined transducer has a flexible membrane (formed by PECVD at 400 ℃) of silicon nitride (Si_3N_4) at a controlled distance from a fixed electrode on insulator, with an air gap between them. Typically, for generating the gap between the membrane and the substrate, 2 μm sacrificial layers (polyimide) are employed. The specifications of fabricated membrane affect the performance of the transducer in terms of bandwidth and sensitivity. The top contact electrode can be formed by sputtering and the intrinsic stress can be controlled by changing RF power.

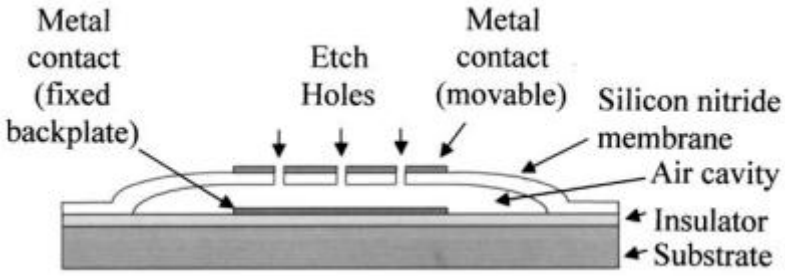


Figure 1.3 Schematic of the micromachined transducer [4].

Different types of ultrasound transducers with a wide range of sizes and shapes can be fabricated [5-8]. Figure 1.4 shows the SEM of a micromachined ultrasound transducer with 1 mm square. The thickness of the membrane is 1 µm and the distance of the air gap from the bottom electrode is 2 µm.

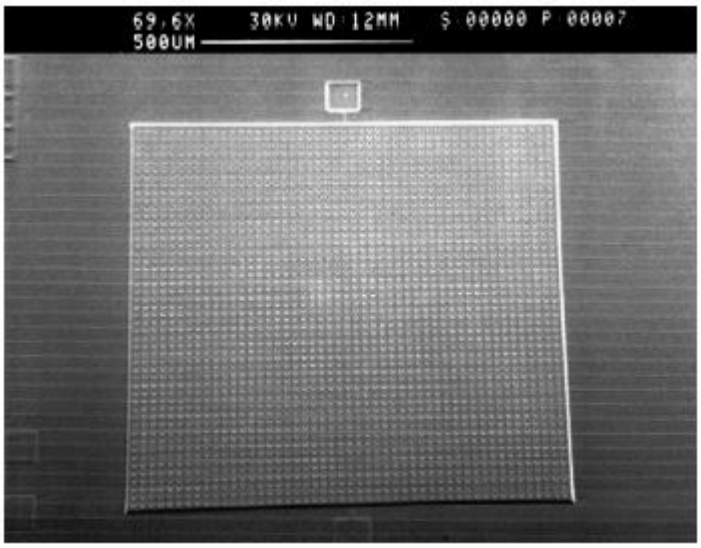


Figure 1.4 SEM of a 1 mm square micromachined ultrasound transducer (MUT) [4].

1.2.1 Piezoelectric Micromachined Ultrasound Transducers (PMUTs)

Among numerous physical principles and techniques, devices that are based on the piezoelectric effect are used in medical applications extensively [9], [10]. The piezoelectric effect is the ability of the material to provide an electric displacement under an applied mechanical stress and similarly, the inverse piezoelectric effect is deformation of the material as a result of an applied electric field [11]. In ultrasound medical applications, the most widely used material among the ferroelectric materials is PZT or zirconate titanate. Instead of using conventional bulk-PZT transducers for high frequency ultrasound imaging

applications, piezoelectric micromachined ultrasound transducers (PMUTs) have been proposed. PMUTs in comparison with conventional PZT transducers have small sizes, higher operations frequencies (over 20 MHz) and low fabrication costs. Hence, several studies have been done around PMUT devices as ultrasound elements [12-25].

A flexible piezoelectric membrane over a cavity makes the structure of a PMUT element. An applied electrical stimulation deforms the cavity mechanically. Figure 1.5 shows the basic structure of a PMUT element with its component layers. Using spin coating process, a PZT film is deposited onto a silicon/silicon oxide (Si/SiO_2) substrate. By photolithographically, to have a 2D array of elements, the PZT film and electrode layers are patterned and then using DRIE (deep reactive ion etching) process, the cavity of the PMUT element is etched in the bulk silicon.

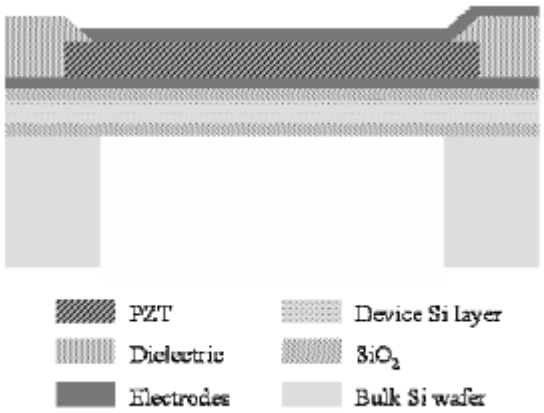


Figure 1.5 Basic structure of the piezoelectric micromachined transducer (PMUT) [4].

As an example, Figure 1.6 shows the cross sectional view of a single element micromachined ultrasonic sensor that has a similar diagram as presented in [26].

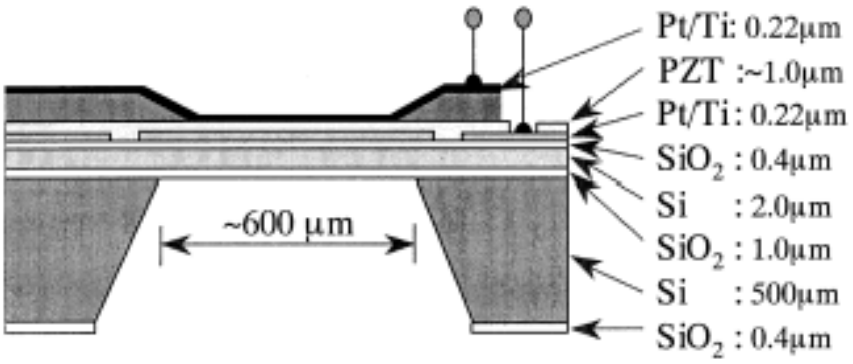


Figure 1.6 Cross sectional view of a single micromachined ultrasonic sensor [27].

1.2.2 Capacitive Micromachined Ultrasonic Transducers (CMUTs)

Since the invention of capacitive micromachined ultrasonic transducers (CMUTs) in the mid-1990s [28], much work has been done to meet the increasing demands of ultrasonic industry in the last two decades. This family of transducers has two major advantages over their piezoelectric counterparts in terms of bandwidth and the possibility of being fabricated with technologies used for integrated circuits [2]. As shown in Figure 1.7, the basic diagram of a CMUT is similar to a conventional capacitor but with some differences. The lower electrode is fixed and has no movement but the upper electrode is a suspended thin movable plate over a vacuum gap. The dimensions of the plate are in the order of tens of micrometers and gap distances in the range of tens to hundreds of nanometers [29].

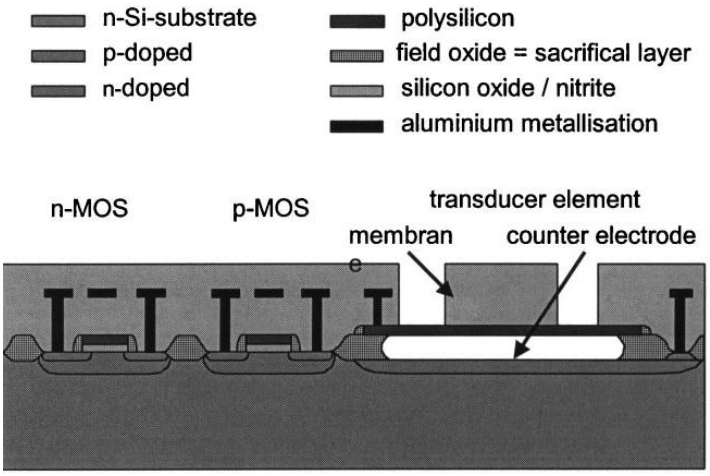


Figure 1.7 Structure of the surface micromachined transducer cell and CMOS transistors [30].

The operating principle of this capacitor cell is simple. When a DC bias voltage is applied between two electrodes of the capacitor, the electrostatic force generated by electric filed attracts the movable plate towards the substrate. The mechanical restoring force due to stiffness of the plate and electrostatic force cancel each other out at a distance between the electrodes where the movable plate finds its new position. If the applied voltage is alternative (AC), the plate generates ultrasound waves. Conversely, if the top plate of the capacitor with constant bias voltage is subjected to ultrasonic waves, an electrical current is produced whose amplitude is a function of the bias voltage, the capacitance of the device and the frequency of the incident wave.

CMUT can operate in conventional, collapsed and collapsed-snapback mode [31]. The factor determining the mode of operation is the bias voltage which establishes an electrostatic attraction force between electrodes. The membrane is suspended over the gap until the bias voltage reaches a value named collapse voltage. At this voltage, the electrostatic force increases faster than the restoring force, so the membrane collapses on the substrate. Figure 1.8 shows the deflection of the membrane to the operation point.

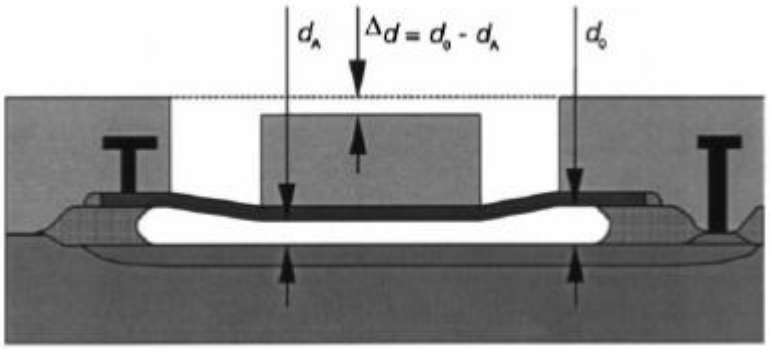


Figure 1.8 Capacitive transducer with membrane deflected to the operation point. The zero voltage gap is d_0 and the operating point gap is d_A [30].

According to what have been mentioned above, it can be observed that the collapse voltage is an important parameter that must be determined. Parallel plate approximation is an approximate method for calculating the collapse voltage [6]. In this method, the average membrane displacement is determined by parallel plate motion model. The major drawback of this method is its inaccuracy which leads to voltages 25% higher than the actual value. The most accurate method to compute the collapse voltage is Finite Element Method (FEM) [32], [33]. FEM analysis uses iteration method so depending on the number of required iterations it may take several hours to complete. In [34] a semi-analytical method has been proposed which depends on the known solution of motion equation of the membrane. This method has been reported to have 0.1 percent accuracy with low calculation time.

Different processes have been proposed for implementing CMUT arrays. They can be generally categorized into two main groups: sacrificial release process and wafer bonding process.

In sacrificial release process, a sacrificial layer is created by depositing or growing procedure. Then the sacrificial layer is selectively removed by an appropriate etchant and a cavity is formed underneath a thin plate [2]. The main drawback of this method is weak control on the thickness, uniformity, and mechanical properties of deposited layers which affect important parameters of the device. The other method of fabricating CMUT, wafer bonding process, has been developed to improve the repeatability issues and process control. The details of different wafer bonding processes can be found in [2]. Figure 1.9 shows the schematic cross section of different CMUT structures.

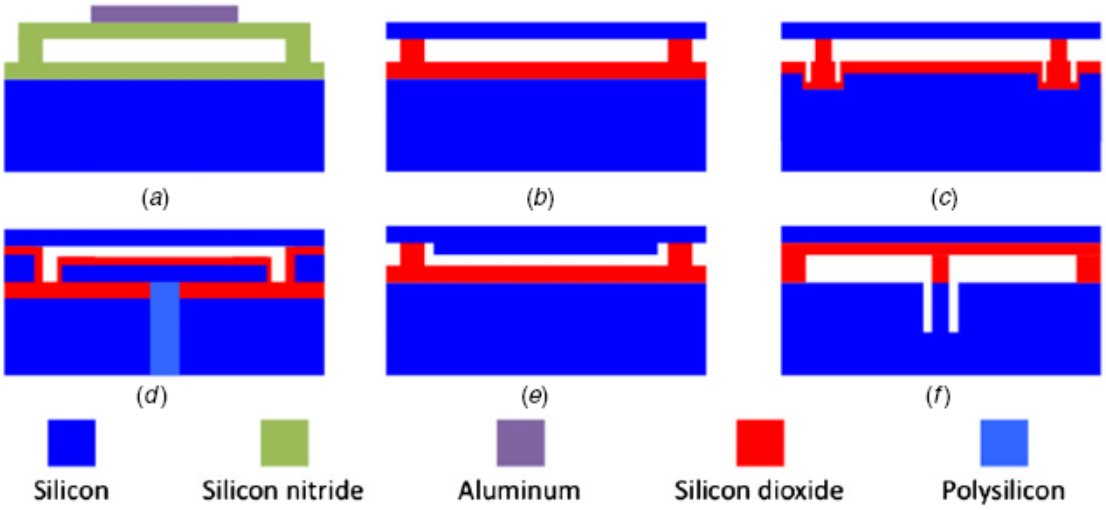


Figure 1.9 Schematic cross-sections for different CMUT structures. (a) CMUT fabricated using the sacrificial release process. (b) CMUT fabricated using the simple wafer bonding process. (c) CMUT fabricated using the LOCOS process. (d) CMUT fabricated using the thick-buried-oxide process. (e) CMUT with added mass on its plate. (f) CMUT with the compliant post structure [2].

CMUT has the capability of being integrated monolithically with the driving circuit, preamplifiers and multiplexers on one chip [30]. This is an advantage especially for transducer arrays with small elements. Small capacitances of these elements in conjunction with large cable capacitance can significantly degrade the signal quality. So the capability of CMUT in being fabricated as close as possible to the electronic circuits can greatly improve the results.

1.3 Interface Electronics for Ultrasound Transducers

Integration of ultrasound transducer arrays with integrated circuits are used in medical applications with a great demand, especially for small elements like in 2D arrays [2]. For CMUT transducers, we need transmitters and receivers for imaging applications and beam-formers for therapeutic applications. In conventional ultrasound systems, CMUT transducers are connected to the main controlling unit using a lot of cables and transmit or beam-former pulsers and receive amplifiers are placed in the main controlling unit. Connection of transducers and processing units using a lot of cables makes the system bulky. Besides, cables show additional capacitances that attenuate the signal quality. Hence, in ultrasound imaging applications receiver electronics need be close to the transducer array. On the other hand, the transmitter and beam-forming circuitry can be integrated with CMUT array to decrease the number of used probes between the system and main controlling unit. There are various methods for integration of CMUTs with front-end electronics. These methods are divided into two main categories: monolithic and multichip (hybrid) approaches [2]. In monolithic integration of CMUT array with electronics, transducers are fabricated on finished electronics wafers but in multichip integration of transducers with circuitry, two different parts (CMUT and IC) are fabricated in different wafers and then they can be bonded directly on top of each other.

They are different approaches that will be briefly explianed in this section, which are followed in the design of the beam-form generator for piezoelectric and capacitive ultrasound transducers in imaging and therapeutic applications. However, the interface electronics for both of imaging and therapeutic applications are composed of similar blocks in the system level. Figure 1.10 shows the generic interface electronics for ultrasound transducers. As can be observed, it includes an ultrasound transducer selection block that generates enable signals with precise delays. This block includes registers, comparators or another kinds of circuits with the ability of generating enable signals in intended times. Enable signals are converted to single pulse with adjustable pulse width or pulse trains with controllable frequencies. The value of the periods and widths of the pulses depend on the operational frequency of designed ultrasound transducers. The magnitude of those pulses can be increased using high voltage circuits in signal magnitude management block. If we want to design interface electronics for ultrasound therapeutic applications, we just need transmitter blocks as the main parts of the beam-forming circuitry. However, interface electronics for ultrasound imaging applications need receiver circuitry to amplify the signals for image formation. Having flexible and fully controllable circuits, low power consumption drivers, low noise amplifiers in receiver part are the main considerations of designing each block.

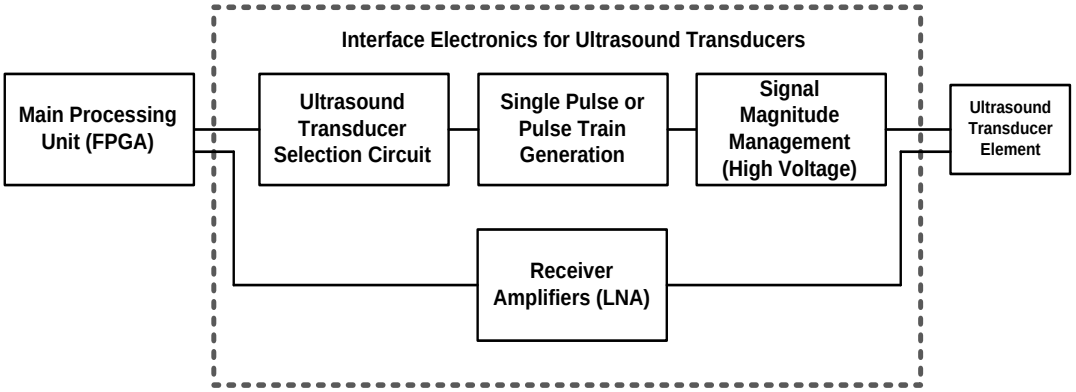


Figure 1.10 The generic interface electronics for ultrasound transducers.

1.3.1 Interface Electronics for Piezoelectric Transducers

Piezoelectric transducers are used in many applications such as detection and visualization of the internal parts of the structures using ultrasonic waves by an echo-graphic procedure [36]. Piezoelectric transducers with their interface electronics are used mainly in medicine and industry. Conventional continuous wave (CW) electronic systems and analysis methods are not adequate for piezoelectric transducers. Hence, most of designed piezoelectric transducers require specific interface electronics for ultrasound applications. Since the electrical excitation and the receiver circuitry are not coupled with the piezoelectric transducers in a suitable mode, the best ultrasonic performance is not obtained in many structures [37], [38].

Driving circuitry of the broadband piezoelectric applications includes high voltage (HV) ramp generators. In imaging applications of piezoelectric transducers, we need transmitter and receiver interface electronics. As can be observed from Figure 1.11, a general diagram of the transmitter circuitry of piezoelectric transducers consists of coupling networks in series and parallel to make the interface electronics [38].

In most of the piezoelectric transducers, the operational frequency varies for 0.5 MHz to 10 MHz. Hence, in high resolution ultrasound detection applications, the rise time of the excitation signals should be adjusted according to operational frequency of the interfaced transducer.

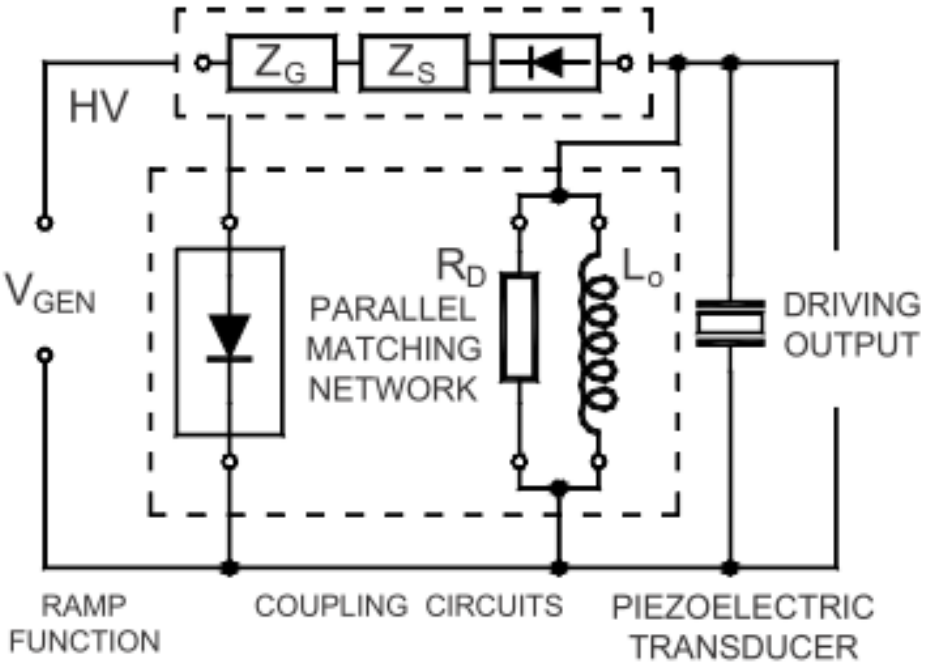


Figure 1.11 Typical schematic of the interface electronics in pulsed piezoelectric transmitters [36].

Because of having attenuation during ultrasound propagation, piezoelectric transducers should be excited using high voltage signals with amplitudes in the range of hundred volts. Figure 1.12 shows a typical high voltage pulse generator that has been used for broadband driving of piezoelectric transducers. This circuit provides high voltage pulses with peak amplitudes of more than 220 volts and rise times between 150 and 250 ns [39]. Hence, this circuit cannot be used for transducers with operational frequencies ranging above 2 MHz. This problem can be solved by using a faster circuit that is shown in Figure 1.13.

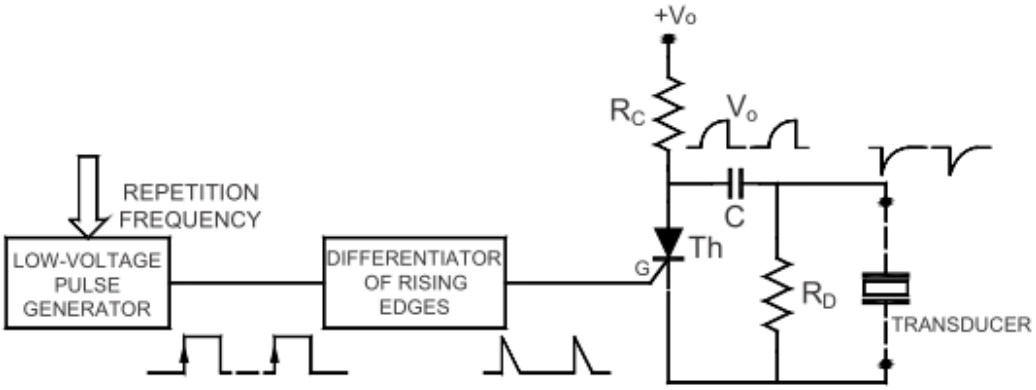


Figure 1.12 Typical schematic of the high voltage pulse generator used for broadband driving of piezoelectric transducers [39].

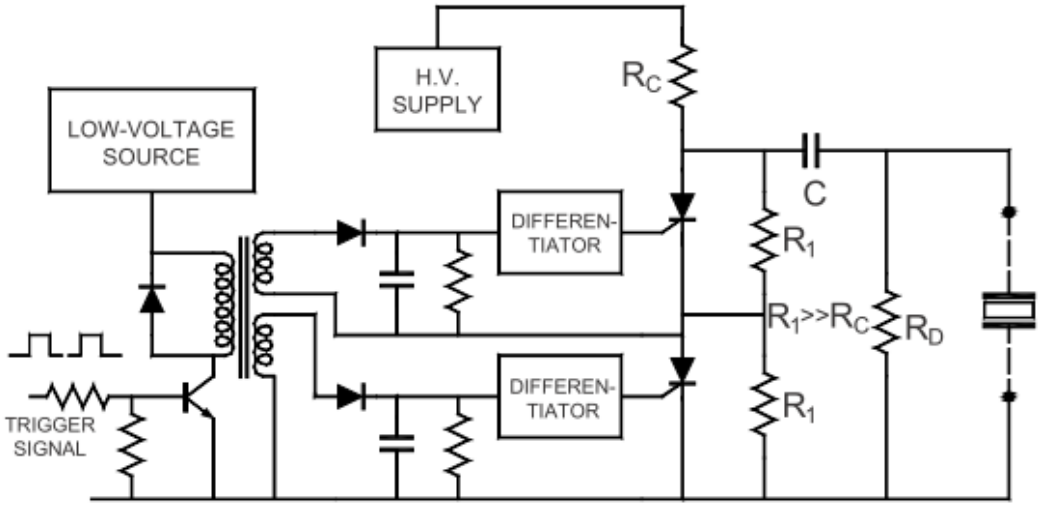


Figure 1.13 Typical schematic of the high voltage pulse generator used for broadband driving of piezoelectric transducers with faster thyristor [39].

Although, the related limitation of the circuit (Figure 1.11) about rise time of the pulses was solved, new drawbacks such as reduction in pulse magnitudes and high power consumption in off mode makes the circuit unsuitable for ultrasound applications. These problems can be overcome by using the power MOSFET transistors [40].

1.3.2 Interface Electronics for Capacitive Micromachined Ultrasonic Transducers (CMUTs)

Most of the related publications in the literature report the design of the front-end electronics for ultrasound imaging applications and do not consider the design of the interface electronics for ultrasound therapeutic applications. Some of the published works just excite the CMUTs using single pulses with adjustable pulse widths. Hence, their works

can just be suitable for black and white imaging applications. As we discussed in previous sections, monolithic and multichip integration methods are the main ways of integrating transducers with electronics [2]. In this section these methods are briefly explained.

Monolithic integration method can be categorized in three major groups: Co-Processing, post-processing by low temperature surface micromachining and post-processing by low temperature direct wafer bonding [2]. Table 1.1 presents three categories of monolithic integration methods with their advantages, constraints and important specifications.

Table 1.1 Comparisons of three categories of monolithic integration methods with their advantages, constraints and important specifications.

Method	Advantages	Constraints	Specifications
Co-Processing	Low-cost	Sharing the area of the transducer element by electronics or interconnects and limitation in vertical direction of the wafer because of having electronics at the same substrate	Fabrication of transducers and electronics using the same process on the same substrate [41]
Post-processing by low temperature surface micromachining (CMUT-in-CMOS) [42]	Fairly simple process	Limitation in vertical direction of the wafer and temperature limitations in CMUTs fabrication	Fabrication of electronics by a foundry process with CMUTs on top of electronics using further process
Post-processing by low temperature direct wafer bonding	Simple process, having control over the plate thickness	----------	Wafer bonding of CMUTs on finished CMOS substrate [43]

Multichip integration method can be classified in two major groups: chip-to-chip bonding method and bonding on intermediate substrates [2]. Table 1.2 presents three categories of multichip integration methods with their advantages, constraints and important specifications.

Table 1.2 Comparisons of two categories of multichip integration methods with their advantages, constraints and important specifications.

Method	Advantages	Constraints	Specifications
Chip-to-chip bonding	Optimized fabrication process	The die area of the chip must be larger than the CMUT's	Direct bonding of CMUT arrays on electronics using flip-chip bonding pads [44]
Bonding on intermediate substrates	Independent CMUT and electronics dice Designing of large array with several CMUT elements [45] Small electronics can be used	----------	Connection of CMUTs and electronics using an intermediate substrate

As shown in Figure 1.14, a large single 2D CMUT array is demonstrated with 32×32 configuration on one side of the interposer and four custom 16×16 application specific integrated circuits (ASICs) bonded on the other side. In this structure, the interposer makes the required connections between the CMUT elements and the integrated circuits.

Figure 1.15 shows eight ICs that are bonded to a 64 CMUT elements ring array using flip-chip bonding pads. As can be observed, an eight flex circuits are folded and the interface of a CMUT array with 3 mm^2 silicon area and an integrated circuits with 8 mm^2 area is accomplished [46].

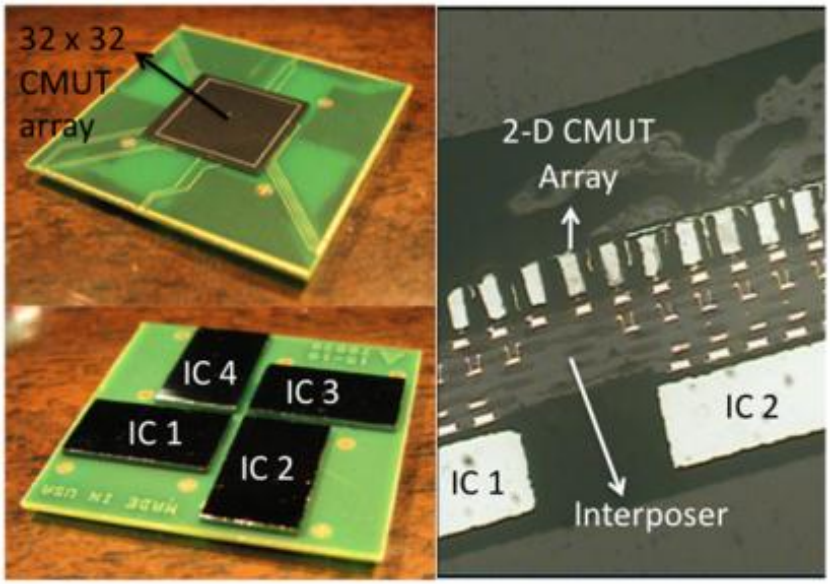


Figure 1.14 Left side top: a flip–chip bonded 32×32 2D CMUT array to top side of an interposer. Left side bottom: four flip–chip bonded chips to bottom side of the interposer. Right side: the cross sectional view of the multichip integration [2].

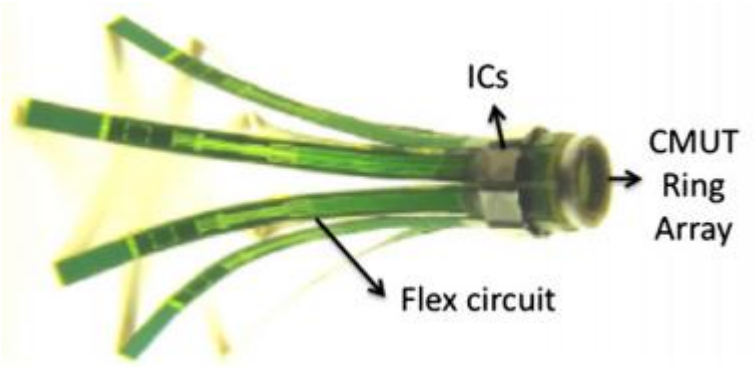


Figure 1.15 Eight ICs that are bonded to a 64 CMUT elements ring array using flip-chip bonding pads [2].

1.4 Objectives of the Thesis

The aim of this research is to design and implement flexible and fully controllable beam-former interface electronics of CMUT transducers for ultrasound therapeutic applications. Designed electronics can also be used as transmitter part of interface electronics for ultrasound real-time 3D imaging applications. An extensive list of objectives of this research is as following:

1. Study and characterization of the required building blocks for the design of flexible and fully controllable beam-former interface electronics of CMUT transducers for ultrasound therapeutic applications.
2. Design of a CMUT selection circuit for generating precise and programmable delays. 3D beam-forms are generated by exciting of ultrasound transducers in different times according to their distances from the focal point. Hence, depending on the coordinate of the focal point, the interface electronics of each transducer gets different delay information.
3. Design of a one-shot circuit to adjust the widths of the single pulses for different operating frequencies of CMUTs. Designed one-shot circuit should control the widths of the pulses in a large range of nanoseconds to support different kinds of transducers.
4. Design of a precise pulse train generator with controllable frequency in the range of 1 to 10 MHz. The frequency of the output signal should be controlled digitally using an FPGA. Besides, proposed circuit should be designed low sensitive to temperature and supply variations.
5. Design of a high voltage pulser circuit with THKOX module. High voltage (HV) pulsers are provided with adjusted single pulses or pulse trains. These circuits are supposed to increase the amplitudes of low voltage (LV) pulses up to 45 volts.
6. Design of a high voltage pulser circuit with HVTHKOX module. There are many DMOS transistors in HVTHKOX module that can be useful in designing of high voltage circuits. However, XFAB MPW run does not support that module in HV 0.35 µm CMOS technology.
7. Design of an ultrasound therapeutic IC for 4X4 and 16X16 CMUT arrays in HV 0.35 µm CMOS process as a complete design to interface with CMUTs including a highly flexible and controllable high voltage single pulse and pulse train generators.

1.5 Outline of the Thesis

The rest of this thesis is divided into six chapters, beginning from Chapter 2 explaining the detailed theory and analysis of all the required building blocks of the beam-form generator for designing of highly flexible and fully controllable beam-former interface electronics of CMUT transducers for ultrasound therapeutic applications. The state-of-the-art designs and a brief literature review for each block of the circuitry is discussed in this chapter.

Chapter 3 explains the schematic, design and simulation results of the ultrasound therapeutic interface electronics for 4X4 CMUT arrays which are implemented in a HV (high voltage) 0.35 µm CMOS technology. The main parts of the ASIC are delay management circuits, adjustable single pulse and pulse train generators and high voltage pulsers (up to 45 V) that are designed to be integrated with capacitive micromachined ultrasonic transducers (CMUTs). The design considerations and optimization techniques are also presented in details.

Chapter 4 presents the layout of the designed interface electronics for 4X4 CMUT arrays. Since these kinds of chips are known with remarkable silicon areas, there are some technical considerations that should be taken into account in final designs.

Chapter 5 introduces the schematic, design, layout and simulation results of the ultrasound therapeutic interface electronics for 16X16 CMUT arrays which are implemented in a HV (high voltage) 0.35 µm CMOS technology. The driver part (LV) of the IC is identical with the previous one that is explained in Chapter 3 but this chip is designed for large number of elements. Moreover, designed high voltage pulsers of this IC can increase the amplitudes of the generated pulses up to 100 volts by employing DMOS transistors with HVTHKOX module instead of THKOX. A programmable pule train generator with a different method is also described. At the end of this chapter, the layout of the proposed IC with its technical considerations is given.

Chapter 6 introduces two different MATLAB programs for providing delay information of CMUT elements. The first program has been proposed for 16X16 CMUT array while the second one was designed for 4X4 CMUT arrays. The major purpose of these programs is calculating delay times for generating different beam-forms using ultrasound elements. Moreover, the second program generates the proposed digital input information that should be given to the IC by an FPGA.

Chapter 7 ends this thesis work by summarizing the results and successes during this research and showing the possible future works under the thesis subject.

CHAPTER 2

INTERFACE ELECTRONICS FOR CAPACITIVE MICROMACHINED ULTRASONIC TRANSDUCERS (CMUTs)

The aim of the ultrasound medical system is to generate beam-forms by exciting ultrasound transducers. Therefore, the interface electronics is required to be integrated with ultrasound transducers to generate 3D beam-forms by firing them in different time according to their distances from the focal point. Most of the previous studies have used the integration of transducers with interface electronics for real time 3D medical imaging applications. However, there are potentially high losses associated with designing of interface electronics for ultrasound transducers in ultrasound therapeutic applications. The importance of the ultrasound technology has recently increased as a therapeutic tool. Since high intensity focused ultrasound (HIFU) generate a accurate ablation pattern deep in tissue without having effect on the surrounding structures, they can be used instead of radio-frequency (RF) or other types of ablations [2]. Recently, most of the HIFU systems employ transducers based on piezoelectric materials such as PZT-8 and PZT-4 with spherical shell and focused operating in the range of 1 to 4 MHz [1]. Since precise beam-formation is required in ultrasound medical applications and phased array structures have improved control features, most recently phased array applications were provided for high intensity focused ultrasound (HIFU) systems. The ultrasound energy fires the focused target area inside the body by passing harmlessly through the tissues. Hence, the delivery of high acoustic energy to the focused target area can be accomplished using large arrays which can be designed and fabricated using CMUTs. A significant advantage of using CMUTs over other ultrasound transducers, e.g. piezoelectric micromachined transducers (PMUTs), is the ability of using large arrays without having self-heating effects. Hence, CMUTs are completely suitable for HIFU continuous wave (CW) applications [47], [48].

In this chapter, the operation principle, analysis, and literature review of all required building blocks that are needed for the beam-form generator of an ultrasound-based therapeutic application are described. The important design considerations which are considered for the ultrasound-based therapeutic applications are also discussed. Section 2.1 presents the overview of the required blocks that are explained in this chapter by introducing the operation of each block and describing how it relates to other blocks in the final system. Section 2.2 explains the methods of selecting CMUTs for exciting them according to their distances from the focal point. The generation of beam-forms is done using an external ultrasound system or on-chip delay generators. Section 2.3 describes the operation of

variable pulse width generators which are used for adjusting the widths of firing pulses according to the operating frequencies of ultrasound transducers. Section 2.4 explains the operation of a pulse train generator by providing an example. Section 2.5 describes different types of high voltage pulsers and the specific design requirements for on-chip and low power consumption interface electronics. Finally, section 2.6 summarizes this chapter by providing a short review of the next chapter.

2.1 System Level Overview

Figure 2.1 shows the system level overview of typical interface electronics for ultrasound transducers including main building blocks.

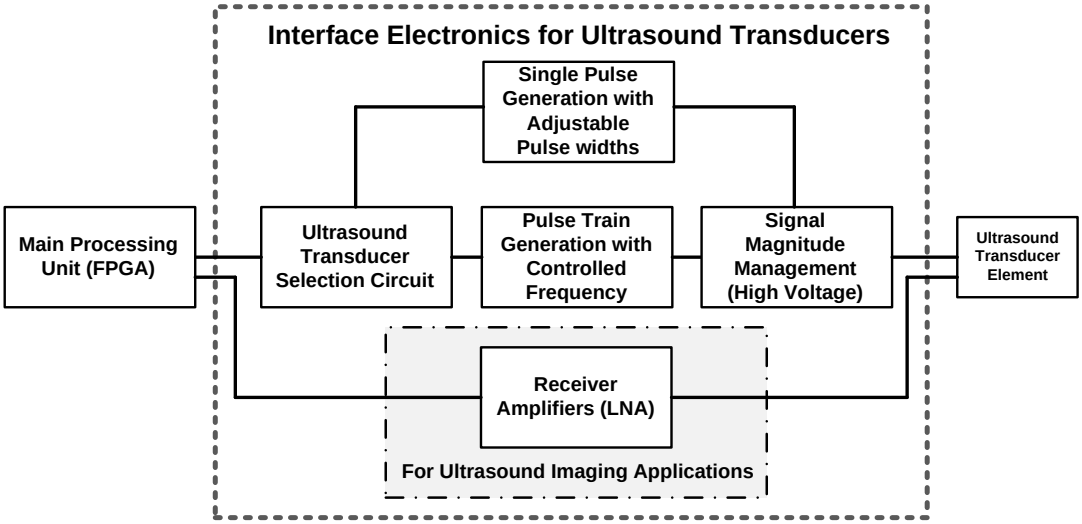


Figure 2.1 System level overview of the interface electronics for both of ultrasound imaging and therapeutic applications.

The selection circuit is the first main block in an ultrasound imaging and therapeutic system that is considered for generating delay information for selection of ultrasound transducers. The interface electronics can transmit single pulses or pulse trains of arbitrarily steered and focused ultrasound only if a suitable method of triggering the pulsers is selected. Since transducers have different distances from a focal point (firing point), they need to be fired using pulses in different times. Hence, sent ultrasound waves are arrived at the same time and phase to the focal point. Single pulse or pulse train circuitry is provided by a narrow enable signal to activate the circuits of next stages for pulse generation. Depending on ultrasound applications, transducers are excited with single pulses or pulse trains. In single pulse mode, the pulse width of the signal according to the operating frequency of the CMUT element can be adjusted by external current source or in-chip digital to analog converters (DACs). For some applications, we need to drive the transducers by pulse trains with a specific frequency. The value of the frequency depends on the operating frequency of the transducer element. The final block is the high voltage circuits which increase the

amplitudes of the pulses generated with previous blocks. Ultrasound transducers are provided with high voltage signals because of having attenuation in ultrasound propagation and focusing beams with high energy at focal points. In ultrasound imaging applications, the transducer provides a mechanical response to the electrical excitation in transmission process. In receiver mode, the reflected echoes subsequently cause mechanical displacement of the ultrasound transducer elements which generate an electrical signal which is used to ultrasound image formation using receiver circuitry. Generated electrical signals by transducers are amplified using low noise amplifiers (LNAs). Since in ultrasound therapeutic applications, the generation of beam-forms is required, there is no need for receiver part in interface electronics for those applications. At final stage, designed interface electronics is connected to the transducer elements. Different types of integration of electronics and transducer array were discussed in Chapter 1. Among explained methods, chip-to-chip bonding can be useful for our therapeutic application.

Figure 2.2 shows the diagram of a probe with a 2D CMUT array integrated with the front-end electronics for therapeutic applications. As can be observed, the topology of a beam-forming probe for therapeutic applications consists of a 2D CMUT array in top and front-end electronics in bottom side of the structure. The delay pattern of ultrasound transducers at which each element is supposed to be fired is determined by designed beam-forming electronics. Designed integrated circuit drives the 2D CMUT array using flip-chip bonding pads. Using this technique, the delay information of CMUT elements can be provided without using many cables and making the system bulky. In final step designed interface electronics is supposed to be launched using a FPGA.

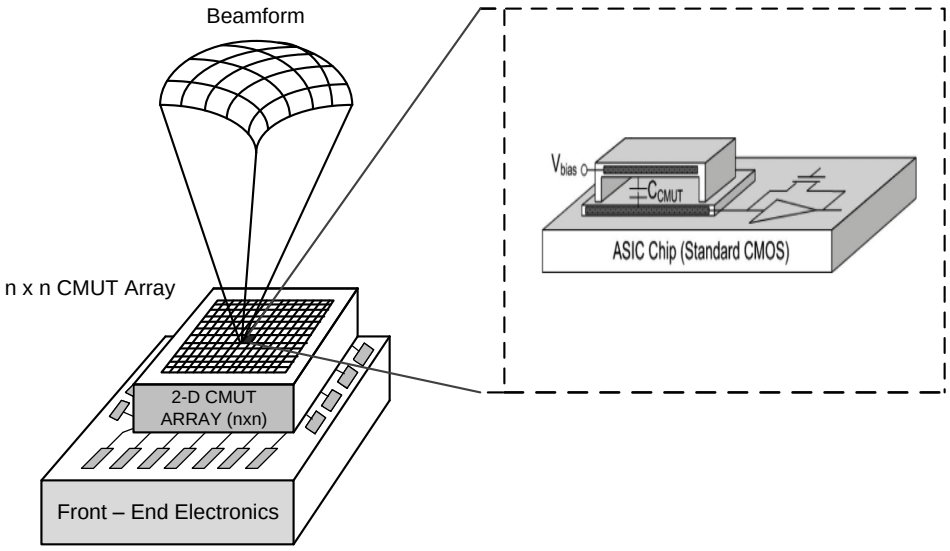


Figure 2.2 Diagram of a therapeutic probe with a 2D CMUT array integrated with the front-end electronics for therapeutic applications [49], [50].

2.2 CMUT Delay Information

High end ultrasound systems are provided with hundreds of high voltage pulses. These high voltage signals are connected to transducer elements (PMUTs or CMUTs). As shown in Figure 2.3, a typical ultrasound system with multiplexers in the probe handle part of the structure provides the enable signals for last (high voltage) stages. As can be observed, the widths of the pulses for different operating frequency of transducers are controlled using ultrasound system.

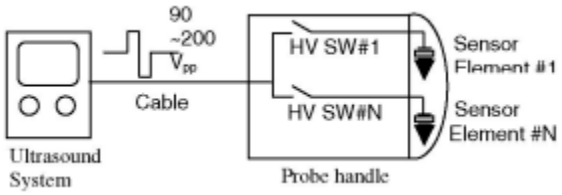


Figure 2.3 A typical ultrasound system with multiplexers in the probe handle [51].

Figure 2.4 shows the sixteen elements of switches that are connected to a 16-bit shift register. The shift register (SIPO) gets the input delay information serially in 5 MHz and deliver them to high voltage switches (HVSW) in parallel mode. For designing of high voltage switches, DMOS (double diffusion MOSFET) transistors can be used [52] which can sustain high values of voltages on their gate-source junctions and much more values on drain-source.

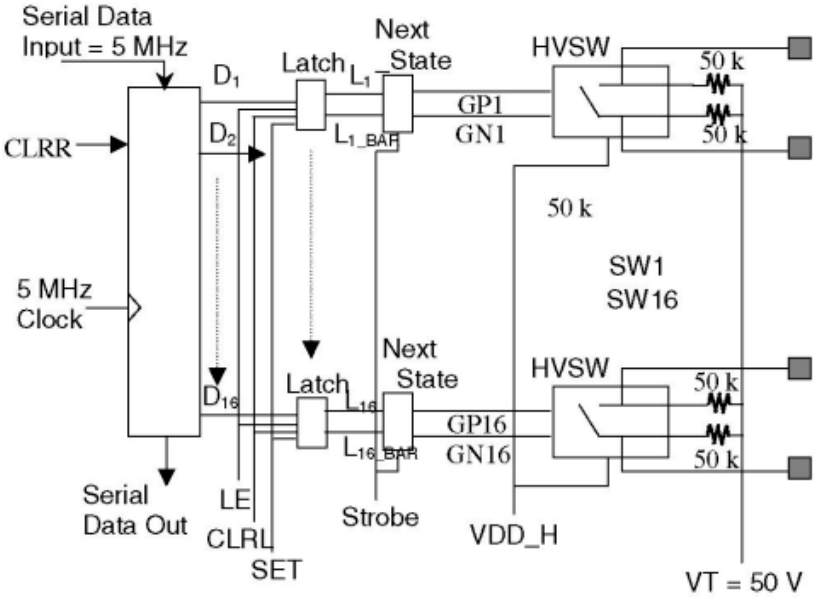


Figure 2.4 The architecture of a high voltage switch array with 16 channels [51].

The previous method may still be acceptable for some ultrasound medical applications where the widths of the pulses are controlled externally (off-chip) and there is no need for exciting the transducers by trains of pulses; however this circuit still needs much more modifications for selection of a transducer and adjusting the specification of the pulses. Another scheme which is proposed in this study is to use the combined SIPO (serial input parallel output) blocks with comparators as the main transducer selection circuit. This is described in more detail in section 3.3.

2.3 Variable Pulse Width

The width of the output single pulses or pulse trains must be optimized according to attached ultrasound transducer elements. The beam-former circuitry can be used with multiple transducers only if the provided signals by the IC are controllable. The widths of the single pulses are adjusted to match the operating frequency of the transducer. Typically, a one-shot circuit (a circuit that provides a single pulse when triggered) controls the width of the pulses by controlling the current of a capacitor. The value of the capacitance and the control current determine the width of the pulses. Figure 2.5 shows a typical one-shot circuit which can be used for ultrasound imaging and therapeutic applications. Since only the upper threshold in the hysteresis loop of this circuit is needed for ultrasound application, the circuit comprises a half Schmitt trigger [53].

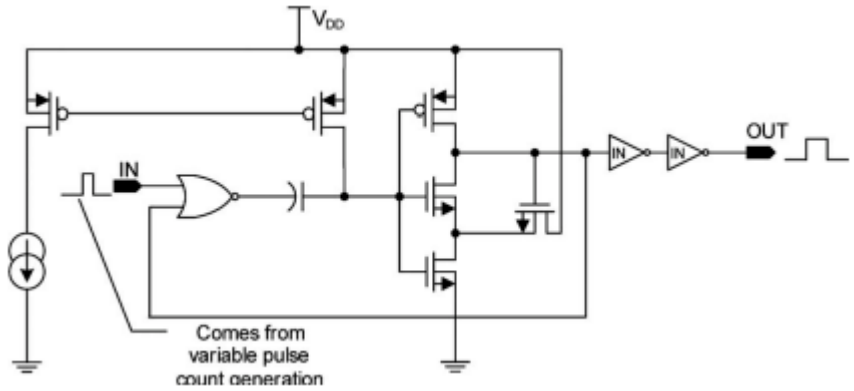


Figure 2.5 A typical one-shot circuit for ultrasound imaging and therapeutic applications [53].

As discussed, the widths of the pulses are adjusted using a capacitor and a current source. The value of the capacitor is fixed according to the application and the one-shot circuit is only controlled by the current flowing through the capacitor. Controlling current can be adjusted using in-chip (e.g. DAC) or off-chip (e.g. an external current source) devices. Figure 2.6 shows a programmable current source for providing the controlling current of the one-shot circuit. This circuit consists of an 8-bit digital to analog converter (8-bit DAC), a voltage to current (V-I) converter, and current mirrors. The 8-bit DAC circuit converts the digital input vector to a constant voltage by dividing the V_{REF} (reference voltage) into 256

(2^8) equal values. An op-amp takes the output voltage of the DAC and through a voltage to current converter (V-I) circuit, the current is mirrored for distribution. The capacitor C and the resistor R2 make a low pass filter while the R1 is employed for controlling the current of I_{OUT} (output current).

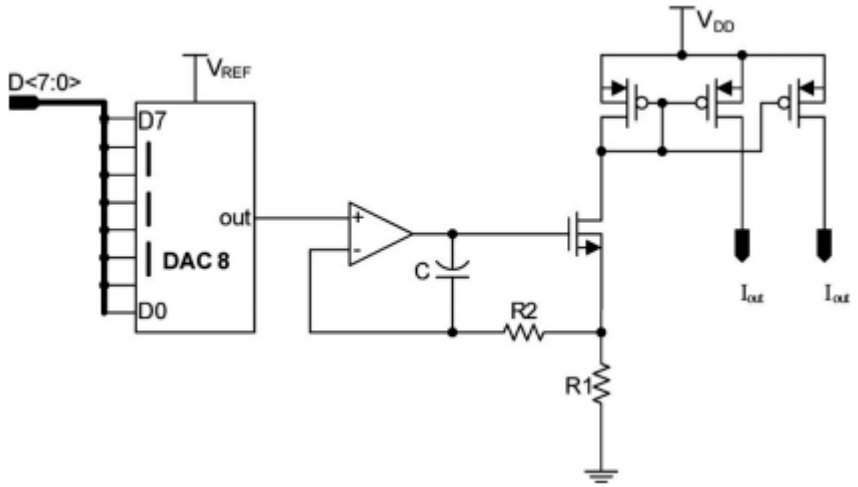


Figure 2.6 A programmable current source for providing the controlling current of the one-shot circuit [53].

Although, the combination of the shown circuits of Figures 2.7 and 2.8 facilitate the controlling of the one-shot circuit externally by digital input vector, the circuit still has some limitations. If the input pulse width at the one-shot circuit is smaller than the required output pulse width, then the output pulse of the circuit is limited to the input pulse width. This problem can be solved by connecting the one-shot circuit to a typical variable pulse width circuit (Figure 2.7). The output pulse width will depend only on the one-shot circuit width and without depending on the input pulse width of the pulse count generator, if a feedback loop with a NAND gate is used. Another port of the NAND gate must be kept permanently high. Designed one-shot circuit for the input pulse widths of 25 ns, gives 100 ns with a control current of 70 µA and 15 ns with a control current of 500 µA. It is obvious that, the one-shot circuit provides small pulse width by consuming large powers. A different one-shot circuit has been proposed in this research and will be described in next chapter. As will be shown, our proposed one-shot circuit adjusts the pulse widths in the range of 15 to 650 ns (large range of widths) with a control current of about 70 to 80 µA (small power consumption).

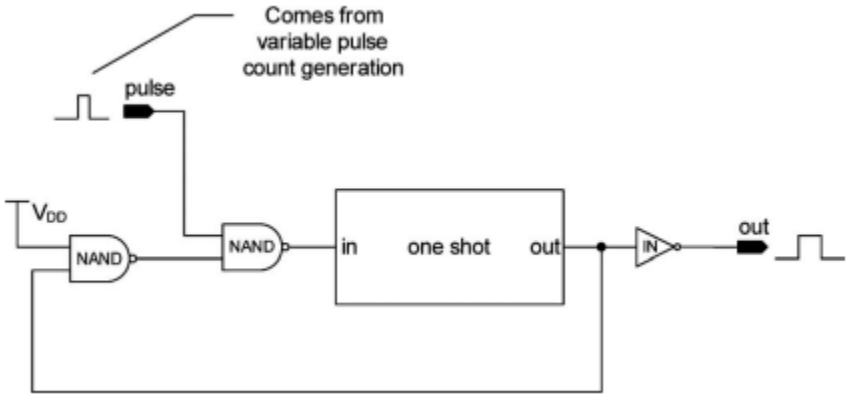


Figure 2.7 A typical variable pulse width circuit for improving the one-shot circuit [53].

2.4 Programmable Pulse Train Generator

Conventional and ordinary ultrasound imaging and therapeutic systems need a single pulse for excitation of the transducers but for new therapeutic or color Doppler imaging applications, a train of pulses can be useful. Figure 2.8 shows a programmable pulse train generator circuit which provides a set of pulses from 1 to 64. The selected serial output information from the delay generator circuit is fed to a 1:64 demultiplexer (DEMUX). Then, the selected delay information is routed to the output of the demultiplexer according to the value of the 6-bit pulse count. The 6-bit pulse count adjusts the number of the pulses at the output of the programmable pulse train, ranging from 1 to 64. The outputs of the demultiplexer are fed to a PISO (parallel in serial out) shift register which is controlled by a clock frequency (Y clock). As can be observed from Figure 2.8, explained pulse train generator circuit can give bursts of up to only 64 pulses. Besides, combination of some pulse trains with different frequencies can be very difficult in shown circuit. A different programmable pulse train generator circuit has been proposed in this research and will be discussed in next chapter. In our proposed circuit, a digitally controlled oscillator (DCO) is combined with three 5-bit digitally controlled delay element (DCDE) that provides the fully controllable pulse trains for ultrasound transducers.

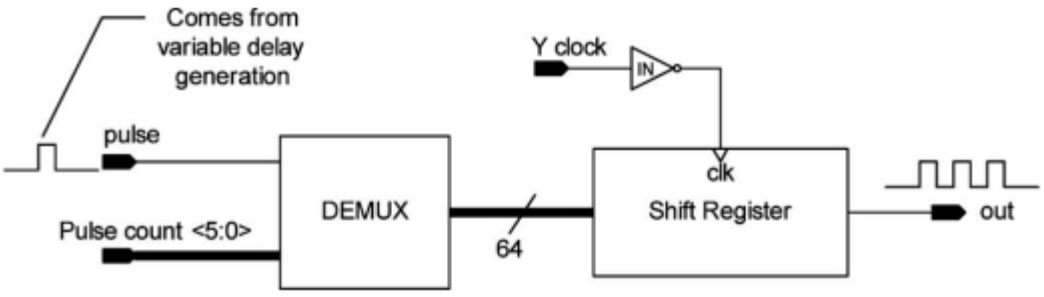


Figure 2.8 A programmable pulse train generator circuit [53].

2.5 High Voltage Pulser Circuits

The importance of the high voltage circuits in deep submicron process by implying low supply voltages has recently increased. In conventional interface circuitry for ultrasound applications, the high voltage circuits are provided outside of the chip (off-chip). However, as the multichip and monolithic integration methods are advanced, many new techniques of providing high voltage electronics inside of the chip (on-chip) have been presented. To produce high voltage pulses BCD (Bipolar/CMOS/DMOS) is a suitable technology [54]. The fabrication of high voltage devices in BCD technologies is very expensive and complex. Hence, the layout of the regular high voltage devices from a LV process should be modified by carefully considering the underlying breakdown mechanisms in MOS transistors to get low cost and high voltage elements [55-57]. Moreover, since the high voltage circuits are optimized for maximum speed, minimum occupied silicon area and minimum power consumption, the power supply of the circuit should be decreased but, in the case of using high voltage circuits the requirements of the system cannot be achieved. Deep submicron technologies enable high voltage techniques by solving this problem.

2.5.1 Conventional High Voltage (HV) Level Shifters

Most of the related publications in the literature, report the design of the high voltage (HV) level shifting circuits, but in this section we focus on those that don't require high voltage capacitors without having static supply current. The conventional and other designed level shifter circuits [58-60] require the input logic LV supply (V_{DDL}) and the HV supply (V_{DDH}) as two different voltage supplies. Figure 2.9 shows a very simple pulser element which has been designed and simulated using high voltage transistors. These kinds of transistors can bear large voltages (e.g. 18 V for HV 0.35 µm CMOS process) on their gate-source junctions and very larger voltages (e.g. 90 V for HV 0.35 µm CMOS process) on their drain-source junctions. As can be observed, by applying a low voltage (3.3 V) signals to the gate of the transistor, high voltage pulsers can be obtained on its drain.

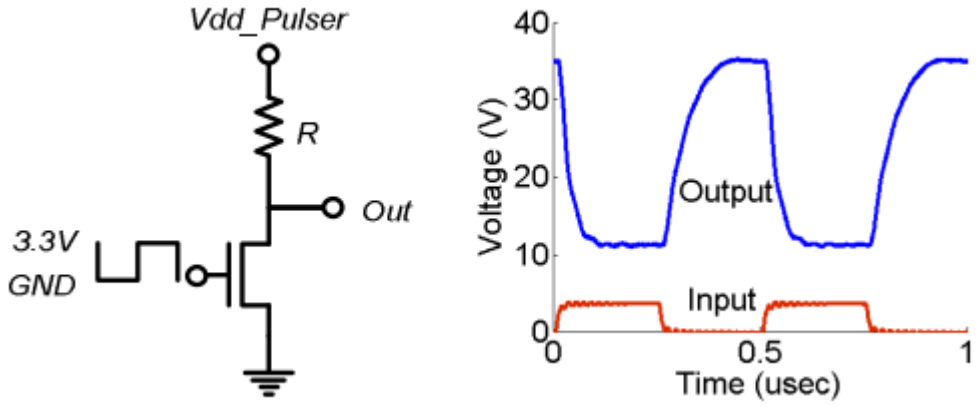


Figure 2.9 A high voltage pulser element (left side) and the simulation results of the circuit (right side) [61].

According to Figure 2.10, one high voltage driver circuit including two HV NMOS and PMOS transistors can be added to output of the circuit which is shown in Figure 2.9. New pulser circuit consists of a push-pull stage including two high voltage MOS transistors. The resistive load controls the voltage across the gate-source junction of the high voltage PMOS transistor. The rise time of the inverter circuit should be decreased because it increases the turn-off time of the pull-up PMOS transistor. Furthermore, using a larger drive transistor for having a reasonable output rise time increases the capacitance at the output of the circuit.

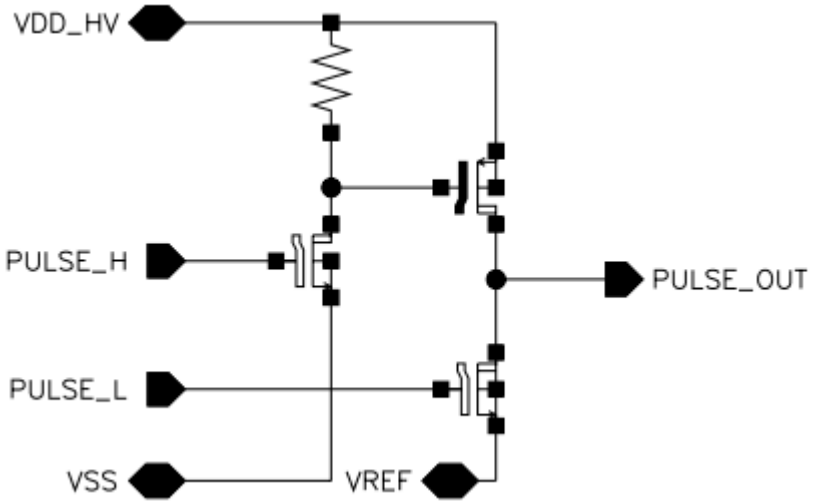


Figure 2.10 A pulser circuit with a push-pull stage including two high voltage MOS transistors [62].

Figure 2.11 shows a classic version of the well-known low voltage level shifter circuit. When IN is at V_{SS}, the transistor M_1 turns off and M_2 turns on. Consequently, the V_D increases to V_{DDH} and the output of the inverter I_2 (OUT) will be at V_{SS}. Transistor M_3 pulls up its drain to V_{DDH} and turn off the M_4 transistor. Conversely, when the IN port is at V_{DDL}, the transistor M_1 turns on and M_2 turns off. Transistor M_1 pulls down the V_D and the output of the inverter I_2 (OUT) will be at V_{DDH}.

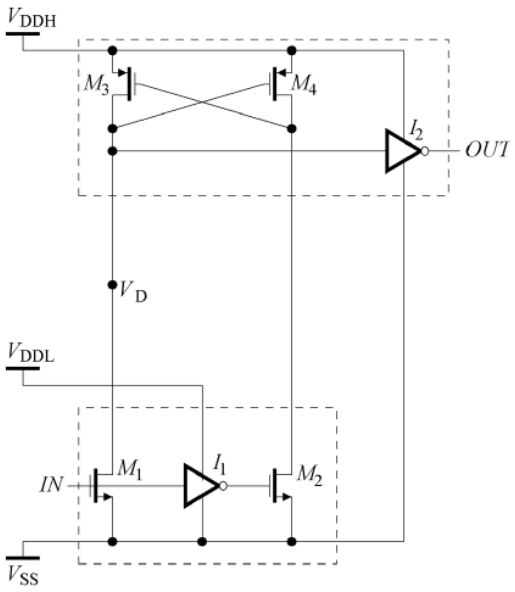


Figure 2.11 A classic version of the well-known low voltage level shifter circuit [63].

If M_1 is in active region and M_3 is in linear triode region (assuming similar threshold voltages for the N and P channel transistors and V_{DDL} is less than V_{DDH}), the currents through M_1 and M_3 can be given by:

$$I_{d-M1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 \left[V_{DDL} - V_{TH1}\right]^2 \tag{2.1}$$

$$I_{d-M3} = \mu_P C_{ox}\left(\frac{W}{L}\right)_3 \left[V_{DDH} - \left|V_{TH3}\right|\right] \times \left|V_{TH3}\right| \tag{2.2}$$

Since the same current flows through M_1 and M_3 transistors, the equations of 2.1 and 2.2 can be equated to get the following design equation:

$$\frac{(\frac{W}{L})_1}{(\frac{W}{L})_3} = 2\frac{\mu_P C_{ox}}{\mu_n C_{ox}} \times \frac{\left[V_{DDH} - \left|V_{TH3}\right|\right] \times \left|V_{TH3}\right|}{\left[V_{DDL} - V_{TH1}\right]^2} \tag{2.3}$$

Figure 2.12 shows a high voltage level shifter circuit using DMOS cascode transistors, which is an improved version of the classic level shifter circuit (Figure 2.11). For protection of the low voltage pull down transistors, M_1 and M_2 with connected gates to V_{DDL} have been used as NDMOS cascode transistors. Similarly, for protection of the floating low voltage circuitry, M_3 and M_4 with connected gates to V_{SSH} have been used as PDMOS transistors.

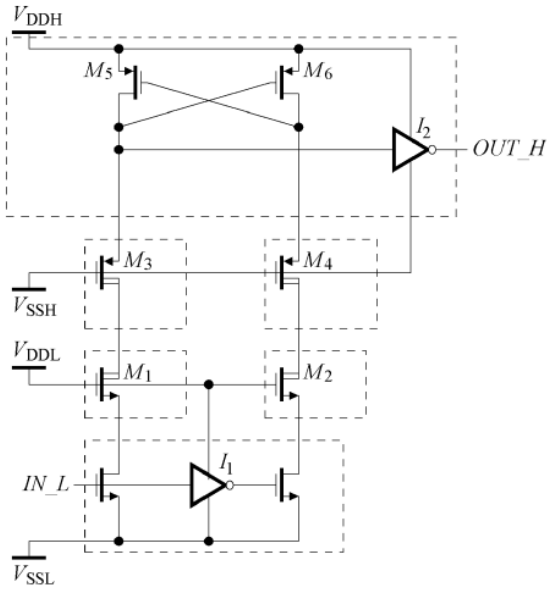


Figure 2.12 A high voltage level shifter circuit using DMOS cascode transistors [63].

2.5.2 Modified High Voltage (HV) Level Shifters

Figure 2.13 shows a modified version of the high voltage level shifter circuit with DMOS cascode transistors. In this circuit, the NDMOS transistors are used directly as pull down transistors for reducing the occupied area in the chip. M_7 and M_8 transistors are added to new circuit to avoid the sources of the PDMOS transistors from pulling down more than a diode drop voltage below V_{SSH}. Although pull up resistors can be used instead of M_7 or M_8 transistors, they dissipate static power [64]. The transistor sizing of modified version is quite different. If M_1 is in active region (on), V_D is pulled down and V_S follows the V_D because M_3 is on too. When V_S decreases, the gate drive of M_3 is reduced and makes the pull-down weaker. Hence, the ratio of M_3 to M_5 is important in design procedure. The transistors of M_2, M_4 and M_6 are sized to have a symmetrical circuit. In LV case, M_5 is in the linear triode region and its current can be given by:

$$I_{d-M5} = \mu_p C_{ox}\left(\frac{W}{L}\right)_5 \left[V_{DDH} - V_{SSH} - \left|V_{TH5}\right|\right] \left|V_{TH5}\right| \tag{2.4}$$

The M_3 can be forced to active region, if $V_D < V_{SSH}$ which can be obtained by the minimum size of M_1. The current through M_3 is given by:

$$I_{d-M3} = \frac{1}{2}\mu_{p-DMOS}\ C_{ox}\left(\frac{W}{L}\right)_3 \left[V_{DD} - \left|V_{THp}\right| - \left|V_{THp-DMOS}\right|\right]^2 \tag{2.5}$$

Since the same current flows through M_5 and M_3 transistors, the equations of 2.4 and 2.5 can be equated to get the following design equation:

$$\frac{(\frac{W}{L})_3}{(\frac{W}{L})_5} = 2\frac{\mu_P C_{ox}}{\mu_{p-DMOS} C_{ox}} \times \frac{\left[V_{DD} - \left|V_{THp}\right|\right] \times \left|V_{THp}\right|}{\left[V_{DD} - \left|V_{THp}\right| - \left|V_{THp-DMOS}\right|\right]^2} \tag{2.6}$$

The M_1 to M_5 ratio can be provided as the following design equation:

$$\frac{(\frac{W}{L})_1}{(\frac{W}{L})_5} = 2\frac{\mu_P C_{ox}}{\mu_{n-DMOS} C_{ox}} \times \frac{\left[V_{DD} - \left|V_{THp}\right|\right] \times \left|V_{THp}\right|}{\left[V_{DDL} - V_{TH-DMOS}\right]^2} \tag{2.7}$$

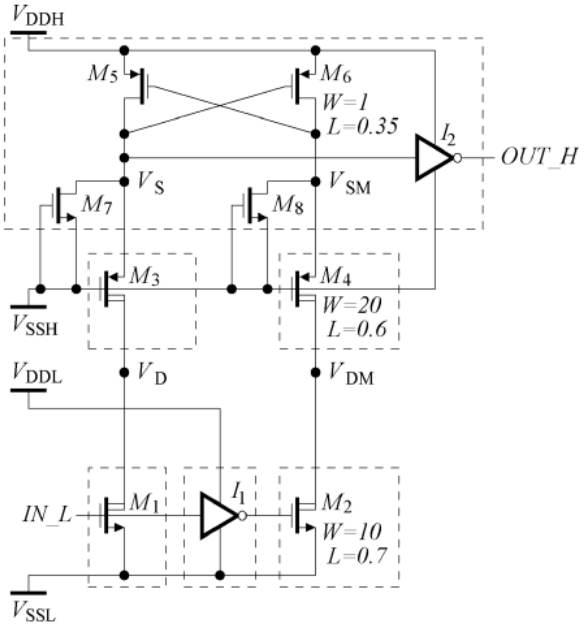


Figure 2.13 A modified high voltage level shifter circuit using DMOS cascode transistors [63].

As can be observed, a traditional HV driver circuit includes a complementary output stage with independent control of high voltage NMOS pull down and high voltage PMOS pull up transistors. The high voltage pull down transistor is controlled by low voltage logics while the gate of the high voltage pull up transistor must be less than $V_{HV} - V_{TH}$ for appropriate operation. The efficiency of the pre-driver (level shifter) circuits is very important especially if they are supposed to be used in portable devices. An improved high voltage circuit with voltage mirror structure [65] for controlling the gate voltage of the PMOS driver transistor has been shown in Figure 2.14. In this case, the gate of the high voltage PMOS transistor is

controlled by a low voltage supply. The gate voltage of the PMOS transistor will never swing larger than the VDD_LV because the same current flows through the flip-flop stage.

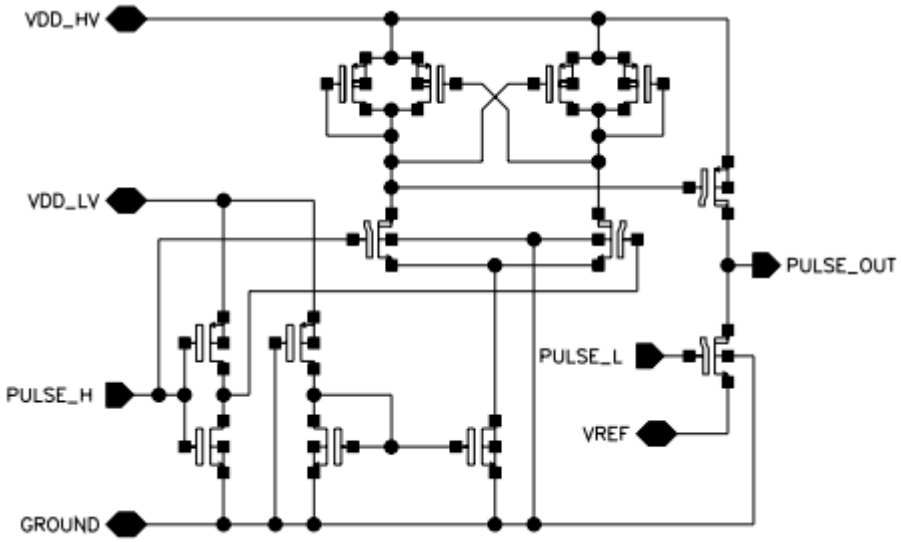


Figure 2.14 An improved high voltage circuit with voltage mirror structure for controlling the gate voltage of the PMOS driver transistor [62].

Figure 2.15 shows the schematic of a conventional cross-coupled level shifter. The nodes of V_{DN6} and V_{DN7} can be driven to V_{PP} using M_2 and M_3 pull up transistors. On the other hand, M_1 and M_4 transistors are used to limit the voltage across the V_{DN6} or V_{DN7} to avoid exceeding gate-oxide breakdown voltage when M_6 or M_7 are on. The major drawback of the Pseudo-NMOS level shifter is its continuous power consumption in both of the cases that the output is high or low.

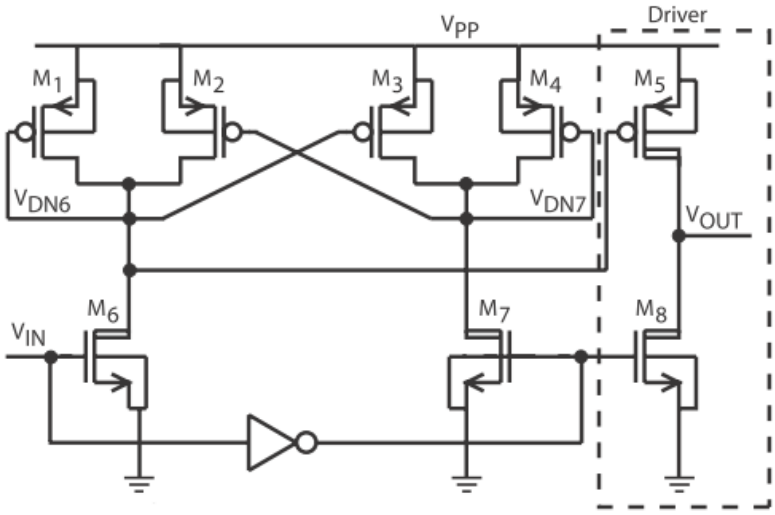


Figure 2.15 The schematic of the Pseudo-NMOS level shifter [65], [66].

Figure 2.16 shows an improved version of the Pseudo-NMOS level-shifter circuit (Figure 2.15). In this circuit power consumption has been reduced dramatically by adding the low voltage (LV) current mirror transistors M_{10} to M_{12}, and the load transistor M_9. The transistors M_6 and M_7 are replaced with the floating versions, because in the layout of the circuit, their source pins are connected to the bulk which is permanently ground. Since the current is reduced, the propagation delay increases. Moreover, the die area of the circuit is significantly increases because of having larger LDMOS floating transistors.

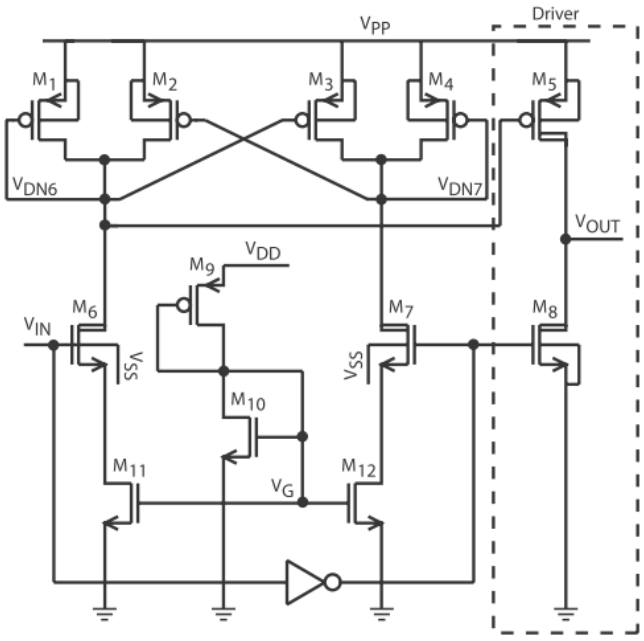


Figure 2.16 The schematic of the Pseudo-NMOS level shifter with current limit [67].

So far, we explained that the typical Pseudo-NMOS level shifter circuit has a great power consumption which is not suitable for portable applications while the modified version of this circuit improves the power consumption very well but it has still some disadvantages such as large propagation delay and die area. The power consumption of described level shifters can be reduced even further by using a three transistors (3T) resistive load full static level shifter circuit (figure 2.17). In conventional level shifters, for controlling the gate-source voltage of the pull up PMOS transistor in driver stage of the circuit, a PMOS load is used rather than a resistive load. Hence, a near threshold drop voltage at the gate of the pull up PMOS transistor is generated when M_1 is off and as a consequence, the output of the circuit, with a slightly different threshold voltage, is not pulled down to an ideal zero voltage. The gate-source voltage of the M_2 transistor should be minimized to ensure that the transistor remains off. The similar current limit concept introduced in Figure 2.16, can be used to drop the gate voltage of the pull up PMOS transistor during output high. The three transistors (3T) resistive load level shifter circuit decreases the power consumption once again but with having an increased propagation delay.

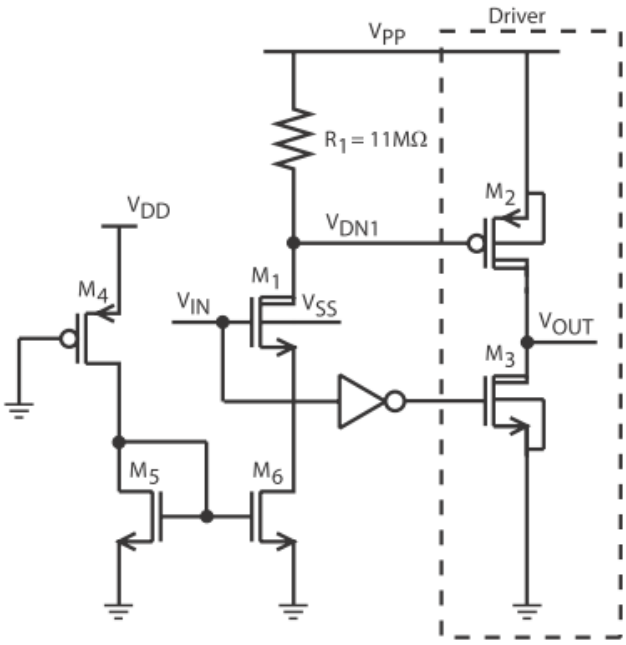


Figure 2.17 The schematic of the three transistors (3T) resistive load level shifter circuit [67].

2.5.3 Single Supply High Voltage (HV) Level Shifter

In conventional level shifters the number of supplies increases and makes the circuits complex and expensive. This problem can be overcome by using the single supply level shifter circuits. These kinds of circuits use only one supply connection without adding any extra supply pin. Besides, the signals of the single supply level shifter circuits can be

interfaced with other I/O interface simultaneously without requiring any extra supply pin [68]. Figure 2.18 shows the schematic of a single supply level shifter circuit. By decreasing the supply voltage of the inverter including p2/n2 and adding a diode connected n1 NMOS transistor, the level shifter circuit can be designed. The supply voltage of the inverter p2/n2 (v) is $V_{DDH} - V_{TH}$ which turns off the transistor p2 when is in high by reducing its gate-source voltage. Conversely, if p2 is in low, p4 turns on and increases the node v to V_{DDH}. Therefore, the transistor p3 is turned completely off and the voltage at node v swings between V_{DDH} and $V_{DDH} - V_{TH}$ depending on the state of the input voltage. If V_{DDH} is higher than the input supply by more than V_{TH}, the power consumption of the circuit is significantly increased due to leakage current. Besides, the diode connected transistor n1 increases the propagation delay of the circuit.

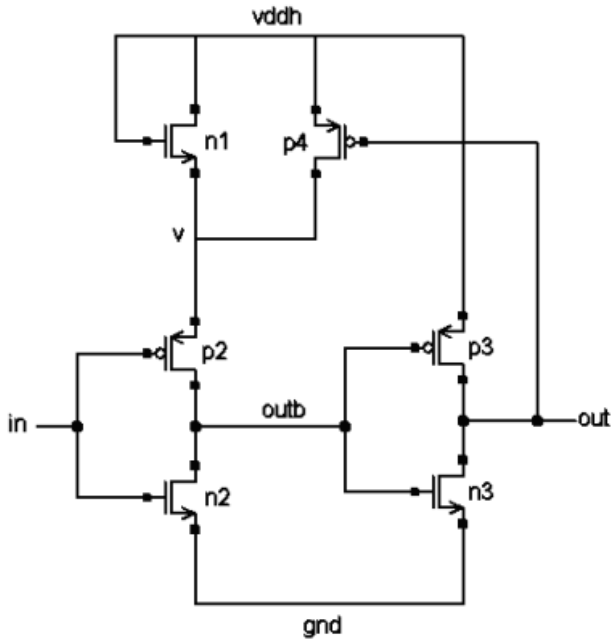


Figure 2.18 The schematic of a single supply level shifter circuit [69].

The single supply level shifter circuit which is shown in Figure 2.18 has also some limitations. If V_{DDH} is higher than the input supply by more than V_{TH}, the power consumption of the circuit due to leakage current is significantly increased. Besides, the diode connected transistor n1 increases the propagation delay of the circuit. An improved and modified version of the single supply level shifter circuit has been proposed (Figure 2.19) to prevent the circuit from having leakage current [68]. If the input (in) is at high state (vdd), the transistor m6 turns on and pulls down the output (outb) to vssa. Then, m5 turns off and m2 turns on and charges the ctrl node to vdd. If the vdda is larger than the vdd, m1 remains off and then the out will be at vdda. In reverse mode, if the input (in) is at low state (vssa), the node ctrl remains at vdd initially and turns on the transistor m1. The transistor m1 should be stronger than m2 to prevent the node ctrl from discharging before out. The transistors m1 and m4 increase the voltage of the node outb to vdda while the node out discharges towards vssa. As the value of the node outb increases above threshold voltage of

the transistor m5, it turns on and reduces node out to vssa. Therefore, the output of the circuit is at vssa when the input is at the same state of vssa.

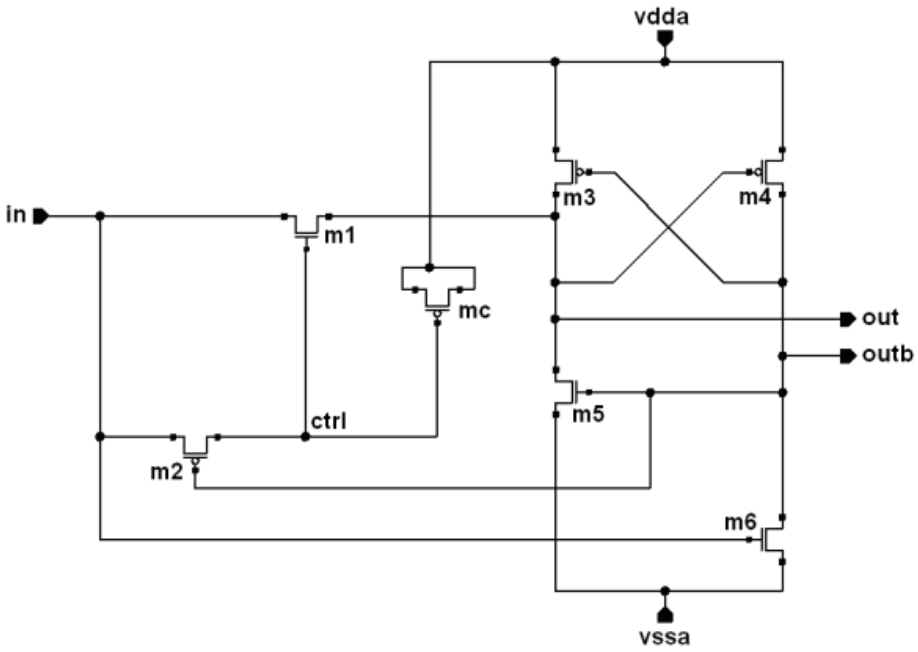


Figure 2.19 The schematic of the improved and modified version of a single supply level shifter circuit [68].

2.6 Summary of the Chapter

This chapter discussed a complete overview on the required building blocks for a typical ultrasound beam-form generator. The theory, design and the state-of-the-art designs for each of the required block is discussed. Also, an explanation on design consideration for high flexible and controllable beam-form generation is given. Next chapter presents the schematic, design and simulation results of the proposed ultrasound therapeutic IC for 4X4 CMUT array in HV (high voltage) 0.35 µm CMOS technology.

CHAPTER 3

THE ULTRASOUND THERAPEUTIC IC FOR 4×4 CMUT ARRAY IN HV 0.35 µm CMOS TECHNOLOGY

In this chapter, the theory, design and simulation results of different blocks (LV and HV) of the IC for 4×4 CMUT array are explained, which have been designed in HV (high voltage) 0.35 µm CMOS technology that is a widely available process. Some of the previously reported blocks of the IC including low voltage and high voltage have also been simulated and their results are compared with the designed and proposed architectures.

Different building blocks that is required for different typical interface circuitry of ultrasound transducers was discussed in previous chapter. Designed beam-forming circuitry includes low voltage and high voltage circuits. Driver part of the circuit (low voltage) includes 8-bit shift register, 8-bit comparator, one-shot circuit, digitally controlled oscillator with 5-bit digitally controlled delay line and frequency down conversion. These blocks provide single pulses with adjustable pulse widths or pulse trains with arbitrary frequencies for final stage of the circuit which is high voltage pulsers. One complete block including low voltage and high voltage electronics is needed for each CMUT. Hence, the number of blocks and subsequently the size of the chip completely depend on the number of used CMUT elements in considered array. In this chapter, section 3.1 explains the typical overview of the IC by presenting the important blocks (LV and HV). Section 3.2 explains the architecture of the proposed integrated circuit by presenting some detail about different blocks of the chip. Section 3.3 describes CMUT selection method for generating enable signals by giving the schematic, design and simulation results of the proposed circuits. Section 3.4 introduces the design and simulation results of the proposed single pulse generation circuit with the ability of controlling pulse widths of the output signals for different operating frequencies of CMUTs. Section 3.5 gives the schematic, design and simulation results of the proposed pulse train generation circuit with the ability of adjusting the frequencies of the output signals for different operating frequencies of CMUTs. Pulse trains can be used in different applications such as color Doppler imaging and CMUT therapeutic applications. Section 3.6 explains the frequency down conversion circuit by providing the schematic, design and simulation results of the proposed circuit. Section 3.7 describes the high voltage circuit by providing the schematic, design, simulation results and important specifications of the proposed circuit. Section 3.8 presents the method of providing DC biasing of a CMUT element. Section 3.9, explains the constraints and challenges of a HV 0.35 µm CMOS technology and states the potential improvements that

can be expected once moving to an advanced process for small size and low power application. Finally, section 3.10 summarizes this chapter.

3.1 The Overview of the Ultrasound Therapeutic IC for 4×4 CMUT Array

The proposed ultrasound therapeutic IC consists of different types of blocks which are placed on the same chip. For each CMUT element, one complete block including all of the designed circuits is considered, hence the final size of the chip is completely depends on the numbers of the CMUT elements. Figure 3.1 shows the view of the top level of the ASIC design in which different blocks have been designed and implemented. In the rest sections of this chapter, the design methods and simulation results of each circuit have been discussed in details.

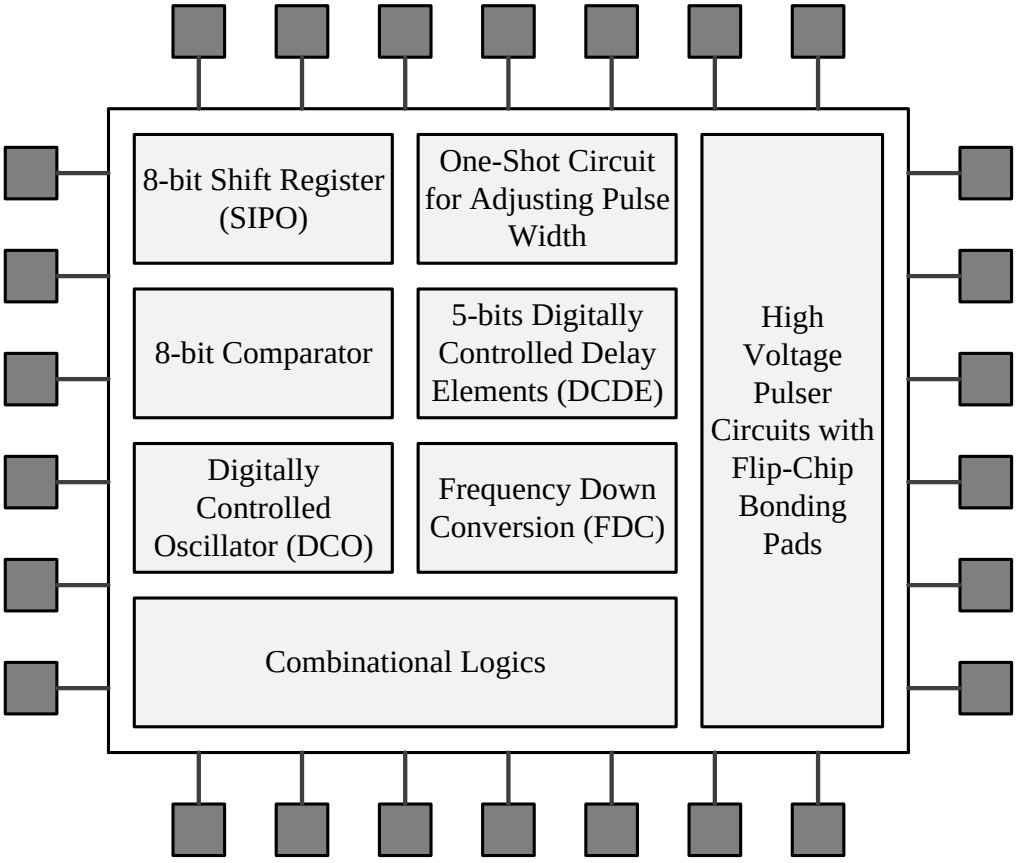


Figure 3.1 The overview of the ultrasound therapeutic IC for 4×4 CMUT array in HV 0.35 µm CMOS technology.

3.2 System Architecture

In this section, the architecture of the complete ASIC design is explained. The main purpose of this section is to make a better view about the proposed designs. The block diagram of the designed integrated circuit is shown in Figure 3.2. The IC uses a 4×4 CMUT element

transducer array for therapeutic applications. The IC consists of 16 element transmit beam-formers for 16 ultrasound transducers. The firing system provides each of 16 CMUT elements with an 8-bit shift register (SIPO), an 8-bit comparator, a one-shot circuit, a digitally controlled oscillator with 5-bit digitally controlled delay elements, a frequency down conversion circuit, 45 V pulser circuit with thick oxide transistors (THKOX) and combinational logics (Figure 3.2). The output of the high voltage blocks are supposed to be connected to CMUT elements one by one using flip-chip bonding pads. Any time that we want to fire an arbitrary point, we should load focusing delay values into the shift registers serially using a field programmable gate array (FPGA). At the same time FPGA controls the selection lines of beam-forming blocks globally.

As we stated before, the IC interfaces 16 of the array elements for beam-forming. As shown in Figure 3.3, the beam-forming circuit includes three main blocks. The first main block which consists of an 8-bit shift register and an 8-bit comparator is considered for generating delay information for selection of CMUTs. If we want to fire the CMUT elements by single pulses, we should activate the first line which includes a one-shot circuit. The pulse width of the signal according to the operating frequency of the CMUT element can be adjusted by external current source or on-chip digital to analog converters (DAC).

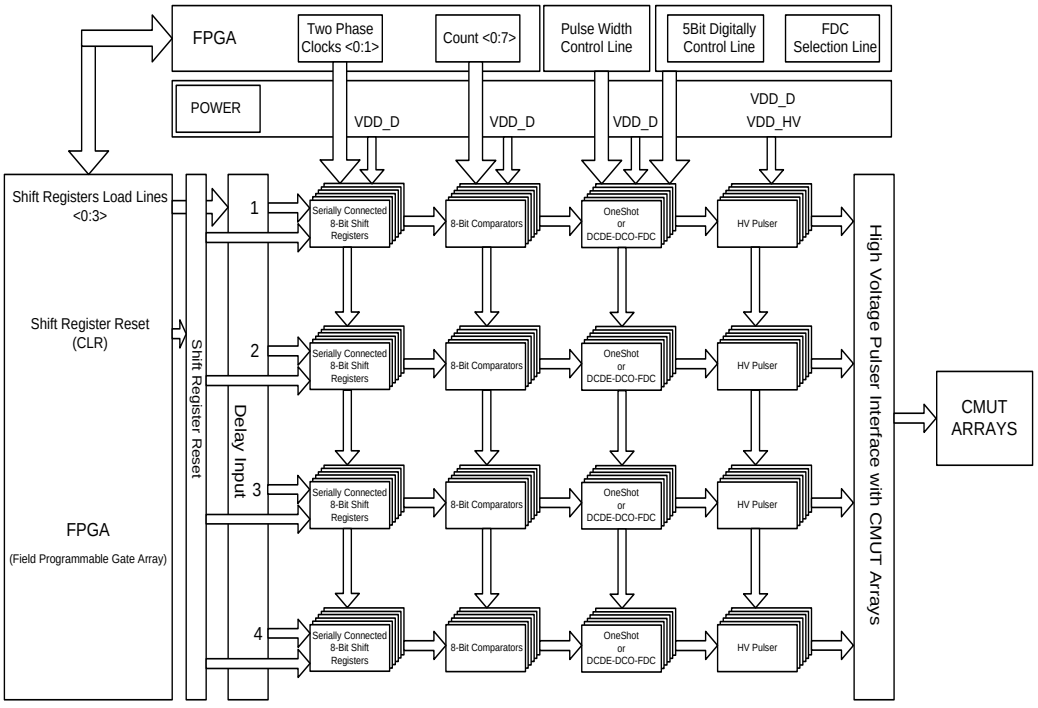


Figure 3.2 Block diagram of the complete ASIC design for ultrasound therapeutic applications.

In some of the cases we want to fire the CMUT elements by pulse trains instead of single pulses. These kinds of signals can be useful in color Doppler imaging applications too [53].

Also our designed beam-former has been considered for therapeutic applications but it can be used as a transmission part of 3D color Doppler imaging applications too. For our application we need pulse trains with adjustable frequencies in the range of 1 to 10 MHz and hence we decided to use digitally controlled oscillator with digitally controlled delay lines and frequency down conversion blocks.

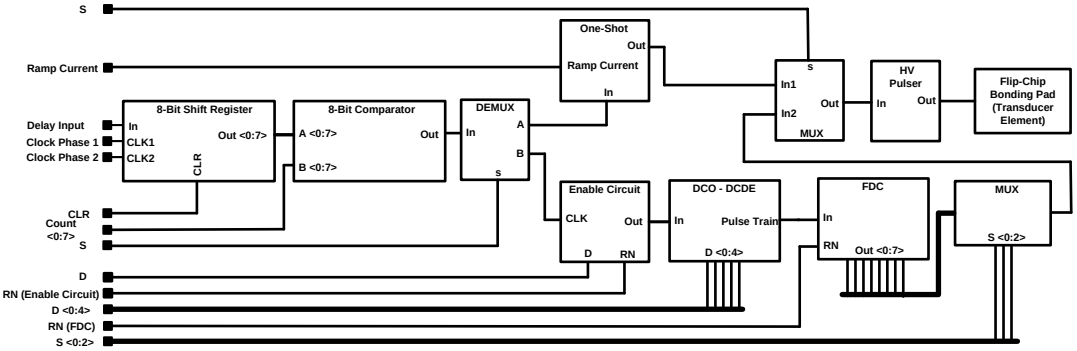


Figure 3.3 Beam-former block diagram for one CMUT element.

Finally, the magnitude of generated low voltage signals, either single pulse or pulse trains are increased up to 45 V. In fact the magnitude of the high voltage signals can be controlled via external lines.

3.3 CMUT Selection Method

In previous section, the complete structure and the main blocks of the IC have been discussed. The IC gets the delay information from a FPGA and generates high voltage single pulses with adjustable pulse widths or high voltage pulse trains with arbitrary frequencies. In this section, CMUT selection method for stimulation of an intended ultrasound transducer using high voltage pulses has been described. For selection of a CMUT element we need a shift register and a comparator. Before generating each new firing beam-form, the FPGA loads 8-bit focusing delay values serially, into every shift register from their D ports in separated lines of the IC. Since there are four CMUT elements in one row, four shift registers have been placed one after another in series mode. Figure 3.4 shows one-bit dynamic shift register which has two input clocks, one data input and one reset line. There are two transmission gates (T-Gate) in each one-bit shift register to store the transmit delay information.

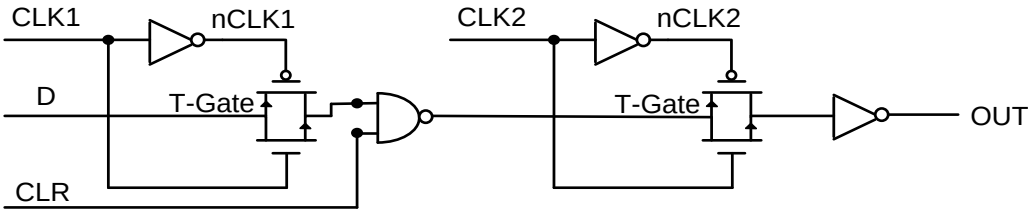


Figure 3.4 One-bit dynamic shift register.

As shown in Figure 3.5, a CMOS transmission gate register can be constructed by parallel combination of NMOS and PMOS transistors, with complementary gate signals. The major advantage of the CMOS transmission gate in comparison with NMOS transmission gate is to allow the input signal to be transmitted to the output without the threshold voltage attenuation. Since the transmission gate has no direct connection to either the power rail or the ground rail, it is different to the inverter and NAND gates except for the substrate. The PMOS gate is connected to nCLK and the NMOS gate is connected to CLK to provide the clock signals of the shift register. Table 3.1 summarizes the final (W/L) values of transistors of the designed transmission gate (T-Gate) register.

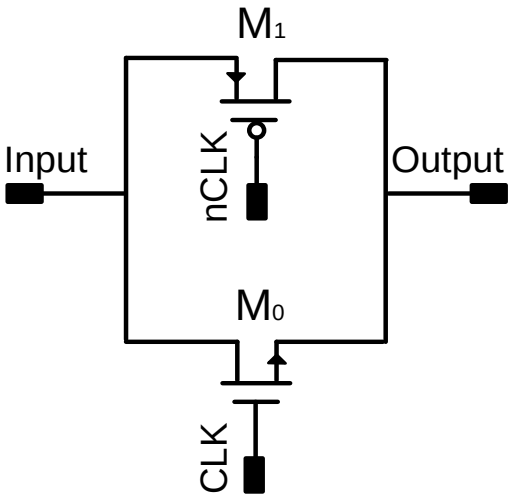


Figure 3.5 Transmission gate (T-Gate) register.

Table 3.1 (W/L) values of the transistors for designed transmission gate (T-Gate) register.

Transistor name	Type	W (μm)	L (μm)
M_0	NMOS	10	0.35
M_1	PMOS	10	0.35

By connecting eight numbers of one-bit dynamic shift registers, one 8-bit shift register can be achieved. As shown in Figure 3.6, for connecting each bit of the shift register to the corresponding bit of the comparator as our next block, a serial to parallel (SIPO) 8-bit shift register has been used.

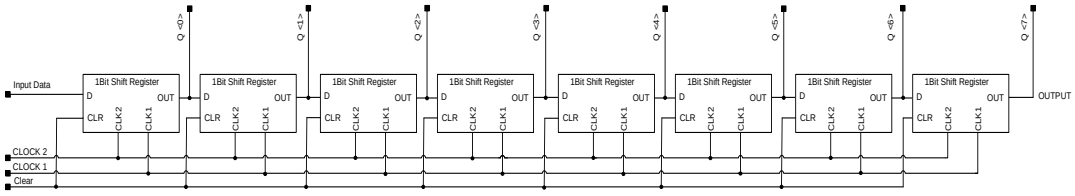


Figure 3.6 8-bit serial to parallel (SIPO) dynamic shift register.

Figure 3.7 shows 8-bit serial to parallel (SIPO) dynamic shift register which has one port of D for getting the delay information from the FPGA, one clear port (CLR) for resetting the shift register, two pins for input clocks which get the clocks in reverse mode from FPGA and eight output pins for delivering the data to 8-bit comparator.

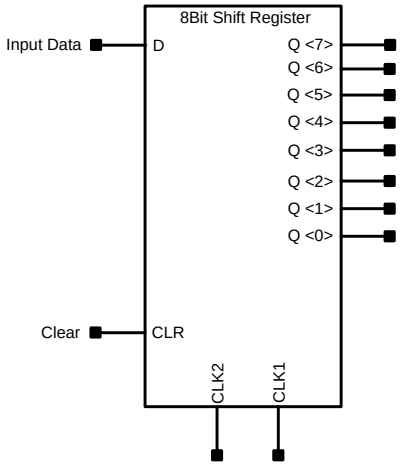


Figure 3.7 8-bit serial to parallel (SIPO) dynamic shift register block.

As we mentioned before, four input signals from the FPGA load the four rows of shift registers in parallel mode. The FPGA is supposed to generate a two-phase clock, delay information for beam-forming, the information about the count rate of the global counter and the input signals for the IC's shift registers. The shift registers have been designed for a load rate greater than 100 MHz. The shift registers have been tested for 100 MHz and 200 MHz clock frequencies. Figures 3.8 and 3.9 show the simulation results of the dynamic 8-bit shift register, when the delay information is 10101111 and the clock frequencies are 100 MHz and 200 MHz, respectively.

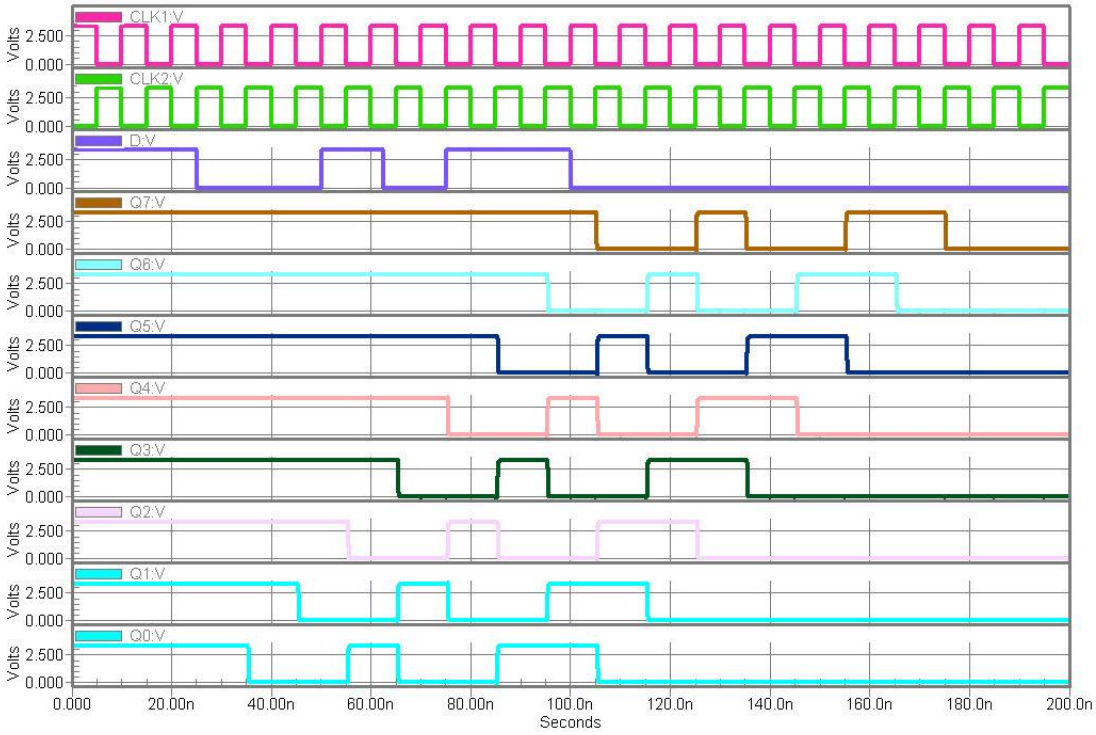


Figure 3.8 Simulation results for 11001011 input code at 100 MHz clock frequency.

According to Figure 3.8, the total delay time for one 8-bit shift register in 100 MHz clock frequency is 80 ns hence at this clock frequency, the load time for all 16 shift registers is 0.32 µs which is negligible in comparison with the time of pule echo.

According to Figure 3.9, the total delay time for one 8-bit shift register in 200 MHz clock frequency is 40 ns hence at this clock frequency, the load time for all 16 shift registers is 0.16 µs which is completely negligible in comparison with the time of pule echo. Table 3.2 summarizes the load time for all of four lines according to their clock frequencies.

Table 3.2 Delay times in different clock frequencies.

8-bit shift register	F_{clock} (MHz)	T_{clock} (ns)	Load time for all 16 shift registers (µs)
Case 1	100	10	0.32
Case 2	200	5	0.16

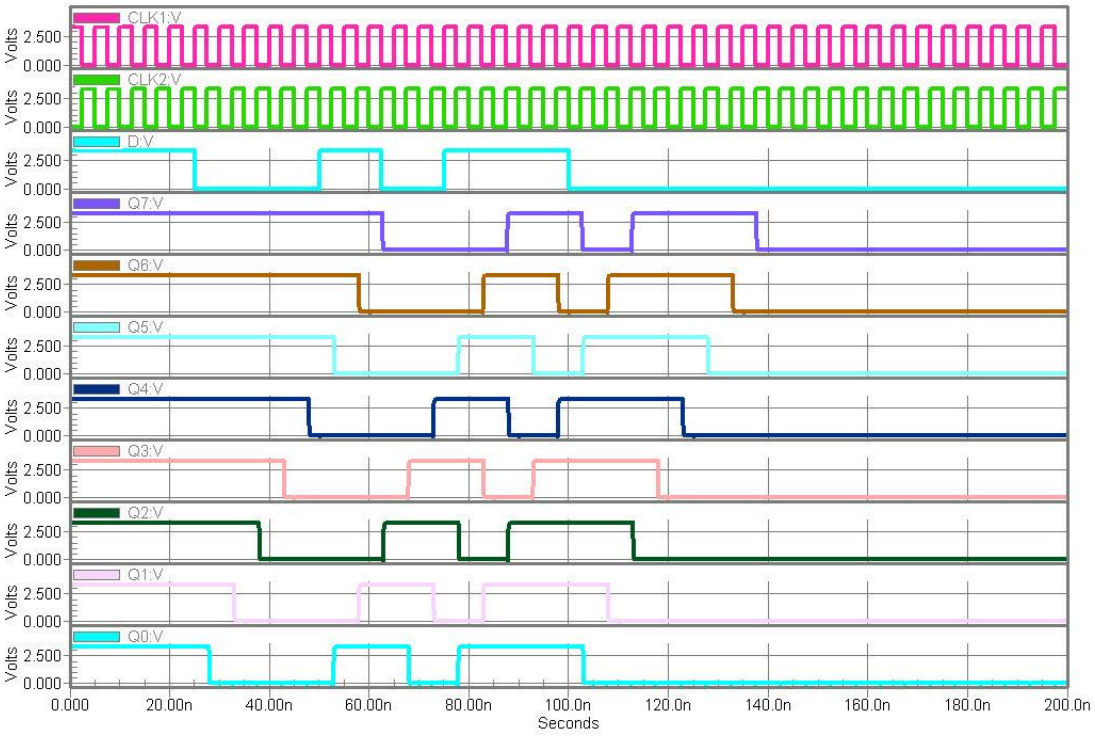


Figure 3.9 Simulation results for 11001011 input code at 200 MHz clock frequency.

When all of the 8-bit shift registers get the delay information from the FPGA, they deliver the data to the 8-bit comparators in parallel mode. 8-bit comparators are supposed to compare the data of their input ports and if they are identical, they send the enable signal to the next stage. Figure 3.10 shows the schematic of 4-bit pseudo NMOS comparator [70]. Although in these kinds of comparators the gate draws the dc current, but they are fast and get small area in chip. Providing a full swing output voltage cannot be obtained easily hence we need to add a buffer at the output side of the circuit. According to Figure 3.10, the comparator gets the data from A and B ports separately and if these ports are identical bit by bit, the drain of the PMOS transistor goes high (3.3 V). Table 3.3 summarizes the final (W/L) values of transistors of the designed 8-bit comparator.

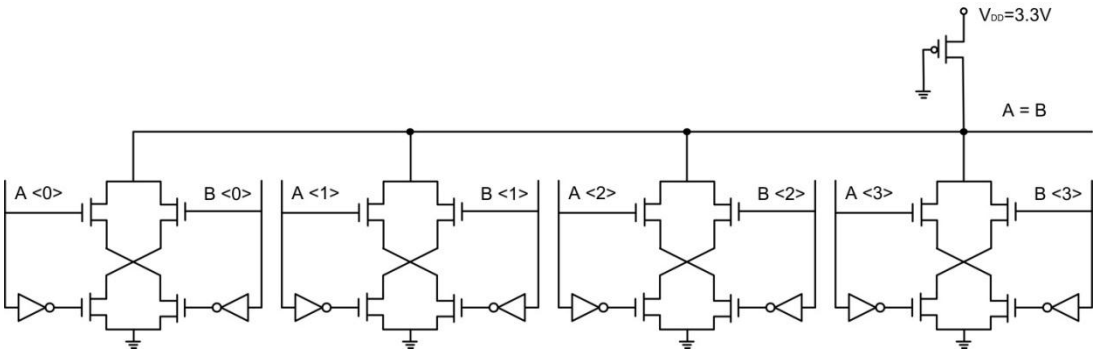


Figure 3.10 Schematic of 4-bit pseudo NMOS comparator.

Table 3.3 (W/L) values of the transistors for designed 8-bit comparator.

	NMOS Transistors	PMOS Transistor
W (μm)	1	0.7
L (μm)	0.35	0.35

In our designed IC, there are 16 comparators. Each of these comparators has two input ports, one port with eight pins for getting the delay information from shift register and the other port which has eight pins too is for getting the information from global counter. FPGA provides the values of 8-bit global counter. In each beam-former circuit, when the value of shift register is identical with global counter's one, the comparator generates enable signal and its output goes high. As shown in Figure 3.11, 8-bit comparator consists of seven 1-bit comparators and one PMOS transistor. The output of the 8-bit shift register is connected to port "A" one by one and FPGA provides the values of global counter using eight lines through port "B".

As shown in Figure 3.12, when port A and port B are equal, the comparator's output goes high. As stated before, connecting the output of the comparator to a buffer gate increases the reliability of the circuit and makes the output voltage to swing in full range but at the same time, it increases the area of the IC.

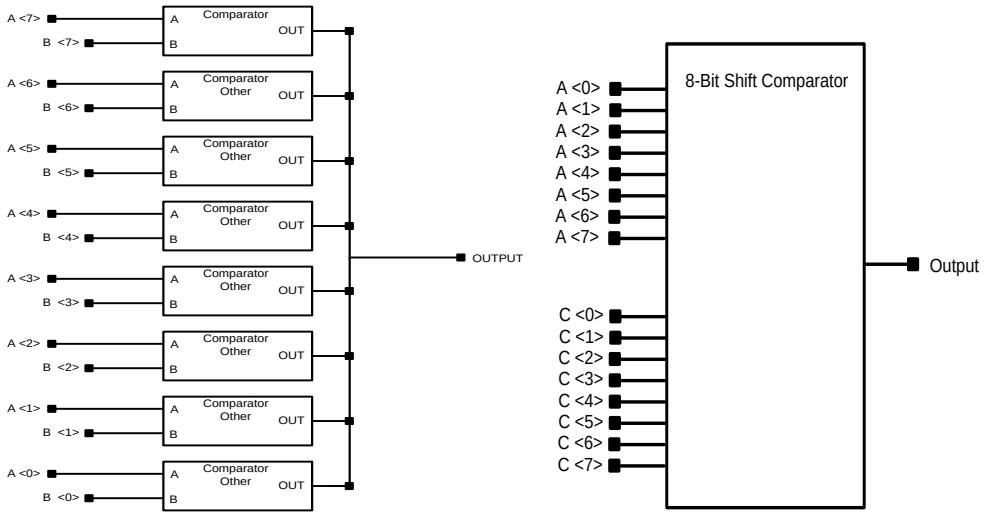


Figure 3.11 Final 8-bit comparator block diagram.

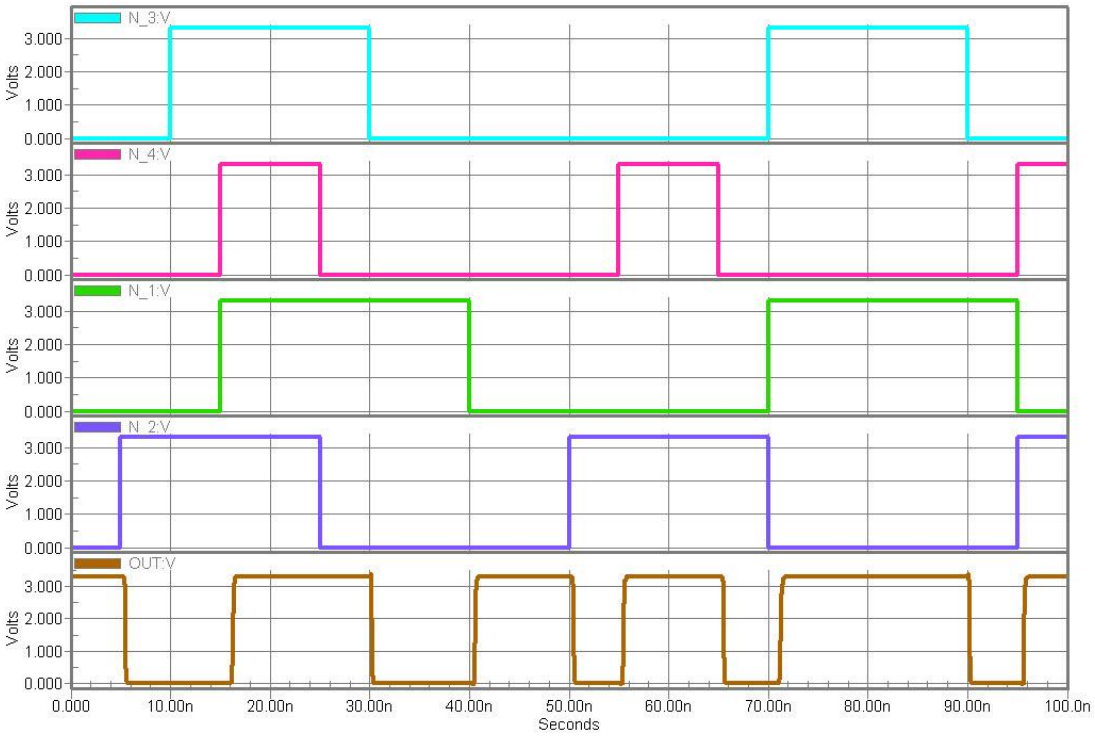


Figure 3.12 simulation result of 8-bit pseudo NMOS comparator.

Figure 3.13 shows the connection of the 8-bit shift register and 8-bit comparator. As we stated before in each beam-form circuit, when the value stored in the shift register is equal with the Gray-code counter provided by the FPGA, the comparator's output goes high. We need an 8-bit comparator for each CMUT element to compare the information of input delay and Gray-counter codes so that we can fire any transducer whenever requested. We just

need to write the codes in FPGA for shift registers and send the same codes for counter in intended time via FPGA. As shown in Figure 3.14, at 100 MHz clock frequency, the 8-bit comparator gets the 8-bit data in parallel mode from shift register and if two ports of it are identical, then the output of the comparator goes high and using next stages the CMUT element will be fired by high voltage pulses or pulse trains.

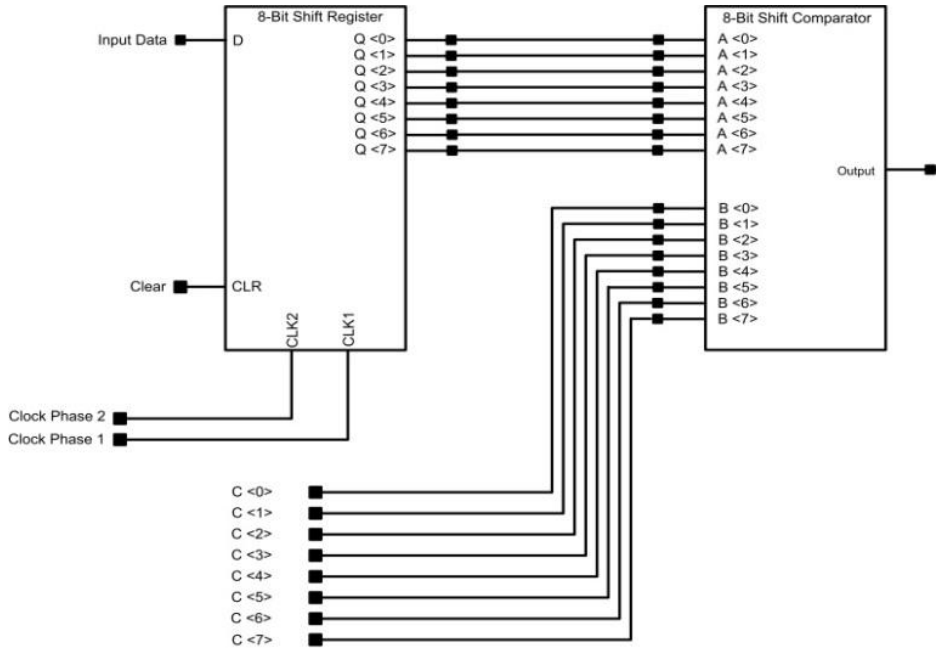


Figure 3.13 Schematic of the CMUT selection circuit.

Figure 3.15 shows the simulation results of the CMUT selection circuit at 200 MHz clock frequency. The pulse width (PW) of the generated delay information by the FPGA should be equal with the period of the clock frequencies.

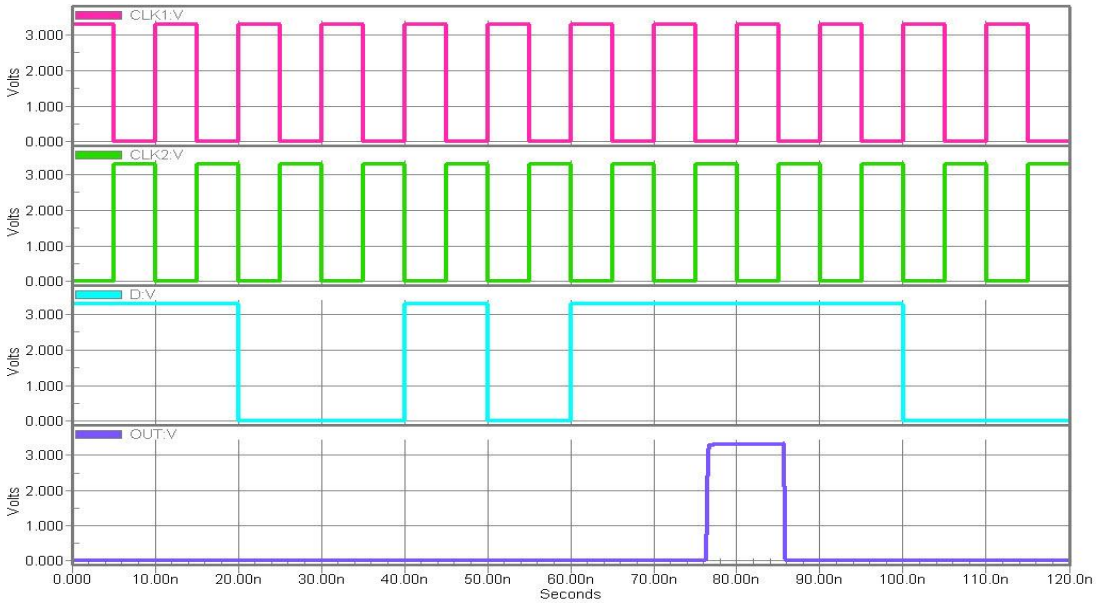


Figure 3.14 The output of the comparator goes high when it senses the same codes of 11001011 at 100 MHz clock frequency.

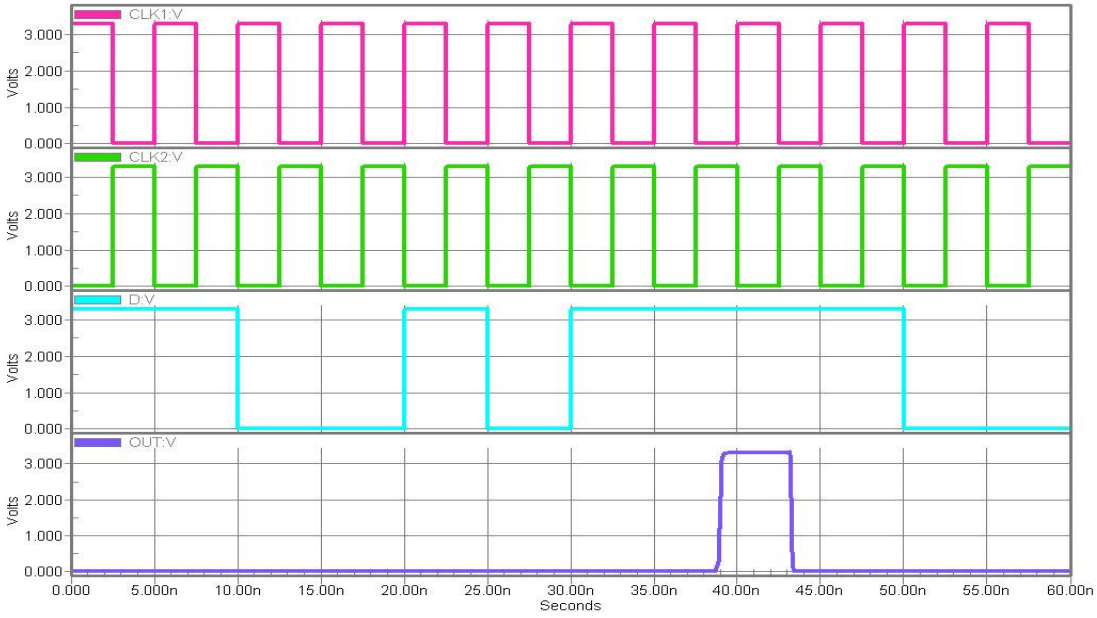


Figure 3.15 The output of the comparator goes high when it senses the same codes of 11001011 at 200 MHz clock frequency.

3.4 Single Pulse Generation Circuit with Adjustable Pulse Width

In previous section, CMUT selection method has been discussed. Before firing a CMUT element with high voltage signals, we should select that element and adjust the

specifications of the firing signal. As we mentioned before, there are two options for CMUT firing in our deigned IC, one is adjusting the pulse width of the single pulses and another is generating pulse trains with arbitrary frequency. In this section, pulse width adjusting of the single pulses has been discussed. Since different CMUT elements have different operating frequencies, we need to adjust the pulse width of the output signals. For instance:

• Pulse width minimum (for 40 MHz transducers): ~ 8 to 10 ns

• Pulse width maximum (for 5 MHz transducers): ~100 ns

In our designed IC, for adjusting the width of the pulses, one-shot circuits have been used. Figure 3.16 shows the proposed one-shot circuit. In our proposed one-shot circuit, we control the width of the pulses using M_0 transistor instead of the M_1 and M_2. By controlling the current (I_{SET}) flowing through the capacitor C, we can adjust the width of the output pulses. In our design, the pulse width of the output signal is proportional to I_{SET}/C ratio which means that by increasing of I_{SET} we can generate signals with large pulse widths. The capacitor of C has been fixed on 2 pF and hence the pulse width is just proportional to I_{SET}. In our designed one-shot circuit for generating signals for 5 MHz ultrasound transducers we need to adjust the I_{SET} on about 75 µA.

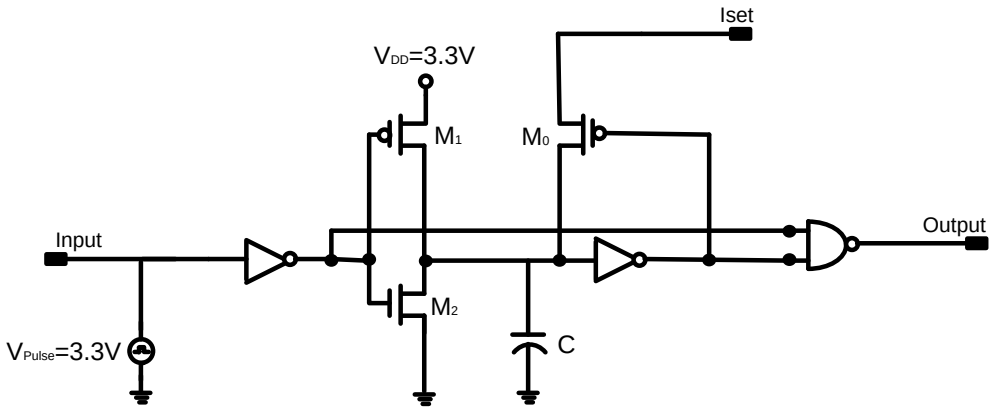


Figure 3.16 The schematic of the one-shot circuit.

Table 3.4 (W/L) values of the transistors for designed transmission gate (T-Gate) register.

Transistor name	Type	W (µm)	L (µm)
M_0	PMOS	8	0.35
M_1	PMOS	2	4
M_1	NMOS	1	4

Table 3.5 Comparisons of different designed one-shot circuits.

	Prior similar designed one-shot circuit in 2009 [49]	Proposed one-shot circuit
Getting I_{SET} through	M_1 and M_2 configuration	M_0
Capacitor C (pF)	1.5	2
I_{SET} VS Pulse width	I_{SET} Between 2 and 1 mA, Pulse widths between 70 and 150 ns [49]	I_{SET} Between 70 and 77.5 µA, Pulse widths between 20 and 650 ns (can be controlled using a DAC)
CMOS Technology (µm)	1.5	0.35
Controlling Method	External current source	External current source or external 5-bit binary codes using in-chip current mirror circuit

According to Table 3.5 we can see that, our designed one-shot circuit can generate large pulse widths by having much less power consumption. Besides, since we just need I_{SET} current in the range of 70 µA to 78 µA, we can drive the circuit using an in-chip DAC (digital to analog converter) circuits.

Instead of controlling the one-shot circuit via an external current source, according to Figure 3.17 we can add a current mirror stage including six PMOS transistors and we can adjust the pulse width of the signal using 5-bit binary codes by FPGA. Current mirror transistors have been sized according to generate the favorite currents for providing needed widths of the pulses. Figure 3.17 shows the simulation results of the designed one-shot circuit. It is obvious that when we increase the I_{SET} from 70 µA to 77.24 µA, the width of the output pulse changes from 19 to 638.2 ns. Controlling part of the one-shot circuit (Figure 3.17) is explained in more detail in section 3.5.4.

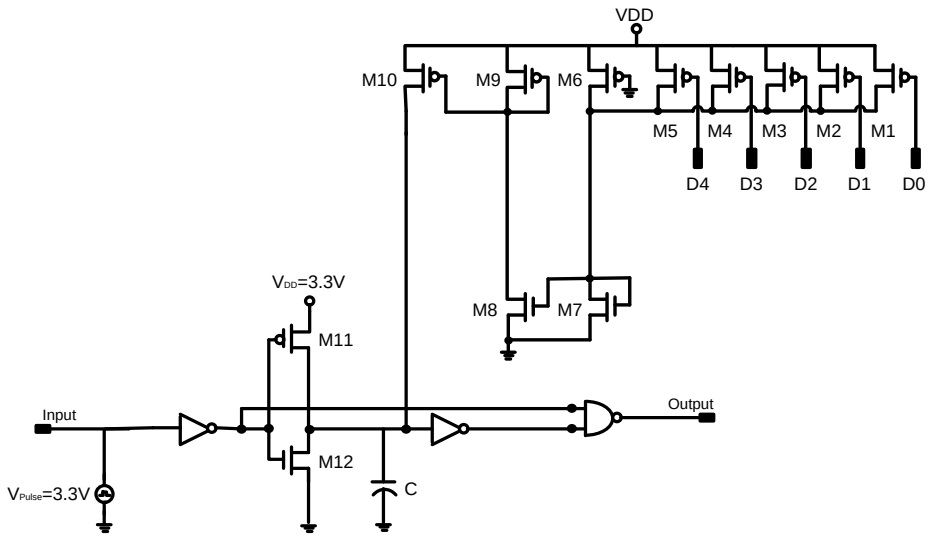


Figure 3.17 The proposed digitally controlled one-shot circuit.

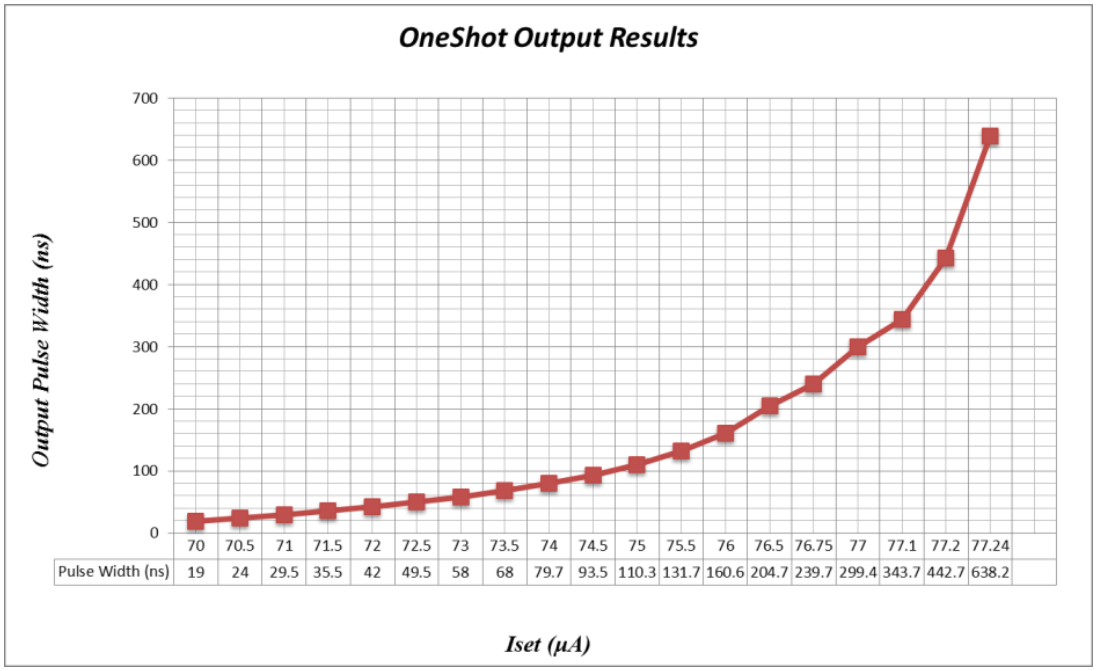


Figure 3.18 Simulation results of one-shot circuit by increasing the I_{SET} current.

3.5 Pulse Train Generation Circuit with Controllable Frequency

In previous section, the controlling methods of pulse widths according to the operating frequency of the CMUT elements have been discussed. If we want to fire the CMUT elements using single pulses, we need to select the first mode for pulse generation. In another cases such as therapeutic or 3D color Doppler imaging applications, we prefer to fire the CMUT elements with pulse trains instead of single pulses. The frequency of generated pulse trains should be selected according to the operating frequency of the CMUT elements. In this section, pulse train generation method with arbitrary frequency in the range of 1 to 10 MHz has been discussed. Since various CMUT elements with different operating frequencies in the range of 1 to 10 MHz can be designed, we tried to design a flexible pulse train generation circuit with good frequency resolution.

3.5.1 Overview of the Variable Delay Elements

Variable delay elements can be used in many VLSI applications such as digital locked loops (DLLs) [71], phase locked loops (PLLs) [72], [73], microprocessor, digitally controlled oscillators (DCOs) [74], [75] and memories [76], [77]. The delay between the input and output can be changed to adjust the delay value. By manipulation of rising or falling edges of the clocks or signals in integrated circuits we can design variable delay elements. Analog or digital circuits can change the value of the delay elements. The delay should be controlled precisely because it affects the overall performance of the IC. By controlling the voltage or current using analog circuits, desired delay values can be achieved [78]. On the other hand, by discrete voltages [76] or capacitance [79] we can manipulate the delay through digital circuits in digitally controlled delay elements (DCDEs). Several different methods with their

advantages and drawbacks have been used for implementing a delay element. Figure 3.19 shows a switch network of NMOS and PMOS transistors which have been placed at the source of M_2 and M_1 transistors in a CMOS inverter, respectively. The delay of the falling and rising edge of the output voltage can be controlled using the input vector of the NMOS and PMOS switch networks, respectively. Different separate delays with required delay resolution can be achieved by increasing the number of the NMOS and PMOS transistors in switch networks. By changing the digital input vector, the current passing through M_2 and M_1 is changed and causes the delay of the inverter circuit to change. One of the main drawbacks of these kinds of circuits is that the delay of the output signal may not change monotonically according to the input vector [78].

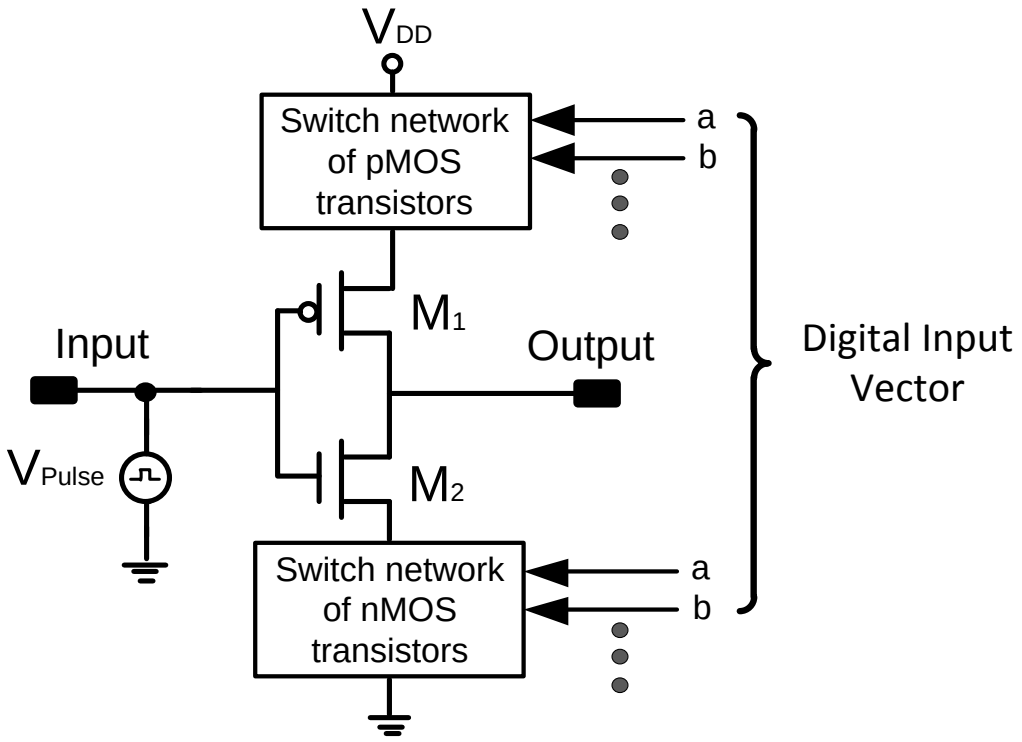


Figure 3.19 Basic structure of a typical delay element with switch networks.

3.5.2 Popular Methods for Designing a Variable Delay Element

Three types of popular techniques can be used for implementing a digitally controlled delay element. These methods are known as shunt capacitor method, current starved method and variable resistor method [74]. Shunt capacitor and current starved method techniques have been discussed in this section.

Figure 3.20 shows a delay element with shunt capacitor implementation. In this circuit, the source of the transistor M_3 is connected to the gate of the transistor M_4 which acts as a capacitor. Transistor M_3 is supposed to control the charging and discharging current to the

transistor M_4 (capacitor). V_{ctrl} controls the discharging current to the M_4 by adjusting the gate voltage of the M_3. As a result the delay of the circuit can be controlled.

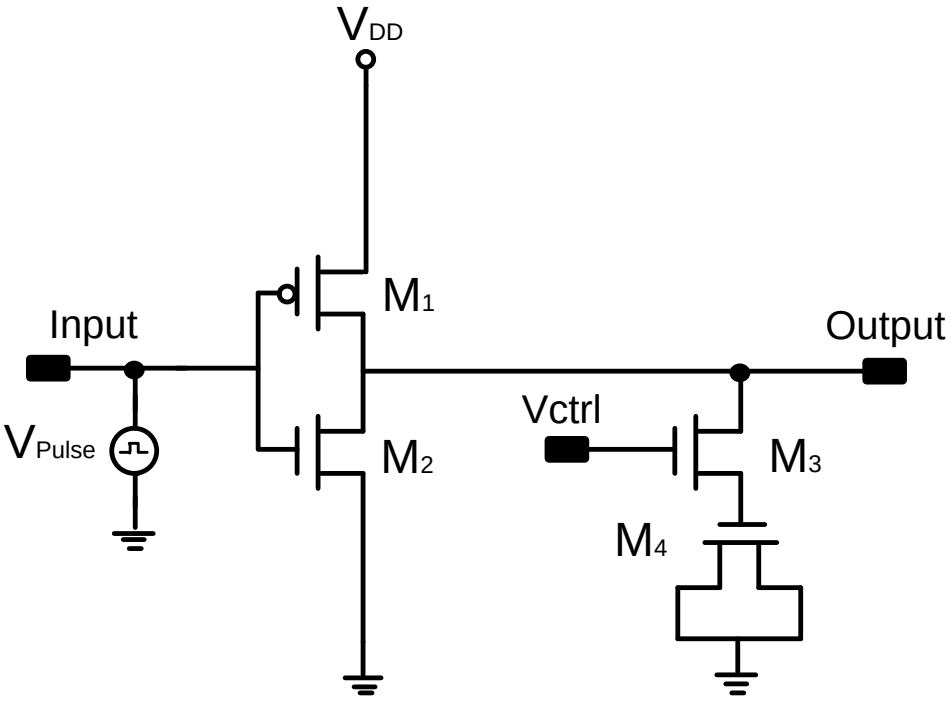


Figure 3.20 Basic structure of a shunt capacitor delay element.

The basic structure of a DCDE based on the current starved inverter is shown in Figure 3.21. As shown in this Figure, M_n – M_p and M_1 – M_2 form two inverters. These inverters have been used between input and output of the circuit. C_L is the output capacitance of the first inverter which is composed of M_n and M_p. The charging and discharging of C_L can be controlled using two sets of NMOS (M_{n1}, M_{n2}, …) and PMOS (M_{p1}, M_{p2}, …) transistors at the source of M_n and M_p, respectively. These sets of transistors control the current of the first inverter and they should be sized in a binary fashion. For example, the W/L ratio of the M_{p2} is n-times of the M_{p1} and so on. The gates of the controlling transistors receive the binary vector from a FPGA to specify the current of first inverter. In each specific binary vector some of the transistors in the source of M_n and M_p are turned on and hence the rise and fall time of the first inverter can be controlled. As a consequence, the delay of the output voltage of the first inverter (M_n – M_p) is adjusted [75], [76].

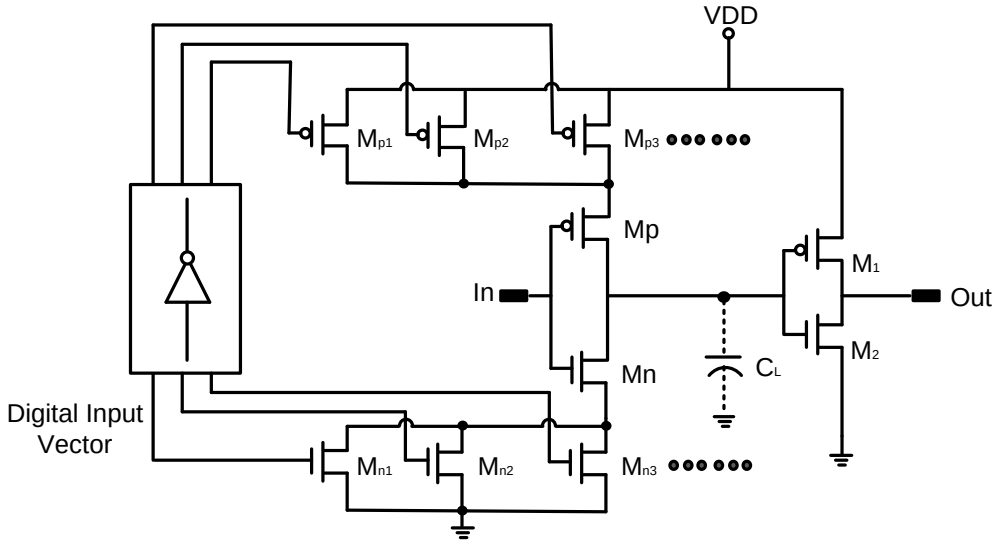


Figure 3.21 Basic structure of a current starved delay element.

3.5.3 Proposed DCO with DCDE Circuit

As we stated before, digitally controlled delay elements (DCDEs) can be used dramatically in integrated circuits. In our therapeutic application, we want to fire CMUT elements using pulse trains instead of single pulses. For pulse train generation mode, the combination of DCOs (Digitally Controlled Oscillators) with DCDEs (Digitally Controlled Delay Elements) can be used. Figure 3.22 shows the proposed DCO-DCDE circuit. DCO as a digitally controlled oscillator circuit changes the state of the output in each cycle and generates pulse trains with 50% duty cycle. The pulse width, period and frequency of the generated pulse train exactly depend on designed variable elements. In fact, the period of the pulse train is twice of the delay time which is generated using digitally controlled delay elements (DCDEs). It is obvious that, if we want to control the period of the pulse trains, we should control the delay value of the variable delay elements. Three DCDEs have been used for controlling the frequency of the pulse trains. Designed DCDEs can be controllable by 5-bit digital input vectors using FPGA, so we have $2^5 = 32$ types of pulse trains with different frequencies.

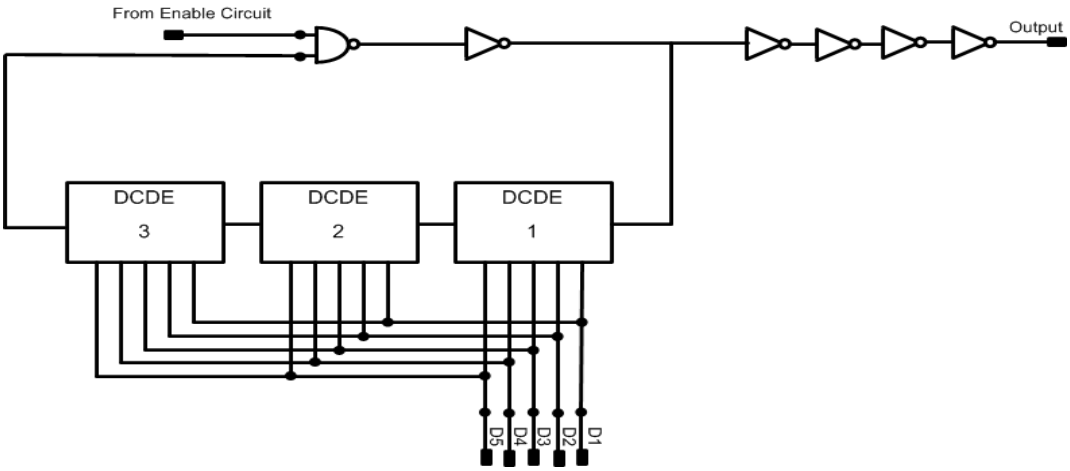


Figure 3.22 Schematic of the DCO circuit with three 5-bit DCDEs.

As shown in Figure 3.22, there is a pin with the name of "From Enable Circuit". If this pin is zero we will not have any signal at the output but if this pin is enabled using enable circuit and the 5-bit of DCDE circuits are given via FPGA, the pulse train with selected frequency can be observed at the output of the DCO-DCDE. The enable pin of DCO-DCDE should be kept high until we want to have a pulse train at the output. Whenever this pin is at the low state, the output goes zero hence we should keep this pin at high state using an enable circuit. For this purpose one simple circuit, which is shown in Figure 3.23, has been used. As shown in Figure 3.23, the enable circuit gets the activation signal from 8-bit comparators using its CLK port. The data port (D) of the circuit should be kept high and finally the RN controls the lifetime of the pulse train. Figure 3.24 shows the schematic of the enable circuit which has been used in DCO-DCDE circuit.

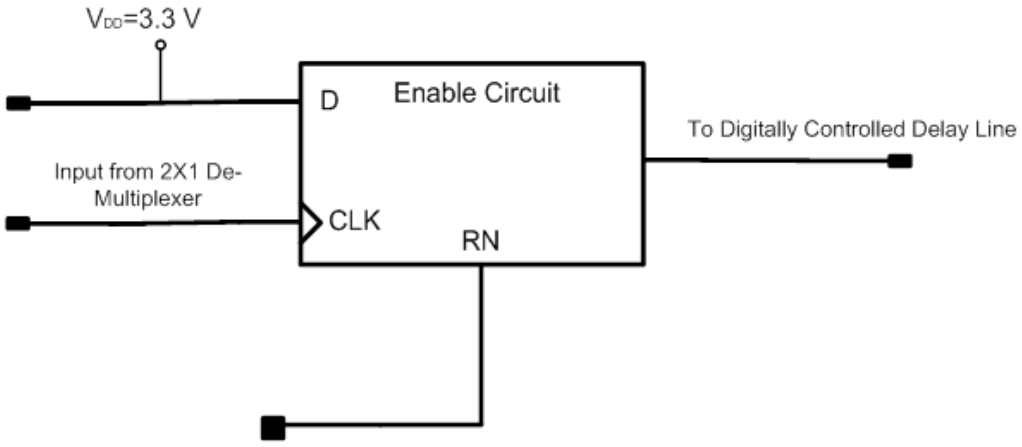


Figure 3.23 Enable circuit of DCO-DCDE.

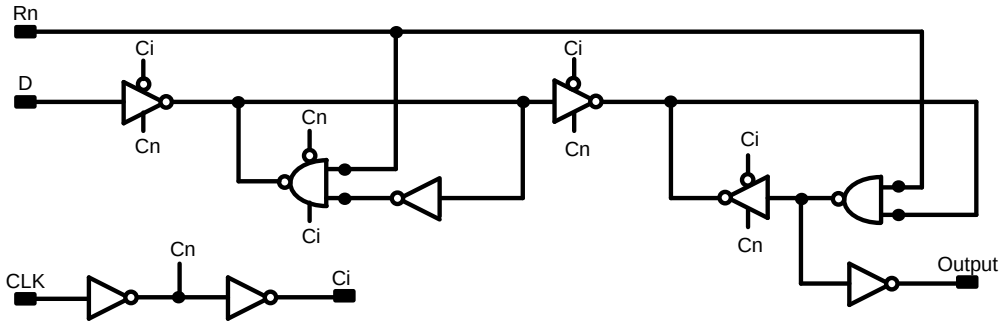


Figure 3.24 Schematic of the enable circuit.

As shown in Figure 3.25, when the enable circuit gets the command from 8-bit comparator, its output goes high and remains until we disable it externally using its RN port, then we can generate pulse trains at the output of the DCO-DCDE. If we want to change the pulse train frequency, we should change the digital input vector of the DCDE circuit using FPGA. Designed circuit is completely flexible for generating different frequencies. Various pulse trains in limited and unlimited times can be generated. Besides, we can generate pulse trains in a limited times and each time with a different frequencies.

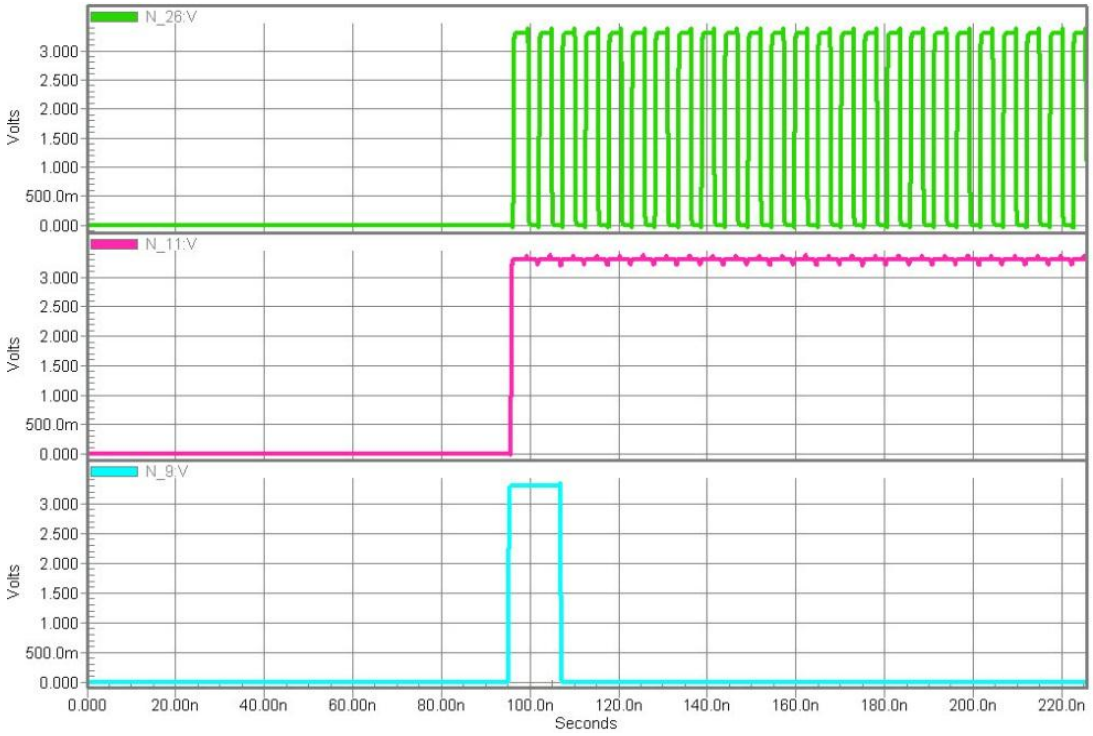


Figure 3.25 Simulation results of the enable circuit.

3.5.4 Digitally Controlled Delay Element (DCDE) with 5-bit Digital Input Vector

Figure 3.26 shows the designed 5-bit digitally controlled delay element [80]. This circuit consists of three major parts. The combination of M10, M11, M12 and M13 transistors make the current starved inverter circuit. Transistors M10 and M13 control the fall and rise time, respectively. The delay of the circuit can be adjusted using the current of M10 and M13 transistors. Having the same rise and fall time (50% duty cycle) in our output signal is very important for our application, hence M7, M8 and M9 transistors for designing a current mirror circuit should be considered. M7 gets the current from digitally controlled transistors and copies the same one to M10 and M13. The current of last stage can be controlled using M1, M2, M3, M4 and M5 transistors. By providing a specific binary vector using FPGA to the controlling transistors (M1 – M5), a combination of those transistors is turned on and applies different currents for current-starved stage. These transistors are turned on or off via external lines using FPGA. We should note that, transistor M6 should be kept on.

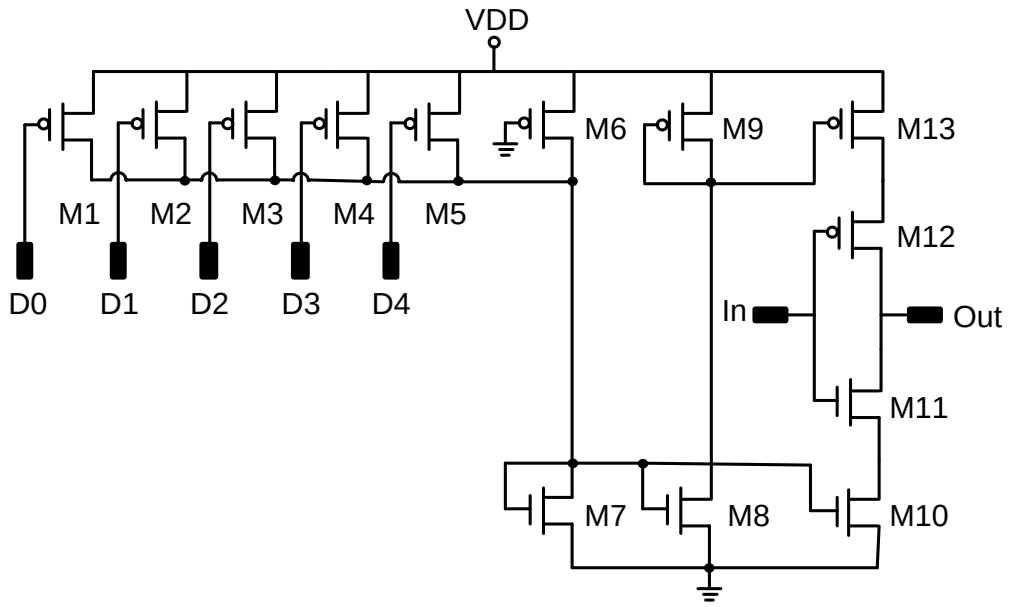


Figure 3.26 Digitally controlled delay element (DCDE) with 5-bit digital input vector.

3.5.5 Mathematical Model of the Designed Digitally Controlled Delay Element (DCDE) with 5-bit Digital Input Vector

In previous section, some information about the design of the DCDE circuit has been provided. More details have discussed in following section. In this section, we want to calculate the DCDE delay time from in to out port of the current starved inverter (Figure 3.26). Figure 3.27 shows part of the digitally controlled delay element (DCDE). As it can be seen from this figure, the controlling transistors dictate the current I to M7. Since M7 and M8 have same specifications like gate-source voltage and W/L ratio, then they will sense

the same amount of current in their drains. M8 copies I to M9 and then M13, as a consequence M13 and M10 will receive the same current of I and the rise and fall time of the output signal will be identical. To control the output of the current starved inverter circuit using M10 and M13 transistors, the sizes (W/L ratio) of the M11 and M12 transistors should be much bigger than the M10 and M13, respectively. In this section we want to find a relationship between the V_g of the M10 (M8 and/or M7) and the delay of the circuit from in to out port of the DCDE circuit.

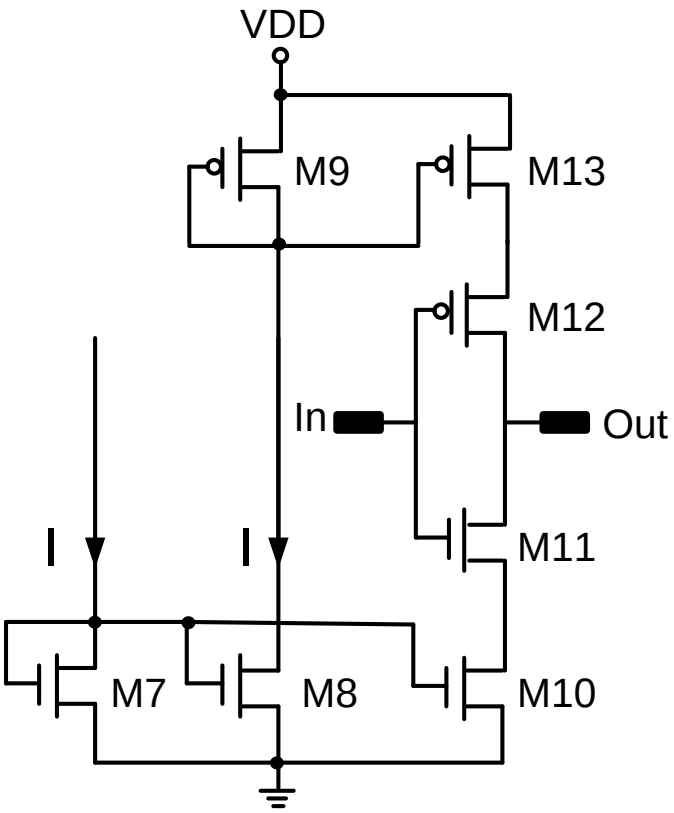


Figure 3.27 Part of the digitally controlled delay element (DCDE).

Following equation as long as the M10 transistor is in the saturation region can be considered as its drain current.

$$I_{d-M10} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{10}\left[V_g - V_{TH10}\right](1+\lambda_{10}V_{DS10}) \tag{3.1}$$

If we suppose that, the drop voltage across the M11 transistor is negligible, we will have:

$$V_{DS10} \cong V_{OUT} \tag{3.2}$$

The output voltage of the DCDE circuit can be found from the following equations:

$$I_{d-M10} = -C_L \frac{dV_{OUT}}{dt} \tag{3.3}$$

$$\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{10}\left[V_g - V_{TH10}\right](1+\lambda_{10}V_{DS10}) = -C_L \frac{dV_{OUT}}{dt} \tag{3.4}$$

C_L is the overall capacitance at the output node. By solving the equation of 3.4 with following initial condition, the results can be found as:

$$V_{OUT} = VDD \ @ \ t = 0 \tag{3.5}$$

$$V_{OUT} = (VDD + \frac{1}{\lambda_{10}})e^{\frac{-t}{\tau}} - \frac{1}{\lambda_{10}} \tag{3.6}$$

$$\tau = \frac{C_L}{\lambda_{10}} \times \frac{1}{\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{10}\left[V_g - V_{TH10}\right]} \tag{3.7}$$

At $t = t_{delay}$ (the delay between in and out ports of the DCDE circuit), V_{OUT} =VDD/2. As a consequence, the final delay time of the DCDE circuit can be shown as following equation:

$$t_{delay} = \tau \times Ln\frac{1+\lambda_{10}VDD}{1+\lambda_{10}\frac{VDD}{2}} \tag{3.8}$$

3.5.6 Design Procedure of Digitally Controlled Delay Element (DCDE) with 5-bit Digital Input Vector

In this section, the design process of the DCDE has been discussed. Since the W/L ratios of the controlling transistors define the delay value of the DCDE circuit, we should evaluate the effects of those transistors on delay time. According to Figure 3.26, transistor M6 should be kept on. To find the effect of M6 transistor on the delay value of the DCDE circuit, M1 – M5 controlling transistors are considered constant. As will be explained later, in our final design the W/L ratio of the M6 is 1/9.75, which is suitable for our application. Figure 3.28 shows the effects of M6 transistor width (W) from 1 µm to 8 µm while its length is 9.75 µm and digital input vector is 00000. As can be observed from Figure 3.28 M6 mainly affects the maximum delay of the DCDE circuit. When the width of the M6 increases the current flowing into M7 enhances too and hence the delay value of the DCDE circuit is increased. As can be seen from Figure 3.28, this variation is slight and monotonic in our designed DCDE circuit.

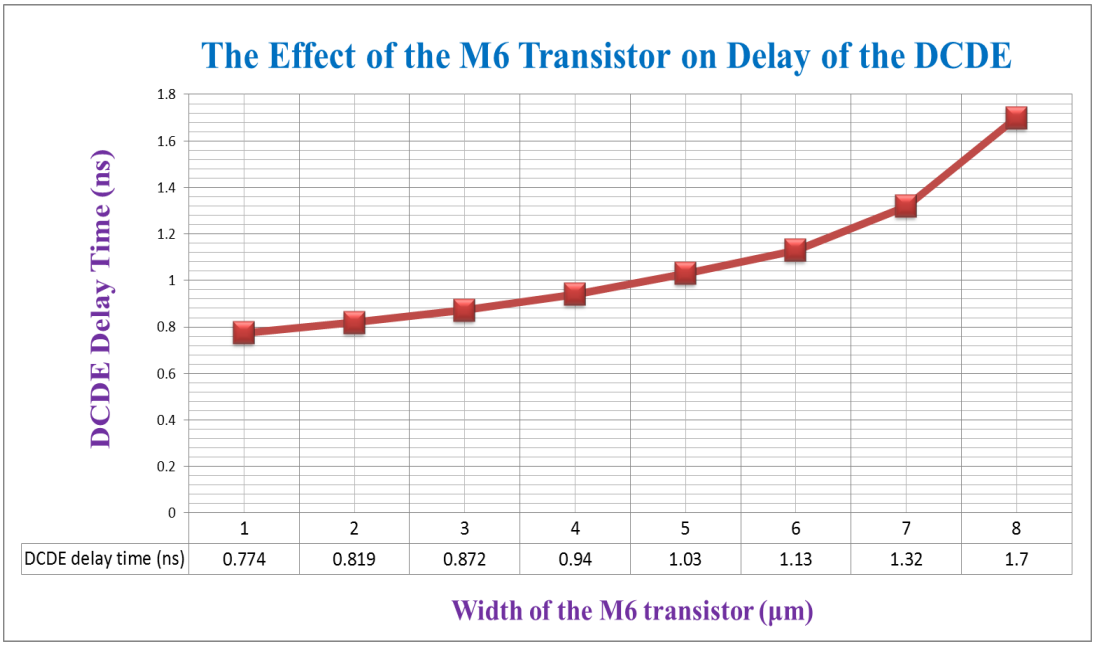


Figure 3.28 Effects of M6 transistor width (W) while its length is 9.75 µm and the digital input vector is 00000.

When we fixed the size of the M6 transistor on 1/9.75 and size the M1 – M5 transistors, we observed that these controlling transistors just affect the minimum delay of the DCDE circuit and has not any effect on the maximum delay of the circuit. Since DCDE is controllable via five bits digital input vector, 32 different frequencies can be obtained. The amount of the frequencies can be changed monotonically with increment of the 5-bit digital input vector but for our application we divided 32 different frequencies into eight packets such that they are monotonic in eight divided small areas. More details will be introduced in following parts.

The sizing of the designed DCDE circuit which is shown in Figure 3.26 can be considered in eight main steps [81].

1. The sizes of the M11 and M12 transistors which make the current starved inverter are determined by the capacitance load.
2. To control the output of the current starved inverter circuit using M10 and M13 transistors, the sizes (W/L ratios) of the M11 and M12 transistors should be much bigger than the M10 and M13, respectively. In this case the charging and discharging current can be adjusted by M13 and M10, respectively.
3. M7 and M8 can be the same size as M10 and M9 can be the same size as M13.
4. The number of the controlling transistors can be obtained according to the number of different delays that we want to have at the output of the circuit. That is

$$d = 2^N \tag{3.9}$$

where d is the number of different delays that can be generated by the DCDE circuit and N is the number of controlling PMOS transistors.

5. M6 is sized according to desired maximum delay value of the DCDE circuit which is shown in Figure 3.28.
6. If we have N number of parallel PMOS transistors as our controlling elements, we can suppose all of these transistors as one united PMOS. In our designed DCDE circuit we considered five PMOS controlling transistors. For sizing of these transistors we made them united and sized the united PMOS transistor (M_0) for our minimum desired delay time.
7. M_0 can be broken into N (five for our application) different PMOS transistors (M1 – M5). The W/L ratio of these transistors can be calculated from following equation.

$$\left(\frac{W}{L}\right)_{M_{Pi}} = \frac{2^{i-1}}{2^N - 1}\left(\frac{W}{L}\right)_{M_0} \qquad \text{For i = 1 to N.} \qquad (3.10)$$

8. The combinations of the M1 – M5 transistors determine the delay of the DCDE circuit and the relationship of those delay values with digital input vector. To have a monotonic relationship between the digital input binary code and the delay of the circuit we should size the M1 – M5 transistors according to step 7 and the methods that were discussed in previous parts.

Designed digitally controlled delay element (DCDE) is simulated using HV 0.35 µm CMOS process under Tanner S-Edit environment. According to previous sections, many points were considered and different circuits were designed. The designs are optimized in a way that designed DCDE meets essential requirements for our application. Table 3.6 summarizes the final (W/L) values of transistors of the designed 5-bit DCDE circuit.

Table 3.6 (W/L) values of the transistors for designed 5-bit DCDE.

Transistor	M1	M2	M3	M4	M5	M6	M7
W (µm)	1	1	1	1	1	1	5.5
L (µm)	11.5	7.5	6.6	5.85	4.8	9.75	1
Transistor	M8	M9	M10	M11	M12	M13	
W (µm)	5.5	7.5	5.5	3.2	12	7.5	
L (µm)	1	1	1	0.35	0.35	1	

Figures 3.29 and 3.30 show the simulation results of the designed 5-bit DCDE. At a glance, these figures feature that by increasing the 5-bit digital input vector, we can reach large periods and fewer frequencies of pulse trains but when we check the details of the graphs, we realize that in some binary codes in spite of getting more values of periods in comparison with the previous ones, less values have been obtained. In typical DCDE design, monotonic relationship between the digital input binary code and delay value is desirable but we found that, when we want to access some delays more than others we need to design a monotonic one in small divided areas.

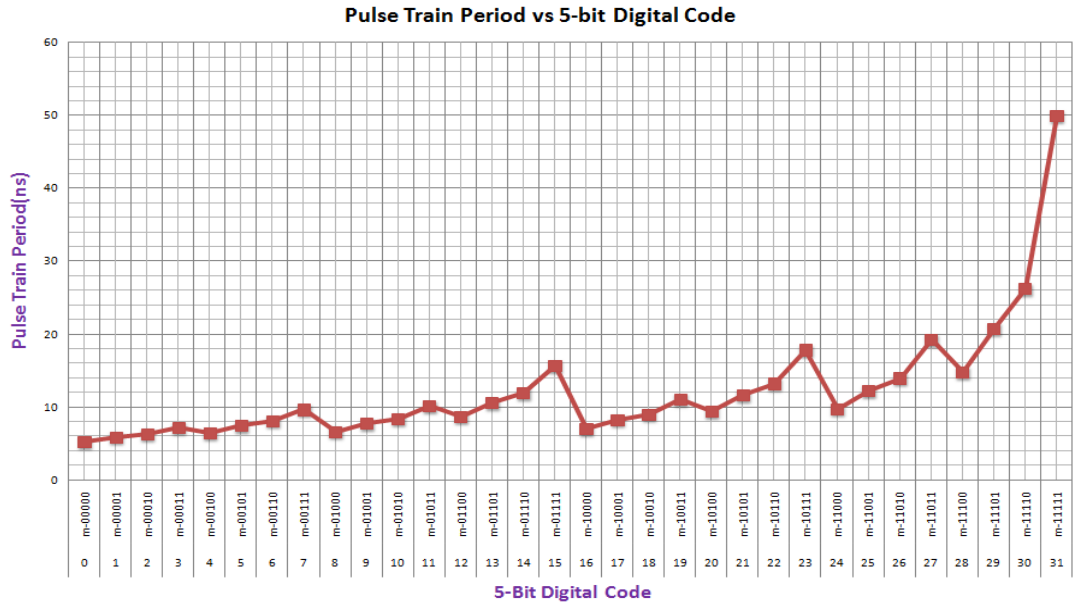


Figure 3.29 Relationship of digital input vector with periods of pulse trains of designed 5-bit DCDE.

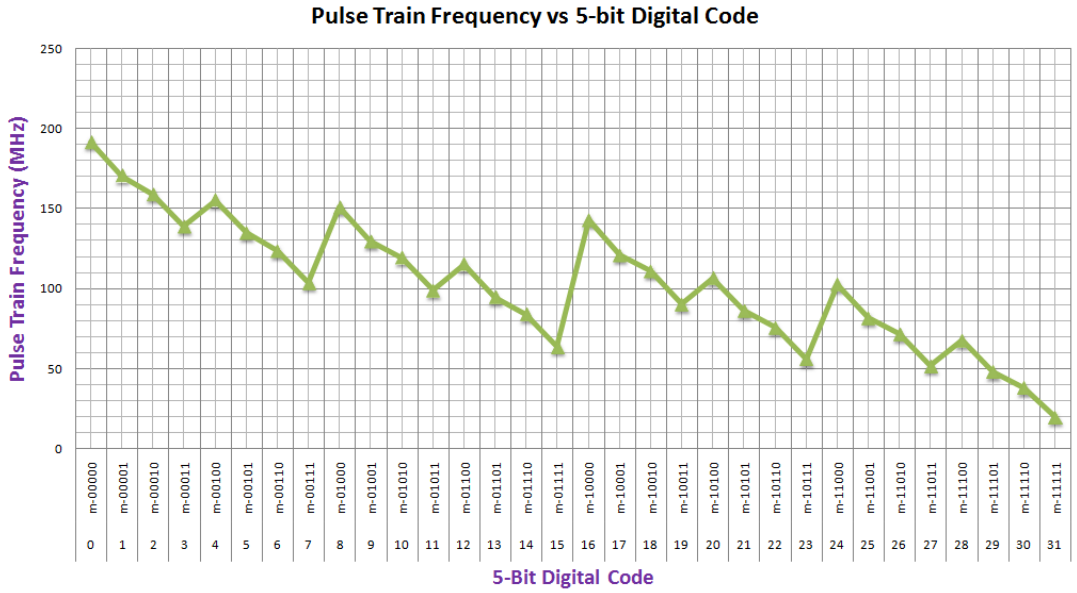


Figure 3.30 Relationship of digital input vector with frequencies of pulse trains of designed 5-bit DCDE.

As we mentioned before, although we could design a completely linear and monotonic DCDE but since we decided to generate specific frequencies (not just in increasing mode), we designed a DCDE in such a way that to have a linear relationship in small divided areas. In fact by designing a completely monotonic DCDE for our application, some important frequencies in the range of 1 to 10 MHz can be lost. As shown in Figure 3.31, the graph of Figure 3.29 has been divided into eight parts. As can be observed, there is a monotonic and ascending relationship between digital input vector and the period of the pulse trains in all

of divided small areas. In each area, there is a reduction in first point of them in comparison with the last point of the previous area, because as shown in Figure 3.32 we don't want to lose desirable frequencies before going to next points.

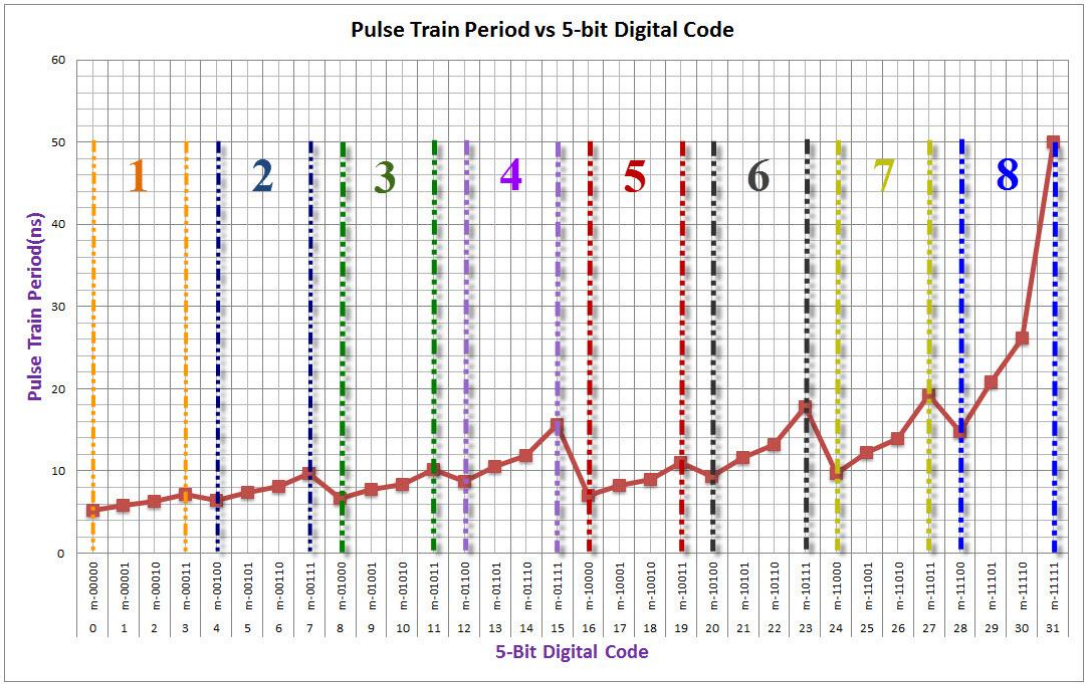


Figure 3.31 Dividing the simulation results of 5-bit DCDE into eight small areas.

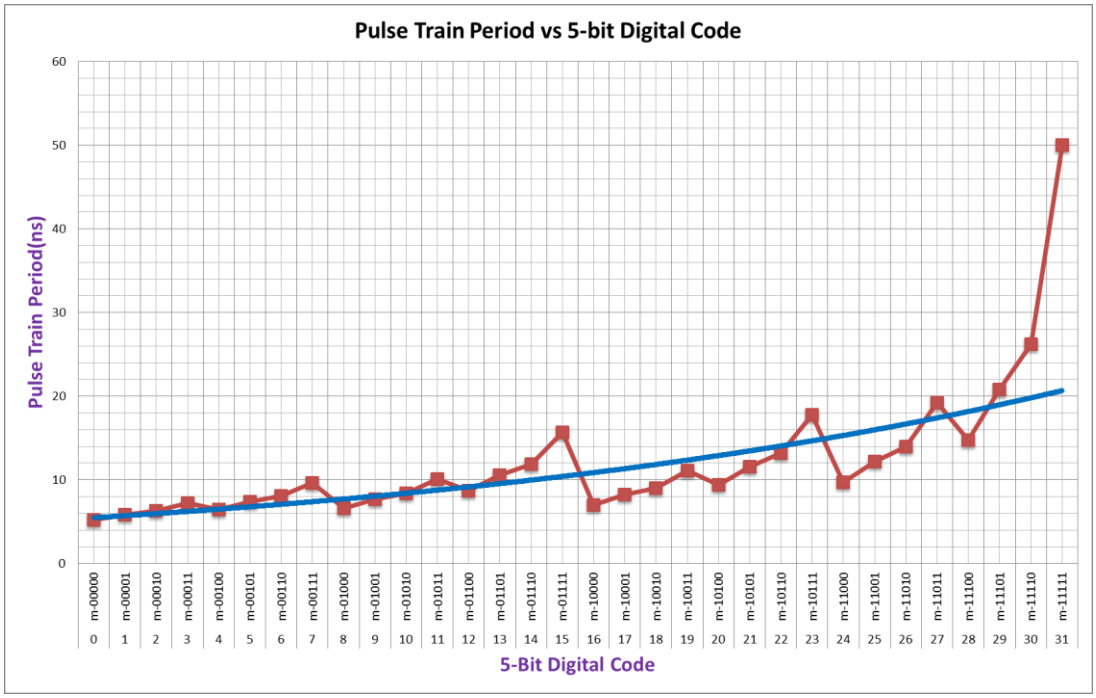


Figure 3.32 Comparison of simulation results of 5-bit DCDE in completely monotonic relationship and monotonic behavior in small divided areas.

The stability of a digitally controlled delay element is very vital because having a very precise and stable DCDE can be desirable in most of the applications. One of the most important performance parameter of a DCDE is the effect of voltage supply (VDD) variations. We have simulated DCDE in -10% VDD variations as our worst case. We have done some techniques in our layout part for delivering the supply voltage for delay elements directly and with short and low resistance metal lines. These techniques reduce the effects of VDD variations on the performance of the DCDE circuit dramatically but in spite of considering those techniques, we designed a low sensitive DCDE to supply variations. Figure 3.33 shows delay values of designed DCDE with -10% supply variation for one small divided area. As can be observed from this figure, the variation values are less than 5%. The average power consumption of designed 5-bit DCDE with two buffers is 165 and 844 µw when the circuit generates delays of 21 ns (for generating 20 MHz pulse trains when the digital input vector is 11111) and 1.54 ps (for generating 650 GHz pulse trains when the digital input vector is 00000), respectively.

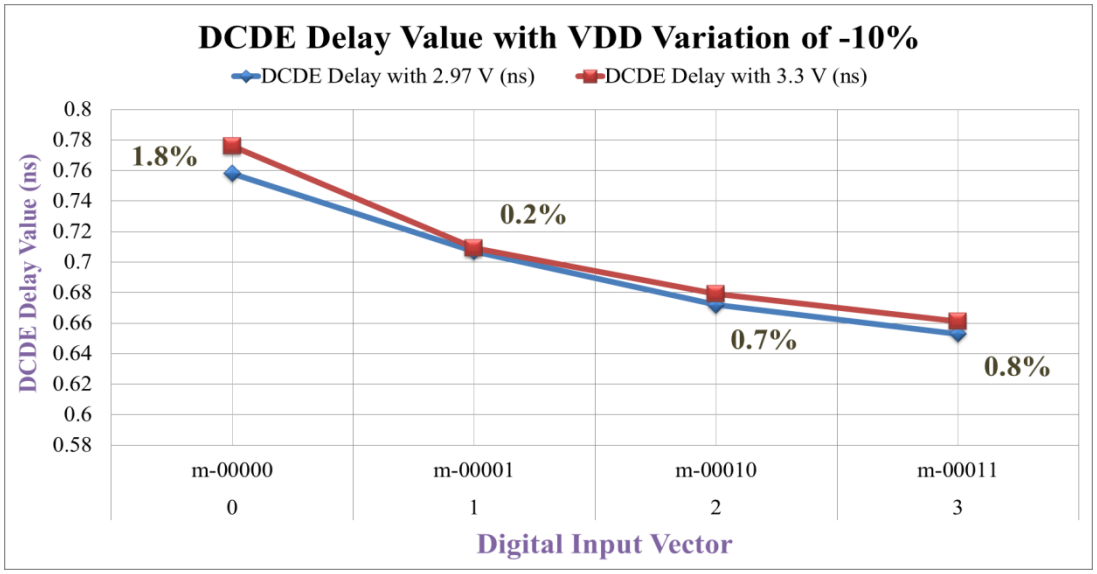


Figure 3.33 Simulation results of delay values of designed DCDE with -10% supply variation for one small divided area.

Figures 3.34 and 3.35 show the simulation results of DCO-DCDE circuits. As shown, when the output of the comparator goes high, the enable signal for DCO is generated with a negligible delay time and finally a pulse train with 50% duty cycle is achieved. As can be observed, a pulse train with 190 MHz and 71.5 MHz frequencies can be generated when the digital input vector of the DCDE is 00000 and 11010, respectively.

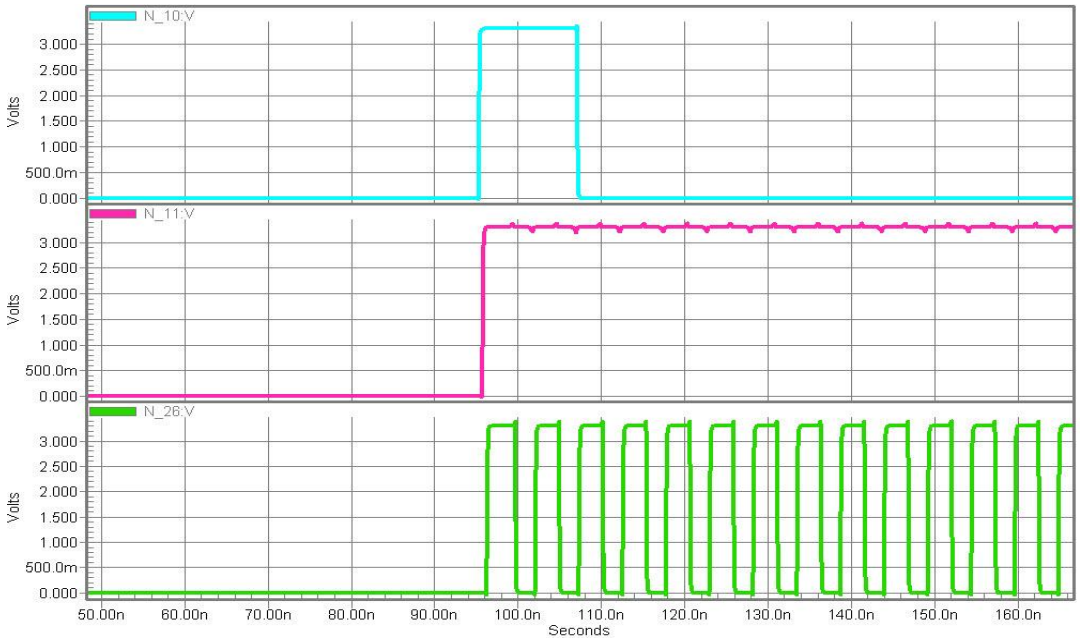


Figure 3.34 Simulation results of DCO-DCDE with 00000 as digital input vector. The period and frequency is 5.25 ns and 190 MHz, respectively.

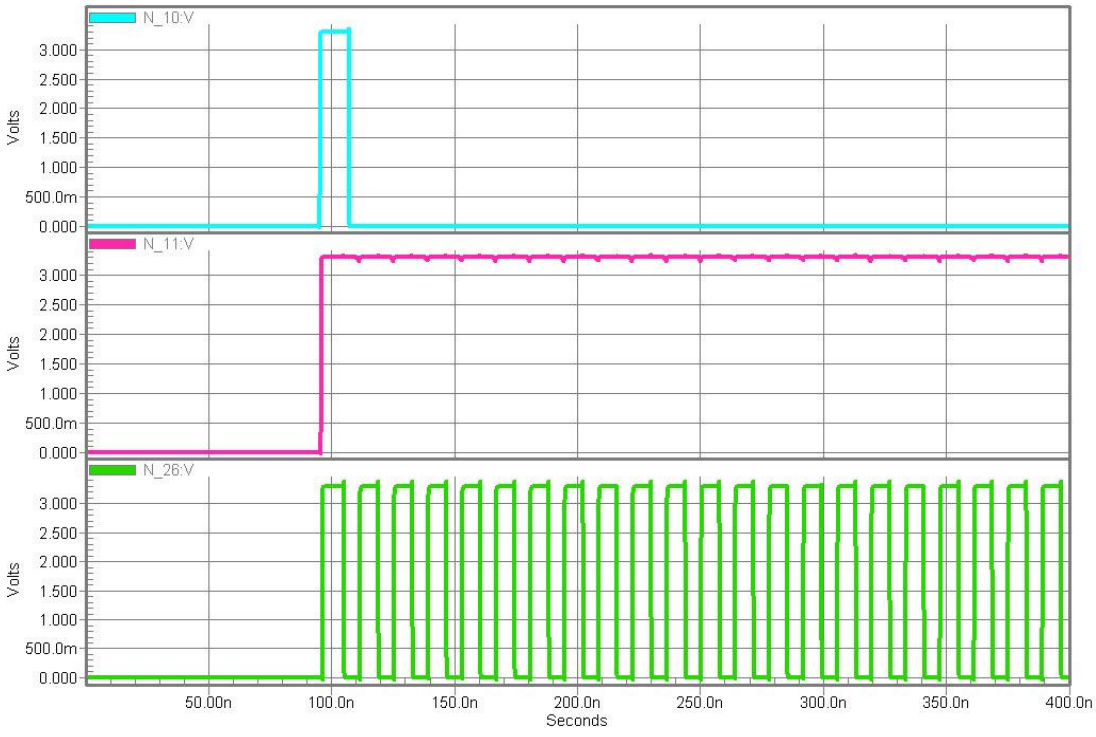


Figure 3.35 Simulation results of DCO-DCDE with 11010 as digital input vector. The period and frequency is 14 ns and 71.5 MHz, respectively.

In previous section, we evaluated the effect of the supply voltage (VDD) on stability of a single designed DCDE. The stability of designed DCO-DCDE circuit is very important too. In addition to the supply (VDD) variations, temperature variations as one of the most important performance parameter of a DCO-DCDE can affect the circuit. DCO-DCDE circuit was simulated in -10% VDD variations and in 25, 50 and 75 ℃ separately. Table 3.7 summarizes the periods of the generated pulse trains by DCO-DCDE circuit in 25 and 50 ℃. As can be observed, by simulating the DCO-DCDE circuit for five sample 5-bit digital input vectors, the variation values between 25 ℃ and 50 ℃, are less than 5%. On the other hand, Table 3.8 summarizes the periods of the generated pulse trains by DCO-DCDE circuit in 25 and 75 ℃. As can be observed, by simulating the DCO-DCDE circuit for the same five sample 5-bit digital input vectors, the variation values between 25 ℃ and 75 ℃, are less than 5% too.

Table 3.7 Effect of temperature (T = 50 ℃) on the period of designed DCO-DCDE.

Digital Input Vector	T = 25 ℃	T = 50 ℃	% of Change
11101	20.8 (ns)	21.5 (ns)	3.3%
10101	11.6 (ns)	12 (ns)	3.4%
11111	50 (ns)	51.9 (ns)	3.8%
00000	5.2 (ns)	5.4 (ns)	3.8%
11110	26 (ns)	26.9 (ns)	3.4%

Table 3.8 Effect of temperature (T = 75 ℃) on the period of designed DCO-DCDE.

Digital Input Vector	T = 25 ℃	T = 75 ℃	% of Change
11101	20.8 (ns)	21.7 (ns)	4.3%
10101	11.6 (ns)	12.1 (ns)	4.3%
11111	50 (ns)	52.4 (ns)	4.8%
00000	5.2 (ns)	5.45 (ns)	4.8%
11110	26 (ns)	27.2 (ns)	4.6%

Table 3.9 shows the periods of the generated pulse trains by DCO-DCDE circuit with -10% supply variation. As can be observed from this table, the variation values are less than 5%.

Table 3.9 Effect of supply voltage (-10%) on the period of designed DCO-DCDE.

Digital Input Vector	VDD = 3.3 V	VDD = 2.97 V	% of Change
11101	20.8 (ns)	21.5 (ns)	3.3%
10101	11.6 (ns)	11.9 (ns)	2.5%
11111	50 (ns)	52.3 (ns)	4.6%
00000	5.2 (ns)	5.44 (ns)	4.6%
11110	26 (ns)	27.1 (ns)	4.2%

3.6 Frequency down Conversion (FDC) Circuit

Since our generated frequencies are in the range of large frequencies, we need to decrease them into 1 to 10 MHz range because the operational frequencies of our designed ultrasound transducers work in that ranges of frequencies. Figure 3.36 shows the frequency down conversion (FDC) circuit which generates desirable frequencies for our therapeutic application.

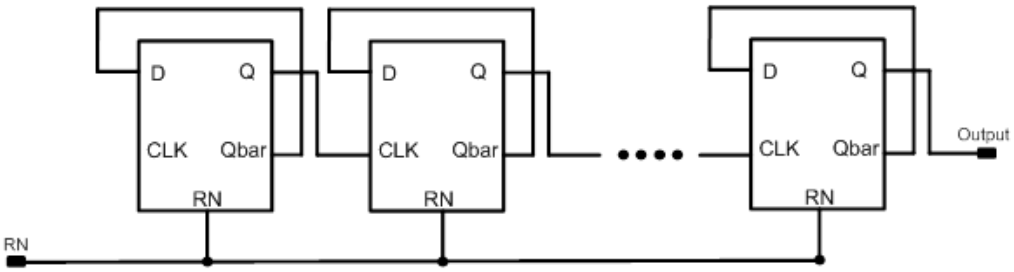


Figure 3.36 Frequency down conversion (FDC) circuit.

In our design, the frequencies of the generated pulse trains by DCO-DCDE can be divided by two in seven steps. Figure 3.37 shows the schematic of the frequency down conversion (FDC) circuit. Seven numbers of designed DFFs are placed next to each other according to Figure 3.36.

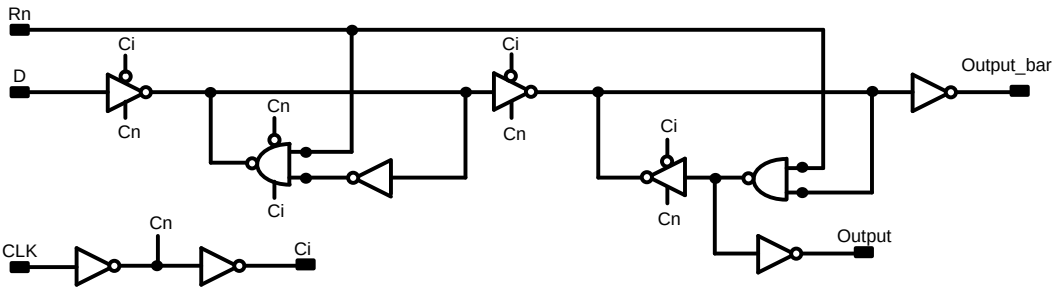


Figure 3.37 The schematic of the frequency down conversion (FDC) circuit.

Figure 3.38 shows the simulation results of the FDC circuit in seven stages. Since 32 different pulse trains are generated using DCO-DCDE circuits and eight different outputs are in FDC circuit, 256 pulse trains with different frequencies can be obtained. Finally by simultaneous use of DCO-DCDE-FDC circuits, various frequencies of pulse trains can be generated in the range of 1 to 10 MHz with good resolution.

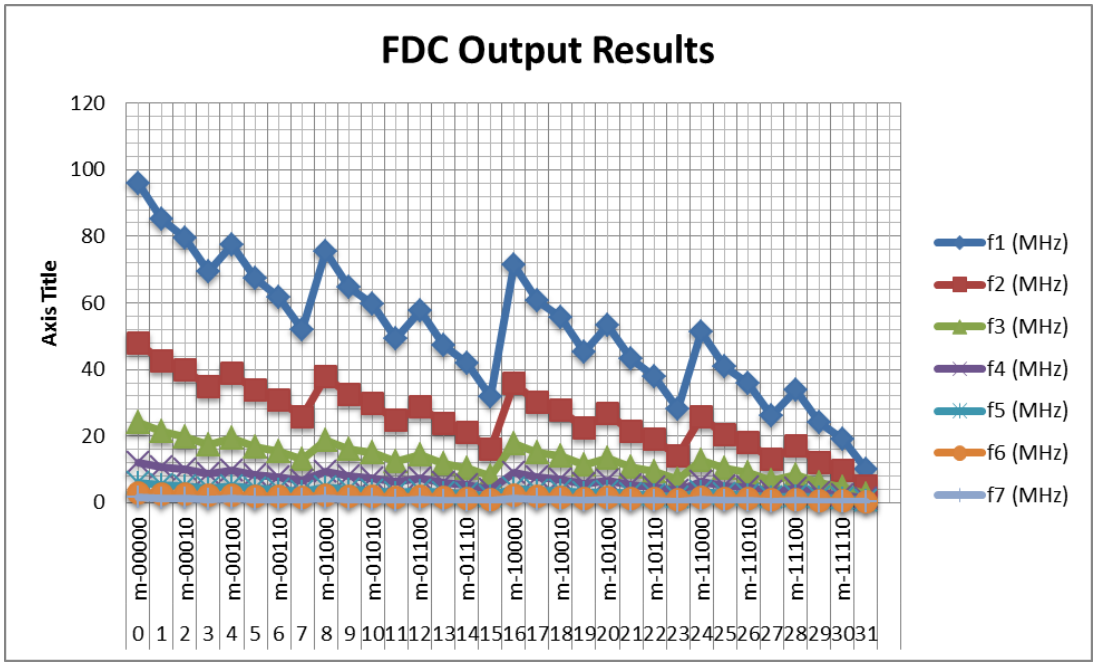


Figure 3.38 Simulation results of frequency down conversion (FDC) circuit.

Simulation results of FDC circuit with 00000 and 11010 as digital input vectors are shown in Figures 3.39 and 3.40, respectively. As can be observed from these figures, whenever FDC circuit receives pulse trains, the frequency of the signal is divided by two in seven different stages. In fact the circuit divides the frequency by the factor of 128 at the final step. The combination of DCO-DCDE and FDC circuits are connected to an 8X1 multiplexer for selection of generated frequencies for various applications. For example, by generating a pulse train with the frequency of 20 MHz, we can access the frequencies of 10, 5, 2.5, 1.25, 0.625, 0.3125 and 0.15625 MHz's. The combination of the enable circuit with DCO and three 5-bits DCDE circuits consume an average power of 1.98 and 3.9 mw at 20 and 190 MHz, respectively.

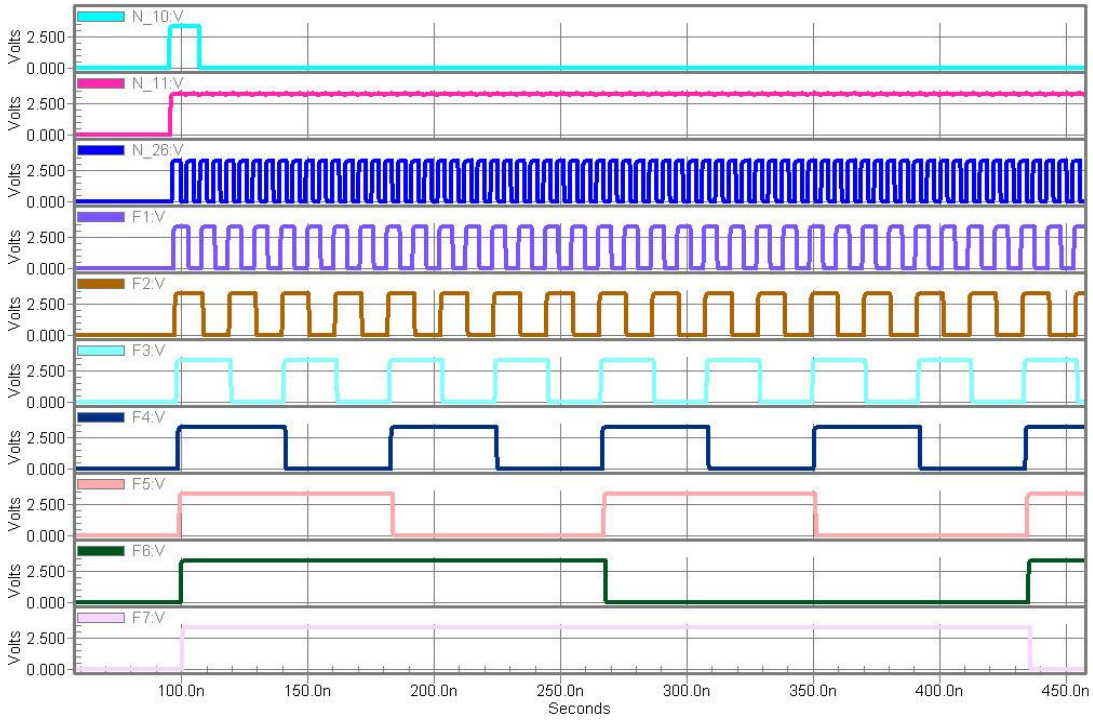


Figure 3.39 Simulation results of FDC with 00000 as digital input vector. The period and frequency is 5.25 ns and 190 MHz, respectively.

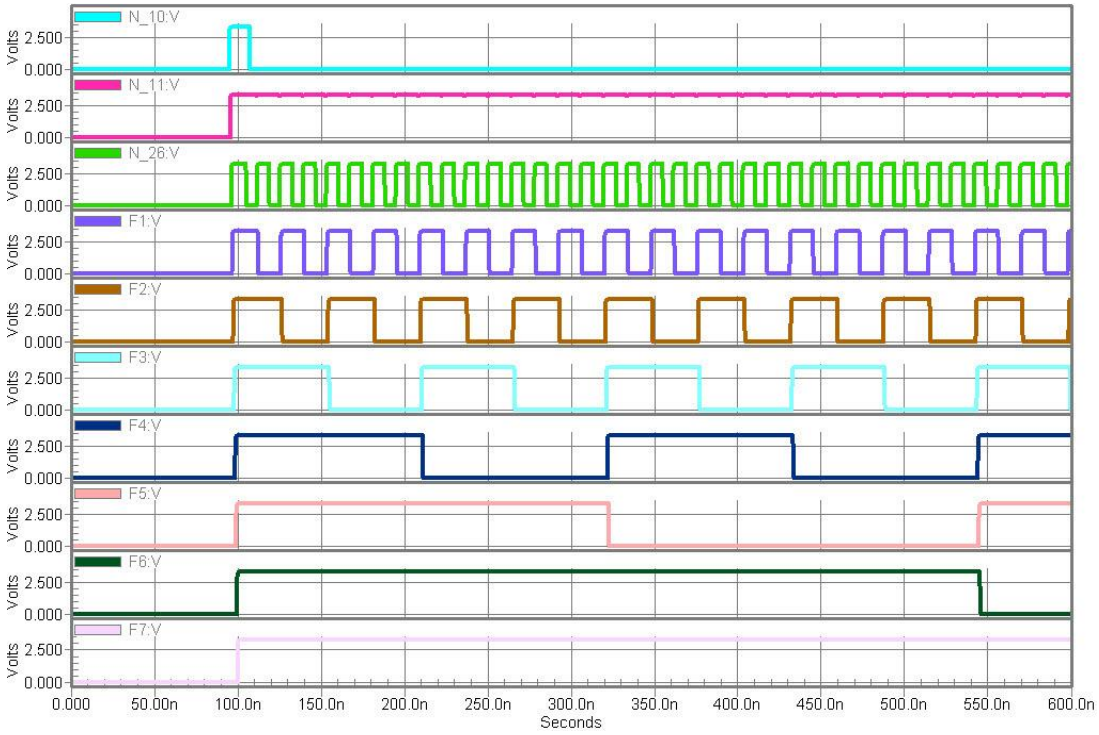


Figure 3.40 Simulation results of FDC with 11010 as digital input vector. The period and frequency is 14 ns and 71.5 MHz, respectively.

3.7 High Voltage Pulser Circuit Design

In previous sections, designing of low voltage (LV) blocks of our ASIC design is discussed. The firing system provides each of 16 CMUT elements with one driver circuit. As we mentioned in previous sections, CMUT elements are fired by single pulses with adjustable pulse widths and pulse trains with controllable frequencies according to their operating frequencies. Until this section, we explained how we generate firing signals for our ultrasound therapeutic applications but the magnitudes of those signals are 3.3 (LV) volts. In this section, converting of those low voltage signals to high voltage ones are discussed.

Modern CMOS technologies offer high voltage (>15V) extensions using special MOS transistors in VLSI chips for different kinds of applications. Low voltage (LV) circuitry can be used with high voltage (HV) blocks for digital control signals [64]. We designed different types of high voltage pulser and level shifter circuits via THKOX and HVTHKOX modules for our therapeutic applications. These circuits are discussed in this and next chapters. There are a lot of challenges in designing of high voltage circuits that should be considered carefully such as [82]-[90];

1) Low switching speed [82], [83]: Since high voltage transistors have large gate and drain capacitances, they have high switching delays. For instance, driving of high voltage pulser circuits with high frequency pulse trains can cause serious problems.

2) Large silicon area [82], [83]: For generation of high voltage signals, transistors with large widths are needed and hence high voltage pulser circuits occupy great area in the layout of the chips.

3) Static power consumption [78]-[64]: Since the transistors of the high voltage circuits have very large widths, these kinds of circuits have dramatic power consumptions. These high voltage circuits are not suitable for implantable battery powered applications at all. Hence, in most of the papers there is no information about the power consumptions.

4) Dynamic control signals [74], [88]: This factor makes the design of the high voltage circuit complex, especially for level shifter arrays.

5) High voltage capacitors [89], [90]: Although high voltage capacitors have not been used in our designs but if we decide to use them, we should consider that, they require large area to obtain reasonable capacitance values.

3.7.1 A 45-V High Voltage Pulser Circuit with THKOX Modules

In this section, the design of the high voltage pulser is explained. The main purpose of this section is to make a better view about the proposed design and the method of converting low voltage pulses to high voltage ones. Figure 3.41 shows the schematic of used high voltage pulser circuit which has been designed in HV 0.35 µm CMOS technology [91]. The outputs of these pulsers are connected to flip-chip bonding pads. Designed pulser is configured as a source-follower. One strong inverter including M7 and M8 transistors is connected to S_N and S_P nodes. Transmitted signals (single pulses or pulse trains) from driver part of the integrated circuit are delivered to S_P node of the pulser. When S_P transits from zero to

VDD (3.3 V), the S_N is changed in reverse mode, so the gate voltage of M_4 is decreased. The maximum allowed voltage across the source-gate of M_4, is determined by used CMOS process (18 V for our process). When M_4 is turned on, the output of this transistor begins to increase toward HVDD (45 V) and finally M_6 which is a source-follower transistor, follows that transition and the output of the pulser is increased to HVDD. Since the output of the inverter is in low state, M_3 and M_4 are off. In reverse mode, when the S_P falls to ground, a transition of zero to VDD over the node of S_N turns M_3 and M_4 on and hence the output of the pulser falls to ground.

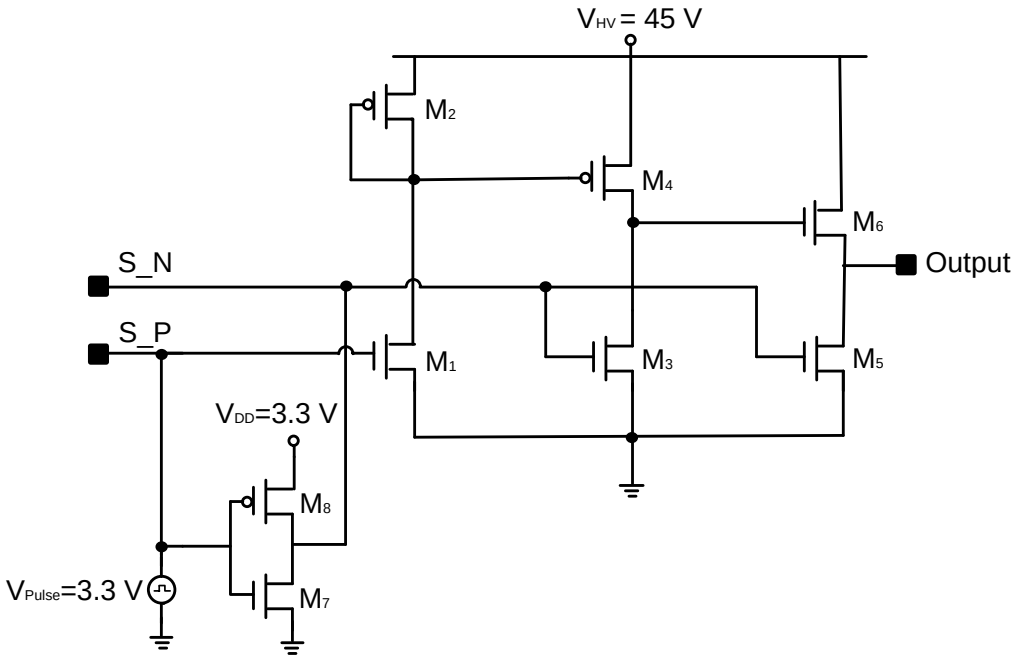


Figure 3.41 Schematic of the 45 V high voltage pulser with THKOX transistors.

The designs of high voltage pulser are optimized in such a way that designed circuit meets essential requirements for our application. Table 3.10 summarizes the selected (W/L) values of transistors of the designed 45 V pulser circuit.

Table 3.10 (W/L) values of the transistors for designed 45-V pulser.

Device	M1	M2	M3	M4
W (µm)	5	7	5	7
L (µm)	3	3	3	3
Number of Gates	6	6	6	6
Device	M5	M6	M7	M8
W (µm)	30	15	20	40
L (µm)	5	5	0.35	0.35
Number of Gates	15	12	1	1

Figure 3.42 shows the simulation results of high voltage pulser circuit which has been designed with THKOX (thick oxide) transistors. As can be observed, the output of the circuit is 45 V (HV) while its input is 3.3 V (LV).

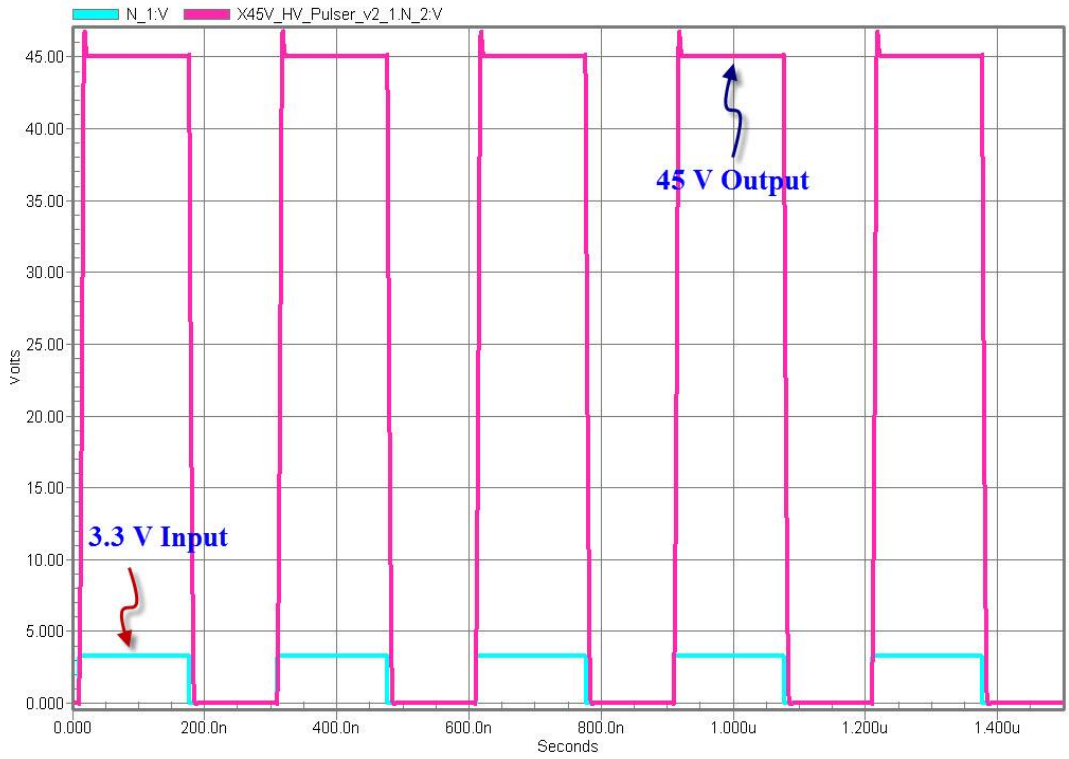


Figure 3.42 Simulation results of designed high voltage pulser circuit at 3.33 MHz.

Table 3.11 summarizes some of the important specifications of the 45 V pulser circuit such as the rise/fall time, slew rate, power dissipation and figure of merit. The values of these parameters have been presented for 15, 30 and 45 V as the output magnitudes. Designed circuit shows good results in comparison with previous works by others [67].

Table 3.11 Specifications of designed high voltage pulser for up to 45-V at 3.33 MHz (Driving a 2.5 pF capacitance load).

Parameter	Simulation Results	Units
Rise Time (10%-90%) @ V_{HV} = 15 V	3.85	ns
Fall Time (90%-10%) @ V_{HV} = 15 V	2.75	ns
Rise Time (10%-90%) @ V_{HV} = 30 V	4.45	ns
Fall Time (90%-10%) @ V_{HV} = 30 V	5.53	ns
Rise Time (10%-90%) @ V_{HV} = 45 V	5.13	ns
Fall Time (90%-10%) @ V_{HV} = 45 V	8.7	ns
Slew Rate (rising) @ V_{HV} = 30 V	2.33	V/µs
Slew Rate (falling) @ V_{HV} = 30 V	1.52	V/µs
Slew Rate (rising) @ V_{HV} = 45 V	3.9	V/µs
Slew Rate (falling) @ V_{HV} = 45 V	1.89	V/µs
P_{av} (dissipation) @ V_{HV} = 15 V	13.77	mw
P_{av} (dissipation) @ V_{HV} = 30 V	29.04	mw
P_{av} (dissipation) @ V_{HV} = 45 V	51.66	mw
Figure of Merit = D/(LV) @ V_{HV} = 15 V	1.08	ns/(µm.V)
Figure of Merit = D/(LV) @ V_{HV} = 30 V	0.66	ns/(µm.V)
Figure of Merit = D/(LV) @ V_{HV} = 45 V	0.51	ns/(µm.V)

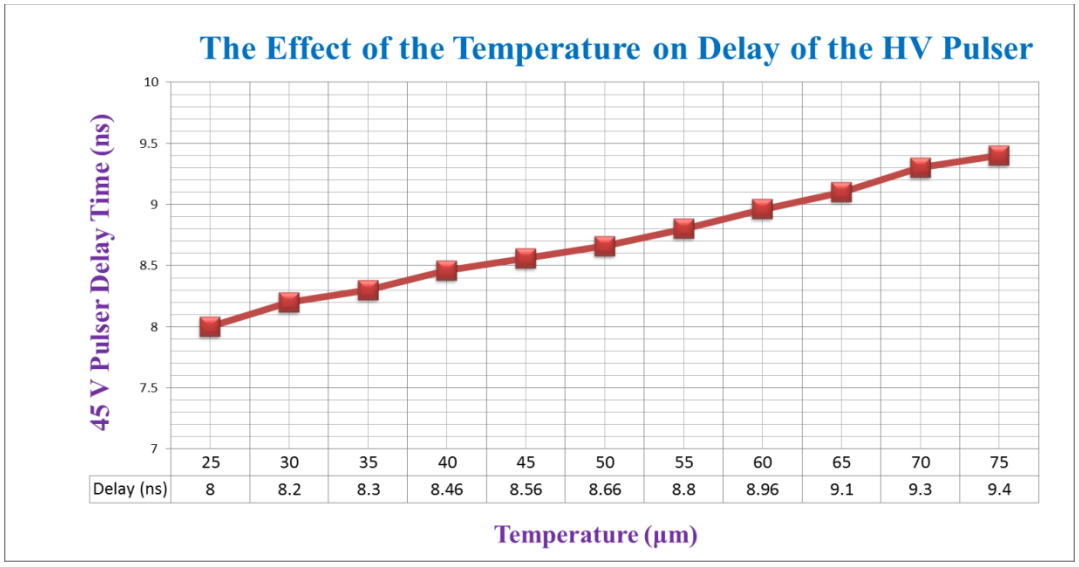


Figure 3.43 The effect of the temperature variations on delay of the high voltage pulser circuit.

Designed high voltage pulser circuit should be remained stable versus temperature variations. As shown in Figure 3.43, the total delay time of the circuit changes 1.4 ns from 25 to 75 ℃ which means 17.5% variation on delay time. Besides, the value of the figure of merit of the circuit changes from 0.51 to 0.59 ns/(µm.V).

Table 3.12 compares some specifications of designed high voltage circuit with previous works by others.

Table 3.12 Comparison of designed high voltage circuit with previous works by others.

Case	Prior Work	Year	Tech Type	Tech Node L(µm)	Delay D (ns)	Voltage V (V)	Figure of Merit=D/(LV) ns/(µm.V)
1	Declerq et al. [65]	1993	CMOS	2	80	50	0.8
2	Doutreloigne et al. [84]	1999	HV CMOS	0.7	15	20	1.07
3	Pan et al. [82]	2003	HV SOI	0.35	20	18	3.2
4	Park et al. [85]	2006	DMOS	1	50	160	0.31
5	Doutreloigne et al. [88]	2006	HV CMOS	0.7	2000	100	28.6
6	Serneels et al. [90]	2006	CMOS	0.13	0.08	2.4	0.26
7	Chebli et al. [89]	2007	HV CMOS	0.8	475	100	5.9
8	Rossberg et al. [86]	2007	SOI - CMOS	-	350	400	-
9	Buyle et al. [87]	2008	HV CMOS	0.35	2.5	25	0.29
10	Khorasani et al. [67]	2008	HV CMOS	0.8	-	300	-
11	Choi et al. [83]	2009	SOI	-	-	100	-
12	Khorasani et al. [64]	2009	HV CMOS	0.8	-	150	-
13	Moghe et al. [63]	2010	HV CMOS	0.35	2.4	10	0.69
14	Present work	2013	HV CMOS	0.35	5.8	15	1.08
15	Present work	2013	HV CMOS	0.35	7	30	0.66
16	Present work	2013	HV CMOS	0.35	8	45	0.51

Table 3.13 summarizes the disadvantages of the previous works by others in comparison with our designed high voltage circuit according to the case numbers of Table 3.12.

Table 3.13 Advantages of designed high voltage circuit in comparison with previous works by others.

Case	Disadvantages of previous works compared to our work
1	Large delay time, older CMOS technology and static power consumption
2	Large delay time with less output voltage, older CMOS technology, static power consumption and external dynamic controls
3	Large delay time with less output voltage, low speed and large area
4	Older CMOS technology, static power consumption and high voltage capacitors
5	Dramatic delay time, older CMOS technology and external dynamic controls
6	Much less output voltage and high voltage capacitors
7	Dramatic delay time, older CMOS technology and high voltage capacitors
8	Dramatic delay time and static power consumption
9	Less output voltage and static power consumption
10	Older CMOS technology and static power consumption
11	Low speed and large area
12	Older CMOS technology, low speed, large area and static power consumption
13	Less output voltage

3.8 DC Biasing of CMUT Elements

As we discussed in Chapter 1, by applying a DC voltage between top and bottom electrodes of a CMUT, the top plate of the CMUT is attracted toward the substrate because of an electrostatic force. Some flip-chip bonding pads on the IC are considered for DC bias voltage of the array. As can be observed from Figure 3.44, these pads are connected to the top electrode of the CMUT array with through-wafer interconnections. In fact, the top electrode of the CMUT array is common to all of the transducer elements and is used to DC bias of the CMUTs through the IC. The bottom electrodes of the CMUTs are connected to outputs of the high voltage pulsers one by one using flip-chip bonding pads. Resistor R and capacitor C are shared by all of the ultrasound transducers. Resistor R and capacitor C are in the range of several hundred kilo ohms and hundreds of nanofarads or more, respectively. The Resistor is used to isolate the voltage supply from a shorted element by limiting the current while the capacitor filters the noise of the high voltage supply and provides an AC ground for the CMUT.

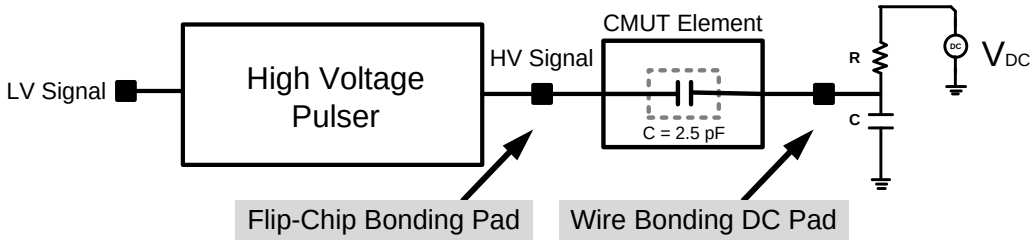


Figure 3.44 Schematic of the DC biasing of a CMUT element.

3.9 Constraints and Challenges of the HV 0.35 µm CMOS Technology

The array of the ultrasound transducers (PMUTs or CMUTs) consist of many elements for both of imaging and therapeutic applications. Each element is provided with one separated interface electronics including all of the required blocks. Hence, many blocks are placed in the same chip that should be routed precisely to the transducers. Consequently, the size of the chip will be dramatically large and these kinds of designs are too costly in fabrication step. In the design of the high voltage and low voltage electronics for therapeutic applications, reduction of the power consumption can be a major concern and should be kept as low as possible. The power dissipation of the beam-form generator could be improved significantly by using an advanced high voltage CMOS technology (e.g. HV CMOS 0.18 µm process) where lower voltages can be processed with better results. As discussed in this chapter, the widths of the single pulses or the frequencies of the pulse trains are adjusted according to the operational frequency of the used ultrasound transducers. These values should be very independent from the supply and temperature variations. Therefore, some useful techniques are used both in designing of the circuits and in connecting the sensitive elements to the bonding pads. Working with large values of voltages is very challenging because they occupy large die areas and have remarkable power consumptions. However, high voltage pulsers with less power consumptions can be achieved in a design environment that various types of transistor models are accessible. On the other hand, designing of high voltage pulsers with much more amplitudes can be implemented easily using DMOS transistors by HVTHKOX module but unfortunately this module is not available for XFAB MPW run.

3.10 Summary of the Chapter

In this chapter, the schematic, design and simulation results of the proposed ultrasound therapeutic IC for 4×4 CMUT array in HV 0.35 µm CMOS technology has been discussed. The designed beam-former includes different blocks (LV and HV) which are specifically designed to interface the capacitive micromachined ultrasound transducers (CMUTs). The design of the CMUT selection circuit, single pulse generator with adjustable pulse widths and pulse train generator with controlled frequencies has been explained. The widths of the single pulses or the frequencies of the pulse trains were designed flexible and controllable for driving of CMUT elements with different operating frequencies. The sensitivity of designed circuits to temperature and supply variations was evaluated and reasonable results were obtained. At final stage, signal generators (LV) were combined with high voltage pulsers to increase the magnitude of the signals. The outputs of the pulsers are connected to flip-chip bonding pads and then top electrode of the transducers. Designed pulsers have been simulated in various temperatures and some specifications of the circuit were compared with similar prior works by other. Next chapter describes the layout of the ultrasound therapeutic IC for 4×4 CMUT array in HV 0.35 µm CMOS technology with important and useful considerations. The placement and routing process of the LV and HV blocks in the same chip and making them suitable to be bonded to CMUT elements using flip-chip bonding techniques are very important in these kinds of ICs.

CHAPTER 4

THE LAYOUT OF THE ULTRASOUND THERAPEUTIC IC FOR 4X4 CMUT ARRAY IN HV 0.35 µm CMOS TECHNOLOGY

In this chapter, the layouts of the different parts of the IC with their important considerations are explained. The schematic, design and simulation results of the proposed ultrasound therapeutic IC for 4×4 CMUT array in HV 0.35 µm CMOS process has been explained in previous chapter. The new combination of single pulse and pulse train generators at the same IC with the ability of adjusting their specifications for driving ultrasound transducers with different operating frequencies have been developed and processed using this high voltage technology. However, in the design of the IC especially high voltage pulsers, better performance can be achieved using an advanced CMOS technology for a typical ultrasound beam-form generator.

Section 4.1 explains the layout overview of the ultrasound therapeutic IC for 4×4 CMUT array by introducing the estimated shape of the final chip. Section 4.2 describes the layout of the driver (LV) part of the chip including the 8-bit shift register, 8-bit comparator, one-shot circuit, enable circuit of the digitally controlled oscillator (DCO), DCO with 5-bits digitally controlled delay element (DCDE) and frequency down conversion (FDC) circuit. Each CMUT element is provided by one of the proposed driver circuitry. Section 4.3 presents the placement and routing process of main blocks of the driver electronics. Section 4.4 and 4.5 explain the final layout of the low voltage (LV) and high voltage parts of the chip, respectively. Section 4.6 presents the configuration of the driver blocks of the IC in a 4×4 array. Section 4.7 describes the integration of LV and HV of the chip and section 4.8 presents the final core of the IC. Section 4.9 describes different used wire bonding pads with their additional cells. Section 4.10 demonstrates the final custom designed chip for 4X4 CMUT ultrasound therapeutic applications. Finally, section 4.11 summarizes this chapter.

4.1 The Layout Overview of the Ultrasound Therapeutic IC for 4X4 CMUT Array

In this section, the layout of the designed integrated circuit for 4X4 CMUT array is explained. According to Figure 4.1, the layout of the final integrated circuit (IC) has been divided into two main parts. The left side of the layout consists of CMUT driver circuits with low voltage (LV) blocks that should be drawn, routed and connected precisely and the right side includes high voltage (HV) pulsers and flip-chip bonding pads that are supposed to be connected to CMUT elements one by one. In driver part of the integrated circuit, there

are 16 separated blocks which have been considered for 16 high voltage pulser circuits. Since we have 16 CMUT elements in our final design, 16 numbers of complete blocks including LV, HV and flip-chip bonding pads should be placed in final integrated circuit. The layout of the LV and HV blocks provide each of 16 CMUT elements with an 8-bit shift register, an 8-bit comparator, an one-shot circuit, a digitally controlled oscillator with 5-bits digitally controlled delay elements, a frequency down conversion circuit, 45 V pulser circuit with thick oxide transistors and combinational logics that will be discussed in following sections in depth. Placement and routing of these blocks in as small as possible area, demands a lot of considerations.

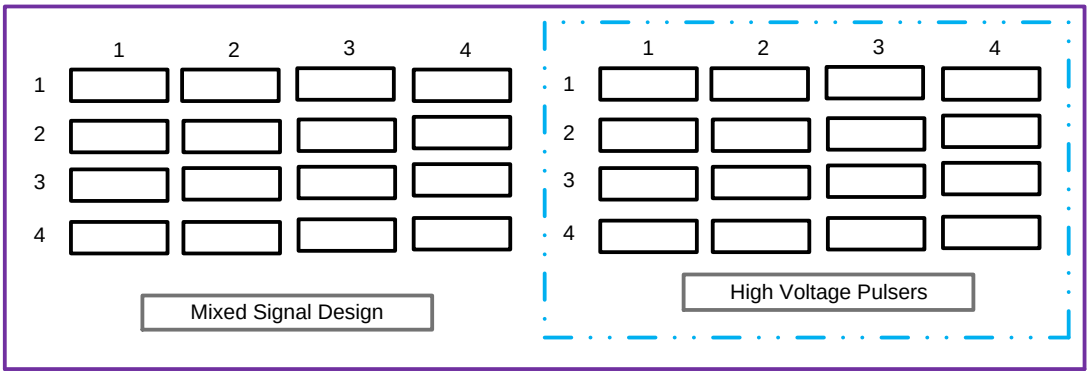


Figure 4.1 Layout structure of the ultrasound therapeutic IC for 4X4 CMUT array.

As we mentioned before our integrated circuit has been designed in XH035 CMOS technology and our final process for fabrication includes 20 mask layers and 23 process layers. Four different modules including MOS, CAPPOLY, METAL4 and THKOX have been used in our IC. In our process we used four kinds of metals. MET1 and MET2 layers are used for internal connections of 16 main LV blocks. For connecting VDD and GND lines together we decided to use MET3 layer. Also MET3 layer can be used for other connections but we should be careful about VDD and GND lines. Finally, we decided to use MET4 layer for the connections of the two major parts of the IC and other connections in HV regions. Since there are a lot of blocks in the chips like ours we should consider a lot of points, hence these kinds of designs are dramatically time consuming. DRC and LVS should be done for each step to make sure that we have drowned the same circuit as we did for schematic part.

4.2 Layout of the Driver part (LV) of the Chip

In this section, the layout of the designed driver circuitry including an 8-bit shift register, an 8-bit comparator, a one-shot circuit, a digitally controlled oscillator (DCO) with 5-bits digitally controlled delay elements (DCDE) and a frequency down conversion (FDC) circuit with some essential considerations is explained.

4.2.1 Layout of the 8-bit Shift Register

As we discussed in previous chapter, for selection of a CMUT element we need a shift register and a comparator. The 8-bits shift register design as one of the main blocks in integrated circuit design for CMUT elements in therapeutic applications with its simulation results has been explained too.

The shift registers for each row of 4 ultrasound transducer elements are connected in series. Four input signals from the FPGA, load the 4 rows of shift registers in parallel and separately. The FPGA is supposed to generate a two-phase clock frequency for shift registers, the information about the count rate of the global counter for comparators and the input delay information for the IC's shift registers. The shift registers have been simulated in 100 MHz, 200 MHz and even high clock frequencies. Figure 4.2 shows the layout of the 1-bit shift register. This cell consists of three inverters, one two-input NAND and two transmission gates (T-Gate). All these cells were routed according to our design. The die area of the 1-bit shift register is 697.84 μm^2 (14.3 µm x 48.8 µm).

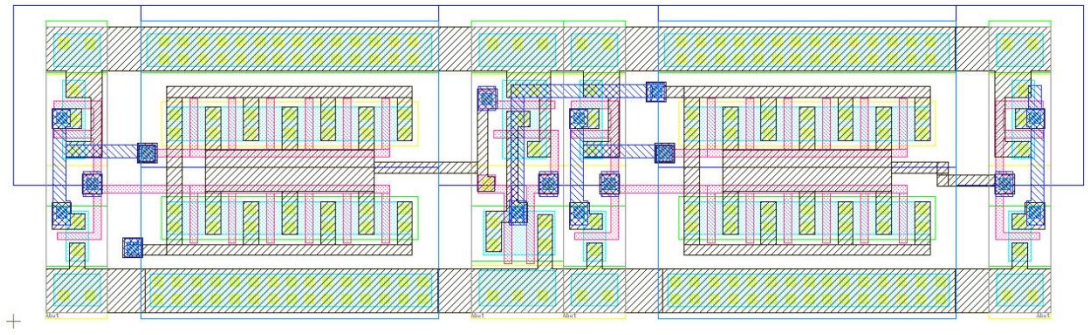


Figure 4.2 Layout of the 1-bit shift register.

Since eight numbers of 1-bit shift registers are connected serially together, we decided to put 1-bit shift registers one after another in the same line. The routing process of these cells was accomplished by "METAL1" and "METAL2" layers. At the final step, the "GND" and "VDD" lines of each 1-bit shift register were connected to another one, respectively. Figure 4.3 shows two numbers of 1-bit shift register which has been placed at the same line and routed together via "METAL1" and "METAL2" layers.

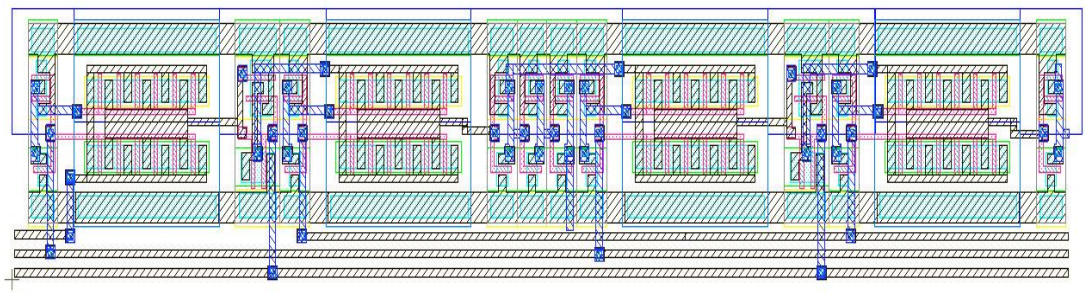


Figure 4.3 Layout of the 2-bit shift registers.

Figure 4.4 shows the final layout of the 8-bit shift register which consists of eight numbers of 1-bit shift registers. As it can be seen, these cells are connected serially one after another. In this cell, eight external lines have been considered for 8-bit comparator connections. These lines were drawn downward, because we will put the 8-bit comparator in down side of the 8-bit shift register in final layout of the IC. The DRC (Design Check Rule), layout extraction and LVS (Layout VS Schematic) was successful for this cell. The die area of the 8-bit shift register is 7352.05 μm^2 (17.75 µm x 414.2 µm).

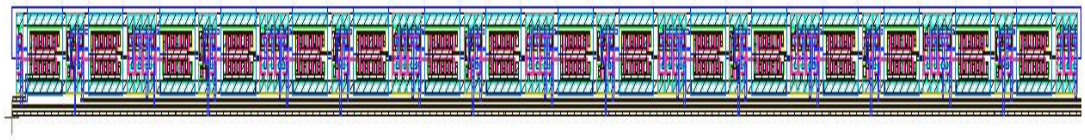


Figure 4.4 Layout of the 8-bit shift register.

4.2.2 Layout of the 8-bit Comparator

As discussed in previous chapter, in each beam-forming circuit for each CMUT element, when the value stored in the 8-bit shift register equals the 8-bit global Gray-code counter provided by the FPGA, the comparator's output goes high. We need an 8-bit comparator for each CMUT element to compare the information of the input delay (provided by 8-bit shift register) and Gray-counter codes (provided by FPGA), so that we can fire any CMUT element whenever requested.

As we explained in previous chapter, Pseudo-NMOS comparator has been used as our data comparing circuit. These kinds of comparators are fast and get small area in the layout of the chip. Figure 4.5 shows the layout of the 1-bit comparator. The layout of the 1-bit comparator consists of four NMOS transistors with two CMOS inverter gates. The die area of the 1-bit comparator is 265.265 μm^2 (14.3 µm x 18.55 µm).

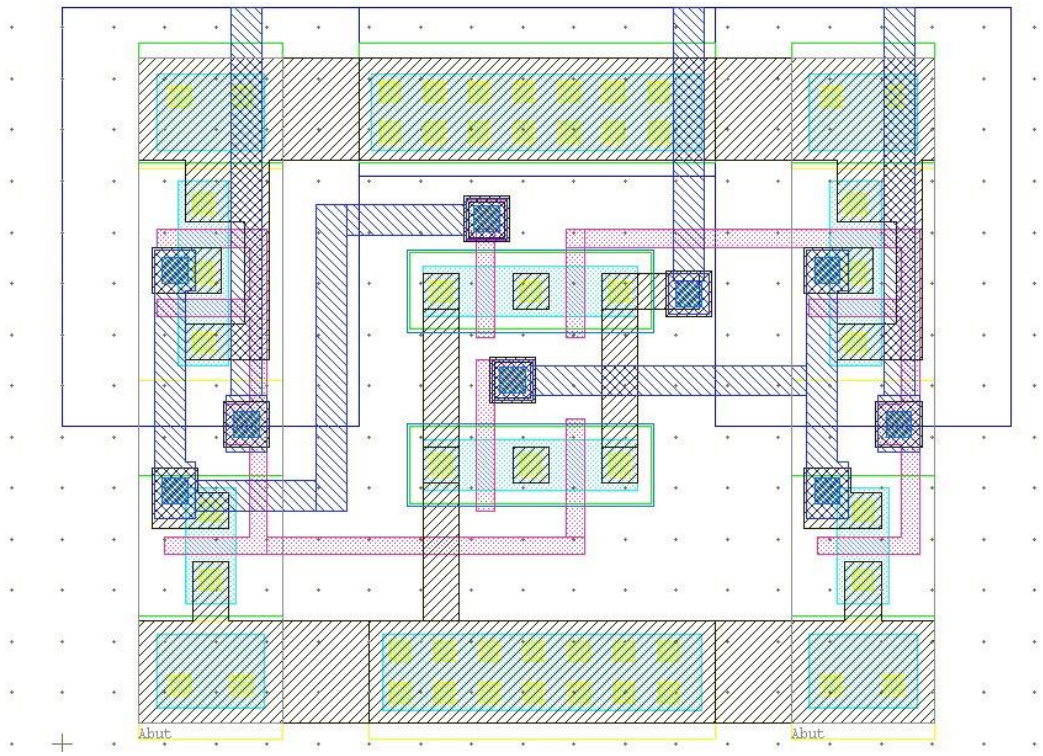


Figure 4.5 Layout of the 1-bit comparator.

Eight numbers of 1-bit comparators are connected together one after another in the same line. The routing process of these cells was accomplished by “METAL1” and “METAL2”. At the final step, the “GND” and “VDD” lines of each 1-bit comparator were connected to the next one, respectively. Figure 4.6 shows two numbers of the 1-bit comparator which is placed at the same line and routed together via “METAL1” and “METAL2”.

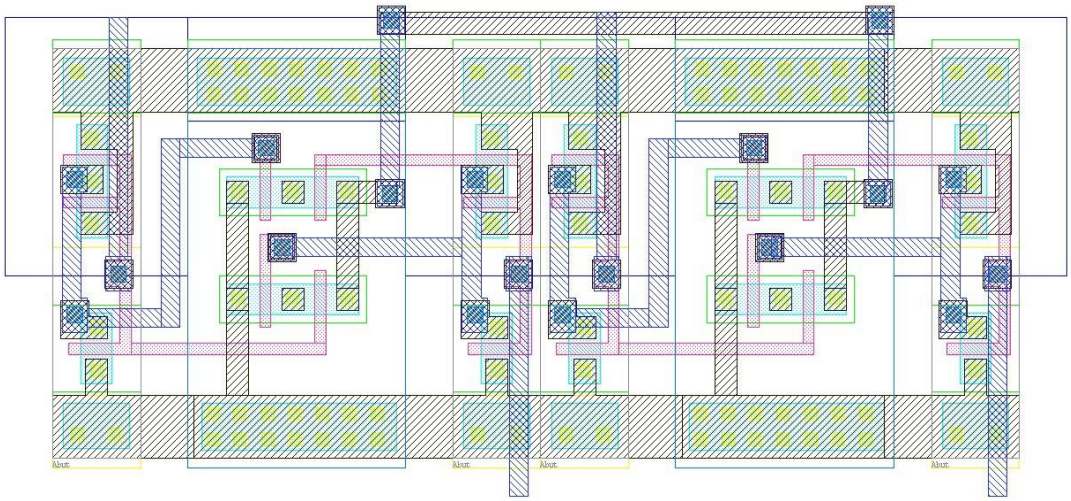


Figure 4.6 Layout of the 2-bit comparator.

Figure 4.7 shows the final view of the 8-bit comparator cell which consists of eight numbers of 1-bit comparators. As it can be seen, these cells are connected together in the same line. In this cell, eight external lines were supposed for 8-bit shift register connections from top side. These lines were drawn upward, because we will put the 8-bit comparator in down side of the 8-bit shift register. At the same time, eight external lines were supposed for 8-bit global lines at the bottom side of the 8-bit comparator which will be supported by FPGA externally. The DRC (Design Check Rule), layout extraction and LVS (Layout VS Schematic) was successful for this cell. The die area of the 8-bit comparator is 3419.36 μm^2 (24.85 µm x 137.6 µm).

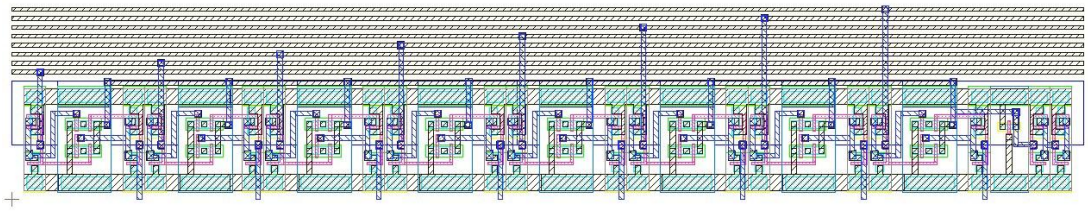


Figure 4.7 Layout of the 8-bit comparator.

4.2.3 Layout of the Demultiplexer

We can fire CMUT elements with single pulses or pulse trains. Each of these methods has their own applications. For example in some of the simple 3D imaging or therapeutic applications, single pulses can be preferred but in Color Doppler Imaging or other kinds of therapeutic applications pulse train generation method can be suitable. As we discussed in previous chapter, we preferred to combine these two applications together and design an integrated circuit which can support these applications simultaneously.

Until this step, we have the same process of firing CMUT elements. We need to choose a CMUT element at any time needed. After this step, the integrated circuit will be divided into two main parts, one for generating single pulses via One-Shot circuits with adjustable pulse width and another for generating pulse trains with arbitrary periods and frequencies. If the selection signal of the demultiplexer is zero, single pulse application will be selected and if that line is in high state, pulse trains are fired CMUT elements. Figure 4.8 shows the layout of the 2X1 demultiplexer circuit. DRC (Design Check Rule), layout extraction and LVS (Layout VS Schematic) was successful for this cell. The die area of the 2X1 demultiplexer is 263.12 μm^2 (14.3 µm x 18.4 µm).

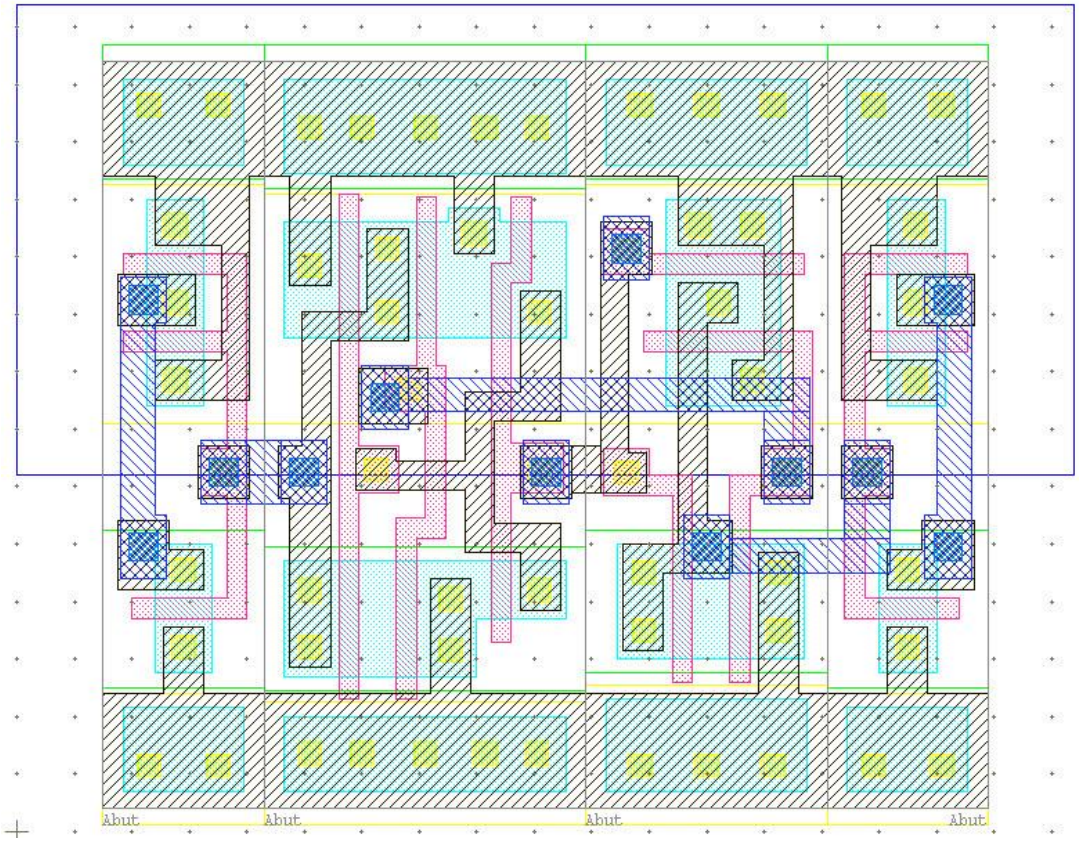


Figure 4.8 Layout of the 2X1 demultiplexer.

4.2.4 Layout of the Final One-Shot Circuit

If zero is selected for selection port of the 2X1 demultiplexer, the output port of the 8-bit comparator will be transferred to one-shot circuit. Variable pulse widths should be provided for different operating frequencies of ultrasound transducers. By varying the pulse width, transducer's operating frequency can be matched and adopted with multiple ultrasonic transducers. The one-shot circuits drive the high voltage pulsers and thus dictate the width of the pulse applied to the ultrasound transducer element.

The width of the output single pulse or pulse trains can be controlled by adjusting the current of a capacitor (in the range of pF) in a one-shot circuit. The value of this capacitor in our designs is 2 pF. The layout of the one-shot circuit should have a global port for current injection with external source using wide metal layers.

The one-shot circuit consists of some digital gates. As we explained in previous chapter, one of the inverters of one-shot circuit should be designed especially, so that we can adjust the pulse width using the delay of that inverter, the capacitor and the current flowing through a PMOS transistor.

Figure 4.9 shows the layout of the left side of the one-shot circuit which consists of two inverters, two inputs NAND gate and one special inverter.

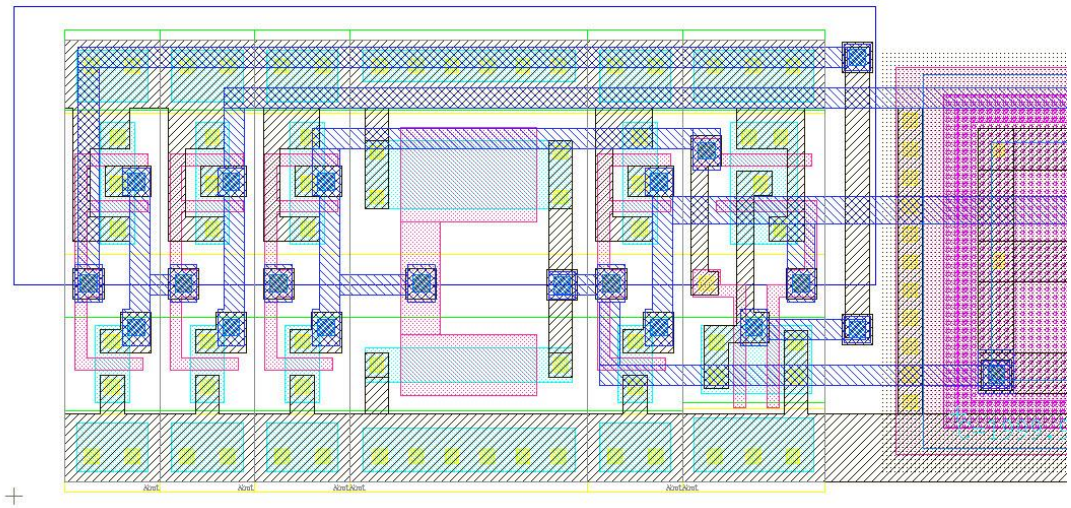


Figure 4.9 The layout of the left side of the One-Shot circuit.

Figure 4.10 shows the layout of the right side of the one-shot circuit which consists of a PMOS transistor for external current injection. Since current line of One-Shot circuit carries currents up to 80 µA, we decided to widen the METAL1 and METAL2 lines of current injection port. Besides, widening of these lines reduces their resistances too.

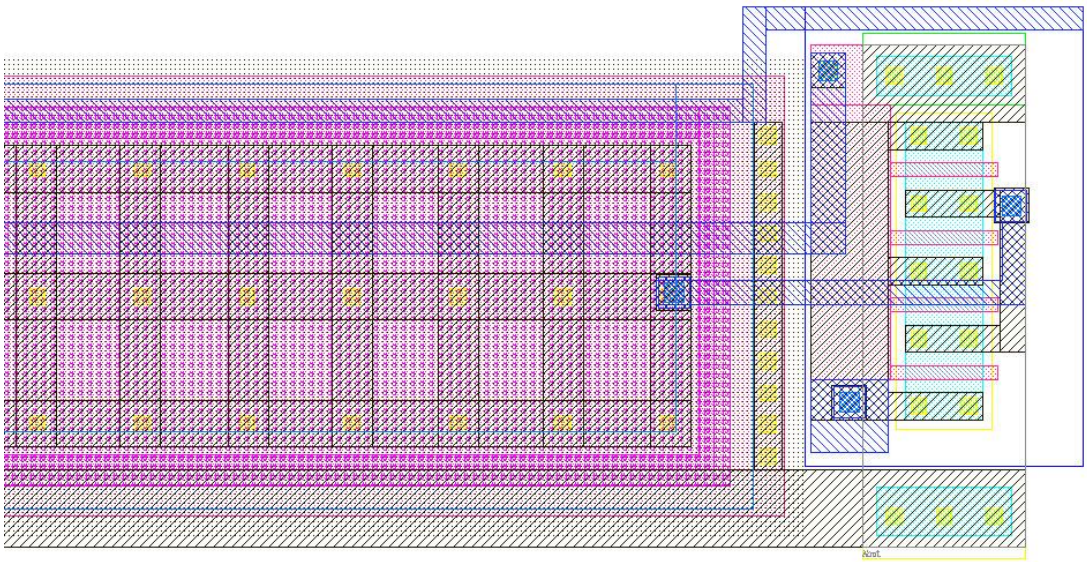


Figure 4.10 The layout of the right side of the One-Shot circuit.

For 2 pF capacitance, we designed a "9 µm by 262 µm" POLY1 – POLY2 structure. We could obtain the capacitance of 1.999913 pF by selecting those dimensions. At the output of the layout of the one-shot, one buffer was used for driving large capacitive loads. Figure 4.11 shows the final layout of the one-shot. DRC (Design Check Rule), layout extraction

and LVS (Layout VS Schematic) was successful for this cell. The die area of the one-shot circuit is 4251.39 μm^2 (14.3 µm x 297.3 µm).

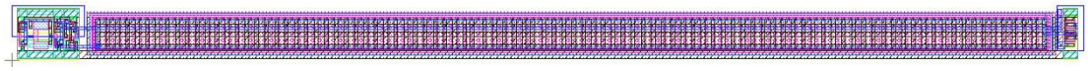


Figure 4.11 Final layout of the one-Shot circuit.

4.2.5 Layout of the Enable Circuit for Digitally Controlled Oscillator (DCO)

In previous chapter, we discussed that if we want to have a pulse train instead of single pulse at the input of the pulser circuit in specific duration of time or in an unlimited interval, we should control the input of the DCO-DCDE using an enable circuit. If we make the selection port of the 2X1 demultiplexer high, the output port of the 8-bit comparator will be transferred to enable circuit. Since the data port of the enable circuit is connected to VDD, the output of the enable circuit will raise to VDD whenever the circuit senses zero to one transition (rise edge) on its CLK port. RN port controls the time duration for pulse train generation.

Figure 4.12 shows the layout of the enable circuit. DRC (Design Check Rule), layout extraction and LVS (Layout VS Schematic) was successful for this cell. The die area of the enable circuit layout is 383.24 μm^2 (14.3 µm x 26.8 µm).

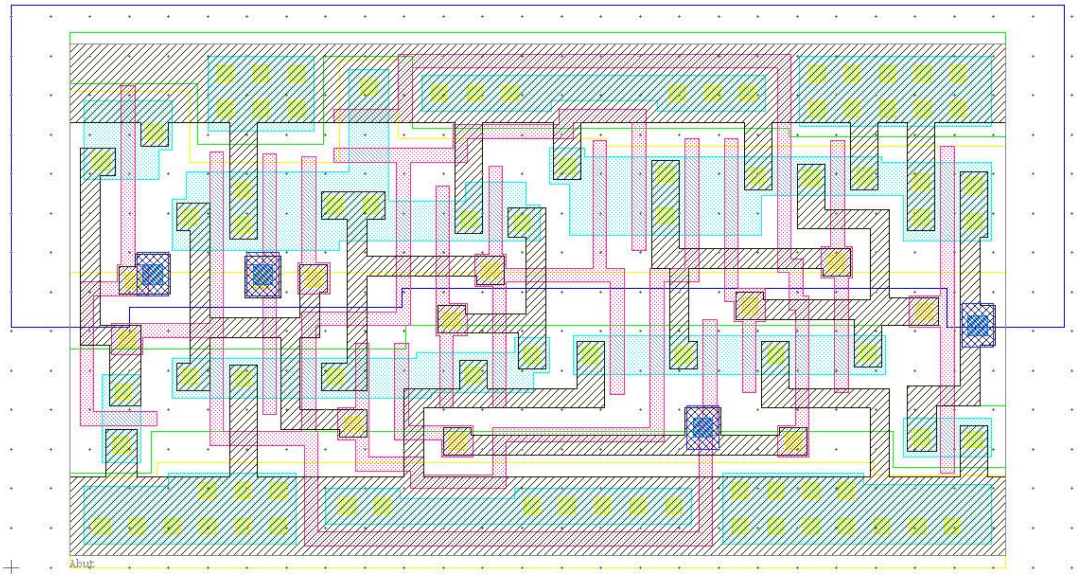


Figure 4.12 Layout of the enable circuit.

4.2.6 Layout of the Digitally Controlled Oscillator (DCO)

The layout of the DCO-DCDE circuit consists of two parts; one for DCO and another for delay elements. Figure 4.13 shows the layout of the digitally controlled oscillator (DCO) without DCDE elements. DRC (Design Check Rule), layout extraction and LVS (Layout VS Schematic) was successful for this cell. The die area of the DCO circuit without DCDE is 303.16 μm^2 (14.3 µm x 21.2 µm).

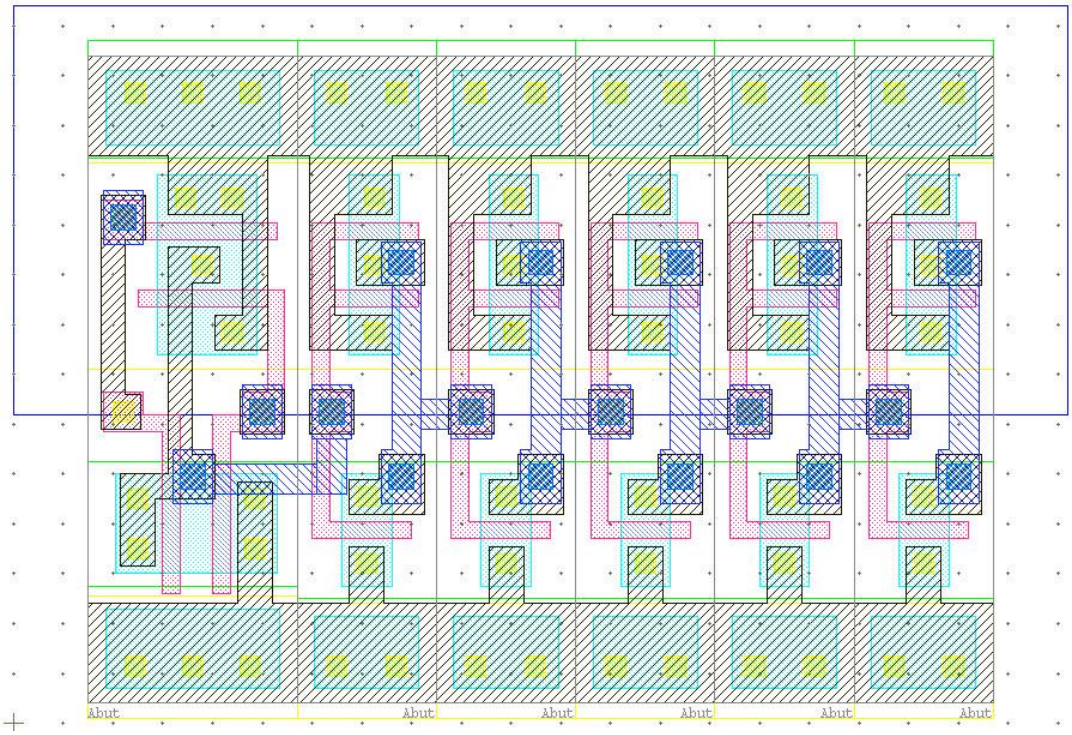


Figure 4.13 The layout of the DCO circuit without DCDE.

4.2.7 Layout of the 5-bits Digitally Controlled Delay Element (DCDE)

Figure 4.14 shows the layout of the 5-bits digitally controlled delay element (DCDE) without DCO circuit. The layout of this circuit has five global connections. In final layout of the chip, all 5-bits controlling lines of DCDEs are connected together one by one. DRC (Design Check Rule), layout extraction and LVS (Layout VS Schematic) was successful for this cell. The die area of the 5-bits DCDE is 985.985 μm^2 (14.3 µm x 68.95 µm).

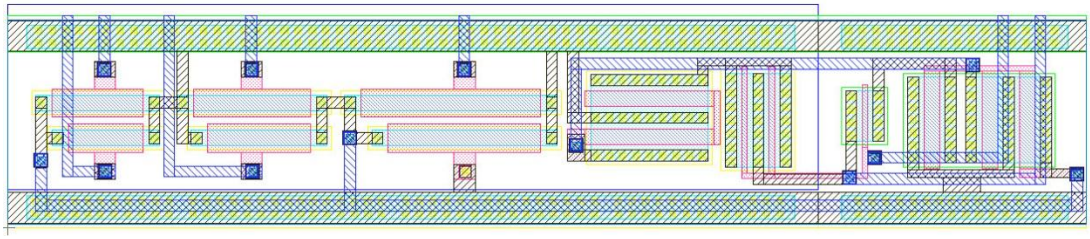


Figure 4.14 Layout of the 5-bits DCDE circuit without DCO.

4.2.8 Layout of the Final DCO with 5-bits DCDE

As shown in Figure 4.15, we placed the layouts of the DCO and DCDE at the same line. As it can be seen from this figure, digital control lines have been connected together via METAL1 and METAL2. DRC (Design Check Rule), layout extraction and LVS (Layout VS Schematic) was successful for this cell. The die area of the DCO-DCDE circuit is 5461.7975 μm^2 (23.95 µm x 228.05 µm).

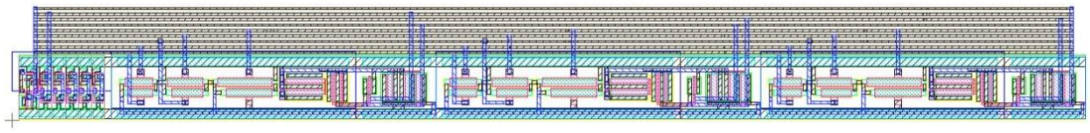


Figure 4.15 Layout of DCO with 5-bits DCDE.

4.2.9 Layout of the Frequency down Conversion (FDC) Circuit

Figure 4.16 shows the layout of one stage of frequency down conversion (FDC) circuit. DRC (Design Check Rule), layout extraction and LVS (Layout VS Schematic) was successful for this cell. The die area of one stage of FDC circuit is 403.26 μm^2 (14.3 µm x 28.2 µm).

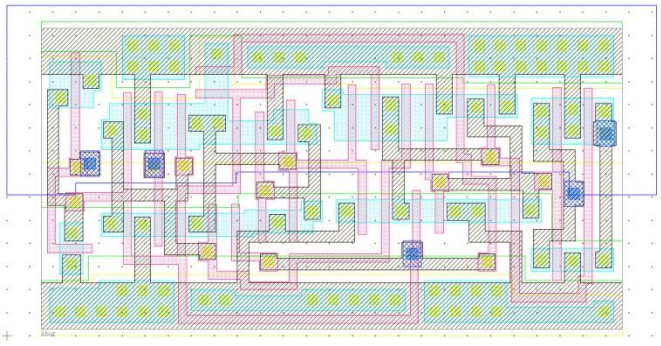


Figure 4.16 Layout of one stage of frequency Down Conversion (FDC) circuit.

Since seven numbers of FDC circuits are connected together, we decided to put seven stages of the FDCs next to each other in the same line. The routing process of these cells was accomplished by “METAL1” and “METAL2”. At the final step, the “GND” and “VDD” lines of each FDC were connected to another one, respectively. Figure 4.17 shows the layout of two numbers of FDC that has been placed at the same line and routed together via “METAL1” and “METAL2”. DRC (Design Check Rule), layout extraction and LVS (Layout VS Schematic) was successful for this cell. The die area of two routed FDCs is 763.62 μm^2 (14.3 µm x 53.4 µm).

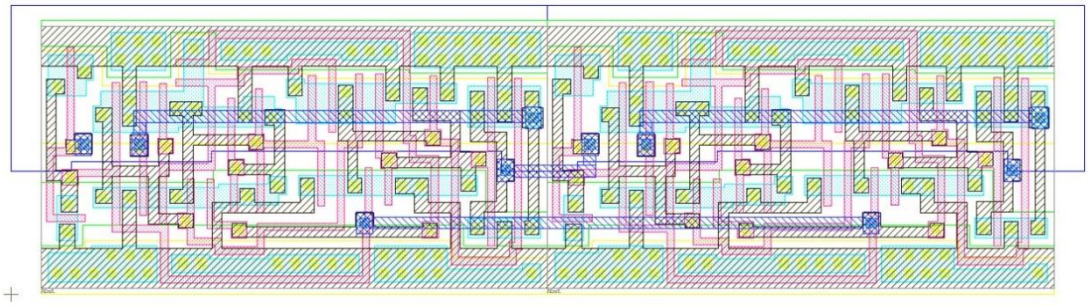


Figure 4.17 Layout of two routed FDC circuits.

Figure 4.18 shows the final layout of the frequency down conversion (FDC) circuit which consists of seven numbers of edged trigged DFFs. In this cell, eight external lines are considered for the layout of the DCO-DCDE block. These lines were drawn downward, because we put the layout of the DCO-DCDE adjacent to the FDC and they are connected via METAL1 and METAL2. The DRC (Design Check Rule), layout extraction and LVS (Layout VS Schematic) was successful for this cell. The die area of the final FDC circuit is 2565.42 μm^2 (14.3 µm x 179.4 µm).

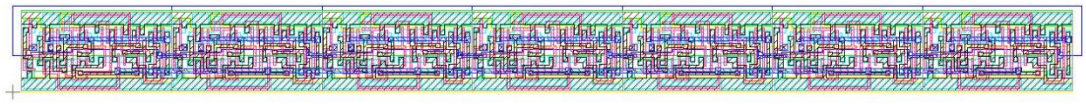


Figure 4.18 Final layout of FDC circuit.

4.2.10 Layout of the 8X1 Multiplexer

From the combination of DCO-DCDE and FDC circuits, we can get eight different frequencies at any 5-bits digital input vector of DCDE circuit. It means that we can get 256 different kinds of pulse trains with different frequencies. Selection of these different signals is done using 5-bits DCDE circuits and a multiplexer with eight input ports. This multiplexer has three input signal selection lines for selecting different input pins, hence we

need to select a code for DCDE and a 3-bits digital code for 8X1 multiplexer. The layout of this multiplexer is shown in Figure 4.19. The DRC (Design Check Rule), layout extraction and LVS (Layout VS Schematic) was successful for this cell. The die area of the 8X1 multiplexer is 683.54 μm^2 (14.3 µm x 47.8 µm).

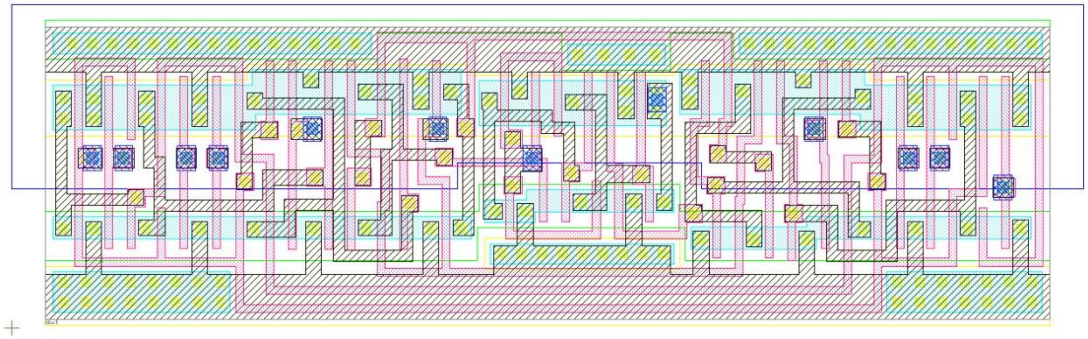


Figure 4.19 Layout of the 8X1 multiplexer.

4.2.11 Layout of the 2X1 Multiplexer

From 8-bits shift register until this section, two kinds of signals can be obtained, single one from one-shot with adjustable pulse width and the second one which is pulse train with arbitrary frequency from DCO-DCDE-FDC circuit combinations. These signals are supposed to drive the input of the high voltage pulsers. The selection of these signals can be done using a 2X1 multiplexer for each CMUT element. One selection port controls this process by changing it to one or zero. The layout of this 2X1 multiplexer is shown in Figure 4.20. The DRC (Design Check Rule), layout extraction and LVS (Layout VS Schematic) was successful for this cell. The die area of the 2X1 multiplexer is 183.04 μm^2 (14.3 µm x 12.8 µm).

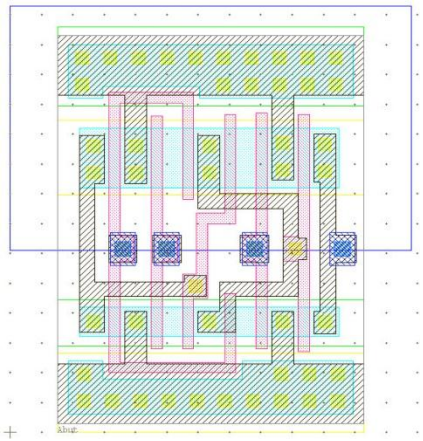


Figure 4.20 Layout of the 2X1 multiplexer.

4.3 Placement and Routing Process between Main Blocks of the Driver Part of the Chip

Placement is an essential step in integrated circuit design. Placement is the process of physical design flow for selecting exact locations for various blocks within the chip's core area. Placement of the main blocks of the IC affects the performance of the chip and if it has not been performed correctly, the chip cannot be adoptable for manufacturing. Consequently, a designer should perform the placement process by optimizing the number of blocks to ensure that the designed integrated circuit meets its performance demands. A typical process of placement of objectives includes total length of wires, timing, congestion and power.

In previous sections, the layout of the all required blocks for driver part of the chip was explained. In this section, the placement of those blocks and routing process between them are discussed. In placement and routing process of our designed chip a lot of considerations should be attended. We tried to place all of the main blocks together in a rectangular shape. All of the empty spaces in this shape were filled by main blocks by considering their sizes. In following sections, the placement and routing process has been discussed in detail.

4.3.1 Placement and Routing of 8-bit Shift register and 8-bit Comparator

Figure 4.21 shows the 8-bit shift register and 8-bit comparator that have been routed together. It can be seen that, these two blocks have been connected via METAL1 and METAL2. As we mentioned before, the top block is 8-bit shift register and the bottom one is 8-bit comparator. Eight lines of each block are connected to the second one. 8-bit shift register receives the delay information from FPGA and delivers it to the 8-bit comparator in parallel mode. Eight lines of 8-bit comparator have been considered for global gray code from down side of the layout.

Figure 4.21 Routed 8-bit shift register and 8-bit comparator.

4.3.2 Placement and Routing of 8-bit Shift register, 8-bit Comparator and DEMU1X2

As marked in Figure 4.22, we decided to put DEMU2X1 in front of the 8-bit comparator because it is connected directly to the output of that cell. The essential connections between these three cells were accomplished precisely.

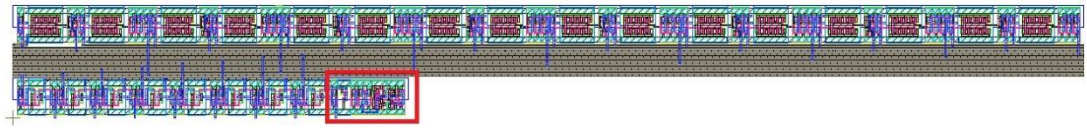


Figure 4.22 Routed 8-bit shift register, 8-bit comparator and DEMU2X1.

4.3.3 Placement and Routing of One-Shot

First output of the demultiplexer has been dedicated for single pulse generation mode and connected to the one-shot circuit which is one of the most important blocks in our design. According to Figure 4.23, we placed the layout of the one-shot circuit at front of the DEMU2X1 and under the 8-bit shift register. The routing process has been done between main cells. One wide METAL1 line was considered for global current injection from an external current source.

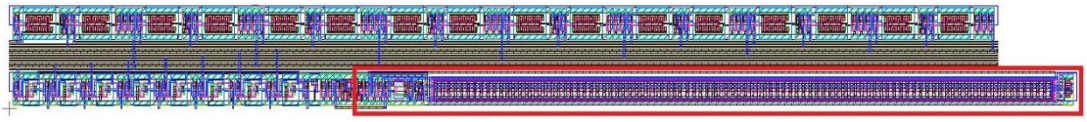


Figure 4.23 Placement and routing of one-Shot.

4.3.4 Placement and Routing of Enable Circuit

Placement and routing of single pulse generation mode was completed in previous section and it can be connected to high voltage pulser circuit. In following sections the placement and routing process of pulse train generation mode is explained. Enable circuit as first block of this section must be connected to the DEMU2X1. As shown and marked in Figure 4.24, enable circuit has been placed in front of the 8-bit shift register because there is an empty place there and we want to occupy less chip area. The routing process was accomplished via METAL1 and METAL2.

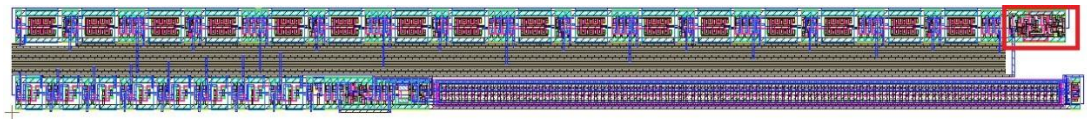


Figure 4.24 Placement and routing of enable circuit.

4.3.5 Placement and Routing of FDC and MU8X1

Placement and routing of frequency down conversion (FDC) and 8X1 multiplexer is shown in Figure 4.25 in which two cells have been placed at the same line. These cells are supposed to be placed at the third floor of first major block. The routing process was accomplished via METAL1 and METAL2. The DRC (Design Check Rule), layout extraction and LVS (Layout VS Schematic) was successful for this cell. The die area of FDC-MU8X1 cell is 5111.76 μm^2 (22.8 µm x 224.2 µm).

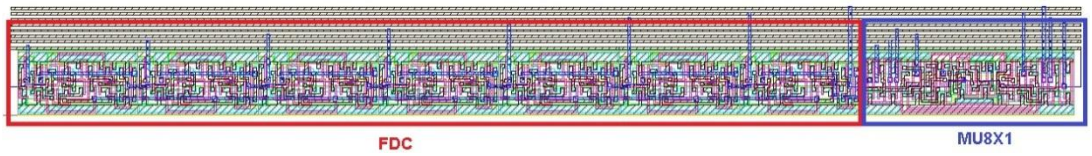


Figure 4.25 Placements and Routing of FDC and MU8X1.

4.3.6 Placement and Routing of DCO-DCDE and FDC-MU8X1

As shown in Figure 4.26, we placed the combinations of DCO-DCDE and FDC-MU8X1 at the same line. These cells are supposed to be placed at the third row of the first main block. The DRC (Design Check Rule), layout extraction and LVS (Layout VS Schematic) was successful for this cell. The die area of the DCO-DCDE-FDC-MU8X1 is 11351.475 μm^2 (25.1 µm x 452.25 µm).

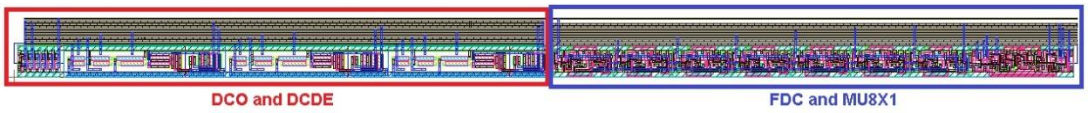


Figure 4.26 Placement and routing of the DCO-DCDE and FDC-MU8X1 blocks.

4.4 Final Layout of the Low Voltage (LV) Part of the Integrated Circuit

In previous sections all of the low voltage blocks of the driver part of the circuit have been explained. In this section all of designed LV blocks have been integrated in the same layout. Figure 4.27 shows the layout of the driver part of the chip. The beam-forming system provides each CMUT element with one of these LV blocks. Since we have sixteen CMUT elements, we need sixteen driver (LV) blocks. These blocks have been placed in four by four configurations and as compact as possible in a small area. According to Figure 4.27, the driver part of the chip has been placed in three floors. At first floor, an 8-bit shift register, enable circuit and MU2X1 have been placed. At the second one we have 8-bit comparator and one-shot circuit and finally at the third floor we placed DCO-DCDE, FDC and MU8X1 blocks. All of the routing process has been done using METAL1, METAL2 and METAL3.

The VDD and GND lines are connected via METAL3. Each MU2X1 provides the input of the correspondent high voltage pulser. The DRC (Design Check Rule), layout extraction and LVS (Layout VS Schematic) was successful for this cell. The die area of the driver part of the chip is 43283.7 μm^2 (94.3 µm x 459 µm).

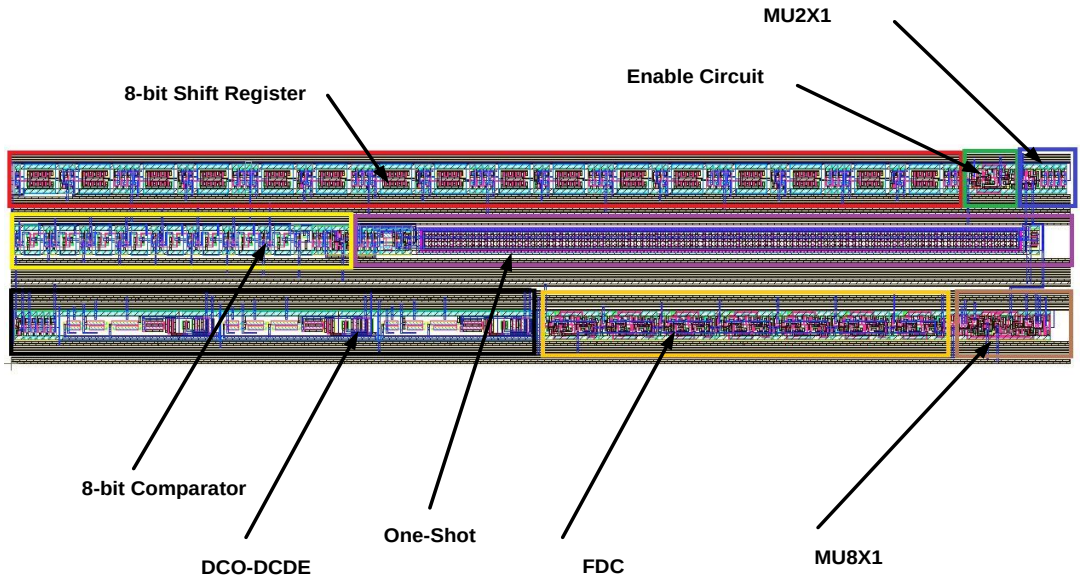


Figure 4.27 Layout of the driver part of the chip.

4.5 Layout of the Right Side of the Chip Core

In previous sections, layouts of the low voltage (LV) blocks of our ASIC design are discussed. As we mentioned before, the firing system provides each of 16 CMUT elements with one driver circuit shown in Figure 4.27. In this section, layouts of the high voltage (HV) part are explained. We decided to place high voltage pulser circuits and flip-chip bonding pads in the right side of the chip. Right side of the chip includes 4X4 configuration of flip-chip bonding pads that are supposed to be bonded to CMUT transducers. There are sixteen pulsers and flip-chip bonding pads for sixteen CMUT transducers. Figure 4.28 shows the dimensions of flip-chip bonding pads and their distances from each other. As can be observed, each pad is drawn in a square shape with 80 µm x 80 µm dimensions that is suitable for our application. The center to center distance between two adjacent CMUT elements in horizontal or vertical mode is 300 µm.

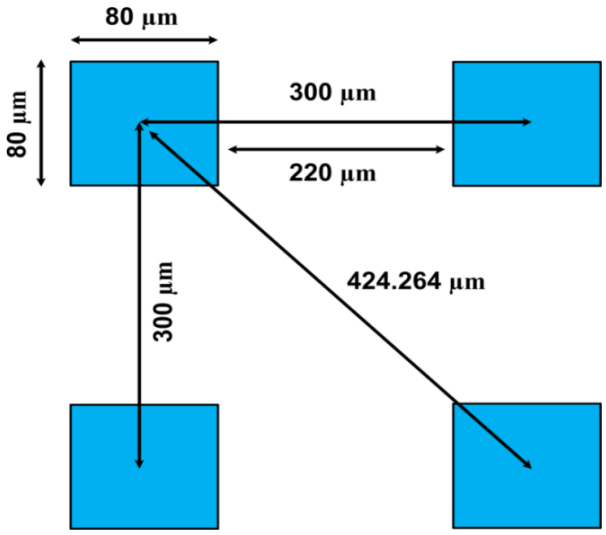


Figure 4.28 Configuration of flip-chip bonding pads with their dimensions.

Since the center to center distance of two adjacent CMUT elements is 300 µm and the total number of transducers in our first design is sixteen in 4X4 configuration, a 1200 µm by 1200 µm silicon area as right side of the chip-core is available. The 1.44 mm^2 area is divided into sixteen squares. According to dimensions of flip-chip bonding pads and the center to center distance of them, we decided to place the pads and the layouts of the corresponding pulsers in a 300 µm x 300 µm square. Figure 4.29 shows the combination of a flip-chip bonding pad with a pulser. As can be observed, if we place the pad at top of the square and the layout of the pulser at bottom side, they occupy less area. The routing between these two blocks are implemented using METAL3 and METAL4 layers.

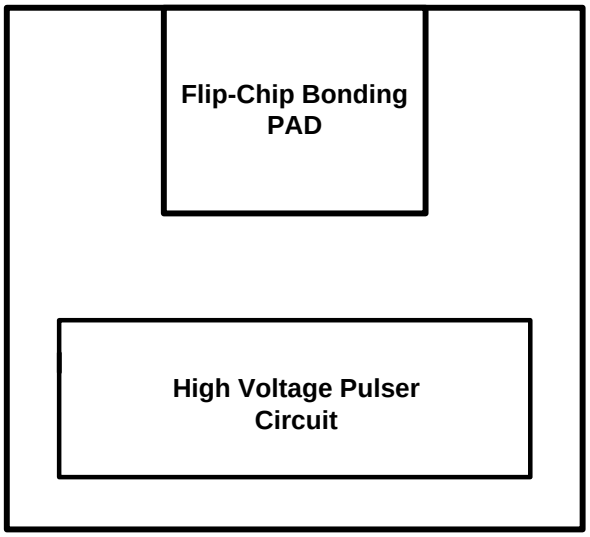


Figure 4.29 The combination of a flip-chip bonding pad with a pulser in a 300 µm x 300 µm square.

4.5.1 Layout of the High Voltage (HV) Pulser

In previous chapter, a 45 V high voltage pulser was presented. In this section, the layout of designed circuit with essential considerations is discussed. The layouts of the high voltage circuits are very important because we should care of many points. For example, the connections between high voltage transistors have been done via top metal layers and these metals should be as wide as possible. Figure 4.30 shows the layout of the 45 V pulser circuit. As can be observed, the HVDD and HVSS lines of the layout of high voltage circuit have been drawn in top side and down side of the layout wide METAL3 lines, respectively. The widths of metal lines are considered according to the amount of current that is flowing through them. The values of these currents were measured using simulation programs one by one.

As we observed in previous chapter, high voltage pulser has six transistors and one large inverter. Large inverter was placed in driver part of the layout and six transistors were placed in as small as possible die area. The driver signals of high voltage circuits are provided using two METAL3 lines which are close to each other and one is for input and next for output of the strong inverter. The DRC (Design Check Rule), layout extraction and LVS (Layout VS Schematic) was successful for this cell. All these cells were routed according to our design. The die area of the 45 V pulser circuit is 0.0434 mm^2 (152.3 µm x 285.075 µm).

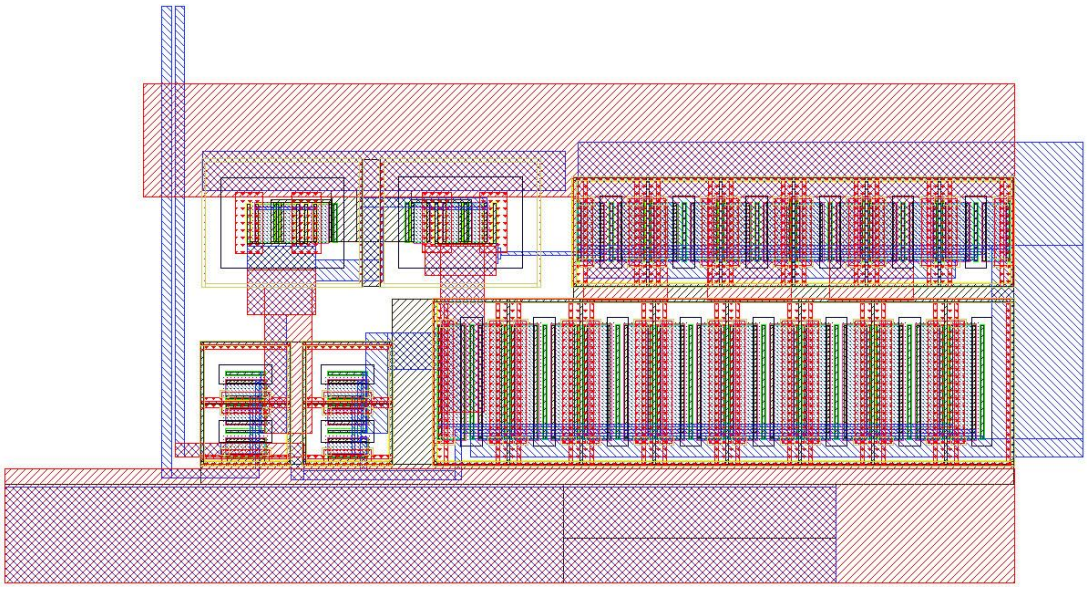


Figure 4.30 Layout of the 45 V high voltage pulser circuit.

4.5.2 Layout of the High Voltage Pulser with Flip-Chip Bonding Pad

In this section, the layout of the high voltage pulser is integrated with a flip-chip bonding pad in a 300 µm by 300 µm area. As we discussed in previous chapter, sixteen blocks including high voltage circuits and flip-chip bonding pads in 4X4 configuration is needed. The layouts of the pads are discussed in following sections. To have a negligible attenuation, these pads should be placed very close to the outputs of the high voltage

pulsers. As shown in Figure 4.31, drawn pad is placed exactly in mid of this region and hence the 300 µm separation from next pad can be obtained. As can be observed from this figure, two separated wide METAL4 lines have been drawn to make the connections of the HVDD and HVSS lines. The DRC (Design Check Rule), layout extraction and LVS (Layout VS Schematic) was successful for this cell. All these cells were routed according to our design. The die area of the high voltage pulser circuit with flip-chip bonding pad is 0.09 mm^2 (300 µm x 300 µm).

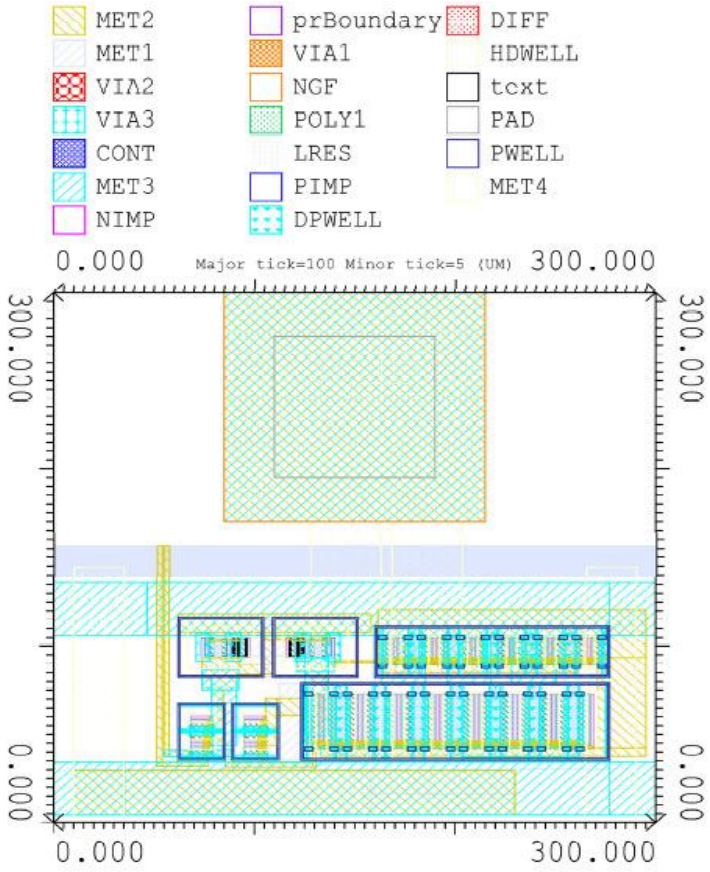


Figure 4.31 Layout of the high voltage pulser with flip-chip bonding pad in a 300 µm by 300 µm area.

As shown in Figure 4.31, there are 8 METAL1 lines that provide the driver signals of the high voltage circuits and make the connections of LV and HV parts. These lines are connected to high voltage pulsers one by one using METAL2 layers. On the other hand, wide METAL4 lines make the connections of high voltage circuits with flip-chip bonding pads.

4.5.3 Flip-Chip Bonding Pad

Figure 4.32 shows the first designed flip-chip bonding pad. Four different metals (METAL1, METAL2, METAL3 and METAL4) are used in parallel mode and connected using VIA1, VIA2 and VIA3. According to design rule check (DRC), we are not permitted

to use metals wider than 35 µm unless they are slotted or pad layers are used inside them. Since for our application, the minimum pad size is considered 50 µm by 50 µm and according to design rules, the minimum size of pads must be 72 µm by 72 µm, pad layers with 80 µm by 80 µm dimensions have been used in our designed chips. Pad layers are placed exactly in the mid of drawn four metal layers.

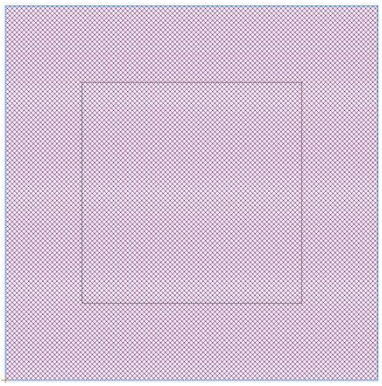


Figure 4.32 Layout of the first flip-chip bonding pad.

The DRC (Design Check Rule), layout extraction and LVS (Layout VS Schematic) was successful for this cell. The die area of the first flip-chip bonding pad is 0.015 mm^2 (122 µm x 122 µm).

4.6 Placement and Routing of Driver part (LV) of the Chip

In previous sections, the layouts of the used blocks in designed integrated circuit were shown and discussed. Drawn layouts were divided into low voltage and high voltage parts. Since in high voltage part of the chip, there is no enough space for placement of driver circuits, they are placed in left side of the high voltage region. In this section, the placement and routing process of left side of the chip are explained. Sixteen numbers of driver cells including 8-bit shift register, 8-bit comparator, one-shot, DCDE, FDC, multiplexer, demultiplexer, enable circuit and some combinational logic circuits, are placed in left side of the final chip. Since we have four CMUT elements in each row of our structure and each transducer needs one driver circuit, we decided to place the driver circuits in 4X4 configuration. Instead of placing four driver cells in one row, we combined two cells together and we decreased the occupied area by half. Figure 4.33 shows two routed driver cells. These cells are routed together vertically via METAL3 lines. The DRC (Design Check Rule), layout extraction and LVS (Layout VS Schematic) was successful for this cell. The die area of two routed driver cells is 0.128 mm^2 (271.15 µm x 472.15 µm).

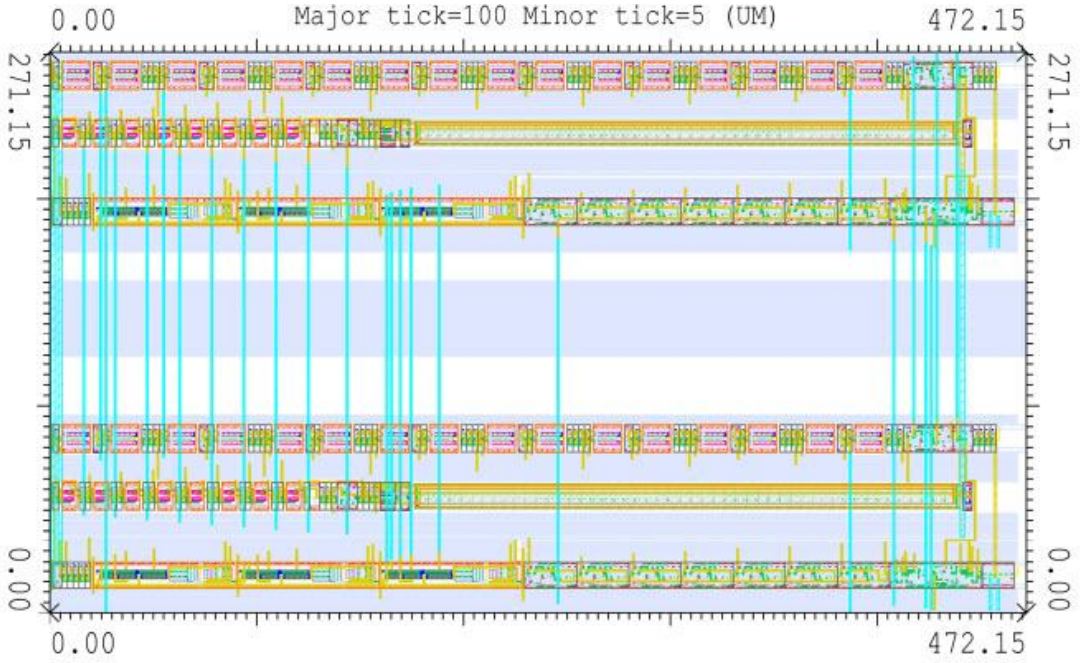


Figure 4.33 Layout of the two routed driver cells.

4.6.1 Final Layout of the Driver part (LV) of the Chip

Two of routed driver cells that have been shown in Figure 4.33 make the final layout for each row of the driver part of the chip. According to Figure 4.34, routed driver cells are placed next to each other and all the connections between them are completed automatically. As can be observed, by placing the driver cells in two rows and two columns, large silicon area can be saved. The DRC (Design Check Rule), layout extraction and LVS (Layout VS Schematic) was successful for this cell. The die area of the final layout for each row of the driver part of the chip is 0.25564 mm^2 (271.15 µm x 942.8 µm).

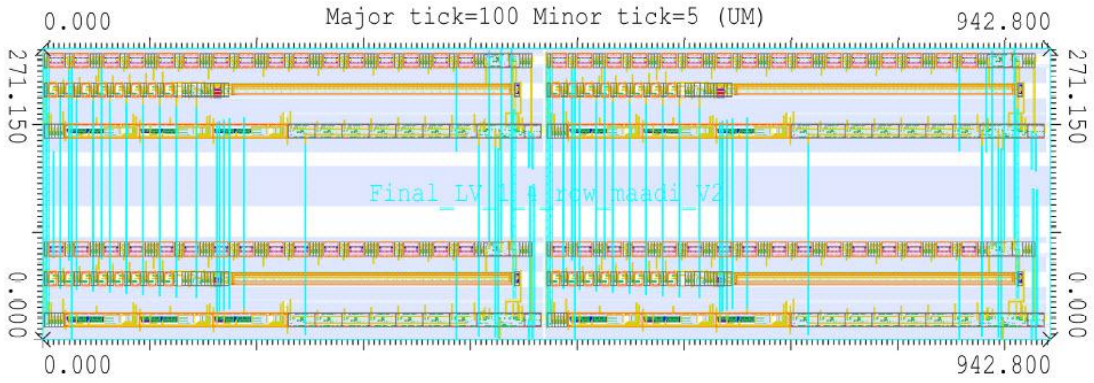


Figure 4.34 Layout for each row of the driver part of the chip.

4.7 Integration of LV and HV blocks of the Chip

In previous section, driver cells of the chip for one row were placed and routed. In this section, high voltage blocks are added to driver cells of the chip. Since four CMUT elements are in one row, four high voltage blocks are placed next to each other in front of the driver cells of the chip. Figure 4.35 shows the final layout of the chip that is considered for one row of CMUT elements. Before placing the driver part of the layout we considered some connection lines via METAL1. These connections are completed the communication between digital and high voltage parts. DRC (Design Check Rule), layout extraction and LVS (Layout VS Schematic) was successful for this cell. The die area of the final layout of the chip that is considered for one row of CMUT elements is 0.64284 mm^2 (300 µm x 2142.8 µm).

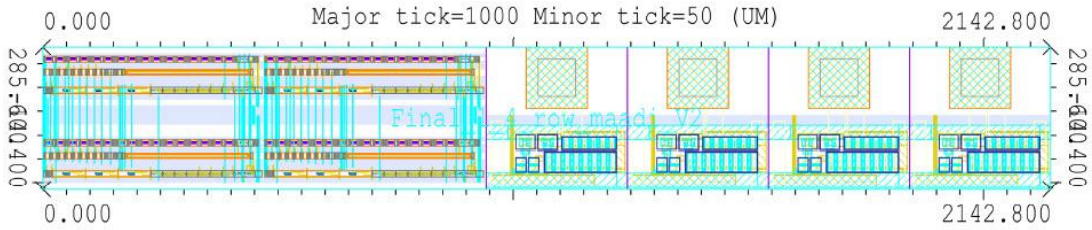


Figure 4.35 Final layout of the chip that is considered for one row of CMUT elements.

4.8 Core of the Chip

In previous sections, layouts of the low voltage and high voltage blocks with their essential considerations were discussed. In this section, four final layouts of the chip (shown in Figure 4.35) that is considered for one row of CMUT elements are placed in different lines and make the 4X4 configuration. Figure 4.36 shows the layout of the chip core. It is obvious that the core of the chip has been divided into two completely different parts: one is for driver circuitry and another for high voltage pulsers and flip-chip bonding pads. As can be observed, the center to center distance between each adjacent flip-chip bonding pads is 300 µm. This specification is very important for us because the CMUT array is supposed to be bonded on this part of the layout with the same configuration. The DRC (Design Check Rule), layout extraction and LVS (Layout VS Schematic) was successful for this cell. The die area of the chip core for 4X4 CMUT elements is 2.57 mm^2 (1.2 mm x 2.1428 mm).

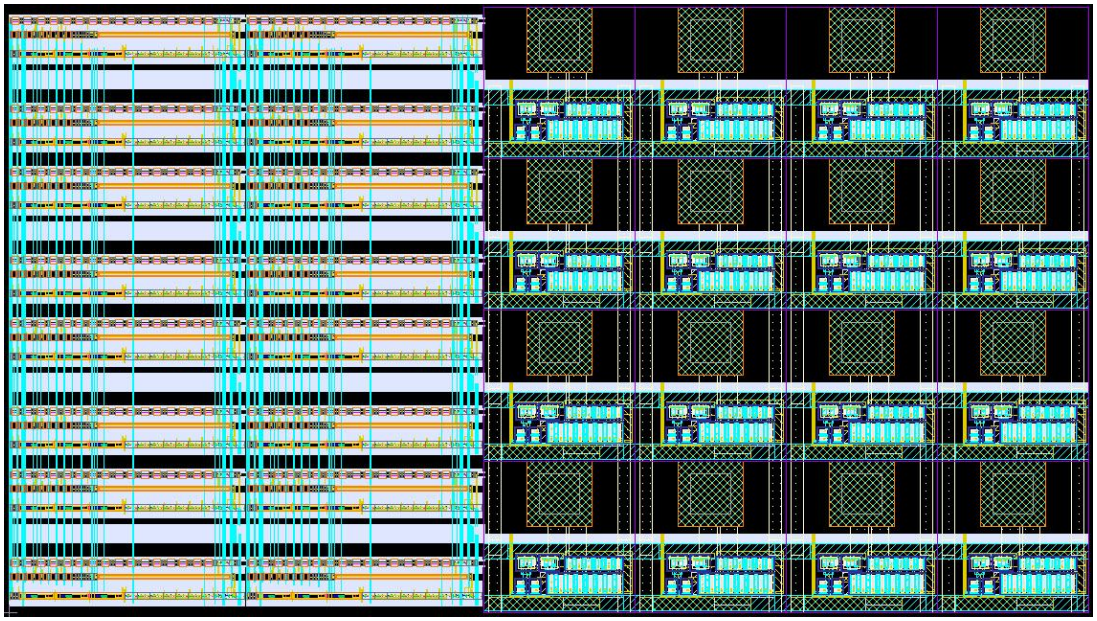


Figure 4.36 Core of the chip.

4.9 Wire Bonding Pads with Additional Cells

In previous sections, the core of the chip was prepared. In this section, the connections of the IC with external world are completed. According to our deigned chip, two kinds of bonding pads including low voltage (3.3 V) and high voltage (45 V) are needed. Low voltage bonding pads are considered for making the connections of the IC with FPGA and providing the supply voltage (3.3 V) of driver circuitry. Some of these pads are considered for providing the signals of the IC such as clocks, enable signals, delay information and so on and the rest are placed for testing the chip. As discussed in previous chapter, the HVDD of the high voltage pulsers is around 45 volts. Hence, custom designed pads for providing the supply of the pulsers are considered. These pads consist of four metal layers that are connected using VIA layers. As we explained before, CMUTs should be biased with DC and AC sources. The DC biasing pads of the CMUTs are bonded to the chip using flip-chip bonding method. In fact, the DC supply of the transducers is provided via bonding pads of the IC. In following sections, some details will be presented around bonding pads of the chip.

4.9.1 Low Voltage (3.3 V) Bonding PADs

There are various options such as gated pull-up and pull-down, input hold or gated input for CMOS and TTL input levels. Pad-limited input cells provide mentioned specifications as I/O libraries. Pad-limited instead of core-limited cells have been used as our I/O bonding pads, because core-limited cells are not recommended for the chips with large areas.

Figure 4.37 shows the 3.3 V pad-limited input cell. These pads are among non-inverting input buffer pad-limited 3.3 V input cells. Although these kinds of pads are characterized for the voltages between 1.8 V and 3.6 V, they can work with voltages in outside of those

ranges too, but with inaccurate delay times. The die area of the pad-limited 3.3 V input cell is 0.054 mm^2 (446.55 µm x 122 µm). As can be observed from Figure 4.37, these pads have eight pins. The PAD should be placed toward outside and the Y pin should be placed toward the core of the chip. All the rest pins are connected to corresponding pins of the adjacent cells automatically.

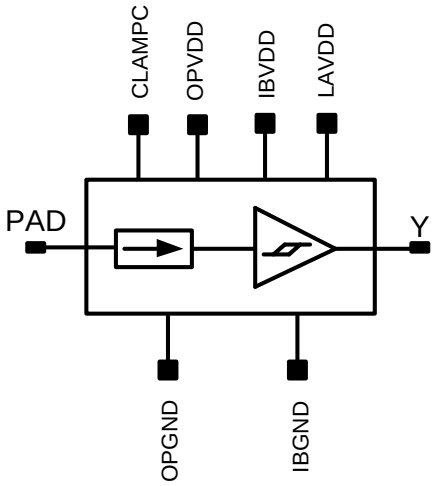


Figure 4.37 Pad-limited 3.3 V input cell.

Table 4.1 shows the truth table of pad-limited 3.3 V input cell. As can be observed there is no extra options for controlling the output of these kinds of pads.

Table 4.1 The truth table of pad-limited 3.3 V input cell.

PAD	OUTPUT
0	0
1	1
Z	X

4.9.2 Pad-Limited 3.3 V VDD and GND Power Supply Cells

As our supply bonding pads, 3.3 V VDD core supply cells were selected. These kinds of cells connect all VDD rails together and provide connection for chip core supply. For sharing the current equally, several VDD cells are used in a symmetric configuration. Since some cells like DCDEs are sensitive for VDD variations, we should provide the VDD in a short path with least attenuation. The die area of the pad-limited 3.3 V VDD and GND power supply cell is 0.055 mm^2 (447.51 µm x 122 µm). On the other hand, like VDD cells,

GND cells connect all GND rails together and provide connection for chip core ground supply.

4.9.3 Filler Cells

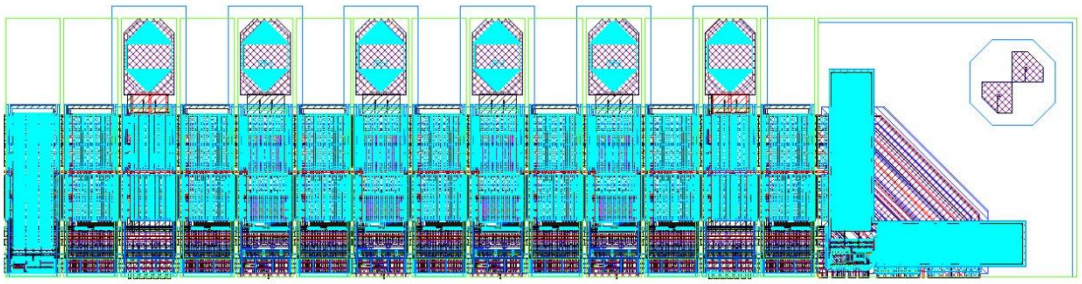
Although pad-limited I/O cells can be used together without adjacent filler cells, we need to separate them with filler cells because of some limitations in wire bonding process. Pad-limited 3.3 V I/O cells must be placed in a minimum pitch of 89.6 µm. Filler cells should be placed at increments of 11.2 µm and without having overlays in I/O cells. Depending on the position of the pads, in some of the cases wide filler cells with 89.6 µm wide and power supply protection diodes are used. The die area of the pad-limited filler cell with power supply protection diodes is 0.040 mm^2 (424.2 µm x 95.4 µm).

4.9.4 Clamp Cells

In the case of having electrostatic discharge (ESD), the power supply clamp circuits turn to low resistance and they make the OPVDD and OPGND power supply rails, short circuits. There is a huge PMOS clamp transistor and a RC timer circuit inside of the power supply clamp circuits. For every pulse in power rail, this PMOS is going to be turned on and after a certain time longer than an ESD pulse, the RC timer circuit turns off the clamp device. Two kinds of power supply clamp cells can be used as pad-limited I/O cells. The first one is corner clamp cell that can be placed in the corners of the chip. Another one is I/O clamp cell that requires the space of one I/O cell in its configuration. In fact filler cells do not have an own clamp driver circuits and must only be used with clamp cells containing a driver circuit. In fact, clamp cells do not have a bonding pad. The die area of the pad-limited I/O clamp cell is 0.038 mm^2 (424.2 µm x 89.6 µm). Since one pad-limited I/O clamp cell has the same width of one I/O cell, they decrease the maximum number of I/O cells that can be placed around a chip. Instead of the corner cell, we can use pad-limited corner clamp cell. We should note that, every 3 mm of chip perimeter needs one clamp cell. The die area of the Pad-limited I/O corner clamp cell with power supply clamp circuit is 0.182 mm^2 (426.5 µm x 426.55 µm).

4.9.5 A Sample Configuration of Bonding Pads in Driver Part of the Chip

In previous sections, different I/O cells of bonding pads were discussed. Before starting the placement process of bonding pads, we should know that how many pads we need for our chip and where they should be placed. Figure 4.38 shows a sample configuration of bonding pads in driver part of the IC. As can be observed, adjacent cells should be connected together by attaching their pro-boundary layers and all of their pins are connected automatically.



CLAMP CELL	FILLER CELL	VDD CELL	FILLER CELL	I/O CELL	FILLER CELL	I/O CELL	FILLER CELL	I/O CELL	FILLER CELL	I/O CELL	FILLER CELL	GND CELL	FILLER CELL	CRNER CELL

Figure 4.38 A sample configuration of I/O bonding pads in driver part of the IC.

4.10 Custom Designed Chip for 4X4 CMUT Ultrasound Therapeutic Applications

In previous sections, all blocks of the IC for 4×4 CMUT therapeutic applications were explained. In this section, final designed chip are presented. As shown in Figure 4.39, designed IC consists of four main regions as low voltage (LV) bonding pads, high voltage (HV) bonding pads, CMUT DC pads and core of the chip. LV bonding pads provide the communication of driver part of the chip with FPGA. HV bonding pads provide the high voltage power supply of the pulsers and DC pads are supposed to be bonded to CMUT transducers using flip-chip bonding pads to provide DC voltages of the CMUT elements. Some pads have been placed both in LV and HV parts for getting some test results from the IC.

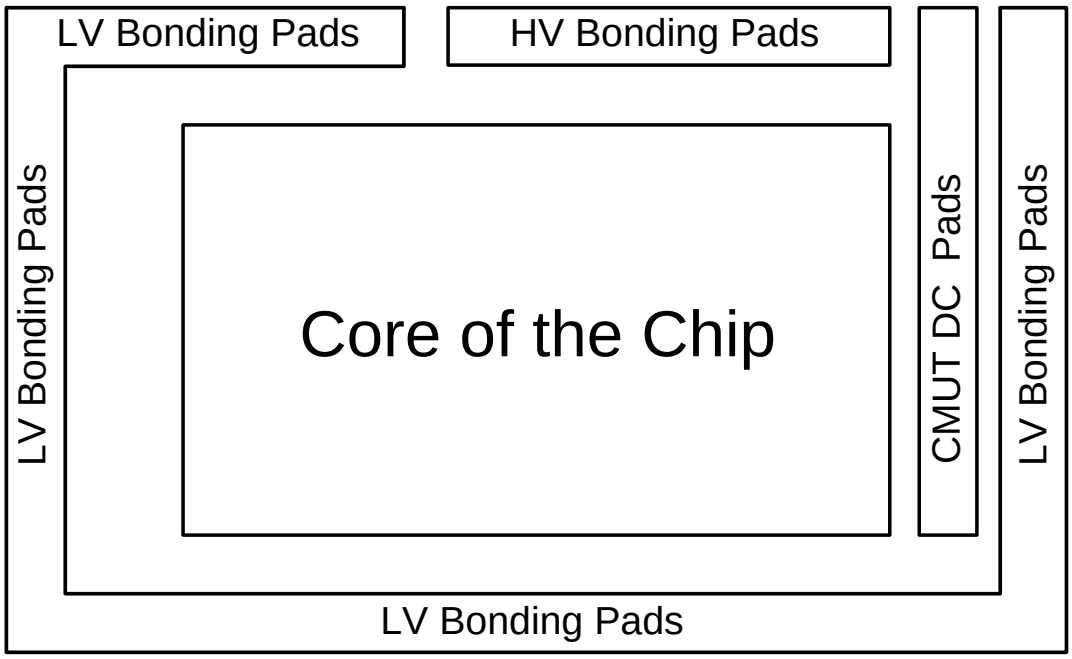


Figure 4.39 Final chip for 4X4 CMUT therapeutic applications.

Figure 4.40 shows the final layout of the designed integrated circuit for ultrasound therapeutic application. The final IC has 45 I/O LV (3.3 V) bonding pads, seven supply bonding pads for 3.3 V, nine HV bonding pads and one pad for DC supply of the CMUT ultrasound transducers. The low voltage pads have been considered for testing and driving the IC using FPGA, the high voltage pads are for testing and supporting the high voltage supply of the IC and finally the DC pad is supposed to be connected to MEMS part using flip-chip bonding pads and we will give the DC supply of the CMUTs using this pad. The DRC (Design Check Rule), layout extraction and LVS (Layout VS Schematic) was successful for this cell. The die area of the final designed chip for CMUT therapeutic application is 13.5725 mm^2 (4450 µm x 3050 µm).

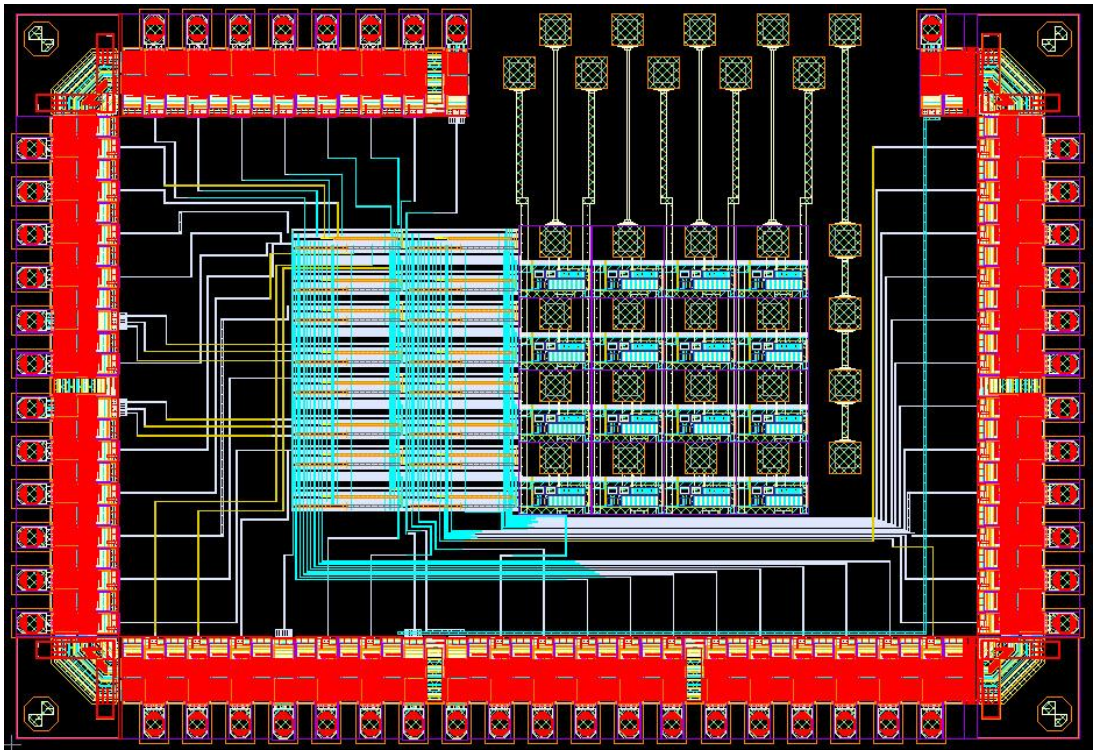


Figure 4.40 Final chip for 4X4 CMUT therapeutic applications.

4.11 Summary of the Chapter

In this chapter, the layout of the IC for CMUT therapeutic applications in 4×4 configuration has been demonstrated. The designed ASIC includes LV (driver) and HV electronics that have been placed next to each other. Each CMUT elements is provided with one LV and HV circuitry. LV part of the chip consists of sixteen driver blocks that have been placed in 4×4 array while HV region in right side of the IC includes sixteen high voltage pulsers with their flip-chip bonding pads. In fact, LV part of the chip provides beam-forming signals of the HV blocks. Since the IC needs to be controlled with many external lines, final chip was provided by many wire bonding pads with their own protection circuits. The DC biasing of the CMUTs is given by the IC using flip-chip bonding pads. Next chapter explains the theory, design and simulation results of a different IC in 0.35 CMOS technology, suitable for CMUT ultrasound therapeutic applications in 16×16 configurations with the ability of generating 100 V signals using HVTHKOX modules.

CHAPTER 5

THE ULTRASOUND THERAPEUTIC IC FOR 16X16 CMUT ARRAY IN HV 0.35 µm CMOS TECHNOLOGY

This chapter presents the theory, design, simulation results and layouts of different blocks (LV and HV) of the IC for 16X16 CMUT array, which have been designed in HV (high voltage) 0.35 µm CMOS technology that is a widely available process. The utilized driver circuitry for 4×4 CMUT elements is used for this new IC but the high voltage blocks have been changed with new designs to generate beam-forms with the magnitudes of up to 100 volts. Instead of THKOX modules, HVTHKOX must be used. The transistors of new pulsers can bear up to 100 V on their drain-source junctions. Hence, exciting CMUT elements with large signals and reasonable power consumption is possible. The rest of the chapter describes the layout of the IC by providing important considerations.

The previous chapter presented the different required building blocks that are needed for different typical ultrasound transducers beam-form generator. In chapter 3, schematics, simulation results and design methods of an ultrasound therapeutic IC for 4×4 CMUT elements are discussed. Designed chip consists of LV and HV blocks. Driver part (LV) of the IC provides beam-forming signals of the CMUT elements and HV pulsers increase the magnitudes of provided signals up to 45 volts with THKOX modules. Chapter 4 described the layout of the IC for proposed interface circuitry introducing important considerations. In this chapter, section 5.1 presents the overview of the Ultrasound Therapeutic IC for 16X16 CMUT Array. Section 5.2 explains the driver circuitry of the chip. In this chapter, Section 5.3 describes the designed new high voltage circuits. Section 5.4 gives the schematic, design and simulation results of a different pulse train generator. In section 5.5, designed new pulse train generator is integrated with a 100 V pulser for generating high trains of pulses with large magnitudes and in section 5.6 the same pulser is combined with a one-shot circuit for providing adjustable single pulses with large amplitudes. Section 5.7 to 5.15 presents the layout of the designed integrated circuit for 16X16 CMUT array. Section 5.16 describes another custom designed chip for 4X4 CMUT array with HVTHKOX modules. Finally, section 5.17 summarizes this chapter.

5.1 The Overview of the Ultrasound Therapeutic IC for 16X16 CMUT Array

The proposed ultrasound therapeutic IC consists of different types of blocks which are placed on the same chip in HV 0.35 µm CMOS technology. For each CMUT element, one

complete block including all of designed LV and HV circuits is considered, hence the final size of the chip is completely depends on the numbers of the CMUT elements. The designs for driver (LV) part of the IC have been fully explained in chapter 3 in HV 0.35 µm CMOS process. As we discussed, driver circuitry generate the beam-forms using low voltage signals and deliver the signals to high voltage pulsers. This chapter mostly focuses on the design and simulation results of new high voltage pulser circuits with up to 100 V magnitudes and using DMOS (double diffused MOS) transistors. These circuits are designed using HVTHKOX modules and are not suitable for XFAB MPW runs.

The IC uses a 16×16 CMUT transducer array for therapeutic applications. The IC consists of 256 element transmit beam-formers for 256 ultrasound transducers that are configures in square shape.

5.2 Driver (LV) Circuitry of the Chip

The theory and state-of-the-art designs for driver part of the IC have previously explained in chapter 3. As we discussed, the driver circuitry provides each of 256 CMUT elements with an 8-bit shift register (SIPO), an 8-bit comparator, a one-shot circuit, a digitally controlled oscillator with 5-bits digitally controlled delay elements, a frequency down conversion circuit. In our designed IC for 16×16 CMUT transducer array, we used the same CMUT driver circuitry but the high voltage blocks have been changed and designed using different modules.

5.3 High Voltage Circuit Design with HVTHKOX Modules

High voltage (HV) circuits can be designed using special DMOS or drain extended MOS transistors. These impressing circuits are offered using modern CMOS triple-well processes [63]. The beam-former circuitry provides each of 256 CMUT transducer elements with a 90 V (up to 100 V with temperature limitations) pulser circuit using HV thick oxide transistors (HVTHKOX). The pulser is an analog high voltage circuit. The size of the transistors depends on the output load capacitance [92], [93] and the width of the output signals must be set to match the transducer operating frequency. In following sections, different HV pulser circuits with HVTHKOX modules are presented. The transistors of pulsers are high voltage and high thickness and their parameters are shown in Table 5.1.

Table 5.1 Parameters of high voltage and high thickness transistors.

Device	90V drain PMOS (thick oxide) [a]	90V nDMOS (thick oxide) [a]
Device Name in HV 0.35 µm CMOS Process	phvf	ndhg
Available with module	HVMOSTHK [b]	HVMOSTHK [b]
|VT| (V)	1.60	1.33
IDS (µA/µm)	150	310
|BVDS| (V)	> 105	> 110
RON [kΩ.µm]	64	19
RON*A [mΩ.mm^2]	428	166
Max. |VDS| (V)	90 (100) [c]	90 (100) [c]
Max. VGS (V)	18	18

a) @ VGS = 12V b) Not suitable for XFAB MPW run
c) reduced junction temperature limit @ Tj = -25ºC ... +85ºC

5.3.1 Different Designed High Voltage Pulser Circuits

In this chapter, different high voltage pulsers using DMOS (double diffused MOS) transistors with up to 100 V magnitudes are discussed and their design and simulation results are presented. Integration of DMOS transistors with MOS transistors can be used for driving of CMUT array elements because they can sustain the 90 V on their drain-source junction.

5.3.2 A Simple 100 V High Voltage Driver Circuit

As shown in Figure 5.1, a conventional high voltage driver circuit consists of an output stage with HV-NMOS pull down and HV-PMOS pull-up transistors [67]. While HV-NMOS transistor can be controlled using low voltage (3.3 V) control signals, HV-PMOS transistor is biased by a reference voltage (V_{REF}). For proper operation of HV-PMOS transistor, an appropriate signal must be applied to reference voltage (V_{REF}) according to following equation:

$$V_{REF} < V_{HV} - V_T \tag{5.1}$$

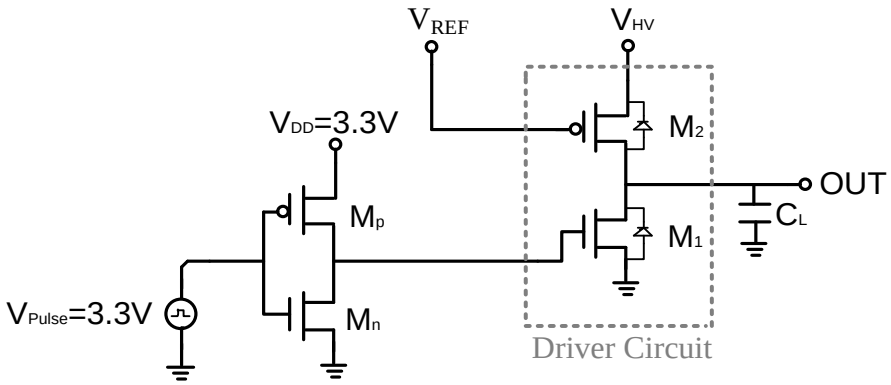


Figure 5.1 A high voltage driver circuit.

The control signals of HV-PMOS transistor can be accomplished by a level shifter or pulser circuit. In following sections, some pre-driver circuits for controlling of driver circuits are presented. HV-NMOS and HV-PMOS transistors are high voltage transistors that have a large breakdown voltage in comparison with standard transistors. The drain-source breakdown voltages of these transistors (90 V in HV 0.35 µm CMOS technology) are very large while they have much lower gate-source breakdown voltages (18 V in HV 0.35 µm CMOS technology). In our designed high voltage driver circuit, the control signal for the HV-NMOS transistor changes from 0 to 3.3 V while the gate voltage of HV-PMOS transistor should be close to V_{HV} to protect the circuit from having high gate-source voltages. Table 5.2 summarizes the selected (W/L) values of transistors of the designed high voltage driver circuit.

Table 5.2 (W/L) values of the transistors for designed high voltage driver circuit.

	M_n	M_p	M_1	M_2
W (µm)	20	40	20	15
L (µm)	0.35	0.35	1.1	2
Number of Gates	1	1	35	13

Figure 5.2 shows the simulation results of 90V driver circuit when the frequency of the input pulse is 100 ns and the V_{REF} is 84 V. As can be observed, the output of the circuit is 90 V (HV) while its input is 3.3 V (LV). The rise and fall time of designed circuit is identical with the value of 22.58 ns and the average power consumption of this circuit is around 450 mw. As discussed in chapter 3, these kinds of circuits consume large values of powers and hence, most of papers and research do not share any information about power consumptions.

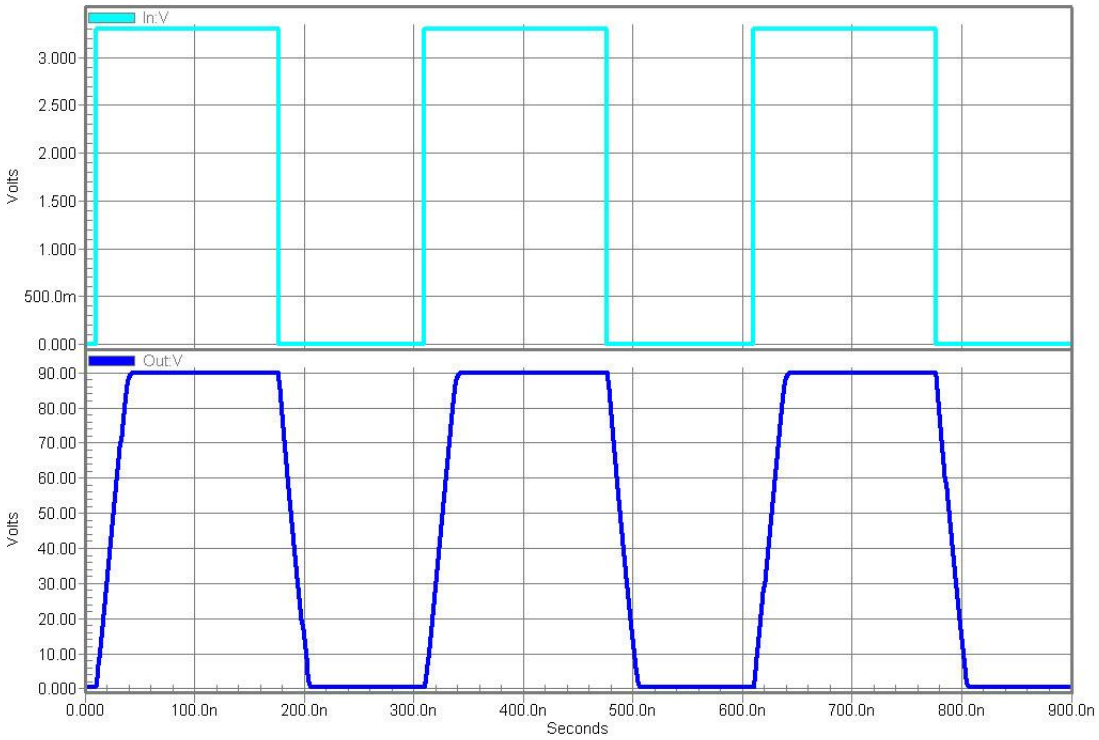


Figure 5.2 Simulation result of 90 V driver circuit when the frequency of the input pulse is 100 ns and the V_{REF} is 84 V.

5.3.3 Designed High Voltage Pulser Circuit with 100 V Amplitude

The high voltage pulser circuit that is shown in Figure 5.3 [44] has been designed using the first stage of the pulser circuit discussed in [65]. High voltage transistors with the ability of sustaining 90 V on their drain-source junctions have been used in designed pulser. Depending on the value of the V_{REF} and input signals, the output of the pulser can be increased up to 100 V. The transistors of the high voltage pulser are sized to drive 2.5 pF capacitive loads and provide pulses as short as 100 ns. In designed circuit, the width of the output pulses depends on the width of the input controlling signal (V_{pulse}). As can be observed from Figure 5.3, if we want to adjust the magnitude of the output pulses on 100 V, the value of the V_{REF} is set 94 volts. The value of the V_{REF} should be as much as possible to decrease the gate-source voltage of upper transistors and as short as possible to gain output high voltage signal. By providing this voltage directly, we can control the gate-source voltage of the transistors.

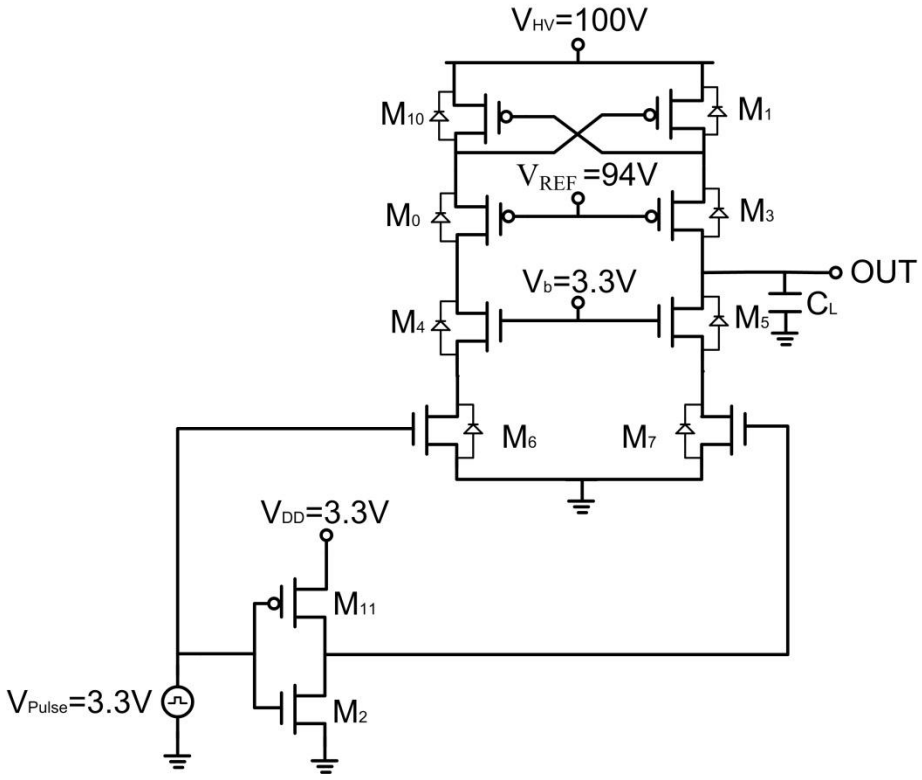


Figure 5.3 Designed 100V pulser circuit.

Two kinds of pulser circuits were designed using the same topology but with different transistor sizes. Tables 5.3 and 5.4, summarize the selected (W/L) values of transistors of the first and second 100 V pulser circuit, respectively.

Table 5.3 (W/L) values of the transistors for the first designed 100 V pulser circuit.

	M_{10}	M_1	M_0	M_3	M_4	M_5	M_6	M_7	M_2	M_9
W (μm)	20	45	20	30	20	50	20	50	3.2	8
L (μm)	2	2	2	2	1.1	1.1	1.1	1.1	0.35	0.35
Number of Gates	12	16	4	8	4	20	4	20	1	1

Table 5.4 (W/L) values of the transistors for the second designed 100 V pulser circuit.

	M_{10}	M_1	M_0	M_3	M_4	M_5	M_6	M_7	M_2	M_9
W (μm)	20	50	20	30	20	50	20	50	6	40
L (μm)	2	2	2	2	1.1	1.1	1.1	1.1	0.35	0.35
Number of Gates	20	32	8	16	8	40	8	40	1	1

As shown in Figure 5.3, similar to a standard flip flop, the gates of M1 and M10 transistors are cross coupled to provide positive feedback for decreasing the switching time. Figures 5.4 and 5.5 show the simulation results of designed 100 V pulser circuit while the input pulse width is 100 ns.

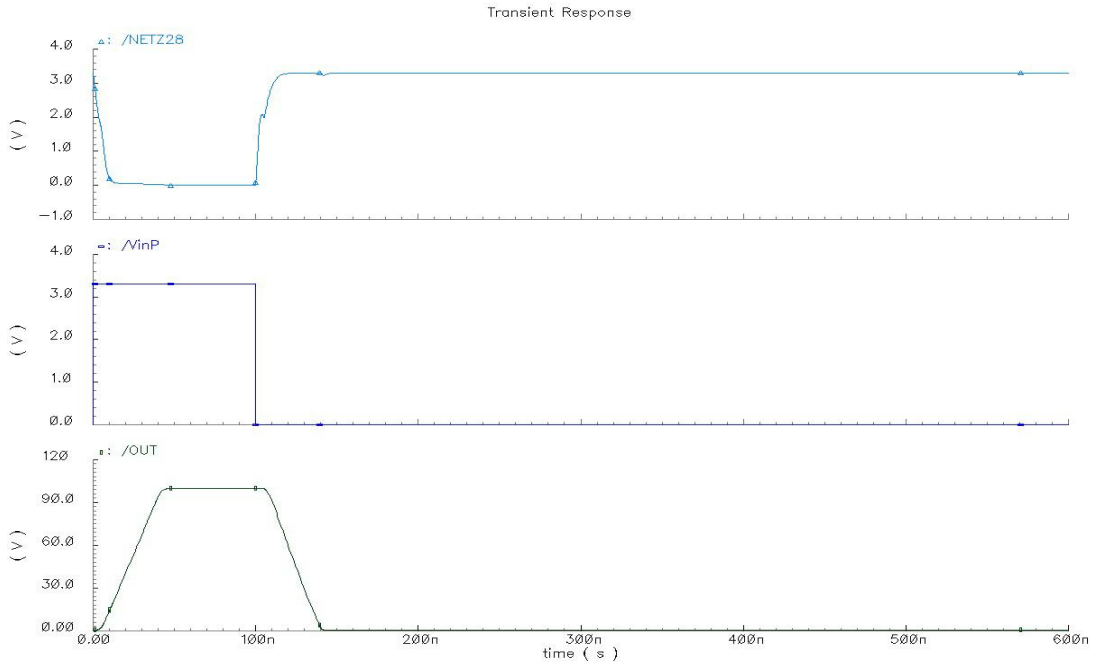


Figure 5.4 Simulation results of first designed high voltage pulser circuit.

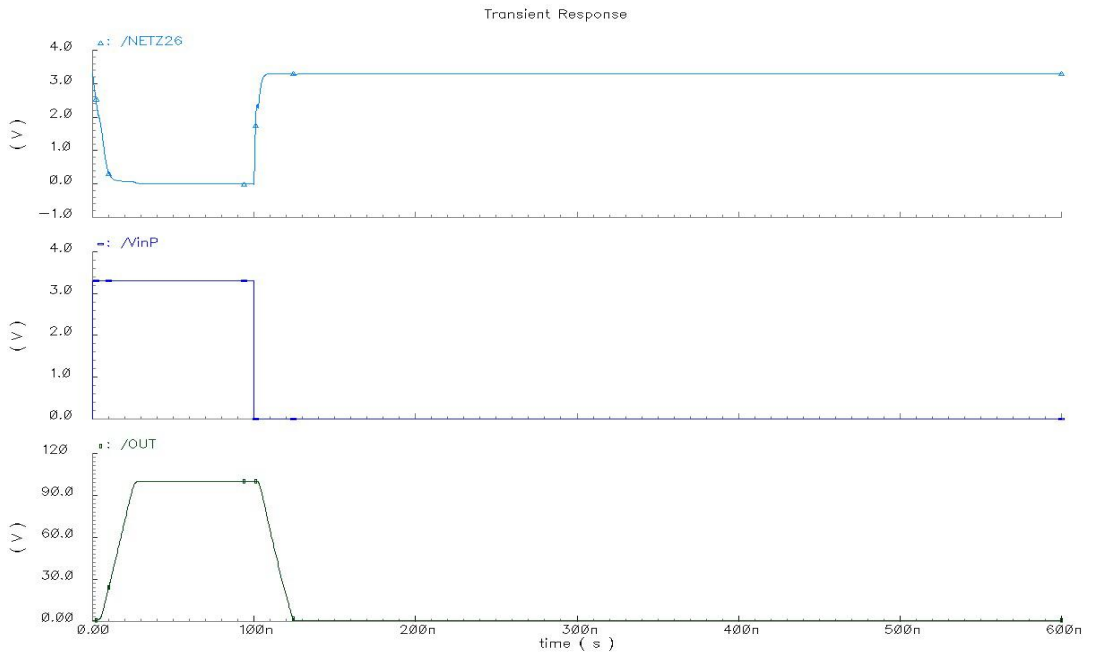


Figure 5.5 Simulation results of second designed high voltage pulser circuit.

As shown in Figure 5.5 and Table 5.5, although the rise and fall time are decreased, the power dissipation was increased dramatically.

Table 5.5 Specifications of designed high voltage pulser circuit for up to 100-V (Driving a 2.5 pF capacitance load).

	P_{diss} (mw)	t_r (ns)	t_f (ns)	C_L (pF)
First designed pulser	808.27	29.84	26.44	2.5
Second designed pulser	1584	16.82	16.65	2.5

5.3.4 Final Designed 100 V High Voltage Pulser Circuit

In previous sections, a high voltage pulser and driver circuit was discussed. In this section, different types of designs using the same circuit are presented. Figure 5.6 shows the final high voltage circuit design that is configured as a source follower circuit. As discussed in chapter 3, the timing circuitry is programmed to control the pulse width or frequency of the pulse train before being passed to the high voltage circuit. In our designed circuit, the output push pull transistors are sized to drive a capacitance load of 2.5 pF. In design of high voltage pulser circuits, we should consider some essential parameters such as, rise and fall time, maximum allowed gate-source or source-gate voltage, the drain current of transistors, the W/L ratio of transistors, power consumption, speed and etc. Different circuits with various topologies were designed and finally the circuit that is shown in Figure 5.6 was used as our high voltage circuit. For optimizing the circuit, all essential parameters were checked. In fact, all the parameters should be considered simultaneously otherwise serious problems may be occurred.

Table 5.6 summarizes eight different designs for shown high voltage circuit (Figure 5.6). For our therapeutic application, the cases 4 and 8 can be suitable. Most of the parameters in case 4 and 8 are the same but the last design (case 8) guarantees the sizes of the transistors by considering their drain-source or source-drain currents.

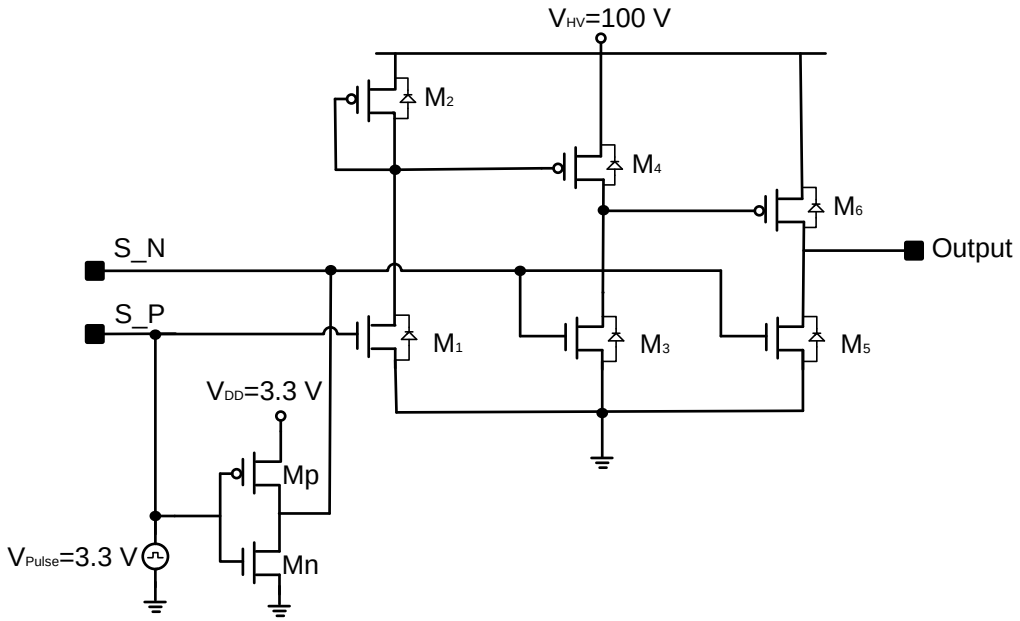


Figure 5.6 Final designed 100 V pulser circuit.

Tables 5.6 and 5.7 summarize eight different designs for shown high voltage circuit (Figure 5.6). For our therapeutic application, the cases 4 and 8 can be suitable. Most of the parameters in case 4 and 8 are the same but the last design (case 8) guarantees the sizes of the transistors by considering their drain-source or source-drain currents. Although rise and fall time can be decreased, but we have to increase the size of transistors at the same time which flows large currents into transistors and hence these circuits occupy much more silicon areas. The final rise and fall time of designed high voltage circuit 20 ns and 27 ns, respectively and the average power consumption of the circuit when the HVDD is 90 is 135.9 mw that in comparison with similar designs this circuit consumes less power [63].

Table 5.6 Specifications of eight different designed high voltage pulser for up to 90-V (Driving a 2.5 pF capacitance load).

Case	Rise time (ns)	Fall time (ns)	Max V_{GS_M6} (V)	Max $V_{SG\_M4,2}$ (V)	W_{M1} (µm)	W_{M2} (µm)	W_{M3} (µm)	W_{M4} (µm)
1	16.73	21.97	5.79	7.88	20	10	20	10
2	17.1	22.7	5.71	5.42	20	20	20	20
3	25.64	32.83	4.65	5.03	12	20	12	20
4	20.3	26.38	5.22	5.1	15	20	15	20
5	31.18	39.53	4.25	4.7	10	20	10	20
6	32.36	41.06	4.3	3.97	10	30	10	30
7	17.65	23.44	5.6	5.36	20	30	20	30
8	20.82	27.16	5.12	4.56	15	30	15	30
$(W/L)_{M6}$=100/1.1 and $(W/L)_{M5}$=300/1.1 C_{Load} = 2.5 pF								

Table 5.7 Specifications of eight different designed high voltage pulser for up to 90-V (Driving a 2.5 pF capacitance load).

	Case 1	Case 2	Case 3	Case 4	Case 5	Case 6	Case 7	Case 8
Max. I_M_6 (mA)	11.44	11.15	7.43	9.4	6.29	6.58	10.8	9.07
Max. I_M_2 (mA)	0.8	0.81	0.597	0.574	0.39	0.43	0.85	0.645
Max. I_Source (mA)	13.2	12.96	8.56	10.69	6.93	6.75	12.48	10.36

Figure 5.7 shows the simulation results of final designed 90V pulser circuit which has been designed with HVTHKOX (high voltage thick oxide) transistors. As can be observed, the output of the circuit is 90 V (HV) while its input is 3.3 V (LV).

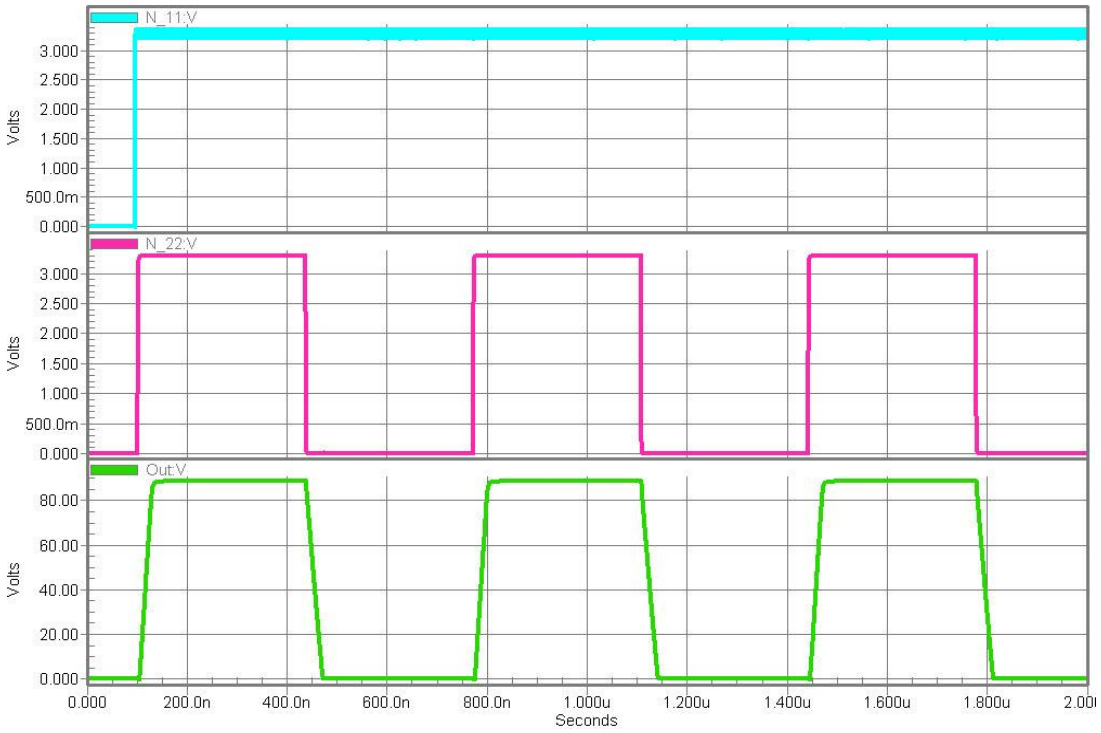


Figure 5.7 Simulation results of final designed high voltage pulser circuit.

Table 5.8 summarizes the important parameters of designed high voltage pulser circuit with the magnitude of 90 volts. These parameters will be compared with previous works by others in following section.

Table 5.8 Specifications of designed high voltage pulser at V_{HV} = 90 V (Driving a 2.5 pF capacitance load).

Parameter	Simulation Results	Units
Rise Time (10%-90%)	20.82	ns
Fall Time (90%-10%)	27.16	ns
Slew Rate (rising)	0.573	V/µs
Slew Rate (falling)	2.46	V/µs
P_{av} (dissipation)	135.9	mw
Figure of Merit = D/(LV)	0.82	ns/(µm.V)

5.3.5 A 45-V High Voltage Pulser Circuit Design with HVTHKOX Modules

In previous section, a high voltage pulser with magnitudes of up to 100 V was presented. In some of the cases, ultrasound transducers are excited with less AC and high DC voltages. In this section, a high voltage pulser circuit with the outputs of up to 45 V is discussed. The same schematic and modules of 90 volts pulser have been used in this circuit but better

specifications have been obtained. Table 5.9 summarizes the selected (W/L) values of transistors of the designed 45 V pulser circuit with HVTHKOX modules.

Table 5.9 (W/L) values of the transistors for designed 45-V pulser.

Device	M1	M2	M3	M4
W (µm)	10	15	10	15
L (µm)	1.1	1.7	1.1	1.7
Number of Gates	1	1	1	1
Device	M5	M6	M7	M8
W (µm)	20	10	20	40
L (µm)	1.1	1.1	0.35	0.35
Number of Gates	8	6	1	1

Figure 5.8 shows the simulation results of designed 45V pulser circuit which has been designed with HVTHKOX (high voltage thick oxide) transistors. As can be observed, the output of the circuit is 45 V (HV) while its input is 3.3 V (LV).

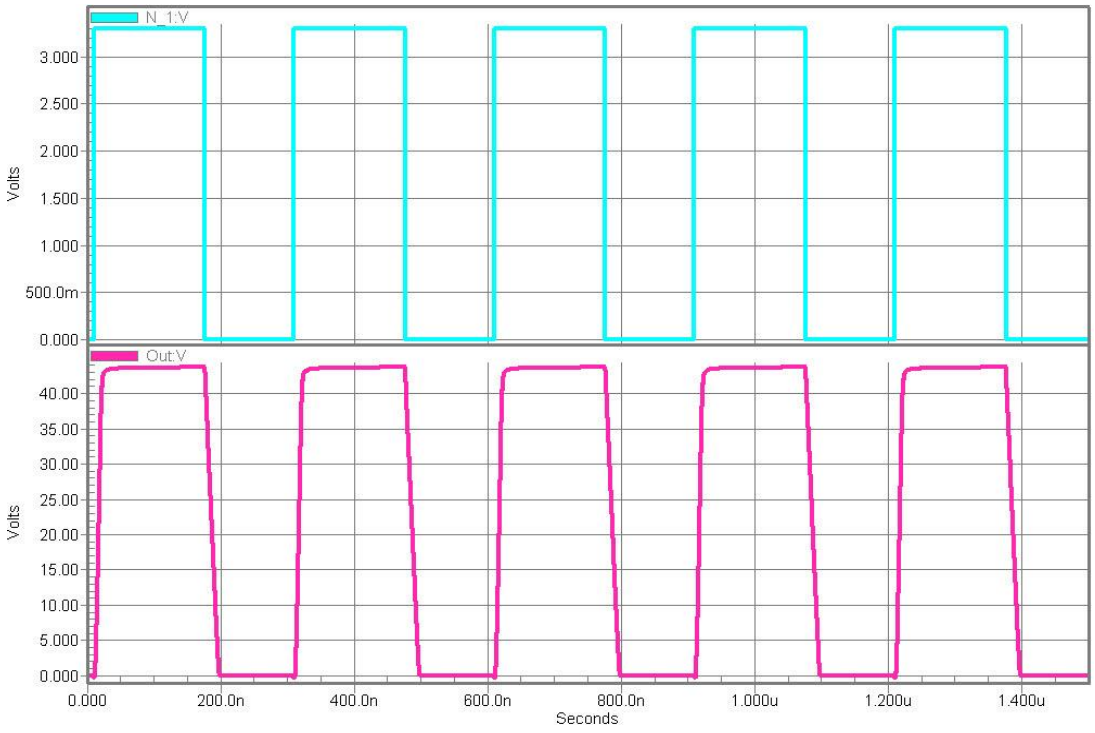


Figure 5.8 Simulation results of designed 45 V high voltage pulser circuit.

Table 5.10 summarizes the important parameters of designed high voltage pulser circuit with the magnitude of 45 volts. These parameters will be compared with previous works by others in following section. As can be observed, this pulse shows better specifications because it is supposed to generate half of the magnitudes of previous pulser circuit.

Table 5.10 Specifications of designed high voltage pulser at V_{HV} = 45 V (Driving a 2.5 pF capacitance load).

Parameter	Simulation Results	Units
Rise Time (10%-90%)	8.15	ns
Fall Time (90%-10%)	16.85	ns
Slew Rate (rising)	0.265	V/µs
Slew Rate (falling)	1.48	V/µs
P_{av} (dissipation)	26.46	mw
Figure of Merit = D/(LV)	0.74	ns/(µm.V)

Table 5.11 compares some specifications of designed high voltage pulser circuit with previous works by others. As can be observed, designed circuit shows reasonable outputs in comparison with prior research.

Table 5.11 Comparison of designed high voltage circuit with previous works by others.

Prior Work	Year	Tech Type	Tech Node L (µm)	Delay D (ns)	Voltage V (V)	Figure of Merit=D/(LV) ns/(µm.V)
Declerq et al. [65]	1993	CMOS	2	80	50	0.8
Doutreloigne et al. [84]	1999	HV CMOS	0.7	15	20	1.07
Pan et al. [82]	2003	HV SOI	0.35	20	18	3.2
Park et al. [85]	2006	DMOS	1	50	160	0.31
Doutreloigne et al. [88]	2006	HV CMOS	0.7	2000	100	28.6
Serneels et al. [90]	2006	CMOS	0.13	0.08	2.4	0.26
Chebli et al. [89]	2007	HV CMOS	0.8	475	100	5.9
Rossberg et al. [86]	2007	SOI - CMOS	-	350	400	-
Boyle et al. [87]	2008	HV CMOS	0.35	2.5	25	0.29
Khorasani et al. [67]	2008	HV CMOS	0.8	-	300	-
Choi et al. [83]	2009	SOI	-	-	100	-
Khorasani et al. [64]	2009	HV CMOS	0.8	-	150	-
Moghe et al. [63]	2010	HV CMOS	0.35	2.4	10	0.69
Present work	2013	HV CMOS	0.35	5.8	15	1.08
Present work	2013	HV CMOS	0.35	7	30	0.66
Present work	2013	HV CMOS	0.35	8	45	0.51
Present work	2013	DMOS	0.35	11.7	45	0.74
Present work	2013	DMOS	0.35	25.95	90	0.82

5.4 Pulse Train Generation Circuit with Different Method

In chapter 3, a pulse train generation circuit using the combination of DCO (digitally controlled oscillator), 5-bits DCDE (digitally controlled delay line) and FDC (frequency down conversion) circuits was explained. As we discussed, firing of CMUT elements in therapeutic applications using pulse trains instead of single pulses is useful from the point of continuous firing of focal points. Besides in imaging applications, although a single pulse with adjustable pulse width is requested for ordinary 3D imaging systems, a pulse trains is useful for color Doppler imaging applications [53]. We designed two kinds of circuits for

these kinds of applications. In the first circuit, the number of pulses is controllable which means that we generate pulse train by counting the pulses. In the second circuit, the pulse train is delivered to CMUT elements whenever the circuit senses the zero to one transition.

5.4.1 Variable Pulse Count

This circuit is considered to adjust the number of pulses from 1 to 2^N. The schematic of designed programmable and controllable pulse train generator circuit for this application is shown in Figure 5.9.

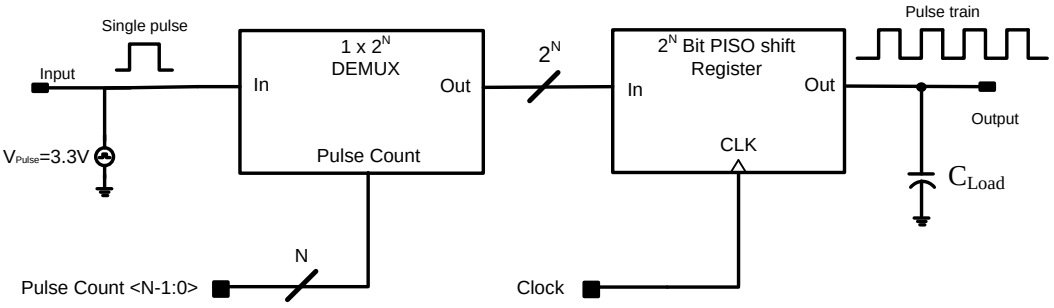


Figure 5.9 Designed programmable pulse train generator.

According to Figure 5.8, to generate pulse train by controlling the number of pulses at the output, one 1 x 2^N DEMUX (demultiplexer) and one 2^N bit PISO (Parallel Input Serial Output) shift register are used. The number of the pulses at the output of the pulse train is determined via the value of the pulse count of 1 x 2^N demultiplexer. 8-bits comparator generates the single pulse of programmable pulse train generator. In fact, the selected serial output from the delay generator circuit is fed to a 1: 2^N demultiplexer (DEMUX). The input of the N-bit data determines which output channel is routed with the input signal. The outputs of DEMUX are connected to a PISO shift register. In fact, PISO operates like a high speed serializer. Therefore, the input of the N-bit Pulse count controls the number of provided pulses ranging from 1 to 2^N. The shift register is clocked using FPGA or external controlling circuit.

5.4.2 1 x 2^N DEMUX (demultiplexer)

Figure 5.10 shows a 1x2^N demultiplexer. In designed circuit, 2^N output lines are considered for 2^N bits of PISO shift register. According to Figure 5.10, a 1x2^N demultiplexer consists of an Nx2^N decoder and combinational logics. As an example one 2x4 decoder is shown in Figure 5.11. Depends on the value of the input of decoder, demultiplexer connects the input line to one of output lines and hence, by using an N bit counter (external or internal) we can connect the input line to the output lines one after one by increasing the counter output value under a specified clock frequency. Therefore a high speed PISO shift register for single pulse serializing is needed.

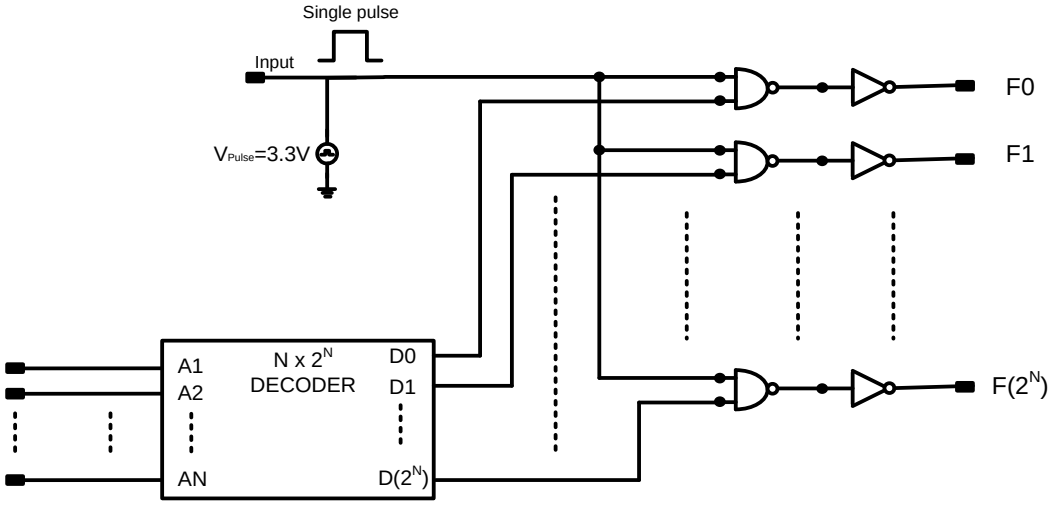


Figure 5.10 Schematic of the 1x2^N demultiplexer circuit.

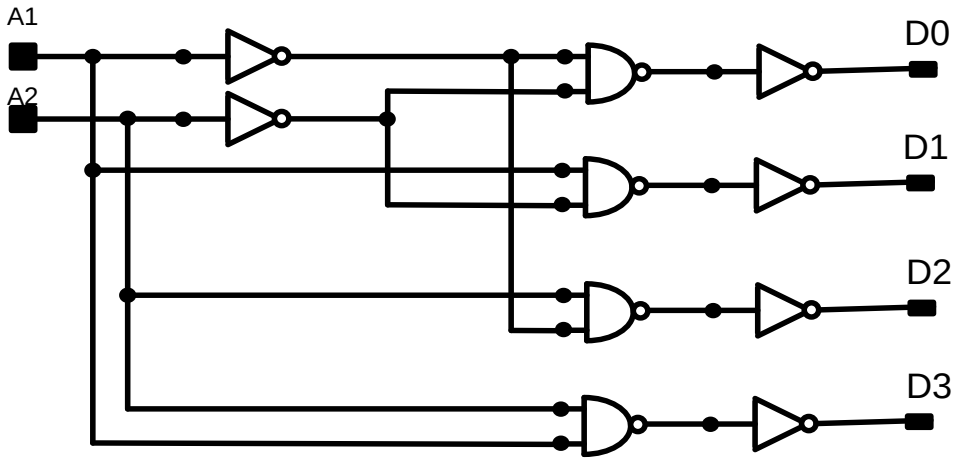


Figure 5.11 Schematic of the 2x4 decoder circuit.

5.4.3 2^N bit PISO Shift Register

Figure 5.12 shows a 2^N PISO shift register. This circuit receives N bit data in parallel mode at specified clock frequency and delivers a serialized 1-bit signal at high frequencies. According to Figure 5.12, in this circuit there are N numbers of DFFs (Edged triggered DFF) and some combinational logics. For this circuit, there is a line with the name of $\overline{WRITE}$ /SHIFT. When this line is zero, the data is written to lines and when this line is one, the data is shifted to next stage.

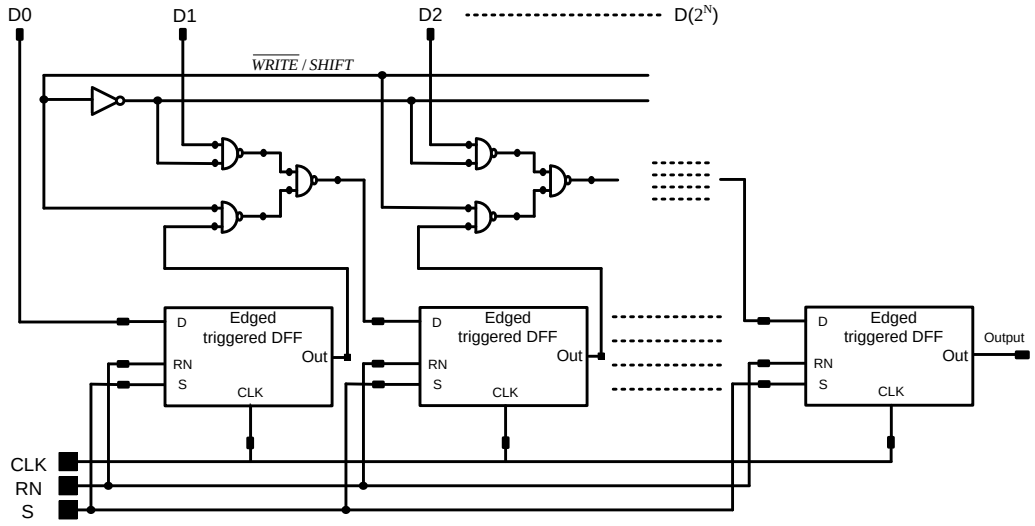


Figure 5.12 A 2^N bits PISO shift register.

As shown in Figure 5.13, an edge triggered D Flip - Flop (DFF) circuit with asynchronous reset consists of five NAND gates with three inputs and six input/output pins; four inputs (S, CLK, RN, and D) and two outputs (Q, Q-bar). The truth table of an edge triggered D Flip - Flop with asynchronous reset is shown in Table 5.13.

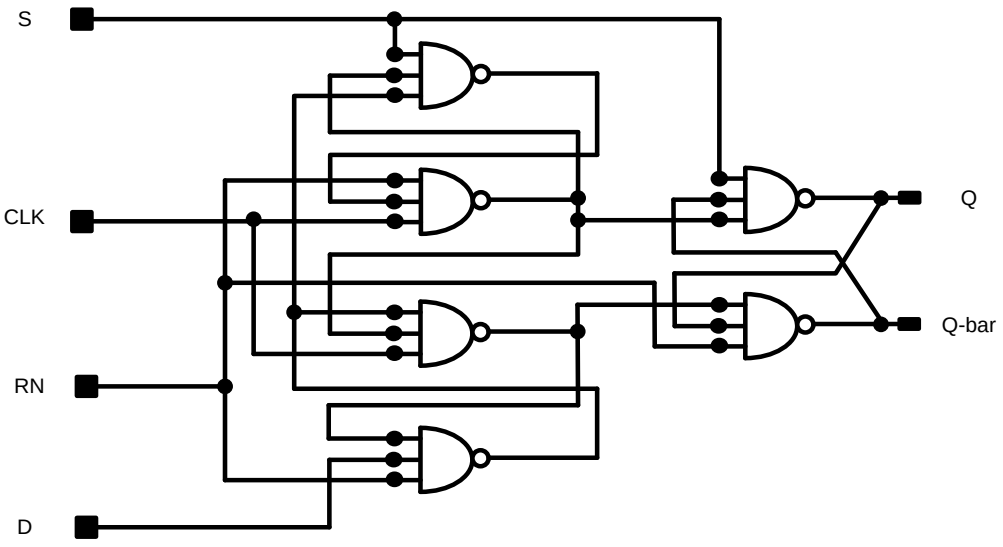


Figure 5.13 Schematic of the edged triggered D flip-flop.

Table 5.12 Truth table of an edge triggered D Flip - Flop with asynchronous reset.

CLK	RN	S	D	Q	Q-bar
X	0	1	X	0	1
X	1	0	X	1	0
X	0	0	X	1	1
1	1	1	X	Q	Q-bar
0	1	1	X	Q	Q-bar
Rising	1	1	0	0	1
Rising	1	1	1	1	0

5.4.4 Simple and precise variable pulse train generation

In previous sections, a different method for pulse train generation was explained. In this section, a simple and precise variable pulse train method is discussed. The previous topology for generating pulse trains occupies large silicon area and has much more power consumption. Although the number of pulses is fully controllable, the system is complicated and needs to be timed precisely. Figure 5.14 shows a simple and precise variable pulse train generator. This circuit decreases the power consumption and die area dramatically. On the other hand the number of pulses and pulse train frequency can be controlled externally and internally. Hence the one-shot circuit can be removed to reduce the total die area and power consumption.

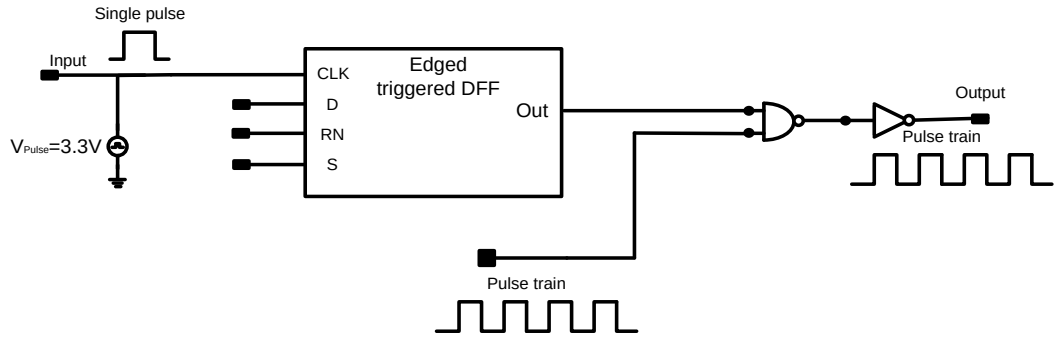


Figure 5.14 Simple and precise variable pulse train generator.

The D, RN and S ports of DFF that is shown in Figure 5.13 must be connected to VDD (3.3 V) so that when DFF senses zero to one transition, it connects D to the Out port of DFF permanently even the input of the DFF goes zero. Since first port of NAND goes high and the other one gets pulse train with specified frequency value externally or internally, the

pulse train will be copied exactly to the output of the inverter. Therefore, instead of driving CMUTs with single pulses, they can be fired using pulse trains.

Figure 5.15 shows the simulation results of the Simple and precise variable pulse train generator. As shown in this figure, when the circuit gets the enable signal, it transfers the pulse train to the output even if the input goes zero. The delay time between the single input pulse and the output pulse train is about 2.14 ns and the total power consumption of the pulse train generator is about 9.29 µw.

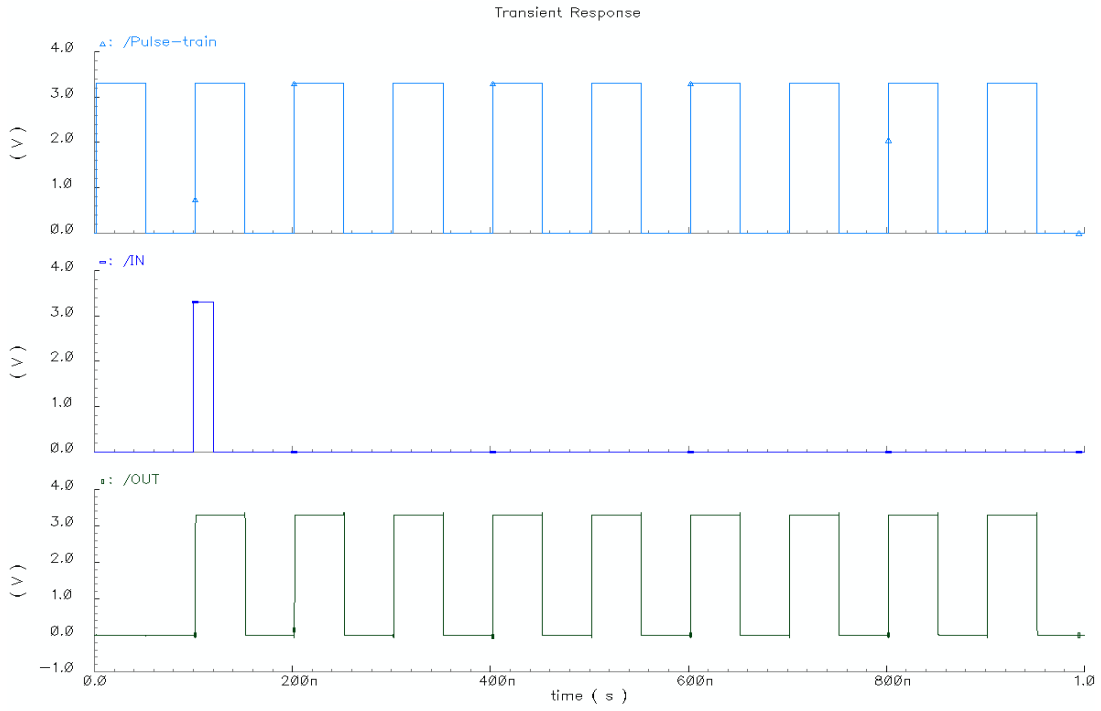


Figure 5.15 Simulation result of a simple and precise variable pulse train generator.

5.5 High voltage pulse train generator

In this chapter, providing of high voltage pulse trains with 90 or 100 volts magnitudes is discussed. According to Figure 5.16, the interfacing of pulse train generator with external frequency control and high voltage pulser circuit is considered for high voltage pulse train generation. 8-bits comparators provide the enable signal for the pulse train generators and they transfer pulse trains to the high voltage pulser circuits and finally high voltage pulse trains are generated at the output of the pulser circuit.

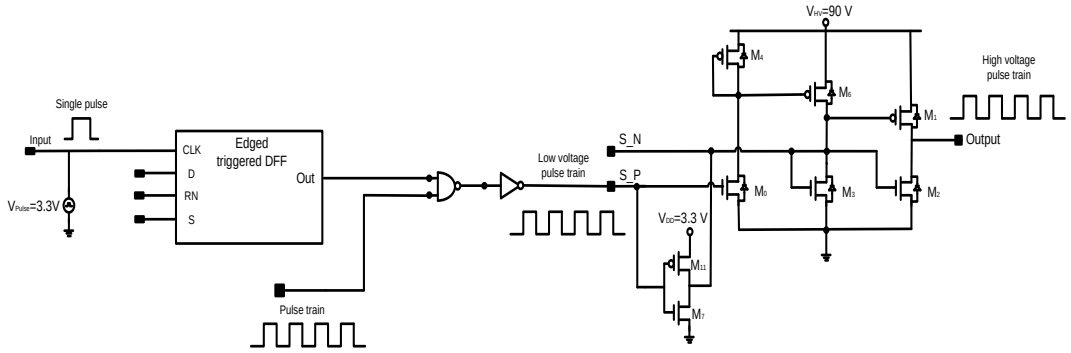


Figure 5.16 Interfacing of pulse train generator with external frequency control and high voltage pulser circuit.

Figure 5.17 shows the simulation results of high voltage pulse train generator. As can be observed, when the enable signal comes from delay lines, the pulse train generator transfers the generated pulse train by FPGA to the input of the high voltage pulser circuit and finally high voltage (90 V) pulse train is generated at the output of the circuit. The total delay time of shown circuit in Figure 5.16 from its input to output is around 8.5 ns.

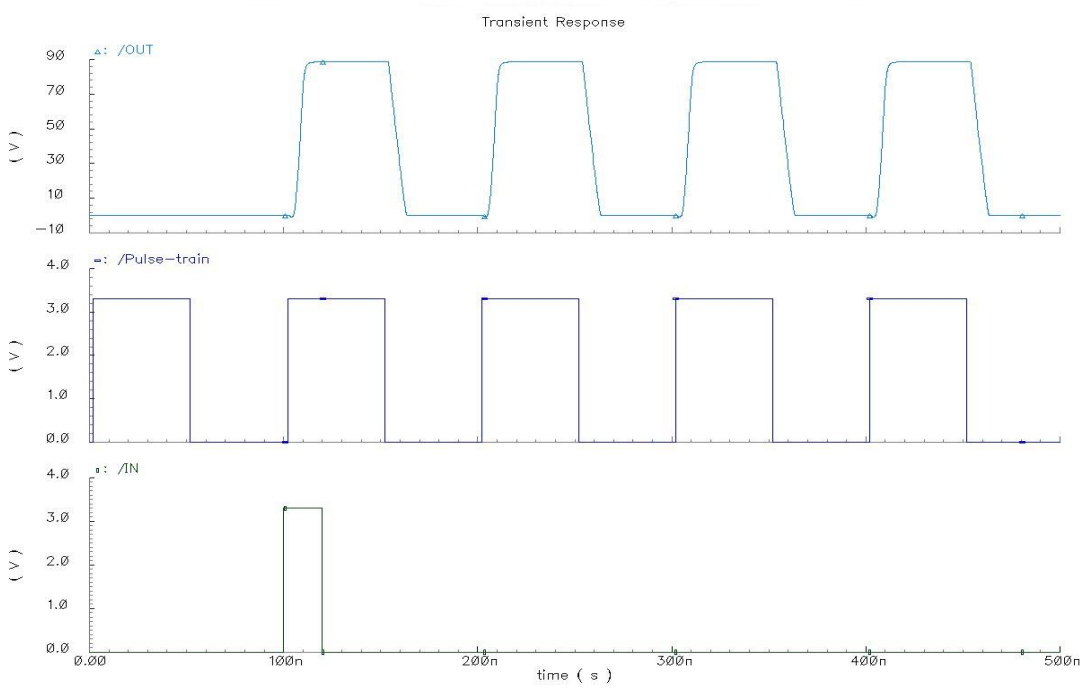


Figure 5.17 Simulation result of high voltage pulse train generator.

Each CMUT element is modeled by a 2.5 pF capacitive load and the transistors of the pulser circuits are sized to drive that value of the capacitance. Figure 5.18 shows the simulation results for firing two CMUT elements in different times when the delay information and clock frequency is 01010101 and 100 MHz, respectively. Once the output of the 8-bits

comparator goes high, the pulse train generation transfers the low voltage pulse train to the input of the high voltage circuit and finally as shown in Figure 5.18, a 90 V high voltage pulse train can be observed at the output of the high voltage pulser.

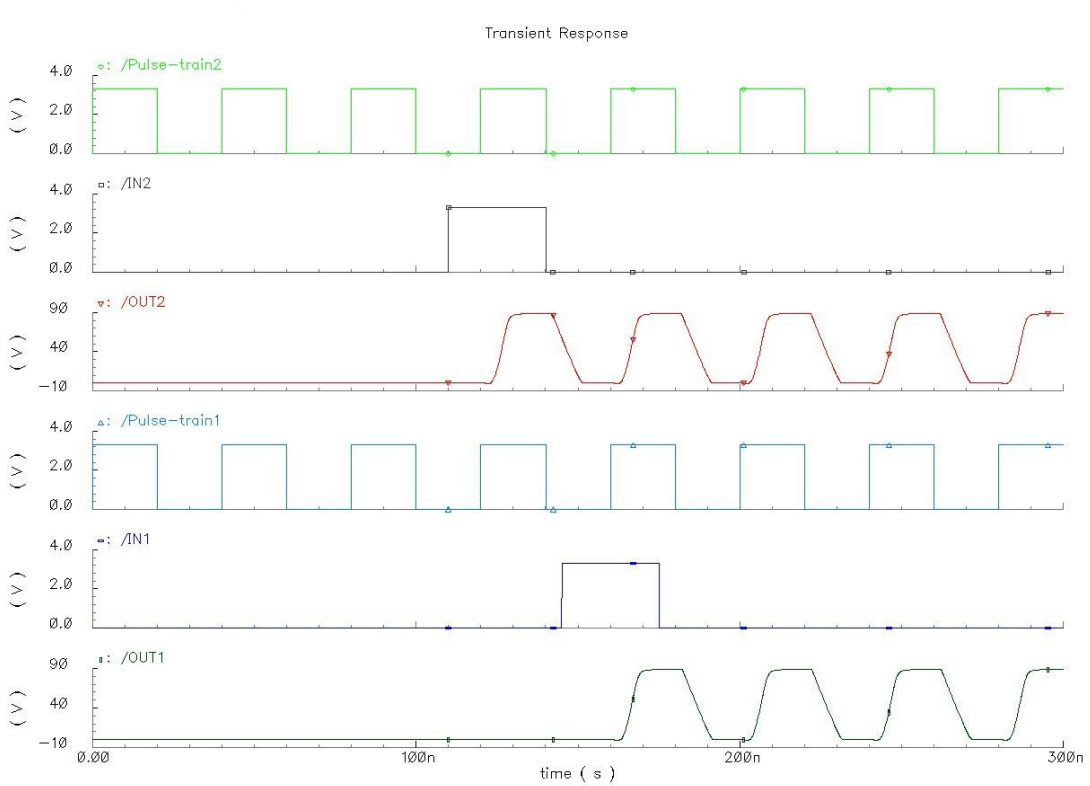


Figure 5.18 Simulation results for firing two CMUT elements in different times.

5.6 High Voltage Single Pulse Generation

In chapter 3, the schematic and simulation results of designed one-shot circuit were discussed. In this section, according to Figure 5.19 designed one-shot circuit is combined with 90 V pulser circuit. Figure 5.20 shows the simulation results of high voltage single pulse generation with adjustable pulse width using a one-shot circuit. The enable circuit generates single pulses with 10 ns or 25 ns as their pulse widths and 3.3 V magnitudes. As discussed before, the width of the pulses is controllable using an external current source via I_{SET} of one-shot circuit.

As shown in Figure 5.20, single pulses with 100 V magnitudes and 100 ns pulse widths are obtained. Delay time between the input and output of the combined one-shot and pulser circuit is 5.68 ns.

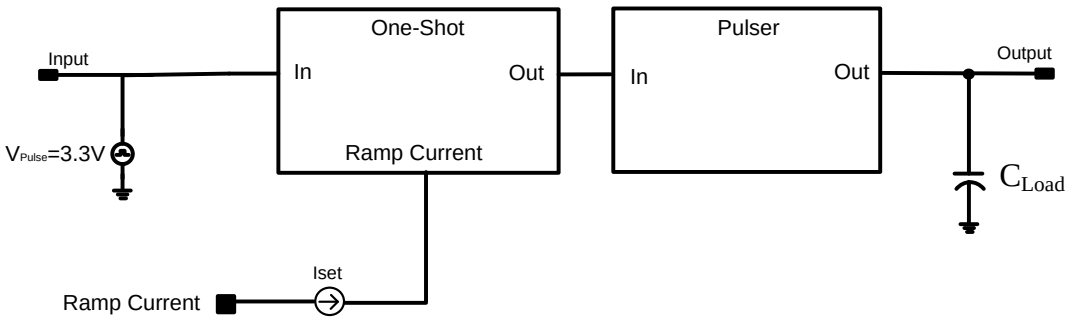


Figure 5.19 Combined one-shot and pulser circuits.

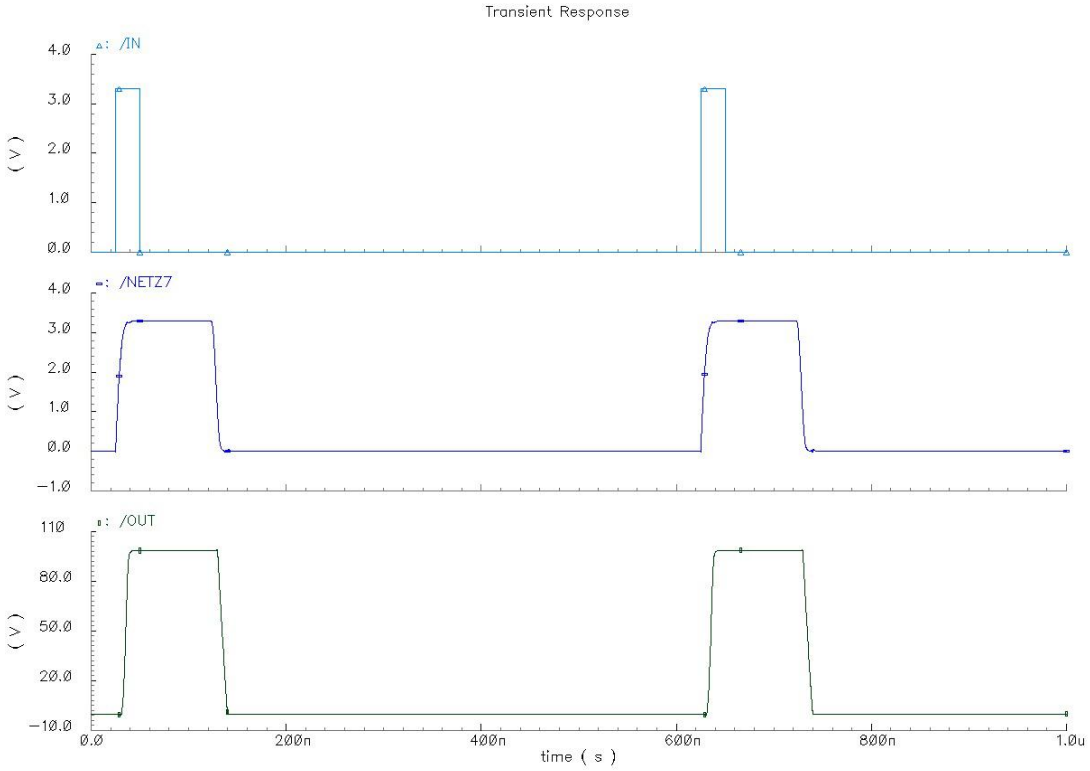


Figure 5.20 Simulation results of high voltage single pulse generation with adjustable pulse width using a one-shot circuit.

Figure 5.21 shows the complete schematic of the beam-forming circuit for firing of CMUT elements using high voltage (90 V) single pulses. A FPGA provides delay information for 8-bits shift registers. If the input ports of the 8-bits shift register and 8-bits comparator are identical, the output of the comparator goes high and after about 5.68 ns the intended CMUT element is fired by 90 V single pulses or pulse trains.

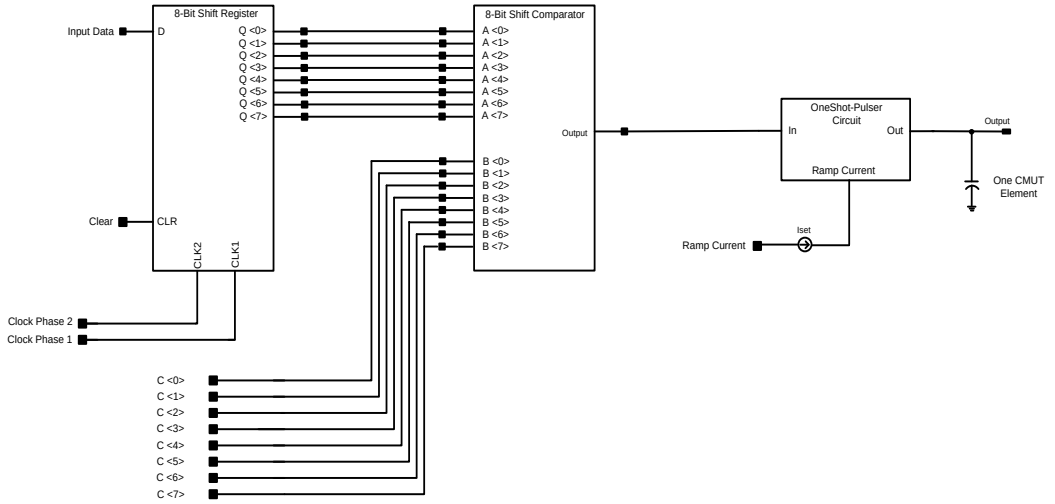


Figure 5.21 Schematic of the beam-forming circuit for firing of CMUT elements using high voltage (90 V) single pulses.

Figure 5.22 shows the simulation results of the beam-forming circuit for firing of CMUT elements using high voltage (90 V) single pulses with 100 ns widths. The circuit senses the same codes of 01010101 at 100 MHz clock frequency. These signals can be suitable for CMUT elements with 5 MHz operating frequencies.

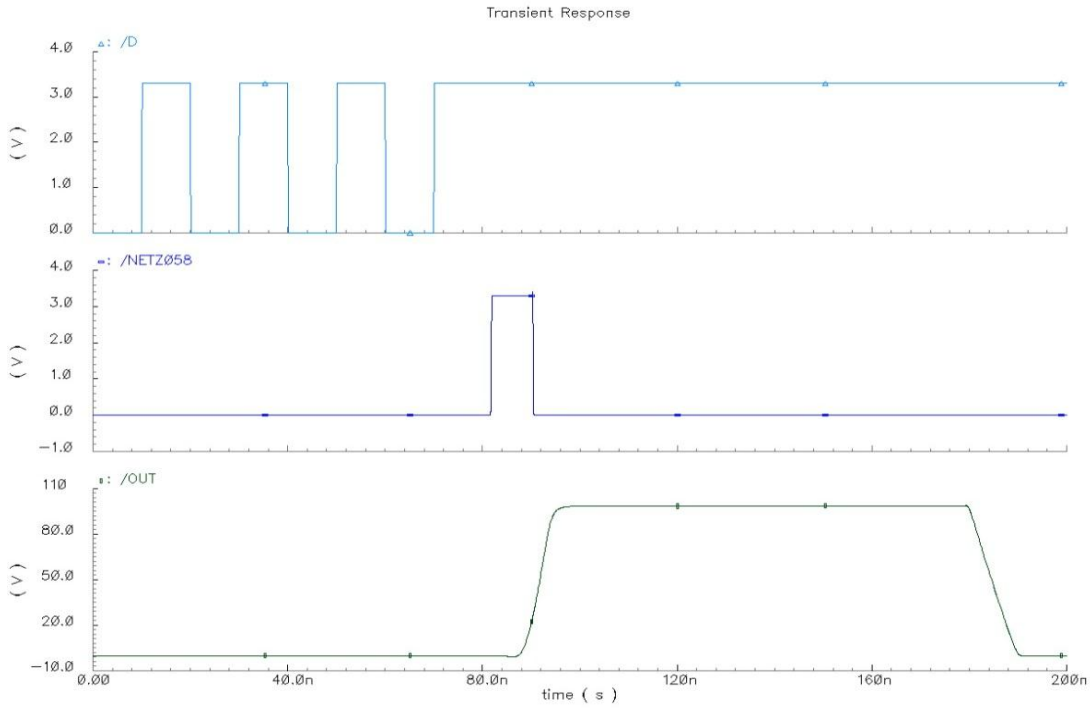


Figure 5.22 Simulation results of the beam-forming circuit for firing of CMUT elements using high voltage (90 V) single pulses with 100 ns widths.

5.7 The Layout Overview of the Ultrasound Therapeutic IC for 16X16 CMUT Array

In chapter 4, layout overview of the proposed IC for 4X4 CMUT array was presented. In this section, the layout of the designed integrated circuit for 16X16 CMUT array is explained. The same topology can be used for 16X16 CMUT array too. As shown in Figure 4.1, the layout of the final integrated circuit (IC) has been divided into driver (LV) and high voltage (HV) parts. In driver part of the integrated circuit, there are 256 separated blocks which have been considered for 256 high voltage pulser circuits. Since we have 256 CMUT elements in our final design, 256 numbers of complete blocks including LV, HV and flip-chip bonding pads should be placed in final integrated circuit. The layout of the LV and HV blocks provide each of 256 CMUT elements with an 8-bit shift register, an 8-bit comparator, an one-shot circuit, a digitally controlled oscillator with 5-bits digitally controlled delay elements, a frequency down conversion circuit, 90 V pulser circuit with HV thick oxide transistors and combinational logics. Placement and routing of these blocks in as small as possible area, demands a lot of considerations.

5.8 Layout of the High Voltage NMOS Transistor

In this section, the layout of the high voltage NMOS transistors is briefly explained. As discussed before, high voltage NMOS and PMOS transistors are used in our designed HV pulser circuits. Used HV NMOS transistors can sustain 90 V (100 V with temperature limitations) and 18 V on their drain-source and gate-source junctions, respectively. These high voltage transistors can be used with a fixed length (L) of 1.1 µm and the minimum width is 10 µm. It means that we are only allowed to change the width (W) of HV NMOS transistors in our circuits. Figure 5.23 shows the layout diagram of the HV NMOS transistor. It is recommended to use a DPWELL (Deep P-Well or Highly Doped P-Well) ring around these kinds of HV transistors. LDWELL and HDWELL mean deep N-Well (low dose) and deep N-Well (high dose), respectively. In designing of high voltage circuits, we should route the drain connections in METAL3 layers where the contacts are placed over DNWELL region. For arrayed devices, it is better to connect the gates using METAL2 or higher.

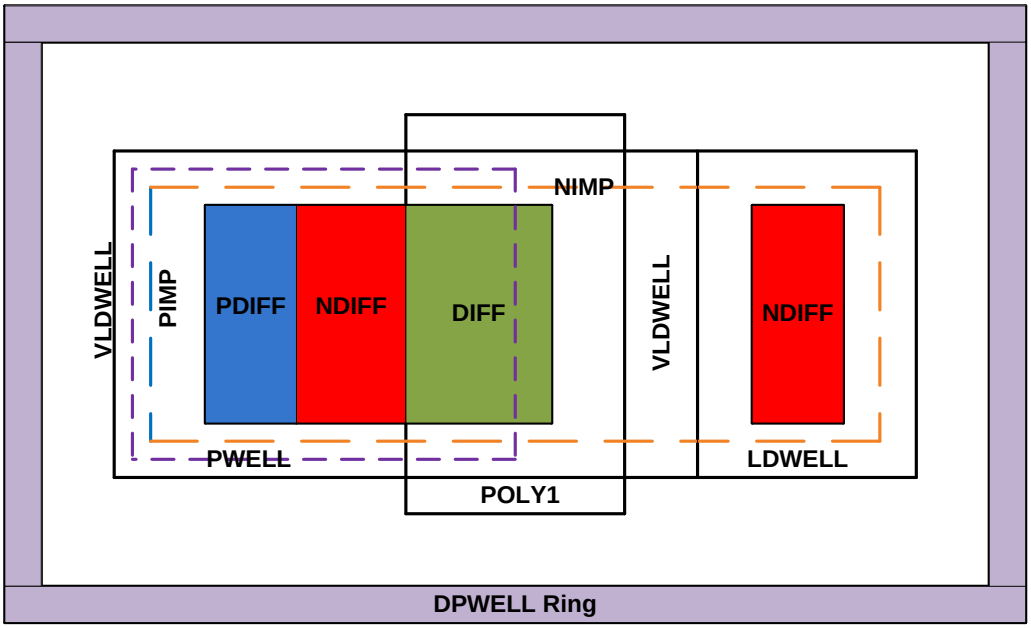


Figure 5.23 Layout diagram of the HV NMOS transistor.

Figure 5.24 shows the layout of the HV NMOS transistor with 10 µm width and 1.1 µm length. All the information of the layers can be obtained by comparing shown layout with the diagram of HV NMOS transistor (Figure 5.23). We put the bulk of the transistor and its connections in DPWELL line. Figure 6.2 shows the transistor with one gate but if we want to use large transistors with many gates, we should connect the gates using "METAL2" or top layers like "METAL3" or "METAL4". In our final layout of the high voltage pulser circuit, all of mentioned techniques have been considered carefully.

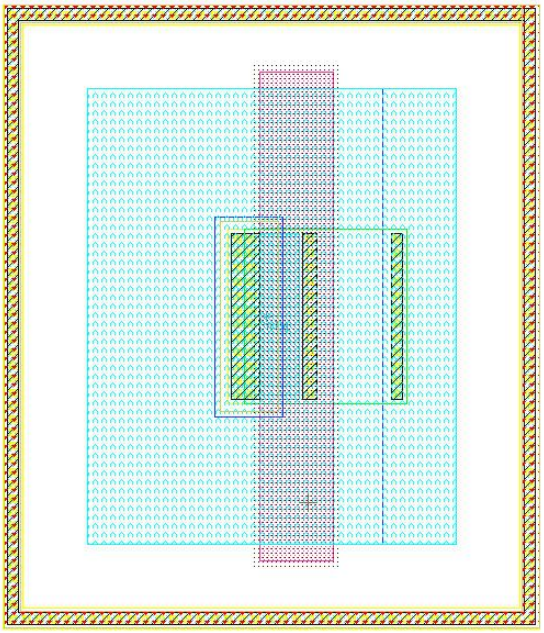


Figure 5.24 The layout of the HV NMOS transistor with 10 µm width and 1.1 µm length.

5.9 Layout of the High Voltage PMOS Transistor

In this section, the layout of the high voltage PMOS transistors is briefly explained. Used HV PMOS transistors can sustain 90 V (100 V with temperature limitations) and 18 V on their source-drain and source-gate junctions, respectively. These high voltage transistors can be used with a fixed length (L) of 2 µm and the minimum width is 10 µm. Like HV NMOS transistors, we are only allowed to change the width (W) of these transistors in our circuits. Figure 5.25 shows the layout diagram of the HV PMOS transistor. It is recommended to use a DNWELL (Deep N-Well or Highly Doped N-Well) ring around these kinds of HV transistors. Like HV NMOS transistors, in designing of high voltage circuits, we should route the drain connections in METAL3 layers where the contacts are placed over DNWELL region. For arrayed devices, it is better to connect the gates using METAL2 or higher. Table 5.13 summarizes a short description of used layers in these kinds of transistors.

Table 5.13 The brief description of some used layers in HV transistors.

Name of Used Layer	Description
DPWELL	Deep P-Well or Highly Doped P-Well
LDWELL	Deep N-Well (Low Dose)
HDWELL	Deep N-Well (High Dose)
VLDWELL	Deep, very lightly doped N-well
LDWELL	Deep, lightly doped N-well
HDWELL	Deep, highly doped N-well
MPWELL	Deeper, highly doped P-well

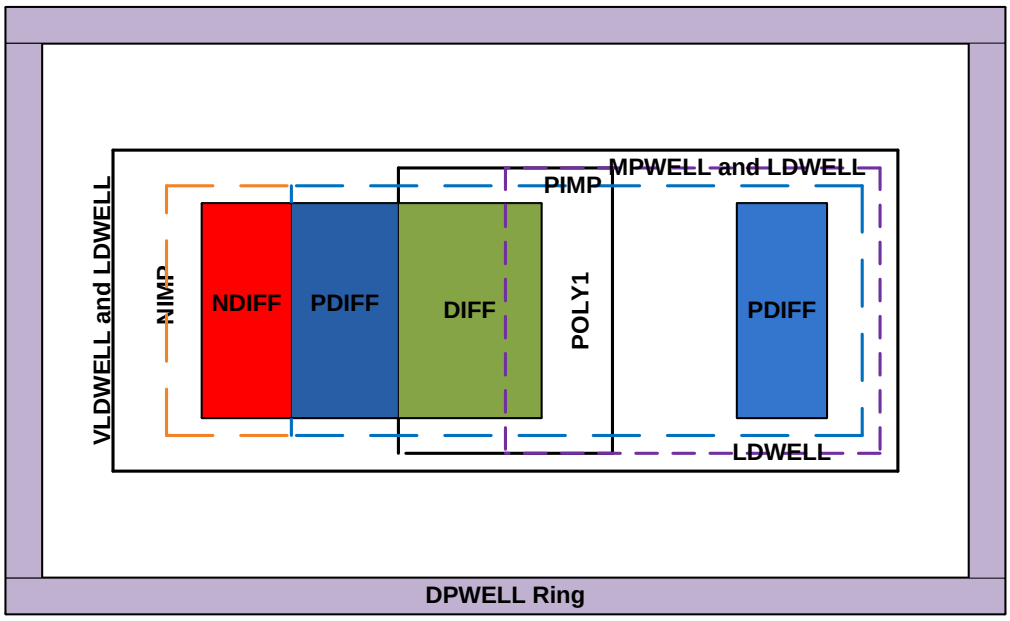


Figure 5.25 Layout diagram of the HV PMOS transistor.

Figure 5.26 shows the layout of the HV PMOS transistor with 10 µm width and 2 µm length. All the information of the layers can be obtained by comparing shown layout with the diagram of HV PMOS transistor (Figure 5.25). We put the bulk of the transistor and its connections in DPWELL line. Figure 5.26 shows the transistor with one gate but if we want to use large transistors with many gates, we should connect the gates using "METAL2" or top layers like "METAL3" or "METAL4". In our final layout of the high voltage pulser circuit, all of mentioned techniques have been considered carefully.

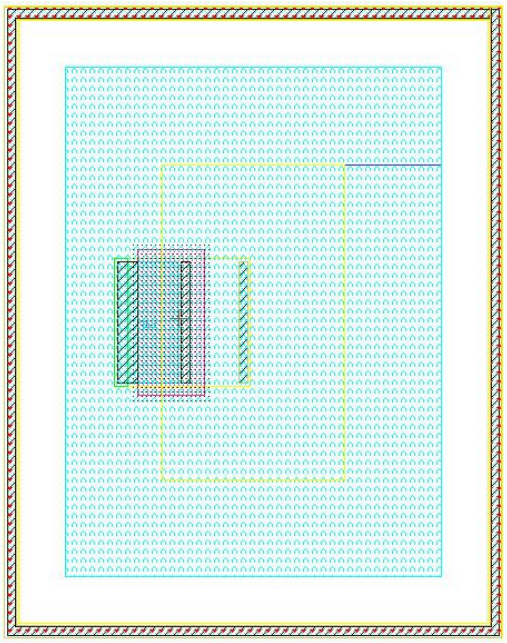


Figure 5.26 The layout of the HV PMOS transistor with 10 µm width and 2 µm length.

5.10 Layout of the High Voltage (90 V) Pulser Circuit with HVTHKOX Modules

In this chapter, a 90 V high voltage pulser was presented. On the other hand, chapter 4 explains the layout of the 45 V high voltage circuit with essential considerations. Similar techniques are used for 90 V pulser circuit. Since different types of transistors have been used in new high voltage circuit, different widths of metal lines are used for the connections of the transistors. Figure 5.27 shows the layout of the 90 V pulser circuit. The DRC (Design Check Rule), layout extraction and LVS (Layout VS Schematic) was successful for this cell. All these cells were routed according to our design. The die area of the 90 V high voltage pulser circuit is 0.042 mm^2 (170.7 µm x 247.9 µm).

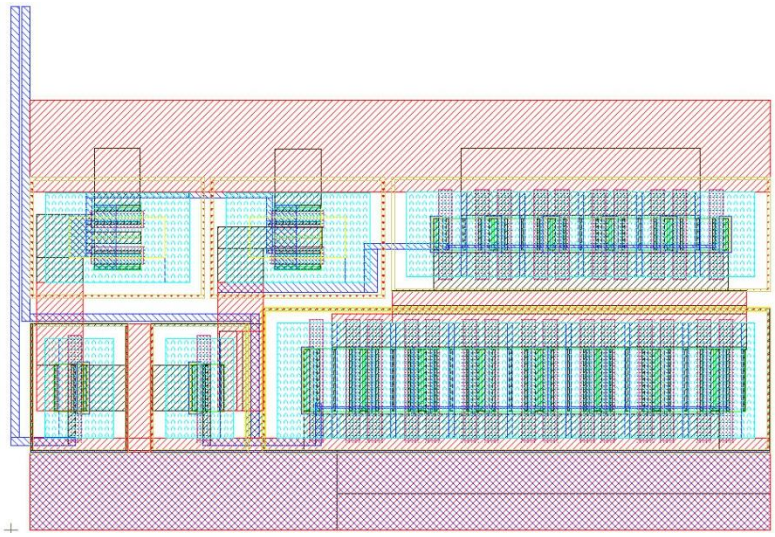


Figure 5.27 Layout of the 90 V high voltage pulser circuit.

5.11 Layout of the High Voltage Pulser Circuit with Flip-Chip Bonding Pad

In this section, the layout of the high voltage pulser is integrated with a flip-chip bonding pad in a 300 µm by 300 µm area. As we discussed in previous chapter, 256 blocks including high voltage circuits and flip-chip bonding pads in 16X16 array configuration is needed. The integration of high voltage pulsers with flip-chip bonding pads have been discussed in chapter 4 in details. The DRC (Design Check Rule), layout extraction and LVS (Layout VS Schematic) was successful for this cell. All these cells were routed according to our design. The die area of the high voltage pulser circuit with flip-chip bonding pad and two parallel METAL4 lines is 0.146 mm^2 (486.70 µm x 300 µm) and without two parallel METAL4 lines is 0.09 mm^2 (300 µm x 300 µm).

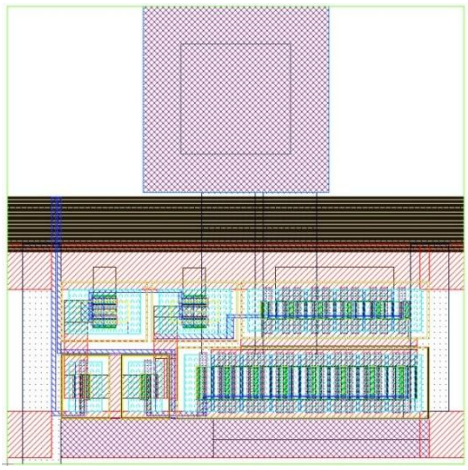


Figure 5.28 Layout of the high voltage pulser with flip-chip bonding pad in a 300 µm by 300 µm area.

As shown in Figure 5.28, there are 32 METAL1 lines that provide the driver signals of the high voltage circuits and make the connections of LV and HV parts. These lines are connected to high voltage pulsers one by one using METAL2 layers. On the other hand, wide METAL4 lines make the connections of high voltage circuits with flip-chip bonding pads.

5.12 Final Layout of the Driver part (LV) of the Chip

Eight of routed driver cells that have been shown in Figure 4.33 make the final layout for each row of the driver part of the chip. According to Figure 5.29, routed driver cells are placed next to each other and all the connections between them are completed automatically. The DRC (Design Check Rule), layout extraction and LVS (Layout VS Schematic) was successful for this cell. The die area of the final layout for each row of the driver part of the chip is 1.02 mm^2 (271.15 µm x 3766.70 µm).

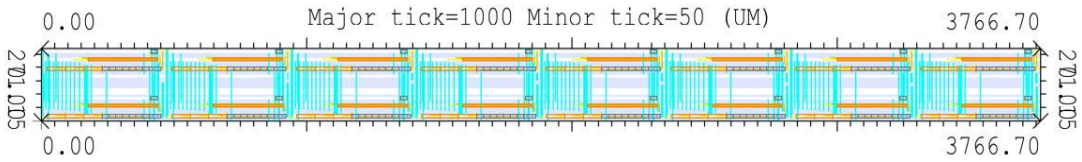


Figure 5.29 Layout for each row of the driver part of the chip.

High voltage blocks are added to driver cells of the chip. Since sixteen CMUT elements are in one row, sixteen high voltage blocks are placed next to each other in front of the driver cells of the chip. Figure 5.30 shows the final layout of the chip that is considered for one row of CMUT elements. The DRC (Design Check Rule), layout extraction and LVS (Layout VS Schematic) was successful for this cell. The die area of the chip that is considered for one row of CMUT elements is 2.32 mm^2 (271.15 µm x 8566.7 µm).

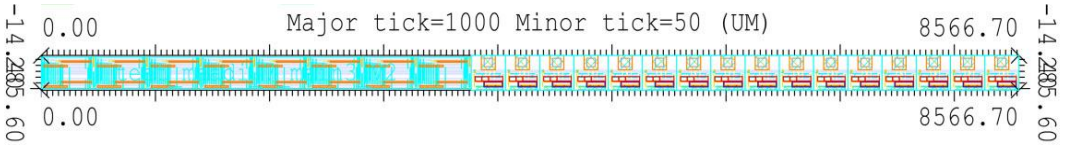


Figure 5.30 Final layout of the chip that is considered for one row of CMUT elements.

5.13 Core of the Chip

In previous sections, layouts of the low voltage and high voltage blocks with their essential considerations were discussed. In this section, sixteen final layouts of the chip (shown in Figure 5.30) that is considered for one row of CMUT elements are placed in different lines and make the 16X16 configuration. Figure 5.31 shows the layout of the chip core. It is

obvious that the core of the chip has been divided into two completely different parts: one is for driver circuitry and another for high voltage pulsers and flip-chip bonding pads. The die area for driver part is 18.08 mm^2 (4.8 mm x 3.7667 mm) and the die area for the pulser part is 23.04 mm^2 (4.8 mm x 4.8 mm). The DRC (Design Check Rule), layout extraction and LVS (Layout VS Schematic) was successful for this cell. The die area of the chip core for 16X16 CMUT elements is 41.12 mm^2 (4.8 mm x 8.5667 mm).

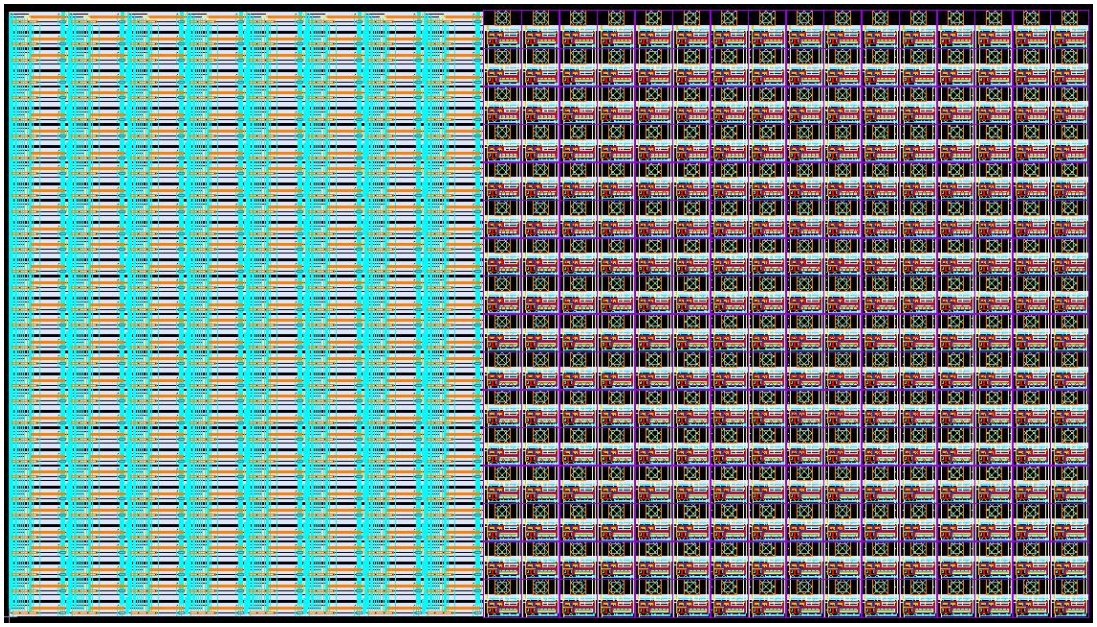


Figure 5.31 Core of the chip.

5.14 Wire Bonding Pads

In previous sections, the core of the chip for 16X16 CMUT array was prepared. In this section, the connections of the IC with external world are completed. According to our deigned chip, two kinds of bonding pads including low voltage (3.3 V) and high voltage (90 V) are needed. Low voltage pads are explained in chapter 4 completely. In high voltage part of the chip, different types of wire bonding pads with the ability of having latch-up robust HV supply I/O ESD (electrostatic discharge) protection circuit for 82V maximum operating voltage and 4kV HBM ESD robustness, have been used. In fact the ESD protection cell has only the bond pad and the ESD protection structure. These kinds of pads are used for high voltage ESD protection cell constructions. The ground lines of HV ESD pads should be continued as wide as possible. These lines should be consisting of different parallel metal layers (three parallel metal layers is recommended). Figure 5.32 shows the high voltage bonding pad of the IC with ESD protection circuit. The pad must not exceed the maximum voltage (133 V) of the protected device. The typical value of the breakdown voltage of these pads is 107 V (84 V) and the maximum ESD current of the pad is 4 A. The pad occupies a silicon area of 576.7 µm x 245.5 µm and requires ISOMOS and HVMOSTHK modules.

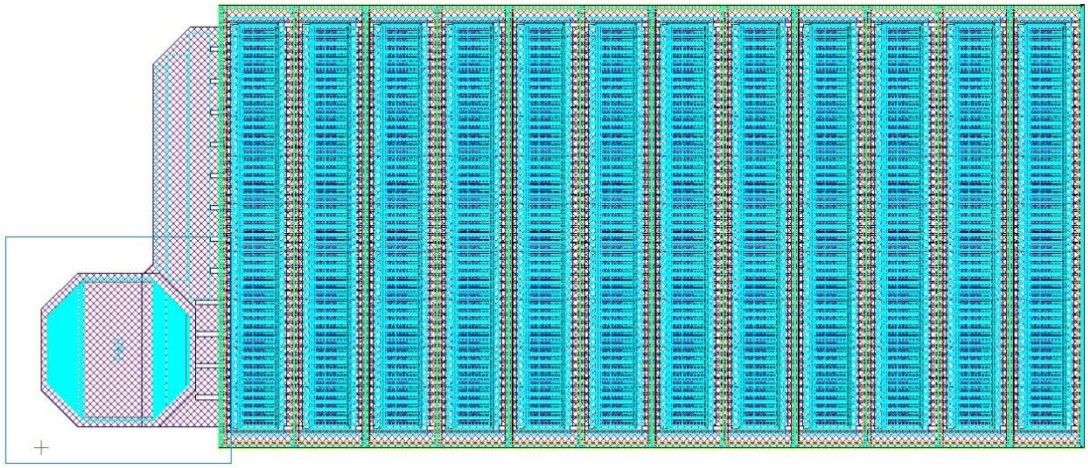


Figure 5.32 High voltage bonding pad with ESD protection circuit.

As shown in Figure 5.33, six high voltage (HVDD-type) bonding pads are used in high voltage part of the IC. These pads are placed in down side of the IC and considered for HVDD and HVGND ports of the IC.

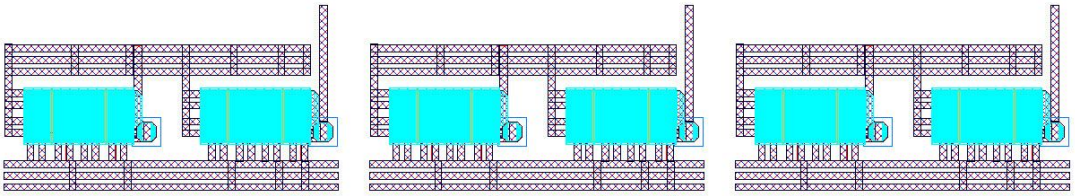


Figure 5.33 Configuration of six HV-type bonding pads.

5.15 Custom Designed Chip for 16X16 CMUTs Ultrasound Therapeutic Applications

In previous sections, all blocks of the IC for 4X4 CMUT therapeutic applications were explained. In this section, final designed chip are presented. As shown in Figure 5.34, designed IC consists of four main regions as low voltage (LV) bonding pads, custom designed high voltage (HV) bonding pads, HV bonding pads with ESD (electrostatic discharge) protection circuits, CMUT DC pads and the core of the chip. LV bonding pads provide the communication of driver part of the chip with FPGA. HV bonding pads with ESD protection provide the high voltage power supply of the pulsers, custom designed HV pads are considered for getting results from high voltage pulsers and DC pads are supposed to be bonded to CMUT transducers using flip-chip bonding pads to provide DC voltages of the CMUT elements.

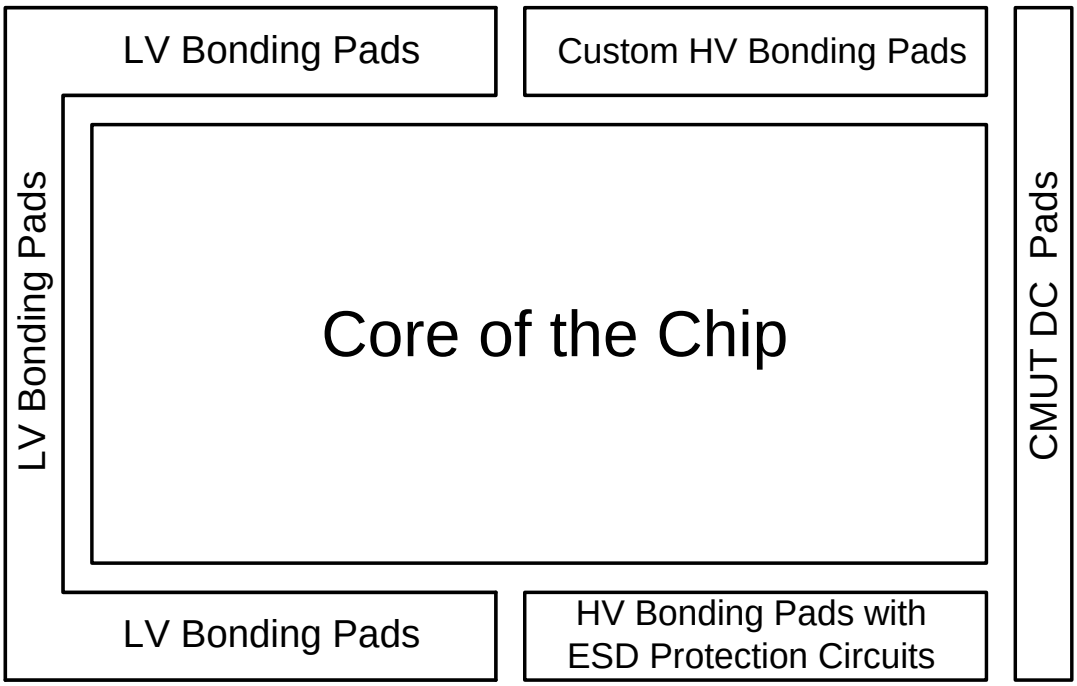


Figure 5.34 Final chip for 16x16 CMUT therapeutic applications.

Figure 5.35 shows the final layout of the designed integrated circuit for ultrasound therapeutic application. The final IC has 82 I/O LV (3.3 V) bonding pads, 16 supply bonding pads for 3.3 V, 16 HV bonding pads, 6 HV bonding pads with ESD protection circuits and one pad for DC supply of the CMUT ultrasound transducers. The DRC (Design Check Rule), layout extraction and LVS (Layout VS Schematic) was successful for this cell. The die area of the final designed chip for CMUT therapeutic application is 57.8075 mm^2 (9500 µm x 6085 µm). It is obvious that, these kinds of chips occupy great silicon areas. However, when we compare this IC with the one that was designed in Stanford University at 2009 [49], it can be observed that, our proposed interface electronics has a reasonable die area in spite of having more blocks in comparison with Stanford's work.

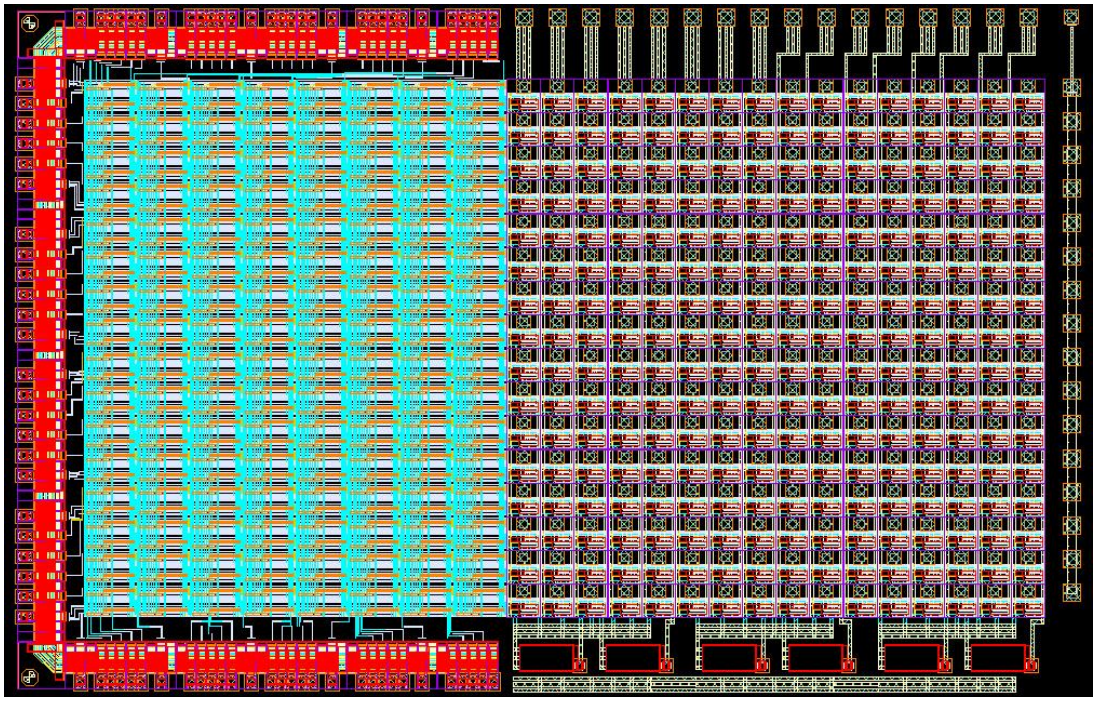


Figure 5.35 Final chip for 16X16 CMUT therapeutic applications.

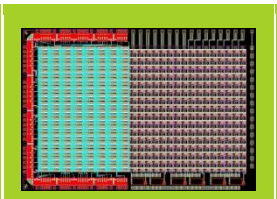
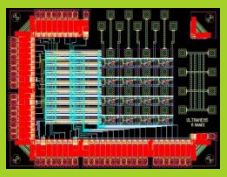
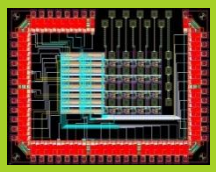
5.16 Custom Designed Chip for 4X4 CMUTs Ultrasound Therapeutic Applications with HVTHKOX Modules

Since designed 45 V high voltage pulser circuit with HVTHKOX module shows better performance in comparison with the pulser that was designed with THKOX modules, the layout of this circuit can be used to make different interface electronics for 4X4 CMUT array. However, the major drawback of this IC is that, the XFAB MPW run does not support the fabrication of the chips with HVTHKOX modules in 0.35 µm CMOS process.

5.17 Summary of the Chapter

This chapter demonstrated the schematic, design and simulation results of the proposed ultrasound therapeutic IC for 16×16 CMUT array in HV 0.35 µm CMOS technology. The same driver (LV) circuitry was used for this IC, however a different method for generating of pulse trains was proposed. The major difference of this IC is its high voltage pulsers. Using DMOS transistors with HVTHKOX modules different 100 V pulser circuits were presented. The main drawback of using HVTHKOX instead of THKOX modules is that the XFAB MPW run does not support these modules. However, various pulsers can be designed easily using HVTHKOX transistors with much more amplitudes. Meanwhile, this IC can be used for driving of large numbers of ultrasound transducers that is desirable for medical 3D imaging and therapeutic applications. In second part of this chapter, the layout of the IC for CMUT therapeutic applications in 16×16 configuration has been demonstrated. Finally, Table 5.14 summarizes three different proposed interface electronics for ultrasound therapeutic applications with CMUT arrays. Next chapter describes pulse delay calculation methods using MATLAB software.

Table 5.14 Different proposed interface electronics for ultrasound therapeutic applications with CMUT arrays.

Custom Designed Chip for Ultrasound Therapeutic Applications			
Configuration	16x16 CMUT Array	4x4 CMUT Array	4x4 CMUT Array
Area (mm^2)	≈ 58	≈ 8.7	≈ 13.5
HV Pulser	90 V (100 V) [a] HVTHKOX	45 V HVTHKOX	45 V THKOX
[a] reduced junction temperature limit @ Tj = -25ºC ... +85ºC			

CHAPTER 6

PULSE DELAY CALCULATION METHODES WITH MATLAB PROGRAM

In this chapter, two different programs for delay calculation of CMUT elements are presented. These programs have been written in MATLAB software and they have some useful specifications that are discussed in following sections. The schematics and layouts of different proposed interface electronics for 4X4 and 16X16 CMUT arrays have been demonstrated in previous chapter. As explained, there is one delay information input port in each row of interface electronics. These ports are loaded using an external control system like an FPGA according to the position of the focal point. The precise timing for generating beam-forms by focusing the ultrasound waves with the same phase on the focal point is very important and challenging. Since ultrasound transducers have different distances from the arbitrary focal point, they should be excited in different times. Hence, the delay times of firing between the transducers generate focused ultrasound beams.

6.1 Calculation of CMUT Firing Times

In ultrasound therapeutic applications, an arbitrary focal point (e.g. cancer cells inside the body) is fired with high power and energy ultrasound waves. To do this, high-voltage pulses are sent to the focal point using CMUT elements with specified delay times. Since we want to generate the most ultrasound energy at the focal point and ultrasound waves should be arrived there with the same phases by considering that each CMUT element may has different distance from the focal point, we need to fire CMUT elements in specific calculated times. In first presented topology which is shown in Figure 6.1, the focal points are considered only at the center line of the CMUT array with any distances from the center point. The array has 256 CMUT elements in a 16 by 16 structure. The CMUT elements are supposed to have a dimension of 300X300 µm hence the total dimension will be 4.8 by 4.8 mm. To find the delay time between each ultrasound element, the distance of each CMUT element from focal point is calculated.

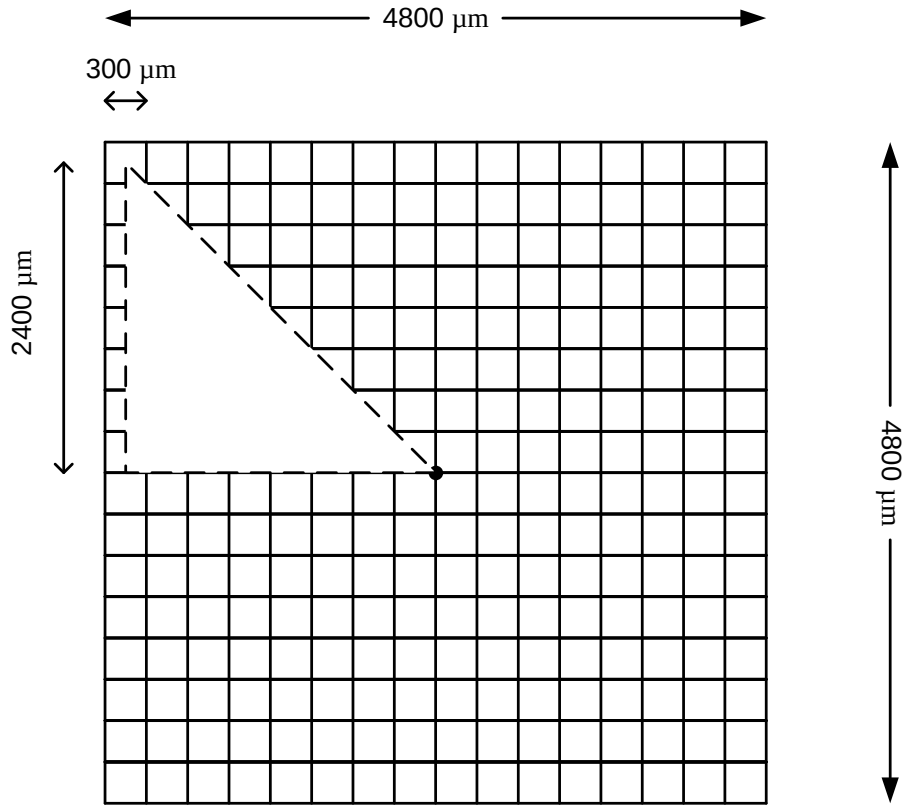


Figure 6.1 CMUT array structure and dimension.

According to Newton's second law, the delay time (Δt) between CMUT elements can be calculated by having the distance (D) of the CMUT elements from the focal point and the velocity (v) of the ultrasound wave in elastic medium like liquid or solid by the following equation:

$$D = v \times \Delta t \tag{6.1}$$

For example, the delay time between two CMUT elements can be obtained by the following equation:

$$\Delta t = \frac{D_{CMUT1} - D_{CMUT2}}{v} \tag{6.2}$$

where, D_{CMUT1} and D_{CMUT2} is the distance of CMUT1 and CMUT2 from the focal point, respectively and v is the velocity of the ultrasound wave in elastic medium. Since the velocity of the ultrasound wave and the place of the focal point are variable, a MATLAB program was prepared to calculate the delay times automatically. This program has been introduced in appendix A. According to the focal points at the center line of the CMUT array, the firing priorities of CMUT elements were calculated and shown in Figure 6.2. Since the structure of the CMUT array is symmetric, a quarter of that is considered. As can be observed from Figure 6.2, there are 32 different CMUT elements that should be fired in

different times which means that if the focal points are supposed at the center line of the array, 32 CMUT elements with different distances from the focal point are obtained. The value of the numbers increases while they are getting close to the center of the array. The elements with the same number should be fired at the same time. The distances between the center of each element and the array center are calculated precisely and the delay time of the pulses between two of the transmitted pulses can be calculated by just having the distance between the focal point and the center of the array. Next section introduces the console of the pulse delay calculation which was written in MATLAB software.

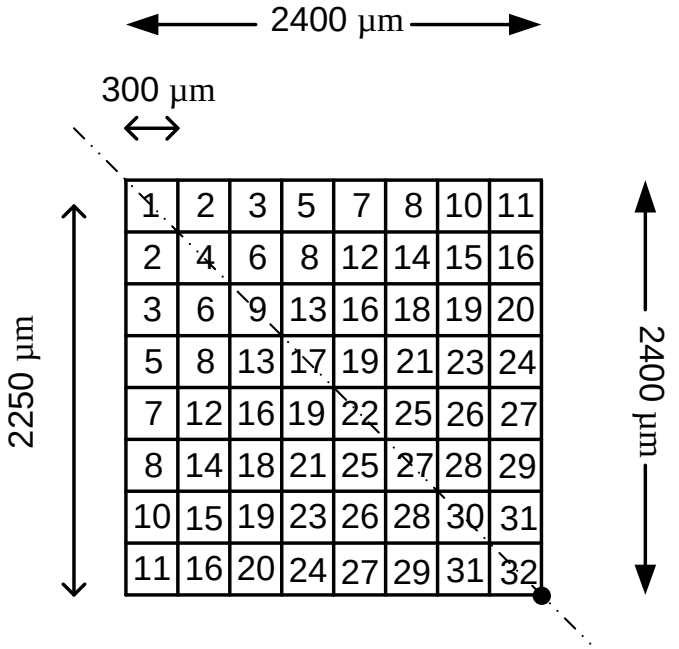


Figure 6.2 A quarter part of the 256 CMUT elements.

6.2 MATLAB Pulse Delay Calculation Program for 16X16 CMUT Array

Figure 6.3, shows the simulation console of the CMUT pulse delay calculation generated by a MATLAB program. As shown, the panel consists of some separated regions such as “CMUT Elements”, “Distance from Center Point”, “Distance from Focal Point”, “Pulse Delay”, “Properties” and “Results” for representing the elements firing priorities in a quarter part of the array.

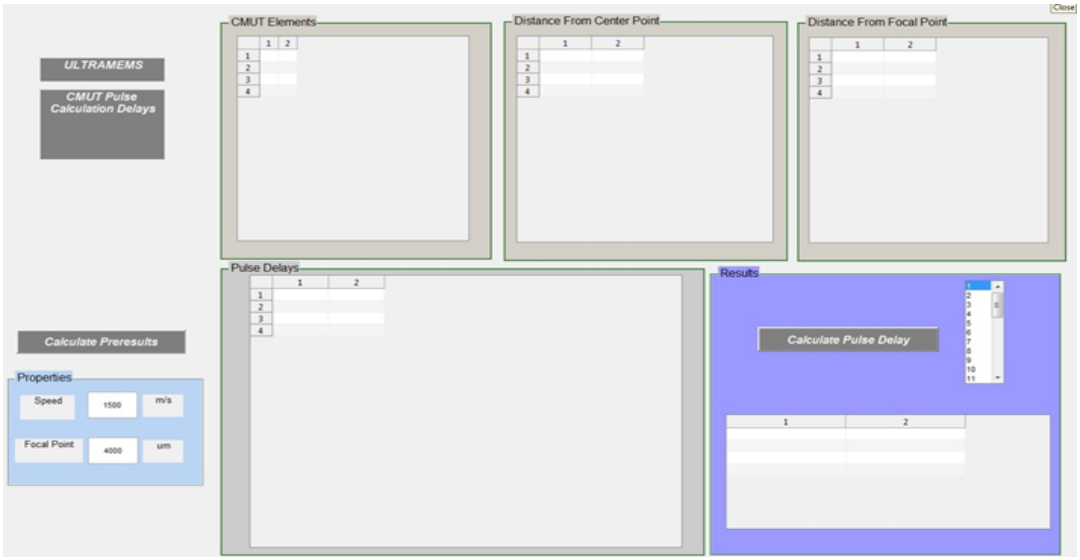


Figure 6.3 Console of the CMUT pulse delay calculation program.

The speed of the ultrasound wave (m/s) and the distance of the focal point from the array center (µm) are given from the "Properties" section of the console. After pressing the "Calculate Preresults" button, the priority of all CMUT elements for excitation with their distances from the focal point and the delay values between transducers are calculated precisely. For example, the first CMUT element in [1,1] position is placed at the distance of 3146.6 µm from the center point and is at the distance of 5089.3 µm from the focal point, if the focal point is at the distance of 4 mm from the array center. Figure 6.4 shows the program results when the speed of the ultrasound wave is 1500 m/s and the focal point is placed at the distance of 4000 µm from array center. To facilitate the imagination of the firing system, the priority of each CMUT element is shown by its own number at "CMUT Element" section.

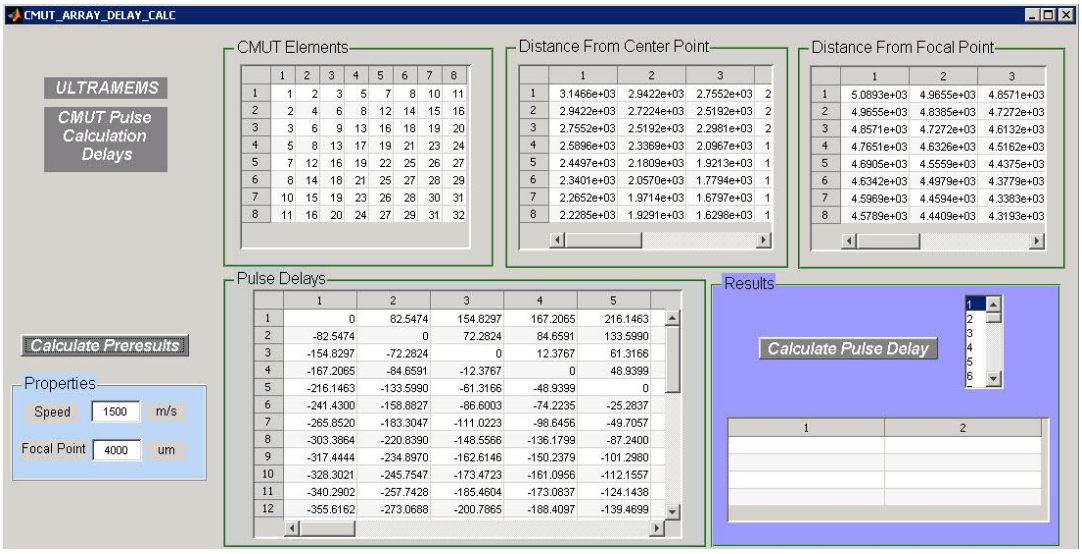


Figure 6.4 Pulse delay calculation when the velocity of the ultrasound wave is 1500 m/s and the focal point is at the distance of 4000 µm form array center.

As explained, the "Pulse Delay" section indicates the delays of pulses that should be taken into account between each CMUT pairs in driving of the final interface electronics using FPGA. For example, the "Pulse Delay" panel shows that if the first CMUT element which is in [1,1] position is fired in time zero with 1500 m/s as ultrasound wave speed, the second CMUT elements which are at [1,2] and [2,1] positions should be fired after 82.5474 ns.

To find the firing delay time between two selected CMUT elements, we need to select one of them from "CMUT Elements" panel and the next one from "Results" panel. After pressing "Calculate Pulse Delay" button, the results will be shown there. For instance, when we want to know how much delay should be considered between the pulses of the 16th and 28th CMUT elements. We should select the 16th CMUT from the "CMUT Elements" panel and 28th from the "Results" panel and finally as shown in Figure 6.5, we need to press "Calculate Pulse Delay" button in "Results" panel.

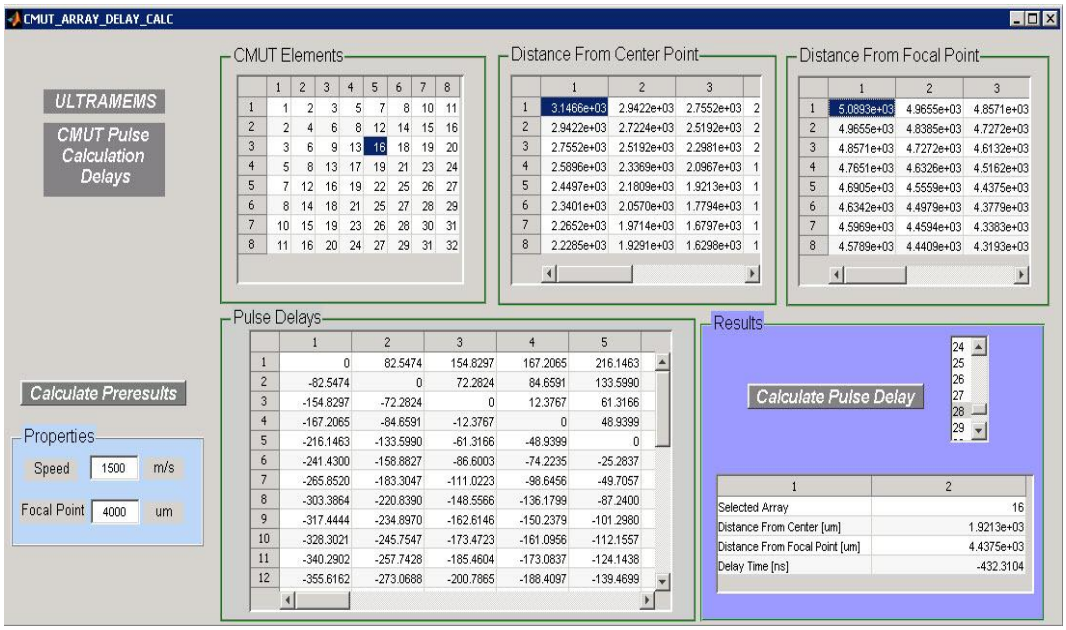


Figure 6.5 Pulse delay calculation between 16th and 28th CMUT elements.

As shown in the Figure 6.6, the "Results" panel presents selected elements, distance from center and focal point in µm, and the delay time in ns. In presented example, the delay between the firing times of 16th and 28th CMUT elements is 432.3104 ns.

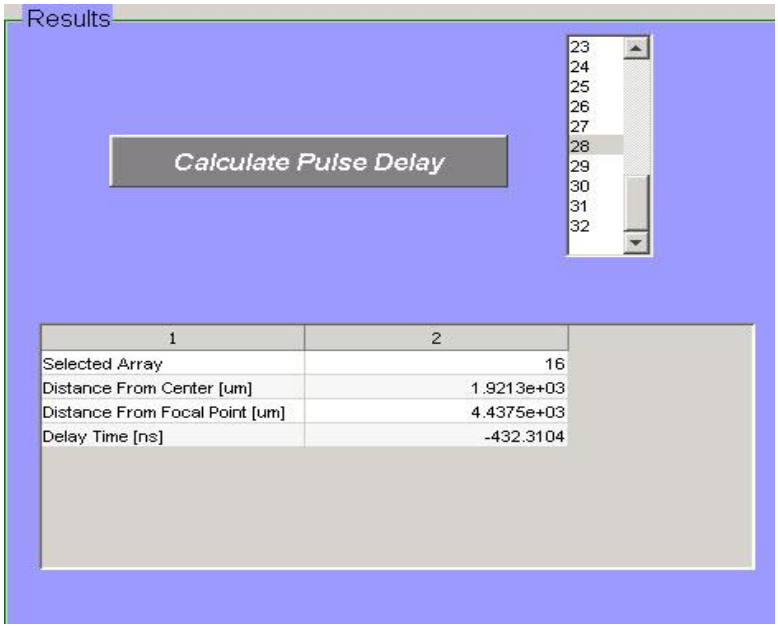


Figure 6.6 Panel of results for pulse delay calculation between 16th and 28th CMUT elements.

6.3 Beam-forming and Pulse Delay Calculation Software for 4X4 CMUT Array with Arbitrary Focal Points

In a fully populated two dimensional (2D) CMUT arrays like the one considered in this thesis work, a focused beam of ultrasound wave is acquired by electrically exciting the array elements in a pre-determined sequence. This software focus on simulation of interface electronics for 4X4 CMUT array where the pre-determined sequence is generated by an FPGA. The user specifies the focal point coordinates (x,y,z) then the software computes the delays per CMUT element and generates the expected code that the FPGA should send to the shift registers. The FPGA code is displayed in binary, the delays are plotted in a bar graph and the excitation sequence is shown by animation. Similar to the previous software, this one is also written in MATLAB program.

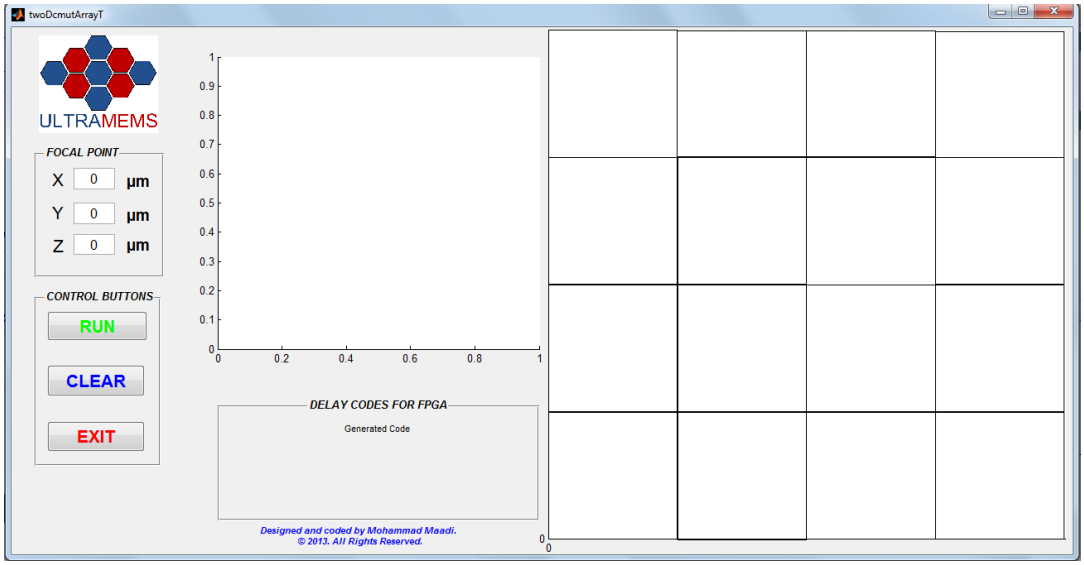


Figure 6.7 Console of the beam-forming and pulse delay calculation program for 4X4 CMUT array with arbitrary focal points.

As shown in Figure 6.7, the interface program consists of a control section, axes, delay codes for FPGA and CMUT elements area. The control section including the focal point entry fields and the control buttons allows the user to specify the coordinate of the focal point of the beam using (x,y,z) Cartesian system. The x and y values indicate the position of the focal point on the plane of the CMUT elements while the z value specifies the position orthogonally above the plane of the CMUT elements. The control button RUN is used to execute the program, CLEAR is used to rest the program for new entry, and EXIT is considered for closing the program. "Axes" region displays bar graphs of delays with respect to the trigger priority of the CMUT elements. The codes that should be generated by the FPGA for appropriate CMUT element selection process is displayed in "DELAY COES FOR FPGA" section. CMUT elements area consists of a 4X4 array of squares representing the 16 CMUT elements. The squares assume a certain color accompanied by a numerical representation for element priority.

6.4 How the Program Works

The program reads the values of (x,y,z) fields specified by the user in micrometers and interprets them as the x, y, z distance from the reference corner to the focal point. The program then computes the time it takes an ultrasound wave reach the focal point from each CMUT element in the array. Based on the calculated timings, the program generates the beam forming delays to be introduced during the triggering of the CMUT elements. A predetermined sequence is then formulated from the delays and the code expected from the FPGA is generated. The beam forming delays are plotted in bar graphs, the code expected from the FPGA are displayed in binary code while the triggering sequence is displayed by color code and the corresponding priority number on each CMUT element. For providing a better outlook, an example is presented. In this example the simulation was performed for a position of 1000 µm above the plane of the CMUT array and the values of x and y is 750

and 450 µm, respectively. The computed beam-forming delays are summarized in Table 6.1. As can be observed from this table, if the first CMUT elements are excited at the time of zero, the next elements are supposed to be fired after 69.694 ns. For assumed focal point, we need to generate five different delay times.

Table 6.1 The computed beam-forming delays.

Element triggering priority and color	Beam forming delay (µS)
1 - yellow	0
2 - light-blue	0.069694
3 - green	0.094349
4 - blue	0.14624
5 - red	0.17367
6 - white	0.20226

In addition to precise delay time calculations, the program generates the proposed digital input information that should be given to the IC by an FPGA. Since the interface electronics is loaded using four separated delay lines, four digital codes should be provided. As shown in Figure 6.8, D0, D1, D2, D3 correspond to digital delay code for the four rows of CMUT elements from top to bottom. Each nibble corresponds to least significant nibble to be shifted into the shift register content for the corresponding element in the ASIC.

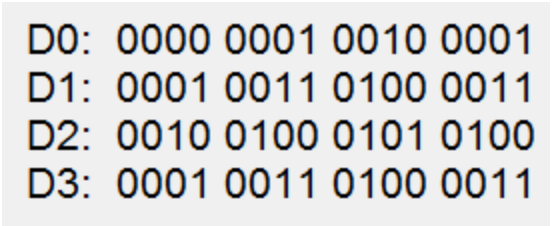


Figure 6.8 The proposed digital input information provided by an FPGA.

As shown in Figure 6.9, the triggering sequence is indicated by turning on a specific color and corresponding priority number. As can be observed, six different delay times must be generated for considered focal point.

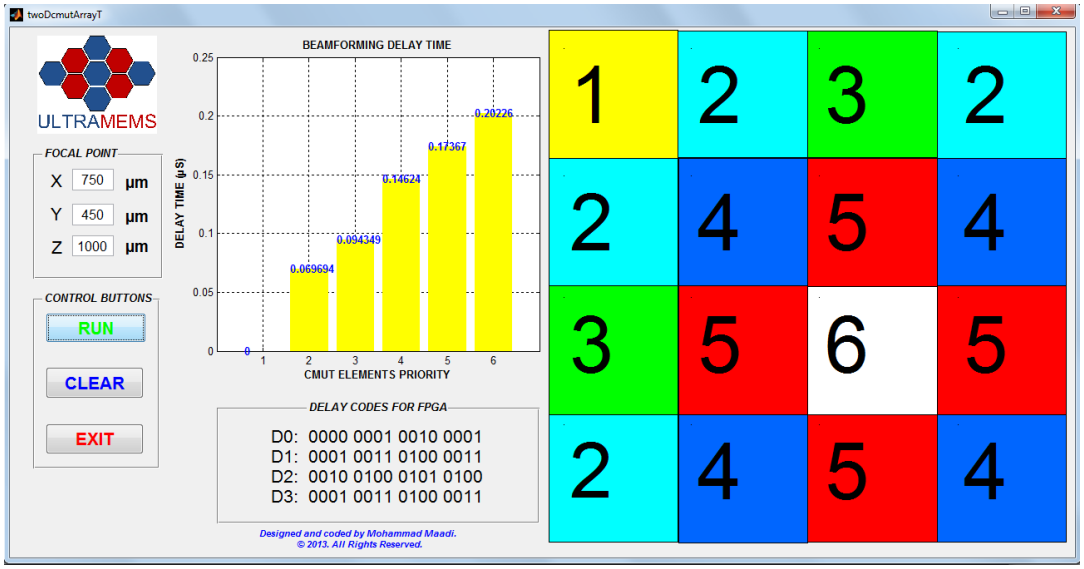


Figure 6.9 The output of the beam-forming and pulse delay calculation program for the focal point of (X = 750µm, Y = 450 µm, Z = 1000 µm).

6.5 Summary of the Chapter

In this chapter, two different MATLAB programs have been explained. The first program has been proposed for 16X16 CMUT array while the second one was designed for 4X4 CMUT array. The major purpose of these programs is calculating delay times for generating different beam-forms using ultrasound elements. In the first program, the focal point has been considered just in the center line of the array while the second one accepts any values for the Coordinate of the focal point. After entering the coordinate of the focal point in the second program, the different delay times for firing of CMUT elements are displayed in bar graphs. Moreover, the program generates the proposed digital input information that should be given to the IC by an FPGA.

CHAPTER 7

CONCLUSIONS AND FUTURE WORKS

In this research, highly flexible and controllable beam-form generator for capacitive micromachined ultrasound transducers (CMUTs) have been designed and presented. The aim of the beam-form generator is to generate 3D beam-forms by excitation of CMUTs for real ultrasound therapeutic applications. However, designed integrated circuit can be used as transmitter part of the real time 3D imaging applications. The proposed interface circuitry can be merged with ULTRAMEMS designed CMUTs with the membrane of diamond for final system development.

Results and accomplishments of this research are listed as following:

1. A detailed and comprehensive thesis work has been made on the required building blocks of the interface electronics and their design considerations which are needed for high flexible and controllable beam-form generator for capacitive micromachined ultrasound transducers (CMUTs). A state-of-the-art literature review has been proposed for all of the required blocks to categorize the available designs and highlights the missing points in the literature for each needed block.

2. New designs are proposed for high flexible and controllable single pulse and pulse train generators to adjust the widths of the pulses or the frequencies of the pulse trains for various ultrasound transducers with different operating frequencies. These blocks have been used at the same chip to provide different kinds of pulses for various medical applications. In final stage, the amplitudes of the provided low voltage (LV) signals have been increased by high voltage pulsers. The performance comparison of these architectures has also been made with previous works to show the improvements in our designs and show the possibility of highly flexible and controllable beam-forming circuitry.

3. Three different kinds of complete ultrasound therapeutic IC including 8-bit shift registers, 8-bit comparators, one-shot circuits, digitally controlled oscillators (DCOs) with 5-bit digitally controlled delay elements (DCDEs), frequency down conversion (FDCs) circuits and high voltage (HV) pulsers, has been designed in XFAB HV 0.35 µm CMOS technology. All of the proposed chips are provided by the same driver circuitry however, the high voltage blocks of them utilize different modules or transistors and generate

different outputs. The first and second designed interface electronics has been designed for 4X4 CMUT array. The high voltage pulser of the first IC has been designed using THKOX module while the second one uses HVTHKOX module in its pulsers. However, both of them produce single pulses or pulse trains with 45 volts amplitudes. The third proposed interface electronics has been designed for 16X16 CMUT array which generates high voltage signals with 100 volts magnitudes using HVTHKOX modules. The simulation results of all proposed ICs show a suitable solution for next generation MEMS-based capacitive micromachined ultrasound transducers (CMUTs) in ultrasound medical applications.

4. Part of the results of this work has been presented in 12th international conference of MUT (micromachined ultrasound transducer). Also, based on the achieved results, one journal paper has been recently submitted to IEEE TRANSACTIONS ON ULTRASONICS, FERROELECTRICS AND FREQUENCY CONTROL (UFFC) Journal.

Since this project was the first conducted research in interface electronics design for ultrasound therapeutic applications based on CMUTs, there is currently a high potential of research on it. A comprehensive list of future work is:

1. The final designed IC has been sent for fabrication to XFAB MPW run but since the die areas of these kinds of chips are dramatically large, they are too costly. Hence, we applied for a TUBITAK project to get the budget of fabrication. The fabricated IC's will be bonded to new designed CMUTs using flip-chip bonding pads and tested with FPGA boards.

2. Two different designed ASIC in XFAB HV 0.35 µm CMOS technology is ready for fabrication. The fabricated IC's can be integrated with new designed CMUTs.

3. Developing of the real-time ultrasound 3D imaging applications can be implemented by adding receiver circuitry including low noise amplifiers (LNAs) to proposed interface electronics easily.

4. Designed interface electronics can be integrated with different structures of CMUT arrays such as ring mode arrays for different applications.

5. Since CMUT elements show various responses for different types of signals such as pulse, sinusoid and triangular, in new interface electronics high voltage pulsers can be replaced with new circuits for providing different kinds of high voltage signals to CMUT elements.

REFERENCES

[1] E. S. Ebbini, R. Seip, P. Vanbaren, O. Haddadin, C. Simon, and Y. Y. Botros, *Therapeutic ultrasound*, John Wiley & Sons, Inc, 1999.

[2] B. T. Khuri-Yakub, and Ö. Oralkan, "Capacitive Micromachined Ultrasonic Transducers for Medical Imaging and Therapy," *Journal of micromechanics and microengineering*, vol. 21, no.5, 054004, 2011.

[3] I. Ladabaum, B. T. Khuri-Yakub, D. Spoliansky, and M. I. Haller, "Micromachined Ultrasonic Transducers (MUTs)," *IEEE Proce. Ultrason. Symp.*, vol. 1, pp. 501–504. nov. 1995.

[4] J.S. McIntosh, D.A. Hutchins, D.R. Billson, T.J. Robertson, R. A. Noble and A. D. R. Jones, "The Characterization of Capacitive Micromachined Ultrasonic Transducers in Air," *Ultrasonics*, vol. 40, no. 1, pp. 477-483, 2002.

[5] M.I. Haller, B.T. Khuri-Yakub, "A Surface Micromachined Electrostatic Ultrasonic Air Transducer," *IEEE Trans. Ultrason. Ferroelectr. Freq. Contr.*, vol. 43, no. 1, pp. 1–6, 1996.

[6] I. Ladabaum, X. Jin, H.T. Soh, A. Atalar, B.T. Khuri-Yakub, "Surface Micromachined Capacitive Ultrasonic Transducers," *IEEE Trans. Ultrason. Ferroelectr. Freq. Contr.*, vol. 45, no. 3, pp. 678–690, 1998.

[7] P.C. Eccardt, and K. Niederer, "Micromachined Ultrasound Transducers with Improved Coupling Factors from a CMOS Compatible Process," *Ultrasonics*, vol. 38, no. 1, pp. 774–780, 2000.

[8] X. Jin, I. Ladabaum, F. L. Degertekin, S. Calmes, and B. T. Khuri-Yakub, "Fabrication and Characterisation of Surface Mi- Cromachined Capacitive Ultrasonic Transducers," *IEEE J. Micro-electromech. Syst.*, vol. 8, no. 1, pp. 100–114, 1999.

[9] J. W. Hunt, M. Arditi, and F. S. Foster, "Ultrasound Transducers for Pulse-Echo Medical Imaging," *IEEE Trans. Biomedical Engineering*, vol. 30, no. 8, pp. 453-481, Aug. 1983.

[10] A. Safari and E. K. Akdogan, "Piezoelectric and Acoustic Materials for Transducer Applications," New York, Springer, 2008.

[11] J. Curie, and P. Curie, "Developpement par pression de l'eletricite polaire dans les cristaux hemiedres a faces enclinees," *Compt. Rend*., vol. 91, pp. 383, 1880.

[12] F. Akasheh, T. Myers, J. D. Fraser, S. Bose, and A. Bandyopadhyay, "Development of Piezoelectric Micromachined Ultrasonic Transducers," *Sensors and Actuators A Phys.*, vol. 111, no. 2, pp. 275-287, 2004.

[13] J. J. Bernstein, S. L. Finberg, K. Houston, L. C. Niles, H. D. Chen, L. E. Cross, K. K. Li, and K. Udayakumar, "Micromachined High Frequency Ferroelectric Sonar Transducers," *IEEE Trans. Ultra. Ferroelectr. Freq. Contr.*, vol. 44, no. 5, pp. 960-969, Sep. 1997.

[14] G. Percin and B. T. Khuri-Yakub, "Piezoelectrically Actuated Flextensional Micromachined Ultrasound Transducers - II: Fabrication and Experiments," *IEEE IEEE Trans. Ultra. Ferroelectr. Freq. Contr.*, vol. 49, no. 5, pp. 585-595, May. 2002.

[15] S. H. Chang and Y. C. Tung, "Electro-Elastic Characteristics of Asymmetric Rectangular Piezoelectric Laminae," *IEEE Trans. Ultra. Ferroelectr. Freq. Contr.*, vol. 46, no. 4, pp. 950-960, Jul. 1999.

[16] J. Cho, M. Anderson, R. Richards, D. Bahr, and C. Richards, "Optimization of Electromechanical Coupling for a Thin-Film PZT Membrane: I. Modeling," *Journal of Micromechanics and Microengineering*, vol. 15, no. 10, pp. 1797-1803, 2005.

[17] H. S. Choi, J. L. Ding, A. Bandyopadhyay, M. J. Anderson, and S. Bose, "Characterization and Modeling of a Piezoelectric Micromachined Ultrasonic Transducer with a very Large Length/Width Aspect Ratio," *Journal of Micromechanics and Microengineering*, vol. 18, no. 2, 025037, 2008.

[18] P. C. Eccardt, P. Wagner, and S. Hansen, "Analytical Models for Micromachined Transducers - an Overview," *IEEE Ultrason. Sympos*., Vols. 1-5, Proceedings, pp. 572-581, Oct. 2006.

[19] P. Muralt, N. Ledermann, J. Baborowski, A. Barzegar, S. Gentil, B. Belgacem, S. Petitgrand, A. Bosseboeuf, and N. Setter, "Piezoelectric Micromachined Ultrasonic Transducers Based on PZT Thin Films," *IEEE Trans. Ultra. Ferroelectr. Freq. Contr.*, vol. 52, no. 12, pp. 2276-2288, 2005.

[20] G. Percin, "Plate Equations for Piezoelectrically Actuated Flexural Mode Ultrasound Transducers," *IEEE Trans. Ultra. Ferroelectr. Freq. Contr.*, vol. 50, no. 1, pp. 81-88, 2003.

[21] G. Percin and B. T. Khuri-Yakub, "Piezoelectrically Actuated Flextensional Micromachined Ultrasound Transducers - I: Theory," *IEEE Trans. Ultra. Ferroelectr. Freq. Contr.*, vol. 49, no. 5, pp. 573-584, 2002.

[22] G. Percin and B. T. Khuri-Yakub, "Piezoelectrically Actuated Flextensional Micromachined Ultrasound Transducers," *Ultrasonics*, vol. 40, no. 1, pp. 441-448, 2002.

[23] Z. H. Wang, J. M. Miao, and W. G. Zhu, "Micromachined Ultrasonic Transducers and Arrays Based on Piezoelectric Thick Film," *Applied Physics a-Materials Science & Processing*, vol. 91, no. 1, pp. 107-117, 2008.

[24] Z. H. Wang, N. G. Zhu, H. Zhu, J. M. Miao, C. Chao, C. L. Zhao, and O. K. Tan, "Fabrication and Characterization of Piezoelectric Micromachined Ultrasonic Transducers with Thick Composite PZT Films," *IEEE Trans. Ultra. Ferroelectr. Freq. Contr.*, vol. 52, no. 12, pp. 2289-2297, 2005.

[25] L. Q. Yao, L. Lu, Z. H. Wang, W. G. Zhu, and Y. Dai, "Exact Solution of Multilayered Piezoelectric Diaphragms," *IEEE Trans. Ultra. Ferroelectr. Freq. Contr.*, vol. 50, no. 10, pp. 1262-1271, 2003.

[26] K. Yamashita, H. Katata, M. Okuyama, H. Miyoshi, G. Kato, S. Aoyagi, and Y. Suzuki, "Arrayed Ultrasonic Microsensors with High-Directivity for In-Air Use Using PZT Thin Film on Silicon Diaphragm," *Sens. Actuators*, vol. A97–98C, pp. 302–307, 2002.

[27] Y. Mo, T. Tanaka, K. Inoue, K. Yamashita, and Y. Suzuki, "Front-end Processor Using BBD Distributed Delay-sum Architecture for Micromachined Ultrasonic Sensor Array," *J. Microelectromechanical Systems*, vol. 12, no. 4, pp. 506-512, 2003.

[28] M. I. Haller, and B. T. Khuri-Yakub, "A Surface Micromachined Electrostatic Ultrasonic Air Transducer," *IEEE Proce. Ultrason. Symp.*, vol. 2, pp 1241–1244, Oct. 1994- Nov. 1994.

[29] D. R. Chou, "Piezoelectric Micrimachined Ultrasound Transducer for Medical Imaging," *Ph.D. Thesis*, Duke University, 2011.

[30] P. C. Eccardt, and K. Niederer, "Micromachined Ultrasound Transducers with Improved Coupling Factors from a CMOS Compatible Process," *Ultrasonics*, vol. 38, no. 1, pp. 774-780, 2000.

[31] B. Bayram, Ö. Oralkan, A. S. Ergun, E. Hæggstrom, G. G. Yaralioglu, and B. T. Khuri-Yakub, "Capacitive Micromachined Ultrasonic Transducer Design for High Power Transmission," *IEEE Trans. Ultra. Ferroelectr. Freq. Contr.*, vol. 52, no. 2, pp. 326-339, Feb. 2005.

[32] G. G. Yaralioglu, A. S. Ergun, and B. T. Khuri-Yakub, "Finite-element Analysis of Capacitive Micromachined Ultrasonic Transducers," *IEEE Trans. Ultra. Ferroelectr. Freq. Contr.*, vol. 52, no. 12, pp. 2185–98, Dec. 2005.

[33] Y. Roh, and B. T. Khuri-Yakub, "Finite Element Analysis of Underwater Micromachined Ultrasonic Transducers," *IEEE Trans. Ultra. Ferroelectr. Freq. Contr.*, vol. 49, no. 3, pp. 293–298, March, 2002.

[34] A. Nikoozadeh, B. Bayram, G. G. Yaralioglu, and B. T. Khuri-Yakub, "Analytical Calculation of Collapse Voltage of CMUT Membrane [Capacitive Micromachined Ultrasonic Transducers]," *IEEE Ultrason. Sympos.*, vol. 1, pp. 256-259, Aug. 2004.

[35] G. Hayward, "The Influence of Pulser Parameters on the Transmission Response of Piezoelectric Transducers," *Ultrasonics*, vol. 23, no. 3, pp. 103-112, 1985.

[36] A. A. Vives, and A. Arnau (Eds.), "Piezoelectric Transducers and Applications," Springer, 2008.

[37] M. E. Schafer, and P. A. Lewin, "The Influence of Front-End Hardware on Digital Ultrasonic Imaging," *IEEE Trans. Sonics Ultrason*., vol. 31, no. 4, pp. 295-306, Jul. 1984.

[38] A. Ramos, J. L. San Emeterio, and P.T. Sanz, "Electrical Matching Effects on the Piezoelectric Transduction Performance of a Through Transmission Pulsed Process" *Ferroelectrics*, vol. 202, no. 1, pp. 71-80, 1997.

[39] J. G. Okyere, and A. J. Cousin, "The Design of a High voltage SCR Pulse Generator for Ultrasonic Pulse Echo Applications," *Ultrasonics*, vol. 17, no. 2, pp. 81-84, 1979.

[40] P. Mattila, and M. Luukkala, "FET Pulse Generator for Ultrasonic Pulse Echo Applications," *Ultrasonics*, vol. 19, no. 5, pp. 235-236, 1981.

[41] P. C. Eccardt, K. Niederer, and B. Fischer, "Micromachined Transducers for Ultrasound Applications," *IEEE Proce. Ultrason. Symp.*, vol. 2, pp. 1609–18, Oct. 1997.

[42] X. Cheng, D. F. Lemmerhirt, O. D. Kripfgans, M. Zhang, C. Yang, C. A. Rich, and J. B. Fowlkes, "CMUT-IN-CMOS Ultrasonic Transducer Arrays with On-Chip Electronics," *IEEE Int. Conf. Solid-State Sensors and Actuators*, pp. 1222–1225, June, 2009.

[43] Y. Tsuji, M. Kupnik, and B. T. Khuri-Yakub, "Low Temperature Process for CMUT Fabrication with Wafer Bonding Technique," *IEEE Ultrason. Symp*., pp. 551-554, Oct. 2010.

[44] I. Wygant, X. Zhuang, D. Yeh, Ö. Oralkan, A. S. Ergun, M. Karaman, and B. T. Khuri-Yakub, "CMUT Arrays with Front-end Electronics for Volumetric Ultrasound Imaging," *IEEE Trans. Ultra. Ferroelectr. Freq. Contr.*, vol. 55, no. 2, pp. 327–342, Feb. 2008.

[45] R. Wodnicki, C. G. Woychik, A. T. Byun, R. Fisher, K. Thomenius, D. S. Lin, X. Zhuang, Ö. Oralkan, S. Vaithilingam, and B. T. Khuri-Yakub, "Multi-row Linear CMUT Array Using CMUTs and Multiplexing Electronics," *IEEE Int. Ultrason. Symp.*, pp. 2696-2699, Sept. 2009.

[46] A. Nikoozadeh, et al. "Forward-looking Hntracardiac Hmaging Catheters Using Fully Integrated CMUT Arrays," *IEEE Ultrason. Symp.*, pp. 770-773, Oct. 2010.

[47] S. H. Wong, R. D. Watkins, M. Kupnik, K. B. Pauly, and B. T. Khuri-Yakub, "Feasibility of MR-Temperature Mapping of Ultrasonic Heating from a CMUT," *IEEE Trans. Ultra. Ferroelectr. Freq. Contr.*, vol. 55, no. 4, pp. 811-818, April, 2008.

[48] S. H. Wong, M. Kupnik, R. D. Watkins, K. B. Butts-Pauly, and B. T. Khuri-Yakub, "Capacitive Micromachined Ultrasonic Transducers for Therapeutic Ultrasound Applications," *IEEE Trans. Biomedical Engineering.*, vol. 57, no. 1, pp. 114–123, Jan. 2010.

[49] I. O. Wygant, N. S. Jamal, H. J. Lee, A. Nikoozadeh, Ö. Oralkan, M. Karaman, and Butrus T. Khuri-Yakub, "An Integrated Circuit with Transmit Beam forming Flip-Chip Bonded to a 2-D CMUT Array for 3-D Ultrasound Imaging," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control.*, vol. 56, no. 10, pp. 2145– 2156, Oct. 2009.

[50] G. Gurun, P. Hasler, and F. Degertekin, "Front-end receiver electronics for high-frequency monolithic CMUT-on-CMOS imaging arrays," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control.*, vol. 58, no. 8, pp. 1658-1668, 2011.

[51] Y. M. Li, R. Wodnicki, N. Chandra, and N. Rao, "An Integrated 90V Switch Array for Medical Ultrasound Applications," *IEEE conf. Custom Integrated Circuits.*, pp. 269-272, Sept. 2006.

[52] H. Ballan, and M. Declercq, " High Voltage Devices and Circuits in Standard CMOS Technoloie, Kluwer Academic Publishers," Springer, March, 1999.

[53] G. I. Athanasopoulos, S. J. Carey, and J. V. Hatfiel, "Circuit Design and Simulation of a Transmit Beamforming ASIC for High-Frequency Ultrasonic Imaging Systems," *IEEE Trans. on Ult., Ferro Elec. and Freq. con.*, vol. 58, no. 7, pp. 1320–1331, Jul. 2011.

[54] A. Moscatelli, A. Merlini, G. Cme, P. Galbiati, and C. Contiero, "LDMOS Implementation in a 0.35pm BCD Technology (BCD6)," *IEEE 12th Int. Symp. Power Semiconductor Devices and ICs,* pp. 323-326, May, 2000.

[55] N. I. Maluf, R. J. Reay, and G. T. A. Kovacs, "High-voltage Devices and Circuits Fabricated Using Foundry Cmos for Use with Electrostatic Mem Actuators," *The 8th Int. Conf. Solid-State Sensors and Actuators*, vol. 1, pp. 158-161, Jun, 1995.

[56] C. Bassin, H. Ballan, and M. Declercq, "High-Voltage Devices for 0.5-μm Standard CMOS Technology," *IEEE Electron Device Letters*, vol. 21, no. 1, pp. 40-42, Jan. 2000.

[57] P. M. Santos, M. C. Vitor Costa, Gomes, Beatriz Borges, Mario Lanca, "High-voltage LDMOS Transistors Fully Compatible with a Deep-Submicron 0.35 μm CMOS Process," *J. Microelectronics* , vol. 38, Issue. 1, pp. 35-40, Jan. 2007.

[58] R. A. Noble, R. R. Davies, M. M. Day, L. Koker, D. O. King, K. M. Brunson, A. R. D. Jones, J. S. McIntosh, D. A. Hutchins, T. J. Robertson and P. Saul, "A Cost-effective and Manufacturable route to the Fabrication of High-density 2D CMUT Arrays and Signal Conditioning electronics on the Same Silicon Substrate," *IEEE Ultrason. Symp.*, vol. 2, pp. 941-944, 2001.

[59] C. Daft, S. Calmes, D. da Graca, K. Patel, P. Wagner, and I. Ladabaum, "Microfabricated Ultrasonic Transducers Monolithically Integrated with High Voltage Electronics," *IEEE Ultrason. Symp.*, vol. 1, pp. 493-496, Aug. 2004.

[60] R. Guldiken, J. Zahorian, G. Gurun, M. S. Qureshi, M. Balantekin, C. Tekes, P. Hasler, M. Karaman, S. Carlier, and F. L. Degertekin, "P0-18 Forward-Looking IVUS Imaging Using a Dual-Annular Ring CMUT Array: Experimental Results," *IEEE Ultrason. Symp.*, vol., pp. 1247-1250, Oct. 2007.

[61] G. Gurun, M. S. Qureshi, M. Balantekin, R. Guldiken, J. Zahorian, P. Sheng-Yu, A. Basu, M. Karaman, P. Hasler and L. Degertekin, "Front-end CMOS Electronics for Monolithic Integration with CMUT Arrays: Circuit Design and Hnitial Experimental Results," *IEEE Ultrason. Symp.*, pp. 390-393, Nov. 2008.

[62] U. Guler, and A. Bozkurt, "A Low-Noise Front-End Circuit for 2D CMUT Arrays," *IEEE Ultrason. Symp.*, pp. 689-692, Oct. 2006.

[63] Y. Moghe, T. Lehmann, and T. Piessens, "Nanosecond Delay Floating High Voltage Level Shifters in a 0.35 um HV-CMOS Technology," *IEEE J. Solid-State Circuits*, vol. 46, no. 2, pp. 485-497, Feb. 2011.

[64] M. Khorasani, M. Benham, L. van den Berg, C. J. Backhouse, and D. G. Elliott, "High-Voltage CMOS Controller for Microfluidics," *IEEE Trans. Biomed. Circuits Syst*., vol. 3, no. 2, pp. 89–96, 2009.

[65] M. J. Declerq, M. Schubert, and F. Clement, "5 V-to-75 V CMOS Output Interface Circuits," *IEEE 40th Int. conf. Solid-State Circuits, Digest of Technical Papers.*, pp. 162-163, Feb. 1993.

[66] J. F. Richard, B. Lessard, R. Meingan, S. Martel, and Y. Savaria, "High Voltage Interfaces for CMOS/DMOS Technologies," *IEEE Northeast Workshop on Circuits and Systems.*, pp. 93-96, June, 2003.

[67] M. Khorasani, L. van den Berg, P. Marshall, M. Zargham, V. Gaudet, D. Elliott, and Martel, S, "Low-Power Static and Dynamic High-Voltage CMOS Level-Shifter Circuits," *IEEE Int. Symp*., pp. 1946-1949, May, 2008.

[68] Q. A. Khan, S. K. Wadhwa, and K. Misri, "A Single Supply Level Shifter for Multi-Voltage Systems," *IEEE Held jointly with 5th International Conference on Embedded Systems and Design., 19th International Conference.*, pp. 4-pp, Jan. 2006.

[69] R. Puri, L. Stok, J. Cohn, D. Kung, D. Pan, D. Sylvester, A. Srivastava, and S. Kulkarni, "Pushing ASIC Performance in a Power Envelope," *Proceedings of Design Automation Conference*, pp. 788 – 7932, June, 2003.

[70] C. C. Wang, P. M. Lee, C. F. Wu, and H. L. Wu, "High Fan-in Dynamic CMOS Comparators with Low Transistor Count," *IEEE trans. Circuits and Systems*., vol. 50, no. 9, pp. 1216-1220, Sept. 2003.

[71] S. Eto, H. Akita, K. Isobe, K. Tsuchida, H. Toda, and T. Seki, "A 333MHz, 20mW, 18ps Resolution Digital DLL Using Current Controlled Delay with Parallel Variable Resistor DAC (PVR-DAC)," *IEEE 2nd Asia Pacific Conf. on ASIC*, , pp. 349–350, 2000.

[72] M. G. Johnson, E. L. Hudson, and H. Kopka, "A Variable Delay Line PLL for CPU-Coprocessor Synchronization," IEEE J. Solid-State Circuits, vol. 23, pp. 1218–1223, Oct. 1988.

[73] J. Dunning, J. Lundberg, and E. Nuckolls, "An All-Digital Phase Locked Loop with 50-Cycle Lock Time Suitable for High Performance Microprocessors," *IEEE J.Solid-Sate Circuits*, vol. 30, no. 4, pp. 412–422, Apr. 1995.

[74] J. S. Chiang and K. Y. Chen, "The Design of an All-Digital Phase Locked Loop with Small DCO Hardware and Fast Phase Lock," *IEEE Trans.Circuits Syst*. I, vol. 46, no. 7, pp. 945–950, July, 1999.

[75] M. Saint-Laurent and G. P. Muyshondt, "A Digitally Controlled Oscillator Constructed Using Adjustable Resistors," *IEEE in Proc. Southwest Symp. Mixed-Signal Design*, pp. 80–82, 2001.

[76] M. Saint-Laurent and M. Swaminathan, "A Digitally Adjustable Resistor for Path Delay Characterization in High Frequency Microprocessors," *IEEE in Proc. Southwest Symp. Mixed-Signal Design*, pp. 61–64, 2001.

[77] H. Noda, M. Aoki, H. Tanaka, O. Nagashima, and H. Aoki, "An On-Chip Clock Adjusting Circuit with Sub 100-Ps Resolution for a High Speed DRAM Interface," IEEE Trans. Circuits Syst.II, vol. 47, no. 8, pp. 771–775, Aug. 2000.

[78] G. C. Moyer, "The Vernier Techniques for Precise Delay Generation and other Applications," *Ph.D. dissertation*, Dept. of Electrical and Computer Engineering, Univ. of Raleigh, Durham, NC, 1996.

[79] F. Baronti, D. Lunardini, R. Roncella, and R. Saletti, "A Self Calibrating Delay-Locked Delay Line with Shunt Capacitor Circuit Scheme," *IEEE J. Solid-State Circuits*, vol. 39, no. 2, pp. 384-387, Feb. 2004.

[80] M. Maymandi-Nejad, and M. Sachdev, "A Monotonic Digitally Controlled Delay Element," *IEEE J.*, vol. 40, no. 11, pp. 2212-2219, Nov. 2005.

[81] M. Maymandi-Nejad, and M. Sachdev, "A Digitally Programmable Delay Element: Design and Analysis," *IEEE trans. Very Large Scale Integration (VLSI) Systems.*, vol. 11, no. 5, pp. 871-878, Oct. 2003.

[82] D. Pan, H. W. Li, and B. M. Wilamowski, "A low Voltage to High Voltage Level Shifter Circuit for MEMS Application," *IEEE in Proc. 15th Biennial University/Government/Industry Microelectronics Symp.*, pp. 128–131, July, 2003.

[83] B. Choi, "Enhancement of Current Driving Capability in Data Driver ICs for Plasma Display Panels," *IEEE Trans. Consumer Electron.*, vol. 55, no. 3, pp. 992–997, Aug. 2009.

[84] J. Doutreloigne, H. De Smet, J. Van den Steen, and G. Van Doorselaer, "Low-Power High-Voltage CMOS Level-Shifters for Liquid Crystal Display Drivers," *IEEE in Proc. 11th Int. Conf. Microelectronics (ICM'99)*, pp. 213–216, Nov. 1999.

[85] W.-K. Park, C.-U. Cha, and S.-C. Lee, "A Novel Level-Shifter Circuit Design for Display Panel Driver," *IEEE 49th Int. in Midwest Symp. Circuits and Systems.*, vol. 2, pp. 391–394, Aug. 2006.

[86] M. Rossberg, B. Vogler, and R. Herzer, "600V SOI Gate Driver IC with Advanced Level Shifter Concepts for Medium and High Power Applications," *IEEE in Proc. Conf. Power Electronics and Applications.*, pp. 1–8, 2007 Eur.

[87] J. Buyle, V. De Gezelle, B. Bakeroot, and J. Doutreloigne, "A New Type of Level-Shifter for n-type High Side Switches Used in High-Voltage Switching ADSL Line-Drivers," *IEEE in Proc. Int. Conf. Electronics, Circuits and Systems.,* pp. 954–957, Aug. 2008.

[88] J. Doutreloigne, "A Fully Integrated Ultra-Low-Power High-Voltage Driver for Bistable LCDs," *IEEE in Proc. Int. Symp. VLSI Design, Automation and Test.*, pp. 267–270, April, 2006.

[89] R. Chebli, M. Sawan, Y. Savaria, and K. El-Sankary, "High-Voltage DMOS Integrated Circuits with Floating Gate Protection Technique," *IEEE in Proc. Int. Symp. Circuits and Systems,* pp. 3343–3346, May, 2007.

[90] B. Serneels, M. Steyaert, and W. Dehaene, "A High Speed, Low Voltage to High Voltage Level Shifter in Standard 1.2 V 0.13 μm CMOS," *IEEE in Proc. Int. Conf. Electronics, Circuits, and Systems*., pp. 668–671, Dec. 2006.

[91] J. V. Hatfield, and K. S. Chai, "A Beam-Forming Transmit ASIC for Driving Ultrasonic Arrays," *Sensors and Actuators A: Phys., vol. 92, no. 1, pp.* 273-279, 2001.

[92] P. Behnamfar, and Sh. Mirabbasi, "Design of a High-Voltage Analog Front-End Circuit for Integration with CMUT Arrays," *IEEE conf. Biomedical Circuits and Systems.*, pp. 298-301, Nov. 2010.

[93] J. V. Hatfield, M. K. Al-Absi, and K. S. Chai, "A Beam-Forming Transmit ASIC for Driving Ultrasonic Arrays -Forming Transmit ASIC for Driving Ultrasonic Arrays," *The 14th European Conference on Solid-State Transducers.*, pp. 257-258, Aug. 2000.

APPENDIX A

FIRST DATA RELATIVE TO CHAPTER 6

```
function varargout = CMUT_ARRAY_DELAY_CALC(varargin)
% CMUT_ARRAY_DELAY_CALC MATLAB code for CMUT_ARRAY_DELAY_CALC.fig
gui_Singleton = 1;
gui_State = struct('gui_Name',       mfilename, ...
                   'gui_Singleton',  gui_Singleton, ...
                   'gui_OpeningFcn',
@CMUT_ARRAY_DELAY_CALC_OpeningFcn, ...
                   'gui_OutputFcn',
@CMUT_ARRAY_DELAY_CALC_OutputFcn, ...
                   'gui_LayoutFcn',  [] , ...
                   'gui_Callback',   []);
if nargin && ischar(varargin{1})
    gui_State.gui_Callback = str2func(varargin{1});
end

if nargout
    [varargout{1:nargout}] = gui_mainfcn(gui_State, varargin{:});
else
    gui_mainfcn(gui_State, varargin{:});
end
function CMUT_ARRAY_DELAY_CALC_OpeningFcn(hObject, eventdata,
handles, varargin)
handles.output = hObject;

guidata(hObject, handles);

function varargout = CMUT_ARRAY_DELAY_CALC_OutputFcn(hObject,
eventdata, handles)
varargout{1} = handles.output;

function edit_focal_Callback(hObject, eventdata, handles)
function edit_focal_CreateFcn(hObject, eventdata, handles)
if ispc && isequal(get(hObject,'BackgroundColor'),
get(0,'defaultUicontrolBackgroundColor'))
    set(hObject,'BackgroundColor','white');
end

function listbox_cmut_Callback(hObject, eventdata, handles)

function listbox_cmut_CreateFcn(hObject, eventdata, handles)
```

```
if ispc && isequal(get(hObject,'BackgroundColor'),
get(0,'defaultUicontrolBackgroundColor'))
    set(hObject,'BackgroundColor','white');
end

function pushbutton1_Callback(hObject, eventdata, handles)
global cmut_array dis_table
cmut_array=diag([1,4,9,17,22,27,30,32]);
temp=[2 3 5 7 8 10 11 6 8 12 14 15 16 13 16 18 19 20 19 21 23 24 25
26 27 28 29 31];
k_num=1;
for i_num=1:8
    for j_num=i_num+1:8
        cmut_array(i_num,j_num)=temp(k_num);
        cmut_array(j_num,i_num)=temp(k_num);
        k_num=k_num+1;
    end
end
set(handles.uitable_cmut,'data',cmut_array);
for i_num=1:8
    for j_num=1:8
        dis_table(i_num,j_num)=sqrt(((8-i_num)*250+125)^2+((8-
j_num)*250+125)^2);
    end
end
set(handles.uitable_dist,'data',dis_table);
focal_point=str2num(get(handles.edit_focal,'string'));
for i_num=1:8
    for j_num=1:8

cmut_focal_dis(i_num,j_num)=sqrt(dis_table(i_num,j_num)^2+focal_poin
t^2);
    end
end
set(handles.uitable_dist_focal,'data',cmut_focal_dis);
%
finalresults=zeros(32,32);
for i_num=1:32
    for j_num=1:32
        [first_r,first_c]=find(cmut_array==i_num);
        [second_r,second_c]=find(cmut_array==j_num);
        first=cmut_focal_dis(first_r(1),first_c(1));
        second=cmut_focal_dis(second_r(1),second_c(1));
        speed=str2num(get(handles.edit_speed,'string'));
        finalresults(i_num,j_num)=(first-second)/speed*1000;
    end
end
set(handles.uitable_final,'data',finalresults);
temp=handles.selectedCells;
rows=temp(1);
columns=temp(2);
test_temp1={'Selected Array',cmut_array(rows,columns)...
    ;'Distance From Center [um]',dis_table(rows,columns)...
    ;'Distance From Focal Point
[um]',cmut_focal_dis(rows,columns)...
    ;'Delay Time [ns]',finalresults(cmut_array(rows,columns))};
set(handles.uitable_selecting,'data',test_temp1);
```

```
function uitable_cmut_CellSelectionCallback(hObject, eventdata,
handles)
handles.selectedCells = eventdata.Indices;
guidata(hObject, handles);

function listbox_selection_Callback(hObject, eventdata, handles)


function listbox_selection_CreateFcn(hObject, eventdata, handles)
if ispc && isequal(get(hObject,'BackgroundColor'),
get(0,'defaultUicontrolBackgroundColor'))
    set(hObject,'BackgroundColor','white');
end

function edit_speed_Callback(hObject, eventdata, handles)


function edit_speed_CreateFcn(hObject, eventdata, handles)
if ispc && isequal(get(hObject,'BackgroundColor'),
get(0,'defaultUicontrolBackgroundColor'))
    set(hObject,'BackgroundColor','white');
end
function pushbutton2_Callback(hObject, eventdata, handles)
global cmut_array dis_table
cmut_array=diag([1,4,9,17,22,27,30,32]);
temp=[2 3 5 7 8 10 11 6 8 12 14 15 16 13 16 18 19 20 19 21 23 24 25
26 27 28 29 31];
k_num=1;
for i_num=1:8
    for j_num=i_num+1:8
        cmut_array(i_num,j_num)=temp(k_num);
        cmut_array(j_num,i_num)=temp(k_num);
        k_num=k_num+1;
    end
end
set(handles.uitable_cmut,'data',cmut_array);
for i_num=1:8
    for j_num=1:8
        dis_table(i_num,j_num)=sqrt(((8-i_num)*250+125)^2+((8-
j_num)*250+125)^2);
    end
end
set(handles.uitable_dist,'data',dis_table);
focal_point=str2num(get(handles.edit_focal,'string'));
for i_num=1:8
    for j_num=1:8

cmut_focal_dis(i_num,j_num)=sqrt(dis_table(i_num,j_num)^2+focal_poin
t^2);
    end
end
set(handles.uitable_dist_focal,'data',cmut_focal_dis);
%
finalresults=zeros(32,32);
for i_num=1:32
    for j_num=1:32
        [first_r,first_c]=find(cmut_array==i_num);
```

```
        [second_r,second_c]=find(cmut_array==j_num);
        first=cmut_focal_dis(first_r(1),first_c(1));
        second=cmut_focal_dis(second_r(1),second_c(1));
        speed=str2num(get(handles.edit_speed,'string'));
        finalresults(i_num,j_num)=(first-second)/speed*1000;
    end
end
set(handles.uitable_final,'data',finalresults);
```

APPENDIX B

SECOND DATA RELATIVE TO CHAPTER 6

twoDcmutArrayT.m file

```
function varargout = twoDcmutArrayT(varargin)

      gui_Singleton = 1;
      gui_State = struct('gui_Name',       mfilename, ...
                         'gui_Singleton',  gui_Singleton, ...
                         'gui_OpeningFcn',
      @twoDcmutArrayT_OpeningFcn, ...
                         'gui_OutputFcn',
      @twoDcmutArrayT_OutputFcn, ...
                         'gui_LayoutFcn',  [] , ...
                         'gui_Callback',   []);
      if nargin && ischar(varargin{1})
          gui_State.gui_Callback = str2func(varargin{1});
      end

      if nargout
          [varargout{1:nargout}] = gui_mainfcn(gui_State,
      varargin{:});
      else
          gui_mainfcn(gui_State, varargin{:});
      end


function twoDcmutArrayT_OpeningFcn(hObject, eventdata, handles,
varargin)

      handles.output = hObject;
      X = imread('Ultramems.jpg');
      axes(handles.axes2);
      imshow(X)
      axis off
      handles.h=withscale;
      guidata(hObject, handles);
```

```
function varargout = twoDcmutArrayT_OutputFcn(hObject, eventdata,
handles)

      varargout{1} = handles.output;


function pushbutton1_Callback(hObject, eventdata, handles)
      xi=str2double(get(handles.edit1,'String'));
      yi=str2double(get(handles.edit2,'String'));
      zi=str2double(get(handles.edit3,'String'));
      [A,D]=twoDcmutArraySim(xi,yi,zi);
      axes(handles.h);
      axis off;
      [d1,p,dt3,dt2,dt1,dt0]=fireCMUT(A,D);
      axes(handles.axes3);
      yb=d1(1,1:p);
      L=size(yb);
      xb=1:L(1,2);
      bar(yb,'y','EdgeColor','y');
      for i=1:L(1,2)
          text(xb(i)-
      0.4,yb(i),num2str(yb(i)),'Color','b','FontWeight','bold')
      end
      title('BEAMFORMING DELAY TIME','FontWeight','bold');
      xlabel('CMUT ELEMENTS PRIORITY','FontWeight','bold');
      ylabel('DELAY TIME (µS)','FontWeight','bold');
      grid on;
      set(handles.text8,'String',[dt0,char(10),dt1,char(10),dt2,char
      (10),dt3],'FontSize',16);
      guidata(hObject, handles);



function edit1_Callback(hObject, eventdata, handles)
      x=str2double(get(hObject,'String'));
      if(isempty(x))
          set(hObject, 'String',0);
      end


 function edit1_CreateFcn(hObject, eventdata, handles)

      if ispc && isequal(get(hObject,'BackgroundColor'),
      get(0,'defaultUicontrolBackgroundColor'))
          set(hObject,'BackgroundColor','white');
      end



function edit2_Callback(hObject, eventdata, handles)
      y=str2double(get(hObject,'String'));
```

```
    if(isempty(y))
        set(hObject, 'String',0);
    end


function edit2_CreateFcn(hObject, eventdata, handles)
    if ispc && isequal(get(hObject,'BackgroundColor'),
    get(0,'defaultUicontrolBackgroundColor'))
        set(hObject,'BackgroundColor','white');
    end



function edit3_Callback(hObject, eventdata, handles)
    z=str2double(get(hObject,'String'));
    if(isempty(z))
        set(hObject, 'String',0);
    end


function edit3_CreateFcn(hObject, eventdata, handles)
    if ispc && isequal(get(hObject,'BackgroundColor'),
    get(0,'defaultUicontrolBackgroundColor'))
        set(hObject,'BackgroundColor','white');
    end


function [a,d]=twoDcmutArraySim(xi,yi,zi)
    xp=xi;yp=yi;zp=zi;%xp=750;yp=750;zp=100;
    A(4,4)=twoDcmutArray;
    Tmax=0;
    for y=1:4
        for x=1:4
            A(y,x).yc=150+(y-1)*300;
            A(y,x).xc=150+(x-1)*300;
            A(y,x).s=1540;
            A(y,x).xt=abs(xp-A(y,x).xc);
            A(y,x).yt=abs(yp-A(y,x).yc);
            A(y,x).d=sqrt(A(y,x).xt^2+A(y,x).yt^2);
            A(y,x).wd=sqrt(A(y,x).d^2+zp^2);
            A(y,x).tc=A(y,x).wd/A(y,x).s;
            if A(y,x).tc > Tmax
                Tmax=A(y,x).tc;
            end
        end
    end
    D=zeros(1,16);
    dmax=0;
    for y=1:4
        for x=1:4
            A(y,x).dt=Tmax-A(y,x).tc;
```

```
            if A(y,x).dt > dmax
                dmax=A(y,x).dt;
            end
            D(1,((y-1)*4+x))=A(y,x).dt;
        end
    end
    DS=sort(D);
    a=A;
    d=DS;



function pushbutton2_Callback(hObject, eventdata, handles)
    close all;

    function hd=withscale
    axes1 = axes('YTick',[0 300 600 900 1200],...
        'XTick',[0 300 600 900 1200],...
        'Position',[0.505856515373353 0.0291411042944785
    0.486822840409956 0.964723926380368]);

    title('2D-CMUT ARRAY');

    annotation('rectangle',...
        [0.506124450951684 0.0287081339712919 0.121254758418741
    0.242424242424242],...
        'FaceColor','flat');

    annotation('rectangle',...
        [0.627881405563696 0.0278468899521531 0.121254758418741
    0.242424242424242],...
        'FaceColor','flat');

    annotation('rectangle',...
        [0.749169838945841 0.0287081339712919 0.121254758418741
    0.242424242424242],...
        'FaceColor','flat');

    annotation('rectangle',...
        [0.870692532942913 0.0287081339712919 0.121254758418741
    0.242424242424242],...
        'FaceColor','flat');

    annotation('rectangle',...
        [0.506124450951684 0.269537480063796 0.121254758418741
    0.242424242424242],...
        'FaceColor','flat');

    annotation('rectangle',...
        [0.627647144948763 0.269537480063796 0.121254758418741
    0.242424242424242],...
```

```
    'FaceColor','flat');

annotation('rectangle',...
    [0.749169838945841 0.269537480063796 0.121254758418741
0.240829346092503],...
    'FaceColor','flat');

annotation('rectangle',...
    [0.870692532942913 0.269537480063796 0.121254758418741
0.242424242424242],...
    'FaceColor','flat');

annotation('rectangle',...
    [0.506124450951684 0.510366826156305 0.121254758418741
0.242424242424238],...
    'FaceColor','flat');

annotation('rectangle',...
    [0.627881405563695 0.511100478468905 0.121254758418741
0.242424242424238],...
    'FaceColor','flat');

annotation('rectangle',...
    [0.749404099560774 0.511100478468904 0.121254758418741
0.242424242424238],...
    'FaceColor','flat');

annotation('rectangle',...
    [0.870926793557846 0.511100478468904 0.121254758418741
0.242424242424238],...
    'FaceColor','flat');

annotation('rectangle',...
    [0.506358711566619 0.753524720893153 0.121254758418741
0.241690590111631],...
    'FaceColor','flat');

annotation('rectangle',...
    [0.870926793557835 0.753524720893154 0.121254758418741
0.238500797448154],...
    'FaceColor','flat');

annotation('rectangle',...
    [0.627383601756962 0.754258373205753 0.121518301610534
0.239362041467293],...
    'FaceColor','flat');

annotation('rectangle',...
    [0.748901903367496 0.754258373205753 0.121991215226954
0.238500797448154],...
    'FaceColor','flat');
```

```
        hd=axes1;


function [delay1,e,d3,d2,d1,d0]=fireCMUT(obj,DS)

        pause(1);
        delays=zeros(1,16);
        pos=0;
        code=zeros(1,16);
        for i=1:16
            if (i~=16)&&(DS(1,i)==DS(1,i+1))
                continue;
            else
                pause(DS(1,i));
                pos=pos+1;
                delays(1,pos)=DS(1,i);
                cl=selectColor(pos);

               if obj(1,1).dt==DS(1,i)
        annotation('rectangle',...
        [0.506124450951684 0.0287081339712919 0.121254758418741
        0.242424242424242],...
            'FaceColor',cl);
        annotation('textbox', [0.52 0.25 0 0],'FontSize',70, 'String',
        pos);
        code(1,1)=pos-1;
         end

        if obj(1,2).dt==DS(1,i)
        annotation('rectangle',...
            [0.627881405563696 0.0278468899521531 0.121254758418741
        0.242424242424242],...
            'FaceColor',cl);
        annotation('textbox', [0.64 0.25 0 0],'FontSize',72, 'String',
        pos);
        code(1,2)=pos-1;
        end

        if obj(1,3).dt==DS(1,i)
        annotation('rectangle',...
            [0.749169838945841 0.0287081339712919 0.121254758418741
        0.242424242424242],...
            'FaceColor',cl);
        annotation('textbox', [0.76 0.25 0 0],'FontSize',72, 'String',
        pos);
        code(1,3)=pos-1;
        end

        if obj(1,4).dt==DS(1,i)
        annotation('rectangle',...
```

```
    [0.870692532942913 0.0287081339712919 0.121254758418741
0.242424242424242],...
    'FaceColor',cl);
annotation('textbox', [0.89 0.25 0 0],'FontSize',72, 'String',
pos);
code(1,4)=pos-1;
end

if obj(2,1).dt==DS(1,i)
annotation('rectangle',...
    [0.506124450951684 0.269537480063796 0.121254758418741
0.242424242424242],...
    'FaceColor',cl);
annotation('textbox', [0.52 0.49 0 0],'FontSize',72, 'String',
pos);
code(1,5)=pos-1;
end

if obj(2,2).dt==DS(1,i)
annotation('rectangle',...
    [0.627647144948763 0.269537480063796 0.121254758418741
0.242424242424242],...
    'FaceColor',cl);
annotation('textbox', [0.64 0.49 0 0],'FontSize',72, 'String',
pos);
code(1,6)=pos-1;
end

if obj(2,3).dt==DS(1,i)
annotation('rectangle',...
    [0.749169838945841 0.269537480063796 0.121254758418741
0.240829346092503],...
    'FaceColor',cl);
annotation('textbox', [0.76 0.49 0 0],'FontSize',72, 'String',
pos);
code(1,7)=pos-1;
end

if obj(2,4).dt==DS(1,i)
annotation('rectangle',...
    [0.870692532942913 0.269537480063796 0.121254758418741
0.242424242424242],...
    'FaceColor',cl);
annotation('textbox', [0.89 0.49 0 0],'FontSize',72, 'String',
pos);
code(1,8)=pos-1;
end

if obj(3,1).dt==DS(1,i)
annotation('rectangle',...
```

```
    [0.506124450951684 0.510366826156305 0.121254758418741
0.242424242424238],...
    'FaceColor',cl);
annotation('textbox', [0.52 0.72 0 0],'FontSize',72, 'String',
pos);
code(1,9)=pos-1;
end

if obj(3,2).dt==DS(1,i)
annotation('rectangle',...
    [0.627881405563695 0.511100478468905 0.121254758418741
0.242424242424238],...
    'FaceColor',cl);
annotation('textbox', [0.64 0.72 0 0],'FontSize',72, 'String',
pos);
code(1,10)=pos-1;
end

if obj(3,3).dt==DS(1,i)
annotation('rectangle',...
    [0.749404099560774 0.511100478468904 0.121254758418741
0.242424242424238],...
    'FaceColor',cl);
annotation('textbox', [0.76 0.72 0 0],'FontSize',72, 'String',
pos);
code(1,11)=pos-1;
end

if obj(3,4).dt==DS(1,i)
annotation('rectangle',...
    [0.870926793557846 0.511100478468904 0.121254758418741
0.242424242424238],...
    'FaceColor',cl);
annotation('textbox', [0.89 0.72 0 0],'FontSize',72, 'String',
pos);
code(1,12)=pos-1;
end

if obj(4,1).dt==DS(1,i)
annotation('rectangle',...
    [0.506358711566619 0.753524720893153 0.121254758418741
0.241690590111631],...
    'FaceColor',cl);
annotation('textbox', [0.52 0.96 0 0],'FontSize',72, 'String',
pos);
code(1,13)=pos-1;
end

if obj(4,2).dt==DS(1,i)
annotation('rectangle',...
```

```
    [0.627383601756962 0.754258373205753 0.121518301610534
0.239362041467293],...
    'FaceColor',cl);
annotation('textbox', [0.64 0.96 0 0],'FontSize',72, 'String',
pos);
code(1,14)=pos-1;
end

if obj(4,3).dt==DS(1,i)
  annotation('rectangle',...
    [0.748901903367496 0.754258373205753 0.121991215226954
0.238500797448154],...
    'FaceColor',cl);

annotation('textbox', [0.76 0.96 0 0],'FontSize',72, 'String',
pos);
code(1,15)=pos-1;
end

if obj(4,4).dt==DS(1,i)
annotation('rectangle',...
    [0.870926793557835 0.753524720893154 0.121254758418741
0.238500797448154],...
    'FaceColor',cl);

annotation('textbox', [0.89 0.96 0 0],'FontSize',72, 'String',
pos);
code(1,16)=pos-1;
end

end
 end
 D3='D3: ';D2='D2: ';D1='D1: ';D0='D0: ';
 for s=1:4
    D3=[D3,' ',dec2bin(code(1,s),4)];
 end
 for s=5:8
    D2=[D2,' ',dec2bin(code(1,s),4)];
 end
 for s=9:12
    D1=[D1,' ',dec2bin(code(1,s),4)];
 end
 for s=13:16
    D0=[D0,' ',dec2bin(code(1,s),4)];
 end
 delay1=delays;
 e=pos;
 d3=D3;
 d2=D2;
 d1=D1;
 d0=D0;
```

```
      axis('off');

function color = selectColor(n)
switch(n)
    case 1
        color= 'y';
    case 2
        color='c';
    case 3
        color='g';
    case 4
        color=[0,0.4,1];
    case 5
        color='r';
    case 6
        color='w';
    case 7
        color='m';
    case 8
        color=[165/255,42/255,42/255];
    case 9
        color=[188/255,143/255,143/255];
    case 10
        color=[1,165/255,0];
    case 11
        color=[128/255,128/255,128/255];
    case 12
        color=[245/255,222/255,179/255];
    case 13
        color=[32/255,178/255,170/255];
    case 14
        color=[240/255,230/255,140/255];
    case 15
        color=[210/255,180/255,140/255];
    otherwise
        color=[210/255,105/255,30/255];
end



function pushbutton3_Callback(hObject, eventdata, handles)
      axes(handles.h);
      erase=[192/255,192/255,192/255];
      annotation('rectangle',...
          [0.506124450951684 0.0287081339712919 0.121254758418741
      0.242424242424242],...
          'FaceColor',erase);

      annotation('rectangle',...
          [0.627881405563696 0.0278468899521531 0.121254758418741
      0.242424242424242],...
```

```
    'FaceColor',erase);

annotation('rectangle',...
    [0.749169838945841 0.0287081339712919 0.121254758418741
0.242424242424242],...
    'FaceColor',erase);

annotation('rectangle',...
    [0.870692532942913 0.0287081339712919 0.121254758418741
0.242424242424242],...
    'FaceColor',erase);

annotation('rectangle',...
    [0.506124450951684 0.269537480063796 0.121254758418741
0.242424242424242],...
    'FaceColor',erase);

annotation('rectangle',...
    [0.627647144948763 0.269537480063796 0.121254758418741
0.242424242424242],...
    'FaceColor',erase);

annotation('rectangle',...
    [0.749169838945841 0.269537480063796 0.121254758418741
0.240829346092503],...
    'FaceColor',erase);

annotation('rectangle',...
    [0.870692532942913 0.269537480063796 0.121254758418741
0.242424242424242],...
    'FaceColor',erase);

annotation('rectangle',...
    [0.506124450951684 0.510366826156305 0.121254758418741
0.242424242424238],...
    'FaceColor',erase);

annotation('rectangle',...
    [0.627881405563695 0.511100478468905 0.121254758418741
0.242424242424238],...
    'FaceColor',erase);

annotation('rectangle',...
    [0.749404099560774 0.511100478468904 0.121254758418741
0.242424242424238],...
    'FaceColor',erase);

annotation('rectangle',...
    [0.870926793557846 0.511100478468904 0.121254758418741
0.242424242424238],...
    'FaceColor',erase);
```

```
        annotation('rectangle',...
            [0.506358711566619 0.753524720893153 0.121254758418741
        0.241690590111631],...
            'FaceColor',erase);

        annotation('rectangle',...
            [0.870926793557835 0.753524720893154 0.121254758418741
        0.238500797448154],...
            'FaceColor',erase);

        annotation('rectangle',...
            [0.627383601756962 0.754258373205753 0.121518301610534
        0.239362041467293],...
            'FaceColor',erase);

        annotation('rectangle',...
            [0.748901903367496 0.754258373205753 0.121991215226954
        0.238500797448154],...
            'FaceColor',erase);
        set(handles.edit1, 'String',0);
        set(handles.edit2, 'String',0);
        set(handles.edit3, 'String',0);
        set(handles.text8, 'String',' ');
        axes(handles.axes3);
        y=zeros(1,16);
        bar(y);
```

twoDcmutArray.m file

```
classdef twoDcmutArray
   properties(GetAccess = 'public', SetAccess = 'public')
      xc
      yc
      xt
      yt
      d
      wd
      tc
      dt
      s
 end
end
```