A LOW-COST UNCOOLED INFRARED IMAGING SENSOR USING MEMS AND A MODIFIED STANDARD CMOS PROCESS

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AL LOW-COST UNCOOLED INFRARED IMAGING SENSOR

USING MEMS AND A MODIFIED STANDARD CMOS PROCESS

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ABSTRACT

A LOW-COST UNCOOLED INFRARED IMAGING SENSOR
USING MEMS AND A MODIFIED STANDARD CMOS PROCESS

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The thesis presents a monolithically integrated low-cost uncooled infrared imaging sensor using a MEMS process and a modified standard CMOS process. The designed sensor has an image format of 160×120 with a pixel pitch of 40 µm. The sensor is implemented with microbolometers that sense the infrared radiation in the 8-12 µm spectral band, where the sensing elements in each pixel are formed with CMOS diodes to sense the temperature variation in the pixel by monitoring the change in the forward bias voltage of diodes. The pixels have multiple serially connected diodes to increase the temperature sensitivity. The number of serially connected diodes in each pixels can be configured as 4, 5, and 6 with simple modification in the CMOS metal layers, at the expense of using higher supply voltages required to bias the pixel array. The current sensor design has 6 serially connected diodes in the pixel, requiring a 7 V supply voltage in the pixel array. The sensor has been implemented using a 1 µm SOI-CMOS process, with a slight process modification, where the pixel area is processed using a higher grade photolithography process allowing a minimum feature size of 0.5 µm. The smaller feature size in the pixel area allows obtaining better thermal isolation of the suspended bridges that hold the diodes through support arms. Suspended bridge like structures are obtained with a simple post-CMOS etching process, which does not require any critical lithography steps. Hence, microbolometer fabrication cost can be decreased drastically, making these microbolometers potentially suitable for newly emerging various cost-effective infrared imaging applications, such as automotive, advanced presence detection, security, and consumer electronics.

The designed infrared imaging sensor has a system-on-chip (SoC) architecture, and it runs on a single 7 V supply voltage. The designed sensor has both analog and digital integrated circuit modules, typically running at 5 V supply voltage except the pixel array. The designed imaging sensor is highly programmable, where timing of the critical digital signals and level of analog voltage and current biases can be programmed using programmable on-chip digital controllers

and digital-to-analog converter (DAC) based voltage and current biasing circuits. The chip has also an integrated output buffer to drive high capacitance external loads.

The infrared imaging sensor developed in this thesis has been fabricated in a 1 µm SOI-CMOS process using a wafer-level test run with a slight modification to allow fabrication of pixels with 0.5 µm minimum features size in the pixel area. Fabricating the imaging sensor at wafer-level allows also using conventional wafer-level microfabrication and MEMS processing steps, avoiding any difficulties that may arise due to use of die-level processing. The fabricated imaging sensor measures 10.5 mm×11.0 mm, where the readout circuitry is integrated in two parts at the top and the bottom of the chip. In this way, the pixel array is placed in the middle of the chip, hence it is possible to add a rectangular ring structure around the pixel array, which can later be used as a bonding surface required by several wafer-level vacuum packaging processes.

The fabricated infrared imaging sensor is tested in detail to verify its functionality and to perform its characterization. The sensitivity and DC responsivity of single pixel test structures having 6 serially connected diodes are measured to be -7.05 mV/K and 18,194 V/W, respectively. The overall output noise of the readout circuit is measured as 124 μV_{rms}. The integrated detector noise of the single pixel is measured as 5.19 μV_{rms} in a 4 kHz bandwidth, resulting in an expected NETD value of 840 mK for the imager with an f/1 optics.

Keywords: Uncooled infrared detectors, low-cost microbolometers, low-cost infrared imaging sensor, diode type microbolometers, infrared readout circuits

ÖZ

DÜŞÜK MALİYETLİ SOĞUTMASIZ KIZILÖTESİ DETEKTÖR DİZİNİ

Gülden, Mehmet Ali

Yüksek Lisans, Elektrik ve Elektronik Mühendisliği Bölümü

Tez Yöneticisi : Prof. Dr. Tayfun Akın

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Bu tezde MEMS süreci ve değiştirilmiş bir standart CMOS işlemi kullanılarak kendisiyle bütünleşik odak düzlem matrisi (ODM) sunulmaktadır. ODM 160×120 çözünürlükte olup 40 µm adım uzunluğundaki piksellerden oluşmaktadır. Mikrobolometreler piksellerindeki CMOS diyotların açılım voltajlarındaki ortam sıcaklığına bağlı değişimleri izleyerek, 8-12 µm bandındaki kızılötesi ışınımları algılar. Piksellerdeki sıcaklık duyarlılığını artırmak için çok sayıda seri bağlanmış diyotlar bulunur. Piksellere güç vermek için gerekli yüksek gerilim pahasına, piksellerdeki diyot sayısı CMOS metal katmanlarında ufak bir değişiklikle 4, 5 ve 6 olarak yapılandırılabilir. Tez tasarımı 6 adet seri bağlanmış diyottan oluşmaktadır ve yonga için 7 V gerilim gerekmektedir. Tez piksel alanı içerisinde ufak bir değişiklikle 0.5 µm minimum özellik boyutlu maskeler kullanarak, standart 1 µm SOI-CMOS üretimi ile üretilmiştir. Piksel alanındaki diyotları tutan küçük özellik boyutlu destek kolları ile daha iyi ısı izolasyonu sağlanır. Piksellerin asma köprüye benzer bir yapıya getirilmesi hiçbir kritik pozlama işlemi gerektirmeyen basit CMOS sonrası kazıma işlemi ile yapılır. Bu basit CMOS sonrası kazıma işlemi sayesinde mikrobolometrenin üretim maliyeti aşırı derecede düşer ve mikrobolometreler otomotiv, gelişmiş varlık algılama, güvenlik ve tüketici elektroniği gibi birçok yeni uygun maliyetli kızılötesi görüntüleme uygulamalar için potansiyel olarak elverişli hale gelir.

Tasarlanan kızılötesi görüntüleme sensörü çip üzerinde sistem mimarisindedir ve sadece 7 V besleme gerilimi ile çalışır. Tasarlanan sensör hem analog hem de sayısal entegre devre modüllerine sahiptir ve piksel besleme gerilimi dışında 5 V ile çalışır. Tasarlanan görüntüleme sensörü çip üzerinde bulunan sayısal kontrol devresi ile kritik sinyallerin boyutlarını ve sayısaldan analoğa çevirici kutuplama devreleri sayesinde kutuplama gerili ve akımlarının seviyeleri ayarlanabilir. Çipte ayrıca yüksek kapasite dış yükleri sürmek için entegre çıkış tamponu bulunur.

Bu tezde geliştirilen kızılötesi görüntüleme sensörü silikon devre levhasında test üretimi şeklinde 1.0 µm SOI-CMOS sürecinde, sadece piksel alanında ufak bir değişiklikle 0.5 µm minimum özellik

boyutu kullanılarak üretilmiştir. Silikon devre levhası düzeyinde görüntüleme sensörü üretimi levha seviyesinde mikro üretim ve MEMS işlemi adımlarına izin verir. Görüntüleme sensörü iki parça halinde entegre olmuştur ve 10.5mm×11mm alana sığar. Bu şeklide piksel dizisi çipin ortasına yerleştirilir, ve bundan dolayı silikon levha seviyesinde paketleme işlemleri için paket bağlama işlemlerinde kullanılmak üzere piksel dizini etrafına dikdörtgen halka şeklinde bir yapı eklemek mümkün olur.

Üretilen yonga çalıştığını görmek ve performansını karakterize etmek için test edilmiştir. Piksel duyarlılığı ve piksel kızılötesi tepkiselliği 6 diyot ile sırasıyla -7.05 mV/K ve 18,194 V/W olarak ölçülmüştür. Okuma devresi ve çıkış tamponunun gürültü seviyesi 124 μV_{rms} olarak ölçülmüştür. Piksellerin 4 kHz frekans genişliğindeki gürültü seviyesi 5.19 μV_{rms} olarak ölçülmüştür, bu da mikrobolometrenin f/1 optik ile 840 mK NETD değerine karşılık gelir.

Anahtar kelimeler: soğutmasız kızılötesi detektörler, düşük maliyetli detektörler, diyot tipi mikrobolometre, mikrobolometre okuma devresi

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CHAPTER 1

INTRODUCTION

Seeing an object when there is no light is among the most important desires of the mankind, and there have been a lot of researches conducted to find a solution to satisfy this need. These researches can mainly be divided into two categories: photonic based infrared detectors and thermal based infrared detectors [1]. These detectors are used to detect the radiation emitted from the surrounding objects, as very thing above 0 K emits radiation maximum at certain wavelength, which is around 10μm wavelength for objects at around room temperature.

In photonic detectors, the received radiations typically generate E-H pairs, which are sensed by the help of readout integrated circuits. However, there are also thermally generated E-H pairs in the material, and these thermally generated E-H pairs dominate the photonically generated E-H pairs. To be able to differentiate photonically generated E-H pairs from the thermally generated ones, the detector should be cooled down to cryogenic temperatures (77K) to reduce the thermally generated E-H pairs. This cooling operation makes the system bigger and expensive. Therefore, these cooled detectors are mostly used in military applications, astronomical observation stations, and sophisticated medical instruments.

In thermal detectors, thermal waves hitting on the absorber material heats up the surface and changes the temperature of a suspended and thermally isolated bridge. This change in temperature causes the electrical parameters of a device embedded in the bridge to change, where the temperature sensing device is mostly implemented with a resistor or diode [2]. The change in the electrical parameters is read out by using a readout integrated circuit, which is used to generate a thermal image. Since these types of detectors do not need to be cooled, they are also named as uncooled infrared detectors. Uncooled infrared detectors sense the infrared radiation indirectly as heating. Therefore, their performance parameters are relatively low compared to photonic detectors. However, they have small size, require low power, and result in low-cost detectors. They can be used both military applications and commercial applications. There is a constant push to decrease the cost of the uncooled microbolometers to make them potentially suitable for many new cost-effective infrared imaging applications, such as automotive, advanced presence detection, security, and consumer electronics.

Uncooled thermal imagers emerged to satisfy the military needs or high-end applications. Therefore, performance parameters and the size is the primary concern. The cost is still high for commercial applications. The reason for high cost is that they use either complicated post CMOS processes or they need dedicated foundries. This thesis work aims for low-cost uncooled thermal imager for commercial applications. The designed uncooled thermal imager is compatible with the CMOS production line, and it needs basic post-CMOS processes. Therefore, the cost of the imager is very low compared to the previously designed uncooled thermal imagers.

This thesis reports development of a 160×120 low-cost uncooled thermal imager with a 40 µm pixel pitch for commercial applications, where the diode type microbolometer approach is used. The rest of this chapter is organized as follows. First, Section 1.1 mentions the types of uncooled thermal infrared detectors. Then, Section 1.2 describes the microbolometers mainly diode type, while Section 1.3 summarizes the previous works at Middle East Technical University regarding diode type microbolometers. Finally, Section 1.4 gives research objectives and thesis organization.

1.1 Types of Uncooled Infrared Detectors

There are mainly three types of thermal detectors: thermoelectric detectors, pyroelectric/ferromagnetic detectors, and microbolometers. This section briefly mentions thermoelectric and pyroelectric type of detectors, while microbolometers are mentioned in more details in a separate section, i.e., in Section 1.2, as this thesis is about microbolometers.

Figure 1-1 shows schematics of a thermocouple [3] used in thermoelectric infrared detectors. There is a serially connected two thermoelectric couples with different Seebeck coefficients. When heat is applied at the junction, a voltage difference occurs between the other ends of the thermocouples at the cold junction.

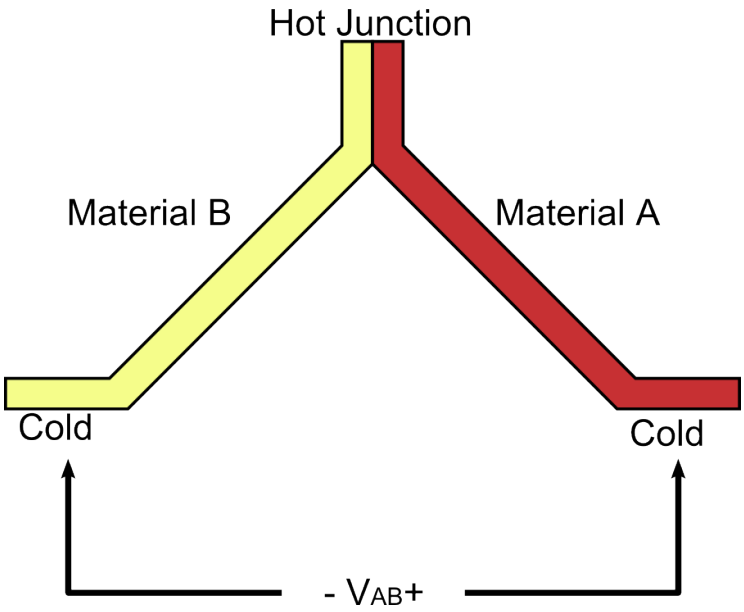


Figure 1-1: Schematics of a thermocouple [3] used in thermoelectric infrared detectors.

The voltage difference of a thermocouple is given as [4];

$$V_{AB} = (\alpha_A - \alpha_B)\Delta T_{hot-cold} \tag{1.1.1}$$

where α_A and α_B are Seebeck Coefficients of two materials, and $\Delta T_{hot\text{-}cold}$ is temperature difference between hot and cold junctions. A number of thermocouples can be connected to increase the responsivity, and these kinds of devices are called thermopiles. There are thermopile type infrared imaging arrays in the market, but their use is limited due to their low performance, high pixel sizes (typically 100-250 µm), and low array formats (typically 8×8-32×32).

Pyroelectric thermal detectors use pyroelectric effect of the materials, which is the generation of an electrical charge due to rapid changes of the temperature. The temperature induced current across the detector is given as [5];

$$i_d = pA\frac{dT}{dt} \tag{1.1.2}$$

where, p is the pyroelectric coefficient, A is area of the electrode, T is detector temperature, and t is time. There is no output current for DC constant infrared radiation or no infrared radiation. Therefore, incoming radiation energy should be modulated with the help of a chopper. The chopper causes a constant infrared radiation to seem as an AC excitation, which yields an AC current as an output. The peak of the AC current can be interpreted as infrared radiation level. However, there is one downsize of the pyroelectric detectors, whose sensing mechanism is pyroelectric effect. Pyroelectric effect of a material vanishes above critical temperature. This temperature is called as Curie temperature. For higher responsivity, pyroelectric detectors operate just below their Curie temperature level, which makes the use of thermoelectric temperature stabilizers obligatory for preventing the detector temperature to reach up to the Curie temperature [6].

Ferroelectric detectors also use pyroelectric effect of the materials to detect thermal radiation. Unlike pyroelectric detectors, the detector is biased to create an internal electric field, which increases the responsivity of the material. Unlike pyroelectric detectors, Curie temperature of the ferroelectric detectors is well above the room temperature, and they do not require temperature stabilizers [6]. Although ferroelectric type detectors were popular in 1990's and 320×240 FPAs with 50 µm pixel sizes were sold in high volumes, these detectors could not compete with the microbolometer technology both in price and in performance that showed impressive development with 17 µm pixel pitch and mega pixel formats.

1.2 Microbolometers

Figure 1-2 shows perspective view of a microbolometer [7], which is the most popular type of uncooled thermal detectors. When the infrared radiation heats the absorber material, electrical parameters of the active materials under the surface will change due to slight temperature changes. These electrical parameters are either resistance of a resistor or forward bias voltage of a diode. If the electrical parameter is resistance, microbolometer can be called as a resistive microbolometer or if the electrical parameter is forward bias voltage of a diode, microbolometer is named as a diode microbolometer.

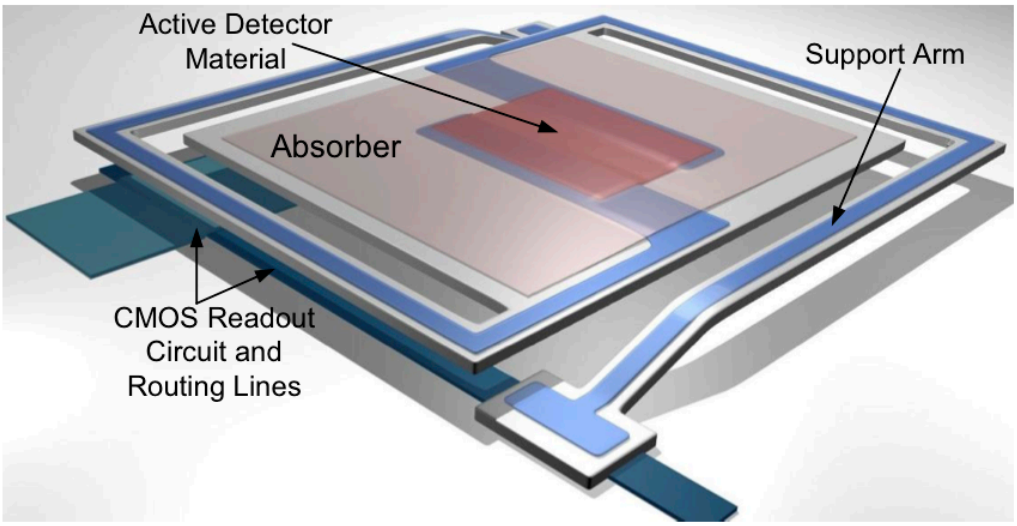


Figure 1-2: Perspective view of a microbolometer [7].

Thermal isolation and the quality of the absorber material are among the most important parameters of the microbolometers. To increase the thermal isolation of the pixel from the surrounding environment and each other, the shape of the pixel structure should be in the form of suspended bridges. There are two methods for creating the suspended bridge structures, and building thermally sensitive diodes or resistors on the absorber layer. The first method is the surface micromachining. The surface micromachining technique allows the designer to build thermally sensitive layers over the readout chips with good thermal isolation, good absorption, and very small mass. Different materials such as vanadium oxide (VO_x) [8], amorphous silicon (a-Si) [9], polycrystalline silicon-germanium (poly SiGe) [10], Yttrium Barium Copper Oxide (YBaCuO) [11], and metal films [12] are used for implementing microbolometer pixel structures. All of these materials have some drawbacks. VO_x is not compatible with the CMOS process line, a-Si and poly SiGe requires high temperature annealing, and YbaCuO needs complicated post CMOS processes. The second method is the bulk micromachining. In bulk micromachining technique, suspended pixel structures are obtained by the etching of the produced CMOS readout chips. In this thesis work, bulk micromachining technique, which is compatible with the CMOS process is applied after the readout chip is produced. Therefore, the cost of the uncooled thermal imager reduces almost down to the cost of the CMOS readout circuit, which can be improved with the reduction in the size of the chip.

1.2.1 Resistive Microbolometer

Sensing mechanism of the resistive microbolometer is the resistance of a resistor embedded in the suspended bridge. Temperature of the suspended bridge increases due to absorbed incident infrared radiation. The resistance of a resistor changes upon this thermal change, related with its temperature coefficient of a resistor (TCR) value. The change in the resistance is given as;

$$\Delta R = R\Delta T\alpha \qquad (1.2.1.1)$$

where, ΔR is resistance change, ΔT is temperature change, and α is TCR coefficient in %/K. Since temperature change due to infrared radiation is low, the materials used as detector resistance should have high TCR values. High TCR materials are used as resistance on the suspended structure to increase the resistance difference for a slight temperature changes. The most widely used material is vanadium oxide VO_x [13]. VO_x has a TCR value of 2-3%/K. There are two drawbacks of VO_x. The material is not compatible with CMOS line, and it is patented to some companies. Therefore, there are not many process specifications n the literature.

Figure 1-3 shows the simple half bridge structure for reading slight resistance changes on the microbolometer resistance. When the detector resistance changes due to infrared radiation, voltage drop across this resistance also changes. The column readout circuit then reads out the difference of the voltage drop, and creates a meaningful output voltage related with the incoming infrared radiation. There are also more advanced circuits to read out the slight resistance changes accurately in the literature [14].

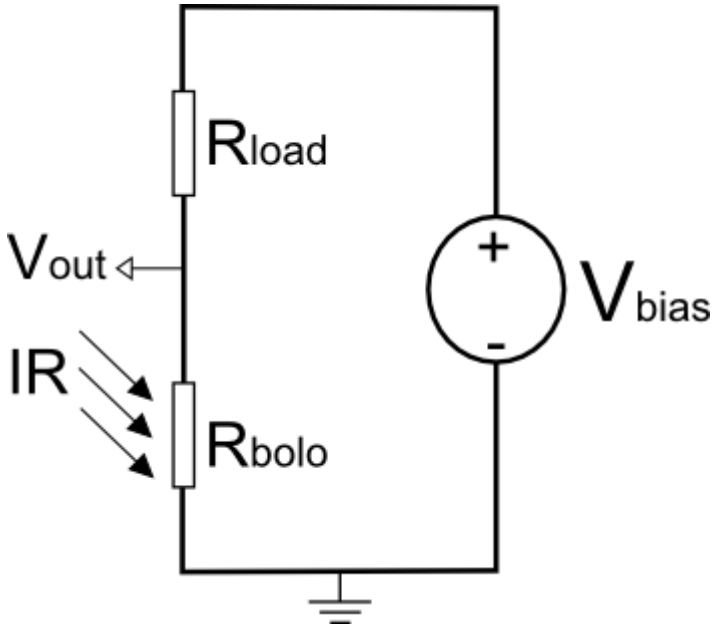


Figure 1-3: Simple half bridge structure for reading slight temperature changes on the detector resistance due to temperature change of the medium [3].

1.2.2 Diode Microbolometer

Another approach to detect slight temperature changes is using diodes as the detector elements. Forward bias voltage of a diode decreases if the temperature of the diode increases for a constant current bias. Figure 1-4 shows a simple diode microbolometer pixel circuitry. The circuitry includes serially connected diodes and constant current bias elements. The output voltage increases when the temperature of the surface increases, because the forward bias voltage of the diode has negative temperature coefficient. Readout electronics detects the slight voltage changes at the output and creates the infrared image of the scene. Since this

thesis work is one of diode microbolometer implementation, Chapter 2 examines the figure of merits for diode microbolometers, and Chapter 3 mentions the implemented readout circuit for detection of a slight temperature changes.

In the literature, there are some implementations of diode type microbolometers in SOI-CMOS wafers. Mitsubishi is a leading company in this area. Mitsubishi has managed to fabricate 320×240 FPA with 40 µm pixel pitch and 640×480 FPA with 25 µm pixel pitch with NETD values around 40 mK [15]. Mitsubishi also developed a mega pixel diode microbolometers with 17 µm pixel pitch [16], and Toshiba has developed 22 µm pixel pitch diode microbolometers [17]. These studies show the state of the art in diode type microbolometers targeting military applications; however, these approaches use internal CMOS processes of the companies with some modified process steps. Therefore, these detector arrays cannot be fabricated in high volume CMOS and MEMS foundries, which is a key issue to drastically decrease the cost of these detectors.

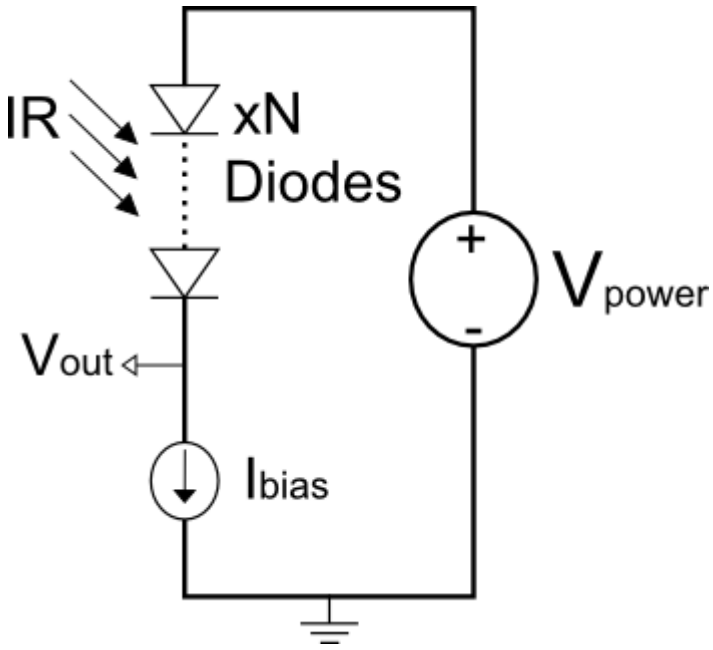


Figure 1-4: Simple diode microbolometer pixel bias.

1.3 Low-Cost Microbolometers in METU

The main aim of the study in METU is to decrease the fabrication cost of microbolometers by using minor post-CMOS processes to implement microbolometer FPAs. This is achieved by implementing diode microbolometer detector arrays using an SOI-CMOS process together with a post-CMOS process that requires only one mask. The first SOI-CMOS diode microbolometer goes back to 2005 [18], which was a 16×16 FPA. Later, 64×64 [19] and 128×128 [20] FPAs were produced. The first working 128×128 FPA array was produced in 2008, and it is reported that NETD value of the FPA array is 1.1 K due to bad camera electronics. After this high NETD value, a

new 128×128 FPA array with new digital features and new camera electronics study is started [21], where the produced array provided an average NETD value of 460 mK and peak NETD of 340 mK. Figure 1-5 shows the first successful room temperature image taken with the diode type microbolometer at METU with SOI-CMOS diode microbolometer array with a pixel pitch of 70 µm designed in 2011 [21].

Figure 1-5: The first successful room temperature image taken with the diode type microbolometer at METU with SOI-CMOS diode microbolometer array with a pixel pitch of 70 µm designed in 2011 [21].

After these successful works, a new company founded in the METU Technopolis, as a spin-off from METU-MEMS Center [22]. This company focuses on increasing the performance of the uncooled microbolometers, making them suitable for many new cost-effective applications, and named as MikroSens [22]. They have produced different versions of the uncooled thermal imager developed in METU, which has a 70 µm pixel pitch. Figure 1-6 shows the image taken with the developed uncooled microbolometer by MikroSens.

Figure 1-6: Image taken with the new version of the uncooled microbolometer by MikroSens, which is implemented with 70 µm pixel pitch.

The image taken with the developed microbolometer by Mikrosens, in Figure 1-6, does not contain column based defects in the Figure 1-5 via developments in the readout and the image processing algorithms. MikroSens have both worked on the increasing the performance parameters of the microbolometer and increasing the image quality with the software tools.

Currently, Mikrosens is working with MEMS foundries to develop a wafer level vacuum packaging technology. Figure 1-7 shows a picture of the wafer-level vacuum packaged 160×120 FPA with 70 µm pixel pitch. Figure 1-8 shows pictures of a miniature camera that was developed as a demonstration platform. It should be noted that the pixel size of these detectors needs to be reduced to reduce the cost of the FPAs further to be able to compete in the market.

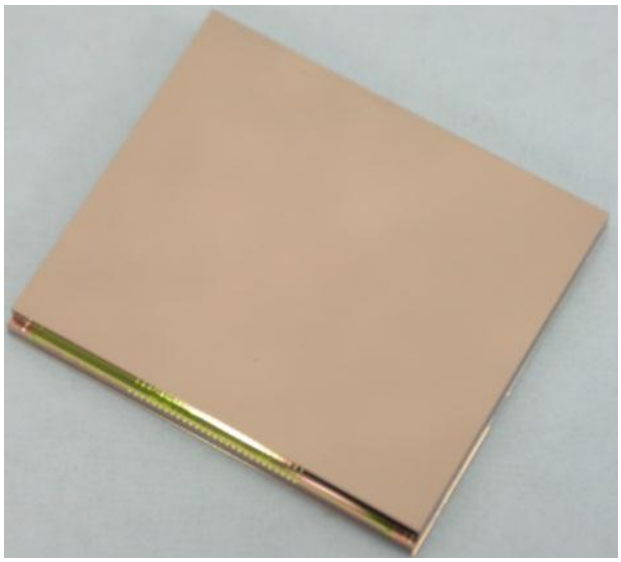
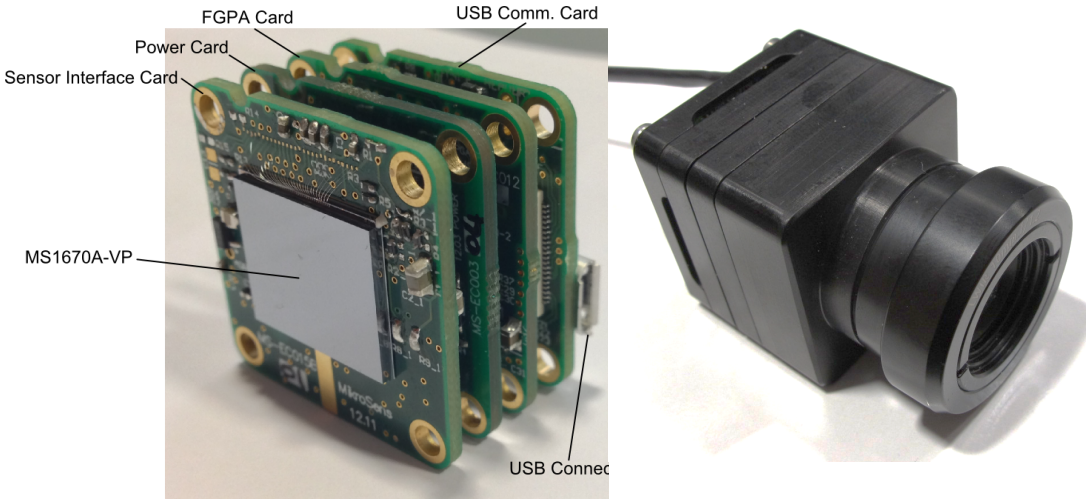


Figure 1-7: A picture of the wafer-level vacuum packaged 160×120 FPA with 70µm pixel pitch [23].



(a) (b)

Figure 1-8: The photographs of a miniature camera that was developed as a demonstration platform: (a) the developed camera module cards and (b) the camera module itself [24].

1.4 Research Objectives and Thesis Organization

This thesis work is focused on developing a low-power low-cost uncooled microbolometer detector array that aims to be an advanced version of the previously done microbolometer at METU [21]. In order to have the advanced features from the previous work, the designed microbolometer should have the following features:

1. Microbolometer pixels should be made smaller. The pixel pitch is reduced from 70 µm [21] to 40 µm.
2. Internal analog and digital blocks should be implemented. Internal R2R DACs for control voltages and internal regulators should be implemented for column readout and pixel powers.
3. Designed microbolometer should be compatible with an FPGA. Therefore, internal up and down level shifters should be designed to have 3.3 V scale digital input or output voltages.
4. New readout architecture should be designed to decrease the layout area of the readout channel, which gives enough space to make the readout array double-sided. This results in faster frame rates with double output options.
5. Analog output buffers should be implemented in the chip to eliminate the need for the external buffers. Elimination of the external buffers together with the elimination of the external level shifters decreases the PCB area of the product.

Organization of this thesis is as follows:

Chapter 2 mentions about the figure of merits for designing diode type uncooled microbolometer arrays. Besides mentioning figure of merits, this chapter also gives detailed analysis of the designed microbolometer, and states the theoretical pixel performance parameters.

Chapter 3 gives the explanations of the digital and analog blocks of the designed diode microbolometer. This chapter also mentions about the pixel size reduction, the newly implemented column readout circuit, configurable timing generator, and configurable on-chip bias generator.

Chapter 4 shows the primary pixel test results, and compares them with the previous work at METU [21]. This chapter also mentions the electrical test environment, and states the pixel performance test results and the electrical test results of the readout electronics of the microbolometer.

Chapter **Error! Reference source not found.** summarizes the thesis work and mentions about what should be done in the metal revision of this chip. Then this chapter finishes with the future work regarding diode microbolometer.

CHAPTER 2

FIGURE OF MERITS FOR DIODE MICROBOLOMETERS

This chapter explains the important parameters for comparing the performances of infrared imagers, and gives the calculated results of the designed diode microbolometer array. The most important parameters for infrared imaging applications are temperature sensitivity, thermal time constant, responsivity, noise equivalent power, noise equivalent temperature difference, and detectivity. The following sections explain these parameters, and how they are calculated. The sections also give the numerical information of the designed diode microbolometer.

Figure 2-1 shows the top view of the microbolometer pixel, and Table 2-1 gives the physical dimensions of the designed microbolometer pixel. Support arm etch margin, etch opening, and support arm width are process related parameters. These parameters are desired to be as small as possible. Support arm etch margin is the mask on both sides of the support arms to prevent the etching of these arms, and placed as 0.5 μm on both sides of the support arm polysilicon. Totally, 1 μm extra metal masks is needed for each support arm. The designed microbolometer is in 160 by 120 array format, and has a pixel pitch of 40 μm. Dimensions of the designed microbolometer in the scope of this thesis are 10.5 mm by 11 mm.

Table 2-1: Physical dimensions of the designed microbolometer pixel.

Parameters	Value
Pixel Pitch	40 μm
Absorbing Pitch	25 μm
Wall Width	3 μm
Etch Opening	1.5 μm
Support Arm Etch Margin	1 μm
Support Arm Width	0.5 μm
Support Arm Length	60.5 μm

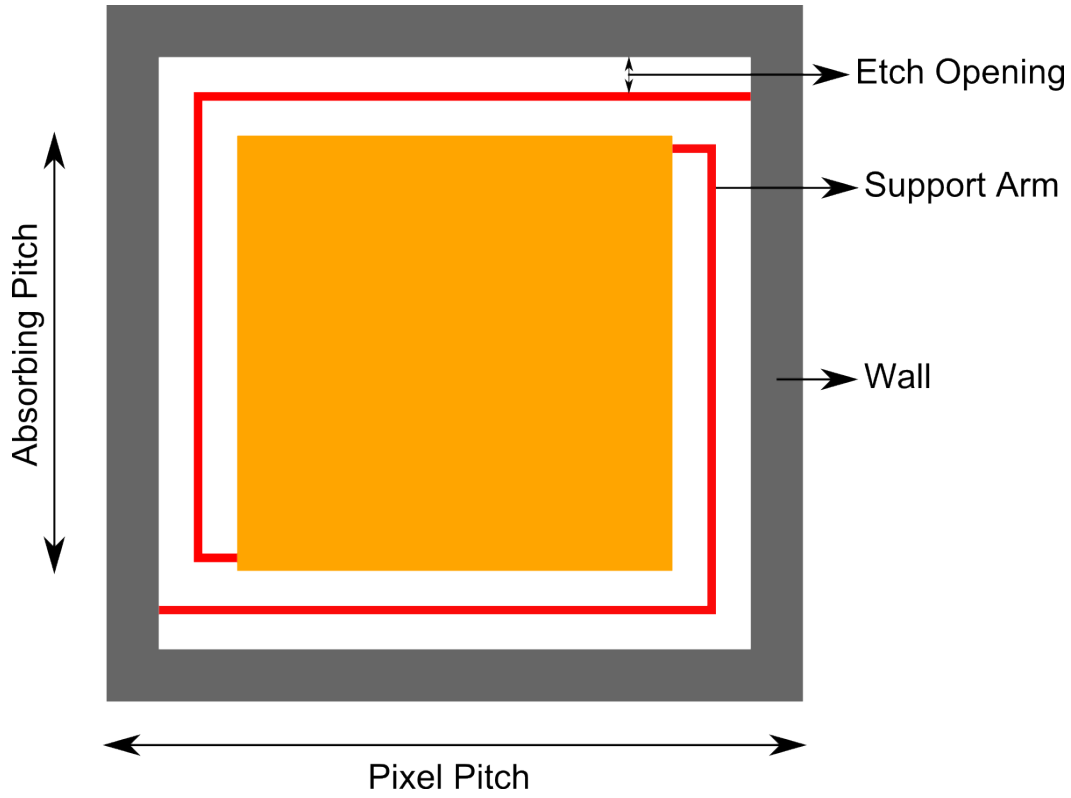


Figure 2-1: Top view of microbolometer pixel.

This chapter is organized as follows: Section 2.1 mentions temperature sensitivity for diode microbolometers. Section 2.2 explains thermal time constant. Section 2.3 describes responsivity. Section 2.4 explains noise equivalent power. Section 2.5 mentions noise equivalent temperature difference. Section 2.6 shows the last important parameter, detectivity. Finally, Section 2.7 concludes this chapter by giving the parameter values of the designed microbolometer.

2.1 Temperature Sensitivity

Diode microbolometers use forward bias voltage of a diode as thermal sensing element. When an infrared radiation hits the absorber structure, forward bias voltage of a diode implanted on the absorber structure changes. Temperature sensitivity is defined as the ratio of change in forward bias voltage to the change in temperature [25].

$$TC = \frac{dV_D}{dT} \tag{2.1.1}$$

where, TC is the temperature sensitivity of a diode in V/K, V_d is forward bias voltage of a diode in V, and T is the temperature in K.

Current flowing through a forward biased diode is expressed as [24] ;

$$I_D = I_S(e^{\frac{qV_D}{nkT}} - 1) \tag{2.1.2}$$

where, I_D is the bias current of the diode in A, I_S is the saturation current in A, V_D is the forward bias voltage of the diode in V, n is the ideality factor generally taken as 1, k is the Boltzmann constant, T is the temperature in K. V_D can be derived as follows [20] ;

$$V_D = \frac{kT}{q}\ln\left(\frac{I_D}{I_S}\right) \tag{2.1.3}$$

Taking derivative of the equation 2.1.3 with respect to temperature results in;

$$\frac{dV_D}{dT} = \frac{k}{q}\ln\left(\frac{I_D}{I_S}\right) - \frac{kT}{qI_S}\frac{dI_S}{dT} \tag{2.1.4}$$

I_S, saturation current, can be written as;

$$I_S = KT^m e^{\frac{-E_g}{kT}} \tag{2.1.5}$$

where, K and m are constants, m between 2.5 and 5, E_g is the bandgap energy of silicon, 1.12 eV. Taking derivative of equation 2.1.5 with respect to temperature gives the last portion of the temperature sensitivity equation. Putting derivative of the equation 2.1.5 into the equation 2.1.4 yields [15];

$$\frac{dV_D}{dT} = \frac{k}{q}\ln\left(\frac{I_D}{I_S}\right) - \frac{mkT}{qT} - \frac{E_g}{qT} = -\frac{\frac{mkT}{q} + \frac{E_g}{q} - V_D}{T} \tag{2.1.6}$$

where, m is a constant between 2.5 and 5, k is the Boltzmann constant, q is the electron charge, T is the temperature, V_D is the diode forward bias voltage, and E_g is the bandgap energy of silicon. For a constant current bias of 8 μA, m is taken as 2.5, V_d is simulated as 837 mV, and the resulted temperature sensitivity of the diode microbolometer is found as -6.96 mV/K. This temperature sensitivity is calculated for 6 serially connected diodes, which is the implemented diode number in order to increase the temperature sensitivity of the microbolometer.

2.2 Thermal Time Constant (τ)

Thermal time constant is defined as the time required for the temperature of the structure to decrease 1/e of its value when the infrared radiation falling on the pixel is instantaneously removed. Thermal time constant can be formulated as follows;

$$\tau = \frac{C_{th}}{G_{th}} \tag{2.2.1}$$

where, τ is the thermal time constant in seconds, C_{th} is the thermal capacitance of the structure in Joules/Kelvin, and G_{th} is the thermal conductance of the structure in Watts/Kelvin. The temperature rise of the structure increases as the thermal isolation of the pixel improves, i.e.

thermal conductance decreases. Thermal time constant should be as low as possible in order for the pixel to follow instant temperature changes.

2.2.1 Thermal Capacitance (C_{th})

Thermal capacitance is defined as the ability of the structure to withhold its temperature. It can be expressed as;

$$C_{th} = cV \tag{2.2.1.1}$$

where, c is the specific heat of the layer in J/cm^{3}K and V is the volume of the layer in cm^3. In order to decrease thermal time constant, thermal capacitance should be decreased. Only making the pixel smaller since specific heat is constant can decrease thermal capacitance. Table 2-2 shows the thickness of the layers in the process used for producing the microbolometer [20].

Table 2-3 gives the specific heat values of the layers in the pixel structure of the microbolometer that has significance in calculations, and the calculated thermal capacitance value of the microbolometer [26].

Table 2-2: Thickness of the layers in in the process used for producing the microbolometer [20].

Layer	Thickness (µm)
Field Oxide	0.9
Polysilicon	0.3
Poly Metal-1 Oxide	1
Metal-1	0.72
Metal-1 Metal-2 Oxide	0.65

Layer	Thickness (µm)
Metal-2	0.65
Metal-2 Metal-3 Oxide	0.65
Metal-3	0.94
Active Silicon	0.25
Buried Oxide	1

Table 2-3: Specific heat values of the layers in the pixel structure of the microbolometer, and the calculated thermal capacitance value of the microbolometer [26].

Specific Heat (J/cm^{3}K)	Metal	2.24
	Oxide	1.74
Thermal Capacitance (J/K)	C_{th}	4.26×10^{-9}

2.2.2 Thermal Conductance (G_{th})

Thermal conductance is the measure of a detector that shows how good the detector is thermally isolated from its surroundings. Therefore, it can be expressed as the sum of all the heat loss mechanisms of the pixel structure [6]. The major heat loss mechanism of the uncooled microbolometer is the support arms. Thermal conductance of the support arms can be expressed as follows;

$$G_m = \sigma_m \frac{A_m}{L_m} \tag{2.2.2.1}$$

where, σ_m is the thermal conductivity of a material, A_m is the cross sectional of that material, and L_m is the length of the material. Thermal conductance of the support arm is calculated by summing all the thermal conductance of the materials used in the structure. The value of thermal conductance of one support arm must be multiplied by the number of arms used in the pixel structure to find overall thermal conductance. For good isolation, materials with low thermal conductivity and smaller cross sectional areas should be preferred.

Table 2-4 shows the thermal conductivities of the specific layers used in the support arm of the microbolometer, and overall thermal conductance of the designed microbolometer. Designed microbolometer has 0.5 um polysilicon support arms since polysilicon is the best choice in regards for thermal isolation and sheet resistance. Overall thermal conductance and the time constant of the pixel structure are obtained with the help of Table 2-2.

Table 2-4: Thermal conductivities of the specific layers used in the support arm of the microbolometer, and overall thermal conductance of the designed microbolometer [26].

Parameters		Value
Thermal conductivity (W/m.K)	Poly	30
	Metal	194
	Oxide	1.22
Thermal Conductance (W/K)	G_{arm}	242×10^{-9}
Thermal Time Constant (ms)	τ	17.6

2.3 Responsivity

Responsivity is a measure of how good the detector converts an infrared radiation to an electrical signal. It is defined as the ratio of the detector output signal to the incident infrared radiation. Responsivity can be applied for an array as well as a single pixel. The detector output for a diode microbolometer is voltage depending on the biasing. Therefore, responsivity of a diode microbolometer is expressed in Volts/Watts (V/W).

Figure 2-2 shows thermal equivalent circuit for microbolometer detector with temperature difference ΔT, thermal capacitance C_{th}, thermal conductance G_{th}, incident infrared radiation P_{inf}, and absorption coefficient η.

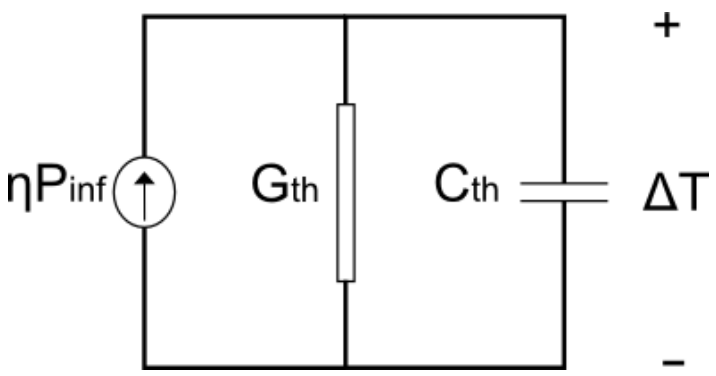


Figure 2-2: Thermal equivalent circuit for microbolometer detector.

Heat flow equation for thermal equivalent circuit with constant infrared excitation yields [6];

$$|\Delta T| = \frac{\eta P_{inf}}{G_{th}} \tag{2.3.1}$$

When the infrared radiation is modulated at w_0 frequency, temperature change can be written as [6];

$$|\Delta T| = \frac{\eta P_{inf}}{G_{th}\sqrt{1+(w_0\tau)^2}} \tag{2.3.2}$$

where, w_0 is the infrared modulation frequency and τ is the thermal time constant. Replacing temperature change, ΔT, with expression given in Equation 2.1.1 gives,

$$\Delta V_{out} = \frac{TC_d\eta P_{inf}}{G_{th}\sqrt{1+(w_0\tau)^2}} \tag{2.3.3}$$

For a constant infrared radiation, Equation 2.3.3 becomes;

$$\Delta V_{out} = \frac{TC_d\eta P_{inf}}{G_{th}} \tag{2.3.4}$$

The responsivity of a diode microbolometer can be extracted from Equation 2.3.4 as;

$$R = \frac{TC_d\eta}{G_{th}\sqrt{1+(w_0\tau)^2}} \tag{2.3.5}$$

If the incident radiation is constant, w_0 is taken as 0 and DC responsivity is found as;

$$R = \frac{TC_d\eta}{G_{th}} \tag{2.3.6}$$

Responsivity of a detector is among the most important parameters for infrared radiation applications. The responsivity should be as high as possible for better performance. Either increasing temperature sensitivity or decreasing thermal conductance of the pixel structure, i.e. thermal conductance of the support arm, can achieve higher responsivity values.

In the designed diode microbolometer structure, temperature sensitivity of diodes is calculated as -6.96 mV/K, and thermal conductance of the pixel is calculated as 242 nW/K. The absorption coefficient of the pixel is taken as 0.43 [20], which is the absorption coefficient of the pixel structure found in previous work, since both the pixels have same structure and almost same fill factor. The resultant DC responsivity of the pixel is calculated as 12360 V/K.

2.4 Noise Equivalent Power (NEP)

Noise Equivalent Power is defined as the power required for producing an output voltage that equals to the root mean square (rms) noise of the detector. NEP is expressed in Watts and given as;

$$NEP = \frac{V_n}{R} \tag{2.4.1}$$

where, V_n is the root mean square noise of the detector and R is the responsivity of the detector. Since root mean square noise depends on the bandwidth of the detector, it is important to mention the scanning rate and the size of the detector array when comparing NEP of different detectors.

There are mainly two kinds of noise sources present in the detector. These sources are shot noise of the diode and thermal noise of the supporting arm resistances. Flicker noise of the diode and the support arms are not taken into account. These calculations are done just to give us a clue about the noise levels of the microbolometer. Exact measurements are done in Chapter 4. Shot noise of a diode is defined as;

$$\overline{V_{sh}^2} = 2qI_{bias} \tag{2.4.2}$$

where, q is the electron charge and I_{bias} is the bias current of a diode. Dynamic resistance of a diode is given by;

$$r_d = \frac{dV_d}{dI_{bias}} = \frac{kT}{qI_{bias}} \tag{2.4.3}$$

where, r_d is the dynamic resistance in Ω, k is Boltzmann constant, T is the temperature in K. Replacing I_{bias} in Equation 2.4.2 with Equation 2.4.3 yields a shot noise of;

$$\overline{V_{sh}^2} = 4kT\frac{r_d}{2} \tag{2.4.4}$$

Thermal noise of a resistance is given as;

$$\overline{V_{th}^2} = 4kTR_s \tag{2.4.5}$$

where, R_s is the support arm resistance. Thermal and Shot noise components of a detector can be summed as;

$$\overline{V_{d,th}^2} = 4kT(\frac{r_d}{2} + R_s)\Delta f \tag{2.4.6}$$

where, $V_{d,th}$ is the thermal and shot noise components of a detector and Δf is the bandwidth of the detector related with the scanning rate of the detector. Total rms noise voltage of detector can be found by taking square root of sum of detector and readout circuit noises.

$$V_n = \sqrt{\overline{V_d^2} + \overline{V_{roic}^2}} \tag{2.4.7}$$

where, V_n is the total root mean square noise, V_d is the detector noise, and V_{roic} is the total rms noise voltage of the readout circuit referred to the detector side.

In the light of all of the formulations given, the equivalent resistance of each diode in the pixel is found as 3.23 kΩ, and the arm resistance is calculated as 3.63 kΩ. The noise contributions of the diodes are calculated as 1.6×10^{-16} V^2/Hz, and the noise contributions of the arm resistances is calculated as 1.2×10^{-16} V^2/Hz. This results in a 1.02 μV_{rms} total integrated output noise for 30 frames per second imaging operations. Since the detector is the dominant part in terms of noise when compared to ROIC, detector noise can be taken as overall noise value. For a constant infrared radiation, DC NEP is found as 8.27×10^{-11} Watts.

2.5 Noise Equivalent Temperature Difference (NETD)

NETD is defined as the temperature difference of a blackbody that generates an output voltage at the detector that equals to the root mean square noise of the system. NETD also shows the minimum detectable temperature difference for the detector. NETD is a performance parameter of focal plane arrays, which also has information about the optics. NETD has a unit of K and defined as [6];

$$NETD = \frac{4F^2 V_n}{A_d R(\frac{\Delta p_{target}}{\Delta T_{target}})_{\lambda_1-\lambda_2}} \tag{2.5.1}$$

where, F is the F-number of the optics, V_n is the rms voltage noise, A_d is the infrared absorbing area of the detector, R is the responsivity of the detector, and $(\Delta p_{target}/\Delta T_{target})_{\lambda 1-\lambda 2}$ is a constant which is defined as the change in power per unit area radiated by a blackbody per temperature change in the target (ΔT), measured within the spectral bandwidth from λ_1 to λ_1 [6]. For 8-14 μm spectral band at 300 K, the value of this constant is 2.62×10^{-4} W/cm^{2}K [6]. If the target is at infinity, $4F^2$ can be written as;

$$4F^2 = 4(\frac{f}{D})^2 + 1 \tag{2.5.2}$$

where, f is the focal length of the optics and D is the diameter of the optics. For f/1 optics, meaning f/D equals to 1, $4F^2$ is taken as 5. Table 2-5 gives the NETD value of the designed microbolometer and the parameter values needed for NETD calculation with f/1 optics. 6

serially connected diode configuration is implemented in this thesis, unlike the previous works, which implements 1 diode [3], and 4 diodes [21] in the pixel structures.

Table 2-5: NETD value of the designed microbolometer and the parameter values needed for NETD calculation.

Parameters	Value
Absorbing Area (A_d)	25 µm×25 µm
Responsivity (R)	12360 V/W
V_n	1.02 μV_{rms}
Noise Equivalent Temperature Difference (NETD)	252 mK

2.6 Detectivity (D^*)

Detectivity is a parameter that is used to compare detectors with different pixel sizes and frame rates. Detectivity does not depend on either frame rate or pixel sizes. It has a unit of $cm.Hz^{1/2}/W$ and given as;

$$D^* = R\frac{\sqrt{A_d \Delta f}}{V_n} = \frac{\sqrt{A_d \Delta f}}{NEP} \tag{2.6.1}$$

where, R is the responsivity of the detector, A_d is the absorbing area of the detector, Δf is the electrical bandwidth, and V_n is the rms voltage noise measured in the specified bandwidth. As D^* increases, the performance of the detector also increases.

The detectivity of the designed microbolometer is found as $1.84x10^9$ $cm.Hz^{1/2}/W$. Thermal detectors with reasonable performances require high detectivity values such as 10^{10} $cm.Hz^{1/2}/W$ or more [6]. For higher detectivity, responsivity of the detector should be as high as possible, and rms noise of the detector should be as low as possible.

2.7 Conclusion

This chapter stated the figure of merits for infrared detection. These figures of merits enable to compare different microbolometer arrays. Table 2-6 shows the important properties of the designed microbolometer and the figures of merits of the designed microbolometer for uncooled thermal imaging applications.

Table 2-6: important properties of the designed microbolometer and the figures of merits of the designed microbolometer for uncooled thermal imaging applications.

Parameters	Value
Temperature Sensitivity	-6.96 mV/K
Thermal Time Constant	17.6 ms
Thermal Capacitance	$4.26×10^{-9}$ J/K
Thermal Conductance	$242×10^{-9}$ W/K
Noise Equivalent Temperature Difference (NETD)	252 mK
Detectivity (D^*)	$1.84×10^9$ $cm.Hz^{1/2}/W$

CHAPTER 3

A 160×120 MICROBOLOMETER IMAGING SENSOR

This chapter explains the design and implementation of the 160×120 low-cost low-power microbolometer circuit. First, Section 3.1 provides brief information about the developments made for this thesis work. Then, Section 3.2 gives the architecture of the 160×120 microbolometer imaging sensor and mentions the sub blocks of this architecture. And finally, Section 3.3 explains the top level integration, along with a summary of the implementation.

3.1 Introduction

As explained in Chapter 1, there are three important design advancements for this thesis work. These important advancements are namely, smaller chip size, compatibility with the FPGA, and sufficiency on its own, i.e., the microbolometer should be able to work without need for lots of different bias voltages or bias currents.

There are two important factors affecting the size of the microbolometer. The first one is the pixel pitch. The pixel pitch of the designed microbolometer is reduced from 70 µm [21] to 40 µm. Reducing the pixel pitch affects two important parameters of the microbolometer design. The first parameter is the thermal conductance of the pixel structure. Length of the support arm is directly related with the pixel pitch. As the pixel pitch reduces, length of the support arm also reduces. The reduction in the support arm length causes thermal conductance of the pixel structure to increase. The increase in the thermal conductance results in lower NETD values. To be able to compensate the reduction in the length of the support arms, the width of the support arms is also reduced to 0.5 µm. This gives us higher support arm resistance and higher noise contribution through the support arms.

The second important parameter that is affected from the reduction in the pixel pitch is the length of the diodes implanted on the pixel structure. When the pixel pitch is reduced, the length of the diodes implemented on the pixel area is also reduced. Smaller diode length results in higher forward bias voltage of a diode, and hence lower temperature sensitivity of the detector as explained in Section 2.1. To be able to compensate the reduction of the temperature sensitivity, number of series diodes implemented in the pixel area is increased. The increase in the number of series diodes means that supply voltages for the pixel biases should

also be increased. Therefore, the microbolometer needs higher bias voltages for pixel voltage biases. Analog blocks driving the pixel supply voltages should be designed carefully to operate in this high voltage range. The design is explained in Section 3.2.

The second factor affecting the chip size is the length of the readout channel. To be able to reduce the length of the readout channel of the microbolometer, the readout architecture for this thesis work is re-designed. The readout architecture is made double-sided, and new approach is implemented in the readout architecture. The re-design of the readout architecture is also explained in Section 3.2.2.

Another important feature of this thesis work is that the microbolometer should able to talk with the FPGA without need of any external elements. The microbolometers designed before this thesis work has only 5 V digital inputs or digital outputs. This results in use of external level shifter circuits for both inputs and outputs. This need increases the dependency on the external elements and the size of the board. Therefore, in this work internal up and down level shifters implemented, and the need for external level shifter elements is eliminated. The detailed information about the digital blocks is given in Section 3.2.6.

The last important feature of this thesis work is that the designed microbolometer does not need any external analog biases. The microbolometer has regulators whose outputs digitally controlled with the help of R2R DACs. The microbolometer also has current-steering DACs for the current bias needs of the readout channel, and the pixel circuitry.

3.2 Architecture

Figure 3-1 shows the architecture of the designed imaging sensor. The main property of this architecture is that the designed imager can work with only power and clock inputs. This means that the imager is a stand-alone product after the etching process is done. It is obvious from the Figure 3-1 that the imager has 6 different parts: namely pixel array, column readout, output buffer, bias generator, row and column select circuits, and digital controller and serial programming interface blocks. Figure 3-2 show the analog signal chain of the designed imaging sensor.

Pixel array includes 164×124 pixels, whose 4 of the rows and 4 of the columns are used as reference pixels. These reference pixels are not exposed to etching and they are thermally blind to the infrared radiations. Column readout circuits amplify the change in the pixel voltage, and create a meaningful data for the output buffers. Output buffers are responsible for buffering the created column output voltage to the high external output capacitances. Bias generator produces the bias currents and bias voltages for column readout circuits, output buffers, and pixel arrays.

Row select circuit enables the rows one by one, and column select circuits select the columns and connect them to the output buffers sequentially. Digital controller and serial programming interface creates the necessary timing signals for the row and column select circuits, column readout. Besides producing the necessary imaging signals, digital controller also produces the signals for the chip to communicate with the outer world. These signals indicate that the conditions of the imager, which are for example the start of a new frame and start of the new line. Serial interface also defines the gain of the integration block and bias generator voltage and currents.

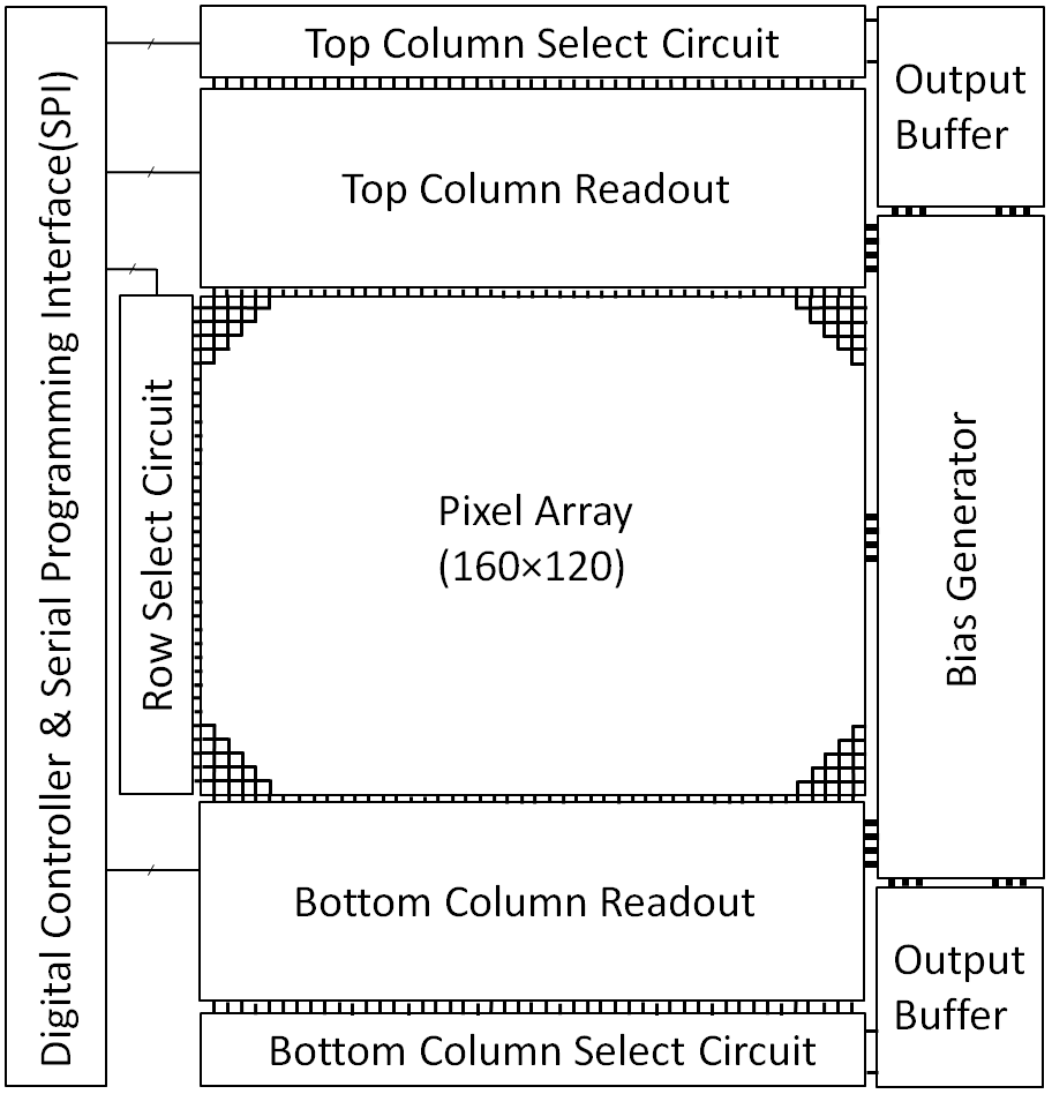


Figure 3-1: Architecture of the designed imaging sensor.

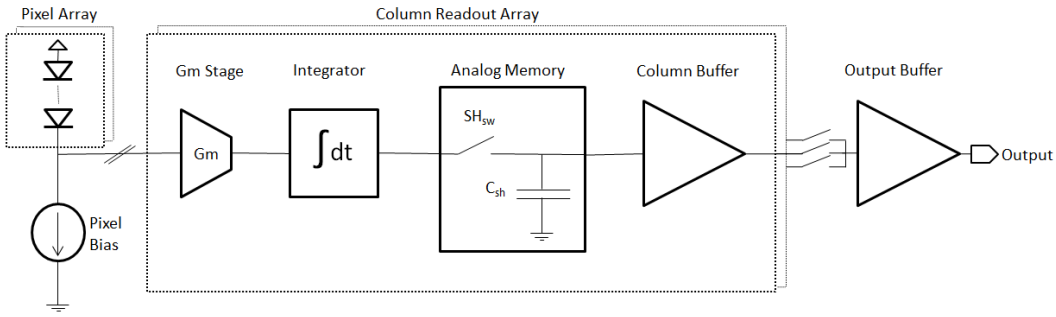


Figure 3-2: Analog signal chain of the designed imaging sensor.

Section 3.2.1 explains the pixel array and the modifications made in this thesis work. This section also mentions the important parameters explained in Section 2 with more details. Section 3.2.2 introduces the column readout architecture, and explains the important blocks of the column readout. Section 3.2.3 gives the output buffer properties. Section 3.2.4 explains the features of the implemented bias generator. Section 3.2.5 gives the working concept of both row and column scanning circuits. Finally Section 3.2.6 explains the digital controller and serial programming interface of the 160×120 microbolometer imager.

3.2.1 Pixel Array

Pixel array is composed of 164 columns and 124 rows. 4 of the rows and columns are used as reference pixels. Therefore, the name of the microbolometer is stated as 160×120 microbolometer imager. The pixel of the designed imager is 40 µm by 40 µm.

Figure 3-3 shows the pixel layout view of the designed imager. The dark green areas are arms of the suspended bridge structure. The gray areas on top of the dark areas are put in order to give a safety margin during the etching process. This area is named as support arm etch margin in Table 2-1. Table 2-1 also shows the other dimensions of the pixel. The pixel has 40 µm pitches with an absorbing area of 25 µm. The etch margins are 0.5 µm on both sides of the arms. There are also 3 µm walls on both sides of the pixel in order to have signal flow on these walls. Etch openings between the arms and the absorbing area is 1.5 µm.

Table 2-6 gives the resultant infrared imager parameters of the designed pixel. The pixel has -6.96 mV/K temperature sensitivity, 242 nW/K thermal conductance, 4.26 nJ/K thermal capacitance, and 17.6 ms thermal time constant. The resultant NETD and the detectivity of the pixel are 252 mK and 1.84×10^{9} cm.$Hz^{1/2}$/W respectively.

Figure 3-4 shows the layout (a) and the cross-section (b) view of the previously designed 70 µm pixel [21], and Figure 3-5 shows the layout (a) and cross-section (b) view of the designed imager pixel with 40 µm pitch. Both of the imaging sensors are designed in 1 µm process. This dictates a minimum feature size of 1 µm. However, this thesis work has a feature of 0.5 µm support arm width, which is less than the feature size of the process. Figure 3-5 shows us the layout and the cross-section views of the pixel when a modified process with 0.5 µm feature size is used in the pixel area.

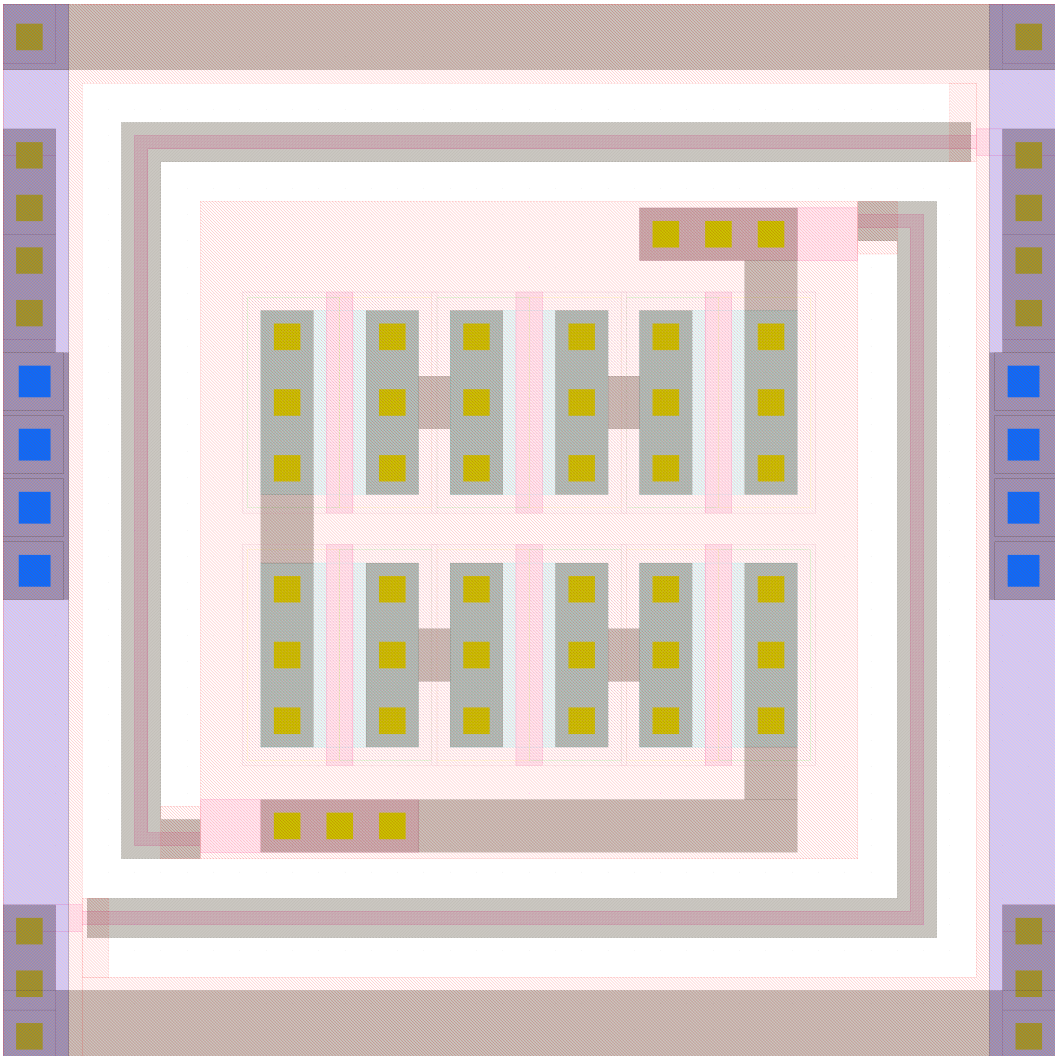


Figure 3-3: Pixel layout view of the designed imager.

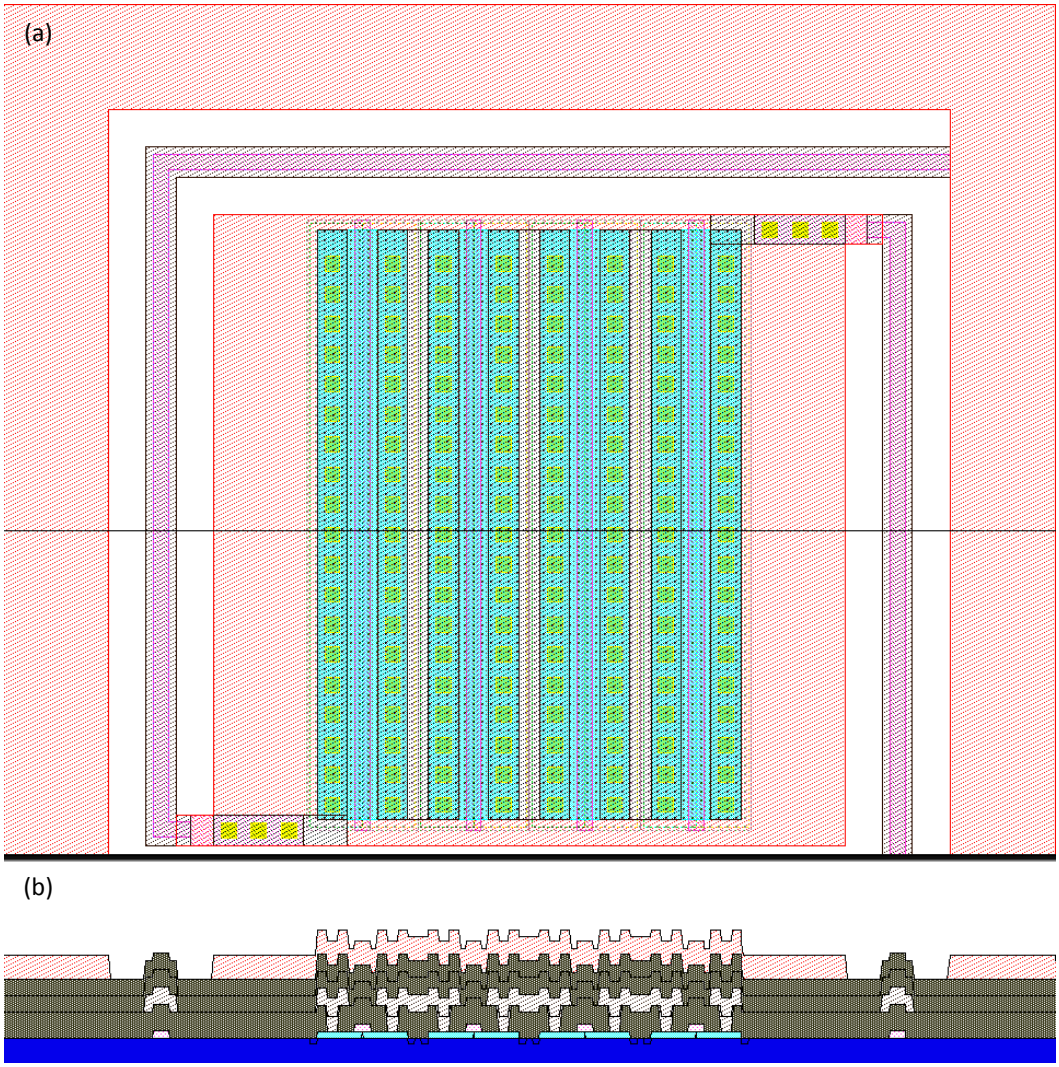


Figure 3-4: Layout (a) and cross-section (b) view of the previously designed 70 µm pixel [17].

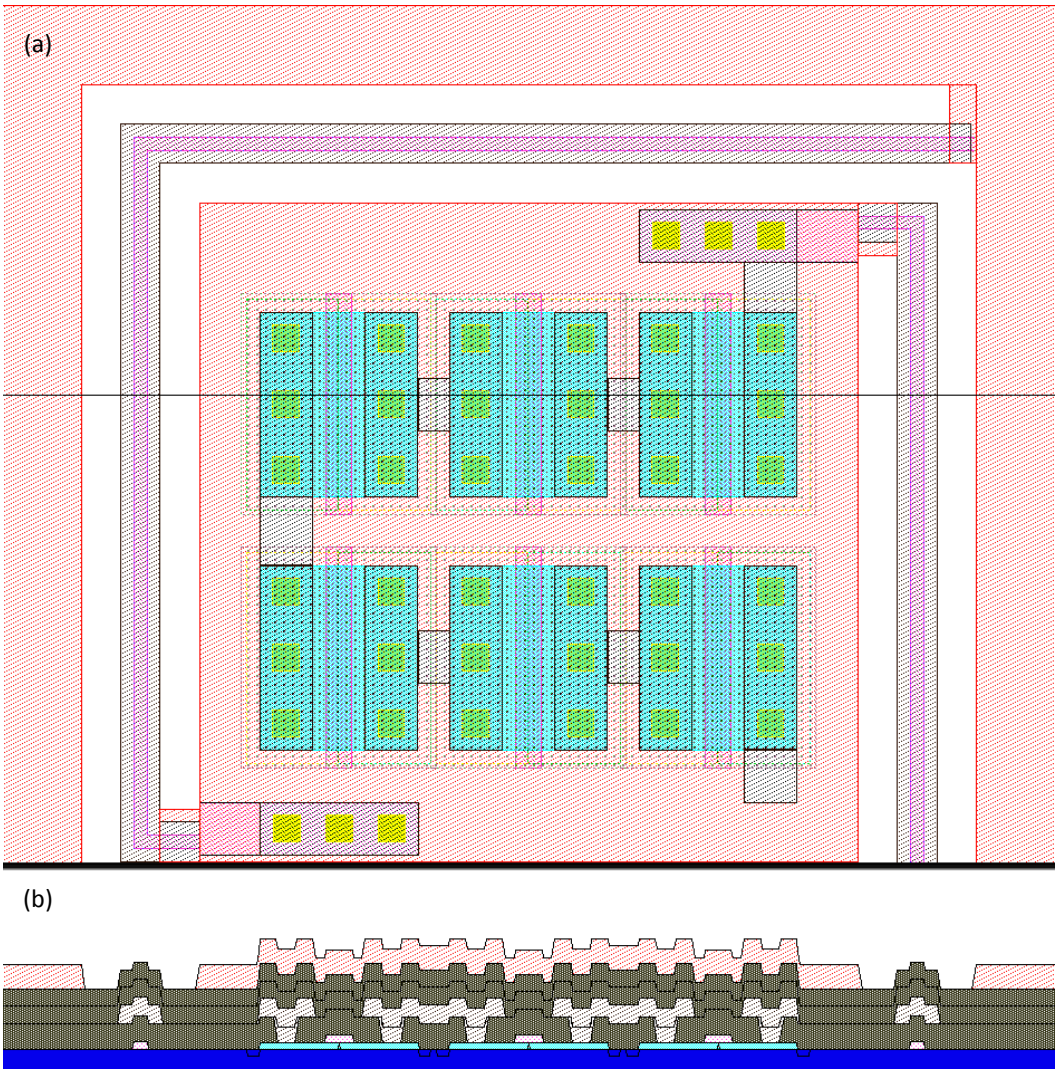


Figure 3-5: Layout (a) and cross-section (b) view of the designed imager pixel with 40 µm pitch.

After the chip is fabricated, the pixels should be suspended in order to have a thermal isolation between the bulk and the pixels, and two neighboring pixels. The designed microbolometer is an ultra low-cost imager. This is because of the fact that there is only etching involved in the post-CMOS processes. This etching process requires neither any critical lithography steps nor special masks for etching. The mask layers are also produced in the CMOS fabrication. One of the metal layers of the process is used as a mask for etching the chip. Figure 3-6 shows the post-CMOS process steps of the multi-diode microbolometer pixels in a SOI-CMOS process [18].

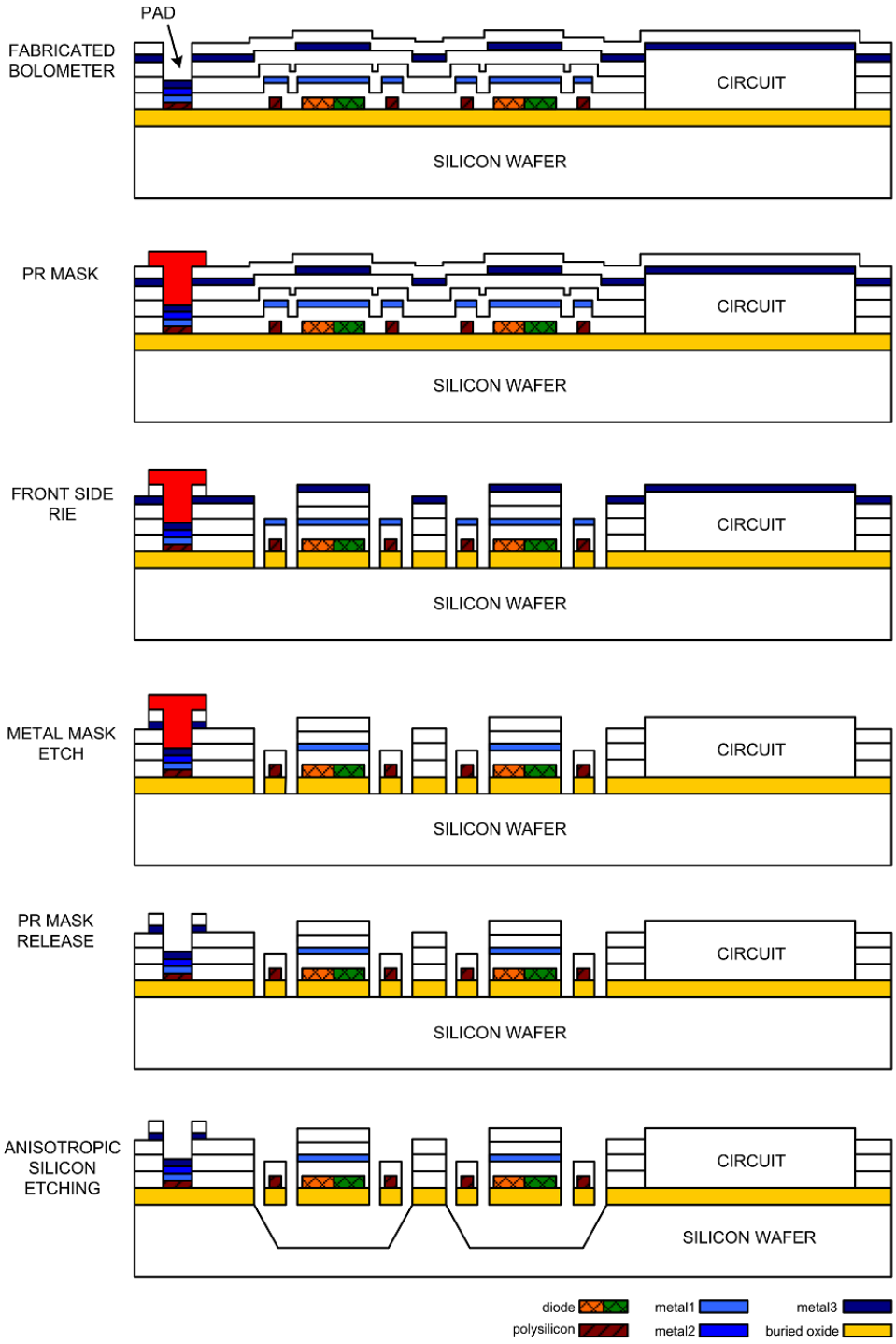


Figure 3-6: The post-CMOS process steps of the multi-diode microbolometer pixels in an SOI-CMOS process [18].

3.2.2 Column Readout

The column readout circuit is composed of three important parts: Gm stage and integrator block, analog memory block, and column buffer block. Figure 3-7 shows the block diagram of the column readout circuit. The pixel output is integrated into the integration capacitance with the help of the Gm stage and integrator. The analog memory samples the integrated voltage and sends it to the column buffers. Column buffer as the name implies buffers the sampled integration voltage to the output buffers.

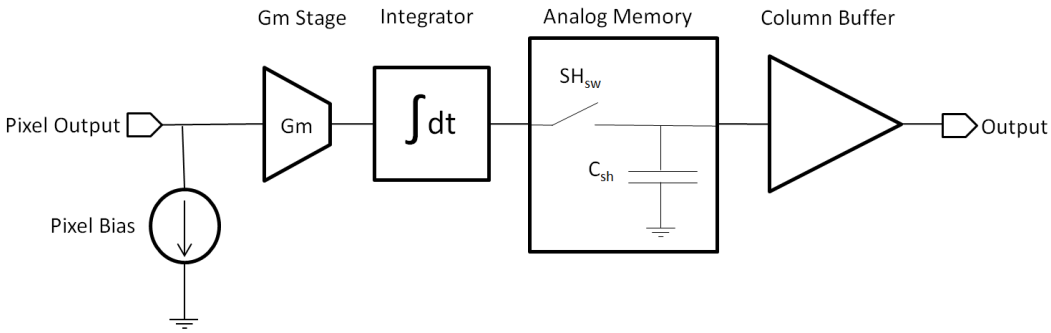


Figure 3-7: Block diagram of the column readout circuit.

The sub sections give the detailed information about the sub blocks of the column readout circuit. Section 3.2.2.1 introduces the Gm stage and Integrator block, and gives the properties of this block. Section 3.2.2.2 mentions about the analog memory of the column readout, which samples the integration voltage, and explains the newly implemented readout structure. Finally, Section 3.2.2.3 explains the column buffer, and gives the simulation results of the implemented column buffers.

3.2.2.1 Gm Stage and Integrator

Figure 3-8 shows Gm Stage and Integrator block schematics. Gm Stage and Integrator block converts the voltage difference occurring at the pixel to the readable voltage levels. For this reason, the voltage difference at the pixel is converted to the current with the Gm Stage block and then this current is converted to the readable voltage levels with the help of the integrator block.

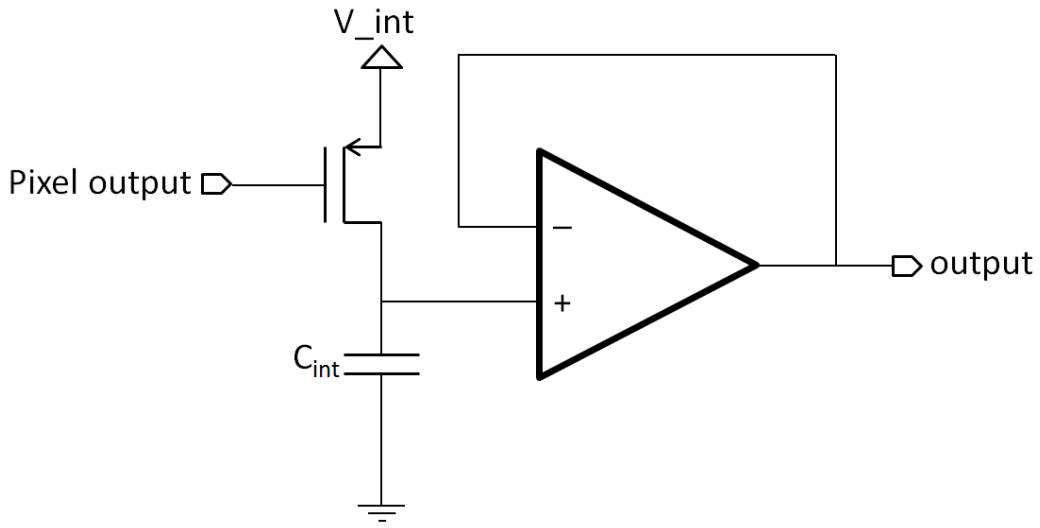


Figure 3-8: Gm Stage and Integrator block schematics.

In this thesis, Gm stage consists of only one PMOS transistor whose gate is connected to the pixel output voltage and source is connected to the integration voltage produced in the bias generator of the chip. The current flowing through the PMOS transistor is known as;

$$I_{out} = \frac{K_p}{2}(\frac{W}{L})_p(V_{int} - V_{pix})^2 \qquad (3.2.2.1.1)$$

where, I_{out} is the output current of the PMOS transistor, K_p is the gain factor of the PMOS transistor, $(W/L)_p$ is the ratio of the PMOS transistor, V_{int} is the source bias voltage of the PMOS transistor, and V_{pix} is the pixel output voltage. When the temperature of the pixel diodes increase, the voltage across the series pixel diodes decreases, and the pixel output voltage increases. The increase in the pixel output voltage results in the decrease of the output current. Therefore, integrated voltage decreases when the temperature increases. For very small changes in the pixel voltage, the integration current changes with the gm factor of the pmos transistor. The gain of the Gm stage can also be arranged via serial interface of the chip. There are 4 different (W/L) ratio gain transistors in the readout channel. Selecting between these transistors can increase the gm of the stage and hence the gain of this stage.

In this thesis, as an integrator simple capacitor is implemented. There is also another way of increasing the gain of the stage. This way is selecting between different integration capacitances. There are 1 pF, 2 pF, 4 pF, 8 pF, and 16 pF capacitances selectable in the readout channel. The maximum of selectable integration capacitance is 31 pF.

There is also operational amplifier as a buffer implemented between the integration voltage and the analog memory block. This buffer is needed for eliminating charge sharing effects between the integration capacitance and the sampling capacitance. Another reason for using this buffer is to separate the integration phase from the sample phase.

The buffer should draw as small current as possible because it is implemented in all of the readout channels, and it is active for whole line time. Another property of the buffer is that the layout should be as small as possible. The implemented buffer uses classical 5-Transistor opamp topology [27] to be able to compensate these properties.

Figure 3-9 shows the output vs. input graph of the implemented buffer. Due to 5-Transistor Opamp topology, input and output voltage swing of the buffer is limited. The input voltage of the buffer should be in the range of 0.5 V- 4.3 V. This dictates a limit on the lower limit of the integration voltage. The buffer does not work for the input voltages lower than 0.5 V properly. Therefore, integration voltage should be reset to the voltages higher than 0.5 V for a proper buffering operation between the integration and the sampling capacitances.

Figure 3-10 shows AC simulation results of the operational amplifier used as the buffer. The DC gain is simulated as 40 dB, and the phase margin is simulated as 94^{o} degrees for a 1 pF load capacitance. This DC gain corresponds to 100 V/V gain. This results in an error of 10 mV for a 1 V input voltage between input and output for buffering operation. This error is not so important because it can be eliminated with the software tools. The buffer has 60 μV_{rms} total integrated output noise with a load capacitance of 4 pF, 1 pF of which is the output capacitance of the buffer, and the other 3 pF is the sampling capacitances. The total power consumption of the all buffers is calculated as 5 mW (1 mA current drawn from 5 V supply).

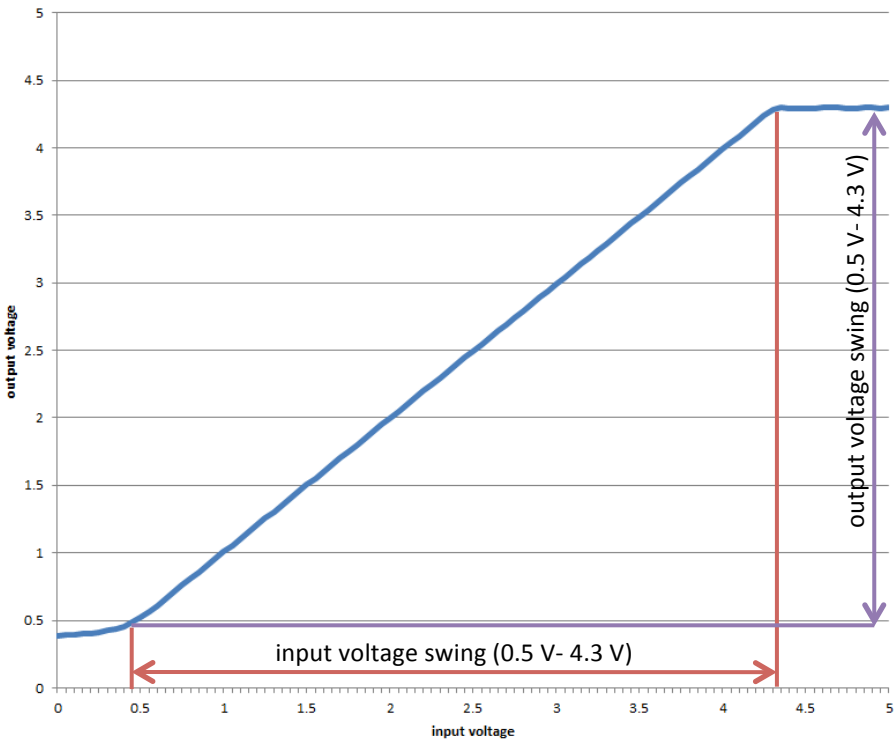


Figure 3-9: Output vs. input graph of the implemented buffer.

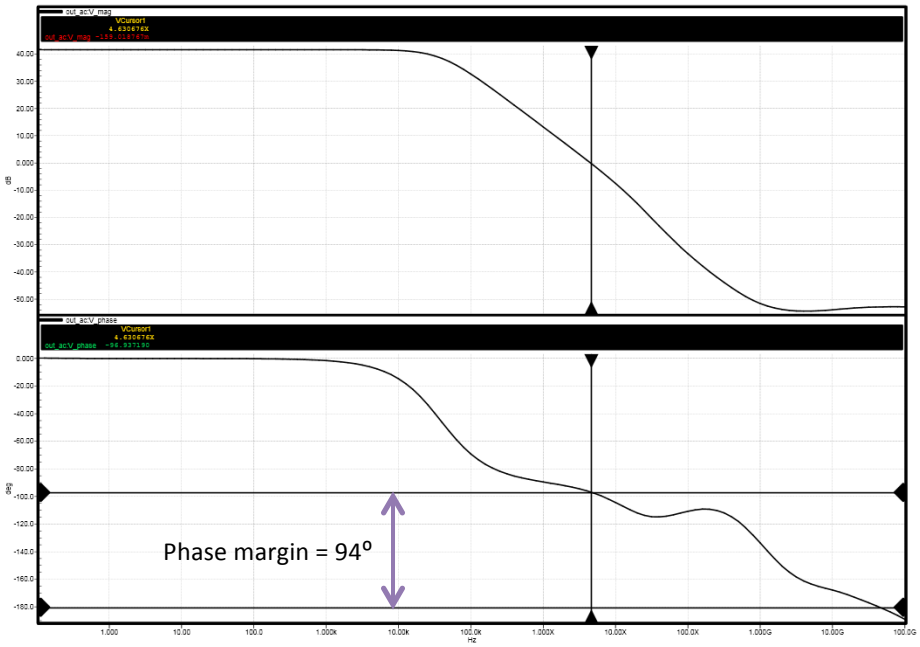


Figure 3-10: AC Simulation results of the operational amplifier used as the buffer.

3.2.2.2 Analog Memory

Analog memory consists of two components: sampling switch and the sampling capacitance. However, in this thesis work, there is a double of both of these components. Figure 3-11 shows the analog memory structure, implemented newly in this infrared imaging sensor.

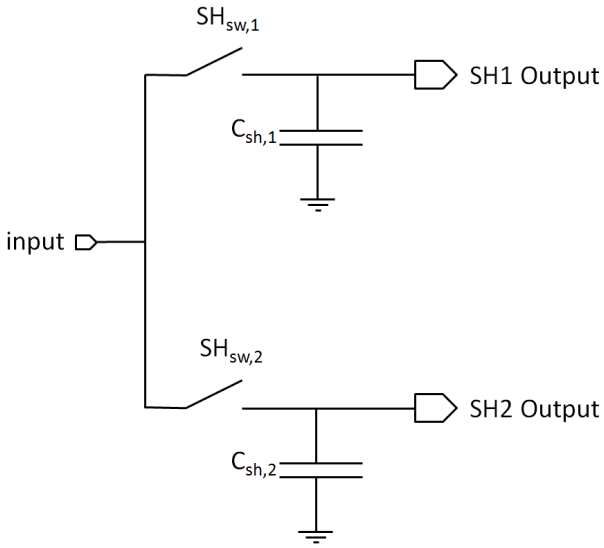


Figure 3-11: Analog memory structure.

There are different reasons of why there are two sampling switches and two sampling capacitances in the analog memory structure of this column readout circuit. One of the sampling capacitances is used to sample the integration voltage when the reset operation takes place. Reading the reset voltage with the column readout circuit and accepting this voltage as a reference voltage for the analog to digital converter decreases the supply related and system related noise effects. This phenomenon can also be appreciated as correlated double sampling, and this decreases the reset noise of the system. Therefore, double reading structure is implemented in the analog memory of the column readout circuit.

3.2.2.3 Column Buffer

Column buffer is implemented for separating the sampling capacitance from the output multiplexers to avoid any charge sharing effects. The other reason for implementing the column buffer in the column readout is to drive the long common busses with large capacitive loads. Therefore, column buffers are designed as an operational amplifier but used in the buffer configuration.

Column buffers are implemented in all of the readout channels. Therefore, the power dissipation should be as small as possible. The column buffer should be able to drive large capacitances in a small time period because 82 columns will be sent to the output multiplexer in one line time. The input and output swing of the column buffer should be in the same range with the buffer used in the Gm stage and integrator block. Therefore, folded cascode operational amplifier topology is used for column buffer design. Figure 3-12 shows the folded cascode operational amplifier topology [27].

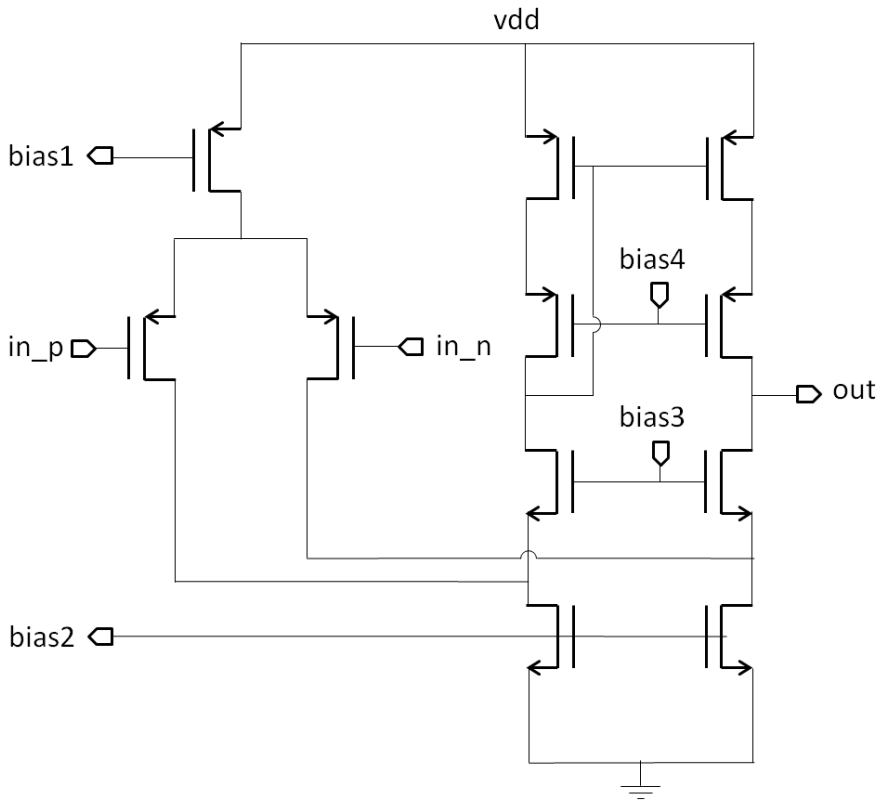


Figure 3-12: Folded cascode operational amplifier topology [27].

Figure 3-13 shows the output vs. input graph of the column buffer. The input and output voltage swing of the column buffer is between 0.1 V-3.9 V ranges. Figure 3-14 shows the AC simulation results of the operational amplifier used as the column buffer. The gain of the operational amplifier is 80 dB, and the phase margin is 75^{o} degrees for the load capacitance of 1 pF. Column buffer has an integrated output noise of 70 μV_{rms} with a load capacitance of 4 pF for the whole band.

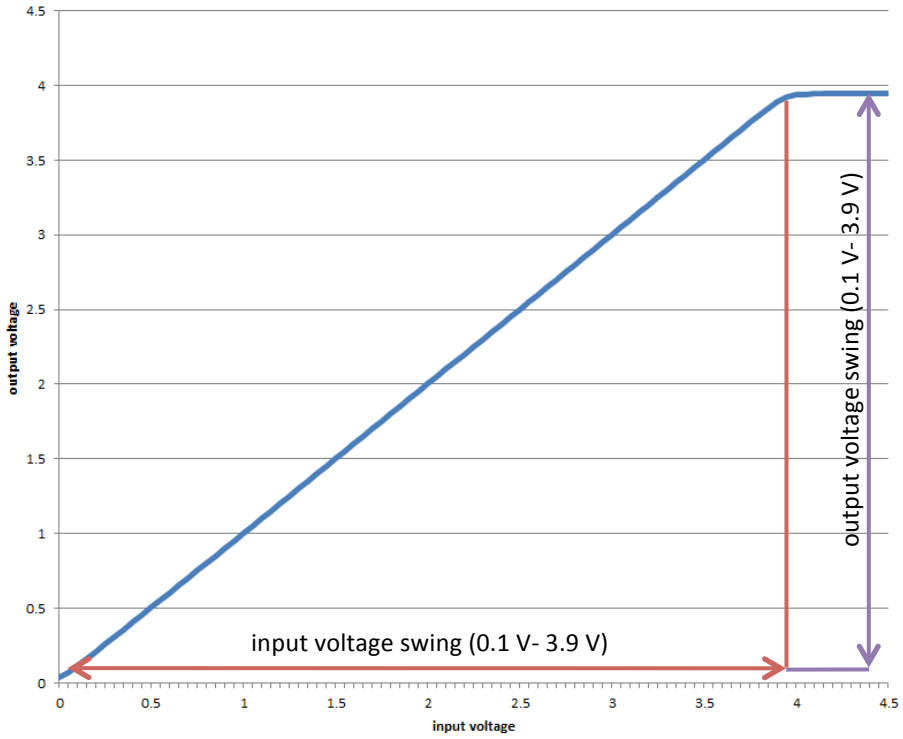


Figure 3-13: Output vs. input graph of the implemented buffer.

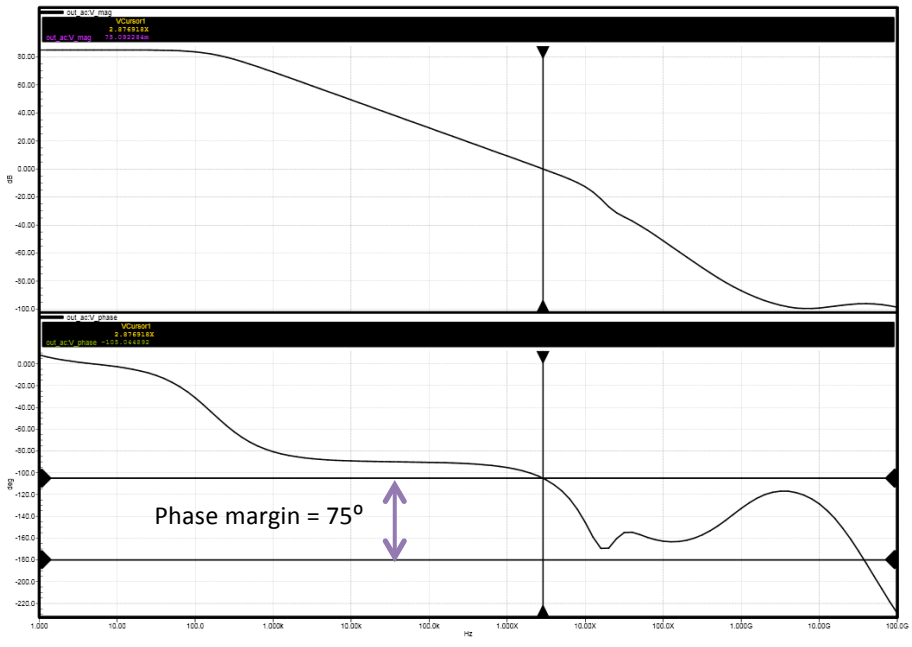


Figure 3-14: AC simulation results of the operational amplifier used as the column buffer.

3.2.3 Output Buffer

Output buffer is used for driving external capacitive loads with the processed pixel voltages. There are two output drivers for the outputs of the top column readout and two output drivers for the output of the bottom column readout array. One of the output drivers is used for driving the reset voltage and the other one is used for driving video voltage to the analog to digital converter.

Output buffers implement a buffer connected operational amplifier. The topology of the operational amplifier is selected to be a folded cascade topology [27]. This topology is chosen because of the drive capability of the capacitive loads and output swings of the previous blocks, such as column buffers.

Figure 3-15 shows the output vs. input graph of the output buffer. The input and output voltage swing of the output buffer is 0.2 V- 3.8 V. This swing is enough for buffering the column buffer outputs to the external loads.

Figure 3-16 shows the AC simulation results of the operational amplifier used as the output buffer. The gain of the operational amplifier is 70 dB, and the phase margin is 88° degrees with a load capacitance of 20 pF. Total integrated output noise of the output buffer is 36 μV_{rms}.

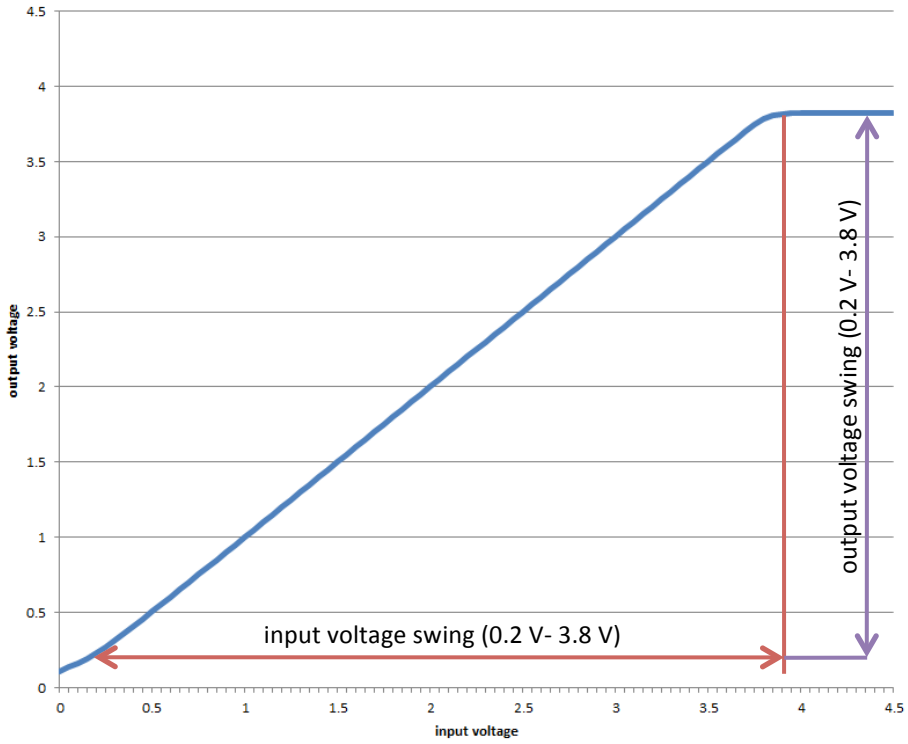


Figure 3-15: Output vs. input graph of the output buffer.

Figure 3-16: AC simulation results of the operational amplifier used as the output buffer.

Settling is one of the most important parameters of the output buffers. The designed buffer can drive up to 20 pF loads with a 0.7 µs settling time. Figure 3-17 shows the transient simulation results of the output buffer with 20 pF load: (a) input voltage, (b) output voltage. For this transient simulation, the input voltages change between 0.7 V and 3.0 V with a frequency of 100 kHz. The frequency is selected as low in order to measure the settling error of the output buffer.

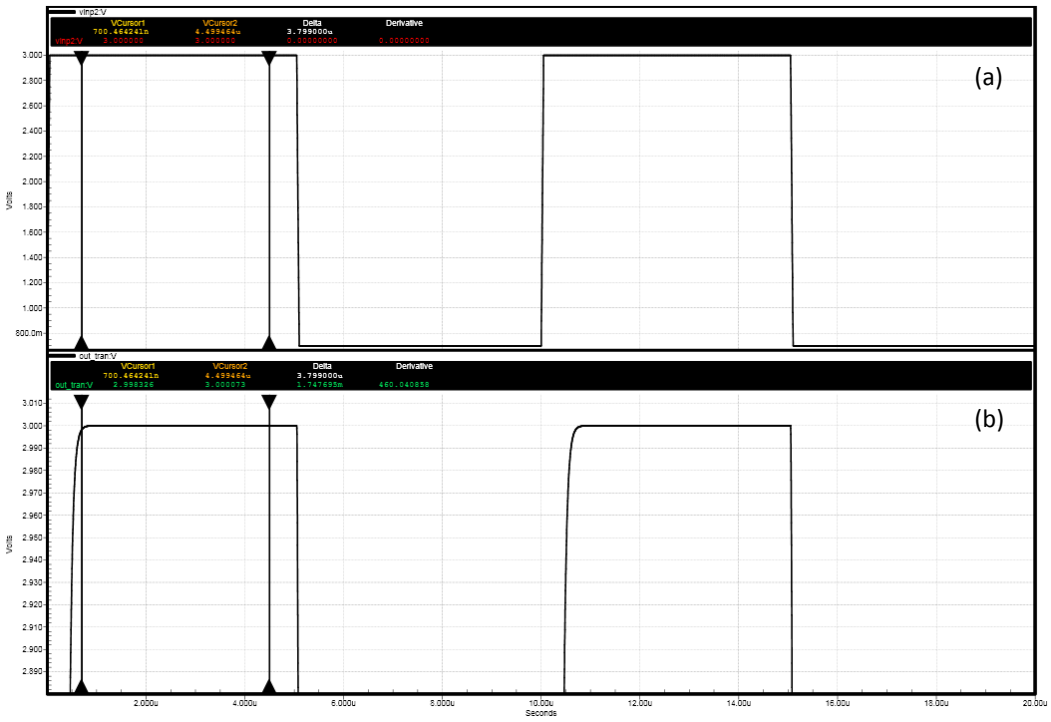


Figure 3-17: Transient Response of the output buffer with 20 pF load: (a) input voltage, (b) output voltage.

Conclusion of the transient simulation of the output buffer: Output buffer can be used to drive 20 pF load at sampling rate up to 1 MHz (with a settling time of 700 ns) with a settling error of 1.74 mV corresponding to 0.05% of the input voltage. The current need of the output driver when it is used in the same configuration with the transient simulation is obtained as 250 µA. this results in 1.25 mW power consumption for each of the output buffers.

3.2.4 Bias Generator

The bias generator produces the voltage and current biases of the pixel array, the column readout, and the output buffers. The 160×120 microbolometer imager is designed so as to need minimum number of external bias or power supplies; it is desired to be the system on a chip microbolometer imager. The voltage and currents produced in this block can also be configured throughout the serial interface of the chip.

Figure 3-18 shows the bias generator block diagram. Bias generator works with the power supply of 7 V in order to produce the pixel bias voltage in the bias generator circuit. There is an

internal bandgap circuit producing 1.2 V. This bandgap voltage is then multiplied with 5.5 to produce the reference voltage. The reference voltage of 6.5 V is then used in the other voltage and current DACs to produce the temperature independent low noise voltage and current biases of the sub blocks of the imaging sensor.

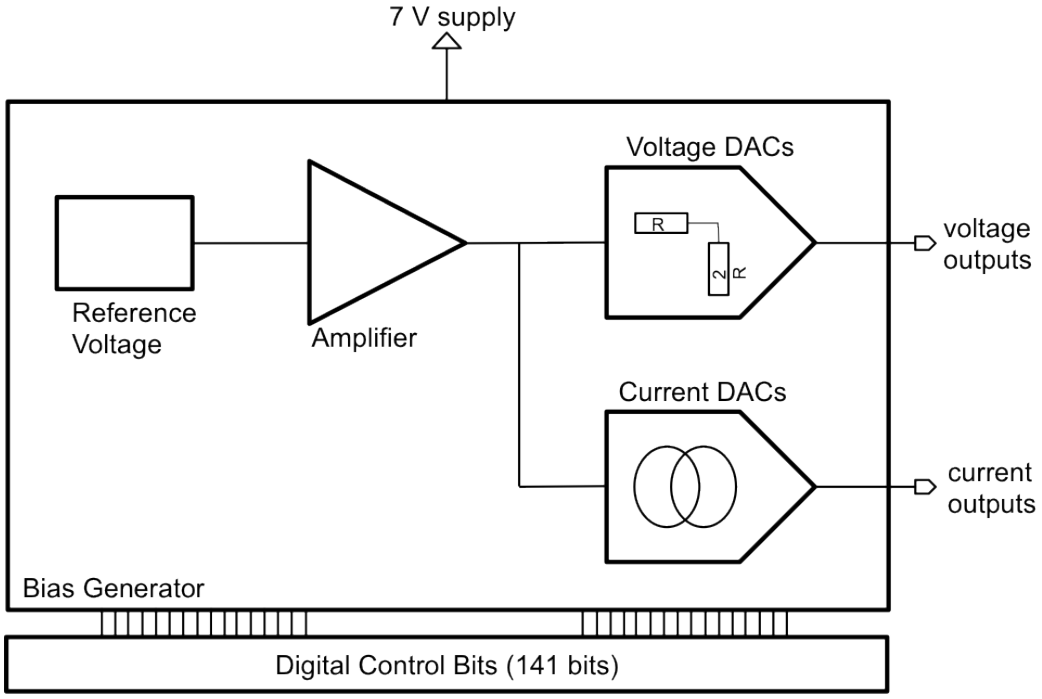


Figure 3-18: Bias generator block diagram.

The voltage DACs include R2R DAC and a regulator. R2R DACs have 8 bits resolution, and minimum step size of the R2R is 25 mV. The regulator consists of a 5 Transistor operational amplifier and a pmos transistor as an output transistor. The input and output swing of the DACs is limited to 2 V- 6.4 V. The operational amplifier dictates the lower limit and the output pmos transistor dictates the upper limit. The current steering DACs have 7 bits resolution with a step size of 1.25 µA. The swing of the current steering DACs is 1.25 µA- 158.75 µA.

The most important voltage that the bias generator produced is the pixel bias voltage. Therefore, the noise of this voltage is simulated. The produced pixel bias voltage has a 33 μV_{rms} total integrated noise when there is no external capacitance to limit the bandwidth of this supply. However, when there is an external 100 pF capacitance at this supply voltage, the total integrated output noise drops to 8 μV_{rms}.

3.2.5 Row and Column Select Circuits

There are 124 rows and 164 columns are implemented in the designed imager. 2 of the rows and 2 of the column are designed as reference rows and reference columns. The pixels in these rows are blind to infrared radiation, and do not respond to the thermal changes. Main responsibility of the selection circuits are enabling the rows for the integration and connecting the column outputs to the output multiplexers.

Shift register based addressing scheme is used for both row selection and the column selection circuits. Shift register consists of D Flip Flops connected successively. At the rising edge of the clock pulse the data in the previous memory element is transferred to the next memory element. For selecting one row or one column at a time, the data of the shift register should be one clock cycle pulse width of the clock of the shift register.

Figure 3-19 shows the row selection circuit schematics (a) and expected output waveforms (b). Only one row is selected at a time, and the pixel voltages are integrated in the column readout. Therefore, shift register based addressing scheme is used as the row selection circuit. Row selection circuit consists of 123 bits shift register to select each row separately. Top 2 and bottom 2 rows are named as reference rows.

Figure 3-20 shows the column selection circuit schematics (a) and expected output waveforms (b). There are two of the column selection circuits implemented in the design, one is for top column readout array and the other is for bottom readout array. Each of the column selection circuit has 82 bits shift register. Since the columns are connected in an interlaced manner, the first and last elements of the shift registers select the reference columns outputs.

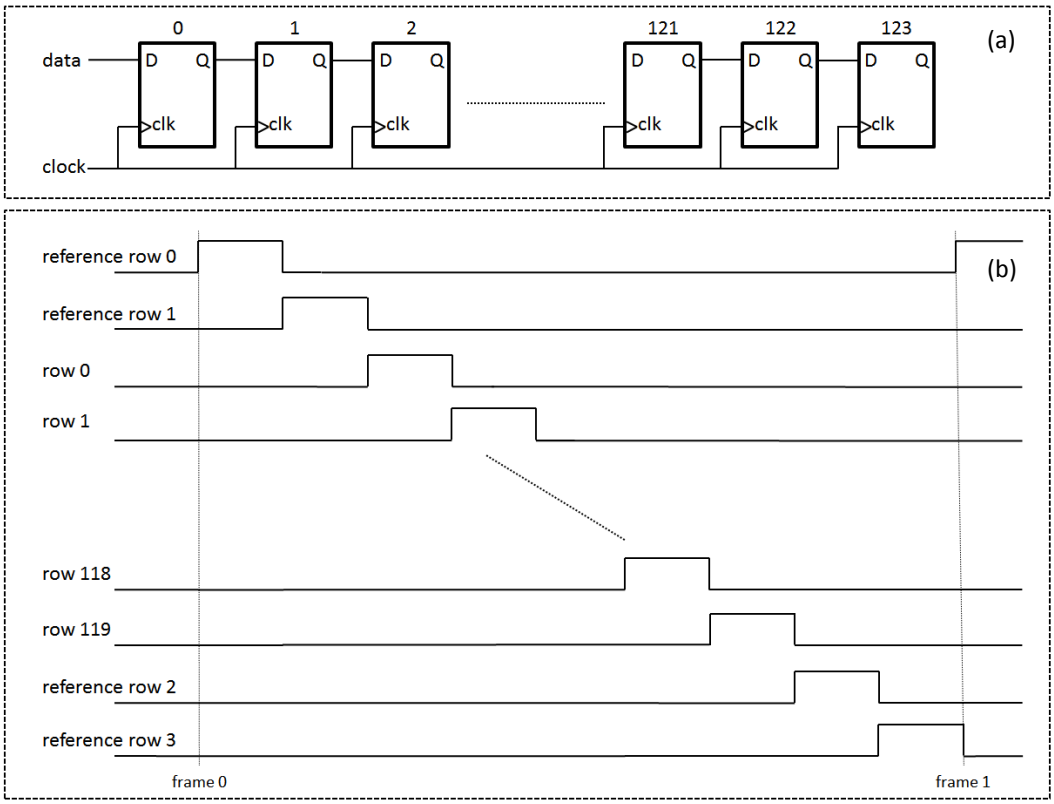


Figure 3-19: Row selection circuit schematics (a) and expected output waveforms (b).

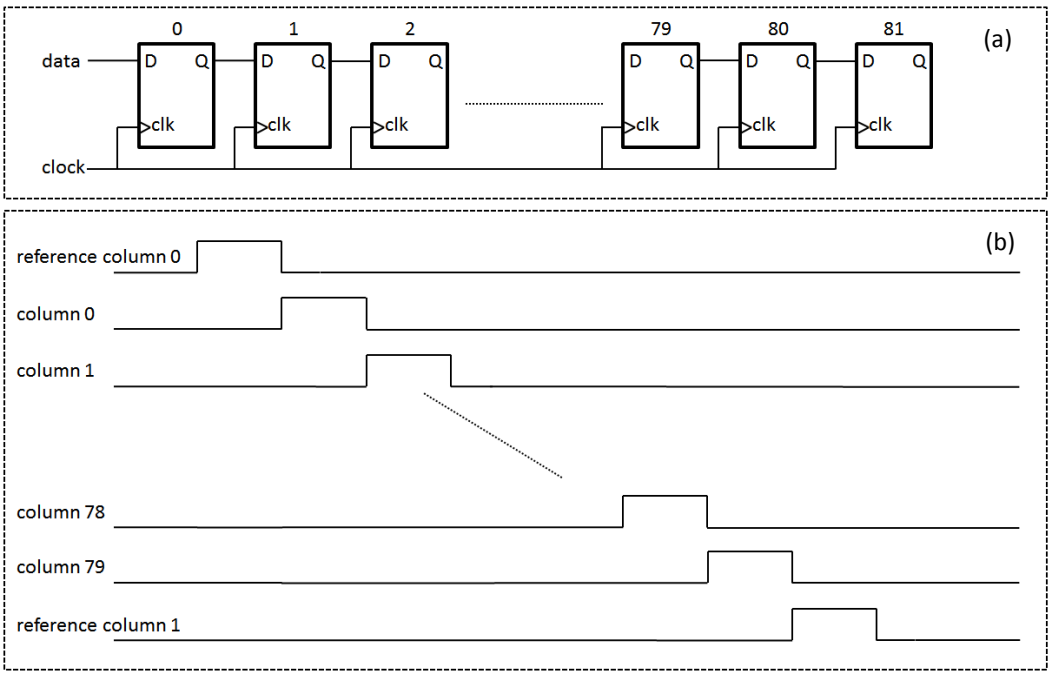


Figure 3-20: Column selection circuit schematics (a) and expected output waveforms (b).

Figure 3-21 shows the timing scheme of the selection circuit signals. Row selection circuit needs three signals, namely *start_vs* and *clk_vs*. Data of the shift register is named as *start_vs*, and clock of the shift register is *clk_vs*. Column selection circuit needs also the same signals, *start_hs* and *clk_hs*. Data of the shift register is named as *start_hs*, and clock of the shift register is *clk_hs*. The layout placement is the reason for the extensions of these names, "vs" comes from the vertical selection, and "hs" comes from the horizontal selection.

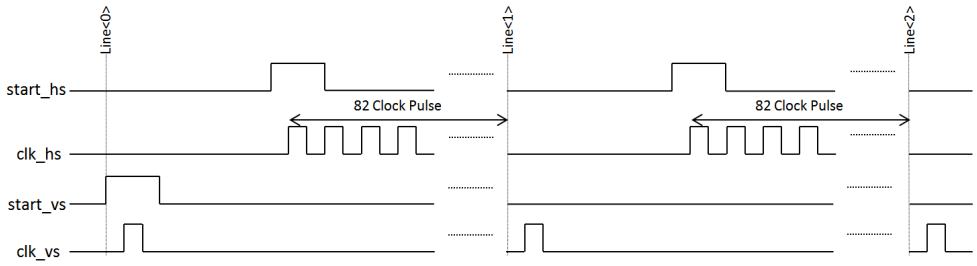


Figure 3-21: Timing scheme of the selection circuit signals.

3.2.6 Digital Controller and Serial Programming Interface

The digital controller creates the necessary digital signals for the column readout and the output multiplexer. Serial programming interface is used for adjusting the bias voltages, bias currents, column readout gain, line time, integration time, and sampling times.

The process dictates the digital cells at 5 V, but the FPGA sends the signal in 3.3 V logic. Therefore, a level shifter is designed for easy communication between the FPGA and the chip. The up level shifter (5 V to 3.3 V) is just like the normal inverter whose supply voltages are connected to the 3.3 V supply. However, for down conversion process, this type of structure could not be used because of the fact that the transistors do not completely turn off at steady state. Therefore, contention-mitigated level shifter topology is used [28]. In stable operations, there occurs no current flow from the digital power to the ground.

The serial interface is the communication port of the microbolometer with the FPGA. The serial peripheral interface (SPI) uses 4 wire communication, serial data input, active low enable signal, active low reset signal, and serial clock. Serial clock and the reset inputs are same with the system clock and system reset inputs. Therefore, extra 2 pins are added to the system.

Figure 3-22 shows the serial interface timing scheme. The microbolometer has 212 bits of memory, 79 of them for digital signals and 141 of them for analog signals. The memory is shift register type memory. There are two registers in the memory structure; shadow register and memory register. 212 bits are serially shifted through shadow registers if the enable signal is low. When the enable signal goes from low to high, memory registers are updated with the shadow register data.

Figure 3-22 also states the order of bits in the communication procedure. The FPGA should send data to the chip from LSB to MSB. For better operation, FPGA should change the data at the negative edge of the clock signal since the data is sampled at the positive edge of the clock inside the chip. Serial data output pin gives the data starting from LSB to MSB. When the data is written twice to the chip, serial data output pin shows the written data.

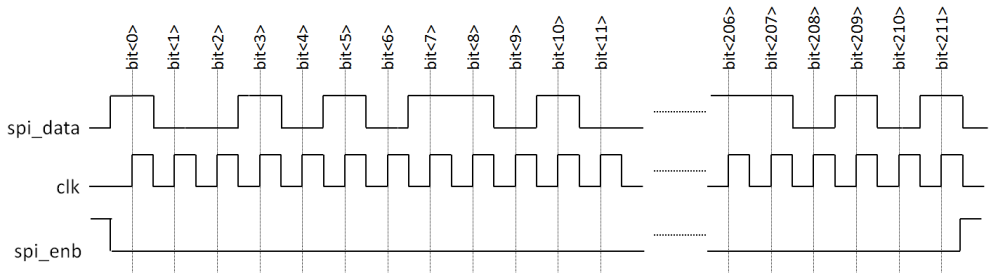


Figure 3-22: The serial interface timing. Chip samples spi_data at the positive edge of clock.

The digital controller generates the necessary time-dependent for the readout circuit. The implemented readout scheme for this thesis work is rolling line type. This means that pixels are integrated row by row with the same integration time. The integration time and the read time cycles are separated in one line time operation. The imaging operation is as follows: the column

readout array integrates all the pixel voltages into the integration capacitances, two sampling data are taken during the integration, and then the sampled voltages fed to the output multiplexers.

Table 3-1 gives the readout signals created in the timing generator block and their functions. There are mainly 5 different signals needed for the readout circuit. These signals are for row selection, integration enabling, and reset operation, first and second sampling and column selection purposes.

Table 3-1: Readout signals created in the timing generator block and their functions.

Block Name	Signal Name	Signal function
Row scanning circuit	*start_vs*	Data of the shift register of row scanning circuit
	clk_vs	Clock of the shift register of row scanning circuit
Column scanning circuit	*start_hs*	Data of the shift register of column scanning circuit
	clk_hs	Clock of the shift register of column scanning circuit
Column readout	*reset_en*	Resets the integration capacitance to known voltage.
	int_en	Starts the integration
	SH1_en	Samples the integration or reset voltage, 1^{st} sampling,
	SH2_en	Samples the integration voltage, 2^{nd}sampling,
Output Multiplexer	*clk_av*	Multiplexes the top and bottom outputs

Figure 3-23 gives the general timing scheme of the column readout signals. The red pointers in Figure 3-23 can be arranged through the serial interface of the chip. Some of the signals produced in the block are configurable through the serial interface of the chip. However, some of them are not configurable. Reset enable signal (*reset_en*) is one of the signals which is not configurable, and it start with the every line, and goes high for 10 clock cycle then goes low. The start and end of the row and column selection circuit signals are also not configurable.

Figure 3-23 also shows that integration and read operation times are separated from each other. Integration starts with the integration enable (*int_en*) signal. The rise of the integration enable (*int_en*) signal depends on the fall of the reset enable (*reset_en*) signal and the end of the integration is determined from the memory. Read operation starts exactly half clock cycle after the integration is done. The start of the first sampling (*SH1_en*) and the second sampling (*SH2_en*) signals are also configurable. Their pulse width is fixed and 5 clock cycle length.

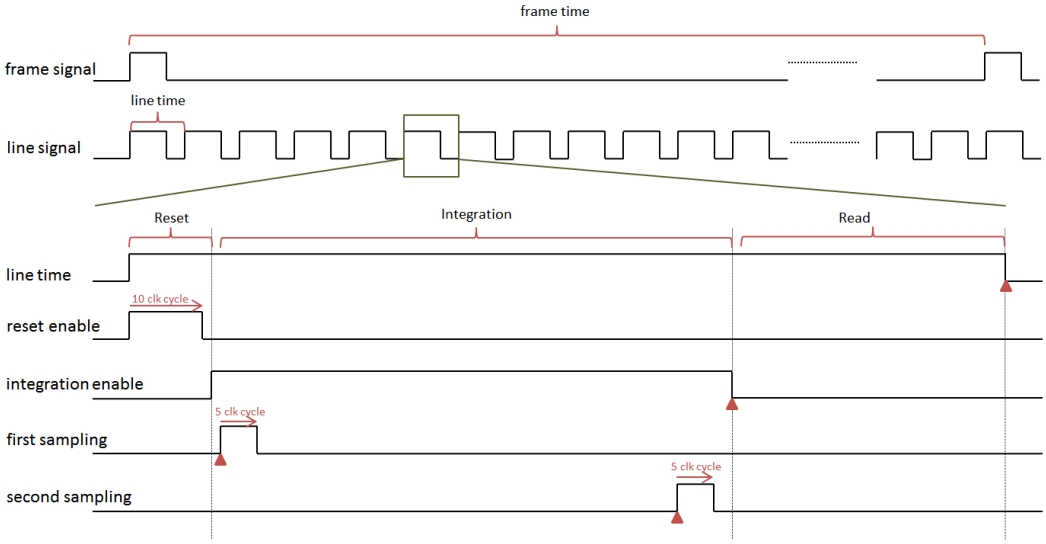


Figure 3-23: General timing scheme of the column readout signals.

There are two counters used in the digital controller. One of the counters is used for determining the line time of the readout circuit, and the other one is used for counting the rows. Line time counter is 10 bits counter, which gives the readout a max 2^{10}= 1024 clock cycle of line time length. The other counter is 7 bit counter, and its maximum value is 2^{7}=128. Since there are only 124 rows in the readout circuit, the number of bits used in the second counter is more than enough. Digital controller block also produces two outputs for the FPGA to help configure the outputs of the chip. These signals are *pix_clk* and *frame_clk*. *pix_clk* signal shows the user that the pixel output is at the output pad and *frame_clk* signal gives information of the new frame.

3.3 Top Level Integration

The interface between the digital blocks and the analog blocks are made with the buffers provided by the process. However, there should be circuits at the interface between bias generator and the readout arrays. The bias voltages of column amplifier, line driver, and pixel circuit are connected in readout basis. Therefore, the currents created in the bias generator should be converted to the voltages with a diode connected loads near the both the top and the bottom readout arrays.

The chip has 3.3 V logic interface for the easy communication with the FPGA. This feature also gives us the reduction in the space of the external electronics by eliminating the external level shifters. The designed chip has an internal bias generator and the internal output buffer. These features also reduce the size of the external electronics. These are the conclusion of the design with a system on a chip approach.

Table 3-2 shows the pad list of the 160×120 microbolometer imager. There are a total of 54 functional pads in this imager, which are spaced with 12 mil distance corresponding to 308.4 µm.

The signals produced in the digital controller can also be observed using a 12-bit digital signal test bus added in the pad frame of the chip. Using the 12-bit digital test bus allows flexible debugging as well as external driving capability in case the internally generated digital signals have functionality issues. All the analog signals produced in the bias generator are similarly connected to the pads of the imager. There are also on-chip temperature and vacuum sensors to monitor both the temperature and the vacuum level of the final packaged part. The chip requires wire-bonding of 21 pads at minimum, which are blue colored in the table, to be able to work properly. This is another conclusion of the system on a chip design approach for the microbolometer imager.

Figure 3-24 shows the layout of the 160×120 microbolometer imager, which measures 10.5×11 mm in 1 µm SOI-CMOS process. The pads also have double pad structure: one for the probe tests and the other for the packaging and normal usage.

Table 3-2: Pad list of the 160×120 microbolometer imager.

Pad Number	***Pad Name***	***Pad Number***	***Pad Name***	***Pad Number***	***Pad Name***
1	Digital Supply	19	Analog Signal	37	Analog Supply
2	Digital Supply	20	Analog Supply	38	Analog Supply
3	Digital Ground	21	Analog Supply	39	Analog Supply
4	spi_latchb	22	Analog Supply	40	Analog Supply
5	spi_data	23	Analog Supply	41	Pad_gnd
6	sdout	24	Analog Ground	42	Pad_vdd
7	RN	25	Analog Ground	43	Digital Signal_0
8	clk	26	Reference<0>	44	Digital Signal_1
9	pix_clk	27	Output<0>	45	Digital Signal_2
10	frame_clk	28	Reference<1>	46	Digital Signal_3
11	Digital signal	29	Output<1>	47	Digital Signal_4
12	Pad_vdd	30	Analog Signal	48	Digital Signal_5
13	Pad_gnd	31	Analog Supply	49	Digital Signal_6
14	Analog Supply	32	Analog Supply	50	Digital Signal_7
15	Analog Supply	33	Analog Supply	51	Digital Signal_8
16	Temp Sensor	34	Analog Ground	52	Digital Signal_9
17	Vacuum sensor	35	Analog Ground	53	Digital Signal_10
18	Analog Ground	36	Analog Supply	54	Digital Signal_11

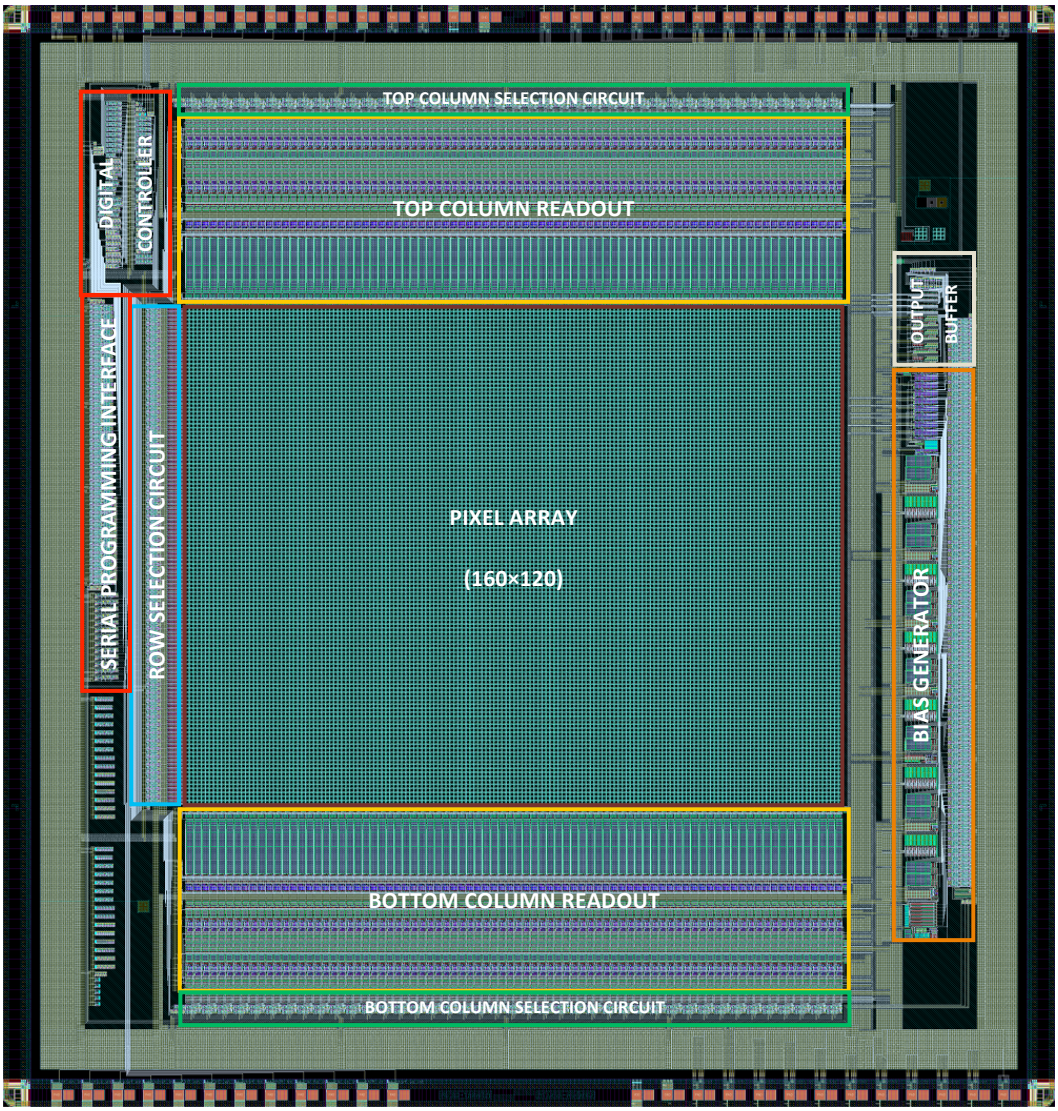


Figure 3-24: Layout of the 160×120 microbolometer imager, which measures 10.5×11.0 mm in a 1 µm SOI-CMOS process.

CHAPTER 4

TEST OF THE MICROBOLOMETER

This chapter explains the microfabrication of the microbolometer, mentions the test setup of the designed microbolometer, and shows the primary test results. Section 4.1 explains the process steps in general with the visual aids and provides a die photograph of the CMOS wafer. Section 4.2 explains the single pixel tests and gives the necessary single pixel test results. Section 4.3 shows the electrical test environments and gives functional test results and the noise results of the designed microbolometer.

4.1 Microfabrication

The post-CMOS microfabrication of the chip starts after receiving the fabricated wafers from the CMOS foundry. The fabrication approach is selected to be full wafer fabrication using a 1 µm SOI-CMOS process on a 150 mm wafer, so that the detectors can be implemented with easy post-CMOS process steps. Figure 4-1 shows the wafer photograph of the fabricated 160×120 microbolometer infrared imaging sensor after CMOS fabrication. Figure 4-2 shows the die photograph of the microbolometer imaging sensor from the CMOS wafer.

Dies are stepped on the wafer with horizontal and vertical stepping dimensions of 10880 µm and 11140 µm, respectively. The designed microbolometer sensor measures 10500 µm and 11000 µm in horizontal and vertical dimensions, which leaves 380 µm and 140 µm horizontal and vertical spacing between the dies on the fabricated wafer. The above spacing is more than enough for the proper vacuum packaging for the low-cost microbolometer production. There is also ring surrounding the microbolometer pixel array inside the chip consisting of all the metal layers for easy vacuum packaging, named as vacuum seal ring.

The fabricated wafer should be exposed to some process steps in order to have the bridge type structures on the pixels. Figure 3-6 shows the post-CMOS process steps of the multi-diode microbolometer pixels in a SOI-CMOS process [18], however in this part of the thesis the die

photographs will be shown between these process steps. Therefore, simple process steps will be defined, and the die photographs will be given accordingly. Figure 4-3 shows the process flow used to obtain suspended bridge-like structures on microbolometer pixels.

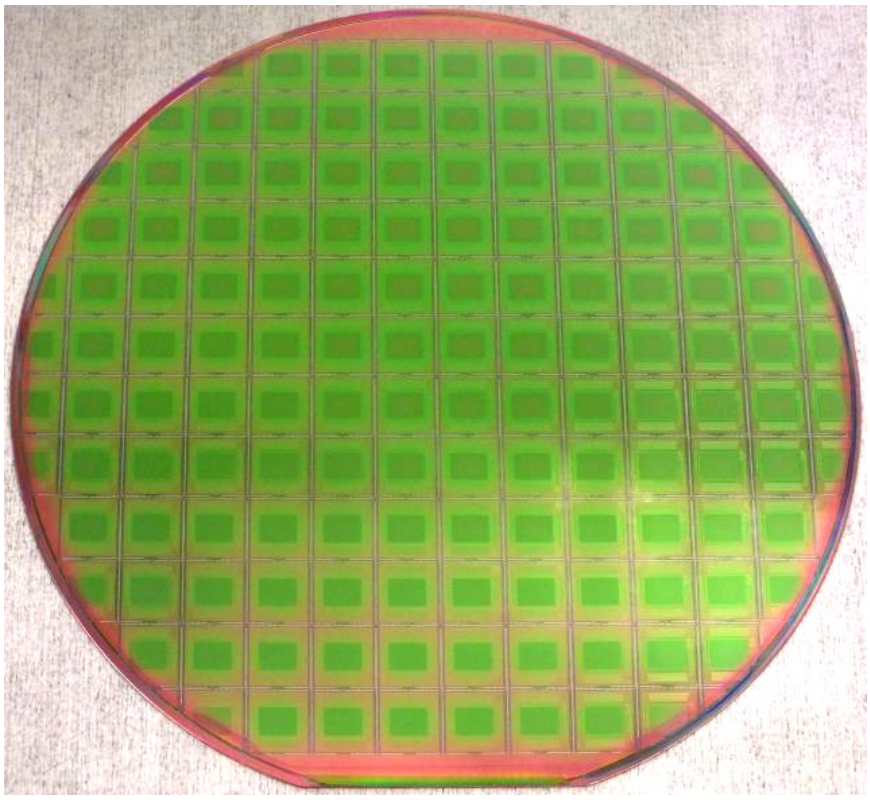


Figure 4-1: Wafer photograph of the fabricated 160×120 microbolometer infrared imaging sensor after CMOS fabrication.

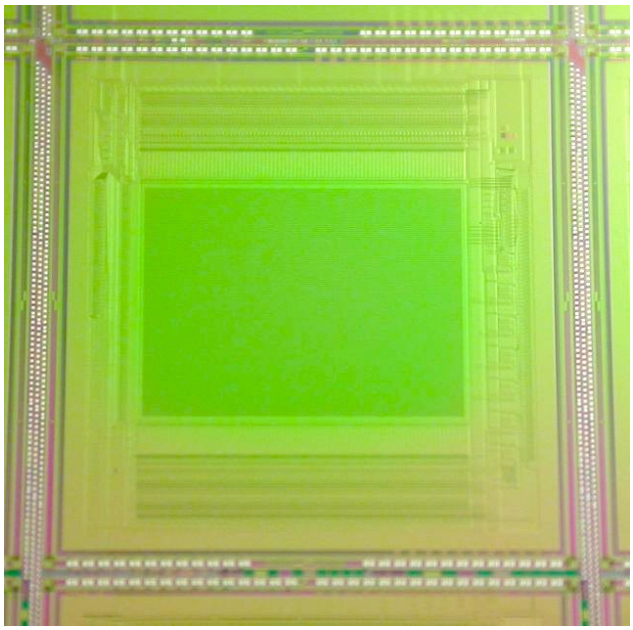


Figure 4-2: Die photograph of the microbolometer imaging sensor from the CMOS wafer.

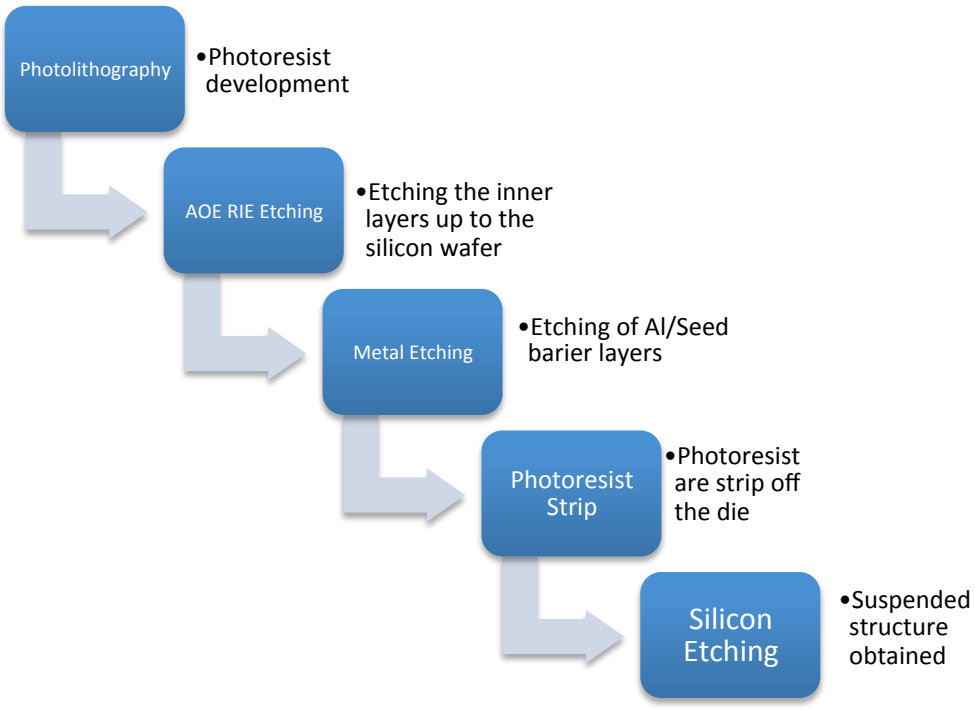


Figure 4-3: Process flow used to obtain suspended bridge-like structures on microbolometer pixels.

Microbolometer process starts with the CMOS wafer. The CMOS wafer is exposed to the photolithography step for three reasons: (1) Protecting the pads from the damages throughout the etching periods, (2) protecting the area between the vacuum ring and the pads, (3) opening the top of the focal plane array. CMOS foundry sends the dies with a passivation layer on top of each chip except the pad structures. Therefore, when the dies are exposed to any processes, the pads will be damaged. To protect the pads and the area between the pads and the vacuum ring from getting damaged during the etching processes, the dies are covered with the photoresist. Figure 4-4 shows photograph of bottom left corner of the die after photoresist development process.

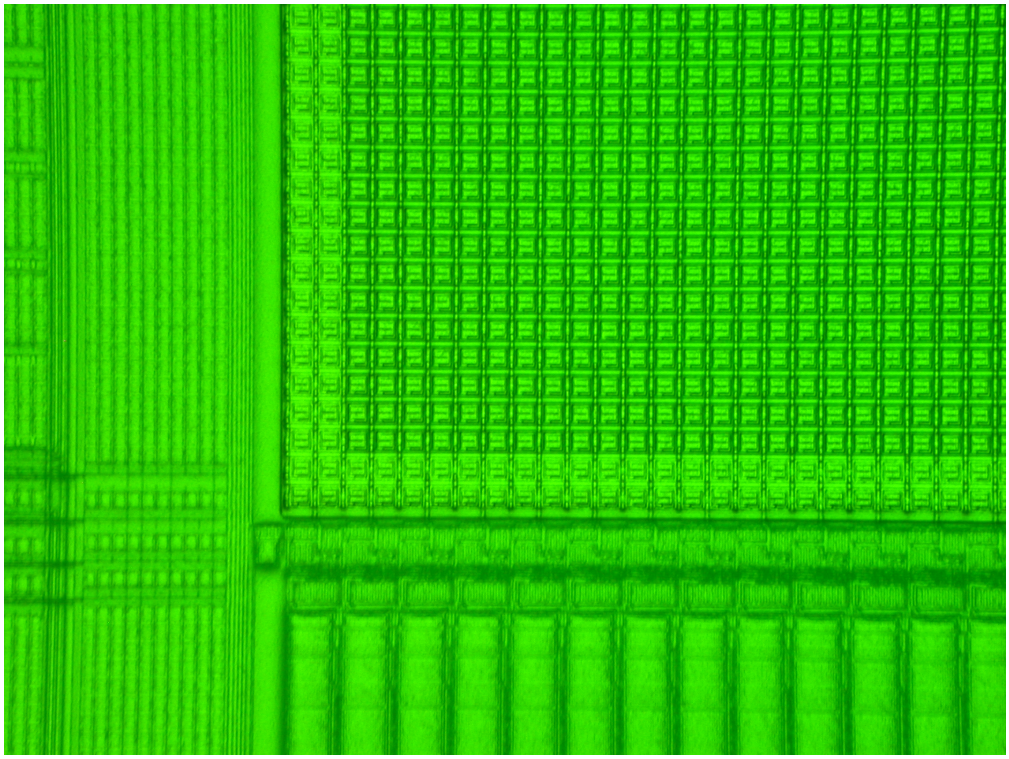


Figure 4-4: Photograph of bottom left corner of the pixel array after photoresist development process.

After photoresist is developed on top of the wafer, the wafer will go under AOE (Advanced Oxide Etching)-RIE etching. With the AOE-RIE process, the oxide layers will be etched. Around the pixel structures, the sides of the arms will be etched up to the silicon. Figure 4-5 shows SEM photograph of one microbolometer pixel in the array after the AOE-RIE etching process. There is a metal layer on top of the arms because the inner metal layer is used as a mask layer. Top side of the readout circuits are covered with the top metal because top metal layer is also used as a mask layer. Since the metal layers cause the thermal conductance of the arms to increase, the metal layers should also be stripped off. For this purpose, Al/Seed barrier etching process step is implemented. Figure 4-6 shows SEM photograph of the pixel after metal etching process. Since the masking metal layers covering on top of the pixels and the arms are eliminated, the polysilicon on the arms and the diodes on the pixels can be seen easily after the metal removal process.

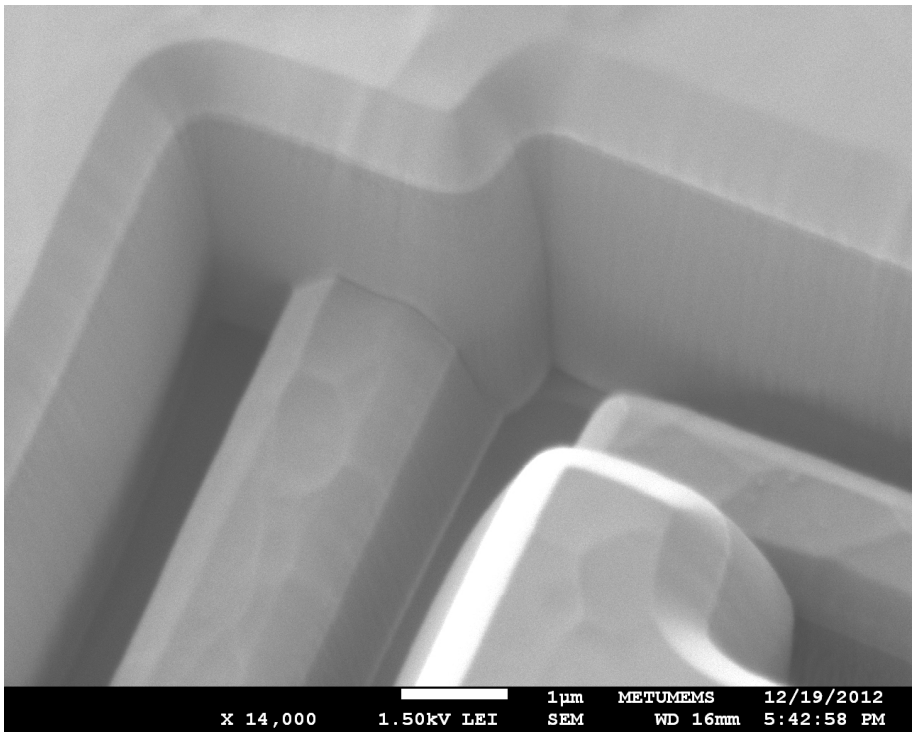


Figure 4-5: SEM photograph of one microbolometer pixel in the array after the AOE-RIE etching process.

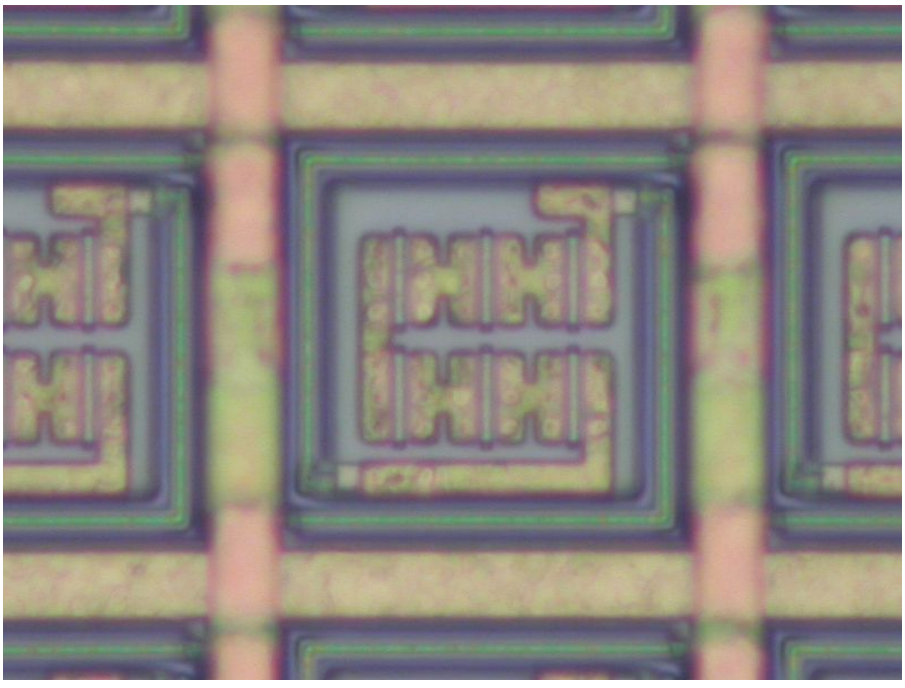
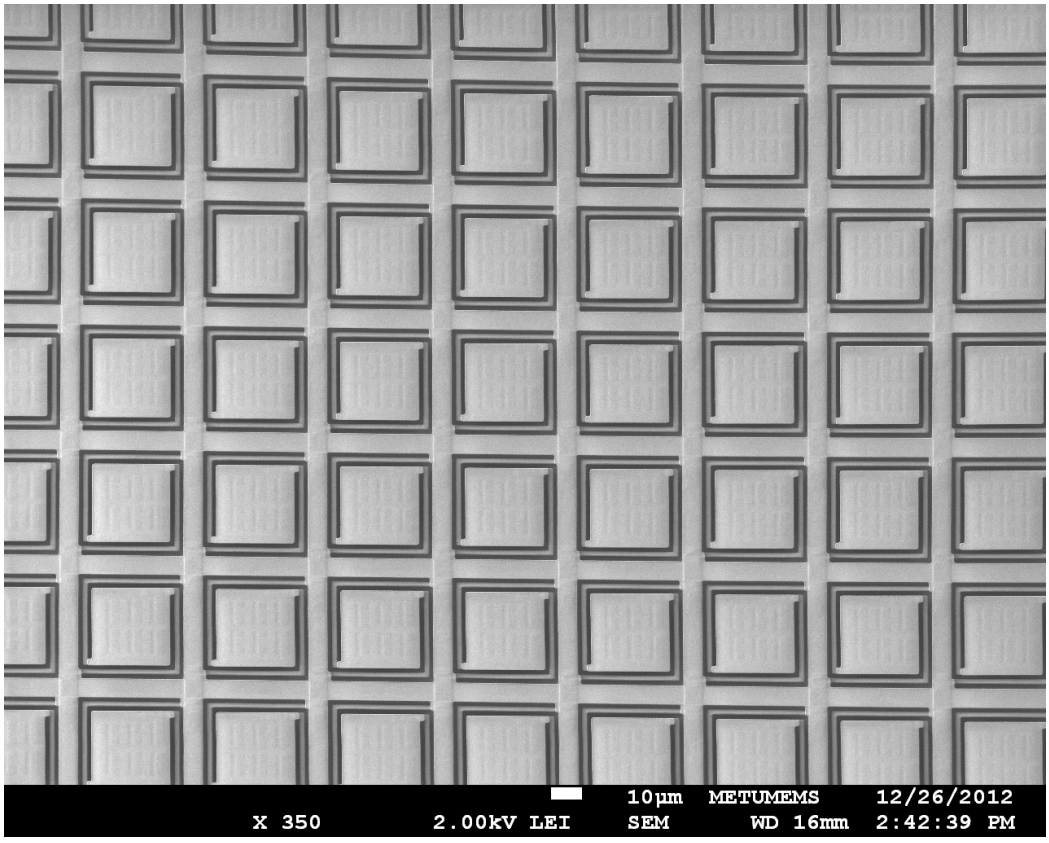


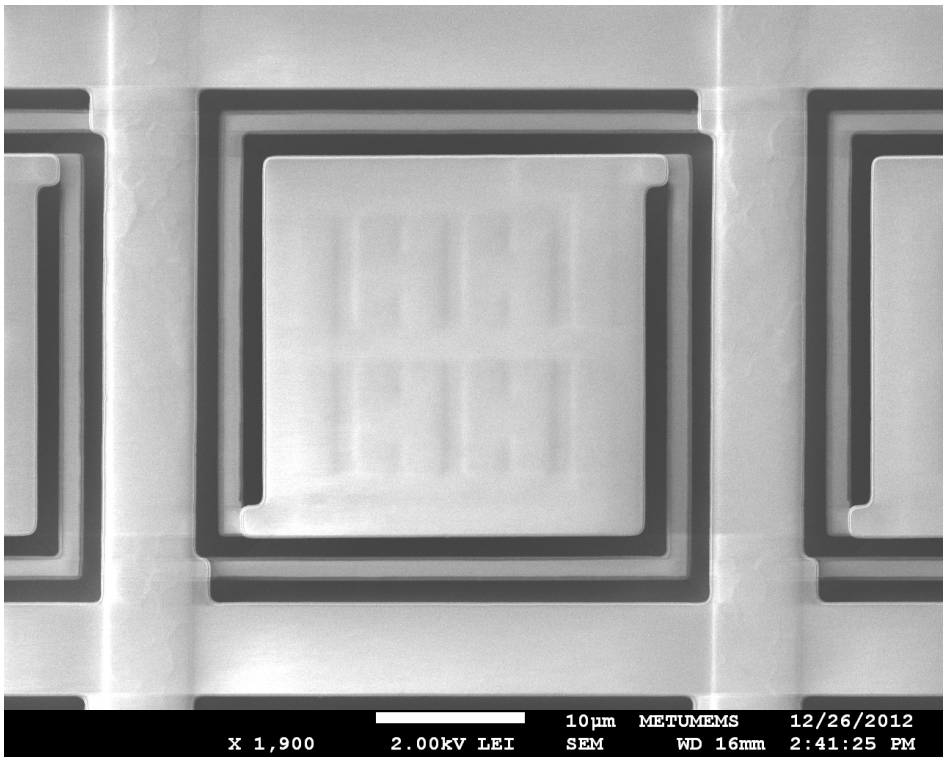
Figure 4-6: SEM photograph of the pixels after the metal etching process.

The final step for the microbolometer fabrication process is the etching of the silicon under the microbolometer pixels. Figure 4-7 shows the SEM photographs of the fabricated dies at the end of the processing steps: (a) zoomed view, (b) top view, (c) corner view of the pixels. Last part (c) of the Figure 4-7 shows that 0.5 µm feature size can be used in 1.0 µm modular SOI-CMOS process without causing any problem during the process steps.

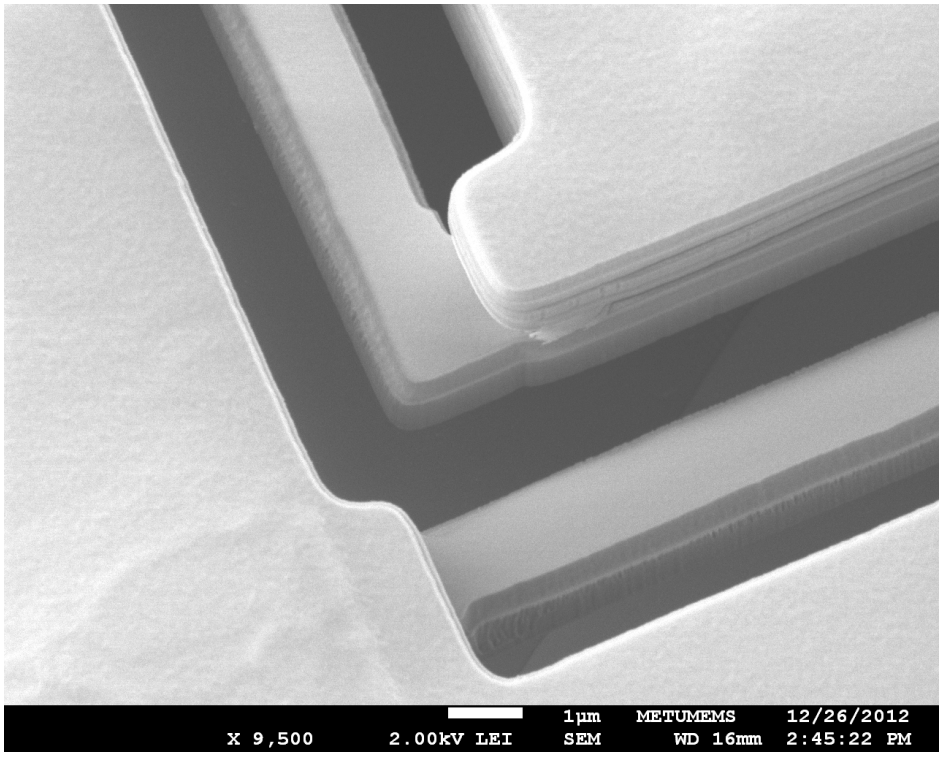


(a)

Figure 4-7: SEM photographs of the fabricated dies at the end of the processing steps: (a) zoomed view, (b) top view, (c) corner view of the pixels.



(b)



(c)

Figure 4.7: cont'd

These SEM photographs shows that 0.5 µm feature size is obtained with the 1.0 µm modular SOI-CMOS process and the microfabrication steps can also be applied for these feature size. Therefore, for the future works, 0.5 µm arm width can be chosen in order to connect the pixel outputs to both power and the output busses. The reason why smaller feature size is necessary is that the thermal conductance of the pixels drop significantly and the pixel infrared absorbing area, i.e. fill factor of the pixel increases. The thermal conductance and time constant of the pixels are measured as 205 nW/K and 25.3 ms respectively. The next section of the thesis explains how these parameters are measured and how they coincide with the expected values. As a result, 0.5 µm feature size in a 1.0 µm modular SOI-CMOS process can be used for the further studies and further products.

4.2 Single Pixel Tests

This part of the thesis focuses on the single pixel tests. For this reason, etch and vacuum indicator test pixels, which are located as 3×3 array on the top left corner of the detector array. Two ports of the middle pixels are connected to the output pads.

There are 5 different test setups implemented to measure 5 different aspects of the single pixel. First of all, I-V curve of the single pixel is measured and the diode parameters are calculated. Secondly, temperature sensitivity of the pixel is measured with the help of temperature stabilizer. After these tests, there is two more tests need to be done. These two tests should be done under vacuum and measures both the thermal conductance and the responsivity of the detector. These tests are done in clean room by using probe station.

This chapter explains the microfabrication of the microbolometer, mentions the test setup of the designed microbolometer, and shows the primary test results. Section 4.1 gives the die photograph of the CMOS wafer and explains the process steps in general with the visual aids. Section 4.2 explains the single pixel tests and gives the necessary single pixel tests. Section 4.3 shows the electrical test environments and gives functional test results and the noise results of the designed microbolometer.

4.2.1 I-V Curve

I-V measurements are performed in order to measure the detector voltage for different bias currents and determine the detector arm resistance and the diode parameters. Since the pixel under the test has 6 serially connected diodes, the measured detector voltage values are in the range of 5 V. Figure 4-8 shows the measured I-V characteristics of the diode type microbolometer pixel at room temperature. Since the measured detector is not a suspended detector and not under the vacuum, there is not much of a self heating involved. Therefore, the series connected diodes and resistor equation can be applied.

$$I_D = I_S(e^{\frac{qV_D}{nkT}} - 1) \tag{4.2.1.1}$$

where, I_D is the detector current, I_S is the reverse saturation current of the diode, V_D is the voltage on the single diode, n is the diode ideality factor, k is the Boltzmann constant, and T is the temperature in Kelvin. V_D can be found for the detector under the test as follows,

$$V_D = \frac{(V_m - I_D \times R_S)}{6} \qquad (4.2.1.2)$$

where, V_m is the measured bias voltage shown on the graph as a bias voltage, R_S is the series connect resistance due to arms of the pixel structure, and 6 comes from the 6 series connected diodes in the pixel.

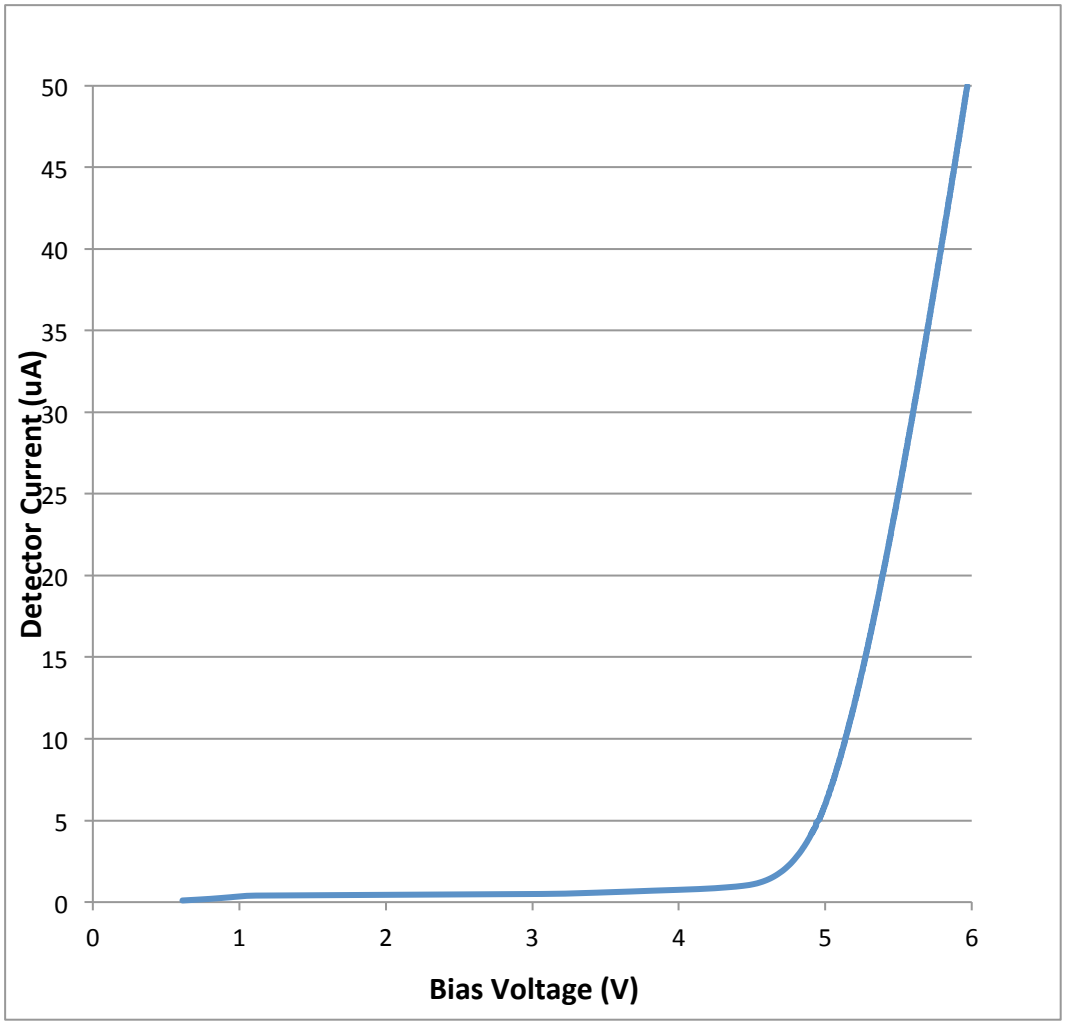


Figure 4-8: Measured I-V characteristics of the diode type microbolometer pixel at room temperature.

From these measurement results, at high current bias regions, mostly the effect of the series connect resistance occurs. The value of the connect resistance is calculated as 15 kΩ. The measured arm resistance is twice of the expected arm resistance. When the curve fitting algorithms are applied to the diode equations, the value of the n, I_S are found as 1.027 and 1.0×10^{-19} A, respectively.

4.2.2 Temperature Sensitivity

Temperature sensitivity tests are also done for the test pixels with the same setup used for I-V measurement. For measuring temperature sensitivity of the detectors, the temperature of the detector is stabilized at different temperature levels and the detector voltage is read for the same bias current levels. Figure 4-9 shows the measured variation of detector voltage with temperature at different detector bias levels. The measured pixel has 6 serially connected diodes. The temperature sensitivity is measured as -8.1 mV/K at 1 µA, which decreases in magnitude to -6 mV/K at 40 µA. Moreover, the thermal sensitivity of the pixels for 8 µA bias current is found as -7.05 mV/K.

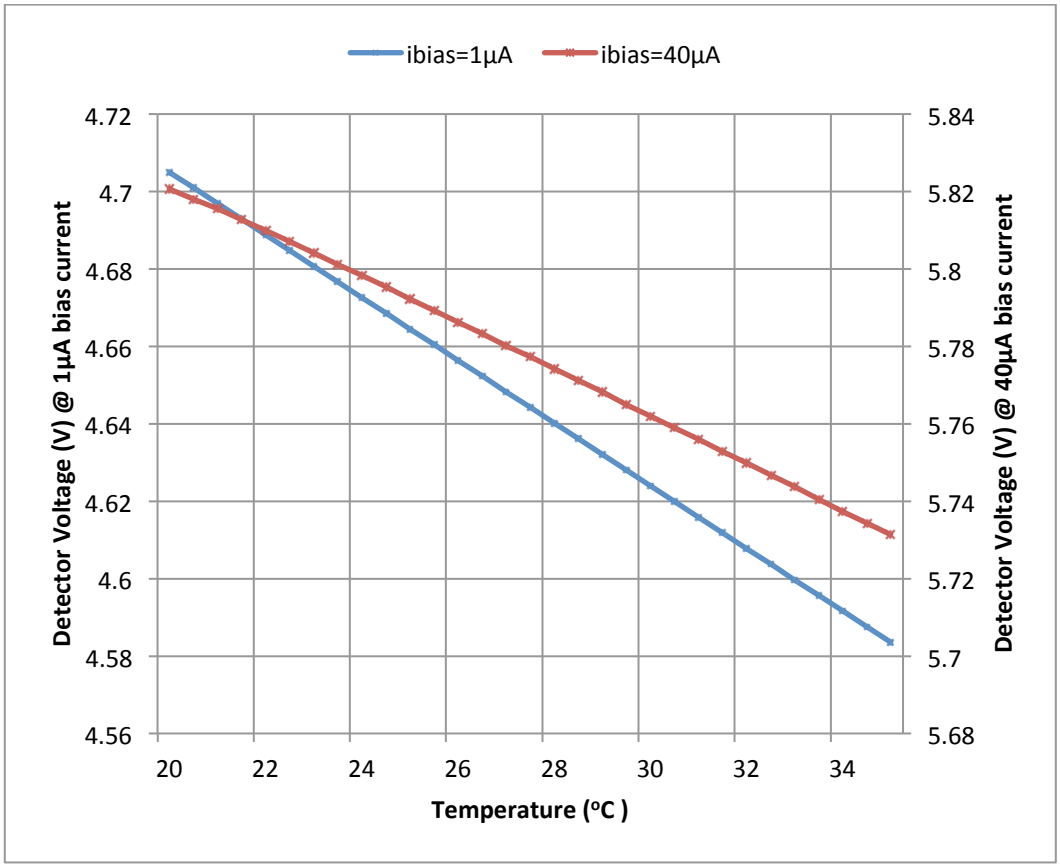


Figure 4-9: Measured variation of detector voltage with temperature at different detector bias levels. The measured pixel has 6 serially connected diodes. The temperature sensitivity is measured as -8.1 mV/K at 1 µA, which decreases in magnitude to -6 mV/K at 40 µA.

4.2.3 Thermal Conductance (G_{th})

Thermal conductance of the pixels is measured under the vacuum and with the help of probe station. Two chips are put on the empty wafer in order to measure the thermal conductance of

the pixels. The first detector is not a suspended detector and the second detector is a suspended detector. The bias current is increased from 0.1 µA to 2 µA with a step size of 0.1 µA, and the detector voltages are recorded. Figure 4-10 shows the measured I-V characteristics of the suspended and unsuspended detectors at different bias currents obtained using vacuum probe station.

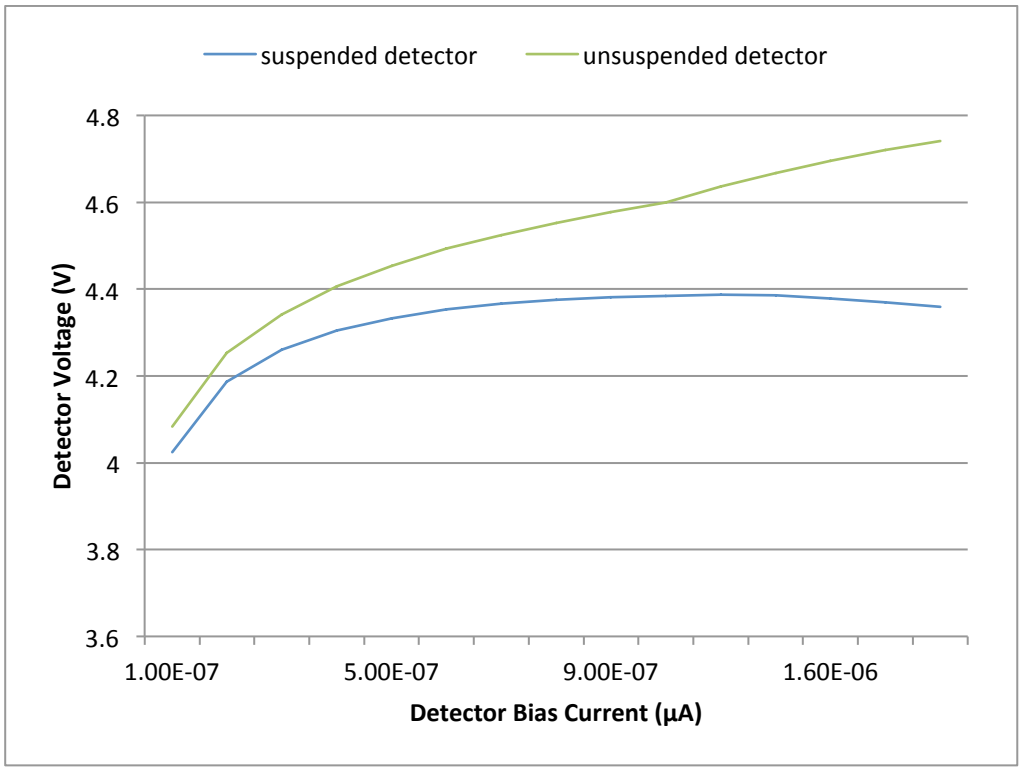


Figure 4-10: Measured I-V characteristics of the suspended and unsuspended detectors at different bias currents obtained using vacuum probe station.

Thermal conductance of the detector is calculated as follows,

$$V_1 - V_2 + (V_{2,0} - V_{1,0}) = \frac{(I_1 \times V_1 - I_2 \times V_2)}{G_{th}} \times TC \qquad (4.2.3.1)$$

where, V_1 and V_2 are the voltages of the both suspended and unsuspended detectors at vacuum condition, $V_{1,0}$ and $V_{2,0}$ are voltages of the both suspended and not suspended detectors at atmospheric pressure condition, I_1 and I_2 are bias currents, and TC is the temperature sensitivity of the detector at I_1 current. The logic behind this formula is that the heating due to different bias currents will turn into the temperature in relation with the thermal conductance of the detector. However, the bias currents should be selected small so that the detector will not burn due to too much heating. When 4 data points on the Figure 4-10 around 1 µA bias current level is selected and the temperature sensitivity is selected as -8.1 mV/K , the thermal conductance of the detector is found as 205 nW/K. The estimated thermal conductance is 250 nW/K. The difference is because of the fact that the arms are etched more than estimated.

4.2.4 Responsivity

Responsivity measurement is done under vacuum condition in probe station. Figure 4-11 shows responsivity measurement test setup, including a blackbody, a chopper, an IR filter, a probe station, an amplifier, and a dynamic signal analyzer. The amplifier should be put between the detector output and the digital signal analyzer since the output voltage levels of the detector is around 80 µV for the given blackbody power.

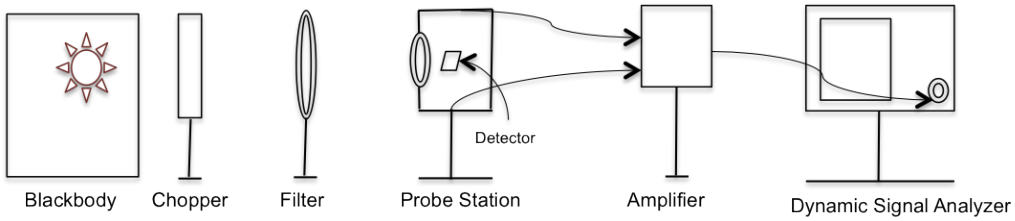


Figure 4-11: Responsivity measurement test setup, including a blackbody, a chopper, an IR filter, a probe station, an amplifier, and a dynamic signal analyzer.

In the responsivity measurement setup, the blackbody is heat up to the 1000 ^{o}C degrees, and the power level on the detector surface is known from the previous works [7]. The detector is biased with 1 µA of constant current bias in order to prevent thermal run-away. The chopper frequency is increased from 10 Hz to 100 Hz with small step size and the rms voltage level at the digital signal analyzer is recorded for all of the chopper frequencies. Figure 4-12 shows the measured output voltage of the detector with respect to chopper frequency. Red line indicates the fitted for the measured output voltages. DC responsivity and absorption coefficient of the detector is extracted as 21,920 V/W and 55.5% respectively.

The DC responsivity of the detector is estimated to be 12,960 V/W for the bias current of 8 µA, the absorption coefficient is taken as 43% and the thermal conductance is taken as 250 nW/K. However, the responsivity is measured for 8 µA bias current. Therefore, new estimation should be done to compare what is measured with the what is estimated. When the bias current is taken as 1 µA, the absorption coefficient is taken as 55.5%, and thermal conductance is taken as 205 nW/K., the resultant DC responsivity becomes 21,930 V/W, which is close to the measured responsivity from the test setup. Figure 4-13 shows measured responsivity of the diode type microbolometer detector with respect to infrared blocking chopper frequency under vacuum condition. The DC responsivity is extracted as 21,920 V/W for 1 µA bias current. The estimation for 8 µA bias current should also be made in order to compare the responsivity of the previous work with this design. When the bias current is taken as 8 µA, which is the bias currents of the previous designs that their performance parameters is given, the responsivity of the pixels are calculated as 18,190 V/W which is almost twice of the responsivity of the previous design [17], 9490 V/W. The difference is because of the higher temperature sensitivity and lower thermal conductance values obtained in this design.

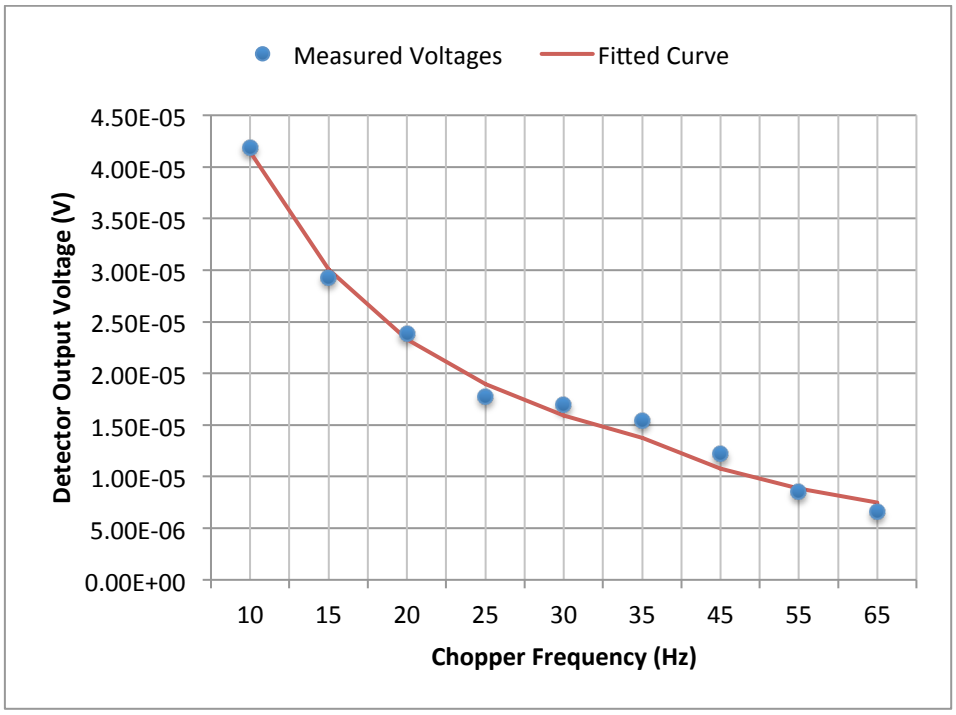


Figure 4-12: Measured output voltages of the detector with respect to chopper frequency. Red line indicates the fitted curve for the measured voltages. DC Responsivity and absorption coefficient of the detector is extracted as 21920 V/W and 55.5% respectively.

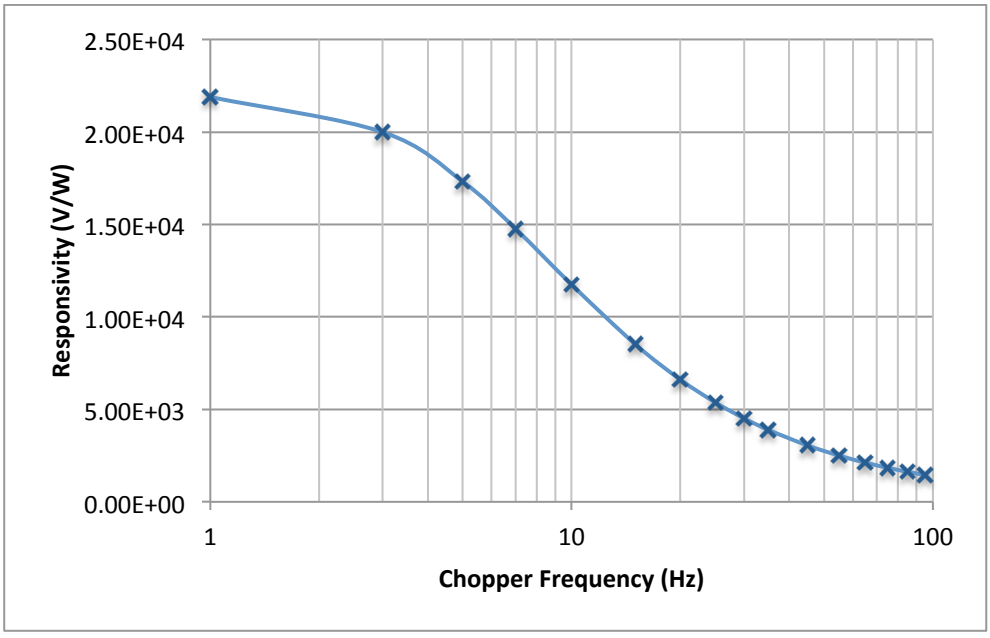


Figure 4-13: Measured responsivity of the diode type microbolometer detector under the vacuum condition. The DC responsivity is extracted 21920 V/W.

Final pixel performance test is related with the noise of the detectors. There are difficulties in measuring the exact noise performance of the pixel used in the imaging sensor due to the fact that multiple diodes increase the required detector bias voltage causing voltage compatibility issues with the custom made low-noise pre-amplifiers used in the test setup. For this purpose, the noise of a multiple parallel connected test structures with single diodes is measured using the existing pre-amplifiers. Figure 4-14 shows the measured noise of 30 parallel connected test structures with single diodes. The total bias current is adjusted to be 30 times that of the pixel bias current used in the imaging sensor. The total noise of 30 parallel connected test structures with single diodes is measured as 0.38 μV_{rms} in 4 kHz bandwidth. The noise of the actual sensor pixel is expected to be $\sqrt{180}$ times of the measured result corresponding to 5.19 μV_{rms}, where a factor of $\sqrt{30}$ comes from the noise reduction due to parallel connection and another factor of $\sqrt{6}$ comes from the noise increase due to series connection. From this data, using the measured DC responsivity value and assuming an f/1 optics, the detectivity and the NETD values of the sensor pixels are found as 5.74×10^{8} cm.$Hz^{1/2}$/W and 840 mK, respectively.

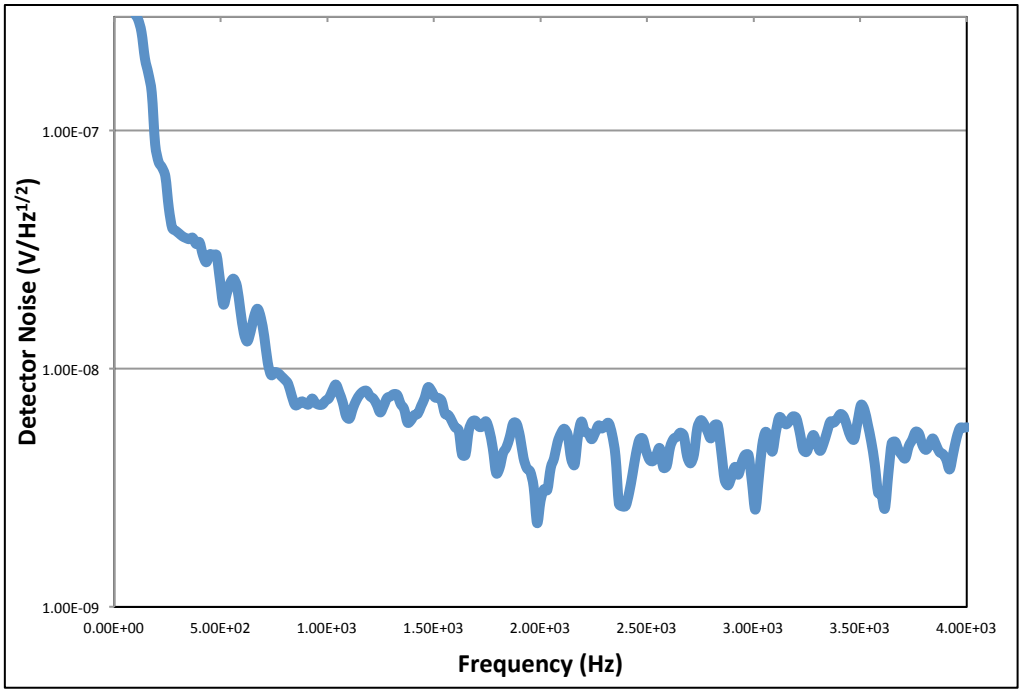


Figure 4-14: The measured noise of 30 parallel connected test structures with single diodes. The total bias current is adjusted to be 30 times that of the pixel bias current used in the imaging sensor. The total noise of 30 parallel connected test structures with single diodes is measured as 0.38 μV_{rms} in 4 kHz bandwidth. The noise of the actual sensor pixel is expected to be $\sqrt{180}$ times of the measured result corresponding to 5.19 μV_{rms}.

Table 4-1 shows the pixel performance parameters, compared with previous work [21]. The previous work reported a peak NETD value of 350 mK with an average NETD value of 820 mK, which are obtained from the histograms of the recorded images. The NETD value reported in this thesis is calculated from the noise measurement of parallel connected diodes. The NETD value of the single pixel based on the noise measurement results is extracted as 840 mK for an f/1 optics.

Table 4-1: The pixel performance parameters compared with previous work [21].

Parameters	Previous Work [21]	This Design
Pixel Pitch	70 μm	40 μm
Absorbing Area	42 μm×42 μm	25 μm×25 μm
Temperature Sensitivity	-5.49 mV/K	-7.05 mV/K
Thermal Time Constant	45.9 ms	25.3 ms
Thermal Conductance	253 nW/K	205 nW/K
Thermal Capacitance	11.60×10^{-9} J/K	5.18×10^{-9} J/K
NETD	350 mK	840 mK

Table 4-1 shows that the pixel area is reduced more than 3 times for this 40 μm pixels compared to the previous work. The reduction in the pixel area results in also a reduction in the absorbing area, which in turn causes an increase in the NETD value due to reduction of reduced infrared light collecting capability. Furthermore, the reduction in the pixel size typically results in shorter support arms and therefore increased thermal conductance, resulting in a further increase in the NETD value. From these arguments, it is clear that some improvements are required to compensate these expected performance losses. In this work, it has been shown that thermal conductance value can be reduced back to similar or lower levels as in the previous work provided that the support arms can be implemented with narrower conducting structures, which is obtained in this work using a slightly modified CMOS process allowing reducing the effective width of the arms from 1.0 μm to 0.5 μm as explained previous chapters. It is also clear that the new pixel has much smaller volume and thermal capacitance, resulting in about 2 times improvement in the thermal response time. Furthermore, the new pixel contains 6 serially connected diodes, which improves the temperature sensitivity by a factor of 1.3. It should be noted here that without these improvements implemented in this thesis, a simple size reduction of the previous work with the same number of diodes and same support arm width the NETD value would be as high as 2.2 K for f/1 optics. However, combining all of these improvements reported in this work, it became possible to keep the NETD value for this 40 μm pixels below 840 mK.

4.3 Electrical Tests

This part of the thesis focuses on the electrical tests of the microbolometer. Electrical tests of the microbolometer consist of the testing of the digital, analog and the noise performance of the microbolometer readout circuit. First section of this part mentions the test setup and the software used throughout the test period. The second part gives the results of the tests.

4.3.1 Test Setup

Test setups mainly consist of three separate parts. These parts are proximity card that the chip is bounded, FPGA card which creates the necessary signals for the chip, and reads the outputs of the chip, and the software tool to control the chip and FPGA via computer. Figure 4-15 shows the test setup and the signal flow between these three tools.

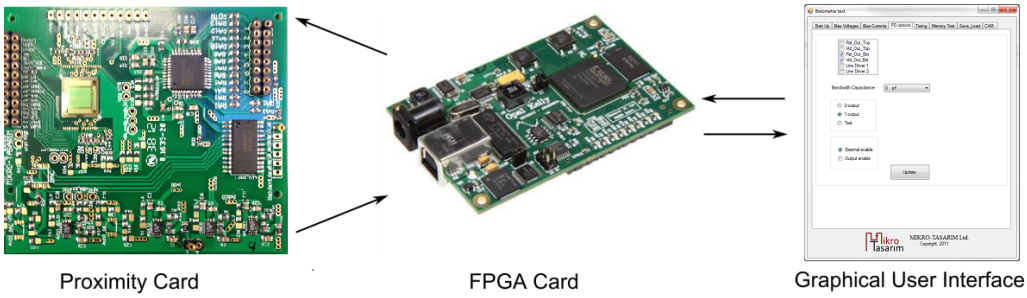


Figure 4-15: The test setup consists have a custom designed card and commercial components [29].

4.3.1.1 *Proximity Cards*

There are two proximity cards designed for the test of the microbolometer. The first one is for the primary tests and the second one is for the imaging tests, and it will be used in Dewar. The second proximity card is designed in a way that it is compatible with the previously designed camera cards for Dewar [21].

Figure 4-16 shows the proximity card designed for the primary tests of the microbolometer. This proximity card needs only one supply voltages of 7.5 V. The proximity card consists of an analog to digital converter for outputs of the chip, digital to analog converters for external biasing of the integration and reset voltages of the chip, level shifter to create an interface between FPGA and both DAC and ADC, and regulators for producing the supply and bias voltages of the chip, ADC, and DAC elements. Table 4-2 shows the components that are used in the first proximity card.

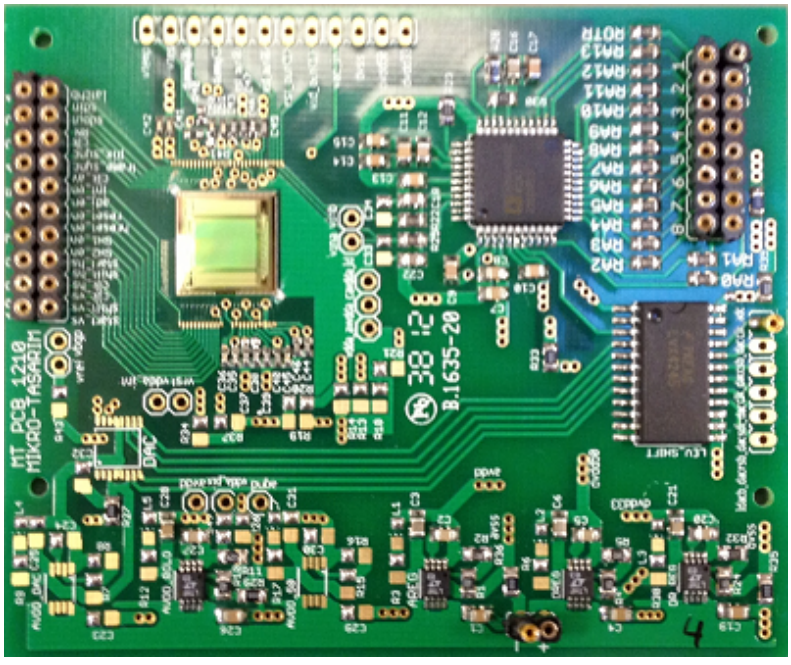


Figure 4-16: Proximity card for the primary tests of the designed microbolometer.

Table 4-2: Components used in the proximity card designed for the primary tests.

Name	Count	Description
LT1762 [30]	5	Adjustable power supply for different power domains on the card
AD9240 [31]	1	14 bit A/D Converter connected to the outputs of the chip
AD7304 [32]	1	D/A converter for external biasing of some of the voltages of the chip

Figure 4-17 shows the layout view of the second proximity card for the imaging tests. This proximity card is designed for imaging tests, and it is compatible with the previously designed camera electronic cards for the Dewar [21]. It only consists of passive elements. The bias voltages for this card are produced in the camera electronics card, which is connected to the proximity card through the pins at the circumference of the proximity card. The microbolometer chip is placed at the center of the proximity card.

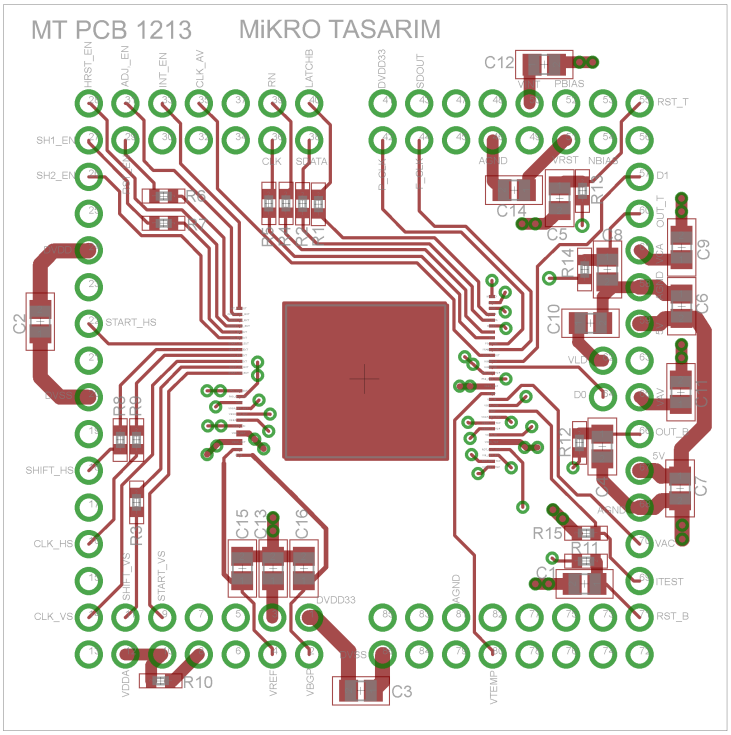


Figure 4-17: The layout view of the second proximity card, which is compatible with the previously designed Dewar electronics card [21].

4.3.1.2 *Software and Firmware*

Software and firmware tools are used to configure the microbolometer chip through the serial interface and to evaluate the outputs of the chip. Firmware is written in Verilog, and implemented on the commercial FPGA card called OPAL Kelly XEM 6010 [29]. The graphical user

interface of the microbolometer is written in Visual Basic environment with C# programming language. These two software tools were developed at Mikro-Tasarım with the help of Nusret Bayhan and Siner Gökhan Yılmaz. Figure 4-18 shows the snapshot of the graphical user interface of the developed software controlling microbolometer.

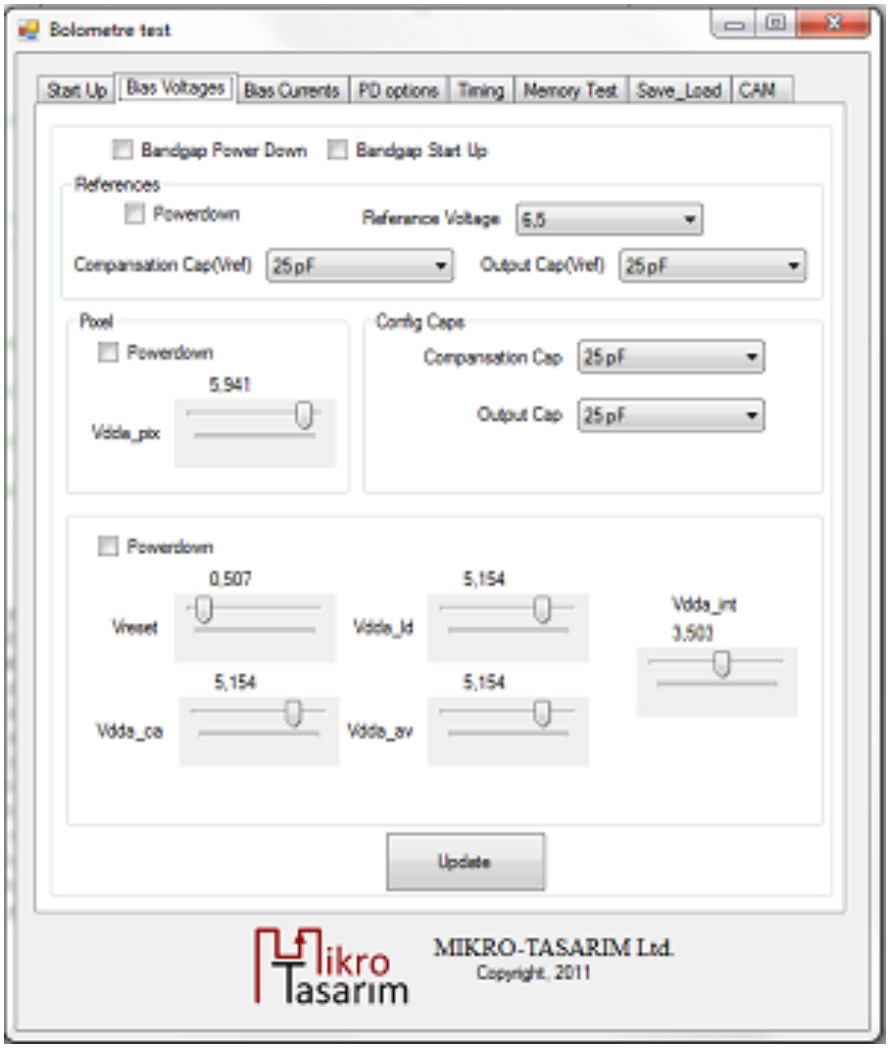


Figure 4-18: Snapshot of the graphical user interface of the developed software controlling microbolometer.

The GUI can control the bias voltages and bias current of the chip, control the power down options of the chip. It can also arrange the line time, integration time, and the sampling points of the imaging operation. Besides controlling the chip via serial interface of the chip, it can also adjust the sampling point of the analog to digital converter on the PCB, and showing the video output at the screen. Another good property of the GUI is that it can take series images of the chip, and measure the noise and the mean voltage of the specific pixel for a given number of samples.

4.3.2 Test Results

Test results of the microbolometer can be divided into three categories. These categories are test results of the digital signals, test results of the analog signals, readout chain and bias circuits, and measurement results of the noise of the sub blocks.

4.3.2.1 *Digital Test Results*

Digital test results are taken with the digital scope. The threshold of the scope voltage is arranged to 1.64 V and the snapshots are recorded to the computer via Tektronix software tools. For all the tests, only serial interface pins are connected to the FPGA, and the digital output signals are observed at the chip side.

Figure 4-19 shows the scope view of the serial programming interface signals with the serial data output signal. This test is made for observing whether the right configuration data can be written to the chip with the serial interface.

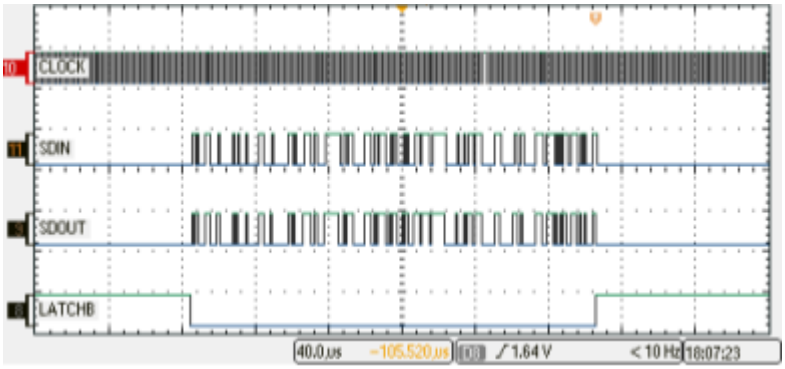


Figure 4-19: Scope view of the serial programming interface signals including serial data output signal.

Figure 4-20 shows the zoomed scope view of the serial programming interface signals. Serial data input signal changes at the negative edge of the clock signal. Chip is programmed with the same data twice to be able to see the same serial data output signal (SDOUT) with the serial data input signal (SDIN). SDOUT signal changes with the positive edge of the clock as expected, and it is same with the SDIN signal at the positive edge of the clock signal.

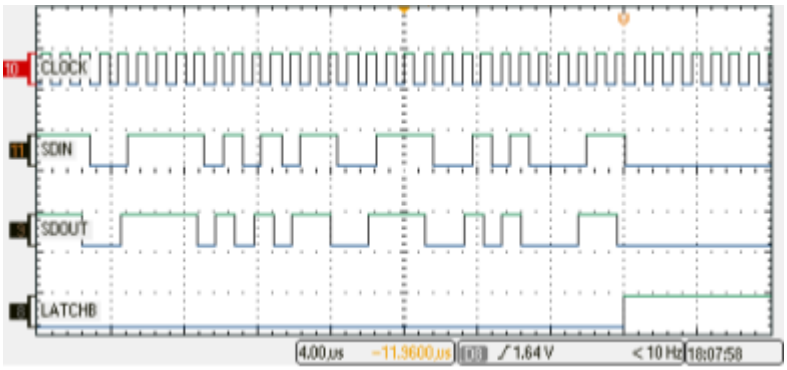


Figure 4-20: Zoomed scope view of the serial programming interface signals.

Figure 4-21 shows the scope view of the row select circuit signals: (a) full view, (b) zoomed view. Clock of the shift register of the row select circuit comes at the middle of the both data of the shift register (START_VS) and shift enable of the shift register (SHIFT_VS). START_VS signal comes only at the start of an each frame.

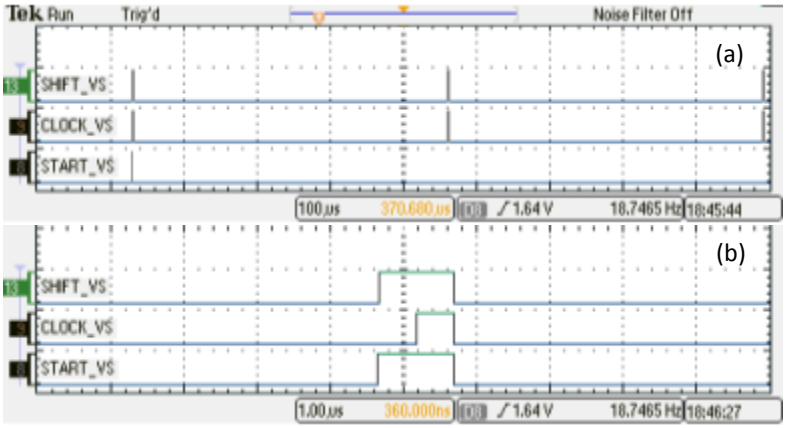


Figure 4-21: Scope view of the row select circuit signals: (a) full view, (b) zoomed view.

Figure 4-22 shows the scope view of the column select circuit signals: (a) full view, (b) zoomed view. Clock of the shift register (CLK_HS) of the column select circuit comes after the data of the shift register (START_HS) and shift enable of the shift register (SHIFT_HS) comes. Zoomed view of the Figure 4-22 shows that START_HS is high for one clock cycle and then goes low. This operation is needed for selecting only one column at a time. However, there has been a mistake in the design that the START_HS pulse occurs only one time after the reset operation of the chip, and does not occur again. This results in no column selection operation after the first line. This phenomenon is shown in the Figure 4-22 with purple circle and named as “Missing pulse”. This mistake has been corrected in the revised version of the chip.

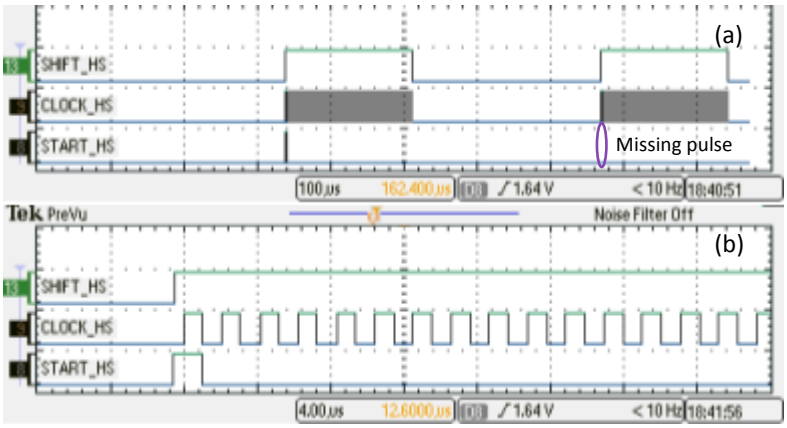


Figure 4-22: Scope view of the column select circuit: (a) full view, (b) zoomed view.

Figure 4-23 shows the scope view of the column readout signals. The signals come in a sequence. First HARD_RESET_EN (resets the integration capacitances to the ground) pulse occurs, and then RESET_EN (sets the integration voltage to 0.7 V) pulse comes. After resetting and setting process, INT_ENABLE (starts the integration of the pixel voltage to the integration capacitance) pulse comes, and the integration starts. Sampling signals, SH1_EN (samples the reset voltage) and SH2_EN (samples the integration voltage), comes and the sampling of the integration voltage to the analog memory is done. With SHIFT_HS pulse, the column selection circuit sends the output of the analog memory of each column to the output multiplexer successively.

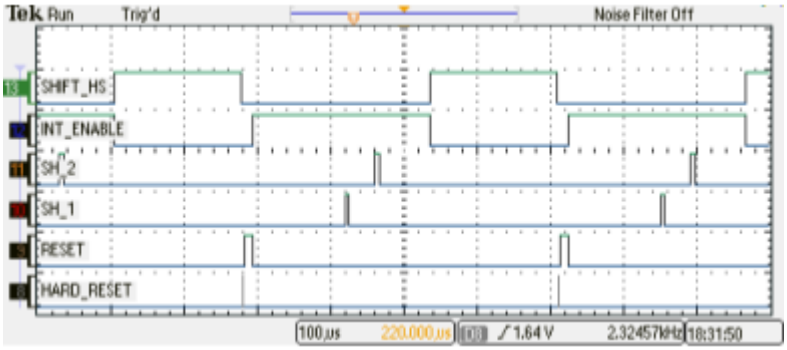


Figure 4-23: Scope view of the column readout signals.

Figure 4-24 shows the scope view of the column readout signals at different sampling points: (a) Sampling points at first location, (b) Sampling points at second location. The start of the SH_1 and SH_2 pulses is changed in the 2nd sampling points. These arrangements are made throughout the serial interface of the chip. Besides start of SH_1 and SH_2 pulses, duration of the integration time and the line times are also configurable through the serial interface of the chip.

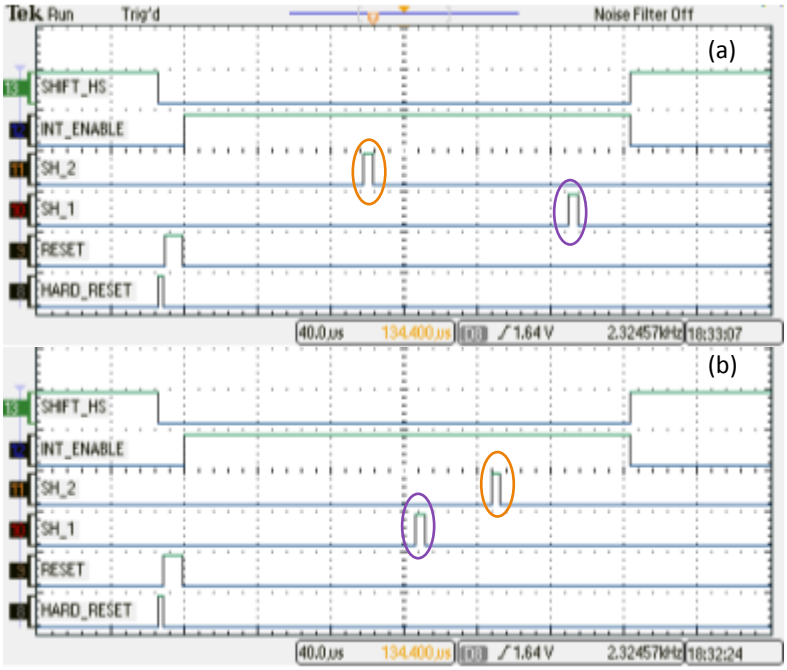


Figure 4-24: Scope view of the column readout signals at different sampling points: (a) Sampling points at first location, (b) Sampling points at second location.

4.3.2.2 *Analog Test Results*

Analog test results consists of three test results, namely power consumption tests for two different operating speeds and output buffer test results.

Power consumption tests are made in order to differentiate the current needs of the sub blocks of the microbolometer. Power consumption tests are made in two different working conditions. The first condition is normal operating condition, and the second condition is the slow operation condition. For slow operation condition, the clock frequency is changed to ¼ of the original frequency and the slew currents of the readout blocks are decreased accordingly.

Table 4-3 shows the current demand of the supplies for both normal operation and slow operation mode. Table 4-4 shows the current demand of the sub-blocks of the microbolometer for both normal operation and slow operation modes.

Table 4-3: Current Demand of the digital and analog power supplies for both normal operation and slow operation modes.

Power	Current Demand (I)	
	Nominal	Slow
5 V Digital Power	<= 1 mA	<= 1 mA
3.3 V Digital Power	<= 1 mA	<= 1 mA
7 V Analog Power	9 mA	7 mA

Table 4-4: Current Demand of the sub-blocks of the microbolometer for both normal operation and slow operation speeds.

Supplied Blocks	Current Demand (I)	
	Nominal	Slow
Integrator Buffer	<= 2 mA	<= 1 mA
Column Buffer	<= 2 mA	<= 1 mA
Output Buffer	1 mA	1 mA
Pixel Array	<= 2 mA	<= 2 mA
Bias Generator	2 mA	2 mA

The 160×120 microbolometer imager has only one test feature. This feature is about the output multiplexer block. The reset voltage produced in the bias generator block is fed to the output multiplexer in this test feature. Figure 4-25 shows the scope view of the output buffer test results: (a) Sweep of the input voltage, (b) Square wave input voltage. There have been two different tests made by using the internal test feature. These are sweep test and square wave input test. In sweep test, the test voltage is swept from 0 V to 5 V, and both test voltage and output voltage of the output buffer is recorded with the oscilloscope. In square wave test, the test voltage is changed between 1 V and 3 V as a square wave, which is the voltage range of the video driver operational amplifiers, and the output and the test voltages are observed.

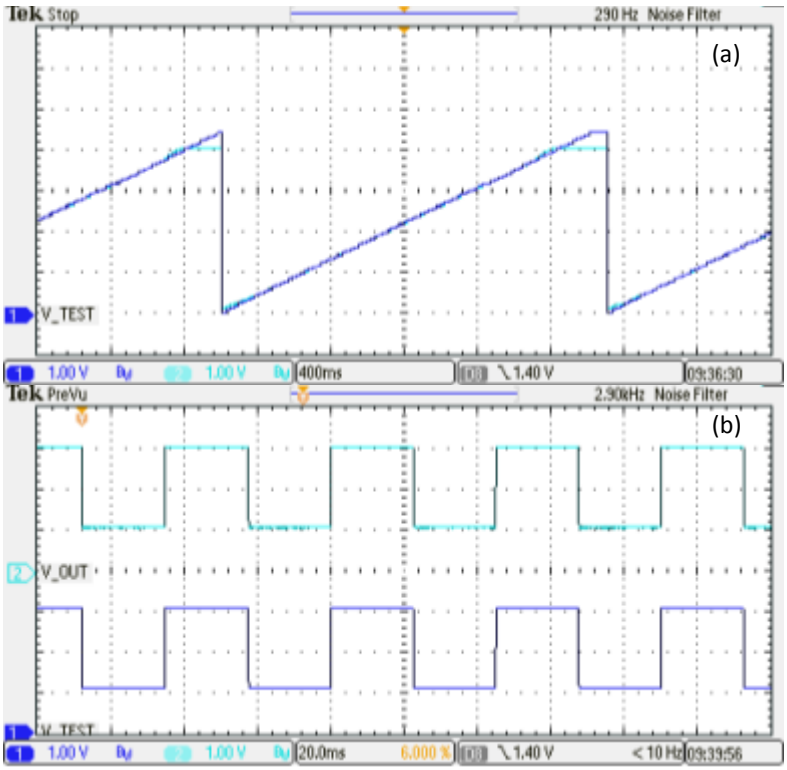


Figure 4-25: Scope view of the output buffer test results: (a) Sweep of the input voltage, (b) Square wave input voltage.

4.3.2.3 *Noise Test Measurements*

This section of the thesis gives the noise contributions of the sub blocks of the microbolometer. The pixel noise and the uniformity of the pixel array could not be retrieved because of the fact that there has been a mistake on the interface between column selection circuit, the pixel circuitry, and the column readout. This mistake has been corrected in the later version of the chip.

The noise tests are done by giving the column readout signals externally with the FPGA due to error made in the column selection circuit. The noise setup consists of a 14 bits ADC [31], FPGA, and MATLAB. ADC is arranged in 3 V swing. Therefore, one LSB of the ADC corresponds to 183 μV.

There are four different noise tests has been made so as to find the noise contributions of the sub blocks. Table 4-5 gives four different noise test setups and the targeted blocks for noise measurements.

Table 4-5: Four different noise test setups and the targeted blocks for noise measurements.

	Blocks Under Test	Comments
Test 1	ADC	This test measures the noise of the ADC and the setup.
Test 2	Output Buffer Bias Generator ADC	The reset voltage produced in the bias generator is connected to the both reference and video output buffers.
Test 3	Integrator Column Buffer Output Buffer ADC	The reset voltage is fed to the integration capacitances and the video and the reference voltages are sampled for different times at the analog memory for the same column. Column selection circuit connects the same column.
Test 4	Integrator Column Buffer Output Buffer ADC	The reset voltage is fed to the integration capacitances and the video and the reference voltages are sampled for different times at the analog memory for the same column. Column selection circuit is also active.

The first test gives us the noise of the setup and the ADC component. For this purpose, the output buffers in the pixel circuit are shut down, and the several data taken with the ADC. The noise contribution of the ADC and the setup is obtained to be 0.6390 count, which corresponds to 117 μV_{rms} .

Figure 4-26 shows the histogram of the standard deviation each pixel when the output buffers are in test mode, and the mean of the standard deviation is found as 0.8789 counts, which corresponds to 161 μV_{rms}. This test is made for measuring the noise contribution of the output buffer together with the reset voltage generated in the bias generator of the chip. For this measurement, output buffers are arranged to drive the reset voltage out of the chip. Consecutive frames are taken, and the standard deviation of each pixel is calculated. The mean of the standard deviation of each pixel in frames are found as 0.8789 ADC counts, which corresponds to 161 μVrms total output, integrated noise. When the noise contributions of the setup and the ADC are subtracted, the noise contribution of the output buffer with the reset voltage generated in the bias generator of the chip is found as 111 μV_{rms} .

The third test is done to measure the noise contribution of the column readout when the column selection circuit is stopped at some point. This means that same column is read over and over again. Figure 4-27 shows the histogram of standard deviations of each pixel when the reset voltage is driven to the column readout and the column selection circuit connects the same

column for all the lines and frames, and the mean of the standard deviation is found as 0.9248 counts which corresponds to 170 μV_{rms} total integrated output noise. When the setup and ADC noise is subtracted, the noise contribution of the column readout together with the output buffer when there is no integration from the pixels is obtained as 124 μV_{rms} .

In the final test, the noise contribution of the column selection circuit is also added to the measurements. Figure 4-28 shows the histogram of standard deviations of each pixel when there is no contribution from the pixel and the gm stage circuits. When the standard deviation of each pixel is observed, some columns are seen to be defected, and they are not added into the histogram, and the calculations are done after subtracting those defected columns. The mean of the standard deviations of each pixel in frames are obtained as 0.9920 ADC counts, which correspond to 182 μVrms, total integrated output noise. When the setup and the ADC noise contributions are subtracted, the noise contribution of the column readout together with the output buffer when the column selection circuit is active is calculated as 140 μV_{rms} .

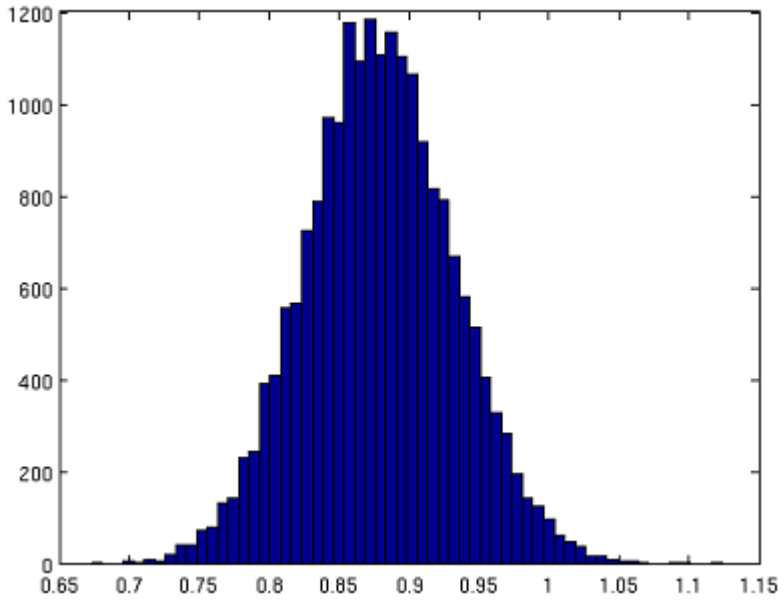


Figure 4-26: Histogram of standard deviation of each pixel when the output buffers are in test mode, and the mean of the standard deviation is found as 0.8789 counts which corresponds to 161 μV_{rms} total integrated output noise.

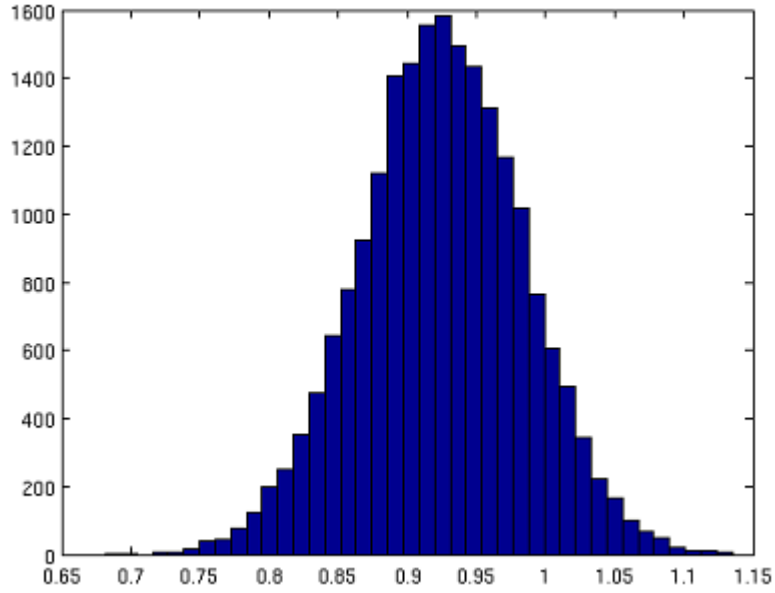


Figure 4-27: Histogram of standard deviation of each pixel when the reset voltage is driven to the column readout and the column selection circuit connects the same column for all the lines in the frames, and the mean of the standard deviation is found as 0.9248 counts which corresponds to 170 μV_{rms} total integrated output noise.

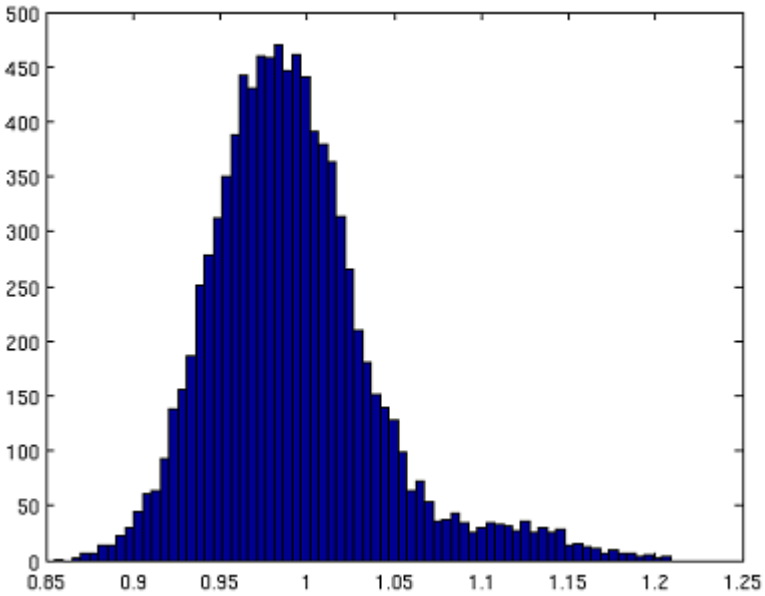


Figure 4-28: Histogram of standard deviations of each pixels when the pixel is off and all the other readout elements are working, the mean of the standard deviation is 0.9920 counts which correspond to 182 μV_{rms} total integrated output noise.

CHAPTER 5

SUMMARY AND CONCLUSIONS

The research conducted in this thesis focuses on the design of a low-cost and low-power uncooled diode type microbolometer infrared imaging sensor. The main target of this research is to develop low-cost microbolometer infrared imaging sensor to be used in newly emerging potentially high volume commercial infrared imaging applications, such as automotive, security, and building automation. To reach this target in terms of cost, functionality, and performance, several improvements have been integrated in this design compared to previous work [21]. To achieve these improvements, the new sensor chip developed in this work has been designed from beginning with a system-on-chip architecture in mind with major design improvements, especially implemented to achieve a smaller pixel size, reduced chip dimension, improved signal quality, and enhanced functional programmability. The improvements implemented in this design are listed, summarized, and then compared with the previous work [21] as below:

1. The pixel pitch of the diode microbolometer is reduced from 70 µm [21] to 40 µm.
2. The chip size is fabricated in a 1.0 µm SOI-CMOS process same as previous work [21], and the chip size is reduced from 14.8 mm×14.5 mm [21] to 10.5 mm×11.0 mm. Therefore, the number of chip per wafer is increased from 52 [21] to 112.
3. To compensate any possible loss due to dramatic reduction in the pixel size, the number of serially connected diodes is increased in this design from 4 [21] to 6 allowing to increase the pixel temperature sensitivity from -5.49 mV/K [21] to 7.05 mV/K.
4. To improve the pixel performance further, the thermal conductance value of the pixel is reduced by using 0.5 µm interconnect widths as compared to 1.0 µm in the previous work [21]. In this way, a better thermal conductance value is achieved even at reduced pixel size of 40 µm. This improvement is made possible by introducing a slight process modification to the 1.0 µm SOI-CMOS process, where a higher resolution photolithography process is used only in the pixel array to allow fabrication of 0.5 µm features with.
5. The imaging sensor architecture is improved by adding readout capability of pixel reset level along with the regular analog pixel voltage level. This allows a so-called pseudo-differential operation, which helps considerably in eliminating the system noise.
6. The readout circuit is implemented in two parts at the top and the bottom of the chip, so that corresponding column readouts can be layed out efficiently and the pixel array is centered nearly in the center of the chip.

7. By placing the pixel array in the center of the chip, it was also possible to integrate dedicated area around the pixel array to be used as a bonding surface required by various wafer level vacuum packaging techniques.
8. The wire bonding pads of the sensor has been implemented using double pad structures to allow dedicated bonding areas to be used during probe station tests and wire bonding. These bonding pads are placed only at the top and bottom of the chip, which simplifies wafer level packaging as well as die singulation afterwards.
9. There are on-chip programmable timing and biasing circuits allowing flexible operation and simplified system integration. For example, pixel integration time and the readout biasing levels can easily be programmed via a simple digital interface, which helps optimization of power dissipation and overall performance of the sensor for a given frame rate.
10. Analog outputs of the sensor are driven by on-chip buffer circuits capable of driving large external capacitive loads. The previous design [21] did not have these buffers, therefore an external additional buffers had to be used between the sensor and ADC circuits. However, this sensor can directly drive external ADCs with reduced overall power dissipation and reduced overall system noise without any external blocks and interconnects in between.
11. The chip has integrated regulators that run 7 V, and generate required regulated voltages for on-chip critical blocks, such as pixel array and analog column readout circuit. Unlike the previous work, the use of an internal voltage regulators especially for the pixel array eliminates any external noise coupling at the critical sensor bias voltages.
12. The chip uses 3.3 V CMOS logic levels for the digital input and output pads. This simplifies interfacing of this sensor with modern digital external circuit components, such as microcontrollers and FPGAs. By having 3.3 V CMOS logic interface, the need for the external level shifters is eliminated, and the overall system size can be reduced with much lower overall switching noise.
13. There are on-chip integrated temperature and vacuum sensors allowing continuous monitoring temperature and vacuum level of the packaged parts. Use of such integrated sensors allows building compact and smart sensor solutions without the need for any external sensor components.

The sensor developed in this thesis has been electrically tested in grate detail to verify its functionality and to determine its performance parameters. Test results showed that there are two areas in the design that needs to be revised. First, it has been found that there is a minor logic design error in one of the sub blocks of the digital controller that causes timing related problems in driving the sensor in its default mode. However, the sensor can still be operated in its so-called test mode by applying control signals externally. Test results reported in this thesis are obtained by running this chip in the test mode. Second, the use of 6 diodes in the pixel requires high voltage levels both to bias the pixel array as well as to provide the required control signals for the analog switches used in the row and column select circuits of the pixel array, which are operated at 5 V in the current design. However, the performed test indicates that this voltage level should at least be increased to 6 V to guarantee proper switching of the columns and rows. It is also possible to apply higher supply voltages for the current design to solve this problem temporarily for short tests, however it is not suitable as higher voltages above nominal levels decrease the overall reliability of the part. Therefore, the current design requires a minor design revision to fix the abovementioned two errors. The initial analysis shows that the first problem can easily be solved by modifying some local interconnections in the digital controller block, which can be done using simple metal mask changes. The second problem can be solved by two methods. The first method requires the use of high voltage transistors instead of regular 5 V transistors in the row and column select circuits. However, it is not a preferred solution since it increases the required supply voltages as well as it requires a major design change affecting the fabrication technology from the beginning. The second is to decrease the number

of diodes in the pixel from 6 to 5, and it can be implemented using a simple metal mask change, making it the preferred solution for the first design revision.

Based on the results obtained in this thesis, it has been concluded that there are several areas requiring further research and study as summarized below;

1. The current design should be revised and re-manufactured with minor metal mask changes. After that, the revised design should be tested to verify its functionality and to determine its performance parameters.
2. The new parts should be post processed to achieve thermal isolation. Furthermore, they need to be vacuum packaged for infrared imaging tests.
3. Vacuum packaging can be done individually or at wafer level. The latter approach is preferred due to its cost advantages. Therefore, a wafer level vacuum packaging solution should be developed for these new parts. Considering this need, there is already an integrated vacuum seal ring in the current version of the manufactured sensor chips. Since vacuum packaging and circuit functionality are independent from each other from the technology development point of view, it should be possible to start wafer level vacuum packaging related works even using current version sensor chips developed in this thesis.
4. There is a need for a compact infrared imaging test camera to demonstrate the imaging capability of the newly developed compact infrared imaging sensors. Considering the fact that the focus of this thesis is on the development of the low-cost infrared sensors, this required compact infrared camera should be developed along with its imaging software to satisfy overall cost, size, and functionality requirements of the newly emerging potentially high volume commercial infrared imaging applications.

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