INNOVATIVE APPROACHES IN DOHERTY AMPLIFIER DESIGN FOR HIGHER EFFICIENCY AND WIDER FREQUENCY BANDWIDTH

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ABSTRACT

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In the first phase of this thesis, the design optimizations of the bias adapted Doherty power (BA-DPA) and asymmetric Doherty power amplifier (ADPA) are presented for maximum efficiency criteria in the high power region. BA-DPA is analyzed by a novel approach in terms of efficiency. The ideal efficiency characteristics of BA-DPA with different bias adaptation schemes are illustrated. The maximum conduction angle and periphery requirement of the class-C biased peaking power amplifier (PPA) to realize fully load modulated ADPA are investigated. The appropriate maximum conduction angles and relative peripheries for the PPA are evaluated for different load modulation regions. The advantages and drawbacks of the BA-DPA and ADPA based on the simulated and measured performances of the designed amplifiers are concluded. In the second phase of this thesis, it is focused on the hot research topic of widening the operational bandwidth of the DPA. A novel combiner that solves the fundamental bandwidth limitation problems of the conventional Doherty structure is proposed. A new Doherty amplifier structure with an octave operational bandwidth based on the proposed combiner is presented. The implemented DPA has approximately one and half times higher bandwidth with respect to the similar studies in the literature.

Keywords: Doherty Power Amplifier, Efficiency, Linearity, Wideband, Combiner

ÖZ

VERİM ARTTIRIMI VE FREKANS BANDI GENİŞLETİMİ İÇİN DOHERTY YÜKSELTECİ TASARIMINDA YENİLİKÇİ YAKLAŞIMLAR

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Bu çalışmanın ilk aşamasında, besleme uyumlu Doherty güç yükselteci (BU-DGY) ve asimetrik Doherty güç yükselteci (ADGY)'nin yüksek güç seviyelerindeki verimlilik değeri göz önüne alınarak, tasarım iyileştirilmesi üzerine çalışılmıştır. Özgün yöntemler kullanılarak BU-DGY'nin verimlilik analizi yapılmıştır. Değişik besleme formları ile ulaşılabilecek verim karakteristikleri incelenmiştir. Tam yük performansına sahip bir ADGY'de kullanılabilecek tepeleyici güç yükselteci (TGY)'nin sahip olması gereken tranzistör büyüklüğü ve tepe iletim açısı irdelenmiştir. TGY'nin sahip olması gereken transistor büyüklüğü ve tepe geçirim açısı değişik yük modülasyon aralıkları için hesaplanmıştır. Gerçekleştirilen benzetim ve deneysel ölçüm sonuçlarına dayanılarak, BU-DGY ve ADGY yapılarının göreceli olarak sahip olduğu avantaj ve dezavantajlar ortaya konulmuştur. Çalışmanın ikinci aşamasında ise, gündemde olan çalışma bant genişliğinin arttırılması üzerine çalışmalar yürütülmüştür. Geleneksel DGY'nin temel bant genişliği problemini çözen özgün bir birleştirici yapısı önerilmiştir. Bu birleştirici yapısı temel alınarak yeni bir DGY yapısı geliştirilmiştir. Tasarlanan DGY yapısı üzerinde yapılan deneysel testler, önerilen DGY yapısının literatürde var olan geleneksel DGY yapılarına oranla yaklaşık bir buçuk kat daha geniş çalışma bandına sahip olduğunu ortaya koymuştur.

Anahtar Kelimeler: Doherty Güç Yükselteci, Verimlilik, Doğrusallık, Geniş Bant, Birleştirici

To my unique wife Havva and our angel Tuana

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LIST OF ABBREVIATIONS

ABBREVIATIONS

RF	Radio Frequency
PA	Power Amplifier
RFPA	Radio Frequency Power Amplifier
BPA	Balanced Power Amplifier
DPA	Doherty Power Amplifier
SDPA	Symmetric Doherty Amplifier
ADPA	Asymmetric Doherty Amplifier
BA-DPA	Bias Adapted Doherty Amplifier
IDPA	Inverted Doherty Power Amplifier
CPA	Carrier Power Amplifier
PPA	Peaking Power Amplifier
TP	Transition Point
PAE	Power Added Efficiency
DE	Drain Efficiency
BW	Bandwidth
PBO	Power Backed Off
PAPR	Peak-Average Power Ratio
IMD	Inter-modulation Distortion
EVM	Error Vector Magnitude
NPR	Noise Power Ratio
ACPR	Adjacent Channel Power Ratio
ACLR	Adjacent Channel Leakage Ratio
3GPP	Third Generation Partnership Project
4G	Fourth Generation
GSM	Global System for Mobile Communications
W-CDMA	Wideband Code Division Multiple Access
LTE	Long Term Evolution
PEP	Peak Envelope Power
EER	Envelope Elimination & Restoration
RoP	Ratio of Peripheries
FET	Field Effect Transistor
GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
DPD	Digital Pre-distortion
CW	Continuous Wave
FM	Frequency Modulation
FSK	Frequency Shift Keying

AM	Amplitude Modulation
SSB	Single Side-Band
VSB	Vestigial Side-Band
TDMA	Time Division Multiple Access
OFDMA	Orthogonal Frequency Division Multiple Access
QPSK	Quadrature Phase Shift Keying
QAM	Quadrature Amplitude Modulation
OQPSK	Orthogonal Quadrature Phase Shift Keying
D-QPSK	Differential Quadrature Phase Shift Keying
GMSK	Gaussian Minimum Shift Keying
NADC	North American Digital Cellular

CHAPTER I

INTRODUCTION

In modern wireless communication, most of the modulation schemes result in radio frequency (RF) envelopes with significant peak-to-average power ratios (PAPR). It exposes the significant linearity requirement of accurately amplifying the complex envelopes in terms of amplitude and phase. Modern communication systems use digital pulse-shaped modulation schemes such as GMSK, D-QPSK, QAM and multi-carrier systems. Constant envelope modulated signals like GMSK, do not require any linearity function. However others, using varying envelope modulations such as D-QPSK, QAM or Multi-Carrier signals, offering higher data rates and spectral efficiencies require linear amplification. The degree of linearity is determined by the PAPR of the envelope that modulation scheme has. Currently, the well-known RF and microwave amplifiers are called as "conventional power amplifiers". This term includes the linear amplification methods of class-A, -AB, -B, nonlinear, efficient amplification methods of reduced conduction angle mode class-C and switched mode types of class-D, -E, -F. Conventional linear power amplifiers (PAs) such as class-A, -AB, -B are not suitable for envelope varying modulations. The power amplification of amplitude modulated RF signals via the conventional power amplifiers has two inherent problems. The first is that modulating signal envelope will be distorted if the power amplifying device is used at its full rated power level. The second problem is that conventional power amplifiers give maximum efficiency at a maximum rated power level. As the drive power is backed off, the efficiency drops sharply. Such situation is unavoidable when the driving signal of the power amplifier has a significant PAPR. They require power-back-off (PBO) to satisfy emission masks of communication standards so their efficiencies are usually as low as 5-8% with high PAPR signals. The efficiency degradation under the power back-off cases is a crucial problem especially in mobile systems where the battery life and thermal management have a great importance. On the other hand, linear amplifiers are unavoidable elements for most of modern communication systems due to spectrally efficient and higher data rates modulation schemes they have. Time varying envelope driving signals have very wide use of range in these systems. It is clear that usage of conventional PA schemes cannot be a solution for modern communication mobile systems where linear and high efficient operation is desired. Academicians and RF design engineers have been searching for linear and efficient amplification architectures for many years. These methods include linearization methods, efficiency enhancement methods and some linear transmitter architectures [1].

The linearity problem can be solved by linearizing the transfer characteristic of PAs. This kind of enhancement is called as "Linearization". In some applications such as multi-channel transmitters, efficiency is secondary consideration in comparison to linearity. These applications have challenging PA specifications including -60 dBc inter-modulation distortion (IMD) products. Such requirement cannot be achieved by using back off characteristics of conventional linear PAs. In these cases, linearization techniques come to help. Linearization techniques take the amplitude and phase of input RF envelope as a template to compare the output and generate appropriate corrections. However, they have some natural limitations such as lower efficiency than the original PA and narrow modulation bandwidth (BW). Another linearity enhancement method is based on the usage of "Linear Transmitter Architectures". They do not increase power output of the amplifiers; they just give harder saturation characteristics to them. In general, these kind of architectures use the least linear and most efficient PAs such as class-C, -D, -E, -F, and then linearize them to provide the necessary low distortion. They do not provide better linearity characteristic than backed-off conventional linear amplifiers. However, they are noteworthy candidates for the applications where moderate linearity and efficiency are sufficient [2], [3].

On the other hand, “Efficiency Enhancement” methods, solution of battery life problem, attempt to increase the efficiency of linear amplifiers such as class-A, -AB, -B. Efficiency enhancement techniques improve average efficiency of amplifiers without distorting linearity or RF output power in ideal situation. However, as a nature of complexity, it does not provide better distortion characteristic than the original signals in practice. It provides a useful alternative for applications where efficiency is primary concern and linearity is necessary but secondary concern. Efficiency enhancement methods aim to prevent efficiency reduction in low levels of envelope. Most of the electronic warfare systems require moderate linearity but maximum efficiency to deal with excess power consumption problems in mobile systems such as heat and battery life. Such techniques are of serious importance in mobile systems in which the battery life time and thermal management are crucial. High-efficiency PAs are the key components of modern communication systems; they form the final stage of the transmitters for transmitting high output power signals. Designing an efficient PA has a vital importance especially for the mobile systems to save power and to minimize the complexity of cooling structures. Conventional PAs suffer from the efficiency degradation at the low power levels. The modern communication signals due to their high PAPR, force these amplifiers to work at backed-off region, thus reducing the power efficiency of the transmitter considerably. Most of the mobile electronic warfare systems require moderate linearity but maximum achievable efficiency to deal with power consumption, cooling and battery life problems [4]-[6].

The Doherty power amplifier (DPA) is a promising technique for improving the efficiency under output power backed-off conditions. The DPA has lower circuit complexity and cost effective implementation with respect to its alternatives. Moreover, the structure of the DPA can be arranged for different PAPR signals. Its operation is based on the active load modulation technique where the peaking device decreases the load impedance seen by the carrier device, as the driving level increases beyond the transition point. In its standard operation, transition point is set at 6 dB output power backed-off level and the carrier power amplifier (CPA) is active at all power levels whereas the peaking power amplifier (PPA) is active only in upper 6 dB power region. In W.H. Doherty’s original study, the DPA was constructed on vacuum tube amplifiers [7]. The efficiency analysis of solid-state DPA in class-B/class-B configuration was reported by F. H. Raab in 1987 [8]. However, class-B/class-B realization using solid-state transistors require driving level controlled attenuator which should have a special behavior of being shaped at least in two distinct regions with highly nonlinear characteristics [4]. In an alternative usage of DPA with solid state transistors, the CPA is biased in class-B and the PPA is biased in class-C so that it turns on the transition point. However, conventional symmetrical Doherty power amplifier (SDPA) in which the CPA and PPA employ the same periphery transistors result in reduced maximum output power due to the lack of full load modulation at the maximum drive level [9]. In order to improve the performance of class-B/class-C SDPA, different techniques have been proposed and implemented. One of the most cost effective solutions is using uneven power divider in favor of the PPA [10]. Nevertheless, uneven input power division reduces the output power delivered by CPA and consequently reduces the gain at the low power levels at which only the CPA operates [11]. Two of the most popular solutions proposed to improve the performance of realizable DPA are using larger periphery transistor for the class-C biased PPA section or applying a proper bias adaptation to the PPA section [12]. The former method is referred to as asymmetrical Doherty power amplifier (ADPA) and has been widely used in recent applications [13]-[17]. The latter one is known as bias adapted Doherty power amplifier (BA-DPA) and it is realized by using an additional control circuit to change the bias condition of the peaking device from off-state to class-B. Similar to ADPA, the BA-DPA has been widely used in recent applications and promising measurement results have been reported [18]-[20].

In the first phase of this study, the BA-DPA is analyzed by a novel approach in terms of efficiency; various bias waveforms are proposed and their effects on efficiency performance are demonstrated. Analytical results and measurements verify the enhanced efficiency characteristic of BA-DPA over ideal class-B/class-B DPA at high power levels. Moreover, this study also facilitates an approach to determine the required relative periphery of the peaking amplifier in order to have a full load modulated asymmetrical DPA. The improved efficiency characteristic of the asymmetrical DPA with optimal periphery devices is illustrated for the classical 6 dB load modulation region. The BA-DPA and ADPA are designed and implemented at the output power of 50 dBm with nearly 60% drain efficiencies in 6 dB load modulation region. As a first time in the literature, the performances of the asymmetrical DPA and bias adapted DPA are compared on the same platform

and their advantages as well as drawbacks are explained separately. Analytically predicted achievements are verified by measured results obtained from the BA-DPA and ADPA in comparison to conventional SDPA and conventional balanced power amplifier (BPA).

In order to improve the efficiency, various kinds of DPA architectures such as bias adapted DPA and asymmetrical DPA have been proposed up to date [21], [22].There has been a lot of announced Doherty implementation in the literature where the back-off efficiency and the linearity were enhanced by the utilization of the Doherty architecture with the aid of inter-modulation cancellation and digital pre-distortion techniques [23]. The DPA is a strong candidate for multimode multiband operation due to its low hardware complexity, a wide aggregated instantaneous bandwidth and tunable efficiency characteristic for different power ranges. However, most of these studies on Doherty PAs have addressed the narrowband operation and are not suitable for the multimode/multiband operation requirements of the modern communication systems. The conventional Doherty PA offers enhanced efficiency characteristic in a fractional bandwidth of smaller than 10% [24], [25]. Narrow bandwidth operation is the fundamental weakness of the DPA and it compromises the convenience of DPA for multimode/multiband operations.

In the second phase of this study, the DPA structure is modified for broadband operation. The output combiner structure that is composed of quarter-wavelength impedance inverter and impedance transformer in the conventional DPA is replaced by a novel combiner structure. It simplifies the broadband DPA design problem into the design of broadband sub-amplifiers and broadband input power divider. Other key point in this work is designing the CPA and PPA for 25 Ω terminal impedances. The reduced load and source impedances facilitate the achievements of the optimum power and efficiency performances especially in a broadband application. Any additional component in the output matching network of the PPA that introduces positive phase dispersion narrows the maximum achievable bandwidth of the DPA [26]. Hence the reduced load impedance extends the bandwidth of the DPA by simplifying the output matching network of the PPA. Finally, the optimum load impedance of the CPA in low power region that is twice the rated power impedance in the conventional structure is also modified to enhance the efficiency performance in low power region. DPA operation in the frequency band of 0.85-1.85 GHz was achieved with minimum 42% and 37% drain efficiencies through the 6 dB PBO regions in the simulation and implementation phases respectively. The implemented design showed a great performance in the band of 0.9-1.6 GHz with a drain efficiency of higher than 52% through 6 dB PBO region.

This thesis is organized as follows. In Chapter II, the basics about the modern wireless communication as well as the efficiency and linearity challenges in modern wireless communication are discussed. The question of why the conventional amplifiers are not valuable candidates for modern wireless communication is answered. The efficiency enhancement methods in the literature are outlined. In Chapter III, the Doherty PA is discussed in depth. Its operation mechanism and different topologies of DPA are investigated. In Chapter IV, new analyzes on the BA-DPA and ADPA are hold and the enhanced efficiency characteristics over the conventional DPA are verified by implementations. In Chapter V, the broadband Doherty power amplifier using a novel combiner is presented. Finally, the conclusions are drawn in Chapter VI.

CHAPTER II

EFFICIENCY ENHANCEMENT TECHNIQUES IN MODERN WIRELESS COMMUNICATION

Today's communication technology forces us to name the well-known microwave amplifiers as "Conventional Power Amplifiers (PAs)". This term include linear amplification methods of class-A, -AB, -B; nonlinear, efficient amplification methods of reduced conduction angle mode class-C and switched mode types class-D, -E, -F. Nonlinear characteristic of power amplifiers prevent the signal being amplified to reproduce its exact amplified replica at the output. It results in distortion in the amplified signal or splitting it into adjacent channels. Amplitude nonlinearity causes the instantaneous output amplitude or envelope to differ in spectral shape from the corresponding input. Such nonlinearities are due to variable gain in linear region or compression in saturation region in amplifiers. Some classical signals such as CW, FM and FSK have constant envelope. They do not require linear amplification. On the other hand, AM, SSB, VSB like classical signals have time varying envelope so require linear amplification. Moreover, modern signals that require linearity include shaped pulse data modulation for higher data rates and spectral efficiencies such as QAM, QPSK, modulating both I&Q subcarriers, and multiple carrier signals like OFDM. Most popular modern communication signals $\pi/4$-DQPSK is used in NADC-TDMA system, OQPSK, offset-QPSK, is used in CDMA and GMSK is used in European GSM system. In modern wireless communication, the measurement methods of the linearity and efficiency are quite different than those used in old communication systems. The envelope varying signals require different and challenging methods of characterization. The conventional PAs are very sensitive to power backed-off cases in terms of efficiency reduction. Hence, they are not noteworthy candidates to be used with modern communication signals with high PAPR. Some common methods were suggested to overcome this problem and to achieve simultaneous operation with high efficiency and linearity. However, before taking these methods into consideration, it is appropriate to outline the conventional PAs as well as the linearity and efficiency challenges in modern communication.

2.1 Conventional Power Amplifiers

The performances of oldest amplification methods of class-A, -AB, -B and –C depends on biasing scheme. Each classes operation is limited to a specific portion of the input signal during which current flows in the amplifying device. The portion of the RF cycle, active device, transistor, spends in its active region is the conduction angle, denoted by $2\Theta_C$. Classes of operation differ not in only the method of operation and efficiency, but also in their power output capability. The c**lass-A** operation has 360^o conduction angle. In other words, the quiescent current is elected to keep the transistor in its active region during the entire RF cycle. The transistor should be biased in the centre of its linear region, as shown in Figure 2.1, for ideal class-A operation. Because the required bias current is close to a value equal to half of the maximum allowable current. If the transistor is biased in this manner and the input drive signal is kept small enough to prevent the transistor from being driven out of the linear region, the output signal will be a faithful reproduction of the input signal with appropriate amplification. The DC input power is constant and the efficiency of an ideal class PA is 50% at peak envelope power, PEP. Consequently, the instantaneous efficiency is proportional to the power output and the average efficiency is inversely proportional to the PAR for AM. The amplification process in class-A is inherently linear, hence increasing the quiescent current or decreasing the input drive level decreases the harmonic and IMD (inter-modulation distortion) levels. However the efficiency of this class of operation is low. The efficiency of class-A amplifier is degraded by the on state resistance or saturation voltage of the transistor. It is also degraded by the presence of load reactance, which in essence requires the PA to generate more output voltage or current to deliver the same power to the load. Therefore, class-A amplifiers are

typically used in applications requiring low power, high linearity, high gain broadband operation or high frequency of operation.

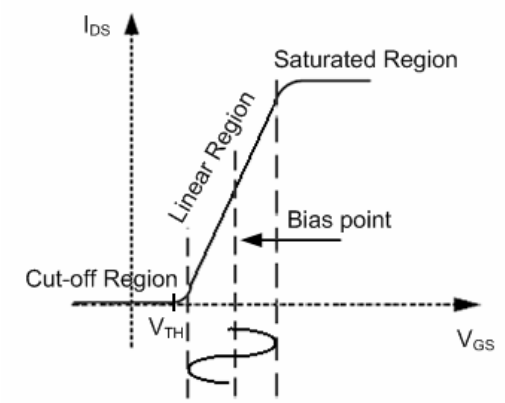


Figure 2.1 Class-A PA Operation

As shown in Figure 2.2, in **class-B** amplifier, the gate bias voltage is set at the threshold resulting in zero idle current flow so 180^o conduction angle. As a result, the transistor is active half of the time and the drain current is a half sinusoid. The DC current is proportional to the drain current which is in turn proportional to the RF output current. Consequently, the instantaneous efficiency of a class B PA varies with the output voltage and for an ideal PA reaches 78.5% at PEP. In class AB, where the conduction angle is between 180^o-360^o, the gate bias voltage is slightly higher than the device threshold value, resulting in drain idle current flow. With respect to the idle current that the transistor consumes from DC source, efficiency reduces from 78.5%, which is the efficiency for zero idle current biasing. The idle current required to place the device into the linear mode of operation is usually given in a datasheet. Real transistors do not change abruptly from cut off to the active region for both BJTs and MOSFETs, the transition is gradual, nonlinear and involves an offset voltage. Therefore, if the device is not biased to produce a small quiescent collector current, there will be crossover distortion. Crossover distortion is reduced by biasing the transistor at a small quiescent collector current typically "1 to 10%" from the peak collector current. Hence, class B amplifier should be considered as a theoretical class of operation, because to overcome the crossover distortion, the conduction angle is made slightly higher than 180^o, and active device operate with small bias current as in class AB. Class B circuits with small idle current, or class AB in more correct definition, are widely used in push-pull topology to provide enough linearity as well as to reach the efficiency of that of class B. These types of amplifiers are very suitable in linear, high power and broadband applications because of the mentioned reasons above. Furthermore the even order harmonics are eliminated automatically in the ideal case.

The gate of a **class-C** power amplifier is biased below threshold, as shown in Figure 2.3 so that the transistor is active for less than half of the RF cycle. Current flows in the output circuit only during the peak swings of the input signal. Class C amplifiers have an important advantage because their collector efficiency is higher than that obtained in class A, class B or class AB amplifiers. The major disadvantages, with respect to other classes of operation, are a higher harmonic content of the output that may require additional filtering and a lower power gain. Linearity is lost but efficiency can be increased up to 100% theoretically by decreasing conduction angle toward zero. Unfortunately this makes output power zero and the input power infinity. A typical compromise is to set angle of conduction as nearly 50% and the resulting efficiency is approximately 85%. Class C is widely used in high-power vacuum-tube transmitters. It is, however seldom used in solid state PAs because it requires low drain resistances making impedance matching difficult [27-31].

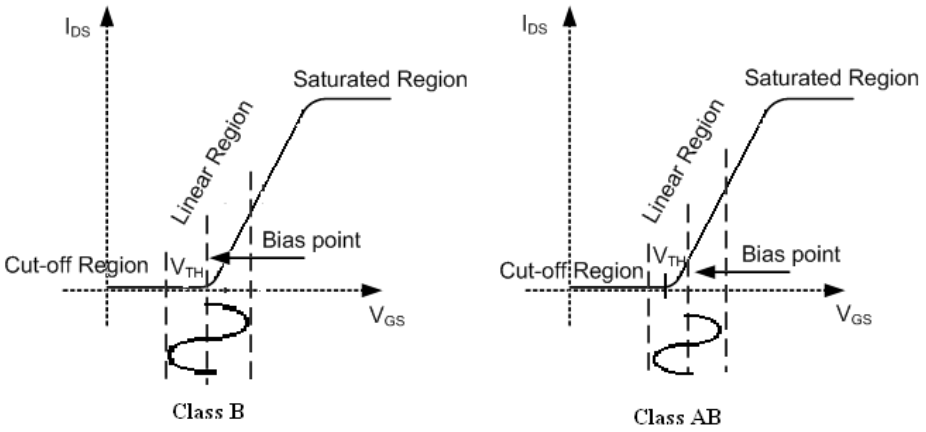


Figure 2.2 Class-B and Class-AB Operations

Other high efficient switched mode amplifiers include class-D, -E, -F saturation PAs. They are suitable for narrowband applications where high efficiency is crucial. All of them have nearly class-B biasing scheme ($2\Theta_C$=180°). However, all these PA schemes have strongly nonlinear characteristics and cannot be used for linear applications. The high efficiency switching mode PA modes of class-D, -E, -F are based on the description of particular loads at the harmonic frequencies.

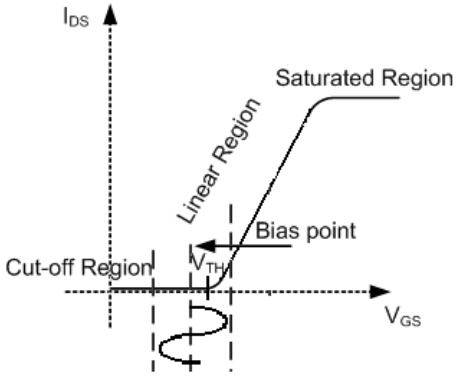


Figure 2.3 Class-C Operation

Class-D is first switching PA topology used in lower HF. Voltage and current waveforms on the active device have never non-zero value simultaneously. The voltage waveform is in rectangular shape compromising of fully odd harmonics and the current waveform is in half rectified sine shape compromising of fully even harmonics. It means that there is no power content in harmonics. Thus, in class-D PAs, given in Figure 2.4, the maximum efficiency is as high as 100% in ideal case. In practice, however, the practical value is 85-90% due to finite switching speed [32].

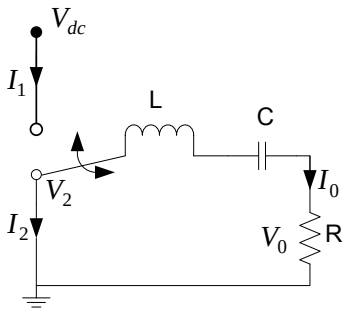


Figure 2.4 Class-D PA Circuitry

Other class of operation which can be named as semi-switching mode PA is **class –E**. Class-E PAs, shown in Figure 2.5, has 100% efficiency again in ideal case. The feedback capacitance, $C_{DS,}$ which is primary terminating factor for class-D, is now part of operation mechanism. Thus it is possible to use class-E scheme up to few GHz frequency range. However, as a rule of thumb, minimum 12-13 dB power gain is mandatory for appropriate operation of this configuration [33].

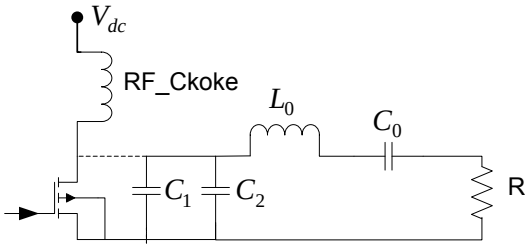


Figure 2.5 Class-E PA Circuitry

As the last class of operation which can be counted between switching mode PAs is **class-F** configuration, given in Figure 2.6. It has half wave rectangular RF current and 3rd harmonic enhanced sine wave RF voltage waveforms. Although class-F PAs has only 88.4% theoretical maximum efficiency, circuitry allows to be used up to few GHz frequency range. Thus, class-F found wide range of usage over the other switching mode PAs especially in GSM or WiMAX applications. One drawback key feature of this class of operation is the three times higher supply voltage level oscillating on the transistor. Designers should be careful to prevent active device from permanent damage via breakdowns [34-36].

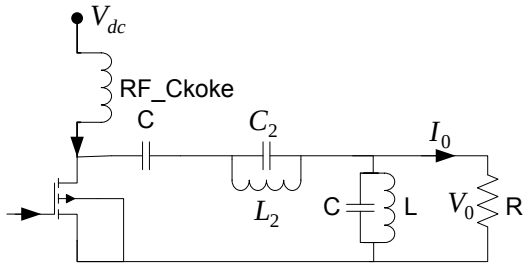
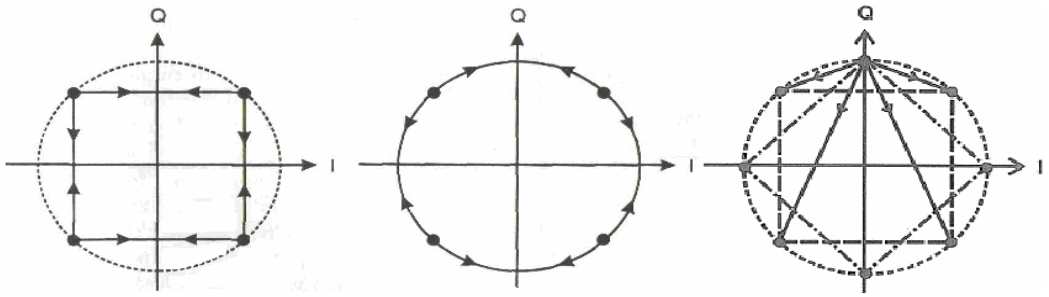


Figure 2.6 Class-F PA Circuitry

2.2 Efficiency and Linearity Challenges in Modern Wireless Communication

In modern wireless communication, digital modulation schemes are used in order to achieve high data rates and to have spectral efficient communication. The envelope functions of the analog modulations can be stated with full mathematic certainty. Envelope repeats itself in every cycle of modulation. On the other hand, digital signals like QPSK have pseudo-random bit sequences. Each bit sequence drives I & Q channels and it never repeats itself. Each point on the constellation diagram of OQPSK, shown in Figure 2.7, is represented by a vector which has specified magnitude and phase. It should be noted that each point has constant amplitude and is determined specifically by its phase angle. However, it does not mean that it has constant envelope because the envelope variation is determined by the trajectory followed during the transition along constellation diagram. The term "offset" means that the phase transitions are allowed to move around the square of transition points in either direction and not allowed to cross along constant circle. Investigations show that OQPSK has nearly 5-6 dB PAPR in envelope. If the transitions were quick enough and signals spent most of the time at specified points on constant amplitude constellation diagram, the envelope variation would be minimal. Basic GMSK constellation diagram, given in Figure 2.7 again, has phase transitions moving along a constant amplitude circle. Hence, GMSK signals have constant envelope. However this benefit of constant envelope comes at a price in that the GSM system is less efficient than OQPS systems in terms of channel capacity. Alternative system using the channel capacity advantage of OQPSK and not constant but low PAPR, advantage of GMSK offers the usage of π/4-DQPSK. The π/4-DQPSK system, whose constellation diagram is shown in Figure 2.7, has nearly 3.5 dB PAPR. Other modern communication signal scheme is "multi-carrier" systems having very high peak-to-average envelope ratio respectively. If there are n carriers in a given operating BW, the theoretical maximum PAPR will be √n. As n increases, however, the chances of a random in-phase alignment becomes much lower, so that in the limit such signals tend toward behaving like Gaussian noise having a peak-to-average envelope ratio of about 9 dB [37].



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OQPSK GMSK $\frac{\pi}{4}$DQPSK

Figure 2.7 Constellation Diagrams of OQPSK, GMSK and π/4-DQPSK

High spectral efficiency and high data rate requirements in the radio standards force the PAs to operate with wider instantaneous BW and higher PAPR signals. The modern communication standards have wider bandwidth up to 100 MHz and higher PAPR up to 12 dB due to high data rates used in the spectrally efficient digital modulation schemes [38]. Currently, a few hundred Mbps level data rates are possible in 4G/LTE-Advanced communications. The evolution of the wireless communication from 2G to 4G-Advanced is summarized in Figure 2.8. The latest wireless communication standard of 4G-LTE is currently used in a few countries but it is supposed to become widespread in the following 3 years. The projected operating bands of 4G-LTE can be summarized as given in Table 2.1.

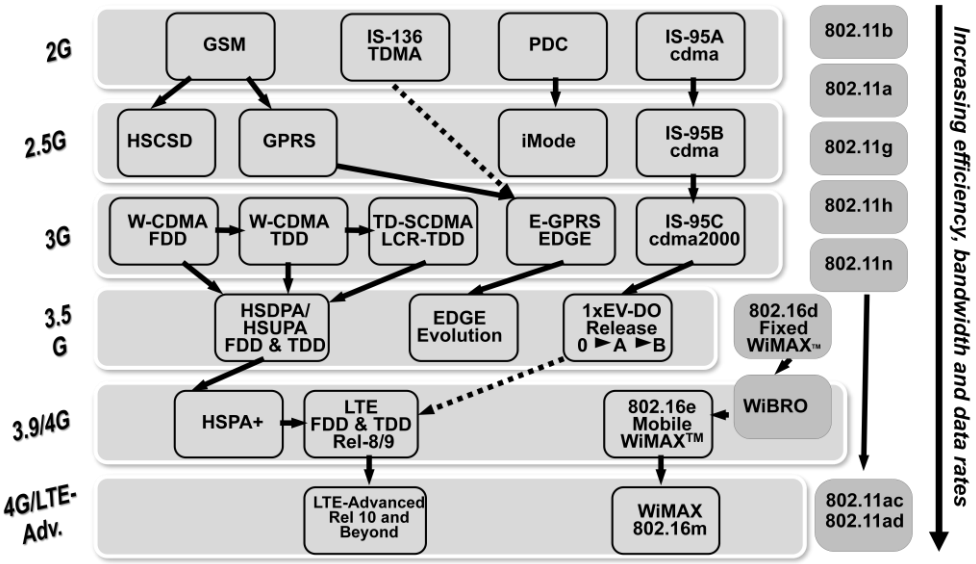

Figure 2.8 Wireless Evolution Between 1990 and 2012

Table 2.1 3GPP, 4G-LTE Operating Bands

LTE Band Number	Uplink (MHz)	Downlink (MHz)	Width of Band (MHz)	Duplex Spacing (MHz)	Band Gap (MHz)
12	698 - 716	728 - 746	18	30	12
17	704 - 716	734 - 746	12	30	18
13	777 - 787	746 - 756	10	-31	41
14	788 - 798	758 - 768	10	-30	40
18	815 - 830	860 - 875	15	45	30
5	824 - 849	869 - 894	25	45	20
6	830 - 840	875 - 885	10	35	25
19	830 - 845	875 - 890	15	45	30
20	832 - 862	791 - 821	30	-41	71
8	880 - 915	925 - 960	35	45	10
11	1427.9 - 1452.9	1475.9 - 1500.9	20	48	28
21	1447.9 - 1462.9	1495.5 - 1510.9	15	48	33
24	1625.5 - 1660.5	1525 - 1559	34	-101.5	135.5
4	1710 - 1755	2110 - 2155	45	400	355
10	1710 - 1770	2110 - 2170	60	400	340
3	1710 - 1785	1805 -1880	75	95	20
9	1749.9 - 1784.9	1844.9 - 1879.9	35	95	60
2	1850 - 1910	1930 - 1990	60	80	20
25	1850 - 1915	1930 - 1995	65	80	15
15	1900 - 1920	2600 - 2620	20	700	680
1	1920 - 1980	2110 - 2170	60	190	130
23	2000 - 2020	2180 - 2200	20	180	160
16	2010 - 2025	2585 - 2600	15	575	560
7	2500 - 2570	2620 - 2690	70	120	50

2.2.1 Linearity and Efficiency

The degree of linearity is determined by PAPR of the envelope that the modulation scheme has. Very high PAPR levels are used in this modern era. Although high efficient conventional PAs such as class-C, -D, -E, -F can be used for constant envelope signals, conventional linear PAs such as class-A, -AB, -B are not suitable for envelope varying modulations. Since they require output-backed-off to satisfy emission masks of communication standards, PAE of such amplifiers may be as low as 3-5%.There are many methods for characterization and measurement of linearity depending upon the specific signal and application. Four common techniques to characterize the linearity of RF PAs are; Carrier to Inter-modulation Ratio (C/I), Noise Power ratio (NPR), Error Vector Magnitude (EVM) and Adjacent Channel Power Ratio (ACPR) [1]. In C/I technique, amplifier is driven with two or more tones of equal amplitude. Nonlinear characteristic of power amplifier causes the inter-modulation components at frequencies such as third order IMDs of $2f_1$-f_2, $2f_2$-f_1 and higher terms. C/I is determined by comparing the levels of fundamental carriers with 3rd order IMDs; IMD_3(dBc)=OIP3(dBm)-Pout(dBm). NPR technique has a wide range of usage in the systems using broadband and noise like signals. Gaussian noise is used to drive PA with notch in one segment of its spectrum. Amplifier nonlinearity causes power to appear in the place of notch over the spectrum. NPR is calculated by taking the ratio of the power appearing in the notch to the power over the spectrum. EVM is measure of how nonlinearity interferes with the detection process. It is defined as the distance between the desired and actual signal vectors normalized to a fraction of the signal amplitude. Often, both root-mean square and peak errors are specified. The linearity characterization technique which is widely used in modern shaped digital signals is ACPR that can be expressed as given in (2.1). It defines how nonlinearity affects adjacent channels. It is defined as the ratio of the power in specified band outside the signal bandwidth to the RMS power in the original signal bandwidth.

$$ACPR = \frac{\int_{f_C - f_0 - BW/2}^{f_C - f_0 + BW/2} [H(f)]^2 S(f) df}{\int_{f_L}^{f_U} [H(f)]^2 S(f) df} \tag{2.1}$$

f_C: center frequency,

f_0: offset frequency,

f_L and f_U: band edges,

BW: band-width,

H(f): pulse shaping filter frequency response, usually it is SRRC,

S(f): actual power spectrum.

H(f) is usually used to weight S(f).Applied offsets and required ACPRs may vary with applications. As a specific example, in W-CDMA systems, -43 dB ACPR is required with the usage of variables as 5 MHz (10 MHz) offset frequency, 3.84 MHz (4.68 MHz) bandwidth and SRRC with α=0.22.

Other critical parameter in PA design is efficiency like linearity. Most widely used definitions are drain efficiency (DE) and power-added efficiency (PAE) which are defined as given in (2.2) and (2.2) respectively.

$$DE = \frac{P_{OUT}}{P_{DC}} \tag{2.2}$$

$$PAE = \frac{P_{OUT} - P_{IN}}{P_{DC}} \tag{2.3}$$

This kind of definition is related to instantaneous efficiency and it is not meaningful for envelope varying signals. The instantaneous efficiency is the efficiency at one specific output level. It is highest at peak output power, PEP, level and decreases as driving signal so output power decreases. Signals with time varying amplitudes produce time varying efficiencies. Hence, most powerful definition for envelope varying signals is average efficiency, which is defined as in (2.4).

$$\eta_{AVG} = \frac{P_{OUT,AVG}}{P_{DC,AVG}} \tag{2.4}$$

Relative amount of time an envelope spends at various amplitudes, is given by the probability density function, PDF, of envelope. Sample PDF characteristics for multi-carrier systems and QPSK systems are shown in Figure 2.9. Note that QPSK like shaped data pulses have PDF concentrated primarily in the upper half of the voltage range assuring PAPR of 3-6 dB. On the other hand, multicarrier systems like OFDM have Rayleigh like distributed envelope characteristic and relatively higher PAPR as much as 6-13 dB. The average input DC power and output power, $P_{DC,AVG}$ and $P_{OUT,AVG}$, can be found by integrating the product of their variation with amplitude and the PDF of envelope. For instance, class-A (constant DC power) and class-B (envelope proportional DC power) has 50% and 78.5% PEP instantaneous efficiencies whereas they have average efficiencies as defined in (2.5) and (2.6) respectively.

$$\eta_{AVG} = \frac{\eta_{PEP}}{PAPR_{dB}} \tag{2.5}$$

$$\eta_{AVG} = \frac{\eta_{PEP}}{\sqrt{PAPR_{dB}}} \tag{2.6}$$

As a numerical example, for the signal whose PAPR=10dB, class-A and class-B amplifiers provide only 5% and 28% average efficiencies respectively [39].

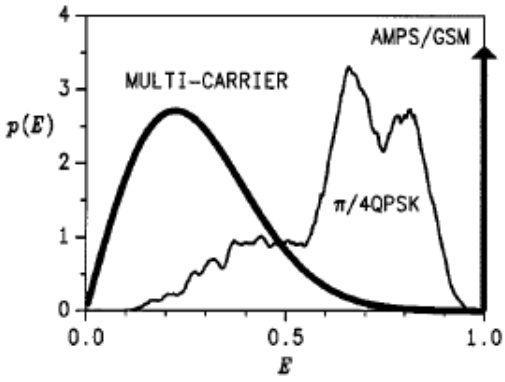

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Figure 2.9 Envelope PDFs of Multicarrier and QPSK Systems

2.2.2 Conventional Power Amplifiers in Modern Wireless Communication

The efficiency degradation under the power back-off cases is crucial problem especially in mobile systems where the battery life and thermal management have a great importance. On the other hand, linear amplifiers are unavoidable elements for most of modern communication systems due to spectrally efficient and higher data rates modulation schemes they have. Time varying envelope

driving signals have very wide use of range in these systems. It is better to make an analogy to class-B PA efficiency derivation in order to remember the source of efficiency reduction at the low levels of envelope and search for the solution to enhance reduced efficiency based on Figure 2.10 [4], [29].

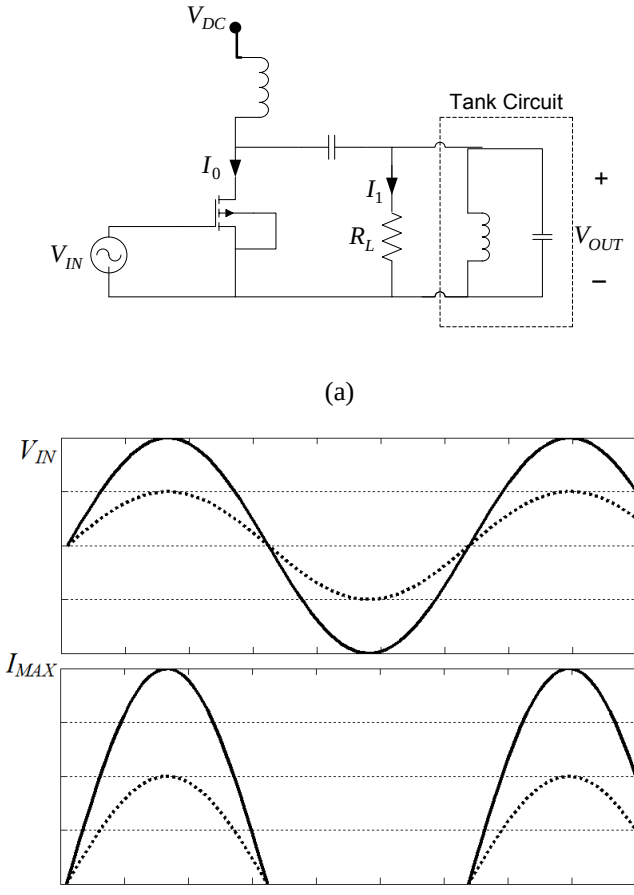

Figure 2.10 Class-B PA; (a) Circuit Schematic, (b) Voltage and Current Waveform with Varying Envelope Drive Signal (dotted line refers to 6-dB power back-off, i.e. 3-dB envelope voltage variation)

Assume that the RF voltage, $V_{OUT}=V_{DC}$ and input driving voltage, $V_{IN}=V_{IN,MAX}$ are given for full swing at the output of the amplifier. And, the resultant half-wave rectified sinusoidal output current I_O has a maximum value of $I_{MAX.}$ Thus, the fundamental component of output current and the DC component are given readily as in (2.7) and (2.8) respectively using Fourier series expansion of half-wave rectified sinusoidal current.

$$I_1 = \frac{I_{MAX}}{2} \tag{2.7}$$

$$I_{DC} = \frac{I_{MAX}}{\pi} \tag{2.8}$$

The optimum load resistance that should be used for maximum voltage swing is given in (2.9).

$$R_{OPT} = \frac{V_{OUT}}{I_1} = \frac{2V_{DC}}{I_{MAX}} \tag{2.9}$$

The overall DC power consumption, output RF power from the amplifier and the overall efficiency can be given as in (2.10)-(2.12).

$$P_{DC} = V_{DC} \cdot I_{DC} = \frac{V_{DC} I_{MAX}}{\pi} \tag{2.10}$$

$$P_{RF} = \frac{1}{2} \cdot V_{OUT} \cdot I_1 = \frac{V_{DC} I_{MAX}}{4} \tag{2.11}$$

$$\eta = \frac{P_{RF}}{P_{DC}} = \frac{\pi}{4} \tag{2.12}$$

Result is no surprising surely. It is the value of 78.4% as given the maximum theoretical efficiency for class-B PA as given before. The actual question, "what will be the new value of efficiency?" is rising in back-off cases for envelope varying signals. Now, assume that; k is voltage wise envelope level reduction in driving signal, or equivalently k^2 is the power wise back-off level. So; the new value of input driving signal can be expressed as in (2.13).

$$V'_{IN} = \frac{V_{IN}}{k} \tag{2.13}$$

The maximum value of the rectified sinusoidal current wave takes the form of (2.14). So, the values of the fundamental output current and the DC current levels are given as in (2.15) and (2.16) respectively.

$$I'_{MAX} = \frac{I_{MAX}}{k} \tag{2.14}$$

$$I'_1 = \frac{I_{MAX}}{2k} \tag{2.15}$$

$$I'_{DC} = \frac{I_{MAX}}{\pi k} \tag{2.16}$$

Using the same load resistance, R_{OPT}, which is not optimum for back-off case of course, new value of output voltage swing takes the form of (2.17).

$$V'_{OUT} = I'_{OUT} \cdot R_{OPT} = \frac{V_{DC}}{k} \tag{2.17}$$

Thus, the updated values of DC power, RF output power and the overall efficiency in back-off case are given as in (2.18)-(2.20).

$$P'_{DC} = V_{DC} \cdot I'_{DC} = \frac{V_{DC} I_{MAX}}{\pi k} \tag{2.18}$$

$$P'_{RF} = \frac{1}{2} \cdot V'_{OUT} \cdot I'_1 = \frac{V_{DC} I_{MAX}}{4k^2} \tag{2.19}$$

$$\eta = \frac{P'_{RF}}{P'_{DC}} = \frac{\pi}{4k} \tag{2.20}$$

Consequently, the efficiency of class-B linear amplifier reduces with voltage reduction coefficient, k, in driving signal envelope. To give a numerical example, 6 dB reduction in input power level (i.e. k=2) reduces the instantaneous efficiency of class-B amplifier to half of its maximum value, to 39% from %78. Similar analyses can be hold for other linear conventional PAs to see the effect of back-off level on efficiency reduction. For instance, maximum efficiency of class-A amplifier is $\eta=1/2$ and the value of efficiency in back-off case deviates to $\eta=1/(2k^2)$. That is, the efficiency of class-A amplifier reduces with the square of voltage reduction (i.e. power reduction) in driving signal level. Thus, class-A and similarly class-AB PAs are more sensitive to back-off cases in terms of efficiency reduction. Although degradation slows as conduction angle is reduced (from class-A to class-B), it is still critical problem in maintaining high average efficiency for signals having high PAPRs.

It is clear that usage of conventional PA schemes cannot be a solution for modern communication mobile systems where linear and high efficient operation is desired. Two methods that are used by all efficiency enhancement methods are tuning the load impedance or supply voltages of the transistors adaptively. Active load pull mechanism can be put in operation at this point. Assume load resistance seen by power amplifier does not remain constant as in (2.9) for reduced envelopes but change proportional to envelope reduction ratio k (voltage wise) as given in (2.21).

$$R'_{OPT} = \frac{2V_{DC}}{I_{MAX}} \cdot k \tag{2.21}$$

Thus, the new forms of the output RF voltage, RF output power and the instantaneous efficiency can be achieved as given in (2.22)-(2.24). Ione should be note that he DC power consumed does not change due to load resistance.

$$V''_{OUT} = I'_{OUT} \cdot R'_{OPT} = V_{DC} \tag{2.22}$$

$$P''_{RF} = \frac{1}{2} \cdot V''_{OUT} \cdot I'_1 = \frac{V_{DC} I_{MAX}}{4k} \tag{2.23}$$

$$\eta = \frac{P''_{RF}}{P'_{DC}} = \frac{\pi}{4} \tag{2.24}$$

Derivation shows that if the load resistance is increased proportional to the reduction ratio in envelope level, maximum instantaneous efficiency value can be maintained. It explains the power of active load pull technique on efficiency enhancement. However, it should be noted that using above simple load changing scheme, the output power achieved is given in (2.25).

$$P''_{RF} = \frac{1}{2} \cdot V''_{OUT} \cdot I'_1 = \frac{V_{DC} I_{MAX}}{4k} \tag{2.25}$$

It means that it is proportional to voltage reduction ratio, k, in driving signal. However, to satisfy linear operation, output power should be proportional to power reduction ratio, k^2. Thus, using simply active load pull scheme does not offer linear operation. At this point, Doherty configuration, proposed by W. H. Doherty in 1936, comes to help. Linearity problem solution and active load resistance changing with envelope level are realized using two different power amplifiers in a single configuration originally proposed by Doherty. Doherty configuration changes load resistor optimally for different level of envelope at least to a useful range and it also restores linearity to fulfill exact reproduction of input spectrum. In Doherty structure active load pull is realized via using another amplifier that supplies current to load and effectively changes the load resistance seen by the carrier amplifier [8].

Academicians and RF design engineers have been searching for linear and efficient amplification architectures for many years. These methods include linearization methods, efficiency enhancement methods and some linear transmitter architectures.

2.3 Linearization Methods

Some applications including multi-channel systems have challenging amplifier requirements. Such specs typically are -60 dBc IM products. This amount of required linearity cannot be realistically held using conventional linear PAs in back off. For instance, assume 3rd inter modulation product for a two carrier input is at -20 dBc for an amplifier running at a1 dB compression point. To get that down for another 40 dBc requires that the amplifier is backed off by 20 dB. It means that operate a 100W power amplifier at 1W output power level. This much of back off reduces the efficiency of linear power amplifiers drastically. Hence, only way of obtaining excellent linear characteristic from amplifiers is lying under the usage of linearization techniques. Three common linearization techniques, which give harder saturation characteristics to PAs as shown in Figure 2.11, proposed and realized are feedback linearization method, pre-distortion method and feedforward system [2].

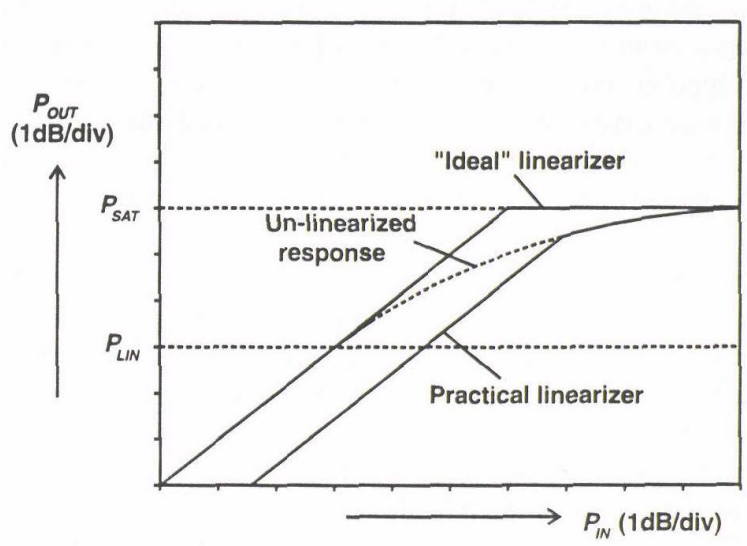

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Figure 2.11 Linearizer Characteristic

2.3.1 Feedback Linearization Method

Feedback linearization method provides high level of linearization but it is limited in terms of modulation bandwidth and it has stability problem. It can be applied either directly to the RF amplifier or indirectly upon the modulation (envelope, phase or I&Q components). Envelope feedback utilizes the signal envelope as the feedback parameter. Harmonic distortion products are generally not issue as they can easily be removed by filtering in most applications. This approach takes care of in-band distortion products associated with amplitude nonlinearity.

In RF feedback technique, shown in Figure 2.12, a portion of RF output signal from amplifier is fed back to and subtracted from RF input signal. The delays involved must be small to ensure stability and moderate gain. The RF input signal is sampled by coupler and the envelope of the input sample is detected. The resulting envelope is then fed to one input of a differential amplifier, which subtracts it from a similarly obtained sample of the RF output. The difference signal representing the error between the input and output envelopes is used to drive a modulator in the main RF path. This modulator modifies the envelope of the RF signal which drives the RFPA. Typical linearity improvement is 10 dB level of the AM-AM. AM-PM distortion is not corrected by envelope

feedback. Other kinds of feedback linearization techniques such as polar feedback or cartesian feedback can be solution to improve AM-PM characteristic [1], [40], [41], [46].

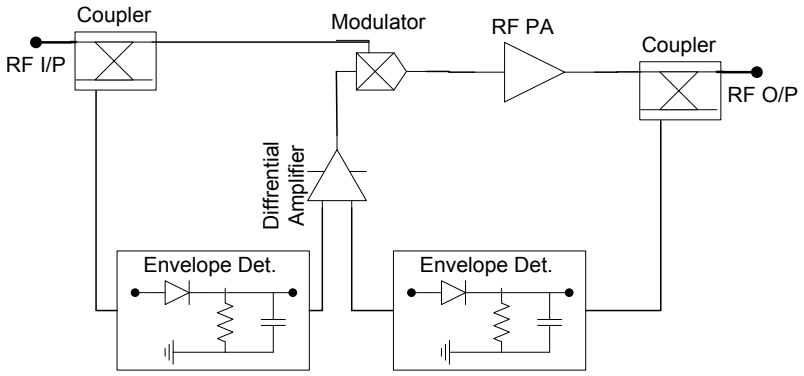


Figure 2.12 Feedback (Envelope) Linearization Scheme

2.3.2 Pre-distortion Method

Pre-distortion method never has the correction precision of a feedback linearizer. However it has the capability of handling much wider modulation bandwidth including multi-carrier signals. They also have no inherent stability problems of closed loop system like feedback linearization method. Basic concept of a pre-distortion system, as shown in Figure 2.13, involves the insertion of nonlinear element prior to the RFPA such that the combined transfer characteristic of both is linear.

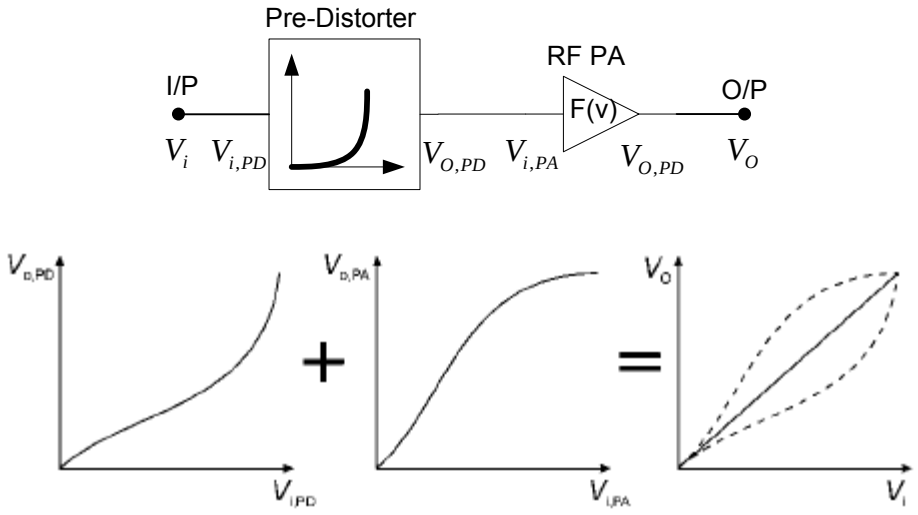


Figure 2.13 Pre-distortion Concept

Pre-distortion can be accomplished at either RF or baseband. RF pre-distorter, shown in Figure 2.14, creates the expansive pre-distortion characteristic by subtracting a compressive transfer function from a linear transfer function (like diode characteristic). The operating bandwidth is limited by the gain and phase flatness of the pre-distorter itself and of the RFPA. Digital pre-distortion (DPD) techniques exploit the considerable processing power now available from DSP

devices which allows them both the form and to update the required pre-distortion characteristic. The availability of faster DSP will open up the possibilities for more precise realization of pre-distortion functions. It seems that DSP drivers will replace analog pre-distorters in most applications [47].

Pre-distortion technique needs few components and it is simple in implementation. It is an open loop system so it has unconditionally stable operation. However, it offers modest linearity improvement. One other fundamental problem in using pre-distortion method is that the cascading of two nonlinear devices possibly generates higher order nonlinear products which do not exist in the original PA response [1], [2], [42], [43].

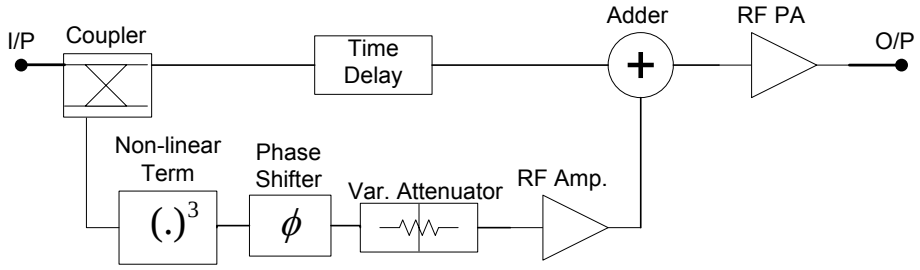


Figure 2.14 RF Pre-distortion Scheme

2.3.3 Feedforward Method

The basic feedforward configuration is shown in Figure 2.15. The input signal is first split into two paths, with one path going to the high power main amplifier while the other signal path goes to a delay element. The output signal from the main amplifier contains both the desired signal and distortions. This signal is sampled to be combined with the delayed portion of the input signal which is regarded as distortion free. The resulting error signal is ideally contains only the distortion components in the output of the main amplifier. The error signal is then amplified by the low power high linear error amplifier and then combined with a delayed version of main amplifier output via coupler. This combination ideally cancels the distortion components in the main amplifier output while leaving the desired signal unaltered.

Successful isolation of an error signal and the removal of distortion components depend upon precise signal cancellation over a band of frequencies. The allowable amplitude and phase mismatches for different cancellation levels related to distortion suppression levels are given in Figure 2.16.

In practice, most of the power of main PA and less of the power of error amplifier reaches the load due to the use of coupler with tens of dB coupling ratio. The peak to average ratio (PAR) of error signal is often much higher than that of the original signal, making amplification of the error signal inherently much less efficient than that of the main signal. As a result, the power consumed by the error amplifier can be a significant fraction of that of main amplifier (e.g. one third). In addition, it is usually necessary to operate both amplifiers, which are low efficient linear type, well into back off to improve linearity. Thus the overall efficiency of a feedforward transmitter may be only 10-12 percent for typical multi-carrier transmitters.

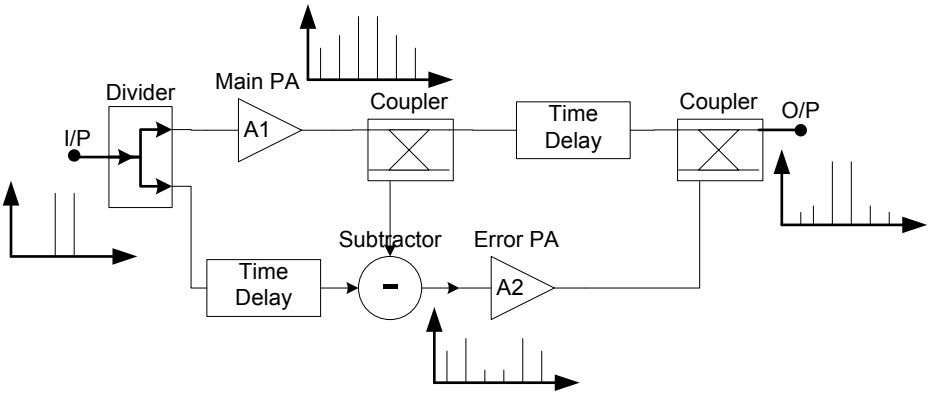


Figure 2.15 Basic Feedforward Amplifier

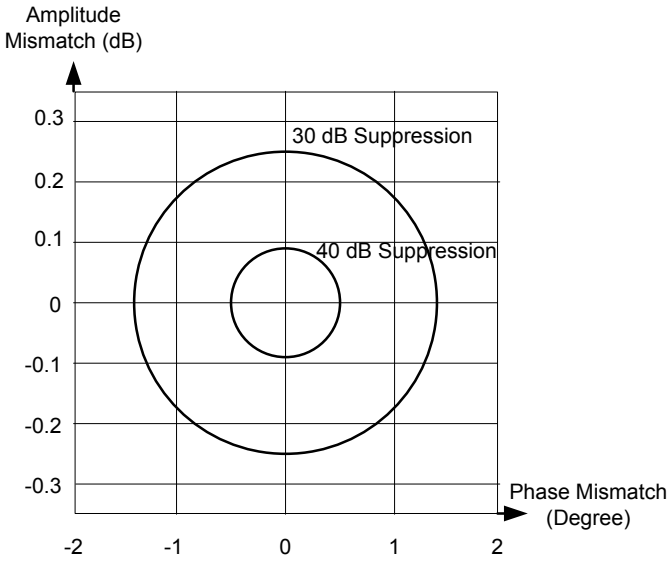


Figure 2.16 Required Gain/Phase Matching of Feedforward Amplifier

Feedforward method offers the precise linearization of feedback technique and the stability and bandwidth of a pre-distortion technique. However, the matching between circuit elements in both amplitude and phase must be maintained to a very high degree. Moreover, the open loop nature of feedforward system does not permit the compensation of changing device characteristic with time and temperature. Although it has poor overall efficiency due to need for an additional power amplifier in the correction loop, it is still the key technique to provide necessary linearity in modern multi-channel digital communication PAs. Today, multi-carrier systems have much more strict IM specification and have envelopes varying at tens of MHz BW rates. These requirements dictate the use of feedforward systems unavoidably. Moreover, feedforward linearizers do not reduce amplifier gain unlike feedback systems in which linearity is achieved at the expense of gain. In this unconditionally stable operation, an arbitrarily high level of correction is possible due to unlimited number of correction path as another advantage of feedforward systems [1], [2], [44], [45], [48].

2.4 Linear Transmitter Architectures

Another linearity enhancement method is based on the usage of "Linear Transmitter Architectures". They do not increase power output of the amplifiers; they just give harder saturation characteristics to them. In general, these kind of architectures use the least linear and most efficient PAs such as class-C, -D, -E, -F, and then linearize them to provide the necessary low distortion. They do not provide better linearity characteristic than backed-off conventional linear amplifiers. However, they are good candidates for the applications where moderate linearity and efficiency are enough.

2.4.1 Envelope Elimination & Restoration (EER) Technique

Kahn proposed EER technique, in 1952, as a more efficient alternative to class-AB RF amplification for SSB transmitters where the information was carried in phase as well as amplitude of the modulated RF carrier [49]. In EER system, shown in Figure 2.17, phase modulation of RF input signal is preserved by passing it through a limiter. The limiter eliminates the possibility of AM-PM distortion in nonlinear amplifier, so undistorted phase characteristic of input signal is obtained at the output of PA. The envelope amplitude can be restored at the output of PA by using a conventional high level voltage supply modulation. In this case, the modulating signal is derived from an envelope detector, followed by a suitable conditioning network. By this way, the efficiency of highly saturated nonlinear PA remains constant due to reduced supply voltage. This constant efficiency idea is lying under the fact that saturated PAs can be approximated as an RF voltage generator whose amplitude is proportional to the DC supply voltage. Thus, in this concept output RF envelope amplitude will be proportional to the modulating supply voltage and no other functionality is needed.

The baseband AM signal A(t) is amplified by an audio amplifier (class-S) or is used to feed a pulse width modulator with subsequent class-D amplifier. Finally, the resulting high power audio signal is used to modulate the collector or power supply of the final RF power stage (class-C, -D, -E). This high level modulation process restores the signal envelope and, assuming that the relevant delays between two paths are suitably equalized, results in a high power replica of input signal being produced at the output. Actually in complete transmitter the input signals are generated at baseband as separate amplitude and phase modulating signals, similar to I&Q signal generation in Cartesian loop transmitters. This may be performed by a digital signal processor.

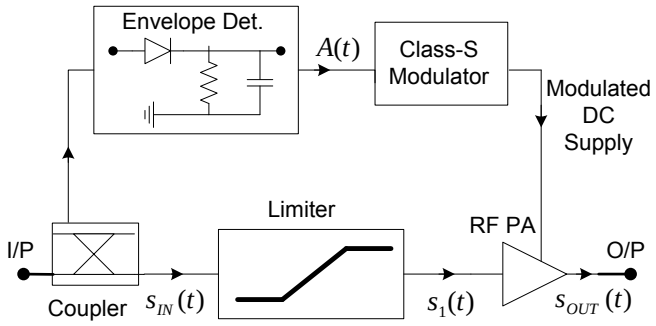


Figure 2.17 EER Transmitter Block Diagram $s_{OUT}(t)$

If losses of conditioning network are ignored, 100% PA efficiency could be maintained over the whole envelope range down to zero. However, in practice there are so many problems in the realization of EER circuit. Bandwidth of the envelope modulator amplifier, differential delay between the envelope and phase signals and AM-PM conversions in limiter are the potential source of IMD in the EER transmitter. Video power conditioner consume a significant amount of power in amplifying the detected envelope signal up to required level of voltage & current capacity to

modulate PA. The efficiency of an EER system is simply the product of efficiencies of high power audio amplifier and the nonlinear RF power amplifier. One other problem is the BW of modulator which is limited to a few MHz. Thus, EER scheme may be adequate for single channel applications not for multi-channel systems. The EER system has the potential for good linearity for the systems with low envelope variation as $\pi/4$-DQPSK. However it does not offer good linearity for systems requiring a full envelope variation such as SSB and 16-QAM [1]-[3].

2.4.2 Linear Amplification Using Non-linear Components (LINC), Chireix Technique

In LINC technique, two similar RFPAs are used. Both PAs operate at a fixed power level so these PAs can be highly nonlinear, efficient types. An outphasing transmitter produces an amplitude modulated signal by combining the outputs of 2 PAs driven with signals of different time varying phases [50]. The phase modulation causes the instantaneous vector sum of 2 PA outputs to follow the desired signal amplitude. Usage of conventional combiner the average efficiency to be changing that is conversely proportional to PAR as in conventional PAs. The Chireix technique uses shunt reactance on the input to the combiner to tune out the drain reactance at particular amplitude which in turn maximizes the efficiency in the vicinity of amplitude variation.

As shown in Figure 2.18, AM/PM modulator converts AM modulated signal into two PM signals having opposite sense.

$s_{in}(t) = A(t)\cos(\omega t)$;

$s_1(t) = \cos\{\omega t + \cos^{-1}(A(t))\}$ and $s_1(t) = \cos\{\omega t - \cos^{-1}(A(t))\}$;

Using the equality of $\cos(a+b) + \cos(a-b) = 2\cos(a)\cos(b)$;

$G\{s_1(t) + s_2(t)\} = 2GA(t)\cos(\omega t) = s_0(t)$,

where G is voltage gain of amplifiers.

Simple outphasing PAs use a power combiner and DSP phase control and still offer some potential for using nonlinear PA, in linear amplification. In all cases, however, this method requires a priori knowledge of the signal which reduces the flexibility of the systems.

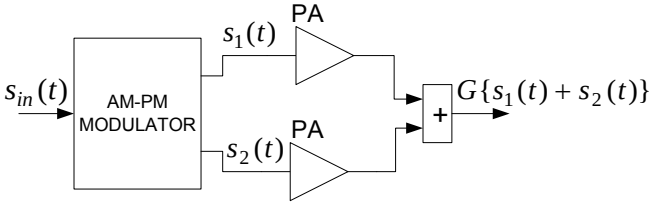


Figure 2.18 Chireix Outphasing Amplifier

It is capable of an ideal 100% efficiency at all envelope levels of output RF signal theoretically. Any degradation is due to non-ideal components and original PA efficiency. Moreover, technique is straightforward to understand and implement. There are, however, a number of practical difficulties which have led to the relatively few applications of the technique to date. Moreover, direct processing of RF modulated signal is difficult to realize and distorts the linearity of LINC transmitter. Since the two signals are not co-phased, conventional RF power combiners cannot be used alone. One possible usage of conventional combiner is possible with the additions of L, C type elements. Good compensation characteristics is obtained at low outphasing phase angles (i.e. low envelope variation), but efficiency at high phase angles (i.e. higher envelope amplitude variation) is

lower. It is because of that load seen by PAs is dramatically changed with varying phase angle. Moreover, required phase compensation may have bandwidth restriction [1]-[3].

2.5 Efficiency Enhancement Methods

Efficiency enhancement techniques improve average efficiency of amplifiers without distorting linearity or RF output power in ideal situation. However, as a nature of complexity, it does not provide better distortion characteristic than the original signals in practice. The methods that will be mentioned under this title are used to increase average efficiency of linear amplifiers under envelope varying signals. They distort linearity a bit to achieve high efficiency.

2.5.1 Adaptive Biasing, Envelope Tracking, and Dual Bias Control

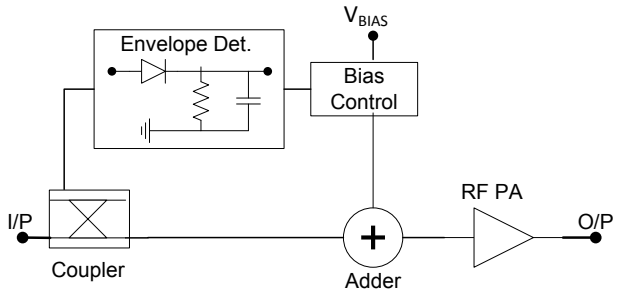
Envelope tracking, adaptive biasing and dual bias control schemes, shown in Figure 2.19, are all like EER method. However these methods are simple in implementation and less effective relatively. One other common key point of these three methods separating them from EER technique is that they require linear power amplifiers in RF section [51], [52].

In adaptive bias method standing DC bias is varied on a class-A amplifier which is varied with the envelope level like in EER method. However, constant envelope signal drives power amplifier in EER method so linear amplifier is not mandatory item. Coupler takes the sample and after detection, this sample is used to bias control. By this way, it is ensured that the PA always has sufficient bias current to operate in its linear region, hence maintaining low distortion without drawing an excessive supply current at low envelope levels to enhance efficiency.

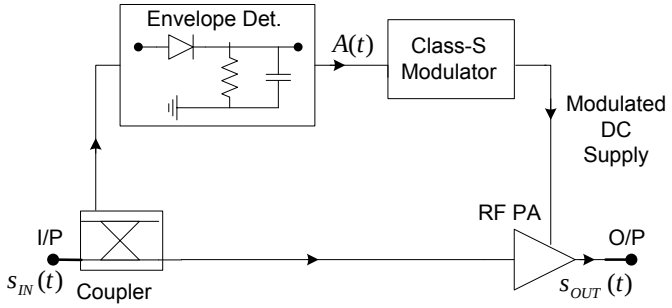
As mentioned before, class-A has 50% efficiency maximally and it is lowered in proportion to the square of the back off level. In this method, bias is controlled with respect to the changing level, so more efficient linear amplifier like class-B is not suitable. Thus, the overall efficiency is not so good. Serious restriction is the changing gain with the bias levels of gate biasing voltage that result in AM-AM distortion degrading linearity of the PA. In Table 2.2, efficiency enhancement with class-A adaptive biasing scheme is given for different envelope cases.

Another simple version of EER is envelope tracking methods which needs class-A, -AB, -B type linear amplifier due to the non-constant amplitude driving signal. Envelope detector extracts the envelope information from a sample of input RF signal and feed it to a high efficient audio class-S amplifier as in EER. In envelope tracking, class-S modulator just provides sufficient supply voltage to the amplifier so that the efficiency is not distorted excessively at the low levels of instantaneous efficiency. However, in EER, modulator is used to modulate the supply voltage of nonlinear PA to linearize its characteristic. In envelope tracking scheme, class-A type PA is not mandatory in contrast to adaptive biasing circuit, thus PEP and overall efficiencies can be possibly higher. However, due to class-S modulator own efficiency, PEP efficiency can never reach the level of PEP efficiency values of class-A, -AB, -B type PAs.

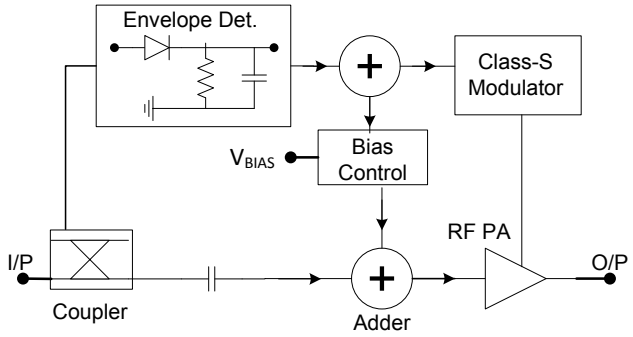
Third similar method of efficiency enhancement technique, dual bias control, is the extension of adaptive biasing and envelope tracking schemes. It enhances the average efficiency using the power of both methods. As an numerical example, class-A PA has only 3.3% average efficiency for multi-carrier signal of Rayleigh distribution with 10 dB PAR. Adaptive biasing and envelope tracking methods supply 9% and 10% average overall efficiencies where dual bias control scheme gives 24% for the same driving signal scheme [1], [4], [6].



a-) Adaptive Biasing Scheme



b-) Envelope Tracking Scheme



c-) Dual Bias Control Scheme

Figure 2.19 Adaptive Biasing, Envelope Tracking and Dual Bias Control Schemes

2.5.2 Doherty PA Architecture

Doherty amplification method whose basic structure is given in Figure 2.20 is the most powerful method of efficiency enhancement. The efficiency reduction at the low levels of driving envelope can be solved at least to a useful range. Main operation mechanism of active load pull technique is the key point lying behind Doherty amplifier operation. RF load impedance is modified by applying current from a second phase coherent source [7], [12].

Table 2.2 Comparison of Class-A & Adaptive Biasing Class-A Efficiencies

Modulation	r^2	Class-A PA Av. Eff., $\eta_{AVG,A}$	Adaptive Biasing Av. Eff. $\eta_{AVG,A.B.}$
Single FM Carrier	1	0.5	0.5
2-Tone Test	0.5	0.25	0.392
6-dB Back-off	0.25	0.125	0.282
16 QAM	0.556	0.278	0.394
64 QAM	0.429	0.215	0.350
256 QAM	0.378	0.189	0.328

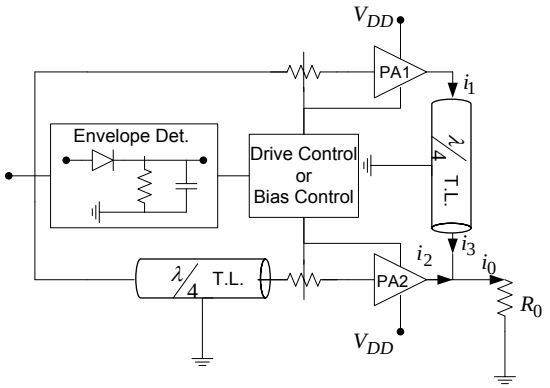


Figure 2.20 Doherty Power Amplifier Structure

DPA is not a method offering maximum efficiency or perfect linearity over the other techniques. However, it is the most practical method of efficiency enhancement with optimal linearity as the key requirements of many electronic warfare transmitters. This is due to the advantages below that DPA offers [6];

- DPA offers linear operation and does not have limitations in the high frequency range unlike high efficient conventional PAs like class -D, -E, -F.
- Optimum efficiency characteristics for envelope varying signals with different Peak-to-Average Ratios (PARs) can be achieved with small modifications on the DPA architecture.
- DPA modulation BW is not limited by the modulator (e.g. class-S modulator) as in EER technique.
- In DPA configuration, high power IF amplifiers and modulation transformers are not required, it can be realized using pure RF techniques.
- DPA's efficiency is as good as or better that that of envelope tracking or outphasing systems, however, DPA operates in purely real load impedances in contrasts to highly reactive load impedance produced in an outphasing system.

Extra linearization methods such as DPD, feedforward and envelope feedback can be easily used with DPA. The details about its operation concept and its different architectures are discussed further in Chapter III.

CHAPTER III

DOHERTY POWER AMPLIFIER

The DPA, as mentioned in the previous chapter, solve the efficiency reduction problem of conventional PAs in the power back-off (PBO). In order to realize DPA operation, the structure should be analyzed in detail. Class-B PA efficiency has been derived in Chapter II for varying envelope signals. It is better to make an analogy to that derivation in order to remember the source of efficiency reduction at the low levels of envelope and search for the solution to enhance reduced efficiency. The overall efficiency of class-B amplifier in back-off case had been derived as in (3.1) where k represents the voltage level back-off. Thus, it had been concluded that the efficiency of class-B amplifier reduces proportional to the PBO level.

$$\eta = \frac{P'_{RF}}{P'_{DC}} = \frac{\pi}{4k} \tag{3.1}$$

If the optimum load impedance is increased proportional to the envelope reduction, k, the efficiency takes the form of (3.2) that is the peak efficiency of class-B amplifier.

$$\eta = \frac{P''_{RF}}{P'_{DC}} = \frac{\pi}{4} \tag{3.2}$$

However, it should be noted that using above simple load changing scheme, the resultant output power given in (2.25) does not offer linear operation. It is proportional to the voltage reduction ratio, k. However, in linear amplifying scheme, output power is required to be proportional to power reduction ratio, k^2. Thus, using simply active load pull scheme does not offer linear operation.

$$P''_{RF} = \frac{1}{2} \cdot V''_{OUT} \cdot I'_1 = \frac{V_{DC} I_{MAX}}{4k} \tag{3.3}$$

Doherty power amplifier (DPA), proposed by W. H. Doherty in 1936, solves the linearity problem by active load resistance changing with respect to the envelope level. In Doherty structure active load pull is realized via using peaking amplifier that supplies current to load and effectively changes the load resistance seen by the carrier amplifier. Doherty configuration changes load resistor optimally for different levels of envelope at least to a useful range and it also restores linearity to fulfill exact reproduction of input spectrum. The original DPA is in two-stages configuration. However, some requirements such as wider high efficiency PBO, higher efficiency, higher linearity and higher frequency of operation cause to development of different DPA structures. The structures beyond the original two-stages DPA can be categorized as multi-way DPA, inverted DPA and distributed DPA.

3.1 Doherty Load Modulation Concept

The DPA based on the active load modulation scheme besides the power combining property it has. The Device, called as Auxiliary or Peaking power amplifier (PPA) decreases the load impedance seen by other device, called as Main or Carrier power amplifier (CPA), as the driving level increases beyond the transition point. In order to observe this load modulation scheme, operation of two generators connected via load can be investigated as the starting point of DPA configuration analysis. Original generator (GEN1), given in Figure 3.1, experiences the effect of gradual lowering of load impedance due to the added generator (GEN2). GEN1's output current increases without any increase in its output voltage and when GEN2 has a voltage equal to that of GEN1, the

effective impedance, normally 2R, seen by GEN1 is reduced to R. Thus, the current sourced by GEN1 is, i'=V/R instead of i'=V/2R. In order to realize combined power characteristic of this structure, one can look for the current-output load impedance dynamics. GEN1 supplying i current into R load achieves the power of (3.4).

$$P = i^2 R \tag{3.4}$$

GEN1 alone supplies i/2 current into 2R load (for constant voltage level V), thus it achieves the output power of (3.5).

$$P' = \frac{i^2}{4} \cdot 2R = \frac{i^2}{2} R = \frac{P}{2} \tag{3.5}$$

GEN1 and GEN2 supplying (i/2)+(i/2)=i current into 2R load results in the power of (3.6).

$$P'' = i^2 \cdot 2R = 2i^2 R = 2P \tag{3.6}$$

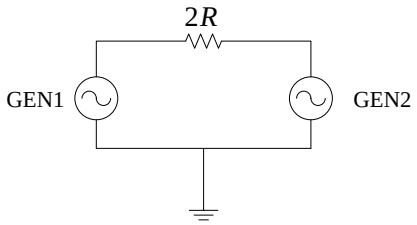


Figure 3.1 Ideal form of Doherty Load Modulation Scheme

Thus, in overall structure with 2R load impedance, 2P amount of power can be achieved where each PA can supply P power output into R load impedance. Moreover, assuming the maximum efficiency operation of each device in P power level into R load impedance case, there is not any degradation in efficiency for P/2 output power operation into 2R load impedance. Current sourced by device is halved to its original value, i'=i/2, under 2R load impedance and same output voltage condition. The reduced output power and DC component of current take the form of (3.7) and (3.8) respectively. The DC power consumption is halved and overall efficiency remains constant.

$$P' = \frac{i^2}{4} \cdot 2R = \frac{i^2}{2} R = \frac{P}{2} \tag{3.7}$$

$$i_{DC} = \frac{4}{\pi} i \tag{3.8}$$

To conclude the overall operation of the block in Figure 3.1; GEN1 which have maximum efficiency operation with P level of power into R load impedance can provide same efficiency in the case of P'=P/2 output power into 2R load impedance. Moreover GEN1 and GEN2 supply 2P level of total output power into 2R load impedance (P amount of power from each) again with maximum efficiency. This is the result of load modulation effect of GEN2 on GEN1.

In order to realize practical amplifying operation, two generators in Figure 3.1 should be replaced by PAs. Ideal generator shows no impedance to the current flow whereas PA shows infinite impedance. To maintain same operation mechanism with PAs, $\lambda/4$ transmission line or equivalent lumped network like transformer is required in order to have inversely proportional input impedance to the terminating impedance. Modified circuit for practical applications is given in Figure 3.2. In this topology, when PA2 is in off state, it shows an open circuit and transformer

inverts it to a short circuit hence, PA1 operates into 2R load impedance. That is, with inactive PA2, the impedance values are realized as given in (3.9).

$$Z_2 = \infty,\ Z_T = 0 \text{ and } Z_1 = 2R \tag{3.9}$$

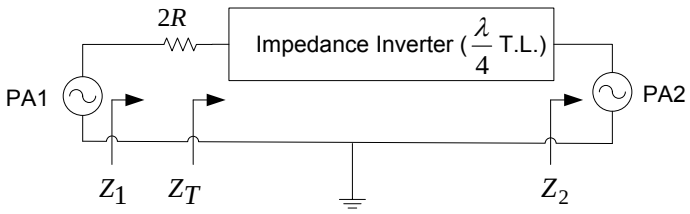


Figure 3.2 Basic form of Doherty Load Modulation Scheme

While the power contribution by PA2 increases from zero, since its drain current is opposite phases to its voltage, the impedance contributed by PA2, Z_2 can be modeled as negative shunt resistance increased toward zero in ideal case. By the way, the impedance due to transformer, Z_T, decreases from zero to negative values which provides PA1 by working into impedance lower than 2R. At the peak level of driving signal, where the power distribution from both PAs are in same amount, transformer impedance and load impedance to PA1 take the values of Z_T=-R and Z_1=R respectively.

At this point it should be noted that, current at the second port of transformer is directly related with the voltage at the input port. This is the result of transformation action and it can be easily observed by ABCD (chain) parameters of the transformer referring to the Figure 3.3. Let λ/4 transmission line transformer be used, the ABCD parameters of that network can be written as in (3.10).

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cos(\theta) & jZ_c \sin(\theta) \\ \dfrac{j\sin(\theta)}{Z_c} & \cos(\theta) \end{bmatrix} = \begin{bmatrix} 0 & jZ_c \\ \dfrac{j}{Z_c} & 0 \end{bmatrix} \tag{3.10}$$

Since the input/output voltages and currents of network are associated with the equality given in (3.11), by inserting the above result here, the result of (3.12) can be reached.

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \tag{3.11}$$

$$V_1 = BI_2 \tag{3.12}$$

In other words, current injected by PA2 at the second port of transformer is realized as voltage injection at the input port in series with the voltage of PA1.

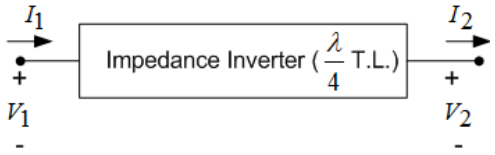


Figure 3.3 Transformer (Inverter) Action on Voltage/Current

To conclude, PA2 holds two actions simultaneously. Besides delivering its power, it lowers the effective load impedance of PA1 with the action of impedance inverting network. Power distributed by PA1 increases without any increment in its drain voltage level which is already at the maximum level.

However, the configuration given in Figure 3.2 does not expose the practical way of implementation because all loads are grounded in practice. Hence, realizable alternative form of power combining and load modulation scheme related to Doherty configuration can be given as in Figure 3.4.

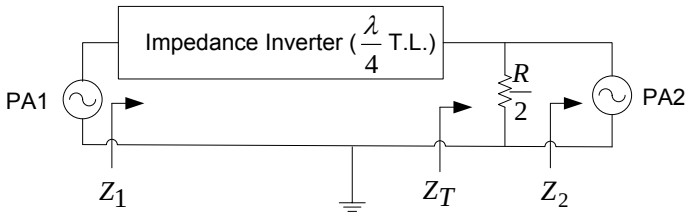


Figure 3.4 Realizable Form of Basic Doherty Load Modulation Scheme

In this configuration, shunt load impedance of R/2 is used instead of series load impedance of 2R. In the inactive mode of PA2, Z_T=R/2 and the transformer is designed to have Z_1=2R. That is, if the quarter wave (λ/4) transmission line is used as inverting network, the characteristic impedance of that line should be Z_C=R. While the power distribution by PA2 is increasing, the equivalent negative shunt resistance, Z_2, starts to decrease towards zero and consequently Z_T increases and Z_1 decreases. Again, at the maximum level of driving signal, both PAs operate into the load impedance of R with delivering maximum output powers at the maximum efficiencies [7], [12].

3.2 Two-Stages Standard Doherty Power Amplifier Configuration

The most common practical representation of Doherty configuration is given in Figure 3.5. The operation mechanism of DPA was explained in the previous report. However, before carrying the analysis on this common Doherty configuration, it is better to conclude the DPA operation without going into detail. At low output power levels relating to low driving level, only PA1, CPA, is active and it operates as linear amplifier due to class-B biasing scheme it is set. By the action of the transformer, it reaches to saturation region at the transition point which is well below the PEP output power of overall configuration. In classical scheme, transition point has been set at 6 dB Power Back off, PBO, level which is relating to the half of the peak output voltage. At output voltage levels higher than this transition point, PA1 remains saturated and PA2, PPA, operates linearly. Hence, PA2 acts as a controlled current source and PA1 acts as a voltage source but due to the transformer, PA1 is seen as controlled current source from the output of the transformer as well. After the transition point, PA2 injects current to the load and the higher output voltage on the load than the voltage level due to PA1 is achieved. Thus, impedance to the output of the transformer increases beyond the original load impedance which means that the impedance seen by PA1 decreases due to impedance inversion. This results in increasing of current injected so the power delivered by PA1. In DPA configuration, maximum efficiency is achieved at both the transition point, where PA1 is saturated and PA2 is inactive, and at the PEP point where both PAs are saturated.

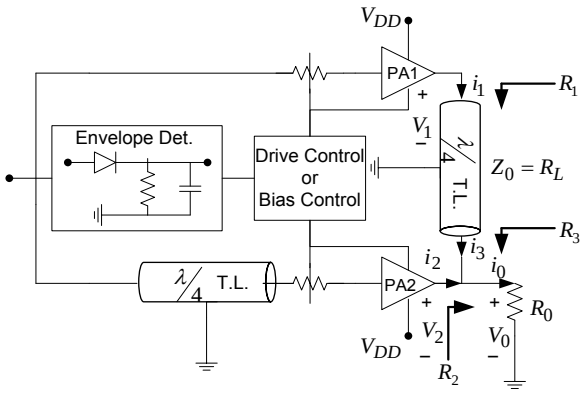


Figure 3.5 Common Practical Representation of DPA Configuration

In ideal DPA configuration, proper operation of PAs which are operated in different manner can be provided by controlling the driving levels or bias points as shown in Figure 3.5. The efficiency characteristic of DPA can be observed by analyzing its operation under three sub-classified power states; 1-) Peak power region, 2-) Low Power region, 3-) Medium power region [8]. As mentioned, PA1 is active over all states and PA2 is active only in upper states beyond the transition point. Analysis can be started by adapting on the transformer action of transforming action of λ/4 transmission line after PA1. At this point it should be noted that, the λ/4 transmission line prior to PA2 is used just for achieving phase coherence between two amplifier paths. Referring to Figure 3.5 again, power delivered by each amplifier to the output can be stated as follows.

Basic λ/4 transformer identity gives the equation of (3.13).

$$Z_0{}^2 = R_1 R_3 \tag{3.13}$$

Voltage transformation ratio, T, due to λ/4 transformer using the power conservation identity at two sides of transformer can be written as in (3.14).

$$\frac{V_1{}^2}{R_1} = \frac{V_3{}^2}{R_3}, \; \mathrm{T} = \frac{V_1 2}{V_3{}^2} = \frac{R_1}{R_3} = \frac{Z_0{}^2}{R_3{}^2} \tag{3.14}$$

Conservation of power at the sides of transformer also dictates the equation of (3.15). The (3.14) and (3.15) gives the identity of (3.16).

$$i_3 = \frac{V_1}{\sqrt{R_1 R_3}} = \frac{V_1}{Z_0} \tag{3.15}$$

$$i_3{}^2 R_3 = \frac{V_1{}^2}{R_1} \tag{3.16}$$

Both PAs distribute current to the output; $i_0=i_2+i_3$. At this point defining current distribution ratio of PA1 to total output current, α, as in (3.17), the current distribution of PA2 can be obtained as in (3.18)..

$$\alpha = \frac{i_3}{i_0} = \frac{i_3}{i_2 + i_3} \tag{3.17}$$

$$\frac{i_2}{i_0} = 1 - \alpha \tag{3.18}$$

Since the power delivered to the output is defined as in (3.19), the power delivered to output by PA1 can be stated as in (3.20). Similarly, the power delivered by PA2 can be found as in (3.21). Hence, it can be concluded that the power delivered to the output load by amplifiers are proportional to the current distributed by them.

$$P_0 = \frac{V_0 i_0}{2} \tag{3.19}$$

$$P_1 = \frac{V_0 i_3}{2} = \frac{i_3}{i_0} i_0 \frac{V_0}{2} = \alpha P_0 \tag{3.20}$$

$$P_2 = (1-\alpha) P_0 \tag{3.21}$$

The impedance seen by PA1 through transformer, R_3, and by PA2, R_2, in terms of output load impedance R_0 can also be written as in (3.22) and (3.23).

$$R_3 = \frac{V_0}{i_3} = \frac{V_0}{\alpha i_0} = \frac{R_0}{\alpha} \tag{3.22}$$

$$R_2 = \frac{V_0}{i_2} = \frac{V_0}{(1-\alpha) i_0} = \frac{R_0}{1-\alpha} \tag{3.23}$$

At **peak power** operation where both PAs are in saturated regions, peak output voltages of both amplifiers are therefore V_{DD}, so does the peak output voltage of the system Hence the output power at PEP is given as in (3.24).

$$P_{0,PEP} = \frac{{V_{DD}}^2}{2R_0} \tag{3.24}$$

Since, peak output voltages of PA1, PA2 and the system are equal as given in (3.25) and $V_{DD1}=T \cdot V_{DD2}$, it can be concluded that the voltage transformation ratio is unity at PEP, T=1.

$$V_{DD1} = V_{DD2} = V_0 = V_{DD} \tag{3.25}$$

Conservation of power identity gives the relation of (3.26). It should be noted that α is relating to the power division ratio at PEP. It also addresses the transition point where PA1 saturates and PA2 starts to conduct.

$$R_1 = R_3 = Z_0 = \frac{R_0}{\alpha} \tag{3.26}$$

In classical operation scheme of DPA, α=1/2, so $Z_0=2R_0$ and both PAs distribute same amount of power to the output at PEP and transition point is at 6 dB BOP level.

Currents i_1, i_2 and i_3 can be expressed in terms of output current i_0. Since the equation of (3.27), (3.28) and (3.29) are all valid expressions, all current values can be calculated in terms of output current as in (3.30) and (3.31).

$$R_0 = \alpha R_1 = \alpha R_3 = (1-\alpha) R_2 \tag{3.27}$$

$$i_1 = \frac{V_{DD}}{R_1},\ i_3 = \frac{V_{DD}}{R_3},\ i_2 = \frac{V_{DD}}{R_2} \tag{3.28}$$

$$i_1 = i_3 = \alpha i_0 \tag{3.29}$$

$$i_0 = \frac{V_{DD}}{R_0} = \frac{V_{DD}}{\alpha R_1} = \frac{i_1}{\alpha} = \frac{V_{DD}}{\alpha R_3} = \frac{i_3}{\alpha} \tag{3.30}$$

$$i_0 = \frac{V_{DD}}{R_0} = \frac{V_{DD}}{(1-\alpha)R_2} = \frac{i_2}{1-\alpha},\ i_2 = (1-\alpha)i_0 \tag{3.31}$$

Assuming class-B operation of both amplifiers, DC currents drawn by each amplifier is just the scaled version of their fundamental output current as given in (3.32) and (3.33). Thus, the total DC current consumption by both PAs and total DC power consumed by PAs can be found as expressed in (3.34) and (3.35).

$$I_{1,DC} = \frac{2}{\pi} i_1 = \frac{2}{\pi} \frac{\alpha V_{DD}}{R_0} \tag{3.32}$$

$$I_{2,DC} = \frac{2}{\pi} i_2 = \frac{2}{\pi} (1-\alpha) \frac{V_{DD}}{R_0} \tag{3.33}$$

$$I_{DC} = I_{1,DC} + I_{2,DC} = \frac{2}{\pi} \frac{V_{DD}}{R_0} \tag{3.34}$$

$$P_{DC} = V_{DD} I_{DC} = \frac{2}{\pi} \frac{{V_{DD}}^2}{R_0} \tag{3.35}$$

Since the output RF power distributed by PAs is as given in (3.36) and the instantaneous efficiency at PEP can be calculated as in (3.37). This result concludes that DPA has the maximum efficiency of PAs used inside at PEP level.

$$P_{RF} = \frac{i_0 V_{DD}}{2} \tag{3.36}$$

$$\eta_{PEP} = \frac{P_{RF}}{P_{DC}} = \frac{\pi}{4} \tag{3.37}$$

At low power levels below the transition point where PA2 is inactive and PA1 operates as linear current source, similar derivations can be hold to calculate instantaneous efficiency. In this segment, since PA2 is in cutoff state; R3=R0 and α is found be as in (3.38).

$$\alpha = \frac{R_0}{R_L},\ R_1 = \frac{{R_L}^2}{R_0} = R_0 \frac{{R_L}^2}{{R_0}^2} = R_0 \frac{1}{\alpha^2} \tag{3.38}$$

Correspondingly, the voltage transformation ratio can be expressed as in low power region as given in (3.39) and the voltage of PA1 can be expressed as $V0=\alpha \cdot V1$.

$$\mathrm{T}^2 = \frac{R_1}{R_0} = \frac{1}{\alpha^2} = \frac{{V_1}^2}{{V_0}^2} \tag{3.39}$$

Since peak voltage of PA1 is $V_1=V_{DD}$, PA1 reaches saturation at the output voltage of $V_0=\alpha \cdot V_{DD}$. Similarly, the current relation satisfies the equation of (3.40) and DC component of it can be written as in (3.41).

$$i_1 = \frac{i_0}{\mathrm{T}} = \alpha i_0 = \alpha \frac{V_0}{R_0} \tag{3.40}$$

$$I_{1,DC} = \frac{2}{\pi} i_1 = \frac{2}{\pi} \alpha \frac{V_0}{R_0} \tag{3.41}$$

Hence, the total power delivered to output and consumed by PA1 can be expressed easily as in (3.42) and (3.43).

$$P_{RF} = \frac{{V_o}^2}{2R_0} \tag{3.42}$$

$$P_{DC} = I_{DC}V_{DC} = I_{DC}V_{DD} = (\frac{2}{\pi})(\alpha V_{DD}\frac{V_0}{R_0}) \tag{3.43}$$

Then the instantaneous efficiency at low power levels below the transition point can be found as in (3.44).

$$\eta_{BelowT.P.} = \frac{P_{RF}}{P_{DC}} = \frac{\pi}{4\alpha}\frac{V_0}{V_{DD}} \tag{3.44}$$

Since the peak output voltage of the system is $V_{0,PEP}=V_{DD}$, as found before, and by remembering the voltage wise back-off factor which was called as k, the instantaneous efficiency can be rearranged as in (3.45).

$$\eta_{BelowT.P.} = \frac{\pi}{4\alpha}\frac{V_0}{V_{0,PEP}} = \frac{\pi}{4k}\frac{1}{\alpha} \tag{3.45}$$

In conclusion, in the region below the transition point, instantaneous efficiency of DPA has in the form of class-B PA but it is higher by the value of power division ratio at PEP, α. This result shows one of the major advantageous of DPA in low drive levels clearly.

Finally, similar characteristics should be investigated in **medium power** range beyond the transition point where PA1 is in saturation region and PA2 acts as a linear current source. In this region since PA1 is saturated, i_3 is constant. The relationship between impedances can be remembered once more as in (3.46).

$$R_1 = R_3 = Z_0 = \frac{R_0}{\alpha} \tag{3.46}$$

In order to express i_2 and i_3 in terms of known supply voltage V_{DD} and output load impedance R_0, the identities of (3.47) and (3.48) can be followed by using the power conservation across transformer.

$${i_3}^2 R_3 = {i_1}^2 R_1 = \frac{{V_{DD}}^2}{{R_1}^2}R_1 = \frac{{V_{DD}}^2}{R_1} \tag{3.47}$$

$$i_3 = \frac{V_{DD}}{\sqrt{R_1 R_3}} = \frac{V_{DD}}{Z_0} = \frac{R_0}{Z_0}\frac{V_{DD}}{R_0} = \alpha\frac{V_{DD}}{R_0} \tag{3.48}$$

The output current distributed by PA2 is then stated as in (3.49).

$$i_2 = i_0 - i_3 = \frac{V_0}{R_0} - \alpha\frac{V_{DD}}{R_0} \tag{3.49}$$

Actual current delivered by PA1, i_1, can be calculated as in (3.51) by using the voltage transformation ratio of (3.50).

$$\mathrm{T} = \frac{V_1}{V_3} = \frac{V_{DD}}{V_0} \tag{3.50}$$

$$i_1 = \frac{i_3}{\mathrm{T}} = \alpha \frac{V_{DD}}{R_0} \frac{V_0}{V_{DD}} = \alpha \frac{V_0}{R_0} \tag{3.51}$$

Consequently, total DC current consumed by PA1 and PA2 can easily be expressed as in (3.52).

$$I_{DC} = I_{1,DC} + I_{2,DC} = \frac{2}{\pi}(i_1 + i_2) = \frac{2}{\pi} \frac{(1+\alpha)V_0 - \alpha V_{DD}}{R_0} \tag{3.52}.$$

Thus DC power consumption and delivered RF output power and hence the instantaneous efficiency of the system above transition point can be expressed as in (3.53)-(3.55).

$$P_{RF} = \frac{{V_0}^2}{2R_0} \tag{3.53}$$

$$P_{DC} = I_{DC} V_{DD} = \frac{2}{\pi} \frac{\left[(1+\alpha)V_0 - \alpha V_{DD}\right] V_{DD}}{R_0} \tag{3.54}$$

$$\eta_{AboveT.P.} = \frac{P_{RF}}{P_{DC}} = \frac{\pi}{4} \frac{{V_0}^2}{{V_{DD}}^2} \frac{1}{\left[(1+\alpha)V_0 / V_{DD} - \alpha\right]} \tag{3.55}$$

To check the derivation, one can evaluate this value for PEP level, where $V_{0,PEP}=V_{DD}$ so efficiency is $\eta=\pi/4$ as found before for PEP. All evaluated instantaneous efficiency values for PEP level, level below transition point and above transition point can be used to draw the efficiency graph of the DPA. Note that at the transition point, output voltage reaches to $V_0=\alpha \cdot V_{DD}$ and at PEP level it reaches to $V_0=V_{DD}$. As a nature of linear class-B amplifier, output voltage is directly proportional to the input driving voltage. Making analogy to normalized input drive voltage level or voltage wise PBO coefficient, k, it can be redefined as in (3.56).

$$k = \frac{V_{IN}}{V_{IN,PEP}} = \frac{V_0}{V_{0,PEP}} = \frac{V_0}{V_{DD}} \tag{3.56}$$

Now, the instantaneous efficiency characteristics given above can be rearranged in terms of k as given in (3.57).

$$\begin{Bmatrix} \eta_{BelowT.P.} = \dfrac{P_{RF}}{P_{DC}} = \dfrac{\pi}{4\alpha} k & k \le \alpha \\ \eta_{AboveT.P.} = \dfrac{P_{RF}}{P_{DC}} = \dfrac{\pi}{4} k^2 \dfrac{1}{\left[(1+\alpha)k - \alpha\right]} & 1 \ge k \ge \alpha \\ \eta_{PEP} = \dfrac{P_{RF}}{P_{DC}} = \dfrac{\pi}{4} & k = 1 \end{Bmatrix} \tag{3.57}$$

These findings are plotted in Figure 3.6 for different transition points of α. As mentioned before, the transition point, α, is also called as power division ratios of two PAs at PEP.

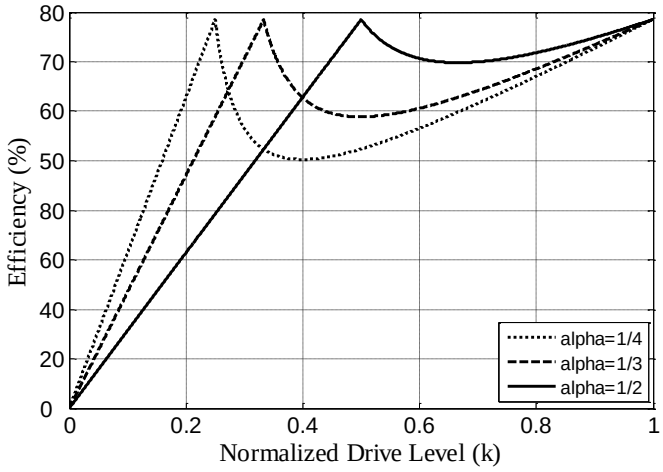


Figure 3.6 Efficiency Characteristics of DPA for Different Values of (alpha) α

Analysis followed up to now gives some other important results related to design parameters. First of all, the characteristic impedance of λ/4 transmission line used after PA1 was found in terms of output load resistance for appropriate operation of DPA as in (3.58).

$$Z_0 = \frac{R_0}{\alpha} \tag{3.58}$$

The impedance seen by each amplifier is changed in different portion of operation scale with respect to input driving envelope amplitude. These values can be stated as in (3.59) for the region below transition point, (3.60) for the region above transition point and (3.61) for peak power point.

$$R_3 = R_0,\ R_1 = \frac{{Z_0}^2}{R_3} = \frac{R_0}{\alpha^2} \tag{3.59}$$

$$R_1 = \frac{R_0}{\alpha^2} \tag{3.60}$$

$$R_3 = \frac{R_0}{\alpha},\ R_2 = \frac{R_0}{1-\alpha},\ R_1 = \frac{{Z_0}^2}{R_3} = \frac{R_0}{\alpha} \tag{3.61}$$

Similar conclusion can be hold for multi-stage DPA. As an example, for 3-stage DPA given in Figure 3.8, characteristic impedances of that configuration can be concluded as given in (3.62).

$$Z_{0,1} = \frac{R_0}{\alpha_1\alpha_2},\ Z_{0,2} = \frac{R_0}{\alpha_2} \tag{3.62}$$

The voltage and current forms of individual PAs in two-stage configuration can be drawn upon the analysis above. These graphs are given in Figure 3.7 over the operation range.

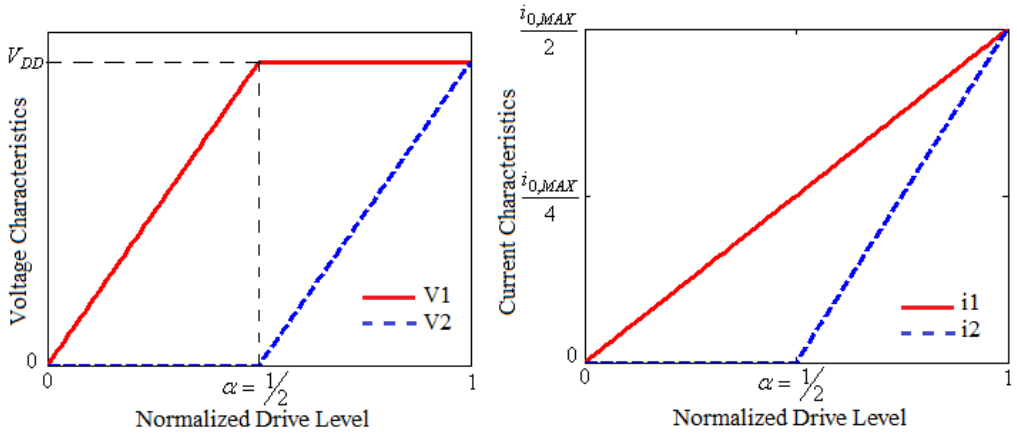


Figure 3.7 Voltage and Current Characteristic of PAs in DPA Configuration

3.3 Multi-way Doherty Power Amplifier Configuration

As mentioned, asymmetrical DPAs where transition point, α, is set below 0.5 can be used to widen the load modulation region. However, the efficiency drops between transition point and PEP point. Similar analysis can be hold for multi-stage DPA. Multi-stage DPA may be useful for different kind of modulation schemes. 3-stage example of DPA is shown in Figure 3.8. Operational regions can be separated over four ranges with respect to set transition points, α1, α_2 and input drive voltage level, k, similar to three ranges of 2-stage DPA. Table 2.1 shows these ranges with respect to drive level and the states of each amplifier over these ranges. Here, input voltage ratios can be given as (3.63) for "Low-Power" region, (3.64) for "Medium-Power", (3.65) for "High-Power" and (3.66) for "Full-Power" point.

$$\frac{v_{IN}}{v_{IN,MAX}} < \alpha_1 \tag{3.63}$$

$$\alpha_1 < \frac{v_{IN}}{v_{IN,MAX}} < \alpha_2 \tag{3.64}$$

$$\alpha_2 < \frac{v_{IN}}{v_{IN,MAX}} \tag{3.65}$$

$$v_{IN} = v_{IN,MAX} \tag{3.66}$$

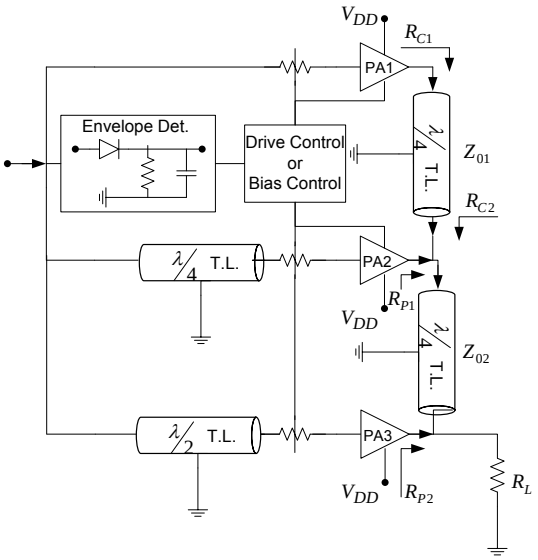


Figure 3.8 Three-Stages DPA Configuration

Table 3.1 Amplifier's Operation for 3-Stage DPA

Operation Region	**First Amplifier**	**Second Amplifier**	**Third Amplifier**
Low-Power	Linear Current Source	Shut-off	Shut-off
Medium-Power	Saturated	Linear Current Source	Shut-off
High-Power	Saturated	Saturated	Linear Current Source
Full-Power	Saturated	Saturated	Saturated

Normalized efficiency characteristics with respect to normalized input voltage drive level or voltage wise PBO constant, k, can be expressed as given in (3.67) [6], [12].

$$\left\{\begin{array}{ll} \eta_{Below,T.P.1} = \dfrac{\pi}{4}\dfrac{\pi}{4}\dfrac{k}{\alpha_1} & 0 \le k \le \alpha_1 \\ \eta_{Above,T.P.1,BelowT.P.2} = \dfrac{\pi}{4}k^2\dfrac{1}{\alpha_1 k + \alpha_2 k - \alpha_1\alpha_2} & \alpha_1 \le k \le \alpha_2 \\ \eta_{AboveT.P.2} = \dfrac{\pi}{4}k^2\dfrac{1}{k + \alpha_2 k - \alpha_2} & \alpha_2 \le k \le 1 \end{array}\right\} \quad (3.67)$$

The efficiency characteristic of 3-stages DPA is given in Figure 3.9 for first transition point α_1=0.4 and second transition point α_2=0.6 as an example.

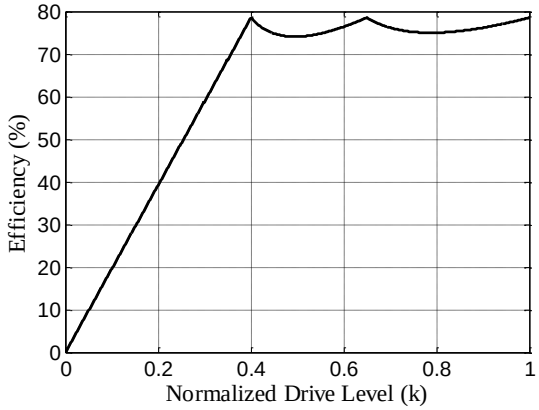


Figure 3.9 Efficiency Characteristic of 3-Stages DPA with α_1=0.4 and α_2=0.6

Alternatively, multi-stage DPA can be used to extend back-off level without drastic drop in efficiency characteristic. The output impedance and the characteristic impedance of the λ/4 line transformer are most critical points in design issue. The characteristic impedances of the transformers, Z_{0i}, depend on the back-off level and the number of stages used. The relation between them can be illustrated as in (3.68) [11], [53].

$$Z_{0i} = R_L \prod_{j=1}^{i} \gamma_j \,,\ \prod_{j=k}^{\frac{i+k}{2}} \gamma_{(2j-k)} = 10^{\frac{B_i}{20}} \tag{3.68}$$

In order to simplify the calculations, 3-stage DPA can be taken into consideration with the equation set of (3.69)-(3.72).

$$Z_{01} = \gamma_1 R_L \tag{3.69}$$

$$Z_{02} = \gamma_1 \gamma_2 R_L \tag{3.70}$$

$$\gamma_1 = 10^{\frac{B_i}{20}} \tag{3.71}$$

$$\gamma_2 = 10^{\frac{B_2}{20}} \tag{3.72}$$

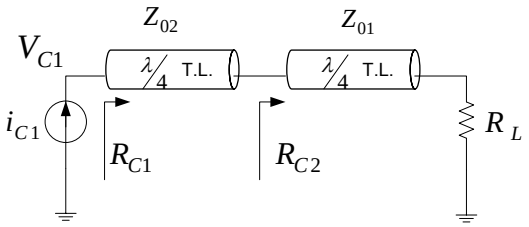
In these terms, B_i's are the transition points in terms of power back-off levels. Let's assume that it is desired transition points at 6 and 12 dB back-off levels, i.e., B_1=6 and B_2=12 so, γ_1=2 and γ_2=4. Then, the characteristic impedances takes the form of $Z_{01}=2R_L$ and $Z_{02}=8R_l$. In order to investigate the operational mechanism of 3-stages DPA in three distinct regions namely; Low Power Region, Medium Power Region and High Power Region, the equivalent circuit of 3-stages DPA referred to Figure 3.8 shown in Figure 3.10 can be analyzed.

In **Lower Power** region, representing the region lower than transition point 2, the PPA1 and PPA2 are in off states. Hence, the impedances satisfy the equalities in (3.73) and (3.74).

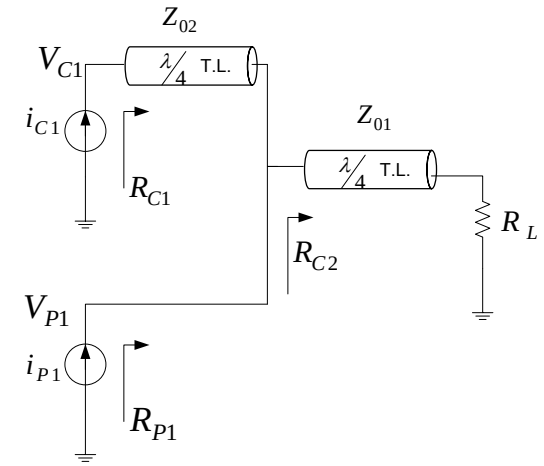
$$R_{C2} = \frac{{Z_{01}}^2}{R_L} = \frac{{\gamma_1}^2}{R_L} = 4R_L \tag{3.73}$$

$$R_{C1} = \frac{{Z_{02}}^2}{R_{C2}} = {\gamma_2}^2 R_L = 16R_L \tag{3.74}$$

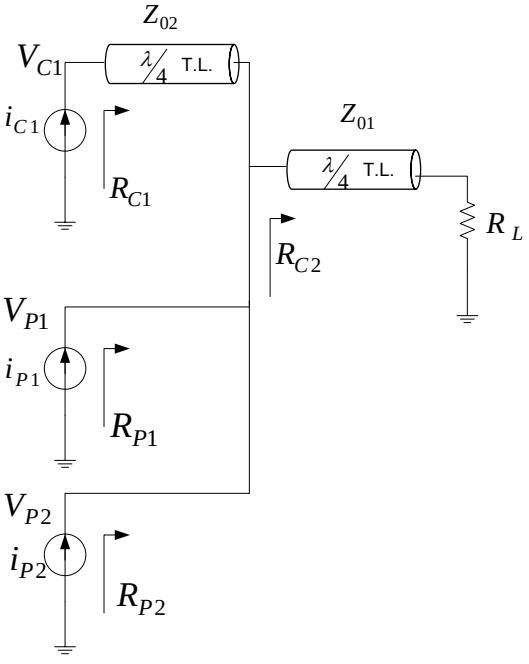
The power distributed in low power region can be stated as in (3.75) which is 1/16 of maximum power of the three-stage DPA given in (3.76).



(a)



(b)



(c)

Figure 3.10 Equivalent Circuit of 3-Stages DPA in a-) Low Power Region b-) Medium Power Region c-) High Power Region

$$P_L = \frac{{V_{DD}}^2}{2R_{C1}} = \frac{{V_{DD}}^2}{2{\gamma_2}^2 R_L} = \frac{{V_{DD}}^2}{32R_L} \tag{3.75}$$

$$P_{L,MAX} = \frac{{V_{DD}}^2}{2R_L} \tag{3.76}$$

In **Medium Power** region, region between transition point 1 and transition point 2, the MPA (CPA) is saturated, the PPA1 is in active state and the PPA2 is in off state. Using the power conservation principle, the following relations of (3.77)-(3.79) can be derived.

$$R_{C1} = \frac{\gamma_1 \gamma_2 R_L}{a_1} \tag{3.77}$$

$$R_{P1} = \frac{a_1 \gamma_1 \gamma_2}{a_1 \gamma_2 - \gamma_1} R_L \tag{3.78}$$

$$a_1 = \frac{V_{P1}}{V_{C1}} = \begin{bmatrix} \gamma_1 / \gamma_2 & @T.P.2 \\ 1 & @T.P.1 \end{bmatrix} \tag{3.79}$$

Inserting the γ_1=2 and γ_2=4 values; the impedance of MPA and the total power delivered is found as in (3.80) and (3.81) which is ¼ of $P_{L,MAX}$.

$$\begin{Bmatrix} R_{C1} = 16R_L @T.P.2 \\ 8R_L @T.P.1 \end{Bmatrix} \tag{3.80}$$

$$P_L = \frac{{V_{DD}}^2}{16R_L} + \frac{{V_{DD}}^2}{16R_L} = \frac{{V_{DD}}^2}{8R_L} \tag{3.81}$$

Similarly, in high power region, the region above transition point 1, the MPA and PPA1 are saturated and the PPA2 is active. The impedance equations of (3.82)-(3.85) are hold for this region.

$$R_{C1} = \gamma_1 \gamma_2 R_L = 8R_L \tag{3.82}$$

$$R_{P1} = \frac{\gamma_1 \gamma_2}{a_2 \gamma_2 - 1} R_L = \begin{matrix} 8R_L @T.P.1 \\ 8/3 R_L @PEP \end{matrix} \tag{3.83}$$

$$R_{P2} = \frac{a_2 \gamma_1}{a_2 \gamma_1 - 1} R_L = 2R_L @PEP \tag{3.84}$$

$$a_2 = \frac{V_{P2}}{V_{P1}} = \begin{bmatrix} 1/\gamma_1 & @T.P.1 \\ 1 & @PEP \end{bmatrix} \tag{3.85}$$

Note that, at PEP level, the MPA, PPA1 and PPA2 distribute the power of (3.86), (3.87) and (3.88) respectively.

$$P_{L,MAX}/8 \tag{3.86}$$

$$3P_{L,MAX}/8 \tag{3.87}$$

$$P_{L,MAX}/2 \tag{3.88}$$

After shifting required characteristic impedances as above, the load impedance R_L can be chosen related to optimum impedance of PPA2 as represented in (3.89) because the PPA2 gives the highest power relatively.

$$R_L = \frac{\gamma_1 - 1}{\gamma_1} R_{OPT,PPA2} \tag{3.89}$$

Similarly, the efficiency characteristics in three distinct regions as well as the PEP point can be calculated as in (3.90) based on the characteristic impedances derived and power conservation criteria. In these representations the back-off level, k, is defined as given in (3.91).

$$\begin{cases} \eta = \frac{\pi}{4}\gamma_2 \frac{V_0}{V_{DD}} & 0 \le V_0 \le \frac{V_{DD}}{\gamma_2} \\ \eta = \frac{\pi}{4} \frac{\gamma_1\gamma_2 (\frac{V_0}{V_{DD}})^2}{\left[(\gamma_1+\gamma_2)(\frac{V_0}{V_{DD}}) - 1\right]} & \frac{V_{DD}}{\gamma_2} \le V_0 \le \frac{V_{DD}}{\gamma_1} \\ \eta = \frac{\pi}{4} \frac{\gamma_1 (\frac{V_0}{V_{DD}})^2}{\left[(\gamma_1+1)(\frac{V_0}{V_{DD}}) - 1\right]} & \frac{V_{DD}}{\gamma_1} \le V_0 \le V_{DD} \\ \eta = \frac{\pi}{4} & V_0 = V_{DD} \end{cases} \tag{3.90}$$

$$k = \frac{V_0}{V_{DD}} \tag{3.91}$$

Note that at the transition point 2, TP2, and transition point 1, TP1, the equalities of (3.92) and (3.93) hold respectively.

$$V_0 = \frac{V_{DD}}{\gamma_2} = \frac{V_{DD}}{4},\ \eta = \frac{\pi}{4} \tag{3.92}$$

$$V_0 = \frac{V_{DD}}{\gamma_1},\ \eta = \frac{\pi}{4} \frac{\gamma_1\gamma_2\gamma_1^{-2}}{(\gamma_1+\gamma_2)\gamma_1 - 1} \tag{3.93}$$

3.4 Distributed and Inverted Doherty Power Amplifier Configurations

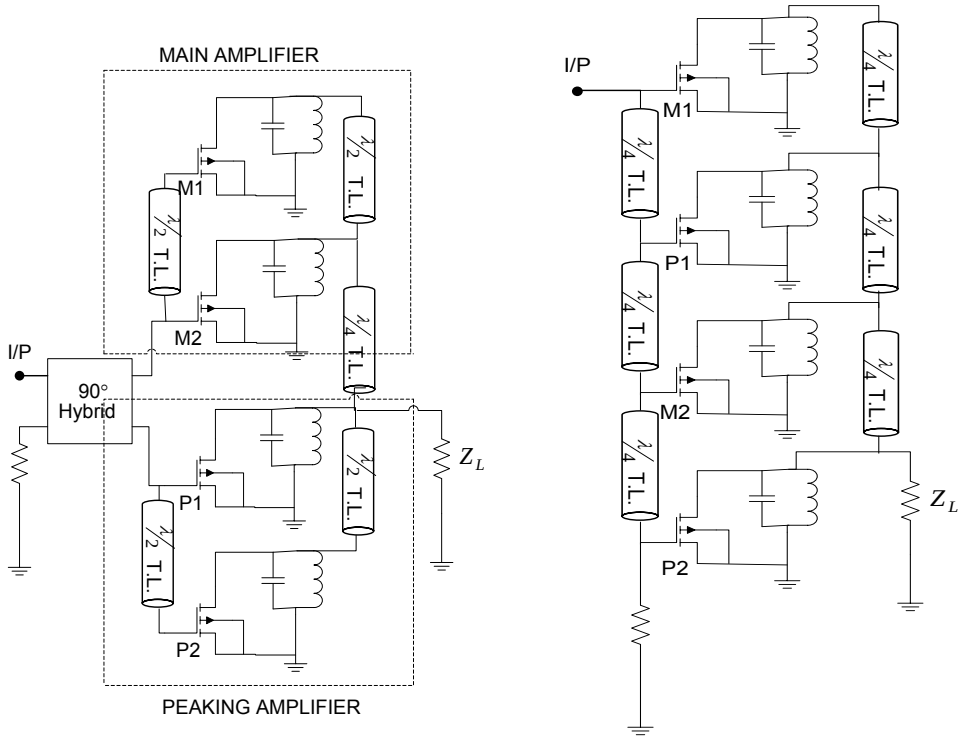
Distributed amplifier concept can be applied to DPA with using more than one MPAs and PPAs as shown in Figure 3.11(a) If PPAs are distributed between CPAs, this new configuration takes the name of Inverted DPA (IDPA) [54], whose size is smaller than conventional DPA. An example of IDPA with using two MPAs and two PPAs is shown in Figure 3.11 (b). The equivalent circuit of 4-FETs IDPA can be deduced as in Figure 3.12, by modeling the output of each PA as a current source. Using ABCD parameters and the superposition principle over current sources, the output voltages of each amplifier; V_1, V_2, V_3, V_4 can be expressed in terms of the output currents of each amplifier; I_1, I_2, I_3, I_4, as given in (3.94)-(3.97).

$$V_1 = \frac{Z_{01}^{\ 2} Z_{03}^{\ 2}}{Z_{02}^{\ 2} Z_L} I_1 - jZ_{01} I_2 - \frac{Z_{03}^{\ 2} Z_{01}}{Z_{02} Z_L} I_3 + J \frac{Z_{01} Z_{03}}{Z_{02}} I_4 \tag{3.94}$$

$$V_2 = -jZ_{01} I_1 \tag{3.95}$$

$$V_3 = -\frac{Z_{01} Z_{03}^{\ 2}}{Z_{02} Z_L} I_1 + \frac{Z_{03}^{\ 2}}{Z_L} I_3 - jZ_{03} I_4 \tag{3.96}$$

$$V_4 = j\left(\frac{Z_{01} Z_{03}}{Z_{02}} I_1 - Z_{03} I_3\right) \tag{3.97}$$



(a) (b)

Figure 3.11 Other DPA Configurations; (a) Distributed DPA, (b) Inverted DPA

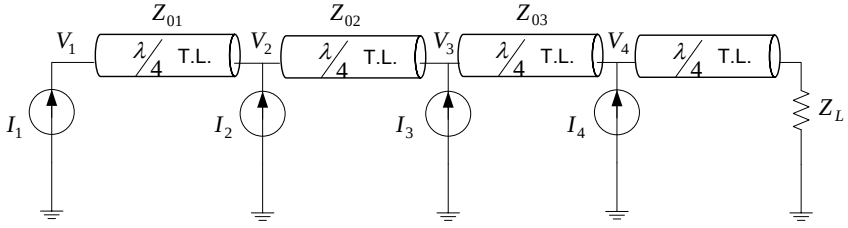


Figure 3.12 Equivalent Circuit of Inverted DPA

These expressions show that first MPA (CPA), M1 is load modulated by both PPAs while M2 is load modulated by only P2. Moreover, output voltage V_4 is directly proportional to M1 which is class-B biased linear PA hence the IDPA is also linear. Although IDPA is good candidate for smaller size realization of DPA, PAs in this configuration are more sensitive to non-ideal transistor characteristics and parasitic.

3.5 Practical Issues in Designing Doherty Power Amplifier

Since the ideal class-B/class-B DPA requires controlled nonlinear attenuator, the different topologies have been proposed and implemented in the literature. The carrier PA (CPA) is biased in class-AB scheme to achieve high enough gain at the design frequencies where peaking PA (PPA) is biased in class-B or class-C for high efficiency consideration. Class-C biased PPA does not require an extra control circuit for proper operation. However, in this case, breakdown problem can arise for deep class-C devices and maximum output voltage swing cannot be achieved so the total power is reduced. In practice class-B circuit is used for peaking PA. Control circuit on gate biasing can be used to achieve better performance, however even without any control circuit, class-B biased peaking PA gives a valuable enhancement on PAE at PBO. Drain current swing of class-B biased peaking PA can reach the same value of that of class-AB biased CPA at PEP and at low drive levels, its drain current is so small comparably to PPA because of low transconductance of the drain current source near pinch-off [55]. The power range over load modulation region depends on the power distribution ratio of CPA and PPA at PEP. As investigated, theoretical efficiency values of classical DPA can be stated as; 78.4% at PEP and at the transition point, minimum 70% at the middle of load modulation region. For an asymmetrical DPA, the transition point is shifted below 6 dB PBO point with significant efficiency degradation in load modulation region. On the other hand, using multi stage DPA, it is possible to maintain flatter efficiency characteristic over wider power back-off range. However, in this case, circuit complexity grows. Although optimum configuration is based on the driving signal modulation scheme, classical DPA consisting of 2 stages is usually accepted as a most appropriate one. Usually in practice, asymmetric input power divider or peaking device are used to compensate class-C biased PPA. Alternatively, characteristic impedance or the length of the transformer can be adjusted to achieve same amount of power from both PAs at PEP. Similarly, phase compression experienced by class-AB and –C circuits are not same and the length of input transformer on the PPA side can be adjusted to solve this problem. Moreover, one segment of transmission line is used in front of the PPA to ensure high impedance at off state. Splitter asymmetry, A, for proper operation of DPA with class-C biased PPA can be defined as in (3.98) where G1and $G_2$are the power gains of the CPA and PPA respectively. The overall gain of DPA can be deduced as in (3.99) [56].

$$A = G_1 - G_2 \tag{3.98}$$

$$G_{DPA} = 3 + G_1 - 10\log(1 + 10^{\lambda/10}) \tag{3.99}.$$

Although the class-B biased PPA with biasing control circuitry seems to be best to obtain maximum output power, maximum PAE over wide input range, alternative to class-B PPA and control circuitry, in order to reduce the complexity of the system, class-C biased PPA can be used without any requirement of control circuitry. However, in this case, evaluated norms such as power, PAE and PBO range with high efficiency are changed. Moreover, even and odd harmonics should be filtered out for proper operation. If PPA is biased to class-C, its conduction angle becomes an important parameter for calculation of DPA performance [9]. Maximum conduction angle depends on α value set by designer as in (3.100).

$$\theta_{MAX} = 2\cos^{-1}(\alpha) \tag{3.100}$$

The maximum PAE offered by DPA also depends on conduction angle. For instance, 82.1% PAE can be achieved for α=0.4 maximally for DPA. The main disadvantage of using class-C DPA is preventing it from delivering its maximum power at PEP and hence modulating the load of CPA without full sense. Analyzes show that, the 62% of full power can be achieved by setting α=0.2. As mentioned, using an asymmetrical input power divider can solve this problem, however one other

effective solution is using two unequal periphery transistors in the CPA and PPA devices. If class-C biasing scheme is chosen for PPA, choice of $\alpha<1/2$ is more meaningful [57]. If $\alpha = 1/3$is chosen, the impedance seen by CPA $R_1=3R_{opt}$ at transition point and $R_1<R_{opt}$ at PEP, where R_{opt} is optimum load desired by CPA for full power. In this configuration, class-C circuit is biased more near to pinch-off than that used in standard configuration with $\alpha = 0.5$. Since the load of CPA is not modulated by the PPA in a full sense, the power delivered by the PPA is higher than that of CPA at PEP. This configuration has two main advantages over standard scheme; it provides high efficiency at wider input power range and since PPA is biased more near to pinch-off, gate breakdown phenomena is avoided. In order to achieve higher efficiencies with respect to classical DPA, class-F like saturated PAs including harmonic control circuit can be used [58]. However, with this kind of matching circuit, it is very hard to satisfy the fundamental, second and third harmonic impedances simultaneously. Hence, the peak power, efficiency and acceptable linearity are not achieved in this structure because of the improper load modulation and harmonic cancellation between the carrier and peaking amplifiers. Class-F operation includes the half sinusoidal current form and square voltage wave form. These wave forms can be created by realizing zero impedance at even harmonics and infinite impedance at odd harmonics and vice versa for inverse class-F amplifier. Since both PAs are saturated type, DPA with class-F CPA has poorer linearity characteristic than conventional DPA. However, due to the harmonic cancellation mechanism of two amplifiers at appropriate gate biasing in DPA configuration, its linearity is better than conventional switching PAs like class-F.

Although DPA is appropriate for high efficiency linear amplification in ideal 50 Ω load situation; it is very sensitive to load mismatch effects. Its linearity and efficiency are seriously affected by mismatched loads. System level load mismatch compensator scheme can be applied to recover linearity and maintain PAE at maximum range. Load mismatch analysis on DPA shows that, output power, PAE and linearity are seriously affected by the amplitude of load reflection coefficient [59]. However, in small range of phase of load reflection coefficient, these characteristics remain constant over different load reflection amplitudes. Hence, to compensate load mismatches, system level compensator operating based on the controlling of phase of the load reflection coefficient can be applied.

Load pull measurement technique is the most precise method to extract non-linear behavior of a transistor as a function of source and load impedances at a specified bias point, V_{GS} and V_{DD}. Design procedure offered by reference [59] can be stated as follows;

1- Design class-AB CPA and class-C PPA as initial designs,
2- Insert designed PAs to Doherty combining network,
3- Adjust two PAs output matching networks or characteristic impedance of combining network (output transformer) to optimize the load impedance seen by both transistors at PEP which are equal in theory,
4- Adjust the length of input transformer to compensate phase between two lines,
5- Adjust the length of output transformer to realize active load modulation at the output of CPA,
6- If load impedance moves along optimal line, procedure can be finalized, if not, the procedure should be initialized from step 2.

3.5.1 Gain and Linearity

The mobile phone system is moving onto the 3G (3rd Generation), 3.5G and 4G systems using WCDMA (Wideband Code Division Multiple Access) signals and OFDM signals respectively. These systems require high linearity in the base station transmitters due to the nearly 10 dB PAPR. For instance, UMTS-LTE (Universal Mobile Telecommunication System-Long Term Evaluation) using high efficient signals offers superior user experience and simplified technology but has PAPR up to 12 dB [60]. In low power region, linearity is entirely determined by CPA, so it should be highly linear even though the load impedance is high. Linearity in high power region (load modulation region) is dependent on the harmonic cancellation degree from two amplifiers using appropriate gate biases. The gain characteristic can be linearized by compensating the saturation response of CPA by turning PPA to on state slightly after the transition point. As the gain of CPA compresses, IMD_3 level due to CPA increases whereas the phase of related IMD_3 decreases. In

contrast, since the gain of PPA expands in high power region, both the amplitude and the phase of related IMD_3 from PPA increases. Thus, to cancel out the IMD_3 from two PAs, the IMD_3 components must be 180 degree out of phase and with the same amplitudes. The bias voltages of both PAs are optimized during simulations and experimental validations for better cancellation of harmonics or IMD_3 generated by PPA and CPA with the slight degradation in efficiency characteristic [61], [62]. PPA should have lower impedance due to its lower bias point to enhance IMD_3 cancellation. Further improvement on linearity can be accomplished by using asymmetrical drain voltages for CPA and PPA. Usage of different drain voltages widens the load modulation region as well which can be accomplished with using lower transition point in classical scheme. Drain voltages should be chosen in a favor of PPA and the related output matching circuits should be optimized with respect to the drain voltages [63]. In classical class-AB/C DPA scheme, linearity is obtained with compensating the gain compression of class-AB CPA by late gain expansion of class-C PPA [64].

Two-tone test for IMD specifications and ACLR (Adjacent Channel Leakage Ratio) can be measured for linearity specification. ACLR is calculated usually with 5 or 10 MHz offsets and for either 1-carrier WCDMA or 2-carrier WCDMA. The ACLR can be calculated as [60]; ACLR= {Total Power in Specified BW at Specified Offset to Center Frequency}-{Total Power in Specified BW at Center Frequency}. In order to improve the linearity of DPA, DPD (Digital Pre-Distortion) can easily be adopted. Usage of on shell chip devices prior to DPA provides up to 20 dB correction in IMD_3 or ACLR levels [65].

3.5.2 Efficiency

In order to have maximum PAE, transition point is decided with respect to the modulation scheme applied and for the signals whose PAPR is greater, the transition point (TP) is set at low levels than the conventional one which is at 6 dB PBO from maximum power. Alternatively, an approach of optimizing average efficiency instead of PAE can be chosen. Lowering the bias voltage of PPA enhance the efficiency of DPA structure but degrades linearity [66]. Efficiency characteristic of ideal DPA scheme can only be improved further by increasing the individual efficiencies of two amplifiers. Class-F or Inverse class-F CPA strategy can be used for this purpose. Theoretical improvement with respect to class-AB/C standard DPA configuration can be achieved for the efficiency providing the proper output harmonic loading condition. In this configuration, fundamental output voltage is increased up to 10-20% and impedance seen by CPA is increased as well. Although it offers higher output power and efficiency, gain is degraded compared to standard DPA configuration due to required higher input divider dividing ratio [67], [68], [69]. Efficiency of DPA can be optimized by the adaptation of harmonically tuned load. Tuned load configuration for both PAs offer short circuit loading condition for the impedances at harmonic frequencies [70].

3.5.3 Offset Lines

Optimization on efficiency and linearity trade-off can be accomplished with using proper length offset lines whose characteristic impedances are determined with respect to high power conditions [61]. These offset lines are used to obtain optimized efficiency from CPA and to represent high output impedance from PPA at low power levels below transition point. At low power region, the off state output impedance of PPA is very low resistive and highly capacitive. It can be carried to a high resistive value nearly open by using a length of offset line after its matching circuitry and low power leakage from CPA can be reduced to a negligible value. Length of offset line is optimized by observing the angle of reflection coefficient taken from combination point to PAs [71]. Similarly, offset line usage provide CPA by proper load impedances to deliver maximum power at high efficiency [64]. Usage of offset line for CPA provides the phase matching to ensure that a resistive load of twice the nominal value is presented to the transistor of CPA [56]. Inverted Doherty Power Amplifiers (IDPAs) use these kind of offset lines only and they do not require any $\lambda/4$ length transmission line transformer. The DPA having output reflection coefficient with negative phase can be implemented in a more compact size with respect to conventional DPA [72].

One of the critical elements of DPA is impedance inverter network having the property of transforming the output voltage at one pair of terminals into a definite coexisting current at the other pair regardless of terminating impedance. In classical DPA configuration, simple λ/4 transmission line is used for this purpose [73], [74].

Low off impedance of PPA in low power region due to high parasitic can be got over employing DPA with push-pull configuration. In Push-pull configuration off state impedance of PPA in low power region is desired to be low contrary to classical DPA configuration. It has the advantages of removed λ/4 length transformer and additional offsets line which is nearly half wavelength long most of the time. Moreover bal-un type transformer enables easy matching with its practical implementation in 4:1 or 9:1 impedance ratios [75].

3.5.4 Gallium Nitride (GaN) Transistors

Gallium nitride (GaN) transistors are well suited to design and implement a DPA due to their low parasitic output capacitance which provide broadband characteristic to the transistors [76]. GaN transistors have high current density, high breakdown voltage, higher power operation capability with high efficiency and reduced R_{DS} and C_{DS} parasitic values [77]. Moreover, today's GaN transistors are well modeled in a large signal scheme. Since DPA has a number of variables, practical uneven power driving l tuning methods are very hard task to accomplish by the designers. Having an accurate large signal model provides the designer with more practical and flexible designs with confidence [78].

In GaN devices, improved analysis accounting for dynamic on-resistance is necessary. Accounting ohmic resistance, main output current of CPA is reduced while voltage swing is increased which provides enhanced efficiency and output power [70]. Dual path high power devices like push-pull package enables size and cost reduction of the realized power amplifier [66].

3.5.5 Uneven Power Drive

To prevent the complicated hardware implementation using a control circuit to control the on/off state of PPA, class-C biasing scheme for PPA is usually applied instead of class-B as used in its first implementation by W.H. Doherty in 1936 [73], [74]. This causes to result in obtaining reduced power from peak power level and load modulation of CPA cannot be hold in a full sense. Moreover, CPA is not saturated at the transition point. Usually, in practice, former problem can be overcome with using unequal periphery devices and uneven power driving for CPA and PPA. In standard class-AB/C biased DPA configuration, full power of PPA can be obtained by choosing nearly 2 times larger periphery devices (i.e. 2 times higher output power device) for PPA. Otherwise, both the linearity and power of entire system are degraded due to early saturation of CPA in weak load modulation. However, in this case only half of the power capability of PPA can be delivered to output. Instead, both uneven power divider at the input side and but different but less extreme device periphery for PPA can be applied simultaneously. For instance, 1.4:1 device periphery ratio and 2 dB coupler, in other words, 25:35W devices with 66% of power input to PPA can be applied for 6 dB PBO transition point DPA. In this scheme, the gate bias of class-C PPA should be tuned by considering the uneven power ratio [13]. With the usage of appropriate periphery devices the drain current of PPA at PEP become strictly dependent on the current of CPA with the simple formulation of (3.101) where α is voltage wise transition point [79].

$$I_{PPA} = \frac{1-\alpha}{\alpha} I_{MPA} \tag{3.101}$$

When the transition point is set lower than classical value of 1/2, the power delivered by PPA at PEP is higher than that of the CPA. However, proper size periphery is required and it has larger ratio with respect to classical scheme. For instance 3:1 scale is required for α=1/3 [17]. Drive level should be high for CPA at low power region to guarantee SAT operation of it. On the other hand, higher drive level is required for PPA in load modulation region to get maximum power from it. One other solution to get maximum power from PPA and to modulate load of CPA fully, larger

periphery device can be used in PPA. Even power drive causes lower power from PPA at PEP due to class-C biasing scheme. Moreover, since input impedance changes as input power increases, more power goes to CPA, increasing its gain so worse gain flatness at all. If uneven power drive in a favor of PPA is used, PPA become active earlier than proposed power level reducing overall efficiency at set transition point. However if uneven drive scheme as higher power to PPA and higher power to CPA at low power and high power regions respectively solve this problem. In this case, current and power delivered by PPA reaches CPA at PEP, load modulation by PPA is better for high efficiency from CPA at PEP and since CPA comes to saturation region at transition point, efficiency at transition point also increases. Moreover, since IMD_3 cancellation by high driven and proper load modulation PPA is better at high power region, linearity enhances. Overall PA provides high gain and efficiency below transition point. Uneven power drive can not be established with using regular divider, but can be established through using directional coupler or direct dividing by using high-pass circuit and phase compensation network prior to CPA [80], [81].

3.5.6 Matching and Biasing

To get highest possible power, higher linearity and wider BW from DPA uneven power drive is used in class-AB/C based DPA to open PPA fully and modulate the load of CPA properly. Matching network of both PAs should be designed appropriately to have low load impedances for higher linearity. Moreover, if class-C biased PPA is used, it should have lower impedance as the nature of low conduction angle amplifiers. Matching networks should also be optimized to enhance IMD cancellation over whole ranges. On the other hand, bias circuit is another critical part of DPA that have to be optimized to minimize memory effects. It can be satisfied by using quarter wave bias line for narrow band applications and decoupling capacitors for each frequency including operating frequencies and envelope frequencies. Bias levels should also be optimized to have higher linearity and efficiency [64].

Good way of designing matching networks is applying load pull simulations or measurements. Load pull data provides the maximum power load point and maximum efficiency load point. Matching network of PPA is designed to match 50Ω load to the maximum power load. The matching network of CPA is designed to match 50Ω load to the maximum power load and to match 100Ω to maximum efficiency load. It means that, the matching of PPA is designed to have the highest output power at PEP and the matching of CPA is designed to have the highest output power at PEP and the highest efficiency at TP [78]. Class-AB biasing scheme for CPA is typically preferred to a class B in order to reduce cross over distortion, to increase overall DPA linearity and to increase the gain level at the expense of slight degradation in efficiency [70].

Biasing circuits should be designed to minimize the memory effects. The effects of memory effect on PAs are IMD or ACLR asymmetry and BW dependent ACLR or IMD characteristics [62]. To reduce memory effects, bias circuit should not have any frequency dispersion of envelope. The load impedance should be reduced to short for envelope frequency voltage component. This can be satisfied with using tantalum capacitors at the end of quarter wave length bias line in addition to RF decoupling capacitors.

3.5.7 Parasitic and Harmonics

Theoretical operation mechanism of DPA does not take the parasitic components into account. However, unavoidable parasitic components of transistors cause two problems in operation. Firstly, output power of the CPA can leak into PPA port at low power levels. Moreover, optimum power matching impedance become complex thus maximum power cannot be delivered and ideal load modulation on CPA cannot be satisfied [64]. Higher order harmonics in the content of output voltage should be removed for proper operation. Matching circuits can be realized in low-pass type [82]. Alternatively, different length stubs can be utilized to get rid of harmonic content.

CHAPTER IV

ANALYSIS AND DESIGN OPTIMIZATIONS OF DOHERTY TOPOLOGIES

Most of the modulation schemes used in the modern wireless communication systems have RF envelopes with significant Peak-to-Average Power Ratio (PAPR). High-efficiency power amplifiers (PAs) are the key components of modern communication systems; they form the final stage of the transmitters for transmitting high output power signals. Designing an efficient PA has a vital importance especially for the mobile systems to save power and to minimize the complexity of cooling structures. Doherty power amplifier (DPA) is a promising technique for improving the efficiency under output power backed-off conditions.

The DPA is based on active load modulation and the power combining property it has. The peaking (or auxiliary) device decreases the load impedance seen by carrier device, as the driving level increases beyond the transition point (TP), which is set by the designer. At low output power levels relating to low driving level, only the carrier power amplifier (CPA) is active, and it operates as a linear amplifier due to its class-B biasing scheme. By the transformer action, it reaches to saturation at TP, which is well below output peak envelope power (PEP) of overall amplifier. In classical scheme, the TP has been set at 6 dB PBO level, which is related to half of the peak output voltage. At output voltage levels higher than this point, namely load modulation region, the CPA remains saturated and the peaking power amplifier (PPA) operates linearly. A $\lambda/4$ line in front of the CPA is used to tune out the active load resistance that is decreased dynamically by the PPA. The other $\lambda/4$ line or 3 dB/90° hybrid and extra offset lines are used to achieve in-phase power combination. In DPA, maximum efficiency is achieved at the transition point, where CPA is saturated and PPA is inactive, and at the PEP point where both PAs distribute equal power in standard configuration. The overall output power, which is the combination of power from CPA and PPA, has a linear characteristic.

The DPA has lower circuit complexity and cost effective implementation with respect to its alternatives. In W.H. Doherty's original study, the DPA was constructed on vacuum tube amplifiers [7]. The efficiency analysis of solid-state DPA in class-B/class-B configuration was reported by F. H. Raab in 1987 [8]. However, class-B/class-B realization using solid-state transistors require driving level controlled attenuator which should have a special behavior of being shaped at least in two distinct regions with highly nonlinear characteristics [4]. In an alternative usage of DPA with solid state transistors, the CPA is biased in class-B and the PPA is biased in class-C so that it turns on the transition point. However, conventional symmetrical Doherty power amplifier (SDPA) in which the CPA and PPA employ the same periphery transistors result in reduced maximum output power due to the lack of full load modulation at the maximum drive level [9]. In order to improve the performance of class-B/class-C SDPA, different techniques have been proposed and implemented. One of the most cost effective solutions is using uneven power divider in favor of the PPA [10]. Nevertheless, uneven input power division reduces the output power delivered by CPA and consequently reduces the gain at the low power levels at which only the CPA operates [11]. The multi-way Doherty structure is another method to increase the overall performance [5], [83], [84]. However, multi-way structure results in higher structural complexity and more expensive implementation.

Two of the most popular solutions proposed to improve the performance of realizable DPA are using larger periphery transistor for the class-C biased PPA section or applying a proper bias adaptation to the PPA section [12]. The former method is referred to as asymmetrical Doherty power amplifier (ADPA) and has been widely used in recent applications [13-17]. The latter one is known as bias adapted Doherty power amplifier (BA-DPA) and it is realized by using an additional control circuit to change the bias condition of the peaking device from off-state to class-B. Similar to ADPA, the BA-DPA has been widely used in recent applications and promising measurement

results have been reported [18-20]. The structures of the BA-DPA and ADPA are given in Figure 4.1 (a) and (b), respectively.

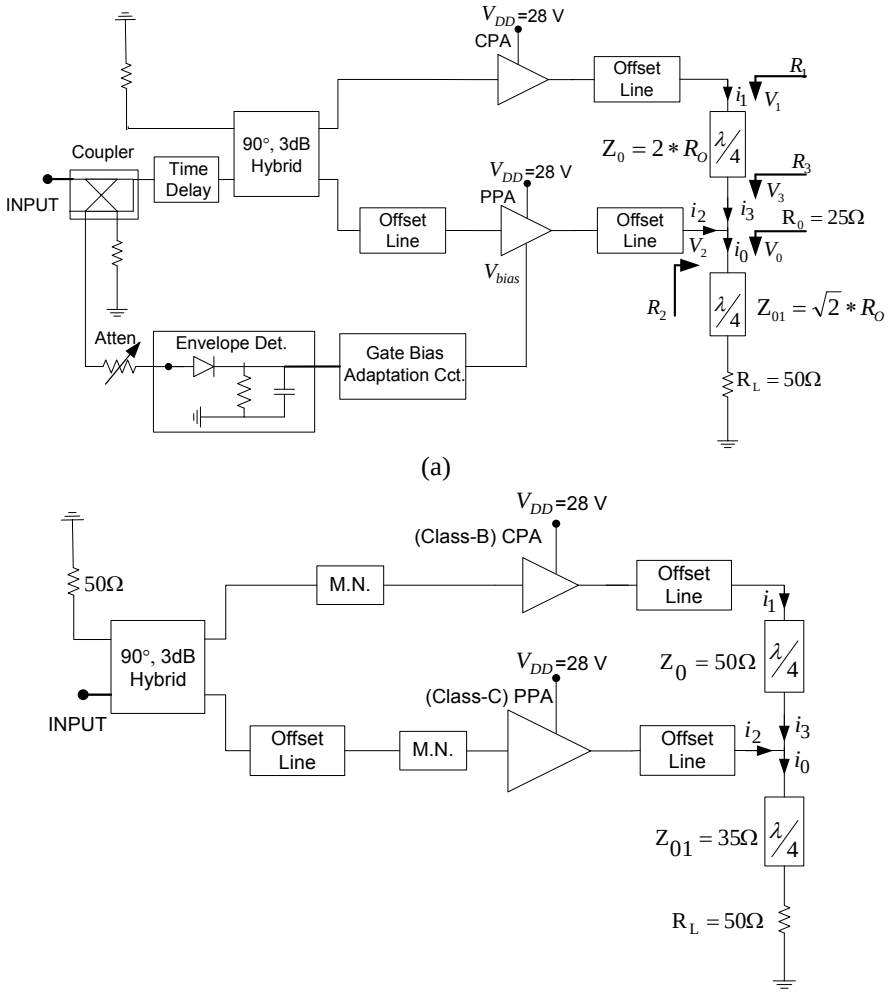


Figure 4.1 Doherty Power Amplifier Structures for 6 dB Load Modulation Region (a) Bias Adapted-DPA (BA-DPA), (b) Asymmetrical DPA (ADPA)

In this chapter, utilization of gate bias adaptation for PPA is analytically investigated and enhanced efficiency characteristic of BA-DPA in load modulation region (high power region) over ideal, class-B/class-B DPA is shown. In addition, the efficiency performance of the ADPA is investigated and the required periphery ratio of the PPA to CPA for proper Doherty operation for different load modulation regions is introduced. The improved efficiency characteristic of the ADPA for 6 dB load modulation region is illustrated. Analytically predicted achievements are verified by measured results obtained from BA-DPA and ADPA in comparison to the conventional SDPA and conventional balanced power amplifier.

Although the ADPA and BA-DPA methods have been widely researched and realized up to date, these applications differ with at least one aspect in terms of specific application frequency, power level and employed transistor technology. Therefore, to the authors' knowledge, a fair comparison between the ADPA and BA-DPA techniques has not been reported as yet. In this chapter, optimally designed ADPA with adequate maximum conduction angle and adequate periphery PPA is

compared with BA-DPA technique which was implemented at the common operation frequency, with similar output powers and by employing the same technology transistors.

4.1 Bias Adapted Doherty Power Amplifier (BA-DPA)

In the BA-DPA application, the PPA is kept on deep class-C bias with zero conduction angle up to the transition point, after which the PPA starts to conduct. After the transition point, quiescent point of the PPA is adaptively brought to class-B, identical to the CPA's biasing. On the other hand, the ADPA has a fixed class-C biased PPA. Thus, the conduction angles of the PPAs become an important parameter for efficiency performance. The presented efficiency analysis of BA-DPA is based on the conduction angle, γ. The efficiency analysis of BA-DPA is then extended to comprise ADPA case with appropriate periphery scaling conditions.

In both cases, the theoretical efficiency is identical to that of the ideal class-B/class-B DPA in the low power region. In the load modulation region where the actual Doherty operation is present, the range of normalized voltage factor, k can be defined as in (4.1), and in this region, the ideal configuration of DPA offers the efficiency as given in (4.2) [8].

$$0.5 \le k = \frac{V_O}{V_{DD}} \le 1 \tag{4.1}$$

$$\eta_{DPA} = \frac{P_{RF}}{P_{DC}} = \frac{\pi}{4} k^2 \frac{1}{\left[\frac{3}{2}k - \frac{1}{2}\right]} \tag{4.2}$$

4.1.1 Analysis and Design Optimization

In the high power region, efficiency of BA-DPA can be analyzed based on the conduction angle variation and by taking the quiescent current I_{dq} as a negative valued current for class-C amplifiers analogous to class-A/B amplifiers [30]. Its value is I_{dq}= -I'_{DD} at γ=0 (OFF-state) and I_{dq}=0 at γ=π/2 (class-B). Assuming the drain current waveform of class-C biased PPA, $i_D(t)$, is as in Figure. 4.2, the mathematical expressions of PPA's fundamental output current, i_2, DC current, $i_{2,DC}$, voltage, V_2, RF output power delivered, P_2, and DC power dissipated, $P_{2,DC}$, related to Figure 4.1(a) can be given as in (4.3)-(4.6).

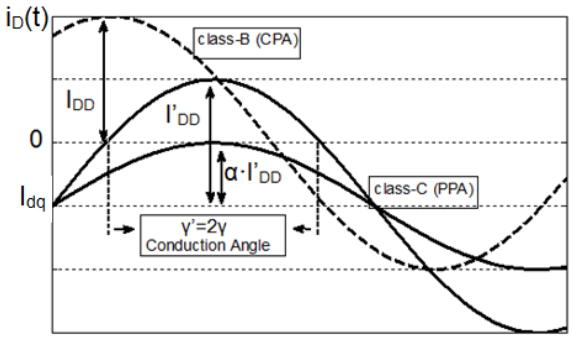


Figure 4.2 Drain Current Waveforms of CPA and PPA

$$i_{2,DC} = \frac{1}{2\pi}\int_0^{2\pi} i_D(\theta)d\theta = \frac{I'_{DD}}{\pi}\{\sin(\gamma) - \gamma\cdot\cos(\gamma)\} \tag{4.3}$$

$$|i_2| = \frac{|V_2|}{R_2} = \frac{I'_{DD}}{2\pi}\{2\cdot\gamma - \sin(2\cdot\gamma)\} \tag{4.4}$$

$$P_2 = \frac{1}{2}\cdot|V_O|\cdot|i_2| = \frac{1}{2}|V_O|\frac{I'_{DD}}{2\pi}\{2\cdot\gamma - \sin(2\cdot\gamma)\} \tag{4.5}$$

$$P_{2,DC} = V_{DD}\cdot i_{2,DC} = V_{DD}\frac{I'_{DD}}{\pi}\{\sin(\gamma) - \gamma\cdot\cos(\gamma)\} \tag{4.6}$$

To express power delivered by CPA, i_3 or i_1 and DC current can be written as in (4.9) with the aid of (4.7) and (4.8) which state the power conservation on λ/4 length transmission line and proper characteristic impedance, Z_0required for impedance transformation. Note that since the CPA is saturated in this region its output voltage is equal to supply voltage assuming rail to rail operation from the transistor and neglecting the knee voltage effect, $V_1 = V_{DD.}$

$$|i_3|^2\cdot R_3 = |i_1|^2\cdot R_1 = \frac{|V_1|^2}{R_1} = \frac{{V_{DD}}^2}{R_1} = \frac{|V_3|^2}{R_3} = \frac{|V_O|^2}{R_3} \tag{4.7}$$

$$Z_0 = \frac{R_O}{\alpha} = 2\cdot R_O \tag{4.8}$$

$$|i_3| = \frac{1}{2}\frac{V_{DD}}{R_O},\ |i_1| = \frac{1}{2}\frac{|V_O|}{R_O},\ \frac{|i_1|}{i_{1,DC}} = \frac{\pi}{2} \tag{4.9}$$

RF power and DC power of the CPA in the load modulation region can be expressed as in (4.10) and (4.11).

$$P_1 = \frac{1}{2}\cdot|V_O|\cdot|i_3| = \frac{1}{4}\frac{|V_O|\cdot V_{DD}}{R_O} \tag{4.10}$$

$$P_{1,DC} = V_{DD}\cdot i_{1,DC} = \frac{1}{\pi}\frac{|V_O|\cdot V_{DD}}{R_O} \tag{4.11}$$

Total RF output power, DC power consumption and resultant efficiency of BA-DPA in load modulation region can now be easily calculated in terms of normalized voltage factor, k, and conduction angle, $\gamma'=2\gamma$ (Radians) of the PPA as given in (4.13)-(4.15) by expressing the I'_{DD} term by (4.12). In-phase operation was assumed between the CPA and PPA as in the ideal configuration of DPA.

$$I'_{DD} = \frac{|V_O| - \frac{1}{2}V_{DD}}{R_O}\cdot\frac{2\pi}{\{2\cdot\gamma - \sin(2\cdot\gamma)\}} \tag{4.12}$$

$$P_O = P_1 + P_2 = \frac{|V_O|^2}{2\cdot R_O} \tag{4.13}$$

$$P_{DC} = P_{1,DC} + P_{2,DC} = \frac{{V_{DD}}^2}{R_O}\left[\frac{|V_O|}{2\pi V_{DD}} + 2\left\{\frac{|V_O|}{V_{DD}} - \frac{1}{2}\right\}\left\{\frac{\sin(\gamma) - \gamma\cdot\cos(\gamma)}{2\cdot\gamma - \sin(2\cdot\gamma)}\right\}\right] \tag{4.14}$$

$$\eta_{BA-DPA} = \frac{P_O}{P_{DC}} = \frac{k^2}{2\left[\frac{k}{\pi} + \{2k-1\}\left\{\frac{\sin(\gamma) - \gamma\cdot\cos(\gamma)}{2\cdot\gamma - \sin(2\cdot\gamma)}\right\}\right]} \tag{4.15}$$

Efficiency of the BA-DPA was calculated in terms of conduction angle where $0 \leq \gamma \leq \pi/2$ for transition of PPA from OFF-state to class-B biasing. However, in practice, instead of conduction angle variation, gate bias voltage, V_{gs} variation is much more useful. At this point, the relation between γ and V_{gs} can be expressed as given in (4.17) by the aid of (4.16) where K is a physical constant of the transistor related to transistor's internal parameters such as channel width and length.

$$\gamma = \cos^{-1}\left(\frac{I_{dq}}{I_{DD}}\right) \tag{4.16}$$

$$\gamma = \cos^{-1}\left(\left|\frac{-K(V_{gs}-V_{TH})^2}{I_{DD}}\right|\right) \tag{4.17}$$

Two basic adaptation schemes were investigated in this study, but many other schemes can be proposed and examined using the efficiency equation given as (4.15). In the first case, efficiency characteristic with linearly changing V_{gs} and in the second case the efficiency characteristic with linearly changing conduction angle are observed. The efficiency characteristics in load modulation regions for ideal DPA and BA-DPAs deduced from (4.15) are given in Figure 4.3. Analysis and theoretical plots show that BA-DPA offers higher efficiency characteristic in load modulation region with a shallower dip compared to the ideal DPA.

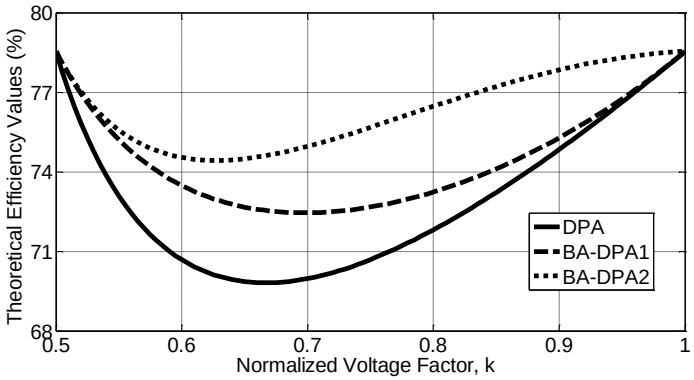


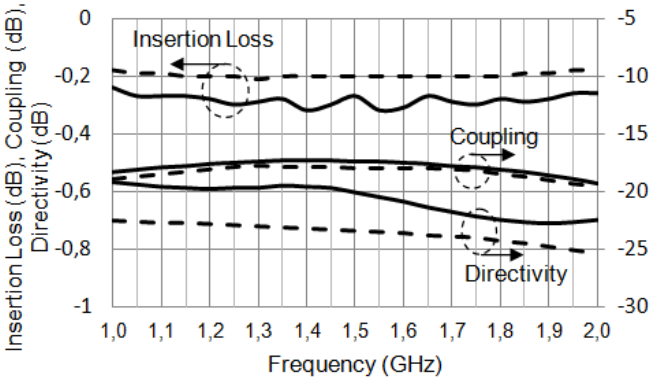
Figure 4.3 Theoretical Efficiency Characteristics in Load Modulation Region (DPA: Ideal, Class-B/class-B DPA, BA-DPA1: Linearly Changing Gate Voltage Adaptation, BA-DPA2: Linearly Changing Conduction Angle Adaptation)

4.1.2 Design and Implementation

Implementation phase is divided into 3 sub-phases. In the first phase, the critical RF element of bias adaptation circuit, the coupler, was designed using CAD tools. Wideband operation was aimed for future work of this study. Afterwards, bias adaptation circuit was designed and implemented based on the designed coupler. In the second phase, single ended PA and its BPA (Balanced Power Amplifier) versions, combination of two single-ended amplifiers with 90° hybrids, were implemented and tested on the bench. Finally, BA-DPA which uses same single-ended PA as building block was implemented, tuned for best efficiency and tested in a similar way. Both 1-tone measurements for power, gain and efficiency characteristics and modulated signal test for adjacent leakage ratio (ACLR) characteristics were hold. The measured performances of BA-DPA, SDPA and BPA were compared in this study.

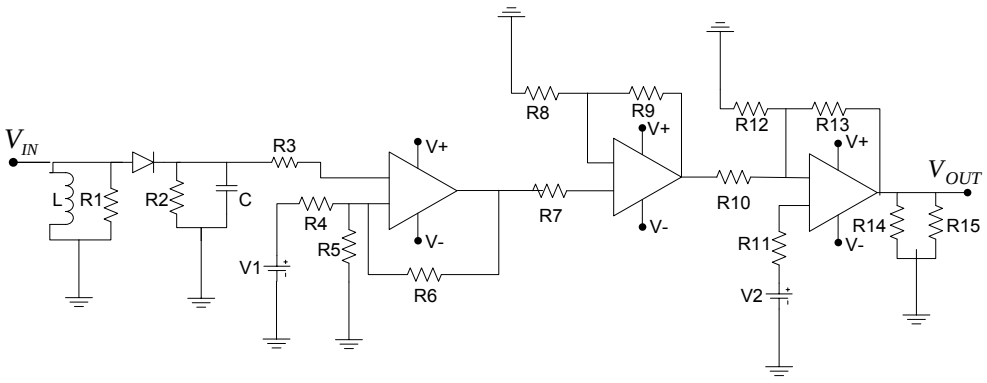
Couplers are one of the most critical elements of transmitters. They are widely used for forward and reflected power monitoring. In such kind of application, designed couplers should have flat coupling characteristic and high directivity over the frequency band. Although micro-strip coupled lines have easy implementations, they suffer from two natural limitations for broadband operations. The coupling ratio of a coupled micro-strip line is not constant on frequency spectrum. They shows approximately 6 dB/octave coupling ratio slope. Moreover, their directivity characteristic as a measure of isolation is not high enough to use them in power monitoring applications. Minimized coupling ripple can be achieved by using low-pass, resistive equalizer circuits at the coupling ports. However, in high frequencies, the equalizer can give in-band resonance and in-band coupling characteristic can be fluctuated over the tolerated values. On the other hand, directivity problem is originated from the inhomogeneous dielectric constant which results in mismatched phase velocities for even and odd modes. Beside of these limitations, the separation between coupled lines with high coupling ratio may become so small values which can not be realized in practice. In literature there are some common methods to overcome those limitations. High dielectric constant overlay material can be attached on the top of coupler to reduce the effect of inconsistent phase velocities between even and odd modes [85]. Alternatively, reactive elements like capacitor can be added between coupled lines to solve the phase difference problem [86]. However, the former application has dedicated fabrication procedure and the later application suffers from maximum voltage ratings and tight tolerances of lumped elements. Capacitors are usually very small values like 50-100 fF, so lumped element realization is impossible in most of the application. Alternatively, the inter-digital type micro-strip capacitors can be used as reactive elements without any limitations [87]. In this study, symmetric micro-strip coupled line with inter-digital capacitor compensation is preferred. Inter-digital capacitors can provide high directivity and minimum in-band coupling ripple for broadband application. The separation between lines is also large with respect to uncompensated couplers. After the tuning and optimization in ADS electromagnetic simulations, the coupler shown in Figure 4.4 (a) was designed. The simulation and measurement results after implementation have high consistency as shown in Figure 4.4 (b).

(a)

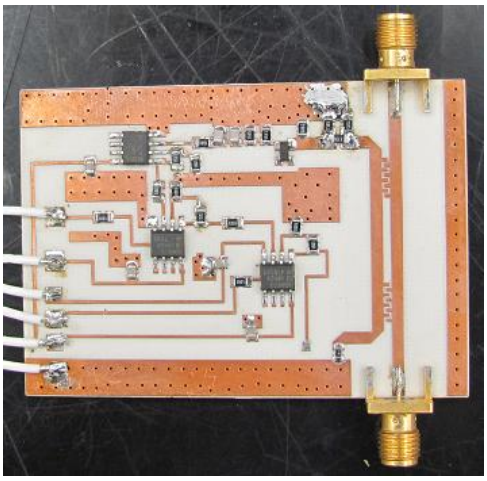


(b)

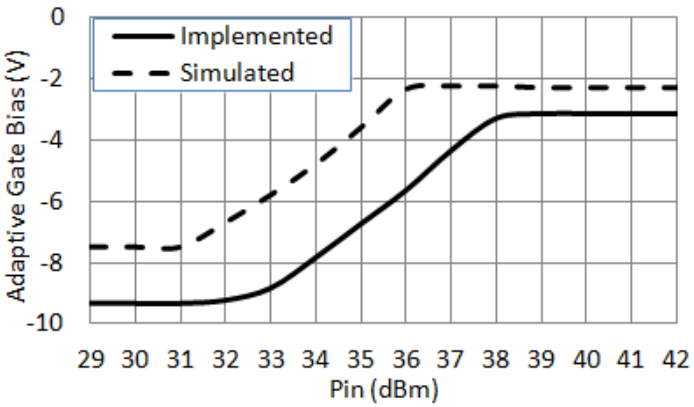
Figure 4.4 1-2 GHz Coupler, (a) Layout, (b) Simulated (Dashed) and Measured (Solid) Performances



(a)



(b)



(c)

Figure 4.5 Linearly Changing Bias Shaped Bias Adaptation Circuit, (a) Schematic, (b) Photograph of Implemented Circuit, (c) Measured Response

Although, linearly changing conduction angle shaped bias adaptation circuit offers higher efficiencies in load modulation region, it requires non-linear elements in realization. However, linearly changing gate bias voltage type bias adaptation circuit can be implemented using op-amp type linear elements. Designed and implemented circuit of this kind bias adaptation and its output

response are given in Figure 4.5. The resistor and supply voltage values were tuned for 6-dB load modulation region from 32 dBm to 38 dBm input power level.

In the first phase of PA design, the CAD design of narrowband single-ended PA was completed and validated by implementation. Matching networks were optimized for optimum power, efficiency and linearity within 50 MHz operational bandwidth centered at 1500 MHz. For reference, a BPA was also designed and implemented with the same transistors that are biased and matched identically. Although the efficiency is degraded, because of lower gain in class-B biasing, both BPA and BA-DPA were designed to have light class-AB biasing. Class-AB biasing scheme for the CPA is typically preferred to a class B, to reduce cross over distortion, to increase overall DPA linearity and to increase the gain at the expense of slight degradation in efficiency [70].

GaN transistors have high current density, high breakdown voltage, higher power operation capability with high efficiency at high frequencies and reduced R_{DS} and C_{DS} parasitic values. Dual path high power devices like push-pull package enables size and cost reduction of the realized power amplifier [66]. Due to the mentioned advantages we chose push-pull packaged CGH40090PP GaN on SiC transistor from Cree (Durham, USA).

Load pull simulations in ADS showed that the optimum load impedance for single side of CGH40090PP can be taken as $Z_{L,opt}$ =7.2+j2.5 for optimum power, efficiency and linearity. The output matching circuit was designed to meet this specification. Moreover, since the DPA is very sensitive to harmonic levels, filtering 2nd and 3rd harmonics is the second function of the output matching circuit. Design of output matching circuit is based on the narrowband L-C matching and uses a discrete capacitor and transmission lines instead of the inductors. Inductors are avoided due to low Q values over 1GHz. Capacitor was chosen from 600S family from ATC, USA by taking its ESR (Effective Series Resistance), voltage handling and Q values into consideration around 1.5 GHz. In the simulations, S-parameter files of the capacitors were used. $\lambda/12$-length open circuit stub and $\lambda/4$-length short circuit stub were used to eliminate 3rd and 2nd harmonic contents respectively. Same $\lambda/4$ length stub can be shortened with using decoupling capacitors at the drain bias side. Moreover, this kind of biasing technique with properly chosen valued capacitors reduces the memory effect as well [88]. The memory effects on PAs are IMD or ACLR asymmetry and BW dependent ACLR or IMD characteristics [62], [92]. The load impedance should be reduced to short for envelope frequency voltage components. Input matching network was designed to satisfy low return loss and sufficient gain with unconditionally stable operation. Similar to output matching network, simple L-C network was used for input matching. The electromagnetic simulation using ADS momentum analysis was performed on the matching network. The layout used in electromagnetic simulation and the overall response was tuned observing the power, efficiency and linearity characteristics.

In order to observe its large signal characteristics, such as output power, gain and PAE, the narrowband single-sided amplifier and BPA were simulated using Harmonic Balance. Both single tone harmonic balance simulation to observe PAE characteristic and 2-tones harmonic balance simulation to observe IMD3 levels were performed. 1-tone harmonic balance simulation showed that BPA can provide up to 50dBm (100 W) output power with nearly 60% PAE. On the other hand, for minimum 20dBc IMD3 level, 2-tone harmonic balance simulation showed that BPA can provide 48 dBm average output power related to 51 dBm PEP output power.

In the second phase, BA-DPA using bias adaptation was designed and implemented. Actually, Figure 4.3 concludes that linearly changing conduction angle offers higher efficiency in load modulation region. However, that kind of bias adaptation circuit requires non-linear components at gate bias side and the implementation requires more complex design. Hence, the DPA design was constructed with a linearly changing bias voltage type adaptation circuit, named BA-DPA in this paper. Both PAE and linearity can be improved by changing the gate bias shape of PPA. Similarly, the same control circuitry can be applied to the bias of CPA for further tuning of overall linearity by increasing the IMD cancellation degree [20], [89]. The gate bias adaptation circuit includes input coupler, attenuator, envelope detector and bias shaping circuit. There should also be delay line which can be realized by a length of coaxial line or delay filter for few nano-seconds of time delay [19]. The overall schematic of the BA-DPA circuit is given in Fig. 4. The bias adaptation circuit and its simulated response are also shown in Fig. 4. Input power of DPA is sampled over coupler at the input of DPA and this sampled power level is used to drive bias adaptation circuitry

to provide appropriate bias voltage to PPA. To widen the load modulation region, the matching circuits of CPA and the load modulation section as well as the bias shaping circuit should be changed.

In BA-DPA configuration whose layout is given in Fig. 5, the same single-sided power amplifier used in BPA were used with slight modifications for both PPA and CPA. The output transformer that transforms 50Ω real load to 25Ω load and Doherty load modulation inverter that transforms 25Ω to 100Ω were designed and simulated by linear model and electromagnetic model by momentum analysis of ADS. The shapes were decided by considering the practical realization. Doherty inverter should have the property of transforming the output voltage at one pair of terminals into a definite coexisting current at the other pair regardless of terminating impedance. In both design, λ/4 length transmission lines were used as a part of narrowband application. In classical DPA, in phase power combination at the end point is easily achieved by the usage of simple λ/4 delay line prior to PPA. However, in practice, optimum phase changed slightly over frequency range. Thus, extra delay lines called as offset lines are added. These offset lines are used to obtain optimized efficiency from CPA at TP and to represent high output impedance from PPA at low power levels below transition point [91]. In low power region, the OFF-state output impedance of PPA is very low resistive and highly capacitive. It is transformed to a high resistive value by using an offset line after its matching circuitry and power leakage from CPA is reduced to a negligible value [64]. In choosing the length of these delay lines, best-fit optimization should be applied, especially to the input delay line, which shows differences for maximum efficiency or flat gain i.e. linearity. To determine the required length of the offset line, output impedance of PPA in OFF state was investigated on Smith Chart. Simulations showed that 12.5 mm offset line is enough to obtain pure resistive high output impedance level from PPA in OFF-state. Finally, the phase difference between two PAs (CPA and PPA) was tuned to zero degree by using transmission lines at the input side of CPA. The required input offset line for CPA was found to be 10 mm. As observed from linear simulations, with this length of offset line for CPA, near 0 degree phase difference could be maintained between CPA and PPA.

1-tone harmonic balance simulation results to observe gain, power and drain efficiency characteristics of designed BPA and BA-DPA are given in Figure 4.6. BA-DPA provides well enhanced efficiency in nearly 6 dB power range between TP (44.5 dBm) and PEP (50.5 dBm). Real OFF-state condition for PPA below TP results in better efficiency characteristics at low power levels as well. Due to the convergence problem, 2-tone simulations cannot be completed on BA-DPA.

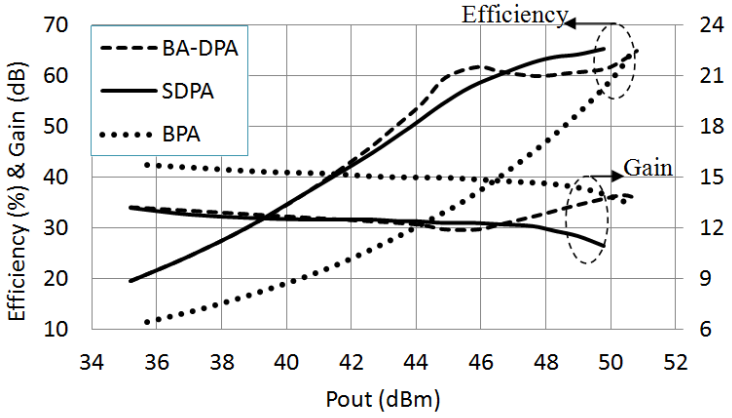


Figure 4.6 Simulated Efficiency and Gain Characteristics of BA-DPA

The simulated circuit belonging to the CPA and PPA of BA-DPA is shown in Figure. 4.7. To reduce memory effect, bypass capacitors at both operating frequencies and low envelope frequencies were used at the drain supply end of quarter-wavelength transmission line.

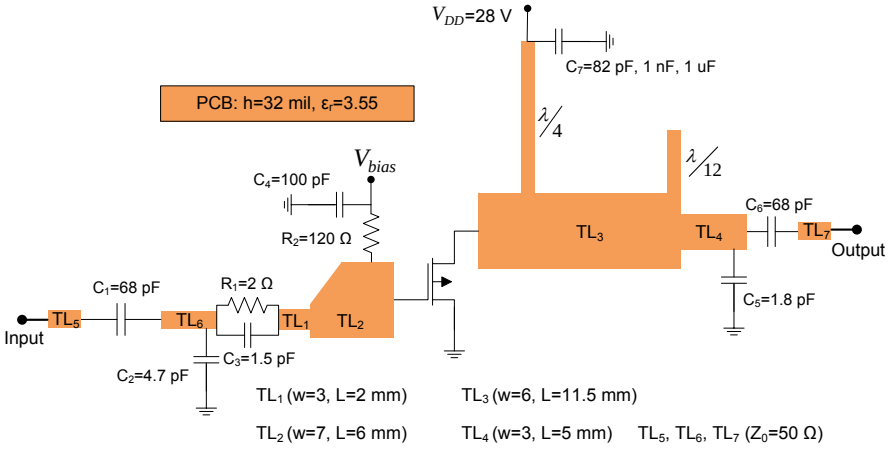
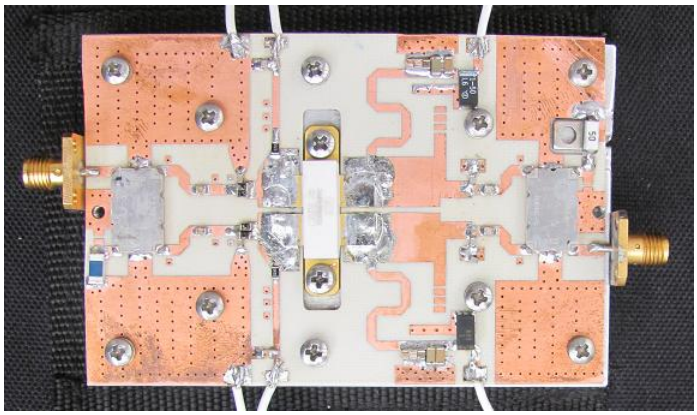
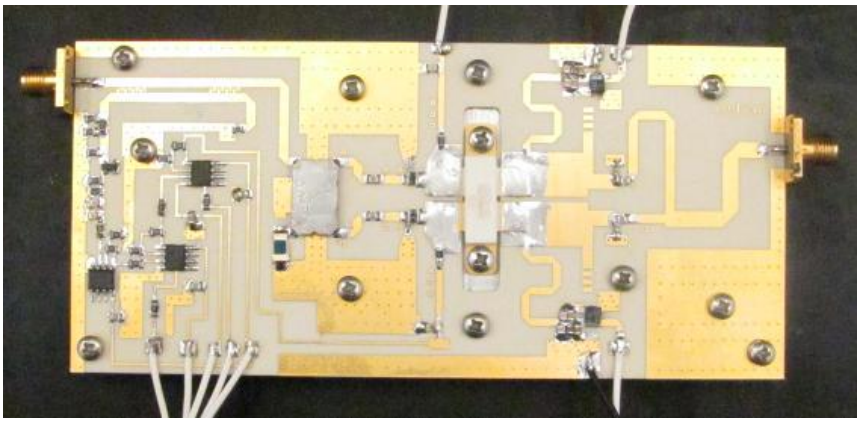


Figure 4.7 Schematic of CPA/PPA Sections of BA-DPA



(a)



(b)

Figure 4.8 Fabricated Circuits, (a) BPA, (b) BA-DPA

The realized BPA and BA-DPA, shown in Figure 4.8, were tested in terms of Gain and Drain Efficiency (DE). Their measured performances are given in Figure 4.9. The BA-DPA offers well enhanced efficiency over BPA. Moreover, BA-DPA has lower dip in load modulation region compared to conventional DPA. The lower deep in load modulation region and higher efficiency level at low power levels show that the analytical expressions given in the previous section were satisfied successfully.

The linearity characteristics of the BA-DPA have also been observed experimentally as shown in Figure 4.10. A single carrier wideband code-division multiple access (W-CDMA) signal with a peak-to-average power ratio (PAPR) of 6.5 dB has been applied and the adjacent-channel leakage ratio (ACLR) of the amplifiers have been measured. The BA-DPA has achieved an $ACLR_1$ (5 MHz offset) of -29 dBc and an $ACLR_2$ (10 MHz offset) of -40 dBc in the 6 dB power backed-off. Using DPA as the main amplifier of feed-forward systems, using pre-distortion or post distortion methods that utilize peaking compensation line and bias adjustment enhance the linearity performance significantly [23], [81], [90]. Usage of on shell chip devices prior to DPA provides up to 20 dB correction in ACLR or IMD levels [65].

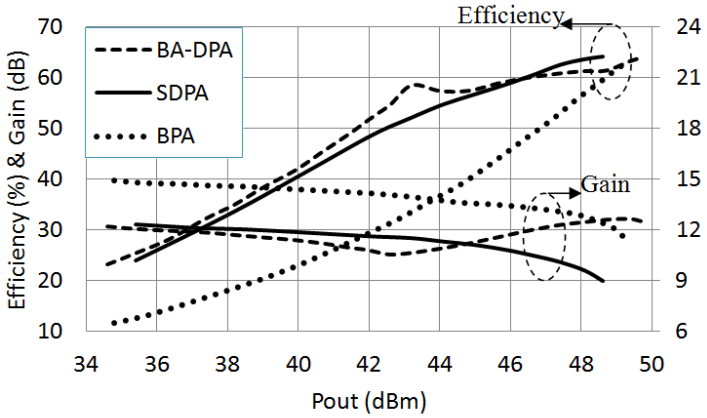


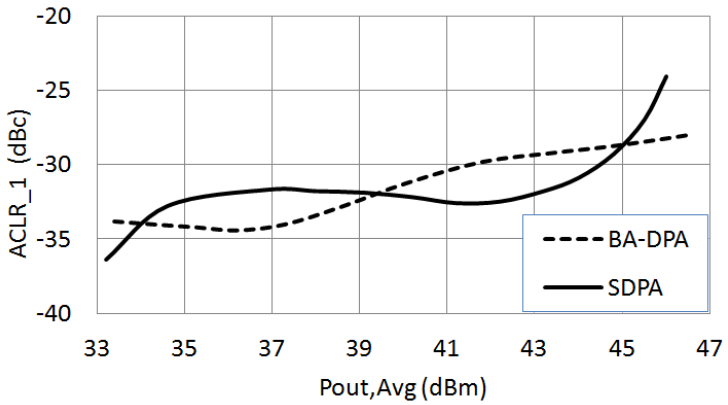
Figure 4.9 Measured Efficiency and Gain Characteristics of BA-DPA

4.2 Asymmetric Doherty Power Amplifier (ADPA)

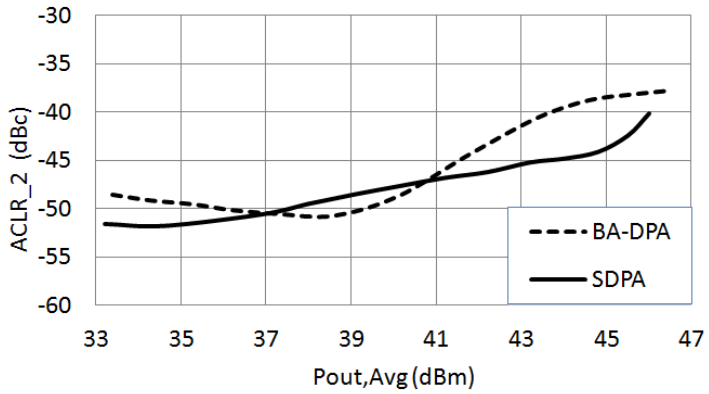
Another alternative topology of DPA is ADPA in which the different periphery devices with class-B/class-C configurations are used. Although the simple usage of class-B/class-C biased same sized transistors simplifies the implementations, it prevents delivering maximum power at the output of the DPA due to the lack of full load modulation at the maximum drive level. In order to improve the performance of class-B/class-C DPA, the other alternative topology addresses the use of larger periphery transistor in the class-C biased PPA section. This method is referred to as asymmetrical Doherty power amplifier (ADPA) and has been widely used in the recent applications [13-17]. The structure of the ADPA with higher periphery device in PPA section is given in Figure 4.1 (b). In (4.15), the closed form of efficiency equation in terms of the conduction angle ($\gamma'=2\gamma$) of PPA has been derived for BA-DPA in the usual 6 dB load modulation region. In BA-DPA case, full load modulation of CPA by PPA is guaranteed by adapting the biasing scheme which provides class-B condition for PPA at the maximum output power.

The class-C biased PPA that has same periphery with CPA cannot reach the output current or power of the CPA at the maximum drive level due to the insufficient driving signal. It results in the lack of full load modulation for the CPA and reduced output power of overall Doherty amplifier. Hence, the efficiency equation (4.15) is not valid for symmetrical DPA which is implemented by the same periphery devices.

In this section, the efficiency performance of ADPA is investigated and the required periphery ratio of the PPA to CPA for proper Doherty operation for different load modulation regions is introduced. Theoretical efficiency characteristic of the ADPA for 6 dB load modulation region is also illustrated.



(a)



(b)

Figure 4.10 Measured Linearity Characteristics of BA-DPA (a) $ACLR_1$, (b) $ACLR_2$

4.2.1 Analysis and Design Optimization

If higher periphery device is used in PPA, the output current of the PPA can reach the output current of CPA at the maximum output power. Hence, the full load modulation condition can be satisfied by appropriate scaling of PPA device and this configuration is referred as ADPA. Assuming the drain current waveforms of class-B biased CPA and class-C biased PPA, $i_D(t)$ and $i_D'(t)$ respectively, are as shown in Figure 4.2, the fundamental output current of CPA, namely i_1, and the fundamental output current of PPA, namely i_2, can be expressed as (4.18). The drain current swings, I_{DD} and $I'_{DD,}$ are proportional to the driving level, and the driving level of Doherty amplifier can be expressed in terms of normalized voltage factor, k, as in (4.19) with the linear operation property of DPA. The range of load modulation region is determined by the transition point, α, after which the PPA starts to conduct. Since the PPA is class-C biased, its conduction angle is proportional to its driving level. Assuming the class-C amplifier does not reach to the saturation level and it has constant transconductance, the conduction angle should satisfy the boundary conditions given in (4.20) for proper operation with adequate peripheries.

$$|i_1| = \frac{I_{DD}}{2},\ |i_2| = \frac{I'_{DD}}{2\pi}\{2\cdot\gamma - \sin(2\cdot\gamma)\} \tag{4.18}$$

$$\alpha \le k = \frac{V_O}{V_{DD}} = \frac{V_{IN}}{V_{IN,\max}} \le 1 \tag{4.19}$$

$$\begin{Bmatrix} \gamma = 0, & k = \alpha \\ \gamma = \gamma_{\max}, & k = 1 \end{Bmatrix} \tag{4.20}$$

Since conduction angle of non-saturated class-C biased PPA depends on current swing, I'_{DD}, and bias point, I_{dq}, the equations given in (4.21) can be deduced for the same boundary conditions. The maximum conduction angle, $\gamma'_{max}=2\gamma_{max}$, is obtained in terms of transition point as given in (4.23) by the aid of (4.22).

$$\begin{Bmatrix} \gamma = \cos^{-1}\left(\left|\frac{I_{dq}}{\alpha\cdot I'_{DD}}\right|\right) = 0, & k = \alpha \\ \gamma = \cos^{-1}\left(\left|\frac{I_{dq}}{I'_{DD}}\right|\right) = \gamma_{\max}, & k = 1 \end{Bmatrix} \tag{4.21}$$

$$|I_{dq}| = \alpha\cdot I'_{DD} \tag{4.22}$$

$$\gamma_{\max} = \cos^{-1}(\alpha) \tag{4.23}$$

In order to satisfy full load modulation of CPA by PPA, their fundamental output currents should have the same amplitude at the maximum driving point, for k=1. Since I_{DD} and I'_{DD} are determined by the device peripheries, necessary periphery ratio (RoP) of the PPA device to the CPA device for full load modulation can be deduced as given in (4.25) by using (4.24). The necessary periphery ratios and corresponding maximum conduction angles for proper Doherty operation are summarized in Table 4.1 for different load modulation regions.

$$|i_2|_{\max} = \frac{I'_{DD}}{2\pi}\{2\cdot\gamma_{\max} - \sin(2\cdot\gamma_{\max})\} = |i_1| = \frac{I_{DD}}{2} \tag{4.24}$$

$$RoP = \frac{I'_{DD}}{I_{DD}} = \frac{\pi}{[2\cdot\gamma_{\max} - \sin(2\cdot\gamma_{\max})]} \tag{4.25}$$

The efficiency characteristic of the ADPA with appropriate periphery ratio devices can be observed using the efficiency equation given in (4.15). Although it has been derived in terms of k and γ for the usual 6 dB load modulation region, it can be modified for different load modulation regions such as 9 dB and 12 dB. In (4.15) k and γ are not independent parameters; for a class-C biased PPA with an appropriate periphery, γ can be interpreted in terms of k.

For a fixed I_{dq} level, γ is a function of $I'_{DD,}$ which is proportional to the k value for a constant transconductance device, with relation given in (4.26). The theoretical efficiency characteristic of ADPA derived for 6 dB load modulation region with appropriate γ_{max} and RoP is shown in Figure 4.11 in comparison to the BA-DPA and ideal class-B/class-B DPA.

$$-I_{dq} = I'_{DD}\cos(\gamma);\quad 0 \le \gamma \le \pi/2 \tag{4.26}$$

Table 4.1 Maximum Conduction Angle of PPA at k=1 and Required Periphery Ratios for Different Load Modulation Regions

Load Modulation Region (α)	12 dB (1/2)	9 dB ($1/2\sqrt{2}$)	6dB (1/4)
Maximum Conduction Angle, $2\cdot\gamma_{max}$	0.84π	0.78π	0.67π
Periphery Ratio, RoP	1.5	1.8	2.6

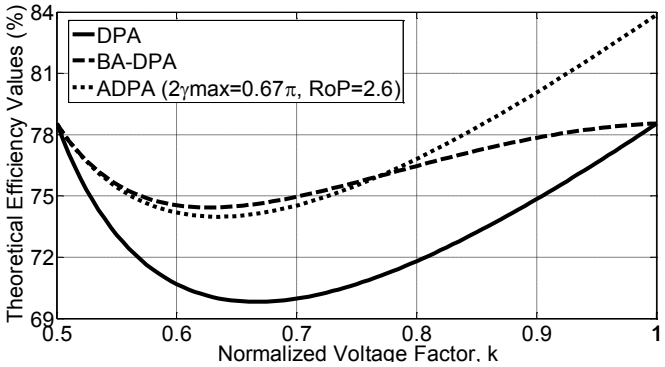


Figure 4.11 Theoretical Efficiency Characteristic of Asymmetrical DPA (ADPA) with $2\cdot\gamma_{max}=0.67\pi$ and RoP=2.6 in Comparison to Bias Adapted-DPA (BA-DPA) and Ideal Class-B/Class-B DPA

4.2.2 Design and Implementation

In ADPA structure, single 45 W transistor (CGH40045) for the carrier device and ~2.6 times larger sized 120 W transistor (CGH400120) for the peaking device were utilized. In the first phase, the CAD design of class-AB and class-C single-ended PAs was completed and validated by implementation. The class-AB biased CPA sections of ADPA and BA-DPA are identical to the amplifiers of BPA. Light class-AB biasing scheme for the CPA is typically preferred to a class-B, in order to reduce cross over distortion, to increase overall DPA linearity and to increase the gain at the expense of slight degradation in efficiency. The PPA section of ADPA was biased in class-C configuration. Matching networks were optimized for optimum power, efficiency and linearity within 50 MHz operational bandwidth centered at 1500 MHz.

Based on the load pull simulations in ADS the optimum load impedances were determined as $Z_{L,opt}$=7.2+j2.5 and $Z_{L,opt}$=3-j1.2 for class-AB biased 45 W and class-C biased 120 W transistors respectively. The output matching circuits were designed to match these optimum load impedances to the 50 Ω terminals [93]. Moreover, since the DPA is very sensitive to harmonic levels, 2nd and 3rd harmonics filtering is the second function of the output matching circuit. Design of output matching circuit is based on the narrowband L-C matching that includes discrete capacitors and transmission lines. The capacitors were chosen from 600S family from ATC Inc. (USA) by taking its ESR (Effective Series Resistance), voltage handling and Q values into consideration around 1.5 GHz. S-parameter files of the capacitors were used in the simulations. Optimized λ/12-length open circuit stub and λ/4-length short circuit stub were used to reject 3rd and 2nd harmonic contents respectively. The drain bias was provided at the end of λ/4 length stub that was shortened with using decoupling capacitors. This kind of biasing technique with properly chosen valued capacitors

reduces the memory effect as well. The memory effects on PAs are IMD asymmetry and BW dependent IMD characteristics. Input matching network was designed to achieve low return loss and sufficient gain with unconditionally stable operation. The electromagnetic simulation using ADS momentum analysis was performed on the matching networks. The output transformer that transforms 50 Ω real load to 25 Ω load and Doherty load modulation inverter that transforms 25 Ω to 100 Ω were also designed and simulated by electromagnetic momentum analysis of ADS. In both design, λ/4 length transmission lines were used as a part of narrowband application. In an ideal Doherty application, in-phase power combination at the end point is easily achieved by using simple λ/4 delay line prior to PPA.

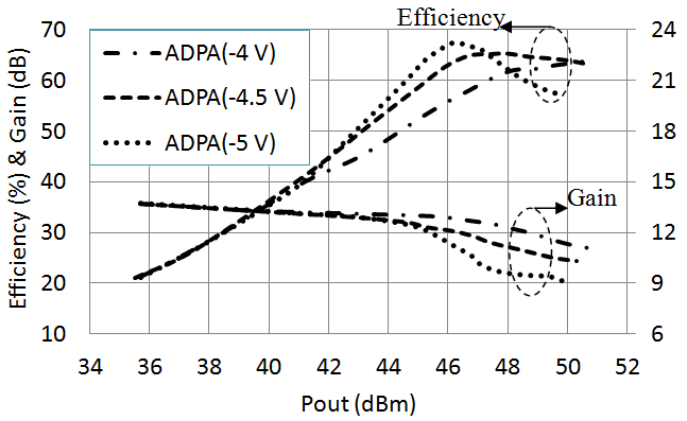


Figure 4.12 Simulated Performance of ADPA with Different Bias Points

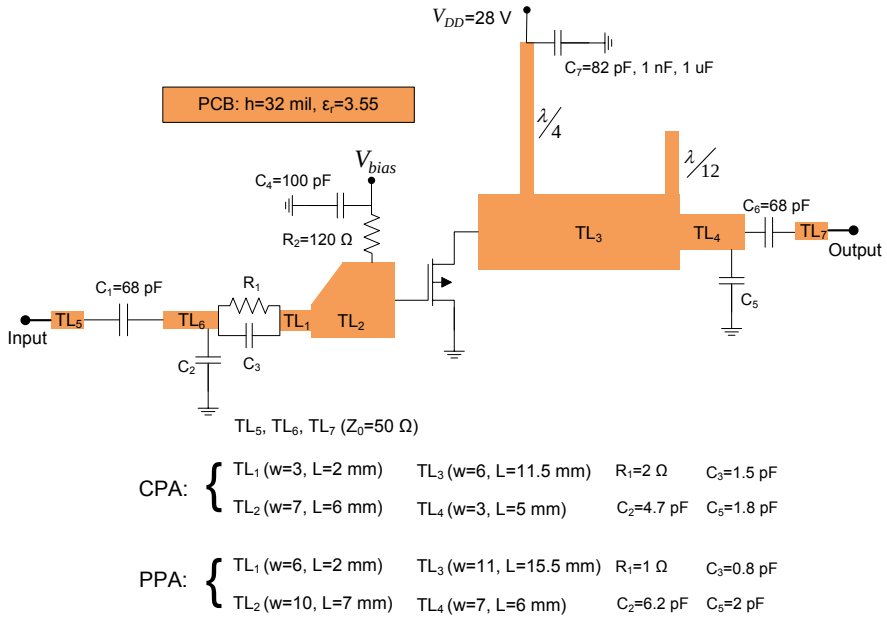


Figure 4.13 Schematics of CPA/PPA Sections of ADPA

However, in practice, optimum phase changes slightly over frequency range. Thus, extra delay lines called as offset lines are added. These offset lines can also be used to obtain optimized efficiency from CPA and to represent high output impedance from the PPA at low power levels below the transition point. In low power region, the off-state output impedance of PPA is very low resistive and highly capacitive. It is transformed to a high resistive value by using an offset line after its matching circuitry and power leakage from CPA is reduced to a negligible value. In order to determine the required length of the offset line, the output impedance of the PPA in off-state was investigated on Smith Chart. Simulations showed that 8 mm offset line is enough to obtain pure resistive high output impedance from the PPA in its off-state. The required input offset line for the PPA was found to be 6 mm in order to maintain nearly zero degree phase difference between the CPA and PPA. The final and the most critical design step for ADPA structure is determining the bias point of class-C PPA. As concluded from the analysis carried in the previous part, the appropriately biased class-C PPA should satisfy two conditions simultaneously. It should start to conduct at the transition point where the CPA saturates and it should represent full load modulation to the CPA by providing sufficient maximum current at the peak output power level. In order to determine the most appropriate biasing level, the ADPA was simulated using the harmonic balance tool in ADS by observing its large signal characteristics, such as output power, gain and efficiency. The simulated drain efficiency and gain characteristics of the ADPA are given for different biasing schemes between V_{gs}=-4 V and -5 V in Figure 4.12. With the -4 V biasing point, the peaking device starts to conduct earlier than the saturation of the carrier device and the maximum efficiency is not achievable at the transition point. On the other hand, more dip class-C biasing with -5 V, causes the late conduction and insufficient conduction angle for peaking device resulting in lower gain at the transition point and reduced maximum power level due to the lack of load modulation. Therefore, the appropriate biasing point was determined as ~-4.5 V at the end of the simulation phase. The single-ended CPA and PPA that were designed and used in the simulations of the ADPA are given in Figure 4.13.

The peaking devices start to conduct at nearly 6 dB below the maximum power level. Their drain currents become closer to the drain currents of the carrier devices as an indication of full load modulation at the maximum power level. 1-tone harmonic balance simulation given in Figure 4.14 showed that the ADPA can provide well enhanced efficiency over conventional BPA and SDPA in nearly 6 dB power range between the transition point (44.5 dBm) and maximum power point (50.5 dBm). At the maximum power level, the efficiency degradation of the ADPA with respect to the analytical result is due to non-constant transconductance of the class-C biased PPA that starts to saturate before the maximum power level.

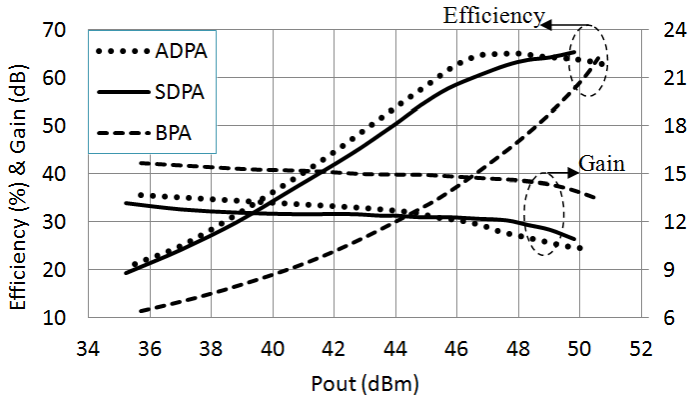


Figure 4.14 Simulated Efficiency and Gain Characteristics of ADPA

The layouts and component values used in electromagnetic simulations were tuned observing the overall responses such as output power, efficiency and gain characteristics. The implemented ADPA is shown in Figure 4.15. The transistor used in the carrier device was set to lightly biased class-AB scheme with 200 mA drain current. To reduce memory effect, coupling capacitors at both

operating frequencies and low envelope frequencies were used at the drain supply end of quarter-wavelength transmission line. The realized ADPA was tested in terms of gain and drain efficiency characteristics as given in Figure 4.16. The measured performances at the center frequency of 1.5 GHz have high conformance with the simulated ones. The amplifier offer well enhanced efficiency over conventional BPA. ADPA has an efficiency curve in a different shape from the ideal case but still has acceptable efficiency enhancement in the load modulation region.

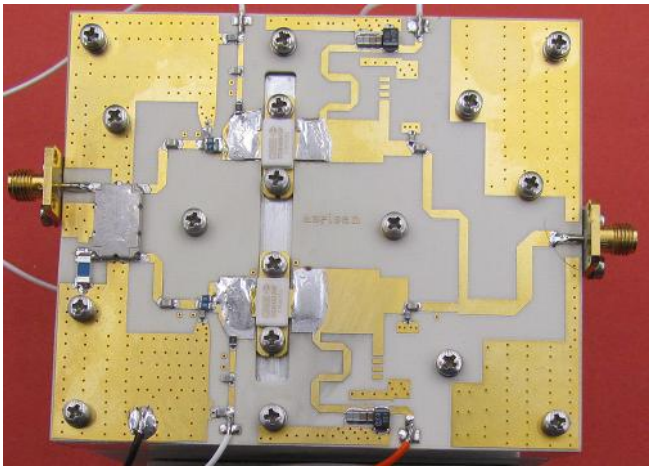


Figure 4.15 Fabricated Circuit of ADPA

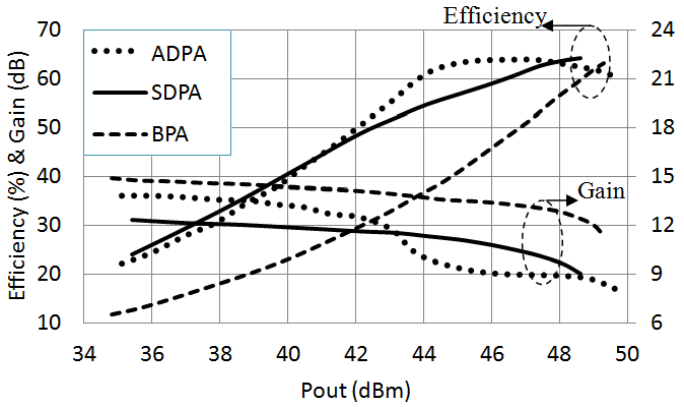
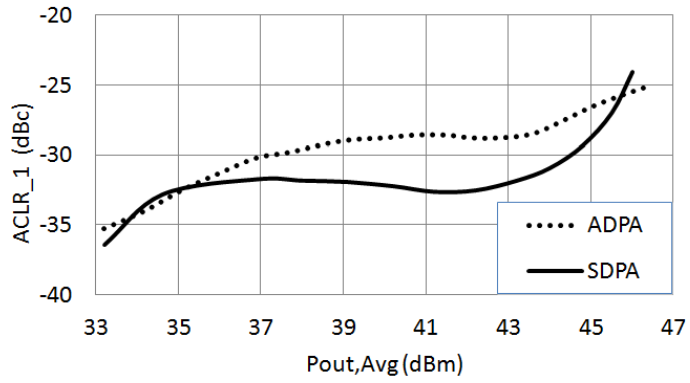
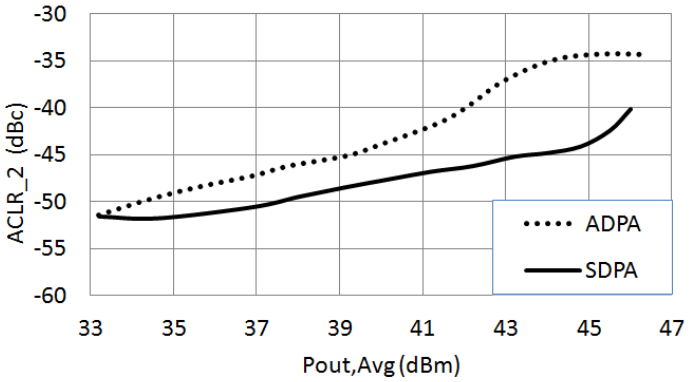


Figure 4.16 Measured Efficiency and Gain Characteristics of ADPA

The linearity characteristics of the ADPA have also been observed experimentally as shown in Figure 4.17. A single carrier wideband code-division multiple access (W-CDMA) signal with a peak-to-average power ratio (PAPR) of 6.5 dB has been applied and the adjacent-channel leakage ratio (ACLR) of the amplifiers have been measured. The ADPA has achieved an $ACLR_1$ (5 MHz offset) of -27 dBc and an $ACLR_2$ (10 MHz offset) of -36 dBc in the 6 dB power backed-off.



(a)



(b)

Figure 4.17 Measured Linearity Characteristics of ADPA (a) $ACLR_1$, (b) $ACLR_2$

4.3 Performance Comparison of BA-DPA and ADPA

Although the ADPA and BA-DPA methods have been widely researched and realized up to date, these applications differ with at least one aspect in terms of specific application frequency, power level and employed transistor technology. Therefore a fair comparison between the ADPA and BA-DPA techniques has not been reported as yet. In this section, optimally designed ADPA with adequate maximum conduction angle and adequate periphery PPA is compared with BA-DPA technique which is implemented at the common operation frequency, with similar output powers and by employing the same technology transistors.

The fabricated ADPA and BA-DPA are shown in Figure 4.18. The realized ADPA and BA-DPA have been tested in terms of gain and drain efficiency characteristics as given in Figure 4.19. Although there is nearly 1 dB reduction in the maximum power level with respect to the simulation results, the measured efficiency and gain characteristics at the center frequency of 1.5 GHz have high conformance with the simulated ones. The maximum output power has been noted as 49.6 dBm. Both amplifiers have better efficiency characteristic and nearly 1 dB higher output power than the conventional SDPA. In the load modulation region of 6 dB, the efficiency of BA-DPA has very similar characteristic to ideal Doherty operation and it is above 57% through the load modulation region. The ADPA has an efficiency curve in a different shape from the ideal case but still has acceptable efficiency enhancement, between 56% and 63%, in the load modulation region. The BA-DPA has better gain characteristic because the class-C biased peaking device lowers the overall gain of the ADPA.

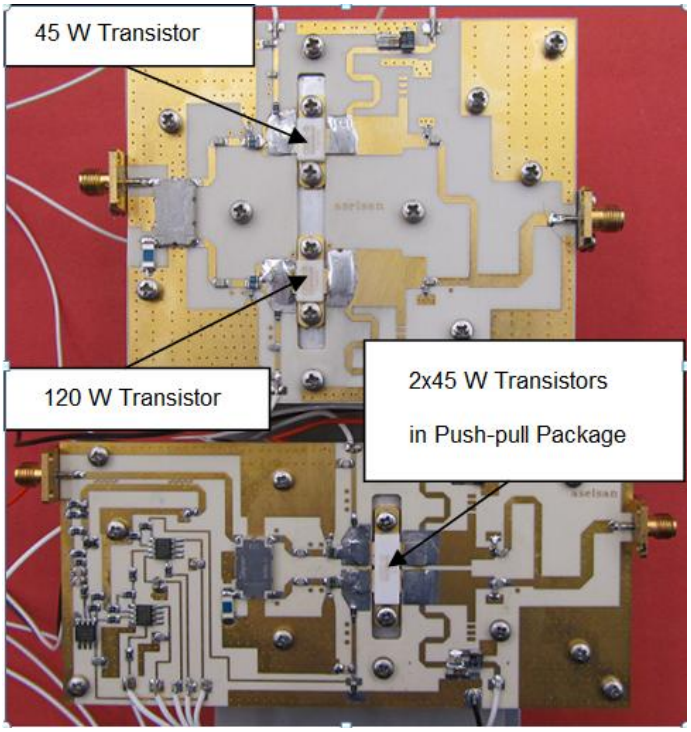


Figure 4.18 Dimension Comparison of BA-DPA and ADPA

A single carrier wideband code-division multiple access (W-CDMA) signals with a peak-to-average power ratio (PAPR) of 6.5 dB has been applied and the adjacent-channel leakage ratio (ACLR) of the amplifiers have been measured. The BA-DPA has achieved an $ACLR_1$ (5 MHz offset) of -29 dBc and an $ACLR_2$ (10 MHz offset) of -40 dBc in the 6 dB power backed off. At the same output power level, the $ACLR_1$ and $ACLR_2$ of the ADPA have been measured as -27 dBc and -36 dBc respectively. The linearity performances given in Figure 4.20 can be further improved by using the pre-distortion techniques.

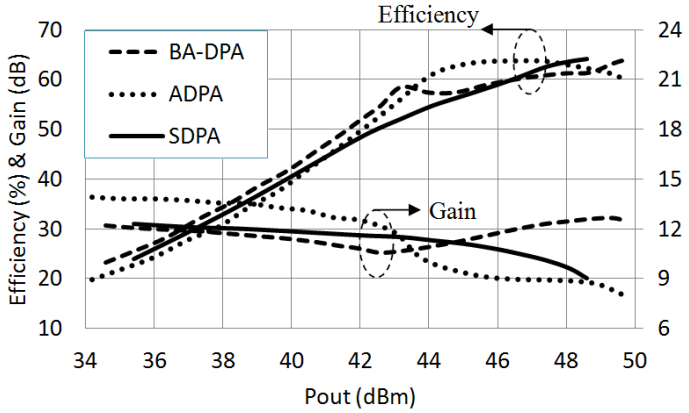
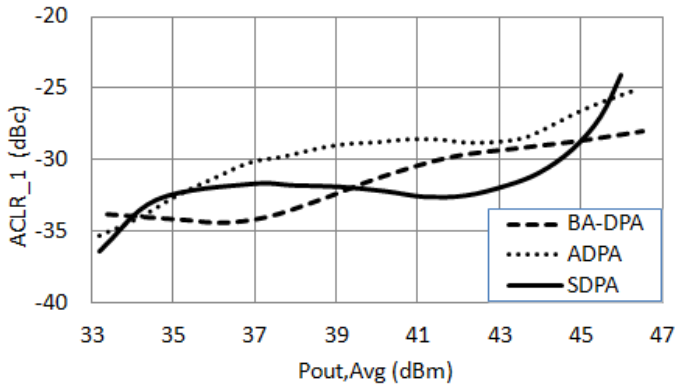
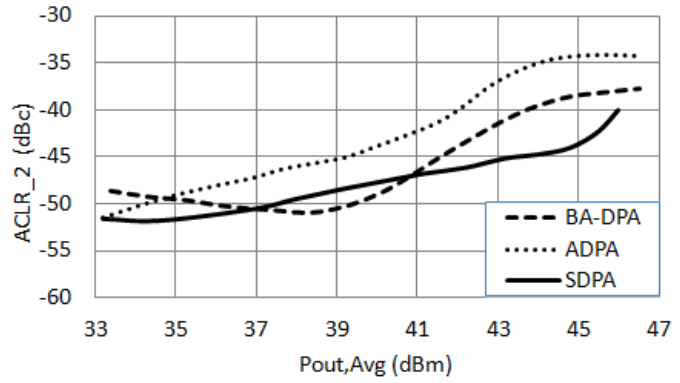


Figure 4.19 Performance Comparison of BA-DPA and ADPA; Measured Drain Efficiency and Gain



(a)



(b)

Figure 4.20 Linearity Comparison of BA-DPA and ADPA Using W-CDMA Signal with PAPR=6.5 dB, (a) $ACLR_1$ (5 MHz offset), (b) $ACLR_2$ (10 MHz offset)

Both the BA-DPA and ADPA structures offer well enhanced efficiency characteristic with respect to the conventional ADPA. The conduction angle of the class-C biased peaking device has important role on the efficiency, gain, power and linearity characteristics of the overall Doherty amplifier. The gain degradation of the ADPA in the load modulation region where the class-C biased peaking device starts to conduct results in poorer power-added efficiency. On the other hand, BA-DPA ensures the full load modulation of the carrier device through the bias adapted peaking device, so the output power is inherently maximized. The efficiency characteristic that is closer to the ideal Doherty operation is another aspect of the BA-DPA. The measurements have also shown that the BA-DPA can perform with higher linearity in the high power region due to the bias adapted PPA from class-C to class-B biasing scheme. The larger periphery transistor requirement of ADPA in the peaking amplifier avoids having cost effective solution. It is a waste of periphery and in some extreme cases the discrete transistor with an appropriate periphery cannot be available. Furthermore, the impedance matching of the larger periphery transistor that has lower input and output impedances requires an intensive effort especially for wideband applications. On the other hand, an additional control circuit of the BA-DPA is the most common drawback of the structure. Although its simple implementation ensures a cost effective solution the envelope detector and bias shaping circuitry inherently limits the instantaneous bandwidth of the amplifier. The BA-DPA can be used for the signals whose aggregated bandwidth is up to a few MHz. However, it is not a candidate for the wideband signals like long-term evaluation signals in which the bandwidth can reach 100 MHz

CHAPTER V

A NOVEL WIDEBAND DOHERTY POWER AMPLIFIER

The octave-bandwidth PAs are usually employed in many electronic warfare systems (Electronic Attack AT and Electronic Stand, ES) where broadband operation is necessary. Modern signals with high PAPRs forces the PAs used in these systems to have linear characteristics. Efficiency is also crucial for that kind of systems especially for the mobile ones where the battery or generator power is limited. Thus, the accomplishment of broadband DPA can replace the conventional Balanced class-AB/B PAs which are used in this systems with today's technology.

Although, Doherty system rivals the other alternative systems in term of efficiency enhancement capability for different power back-off varying envelope signals, the narrow bandwidth operation is serious and attractive problem that DPA suffers. This is due to the quarter-wave ($\lambda/4$) lines used in the topology and phase mismatches between two active devices, main amplifier and peaking amplifier, which are operated in different manners. Bandwidth restriction of DPA due to the use of quarter-wave line and the requirements for accurate phase matching between two devices is still one of the hottest research topics in this field.

In modern communication era, wireless communication systems require radio transmitters to operate over a wide frequency range providing multiband multimode operation. The modern communication standards cover wider bandwidth as high as 100 MHz and higher peak-to-average power ratio (PAPR) up to 12 dB due to high data rates used in the spectrally efficient digital modulation schemes [38].

One of the key elements of such transmitters is the wideband power amplifier (PA). High PAPR signals force the PAs to work at power backed-off region, thus reducing the power efficiency of the conventional transmitters considerably. In addition, many electronic warfare systems such as jammers and electronic attack systems also require multimode and multiband operation when the transmission of older communication standards is needed for backward compatibility.

Multimode operation force the PAs to operate in wide output power range with peak efficiency in order to save the limited line power. Therefore, the requirement on the PAs of modern transmitters are designated as operating in a wide frequency range and maintaining high efficiency in a wide output power range.

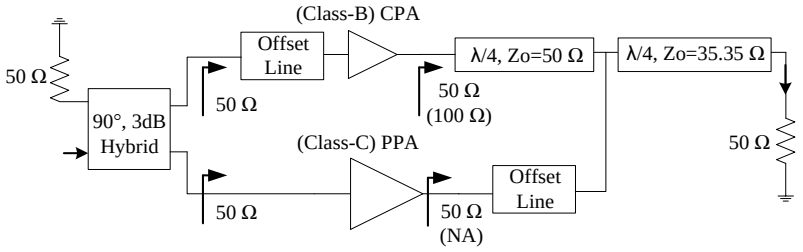
Using dual-band or broadband design techniques provide the systems with the capability of operating on multiband standards and covering many communication frequency bands with the least number of devices eliminating the redundant hardware. The conventional balanced broadband PAs which use broadband class-A/-AB PAs and 90°, 3dB hybrids are offered as octave bandwidth devices by many manufacturers in the market. However, the conventional linear PAs are optimized to operate at the specific maximum output power with a fixed supply voltage and optimized load impedance. Hence, they exhibit poor efficiency performance in back-off power levels. The Doherty power amplifier (DPA) is a strong candidate for multimode multiband operation due to its low hardware complexity, a wide aggregated instantaneous bandwidth and tunable efficiency characteristic for different power ranges. It provides an inherent linear performance and significant efficiency enhancement at the power back-off (PBO) operation.

The operation principle of a DPA is based on active load modulation and power combining properties. The peaking (auxiliary) device decreases the load impedance seen by carrier (main) device, as the driving level increases beyond the transition point (TP) at which the carrier device reaches saturation and peak efficiency.

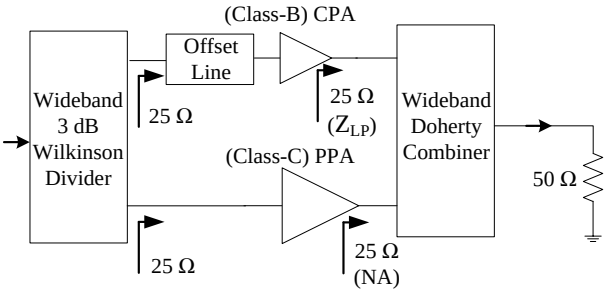
In order to improve the efficiency, various kinds of DPA architectures such as bias adapted DPA and asymmetrical DPA have been proposed up to date. There has been a lot of announced Doherty

implementation in the literature where the back-off efficiency and the linearity were enhanced by the utilization of the Doherty architecture with the aid of inter-modulation cancellation and digital pre-distortion techniques. However, most of these studies on Doherty PAs have addressed the narrowband operation and are not suitable for the multimode/multiband operation requirements of the modern communication systems.

The conventional Doherty PA offers enhanced efficiency characteristic in a fractional bandwidth; smaller than 10% [24], [25]. Narrow bandwidth operation is the fundamental weakness of the DPA and it compromises the convenience of DPA for multimode/multiband operations. The conventional DPA shown in Figure 5.1 (a) is composed of class-B carrier power amplifier (CPA), class-C peaking power amplifier (PPA), 90° transmission lines and extra offset lines. The 90° transmission line prior to load is used in order to transform the 50 Ω output impedance to the 25 Ω common load impedance for the CPA and PPA. It does not impose a serious restriction for broadband operation. However, use of the 90° transmission line in front of the CPA should have two folds and it has a great influence on the bandwidth extension problem. Firstly, this line is used to saturate the CPA below the rated power level by providing load transformation action in low power region. Secondly, it performs the load modulation action of the CPA by PPA in high power region. Another limiting factor in bandwidth extension problem is the necessity of quasi-open-circuit at the output of the off-state PPA to prevent power leakage in low power region. Unlike to the ideal devices, the capacitive output impedance of the PA in the real world reveals the power leakage and causes degradation in efficiency performance [94].



(a)



(b)

Figure 5.1 Doherty Power Amplifier (DPA) Structures, (a) Conventional DPA (b) Proposed DPA

Recently, there have been several investigations in order to enhance the efficiency performance of the DPA over a wide frequency range [24]-[26], [95]-[100]. Most of the efforts are concentrated on widening the limited bandwidth of the quarter-wavelength impedance inverter. A simple offset-line is utilized to form the quasi-open impedance condition at the output of the PPA in low power region. The work done in the literature can be briefed as follows. M. Sarkeshi *et al.* used adaptive impedance inverter based on the varactors [95]. J. H. Qureshi *et al.* proposed a quasi-lumped transmission line impedance inverter compensating the output capacitance of the transistor [96]. K.

Bathich *et al*. proposed the usage of a ladder-type multi-section matching network and a quarter-wavelength impedance inverter with reduced transformation ratio to extend the bandwidth of the conventional DPA [97], [98]. D. Kang *et al.* used a direct power dividing technique by taking the effects of broadband matching networks into account [99]. G. Sun and R. H. Jansen implemented a broadband DPA and investigated its limitations by using simplified real frequency technique [26]. D. Y. Wu *et al.* designed a wideband DPA by utilizing quasi-lumped quarter-wavelength impedance inverter and Klopfenstein taper based broadband matching network [24]. R. Darraji *et al.* proposed a digital technique to control the input power distribution and phase variation between the CPA and PPA [25]. In summary, efforts in the cited works are concentrated on widening the limited bandwidth of the quarter-wavelength impedance transformers.

In this study, the DPA structure is modified for broadband operation as shown in Figure 5.1 (b). The output combiner structure that is composed of quarter-wavelength impedance inverter and impedance transformer in the conventional DPA is replaced by a new combiner structure. The proposed combiner solves both the broadband impedance inverter and quasi-open impedance condition problems. The proposed combiner is designed by considering the boundary operation conditions of the conventional combiner for proper load modulation. The boundary operation conditions of the conventional DPA combiner are defined at the transition point where the CPA reaches saturation and at the maximum power point where both amplifiers distribute their rated powers.

The proposed combiner structure also eliminates the additional off-set line usage for quasi-open impedance condition at the output of the PPA. Hence, it simplifies the broadband DPA design problem into the design of broadband sub-amplifiers and broadband input power divider.

The other key point in this work is designing the CPA and PPA for 25 Ω terminal impedances. The reduced load and source impedances facilitate the achievements of the optimum power and efficiency performances especially in a broadband application. Any additional component in the output matching network of the PPA that introduces positive phase dispersion narrows the maximum achievable bandwidth of the DPA [26]. Hence the reduced load impedance extends the bandwidth of the DPA by simplifying the output matching network of the PPA.

Finally, the optimum load impedance of the CPA in low power region that is twice the rated power impedance in the conventional structure is also modified to enhance the efficiency performance in low power region. DPA operation in the frequency band of 0.85-1.85 GHz was achieved with minimum 42% and 37% drain efficiencies through the 6 dB PBO regions in the simulation and implementation phases respectively. The implemented design demonstrated a great performance in the band of 0.9-1.6 GHz with a drain efficiency of higher than 52% through 6 dB power-back-off (PBO) region. By using the proposed structure, all the current third-generation (3G) and fourth-generation (4G) bands can be covered using only two DPAs operating on 0.7-1.4 GHz and 1.4-2.8 GHz frequency bands.

5.1 Wideband Doherty Combiner

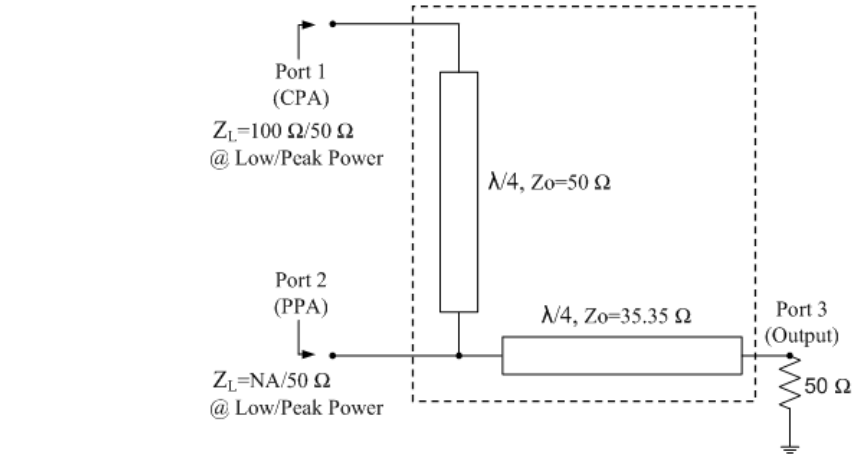
The fundamental band limitation of the conventional Doherty combiner originates from the quarter-wavelength transmission line at the output of the CPA. The CPA that is designed with 50 Ω load impedance for maximum power and efficiency performances operates into the load impedance of 100 Ω due to the impedance transformation of the quarter-wavelength line. Doubled load impedance provides the CPA with saturating at the half of its rating power with the maximum efficiency. The CPA that is the only active portion of the DPA in the low power region performs with higher efficiency performance up to the transition point (TP) after which the PPA starts to operate.

In the high power region, PPA modulates the load of CPA through the quarter wavelength line. By the impedance inverting action of the quarter-wavelength line, the PPA decreases the load impedance seen by the CPA, as the driving level increases beyond the TP. Both the CPA and PPA operate into 50 Ω common load impedance presenting their optimum performances and delivering equal powers to the output at the maximum power point. However, the quarter-wavelength transformer has a narrow-band operation. Although the reduction of the transformation ratio

enhances its bandwidth, the non-optimum transformation ratio degrades the efficiency performances of the DPA, and the bandwidth enhancement is limited well below the octave-bandwidth levels.

In this work, the output portion of the Doherty structure including the band limited quarter wave-length line is interpreted as a special combining network as shown in Figure 5.2 (a). The operation of this combiner is characterized at the TP and maximum power point of the ideal Doherty operation. At the TP where the PPA (port 2) represents open circuit impedance, the combiner represents low return loss (S_{11}) and insertion loss (S_{31}) when port-1 and port-3 are terminated with 100 Ω and 50 Ω respectively. The combiner distributes equal power from port 1 and port 2 to the output with minimum insertion losses (S'_{31} and S'_{32}) at the maximum power point where both the CPA and PPA operate into the ideal load impedance of 50 Ω. If these boundary operation conditions are satisfied in a wide bandwidth, the broadband DPA design problem would be simplified into the design of broadband sub-amplifiers and broadband input power divider.

A novel Doherty combiner structure satisfying the boundary conditions is proposed in this maximum power point. The CPA and PPA were designed to operate into 25 Ω load impedance at the maximum power as discussed in Section 5.2. The proposed combiner is designed using the short-length taper lines. The taper lines are strong candidates for the applications of broadband matching and impedance transformation [101]. The optimized combiner for an octave-bandwidth application ranging from 1 to 2 GHz is shown in Figure 5.2 (b).



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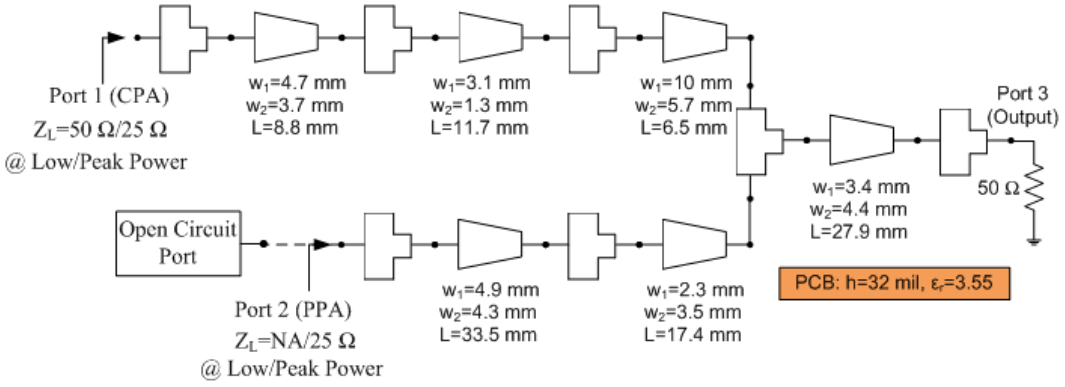
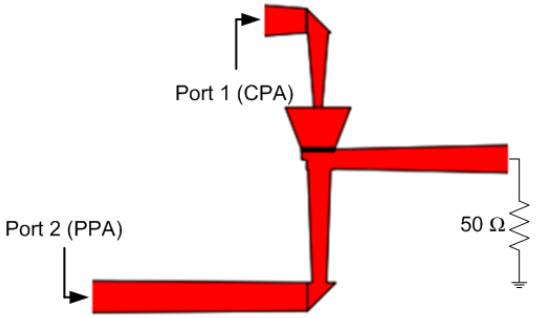


(b)

Figure 5.2 Doherty Combiner Structures, (a) Conventional Combiner, (b) Proposed Wideband Combiner for 1-2 GHz

The simulated and measured characteristics of the conceptually verified wideband Doherty combiner and its layout are given in Figure 5.3. In this design, the ideal operation condition of DPA in which the output port of the PPA (port 2) presents exact open circuit condition in low power region was assumed. The design goals were derived from the boundary operating conditions of the conventional Doherty combiner at the TP and maximum power point.



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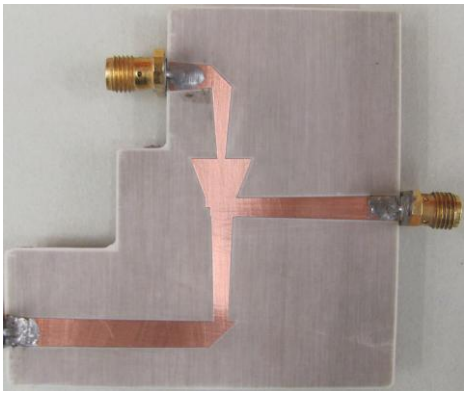

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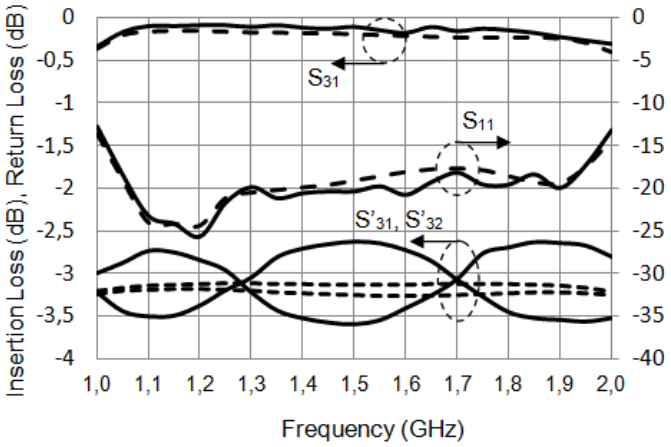


(c)

Figure 5.3 Ideal Wideband Doherty Combiner Structure and Its Simulated (Dashed Lines) and Measured (Solid Lines) Performances, (a) Layout, (b) Photograph, (c) Low Power Behaviors; Insertion Loss (S_{31}), Return Loss (S_{11}) When Port 2 is Open Circuited, Port 1 is Matched to 50 Ω and High Power Behaviors; Combiner Insertion Losses (S'_{31} and S'_{32}) When Port 1 and Port 2 are 25 Ω.

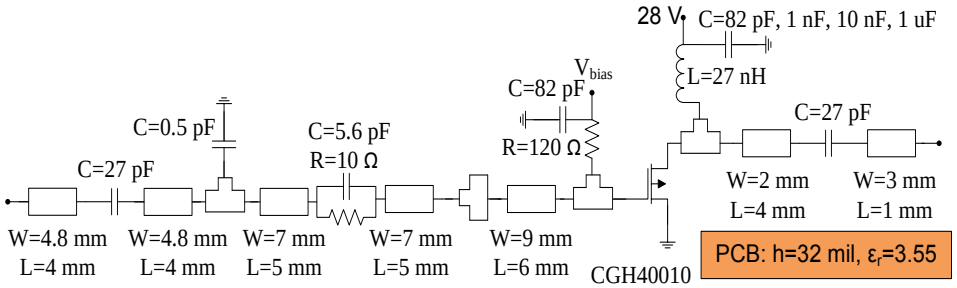
In low power region up to TP, the CPA (port 1) was intended to operate for 50 Ω load impedance with minimum insertion loss between port 1 and output port (port 3). The return loss and insertion loss behaviors of the designed combiner are shown in Figure 5.3 (c) as S_{11} and S_{31}, respectively. Lower than 0.4 dB insertion loss was maintained through the targeted frequency range. It shows the efficient power transfer from the CPA to the output of the DPA in low power region. Similarly, a return loss of higher than 14 dB was achieved. This indicates that the CPA operates into the proposed load impedance of 50 Ω in low power region up to TP. At the maximum power point, both the CPA and PPA which were designed to operate into 25 Ω load impedances for their rating powers were intended to deliver powers to the output of the DPA with minimum losses. The combiner loss characteristics from the CPA port (S'_{31}) and PPA port (S'_{32}) are shown in Figure 5.3 (c). Acceptable loss performances at the maximum power point where both the CPA and PPA operate into 25 Ω load impedances were measured with ±0.5 dB amplitude imbalance. Wideband 50/25 Ω tapered line transformer has been used in the measurement phase of 25 Ω ports by network analyzer.

By this way, the wideband operation of the Doherty combiner is verified, however; in this verification ideal operation of the DPA was assumed. In practical Doherty operation, the output impedance of the inactive PPA is highly capacitive and it limits the achievable bandwidth as well. This limitation was also imported to the combiner design and the proposed combiner was improved by taking the non-open circuit condition of the inactive PPA output impedance into consideration as further explained in Section 5.3.

5.2 Designing Wideband Carrier/Peaking Amplifiers and Input Power Divider

The proposed Doherty combiner whose broadband operation capability has been verified in Section 5.1 simplifies the broadband DPA design problem into the design of broadband sub-amplifiers and broadband input power divider. The DPA was aimed to operate in the octave-bandwidth ranging from 0.9 to 1.8 GHz. Appropriate transistor technology selection is a key requirement in achieving a broadband power amplifier operation. The gallium nitride (GaN) transistors that have low parasitic and efficient operation are strong candidates in designing a broadband amplifier. In this work, the usage of GaN HEMT transistors; CGH40010 and CGH40025 from Cree Inc. (Durham, NC) were chosen in the design of CPA and PPA sections respectively. The asymmetric DPA configuration requires different sized class-AB/C biased devices in the CPA and PPA sections in order to guarantee the full voltage swing and peak power at the output of the class-C biased PPA. The Doherty structure provides the designers with the flexibility of designing the sub-amplifiers for different terminal impedances. The combiner and divider should also be modified with respect to designed impedances of the CPA and PPA. Using the reduced load and source impedances instead of 50 Ω enhances the power and efficiency performances of the broadband PAs. Moreover, the reduced load impedance extends the bandwidth of the DPA by simplifying the output matching network of the PPA. This is due to the fact that the additional component in the output matching network of the PPA that introduces positive phase dispersion narrowed the maximum achievable bandwidth of the DPA [26]. Hence, the CPA and PPA devices were designed to operate into 25 Ω load and source impedances similar to the proposed wideband combiner outlined in Section 5.1.

The class-AB biased CPA whose schematic and performance are given in Figure 5.4 was designed to satisfy optimum power-efficiency performance over the frequency range of 0.9-1.8 GHz. The CPA was designed using 10 W Cree CGH40010 GaN HEMT transistor. The quiescent current of 30 mA was used in both the simulation and measurement phases. The parallel resistor-capacitor used in the input matching network enhanced the stability and gain flatness over the operation frequencies. The load pull analysis and large signal simulations of the designed amplifier was hold on Agilent-ADS simulation tool. The empirical performances possess high conformity with the simulation performances. The implemented CPA performs with an output power of higher than 40 dBm, a drain efficiency of higher than 57% and a gain of higher than 13 dB over the targeted bandwidth of 0.9-1.8 GHz.



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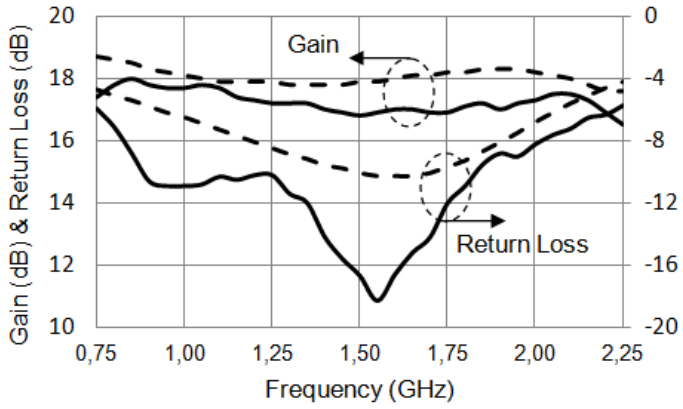

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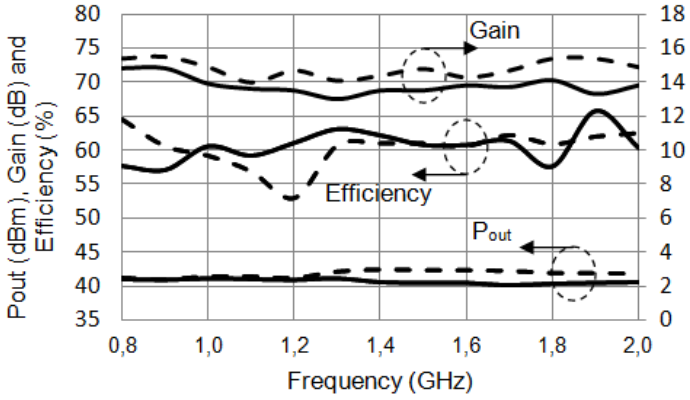
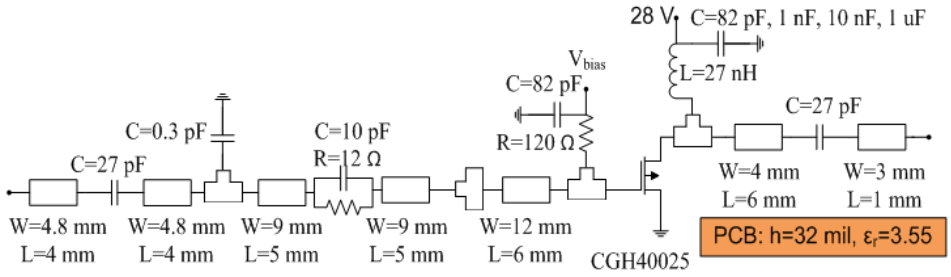


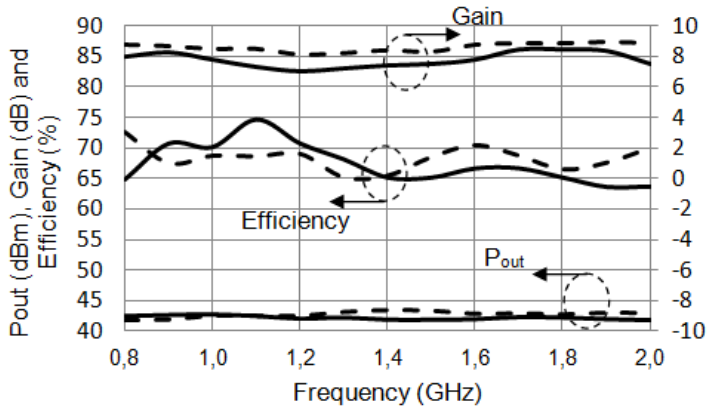
(c)

Figure 5.4 Class-AB Carrier Power Amplifier Operating on 25 Ω Load/Source Impedances and Its Simulated (Dashed Lines) and Measured (Solid Lines) Performances, (a) Circuit Schematic, (b) Small Signal Gain and Return Loss Characteristics, (c) Large Signal Gain, Output Power and Efficiency Characteristics

Similar to the CPA, the PPA design was initialized by the simulation phase on ADS. 25 W Cree CGH40025 GaN HEMT transistor was utilized in design of the PPA. The gate bias voltage of -4.9 V for the peaking device whose pinch-off voltage is -3.1 V was used. The schematic of the designed class-C amplifier, its simulation and empirical performances over the targeted frequency band are shown in Figure 5.5 The implemented PPA achieved an output power of higher than 42 dBm, a drain efficiency of higher than 64% and a gain of higher than 7 dB over the targeted frequency band. The simplified output matching network due to the reduced load impedance of 25 Ω enhances the maximum achievable bandwidth of the resultant DPA.



(a)



(b)

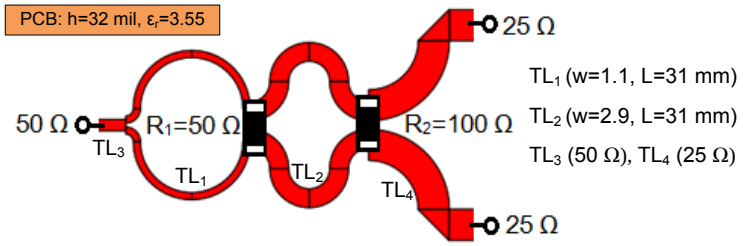
Figure 5.5 Class-C Peaking Power Amplifier Operating on 25 Ω Load/Source Impedances and Its Simulated (Dashed Lines) and Measured (Solid Lines) Performances, (a) Circuit Schematic, (b) Large Signal Gain, Output Power and Efficiency Characteristics

The last building block of the DPA structure is the wideband power divider. Since both the CPA and PPA sections were designed with 25 Ω source impedances, the input divider was also designed to operate from 50 Ω input impedances to 25 Ω output impedances. Two-section Wilkinson divider with modified port impedances was utilized to accomplish this task. The fabricated divider and its measured performance are given in Figure 5.6. The measurement results show that the divider has an insertion loss of lower than 0.4 dB, a return loss of higher than 14 dB and an isolation of higher than 17 dB over the targeted frequency band of 0.9-1.8 GHz.

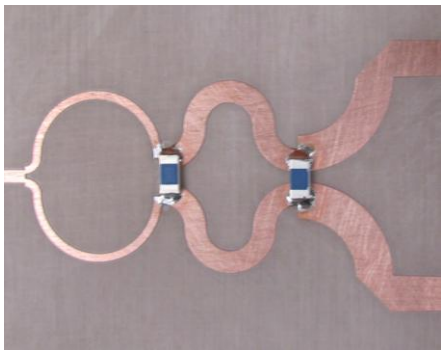
5.3 Implementation of Wideband Asymmetric Doherty Power Amplifier

The wideband Doherty combiner had been designed and fabricated for an ideal Doherty structure in Section 5.1. The output impedance of the inactive PPA has been modeled as open circuit in that verification. However, the inactive PPA represents capacitive output impedance in the low power region of Doherty operation. In order to achieve quasi-open impedance from the PPA, the offset

line is used in conventional Doherty applications. In this study, the quasi-open circuit requirement is also satisfied by the proposed combiner. The measured output impedance of the off-state PPA has been modeled as one-port network and it is used in the optimization of the Doherty combiner. The maximum power load impedances of the CPA and PPA ports have been defined as $Z_{L,MP}$=25 Ω similar to the ideal wideband combiner of Section 5.2. However, as the low power load impedance of the CPA, $Z_{L,LP}$=40+j·25 Ω has been used instead of the conventional usage of $Z_{L,LP}$=2·$Z_{L,MP}$=50 Ω. The load impedance of $Z_{L,LP}$=40+j·25 Ω has been decided upon the wideband simulated efficiency performance of the CPA in the low power region.



(a)



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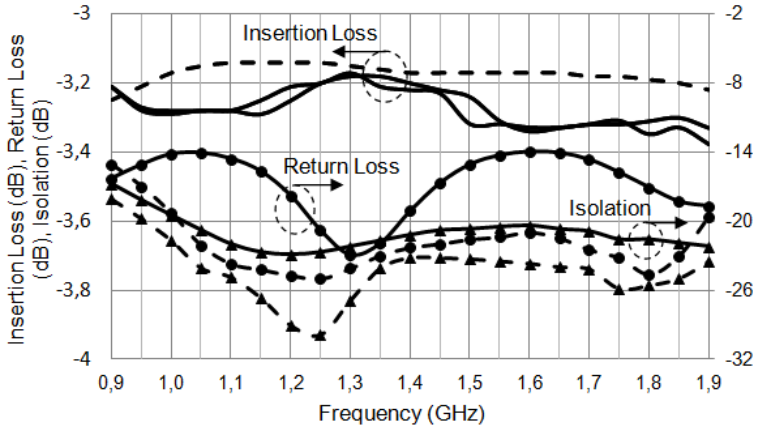
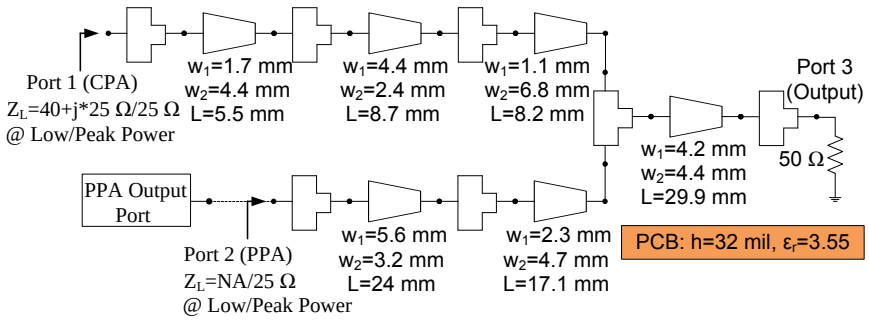
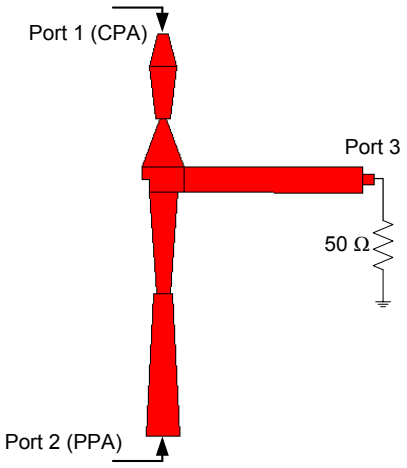


(c)

Figure 5.6 50Ω/25Ω Power Splitter and Its Simulated (Dashed Lines) and Measured (Solid Lines) Performances, (a) Layout, (a) Photograph, (c) Insertion Loss, Return Loss and Isolation Characteristics



(a)



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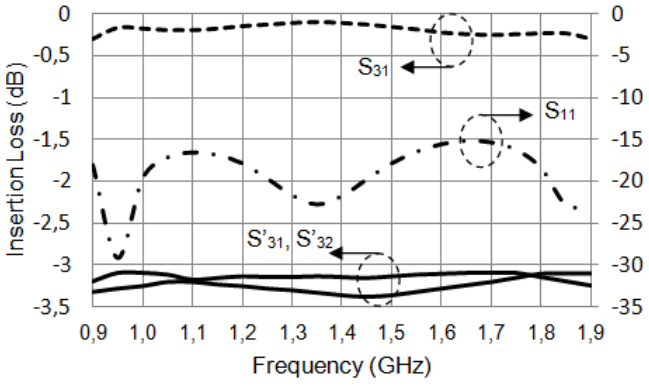
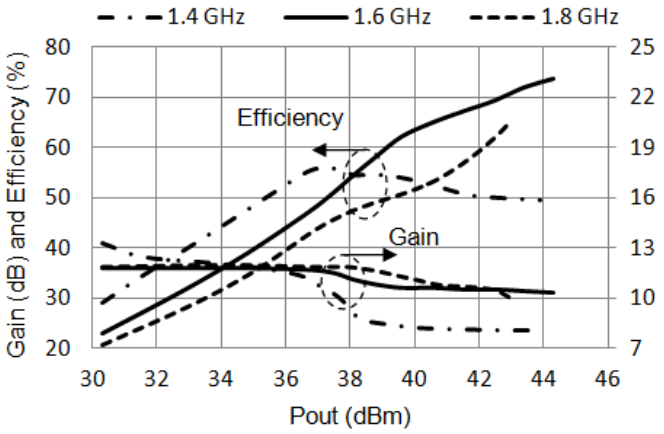
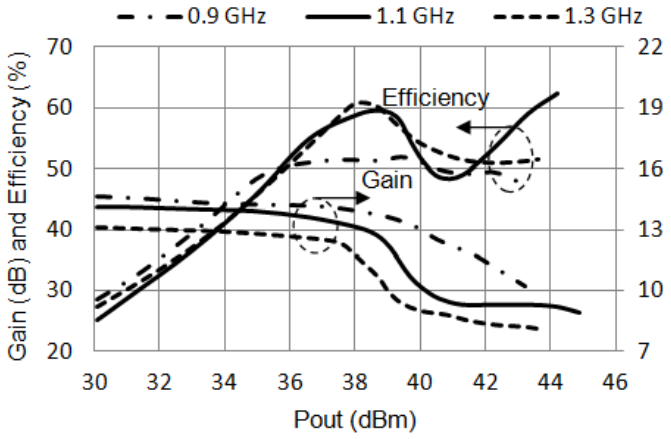


(c)

Figure 5.7 Wideband Doherty Combiner for non-ideal Doherty Structure (a) Optimized Circuit Schematic in 0.9-1.8 GHz, (b) Simulated Layout (c) Low Power Behaviors; Insertion Loss (S_{31}), Return Loss (S_{11}) When Port 2 is Loaded with OFF-State PPA, Port 1 is Matched to 40+j·25 Ω and High Power Behaviors; Combiner Insertion Losses (S'_{31} and S'_{32}) When Port 1 and Port 2 is 25 Ω Loaded



(a)



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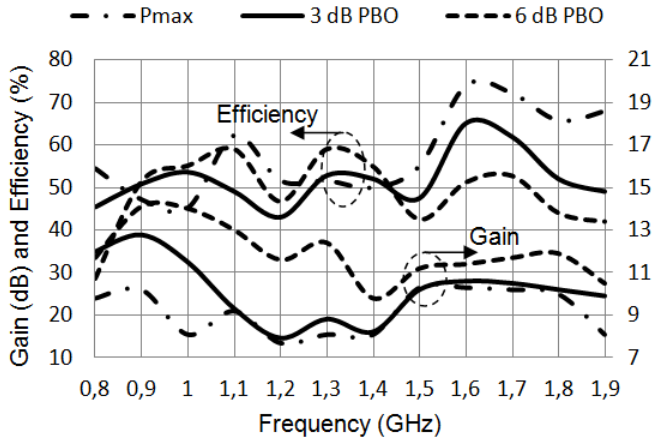
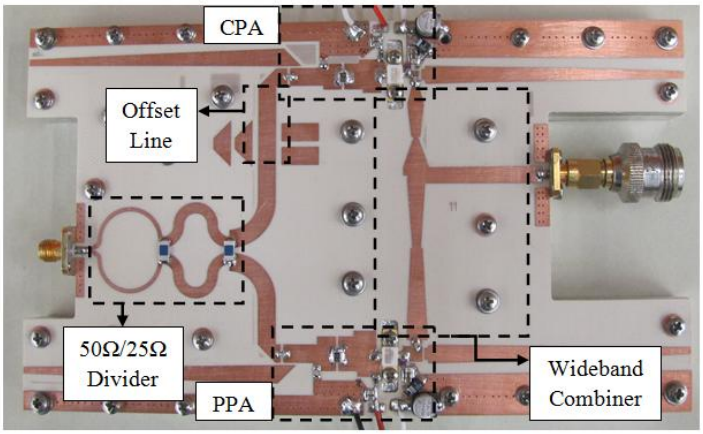


(c)

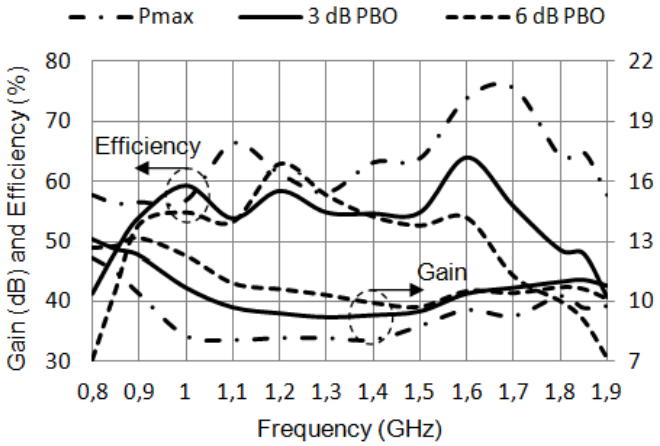
Figure 5.8 Simulated Drain Efficiency and Gain Performances of the Wideband Doherty Power Amplifier, (a) Operating Frequencies of 1.4, 1.6 and 1.8 GHz, (b) Operating Frequencies of 0.9, 1.1 and 1.3 GHz, (c) Power backed-off (PBO) Characteristics over Frequency

The schematic and layout of the optimized wideband Doherty combiner for the targeted frequency band of 0.9-1.8 GHz is given in Figure 5.7 (a), (b). The simulated performance of the modified combiner is given in Figure 5.7 (c). In the low power region where the CPA operates into $Z_{L,LP}$=40+j·25 Ω and the PPA is in off-state, the combiner has an insertion loss (S_{31}) lower than 0.3 dB and a return loss (S_{11}) higher than 15 dB. A combination loss (S'_{31} and S'_{32}) lower than 0.3 dB with an amplitude imbalance of ±0.2 dB has been achieved as the maximum power point operation case.

The modified wideband combiner, wideband power divider, CPA and PPA has been assembled to form an asymmetric DPA in the targeted frequency band of 0.9-1.8 GHz. The offset line of 21 mm prior to the CPA was found to be optimum to satisfy the in-phase power combination at the output of the DPA. The simulation results of the wideband DPA shows promising results in the whole frequency band. The simulated drain efficiency and gain characteristics with 200 MHz frequency steps are given in Figure 5.8 (a) and (b). The drain efficiency and gain performances at different PBO cases; 0-dB, 3-dB and 6-dB, are given in Figure 5. 8 (c). In the simulation phase, a drain efficiency of higher than 43% and a gain of higher than 8 dB in 6 dB PBO region have been achieved in the frequency range from 0.85 to 1.85 GHz.

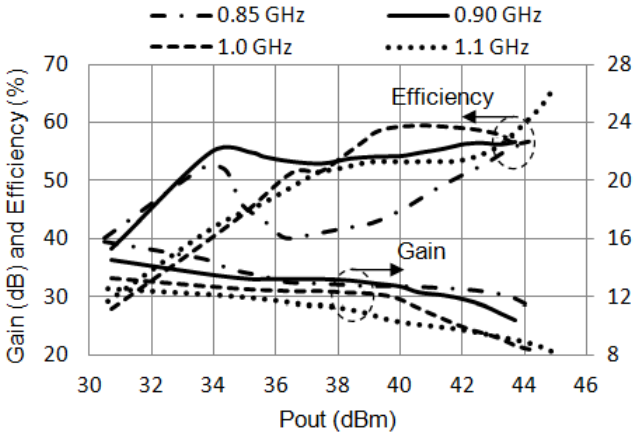


(a)

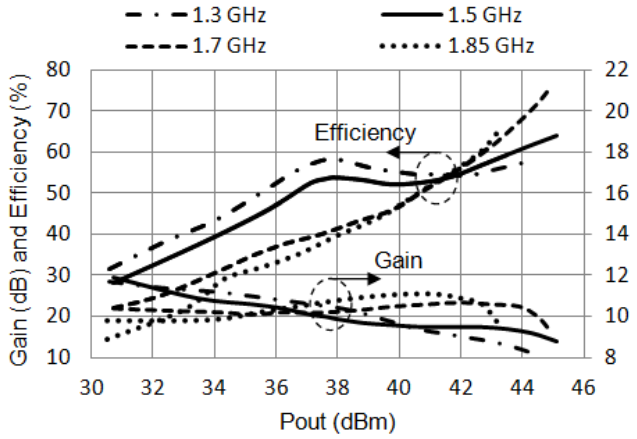


(b)

Figure 5.9 Fabricated Wideband Doherty Power Amplifier and Its Performance Summary, (a) Photograph, (b) Drain Efficiency and Gain Characteristics for Maximum, 3 dB Power Backed-off (PBO) and 6 dB PBO Power Levels



(a)



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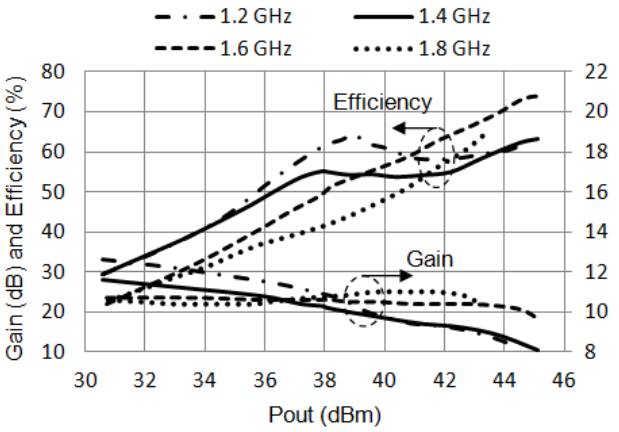
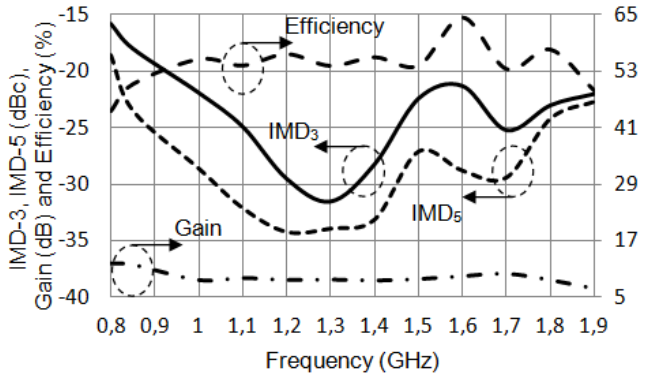


(c)

Figure 5.10 Measured Drain Efficiency and Gain Performances of the Fabricated Wideband Doherty Power Amplifier, (a) Operating Frequencies of 0.85, 0.9, 1.0 and 1.1 GHz, (b) Operating Frequencies of 1.3, 1.5, 1.7 and 1.85 GHz, (c) Operating Frequencies of 1.2, 1.4, 1.6 and 1.8 GHz

The fabricated prototype of the proposed amplifier is shown in Figure 5.9 (a); post-tuning on the simulated structure is not required. The operating points of the class-AB carrier and class-C peaking devices have been set to $I_{DS,CPA}$=30 mA and $V_{GS,PPA}$=-4.9 V respectively. The drain efficiency and gain performances of the fabricated amplifier for different PBO cases are summarized in Figure 5.9 (b). The measurements were taken in the frequency range from 0.8 to 1.9 GHz with a step of 50 MHz. The power dependent drain efficiency and gain characteristics of the amplifier for different operating frequencies between 0.85 GHz and 1.85 GHz are given in Figure 5.10. The proposed wideband DPA delivers an output power of higher than 43.2 dBm in the frequency band ranging from 0.85 to 1.85 GHz. In 6 dB PBO region, it maintains higher than 37% and 52% drain efficiencies across the frequency ranges from 0.85 to 1.85 GHz and 0.9 to 1.6 GHz respectively. The gain of the proposed wideband amplifier is higher than 8 dB in 6 dB PBO region at all operating frequencies.

The linearity properties of the fabricated wideband DPA were characterized by applying the two-tone signal and wideband code-division multiple access (W-CDMA) signal. The third-order and fifth-order inter-modulation distortions (IMD_3 and IMD_5) were measured by applying two-tone signals with 1 MHz frequency spacing. The IMD_3 and IMD_5 performances shown in Figure 5.11 (a) are measured at 3 dB PBO, 41-42 dBm, in the frequency band of 0.8-1.9 GHz with a step of 50 MHz. In the center frequency of 1.35 GHz, the fabricated amplifier maintains -30 dBc IMD_3 and -34 dBc IMD_5 with a drain efficiency of 55%.



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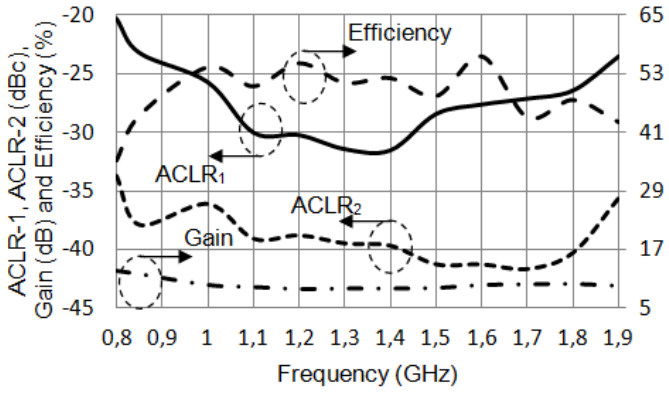

(b)

Figure 5.11 Measured Nonlinearity Performances of the Wideband Doherty Power Amplifier, (a) IMD_3, IMD_5, Efficiency and Gain at 40-41 dBm (3-dB PBO) 2-Tone Average Output Power, (b) $ACLR_1$ (5 MHz offset), $ACLR_2$ (10 MHz offset), Efficiency and Gain at 37-38 dBm (6-dB PBO) Average Output Power.

Linearity performance of this amplifier is considered to be acceptable for the greater-than-octave-bandwidth frequency range of 0.85-1.85 GHz. W-CDMA signal with PAPR of 6.5 dB was applied to observe the adjacent-channel leakage ratio (ACLR) of the amplifier. The $ACLR_1$ (with 5 MHz offset) and $ACLR_2$ (with 10 MHz offset) were measured at 6 dB PBO, 38-39 dBm. The measurement results are given in Figure 5.11 (b). The fabricated amplifier achieves an $ACLR_1$ of -31 dBc and an ACLR2 of -39 dBc at center frequency operation of 1.35 GHz. The related drain efficiency was noted as 51%. The ACLR values measured in such a wideband application is again considered to be acceptable. In order to satisfy the spectral emission mask requirements of the communication standards, there have been many reported promising works with using digital pre-distortion methods.

Table 5.1 summarizes the performance of the fabricated wideband DPA and it compares the performance of the wideband DPA of this study with those present in the literature. The modified DPA of [100] is out of this comparison due to the required external system used to configure the input signals of the CPA and PPA. The widest band DPA in the literature has 41.9% BW with minimum DE of 36% in 6 dB PBO region whereas the fractional BW of 74.1% with DE of higher than 37% has been achieved in this study. Similarly, the most efficient, wideband DPA in the literature has a minimum DE of 52% in the fractional BW of 35.3% whereas the DPA implemented in this study has a DE of higher than 52% in the BW of 56%. This enhancement in the BW is possible because unlike the previous studies that focused on quarter-wave length inverter optimization or matching network optimization, the whole output section of the DPA is interpreted as a special combiner network and the broadband combiner structure is proposed and used to solve the bandwidth limitation problem in this study. Moreover, the reduced load impedance of 25 Ω instead of conventional 50 Ω enhances the fractional BW by reducing the phase dispersion at the output of the PPA in low power region.

Table 5.1 Comparison Of Broadband Doherty Amplifiers In The Literature

Publication Year	Frequency Range (GHz)	BW (%)	Minimum DE (%) in 6 dB PBO Region	Minimum 6 dB PBO P_{out} (dBm)	Technology	Reference
2010	1.7-2.3	30	~35	~36	LDMOS	[17]
2010	1.5-2.14	35.2	33	36.1	GaN	[18]
2011	1.7-2.6	41.9	~36	~36.2	GaN-Asymmetric	[19]
2012	2.2-2.96	29.5	~37	~34.2	GaN	[21]
2012	0.7-1	35.3	~52	-43.2	GaN	[22]
2013	0.85-1.85 (0.9-1.6)	74.1 (56)	37 (52)	37.2 (37.7)	GaN-Asymmetric	This work

CHAPTER VI

CONCLUSIONS AND FUTURE WORK

High-efficiency power amplifiers (PAs) are the key components of modern communication systems; they form the final stage of the transmitters for transmitting high output power signals. Designing an efficient PA has a vital importance especially for the mobile systems to save power and to minimize the complexity of cooling structures. Conventional PAs suffer from the efficiency degradation at the low power levels. The modern communication signals due to their high peak to average power ratios (PAPR), force these amplifiers to work at backed-off region, thus reducing the power efficiency of the transmitter considerably. Most of the mobile electronic warfare systems require moderate linearity but maximum achievable efficiency to deal with power consumption, cooling and battery life problems. Doherty power amplifier (DPA) is a promising technique for improving the efficiency under output power backed-off conditions. The DPA has lower circuit complexity and cost effective implementation with respect to its alternatives. Moreover, the structure of the DPA can be arranged for different PAPR signals. Its operation is based on the active load modulation technique where the peaking device decreases the load impedance seen by the carrier device, as the driving level increases beyond the transition point. In its standard operation, transition point is set at 6 dB output power backed-off level and the carrier power amplifier (CPA) is active at all power levels whereas the peaking power amplifier (PPA) is active only in upper 6 dB power region. The class-B/class-B configured ideal DPA that was proposed by W. H. Doherty in 1936 was analyzed in terms of efficiency by F. H. Raab in 1987. However, class-B/class-B realization using solid-state transistors require driving level controlled attenuator which should have a special behavior of being shaped at least in two distinct regions with highly nonlinear characteristics. In an alternative usage of DPA with solid state transistors, the CPA is biased in class-B and the PPA is biased in class-C so that it turns on the transition point. However, conventional symmetrical Doherty power amplifier (SDPA) in which the CPA and PPA employ the same periphery transistors result in reduced maximum output power due to the lack of full load modulation at the maximum drive level. In order to improve the performance of class-B/class-C SDPA, different techniques have been proposed and implemented. The most common DPA implementations propose the use of bias adaptation or the use of asymmetrical device in the PPA section.

In this study, the modified DPA utilizing gate bias adaptation without requiring different periphery devices or uneven power dividers has been analyzed in terms of efficiency with a novel technique. The ideal efficiency characteristics of bias adapted DPA (BA-DPA) with different bias adaptation schemes have been illustrated. The derived analytical expression of efficiency in load modulation region indicated that, with various bias adaptation shapes, efficiency characteristic with smaller deeps over ideal DPA can be achieved in load modulation region. Moreover, the maximum conduction angle and periphery requirement of the class-C biased PPA to realize fully load modulated asymmetrical DPA (ADPA) have been investigated. The appropriate maximum conduction angles and relative peripheries for the PPA have evaluated for different load modulation regions. The ideal efficiency characteristic of ADPA with adequate periphery devices has been illustrated in comparison to the classical DPA and BA-DPA. The design optimization of the ADPA and BA-DPA has been presented for maximum efficiency criteria in the load modulation region. The BA-DPA and ADPA have been designed and implemented based on the analytical findings. The implemented amplifiers maintain 50 dBm output power with nearly 60% drain efficiencies in 6 dB load modulation region.

In addition, for the first in the literature, this study represents the performance comparison of two common DPA techniques; ADPA and BA-DPA, under the same conditions in terms of the output power, operation frequency and employed transistor technology. The advantages and drawbacks of the DPAs based on the simulated and measured performances of the implemented amplifiers have been concluded. Both amplifiers have presented well enhanced efficiency and acceptable linearity

over the conventional symmetric DPA and class-B amplifier. The efficiency characteristic of the bias adapted DPA which is closer to the ideal operation has been noted. Although it has simple, cost effective implementation and sufficient bandwidth for most of the current communication systems, the band limited control circuit has been noted as the fundamental drawback of the BA-DPA structure. The lower gain at the modulation region, and a waste of periphery in the peaking device which leads to matching problem of low impedances, have been mentioned as the main drawbacks of ADPA.

Although the DPA offers superior efficiency and inherent linearity performances, the narrowband operation is accepted as a fundamental weakness of the structure. In modern communication era, wireless communication systems require radio transmitters to operate over a wide frequency range providing multiband multimode operation. The modern communication standards have wider bandwidth up to 100 MHz and higher peak-to-average power ratio (PAPR) up to 12 dB due to high data rates used in the spectrally efficient digital modulation schemes. One of the key elements of such transmitters is the wideband power amplifier (PA). High PAPR signals force the PAs to work at power backed-off region, thus reducing the power efficiency of the conventional transmitters considerably. In addition, many electronic warfare systems such as jammers and electronic attack systems also require multimode and multiband operation when the transmission of older communication standards is needed for backward compatibility. Multimode operation force the PAs to operate in wide output power range with peak efficiency in order to save limited line power. Therefore, the requirement on the PAs of modern transmitters are designated as operating on wide frequency range and maintaining high efficiency in a wide output power range. Using dual-band or broadband design techniques provide the systems with the capability of operating on multiband standards and covering many communication frequency bands with the least number of devices eliminating the redundant hardware. The conventional balanced broadband PAs which use broadband class-A/-AB PAs and 90°, 3dB hybrids are offered as octave bandwidth devices by many manufacturers in the market. However, the conventional linear PAs are optimized to operate at the specific maximum output power with a fixed supply voltage and optimized load impedance. Hence, they exhibit poor efficiency performance in back-off power levels. Since the DPA has its low hardware complexity, a wide aggregated instantaneous bandwidth and tunable efficiency characteristic for different power ranges, it would be a strong candidate for multimode multiband operation if the band limitation problem of the structure is solved.

In the scope of this study, a new Doherty amplifier structure with an octave bandwidth characteristic has been presented based on the proposed combination method. A novel combiner that solves the fundamental bandwidth limitation problems of a conventional Doherty structure has been introduced. It achieves the required load transformation function of the carrier amplifier by the peaking amplifier in load modulation region by taking the boundary operation conditions of the conventional Doherty combiner structure at the transition and peak power points into consideration. Moreover, the proposed combiner removes the requirement of an extra offset line in front of the peaking amplifier. The proposed combiner simplifies the bandwidth limitation problem of the Doherty amplifier into the wideband design of the carrier amplifier, peaking amplifier and the input power divider. The conceptual implementation of the proposed combiner has been verified by achieving an octave bandwidth operation ranging from 1 to 2 GHz.

For the verification of an octave bandwidth Doherty amplifier, a carrier and a peaking amplifier with 25 Ω terminal impedances, and a wideband input divider from 50 Ω to 25 Ω terminal impedances have been designed optimally in the frequency band ranging from 0.9 to 1.8 GHz. After the optimization of the proposed output combiner in 0.9-1.8 GHz frequency band, an asymmetric Doherty amplifier has been designed and implemented. The implemented asymmetric Doherty amplifier structure has represented higher than 52% and 37% drain efficiencies through 6 dB PBO region in the operation frequency of 0.9-1.6 GHz and 0.85-1.85 GHz respectively. The implemented DPA also represents acceptable linearity performance for such a wideband amplifier. In two-tone signal characterization, the amplifier represents an IMD_3 of -30 dBc at a drain efficiency of 55% at the center operation frequency. In a single-carrier W-CDMA operation mode with a PAPR of 6.5 dB, a drain efficiency of 51% has been achieved with an ACLR of –31 dBc. This thesis work represents the most wideband Doherty amplifier published in the literature. Acceptable wideband nonlinearity characteristics can be further improved applying linearization techniques such as feedforward or pre-distortion. By using the proposed structure, all the current

third-generation (3G) and fourth-generation (4G) frequency bands can be covered using only two amplifiers operating on 0.7-1.4 GHz and 1.4-2.8 GHz frequency bands respectively.

As a future work of this study, the optimum linearity enhancement method specialized to the DPA should be investigated. Although, the linearity of the DPA is conserved in theoretical sense, the sufficient IMD cancellation by proper gate biasing is not possible due to strong memory effect. Moreover, the modern wireless communication standards impose higher linearity requirements to the systems in order to reduce the adjacent channel leakages. Similar to the other topologies, without the use of an appropriate linearization method, the DPA cannot satisfy the spectral emission mask requirements of the modern wireless communication standards. The most recent researches have concluded that the DPA used with a digital pre-distortion or feedforward techniques can achieve the current linearity requirements [23], [102]. However, since the feedforward structure reduces the overall efficiency performance, the pre-distortion techniques are accepted to be the best linearization method of the DPA. The simultaneous usage of the pre-distortion and DPA structure offers the today's best amplification topology ensuring the superior efficiency and linearity performances. The modern communication signals having wide aggregated bandwidths and high PAPRs enhance the depth of electrical memory and thermal memory. The pre-distortion method based on the memory polynomials or Volterra series is a strong candidate in order to maintain the linearity of the DPA.

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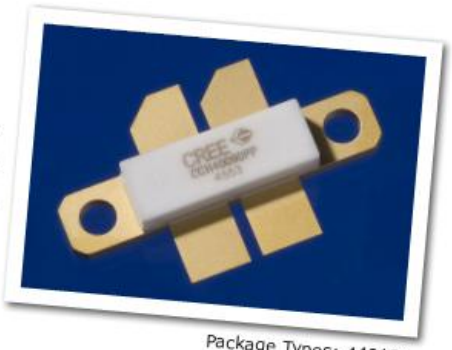
APPENDIX A

DATASHEET OF CGH40090PP

CGH40090PP

90 W, RF Power GaN HEMT

Cree's CGH40090PP is an unmatched, gallium nitride (GaN) high electron mobility transistor (HEMT). The CGH40090PP, operating from a 28 volt rail, offers a general purpose, broadband solution to a variety of RF and microwave applications. GaN HEMTs offer high efficiency, high gain and wide bandwidth capabilities making the CGH40090PP ideal for linear and compressed amplifier circuits. The transistor is available in a 4-lead flange package.



Package Types: 440199
PN: CGH40090PP

Typical Performance Over 500 MHz - 2.5 GHz (T_c = 25 °C) of Demonstration Amplifier

Parameter	500 MHz	1.0 GHz	1.5 GHz	2.0 GHz	2.5 GHz	Units
Small Signal Gain	17.6	15.6	14.1	12.4	12.4	dB
Gain at P_{SAT}	13.7	11.7	9.2	7.0	10.4	dB
Saturated Power	66.8	102.7	91.4	101.7	57.0	W
Drain Efficiency at P_{SAT}	48.5	57.0	56.6	59.2	37.3	%
Input Return Loss	7.3	23.0	14.9	14.3	11.3	dB

Features

- Up to 4 GHz Operation
- 16 dB Small Signal Gain at 2.0 GHz
- 12 dB Small Signal Gain at 4.0 GHz
- 100 W Typical P_{SAT}
- 55 % Efficiency at P_{SAT}
- 28 V Operation
- Use as a Pair of 45 W Transistors

Absolute Maximum Ratings (not simultaneous) at 25°C Case Temperature

Parameter	Symbol	Rating	Units
Drain-Source Voltage	V_{DSS}	84	Volts
Gate-to-Source Voltage	V_{GS}	-10, +2	Volts
Storage Temperature	T_{STG}	-55, +150	°C
Operating Junction Temperature	T_J	225	°C
Maximum Forward Gate Current	I_{GMAX}	28	mA
Soldering Temperature[1]	T_S	245	°C
Screw Torque	τ	80	in-oz
Thermal Resistance, Junction to Case[2]	$R_{\theta JC}$	1.45	°C/W
Case Operating Temperature[2,3]	T_C	-40, +85	°C

Note:
[1] Refer to the Application Note on soldering at www.cree.com/products/wireless_appnotes.asp
[2] Measured for the CGH40090PP at P_{DISS} = 112W.
[3] See also, the Power Dissipation De-rating Curve on Page 5.

Electrical Characteristics (T_C = 25°C)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Conditions
DC Characteristics[1]						
Gate Threshold Voltage	$V_{GS(th)}$	-3.8	-3.3	-2.3	VDC	V_{DS} = 10 V, I_D = 28.8 mA
Gate Quiescent Voltage	$V_{GS(Q)}$	–	-3.0	–	VDC	V_{DS} = 28 V, I_D = 1.0 A
Saturated Drain Current[2]	I_{DS}	23.2	28.0	–	A	V_{DS} = 6.0 V, V_{GS} = 2.0 V
Drain-Source Breakdown Voltage	V_{BR}	84	100	–	VDC	V_{GS} = -8 V, I_D = 28.8 mA
RF Characteristics[3,4] (T_C = 25°C, F_0 = 2.0 GHz unless otherwise noted)						
Small Signal Gain	G_{SS}	11.5	12.5	–	dB	V_{DD} = 28 V, I_{DQ} = 1.0 A
Power Output at Saturation[5]	P_{SAT}	80	100	–	W	V_{DD} = 28 V, I_{DQ} = 1.0 A
Drain Efficiency[6]	η	45	55	–	%	V_{DD} = 28 V, I_{DQ} = 1.0 A, P_{OUT} = P_{SAT}
Output Mismatch Stress	VSWR	–	10 : 1	–	Ψ	No damage at all phase angles, V_{DD} = 28 V, I_{DQ} = 1.0 A, P_{OUT} = 90 W CW
Dynamic Characteristics						
Input Capacitance	C_{GS}	–	32.5	–	pF	V_{DS} = 28 V, V_{GS} = -8 V, f = 1 MHz
Output Capacitance	C_{DS}	–	8.9	–	pF	V_{DS} = 28 V, V_{GS} = -8 V, f = 1 MHz
Feedback Capacitance	C_{GD}	–	1.2	–	pF	V_{DS} = 28 V, V_{GS} = -8 V, f = 1 MHz

Notes:
[1] Measured on wafer prior to packaging.
[2] Scaled from PCM data.
[3] Measured in CGH40090PP-TB.
[4] I_{DQ} of 1.0 A is by biasing each device at 0.5 A.
[5] P_{SAT} is defined as: Q1 or Q2 = I_G = 14 mA.
[6] Drain Efficiency = P_{OUT} / P_{DC}

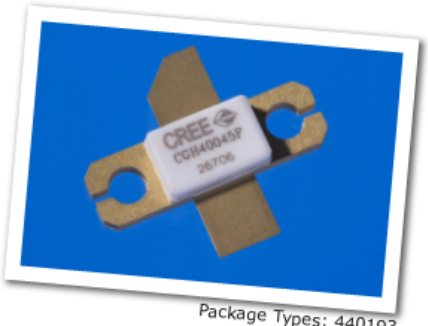
APPENDIX B

DATASHEET OF CGH40045

CGH40045

45 W, RF Power GaN HEMT

Cree's CGH40045 is an unmatched, gallium nitride (GaN) high electron mobility transistor (HEMT). The CGH40045, operating from a 28 volt rail, offers a general purpose, broadband solution to a variety of RF and microwave applications. GaN HEMTs offer high efficiency, high gain and wide bandwidth capabilities making the CGH40045 ideal for linear and compressed amplifier circuits. The transistor is available in a flange package.



Package Types: 440193
PN: CGH40045F

FEATURES

- Up to 4 GHz Operation
- >16 dB Small Signal Gain at 2.0 GHz
- 12 dB Small Signal Gain at 4.0 GHz
- 55 W Typical P_{3dB}
- 55 % Efficiency at P3dB
- 28 V Operation

APPLICATIONS

- 2-Way Private Radio
- Broadband Amplifiers
- Cellular Infrastructure
- Test Instrumentation
- Class A, AB, Linear amplifiers suitable for OFDM, W-CDMA, EDGE, CDMA waveforms

RoHS COMPLIANT

Absolute Maximum Ratings (not simultaneous) at 25°C Case Temperature

Parameter	Symbol	Rating	Units
Drain-Source Voltage	V_{DSS}	84	Volts
Gate-to-Source Voltage	V_{GS}	-10, +2	Volts
Storage Temperature	T_{STG}	-55, +150	°C
Operating Junction Temperature	T_J	175	°C
Maximum Forward Gate Current	I_{GMAX}	15	mA
Soldering Temperature	T_S	225	°C
Screw Torque	T	80	in-oz
Thermal Resistance, Junction to Case [1]	$R_{\theta JC}$	2.7	°C/W

Note:
[1] Measured for the CGH40045F at 43W P_{DISS}.

Electrical Characteristics (T_C = 25°C)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Conditions
DC Characteristics[2]						
Gate Threshold Voltage	$V_{GS(th)}$	-3.0	-2.5	-1.8	VDC	V_{DS} = 10 V, I_D = 14.4 mA
Gate Quiescent Voltage	$V_{GS(Q)}$	–	-2.3	–	VDC	V_{DS} = 28 V, I_D = 400 mA
Saturated Drain Current[3]	I_{DS}	9.6	10.8	–	A	V_{DS} = 6.0 V, V_{GS} = 2.0 V
Drain-Source Breakdown Voltage	V_{BR}	84	100	–	VDC	V_{GS} = -8 V, I_D = 14.4 mA
Case Operating Temperature[4]	T_C	-10	–	+60	°C	P_{DISS} = 43 W
RF Characteristics (T_C = 25°C, F_0 = 2.5 GHz unless otherwise noted)						
Small Signal Gain	G_{SS}	12.5	14	–	dB	V_{DD} = 28 V, I_{DQ} = 400 mA
Power Output at 3 dB Compression	P_{3dB}	45	55	–	W	V_{DD} = 28 V, I_{DQ} = 400 mA
Drain Efficiency[1]	η	45	55	–	%	V_{DD} = 28 V, I_{DQ} = 400 mA, P_{OUT} = P_{3dB}
Output Mismatch Stress	VSWR	–	TBD	–	Ψ	No damage at all phase angles, V_{DD} = 28 V, I_{DQ} = 400 mA, P_{OUT} = 45 W CW
Dynamic Characteristics						
Input Capacitance	C_{GS}	–	19.3	–	pF	V_{DS} = 28 V, V_{gs} = -8 V, f = 1 MHz
Output Capacitance	C_{DS}	–	4.6	–	pF	V_{DS} = 28 V, V_{gs} = -8 V, f = 1 MHz
Feedback Capacitance	C_{GD}	–	1.7	–	pF	V_{DS} = 28 V, V_{gs} = -8 V, f = 1 MHz

Notes:
[1] Drain Efficiency = P_{OUT} / P_{DC}
[2] Measured on wafer prior to packaging.
[3] Scaled from PCM data.
[4] See also, the Power Dissipation De-rating Curve on Page 4.

APPENDIX C

DATASHEET OF CGH40120

CGH40120F

120 W, RF Power GaN HEMT

Cree's CGH40120F is an unmatched, gallium nitride (GaN) high electron mobility transistor (HEMT). The CGH40120F, operating from a 28 volt rail, offers a general purpose, broadband solution to a variety of RF and microwave applications. GaN HEMTs offer high efficiency, high gain and wide bandwidth capabilities making the CGH40120F ideal for linear and compressed amplifier circuits. The transistor is available in a flange package.

Package Types: 440193
PN: CGH40120F

FEATURES

- Up to 4 GHz Operation
- 20 dB Small Signal Gain at 1.0 GHz
- 15 dB Small Signal Gain at 2.0 GHz
- 120 W Typical P_{SAT}
- 70 % Efficiency at P_{SAT}
- 28 V Operation

APPLICATIONS

- 2-Way Private Radio
- Broadband Amplifiers
- Cellular Infrastructure
- Test Instrumentation
- Class A, AB, Linear amplifiers suitable for OFDM, W-CDMA, EDGE, CDMA waveforms

RoHS COMPLIANT

Absolute Maximum Ratings (not simultaneous) at 25°C Case Temperature

Parameter	Symbol	Rating	Units
Drain-Source Voltage	V_{DSS}	84	Volts
Gate-to-Source Voltage	V_{GS}	-10, +2	Volts
Storage Temperature	T_{STG}	-55, +150	°C
Operating Junction Temperature	T_J	225	°C
Maximum Forward Gate Current	I_{GMAX}	30	mA
Soldering Temperature[1]	T_S	245	°C
Screw Torque	τ	80	in-oz
Thermal Resistance, Junction to Case[2]	$R_{\theta JC}$	1.5	°C/W
Case Operating Temperature[2,3]	T_C	-40, +85	°C

Note:
[1] Refer to the Application Note on soldering at www.cree.com/products/wireless_appnotes.asp
[2] Measured for the CGH40120F at P_{DISS} = 112 W.
[3] See also, the Power Dissipation De-rating Curve on Page 7.

Electrical Characteristics (T_C = 25°C)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Conditions
DC Characteristics[1]						
Gate Threshold Voltage	$V_{GS(TH)}$	-3.8	-3.3	-2.3	VDC	V_{DS} = 10 V, I_D = 28.8 mA
Gate Quiescent Voltage	$V_{GS(Q)}$	-	-3.0	-	VDC	V_{DS} = 28 V, I_D = 1.0 A
Saturated Drain Current[2]	I_{DS}	23.2	28.0	-	A	V_{DS} = 6.0 V, V_{GS} = 2.0 V
Drain-Source Breakdown Voltage	V_{BR}	84	100	-	VDC	V_{GS} = -8 V, I_D = 28.8 mA
RF Characteristics[3] (T_C = 25°C, F_0 = 1.3 GHz unless otherwise noted)						
Small Signal Gain	G_{SS}	17.5	19	-	dB	V_{DD} = 28 V, I_{DQ} = 1.0 A
Power Output[4]	P_{SAT}	100	120	-	W	V_{DD} = 28 V, I_{DQ} = 1.0 A
Drain Efficiency[5]	η	60	70	-	%	V_{DD} = 28 V, I_{DQ} = 1.0 A, P_{OUT} = P_{SAT}
Output Mismatch Stress	VSWR	-	10 : 1	-	Ψ	No damage at all phase angles, V_{DD} = 28 V, I_{DQ} = 1.0 A, P_{OUT} = 100 W CW
Dynamic Characteristics						
Input Capacitance	C_{GS}	-	33	-	pF	V_{DS} = 28 V, V_{gs} = -8 V, f = 1 MHz
Output Capacitance	C_{DS}	-	10	-	pF	V_{DS} = 28 V, V_{gs} = -8 V, f = 1 MHz
Feedback Capacitance	C_{GD}	-	3.0	-	pF	V_{DS} = 28 V, V_{gs} = -8 V, f = 1 MHz

Notes:
[1] Measured on wafer prior to packaging.
[2] Scaled from PCM data.
[3] Measured in CGH40120F-TB.
[4] P_{SAT} is defined as I_G = 2.8 mA.
[5] Drain Efficiency = P_{OUT} / P_{DC}

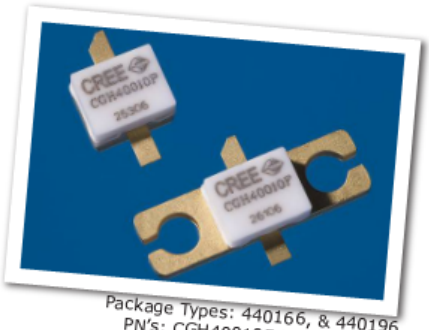
APPENDIX D

DATASHEET OF CGH40010

CGH40010

10 W, RF Power GaN HEMT

Cree's CGH40010 is an unmatched, gallium nitride (GaN) high electron mobility transistor (HEMT). The CGH40010, operating from a 28 volt rail, offers a general purpose, broadband solution to a variety of RF and microwave applications. GaN HEMTs offer high efficiency, high gain and wide bandwidth capabilities making the CGH40010 ideal for linear and compressed amplifier circuits. The transistor is available in both screw-down, flange and solder-down, pill packages.



Package Types: 440166, & 440196
PN's: CGH40010F & CGH40010P

FEATURES

- Up to 4 GHz Operation
- 16 dB Small Signal Gain at 2.0 GHz
- 14 dB Small Signal Gain at 4.0 GHz
- 13 W typical P_{3dB}
- 65 % Efficiency at P3dB
- 28 V Operation

APPLICATIONS

- 2-Way Private Radio
- Broadband Amplifiers
- Cellular Infrastructure
- Test Instrumentation
- Class A, AB, Linear amplifiers suitable for OFDM, W-CDMA, EDGE, CDMA waveforms

RoHS COMPLIANT

Absolute Maximum Ratings (not simultaneous) at 25°C Case Temperature

Parameter	Symbol	Rating	Units
Drain-Source Voltage	V_{DSS}	84	Volts
Gate-to-Source Voltage	V_{GS}	-10, +2	Volts
Storage Temperature	T_{STG}	-55, +150	°C
Operating Junction Temperature	T_J	175	°C
Maximum Forward Gate Current	I_{GMAX}	4.0	mA
Soldering Temperature	T_S	245	°C
Thermal Resistance, Junction to Case [1]	$R_{\theta JC}$	5.0	°C/W
Screw Torque	T	60	in-oz

Note:
[1] Measured for the CGH40010F at P_{DISS} = 14 W.

Electrical Characteristics (T_C = 25°C)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Conditions
DC Characteristics[4]						
Gate Threshold Voltage	$V_{GS(th)}$	-3.0	-2.5	-1.8	VDC	V_{DS} = 10 V, I_D = 3.6 mA
Gate Quiescent Voltage	$V_{GS(Q)}$	–	-2.0	–	VDC	V_{DS} = 28 V, I_D = 200 mA
Saturated Drain Current	I_{DS}	2.4	2.7	–	A	V_{DS} = 6.0 V, V_{GS} = 2.0 V
Drain-Source Breakdown Voltage	V_{BR}	84	100	–	VDC	V_{GS} = -8 V, I_D = 3.6 mA
Case Operating Temperature	T_C	-10	–	+105	°C	
RF Characteristics (T_C = 25°C, F_0 = 3.7 GHz unless otherwise noted)						
Small Signal Gain	G_{SS}	12.5	14.5	–	dB	V_{DD} = 28 V, I_{DQ} = 200 mA
Power Output at 3 dB Compression	P_{3dB}	10	12.5	–	W	V_{DD} = 28 V, I_{DQ} = 200 mA
Drain Efficiency[1,2]	η	55	65	–	%	V_{DD} = 28 V, I_{DQ} = 200 mA, P_{3dB}
Output Mismatch Stress	VSWR	–	TBD	–	Ψ	No damage at all phase angles, V_{DD} = 28 V, I_{DQ} = 200 mA, P_{OUT} = 12 W CW
Dynamic Characteristics						
Input Capacitance	C_{GS}	–	5.00	–	pF	V_{DS} = 28 V, V_{gs} = -8 V, f = 1 MHz
Output Capacitance	C_{DS}	–	1.32	–	pF	V_{DS} = 28 V, V_{gs} = -8 V, f = 1 MHz
Feedback Capacitance	C_{GD}	–	0.43	–	pF	V_{DS} = 28 V, V_{gs} = -8 V, f = 1 MHz

Notes:
[1] Drain Efficiency = P_{OUT} / P_{DC}
[2] When tuned for best efficiency (see the applications chart in this data sheet).
[3] When tuned for best P_{1dB} (see the applications chart in this data sheet).
[4] Measured on wafer prior to packaging.

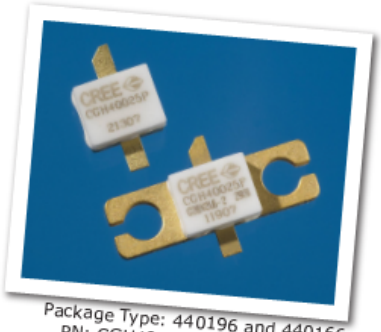
APPENDIX E

DATASHEET OF CGH40025

CGH40025

25 W, RF Power GaN HEMT

Cree's CGH40025 is an unmatched, gallium nitride (GaN) high electron mobility transistor (HEMT). The CGH40025, operating from a 28 volt rail, offers a general purpose, broadband solution to a variety of RF and microwave applications. GaN HEMTs offer high efficiency, high gain and wide bandwidth capabilities making the CGH40025 ideal for linear and compressed amplifier circuits. The transistor is available in a screw-down, flange package and solder-down, pill packages.



Package Type: 440196 and 440166
PN: CGH40025P and CGH40025F

FEATURES

- Up to 4 GHz Operation
- 15 dB Small Signal Gain at 2.0 GHz
- 13 dB Small Signal Gain at 4.0 GHz
- 30 W typical P_{3dB}
- 62 % Efficiency at P3dB
- 28 V Operation

APPLICATIONS

- 2-Way Private Radio
- Broadband Amplifiers
- Cellular Infrastructure
- Test Instrumentation
- Class A, AB, Linear amplifiers suitable for OFDM, W-CDMA, EDGE, CDMA waveforms

RoHS COMPLIANT

Absolute Maximum Ratings (not simultaneous) at 25°C Case Temperature

Parameter	Symbol	Rating	Units
Drain-Source Voltage	V_{DSS}	84	Volts
Gate-to-Source Voltage	V_{GS}	-10, +2	Volts
Storage Temperature	T_{STG}	-55, +150	°C
Operating Junction Temperature	T_J	175	°C
Maximum Forward Gate Current	I_{GMAX}	7.0	mA
Soldering Temperature	T_S	245	°C
Screw Torque	T	60	in-oz
Thermal Resistance, Junction to Case [1]	$R_{\theta JC}$	3.8	°C/W

Note:
[1] Measured for the CGH40025F at P_{DISS} = 28 W.

Electrical Characteristics (T_C = 25°C)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Conditions
DC Characteristics[2]						
Gate Threshold Voltage	$V_{GS(th)}$	-3.0	-2.5	-1.8	VDC	V_{DS} = 10 V, I_D = 7.2 mA
Gate Quiescent Voltage	$V_{GS(Q)}$	–	-2.0	–	VDC	V_{DS} = 28 V, I_D = 250 mA
Saturated Drain Current	I_{DS}	4.8	5.4	–	A	V_{DS} = 6.0 V, V_{GS} = 2.0 V
Drain-Source Breakdown Voltage	V_{BR}	84	100	–	VDC	V_{GS} = -8 V, I_D = 7.2 mA
Case Operating Temperature	T_C	-10	–	+65	°C	
RF Characteristics[3] (T_C = 25°C, F_0 = 3.7 GHz unless otherwise noted)						
Small Signal Gain	G_{SS}	12	13	–	dB	V_{DD} = 28 V, I_{DQ} = 250 mA
Power Output at 3 dB Compression	P_{3dB}	25	30	–	W	V_{DD} = 28 V, I_{DQ} = 250 mA
Drain Efficiency[1]	η	55	62	–	%	V_{DD} = 28 V, I_{DQ} = 250 mA, P_{3dB}
Output Mismatch Stress	VSWR	–	TBD	–	Ψ	No damage at all phase angles, V_{DD} = 28 V, I_{DQ} = 250 mA, P_{OUT} = 12 W CW
Dynamic Characteristics						
Input Capacitance	C_{GS}	–	9.3	–	pF	V_{DS} = 28 V, V_{gs} = -8 V, f = 1 MHz
Output Capacitance	C_{DS}	–	2.0	–	pF	V_{DS} = 28 V, V_{gs} = -8 V, f = 1 MHz
Feedback Capacitance	C_{GD}	–	0.9	–	pF	V_{DS} = 28 V, V_{gs} = -8 V, f = 1 MHz

Notes:
[1] Drain Efficiency = P_{OUT} / P_{DC}
[2] Measured on wafer prior to packaging.
[3] Measured in CGH40025F-TB.

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WORK EXPERIENCE

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FOREIGN LANGUAGES

Advanced English, Basic German

PUBLICATIONS

1. N. Sahan, M.E. Inal, S. Demir and C. Toker, “High power 20-100 MHz Linear and Efficient power amplifier design,” *IEEE Trans. Microw. Theory and Tech*., vol. 6, no. 9, pp. 2032-2039, Sept., 2008.
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AWARDS

1. Technology Development Foundation of Turkey (TTGV), 3. Dr. Akın Çakmakçı Thesis Award 2010.
2. METU Best Thesis of the Year, 2007.
3. Electrical & Electron. Eng. Dept., METU, Dr. Bülent Kerim Altay Award, 2003.
4. Electrical & Electron. Eng. Dept., METU, Dr. Bülent Kerim Altay Award, 2000.

CERTIFICATES

1. Risk Management Training Certificate, by Ministry of National Defense, Ankara-Turkey, 2009.
2. Advanced Power Amplifier Design Tech. Training Certificate, by CEI-EUROPE, Barcelona-Spain, 2004.
3. Measurement and Analysis Training Certificate, by Bilkent University, Ankara-Turkey, 2004.