# INVESTIGATION OF DC BUS CURRENT HARMONICS IN TWO AND THREE LEVEL THREE-PHASE INVERTERS

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Approval of the thesis:

**INVESTIGATION OF DC BUS CURRENT HARMONICS IN TWO AND THREE LEVEL THREE-PHASE INVERTERS**

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## ABSTRACT

INVESTIGATION OF DC BUS CURRENT HARMONICS IN TWO AND THREE LEVEL THREE-PHASE INVERTERS

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Within scope of this work, double-fourier analysis method of rapid calculation and detailed simulation method, which are used to investigate DC bus current harmonics in two level and three level three-phase inverters systematically, will be emphasized and two methods will be compared via applying different modulation techniques. In addition, DC bus currents will be investigated visually for various working conditions and modulation methods. After that, analysis methods will be applied and harmonic spectrums will be determined. After all, it will be showed that calculated harmonic spectrums could be treated as unified harmonics around certain frequencies and these unified harmonics could be reached easily via looking at predetermined table. Moreover, it will also be showed that unified harmonic values could be used to determine harmonic current components that are necessary for sizing DC bus capacitor and could be used in various inverter analysis.



Keywords: fourier, dc bus, current harmonics, inverter, PWM, unified harmonics

# ÖZ

İKİ VE ÜÇ SEVİYELİ ÜÇ FAZLI EVİRİCİLERDE DC BARA AKIMI HARMONİKLERİNİN İNCELENMESİ

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Bu çalışmada, iki ve üç seviyeli üç fazlı eviricilerde DC bara akım harmoniklerinin sistematik bir şekilde incelenmesi için kullanılan ayrıntılı benzetim yöntemi ve hızlı hesap yöntemi olan çift-fourier analitik yöntemi ele alınıp çeşitli modülasyon yöntemleri uygulanarak iki yaklaşım değerlendirilip karşılaştırılacaktır. Çalışmada DC bara akımları çeşitli çalışma koşulları ve modülasyon yöntemleri için görsel olarak incelenecek, ardından analiz yöntemleri uygulanacak ve harmonik spektrumları belirlenecektir. Daha sonra, hesaplanan harmonik spektrumların, belli frekans bölgelerinde birleştirilmiş olarak ele alınabileceği ve önceden oluşturulan tablo ile birleştirilmiş harmonik değerlerine kolayca ulaşılabileceği; birleştirilmiş harmonik değerlerinin, DC bara kondansatörü boyutlandırmada gerekli olan harmonik akımı bileşenlerini belirlemekte ve çeşitli evirici analizlerinde kullanılabileceği gösterilecektir.

Anahtar Kelimeler: fourier, da bara, akım harmonikleri, evirici, DGM, birleştirilmiş harmonik

*To My Family*

*And to the memory of my grandfather, Memiş Çakıllı*

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# INTRODUCTION

## 1.1 Three-Phase Voltage Source Inverters as Applied to AC Motor Drives and PWM Rectifiers

Different kinds of electrical energy sources like renewable energy sources, turbine driven AC generators exist. The distribution system is constructed to deliver this energy to the end user like factory, households, and so on. However, electrical energy must be conditioned in terms of voltage and current to such a degree that can be used by the end user. An example of this process is the conversion between DC sources (renewable energy sources) and AC sources (AC generators and AC distribution system) in order to construct a interconnected system or to drive AC driven machines (industrial motors like induction machine etc.) using DC source. Power electronic conversion devices have been invented for these purposes. Moreover, these power converter circuits improve the system efficiency, controllability and reliability.

There are many types of power converters today and VSI (voltage source inverter) is the mostly used one among them in a range of kilowatt to megawatt and it is used in different applications like industrial, military, and general purpose.

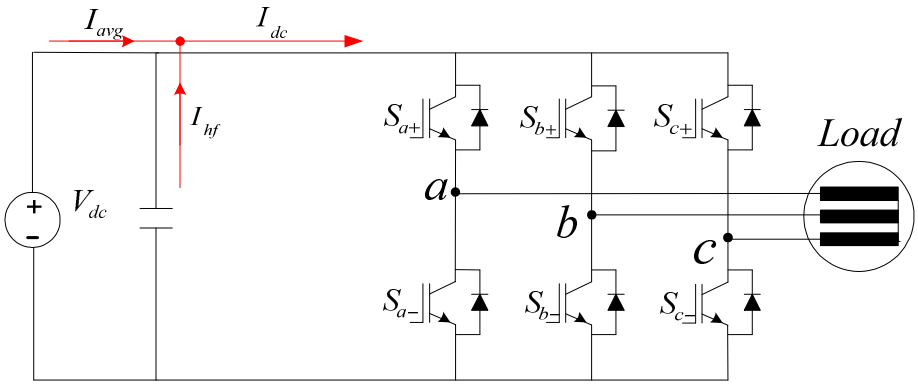


Figure 1.1 The dc bus current and its average and ripple components in the three phase two-level VSI topology

There are different conversion topologies and these can be grouped as four main types. In one application, AC voltage is converted directly to DC voltage and this process is called rectification. In order to minimize the harmonic current injected to the AC source (mains), and to sink sinusoidal current with desired low THD (total harmonic distortion) and with high power factor, the pulse width modulated (PWM) VSI is widely used and this process is shown at first row in Figure 1.2. Another application is the interfacing between renewable sources like photo voltaic panel, hydrogen fuel cell, and end user like residentals, factories or more generally the power system grid. In this interfacing process, the PWM VSI is used to inject very low THD and unity power factor sinusoidal current to the grid. Third application is the conversion from AC voltage to DC voltage via PWM rectifier and reconversion of DC voltage to AC voltage via PWM inverter. This type of application is used in regenerative drives and active filters that need dynamic circulation of energy back and forth through the switches of power converter. Elevator drive system, active power filtering system and UPS system are some examples for the use of this application. Last application is again an AC-DC-AC conversion but with the difference of rectifier stage. In this type, AC-DC conversion is done via diode / thyristor rectifier and used mostly in industrial AC motor drive with the dynamic control of magnitude and frequency of the output AC voltage.

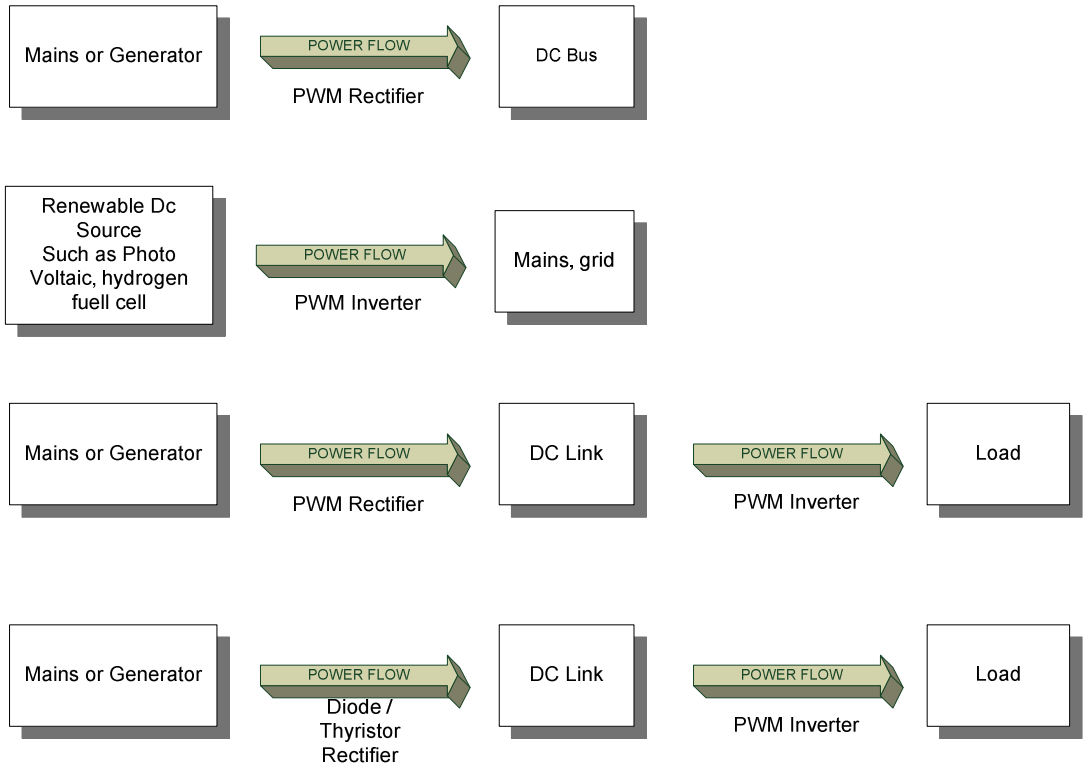


Figure 1.2 Main application types

As seen from the topologies of main application types, the key element of such energy conversion systems is the PWM VSI.

In DC – AC conversion process of the PWM-VSI, the switches are switched at a frequency over 10-20 times of fundamental frequency in order to yield a sinusoidal output voltage or current after a low pass filtering process via LC circuit at the output. Moreover, in applications where there is no neutral return wire like industrial motor drive, some third harmonic patterns are inserted to the pure sinusoidal reference signal (modulation wave) and the magnitude of the pure sinusoidal output voltage per phase is increased as a result of the line to line cancellation of third harmonic voltages. This results in a better usage of DC Bus voltage that is limited. For this purpose and for other technical constraints, different modulation techniques have been invented.

## 1.2 PWM Techniques

Among the various PWM methods existing, the following methods are popular due to their simplicity and performance advantages; sinusoidal PWM (SPWM), space vector PWM (SVPWM), discontinuous PWM (DPWM1) [1], active zero state PWM (AZSPWM1) [2], and near state PWM (NSPWM) [3]. The benefit of SPWM and SVPWM is low ripple at low $M_i$, DPWM1 benefits with low ripple and low loss at high $M_i$, and AZSPWM1 benefits with low common mode voltage and NSPWM benefits with both low common mode voltage and low losses at high $M_i$ [4]. While SPWM, SVPWM and DPWM1 employ a common carrier (triangle), AZSPWM1 and NSPWM employ alternating polarity triangles for each phase [5]. All these methods are easy to implement with modern inverter control chips with advanced PWM generation units. The modulation waves of these methods and the associated carrier signals are shown in Figure 1.3.

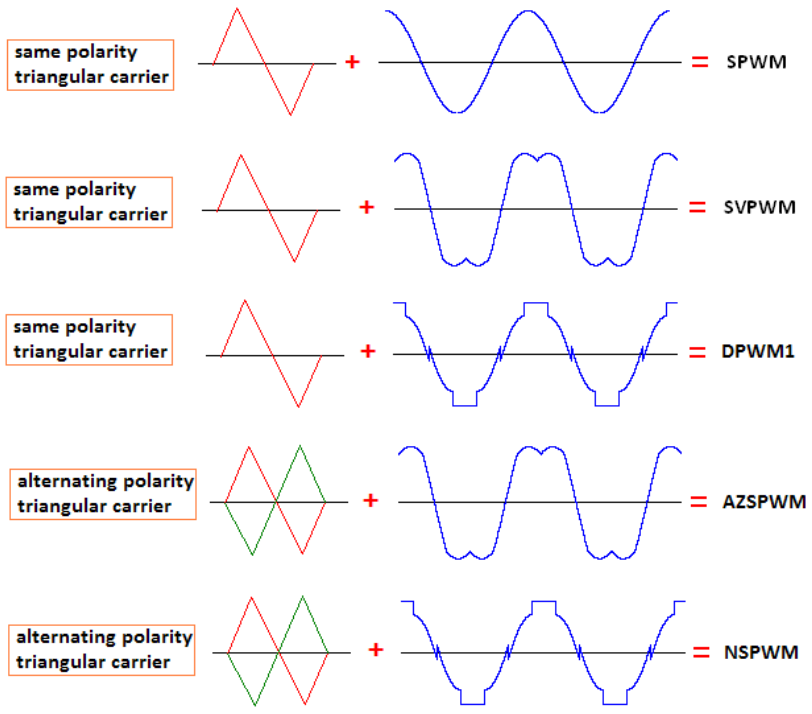


Figure 1.3 Two-level three-phase inverter popular PWM methods; the high frequency carrier waves (left) and the modulation waves (right)

## 1.3 High Frequency Effects of PWM Operation

PWM operation of the VSI effects the input side and the output side of the inverter system via injecting current harmonics at high frequency (carrier frequency and integer multiple of carrier frequency). The output of the inverter is composed of rectangular voltage pulses of which the low pass filtered value is the desired sinusoidal voltage or current. The input side (dc bus side) of the inverter sinks rectangular high frequency currents which must be filtered via dc bus capacitor.

In three-phase inverters, with PWM operation, the inverter input current (dc bus current, $I_{dc}$ in Figure 1.1) consists of high frequency rectangular pulses. The average value $I_{avg}$ comes from the supply, while the harmonic content (ripple current) $I_{hf}$ is bypassed through the dc bus capacitor (filter capacitor). The ripple current frequency spectrum is at the carrier frequency (and its sidebands) and its multiples (and their sidebands). The dc bus PWM ripple current and its spectra depend on the modulation index $M_i$, PWM method, the load (output) current magnitude ($I_{om}$), and the load power factor angle ($\varphi$) (or power factor PF=cos($\varphi$)) [1], [2], [6], [7]-[9]. The dc bus current and its spectra affect the drive performance, thus influence the inverter design both from the dc bus voltage ripple and the dc bus capacitor losses (due to the capacitor equivalent series resistor (ESR) and/or dielectric losses) perspective. Thus, it is important to obtain the detailed dc bus ripple current characteristics for an effective inverter design.

The analysis of the dc bus current ripple has been previously investigated by means of rms ripple value [1], [2], [6] and by means of spectral component calculations [7]-[9] for various PWM methods. The rms ripple value obtained via closed form formulas is easy to use, yet it hides the spectral information, which is necessary in analysis and design. The spectral analysis could be conducted by means of detailed computer simulations (labor and computation intensive with case specific results) or by means of analytical methods, for example the double Fourier integral approach (more general, less computations, but requires math skills) [8]-[9]. While literature based on both rms and spectral methods provide various aspects of the dc

bus current ripple characteristics, comparison based on PWM methods and operating conditions ($M_i$, $\varphi$, $I_{om}$), understanding of the dominant frequency range in terms of ripple and losses, etc. is lacking.

The prime purpose of the dc bus current ripple analysis is the dc bus capacitor design and PWM method selection. However, this analysis by itself is not sufficient to complete the inverter design process. In various inverter applications, different capacitor types are used and each capacitor technology exhibits different ripple and loss attributes and involves different design rules. Thus, the utilization of the dc bus current ripple and spectrum analysis results requires that the capacitor technology is taken into account. For example, electrolytic and film capacitors have different loss mechanisms and different behavior. Therefore, for each type of application a different capacitor type and different design rules should be considered. For this purpose a basic dc bus capacitor technology classification and design issues should be discussed to guide a proper design. The capacitor suppliers/manufacturers usually provide capacitor operating condition data and give empirical design methods for the design engineer [10]-[15]. There is no clear understanding and a rigorous guide to the inverter design in terms of dc bus capacitor ripple and losses. Based on the above discussions it becomes obvious, a clear understanding of the dc bus ripple current characteristics and capacitor design study involves very detailed case by case study for each application.

This thesis work provides an analysis method and graphic tools to overcome these difficulties. In addition to the dc bus current ripple analysis, it also provides a fundamental review of the power electronic capacitor technologies (focused on inverter applications) which is required in the design. Combining the ripple current analysis and the capacitor technology information, it applies the approach to specific examples to be used in inverter design. It yields the information on correct PWM method and correct capacitor sizing, and then correct and simple dc bus capacitor performance prediction for a given application.

## 1.4 Scope of The Thesis

This thesis mainly focuses on the harmonic spectrum analysis of dc bus current of two level VSI at different operating conditions and under various modulation methods. The thesis evaluates the harmonic spectrum microscopically and globally, and then provides frequency-local spectral information (termed as the centered harmonic) that is useful and simple for dc bus ripple performance evaluation.

The second contribution involves a 3D harmonic analysis graph that can be used as a quick design guide which gives dc bus current harmonic spectrum up to the fourth integer multiple of switching frequency over various modulation index and output power factor operating points for all five types of modulation methods. With the help of this graphic, the choice of appropriate PWM method for a specific inverter application becomes easily visible. Likewise, performance evaluation with simple calculations becomes possible.

The final contribution of the thesis is the algorithm for the selection of dc bus capacitor for different applications and an estimation of the ripple over dc bus voltage.

In the 2$^{nd}$ chapter, a summary of different application topologies using the PWM-VSI will be given.

In the 3$^{rd}$ chapter, dc bus current ripple of VSI will be thoroughly studied; ripple current characteristics depending on the operating point and PWM technique utilized will be examined. The microscopic (per PWM cycle), the rms, and spectral components will be discussed for various PWM method and operating conditions. The double Fourier analysis approach will be briefly reviewed and utilized to generate the spectral data. Then the equivalent centered harmonic approach will be proposed and its results will be demonstrated. After the introduction of the method, the design stage will be elaborated on. Moreover, PWM methods in terms of dc bus ripple performance will be compared.

In the 4th chapter, power electronic capacitors are reviewed and the film and electrolytic capacitors suitable for PWM-VSI application are investigated in detail.

In the 5th chapter, different design examples are introduced on application basis. After that, a rectifier system simulation results are demonstrated and they are compared with analytical calculation results. Moreover, output current harmonic is studied with some simulation examples.

In the 6th chapter, experimental results for dc bus current spectra for various loads and operating conditions will be evaluated and compared with the calculation based methods.

In the 7th chapter, DC Bus current harmonic spectrum calculation of three level inverters will be briefly discussed as an extension of the developed technique to more advanced inverter topologies.

In the 8th chapter, all the work will be summed up and future work recommended.

# CHAPTER 2

# TOPOLOGIES AND BASIC APPLICATIONS

## 2.1 Introduction

PWM VSIs are widely used in energy conversion applications with their high efficiency and low distortion characteristics. They are used as rectifier, inverter or both of them depending on the desired direction of power flow for the given application. Moreover, PWM VSIs can be used as the inverter side of rectifier / inverter cascaded system that contains diode / thyristor rectifier stage that interfaces the dc link with the mains.

As mentioned in Chapter 1, application types can be grouped in four main types in which the circulation path and magnitude – frequency relation of high frequency dc bus current differ. The mentioned three-phase power conversion topologies and their dc bus current characteristics will be explained in the following sections. In the simulations of these topologies, the peak of the sinusoidal input or output current of PWM converter side of these topologies is 100A per phase.

## 2.2 PWM Rectifier

PWM rectifiers are increasingly utilized in applications with constant dc bus voltage requirement, typically feed passive loads. PWM rectifiers have the same $I_{dc}$ harmonic characteristics with the PWM inverters, however, they have some differences such as the usage of freewheeling diodes of inverter switches and the direction of power flow which is from AC side to DC side. High frequency

component of dc link current ($I_{hf}$) circulates between switches and the dc bus capacitor as seen in Figure 2.1 and the harmonic spectrum of $I_{dc}$ is seen in Figure 2.2 for a given operating condition in which the dominant current harmonic is located at double $f_s$ (30 kHz). The magnitude of the spectrum decreases with the increasing frequency.

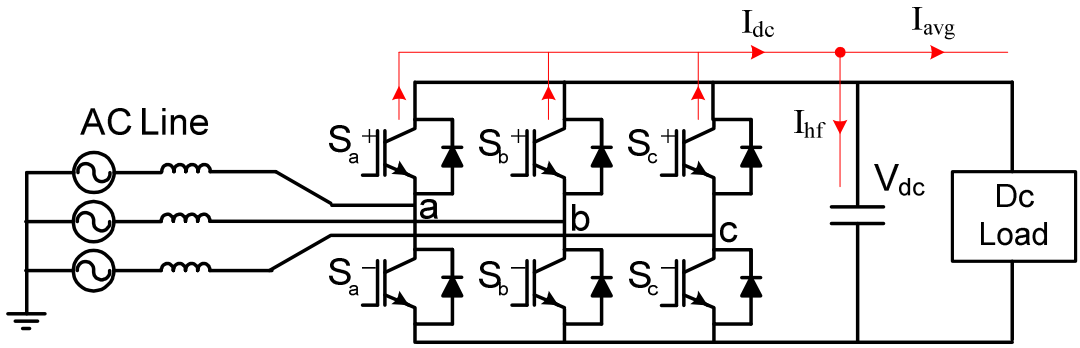


Figure 2.1 PWM rectifier topology and the current distribution

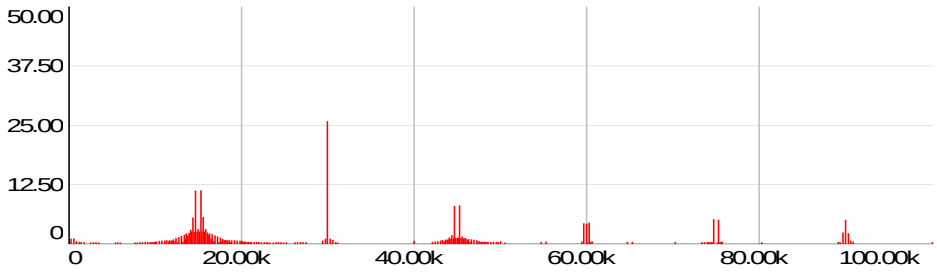


Figure 2.2 Harmonic spectrum of dc link current $I_{dc}$ for a working condition of NSPWM, $M_i$ = 0.7, φ = 0°, $f_c$=15kHz, (12.5A/div, 20kHz/div)

## 2.3 PWM Inverter

PWM Inverters are mostly used in motor drive, interfacing between regenerative sources and mains, and other AC supply applications with their capability of power flow from DC side to AC side. Actually their topology are same with rectifier, however, inverter controller drives six switches (Sx+, Sx-, x = a,b,c) in such a way

that all inverter legs act as buck converter and pumps AC current to the load after a low pass filtering stage of LC filter. $I_{hf}$ circulates between dc bus capacitor and the inverter switches. A sample of harmonic spectrum of $I_{dc}$ is seen in Figure 2.4 for a given operating condition. The only difference of inverter is the direction of power flow and the usage of semiconductor devices (the usage of freewheeling diode is lower than rectifier application) compared with the rectifier application. The dc bus current harmonic spectrum is same as in the rectifier. The spectral analysis in chapter 3 is based on this inverter structure.

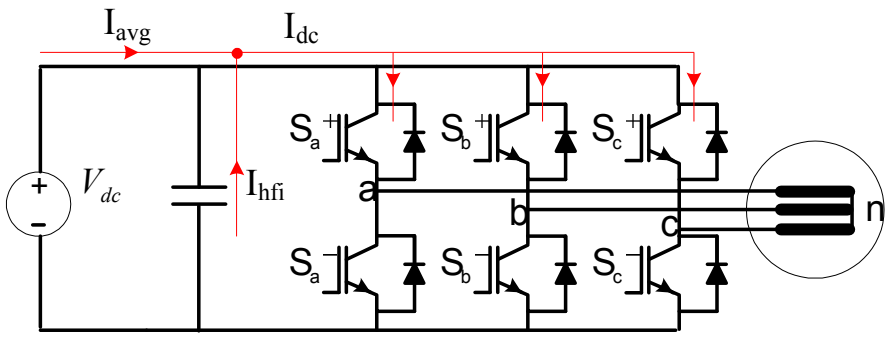


Figure 2.3 PWM VS Inverter topology and current distribution with 3Ø motor load

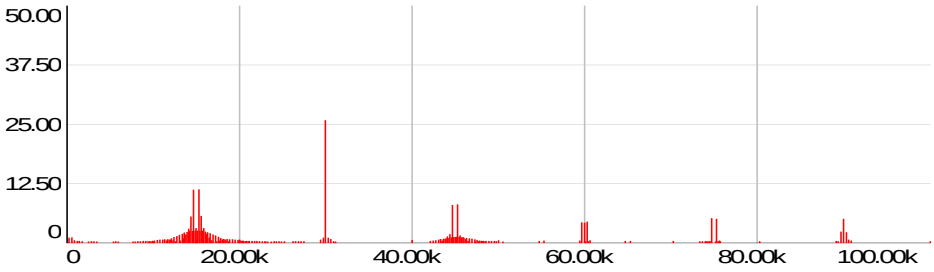


Figure 2.4 Harmonic spectrum of dc link current $I_{dc}$ for a working condition of NSPWM, $M_i$ = 0.7, φ = 0°, $f_c$=15kHz (12.5A/div, 20kHz/div)

## 2.4 PWM Rectifier Cascaded with PWM Inverter

In UPS (uninterruptible power source) applications and in motor drive applications that includes regenerative characteristics where power flow is bidirectional, *inverter cascaded rectifier*, in other words *back to back inverter topology*, is commonly

used. In this topology, $I_{hf}$ (high frequency current component) is composed of two parts which are rectifier side high frequency current component ($I_{hfr}$) and inverter side high frequency current component ($I_{hfi}$). Typically both sides operate at the same PWM frequency, and depending on the phase difference between triangular carriers of rectifier and inverter, these high frequency components can be added or subtracted algebraically or can be added in phasor domain depending on the polarities and frequencies of triangular carriers of both sides. If the frequencies are different, then (2.1), where magnitudes are rms, can be directly used to calculate the overall rms value of $I_{hf}$. If the carriers are in the same frequency but not in phase, $I_{hf}$ is higher than the right side of (2.1). If the carriers are in the same frequency and in phase, then $I_{hf}$ is smaller than the right side of (2.1). In the harmonic spectrum of Figure 2.6, triangular carriers are in the same frequency and in phase and thus some of the harmonic of rectifier side is cancelled with the harmonic of inverter side. Therefore the harmonic spectrum is flatter than the case in which carrier frequencies are different. This case is shown in Figure 2.7 with the same simulation parameters except the carrier frequencies. If the modulator types were the same in the case in which carriers are in the same phase with same frequency, the cancellation of $I_{hfr}$ and $I_{hfi}$ would be better.

$$I_{hf} = \sqrt{I_{hfr}^{\,2} + I_{hfi}^{\,2}} \qquad (2.1)$$

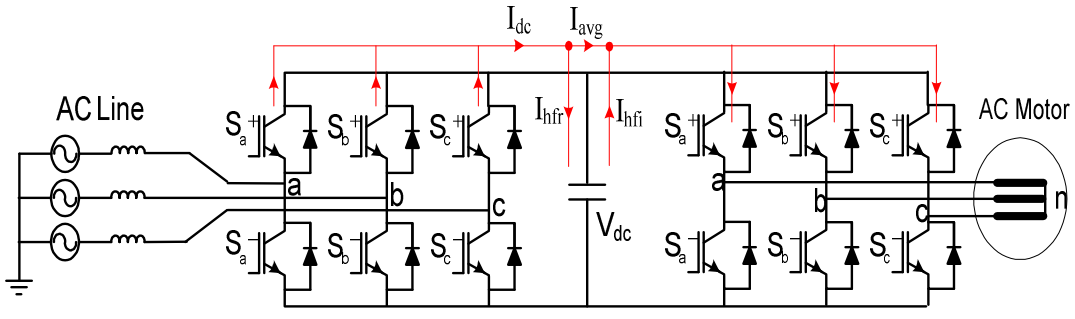


Figure 2.5 Back to back inverter topology and the current distribution

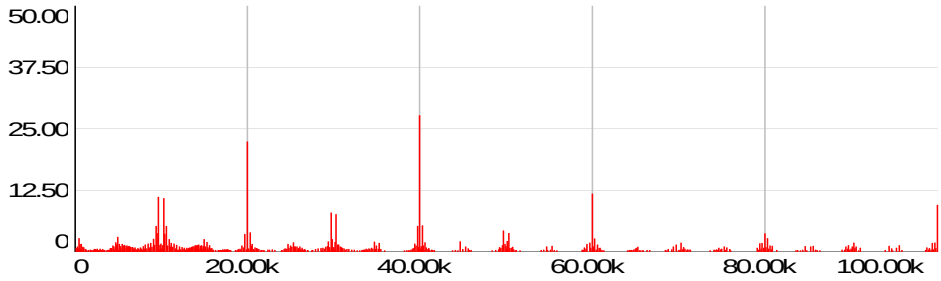


Figure 2.6 Harmonic spectrum of dc link capacitor current $I_{hf}$ for rectifier working condition of NSPWM, $M_i = 0.7$, $\varphi = 0°$, $f_c$=10kHz and inverter working condition of SVPWM, $M_i = 0.7$, $\varphi = 0°$, $f_c$=10kHz (12.5A/div, 20kHz/div)

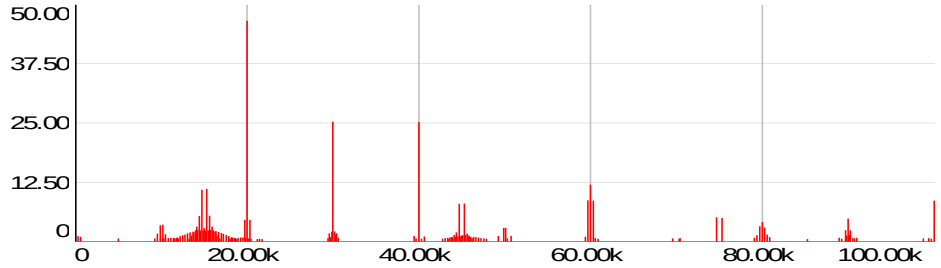


Figure 2.7 Harmonic spectrum of dc link capacitor current $I_{hf}$ for rectifier working condition of NSPWM, $M_i = 0.7$, $\varphi = 0°$, $f_c = 15$ kHz and inverter working condition of SVPWM, $M_i = 0.7$, $\varphi = 0°$, $f_c = 10$ kHz,
(12.5A/div, 20kHz/div)

## 2.5 Diode / Thyristor Rectifier Cascaded with PWM Inverter

This topology is different from other topologies in the sense that rectifier stage is composed of diodes or thyristors that switch at low frequency (fundamental frequency). This causes injection of dc bus current at low frequency and harmonics at low frequency (6 times the fundamental frequency and its multiples) as seen in Figure 2.9. In order to filter this low frequency current, dc bus capacitor size must be large enough. The harmonic spectrums of $I_{lfr}$ and $I_{hfi}$ are illustrated in Figure 2.10.

The simulation parameters used to output the waveform of Figure 2.9 and the spectrum of Figure 2.10 are tabulated in Table 2.1. As observed in the simulation data, at low frequency, the dominant harmonic is located at 300 Hz for the fundamental frequency of 50 Hz and the magnitude of the spectrum decreases rapidly with the increasing frequency. At high frequency, the typical spectrum is observed for the given operating condition.

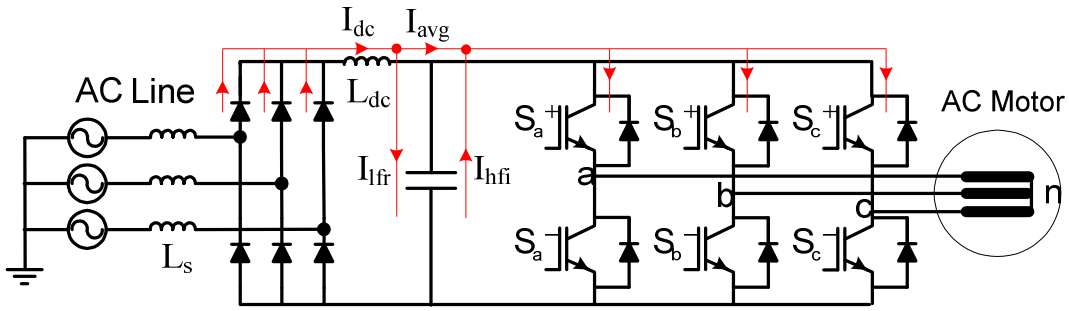


Figure 2.8 Diode / thyristor rectifier cascaded with PWM inverter

Table 2.1 3-phase diode rectifier side simulation parameters

| $V_{in\_rms\_per\_phase}$ | $f_{input}$ | $P_{out}$ of inverter | $L_s$ of rectifier input | $L_{dc}$ | $C_{dc\ bus}$ |
|---|---|---|---|---|---|
| 220 V | 50 Hz | 34 kW | 540 µH | 270 µH | 6.8 mF |

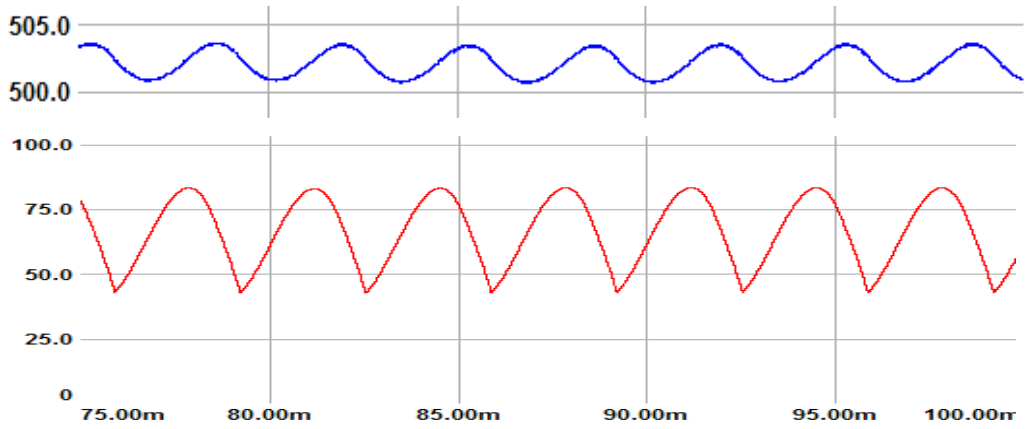


Figure 2.9 Dc link current $I_{dc}$ of rectifier (red, 25A/div) and dc bus voltage (blue, 5V/div) with the fundamental frequency of 50 Hz at the input of diode rectifier, (time axis, 5ms/div)

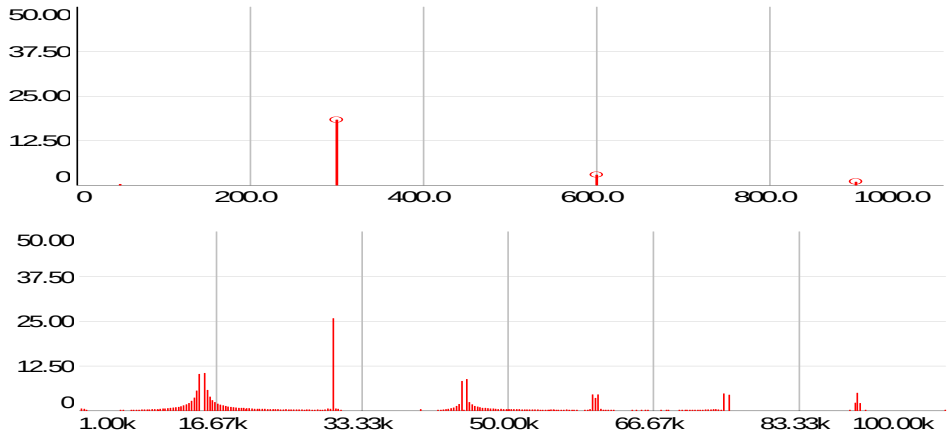


Figure 2.10 Low frequency (top) and high frequency (bottom) harmonic spectrum of $I_{dc}$ of rectifier with 34 kW output power and inverter working condition of NSPWM, $M_i = 0.7$, $\varphi = 0°$, (12.5A/div, 16.67kHz/div)

Table 2.2 Dc bus current frequency spectrum comparison

| **Topology** | | **Dc bus ripple current** | |
|---|---|---|---|
| **Source side** | **Load side** | **Source side** | **Load side** |
| diode / thyristor rectifier | PWM inverter | low frequency | high frequency |
| pv / dc battery | | | |
| PWM transistor rectifier | | high frequency | |

At PWM driven sides of these topologies, the dc bus current spectrum changes depending on the pwm method and operating point. Therefore they are important in evaluation of the dc bus performance and design. The topologies and the frequency content of their dc buses are tabulated in Table 2.2. In all these topologies, the PWM structure is common and the core point. Since, diode / thyristor rectifier needs much dc bus capacity with its dc bus current harmonics at low frequency and it injects much current harmonics to mains, this kind of converter is not focused on in this work.

In the next chapter, the detailed analysis of $I_{dc}$ harmonic spectrum of PWM structure depending on various operating conditions will be done and also a new concept of equivalent harmonic approach, which means grouping the fringe harmonic components under the umbrella of center harmonic, will be introduced.

# CHAPTER 3

# ANALYSIS AND CHARACTERIZATION OF DC BUS RIPPLE CURRENT

## 3.1 Introduction

As mentioned in previous chapters, three-phase Voltage Source Inverters (VSIs) are widely utilized in ac motor drives, uninterruptible power supplies (UPS), renewable energy systems, etc. to control the energy flow precisely, obtain high power quality and high energy efficiency. Pulse Width Modulation (PWM) is the standard approach to operate the inverter switches in order to generate the required output voltages. Due to high frequency switching both the ac and the dc side of the inverter involve high frequency rectangular voltage/current pulses that create stress on the inverter components. This chapter studies the dc bus ripple current due to the PWM operation, and it elaborates on the stresses the ripple creates on the dc bus capacitor.

In this chapter, dc bus current ripple of VSI will be inspected; ripple current characteristics depending on the operating point and PWM technique utilized will be studied. The microscopic (per PWM cycle), the rms, and spectral components will be discussed for various PWM method and operating conditions. The double Fourier analysis approach will be briefly reviewed and utilized to generate the spectral data. Then the equivalent centered harmonic approach (EHA) will be proposed and its results will be demonstrated. After the demonstration of the method, 3D $I_{dc}$ graph will be shown as a design tool based on EHA.

### 3.2 Dc Bus Current Ripple of VSI

This section reviews the dc bus current ripple of the three-phase, two-level inverter for various operating conditions and PWM methods. The main purpose is to provide a basic tutorial before attempting advanced analysis. First via microscopic waveforms the physical understanding will be established. Second via evaluation of the spectral components the dominant frequency range will be shown. In this section, the spectral data used will be based on the double Fourier approach (also verified by means of computer simulations). Finally the ripple current rms value for various PWM methods will be evaluated for various PWM methods and operating condition.

It is helpful to define a modulation index ($M_i$, voltage utilization level) term at this stage. For a given dc link voltage ($V_{dc}$), the ratio of the fundamental component magnitude of the line to neutral inverter output voltage ($V_{1m}$) to the fundamental component magnitude of the six-step mode voltage ($V_{1m\text{-}6\text{-}step} = 2V_{dc}/\pi$) is termed the modulation index $M_i$ [1] as defined in (3.1).

$$M_i = V_{1m} / V_{1m-6-step} \tag{3.1}$$

The inverter under analysis is the three phase, three wire PWM VSI and the inverter is assumed to be loaded with balanced three phase sinusoidal output current at steady state operation.

#### 3.2.1 Microscopic View

Under balanced, sinusoidal steady state operation, the inverter dc bus current ripple instantaneous waveforms appear as picket-fences (as rectangular pulses at the carrier frequency or higher) and their outer appearance depends on the load current magnitude ($I_{om}$) and power factor, as shown in Figure 3.1 (obtained by computer simulations for SVPWM). The magnitude of the sinusoidal load current is the prime factor in determining the magnitude of current pulses. With unity power factor, the current pulses are always with positive value. However, with decreasing power

factor negative current pulses appear in the waveform. The balanced sinusoidal output current waveforms are expressed in (3.2), the average value of the dc bus current ($I_{avg}$) is expressed in (3.3), and it is supplied by the dc voltage source. The difference of $I_{dc}$ and $I_{avg}$ is defined as the ripple current $I_{hf}$ as given in (3.4), and it is bypassed through the dc bus capacitor. The phase currents are assumed as balanced cosinusoidal with the peak of $I_{om}$ and lagging power factor of *cos φ*.

$$I_a = I_{om} \cdot \cos(\omega t - \varphi) \tag{3.2}$$
$$I_b = I_{om} \cdot \cos(\omega t - \frac{2\pi}{3} - \varphi)$$
$$I_c = I_{om} \cdot \cos(\omega t - \frac{4\pi}{3} - \varphi)$$

$$I_{avg} = \left(\frac{3}{\pi}\right) \cdot M_i \cdot I_{om} \cdot \cos\varphi \tag{3.3}$$

$$I_{hf} = I_{dc} - I_{avg} \tag{3.4}$$

While Figure 3.1 is obtained for SVPWM, it is difficult to distinguish it from the waveforms of other PWM methods by outer appearance. However, as will be shown, in the detailed (microscopic) view, significant differences exist. Thus, the harmonic spectrum of different modulation techniques can be correlated with microscopic analysis of dc bus current within a switching period.

As Figure 3.2 shows, in SVPWM and AZSPWM1, $I_{dc}$ is composed of two rectangles in a PWM cycle. Thus, they are expected to result in dominant harmonics centered at double the switching frequency ($2f_c$). For φ = 0° the rectangle is full with high average value and low ripple. For φ = 90° the rectangle has low average value and high ripple. Thus, high power factor implies low ripple current. As shown in Figure 3.3, for DPWM1 and NSPWM, the rectangles are gathered into one piece. Based on the appearance of the waveform shapes, it becomes obvious now strong harmonics exist at both $f_c$ and $2f_c$. For φ = 0° the rectangle is full with high average value and low ripple. For φ increasing the rectangle has low average value and high ripple. Thus, high power factor implies low ripple current. In particular, in NSPWM

the φ dependency is strong and the performance rapidly degrades as φ approaches 30°. Apparent from this discussion, the visual observation does not yield sufficient information about the ripple content and spectral analysis is necessary.

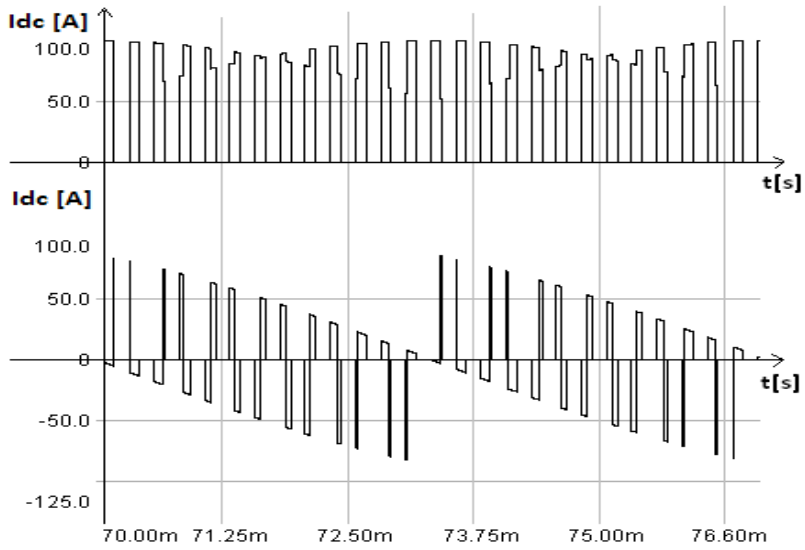


Figure 3.1 DC bus current waveform over a 60º of a fundamental cycle for SVPWM under the operating conditions of $M_i$=0,785, $I_{om}$=100 A. Top: φ = 0°, bottom φ = 90°, (50A/div, 1.25ms/div)

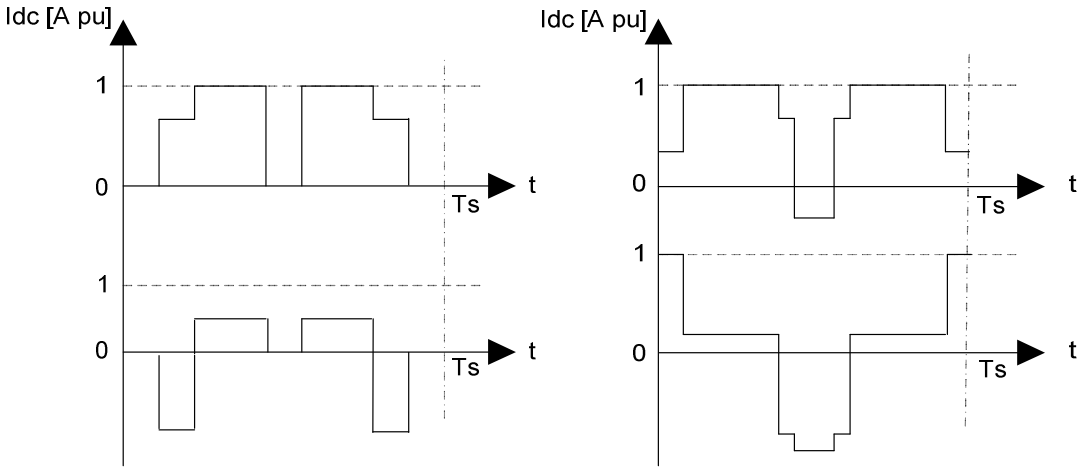


Figure 3.2 Inverter microscopic dc bus currents in a PWM period for continuous PWM methods; Left: SVPWM ($M_i$=0.7, top: φ = 0°, bottom φ = 90°), Right: AZSPWM1 ($M_i$=0.7, top: φ = 0°, bottom φ = 90°)

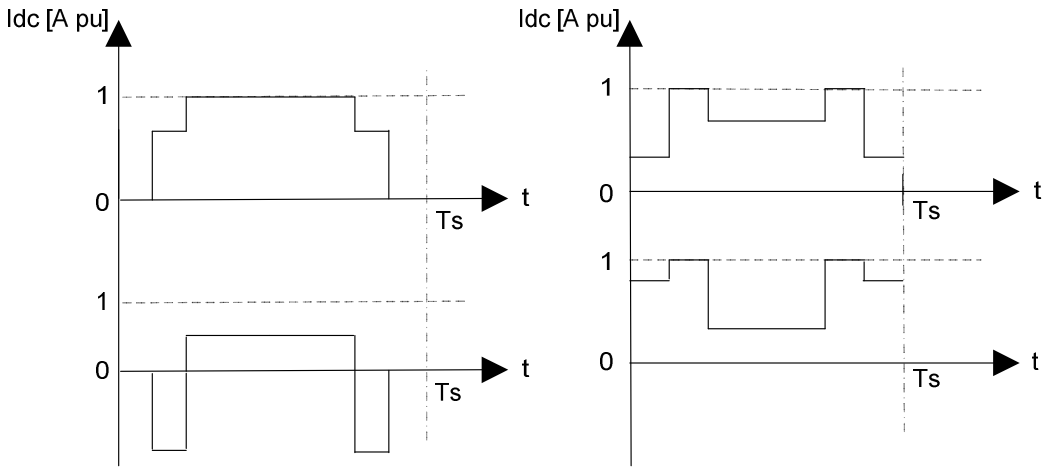


Figure 3.3 Inverter microscopic dc bus currents in a PWM period for discontinuous PWM methods; Left: DPWM1 ($M_i$=0.7, top: $\varphi = 0°$, bottom $\varphi = 90°$), Right: NSPWM ($M_i$=0.7, top: $\varphi = 0°$, bottom $\varphi = 30°$)

### 3.2.2 Spectral Content

As apparent from the preceding section, the spectral content of the dc bus ripple current is PWM method dependent, as well as the operating conditions. To illustrate typical spectral content, several methods and operating conditions are considered. A three-phase inverter drive is considered. Balanced sinusoidal operation is assumed. The load current ripple is neglected. The discussed PWM methods with a pure-sinusoidal, 100A peak value rated output current, with 50Hz fundamental frequency are considered. The inverter DC bus is 800V and the carrier frequency ($f_c$) is 10kHz for SVPWM and AZSPWM1 and 15kHz for NSPWM and DPWM1 such that the average switching frequency is the same (10kHz) in all cases. By this way, continuous and discontinuous PWM methods cause same power loss on the inverter switches which means the same thermal stress inserted on the inverter.

The harmonic spectrum for various methods is shown from Fig. 3.4 to Fig. 3.9 for various operating conditions. As shown in Figure 3.4 and Figure 3.5, for SVPWM and AZSPWM1 at low $M_i$ the dominant harmonics are at twice the carrier frequency $2f_c$ (AZSPWM1 has some notable harmonics at $f_c$ also). As shown in Figure 3.6 and Figure 3.7, DPWM1 dominant harmonics are at $f_c$. As shown in

Figure 3.8 and Figure 3.9, NSPWM has harmonics both at $f_c$ and $2f_c$. Depending on φ and $M_i$, the dominant term may become at $f_c$ or $2f_c$. While $2f_c$ harmonic is dominant for φ = 0°, $f_c$ harmonic is dominant for φ = 30º.

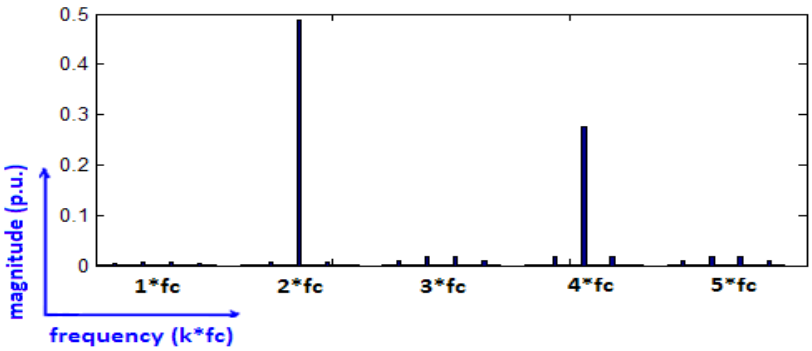


Figure 3.4 Ripple current spectrum (0.1A-pu/div), SVPWM, $M_i$=0,3, φ = 0°, $I_{om}$=100 A

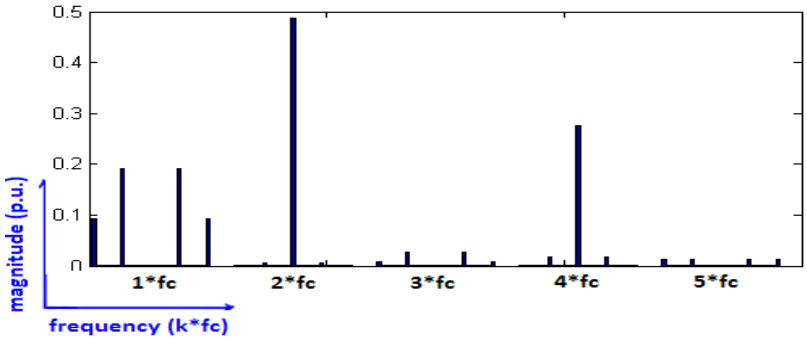


Figure 3.5 Ripple current spectrum (0.1A-pu/div), AZSPWM1, $M_i$=0,3, φ = 0°, $I_{om}$=100 A

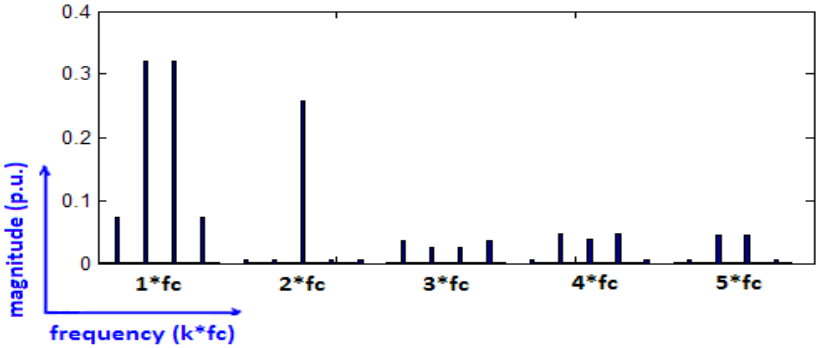


Figure 3.6 Ripple current spectrum (0.1A-pu/div), DPWM1, $M_i$=0,7, φ = 0°, $I_{om}$=100 A

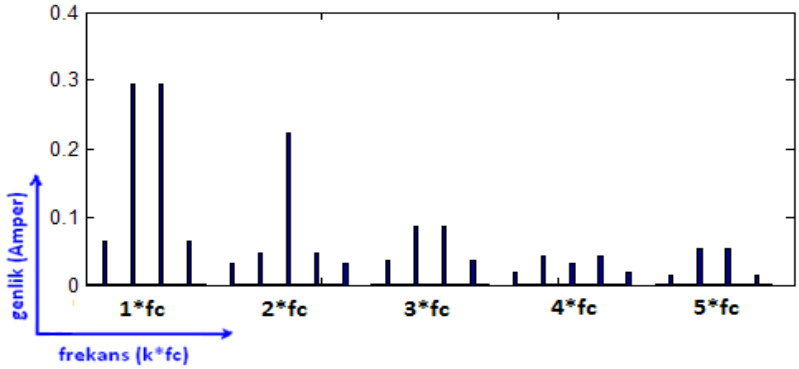


Figure 3.7 Ripple current spectrum (0.1A-pu/div), DPWM1, $M_i$=0,7, φ = 30°, $I_{om}$=100 A

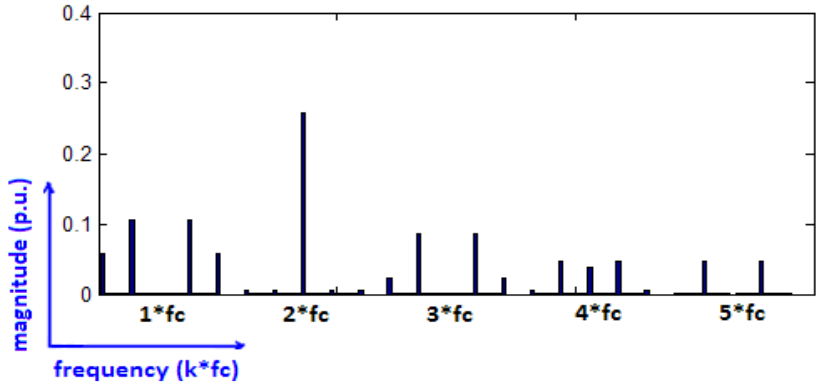


Figure 3.8 Ripple current spectrum (0.1A-pu/div), NSPWM, $M_i$=0,7, φ = 0°, $I_{om}$=100 A

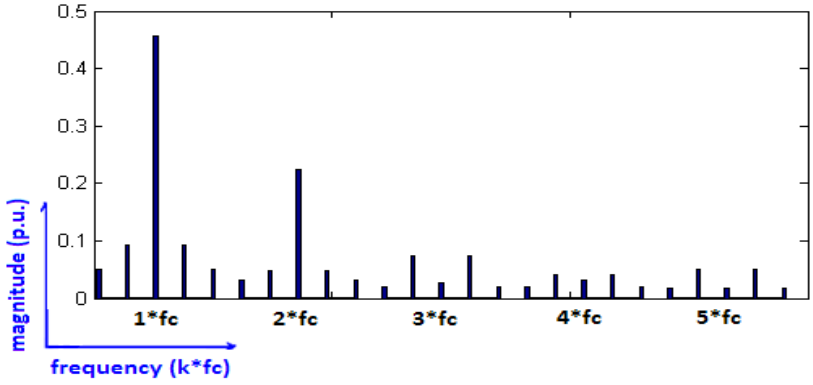


Figure 3.9 Ripple current spectrum, (0.1A-pu/div), NSPWM, $M_i$=0,7, φ = 30°,

$I_{om}$=100 A

### 3.2.3 Total RMS Value

In order to compare the DC link current ripple performance of the PWM methods, the ratio of the harmonic rms value of the DC link current $I_{h\text{-}rms}$ to the inverter AC output fundamental component current rms value $I_{1rms}$ ($I_{om}/\sqrt{2}$) is evaluated and its square is termed as the dc link current coefficient $K_{dc}$ [1]-[3] defined in (3.5).

$$K_{dc} = I^2_{h-rms} / I^2_{1rms} \tag{3.5}$$

For given $M_i$ and φ, the RMS ripple DC link current is first calculated over a PWM cycle, then over a fundamental cycle to obtain $I_{h\text{-}rms}$. Then (3.5) is analytically calculated for all the methods discussed. Evaluating $K_{dc}$ reveals some important attributes of the modulators. As Figure 3.10 indicates, all methods are $M_i$ and φ dependent. The reduced common mode voltage PWM methods have several times higher DC link current stress than the SVPWM and DPWM methods. At low $M_i$ AZSPWM1 (especially at low cosφ) method exhibits large stresses. At higher $\cos\varphi$ the AZSPWM1 stresses become less. At higher $M_i$ the DC link current stresses of the AZSPWM1 method become comparable to the conventional methods due to the expiration of the active zero state duration. The DC link current harmonic content of NSPWM is strongly dependent on PF and $M_i$. $K_{dc}$ of NSPWM decreases with increasing $M_i$ and PF. For PF = 1, NSPWM has lower DC link ripple content than all other PWM methods. For PF of 0.8-0.9, $K_{dc}$ of all PWM methods are similar. However, for PF lower than 0.6, $K_{dc}$ of NSPWM is inferior to other methods.

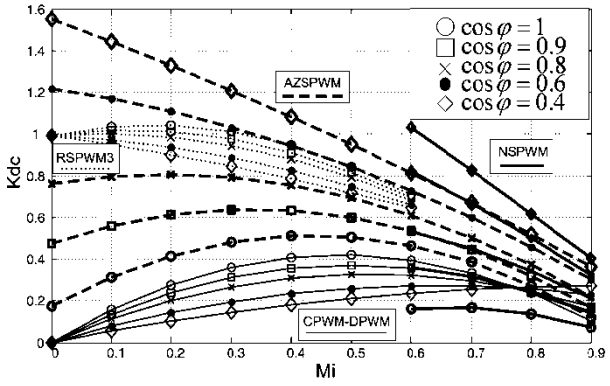


Figure 3.10 RMS ripple current characteristics, $K_{dc} = f(M_i,\cos\varphi)$ for various PWM methods

### 3.3 Ripple Current Spectral Analysis

As apparent from the preceding section, the ripple current harmonic content is highly PWM method and operating point dependent. For inverter design and analysis purposes, it is necessary to have broad information on the spectra. Thus, a method to calculate the spectral content and a simple approach to be utilized in the inverter design is required. While detailed simulations are exhaustive and not intuitive, the simple rms value approach is insufficient. Thus in this section the double Fourier approach [7]-[9] will be utilized to obtain the spectral data, and in the next section a method to provide a simple design tool based on the data obtained from the double Fourier approach will be introduced. The general analytical approach to obtain the exact harmonic content of periodically switching circuits involves the double Fourier approach. In this approach, first, the phase current functions as in (3.2) and the PWM switching functions as in (3.6), (3.7), and (3.8) are defined. Second, these functions are algebraically manipulated to obtain a raw $I_{dc}$ function as in (3.13) to be processed in the double integral of (3.14) in order to calculate the harmonic coefficients. For the cosine modulation expressed in (3.6), the fourier integral of (3.14) can be expanded as in (3.10) by using the trigonometric identity in (3.9) and using the bessel function of the first kind expressed in (3.11), the closed form expression of the harmonic spectrum coefficients are obtained as in (3.12).

The closed form expression for cosine modulation is obtained easily and systematically expanding the double fourier integral to the bessel function, however, it is impossible to get such a closed form bessel expression for the other modulation functions since these modulation functions are piecewise as in (3.7) for SVPWM and in (3.8) for DPWM1 modulators. Thus, for these modulators and other modulators with phase reversing carrier (NSPWM, AZSPWM1), the double fourier integral is calculated numerically using matlab code as illustrated in appendix.

In (3.2), the phase currents are defined as balanced three phase cosinusoidal currents with the magnitude $I_{om}$. In (3.14), F(·) is the double Fourier transform where $p = a, b, c$ *and* $y = \omega_c t$, $x = \omega_f t$. Moreover, $S_p$ denotes switching function and $M_p$ denotes modulation function. All three phase modulation functions are 120° phase shifted and denoted as $M_a, M_b, M_c$.

From the linearity of fourier transform, fourier transform of the $I_{dc}$ is decomposed into fourier transform of switched phase leg currents. These leg current transforms are added linearly as in (3.15) and the magnitudes of $I_{dc}$ harmonic components are calculated via using (3.16).

In Figure 3.11, each (2π, 2π) region involves a bounded wall structure which is laterally bounded with modulation function (modulation function is SPWM in Figure 3.11). The top (towards the reader) bound of the walls is the output sinusoidal current function which also changes sinusoidally up and down at the fundamental frequency with respect to *y* axis. Moreover, this pattern repeats itself over (*x*, *y*) plane.

$$M(\omega t) = \cos(\omega t) \tag{3.6}$$

$$M(\omega t) = \begin{cases} \frac{\sqrt{3}}{2} \cdot M \cdot \cos\left(\omega t - \frac{\pi}{6}\right), & 0 < \omega t < \frac{\pi}{3} \\ & \cup \quad \pi < \omega t < \frac{4\pi}{3} \\ \frac{3}{2} \cdot M \cdot \cos(\omega t), & \frac{\pi}{3} < \omega t < \frac{2\pi}{3} \\ & \cup \quad \frac{4\pi}{3} < \omega t < \frac{5\pi}{3} \\ \frac{\sqrt{3}}{2} \cdot M \cdot \cos\left(\omega t + \frac{\pi}{6}\right), & \frac{2\pi}{3} < \omega t < \pi \\ & \cup \quad \frac{5\pi}{3} < \omega t < 2\pi \end{cases} \tag{3.7}$$

$$M(\omega t)=\begin{cases} 1, & \frac{-\pi}{6}<\omega t<\frac{\pi}{6} \\ \sqrt{3}\cdot M\cdot\cos\left(\omega t-\frac{\pi}{6}\right)-1, & \frac{\pi}{6}<\omega t<\frac{\pi}{2} \\ \sqrt{3}\cdot M\cdot\cos\left(\omega t+\frac{\pi}{6}\right)+1, & \frac{\pi}{2}<\omega t<\frac{5\pi}{6} \\ -1, & \frac{5\pi}{6}<\omega t<\frac{7\pi}{6} \\ \sqrt{3}\cdot M\cdot\cos\left(\omega t-\frac{\pi}{6}\right)+1 & \frac{7\pi}{6}<\omega t<\frac{3\pi}{2} \\ \sqrt{3}\cdot M\cdot\cos\left(\omega t+\frac{\pi}{6}\right)-1 & \frac{3\pi}{2}<\omega t<\frac{11\pi}{6} \end{cases} \tag{3.8}$$

$$\cos\theta=\frac{1}{2}\cdot\left(e^{j\theta}+e^{-j\theta}\right) \tag{3.9}$$

$$\begin{aligned} F\left(S_p\cdot I_p\right)=\frac{I_{om}}{j4\pi^2 m}\cdot\Big[ & e^{j\left(m\frac{3\pi}{2}-\varphi\right)}\int_0^{2\pi}e^{j(n+1)y}\cdot e^{j\left(m\cdot\frac{\pi}{2}\cdot M\cdot\cos(y)\right)}\cdot dy \\ & -e^{j\left(m\frac{\pi}{2}-\varphi\right)}\int_0^{2\pi}e^{j(n+1)y}\cdot e^{j\left(-m\cdot\frac{\pi}{2}\cdot M\cdot\cos(y)\right)}\cdot dy \\ & +e^{j\left(m\frac{3\pi}{2}+\varphi\right)}\int_0^{2\pi}e^{j(n-1)y}\cdot e^{j\left(m\cdot\frac{\pi}{2}\cdot M\cdot\cos(y)\right)}\cdot dy \\ & -e^{j\left(m\frac{\pi}{2}+\varphi\right)}\int_0^{2\pi}e^{j(n-1)y}\cdot e^{j\left(-m\cdot\frac{\pi}{2}\cdot M\cdot\cos(y)\right)}\cdot dy\Big] \end{aligned} \tag{3.10}$$

$$J_n(Z)=\frac{j^{-n}}{2\pi}\cdot\int_0^{2\pi}e^{jZcos(\theta)}\cdot e^{jn\theta}\cdot d\theta \tag{3.11}$$

$$\begin{aligned} F\left(S_p\cdot I_p\right)=\frac{I_{om}\cdot j^n}{2\pi m}\cdot\Big[ & e^{j\left(m\frac{3\pi}{2}-\varphi\right)}\cdot J_{n+1}\left(m\cdot\frac{\pi}{2}\cdot M\right)-e^{j\left(m\frac{\pi}{2}-\varphi\right)}J_{n+1}\left(-m\cdot\frac{\pi}{2}\cdot M\right) \\ & -e^{j\left(m\frac{3\pi}{2}+\varphi\right)}J_{n-1}\left(m\cdot\frac{\pi}{2}\cdot M\right)+e^{j\left(m\frac{\pi}{2}+\varphi\right)}J_{n-1}\left(-m\cdot\frac{\pi}{2}\cdot M\right)\Big] \end{aligned}$$

$$for\ n=\ -\infty\ldots.+\infty\ and\ m=1,2,3,\ldots. \tag{3.12}$$

$$I_{dc}=\ S_aI_a+S_bI_b+S_cI_c$$

$$F(I_{dc})=\ F(S_aI_a)+\ F(S_bI_b)+\ F(S_cI_c) \tag{3.13}$$

$$F(S_p \cdot I_p) \equiv \frac{1}{2\pi^2} \cdot \int_0^{2\pi} \left( \int_{\frac{\pi}{2}(1-M_p(y))}^{\frac{\pi}{2}(3+M_p(y))} I_p e^{j(mx+ny)}\, dx \right) dy \tag{3.14}$$

$$A_{mn} + jB_{mn} = \sum_{p=a,b,c} F(S_p \cdot I_p) \tag{3.15}$$

$$I_{mn} = \sqrt{A_{mn}^2 + B_{mn}^2} \tag{3.16}$$

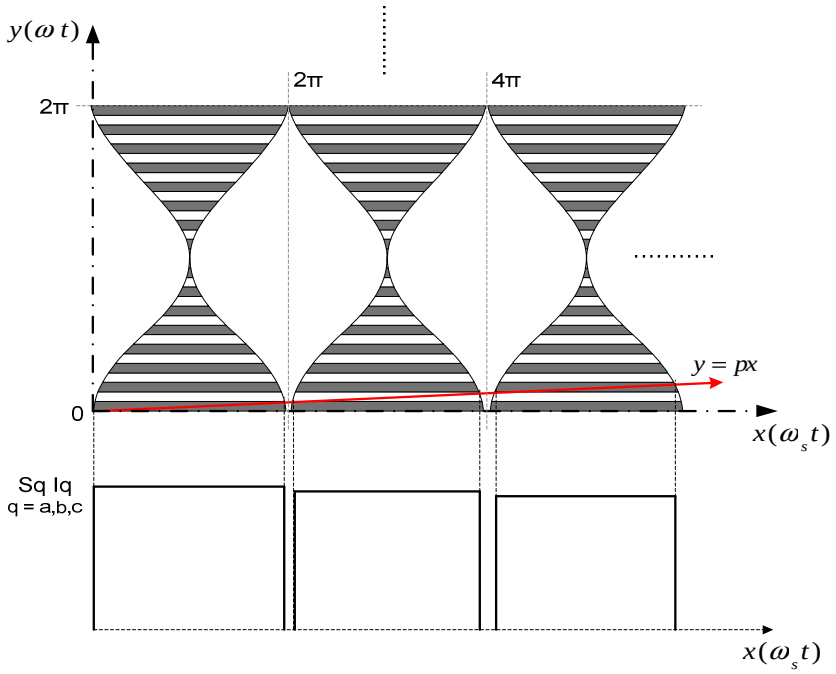


Figure 3.11 Repeated wall structure with natural triangular sampling

In Figure 3.12, shaded areas are the integration domains that construct the inner integral limits in (3.14) for sinusoidal PWM (SPWM). For other PWM methods, the boundary of the shaded region (modulation function) is changed depending on the PWM waveform under analyze.

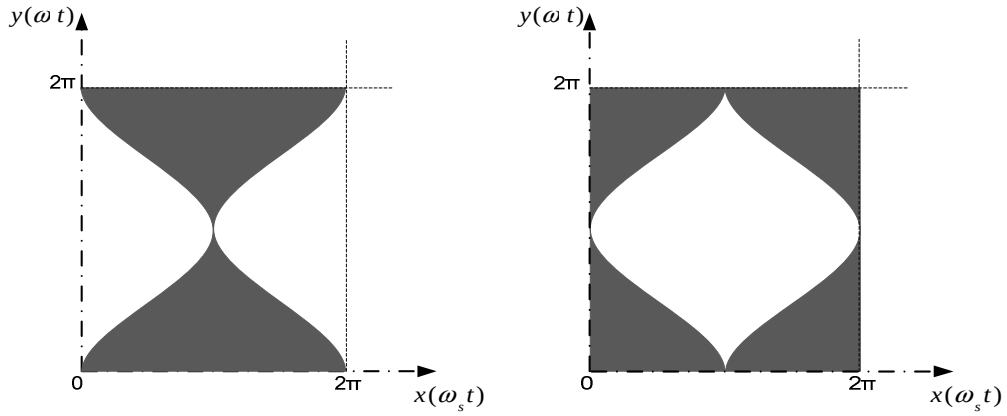


Figure 3.12 Integration domains for inner integral of double fourier transform for SPWM. Fourier Integral is calculated in the left domain in the case of normal triangular carrier and calculation is done in the right domain in the case of reverse triangular carrier

The general spectrum calculation algorithm works as follows: In terms of equations, using the integral of (3.14), the coefficients $A_{mn}$ and $B_{mn}$ are obtained as in (3.15), then the ripple current magnitude for each frequency is obtained as $I_{mn}$ in (3.16). Here m corresponds to the carrier frequency and its multiples, and n corresponds to the fundamental component and its multiples. Thus, the harmonics are at the $mf_c \pm nf_o$. As a result, the dc link current is obtained as the fourier series expansion F(x,y) given in (3.17). Of the four terms in (3.17), the first one gives the average current of (3.3). The second term gives the possible sub-carrier frequency components. The third term gives the carrier frequency and its multiples (center frequency harmonics). And the final term gives the sideband harmonics for the carrier and its multiples. The details of the double Fourier approach as applied to dc current ripple calculation are laid out in [9].

$$F(x,y) = \frac{A_{00}}{2} + \sum_{n=1}^{\infty}[A_{0n}\cdot\cos(ny) + B_{0n}\cdot\sin(ny)] + \sum_{m=1}^{\infty}[A_{m0}\cdot\cos(mx) + B_{m0}\cdot\sin(mx)] + \sum_{m=1}^{\infty}\sum_{n=\mp1}^{\mp\infty}[A_{mn}\cdot\cos(mx+ny) + B_{mn}\cdot\sin(mx+ny)] \quad (3.17)$$

Employing the above described double Fourier integral approach and utilizing advanced computational tools with double integral routines, the spectral components can be easily obtained. In this work, MATLAB software has been used for this purpose. The spectral data of Figure 3.6 to Figure 3.11 were obtained by this method. However, to confirm the results, detailed inverter simulation model was built via Simplorer power electronics simulation software and via FFT analysis of the dc link current the double Fourier results were verified.

While the double Fourier approach gives the spectral information, there are difficulties in applying this approach in practice. The approach involves advanced mathematical skills, and complex to implement for a typical design engineer. The spectral graphics are strongly dependent on the PWM method and operating conditions ($M_i$, $\varphi$, $I_{om}$). The wide range of harmonics are difficult to individually consider in the design. Thus simplification is necessary. The following section elaborates on this issue.

### 3.4 The Equivalent Centered Harmonic Approach

Since the ripple current consists of carrier and sidebands and multiples with sidebands, it is difficult to evaluate the total effect of the ripple current by observing individual components (as there are too many terms). Using the total RMS value (as in Figure 3.10) hides the frequency information, which is necessary in design and performance evaluation. Thus, an approach more informative than the rms value approach, but not as complicated as the full harmonic spectrum study is required. As illustrated in Figure 3.13, the equivalent centered harmonic approach developed in this section lumps the ripple current carrier frequency component and its sidebands to the center (to the carrier frequency) as a single frequency equivalent. The same is done for the multiples of the carrier, for example harmonics at $2f_c$ and the sidebands are lumped at an equivalent harmonic at $2f_c$ and so on. In other words, bunches of harmonics are localized at integer multiple of carrier frequency and therefore can also be called as ‘local rms’. The equivalent centered harmonic current equation for the mth carrier multiple frequency $I_{h\text{-}me}$ is given in (3.18),

where m is the multiple index of the carrier frequency and n is the sideband index. M and N define the range to be covered.

$$I_{h-me} = \sqrt{\sum_{n=-N}^{N} I_{h-mn}^2} \qquad m=1, ..., M \qquad (3.18)$$

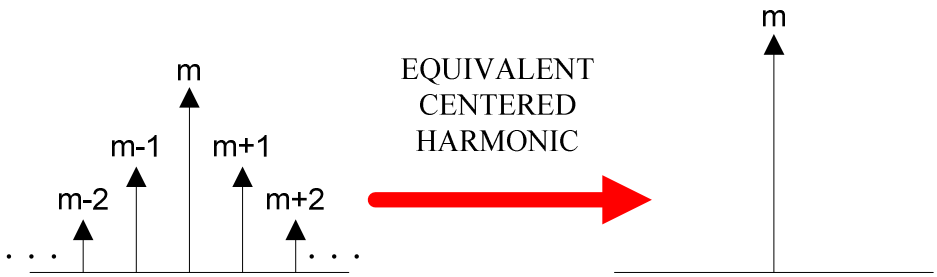


Figure 3.13 The equivalent centered harmonic representing the carrier frequency harmonic and its sidebands

The equivalent harmonic concept has a physical meaning from the practical application perspective. In both electrolytic and film capacitors the loss mechanism involved is frequency dependent. In both electrolytic and film capacitors the ESR losses are frequency dependent. The carrier frequency and its sideband harmonics are typically very close to each other that in this range the losses don't vary significantly. Thus, in terms of losses the harmonics can be represented with one equivalent centered harmonic as defined in (3.18). In this case the equivalent harmonic approach may be used to calculate the losses with more accuracy than a simple rms or single frequency calculation. Similarly, in applications with small film capacitor, the voltage ripple can be approximately calculated based on the dominant equivalent harmonic term using the $V_{h\text{-}me} = I_{h\text{-}me}/(\omega_{me}C)$ terminal law.

In practice the dominant harmonics are in the first 4 terms and their sidebands (M=4). Thus, it is sufficient to consider harmonics from $f_c$ to $4f_c$. In terms of sidebands, while a wide range can be considered, the first 10 (±10) are sufficient to represent the exact system (N=10). Considering this range, for the system parameters defined in the sub section 3.2.2, the equivalent centered harmonics have been calculated using equations (3.6) to (3.9) for the discussed PWM methods and a

full range of $M_i$ and PF was swept. Moreover, the ac output current has been normalized (100 Apeak = 1 unit) such that per unit equivalent harmonic content could be obtained. Using the MATLAB software, the formulas were executed (executed code is attached in the appendix part), and 3-D graphics were obtained as shown in Figure 3.14. In the figure, the rms total value consistent with Figure 3.10, and the first four equivalent centered harmonics ($f_c$, $2f_c$, $3f_c$, $4f_c$) are shown. Since it is given in normalized form, this graphic is general and can be used to obtain the harmonic information for any operating condition. Thus, a design engineer can use (look-up through the data) this graphic directly, and there is no more need for double Fourier analysis and detailed computer programming to do the calculations.

The 3-D graphic results show that for SPWM and SVPWM, the dominant harmonics are at m=2. For AZSPWM1, the first two harmonics are dominant (the $2f_c$ term being stronger), but the harmonics vary significantly and highly depend on the operating point. Thus, given an operating point the dominant harmonics could be selected by comparing all four harmonics. For DPWM1 the first two are dominant (the $f_c$ term being stronger), and the rest should be taken into account depending on the operating point. For NSPWM, the operating point sensitivity is the strongest as the graphics show. Thus, given an operating point all the four components should be taken into consideration carefully. The results of Figure 3.4 to Figure 3.9 are consistent with the graphics and the results of this discussion. Furthermore, many additional simulations were conducted to verify the accuracy of the 3-D graphic data, and correlation was established. Thus only the 3-D graphic data is shown and simulation results omitted.

In the next section, a general information about power electronic capacitors will be given and in the following chapter, based on the application type and its operating points, the selection of the right PWM method and later the inverter design in terms of dc bus capacitor sizing will be studied. This design process becomes possible by using these 3-D graphic results.

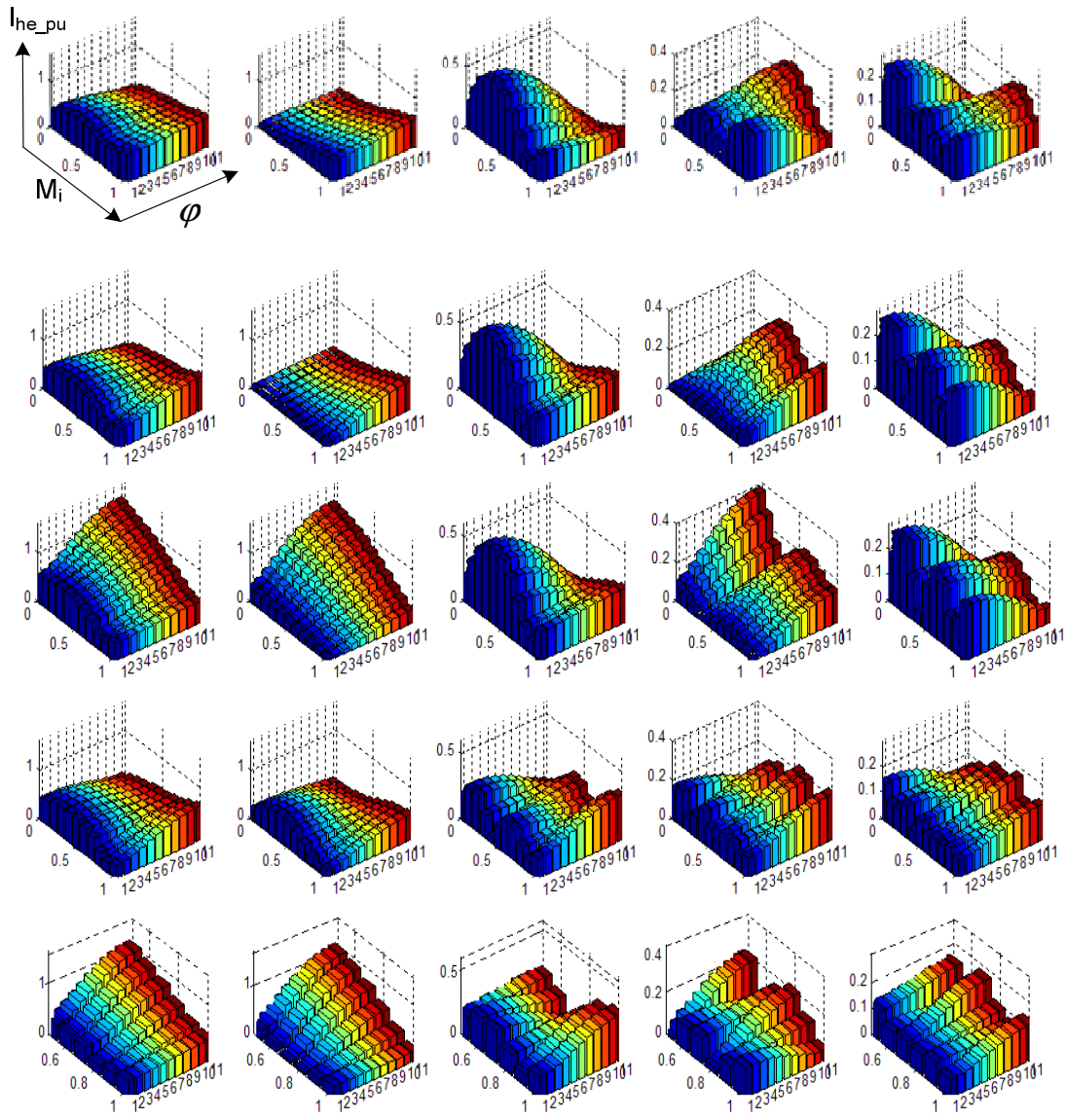


Figure 3.14 The normalized rms and normalized equivalent centered dc bus current harmonics. From top to bottom: SPWM, SVPWM, AZSPWM1, DPWM1, NSPWM. From left to right: normalized rms value (scaled with √2), first centered harmonic peak value (m=1), second centered harmonic peak value (m=2), third centered harmonic peak value (m=3), fourth centered harmonic peak value (m=4). $M_i$ axis: 0.1 to 0.9 in 0.1 increments, and φ axis: 0º to 90º in 9° increments

# CHAPTER 4

# POWER ELECTRONIC CAPACITORS

## 4.1 Introduction

In this chapter, it is aimed to cover all types of capacitors used in power electronic applications and to focus on film and electrolytic type capacitors that are related to the topologies and designs elaborated on this thesis work.

Capacitors are the essential components in power electronics where energy accumulation, energy circulating via switching and filtering are basic mechanisms. Power electronics spectrum ranges from low power SMPS applications to high power inverting – rectifying applications. Moreover, depending on circuit parameters like voltage and current levels, application categories like industrial applications, military applications, space applications and commercial applications that dictate different environmental parameters like temperature, atmospheric pressure etc., different types of capacitors are manufactured to match this wide spectrum of needs. Fundamental and mostly manufactured types of capacitors can be grouped as: Electrolytic capacitors, Tantalum Capacitors, Film Capacitors and Ceramic Capacitors. Electrolytic and film capacitors are used in both low power and high power applications with their wide voltage and current range. However, ceramic and tantalum capacitors are used in low power applications with their limited voltage and current range characterized from their internal dielectric material and physical structure different from electrolytic and film. Capacitors can be compared with their voltage rating, rms current rating and ESR (Equivalent Series Resistor) value, which is responsible for the thermal dissipation inside

capacitor, and drifting of these values depending on ambient temperature, bias voltage and atmospheric pressure. With these internal losses, temperature dependency and other parameter dependencies make the capacitor far from ideal capacitor which is a theoretical circuit element. Therefore the actual circuit model of capacitor is as in Figure 4.1.


Figure 4.1 Capacitor equivalent circuit model [17]

In Figure 4.1, *L* is the equivalent series inductance sourced from the lead wires, internal connection wires and planes, *R* is the equivalent series resistance that can be decomposed into the resistance that symbolizes the dielectric loss and the resistance which is sourced from contact resistance, lead wire resistance, and electrolyte resistance for electrolytic capacitors. *r* is the resistance that defines the leakage current and *C* is the ideal capacitance. Another parameter that is the measure of ratio of resistive loss to reactive energy in the capacitor is DF (Dissipation Factor) or $tan\delta$ where $\delta$ is the loss angle. The geometric definition of DF is shown in Figure 4.2.

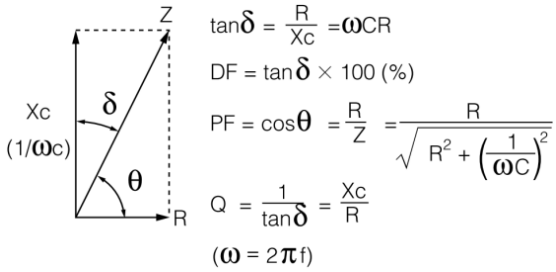


Figure 4.2 Geometrical definition of DF [17]

The comparison of different types of capacitors depending on mentioned environmental conditions and capacitor parameters and ratings are shown in Table 4.1. In this table, another capacitor parameter 'Dielectric Absorption' is added as comparison criteria. Dielectric Absorption is the residual charge or voltage on

capacitor after discharging of the capacitor. This phenomenon is called as battery action.

Table 4.1 Comparison of capacitors [20]

| | TYPE | TYPICAL DIELECTRIC ABSORPTION | ADVANTAGES | DISADVANTAGES |
|---|---|---|---|---|
| | NPO ceramic | <0.1% | Small case size<br>Inexpensive<br>Good stability<br>Wide range of values<br>Many vendors<br>Low inductance | DA generally low, but may not be specified<br>Limited to small values (10 nF) |
| Polymer Film Capacitors | Polystyrene | 0.001%<br>to 0.02% | Inexpensive<br>Low DA available<br>Wide range of values<br>Good stability | Damaged by temperature > +85°C<br>Large case size<br>High inductance |
| | Polypropylene | 0.001%<br>to 0.02% | Inexpensive<br>Low DA available<br>Wide range of values | Damaged by temperature > +105°C<br>Large case size<br>High inductance |
| | Teflon | 0.003%<br>to 0.02% | Low DA available<br>Good stability<br>Operational above +125°C<br>Wide range of values | Relatively expensive<br>Large size<br>High inductance |
| | MOS | 0.01% | Good DA<br>Small<br>Operational above +125°C<br>Low inductance | Limited availability<br>Available only in small capacitance values |
| | Polycarbonate | 0.1% | Good stability<br>Low cost<br>Wide temperature range | Large size<br>DA limits to 8-bit applications<br>High inductance |
| | Polyester | 0.3%<br>to 0.5% | Moderate stability<br>Low cost<br>Wide temperature range<br>Low inductance (stacked film) | Large size<br>DA limits to 8-bit applications<br>High inductance |
| | Monolithic ceramic (High K) | >0.2% | Low inductance<br>Wide range of values | Poor stability<br>Poor DA<br>High voltage coefficient |
| | Mica | >0.003% | Low loss at HF<br>Low inductance<br>Very stable<br>Available in 1% values or better | Quite large<br>Low values (<10 nF)<br>Expensive |
| | Aluminum electrolytic | High | Large values<br>High currents<br>High voltages<br>Small size | High leakage<br>Usually polarized<br>Poor stability<br>Poor accuracy<br>Inductive |
| | Tantalum electrolytic | High | Small size<br>Large values<br>Medium inductance | Quite high leakage<br>Usually polarized<br>Expensive<br>Poor stability<br>Poor accuracy |

As seen from Table 4.1 and Figure 4.3, aluminum electrolytic and film capacitors have the most wide range of values and ratings and therefore they are the mostly used capacitors in power electronics applications.

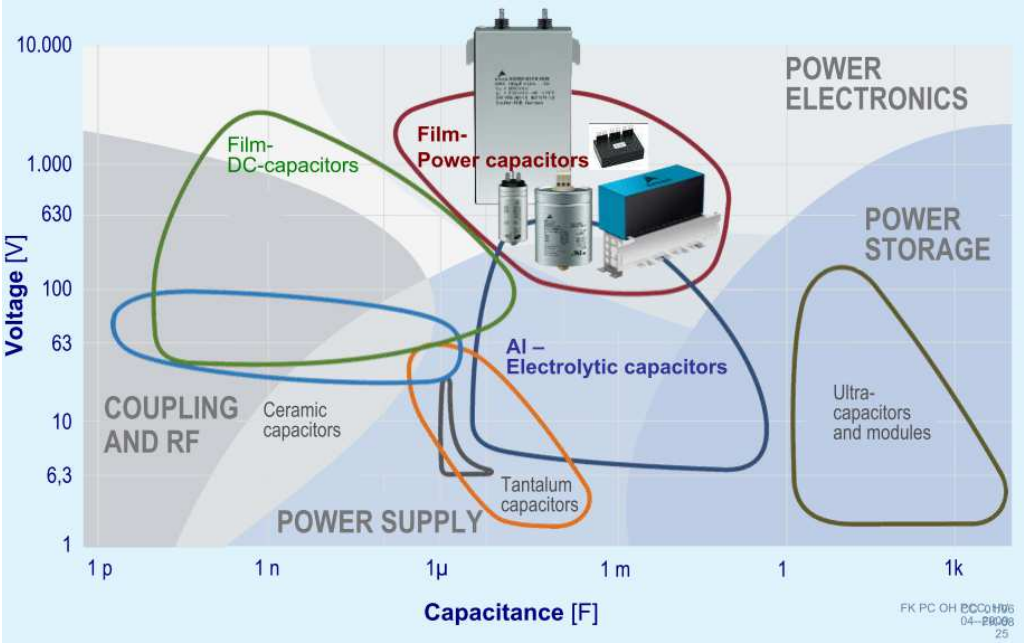


Figure 4.3 Usage of different kinds of capacitors over capacitance and voltage rating plane [19]

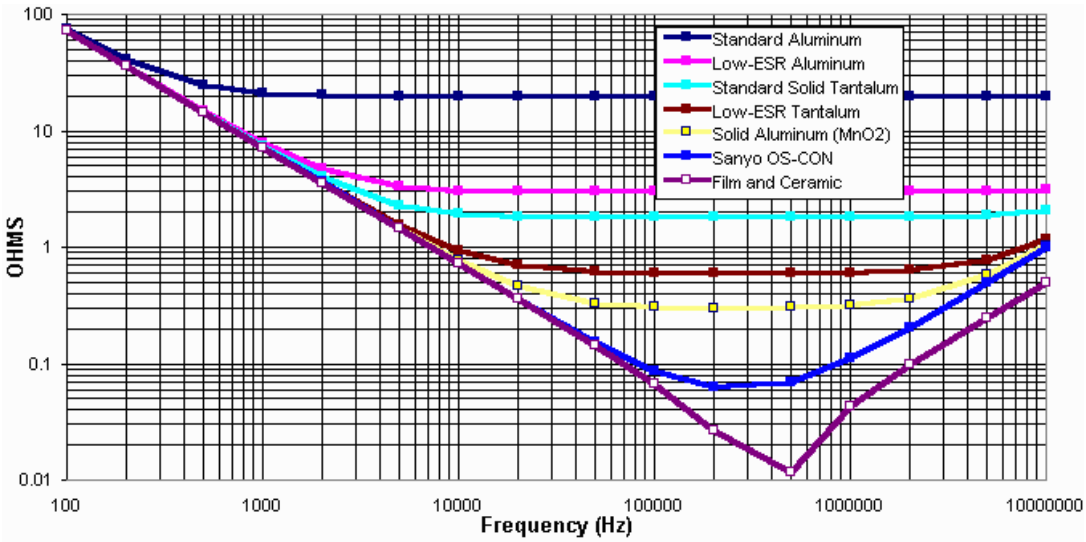


Figure 4.4 Impedance graph of different kinds of capacitors. Inductance of electrolytic capacitors is taken as 0.016 µH and ESR is assumed as constant with frequency [18]

## 4.2 Terminology and Loss Mechanisms in Capacitors

As in Fig. 4.2, when an AC voltage is applied between terminals of a capacitor, this voltage is distributed mainly on ideal capacitive element and resistive element in sub-resonance circuit of a capacitor. Therefore, ac voltage phasor is decomposed into capacitive (axis at 90º) and resistive (axis at 0º) phasors. Moreover, δ and θ angles can be defined as in Fig. 4.2. The Equivalent Series Resistance (ESR) is actually the combined effect of all complex energy loss mechanisms that occur under operating condition. Moreover, the relation between ESR and the capacitive impedance can be formulated as :

$$\tan(\delta) = \frac{ESR}{Z_C} = ESR \cdot \omega \cdot C \qquad (4.1)$$

*tan(δ)* can be also defined as dissipation factor (DF) that defines the ratio of dissipated energy to the stored energy.

The loss mechanisms in capacitor can be listed as follows [21]:

- Dielectric Losses: They are usually the most important losses in film capacitors. These losses are associated with polarization and relaxation of dielectric material. These losses are frequency and temperature dependant such that largest losses occur at highest frequency or lowest temperature. The dielectric losses of a given capacitor can be characterized by its Dissipation Factor (DF).
- Ferroelectric Hysteresis Losses: These losses are observed in high dielectric constant materials such as ceramics.
- Dielectric Conduction Losses: These losses occur as a result of actual transport of charge through nonlinear conductive (highly dependent on applied voltage) dielectric material. These losses are largest at low frequency and high temperatures.
- Interfacial Polarization Losses: In high voltage capacitors, there occurs different dielectric layers that has different conductivity and permittivity and when voltage is applied, charge accumulates along with boundaries of these layers,

This process has low frequency characteristics and important in charge – discharge applications.

- Partial Discharge Losses: This type of losses occur in gas – filled or defective solid capacitors characterized with partial discharge through inside material under high dV/dt changes at high voltages.
- Electromechanical Losses: These are the losses that result from electrostriction of dielectric material or flexing of internal wiring because of Lorentz forces.
- Ohmic Resistance Losses: These losses are caused by resistance effect through metallic electrodes, internal wiring and terminals of the capacitor. In electrolytic capacitors, the ohmic resistance through electrolyte contributes the largest part of ohmic resistance loss.
- Sparking Losses: This phenomenon occurs between conductors and different points on the same conductor during discharging at pulse capacitors.
- Eddy Current Losses: This occurs if large magnetic field in capacitor couples to the ferromagnetic material in capacitor. Since the internal inductance inside capacitors are very small, this type of losses will be very small.

### 4.3 Electrolytic and Film Capacitors in Dc Link Applications

Generally electrolytic and film capacitors are used in the dc bus of an inverter or rectifier. Aluminum type electrolytic capacitors have high capacitance / volume ratio, which makes them ideal to decrease the dc bus voltage ripple (create a stiff dc bus voltage) and introduce high energy storage. Nevertheless, they have considerably high series equivalent resistance (ESR) and as a result, low ripple current rating, typically 20mA / µF [11]. The ESR value of an electrolytic capacitor depends on the dc bias voltage amplitude and frequency of the applied voltage, and the operating temperature as seen in Figure 4.5 and Table 4.2. The ESR increases with voltage, which limits the operating voltage. On the other hand, film capacitors have very low ESR value which is flat over temperature. and their rms current rating is higher (typically 1A / µF) [11]. In addition, they can operate under higher voltage levels. These facts make them very long-life devices compared to electrolytic type and they suit well with circuits with high ripple currents and

voltages at the dc bus. Their energy storage capacity is lower than the electrolytics. Their ESR versus temperature and frequency graph is shown in Figure 4.6.

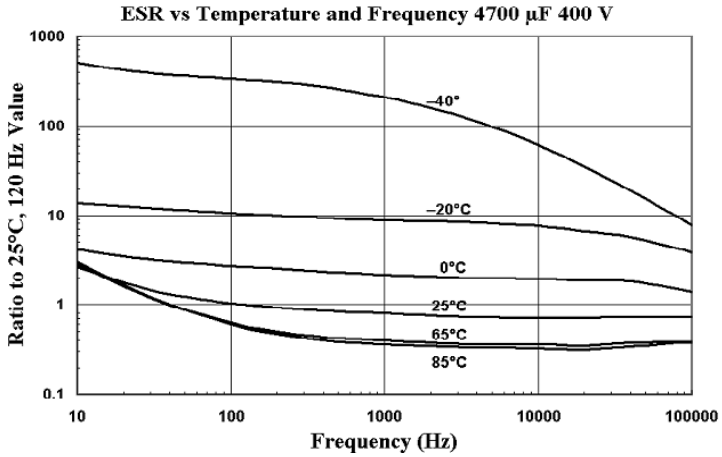


Figure 4.5 ESR of Aluminum Electrolytic Capacitor with ESR:23mΩ @ 120 Hz, 25ºC

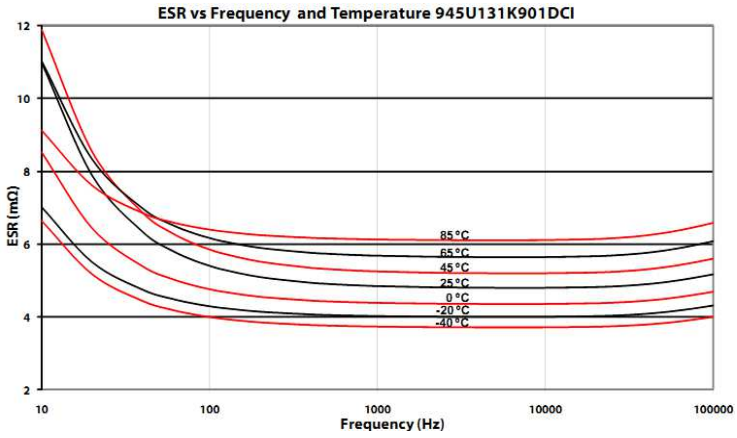


Figure 4.6 ESR of film capacitor [25]

Table 4.2 ESR % ratio to ESR at 25 °C for aluminum electrolytic capacitors

| Rated Voltage $V_{dc}$ | Capacitor Temperature | | |
|---|---|---|---|
| | 45 °C | 65 °C | 85 °C |
| Up to 150 | 82 | 77 | 77 |
| 200 to 300 | 75 | 70 | 70 |
| 350 to 450 | 70 | 60 | 60 |
| 500 | 61 | 49 | 45 |

Electrolytic capacitors are used in low frequency high current ripple applications with their large capacity in a unit volume. These applications cover SRC/Diode rectifier applications at which large low frequency current ripple causes large voltage ripple at DC Bus. In order to suppress voltage ripple, the capacity of dc bus capacitor must be high enough. Because of its electrolyte between foils, the ESR value is higher than the film capacitors. This is because of the power loss in electrolyte [22]. The equivalent circuit of aluminum electrolytic capacitors is shown in Figure 4.7.

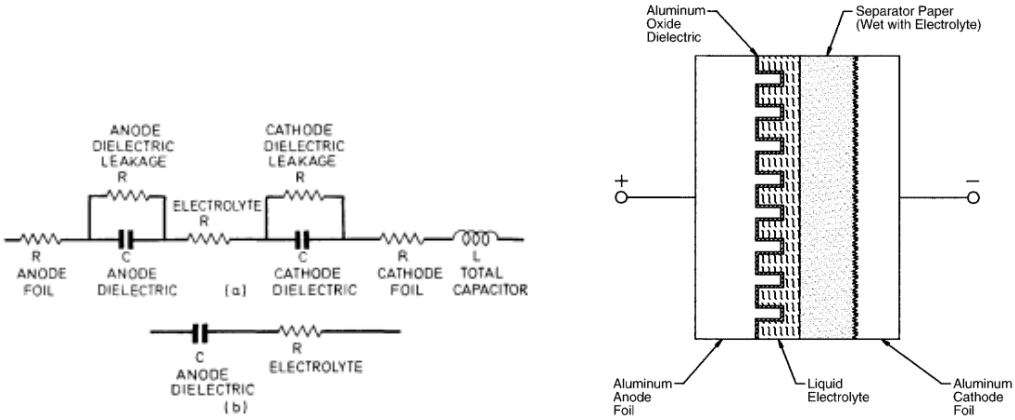


Figure 4.7 (a) Complete internal circuit of electrolytic capacitor (b) Simplified circuit at low frequencies [22]. The internal layer structure of aluminum electrolytic capacitor [23]

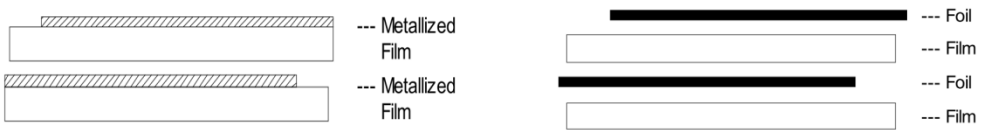


Figure 4.8 Metallized film technology and foil film technology [24]

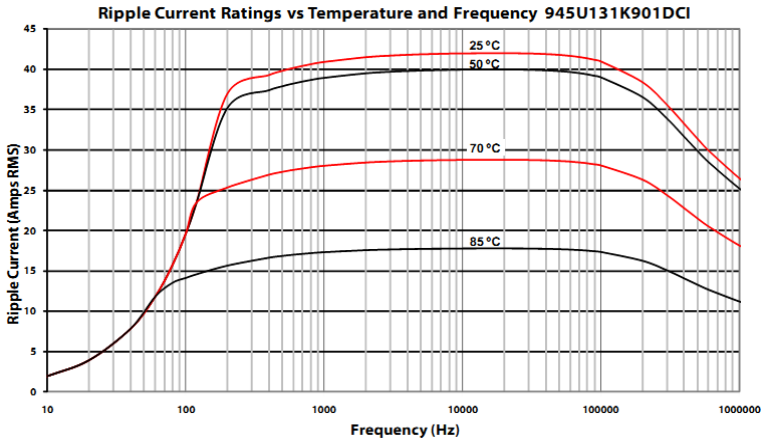


Figure 4.9 Ripple current rating of film capacitor with the ratings: 130µF, 900V [25]

Film capacitors are mainly used in high frequency current ripple (PWM) applications. A typical rms current rating of a power film capacitor is illustrated in Figure 4.9. In order to filter high frequency current ripple, low capacity is sufficient and the low ESR value of film capacitor brings less power loss compared with aluminum electrolytics. In Figure 4.8, the two types of film capacitors are shown. Metalized film technology is newer than film foil technology. In metalized film technology, film layers are covered with very thin metal layer and these layers are stacked. This stacked structure causes ESR to decrease compared with film foil structure. Moreover, the current ripple capacity of stacked film capacitor is higher with the help of its low ESR value and direct terminated electrode structure. Another advantage of stacked-metalized film capacitor is the self healing ability with the aid of clearing effect that is the vaporization of very thin metalized layer at the dielectric breakdown point at the instance of high voltage pulse. By this way, the breakdown point is isolated from other layers.

In power electronics applications which cover the kilowatt to Megawatt range, film or the electrolytic capacitors are the choice with their high capacity, high voltage rating, and high current ripple rating. In wind power applications, where PWM rectifier converts AC to DC, using film capacitor is advantageous over electrolytic capacitors with its small volume, less ESR that means more current ripple, and

higher voltage rating in the order of kV. Moreover, in other applications like renewable power conversion applications such as solar cells and hydrogen fuel cells, where DC power is converted to AC of power grid, and traction drives that is sourced by DC source such as batteries, PWM inverter is the choice and again film capacitor is the best choice with its small volume, high current ripple capability and higher voltage rating compared with electrolytics.

As an example, in a 600 kVA windmill application, 1100 volts rated 1000 µF film capacitor with the dimensions of 203mm x 160mm x 89mm (Length, width, height) replaces the dc bank of 12 electrolytic capacitors that contains 4 branches one of which contains 3 serially connected capacitors, each of which is 350 V, 19.44 Arms rated and has the dimension of 63.5 mm x 110mm (diameter, height) [26]. This shows that the necessary volume of film capacitor is 40% of the volume of electrolytic capacitor bank. Another advantage of the film capacitor is the operating life which is expected as 122000 hours for film capacitor and 20000 hours for electrolytic [26].

In low voltage grid operated diode/thyristor rectifier applications (400Vrms line-to-line voltage rated grid) for motor drives, UPS systems etc., in kW to MW range, electrolytic capacitor is the choice with its large capacity in a unit volume as mentioned in previous sections. Large capacity is needed in the dc bus in order to make a low impedance path for low frequency dc bus current harmonics. Higher voltage levels in these applications involve film capacitors, as illustrated in the previous paragraph example.

Photovoltaic power conversion involving three-phase systems, benefit from the balanced operation and the dc bus capacitor size can be small. As in such applications the converter life is very important from the perspective of return on investment, high life with small film capacitors becomes the favorable choice. Although the electrolytic capacitor technology is suitable in terms of ratings (because the typical dc bus voltage is less than 800V which could be matched by two series capacitors with electrolytic type), here the converter life determines the

design. Several manufacturers have been recently introducing products with film capacitors.

Electrical vehicles, full or hybrid, also benefit from the film capacitor technology. Although the application involves voltage levels less than 500V, the electrolytic capacitor technology has been less and less favorable due to the life issues associated with the high temperature operating environments [27].

In high power battery powered traction motor drives, the dc bus must be designed in a way to bypass the high frequency ripple current sourced from the PWM switching of the VSI. Thus, the choice is the film capacitor with high current ripple rms rating at high frequency. Moreover, film capacitor helps in reducing the voltage transients caused of the leakage inductance and fast switching of the inverter switches [28].

In summary, electrolytic capacitors are widely used in large number of conventional applications in the low voltage grid system, the film capacitors are widely used in high voltage and/or high reliability/long life systems. Therefore, both capacitor types are important for inverter applications and thus, these types of capacitors are focused on in this work, in the design of dc bus capacitor of different PWM VSI applications demonstrated in the next chapter.

In the next chapter, typical operating conditions for PWM VSI and the ripple characteristics at these conditions will be studied with the aid of ripple current analysis tools demonstrated in the chapter 3. After that, some formulations about dc bus capacitor design will be set and a design algorithm will be constructed. Moreover, some dc bus capacitor design examples for typical topologies will be demonstrated.

# CHAPTER 5

# TOPOLOGIES, APPLICATIONS, INVERTER DESIGN AND PERFORMANCE EVALUATION

## 5.1 Introduction

In the second chapter, the inverter applications were reviewed and various application fields, such as motor drives, UPS systems, PWM rectifiers, renewable energy systems, etc. were identified. Although these applications have major differences in terms of user, and ratings, the inverter operating conditions for all these can be summarized in only a few operating modes. Thus, when considering an inverter design for an application, depending on which inverter operating conditions are valid, a simple design approach can be followed. Likewise, performance evaluation becomes an easy task.

This chapter first reviews the inverter applications and classifies the application types into a few inverter operating modes. Following this step, inverter design, including PWM methods selection, dc bus capacitor type and size selection becomes a simple task. With the design completed, the performance can also be evaluated. Depending on whether the application requires a single stage as in the PWM rectifier case, or regenerative motor drive involving back to back inverters, or an alternative structure among the previously discussed, the design and performance evaluation steps are conducted in different manner. Thus, this chapter provides detailed design examples for each of these basic cases.

In this chapter, using the dc link current analysis tools and information about dc bus capacitor characteristics mentioned in previous chapters, some guidelines about inverter design and dc bus capacitor sizing will be demonstrated with application specific design examples and after that R-L-E model based simplified load system simulation results will be demonstrated. Finally, the harmonics at the output of the 3-phase 3-wire VSI will be mentioned briefly with simulation results.

Three-phase, two-level VSIs have three common applications one of which is driving induction motors, servo motors, synchronous generators. Induction and servomotors while operating at low speed require low voltage corresponding to low $M_i$. Also both motors have near unity power factor steady-state behavior in this range. For induction machines high speed operation corresponds to lagging power factor and high $M_i$. For synchronous machines high speed operation typically corresponds to high $M_i$, but near unity power factor due to the field excitation or permanent magnet.

The second involves grid interface like PWM rectifier, uninterruptible power supplies (UPS) system grid side, renewable energy applications such as solar and wind power converters. For this type of operation, power transfer between the power grid involves high $M_i$ and typically the power factor is unity.

The third application involves power supplies where sinusoidal output voltage is generated to feed passive / active loads (which can be considered similar to PWM rectifier application).

DC/AC power supplies and UPS outputs also operate at single frequency and high $M_i$, but the load power factor is typically lagging and less than unity. In summary the operating points described in Figure 5.1 cover most of the three-phase inverter applications.

## 5.2 PWM Method Selection

Considering that the wide range of application fields all fall into a small class of operating conditions, the available PWM methods could be evaluated for these conditions to determine which method is suitable for each application. For the selected operating points, assuming an ac load current with 100A (peak) per phase, and with the parameters of section 3.2.2, the dc bus ripple current rms value and the dominant equivalent harmonic components (termed as mD) have been evaluated and the results are comparatively listed in Table 5.1 for one basic (SPWM) and four advanced PWM methods. The results of the table are obtained from the 3-D graph of Figure 3.14. In the table, $I_{avg}$ is calculated from (3.3).

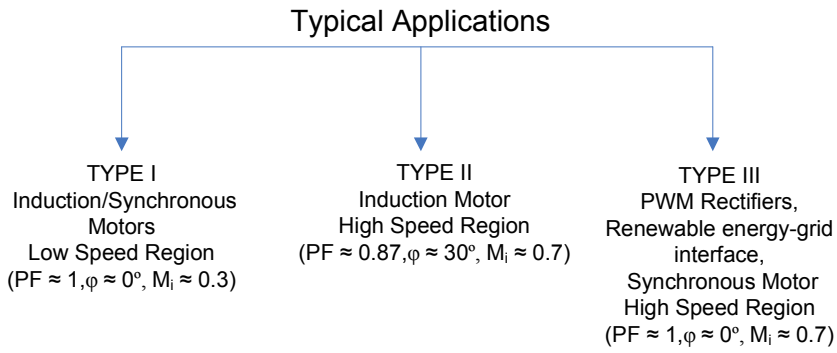


Figure 5.1 PWM inverter applications and typical operating points

Table 5.1 Rms and dominant harmonics of $I_{hf}$ of PWM methods

| PWM method | $M_i$ = 0.3 φ = 0° $I_{avg}$=28,6 A | | $M_i$ = 0.7 φ = 30° $I_{avg}$=58,1 A | | $M_i$ = 0.7 φ = 0° $I_{avg}$=66,8 A | |
|---|---|---|---|---|---|---|
| | ($I_{hf}$ ) rms | mD | ($I_{hf}$ ) rms | mD | ($I_{hf}$ ) rms | mD |
| SPWM | 39,9 | 2 | 36,2 | 2 | 37,7 | 2 |
| SVPWM | 39,9 | 2 | 37,4 | 2 | 39 | 2 |
| AZSPWM1 | 44,2 | 2 | 46,3 | 1,2 | 41,4 | 2 |
| DPWM1 | 40,1 | 1 | 37,4 | 1 | 39,2 | 1 |
| NSPWM | NA | NA | 40,3 | 1 | 25,5 | 2 |

In terms of dc bus ripple current, SPWM supplies the lowest rms value with the dominant harmonic at $2f_c$. SPWM is mostly used in 4-wire applications (3 phase wires + neutral wire) such as UPS grid interface since there is no third harmonic signal injection which causes third harmonic currents to flow to the neutral wire in case of it's existance. The dc bus ripple current performance of SVPWM is very near to the performance of SPWM for all three typical applications. Thus, in 3-wire applications, SVPWM is the substitution for SPWM and it also provides better dc bus voltage usage (wide linear range of $M_i$). For motor drive low speed applications SVPWM is the best method as it has the lowest rms ripple current and the dominant equivalent harmonic is at $2f_c$ (easy to filter). For induction motor drive at high speed AZSPWM1 is the worst method, while other methods exhibit some trade-off relations; SVPWM is the easiest to filter (with harmonics at $2f_c$), DPWM1 has low switching losses and similar rms ripple but more difficult to filter (with harmonics at $f_c$), NSPWM has low common mode voltage and similar rms ripple current characteristics to DPWM1. Thus, depending on the performance priorities set for the application, a method is chosen. For near unity PF and high $M_i$ applications, as it appears clearly from the table, NSPWM is overall better method than all. This section, thus provides the first clear step in inverter dc bus side design by involving the PWM method choice. Having a PWM method selected, the next step involves the dc bus capacitor design depending on the basis of capacitor technology knowledge which is summerized in chapter 4.

### 5.3 Review and Design of DC Bus Capacitors for Inverters

In chapter 2, typical PWM VSI topologies are stated with their dc bus current characteristics and in chapter 4, power electronic capacitors are investigated and film and electrolytic capacitors are focused on with their wide usage in high power / high voltage applications within the scope of this work. Depending on these background data, detailed design works will be done.

Inverters with diode / thyristor rectifier inputs require large capacitors as filters to suppress the low frequency harmonics due to the input side. Thus, in such applications, electrolytic capacitors are the favorable choice, especially in voltage levels 500V or less. If the dc bus voltage is over 500 V, two or more of them are serially connected in order to increase the overall voltage rating. If the input involves a dc supply (such as battery, fuel cell, photovoltaic module) or a high frequency converter (dc-dc converter or, PWM rectifier), in this case, the filtering requirement is at high frequency and small capacitance is sufficient. In such cases film capacitors are favorable, and avaliable in a wide range expanding beyond 500V.

In electrolytic capacitors the component life and performance is highly temperature dependent. The ESR is the dominant loss mechanism, and it is frequency dependent. Especially in the sub kHz range the ESR is high and causes thermal problems if the ripple current is high. Typically not the voltage ripple criteria, but the current ripple criteria dominates the design. Film capacitors used in inverter applications have self-healing property, their thermal reliability is higher and their life is longer. Polyester and polypropylene capacitors are the most frequently used type. Film capacitors can carry more high frequency current than electrolytic capacitors. As a rule of thumb, film capacitor can carry 1A/µF, however, electrolytic capacitor can carry 20mA/µF [11]. In both electrolytic and film capacitor sizing for inverter application, alone with the capacitor manufacturer datasheet information, the ripple current information is necessary to estimate the losses and calculate the voltage ripple. Several papers and application notes elaborate on the design and performance issues of dc bus capacitors [11], [23]-[28].

In the PWM VSI dc bus design, if the dominant peak ripple current ($I_{mD}$, equivalent centered harmonic) at the dominant frequency ($f_{mD}$) is known, and the peak voltage ripple $V_{ripple}$ is specified, then the required capacitance can be calculated as in (5.1). This formula comes from the simplified harmonic model of the dc bus system. The dominat frequency ripple current forces the dominant capacitor voltage harmonic at the same frequency as the impedance formula shows.

$$C = \frac{1}{2\pi \cdot f_{mD} \cdot V_{ripple}} \cdot I_{md} \tag{5.1}$$

In order to calculate the high frequency voltage ripple more precisely, a more accurate $V_{ripple}$ formula can be introduced as in (5.2). In this equation, $I_{dc}$ current is assumed as composed of rectangle pulses and therefore the $V_{ripple}$ voltage is triangular and using parsevals theorem a relation is obtained between $I_{dc}$ harmonics and $V_{ripple}$.

$$\left|\frac{1}{j \cdot \omega_{m1} \cdot C} \cdot I_{m1}\right|^2 + \left|\frac{1}{j \cdot \omega_{m2} \cdot C} \cdot I_{m2}\right|^2 + \cdots \approx \frac{V_p^2}{3} \text{ and } V_{pp} = 2 \cdot V_p = \Delta V_{cdc} \tag{5.2}$$

In three-phase diode rectifier dc bus design, an equation that relates $V_{ripple}$, $V_{max}$, $P_{load}$, and the frequency of pulsed current (f) is necessary to calculate a dc bus capacitance value to suppress $V_{ripple}$ ($V_{pp}$) to a desired level. In a typical three-phase diode rectifier, the ripple current pulsates at six times the fundamental frequency. Assuming the rectifier output current is discontinuous, output load power can be calculated using the energy difference over the dc bus capacitor in a pulsating period. Thus, from the energy difference in a pulse period, from equation 5.3, output power of the rectifier can be related to the dc bus parameters and the pulsating frequency. Moreover, combining it with the power and voltage ripple equation in (5.4), equation of (5.5) is obtained as an approximate dc bus design formula. Given the C value, if the available capacitor has sufficient current ripple capability (to be checked through manufacturer datasheets), then this capacitor can be used. Otherwise, a capacitor with higher current capacity to accommodate the specified ripple current should be selected.

$$\Delta E = \frac{1}{2} \cdot C \cdot \left(V_{dc} + V_p\right)^2 - \frac{1}{2} \cdot C \cdot \left(V_{dc} - V_p\right)^2 = C \cdot V_{dc} \cdot V_{pp}\,, \tag{5.3}$$

$$P_{load} = \frac{\Delta E}{T} = \frac{\Delta E}{\frac{1}{f}} = C \cdot V_{dc} \cdot V_{pp} \cdot f$$

$$P_{load} = V_{dc} \cdot I_{load} \quad and \quad V_{dc} = V_{max} - {}^{V_{pp}}/_{2} \tag{5.4}$$

$$C = \frac{P_{load}}{V_{ripple} * \left(V_{max} - \frac{V_{ripple}}{2}\right) * f} \tag{5.5}$$

The equations of (5.1), (5.2) are used to estimate ripple over dc bus or to find the initial capacitance of dc bus capacitor design algorithm of PWM VSI. Equation of (5.5) is used to estimate the voltage ripple over the dc bus of three-phase diode rectifier or can be also used to find the initial capacitance of dc bus capacitor design algorithm.

Another design tool is the loss calculation of the dc bus capacitor depending on the specs given by the manufacturer. For electrolytic capacitors, DF value of the capacitor is given by manufacturer at low frequency (around 120 Hz). Using this DF data, The ESR of the capacitor at low frequency can be calculated approximately as in (5.6) [29]. Another method of calculation of ESR and DF at high frequencies is as in (5.7) and (5.8) [36]. In this formulation, $ESR_{hf}$ is the ohmic loss at high frequency which has negative temperature coefficient characteristic (1-2 % per ºC near room temperature) and $DF_{LF}$ is the dissipation factor at low frequency usually has a positive temperature coefficient (0.3% per ºC typical). And a typical value of $DF_{LF}$ for electrolytic capacitors is $DF_{LF} = 0.013$ [10] .

$$\tan(\delta) = \frac{ESR}{Z_c} = ESR \cdot \omega \cdot C \tag{5.6}$$

$$DF = DF_{LF} + 2\pi f C \cdot ESR_{hf} \tag{5.7}$$

$$ESR = \frac{DF_{LF}}{2\pi f C} + ESR_{hf} \tag{5.8}$$

The conventional approach uses the worst case (largest) $ESR_{max}$ to find the total ESR power loss of a capacitor employing (5.9). Since the losses in this approach are overestimated, the approach yields an oversized capacitor. The more accurate approach should employ the detailed current harmonic spectrum information and take into account the frequency dependent ESR as in (5.10), where, $I_{\omega 1}, I_{\omega 2}, I_{\omega 3}, \ldots$

are the rms magnitudes of the dominant frequency ripple current components and $ESR_{\omega1}, ESR_{\omega2}, ESR_{\omega3}, \ldots$ are the corresponding ESR values.

$$P_{loss} = I_{rms}^2 . ESR_{max} \tag{5.9}$$

$$P_{loss} = (I_{\omega1}^2 . ESR_{\omega1}) + (I_{\omega2}^2 . ESR_{\omega2}) + (I_{\omega3}^2 . ESR_{\omega3}) + \cdots \tag{5.10}$$

Using the above approach, the ESR losses of an electrolytic capacitor and the ESR related loss part of a film capacitor can be calculated. Moreover, for the film capacitor, the dielectric losses which occur due to voltage ripple should be taken into account separately. However, in medium or high power applications where modulation frequency is up to 20 kHz, the contribution of the dielectric loss part of the formula may be ignored since the dielectric loss part becomes effective over 100 kHz range. Thus, a more general loss calculation formula is obtained in (5.11) which covers all loss components.

$$P_{loss} = I_{mDrms}^2 \cdot ESR_{fmD} + \frac{1}{2} \cdot C_{DC} \cdot V_{ripple}^2 \cdot f_{mD} . tan\delta \tag{5.11}$$

In the proposed approach, first the harmonic current spectrum is taken into consideration. From here the dominant current ripple and its frequency ($f_{mD}$ and $I_{mD}$) are obtained. Then, selecting a capacitor for the given ripple current, the resulting peak to peak voltage ripple $V_{ripple}$ is calculated in (5.1) for PWM driven application or in (5.5) for low frequency application. If this meets the design specification, the loss calculation can be pursued. Otherwise the capacitor value is incremented until the design specification is met. Then, the total dissipation in the film capacitor can be calculated as in (5.11), where the first term involves the ESR losses, which is also the only loss formula for electrolytic capacitor, and the second term involves the dielectric losses. In this formula, $ESR_{fmD}$ symbolizes the ESR of the capacitor at the dominant frequency and $I_{mDrms}$ symbolizes the rms value of the dominant harmonic component of dc bus current.

The capacitor loss calculation thus, in the proposed approach involves (5.11) and in this approach the harmonic current components are the key components. The approach developed for PWM driven applications, is aimed to obtain the simplified harmonic spectrum (illustrating the dominant components and their frequencies in an easy to read normalized look-up table) in Figure 3.14 and it can be used for each PWM method, operating condition, and current magnitude. For low frequency ($I_{LF}$) applications, that forces high dc bus capacity to ensure low dc bus impedance to obtain low voltage ripple on the bus, electrolytic capacitors are the choice with high capacity density as demonstrated in previous paragraphs. However, over 1000V dc bus voltage, three of these capacitors must be connected in series to provide sufficient voltage rating. The series connection decreases the overall capacity of a branch and therefore the capacity density of the branch decreases with the square of the number of the serialized capacitors. Thus, if much voltage ripple is acceptable for low frequency applications of which dc bus is over 1000 V, film capacitors can be the choice for its less volume and long operation life.

In design algorithm, first the converter topology is selected and then a PWM method is chosen that results in minimum $I_{hf}$ rms with maximum dominant harmonic frequency. By this way the current ripple stress on the capacitor, the voltage ripple on dc bus and the dimension of the capacitor will be minimized. After that, depending on the frequency of the dc bus ripple current of the application, two options occur. If application contains frequency current ripple, then film capacitor is chosen to filter high frequency ripple current. If the application contains low frequency ripple current, electrolytic capacitor is chosen to suppress low frequency current ripple with large capacity. After determination of the capacitor type, ripple current rms is calculated and an initial capacitor is chosen due to the voltage ripple criteria. After the power loss calculation with the parameters of initial capacitor, core temperature of the capacitor is calculated, and if the core temperature is below the threshold defined in the spec sheet, design is completed, otherwise, another capacitor is paralleled and the loss calculations are repeated until the core temperature is decreased below the threshold. The flowchart of the algorithm is demonstrated in Figure 5.2.

In this section, the tools and the algorithm which helps in designing the dc bus of three phase PWM inverter/rectifier and three phase diode rectifier are demonstrated. In the next section, these tools will be used in the design examples.

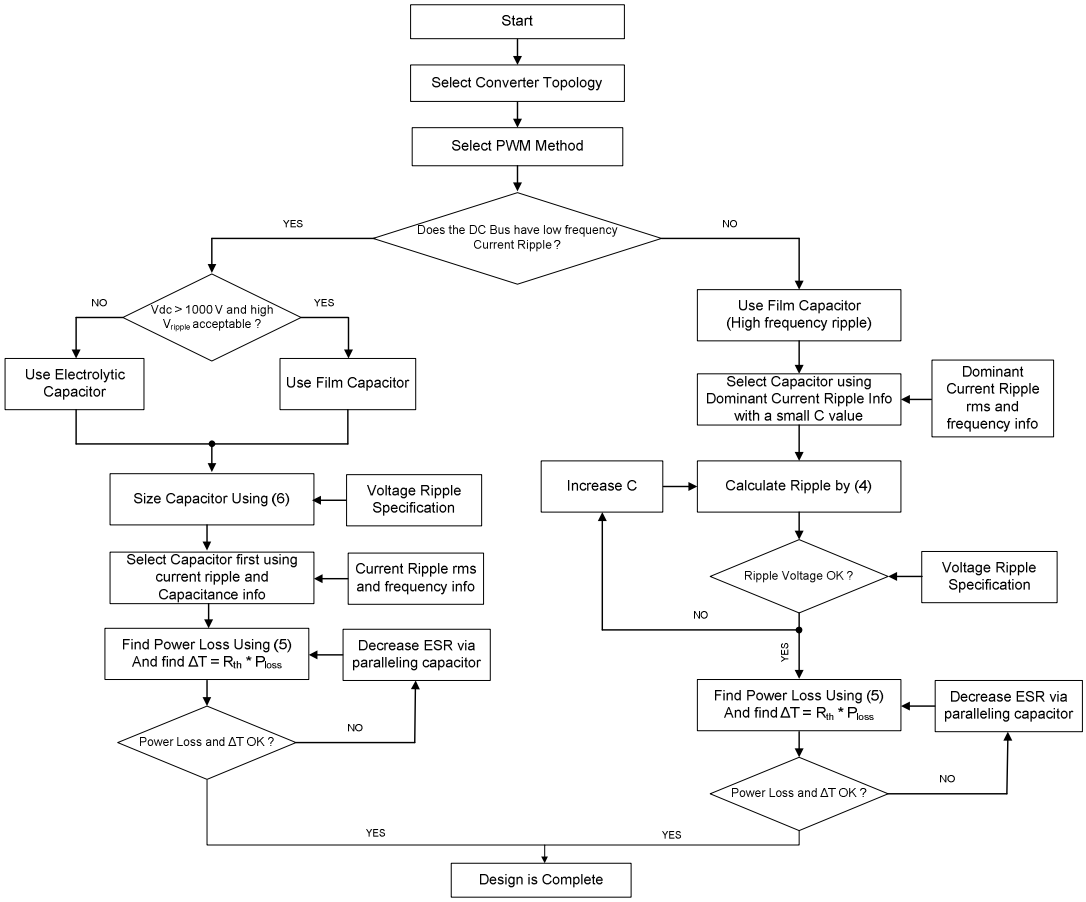


Figure 5.2 Dc bus capacitor sizing flow chart

## 5.4 Design Examples

### 5.4.1 PWM Rectifier Design Example

As previously discussed in chapter 2 and section 5.2, unity power factor with high $M_i$ operation is widely used in many applications. PWM rectifiers, PV systems, are several of many application fields. In such systems, the dc bus mainly experiences high frequency PWM ripple coming only from one side, namely, the inverter side. Since the operation is high frequency, the dc bus capacitor type is film.

In this example, PWM rectifier with 220 V rms input voltage per phase, 46.7 kW input power, 800 V dc bus voltage, 50 Hz grid frequency will be designed. For the rectifier operation, common operating point is $\varphi = 0^o$ and $M_i = 0.7$. Starting with the flow chart in Figure 5.2, first step is to choose the modulation type. From Table 5.1, it is seen that NSPWM is the best method for it results in minimum high frequency current ($I_{hf}$) at maximum dominant harmonic frequency (mD = 2, @$2f_c$). Since the operation is high frequency, the dc bus capacitor type is film. With the design parameters of $V_{dc}$ = 800 V and $I_{in\_max}$ = 100A, $T_A$ = 50°C, $f_c$ = 15 kHz and using 3D graph in Figure 3.14, from $I_{hf\_mD\_rms}$ = 17.7 A and $I_{hf\_rms}$ = 25.5 A, a film capacitor with the following specs can be chosen initially: 220uF, 38A rms @ 10kHz, 7.5 mΩ ESR, $R_{th}$ = 5 °C/W. And calculating the voltage ripple from (5.1), $V_{ripple}$ is found as 6.3 V peak to peak (pp). This is lower than 1% and acceptable. Moreover, the power loss can be calculated, using (5.11), as 4.87 W and this causes a temperature rise (ΔT) of 24.35 °C. This value is also acceptable since $T_c = T_A + \Delta T$ = 74.35 °C and this is lower than 120 °C. Therefore the design is completed.

### 5.4.2 PWM Rectifier Cascaded with PWM Inverter Design Example

This design covers the modern transformerless UPS systems and regenerative motor drives with active front end. Since the system contains input and output sides, different cases must be considered. First case is the 4-wire input UPS system, which contains half bridge topology at the input side that provides neutral wire ($4^{th}$ wire) return and contains 3-wire secondary side. Other case is the 3-wire input, 3-wire output regenerative motor drive system. For both cases, power ratings, dc bus voltage and line frequency are same and the design parameters are listed as follows: 380 V rms input voltage per phase, 81 kW input power, 100A peak current rating for both input and the output, 800 V dc bus voltage, 50 Hz grid frequency.

#### 5.4.2.1 Transformerless UPS System Case

In this case, due to the neutral return of 4-wire input rectifier, third harmonic signal injection can't be applied and the only applicable PWM strategy is SPWM for both the input and output side. The input and the output of the transformerless UPS system is tabulated in Table 5.2. The PWM method of the input side is SPWM with $M_i$ = 0.7, PF = 1 operating point on which real power is transferred between the mains and the input with dominant harmonic at $2f_c$ (mD = 2). For the output side, PF changes between 0.8 and 1. Within this range, $M_i$ = 0.7, PF = 1 operating point causes more ripple current stress as concluded from Table 5.1 and will be used for the design to cover the highest stress point for demanding application.

Table 5.2 Transformerless UPS system operating points

| Input (SPWM, $f_c$=10kHz) | | | | Output (SPWM, $f_c$=10kHz) | | | |
|---|---|---|---|---|---|---|---|
| $M_i$ | PF | $I_{hfrms}$ | $I_{mDrms}$ | $M_i$ | PF | $I_{hfrms}$ | $I_{mDrms}$ |
| 0.7 | 1 | 37.7A | 27.7A | 0.7 | 1 | 37.7A | 27.7A |

Since both rectifier and inverter side high frequency currents contribute to dc bus current harmonics and assuming that the the carriers of input side and the output

side are not synchronized, equation (2.1) is used to combine their effects in rms manner. Therefore, the overall dc bus high frequency current harmonics rms value can be calculated as approximately 53.3 A.

A film capacitor with the following specs can be chosen initially: 130uF, 61A rms @ 10kHz, 1.7 mΩ ESR, $R_{th}$ = 3.4 °C/W. And calculating the voltage ripple from (5.1), $V_{ripple}$ is found approximately as 6.8 V peak to peak (pp). This is lower than 1% and acceptable. Moreover, the power loss can be calculated using (5.11) as 4.8 W and this causes a temperature rise of 16.3 °C. This value is also acceptable since $T_C = T_A + \Delta T$ = 66.3 °C for $T_A$ = 50 °C and this is lower than 120 °C. Therefore, the design is completed for this case with the initially chosen capacitor.

#### 5.4.2.2 Regenerative Motor Drive with Active Front End Case

In this case, both the input and the output are 3-wire and all modulators can be used for both sides. For the input side of which operating point is stated in Table 5.3, and from Table 5.1, it is seen that NSPWM is the best method for it results in minimum high frequency current ($I_{hf}$) and it also results in dominant harmonic frequency of maximum integer index (mD = 2, @$2f_c$) which halves the dc bus impedance that eases filtering of high frequency current. Moreover, for the output side, $M_i$ = 0.3, PF = 1 operating point causes more ripple current stress and will be used for the design to cover the highest stress point for demanding application as concluded from Table 5.1. For the output side inverter, the PWM method is chosen as SVPWM which results in minimum $I_{hf}$ with mD = 2 (halves the dc bus impedance that eases filtering of high frequency current) and more dc bus voltage usage in 3-wire output drive compared with SPWM.

Table 5.3 Regenerative motor drive with active front end

| Input (NSPWM, $f_c$=15kHz) | | | | Output (SVPWM, $f_c$=10kHz) | | | |
|---|---|---|---|---|---|---|---|
| $M_i$ | PF | $I_{hfrms}$ | $I_{mDrms}$ | $M_i$ | PF | $I_{hfrms}$ | $I_{mDrms}$ |
| 0.7 | 1 | 25.5A | 18.2A | 0.7 | 0.87 | --- | --- |
| | | | | 0.7 | 1 | --- | --- |
| | | | | 0.3 | 1 | 39.9A | 34.4A |

Since both rectifier and inverter side high frequency currents contribute to dc bus current harmonics and carrier frequencies are different ($f_c$=10kHz for input side, 15kHz for output side), equation (2.1) is used to combine their effects in rms manner. Therefore, the overall dc bus high frequency current harmonics rms value can be calculated as approximately 47.35 A.

A film capacitor with the following specs can be chosen initially: 130uF, 61A rms @ 10kHz to 30kHz, 1.7 mΩ ESR, $R_{th}$ = 3.4 °C/W. And calculating the voltage ripple from (5.1), $V_{ripple}$ is found approximately as 2.1 V peak to peak (pp) for the input side and 5.96 V pp for output side and getting the square root of the sum of their squares, $V_{ripple}$ is found as 6.3V pp. This is lower than 1% and acceptable. Moreover, the power loss can be calculated using (5.12) as 3.8 W and this causes a temperature rise of 12.9 °C. This value is also acceptable since $T_C = T_A + \Delta T$ = 62.9 °C and this is lower than 120 °C. Therefore the design is completed.

### 5.4.3 Diode/Thyristor Rectifier Cascaded with PWM Inverter Design Example

Starting from the rectifier side and following the algorithm in Figure 5.2, first step is to calculate the dc bus capacitance that provides the desired peak to peak voltage ripple. In order to provide a 5% ripple and from the equation (5.5) and with a quick simulation of rectifier side using the parameters in Table 5.4, the C value is calculated as 6.8 mF. Since the capacitance is large, the voltage ripple contributed from PWM inverter side is negligible.

In motor drive application, asynchronous induction machine high speed operation covers the operating point of TYPE II, pm machine high speed operation covers the operating point of TYPE III, and the low speed drive covers TYPE I operating point. These typical operating points are classified in Figure 5.1. Since TYPE II operating point induces the most stress in terms of dc bus ripple current, the design will be done regarding this operating point as tabulated in Table 5.5.

Table 5.4 Parameters of diode rectifer

| $V_{in\_rms\_per\_phase}$ | $f_{input}$ | $P_{out}$ of inverter | $L_s$ of rectifier input | $C_{dc\ bus}$ |
|---|---|---|---|---|
| 220 V | 50 Hz | 29 kW | 540 µH | 6.8 mF |

Table 5.5 Motor drive application operating points

| Input | Output (SVPWM, $f_c$=10kHz) | | | |
|---|---|---|---|---|
| | $M_i$ | PF | $I_{hfrms}$ | $I_{mDrms}$ |
| Three phase diode rectifier with $I_D$=12.5 A rms @ $f_D$ = 300 Hz | 0.7 | 0.87 | 37.4A | 28.5A |
| | 0.7 | 1 | --- | --- |
| | 0.3 | 1 | --- | --- |

Moreover, 12.5 A rms low frequency current (dominant at 300 Hz) comes from the rectifier side and 37.4 A rms high frequency current comes from inverter side. Since $V_{dc\_max}$ is approximately 500 V, two aluminum electrolytic capacitors must be connected in series and finally, the dc bus capacitor branch is obtained as in Figure 5.3.

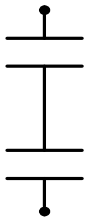

Figure 5.3 Dc bus capacitor branch

Each capacitor is rated as 300V and this gives an overall rating of 600V. And the capacitor block should be rated as $\sqrt{12.5^2 + 37.4^2} \approx 39.4$ A rms. This shows that each capacitor at capacitor branch should be rated as 39.4 A rms at 20 kHz, because dominant current harmonic is at 20 kHz. Therefore, from a catalog of a manufacturer, 14mF, 300V, 43A rms @ 20 kHz current rated aluminum electrolytic capacitor is choosen. Thus, the overall branch capacity is 7 mF because two of them are connected in series. Jumping to the next step of the algorithm, thermal dissipation should be calculated. From datasheet, the ESR at 300 Hz is given as 9 mΩ and ESR at 20 kHz (dominant frequency) is given as 8.3 mΩ. Therefore the power dissipation can be calculated as: $P_{diss} = 12.5^2 \cdot 0.009 + 37.4^2 \cdot 0.0083 \approx 13$ W per cap. This causes a temperature rise of 65 °C for a $R_{th}$ of 5 ºC / W. With a $T_A$ = 50 °C ambient temperature, this results in a core temperature of $T_C = T_A + \Delta T$ = 115 °C for each capacitor. And from $T_C$ is smaller than 120 °C, design is completed.

### 5.5 Comparing Theoric Calculations and System Simulation Results

In this section, dc bus ripple current harmonic spectrum analysis and the voltage ripple on the dc bus will be analyzed via using the Simplorer simulation tool. Moreover, the fft spectrum results will be compared with the spectrums obtained from double fourier analysis.

By using d-q axis controlled PWM rectifier system model, with the flexibility of controlling the phase and magnitude of balanced three phase sinusoidal currents of rectifier input, and also changing the magnitude of the balanced three phase input voltages, all three types (TYPE I, TYPE II, TYPE III) are covered depending on the phasor relation in Figure 5.4. Simulation model is shown in Figure 5.5 and the control model is illustrated in Figure 5.6.

In the simulation model, LF is used to prevent the current ripple to flow to the load side and ESR symbolizes the internal loss of dc bus capacitor ($C_{DC}$).

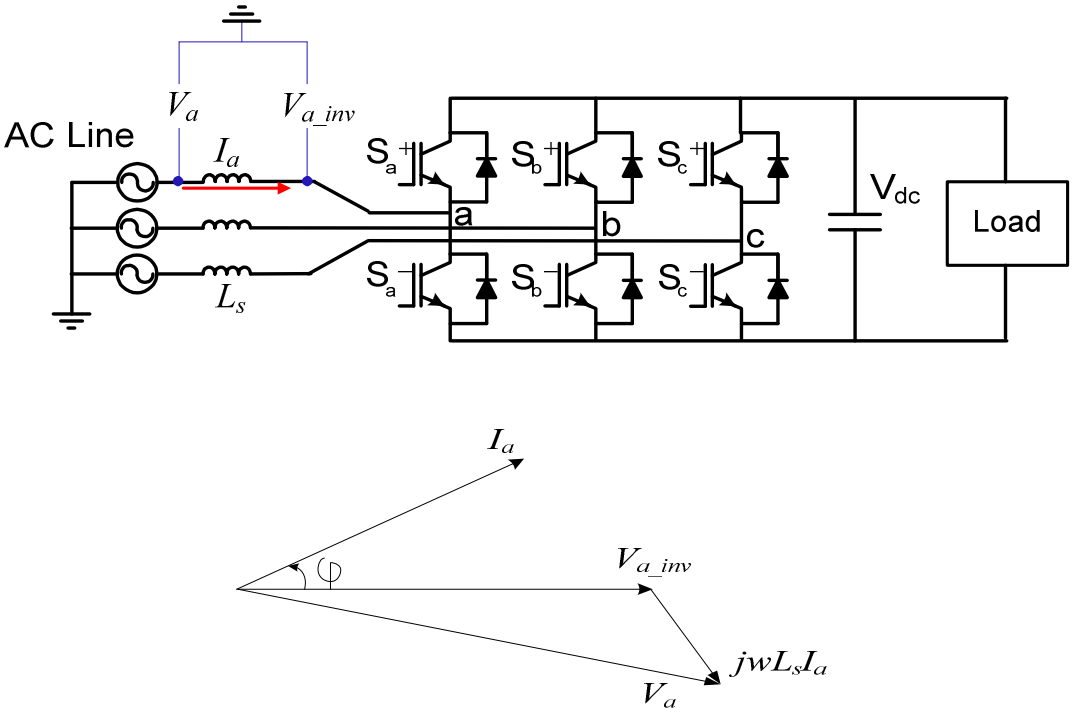


Figure 5.4 Rectifier circuit (top) and phasor diagram (bottom) for lagging power factor operation

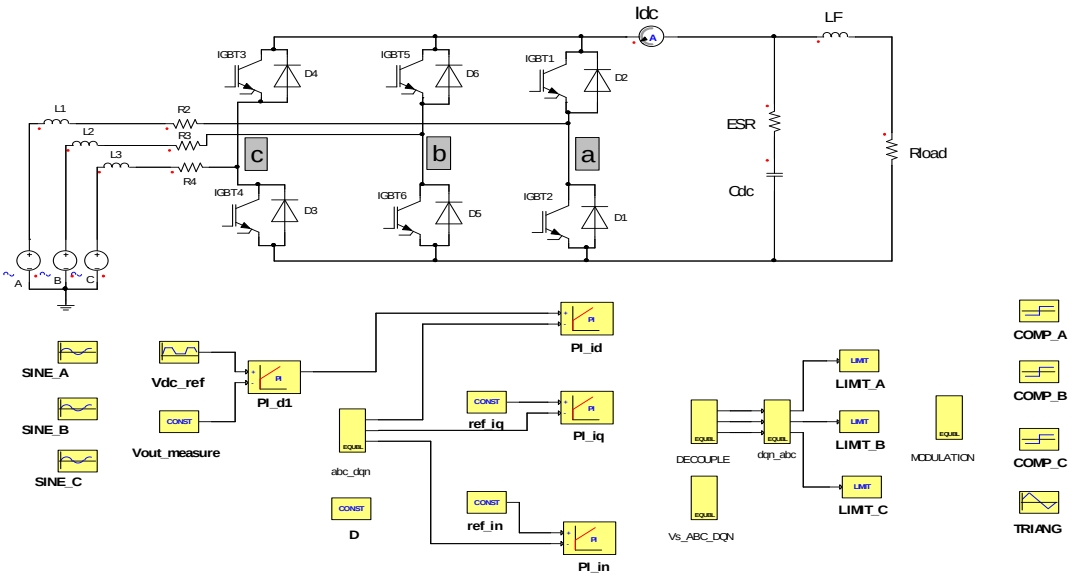


Figure 5.5 Three-wire two-level voltage source rectifier used to simulate R-L-E system.

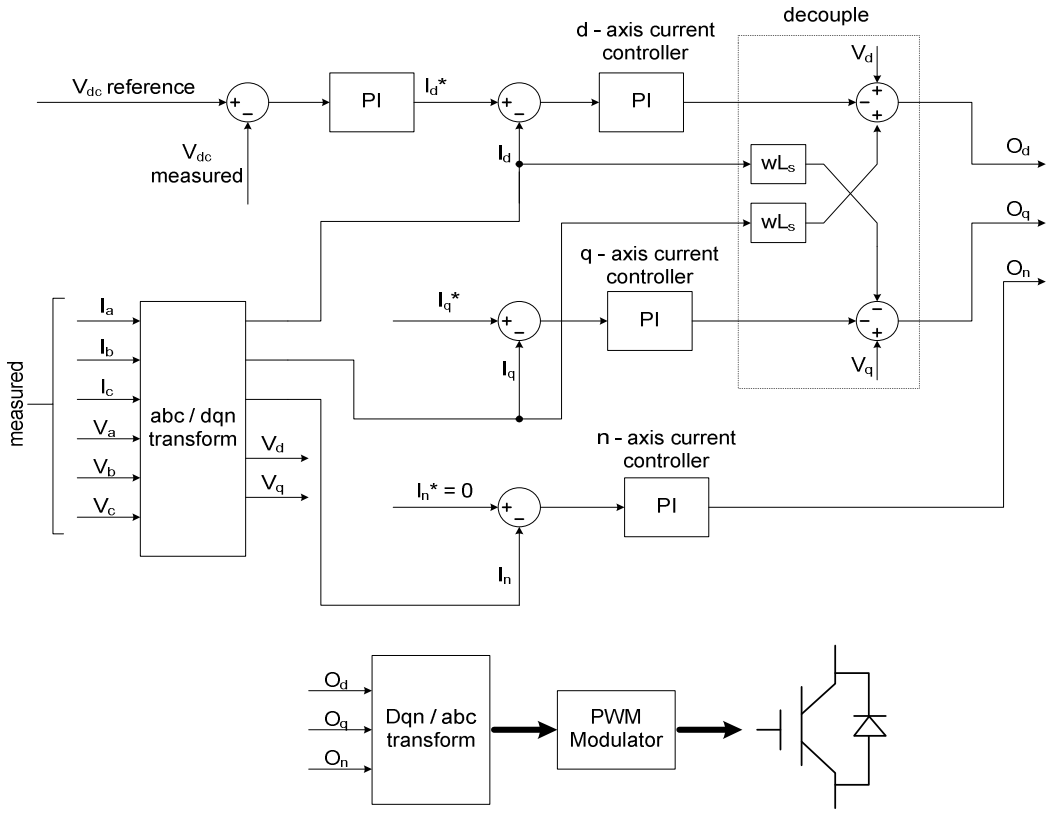


Figure 5.6 Three wire two level voltage source rectifier control block diagram

### 5.5.1 Comparison for Typical Application I

Typical application I parameters are listed in Table 5.6. For TYPE I operating point, NSPWM method is not covered since the $M_i$ is under 0.6. Within remaining modulators, AZSPWM1 causes dominant current ripple harmonic at $2f_c$ with same amount of $2f_c$ harmonic of SVPWM, but the extra harmonic at $f_c$ increases the voltage ripple value. DPWM1 results in current ripple harmonic at $f_c$, but with the advantage of higher carrier frequency which is 1.5 times the $f_c$ of AZSPWM1, voltage ripple value of DPWM1 is lowered below the ripple value of AZSPWM1. Thus, AZSPWM1 results in the highest voltage ripple value within all three modulators. This is agreed with the dc bus voltage and current ripple waveforms of Figure 5.10 and Figure 5.11, also the fft spectrums and double fourier spectrums are well matched.

Table 5.6 Simulation circuit parameters for typical application I

| Modulation type | $M_i$ | PF, φ | $V_{dc}$ (V) | $I_{phase\_max}$ (A) | $V_{phase\_max}$ (V) | $F_c$ (Hz) | $F_{fund}$ (Hz) |
|---|---|---|---|---|---|---|---|
| SVPWM, AZSPWM1 | 0.3 | 1, 0° | 800 | 100 | 154.82 | 10000 | 50 |
| DPWM1, NSPWM | 0.3 | 1, 0° | 800 | 100 | 154.82 | 15000 | 50 |

| $R_{load}$ (Ω) | LF (mH) | $L_{input}$ (mH) | $R_{input}$ (mΩ) | $C_{DC}$, ESR (mF, mΩ) |
|---|---|---|---|---|
| 27.925 | 100 | 0.8 | 20 | 0.4, 5 |

| Modulation type | Dc bus voltage controller PI parameters | | D, q, n axis current controller PI parameters | | $T_s$ |
|---|---|---|---|---|---|
| | $K_p$ | $K_I$ | $K_p$ | $K_I$ | (µsec) |
| SVPWM, AZSPWM1 | 0.5 | 100 | 1 | 75 | 100 |
| DPWM1, NSPWM | 1 | 100 | 3 | 750 | 66.67 |

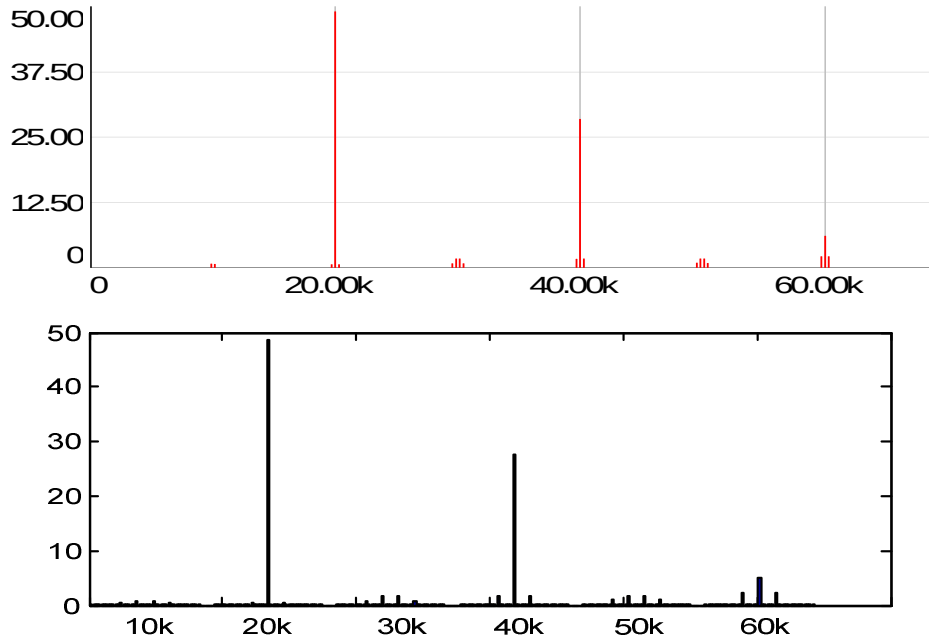


Figure 5.7 $I_{hf}$ spectrum from simulation fft (top, 12.5A/div, 20kHz/div) and $I_{hf}$ spectrum from matlab analysis (bottom, 10A/div) for SVPWM

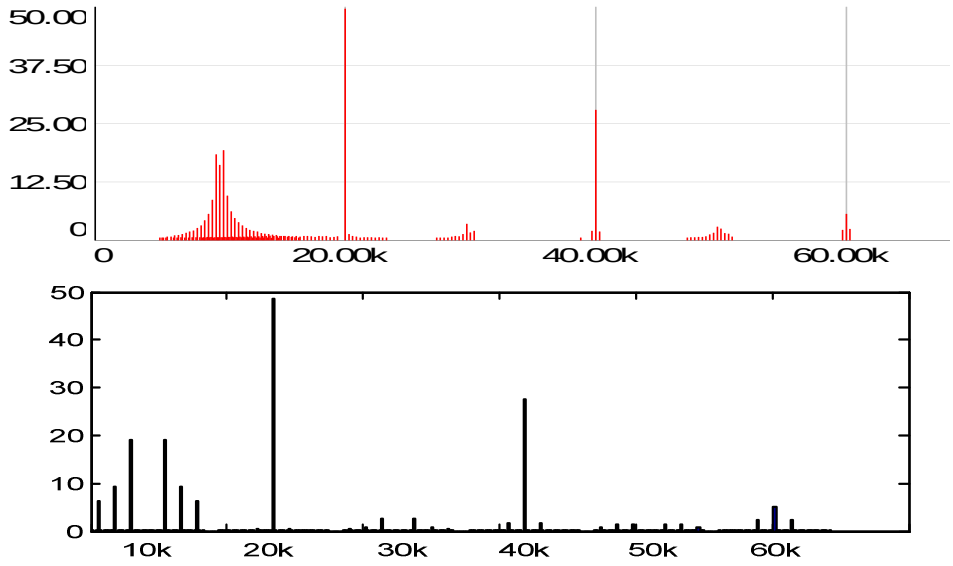


Figure 5.8 $I_{hf}$ spectrum from simulation fft (top, 12.5A/div, 20kHz/div) and $I_{hf}$ spectrum from matlab analysis (bottom, 10A/div, 10kHz/div) for AZSPWM1

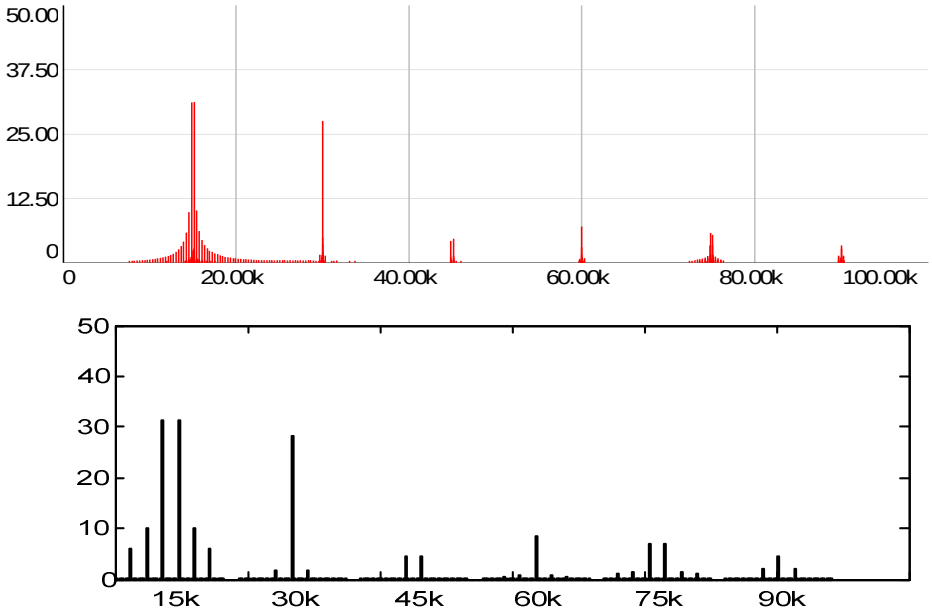


Figure 5.9 $I_{hf}$ spectrum from simulation fft (top, 12.5A/div, 20kHz/div) and $I_{hf}$ spectrum from matlab analysis (bottom, 10A/div, 15kHz/div) for DPWM1

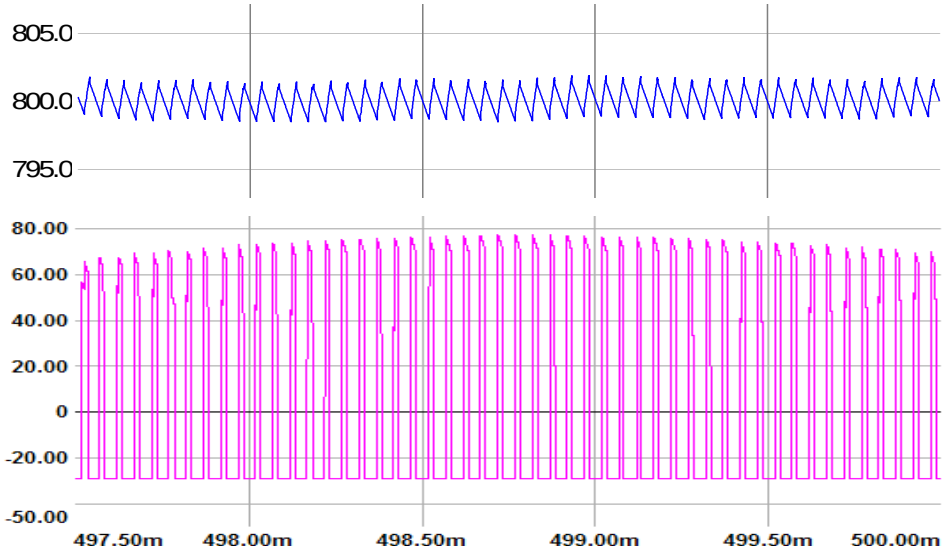


Figure 5.10 Dc bus capacitor voltage waveform (blue, 5V/div) and the $I_{hf}$ current waveform (pink, 20A/div), time axis (0.5ms/div) for SVPWM

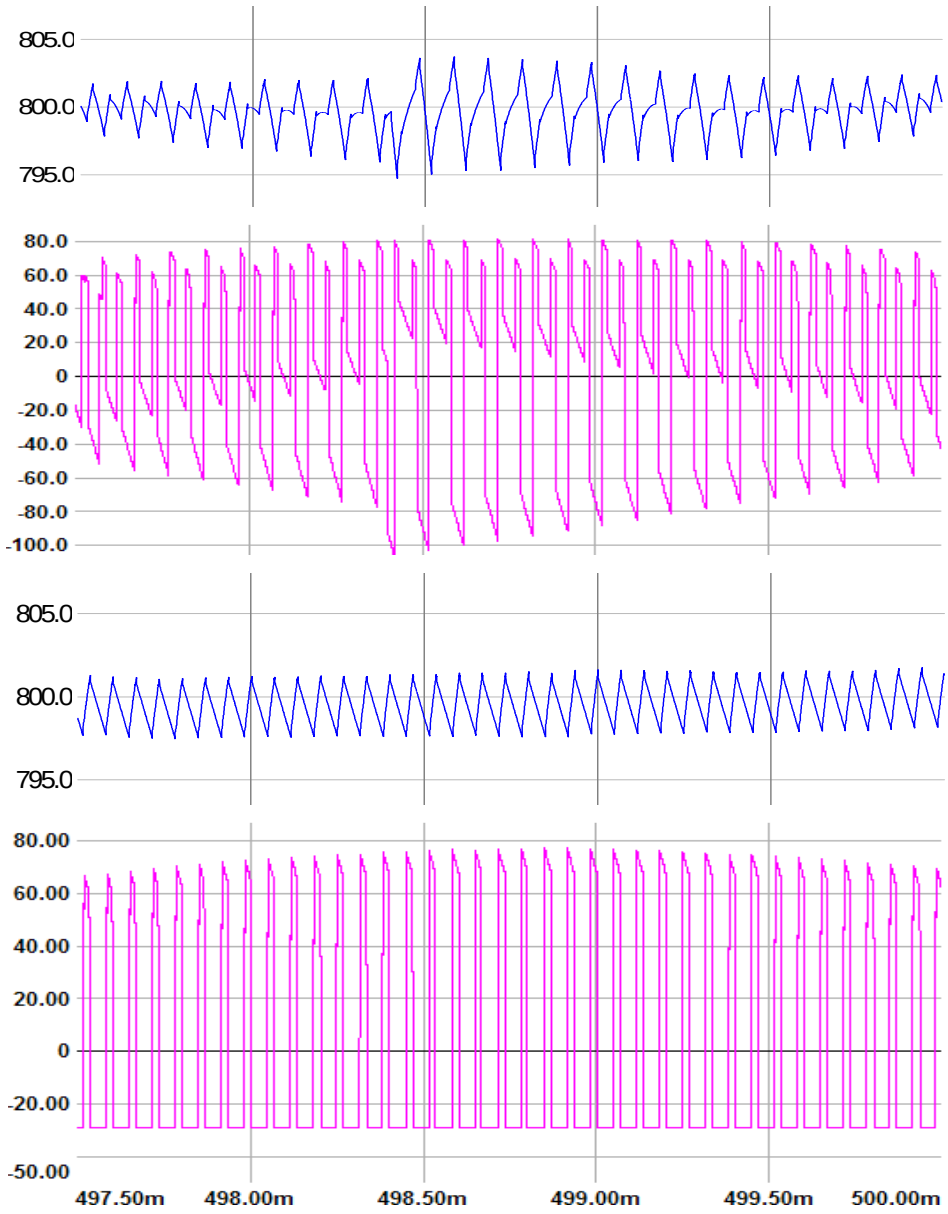


Figure 5.11 Dc bus capacitor voltage waveform (blue, 5V/div) and the $I_{hf}$ current waveform (pink, 20A/div), time axis (0.5ms/div) for AZSPWM1, DPWM1 respectively from top to bottom

### 5.5.2 Comparison for Typical Application II

Typical application II parameters are listed in Table 5.7. For this operating point, the current ripple value of SVPWM is dominant at $2f_c$, however, AZSPWM1 is dominant at both $f_c$ and $2f_c$. Thus the voltage ripple value of AZSPWM1 driven application is higher than the one of SVPWM. NSPWM and DPWM1 current

ripples are also dominant at $f_c$, however, their carrier frequency is 1.5 times the carrier frequency of other modulators and this makes their voltage ripple value lower than the ripple value of AZSPWM1. This is agreed with Figure 5.16 and Figure 5.17, also the fft spectrums and double fourier spectrums are well matched.

Table 5.7 Simulation circuit parameters for typical application II

| Modulation type | $M_i$ | PF, φ | $V_{dc}$ (V) | $I_{phase\_max}$ (A) | $V_{phase\_max}$ (V) | $F_c$ (Hz) | $F_{fund}$ (Hz) |
|---|---|---|---|---|---|---|---|
| SVPWM, AZSPWM1 | 0.7 | 0.87, 30° | 800 | 100 | 369.64 | 10000 | 50 |
| DPWM1, NSPWM | 0.7 | 0.87, 30° | 800 | 100 | 369.64 | 15000 | 50 |

| $R_{load}$ (Ω) | LF (mH) | $L_{input}$ (mH) | $R_{input}$ (mΩ) | $C_{DC}$, ESR (mF, mΩ) |
|---|---|---|---|---|
| 13.819 | 100 | 0.8 | 20 | 0.4, 5 |

| Modulation type | Dc bus voltage controller PI parameters | | D, q, n axis current controller PI parameters | | $T_s$ |
|---|---|---|---|---|---|
| | $K_p$ | $K_I$ | $K_p$ | $K_I$ | (µsec) |
| SVPWM, AZSPWM1 | 0.5 | 100 | 3 | 75 | 100 |
| DPWM1, NSPWM | 1 | 100 | 3 | 750 | 66.67 |

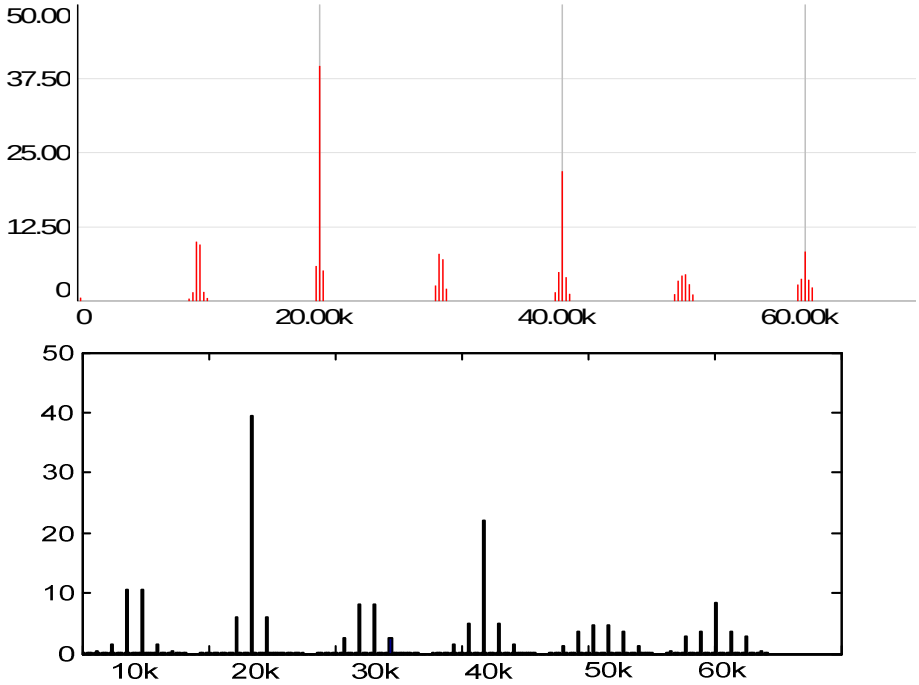


Figure 5.12 $I_{hf}$ spectrum from simulation fft (top, 12.5A/div, 20kHz/div) and $I_{hf}$ spectrum from matlab analysis (bottom, 10A/div, 10kHz/div) for SVPWM

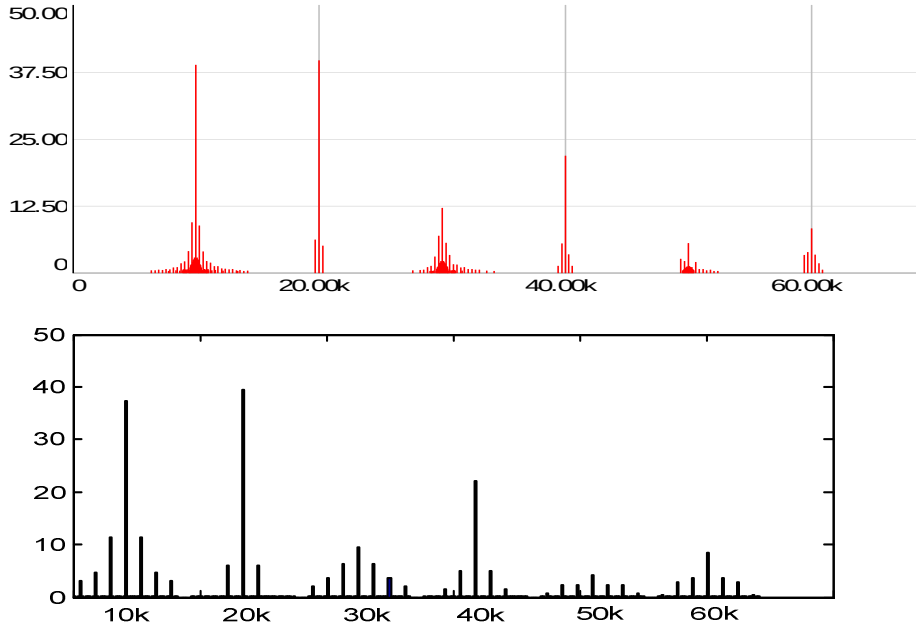


Figure 5.13 $I_{hf}$ spectrum from simulation fft (top, 12.5A/div, 20kHz/div) and $I_{hf}$ spectrum from matlab analysis (bottom, 10A/div, 10kHz/div) for AZSPWM1

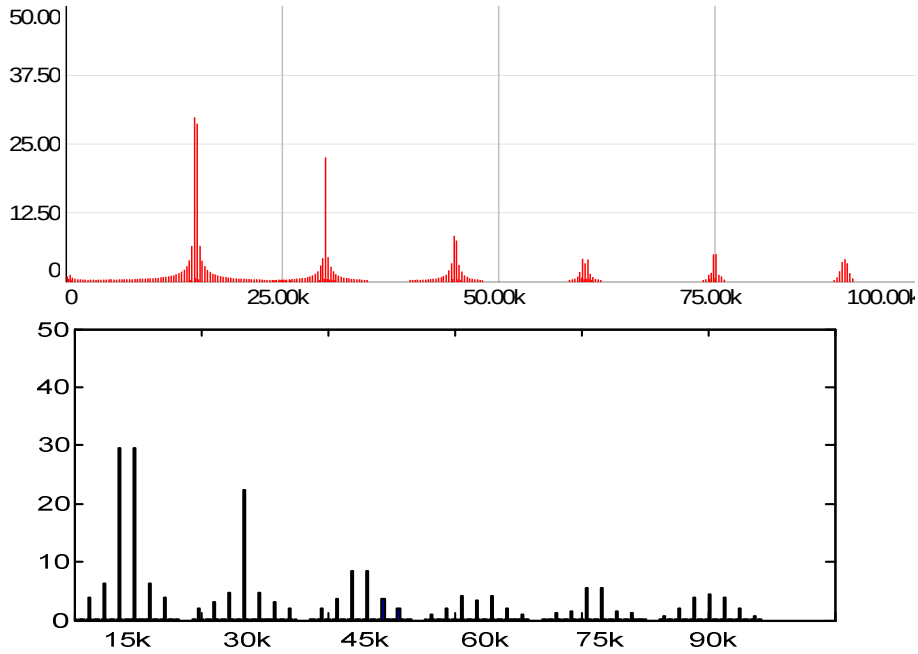


Figure 5.14 $I_{hf}$ spectrum from simulation fft (top, 12.5A/div, 25kHz/div) and $I_{hf}$ spectrum from matlab analysis (bottom, 10A/div, 15kHz/div) for DPWM1

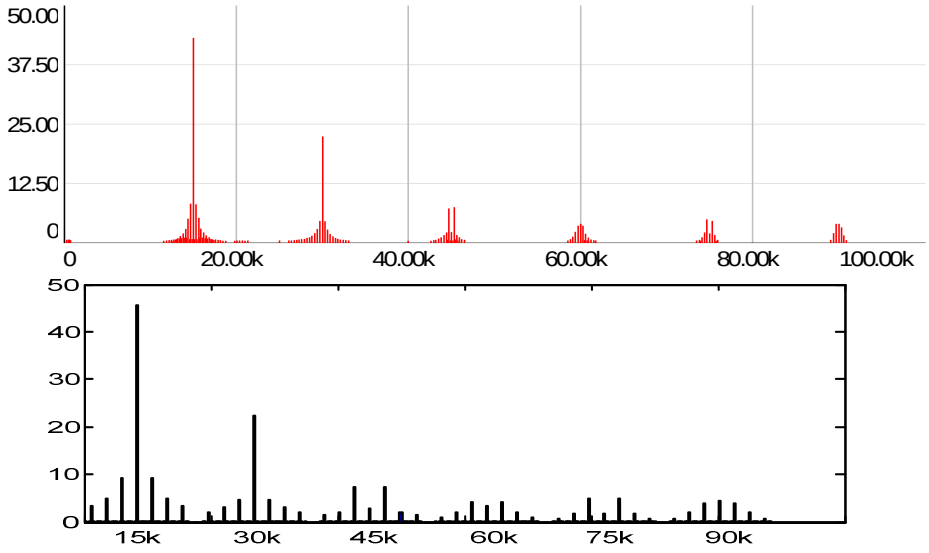


Figure 5.15 $I_{hf}$ spectrum from simulation fft (top, 12.5A/div, 20kHz/div) and $I_{hf}$ spectrum from matlab analysis (bottom, 10A/div, 15kHz/div) for NSPWM

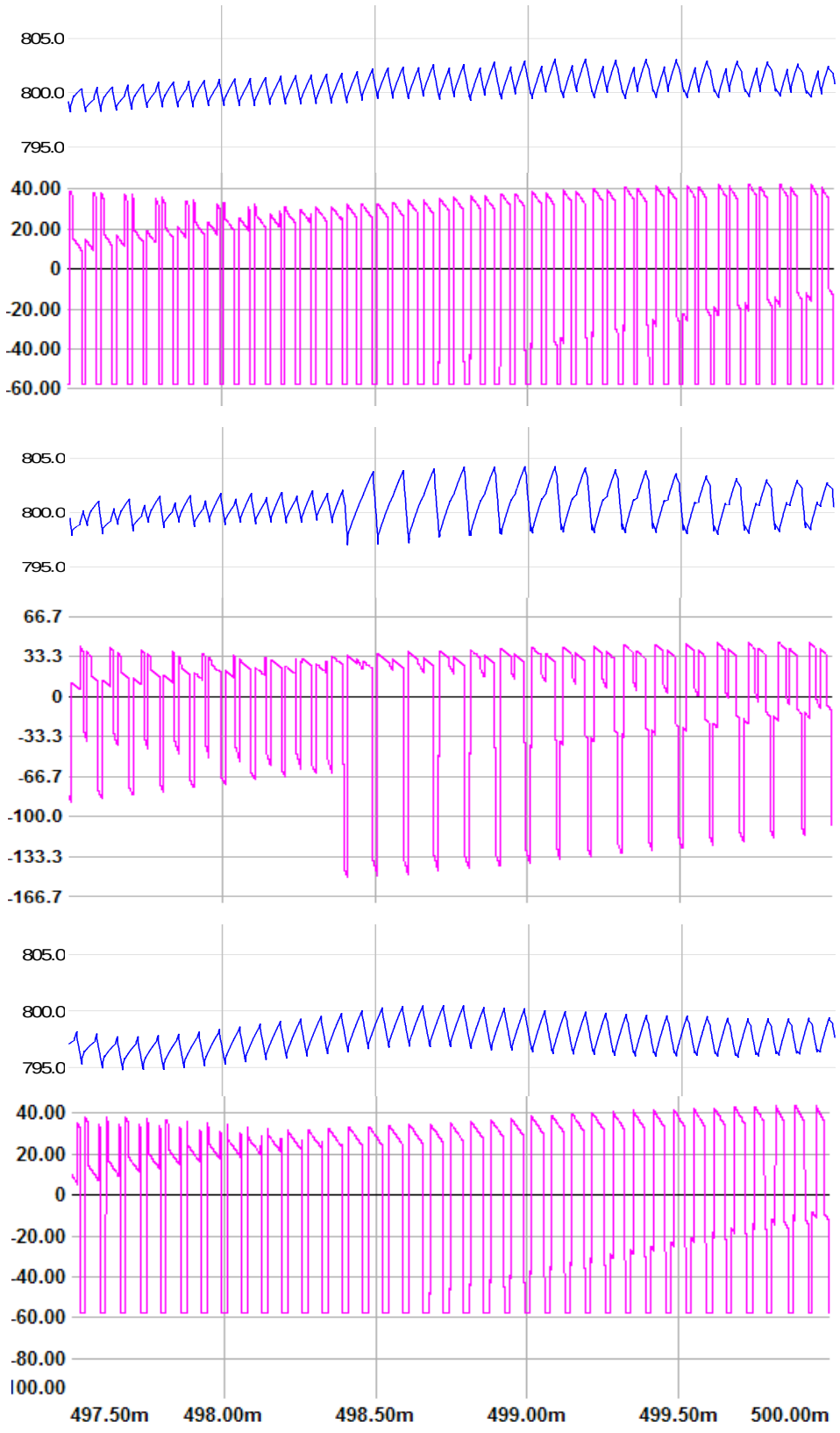


Figure 5.16 Dc bus capacitor voltage waveform (blue, 5V/div) and the $I_{hf}$ current waveform (pink, 20A/div, 33.3A/div), time axis (0.5ms/div) for SVPWM, AZSPWM1, DPWM1 respectively from top to bottom

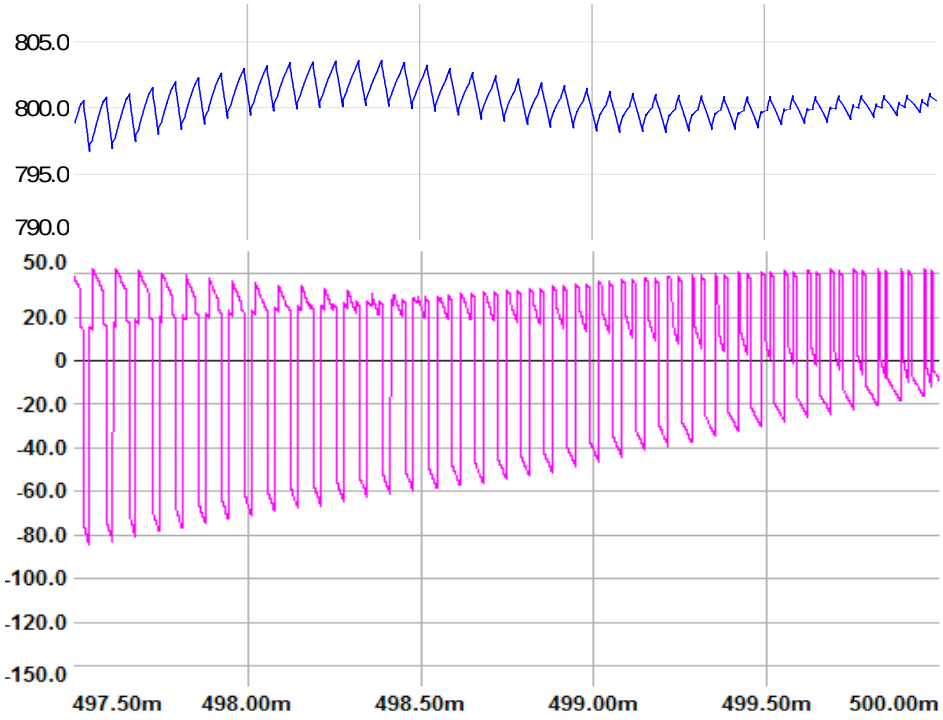


Figure 5.17 Dc bus capacitor voltage waveform (blue, 5V/div) and the $I_{hf}$ current waveform (pink, 20A/div), time axis (0.5ms/div) for NSPWM

### 5.5.3 Comparison for Typical Application III

Typical application III parameters are listed in Table 5.8. In this operating point, as correlated with the current ripple rms value and the spectrum distribution of modulators, NSPWM results in minimum voltage ripple value and SVPWM results in voltage ripple slightly higher than the one of NSPWM. The voltage ripple values of AZSPWM1 and DPWM1 are higher than the ripple values of other modulators. Moreover, AZSPWM1 results in the maximum voltage ripple value of all the modulators. Thus, the voltage and current ripple graphs are as expected and fft spectrums are well matched with the analytical calculation results.

Table 5.8 Simulation circuit parameters for typical application III

| Modulation type | $M_i$ | PF, φ | $V_{dc}$ (V) | $I_{phase\_max}$ (A) | $V_{phase\_max}$ (V) | $F_c$ (Hz) | $F_{fund}$ (Hz) |
|---|---|---|---|---|---|---|---|
| SVPWM, AZSPWM1 | 0.7 | 1, 0° | 800 | 100 | 357.38 | 10000 | 50 |
| DPWM1, NSPWM | 0.7 | 1, 0° | 800 | 100 | 357.38 | 15000 | 50 |

| $R_{load}$ (Ω) | LF (mH) | $L_{input}$ (mH) | $R_{input}$ (mΩ) | $C_{DC}$, ESR (mF, mΩ) |
|---|---|---|---|---|
| 13.819 | 100 | 0.8 | 20 | 0.4, 5 |

| Modulation type | DC bus voltage controller PI parameters | | D, q, n axis current controller PI parameters | | $T_s$ |
|---|---|---|---|---|---|
| | $K_p$ | $K_I$ | $K_p$ | $K_I$ | (μsec) |
| SVPWM, AZSPWM1 | 0.5 | 100 | 3 | 75 | 100 |
| DPWM1, NSPWM | 1 | 100 | 3 | 750 | 66.67 |

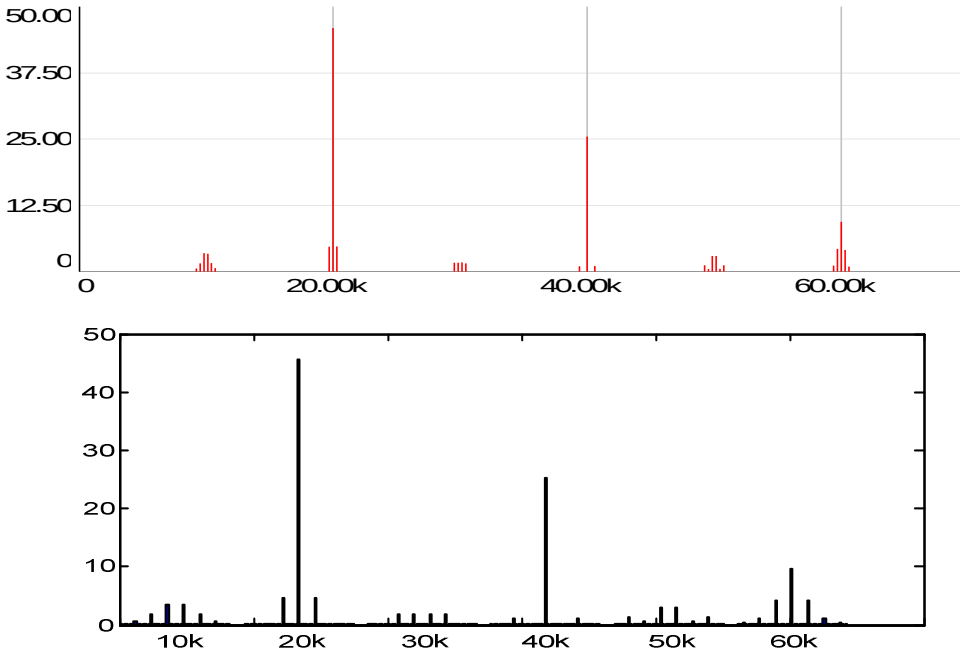


Figure 5.18 $I_{hf}$ spectrum from simulation fft (top, 12.5A/div, 20kHz/div) and $I_{hf}$ spectrum from matlab analysis (bottom, 10A/div, 10kHz/div) for SVPWM

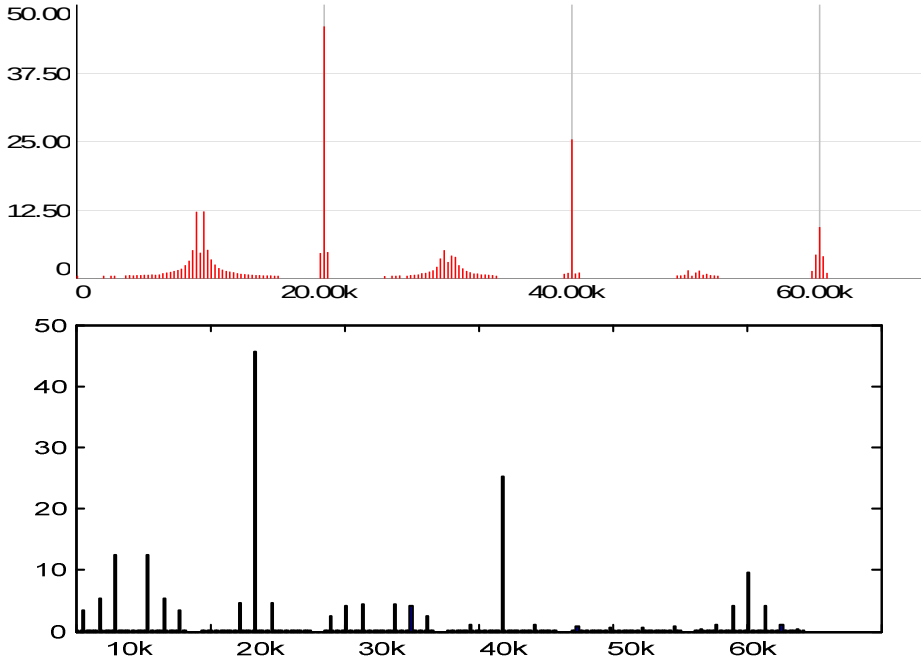


Figure 5.19 $I_{hf}$ spectrum from simulation fft (top, 12.5A/div, 20kHz/div) and $I_{hf}$ spectrum from matlab analysis (bottom, 10A/div, 10kHz/div) for AZSPWM1

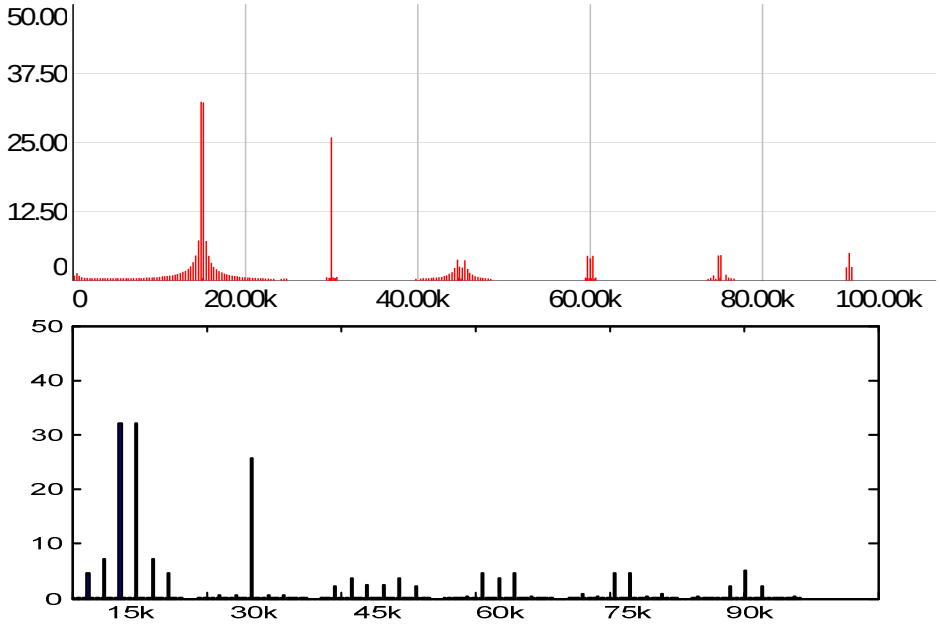


Figure 5.20 $I_{hf}$ spectrum from simulation fft (top, 12.5A/div, 20kHz/div) and $I_{hf}$ spectrum from matlab analysis (bottom, 10A/div, 15kHz/div) for DPWM1

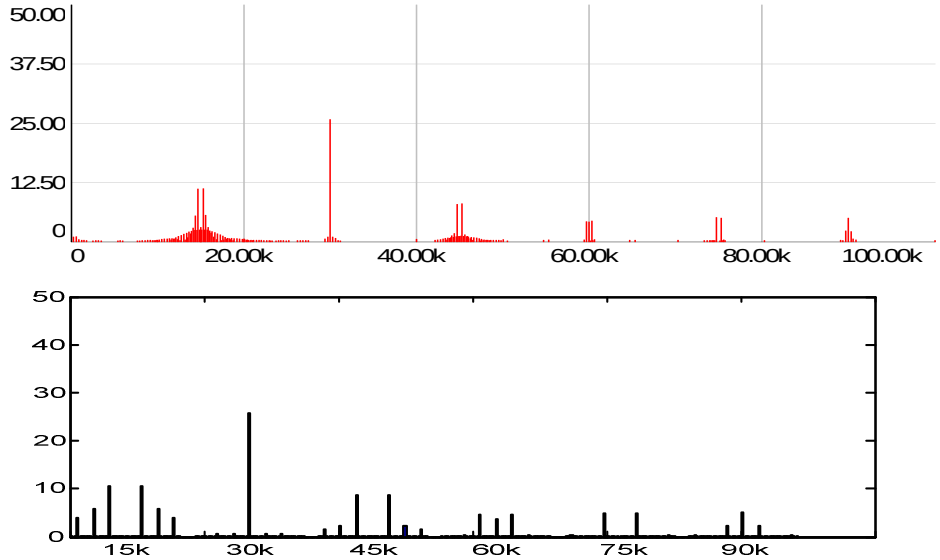


Figure 5.21 $I_{hf}$ spectrum from simulation fft (top, 12.5A/div, 20kHz/div) and $I_{hf}$ spectrum from matlab analysis (bottom, 10A/div, 15kHz/div) for NSPWM

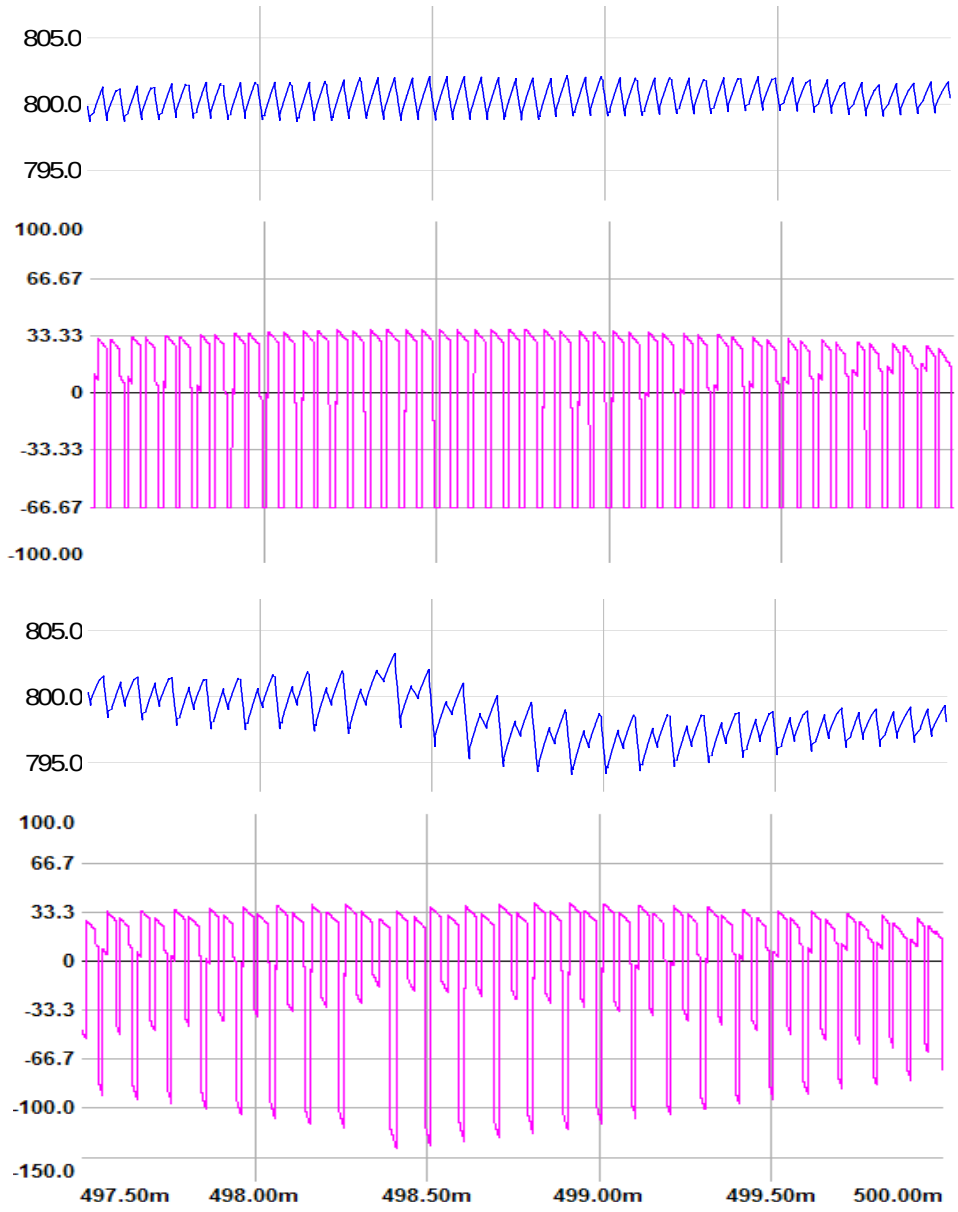


Figure 5.22 Dc bus capacitor voltage waveform (blue, 5V/div) and the $I_{hf}$ current waveform (pink, 33.3A/div), time axis (0.5ms/div) for SVPWM, AZSPWM1 respectively from top to bottom

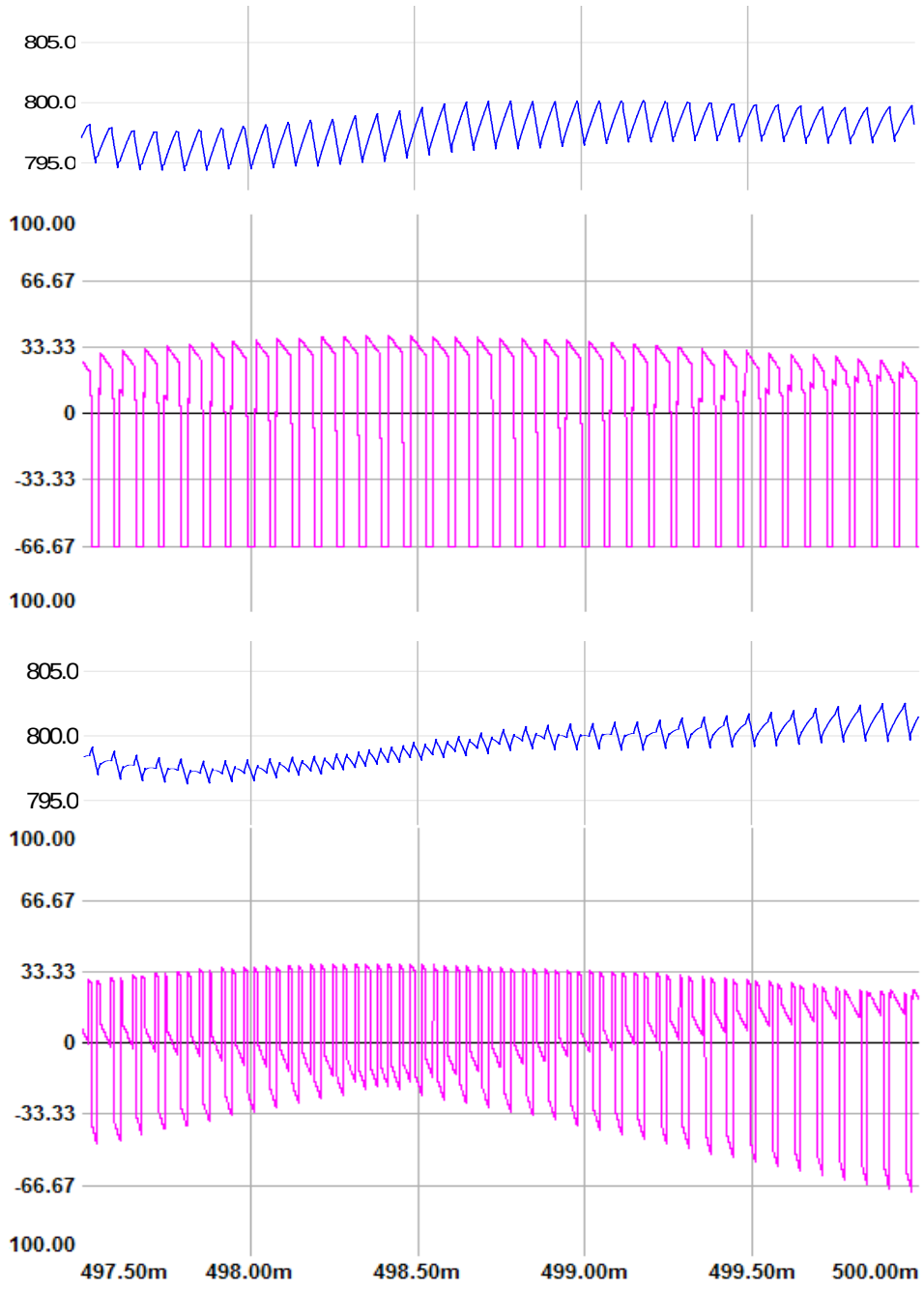


Figure 5.23 Dc bus capacitor voltage waveform (blue, 5V/div) and the $I_{hf}$ current waveform (pink, 33.3A/div), time axis (0.5ms/div) for DPWM1, NSPWM respectively from top to bottom

As demonstrated in the previous graphs, simulation $I_{dc}$ fft graphs and analytically calculated $I_{dc}$ harmonic spectrum graphs are well matched for all three typical application operating points. In typical application I and typical application II,

SVPWM supplies the minimum high frequency voltage ripple over dc bus because of its minimum $I_{hf}$ rms value of which dominant harmonic component is at $2f_c$. In typical application III, NSPWM method usage results in minimum $I_{hf}$ rms value and dominant harmonic component located at $2f_c$. By this way, NSPWM results in minimum high frequency voltage ripple for this application point compared with other modulators. Moreover, it is demostrated that the analytical spectrum calculation results are well matched with the fft spectrum of simulation data for all three application types.

## 5.6 Output Current Harmonic of Two level VSI

In a whole design of a VSI, dc bus design is not sufficient, the AC side must also be investigated to match the desired performance criteria of the whole inverter system. This section supplies supporting information about the AC side and the works in [1] – [5] references could be followed for the detail.

Output phase currents of VSIs are generated by low pass filtering of phase voltage outputs of them. Since phase voltage outputs are composed of harmonic component at line frequency and harmonic component at switching (carrier) frequency and integer multiple of switching (carrier) frequency, a portion of current harmonic at switching and over frequency passes to the output depending on the impedance of output filter at the corresponding frequency.

The two level three wire inverter structure is illustrated in Figure 5.24. In this figure, inverter voltage outputs and the low pass filtered (with the R-L loads at outputs) current outputs are labeled.

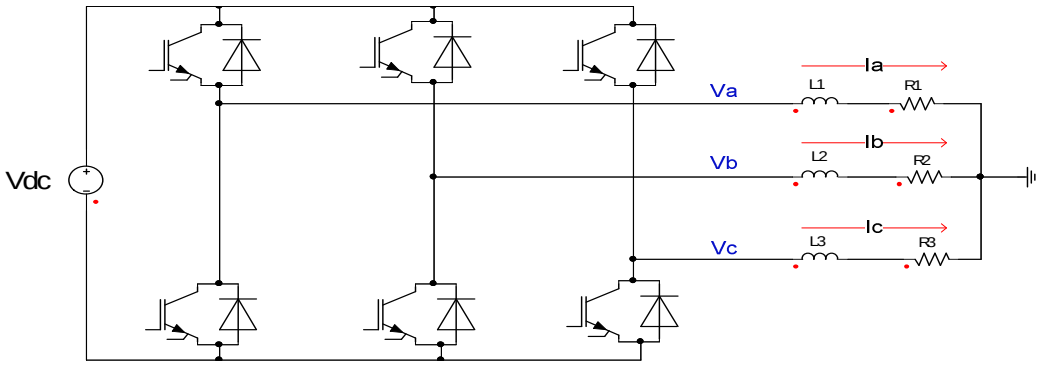


Figure 5.24 Two level 3 wire inverter with low pass filter (R-L) outputs

The $V_a$ voltage at phase a output of inverter is referenced to the ground potential as in Figure 5.24. The $V_a$ voltage and a phase output current ($I_a$) waveforms can be seen in Figure 5.25. Following waveforms are obtained as the simulation result of the open loop inverter circuit in Figure 5.24 with the following simulation parameters in Table 5.9.

Table 5.9 Parameters for inverter

| $V_{dc}$ | $L_{out}$ (mH) | $R_{out}$ (Ω) | Φ (°) | $M_i$ | $I_{omax}$ | $f_c$ (kHz) |
|---|---|---|---|---|---|---|
| 800 | 1 | 3.55 | 0 | 0.7 | 100 | 10 / 15 |

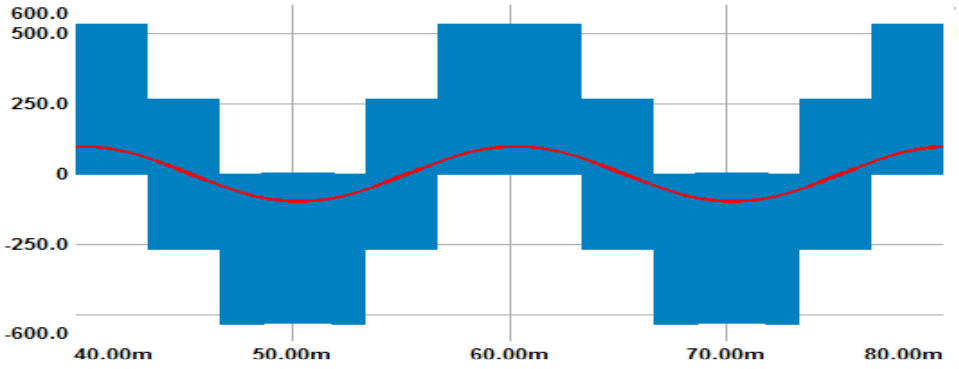


Figure 5.25 A phase output voltage ($V_a$) and a phase output current ($I_a$) waveforms for φ = 0°

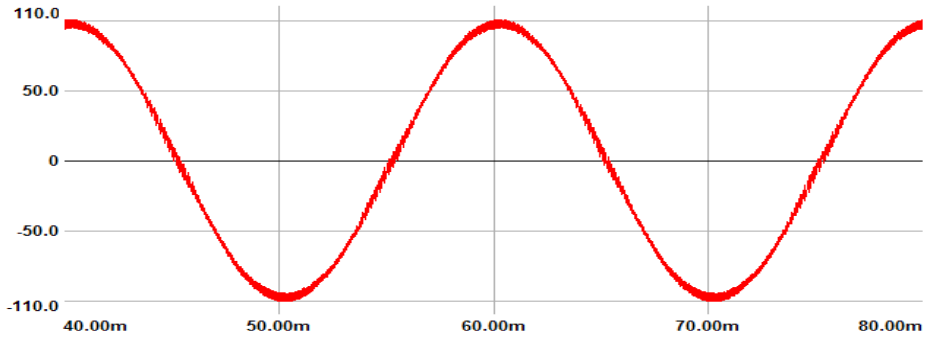


Figure 5.26 Output current waveform for SVPWM

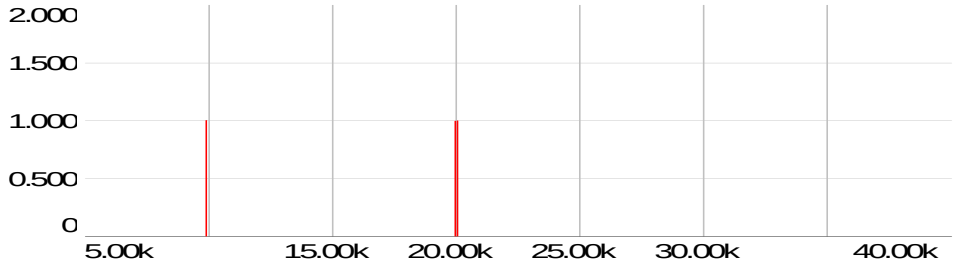


Figure 5.27 High frequency harmonic spectrum of output current ($I_a$) for SVPWM, (0.5A/div, 5kHz/div)

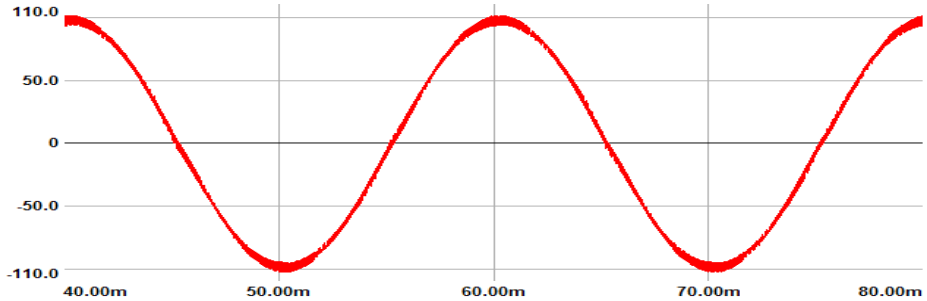


Figure 5.28 Output current waveform for DPWM1, (50A/div, 10ms/div)

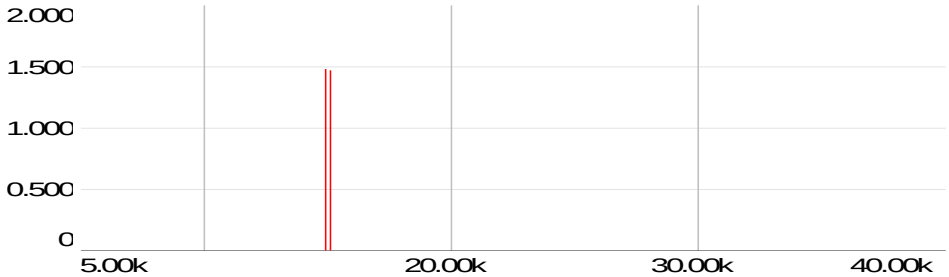


Figure 5.29 High frequency harmonic spectrum of output current ($I_a$) for DPWM1, (0.5A/div, 10kHz/div)

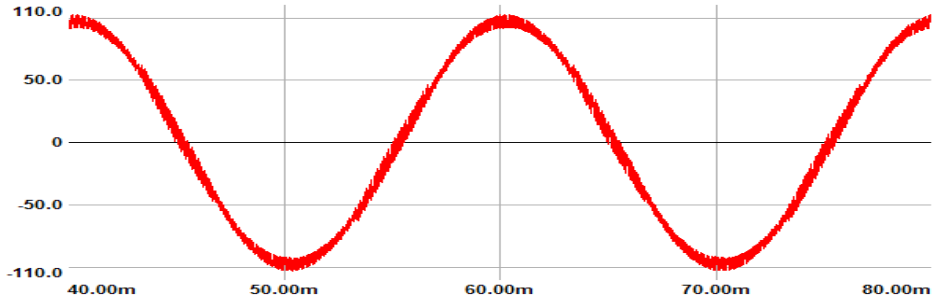


Figure 5.30 Output current waveform for AZSPWM1, (50A/div, 10ms/div)

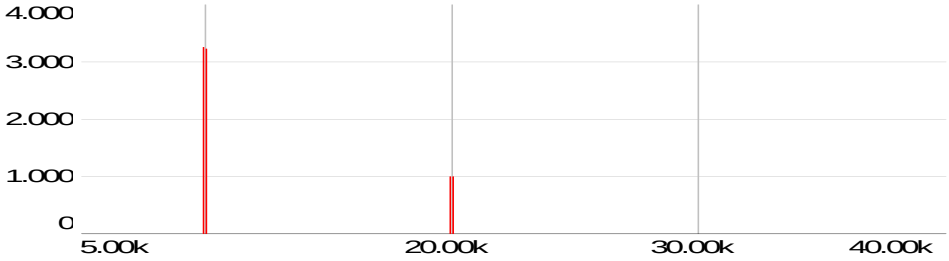


Figure 5.31 High frequency harmonic spectrum of output current ($I_a$) for AZSPWM1, (1A/div, 10kHz/div)

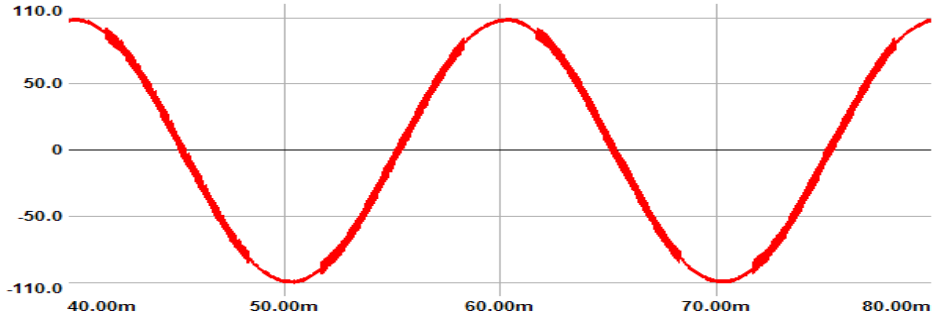


Figure 5.32 Output current waveform for NSPWM, (50A/div, 10ms/div)

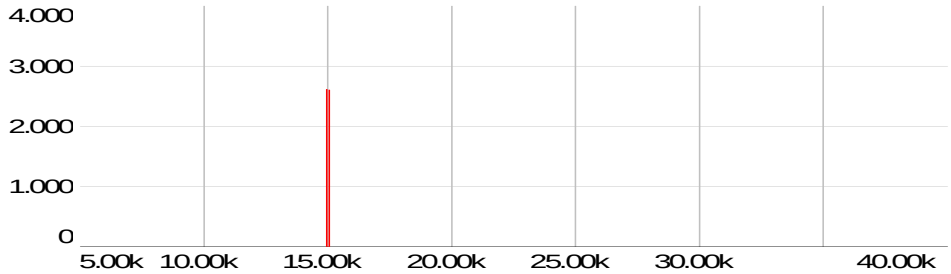


Figure 5.33 High frequency harmonic spectrum of output current ($I_a$) for NSPWM, (1A/div, 5kHz/div)

As illustrated in Figure 5.26, 5.28, 5.30, 5.32, for the given operating point, SVPWM results in the lowest high frequency harmonic content and AZSPWM1 results in the highest high frequency harmonic content at the output of the inverter. The highest high frequency content of AZSPWM1 occurs because of the lack of zero vectors in this modulator. Switching between $V_{dc}$ and $-V_{dc}$ voltage levels increase the voltage harmonic magnitude at the switching frequency and this results in more high frequency current at the output.

In summary, in this chapter, a guide for the design of dc bus of typical three VSI application types with the selection of PWM method is set. Moreover, the design algorithm is applied to the examples for all typical applications. In addition, the performance of all four PWM methods in terms of ripple current and ripple voltage are compared for all application types and the analytical calculation results are compared with the fft spectrum obtained using simulation tool. Finally, supplementary information is given about the AC side of PWM VSI with simulation results.

# CHAPTER 6

# EXPERIMENTAL RESULTS

## 6.1 Introduction

In this chapter, it is aimed to verify the analytical work, which is demonstrated in previous chapters, via experimental results obtained using a three phase diode rectifier cascaded 3-4 kwatt inverter setup. The parameters of the inverter is given in Table 6.1. Dc link current data is collected via using wide bandwidth hall effect current sensor and the sensor probe is connected as in Figure 6.1. The fft analysis of this data set is done on matlab software. Experiment is done in two parts. At first stage, a three-phase 4-kW, 380-V, 4-pole, 1440-$min^{-1}$ rated induction motor is driven under no load operation at $M_i = 0.4$ and $M_i = 0.8$ modulation index points. At the second stage, three-phase star connected balanced RL load (R = 75Ω, L = 3.3mH) is connected to the output of the inverter such that inverter is loaded under rated current condition and dc bus current data is collected for $M_i = 0.4$ and $M_i = 0.8$ points. The operating points of data collection are also given in Table 6.2.

In this experiment, the high bandwidth data collection is obtained via tektronix current probe which has 0.1 Hz to 10 Mhz measurement bandwidth with a sensitivity of 1A/V. It is composed of a hall effect probe and a measurement electronics box which mainly outputs the measured current with the predefined sensitivity scale.

Depending on the limited laboratory conditions, only passive loading is obtained. The induction motor at no load operates mostly reactive and is used for the condition of approximately zero power factor condition ($\varphi \approx 90^{o}$).

Another passive load is the star connected resistance bank with 75Ω per phase, series connected with 3.3 mH per phase inductor to filter out the high frequency voltage ripple of inverter output and to yield sinusoidal output current. Since the overall load is heavily resistive, the approximately unity power factor condition is obtained ($\varphi \approx 0^{o}$).

Table 6.1 Parameters for the motor drive system

| Input | Protection, 3Ø AC line reactor | Bridge rectifier, fuse | Dc bus |
|---|---|---|---|
| Variable transformer cascaded isolation transformer | Three phase circuit braker, 1.8 mH 3Ø reactor | Semikron SKD30/12 1200V, 30A and 20A fuse | Series connected two 2200uF, 450V electrolytic capacitors |

| Inverter switch, gate driver | Controller electronics | $I_{dc}$ measurement | $I_o$ measurement |
|---|---|---|---|
| SKM75GB123D dual pack IGBT modules, Skyper 32 Pro gate driver module | TMS320F2808 fixed point DSP, peripherals, A/D converters | Tektronix hall effect current probe | LEM LA25 P/SP1 hall effect current transducer |

Table 6.2 Operating points for experimental data

| PWM | No load motor exp. (φ≈90°) | | | | RL load exp. (φ≈0°) | | | |
|---|---|---|---|---|---|---|---|---|
| | $M_i$ | | $f_c$ (kHz) | | $M_i$ | | $f_c$ (kHz) | |
| | 0.4 | 0.8 | 10 | 15 | 0.4 | 0.8 | 10 | 15 |
| SV | X | X | X | | X | X | X | |
| AZS1 | X | X | X | | X | X | X | |
| DP1 | X | X | | X | X | X | | X |
| NS | | X | | X | | X | | X |

As mentioned in first paragraph, fft data of $I_{hf}$ current of dc bus capacitors are taken for the defined operating points, then the data are transferred to matlab environment and these fft spectrums are plotted via matlab graphic tool. In Figure 6.6, the spectrum of a modulator is shown plotted up to 6 multiple of $f_c$. Since, the magnitudes decrease with increasing integer multiple of $f_c$, and the dominant harmonics are located in $f_c$ or $2f_c$, only the spectrum covering this frequency range is zoomed and analyzed.

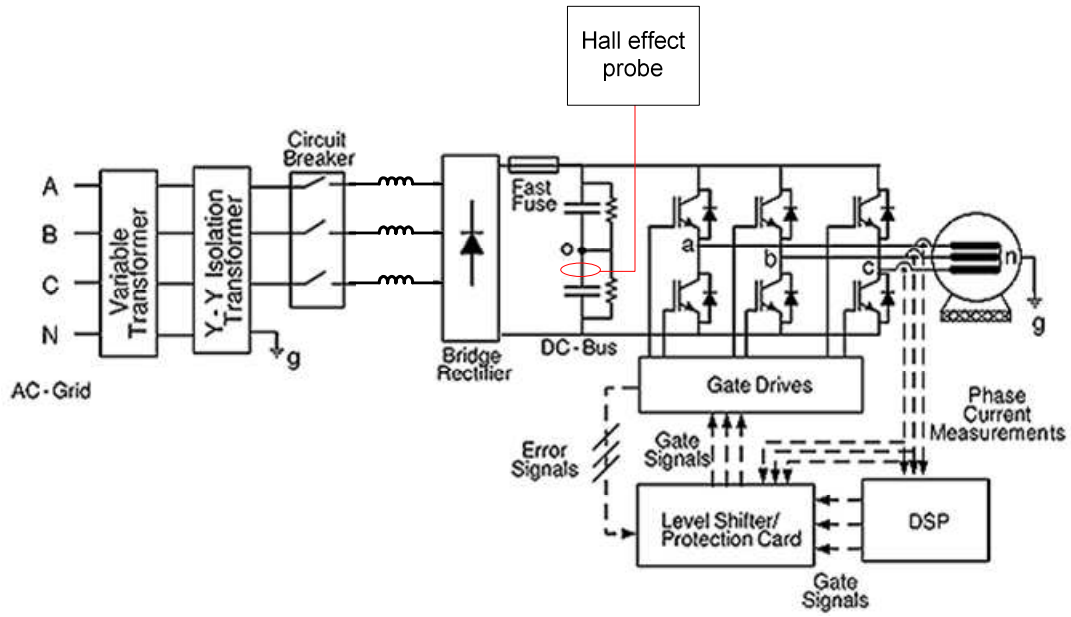


Figure 6.1 The motor drive system of experimental work

### 6.2 No load induction motor experiment results

In this experiment, induction motor is driven under two v/f ratios depending on two modulation index points of $M_i$ = 0.8 and $M_i$ = 0.4. For $M_i$ = 0.8, and for the dc bus voltage of $V_{dc}$ = 500V, v/f ratio is obtained as 5.092 $V/s^{-1}$ and for $M_i$ = 0.4, v/f ratio is obtained as 2.546 $V/s^{-1}$ for the same $V_{dc}$.

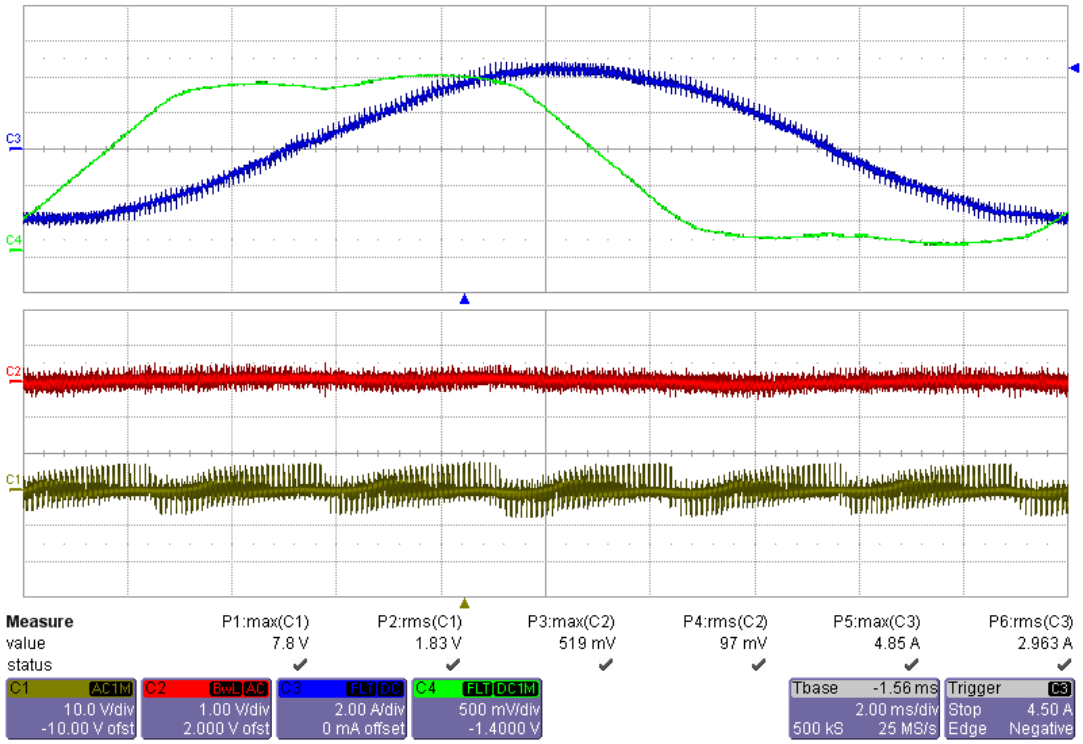


Figure 6.2 Modulation waveform (green, 0.5V/div), output current waveform (blue, 2A/div), dc bus voltage (red, ac coupled, 1V/div) and $I_{hf}$ current (brown, 10A/div), time axis (2ms/div) for SVPWM, $M_i$=0.8, $f_c$=10 kHz

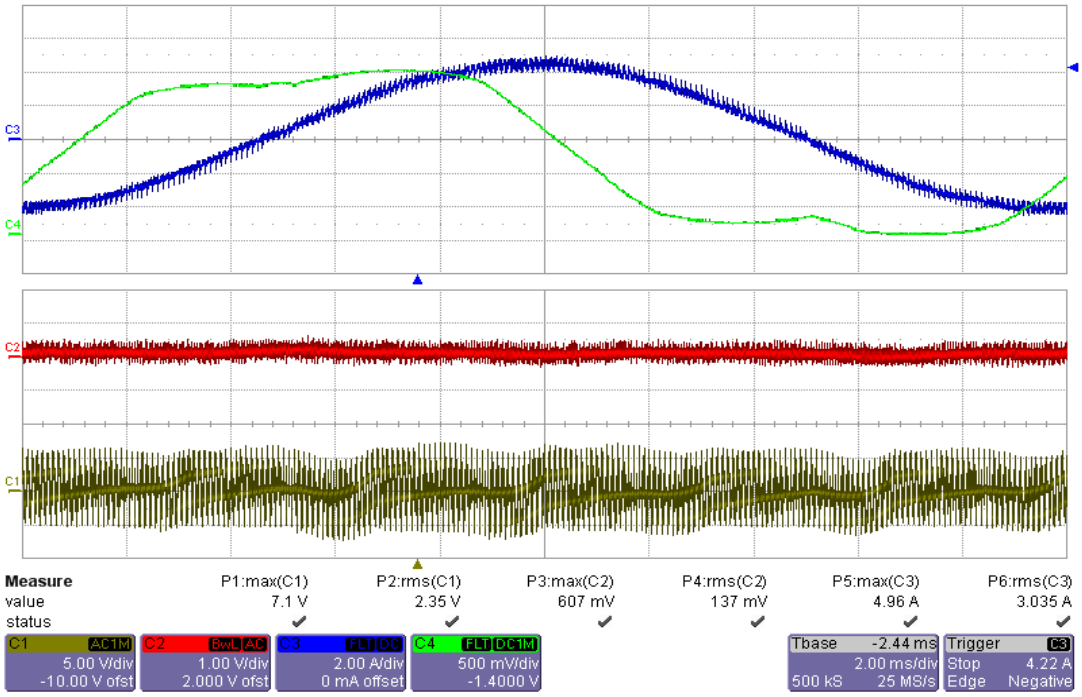


Figure 6.3 Modulation waveform (green, 0.5V/div), output current waveform (blue, 2A/div), dc bus voltage (red, ac coupled, 1V/div) and $I_{hf}$ current (brown, 5A/div), time axis (2ms/div) for AZSPWM1, $M_i$=0.8, $f_c$=10 kHz

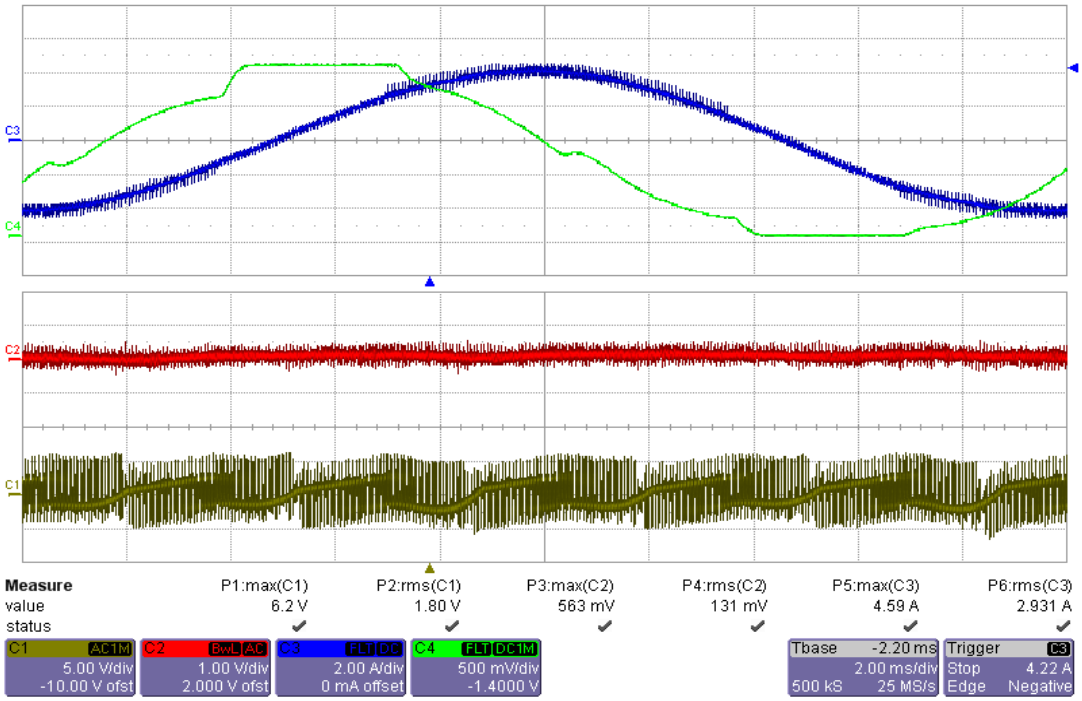


Figure 6.4 Modulation waveform (green, 0.5V/div), output current waveform (blue, 2A/div), dc bus voltage (red, ac coupled, 1V/div) and $I_{hf}$ current (brown, 5A/div), time axis (2ms/div) for DPWM1, $M_i$=0.8, $f_c$=15 kHz

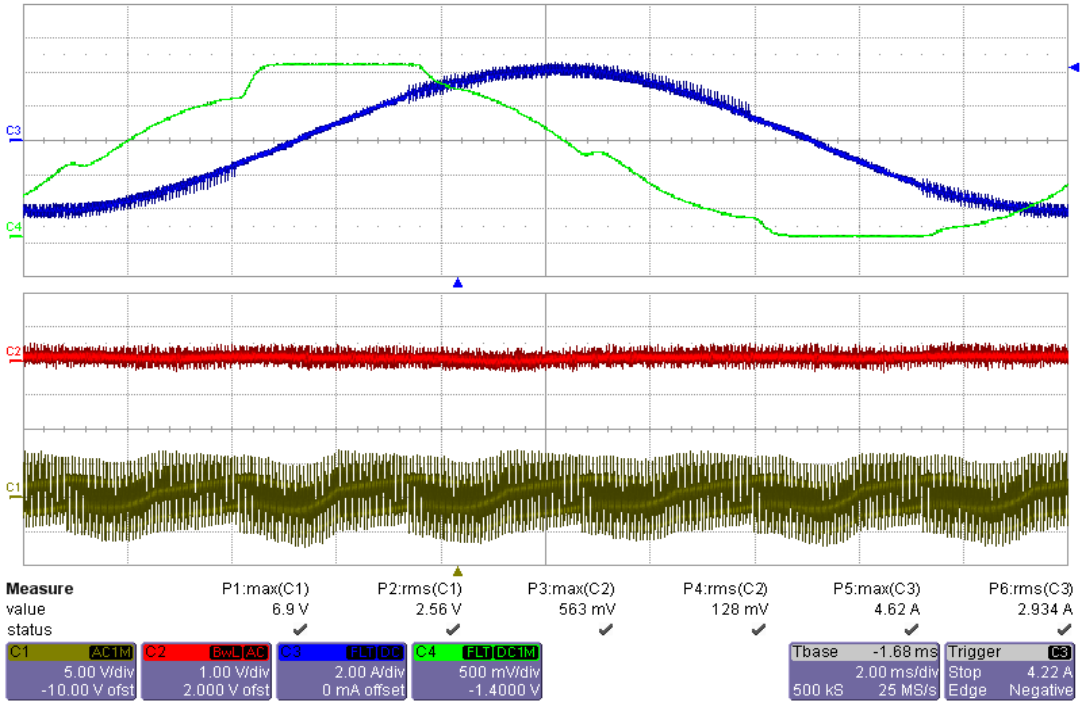


Figure 6.5 Modulation waveform (green, 0.5V/div), output current waveform (blue, 2A/div), dc bus voltage (red, ac coupled, 1V/div) and $I_{hf}$ current (brown, 5A/div), time axis (2ms/div) for NSPWM, $M_i$=0.8, $f_c$=15 kHz

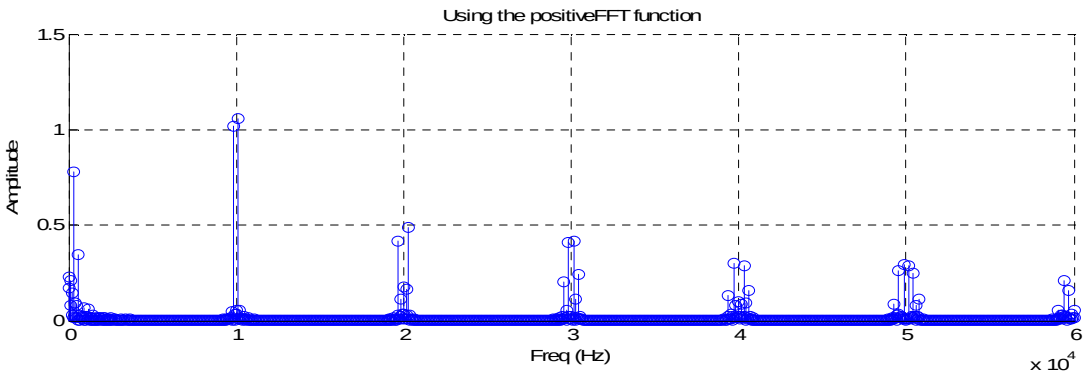


Figure 6.6 $M_i$ = 0.8, SVPWM, dc bus current harmonic fft for $f_c$ = 10 kHz, (0.5A/div, 10kHz/div)

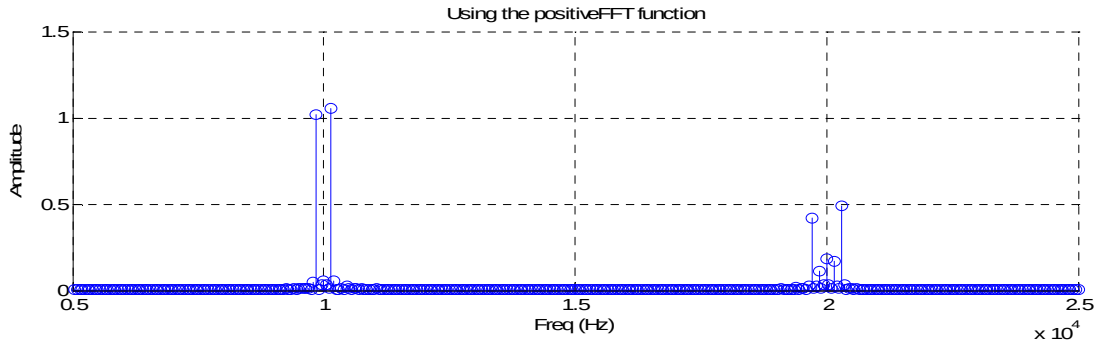


Figure 6.7 $M_i$ = 0.8, SVPWM, dc bus current harmonic fft for $f_c$ = 10 kHz, (0.5A/div, 5kHz/div)

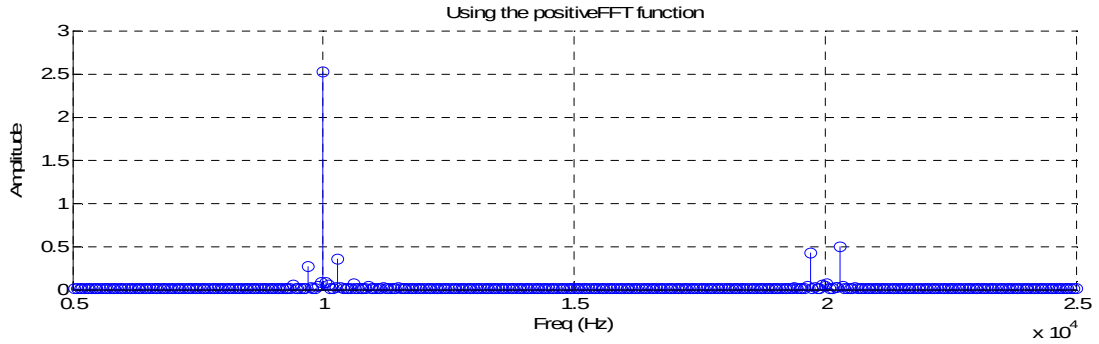


Figure 6.8 $M_i$ = 0.8, AZSPWM1, dc bus current harmonic fft for $f_c$ = 10 kHz, (0.5A/div, 5kHz/div)

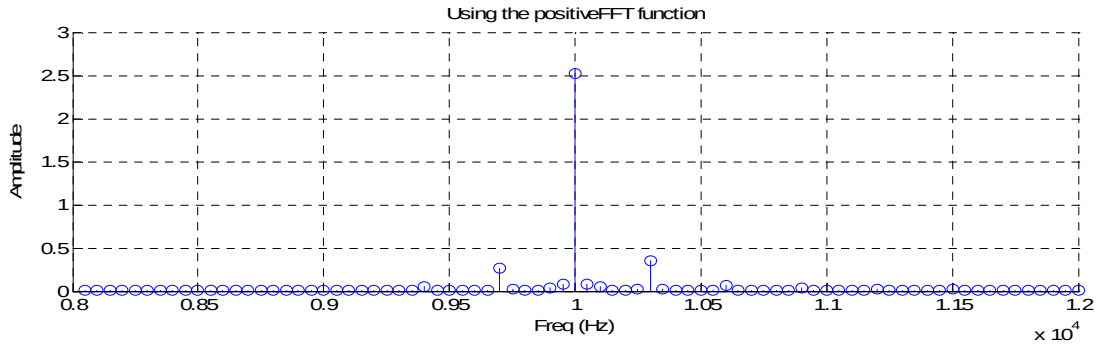


Figure 6.9 $M_i$ = 0.8, AZSPWM1, zoomed dc bus current harmonic fft for $f_c$ = 10 kHz, (0.5A/div, 0.5kHz/div)

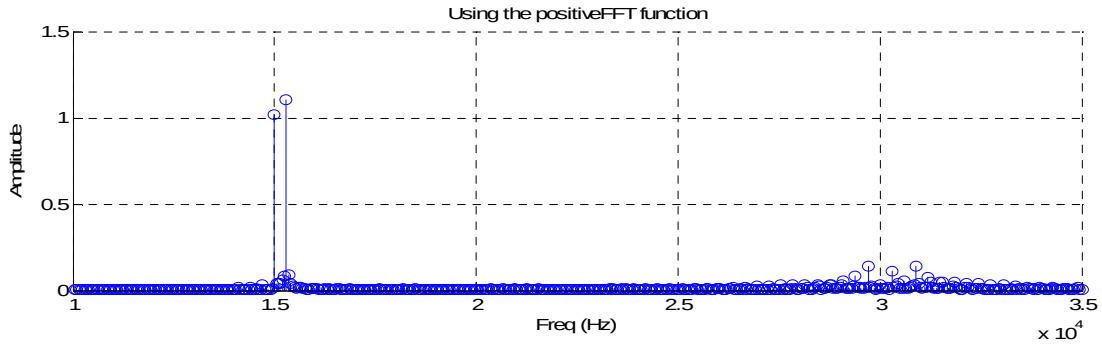


Figure 6.10 $M_i$ = 0.8, DPWM1, dc bus current harmonic fft for $f_c$ = 15 kHz, (0.5A/div, 5kHz/div)

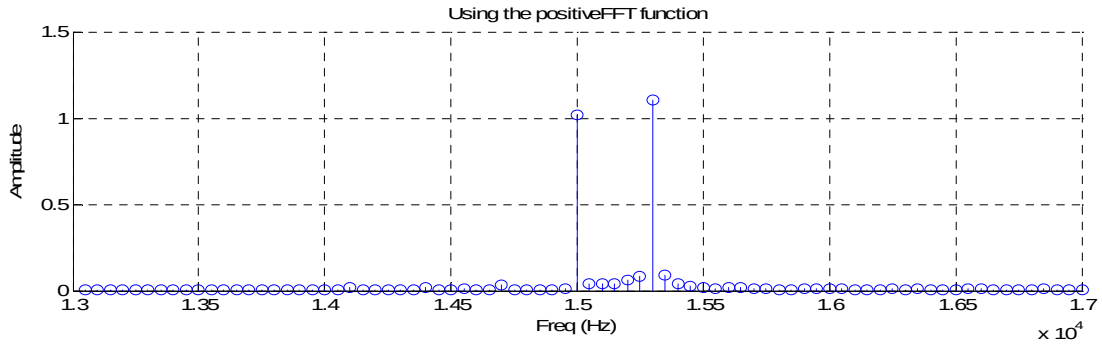


Figure 6.11 $M_i$ = 0.8, DPWM1, zoomed dc bus current harmonic fft for $f_c$ = 15 kHz, (0.5A/div, 0.5kHz/div)

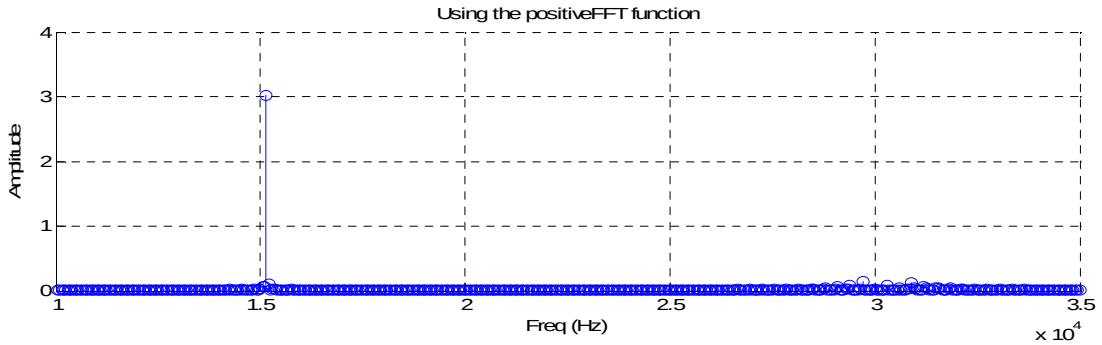


Figure 6.12 $M_i$ = 0.8, NSPWM, dc bus current harmonic fft for $f_c$ = 15 kHz, (1A/div, 5kHz/div)

In the no load motor experiment, motor load is inductive and therefore $\varphi \approx 90°$. At the operating point of $\varphi \approx 90°$ and $M_i$ = 0.8, when the 3D harmonic spectrum plot of Figure 3.14 is examined, it is seen that equivalent harmonic magnitudes of SVPWM and AZSPWM at $2f_c$ are nearly same and matched with the fft data in Figure 6.7 and Figure 6.8 respectively. Moreover, $f_c$ equivalent harmonic of AZSPWM is

double the $f_c$ equivalent harmonic of SVPWM from Figure 3.14, and this is agreed with the fft data. Again for the same operating condition, $f_c$ equivalent harmonic of NSPWM is double the $f_c$ equivalent harmonic of DPWM1 from 3D spectrum and this is matched with the fft data in Figure 6.10 and Figure 6.12. In addition, $2f_c$ equivalent harmonic of DPWM1 is approximately same as the $2f_c$ equivalent of NSPWM as extracted from 3D spectrum and agreed with the fft data.

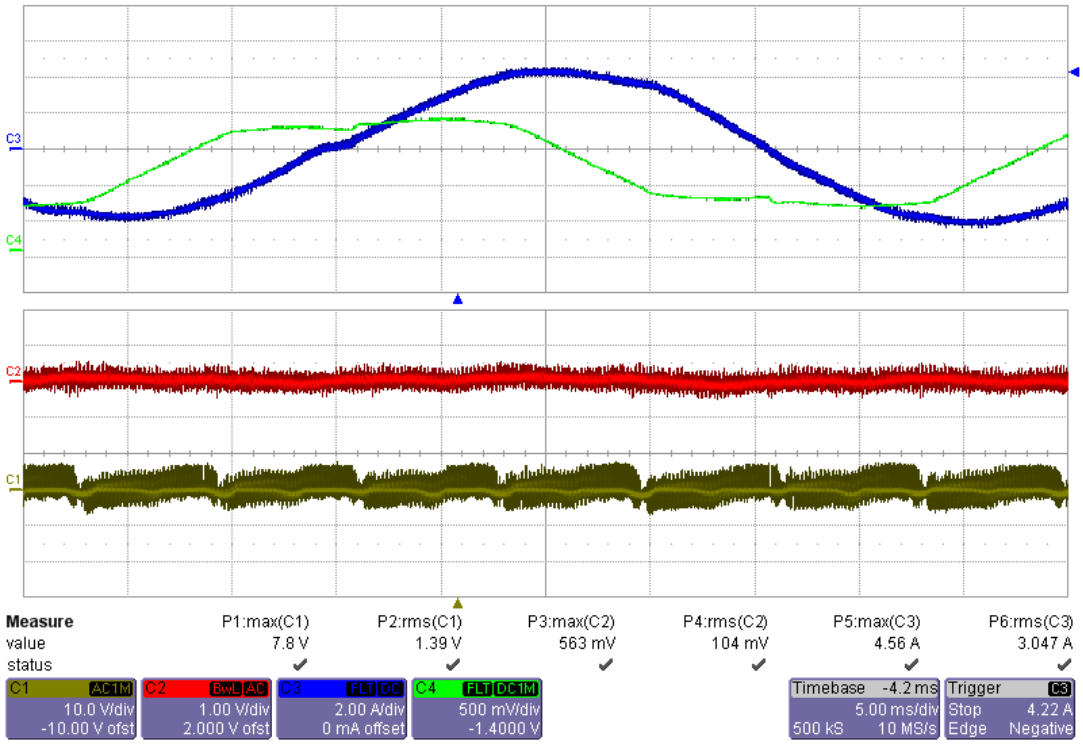


Figure 6.13 Modulation waveform (green, 0.5V/div), output current waveform (blue, 2A/div), dc bus voltage (red, ac coupled, 1V/div) and $I_{hf}$ current (brown, 5A/div), time axis (5ms/div) for SVPWM, $M_i$=0.4, $f_c$=10 kHz

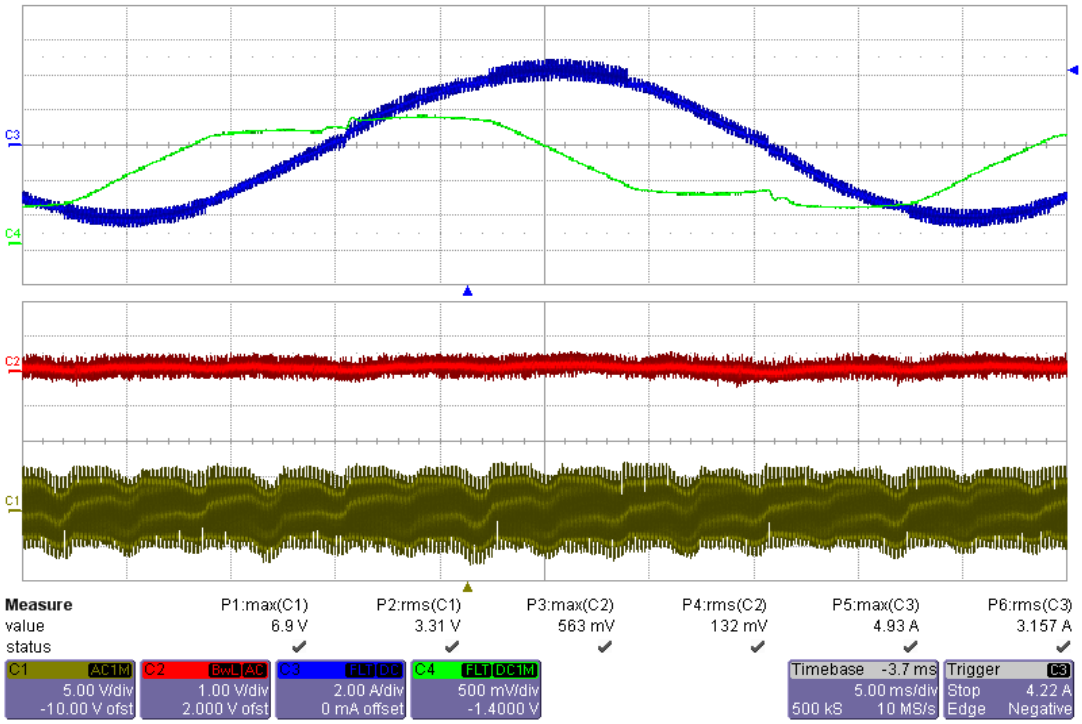


Figure 6.14 Modulation waveform (green, 0.5V/div), output current waveform (blue, 2A/div), dc bus voltage (red, ac coupled, 1V/div) and $I_{hf}$ current (brown, 5A/div), time axis (5ms/div) for AZSPWM1, $M_i$=0.4, $f_c$=10 kHz

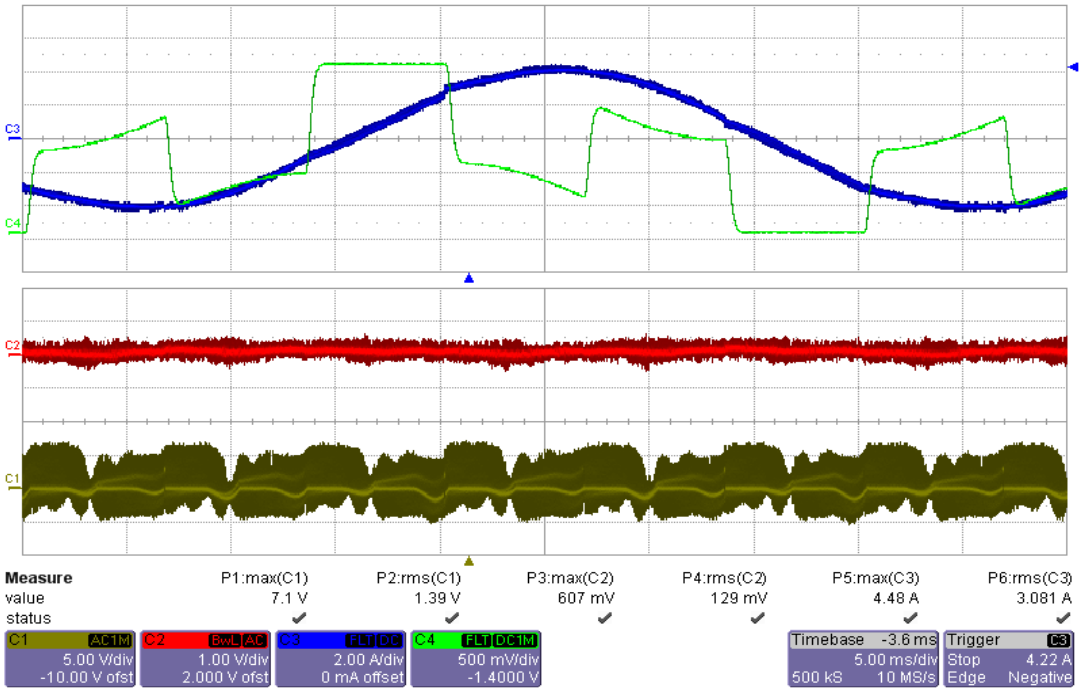


Figure 6.15 Modulation waveform (green, 0.5V/div), output current waveform (blue, 2A/div), dc bus voltage (red, ac coupled, 1V/div) and $I_{hf}$ current (brown, 5A/div), time axis (5ms/div) for DPWM1, $M_i$=0.4, $f_c$=15 kHz

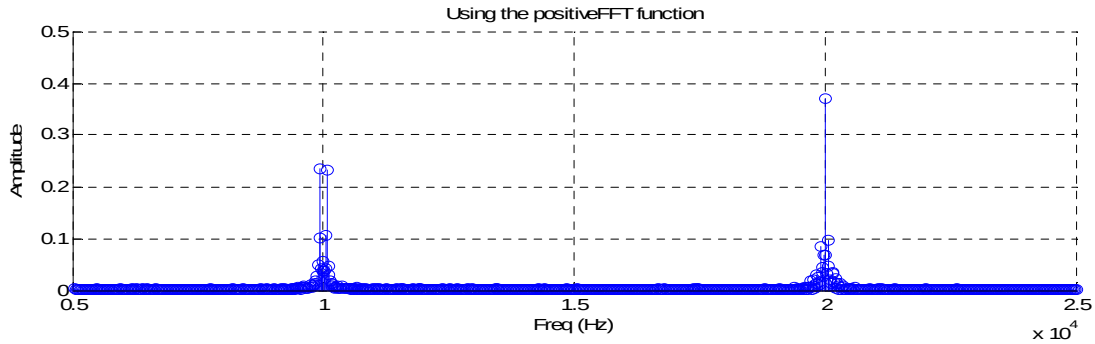


Figure 6.16 $M_i$ = 0.4, SVPWM, dc bus current harmonic fft for $f_c$ = 10 kHz, (0.1A/div, 5kHz/div)

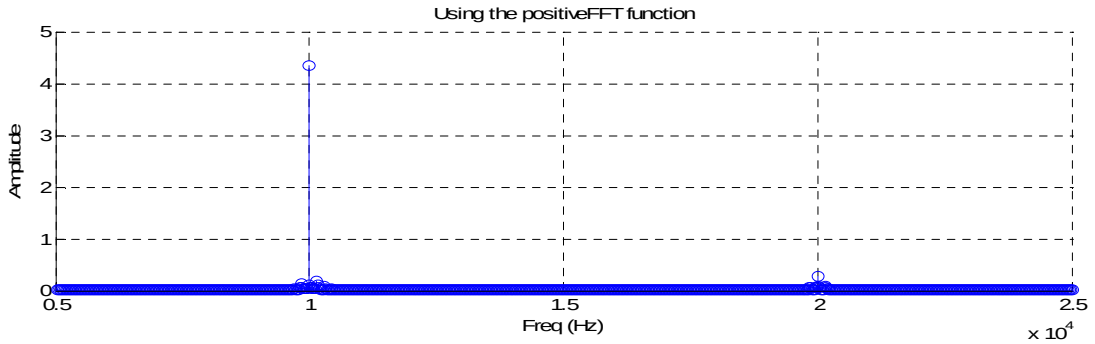


Figure 6.17 $M_i$ = 0.4, AZSPWM1, dc bus current harmonic fft for $f_c$ = 10 kHz, (1A/div, 5kHz)

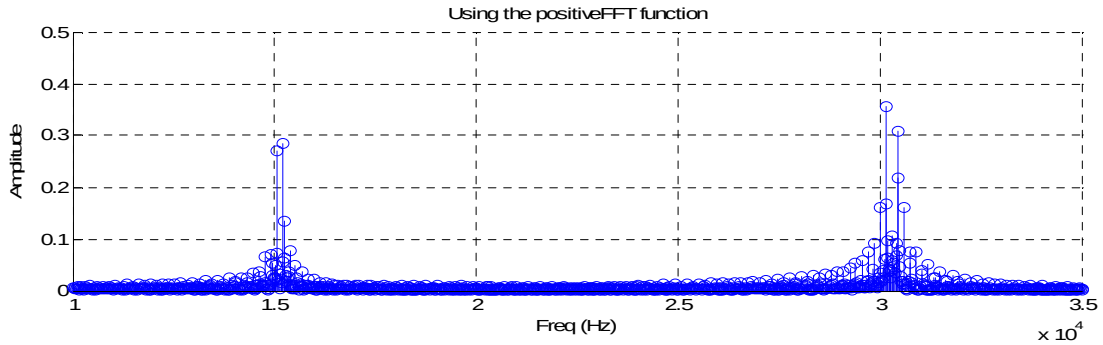


Figure 6.18 $M_i$ = 0.4, DPWM1, dc bus current harmonic fft for $f_c$ = 15 kHz, (0.1A/div, 5kHz/div)

For the operating point of $M_i$ = 0.4 and $\varphi \approx 90°$, the $f_c$ equivalent harmonic of AZSPWM reaches to the peak point of 3D spectrum graph and same harmonic of SVPWM falls to the minimum point and this is also well matched with fft data in Figure 6.16 and Figure 6.17. Moreover, $2f_c$ equivalent harmonics of both SVPWM and AZSPWM should be very low as observed in 3D spectrum and this is checked

with the fft data. In addition, for the same operating condition ($M_i$ = 0.4 and φ ≈ 90°), as inferred from 3D spectrum, all equivalent harmonics of DPWM1 is small in magnitude and the spectrum is flat and this is also agreed with the fft data in Figure 6.18. The low frequency harmonics is sourced from the low frequency fluctuations of three phase diode rectifier that supplies the inverter dc bus.

### 6.3 RL load experiment results

In this experiment, as demonstrated in introduction, 75 Ω per phase star connected R load is interfaced to the inverter output with series connected inductors of 3.1 mH in order to suppress the voltage ripple of the three phase inverter outputs. For the 50 Hz operation, $X_{inductor} = 2\pi fL \approx 0.97\Omega$ and the overall impedance is calculated as $Z = 75 + j0.97$ and this gives a power factor angle of φ = 0.74° ≈ 0°.

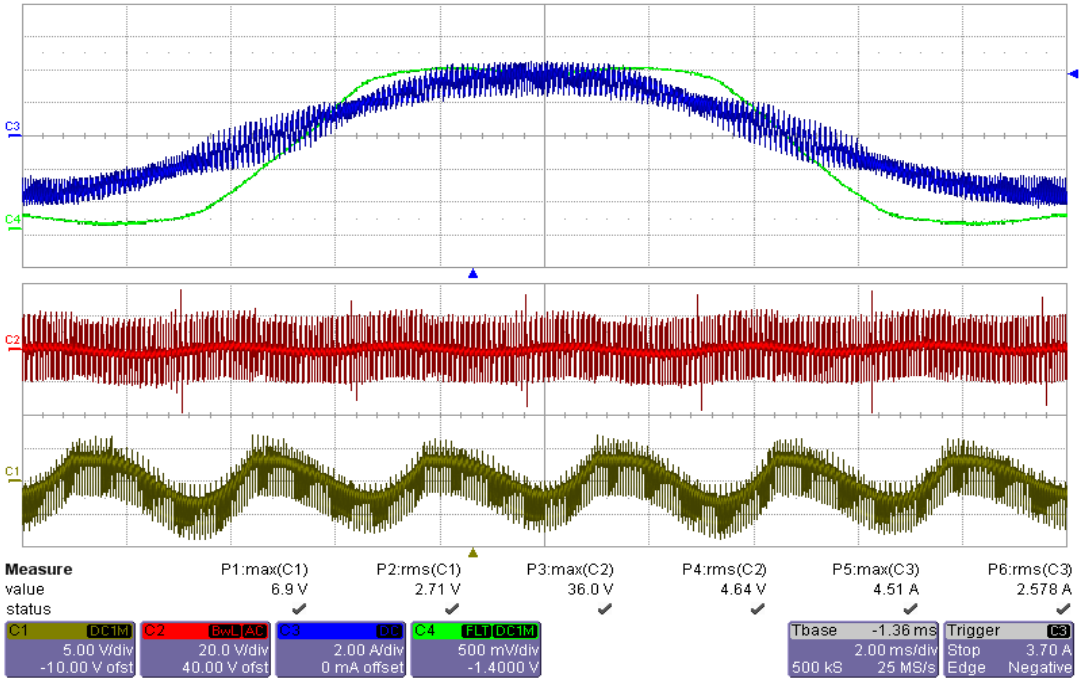


Figure 6.19 Modulation waveform (green, 0.5V/div), output current waveform (blue, 2A/div), dc bus voltage (red, ac coupled, 20V/div) and $I_{hf}$ current (brown, 5A/div), time axis (2ms/div) for SVPWM, $M_i$=0.8, $f_c$=10 kHz

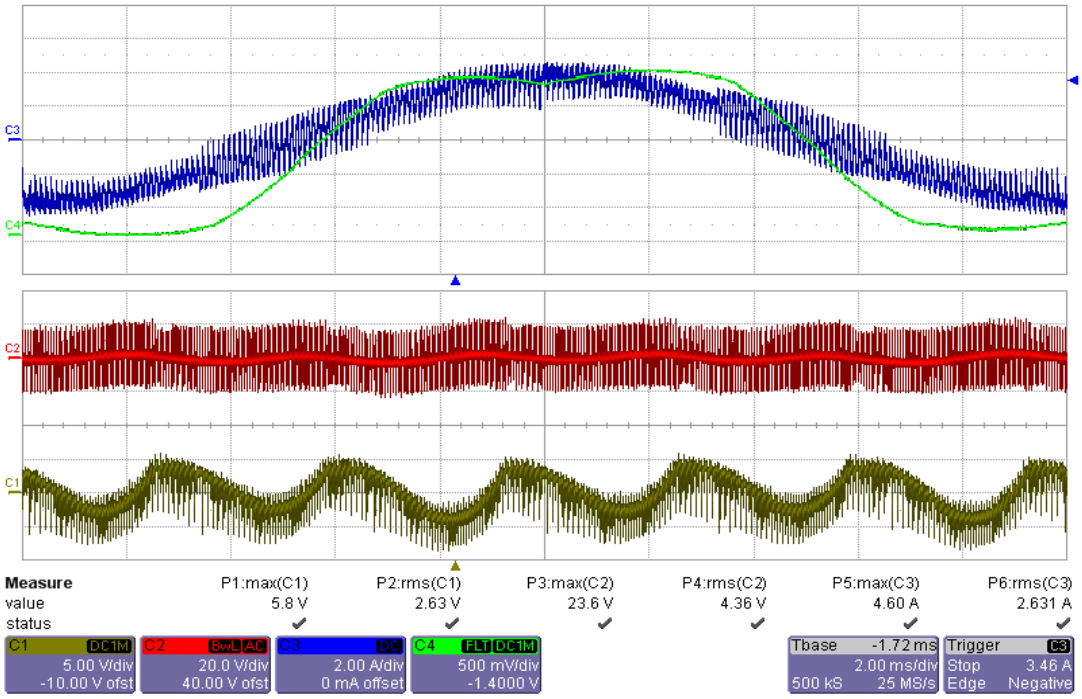


Figure 6.20 Modulation waveform (green, 0.5V/div), output current waveform (blue, 2A/div), dc bus voltage (red, ac coupled, 20V/div) and $I_{hf}$ current (brown, 5A/div), time axis (2ms/div) for AZSPWM1, $M_i$=0.8, $f_c$=10 kHz

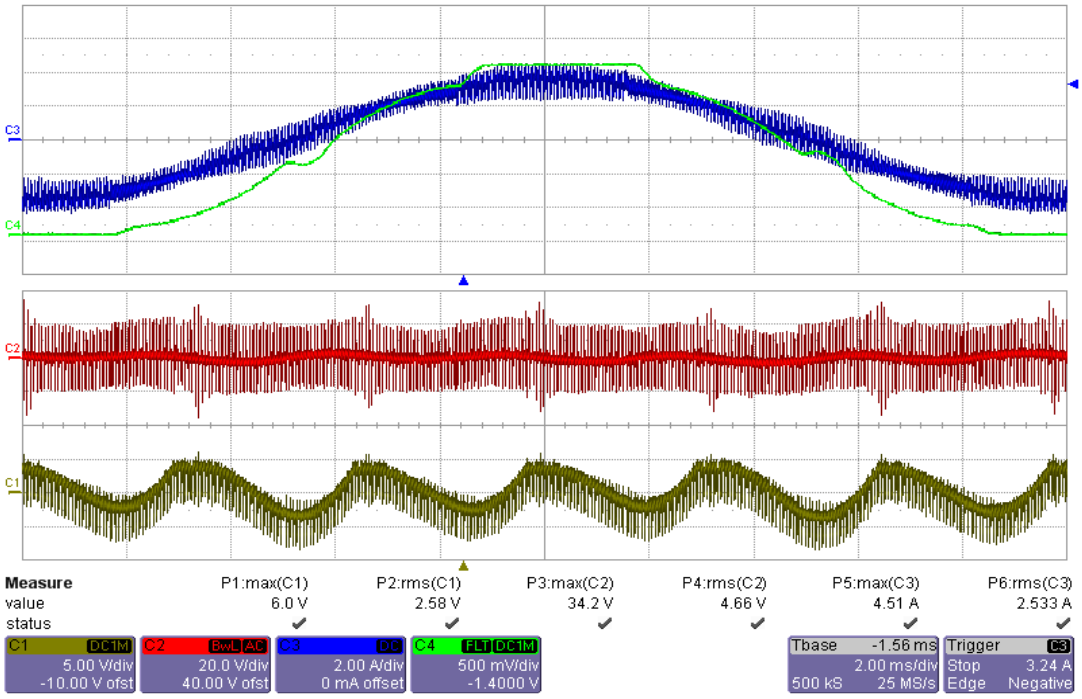


Figure 6.21 Modulation waveform (green, 0.5V/div), output current waveform (blue, 2A/div), dc bus voltage (red, ac coupled, 20V/div) and $I_{hf}$ current (brown, 5A/div), time axis (2ms/div) for DPWM1, $M_i$=0.8, $f_c$=15 kHz

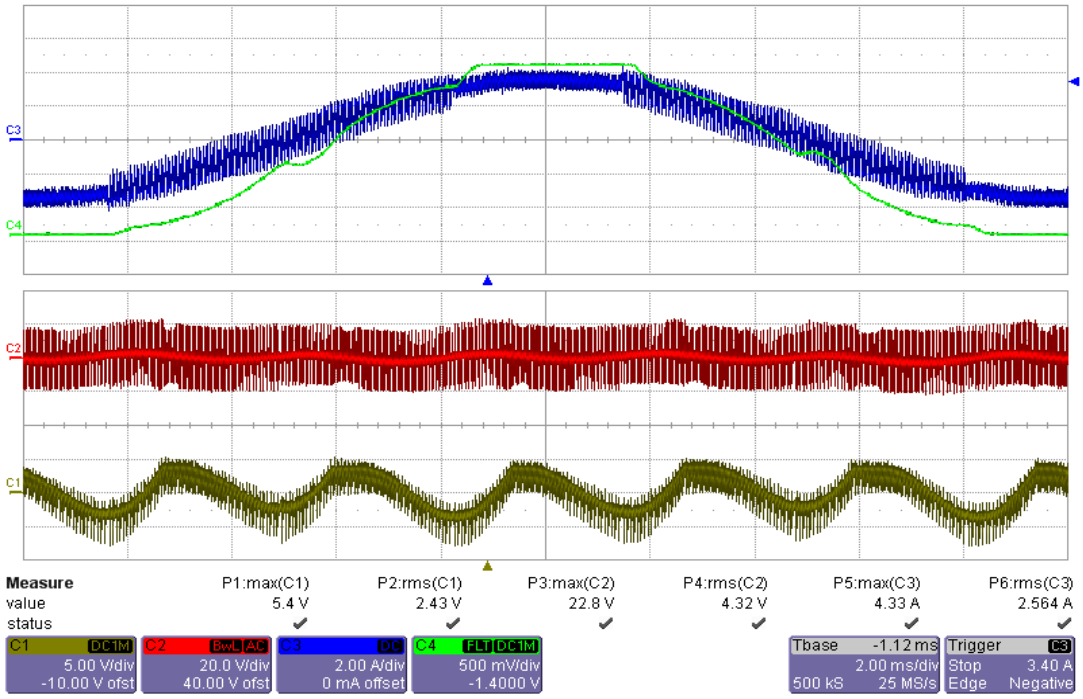


Figure 6.22 Modulation waveform (green, 0.5V/div), output current waveform (blue, 2A/div), dc bus voltage (red, ac coupled, 20V/div) and $I_{hf}$ current (brown, 5A/div), time axis (2ms/div) for NSPWM, $M_i$=0.8, $f_c$=15 kHz

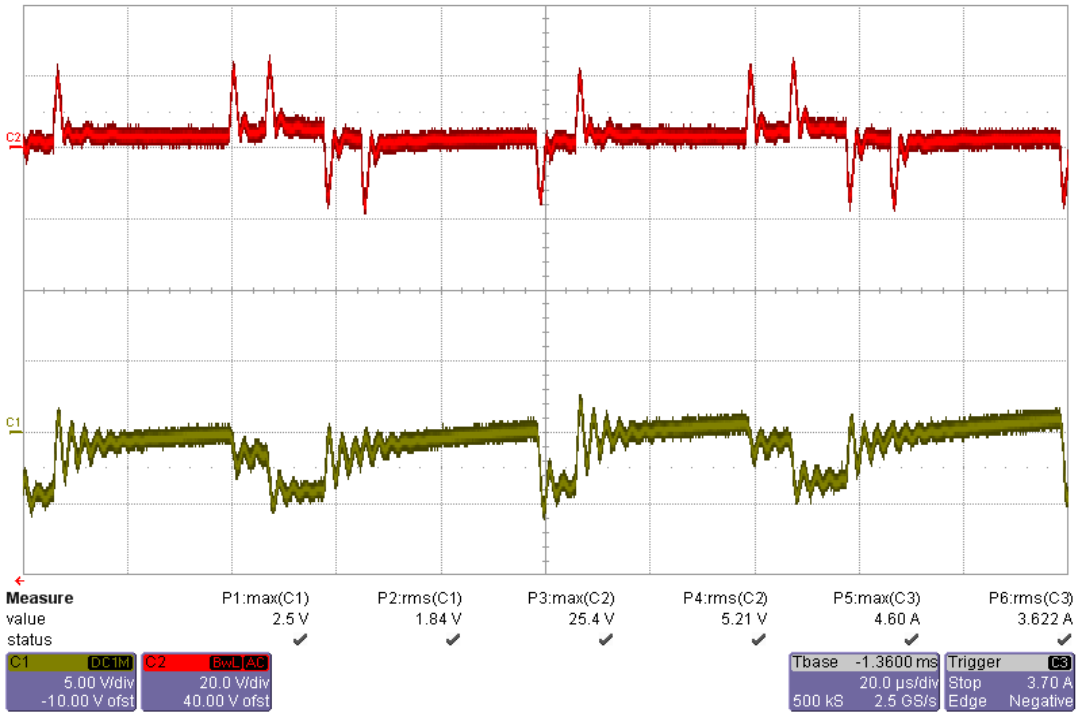


Figure 6.23 Zoomed in $I_{hf}$ current waveform (green, 5A/div), ac coupled $V_{dc}$ waveform (red, 20V/div), time axis (20µs/div) for SVPWM, $M_i$ = 0.8, $f_c$ = 10kHz

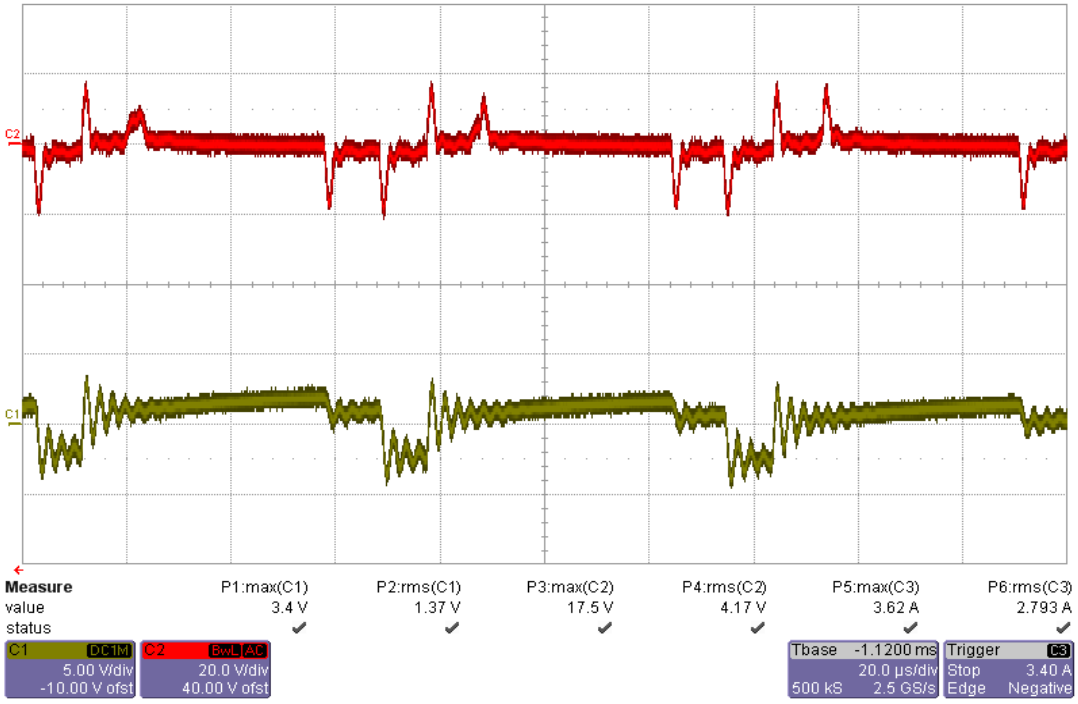


Figure 6.24 Zoomed in $I_{hf}$ current waveform (green, 5A/div), ac coupled $V_{dc}$ waveform (red, 20V/div), time axis (20µs/div) for DPWM1, $M_i = 0.8$, $f_c = 15kHz$

In Figure 6.23, the zoomed in waveform of $I_{hf}$ current of SVPWM is illustrated for the operating point of $M_i = 0.8$, $\varphi \approx 0°$. It is seen from the waveform that two current rectangles in one switching period ($T_{sw}$) are explicit and this makes the $2f_c$ harmonic dominant for the given operating point and modulator. Moreover, for the same operating point, the $I_{hf}$ current of DPWM1 at one $T_{sw}$ includes one explicit rectangle as illustrated in Figure 6.24 and therefore $I_{hf}$ is dominant at $f_c$ as agreed with fft spectrum of Figure 6.27.

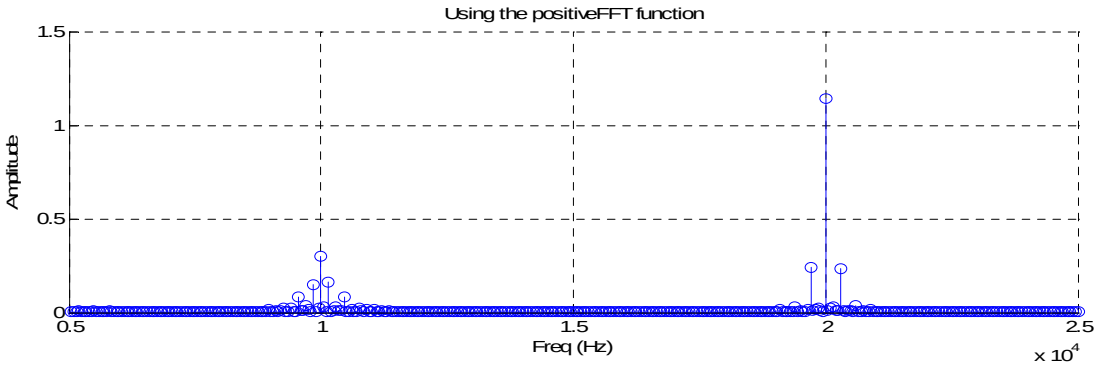


Figure 6.25 $M_i$ = 0.8, SVPWM, dc bus current harmonic fft for $f_c$ = 10 kHz, (0.5A/div, 5kHz)

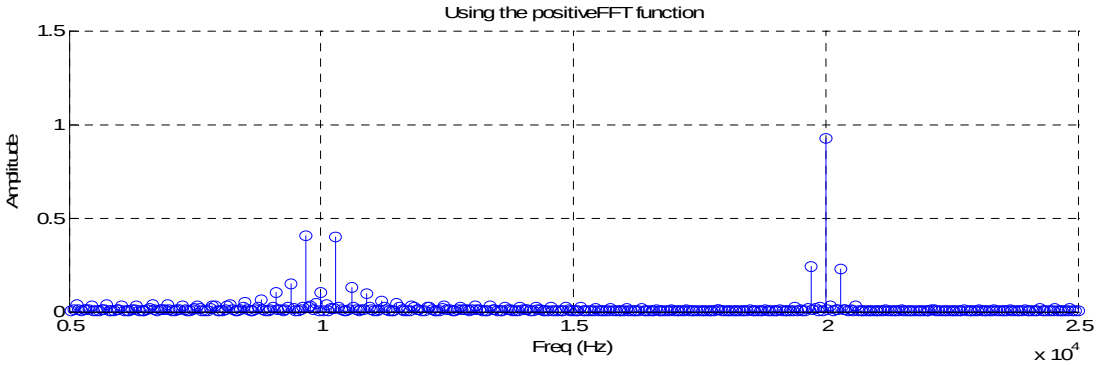


Figure 6.26 $M_i$ = 0.8, AZSPWM1, dc bus current harmonic fft for $f_c$ = 10 kHz, (0.5A/div, 5kHz)

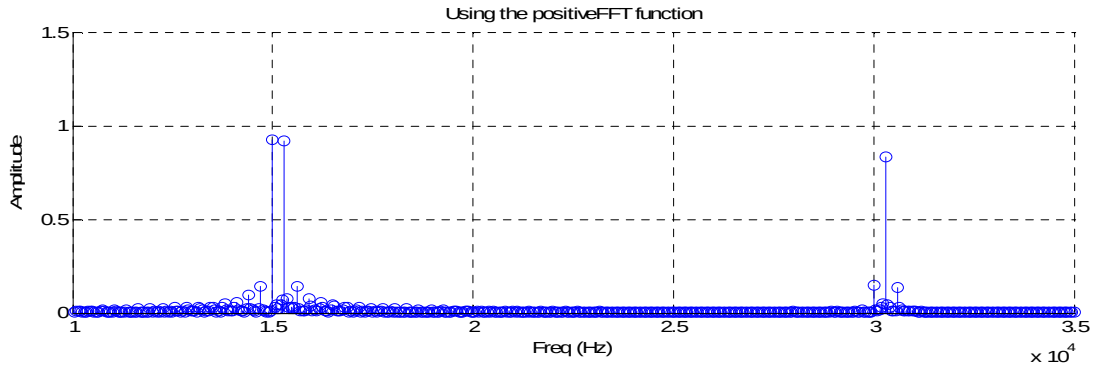


Figure 6.27 $M_i$ = 0.8, DPWM1, dc bus current harmonic fft for $f_c$ = 15 kHz, (0.5A/div, 5kHz)

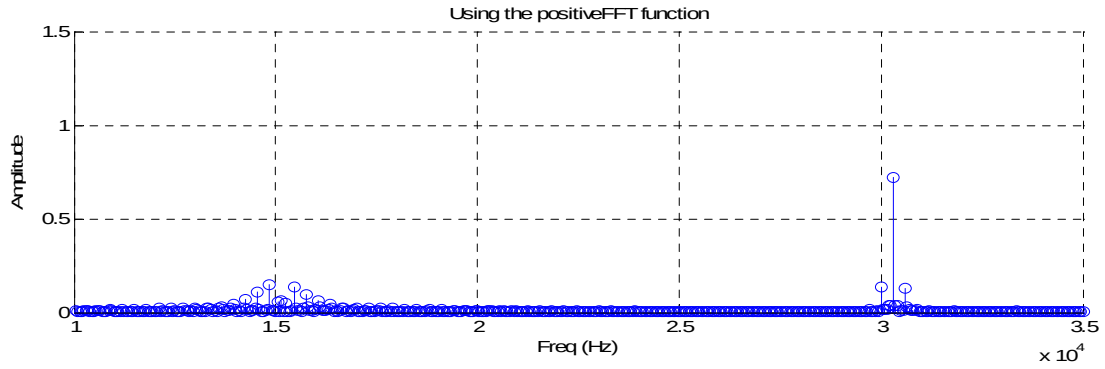


Figure 6.28 $M_i$ = 0.8, NSPWM, dc bus current harmonic fft for $f_c$ = 15 kHz, (0.5A/div, 5kHz)

In this part of experiment, inverter is operated with near unity power factor $\varphi \approx 0°$ and high modulation index of $M_i$ = 0.8. In this operating point, from 3D graph of Figure 3.14, for the SVPWM method, the dominant harmonic is located at $2f_c$, and in the fft data, dominant harmonic is located at $2f_c$ (Figure 6.25) and thus well matched with the analytical result of 3D graph.

For AZSPWM1 switched $I_{dc}$ current fft spectrum, for the same operating point, the dominant harmonic is located at $2f_c$ (Figure 6.26) which is agreed with the 3D graph of Figure 3.14.

The dominant harmonic of DPWM1 should be at $f_c$ and less harmonic component at higher frequencies of spectrum. This condition is agreed with the fft data in Figure 6.27. Moreover, at this operating point, the $2f_c$ equivalent harmonic of NSPWM is dominant and this condition is also correlated with fft data in Figure 6.28. Moreover, from 3D harmonic spectrum graph of Figure 3.14, the $2f_c$ harmonics of DPWM1 and NSPWM are nearly same and this is also agreed with the fft data.

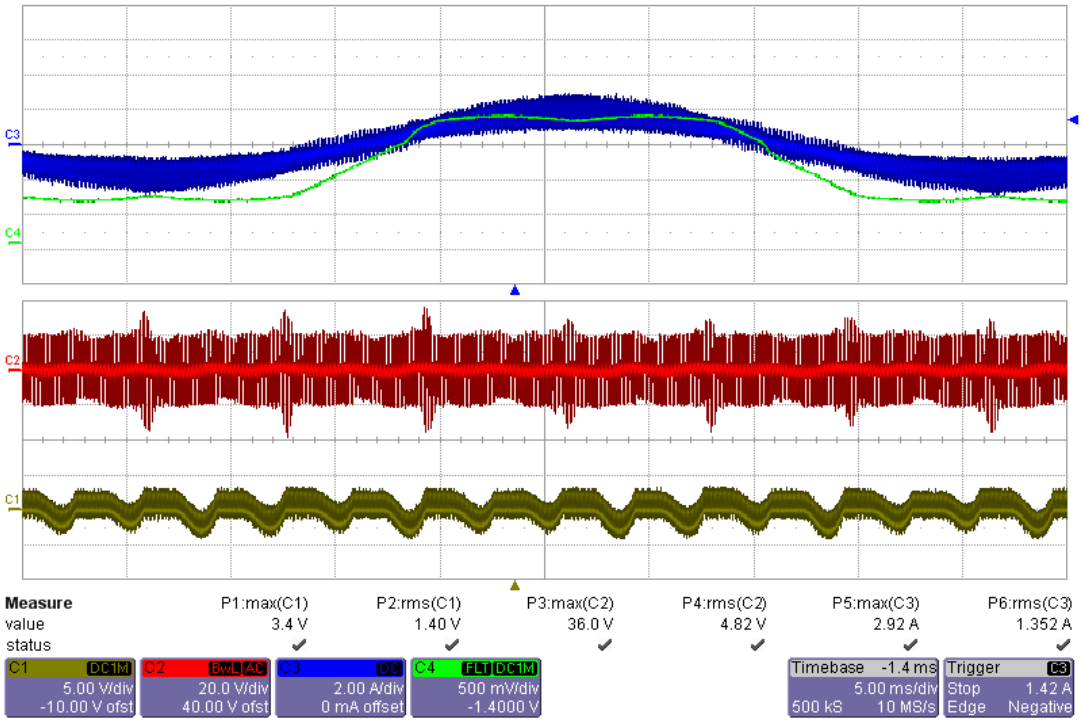


Figure 6.29 Modulation waveform (green, 0.5V/div), output current waveform (blue, 2A/div), dc bus voltage (red, ac coupled, 20V/div) and $I_{hf}$ current (brown, 5A/div), time axis (5ms/div) for SVPWM, $M_i$=0.4, $f_c$=10 kHz

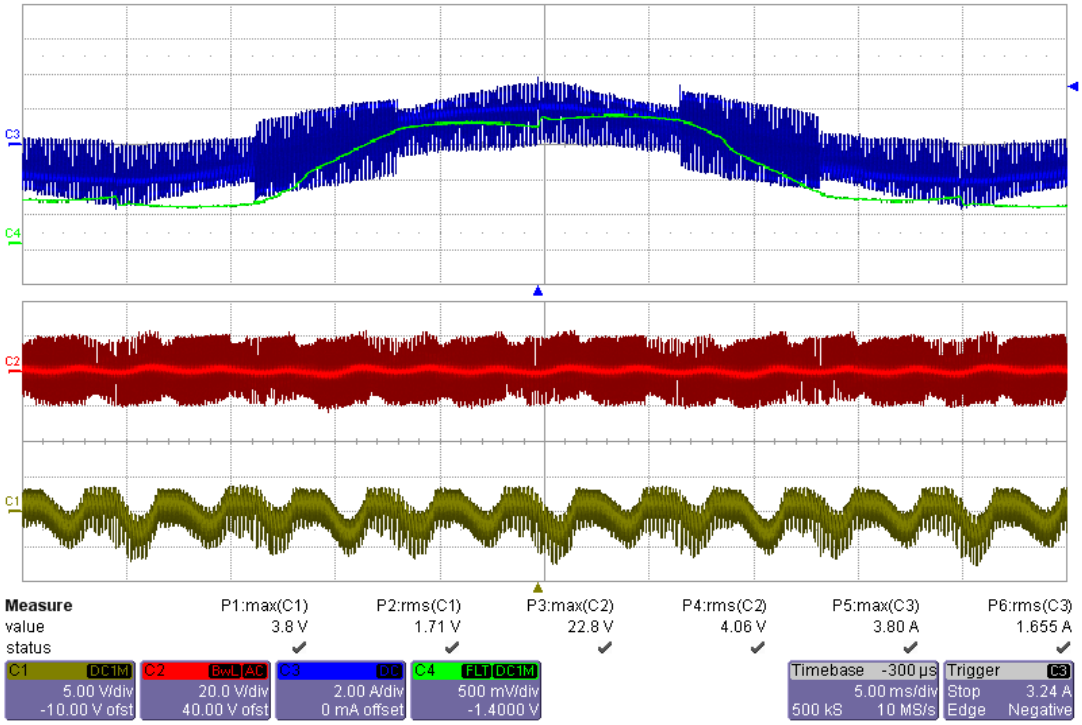


Figure 6.30 Modulation waveform (green, 0.5V/div), output current waveform (blue, 2A/div), dc bus voltage (red, ac coupled, 20V/div) and $I_{hf}$ current (brown, 5A/div), time axis (5ms/div) for AZSPWM1, $M_i$=0.4, $f_c$=10 kHz

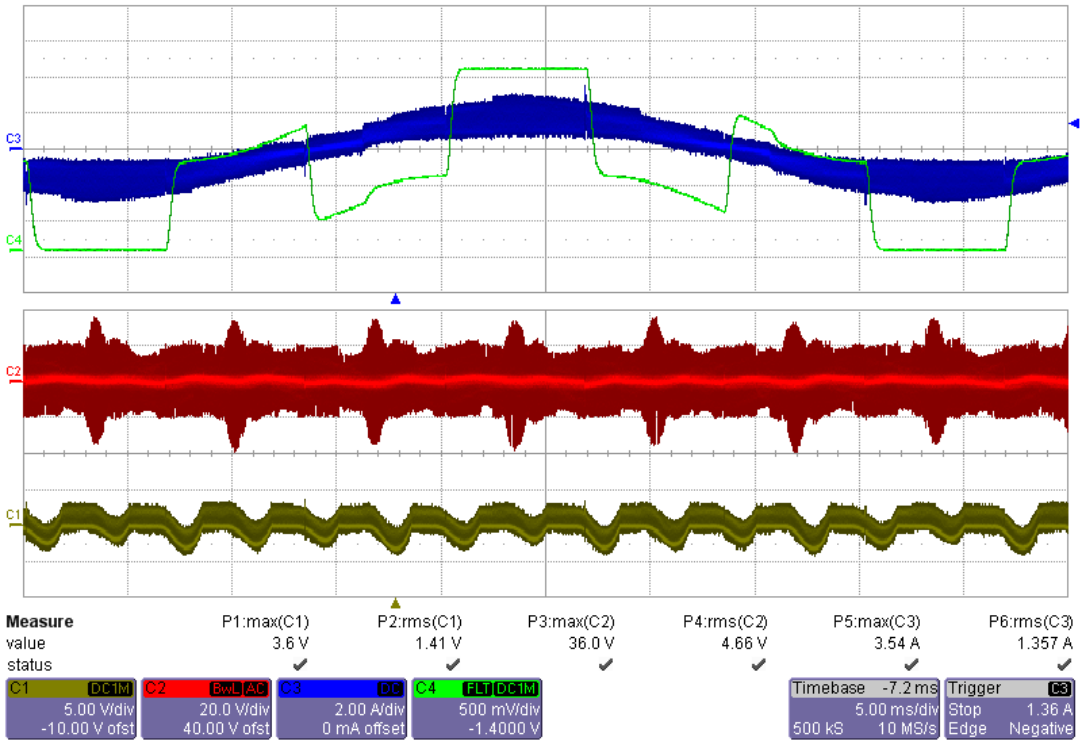


Figure 6.31 Modulation waveform (green, 0.5V/div), output current waveform (blue, 2A/div), dc bus voltage (red, ac coupled, 20V/div) and $I_{hf}$ current (brown, 5A/div), time axis (5ms/div) for DPWM1, $M_i$=0.4, $f_c$=15 kHz

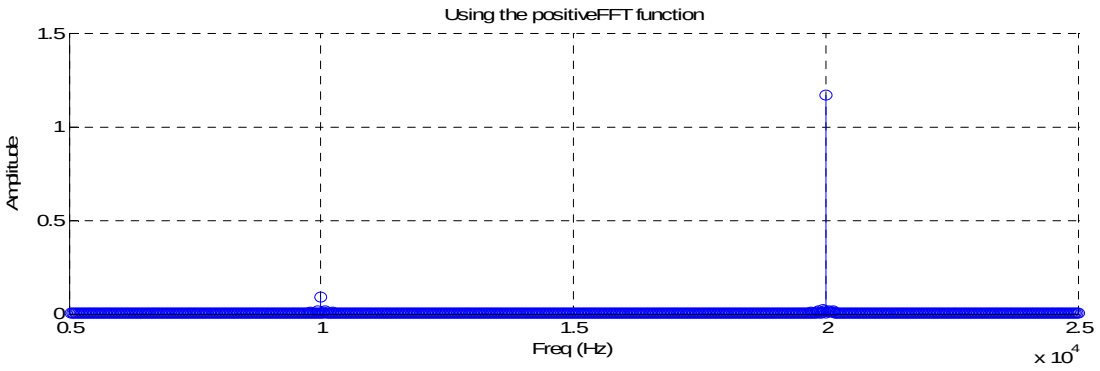


Figure 6.32 $M_i$ = 0.4, SVPWM, dc bus current harmonic fft for $f_c$ = 10 kHz, (0.5A/div, 5kHz)

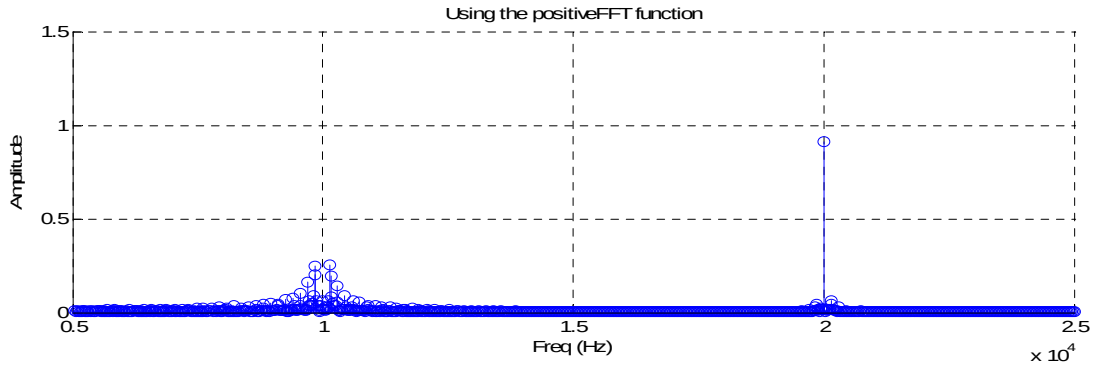


Figure 6.33 $M_i$ = 0.4, AZSPWM1, dc bus current harmonic fft for fc = 10 kHz, (0.5A/div, 5kHz)

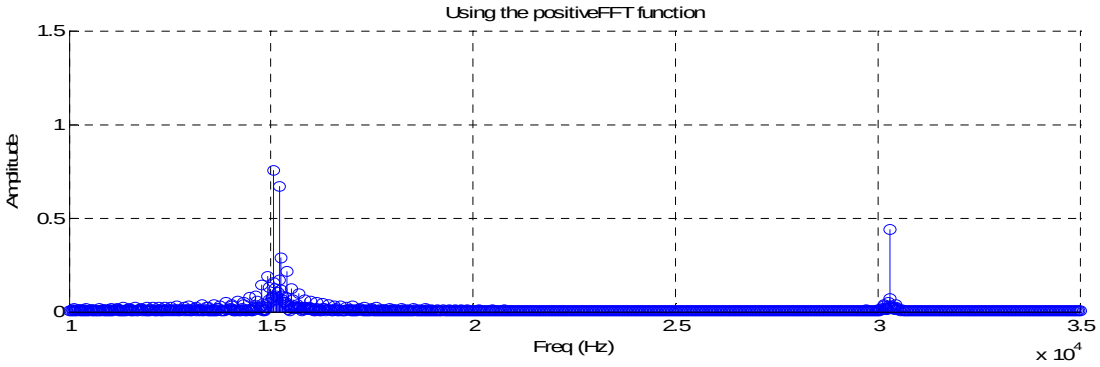


Figure 6.34 $M_i$ = 0.4, DPWM1, dc bus current harmonic fft for fc = 15 kHz, (0.5A/div, 5kHz)

For the operating point of $\varphi \approx 0°$ and low modulation index of $M_i$ = 0.4, the fft spectrums of $I_{hf}$ currents of SVPWM, AZSPWM1 and DPWM are obtained, except for the spectrum of NSPWM, since NSPWM doesn't work linearly under $M_i$ = 0.6 point and thus is not used in this range. The spectrums of SVPWM, AZSPWM and DPWM1 are well correlated with the 3D graph of Figure 3.14.

As demonstrated earlier, low frequency fluctuation on the dc bus current is sourced from the diode rectifier that interfaces with the mains and charges the dc bus capacitor branch. In no load motor experiment, since the drawn real power is very low (the losses of the motor), the magnitude of the low frequency dc bus current fluctuation is low as illustrated in Figure 6.35.

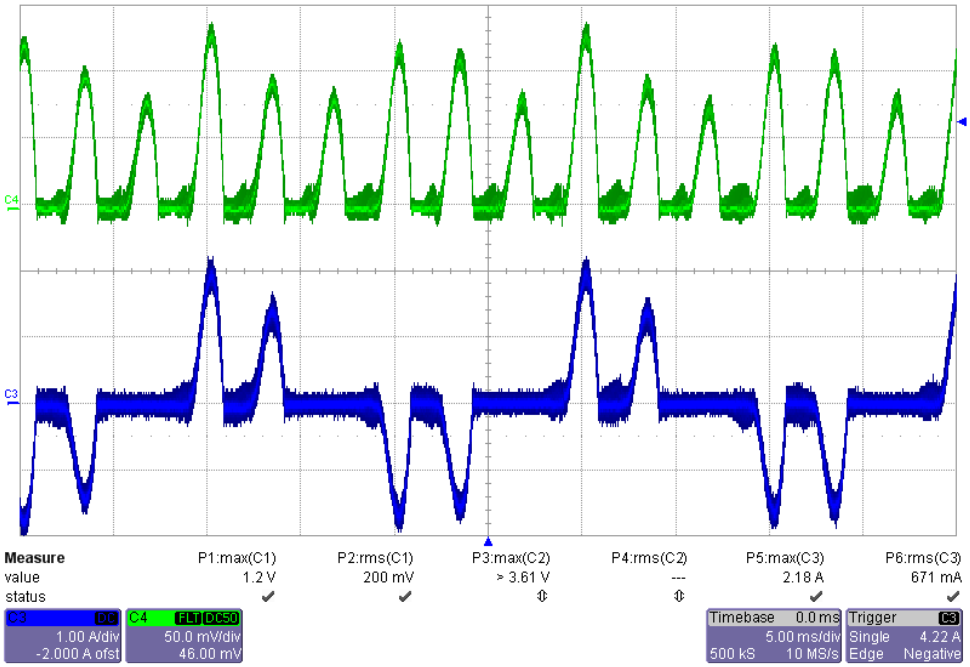


Figure 6.35 No load motor diode rectifier AC input current (blue, 1A/div), DC output current (green, 0.8A/div), (5ms/div), $M_i = 0.8$

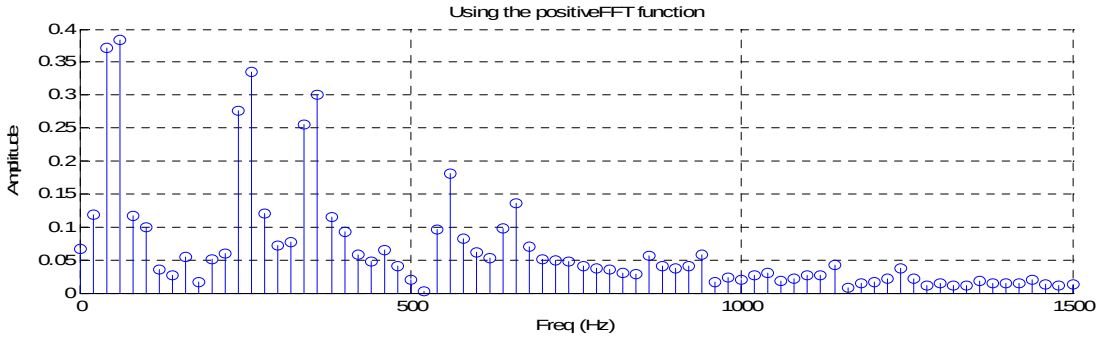


Figure 6.36 No load motor diode rectifier AC input current fft (0.05A/div, 500Hz/div), $M_i = 0.8$

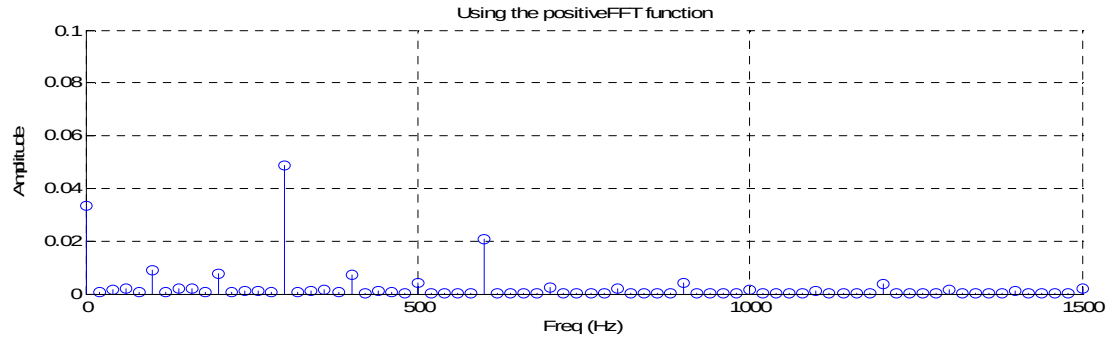


Figure 6.37 No load motor rectifier DC output current fft (0.32A/div, 500Hz/div), $M_i = 0.8$

The spectrums of the rectifier per phase input current and the rectifier dc output current are illustrated in Figure 6.36 and Figure 6.37 for the no load motor experiment with $M_i = 0.8$.

In the RL load experiment, since much power is dissipated in the resistive load bank, much current is drawn from dc bus and hence from the rectifier output and the inputs. The input per phase current and the dc output current of the diode bridge rectifier is illustrated in Figure 6.38, for the operating point of $M_i = 0.8$. Moreover, the fft spectrum of these waveforms are obtained in Figure 6.39 and Figure 6.40. In Figure 6.40, the typical harmonic distribution located at even integer multiples of third harmonic (150Hz) of the fundamental frequency (50Hz) is observed.

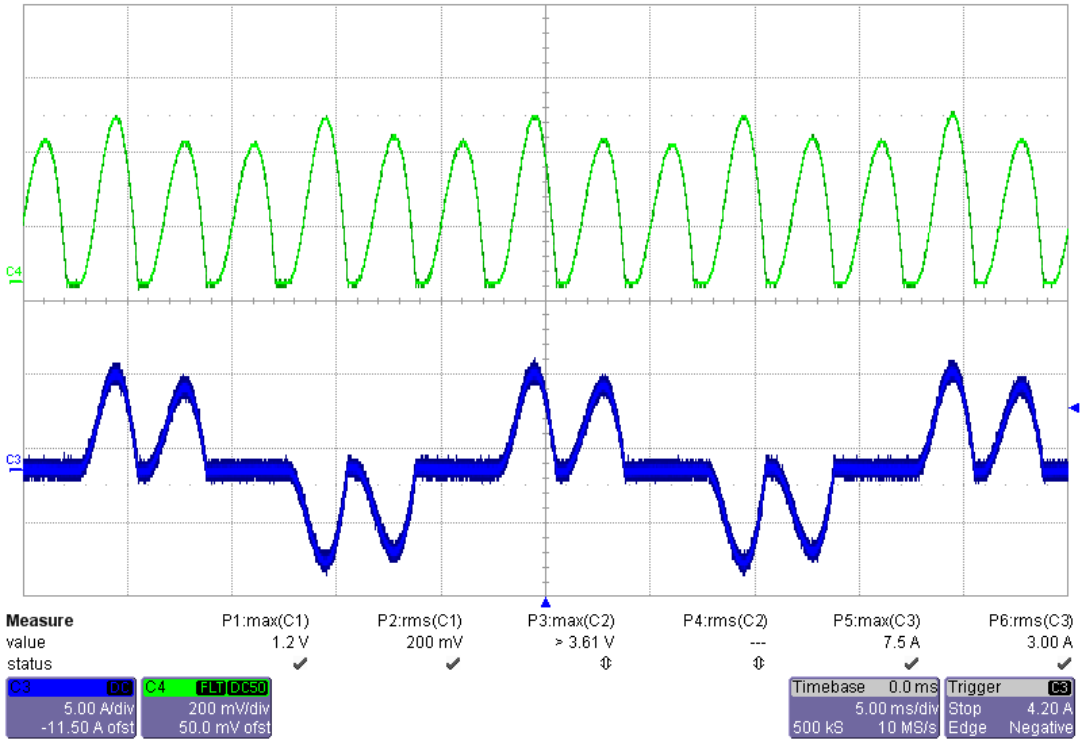


Figure 6.38 RL load diode rectifier AC input current (blue, 5A/div), DC output current (green, 3.2A/div), (5ms/div), $M_i = 0.8$

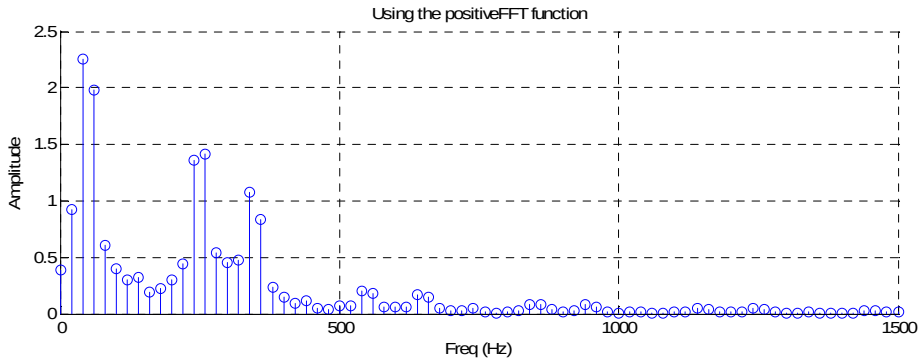


Figure 6.39 RL load rectifier AC input current fft (0.5A/div, 500Hz/div), $M_i = 0.8$

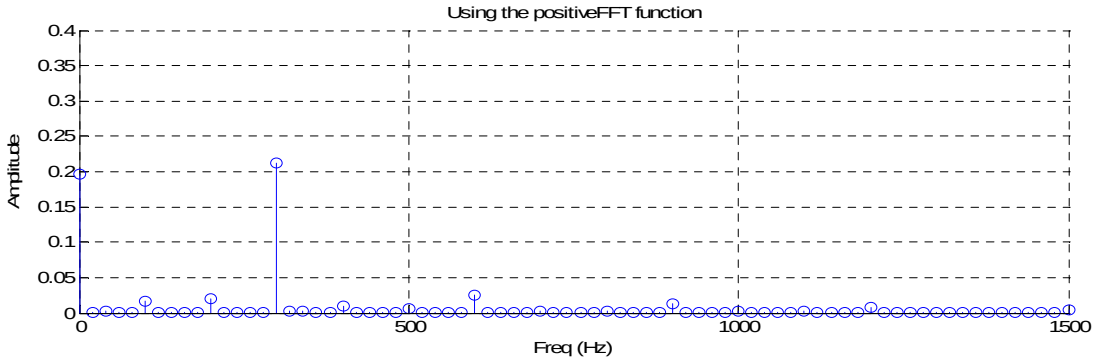


Figure 6.40 RL load rectifier DC output current fft (0.8A/div, 500Hz/div), $M_i = 0.8$

In summary, in chapter 6, the experimental data which is collected via using the experimental setup that drives available loads in the laboratory is investigated and it is demonstrated that the fft of the experimental data is well matched with the analytical harmonic spectrum calculation results. Moreover, ac input and dc output current waveforms of the three phase diode rectifier of the experimental setup are investigated and typical spectrums are observed.

In the next chapter, a brief information about the 3L PWM VSI will be given and the expansion of the 2L double fourier analysis to the 3L will be demonstrated.

# CHAPTER 7

## BASIC INVESTIGATION OF THREE PHASE THREE LEVEL PWM VSI

In this chapter, dc bus harmonic current analysis of Three Level Voltage Source Inverter is demonstrated with additional low frequency harmonic analysis. In the following pages, The brief information about the Three Level PWM VSI is given and some simulation works are illustrated and a modification of previously used harmonic spectrum analysis method for 2L PWM VSI is mentioned to be applied for multi level PWM VSI topologies.

3L (three level) 3-Phase PWM inverter outputs one of three different voltage levels per phase output at a switching time ($T_s$). This VSI topology gets its name '3L' from these three kind of voltage levels. These voltage levels are $V_{dc}$ / 2, -$V_{dc}$ / 2, and 0 volts. Last voltage level is performed via using clamp diodes which are labeled as (DU1, DU2, DV1, DV2, DW1, DW2) in Figure 7.1. In order to prevent the short of dc bus during clamping action, active switches are used to isolate the dc bus rails from neutral rail (the middle rail in Figure 7.1). These active switches are labeled as (SU1, SV1, SW1, SU4, SV4, SW4) in Figure 7.1.

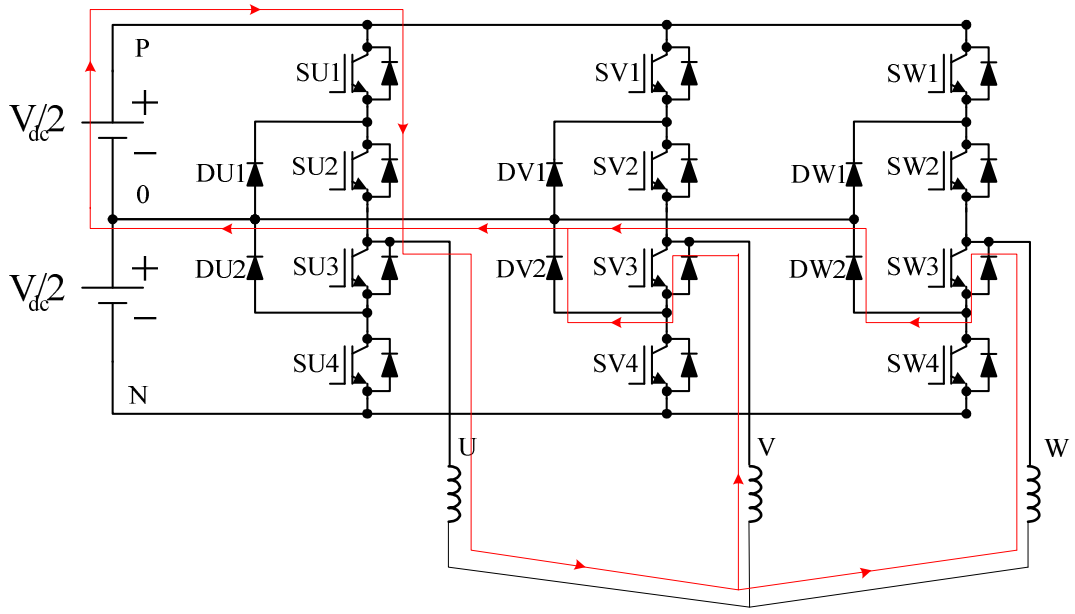


Figure 7.1 3L inverter topology and current circulation path in a switching state

At positive half cycle of modulation waveform, output of 3L inverter leg switches between $V_{dc}$ / 2 and 0 volts voltage levels. Assuming the unity power factor operation, that means output current is also positive, the current path during the on state (inverter leg output is pulled up to $V_{dc}$ / 2) is shown in Figure 7.1. In this switching state, V and W phase legs outputs are clamped to 0 volts level and current loop is closed via clamp diodes.

At negative half cycle of modulation waveform and assuming unity power factor operation, the current path during the on state (inverter leg output is pulled up to -$V_{dc}$ / 2) is symmetric to previous path with respect to neutral wire (middle rail). This current path is shown in Figure 7.2. In this switching state, U phase leg output is pulled down to –$V_{dc}$ / 2 level and V, W phase leg outputs are clamped to 0 volts via upper clamp diodes (DV1, DW1).

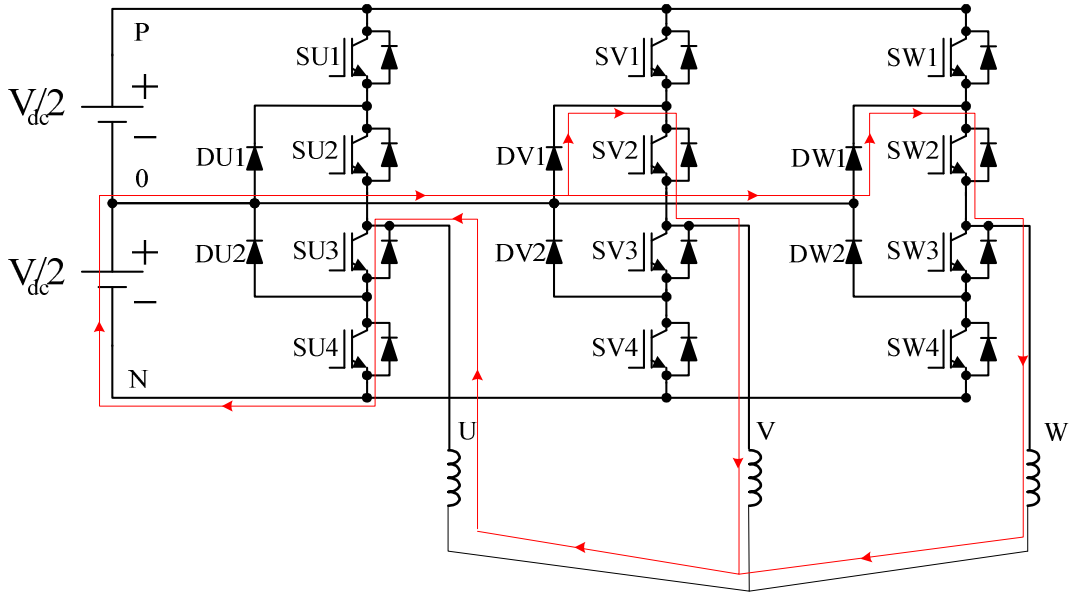


Figure 7.2 3L inverter topology and current circulation path in a switching state

Switching between $V_{dc}$ / 2 and 0 volts voltage levels helps decreasing the switching loss of semiconductor switches compared with the $V_{dc}$ and 0 volts switching levels of 2 level inverters.

Following waveforms and spectrums are the outputs of 3L PWM VSI simulation with following simulation parameters shown in Table 7.1. The output loads of the inverter are three phase balanced sinusoidal current sources.

Table 7.1 3L PWM VSI simulation parameters

| Modulation | $M_i$ | Φ (°) | $I_{o\_max}$ (A) | $V_{dc}$/2 (V) | $f_c$ (Hz) |
|---|---|---|---|---|---|
| SVPWM | 0.7 | 0 | 100 | 400 | 10000 |

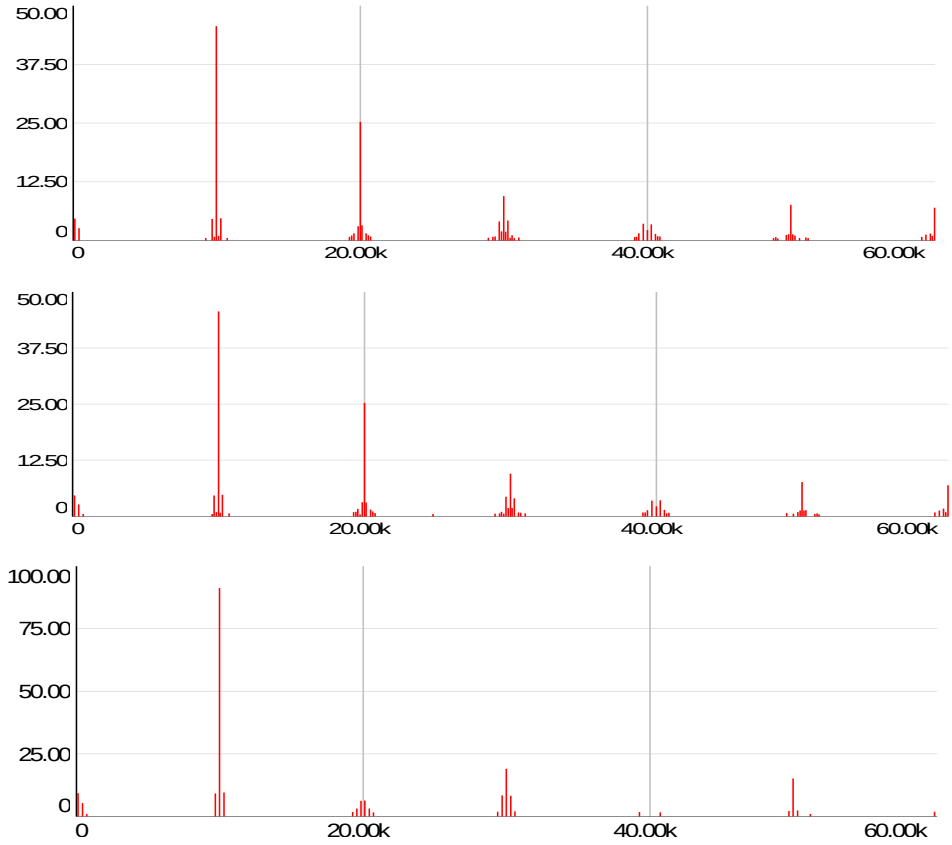


Figure 7.3 From top to bottom: $I_{dc\_P}$ ($V_{dc}/2$ rail current) harmonic spectrum (12.5A/div, 20kHz/div), $I_{dc\_N}$ ($-V_{dc}/2$ rail current) harmonic spectrum (12.5A/div, 20kHz/div), and the $I_{dc\_O}$ (neutral wire current) harmonic spectrum (25A/div, 20kHz/div)

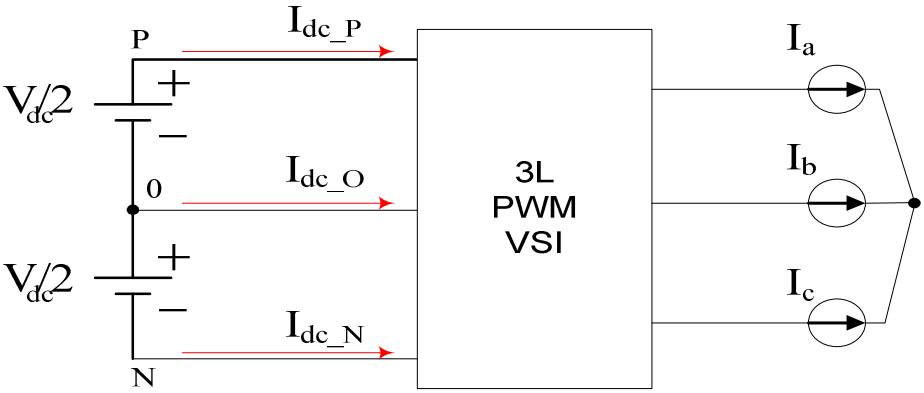


Figure 7.4 Dc bus current notations for 3L PWM VSI

As illustrated in Figure 7.3, $I_{dc\_P}$ and $I_{dc\_N}$ currents harmonics are same in magnitude ( $|I_{dc\_P}| = |I_{dc\_N}|$ ) as a result of symmetrical switching of $V_{dc} / 2$ and $– V_{dc} / 2$ rails.

Moreover, as a special working condition of unity power factor operation ($\Phi = 0^o$), they are same in magnitude in odd integer multiples of $f_c$, however, they are 180º out of phase at even integer multiple of $f_c$. From the node equation at node 0, $I_{dc\_O} = -(I_{dc\_P} + I_{dc\_N})$ and therefore $|I_{dc\_O}| = 2 \cdot |I_{dc\_P}|$ at odd integer multiple of $f_c$ and $I_{dc\_O} = 0$ at even integer multiple of $f_c$. Moreover, there occures low frequency current harmonics at 150 Hz and 450 Hz different from 2L PWM VSI.

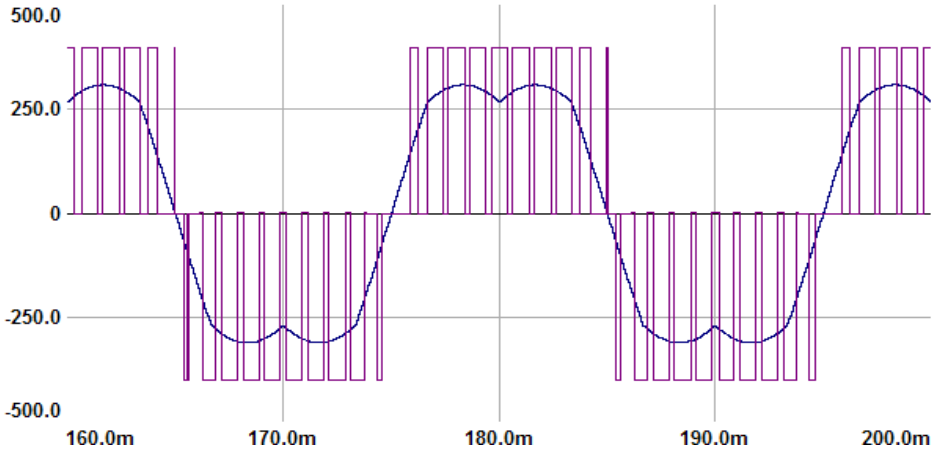


Figure 7.5 Inverter A phase output and the modulation waveform

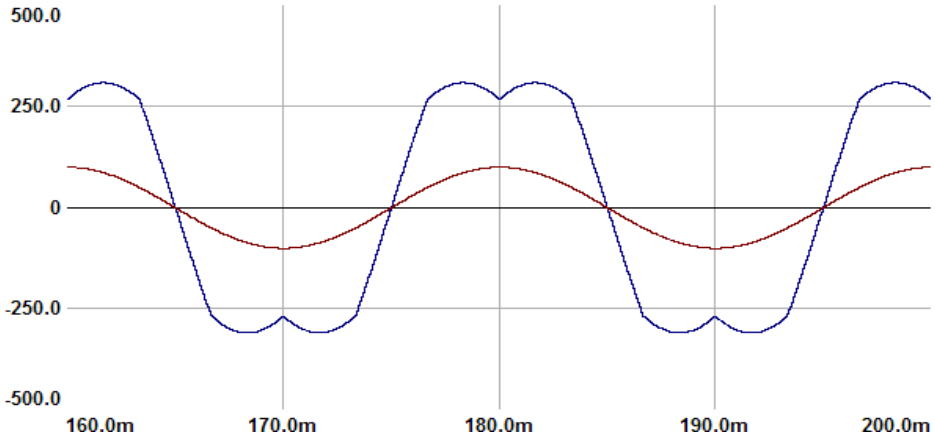


Figure 7.6 A phase output current waveform and the modulation waveform in phase

In the following graphs (Figure 7.7 – Figure 7.13), the harmonic spectrums of $I_{dc\_P}$ current of 3L inverter under each modulation technique are compared depending on different operating conditions.

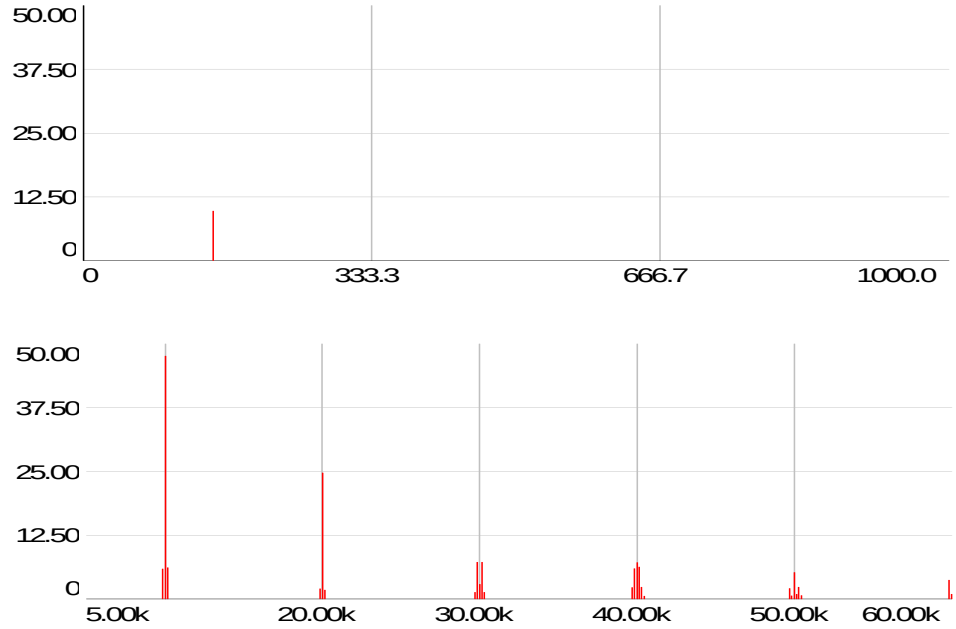


Figure 7.7 SPWM ripple current spectrum, low frequency harmonics (top, 12.5A/div, 333Hz/div), high frequency harmonics (bottom, 12.5A/div, 10kHz/div), ($M_i$=0,3, φ = 0°, $I_{om}$=100 A)

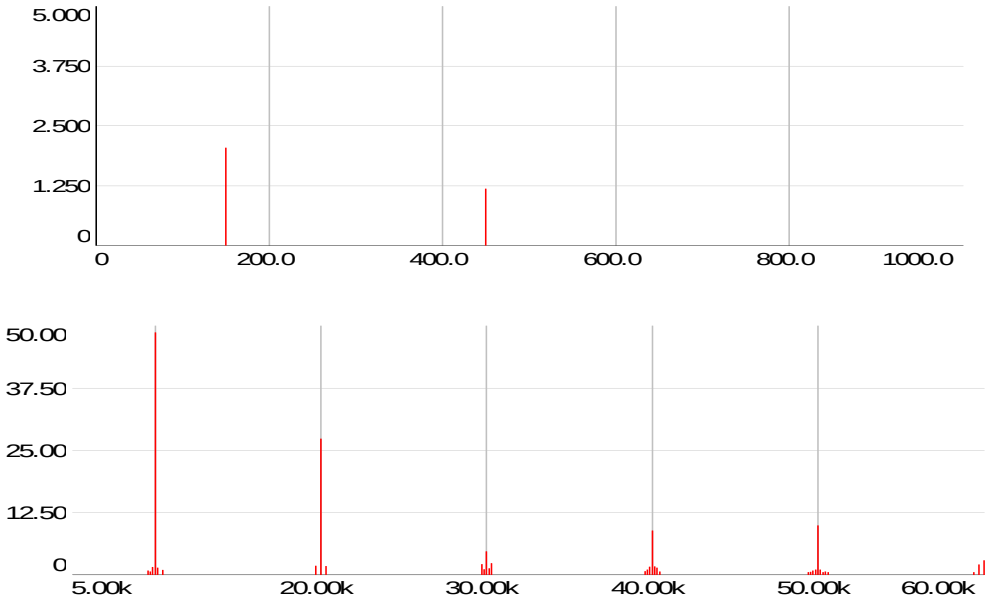


Figure 7.8 SVPWM ripple current spectrum, low frequency harmonics (top, 1.25A/div, 200Hz/div), high frequency harmonics (bottom, 12.5A/div, 10kHz/div), ($M_i$=0,3, φ = 0°, $I_{om}$=100 A)

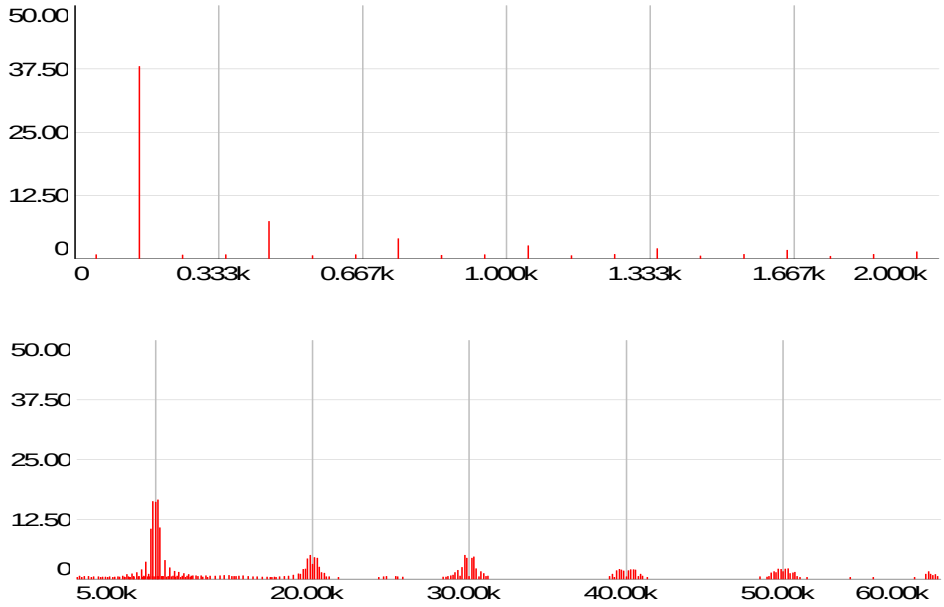


Figure 7.9 AZSPWM1 ripple current spectrum, low frequency harmonics (top, 12.5A/div, 333Hz/div), high frequency harmonics (bottom, 12.5A/div, 10kHz/div), ($M_i$=0,3, φ = 0°, $I_{om}$=100 A)

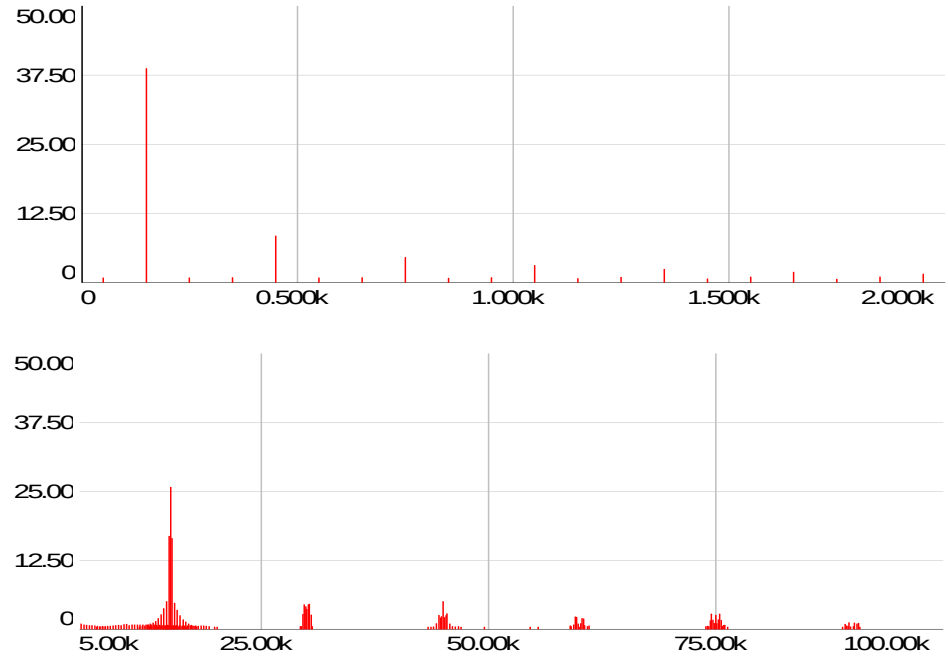


Figure 7.10 DPWM1 ripple current spectrum, low frequency harmonics (top, 12.5A/div, 500Hz/div), high frequency harmonics (bottom, 12.5A/div, 25kHz/div), ($M_i$=0,7, φ = 0°, $I_{om}$=100 A)

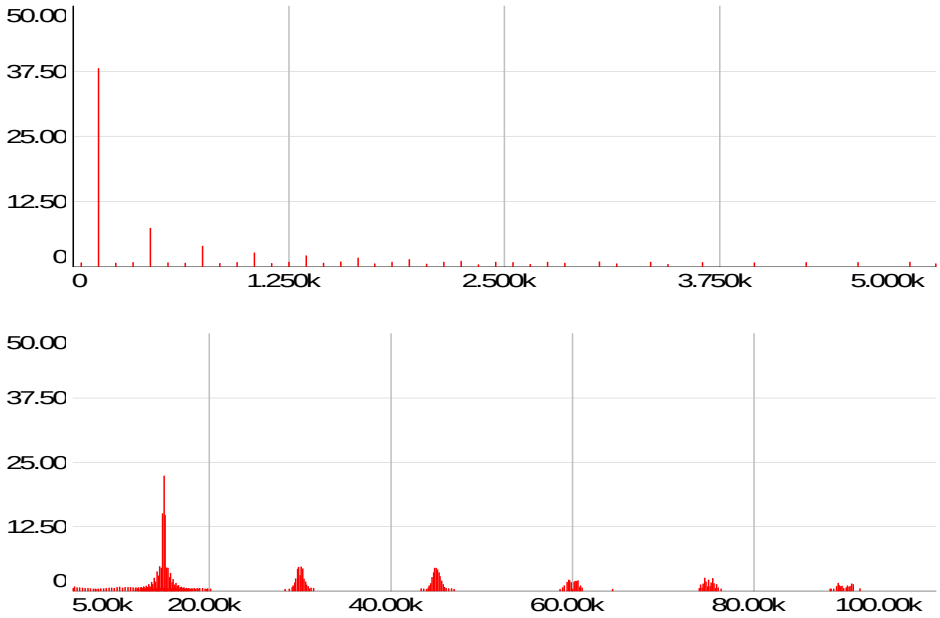


Figure 7.11 DPWM1 ripple current spectrum, low frequency harmonics (top, 12.5A/div, 1.25kHz/div), high frequency harmonics (bottom, 12.5A/div, 20kHz/div), ($M_i$=0,7, φ = 30°, $I_{om}$=100 A)

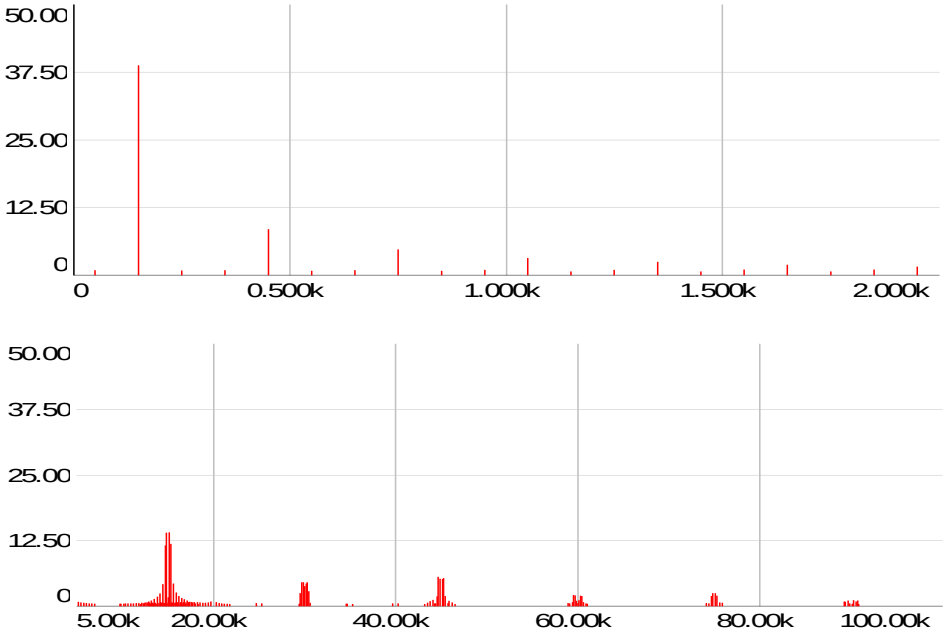


Figure 7.12 NSPWM ripple current spectrum, low frequency harmonics (top, 12.5A/div, 20kHz/div), high frequency harmonics (bottom, 12.5A/div, 20kHz), ($M_i$=0,7, φ = 0°, $I_{om}$=100 A)

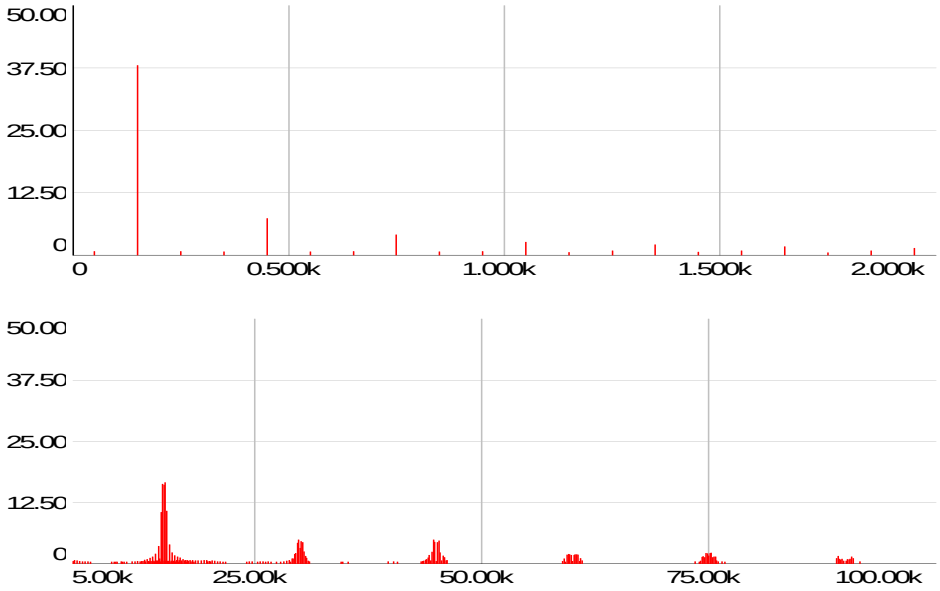


Figure 7.13 NSPWM ripple current spectrum, low frequency harmonics (top, 12.5A/div, 500Hz/div), high frequency harmonics (bottom, 12.5A/div, 25kHz/div), ($M_i$=0,7, φ = 30°, $I_{om}$=100 A)

As illustrated in the graphs, for the continuous PWM methods, at low $M_i$, the dc bus current harmonics are dominant at the $f_s$ and double the $f_s$, and the magnitude of harmonics at low frequencies (150Hz, 450Hz) are very low. In the discontinuous PWM methods at high $M_i$, there occures dc bus current of low frequency in huge magnitude and this is the largest dc bus current harmonic compared with the harmonics of high frequency of which the dominant one occures at $f_s$.

Generally for all operating conditions, the harmonic content of the rail currents can be calculated analytically via using double fourier integral. Depending on different modulation technique and carrier type, the domain in which fourier integral is calculated differs and this domain is the finger print of modulation method in the sense of dc bus current harmonics. The triangular carrier type used in this simulation is the Phase Disposition (PD) carrier. In this type, two carriers in the same phase are used for each positive and negative cycle of the modulation waveform as shown in Figure 7.14.

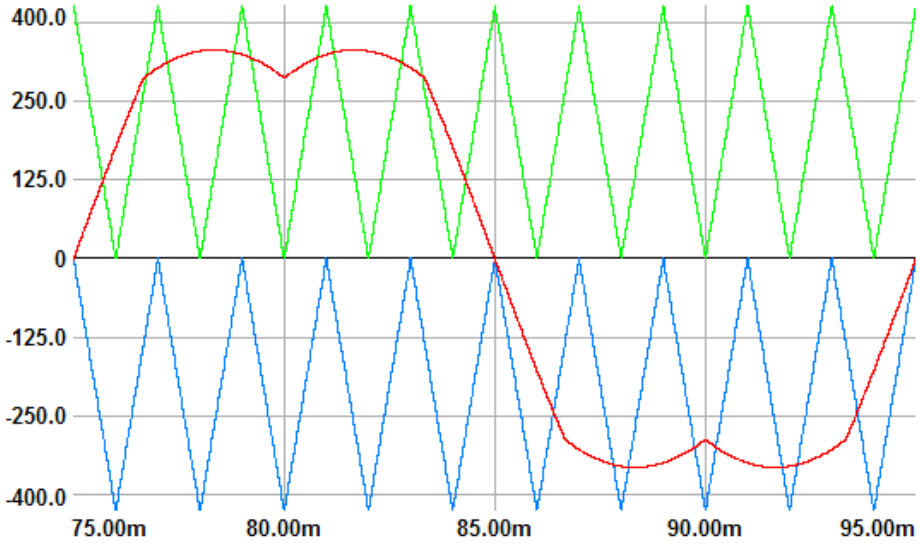


Figure 7.14 PD carrier waveforms: carrier for positive cycle of modulation waveform (green ) and carrier for negative cycle of modulation waveform (blue)

The limits used for harmonic spectrum calculation of $I_{dc\_P}$ is different than the limits used for $I_{dc\_N}$. The inner integral limits used for $I_{dc\_P}$ for two types of triangular carriers are shown in Figure 7.15 and the limits for $I_{dc\_N}$ are illustrated in Figure 7.16. In order to analyze the neutral current harmonics, the linearity of double fourier is used as in (7.1).

$$F(I_{dc_O}) = F[-(I_{dc_P} + I_{dc_N})] = -F(I_{dc_P}) - F(I_{dc_N}) \tag{7.1}$$

The analysis guidelines demonstrated in this chapter can be also used for multi-level PWM VSIs. The key point is to define the fourier integration domain and to observe the dc bus current circulation path through the switches and the dc bus capacitor bank. After the decomposition of $I_{dc}$ current, last step is to use the linearity property of fourier integral in order to calculate the overall harmonic spectrum.

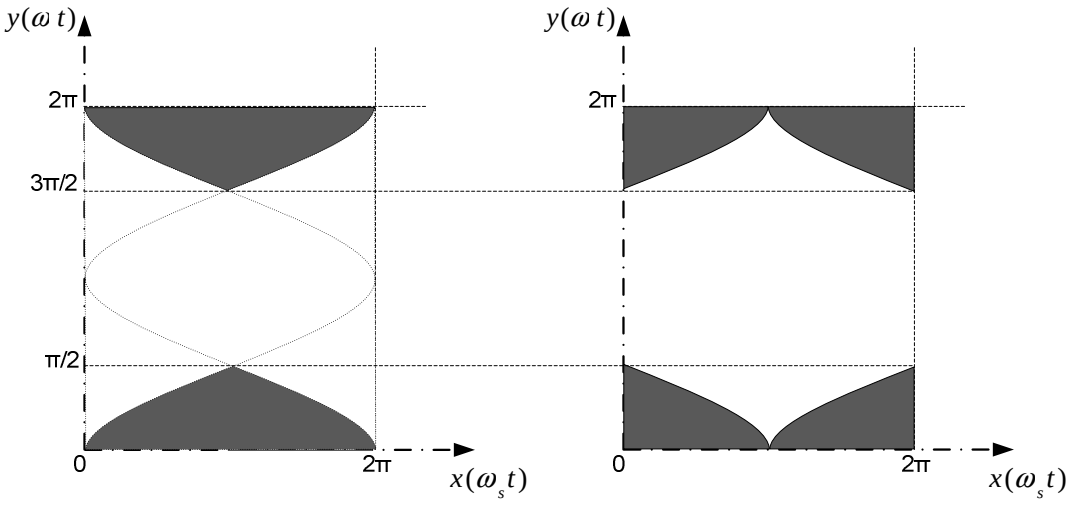


Figure 7.15 Inner Integral calculation domains (grey region) for normal triangular carrier (left) and reverse triangular carrier (right) for positive cycle of modulation signal

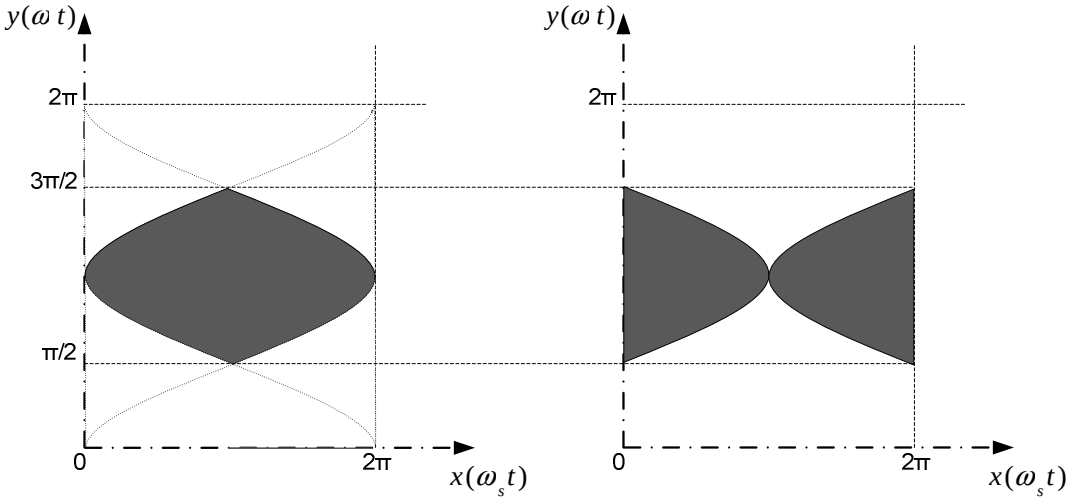


Figure 7.16 Inner Integral calculation domains (grey region) for normal triangular carrier (left) and reverse triangular carrier (right) for negative cycle of modulation signal

In summary, the double fourier analysis tool of 2L PWM VSI can be extended to 3L and multi level PWM VSI topologies and a correlation can be done between the inner fourier integral limits and the spectrum of various PWM VSI topologies.

# CHAPTER 8

# CONCLUSIONS

This thesis work mainly reviewed the dc bus ripple current characteristics of three-phase voltage source inverters, evaluated the spectral characteristics, and provided a simple approximation for spectral components.

In chapter 2, four main PWM VSI topologies are demonstrated with sample harmonic spectrum graphics of dc bus currents. The circulation paths and the contributers of dc bus current are illustrated with schematics of topologies. The application areas of these topologies are also mentioned.

In chapter 3, the dc bus current waveform is focused on to explain the mechanism of the construction of it's harmonic spectrum. Thus, the $I_{dc}$ waveforms of all four main modulation methods are examined in one switching period and a correlation is obtained between $I_{dc}$ current rectangles distribution and the harmonic spectrum. Double fourier transformation is demonstrated as an analysis tool for calculation of spectrum of pulse width modulated dc bus current. The equivalent centered harmonic approach, which models the carrier and sideband dc bus capacitor current harmonics with an equivalent harmonic at the center (same is applied to the multiples of $f_c$), is demonstrated. This simplification aids in clear understanding the dominant harmonics and their effects. As a consequence, with this approach, capacitor losses (ESR or dielectric) and voltage ripple can be accurately calculated. The centered current harmonics are put in 3-D graphic for look-up to be used in dc bus capacitor design. Therefore, the designer does not have to do complex

calculations such as double Fourier integrals and involved computational algorithms.

In chapter 4, the power electronic capacitors are investigated. In high voltage and high power applications, film and electrolytic capacitors are used depending on their high voltage and ripple current ratings, thus these types of capacitors are focused on in the scope of the thesis work.

In chapter 5, typical PWM VSI applications are investigated in detail and these applications are grouped under three main operating points ($M_i$, $\varphi$). In addition, PWM methods are evaluated and suggested for these typical operating points with the dc bus ripple performance being the main constraint. Dc bus capacitor design examples are given for these typical applications. Moreover, full system rectifier simulation is done covering all these three operating points and all four modulation methods. The fft results are compared with the analytical calculation outputs. The ac side of the inverter is investigated briefly with some simulation outputs.

In chapter 6, experimental results are interpreted. In the experimental setup, the high frequency dc bus capacitor current data are collected and fft of these data are plotted in the Matlab plotter tool. The aggreement between these fft graphs and the 3D equivalent harmonic graph is investigated and high correlation is observed.

In chapter 7, the three level (3L) three phase PWM VSI is investigated briefly and it is shown that the analytical tool of double fourier can be used to analyze the harmonic spectrum of dc bus rail and neutral point currents via making some modifications to the analysis steps used in two level PWM VSI.

Overall, this thesis work supplies the main tools in order to improve the design of an inverter and it’s dc bus capacitor via obtaining simple 3D look up graph, a basic design algorithm and grouping the applications with specific design examples.

As future work, the investigation of dc bus rail and neutral point currents of three phase three and multi level PWM VSIs could be done as an extension of this thesis work.

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## APPENDIX A

## MATLAB CODE FOR DOUBLE FOURIER ANALYSIS

```
% ********************************************************************
% By:  Ufuk Ayhan
% Date:  31/12/2011
% ********************************************************************
% “modulator_svp” function defines the SVPWM  waveform
% “y” is the array in the range 0 < y <2pi with data points predefined by integral
% calculator (quad(.) function)
% M is the scaled modulation index of M = Mi * 1.273
function out1 = modulator_svp(y,beta,M,m)

y = mod(y+beta,2*pi);
[k,l] = size(y);
sign=1;
for(i =1:l)

   if ((y(i) >= 0 & y(i) <= pi/3) | (y(i) > pi & y(i) <= 4*pi/3))
      func = (sqrt(3)/2)*M*cos(y(i)-pi/6);
      out1(i) = modulator_int(func,m);
   elseif ((y(i) > pi/3 & y(i) <= 2*pi/3) | (y(i) > 4*pi/3 & y(i) <= 5*pi/3))
      func = (3/2)*M*cos(y(i));
      out1(i) = modulator_int(func,m);
   elseif ((y(i) > 2*pi/3 & y(i) <= pi) | (y(i) > 5*pi/3 & y(i) <= 2*pi))
      func = (sqrt(3)/2)*M*cos(y(i)+pi/6);
```

```
        out1(i) = modulator_int(func,m);
    else
        error('interval is wrong');
    end
end
end
% “modulator_dp” function defines the DPWM1 waveform
function out = modulator_dp(y,beta,M,m)

y = mod(y+beta+pi/6,2*pi) - pi/6;
[k,l] = size(y);
sign = 1;
for(i =1:l)
    if ((y(i) >= -pi/6 & y(i) <= pi/6))
        func = 1;
        out(i) = sign*modulator_int(func,m);
    elseif ((y(i) > pi/6 & y(i) <= pi/2))
        func = (sqrt(3)*M*cos(y(i)-pi/6)-1);
        out(i) = sign*modulator_int(func,m);
    elseif ((y(i) > pi/2 & y(i) <= 5*pi/6))
        func = (sqrt(3)*M*cos(y(i)+pi/6)+1);
        out(i) = sign*modulator_int(func,m);
    elseif ((y(i) > 5*pi/6 & y(i) <= 7*pi/6))
        func = -1;
        out(i) = sign*modulator_int(func,m);
    elseif ((y(i) > 7*pi/6 & y(i) <= 3*pi/2))
        func = (sqrt(3)*M*cos(y(i)-pi/6)+1);
        out(i) = sign*modulator_int(func,m);
    elseif ((y(i) > 3*pi/2 & y(i) <= 11*pi/6))
        func = (sqrt(3)*M*cos(y(i)+pi/6)-1);
        out(i) = sign*modulator_int(func,m);
    else
```

```
        error('interval is wrong');
    end
end
end


% “modulator_ns” function defines the NSPWM waveform
function out = modulator_ns(y,beta,M,m)

y = mod(y+beta+pi/6,2*pi) - pi/6;
[k,l] = size(y);

for(i =1: l)
    if ((y(i) >= -pi/6 & y(i) <= pi/6))
        func = +1;
        out(i) = modulator_int(func,m);
    elseif ((y(i) > pi/6 & y(i) <= pi/2))
        func = (sqrt(3)*M*cos(y(i)-pi/6)-1);
        out(i) = modulator_int_comp(func,m);
    elseif ((y(i) > pi/2 & y(i) <= 5*pi/6))
        func = (sqrt(3)*M*cos(y(i)+pi/6)+1);
        out(i) = modulator_int_comp(func,m);
    elseif ((y(i) > 5*pi/6 & y(i) <= 7*pi/6))
        func = -1;
        out(i) = modulator_int(func,m);
    elseif ((y(i) > 7*pi/6 & y(i) <= 3*pi/2))
        func = (sqrt(3)*M*cos(y(i)-pi/6)+1);
        out(i) = modulator_int(func,m);
    elseif ((y(i) > 3*pi/2 & y(i) <= 11*pi/6))
        func = (sqrt(3)*M*cos(y(i)+pi/6)-1);
        out(i) = modulator_int(func,m);
    else
```

```
        error('interval is wrong');
    end
end
end


% modulator_AZS function defines the AZSPWM1 waveform
function out1 = modulator_azs(y,beta,M,m)

y = mod(y+beta,2*pi);
 [k,l] = size(y);

for(i =1:l)

    if((y(i) >= 0) & (y(i) <=pi))
        sign = -1;
    else
        sign =1;
    end

    if ((y(i) >= 0 & y(i) <= pi/3) | (y(i) > pi & y(i) <= 4*pi/3))
        func = (sqrt(3)/2)*M*cos(y(i)-pi/6);
        if( sign == 1)
            out1(i) = modulator_int(func,m);
        elseif (sign == -1)
            out1(i) = modulator_int_comp(func,m);
        end
    elseif ((y(i) > pi/3 & y(i) <= 2*pi/3) | (y(i) > 4*pi/3 & y(i) <= 5*pi/3))
        func = (3/2)*M*cos(y(i));
        if( sign == 1)
            out1(i) = modulator_int(func,m);
        elseif (sign == -1)
```

```
            out1(i) = modulator_int_comp(func,m);
        end
    elseif ((y(i) > 2*pi/3 & y(i) <= pi) | (y(i) > 5*pi/3 & y(i) <= 2*pi))
        func = (sqrt(3)/2)*M*cos(y(i)+pi/6);
        if( sign == 1)
            out1(i) = modulator_int(func,m);
         elseif (sign == -1)
            out1(i) = modulator_int_comp(func,m);
         end
    else
        error('interval is wrong');
    end
end
end

% function for the inner integral reduction for normal triangular carrier
% “m” is the integer multiplier of the carrier frequency (fc)
% “x” is the resultant array of calculation of magnitudes depending on modulation
% function
function out = modulator_int(x,m)

    out = (exp(i*m*(3*pi/2+ (pi/2)*x)) - exp(i*m*(pi/2 - (pi/2)*x)));

end

% function for the inner integral reduction for reverse triangular carrier
function out = modulator_int_comp(x,m)

    out = exp(i*m*(pi/2+(pi/2)*x)) - 1 + exp(i*m*2*pi) - exp(i*m*(pi/2)*(3-x));

end
```

```
% function for the overall double integral calculation for different PWM
% methods
% “n” is the integer multiplier of fundamental frequency (fo)
% “phi” is the phase angle in radians between the output of the inverter at
% fundamental frequency and the output current of one phase (one of a, b, c)
% “iL” is the magnitude of the output sinusoidal current
% “beta” is the phase angle between balanced three phases (2pi / 3 in radians)
% “mod_select” defines the modulation function under spectrum calculation
function out = fourier_multiplier(m, n, phi, M, iL, beta, mod_select)

switch  mod_select

    case 1  % SVPWM
       f = @(y) exp(i*n*y) .* cos(y-phi) .* modulator_svp(y,beta,M,m); % SVPWM
       Int11 = quad(f,0,2*pi,0.0000001);
       mn_iV1 = (iL/(i*2*pi^2*m)) * Int11;
       out = mn_iV1;

   case 2 % DPWM1
       f = @(y) exp(i*n*y) .* cos(y-phi).* modulator_dp(y,beta,M,m); %DPWM
       Int11 = quad(f,0,2*pi,0.00001);
       mn_iV1 = (iL/(i*2*pi^2*m)) * Int11;
       out = mn_iV1;

   case 3 % NSPWM
       f = @(y) exp(i*n*y) .* cos(y-phi) .* modulator_ns(y,beta,M,m); % NSPWM
       Int11 = quad(f,0,2*pi,0.0000001);
       mn_iV1 = (iL/(i*2*pi^2*m)) * Int11;
       out = mn_iV1;

   case 4 % AZSPWM1
       f = @(y) exp(i*n*y) .* cos(y-phi) .* modulator_azs(y,beta,M,m); % AZSPWM
```

```
    Int11 = quad(f,0,2*pi,0.00001);
    mn_iV1 = (iL/(i*2*pi^2*m)) * Int11;
    out = mn_iV1;

 end

% “leg_spectrum” function calculates the harmonic spectrum of one leg of inverter
% “delta” is the space between bunches of fringes of switching frequency integer
% multiples
% n_fringe is the number of fringes per switching frequency multiple
% n_wc is the number of multiples of switching frequency to plot
% fc is the switching (carrier) frequency
% fo is the fundamental frequency of modulating function
function out = leg_spectrum (fc, fo, n_wc, n_fringe, delta, phi, M, iL, beta,
mod_select)

phi = -1 * phi;
pf = phi + beta;
wc = 2*pi*fc;
wo = 2*pi*fo;
fringe_array = zeros(1, ((n_fringe + 1) * n_wc + (n_wc - 1) * delta));
i = 0; Amn = 0; Bmn = 0;

for  m = 1 : n_wc

   for  n = (-n_fringe/2) : (n_fringe/2)

       i = i + 1;
       AB_mn = fourier_multiplier(m, n, phi, M, iL,beta,mod_select);
       fringe_array(1, (i + (m-1)*(n_fringe+1) + (m-1)*delta)) = AB_mn;

   end
```

```
    i = 0;
end

out = fringe_array;

end
% “dc_link_spectrum” function calculates the harmonic spectrum of Idc
function [out1, out2] = dc_link_spectrum(fc, fo, n_wc, n_fringe, delta, phi, M,
iL,mod_select)

[f1, f2] = leg_spectrum(fc, fo, n_wc, n_fringe, delta, phi, M, iL, 0, mod_select);
[f3, f4] = leg_spectrum(fc, fo, n_wc, n_fringe, delta, -2*pi/3+phi, M, iL, -2*pi/3,
mod_select);
[f5, f6] = leg_spectrum(fc, fo, n_wc, n_fringe, delta, -4*pi/3+phi, M, iL, -4*pi/3,
mod_select);
out1 = f1 + f3 + f5;  % addition of leg spectrums for over carrier band
out2 = f2 + f4 + f6;  % addition of leg spectrums for sub carrier band

end
%  ****************************************************************
%  *   this is the 3D Equivalent Harmonic plotting function       *
%  *   fc: carrier frequency                                      *
%  *   fo: output frequency                                       *
%  *   n_wc: number of centers (1*fc, 2*fc, ....)                 *
%  *   n_fringe: number of harmonic fringes around center         *
%  *   delta: space between center bunches                        *
%  *   iL: magnitude of output load current                       *
%  *   mod_select: selection of modulation type:                  *
%  *            1) SVPWM                                          *
%  *            2) DPWM1                                          *
%  *            3) NSPWM                                          *
%  *            4) AZSPWM                                         *
```

```
%  *  plot_select:                                                    *
%  *          1) line bar graph                                       *
%  *          2) 3D bar graph of unified harmonics                    *
%  ************************************************************
function dc_link_spect_3D_rms_plot(fc, fo, n_wc, n_fringe, delta,iL,
mod_select,plot_select)

spectrum_array_m = zeros(11, ((n_fringe + 1) * n_wc + (n_wc-1)*delta));

fringe_mag_1 = zeros(11,11);
fringe_mag_2 = zeros(11,11);
fringe_mag_3 = zeros(11,11);
fringe_mag_4 = zeros(11,11);
fringe_mag_5 = zeros(11,11);
fringe_mag_6 = zeros(11,11);
fringe_mag_7 = zeros(11,11);
fringe_mag_8 = zeros(11,11);
fringe_mag_9 = zeros(11,11);
fringe_mag_10 = zeros(11,11);
fringe_mag_rms = zeros(11,11);
I_hrms_sqr = zeros(11,11);
fr_mag_1 = 0;fr_mag_2 = 0;fr_mag_3 = 0;fr_mag_4 = 0;fr_mag_5 = 0;fr_mag_6 =
0;fr_mag_7 = 0;fr_mag_8 = 0;fr_mag_9 = 0;fr_mag_10 = 0;

switch  plot_select

case 1

    for i = 1:11

        [s1, s2] = dc_link_spectrum(fc, fo, n_wc, n_fringe, delta, 0,i/10,
        iL,mod_select);
```

```
            spectrum_array_m(i,:) = s1;        % s1: carrier integer multiple harmonics
                                               % s2: subcarrier harmonics
        end
        bar3(abs(spectrum_array_m));

case 2

for i = 1:11                                   % loop index for Modulation index
      for k = 1:11                             % loop index for output current phase

        [s1, s2] = dc_link_spectrum(fc, fo, n_wc, n_fringe, delta, -(pi/20)*(k-1)
         ,i*1.273/10, iL,mod_select);
        spectrum_array_m(i,:) = s1;    % modulation arrays ( Mi = 0.1, Mi = 0.2, ....)

        for j = 1:(n_fringe+1)
% summation of squares of harmonics around center
fr_mag_1 = fr_mag_1 + abs(spectrum_array_m(i,j))^2;
fr_mag_2 = fr_mag_2 + abs(spectrum_array_m(i,j+n_fringe+1+delta))^2;
fr_mag_3 = fr_mag_3 + abs(spectrum_array_m(i,j+2*(n_fringe+1)+2*delta))^2;
fr_mag_4 = fr_mag_4 + abs(spectrum_array_m(i,j+3*(n_fringe+1)+3*delta))^2;
fr_mag_5 = fr_mag_5 + abs(spectrum_array_m(i,j+4*(n_fringe+1)+4*delta))^2;
fr_mag_6 = fr_mag_6 + abs(spectrum_array_m(i,j+5*(n_fringe+1)+5*delta))^2;
fr_mag_7 = fr_mag_7 + abs(spectrum_array_m(i,j+6*(n_fringe+1)+6*delta))^2;
fr_mag_8 = fr_mag_8 + abs(spectrum_array_m(i,j+7*(n_fringe+1)+7*delta))^2;
fr_mag_9 = fr_mag_9 + abs(spectrum_array_m(i,j+8*(n_fringe+1)+8*delta))^2;
fr_mag_10 = fr_mag_10 + abs(spectrum_array_m(i,j+9*(n_fringe+1)+9*delta))^2;
end

fringe_mag_rms(i,k) =
sqrt(fr_mag_1+fr_mag_2+fr_mag_3+fr_mag_4+fr_mag_5+fr_mag_6+fr_mag_7+
fr_mag_8+fr_mag_9+fr_mag_10);
```

```
fringe_mag_1 (i,k) = sqrt(fr_mag_1);
fringe_mag_2 (i,k) = sqrt(fr_mag_2)
fringe_mag_3 (i,k) = sqrt(fr_mag_3);
fringe_mag_4 (i,k) = sqrt(fr_mag_4);

fr_mag_1 = 0; fr_mag_2 = 0; fr_mag_3 = 0; fr_mag_4 = 0; fr_mag_5 = 0;
fr_mag_6 = 0; fr_mag_7 = 0; fr_mag_8 = 0; fr_mag_9 = 0; fr_mag_10 = 0;

end
end
% plotting commands
 x_axis = [0:10] * 0.1;
 subplot(1,5,1);
 bar3(x_axis,fringe_mag_rms/100 );
 subplot(1,5,2);
 bar3(x_axis,fringe_mag_1/100 );
 subplot(1,5,3);
 bar3(x_axis,fringe_mag_2/100 );
 subplot(1,5,4);
 bar3(x_axis,fringe_mag_3/100 );
 subplot(1,5,5);
 bar3(x_axis,fringe_mag_4/100 );

 end
```