A LOW-COST UNCOOLED INFRARED DETECTOR ARRAY AND ITS CAMERA ELECTRONICS

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
MIDDLE EAST TECHNICAL UNIVERSITY

BY

DİNÇAY AKÇÖREN

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF MASTER OF SCIENCE
IN
ELECTRICAL AND ELECTRONICS ENGINEERING

FEBRUARY 2011

Approval of the thesis:

A LOW-COST UNCOOLED INFRARED DETECTOR ARRAY AND ITS CAMERA ELECTRONICS

submitted by **DİNÇAY AKÇÖREN** in partial fulfillment of the requirements for the degree of **Master of Science in Electrical and Electronics Engineering Department, Middle East Technical University** by,

Prof. Dr. Canan Özgen _____
Dean, Graduate School of **Natural and Applied Sciences**

Prof. Dr. İsmet Erkmen _____
Head of Department, **Electrical and Electronics Engineering**

Prof. Dr. Tayfun Akın _____
Supervisor, **Electrical and Electronics Engineering, METU**

Asst. Prof. Dr. Selim Eminoğlu _____
Co-supervisor, **Micro and Nanotechnology Program, METU**

Examining Committee Members:

Prof. Dr. Cengiz Beşikci
Electrical and Electronics Engineering, METU _____

Prof. Dr. Tayfun Akın
Electrical and Electronics Engineering, METU _____

Asst. Prof. Dr. Selim Eminoğlu
Micro and Nanotechnology Program, METU _____

Assoc. Prof. Dr. Haluk Kulah
Electrical and Electronics Engineering, METU _____

Assoc. Prof. Dr. Ali Ziya Alkar
Electrical and Electronics Engineering, Hacettepe University _____

Date: _____

I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

Name, Last Name: DİNÇAY AKÇÖREN

Signature :

ABSTRACT

A LOW-COST UNCOOLED INFRARED DETECTOR ARRAY AND ITS CAMERA ELECTRONICS

Akçören, Dinçay

M.S., Department of Electrical and Electronics Engineering

Supervisor : Prof. Dr. Tayfun Akın

Co-Supervisor : Asst. Prof. Dr. Selim Eminoğlu

February 2011, 75 pages

This thesis presents the development of integrated readout electronics for diode type microbolometers and development of external camera electronics for microbolometers. The developed readout electronics are fabricated with its integrated 160x120 resolution FPA (Focal Plane Array) in the XFAB SOI-CMOS 1.0 μm process. The pixels in the FPA have 70 μm pixel pitch, and they are sensitive in the 8–12 μm band of the infrared spectrum. Each pixel has 4 serially connected diodes, and diode turn on voltage changes as the temperature of the suspended and thermally isolated pixel increases due to the absorbed infrared power. Suspension of the pixels is obtained with a post-CMOS MEMS etching process, but this process requires no critical litography and/or deposition steps. This dramatically reduces the detector process cost, which makes this microbolometer FPA suitable for ultra low-cost applications such as automobile, security, and commercial applications. The readout electronics of the FPA include digital blocks such as timing and programming blocks as well as analog blocks such as a differential trans-conductance amplifier, a switched capacitor integrator, a sample-and-hold, and current DACs. This new readout design has reduced number of pins to simplify the external electronics and allows wafer-level vacuum packaging compared to the 128x128

FPA developed in a previous study at METU with the same approach. Both of these features further decrease the cost.

Two kinds of external camera electronics are developed for two SOI type microbolometers. The first one is for the 128x128 SOI microbolometer previously designed in METU. The developed external camera electronics have $1.5mV_{rms}$ noise, which is much less than the microbolometer noise. The overall system has an average NETD of 465 mK and a peak NETD of 320mK. The second developed external camera electronics are for the 160x120 SOI microbolometers that developed in the scope of this thesis. The developed external camera electronics has $0.55mV_{rms}$ noise which is much less than the bolometer noise which is $5mV_{rms}$. The overall system has an average NETD of 820 mK and a peak NETD of 350 mK. Each of these external camera electronics include a custom designed PCB, an FPGA board with appropiate configurion and a software working on a PC. The custom designed PCB holds the external components for the microbolometer, an FPGA takes and processes the bolometer data and it sends to a PC, and a PC processes these data and forms a streaming video. These two external camera electronics allow to obtain human images verifying that the developed microbolometers can be used for security and automotive applications.

Keywords: uncooled infrared detectors, low-cost SOI microbolometers, bolometer external electronics, readout electronics for diode type microbolometers

ÖZ

DÜŞÜK MALİYETLİ SOĞUTMASIZ KIZILÖTESİ DETEKTÖR DİZİNİ VE KAMERA ELEKTRONİĞİ

Akçören, Dinçay
Yüksek Lisans, Elektrik ve Elektronik Mühendisliği Bölümü
Tez Yöneticisi : Prof. Dr. Tayfun Akın
Ortak Tez Yöneticisi : Yard. Doç. Dr. Selim Eminoğlu

Şubat 2011, 75 sayfa

Bu tezde diyot tipi mikrobolometreler için okuma devresi geliştirilmesi ve mikrobolometreler için harici kamera elektroniği geliştirilmesi sunulmuştur. Geliştirilen okuma devresi, kendisiyle bütünleşik 160x120 çözünürlükteki ODM (Odak Düzlem Matrisi) ile XFAB 1.0 μm SOI-CMOS teknolojisi ile üretilmiştir. Odak düzlem matrisindeki pikseller 70 μm adım uzunluğunda ve kızılötesi spektrumun 8–12 μm bandına duyarlıdır. Her piksel, seri baglı 4 diyottan oluşur ve diyot açılma voltajı, asılı ve ısıl yalıtkan pikselin emdiği kizilötesi güç yüzünden artan sıcaklığından dolayı değişir. Piksellerin asılı hale gelmesi, CMOS-sonrası MEMS kazıma süreci ile yapılır, fakat bu süreç herhangi bir kritik litografi ve serim adımı gerektirmez. Bu, dedektor süreç maliyetini çok düşürür ve bu mikrobolometre ODM'sini otomotiv, güvenlik ve ticari uygulamalar gibi çok düşük maliyetli uygulamalar için cazip hale getirir. ODM'nin okuma devresi zamanlama ve programlama blokları gibi sayısal blokları içerdiği gibi fark-geçiş-iletimi yükselteci, anahtarlamalı kapasitör integratörü, örnekle-ve-tut devresi ve akım sayısal-analog çevirici devrelerini de içermektedir. Bu yeni okuma devresi tasarımı, ODTU'de daha önceden tasarlanan 128x128 ODM'ye kıyasla, gerekli pin sayısını, harici elektroniği basitleştirmek için, düşürmüştür ve pul seviyesi vakum paketleme-

ye elverişlidir.

İki mikrobolometre için iki tip harici kamera elektroniği geliştirilmiştir. İlk geliştirilen, ODTÜ'de daha once tasarlanan 128x128 mikrobolometre içindir. Geliştirilen harici kamera elektroniğinin gürültü seviyesi 8.4mV_{rms} olan mikrobolometrenin gürültü seviyesinin çok altında olup 1.5mV_{rms}'tir. Tüm sistemin ortalama GDSF'si (Gürültüye Denk Sıcaklık Farkı) 465 mK ve tepe GDSF'si 320 mK'dir. İkinci geliştirilen harici kamera elektroniği bu tez kapsaminda geliştirilmiş olan 160x120 mikrobolometre içindir. Geliştirilen harici kamera elektroniğinin gürültü seviyesi 0.55mV_{rms}'dir ve bu değer 5mV_{rms} olan mikrobolometrenin gürültü seviyesinden çok aşagıdadır. Genel sistemin ortalama GDSF'si 820 mK ve tepe GDSF'si 350 mK'dir. Bu iki kamera elektroniği de bir özel tasarlanmış baskıdevre kartı, bir uygun olarak programlanmı ş FPGA ve bilgisayar üzerinde çalışan bir yazılımıiçermektedir. Özel tasarlanmış baskıdevre kartı gerekli harici devre elemanlarını barındırır; FPGA, mikrobolometre verisini alır, işler ve bilgisayara yollar; bilgisayar bu veriyi işler ve akan bir video görüntüsü oluşturur. Bu iki kamera elektroniği ile insan görüntüleri alınmıştır ve bu görüntüler geliştirilen mikrobolometrelerin güvenlik ve otomotiv uygulamalarında kullanılabileceğini doğrulamıştır.

Anahtar Kelimeler: soğutmasız kızıl ötesi dedektörler, düşük maliyetli mikrobolometreler, bolometre harici elektroniği, diyot tipi mikrobolometreler için okuma devreleri

To my family and
"My rainbow" Derya

ACKNOWLEDGMENTS

I would like to express my appreciation and gratitude to my advisor Prof. Dr. Tayfun Akın and Asst. Prof. Dr. Selim Eminoğlu for their guidance, support, and help throughout my thesis study and graduate life. I am grateful to Orhan Akar for his effort for the post-CMOS fabrication of the chips. I would like to thank to Dr. Yusuf Tanrıkulu and Selçuk Keskin for their wire-bondings. I would like to thank to "Duchess" Şeniz Esra Küçük for her help in NETD calculations. I would also like to thank Alperen Toprak and Burak Eminoglu for sharing their knowledge and experience.

Thanks to all members of DZ-15 for their friendship. They create a lovely environment that I am very happy to work in.

Thanks to all members of the MEMS-VLSI, BIO-MEMS and RF-MEMS research groups for providing a friendly environment.

I would like to express my appreciation to TÜBİTAK for their support of my M.Sc. study with their scholarship.

Last but not least, I would like to thank my family for their continuous support and encouragement through all my life.

TABLE OF CONTENTS

LIST OF TABLES

TABLES

LIST OF FIGURES

FIGURES

CHAPTER 1

INTRODUCTION

There are two main types of detectors used in infrared imaging: photon detectors and thermal detectors. Photon detectors measure the incident photons on the detector by using low-bandgap semiconductor structures. Incident photons excite electrons in the semiconductor lattice and create electron-hole(E-H) pairs. The amount of created E-H pairs is proportional to the amount of incident photons. By measuring the E-H pairs, the incident infrared radiation on the detector can be determined. Typical applications of photonic infra-red detectors are military applications, medical imaging, and space observation. The examples of photonic IR detectors in literature are QWIP (Quantum Well Infrared Detector) [1], MCT (Mercury Cadmium Telluride) [2], InSb (Indium Antimonide) [3], and super lattice detectors [4].

A thermal detector measure the absorbed heat from an IR source by the detector. This heat is coming from the absorbed infrared radiation. The heat increases the temperature of the detector. This temperature increase changes an electrical parameter (voltage, current or charge) of the circuit on the detector. By measuring the change in the parameter, the amount of incident infrared radiation can be determined. There are many different approaches to measure the incident IR, and each method leads to a different type thermal detector. Most widely known ones are pyroelectric detectors [5], thermopiles [6], and microbolometers [7].

Pyroelectric detectors use the pyroelectric effect, i.e., when the temperature of a crystal structure is changed, the crystal generates electricity. The main advantage of these detectors are that they do not require any bias, so they have no self heating problems. However, their DC responsivity is zero, so a chopper should be employed. Also, their CMOS integration is difficult.

Thermopiles are made of serially connected thermocouples. A thermocouple is formed by

joining two conductive materials with a junction. When a thermocouple is heated at one end it generates voltage because of the Seebeck effect. The Seebeck effect is a conversion from temperature difference to a voltage. Serial connection of many thermocouples amplifies the generated voltage. The main advantage of thermopiles is they do not require any bias, so they have no self heating problems, like pyroelectric detectors. Also, their noise levels are very low. The drawbacks of thermopiles are: their signal levels are low which require very low noise electronics and their pixel sizes are large which limits their usage to low resolution applications.

Microbolometers are the most widely used type of thermal detectors. The next section is dedicated to microbolometers because this thesis is focused on microbolometer type infrared detectors that use suspended diode structures to detect infrared radiation.

1.1 Microbolometers

A microbolometer is an infrared sensor that changes an elecrtical parameter (mostly resistnace) as the sensor temperature changes due to the infrared illumination. The amount of resistance change is proportional to the absorbed heat due to the incident infrared radiation. Most of the bolometers are resistive-type, but there are also diode-type microbolometers like the one studied in the scope of this thesis. The resistive-type microbolometers measure the resistance change of the sensitive resistor on the detector, while the diode-type microbolometers measure the voltage change of a forward biased diode.

A microbolometer pixel can be fabricated with both surface micromachining and bulk micromachining. Figure 1.1 gives a typical surface micromachined pixel structure, and Figure 1.2 gives a typical bulk micromachined pixel structure [9]. Both type of the pixels have an absorber and support arms that also carries the interconnect layer.

The absorber layer provides high IR absorption, maximizing the energy received from IR radiation. A larger absorber area and higher absorption coefficient increase the absorbed radiation; therefore, the detector gives higher response to the same radiation level.

The purposes of the interconnect layer are to mechanically support the pixel and to provide a

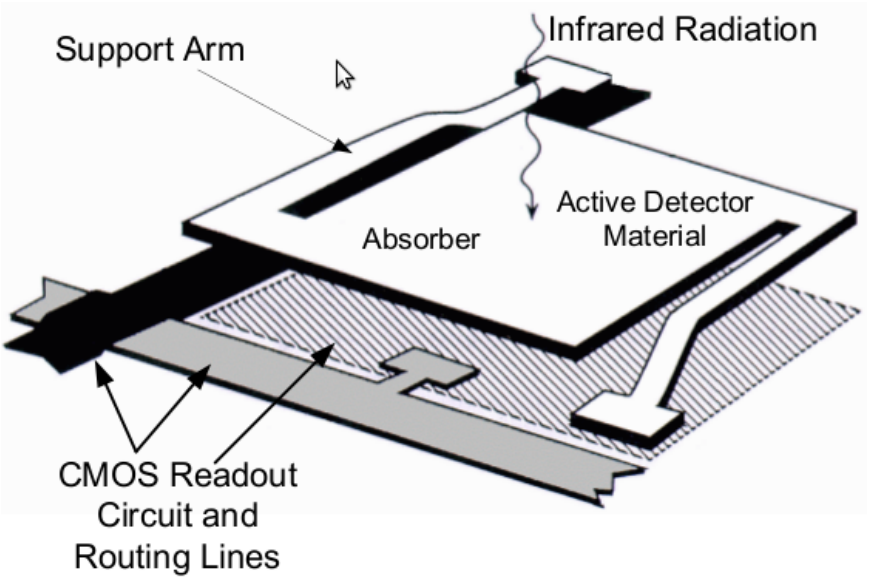

Figure 1.1: Surface micromachined microbolometer pixel structure [8].

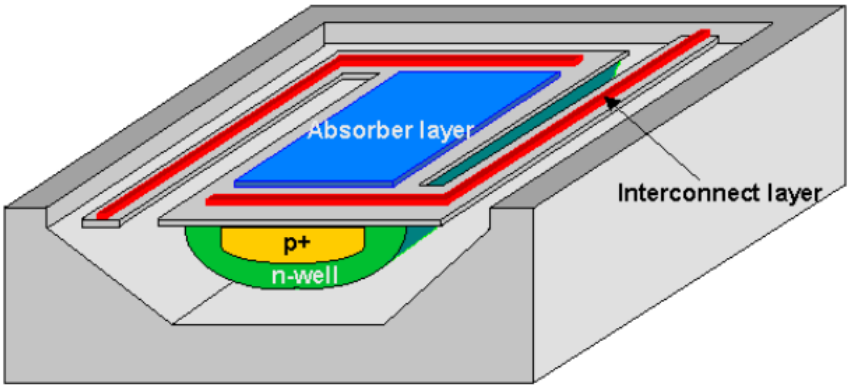

Figure 1.2: Bulk micromachined microbolometer pixel structure developed previously at METU for low-cost microbolometers that can be developed from a standard CMOS process [9].

good thermal isolation of the pixel from the bulk as well as provide an electrical connection. Thinner and longer support arms provide better thermal isolation. Typical received power from IR radiation of a pixel is in the order of nanowatts. Therefore, a good thermal isolation is required for the pixel to heat up.

1.1.1 Performance Parameters

There are some performance parameters of a pixel structure. Most widely used ones are responsivity and NETD (Noise Equivalent Temperature Difference).

Responsivity is defined as the ratio of the signal change of the detector over the incident power on it. It is given as

$$\mathfrak{R} = \frac{\Delta V_o}{P_i} \tag{1.1}$$

where ΔV_o is output voltage change of the detector and P_i is the incident IR power on detector.

Higher responsivity means larger change in the output signal under the same level of incident radiation. It is easier to read small infrared radiations with higher responsivity, which can be achieved with higher absorbance and lower thermal conductance.

NETD is defined as the change in the temperature of a blackbody that results in the signal to noise ratio of one in the detector output signal [10]. It is given as

$$NETD = \frac{4F^2 V_n}{A_D \mathfrak{R} (\Delta p_{target} / \Delta T_{target})_{\lambda_1 - \lambda_2}} \tag{1.2}$$

where F is the F-number of the optics, V_n is the electrical noise of the bolometer, A_D is the active detector area, $\mathfrak{R}$ is the responsivity, and the term in parenthesis is the amount of emitted power change for unit temperature change of the object in a specific wavelength window of $\lambda_1 - \lambda_2$. This value is constant and equal to $2.62x10^{-5} W/(cm^2 K)$ for the 8-12 μm window and 300 K objects.

As seen from Equation 1.2, the noise of the detector has a direct effect on the NETD value. This noise includes the detector noise, the readout noise, and also the noise from the external electronics. Therefore, the low-noise readout electronics and external electronics have very important roles on the NETD value.

The NETD is important however the cost of the detectors is also an important parameter. There are some other groups that developed low-cost infrared imaging systems. Bosch developed a 100x50 FPA with 12.5 fps that has NETD of below 500mK, but it has 225μm pixel pitch [12]. Toshiba had reported a 160x120 SOI bolometer [13]. It has 30 fps with an NETD of 500mK, and the designed pixels have 32μm pixel pitch, but it is based on a custom SOI-CMOS process, limiting its cost reduction. ULIS reported a 160x120 TEC-less (Thermo-Electric Cooler-less) infrared bolometer with 25μm pixel pitch with an NETD of

86 mK [14]. They use amorphous silicon as the infrared sensitive material. However, their post-CMOS process requires 8 masks which limits their low-cost potential. The goal in this thesis is to obtain moderate performance microbolometer with very low cost approach.

1.2 Readout Architecture for Microbolometers

The readout architecture defines how an FPA (Focal Plane Array) is read, how the data is send to an output, and how the addressing of individual pixels in the FPA is done. Figure 1.3 shows the typical block diagram of a microbolometer readout architecture. An analog readout channel array is the main readout block. It amplifies and conditions the pixel outputs. The performance of the readout channel array directly effects the performance of the microbolometer. An output multiplexer multiplexes the readout channel outputs to a limited number of output pads. Larger format arrays usually require more than one output, because larger format arrays have higher data throughput and output time for one pixel is very short. Whereas one output is sufficient in small and mid-resolution FPAs. A vertical shift register addresses the pixels that are going to be read. During the normal operation, the vertical shift register addresses the whole FPA sequentially, allowing all FPA is read. A timing block generates the required timing signals for the readout channels (such as integration enable and sample) and the addressing blocks (such as shift enable and load).

1.3 Previous Work on Low-Cost Microbolometers in METU

All the microbolometers in literature require separate fabrication lines for their readout and detector array, and this increases the cost of the microbolometers. The aim of this study is to develop a monolithic bolometer that doesn't require any critical post-CMOS processing steps. The origin of this study goes back to 1997. The first developed microbolometer detectors were resistive type [15]. Because of the some problems in post-CMOS processing, diode-type detectors were started to be developed. Previous studies at METU include the development and fabrication of a 16x16 FPA [16, 17, 18], a 64x64 FPA [19], and a 128x128 FPA [20, 21]. The 16x16 FPA was the first microbolometer that allowed an image which was a hot soldering iron, as it had a lower performance. Due to the fabrication difficulties in the bulk diode structures, SOI structures were began to be developed, and a 64x64 and a 128x128 FPA

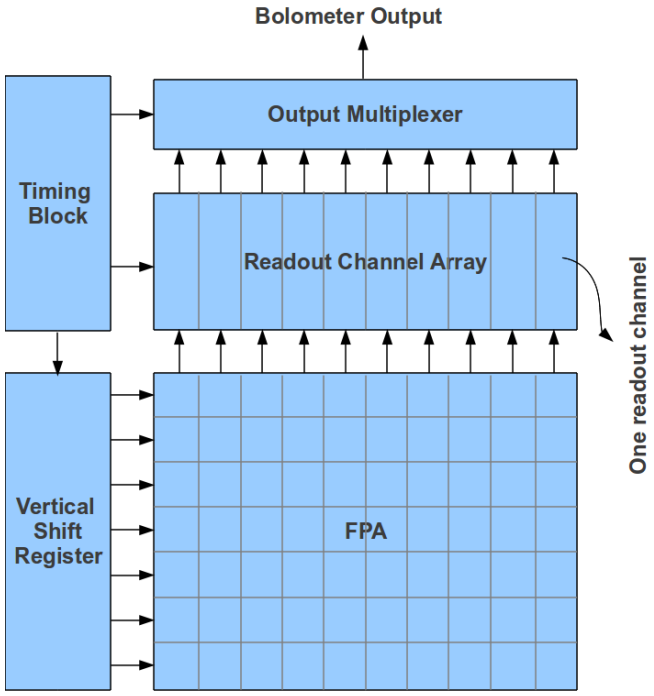

Figure 1.3: Readout architecture of a typical bolometer.

were designed and fabricated with the XFAB 1.0μm SOI-CMOS process. Figure 1.4 shows a hot soldering iron image taken from the 64x64 SOI-CMOS FPA. The first human images were taken in 2008 with the 128x128 SOI-CMOS microbolometer [11]. Figure 1.5 shows some sample human images taken from this bolometer. The reported NETD value for this bolometer is 1.11 K. The performance of this microbolometer was limited by its external camera electronics, and this thesis study started by developing a low noise external camera electronics to show the true performance of the 128x128 SOI-CMOS microbolometer FPA.

1.4 Research Objectives and Thesis Organization

The aim of this research is to develop a low-cost 160x120 microbolometer integrated electronics and camera electronics for this microbolometer. The specific and more detailed objectives can be listed as follows:

1. Design of readout electronics for the SOI pixel structure developed at METU. These

Figure 1.4: An image of hot soldering iron taken with the 64x64 SOI-CMOS microbolometer implemented with XFAB SOI-CMOS technology in METU.

include both analog blocks and digital blocks. The designed microbolometer should have a low-noise operation with a small silicon area.

2. Add some bolometer features like internal DACs and programming interface to reduce the pin count. This gives the bolometer an easier and cheaper operation. This also allows the microbolometer FPA to be vacuum packaged with wafer level packaging technology for lower cost detector array.

3. Design of an external camera electronics for the 128x128 microbolometer and the 160x120 microbolometer. The developed systems should be low-noise, easy to operate, and user-friendly.

4. Implementation of the software program to display and process the bolometer data. The software should include the basic image processing capabilities for the bolometers like one point correction, dead pixel correction, and gain correction.

The thesis organization is as follows:

Chapter 2 gives the details of the designed 160x120 SOI-CMOS microbolometer. Basic blocks and their operation principles are described and simulation results are presented. Chapter 3 shows the test results and verifications of the designed circuits explained in Chapter

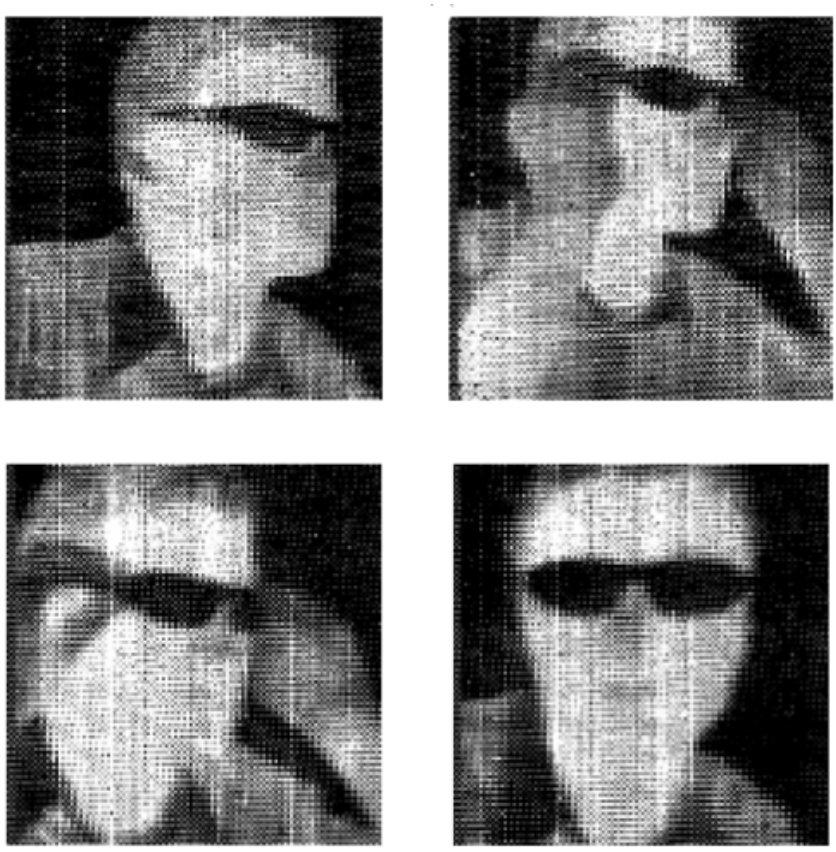

Figure 1.5: First human images taken in METU. The developed bolometer has 128x128 FPA and fabricated with the XFAB 1.0 μm SOI-CMOS technology.

2. Chapter 4 describes the developed camera electronics for the 128x128 SOI-CMOS microbolometer designed and fabricated in 2008 and the 160x120 SOI-CMOS microbolometer designed and fabricated in 2010. This chapter also presents the external electronics of a microbolometer, imaging setup, and data processing for the developed microbolometers. Chapter 5 gives a conclusion and points out the future works for the 160x120 SOI-CMOS microbolometer and the external camera electronics for this microbolometer.

CHAPTER 2

DESIGN OF THE 160X120 LOW-COST MICROBOLOMETER

This chapter gives the overview of the designed 160x120 low-cost SOI bolometer integrated electronics. The integrated electronic is composed of analog blocks for detector readings and digital blocks for generation of timing signals, pixel addressing and programming. Section 2.2 gives the details of the digital blocks, Section 2.3 gives the details and simulation results of the analog blocks, and Section 2.4 explains the floorplan of the chip.

2.1 Pixel Structures

The diode structures in XFAB SOI 1.0 μm process is N-Diff–P-Well type diodes with a gate polysilicon layer on top of it [25]. Figure 2.1 shows a diode layout for this process. The floating gate polysilicon may introduce noise to the pixels. Therefore different types of pixels with different gate biases are designed to see the effect of the gate voltage on noise levels of diodes. This effect cannot be observed in simulation because it is not modeled. Therefore no simulation data is presented. Four different pixel structures are designed with different gate voltage biases. Figure 2.2 shows the schematic view of the designed pixels.

The performance of the pixel structure can be increased by changing some parameters of the pixel such as the pixel pitch, the arm width or the active detector area. If the arm width or the active detector area can be increased the performance of the pixel increases, and the small pixel pitch decreases the silicon area that decrease the cost of the detectors. A set of pixels with different support arm widths, a set of pixels with different active area, and a set of pixels with different pixel pitch are designed for test purposes. Table 2.1 shows the specifications of

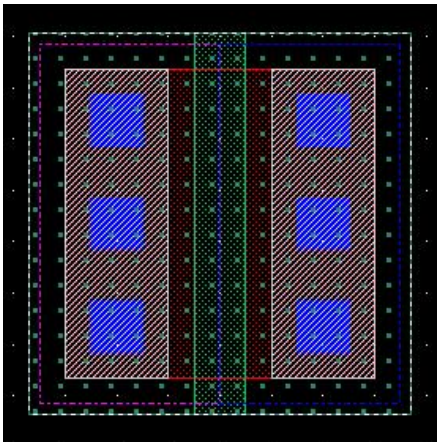

Figure 2.1: Diode structure in the XFAB 1.0μm SOI-CMOS process. Diodes are P-I-N type diodes with floating gates.

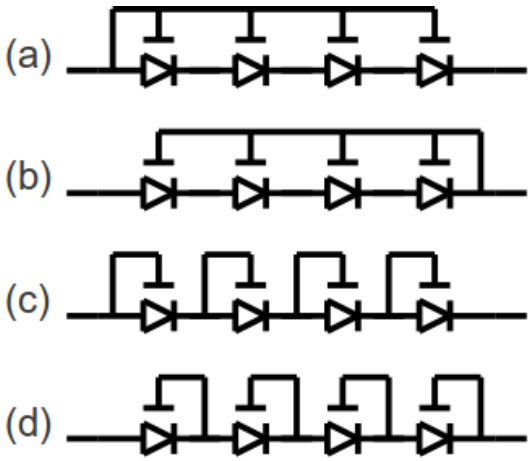

Figure 2.2: Pixels with different gate biases. The third terminal shows the gate connection. Four different pixel structures are (a) gate voltages are connected to highest voltage, (b) gate voltages are connected to lowest voltage, (c) each diode gate is connected to its highest voltage, and (d) each gate is connected to its lowest voltage.

the designed pixels and their expected NETD performances.

2.2 Digital Blocks

This section gives a detailed view of the designed digital blocks. The digital blocks can be grouped into 3 parts: addressing, timing, and programming blocks. The addressing block selects appropriate pixels for a proper readout operation. The timing block generates the

Table 2.1: Different pixel structures for the pixel performance tests and their expected NETD values. The pixel in the first line is the one used in the microbolometer FPA designed in the scope of this thesis.

Pixel Pitch	Arm Width	Active area	Expected NETD (K)
70μm	1.0μm	42μm^2	0.276
70μm	0.9μm	42μm^2	0.257
70μm	0.8μm	42μm^2	0.238
70μm	0.7μm	42μm^2	0.220
70μm	0.6μm	42μm^2	0.202
70μm	1.0μm	44μm^2	0.252
70μm	1.0μm	46μm^2	0.230
70μm	1.0μm	47.2μm^2	0.219
35μm	1.0μm	16μm^2	7.130
50μm	1.0μm	31μm^2	0.630

required signals for the readout channels and the addressing block. The programming block allows the chip to be serially programmed.

2.2.1 Reading Algorithm and Addressing

Figure 2.3 shows the FPA scanning scheme of the microbolometer. A readout channel is responsible for two columns of pixels. Therefore, there are $160/2 = 80$ readout channels. The reason for employing one readout channel for two columns of pixels is a readout channel pitch of one pixel width (70 μm) would result impractically long readout channels.

With this readout scheme, the 160x120 FPA practically becomes a 80x240 format. Two counters are used to address the pixels. One is a mod-80 counter and shows which readout channel output is passed to the output pad. The other counter is a mod-240 counter, and it shows which line is being read. The mod-240 counter is increased by 1 when the mod-80 counter completes its one loop. The FPA is read starting from the top left corner.

Counters are not sufficient for selectively biasing the pixels, so shift registers are used for this job. A vertical shift register is selected as a 120-bit shift register. It biases one horizontal line of pixels each time. The reason to be named as ”vertical” is, its orientation in the layout is vertical. The output shift register is a 80-bit shift register. It selects one readout channel output each time. There is also a third shift register, which is the horizontal shift register. It is

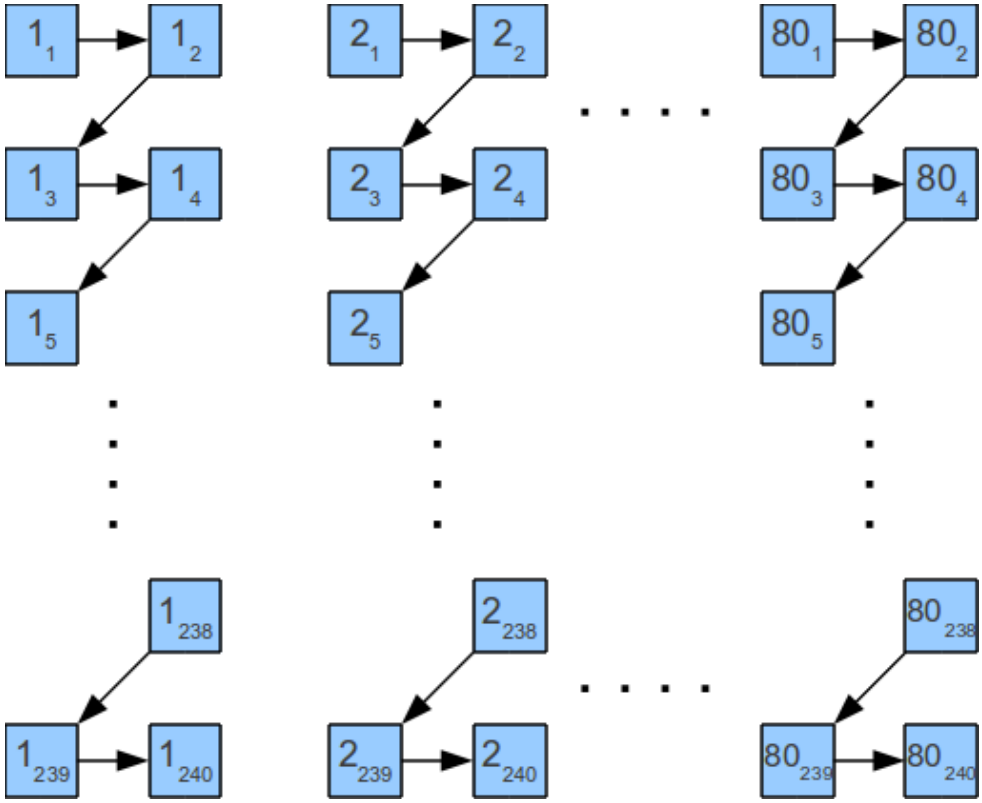

Figure 2.3: The scanning scheme of the microbolometer. The number shows the readout channel number, the index shows the order. m_n means this pixel is read by the readout channel #m in n^{th} turn

a 2-bit shift register that selects the even and odd columns of the FPA. The counter topology, their counting method, and required signaling are described in the previous thesis completed in METU-MEMS Group [11, 16].

2.2.2 Timing Block

The timing block generates the required timing signals for the readout channels and the addressing block. It also generates the output synchronization signals for the external electronics.

The readout timing signals are rst, int_enb and phi. Since they are used for readout channels and readout channels perform the same operation for each line, their period is one line time. They are generated with an RS latch and 2 comparators for Set and Reset. Figure 2.4 shows the block diagram of the readout timing signal generator block. Figure 2.5 shows the

simulation results of the readout timing signals.

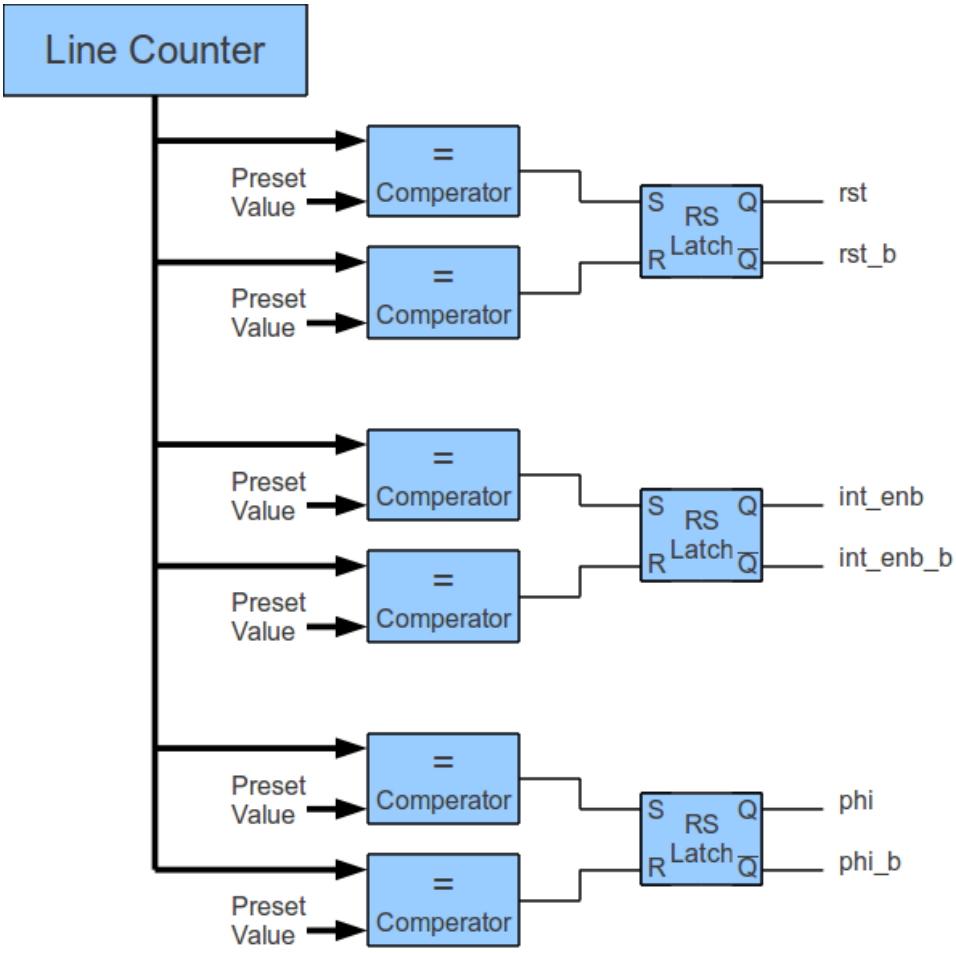

Figure 2.4: Readout timing signal generator block diagram. Bold lines show the bus lines. Each preset value determines when the signal is rising or falling. Their bits are tied to V_{DD} and GND.

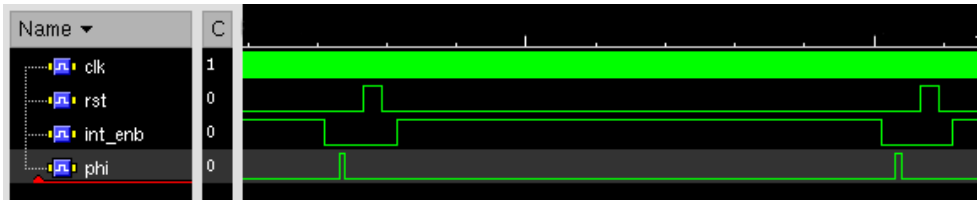

Figure 2.5: Verilog-XL simulation of readout timing signals. One line time is shown in the figure. The periods of these signals is one line time.

There are two synchronization signals named as frame_sync and pixel_sync. Frame_sync

shows the beginning of a frame, pixel_sync shows a new pixel is ready at the analog output. Figure 2.6 shows the simulation results of these two signals. A larger frame_sync pulse prevents the external electronics to miss the start of the new frame [11].

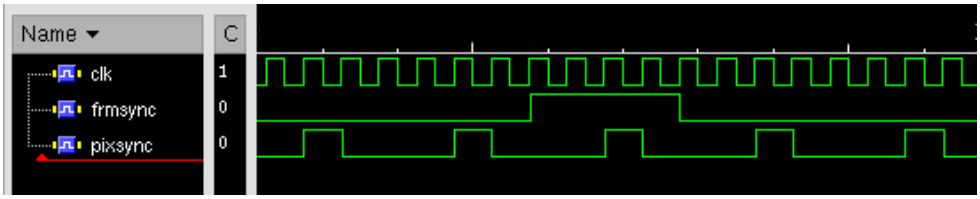

Figure 2.6: Verilog-XL simulations of the frame_sync and the pixel_sync signals of the microbolometer. The pixel_sync pulse when the frame_sync is 1 shows the first pixel of the new frame.

2.2.2.1 Windowing Mode

The designed microbolometer has a windowing mode that changes the active FPA area from 160x120 to 160x60. This allows the microbolometer to double the frame rate, because the number of pixels in a frame is halved whereas one pixel time remains constant. Figure 2.7 shows the active FPN area for windowing mode disabled and enabled. Windowing is achieved by changing the end value of the mod-240 counter to 120 and changing the beginning and end bits of the vertical shift register.

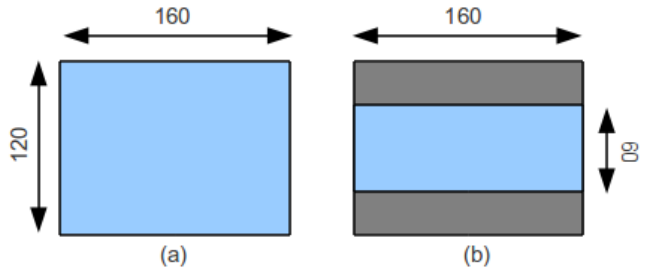

Figure 2.7: Active FPN are and dimensions when windowing mode is disabled (a) and enabled (b). Lines on the arrows show the dimensions in pixels.

Figure 2.8 shows the frame_sync signal and windowing_enable signal (It is named as *narrow_lin* in figure). When windowing_enable signal is high, frame_sync period is halved. This means the frame rate is doubled.

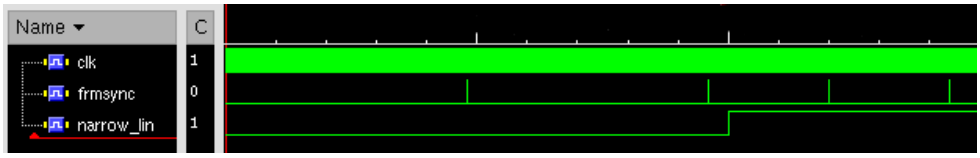

Figure 2.8: Verilog-XL simulation of windowing mode. When the windowing enable signal narrow_lin becomes 1, frame_sync period is halved, because the active FPA area is halved.

The windowing mode decreases the number of pixels in a frame, so one frame is read in a shorter time. This results higher frame-per-seconds(FPS). This allows to capture higher speed objects in a wide window. This feature is very important in microbolometer applications in automotive industries. Because a car travels with a high speed and objects around the car cannot be captured with a low-FPN camera.

2.2.2.2 Clock Detector

During the normal operation, if the clock signal is cut while the power is still supplied to the microbolometer, the same pixels are being hold biased until the clock is fed again, because the shift registers will not advance in the absence of the clock. If a pixel is biased for a long time, its temperature will reach to critical values because the pixels have very good thermal isolation. High temperature will burn the pixels, permanently creating dead-pixel points in the image. To prevent this situation, a clock detector is designed, it detects whether the clock is fed or cut. If the clock is cut, the clock-detector disables the shift-register outputs and claims all the pixels unbiased. Figure 2.9 shows the schematic of the designed clock detector.

Figure 2.10 shows the simulation results of the clock-detector. The operation principle of this circuit is as follows. Clock pulses charge the capacitor. The diode ensures the clock signal only charges the capacitor, not discharges. The capacitor discharges through the resistor but the clock pulses repeatedly charges the capacitor, preventing its output to drop below the input high voltage of the inverter. When the clock is cut, the capacitor discharges through the resistor, and its voltage drops below the critical voltage to switch the inverter. When the inverter gives logic 1, the circuit gives logic 0, and disables the shift register outputs. The whole operation can be bypassed by setting standby_enb_b signal to 1. In this case, the circuit gives logic 1, regardless of the clock presence.

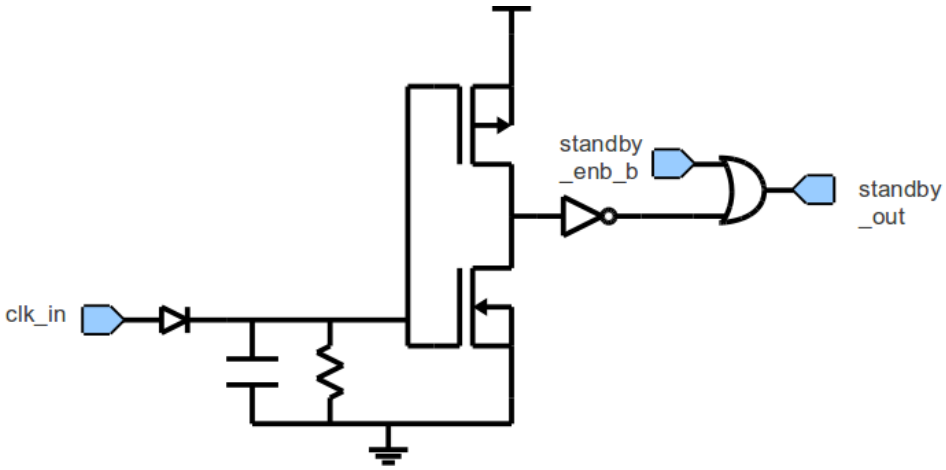

Figure 2.9: Clock detector schematic. The clock signal charges the capacitor. In its absence, capacitor voltage falls below a critical voltage to switch the inverter.

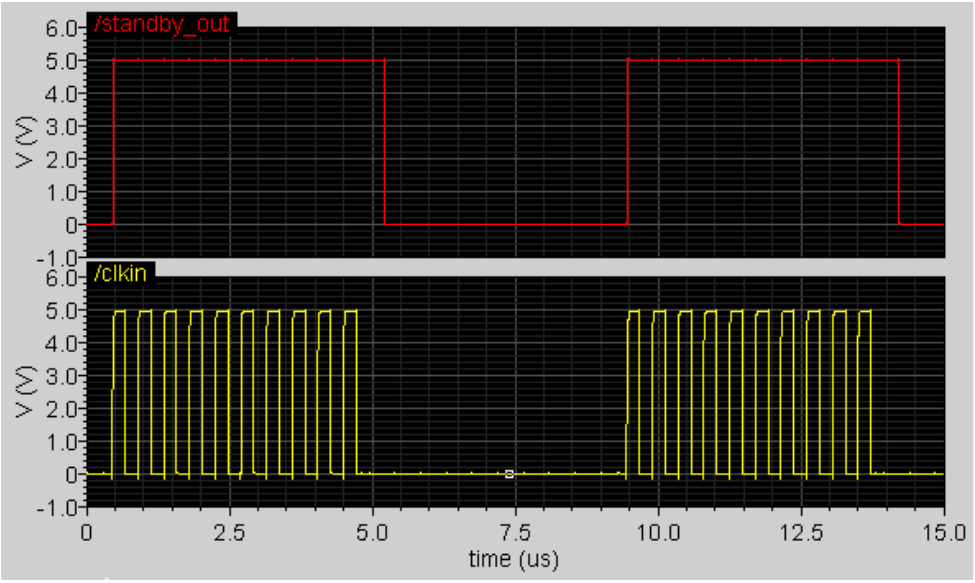

Figure 2.10: Clock detector simulation. When clock is cut, output falls down to logic 0.

2.2.3 Programming Block

The 160x120 microbolometer was designed to have as least number of pads as possible. Therefore, a serial programming block was designed to reduce the pad count. A user can control the internal DACs as well as change the modes of the microbolometer with the pro-

gramming block. The programming block has three main functions: (i) control the inputs of the DACs and digital option bits, (ii) allow a user to change these values, and (iii) perform these functions with the least amount of possible pads. Figure 2.11 shows the block diagram of the programming block. There are 2 main sub-blocks: an SPI module and an internal memory.

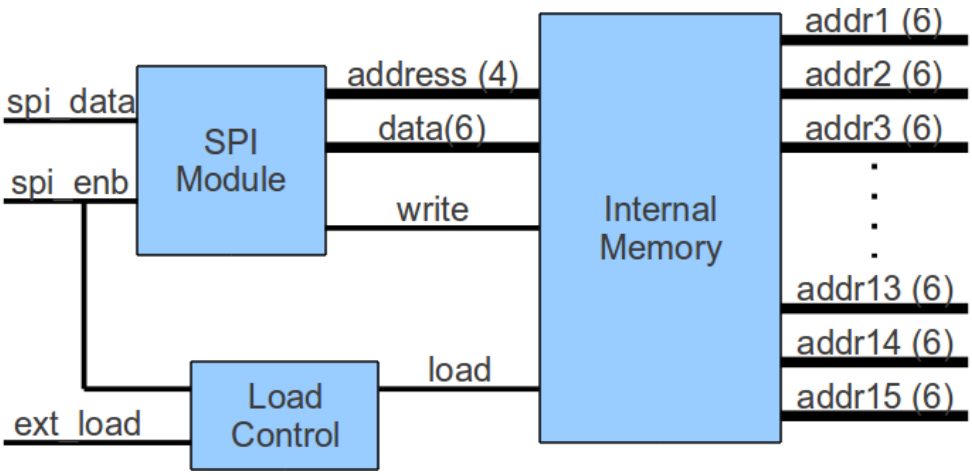

Figure 2.11: Programming block block diagram. 2 main parts are spi module and internal memory. Bold lines represent a bus. Number in parenthesis shows the bus width.

2.2.3.1 SPI Module

SPI is an acronym for Serial Peripheral Interface [23]. A standard SPI bus has 4 wires: SCLK (serial clock), MISO (Master In, Slave Out), MOSI (Master Out, Slave In), and CS (Chip Select, serial enable). The designed microbolometer uses a simplified SPI, and it has 2 dedicated pins instead of 4. For a serial clock, the microbolometer's global clock is used, and MISO pin is omitted because there is no need for the microbolometer to send a data to a master (i.e, FPGA or PC). The two signals are named as spi_data and spi_enb.

Figure 2.12 shows the block diagram of the SPI module. The block does not have any data control mechanisms, unlike todays most of the commercial ICs have such as bit count check [24] to save silicon area. If more than 10 bits of data is send, the first came bits will be discarded. Therefore, the external electronic should ensure the proper communication.

Figure 2.13 shows the SPI signals for receiving $(0010100101)_2$. As seen from the figure, the

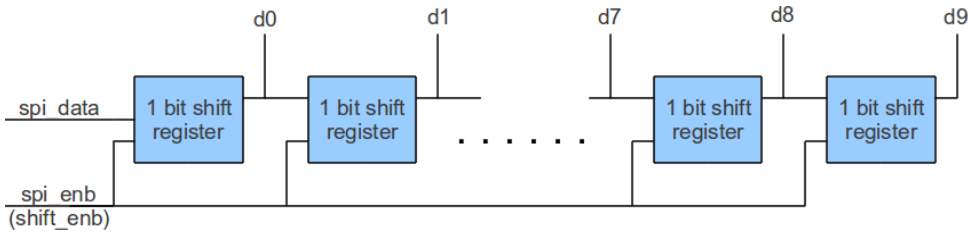

Figure 2.12: Spi module block diagram. There are 10 1-bit shift registers.

clock polarity is rising edge and the enable signal polarity is active-high. Data is sampled on the rising edge of clock if the enable signal is 1.

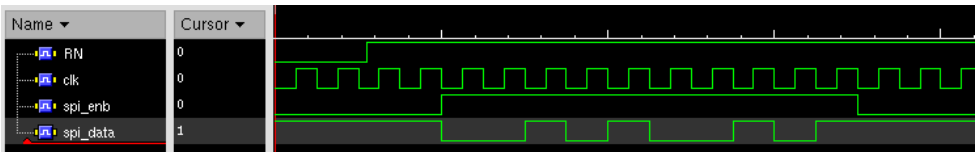

Figure 2.13: Spi module simulation results for receiving $(0010100101)_2$.

2.2.3.2 Internal Memory

The internal memory holds the data for DACs and microbolometer configuration. It is organized as 16x6 bits. The reason to use a 6-bit word length is because the internal DACs have a 6-bit resolution, so each DAC data is defined by one word of the memory. There are 7 DACs, so 7 addresses are reserved for them. Two addresses are used for the microbolometer configuration. Table 2.2 shows the memory address map of the microbolometer. The unused address locations are not implemented in silicon to save the layout area.

The nature of the SPI protocol does not allow more than one address to be updated simultaneously. This is a risky situation where a sequential update of internal DAC voltages may force the readout channels to enter an unrecoverable state, because for some time, some bias voltages will be updated whereas the rest of them will remain in their previous values. To overcome this situation, a buffer memory is used. Data coming from the SPI module is written to a buffer memory first. After a writing operation is completed, contents of the buffer

Table 2.2: Memory map of the designed microbolometer.

	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 0	gm_bias[5:0]					
Address 1	op_bias[5:0]					
Address 2	sink_fine_bias[5:0]					
Address 3	sink_coarse_bias[5:0]					
Address 4	source_fine_bias[5:0]					
Address 5	source_coarse_bias[5:0]					
Address 6	N/C	pix_bias[4:0]				
Address 7	N/C					
Address 8	Standby_enb	N/C	Windowing_enb	cap_sel[2:0]		
Address 9	N/C		Test_out[3:0]			
Address 10	N/C					
Address 11	N/C					
Address 12	N/C					
Address 13	N/C					
Address 14	N/C					
Address 15	N/C					

memory is copied to main memory. This allows the microbolometer to start from a known state. The size of the buffer memory is the same as the internal memory, which is 16x6 bits.

Two events determine when a writing operation is completed. The first event is asserting the beginning-of-frame signal. This signal is generated from the timing block. When this signal is asserted, the memory contents are updated. Figure 2.14 show the simulation results of this event. However, this signal can be masked. If a data transfer takes place (i.e. spi_enb signal is high) no update occurs, even the beginning-of-frame signal is asserted. Figure 2.15 shows the simulation results of this situation.

If multiple address data will be send, the spi_enb signal must go to low at least one clock cycle to complete a transfer of one address data. If the beginning-of-frame signal becomes 1 at this time, the memory will be updated inadvertently. To prevent this situation the spi_enb signal must stay at 0 for at least 4 clock cycles, otherwise the beginning-of-frame signal will be masked. Figure 2.16 shows the simulation results of this situation. The load control unit shown in Figure 2.11 generates the load signal.

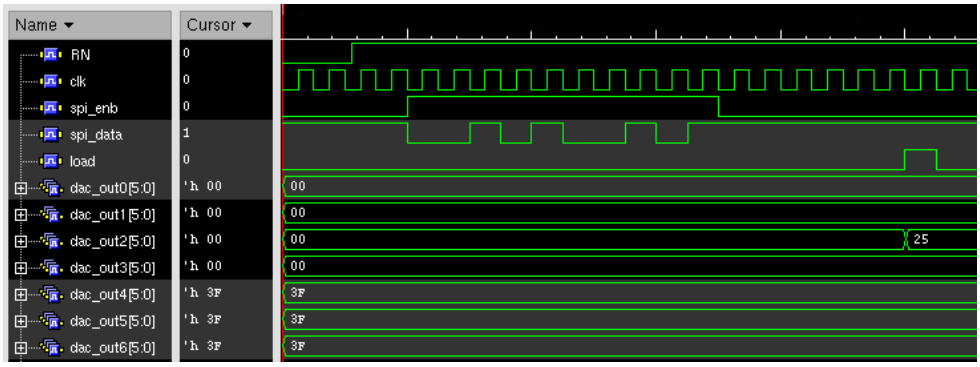

Figure 2.14: Internal memory, normal update. When the load signal is asserted, if the spi_enb signal is low, a memory update takes place.

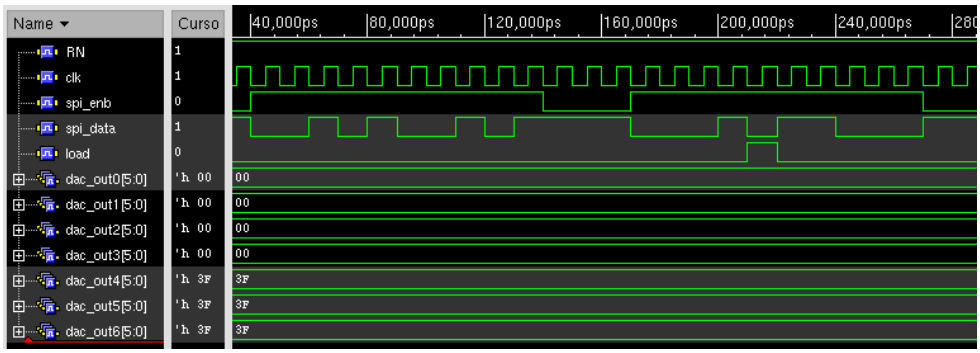

Figure 2.15: Verilog-XL simulation of load masking. The load signal is masked if data transfer occurs. No update takes place.

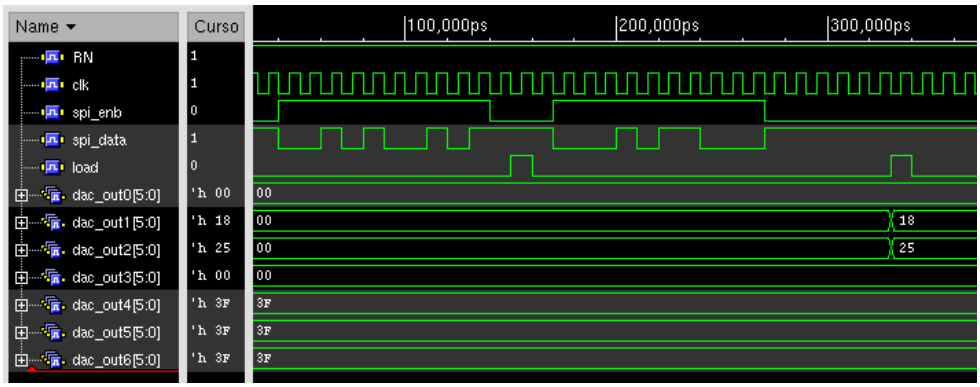

Figure 2.16: Load masking-2 simulation. The load pulse between two spi_enb pulse is masked. The memory is updated at the second load pulse.

2.3 Analog Blocks

The analog blocks in the microbolometer can be grouped as the readout channel and DACs. The readout channel amplifies and conditions the pixel outputs. DACs provide the bias voltages. The readout channel has three stages: a differential transconductance amplifier, a switched capacitor integrator (SCI), and a sample-and-hold circuit (SH).

2.3.1 Differential Transconductance Amplifier

The input stage of the readout channel is a differential transconductance amplifier. It amplifies the reference pixel voltage minus the pixel voltage and gives an output current to the next stage. The designed differential transconductance amplifier is a low-noise, variable gain amplifier with output offset cancellation capability.

Figure 2.17 gives the schematic of the amplifier. A telescopic cascode topology is used. The reason to choose this topology is that it provides a very high output resistance because of the cascode transistors at the output. A high output resistance reduces the noise coming from the next stage, i.e, the switched capacitor integrator [11].

The output of this amplifier is current. The current gain of this circuit is equal to the transconductance values of the input transistors. The transconductances of the input transistors can be adjusted with the bias current. Figure 2.18 shows the simulation results of gain versus frequency when $V_{com} = 1.8V, V_{bp} = 1.2V, V_{bn} = 3.0V, V_{gm\_bias} = 2.0V$. Simulation results show the gain is constant in the frequency range of interest (DC–8kHz).

Noise of the differential transconductance amplifier is critical, because it is the first stage in the readout channel. It should provide a low noise amplification. Therefore, the input transistors are designed to have very large W/L values to decrease the thermal noise as well as WxL values to decrease the flicker noise. The model in the XFAB 1.0 μ SOI process design kit does not have any flicker noise data. Therefore, it is not possible to simulate the real noise of the circuit. The previous trials in METU-MEMS show that increasing the bandwidth to 4 times gives the approximate result [16].

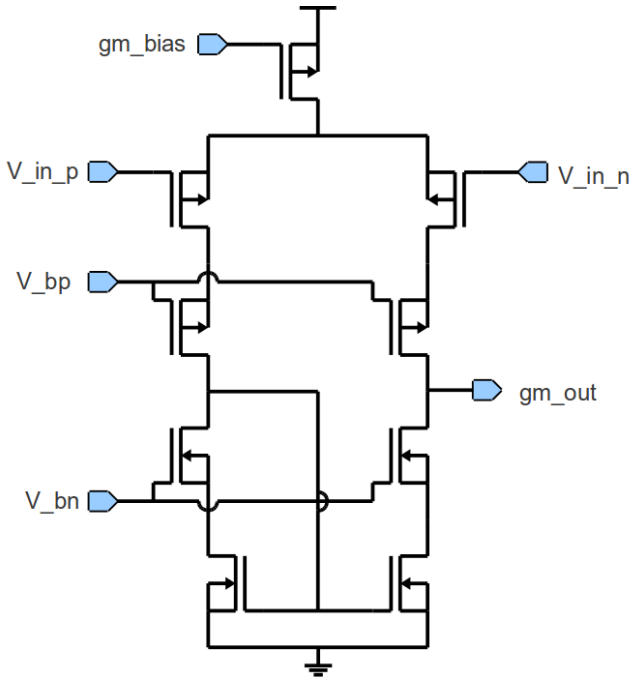

Figure 2.17: The differential transconductance amplifier schematic, where a telescopic cascode topology is used.

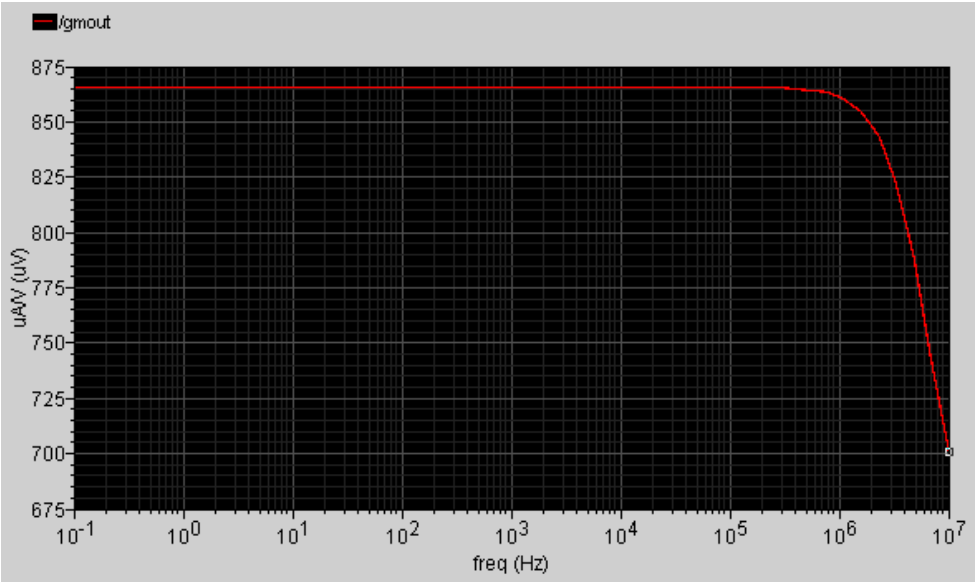

Figure 2.18: The simulation results of the gain of the differential transconductance amplifier. The gain is flat in the region of interest (DC–8kHz).

2.3.1.1 Sink Source Block

The aim of the sink-source block is to remove any offset current caused by process variations.

It is achieved by sinking or sourcing a DC current from or to the differential transconductance

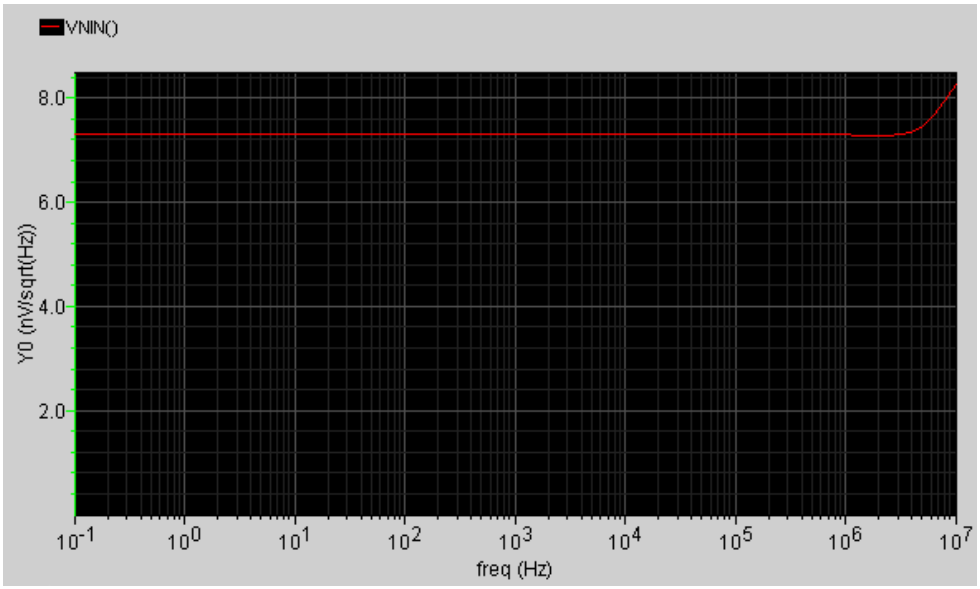

Figure 2.19: The simulation results of the input referred noise of the differential transconductance amplifier. Increase in higher frequencies is caused by lower gain in these frequencies, however, this increment is very low.

amplifier output. Figure 2.20 shows the amplifier with the sink-source block. The reason to use cascode transistors is to reduce the degrading effect on the output resistance of the amplifier.

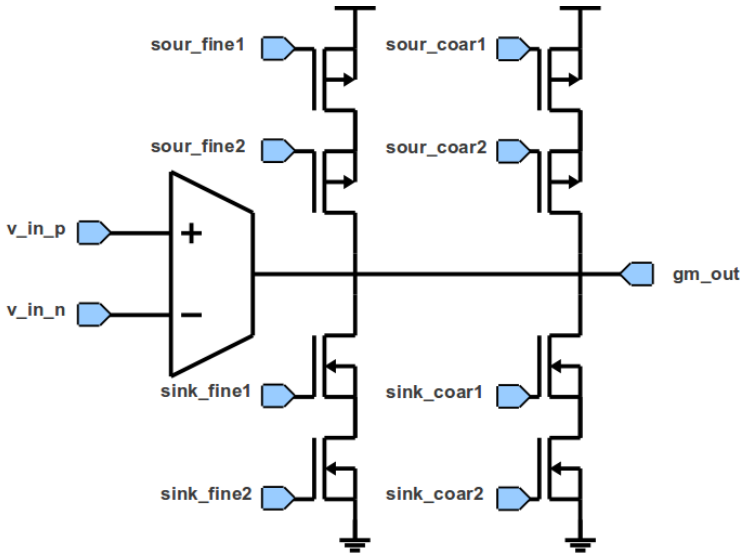

Figure 2.20: Sink-source block schematic.

There are 2 pairs of cascode transistors for both sinking and sourcing. One pair is used for fine adjustment of the DC current, other is used for coarse adjustments. Figure 2.21 shows the simulation results of the introduced DC current of the coarse sink block with increasing bias values, and Figure 2.22 shows the simulation results of the introduced DC current of the fine sink block with increasing DAC input values. The simulation results show that up to 40μA current with a resolution of 40nA can be sinked or sourced.

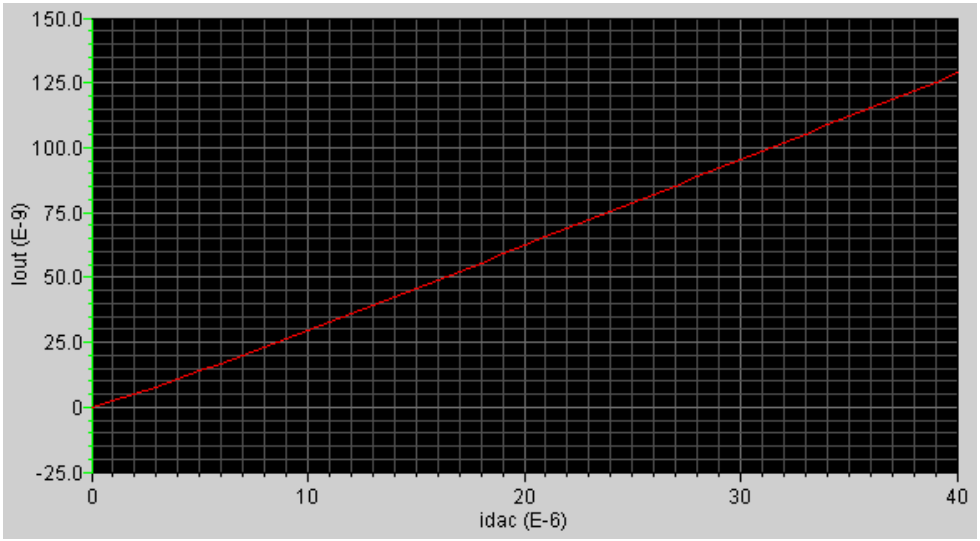

Figure 2.21: Simulation results of the coarse adjustment sink block.

2.3.2 Switched Capacitor Integrator

The next stage in the readout channel is the switched capacitor integrator (SCI) block. The SCI integrates the current from the differential transconductance amplifier on to an integration capacitance. There are two reasons to employ an integrator in the readout channel:

- To amplify the signal to readable levels.
- To limit the bandwidth to reduce the noise.

An integrator limits the bandwidth to $1/2T_{int}$ where T_{int} is the integration time. A narrower bandwidth decreases the noise, however, higher integration time requires larger integration

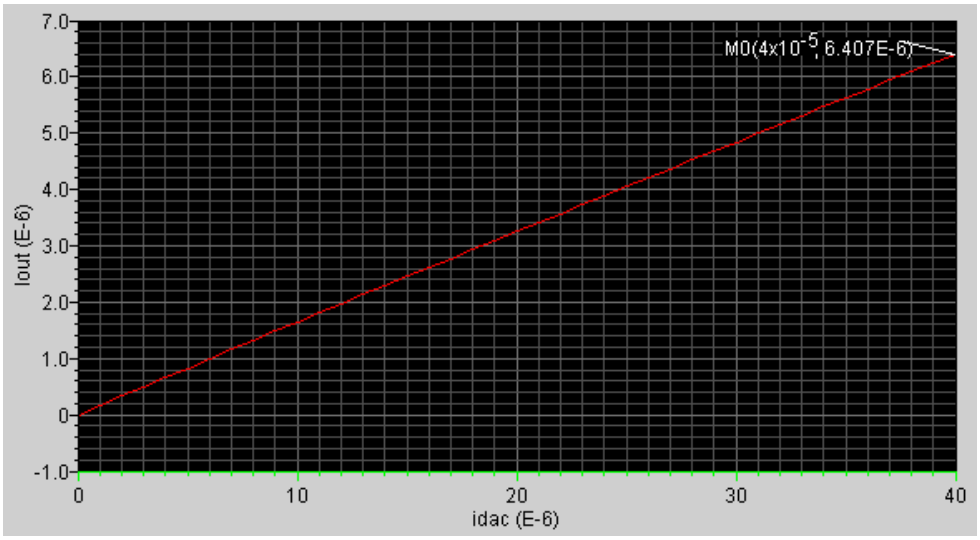

Figure 2.22: Simulation results of the fine adjustment sink block.

capacitances to prevent saturation. High number of readout channels can also be used to increase the integration time but this also increases the chip area.

Figure 2.23 shows the schematic of the switched capacitor integrator. There are 2 digital signals and 2 biases. The operation can be summarized as, first reset the capacitor, then integrate. There are two distinct non-overlapping phases controlled by the two digital timing signals: rst and int_enb. Their timing simulations are given in Figure 2.5.

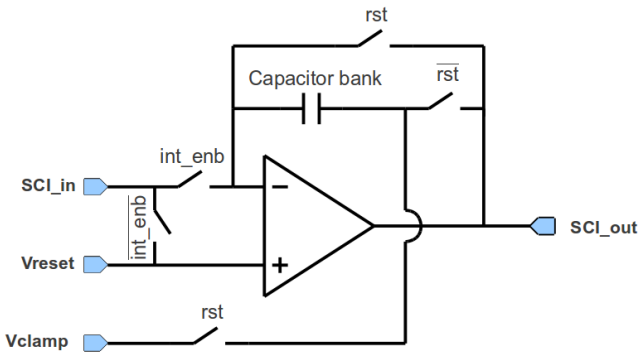

Figure 2.23: The schematic of the switched capacitor integrator block.

Figure 2.24 shows the SCI in a reset phase. In the reset phase, the voltage on the integration capacitance can be written as

$$V_{C_{int}} = V_{clamp} - V_{reset} \tag{2.1}$$

So the capacitor is reset to a known value. The opamp is buffer connected, and the SCI output is equal to V_{reset} during that phase.

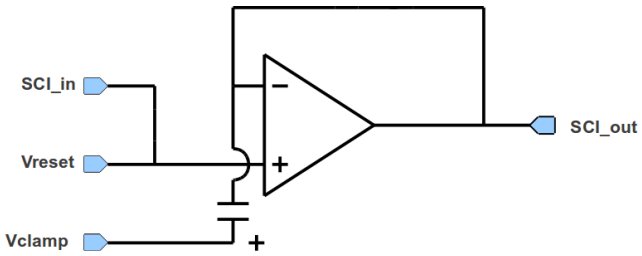

Figure 2.24: The switched capacitor integrator block in a reset phase.

After the rst signal returns to 0 and the int_enb signal becomes 1, the SCI enters the integration phase. Figure 2.25 shows the SCI in the integration phase. During this phase the capacitor voltage can be given as

$$V_c(t) = V_c(t_{init}) + \frac{1}{C_{init}} \int_{t_{init}}^{t} i_{int}(t)dt \tag{2.2}$$

where $V_c(t_{init})$ is the capacitance voltage from the reset state. The output of the SCI is

$$V_{out}(t) = V_c(t) + V_{reset} \tag{2.3}$$

If $V_c(t)$ is replaced with the Equation 2.2 and $V_c(t_{init})$ is replaced with the Equation 2.1, V_{out} can be written as

$$V_{out}(t) = V_{clamp} + \frac{1}{C_{int}} \int_{t_{init}}^{t} i_{int}(t)dt \tag{2.4}$$

Equation 2.4 shows that the integration starts from V_{clamp}, and that V_{reset} has no effect on the output. The main role of V_{clamp} voltage is actually to increase the integration headroom but V_{reset} has an effect on the output voltage. It sets the differential transconductance amplifier output voltage. If the V_{reset} is different from the natural output of the amplifier, an offset current is introduced from the amplifier.

If the input current of the SCI is assumed constant, than the SCI output can be written as

$$V_{out}(t) = V_{clamp} + \frac{1}{C_{int}} T_{int} i_{int} \tag{2.5}$$

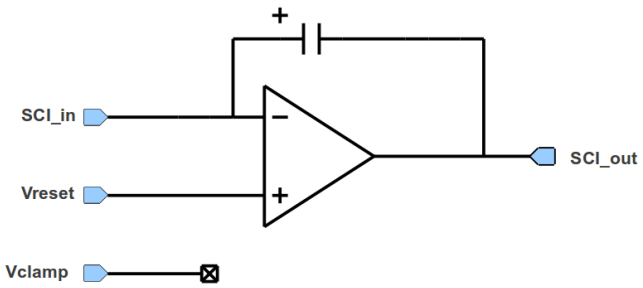

Figure 2.25: The switched capacitor integrator block in an integration phase.

where T_{int} is the integration time. So the output voltage change is

$$\Delta V_{out}(t) = \frac{T_{int}}{C_{int}} i_{int} \tag{2.6}$$

and the gain of the SCI is

$$A = \frac{T_{int}}{C_{int}} \tag{2.7}$$

The integration capacitance can be changed by changing the corresponding data bits in the internal memory as shown in Table 2.2. Table 2.3 shows the capacitance select values, the corresponding integration capacitance values and the resulting SCI gains.

Table 2.3: Capacitor select values and corresponding SCI gains

cap_sel[2:0]	**C_{int}**	**Gain**
000	4 pF	60M V/A
001	8 pF	30M V/A
010	12 pF	20M V/A
011	16 pF	15M V/A
100	20 pF	12M V/A
101	24 pF	10M V/A
110	28 pF	8.57M V/A
111	32 pF	7.5M V/A

The switches and the op-amp used in the SCI is the same switches and op-amp used in previous theses in METU-MEMS [11].

Figure 2.26 shows the simulation results of the SCI block with different input current values. In the simulation V_{reset}=2.1V, V_{clamp}=4.0V and V_{DD}=5V.

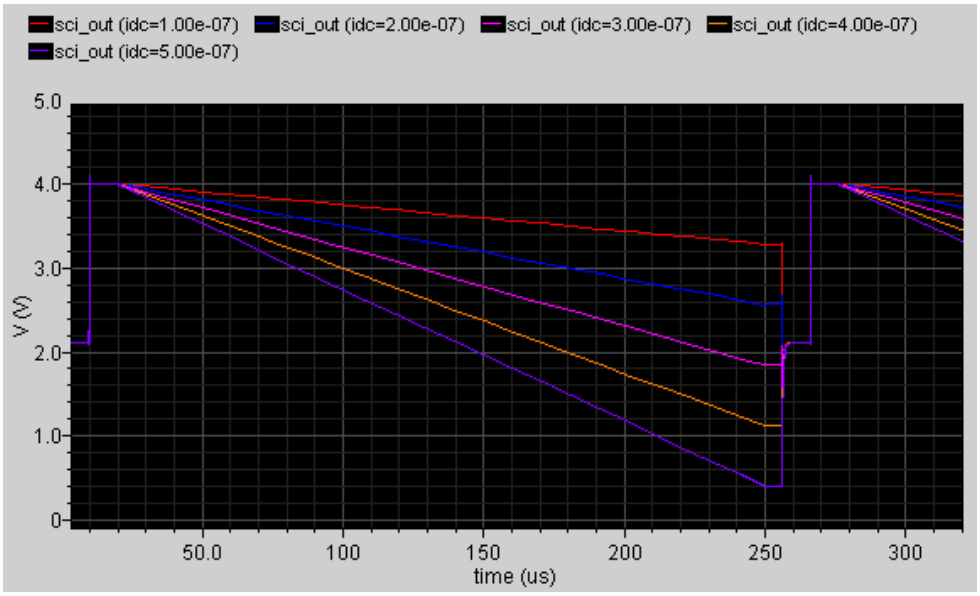

Figure 2.26: The simulation results of the switched capacitor integrator block.

2.3.3 Sample and Hold

The sample-and-hold circuit acts like a one bit analog storage element. It stores the integrator output and allows the rest of the readout channel to begin reading the next pixel. Figure 2.27 shows the sample-and-hold schematic. There is one digital timing signal associated with it: phi. The timing simulation of the phi is shown in Figure 2.5.

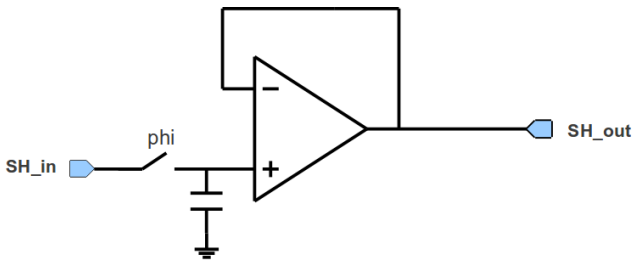

Figure 2.27: The sample-and-hold block schematic.

Figure 2.28 shows the circuit when phi is equal to 1. In this case the input voltage is applied to the sampling capacitance. The opamp is buffer connected and the output is equal to $V_{out} = V_{in}$.

Figure 2.29 shows the circuit when phi is equal to 0; In this case the sampling capacitance

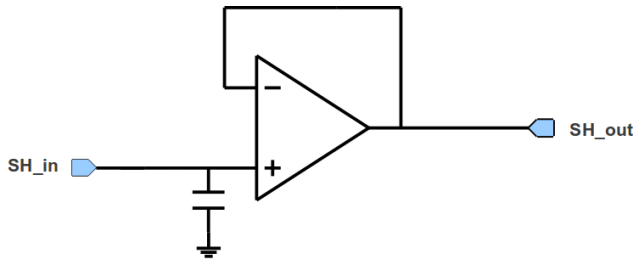

Figure 2.28: The sample-and-hold block in sample phase.

is disconnected from the input, storing the value just before phi is equal to 0. The opamp provides a buffer and prevents any charge to escape from the sampling capacitance. In this situation the output is $V_{out} = V_{cap}$.

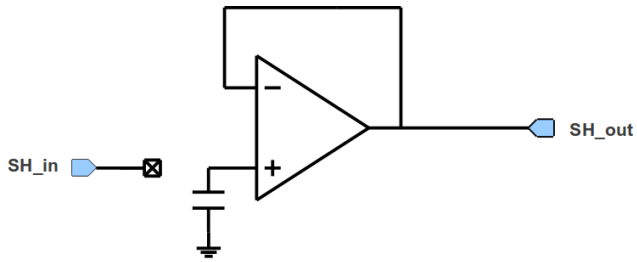

Figure 2.29: The sample-and-hold block in hold phase.

Figure 2.30 shows the simulation results of the sample-and-hold block. Notice during the sample state, the output follows the input.

2.3.4 Current Steering DAC

Internal DACs are used to provide the bias currents required for the readout channels. Two different DACs are designed for current sinking and sourcing. They have the same topology, but they are the complements of each other. Figure 2.31 shows the current sinking DAC and Figure 2.32 shows the current sourcing DAC. Designed DACs have 6 bit resolution with a maximum current of 40 μA. A current mirror is used to scale the current to the required ranges. The reason to choose a large reference current is to reduce the noise of the DACs, since there are only 7 of DACs on a microbolometer chip, their power consumption has very

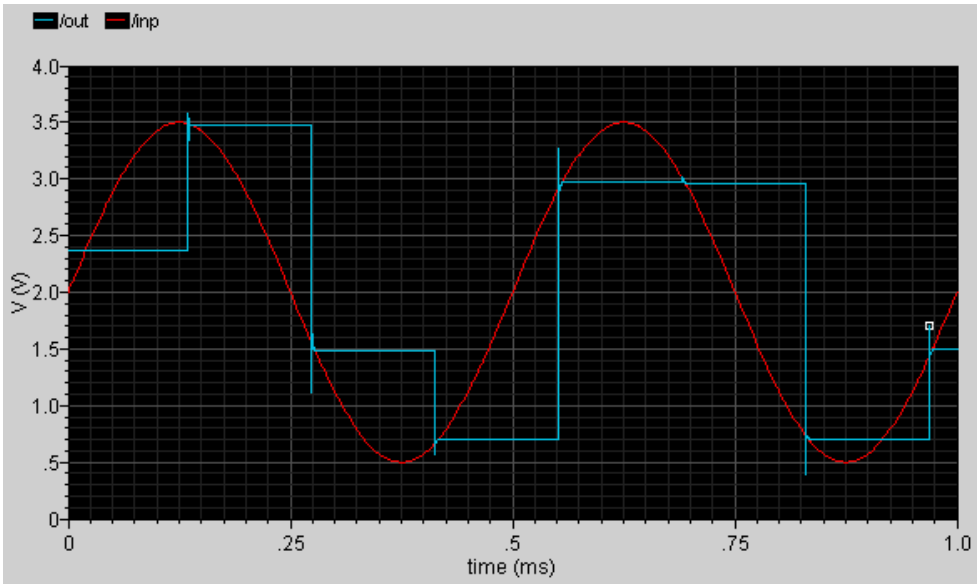

Figure 2.30: Simulation results of sample-and-hold block.

little effect on the overall power consumption of the chip.

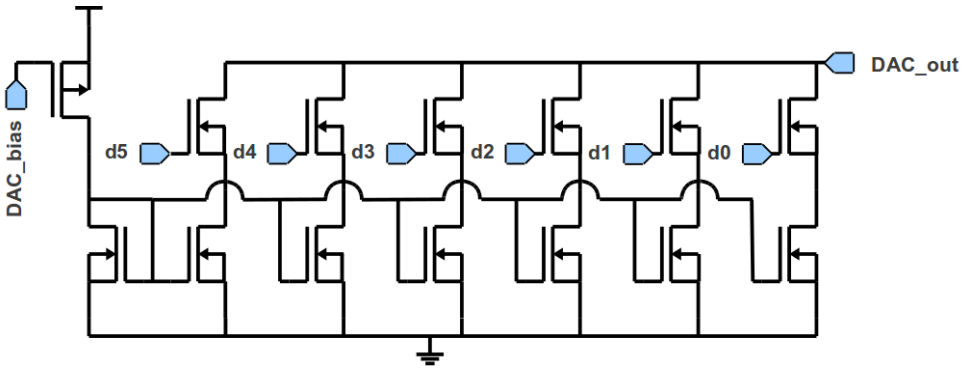

Figure 2.31: Schematic of the current sinking DAC.

There are 7 DACs used in the microbolometer. Table 2.4 shows their purposes. Figure 2.33 shows the simulation result of the current sourcing DAC. Input of the DAC is swept from $(000000)_2$ to $(111111)_2$ and the output is current.

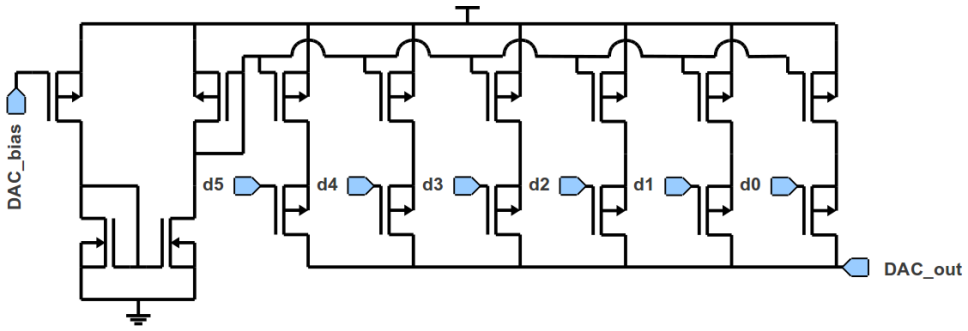

Figure 2.32: Schematic of the current sourcing DAC.

Table 2.4: DACs and their purposes in the microbolometer

DAC Name	Purpose
gm_bias	Adjust the gain of differential transconductance amplifier
op_bias	Adjust the open loop gain of op-amps
pix_bias	Adjust the bias currents of pixels
sink_fine	Adjust the fine sink current
sink_coarse	Adjust the coarse sink current
source_fine	Adjust the fine source current
source_coarse	Adjust the coarse source current

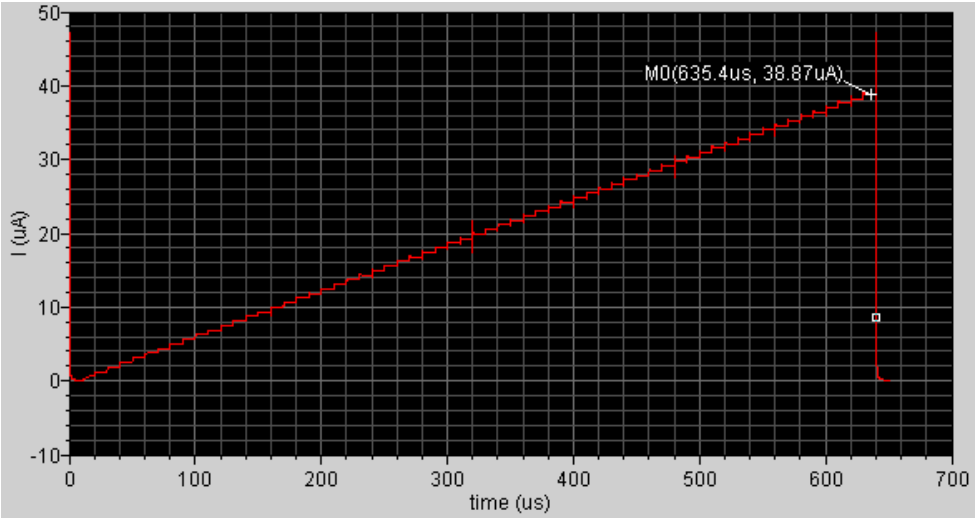

Figure 2.33: Simulation results of the current source DAC.

2.3.5 Readout Channel Architecture

Figure 2.34 shows the block diagram of the readout channel. Under no IR radiation, the constant current biased pixel and reference pixel have the same voltage drop across their terminals, so both terminals of the differential transconductance amplifier are the same, and no current is flowed to the switched capacitor integrator. If there is a mismatch in pixel voltages because of process variations and/or post-CMOS processing, an offset current is generated under no IR radiation. But this current can be canceled by the sink-source block.

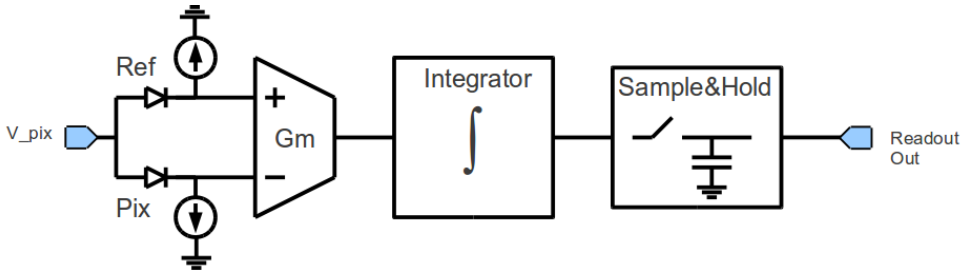

Figure 2.34: Block diagram of the readout channel. The reference and normal pixels are included.

When an IR radiation is absorbed by the pixel, the voltage drop on it is increased, so the voltage on (–) terminal of the differential transconductance amplifier is decreased. This generates a current flowing to the SCI block. The SCI output decreases during the integration. After the integration, the sample-and-hold samples the signal, and the output becomes ready to be read.

2.4 Floorplan and Layout of the Microbolometer

Good floor-planning and layout planning reduce the unwanted coupling of different signals and/or supplies. This reduces the system noise of the microbolometer. Figure 2.35 shows the layout of the designed readout channel. Its width and length are 130μm and 2686μm respectively. With the 10μm spacing between two readout channels, a readout channel covers 140μm width, 2 pixel pitch. The largest part is the differential transconductance amplifier. The input transistors have a W/L ratio of 2730/10 to have a low noise operation.

Figure 2.36 shows the floorplan of the microbolometer. Digital blocks are shown in blue, and

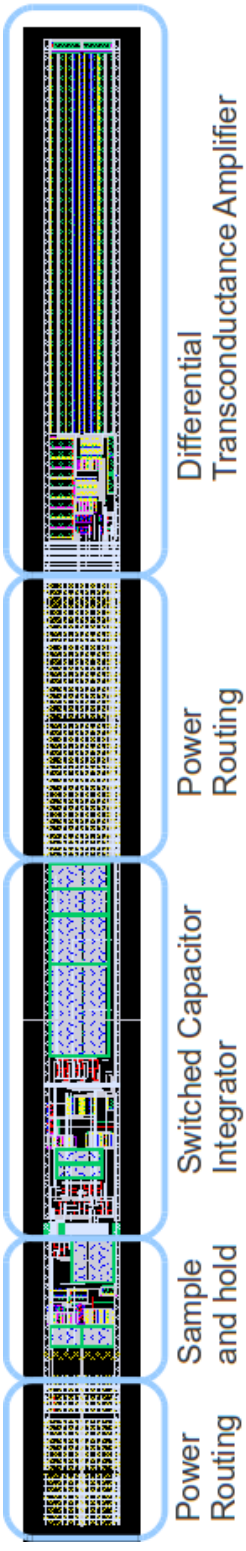

Figure 2.35: Layout of the designed readout channel. It measures 130μm x 2686μm

analog blocks are shown in grey. They are placed as far away as possible to each other. Figure 2.37 shows the top level layout of the microbolometer. The dimensions of the chip are 14.8mm x 14.5mm. There are only 28 pads, all are placed on the top edge of the pad frame. The only test block is a 16x1 multiplexer to observe the internal timing signals. The reason not to place any test blocks to this design is because the previously designed SOI microbolometers in METU-MEMS were succesfully operated [11]. Figure **??** shows the photograph of the fabricated microbolometer with its package. The package is a standard LCC84 package with 0.7 inch^2 cavity.

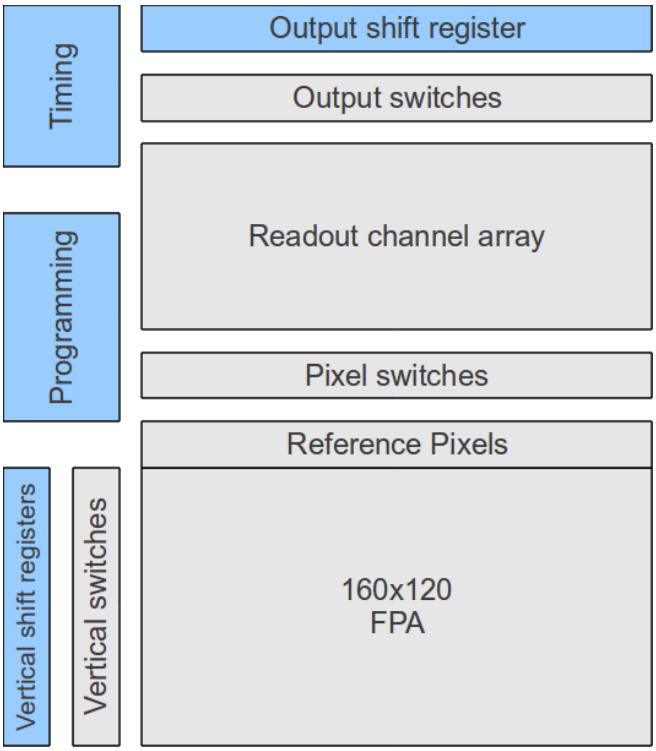

Figure 2.36: Floorplan of the designed microbolometer.

.

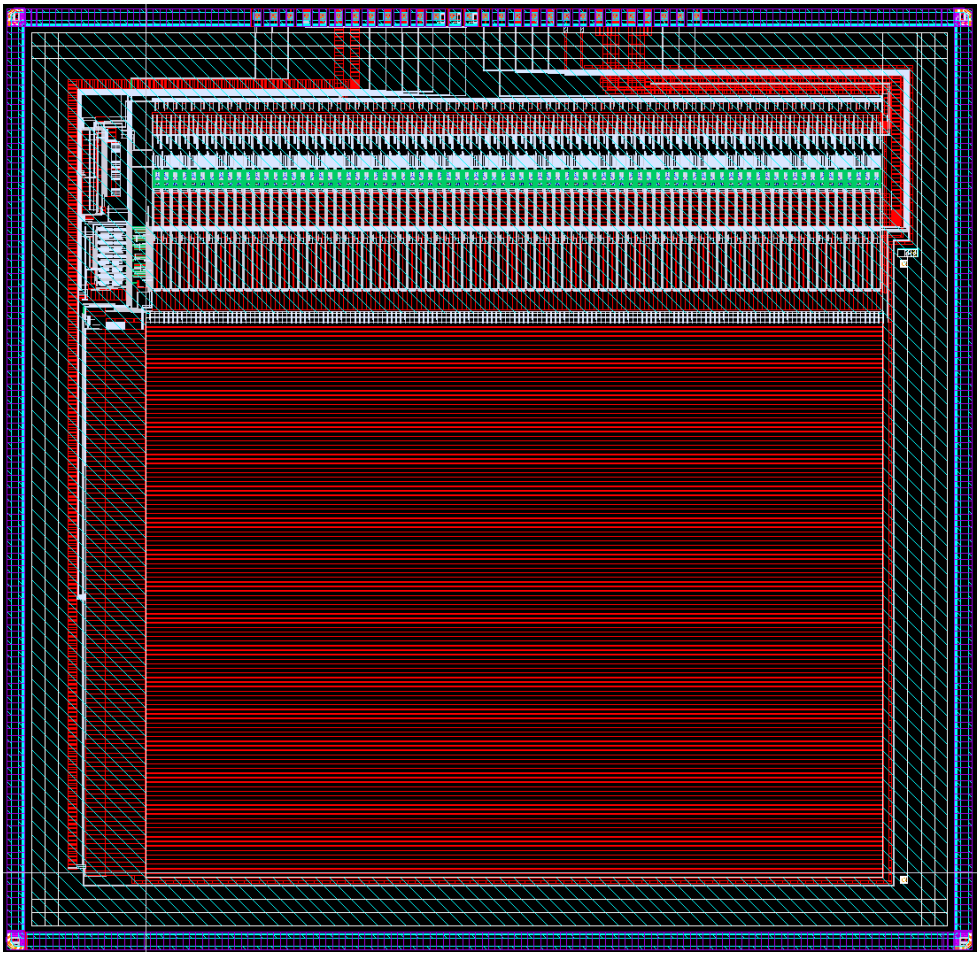

Figure 2.37: Top level layout of the designed and fabricated 160x120 SOI microbolometer. The dimensions of the chip are 14.8mm x 14.5mm.

.

CHAPTER 3

TEST RESULTS OF THE FABRICATED 160X120 LOW-COST MICROBOLOMETERS

This chapter gives the test results of the fabricated 160x120 microbolometer FPA. To determine the functionality and the performance of the fabricated microbolometer FPA, the designed FPA is first send to fabrication in the XFAB 1.0μm SOI-CMOS process. The fabrication is done in a full 6" wafer run, instead of an Multi-Project-Wafer run, as the chip size is large. Figure 3.1 shows the photograph of the 6" wafer, and Figure 3.2 shows a photograph of the individual chip before post-processing. The post-CMOS processing of the FPAs is completed in singulated dies, but wafer level processing is also possible for high volume production. Some of the tests are completed on chips that are not post-CMOS processed, whereas some other tests are completed on post-CMOS processed chips. The chapter is grouped into four sections. Section 3.1 presents the fabricated pixel tests, Section 3.2 shows the test results of digital blocks, Section 3.3 gives the test results of analog blocks, and Section 3.4 gives the details of the post-CMOS process.

3.1 Pixel Tests

The pixel structure used in the 160x120 microbolometer is the same as the pixel structures used in previous thesis at METU-MEMS [11]. However, more detailed noise tests are carried out for this thesis. A statistical noise data is tried to be extracted from many pixel samples. Figure 3.3 shows the block diagram of the noise test setup. A low-noise amplifier with discrete components are used to amplify the pixel noise to readable levels. The amplifier is

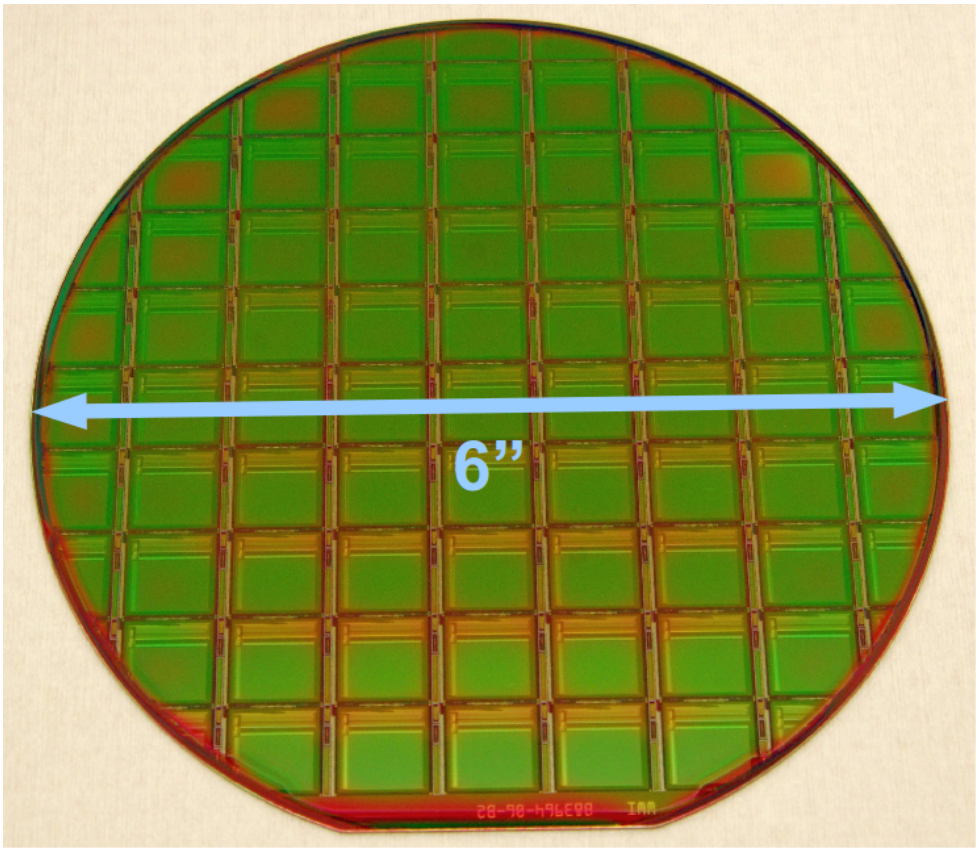

Figure 3.1: Photograph of the full wafer of the fabricated microbolometer FPA.

implemented and characterized at METU-MEMS [20]. It has a gain of 10000V/V in the frequency band of interest. Figure 3.4 shows the photo of the noise setup. The floating ground 3V supply is generated with two alkaline AA batteries. The resistor sets the bias current of the pixel and the offset voltage of the input. The detector is needed to be biased with 8μA, and it has ~3.0V drop on it. So $\frac{3.0V}{8\mu A} = 375k\Omega \simeq 330k\Omega$ resistor is used to set the offset voltage as close to 0 as possible while maintaining the 8μA bias current.

Figure 3.5 shows the test results of the pixels of different die. As seen from the figure, the diode noises are changed abruptly from die-to-die. Also different samples are measured to get a statistical noise data. Different types of pixels in a same die were taken to the test. Figures 3.6, 3.7 and 3.8 show noise measurements of three die. The label *old* shows previously designed pixel structure, the label *all_high shows* the noise of the pixels in which all the gates of the diodes are connected to the highest potential in the detector (Type (a) in Figure 2.2), the

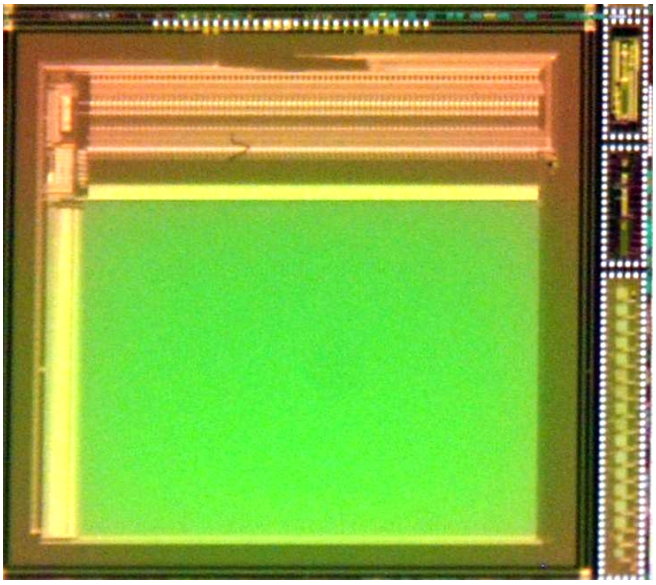

Figure 3.2: Photograph of the single chip before post-CMOS processing.

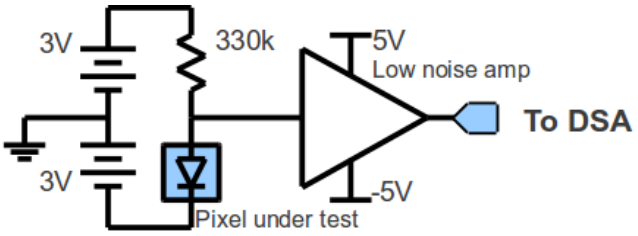

Figure 3.3: Block diagram of the pixel noise measurement test setup.

label *all_low* shows the noise of the pixels in which all the gates of the diodes are connected to the lowest potential in the detector (Type (b) in Figure 2.2), the label *each_drain* shows each gate of the diodes are connected to the higher potential pins of themselves (Type (c) in Figure 2.2), the label *each_source* shows the noise of the pixels in which each gate of the diodes are connected to the lower potential pins of themselves (Type (d) in Figure 2.2) and the label *no_res* shows the noise of the pixels in which these detector structures have metal arms therefore, they have no support arm ressitances. The noise levels of the pixels seem to be randomly distributed, regardless of their gate biasing. Test results claim that there is no relation between gate biasing and noise levels of the pixels.

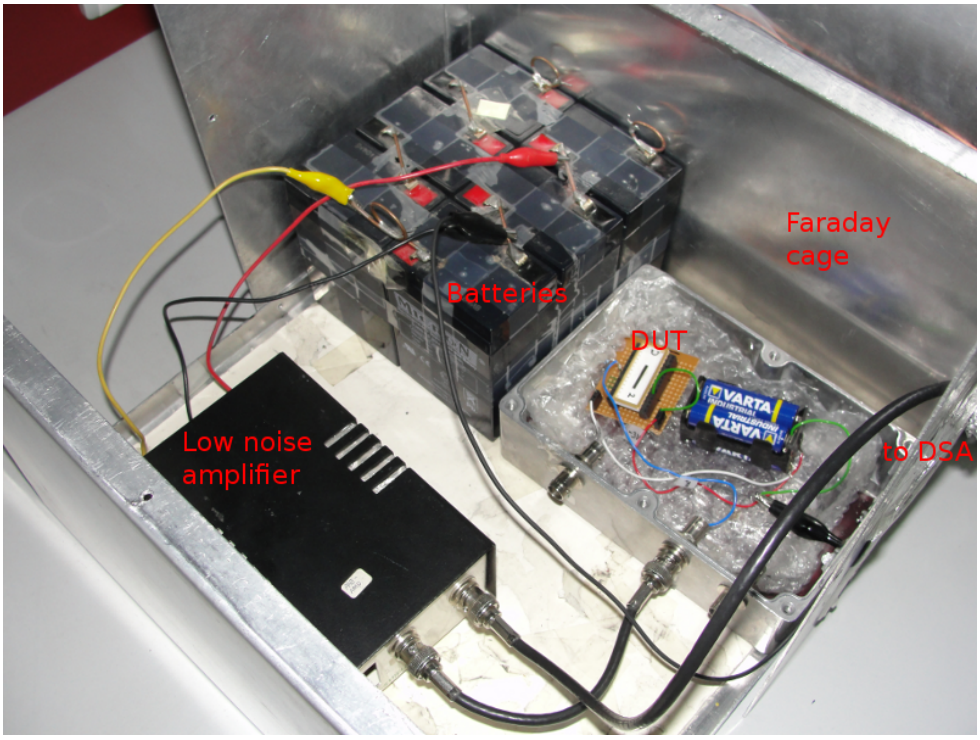

Figure 3.4: Photograph of the pixel noise measurement test setup.

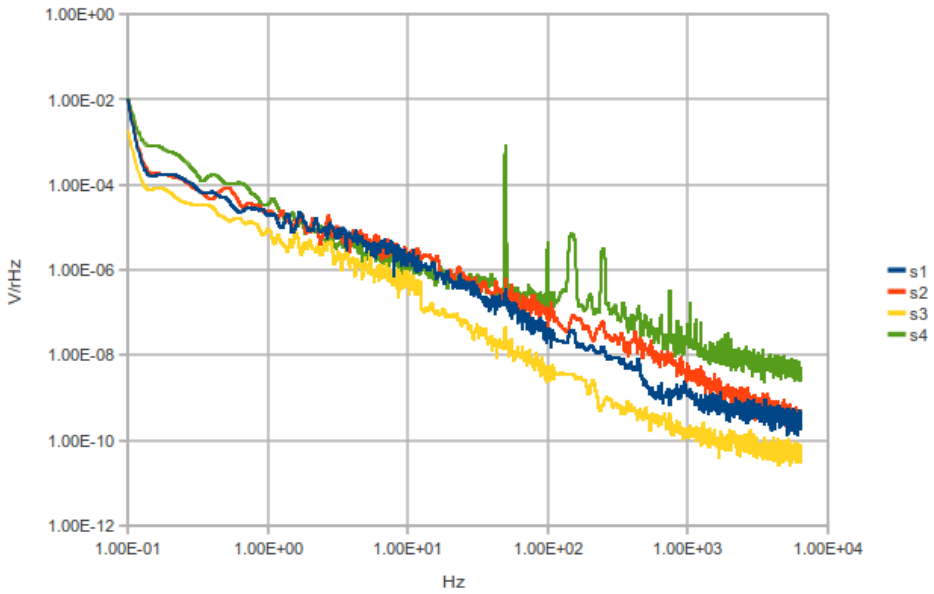

Figure 3.5: Noise levels of individual pixels in different dice. Noise levels distribution is random.

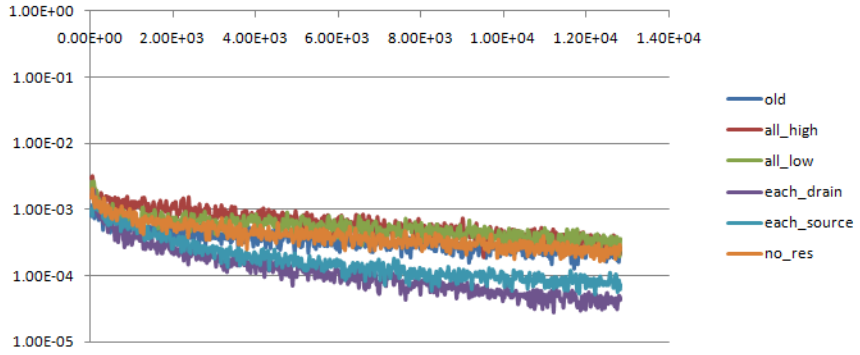

Figure 3.6: Noise levels of different gate biased pixels in a die. In this sample, pixel with individual gates are connected to their high voltage terminals (Type (c) in Figure 2.2) has the lowest noise.

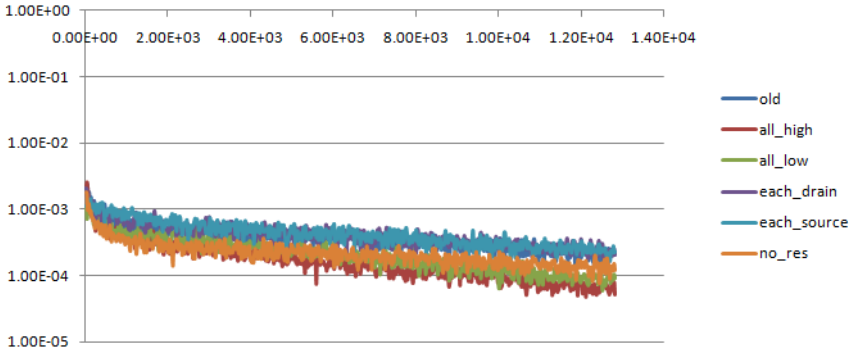

Figure 3.7: Noise levels of different gate biased pixels in a die. In this sample. pixel with all gates are connected to highest voltage (Type (a) in Figure 2.2) has the lowest noise.

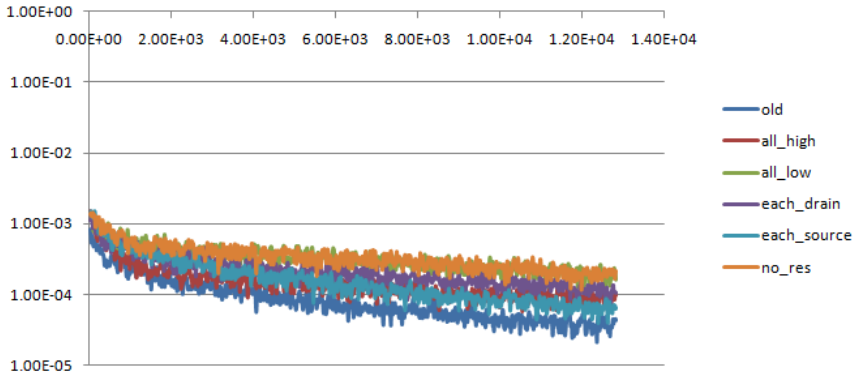

Figure 3.8: Noise levels of different gate biased pixels in a die. In this sample, pixel with floating gates has the lowest noise.

3.2 Digital Blocks Test Results

Critical digital signals are observed and presented in this section. A PGA181 breakout board is used to test the digital signals of the microbolometer. A level shifter is used to increase the output high level of the FPGA to 5V. The FPGA provides clock, reset, and programming signals. Figure 3.9 shows the readout channel timing signals when the clock frequency is 2MHz. The timing signals are generated as expected. Also there are 2 digital signals generated by the microbolometer. Figure 3.10 shows the test results of these synchronization signals. These signals were generated as expected.

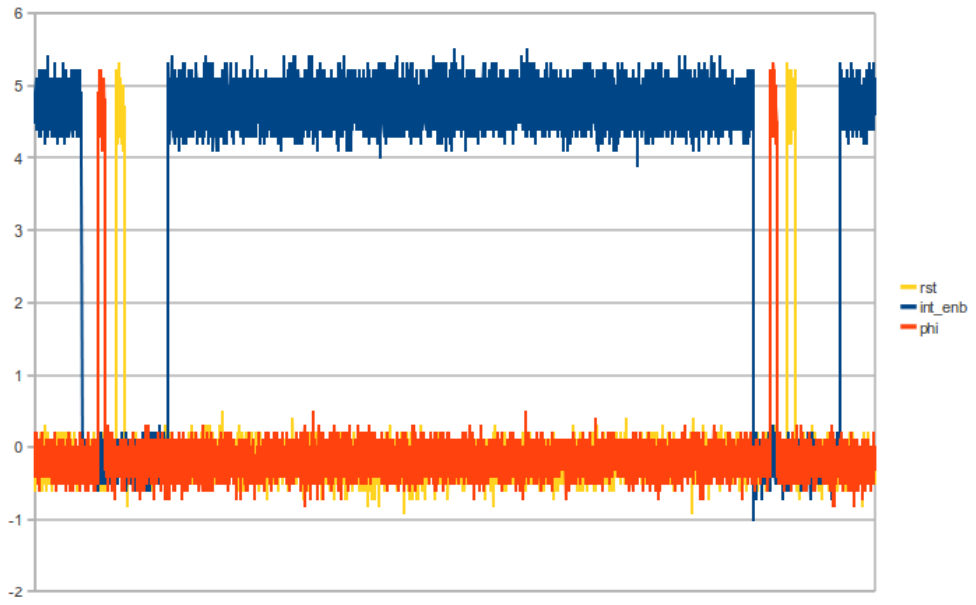

Figure 3.9: Test results of the readout timing signals. These signals are measured from the test output of the microbolometer.

3.3 Analog Blocks Test Results

This section gives the test results of the analog blocks in the developed 160x120 microbolometer. The tested analog blocks are differential transconductance amplifier, switched capacitor circuit, and sample-and-hold block.

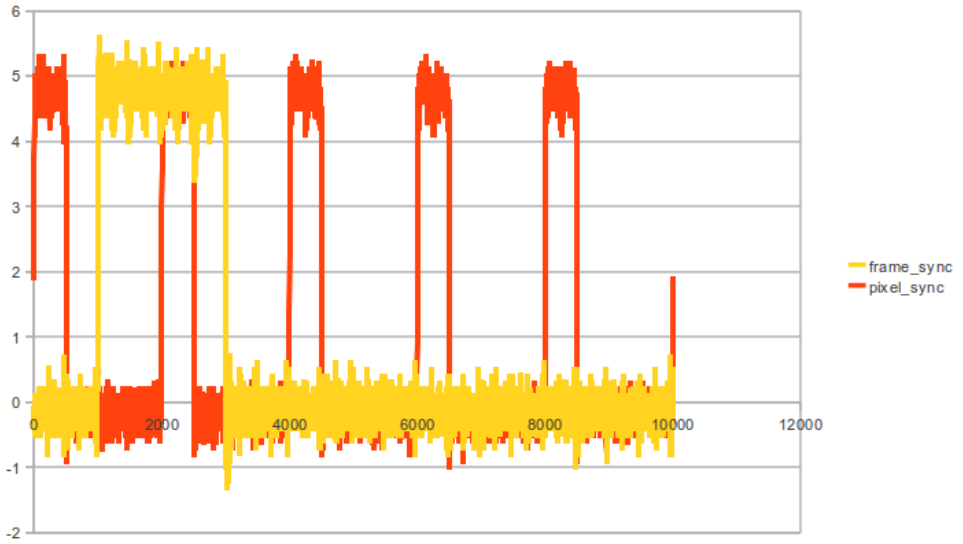

Figure 3.10: Test results of the synchronization signals.

3.3.1 Differential Transconductance Amplifier Test Results

The differential transconductance amplifier is the most important analog block in the read-out channel. Its linearity, gain characteristics, and noise performance should be known to estimate the overall performance of the microbolometer. To test the linearity and ac gain of the amplifier, the PCB shown in Figure 3.11 is used. Same PCB is used for the SCI and the sample-and-hold tests also.

To test the linearity of the amplifier, the schematic in Figure 3.12 is built. A current source creates a small voltage difference on the input terminals of the amplifier, and a voltage source sets the common mode voltage of the inputs. The output current is converted to a voltage by the transresistance amplifier. The gain of the transresistance amplifier is equal to the feedback resistance value. In the tests, 220kΩ resistor is used. Figure 3.13 shows the output current versus the input voltage of the amplifier. The slope at the origin is 905 μA/V. The amplifier output is linear for the input voltages between -50mV – 50mV. In this test the voltages are set as follows: $V_{com} = 1.8V$, $V_{bp} = 1.2V$, $V_{bn} = 3.0V$, $V_{gm\_bias} = 2.0V$, and $V_{out\_bias} = 2.1V$.

The test circuit shown in Figure 3.14 is used to measure the frequency gain of the amplifier. The function of the transresistance amplifier is the same as in linearity tests,i.e., to convert the

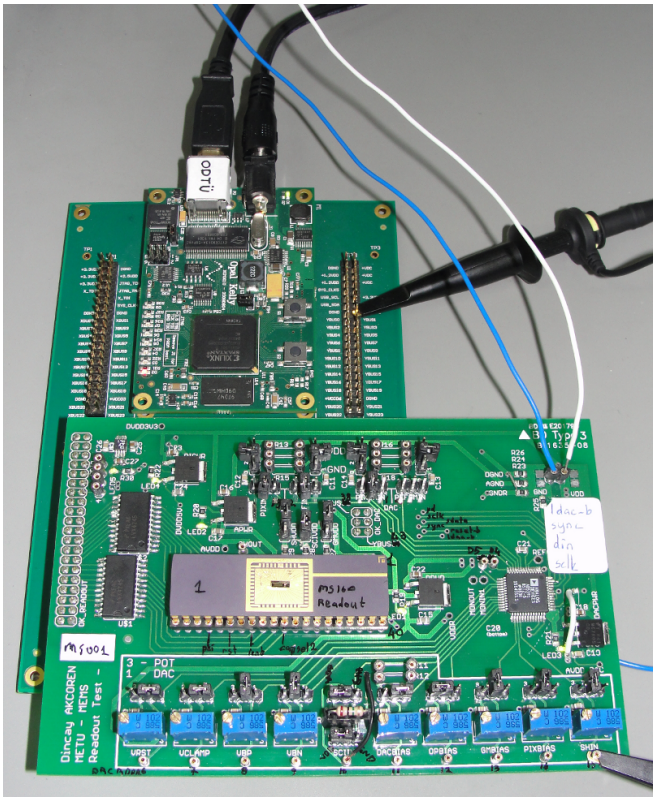

Figure 3.11: PCB used for most of the readout channel tests. Jumpers allow the user to select appropriate operation modes. Potentiometers and DAC allow the user to provide bias voltages to the DUT(Device Under Test).

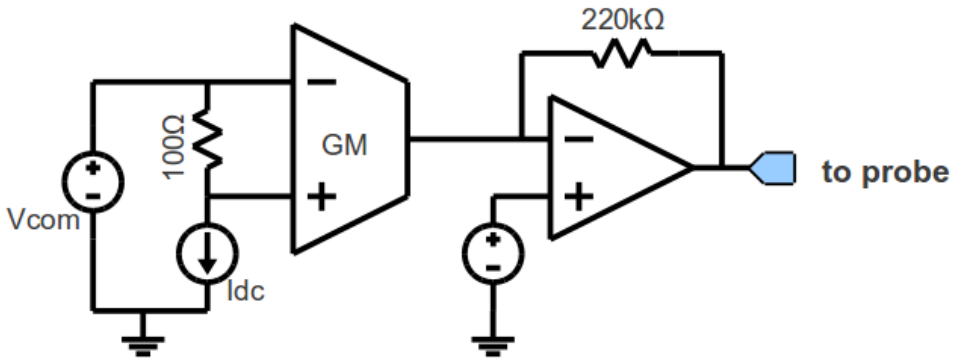

Figure 3.12: Test circuit for the differential transconductance amplifier linearity measurement.

current to voltage and amplify it to readable levels. This time the gain of the transresistance amplifier is 1000V/A. Figure 3.15 shows the test results of the amplifier. The gain is 900μA/V which is very close to the simulation results of 865μA/V. The gain is flat in the band of 0.1Hz–40kHz.

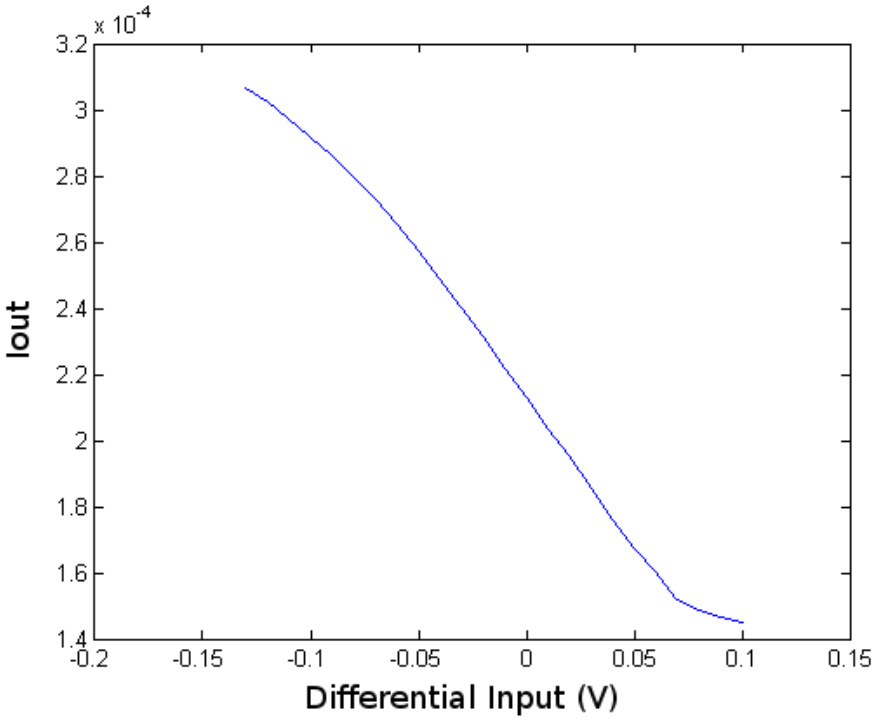

Figure 3.13: Test results of the differential transconductance amplifier. The amplifier output is linear for the input voltages between -50mV – 50mV.

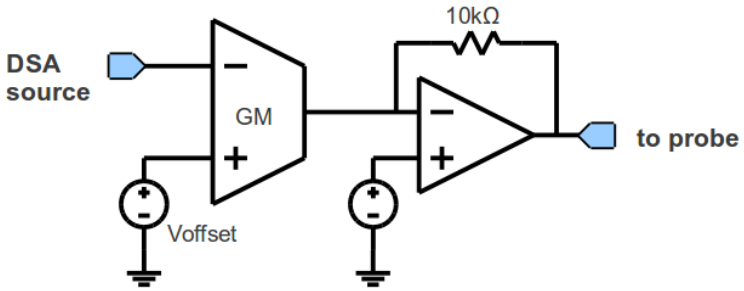

Figure 3.14: Test circuit for the differential transconductance amplifier gain measurement.

3.3.2 Switched Capacitor Integrator Test Results

The switched capacitor integrator (SCI) integrates the input current using a capacitor. A 5.6 MΩ resistor is connected between V_{DD} and the input that acts as a current source. The bias

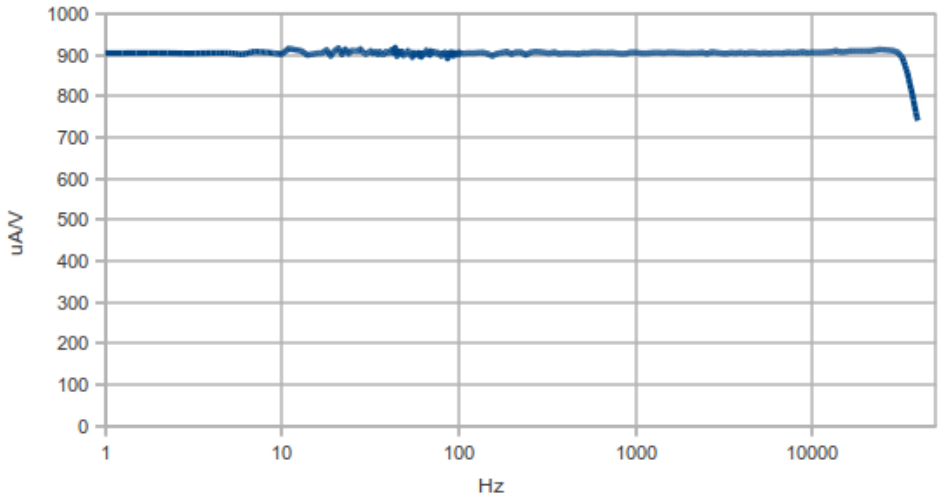

Figure 3.15: Test results of the differential transconductance amplifier. The gain is 900μA/V in the frequency band of 0.1Hz–40kHz.

levels during the tests are $V_{reset} = 2V$ and $V_{clamp} = 4V$. The input current is

$$I_{int} = \frac{5V - 2V}{5.6M\Omega} = 0.53\mu A \tag{3.1}$$

That much current is collected on the 32 pF capacitor for 240 μsec. This makes 3.8V output change according to Equation 2.6. Figure 3.16 shows the oscilloscope output of the SCI block. The measured output change is 3.65 V. V_{reset} and V_{clamp} voltage values can be seen on the figure. The small step just before the beginning of integration is V_{reset} voltage and the starting voltage of the integration is V_{clamp} voltage. So according to the measurements results, the SCI block operates as expected.

3.3.3 Sample-and-Hold Test Results

The sample-and-hold block in the circuit holds the integrator output and stores it for a line time. Figure 3.17 shows the oscilloscope screen. The purple signal is *phi*, the sample signal for the sample-and-hold, the green signal is a sinusoidal with V_{pp}=3V and a mean of 2V, and the yellow is the sample-and-hold output. Measurement results show that the sample-and-hold block operates as expected.

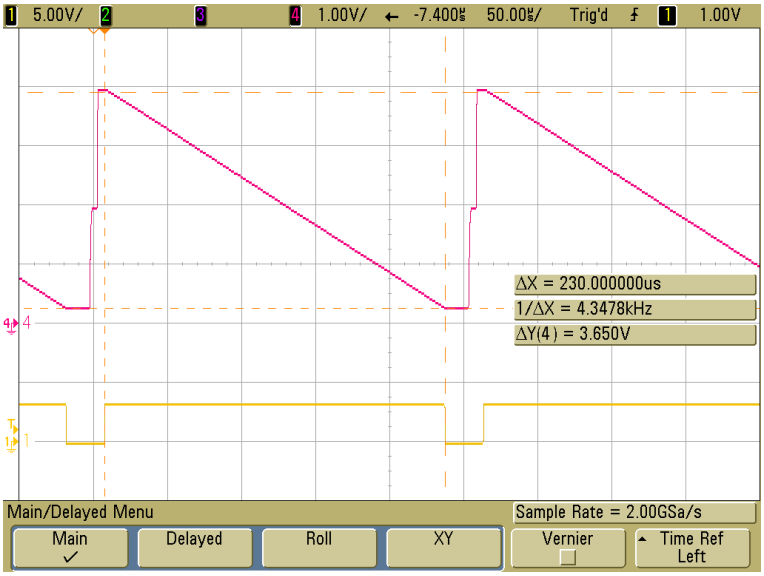

Figure 3.16: Test results of the SCI block.

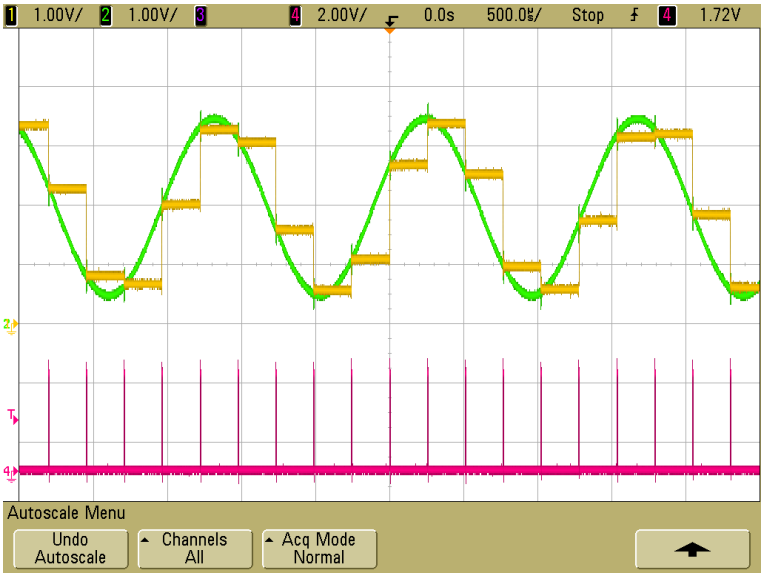

Figure 3.17: Test results of the sample-and-hold block. The block can successfully store signals between 0.5-3.5V.

3.4 Post-CMOS Process

The post-CMOS process steps of the 160x120 SOI microbolometer studied in the framework of this thesis are performed in the METU-MET facility. All the process steps are completed

and suspended chips are developed by Mr. Orhan Akar. The chips are processed and suspended at the die level rather than at the wafer level due to the limited number of wafers available, but the process can be easily applied to wafer level. Figure 3.18 show the fabricated test pixels. Figure 3.19 shows the picture of a part of the 160x120 SOI microbolometer FPA before any post-CMOS processing. Figure 3.20 shows the picture of a part of the 160x120 SOI microbolometer FPA after all the post-CMOS processes are completed. Both the reference and array pixels are given in the figure. Figure 3.21 shows the SEM photographs of both the array and the reference pixels after all the post-CMOS processes are completed, and also shows a part of the FPA where some of the pixels were removed to observe the anisotropic etching underneath the pixels.

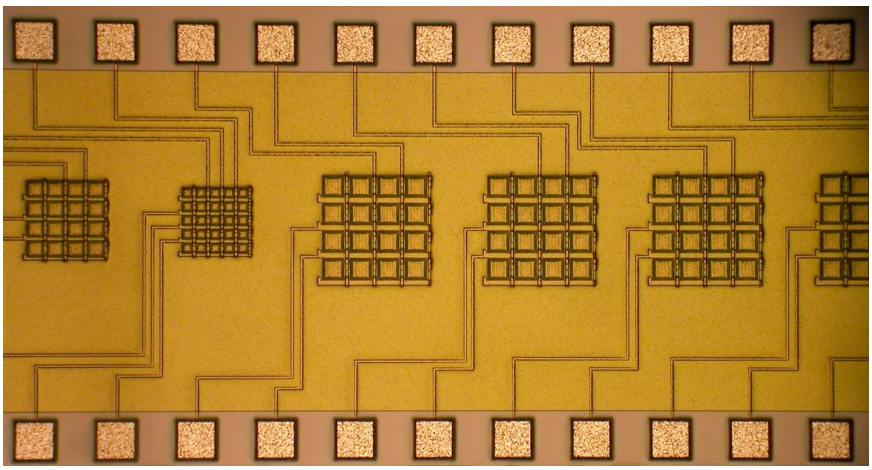

Figure 3.18: Picture showing the part of the fabricated test pixels. The set of 50μm pixel pitch, 35μm pixel pitch, and the set of pixels with different poly arm width can beseen in the figure.

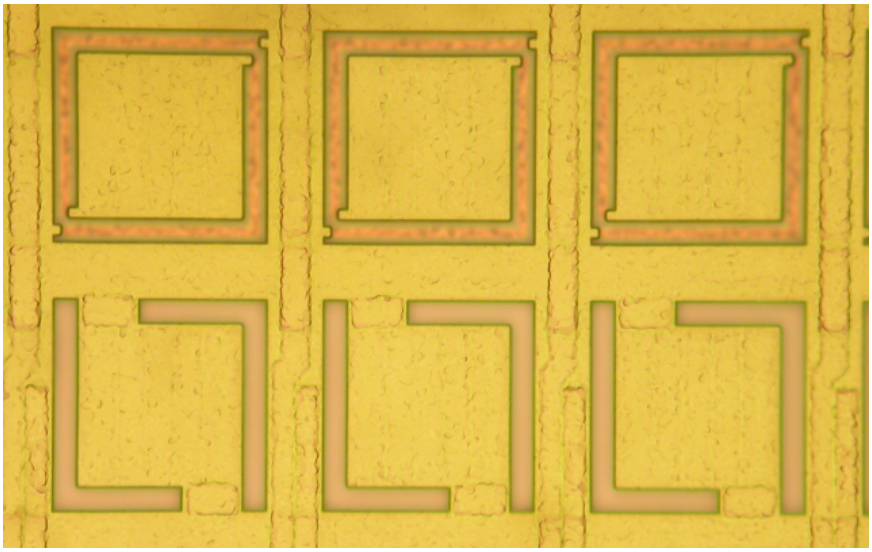

Figure 3.19: Picture showing the part of the 160x120 SOI microbolometer FPA before any the post-CMOS process.

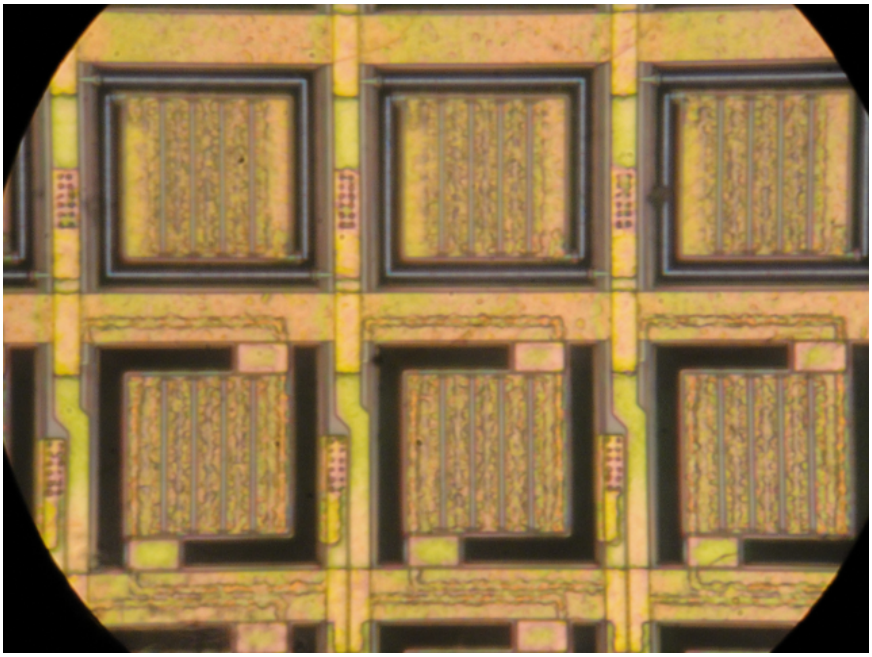

Figure 3.20: Picture showing the part of the 160x120 SOI microbolometer FPA after all the post-CMOS processes are completed. Both of the array pixels (upper row) and reference pixels (lower row) can be seen in the figure.

.

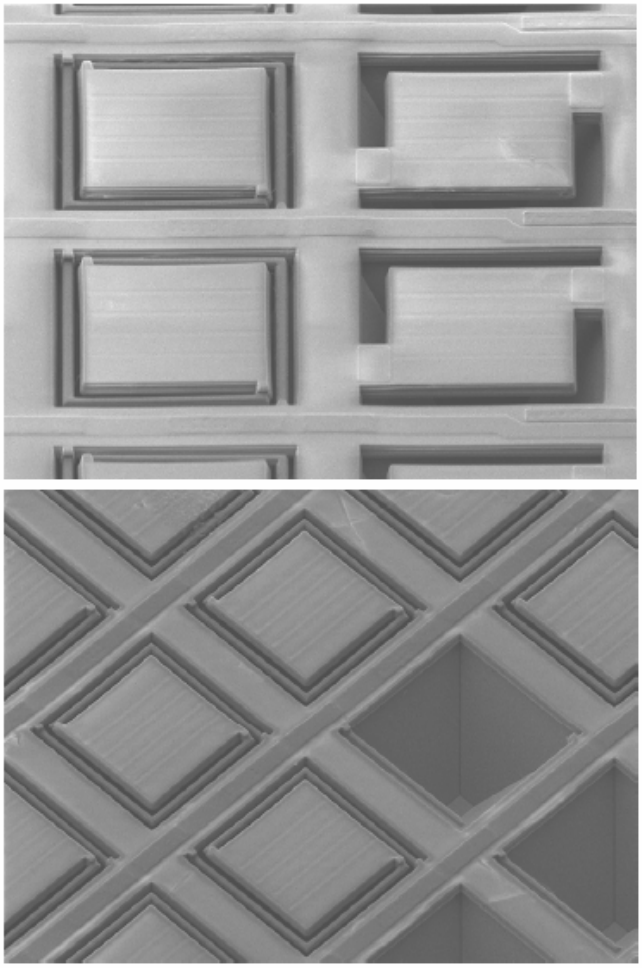

Figure 3.21: SEM pictures of both the array and the reference pixels after all the post-CMOS processes are completed.

.

CHAPTER 4

CAMERA ELECTRONICS

This chapter gives detailed information about the designed camera electronics for low-cost IR microbolometers developed at METU-MEMS. The camera electronics include external signal biasing, and microbolometer data processing. One purpose of the camera electronics is to provide appropriate signaling such as low-noise references, supply voltages and digital signals for programming. Another purpose of the camera electronics is to successfully read the microbolometer outputs and to process them in both hardware and software. The developed camera electronics should be low-noise, such that the overall system will be limited by the pixel and/or readout noise.

4.1 Camera Electronics for 128x128 Low-Cost Microbolometer

This section explains the developed camera electronics for the 128x128 SOI microbolometer which was developed in the framework of the previous study at METU on low-cost microbolometers [11].

4.1.1 Signal Biasing

The 128x128 microbolometer requires 9 external analog bias voltages and 13 external digital option bits. A DAC and an FPGA is used in this part. The analog biases are generated with a multichannel DAC. The employed DAC has 16 channels with 12 bit resolution with an output voltage span of 0–5 V [24]. The DAC is programmed by the FPGA. Although DAC is operating with a 5V supply, its digital inputs have V_{IH}=2V, so the FPGA can directly program it.

The communication between the FPGA and the DAC is done with the SPI protocol. Digital option pins set the operation modes of the microbolometer. The FPGA directly controls these inputs. The microbolometer operates with a 5V digital supply. V_{IH} value of the microbolometer is $V_{DD} - V_{TP} \simeq 3.8V$ [25]. So the FPGA cannot be used without a level shifter circuit. A 5V buffer with an $V_{IH} < 3.3V$ is used between the FPGA and the microbolometer [28]. Figure 4.1 shows the block diagram of the signal biasing part of the external electronics. The FPGA-PC communication will be explained in the following section.

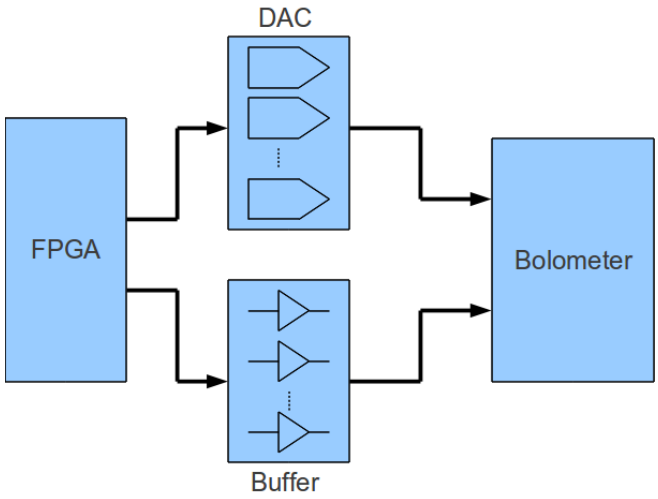

Figure 4.1: Block diagram of the signal biasing block.

4.1.2 Output Processing

The output processing part is responsible about everything between from succesfully receiving the microbolometer pixel data to final image formation. Figure 4.2 shows block diagram of the output processing part.

4.1.2.1 Output Processing Hardware

The 128x128 microbolometer has one channel analog output. In order to transfer it to a PC and form an image, this data should be converted to digital by using an ADC. Another benefit of digital conversion is to prevent any external noise to couple with the microbolometer

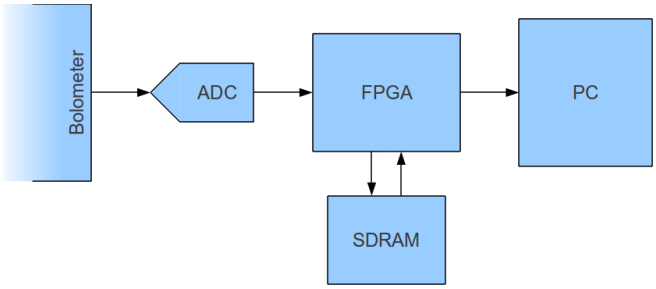

Figure 4.2: Block diagram of the output processing block.

output. Therefore, data is coverted to digital just after the microbolometer output pad. The employed ADC has 14 bit resolution with a 0–5V_{PP} input range and has a speed of 10 MSPS [26]. It has parallel outputs and needs an external clock to operate. The ADC clock is generated by the FPGA. The microbolometer pixel_sync signal can be used for the ADC clock but, microbolometer state is changed at the rising edge of the pix_sync, and glitches may occur on the analog output. Therefore, the ADC should sample the analog signal some time after the rising edge of the pixel_sync. The ADC clock has the same frequency but the rising edge is delayed a bit. Figure 4.3 shows the ADC clock with the pixel_sync signal.

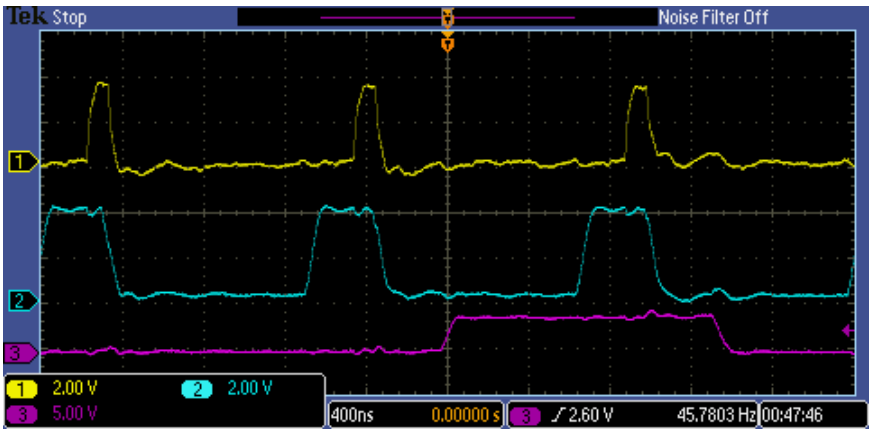

Figure 4.3: ADC clock delay. Purple is frame_sync, blue is pixel_sync and yellow is adc clock. The edge of adc_clk is delayed w.r.t. pixel_clock.

The ADC output is sampled by an FPGA. The FPGA is the central unit of the hardware side of the output processing part. It is responsible for

- Drive and read the ADC.

- Store the ADC data into the on-board SDRAM.
- Send the SDRAM data to a PC when requested.

The FPGA card shown in Figure 4.4 is used in this thesis. The key features of this board are: it has (i) a mid-performance Spartan 3-1500 FPGA, (ii) 32 MByte SDRAM and (iii) a Cypress usb-microcontroller that allows very fast and easy FPGA-PC communication [27].

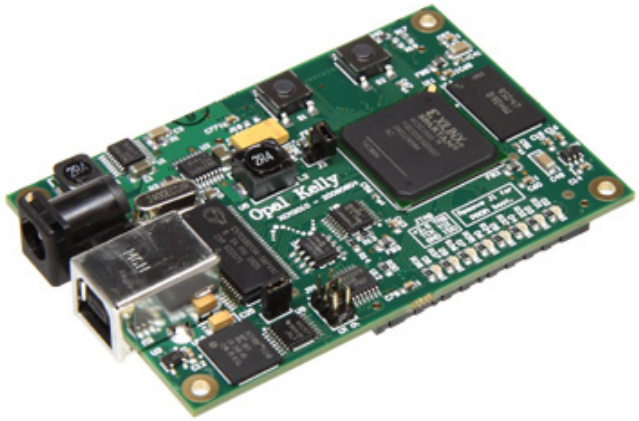

Figure 4.4: The Opal Kelly XEM3010 FPGA board used in this thesis.

A Verilog program is developed for the scope of this thesis. Figure 4.5 shows the block diagram of the verilog program in the FPGA. The data path for a pixel is as follows: write-to-ram FIFO → SDRAM → read-from-ram FIFO → PC.

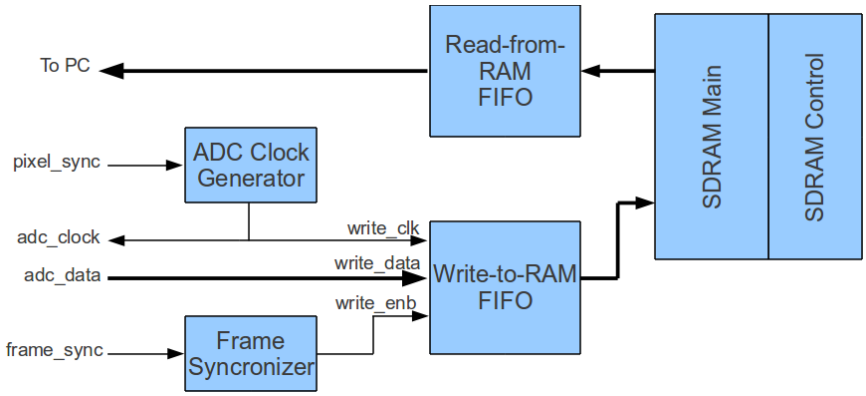

Figure 4.5: Block diagram of the Verilog code.

The SDRAM Control block handles the required signaling and refreshing of the SDRAM, so the rest of the logic can use the SDRAM as if it is an SSRAM. Two FIFOs are used for RAM communications. The reason to employ these FIFOs are the page based memory organization of the SDRAM. The RAM is divided into 512 word length pages. Only the pages are addressable, individual words in the pages are not addressable. When a write or read operation takes place, the whole page will be written or read. Therefore 512 words of data should be ready in writing, and 512 words of data should be stored in reading. The FIFOs provide these buffers. One FIFO is used for reading data to RAM, and one FIFO is used for writing data to RAM. The SDRAM main block controls the states of the FIFOs. If the read-from-ram FIFO is empty, the main block fills it with data from SDRAM. If the write-to-ram FIFO is full, the main block empties its content to the SDRAM. Therefore, this block keeps the FIFOs ready to do their jobs. If the block malfunctions, data (i.e., frames) will be lost. However, the data speed between FPGA and SDRAM is significantly higher than the data speed between FPGA and PC as well as FPGA and microbolometer, so the SDRAM–FPGA communications will not be a bottleneck. The frame synchronizer block enables the FIFO at the beginning of a frame. It ensures the beginning of the SDRAM is also the beginning of a new frame. It performs a synchronization operation.

4.1.2.2 Output Processing Software

The software part processes the ADC data coming from the FPGA. The software used in the tests is written in C++. OpenGL libraries are used to display the infrared image, GLUI libraries are used to create a user interface. Software performs the following operations:

- Take image data from FPGA.
- Map the pixel data to a grey-scale palette.
- One point correction (Also known as fixed pattern noise correction).
- Two point correction (Also known as gain correction).
- Dead pixel correction.

The software polls the SDRAM state to check if a new frame is available to read. If a new frame is available, it reads one frame length data from the FPGA, so software determines

when to get a new frame. This serial raw data is ordered and converted to a matrix. This matrix needs some basic image processing. At first, an offset data should be subtracted from each pixel. The offset value is the value when pixel has no incident IR on it. Offset can be different for each pixel. The reasons for different offset values are process variations, post-CMOS variations, and routing resistances. After offset removal, each pixel data is multiplied by a gain coefficient. Different pixels may react differently to the same level of IR radiation. Process variations and post-CMOS variations cause gain errors.

There are no standard way of defining a dead pixel. A dead pixel can be defined as a pixel with either small or no or very high responsivity. For the 128x128 microbolometer, pixels whose gains are 3 times greater or 0.7 times less than average gain value are considered as dead pixels. The dead pixel data is ignored in image formation. The software determines a dead pixel value by averaging the 8 neighbors of it. If there is a dead pixel in the neighbor, its value is ignored in the calculation.

Offset and gain coefficients are determined by using a blackbody. Five blackbody images are captured with five different blackbody temperatures, so each pixel has five records. A line is fitted to these five points. A line equation is $y = a * x + b$. Here "a" is the gain coefficient and "b" is the offset coefficient. Fitting is done with MATLAB and MATLAB extracts the coefficients and write them to a file. A C program reads the file to get coefficients.

The software can perform one additional image processing: it can apply the median filtering the the image. Median filters are used to remove the salt-and-pepper noise of the images. In median filtering, to find a value of a pixel, a n*n square around the pixel is taken where n is an odd number. The pixels in the square is ordered and the median value is taken. A 3x3 square is used for this camera electronics.

4.1.3 Results

This section shows the test results and the images taken with the explained camera electronics. Figure 4.6 shows the test setup and Figure 4.7 shows the designed dewar PCB. It has an ADC, a DAC, and level shifter buffers. All analog signals are processed/generated on this PCB. Every I/O of this PCB is digital. This feature greatly improves the noise performance of the camera electronics. Figure 4.8 shows the software control panel. The microbolometer and

the FPGA is controlled and monitored with this panel. Figure 4.9 shows two images of the same scene. The figure on the right has dead pixel correction. Figure 4.10 shows the same scene with and without gain correction. The visual quality of images are noticeably improves when image correction algorithms are applied. Figure 4.11 shows another image taken with the developed camera electronics. Figure 4.12 shows an image before and after applying a median filtering.

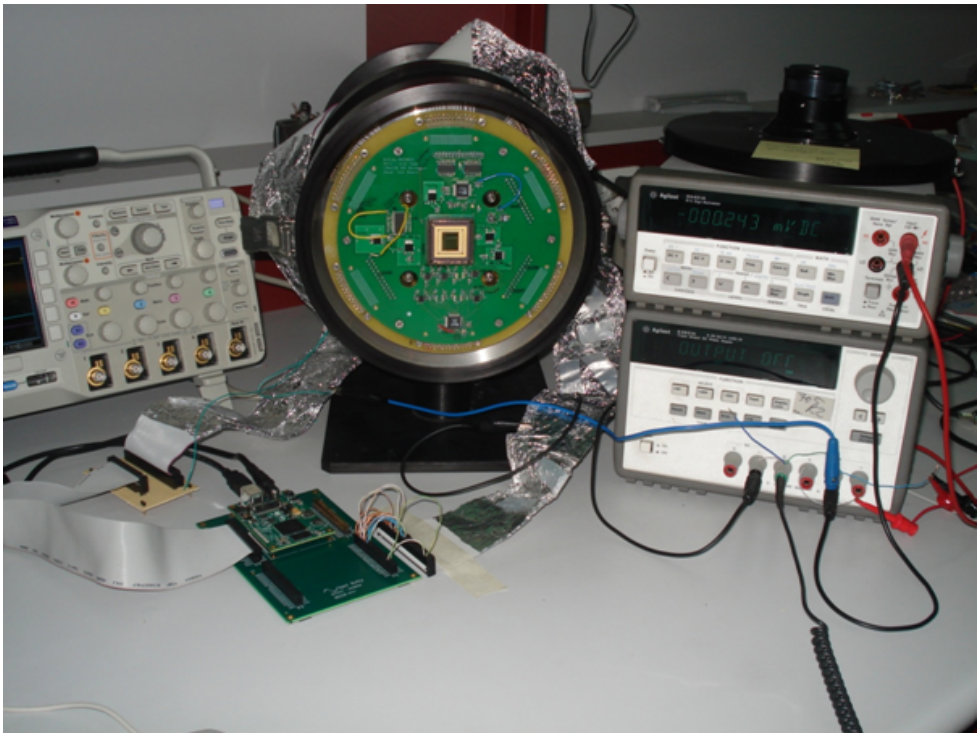

Figure 4.6: Test setup for the 128x128 microbolometer. In addition to dewar PCB, there is only one break-out PCB is used.

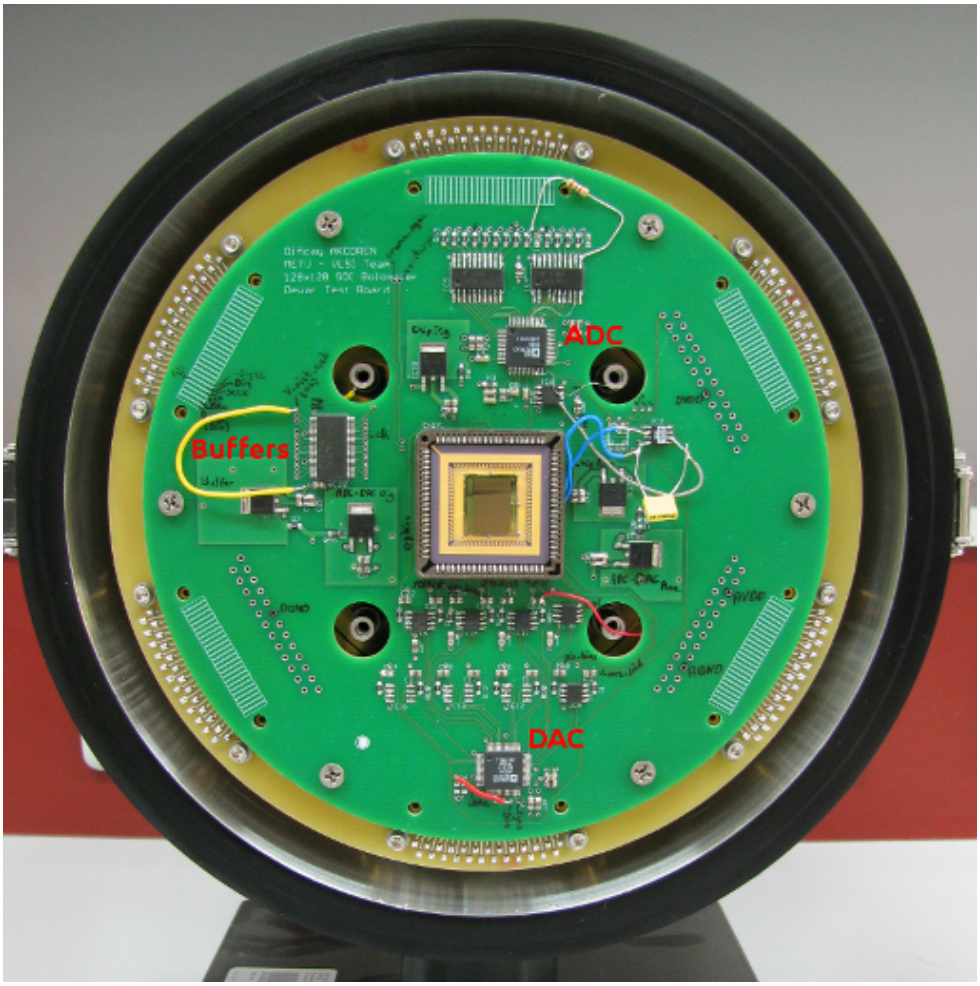

Figure 4.7: Designed dewar PCB for the 128x128 microbolometer. It has an ADC, a DAC and digital level shifters as well as required regulators for supply.

.

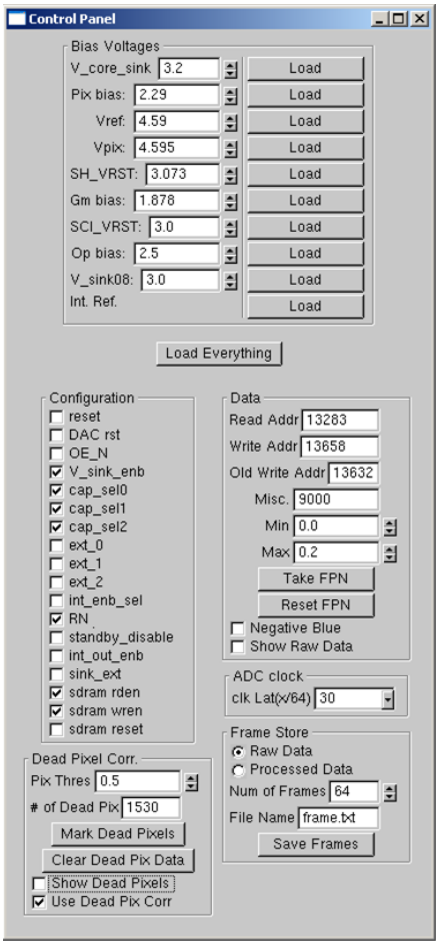

Figure 4.8: Software control panel used in tests. From this panel, DACs can be programmed, the microbolometer configuration can be changed and the RAM state can be monitored. The panel is created with GLUI libraries.

.

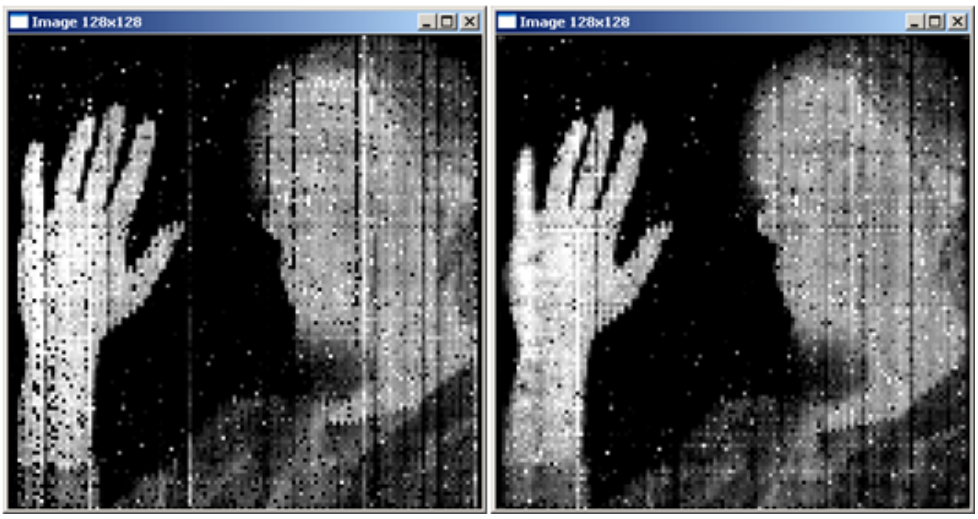

Figure 4.9: Same scene without dead pixel correction (left) and with dead pixel correction (right). Correction is made with the software.

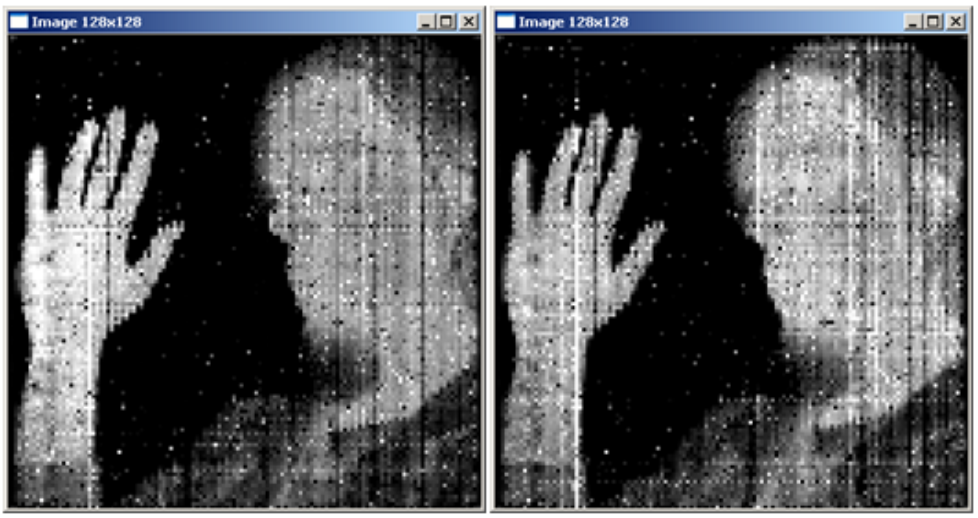

Figure 4.10: Same scene without gain correction (left) and with gain correction (right). Correction is made with the software. Notice the face and hand have same brightness level in the right image.

.

Figure 4.11: Another image taken using the 128x128 bolometer with the developed camera electronics.

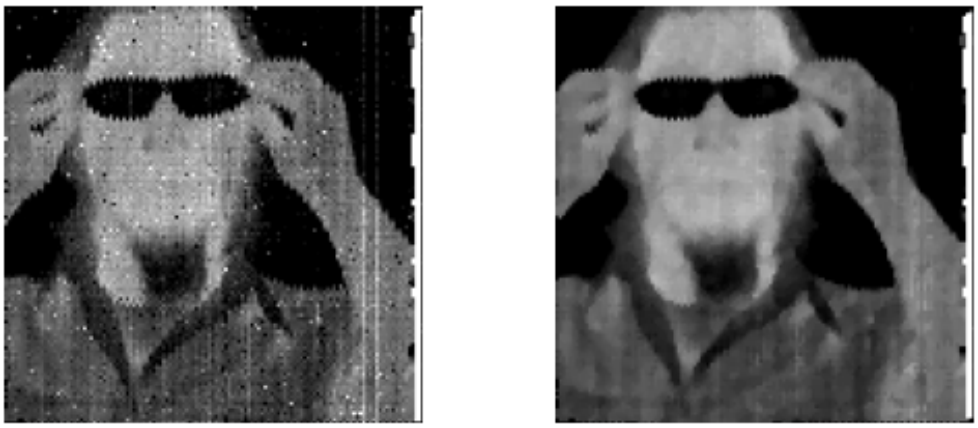

Figure 4.12: An image before (left) and after (right) median filtering. The salt and pepper noise is mostly removed. The image is smoother without losing the sharpness.

To measure the noise of the camera electronics, the microbolometer is disconnected from the system, and a battery is connected to the analog input of the ADC. The bolometer digital outputs are imitated by the FPGA. 64 consecutive frames are saved by the software and anaylsed by MATLAB. The average noise of the pixels are found as $1.5mV_{rms}$ which is equal to 5 LSB of the employed 14 bit ADC in the setup.

The developed camera electronics reduces the NETD of the system from 1.1K to 0.46K. Figure 4.13 show the NETD histogram. The peak NETD is found as 0.34K, and the average

NETD is 0.46K. The total RMS noise of the system is found as $8.4mV_{rms}$. The theoretic noise level is calculated as $5mV_{rms}$. The difference can be caused by wrong 1/f estimation, bolometer system noise, or camera electronics noise. The developed camera electronics simplifies the required external electronics to a dewar PCB and an FPGA board as well as improving the performance of the system. An easy way to transfer data from the microbolometer to an FPGA is developed. This is an important step to reduce the cost of the bolometer system. The analog parts of the external electronics are minimized to decrease the system noise. This increases the overall performance of the microbolometer. Figure 4.14 shows the images taken with previous camera electronics and developed camera electronics for this thesis.

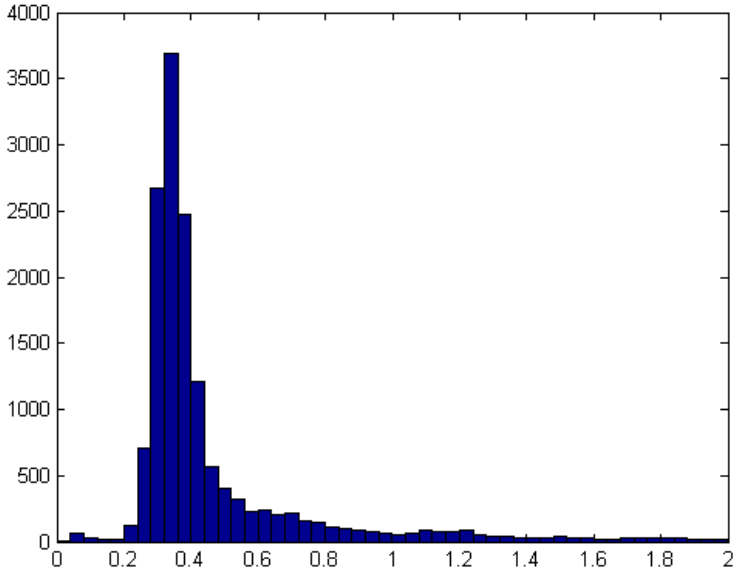

Figure 4.13: NETD histogram of 128x128 bolometer, taken with developed camera electronics. Peak NETD is 0.34K and average NETD is 0.46K.

One of the aims of this study is to make a compact external electronics design. Figure 4.15 shows the previous external camera electronics setup for the 128x128 microbolometer. A vacuum pump, a TEC, and a dewar are common in both of the setups, but the previous setup requires 3 PCBs (dewar PCB, analog PCB and digital PCB) whereas the newly developed setup requires only a dewar PCB.

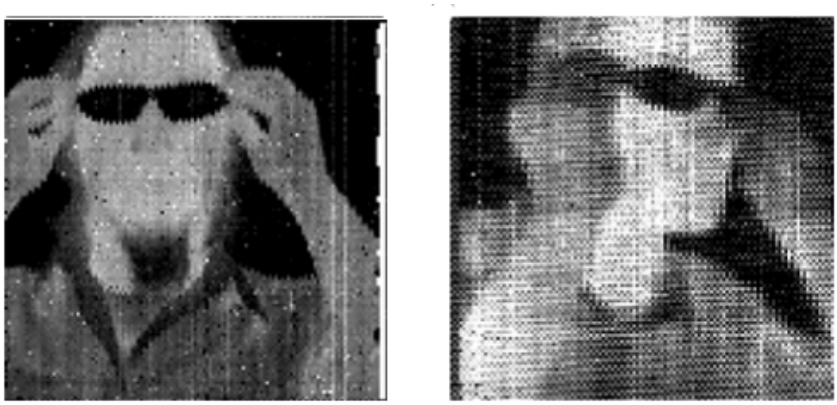

Figure 4.14: Two images taken with two cameras put together for comparison. Image on the left was taken with newly developed camera electronics and image on the right is taken with previous camera electronics.

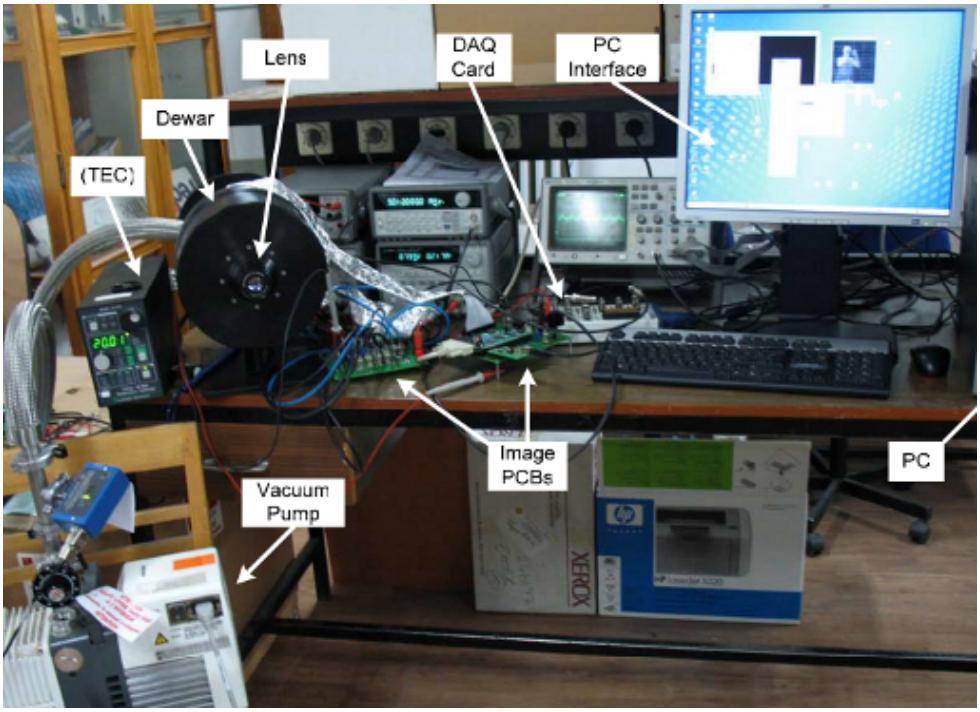

Figure 4.15: Previous setup for 128x128 bolometer. This setup requires 3 PCBs: Dewar PCB, analog PCB and digital PCB [11].

.

4.2 Camera Electronics for 160x120 Low-Cost Microbolometer

This section explains the external electronics developed for the 160x120 SOI microbolometer developed in the framework of this thesis. The improvements over the previous design is described in this section.

4.2.1 Signal Biasing

The camera electronics for the 160x120 microbolometer uses the same signal biasing as the previous system, the same DAC is employed. The microbolometer requires five analog biases instead of nine as in the 128x128 microbolometer camera setup. For digital signals, instead of a digital buffer, a level shifter, utilized for 3.3V–5V level conversion, is used [29].

4.2.2 Output Processing

The hardware for the output processing is same as the one used in the 128x128 microbolometer camera setup. An Opal Kelly FPGA board is used to get data from the microbolometer and transfer it to a PC. However there are some major improvements in the firmware and the software. Most important improvement is the tagging feature, which is explained below.

4.2.2.1 Tagging

The most important improvement of the 160x120 microbolometer camera electronic is the tagging feature. The FPGA inserts some tags in between pixel data. Tagging allows the software to easily recognize the pixel data and to synchronize with it. In a no-tagging system, if a pixel data is lost, the rest of the image will be shifted. If this occurs, the offset and the gain correction algorithms fail, because pixels are shifted in a frame whereas the offset and the gain coefficients will still be same. So pixels will be processed with different coefficients. Figure 4.16 show this situation.

Tagging allows the software to synchronize itself with the received pixel data. Tags are inserted by the FPGA and decoded by the software. The tagging algorithm used in this camera electronics uses 2 different tags: the frame tag and the line tag. Frame tag shows the beginning

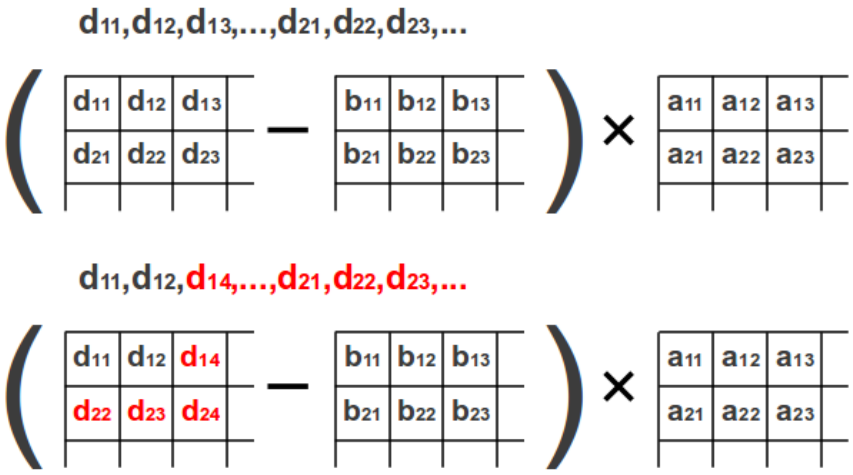

Figure 4.16: Situation when a pixel data is missing if no tagging is used. Pixels will be processed with different offset and gain corrections, which results a messy image. d13 is missing in situation below. d14 will be subtracted from b13 and multiplied by a13, which cause wrong outputs.

of a frame and line tag shows a beginning of a line. Figure 4.17 shows the tagging scheme. Tags also contain numbers. This helps the software to synchronize better and easier. Table 4.1 shows the tag bit map. The RAM word length is 16 bit, ADC output is 14 bit, so 2 bits are remaining for tags. The 14 bits are used for numbering the tags.

frame n	d0	d1	d2	...	...	d158	d159
line 1	d0	d1	d2	...	...	d158	d159
line 2	d0	d1	d2	...	...	d158	d159
line 3	d0	d1	d2	...	...	d158	d159
...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...
line 118	d0	d1	d2	...	...	d158	d159
line 119	d0	d1	d2	...	...	d158	d159
frame n+1	d0	d1	d2	...	...	d158	d159
line 0	d0	d1	d2	...	...	d158	d159
line 1	d0	d1	d2	...	...	d158	d159
...	...	...	...	...	...	...	...

Figure 4.17: Tagging scheme of the camera electronics. Frame tag shows the beginning of the frame and line tag shows the beginning of a line.

Table 4.1: Tag bit structure and explanations.

Tag ID (2)	**Data (14)**	**Explanation**
00	Pixel data	Normal data
01	Line Number	Line tag, line number between [0,118]
10	Frame number	Frame Tag, frame number between [0, $2^{14} - 1$]

When pixel data is tagged, if a pixel data is lost, only the pixels before the next tag will be shifted. The software can understand the beginning of a new frame and the beginning of a new line. It can also understand if a frame tag and/or a line tag is missing by checking the numbers inserted to the tags. Tags are created by the FPGA. Figure 4.18 shows the block diagram of the tagging module. A frame counter counts the number of frames starting from power up, and a line number counts the lines in a frame. The count enable signals are controlled by a tag control block. The tag control block also determines the output of the module by determining the select bus of the multiplexer. An edge detector gives one clock cycle pulses when an edge is detected on the pixel clock. Unless tag_enable is active, one data is written to FIFO. If tag_enable is active, a data is written to FIFO on both the rising edge and the falling edge of the pixel clock. This double edge operation is maintained by faster operation of this module than the microbolometer. It operates with 100MHz whereas the microbolometer operates with 2MHz.

Tags are decoded by the software, which uses the flowchart shown in Figure 4.19. There are two queue structures in the software: data queue and frame queue. Data received from the FPGA is first pushed to the data queue, then data between two frame tags are pushed to the frame queue. This check is done in the grey square #1 in Figure 4.19. With this way, a beginning of a frame cannot be missed. Data in the frame queue is placed into the image matrix with the help of line tags. When a line tag is popped, the active line is updated. It is like pressing the Enter key while typing. If a normal pixel data is popped, it is placed next to the last placed pixel in the same line. Line tag check is done in the grey square #2 in Figure 4.19. By employing tags, the software can synchronize itself with the microbolometer data and ensures a reliable and stable operation under non-ideal circumstances.

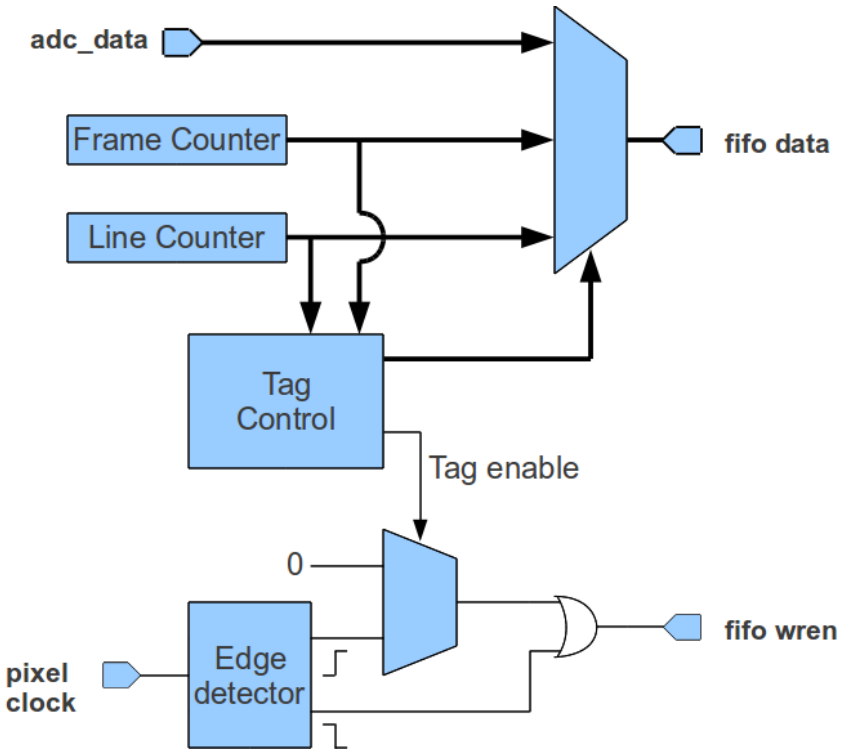

Figure 4.18: Tagging module implemented in an FPGA. OR operation in fifo_wren signal, implies that tags are inserted in between the pixel data without delaying them.

4.2.3 Results

This section shows the improvements over the previous camera electronics and some images taken with the 160x120 bolometer by using this camera electronics. Figure 4.20 shows the test setup used for the 160x120 microbolometer. Figure 4.21 shows the dewar PCB designed for this bolometer. This PCB has same functionality as the previous dewar PCB shown in Figure 4.7. However the used area is much less than previous PCB. This improvement is very critical, since smaller PCB area allows easier miniaturization of external electronics.

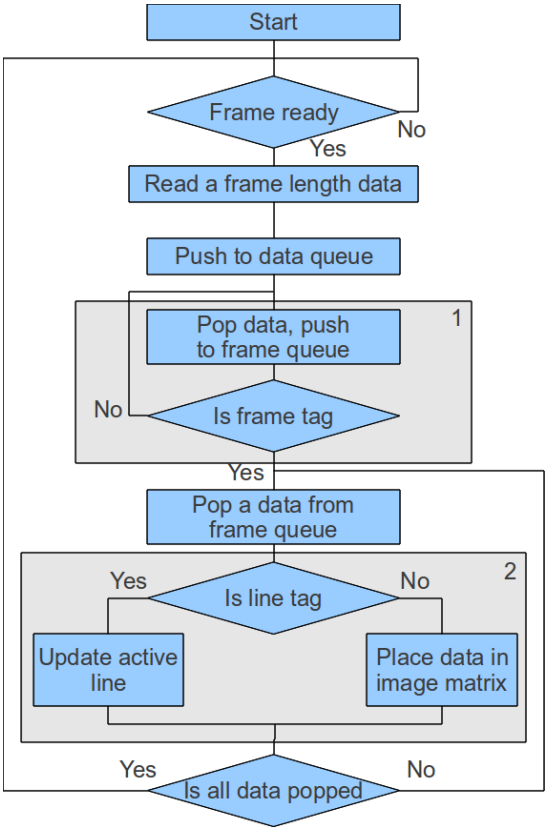

Figure 4.19: Tagging module implemented in FPGA. The OR operation in fifo_wren signal implies that the tags are inserted between the pixel data without delaying them.

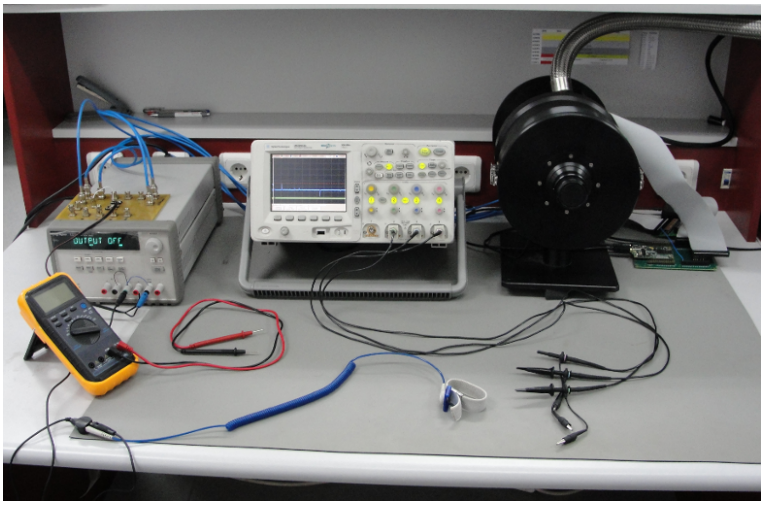

Figure 4.20: Test setup for the 160x120 microbolometer. The PCB on the power supply is just a break-out board that separates a ground and supply connections to multiple BNC connectors.

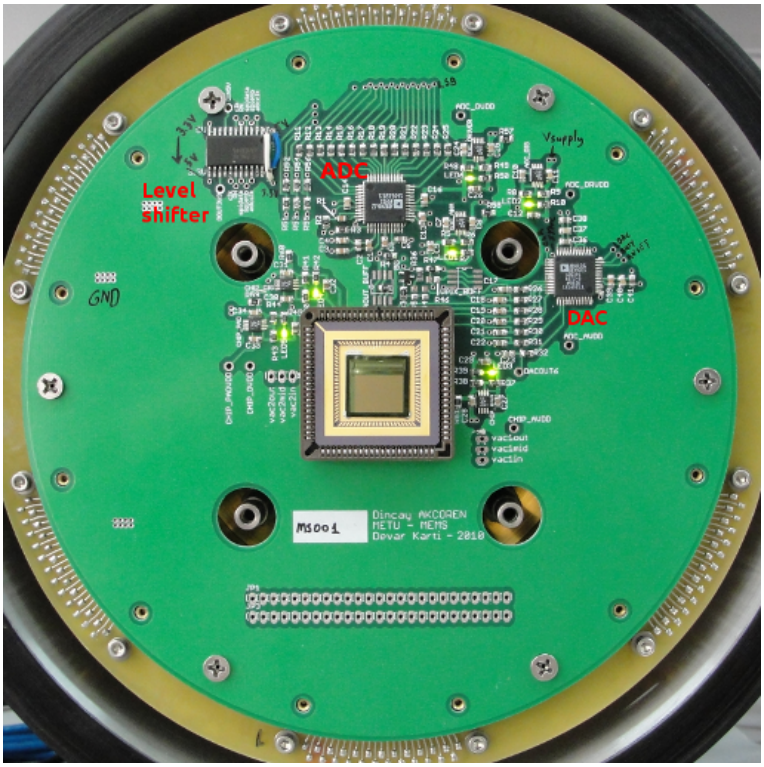

Figure 4.21: Dewar PCB designed for the camera electronics for the 160x120 microbolometer.

To find the NETD of the overall system, consecutive 64 frames are saved to a file and anaylsed in MATLAB. Figure 4.22 shows the calculated NETD histogram. The average NETD is 820 mK and the peak NETD is 350 mK. The noise of the system is calculated as $5.4mV_{rms}$ which corresponds to 17.7 LSB of employed 14 bit ADC.

To measure the noise of the external camera electronics, the 160x120 microbolometer is disconnected from the system, and a battery is connected to the analog input of the employed ADC. The microbolometer digital blocks are generated by the FPGA, so the operation of the rest of the camera electronics will be the same as if the microbolometer is present in the setup. Consecutive 64 frames are recorded and the noise is calculated. The average noise is calculated as $0.53mV_{rms}$, which corresponds to 1.72 LSB of employed 14 bit ADC. Considering the noise level when the microbolometer is present, the overall system is noise limited by the microbolometer noise. Also this noise value is less than the noise value of the external camera electronics for the 128x128 microbolometer.

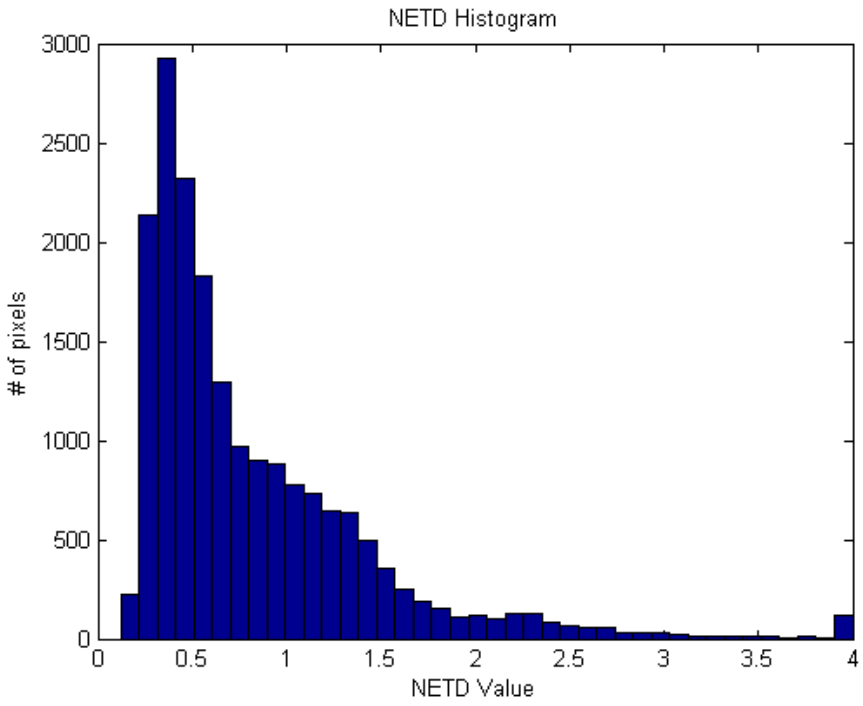

Figure 4.22: NETD historam of the of 160x120 bolometer with newly developed external camera setup. The peak NETD is 350 mK and average NETD is 820 mK.

Figure 4.23 and figure 4.24 shows some images taken with this microbolometer with using the described camera electronics. Only an offset cancellation algorithm is used in the figures.

Figure 4.23: An image taken with the 160x120 microbolometer with developed camera electronics.

Figure 4.24: Another image taken with the 160x120 microbolometer with developed camera electronics.

Figure 4.25 shows two images without median filtering and with median filtering taken with the 160x120 SOI microbolometer and the developed external camera electronics. The median filtering is applied with MATLAB, the processing is done separately. The vertical line is a pipe in the room.

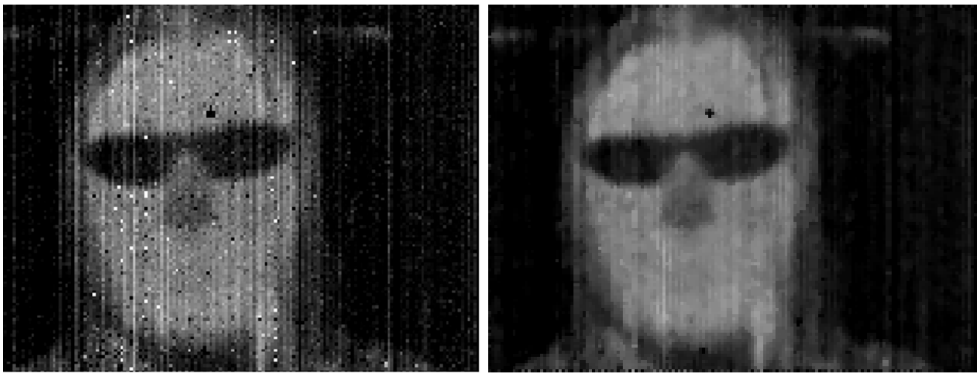

Figure 4.25: An image before(left) and after(right) median filtering taken with the 160x120 SOI microbolometer and newly developed camera electronics. The vertical line is a pipe in the room.

CHAPTER 5

CONCLUSIONS AND FUTURE WORK

The conducted research performed in the framework of this thesis involves the development of a readout electronics for a diode type infrared detector FPA implemented using an SOI-CMOS process and post-CMOS processing along with the development of external camera electronics for obtaining images from these detectors. During this work, analog and digital electronics for the 160x120 FPA is designed. The designed electronics are fabricated with its integrated 160x120 resolution FPA in XFAB 1.0μm SOI process. The developed electronics have features like internal DACs and programmable internal configuration memory that decrease the amount of the required external electronics. The camera electronics for the 128x128 SOI-type microbolometers and the 160x120 SOI-type microbolometers are developed. The major achievements in this thesis can be listed as follows

1. Previously designed camera electronics for the SOI diode-type microbolometers are investigated and their drawbacks are studied. New camera electronics for the 128x128 SOI diode-type microbolometers are developed considering the drawbacks of the previously designed camera electronics to improve the overall NETD performance. The overall system became more compact; only one custom designed PCB is used instead of 3 in previous setup. The new designed system has lower noise level than the 128x128 microbolometer itself, and the overall system become noise limited by the microbolometer noise. The designed external electronics decrease the NETD from 1.1K to 0.46K. The quality of obtained images were the best quality among the low-cost uncooled infrared detectors ever designed at METU-MEMS.

2. Previously designed readout channels for SOI-type bolometers are investigated and their drawbacks are studied. A new readout channel is designed considering the draw-

backs of previous designs. The readout channel is tested and the operation of the circuit is verified.

3. Previously designed SOI diode-type microbolometers are investigated, and their drawbacks are studied. New integrated electronics for the 160x120 SOI microbolometer are designed and fabricated with its integrated the 160x120 resolution FPA. The designed electronics have features like internal DACs and programmable internal configuration memory that allows the microbolometer to operate with less amount of external electronics. The designed microbolometer is tested, and the operation is verified.

4. A new camera electronics for the 160x120 SOI diode-type microbolometer is developed and tested and its operation is verified. The developed camera electronics include a PCB, an FPGA firmware and a software. The designed external electronics have $0.53mV_{rms}$ noise which is ten times less noise than the 160x120 microbolometer developed in the scope of this thesis. The operation of each part is verified and 350 mK peak NETD and 820 mK average NETD is achieved. Human images are obtained by using this external camera electronics, verifying that this system can be used for automotive and security applications.

A great effort has been spent to achieve these results. However, there are some more items that should be performed as future work:

1. The noise of the diodes in the XFAB 1.0 μm SOI process should be characterized. The reasons for variations of the noise should be studied.

2. The op-amps used in readout channel should be re-designed to decrease their power consumption should be decreased to achieve low-power operation.

3. A new and higher performance to output buffer should be designed to decrease the power consumption and increase the signal quality.

4. Integrated voltage DACs should be designed to make all analog biases internal. This will increase the noise susceptibility of the microbolometer and decrease the number of pads.

REFERENCES

[1] O. O. Cellek, S. Ozer, and C. Besikci, "High responsivity InP-InGaAs quantum-well infrared photodetectors: characteristics and focal plane array performance," *IEEE Journal of Quantum Electronics*, Vol. 41, pp. 980-985, 2005.

[2] J. Ziegler, M. Bruder, W. A. Cabanski, H. Figgemeier, M. Finck, P. Menger, T. Simon, and R. Wollrab, "Improved HgCdTe technology for high-performance infrared detectors," in *Proc. of SPIE, Infrared Detectors and Focal Plane Arrays VII*, 1 ed. Vol. 4721, pp. 242-251, 2002.

[3] O. Nesher, I. Pivnik, E. Ilan, Z. Calalhorra, A. Koifman, I. Vaserman, J.O. Schlesinger, R. Gazit, and I. Hirsh, "High resolution 1280 x 1024, 15 μm pitch compact InSb IR detector with on-chip ADC," in *Infrared Technology and Applications XXXV*, 1 ed. Vol. 7298: SPIE, 2009, pp. 72983K-9.

[4] B. M. Nguyen, D. Hoffman, E. K. Huang, P. Y. Delaunay, and M. Razeghi, "High performance Antimony-based Type-II superlattice photodiodes on GaAs substrate," in *Infrared Technology and Applications XXXV*, 1 ed. Vol. 7298: SPIE, 2009, pp. 72981T-13.

[5] C. M. Hanson, H.E Beratan, R. A. Owen, M. Corbin, and S. McKenny, "Uncooled Thermal Imaging at Texas Instruments," *Infrared Detectors: State of the Art*, Proc. of SPIE, Vol. 1735, pp. 17-26, 1992.

[6] T. Kanno, M. Saga, S. Matsumoto, M. Uchida, N. Tsukamoto, A. Tanaka, S. Itoh, A. Nakazato, T. Endoh, S. Tohyama, Y. Yamamoto, S. Murashima, N. Fujimoto, N. Teranishi, "Uncooled Infrared Focal Plane Array Having 128x128 Thermopile Detector Elements," *Proc. SPIE, Infrared Technology XX*, Vol. 2269, pp. 450-459, 1994.

[7] D. Murphy, M. Ray, A. Kennedy, J. Wyles, R. Wyles, E. Gordon, T. Seller, S. Baur, and D. Van Lue, "High Sensitivity 640 x 512 (20 μm Pitch) Microbolometer FPAs," *Proc. of SPIE, Infrared Technology and Applications XXXII*, Vol. 6206, pp. 62061A-1-62061A-14, April 2006.

[8] R. A. Wood, "Uncooled Thermal Imaging with Monolithic Silicon Focal Arrays," Infrared Technology XIX, SPIE Vol. 2020, pp. 322-329, 1993.

[9] S. Eminoğlu, M. Y. Tanrıkulu, D. S. Tezcan, and T. Akin, "A low-Cost Small Pixel Uncooled Infrared Detector for Large Focal Plame Arrays using a Standard CMOS Process," *Proc. of SPIE*, Vol. 4721, pp. 111-121, 2002.

[10] P. W. Kruse, *Uncooled Thermal Imaging Arrays, Systems, and Applications*, SPIE Press, 2001.

[11] E. İncetürkmen, "A Low-Cost 128x128 Uncooled Infrared Detector Array in a Standard SOI-CMOS Technology," M.S. Thesis, Department of Electrical and Electronics Engineering, Middle East Technical University, 2008.

[12] K. F. Reinhart, M. Eckardt, I. Herrmann, A. Feyh, F. Freund, "Low-cost Approach for Far-Infrared Sensor Arrays for Hot-spot Detection in Automotive Night Vision Systems," *Advanced Microsystems for Automotive Applications AMAA*, pp. 397-408, 2009.

[13] Hiroto Honda, Hideyuki Funaki, Ikuo Fujiwara, Hitoshi Yagi, Kouichi Ishii, Kazuhiro Suzuki, Keita Sasaki, Masako Ogata, Risako Ueno, Honam Kwon, "A 320 x 240 pixel uncooled TEC-less infrared radiation focal plane array with the reset noise canceling algorithm," *Proc. of SPIE*, Vol. 7660, 2010.

[14] J. L. Tissot, O. Legras, C. Minassian, P. Robert, B. Fieque, S. Tinnes, B. Dupont, J. J. Yon, A. Arnaud, "Compact uncooled amorphous silicon 160 x 120 IRFPA with 25 μm pixel-pitch for large volume applications," *Proc. of SPIE*, Vol. 6737, 2009.

[15] D. S. Tezcan, S. Eminoğlu, and T. Akın, "A Low Cost Uncooled Infrared Microbolometer Detector in Standard CMOS Technology," *IEEE Transactions on Electron Devices*, Vol. 50, No. 2, pp. 494-502, Feb. 2003.

[16] E. Alpman, "Development of Low-Cost Uncooled Infrared Detector Arrays in Standard CMOS and SOI-CMOS Processes," M.S. Thesis, Department of Electrical and Electronics Engineering, Middle East Technical University, 2005.

[17] K. S. Demirci, "A low-cost 16x16 uncooled infrared detector FPA using standard CMOS and wafer level MEMS processes," M.S. Thesis, Department of Electrical and Electronics Engineering, Middle East Technical University, 2005.

[18] D. S. Tezcan, S. Eminoğlu, O. Akar, and T. Akın, "An Uncooled Microbolometer Infrared Focal Plane Array in Standard CMOS," *Proc. of SPIE*, Vol. 4288, pp. 112-121, 2001.

[19] S. Eminoğlu, M. Y. Tanrikulu, and T. Akın, "Low-Cost 64x64 Uncooled Infrared Detector Arrays in Standard CMOS," *The 12th Int. Conf. on Solid-State Sensors and Actuators (TRANSDUCERS'03)*, pp. 316-319, June 2003.

[20] S. Eminoğlu, "Uncooled Infrared Focal Plane Arrays With Integrated Readout Circuitry Using MEMS and Standard CMOS Technologies," Ph. D. Dissertation, Department of Electrical and Electronics Engineering, Middle East Technical University, 2003.

[21] S. Eminoğlu, M. Y. Tanrikulu, and T. Akın, "Low-Cost Uncooled Infrared Detector Arrays in Standard CMOS," *Proc. of SPIE*, Vol. 5074, pp. 425-436, 2003.

[22] K. Bernstein, N.J. Rohrer, *SOI Circuit Design Concepts*, Kluwer Academic Publishers, 2003.

[23] http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus, Last Access: Feb. 2011.

[24] Analog Devices, "8-/16-Channel, 3 V/5 V, Serial Input, Single-Supply, 12-/14-Bit Voltage Output," AD5391 datasheet, Jan. 2009.

[25] XFAB Semiconductor Foundries, "Process Specification XI10 - 1.0 μm SOI CMOS Release 1.0," Process Specifications, 2001.

[26] Analog Devices, "Complete 14-Bit, 10 MSPS Monolithic A/D Converter," AD9240 datasheet, 2010.

[27] Opal Kelly Inc., “XEM3010 User’s Manual,” XEM3010 User Guide, 2009.

[28] Fairchild Semiconductor, “16-Bit Buffer/Line Driver with 3-STATE Outputs,” May. 2005.

[29] Fairchild Semiconductor, “8-Bit Dual Supply Translating Transceiver with 3-STATE Outputs,” 74LVX3245 datasheet, Feb. 2010.