ZERO-LEVEL PACKAGING OF MICROWAVE AND MILLIMETERWAVE MEMS COMPONENTS

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ABSTRACT

ZERO-LEVEL PACKAGING OF MICROWAVE AND MILLIMETERWAVE MEMS COMPONENTS

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This thesis presents realization of two shunt, capacitive contact RF MEMS switches and two RF MEMS SPDT switches for microwave and millimeter-wave applications, two zero-level package structures for RF MEMS switches and development trials of a BCB based zero level packaging process cycle.

Two shunt, capacitive contact RF MEMS switches for 26 GHz and 12 GHz operating frequencies are designed, fabricated and consistencies between fabricated devices and designs are shown through RF measurements. For the switch design at 26 GHz and at the

operating frequency, return loss in the upstate is measured to be 27.61 dB, insertion loss and isolation in the downstate is measured to be 0.21 dB and 27.16 dB, respectively. For the switch design at 12 GHz and at the operating frequency, return loss in the upstate is measured to be 38.69 dB, insertion loss and isolation in the downstate is measured to be 0.05 dB and 25.84 dB, respectively. Quite accurate circuit models have been obtained for both of the RF MEMS switches. Two RF MEMS SPDT switches, which utilize the shunt, capacitive contact switches as building blocks are designed through circuit simulations. These two designs are fabricated and their RF measurements have been completed. It is shown from circuit model simulations that, the performances of the fabricated devices and desired responses corresponded to each other. For the SPDT switch design at 26 GHz, return loss at the input port is measured to be 12 dB and insertion loss is measured to be 1.24 dB. For the SPDT switch design at 12 GHz, return loss at the input port is measured to be 5.6 dB and insertion loss is measured to be 0.49 dB. The reason behind the unexpectedly bad performances has been investigated and discovered. The bad performances were due to a common mistake in the layouts of both SPDT switches. These mistakes are corrected in the circuit models and expected performances are obtained.

Two different zero-level package structures which use high-resistive Si wafers have been suggested and required design changes have been made on the RF MEMS shunt, capacitive contact switches and SPDT switches in order to minimize the package effects. For this purpose polygonal CPW transitions have been designed and integrated into the designs, followed by the necessary tunings in the switch structures for which EM and circuit simulations are utilized.

For the suggested package structures to be produced, two possible process cycles have been studied. One of the process flows was based on KOH anisotropic Si etching and the other one was based on DRIE (Deep Reactive Ion Etching). Great progress has been achieved in the latter process cycle, however this process cycle still needs some more study and it could not be completed in the time required for this thesis study.

Keywords: RF MEMS, switch, SPDT (single pole double throw), microwave, millimeter-wave, package, CPW, KOH, DRIE.

ÖZ

MİKRODALGA VE MİLİMETREDALGA MEMS BİLEŞENLERİNİN SIFIR-SEVİYE PAKETLENMELERİ

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Eylül 2010, 122 sayfa

Bu tezde, mikrodalga ve milimetre-dalga uygulamaları için iki adet paralel, sığal değeçli RF MEMS anahtar ve iki adet RF MEMS TGÇÇ (Tek Giriş Çift Çıkış) anahtar yapısının tasarımları, üretim aşamaları ve ölçüm sonuçları, RF MEMS anahtarlar için iki adet sıfır-seviye paket yapısının geliştirilmesi ve bu paket yapılarının oluşturulabilmesi için gereken proses adımlarının geliştirilmesi aşamaları anlatılmaktadır.

26 GHz ve 12 GHz çalışma frekanslarında iki adet paralel, sığal değeçli RF MEMS anahtar yapısı tasarlandı, üretildi ve RF ölçümler sonunda üretilen yapılar ile tasarımlar arasındaki

uyumluluk gösterildi. 26 GHz'te tasarlanan anahtar yapısında ve çalışma frekansında, yukarı durumda geriye dönüş kaybı 27.61 dB olarak ölçüldü, aşağı durumda araya girme kaybı ve yalıtım sırasıyla 0.21 dB ve 27.16 dB olarak ölçüldü. 12 GHz'te tasarlanan anahtar yapısında ve çalışma frekansında, yukarı durumda geriye dönüş kaybı 38.69 dB olarak ölçüldü, aşağı durumda araya girme kaybı ve yalıtım sırasıyla 0.05 dB ve 25.84 dB olarak ölçüldü. Her iki RF MEMS anahtar için de oldukça uyumlu devre modelleri elde edildi. Bahsi geçen paralel, sığal değeçli anahtar yapılarının yapı taşı olarak kullanıldığı, iki adet RF MEMS TGÇÇ anahtar yapısı devre benzetimleri ile tasarlandı, üretildi ve RF ölçümleri tamamlandı. Devre modeli benzetimleri gösterdi ki, üretilen yapıların başarımları tasarımlarda elde edilen başarımlarla örtüştü. 26 GHz'teki TGÇÇ anahtar yapısında, geri dönüş kaybı 12 dB ve araya girme kaybı 1.24 dB olarak ölçüldü. 12 GHz'teki TGÇÇ anahtar yapısında, geri dönüş kaybı 5.6 dB ve araya girme kaybı 0.49 dB olarak ölçüldü. Üretilmiş TGÇÇ anahtar yapılarının beklenmeyen derecede kötü başarımlarının sebebi araştırıldı ve bulundu. Bu kötü başarımların SPDT anahtarların serimlerinde ki ortak bir hatadan kaynaklandığı farkedildi. Bu yanlışlıklar devre modeli üzerinde düzeltildi ve beklenen başarımlar elde edildi.

Yüksek özdirençli silisyum pulların kullanıldığı iki adet sıfır-seviye paket yapısı önerildi ve bu paket yapısının RF etkilerini en aza indirebilmek için gereken tasarım değişiklikleri RF MEMS paralel, sığal değeçli anahtar yapılarına ve TGÇÇ anahtar yapılarına uygulandı. Bunun için, EDK (Eşdüzlemsel Dalga Kılavuzu) poligonsal geçişler tasarlandı ve anahtar tasarımlarına eklendi ve bu eklemelerin ardından anahtar yapılarındaki gerekli ayarlamalar EM ve devre benzetimleri üzerinden gerçekleştirildi.

Önerilen paket yapısının elde edilebilmesi için, iki adet proses döngüsü üzerinde çalışıldı. Bunlardan bir tanesi KOH anizotropik silisyum aşındırma yöntemine, diğeri ise DRIE ile silisyum aşındırma yöntemine dayanıyordu. İkinci yöntemde büyük gelişim kaydedildi fakat, bu yöntemin kullanılabilir aşamaya gelmesi için hala çalışılmaya ihtiyaç duyulmaktadır ve bu tez çalışması içinde sonuca ulaşılamamıştır.

Anahtar Kelimeler: RF MEMS, anahtar, TGÇÇ (tek giriş çift çıkış), mikrodalga, milimetre-dalga, paket, KOH, DRIE.

Dedicated to my family...

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INTRODUCTION

Radio Frequency (RF) Micro-Electro-Mechanical Systems (MEMS) mean the devices fabricated by microfabrication processes and they are operational on the RF domain. These sub-millimeter sized movable parts provides the functionality. As they are functional in the RF domain and fabricated by micromachining techniques, RF MEMS devices are constructed on planar transmission lines such as coplanar waveguide (CPW) lines or micro-strip lines. Not only by this structural property but because of their relatively small sizes, low electrical loss is a basic specification of RF MEMS devices. Owing to their high electrical performance, rather simpler design, small size and relatively low cost, RF MEMS devices holds the power the be a key solution especially in telecommunications and space applications [1].

One of the most important properties RF MEMS holds is the reconfigurability which is provided automatically. Basic RF MEMS devices are switches [2-14] and tunable capacitors [15-19] that provides the reconfigurability. RF MEMS switch is the basic unit of the technology, by which more complicated devices are constructed. "RF MEMS switch is favored due to its low insertion loss and high isolation, which substantially exceeds the performances of its Field Effect Transistor (FET) and PIN diode counterparts" [1].

Operations of most of the RF MEMS devices are based on the movement of sub-millimeter sized parts. These devices are produced by microfabrication processes and

require a clean environment during fabrication and during operation as well. Because contamination may affect the mechanical movement of the devices which directly influence the electrical performance. Furthermore, RF MEMS devices may be affected from humidity, electromagnetic fields or magnetic fields, which is a drawback in terms of reliability. Especially the performances of the shunt, capacitive contact RF MEMS switches, which this study is mostly based on are exponentially decrease in terms of life time due to humidity. On the other hand, it will not be meaningful to expect cleanroom conditions wherever RF MEMS devices utilized. In order to be able to use RF MEMS devices in outside world, we need protection from the harsh conditions which may affect the functionality.

Packaging of RF MEMS devices is a requirement not only for protection but also for controllability of the environment which the devices work in. Packaging is one of the most essential requirement for gyroscopes, infrared detectors and RF components which are fabricated by MEMS technology [20-23]. Packaging of the micro devices can be classified into three as zero-level (wafer level) packaging, first-level packaging and second-level packaging.

- Wafer level packaging creates an on-wafer device scaled sealed cavity for the fragile MEMS device, carried out during wafer processing, prior to die singulation [24],
- First-level packaging is, embedding the device into a package usable in the outside world where the connections should be carried outside the package [25],
- Second-level packaging is to mount the first-level packaged system to a board.

In the context of this thesis, zero-level packaging is studied and this subject is considered in detail under the following title.

1.1 Wafer Level Packaging

Packaging and testing the packaged devices compose a great portion of the total cost needed to obtain the MEMS components. In order to decrease the total cost, packaging should be done prior to die singulation on wafer level. By wafer-level packaging approach, MEMS devices can indeed be protected from the chemical and mechanical harms which can occur during the wafer dicing operation. Thus, throughput of the MEMS fabrication may increase. Wafer level package can be defined as the first protective interface which is encapsulation of the movable parts on wafer level in a sealed cavity [23].

Being able to utilize conventional package structures for the zero-level packaged MEMS components is another advantage of wafer-level packaging. Because, by this method the cost required to produce a utilizable MEMS device can be decreased. Wafer level packaging actually is a part of the complete packaging work, which is shifted back in the process chain prior to wafer dicing [25].

Wafer level packages make the handling of the fragile MEMS devices easy. So rather than monolithically fabricating every part of a complete system which is usually not possible, integration of different technologies becomes feasible. Wafer-level packaging processes increase the effectiveness of the integration of passive components into complete systems [26].

In wafer-level packaging processes, either a cap wafer is bonded to the process wafer by using an adhesive material if necessary (wafer bonding) [21],or a shell is formed by growing new layers on top of the device (thin film encapsulation) [22].

In addition to these benefits of wafer level packaging, the conditions inside the package can be controlled. The process can be made hermetic or semi-hermetic, also instead of vacuum

inside, an inert gas can be used such as argon (Ar) to prevent any chemical reaction that may take place.

The electrical effects of wafer level packaging to the operation of the structures is not crucial for low frequency applications, however in RF MEMS structures these effects become significant. There are two main electrical effects that should be considered.

- The electrical performance will be altered after 0-level packaging due to the closeness of the wafer level package to the surface of RF MEMS structure. Etched cavities are provided on cap-wafers to minimize these effects.
- Characteristic impedances of the signal paths will be altered due to the loading of the zero-level package and reflections will occur because of the induced mismatches.

Packaging issues should be taken into consideration during the design because of these effects which could alter the performance of the structure significantly. That is why the models used in EM simulations prior to the process should include the zero level packages with the device intended to be packaged.

Zero-level packaging can be categorized into two in terms of the packaging method utilized; chip capping and thin film encapsulation. Furthermore, chip capping can be divided into two as wafer to wafer level packaging and chip to wafer level packaging.

1.1.1 Thin Film Encapsulation

By using LPCVD (Low Pressure Chemical Vapor Deposition) or PECVD (Plasma Enhanced Chemical Vapor Deposition) techniques, poly-SiGe, silicon nitride (Si_xN_y), silicon oxide (SiO_2) materials can be deposited and these layers can be used to encapsulate the MEMS devices [27]. In thin film encapsulation packaging method, a second sacrificial layer

is coated or formed on top of the MEMS device, before releasing the structures, in other words before removing the first sacrificial layer. Forming second sacrificial layer is followed by deposition of the thin film (poly-SiGe, Si_xN_y, SiO_2 etc) on top of it as a shell. Sacrificial layers are removed either by wet etching or plasma etching, which could both penetrate into the sacrificial layers from the holes opened on the thin film. After removing the sacrificial layers, the holes on the shell can be closed by applying another PECVD or LPCVD process. Many MEMS components are reported to be packaged by thin film encapsulation [22, 28-31].

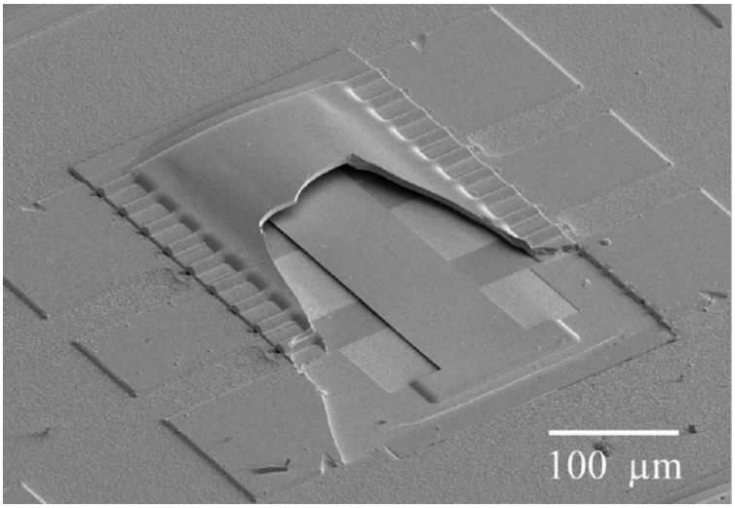


Figure 1.1: SEM image of a dielectric shell over an RF MEMS switch. Shell partially removed to see underlying switch [22].

In thin film packaging hermeticity may be ensured however, it is not possible to control the environment inside the package. Inside the package, it will be the exact same conditions and gases, which have been utilized in the deposition of the thin films in the PECVD or LPCVD chamber. In addition to this, the temperatures during the deposition of thin films may exceed 400 ºC, which will not be suitable if gold structural layer is utilized.

1.1.2 Chip Capping

Chip capping utilizes a cap wafer for enclosing the MEMS device and requires wafer bonding processes. The cap wafer is processed and have cavities on it for housing the MEMS devices. The process wafer and cap wafer are bonded to each other by the use of an adhesive material. Adhesive material is given the shape of a ring around the MEMS devices and seals the MEMS device under the cavity. The hermeticity of the package indeed is determined by the adhesive material utilized. There are many reported package structures which uses gold (eutectic bonding) [32, 33], glass frit [20], BCB [34-38] etc. There are two types of chip capping methods which are wafer-to-wafer encapsulation and cap-to-wafer encapsulation. There is no structural difference between the packages these two methods provide, the only difference is in terms of process chain.

1.1.2.1 Wafer to Wafer Encapsulation

In the wafer-to-wafer encapsulation all of the structures on the process wafers could be capped simultaneously and by this way the spent time decreases substantially.

The bonding material ensures a uniform pressure distribution between the cap wafer and the process wafer. This uniform pressure distribution provides a fixed and uniform cap to device spacing throughout the whole wafer. However, in this case dicing becomes problematic since you have to dice two wafers at the same time.

1.1.2.2 Cap to Wafer Encapsulation

This type of encapsulation can be done with flip chip bonding. (Flip chip microelectronic assembly is the direct electrical connection of face-down (hence, "flipped") electronic components onto substrates, circuit boards, or carriers, by means of conductive bumps on the chip bond pads. In contrast, wire bonding, the older technology which flip chip is

replacing, uses face-up chips with a wire connection to each pad) Cap-to-wafer encapsulation has the disadvantage of being more time consuming. It is because in this type of encapsulation the structures to be packaged will be processed separately. However, in cap-to-wafer encapsulation, dicing is much simpler than in wafer-to-wafer encapsulation.

1.2 Motivation of Dissertation

RF MEMS packaging studies have been started by Dr. Kağan Topallı in METU RF MEMS group. A wafer to wafer encapsulation process has been developed by the use of glass frit as the bonding material [39]. The properties of glass frit which lead METU RF MEMS group to work with this material can be itemized as;

- Proven quality of the glass frit bonding in gyroscope and accelerometer packages,
- Hermetic packaging ability,
- Easy processing and patterning of glass frit by screen printing technology,

In the context of the study CPW transmission lines have been packaged using glass frit bonding. Figure 1.2 presents bonded process wafer and cap wafer, utilized in the glass frit packaging. In addition to this, presents a closer view inside a pad window where CPW lines can be seen. In the processing of the Si cap wafer, KOH anisotropic etching has been utilized and both cavities and pad windows have been formed.

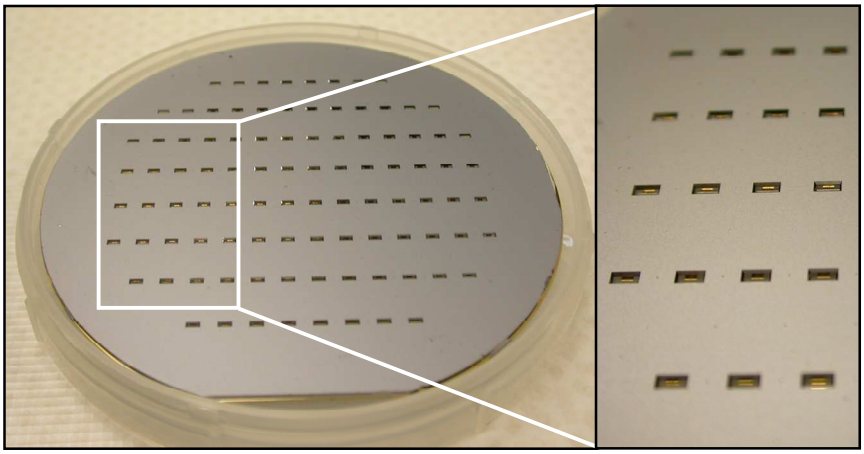


Figure 1.2: Zero-level packaged CPW lines after the wafer bonding. Pad windows opened for measurement purposes can be seen better in the right image

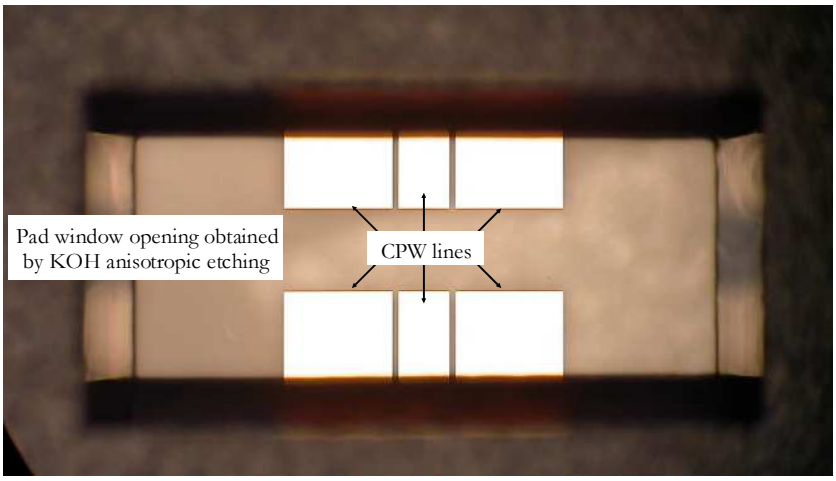


Figure 1.3: Closer view of one of the pad window openings seen in Figure 1.2

SEM pictures showing the glass frit layer after the wafer bonding can be seen in Figure 1.4.

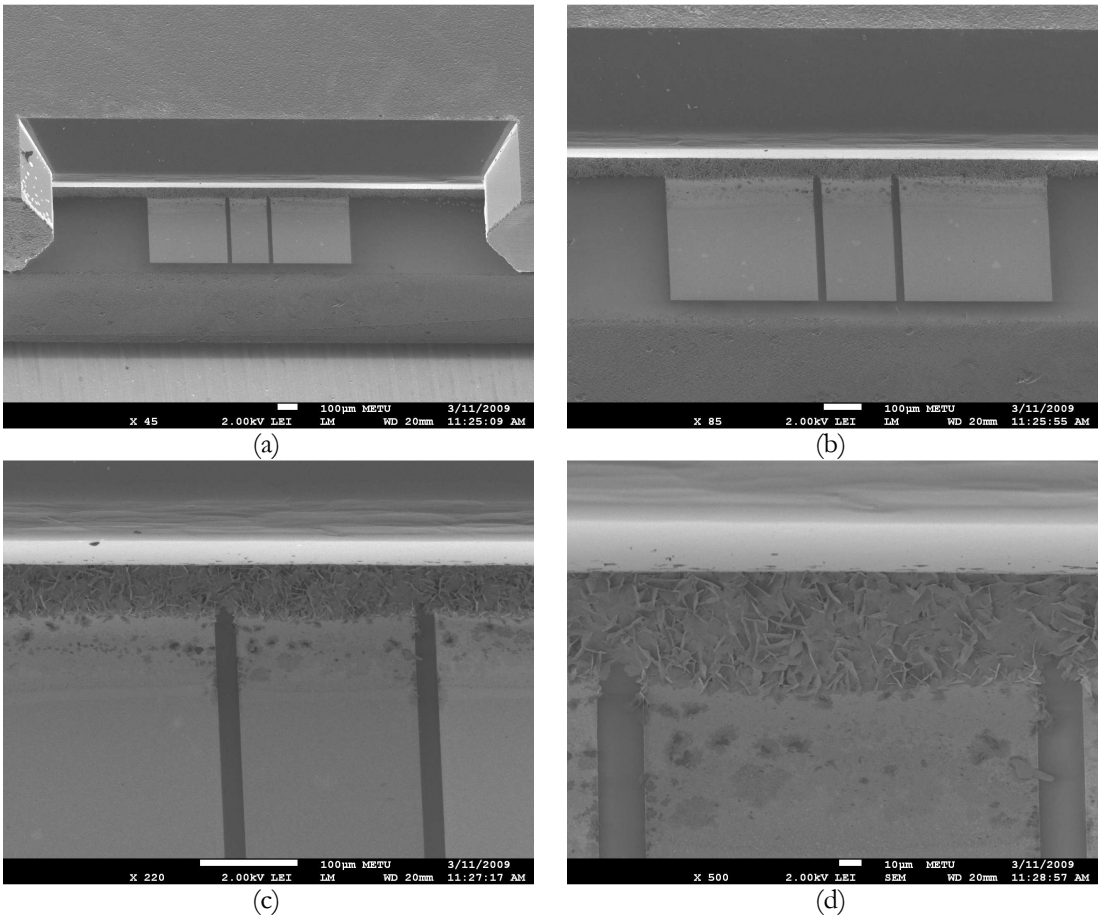


Figure 1.4: SEM pictures of the same pad window after glass frit packaging with different magnifications

CPW transmission lines have been packaged with glass frit bonding successfully, however packaging a MEMS switch is different. In a MEMS switch there are movable parts, which are suspended. Since glass frit bonding needs a bonding temperature of ~425 ºC, packaging suspended structures made of gold is not appropriate for this kind of bonding material.

This reasoning lead METU RF MEMS group to change the bonding material and BCB has been adopted, because;

- BCB needs a relatively low bonding temperature (250 ºC),
- BCB is a semi-hermetic material which the RF MEMS group's needs overlap,
- BCB is photodefinable material which can easily be processed and patterned by UV photolithography techniques.

1.3 Overview of the Thesis

This thesis consists of five chapters. This chapter has provided an overview on RF MEMS and RF MEMS wafer-level packaging. Chapter 2 starts with an overview of the RF MEMS switch which is the key component of the technology. Then it gives detailed information on the realization of two, shunt, capacitive contact RF MEMS switches and two RF MEMS SPDT switches where shunt, capacitive contact switches are utilized as building blocks. Realization of the SPDT switches is divided into subsections such as design steps, fabrication steps and measurement results. Chapter 3 provides explanations on the structures of two proposed zero-level packages. Introduction of these packages into a 35 GHz shunt, capacitive contact RF MEMS switch is provided in this section as well. In addition to this, package integrations of RF MEMS SPST and SPDT switches, whose design steps, fabrication steps and measurement results are provided in Chapter 2, are expressed in Chapter 3. Third chapter ends with EM and circuit simulation results of the packaged structures. Process development steps of the proposed BCB based zero-level package structures are provided in Chapter 4. Development of the process cycle is divided into three groups; BCB process optimizations, KOH anisotropic Si etching based packaging approach and DRIE based packaging approach. Chapter 5 presents the conclusions from this study and future work that can be conducted to further the capabilities of presented SPDT switches and to realize the packaging process.

CHAPTER 2

REALIZATION OF KU-BAND AND KA-BAND SPST AND SPDT RF MEMS SWITCHES

This chapter investigates development of two SPDT (single pole double throw) RF MEMS switches for microwave applications using an in-house RF MEMS fabrication process. The SPDT switch structure consists of two, shunt, capacitive contact SPST (single pole single throw) RF MEMS switches, a CPW (Coplanar Waveguide) T-junction structure, two CPW 90º Bend structures, two MIM (Metal-Insulator-Metal) DC-Blocking capacitors and CPW lines with various types and lengths. This chapter begins with an introduction section which gives detailed information on operating principles and types of RF MEMS SPST switches and SPDT switches. Section 2.2 introduces the electromagnetic designs of the SPDT switches at Ku-Band and Ka-Band by investigating each component individually. Then, Section 2.3 provides information on the in-house RF MEMS fabrication process which has been used during the fabrication of the SPDT and SPST switches. Utilized RF measurement setup, encountered problems during the measurements and obtained results will be presented in Section 2.4, by providing comparisons with the electromagnetic and circuit simulation results.

2.1 Introduction

Among the RF MEMS components, RF MEMS switch is the key component for the enabling technology and it serves as a building block for more complicated device configurations. Since this chapter focuses on RF MEMS SPST and SPDT switches and for

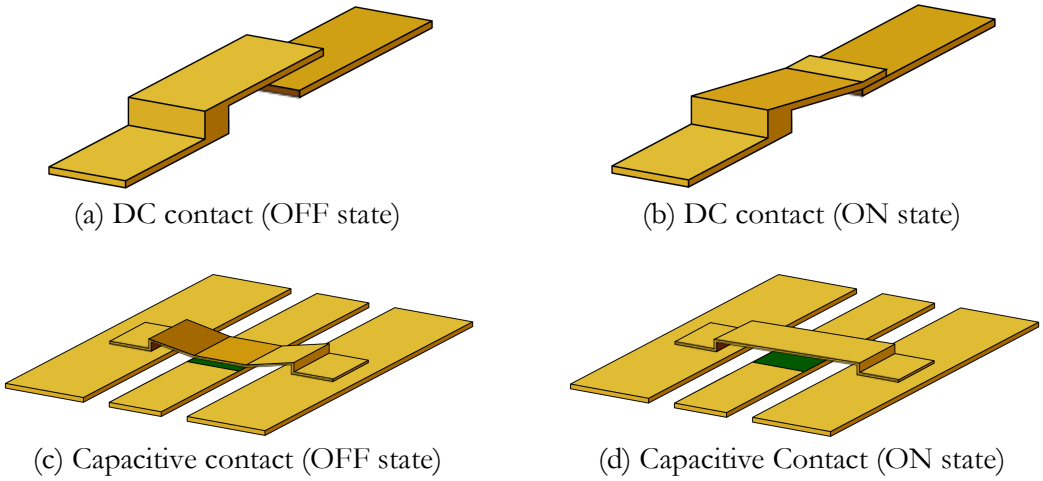
comprehensibility of RF MEMS technology, an overview of the types and features of its key component holds great significance.

2.1.1 Overview of RF MEMS SPST Switch

RF MEMS switches can be classified into different groups according to their contact types, circuit configurations and actuation mechanisms.

2.1.1.1 Contact Types

RF MEMS switches can be categorized into two groups in terms of the contact types between the signal line and the MEMS bridge. Figure 2.1 indicates some MEMS switches, which are the most common switch types, classified according to their contact types.



(a) DC contact (OFF state) (b) DC contact (ON state)

(c) Capacitive contact (OFF state) (d) Capacitive Contact (ON state)

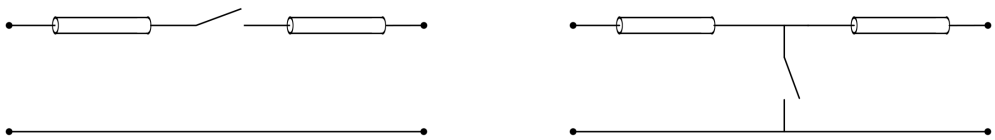
Figure 2.1: RF MEMS switch examples in terms of their contact types.

Considering the DC contact switches in Figure 2.1 (a) and Figure 2.1 (b), when the switch is in OFF state the RF signal cannot be transferred through signal line owing to lack of

electrical connection. In the ON state, the electrical connection is established via MEMS bridge and in this state RF signal is allowed to pass. From a circuit point of view in the ON state, the contact can be modeled by the contact resistance, which is why DC contact switches can operate near DC frequencies. Capacitive contact switches in Figure 2.1 (c) and Figure 2.1 (d) on the other hand, have a different operation type. When the switch is in ON state the MEMS bridge is in upstate position and due to low coupling capacitance between the bridge and the signal line, RF signal can be transferred with insignificant disturbance. The MEMS bridge is in downstate position in the OFF state and due to increased coupling capacitance between the bridge (ground) and the signal line, RF signal is not allowed to pass. Capacitive contact type switches cannot operate properly near DC frequencies since the coupling mechanism will fail.

2.1.1.2 Circuit Configuration Types

RF MEMS switches are constructed on top of transmission lines as they can be used to prevent or allow the electrical signals to pass through. Since they are fabricated using planar micro-fabrication processes, transmission lines have been chosen to be either CPW lines or microstrip lines. From a circuit point of view every transmission line needs a signal line and a reference ground line which leads to two types of circuit configurations automatically. In order to allow or prevent the signal flow, RF MEMS switches may be constructed on the signal line which happens to be a series connection or may be constructed between the signal and ground lines which happens to be the shunt connection. Figure 2.2 indicates the two circuit configuration types.



(a) Series Configuration (b) Shunt Configuration

Figure 2.2: Circuit configurations for RF MEMS switch.

In series configuration when the switch is ON state (closed position) RF signal can be transferred through the transmission line. On the other hand, when the switch is in OFF state (open position) it prevents the RF signal to pass through. In shunt configuration, situation is the exact opposite; when the switch is in ON state, RF signal cannot pass through the transmission line since its grounded and when the switch is in OFF state, RF signal can be transferred through the line.

2.1.1.3 Actuation Mechanism Types

RF MEMS switches owe their functionality in RF domain to their sub-millimeter sized movable parts. ON and OFF states of the switch are achieved by moving these movable parts. These movements in RF MEMS switches are achieved by electrostatic, piezoelectric, electrothermal and magnetic actuation mechanisms. Among these mechanisms, electrostatic actuation is the most favored, due to the fast response times, rather smaller size and almost zero power consumption of the switches. Since MEMS switches considered in this study have electrostatic actuation mechanisms, it is better to investigate its properties a little deeper.

Shunt, capacitive contact switch structure, whose OFF and ON states have been indicated in Figure 2.1 (c) and Figure 2.1 (d) respectively, is an example for an electrostatically actuated switch. MEMS bridge can be collapsed by applying a DC potential difference between the signal trace and ground planes of the CPW line which is the MEMS bridge

itself. Generated electric field between the bridge and the signal trace of the CPW line will cause a force to be exerted on the bridge. When this force is strong enough to overcome the mechanical stiffness of the MEMS bridge, the bridge will collapse. This phenomenon is known as the pull-in phenomenon and the minimum potential difference applied between the signal trace and ground planes of the CPW line to collapse the bridge is defined as pull-in voltage (V_{PI}).

To sup up, when a potential difference greater than or equal to V_{PI} is applied between the signal trace and the MEMS bridge, the bridge will collapse and the switch will be in OFF state. When the potential difference is smaller than V_{PI}, MEMS switch will be in ON state.

2.1.2 Considered SPST RF MEMS Switches in This Study

In the light of expressed classifications for an RF MEMS switch in previous sections, considered switch structure can be put into words as a shunt, capacitive contact switch with an electrostatic actuation mechanism. In fact, Figure 2.1 (c) and Figure 2.1 (d) shows a rather simpler model of the considered switch.

Two switches have been considered in this study sharing the same switch structure. One of the switches has been designed for 12 GHz operating frequency and the other one is designed for 26 GHz operating frequency.

2.2 Electromagnetic Design of Devices Used in the SPDT Switch Configurations Including SPST Switches

The ultimate aim of this study was to design RF MEMS SPDT switches at 26 GHz and 12 GHz operating frequencies. Owing to the previously obtained experiences on shunt, capacitive contact switches in METU RF MEMS group, this type of switches have been utilized as the main building blocks for the SPDT designs. In addition to the SPST

switches, a CPW T-junction, two CPW 90º Bend designs and two MIM capacitors for each design were required. Electromagnetic design steps will be presented separately for each building block, after explaining the SPDT switch structures.

2.2.1 Structure of the SPDT Switches

A simplified circuit model is presented in this part in Figure 2.3, in order to demonstrate the operating principle of the SPDT switch structure utilized in this study.

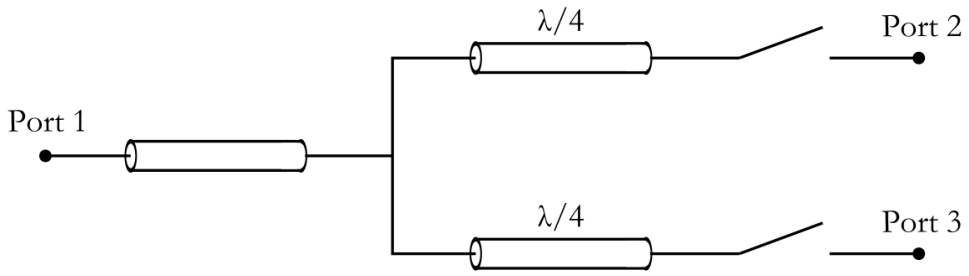


Figure 2.3: Simplified circuit model of SPDT switch structure

As depicted, the circuit model in Figure 2.3 is rather a simplified version. It did not include the CPW 90º Bend structures, CPW T-junction or MIM DC blocking capacitors. However, this model may give the basic idea behind the design. The transmission lines on branches of Port 2 and Prot 3 have an electrical length of λ/4 on the operating frequency and the switches seen on the model are shunt, capacitive contact MEMS switches. It has been mentioned in the previous sections of this chapter that, when a shunt, capacitive contact switch will be in its OFF state, which was shown Figure 2.1 (c), the MEMS bridge will be in downstate position and there will be an RF virtual short circuit on the signal trace of the CPW line. This short circuit will be transferred as a virtual open circuit to the T-connection and the power will not be allowed to go into that branch. By this method it is possible to

choose the path of the RF signal and transfer it out from one of the output ports selectively. A more detailed explanation will be given about the operation principles of the SPDT switch structure after examining each building block separately.

In order to have a better understanding of SPDT structure, Figure 2.4 demonstrates one of the designed and fabricated SPDT switches. Building blocks are also indicated separately on the micrograph.

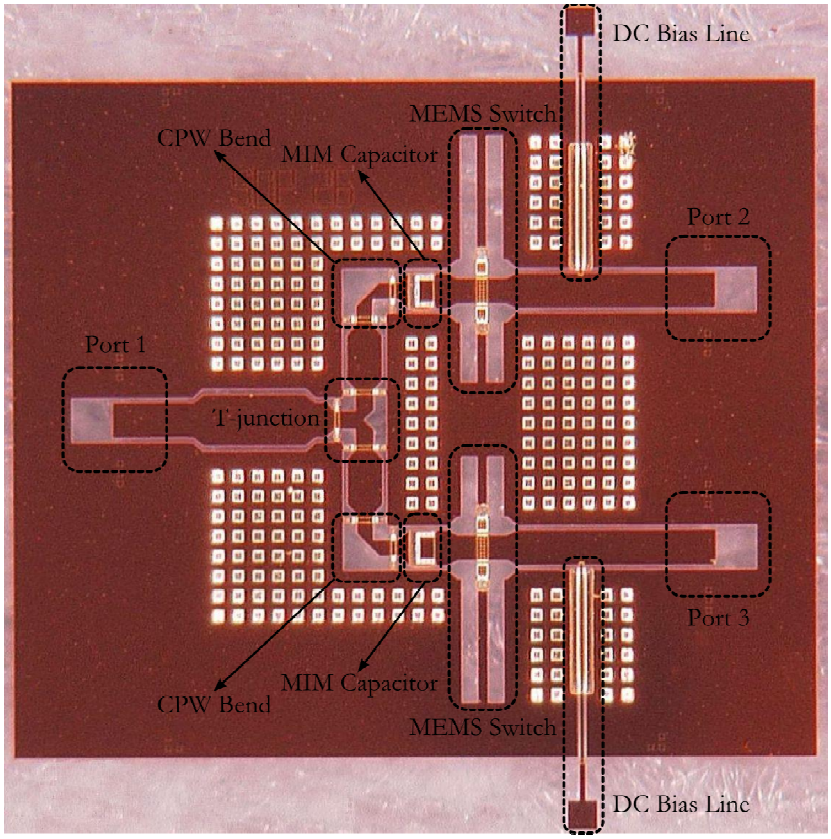


Figure 2.4: One of the designed and fabricated SPDT switch (building blocks are indicated)

2.2.2 Electromagnetic Design of RF MEMS Switches

In this section, electromagnetic designs of the two shunt, capacitive contact switches are investigated for operating frequencies 26 GHz and 12 GHz. The design parameter values will be given separately for each design, under the same titles. To begin with, electromagnetic design specifications of the switches will be given. After that, layouts and circuit models of the switches will be presented. Then, fabrication steps will be covered and finally measurement results will be given including the verification of for the RF MEMS switches.

2.2.2.1 Electromagnetic Design Specifications

Electromagnetic design step has been started based on some design specifications and it is aimed to obtain a SPDT switch coherent with these attributes. ON states and OFF states of the switches have different specifications which can be found in Table 2.1 and Table 2.2 for 26 GHz and 12 GHz designs, respectively.

Table 2.1: Design specifications for RF MEMS switch for 26 GHz operating frequency

STATE	SPECIFICATIONS
ON	Return Loss better than 15 dB in a 5 GHz band around 26 GHz, Insertion Loss better than 0.5 dB in a 5 GHz band around 26 GHz
OFF	Isolation better than 20 dB at 26 GHz

Table 2.2: Design specifications for RF MEMS switch for 12 GHz operating frequency

STATE	SPECIFICATIONS
ON	Return Loss better than 15 dB in a 3 GHz band around 12 GHz, Insertion Loss better than 0.5 dB in a 3 GHz band around 12 GHz
OFF	Isolation better than 20 dB at 12 GHz

2.2.2.2 Layout and Circuit Model of the Switches

Layout drawing of the shunt, capacitive contact switch, whose specifications are given in Table 2.1 and Table 2.2, can be seen in Figure 2.5. Despite being the layout of a shunt, capacitive contact switch such as Figure 2.1 (d), the drawing in Figure 2.5 has some differences and is more complicated.

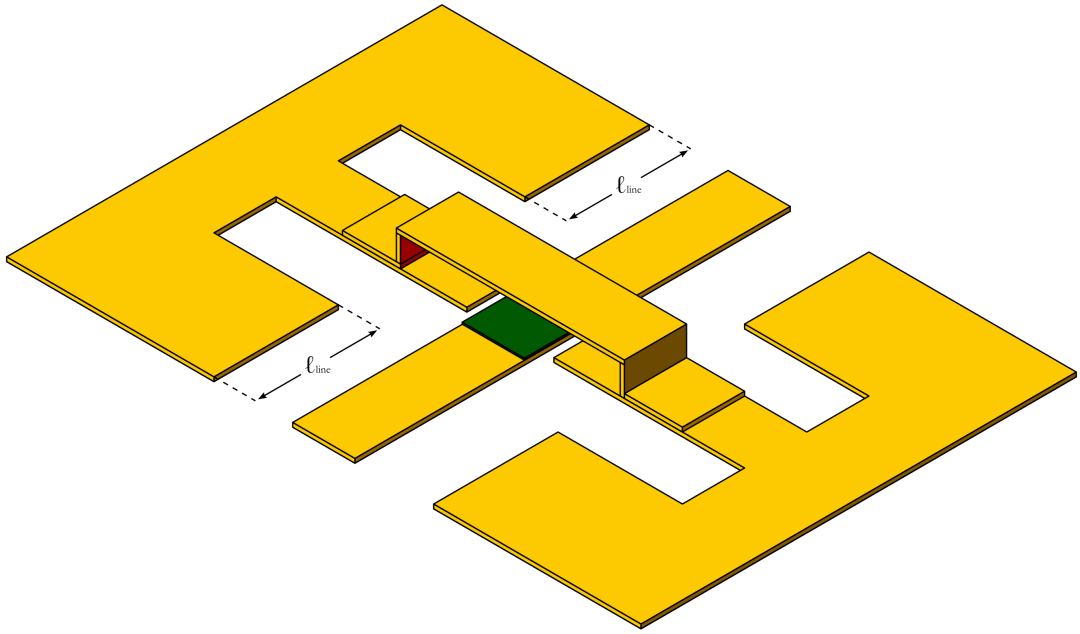


Figure 2.5: Layout of shunt, capacitive contact SPST MEMS switch

The first thing to be noticed is the recesses near the MEMS bridge legs, which extends into the ground planes of the CPW line. These recesses are used for *inductive tuning* and their purpose will be explained in detail in the following sections. In addition to the recesses, anchors of the MEMS bridge have extensions towards the signal trace of the CPW line. This so called "*anchor extensions*" will be given some attention in the following sections as well.

Constituting a circuit model for the MEMS switches is significant because this approach makes it possible to use circuit simulators instead of electromagnetic simulators, which require more effort and time for the simulations. Especially the SPDT structures utilized in this study are too large in this sense, for which it is not possible for the EM simulators to give accurate results. Rather than trying to solve the whole problem in an EM simulator, circuit models of the switches were constructed and rest of the study is attended by the use of these circuit models. Figure 2.6 indicates the utilized circuit model.

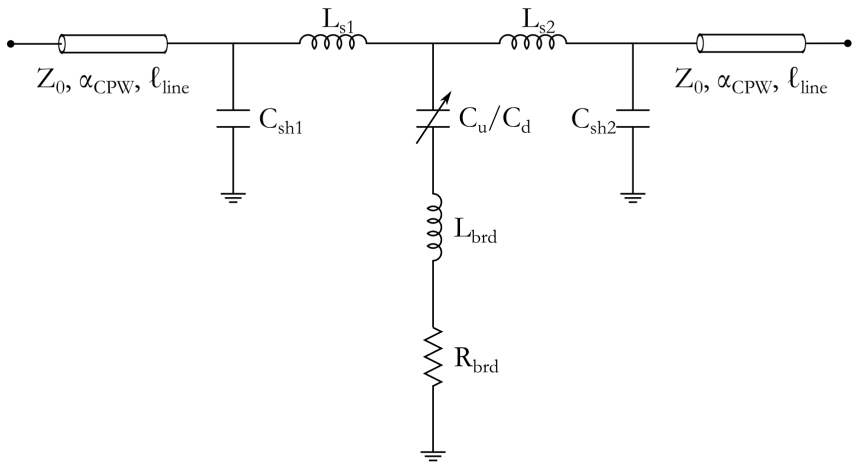


Figure 2.6: Circuit model of the shunt, capacitive contact SPST RF MEMS switch

Utilized circuit model is an advanced version of the common CLR circuit model [7] of a shunt, capacitive contact RF MEMS switch. RF MEMS switch model consists of C_{sh1}, C_{sh2}, L_{s1} and L_{s2} which accounts for the step discontinuities on the recess interfaces [40] and two short transmission line segments, whose lengths (ℓ_{line}) are shown in Figure 2.5, on the series branches. C_{sh1}, C_{sh2} and L_{s1}, L_{s2} are chosen to have different values due to a possible nonsymmetry between the recesses on different ground planes, which will be the case for the designed switch at 26 GHz due to physical layout problems in the SPDT switch design. Shunt branch consists of a two state variable capacitor, an inductor and a resistor. C_u and C_d

are abbreviation of upstate and downstate capacitances for the switch. L_{brd} and R_{brd} are abbreviations of bridge inductance and bridge resistance, respectively. Shunt branch models the MEMS bridge and the electrical components denote the values originated from the bridge itself.

2.2.2.3 Design Methodology

Design methodology can be investigated under three subtitles such as CPW transmission line design, return loss optimization in upstate and isolation optimization by inductive tuning in downstate.

2.2.2.3.1 CPW Transmission Line Design

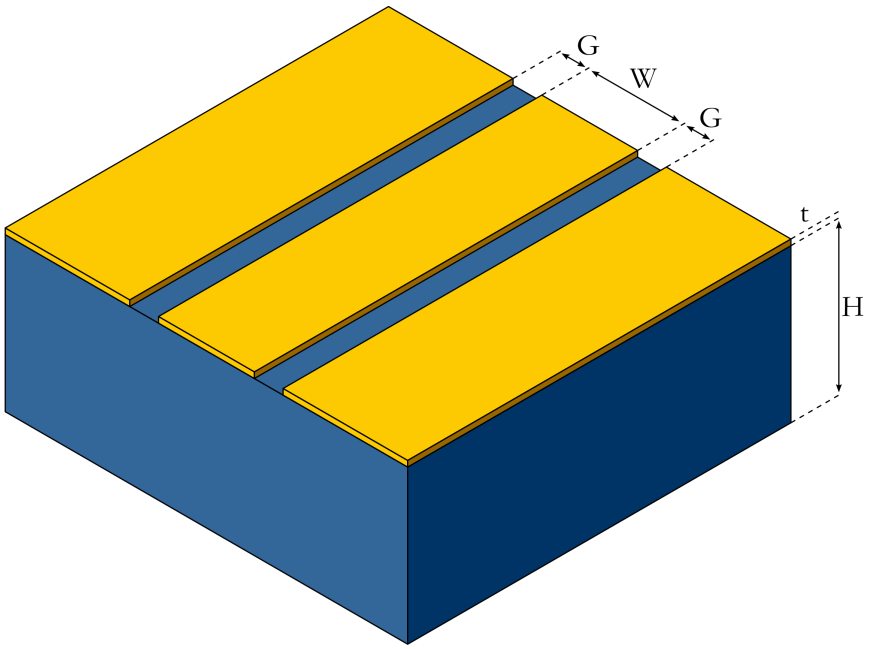


Figure 2.7: CPW transmission line and dimensions

Since shunt, capacitive contact RF MEMS switches are constructed on CPW transmission lines, modeling the line by finding its characteristic impedance (Z_0), electrical length at operating frequency (ℓ_{line}) and attenuation constant is prior and a significant step. Figure 2.7 indicates the physical dimensions of a CPW transmission line on a substrate. Required formulation in order to calculate the characteristic impedance of a conductor-backed CPW transmission line is provided below [41]:

$$Z_0 = \frac{60\pi}{\sqrt{\epsilon_{eff}}} \frac{1}{\frac{K(k_1)}{K(k_1')} + \frac{K(k_2)}{K(k_2')}} \tag{2.1}$$

where,

$$k_1 = \frac{\tanh(\pi W/4H)}{\tanh(\pi(W+2G)/4H)} \tag{2.2}$$

$$k_1' = \sqrt{1-k_1^2} \tag{2.3}$$

$$k_2 = \frac{W}{W+2G} \tag{2.4}$$

$$k_2' = \sqrt{1-k_2^2} \tag{2.5}$$

$$\epsilon_{eff} = 1 + q(\epsilon_R - 1) \tag{2.6}$$

$$q = \frac{\frac{K(k_1)}{K(k_1')}}{\frac{K(k_1)}{K(k_1')} + \frac{K(k_2)}{K(k_2')}} \tag{2.7}$$

W, G and H are physical dimensions of the CPW transmission line structure which are indicated in Figure 2.7, ϵ_R is the relative permittivity of the substrate and K(k) is the complete elliptic integral of first kind. W and G values differs for the two designs, however H is 500 μm and ϵ_R is 3.8, which are fixed values.

G and W values of the CPW transmission line for the 26 GHz design has been chosen to be 90 μm and 130 μm. Characteristic impedance and effective permittivity for the 26 GHz design are found to be 85.9 Ω and 2.38, respectively.

On the other hand, G and W values for the 12 GHz design have been chosen to be 150 μm and 220 μm which lead to a characteristic impedance of 86.2 Ω. Effective permittivity in this case is calculated to be 2.34.

Attenuation constant of a CPW transmission line (α_{CPW}) have two components; one of them is due to conductor losses (α_C) and the second one is for dielectric losses (α_D), where:

$$\alpha_{CPW} = \alpha_C + \alpha_D \tag{2.8}$$

Formulations for the two components are available in the literature [41], however it has been observed that these formulations underestimates the real values. Most convenient way seems to be extracting α_{CPW} from the EM simulation results.

2.2.2.3.2 Switch Modeling in the Upstate

Return loss should be minimized at the desired operating frequency in the upstate (ON state) of a shunt, capacitive contact RF MEMS switch.

In order to explain the design procedure for the upstate of the switches, loading effect of the shunt, capacitive contact MEMS switches should be investigated. This type of switch loads the CPW transmission line capacitively due to the capacitance between the bridge and the signal trace. Figure 2.8 shows the general lumped element circuit model of a transmission line segment, which is the CPW line in our case.

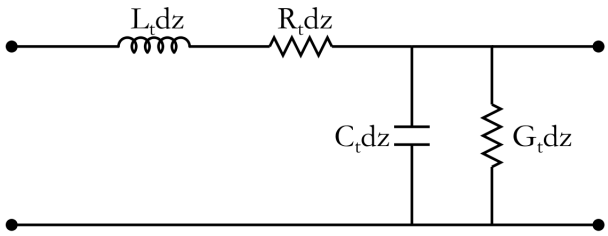


Figure 2.8: Lumped element circuit model of a transmission line

For the case of a shunt, capacitive contact switch, the transmission line will be loaded by a shunt capacitance. Furthermore, low loss assumption may be made and loss components may be ignored for simplicity. The resulting circuit model for a short section ($s \ll \lambda$) of a loaded transmission line with a length of s can be seen in Figure 2.9.

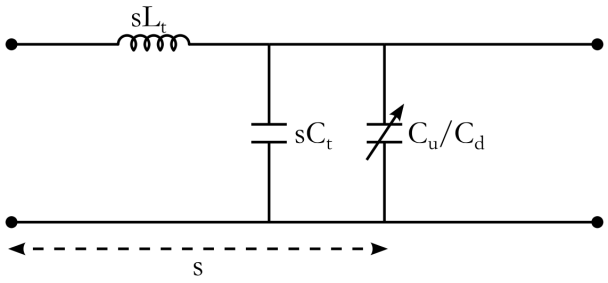


Figure 2.9: Simplified lumped element circuit model of a capacitively loaded transmission line with low loss assumption

After the low loss assumption, unloaded transmission line characteristic impedance may be approximated as:

$$Z_0 \cong \sqrt{\frac{L_t dz}{C_t dz}} = \sqrt{\frac{L_t}{C_t}} \tag{2.9}$$

The loaded line impedance, whose circuit model is indicated in Figure 2.9, may be calculated as follows:

$$Z_L = \sqrt{\frac{sL_t}{sC_t + C_u}} \tag{2.10}$$

where C_u is the upstate capacitance of the RF MEMS switch.

By a comparison between (2.9) and (2.10), loaded line impedance (Z_L) will be smaller than unloaded line impedance (Z_0) and loading will take part by the effect of the upstate

capacitance of the switch. Therefore, by selecting a high Z_0 and appropriate upstate capacitance, Z_L may be tuned to be close to 50 Ω reference impedance at the desired operation frequency and return loss can be minimized.

2.2.2.3.3 Switch Modeling in the Downstate

Isolation should be optimized for the downstate (OFF state) of a shunt, capacitive contact RF MEMS switch.

Standard RF MEMS fabrication process cycle fixes some of the variables for the devices. Sacrificial layer thickness and dielectric layer thickness are two of them. In addition to these, upstate capacitance is fixed in the optimization of ON state return loss. If the circuit model of the switch in Figure 2.6 is considered, only variable remaining for optimizing OFF state isolation is the bridge inductance (L_{brd}). By tuning bridge inductance resonance frequency of the switch may be tuned to the desired operation frequency which will maximize the isolation. This method is called inductive tuning and the bridge inductance can be controlled by recesses extending into the ground planes near the bridge.

Recess dimensions may be obtained after finding the required bridge inductance from the circuit model by sweeping this variable in the circuit simulations.

During the downstate design of the switches, partial contact approach is utilized. In this approach the contact area of the downstate capacitance is decreased intentionally in the EM simulations. By this approach, it is aimed to lower the actuation voltages and obtain an ability to tune the resonance frequency by tuning actuation voltage during the measurements. The procedure for this approach has been explained and can further be investigated in [14]. η defined in [14] has been chosen as 25 μm for 26 GHz design and 50 μm for the 12 GHz design.

After applying the design procedure in both upstate and downstate of the MEMS switches, electromagnetic simulation results have been curve fitted with the circuit model simulations and circuit model parameters have been extracted. The circuit model parameters appearing in Figure 2.6, can be seen in Table 2.3 and Table 2.4 for 26 GHz design and for 12 GHz design, respectively.

Table 2.3: Circuit model parameters for the RF MEMS switch designed for 26 GHz operating frequency

Parameter	Value
Z_0	85.9 Ω
C_u	62.7 fF
C_d	423.3 fF
L_{brd}	90.1 fF
R_{brd}	0.41 Ω
L_{s1}	201 nH
L_{s2}	201.2 nH
C_{sh1}	9.7 fF
C_{sh2}	10.5 fF
ℓ_{line}	810 μm

Table 2.4: Circuit model parameters for the RF MEMS switch designed for 12 GHz operating frequency

Parameter	Value
Z_0	86.2 Ω
C_u	156.9 fF
C_d	1056 fF
L_{brd}	90.1 fF
R_{brd}	0.36 Ω
L_s	366.8 nH
C_{sh}	17.4 fF
ℓ_{line}	1760 μm

It must be noted that, L_s and C_{sh} parameters differs in the two series branch for the 26 GHz design due to nonsymmetry between recesses.

2.2.2.3.4 CPW Transition Integrations

Probes utilized in the RF measurements have 220 μm ground-to-ground spacing in METU Electrical and Electronics Department. Therefore, it is necessary to have the exact spacing at the ports of the designed switches or any other MEMS devices. In order to accomplish this necessity linear CPW transitions are utilized. Loading effect of the bridge has been explained in the previous sections, where Z_L has been tuned to have an impedance value close to 50 Ω reference impedance. Thus it is practical to choose the CPW line impedance close to 50 Ω reference impedance at the ports of the switches. By assuming a ground to ground spacing of 220 μm and using the formulations from (2.1) to (2.5), G and W values have been chosen to be 20 μm and 180 μm for both 26 GHz and 12 GHz designs which leads to a 52 Ω characteristic impedance.

Figure 2.10 and Figure 2.11 indicates the micrographs of fabricated RF MEMS switches for 26 GHz and 12 GHz operating frequencies. In Figure 2.10, significant physical dimensions are shown, whose values are tabulated in Table 2.5 and Table 2.6.

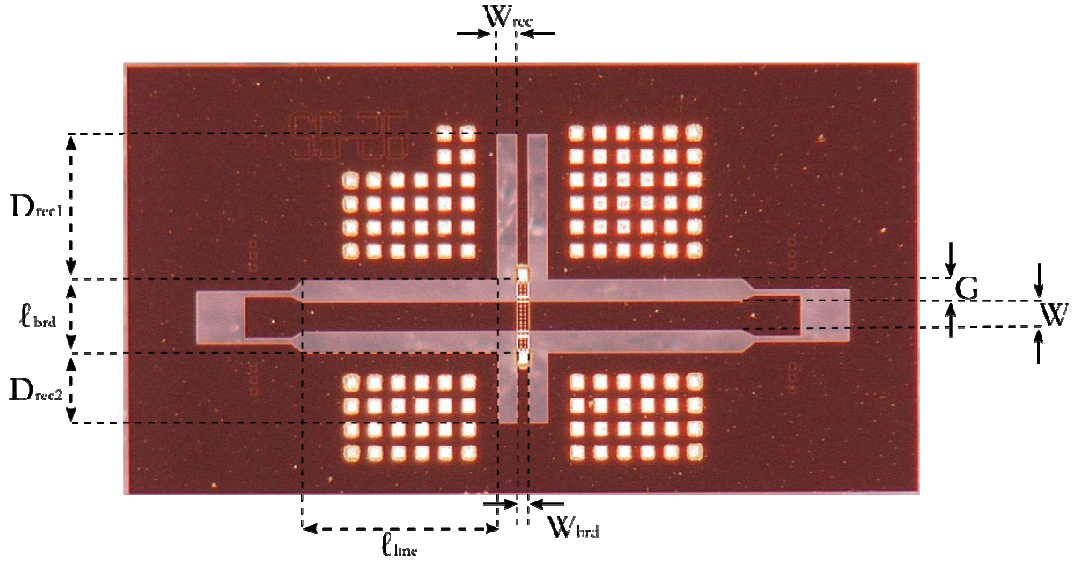


Figure 2.10: A micrograph of fabricated RF MEMS switch at 26 GHz operating frequency, physical dimensions are also defined

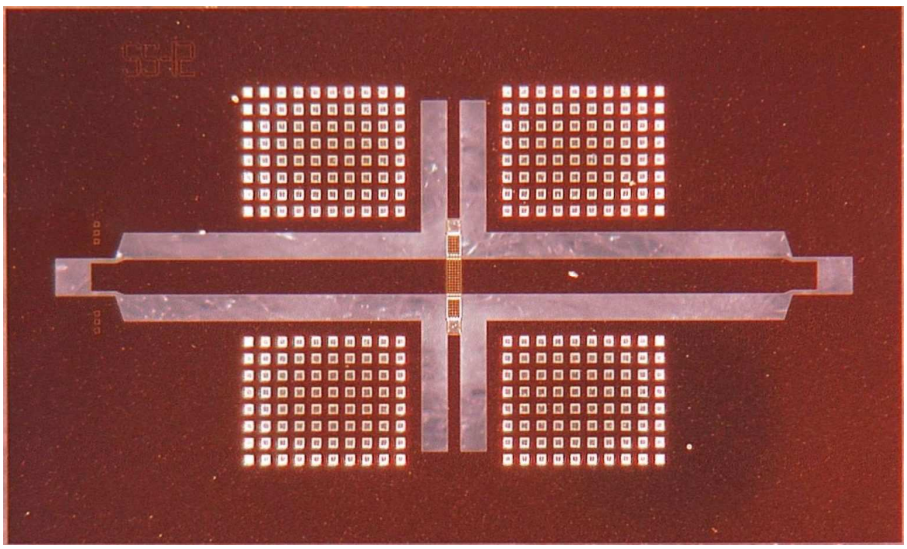


Figure 2.11: A micrograph of fabricated RF MEMS switch at 12 GHz operating frequency

Table 2.5: Physical dimensions of the RF MEMS switch at 26 GHz

Parameter	Value
W	130 μm
G	90 μm
W_{rec}	80 μm
D_{rec1}	620 μm
D_{rec2}	300 μm
W_{brd}	50 μm
ℓ_{brd}	310 μm
ℓ_{line}	830 μm

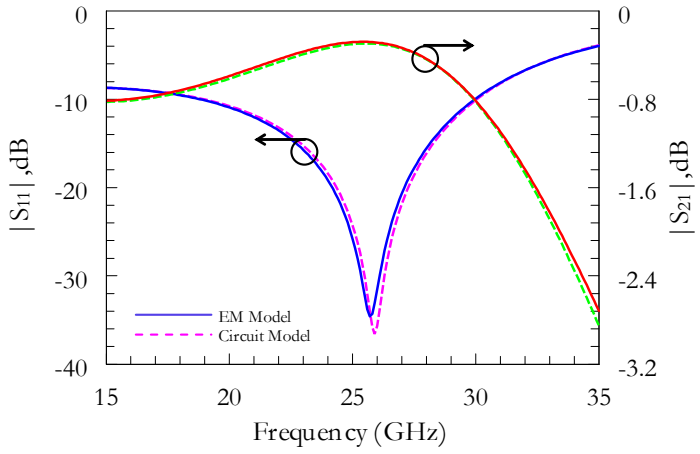
Table 2.6: Physical dimensions of the RF MEMS switch at 12 GHz

Parameter	Value
W	220 μm
G	150 μm
W_{rec}	150 μm
D_{rec}	775 μm
W_{brd}	80 μm
ℓ_{brd}	520 μm
ℓ_{line}	1760 μm

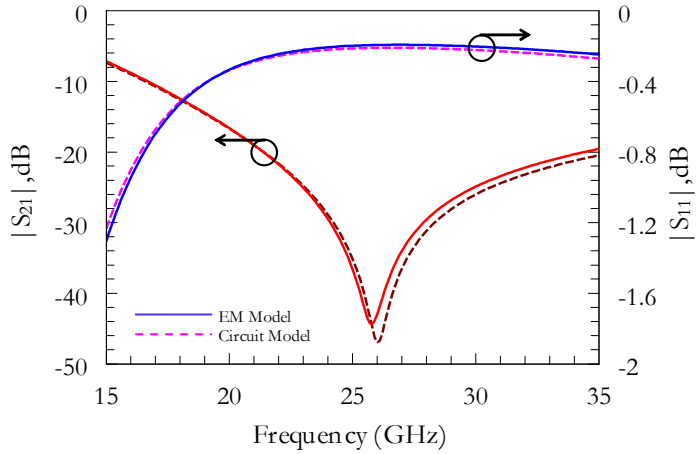
2.2.2.3.5 Obtained Switches at 26 GHz and 12 GHz and Their Responses

Table 2.3 and Table 2.4 indicate obtained circuit model parameters for the switches both at 26 GHz and 12 GHz. As mentioned before these parameters are obtained by curve fitting of circuit simulation results and electromagnetic simulation results. Ansoft HFSS™ v11 is used to perform the electromagnetic simulations and the circuit simulations have been made by the use of AWR Microwave Office™ 2006. After obtaining the circuit parameters, CPW transitions are added to the circuit model just by importing their EM simulations results and final circuit model, where fabricated switches can be simulated.

Figure 2.12 indicates obtained RF performances of the RF MEMS switch operating at 26 GHz both from EM simulations and circuit simulations. Consistency between EM and circuit simulation is noticeable.



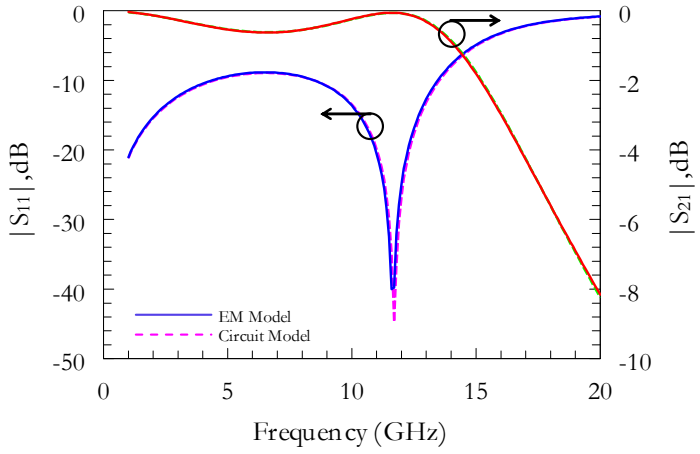
(a) upstate



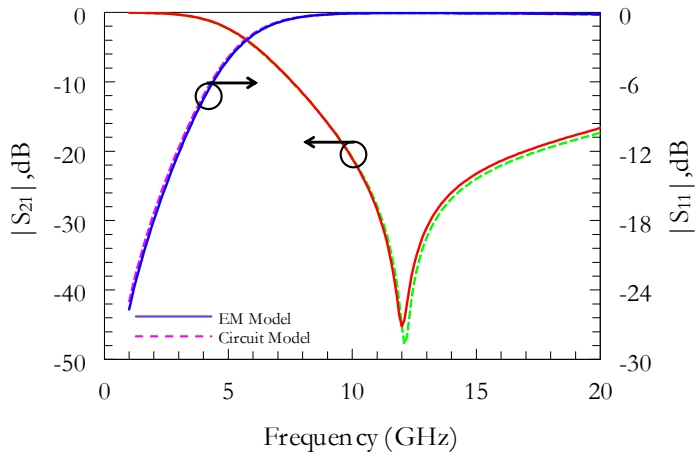
(b) downstate

Figure 2.12: Magnitude S-parameters obtained by electromagnetic and circuit simulations for the RF MEMS switch designed at 26 GHz

Figure 2.13 indicates obtained RF performances of the RF MEMS switch operating at 12 GHz both from EM simulations and circuit simulations. EM and circuit simulation results are consistent again.



(a) upstate



(b) downstate

Figure 2.13: Magnitude S-parameters obtained by electromagnetic and circuit simulations for the RF MEMS switch designed at 12 GHz

2.2.3 CPW T-junction Design

CPW T-junction design is an important part for the utilized SPDT structures. Since a T-junction includes several discontinuities, mode conversion takes place within the circuit. A simple method to suppress the excitation of the coupled slot-line mode is by maintaining electrical continuity between the ground planes of the circuit [41]. It is important in a T-junction design that its effects on the general circuit are minimized. A T-junction should behave as connection of three 50 Ω transmission lines [42].

Two CPW T-junctions have been designed in this study; one of them for the SDPT at 26 GHz and the second is for the SPDT at 12 GHz. By inserting air bridges in the vicinity of the T-junction ports, mode conversion and so power loss is prevented. Width of the utilized air bridges are chosen to be as small as possible in order to decrease the loading effects, however due to process limitations a lower bound encountered. Loading effect of the MEMS bridges on the transmission lines has been explained in detail in Section 2.2.2.3.2. This loading effect has been considered in the ports of T-junction designs, where the loaded line impedances are adjusted to be 50 Ω. Ground to ground spacing of the CPW transmission lines entering the T-junction ports are conserved through the T-junction and CPW line dimensions under the MEMS bridges are analytically calculated by considering the loading effects of the bridges by using Matlab™. In addition to these, notches are opened on the connection points of the two designs on the thru line directions. Dimensions of the notches are selected by comparing the EM simulation results, conducted in Ansoft HFSS™ v11. Obtained T-junction layouts for 26 GHz and 12 GHz operating frequencies are indicated in Figure 2.14, including abbreviations for the physical dimensions.

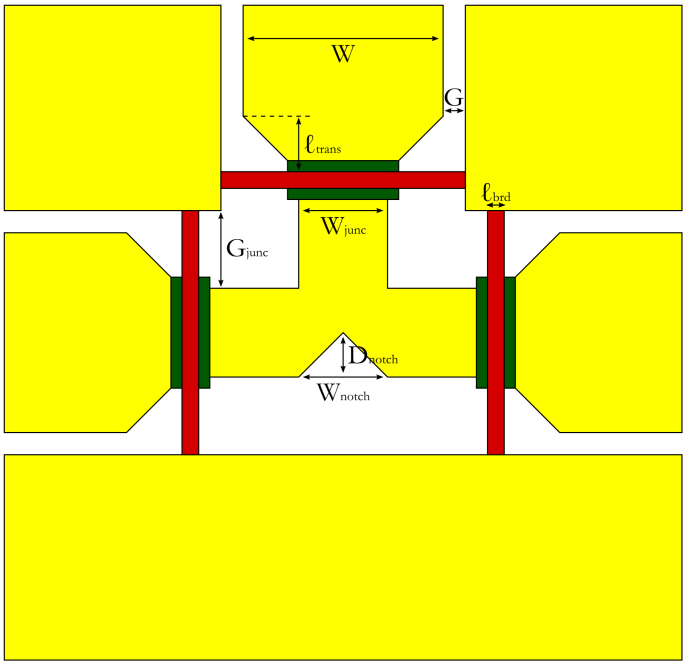


Figure 2.14: CPW T-junction layout and physical dimensions

Physical layout dimension appearing in Figure 2.14 are tabulated for both designs in Table 2.7 and Table 2.8.

Table 2.7: Dimensions of CPW T-junction design for 26 GHz operating frequency

Parameter	Value
W	180 μm
G	20 μm
ℓ_{brd}	15 μm
W_{notch}	94 μm
D_{notch}	50 μm
ℓ_{trans}	50 μm
W_{junc}	94 μm
G_{junc}	63 μm

Table 2.8: Dimensions of CPW T-junction design for 12 GHz operating frequency

Parameter	Value
W	260 μm
G	25 μm
ℓ_{brd}	15 μm
W_{notch}	110 μm
D_{notch}	50 μm
ℓ_{trans}	50 μm
W_{junc}	110 μm
G_{junc}	100 μm

2.2.4 CPW 90º Bend Design

Measurement setup, actually the probe stations, in METU Electrical and Electronics Department necessitates utilizing CPW 90º Bend structures in the SPDT designs. Without using these bends it would be impossible for the RF measurements to be done. Due to this necessity two CPW 90º Bend structures have been designed and utilized in the SPDT structures as building blocks.

As pointed out in the CPW T-junction design, discontinuities may give rise to unwanted electromagnetic modes and air bridges may be used for preventing these modes. CPW 90º Bend structures have discontinuities and in order to suppress the unwanted modes air bridges were used. Due to introduced air bridges, loading effects are taken into account, as in the CPW T-junction design section, CPW line dimensions are calculated in order to have loaded line impedance (Z_{loaded}) close to 50 Ω.

In addition to compensating for the reactances associated with the bend, chamfering provides a simple way to partially compensate for the effects of the air bridges [43]. Chamfering in the CPW 90º Bend structures in this study is optimized based on EM

simulations. Obtained CPW 90º Bend structure layouts and the abbreviations of the dimensions can be seen in Figure 2.15.

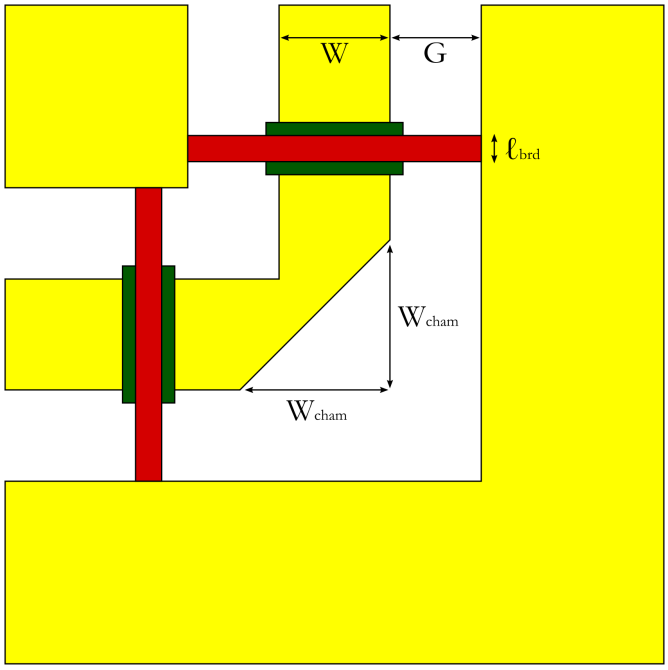


Figure 2.15: CPW 90º Bend layout and its dimensions

Physical layout dimension appearing in Figure 2.15 are tabulated for both designs in Table 2.9 and Table 2.10.

Table 2.9: Dimensions of CPW 90º Bend design for 26 GHz operating frequency

Parameter	Value
W	84 μm
G	68 μm
ℓ_{brd}	20 μm
W_{cham}	112 μm

Table 2.10: Dimensions of CPW 90º Bend design for 12 GHz operating frequency

Parameter	Value
W	110 μm
G	100 μm
ℓ_{brd}	15 μm
W_{cham}	110 μm

2.2.5 Inclusion of DC Bias Lines, DC Pads and CPW Transitions

In order to actuate shunt, capacitive contact switches, which provides the selectability between the output ports of SPDT switches; SiCr DC bias lines have been introduced into the SPDT designs. One end of DC bias lines are placed under the signal trace of the CPW line in the vicinity of MEMS switches, they extend through the ground planes of the CPW line and the other end connects to a DC pad. Since bias line extends through the ground plane, ground plane is separated into two parts. In order to prevent this, ground planes have been connected by the use of a MEMS bridge whose width is nearly as large as DC bias line length. Design of the DC bias lines has been done by EM simulations and these results have been included to the circuit model of the SPDT switches. It is seen that they did not affect the performance of the structure. EM model of the DC bias line structure can be seen in Figure 2.16. The dimensions are altered in order to indicate the structure better.

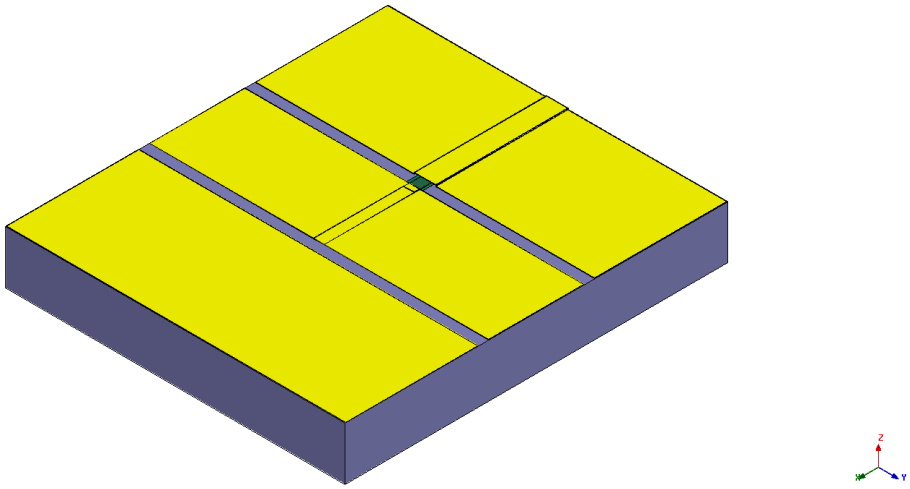


Figure 2.16: EM model utilized in the design of DC bias lines

Linear CPW transitions are integrated at all ports of the SPDT switches, for the measurement purposes. Reasoning behind this action is explained in Section 2.2.2.3.4.

2.2.6 Inclusion of DC Blocking MIM Capacitors

MIM capacitors were included in the SPDT design due to the actuation mechanism. In order to actuate the MEMS switches, DC bias lines were introduced into the circuitry and connected to the signal trace in the vicinity of the MEMS switches as pointed out in the previous section. Since bias lines are connected to the signal trace it is possible that actuation voltage may actuate the MEMS bridges on the CPW T-junction and the CPW 90º Bends which is not desired. This is prevented by adding two DC blocking MIM capacitors, one for each output branch. Capacitance value is chosen to be 2 pF for 26 GHz design and 4 pF for 12 GHz design.

2.2.7 Integration of Designed Building Blocks and SPDT Switches

Building blocks for the SPDT switches have been explained in a detailed manner so far. All of the building blocks were added to the circuit model as they are completed and final tunings are done by the use of the general model.

Figure 2.17 and Figure 2.18 indicate how building blocks are integrated and the final structure of the SPDT switch. It can be noticed that CPW 90º Bends are on the λ/4 lines and their electrical lengths are added to the lines. Due to this structure, electrical lengths of the λ/4 lines have been tuned in order to give the optimum response after the integration of CPW 90º Bends.

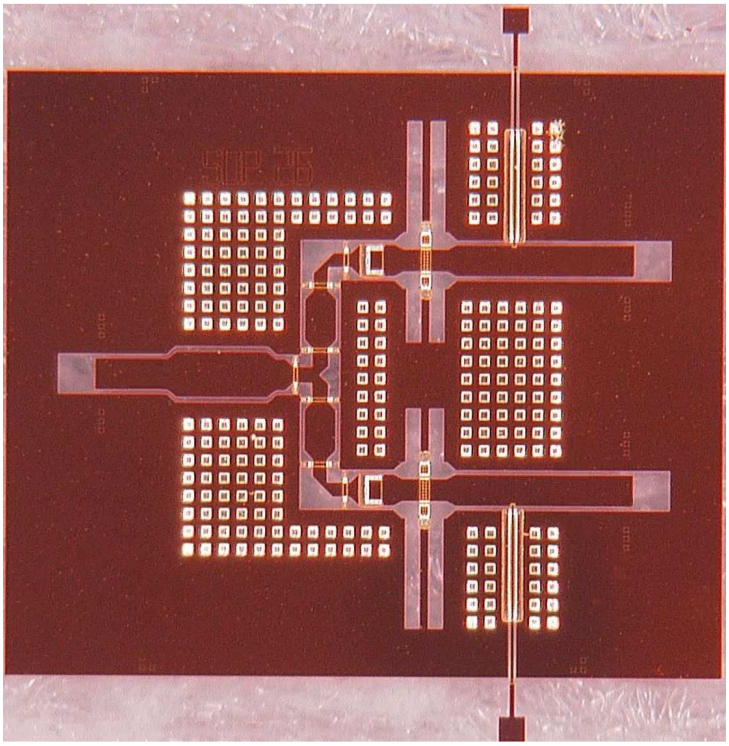


Figure 2.17: Designed and fabricated SPDT switch with 26 GHz operating frequency

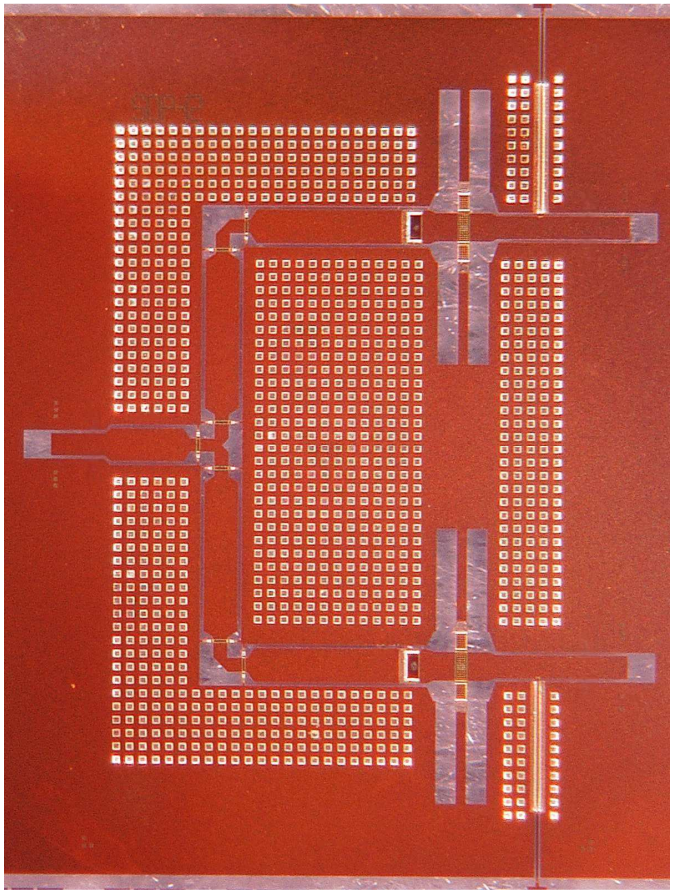


Figure 2.18: Designed and fabricated SPDT switch with 12 GHz operating frequency

During the circuit simulations for both SPDT switches, two assumptions are made and these assumptions are followed throughout the complete study in order to avoid confliction;

- RF MEMS switches on the upper branches, which is finalized with port 2, are actuated and they are in downstate position,
- RF MEMS switches on the lower branches, which is finalized with port 3, are not actuated and they are in upstate position.

For the 26 GHz design, return loss for the overall SPDT switch response is better than 20 dB between 23.77 GHz and 28.89 GHz. Furthermore, insertion loss at the operating frequency is lower than 0.5 dB and isolation is better than 30 dB in a 4 GHz band around 26 GHz. Obtained responses for the SPDT switch at 26 GHz can be seen in Figure 2.19.

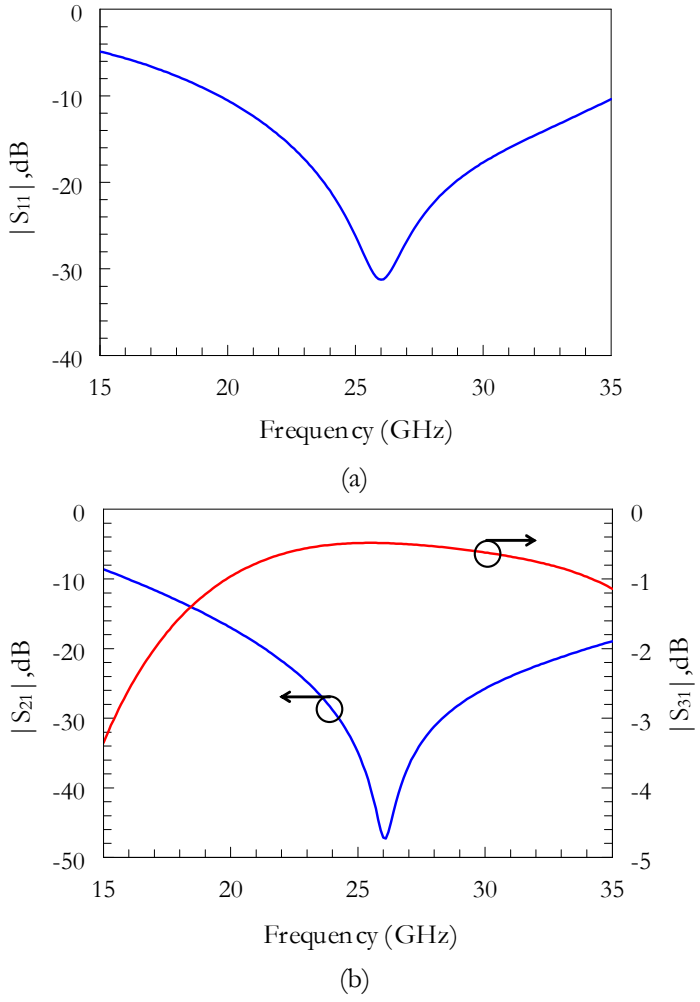


Figure 2.19: Circuit simulation responses for the SPDT switch operating at 26 GHz

For the 12 GHz design, return loss for the overall SPDT switch response is better than 20 dB between 10.87 GHz and 13.17 GHz. Furthermore, insertion loss at the operating frequency is lower than 0.6 dB and isolation is better than 30 dB in a ~2 GHz band around 12 GHz. Obtained responses for the SPDT switch at 12 GHz can be seen in Figure 2.20.

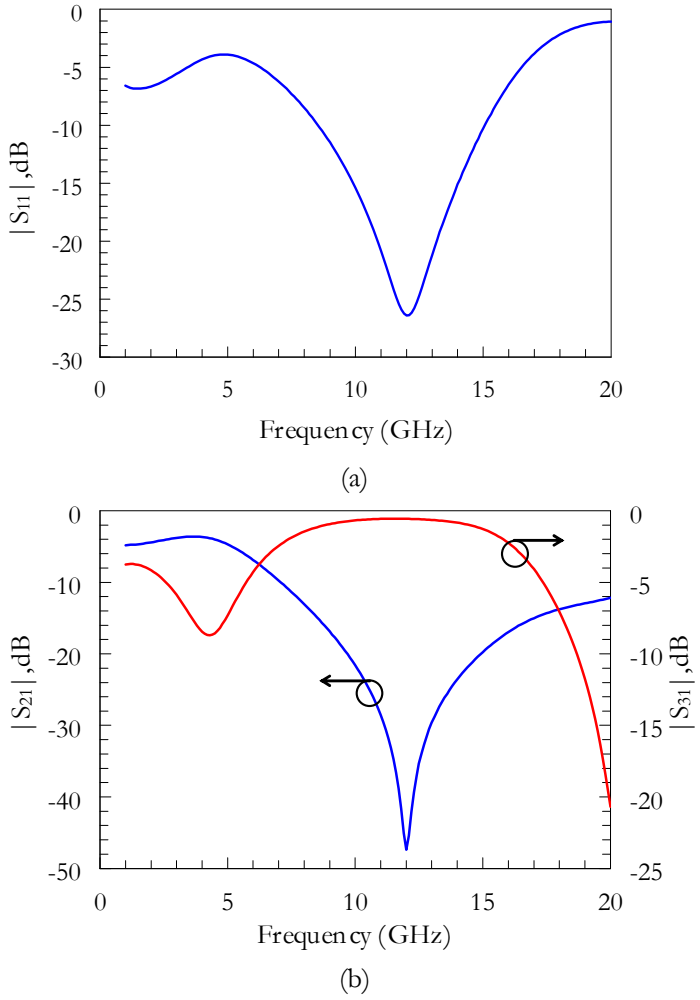


Figure 2.20: Circuit simulation responses for the SPDT switch operating at 12 GHz

2.3 Fabrication of the Devices

Designed RF MEMS SPDT switches are fabricated on a quartz substrate with 500 μm thickness by an in-house micro fabrication process cycle developed by METU RF MEMS group. Developed process cycle requires seven masks to be used and based on surface micromachining techniques. Every step of the process cycle and their detailed explanations are itemized and can be found under the following title. Following the detailed explanations figures indicating these steps are provided for better visualization. In these figures, process steps of a shunt, capacitive contact SPST switch have been chosen for demonstration.

2.3.1 Detailed Explanations of Process Steps

i) Resistive SiCr layer is sputtered on the top surface of a blank quartz wafer. This layer is patterned with a photolithography step in order to obtain DC bias lines. Figure 2.21 and Figure 2.22 indicate these steps. (t_{SiCr} = 0.2 μm)

ii) Ti/Au layer is sputtered on top of patterned SiCr layer as the first metallization. First metallization layer has been patterned in order to obtain CPW line traces and recesses utilized for the inductive tuning. Figure 2.23 and Figure 2.24 describe these steps. (t_{Ti} = 30 nm, t_{Au1} = 1 μm)

iii) Insulative Si_xN_y is deposited on top of first metallization by PECVD (Plasma Enhanced Chemical Vapor Deposition) method and patterned in order to obtain the dielectric layer under the MEMS bridges. Figure 2.25 and Figure 2.26 show these steps. (t_{SiN} = 0.3 μm)

iv) Polyimide sacrificial layer is coated by spin coating method and patterned in order to have anchor openings. Figure 2.27 and Figure 2.28 indicate these steps.

v) Second or structural gold metallization layer is sputtered on top of the polyimide sacrificial layer. This layer will form the MEMS bridges after patterning in the following steps. For the electroplating step a PR (photoresist) layer is spin-coated and patterned on top of structural metal layer. Figure 2.29 and Figure 2.30 show these steps. (t_{Au2} = 1.2 μm).

vi) Gold is electroplated on top of the anchor points of the MEMS bridges in order to enhance mechanical stiffness and then photoresist is stripped. Figure 2.31 demonstrates the result of this step. (5 μm ≤ t_{Au3} ≤ 10 μm)

vii) Structural metallization layer is patterned and MEMS bridges are formed. Figure 2.32 shows the results after this step.

viii) Sacrificial polyimide layer is etched away and the MEMS switches have been released afterwards which can be seen in Figure 2.33.

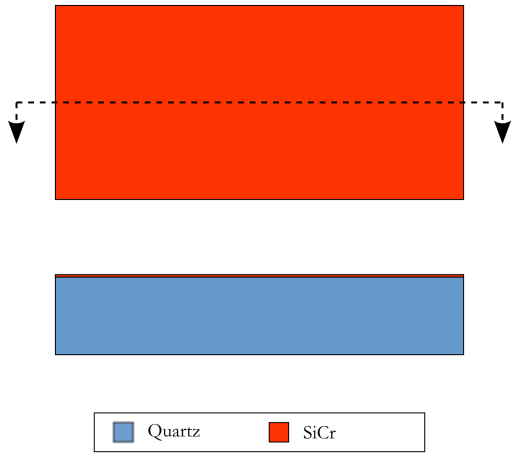


Figure 2.21: 0.2 μm thick SiCr layer is sputtered on blank quartz substrate

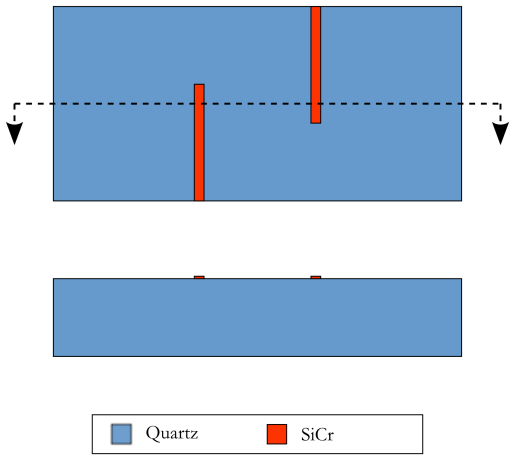


Figure 2.22: Sputtered SiCr layer is patterned

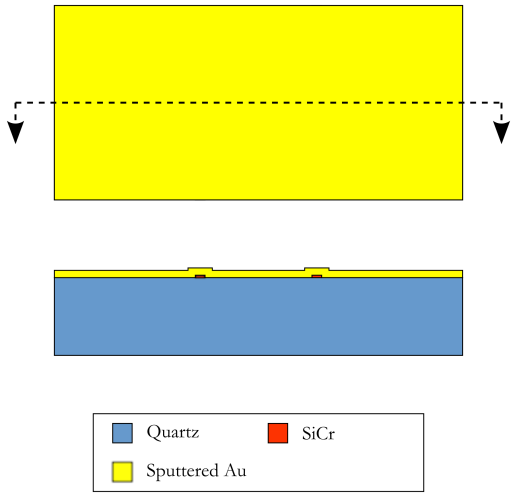


Figure 2.23: 30 nm Ti and 1 μm Au layer is sputtered on patterned SiCr layer. (Ti is not shown on the figure since its thickness is insignificant compared to other layers)

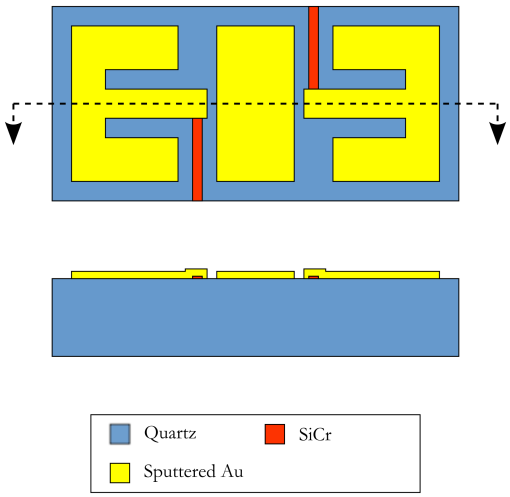


Figure 2.24: Sputtered Ti and Au layers are patterned

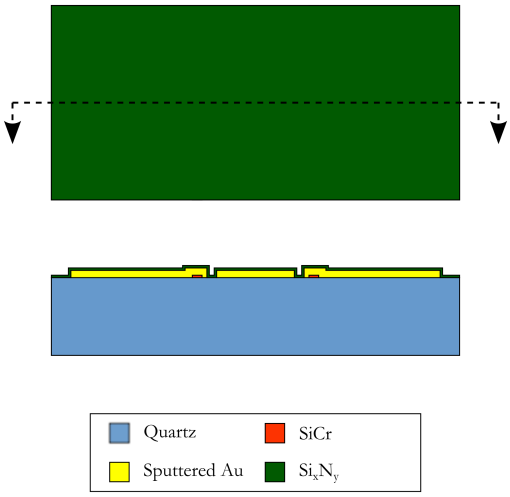


Figure 2.25: 0.3 μm Si_xN_y layer is deposited on patterned first gold metallization layer

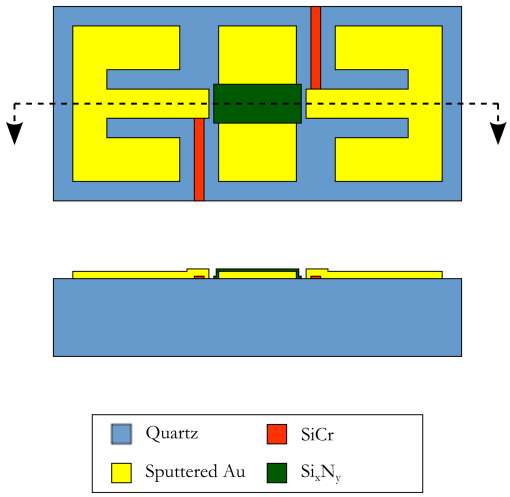


Figure 2.26: Deposited Si_xN_y layer is patterned

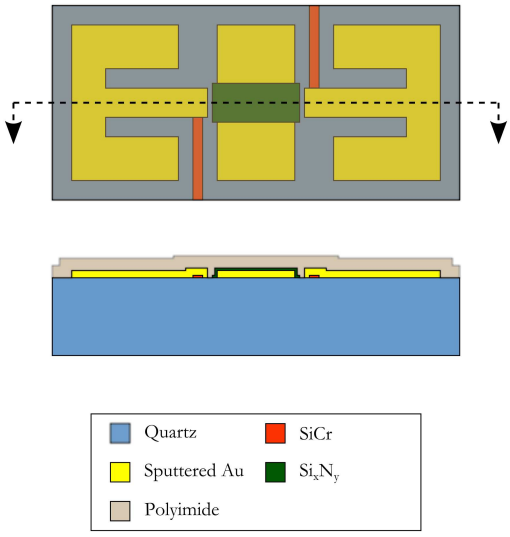


Figure 2.27: Polyimide sacrificial layer is spin-coated on top of pre-patterned layers

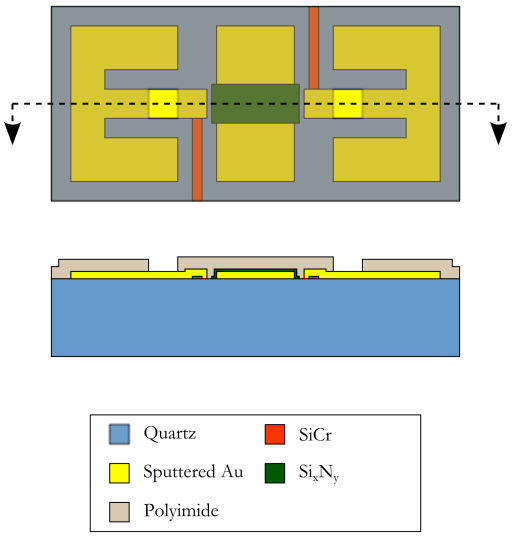


Figure 2.28: Polyimide sacrificial layer is patterned

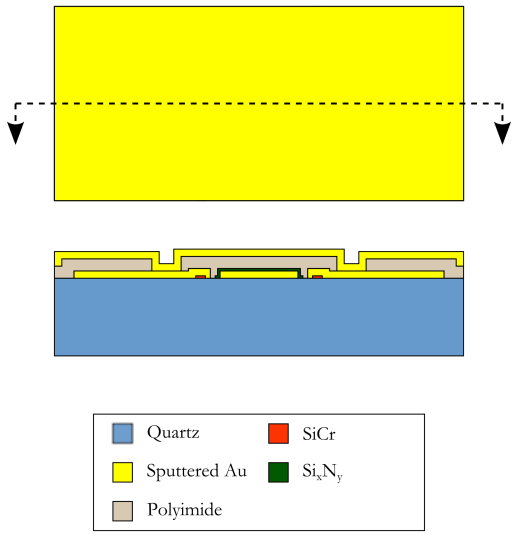


Figure 2.29: Structural metal layer sputtered on top of polyimide layer

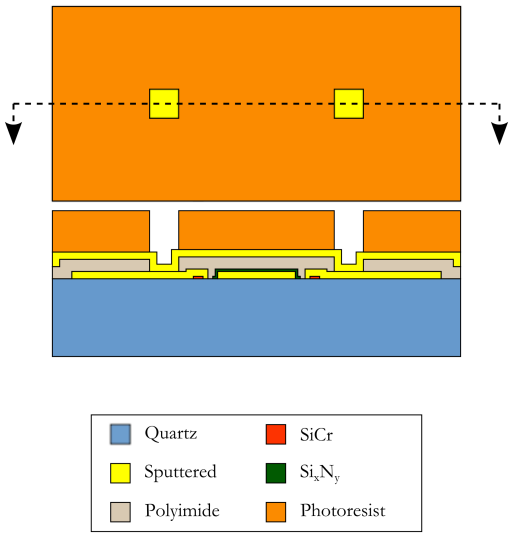


Figure 2.30: Photoresist spin-coated and patterned for gold electroplating

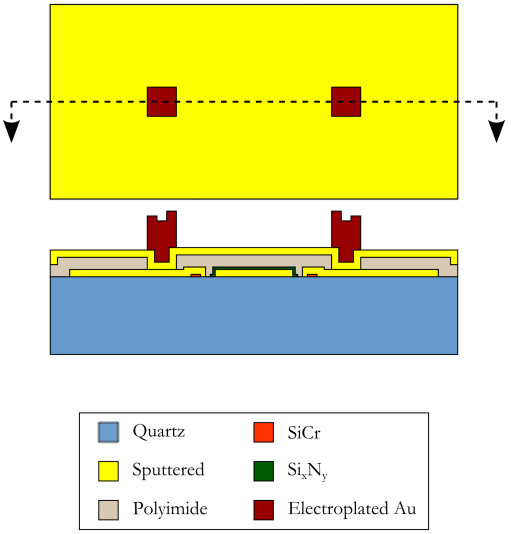


Figure 2.31: Gold electroplating is completed and photoresist is stripped

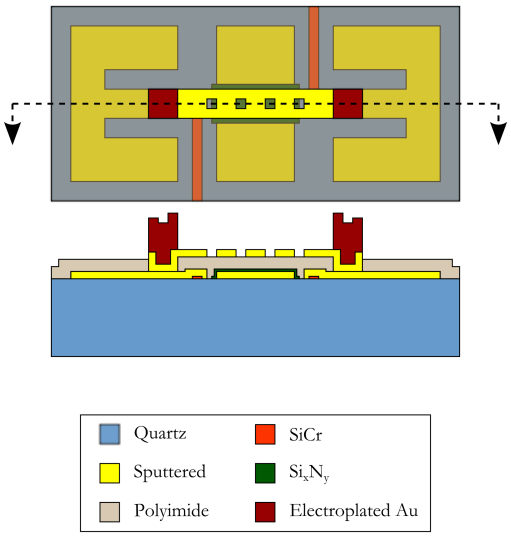


Figure 2.32: Structural gold layer is patterned and MEMS bridges are formed

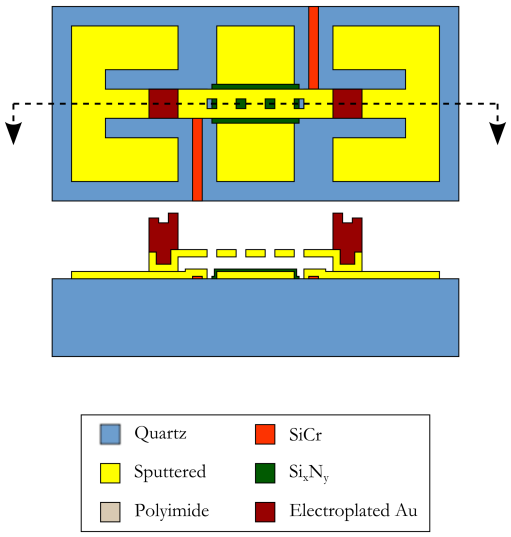


Figure 2.33: Polyimide sacrificial layer is stripped and MEMS bridges are released

Produced SPDT switches with the standard METU RF MEMS process cycle can be seen Figure 2.17 and Figure 2.18.

2.4 RF Measurements and Performances of SPST and SPDT Switches

RF measurements of fabricated SPST and SPDT RF MEMS switches and many test devices are performed in Microwave and Millimeter-Wave Laboratory of METU Electrical and Electronics Engineering Department. Cascade Microtech Summit 9000 analytical probe station and Agilent E8361A Vector Network Analyzer are the utilized devices in the measurements. In order to actuate fabricated MEMS switches, a 200 Hz, unilevel, bipolar waveform is utilized. This waveform is obtained by a bias generator card which has been designed and presented in his thesis by Halil İbrahim Atasoy [44]. SPST switches are actuated by the use of a bias-tee, however due to the DC bias pads it was not needed in the measurements of SPDT switches. Vector Network Analyzer is calibrated in the 10-40 GHz band by SOLT (short-open-load-thru) calibration scheme by the use of Cascade 101-190 Impedance Standard Substrate. As pointed out in the previous sections, pitch spacing (ground to ground spacing) of the utilized RF probes are approximately 220 μm.

As mentioned in the previous paragraph, many test structures other than the MEMS switches have been utilized in the measurements in order to characterize MEMS switches better. One of the important test structures to be measured was the CPW lines in various dimensions. All the CPW configurations utilized in the SPDT switch structures are also produced as independent test structures. Physical length of the all the fabricated CPW lines were around 7 mm and by curve fitting between the measurement results and circuit model simulation results, circuit model parameters were extracted. Extracted parameters for the CPW lines were characteristic impedance (Z_0), loss component (dB/m) and effective permittivity (ϵ_{eff}) of the measured line. Parameter values are tabulated for various CPW line structures and can be seen in Table 2.11.

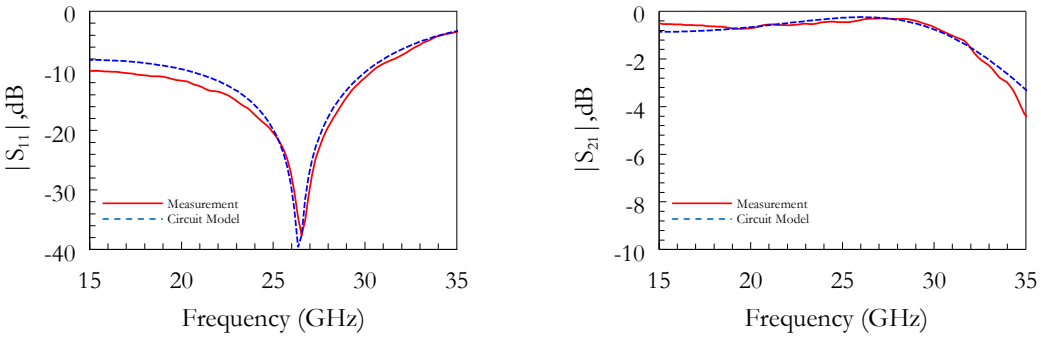
Table 2.11: Extracted parameters based on the measurements for various CPW line structures

Gap-Signal-Gap (μm)	Length (μm)	Z_0 (Ω)	Loss (26 GHz | 12 GHz)	ϵ_{eff}
68 – 84 – 68	6951.5	92.52	(64.71 | NN*)	2.358
63 – 94 – 63	6951.5	87.66	(70.33 | NN*)	2.358
20 – 180 – 20	7000.0	54.44	(87.49 | 59.32)	2.366
25 – 260 – 25	7000.0	54.01	(81.79 | 52.76)	2.371
90 – 130 – 90	7000.0	90.18	(63.01 | NN*)	2.383
100 – 110 – 100	7000.0	96.59	(NN* | 36.87)	2.391
150 – 220 – 150	7000.0	90.43	(NN* | 27.40)	2.414

NN*=not necessary

During the circuit modeling of SPST and SPDT RF MEMS switches, these extracted parameters will be utilized in the modeling of transmission lines.

CPW line measurements were followed by the SPST switch measurements and circuit modeling studies. Circuit model presented in Figure 2.6 is utilized and linear CPW transitions have been integrated into the model from the EM simulation results, since their modeling by a transmission line is not trustworthy. RF measurement results and curve fitted circuit model simulation results for the shunt, capacitive contact RF MEMS switch, designed for 26 GHz operating frequency, are presented in Figure 2.34. Fabricated switch can be seen in Figure 2.10.



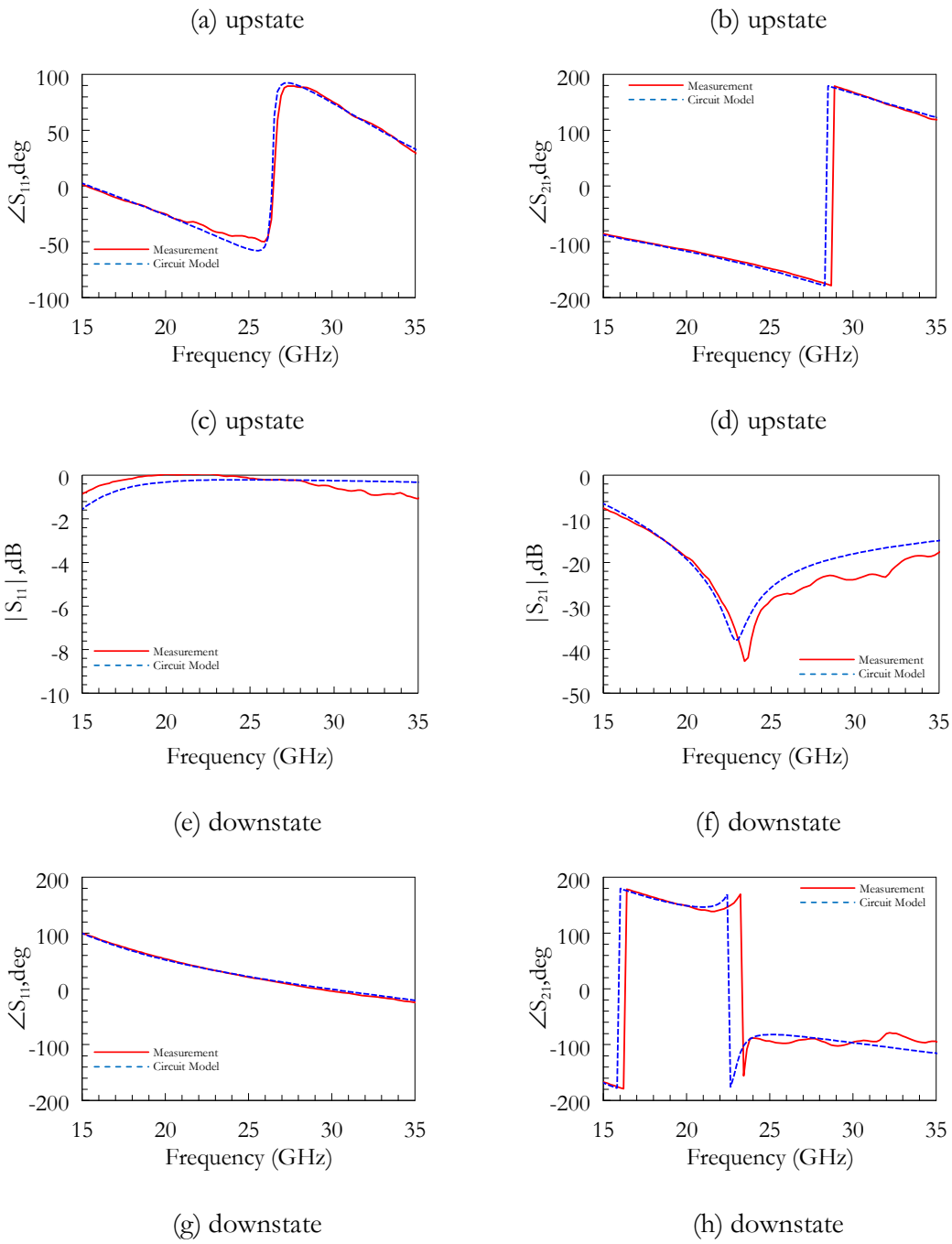


Figure 2.34: RF measurement results and curve fitted circuit model response of the shunt, capacitive contact RF MEMS switch designed at the operating frequency of 26 GHz

Return loss in the upstate has a resonance at 26.5 GHz and return loss value at 26 GHz operating frequency is 27.61 dB. Insertion loss in the downstate is observed to be 0.21 dB. However, it seems that the resonance frequency for the isolation performance in the downstate is shifted through 23.43 GHz. It should be noted, that the measurements are done at a voltage slightly higher than the pull in voltage and resonance frequency is decreased due to high bridge capacitance. It is been observed that, when the measurements are done at a lower voltage (hold voltage) than the pull in voltage after the bridge has collapsed, it is possible to tune the resonance frequency to 26 GHz. This performance is actually obtained due to partial contact approach utilized in the EM simulations. In Figure 2.34, the peak value for the isolation can be observed to be approximately 40 dB.

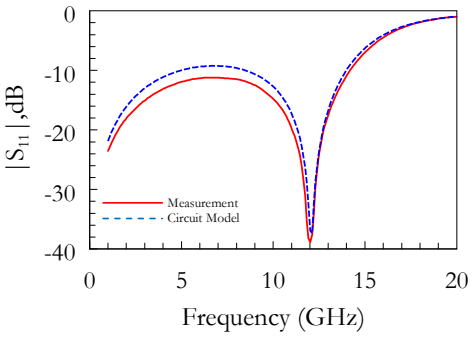
Extracted circuit model parameters by curve fitting from the measurements and EM simulations and their differences are tabulated and can be seen in

Table 2.12. Parameters in Table 2.12 will be utilized directly in the SPDT switch modeling in the following pages.

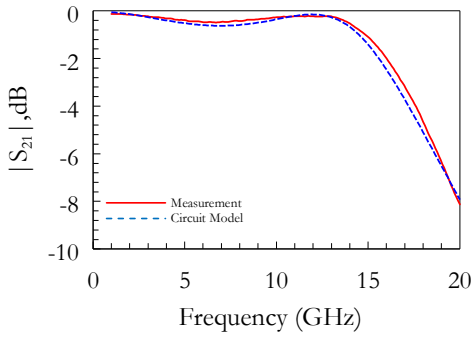
Table 2.12: Circuit model parameters extracted from the measurements for the shunt, capacitive contact RF MEMS switch designed to operate at 26 GHz

Parameter	Value
Z_0	85.9 Ω
C_u	59.25 fF
C_d	352.9 fF
L_{brd}	136.8 pH
R_{brd}	0.771 Ω
L_{s1}	144.5 pH
L_{s2}	171.4 pH
C_{sh1}	1.186 fF
C_{sh2}	6.847 fF
ℓ_{line}	810 μm

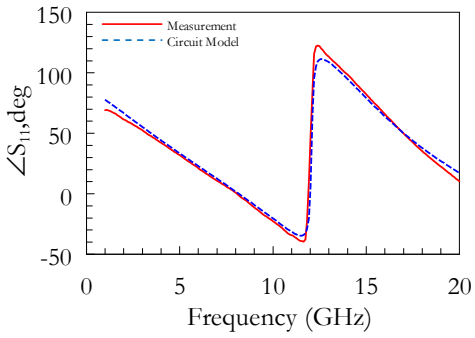
Same procedures have been applied to the RF MEMS SPST switch operating at 12 GHz. Measurement results and curve fitted circuit model responses can be seen in Figure 2.35. It is easily seen that circuit model is quite accurate. Fabricated switch utilized in the measurements can be seen in Figure 2.11.



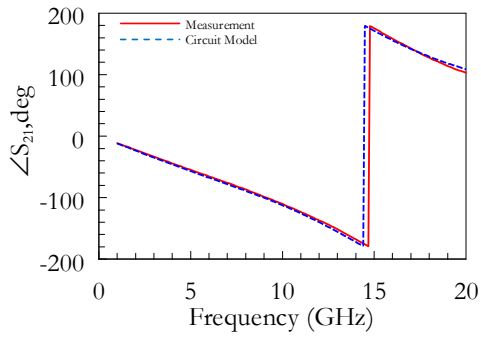
(a) upstate



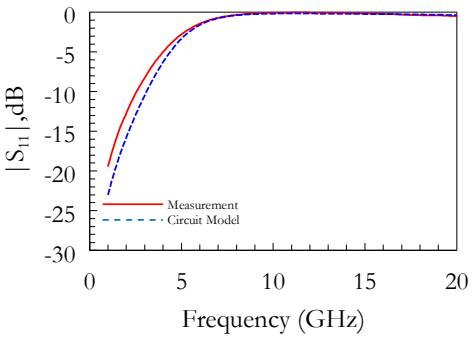
(b) upstate

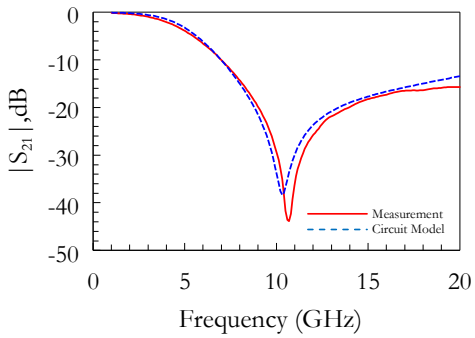


(c) upstate



(d) upstate





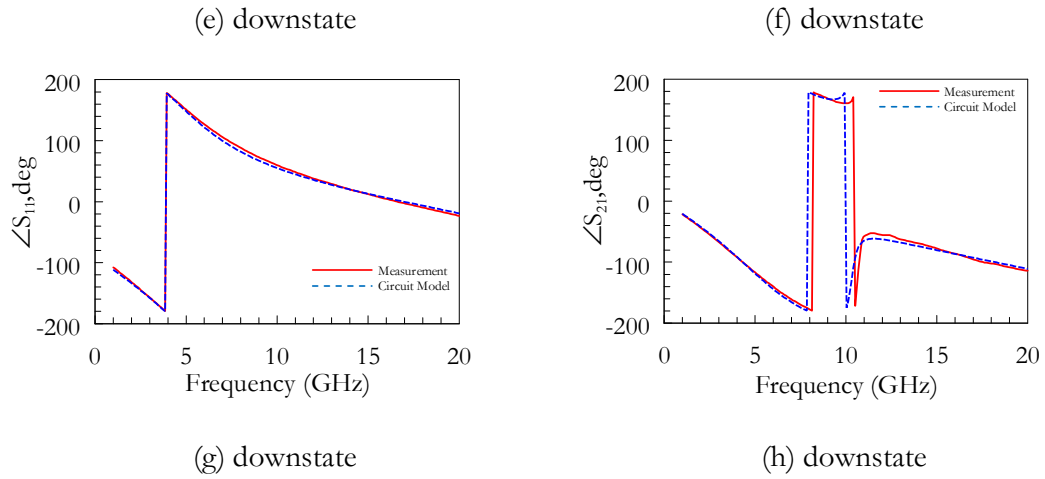


Figure 2.35: RF measurement results and curve fitted circuit model response of the shunt, capacitive contact RF MEMS switch designed at the operating frequency of 12 GHz

Return loss in the upstate has a resonance at 12.02 GHz and return loss value at the operating frequency is 38.69 dB. Insertion loss in the downstate is observed to be 0.05 dB at the operating frequency. However, it seems that the resonance frequency for the isolation performance in the downstate is shifted through 10.69 GHz. It should be noted, that the measurements are done at a voltage slightly higher than the pull in voltage and resonance frequency is decreased due to high bridge capacitance. It is been observed that, when the measurements are done at a lower voltage (hold voltage) than the pull in voltage after the bridge has collapsed, it is possible to tune the resonance frequency to 12 GHz. This performance is actually obtained due to partial contact approach utilized in the EM simulations. In Figure 2.35, the peak value for the isolation can be observed to be approximately 45 dB.

Extracted circuit model parameters by curve fitting from the measurements are tabulated and can be seen in Table 2.13. Parameters in Table 2.13 will be utilized directly in the SPDT switch modeling in the following pages.

Table 2.13: Circuit model parameters extracted from the measurements for the shunt, capacitive contact RF MEMS switch designed to operate at 12 GHz

Parameter	Value
Z_0	85.9 Ω
C_u	133.2 fF
C_d	1107.0 fF
L_{brd}	215.0 pH
R_{brd}	0.660 Ω
L_s	215.0 pH
C_{sh}	16.55 fF
ℓ_{line}	810 μm

Following the circuit modeling of shunt, capacitive contact RF MEMS switches, it has been concentrated on the measurements and circuit modeling of SPDT switches. Same measurement procedures have been applied as in the SPST switches, except actuation voltage is applied through DC bias lines. It is assumed that RF signal is being transmitted only from one of the output ports every time, so circuit modeling is not carried out for the case where both switches are at upstate. In order to clarify, it can be said that one of the switches was at upstate while the other one was in downstate.

At the measurement step of the SPDT switches a problem has been encountered and measurements are done in a different way than the intended. Due to mechanical reasons RF probes could not have been utilized at both output ports simultaneously, so one of the ports is hold as open circuit. Although, this seems to be a significant problem, the effects were insignificant and did not affect the circuit performance due to the utilized SPDT structure. In the measurements, port 2 is hold at open circuit and these changes are also applied to the circuit models and the SPDT switches are treated as two port devices. Obtained measurement results and circuit model responses are presented in Figure 2.36 for RF MEMS SPDT switch, designed to operate at 26 GHz. Fabricated device is presented in Figure 2.17.

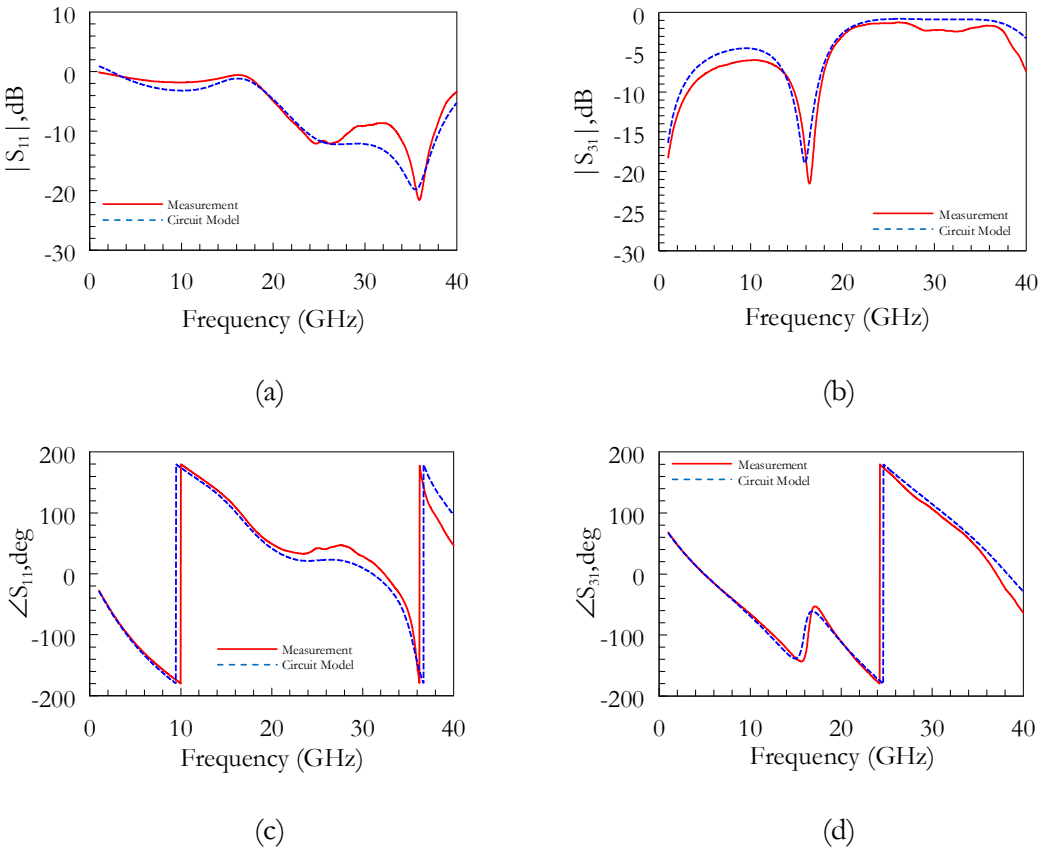


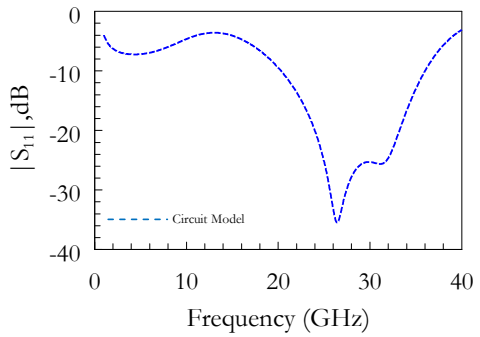
Figure 2.36: RF measurement results and circuit model response of the RF MEMS SPDT switch designed at the operating frequency of 26 GHz

Return loss at the input port is measured to be 12 dB at 26 GHz operating frequency and insertion loss at the transmission port is obtained to be 1.24 dB. These results were surprising and the circuit hardly reflected the expected performance. Investigations through circuit model revealed that the problem was in the DC blocking MIM capacitor values. Since MIM capacitors were fabricated as independent test structures, their capacitance values are easily measured and the responses are modeled by a circuit model. It has been clarified that the capacitance value at the 26 GHz design was around 225 fF, which is hardly close to the expected 2 pF capacitance. Furthermore, same problem has been observed in

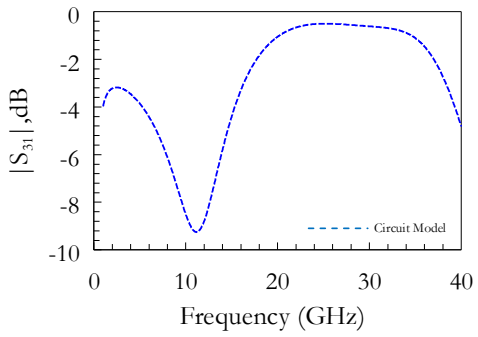
the 12 GHz design and the capacitance value of the DC blocking capacitor was found to be approximately 380 fF, which is again incomparable to the expected 4 pF value. Through these results it was observed that obtained results were around 10% of the expected values, so the layouts drawings have been investigated. It is discovered that, the problem was at the layout drawings and the MIM capacitors are fabricated as bridges and so the capacitance values were hardly satisfies the needs.

The capacitance values are corrected in the circuit model and it is observed from circuit model responses that, expected performances can easily be approximated. Obtained SPDT switch performance designed at 26 GHz operating frequency, is presented in Figure 2.37.

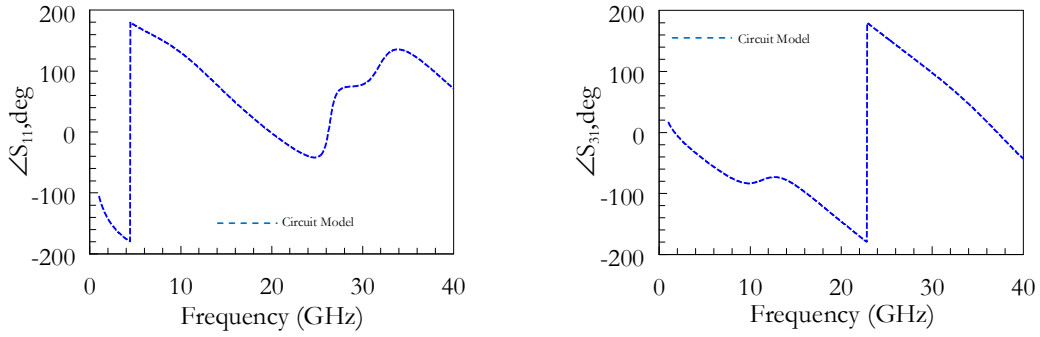
In Figure 2.37, at the 26 GHz operating frequency return loss is measured to be 33.24 dB and insertion loss is measured to be 0.51 dB.



(a)



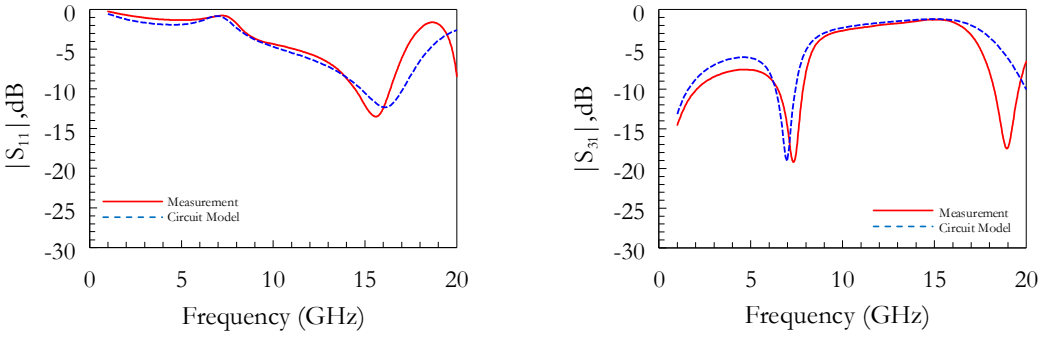
(b)



(c) (d)

Figure 2.37: Altered circuit model response of the RF MEMS SPDT switch designed at the operating frequency of 26 GHz

Same procedures have been applied to the SPDT switch designed at 12 GHZ operating frequency and obtained results are presented in Figure 2.38, including the circuit model responses.



(a) (b)

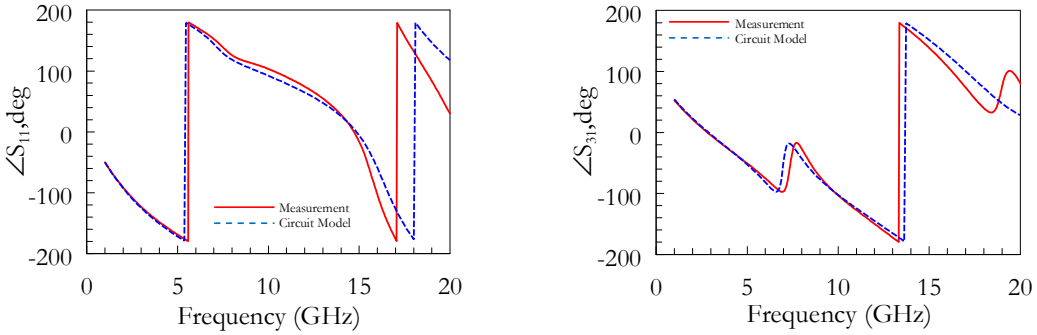


Figure 2.38: RF measurement results and circuit model response of the RF MEMS SPDT switch designed at the operating frequency of 12 GHz

The capacitance values are corrected in the circuit model and it is observed from circuit model responses that, expected performances can easily be approximated. Obtained SPDT switch performance designed at 12 GHz operating frequency, is presented in Figure 2.39.

In Figure 2.39, at the 12 GHz operating frequency return loss is measured to be 18.48 dB and insertion loss is measured to be 0.49 dB.

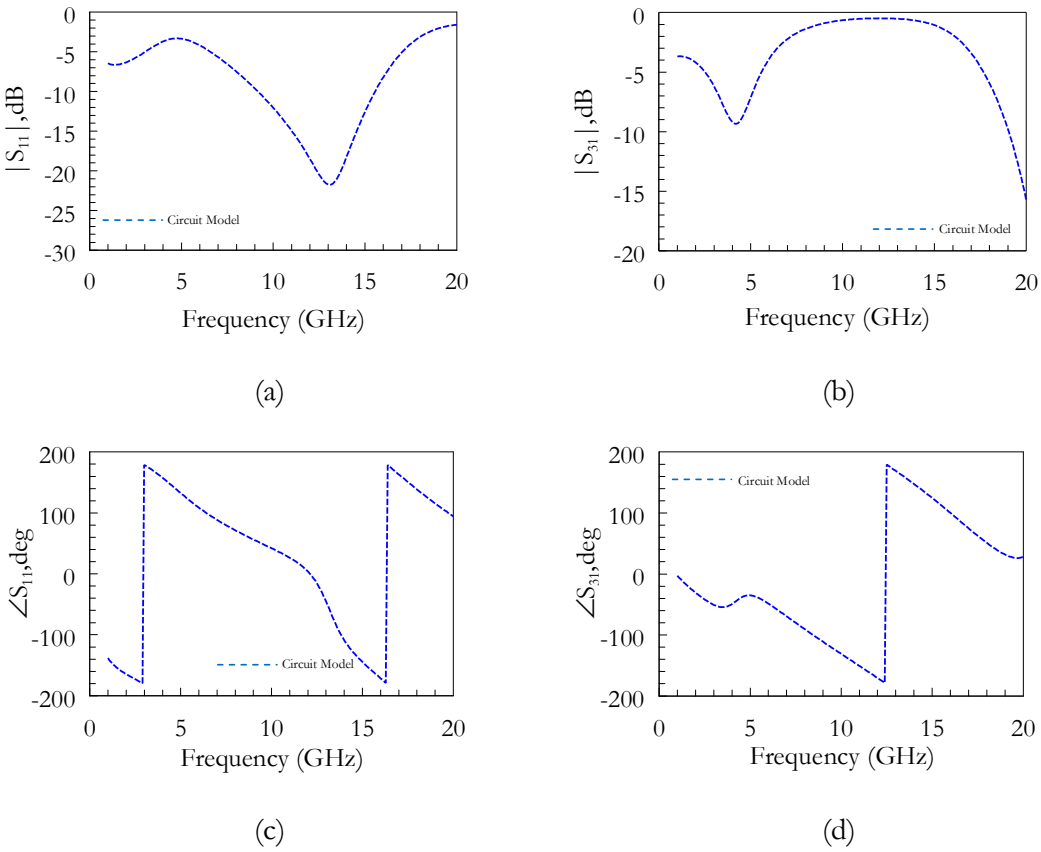


Figure 2.39: Altered circuit model response of the RF MEMS SPDT switch designed at the operating frequency of 12 GHz

CHAPTER 3

ZERO-LEVEL PACKAGE STRUCTURES AND MODIFICATIONS IN THE SPST AND SPDT SWITCH DESIGNS

This chapter investigates two proposed zero-level package structures for shunt, capacitive contact RF MEMS switches and RF MEMS SPDT switches. Furthermore, the chapter includes the necessary design modifications in the switch structures after the packages are introduced, based on EM and circuit simulations. Both of the suggested package structures are intended to be formed by bulk micromachining of high resistive Si wafers and utilize BCB (Benzocyclobutane) as the adhesive wafer bonding material. This chapter begins with an introduction on the necessities of RF MEMS packaging and chosen zero-level packaging method. Section 3.2 introduces the proposed package structures. Section 3.3 presents the required design modifications on a shunt, capacitive contact RF MEMS switch which operates at 35 GHz [14]. Section 3.4 provides the design modifications for the shunt, capacitive contact RF MEMS switches and SPDT switches, whose design, fabrication and RF measurement steps have been presented in Chapter 2.

3.1 Necessities and Characteristics of Chosen Zero-Level RF MEMS Packaging Method

Types of zero-level packaging methods can be classified into three as pointed out in Chapter 1 of this thesis. Chosen packaging method, in the concept of this thesis is the wafer to wafer zero-level packaging. "The zero-level package creates an on-wafer device scale enclosure around (or sealed cavity for) the MEMS device, serving as a first protective interface. In other words, the zero-level packaging is realized by bonding a protective cavity

housing the MEMS fragile structures" [23]. The bonding process in this sense needs a mid-material that should serve as the bonding and sealing material. In this study bonding material is chosen to be BCB.

3.2 Proposed Package Structures

Both of the package structures are designed as they are formed by high-resistive (>10000 Ω.cm) Si wafers and by assuming BCB as the adhesive and sealing material, which has a relative electrical permittivity of 2.65. In both of the structures the RF MEMS devices are intended to be housed in a cavity which is surrounded by a rectangular BCB ring. Planar feed-through approach is adopted in both of the package structures and this caused the BCB ring to pass on top of CPW lines. Figure 3.1 presents the general package structure, where all the mentioned properties may be visually comprehended better.

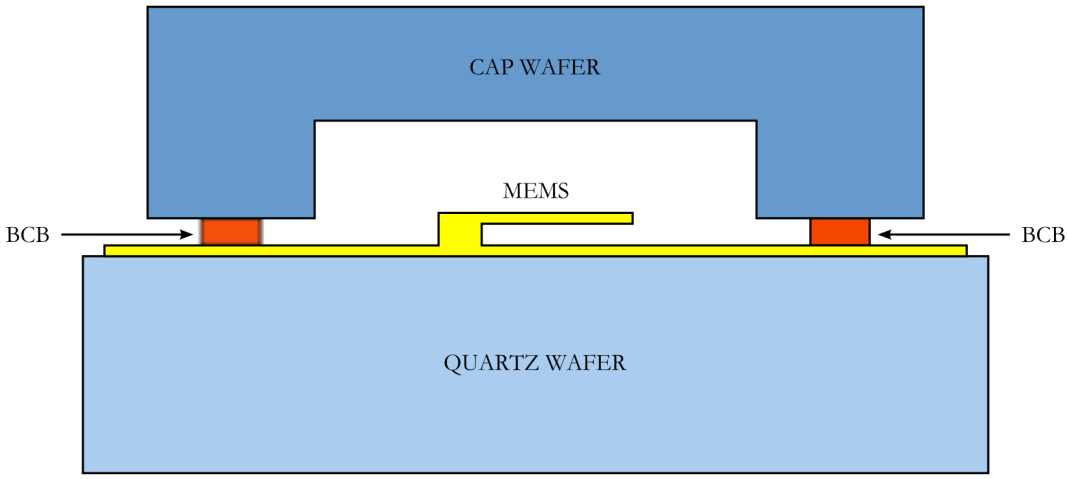


Figure 3.1: General package structure

Since the BCB rings and Si wafer on top of them passes through the CPW line, they load the line and causing the characteristic impedance (Z_0) to decrease. If this loading effect is not considered, this may cause reflections on the CPW lines and the performance of the MEMS device may be distorted. In order to minimize the effects of this loading, polygonal CPW transitions are designed and utilized under the BCB rings. Their physical characteristics and performances will be explained in the following section. The reason that this approach is mentioned here is because, the two package structures differs in the placement of this CPW transitions. In other words, they differ by the placement of the BCB ring.

Section 2.2.2.3.4 indicated that, in order to be able to measure the RF MEMS switches in METU, port dimensions should be altered to have a gap to gap spacing of 220 μm. In the first structure, BCB rings are placed between the MEMS bridge and the CPW transitions. In the second package structure, the BCB rings are placed between the CPW transitions and the ports. Figure 3.2 and Figure 3.3 indicates EM models of the first and second package structures, respectively. BCB rings and the MEMS switch are visible since Si cap is drawn transparently.

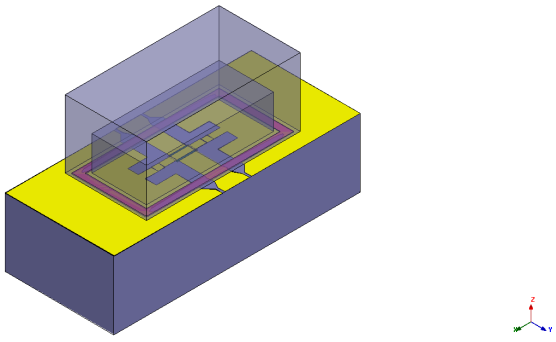


Figure 3.2: EM Model drawn for the first package structure without any modifications in the MEMS switch design (air boxes are not shown)

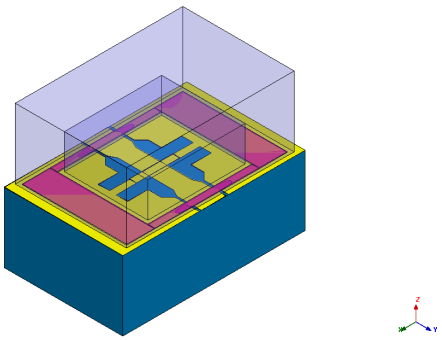


Figure 3.3: EM Model drawn for the second package structure without any modifications in the MEMS switch design (air boxes are not shown)

3.3 Required Design Modifications for a Shunt, Capacitive Contact RF MEMS Switch After Introducing Packages

Effects of proposed package structures have been investigated on a shunt, capacitive contact RF MEMS switch designed for 35 GHz operating frequency [14]. In this section, firstly the RF MEMS switch operates at 35 GHz will be introduced and its RF performance will be given. Secondly, performance shifts will be indicated after the packages are introduced to the switch by EM simulations. Finally, design modifications on the RF MEMS switch, required to minimize the both package effects will be investigated.

3.3.1 Physical Structure and RF Performances of the RF MEMS Switch at 35 GHz

RF MEMS switch at 35 GHz has been investigated by electromagnetic simulations and the responses are different than the responses in [14]. It is because; simulation conditions are not identical in two cases, such as boundary conditions and excitation ports. Utilized EM model for the switch at hand can be seen in Figure 3.4.

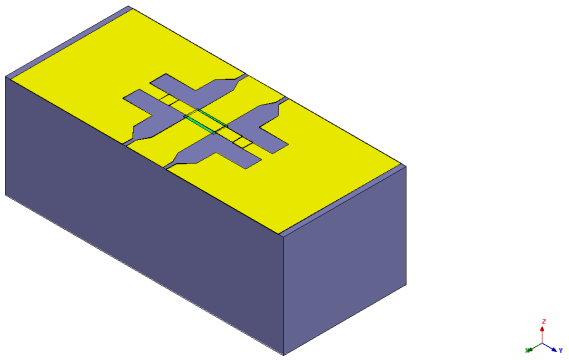


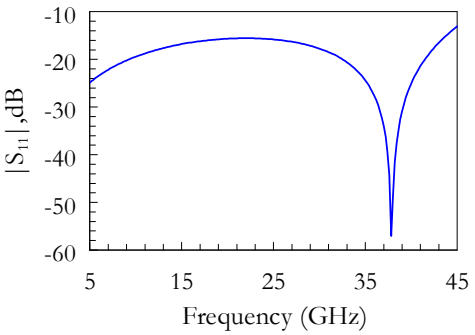
Figure 3.4: EM model of the shunt, capacitive contact RF MEMS switch at 35 GHz (air boxes are not shown)

Physical dimensions of the switch in Figure 3.4, which were defined in Figure 2.10, are tabulated in Table 3.1.

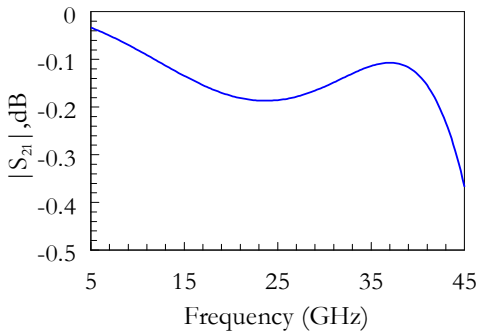
Table 3.1: Physical dimensions of the shunt, capacitive contact RF MEMS switch designed for 35 GHz operating frequency

Parameter	Value
W	130 μm
G	90 μm
W_{rec}	80 μm
D_{rec1}	145 μm
D_{rec2}	145 μm
W_{brd}	50 μm
ℓ_{brd}	310 μm
ℓ_{line}	95 μm

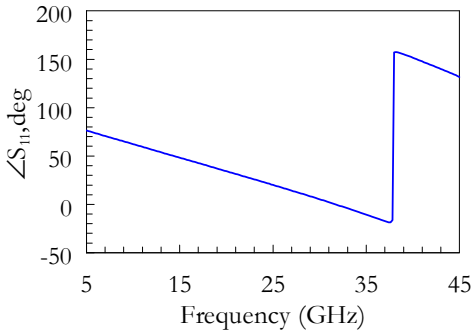
EM simulations are completed for both upstate and downstate of the switch and the magnitude and angle S-parameters are presented in Figure 3.5. These graphs will serve as a control group and package effects will be examined in reference with them.



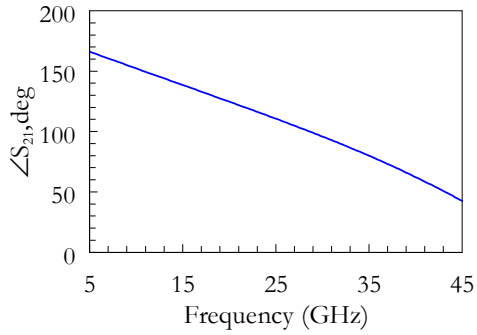
(a) upstate



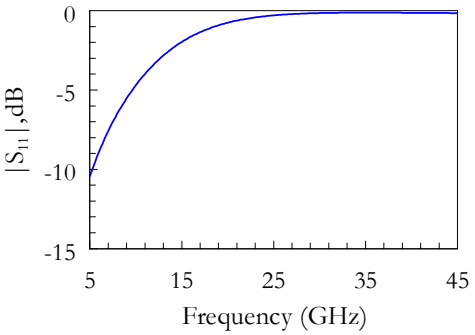
(b) upstate



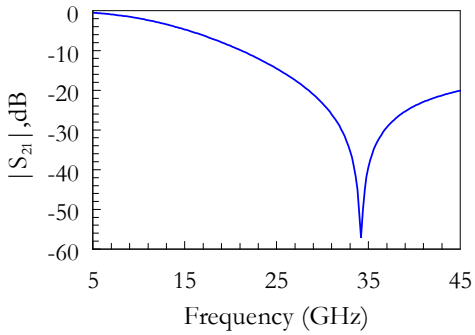
(c) upstate



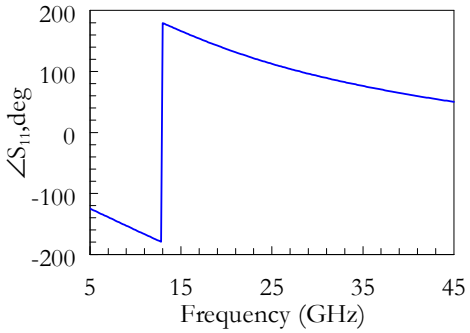
(d) upstate



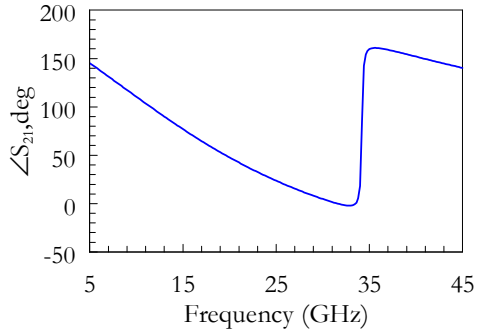
(e) downstate



(f) downstate



(g) downstate

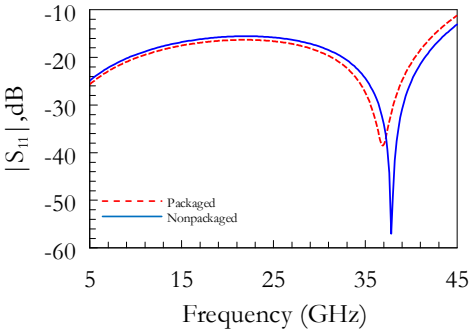


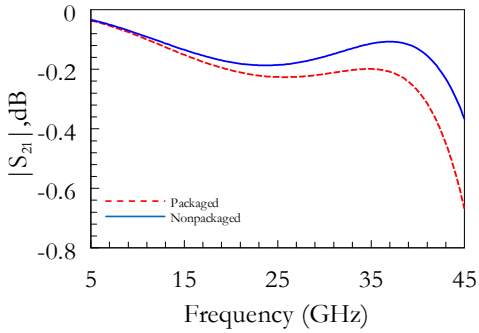
(h) downstate

Figure 3.5: S-parameters of the MEMS switch, designed to operate at 35 GHz, obtained from EM simulations

3.3.2 Integration of Packages to the EM Models

Both package structures are integrated into the EM model of the RF MEMS switch operational at 35 GHz, which can be seen in Figure 3.2 and Figure 3.3. Electromagnetic simulation results of the structure in Figure 3.2 and simulation results of the unpackaged switch in Figure 3.4 are presented in Figure 3.6. In addition to this, the same results for the structure in Figure 3.3 are presented in Figure 3.7.





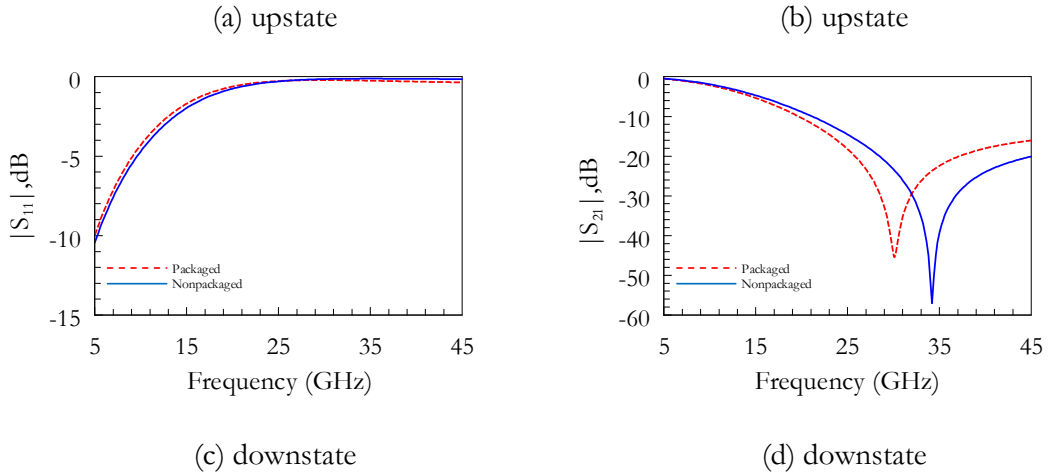
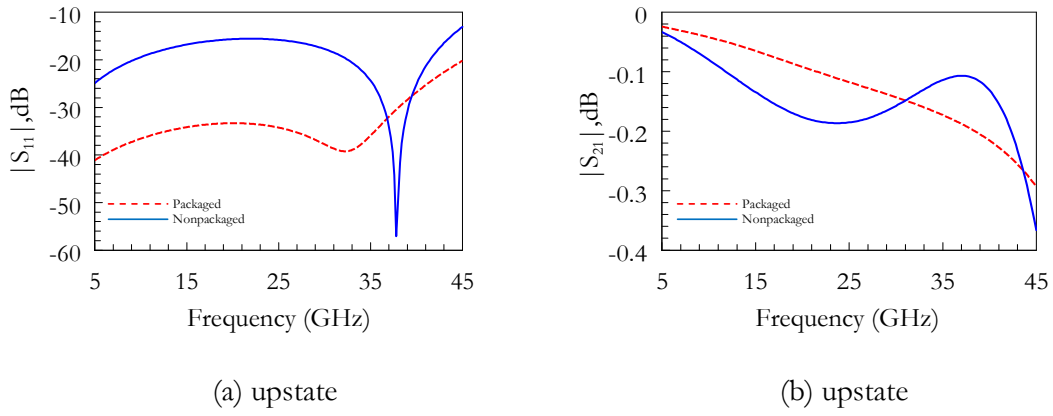
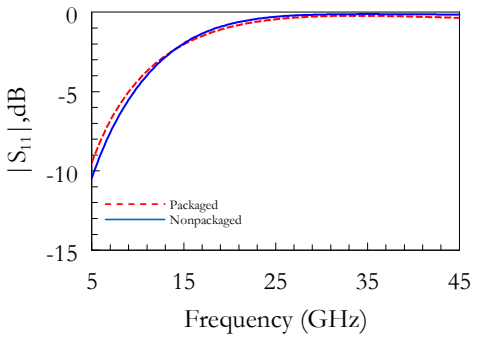


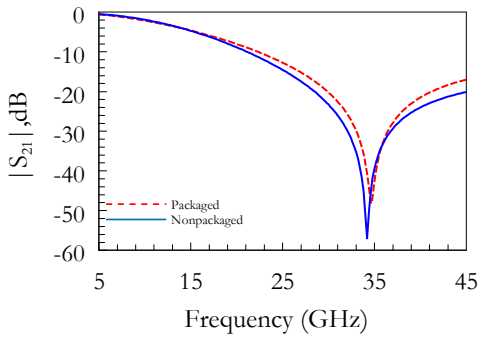
Figure 3.6: Comparison between the non-packaged and packaged MEMS switch performances without any design modifications in the switch (first package structure)

Figure 3.6 shows the effects of the first package structure and especially $|S_{21}|$ (isolation) in the downstate is problematic, where resonance frequency is shifted towards 30 GHz from 35 GHz. Rest of the S-parameters did not affected as much as downstate $|S_{21}|$ and the performances are acceptable.





(c) downstate



(d) downstate

Figure 3.7: Comparison between the non-packaged and packaged MEMS switch performances without any design modifications in the switch (second package structure)

Figure 3.7 indicates the magnitude S-parameters and effects of the second package structure without any design modifications in the switch. Performance of the switch did not affected much and the effects can be considered to be positive. Since the physical length of the CPW lines at the ports are increased, $|S_{11}|$ in the upstate is enhanced.

3.3.3 Design Modifications in the Packaged Switch

Design modifications in the MEMS switch will be expressed in this section. Polygonal CPW transitions are common for both package structures so, their design will be explained first. Then, design modifications for the first package structure will be explained, followed by the design modifications for the second package structure.

3.3.3.1 Polygonal CPW Transition Design

It is better to indicate a polygonal CPW transition prior to design steps. Figure 3.8 demonstrates top view of such a structure utilized in this study.

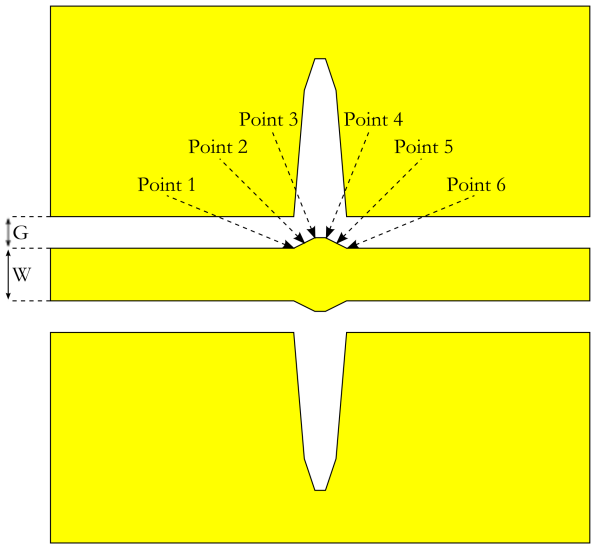


Figure 3.8: Top view of a polygonal CPW transition

It is pointed out in the previous sections that the BCB layer and Si wafer on top of it will load the CPW line under themselves due to the change in the ϵ_{eff} value. In order not to have reflections on the line, this loading effect should be taken into account. The idea in such a transition is to change the physical dimensions of the line section under the BCB, to have high impedance, so that loaded line impedance will be identical to the utilized reference impedance. Furthermore, in order to avoid a strong discontinuity, the transition area can be divided into sections. At the points between these sections, same high impedance value can be achieved by different physical dimensions and these points can be joined by linear lines. These points are shown in Figure 3.8. This approach leads to the

polygonal transition in Figure 3.8. If it is assumed that the transition length is 50 μm, then it is divided into 5 sections which have 10 μm lengths each.

Required high impedance that leads to the intended loaded line impedance is found from EM simulations. Then, different physical dimensions which give the same high impedance value are found analytically and the polygonal transition is formed. Obtained dimensions of the polygonal CPW transitions for the 35 GHz switch with both first package and second package structures are tabulated in Table 3.2 and Table 3.3, respectively.

Table 3.2: CPW dimensions and characteristic impedances at the points shown in Figure 3.8, for the switch at 35 GHz with first package structure

Point #	W	G	Z_0
1	130 μm	90 μm	85.91 Ω
2	130 μm	397 μm	132.93 Ω
3	140 μm	418 μm	131.96 Ω
4	140 μm	418 μm	131.96 Ω
5	130 μm	397 μm	132.93 Ω
6	130 μm	90 μm	85.91 Ω

Table 3.3: CPW dimensions and characteristic impedances at the points shown in Figure 3.8, for the switch at 35 GHz with second package structure

Point #	W	G	Z_0
1	180 μm	17 μm	49.96 Ω
2	200 μm	84 μm	74.54 Ω
3	220 μm	91 μm	74.31 Ω
4	220 μm	91 μm	74.31 Ω
5	200 μm	84 μm	74.54 Ω
6	180 μm	17 μm	49.96 Ω

3.3.3.2 Design Modifications for the Switch at 35 GHz with First Package Structure

The first package structure is application specific and the modifications may change according to the device to be packaged. In the case of a shunt, capacitive contact RF MEMS switch, required changes may be understood better if the circuit model in Figure 2.6 is considered. The resonance frequency of the isolation characteristics in the downstate is determined by the bridge capacitance and bridge inductance. In order to shift the optimum frequency of the isolation back to 35 GHz, either the bridge capacitance or the bridge inductance may be decreased. In order to decrease the bridge capacitance bridge dimensions should be modified which is not preferable. This may cause mechanical performance shifts and since the capacitive loading will be altered, the design procedure should be started over. Instead of modifying bridge dimensions, inductive tuning is a better solution. However, it should be noted that inductive tuning will also affect the upstate performance of the switch. This modification on the other hand may be compensated without altering the bridge dimensions as well. Without modifying the dimensions under the bridge, signal line may be narrowed. By considering both modifications the non-packaged switch characteristics may be approached.

Expressed modifications are utilized for tuning the switch characteristics in a controllable way via EM simulations. Modified EM model may be seen in Figure 3.9.

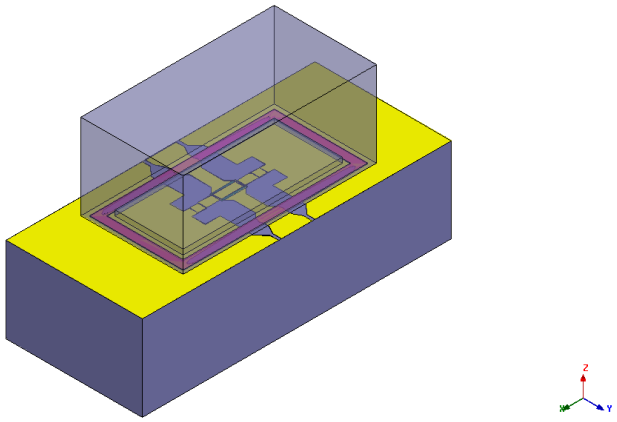


Figure 3.9: EM Model drawn for the first package structure including design modifications in the MEMS switch (air boxes are not shown)

Obtained magnitude S-parameters for the EM model in Figure 3.9 are presented in Figure 3.10. Modified dimensions are defined in Figure 2.10 and tabulated in Table 3.4.

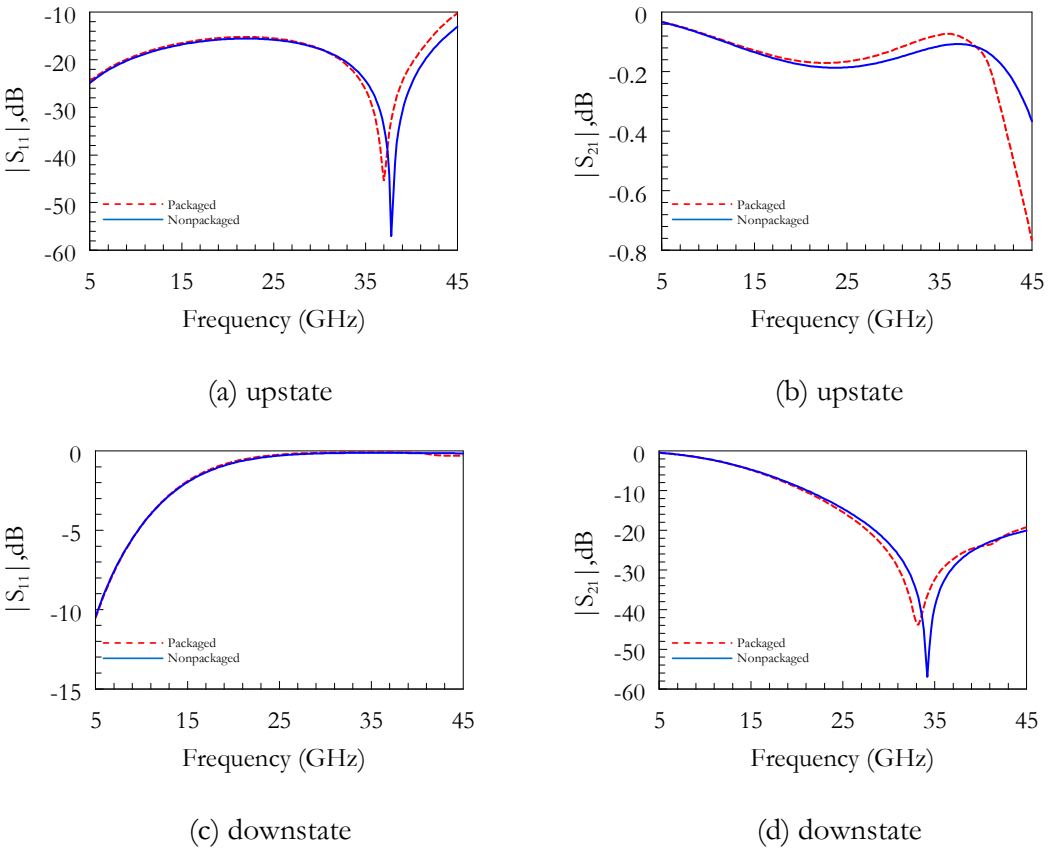


Figure 3.10: Comparison between the non-packaged and packaged MEMS switch performances with applied design modifications in the switch (first package structure)

Table 3.4: Modified dimensions and their values for the packaged RF MEMS switch operational at 35 GHz (first package structure)

Parameter	Original value	Modified Value
D_{rec}	145 µm	85 µm
W	130 µm	70 µm

3.3.3.3 Design Modifications for the Switch at 35 GHz with Second Package Structure

Since the obtained performances for the second package structure are acceptable, switch design is not modified. Only difference is the increased CPW line lengths at the ports, for easy access of RF probes in the measurements. Modified EM model of the packaged switch can be seen in Figure 3.11.

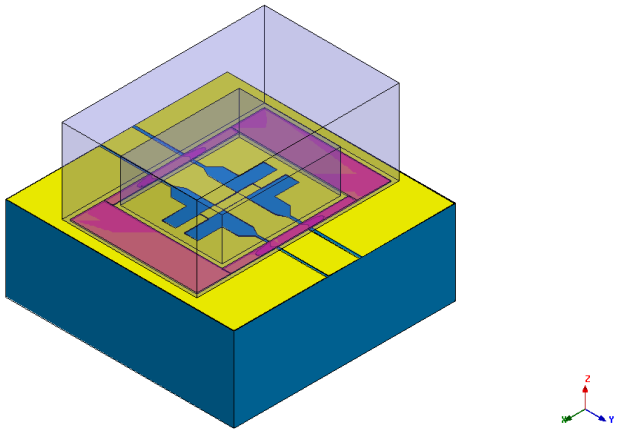


Figure 3.11: EM Model drawn for the second package structure including design modifications in the MEMS switch (air boxes are not shown)

Obtained magnitude S-parameters for the EM model in Figure 3.11 are presented in Figure 3.12.

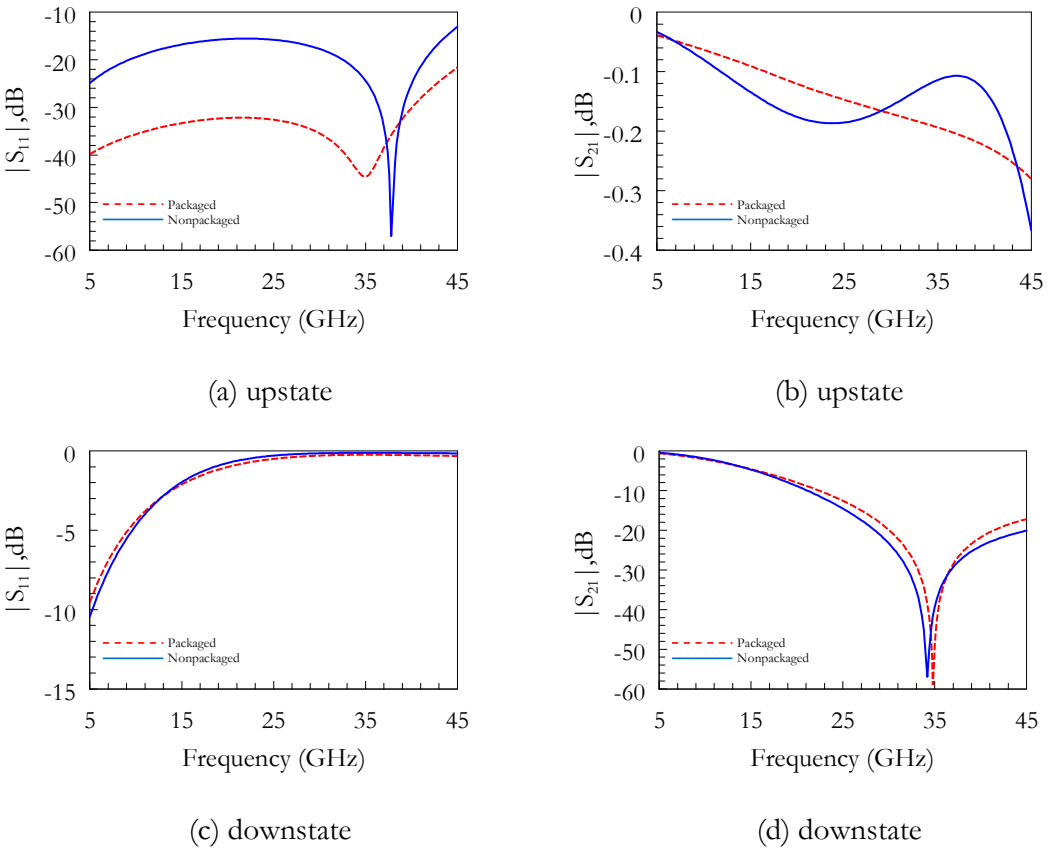


Figure 3.12: Comparison between the non-packaged and packaged MEMS switch performances with applied design modifications in the switch (second package structure)

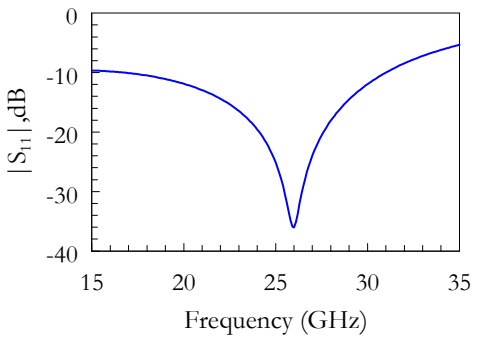
3.4 Design Modifications in the SPST and SPDT Switches

Due to its ease of applicability to all switches, second package structure is utilized in the packaging studies of shunt, capacitive contact RF MEMS switches and SPDT RF MEMS switches, whose design, fabrication and measurement steps are expressed in Chapter 2. Second package structure indeed cannot alter the isolation characteristics of the switches however; due to the package electrical lengths of the devices increase. Not only owing to the extra polygonal transition lengths but also due to the extra CPW lengths added to the

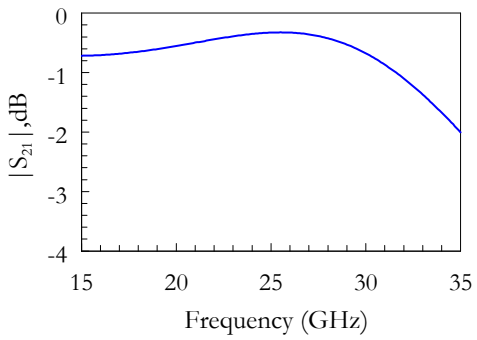
ports for measurement purposes, the characteristics may be modified. Physical dimensions of the devices should be tuned following the integration of the package for each device.

In the package integration of SPST and SPDT switches, full model EM simulations were not performed. Especially, when the physical sizes of the SPDT switches are considered EM simulations would be time consuming. EM simulations are performed for the polygonal transitions and their responses are imported into the circuit models. Then necessary physical dimension tunings are performed. Considering SPST switches, ℓ_{line} shown in Figure 2.10 is the tunable parameter, and it is for the SPDT switches physical length of the $\lambda/4$ line sections. In the second package structure, polygonal transitions are close to the ports and CPW dimensions at the ports are identical for all SPST and SPDT switches. In other words, previously designed polygonal transitions have been utilized in the designs whose physical dimensions are presented in Table 3.3.

Circuit model performances of the packaged shunt, capacitive contact RF MEMS switches for 26 GHz and 12 GHz operating frequencies are presented in Figure 3.13 and Figure 3.14, respectively.



(a) upstate



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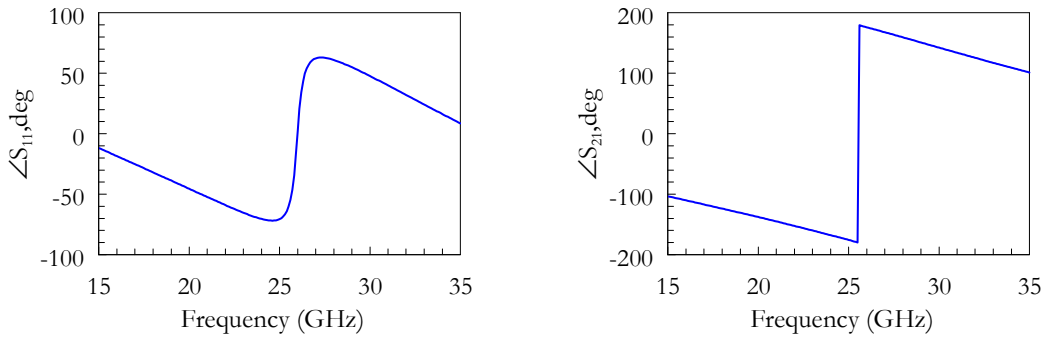

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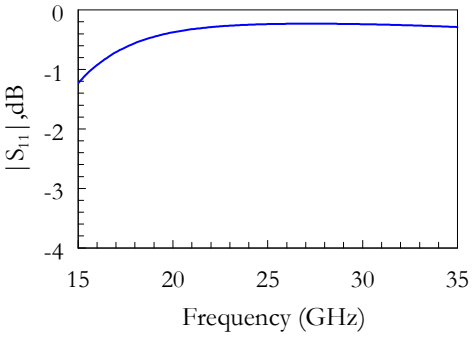

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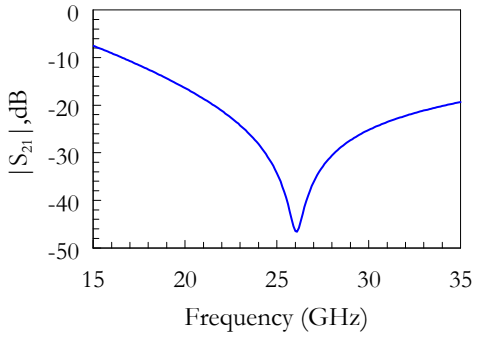

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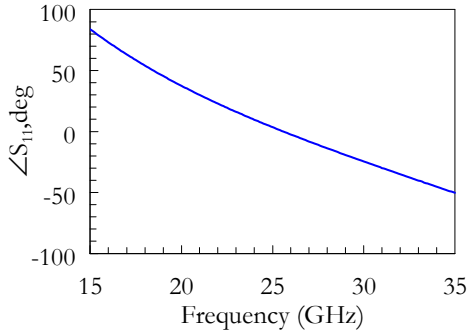

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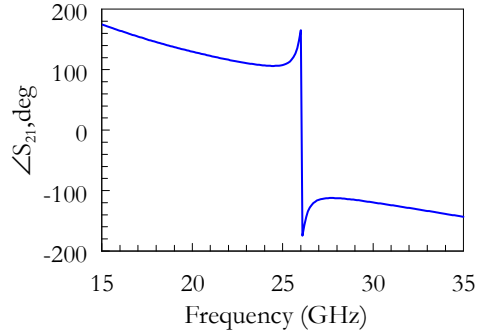
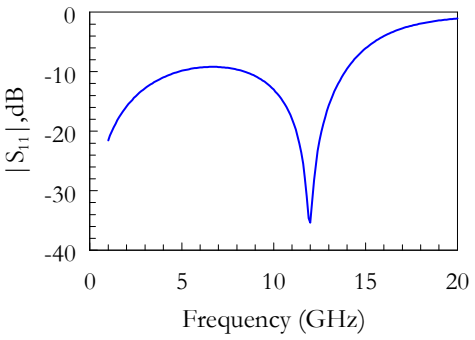
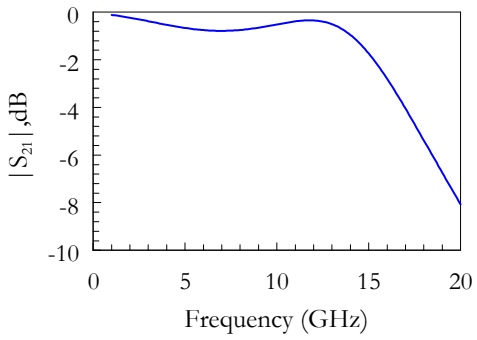


(h) downstate

Figure 3.13: Circuit model simulation results for the packaged shunt, capacitive RF MEMS switch operational at 26 GHz



(a) upstate



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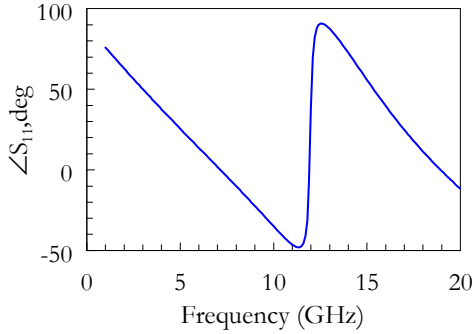

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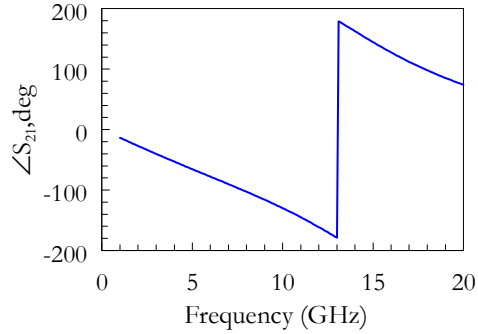

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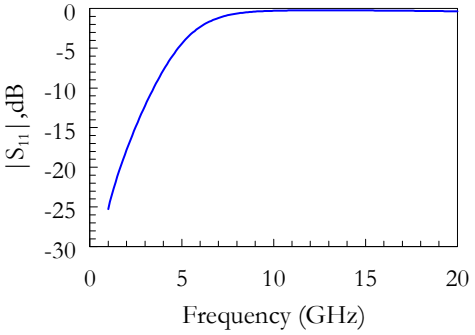

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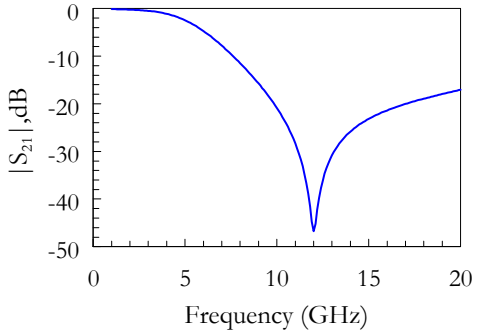

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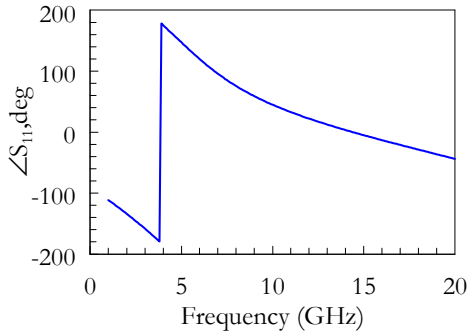

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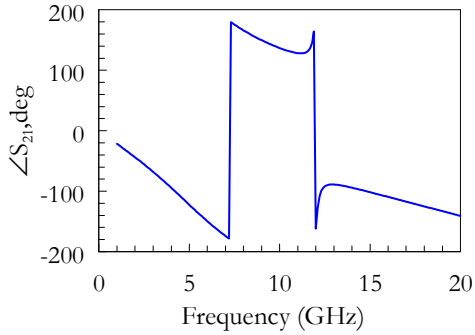

(h) downstate

Figure 3.14: Circuit model simulation results for the packaged shunt, capacitive RF MEMS switch operational at 12 GHz

Modified dimensions are defined in Figure 2.10 and tabulated in Table 3.5.

Table 3.5: Modified dimensions and their values for the packaged RF MEMS switches operational at 26 GHz and 12 GHz

Parameter	26 GHz		12 GHz	
	Original	**Modified**	**Original**	**Modified**
ℓ_{line}	830 μm	820 μm	1760 μm	1740 μm

Circuit model simulation responses for the packaged RF MEMS SPDT switches are presented in Figure 3.15 and Figure 3.16 for 26 GHz and 12 GHz designs, respectively.

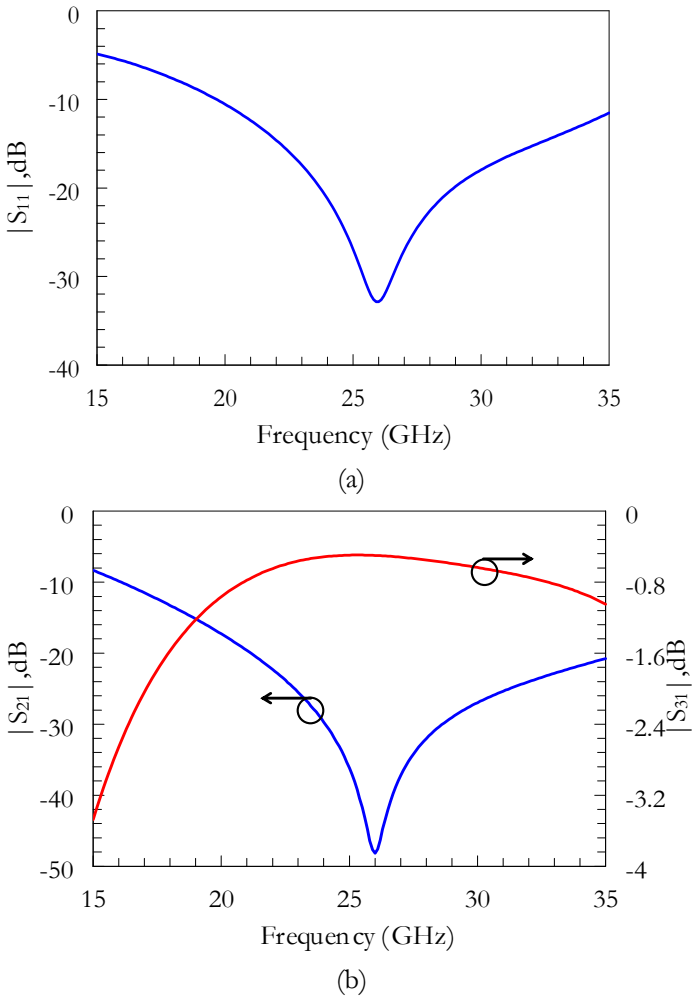

Figure 3.15: Circuit simulation results for the packaged RF MEMS SPDT switch at 26 GHz

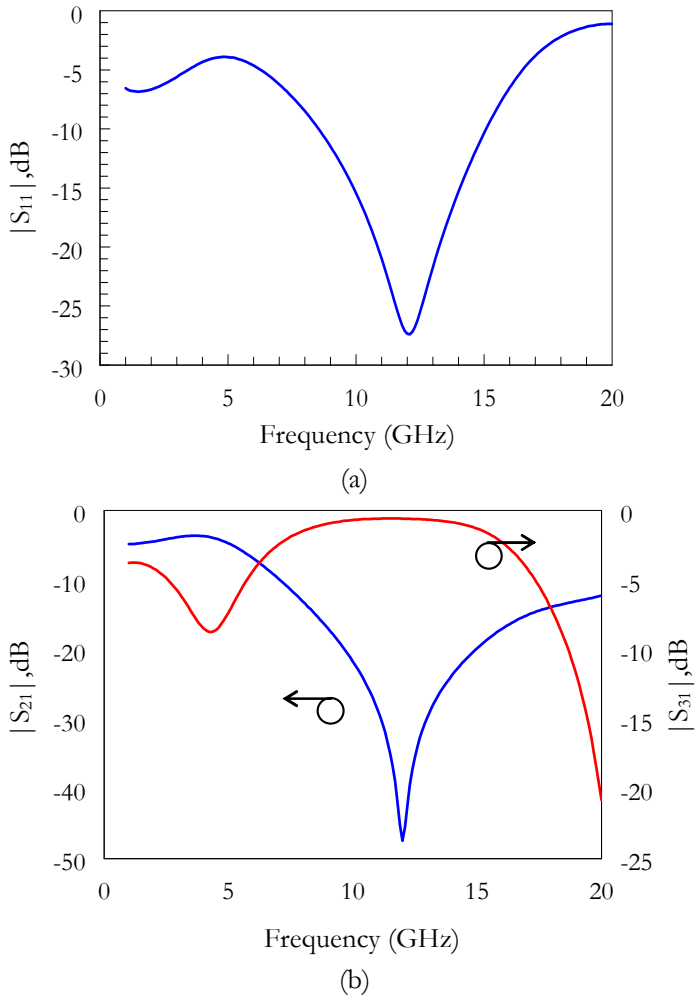

Figure 3.16: Circuit simulation results for the packaged RF MEMS SPDT switch at 12 GHz

λ/4 line sections at both of the designs are shortened 20 μm at each branch, for tuning the performances after introducing the package.

CHAPTER 4

DEVELOPMENT OF ZERO-LEVEL PACKAGING PROCESS

This chapter investigates process development steps for the zero-level packaging with BCB as the bonding and sealing material. In the concept of the study two process development approaches are considered. The approaches differ in the sense of their Si etching process choices. One of them utilizes KOH anisotropic Si etching in order to obtain cavities and pad windows and the other approach is based on DRIE (Deep Reactive Ion Etching). This chapter begins with an assessment on the packaging method in a process point of view and separates the process development operation into smaller tasks. Wafer bonding optimization with BCB adhesive material is presented in Section 4.2. Section 4.3 presents the process development steps for the KOH anisotropic Si etching based packaging approach. Section 4.4 gives a detailed explanation of the completed parts of the process development operation for DRIE based approach. Section 4.5 presents the modified DRIE based approach.

4.1 Utilized Packaging Method in a Process Point of View

Utilized packaging approach in this study can be classified as wafer to wafer zero level packaging. In brief, a cap wafer patterned with bulk micromachining techniques is bonded on top of a process wafer, on which the MEMS devices are fabricated, by BCB as adhesive material. The method is categorized into wafer to wafer zero-level packaging because; neither the cap wafer nor the process wafer is diced prior to wafer bonding.

Process wafer is quartz by default, because the RF MEMS devices in this study are designed assuming quartz substrate. Cap wafer is chosen to be Si, due to its ease of use in bulk micromachining technologies. For instance, SiO_2 which is easy to obtain by thermal oxidation is utilized as the masking layer in KOH anisotropic Si etching. In addition to this, regular DRIE equipments are suitable for Si etching and require additional properties for metal etching as an example. The reasons behind the choice of BCB are explained in the previous chapter. As to repeat, BCB has a relatively low bonding temperature (250 °C), is processable with photolithography techniques and is a semi hermetic sealing material. Low bonding temperature is considered to be the most significant property, because high temperatures may affect the MEMS bridges, which are in fact made of gold. Since the MEMS bridges are suspended structures, plastic deformation may occur at high temperatures and this should be avoided. Furthermore, gold has a melting temperature around 420 °C which is a point that should not be exceeded no matter what. Processability by photolithographic techniques is quite favorable since it saves time and provides easy process. Full hermeticity may be required in many MEMS applications, however RF MEMS devices in this study does not need such high measures. This is why BCB is still favorable, although it does not provide full hermeticity.

In the zero-level packaging approach, there needs to be cavities which are housing the MEMS devices and pad windows which are the gates for the measurement probes to enter on the cap wafer. In other words, pad windows are required in order to be able to measure the performances of the packaged devices. Pad windows on the wafer should be opened through the wafer and cavities should be half way for instance. In both approaches which have been adopted so far, cavities and pad windows are tried to be formed which requires a two sided process for the cap wafers.

The process development can be divided into three smaller tasks which is the adopted method in this study. Since this was the first time, METU RF MEMS group used BCB in their processes, it was crucial to get familiarize with the material. The first step was to

obtain high quality wafer bonding using blank wafers with the BCB adhesive material. Following this step, it is aimed to bond a Si cap wafer (only cavities are opened) to a blank glass wafer. Then, the final step is to bond a fully processed cap wafer to a fully processed process wafer.

4.2 Wafer Bonding Optimization Using BCB as the Adhesive Material

Although, the process optimization period is divided into sub-works, all the optimization took place at the same time. Cap wafers utilized in order to optimize BCB coating procedure are utilized as well in the wafer bonding optimization.

4.2.1 BCB Process Optimization

Although, photolithography is the enabling technology for micromachining, BCB was a new material for METU RF MEMS group before this study. During the optimization of BCB processing, end point monitoring has been utilized in accordance with the process guidelines from Dow Chemical Company. Cyclotene 4024-40 resist is preferred, due to the intended 5.5 μm layer thickness and in order to obtain this thickness, rotational speed is calculated to be 3300 rpm. Surface treatment is done prior to spin coating of BCB by the use of AP 3000 adhesion promoter. Steps of the optimized process cycle are itemized and are as follows;

- Dehydration of the cap wafer,
- Spin coating as surface treatment (AP 3000, 3300 rpm),
- Spin coating of BCB (Cyclotene 4024-40, 3300rpm),
- Soft bake (90 sec @ 65 ˚C),
- UV expose (16.5 sec in vacuum contact),
- Development (~4.5 min development time in DS 3000 @ 36 ˚C).

4.2.2 Wafer Bonding Optimization

Many trials have been made in order to find the right process parameters during the wafer bonding optimization. EVG Bonder 501 is utilized throughout the duration of packaging process development. There have been eight wafer bonding trials until a good bonding is achieved between the wafers. The process conditions and results of the eight trials will be presented in Table 4.1.

Table 4.1: Process conditions and results of the trials during the wafer bonding process optimization (RT=Room Temperature)

Trial #	Process Summary	Results
1	UV expose time: 16.5 s, Development: 10 min, Bonding force: 2800 N, Bonding Temp.: 250 °C for 20 min, Heating: RT to 250 °C as fast as the equipment can reach, Cooling: Natural Cooling.	Many voids on the BCB has been observed and it has been decided to increase the wafer bonding time.
2	UV expose time: 25 s, Development: 10 min, Bonding force: 2800 N, Bonding Temp.: 250 °C for 60 min, Heating: RT to 250 °C in 30 minutes, Cooling: Natural Cooling.	It has been observed that bonding had occurred in a limited area on the center of the wafers. In addition to this, the wafers are bonded at the edges of the wafers, although there is not any BCB at the edges. Bonding at the edges occurred between glass and Si wafers. It has been decided to increase the bonding force due to this nonuniform distribution.

3	UV expose time: 40 s, Development: 10 min, Bonding force: 3500 N, Bonding Temp.: 250 °C for 60 min, Heating: RT to 250 °C in 30 minutes, Cooling: Natural Cooling.	The same results are obtained as in trial #2. At this point it has been observed that, BCB was overexposed and the BCB layer was overdeveloped. A drawing regarding the condition of the BCB layer is presented in Figure 4.1. Expose and development times are optimized after this trial.
4	UV expose time: 16.5 s, Development: 5 min, Bonding force: 3500 N, Bonding Temp.: 250 °C for 60 min, Heating: RT to 250 °C in 30 minutes, Cooling: Natural Cooling.	No change has been observed relative to the previous case in the bonding quality.
5	UV expose time: 16.5 s, Development: 4.5 min, Bonding force: 3500 N, Bonding Temp.: 250 °C for 60 min, Heating: RT to 250 °C in 30 minutes, Cooling: Natural Cooling. Flags have been utilized during the wafer bonding in order to prevent any gases (including the gases outgassed by BCB) to be trapped between the wafers.	The results were promising. The bonded areas were increased and bonded areas demonstrated a more uniform distribution on the wafers. However, the efficiency was still low and it is thought that BCB was outgassing at 250 °C, which prevents the bonding in most of the areas.

6	UV expose time: 16.5 s, Development: 4.5 min, Bonding force: 3500 N, Bonding Temp.: 250 °C for 60 min, Heating: RT to 250 °C in 30 minutes, Cooling: Natural Cooling. Flags have been utilized during the wafer bonding in order to prevent any gases (including the gases outgassed by BCB) to be trapped between the wafers. The flags have been removed after the temperature rised to 250 ◦C. The aim was to remove the outgassed gases as well.	No change has been observed relative to the previous cases. A small area at the center and the edges of the wafers were bonded. Figure 4.2 presents a photo of the bonded wafers after trial #6, which shows the bonded areas. Furthermore, a micrograph of the bonded areas at the center can be seen in Figure 4.3. Void and channel formations are thought to be due to outgassing of BCB. It has been decided to hard bake the BCB layer and to use non-patterned BCB in order to see, if the non-uniformity in the bonded areas are due to force non-uniformity in the bonding equipment.
7	Hardbake: 30 min @ 200 ◦C, Bonding force: 3500 N, Bonding Temp.: 250 °C for 60 min, Heating: RT to 250 °C in 30 minutes, Cooling: Natural Cooling.	Success is achieved in trial #7; most of the areas were bonded on the wafers. It is observed that unbonded areas were due to dust particles. It is seen that there was no nonuniformity in the force distribution of the bonding equipment and it is confirmed that hard bake is a necessity in order the BCB not to outgas during the bonding. Bonded wafers can be seen in Figure 4.34 and a closer view of the boundary between the bonded and unbounded areas under the microscope is

		presented in Figure 4.5. In order to do the bonding with patterned BCB, it is decided to form a BCB ring at the edges of the cap wafer whose structure can be seen in Figure 4.6. This ring and its purpose will be investigated in Section 4.2.2.1.
8	UV expose time: 16.5 s, Development: 4.5 min, Hardbake: 30 min @ 200 °C, Bonding force: 3500 N, Bonding Temp.: 250 °C for 60 min, Heating: RT to 250 °C in 30 minutes, Cooling: Natural Cooling.	Success is achieved in trial #8. Nonuniformity of the bonded areas through the surface of the wafers decreased. However, bonding quality is still higher than other areas. Bonded areas increased as well. Figure 4.7 presents two rectangular BCB rings which have been bonded properly.

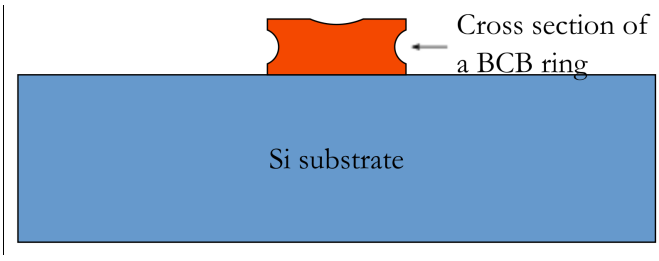

Figure 4.1: Cross section view of a BCB ring, obtained in Trial #3 in Table 4.1

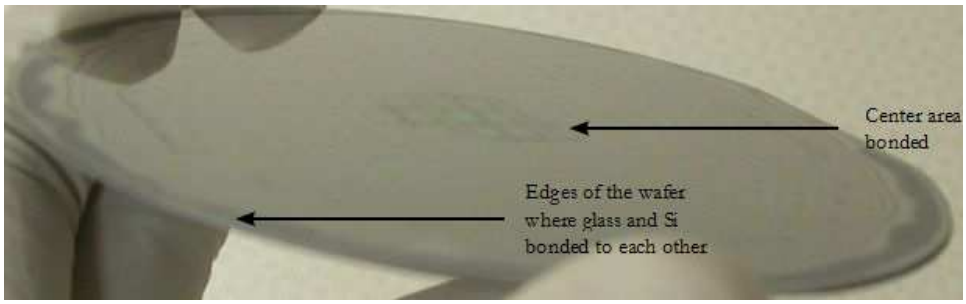

Figure 4.2: Bonded wafers at the end of trial #6

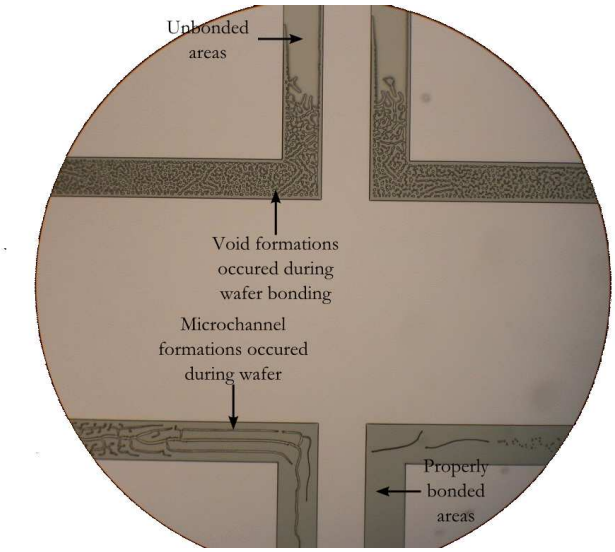

Figure 4.3: A micrograph taken from the center of the wafers, which can be seen in Figure 4.2, for a closer view

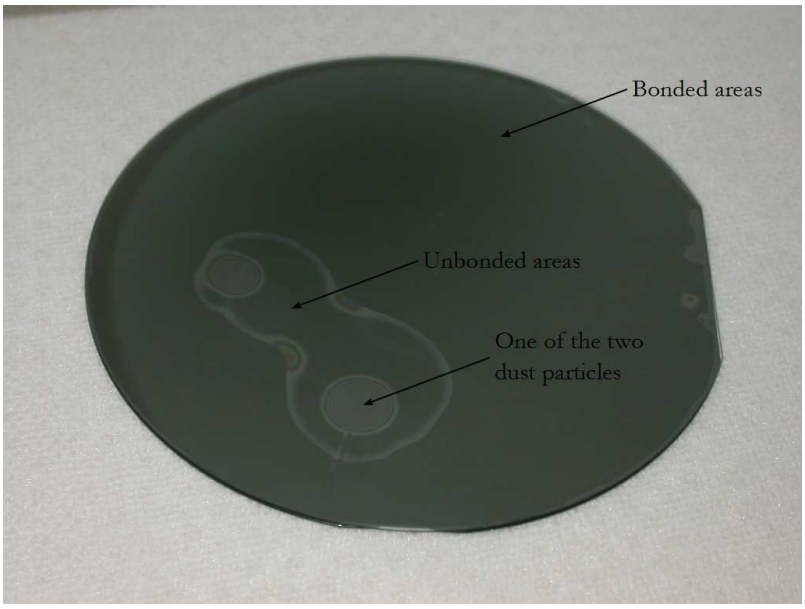

Figure 4.4: Bonded wafers in trial #7

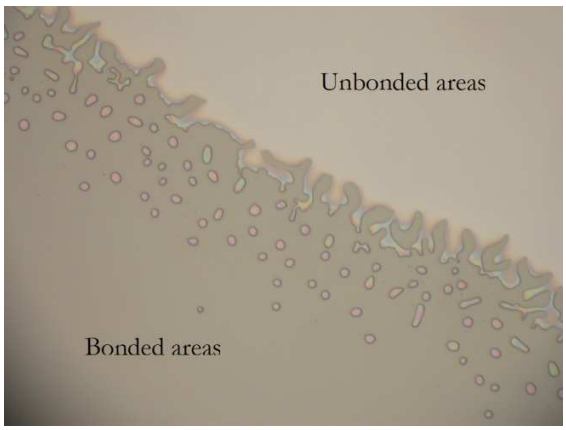

Figure 4.5: Boundary between the bonded areas and unbounded areas of Figure 4.4

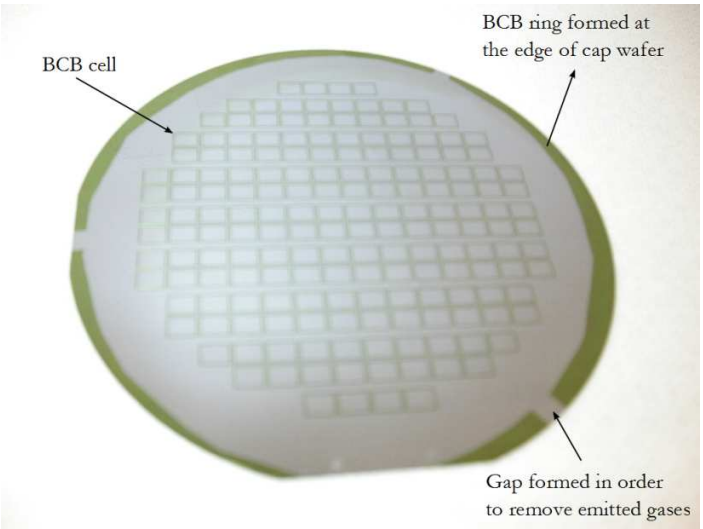

Figure 4.6: A drawing showing top view of the BCB ring at the edge of the cap wafer

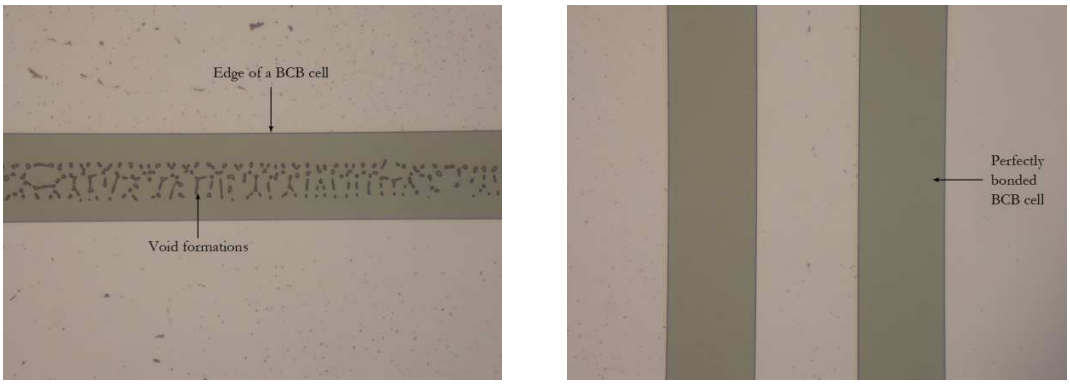

Figure 4.7: Properly bonded two BCB cells

4.2.2.1 Addition of BCB Ring at the Edges of the Cap Wafer

Addition of the BCB ring at the edge of the cap wafer increased the bonded areas and the uniformity of the bonded areas on the wafer surface. The reasoning lies in the wafer bonding equipment. The wafers are placed on top of each other before the bonding and they are attached to the bonder chuck from the edge of the wafers. Since the BCB cells

have a thickness of 5.5 μm thickness at the center, and there is no BCB on the edge of the wafers, the wafer on the top is buckles and takes the shape of a dome. This explains why the edges of the wafers are bonded although there was no BCB and the areas between the edge and center are not. Furthermore, bonding force is applied through a pin to the center of the wafer and this alone explains why the center of the wafers is always bonded better. In order to remove the height difference between the edge of the wafers and center of the wafers, a BCB ring has been placed at the edges and this method worked properly.

4.3 Packaging Process Development Trials with KOH Anisotropic Si Etching

After the optimization of BCB wafer bonding, a KOH anisotropic Si etching based three mask packaging approach has been investigated. Utilized process flow can be itemized as follows;

i) Both surfaces of a 4" Si wafer is oxidized by dry thermal oxidation process resulting in a thickness of 1.2 μm.

ii) SiO_2 on both of the wafer surfaces is patterned with photolithography followed by wet etching of SiO_2 in BHF (Buffered HF) solution. Then, the photoresist layers on both surfaces are stripped.

iii) Cavities and pad windows are formed in a KOH anisotropic Si etching process. It takes 5.5 hours to obtain the pad window openings at 80 °C with a 30% KOH solution.

iv) A handle wafer is attached to the cap wafer by polyimide bands in order to be able to spin coat BCB on the cap wafer. BCB is coated by spin coating at 3300 rpm for a thickness of 5.5 μm.

v) BCB is patterned by photolithography and hardbaked.

vi) Wafer bonding of the cap wafer with a process wafer.

KOH anisotropic Si etching based packaging process has many advantages. Since it is possible to process more than one wafer at a time, it is a time and money saving process. Furthermore, KOH anisotropic Si etching process is a very stable process, whose conditions and results did not change in time. A cap wafer processed with KOH anisotropic Si etching is presented in Figure 4.8. In Figure 4.8, the cap wafer is also attached to a handle wafer with polyimide bands in order to be able to spin-coat BCB. In addition to this, cavities and pad windows are visible in the picture.

Figure 4.8: A cap wafer processed with KOH anisotropic Si etching

BCB processing and wafer bonding parts of the process cycle has been tried with four wafers. Process conditions and results are presented in Table 4.2.

Table 4.2: Process conditions and obtained results for wafer bonding process trials by using cap wafers patterned with KOH anisotropic Si etching

Trial #	Process Summary	Results
1	UV expose time: 16.5 s, Development: 4.5 min, Bonding force: 3500 N, Bonding Temp.: 250 °C for 20 min, Heating: RT to 250 °C in 30 minutes, Cooling: Natural Cooling. Flags have been utilized during the wafer bonding in order to prevent any gases (including the gases outgassed by BCB) to be trapped between the wafers. The flags have been removed after the temperature rised to 250 °C.	The wafers were broken where flags have been utilized. It is decided to remove the flags in the next trial. In addition to this, it is observed that BCB layer was non-uniform in thickness due to the effect of pad windows and cavities. This non-uniformity effect can be seen in Figure 4.9.
2	UV expose time: 16.5 s, Development: 4.5 min, Bonding force: 3500 N, Bonding Temp.: 250 °C for 60 min, Heating: RT to 250 °C in 30 minutes, Cooling: Natural Cooling.	No flags have been utilized, however the wafers were broken again. It is decided to decrease the bonding force. Quality of the adhesion on the non-broken areas was bad due to the non uniformity of the BCB layer.

3	UV expose time: 16.5 s, Development: 4.5 min, Bonding force: 800 N, Bonding Temp.: 250 °C for 60 min, Heating: RT to 250 °C in 30 minutes, Cooling: Natural Cooling.	The wafers were not broken and the aim has been achieved in this sense. However, bonding quality was the same as in the previous trials. It is decided to optimize the uniformity of the BCB layer thickness.
4	UV expose time: 16.5 s, Development: 4.5 min,	It is tried to optimize the BCB thickness uniformity by modifications in the spin coating, however no progress has been achieved. It is decided to increase the vacuum during wafer bonding in order to prove that, bonding quality did not depend on it.
5	UV expose time: 16.5 s, Development: 4.5 min, Bonding force: 800 N, Bonding Temp.: 250 °C for 60 min, Heating: RT to 250 °C in 30 minutes, Cooling: Natural Cooling.	Same results have been achieved in trial #5.

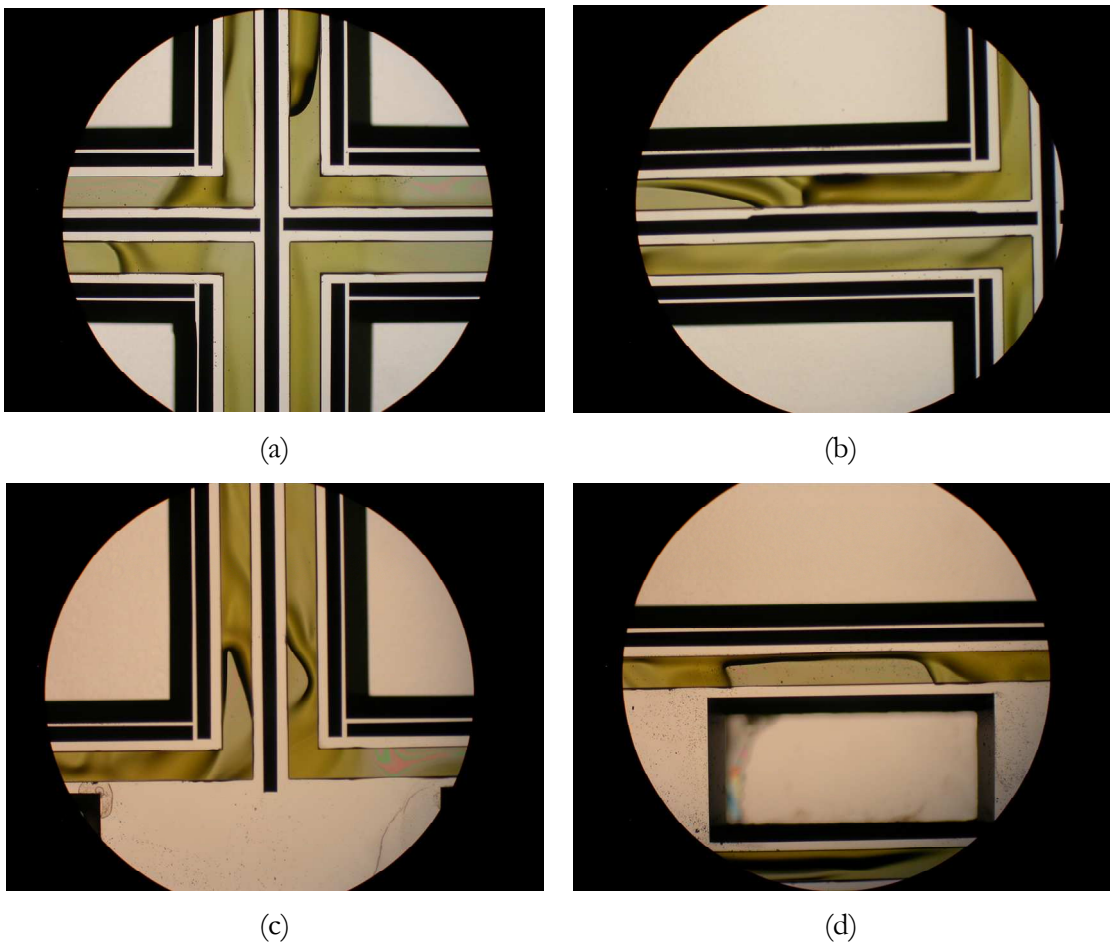

Figure 4.9: BCB layer non-uniformities throughout a wafer utilized in trial #1

Not being able to obtain uniform BCB thickness on the cap wafers due to cavities and pad windows, prevented good bonding quality. It has been tried to optimize the uniformity of the BCB layer thickness, however no progress has been achieved.

After realizing that, spin coating results in non uniform BCB thicknesses, which decreases the bonding quality, spray coating approach has been considered. Due to lack of equipment at that time, this study was carried out together with EV Group. EV Group spray coated

BCB onto Si wafers, which have been processed with KOH anisotropic etching, and sent the wafers back to METU. However, being not able to expose the BCB layer on the wafers uniformly due to side walls of the pad windows and cavities (UV light reflected on the side walls) caused BCB residues to remain on the field. Furthermore, more important than the BCB residues, four wafer bonding trials failed and no good results have been achieved.

Instead of using KOH process for opening cavities and pad windows, DRIE based process cycle has been adopted. It is aimed to obtain uniform BCB layer thickness, which could not be achieved by KOH anisotropic Si etching.

4.4 Packaging Process Development Trials with DRIE

Since it was not possible to spin coat BCB prior to etching of Si and protect it during the KOH anisotropic Si etching process, a uniform layer thickness could not have been achieved. It was then a BCB based process cycle has been considered. As mentioned, the basic idea in this approach is to spin coat BCB layer at a blank wafer and then protect it in the DRIE processes until the cap wafer is totally prepared for wafer bonding. Detailed explanations of the DRIE based process cycle steps are as follows;

i) Spin coating and patterning of photoresist on the back side of a blank Si wafer,

ii) Half-way through DRIE on the backside of the wafer in order to obtain pad window openings from one side and stripping of photoresist,

iii) Spin coating of Cyclotene 4024-40 at 3300 rpm to get 5.5 μm layer thickness and patterning it with photolithography on the front side, followed by hard bake,

iv) Spin coating of photoresist on top of patterned BCB layer, both for protection and as a mask layer in DRIE process,

v) Second half-way through DRIE process from front side in order to have cavities and complete pad window openings and stripping photoresist without damaging BCB layer,

vi) Wafer bonding of the cap wafer with a process wafer.

DRIE based process cycle can be followed through drawings, showing the process cycle step by step starting from Figure 4.10 to Figure 4.14.

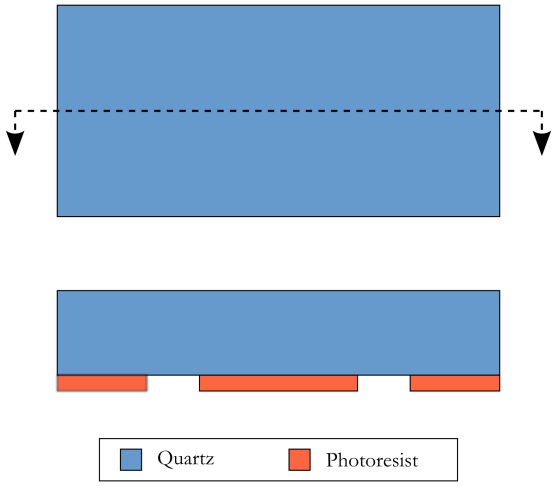

Figure 4.10: Spin coating and patterning of photoresist on the backside

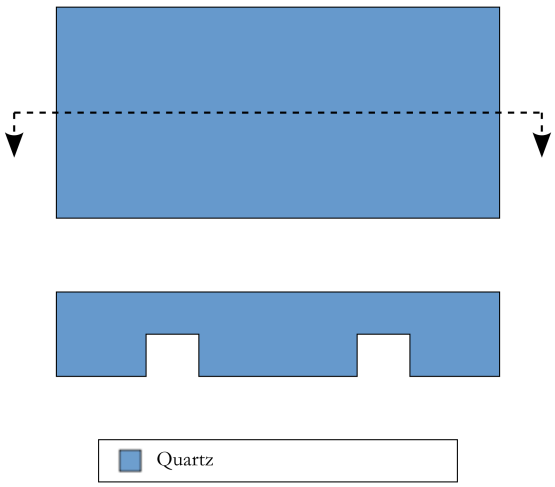

Figure 4.11: Half-way through DRIE on the backside of the wafer in order to obtain pad windows

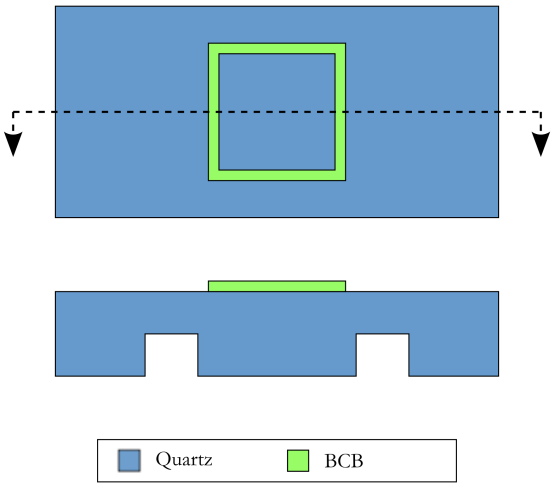

Figure 4.12: Spin coating and patterning BCB on the front side of the wafer

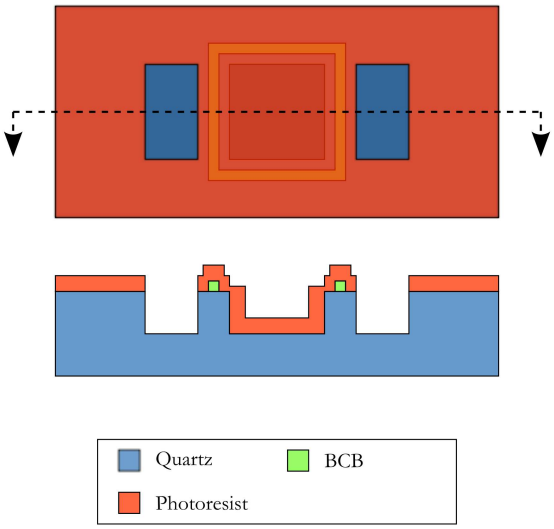

Figure 4.13: Spin coating and patterning photoresist on top of BCB layer on the front side of the wafer

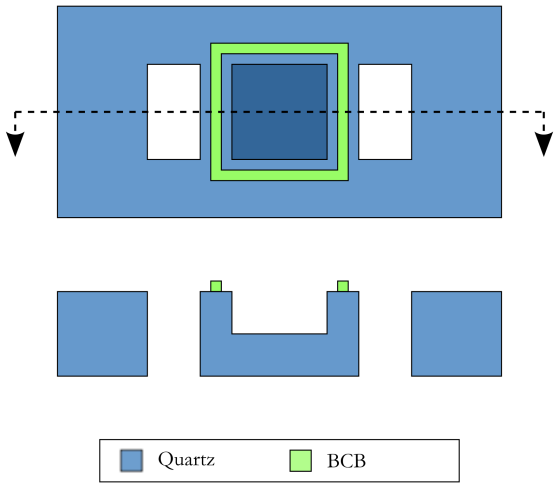

Figure 4.14: Half-way through DRIE on the front side of the wafer in order to obtain both pad windows and cavities

Development steps of the DRIE based packaging process can be divided into two main steps; first DRIE process to obtain half-way pad window openings and the second DRIE step in order to obtain cavities and full-way pad window openings.

4.4.1 Optimization of First DRIE Step and Wafer Bonding

There were some questionable parts about the DRIE based packaging process cycle. One of the possibly problematic parts was the condition, which BCB layer would get after the photoresist on top of it have been stripped away. It was possible to damage BCB layer, while stripping the photoresist layer on top of it. In order to clear this problematic part, different approaches have been considered and tried. First approach was to strip the photoresist layer by wet etching using PRS 2000. The BCB layer in this approach has taken damage and final result was appropriate for packaging. The second approach was to use acetone as the stripper for the photoresist which will not damage hard baked BCB. After this trial, there were small cracks on the BCB layer; however it was possible to use this approach. The final approach on the other hand, gives better results and decided to be utilized. In this approach, photoresist on top of BCB has been stripped by O_2 plasma. By using this method, unharmed BCB layer has been obtained although there were remaining photoresist residues on the field.

A significant mid-step on the DRIE based process cycle was to bond a cap wafer following a DRIE process. It was crucial, not only to check the BCB layer in wafer bonding but also to see if a cap wafer, with cavities on it, is capable of withstanding the wafer bonding process.

Many trials have been completed in order to obtain unharmed BCB layer, after the stripping of photoresist on top of it, utilizing O_2 plasma processes. As a result, a cap wafer with cavities on it was bonded to a blank glass wafer properly. Micrographs of some areas on the bonded wafers and bonded wafers themselves are presented in Figure 4.15. Due to

photoresist residues in the vicinity of BCB rings, BCB layer has flood over in some of the areas.

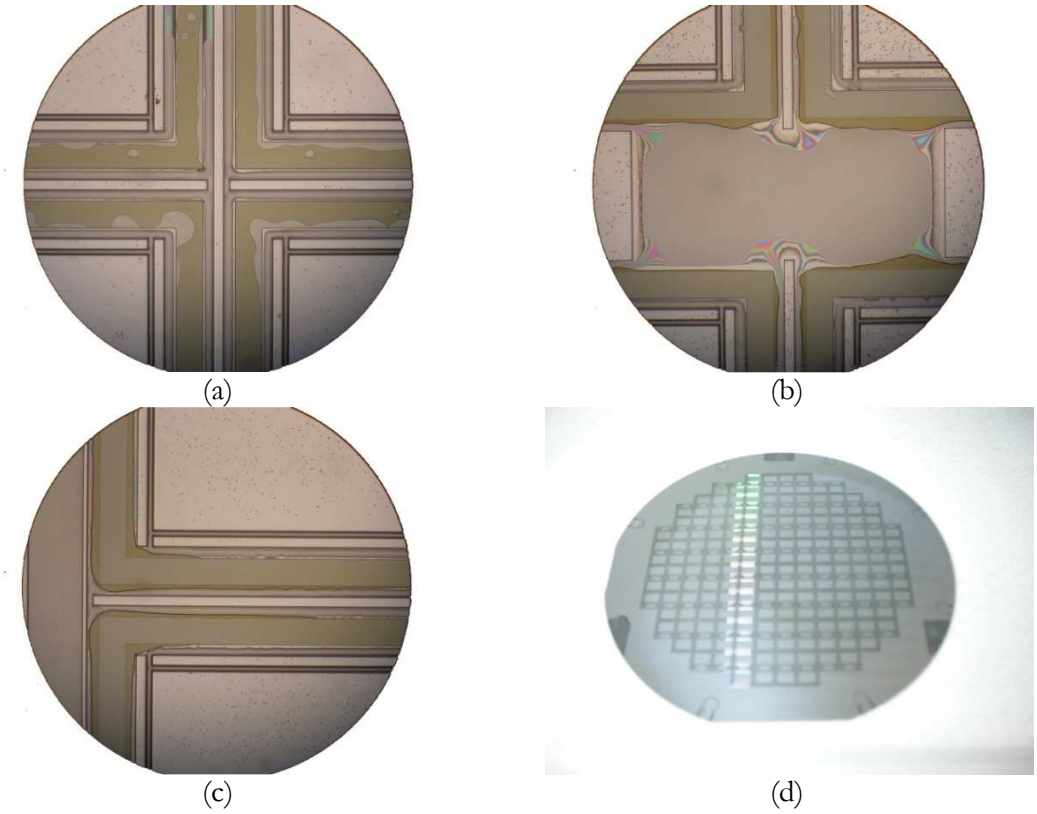

Figure 4.15: Bonded areas and bonded wafers themselves of a successful wafer bonding trial where cavities have been formed on the cap wafer

Obtaining good results in wafer bonding with the cap wafers, which have cavities on them, was a great and significant step in the development of the full packaging process. Remaining step was to obtain the same results with a cap wafer, which have both cavities and fully opened pad windows.

4.4.2 Optimization of Second DRIE Step

Since it was available at this point a new mask set has been utilized in the DRIE processes. Pointed out mask set contains the shunt, capacitive contact switches and SPDT switches for 26 GHz and 12 GHz, whose designs, fabrication steps and measurement results have been given in the previous chapters. The layout of the mask set can be seen in Figure 4.16. Although the effects have been minimized, the pattern seen in Figure 4.2 remained throughout the wafer bonding processes. Owing to this pattern and in order to increase the efficiency of the packaging processes, switches to be packaged have been placed near center.

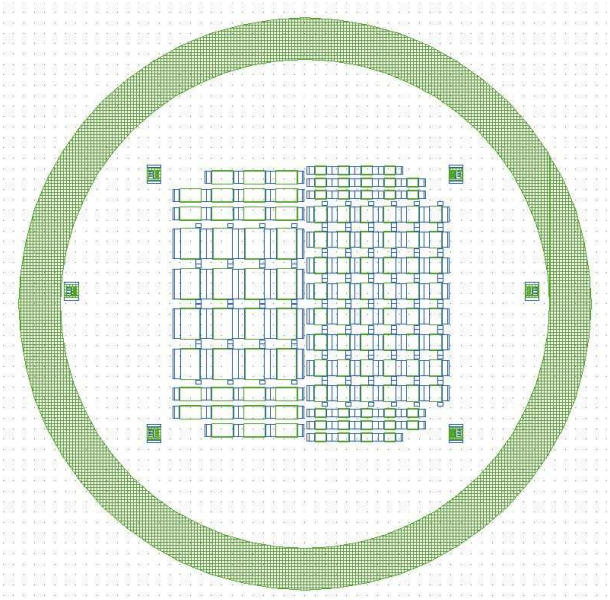

Figure 4.16: Layout of the mask set utilized in the packaging trials showing the distribution of the devices to be packaged on a wafer

While trying to optimize DRIE processes many Si wafers have been utilized with different thicknesses. At the beginning, wafers with thicknesses 500 μm and 150 μm have been

utilized due to their availabilities. 500 μm wafers were more durable however; it was hard to obtain full way pad window openings in the DRIE process, because the photoresist layers were not able to withstand long process times. 150 μm wafers on the other hand, was easy to process with DRIE, but the wafers could easily broke even during N_2 drying. Due to the problems with both 500 μm and 150 μm wafers, 250 μm wafers have been purchased and effects of the mentioned problems have been minimized. With the new mask set, 250 μm wafers have been started to be utilized and from this point on all the trials have been completed with 250 μm wafers.

In optimizing second DRIE process in the process cycle given from Figure 4.10 to Figure 4.14, some difficulties have been encountered. While trying to solve the encountered problems, some modifications in the process cycle have been done.

4.4.2.1 Thermal Contact Problems During Second DRIE Process

In order to understand the problem in this case, an insight on the DRIE processes is required. DRIE processes are generally used in order to etch Si wafers. It is not only a chemical etching process but also directive etching takes place. SiO_2, Si_xN_y or different kind of photoresists can be utilized as the mask layer in the processes however; photoresists are preferred in most applications due to their easy processing. Due to the directive etching that takes place during the DRIE processes, mask layers are prone to etching as well, which is the actual case. It should be noted that etch rates of the mask layers are insignificant compared to the etch rates of the silicon. Etch selectivity is an important parameter in the DRIE processes.

Etch rates of the photoresist mask layers increases when the temperature increases and the selectivity of the process decreases. Due to the selective etching during the DRIE processes, temperature of the processed wafers increases and this prevents the photoresist layers to survive long. In order to get rid of this problem, processed wafers are cooled by

He gas from underneath during the process. In addition to this, the wafers are fixed on the chuck electrostatically.

While opening pad windows or any other openings on a wafer with DRIE process, the chamber and chuck of the DRIE equipment should be protected. In order to protect the chuck, handle wafers are utilized when opening the holes on the wafers completely. Handle wafers are attached to the process wafers either by an adhesive material or simply with bands. In this kind of processes, He gas cools not the process wafer but the handle wafer and if the contact is not good between the handle wafer and process wafer, thermal conductivity may be affected. This is the exact problem in the packaging approach utilized in this study. Since, the wafer is half-way etched during the first DRIE process, contact area between the handle wafer and process wafer decreases dramatically. The process wafer cannot be cooled by the He gas and photoresist layer could not last during the DRIE processes.

A thermally conductive adhesive material, Crystal Bond, is utilized for attaching the handle wafer to the process wafer. This material is easy to process and most importantly easy to remove after the DRIE processes. It dissolves in methanol easily which makes it preferable. Crystal Bond is utilized in the attachment of handle wafers and process wafers however, another problem occurred in that case. Most probably due to the expansion of the Crystal Bond layer between the wafers, process wafers have broken during the DRIE process in every trial.

After failing with this approach, the process is tried without using handle wafers, in which case thermal contact problem is eliminated. This approach was not preferable at the beginning, because the chamber should be opened afterwards and the chuck should be cleaned. This causes drifts in all the process conditions and time consuming optimizations may be required. The process wafers are completely etched without harming the BCB layer

in this approach however; wafers did brake while removing the wafers from the chamber every time. This was probably due to decreased durability of the wafers.

In order to overcome these problems, packaging approach has been modified. Instead of doing DRIE processes from backside and front side, the process has been modified so that both DRIE steps can be done from front side.

4.5 Modified DRIE Based Packaging Process Cycle

Modified DRIE based approach can be followed through from Figure 4.17 to Figure 4.21.

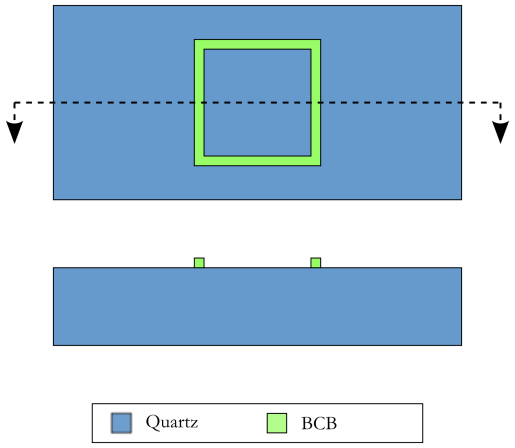

Figure 4.17: Spin coating and patterning and hardbaking of BCB on the front side

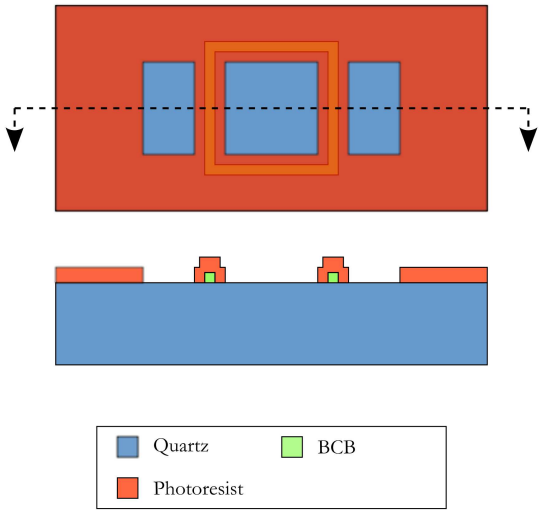

Figure 4.18: Spin coating and patterning photoresist on top of patterned BCB fro first DRIE

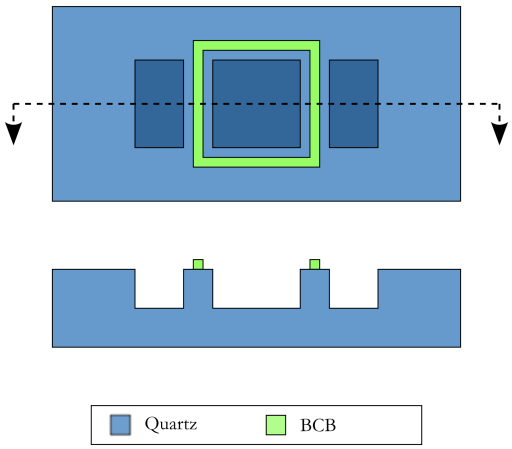

Figure 4.19: Half-way DRIE from the front side including both cavities and pad windows, stripping photoresist

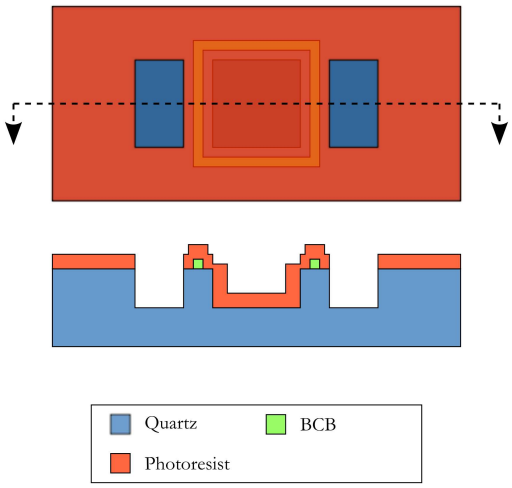

Figure 4.20: Spin coating and patterning of photoresist for second DRIE

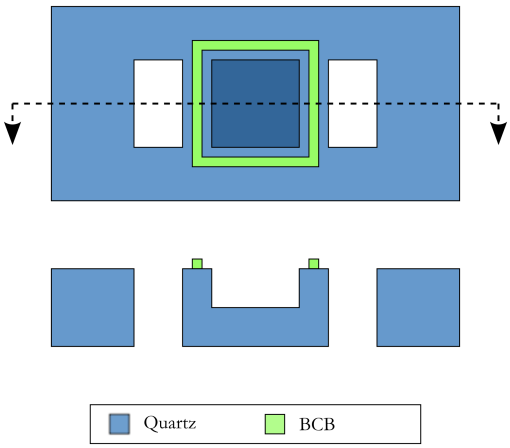

Figure 4.21: Second half-way DRIE in order to have both cavities and pad windows and stripping photoresist

In order to test this approach, test wafers were full-way etched from one side and it is observed that the wafers did not break while removing the wafers from the chamber. Applicability of the modified approach has been proven by this way.

Some trials have been completed by this approach and promising results have been obtained. Only one problem has been observed with this approach. The photoresist layer in the second DRIE did not last long enough to open the pad windows completely. This problem however, may be solved by applying three steps DRIE or by utilizing thicker photoresist layers. This approach could not be completed in the context of this study.

CHAPTER 5

CONCLUSION AND FUTURE WORK

Packaging is an inevitable stage for integrated circuit applications to be used in practical systems. Considering the use of mechanical movement in RF MEMS structures, packaging becomes much more important. Not only the protection from the environmental effects but also the relation of performance to the package and packaging process must be considered all through the design and implementation steps.

There are various methods for IC packaging but applications to MEMS structures are very limited. In this thesis, packaging and consequences of packaging on the performance of RF MEMS structures are studied. Particularly, a zero-level packaging approach considered for the microwave and millimeter wave RF MEMS components is introduced.

Conducted research can be considered as a three step study. As the first step, Ku band and Ka band RF MEMS shunt, capacitive contact switches and RF MEMS SPDT switches have been designed, fabricated and measured. It is shown through RF measurements that the design goals have been achieved.

The SPDT switches studied in the context of this thesis are the very first examples for METU RF MEMS Group. Furthermore, these SPDT switches have been shown to operate at two different operating frequencies (26 GHz and 12 GHz), and it is safe to assume that the design and implementation methods of this SPDT structure can be operational at any frequency. The limitation in this sense may come from the shunt, capacitive contact switches.

As the second step, two zero-level package structures have been proposed and their effects on a shunt, capacitive contact RF MEMS switch operational at 35 GHz [14] are studied. Furthermore, one of the package structures have been utilized with the shunt, capacitive contact RF MEMS switches and SPDT switches realized in the first step of this study.

In both of the package structures, planar feed through approach is adopted and CPW transitions are designed in order to prevent reflections. In addition to this owing to the package effects, resonance frequency of the isolation response may alter. Resonance effects may change the RF MEMS performance. In this step, design modifications on the RF devices have been studied in order to minimize the effects caused by the integrated package structures. By EM simulations, it is shown that both package structures can be utilized for the shunt, capacitive contact RF MEMS switches. Furthermore, especially the second package structure is applicable to many RF MEMS devices and requires very little design modifications.

As the third and final step, a zero-level packaging process cycle is developed. By utilizing bulk micromachining techniques a Si cap wafer is tried to be formed. On this structure there were both cavities and pad window openings. Cavities are used for housing RF MEMS devices and pad windows are opened in order the RF probes to have connection to the device ports. In the wafer bonding processes BCB is utilized as the adhesive and sealing material. BCB is preferred due to its low bonding temperature, semi-hermetic character and ease of process. The research on the development of zero-level packaging process is almost completed and improvement in the realization of pad windows without harming the BCB layer is the only requirement left.

By this work, a zero-level packaging approach that is applicable for RF MEMS devices with movable parts have been studied for the first time in METU RF MEMS Group and many experiences have been gained.

Conclusions achieved during this study are itemized and presented as follows;

- RF MEMS shunt, capacitive contact switches at 26 GHz and 12 GHz operating frequencies have been designed, fabricated and through measurements it is shown that the design goals have been achieved.

- Utilizing RF MEMS shunt, capacitive contact switches as building blocks, two SPDT switches have been realized. Utilized SPDT switch structure has been studied in two different operating frequencies. By this way, a systematic approach of designing SPDT switches at any desired frequency is presented.

- Two zero-level package structures have been studied on a shunt, capacitive contact RF MEMS switch operational at 35 GHz and by design modifications their effects have been minimized.

- One of the package structures have been applied to the realized shunt, capacitive contact switches and SPDT switches, which can be seen as a general solution for RF MEMS packaging.

- The design modifications required to eliminate the effects of packaging are identified and applied to the specific SPDT designs.

- Great improvement has been attained in the development of a zero-level wafer to wafer packaging process utilizing BCB as the adhesive material. A zero-level packaging method applicable to RF MEMS devices with movable parts have been studied for the first time in METU RF MEMS Group.

Attained conclusions and results can be further developed by the following future works;

- Instead of reflective type SPDT switches, absorptive switch structures can be considered and studied. For this study a match load structure for the output ports can be designed and applied to the structures at hand.

- By studying metal contact RF MEMS switches and utilizing them in the SPDT structures, operation bands can be broadened.

- By working on the studied packaging process cycle, a completely developed RF MEMS packaging study can be achieved.

- Since the problems were about obtaining the pad window structures on the development of packaging process, which are required for the measurement purposes, this step can be skipped by a chip to wafer packaging approach. This kind of approach was not possible when this study has started however; METU MEMS Production Facilities now gives the opportunity to work on chip to wafer packaging.

- The implementation steps of the packaging process such as the thermal cycles may have adverse effects to the performance of the switches. Even the lifetime might be effected. Study of these effects and methods to eliminate them are crucial for reliability of the packaged device.

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