DESIGN AND IMPLEMENTATION OF ADVANCED PULSE WIDTH MODULATION TECHNIQUES AND PASSIVE FILTERS FOR VOLTAGE SOURCE INVERTER DRIVEN THREE-PHASE AC MOTORS

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DESIGN AND IMPLEMENTATION OF ADVANCED PULSE WIDTH MODULATION TECHNIQUES AND PASSIVE FILTERS FOR VOLTAGE SOURCE INVERTER DRIVEN THREE-PHASE AC MOTORS

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ABSTRACT

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Advanced pulse width modulation (PWM) techniques such as space vector PWM, active zero state PWM, discontinuous PWM, and near state PWM methods are used in three-phase AC motor drives for the purpose of obtaining low PWM current ripple, wide voltage linearity range, and reduced common mode voltage (CMV). In some applications, a filter is inserted between the inverter and the motor for the purpose of reducing the stresses in the motor. The motor current PWM ripple components, terminal voltage overshoots, shaft voltage, and bearing currents, etc. can all be reduced by means of PWM techniques and passive filters. Various PWM techniques and passive filter types exist. This thesis studies the combinations of PWM techniques and filters and evaluates the performance of the motor drive in terms of the discussed stresses in the motor. PWM techniques are reviewed, a generalized algorithm for the implementation of PWM techniques is developed, and implementation on a 4 kW rated drive is demonstrated. Filter types are studied, among them the common mode inductor and the pure sine filter (PSF) configurations are investigated in detail. Filters are designed and their laboratory performance is evaluated. In the final stage the advanced PWM techniques and

filters are combined, the incompatibility problem of discontinuous PWM methods with the PSF is illustrated. A cure based on rate of change limiter is proposed and its feasibility proven in the laboratory experiments. With the use of the proposed PWM algorithm and PSF, a motor drive with ideal DC to AC conversion stage (DC to pure sine) is achieved and its performance is demonstrated in the laboratory.

Keywords: AC motor, common mode, differential mode, filter, inverter, PWM, rate of change limiter

ÖZ

GERİLİM KAYNAKLI EVİRİCİLERLE SÜRÜLEN ÜÇ FAZLI AA MOTORLARI İÇİN GELİŞMİŞ DARBE GENİŞLİK MODÜLASYON TEKNİKLERİNİN VE PASİF SÜZGEÇLERİN TASARIM VE GERÇEKLENMESİ

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Uzay vektör darbe genişlik modülasyonu (DGM), etkin sıfır durum DGM, süreksiz DGM ve yakın komşu DGM gibi gelişmiş DGM teknikleri üç fazlı AA motor sürücülerde düşük DGM kıpırtısı, geniş gerilim doğrusallığı ve düşük ortak mod gerilimi (OMG) elde etmek amacıyla kullanılır. Bazı uygulamalarda motordaki zorlanmaları azaltmak için evirici ile motor arasında süzgeç kullanılır. Motor akım DGM kıpırtı bileşenleri, motor terminallerinde gerilim aşımları, mil gerilimi ve rulman akımları vb. olumsuz etkiler DGM teknikleri ve pasif süzgeçler yoluyla azaltılabilir. Birçok DGM tekniği ve pasif süzgeç tipi bulunmaktadır. Bu tezde DGM teknikleriyle süzgeçlerin birleşimi üzerine çalışılmakta ve motor sürücünün sözedilen motor zorlanmaları açısından başarımı değerlendirilmektedir. DGM teknikleri gözden geçirilmekte, DGM tekniklerinin gerçeklenmesi için genelleştirilmiş bir algoritma geliştirilmekte ve gerçekleme 4kW'lık bir sürücüde gösterilmektedir. Süzgeç tipleri incelenmekte ve bunlardan ortak mod bobini ile saf sinüs süzgeci (SSS) detaylı olarak incelenmektedir. Bu süzgeçler tasarlanarak laboratuvar başarımları değerlendirilmektedir. Son aşamada gelişmiş DGM yöntemleriyle bu süzgeçler birleştirilmekte, ve SSS'nin süreksiz DGM teknikleriyle

olan uyumsuzluk sorunu gösterilmektedir. Değişim oranı sınırlama yöntemine dayanan bir düzeltme önerilmekte ve uygulanabilirliği laboratuvar deneyleri ile kanıtlanmaktadır. Önerilen DGM algoritması ve SSS kullanılarak ideal bir DA-AA dönüştürücülü motor sürücü elde edilmekte ve başarımı laboratuvar deneyleri ile gösterilmektedir.

Anahtar Kelimeler: AA motor, ortak mod, diferansiyel mod, süzgeç, evirici, DGM, değişim oranı sınırlayıcı

To My Family

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CHAPTER 1

INTRODUCTION

1.1 Three-Phase Voltage Source Inverters as Applied to AC Motor Drives and PWM Rectifiers

Electric energy is widely utilized in almost every field of life. However, in many industrial and residential applications, the AC line power can not be directly utilized, and it should be conditioned according to the required current and voltage form for the application with desired magnitude, frequency, and quality. For this purpose, power conversion devices have been invented. Inserted between the power line and the load, these power converter circuits improve the performance at both sides. Today, various types of power converter circuits are used to connect many industrial and residential loads to the AC power line, and these circuits enhance the system performance, efficiency, and reliability.

Of all the modern power converters, Voltage Source Inverters (VSIs) are the most widely utilized circuits in different kinds of applications with fractions of a kilowatt to megawatt power range. VSIs are DC-AC converters that generate AC output voltages from a DC input voltage. There are various VSI types. Among the well known VSI topologies, shown in Figure 1.1, the three-phase, three-wire, two-level VSI is one of the most widely employed inverter topology for three-phase applications. The three-phase VSI is composed of six controlled semiconductor switches with anti-parallel freewheeling diodes and it provides three-phase AC output voltages with variable frequency and magnitude from a DC input voltage [1].

The three-phase VSIs are widely employed in AC motor drive and utility interface applications requiring high performance and high efficiency [1]. In AC motor drive applications, typically a three-phase full-bridge diode rectifier converts the three phase AC line voltages to DC voltage (Figure 1.2.a). Generally, large capacitors are used to decrease the voltage ripple on the DC bus. Then the DC bus voltage is converter to AC by the VSI, and the AC output voltages are applied to the motor terminals to control the motor speed, position, and torque. In regenerative drive and uninterruptable power supply applications, the VSI topology is also utilized for AC-DC conversion stage (opposite of inverter mode) (Figure 1.2.b). In AC-DC conversion applications, the converter is generally named as PWM rectifier. PWM rectifiers can operate with sinusoidal line currents at a desired power factor and with nearly constant DC output voltage with a small output capacitor. In both rectifier and inverter mode, the power flow is controlled by the VSI switches in a manner to obtain high performance, high efficiency, and reliable operation.

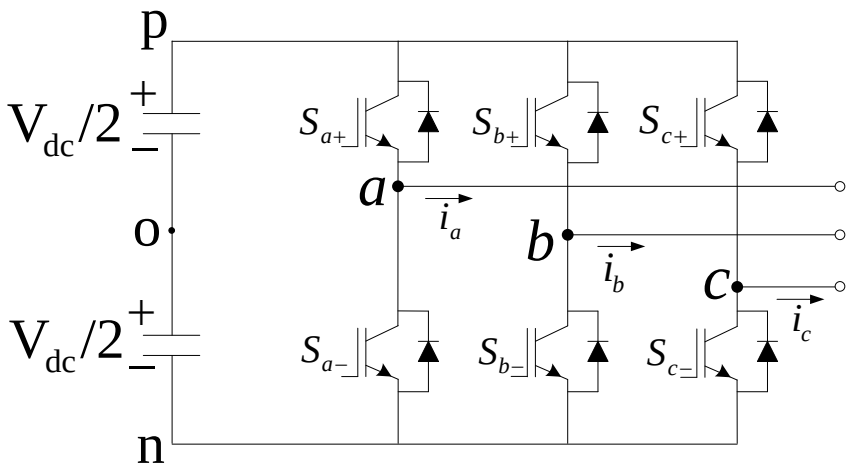


Figure 1.1 The three-phase, three-wire, two-level voltage source inverter circuit topology.

As semiconductor switches, typically, below about hundred volts Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) and at higher voltages Insulated Gate Bipolar Transistors (IGBTs) are utilized. In normal operation mode

of the circuit, the VSI switches are either at conduction or cut-off state, and the upper and lower switches of each inverter leg are gated with complementary logic signals ($S_{a+}=1 \rightarrow S_{a-}=0$). For example, for $S_{a+}=1$ the output voltage (v_{ao}) is $+V_{dc}/2$, and for $S_{a+}=0$ the output voltage (v_{ao}) is $-V_{dc}/2$. In order to avoid short circuit, during switch state transitions both switches of the inverter leg are set to 0 ($S_{a+}=0$ and $S_{a-}=0$) for a short interval named the dead time. During this period, the output current flows through the anti-parallel freewheeling diodes instead of the semiconductor switches, and the polarity of output voltage is determined by the polarity of the output current of the corresponding phase. For example, for $i_a > 0$ the diode of S_{a-} is on thus the output voltage (v_{ao}) is $-V_{dc}/2$, and for $i_a < 0$ the diode of S_{a+} is on thus the output voltage (v_{ao}) is $V_{dc}/2$. As a result, output voltages of the VSI fed by constant DC bus voltage have rectangular waveform. In order to obtain output voltage at desired magnitude and frequency, the VSI switches are turned on and off utilizing the required voltage pulse pattern.

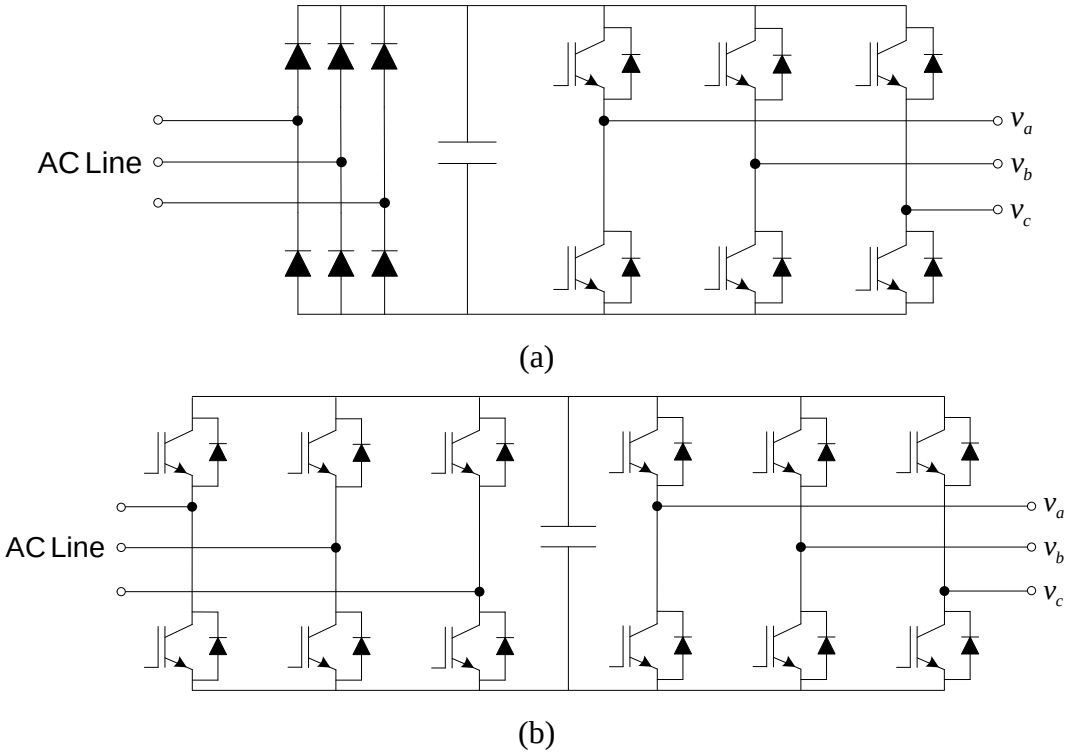


Figure 1.2 The circuit structures of the common VSI drives; (a) diode-rectifier front-end inverter drive, (b) PWM rectifier front-end inverter drive.

1.2 PWM Techniques

In most applications, “carrier-based pulse width modulation (PWM) technique” is used to control the VSI switches due to its low-harmonic distortion characteristics and constant switching frequency. This technique employs “the per-carrier cycle volt-second balance principle” to generate a desired inverter output voltage. According to this principle, in a PWM period, the average value of the output rectangular voltage pulses is equal to the desirable voltage value [2]. There are two main implementation techniques for carrier-based PWM methods: scalar implementation and space vector implementation. In the scalar approach, for each inverter phase, a modulation wave is compared with a triangular carrier wave, and the intersection points determine the switching instants. In the space vector approach, by employing space vector theory the time lengths of the inverter switch states are pre-calculated for each PWM period and the voltage pulses are directly programmed. While with both approaches appropriate pulse patterns yielding high performance can be obtained, the scalar method is simpler and easier to implement, thus it has been the preferred approach [3].

Sinusoidal PWM (SPWM) [4], which is the simplest scalar PWM method, has been used for many decades. However, in three-phase, three-wire inverter applications such as AC motor drives, the inverter performance can be significantly improved by modification of the SPWM pulse pattern. There are various PWM methods proposed in the literature which differ in terms of their voltage linearity range, DC bus and AC output current ripple, switching losses, high frequency common mode voltage (CMV), etc. properties. For example, space vector PWM (SVPWM) [5], discontinuous PWM (DPWM) [6] enhance the voltage linearity range of the inverter (by 15%) compared to SPWM. Utilization of DPWM techniques aids reducing the switching losses of an inverter and enhances the energy efficiency. Further, utilization of CMV reduction techniques such as Active Zero State PWM (AZSPWM) [7] and Near State PWM (NSPWM) [8] provides additional advantages of reducing the influence of high frequency CMV dependent problems (bearing

failure, nuisance trips, etc.) [9], [10]. Therefore, the PWM method to be utilized should be considered along with the application requirements.

1.3 High Frequency Effects of PWM Operation

The PWM-VSI is the standard solution for AC motor drives for high performance and high efficiency. However, the high frequency rectangular output voltage pulses of the PWM-VSI result in undesired effects especially in motor drive applications [9], [11], [12]. Inverter output voltages include high frequency components beside the fundamental frequency component. In order to obtain fundamental output voltage, low-pass filtering at the inverter output is required. In AC motor drive applications, the leakage inductance of the motor partially filters the PWM ripple at the output current. However, when the switching frequency is low or the load inductance is small, the motor PWM current ripple is strong and results losses, thermal stresses, and acoustic noise in the motor [13]. Therefore, in order to reduce PWM ripple, the switching frequency is increased as the switching losses permit [1]. In practical applications the switching frequency is typically 3-25 kHz for kW power levels, and 1-5 kHz at MW levels. Reduction of the turn-on and turn-off transition times of the power semiconductor switches increase the efficiency and allows switchings at higher frequencies. On the other hand, increasing switching speeds causes other problems. For the drives fed by standard utility line-to-line voltage of $400V_{rms}$, the DC bus voltage is approximately 550V. Typically modern IGBTs have turn-on and turn-off times in the range of 0.1-1 μs. For such conditions, the rate of change (*dv/dt*) of the VSI output voltage is approximately 0.5-5 kV/μs. Due to this rapid voltage change, the output voltage generated by a VSI is composed of pulses with sharp edges which result undesired effects on the motor.

One of the important unwanted effects of the sharp edged PWM pulses is the overvoltage appearing across the motor terminals due to the voltage reflection in long cable applications. Especially, when the polarity of the inverter output line-to-line voltages reverses instantaneously, they can have more harmful effects [14].

Due to these overvoltages, insulating breakdown occurs generally at the first coil of the stator phase windings, and in the long term it eventually leads to motor failures.

The high frequency Common Mode Voltage (CMV) is the other important unwanted effect of the PWM pulses with high *dv/dt.* In the standard three-phase VSI, using Figure 1.1 as the reference circuit, the CMV is defined as the instantaneous average of the phase voltages with respect to the DC bus midpoint and can be expressed as follows:

$$v_{cm} = (v_{ao} + v_{bo} + v_{co})/3. \tag{1.1}$$

Since the PWM-VSI can not provide pure sinusoidal voltages and has discrete output voltages, the instantaneous value of the common mode voltage is always different from zero. Excessive CMV with high *dv/dt* results catastrophic problems especially in motor drive applications [9]. Since the distances between the motor windings, rotor frame, and the motor chassis are short, there are equivalent parasitic capacitive paths existing between these layers which become effective at frequencies above about 100 kHz. In practical applications, for safety reasons the conductive motor chassis is grounded. Therefore, high CMV with high *dv/dt* results in high frequency common mode current (CMC) (leakage current) flows from the motor to ground through the parasitic elements of the motor. In motor drive applications, high CMV and CMC can cause negative effects such as inverter-induced bearing currents resulting in bearing failures in a short time, EMI at both the AC grid which feeds the drive and the electronic circuits of the motor drive, and nuisance trips in the system [9].

In the application field, recently, such problems have been increasing due to increasing PWM frequencies [9], [10], [11] and the mitigation techniques for these high frequency effects have been gaining importance.

1.4 Mitigation Techniques For The High Frequency Effects of PWM Operation

Depending on the application, the negative effects of PWM-VSI can be prohibitive. Different applications require specific standards regarding EMI emissions, motor insulation stress, motor bearing currents and shaft voltages, acoustic noise, etc. Therefore, the mitigation of these unwanted effects is mandatory in most applications. Various techniques to mitigate these effects have been proposed in the literature. Passive or active filters inserted between the inverter drive and the motor have been proposed. These filtering methods involve suppressing the effect of the noise created by the inverter through external (additional) devices. In the passive filters, only passive components and their combinations are utilized [13], [15], [16], [17], [18], [19], [20], [21], [22]. Passive filters include the common mode inductor [16], common mode transformer [17], differential mode LC filter [13], [18], differential mode RC type filter [19], and their combinations. In the active filters, semiconductor switches are utilized as well as passive components [23], [24], [25]. While some of these filters solve only line-to-line voltage or common mode voltage problems, some of them provide a complete solution for most/all of the undesired effects of PWM. An alternative approach involves reduction the noise from the inverter (where it is generated) by PWM switching pattern control or by means of inverter topology change (such as utilizing the three-level VSI [26], instead of the two-level VSI). Reducing the effect from the inverter can decrease the filter size and cost. Therefore, the filters should be considered with the PWM techniques and inverter topology for effective mitigation of PWM originated problems.

1.5 Scope of The Thesis

This thesis mainly focuses on the experimental performance investigation of a three phase, two-level VSI based motor drive using the combinations of various PWM techniques and passive inverter output filters. The most important contribution involves a modification for the high performance discontinuous PWM methods by

means of a rate of change limiter to reduce the inverter stresses in the pure sine filter configuration.

The second contribution involves a generalized scalar PWM approach for the implementation of PWM methods for three-phase, three-wire VSIs, which unites all the PWM methods under one umbrella. Easy and successful implementation of various high performance PWM methods is illustrated for a motor drive.

The final contribution of the thesis is experimental investigation of CMV and CMC characteristics of various PWM methods for the two-level VSI, and a commercial three-level neutral-point-clamped VSI with and without a common mode inductor.
The organization of the thesis is as follows:

In the second chapter, the generalized scalar PWM approach is introduced. Important performance characteristics, such as the voltage linearity and output ripple characteristics, common mode and differential mode voltage characteristics of various PWM methods are reviewed, and then scalar implementation of these PWM methods are discussed.

In the third chapter, the high frequency effects of PWM-VSI are discussed. Generating mechanism and different types of these unwanted effects are discussed in detail. Then, the mitigation techniques for these high frequency effects of PWM are reviewed.

In the fourth chapter, the detailed experimental CMV/CMC reduction performances of various PWM methods in the prototype two-level VSI based drive are investigated. The effects of various common mode inductors on CMV and CMC are also investigated. The performance of the two-level VSI is compared with a commercial three-level NPC-VSI. Finally, the combination of CMV/CMC reduction techniques is proposed for optimum overall performance.

In the fifth chapter, first the operation of the pure sine filter (PSF) is described. Second, the performance issues arising from the PSF and PWM method combinations are discussed. Following the design of the PSF, the rate of change limiter approach is introduced. Finally, the improved performance results are reported via detailed simulations and experiments.

The sixth chapter provides the summary of the thesis and comments on future research opportunities in this field.

CHAPTER 2

GENERALIZED SCALAR PWM APPROACH FOR THREE-PHASE, THREE-WIRE VOLTAGE SOURCE INVERTERS

2.1 Introduction

Three-phase, three-wire Voltage Source Inverters (VSIs) are widely employed in AC motor drives and utility interface applications requiring high performance and high efficiency [3]. In Figure 2.1, the standard three-phase two-level VSI circuit diagram is illustrated. The classical VSI generates AC output voltage from DC input voltage with required magnitude and frequency by applying high frequency rectangular voltage pulses. "The carrier-based pulse width modulation (PWM) technique is the standard approach in most VSI applications due to the low-harmonic distortion characteristics with well-defined harmonic spectrum, fixed switching frequency, and control and implementation simplicity [3]".

"Carrier-based PWM methods employ the per-carrier cycle volt-second balance principle to program a desirable inverter output voltage waveform [3]". In every PWM cycle, the reference voltage, which is fixed over the PWM cycle, corresponds to a fixed volt-second value. According to the volt-second balance principle, the inverter output voltages made of rectangular voltage pulses must result in the same volt-seconds as this reference volt-second value.

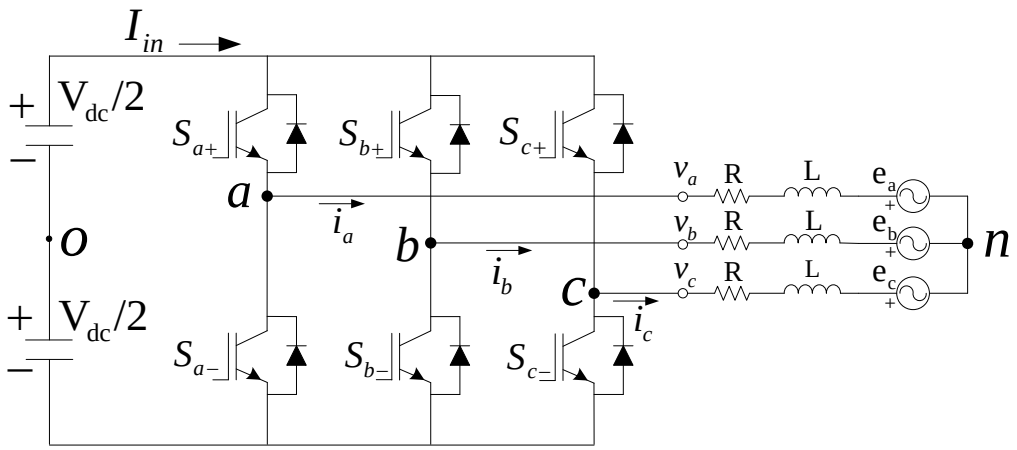


Figure 2.1 The circuit diagram of a VSI connected to a three-phase load.

There are two main implementation techniques for carrier-based PWM methods: scalar implementation and space vector implementation. In the scalar approach, as shown in Figure 2.2, for each inverter phase, a modulation wave is compared with a triangular carrier wave [using analog circuits or digital hardware units (PWM units) as conventionally found in motor control microcontroller or DSP chips] and the intersection points determine the switching instants for the associated inverter leg switches. In the space vector approach, as illustrated in the space vector diagram in Figure 2.3, the time lengths of the inverter states are pre-calculated for each carrier cycle by employing space vector theory and the output voltage pulses are directly programmed [1], [5]. The mathematics involved in the scalar method modulation waves and the space vector calculations is related. With proper modulation waves, the scalar and space vector PWM pulse patterns can be made identical [1]. Thus, both techniques may have equivalent performance results. But the scalar approach is simpler than the space vector approach from the implementation perspective as the involved computations are generally fewer and less complex [1], [3], [5], [27], [28], [29], [30], [31], [32].

Based on the scalar or vector approach, there are various PWM methods proposed in the literature which differ in terms of their voltage linearity range, ripple voltage/current, switching losses, and high frequency common mode

voltage/current properties. The conventional sinusoidal PWM (SPWM) [4], space vector PWM (SVPWM) [5], discontinuous PWM1 (DPWM1) [6], and the recently developed active zero state PWM (AZSPWM) methods [7], [33], near state PWM (NSPWM) [8], and remote state PWM (RSPWM) [34] methods, are a few (and the most important ones) to name. In particular, the last few have been recently developed with the quest for reducing the CMV magnitude of the VSI [35]. However, implementation of these methods is not easy and not reported in the literature to sufficient depth. Furthermore, the relation between the conventional and recently developed reduced CMV (RCMV) PWM methods is not well understood both in terms of implementation characteristics and performance characteristics. Therefore, difficulties arise in implementing and understanding the performance attributes of these PWM methods.

In this chapter, first, PWM principles and pulse patterns and performance of the popular PWM methods are reviewed. Then a generalized scalar approach that treats the conventional and RCMV-PWM methods, and unites most methods under one umbrella, is established. Also guidance for simple practical implementation which is favorable over the conventional methods (space vector or scalar [1], [3], [4], [27], [28], [29], [30], [31], [32]) is provided. The experimental results verify the feasibility of the proposed approach.

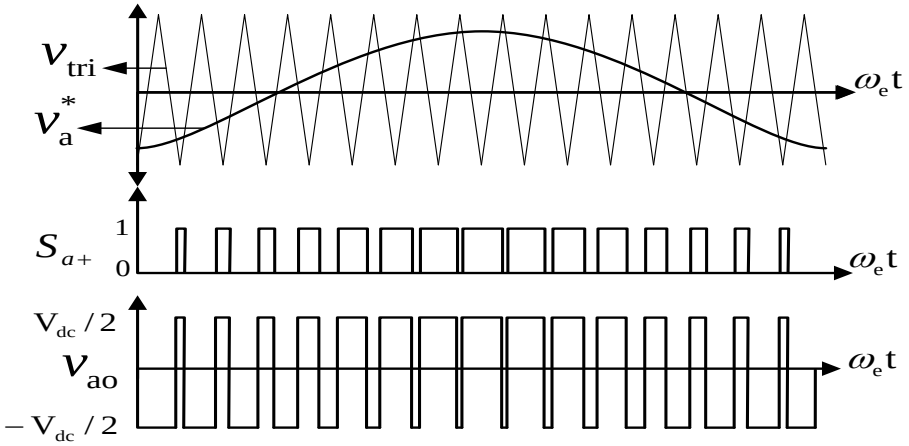


Figure 2.2 Triangle intersection PWM phase "a" modulation wave v^*_a, switching signal and v_{ao} voltage.

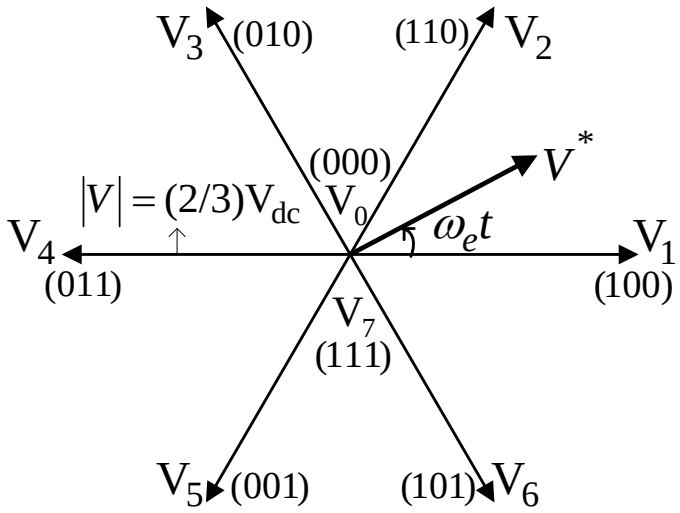


Figure 2.3 Voltage space vectors of three-phase two-level inverter, the upper switch states (S_{a+}, S_{b+}, S_{c+}) "1" (on) and "0" (off) state.

2.2 Review of The Carrier-Based PWM Principles

The PWM approach is based on the "per-carrier cycle volt-second balance" principle, which is a generally applicable principle to all power electronic converters. According to this principle, in a PWM period (T_S), the average value of the output voltage is equal to the reference value. Thus, an output voltage with a desirable value is obtained by creating a reference voltage and matching this reference voltage with the pulse-width modulated inverter output voltages for each PWM period. Therefore, the fundamental constraint in programming the PWM pulses for each phase involves the volt-seconds balance. This principle is illustrated in Figure 2.4.

In scalar PWM, the reference (modulation) wave of each phase (v^*_a, v^*_b, v^*_c) is compared with a carrier wave (v_{tri}) and the intersection points determine the switching instants for switches of the associated inverter phase leg (Figure 2.2). The period of the carrier wave is equal to one PWM period (T_S). In a PWM period, if the modulation wave is larger (smaller) than carrier wave, the upper switch is on (off). The upper and lower switches of each leg operate in complementary manner (S_{a+}=1

→ S_{a-}=0). The per-carrier cycle average value of the voltage of one VSI leg output (v_{ao}) (phase to DC bus midpoint voltage) is equal to the reference value of that leg (v^*_a) due to the volt-second balance principle. The fundamental output voltage (may be obtained by removing the PWM ripple from the output voltage) has the same waveform as the modulation wave. If a sinusoidal fundamental output voltage is wanted, then a modulation wave consisting of sinusoidal form with proper fundamental frequency and magnitude is compared with the high frequency carrier wave.

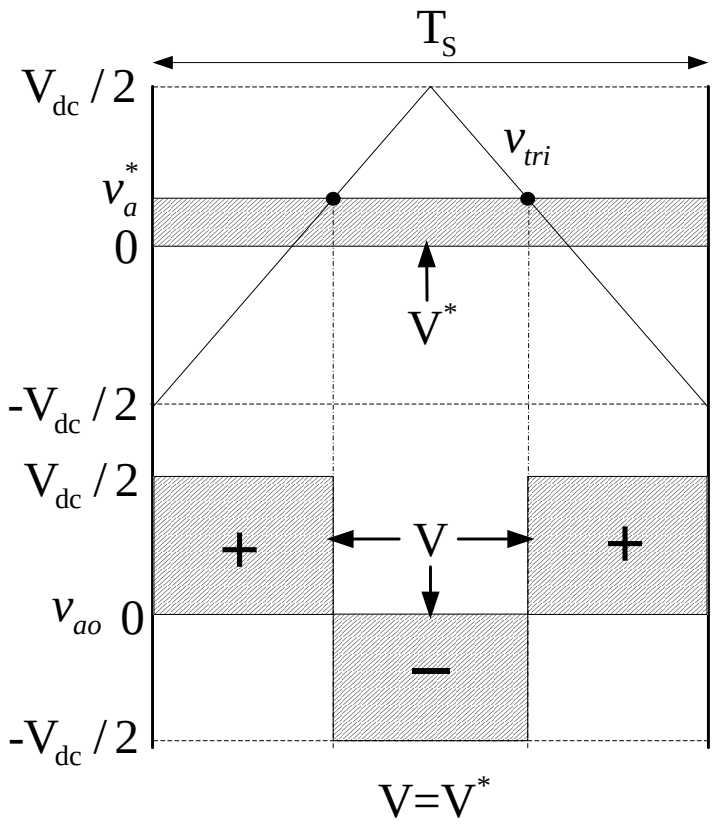


Figure 2.4 An illustration of the per-carrier cycle volt-second balance principle.

In a three-phase VSI, under balanced operating conditions, the reference voltages of each leg have the same shape but they are 120° phase shifted from each other. To obtain sinusoidal output voltages, in the scalar implementation three symmetric and 120° phase shifted sinusoidal modulation waves are compared with the carrier wave

and this method is called as the conventional sinusoidal PWM (SPWM) method, which has been used in motor drives for many decades [4]. However, in three-phase, three-wire VSIs, constraining the reference modulation waves to pure sinusoidal form is not favorable in most cases, as will be discussed in the following.

In three-phase, three-wire inverters where the neutral point of the load is isolated, no neutral current path exists (except for very high frequencies where circuit parasitic capacitances establish a current flow path) and only the inverter line-to-line voltages determine the load current sub-carrier frequency content. Thus, the n-o potential shown in Figure 2.1, which will be symbolized with v_{no}, can be freely varied. In such applications, any common bias voltage [zero-sequence signal (v_0)] can be added (injected) to the SPWM reference voltages (modulation waves). The injection of a zero-sequence signal simultaneously shifts all the reference waves up or down with the same amount (with respect to the carrier wave). Therefore, the average value of line-to-line voltages in one carrier period is not affected. But the positions of the output line-to-line voltage pulses (shown in Figure 2.5) are varied with the zero-sequence signal injection. Therefore, it significantly influences the harmonic distortion, voltage linearity, and switching loss characteristics [1], [3], [36], [37].

With a proper zero-sequence signal injection (theoretically, infinite choices exists [3]), the overall inverter performance increases substantially over SPWM. Ever since this advantage has been understood, the zero-sequence signal injection technique has been in wide utilization in practice. Obtained with zero-sequence signal injection, SVPWM [3], [5], [37] and DPWM1 [6], [38] are two highly popular examples.

In three-phase, three-wire VSIs, not only the modulation waves, but also the carrier waves are per phase and can be arbitrarily selected. The carrier waves may be triangular or sawtooth, for each phase. The carrier of a phase may be phase shifted with respect to the carriers of other phases. It may even be at a different frequency. In all these cases, the volt-seconds balance is not affected and the per-carrier cycle

average value of the VSI leg output voltage is retained. In three-phase VSIs, conventionally one common triangular carrier wave is utilized for all phases due to its symmetric switching sequence which results in low harmonic distortion, low switching loss, and “one switching at a time” characteristics. While this constraint allows easy implementation of conventional PWM methods, it also constrains the variety of PWM methods with the scalar implementation, as will be discussed in section 2.4.

The above discussions indicate that in the scalar implementation both the zero-sequence signal and the carrier signals allow degrees of freedom to obtain various PWM pulse patterns with substantial differences in performance. While some of these possibilities have been explored in the past, some others are undiscovered. Section 2.4 will formally treat the subject and explore the possibilities. However, the space vector approach, as a different approach to form the PWM pulse pattern from the scalar approach requires a brief review at this stage. This is because some PWM methods with favorable pulse patterns have been first invented based on the space vector approach [7], [33], [34] and their scalar equivalents will be found during the above discussed exploration state. While the space vector implementation of such pulse patterns is laborious, to be obtained with aid of the generalized scalar PWM approach, the scalar method based equivalents are easy to implement. Thus, it is important to show the pulse pattern equivalency and implementation advantage.

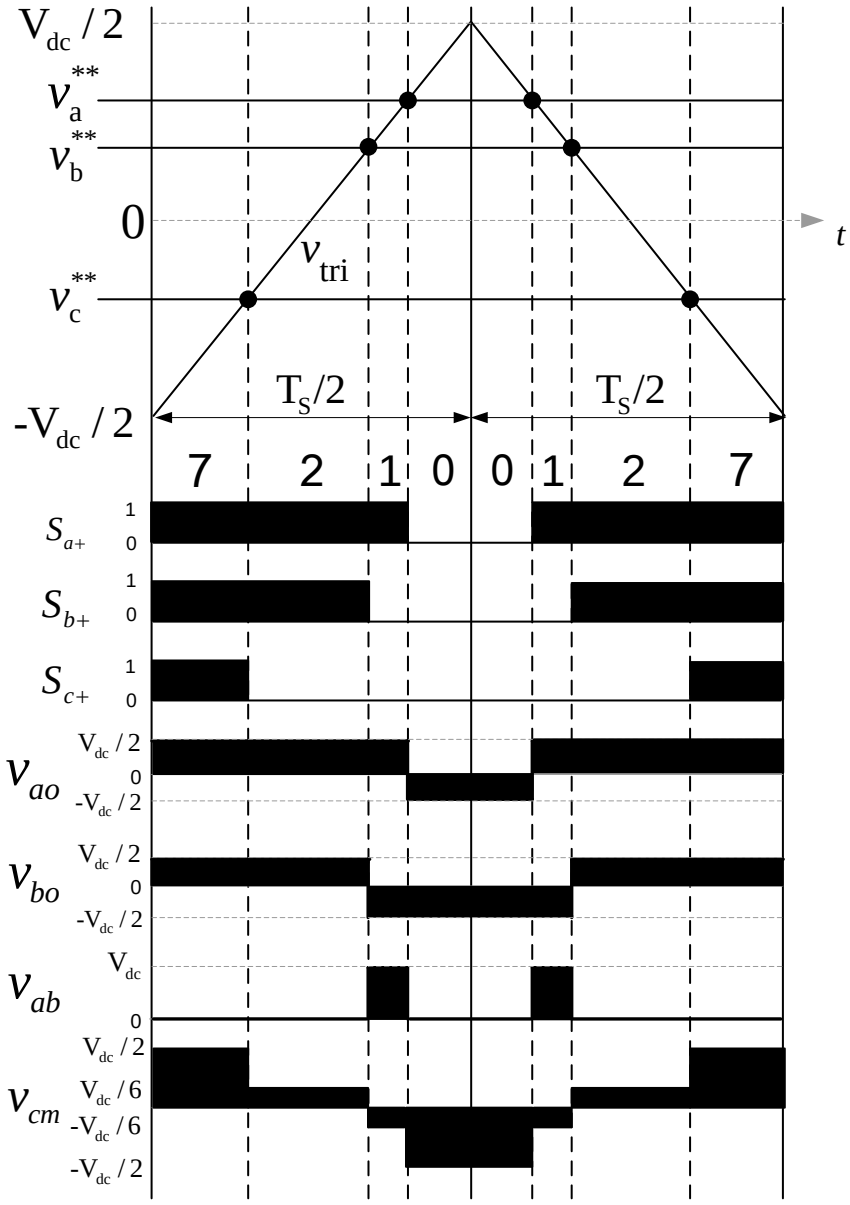


Figure 2.5 The per-carrier cycle view of switch signals, and the resulting phase-to-midpoint, line-to-line, and common mode voltages.

In the space vector implementation, using the complex variable transformation, the time domain phase reference voltages are translated to the reference voltage vector (V^*) with the magnitude (V_{1m}^*) which rotates in the complex coordinates with the $\omega_e t$ angular speed (Figure 2.3) in the following:

$$V^* = \frac{2}{3}\left(v_a^* + a v_b^* + a^2 v_c^*\right) = V_{1m}^* e^{j\omega_e t}, \text{ where } a = e^{j\left(\frac{2\pi}{3}\right)} \tag{2.1}$$

Since there are eight possible inverter states available, the vector transformation yields eight voltage vectors as shown in Figure 2.3. Of these voltage vectors, six of them (V_1, V_2, V_3, V_4, V_5, V_6) are active voltage vectors, and two of them (V_0 and V_7) are zero voltage vectors (which provide degree of controllability similar to the zero-sequence signal of the scalar implementation) which generate zero output voltage. In the space vector analysis, the duty cycles of the voltage vectors are calculated according to the vector volt-second balance rule defined in (2.2) and (2.3), and these voltage vectors are applied with the calculated duty cycles.

$$\sum_{k=0}^{7} V_k t_k = V^* T_S \tag{2.2}$$

$$\sum_{k=0}^{7} t_k = T_S \tag{2.3}$$

Each PWM method utilizes different voltage vectors, vector time lengths, and sequences. Therefore, the vector space is divided into segments. There are 6 A-type and 6 B-type segments available as shown in Figure 2.6. Investigations reveal that all space vector PWM methods utilize either A-type or B-type segments, and the utilized voltage vectors of these PWM methods alternate at the boundaries of the corresponding segments [35]. For example, the space vector implemented SVPWM, AZSPWM1, and AZSPWM3 utilize A-type, NSPWM and RSPWM3 utilize B-type segments [8], [35].

In the space vector approach, the implementation is straightforward, but quite laborious [1], [5], [27], [28], [29], [30], [31], [32]. The space vectors segments must be found and vector duty cycles must be calculated. Then, given a vector sequence, the phase switch duty cycles are calculated and loaded to the PWM counter of the PWM generator of a control board of the VSI. Should the reference voltage tip

point fall out of the inverter voltage hexagon (overmodulation condition [39], [40]), then corrections to the vector duty calculations or re-calculations with the modified reference vector become necessary. Thus, the direct space vector implementation is always a difficult task for a PWM generator. The generalized scalar PWM implementation approach overcomes the involved procedure and computations. Before introducing this approach, the review of various PWM methods and their pulse patterns is provided in the next section.

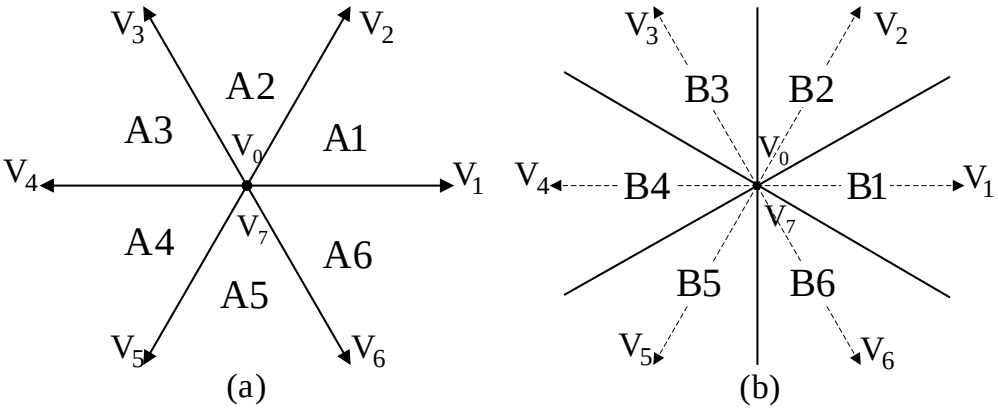


Figure 2.6 Voltage space vectors and 60° sector definitions: (a) A-type, (b) B-type regions.

2.3 Pulse Patterns and Performance Characteristics of Various PWM Methods

There are a large number of PWM methods and each method with unique pulse pattern yields unique performance characteristics. Thus, full investigation of all PWM methods in regard to their pulse pattern and performance is a laborious task. However, the theoretically infinite choice of methods, in practice reduces to a relatively small count when a systematic evaluation and performance comparison (among the many methods) is made. References [1], [3], and [35] involve such thorough investigation of large count of PWM methods. This section aims to review the most important PWM methods with the focus on their pulse patterns such that in the following section their implementation by generalized scalar approach can be

discussed to sufficient depth. Observing the pulse patterns, the performance characteristics can be studied, and thus major advantages and drawbacks of these methods can be recognized. Therefore, while reviewing the pulse patterns, it will also be possible to demonstrate why some of these methods are so well accepted. Since the pulse patterns and performances of the PWM methods are discussed, the space vector approach is used in this section.

The performance characteristics of a PWM method are primarily dependent on the modulation index (M_i, voltage utilization level). "For a given DC bus voltage (V_{dc}), the ratio of the fundamental component magnitude of the line to neutral inverter output voltage (V_{1m}) to the fundamental component magnitude of the six-step mode voltage (which is defined in (2.4)) is termed the modulation index M_i [3]" and expressed as (2.5).

$$V_{1m-6-step} = 2V_{dc} / \pi \tag{2.4}$$

$$M_i = V_{1m} / V_{1m-6-step} \tag{2.5}$$

In this section PWM methods are classified based on the CMV characteristics as conventional PWM methods and Reduced CMV PWM (RCMV-PWM) methods since recently reported various PWM methods have been invented with the aim of CMV reduction. Conventional PWM methods utilize at least one of the two zero-voltage vectors V_0 and V_7, which results a CMV of $-V_{dc}/2$ and $V_{dc}/2$. On the other hand, RCMV-PWM methods do not utilize zero states, thus they avoid a CMV with a magnitude of $V_{dc}/2$ and their CMV magnitude is confined to $V_{dc}/6$.

The most common conventional PWM methods are Sinusoidal PWM (SPWM) [4], Space Vector PWM (SVPWM) [5], and Discontinuous PWM1 (DPWM1) [6] methods. As the simplest method, SPWM has been used for many decades. It is implemented by comparing three sinusoidal reference signals with the triangular carrier wave. As discussed in section 2.2, utilizing zero-sequence signal injection,

SVPWM and DPWM1, which have higher performance characteristics compared to SPWM, have been developed. While the voltage linearity range of SPWM is $0<M_i<0.78$, SVPWM and DPWM1 provide extended voltage linearity region ($0<M_i<0.907$). The pulse patterns and voltage vectors of SVPWM and DPWM1 are illustrated in Figures 2.7 and 2.8, respectively. Both PWM methods utilize two active vectors adjacent to the reference voltage vector. While SVPWM utilizes two zero vectors with equal time duration ($t_0=t_7$) in each PWM cycle, DPWM1 utilizes only one of the zero states (V_0 or V_7) and one switch is retained in a fixed state for a full PWM cycle, thus switching losses are decreased by 33% compared to SVPWM as seen in Figure 2.8. As SVPWM has symmetric zero stages, from the PWM ripple reduction perspective it is the best method. But as M_i increases the ripple also increases and it looses its advantage around $M_i\approx0.6$ where discontinuous PWM methods can be used [3]. For example, increasing the PWM frequency by 50% and employing the DPWM1 method, the switching count and therefore the switching losses remain the same (as one of the phases ceases switching during the PWM period) while the ripple of DPWM1 becomes less compared to SVPWM. Due to reduction of the total zero state duty cycles at high M_i and 50% increase of the carrier frequency (decrease of the carrier cycle), the effect of the zero states on ripple decreases and they can be lumped as one [3]. Thus, low ripple or low loss results. The voltage vector sequences for SVPWM and DPWM1 are given in Table 2.1.

Consequently, SVPWM at low M_i, and DPWM1 at high M_i have been widely used. It has been illustrated that transition between methods is seamless (the load current is not disturbed) and a combination of the two methods has been successfully used in commercial drives. However, for both SVPWM and DPWM1, as shown at the bottom of the pulse pattern diagrams, the inverter CMV magnitude is high ($V_{dc}/2$). In motor drive applications, higher CMV is associated with increased common mode current (motor leakage current), higher risk of nuisance trips, and reduced bearing life [11], [14], [43], which will be explained in detail in the next chapter.

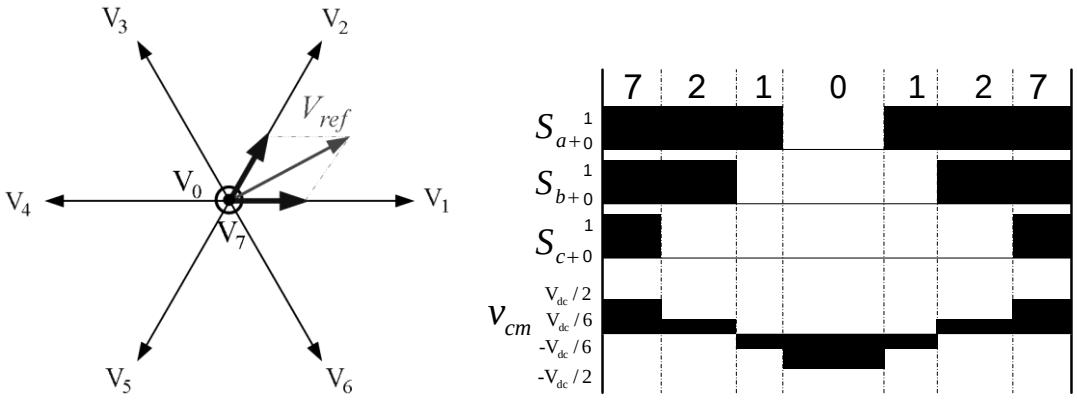


Figure 2.7 Voltage space vectors and pulse pattern of SVPWM for the region A1.

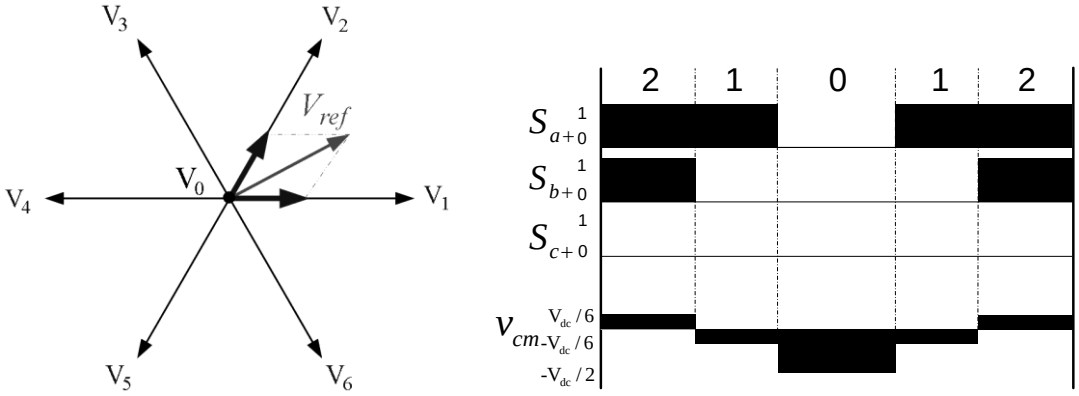


Figure 2.8 Voltage space vectors and pulse pattern of DPWM1 for the region A1∩B2.

Table 2.1 Voltage vector sequences of SVPWM and DPWM1

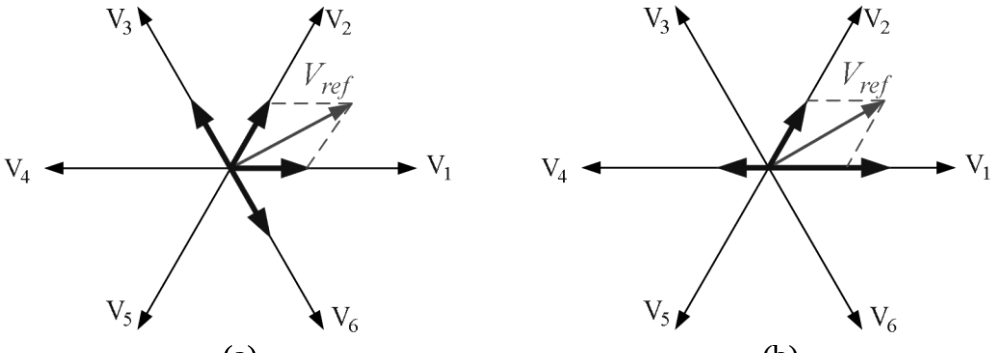
SVPWM	A1	A2	A3	A4	A5	A6
	7210127	7230327	7430347	7450547	7650567	7610167

DPWM1	B1	A1	B2	A2	B3	A3	B4	A4	B5	A5	B6	A6	B1
	72127		23032		74347		45054		76567		61016		
		21012		72327		43034		74547		65056		76167	

Recently, several PWM methods that reduce the CMV have been reported. Of these methods, active zero state PWM1 (AZSPWM1) [7], AZSPWM2 [33], AZSPWM3 [7], remote-state PWM1-2-3 (RSPWM1-2-3) [34], and near state PWM (NSPWM) [8] are the most important ones and they will be reviewed in the following. Since they do not utilize zero states, RCMV-PWM methods avoid a CMV with a

magnitude of $V_{dc}/2$ and their CMV magnitude is confined to $V_{dc}/6$. Thus, these methods can be favorable over SVPWM and DPWM1 in CMV sensitive applications. Since the aim is to avoid zero states (V_0 and V_7), these methods have been first invented based on space vector theory. Therefore, in this section their space vector representations are given. The equivalent scalar implementation of them will be provided in the next section.

AZSPWM methods [7], [33] utilize the same active vectors as in SVPWM. However, instead of the real zero voltage vectors (V_0 and V_7), two active opposite voltage vectors with equal time duration are utilized to create an effective zero vector. Any of the three opposite vector pairs (V_1V_4, V_2V_5, V_3V_6) can be selected. In AZSPWM1 and AZSPWM2, the adjacent pair is utilized. For example, in A1 region, the V_3V_6 pair is utilized since these vectors are adjacent to the V_1V_2 vectors (Figure 2.9.a). The difference of AZSPWM1 and AZSPWM2 is the sequence of the active zero vectors. While AZSPWM1 involves only 60° vector rotation, AZSPWM2 involves 120° rotation as well as 60° rotation (Figure 2.10). In AZSPWM3, the active zero vectors are obtained by utilizing one of the active voltage vectors and its opposite vector (Figure 2.9.b). For example, in A1, the V_1V_2 active vectors are complemented with the V_1V_4 (alternatively with V_2V_5) active zero pair. Thus, only three active voltage vectors $V_1V_2V_4$ are utilized to program the reference voltage. The vector sequence of AZSPWM methods are given in Table 2.2.



(a) (b)

Figure 2.9 Voltage space vectors of (a) AZSPWM1-2 (b) AZSPWM3 for the region A1.

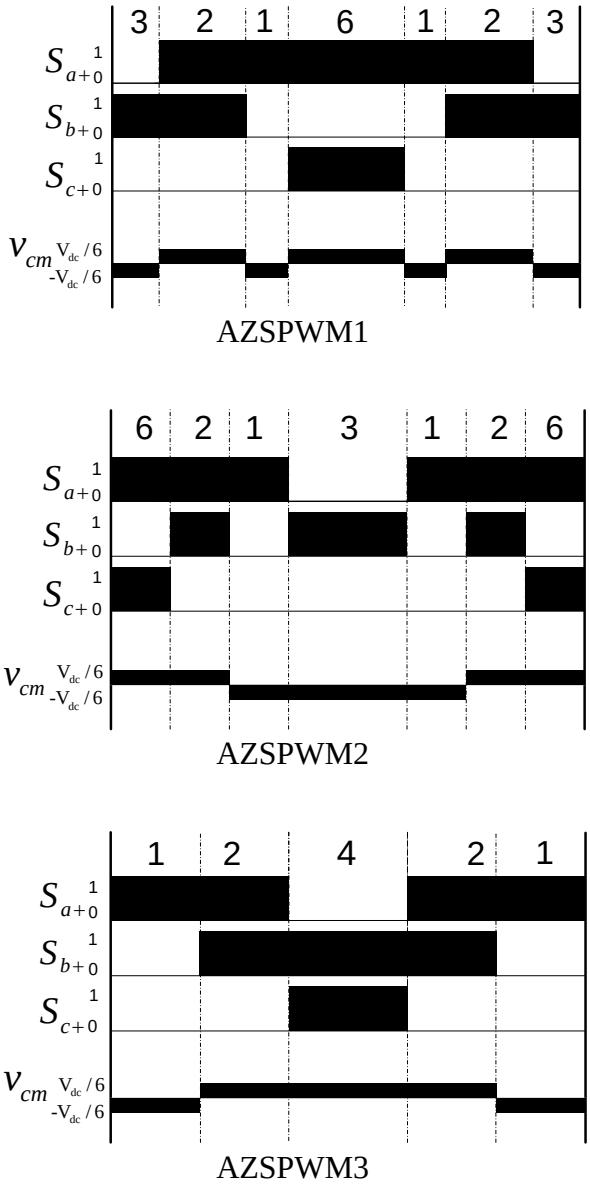


Figure 2.10 Pulse patterns of AZSPWM methods for the region A1.

Table 2.2 Voltage vector sequences of AZSPWM methods

	A1	A2	A3	A4	A5	A6
AZSPWM1	3216123	4321234	5432345	6543456	1654561	2165612
AZSPWM2	6213126	1324231	2435342	3546453	4651564	5162615
AZSPWM3	12421	23532	34643	45154	56265	61316

RSPWM methods [34] obtain the reference voltage from three active voltage vectors that are 120° apart from each other (most remote vectors). They utilize the

vector group $V_1V_3V_5$ and/or $V_2V_4V_6$ in various sequences. They are divided into three subgroups according to the utilized voltage vector groups and their sequences. RSPWM1 utilizes only one vector group (either $V_1V_3V_5$ or $V_2V_4V_6$) and applies the vectors in a fixed sequence. Since each vector group and vector sequence have equivalent performance only the sequence (V_3-V_1-V_5-V_1-V_3) is considered as RSPWM1. Also in RSPWM2, only one group is utilized. However, in this case, the sequence is varied in a specific manner in order to minimize the output voltage distortion. Two patterns that yield relatively good voltage quality performance are given in Table 2.3 as RSPWM2A (utilizes $V_1V_3V_5$) and RSPWM2B (utilizes $V_2V_4V_6$). Since these two pulse patterns have equivalent performance attributes, only RSPWM2A is considered as RSPWM2. RSPWM3 utilizes both vector groups ($V_1V_3V_5$ and $V_2V_4V_6$) which are alternated every 60°, and the vector sequence varies as shown in Table 2.3, according to the region definitions in Figure 2.6.b.

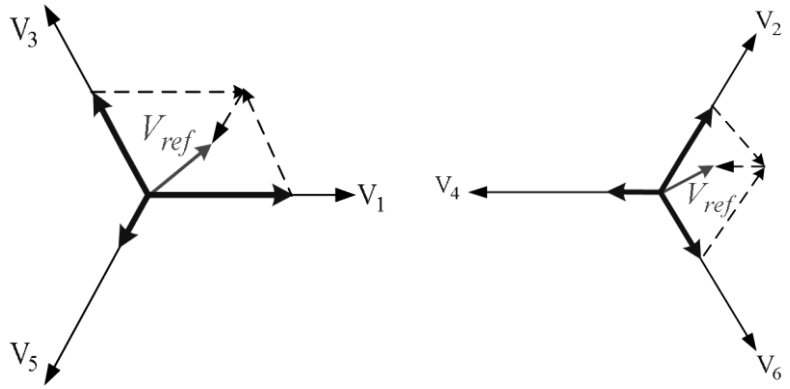


Figure 2.11 Voltage space vectors of RSPWM methods (a) $V_1V_3V_5$, (b) $V_2V_4V_6$.

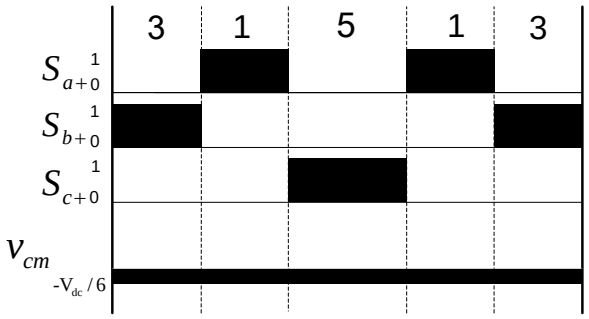


Figure 2.12 Pulse patterns of RSPWM1 (region A1) and RSPWM3 (region B1).

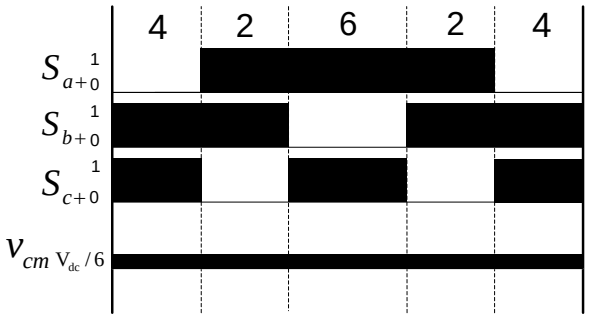


Figure 2.13 Pulse pattern of RSPWM2B for the region A1.

Table 2.3 Voltage vector sequences of RSPWM methods

	A1	A2	A3	A4	A5	A6
RSPWM1	31513	31513	31513	31513	31513	31513
RSPWM2A	31513	13531	13531	15351	15351	31513
RSPWM2B	42624	42624	24642	24642	26462	26462
	B1	B2	B3	B4	B5	B6
RSPWM3	31513	42624	13531	24642	15351	26462

NSPWM [8] employs only three neighbor active voltage vectors and sequences them in the order that the minimum switching count is obtained. Thus, one of the phases is not switched in each PWM cycle. For example, for the region B2, the applied voltage vectors are V_1, V_2, and V_3 with the sequence V_3-V_2-V_1-V_2-V_3. Consequently, the pulse pattern of NSPWM in the region B2 becomes as shown in Figure 2.14. Note that phase “c” is not switched in this PWM cycle (and over B2 region). Comparing the pulse patterns of Figure 2.8 and Figure 2.14, it can be observed that NSPWM is a discontinuous PWM method and it yields equivalent advantages to DPWM1 in terms of switching loss reduction. The difference is that in DPWM1 one of the zero states is avoided, while in NSPWM both zero states are avoided and an active vector is introduced instead. The switching count reduction is obtained by proper sequencing the voltage vectors.

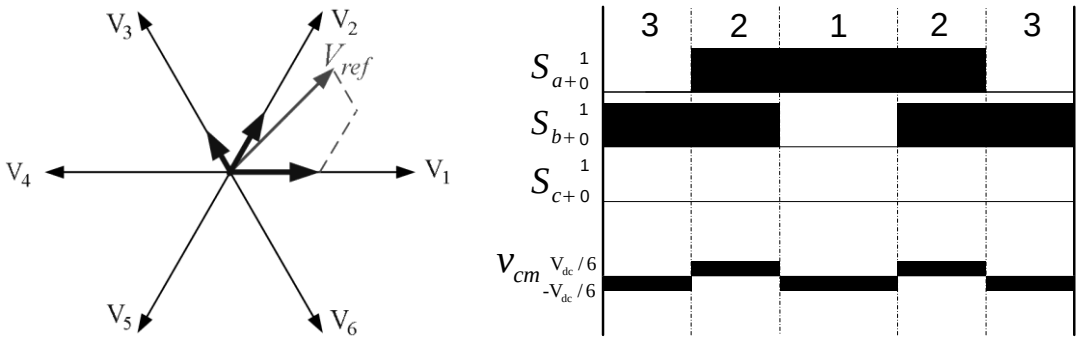


Figure 2.14 Voltage space vectors and pulse pattern of NSPWM for the region B2.

Table 2.4 Voltage vector sequences of NSPWM

	B1	B2	B3	B4	B5	B6
NSPWM	21612	32123	43234	54345	65456	16561

The RMCV-PWM methods differ significantly in terms of performance characteristics. Comparing the voltage linearity ranges, AZSPWM methods have the same voltage linearity characteristics as conventional SVPWM and DPWM1 methods ($0 \leq M_i \leq 0.907$). However, RSPWM methods and NSPWM have limited voltage utilization range. The linearity ranges of both RSPWM1 and RSPWM2 method are $0 \leq M_i \leq 0.52$. The linearity of RSPWM3 is valid for $0 \leq M_i \leq 0.604$. In contrast to RSPWM methods, NSPWM is linear at high M_i ($0.61 \leq M_i \leq 0.907$). It is apparent from this discussion that in terms of voltage linearity range, AZSPWM methods are more advantageous than RSPWM and NSPWM methods. Note that the voltage linearity ranges given in this section are per-fundamental-cycle linearity ranges. In Figure 2.15 the voltage linearity ranges of these PWM methods are illustrated. In the figure the light shaded regions define the per-carrier-cycle voltage linearity regions and the dark shaded regions define the per-fundamental-cycle linearity regions.

The RCMV-PWM methods have higher PWM ripple than conventional PWM methods [35]. AZSPWM methods have very high ripple at low M_i (since the zero states are replaced with active vectors with opposite direction to the reference voltage vector). Similar to AZSPWM methods, RSPWM methods have also high

ripple at low M_i since they utilize three voltage vectors that are 120° apart from each other (most remote vectors). NSPWM is the closest to the conventional methods in terms of PWM ripple. Its ripple is similar to DPWM1 in the high M_i range as the active vectors close to the reference voltage vector dominate. Detailed analytical output current ripple characteristics of the PWM methods have been investigated in [35].

In conclusion all the RCMV-PWM methods yield a low CMV magnitude of $V_{dc}/6$, theoretically. The frequency and polarity of CMV of each RCMV-PWM method is unique. In RSPWM1 and RSPWM2, not only the CMV magnitude is low, but it is also constant, implying no CMV variation, which is the most favorable feature. In RSPWM3, the CMV is constant every 60° in space. In AZSPWM2 and AZSPWM3, the CMV varies at the PWM frequency. In NSPWM and AZSPWM1 the CMV changes four and six times respectively, in one PWM period. However, in practice some pulse patterns are problematic.

Among the discussed PWM methods SVPWM, DPWM1, AZSPWM1, and NSPWM have one switching at a time, while all other methods involve simultaneous switching of two inverter legs. In practice, it is very difficult to switch two inverter legs simultaneously (due to inverter dead-time, gate signal delay differences, and/or unidentical IGBT/diode switching characteristics, etc.). Consequently, unexpected zero states which lead to high CMV may appear and the advantage of the methods disappears, as also illustrated in [7] and [55]. Even if simultaneous switching is realized, it is prohibited for the reason that simultaneous switching creates instantaneous line-to-line voltage reversal (between V_{dc} and $-V_{dc}$) which results in significant overvoltages at the motor terminals (particularly in long cable applications, where cable capacitance is large). As a result, it becomes obvious that except for AZSPWM1 and NSPWM, the RCMV-PWM methods are prohibitive. Although AZSPWM1 exhibits instantaneous line-to-line voltage polarity reversal at some operating conditions [8], this problem is solved with a minor patch to the PWM algorithm [44], [56]. Comparing AZSPWM2 and AZSPWM3, their CMV pulse patterns are similar. However, AZSPWM2 has ten

switchings per PWM cycle, while AZSPWM3 has six switchings per PWM cycle. Thus, switching losses in AZSPWM2 is higher. Therefore, AZSPWM2 is not considered practical and it is not included in this thesis. However, it can be shown that it can be included under the generalized scalar PWM umbrella.

After the pulse patterns and performance characteristics of the PWM methods are reviewed, the generalized scalar implementation approach for the implementation of these PWM methods will be described in the next section.

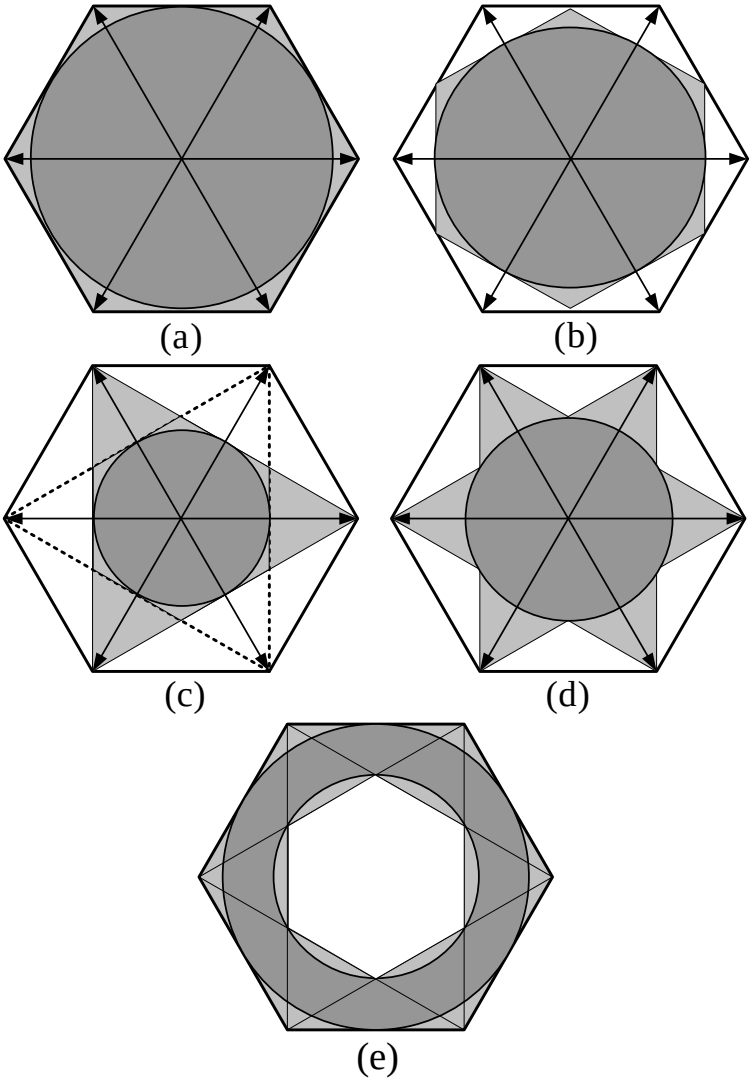


Figure 2.15 Voltage linearity regions of: (a) SVPWM, DPWM1, AZSPWM1-2-3, (b) SPWM, (c) RSPWM1-2, (d) RSPWM3 and (e) NSPWM.

2.4 Generalized Scalar PWM Approach

The generalized scalar PWM approach provides degrees of freedom in the choice of both the zero-sequence signal and the carrier waves [41]. First, the zero-sequence signals can be arbitrarily generated, but generating them based on the phase reference voltages (original modulation signals) provides significant advantages. Until present, most useful conventional PWM pulse patterns could be obtained by this approach [3], [37]. Therefore, in most cases, the zero-sequence signals are obtained by evaluating the reference voltages. Secondly, the carrier waves of different phases can be selected arbitrarily. However, recent studies have illustrated that employing triangular carrier waves at the same frequency, and selecting the phase relation between the carrier waves of different phases based on the voltage references yields favorable results [8], [42], [43]. As a result, the generalized scalar PWM approach will favor such constraints for the purpose of keeping the scope of the thesis within practical boundaries. Given the described set of constraints, the generalized block diagram of scalar PWM approach with zero-sequence signal injection principle is illustrated in Figure 2.16.

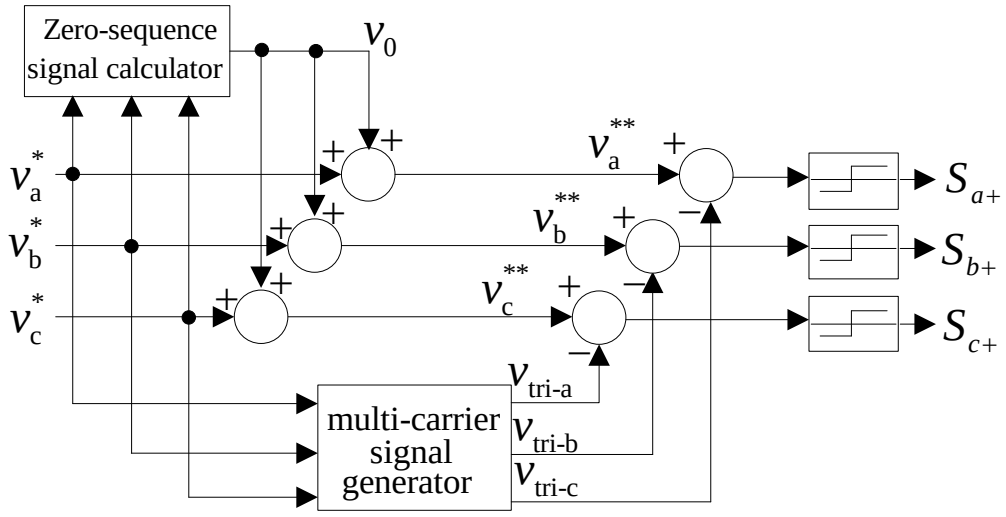


Figure 2.16 The block diagram of the generalized carrier-based scalar PWM employing the zero-sequence signal injection principle and multi-carrier signals.

In the generalized scalar approach; according to the original three-phase sinusoidal reference signals (voltage references with single star subscripts) and zero-sequence signals, the final reference (modulation) signals (voltage references with double star subscripts) are generated. Then, the individual modulation and carrier waves are compared to determine the associated inverter leg switch states and output voltages. In the conventional approach (Figure 2.17), which is the special case of generalized approach, only one triangular carrier wave is utilized for all phases. In the scalar representation the modulation waves are defined as (2.6), (2.7) and (2.8),

$$v_a^{**} = v_a^{*} + v_0 = V_{1m}^{*}\cos(\omega_e t) + v_0 \tag{2.6}$$

$$v_b^{**} = v_b^{*} + v_0 = V_{1m}^{*}\cos(\omega_e t - \frac{2\pi}{3}) + v_0 \tag{2.7}$$

$$v_c^{**} = v_c^{*} + v_0 = V_{1m}^{*}\cos(\omega_e t + \frac{2\pi}{3}) + v_0 \tag{2.8}$$

where, v^{*}_{a}, v^{*}_{b} and v^{*}_{c} are the original sinusoidal reference signals and v_0 is the zero-sequence signal. Using the zero-sequence signal injected modulation waves, the duty cycle of each switch can be easily calculated in the following for both single and multi-carrier methods;

$$d_{x+} = \frac{1}{2}\left(1 + \frac{v_x^{**}}{V_{dc}/2}\right), \ \ for\ x \in \{a,b,c\} \tag{2.9}$$

$$d_{x-} = 1 - d_{x+}, \quad for\ x \in \{a,b,c\}. \tag{2.10}$$

Modulation waveforms can be divided into two groups. In the Continuous PWM (CPWM) methods, the modulation waves are always between the carrier wave peak values. In every PWM cycle, the modulation wave always intersects with the carrier wave, and thus switchings occur.

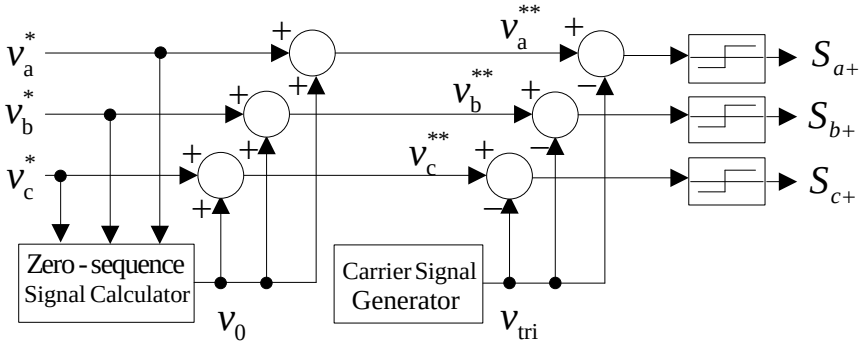


Figure 2.17 The block diagram of the conventional scalar PWM method employing zero-sequence signal injection and a common triangular carrier wave.

In the Discontinuous PWM (DPWM) methods, the modulation wave of a phase is always clamped to the positive and/or negative DC bus for at most a total of 120° over a fundamental period. Thus, in such intervals the corresponding inverter leg is not switched. According to this definition, SPWM, SVPWM, AZSPWM, and RSPWM methods are CPWM methods, DPWM1 and NSPWM are DPWM methods.

As discussed in the previous section the simplest CPWM method is SPWM, where no zero-sequence signal is injected (Figure 2.18). Using one common triangular carrier wave for all phases, SPWM is implemented. Note that SPWM with multi-carrier signals, which has been studied in [42] and found to have quite limited performance, is not discussed in this thesis.

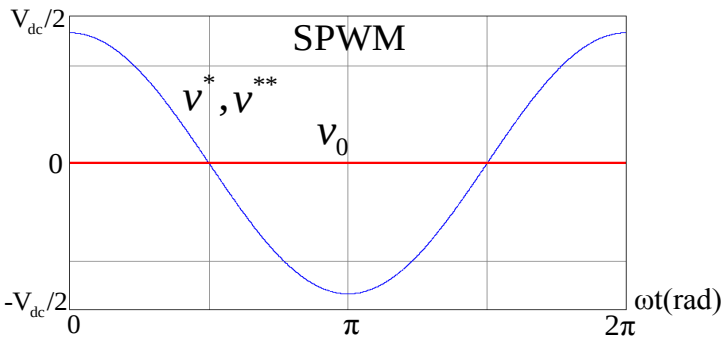


Figure 2.18 Modulation waveform and zero-sequence signal of SPWM (M_i = 0.7).

SVPWM and AZSPWM methods use the same zero-sequence signal shown in Figure 2.19. “It is generated by employing the minimum magnitude test which compares the magnitudes of the three-phase original reference signals and selects the signal which has minimum magnitude [3]”. Multiplying this signal by 0.5, the zero-sequence signal of these methods is found. For example, if $|v_a^*| \leq |v_b^*|, |v_c^*|$, then $v_0 = 0.5 \cdot v_a^*$. This modulation wave is recognized as SVPWM modulation wave in the literature [3]. Using it along with a common triangular carrier wave for all phases, SVPWM method yields. Using the same modulation wave, but varying the triangle polarities (resulting in multi-carrier waves, $v_{tri\text{-}a}$, $v_{tri\text{-}b}$, $v_{tri\text{-}c}$) AZSPWM methods yield. Region dependent multi-carrier signals of AZSPWM methods are given in Table 2.5.

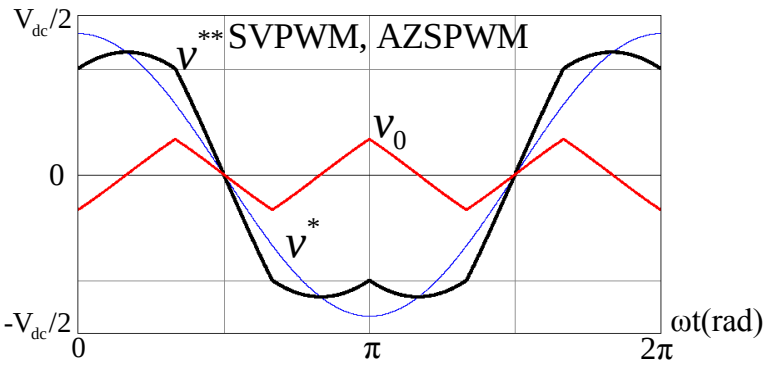


Figure 2.19 Modulation waveform (black) and zero-sequence signal (red) of SVPWM and AZSPWM methods ($M_i = 0.7$).

Table 2.5 AZSPWM1 and AZSPWM3 space vector region dependent multi-carrier signals

AZSPWM1						
Carrier	**A1**	**A2**	**A3**	**A4**	**A5**	**A6**
$v_{tri\text{-}a}$	$-v_{tri}$	$-v_{tri}$	$-v_{tri}$	v_{tri}	v_{tri}	v_{tri}
$v_{tri\text{-}b}$	v_{tri}	v_{tri}	$-v_{tri}$	$-v_{tri}$	$-v_{tri}$	v_{tri}
$v_{tri\text{-}c}$	$-v_{tri}$	v_{tri}	v_{tri}	v_{tri}	$-v_{tri}$	$-v_{tri}$
AZSPWM3						
	A1	**A2**	**A3**	**A4**	**A5**	**A6**
$v_{tri\text{-}a}$	v_{tri}	v_{tri}	$-v_{tri}$	$-v_{tri}$	$-v_{tri}$	v_{tri}
$v_{tri\text{-}b}$	$-v_{tri}$	v_{tri}	v_{tri}	v_{tri}	$-v_{tri}$	$-v_{tri}$
$v_{tri\text{-}c}$	$-v_{tri}$	$-v_{tri}$	$-v_{tri}$	v_{tri}	v_{tri}	v_{tri}

In DPWM methods, DPWM1 and NSPWM, the phase signal which is the largest in magnitude is clamped to the positive and negative DC bus with the same polarity for 60° (a total of 120°) over a fundamental cycle [3] (Figure 2.20). For example, if $|v_a^*| \geq |v_b^*|, |v_c^*|$, then $v_0 = (\text{sign}(v_a^*)) \cdot (V_{dc}/2) - v_a^*$. Using the discussed DPWM modulation wave along with a common triangular carrier wave for all phases, DPWM1 yields. Using the same modulation waves, with the multi-carrier waves given in Table 2.6, NSPWM is obtained.

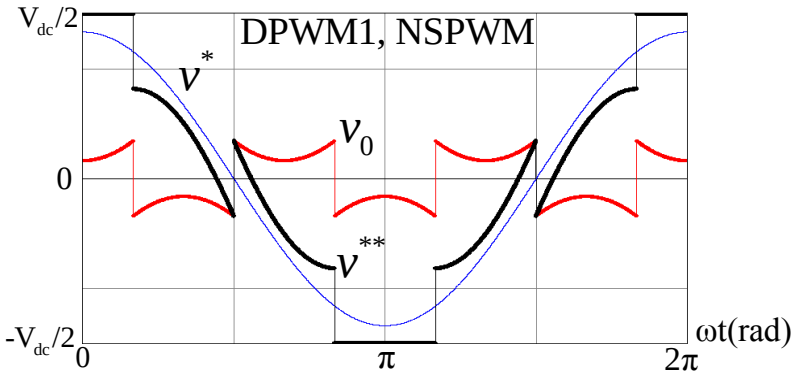


Figure 2.20 Modulation waveform (black) and zero-sequence signal (red) of DPWM1 and NSPWM ($M_i = 0.7$).

Table 2.6 NSPWM space vector region dependent multi-carrier signals

NSPWM						
	B1	**B2**	**B3**	**B4**	**B5**	**B6**
$v_{\textbf{tri-a}}$	v_{tri}	$-v_{tri}$	$-v_{tri}$	v_{tri}	v_{tri}	v_{tri}
$v_{\textbf{tri-b}}$	v_{tri}	v_{tri}	v_{tri}	$-v_{tri}$	$-v_{tri}$	v_{tri}
$v_{\textbf{tri-c}}$	$-v_{tri}$	v_{tri}	v_{tri}	v_{tri}	v_{tri}	$-v_{tri}$

As discussed in the previous section, in RSPWM1 and RSPWM2, the CMV does not vary and its magnitude is constant at $V_{dc}/6$, and in RSPWM3, the CMV is constant every 60° in space. This condition indicates that the zero-sequence signal (thus low frequency CMV) is equal to the instantaneous CMV value. Therefore, the zero-sequence signals of the RSPWM methods are obtained by adding $V_{dc}/6$ and/or

$-V_{dc}/6$ to the sinusoidal reference signals as given in Table. 2.7. The zero-sequence signal and modulation waveform of RSPWM3 is shown in Figure 2.21. In RSPWM methods, the switching patterns of two phases are similar to the PWM methods discussed previously, and they can be implemented by comparing the modulation wave with v_{tri} or $-v_{tri}$. However, the switching frequency of one phase is always twice the other two phases. For example, as seen in Figure 2.12, the switching frequency of phase "a" is twice the others, and a different approach is used to obtain the pulse pattern of this phase. After the switch logic signal of two phases are obtained, the double frequency switch signal is obtained by applying NOR and/or NAND logic operations to the other two switch logic signals. The alternating triangular carrier waves are given in Table 2.8. Note that the marks "-" in Table 2.8 correspond to the double switching frequency signals which are obtained by applying the logic operations given in Table 2.9, and the marks "-" in Table 2.9 correspond to phase switch signals which are obtained according to Table 2.8.

In conclusion, the double switching frequency signals of RSPWM methods are logic functions of the other two phases. However, as will be explained in section 2.6, in the implementation of all PWM signals (including double switching frequency signals of RSPWM methods), a counter is compared with comparator registers which include duty cycle information, and no other mathematical functions are used.

Table 2.7 Zero-sequence signals of RSPWM methods

	Zero-sequence signal
RSPWM1	$v_0 = -V_{dc}/6$
RSPWM2A	$v_0 = -V_{dc}/6$
RSPWM2B	$v_0 = V_{dc}/6$
RSPWM3	$v_0 = -V_{dc}/6$ for B1, B3, B5 regions $v_0 = V_{dc}/6$ for B2, B4, B6 regions

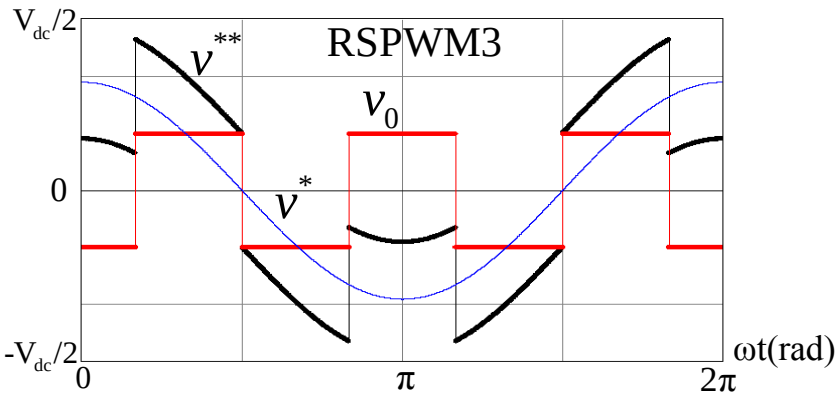


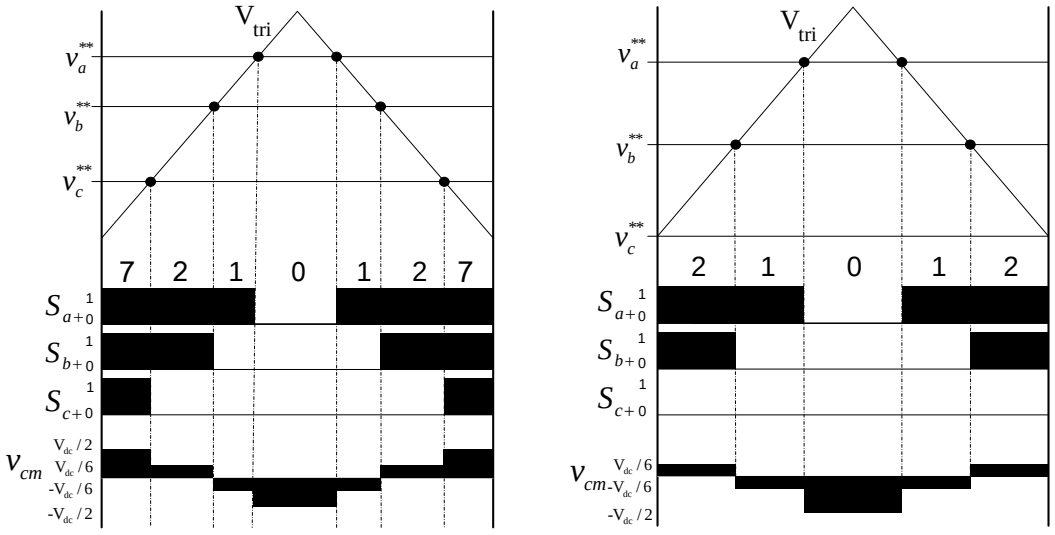
Figure 2.21 Modulation waveform (black) and zero-sequence signal (red) of RSPWM3 (M_i = 0.5).

Table 2.8 RSPWM methods space vector region dependent multi-carrier signals

RSPWM1						
Carrier	A1	A2	A3	A4	A5	A6
v_{tri-a}	-	-	-	-	-	-
v_{tri-b}	v_{tri}	v_{tri}	v_{tri}	v_{tri}	v_{tri}	v_{tri}
v_{tri-c}	$-v_{tri}$	$-v_{tri}$	$-v_{tri}$	$-v_{tri}$	$-v_{tri}$	$-v_{tri}$
RSPWM2A						
	A1	A2	A3	A4	A5	A6
v_{tri-a}	-	v_{tri}	v_{tri}	v_{tri}	v_{tri}	-
v_{tri-b}	v_{tri}	-	-	$-v_{tri}$	$-v_{tri}$	v_{tri}
v_{tri-c}	$-v_{tri}$	$-v_{tri}$	$-v_{tri}$	-	-	$-v_{tri}$
RSPWM2B						
	A1	A2	A3	A4	A5	A6
v_{tri-a}	$-v_{tri}$	$-v_{tri}$	-	-	v_{tri}	v_{tri}
v_{tri-b}	v_{tri}	v_{tri}	v_{tri}	v_{tri}	-	-
v_{tri-c}	-	-	$-v_{tri}$	$-v_{tri}$	$-v_{tri}$	$-v_{tri}$
RSPWM3						
	B1	B2	B3	B4	B5	B6
v_{tri-a}	-	$-v_{tri}$	v_{tri}	-	v_{tri}	v_{tri}
v_{tri-b}	v_{tri}	v_{tri}	-	v_{tri}	$-v_{tri}$	-
v_{tri-c}	$-v_{tri}$	-	$-v_{tri}$	$-v_{tri}$	-	$-v_{tri}$

Table 2.9 RSPWM logic operations for the double switching frequency phases

RSPWM1						
Switch signals	A1	A2	A3	A4	A5	A6
S_{a+}	$(S_{b+}+S_{c+})'$					
RSPWM2A						
	A1	A2	A3	A4	A5	A6
S_{a+}	$(S_{b+}+S_{c+})'$	-	-	-	-	$(S_{b+}+S_{c+})'$
S_{b+}	-	$(S_{a+}+S_{c+})'$	$(S_{a+}+S_{c+})'$	-	-	-
S_{c+}	-	-	-	$(S_{a+}+S_{b+})'$	$(S_{a+}+S_{b+})'$	-
RSPWM2B						
	A1	A2	A3	A4	A5	A6
S_{a+}	-	-	$(S_{b+}\cdot S_{c+})'$	$(S_{b+}\cdot S_{c+})'$	-	-
S_{b+}	-	-	-	-	$(S_{a+}\cdot S_{c+})'$	$(S_{a+}\cdot S_{c+})'$
S_{c+}	$(S_{a+}\cdot S_{b+})'$	$(S_{a+}\cdot S_{b+})'$	-	-	-	-
RSPWM3						
	B1	B2	B3	B4	B5	B6
S_{a+}	$(S_{b+}+S_{c+})'$	-	-	$(S_{b+}\cdot S_{c+})'$	-	-
S_{b+}	-	-	$(S_{a+}+S_{c+})'$	-	-	$(S_{a+}\cdot S_{c+})'$
S_{c+}	-	$(S_{a+}\cdot S_{b+})'$	-	-	$(S_{a+}+S_{b+})'$	-



(a) (b)

Figure 2.22 Pulse patterns of (a) SVPWM and (b) DPWM1 obtained using common triangular carrier wave.

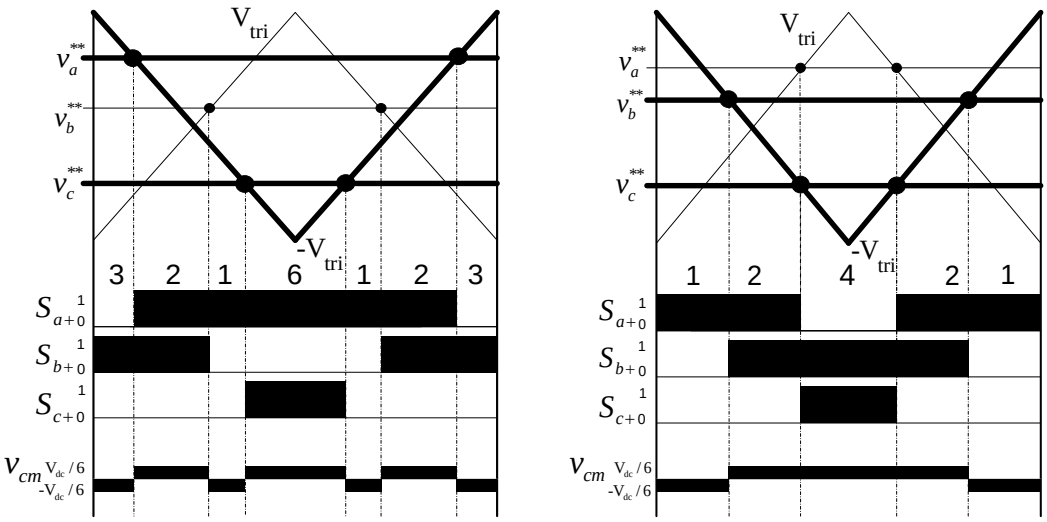


Figure 2.23 Pulse patterns of (a) AZSPWM1 and (b) AZSPWM3 obtained using multi-carrier waves.

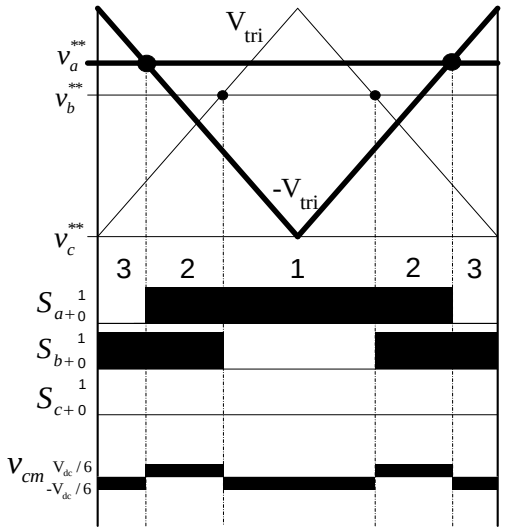


Figure 2.24 Pulse pattern of NSPWM obtained using multi-carrier waves.

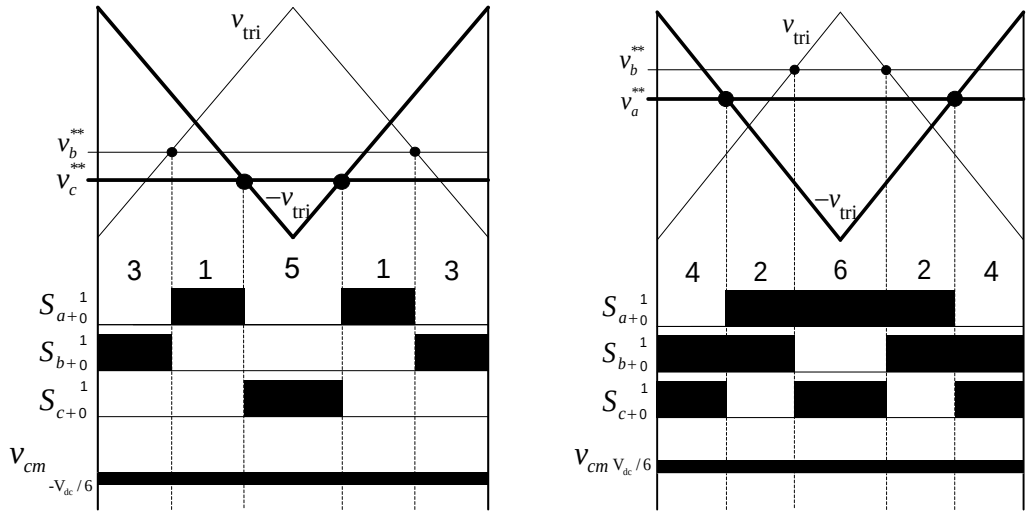


Figure 2.25 Pulse patterns of RSPWM methods obtained using multi-carrier waves.

As a result, using the modulation waves and polarity controlled triangular carrier waves, all the PWM methods could be covered. The pulse patterns of the PWM methods obtained using multi-carrier waves are illustrated in Figures 2.22-2.25. Note that all the popular PWM methods reported in [3] which have different modulation waves than the above discussed methods use common triangle and fall under the same umbrella and can be treated with the generalized scalar PWM approach. Thus the proposed approach is broad and covers most methods reported in the literature. Considering that the methods reported in this section (both conventional and the recently developed RCMV-PWM methods) and the other conventional methods reviewed in [3] are the most important methods (due to their superior performance when compared to other methods), the approach yields sufficient results from the practical utilization perspective. Using the proposed approach and creating a variety of triangular carrier wave patterns and modulation wave shapes, further PWM pulse patterns, and thus new methods can be invented.

In the alternating polarity triangular carrier wave methods, the alternating triangle polarities can be obtained by determining the regions of Figure 2.6. This goal can be easily achieved by comparing the modulation waves. For example, the $|v_b^*| \leq |v_a^*|$, $|v_c^*|$ condition corresponds to A1 region, and the $v_a^* \geq v_b^*$, v_c^* condition corresponds

to B1 region. Such operations can be very easily performed with the PWM units of the modern digital signal processors used in AC motor drives and PWM rectifiers.

It should be noted that in all PWM methods, the injected zero-sequence signal is a low frequency signal (periodic at $3\omega_e$ and/or its multiples, lower than the carrier frequency by at least an order of magnitude) which causes low frequency CMV. At such frequencies the parasitic circuit components (capacitances) are negligible (open-circuit) and therefore the zero-sequence voltage has no detrimental effect on the drive and yields no common mode current (CMC), unless low common mode impedance path is provided by filter configurations included in the drive for the purpose of noise reduction [20], [21]. High frequency CMV, on the other hand, can be harmful and will be discussed in the following chapters. In the next section implementation details of the PWM methods will be provided.

2.5 Implementation

This section discusses the practical implementation of the PWM methods of section 2.3. The modulation waves of the discussed methods are generated according to the simple magnitude rule approach discussed in Section 2.3. Only several comparisons among the three sinusoidal references (original modulation waves) and several algebraic operations are necessary to obtain the zero-sequence signal, as shown in section 2.4 via examples. Having obtained the zero-sequence signal, it is added to the original modulation waves and the final modulation signals result. From these signals, the duty cycles are calculated according to (2.9) and (2.10). The duty cycles are checked and bounded to the range of 0 to 1 (in case overmodulation condition occurs). For SVPWM and DPWM1, a common triangular carrier wave and for the other methods alternating polarity triangular carrier waves given in previous section are generated. Determining the triangle polarity also involves only a comparison of the sinusoidal references. These operations can be lumped together with the zero-sequence signal determination stage to further minimize the computational burden. This task is left to the implementation engineer as a straightforward procedure. Once the final modulation signals and triangles are obtained, the remaining task

involves the sine-triangle comparison stage. This comparison is performed to determine the switching instants via a comparator for each phase.

The scalar PWM implementation of all the discussed methods is an easy task compared to the space vector implementation (discussed at the end of Section 2.2). The implementation can be best realized on digital PWM units such as the modern motion control or power management microcontrollers and DSP chips (which involve a well developed software programmable digital PWM unit) or dedicated FPGA units. Most modern commercial drives and power converters utilize such control chips which are offered at economical price. Thus, the approach can be readily employed in most power converter control platforms. Employing such digital platforms, and considering the simplicity of the scalar PWM algorithms, it is easy to implement (and combine) two or more PWM methods as one modulator algorithm and select the favorable PWM method in each operating region in order to obtain the highest performance [3]. Combination of SVPWM at low M_i and DPWM1 at high M_i is common in industrial drives. Combination of AZSPWM1 at low M_i and NSPWM at high M_i is an alternative approach for low CMV requiring applications [44].

While operating at high M_i (such as full speed operation of a drive or PWM rectifier operating under the normal operating range), overmodulation condition may occur due to dynamics or other line or load variation conditions. In such cases, the treatment of overmodulation can be included in the algorithm as a gain correction step as reported in [39], [40]. Since the gain functions of the discussed modulation waves are provided in [40] the compensation is an easy task.

2.6 Experimental Results

In the laboratory, the discussed PWM methods are implemented using the Texas Instruments TMS320F2808 fixed-point DSP chip. In this chip, the PWM signals are generated by the enhanced PWM (EPWM) module of the DSP [45] which is a hardware digital circuit dedicated for the purpose of generating the PWM signals.

The PWM period (thus the carrier frequency), the deadtime, etc. are all parameters that are controlled by the user via software. The EPWM module includes an internal counter clock (termed as “PERIOD”) which corresponds to the triangular carrier wave. The value of this counter defines the half of the PWM period. One carrier cycle is completed as the counter counts up from “0” to “PERIOD” and then decrements down to “0” again.

For every PWM cycle, the per-phase duty cycles are calculated first. Then, the duty cycles are converted to the count number as they are scaled with the PERIOD. Since the EPWM module has two comparator registers (COMPA and COMPB) per-phase, the count number, its complementary, zero (0), or PERIOD value are loaded to these counters depending on the pulse pattern to be generated. In this application, the switching rule is defined as the PWM signal of the upper switch of an inverter phase (for instance, S_{a+}) is at logic level “1” when the counter value is between the loaded values of COMPA and COMPB comparator registers (Figure 2.26), and at logic “0” otherwise (S_{a-} logic is complementary of S_{a+}).

The conventional PWM pulse patterns (Figure 2.22) are generated such that the PWM cycle starts and ends with the upper switches in the high “1” state, (often termed as “active high” [43]) except for the PWM periods where the switching ceases in DPWM methods. Generating this pulse pattern, which is shown in Figure 2.26.a, involves loading register COMPB with the zero “0” value, and register COMPA with the S_{a+} duty cycle d_{a+}·PERIOD. Methods involving PWM periods with active low (corresponding to the $-v_{tri}$ case), corresponding to the pulse pattern of Figure 2.26.b, require loading the register COMPA with the value PERIOD and the register COMPB with its complementary $(1-d_{a+})$·PERIOD.

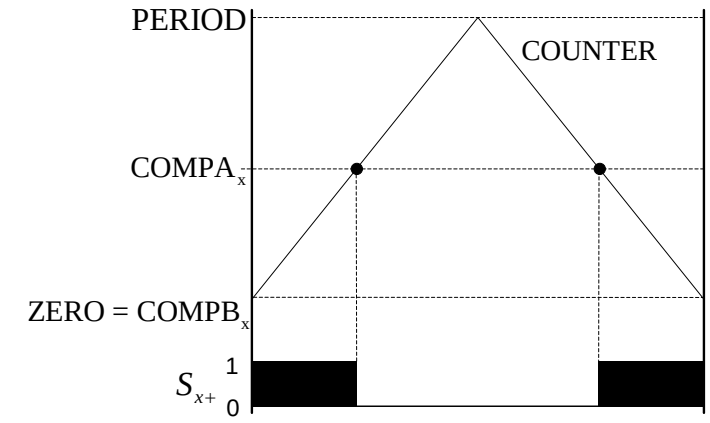
In methods involving PWM periods with both active high and active low (such as RSPWM methods), corresponding to the pulse pattern of Figure 2.26.c, the registers are loaded according to duty cycles of other phases. For example, for B1 region of RSPWM3, the register values are given in Table 2.10. Active low switching instant of phase a in this region is determined by active high switching instant of phase b,

thus $COMPB_a$ is loaded with $(1-d_b)\cdot PERIOD$. Similarly, active high switching instant of phase a is determined by active low switching instant of phase c, thus $COMPA_a$ is loaded with $(1-d_c)\cdot PERIOD$. In conclusion, conventional methods use only the pulse pattern of Figure 2.26.a, while RCMV-PWM methods use all the three.

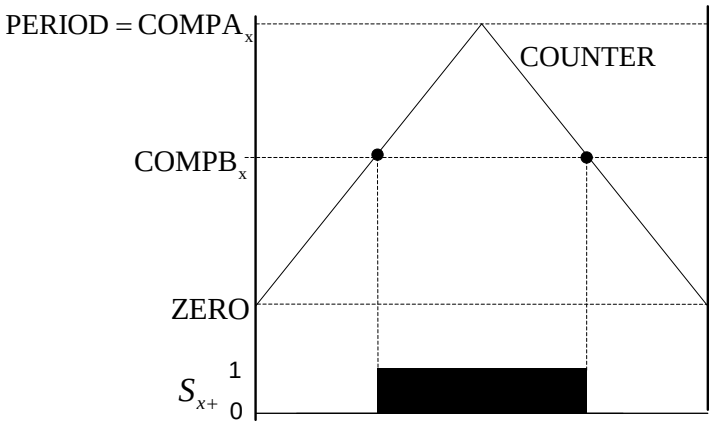
The PWM pulse pattern generation procedure is summarized in the flowchart of Figure 2.27 for AZSPWM1. Note that the zero-sequence signal generation and the alternating triangle determination (region R determination) stages are gathered for reduced computations. While the flowchart is generated for AZSPWM1, the approach is the same and straightforward for all other discussed methods.

Table 2.10 The comparator register values for RSPWM3 in the region B1

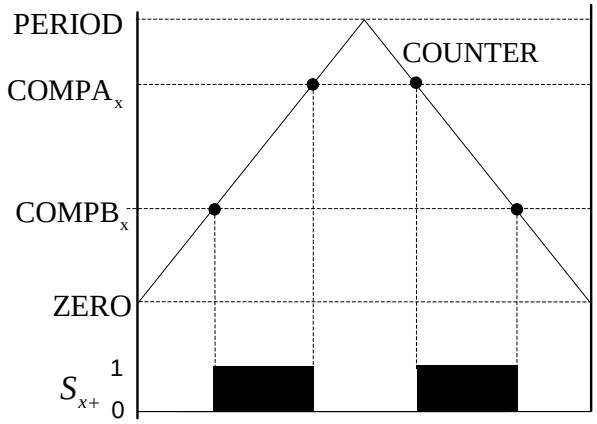
$COMPA_a$	$(1-d_c)\cdot PERIOD$
$COMPB_a$	$(1-d_b)\cdot PERIOD$
$COMPA_b$	$d_b\cdot PERIOD$
$COMPB_b$	0
$COMPA_c$	PERIOD
$COMPB_c$	$(1- d_c)\cdot PERIOD$



(a)



(b)



(c)

Figure 2.26 The PWM pulse pattern generation mechanism of the EPWM unit of the TMS320F2808 for (a) active high (v_{tri}), (b) active low ($-v_{tri}$), (c) both active high and active low.

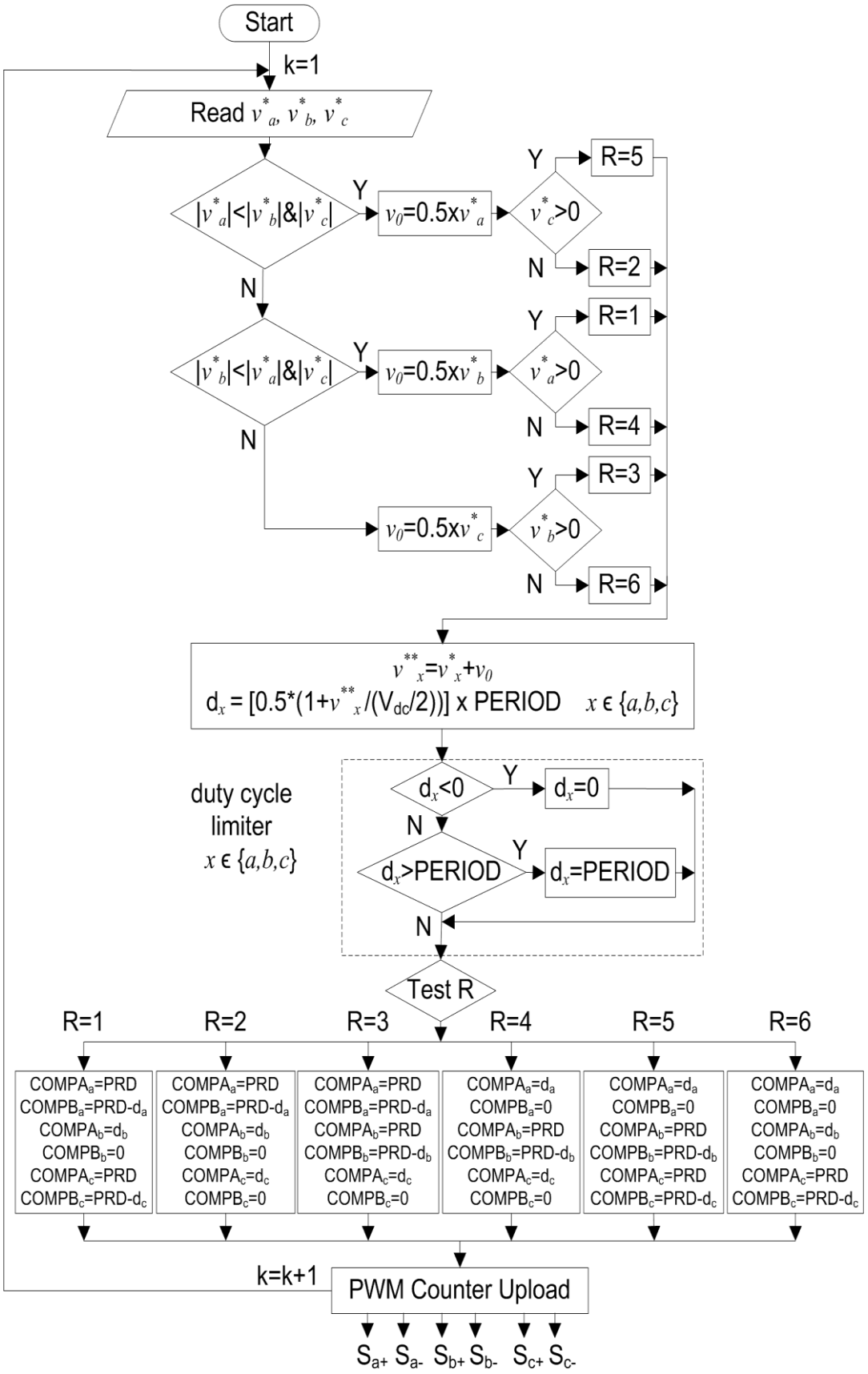


Figure 2.27 The PWM pulse pattern generation flowchart for AZSPWM1.

Employing the scalar implementation approach and utilizing the TMS320F2808 DSP platform, PWM signals are programmed and applied to a three-phase VSI with DC bus voltage of 500V. Inverter upper switch (S_{a+}, S_{b+}, S_{c+}) logic signals and the inverter output CMV (v_{cm}) waveforms for the implemented PWM periods are shown in Figures 2.28-2.33 (compare with Figures 2.22-2.25). This demonstrates that all the intended pulse patterns can be easily generated. Note that SVPWM and DPWM1 utilize zero vectors (000) and (111) which cause a CMV of $-V_{dc}/2$ (–250V) and $V_{dc}/2$ (250V), respectively. Among the RCMV-PWM methods, which utilize only active vectors, AZSPWM1 and NSPWM practically limit the CMV to $\pm V_{dc}/6$ (83V). However in AZSPWM3 and RSPWM3, during simultaneous switchings, unexpected zero states occur and higher CMV values ($\pm V_{dc}/2$) appear. Figures 2.34-2.39 show inverter output voltages (v_{ao}, v_{bo}, v_{co}) and the line-to-line voltages (v_{ab}) of the PWM methods. While in SVPWM and DPWM1 the line-to-line voltages are unipolar, in RCMV-PWM methods they are bipolar [35] as discussed in section 2.3. Bipolar voltage pulses result in higher output current ripple compared to unipolar voltage pulses, and they may cause overvoltages at the motor terminals in long-cable applications [8]. However, curements for overvoltage problem has been provided in [43], [44] as a part of the PWM algorithm. Note that in NSPWM and AZSPWM1, since there is zero-voltage time interval between line-to-line voltage polarity reversals, motor terminal overvoltage is at acceptable levels in NSPWM and with minor patches applied AZSPWM1 [44]. However, in AZSPWM3 and RSPWM3, line-to-line voltage rapidly changes between $\pm V_{dc}$, and extremely high overshoots occur. Thus, AZSPWM3 and RSPWM3 are not practical in the applications involving long cables. In chapter 4 and 5, applying these PWM methods to a motor drive, their performances will be investigated in detail.

These waveforms demonstrate that the various PWM methods can be easily implemented with the generalized scalar PWM approach. As a result, the inverter design engineers can choose among the offered various PWM methods based on the performance requirement of the application and easily implement one of the methods or a combination of various methods. Thus, the PWM method implementation procedure becomes an easy task.

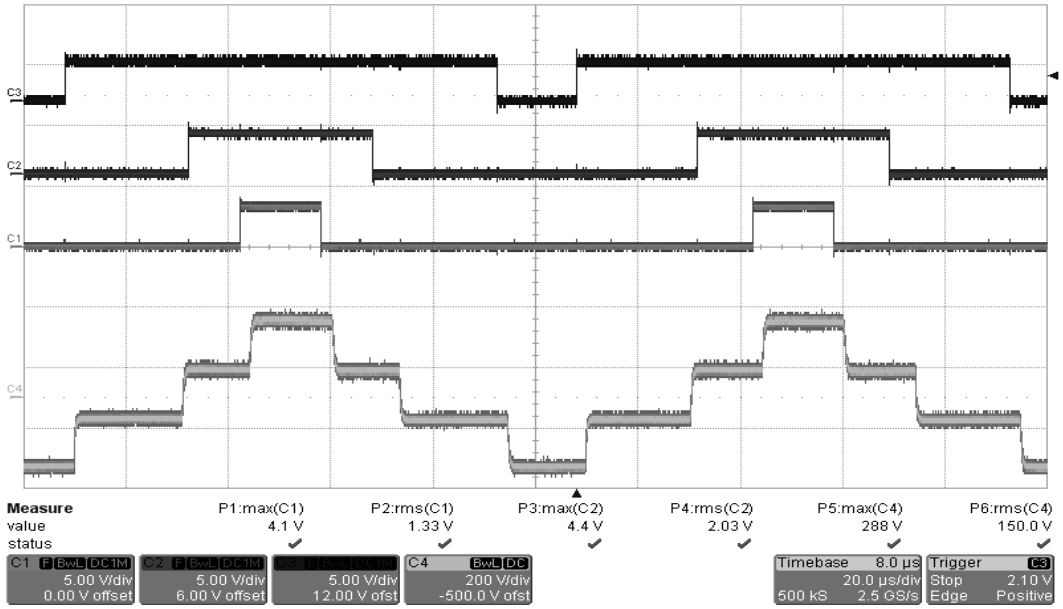


Figure 2.28 Experimental inverter upper switch (S_{a+}, S_{b+}, S_{c+}) logic signals (top three, 5V/div) and the inverter output CMV (v_{cm}) (bottom, 200V/div) waveforms for SVPWM (time scale: 20µs/div).

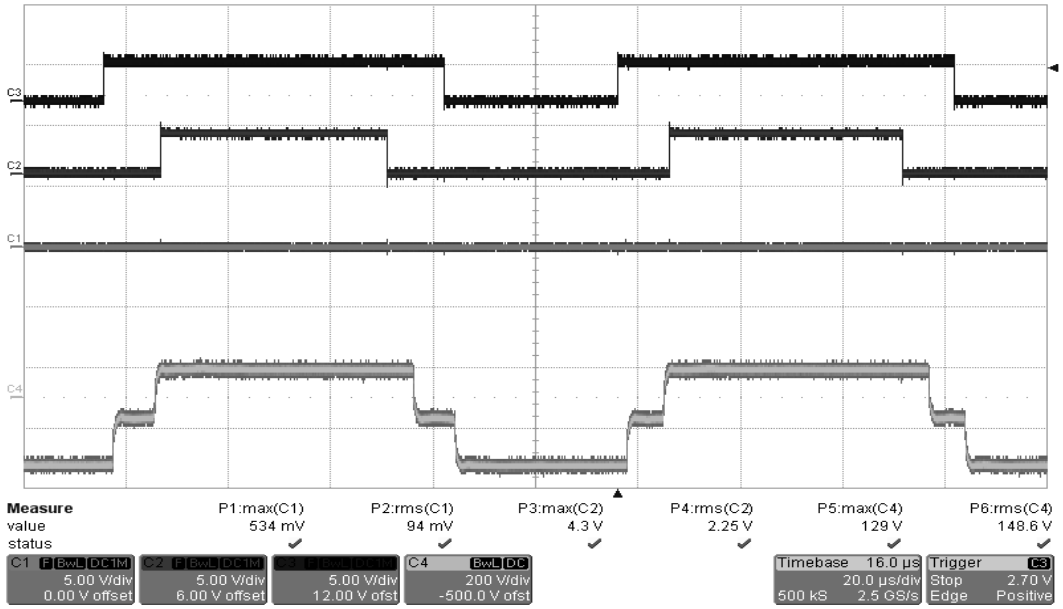


Figure 2.29 Experimental inverter upper switch (S_{a+}, S_{b+}, S_{c+}) logic signals (top three, 5V/div) and the inverter output CMV (v_{cm}) (bottom, 200V/div) waveforms for DPWM1 (time scale: 20µs/div).

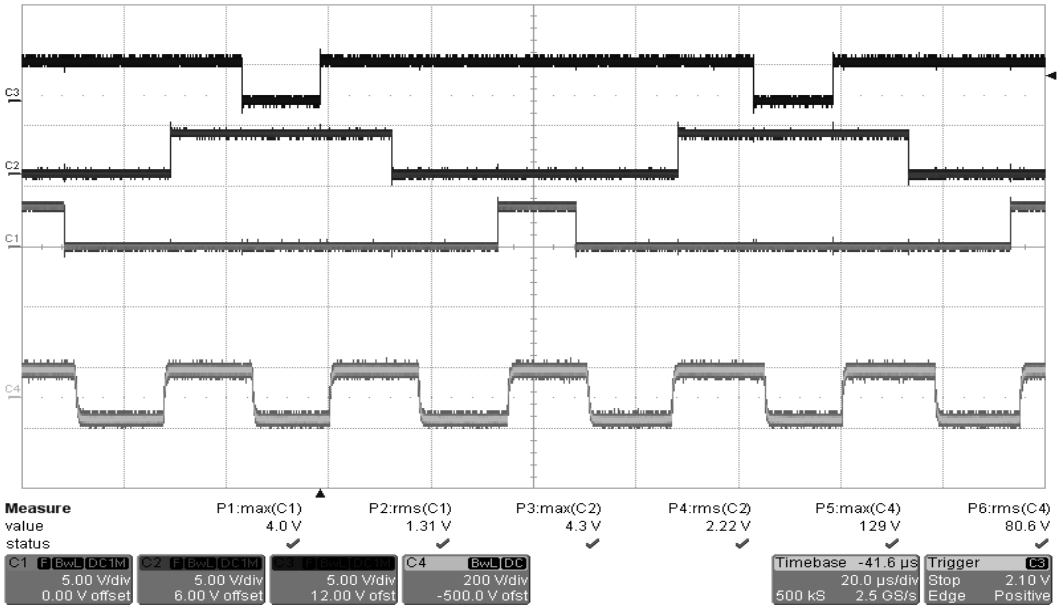


Figure 2.30 Experimental inverter upper switch (S_{a+}, S_{b+}, S_{c+}) logic signals (top three, 5V/div) and the inverter output CMV (v_{cm}) (bottom, 200V/div) waveforms for AZSPWM1 (time scale: 20µs/div).

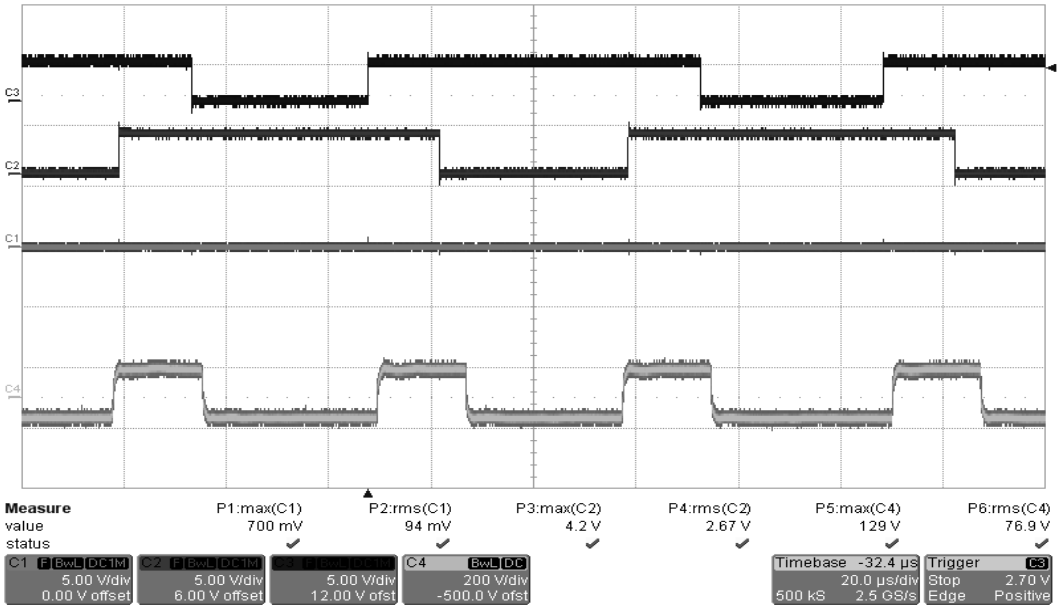


Figure 2.31 Experimental inverter upper switch (S_{a+}, S_{b+}, S_{c+}) logic signals (top three, 5V/div) and the inverter output CMV (v_{cm}) (bottom, 200V/div) waveforms for NSPWM (time scale: 20µs/div).

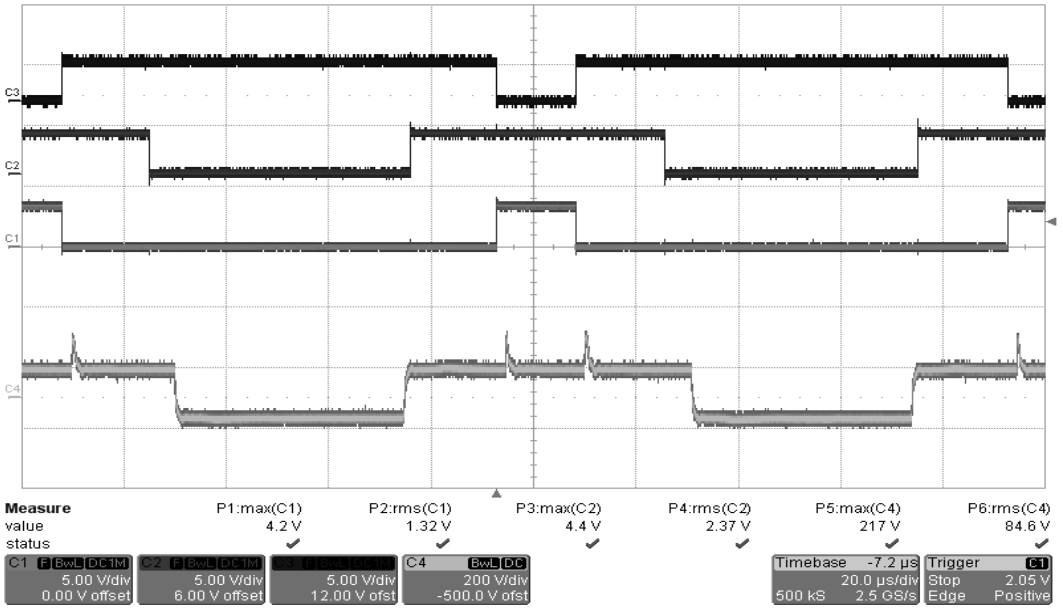


Figure 2.32 Experimental inverter upper switch (S_{a+}, S_{b+}, S_{c+}) logic signals (top three, 5V/div) and the inverter output CMV (v_{cm}) (bottom, 200V/div) waveforms for AZSPWM3 (time scale: 20µs/div).

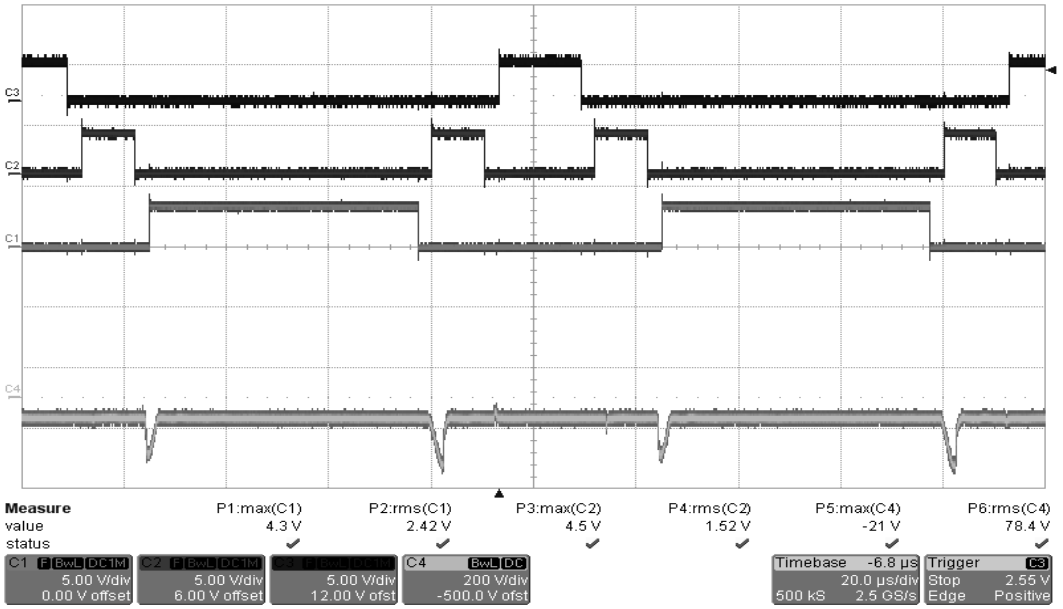


Figure 2.33 Experimental inverter upper switch (S_{a+}, S_{b+}, S_{c+}) logic signals (top three, 5V/div) and the inverter output CMV (v_{cm}) (bottom, 200V/div) waveforms for RSPWM3 (time scale: 20µs/div).

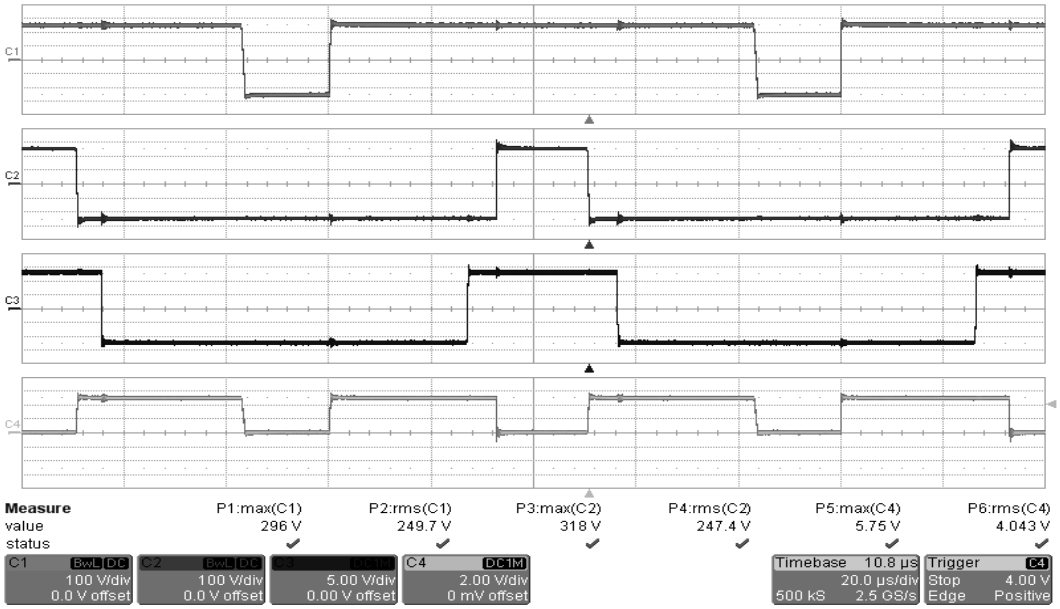


Figure 2.34 Experimental inverter output voltages (v_{ao}, v_{bo}, v_{co}) (top three, 100V/div) and the line-to-line voltage (v_{ab}) (bottom, 200V/div) waveforms for SVPWM (time scale: 20µs/div).

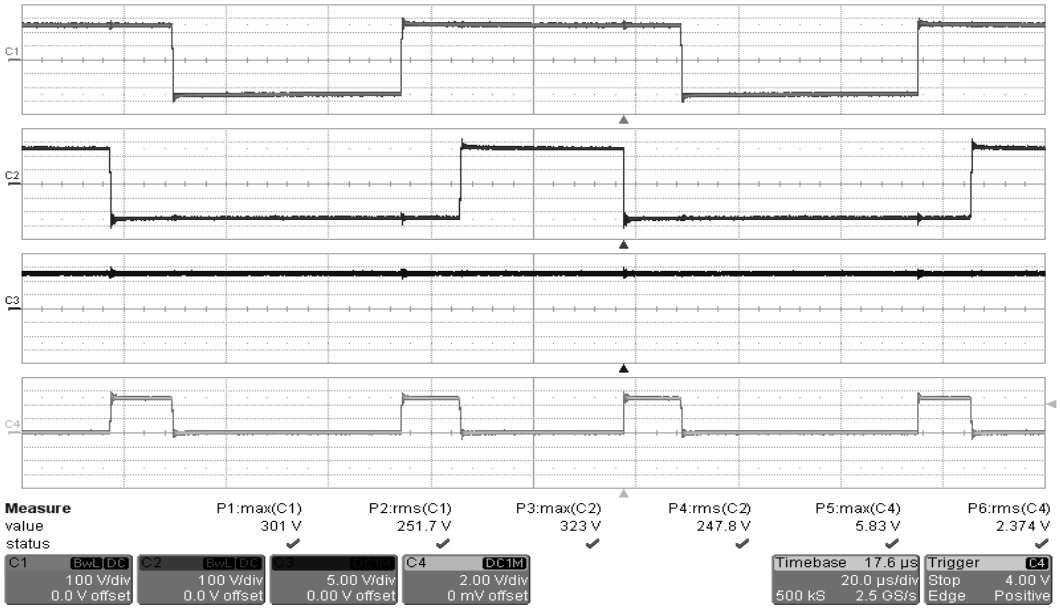


Figure 2.35 Experimental inverter output voltages (v_{ao}, v_{bo}, v_{co}) (top three, 100V/div) and the line-to-line voltage (v_{ab}) (bottom, 200V/div) waveforms for DPWM1 (time scale: 20µs/div).

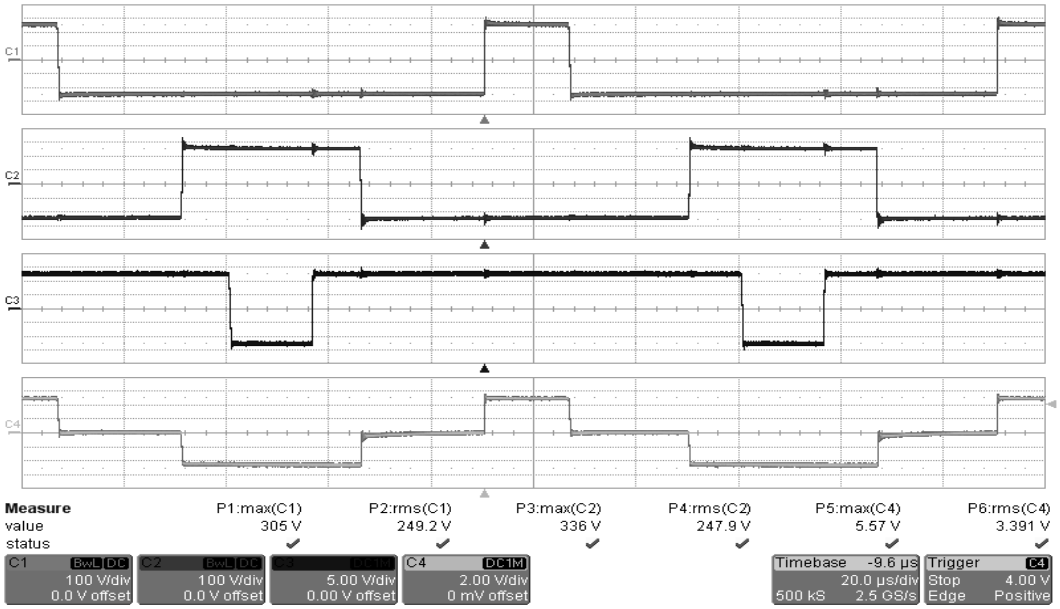


Figure 2.36 Experimental inverter output voltages (v_{ao}, v_{bo}, v_{co}) (top three, 100V/div) and the line-to-line voltage (v_{ab}) (bottom, 200V/div) waveforms for AZSPWM1 (time scale: 20µs/div).

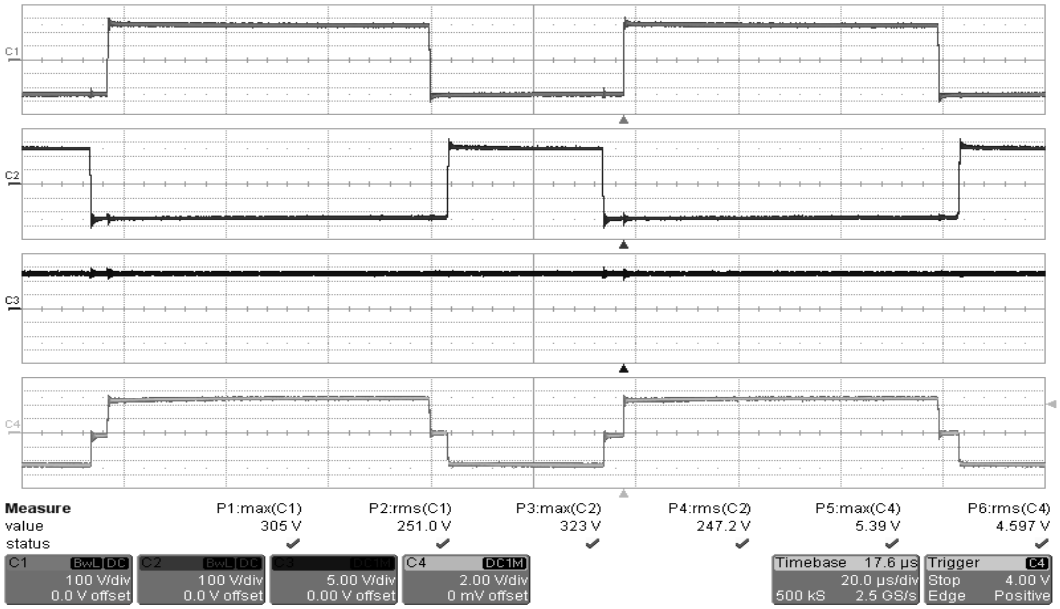


Figure 2.37 Experimental inverter output voltages (v_{ao}, v_{bo}, v_{co}) (top three, 100V/div) and the line-to-line voltage (v_{ab}) (bottom, 200V/div) waveforms for NSPWM (time scale: 20µs/div).

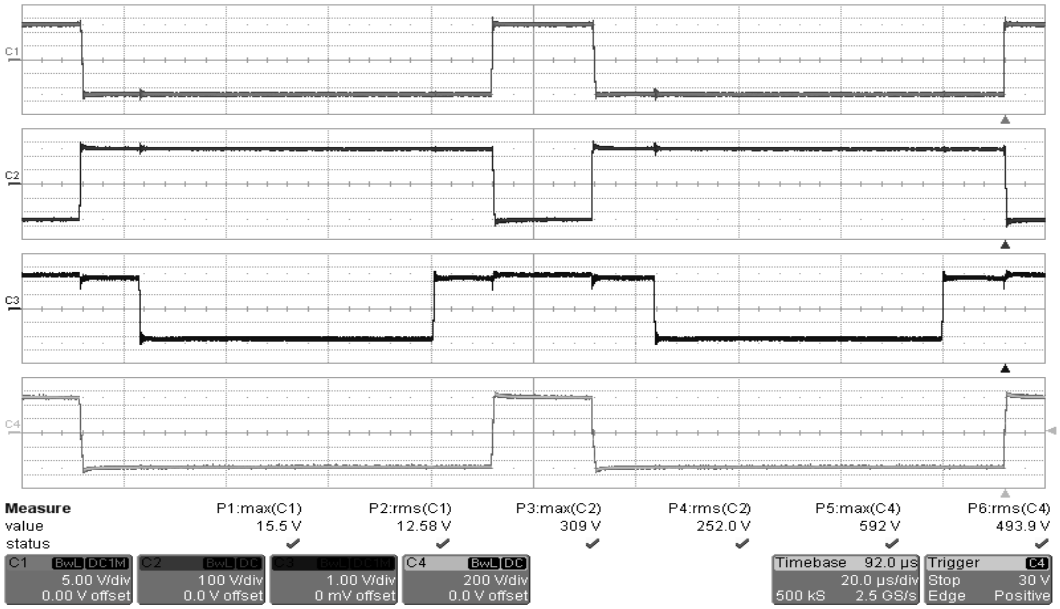


Figure 2.38 Experimental inverter output voltages (v_{ao}, v_{bo}, v_{co}) (top three, 100V/div) and the line-to-line voltage (v_{ab}) (bottom, 200V/div) waveforms for AZSPWM3 (time scale: 20µs/div).

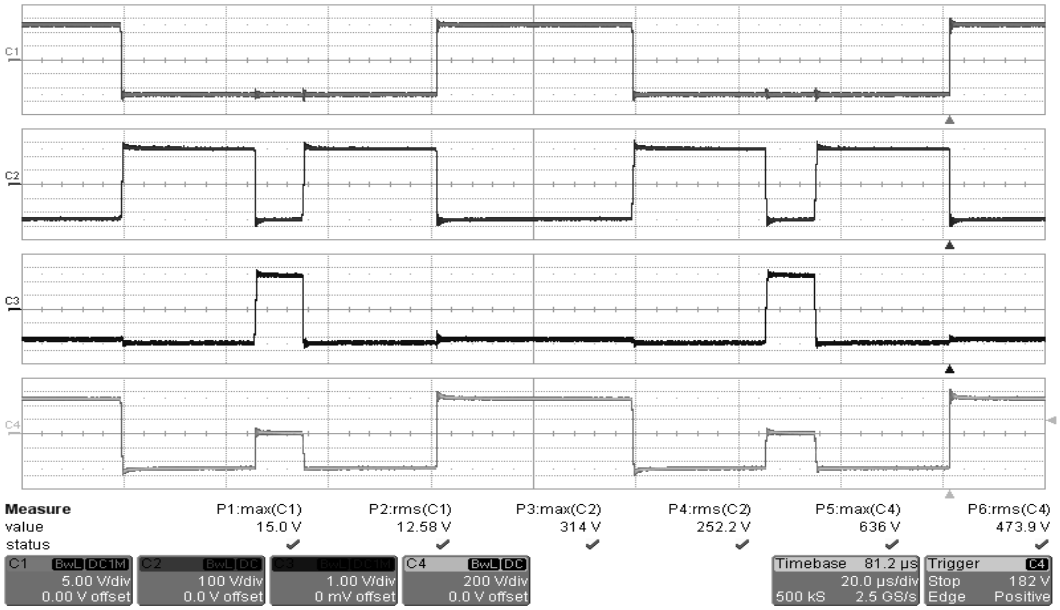


Figure 2.39 Experimental inverter output voltages (v_{ao}, v_{bo}, v_{co}) (top three, 100V/div) and the line-to-line voltage (v_{ab}) (bottom, 200V/div) waveforms for RSPWM3 (time scale: 20µs/div).

2.7 Summary

PWM principles are reviewed for three-phase, three-wire inverter drives. The characteristics, pulse patterns, and implementation of the popular PWM methods are discussed. The generalized scalar PWM approach is established and it is shown that it unites the conventional PWM methods and most recently developed reduced common mode voltage PWM methods under one umbrella. Through a detailed example, the method to generate the pulse patterns of these PWM methods via the generalized scalar PWM approach is illustrated. It is shown that the generalized scalar approach yields a simple and powerful implementation with modern control chips which have digital PWM units. With this approach, it becomes an easy task to program the pulse patterns of various high performance PWM methods and benefit from their performance in modern VSIs for applications such as motor drives, PWM rectifiers, and active filters.

The theory is verified by laboratory experiments. It is demonstrated that with the proposed approach both the conventional PWM pulse patterns (such as those of SVPWM and DPWM1) and the recently developed improved high frequency common mode voltage performance method pulse patterns (NSPWM, AZSPWM methods, and RSPWM methods) can be easily generated. Thus, the inverter design engineers are encouraged to include such pulse patterns in their designs.

In the next chapter, the undesired effects of PWM operation and their mitigation techniques will be discussed.

CHAPTER 3

HIGH FREQUENCY PWM EFFECTS AND MITIGATION TECHNIQUES

3.1 Introduction

In AC motor drives employing PWM-VSIs, inverter output rectangular pulses result undesired effects on the drive. While these effects can be tolerated to some degree in some applications, they can be prohibitive in some others. The high frequency effects can be mainly investigated in two groups. One group includes PWM frequency effects which are caused by output PWM voltage ripple. The other one involves much higher frequency effects related to the turn-on and turn-off times of the inverter switches which appear above 100 kHz levels. Various techniques have been proposed to mitigate these side effects. These mitigation techniques can be divided into two main groups: mitigation by additional devices at the inverter output and mitigation from the inverter which is the source of the high frequency effects. In this chapter, first, the high frequency effects will be discussed, and then various mitigation techniques will be reviewed.

3.2 PWM Frequency Effects

Since the VSI output voltage has PWM voltage pulses, it causes PWM ripple on the output current. The current ripple decreases with increasing output inductance. When the AC motor is directly connected to the VSI output, since the leakage inductance of the motor acts as a low-pass filter, it partially suppresses the PWM current ripple and the motor current is mainly sinusoidal. However, when the switching frequency is low or inverter output inductance is small, the ripple current

becomes high, which results high losses, thermal stresses, and acoustic noise in the motor. Also when the ripple current is high, inverter current reaches high peak values, which increases current stresses on the inverter switches. Thus, in such cases additional filters are needed to reduce the PWM ripple.

3.3 Effects Related to Switch Turn-On and Turn-Off Transients

The inverter output current ripple and the associated problems can be overcome by increasing the PWM switching frequency. This also reduces filter size and cost, and increases control bandwidth. Increasing the switching frequency requires fast turn-on and turn-off switches to confine the switching losses. The turn-on and turn-off times of modern IGBTs approach several hundred nanoseconds or less, which correspond to switching transients with frequencies of MHz range. At these frequencies, the parasitic capacitive elements of the motor drive become effective. For AC motor drives fed by the standard utility grid, the DC bus voltage is approximately 550V and for hundreds of nanoseconds switching times, the rate of change (*dv/dt*) of the inverter output voltage is as high as 5kV/μs. Interaction between these voltage pulses and the parasitic capacitances of the motor drive results undesired effects in the motor drive.

One of the important undesired effects of high *dv/dt* is voltage overshoot at the motor terminals which is caused by the rectangular shaped differential mode (line-to-line) voltages of the inverter. If the motor is a long distance from the inverter, the long cable connecting the motor to the inverter acts like a transmission line due to the parasitic capacitances and inductances of the cable which become effective at *dv/dt* related frequencies. Due to the voltage reflection, excessive overvoltage (higher than two times the DC bus voltage) may appear across the motor terminals (across the closest motor windings to the cable output terminals). These overvoltages can be as high as 3-4 times the DC bus voltage when there are instantaneous polarity reversals on the inverter output differential mode voltages [13]. Motor terminal overvoltages may result breakdown in the motor winding insulation and lead to motor failure [14].

High frequency common mode voltage (CMV) is the other harmful effect of inverter output voltage pulses. The CMV of a three-phase VSI is defined in (1.1), and according this formula, the CMV values of the two-level VSI for all switch states are shown in Table 3.1.

Table 3.1 The three-phase, two-level VSI switch states, phase voltages, and CMV

S_{a+} S_{b+} S_{c+}	v_{ao}	v_{bo}	v_{co}	v_{cm}
000	$-V_{dc}/2$	$-V_{dc}/2$	$-V_{dc}/2$	$-V_{dc}/2$
100	$V_{dc}/2$	$-V_{dc}/2$	$-V_{dc}/2$	$-V_{dc}/6$
110	$V_{dc}/2$	$V_{dc}/2$	$-V_{dc}/2$	$V_{dc}/6$
010	$-V_{dc}/2$	$V_{dc}/2$	$-V_{dc}/2$	$-V_{dc}/6$
011	$-V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/6$
001	$-V_{dc}/2$	$-V_{dc}/2$	$V_{dc}/2$	$-V_{dc}/6$
101	$V_{dc}/2$	$-V_{dc}/2$	$V_{dc}/2$	$V_{dc}/6$
111	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$

As seen from the table, during switch state changes, the CMV changes by $\pm V_{dc}/3$ regardless of the changing states. Thus, at switching times of several hundred nanoseconds and DC bus voltage levels above several hundred volts, the VSI generates high frequency CMV with high *dv/dt* and high magnitude. In Figure 3.1 the detailed high frequency common mode equivalent circuit of the motor drive system is illustrated [17], [34]. As seen from the figure, there are capacitive paths existing between the motor windings and frame which are effective especially at frequencies higher than 100 kHz. At such frequencies related to turn-on and turn-off times of the switches (which correspond to MHz range), these capacitive paths become effective. In practical applications, for safety reasons the conductive motor chassis is grounded. As a consequence, the high frequency CMV causes common mode current (CMC) (leakage current) from motor to ground and bearing currents which result in bearing failures, EMI, and nuisance trips in the system [9].

In Figure 3.2, the equivalent stray capacitances between the stator winding, rotor, and motor frame are illustrated separately [22]. At frequencies above 100 kHz, the common mode path is dominantly capacitive, and the cable resistance and motor

inductance can be neglected. In the figure, v_{cm} is the CMV appearing at the motor terminals. The four parasitic equivalent capacitors are as follows; C_{SF} is the stator windings to motor frame capacitance, C_{SR} is the stator winding to the rotor capacitance, C_{RF} is the rotor to the motor frame capacitance, and C_B is the bearing capacitance. In the figure, i_{cm} is the overall CMC flowing from the stator windings to the ground (CMC), v_b is the bearing voltage, and i_b is the bearing current. Among these capacitances C_{SF} is significantly larger than other capacitances, thus the CMC through the C_{SF} is the most dominant [22].

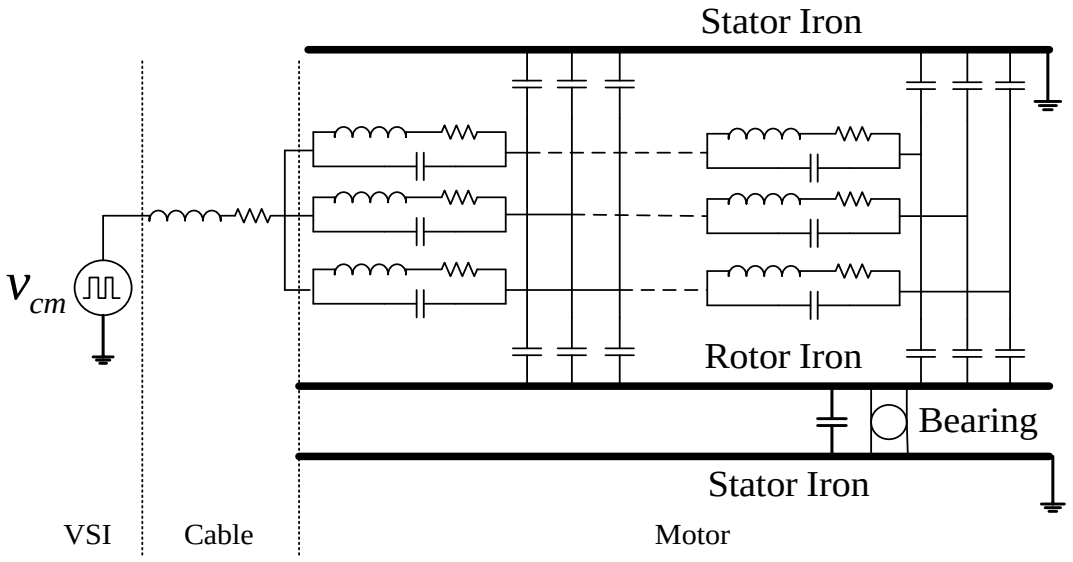


Figure 3.1 Detailed high frequency common mode equivalent circuit of a three-phase AC motor drive (assuming a short cable between the motor and inverter) [34].

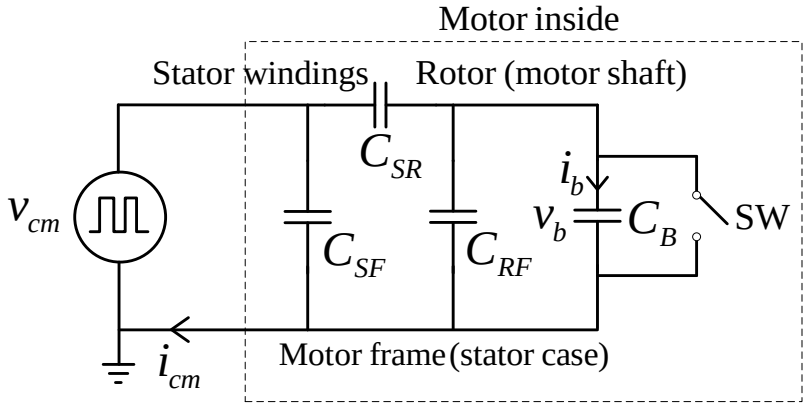


Figure 3.2 Equivalent capacitances between stator, rotor, and motor frame [22].

Another harmful current caused by high frequency CMV is bearing current which may cause bearing failures. There are various types of bearing currents which have different generating mechanisms. The inverter-induced bearing currents are classified in Figure 3.3 according to their causes. Four types of inverter-induced bearing currents can be distinguished [48]:

1) Capacitive bearing currents,
2) Electric discharge machining (EDM) bearing currents,
3) Circulating bearing currents,
4) Rotor to ground bearing currents.

The first two bearing current types are related to the CMV mirrored across the bearing, and the last two are caused by the CMC.

The common mode voltage at the motor terminals appears as the bearing voltage (or shaft voltage) by a capacitive voltage divider. The bearing voltage can be estimated via the Bearing Voltage Ratio (BVR) [49]:

$$BVR = \frac{v_b}{v_{cm}} = \frac{C_{SR}}{C_{SR} + C_{RF} + C_B} \tag{3.1}$$

The BVR is typically in the range of 2-10% [49]. The capacitive bearing currents are caused by the *dv/dt* of the bearing voltage. This type of bearing current is usually considered not dangerous to the drive since its magnitude is negligibly small compared to the other bearing current types [48].

EDM bearing currents result in due to the voltage built up over the bearing. Switch SW in Figure 3.2 models the dielectric breakdown in the grease films of the bearing. It is turned on when the bearing voltage is greater than the dielectric-breakdown voltage, and it remains turned off when the bearing voltage is below this voltage. If the bearing voltage exceeds the threshold voltage of the grease film between the balls and running surfaces (approximately 5-30V), the electrically loaded grease film breaks down. This breakdown causes an electric discharge machining (EDM) current pulse. EDM currents may destroy the grease on the

bearing, which results in corrosion on the bearing. The magnitude of the breakdown current is dependent on the bearing voltage before the discharge. Thus, higher magnitude of CMV results higher EDM current.

Another type of bearing current is the circulating bearing current. The CMC excites a circular magnetic flux around the motor shaft. This flux induces a voltage along the shaft, and between the two bearings of the motor. If this voltage is high enough to break down the grease film of the bearing and destroy its insulating properties, it causes a circulating bearing current in the "stator frame-nondrive end-shaft-drive end" loop [48]. Since the circulating bearing current is caused by the CMC, it is significantly dependent on the *dv/dt* rate of the CMV.

In operations where the rotor is grounded (e.g., via the mechanical load), an important amount of the overall CMC can pass the bearings as rotor ground current. Bearing currents due to rotor ground currents can reach significant magnitudes with increasing motor size and destroy bearings in short time of operation [48].

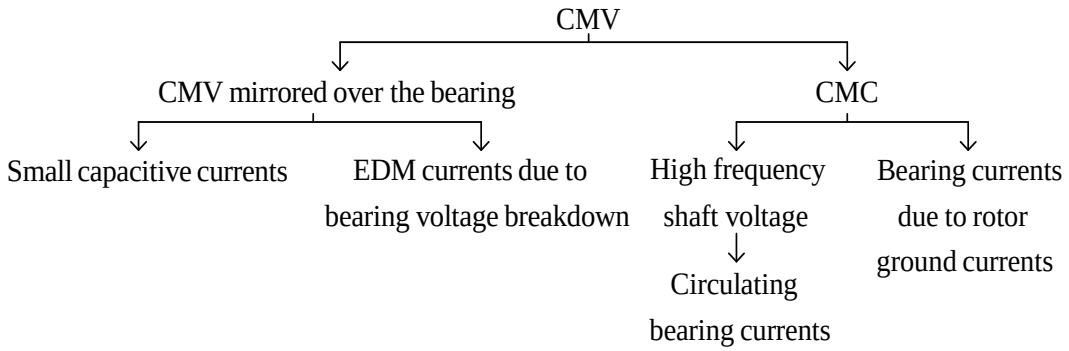


Figure 3.3 Classification of the different bearing current types according to their causes [48].

3.3.1 Factors Affecting CMC and Bearing Currents

The CMC is caused mainly because of the interaction of the high frequency CMV at the motor terminals and the capacitances between motor windings and grounded motor chassis. Therefore, the drives with higher DC bus voltage level and/or higher switching speed cause higher CMC. In large motors the equivalent capacitance between the phase windings and chassis is greater than the smaller motors which results in higher CMC [12]. The magnitude of the EDM bearing current is dependent on the bearing voltage before the discharge. Therefore, higher CMV magnitude causes higher EDM currents [22], [49]. Since the circulating type bearing currents are induced by CMC, the magnitude of the circulating bearing current change by approximately the same percentages as the CMC [10]. Bearing currents are also significantly dependent of the motor size [49]. In the small size motors (few kW and below) nearly all bearing currents are EDM type bearing currents. With large motors (100 kW and above), circulating bearing currents are dominant [49].

3.4 Mitigation Techniques For The High Frequency PWM Effects

The most important PWM originated problems are discussed in the previous sections. While these negative effects can be tolerated to some degree in some applications, they can be prohibitive in some others (such as long cable applications, applications where a specified EMC performance is required, critical applications where the cost of downtime is high, etc.). Thus, depending on the specific application, the mitigation of some or all of these effects may be necessary.

In order to solve these problems various techniques that have been proposed in the literature. These techniques can be divided into two groups. One approach involves suppressing the side effects through external devices. This technique includes passive and active filters inserted between the inverter and the motor. An alternative approach involves reduction the noise from the inverter (where it is generated) by means of topological change (such as utilizing the three-level Neutral-Point-

Clamped (NPC) VSI [26], instead of the two-level VSI) or by PWM pulse pattern modification in the two-level VSI. In this section these solution techniques will be reviewed.

3.4.1 Inverter Output Filters

Various inverter output filter topologies have been proposed. In the passive filters only passive components (inductor, capacitor, resistor, and diode) and their combinations are utilized. In the active filters, controlled semiconductor switches are utilized as well as passive components. While some of these filters suppress only differential mode or common mode noise, some of them suppress both types of noise. In the following, a survey of various output filter topologies that are typically employed in industrial applications is presented.

3.4.1.1 Output Reactor

The simplest differential mode filter is an output reactor. Shown in Figure 3.4, an output reactor consists of a three-phase inductor placed at the output of the inverter. It reduces the *dv/dt* of the motor terminal voltage and the PWM ripple current (by increasing the load inductance). However, in some applications, such as long cable applications, a resonance may occur between the cable capacitance and the reactor. In such cases, voltage overshoots may be further amplified at the motor terminals [13]. Generally, an output reactor, having 3%-5% impedance ratio is inserted at the inverter output [15]. The impedance ratio of the reactor is calculated by (3.2).

$$Z(\%) = \frac{2\pi f_r L_D \cdot I_r}{V_r} \tag{3.2}$$

where Z(%) is the impedance ratio, L_D is the inductance value, f_r is the rated motor frequency, I_r is the rated motor current (rms), V_r is the rated motor voltage (rms).

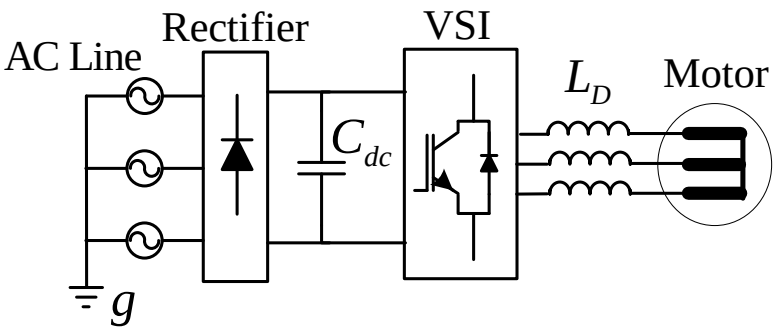


Figure 3.4 Utilization of an output reactor in a motor drive.

3.4.1.2 Differential Mode LCR Filters

Figure 3.5 shows a standard commonly used differential mode LCR filter topology. It consists of a three-phase reactor, three capacitors, and three damping resistors forming a second-order low-pass filter. The frequency components below the cut-off frequency pass almost without reduction of magnitude, whereas the frequency components above the cut-off frequency are filtered. The cut-off frequency is expressed as (3.3).

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{3.3}$$

This filter has two types according to the filter cut-off frequency: differential mode *dv/dt* filter and differential mode sine filter (SF) [13]. The cut-off frequency of the differential mode *dv/dt* filter is above the PWM frequency, and its main aim is to reduce the *dv/dt* of the motor terminal voltage. The cut-off frequency of the differential mode SF is below the PWM frequency, thus it eliminates the differential mode PWM frequency components and switching ripple current, and makes motor terminal voltages sinusoidal. However, the control bandwidth of the inverter is limited by the filter cut-off frequency. Thus, there is a trade-off between the differential mode suppression and the control bandwidth of the drive. In the differential mode *dv/dt* filter voltage overshoots which may occur due to LC

resonance can be damped out by the damping resistors R_D. Because of the damping, the differential mode *dv/dt* filter has better performance compared to the output reactor. In SF, R_D damps oscillations due to disturbances in the inverter and control dynamics. The components of the SF are larger than those of the *dv/dt* filter, thus it increases system size and cost.

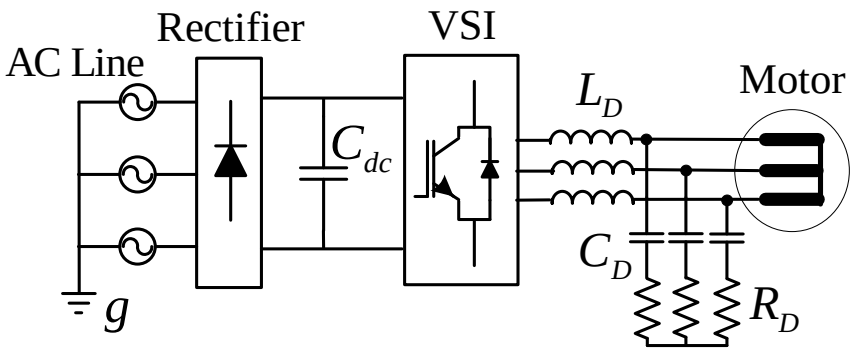


Figure 3.5 Utilization of a standard differential mode LCR filter in a motor drive.

3.4.1.3 Common Mode Inductor

The simplest passive common mode filtering method is adding a common mode inductor [(CMI), also known as common mode choke] between the inverter output and the motor [16] (Figure 3.6). In the CMI, three-phase windings are wound in the same direction around a common core, thus the CMC causes a net flux which provides high common mode impedance and suppresses the CMC. Since the sum of symmetrical three-phase currents is zero, they do not cause a net flux in the core, and the differential mode inductance of the CMI is ideally zero. The CMI is a cost-effective method of reducing such CMCs, and reductions of the original CMC to as low as 10% have been reported [50]. Since the circulating type bearing currents are induced by the CMC, the amplitude of the circulating bearing current is also reduced by approximately the same percentages as the CMC [10].

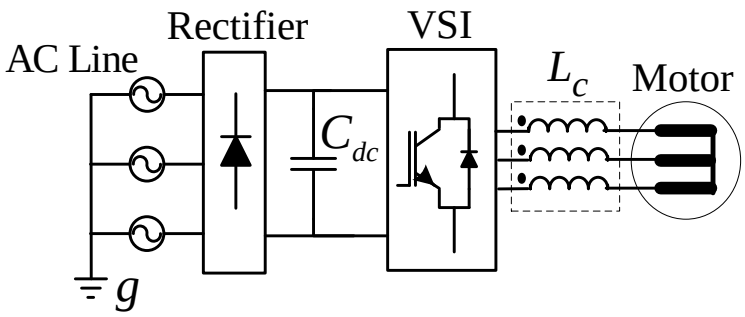


Figure 3.6 Utilization of a common mode inductor in a motor drive.

The CMC with peak magnitude I_{cm} causes magnetic field intensity with amplitude H which results in the flux density B. Therefore, a CMI represents a common mode inductance L_{cm} in the common mode circuit [51]. The inductance L_{cm} is given by (3.4), where λ is the total flux linkage in the core, μ is the permeability of the magnetic core, A_c and l_c are the cross sectional area and the circumferential length of the toroidal core respectively, and N is the number of turns per-phase.

$$L_{cm} = \frac{\lambda}{I_{cm}} = \frac{N \cdot B \cdot A_c}{I_{cm}} = \frac{N \cdot \mu \cdot H \cdot A_c}{I_{cm}} = \frac{N^2 \cdot \mu \cdot A_c}{\pi \cdot l_c} \tag{3.4}$$

If the magnetic field caused by the peak current I_{cm} exceeds the saturation flux density B_{sat}, the performance of the CMI decreases, because the value of the inductance L_{cm} decreases with increasing degree of saturation. Therefore, a CMI should be designed according to the B_{sat} value of the core such that the peak current does not saturate the core. Using (3.4), maximum number of turns is determined for a given core (keeping l_c and μ constant) as expressed in (3.5).

$$N \leq \frac{l_c \cdot \pi \cdot B_{sat}}{I_{cm,max} \cdot \mu} \tag{3.5}$$

Inductance values of the CMIs are typically a few mH and the equivalent common mode capacitances of motors at several kW power ratings are in the order of few

nF. The peak CMC is related to the CMV change with high *dv/dt*, which corresponds to MHz range. At such frequencies, the impedance of the CMI is more dominant than the motor common mode impedance. Thus it effectively suppresses CMC. However, at the CMV frequencies (PWM frequencies) the common mode impedance of the motor is much higher than that of the CMIs, thus the CMIs do not suppress the CMV on the motor. Therefore, the voltage buildup in the bearings which mirror the CMV is not eliminated, and as a result the shaft voltage and EDM type bearing currents are not suppressed by the CMI [10], [22].

The CMC has an oscillatory waveform when the CMI is inserted. While the CMI suppresses the spikes on the CMC, if the core is low-loss type it causes oscillation, and it can not reduce the rms value of the CMC significantly. In lossy cores, the series equivalent of the CMI is an inductance series to a resistance which represents the core loss. The quality factor (Q) of the CMI given in (3.6) is the ratio of its inductance to its resistance at a given frequency and it is a measure of its loss characteristics.

$$Q = \frac{\omega L}{R} \tag{3.6}$$

The lower the quality factor of the inductor, the more lossy characteristics it has. A CMI with lossy core increases the common mode resistance as well as the inductance in the common mode equivalent circuit and helps the oscillation to damp faster, resulting in less rms CMC. Generally, toroidal cores used in CMIs have high core losses at high frequencies related with the CMC, and they can successfully damp the oscillation of the CMC and reduce rms CMC.

3.4.1.4 Common Mode Transformer

Another passive mitigation method of reducing CMC is utilizing a common mode transformer (CMT) [17] (Figure 3.7). The difference between the CMT and the CMI is that the CMT consists a secondary winding on the toroidal core which is

terminated by a damping resistor. If the core material is low-loss, the CMI causes oscillation on the CMC and can not suppress rms CMC.

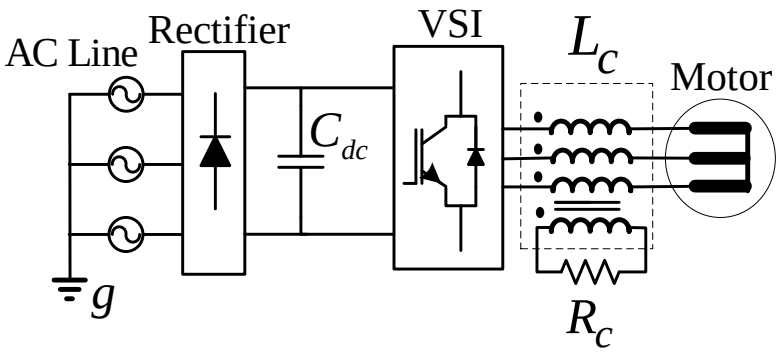
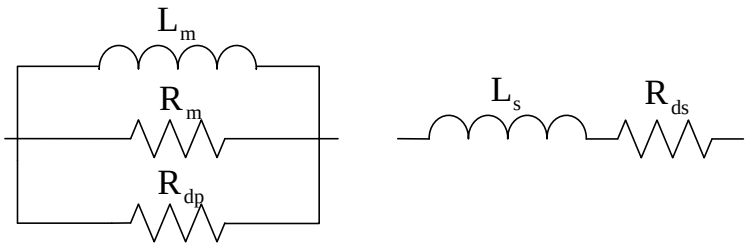


Figure 3.7 Utilization of a common mode transformer in a motor drive.

The simplified equivalent circuit of a CMT is given in Figure 3.8. Here L_m and R_m are the parallel magnetizing inductance and the parallel core loss resistance of the CMT. R_{dp} is the additional secondary damping resistor. When the secondary side is open circuited (infinite R_{dp}) equivalent circuit of the CMT is same as that of the CMI. The equivalent circuit of the CMT can also be modeled as a series R-L circuit (Figure 3.8.b). The additional secondary damping resistor increases the shunt conductance of the parallel equivalent circuit and thus increases the series resistance in the R-L equivalent circuit. The series equivalent resistor (R_{ds}) suppresses the CMC oscillations. Therefore, utilizing a CMT both the peak and rms values of CMC can be reduced [17].



(a) (b)

Figure 3.8 Simplified common mode equivalent circuit of the CMT (a) parallel equivalent circuit, (b) series equivalent circuit.

The damping resistor value is very important in the performance of the CMT. The optimum parallel equivalent resistor (R_{dp}) should be calculated as (3.7) where C is the equivalent CM stray capacitance of the motor between the phase windings and the ground [17].

$$R_{dp,opt} = \frac{1}{2}\sqrt{\frac{L_m}{C}} \tag{3.7}$$

In low-loss cores, the core loss resistance of the transformer (R_m) can be neglected (open-circuited), and the R_{dp} resistor can be selected as $R_{dp,opt}$ as calculated in (3.7). However, in high-loss cores R_m is relatively low and its value may be close to the optimum parallel equivalent resistor $R_{dp,opt}$. In such cases, R_m should be taken into account to calculate the optimum parallel equivalent resistor $R_{dp,opt}$ [17].

3.4.1.5 LCR Type Filters with DC Bus Connection

There are also more complex RLC type filters with connection to DC bus of the inverter [18], [20], [21], [22]. These filters are generally combinations of the filters discussed above. The DC bus connection in these filters provides a common mode impedance path parallel to the load, which circulates the common mode noise inside the inverter rather than the load.

The filter shown in Figure 3.9 consists of a common mode inductor (L_C), along with two capacitors C_C and a resistor R_C which forms the common mode suppression part. One terminal of the resistor is connected to motor neutral point, while the other to the midpoint of the capacitors. This construction eliminates the high frequency CMV from the motor and suppresses the motor CMC very effectively [21]. The differential mode filter part which consists of a parallel-connected inductor L_D and a resistor R_D per-phase, reduce and damps out the voltage overshoots at the motor terminals. The disadvantage of this topology is that it requires a connection to the neutral point of the motor which may not be available.

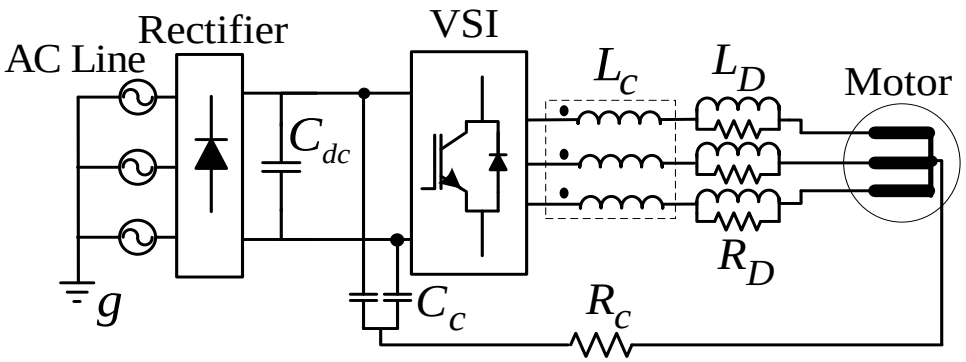


Figure 3.9 The LCR type filter with connection to motor neutral point and DC bus.

Shown in Figure 3.10, the pure sine filter (PSF) with connection to DC bus is the most involved filter type considered for the motor drives [20]. The common mode inductor L_C suppresses the CMC, the differential mode SF ($L_DC_DR_D$) makes motor terminal voltage sinusoidal and eliminates PWM ripple from the motor current. The neutral point of the filter is connected to the DC bus (to the midpoint or positive/negative pole) through a capacitor C_C and a resistor R_C such that a low impedance path for the CMC, which is parallel to the motor CMC path, is formed. This construction further reduces the CMC through the motor and eliminates the high frequency CMV from the motor. Although the filter increases the system cost and size due to the large filter component count and size, it provides a complete solution to all of the high frequency effects caused by the inverter. This topology will be discussed to detail in Chapter 5.

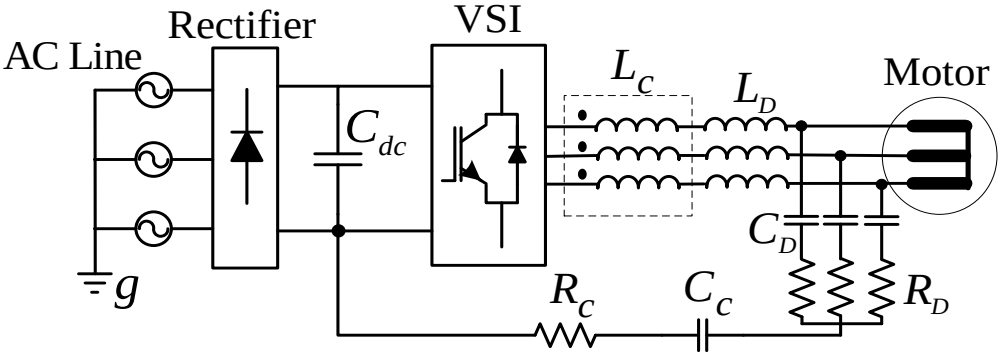


Figure 3.10 The pure sine filter with DC bus connection.

3.4.1.6 Active Common Mode Voltage Filter

In order to suppress the CMV, active filters have been also utilized. They consist of semiconductor switches as well as passive component [23], [24], [25], [52]. The filter shown in Figure 3.11 is an active common-noise canceller (ACC) for eliminating the CMV generated by a PWM inverter [23]. The filter is composed of a CMV detector with three C_1 capacitors, a common mode transformer with 1:1 turn ratio, a push-pull emitter follower, and two C_0 capacitors which form DC bus midpoint. The neutral point of C_1 capacitors indicate the CMV value. The mapped voltage is applied to the CMT secondary winding after buffering by the emitter-follower. The CMT utilized in this method is same as explained previously, except an emitter follower is connected to the secondary winding of the CMT instead of a damping resistor. The filter superimposes a compensating voltage at the inverter output. The compensating voltage applied has the same amplitude as, but opposite polarity to the CMV produced by the inverter. As a result, the CMV applied to the load is cancelled completely, and the CMC is eliminated. However, the method is problematic due to complexity and reliability, and power semiconductor switches utilized increase the cost of the filters significantly.

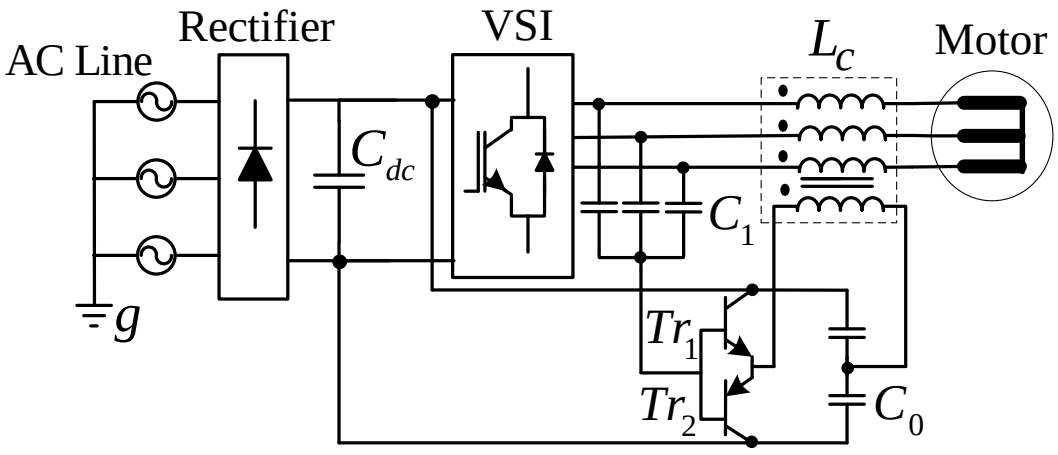


Figure 3.11 Motor drive with active CMV filter.

3.4.1.7 Comparison of The Discussed Filter Types

All filters have a size and cost penalty. Thus the selection of the filter type should be done according to negative effects to be mitigated. Table 3.2 summarizes the performance overview of the discussed filter types.

Table 3.2 Performance overview of the discussed filter types

Filter type	Negative effects				
	Motor overvoltage	PWM ripple	CMV	CMC	Bearing currents
Output reactor (L_D)	-	+	- -	-	-
Common mode inductor (L_C), common mode transformer	- -	- -	-	+	+
Differential mode *dv/dt* filter ($L_DC_DR_D$)	+	-	- -	-	-
Differential mode sine filter ($L_DC_DR_D$)	++	++	- -	-	-
Filters with DC bus connection ($L_CC_CR_C$-$L_DC_DR_D$)	++	++	++	++	++
Active CMV filter	- -	- -	++	++	++

- - not effective - partially effective + effective ++ very effective

3.4.2 Mitigation of PWM Effects From The VSI

3.4.2.1 PWM Pulse Pattern Modification

As discussed in chapter 2, a large number of PWM methods exist and each method has a unique pulse pattern, and thus they have different performance characteristics. Therefore, the PWM methods to be utilized should be selected according to the application requirements. For low PWM ripple, SVPWM is the best method. But the ripple increases as M_i increases. At high M_i a discontinuous PWM method can

be utilized. For example increasing the switching frequency by 50% and utilizing DPWM1 the switching losses are kept the same as in SVPWM, while the PWM ripple is reduced compared to SVPMW. Thus, at low M_i SVPWM and at high M_i DPWM1 is favorable for low PWM ripple. However, utilizing at least one of the zero states, both SVPWM and DPWM1 result in high CMV ($\pm V_{dc}/2$) and CMC [35]. Thus, reduction of the CMV is only possible by avoiding the zero states. The recently proposed RCMV-PWM methods limit the CMV to $\pm V_{dc}/6$ based on this principle. Utilization of the RCMV-PWM methods together with additional small sized filters provides effective and economical CMV/CMC reduction performance. Although all RCMV-PWM methods theoretically reduce CMV, implementation of some of them such as AZSPWM2, AZSPWM3, and RSPWM3, etc. is problematic. Since they require simultaneous switching of two inverter legs, rapid line-to-line voltage reversal occurs which results motor terminal overvoltage problems in long cable applications. Additionally, simultaneous inverter legs switching is very difficult to realize (due to dead-time, unequal rise and fall time of switches, etc.), and unexpected zero states may appear which causes high CMV, and the advantage of the methods disappears. Of the RCMV-PWM methods only AZSPWM1 and NSPWM are free of these problems. Since NSPWM has lower ripple, it is more favorable. For $M_i<0.61$, since NSPWM is not applicable, at low M_i AZSPWM1 is favored. Thus, at low M_i AZSPWM1 and at high M_i NSPWM is favorable for the applications requiring low CMV and CMC.

The PWM pulse pattern modification can be applied by software. Since the hardware remains the same, no additional cost results. Therefore, utilizing the suitable PWM method reduces additional filter requirements, and thus reduces system cost and size.

3.4.2.2 Multi-level Inverter Topologies

There are various VSI topologies utilized at different kinds of applications. All VSI types have different performance attributes. The two-level, three-phase VSI is the most common inverter type utilized at the low voltage applications (DC bus voltage

of 500-600V). However, as the DC bus voltage level is increased, the two-level VSI is not preferred since higher blocking voltage (V_{dc}) is required for the switches. Also, the VSI output voltage change (V_{dc}) becomes excessive. Therefore, in the higher DC bus voltage applications than 500-600V, often three or higher-level VSIs are utilized since they result in less voltage stress over the semiconductor switches.

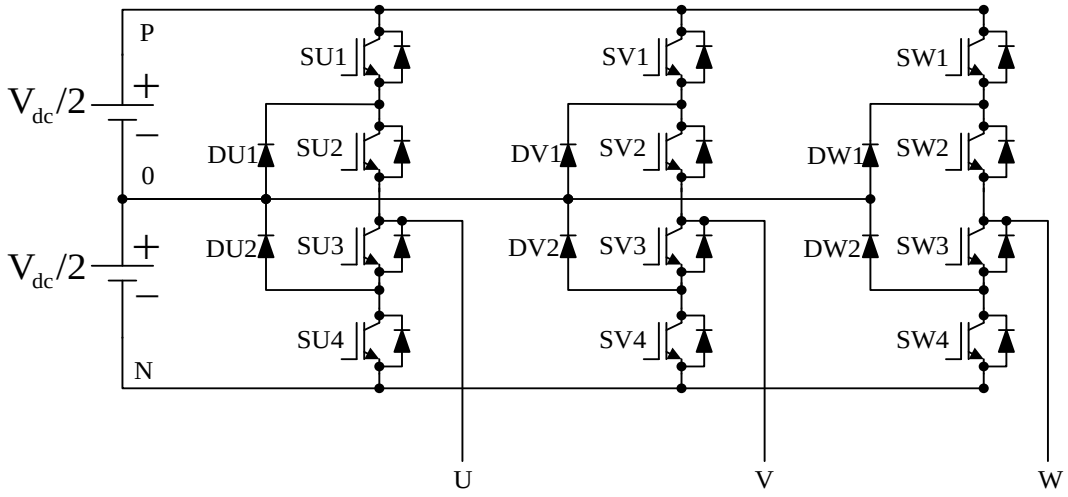


Figure 3.12 The three-level neutral-point-clamped VSI topology.

Shown in Figure 3.12, the three-level Neutral Point Clamped (NPC) VSI [26] involves an active midpoint in the DC bus. Each leg has four switches connected in series and anti-parallel diodes for each switch. Taking phase U as an example, the circuit behaves in the following manner. When SU1 and SU2 are turned on, output U is connected to the positive rail (P) of the DC bus. When SU2 and SU3 are on, it is connected to the mid-point (O), and when SU3 and SU4 are on, it is connected to the negative rail (N). Thus, the output can take three voltage values (three levels) compared to two values for the two-level VSI topology. Relation between the switch states and the resulting output voltages with respect to the DC mid-point are summarized in Table 3.3.

Table 3.3 The three-level VSI switch states and output voltages

	SU1	**SU2**	**SU3**	**SU4**	**v_{UO}**
Switch States	ON	ON	OFF	OFF	$+V_{dc}/2$
	OFF	OFF	ON	ON	$-V_{dc}/2$
	OFF	ON	ON	OFF	0

As seen from the table, the output voltage of the three-level VSI takes the values of 0, and $\pm V_{dc}/2$, and hence, the line-to-line voltage can take the values of 0, $\pm V_{dc}/2$, $\pm V_{dc}$, and from the expression (1.1), the CMV can take the values of 0, $\pm V_{dc}/6$, $\pm V_{dc}/3$, $\pm V_{dc}/2$ according to the switch states. The changes of the line-to-line voltages and the CMV are $V_{dc}/2$ and $V_{dc}/6$, respectively, which are the half of those in the two-level VSI. Consequently, the PWM current ripple and the CMC are lower than the two-level VSI for the same switching frequency. Also the overvoltage at the motor terminal is lower than that of two-level inverter due to lower line-to-line voltage steps. Note that the line-to-line and the CMV values defined here are topologic properties of the three-level inverters and some of these voltage levels may not be generated at different PWM methods. By utilizing different PWM methods these side effects can be further reduced in the three-level VSI [53] The most common PWM method utilized in the three-level NPC-VSI is the Nearest Triangle Vector (NTV) PWM method [54]. In this method, for $M_i<0.5$ the maximum CMV magnitude is $V_{dc}/2$ as in the conventional methods with two-level VSI, and for $M_i>0.5$ the maximum CMV magnitude is $V_{dc}/3$. The step change of the CMV is $V_{dc}/6$ in both cases.

Consequently, high frequency noise performance of the three-level VSI is better than that of the two-level VSI. On the other hand, due to its complex topology and control, the three-level inverters are expensive and have found limited growth in the general purpose inverter drives market for 400V AC line applications.

3.5 Summary

In this chapter, the high frequency effects of PWM and their mitigation techniques are reviewed. The high frequency effects can be mitigated by passive or active inverter output filters. For achieving better suppression performance, larger filters are needed. This increases system size and cost. The high frequency effects also can be reduced from the source. While utilizing a multi-level inverter involves a significant cost increase, the PWM pulse pattern modification approach is practically free as there is no hardware addition or modification involved. Utilizing the suitable the PWM technique, additional filter requirements can be reduced, thus the cost and size of such filters could be less.

In the next chapter, the common mode voltage and common mode current suppression by PWM pulse pattern modification, by utilizing three-level inverter, and by utilizing the common mode inductor will be investigated.

CHAPTER 4

COMMON MODE VOLTAGE AND COMMON MODE CURRENT REDUCTION

4.1 Introduction

As discussed in the previous chapter, the three-phase, two-level inverter generates high frequency common mode voltage (CMV) with high *dv/dt* and magnitude. High CMV causes high common mode current (CMC) and this results in fluting bearing failures, EMI, and nuisance trips in the system [9].

The theoretical characteristics and some basic experimental CMV/CMC performance of most conventional and RCMV-PWM methods have been reported in the literature extensively [7], [8], [33], [34], [55], [56]. The CMV/CMC reduction performance of various inverter output filters and inverter topologies are also studied [55], [56], [57]. However, detailed experimental investigations about the effects of CMV pulse patterns on CMC have not been reported.

In this chapter, different properties of CMV such as magnitude, *dv/dt* rate, and consecutive pulses are separately investigated. The effects of these factors on CMC are observed. Using a prototype two-level VSI, CMV/CMC performances of various PWM methods are investigated. Also a commercial two-level and a three-level VSI are utilized, and compared with the prototype two-level VSI.

In addition to different PWM methods and inverter topologies, the common mode inductor (CMI), which is the simplest CMC suppression technique, is included.

CMV/CMC suppression performances of various CMIs with different core materials are investigated. The relationship between the common mode inductor parameters (such as inductance and loss factor) and CMC suppression is also investigated.

In conclusion, all practical CMV/CMC reduction techniques except those within the motor are included. First, the CMV pulse patterns of various PWM methods are reviewed. Then the properties of the utilized CMIs are given. Finally, the detailed experimental CMV/CMC performances of the discussed approaches are investigated and they are compared with each other.

4.2 CMV Pulse Patterns of Various PWM Methods

Switch logic signals and CMV pulse patterns for the considered PWM methods are shown in Figure 4.1. In the conventional SVPWM and DPWM1 methods, the CMV magnitude reaches $V_{dc}/2$. In the RCMV-PWM methods, the CMV magnitude is reduced to $V_{dc}/6$, but the step change (Δv) of the CMV is the same as that of conventional PWM methods ($V_{dc}/3$) except RSPWM3 (In RSPWM3, CMV variation is theoretically zero but in practice CMV changes of $V_{dc}/3$ are created due to the reasons discussed in chapter 2). Considering the switching times (Δt) (turn-on and turn-off times) is constant, the *dv/dt* rate of CMV will be the same. Since the CMC is mainly caused due to the interaction of the parasitic capacitances of the motor and the *dv/dt* of CMV, the CMC reduction in RCMV-PWM methods is not as significant as the CMV characteristic [8], [55]. However, even if the *dv/dt* is the same, it has been shown that the CMV pulse pattern also affects CMC noticeably [8], [55]. Direction of the consecutive CMV changes and the time interval between them are dependent on the CMV pattern, which affects CMC characteristics.

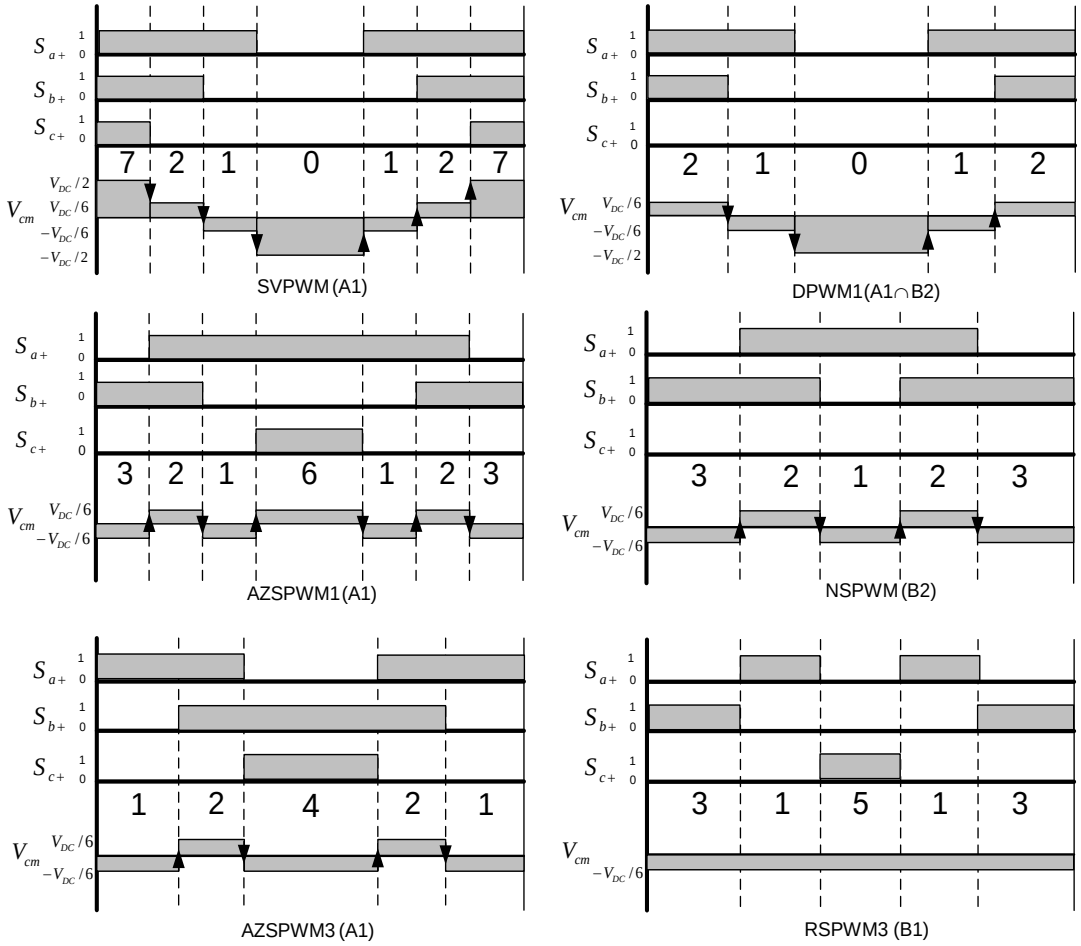


Figure 4.1 Switch signals and CMV pulse patterns of the considered PWM methods.

In the following, the consecutive CMV changes of the PWM methods are discussed. In the conventional SVPWM and DPWM1 methods, consecutive CMV changes at the same direction exist. For example, while voltage vectors change in the sequence of V_2-V_1-V_0, the CMV changes in the sequence of $(+V_{dc}/6)\rightarrow(-V_{dc}/6)\rightarrow(-V_{dc}/2)$ and two CMV changes of $-V_{dc}/3$ occur consecutively. On the other hand, CMC has an oscillatory waveform and when a second switching occurs while CMC initiated by the previous one is still oscillating, the resultant CMC is a superposition of two currents following the two switching instants [12]. As a result, when the time interval between these consecutive CMV changes is too short, the oscillating CMCs

superpose and the resultant CMC magnitude becomes higher than that caused by single CMV change.

Figures 4.2-4.4 illustrate these cases. As illustrated in Figure 4.2 for SVPWM and in Figure 4.3 for DPWM1, when the reference output voltage vector is near the A1-A2 region boundary, the duty cycle of V_1 gets narrower and at the boundary it disappears. This case occurs at every 60° region boundaries. Figure 4.4 shows the three CMV changes in the same direction with short time intervals for SVPWM. As M_i decreases the duty cycles of both active vectors get narrower and CMV changes three times in the same direction with very short time intervals. In DPWM1, this case does not occur since only one of the zero vectors (V_0 or V_7) is utilized in every 60° region.

In RCMV-PWM methods, since CMV changes between $\pm V_{dc}/6$, consecutive CMV changes always occur in the reverse direction as illustrated in Figure 4.1 for NSPWM, AZSPWM1, and AZSPWM3. In the experimental results section, it will be shown that consecutive CMV changes in the same direction in conventional PWM methods increase peak CMC noticeably compared to the RCMV-PWM methods. Also unexpected CMV changes in AZSPWM3 and RSPWM3, which result high CMC, will be shown.

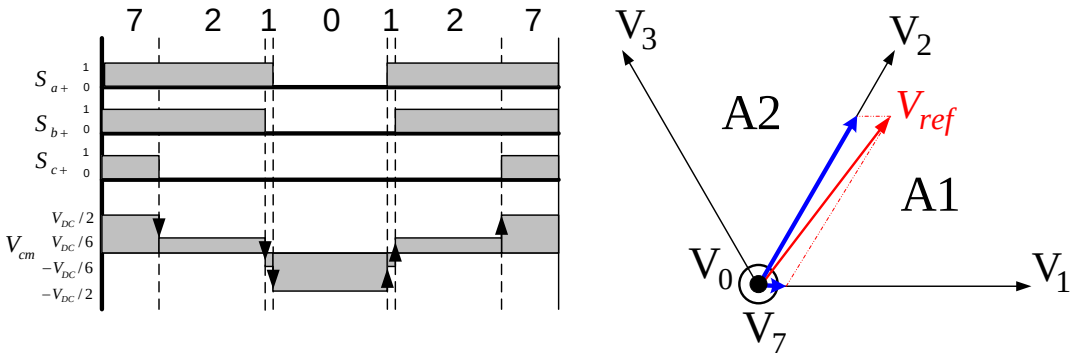


Figure 4.2 CMV pulse pattern of SVPWM near A1-A2 region boundary.

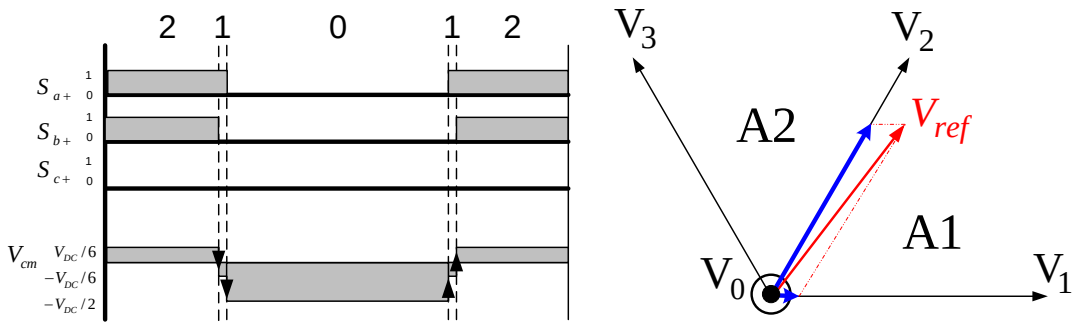


Figure 4.3 CMV pulse pattern of DPWM1 near A1-A2 region boundary.

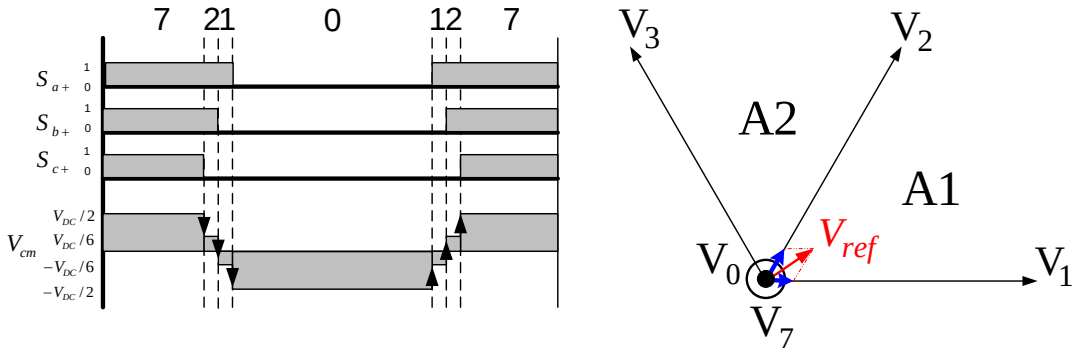


Figure 4.4 CMV pulse pattern of SVPWM at very low M_i.

4.3 Common Mode Inductors

In order to investigate the CMC/CMV reduction performance of the CMI, various CMIs, shown in Figure 4.5, with different core materials are tested. CMI-1, CMI-2, and CMI-3 are prototype CMIs. CMI-4 and CMI-5 are commercial CMIs. The properties of the utilized CMIs are given in Table 4.1. In the design of the CMIs, the number of turns is determined according to equation (3.5) such that the cores do not enter into magnetic saturation. In the equation (3.5), B_{sat}, l_c, and μ values of the cores are taken from their datasheets. The maximum peak CMC without any CMI (about 1A) is taken as the maximum CMC that will not saturate the core ($I_{cm,max}$). Consequently, the CMIs are designed to have maximum number of turns that does not saturate the core, thus they provide maximum common mode inductance and hence maximum CMC suppression. The commercial CMIs are from

Vacuumschmelze [58]. They are listed according to the rated phase current of the windings. The rated current of the motor is 8A, thus the two CMIs, of which rated winding current are 8A, are selected from the product list of Vacuumschmelze.

Each CMI utilizes different magnetic cores, thus their magnetic characteristics are unique. The core material of CMI-1 is ferrite, the core material of the others is nanocrystalline which has been developed recently and can operate at higher flux density than the ferrite core (0.4T of ferrite vs. 1.2T of nanocrystalline). The common mode inductances of the CMIs are measured at 10 kHz, 50 kHz, and 100 kHz to observe the frequency dependency of inductance values. The quality factors of the CMIs are also measured to compare their loss characteristics. As seen in the Table 4.1, CMI-4 is much less lossy than the other CMIs. As seen in Figure 4.5, CMI-1 and CMI-4 are very close to each other in size, and CMI-2, CMI-3, and CMI-5 are larger than these two.

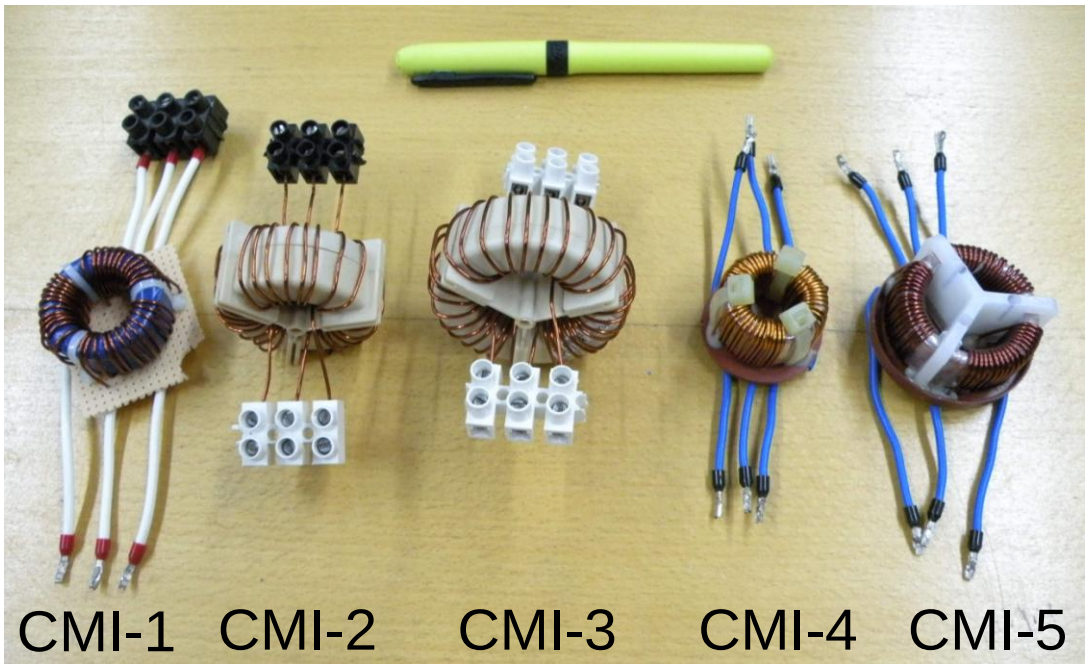


Figure 4.5 The CMIs utilized in the experiment.

Table 4.1 Properties of the utilized CMIs

	CMI-1	CMI-2	CMI-3	CMI-4	CMI-5
Magnetic core manufacturer	Acme	Hitachi	Hitachi	Vacuumschmelze	Vacuumschmelze
Magnetic material	Ferrite	Nanocrystalline	Nanocrystalline	Nanocrystalline	Nanocrystalline
Saturation flux density (T) @ 25˚C	0.38	1.23	1.23	1.23	1.23
Common mode inductance (mH) @ 10kHz	2.2	5.5	7.6	3.3	9.0
Common mode inductance (mH) @ 50kHz	1.21	2.75	3.20	3.03	5.40
Common mode inductance (mH) @ 100kHz	0.67	1.45	1.61	2.56	3.21
Quality factor @ 10kHz	4.3	3.7	3.1	17.9	4.8
Quality factor @ 50kHz	1.2	1.1	1	4.1	1.4
Quality factor @ 100kHz	0.8	0.75	0.66	2.2	0.98
Relative permeability (μ_r)	12000	17000	17000	20000	30000
Turn number per phase (N)	12	9	11	14	17
Outer diameter (mm)	36	46	54	29	42
Inner diameter (mm)	23	21	30	18	30
Height (mm)	15	19	19	18	20

4.4 Experimental Results

4.4.1 Experimental Setup

In the experiments, a two-level prototype VSI is experimentally evaluated with and without the CMIs and for SVPWM, DPWM1, NSPWM, AZSPWM1, AZSPWM3 and RSPWM3. Then the three-level NPC-VSI is considered with and without the CMIs. The three-level NPC-VSI is a commercial drive, which is Yaskawa Varispeed G7 with output ratings 3.7 kVA, 6.2A and input rating of 380-480V. Also a commercial two-level VSI, Siemens Micromaster 6SE3121 with output ratings 5.5 kW, 13.2A and input rating of 380-500V, is utilized without the CMI to compare the *dv/dt* rate of CMV of the inverters and investigate its effects on the CMC. The utilized inverters are shown in Figures 4.6 and 4.7. A three-phase induction motor with the parameters given in Appendix A is driven for all the experimental investigations in this thesis. The motor has been tested at no-load and at 50% load and it has been observed that loading has negligible effect on the CMV/CMC characteristics. In order to observe the motor phase current ripple clearly, only the no-load operating condition performance results are reported. The control algorithm is constant *V/f* method (176.7V_{rms} / 50Hz) since neither loading nor motion dynamics have noticeable effect on the CMV/CMC characteristics.

The experimental setup circuit diagram for the prototype two-level VSI is shown in Figure 4.8. The system is fed from the 400 V_{rms} line-to-line, 50 Hz power line. In order to measure the CMC values correctly, the motor is placed on an insulation base plate and a Y–Y transformer (1:1) is placed between the power line and the diode rectifier. With the neutral point of the transformer secondary connected to the chassis of the motor through a 1m-long cable, the cable current becomes the CMC (motor leakage current). Then the CMC is measured via a high bandwidth current transducer (Tektronix TCP312, DC-100 MHz, 30Apeak, with TCPA300 amplifier). Also the CMVs are measured with a high bandwidth differential voltage probe (LeCroy ADP305, 1000 V, 100 MHz). In order to measure the CMV at the inverter output, a virtual star point is created by a star connected resistor (30 kΩ) network at

the inverter output. The potential difference between the star point (*r*) and DC bus midpoint (*o*) becomes the inverter output CMV which will be symbolized with CMV_{ro}. The CMV at the motor neutral point (v_{no}) which will be symbolized with CMV_{no} is also measured. To make a fair comparison, the DC bus voltage of all the three inverters is set as 500V. A LeCroy Waverunner 6050A oscilloscope (500 MHz bandwidth) and a Tektronix TPS 2024 oscilloscope (200 MHz bandwidth) are utilized for the oscillograms. A DSP (TMS320F2808) is utilized to control the inverter and program the PWM signals. The more detailed information about the experimental setup is given in [56]. The laboratory experimental setup is shown in Figure 4.9.

The prototype two-level VSI operates at 6.6 kHz for the SVPWM, AZSPWM1, AZSPWM3, and RSPWM3 and at 10 kHz for DPWM1 and NSPWM methods (to provide equal average switching frequency of 6.6 kHz in all). The commercial two-level VSI operates at 8 kHz, and utilizes SVPWM for $M_i \leq 0.51$ and DPWM-MIN [38] for $M_i \geq 0.51$. The operating frequency of the commercial three-level VSIs is 5 kHz (most suitable available frequency of the commercial drive for comparison with the two-level VSI). The three-level NPC-VSI utilizes the Nearest Triangle Vector (NTV) PWM method which is described in Section 3.4.2.2.

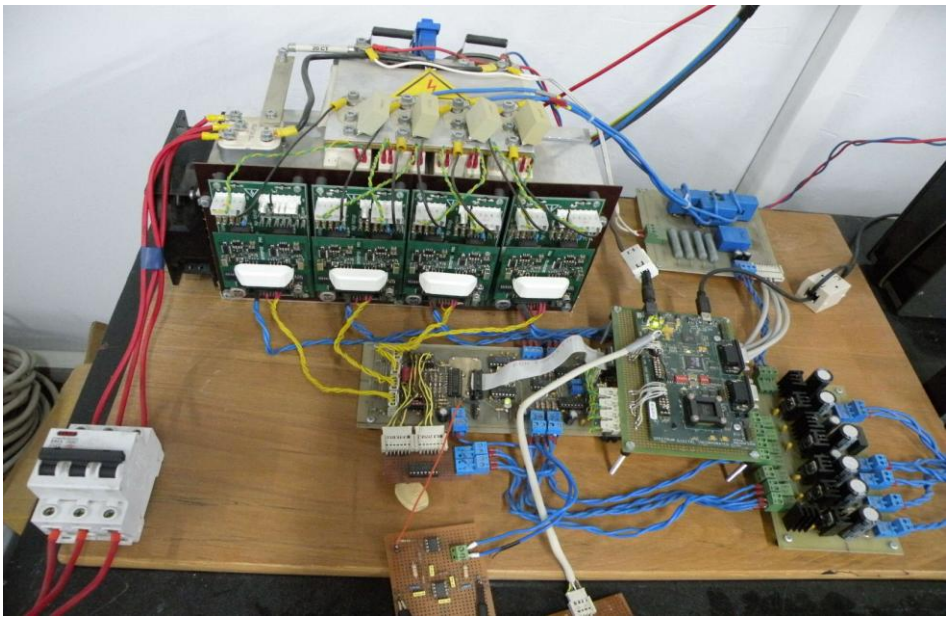
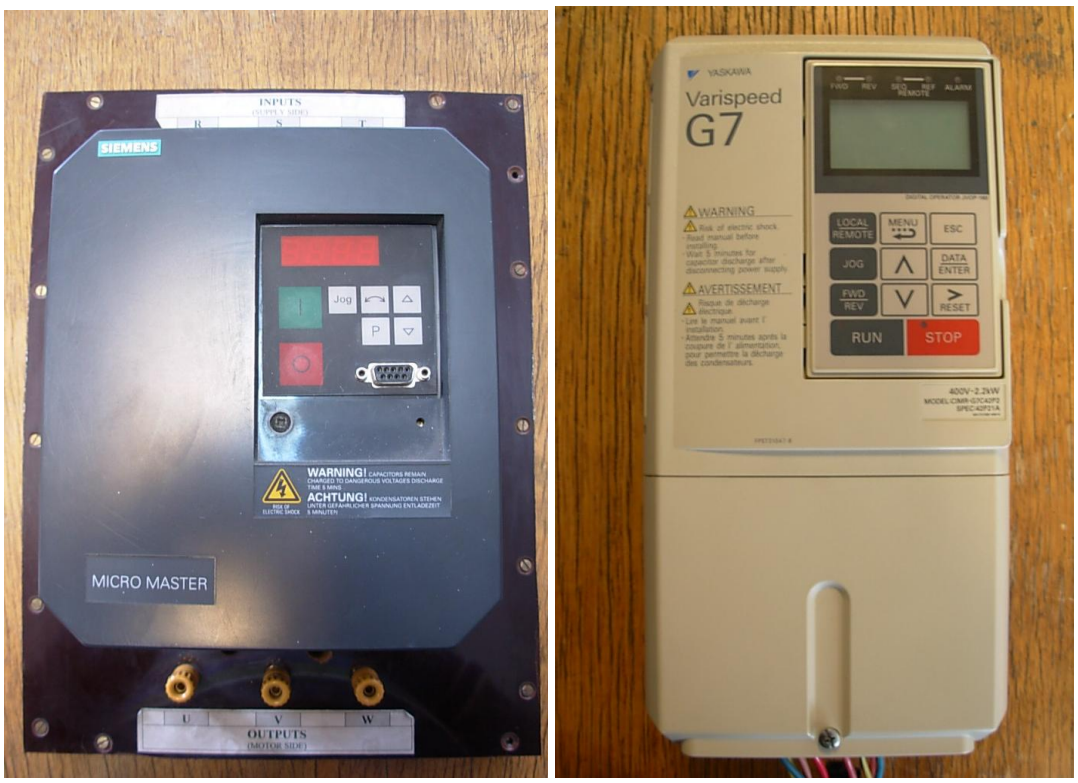


Figure 4.6 The prototype two-level VSI.



(a) (b)

Figure 4.7 The commercial VSIs utilized in this thesis; (a) standard two-level VSI, (b) three-level NPC-VSI.

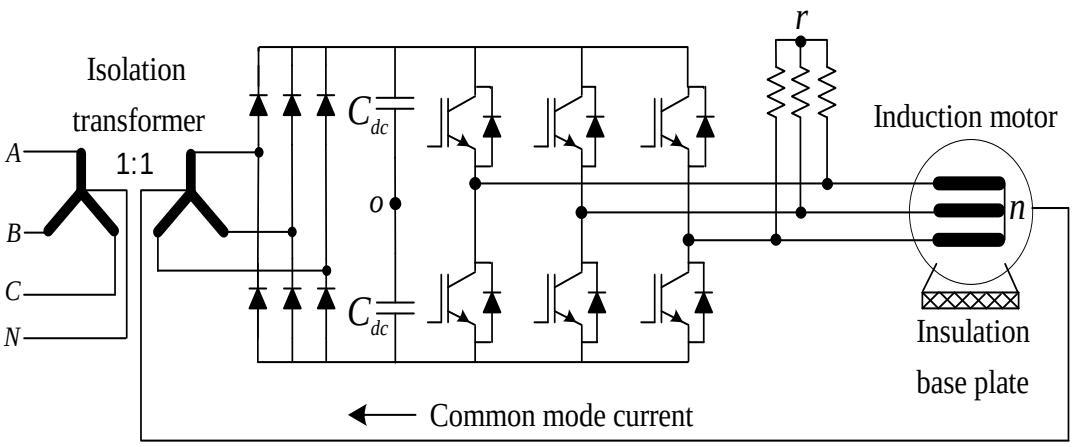


Figure 4.8 The experimental setup circuit diagram.

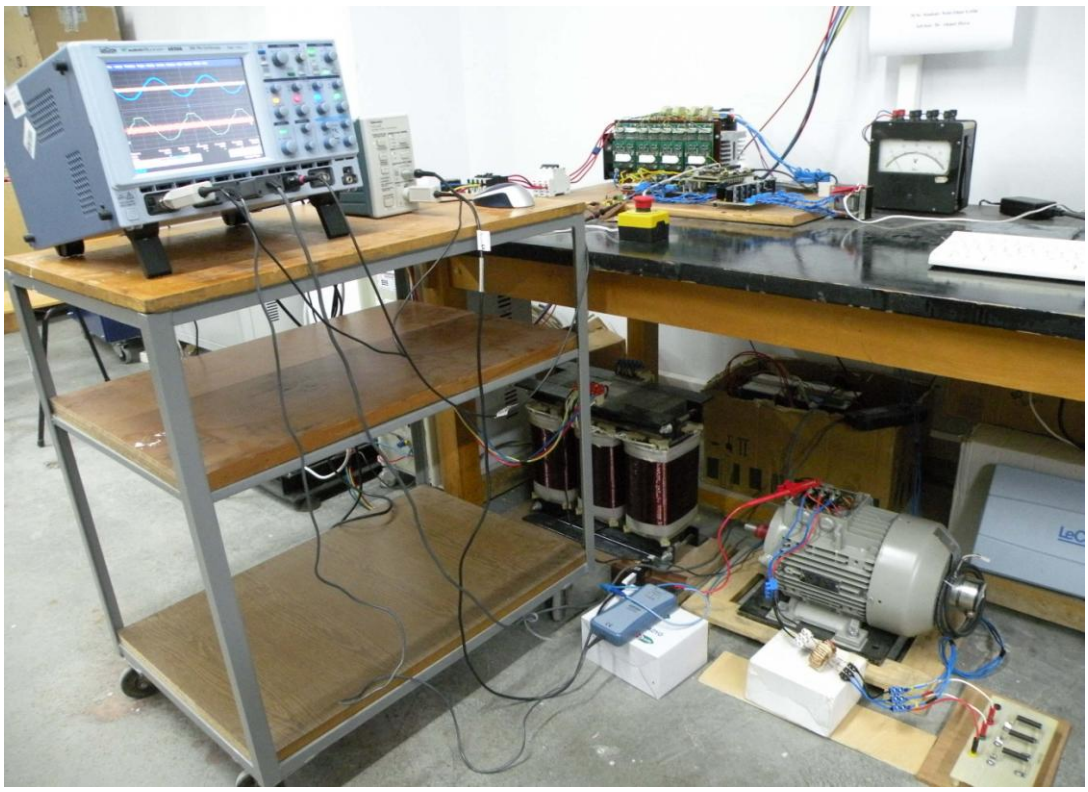


Figure 4.9 The laboratory experimental setup.

4.4.2 CMV/CMC Measurements Under Floating and Grounded Motor Chassis Conditions

The CMV_{ro}, the CMV_{no}, and the CMC waveforms under floating and grounded motor chassis conditions are illustrated in Figure 4.10 for the two-level VSI with SVPWM and AZSPWM1, and the NPC-VSI to demonstrate the effect of the motor drive parasitic capacitances. In the floating chassis case the CMV_{no} waveforms are rectangular and similar to the CMV_{ro} and no CMC flows, as expected. The CMV change is $V_{dc}/3$ (83V) for the two-level VSI, and is $V_{dc}/6$ (41.5V) for the NPC-VSI. In the grounded chassis case, as shown in Figure 4.11, the CMV_{no} waveform is oscillatory and it reaches higher values than the CMV_{ro}, and a significant CMC flows. As seen, the shape of the CMC waveform is a damped oscillating current. The motor-inverter-based system model involves parasitic L-C components, and as the CMC flows, due to the parasitic component impedances, the CMV_{no} deviates from the rectangular shape.

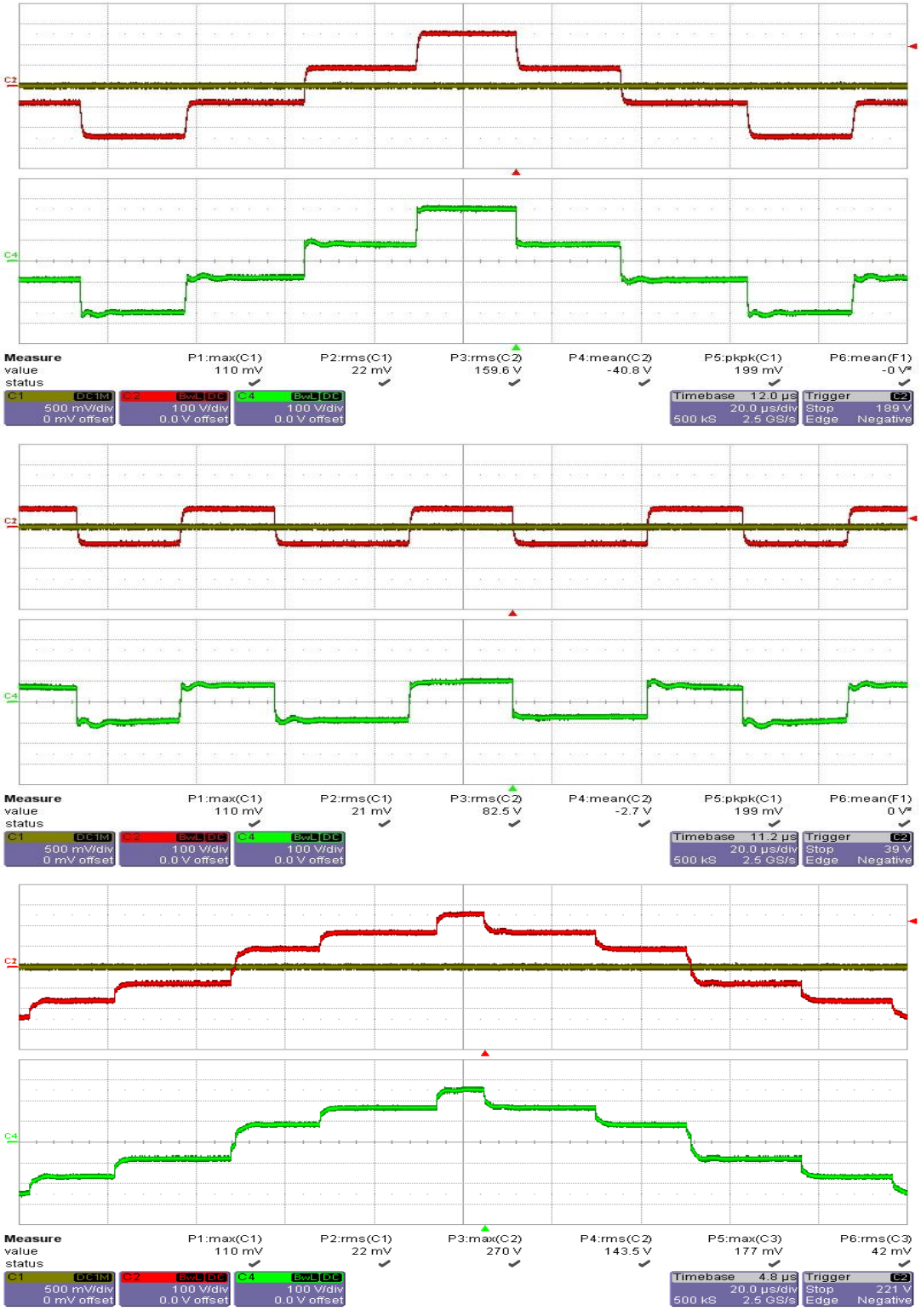


Figure 4.10 CMV_{ro}(red), CMV_{no} (green), and CMC (yellow) waveforms of SVPWM (top), AZSPWM1 (middle), and the NPC-VSI (bottom) for the motor chassis floating (scales: 500 mA/div, 100 V/div, 20 µs/div).

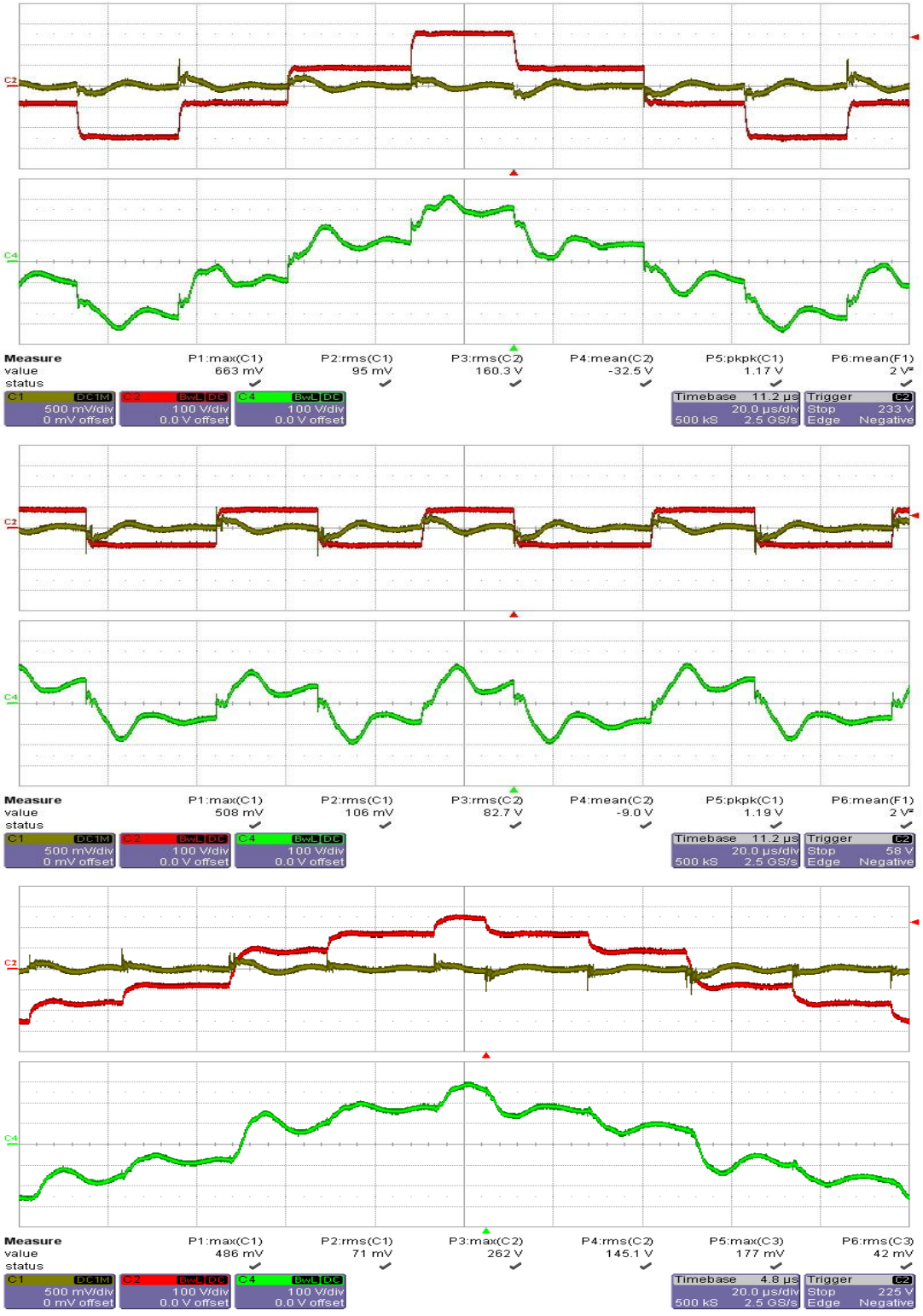


Figure 4.11 CMV_{ro}(red), CMV_{no} (green), and CMC (yellow) waveforms of SVPWM (upper), AZSPWM1 (middle), and the NPC-VSI (bottom) for the motor chassis grounded (scales: 500 mA/div, 100 V/div, 20 µs/div).

4.4.3 CMV/CMC Performance Evaluations Without the CMI

Figures 4.12-4.19 show the experimental two-level VSI and three-level NPC-VSI phase current, CMC, and CMV_{no} waveforms over a fundamental cycle without any CMI. The phase currents are sinusoidal, and the PWM current ripple is small and comparable both in the two-level VSI and the NPC-VSI. SVPWM and DPWM1 have high CMV. Of the RCMV-PWM methods, AZSPWM1 and NSPWM have low CMV. AZSPWM3 and RSPWM3 have high CMV compared to NSPWM and AZSPWM1 due to unexpected zero states discussed in chapter 2, but their CMV/CMC frequency is less than the other methods. The CMV of the NPC-VSI is similar to those of NSPWM and AZSPWM1 at high M_i where the inverter CMV_{ro} magnitude is $V_{dc}/3$, but it is noticeably higher at low M_i where the inverter CMV_{ro} magnitude is $V_{dc}/2$. Comparing the CMC characteristics, over a fundamental cycle the difference is not as noticeable as the CMV characteristic, because the *dv/dt* of CMV is the same in all methods in the two-level VSI. The CMC in the NPC-VSI is slightly less than the two-level VSI.

It is observed that the CMV/CMC characteristics do not change noticeably with M_i level for the two-level VSI. Thus, in the two-level VSI, only operation at one M_i point is discussed. In the NPC-VSI, since the magnitude and frequency of the CMV is different for $M_i<0.5$ and $M_i>0.5$, operations at $M_i=0.4$ and $M_i=0.8$ are discussed to show the effects of different CMV pulse patterns.

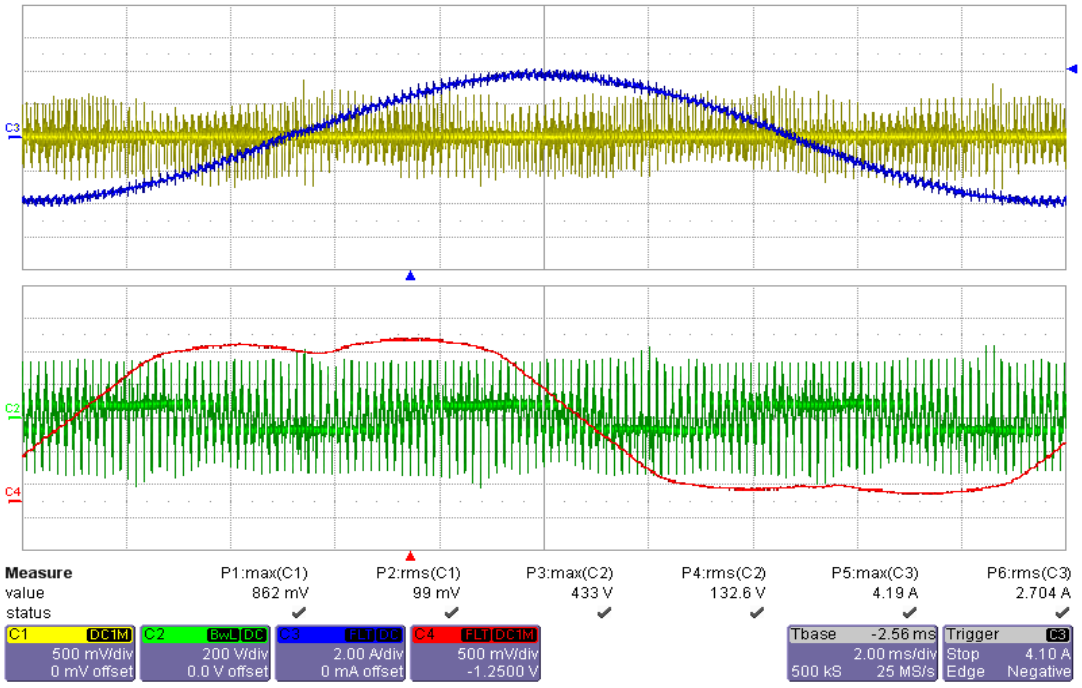


Figure 4.12 Phase current (blue), CMC (yellow), CMV_{no} (green), and modulation signal (red) waveforms for SVPWM (M_i=0.8 and f_s=6.6 kHz).

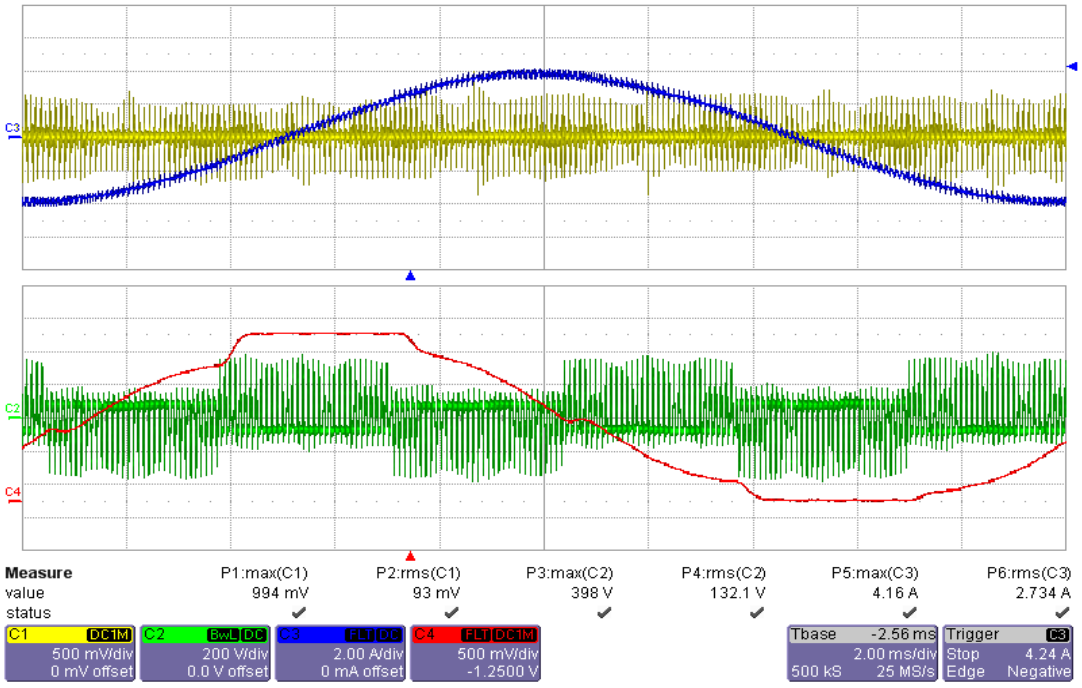


Figure 4.13 Phase current (blue), CMC (yellow), CMV_{no} (green), and modulation signal (red) waveforms for DPWM1 (M_i=0.8 and f_s=10 kHz).

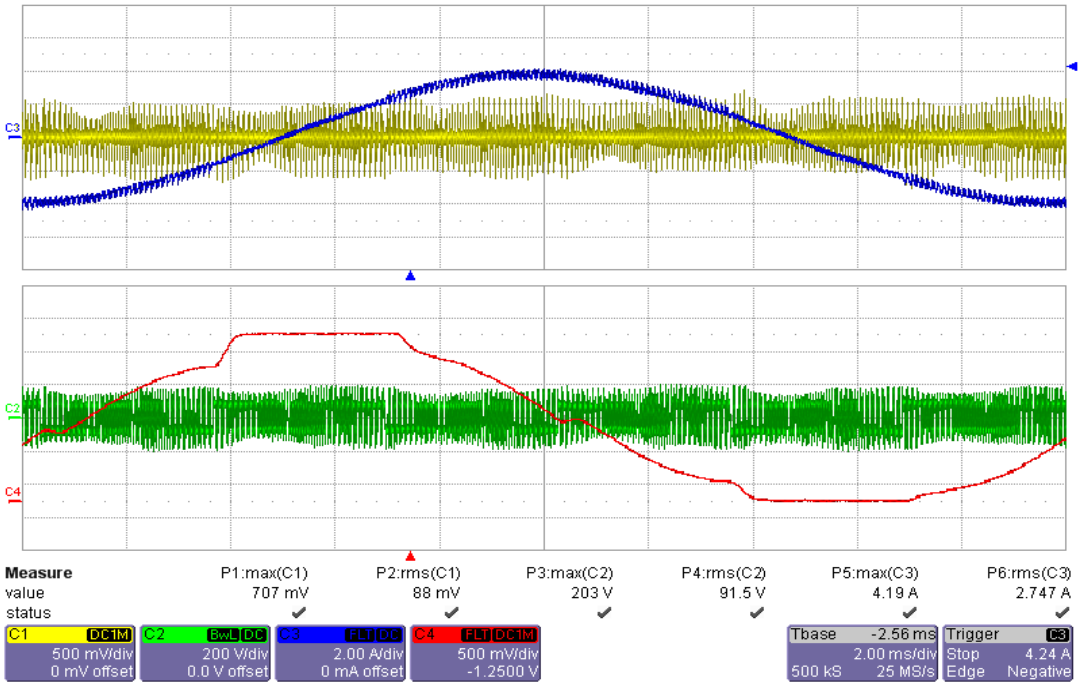


Figure 4.14 Phase current (blue), CMC (yellow), CMV_{no} (green), and modulation signal (red) waveforms for NSPWM (M_i=0.8 and f_s=10 kHz).

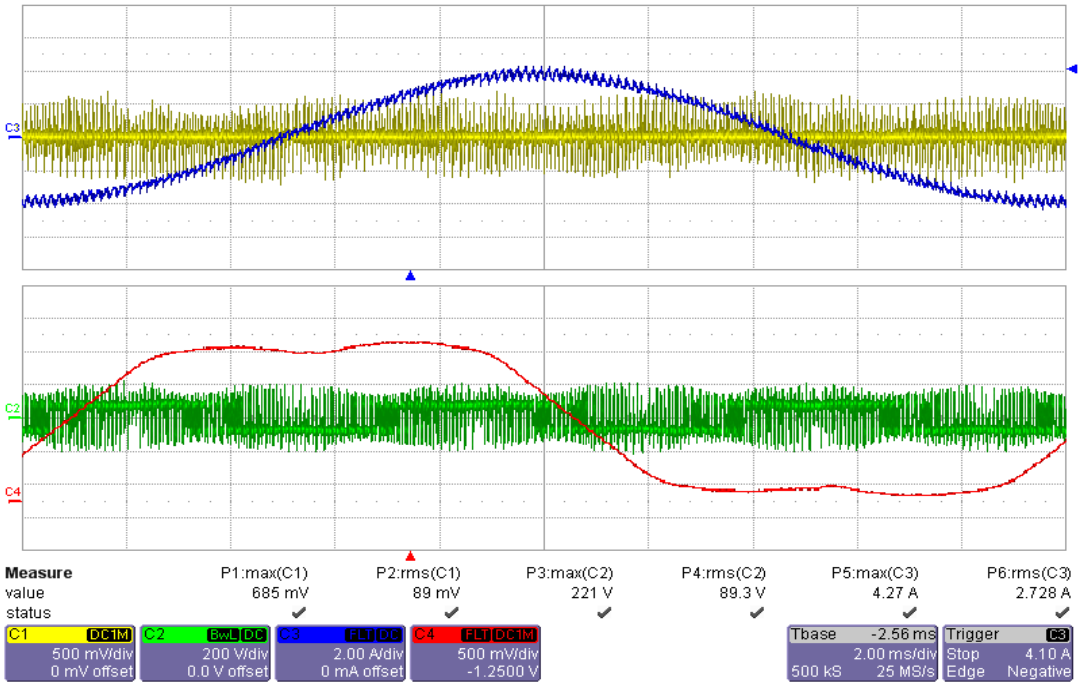


Figure 4.15 Phase current (blue), CMC (yellow), CMV_{no} (green), and modulation signal (red) waveforms for AZSPWM1 (M_i=0.8 and f_s=6.6 kHz).

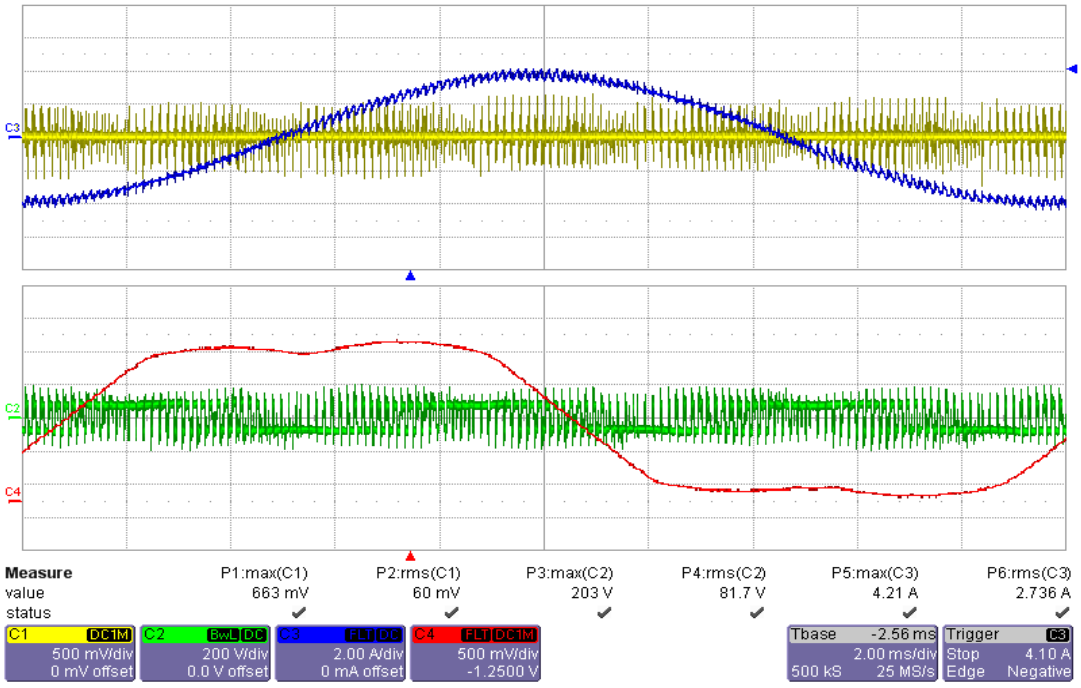


Figure 4.16 Phase current (blue), CMC (yellow), CMV_{no} (green), and modulation signal (red) waveforms for AZSPWM3 (M_i=0.8 and f_s=6.6 kHz).

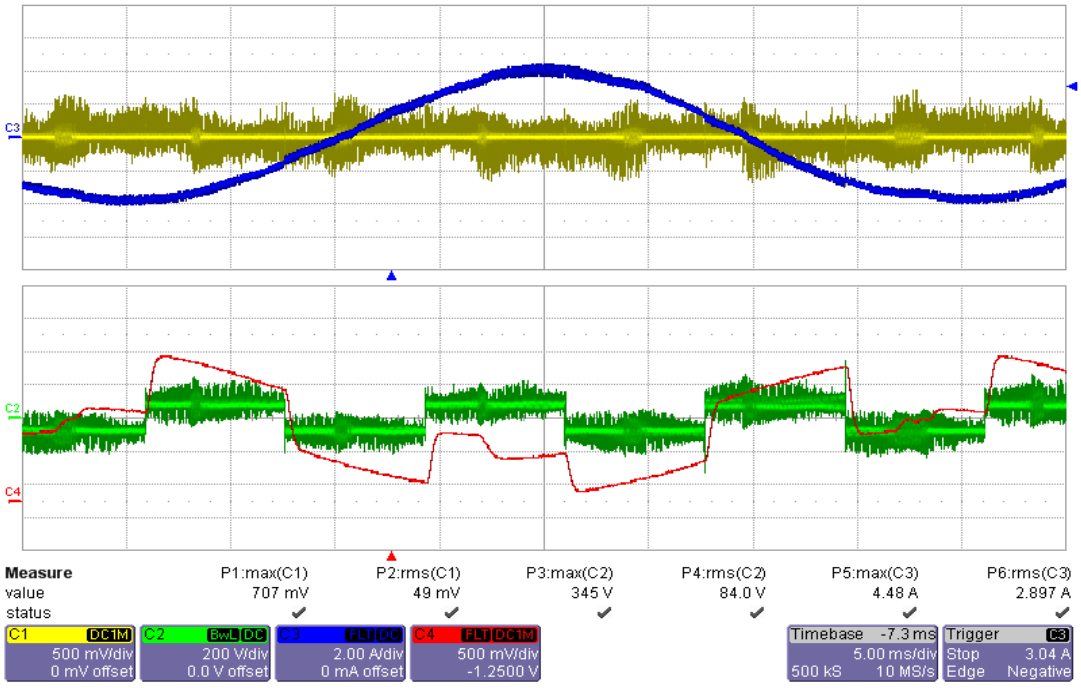


Figure 4.17 Phase current (blue), CMC (yellow), CMV_{no} (green), and modulation signal (red) waveforms for RSPWM3 (M_i=0.4 and f_s=10 kHz).

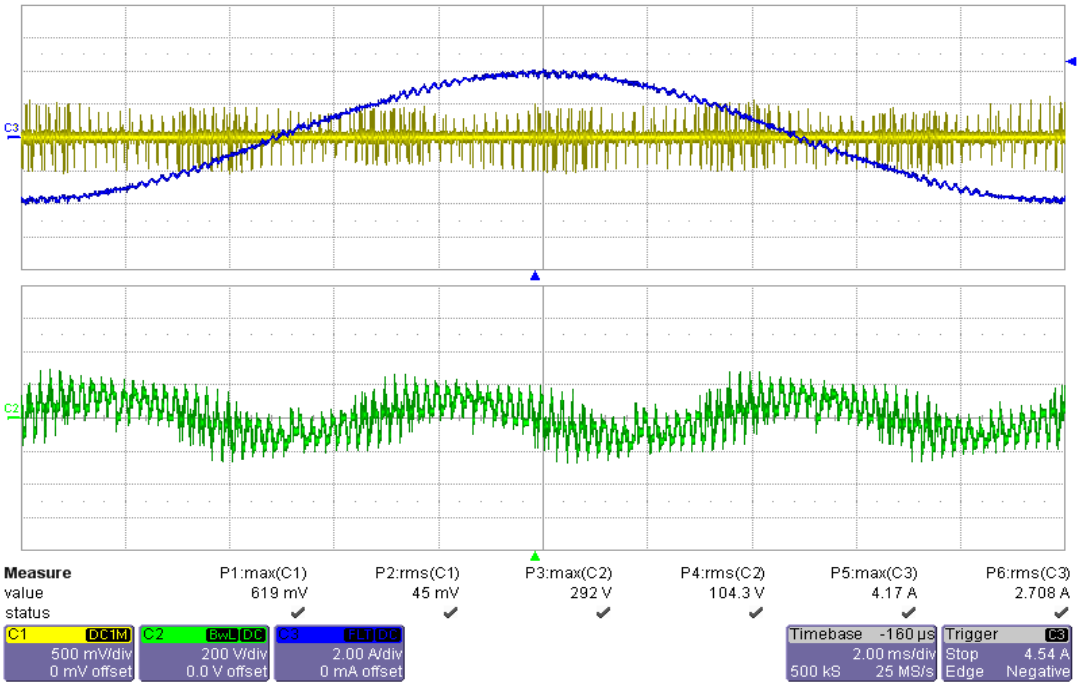


Figure 4.18 Phase current (blue), CMC (yellow), and CMV_{no} (green) waveforms for the NPC-VSI (M_i=0.8 and f_s=5 kHz).

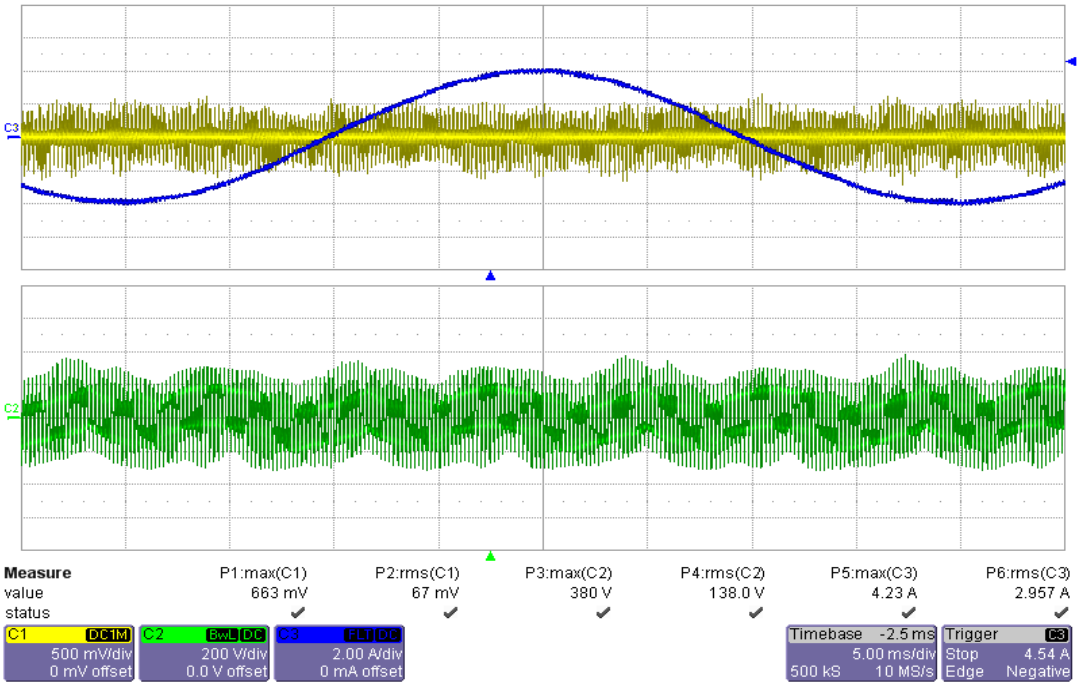


Figure 4.19 Phase current (blue), CMC (yellow), and CMV_{no} (green) waveforms for the NPC-VSI (M_i=0.4 and f_s=5 kHz).

Table 4.2 summarizes the peak and rms CMV/CMC results without the CMI. Since the PWM pulse pattern varies over a fundamental period, the CMV/CMC characteristics also vary in space. When comparing the peak CMV/CMC values, the worst CMV/CMC points are recorded for each method. The CMV/CMC rms values are recorded over a fundamental cycle.

The CMV comparison indicates that the two-level VSI with SVPWM and DPWM1 have high peak CMV. While the maximum CMV_{ro} value is 250V in the conventional methods, and 83V in the RCMV-PWM methods, CMV_{no} reaches 451V in the conventional methods, and 210V-350V range in the RCMV- PWM methods due to the parasitic L-C oscillations in the motor (discussed in section 4.4.2). AZSPWM3 and RSPWM3 has high peak CMV (300V-350V) due to simultaneous switching problem. NSPWM and AZSPWM1 significantly reduce peak CMV (212V-230V range, approximately 50% of conventional methods). The NPC-VSI peak CMV is noticeably higher than the two-level VSI with the RCMV-PWM methods at low M_i (336V), but similar at high M_i (234V). RMCV-PWM methods have the lowest rms CMV values (85V-90V range).

The CMC comparison indicates that the peak and rms CMC values of the two-level VSI with the RCMV-PWM methods are partially decreased compared to conventional methods (approximately 10-30%). NSPWM and AZSPWM1 have the lowest peak CMC. However, the CMC reduction is not as significant as the CMV reduction since the *dv/dt* of CMV_{ro} is the same in the two-level VSI regardless of the PWM method. The peak CMC values of AZSPWM3, RSPWM3 and the NPC-VSI are comparable to those of the conventional methods. The rms CMC values of RSPWM3 and the NPC-VSI at high M_i are significantly lower than the others.

According to the above experimental investigations, of the RCMV-PWM methods, NSPWM and AZSPWM1 significantly reduce the CMV and partially reduce the CMC. AZSPWM3 and RSPWM3 are poor at reducing peak CMV/CMC. Thus, the remainder of the chapter will focus on the two successful RCMV-PWM methods, NSPWM and AZSPWM1. In the NPC-VSI typical peak CMC values in one

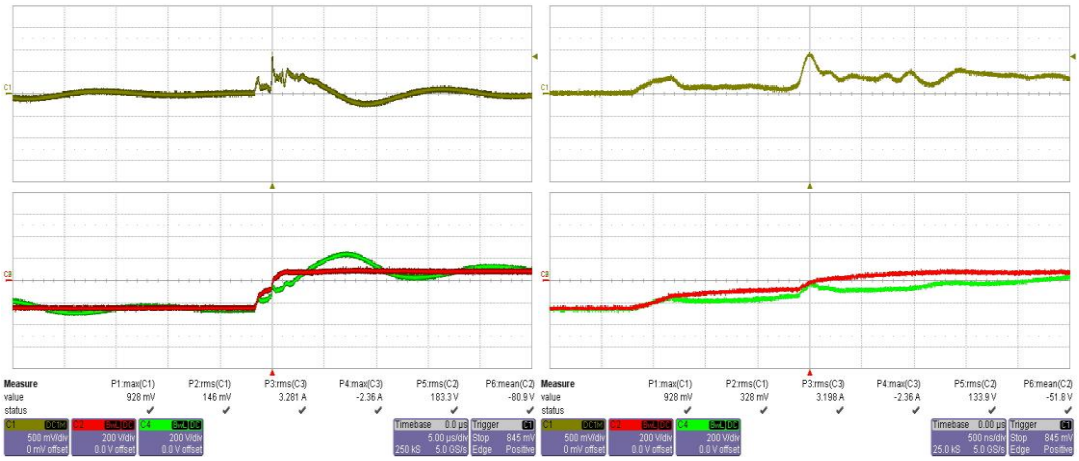
fundamental period are less than the two-level VSI due to the reduction of *dv/dt* of the CMV, but the worst peak CMC is similar to the two-level VSI with conventional methods. In the following, the worst case peak CMC values and the effects of the *dv/dt* and the magnitude of the CMV on the CMC will be investigated.

Table 4.2 CMV and CMC results without the CMI

	M_i	CMV peak (V)	CMV rms (V)	CMC peak (A)	CMC rms (mA)
SVPWM	0.8	451	130	1.1	98
DPWM1		451	131	1.1	93
NSPWM		212	90	0.773	83
AZSPWM1		230	88	0.773	86
AZSPWM3		301	85	0.906	60
RSPWM3	0.4	354	85	0.950	49
NPC-VSI	0.8	234	105.4	1.02	43
	0.4	336	156.7	0.994	66

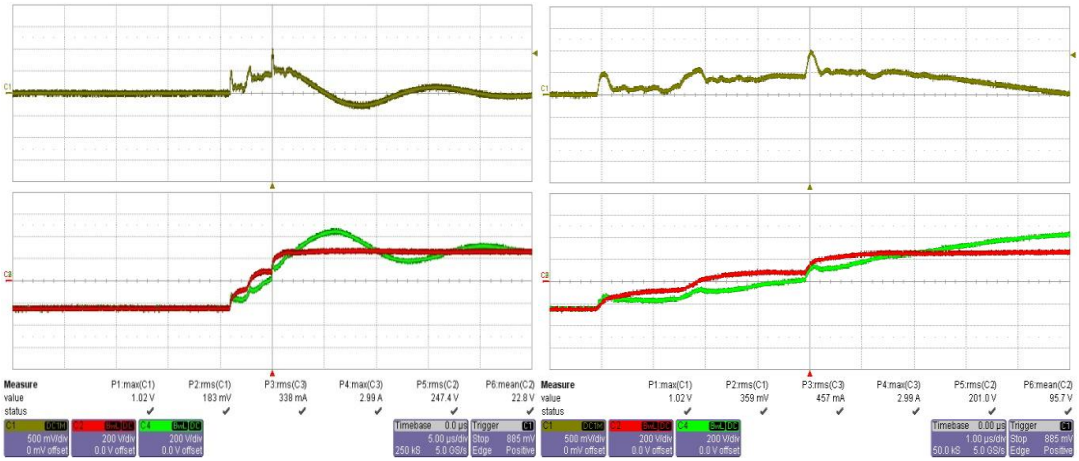
4.4.3.1 The Worst Case Peak CMC Measurements

In Figures 4.20-4.24, the worst peak CMC waveforms (as given in Table 4.2) are shown. The worst peak CMCs occur when a switching occurs while CMC initiated by the previous one is still oscillating. As seen in Figures 4.20, in SVPWM and DPWM1, two consecutive CMV changes which occur at every 60° region boundaries, increase peak CMC up to 1.1A. In Figure 4.21, three consecutive CMV changes with short time intervals which occur at very low M_i, increase peak CMC up to 1.33A in SVPWM.



(a) (b)

Figure 4.20 Worst peak CMC case for SVPWM and DPWM1 at 60° region boundaries, CMC (yellow, 500mA/div), CMV_{ro} (red, 200V/div), and CMV_{no} (green, 200V/div) waveforms, time scales (a) 5us/div, (b) 500ns/div.

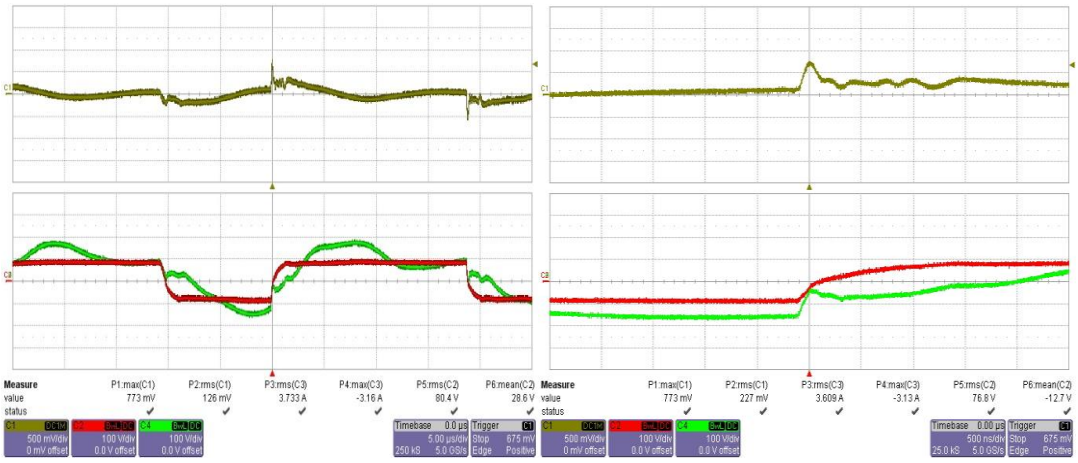


(a) (b)

Figure 4.21 Worst peak CMC case for SVPWM at M_i=0.05, CMC (yellow, 500mA/div), CMV_{ro} (red, 200V/div), and CMV_{no} (green, 200V/div) waveforms, time scales (a) 5us/div, (b) 1us/div.

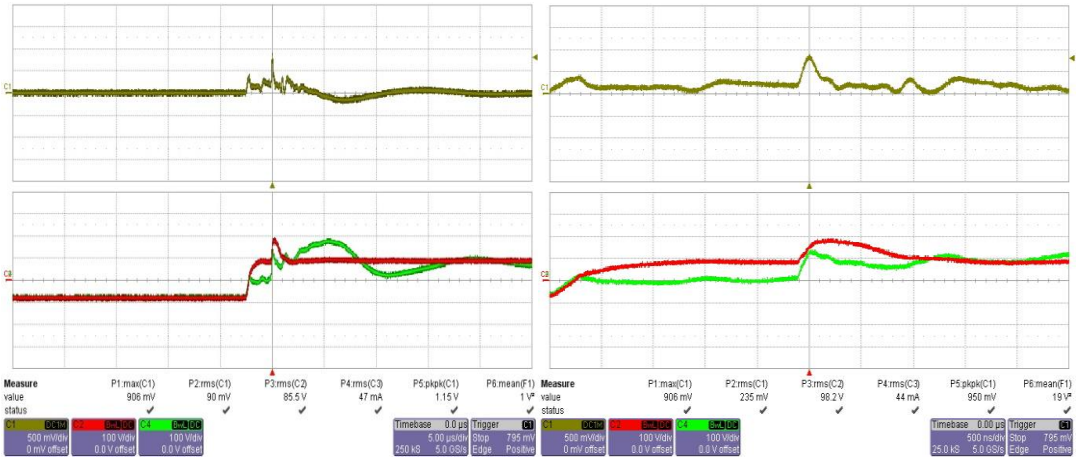
In Figures 4.22 and 4.23 the peak CMC waveforms for the RCMV-PWM methods are shown. In NSPWM and AZSPWM1, the CMC waveforms are almost identical and the peak values are the same. Therefore, only the waveforms for NSPWM are shown in Figure 4.22. The peak CMC is 0.773A in worst case. Note that in this

case, the consecutive CMV changes are always in reverse direction, thus worst peak CMC is lower than that in conventional methods. In AZSPWM3 and RSPWM3, as shown in Figure 4.23, the peak CMC is higher (0.9A) in worst case since the unexpected zero states cause a CMV of $V_{dc}/2$. Shown in Figure 4.24, in the NPC-VSI the peak CMC reaches 1A in the worst case when two CMV changes occur with very short time interval.



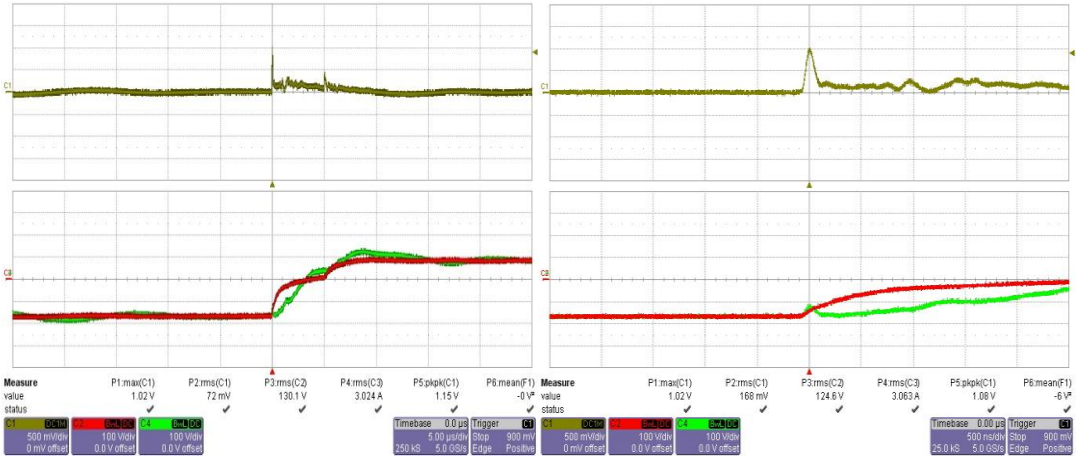
(a) (b)

Figure 4.22 Worst peak CMC case for NSPWM and AZSPWM1, CMC (yellow, 500mA/div), CMV_{ro} (red, 100V/div) and CMV_{no} (green, 100V/div) waveforms, time scales (a) 5us/div, (b) 500ns/div.



(a) (b)

Figure 4.23 Worst peak CMC case for AZSPWM3 and RSPWM3, CMC (yellow, 500mA/div), CMV_{ro} (red, 100V/div) and CMV_{no} (green, 100V/div) waveforms, time scales (a) 5us/div, (b) 500ns/div.



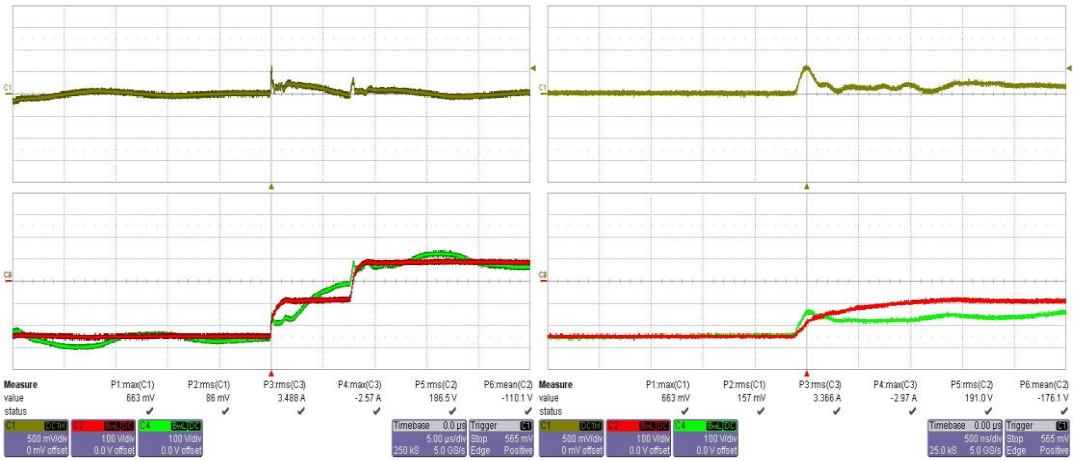
(a) (b)

Figure 4.24 Worst peak CMC case for NPC-VSI, CMC (yellow, 500mA/div), CMV_{ro} (red, 100V/div) and CMV_{no} (green, 100V/div) waveforms, time scales (a) 5us/div, (b) 500ns/div.

4.4.3.2 The Effects of *dv/dt* and Magnitude of CMV on The Peak CMC

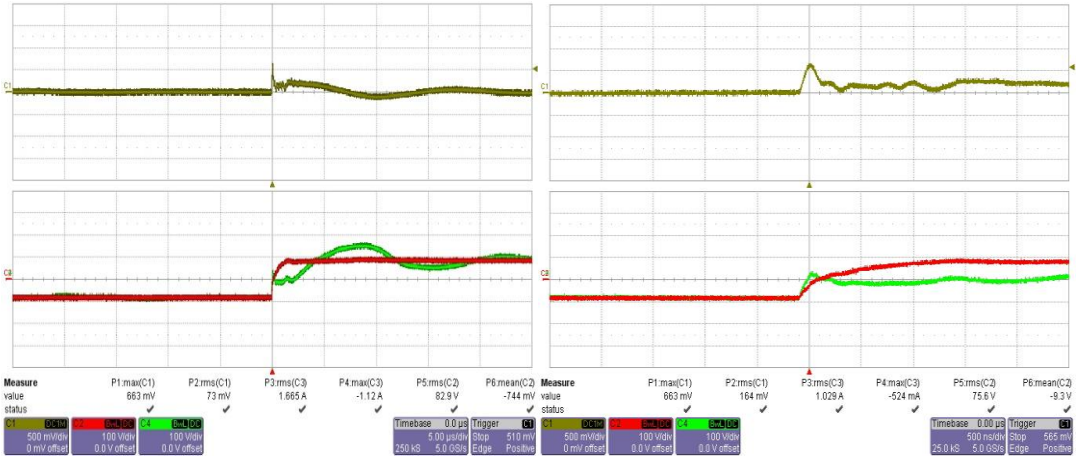
In this section, the effects of the CMV changes on the peak CMC are discussed. In Figures 4.25-4.27, the CMCs caused by single CMV change at different CMV magnitudes are shown for SVPWM with the two-level VSI. In order to observe the effect of single CMV change, the cases in which CMCs are damped before the switching occurs (typical CMC values), are selected. The three CMCs have the same peak value (663mA), and it is observed that they vary in 609mA-683mA range at three CMV changes at different magnitudes. The measurements for the other PWM methods in the two-level VSI are also similar, thus they are not shown for the sake of brevity. In Figure 4.28, the CMC caused by single CMV change in the NPC-VSI is shown. In this case the typical peak CMC value is 508mA and it varies in 450mA-550mA range, and it is similar in all CMV magnitudes. These observations indicate that the peak CMC value is mainly dependent of CMV changes at the switching instants. CMV changes at different magnitudes do not cause a noticeable difference in peak CMC.

The microscopic CMC experiments in sections 4.4.3.1 and 4.4.3.2 show that in the two-level VSI the typical peak CMC caused by single CMV change is similar in all PWM methods (in 609mA-683mA range) since the CMV *dv/dt* is the same. However, the worst case peak CMC noticeably changes with the CMV pulse pattern even the *dv/dt* is the same, due to the consecutive switchings with short time intervals. The worst peak CMC is reduced by about 30% with the RCMV-PWM methods compared to conventional methods (1.1A in conventional methods vs. 0.773A in RCMV methods). In the NPC-VSI, although the typical peak CMC caused by single CMV change is lower than the two-level VSI (508mA), in the worst case it is comparable to the two-level VSI with the conventional methods (1A).



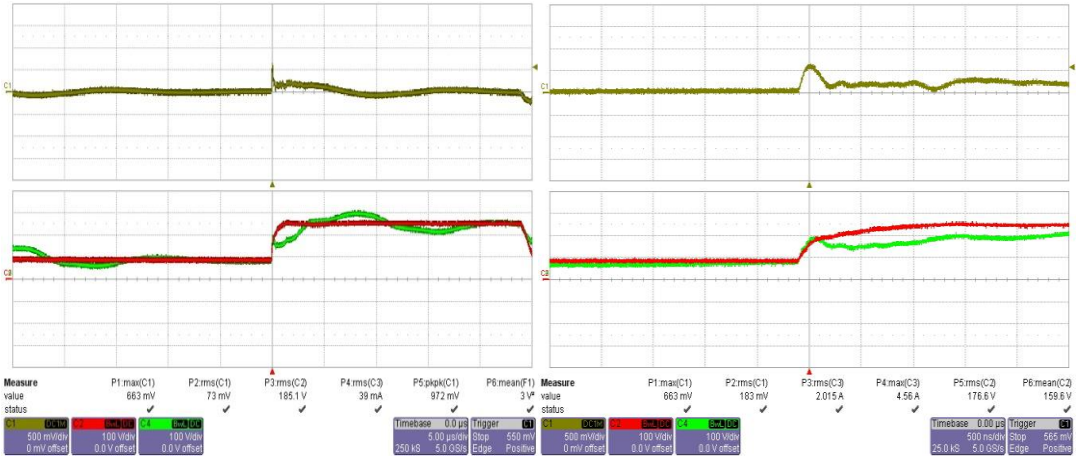
(a) (b)

Figure 4.25 Typical peak CMC (yellow, 500mA/div) waveforms for single CMV change for $-V_{dc}/2 \rightarrow -V_{dc}/6$ transition for the two-level VSI, CMV_{ro} (red, 100V/div), CMV_{no} (green, 100V/div), time scales (a) 5us/div, (b) 500ns/div.



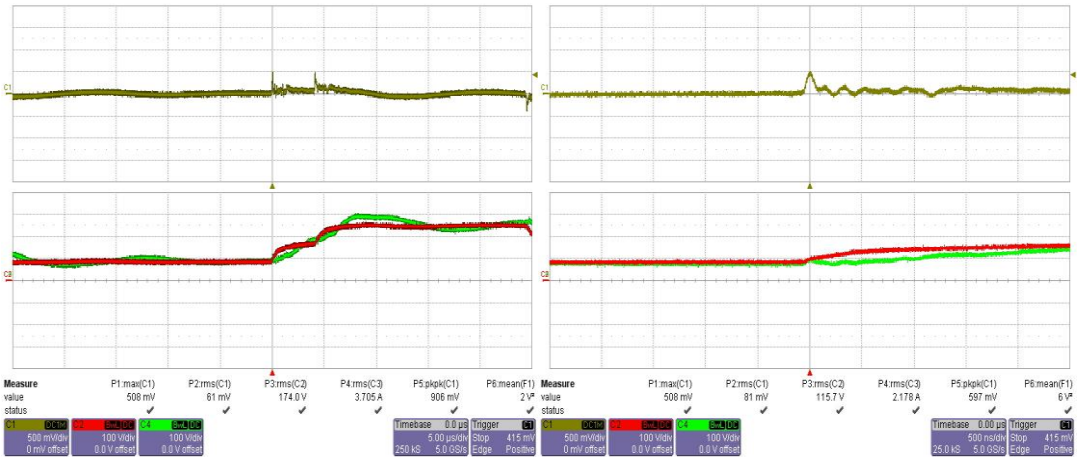
(a) (b)

Figure 4.26 Typical peak CMC (yellow, 500mA/div) waveforms for single CMV change for $-V_{dc}/6 \rightarrow V_{dc}/6$ transition for the two-level VSI, CMV_{ro} (red, 100V/div), CMV_{no} (green, 100V/div), time scales (a) 5us/div, (b) 500ns/div.



(a) (b)

Figure 4.27 Typical peak CMC (yellow, 500mA/div) waveforms for single CMV change for $V_{dc}/6 \rightarrow V_{dc}/2$ transition for the two-level VSI, CMV_{ro} (red, 100V/div), CMV_{no} (green, 100V/div), time scales (a) 5us/div, (b) 500ns/div.



(a) (b)

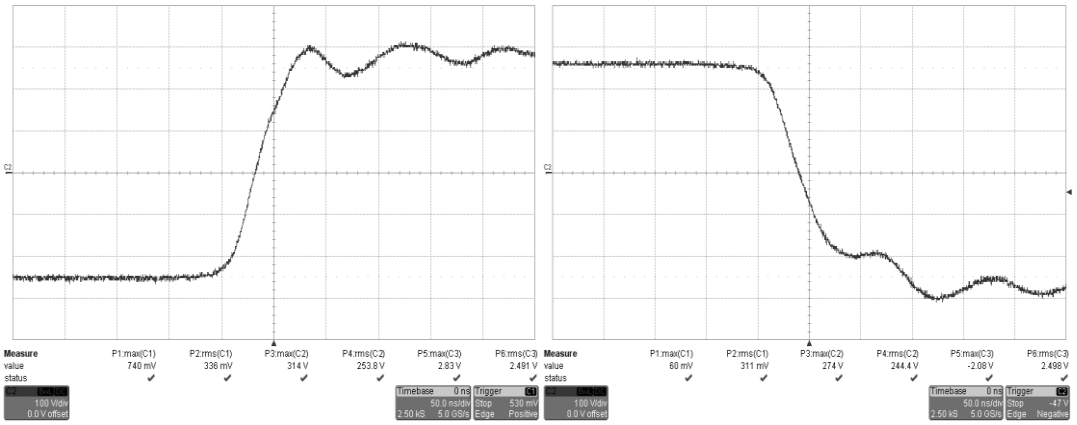
Figure 4.28 Typical peak CMC (yellow, 500mA/div) waveforms for single CMV change for $V_{dc}/6 \rightarrow V_{dc}/3$ transition for the NPC-VSI, CMV_{ro} (red, 100V/div), CMV_{no} (green, 100V/div), time scales (a) 5us/div, (b) 500ns/div.

4.4.3.3 Influence of The Different *dv/dt* Rates on The Peak CMC

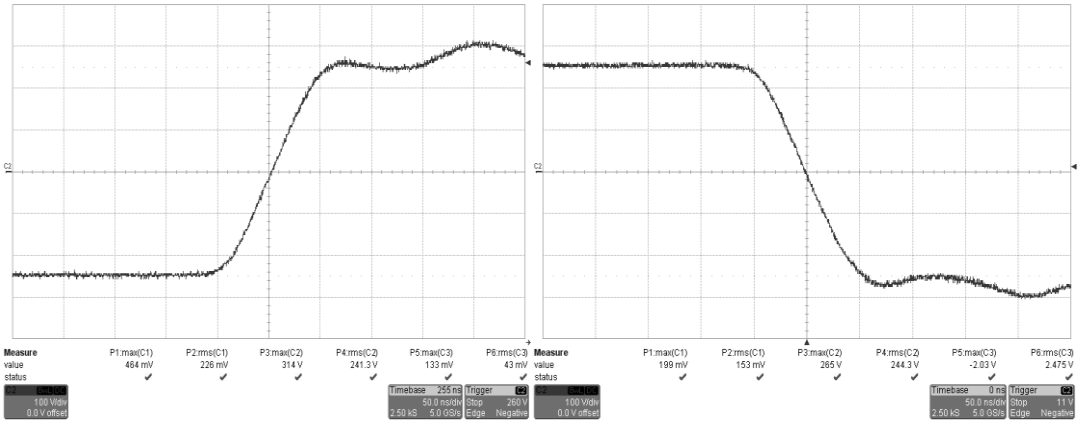
In order to discuss the effect of *dv/dt* of CMV on the peak CMC value, the *dv/dt* values of phase-to-midpoint output voltages (dv_{ph}/dt) of the three inverters are measured and typical CMC values caused by single CMV change are recorded. Table 4.3 shows the measured dv_{ph}/dt values of the inverters and typical peak CMC values caused by single CMV change. Figure 4.29 shows the phase-to-midpoint voltages during switch turn-on and turn-off. The measurements indicate that the peak CMC increases with increasing dv_{ph}/dt.

Table 4.3 Measured dv_{ph}/dt values and the peak CMCs of the inverters

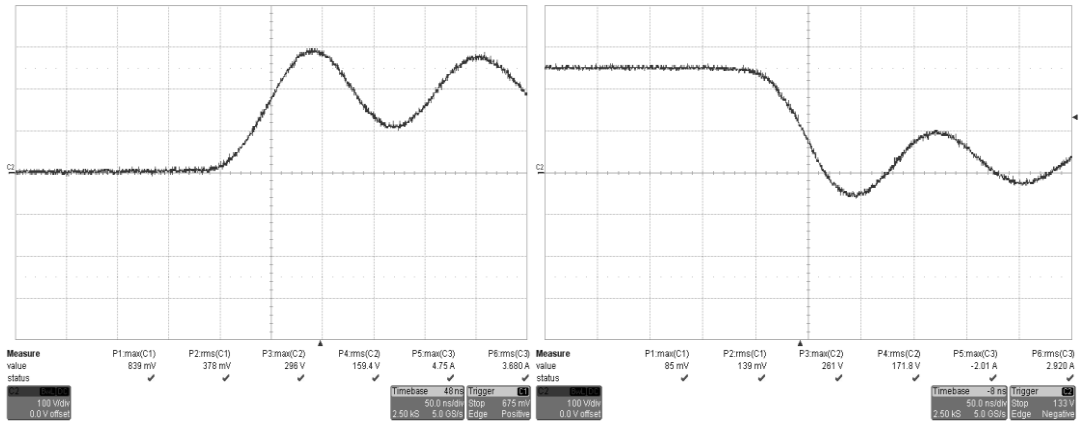
Inverter type	dv_{ph}/dt (kV/μs)	Typical peak CMC (A)
Commercial 2-level	6.66	0.862
Prototype 2-level	5.55	0.663
3-level NPC	4.16	0.508



(a)



(b)



(c)

Figure 4.29 Phase-to-midpoint output voltages (v_{ph}) of (a) commercial two-level (b) prototype two-level, (c) three-level NPC inverters (scales: 100V/div, 50ns/div).

The above CMV/CMC investigations indicate that the CMC is mainly dependent of the *dv/dt* of the CMV, and partially dependent of CMV pulse pattern. The RMCV-PWM methods reduce inverter CMV magnitude by 66% (from $V_{dc}/2$ to $V_{dc}/6$). However, peak CMC is reduced by approximately 30%, since the *dv/dt* of the CMV is the same. In the next section, CMV/CMC reduction performances of various CMIs are investigated.

4.4.4 CMV/CMC Performance Evaluations With The CMI

The experimental results in the previous section show that RCMV-PWM methods decrease CMV and CMC, but the performance improvement may not be sufficient in some applications. Therefore, utilization of passive filters is mandatory to meet a specified EMC performance in such applications. In this section CMV/CMC performances of the discussed PWM methods and inverters are investigated when the common mode inductor, which is a widely used passive common mode filtering method, is inserted between the inverter output terminals and the induction motor terminals. For this purpose five different CMIs whose properties are given in section 4.3 are evaluated. Of the two problematic PWM methods, only AZSPWM3 is considered, RSPWM3 is not included in these experiments.

Tables 4.4 and 4.5 summarize the CMV/CMC suppression performance of the considered CMIs. For CMI-1, CMI-2, and CMI-3, the peak and rms CMV values are similar to the case without a CMI. CMI-3 slightly suppresses the peak CMV due to its higher common mode inductance. For CMI-4 and CMI-5, there is a slight increase in the peak and rms CMV values because the low-loss cores of these CMIs cause the CMV to oscillate highly. From the measurements in Table 4.4 it can be concluded that the CMI does not provide an improvement in the motor CMV as explained in section 3.4.1.3.

As seen from the CMC measurements in Table 4.5, for the CMI-1, CMI-2, and CMI-3 the peak and the rms CMCs are significantly reduced. Commercial CMI-4

and CMI-5 enter magnetic saturation, and thus they are not as successful in suppressing the CMC as the other CMIs. Due to its low-loss characteristics, CMI-4 causes CMC to oscillate and does not provide an improvement in reducing the rms CMC. It causes even higher rms CMC values than the case without a CMI in NSPWM and AZSPWM1. CMI-5 highly saturates in SVPWM and DPWM1, and does not provide an improvement in reducing peak CMC in these methods. Therefore, the performance of three successful CMIs, CMI-1, CMI-2, and CMI-3, are investigated in detail.

When CMI-1 is utilized, the worst case peak CMCs are reduced by approximately 60%, and the rms CMCs are reduced by about 20-30% in the two-level VSI with all PWM methods and in the NPC-VSI. The two-level VSI with NSPWM and AZSPWM1, and the NPC-VSI provide the most significant improvement in peak CMC reduction (0.203A-0.256A range).

When CMI-2 is utilized, the worst case peak CMCs are reduced by 70-85%, and the rms CMCs are reduced by about 40-55% in the two-level VSI with all PWM methods and in the NPC-VSI. Again, the two-level VSI with NSPWM and AZSPWM1, and the NPC-VSI provide the most significant improvement in peak CMC reduction (0.115A-0.190A range).

When CMI-3 is utilized, the worst case peak CMCs are reduced by 80-86%, and the rms CMCs are reduced by about 40-60% in the two-level VSI with all PWM methods and in the NPC-VSI. NSPWM and AZSPWM1 provide the most significant improvement in peak CMC reduction (0.106A-0.115A range). It can be concluded that CMI-3 provides the best CMC suppression performance.

Figures 4.30-4.34 show the experimental phase current, CMC, and CMV waveforms for NSPWM over a fundamental cycle with the CMIs included for the same operating points as in the case without the CMI. As seen from these figures, the CMIs do not affect the phase currents since their normal mode inductance is nearly zero and they only provide common mode inductance. The CMV waveforms

are similar to the case without the CMI for CMI-1, CMI2, and CMI-3, and CMI-5. The CMV and CMC are slightly higher for CMI-4 due to the high oscillation. On the other hand, the CMC for the other CMIs decreases significantly (as numerically given in Table 4.5).

Figures 4.35-4.39 illustrate the worst case microscopic CMV/CMC waveforms for NSPWM. Note that, while the CMC is suppressed, its frequency is also reduced. CMI-4 has highly oscillatory CMV/CMC waveforms due to its low-loss characteristics. Figure 4.40 illustrates the magnetic core saturation for CMI-5 for SVPWM. Note that the CMC reaches nearly 1A in this case.

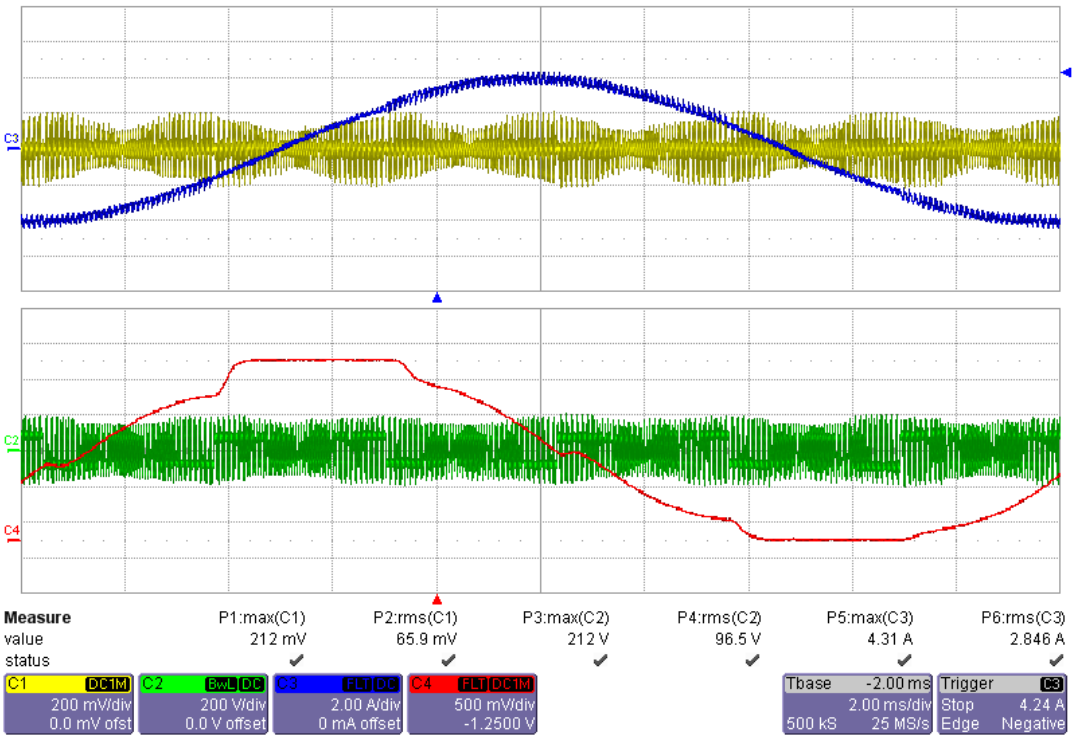


Figure 4.30 Two-level VSI phase current (blue, 2A/div), CMC (yellow, 200mA/div), CMV (green, 200V/div), and modulation signal (red, 500mV/div) waveforms for NSPWM with CMI-1.

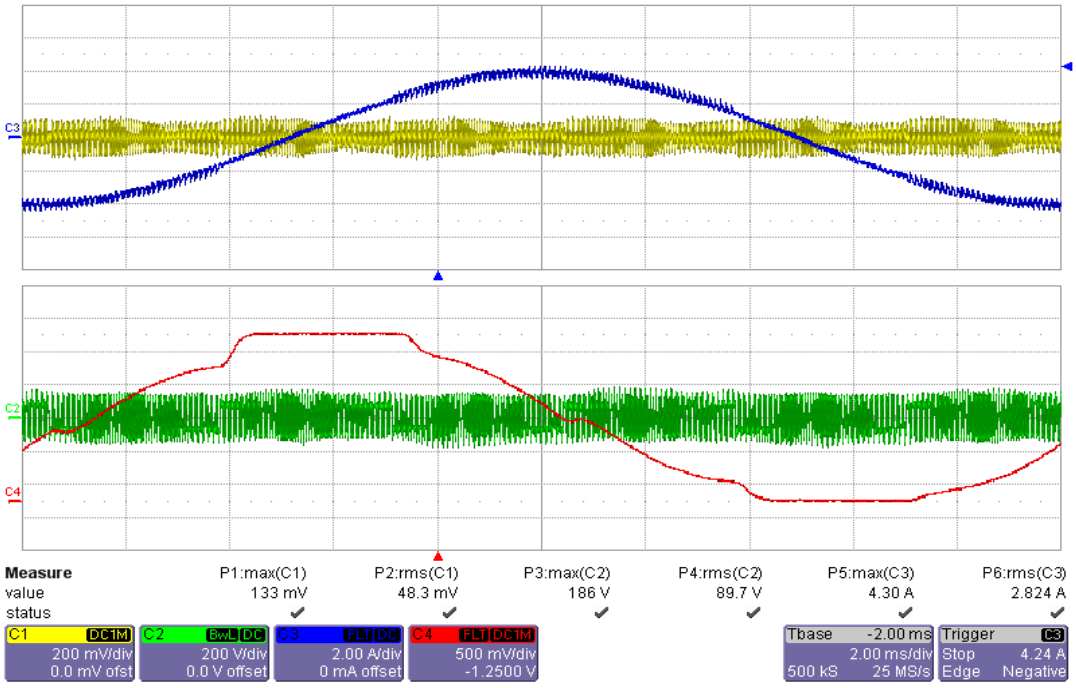


Figure 4.31 Two-level VSI phase current (blue, 2A/div), CMC (yellow, 200mA/div), CMV (green, 200V/div), and modulation signal (red, 500mV/div) waveforms for NSPWM with CMI-2.

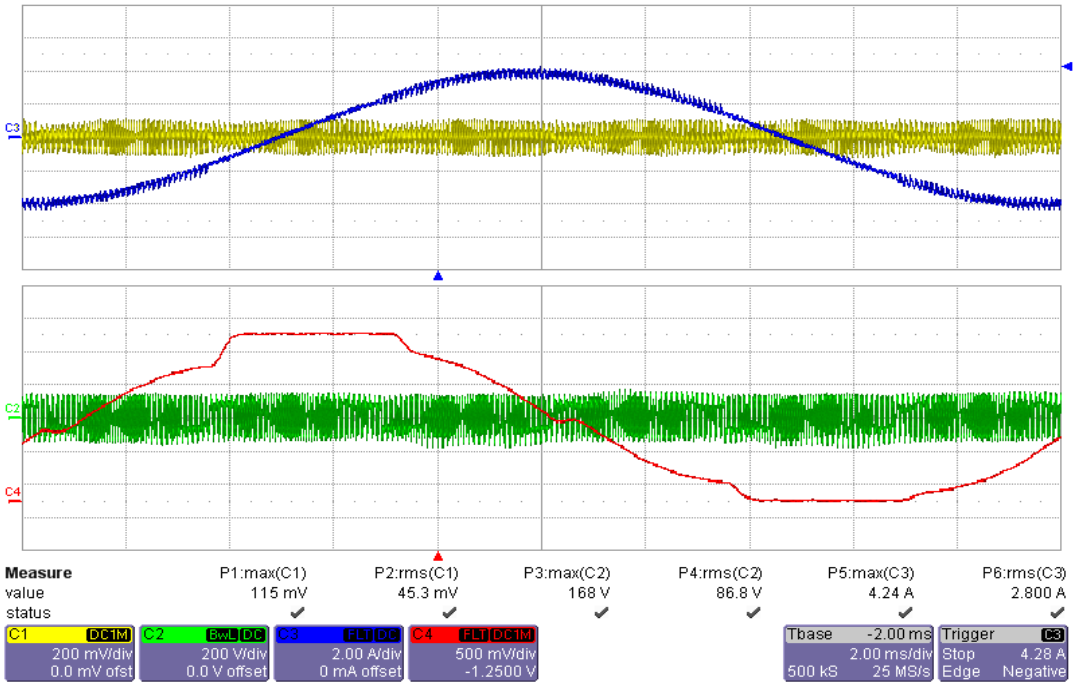


Figure 4.32 Two-level VSI phase current (blue, 2A/div), CMC (yellow, 200mA/div), CMV (green, 200V/div), and modulation signal (red, 500mV/div) waveforms for NSPWM with CMI-3.

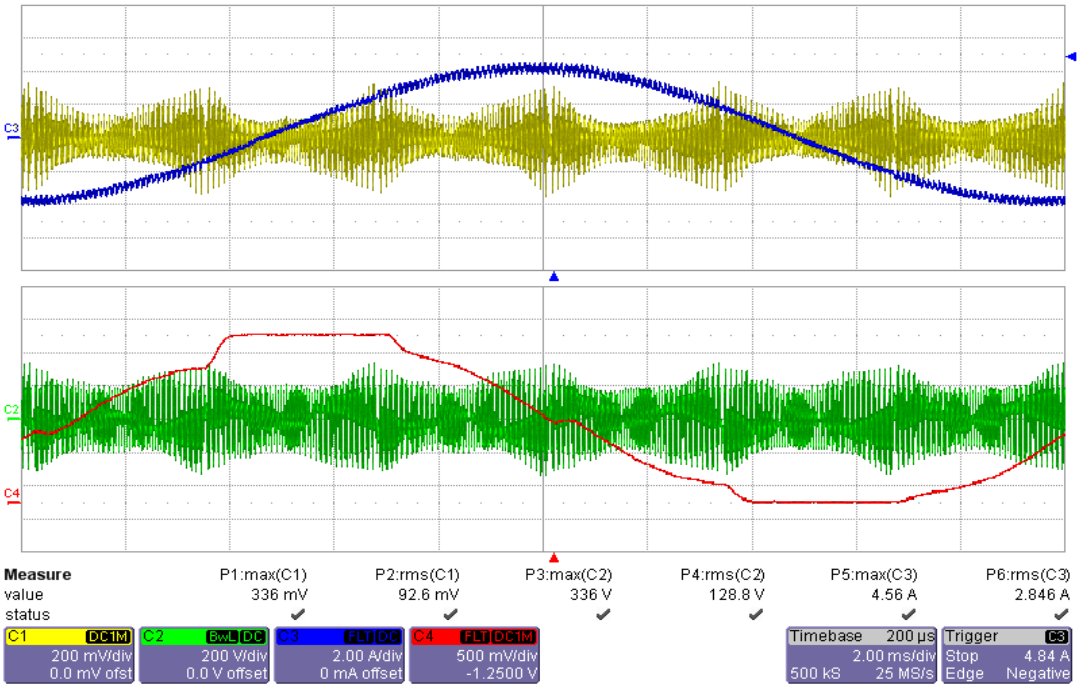


Figure 4.33 Two-level VSI phase current (blue, 2A/div), CMC (yellow, 200mA/div), CMV (green, 200V/div), and modulation signal (red, 500mV/div) waveforms for NSPWM with CMI-4.

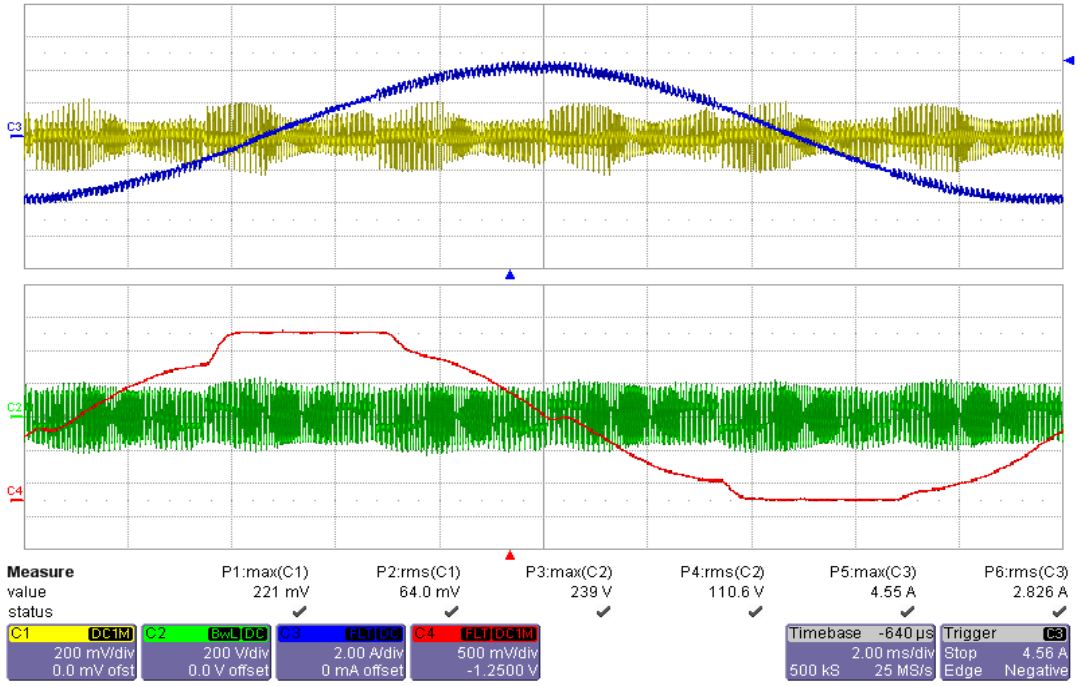


Figure 4.34 Two-level VSI phase current (blue, 2A/div), CMC (yellow, 200mA/div), CMV (green, 200V/div), and modulation signal (red, 500mV/div) waveforms for NSPWM with CMI-5.

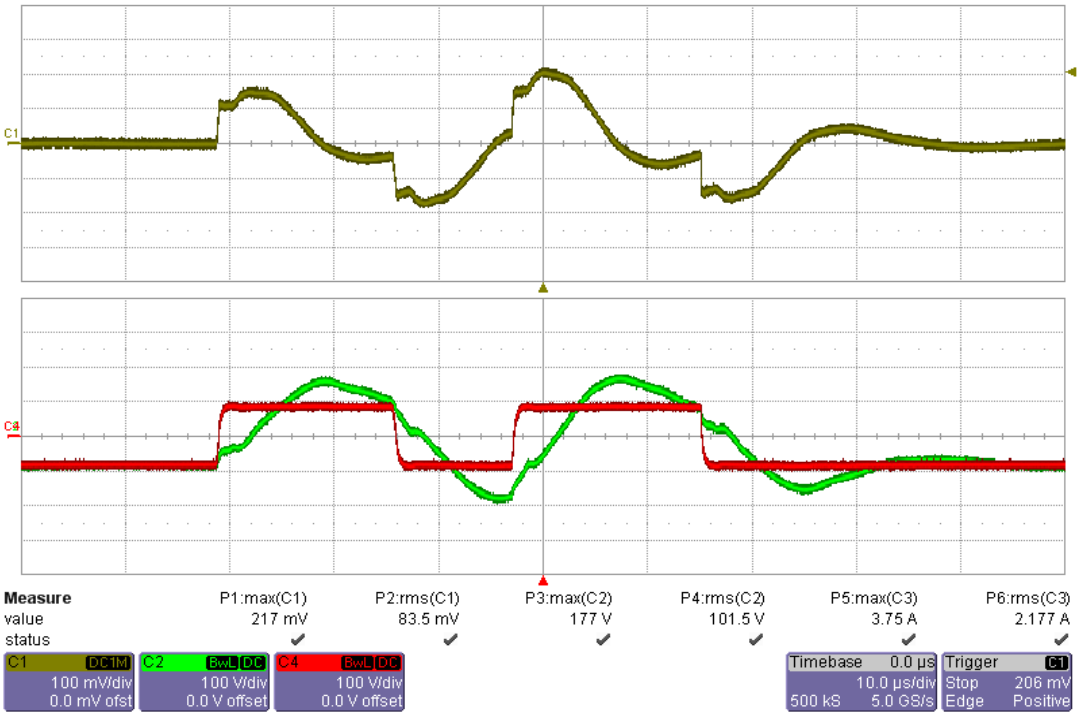


Figure 4.35 Microscopic CMC (yellow, 100mA/div), CMV_{ro} (red, 100V/div), CMV_{no} (green, 100V/div) waveforms for NSPWM with CMI-1.

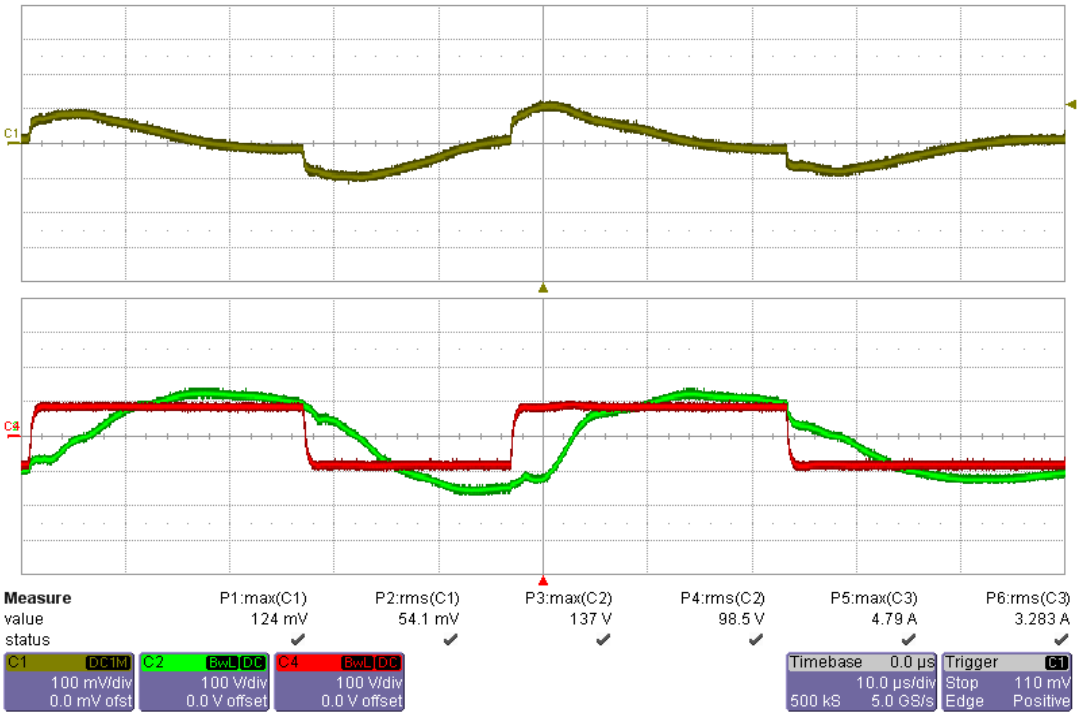


Figure 4.36 Microscopic CMC (yellow, 100mA/div), CMV_{ro} (red, 100V/div), CMV_{no} (green, 100V/div) waveforms for NSPWM with CMI-2.

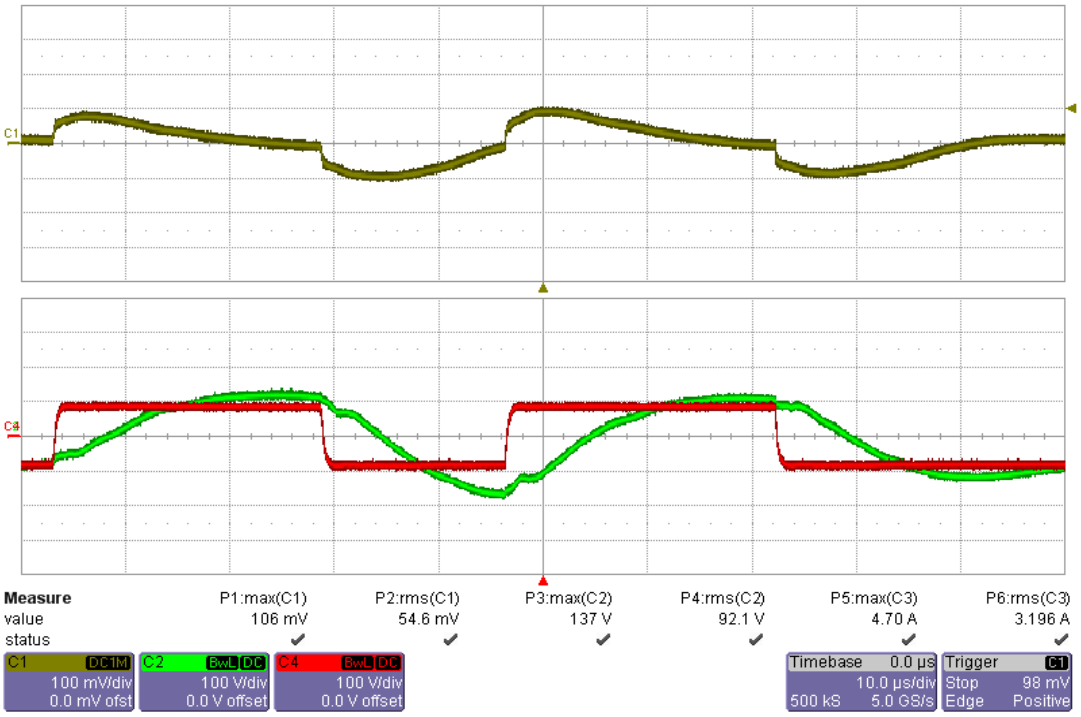


Figure 4.37 Microscopic CMC (yellow, 100mA/div), CMV_{ro} (red, 100V/div), CMV_{no} (green, 100V/div) waveforms for NSPWM with CMI-3.

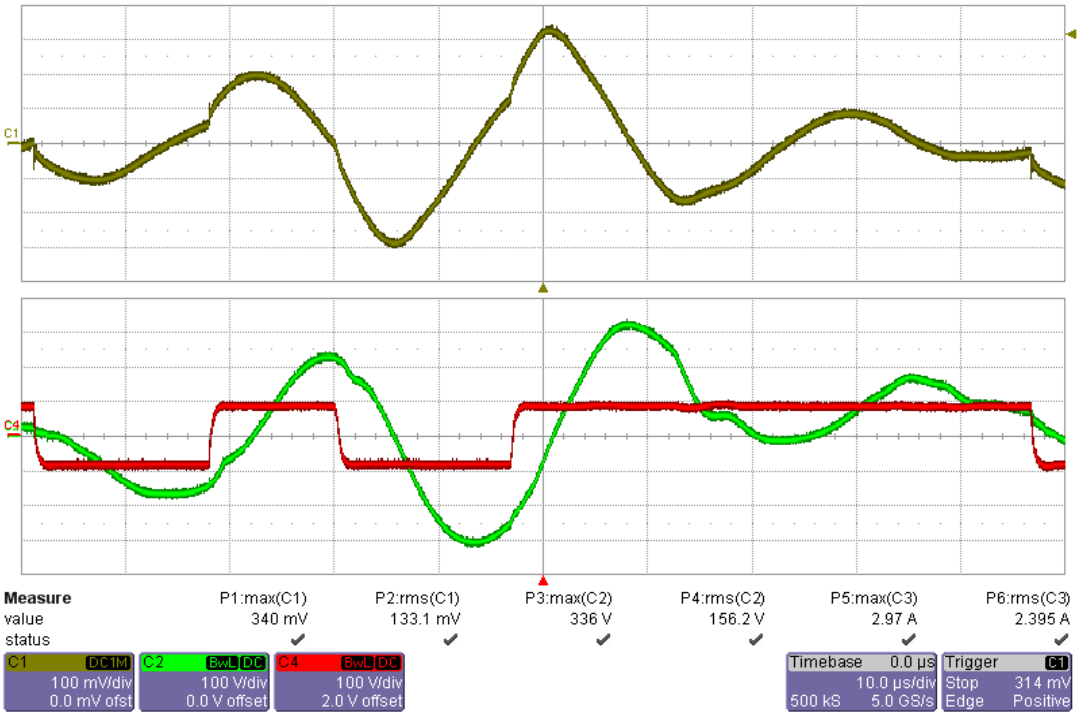


Figure 4.38 Microscopic CMC (yellow, 100mA/div), CMV_{ro} (red, 100V/div), CMV_{no} (green, 100V/div) waveforms for NSPWM with CMI-4.

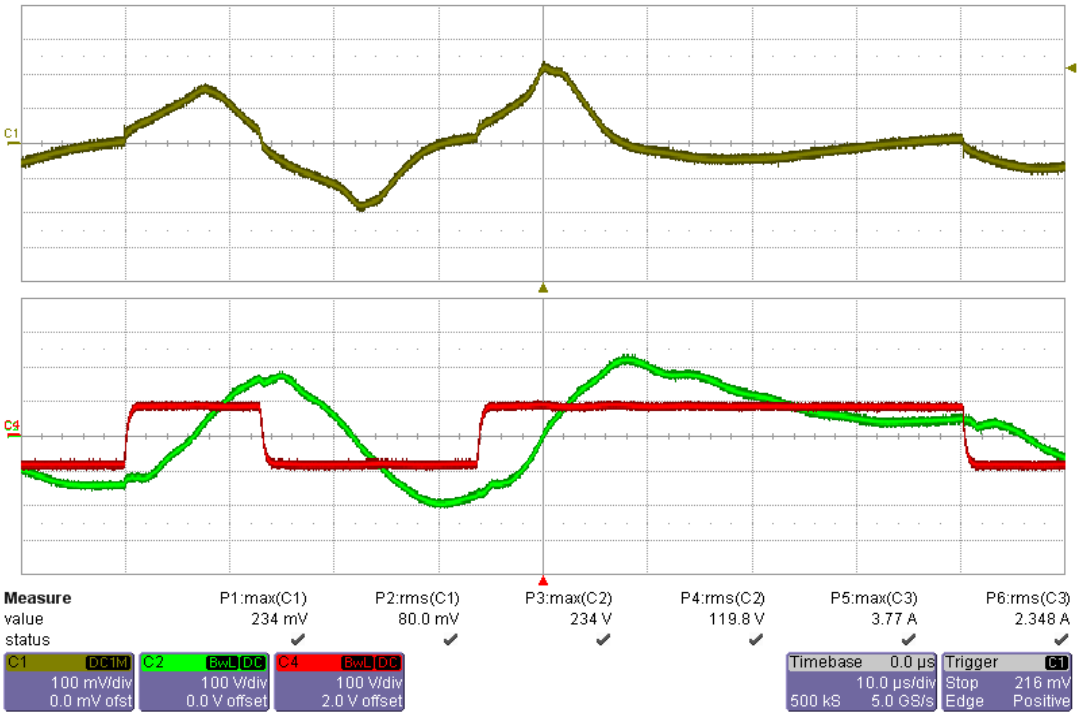


Figure 4.39 Microscopic CMC (yellow, 100mA/div), CMV_{ro} (red, 100V/div), CMV_{no} (green, 100V/div) waveforms for NSPWM with CMI-5.

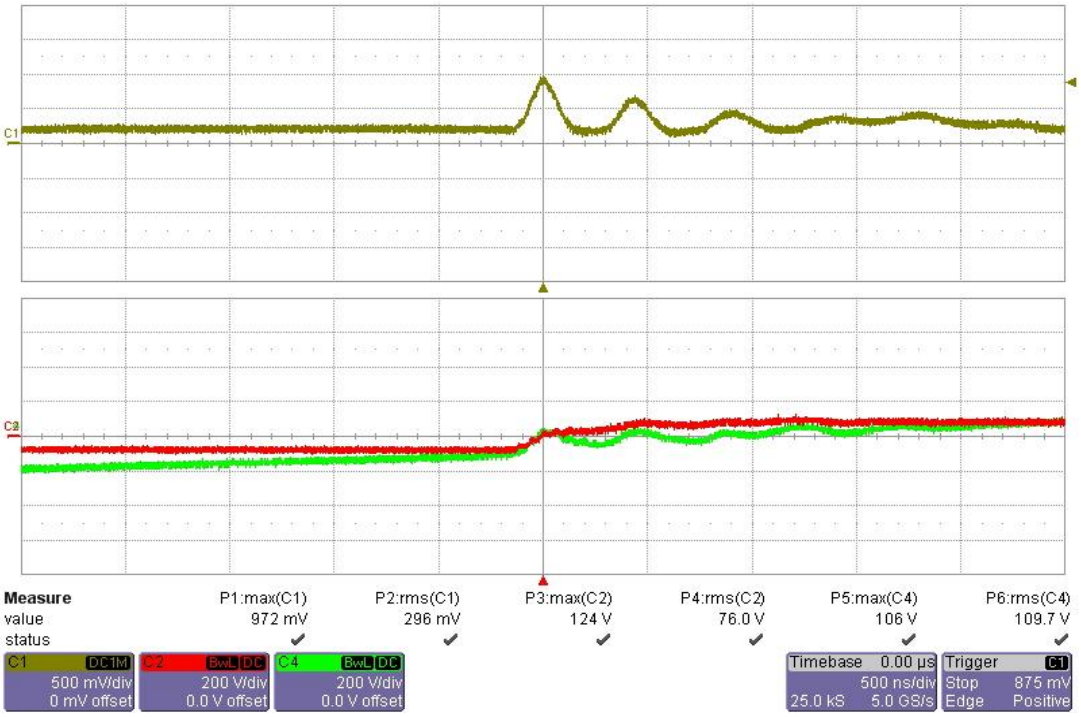


Figure 4.40 Saturation of CMI-5 for SVPWM, CMC (yellow, 500mA/div), CMV_{ro} (red, 200V/div), CMV_{no} (green, 200V/div).

Table 4.4 Experimental CMV measurements

PWM & inverter type		M_i	No CMI		CMI-1		CMI-2		CMI-3		CMI-4		CMI-5	
			CMV peak(V)	CMV rms(V)	CMV peak(V)	CMV rms(V)	CMV peak(V)	CMV rms(V)	CMV peak(V)	CMV rms(V)	CMV peak(V)	CMV rms(V)	CMV peak(V)	CMV rms (V)
2-level VSI	SVPWM	0.8	451	130	468	135.7	424	138.8	407	132.3	530	155.1	495	145.4
	DPWM1		451	131	468	136.6	398	137.7	367	132.9	521	149.5	477	156.4
	NSPWM		212	90	212	92.9	203	90.4	194	87.9	340	123.4	239	107.1
	AZSPWM1		230	88	212	87.1	194	81.1	194	81.6	340	116.6	234	90.1
	AZSPWM3		301	85	225	85.1	212	85.1	208	86.4	274	92.9	234	90
3-level VSI			234	105.4	243	106.7	247	106.4	243	109.1	292	111.7	274	111
		0.4	336	156.7	340	161.6	358	155.6	354	155.4	380	163.1	415	165.7

Table 4.5 Experimental CMC measurements

PWM & inverter type		M_i	No CMI		CMI-1		CMI-2		CMI-3		CMI-4		CMI-5	
			CMC peak (A)	CMC rms (mA)	CMC peak (A)	CMC rms (mA)	CMC peak (A)	CMC rms (mA)	CMC peak (A)	CMC rms (mA)	CMC peak (A)	CMC rms (mA)	CMC peak (A)	CMC rms (mA)
2-level VSI	SVPWM	0.8	1.1	98	0.424	77.5	0.314	59.6	0.208	52.5	0.575	96.4	0.972	68
	DPWM1		1.1	93	0.424	73.8	0.265	60.3	0.177	51.7	0.477	80.1	0.972	79
	NSPWM		0.773	83	0.230	61.6	0.124	48.7	0.106	44.8	0.362	88.1	0.230	60.2
	AZSPWM1		0.773	86	0.239	63.1	0.128	40.8	0.115	38.5	0.380	90.5	0.239	46.9
	AZSPWM3		0.906	60	0.318	37.8	0.190	27.1	0.148	25.9	0.318	47.2	0.327	31.3
3-level VSI			1.02	43	0.203	28.2	0.115	21.4	0.141	21.1	0.221	35.4	0.168	24.4
		0.4	0.994	66	0.256	51.2	0.190	39.5	0.133	35.3	0.336	56.4	0.513	47.1

4.4.5 The Effect of Increase of Common Mode Inductance on the CMC

In this section, the effect of doubling and tripling the common mode inductance on the CMC is investigated. In this experiment only CMI-1 is utilized since its core material is ferrite which is cheaper than the other nanocrystalline cores. In order to observe the effects of doubling and tripling the common mode inductance, two and three identical CMI-1 inductors are included in series.

Table 4.6 shows CMV measurements for one, two, and three CMI-1 inductors inserted in series. As seen, there is no improvement in CMV values as in the previous cases. Table 4.7 shows the CMC measurement results. Including one CMI reduce peak CMCs by approximately 60% as discussed previously, which indicates that common mode impedance is increased by 2.5 times compared to the case without any CMI. Thus, inserting the second and the third CMI-1 inductors increase the common mode impedance by 4 and 5.5 times compared to the case without any CMI. Therefore, peak CMC reduction by 75% and 81% are expected for two CMI-1 and three CMI-1 inductors inserted in series. From the CMC experiments in Table 4.7, for two series CMI-1, peak CMC is reduced by approximately 65% in the conventional SVPWM and DPWM1, and by approximately 75% in the RCMV-PWM methods and in the NPC-VSI. For three series CMI-1, peak CMC is reduced by again approximately 65% in the conventional SVPWM and DPWM1, and by approximately 80% in the RCMV-PWM methods and in the NPC-VSI. In the conventional methods the reduction is lower than the expected rate. However in the RCMV-PWM methods and in the NPC-VSI the reduction rate is as expected.

Table 4.6 CMV results with for one, double, and triple CMI-1 in series

	M_i	1 x CMI-1		2 x CMI-1		3 x CMI-1	
		CMV peak(V)	CMV rms(V)	CMV peak(V)	CMV rms(V)	CMV peak(V)	CMV rms(V)
SVPWM	0.8	468	135.7	460	140.3	451	144.1
DPWM1		468	136.6	460	143.7	442	151.7
NSPWM		212	92.9	234	97.3	234	100.7
AZSPWM1		212	87.1	217	87.3	221	88.3
AZSPWM3		225	85.1	221	86.5	230	88.9
NPC-VSI		243	106.7	261	108.3	270	109.7
	0.4	340	161.6	362	162.2	407	164.2

Table 4.7 CMC results with for one, double, and triple CMI-1 in series

	M_i	1 x CMI-1		2 x CMI-1		3 x CMI-1	
		CMC peak(A)	CMC rms (mA)	CMC peak(A)	CMC rms (mA)	CMC peak(A)	CMC rms (mA)
SVPWM	0.8	0.424	77.5	0.415	69.2	0.408	64.7
DPWM1		0.424	73.8	0.371	69.6	0.362	70.8
NSPWM		0.230	61.6	0.168	56.4	0.146	54.0
AZSPWM1		0.239	63.1	0.177	50.9	0.146	45.9
AZSPWM3		0.318	37.8	0.225	32.1	0.194	30.5
NPC-VSI		0.203	28.2	0.177	24.2	0.155	22.8
	0.4	0.256	51.2	0.217	46.5	0.194	44.3

4.4.6 Performance Comparison

The global and microscopic CMV and CMC evaluations indicate that without the CMI, the two-level VSI with AZSPWM1 and NSPWM has best performance in reducing CMV and CMC. With the inclusion of the CMI, while there is not a

noticeable improvement in the CMV reduction, the CMC is significantly suppressed with CMI-1, CMI-2, and CMI-3 (60%-86% peak CMC reduction). CMI-3 has the best performance with AZSPWM1 and NSPWM in the two-level VSI and with the NPC-VSI (80%-86% peak CMC reduction). The performance difference is indistinguishable between them. Considering the fact that the NPC-VSI has higher cost and lower efficiency than the two-level VSI, the two-level VSI becomes more preferable. CMI-4 is a low-loss CMI, thus it causes CMV/CMC to highly oscillate, and CMI-5 enters magnetic saturation. As a result, CMI-4 and CMI-5 are poor at suppressing CMC.

The core material of CMI-1 is ferrite. Thus it is cheaper than CMI-2 and CMI-3 which have nanocrystalline cores. The performance difference between CMI-2 and CMI-3 is very small. However, the size of CMI-3 is nearly twice that of CMI-2. Therefore, the smaller (the cheaper) CMI-2 is more favorable. Comparable in size to CMI-2, CMI-1 performs noticeably less than CMI-2 in terms of peak CMC reduction (60% of CMI-1 vs. 80% of CMI-2). Its peak CMC is nearly twice that of CMI-2 in NSPWM and AZSPWM1 (230-239mA vs. 124-128mA). On the other hand, the ferrite core of CMI-1 is cheaper than the nanocrystalline core of CMI-2. Thus, there is a trade-off between the CMC suppression and the cost of the magnetic core. The choice between CMI-1 and CMI-2 depends on the specified CMC (EMC) performance.

In conclusion, CMV/CMC reduction by the two-level VSI with NSPWM and AZSPWM1 and including CMI-1 or CMI-2 provides optimum performance. Due to its lower PWM ripple and switching loss, NSPWM, which is applicable for $M_i>0.61$, is more preferable than AZSPWM1 at high M_i. In the $M_i<0.61$ range, since NSPWM is not applicable, there AZSPWM1 is preferred.

4.5 Summary

In this chapter, common mode voltage and common mode (leakage) current performances of the two-level VSI and the NPC-VSI without and with various

common mode inductors are experimentally investigated. The effects of the CMV pulse pattern on the CMC are investigated. It is observed that the CMC is mainly dependent on the *dv/dt* of the CMV and partially dependent on the CMV pulse pattern. In conventional PWM methods, consecutive CMV changes in the same direction increases peak CMC noticeably compared to the RCMV-PWM methods. It is shown that with a two-level VSI employing NSPWM at high M_i and AZSPWM1 at low M_i utilizing a small common mode inductor, a motor drive with very low CMV/CMC can be obtained. With the performance results being comparable to the NPC-VSI, but the cost significantly lower, this approach is more favorable for most industrial applications requiring low CMV and CMC. Depending on the EMC requirements, a cheaper ferrite core or an expensive but higher performance nanocrystalline core could be utilized for the common mode inductor. It is also observed that increasing the common mode inductance reduce the peak CMC approximately at the same rate.

CHAPTER 5

INTERACTION BETWEEN THE PURE SINE FILTER AND PWM UNITS

5.1 Introduction

Among the passive filters discussed in chapter 3, the pure sine filter (PSF) [20], shown in Figure 5.1, provides a complete solution for all the motor side problems caused by inverter output rectangular PWM voltage pulses such as high frequency noise consisting of common and differential mode noise components (which lead to leakage currents causing bearing failure, nuisance trips), and high *dv/dt* leading to motor terminal overvoltages, especially in long cable applications [9], [10], [14], PWM current ripple and the associated losses, and acoustic noise.

Inserted between the inverter and the AC motor for the purpose of providing clean sinusoidal voltage at the motor terminals, the PSF involves common mode and differential mode suppression components. Although the PSF increases the system cost and size due to the large filter component count and size, it eliminates all high frequency components and provides sinusoidal voltages at the motor terminals (as in the ideal power supply case). While employing the PSF alone solves the PWM originated problems at the motor side effectively, the inverter side performance may be limited or degraded compared to the case without the PSF. The PWM ripple circulating inside the inverter may increase, the common and differential mode noise may increase, the voltage linearity of the inverter may be limited due to the PWM method employed, etc. Therefore, enhancements on the inverter side are necessary.

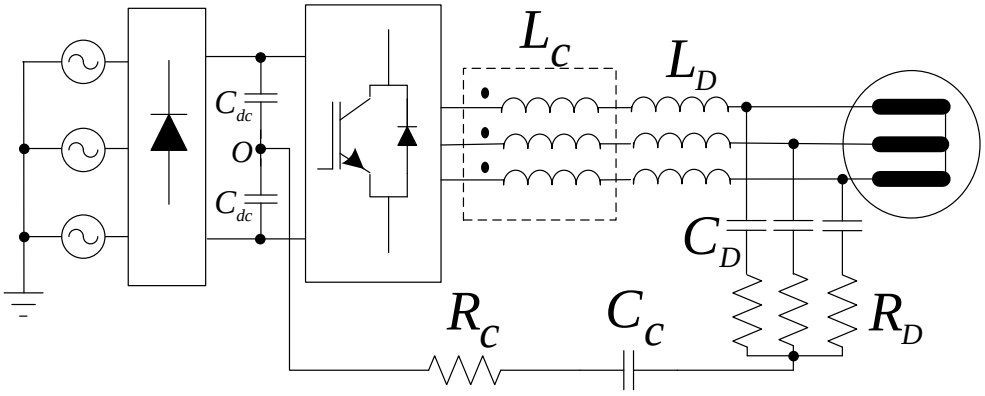


Figure 5.1 Utilization of the pure sine filter with the motor drive.

When considering the PSF and similar filters [18], [21], [22] generally sinusoidal PWM (SPWM) is considered and pulse pattern enhancements have not been reported in the literature. However, the inverter performance can be significantly improved by the switching pattern the PWM generator utilizes as discussed in chapter 2 in detail. Therefore, when used in inverter drives, PSF and similar filters must be considered along with the mentioned advanced PWM techniques.

In this chapter the performance issues of the AC motor drive involving the PSF and the advanced PWM methods are investigated. Among the advanced PWM methods, SVPWM, DPWM1, AZSPWM1, and NSPWM, which provide high performance, are considered. It is shown that the combination of PSF along with these advanced PWM methods may result in a poor performance at the inverter. Particularly, combination of DPWM1 or NSPWM methods yield high overcurrent stresses in the inverter. The rate of change limiting (ROCL) [59] approach is used to overcome the stresses and the drive performance is restored to better levels such that the advantages of both the PSF and advanced PWM methods can be benefited from.

First the operation of the PSF is described, and then the performance issues arising from the PSF and PWM method combinations are discussed. Then, the ROCL approach is introduced, and finally the improved performance results are reported via detailed simulations and experiments.

5.2 Operation of The Pure Sine Filter

The PSF, shown in Figure 5.1, is composed of common mode and differential mode suppression parts. The common mode inductor (CMI) L_C, capacitor C_C, and resistor R_C are the common mode filtering components. The output reactor L_D, three capacitors C_D, and three resistors R_D are the differential mode filtering components.

The common mode equivalent circuit of the filter, shown in Figure 5.2, forms a second-order low-pass filter. Practically, the components are selected such that $L_C >> L/3$, $C_C << 3C$, and $R_C >> R_D/3$, thus the differential mode components (L_D, C_D, and R_D) have negligible effects on the common mode filtering. The CMI L_C suppresses the CMC. The capacitor C_C and resistor R_C provide a low common mode impedance path which is parallel to the motor CMC path. This construction further reduces the CMC through the motor. The capacitor C_C value is much higher than the motor common mode capacitance. Thus, the motor capacitance can be ignored from the common mode equivalent circuit. The impedance of the CMI L_C is much higher than the capacitor C_C at switching frequency range (12 kHz) and above, thus the high frequency CMV generated by the VSI is applied across the L_C. Therefore, it is eliminated from the motor terminals. On the other hand, the low frequency and DC CMV components caused by the zero-sequence signal largely appears across the capacitor C_C which provides much higher impedance than the CMI L_C at such frequencies. The resistor R_C is the damping resistor which damps the oscillations between L_C and C_C.

The differential mode equivalent circuit, shown in Figure 5.3, is a standard differential mode sine filter ($L_DC_DR_D$) discussed is chapter 3, and the common mode suppression components have no effects in differential mode suppression. The cut-off frequency of differential mode filter is below the PWM frequency, thus it eliminates the differential mode PWM frequency components and switching ripple current and makes motor terminal voltages sinusoidal. The resistor R_D is the damping resistor which damps the oscillations between L_D and C_D.

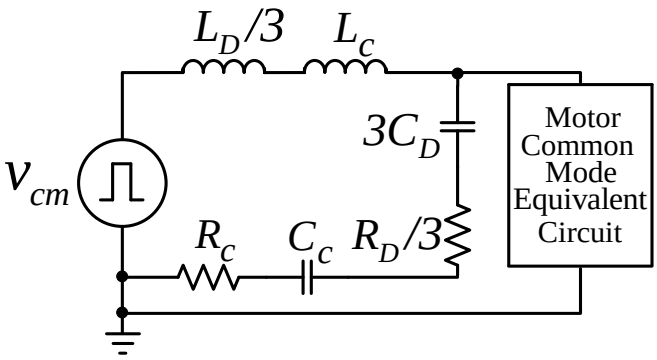


Figure 5.2 Common mode equivalent circuit of the PSF.

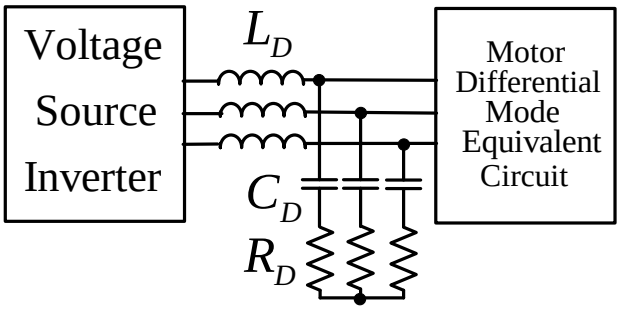


Figure 5.3 Differential mode equivalent circuit of the PSF.

5.3 Interaction Between The PSF and PWM Methods

In the advanced PWM methods, as discussed in chapter 2, the injected zero-sequence signal is a low frequency signal (periodic at $3\omega_e$ and/or its multiples, lower than the carrier frequency by at least an order of magnitude, where ω_e is the fundamental frequency) which causes low frequency CMV. At such frequencies the parasitic circuit components (capacitances) are negligible (open-circuit). Therefore the zero-sequence voltage has no detrimental effect on the drive and yields no CMC, unless low common mode impedance path is established by filter configurations such as those reported in [18], [20], [21], [22] which include PSF.

The PSF structure provides a low impedance common mode path from the inverter output to the DC bus midpoint (through the inverter-L_C-L_D-C_D-R_D-C_C-R_C-O path).

Be it the above mentioned low frequency common mode voltage (usually termed as zero-sequence injection signal) or the CMV at high frequency (the carrier frequency or higher), generated by the inverter, this voltage drives this circuit and forces a CMC. Thus an interaction occurs.

When SPWM is considered, since no zero-sequence signal is injected, no low frequency CMC flows through this path. However, in advanced PWM methods, low frequency CMV causes low frequency CMC through this path. The low frequency CMV caused by the zero-sequence signal largely appears across the capacitor C_C which provides high impedance at such frequencies. Since SVPWM and AZSPWM1 methods have continuous and smoothly varying zero-sequence injection signals, the low frequency CMCs of these methods are negligible compared to the high frequency CMCs. However, in DPWM1 and NSPWM, due to instantaneous polarity change of the zero-sequence signal every 60°, the low frequency CMV across the capacitor C_C also changes rapidly which results high capacitive currents through the common mode filter. As the CMC flows through the inverter IGBTs, in particular at low M_i it becomes large and overcurrent trip or IGBT failure may occur. Even if the current rating of the IGBTs is high and no such failure occurs, a strong acoustic noise is created from the filter inductors due to this current. Therefore, the operation is problematic. On the other hand, discontinuous PWM methods such as DPWM1 and NSPWM can not be disregarded, as they provide the best performance in the upper half of the linear M_i range of the inverter. Thus, a technique to overcome the interaction between the inverter and filter is developed.

In order to reduce the magnitude of the CMC during the zero-sequence signal polarity change, the rate of change of the zero-sequence signal should be reduced. Therefore, the original zero-sequence signal is passed through the rate of change limiter (ROCL) shown in Figure 5.4 such that the zero-sequence signal becomes smooth and with finite derivative. Adding this zero-sequence signal to the modulation signals (v_a^*, v_b^*, v_c^*) the discontinuity of the modulation wave is eliminated. The rate (dv/dt) limit coefficient of the ROCL K_{vo} in Figure 5.5 is

selected based on the maximum current that is allowed to flow through the common mode filter. This coefficient can be calculated from the maximum targeted CMC through C_C as (5.1). Given a C_C, maximum capacitor current is determined by changing K_{vo}.

$$K_{vo} = (dv/dt)_{max} = I_{C,max} / C_C \tag{5.1}$$

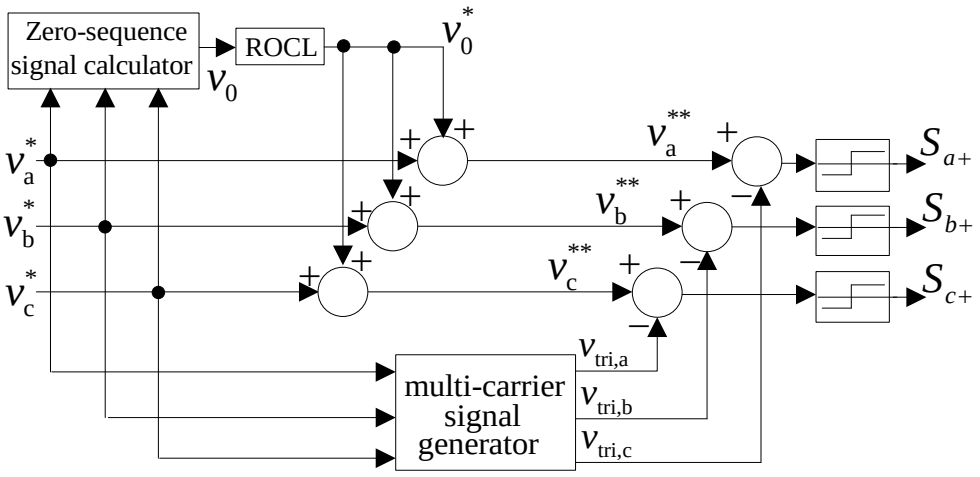


Figure 5.4 The zero-sequence signal injection PWM diagram including ROCL.

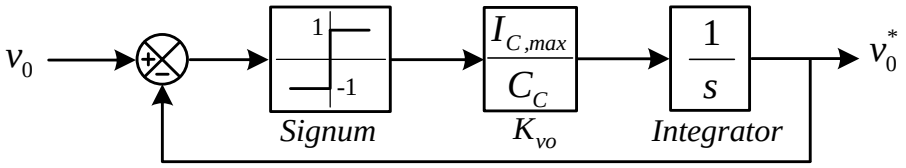


Figure 5.5 Detailed ROCL block diagram.

5.4 Design of The Pure Sine Filter

5.4.1 Design of The Common Mode Filtering Components

Since the high frequency CMV is applied across the common mode inductor L_C, it is the component that suppresses the high frequency CMC, and it should be

designed such that the magnetic core does not saturate at the maximum CMV magnitude. Since the flux in the inductor is directly proportional with the integral of the voltage with respect to time, the flux is maximum in conventional PWM methods when the inverter is operated at M_i=0 where the shape of the CMV at this operating point is a rectangular waveform at switching frequency, and with a magnitude of $V_{dc}/2$. In this case the maximum flux density of the CMI L_C is given by (5.2),

$$B_{max} = V_{dc} /(8NAf_S) \tag{5.2}$$

where V_{dc} is the DC bus voltage, N is the turn number per phase of L_C, A is the cross sectional area of the core, and f_S is the switching frequency. Using a magnetic material with high saturation flux density, decreases the product NA for constant switching frequency and DC bus voltage values, which means smaller core size and turn number. In this design, a nanocrystalline core having a saturation flux density of 1.2T is used [58]. For V_{dc}=500V and f_S=12 kHz cases, a common mode inductor with the parameters given in Table 5.1 is designed.

Table 5.1 The designed common mode inductor parameters

Common mode inductance at 12 kHz	73 mH
Turn number per phase	36
Outer diameter	63 mm
Inner diameter	50 mm
Height	25 mm
AL value at 10 kHz	58.6 μH/N^2
Saturation flux density	1.2 T

In order to avoid the oscillation of injected zero-sequence signal and suppress the PWM frequency CMV, the resonant frequency for the common mode circuit should be much higher (as a rule of thumb at least ten times) than the maximum zero-

sequence signal frequency, and much lower than the switching frequency [20]. For the maximum fundamental output frequency of 60 Hz, the maximum zero-sequence signal frequency becomes 180 Hz. Therefore, the capacitance of C_C is selected as 100 nF, and using the equation (3.3) the resonance frequency is 1.86 kHz. The common mode capacitance of the motor is about 4 nF which is much lower than C_C value. Therefore, the CMC mainly flows through the filter rather than the motor. The damping factor of the common mode equivalent circuit given by (5.3), is typically selected between 0.05 and 0.1 [20], [21].

$$\zeta = \frac{R_C}{2}\sqrt{C_C/L_C} \tag{5.3}$$

The value of damping resistor R_C is selected as 113 Ω, so that the damping factor is 0.07.

5.4.2 Design of The Differential Mode Filtering Components

The inductance of output reactor L_D should be as small as possible for the purpose of low volume, weight, and system cost. The inductance value is selected as 2.4 mH (2.5% on a three-phase, 400 V_{rms} line-to-line, 50 Hz, 5 kVA motor drive). The per-phase leakage inductance of the motor referred to the stator is 7.9 mH. This value is much higher than the output reactor inductance L_D value. Thus, the inverter output current ripple is mainly dependent of L_D value. In order to pass the fundamental frequency output voltage without reduction of magnitude and suppress the PWM frequency component, the resonant frequency of the differential mode filter should be much higher than the maximum inverter output frequency of 60 Hz and much lower than the switching frequency of 12 kHz [20]. The capacitor C_D is selected as 2.2 μF, thus using the equation (3.3) the resonant frequency becomes 2.2 kHz. The resistance value of damping resistor R_D is selected as 3.3 Ω. Thus the damping factor is 0.06.

Table 5.2 The PSF design parameters

Common mode inductor L_C	73 mH
Common mode capacitor C_C	100 nF
Common mode resistor R_C	113 Ω
Output reactor L_D	2.4 mH
Differential mode capacitors C_D	2.2 uF
Differential mode resistors R_D	3.3 Ω

5.5 Performance Analysis of The ROCL Method By Means of Computer Simulations

In order to verify the proposed method, an inverter with the PSF is modeled and simulated employing Ansoft/Simplorer [60]. In the simulations, only the performance of ROCL approach (thus the voltage and current of the capacitor C_C) is investigated. The performance of the PSF, which includes differential mode and common mode noise suppression, is only investigated experimentally.

In Figure 5.6 the simulation circuit diagram is shown. The VSI is fed by a constant DC voltage source of 500V. Two DC bus capacitors are used to form the DC bus midpoint. During construction of the VSI, simplified "system level" semiconductor components (IGBT and diodes) are utilized for the sake of simplicity. The parameters of the simulated PSF are given in Table 5.3. They are the same parameters as those in the experiments. Using Figure 5.2 as a reference circuit, the common mode impedance of the R_C-C_C path, that is parallel to the motor, is very low compared to the common mode impedance of the motor, and the CMC mainly flows through the R_C-C_C path. Since the motor CMC becomes negligible compared to the CMC through the capacitor C_C, the high frequency common mode equivalent circuit model of the motor is not included. Also, since the differential mode parameters of the motor have no effect on the common mode behavior of the PSF, the motor is not included in the simulation circuit.

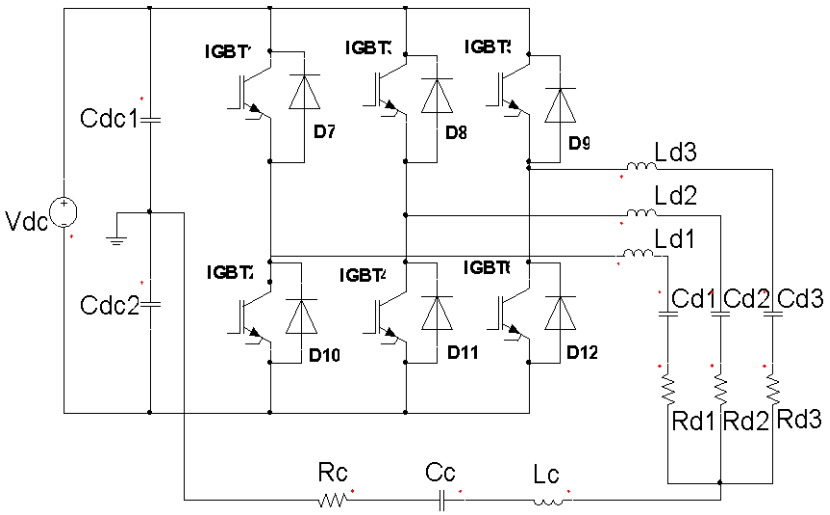


Figure 5.6 The PSF system simplified simulation model.

Table 5.3 The simulation model parameters

Vdc (DC bus voltage)	500 V
Cdc1, Cdc2 (DC bus capacitors)	2 mF
Ld1, Ld2, Ld3 (Differential mode inductors)	2.4 mH
Cd1,Cd2, Cd3 (Differential mode capacitors)	2.2 uF
Rd1, Rd2, Rd3 (Differential mode resistors)	3.3 Ω
Lc (Common mode inductor)	73 mH
Cc (Common mode capacitor)	100 nF
Rc (Common mode resistor)	113 Ω
PWM frequency	12 kHz for SVPWM, 18 kHz for NSPWM

In order to show the effect of continuous and discontinuous zero-sequence signals, first SVPWM, which has smoothly varying zero-sequence signal, is considered. Then NSPWM is considered as a discontinuous PWM method. For SVPWM, M_i=0.9 case, where zero-sequence signal is high, is considered, and for NSPWM, M_i=0.61 (lower boundary of the linearity region) case, where rate of change of the zero-sequence signal is maximum, is considered to show the performance of ROCL noticeably.

In Figure 5.7, the simulation waveforms for SVPWM are shown. As seen, the zero-sequence signal appears across the capacitor C_C. Since the zero-sequence signal is continuous, the voltage across C_C varies smoothly and the low frequency CMC through C_C is very small compared to the high frequency component. The peak CMC is about 30mA. In conclusion, for continuous PWM methods, ROCL is not required.

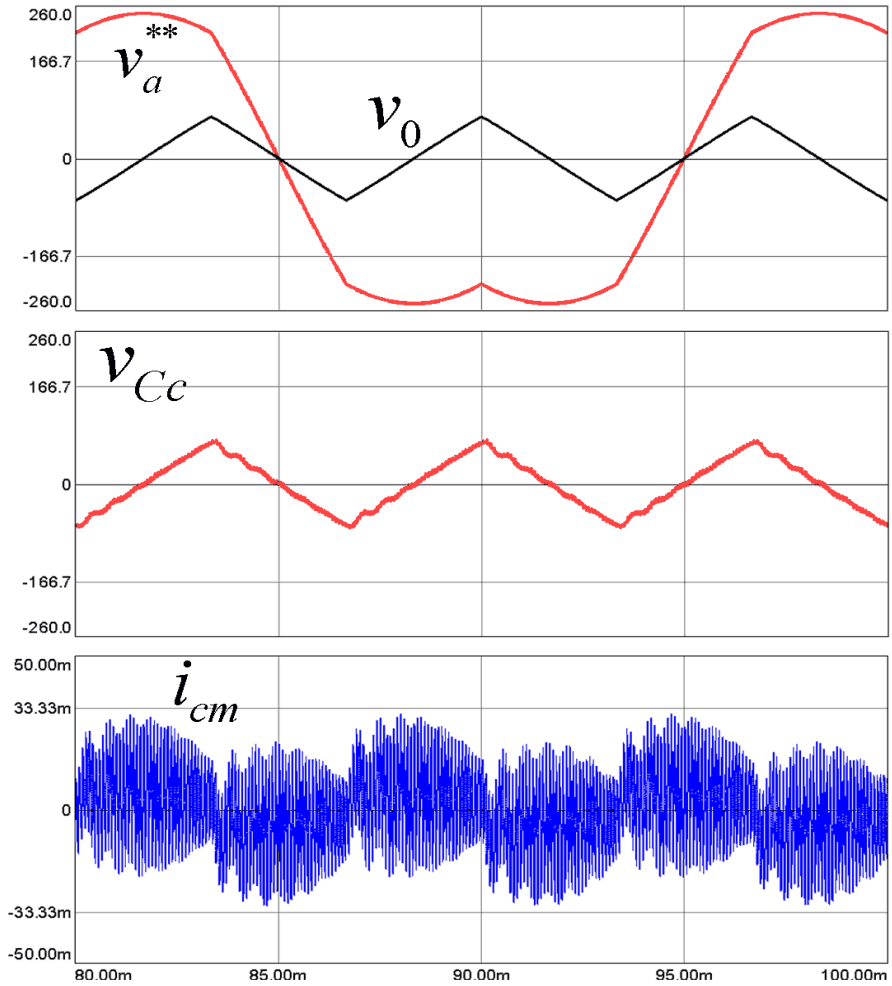


Figure 5.7 Simulation waveforms for SVPWM, zero-sequence signal (top, black), modulation signal (top, red), C_C voltage (middle, red), C_C current (bottom, blue) (M_i=0.9).

In Figure 5.8, the simulation waveforms for NSPWM are shown. As seen in Figure 5.8.a (black waveforms), when no ROCL is employed, the zero-sequence signal and thus modulation wave have discontinuity. If no ROCL is applied and the CMI L_C is considered nonsaturable, the CMC becomes large and the voltage on C_C becomes large and oscillatory. Peak CMC is about 200mA (Figure 5.8.b). In practice, maintaining the CMI size small requires the use of saturable core. In this case, if the CMC becomes large, the core may saturate and the CMC may increase further and the voltage on C_C may still have large overshoots. In order to model saturable CMI, the inductance of the CMI is reduced to a very small value (5mH) during the polarity change of the zero-sequence signal. In this case, the peak CMC reaches 500mA (Figure 5.8.c). Using ROCL the discontinuity of the modulation wave is eliminated as shown in Figure 5.8.a (red waveforms). As a result the capacitor C_C voltage approaches the v_o^* and the current through it is confined to a smaller value (about 100mA) than without ROCL (Figure 5.8.d). As a result, when ROCL is employed the peak CMC is reduced. For saturable CMI case, the reduction rate is higher. In the experimental results, it will be shown that the peak CMC without ROCL is much higher and thus the peak CMC reduction with ROCL is much more.

For a successful ROCL design, two parameters should be carefully considered. The K_{vo} gain should not exceed the value defined in (5.1) and the inductor should be designed such that the core does not saturate at the targeted peak CMC. Given a C_C, and a targeted $I_{C,max}$, the CMI should be designed and implemented in the hardware. Then K_{vo} should be adjusted (gradually decreased) such that the targeted peak current is obtained. Decreasing K_{vo} further is not recommended. Because a very small K_{vo} results in extension of the transition interval (Δt of Fig. 5.8.a) and when the clamped duration of the modulation waves decrease, the switching losses increase. It should be noted that in the ROCL applied region (Δt), during the transition intervals, the resulting PWM pulse pattern becomes identical to that of SVPWM for DPWM1, and that of AZSPWM1 for NSPWM. Thus, the PWM ripple is not affected significantly for DPWM1, and reduced CMV property is not affected for NSPWM.

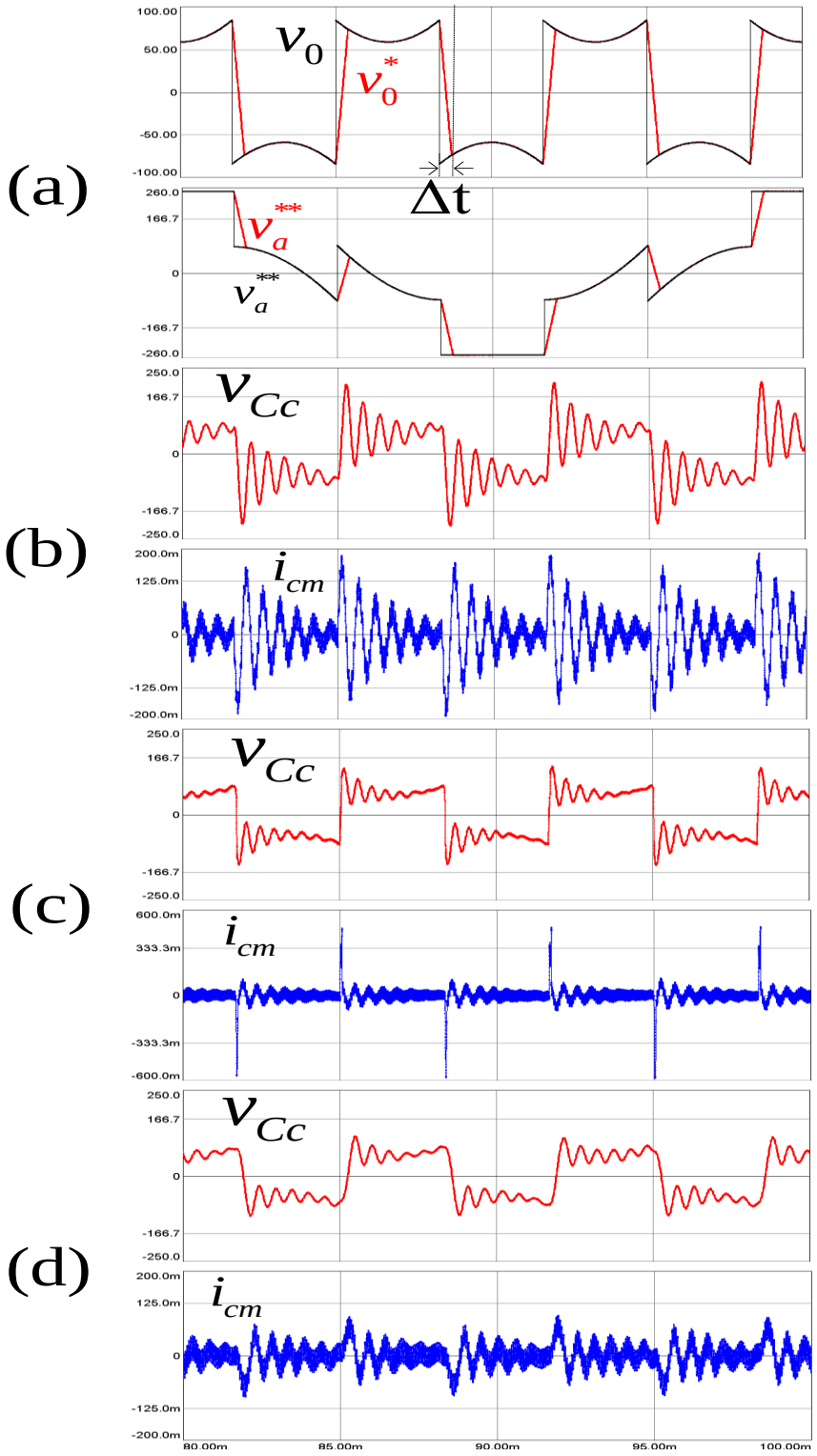


Figure 5.8 Simulation waveforms for NSPWM (M_i=0.61), (a) ideal (black) and ROCL applied (red) zero-sequence signals and modulation waveforms, the capacitor C_C voltage (red) and current (blue) waveforms for (b) without ROCL and nonsaturable CMI, (c) without ROCL and saturable CMI (d) with ROCL.

5.6 Experimental Results

In this section the experimental results of an inverter drive employing the PWM methods and the PSF are discussed. Figure 5.9 shows the experimental setup circuit diagram of the motor drive with the PSF connected. The designed PSF is shown in Figure 5.10. The inverter drive is the same as that described in the previous chapter. The system is fed from $400V_{rms}$ line-to-line, 50 Hz power line. A Y/Y isolation transformer (1:1) is placed between the power line and the diode rectifier for the purpose of the CMC measurement. The 500V DC bus is formed from two series capacitors and provides a midpoint terminal for the PSF CMC (i_{cm}) path. The PSF filter is inserted between the inverter and the motor, which is placed on an insulated base plate. With the neutral point of the transformer secondary connected to the chassis of the motor through a 1-meter-long cable, the cable current becomes the motor CMC (i_g). The two-level inverter operates in the constant *V/f* mode (176.7 V_{rms}/50 Hz), and the inverter output feeds a 4 kW, 400V, 4-pole, Y connected induction motor with the parameters given in Appendix A. The motor is operated at no-load throughout the experiments. The switching frequency is 12 kHz for SVPWM and AZSPWM1, and 18 kHz for DPWM1 and NSPWM (to provide equal average switching frequency of 12 kHz in all).

The experimental procedure is conducted in three major steps. First the motor drive performance without any filters is illustrated. Then the motor side performance enhancement with PSF is investigated. Finally, the inverter side performance of the drive with PSF is investigated.

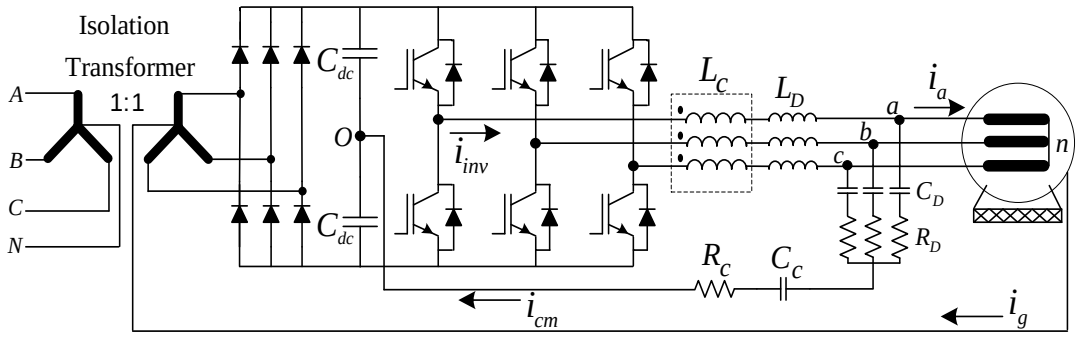


Figure 5.9 The experimental setup of the motor drive with the PSF.

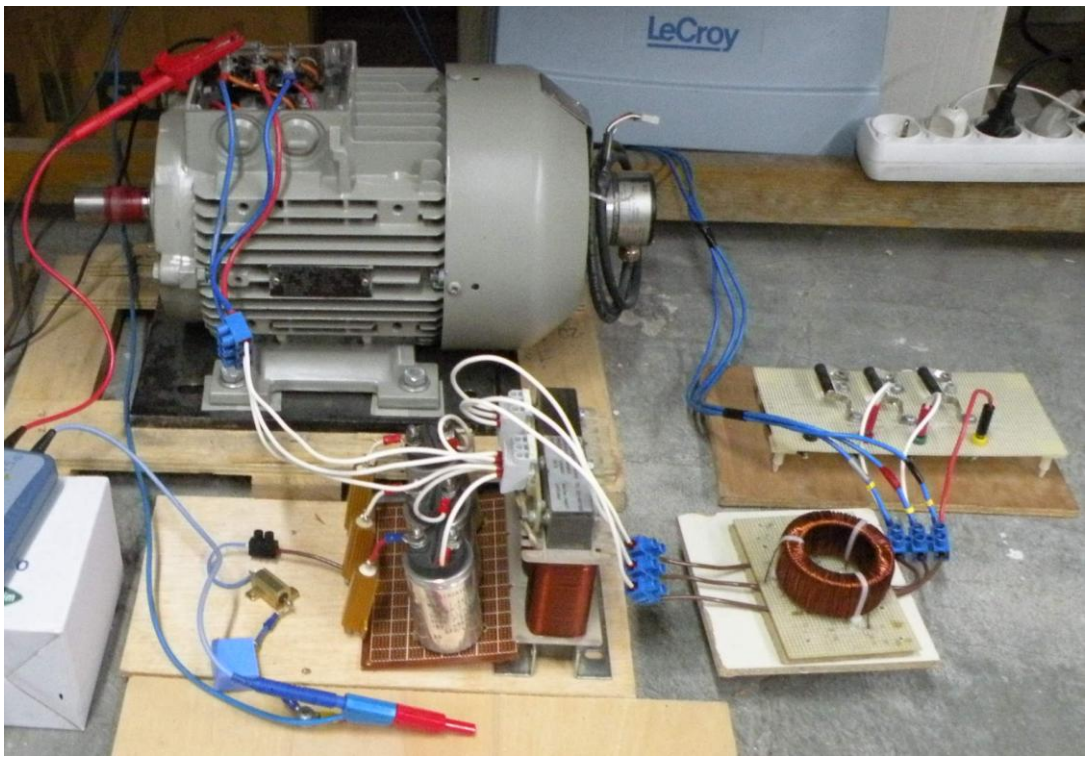


Figure 5.10 The designed PSF.

5.6.1 Experimental Results Without Any Filter

First, the drive is operated without any filter. However, the motor chassis is connected to the transformer secondary star point to allow the motor CMC i_g. In Figures 5.11-5.14, the motor line-to-line terminal voltage, phase current and CMC i_g experimental waveforms are shown. As seen in the figure, the motor is exposed to the inverter output rectangular PWM voltage pulses, which results in PWM current ripple. The motor phase current i_a includes approximately 400mA (10%) peak-to-peak ripple for SVPWM, DPWM1 and NSPWM, and 800mA (20%) peak-to-peak ripple for AZSPWM1 while the peak motor current is 4A. The peak motor CMC i_g is in 0.7A-1A range, and the rms motor CMC i_g is in 110mA-140mA range for all methods with NSPWM performing the best (0.7A peak CMC, 110mA rms CMC).

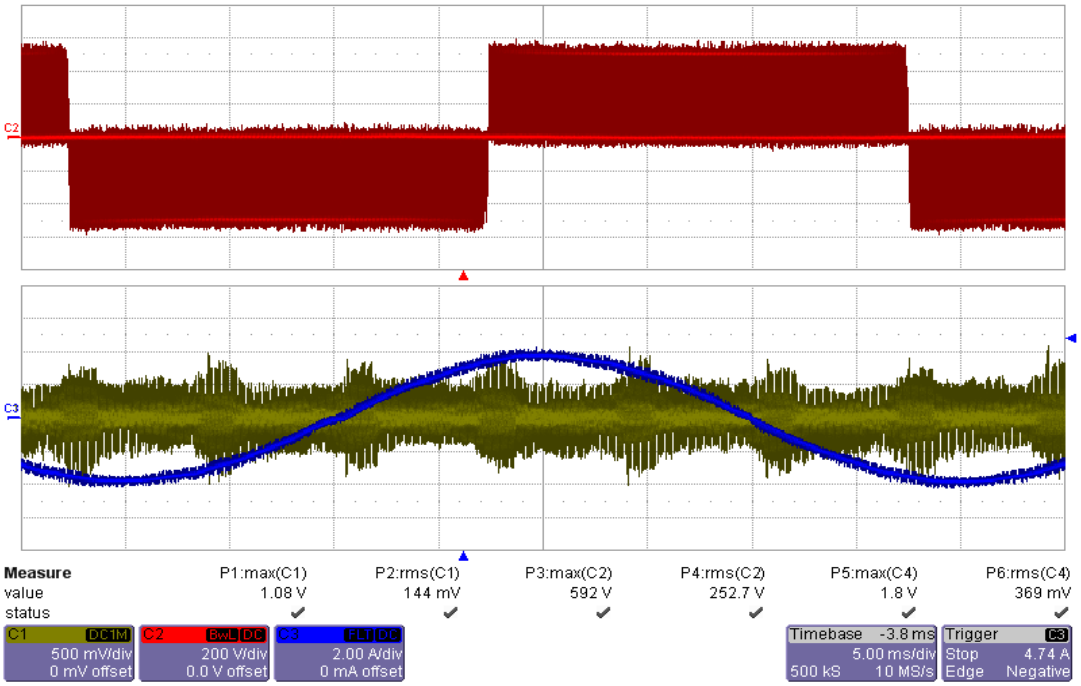


Figure 5.11 Motor terminal voltage (v_{ab}) (red, 200V/div), motor CMC (i_g) (yellow, **500mA/div**), and motor phase current (i_a) (blue, 2A/div) waveforms without any filter for SVPWM (M_i= 0.4) (time scale: 5ms/div).

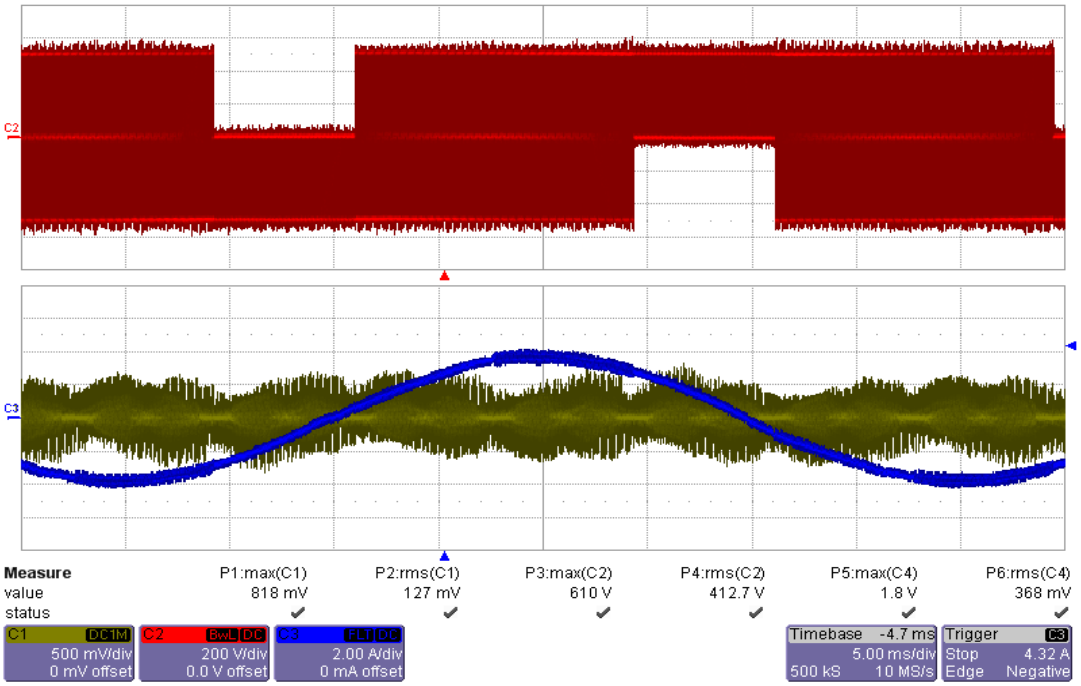


Figure 5.12 Motor terminal voltage (v_{ab}) (red, 200V/div), motor CMC (i_g) (yellow, **500mA/div**), and motor phase current (i_a) (blue, 2A/div) waveforms without any filter for AZSPWM1 (M_i= 0.4) (time scale: 5ms/div).

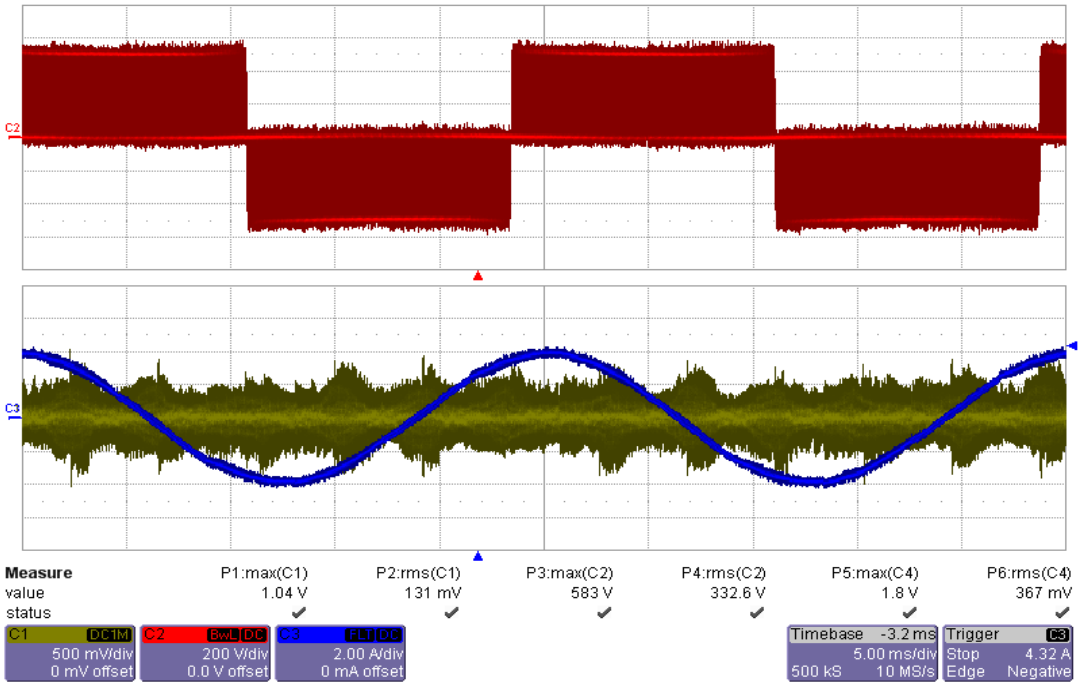


Figure 5.13 Motor terminal voltage (v_{ab}) (red, 200V/div), motor CMC (i_g) (yellow, **500mA/div**), and motor phase current (i_a) (blue, 2A/div) waveforms without any filter for DPWM1 (M_i= 0.6) (time scale: 5ms/div).

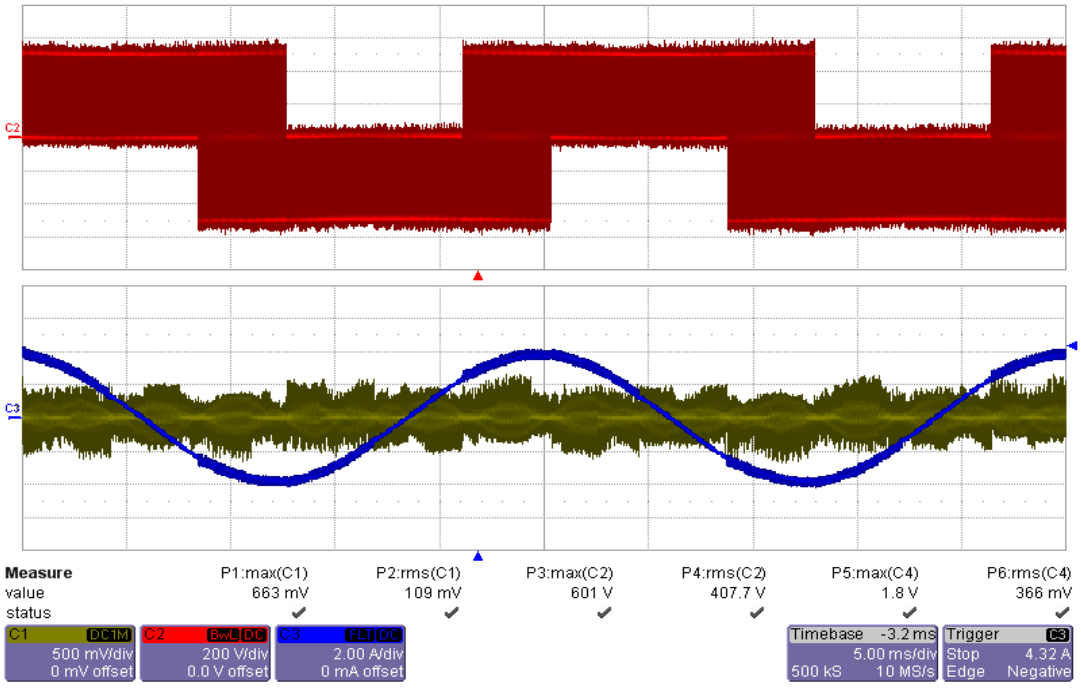


Figure 5.14 Motor terminal voltage (v_{ab}) (red, 200V/div), motor CMC (i_g) (yellow, **500mA/div**), and motor phase current (i_a) (blue, 2A/div) waveforms without any filter for NSPWM (M_i= 0.6) (time scale: 5ms/div).

The microscopic views of the CMC and also the shaft voltage (measured between the motor chassis and load side of the motor shaft) are shown in Figure 5.15. As can be seen from the figure, utilizing RCMV-PWM methods, the negative effects of the CMV can be partially reduced. The peak shaft voltages of SVPWM and DPWM1 methods approach 10V, and the peak CMCs approach 1A. NSPWM and AZSPWM1 reduce the peak shaft voltage to 6V, and the peak CMCs to 0.7A. Figure 5.16 shows the dielectric breakdown in the bearings, which causes EDM bearing currents as discussed in chapter 3. Note that in the dielectric breakdown instant, CMC appears as a sharp needle.

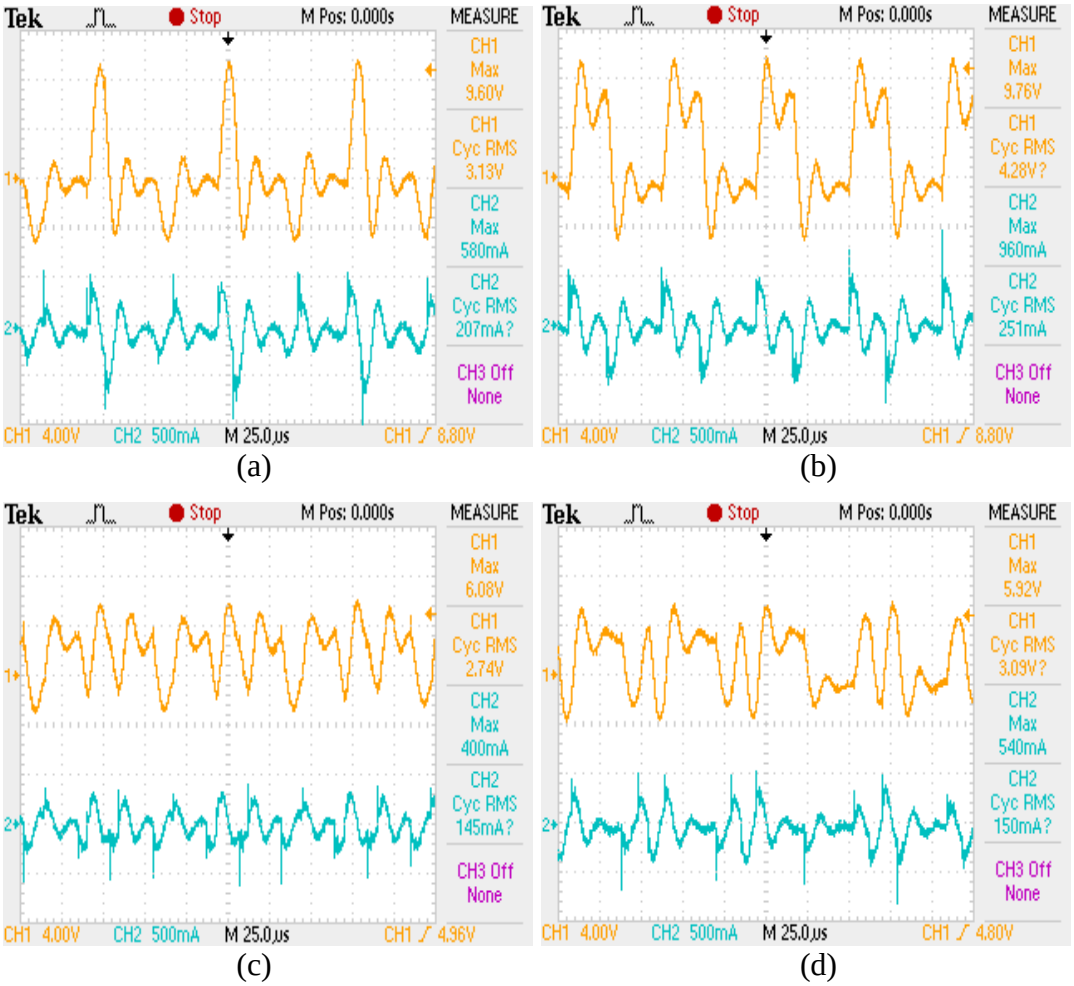


Figure 5.15 Motor shaft-to-frame voltage (yellow, 4V/div) and motor CMC (i_g) waveforms (blue, 500mA/div) without any filter for (a) SVPWM, (b) DPWM1 (c) AZSPWM1, (d) NSPWM (M_i = 0.8) (time scale: 25us/div).

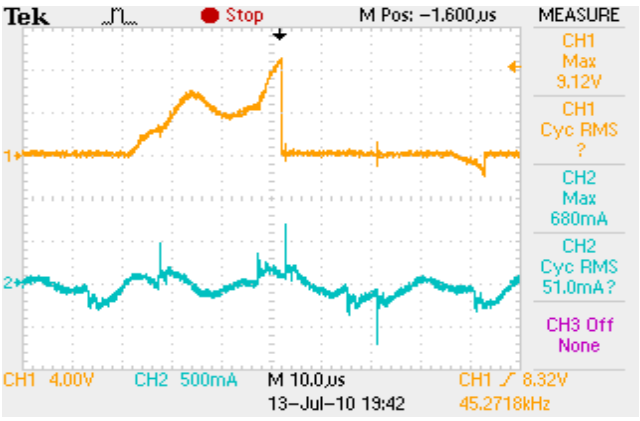


Figure 5.16 Dielectric breakdown in the bearing, motor shaft-to-frame voltage (yellow, 4V/div) and motor CMC (i_g) waveforms (blue, 500mA/div) (time scale: 10us/div).

As seen in Figure 5.17, when a 70m-long cable is inserted between the inverter and the motor, significant line-to-line voltage overshoots arise due to voltage reflection. For 500V DC bus voltage the peak overvoltage stress is as high as 1370V [35]. Based on this set of experiments without any filters, it becomes apparent that the motor copper and iron losses increase due to PWM ripple current, motor winding overstresses and bearing electrical stresses occur, and electromagnetic noise spreads to the external electrical environment. Hence, filtering is required.

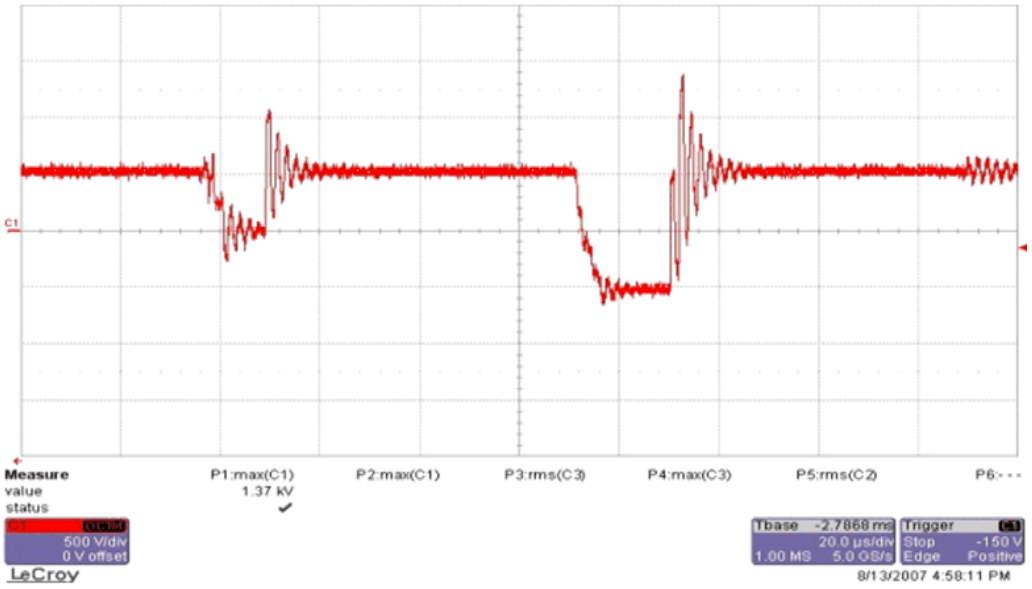


Figure 5.17 Line-to-line voltage pulses of AZSPWM1 (M_i= 0.4) (500V/div) (time scale: 20us/div).

5.6.2 Motor Side Performance Enhancements of The PSF

In order to show the effects of the PSF components separately, three experiment steps are conducted. First, only differential mode filter consisting of $L_{D,}$ C_D, and R_D is connected. Then, in addition to the differential mode filter, CMI L_C is inserted. Finally, connecting R_C and C_C between filter neutral point and DC bus midpoint, the motor side performance of PSF is investigated.

First, only differential mode filter consisting of $L_{D,}$ C_D, and R_D is connected. As shown in Figure 5.18 the motor line-to-line terminal voltage v_{ab} and motor phase current i_a are sinusoidal. The PWM ripple on the phase current is eliminated. On the other hand, as seen in Figure 5.19, CMC i_g and shaft voltage waveforms are nearly similar to the motor without any filter case. There is a slight reduction in peak CMC due to the common mode inductance of the reactor L_D (0.8mH).

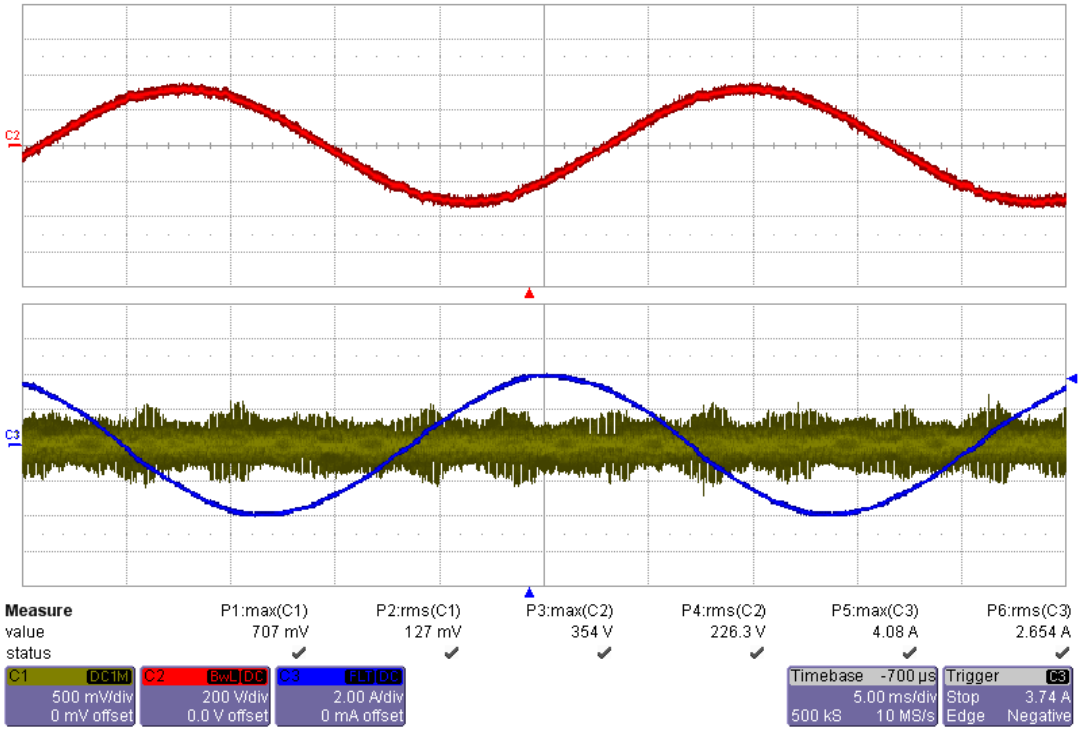


Figure 5.18 Motor terminal voltage (v_{ab}) (red, 200V/div), motor CMC (i_g) (yellow, **500mA/div**), and motor phase current (i_a) (blue, 2A/div) waveforms with only differential mode filter for SVPWM (M_i= 0.6) (time scale: 5ms/div).

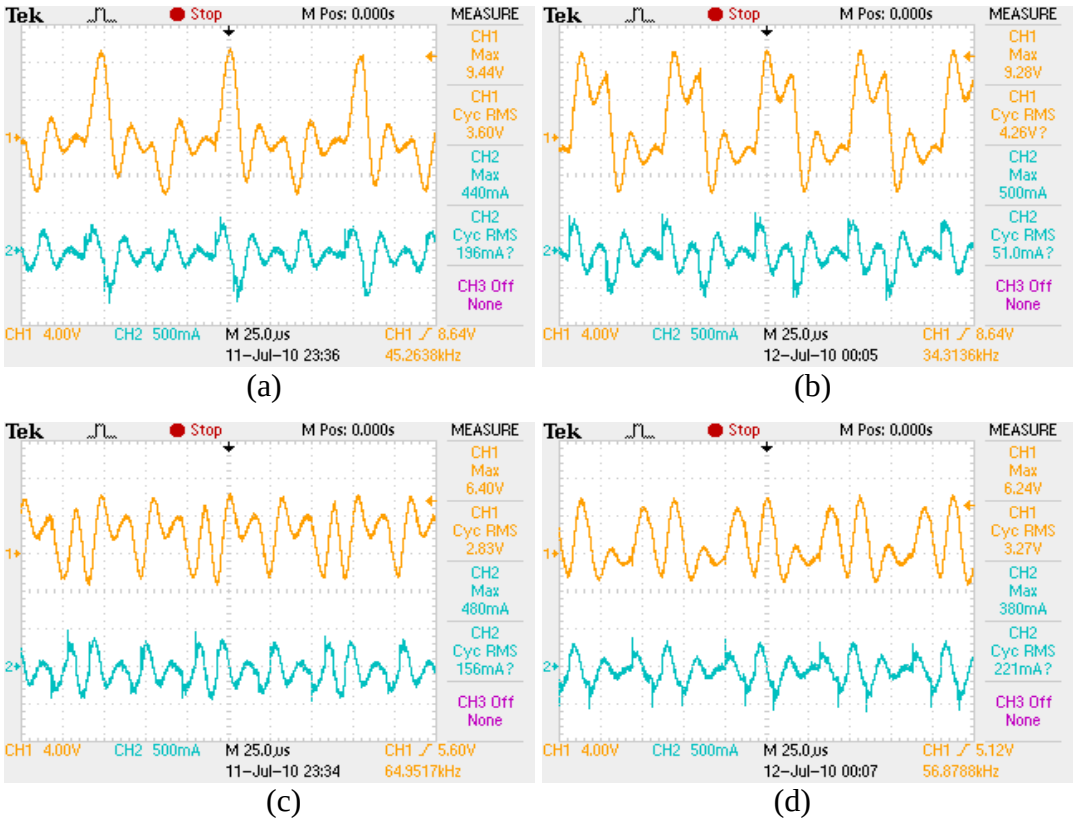


Figure 5.19 Motor shaft-to-frame voltage (yellow, 4V/div) and motor CMC (i_g) waveforms (blue, 500mA/div) with only differential mode filter for (a) SVPWM, (b) DPWM1, (c) AZSPWM1, (d) NSPWM (M_i = 0.8) (time scale: 25us/div).

Second, the CMI L_C is inserted in addition to the differential mode filter but i_{cm} (C_C-R_C) path is remained open. As shown in Figure 5.20, the motor line-to-line terminal voltage v_{ab}, motor phase voltage v_{an}, and motor phase current i_a are the same as previous case because of the differential mode filtering. With the addition of the CMI L_C, the peak CMC i_g is noticeably reduced (about 100mA level). The common mode equivalent circuit consisting of L_C and the motor common mode capacitance (about 4nF) forms a second-order low-pass filter, and the cut-off frequency is about 10 kHz, which is lower than the switching frequency. Thus the above PWM frequency components of motor CMC i_g and shaft voltage are eliminated, and they have smooth waveforms at PWM frequency as shown in Figure 5.21. Note that, the motor CMC i_g leads shaft voltage by 90° since the shaft voltage has the same

waveform as the common mode voltage across the motor. The peak shaft voltage reaches 5V in SVPWM and DPWM1, and 2V in AZSPWM1 and NSPWM.

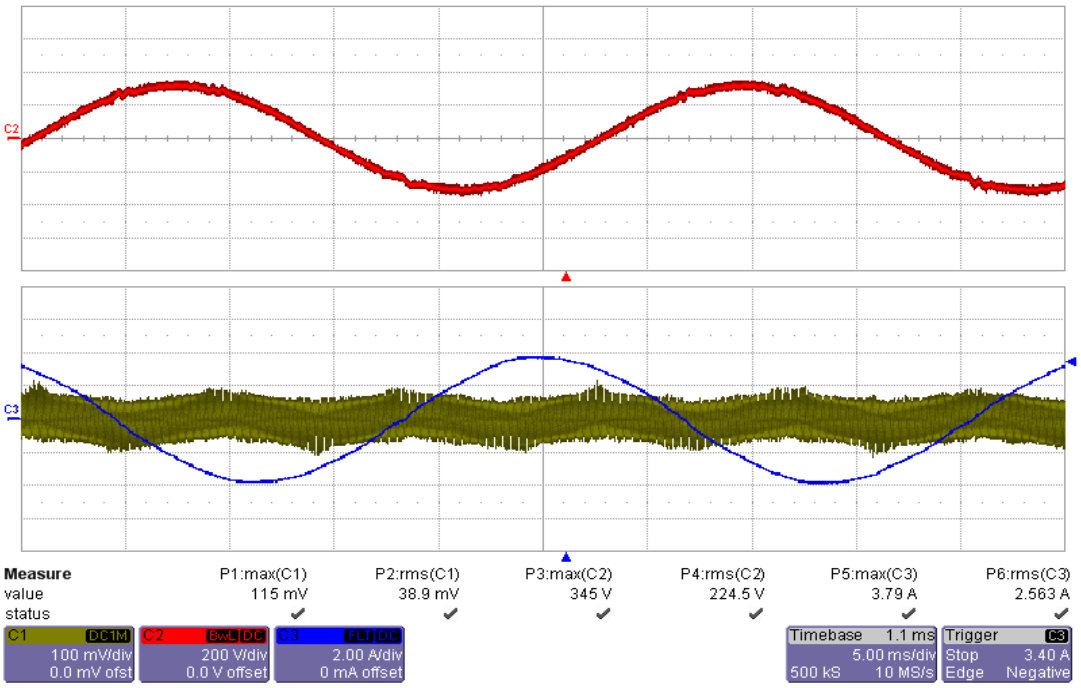


Figure 5.20 Motor terminal voltage (v_{ab}) (red, 200V/div), motor CMC (i_g) (yellow, **100mA/div**), and motor phase current (i_a) (blue, 2A/div) waveforms with only differential mode filter for SVPWM (M_i= 0.6) (time scale: 5ms/div).

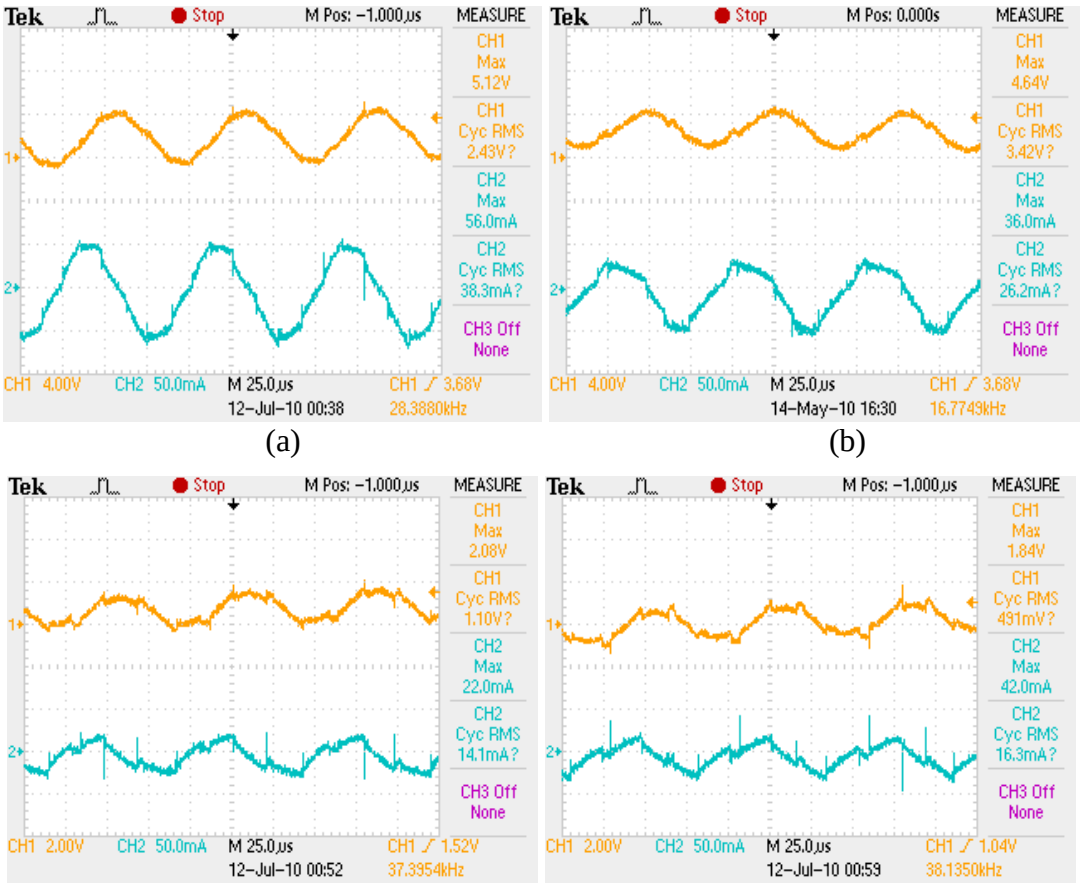


Figure 5.21 Motor shaft-to-frame voltage (yellow, 4V/div) and motor CMC (i_g) waveforms (blue, 50mA/div) with the differential mode filter and the CMI for (a) SVPWM, (b) DPWM1, (c) AZSPWM1, (d) NSPWM (M_i = 0.8) (time scale: 25us/div).

Finally, closing the i_{cm} (C_C-R_C) path, the PSF is connected. In Figure 5.22, the motor side experimental waveforms are shown when NSPWM is applied. The motor line-to-line terminal voltage v_{ab}, motor phase voltage v_{an}, and motor phase current i_a are sinusoidal as in the previous cases due to the differential mode filter. On the other hand, there is a significant improvement in shaft voltage and CMC reduction compared to the previous cases. Since C_C and R_C provide a low impedance path parallel to the motor, all the high frequency CMV appears on the CMI L_C, and it is eliminated for the motor. As a consequence, as seen in Figure 5.23, the shaft voltage is reduced to 500mV and the motor CMC i_g is nearly zero.

Thus, when PSF is included, the inverter drive becomes an ideal DC/AC converter in terms of its output (motor side) performance. Although the results are shown and discussed for NSPWM only, the results for the other discussed PWM methods are the same in terms of output performance. Therefore, they will not be repeated for the sake of brevity.

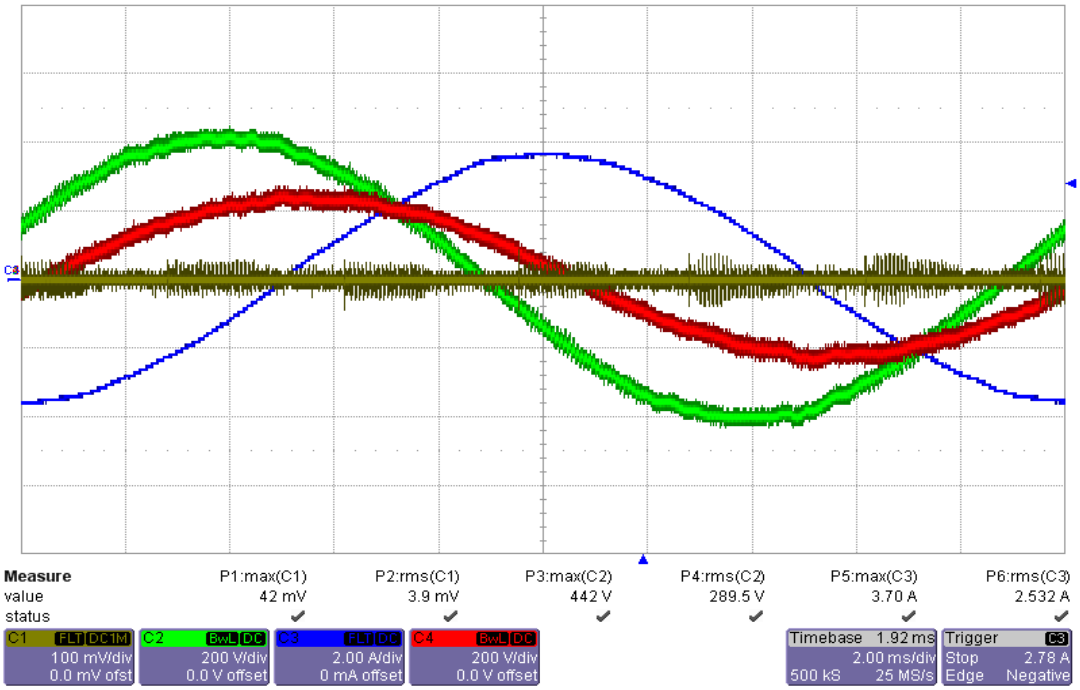


Figure 5.22 Motor phase voltage (v_{an}) (red, 200V/div), motor terminal voltage (v_{ab}) (green, 200V/div), motor phase current (i_a) (blue, 2A/div), motor CMC (i_g) (yellow, **100mA/div**) waveforms with the PSF for NSPWM (M_i = 0.8) (time scale: 2ms/div).

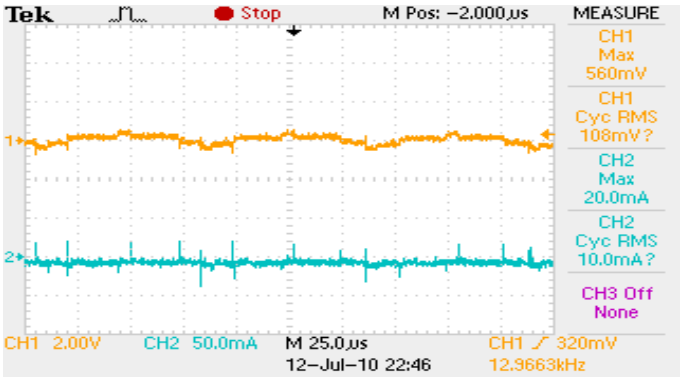


Figure 5.23 Motor shaft-to-frame voltage (yellow, 2V/div) and motor CMC (i_g) (blue, 50mA/div) with the PSF for NSPWM (M_i = 0.8) (time scale: 25us/div).

5.6.3 Inverter Side Performance of The Drive With PSF

After the motor side performance, the inverter side performance of the drive with PSF is evaluated. First, inverter output currents are investigated. While the PWM ripple at the motor current is eliminated, the inverter PWM current ripple increases due to the decrease of the output series inductance (7.3% motor leakage inductance vs. 2.5% L_D of PSF). As a result, the thermal stresses and acoustic noise are higher at the inverter with the differential mode filter compared to the case without any filter. The inverter peak to peak % current ripple values of the PWM methods for various M_i values are given in Table 5.4 and shown in Figures 5.24-5.25. Figures 5.26-5.29 show the inverter output current waveforms with PSF at M_i=0.6. Peak to peak current ripple is increased by approximately 4-5 times in all PWM methods compared to the case without any filter. AZSPWM1 has the highest PWM current ripple. DPWM1 and NSPWM have lower ripple than the others at high M_i. SVPWM has the lowest ripple at low M_i.

Table 5.4 Peak to peak ripple of inverter output current for various PWM methods

	M_i	peak to peak % ripple	
		without any filter	with PSF
SVPWM	0.4	10	37.5
	0.6	11.25	56.25
	0.8	12.5	68.75
AZSPWM1	0.4	20	125
	0.6	16.25	100
	0.8	15	87.5
DPWM1	0.6	10	56.25
	0.8	12.5	56.25
	0.9	7.5	56.25
NSPWM	0.6	12.5	75
	0.8	12.5	62.5
	0.9	7.5	56.25

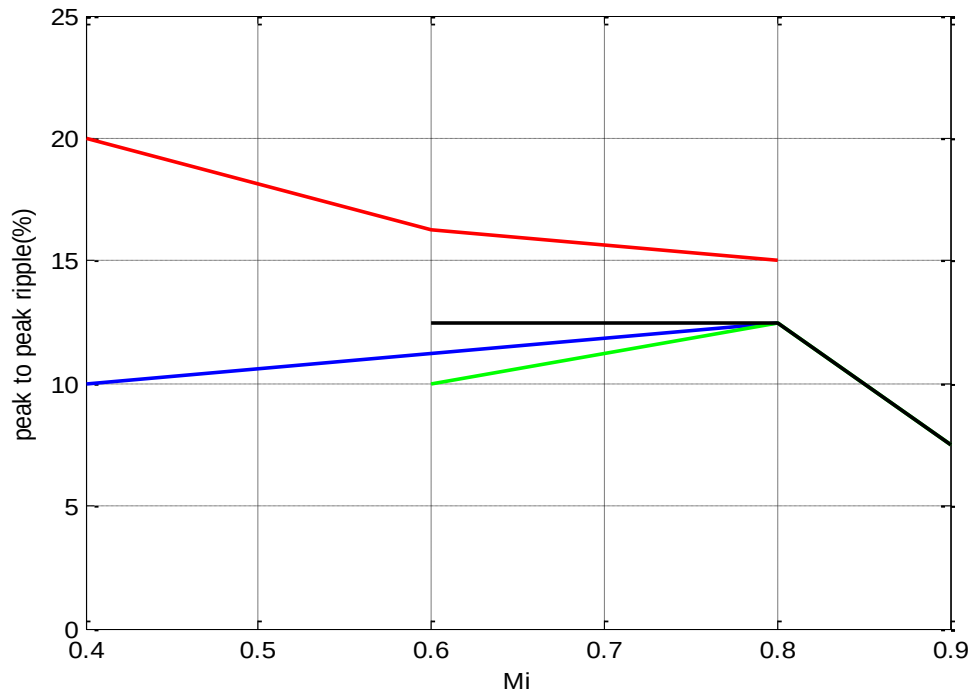


Figure 5.24 Peak to peak (%) ripple variation for SVPWM (blue), AZSPWM1 (red), DPWM1 (green), NSPWM (black) without any filter.

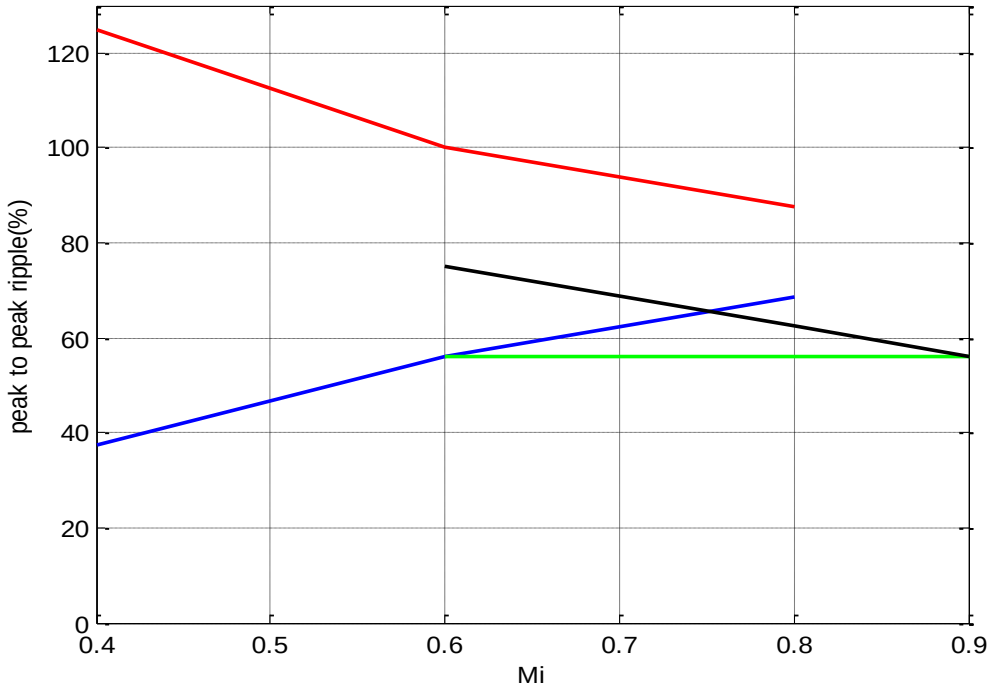


Figure 5.25 Peak to peak (%) ripple variation for SVPWM (blue), AZSPWM1 (red), DPWM1 (green), NSPWM (black) with PSF.

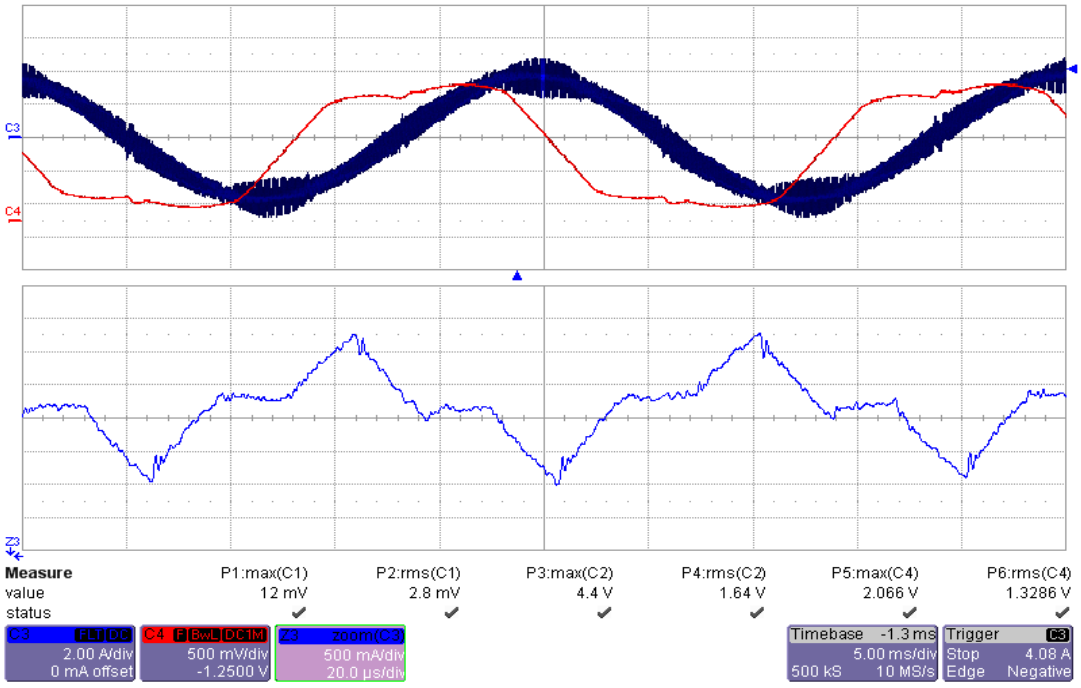


Figure 5.26 Inverter output current in 5ms/div scale (upper, blue) and 20us/div scale (lower, blue), and modulation waveform (upper, red) with PSF for SVPWM (M_i=0.6).

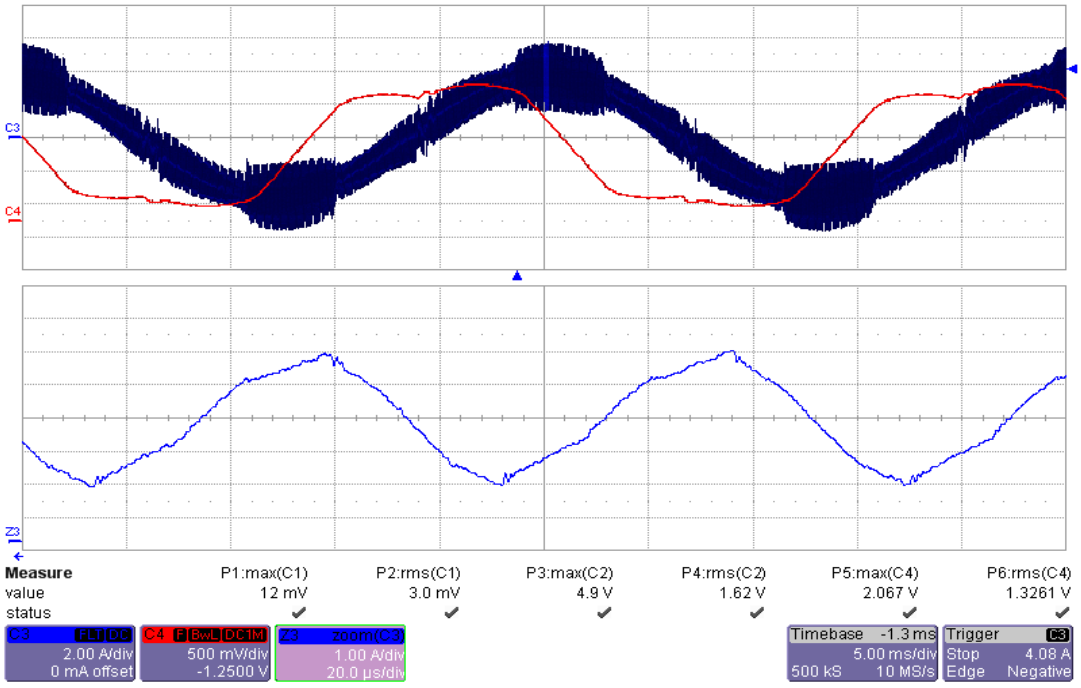


Figure 5.27 Inverter output current in 5ms/div scale (upper, blue) and 20us/div scale (lower, blue), and modulation waveform (upper, red) with PSF for AZSPWM1 (M_i=0.6).

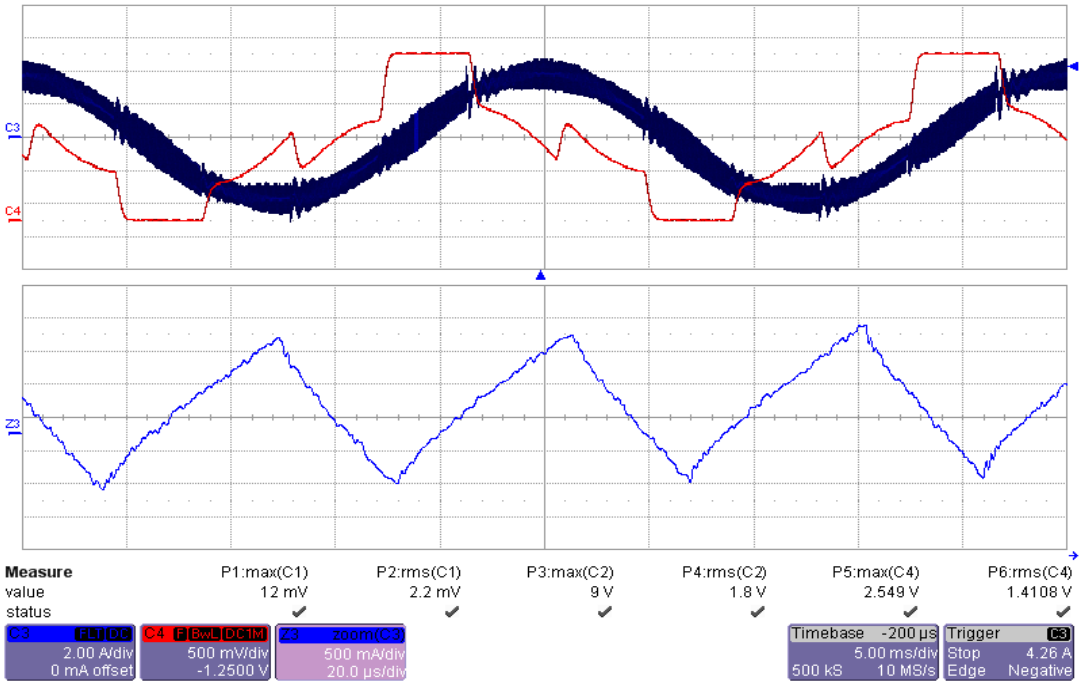


Figure 5.28 Inverter output current in 5ms/div scale (upper, blue) and 20us/div scale (lower, blue), and modulation waveform (upper, red) with PSF for DPWM1 (M_i=0.6).

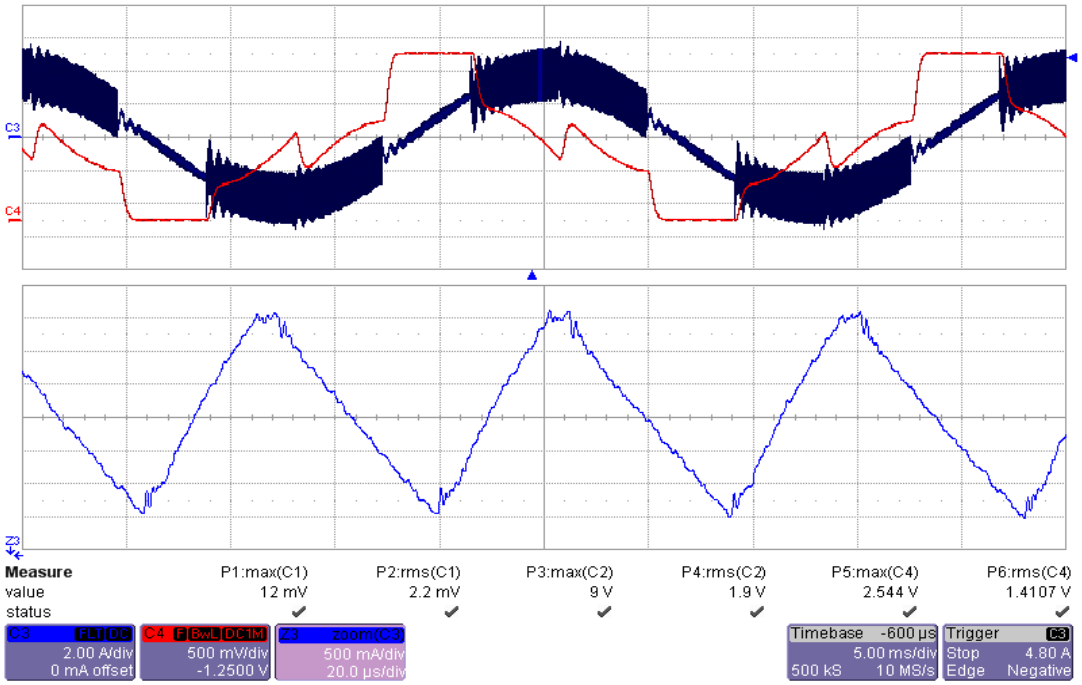


Figure 5.29 Inverter output current in 5ms/div scale (upper, blue) and 20us/div scale (lower, blue), and modulation waveform (upper, red) with PSF for NSPWM (M_i=0.6).

After the PWM current ripple performance, the filter CMC (i_{cm}) performances are investigated. SVPWM and AZSPWM1 are evaluated at low M_i (M_i=0.4) and DPWM1 and NSPWM are evaluated for higher M_i (M_i<0.6). Note that NSPWM is only valid for 0.6<M_i<0.907. DPWM1 and NSPWM methods are evaluated without and with ROCL.

Figures 5.30-5.31 show the inverter side phase current and capacitor C_C voltage and current waveforms for SVPWM and AZSPWM1, respectively. The PWM current ripple of both methods is very high compared to the motor without PSF case for the same reason as discussed above. The injected zero-sequence signal mainly appears across C_C. Since C_C provides a bypass path for the inverter CMC, the CMC through C_C is much higher than the CMC through the motor. Comparing SVPWM and AZSPWM1, the former has less PWM current ripple while the latter has less CMC. As seen in Figures 5.32-5.33, the inverter CMV magnitude is less in AZSPWM1 ($\pm V_{dc}/2$ vs. $\pm V_{dc}/6$), thus it has lower CMC (i_{cm}) than SVPWM. Figure 5.34 aids describing the difference between the CMC of these methods in one PWM cycle. Although the *dv/dt* of the inverter CMV is the same in both methods, the magnitude is less in AZSPWM1. Thus the peak and rms CMC values of C_C are significantly less in AZSPWM1. For both SVPWM and AZSPWM1, the peak CMC (i_{cm}) value is below 100mA and this current does not cause a problem for the drive.

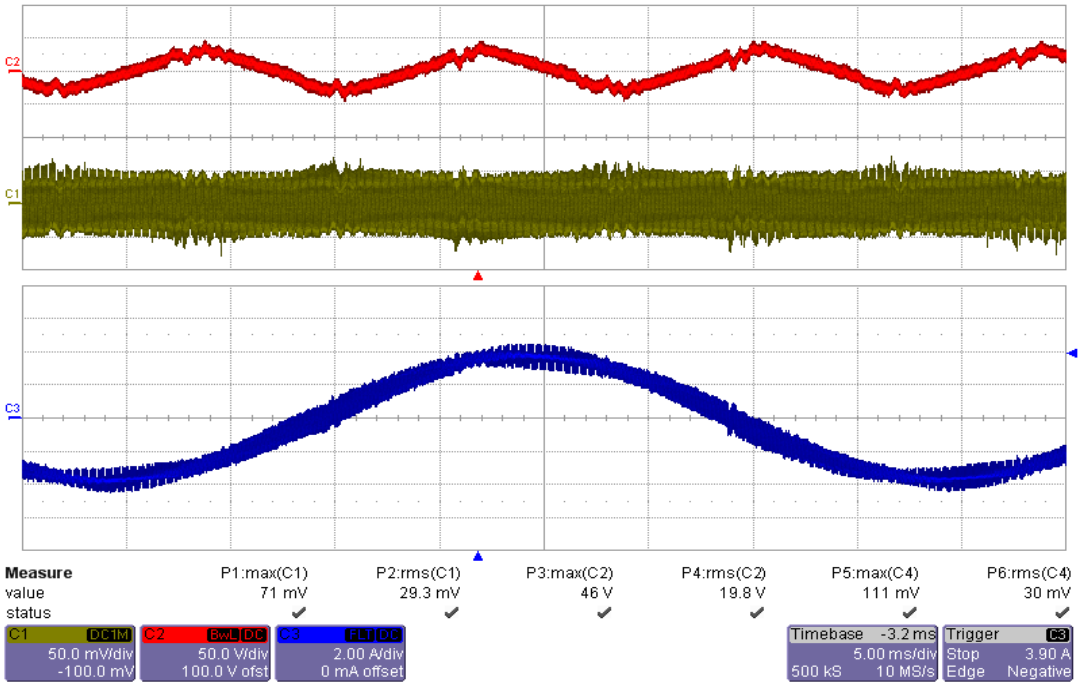


Figure 5.30 C_C voltage (red, 50V/div), filter CMC (i_{cm}) (yellow, **50mA/div**), and inverter output current (i_{inv}) (blue, 2A/div) waveforms with the PSF for SVPWM (M_i = 0.4) (time scale: 5ms/div).

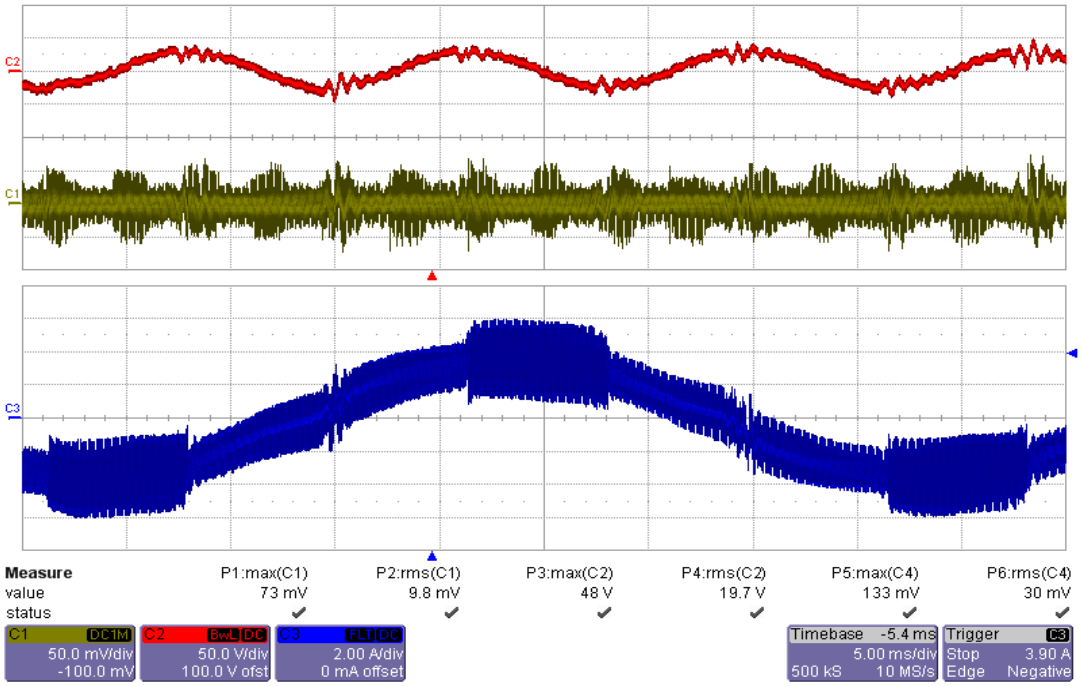


Figure 5.31 C_C voltage (red, 50V/div), filter CMC (i_{cm}) (yellow, **50mA/div**), and inverter output current (i_{inv}) (blue, 2A/div) waveforms with the PSF for AZSPWM1 (M_i = 0.4) (time scale: 5ms/div).

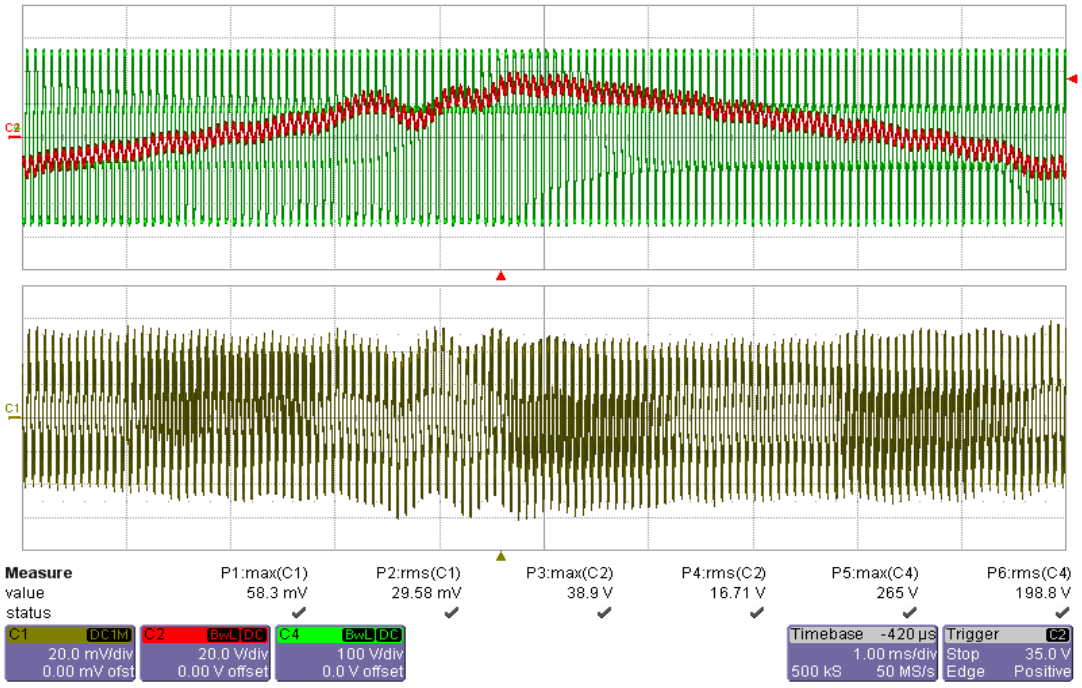


Figure 5.32 C_C voltage (red, 20V/div), inverter CMV (green, 100V/div), and filter CMC (i_{cm}) (yellow, **20mA/div**) waveforms with the PSF for SVPWM (M_i = 0.4) (time scale: 1ms/div).

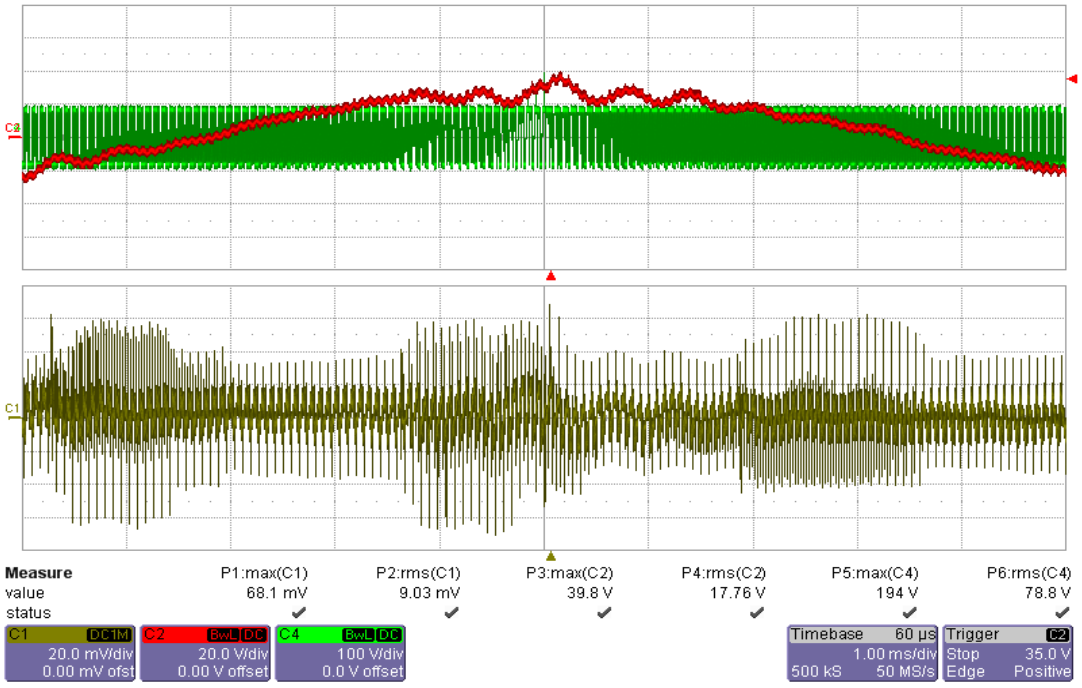
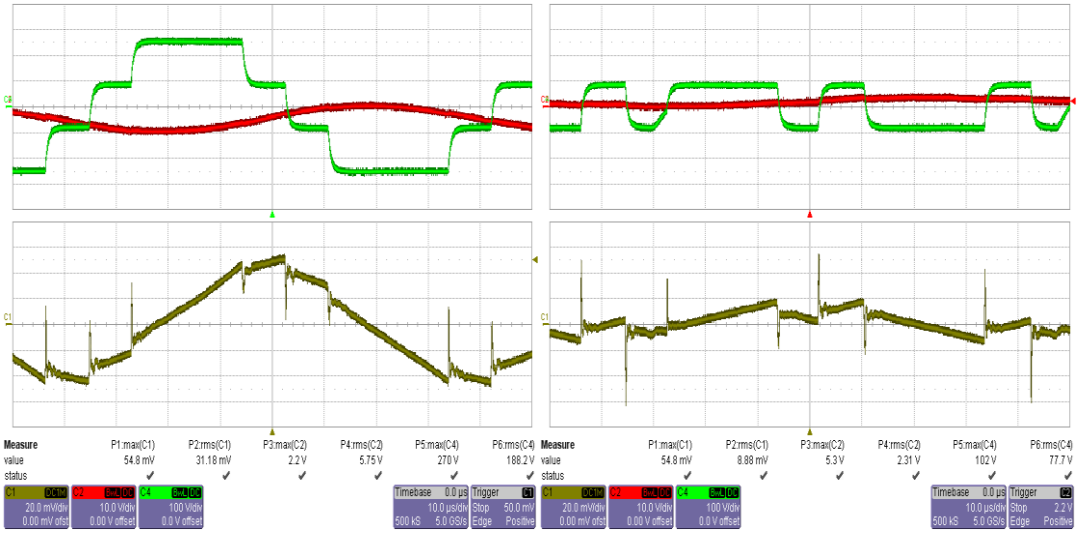


Figure 5.33 C_C voltage (red, 20V/div), inverter CMV (green, 100V/div), and filter CMC (i_{cm}) (yellow, **20mA/div**) waveforms with the PSF for AZSPWM1 (M_i = 0.4) (time scale: 1ms/div).



(a) (b)

Figure 5.34 C_C voltage (red, 10V/div), inverter CMV (green, 100V/div), and filter CMC (i_{cm}) (yellow, **20mA/div**) waveforms with the PSF for (a) SVPWM, (b) AZSPWM1 (M_i = 0.4) (time scale: 10us/div).

Figures 5.35-5.36 show the experimental results for DPWM1 and NSPWM, respectively for M_i=0.6 without ROCL. For the same reason as above, the PWM current ripple of the inverter for both methods is very high compared to the motor without PSF case. The injected zero-sequence signal appearing across C_C is discontinuously varying. As seen in Figures 5.37-5.38 in detail, during the narrow polarity change interval, large CMC (compared to the PWM frequency CMC) appearing as sharp needle flows through C_C. Note that the inverter CMV in DPWM1 is higher than that in NSPWM ($\pm V_{dc}/2$ vs. $\pm V_{dc}/6$). The microscopic view of the needle current is illustrated in Figure 5.39. Since the inverter CMV magnitude is less in NSPWM, the CMI core saturation is lower in NSPWM, and thus the peak CMC of C_C is significantly less in NSPWM (1A for NSPWM, 2A for DPWM1). While NSPWM operates only for M_i>0.6, and its peak CMC is 1A, for DPWM1 it is possible to decrease M_i and observe larger CMC than 2A. In the experiments this has been observed and frequent drive overcurrent trips occurred at very low M_i. These peak CMC values are comparable with the peak motor phase current of 4A. Thus, they should be reduced.

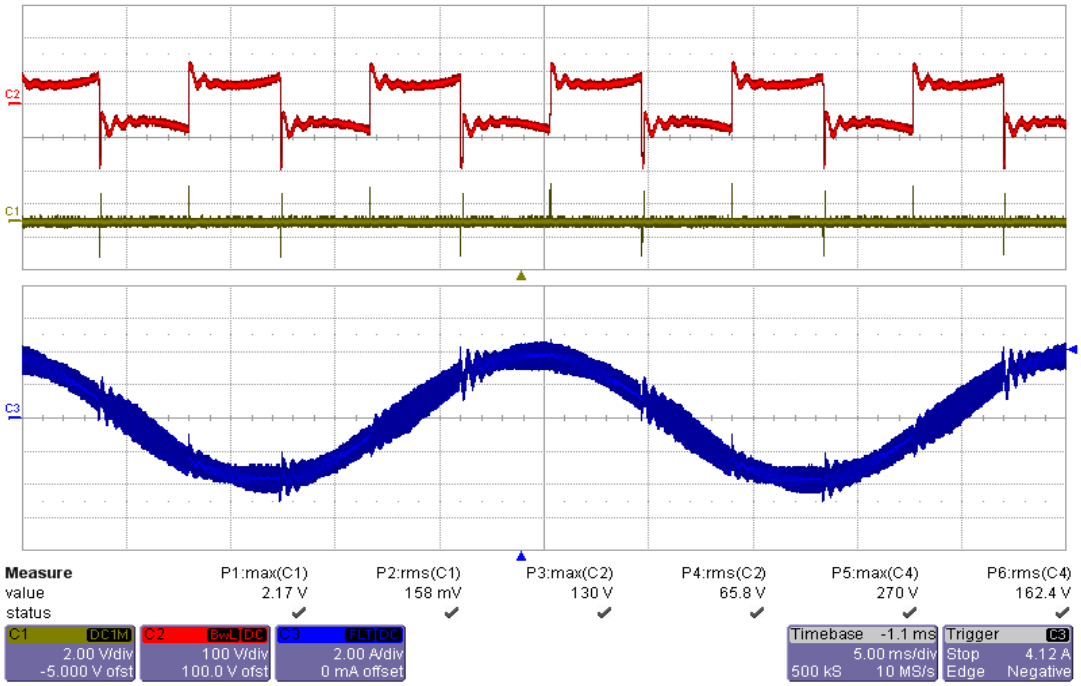


Figure 5.35 C_C voltage (red, **100V/div**), filter CMC (i_{cm}) (yellow, **2A/div**), and inverter output current (i_{inv}) (blue, 2A/div) waveforms with the PSF for DPWM1 without ROCL (M_i = 0.6) (time scale: 5ms/div).

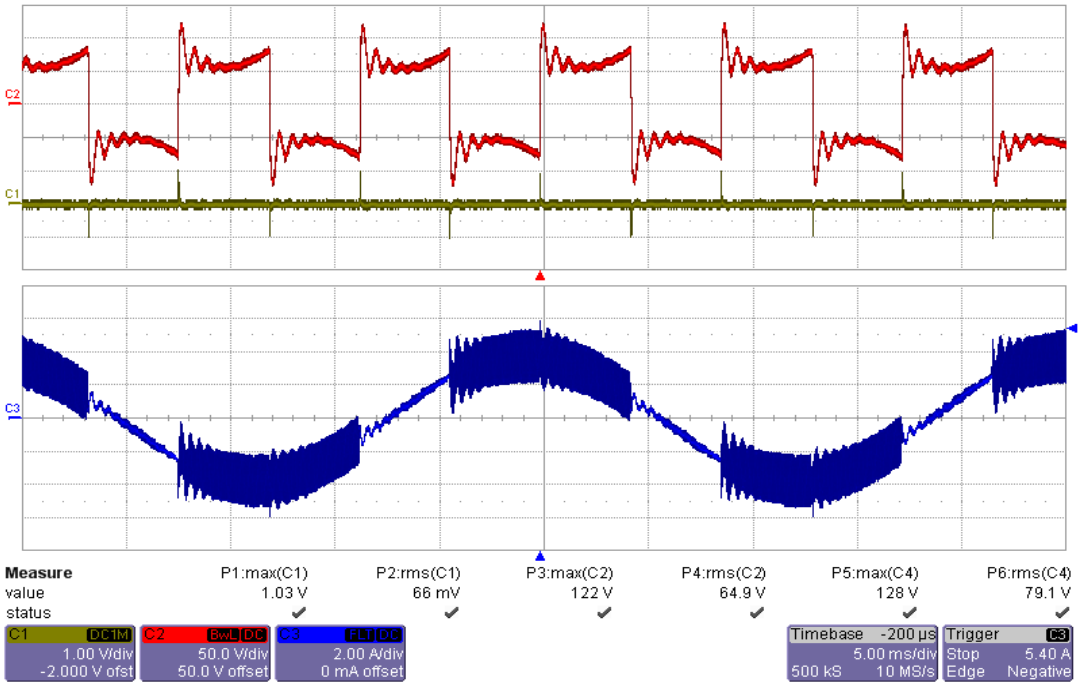


Figure 5.36 C_C voltage (red, **50V/div**), filter CMC (i_{cm}) (yellow, **1A/div**), and inverter output current (i_{inv}) (blue, 2A/div) waveforms with the PSF for NSPWM without ROCL (M_i = 0.6) (time scale: 5ms/div).

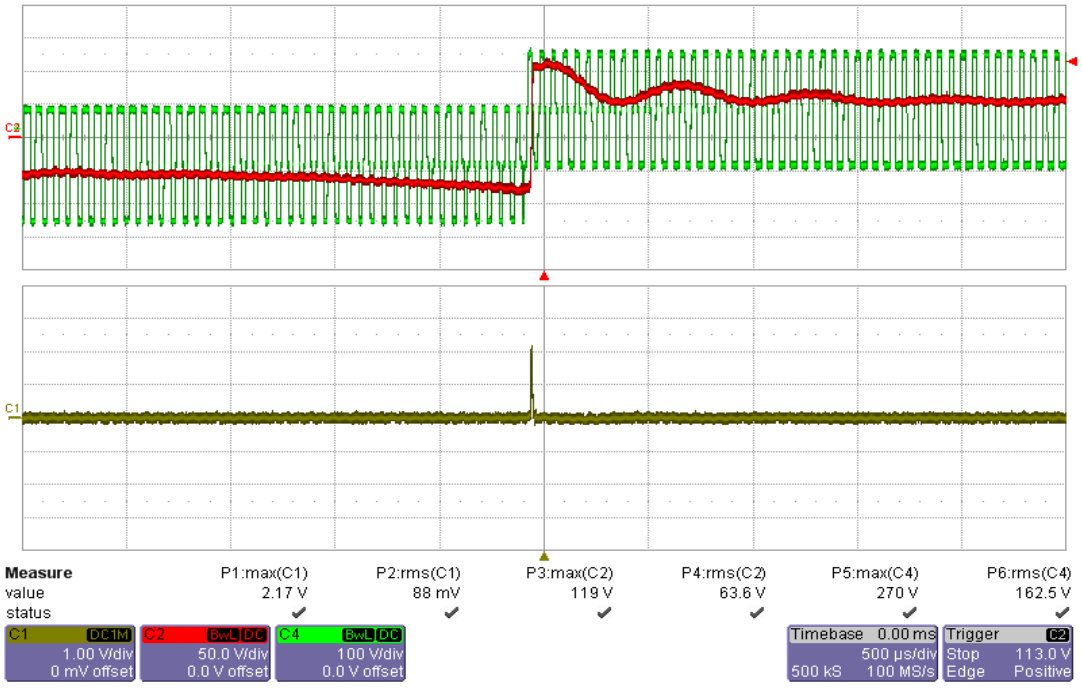


Figure 5.37 C_C voltage (red, 50V/div), inverter CMV (green, 100V/div), and filter CMC (i_{cm}) (yellow, **1A/div**) waveforms with the PSF for DPWM1 without ROCL (M_i = 0.6) (time scale: 500us/div).

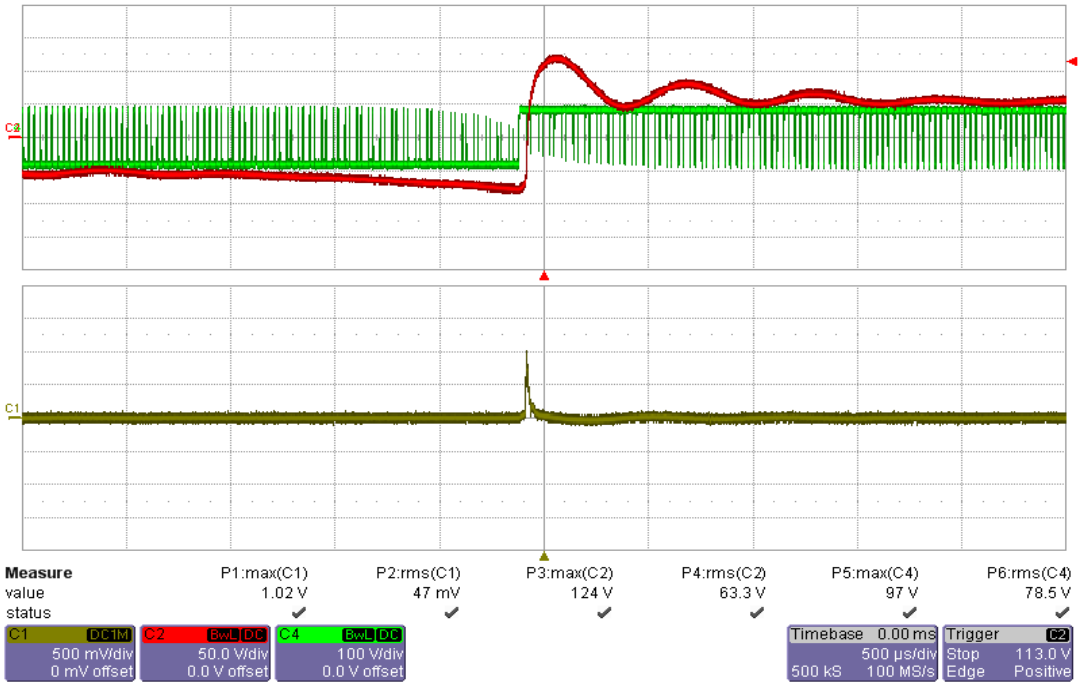
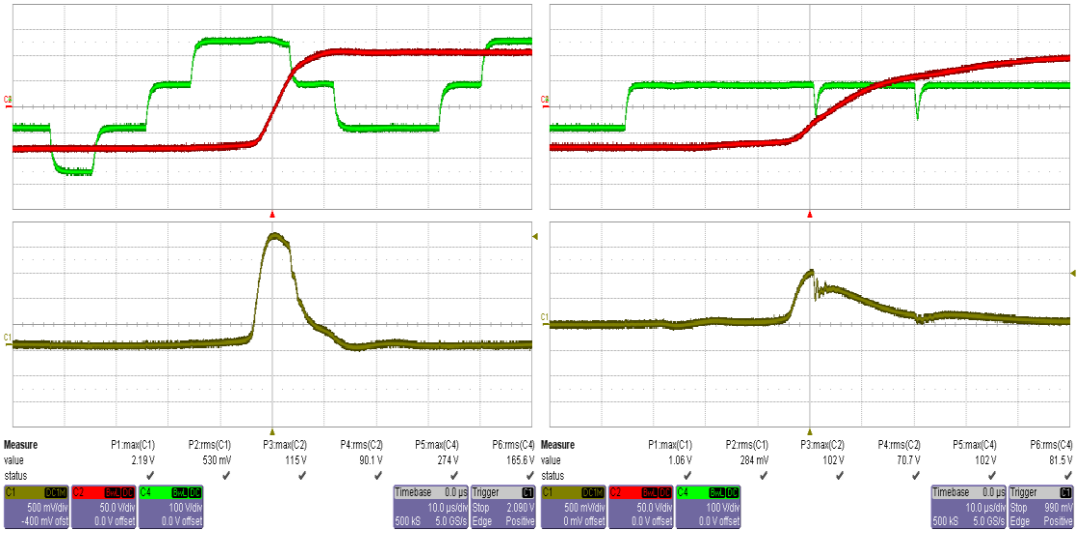


Figure 5.38 C_C voltage (red, 50V/div), inverter CMV (green, 100V/div), and filter CMC (i_{cm}) (yellow, **500mA/div**) waveforms with the PSF for NSPWM without ROCL (M_i = 0.6) (time scale: 500us/div).



(a) (b)

Figure 5.39 C_C voltage (red, 10V/div), inverter CMV (green, 100V/div), and filter CMC (i_{cm}) (yellow, **500mA/div**) waveforms with the PSF for (a) DPWM1, (b) NSPWM without ROCL (M_i = 0.6) (time scale: 10us/div).

In order to reduce the peak C_C current (i_{cm}) value (limit the peak to approximately 100mA), ROCL is applied to both DPWM1 and NSPWM. The ROCL is implemented in the digital signal processor as a discrete time block along with all the control and PWM functions described in the thesis. While (5.1) suggests a K_{vo} gain of 10^6, in the experimental system it could be selected as $0.3\text{x}10^6$ and $0.4\text{x}10^6$ for DPWM1 and NSPWM, respectively. This reduction is due to large *dv/dt* created by the L_C-C_C resonance. In DPWM1 lower K_{vo} is required than NSPWM due to higher CMI core saturation due to larger inverter CMV. As shown in Figures 5.40-5.41, when ROCL is applied, the slope of the zero-sequence signal (and thus the C_C voltage) is decreased to harmless levels and the magnitude of the peak i_{cm} is reduced to less than 100mA for both PWM methods. In Figures 5.42-5.43 inverter CMV, C_C voltage and i_{cm} waveforms are shown. As discussed in section 5.5, in the ROCL applied region (Δt) the pulse pattern of DPWM1 becomes identical to SVPWM, and the pulse pattern of NSPWM becomes identical to AZSPWM1. Thus, in the Δt interval, the inverter CMV changes between $\pm V_{dc}/2$ for DPWM1, and between $\pm V_{dc}/6$ for NSPWM, thus the PWM ripple and CMV characteristics do not change.

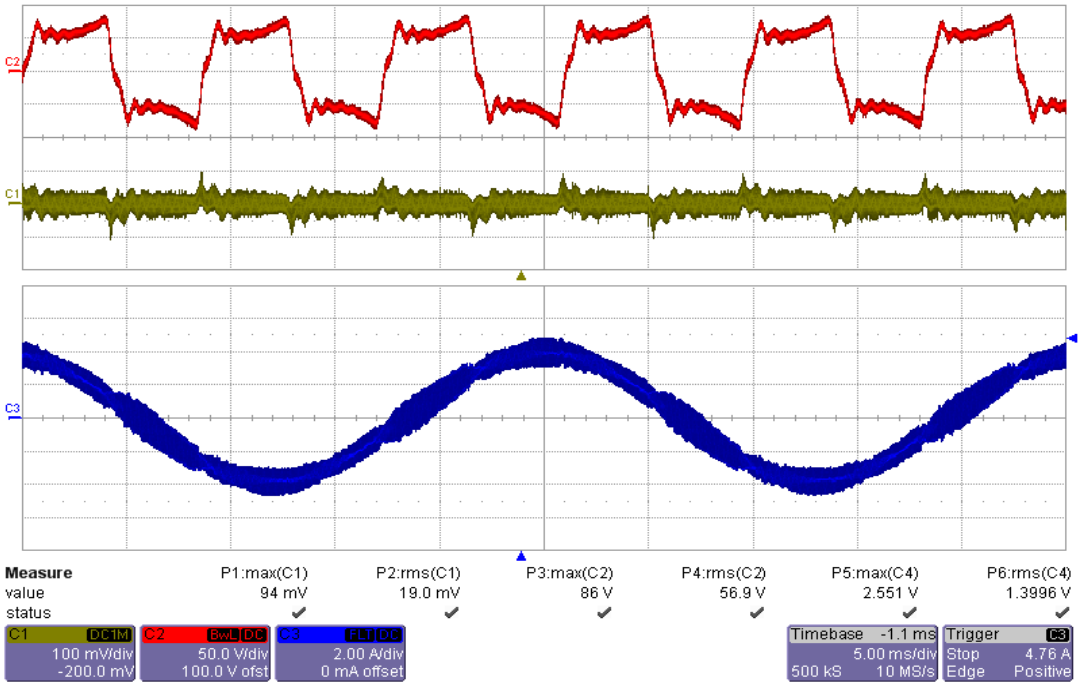


Figure 5.40 C_C voltage (red, 50V/div), filter CMC (i_{cm}) (yellow, **100mA/div**), and inverter output current (i_{inv}) (blue, 2A/div) waveforms with the PSF for DPWM1 with ROCL (M_i = 0.6) (time scale: 5ms/div).

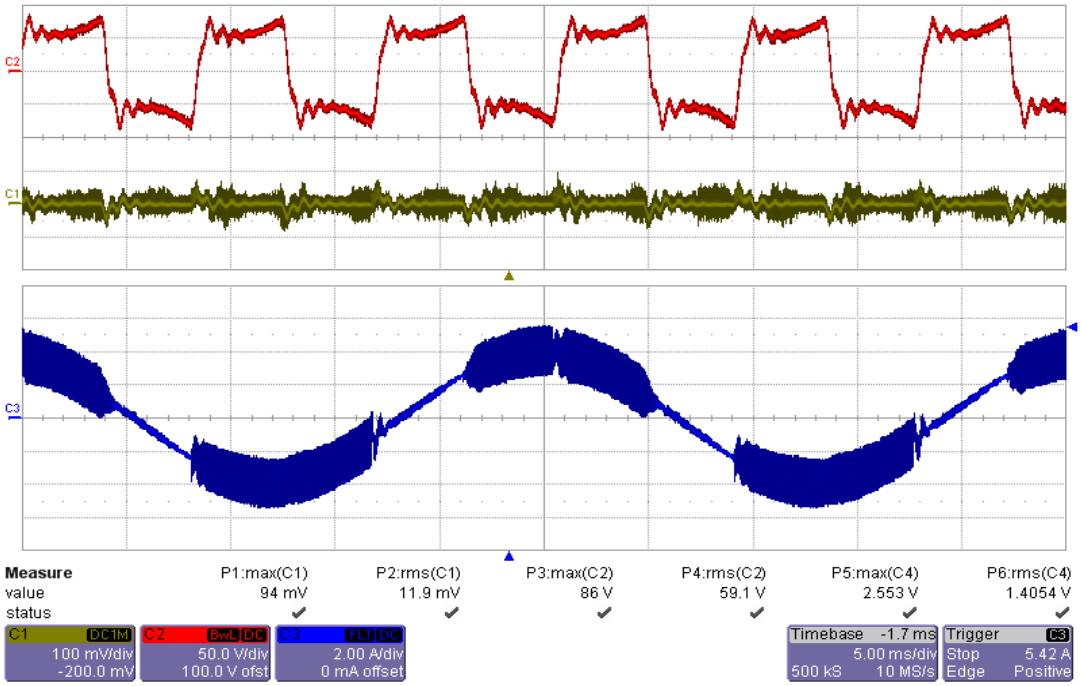


Figure 5.41 C_C voltage (red, 50V/div), filter CMC (i_{cm}) (yellow, **100mA/div**), and inverter output current (i_{inv}) (blue, 2A/div) waveforms with the PSF for NSPWM with ROCL (M_i = 0.6) (time scale: 5ms/div).

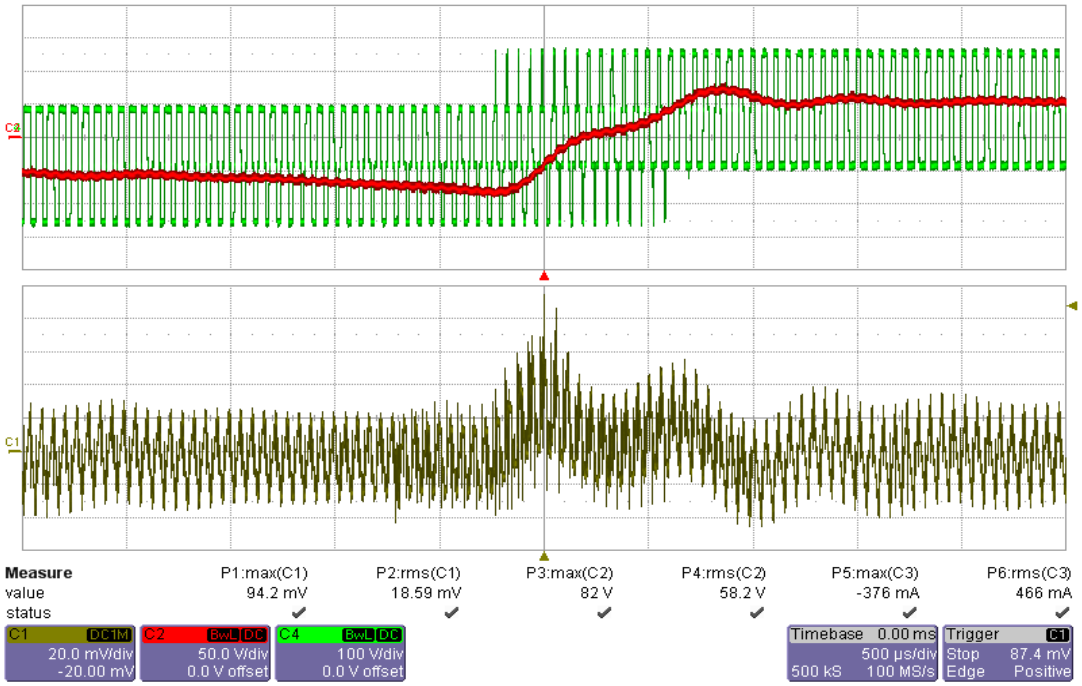


Figure 5.42 C_C voltage (red, 50V/div), inverter CMV (green, 100V/div), and filter CMC (i_{cm}) (yellow, **20mA/div**) waveforms with the PSF for DPWM1 without ROCL (M_i = 0.6) (time scale: 500us/div).

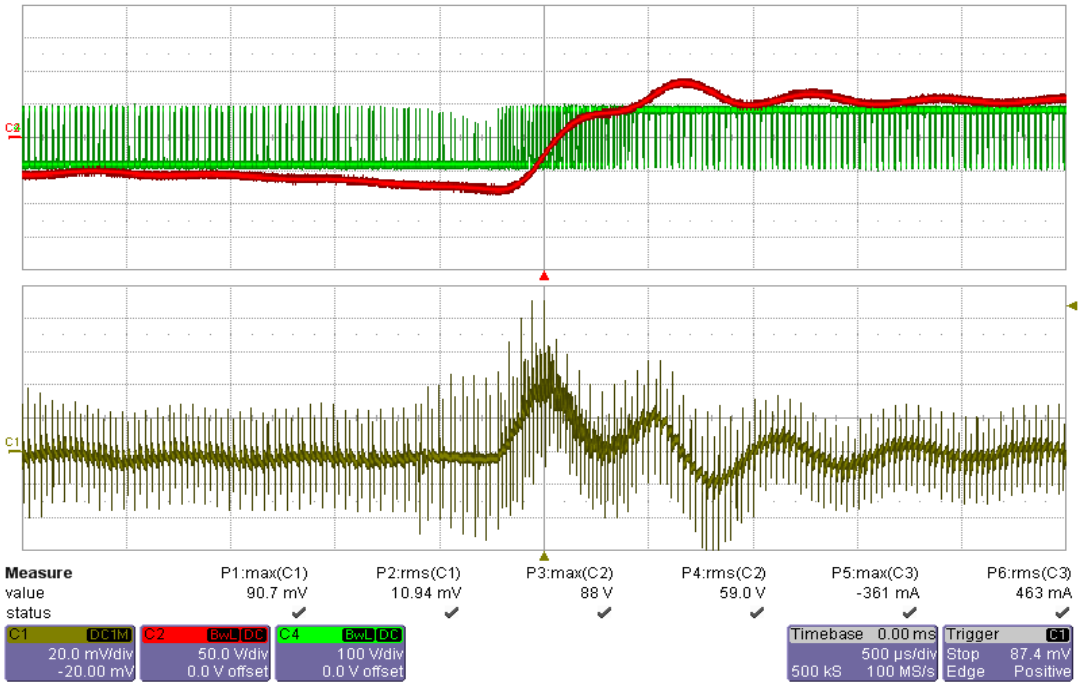
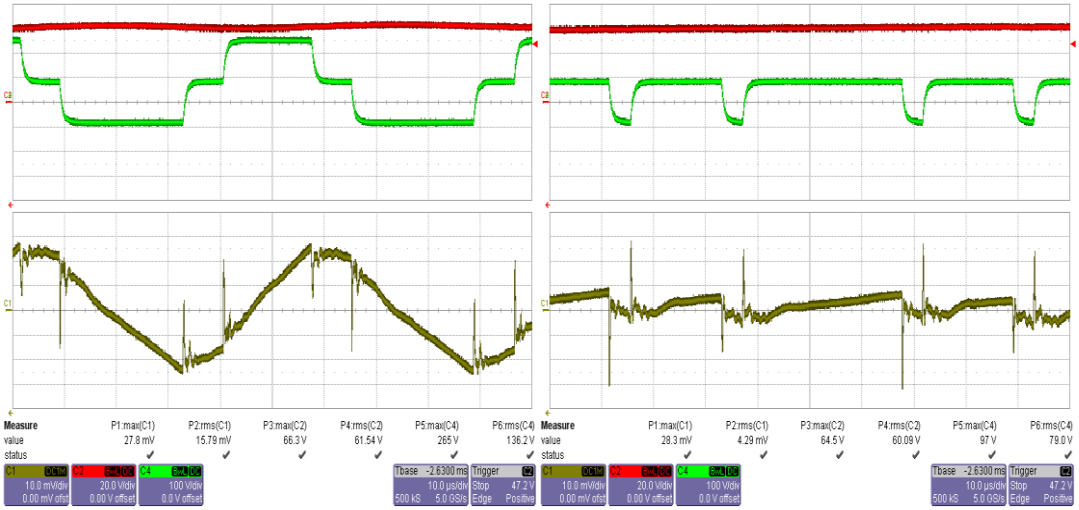


Figure 5.43 C_C voltage (red, 50V/div), inverter CMV (green, 100V/div), and filter CMC (i_{cm}) (yellow, **20mA/div**) waveforms with the PSF for NSPWM with ROCL (M_i = 0.6) (time scale: 500us/div).

Since the modulation wave discontinuity based CMC is suppressed, now the high frequency PWM based CMC becomes observable and dominant. As shown in Figure 5.44, the CMV magnitude of NSPWM is less and as a consequence CMC is less. Thus, the rms i_{cm} is significantly less in NSPWM compared to DPWM1. For M_i=0.6, as the worst case, the ROCL applied interval (Δt in Figure 5.8.a) is approximately 10° for DPWM1 and 7.5° for NSPWM in every 60° zero-sequence signal period. Thus, switching losses increase by about 9% for DPWM1, and 7% for NSPWM. As M_i increases the ROCL applied interval decreases and the loss increase becomes negligible. Figures 5.45-5.46 show the experimental waveforms for DPWM1 and NSPWM at M_i=0.9 and with ROCL. Since the zero-sequence signal varies smoothly, the ROCL unit is effectively bypassed. Thus, in this M_i range the i_{cm} is low and similar to the continuous PWM methods.

Table 5.5 summarizes the capacitor C_C voltage and current (i_{cm}) values for the considered PWM methods. In SVPWM and AZSPWM1, which have continuous modulation waves, the CMC (i_{cm}) is lower compared to discontinuous methods, DPWM1 and NSPWM. AZSPWM1 has lower rms CMC (i_{cm}) than SVPWM due to its lower CMV characteristics. DPWM1 and NSPWM have very high peak C_C voltage and current values without ROCL especially at low M_i. When ROCL is applied, the peak C_C voltage and current values are reduced significantly. Since NSPWM has lower CMV characteristics, its rms CMC (i_{cm}) is less than DPWM1.



(a) (b)

Figure 5.44 C_C voltage (red, 20V/div), inverter CMV (green, 100V/div), and filter CMC (i_{cm}) (yellow, **10mA/div**) waveforms with the PSF with ROCL for (a) DPWM1, (b) NSPWM (M_i = 0.6) (time scale: 10us/div).

Table 5.5 C_C voltage and current values for various PWM methods with PSF

		M_i	$V_{Cc,max}$(V)	$V_{Cc,rms}$(V)	$I_{Cc,max}$(mA)	$I_{Cc,rms}$(mA)
SVPWM		0.4	46	19.8	71	29.3
		0.6	61	28.8	67	22.3
		0.8	75	37.2	65	15.8
AZSPWM1		0.4	48	19.7	73	9.8
		0.6	64	28.9	60	7.8
		0.8	77	36.8	60	8.5
Without ROCL	DPWM1	0.6	200	65.8	2190	158
		0.8	61	17.3	624	37
		0.9	47	25.2	72	10
	NSPWM	0.6	122	64.9	1030	66
		0.8	72	17.9	470	29
		0.9	47	25.2	63	8.4
With ROCL	DPWM1	0.6	86	56.9	94	19
		0.8	38	12.2	70	14.3
		0.9	47	25.3	71	10
	NSPWM	0.6	86	59.1	94	11.9
		0.8	46	14.1	63	11.7
		0.9	46	25.4	64	8.1

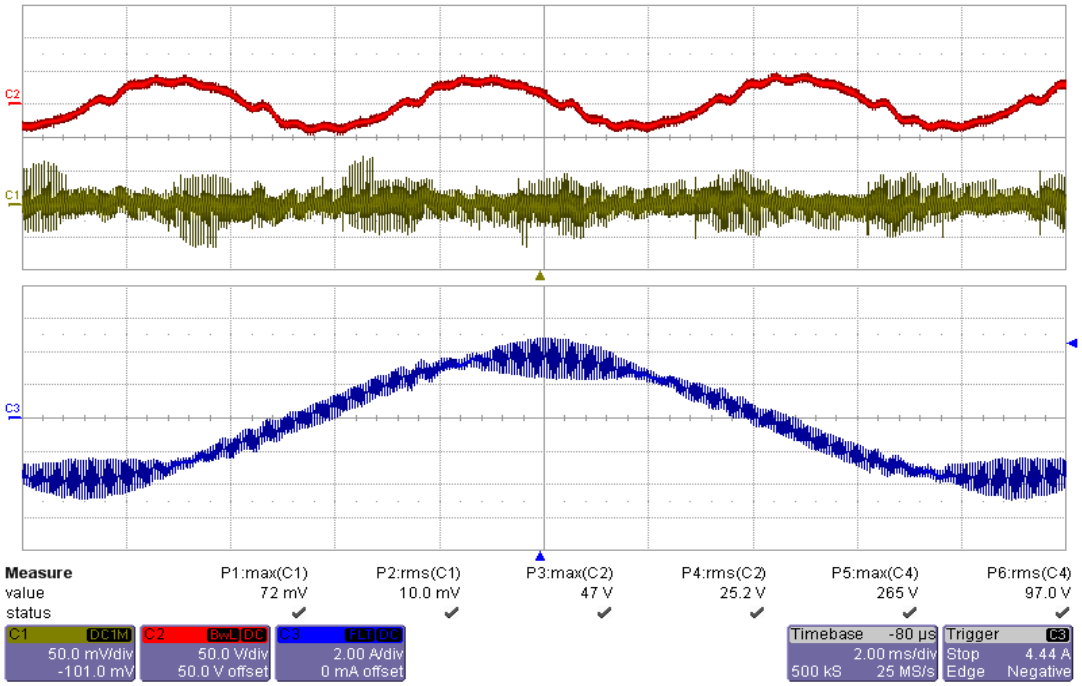


Figure 5.45 C_C voltage (red, 50V/div), filter CMC (i_{cm}) (yellow, **50mA/div**), and inverter output current (i_{inv}) (blue, 2A/div) waveforms without the PSF for DPWM1 with ROCL (M_i = 0.9) (time scale: 2ms/div).

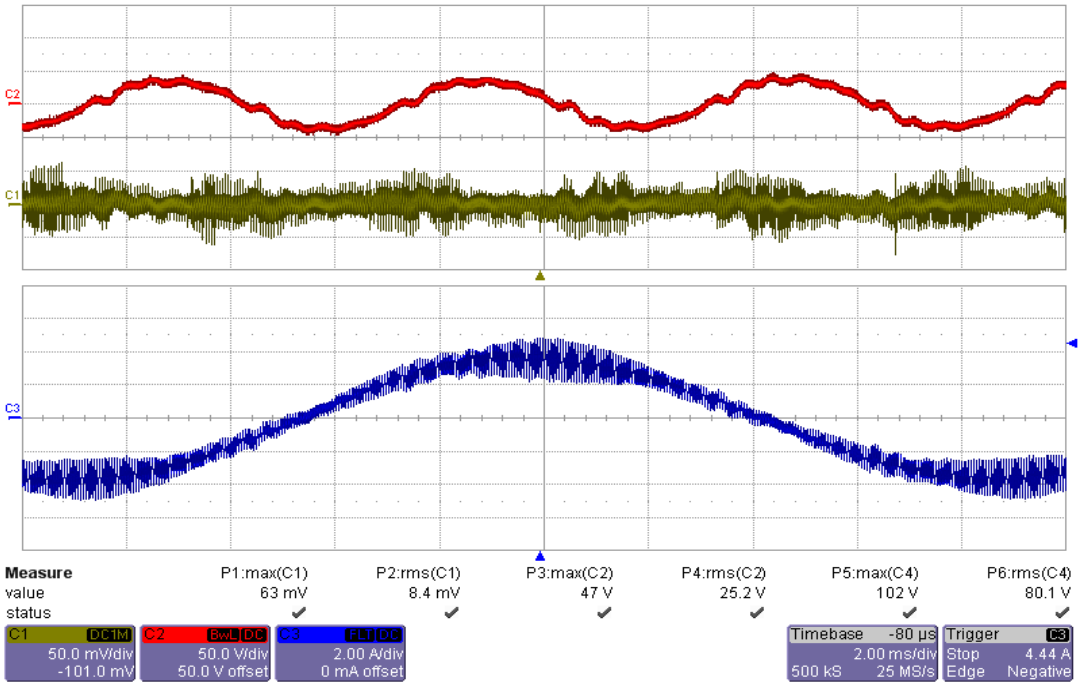


Figure 5.46 C_C voltage (red, 50V/div), filter CMC (i_{cm}) (yellow, **50mA/div**), and inverter output current (i_{inv}) (blue, 2A/div) waveforms without the PSF for NSPWM with ROCL (M_i = 0.9) (time scale: 2ms/div).

5.7 Summary

In this chapter the performance issues of inverter drives using the pure sine filter (PSF) along with advanced PWM methods have been investigated. It has been shown that, when employing advanced PWM methods with discontinuous modulation waves, the inverter common mode current may become excessive leading to significant overcurrent stresses in the inverter drive. The rate of change limiter (ROCL) method has been proposed for the purpose of smoothing the modulation waves during the discontinuity intervals. Thus, with the use of the ROCL method, the inverter common mode current could be suppressed to a predetermined finite value acceptable for the drive. The study is supported by analysis, simulations, and detailed experiments. The experimental results confirm the feasibility of the proposed method. Also the experiments illustrate the successful operation and benefit of employing the reduced CMV PWM methods in such applications.

CHAPTER 6

CONCLUSIONS

This thesis has mainly investigated the utilization of the advanced PWM techniques along with various passive output filters for three-phase, two-level inverters as applied to AC motor drives.

In chapter 2, the generalized scalar PWM implementation approach for three-phase, three wire VSIs has been established. Simple triangle intersection techniques are proposed for the implementation of the advanced PWM methods. The modulation waves of the most important PWM methods are generated, and comparing them with the comparator registers the switch signals are obtained. It has been shown that the conventional PWM methods and recently developed reduced common mode voltage (CMV) PWM methods could be easily implemented using this approach. The theory has been verified by laboratory experiments. Simple and successful implementation of various high performance PWM methods is illustrated for a motor drive.

In chapter 3, the undesired effects of PWM operation such as CMV, CMC, and bearing currents and their mitigation techniques have been reviewed extensively. The mitigation techniques have been investigated in two groups; mitigation from the source (inverter) and mitigation by inverter output filters. Mitigation from the source includes various PWM methods and inverter topologies. Inverter output filters include various passive and active filters. The most common mitigation techniques have been evaluated theoretically in terms of the mentioned undesired effects. Multi-level inverters and inverter output filters increase the system cost.

PWM pulse pattern modification is applied by software and it has no additional cost. Therefore, using a suitable PWM method reduces the cost of noise suppression.

In chapter 4, common mode voltage and common mode current reduction in the three-phase two-level inverters as applied to induction motor drives have been investigated in detail. The dependency of CMV and CMC on the PWM methods, common mode inductors, and the inverter topology has been investigated separately. The effects of the magnitude and *dv/dt* of the CMV on the CMC are separated. It is concluded that the peak CMC is mainly dependent on the *dv/dt* of the CMV and increases with increasing *dv/dt*. In the two-level VSI, typical peak CMC value is about 0.66A for both conventional and RCMV-PWM methods. On the other hand, it is observed that the CMV pulse pattern affects the worst case peak CMC noticeably. In conventional SVPWM and DPWM1 methods, consecutive CMV pulses with short time interval increase peak CMC up to 1.1A. Of the two successful RCMV-PWM methods, NSPWM and AZSPWM1, reduce peak CMC to about 0.7A even though the *dv/dt* of the CMV is the same. When the common mode inductor is inserted, while there is no improvement in the CMV reduction, the CMC is suppressed. Utilizing a successful CMI, the peak CMC is reduced by up to 86%. Nanocrystalline cores are more successful than the ferrite core in terms of CMC suppression. Since the cost of ferrite core is lower than that of nanocrystalline core, there is a trade-off between the CMC suppression and the cost of the magnetic core. Low-loss CMIs cause CMV and CMC to oscillate and they could not suppress rms CMC effectively. It has been observed that the high-loss cores are more successful than the low-loss cores in CMC reduction. The two-level VSI utilizing NSPWM and AZSPWM1 with CMI provides comparable results with the three-level NPC-VSI with CMI (124-128mA vs. 115mA of peak CMC with the most successful CMI). Since the cost of the two-level VSI is lower than the NPC-VSI, two-level VSI utilizing NSPWM and AZSPWM1 with a small size CMI provides optimum CMV/CMC suppression performance. It has also been shown that the relationship between the increasing common mode impedance and the decreasing peak CMC is approximately linear.

In chapter 5, the pure sine filter (PSF), which eliminates all high frequency components and provides sinusoidal voltages at the motor terminals, has been designed and implemented for a motor drive utilizing advanced PWM methods. When no filter is connected, the motor current includes 10-20% PWM ripple, the shaft voltage reaches 10V, and the motor CMC reaches 1A. When PSF is connected, motor terminal voltages become sinusoidal and the PWM ripple on the motor current is eliminated. The shaft voltage is reduced to about 500mV, and the motor CMC is nearly zero. As a result, it has been shown that PSF solves all the PWM originated problems at the motor side effectively. Therefore, when PSF is connected, the inverter drive becomes an ideal DC-AC converter in terms of motor (load) performance. However, utilizing PSF along with zero-sequence signal injecting PWM methods causes a low frequency common mode current circulating through the inverter and PSF. When the continuous PWM methods, SVPWM and AZSPWM1, are utilized, the low frequency the CMC is negligible compared to high frequency CMC. The peak CMC is below 100mA and it does not cause a problem for the drive. On the other hand, utilizing PSF along with the discontinuous PWM methods, DPWM1 and NSPWM, results in extremely high CMC in the inverter. It exceeds 2A for DPWM1 and 1A for NSPWM. These CMC values are comparable with the motor peak phase current (4A), and they increase the inverter current stresses. The rate of change limiter approach has been proposed to solve this problem. Using the ROCL method, the inverter common mode current has been suppressed to 100mA level which is acceptable for the drive. The number of switching increases by about 9% for DPWM1, and 7% for NSPWM at worst case. As M_i increases the loss increase becomes negligible. The study is supported by analysis, simulations, and detailed experiments. The experimental results confirm the feasibility of the proposed method.

Overall, this thesis includes the simple scalar implementation of the high performance advanced PWM methods for AC motor drives and utilization of these PWM methods along with the common mode inductor and the pure sine filter.

As future work, the motor bearing currents should be measured and the effects of reduced common mode voltage PWM methods on the bearing current reduction should be investigated. The high frequency model of the induction motor could be included and the relationship between the common mode impedance and CMV and CMC could be investigated theoretically and experimentally in detail. The size of the pure sine filter could be decreased by increasing PWM switching frequency, and it could be packed together with the inverter. Thus, a compact ideal DC-AC converter could be obtained.

REFERENCES

[1] J. Holtz, “Pulsewidth Modulation for Electronic Power Conversion,”.

[2] J. Holtz, “Pulsewidth Modulation – A Survey,”.

[3] A.M. Hava, R.J. Kerkman, and T.A. Lipo, “Simple analytical and graphical methods for carrier-based PWM-VSI drives,” *IEEE Trans. on Power Electron.*, vol. 14, no: 1, pp. 49 – 61. Jan. 1999.

[4] A. Schönung and H. Stemmler, “Static frequency changers with subharmonic control in conjunction with reversible variable speed ac drives,” *Brown Boveri Rev.*, Sept. 1964, pp. 555–577.

[5] H.V.D. Broeck, H. Skudelny, and G. Stanke, “Analysis and realization of a pulse width modulator based on voltage space vectors,” in *Conf. Rec. IEEE IAS Annu. Meeting*, 1986, pp. 244–251.

[6] M. Depenbrock, “Pulse width control of a 3-phase inverter with nonsinusoidal phase voltages,” in *IEEE-ISPC Conf. Rec.*, pp. 399–403, 1977.

[7] Y.S. Lai and F.S. Shyu, “Optimal common-mode voltage reduction PWM technique for inverter control with consideration of the dead-time effects-part I: basic development,” *IEEE Trans. on Ind. Applicat.*, vol 40, no. 6, pp.1605 – 1612, November-December 2004.

[8] E. Ün and A.M. Hava, "A near state PWM method with reduced switching frequency and reduced common mode voltage for three-phase voltage source inverters," *IEEE Trans. Ind. Applicat.,* vol. 45, no. 2, pp. 782-793. Mar./Apr. 2009.

[9] J.M. Erdman, R.J. Kerkman, D.W. Schlegel, and G.L. Skibinski, "Effect of PWM inverters on AC motor bearing currents and shaft voltages," *IEEE Trans. Ind. Applicat.*, vol. 32, pp. 250-259, March-April 1996.

[10] A. Muetze and A. Binder, "Don't lose your bearings – mitigation techniques for bearing currents in inverter-supplied drive systems," *IEEE Ind. Applicat. Magazine,* vol. 12, no. 4, pp. 22-31, July-August 2006.

[11] G.L. Skibinski, R.J. Kerkman, and D. Schlegel, "EMI emissions of modern PWM AC drives," *IEEE Ind. Applicat. Mag.,* vol. 5, no. 6, pp. 47–81, Nov./Dec. 1999.

[12] A. Muetze and A. Binder, "High Frequency Ground Currents of Inverter-Fed Squirrel-Cage Induction Motors up to 500 kW," Proc. 10th European Conference on Power Electronics and Applications (EPE), Toulouse, 2003.

[13] N. Hanigovszki, J. Landkildehus, and F. Blaabjerg, "Output filters for AC adjustable speed drives," pp. 236-242 *IEEE-APEC 2007 Conf.,* California, pp. 236-242, February 25 – March 1 2007.

[14] R.J. Kerkman, D. Leggate, and G.L. Skibinski, "Interaction of drive modulation and cable parameters on AC motor transients," *IEEE Trans. Ind. Applicat.*, vol. 33, no 3, pp. 722 – 731, May-June 1997.

[15] MTE Corporation, *Line/Load Reactors, Technical User Manuals*, 2006.

[16] Y. Murai, T. Kubota, and Y. Kawase, "Leakage current reduction for a high-frequency carrier inverter feeding an induction motor," *IEEE Trans. on Ind. Applicat.*, vol. 28, pp. 858-863, July/Aug. 1992.

[17] S. Ogasawara and H. Akagi, "Modeling and damping of high-frequency leakage currents in PWM inverter-fed AC motor drive systems," *IEEE Trans. on Ind. Applicat*., vol 32, no 5, pp. 1105-1114, September-October 1996.

[18] D.A. Rendusara and P.N. Enjeti, "An improved inverter output filter configuration reduces common and differential modes dv/dt at the motor terminals in PWM drive systems," *IEEE Trans. Power Electron.*, vol. 13, pp. 1135-1143, Nov. 1998.

[19] G.L. Skibinski, "Design methodology of a cable terminator to reduce reflected voltage on AC motors," in *Conf. Rec. IEEE IAS Annu. Meeting*, San Diego, CA, Oct. 1996, pp. 153–161.

[20] H. Akagi, H. Hasegawa, and T. Doumoto, "Design and performance of a passive EMI filter for use with a voltage-source PWM inverter having sinusoidal output voltage and zero common-mode voltage," *IEEE Trans. on Power Electron.,* vol 19, pp. 1069-1076, July 2004.

[21] H. Akagi and T. Doumoto, "An approach to eliminating high-frequency shaft voltage and ground leakage current from an inverter-driven motor," *IEEE Trans. on Ind. Applicat.*, vol. 40, pp. 1162 – 1169, July/August 2004.

[22] H. Akagi and S. Tamura, "A passive EMI filter for eliminating both bearing current and ground leakage current from an inverter-driven motor," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1459–11469, Sep. 2006.

[23] S. Ogasawara, H. Ayano, and H. Akagi, "An active circuit for cancellation of common-mode voltage generated by a PWM inverter," *IEEE Trans. on Power Electron.,* vol 13, pp. 835-841, September 1998.

[24] A. Kempski, R. Smolenski, E. Kot, and Z. Fedyczak, "Active and passive series compensation of common mode voltage in adjustable speed drive system," *IAS Annual Meeting, IAS'04.* pp 2665-2671 October 2-7 2004.

[25] C. Mei, J.C. Balda, and W.P. Waite, "Cancellation of common-mode voltages for induction motor drives using active method," *IEEE Trans. on Energy Conversion*, vol. 21, no 2, pp. 380 – 386. June 2006.

[26] A. Nabae, I. Takahashi, and H. Akagi, "A new Neutral-Point-Clamped PWM inverter," *IEEE Trans. on Ind. Applicat.,* vol.17, pp. 518-523, September/October 1981.

[27] Y.Y. Tzou, H.J. Hsu, and T.S. Kuo, "FPGA-based SVPWM control IC for 3-phase PWM inverter", *Proc. IEEE Int. Conf. Ind. Electron., Control and Instrum.,* vol. 1, pp. 138 1996.

[28] D.W. Chung, J.S. Kim, and S.K. Sul, "Unified voltage modulation technique for real-time three-phase power conversion", *IEEE Trans. Ind. Applicat.*, vol. 34, pp. 374 1998.

[29] D.C. Lee and G.M. Lee, "A novel overmodulation technique for space-vector PWM inverters", *IEEE Trans. Power Electron.*, vol. 13, pp. 1144 1998.

[30] A.R. Bakhshai, G. Joos, P.K. Jain, and J. Hua, "Incorporating the overmodulation range in space vector pattern generators using a classification algorithm," *IEEE Trans. Power Electron.*, vol. 15, no. 1, pp. 83–91, Jan. 2000.

[31] Z. Shu , J. Tang , Y. Guo and J. Lian, “An efficient SVPWM algorithm with low computational overhead for three-phase inverters”, *IEEE Trans. Power Electron.,* vol. 22, pp. 1797 2007.

[32] A. Cataliotti, F. Genduso, A. Raciti, and G.R. Galluzzo, “Generalized PWM–VSI control algorithm based on a universal duty-cycle expression: Theoretical analysis, simulation results, and experimental validations,” *IEEE Trans. Ind. Electron.*, vol. 54, pp. 1569 2007.

[33] J. Zitzelberger and W. Hofmann, “Reduction of bearing currents in inverter fed drive applications by using sequentially positioned pulse modulation”, *EPE J.*, vol. 14, pp. 2004.

[34] M. Cacciato, A. Consoli, G. Scarcella, and A. Testa, “Reduction of common-mode currents in PWM inverter motor drives,” *IEEE Trans. on Industry Applications,* vol. 35, no 2, pp. 469 – 476, March-April 1999.

[35] A.M. Hava and E. Ün, “Performance analysis of reduced common mode voltage PWM methods and comparison with standard PWM methods for three-phase voltage source inverters,’’ *IEEE Trans. Power Electron.*, vol. 24, no. 1, pp. 241–252, Jan. 2009.

[36] D.G. Holmes, “The significance of zero space vector placement for carrier-based PWM schemes”, *IEEE Trans. Ind. Applicat.*, vol. 32, pp. 1122 - 1129, 1996.

[37] V. Blasko, “Analysis of a hybrid PWM based on modified space-vector and triangle-comparison methods", *IEEE Trans. Ind. Applicat.*, vol. 33, pp. 756 1997.

[38] A.M. Hava, R.J. Kerkman, and T.A. Lipo, "A high performance generalized discontinuous PWM algorithm," *IEEE Trans. Ind. Applicat.*, vol. 34, pp. 1059, 1998.

[39] A.M. Hava, S. Sul, R.J. Kerkman, and T.A. Lipo, "Dynamic overmodulation characteristics of triangle intersection PWM methods", *IEEE Trans. Ind. Applicat.*, vol. 35, pp. 896 1999.

[40] A.M. Hava, R.J. Kerkman, and T.A. Lipo, "Carrier-based PWM-VSI overmodulation strategies: Analysis, comparison and design", *IEEE Trans. Power Electron.*, vol. 13, pp. 674 1998.

[41] N.O. Çetin and A.M. Hava, "Scalar PWM Implementation Methods for Three-phase Three-wire Inverters," ELECO 2009, 6th International Conference on Electrical and Electronics Engineering, 5-8 November 2009, Bursa, Turkey, pp. 447-451.

[42] C.C. Hou and P.T. Cheng, "A multi-carrier pulse width modulator for the auxiliary converter and the diode rectifier," *in Conf. Rec. IEEE PEDS 2009*, pp. 393-398.

[43] R.M. Tallam, R.J. Kerkman, D. Leggate and R.A. Lukaszewski, "Common-Mode Voltage Reduction PWM Algorithm for AC Drives," in *IEEE ECCE 2009 Conf. Rec.* 2009, pp. 3660-3667.

[44] E. Ün and A.M. Hava, "A High Performance PWM Algorithm for Common Mode Voltage Reduction in Three-phase Voltage Source Inverters," in *IEEE-PESC 2008 Conference, June 15-19 2008, Rhodes, Greece*, pp. 1528-1534.

[45] Texas Instruments, *TMS320x28xx, 28xxx Enhanced Pulse Width Modulator (EPWM) Module Reference Guide*, SPRU791D, November 2004– Revised October 2007.

[46] S. Chen, T.A. Lipo, and D. Fitzgerald, "Modeling of motor bearing currents in PWM inverter drives," *IEEE Trans. on Ind. Applicat.*, vol 32, pp. 1365-1370, November-December 1996.

[47] A. Consoli, G. Oriti, A. Testa, and A.L. Julian, "Induction motor modeling for common mode and differential mode emission evaluation," *IAS Annual Meeting, IAS'96*, pp. 595 – 599, October 6-10 1996.

[48] A. Muetze and A. Binder, "Techniques for measurement of parameters related to inverter-induced bearing currents," *IEEE Trans. Ind. Applicat.*, vol. 43, no. 5, pp. 1274–1283, Sep./Oct. 2007.

[49] A. Binder and A. Mütze, "Scaling effects of inverter-induced bearing currents in AC machines," *IEEE-IEMDC Conf.*, Antalya, pp. 1477-1483, May 2-5, 2007.

[50] A. Muetze and B.S. Heng, "Performance of Common-Mode Chokes," *IEEE Ind. Applicat. Magazine*, vol. 16, no. 2, pp. 31-38, Mar. /Apr. 2010.

[51] A. Muetze, ''Scaling issues for common mode chokes to mitigate ground currents in inverter-based drive systems,'' *IEEE Trans. Ind. Applicat.*, vol. 45, no. 1, pp. 286–294, Jan./Feb. 2009.

[52] Y.C. Son and S.K. Sul "A new active common-mode EMI filter for PWM inverter" *IEEE Trans. on Power Electronics*, vol 18, pp. 1309-1314, November 2003.

[53] H.J. Kim, H.D. Lee, and S.K. Sul, "A new PWM strategy for common-mode voltage reduction in neutral-point-clamped inverter-fed AC motor drives," *IEEE Trans. Ind. Applicat.*, vol. 37, no. 6, pp. 518–523, Nov./Dec. 2001.

[54] B. Üstüntepe and A.M. Hava, "Üç-fazlı üç-düzeyli nötr Noktası bağlantılı evirici ve uygulamaları," *ELECO 2006, Elektrik-Elektronik-Bilgisayar Mühendisliği Sempozyumu,* Bursa, sayfa 126-130, 6-10 Aralık 2006.

[55] A.M. Hava, N.O. Çetin, and E. Ün, "On the contribution of PWM methods to the common mode (leakage) current in conventional three-phase two-level inverters as applied to AC motor drives," in *Conf. Rec. IEEE IAS Annu. Meeting*, Edmonton, AB, Canada, Oct. 2008, pp. 1–8.

[56] E. Ün, "Common mode voltage and current reduction in voltage source inverter driven three phase AC motors" M.Sc. thesis, Middle East Tech. Univ., Ankara, Turkey, Nov. 2007.

[57] A. Muetze, ''Bearing currents in inverter-fed AC motors,'' Ph.D. dissertation, Darmstadt Univ. of Technol., Shaker Verlag, Aachen, 2004.

[58] Vacuumschmelze GmbH, *Nanocrystalline EMC Components*, 2004.

[59] W. Leonhard, "Control of electrical drives," Springer-Verlag, 1985.

[60] Ansoft Simplorer, V7.0, *Ansoft Corporation*, Pittsburgh, PA, 2004.

APPENDIX A: THE INDUCTION MOTOR PARAMETERS

SIEMENS 1LA7113-4AA		
	Test Results	**Manufacturer Information**
Rated Power	-	4 kW
Rated Voltage	-	400V
Rated Current	-	8.2A
Power Factor	-	0.83
Rated Speed	-	1440 rpm
Rated Torque	-	26.5 Nm
Pole	-	4
Stator leakage inductance	7 mH	7.9 mH
Stator resistance	1.7 Ω	1.77 Ω
Rotor leakage inductance (stator referred)	7 mH	15.8 mH
Rotor resistance (stator referred)	0.54 Ω	1.23 Ω
Magnetizing inductance	140 mH	172 mH
Neutral to chassis capacitance ($C_{n\text{-}g}$) @100kHz	4.4 nF	-
Motor common mode inductance ($L_{n'\text{-}n}$)	5.6mH @1kHz, 1.2mH @100kHz	-

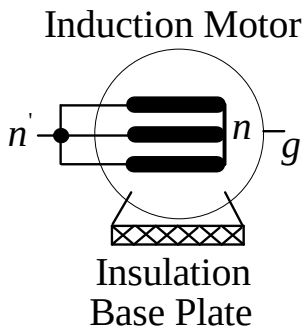


Figure A.1 Measurement of neutral to chassis capacitance ($C_{n\text{-}g}$) and motor common mode inductance ($L_{n'\text{-}n}$).

APPENDIX B: MEASUREMENTS FOR THE MOTOR DIRECTLY CONNECTED TO AC LINE

In this section, first the motor is directly connected to AC line as shown in Figure B.1. Motor phase voltage v_{An}, phase current i_a, neutral point voltage v_{Nn}, and the CMC i_{cm} values are measured for N-n is open-circuited and short-circuited cases. Then, the isolation transformer is placed between the AC line and the motor, as shown in Figure B.2, and the measurements are repeated.

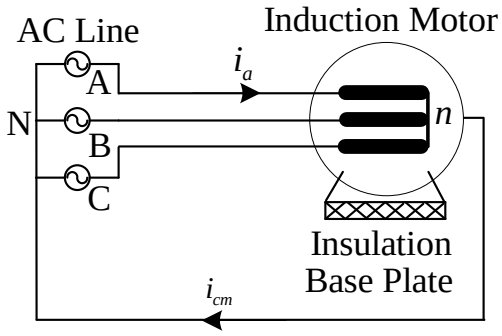


Figure B.1 Measurements without the isolation transformer.

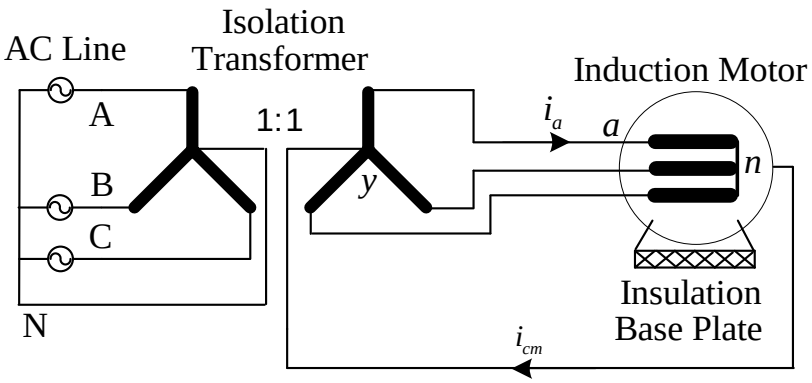


Figure B.2 Measurements with the isolation transformer.

Measurements without the isolation transformer

For N-n is open-circuited: v_{Nn}=8.57V_{rms}, 20.3V_{peak}

For N-n is short-circuited: i_{cm}=3.29A_{rms}, 5.21A_{peak}

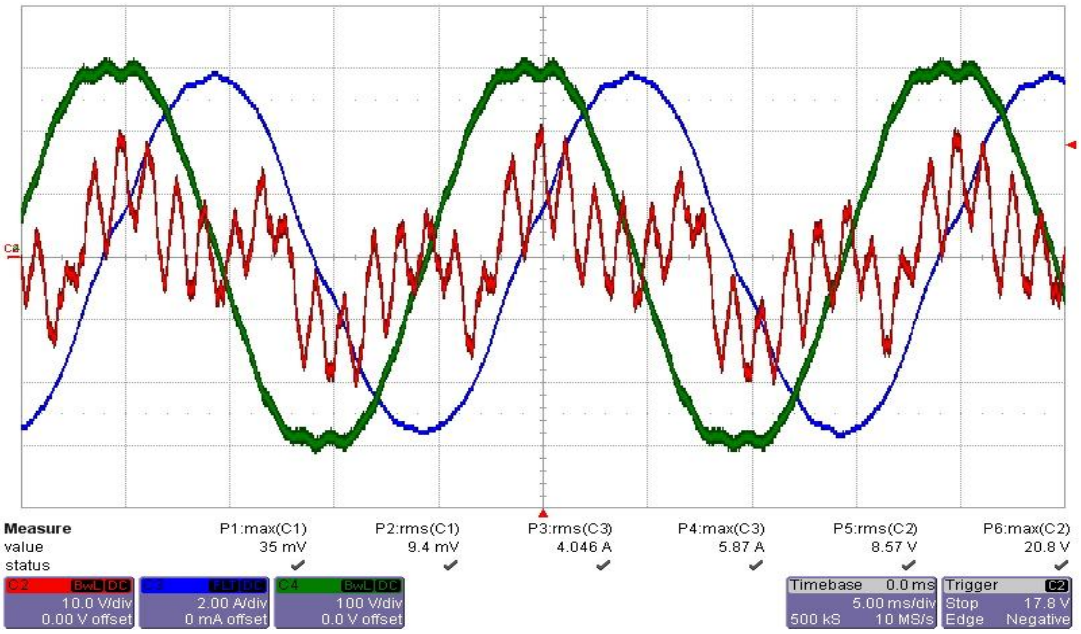


Figure B.3 v_{An} (green, 100V/div), i_a (blue, 2A/div), v_{Nn} (red, 10V/div) waveforms without the isolation transformer.

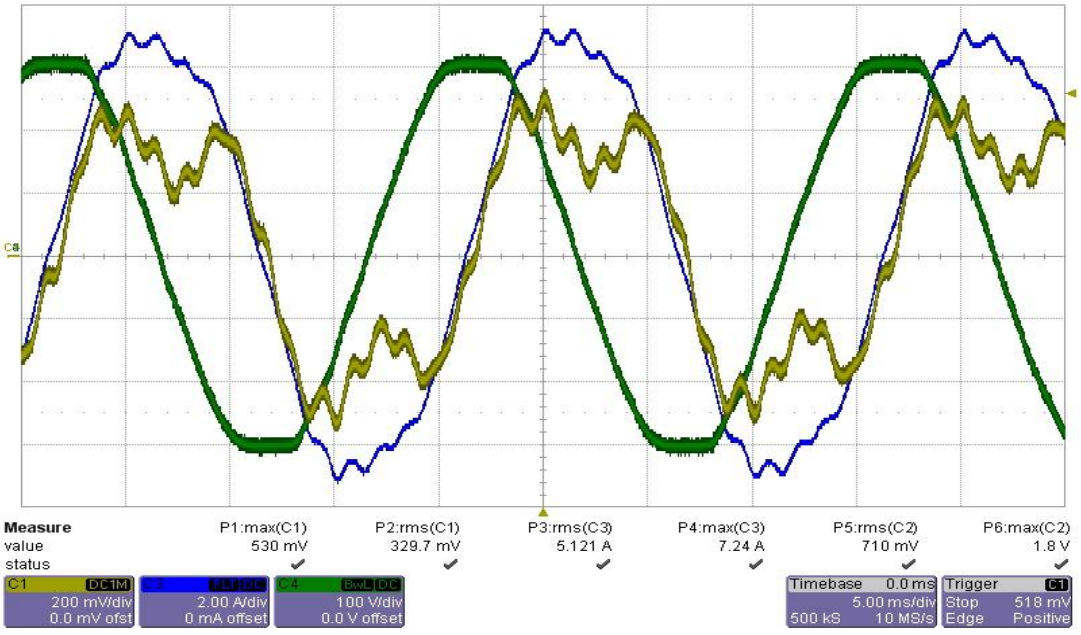


Figure B.4 v_{An} (green, 100V/div), i_a (blue, 2A/div), i_{cm} (yellow, 2A/div) waveforms without the isolation transformer.

Measurements with the isolation transformer

For y-n is open-circuited: v_{yn}=8.27V_{rms}, 21.7V_{peak}

For y-n is short-circuited: i_{cm}=2.9A_{rms}, 5.75A_{peak}

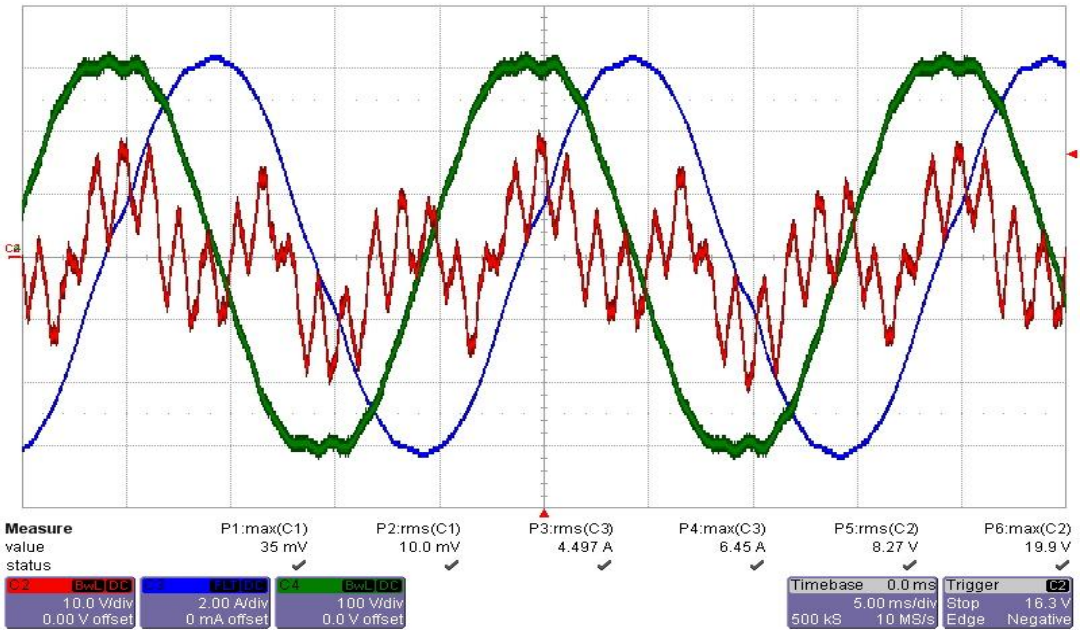


Figure B.5 v_{an} (green, 100V/div), i_a (blue, 2A/div), v_{yn} (red, 10V/div) waveforms with the isolation transformer.

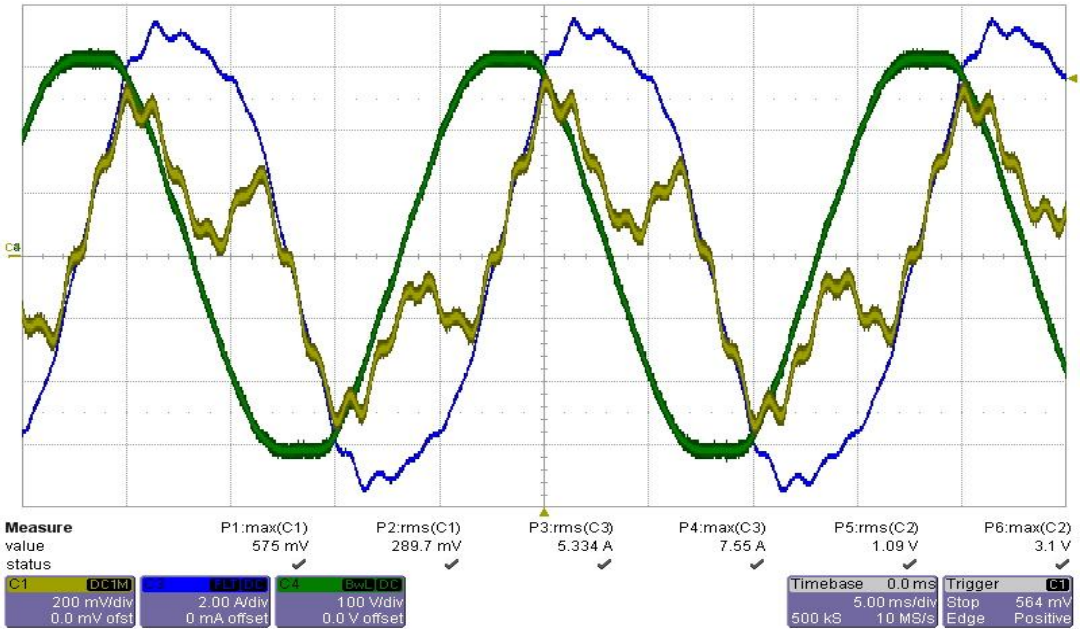


Figure B.6 v_{an} (green, 100V/div), i_a (blue, 2A/div), i_{cm} (yellow, 2A/div) waveforms with the isolation transformer.