DESIGN AND IMPLEMENTATION OF AN ULTRACAPACITOR TEST SYSTEM

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submitted by **HASAN HÜSEYİN EROĞLU** in partial fulfillment of the requirements for the degree of **Master of Science in Electrical and Electronics Engineering Department, Middle East Technical University** by,

Prof. Dr. Canan Özgen _____
Dean, Graduate School of **Natural and Applied Sciences**

Prof. Dr. İsmet Erkmen _____
Head of Department, **Electrical and Electronics Engineering**

Assist. Prof. Dr. Ahmet M. Hava _____
Supervisor, **Electrical and Electronics Engineering Dept., METU**

Examining Committee Members:

Prof. Dr. Muammer Ermiş _____
Electrical and Electronics Engineering Dept., METU

Assist. Prof. Dr. Ahmet M. Hava _____
Electrical and Electronics Engineering Dept., METU

Prof. Dr. Aydın Ersak _____
Electrical and Electronics Engineering Dept., METU

Prof. Dr. Nevzat Özay _____
Electrical and Electronics Engineering Dept., METU

Eyyup Demirkutlu, M.Sc. _____
ELSİS AŞ

Date: 15/07/2010

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Name, Last name : Hasan Hüseyin Eroğlu

Signature :

ABSTRACT

DESIGN AND IMPLEMENTATION OF AN ULTRACAPACITOR TEST SYSTEM

Eroğlu, Hasan Hüseyin

M.Sc., Department of Electrical and Electronics Engineering

Supervisor: Assist. Prof. Dr. Ahmet M. Hava

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In this thesis, a test system is designed and implemented in order to evaluate the basic electrical performance and determine the parameters of ultracapacitors (UC). The implemented UC test system is based on power electronics converters and it is capable of charging and discharging the UC under test with predetermined current profiles. The charging operation is provided by a configuration involving the AC utility grid, a step-down transformer, a diode bridge, and a DC bus filter capacitor followed by a step-down DC-DC converter. The energy stored in the UC under test, as a result of the charging operation, is discharged to a resistor bank through a step-up DC-DC converter and a DC chopper structure. The charging and discharging current applied to the UC under test is provided by means of current mode control of power electronics converters. The control mechanism of the power electronics converters and the transition operations between the charging and discharging phases of the test system is realized via a microcontroller supported hardware structure. In the scope of the thesis study, a UC module composed of five serially connected UC cells is constructed. Constant current and constant power tests are applied to the constructed UC module. The performance of the implemented UC test system is

investigated by means of computer simulations and experimental results. Further, basic electrical behaviour of the constructed UC module is evaluated and the parameters are extracted experimentally.

Keywords: Energy storage devices, ultracapacitor, step-down DC-DC converter, step-up DC-DC converter, current mode control.

ÖZ

BİR ULTRAKONDANSATÖR TEST SİSTEMİNİN TASARIMI VE DENEYSEL GERÇEKLENMESİ

Eroğlu, Hasan Hüseyin

Yüksek Lisans, Elektrik ve Elektronik Mühendisliği Bölümü

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Bu tezde, ultrakondansatörlerin (UK) temel elektriksel özelliklerini değerlendirmek ve güç elektroniği uygulamalarındaki kullanımlarını deneysel olarak öğrenmek maksadıyla bir test sistemi tasarlanmış ve üretilmiştir. Gerçekleştirilen UK test sistemi, güç elektroniği dönüştürücüleri tabanlı bir sistem olup, test edilecek UK'yi istenilen akım profilinde doldurabilecek ve boşaltabilecek bir sistemdir. Doldurma işlevi; AA akım şebekesi, bir alçaltıcı trafo, bir diyot köprüsü, bir DA barası kondansatörü ve bir alçaltıcı DA-DA dönüştürücüsü vasıtasıyla sağlanmaktadır. Doldurma işlevi sonucunda test edilen UK üzerinde depolanan enerji ise bir yükseltici DA-DA dönüştürücüsü ve bir DA kıyıcı yapısı kullanılarak bir direnç grubu üzerine boşaltılmaktadır. Doldurma ve boşaltma işlevleri gerçekleştirilirken, test edilen UK'ye uygulanan akım güç elektroniği dönüştürücülerinin akım kontrollü olarak denetlenmesiyle sağlanmaktadır. Test sisteminde yer alan güç elektroniği dönüştürücülerinin denetimi ile doldurma ve boşaltma fazları arasındaki geçişler mikroişlemci destekli bir donanım yapısı vasıtasıyla gerçekleştirilmiştir. Tez çalışması kapsamında 5 (beş) adet UK hücresinin seri bağlanmasıyla bir UK modülü oluşturulmuş ve oluşturulan UK modülü, UK test sistemi vasıtasıyla sabit akımda ve

sabit güçte doldurma ve boşaltma testlerine tabi tutulmuştur. Gerçekleştirilen UK test sisteminin başarımı bilgisayar benzetimleri yardımıyla ve deneysel olarak ortaya konmuş, oluşturulan UK modülünün temel elektriksel davranışı deneysel olarak gözlemlenmiştir.

Anahtar Kelimeler: Enerji depolama birimleri, ultrakondansatör, alçaltıcı DA-DA dönüştürücü, yükseltici DA-DA dönüştürücü, akım kontrollü denetim.

To my family

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INTRODUCTION

1.1 Energy Storage

In the recent decades, the storage and use of electrical energy efficiently has gained considerable importance in a wide range of applications due to the developments in electronic device, electric vehicle, and industrial system technologies. The scope of the energy storage issue can be classified with respect to the power and energy requirements of applications in many different forms. Portable energy sources for electronic devices like cell phones, digital cameras, laptop computers, auxiliary sources for uninterruptible power supplies (UPS), and secondary sources for electric vehicles are a few examples in this domain. High energy and power density, low cost in terms of installation and maintenance, high performance in terms of operating conditions, long lifetime, and ease of implementation are accepted as the main criteria of energy storage applications.

When the issue is considered from the energy storage device capability point of view, it is seen that meeting the electrical power requirements of applications with a single energy storage device structure has become very difficult in terms of size, cost, and maintenance. The main approach for supplying the electrical power requirements is to divide the requirements into two parts as average power requirements and peak power requirements [1-2]. Energy storage devices like batteries and fuel cells are widely used to provide the average power requirements of applications. On the other hand, it is very common to use capacitors to meet the peak power requirements of applications since the power capability of these devices are

very high [1]. However, pulse duration of peak power requirements has an increasing trend which could not be met by conventional capacitors since these devices have a limited energy density. Therefore, it could be inferred that there is a need for a device that could both deliver high power and store large amount of energy.

Ultracapacitors (UC), also known as supercapacitors or electric double layer capacitors (EDLC) are relatively new energy storage devices that could meet the power and energy requirements of peak power applications. A UC is a special type of capacitor with high capacitance, low equivalent series resistance (ESR), and low rated voltage values. The most attractive property of UCs is their high capacitance value which is expressed with a thousand of farads scale in UC product datasheets [3-6]. When the high capacitance values of UCs are compared with the capacitance values of conventional capacitors, which are commonly in micro farad or milli farad range, it is seen that the capacitance of UCs is at least a thousand times greater than the capacitance of conventional capacitors. Low ESR values of UCs, is the other advantage of UCs for energy storage applications, since the maximum power that could be drawn from an energy storage device is limited with the ESR value. In UC product datasheets, it is reported that the ESR values of UCs are smaller than one milli ohms [3-6]. The ESR values of UCs are also at low levels when compared with the ESR values of conventional capacitors [7]. The main disadvantage of UCs is their low rated voltage values which are at 2.5V level for most of the commercial UC products with organic electrolytes [3-6], [8-12]. For this reason, UCs are connected in series in order to obtain UC modules that have higher voltage ratings [9-10], [12].

When UCs are compared with conventional capacitors by considering the capacitance and rated voltage parameters together, it is seen that the energy storage capacity of UCs for unit volume or mass is higher than conventional capacitors. The stored energy in a capacitor is related with the square of its rated voltage and rated voltage levels of conventional capacitors are higher than UCs. However, the enormous capacitance of UCs brings up the high energy storage capability to UCs despite their low rated voltage values. On the other hand, if the comparison is repeated by considering the ESR and rated voltage parameters, it is seen that the

maximum power capability of UCs is lower than conventional capacitors. The low rated voltage value of UCs brings up this result since the maximum power that could be drawn from an energy storage device is proportional with the square of its rated voltage and inversely proportional with its ESR value [2]. It could be stated that, UCs are connected in series in order to achieve higher rated voltage levels and the ESR value of the serially configured UC module increases proportional with the number of UC cells which will have a decreasing effect to the maximum power capability of the UC module. When the energy storage and maximum power capabilities of conventional capacitors and UCs are compared together, it is seen that UCs are good candidates for supplying the energy requirements of high power applications in a relatively long time period, whereas the conventional capacitors could only deliver electrical energy in a small time period.

In most of the energy storage applications, batteries are the main choice since they can store large amounts of energy in a small volume and weight [1], [13]. Moreover, the cost of using batteries in energy storage applications is very low. On the other hand, the maximum power capability of batteries is at low levels since the ESR of batteries is high. Therefore, it could be concluded that batteries are energy storage devices with large energy storage and low power capability. In this sense, from the energy storage and power capability point of views, it is reported that UCs fill the gap between batteries and conventional capacitors [8], [10], [14].

Batteries are good options for most of the energy storage applications. However, electrochemical energy storage mechanism of batteries limits the cycle and shelf life of the device [1]. During the charging and discharging processes of batteries, oxidation and thermal impacts of electrochemical reactions deteriorates the cycle life of the device. Moreover, when batteries are left unused for many months, corrosion effects are seen due to the self discharging process which reduces the shelf life of the device [1]. On the other hand, the energy storage mechanism of UCs is fully electrostatic and it is not based on electrochemical reactions [12]. Therefore, cycle and shelf life of UCs are better than batteries.

UCs are promising alternatives to battery technology. However, the main limiting factor for practical use of UCs in energy storage applications is the low energy storage capability of UCs in terms of unit volume, mass, and cost. In this sense, it could be said that the use of UCs will become widespread if the energy storage capacity of the device is improved in terms of unit volume, mass, and cost. Although the structural evolution of UCs is not finished, the use of UCs is very common in memory back up applications. Furthermore, UC manufacturers recommend using the device in many applications. Supplying the power requirements of an electric vehicle (EV) in the case of acceleration and storing the regenerative energy appeared in the case of braking, supplying the power requirements of portable electronic devices, starting internal combustion engines, supplying the bridge power requirements for UPS systems, compensating voltage sags for adjustable speed drives (ASD) are a few examples of UC assisted energy storage applications [12], [15].

1.2 Outline and Scope of the Thesis

In Turkey, the common energy storage device used for energy storage applications is battery (lead-acid, lithium ion, Ni-Mh ext.) and up to the present day, no commercial products have been developed utilizing UCs due to the high cost of the device. On the other hand, there is not sufficient knowledge about how and where to use UCs although it is required to develop more robust energy storage systems for most of the applications such as UPS and ASD systems. Moreover, if it is aimed to develop an EV as a home product, the use of UCs will also be required. Therefore, in this thesis study, it is aimed to learn the characteristics and use of UCs experimentally for energy storage applications.

Standard measurement devices like LCR meters are not sufficient for observing the UC characteristics experimentally. For example, the measurement range of standard LCR meters for capacitance measurement is much narrower than the capacitance value of UCs. Furthermore, these measurement devices have limited energy. Most of them are battery powered. Therefore, these devices can not change the stored energy

in a UC. For this reason, a power electronics converter based UC test system is built to measure the characteristics of UCs experimentally. In the implemented test system, charging and discharging energy management procedures are applied. By this way, it is also learned how to utilize UCs with power electronics converter structures. The control methods and hardware design approach used in this study are focused on constructing a UC test system. However, the implemented test system could also be used as a reference design in power electronics applications involving UC utilization or other energy storage-transfer applications, since the approach is general.

Thesis study has been conducted in a step by step approach starting from the general properties of UCs up to a detailed hardware design and UC performance evaluation part. In this sense, the outline of the study could be expressed as follows:

In Chapter 2, basic electrical and structural properties of UCs are reviewed. General information about the design criteria and typical applications of UCs together with the comparison of UCs with other energy storage devices issue are also covered in this chapter.

In Chapter 3, performance evaluation of UCs is discussed. UC testing requirements from the manufacturer and customer point of views, requirements and building blocks of a UC test device, and some of the UC test procedures are discussed in this chapter.

In Chapter 4, power electronics converter structures are investigated for performing the charging and discharging operations of UCs which are the basic operations of a UC test system.

In Chapter 5, design and implementation of a power electronics converter based UC test system is covered. In this chapter, implementation details in terms of microcontroller and mixed signal hardware considerations are shown. The

performance of the implemented test system is put forward by means of computer simulations and experimental results.

In Chapter 6, basic electrical parameters and electrical performance of a UC module which consists of five serially connected UC cells are extracted by the help of the test results obtained as an output of the implemented UC test system. The results of the tests are also compared with the datasheet parameters of the UC cells.

In Chapter 7, the thesis work is summarized, important aspects of the test results and hardware design part are mentioned, and future work is discussed.

CHAPTER 2

CHARACTERISTICS, PERFORMANCE, AND DESIGN CONSIDERATIONS OF ULTRACAPACITORS

2.1 Introduction

A UC is a special type of capacitor based on electric double layer (EDL) mechanism. The storage mechanism of UCs is an electrostatic process where no electrochemical reactions are involved [12]. EDL based energy storage mechanism together with the unique internal structure of UCs results in very high capacitance values. On the other hand, properties of the materials used within the device affect the UC specifications such as the rated voltage and equivalent series resistance (ESR) [8]. Therefore, to design a UC assisted energy storage application, it is necessary to investigate the energy storage mechanism and internal structure of UCs. By this way, basic design criteria of UCs that are critical for energy storage applications could be understood easily. In the scope of the thesis, it is aimed to implement a UC test system for the evaluation of UC performance and to see how this energy storage device could be utilized in power electronics applications. Therefore, in this chapter basic structural and electrical properties of UCs are reviewed by considering the design criteria from the application perspective. Comparison of UCs with other energy storage device types and typical UC applications are also covered.

2.2 Capacitive Energy Storage Method

The energy storage mechanism of UCs has the same properties with conventional capacitors in terms of mathematical formulas [16]. Therefore, it is proper to review the capacitive energy storage method before going into the details of UCs. Capacitive storage method is one of the most common forms of electrical energy storage where electrical energy is held in a device called capacitor. The internal structure of a capacitor is shown in Figure 2.1.

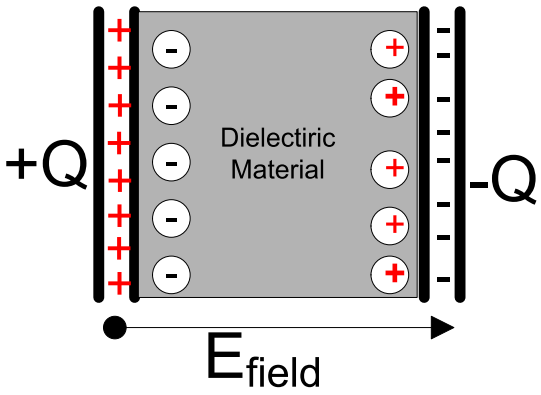

Figure 2.1 Internal structure of a capacitor.

As shown in Figure 2.1, a capacitor consists of two conducting plates separated by an insulating component called dielectric material. When an electrical potential is applied between the terminals, electrical charges within the device start to accumulate near the plates according to the polarity of the applied potential. By this way an electric field is created inside the capacitor. The net electrical charge accumulated on the plates (Q) and the corresponding electrical potential (V) are related with a parameter called capacitance (C) as given in (2.1).

$$C = \frac{Q}{V} \tag{2.1}$$

In order to express the capacitance in terms of dimensions of the device, uniform electric field approximation within the device could be used, since the surface area (A) of the plates is much greater than the length of the dielectric material (d). With

this approximation it could be said that, permittivity (ε) of the dielectric material determines the magnitude of the electric field inside the device. On the other hand, permittivity of a material is the distance passed by an electric charge with a unit electric field and expressed as relative permittivity (ε_r) according to the permittivity of air (ε_o) as given in (2.2).

$$e = e_0 \times e_r \tag{2.2}$$

If the distribution of electrical charge on the plates of the device is also considered uniform in addition to the uniform electric field approximation, the magnitude of the electric field could be expressed in terms of charge density (D) and permittivity as given in (2.3).

$$E = \frac{D}{e} = \frac{\frac{Q}{A}}{e} = \frac{Q}{A \times e} \tag{2.3}$$

After inferring the electric field expression, the electrical potential inside the device could be expressed as the line integral of the electric field within the dielectric length (d) as given in (2.4).

$$V = \int_0^d \frac{D}{e} \times dz = \frac{D \times d}{e} = \frac{Q \times d}{e \times A} \tag{2.4}$$

If (2.1) and (2.4) are considered together, it is seen that the capacitance of the device is related with the surface area of the plates, permittivity, and dielectric length of the insulating material as given in (2.5).

$$C = \frac{e \times A}{d} \tag{2.5}$$

To obtain the energy change expression (ΔE) inside a capacitor, (2.1) should be organized as given in (2.6).

$$Q = C \times V \tag{2.6}$$

If the both sides of (2.6) are differentiated with respect to time, current expression is obtained as given in (2.7).

$$i(t) = C \times \frac{dV(t)}{dt} \tag{2.7}$$

In the next step, instantaneous power expression is obtained by multiplying the current expression with the capacitor voltage as given in (2.8).

$$P(t) = C \times \frac{dV(t)}{dt} \times V(t) \tag{2.8}$$

As a last step, instantaneous power expression is integrated with respect to time in a time interval (t_0-t_1) to obtain the energy change expression of the capacitor within this time interval as given in (2.9).

$$\Delta E = \frac{1}{2} \times C \times \left[(V(t_1)^2 - V(t_0)^2 \right] \tag{2.9}$$

By the help of the energy change expression, the stored energy in a capacitor at a time instant could also be expressed as given in (2.10).

$$E(t) = \frac{1}{2} \times C \times V(t)^2 \tag{2.10}$$

The stored energy expression given in (2.10) shows that, the stored energy inside a capacitor at a time instant is related with the capacitance and instantaneous voltage of the device. Therefore, the maximum energy that could be stored inside a capacitor is

related with the maximum voltage that could be reached within the device. This maximum level is commonly known as the voltage rating (V_{rated}) of a capacitor which is limited with the breakdown voltage of the dielectric material. The breakdown voltage expression (V_{bd}) of a dielectric material is given in (2.11).

$$V_{bd} = E_{ds} \times d \tag{2.11}$$

According to (2.11), it is seen that, breakdown voltage is related with the dielectric length and dielectric stress (E_{ds}) of the material which is defined as the magnitude of the electric field in order to make an insulating material totally conductive. When (2.5), (2.10), and (2.11) are evaluated together, it is seen that capacitors with higher dimensions have a larger energy storage capability. This result shows that capacitors have a low energy density trend where energy density (Ed_{vol}, Ed_m) could be defined according to the volume (Vol) or mass (m) of the device as given in (2.12) and (2.13).

$$Ed_{vol} = \frac{\frac{1}{2} \times C \times V_{rated}^2}{Vol} \tag{2.12}$$

$$Ed_m = \frac{\frac{1}{2} \times C \times V_{rated}^2}{m} \tag{2.13}$$

When capacitors are investigated in terms of maximum power capability, it is seen that the most important term is the equivalent series resistance (ESR) of the devices which represents the ohmic loss. The equivalent circuit model of a capacitor in discharging mode is shown in Figure 2.2.

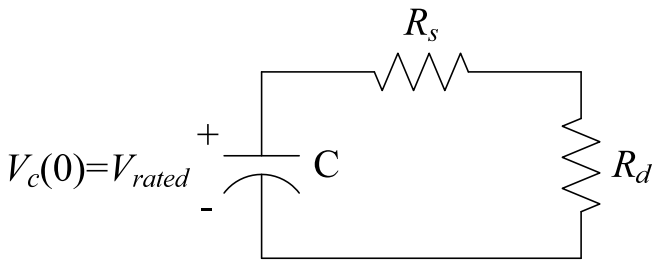

Figure 2.2 Electrical equivalent circuit of a capacitor in discharging mode.

In Figure 2.2, R_s represents the ESR of the device, whereas R_d represents the discharging resistor. The maximum power that can be drawn from a capacitor can be obtained by applying the maximum power transfer principle to the circuit shown in Figure 2.2. The maximum power expression is given in (2.14).

$$P_{\max} = \frac{V_{rated}^{\,2}}{4 \times R_s} \tag{2.14}$$

The circuit shown in Figure 2.2 could also be analyzed according to discharge efficiency (η) considerations as it is shown in [2]. Discharge efficiency is defined as the ratio of the power dissipated on the discharge resistor (P_L) with the power supplied by the capacitor (P_c) as given in (2.15).

$$h = \frac{P_L}{P_c} = \frac{\left(V_c \times \frac{R_d}{R_d + R_s}\right)^2}{\frac{V_c^{\,2}}{R_d + R_s}} = \frac{R_d}{R_d + R_s} \tag{2.15}$$

By rearranging (2.15), the power dissipated on the discharging resistor could be expressed in terms of capacitor voltage (V_c), ESR, and discharge efficiency as given in (2.16).

$$P_L(h) = h \times (1-h) \times \frac{V_c^{\,2}}{R_s} \tag{2.16}$$

The load power expression given in (2.16) could also be reorganized according to the volume (*Vol*) and mass (*m*) of the device as given in (2.17) and (2.18).

$$P_{Lvol}(h) = \frac{h \times (1-h) \times \frac{V_c^{\,2}}{R_s}}{Vol} \tag{2.17}$$

$$P_{Lm}(h) = \frac{h \times (1-h) \times \frac{V_c^{\,2}}{R_s}}{m} \tag{2.18}$$

The load power expression given in (2.16) could be averaged with respect to constant current discharging assumption, where the voltage of the capacitor decreases from V_{rated} level to $V_{rated}/2$ level linearly with respect to time under this assumption. The average load power (P_{L_av}) expression obtained as a result of this approximation is given in (2.19) [1].

$$P_{L\_av}(h) = \frac{9}{16} \times h \times (1-h) \times \frac{V_{rated}^{\,2}}{R_s} \tag{2.19}$$

The variation of average load power with respect to discharge efficiency is shown in Figure 2.3 where the maximum power expression given in (2.14) is taken as reference.

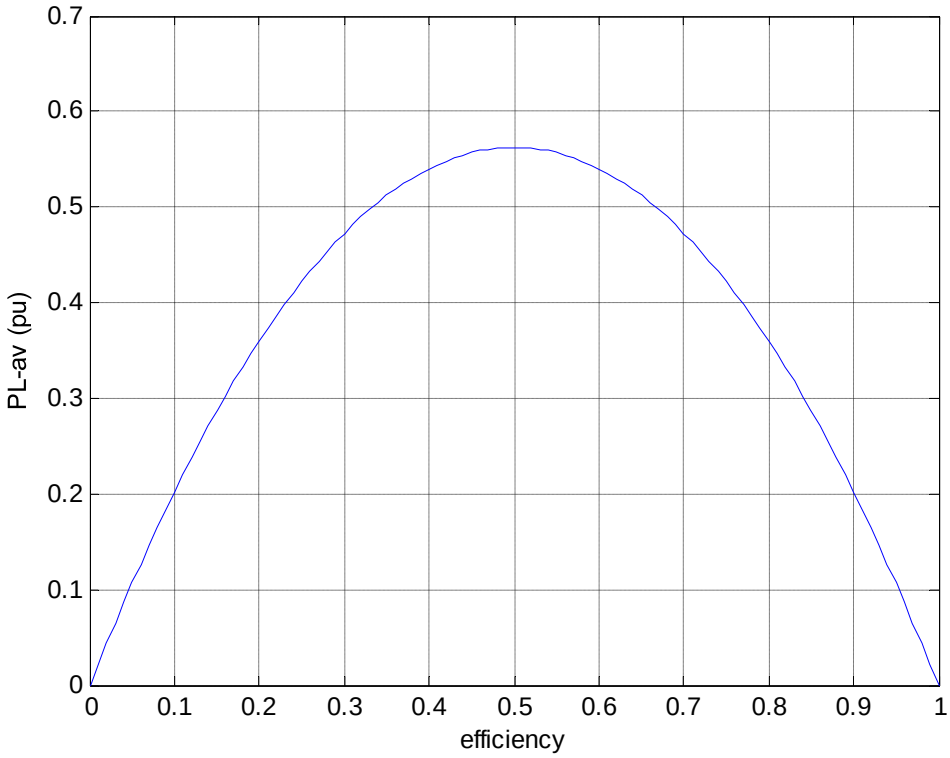

Figure 2.3 Variation of average load power with respect to discharge efficiency.

According to Figure 2.3, it is seen that the maximum discharging power condition occurs for 50% efficiency case where the load resistance is equal to the ESR of the device. It is also observed that as the discharge efficiency increases, discharging power decreases. Therefore, it could be concluded that it is required to limit the discharging power in applications where efficiency is important.

2.3 Ultracapacitors and Their Internal Structure

After reviewing the capacitive energy storage mechanism in a general perspective, it is appropriate to continue with the properties of UCs. The internal structure of UCs is based on electric double layer (EDL) mechanism. For this reason, UCs are commonly known as electric double layer capacitors (EDLC). To understand the behavior of these devices it is necessary to investigate the EDL structure.

2.3.1 The Electric Double Layer (EDL) Structure

When a charged conductor is immersed in a solution, the electric charge carried by the electrons and holes of the conductor and ions within the solution start to accumulate in the contact surfaces of the conductor and solution. The accumulated charge on the conductor and solution sides constitutes the EDL structure which is shown in Figure 2.4.

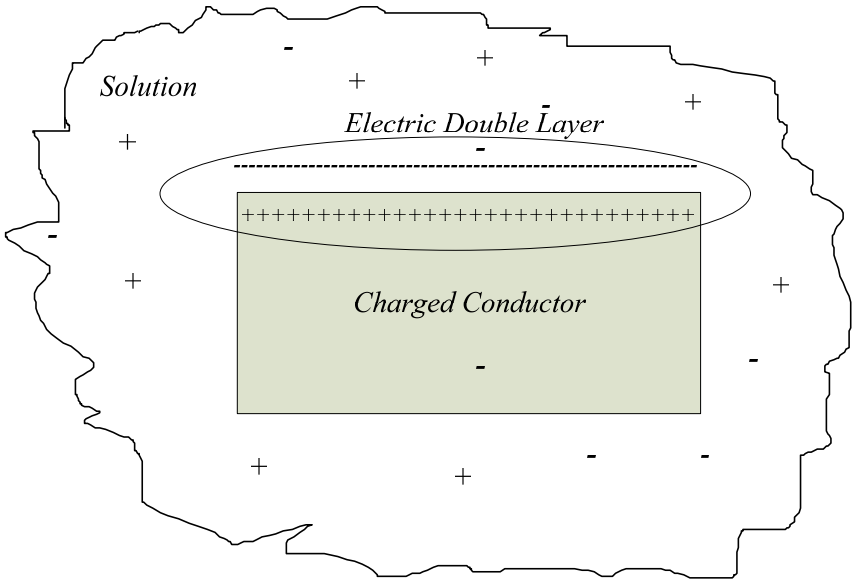

Figure 2.4 EDL structure.

The EDL structure in Figure 2.4, can be described by a three layer model which is shown in Figure 2.5. In this model, the first layer is the space charge layer (SCL) constituted by the excess carriers within the conductor, the second layer is the Helmholtz layer constituted by the adsorbed liquid molecules, and the third layer is the Gouy layer (GL) constituted by the ions within the solution. In Figure 2.5 (a), it is seen that the charge carriers are at highest concentration at the boundary of the SCL and GL. The carrier concentration decreases as the distance from the boundary of the SCL and GL increases. In Figure 2.5 (b), it is seen that the inner potential inside the EDL structure is at highest level in the SCL and shows a decreasing characteristics in the HL and GL, respectively. The working principle of this model is similar to a

passive electric component composed of three serially connected capacitors as shown in Figure 2.5 (c) [17].

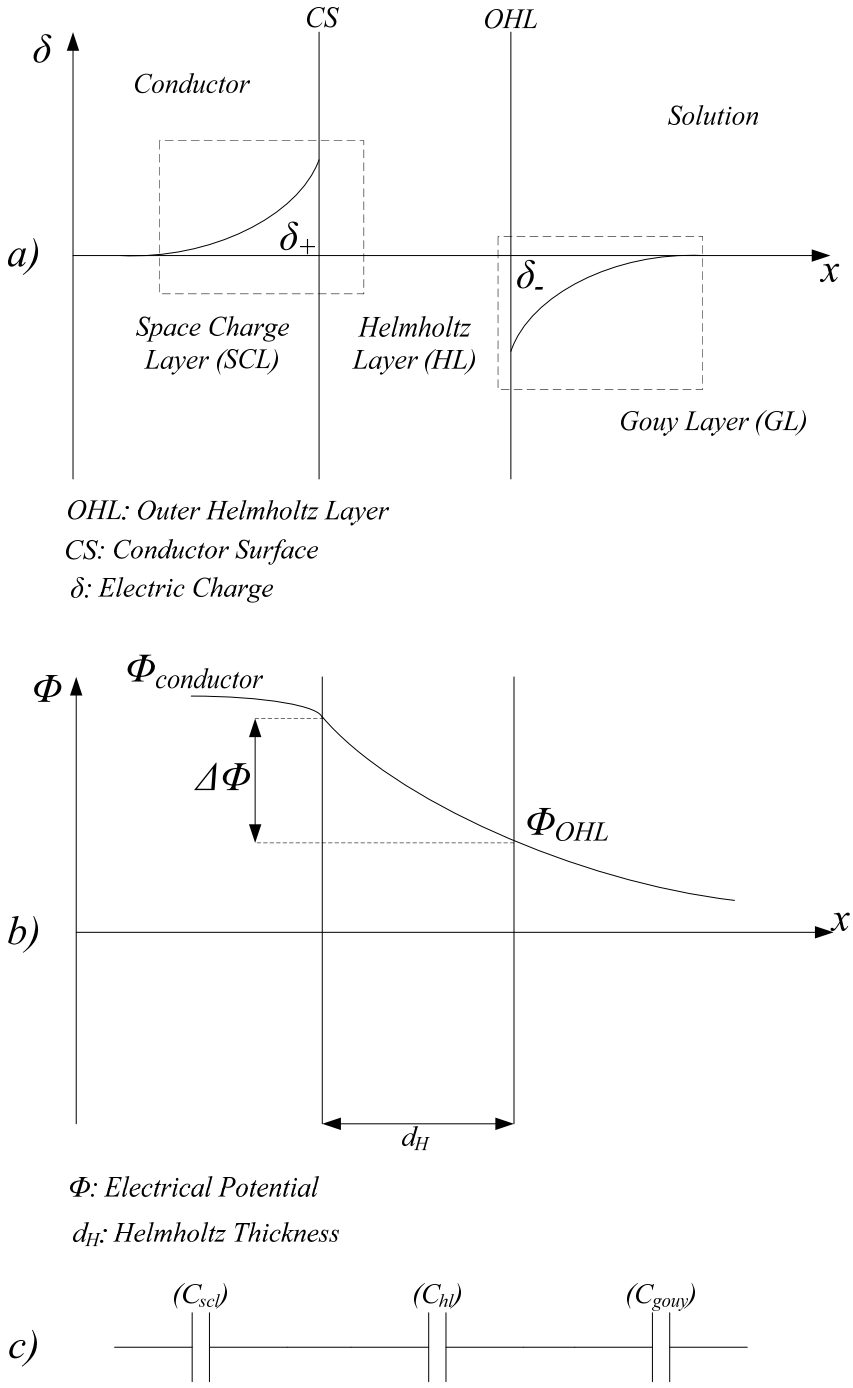

Figure 2.5 Three layer model of the EDL structure: (a) variation of excess charge density, (b) variation of inner potential, (c) capacitor model [17].

In [17], it is stated that the thickness of HL (d_H) is related with the size of the liquid molecules and generally this distance is between 0.5-1 nm. On the other hand, the thickness of SCL and GL are related with the charge carrier concentration where their thickness decreases with increasing carrier concentration. The thickness of SCL and GL are at least 10 times higher than the thickness of HL [17]. Therefore, the capacitance of HL is dominant in the serially configured capacitor configuration shown in Figure 2.5 (c), since the capacitance is inversely related with the thickness of the dielectric material. According to the dominating capacitive characteristic of HL, the EDL structure could be represented by single a capacitor, where the capacitance value is dominated by HL [17]. As a conclusion, it is seen that the nanometric dielectric length property of the EDL structure results in very high capacitance values and low voltage ratings when the equations for capacitive energy storage section are revisited.

2.3.2 Ultracapacitors

A UC is a special capacitor type based on EDL mechanism and it can be considered as a composition of many EDL structures. The capacitance and voltage rating information of some commercial UC products is shown in Table 2.1. As shown in Table 2.1, it is seen that the capacitance range of the commercial UC products varies between a few farads level and thousands of farads level and it can be inferred that these capacitance values are extremely high when compared with the capacitance values of conventional capacitors (e.g. aluminum electrolytic capacitors) which are commonly in µF and mF scale. On the other hand, it is also seen that the voltage rating levels of the commercial UC products varies between 2.3-2.7V for the devices with capacitance values in thousand of farads scale (e.g. Maxwell, Nesscap, ext.) and the rated voltage level reaches the 5.5V level for devices with lower capacitance values (Cap XX, Nec-Tokin).

Table 2.1 Product information of some UC manufacturers

Company	*Country*	*Capacitance Range (F)*	*Voltage Range (V)*
Maxwell Technologies	USA	10-3000	2.5-2.7
Nesscap Co.Ltd.	Korea	5-5000	2.3-2.7
LS Mtron Ltd.	Korea	3-3000	2.5-2.8
Ioxus Inc.	USA	100-5000	2.7
Tecate Industries	USA	0.5-300	2.7
Vinatech Co.	Korea	3-350	2.5-2.7
Cap-XX Ltd.	Australia	0.075-2.4	2.3-5.5
United Chemicon	Japan	350-3200	2.3-2.5
Nec-Tokin Corp.	Japan	0.047-1	3.5-5.5

2.3.3 Internal Structure of Ultracapacitors

UCs consist of two electrodes, a separator, and an electrolyte that fills the space inside the device [8]. The internal structure of a UC is shown in Figure 2.6.

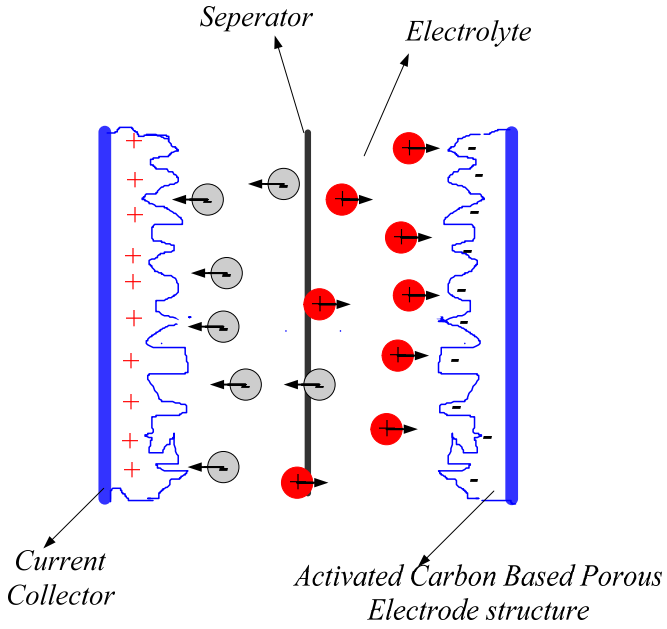

Figure 2.6 Internal structure of a UC [8].

The electrodes of a UC consist of highly conducting metallic current collectors and an activated carbon part with a porous structure. The porous structure of activated carbon increases the contact surface between the electrodes and electrolyte which results in very high capacitance values, since the capacitance increases with the surface area of the electrodes [1], [8], [12]. Basically, it could be thought that the capacitance of a UC increases linearly with the increasing contact surface between the activated carbon and the electrolyte according to the parallel plate capacitor theory. However, in practice the pore sizes of the electrodes should be taken into consideration. Because, effective surface area of the devices with very small pore size is lower than the original surface area due to the insufficient electrostatic effect between the electrolyte and small pores of the activated carbon [8], [17-18].

The electrolyte type of UCs affects the ESR parameter and determines the voltage rating of the device. The most common electrolyte types used in UCs are aqueous (KOH, H_2SO_4) and organic types [18]. There is a tradeoff between the use of aqueous and organic electrolytes in terms of ESR and voltage rating of the device. When the two electrolyte types are compared according to ion conductivity, it is seen that the conductivity of aqueous electrolytes is higher than those of organic electrolytes. Therefore, ESR of devices with aqueous electrolytes is lower than the ESR of devices with organic electrolytes [8]. However, from the voltage rating perspective, it is seen that decomposition voltage of organic electrolytes (~2.5V) is higher than the decomposition voltage of aqueous electrolytes (~1.25V) [8]. Therefore, UCs with organic electrolytes tend to have a higher energy density compared to UCs with aqueous electrolytes when the stored energy expression shown in (2.10) is reconsidered. For this reason, in most of the commercial UC products organic electrolytes are used [3-6].

When the electrode and electrolyte properties of UCs are considered together, it is seen that the capacitance of UCs with aqueous electrolyte types tend to have a higher capacitance value for the same UCs with organic electrolytes. Burke explains the reason of this situation according to the larger size of the ions in organic electrolytes compared to the ions in aqueous electrolytes [1]. Therefore, it could be concluded

that the electrostatic effect between the electrode and electrolyte structure is lower for the organic electrolyte case due to the large ion size.

The separator is a structure that prevents electrical conductance between the two electrodes of the device. On the other hand, it permits ionic conductance. Therefore, it is important to select a proper separator material according to the electrolyte properties, since separator should permit the ion transmission within the electrolyte. For aqueous electrolytes, glass fiber or ceramic separators are used, while polymer or paper based separators are utilized for devices with organic electrolytes [8]. For the UC products of Maxwell Technologies, polypropylene or cellulose separators are used [19].

2.4 Basic Electrical Properties of Ultracapacitors

Modeling the terminal electric behaviour of UCs is very difficult due to their complicated internal structure. However, in order to utilize UCs with full advantage, it is needed to put forward the most consistent electric circuit model of the device [20]. In this study, it is aimed to investigate the basic electric behaviour of UCs by means of utilizing power electronics converters. Therefore, only the basic RC equivalent circuit is considered which is shown in Figure 2.7.

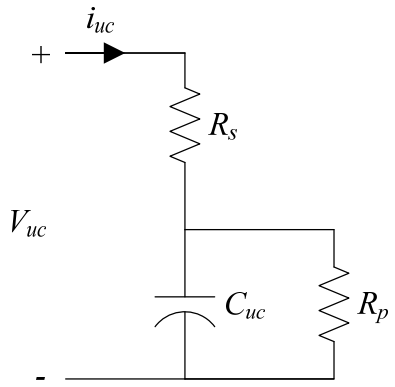

Figure 2.7 Basic electrical equivalent circuit of a UC [21-22].

In Figure 2.7, C_{uc} represents the device capacitance, R_s represents ESR, and R_p represents equivalent parallel resistance (EPR) of a UC. Capacitance values of UCs are very high compared to conventional capacitors which show that the energy density of the device is high [3-7]. On the other hand, ESR represents the ohmic loss within the device and it is a resultant value of the contact resistance of electrodes and electrolyte. ESR of a UC determines the maximum power rating of the device and it is given for DC and AC (100Hz or 1kHz) cases in product datasheets [3-6]. The immediate rise and fall of the terminal voltage of a UC when the charging and discharging operations are initiated or stopped are also resulted from the ESR of the device [22]. The other loss component is EPR. It represents the static loss due to the leakage current of the device and determines the self discharge rate in resting condition. EPR values can be obtained from product datasheets by dividing the voltage rating (V_{rated}) of the device with the leakage current parameter ($I_{leakage}$) as given in (2.20) [21].

$$EPR = \frac{V_{rated}}{I_{leakage}} \tag{2.20}$$

Considering the model shown in Figure 2.7, important parameters of some commercial UC products are listed in Table 2.2 according to [3-6]. As shown in Table 2.2, it is seen that the investigated commercial UC products have enormous capacitance values (1500F-5000F), low rated voltage ratings (~2.7V), and low ESR values (0.25-0.5 mΩ [DC]). It is also seen that the calculated EPR values of the UC products are in 0.415-0.9 kΩ range since the leakage current of the devices are in 3-6.5 mA range. When the energy density of the UC products in Table 2.2 is considered, it is seen that the energy storage capability of the selected UC products are above 15 kJ/kg and 15 kJ/l level. On the other hand, the power density of the selected UC products is above 7.5 kW/kg and 10 kW/l level in terms of gravimetric and volumetric considerations, respectively.

Table 2.2 Important parameters of some UC products

Manufacturer	*Product Part Number*	*C (F)*	*V_{rated} (V)*	*ESR (mΩ)*	*EPR (kΩ)*	*Mass (g)*	*Vol (ml)*	*Energy Density*		*Power Density (P_{max})*	
								(kJ/kg)	*(kJ/l)*	*(kW/kg)*	*(kW/l)*
Maxwell	BCAP 1500	1500	2.7	0.47 (DC) 0.35 (1 kHz)	0.9	320	325	17.1	16.81	16.27	16.02
Nesscap	ESHSR-1200C0-002R7A5	1600	2.7	0.41 (DC) 0.34 (100 Hz)	0.9	335	242	16.70	24.084	16.00	22.15
LS Mtron	HV Series	3000	2.8	0.4 (DC) 0.5 (100 Hz)	0.56	630	469	18.68	25.09	7.78	10.45
Ioxus	RSC2R7508SP	5000	2.7	0.25 (DC) 0.20 (1 kHz)	0.415	840	768	21.71	23.72	10.85	11.87

In many studies, it is reported that the model shown in Figure 2.7 does not represent the terminal electric behaviour of UCs accurately [20], [23-24]. In [23], Zubieta and Bonert state that there are considerable differences between the actual terminal electric behaviour of UCs and the terminal electric response of the basic electrical equivalent circuit model of UCs when the charging and discharging operations are stopped or initiated and they proposed a detailed electrical circuit model for expressing the terminal electric behaviour of UCs which is shown in Figure 2.8.

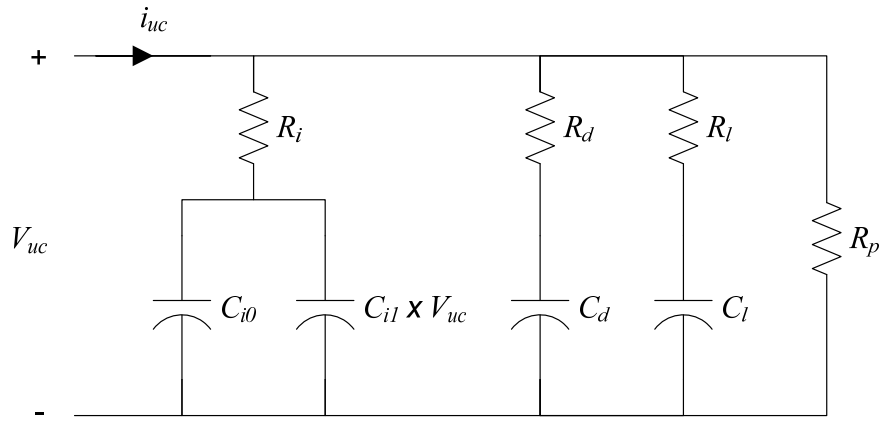

Figure 2.8 Detailed electrical equivalent circuit of a UC [23].

According to [23], each RC branch shown in Figure 2.8 represents the electric behaviour of UCs at different time scales. The first branch is composed of a series resistor (R_i) followed by two parallel capacitors (C_{i0}, $C_{i1}xV_{uc}$) where this branch is effective in a time scale of seconds. Different from the model shown in Figure 2.7, this branch includes a voltage dependent capacitor ($C_{i1}xV_{uc}$). The capacitance of this component increases as the terminal voltage of the device increases. This voltage dependent component is put into the model in order to reflect the rapid rise and fall behaviour of the UC terminal voltage when the charging and discharging operations are initiated or stopped as it is explained in [23]. The second (R_d ,C_d) and third (R_l, C_l) branches are composed of series RC configurations with different time constants which represents the UC behaviour in minutes scale and longer than ten minutes scale, respectively. The function of the last component (R_p) is the same as the function of EPR defined for the model shown in Figure 2.7.

When the models shown in Figure 2.7 and Figure 2.8 are compared, it is seen that the model shown in Figure 2.7 represents only the basic electrical behaviour of UCs where the model shown in Figure 2.8 represent the UC behaviour more accurately. However, it could be inferred that, simplicity of the model shown in Figure 2.7 seems as an advantage from the analysis and computational perspectives [20]. Furthermore, in this study it is aimed to learn the basic characteristics of the device. Therefore, throughout the thesis study the simple model shown in Figure 2.7 is utilized.

2.5 Design Criteria of Ultracapacitors

In order to integrate UCs to power electronics applications it is required to consider the design criteria of UCs which will be discussed in this section.

2.5.1 Voltage Rating and Power Requirement Based Criteria

2.5.1.1 Voltage Window

Miller and Burke define the voltage window as the voltage range in which the capacitor could be operated [21]. There are two reasons for considering the voltage window in UC based designs. The first one is the rated voltage and the second one is the minimum voltage level that will be used in the design. The voltage rating criterion is the key parameter of the designs. Because, when the terminal voltage of UCs goes above the rated level, malfunctions are started to be seen. Maxwell Technologies reports that if the terminal voltage of a UC goes above the rated level for a long duration, the device starts to be affected negatively in terms of decrease in capacitance and increase in ESR. On the other hand, it is also mentioned that voltage spikes for short duration are tolerated by UCs [12].

From a practical point of view, discharging of UCs to zero volts is not possible when they are used in a constant power discharging application. Barrade et al. describes this situation in [25]. They consider a constant power discharging application and state that the current provided by the UC increases as the terminal voltage of the device decreases during the constant power discharging process. They also mention that the discharging current should be limited by determining a minimum voltage level for UCs under discharging process [25].

2.5.1.2 Polarity

Positive and negative terminals of UCs are made from the same materials. Therefore, theoretically it could be thought that there is no need for defining positive and negative terminals for UCs as it is expressed in [26]. However, positive and negative terminals are clearly expressed in all of the commercial products and it is recommended not to use the device in opposite polarity [3-6]. The reason for this recommendation is explained in an application note of Maxwell Technologies as follows: "If the UC has been conditioned for charge in a certain direction and then is changed, the life can be reduced due to this conditioning [26]".

2.5.1.3 Sizing of Ultracapacitors with Respect to Application Requirements

UCs should be connected in series in order to achieve the voltage rating requirement of applications that is usually much higher than the rated voltage of a single device. On the other hand, UC modules constituted by serial connection may be insufficient for the energy storage requirements of some applications. The solution for the mentioned requirement is to connect extra serially configured modules with the same number of devices in parallel with the previous module. By this way, an NxM matrix formed module is obtained. The schematic representation of a module in NxM matrix form is shown in Figure 2.9 and the properties of UC modules are summarized in Table 2.3. When modules in Nx1 and NxM forms are compared with respect to

failure consideration, it is seen that NxM formed modules are more reliable. Because, the worst conditioned UC becomes dominant in Nx1 formed modules. For example, if a UC cell fails and becomes open circuit, the whole module in Nx1 form will show open circuit behaviour. On the other hand, the remaining M-1 branches will be effective if an open circuit condition occurs for one branch in an NxM formed module.

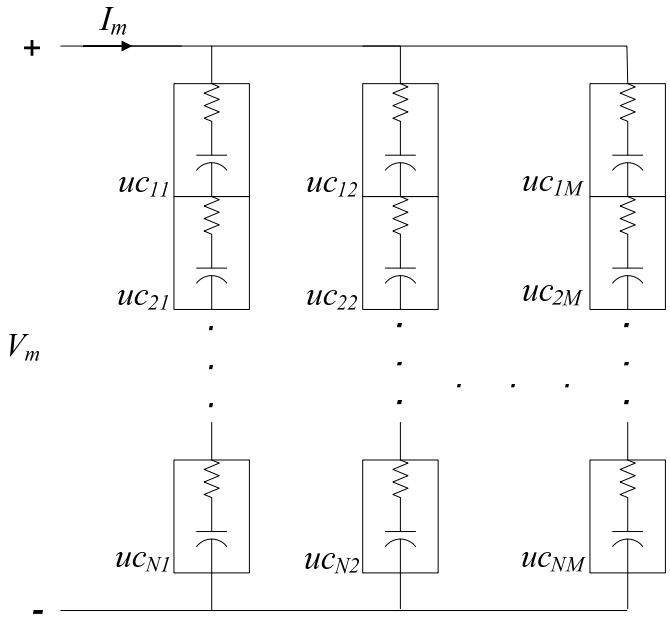

Figure 2.9 Schematic representation of an NxM matrix formed UC module.

Table 2.3 Properties of matrix formed UC modules

	UC (1x1)	*Module (Nx1)*	*Module (NxM)*
Voltage Rating	V	V x N	V x N
Capacitance	C	C / N	C x M / N
ESR	R_s	R_s x N	R_s x N / M
Stored Energy	E	E x N	E x N x M

In many studies and manufacturers' application notes, sizing algorithms and methods are given for determining the appropriate size of NxM formed UC modules [27], [28]. According to the sizing method shown in [28], UC voltage window with respect to the application needs, amplitude and duration of power pulses are reported as the

key parameters. Flowchart of a UC module sizing algorithm is shown in Figure 2.10 according to the method expressed in [28]. The first step in this algorithm is the calculation of average discharging current (I_{av}) with respect to the amplitude of the power pulse (P) and the voltage window of the application (V_w) as given in (2.21)-(2.24).

$$V_w = V_{\max} - V_{\min} \tag{2.21}$$

$$I_{\max} = \frac{P}{V_{\min}} \tag{2.22}$$

$$I_{\min} = \frac{P}{V_{\max}} \tag{2.23}$$

$$I_{av} = \frac{I_{\max} + I_{\min}}{2} \tag{2.24}$$

After calculation of I_{av}, the parameter N which represents the number of series components within a branch of a UC module is calculated with respect to the rated voltage of the application (V_{app}) and a single UC cell (V_{rated}) as given in (2.25).

$$N = \frac{V_{app}}{V_{rated}} \tag{2.25}$$

In the next step, M which represents the number of parallel branches is initiated as one and voltage change of the module (ΔV) is calculated by considering the capacitance and ESR parameter of the module according to the values shown in Table 2.3, pulse duration (Δt), and I_{av} as given in (2.26).

$$\Delta V = \frac{I_{av} \times \Delta t}{C} + I_{av} \times R_s \tag{2.26}$$

After this calculation, ΔV is compared with V_w. If ΔV is higher than V_w, M is increased by one and the same procedure continues. On the other hand, if ΔV is lower than or equal to V_w, then the current values of N and M are accepted as the dimensions of the matrix formed UC module.

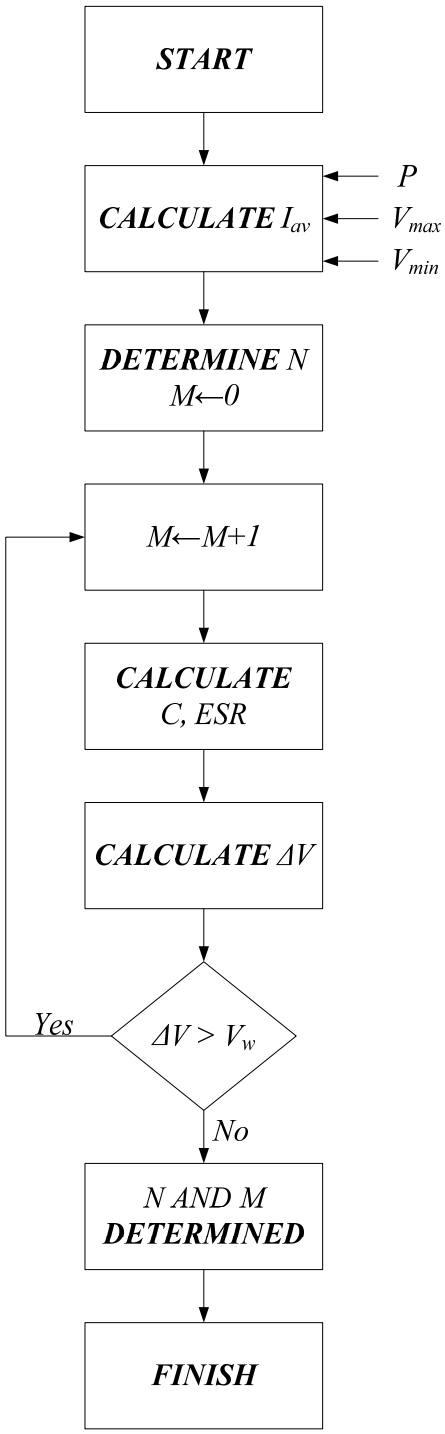

Figure 2.10 Flowchart of a UC module sizing algorithm.

2.5.1.4 Voltage Balancing Structures

When UCs are utilized in a module form composed of serially connected devices, the voltage of individual UCs shows diversity due to the differences in capacitance and EPR of each device [9-10], [29]. Linzen et al. state that voltage differences between the individual UC cells have to be minimized by utilizing voltage equalization circuits in order to provide a long life expectancy for the UC module [29]. According to the same reference, voltage balancing structures are classified into four groups as parallel resistor, zener diode, switched resistor, and DC-DC converter based balancing structures [29]. The schematic representations of balancing structures are shown in Figure 2.11.

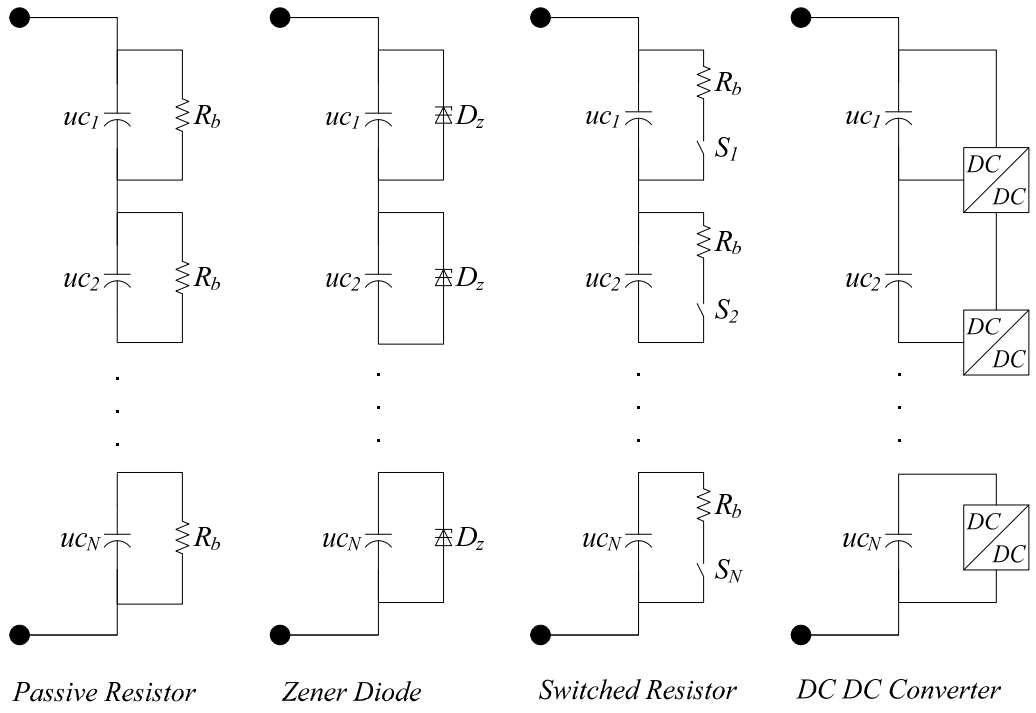

Figure 2.11 Schematic representations of voltage balancing structures [29].

The first voltage balancing circuit is the parallel resistor structure. Its operation is based on current diversion from the individual UCs in resting condition. Therefore, the terminal voltage of the UC module is distributed between the individual UCs with respect to the current drawn by the parallel resistors. If, the values of these

resistors are equal, terminal voltage of the module will be distributed equally. The selection of balancing resistors determines the speed of voltage balancing operation. With low valued balancing resistors, fast self discharge rates are obtained. Therefore, equalization of the individual UCs' terminal voltage will be fast. On the other hand, low valued balancing resistors increase the power loss of the module. Therefore, it could be concluded that there is a trade of between the balancing speed and power loss of the module [30].

The second balancing structure is based on zener diodes. In this structure, when the voltage of an individual UC goes above the voltage rating of the zener diode, voltage regulation is provided by the corresponding zener diode via diverting current from the individual UC. This structure is also based on power loss and temperature dependence of zener diodes is reported as a disadvantage of this structure [29].

Switched resistor configuration is the third balancing structure. The operating principle of this structure is based on diverting current from individual UCs when their voltage goes above a predetermined level [11]. To implement the control of this structure, hysteresis based voltage control mechanism which is shown in Figure 2.12 could be applied.

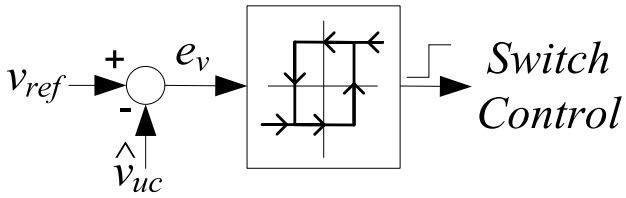

Figure 2.12 Block diagram of switched resistor control structure.

Switched resistor structure is a more efficient configuration when it is compared with the parallel resistor structure. However, voltage measurement and switch control requirements are the disadvantages of this structure [29].

The last voltage balancing configuration is the DC-DC converter based structure. In this method voltage equalization is obtained by means of energy transfer between the

individual UCs with respect to their voltage level. The most obvious advantage of this structure over the previous ones is the higher efficiency, since the power losses are subjected only in the DC-DC converters. On the other hand, integrating DC-DC converters to the module adds an extra cost to the system and it is difficult to implement this method when compared with the previous structures [29].

2.5.2 Thermal Criteria

UCs could be utilized in a wide temperature range since their energy storage mechanism is not based on electrochemical reactions [12], [26]. Operating and storing temperature range of some commercial products with organic electrolyte is summarized in Table 2.4 [3-6].

Table 2.4 Operating and storing temperature range of some UC products

Manufacturer	*Product Part Number*	*Operating Temperature Range*	*Storing Temperature Range*
Maxwell	BCAP 1500	-40 ^{o}C to 65 ^{o}C	-40 ^{o}C to 70 ^{o}C
Nesscap	ESHSR-1200C0-002R7A5	-40 ^{o}C to 65 ^{o}C	-40 ^{o}C to 70 ^{o}C
LS Mtron	HV Series	-40 ^{o}C to 60 ^{o}C	-40 ^{o}C to 70 ^{o}C
Ioxus	RSC2R7508SP	-40 ^{o}C to 70 ^{o}C	-40 ^{o}C to 70 ^{o}C

In the product guide of Maxwell Technologies, it is reported that the capacitance of their products remains constant within the full temperature range and ESR of their products increases as the temperature reduces. The increase in ESR for low temperatures is resulted from the reduction in the mobility of ions at low temperatures [12]. From the lifetime perspective of UCs, it is stated that capacitance decrease and ESR increase will be seen if the devices are kept at rated voltage and high temperature limit for long time duration and it is also recommended to maintain the device temperature at low levels for increasing the lifetime of devices [12].

According to the reported temperature effects, it could be concluded that temperature of UCs should not be kept very near to the high temperature limit for a long time. Therefore, UCs should be utilized with thermal management. The basic parameter of UCs that could be used in thermal management is the thermal resistance (R_{th}) value given in product datasheets. Temperature rise of the device (ΔT) could be expressed as a function of R_{th}, ESR (R_s), magnitude (I), and duty cycle (d) of the applied current as given in (2.27) and this equation should be considered for the thermal design of UC based energy storage systems [12].

$$\Delta T = I^2 \times R_s \times R_{th} \times d \tag{2.27}$$

2.5.3 Cycling Criteria

It is reported that 20 % reduction in capacitance will be encountered in one million charging and discharging cycles for the UC products of Maxwell Technologies [12]. This reduction in capacitance is accepted as the end of lifetime of the devices [3]. Since UCs could be utilized for a large number of cycling process, these devices could be easily integrated to the applications that require a large number of charging and discharging cycles.

2.6 Comparison of Ultracapacitors with Other Energy Storage Devices

Since UCs are relatively new devices, it is proper to compare them with other energy storage devices. In most of the studies that make comparisons between UCs and other energy storage devices, energy and power density, charge and discharge time, and cycle life parameters are taken into consideration. It is also important to compare UCs with different energy storage devices with respect to the cost consideration. UCs are compared with lead acid batteries and conventional capacitors in Table 2.5 by utilizing the information given by Maxwell Technologies [31].

Table 2.5 Comparison of UCs with other energy storage devices [31]

Parameter	*Lead Acid Battery*	*Ultracapacitor*	*Conventional Capacitor (Electrolytic)*
Charge Time	1 - 5 h	0.3 - 30 s	10^{-6} - 10^{-3} s
Discharge Time	0.3 - 3 h	0.3 - 30 s	10^{-6} - 10^{-3} s
Charge/Discharge Efficiency	0.7 – 0.90	0.85 – 0.98	>0.95
Energy Density (Wh/kg)	10 – 100	1 – 10	< 0.1
Power Density (W/kg)	<1,000	<10,000	<100,000
# of Cycles	<1,000	>500,000	>500,000

2.6.1 Energy and Power Density

In Table 2.6, different energy storage devices are compared with respect to the energy density parameter and it is seen that UCs are not an alternative to battery technology according to the energy density parameters presented in this table. On the other hand, it is also seen that the energy density of UCs are higher than conventional capacitors (e.g. electrolytic capacitors). From the power density point of view, it is obvious that power density of UCs is higher than batteries. On the conventional capacitor side, it is seen that power density of UCs are lower than power density of conventional capacitors. As a conclusion it could be said that UCs are suitable for applications that require high power pulses for long time duration.

It can also be concluded that, in some applications where large energy storage devices with high energy density are required, UCs may not be favorable. Energy storage device types like NaS batteries, li-ion batteries, fuel cells are good options for large energy storage applications. On the other hand, UCs can be viewed as a complementary technology for energy storage applications when high power density of UCs is considered.

Table 2.6 Comparison of different commercial energy storage devices with respect to energy density

Device	*Manufacturer*	*Part No*	*Energy (J)*	*Volume (ml)*	*Mass (g)*	*Energy Density*	
						(J/ml)	*(J/g)*
Sodium Sulfur (NaS) Battery	NGK	NAS T5 Cell [32]	4521600	33.508.475	5500	1349.39	822.11
Li-Ion Battery	Maxell	ICP803443AR	17982	11.09	25	1621.46	719.28
	Panasonic	CGR18650CG	29160	17.72	45	1645.32	648
Ni-Mh Battery	Panasonic	HHR900D	35640	52.194	170	682.84	209.65
	GP	GP1000DH	43200	51.34	175	841.45	246.86
Lead Acid (LA) Battery	Haze	UPS140	1416960	4056	11110	349.36	127.54
	Panasonic	LC-P127R2P	311040	973.95	2500	319.36	124.42
Ultracapacitor	Maxwell	BCAP1500	5467.5	325	320	16.82	17.085
	Nesscap	ESHSR-1200-C0-002R7A5	5832	242	335	24.1	17.41
Aluminum Electrolytic Capacitor	CDE	38LX273M100B102V	135	41.250	325	3.27	0.411

2.6.2 Charge and Discharge Time

When UCs and batteries are compared with respect to charge and discharge time, it is seen that UCs have shorter and symmetric charge and discharge time values. Therefore, it could be said that UCs can be both charged and discharged with high current levels which is not possible for batteries. On the conventional capacitor side, it is seen that charge and discharge time of these devices are extremely lower than UCs and batteries due to the low energy and high power density of these devices.

2.6.3 Cycle Life

Charging and discharging process of batteries is maintained by means of electrochemical reactions. Therefore, deformation effects are commonly encountered for batteries due to the oxidation and thermal impacts of electrochemical reactions. With this deformation effects, energy storage parameters of batteries start to deteriorate as they are being used [1]. On the other hand, deformation effects due to the charging and discharging process is lower for UCs compared to batteries since the energy storage mechanism of these devices is not based on electrochemical reactions. Therefore, cycle life parameter of UCs is higher than batteries. Similar explanation is also correct for conventional capacitors from the cycle life point of view.

2.6.4 Cost

The cost of the energy storage devices per unit energy storage capability is very important for the practical use of the energy storage devices. In this sense, a comparison of four different commercial energy storage devices is shown in Table 2.7 with respect to the unit cost and the energy storage capability of the devices which are obtained from the Digi-Key Corporation web site.

Table 2.7: Comparison of different commercial energy storage devices with respect to device cost (* www.digikey.com)

Device	*Manufacturer*	*Part No*	*Energy (kJ)*	Cost ($)	Cost/Energy
LA Battery	Panasonic	LC-R127R2P	311.040	35.51	0.114
Li-Ion Battery	Panasonic	BR-CSSP	54	10.2	0.19
UC	United Chemicon	DDSC2R5LGN242KS4BS	7.5	137.5	18.33
Al.Electrolytic Capacitor	United Chemicon	ESMH101V5N682MA50T	0.034	6.1	179.41

According to Table 2.7, it is seen that the cheapest energy storage device is the lead acid battery and this result explains why the use of lead acid batteries is very common in many energy storage applications. It is seen that the cost of the UC per unit energy storage capability is higher than the cost of batteries per unit energy storage capability. Therefore, it could be concluded that the use of UCs in energy storage applications will be common if the cost of the device decreases. On the other hand, it is also seen that the cost of the UC per unit energy storage capability is almost ten times lower than the aluminum electrolytic capacitor. Therefore, it could be concluded the use of UCs is cheaper than the use of aluminum electrolytic capacitors in energy storage applications.

2.7 Typical Applications of Ultracapacitors

In the present day, UCs have been started to be integrated to the systems with proper sizing in order to provide the whole or part of the power and energy requirements of applications. Due to the maintenance free structure and life increasing effect for other system components by supplying pulse power requirements, UCs are observed as devices that increase the reliability and performance of systems. Therefore, UCs are started to be used in applications such as consumer electronics, industrial systems, transportation engineering, and so on [12]. In general typical applications of UCs are classified as pulse power, bridge power, power quality, main power, and memory back up applications [12].

2.7.1 Pulse Power Applications

Since UCs are devices with low ESR and high capacitance values, these devices can supply the long duration pulse power requirements of applications as it is mentioned in the previous sections. A typical load profile of a pulse power application is shown in Figure 2.13.

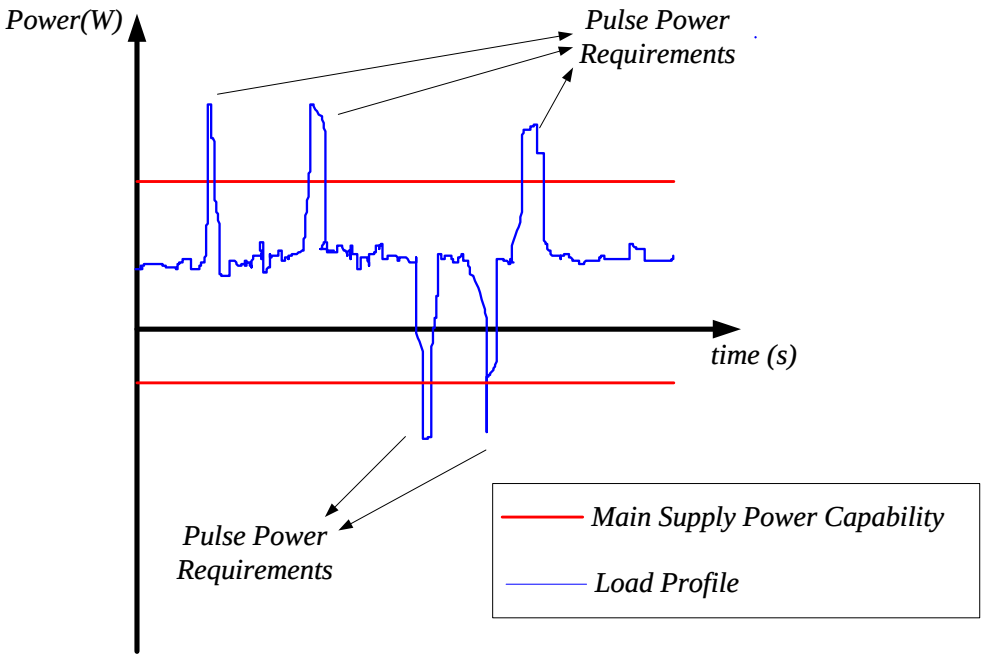

Figure 2.13 A typical load profile with pulse power requirements.

In applications that have a load profile similar to the one shown in Figure 2.13, it is a common practice to supply the average power requirements from devices like batteries, generators, or fuel cells and pulse power requirements from UCs [1]. Using UCs in order to supply the pulse power requirements prevents the aging of the devices that supply the average power requirements [12].

Supplying the pulse power requirement of an electric vehicle in the case of acceleration and storing the regenerative energy appeared in the case of braking is one of the most attractive applications of UCs in pulse power domain [12]. The use of UCs in these applications is provided by means of bi-directional DC-DC converters [33-34]. In these applications bi-directional DC-DC converters provide both charging and discharging operations of UCs. Block diagram of a UC assisted electric vehicle application is shown in Figure 2.14.

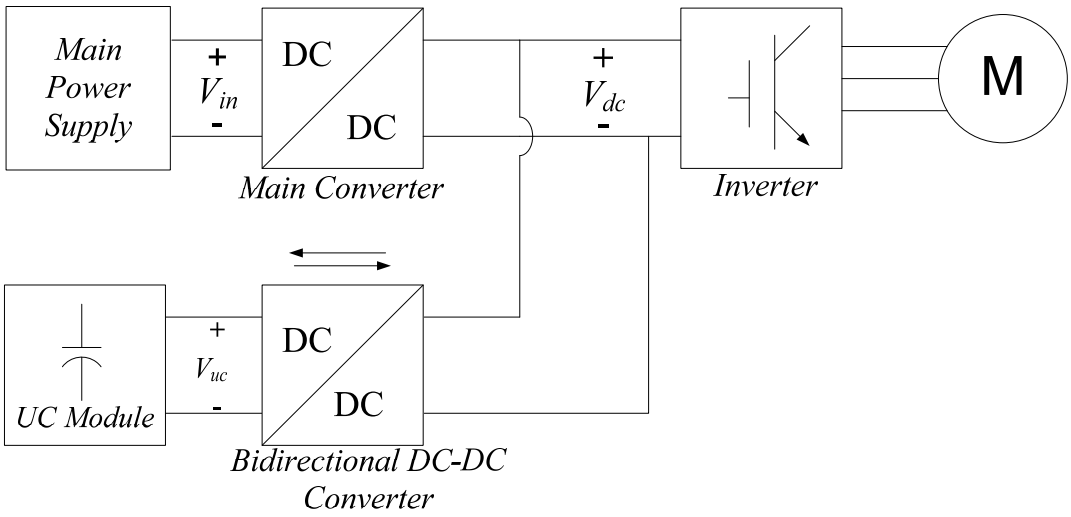

Figure 2.14 Block diagram of a UC assisted electric vehicle application.

UCs could also be utilized in variety of pulse power applications rather than the mentioned electric vehicle application. Supplying the pulse power requirements of portable electronic devices, starting internal combustion engines are some of the other UC applications in pulse power domain [12], [15].

2.7.2 Bridge Power Applications

Bridge power is a concept on providing power from an auxiliary supply in a transition period between the primary and secondary supplies. In this transition period, auxiliary supplies perform a bridge like operation. When energy and power density of UCs are considered, it is seen that these devices are capable of supplying the bridge power requirements of applications. Using UCs in uninterruptible power supplies (UPS) is one of the most common applications in this area [12]. In Figure 2.15, a UPS topology is shown where an internal combustion engine (ICE) alternator set is used as a secondary source and a UC module is used as an auxiliary source [35].

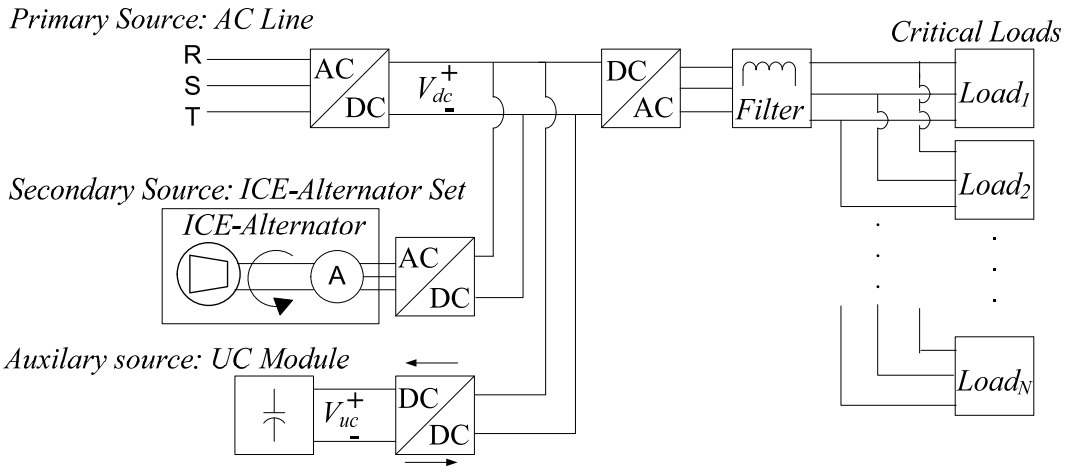

Figure 2.15 Block diagram of a UC assisted UPS application [35].

When the AC line is interrupted in the UPS structure shown in Figure 2.15, ICE-alternator set becomes effective and supplies the critical loads. However, a response time is necessary for the ICE-alternator set to fully regulate the system. In this topology, the power requirement of the system in the critical response time of ICE-alternator set is provided by means of the UC module which has a faster response time.

In conventional UPS systems, bridge power requirements are provided by means of battery blocks. However, battery blocks need to be maintained in predetermined time periods since the energy storage mechanism of these devices is based on electrochemical reactions. This situation increases the service cost of the UPS system in long time perspective [36]. On the other hand, service cost of a UC assisted UPS system is reduced since the aging behaviour of UCs is significantly slower than batteries.

2.7.3 Power Quality Applications

Today, inverter based motor drive systems are commonly used in most of the industrial processes [37-38]. The electrical power supplied to the motor drive systems should meet the power quality standards in order to obtain high quality

products from the output of industrial processes. One of the most common problems in this area is the voltage sag situation which is defined in IEEE Standard 1159-1995 “Recommended Practice for Electric Power Quality” as 10-90 % reduction in supply voltage in an half period of supply voltage waveform up to one minute. This condition is commonly encountered in industrial areas when the motor starting operations take action [39]. The mentioned short term decrease in supply voltage reduces the quality of manufacturing outputs. For example, in textile plants defected products are manufactured due to the voltage sags [39].

Voltage sags should be compensated in order to prevent faulty manufacturing outputs. This compensation concept is commonly known as “Riding Through Voltage Sags”. Therefore, if the motor drive system is integrated with a riding through compensation system better manufacturing results could be obtained. A riding through system is composed of a voltage sag sensing unit and an auxiliary source controlled by a power electronics converter [39]. UCs could be used as auxiliary sources in this perspective [15]. Block diagram of a UC assisted riding through system is shown in Figure 2.16 where the DC bus voltage is regulated by a UC module in the case of voltage sag.

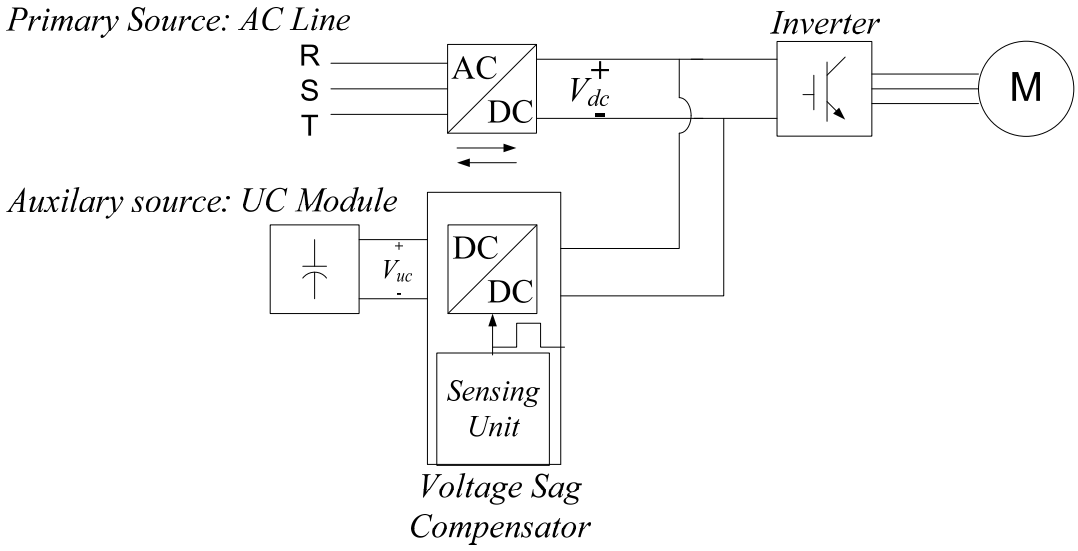

Figure 2.16 Block diagram of a UC assisted riding through system.

2.7.4 Main Power and Memory Back Up Applications

UCs could be used as a primary source in applications where the charge and discharge time values are small and power is required for short time durations. Supplying power to toys, flashlights, and emergency door power applications are the common examples in this area [12]. Besides the use of UCs as a primary energy source, another important area is the use of UCs in memory back up applications. UCs could be utilized for a memory backup purpose by means of maintaining them in a fully charged state to supply the memory units in critical conditions. In this sense, UCs have started to find application in automated meter reading (AMR), microcontroller and board memory areas [12], [15].

2.8 Conclusion

After investigating UCs from a structural and application based point of view, it is seen that these devices have started to find many applications due to the advantages of the devices in terms of energy, power, and cycle life considerations. However, distinctive properties of UCs such as voltage rating, thermal, and cyclic behaviour should be taken into consideration while designing UC based energy storage systems. On the comparison side, it is seen that UCs are between the conventional capacitors and batteries in terms of power and energy density. The advantages of UCs over batteries are also mentioned. Finally, typical applications of UCs are discussed by the help of information given in previous sections of this chapter. Given the basic background about UCs in this chapter, the performance evaluation of UCs will be covered in the next chapter.

CHAPTER 3

PERFORMANCE EVALUATION OF ULTRACAPACITORS

3.1 Introduction

UCs are relatively new devices compared to conventional technologies like batteries and conventional capacitors. Therefore, testing the performance of UCs is very important for both manufacturers and customers. From manufacturer point of view, product specifications should be expressed in datasheets and other documents with high reliability before they put their products into the market. On the customer side, UC performance should be evaluated before using. To evaluate the performance of UCs, many methods are put forward by researchers and manufacturers [21-22], [40-41]. The recommended tests for UCs are very similar to each other. However, to compare different products with each other, it is needed to standardize the test methods constituted by different manufacturers and researchers [21]. The standardized test methods should also be easy to apply.

Standard measurement devices like LCR meters are not sufficient for observing the UC characteristics experimentally. When the measurement probes of a digital LCR meter are connected to the terminals of a UC, commonly over range message is displayed on the measurement result screen of the digital LCR meter. This is resulted from the narrow measurement range of LCR meters. At this point it could be concluded that the signals applied by an LCR meter will not be adequate to create a measurable change in the terminal voltage of the UC under test that the measurement mechanism of LCR meters could sense.

In this study, experimental performance evaluation of UCs is realized by means of applying large DC current signals in order to measure the terminal electrical response of the UC under test. In this sense, to perform the UC tests based on applying large DC current signals, a test system that is capable of applying large DC current signals to the UC in charging and discharging modes is required. In this chapter, the necessary properties of a UC test device and test procedures put forward by researchers and manufacturers are investigated in order to mention the importance of UC testing.

3.2 Requirements of an Ultracapacitor Test Device

Basically, a UC test device could be defined as a device that has the ability of applying large DC current signals to UCs as it is also mentioned in the introductory part. The requirements of a UC test device are summarized in the following sections.

3.2.1 Voltage Range

Voltage rating is the most critical parameter of a UC. Therefore, a UC test device should apply the tests to the UCs within the voltage window of the devices and the terminal voltage of the UCs under test should not exceed the voltage rating during the tests. On the other hand, voltage range of the test process should be adjustable for testing products with different voltage ratings.

3.2.2 Applied Signal

The output of a UC test device is a large DC current signal in order to create a measurable difference in the terminals of a UC. Adjustment of the applied signal parameters and control of the applied signal in terms of dynamic and steady state performance parameters are very important for a UC test device. UC test devices

should adjust the amplitude and test profile of the applied signal in order to apply predetermined current profiles to the UCs under test. The current control method used inside the test device should create output current signals with low steady state error and the dynamic behaviour of the applied current in terms of rise and fall times should be fast enough. Also a current limiting function should be included within the test device for safety reasons.

3.2.3 Cycling Property

A UC test device should be capable of putting UCs in a test process where thermal and cyclic behaviour of the devices could also be observed. The number of test cycles that will be applied to the UCs should be adjustable in order to observe the cyclic behaviour of UCs for different test cycles.

3.2.4 Measurement, Data Acquisition and Parameter Evaluation

A UC test device should measure the terminal voltage, current and temperature of UCs under test. The measured signals should be recorded and transmitted to a digital platform that has the ability of performing calculations to generate the results of the tests. Test results should include at least the basic electrical parameters of the UCs, such as capacitance, ESR and EPR. More detailed calculations could also be included such as energy and power density. One of the key properties of this part is to use a measurement system with proper sampling time and proper data acquisition system.

3.2.5 Documentation

In order to achieve the test results, a UC test device should generate the results of the tests as a hard copy or in a digital format.

3.3 Building Blocks of an Ultracapacitor Test Device

Based on the requirements mentioned in section 3.2, a UC test device is composed of a charge and discharge energy management system, a parameter adjustment part, a measurement and data acquisition system, and a digital platform. Block diagram of a UC test device is shown in Figure 3.1.

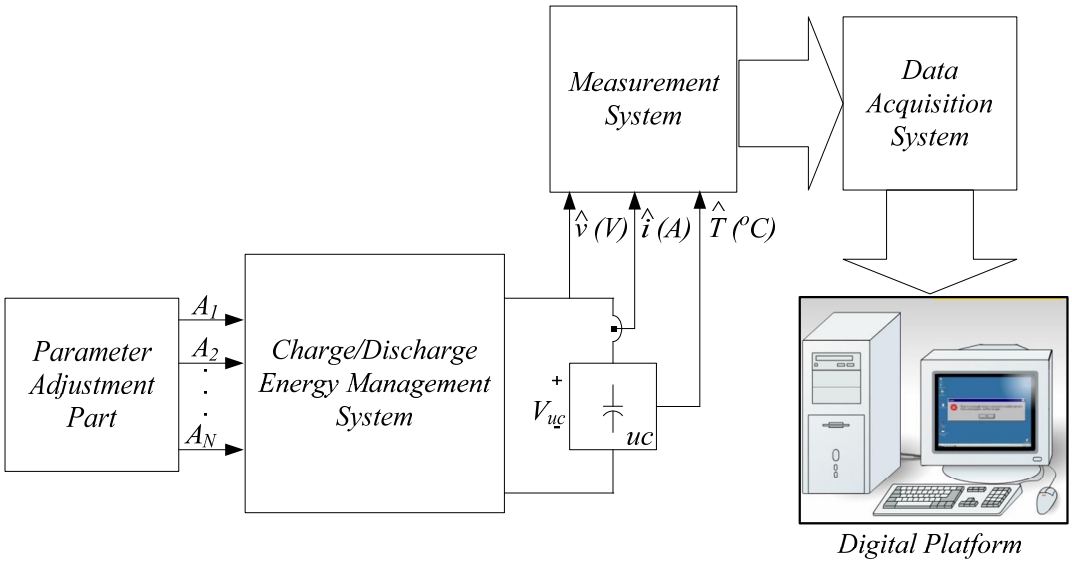

Figure 3.1 Block diagram of a UC test device.

3.3.1 Charge and Discharge Energy Management System

Charge and discharge energy management system is the main part of a UC test device. By means of this part, predetermined current profiles are applied to the UCs under test.

3.3.2 Parameter Adjustment Part

Parameter adjustment part is a peripheral unit that provides the information about the tests. Test information varies according to the properties of the UC test device. At

least magnitude and profile of the applied current, type of the UC test, and number of test cycles information should be adjusted by means of this part.

3.3.3 Measurement System

By means of a measurement system, current, voltage, and temperature variation of the UCs under test are measured and fed to the data acquisition system.

3.3.4 Data Acquisition System

By means of a data acquisition system, measurement information is sent to a digital platform to obtain the results of the tests.

3.3.5 Digital Platform

Digital platform is the part where calculations are performed in order to generate the test results. This part also achieves the test results in a digital format.

3.4 Test Procedures for Performance Evaluation of Ultracapacitors

Both manufacturers and researchers propose large signal DC tests for performance evaluation of UCs [21-22], [40-41]. The recommended tests in manufacturer application notes and researcher studies show how basic electrical parameters such as capacitance, ESR, and EPR as well as some performance parameters like energy and power density, thermal, and cyclic behaviour of UCs can be evaluated. In this section, some of the test procedures of UCs are reviewed by the help of the methods shown in [21] and [41].

3.4.1 Constant Current Tests

Constant current tests are used to evaluate the constant current charging and discharging characteristics of UCs [21]. As a result of constant current tests, capacitance and ESR parameters of UCs could be obtained. In this test method, UCs are put into a constant current charging and discharging cycle between the rated voltage (V_{rated}) and half of the rated voltage ($V_{rated}/2$). The test procedure could be explained according to the information given in [21] and [41]. The first step of the procedure is short circuiting the UC to which the test procedure will be applied and keeping it at zero charge level for at least one hour before starting the tests. After this operation, the UC is charged with constant current from zero volts to the rated voltage. As soon as the terminal voltage of the UC reaches the rated voltage level, charging current is interrupted and no current is applied for at least five seconds in order to stabilize the terminal voltage of the device. After the resting time required for voltage stabilization is passed, UC is discharged with constant current until the terminal voltage of the device reaches half of the rated voltage level. As soon as the terminal voltage of the UC reaches half of the rated voltage level, discharging current is interrupted and no current is applied for at least five seconds in order to stabilize the terminal voltage of the UC. After this operation, charging and discharging process is continued for the number of cycles determined before the test. Constant current test procedure mentioned in this section is shown in Figure 3.2.

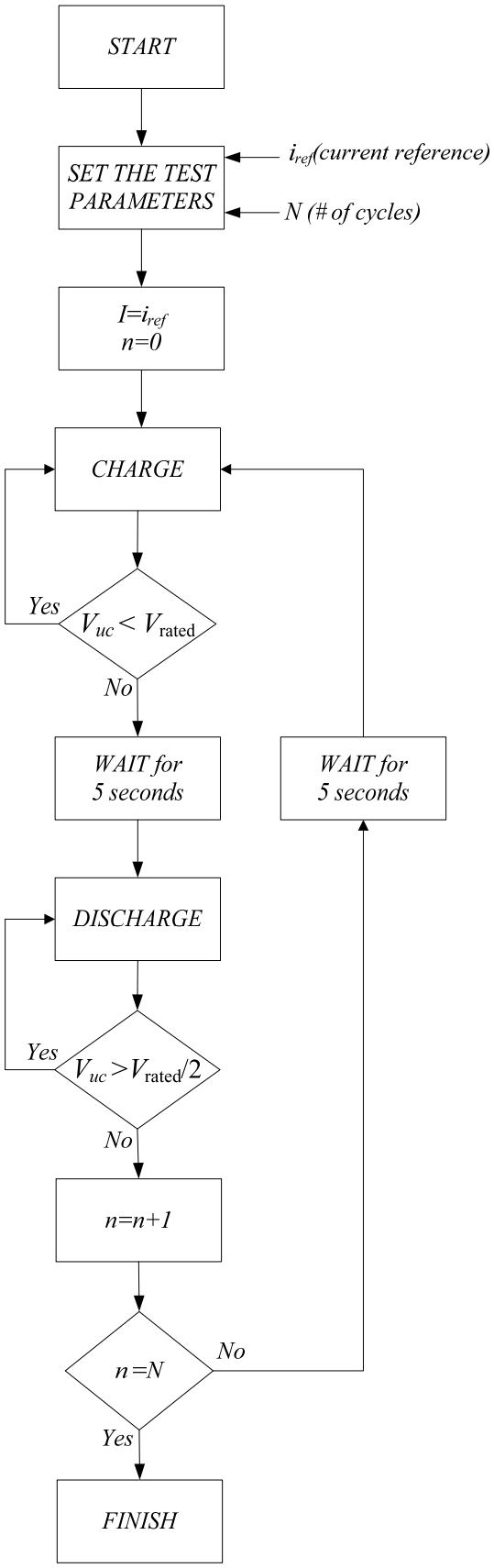

Figure 3.2 Constant current test procedure.

In order to obtain the results of constant current test procedure, voltage and current variation of UCs should be recorded. A typical voltage and current profile of a UC under constant current test is shown in Figure 3.3.

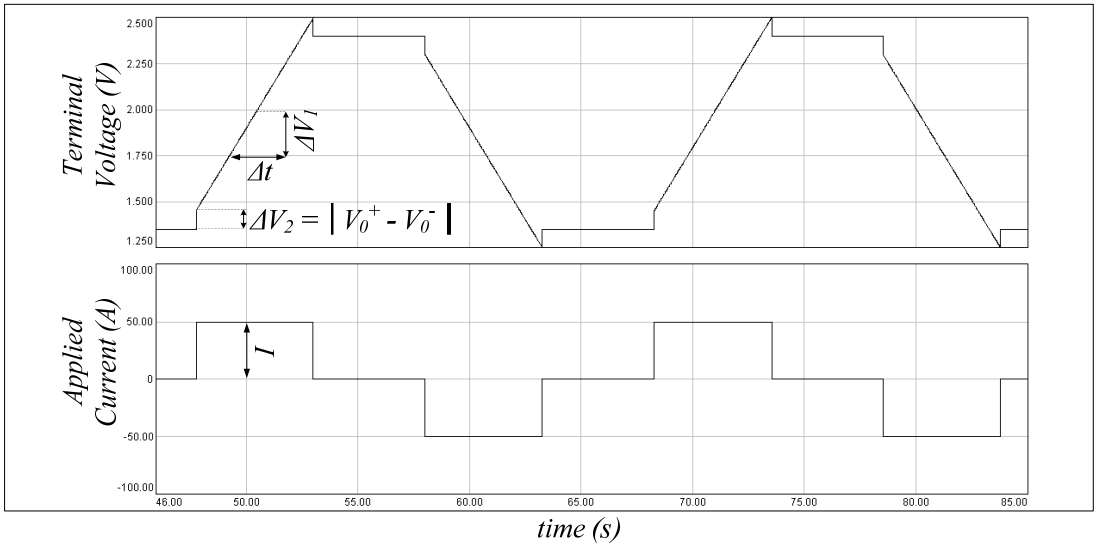

Figure 3.3 A typical voltage and current profile of a UC under constant current test.

The capacitance (C) and ESR (R_s) parameters of UCs can be evaluated by considering the profile shown in Figure 3.3. The capacitance parameter is calculated by considering the linear portions of the terminal voltage variation (ΔV_1), magnitude of the applied current (I), and the time period of the linear voltage variation (Δt) as given in (3.1). ESR of the UC module is calculated by means of dividing the voltage difference (ΔV_2) occurred when the current is applied or terminated by the magnitude of the applied current (I). The sudden voltage difference (ΔV_2) is calculated by means of subtracting the UC terminal voltage before applying or terminating the current signal (V_0^-), from the UC terminal voltage after applying or terminating the current signal (V_0^+) as given in (3.2).

$$C = \frac{I \times \Delta t}{\Delta V_1} \tag{3.1}$$

$$R_s = \frac{|\Delta V_2|}{I} = \frac{\left|V_{0^+} - V_{0^-}\right|}{I} \tag{3.2}$$

It is recommended to evaluate the capacitance and ESR parameters for both charging and discharging cases and observe the repeatability of the constant current test procedure for different cycles of the test [21].

3.4.2 Constant Power Tests

Constant power tests are used to evaluate the constant power discharging characteristics of UCs [21]. In the Electric Vehicle Capacitor Test Manual prepared by Miller and Burke [21], it is recommended to charge the UC with constant current and discharge it with constant power for realizing the constant power tests. The remainder of the test procedure is similar to the flowchart shown in Figure 3.2. By the help of the constant power tests, round trip cycle efficiency (η_{rt}) of UCs could be obtained by integrating and proportioning the recorded voltage and current profiles of the discharging and charging phases as given in (3.3). Round trip cycle efficiency is defined as the ratio of energy expressions in discharging and charging phases which is an important parameter for electric vehicle applications [21].

$$h_{rt} = \frac{\int_0^{\Delta t_{discharge}} v_{uc}(t) \times i_{uc}(t) \times dt}{\int_0^{\Delta t_{charge}} v_{uc}(t) \times i_{uc}(t) \times dt} \tag{3.3}$$

3.4.3 Leakage Current Tests

The leakage current parameter given in product datasheets is an indicator of the static loss of UCs in resting condition [21]. The leakage current parameter is modeled as the EPR in the electrical equivalent circuit model shown in Figure 2.7. The schematic representation of a leakage current test circuit suggested in [21] is shown in Figure 3.4.

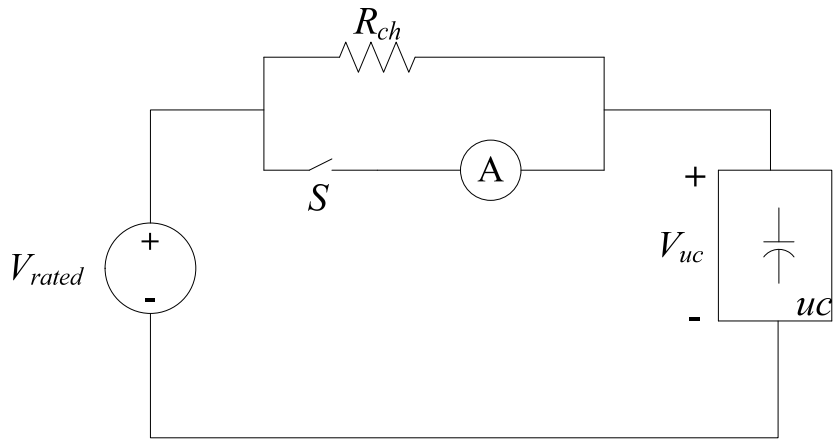

Figure 3.4 Schematic representation of a leakage current test circuit.

The leakage current test procedure expressed in [21] could be summarized by utilizing the test circuit shown in Figure 3.4. In this procedure, the UC that the leakage current test will be applied is charged from a constant voltage DC supply with a series charging resistor (R_{ch}). The supply voltage is set to the rated voltage of the UC (V_{rated}), where as R_{ch} is chosen with respect to the current rating (I_{supply}) of the supply as given in (3.4).

$$R_{ch} = \frac{V_{rated}}{I_{supply}} \tag{3.4}$$

When the terminal voltage of the UC reaches its rated voltage, R_{ch} is bypassed by a switch (S). Finally, the current in the bypassed branch is measured as the leakage current ($I_{leakage}$) measurement. The total measurement period is proposed as three hours and it is recommended to record measurements at every one minute for the first hour and record measurements at every five minutes for the remaining two hours [21]. The EPR (R_p) parameter could be obtained by means of dividing the rated voltage of the UC with the measured leakage current value as given in (3.5).

$$R_p = \frac{V_{rated}}{I_{leakage}} \tag{3.5}$$

3.4.4 Self Discharge Tests

Self discharge tests are performed to evaluate the self discharge characteristics of UCs after they are charged to the rated voltage level [21]. Self discharge test procedure could be summarized by utilizing [21]. In this procedure, the UC to which the test procedure will be applied is charged to its rated voltage level and then held at this voltage level for 30 minutes as the initial step. Then, the UC under test is open circuited from the supply and voltage variation is investigated for 72 hours. Self discharge value (*SD(Volts), SD (%)*) and self discharge loss factor (SDLF) of the UC, that will be obtained as a result of the mentioned test procedure are given in (3.6)-(3.8).

$$SD(Volts) = \left| V_{final} - V_{rated} \right| \tag{3.6}$$

$$SD(\%) = \left| 100 \times \frac{V_{final} - V_{rated}}{V_{rated}} \right| \tag{3.7}$$

$$SDLF = 1 - \left(\frac{V_{uc}}{V_{rated}} \right)^2 \tag{3.8}$$

3.4.5 Cycle Life Tests

Cycle life tests are performed in order to evaluate the cycle life of UCs. Cycle life is a very important parameter, since UCs should be replaced before the end of their cycle life. For this reason, it is proper to evaluate the cycle life of UCs and use this value as a design criterion. To perform cycle life tests, constant current charging and discharging process is applied to UCs and it is recommended to select the magnitude of the test current such that it is able to charge the UC from $V_{rated}/2$ level to V_{rated} level in several tens of seconds [21]. During the tests, a predetermined number of charging and discharging cycles are applied. The capacitance and ESR should be

investigated periodically during the test. The cycle at which the capacitance is reduced 20 % should be recorded as the cycle life of the device [21], [42].

3.4.6 Temperature Performance Tests

The purpose of temperature performance tests is to observe the performance of UCs at different temperatures. Temperature performance tests are realized by putting UCs in a temperature controlled chamber. Miller and Burke recommend repeating the tests mentioned in this chapter at temperatures 25±3^{o}C, -30±3^{o}C, and 65±3^{o}C [21].

3.4.7 Aging Tests

Aging tests are performed in order to evaluate the performance of UCs under accelerated aging conditions. Aging tests are realized by means of putting the UCs that are charged to the rated voltage level in a temperature controlled chamber of 70^{o}C. The terminal voltage of UCs should be maintained constant at rated voltage level during the tests. UCs are left in the accelerated condition for predetermined time intervals and at the end of each time interval test procedures mentioned in this chapter are repeated [21].

3.5 A Commercial Ultracapacitor Test System

In the previous sections, UC testing issue is covered in terms of UC test device requirements and UC testing methods. To evaluate the performance of UCs, test devices that are capable of performing high resolution measurements with fast and reliable data acquisition are needed. Furthermore, automatic parameter calculations based on the UC measurements is a good option. At this point, it could be concluded that, state of art UC test systems are necessary to perform advanced studies on UCs.

For this reason, a commercial UC test system “ARBIN Supercapacitor Testing System (SCTS)**”** is investigated in this section.

ARBIN Instruments is a company specialized on testing equipments for energy storage devices such as batteries, fuel cells, and UCs. Their product, SCTS which is shown in Figure 3.5, provides good options for UC testing [43]. ARBIN presents SCTS in three circuit technology options as linear bipolar, linear unipolar, and pulse width modulation (PWM). They also claim that SCTS could be configured according to customer requirements. The specifications of a standard SCTS product are summarized in Table 3.1 with respect to the information given in the product brochure [43].

Figure 3.5 ARBIN Instruments SCTS [43].

Table 3.1 Specifications of ARBIN Instruments SCTS [43]

System Specifications	Current Range	1 uA - 2000A
	Current Rise Time	20us - 2ms
	Voltage Range	0 - 56V
	Power Range	0 - 60kW
	Maximum Number of Test Channels	20 or 48 channels (independent)
Control Circuitry, Measurements	ADC/DAC	16 bits
	Voltage Clamping Time	< 1 ms
	Leakage Current Measurement Accuracy	0.02-0.2 uA (for a FS of ±10-100uA)
	AC Impendence Measurements	200Hz, 500Hz, 1kHz, 2kHz
Test Modes	Standard Procedures	Constant Current-Power ext…
	User Defined Procedures	Simulation Regime Mathematical Formula
Digital Platform	Built in Software	MITS Pro
	Calculations	ESR, EPR, Capacitance, Power, Energy, and user defined routines

3.6 Conclusion

In this chapter, UC testing issue is investigated in a general perspective. It is seen that, performance evaluation of UCs is important for both customers and manufacturers. Besides, the requirement of specialized test equipments for testing of UCs is shown, since standard measurement devices are not sufficient to perform the UC tests based on applying large DC signals. It can also be concluded that, to obtain the UC performance more accurately, state of art UC test equipments could be utilized.

CHAPTER 4

POWER ELECTRONICS INTERFACES FOR ULTRACAPACITORS

4.1 Introduction

Constructing a UC test system is important for the evaluation of UC performance parameters as mentioned in Chapter 3. On the other hand, designing a UC test system could be viewed as the primary step to see how these new energy storage devices could be utilized in applications. If the issue is simplified from the application point of view, it is observed that the basic operations are charging and discharging of UCs with respect to the given specifications. At this point, it is seen that power electronics converters could be utilized to control the charging and discharging processes of UCs. Therefore, in this chapter the use of power electronics converter topologies is investigated in order to perform the charging and discharging operations of UCs.

4.2 Charging of Ultracapacitors

Charging of UCs is the primary operation of UC test systems and UC based applications and it has some unique characteristics. The first characteristic is about the symmetric charging and discharging rates of the device. UCs could be charged with high current levels unlike batteries [44]. High RC time constant property of UCs should also be taken into consideration while designing a charging supply. Because, during the charging operation, the voltage difference between the input and output of the charging supply will be very high. Therefore, linear regulators could not be used for charging of UCs [44]. Another important property of UC charging issue is the

short circuit behaviour of UCs at zero charge level. For this condition, charging equipment should have a current limiting function [44]. One more important property of the charging supplies is the adjustable charging current requirement from the UC testing point of view. The last and most important property of the charging supplies is the requirement for continuous terminal voltage monitoring in order to prevent overvoltage conditions. To fulfill these requirements of UC charging operation, DC-DC converters could be utilized which is also recommended by the UC manufacturers [44].

4.2.1 Charging Circuit Topology

The step-down DC-DC converter is commonly used for UC charging applications since the charging current of this topology has a continuous characteristic. This property is very important for a UC charger that will be used in a UC test device since the adjustment of charging current is required. The schematic representation of a step-down DC-DC converter based UC charger is shown in Figure 4.1.

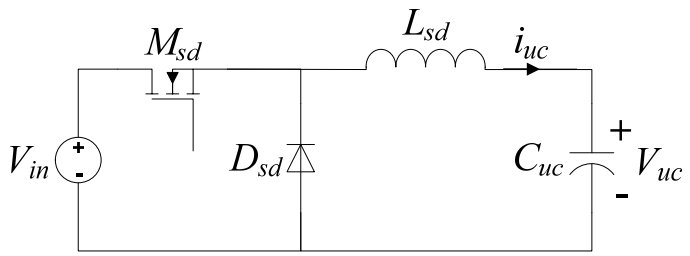

Figure 4.1 Schematic representation of a step-down DC-DC converter based UC charger.

The operation of the step-down DC-DC converter is based on pulse width modulated (PWM) operation of the controlled switch M_{sd}. The operating modes of the step-down DC-DC converter are shown in Figure 4.2 and a typical steady-state charging current waveform (i_{uc}) in continuous conduction mode (CCM) together with the duty cycle signal (d) is shown in Figure 4.3.

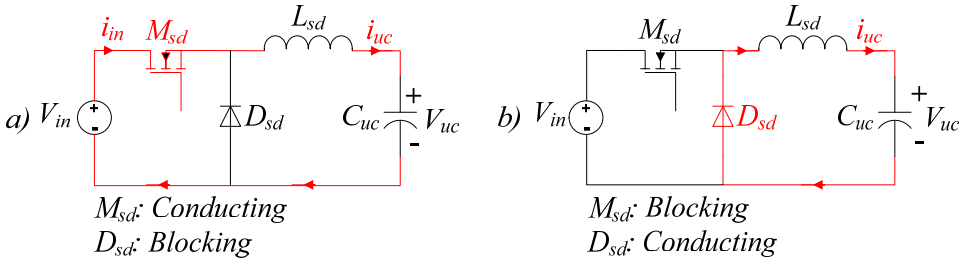

Figure 4.2 Operating modes of a step-down DC-DC converter based UC charger: (a) M_{sd} is in conduction mode, (b) M_{sd} is in blocking mode.

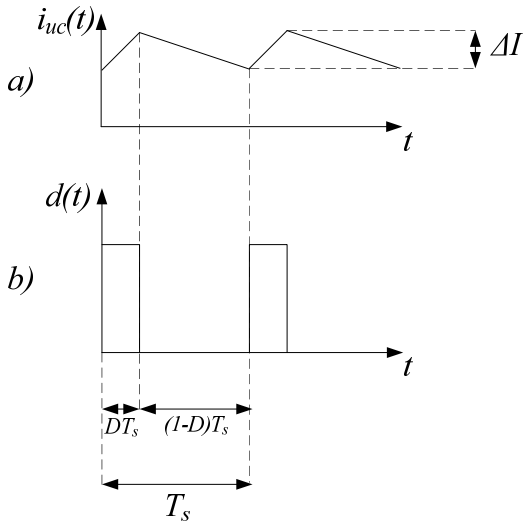

Figure 4.3 A typical steady-state charging current waveform of a step-down DC-DC converter based UC charger in CCM: (a) charging current waveform, (b) PWM signal.

According to Figure 4.2 and Figure 4.3, rise and fall rates of the charging current (di_{uc}/dt) and the steady-state charging current ripple (ΔI) are expressed in (4.1)-(4.3) with respect to the steady-state value of duty cycle (D) and switching period (T_s).

$$\frac{di_{uc}(t)}{dt} = \frac{V_{in}(t) - V_{uc}(t)}{L} \qquad \text{during } DT_s \tag{4.1}$$

$$\frac{di_{uc}(t)}{dt} = \frac{-V_{uc}(t)}{L} \qquad \text{during } (1\text{-}D)T_s \tag{4.2}$$

$$\Delta I = \frac{V_{in}(t) - V_{uc}(t)}{L} \times DT_s = \frac{V_{uc}(t)}{L} \times (1-D)T_s \tag{4.3}$$

As given in (4.1) and (4.2), the charging current (i_{uc}) rises when M_{sd} is in conducting mode and falls when M_{sd} is in blocking mode. It is also seen that, the steady-state charging current ripple (ΔI) could be decreased by selecting high values for the inductance (L_{sd}) and switching frequency.

When the two operating modes of the UC charging structure and the total parasitic resistance value of the converter inductor and UC (R_{eq}) are considered together, an average model shown in Figure 4.4 is obtained.

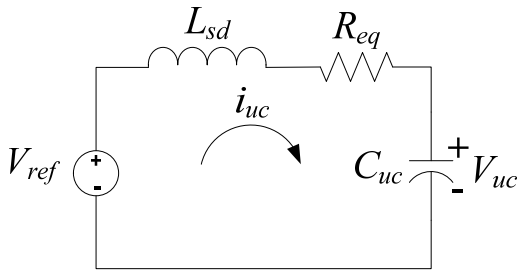

Figure 4.4 Schematic representation of the average model for the UC charging structure.

In the model shown in Figure 4.4, reference voltage parameter (V_{ref}) represents the average value of the input voltage of the RLC circuit constituted by the converter inductance (L_{sd}), total parasitic resistance (R_{eq}), and the UC capacitance (C_{uc}). In this configuration, V_{ref} is generated by the step-down DC-DC converter. The model shown in Figure 4.4 could also be simplified to a first order model, if the terminal voltage of the UC (V_{uc}) is assumed constant within a switching period (T_s) and included inside a new reference voltage (V_{ref}^*) value. This is a valid assumption, since the variation of V_{uc} is very small in a switching period. V_{ref}^* could be viewed as the voltage value that is necessary to put the charging current in a predetermined profile and it is given in (4.4).

$$V_{ref}^* = V_{ref} + V_{uc} \tag{4.4}$$

If the duty cycle parameter is adjusted according to V_{ref}^{*} value as given in (4.5), it could be concluded that the simplification process is completed.

$$D = \frac{V_{ref}^{*}}{V_{in}} \tag{4.5}$$

The first order decoupled model of the UC charging structure obtained by means of the simplification process is shown in Figure 4.5.

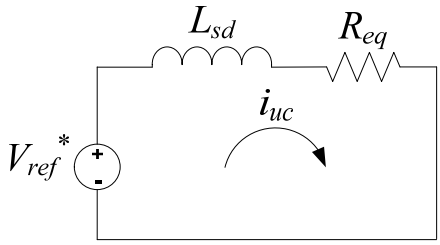

Figure 4.5 Schematic representation of the first order simplified model of the UC charging structure.

4.2.2 Control System of the Charging Circuit

Control system of the charging circuit should be based on current control since it is needed to put the charging current in a predetermined current profile. In other words, the charging current should track the current profile determined by the users. Block diagram of a current control structure for the simplified first order model is shown in Figure 4.6.

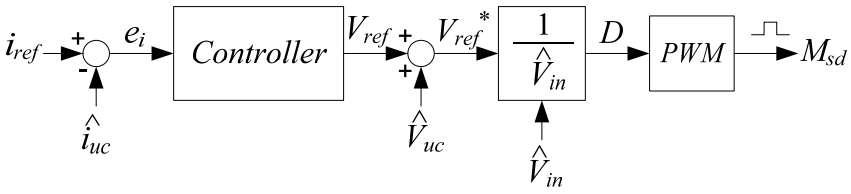

Figure 4.6 Block diagram of a current control structure for a UC charger.

As shown in Figure 4.6, the first step of the control process is the calculation of the current error (e_i) between the reference current (i_{ref}) and the measured charging current ($\hat{i}_{uc}$). After the error calculation, e_i is fed into the controller. The function of the controller is to generate a voltage reference signal (V_{ref}) with respect to e_i. If $\hat{i}_{uc}$ is higher than i_{ref}, V_{ref} is reduced, whereas V_{ref} is increased for the opposite condition. In the next step, the voltage reference signal is added with the measured UC terminal voltage ($\hat{v}_{uc}$) to decouple the effect of UC terminal voltage from the current control system. By the help of this load voltage decoupling mechanism, the voltage reference signal of the first order model (V_{ref}^*) is obtained. After the determination of V_{ref}^*, duty cycle of the system (D) is calculated by proportioning V_{ref}^* with the input voltage ($\hat{v}_{in}$) by means of a scaling operation in order to provide line voltage regulation.

The input voltage scaling part shown by a division operation in Figure 4.6 is one of the most important operations of a current controlled UC charging circuit. Because, to design a suitable UC charging structure the variations in the input voltage should be taken into consideration, since the rise and fall characteristics of the charging current is dependent on the input voltage (V_{in}). In practice, the input voltage is provided to the charging structures by means of unregulated DC power supplies. In this sense, AC utility followed by a step-down transformer, a diode bridge, and a large valued filter capacitor could be used to supply the input voltage requirement of the charging circuit as shown in Figure 4.7.

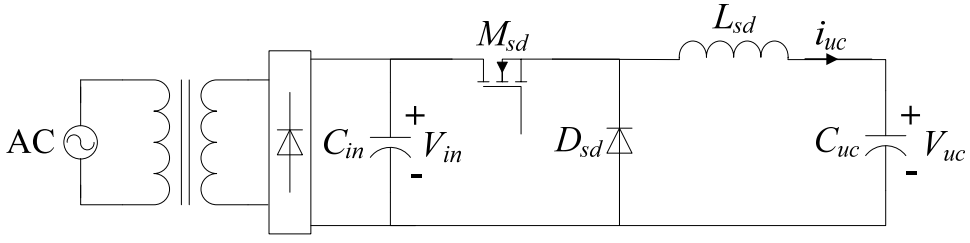

Figure 4.7 Schematic representation of a UC charger supplied by an unregulated DC supply.

The input voltage (V_{in}) of the UC charger shown in Figure 4.7 decreases as the power drawn from the input is increased. Therefore, it is needed to consider the decrease in V_{in} inside the scaling part of the control structure shown in Figure 4.6. The necessary operation is to increase D as V_{in} decreases. After the scaling operation, D is fed into a pulse width modulator (PWM) to generate the switching signal responsible for the control of M_{sd} as a final step of the current control process.

For the controller structure shown in Figure 4.6, proportional integral type (PI) controllers could be used due to easiness of implementation. The implementation details of the charging control structure are expressed in Chapter 5.

4.3 Discharging of Ultracapacitors

Discharging of UCs is the other basic operation of UC test systems and UC based applications. UC discharging issue has also some unique characteristics. In this sense, the first property is the high current handling capability of UCs. Therefore, UCs could be utilized in high current discharging applications. Another property of UCs during the discharging process is the decrease of their terminal voltage. Therefore, the discharging system should adjust its operation according to the decrease in the terminal voltage of UCs. Monitoring the terminal voltage during discharging operation could also be necessary for some applications. Because, the stored energy inside the UCs may not be adequate to fulfill the discharging requirements under certain state of charge levels. The last property of UC discharging issue from the UC test system point of view is the requirement for adjusting the system operation with respect to the user defined current profiles. To provide these requirements of UC discharging operation, DC-DC converters could be utilized.

4.3.1 Discharging Circuit Topology

Step-up DC-DC converters are commonly used for the discharging operation of UCs. By using step-up DC-DC converters, continuous discharging current requirement of UC test systems and high voltage requirements of applications are fulfilled together. The schematic representation of a step-up DC-DC converter based UC discharger is shown in Figure 4.8.

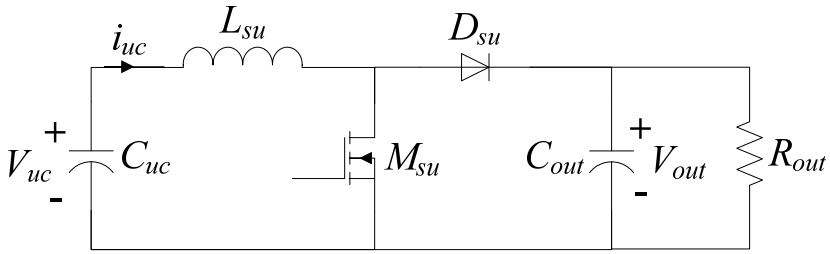

Figure 4.8 Schematic representation of a step-up DC-DC converter based UC discharger.

The operation of the UC discharging circuit is provided by means of controlling the switching signal of M_{su}. The operating modes of the step-up DC-DC converter based UC discharging circuit are shown in Figure 4.9.

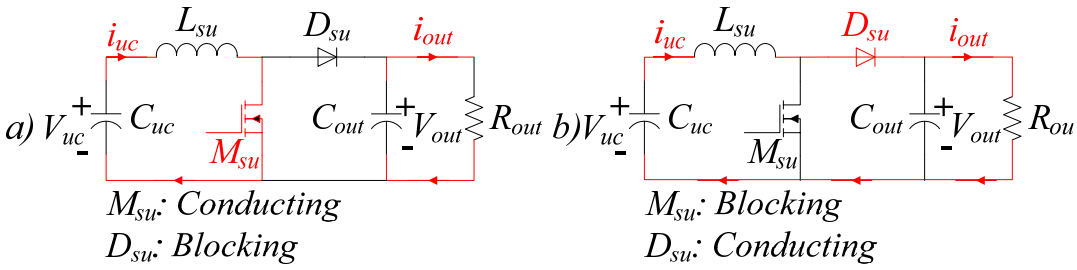

Figure 4.9 Operating modes of a step-up DC-DC converter based UC discharger: (a) M_{su} is in conduction mode, (b) M_{su} is in blocking mode.

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A typical steady-state variation of discharging current waveform (i_{uc}) in CCM for PWM operation of M_{su} is shown in Figure 4.10 together with the duty cycle signal (d).

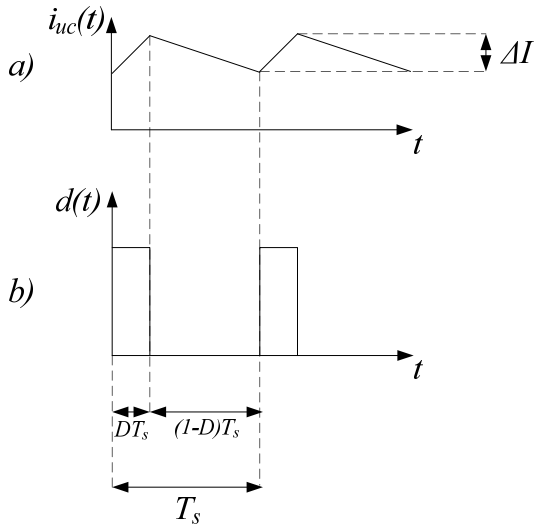


Figure 4.10 A typical steady-state discharging current waveform in CCM for PWM operation of step-up DC-DC converter based UC discharger: (a) discharging current waveform, (b) PWM signal.

According to Figure 4.9 and Figure 4.10, rise and fall rates of the discharging current (di_{uc}/dt) and the steady-state current ripple (ΔI) are expressed in (4.6)-(4.8) with respect to the steady-state value of the duty cycle (D) and switching period (T_s).

$$\frac{di_{uc}(t)}{dt} = \frac{V_{uc}(t)}{L} \qquad \text{during } DT_s \tag{4.6}$$

$$\frac{di_{uc}(t)}{dt} = \frac{V_{uc}(t) - V_{out}(t)}{L} \qquad \text{during } (1\text{-}D)T_s \tag{4.7}$$

$$\Delta I = \frac{V_{uc}(t)}{L} \times DT_s = \frac{V_{out}(t) - V_{uc}(t)}{L} \times (1-D)T_s \tag{4.8}$$

As given in (4.6)-(4.8), discharging current rises when M_{su} is in conducting mode and falls when M_{su} is in blocking mode. It is also seen that the steady-state current ripple (ΔI) could be decreased by means of selecting high values for the inductance (L_{su}) and switching frequency.

4.3.2 Control System of the Discharging Circuit

A current controlled system is necessary for a UC discharging system in order to provide the adjustable discharging current requirement. Block diagram of a current control structure for a UC discharging system is shown in Figure 4.11.

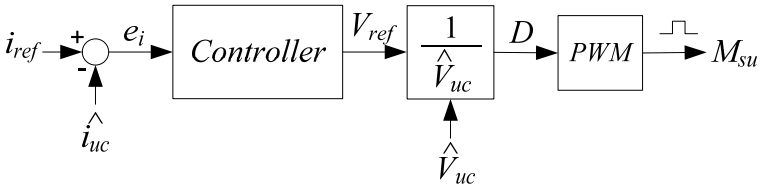


Figure 4.11 Block diagram of a current control structure for a UC discharger.

The first step of the control structure shown in Figure 4.11 is the calculation of the current error (e_i). After this operation, a voltage reference parameter (V_{ref}) is generated by the controller with respect to e_i. The operation principle of the controller is similar to the one shown for the charger case. If the discharging current is higher than the reference, V_{ref} is reduced, whereas V_{ref} is increased for the opposite condition. After the calculation of V_{ref} , duty cycle value (D) is calculated by means of proportioning V_{ref} with the measured UC voltage ($\hat{V}_{uc}$). This part is very important for proper operation of UC discharging circuit since the terminal voltage of a UC decreases during the discharging process. As a final step, D is fed into a pulse width modulator (PWM) to generate the switching signals responsible for the control of M_{su}. For the current controller structure, PI controllers could be used due to easiness of implementation. The implementation details of the control structure are expressed in Chapter 5.

To obtain better performance from a current controlled UC discharging system, the effects of output voltage variations should be minimized. Because, the input voltage varies as the discharging process continues. If the output voltage also varies in addition to the variation in the input voltage, controlling the discharging current could be difficult in terms of rise and fall characteristics. Therefore, using a load structure that has the ability of maintaining the output voltage constant will be proper

for a step-up DC-DC converter based UC discharging system. In this sense, a DC chopper structure could be utilized at the output of a step-up DC-DC converter based UC discharging system as shown in Figure 4.12.

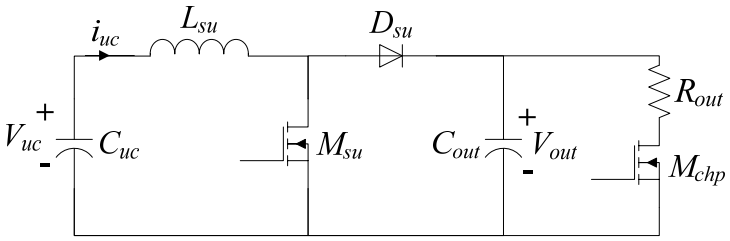


Figure 4.12 Schematic representation of a step-up DC-DC converter based UC charger with a chopper structure.

By controlling the switch (M_{chp}) of the chopper structure, the output voltage of the UC discharging circuit (V_{out}) can be maintained constant. For the control mechanism, a simple hysteresis based voltage control method which is shown in Figure 4.13 could be applied.

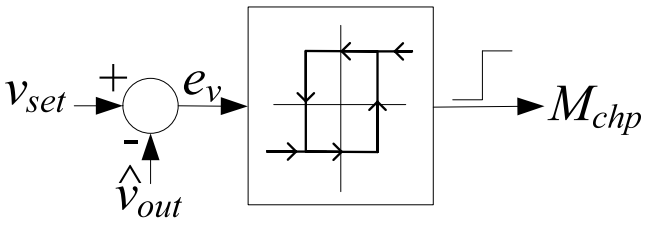


Figure 4.13 Hysteresis control structure for the chopper.

In the method shown in Figure 4.13, if the measured output voltage ($\hat{v}_{out}$) is higher than the set voltage (v_{set}), the switching signal of M_{chp} is made high in order to reduce the output voltage and the switching signal of M_{chp} is made low for the opposite condition.

4.4 Bi-Directional DC-DC Converter Structure

In Section 4.2 and Section 4.3, step-down and step-up DC-DC converter structures and control methods are investigated in order to realize the charging and discharging operations of UCs. However, in most of the UC assisted applications, a single power electronics converter structure that is capable of performing both charging and discharging operations is required to interface UCs to the whole system. For this requirement, the use of a bi-directional DC-DC converter is suggested in [45-48]. The schematic representation of a bi-directional DC-DC converter interfacing a UC to an energy storage device, that has a higher voltage rating than the rated voltage of the UC, is shown in Figure 4.14.

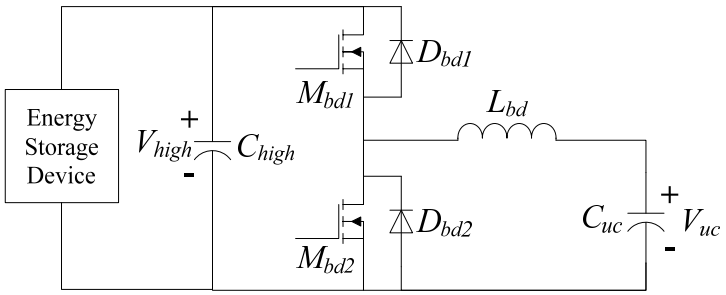


Figure 4.14 Schematic representation of a bi-directional DC-DC converter interfacing a UC to an energy storage device.

As its name implies, bi-directional DC-DC converters are capable of performing bi-directional energy transfer between a UC and an energy storage device. The energy storage device shown in Figure 4.14 represents the high voltage side. The operation principle of the bi-directional DC-DC converter is based on switching operation of the controllable switches (M_{bd1}, M_{bd2}) separately for the charging and discharging phases of the UC. In the charging phase of the UC, M_{bd1} is controlled and the gate signal of M_{bd2} is made low. The operating modes of a bi-directional DC-DC converter for the charging phase of the UC are shown in Figure 4.15.

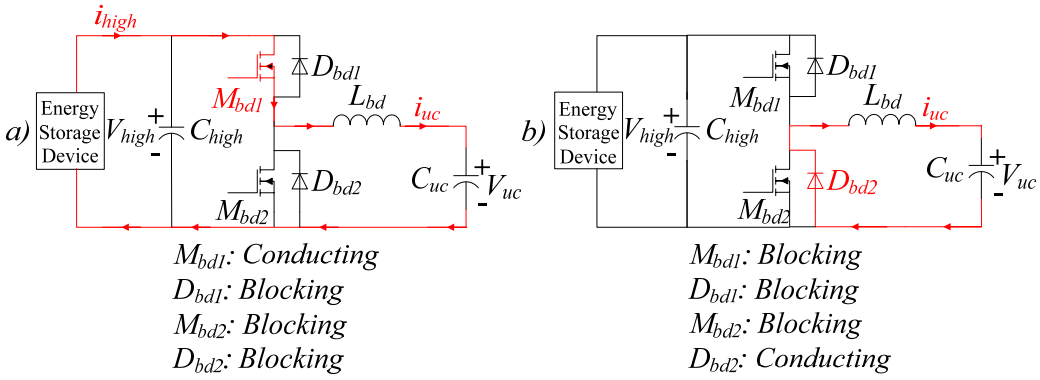


Figure 4.15 Operating modes of a bi-directional DC-DC converter for the charging phase of the UC: (a) M_{bd1} is in conduction mode, (b) M_{bd1} is in blocking mode.

As shown in Figure 4.15, the bi-directional DC-DC converter operates like a step-down DC-DC converter in the charging phase of the UC. Therefore, the operation principle of the bi-directional DC-DC converter in the charging phase of the UC is the same as the operation principle of a step-down DC-DC converter based UC charger.

In the discharging phase of the UC, M_{bd2} is controlled and the gate signal of M_{bd1} is made low. The operating modes of a bi-directional DC-DC converter for the discharging phase of the UC are shown in Figure 4.16.

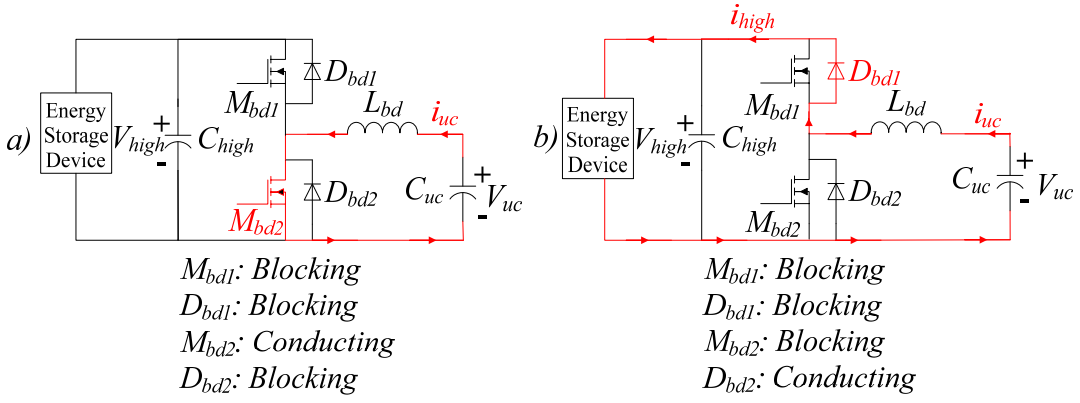


Figure 4.16 Operating modes of a bi-directional DC-DC converter for the discharging phase of the UC: (a) M_{bd2} is in conduction mode, (b) M_{bd2} is in blocking mode.

As shown in Figure 4.16, the bi-directional DC-DC converter operates like a step-up DC-DC converter in the discharging phase of the UC. Therefore, the operation principle of the bi-directional DC-DC converter in the discharging phase of the UC is the same as the operation principle of a step-up DC-DC converter based UC discharger.

4.5 Power Electronics Converter Structure for an Ultracapacitor Test System

To evaluate the performance of UCs, a test system that is capable of performing the charging and discharging operations of UCs is necessary. When the power electronics converter structures given in this chapter are considered, it is seen that two methods exist for realizing a power electronics converter based UC test system. In the first method, UCs are charged by a step-down DC-DC converter supplied by the AC utility grid followed by a step-down transformer, a diode bridge, and a large valued filter capacitor configuration. On the other hand, the energy stored in UCs is discharged to a chopper controlled resistor by means of a step-up DC-DC converter in this method. The schematic representation of the power electronics converter structure for this method is shown in Figure 4.17 which is the composition of the structures shown in Figure 4.7 and Figure 4.12.

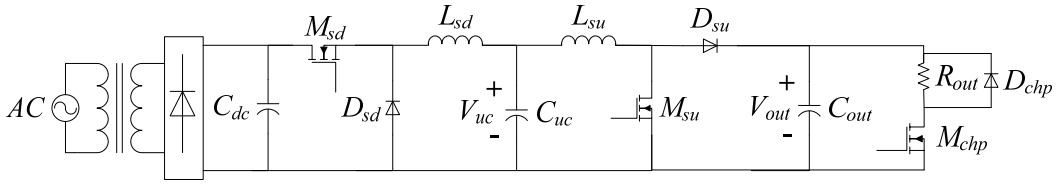


Figure 4.17 Schematic representation of the power electronics converter structure for a loss mechanism based UC test system.

In the second method, the charging and discharging operations of UCs are realized by means of a bi-directional DC-DC converter. For the high side of the bi-directional DC-DC converter, an extra energy storage device is necessary to store the energy

discharged by the UC in the discharging phase of the UC test system and to release the energy back to recharge the UC in the charging phase of the UC test system. In this method, the initial charging operation for the UC and the extra energy storage device is provided by a step-down DC-DC converter supplied by the AC utility grid followed by a step-down transformer, a diode bridge, and a large valued filter capacitor configuration as in the first case. The schematic representation of the power electronics converter structure for the second method is shown in Figure 4.18.

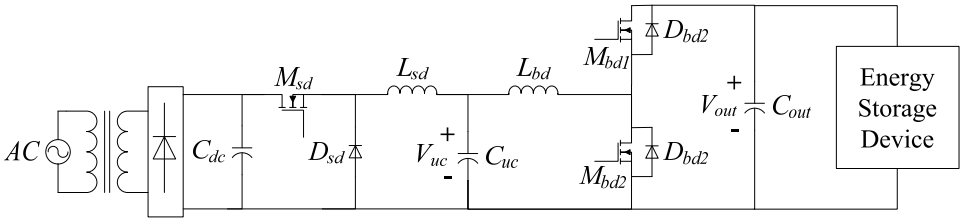


Figure 4.18 Schematic representation of the power electronics converter structure for a bi-directional energy transfer mechanism based UC test system.

Different energy storage device types could be utilized for the structure shown in Figure 4.18. The energy storage device used in this topology should have a high cycle life in order to realize the cycling tests of UCs. Therefore, batteries are not suitable for this structure. On the other hand, an extra UC module with a high voltage rating and energy storage capability could be used for the energy storage device requirement since the cycle life of UCs are very high. However, the use of a UC module for the energy storage device requirement will increase the cost of the system.

When the power electronics converter structures shown in Figure 4.17 and Figure 4.18 are compared, it is seen that the second method is more efficient than the first method. However, the cost of the second method is higher than the first method. Therefore, the structure shown in Figure 4.17 is chosen for the thesis study.

4.6 Conclusion

In this chapter, power electronics converter structures for implementing the charging and discharging operations of UCs are reviewed. It could be concluded that current mode control structures could be utilized for both charging and discharging operations. While investigating the control of charging and discharging circuits, it is seen that the control structures should be supported with complementary mechanisms in order to decouple the effects of voltage variations in the input and output of the charging and discharging circuits.

After investigating the charging and discharging structures, the properties and operating principles of a bi-directional DC-DC converter are reviewed. It is seen that, this topology is the composition of step-down and step-up DC-DC converters and by means of this topology both charging and discharging operations of UCs could be performed which is very important for most of the power electronics applications.

In the last section of this chapter, two power electronics converter structures are shown in order to realize an UC test system. The first structure is based on charging UCs from an input supply and discharging it to a resistor. On the other hand, the second structure is based on energy transfer between the UCs and an additional energy storage device. However, the requirement for an additional energy storage device increases the cost of the system. Therefore, the structure based on loss mechanism is chosen for the thesis study.

CHAPTER 5

HARDWARE DESIGN OF A MICROCONTROLLER BASED ULTRACAPACITOR TEST SYSTEM

5.1 Introduction

In Chapter 3, the UC testing issue and the necessary components of a UC test device were reviewed, whereas in Chapter 4, power electronics converter topologies were investigated in order to realize the charging and discharging operations of UCs. In this chapter, design of a microcontroller (μC) based UC test system is conducted based on the information given in the previous chapters. The information given in this chapter includes full description and operational details of the laboratory constructed UC test system. The performance of the designed UC test system is demonstrated by the help of computer simulations and experimental results.

5.2 General Structure and Components of a Microcontroller Based Ultracapacitor Test System

The implemented UC test system is composed of a charge and discharge energy management system supported by a measurement and data acquisition system which is shown in Figure 5.1. The charge and discharge energy management system is based on power electronics converters which are controlled by a mixed signal hardware structure as shown in Figure 5.1. Inside the control hardware, voltage and current variations of the UC under test and power electronics converters are

measured and conditioned to a suitable level consistent with the analog to digital (A/D) converters of the digital controller.

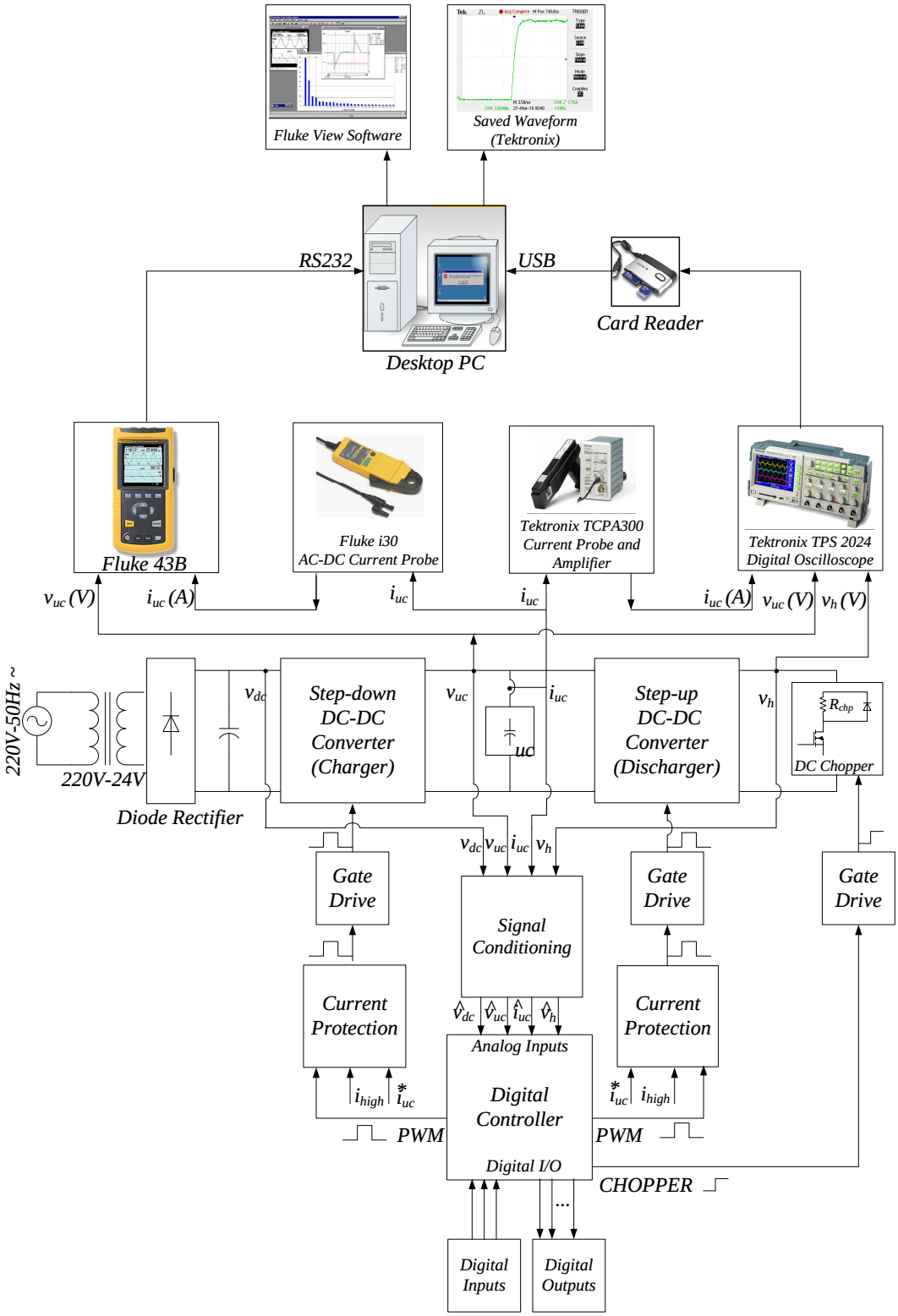


Figure 5.1 Structural diagram of a microcontroller based UC test system.

By interpreting the measured values inside the digital controller, switching signals are generated for the power electronics converters to manage the charging and discharging processes. For evaluating the performance of UCs, measurement and recording devices are used. These measurement devices are supported by a personal computer (PC) to manage the test data effectively. The operational details of the implemented test system are summarized in the following sections.

5.2.1 Charge and Discharge Energy Management System

The charge and discharge energy management system is the main component of the UC test system that applies predetermined current profiles to the UCs under test within selected voltage limits of the UC terminal voltage. It consists of power electronics converters, gate drive circuits, measurement circuits, current protection circuits, and a microcontroller based digital controller.

5.2.1.1 Power Electronics Converters

The charging and discharging phases of the UC test system is provided by the power electronics converter structure shown in Figure 5.2.

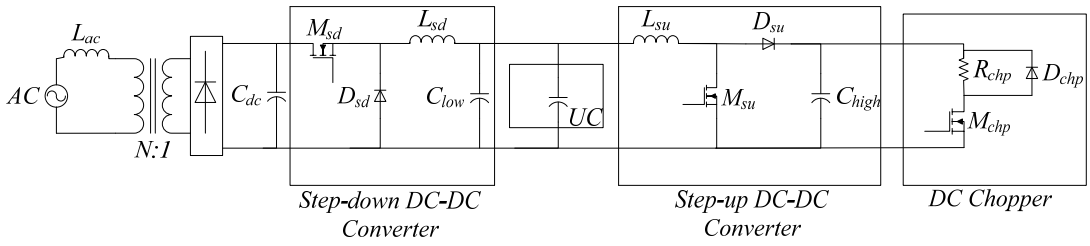


Figure 5.2 Schematic diagram of the power electronics converter structure.

As shown in Figure 5.2, the UC under test is charged from an AC utility grid, a step-down transformer, a diode bridge, and a filter capacitor configuration followed by a step-down DC-DC converter. On the other hand, the discharging process is

provided by means of utilizing a step-up DC-DC converter and a DC chopper configuration. The parameters of the power electronics converter structure are shown in Table 5.1.

Table 5.1 Parameters of the power electronics converter structure

Transformer	220V/24V, 250VA, 50Hz
Full-bridge Diode Rectifier (KBPC1000/W [49]*)*	50V DC Blocking Voltage 10A Average Rectified Output Current
C_{dc}	27.2 mF
C_{low}	2.2 mF
C_{high}	6.8 mF
L_{sd}	1 mH
L_{su}	1 mH
L_{ac}	0.5 mH
R_{chp}	3.13 Ω
f_{sw} *(for* M_{sd} *and* M_{su}*)*	50 kHz

In the design process, the power electronics converter selection is realized according to the continuous current requirement of the charging and discharging phases of the test system which was also expressed in Chapter 4. The reason for using a DC chopper at the output of the step-up DC-DC converter is to maintain the output voltage of the step-up DC-DC converter constant which simplifies the controller design of the step-up DC-DC converter. The controlled and uncontrolled switch requirements of the power electronics converters are fulfilled by utilizing MOSFETs. For the diode operation, body diodes of the MOSFETs are utilized. The reason for using a MOSFET body diode for the uncontrolled switch requirements is due to the high current handling capability of the device within a small package (TO220) which is very important for printed circuit board (PCB) layouts and preventing device compatibility problems by utilizing the same components for both controllable and uncontrollable switch requirements. The chosen component for the switches of the power electronics converters is IRF2807 from International Rectifier. Major electrical characteristics of IRF2807 are summarized in Table 5.2 [50].

Table 5.2 Major electrical characteristics of IRF2807 [50]

Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	75 V
Static Drain to Source on State Resistance	$R_{DS(ON)}$	13 mΩ
Continuous Drain Current (at V_{GS} =10V, T_c=25°C)	$I_{D(25^oC)}$	82 A
Continuous Source Current (Body Diode)	$I_{S(25^oC)}$	82 A
Body Diode Forward Voltage	V_{SD}	1.2V

5.2.1.2 Gate Drive Circuits

Toshiba TLP250 opto-couplers [51] are used for the gate drive requirements of the controllable switches of the power electronics converters (M_{sd}, M_{su}, *and* M_{chp}). Isolated ground requirement of the high side switch M_{sd} is fulfilled by using an isolated power supply for the bias input of the corresponding opto-coupler. The schematic diagram of the gate drive structure is shown in Figure 5.3.

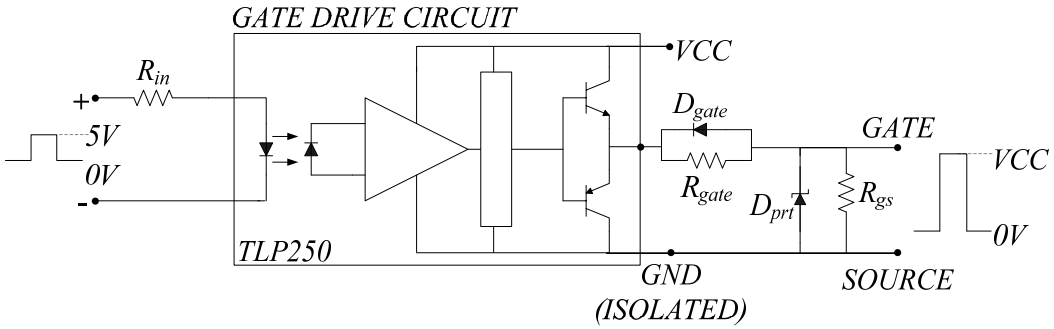


Figure 5.3 Schematic diagram of the gate drive circuit.

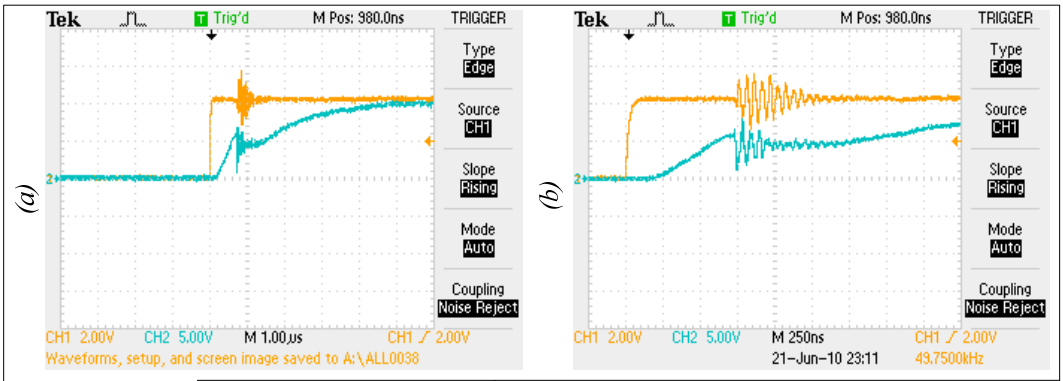
The parameters of the gate drive circuits are shown in Table 5.3. As shown in Figure 5.3, the switching signals generated by the digital controller are applied to the input of the opto-couplers via the input resistors (R_{in}). The levels of the applied signals are increased to VCC (12V) level by means of the opto-couplers. The level increased switching signals are applied to the gate of the MOSFETs via the gate resistors (R_{gate}). The anti-parallel diodes (D_{gate}) discharge the gates of the MOSFETs when the switching signals are made low. The function of the protection diodes (D_{prt}) is to protect the gate of the MOSFETs for overvoltage conditions and the parallel gate to source resistors (R_{gs}) are utilized to stabilize the switching waveforms.

Table 5.3 Parameters of the gate drive circuits

R_{in}	100 Ω
R_{gate}	200 Ω (for M_{sd}) 56 Ω (for M_{su}) 56 Ω (for M_{chp})
D_{gate} *(High Speed Diode)*	1N4148
D_{prt} *(Zener Diode)*	1N4109 (15V)
R_{gs}	10 kΩ

The selection of gate resistance (R_{gate}) values is very important for the gate drive circuit structure shown in Figure 5.3. If gate resistance values are lowered, the MOSFETs show fast turn on behaviour. This fast turn on behaviour increase the magnitude of oscillations in the Miller plateau level which will cause undesired switching noise in the DC-DC converter output. It is needed to increase the gate resistance values in order to slow down the turn on behaviour of MOSFETs which will also reduce the switching noise. On the other hand, higher gate resistance values result in increased switching loss since the switching loss of a MOSFET is related with the turn on time. Therefore, it could be concluded that there is a trade-off between the generated switching noise and switching loss of the MOSFETs when the selection of gate resistance issue is considered.

Gate resistance values are selected by utilizing an experimental approach. Gate resistance values are increased until the switching waveform oscillations are lowered to a suitable level. The temperature of the corresponding MOSFETs is also measured. For the high side MOSFET (M_{sd}), a gate resistance value of 200 Ω gives sufficient performance, whereas a gate resistance value of 56 Ω gives sufficient performance for the low side MOSFETs (M_{su}, M_{chp}). During the experiments it is observed that the switching noise generated by the high side MOSFET is higher than the low side MOSFETs when the voltage on the UC is investigated. Turn on characteristics of the high side MOSFET for a gate resistance value of 200 Ω is shown in Figure 5.4.



	Orange Waveform	*Blue Waveform*
Vertical Axis :	*Applied Signal: 2 V/div*	*High Side MOSFET Gate to Source Voltage: 5V/div*
Horizontal Axis :	*time: (a) 250 ns/div, (b) 1µs/div*	

Figure 5.4 High side MOSFET turn on characteristics for a gate resistance value of 200 Ω: (a) turn on characteristics obtained for a time scale of 1 µs/div, (b) turn on characteristics obtained for a time scale of 250ns/div.

As shown in Figure 5.4, there exists an oscillating behavior in the Miller plateau level. When the gate resistance of the high side MOSFET is lowered the magnitude of the oscillations in the Miller plateau level grows up and the increased oscillations cause switching noise in the step-down DC-DC converter output. The switching noise is experienced as immediate voltage spikes in the step-down DC-DC converter output voltage waveform. It is observed that the magnitude and frequency of the immediate voltage spikes is decreased as the gate resistance is lowered and a gate resistance of 200 Ω gives sufficient performance for the step-down DC-DC converter.

For the step-up DC-DC converter and DC chopper configuration, a gate resistance value of 56 Ω gives sufficient performance and no immediate voltage spikes are experienced during the operation of this configuration. Therefore, it could be concluded that the gate drive circuit design for ground referenced MOSFETs is simpler than designing the high side MOSFET gate drive circuits.

5.2.1.3 Current and Voltage Measurement Circuits

Current measurements are performed by utilizing LTS25-NP Hall Effect current transducers manufactured by LEM. The major advantages of LTS25-NP current transducers are excellent accuracy and linearity, unipolar power supply requirement, insulated plastic case, PCB compatible structure, and its 0-5V output signal range which is compatible with the A/D of microcontrollers. Schematic diagram of the current measurement circuit is shown in Figure 5.5 [52].

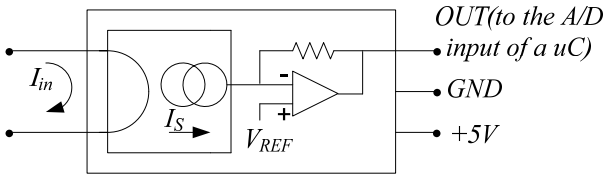


Figure 5.5 Schematic diagram of the current measurement circuit [52].

The nominal input current rating of LTS25-NP is ±25A and by using this current transducer, current levels up to ±75A could be measured. However, the current rating of the implemented UC test system is 15A. Therefore, number of primary turns of the transducer is made three in order to increase the output voltage of the transducer which also improves the measurement accuracy. With the increased number of turns configuration, the input to output relationship of the current measurement circuit is given in (5.1).

$$V_{out} = 2.5 + I_{in} \times 0.075 \tag{5.1}$$

Voltage measurements are performed by a simple structure composed of resistive dividers followed by operational amplifier (TLC272 [53]) based buffer circuits. Schematic diagram of the voltage measurement circuit is shown in Figure 5.6.

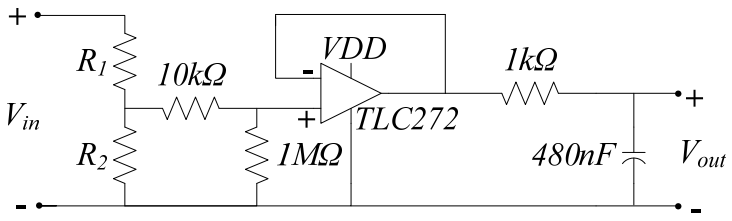


Figure 5.6 Schematic diagram of the voltage measurement circuit.

Input to output relationship of the voltage measurement circuit is given in (5.2).

$$\frac{V_{out}}{V_{in}} = \frac{R_2}{R_1 + R_2} \tag{5.2}$$

5.2.1.4 Current Protection Circuits

One of the important properties of the implemented UC test system is safety and the most obvious parameter for providing the safety is the current measurement signals (V_{LEM}) provided by the current transducers. In the implemented system, current measurements are utilized to block the switching signals of the power electronics converters when they are above the maximum limit determined by a reference signal (V_{ref}). Schematic diagram of the current protection circuit is shown in Figure 5.7.

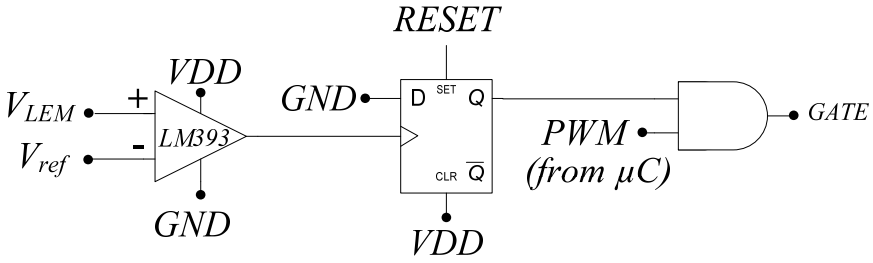


Figure 5.7 Schematic diagram of the current protection circuit.

As shown in Figure 5.7, V_{LEM} is compared with V_{ref} with an analog comparator (LM393 [54]). The output of the comparator is fed to a D type flip-flop and the output of the D type flip flop is put into a logical AND operation with the gate drive

signals that controls the MOSFETs of the power electronics converters. When V_{LEM} is above V_{ref}, corresponding gate drive signal is latched to a digital zero value which disables the corresponding MOSFET and thus provides over current protection.

5.2.1.5 Control Hardware Structure

Control of the implemented UC test system is maintained by means of utilizing two microcontrollers (μC) in master and slave configuration. The chosen microcontroller type for the test system is PIC18F452 from Microchip Technology Inc [55]. Major properties of PIC18F452 from the UC test system perspective is summarized in Table 5.4. Microcontrollers of the test system are used with a 10 MHz high speed oscillator in 4 x Phase Locked Loop (PLL) mode. Therefore, 40 MHz operating frequency is obtained. Since an instruction cycle consists of four oscillator cycles in this microcontroller type, 100ns instruction cycle is obtained with this configuration [55]. Input-output (I/O) diagram of the microcontroller based digital controller structure is shown in Figure 5.8.

Table 5.4 Major properties of PIC18F452 [55]

Word Length	8 Bits
Operating Clock Frequency	Up to 40 MHz operation with 4x PLL
Hardware Multiplier	8 bits x 8 bits
A/D module	8 A/D Channels
	10 Bits A/D Results
	Linearity ≤ 1 Least Significant Bit (LSB)
PWM module	2 PWM outputs
	Accuracy: 8 bits (156 kHz range)
	Accuracy: 10 bits (39 kHz range)

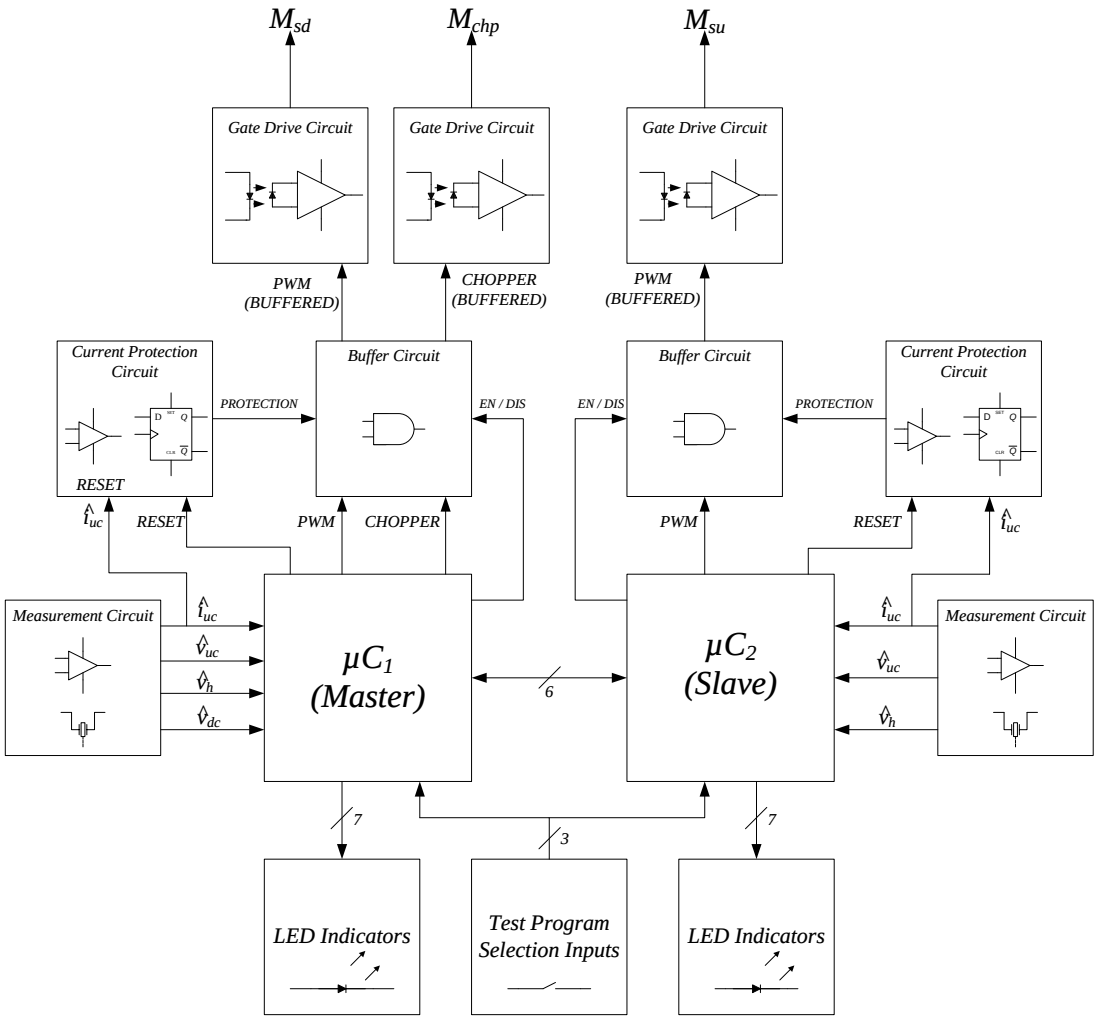


Figure 5.8 I/O diagram of microcontroller based digital controller.

As shown in Figure 5.8, the harmony between the two microcontrollers is provided by means of a six bit communication channel and these microcontrollers generate switching signals (*PWM, CHOPPER*) for the controllable switches of the power electronics converters (M_{sd}, M_{su}, M_{chp}) according to the current and voltage measurements. Selection of the test program parameters such as current profile (i_{ref}) and number of cycles of the charging and discharging procedure (N) is provided by utilizing a peripheral unit which consists of three micro switches. Reading three bit digital information generated by the micro switch configuration allows selecting eight different test programs. The other peripheral unit of the digital controller is the output unit configured by light emitting diodes (LED). The controller generates outputs and illuminates the LED indicators according to the process information.

Another important function of the controller structure is to reset the current protection circuits which operate independent from the microcontrollers. At the beginning of the control process, the latches of the current protection circuits should be initialized by means of sending an active low digital signal. The last point about the controller structure is the availability of enabling and disabling signals for gate drive circuits. When a fault condition such as an over current measurement is detected by the microcontrollers, gate drive outputs of the controller structure are disabled by the help of disabling signals.

The microcontrollers are programmed via C programming language. The code efficiency of the software structure is sufficient for the application by the help of C compiler optimized architecture of PIC18F452 microcontrollers [55]. Inside the microcontrollers, all the calculations are realized by utilizing unsigned 16 bit integers and division operation is not used in order to reduce the calculation time. Instead of division operation, right shift (>>) bitwise operation is utilized. Inside the microcontrollers built in A/D clock is set to the slowest value in order to increase the signal to noise ratio (SNR) of the measurements. This configuration increases the update time of the control loops inside the microcontrollers. On the other hand, if A/D speed is increased, SNR of the measurements decreases. Therefore, it could be concluded that there is a trade-off between the chosen A/D speed and SNR of the measurements. With the chosen A/D clock rate and calculation types, 200 μs control loop update capability is obtained.

The control process of the charge and discharge energy management system is shared between the two microcontrollers. The first microcontroller also mentioned as the master controller manages the step-down DC-DC converter in charging process, whereas the second controller mentioned as the slave controller manages the step-up DC-DC converter in discharging process. The chopping action to provide a constant voltage at the output of the step-up DC-DC converter is also controlled by the master controller in discharging process in parallel with the step-up DC-DC converter control provided by the slave controller. Inside the microcontrollers, an automated

algorithm is realized to synchronize the master and slave operation. Flowchart of the program flow inside the microcontrollers is shown in Appendix E.

5.2.2 Measurement and Data Acquisition System

As shown in Figure 5.1, a Fluke 43B power quality analyzer and a Tektronix TPS2024 digital storage oscilloscope are utilized in order to measure and record the terminal behaviour of the UC under test according to the applied current profiles. Both measurement devices are supported with a PC.

With the implemented test system, long term data for the UC terminal voltage and applied current is obtained by means of Fluke 43B power quality analyzer and Fluke i30 AC/DC current probe configuration. The recorded data of Fluke 43B is the terminal voltage of the UC under test and the RMS value of the applied current. The recorded data can be sent to the PC with a built-in RS232 interface via Fluke View Software. By means of the data obtained from Fluke 43B power quality analyzer, constant current and constant power characteristics of the UC under test could be observed.

To measure the dynamic performance of the test system and see the instantaneous variation of the UC terminal voltage, a Tektronix TPS2024 digital storage oscilloscope is used with the Tektronix TCPA300 AC/DC current measurement system. By means of the oscilloscope and probe pair, waveforms that describe the dynamic and steady-state performance of the UC test system could be obtained and ESR measurements of UCs could be performed. Test waveforms obtained as oscilloscope output are stored in a memory card and the data stored inside the memory card could be viewed with the PC by means of a USB interface.

5.3 Ultracapacitor Charging System

Circuit topology and basic control structure of a UC charging system composed of a step-down DC-DC converter was described in Chapter 4. In this section, implementation details of a UC charging system is expressed in terms of microcontroller hardware considerations. Performance of the proposed control structure is demonstrated by the help of computer simulations and experimental results.

5.3.1 Microcontroller Based Ultracapacitor Charging System

Current programmed control is utilized for the control of the UC charging system in order to apply a predetermined charging current profile to a UC under test. In Chapter 4, a first order model of a UC charging system was derived and the basic control structure for this system was presented. In this section, a proportional integral (PI) type current regulator is integrated to the charging control structure shown in Figure 4.6 with a microcontroller based design perspective.

State variables of a microcontroller based UC charging system are UC current (i_{uc}), UC terminal voltage (v_{uc}), and DC bus voltage (v_{dc}) measurements, whereas the output generated by the system is the PWM signal which will be applied to the controlled switch (M_{sd}) of the step-down DC-DC converter. Block diagram of the charging structure is shown in Figure 5.9 and operational details of the UC charging system are summarized in Table 5.5.

Table 5.5 Operational details of the microcontroller based UC charging system

PWM Frequency		50 kHz
Full Value (Count) of the Duty Cycle (Corresponds to d=1.0)		200
Current Loop Update Period		200 μs
Analog Readings	*Current Measurement*	10 bits
	UC Voltage Measurement	8 bits
	DC Bus Voltage Measurement	8 bits

Inside the controller structure, digital equivalents of the measurement signals are utilized. However, measurements read by the microcontroller are not with the same scaling and offset factors. Therefore, input to output function of each measurement process is considered separately as summarized in Table 5.6.

Table 5.6 Input to output functions of measurement processes

Current Measurement	$i_{uc}[n] = \frac{2.5 + i_{uc}(t) \times 0.075}{5} \times 2^{10}$
UC Terminal Voltage Measurement	$v_{uc}[n] = \frac{0.311 \times v_{uc}(t)}{5} \times 2^{8}$
DC Bus Voltage Measurement	$v_{dc}[n] = \frac{0.1 \times v_{dc}(t)}{5} \times 2^{8}$

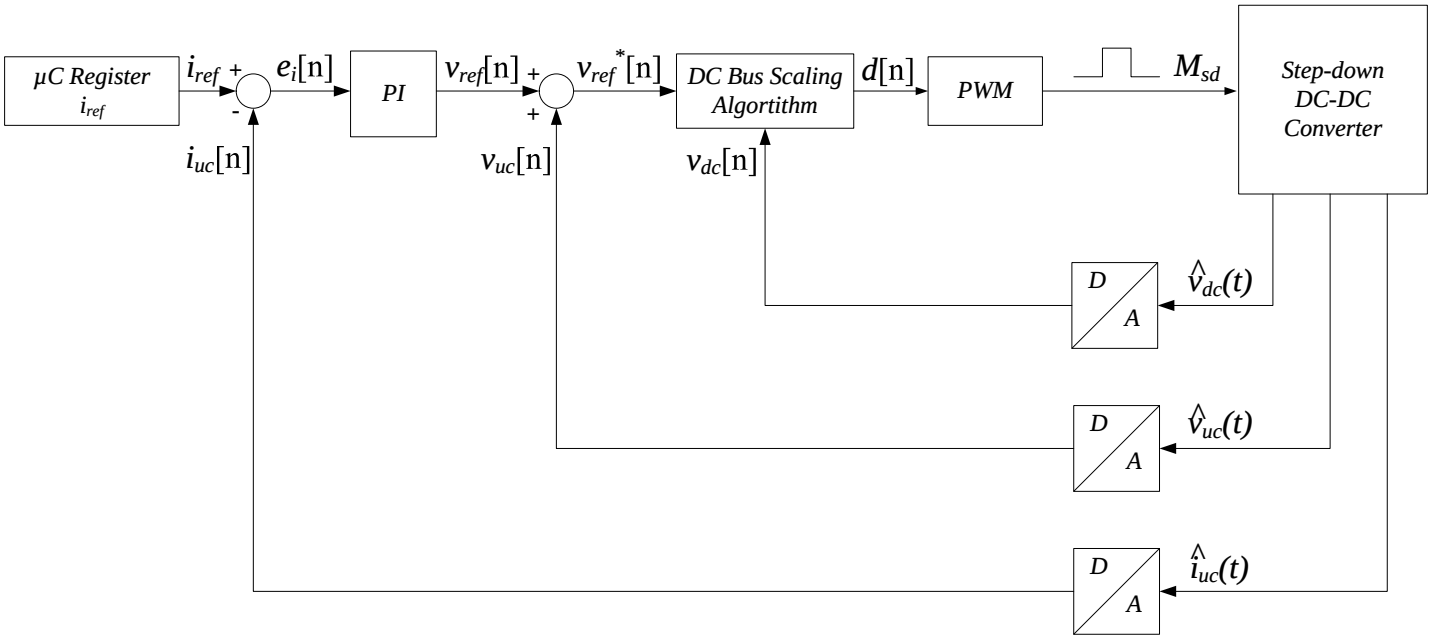


Figure 5.9 Block diagram of the microcontroller based UC charging system.

As shown in Figure 5.9, the first operation of the control process is the calculation of the current error (e_i[n]) between the current reference (i_{ref}) and the digital value of the measured UC current (i_{uc}[n]). After the current error calculation, e_i[n] is fed to a PI calculation block which generates a voltage reference value (v_{ref}[n]). Following the PI calculation, v_{ref}[n] value is added with the digital value of the measured UC voltage (v_{uc}[n]) in order to obtain the voltage reference value of the first order decoupled system (v_{ref}^* [n]). After v_{ref}^* [n] calculation, the last step to obtain the digital value of the duty cycle (d[n]) is the application of a DC bus scaling algorithm.

The purpose of the DC bus scaling algorithm is to prevent the effect of DC bus voltage variation on the control system performance. DC bus scaling algorithm is based on selecting a voltage reference value (v_{dc_ref}) for the digital values of the DC bus voltage measurements and calculating a reference duty cycle (d_{ref} [n]) value accordingly. However, as given in Table 5.6, the scaling factors of UC terminal voltage and DC bus voltage measurements are different and v_{ref}^* [n] is calculated according to the scaling factor of the UC terminal voltage measurement. Therefore, v_{dc_ref} value should be multiplied with 3.11 when it is put into a calculation with v_{ref}^* [n] according to the input to output functions shown in Table 5.6. Calculation of d_{ref}[n] is based on proportioning the voltage reference value of the first order decoupled system (v_{ref}^* [n]) and the scaled version of the DC bus voltage reference value (*3.11* x v_{dc_ref}) and then, multiplying the ratio with the full digital duty cycle (d_{full}) value which is 200 for this application. Calculation of d_{ref} [n] is given in (5.3).

$$d_{ref}[n] = \frac{v_{ref}^*[n]}{v_{dc\_ref} \times 3.11} \times d_{full} = \frac{v_{ref}^*[n]}{128 \times 3.11} \times 200 \approx \frac{v_{ref}^*}{2} \qquad (5.3)$$

As given in (5.3), d_{ref} [n] value could be obtained by means of dividing v_{ref}^* [n] value by 2. However, division operation takes too much time in a PIC18F452 microcontroller since it does not have a hardware divider. It could be concluded that division operation is not suitable for this application. On the other hand, bitwise operations take less time than the division operations inside PIC18F452 microcontrollers. Therefore, instead of the division operation, v_{ref}^* [n] value could be

1 bit right shifted (*>>1 bit*), since 1 bit right shift operation has the same effect with dividing by 2 operation. The calculation of d_{ref} [n] with right shift bitwise operator is given in (5.4).

$$d_{ref}[n] = v_{ref}^{*}[n] >> (1\ \ bit) \tag{5.4}$$

After calculating d_{ref} [n], the digital value for the difference ($diff_{DC\_bus}$[n]) between v_{dc_ref} and the actual DC bus voltage (v_{dc}[n]) can be calculated as given in (5.5). In this calculation, the digital value for v_{dc_ref} is chosen as 128 which corresponds to 25V.

$$diff_{DC\_bus}[n] = \begin{cases} v_{dc}[n] - 128\ , & v_{dc}[n] > 128 \\ 128 - v_{dc}[n]\ , & v_{dc}[n] < 128 \end{cases} \tag{5.5}$$

After the calculation of $diff_{DC\_bus}$[n], the scaling parameter (sp[n]) of the DC bus scaling algorithm is calculated as given in (5.6).

$$sp[n] = \frac{d_{ref}[n] \times diff_{DC\_bus}[n]}{v_{dc\_ref}} \tag{5.6}$$

Since v_{dc_ref} is chosen as 128, instead of division operation, 7 bit right shift operation could be utilized for the calculation of sp[n] in order to reduce the control loop update time as given in (5.7).

$$sp[n] = (d_{ref}[n] \times diff_{DC\_bus}[n]) >> (7\ \ bits) \tag{5.7}$$

The actual value of the duty cycle (d[n]) is calculated according to the sp[n] value as given in (5.8). For the calculation of d[n], sp[n] value is subtracted from d_{ref} [n], if v_{dc}[n] is higher than the reference, whereas sp[n] value is added to d_{ref} [n], if v_{dc}[n] is lower than the reference.

$$d[n]=\begin{cases} d_{ref}[n]-sp[n]\ , & v_{dc}[n]>128 \\ d_{ref}[n]+sp[n]\ , & v_{dc}[n]<128 \end{cases} \tag{5.8}$$

Program flow of the DC bus scaling algorithm is shown in Figure 5.10. The input of this algorithm is the voltage reference value of the first order decoupled system (v_{ref}^{*} [n]), whereas the output generated by the algorithm is the digital duty cycle value of the UC charging system (d[n]).

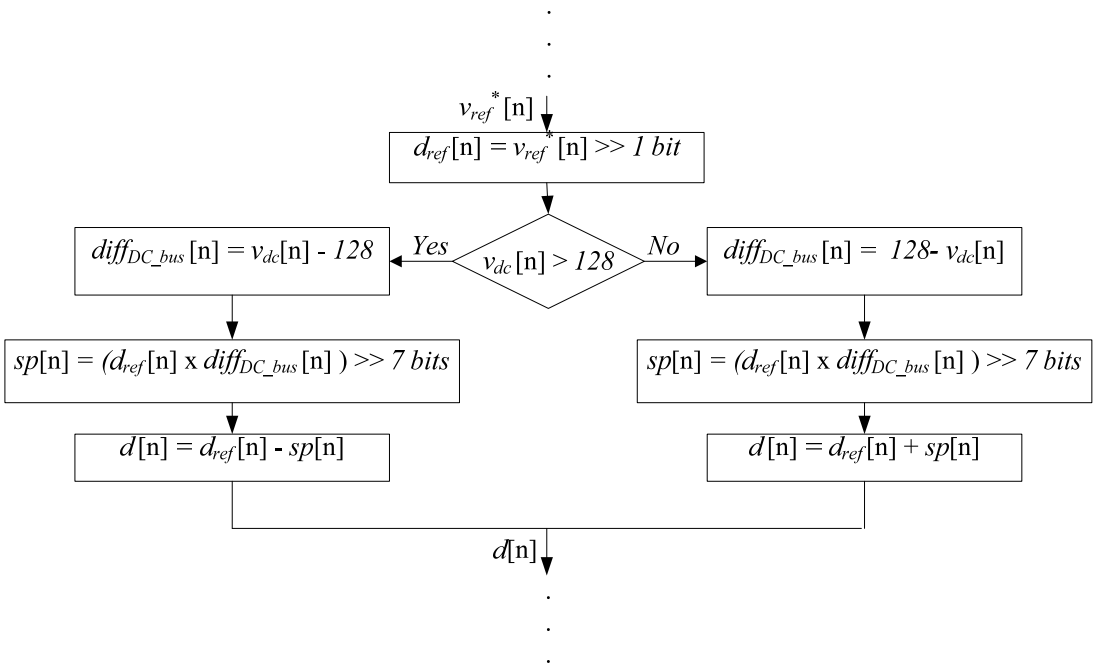


Figure 5.10 Program flow of the DC bus scaling algorithm.

As the final step of the charging system control process, duty cycle parameter of the microcontroller PWM module is updated according to calculation of d[n] and the generated PWM signal is used to control the switching operation of M_{sd}.

When the microcontroller implementation of the charging system control process is investigated, it is needed to consider the selection of reference parameters, the calculation types, the calculation limits, the control loop update time, and the stopping condition for the charging process. In this sense, the first consideration should be given to the selection of current reference parameter (i_{ref}). In the control

system of the charging process, an analog voltage is obtained as an output of the Hall Effect current transducer and this voltage is converted to a 10 bit digital value as given in Table 5.6. Since, the maximum current rating of the implemented UC test system is determined as 15A, the digital equivalent of the maximum current can be calculated as given in (5.9).

$$i_{ref\_\max} = \frac{2.5 + i_{uc}(t) \times 0.075}{5} \times 2^{10} = \frac{2.5 + 15 \times 0.075}{5} \times 1024 = 742 \tag{5.9}$$

The digital equivalent of the minimum current (0 A) can be calculated with a similar approach as given in (5.10).

$$i_{ref\_\min} = \frac{2.5 + i_{uc}(t) \times 0.075}{5} \times 2^{10} = \frac{2.5 + 0 \times 0.075}{5} \times 1024 = 512 \tag{5.10}$$

As given in (5.9) and (5.10), the digital equivalent of the UC charging current varies between 512 and 742. Therefore, i_{ref} values should be chosen according to this range. The reference values for the terminal voltage of UC and DC bus voltage should be considered with a similar approach.

The second consideration is about the calculation types. In the implemented UC test system, unsigned 16 bit integers are utilized inside the microcontrollers. Since the variables are unsigned integers, it is needed to consider the magnitude of the variables while conducting subtraction operations. The calculation of current error (e_i[n]) between the current reference (i_{ref}) and the measured UC current (i_{uc}[n]) could be given as an example to mention the importance of this consideration as given in (5.11).

$$e_i[n] = \begin{cases} i_{ref}[n] - i_{uc}[n] \ , & i_{ref}[n] > i_{uc}[n] \\ i_{uc}[n] - i_{ref}[n] \ , & i_{ref}[n] < i_{uc}[n] \end{cases} \tag{5.11}$$

According to (5.11), it is seen that the subtraction operation is conducted according to the magnitude of the current variables. If a higher magnitude current variable is subtracted from the lower magnitude current variable, overflow condition will occur which will generate wrong results for the current error calculations. Therefore, it is needed to consider the magnitude of the variables when conducting subtraction operations inside the control loop.

The third consideration is about the calculation limits. Inside the control loop, the integral and duty cycle calculations are limited. The reason for limiting the integral operation is due to prevent the wind up mechanism of the integrator. On the other hand, duty cycle limit is applied in order to prevent the occurrence of duty cycle values that is higher than the full duty cycle value.

Control loop update time is the other important parameter of the charging control structure. Inside the microcontroller every operation takes time. On the other hand, the total time required for the calculations inside the microcontroller should be less than the control loop update time for proper operation of the control process. If this condition is not satisfied, the correct values for the control process could not be obtained. In the implemented UC test system, duty cycle value of the step-down DC-DC converter is updated at 200 μs sampling intervals by utilizing a timer based interrupt service subroutine.

The last consideration of the charging control structure is given to the stopping condition. The UC charging system should be stopped when the terminal voltage of the UC reaches a certain level in order to prevent overvoltage conditions. Therefore, at every sampling interval the measured UC terminal voltage (v_{uc}[n]) is compared with a high limit (v_{up}) and the charging process is stopped if v_{uc}[n] reaches v_{up} level.

Program flow of the charging system operation is shown in Figure 5.11 according to the microcontroller implementation considerations mentioned in this section.

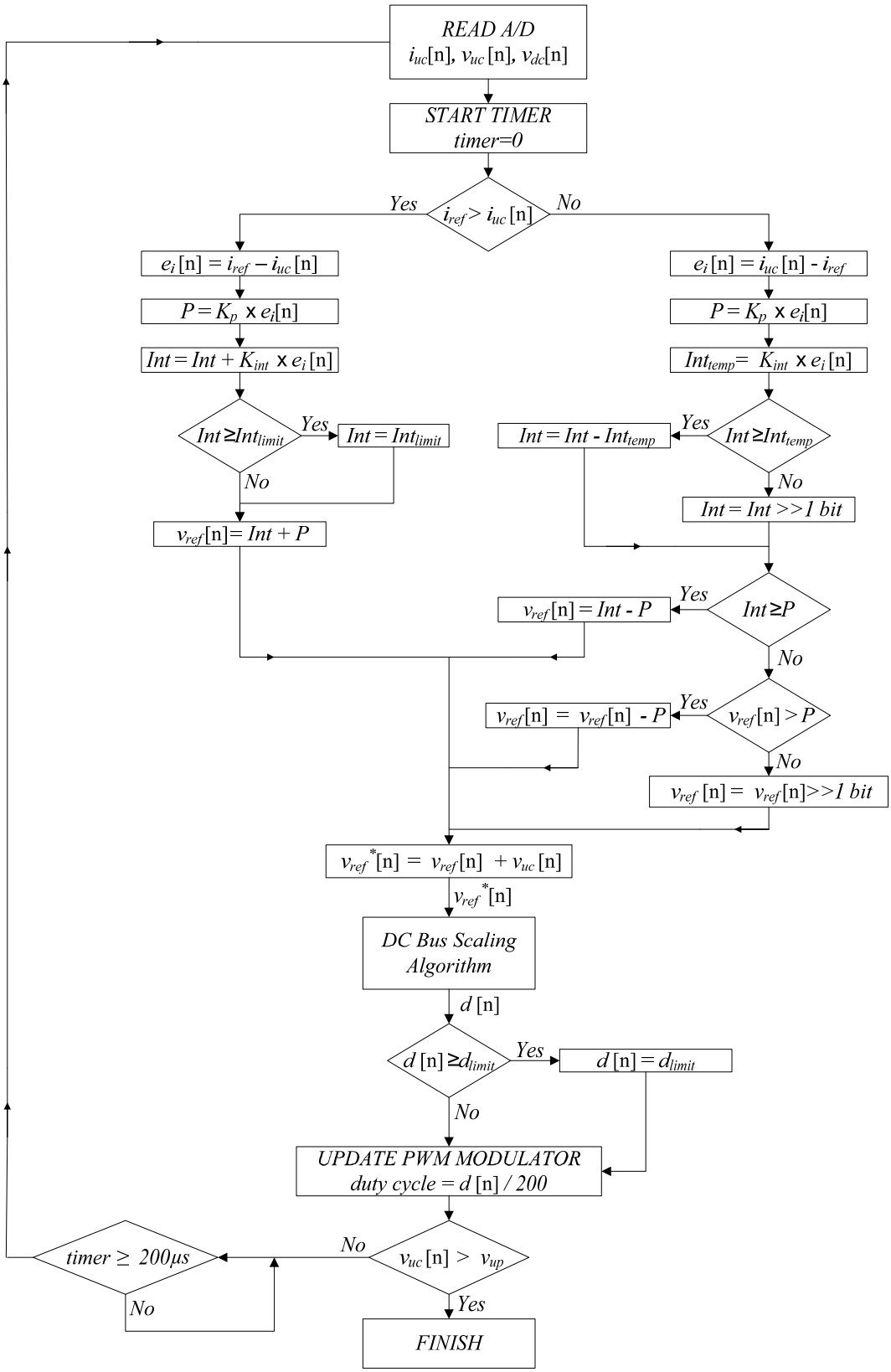


Figure 5.11 Program flow of the UC charging process.

5.3.2 Simulation Performance of Ultracapacitor Charging System

To evaluate the performance of the control structure shown in Figure 5.9, a simulation model is constructed utilizing Ansoft Simplorer 6.0 software by considering the parameters shown in Table 5.1. Input to output functions of the measurement processes, duty cycle update rate, and program flow structure of the implemented charging system are also taken into consideration while building the simulation model which is shown in Figure 5.12. The UC inside the simulation system is modeled as a simple RC branch composed of an ideal capacitance (C_{uc}) of 300F and an ESR component (R_s) of 2.5 mΩ.

The selection of PI parameters (K_p and K_i) is realized with an experimental approach. At first both of the parameters are made zero and K_p is increased in small increments until 80 % of the current command is seen in the steady-state charging current waveform. When the steady-state charging current reaches 80 % of the current command, corresponding K_p is selected as the proportional parameter. After determination of K_p, K_i is started to be increased in small increments until 100 % of the current command is seen in the steady-state charging current waveform. Control loop parameters of the simulation system are shown in Table 5.7.

Table 5.7 Control loop parameters for the simulation model of UC charging system

Sampling Time	*Current Controller (PI)*	200 µs
PI Parameters	K_p *(Proportional)*	0.8
	K_i *(Integral)*	0.5
Controller Limits	I_{limit} *(Integral)*	60
	d_{limit} *(Duty Cycle)*	180
	d_{full} *(Duty Cycle)*	200
Initial Conditions	$I_L(0)$	0A
	$V_{uc}(0)$	6V
Simulation Parameters	*Simulation Step (max)*	2us
	Simulation Step (min)	200ns

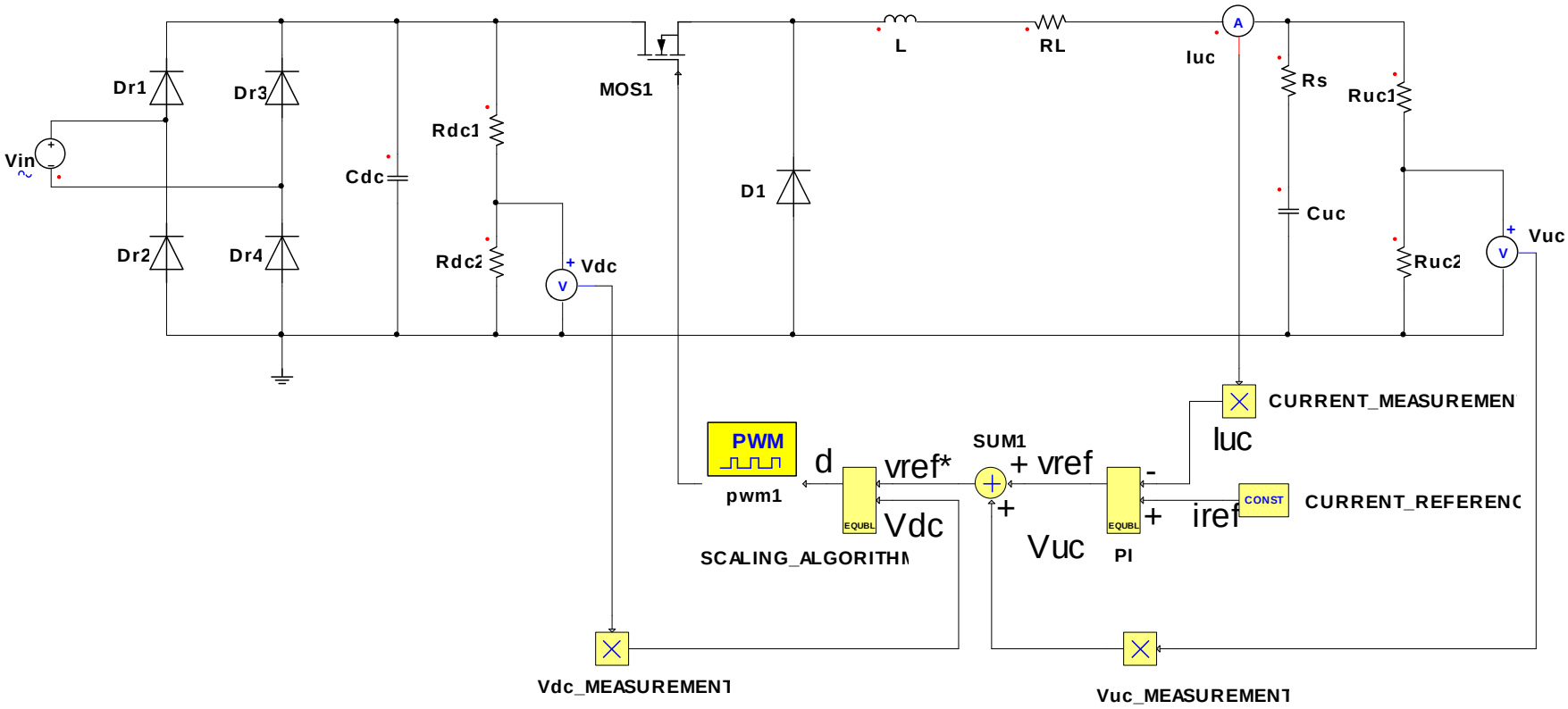


Figure 5.12 Simulation model of UC charging system.

Simulation results for the dynamic response and steady-state ripple characteristics of the UC charging current for a 15A current command are shown in Figure 5.13 and Figure 5.14, respectively.

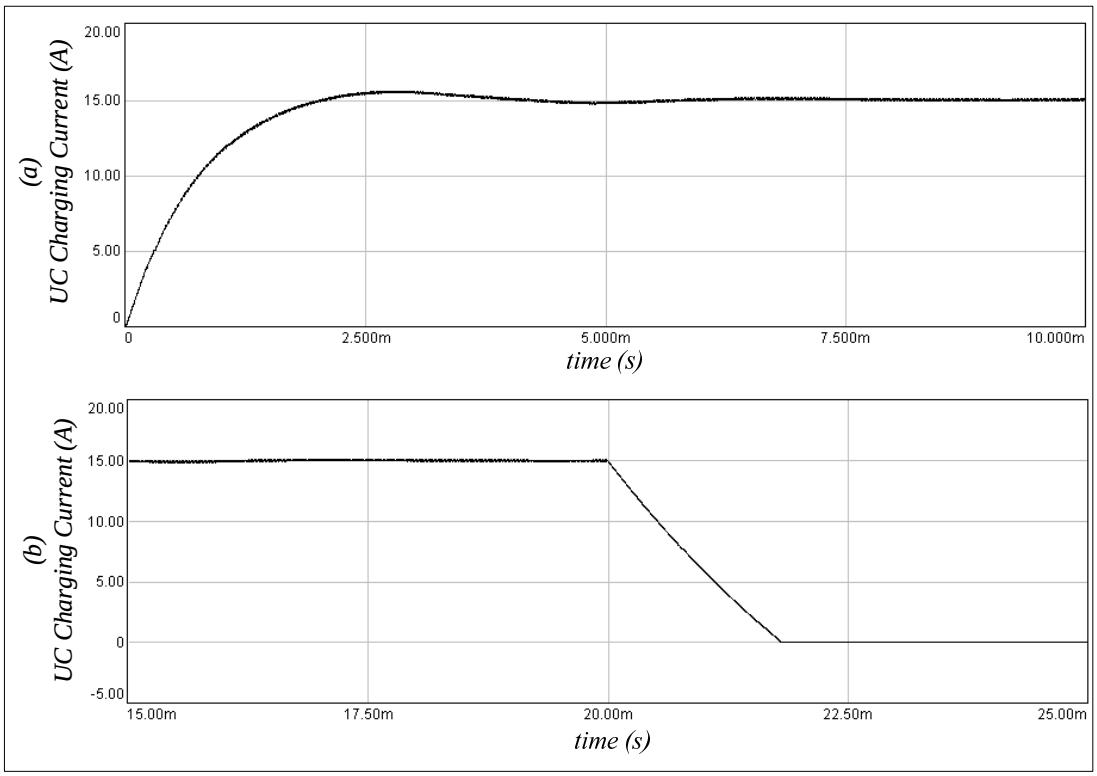


Figure 5.13 Simulation results for the dynamic response of the UC charging current for a 15A current command: (a) UC charging current build-up, (b) UC charging current fall.

As shown in Figure 5.13, the UC charging current shows a slow build-up and fall behaviour. The rise time (t_{rise}) and the fall time (t_{fall}) of the UC charging current for a 15A current command are observed as 2.0 ms and 1.81 ms, respectively. This is an expected result, since the parameters of the passive components (L_{sd}, C_{uc}) of the charging system are very high. This observation also shows that the bandwidth of the UC charging system is also at low levels and the chosen 200µs sampling rate is sufficient for the UC charging application. When the current overshoot characteristic shown in Figure 5.13 (a) is investigated, it is seen that the simulation performance of the charging system is sufficient since the current overshoot is observed as 4.26 %.

According to this observation, it could be concluded that the controller type and parameters suit the UC charging application in terms of dynamic considerations.

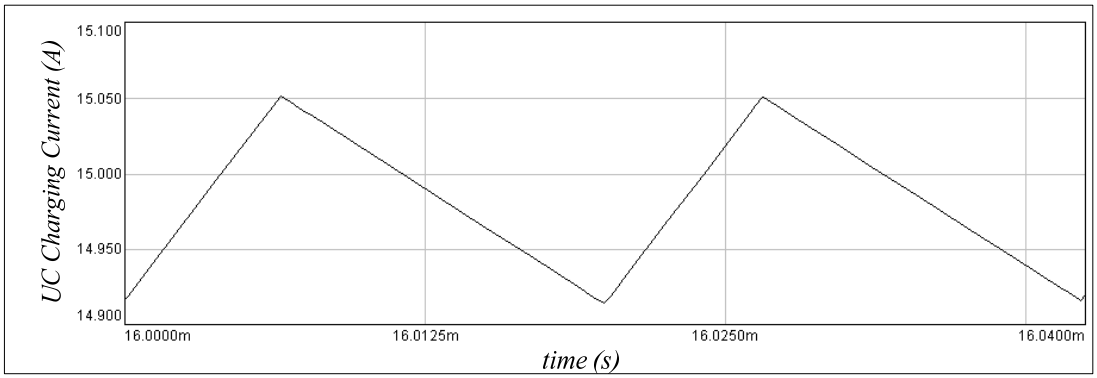


Figure 5.14 Simulation results for the steady-state ripple characteristics of the UC charging current for a 15A current command.

According to the simulation results shown in Figure 5.14, the steady-state UC charging current ripple is observed as 0.125A. The observed current ripple value can be accepted for the operation of the UC charging system, since a 0.125A valued current ripple is not capable of making a measurable difference on the terminal voltage of an UC.

5.3.3 Experimental Performance of Ultracapacitor Charging System

Control loop parameters shown in Table 5.8 are programmed inside the microcontroller of the UC charging system in order to see the actual system performance.

Table 5.8 Control loop parameters of the microcontroller based UC charging system

Sampling Time	*Current Controller (PI)*	200 µs
PI Parameters	K_p *(Proportional)*	0.75
	K_i *(Integral)*	0.5
Controller Limits	I_{limit} *(Integral)*	60
	d_{limit} *(Duty Cycle)*	180 (duty cycle = 0.9)
	d_{full} *(Duty Cycle)*	200 (duty cycle = 1.0)

In the thesis study, a UC module composed of five serially connected UC cells from Maxwell Technologies is utilized. Nameplate data and basic electrical parameters of the UC cells used in this study are shown in Table 5.9 [3].

Table 5.9 Basic parameters and nameplate data of the UC cells [3]

Manufacturer	Maxwell Technologies
Part Number	BCAP 1500 P270 T04
Rated Voltage	2.7V
Capacitance	1500F
ESR (DC)	0.47 mΩ
ESR (1 kHz)	0.35 mΩ
Leakage Current	3 mA
Volume	0.325 liters
Mass	0.32 kg

Boostcap (BCAP) series UCs from Maxwell Technologies are shown in Figure 5.15.

Figure 5.15 Boostcap series UCs from Maxwell Technologies [3].

The constructed UC module is utilized with passive resistor balancing structure. The electrical equivalent circuit of the UC module is shown in Figure 5.16 and the parameters of the UC module are shown in Table 5.10.

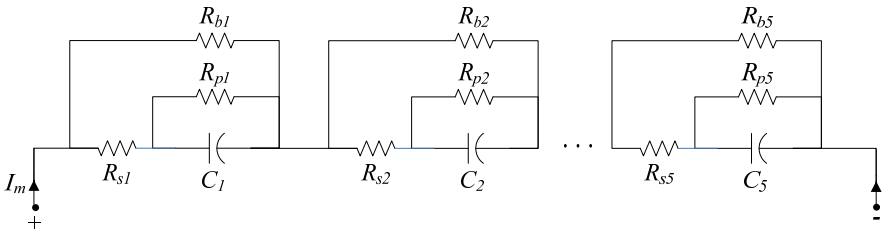


Figure 5.16 Schematic representation of the UC module utilized in the study.

Table 5.10 Parameters of the constructed UC module

	UC Module
Voltage Rating	13.5 V
Capacitance	300 F
ESR (DC)	2.35 mΩ
ESR (1 kHz)	1.75 mΩ
EPR (individual: R_{pi} , i=1,2,…,5)	900 Ω
Balancing Resistor (individual: R_{bi} , i=1,2,…,5)	120 Ω

The corresponding experimental results for a 15A current command are shown in Figures 5.17-5.19 in terms of dynamic and steady-state considerations.

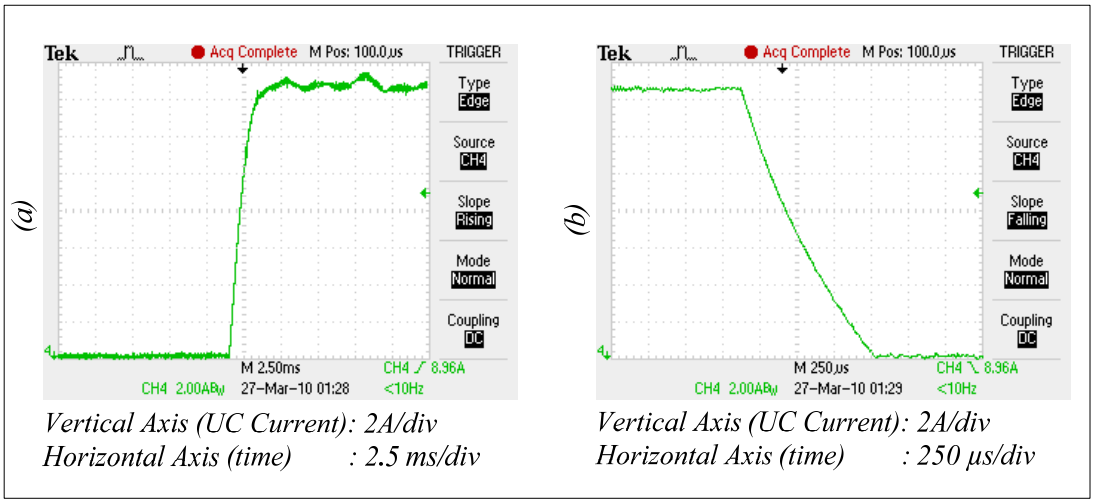


Figure 5.17 Experimental results for the dynamic response of the UC charging current for a 15A current command: (a) UC charging current build-up, (b) UC charging current fall.

According to the experimental results shown in Figure 5.17, the rise time and the fall time of the UC charging current for a 15A current command are observed as 2.5 ms and 0.96 ms, respectively. The obtained experimental values for the rise time and the fall time of the UC charging current show that the dynamic response of the actual charging system performance is consistent with the simulation results and this observation verifies the slow dynamic characteristics of the UC charging system due to the high values of the passive component parameters (L_{sd}, C_{uc}). When the current overshoot characteristics of the UC charging current shown in Figure 5.17 (a) is investigated, it is seen that no current overshoot exists. This result is consistent with the simulation results since the current overshoot observed in the charging system simulations is also at low levels.

The steady-state variation of the UC charging current for a 15A current command is shown in Figure 5.18.

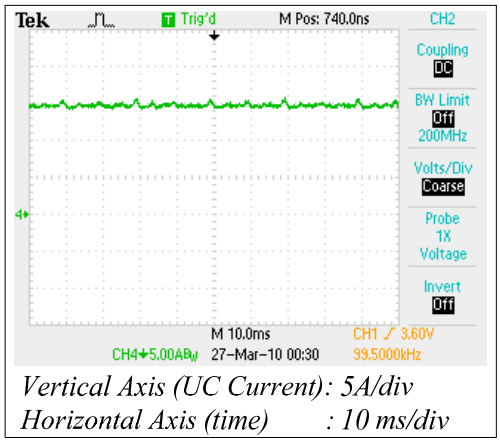


Figure 5.18 Experimental results for the steady-state UC charging current for a 15A current command.

As shown in Figure 5.18, the UC charging current remains constant at 15A level as expected.

The variation of the PWM signal for the controllable switch of the UC charging system together with the UC charging current is shown in Figure 5.19 at different UC terminal voltage levels.

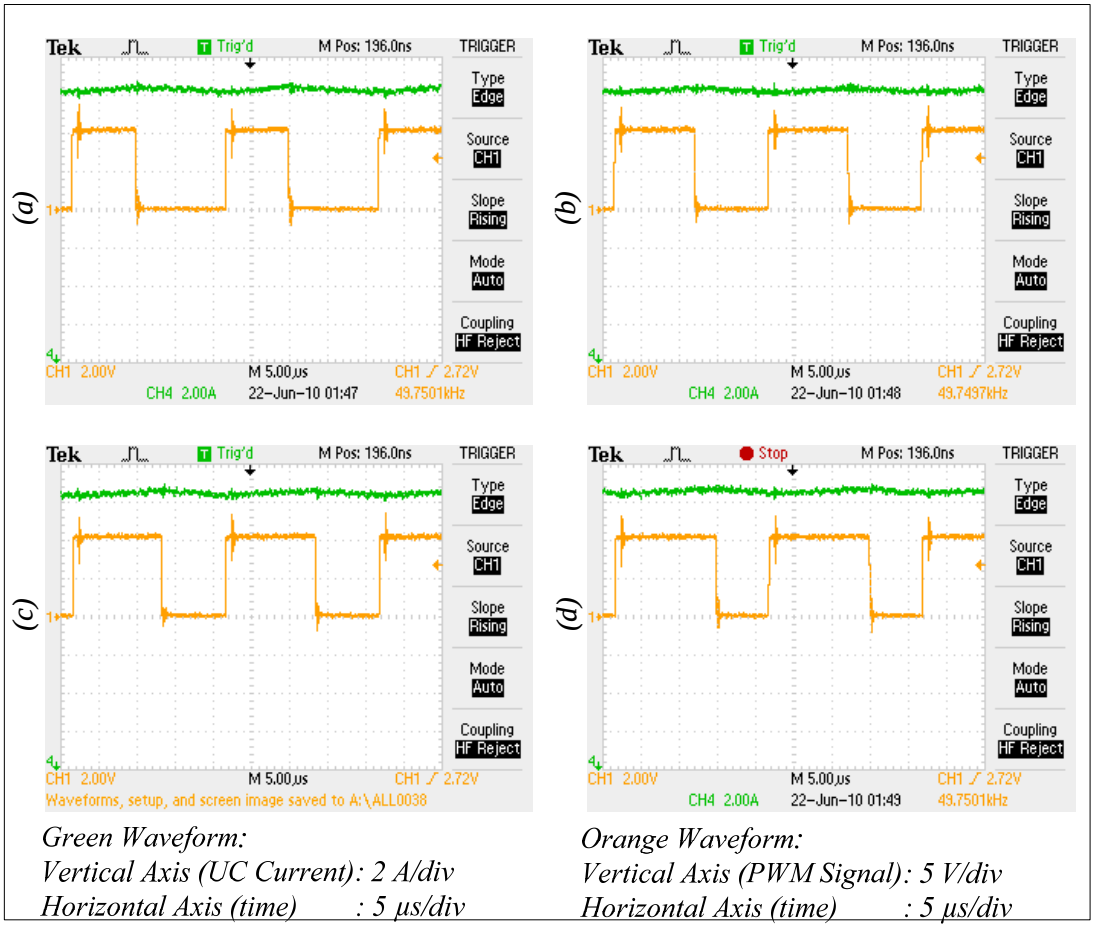


Figure 5.19 Experimental results for the switching signal and steady-state ripple characteristics of the UC charging current for a 15A current command: (a) at V_{uc} =5V, (b) at V_{uc} =6V, (c) at V_{uc} =8V, (d) at V_{uc} =10V.

As shown in Figure 5.19, the duty cycle value of the applied PWM signal increases as the terminal voltage of the UC increases. This is an expected result. Because, as the terminal voltage of the UC increases, the power drawn from the input supply should be increased in order to provide a constant charging current. Therefore, the UC charging system increases the duty cycle value of the applied PWM signal in order to provide a constant charging current throughout the charging operation. When the steady-state ripple characteristics of the UC charging current is investigated, it is seen that the ripple value of the UC charging current remains constant at 0.5A value for different UC terminal voltage levels. The constant ripple characteristic is resulted from the increase in duty cycle value of the PWM signal as the terminal voltage of the UC increases. The charging current ripple value obtained

from the experimental results is higher than the charging current ripple value obtained from the simulation results. The increase in charging current ripple is mainly resulted from the decrease in the inductance value of the step-down converter inductor (L_{sd}) at a switching frequency of 50 kHz.

5.3.4 Conclusions for the Performance of Ultracapacitor Charging System

Dynamic and steady-state performance parameters of the UC charging system according to the simulation and experimental results are summarized in Table 5.11.

Table 5.11 Performance parameters of UC charging system

Performance Parameters		*Simulation Performance*	*Experimental Performance*
Rise Time	t_{rise} (ms)	2.0	2.5
Fall Time	t_{fall} (ms)	1.81	0.96
Overshoot	M_i (%)	4.26	0
Steady-state Current Ripple	Δi (A)	0.125	0.5

As shown in Table 5.11, the experimental and simulation results are consistent in terms of dynamic and steady-state considerations. The most obvious conclusion for the UC charging system is the success of the implemented charging control structure since the performance parameters shown in Table 5.11 are sufficient for this application. It could be inferred that, the use of a PI current regulator with proper UC terminal voltage decoupling mechanism and a DC bus scaling operation gives sufficient performance for the control of the UC charging operation.

5.4 Ultracapacitor Discharging System

In Chapter 4, circuit topology and basic control structure of step-up DC-DC converters were reviewed in order to provide the discharging operations of UCs. In this section, the use of PI and hysteresis current regulators in a step-up DC-DC

converter based UC discharging system is investigated by also considering the implementation details in terms of microcontroller hardware considerations. The performance of the UC discharging system is demonstrated by the help of computer simulations and experimental results.

5.4.1 Microcontroller Based Ultracapacitor Discharging System

The power electronics converter structure of the implemented UC discharging system consists of a step-up DC-DC converter and a DC chopper. The step-up DC-DC converter is used as a discharging current regulator in order to provide the predetermined discharging current profiles to the UC under test. On the other hand, the DC chopper is used to maintain the output voltage of the step-up DC-DC converter constant to prevent the effect of output voltage variation on the performance of the current regulator. In the implemented UC discharging system, the control of step-up DC-DC converter and DC chopper is provided by separate microcontrollers which operate in parallel during the discharging process.

For the discharging current regulation, the performance of PI and hysteresis regulators is investigated, whereas the output voltage control is provided by a hysteresis controller. The control structures built inside the microcontrollers are shown in Figures 5.20-5.22. When the discharging system is operating, one of the current regulator structures shown in Figures 5.20-5.21 runs in parallel with the control structure built for the control of DC chopper which is shown in Figure 5.22. Operational details of the microcontroller based UC discharging system is summarized in Table 5.12. The microcontroller implementation of the control structures shown in Figures 5.20-5.22 is performed by considering the important points mentioned in Section 5.3.1.

Table 5.12 Operational details of the microcontroller based UC discharging system

PWM Frequency (PI Control)		50 kHz
Control Loop Update Period	*Current Regulator (PI)*	200 µs
	Current Regulator (Hysteresis)	50 µs
	Output Voltage Regulator (Hysteresis)	80 µs
Analog Readings	*Current Measurement*	10 bits
	UC Voltage Measurement	8 bits
	High Side Voltage Measurement	10 bits

Input to output functions of the UC discharging current measurement and UC voltage measurement are the same as the functions shown in Table 5.6, whereas the input to output function of the high side voltage measurement is given in (5.12).

$$v_h[n] = \frac{0.1428 \times v_{dc}(t)}{5} \times 2^{10} \tag{5.12}$$

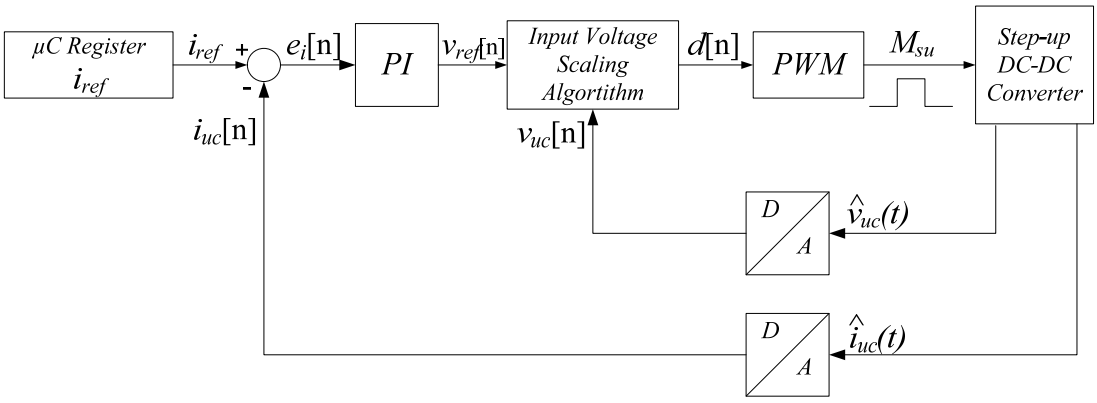


Figure 5.20 Block diagram of the microcontroller based UC discharging current regulator structure with a PI controller.

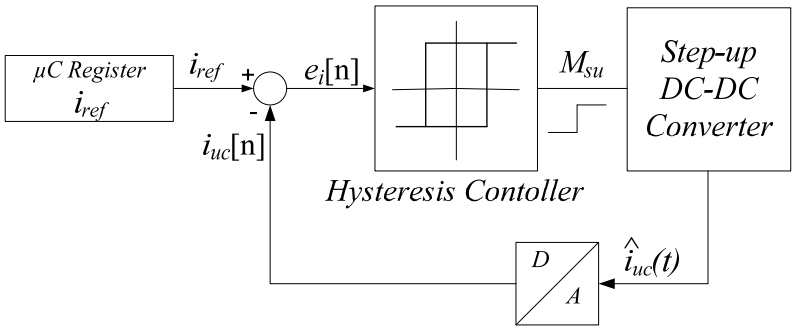


Figure 5.21 Block diagram of the microcontroller based UC discharging current regulator structure with a hysteresis controller.

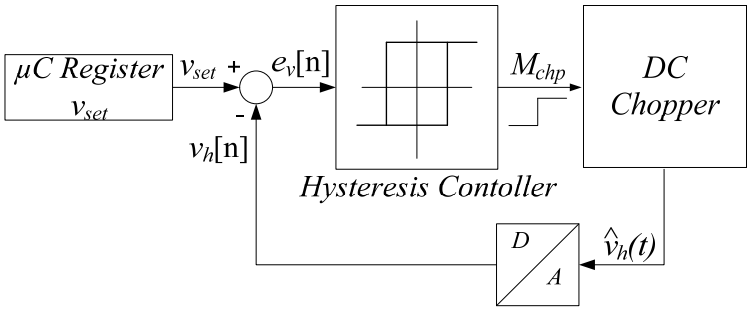


Figure 5.22 Block diagram of the microcontroller based DC chopper control structure with a hysteresis controller.

When the current regulator structure with a PI controller is investigated, it is seen that the first operation is the calculation of the current error signal (e_i[n]). After this operation, e_i[n] is fed to a PI regulator to generate the voltage reference value (v_{ref} [n]). Normally, duty cycle (d[n]) of the PWM signal for M_{su} could be obtained directly by proportioning v_{ref} [n] with the measured UC voltage (v_{uc} [n]). However, division operation could not be used inside the microcontrollers since fast calculation time is necessary. Therefore, an input voltage scaling algorithm is used to calculate d[n] instead of division operation. The algorithm is very similar to the DC bus scaling algorithm utilized for the UC charging system. However, the variation of UC voltage is larger than the variation of DC bus voltage. For this reason, UC voltage range in the discharging process is divided into five sections and the duty cycle calculations are performed in a similar approach that is given in (5.3)-(5.8). The input voltage scaling algorithm is shown in Figure 5.23. As the output of the input

voltage scaling algorithm, d[n] value is obtained and duty cycle parameter of the PWM modulator is updated accordingly.

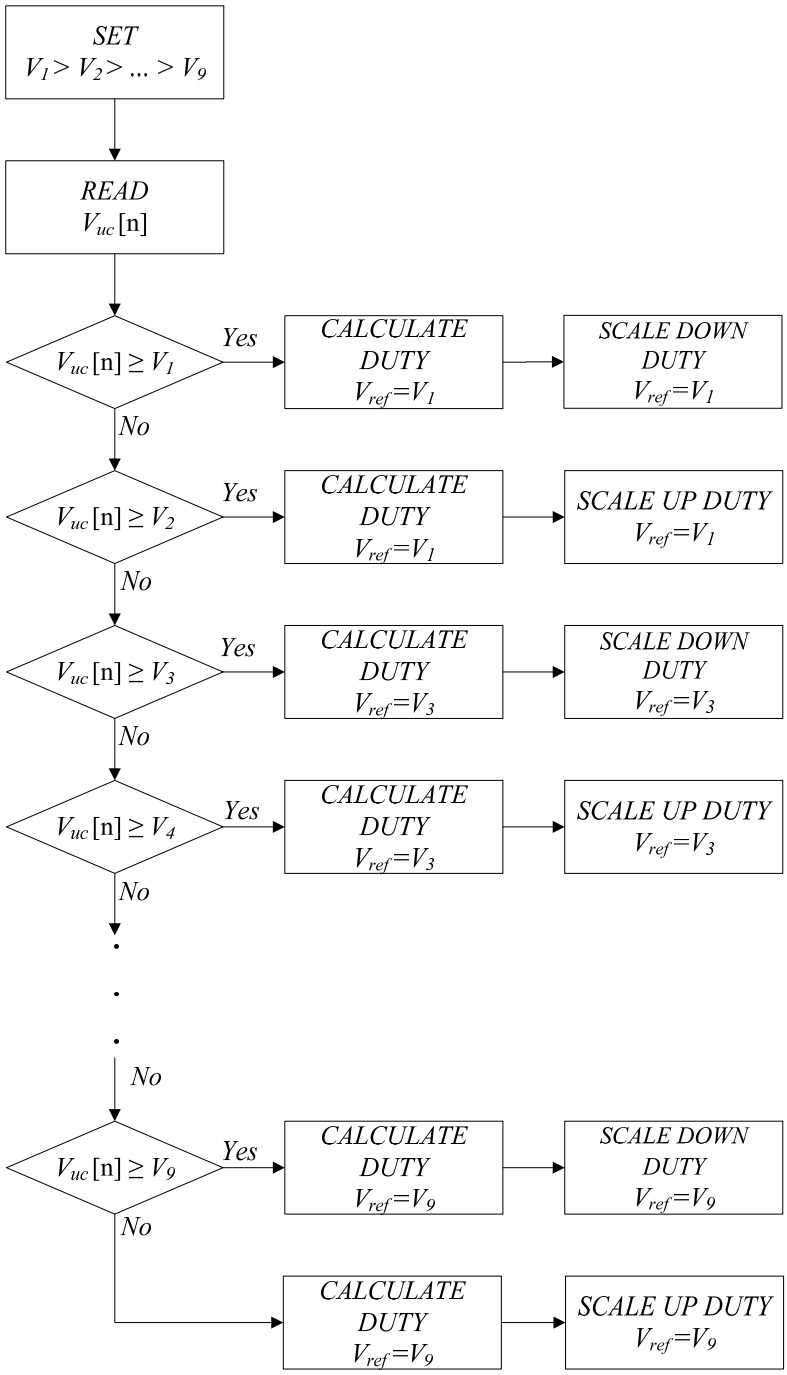


Figure 5.23 Input voltage scaling algorithm.

Program flow of the current regulator structure with a PI controller is shown in Figure 5.24.

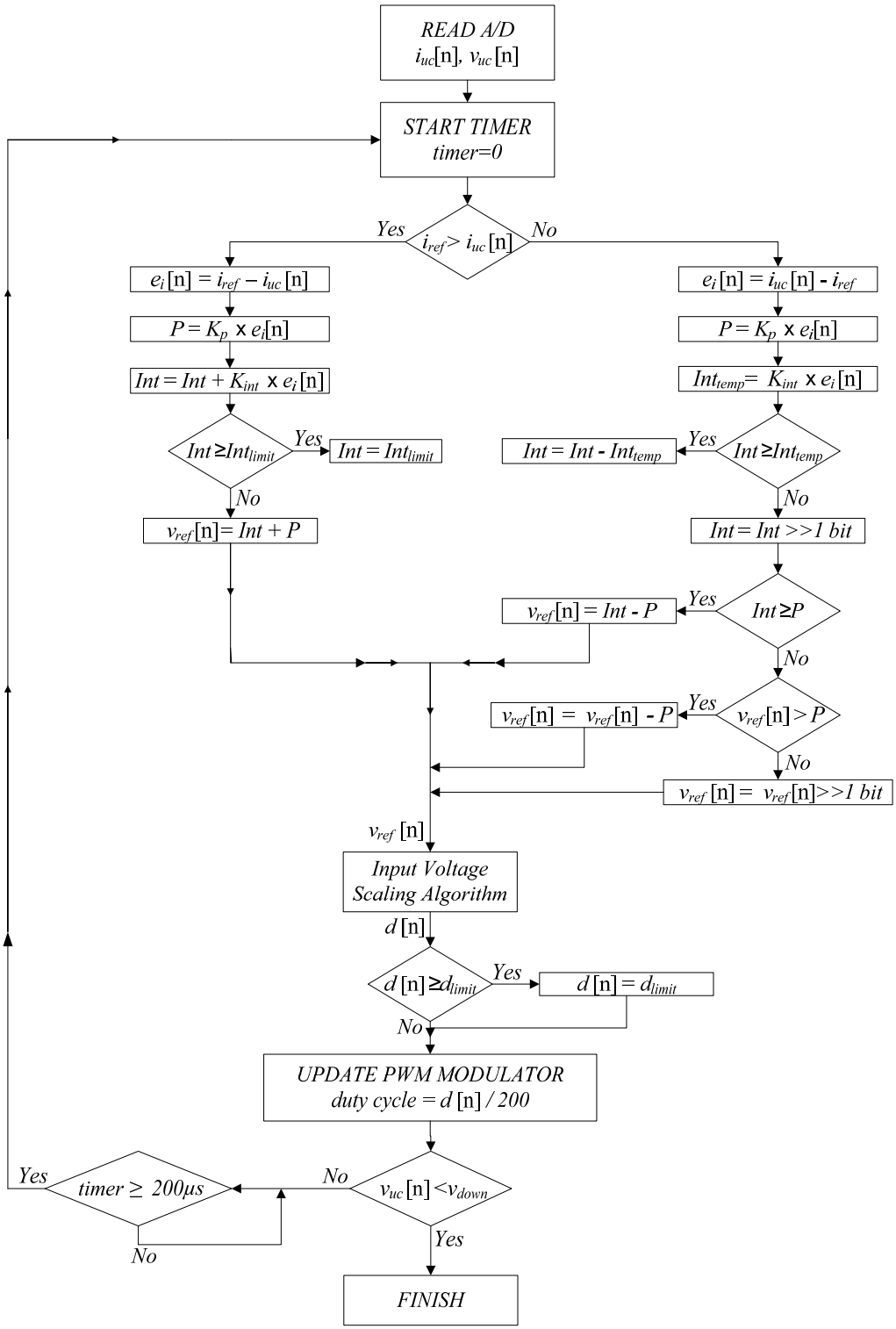


Figure 5.24 Program Flow of the UC discharging current regulator structure with a PI controller.

When the hysteresis regulator structure is compared with the PI regulator structure, it is seen that hysteresis control is simpler and less time consuming in terms of operations performed inside the microcontroller. The only operation performed inside the microcontroller is the adjustment of the switching signal of M_{su} as high (1) or low (0) according to the comparison of the measured UC discharging current (i_{uc}[n]) with the current reference (i_{ref}) and the tolerance band (Δi_{band}) parameter. The switching function of M_{su} ($s[M_{su}]$) obtained as an output of the hysteresis regulator is given in (5.13).

$$s[M_{su}] = \begin{cases} 0\ , & i_{uc}[n] > i_{up}, \quad (i_{up} = i_{ref} + \Delta i_{band}) \\ 1\ , & i_{uc}[n] < i_{down}, \quad (i_{down} = i_{ref} - \Delta i_{band}) \end{cases} \tag{5.13}$$

As given in (5.13), it is seen that the switching signal of M_{su} is made high in order to increase the UC discharging current when it is lower than the down limit (i_{down}) determined for the UC discharging current. On the other hand, switching signal of M_{su} is made low when the discharging current is higher than the up limit (i_{up}) determined for the UC discharging current. Program flow of the UC discharging current regulator structure with a hysteresis controller is shown in Figure 5.25.

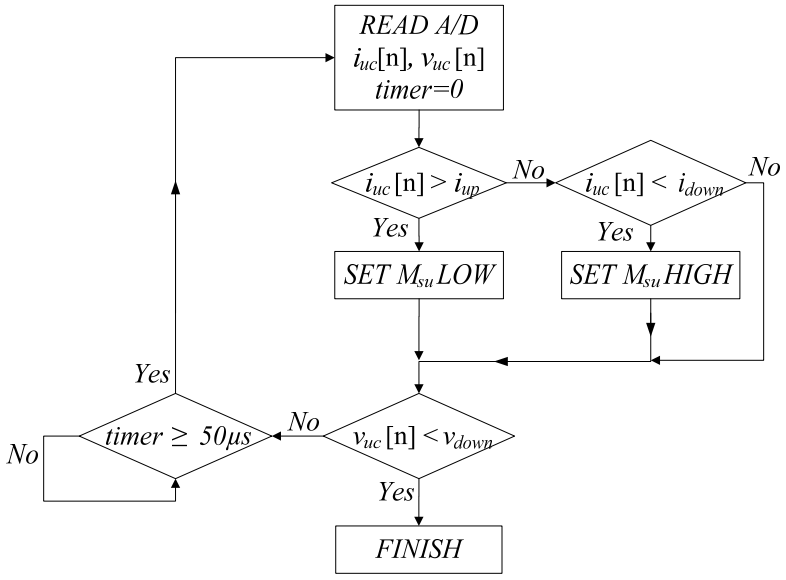


Figure 5.25 Program flow of the UC discharging current regulator structure with a hysteresis controller.

The last control mechanism used for the UC discharging system is the DC chopper control structure with a hysteresis controller. With this control structure output voltage (v_h) of the step-up DC-DC converter is maintained constant around a value determined by the set voltage (v_{set}) and tolerance band (v_{band}) parameter. The switching function of the chopper switch ($s[M_{chp}]$) obtained as an output of the DC chopper control structure is given in (5.14).

$$s[M_{chp}] = \begin{cases} 1\ , & v_h[n] > v_{up}\ , \quad \left(v_{up} = v_{set} + v_{band}\right) \\ 0\ , & v_h[n] < v_{down,} \quad \left(v_{down} = v_{set} - v_{band}\right) \end{cases} \tag{5.14}$$

As given in (5.14), the switching signal of M_{chp} is made high in order to decrease v_h when it is higher than the up limit (v_{up}). On the other hand, switching signal of M_{chp} is made low in order to increase v_h when it is lower than the down limit (v_{down}). Program flow of the DC chopper control structure is shown in Figure 5.26.

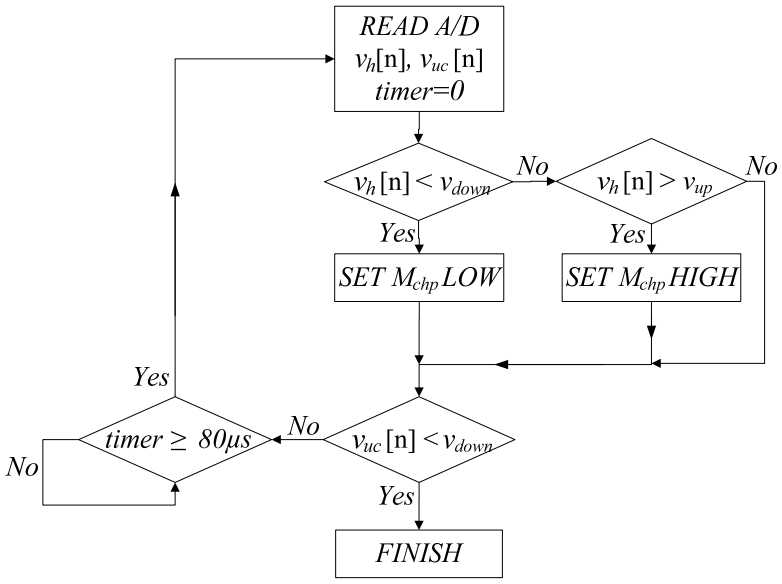


Figure 5.26 Program flow of the DC chopper control structure.

5.4.2 Simulation Performance of Ultracapacitor Discharging System

Performance of the control structures shown in Figures 5.20-5.22 is evaluated by the help of a simulation model built in Ansoft Simplorer 6.0 software. The circuit parameters shown in Table 5.1 and the control loop parameters shown in Table 5.12 are taken into consideration while building the simulation model. Simulation model of the discharging system is shown in Figure 5.27. Inside the current controller block of the simulation model, both PI and hysteresis regulators are implemented. However, scaling block is not used for the hysteresis regulator. Simulation results for both of the regulator types are put forward separately. The UC model used in the discharging simulation system is the same as the model used for the charging system.

Control loop parameters of the simulation model are summarized in Table 5.13. Tuning of the PI parameters is realized with an experimental approach similar to the UC charging system. However, to determine K_p, 60 % of the current command is observed at the steady-state waveform of discharging current. The reason for using 60 % of the current command instead of 80 % is due to reduce the overshoot characteristics of the system. On the hysteresis regulator side, tolerance bands are selected to achieve sufficient performance with minimal switching.

Table 5.13 Control loop parameters of the simulation model of the UC discharging system

Sampling Time	*Current Controller (PI)*	200 µs
	Current Controller (Hysteresis)	50 µs
	Chopper Controller (Hysteresis)	80 µs
PI Parameters	K_p *(Proportional)*	0.75
	K_i *(Integral)*	0.125
Hysteresis Parameters	*Current Band* (i_{uc})	0.2 A
	Voltage Band (v_h)	0.2 V
Controller Limits	I_{limit} *(Integral)*	120
	d_{limit} *(Duty Cycle)*	180
	d_{full} *(Duty Cycle)*	200
Initial Conditions	$I_L(0)$	0 A
	$V_{uc}(0)$	12V
Simulation Parameters	*Simulation Step (max)*	2 µs
	Simulation Step (min)	200 ns

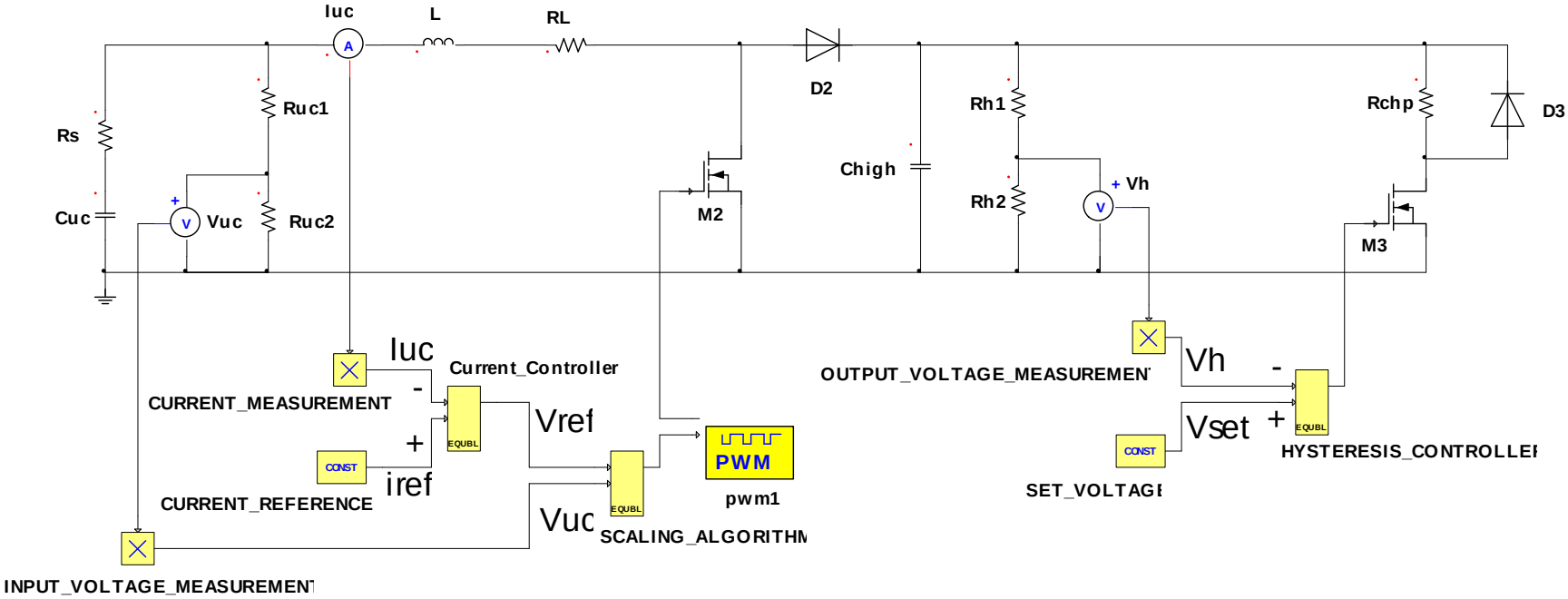


Figure 5.27 Simulation model of the UC discharging system.

Simulation results for the dynamic response and the steady-state ripple characteristics of the UC discharging current for a 15A current command, and output voltage variation of the step-up DC-DC converter for a 19.5V set voltage command are shown in Figures 5.28-5.33 by considering the PI and hysteresis current regulators separately.

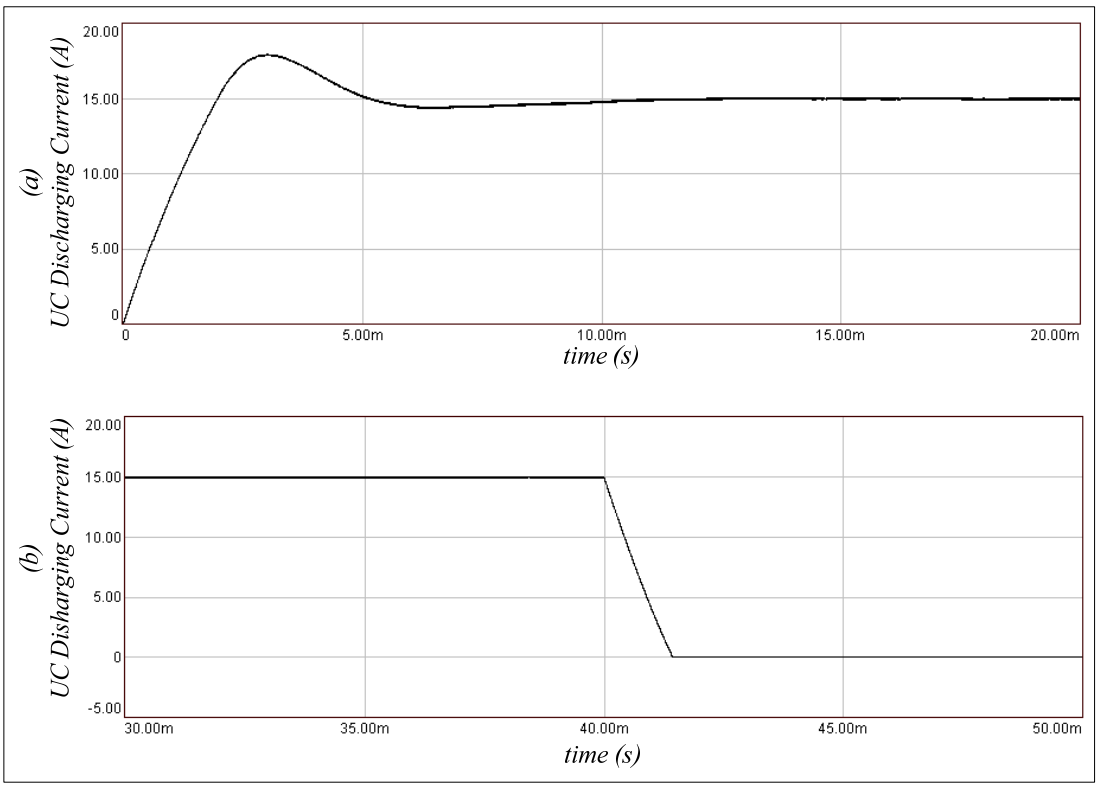


Figure 5.28 Simulation results for the dynamic response of the UC discharging current for a 15A current command considering the PI regulator case: (a) UC discharging current build-up, (b) UC discharging current fall.

According to Figure 5.28, it is seen that the UC discharging current shows a slow build-up and fall behaviour. The rise time (t_{rise}) and the fall time (t_{fall}) of the UC discharging current for a 15A current command are observed as 1.88 ms and 1.45 ms, respectively. It is also observed that the build-up and fall characteristics of the UC discharging current is similar to the build-up and fall characteristics of the UC charging current in terms of rise time and fall time, since the parameters of the passive components of both systems are the same and both of the simulation models are run with PI type controllers. According to the dynamic behaviour of the

discharging current, it is seen that the bandwidth of the UC discharging system is at low levels and the chosen 200µs sampling rate is sufficient for the UC discharging application. When the current overshoot characteristics shown in Figure 5.28 (a) is investigated, it is seen that there is a significant overshoot in the dynamic behaviour of the UC discharging current. The observed current overshoot value is 20 %. According to this observation it could be concluded that a PI type controller results in a significant value of current overshoot which could be problematic for the actual discharging system.

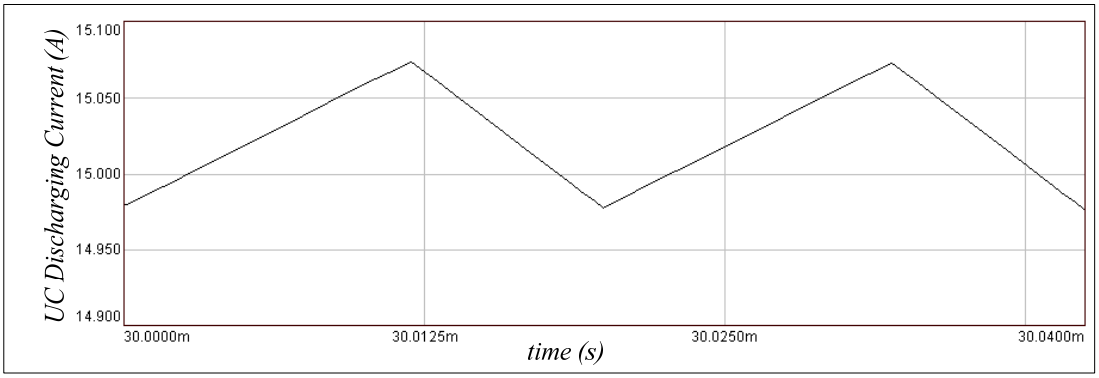


Figure 5.29 Simulation results for the steady-state ripple characteristics of the UC discharging current for a 15A current command considering the PI regulator case.

According to Figure 5.29, the steady-state discharging current ripple is observed as 0.1A. The observed current ripple value will not affect the terminal behaviour of a UC.

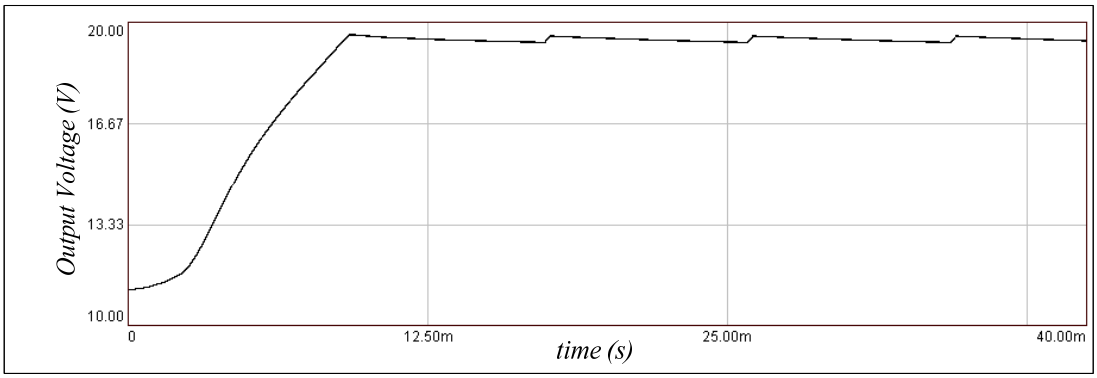


Figure 5.30 Simulation results for the output voltage characteristics of the UC discharging system for a 19.5V set voltage command considering the PI regulator case.

According to Figure 5.30, the output voltage of the step-up DC-DC converter shows a build-up behaviour until it reaches the high voltage limit of the DC chopper controller structure. As soon as the output voltage reaches the high voltage limit, it remains within the tolerance band of the DC chopper controller structure. The output voltage ripple of the UC discharging system is observed as 0.225V. The hysteresis voltage band programmed inside the controller is 0.2V. Therefore, it could be concluded that the chosen sampling time for the DC chopper structure is sufficient for the application.

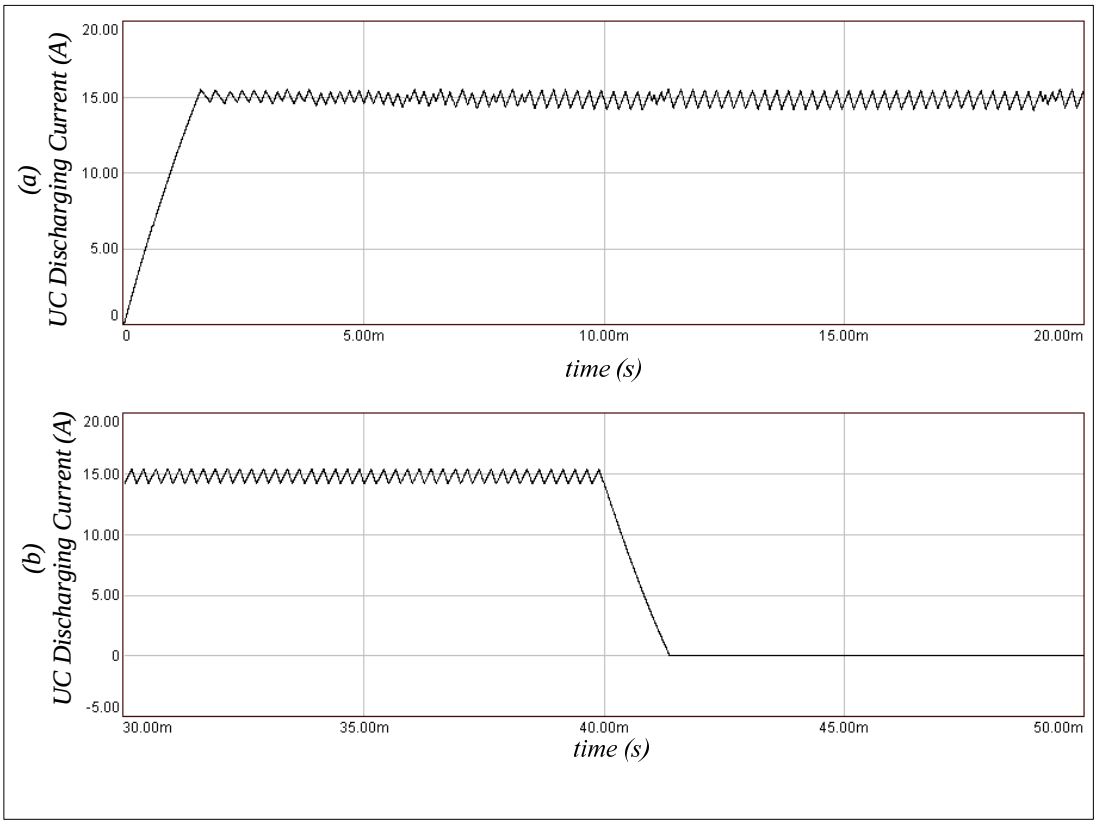


Figure 5.31 Simulation results for the dynamic response of the UC discharging current for a 15A current command considering the hysteresis regulator case: (a) UC discharging current build-up, (b) UC discharging current fall.

According to Figure 5.31, it is seen that the build-up and fall characteristics of the UC discharging current for the hysteresis regulator case is similar to the build-up and fall characteristics of the UC discharging current for the PI regulator case in terms of rise time and fall time. The observed values for the rise time and fall time of the UC discharging current are 1.535 ms and 1.40 ms, respectively. For the hysteresis regulator case the controllable switch of the step-up DC-DC converter (M_{su}) is put in conduction mode until the UC discharging current reaches the upper limit of the hysteresis controller. The decrease in the rise time of the UC discharging current for the hysteresis regulator case is resulted from this behaviour since the optimum structure for building-up the discharging current in minimum time could be achieved by putting M_{su} in conduction mode until the UC discharging current reaches the current command. When the dynamic characteristics of the UC discharging current is investigated in terms of current overshoot, it is seen that there is no overshoot in the

build-up characteristics of the UC discharging current for the hysteresis regulator case. This result could be viewed as an advantage of the hysteresis controller structure over the PI regulator, since 20 % overshoot is observed in the dynamic behaviour of the UC discharging current for the PI regulator case.

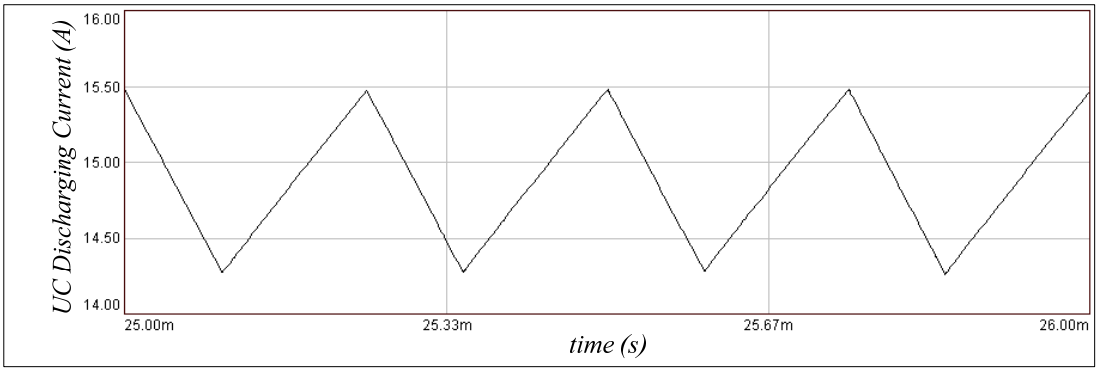


Figure 5.32 Simulation results for the steady-state ripple characteristics of the UC discharging current for a 15A current command considering the hysteresis regulator case.

According to Figure 5.32 it is seen that the steady-state ripple value of the UC discharging current for the hysteresis regulator case is higher than the steady-state ripple value of the UC discharging current for the PI regulator case. The observed discharging current ripple value for the hysteresis regulator case is 1.2A. When compared with the discharging current ripple value of the PI regulator, which is 0.1A, the discharging current ripple value for the hysteresis regulator case is twelve times higher than the discharging current ripple value of the PI regulator. The sampling time chosen for the hysteresis regulator should be increased in order to reduce the current ripple value. However, in practice the reduction in sampling time of the hysteresis controller refers to high speed current measurements which will decrease the measurement accuracy. Therefore, it is obvious that the high steady-state ripple value of the UC discharging current is the disadvantage of the hysteresis regulator.

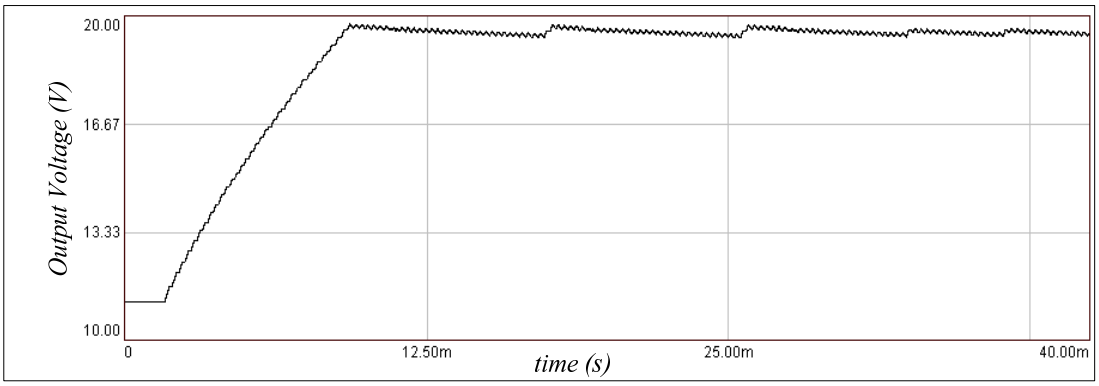


Figure 5.33 Simulation results for the output voltage characteristics of the UC discharging system for a 19.5V set voltage command considering the hysteresis regulator case.

According to Figure 5.33 it is seen that, the build-up and steady-state characteristic of the output voltage of the step-up DC-DC converter for the hysteresis regulator case is similar with the output voltage characteristics shown for the PI regulator case. The observed voltage ripple is 0.4V.

5.4.3 Experimental Performance of Ultracapacitor Discharging System

Experimental performance of the UC discharging system is obtained for the control loop parameters shown in Table 5.14. The UC module used during the charging operation is also used for the discharging operation. The corresponding experimental results for a 15A current command are shown in Figures 5.34-5.40 in terms of dynamic and steady-state considerations.

Table 5.14 Control loop parameters of the microcontroller based UC discharging system

Sampling Time	*Current Controller (PI)*	200 µs
	Current Controller (Hysteresis)	50 µs
	Chopper Controller (Hysteresis)	80 µs
PI Parameters	K_p *(Proportional)*	0.75
	K_i *(Integral)*	0.125
Hysteresis Parameters	*Current Band* (i_{uc})	0.2 A
	Voltage Band (v_h)	0.2 V
Controller Limits	I_{limit} *(Integral)*	120
	d_{limit} *(Duty Cycle)*	180
	d_{full} *(Duty Cycle)*	200

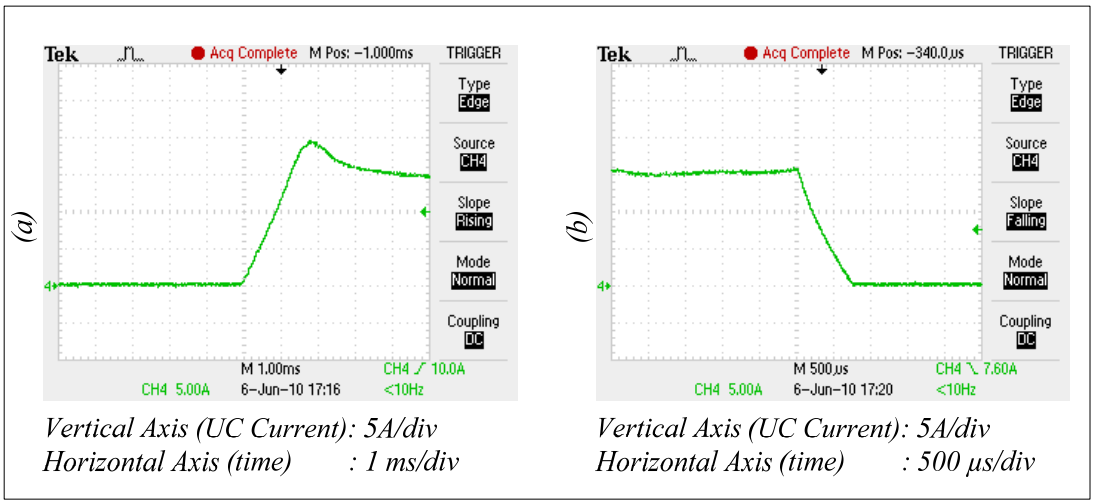


Figure 5.34 Experimental results for the dynamic response of the UC discharging current for a 15A current command considering the PI regulator case: (a) UC discharging current build-up, (b) UC discharging current fall.

According to the experimental results shown in Figure 5.34, rise time and fall time of the UC discharging current for a 15A current command are observed as 1.36 ms and 0.78 ms, respectively. It is seen that the rise time and fall time values obtained from the experimental results are consistent with the simulation results which proves that the dynamic behaviour of the system is slow. On the other hand, the current overshoot is observed as 33 % when the build-up behaviour of the UC discharging current shown in Figure 5.34 (a) is considered. This result shows that the PI regulator

structure results in a high value of current overshoot which is also observed in the simulation results.

The steady-state variation of the UC discharging current is shown in Figure 5.35.

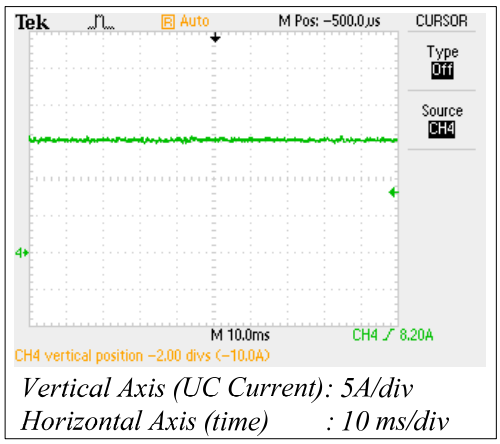


Figure 5.35 Experimental results for the steady-state UC discharging current for a 15A current command considering the PI regulator case.

As shown in Figure 5.35, the UC discharging current remains constant at 15A current command level. This result shows that the PI regulator structure gives sufficient steady-state performance.

The PWM signal of the controllable switch of the step-up DC-DC converter together with the UC discharging current are shown in Figure 5.36 for the PI regulator case.

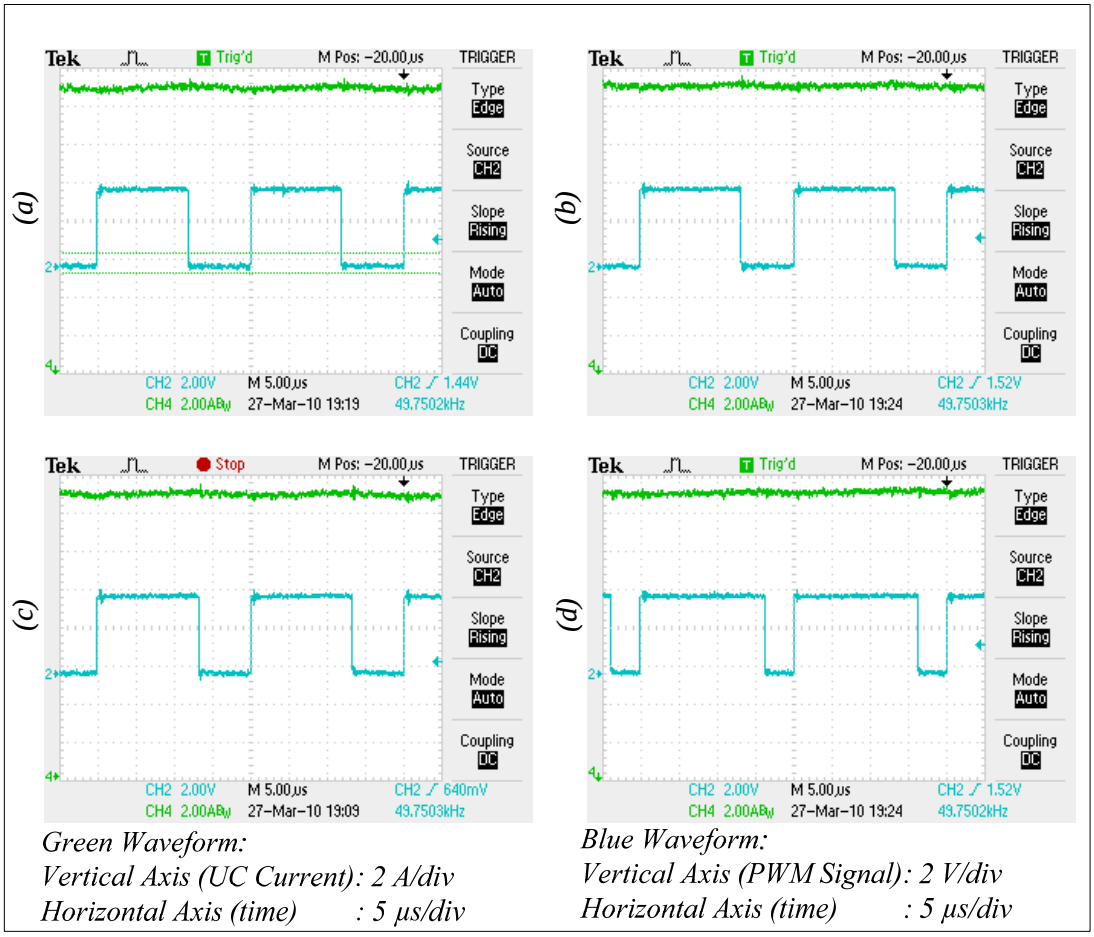


Figure 5.36 Experimental results for the steady-state ripple characteristics of the UC discharging current for a 15A current command considering the PI regulator case: (a)V_{uc} =11.6V, (b)V_{uc} =10V, (c)V_{uc} =8V, (d)V_{uc} =6.4V.

According to Figure 5.36, it is seen that, the duty cycle of the PWM signal increases as the terminal voltage of the UC decreases in order to maintain a constant discharging current. When the ripple characteristic of the UC discharging current is investigated it is seen that the current ripple remains constant at 0.4A level. The constant current ripple characteristic is resulted from the increase in duty cycle of the PWM signal as the terminal voltage of the UC decreases. The observed current ripple value of 0.4A is higher than the 0.1A current ripple value obtained from the simulation results. The increase in the discharging current ripple is mainly resulted from the decrease in converter inductance (L_{su}) value at a switching frequency of 50 kHz which is also observed for the charging operation case.

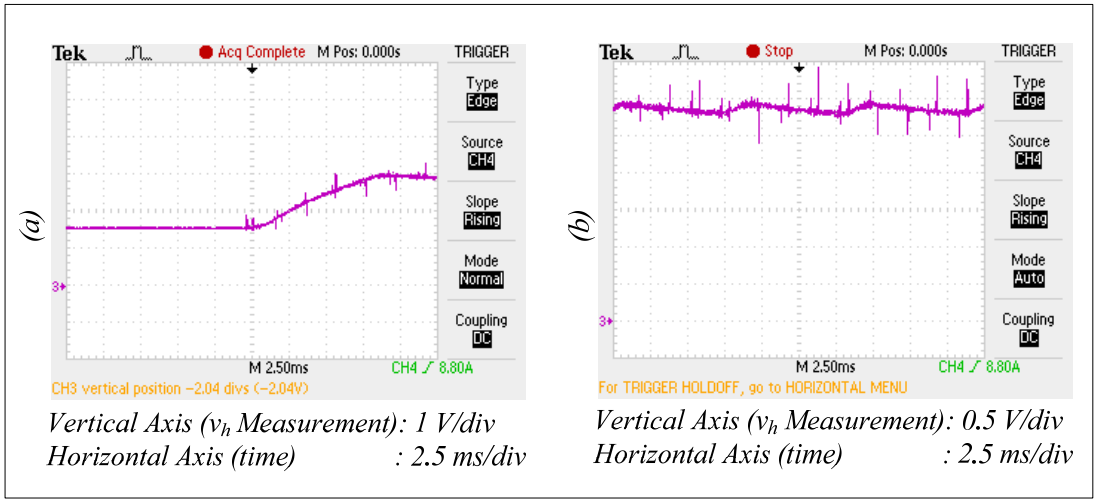


Figure 5.37 Experimental results for the output voltage characteristics of the UC discharging system for a 19.5V set voltage command considering the PI regulator case: (a) output voltage build-up, (b) steady-state variation of output voltage.

The scaled version of the step-up DC-DC converter output voltage variation for the PI regulator case is shown in Figure 5.37. The output voltage increases until it reaches the high voltage level of the DC chopper controller structure. As soon as the output voltage reaches the high limit it remains in a voltage band. It is seen that the output voltage ripple value of the actual UC discharging system is 1.5V. This value is higher than the output voltage ripple value of 0.225V obtained from the simulation results. The increase in voltage ripple is resulted from the reduced measurement accuracy of the actual system. However, an output voltage ripple value of 1.5V does not affect the operation of the UC discharging system negatively.

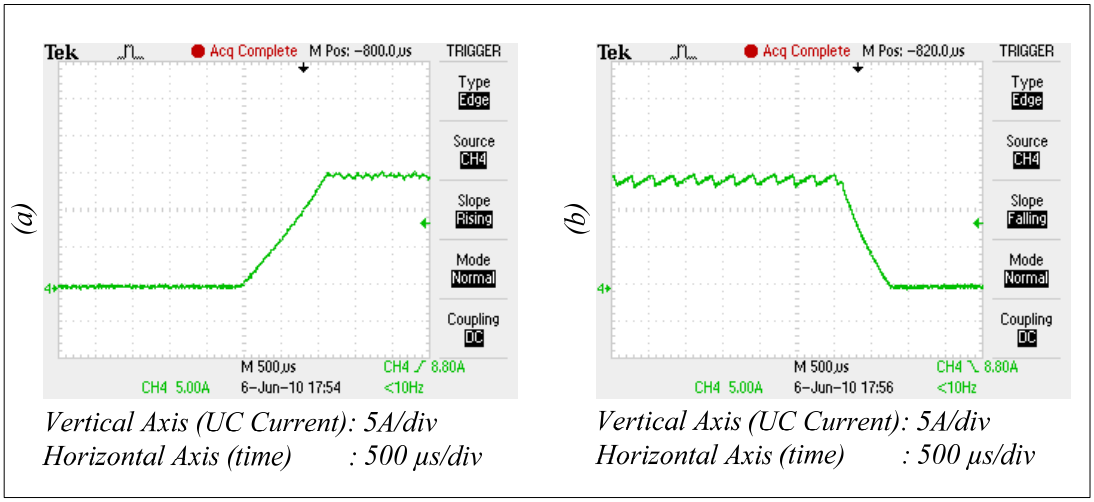


Figure 5.38 Experimental results for the dynamic response of the UC discharging current for a 15A current command considering the hysteresis regulator case: (a) UC discharging current build-up, (b) UC discharging current fall.

The build-up and fall characteristics of the UC discharging current for the hysteresis regulator case are shown in Figure 5.38. According to Figure 5.38, the rise time and the fall time of the UC discharging current are observed as 1.18 ms and 0.74 ms, respectively. It is seen that the rise time of the UC discharging current for the hysteresis regulator case is smaller than the rise time of the UC discharging current for the PI regulator case which is also observed in the simulation results. This result verifies that the hysteresis controller has the capability of building-up the UC discharging current in minimum time. On the other hand, no overshoot is observed in the build-up behaviour of the UC discharging current which could be viewed as an advantage of hysteresis type current regulator.

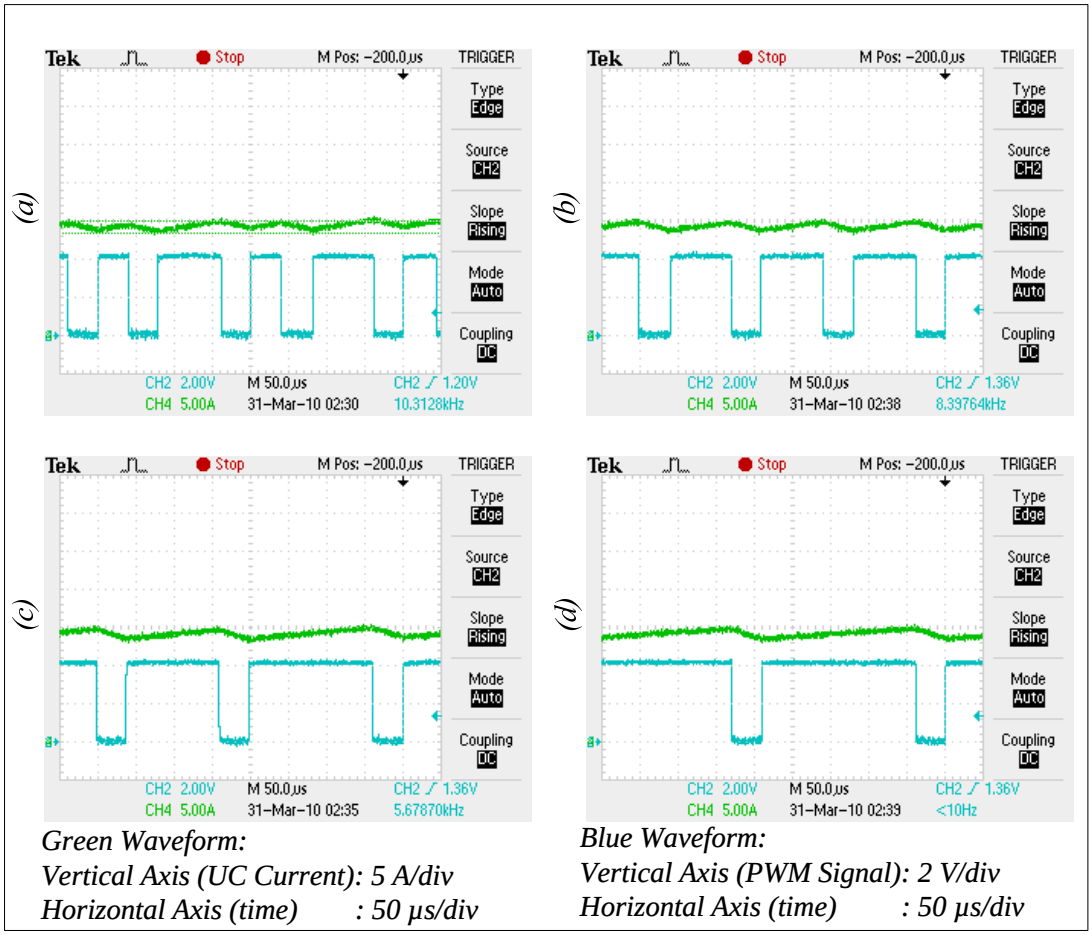


Figure 5.39 Experimental results for the steady-state ripple characteristics of the UC discharging current for a 15A current command considering the hysteresis regulator case: (a) V_{uc} =11.6V, (b) V_{uc} =9.80V, (c) V_{uc} =7.6V, (d) V_{uc} =6.5V.

The switching signals of the controllable switch of the step-up DC-DC converter together with the variation of the UC discharging current is shown in Figure 5.39. It is seen that the frequency of the switching signal is not constant and it decreases as the terminal voltage of the UC decreases in order to maintain a constant discharging current. The discharging current ripple value maintains constant at 1.5A level for different UC terminal voltage levels. The constant current ripple characteristic is resulted from the decrease in the frequency of the switching signal as the terminal voltage of the UC decreases. It is also seen that the observed current ripple value is higher than the discharging current ripple value of 0.4A obtained for the PI regulator case. The higher current ripple value observed for the hysteresis regulator case shows

that the sampling time and measurement accuracy is not sufficient for this control method.

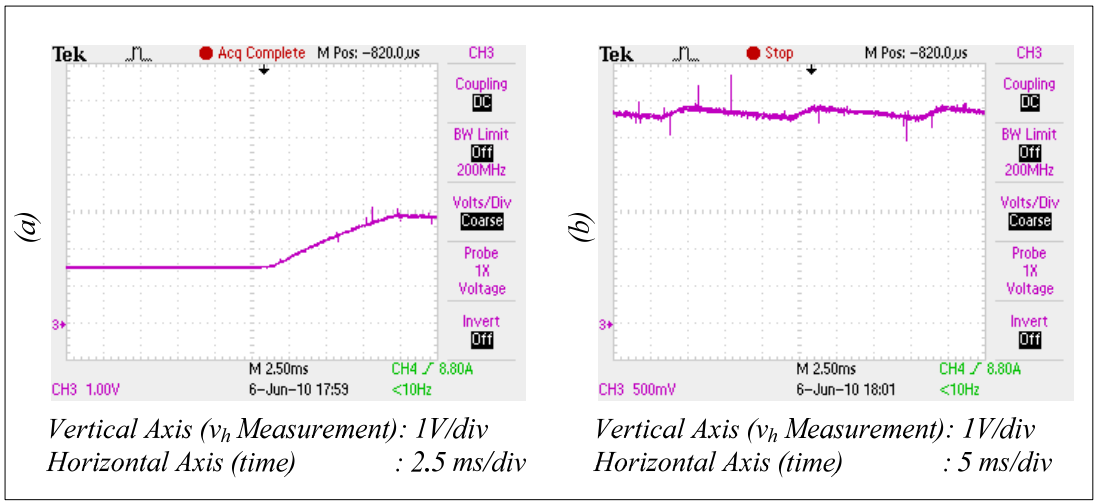


Figure 5.40 Experimental results for the output voltage characteristics of the UC discharging system for a 19.5V set voltage command considering the hysteresis regulator case: (a) output voltage build-up, (b) steady-state variation of output voltage.

In Figure 5.40, output voltage variation of the step-up DC-DC converter for the hysteresis regulator case is shown. The output voltage characteristics observed for the hysteresis regulator case is similar with the output voltage characteristics observed for the PI regulator case.

5.4.4 Conclusions for the Performance of Ultracapacitor Discharging System

Dynamic and steady-state performance parameters of the UC discharging system according to the simulation and experimental results are summarized in Table 5.15. As shown in Table 5.15, the experimental and simulation results are consistent in terms of dynamic and steady-state considerations. The most outstanding conclusion of the UC discharging system is the dynamic response success of the hysteresis regulator and the steady-state response success of the PI regulator. At this point it is seen that a hybrid control structure that utilizes the advantage of both regulators is

suitable for a UC discharging system. Therefore, in the scope of the thesis study a hybrid control structure is built for the discharging operation of UCs according to this conclusion. The flowchart of the hybrid control structure built inside the microcontroller is shown in Figure 5.41.

Table 5.15 Performance parameters of UC discharging system

Performance Parameters		*Simulation Performance*		*Experimental Performance*	
		PI	*Hysteresis*	*PI*	*Hysteresis*
Rise Time	t_{rise} (ms)	1.88	1.535	1.36	1.18
Fall Time	$t_{iniş}$ (ms)	1.45	1.40	0.78	0.74
Overshoot	M_i (%)	20	0	33	0
Steady-state Current Ripple	Δi (A)	0.1	1.2	0.4	1.5
Output Voltage Ripple	Δv_{out} (V)	0.225	0.4	1.5	1.5

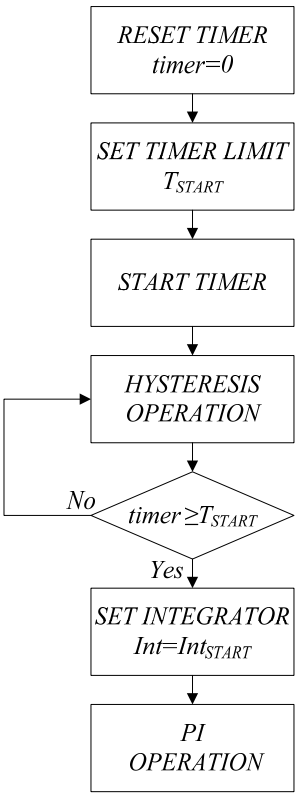


Figure 5.41 Flowchart of the hybrid control structure proposed for the UC discharging system.

As shown in Figure 5.41, the UC discharging process is started with the hysteresis regulator and the hysteresis regulator is made active for a time period determined by the starting time parameter (T_{START}). Within the chosen starting time parameter, the UC discharging current should reach the steady-state level. When the starting time is passed, a value is set to the integrator of the PI regulator and then PI regulator is enabled. The value that will be set to the integrator (Int_{START}) is dependent with the magnitude of the current reference.

Both simulation and experimental performance of the hybrid control structure is investigated in the scope of the study. For the simulation system the starting time parameter (T_{START}) is set to 10ms and a digital value of 100 is selected for the integrator start parameter (Int_{START}). The simulation results of the hybrid structure for a 15A current command are shown in Figure 5.42.

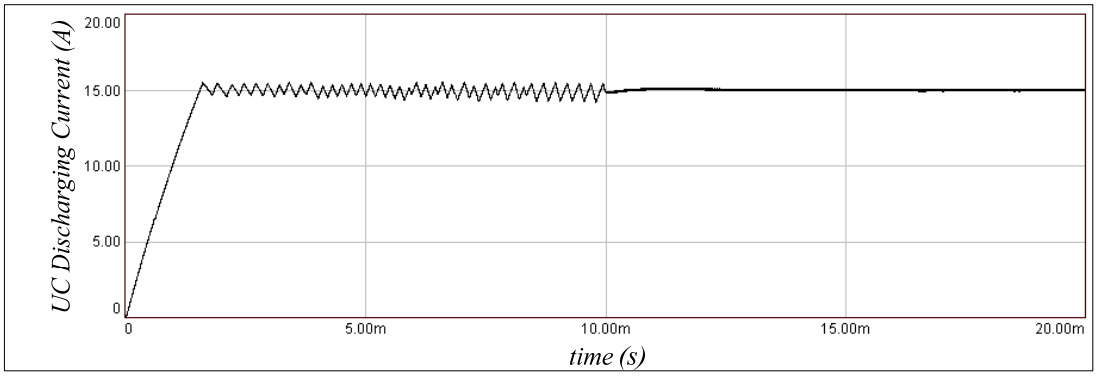
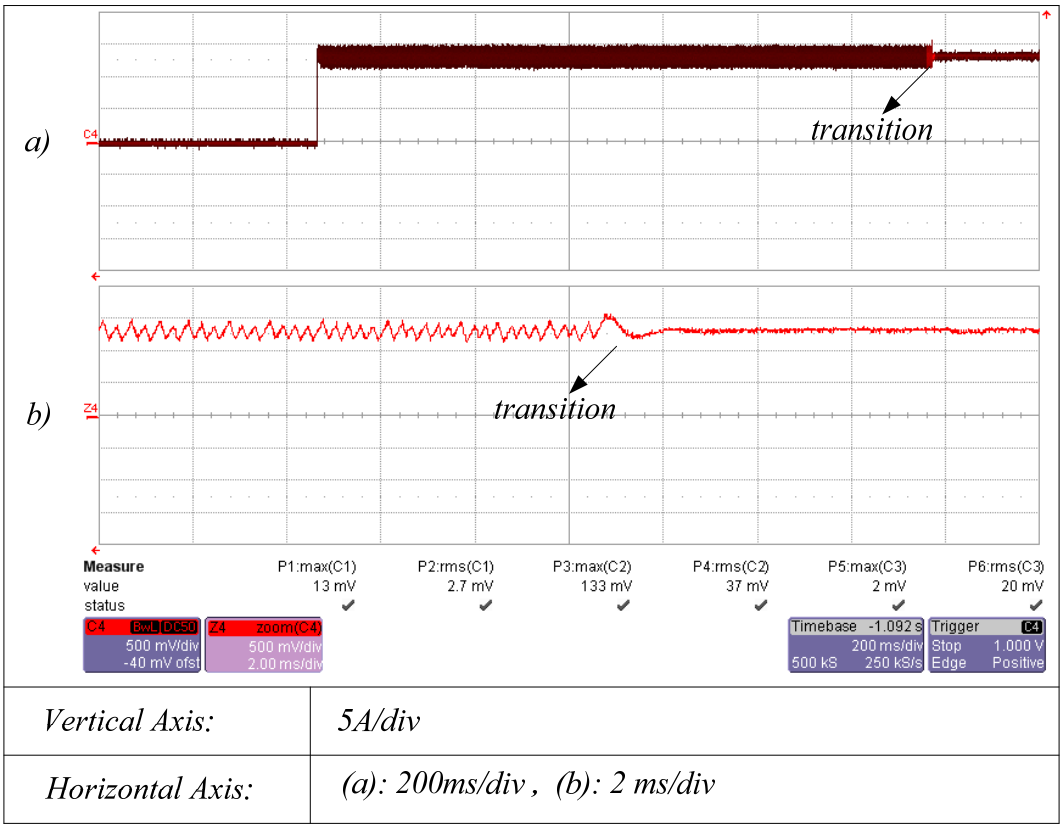


Figure 5.42 Simulation results of the UC discharging system with a hybrid controller structure for a 15A current command.

As shown in Figure 5.42, the UC discharging system is started with the hysteresis regulator. Therefore, no overshoot is observed in the discharging current waveform. After 10 ms is passed, integrator of the PI regulator is set to a value and then, PI regulator is made active. By this way, lower steady-state ripple characteristic of the PI regulator is utilized.

For the experimental system, the starting time parameter (T_{START}) is set to 1.3s and a digital value of 100 is selected for the integrator start parameter (Int_{START}). The experimental results of the hybrid control structure are shown in Figure 5.43.



Vertical Axis:	*5A/div*
Horizontal Axis:	*(a): 200ms/div , (b): 2 ms/div*

Figure 5.43 Experimental results for the UC discharging system with a hybrid controller structure for a 15A current command: (a) build up and transition behaviour of the UC discharging current, (b) transition behaviour of the UC discharging current (zoomed).

As shown in Figure 5.43 (a), the build up of the UC discharging is provided by the hysteresis current regulator. Therefore, no overshoot characteristic is observed in the discharging current waveform. After 1.3s is passed, PI regulator is made active and current ripple value decreases significantly as a result of the PI regulator operation. In Figure 5.43 (b), a zoomed oscillogram for the transition period is shown. It is obvious that there is a soft transition between the hysteresis and PI regulators in this period.

Dynamic and steady-state performance parameters of the UC discharging system with the hybrid controller structure are summarized in Table 5.16 according to the simulation and experimental results.

Table 5.16 Performance parameters of UC discharging system with hybrid controller

Performance Parameters of the Hybrid Controller		*Simulation Performance*	*Experimental Performance*
Rise Time	t_{rise} (ms)	1.535	1.18
Fall Time	t_{inis} (ms)	1.40	0.74
Overshoot	M_i (%)	0	0
Steady-state Current Ripple	Δi (A)	0.1	0.4

Performance parameters summarized in Table 5.16 shows that the hybrid controller utilizes the positive aspects of the hysteresis and PI current regulators in terms of dynamic and steady state considerations. Therefore, for the final verification of the experimental UC test system, hybrid controller is used for the discharging current regulation requirement.

CHAPTER 6

EXPERIMENTAL PERFORMANCE EVALUATION OF AN ULTRACAPACITOR MODULE

6.1 Introduction

In Chapter 5, hardware design and performance of a laboratory constructed UC test system was expressed in terms of dynamic and steady-state considerations. For evaluating the performance of the implemented UC test system, a UC module composed of five serially connected UC cells with a passive resistor voltage balancing structure was utilized. The electrical parameters of the constructed UC module were also expressed in Chapter 5. In the scope of the thesis study, constant current and constant power test procedures are applied to the constructed UC module by utilizing the implemented UC test system.

In this chapter, constant current and constant power test results of the UC module are presented. The aim of the constant current test procedure is to evaluate the capacitance and ESR parameters of the constructed UC module for the charging and discharging phases separately. The capacitance parameter is evaluated by means of considering the linear variation of the terminal voltage of the UC module and the ESR parameter is evaluated by means of considering the immediate voltage rise and fall events when the test current is applied or terminated as described in Chapter 3. After the constant current test results section, constant power test results of the UC module are presented. The aim of the constant power tests is to evaluate the constant power charging and discharging characteristics of the UC module. By means of constant power tests, round trip cycle efficiency of the UC module, which is defined

as the ratio of energy expressions in the charging and discharging phases, is evaluated.

In the laboratory, both a UC module and an electrolytic capacitor module are constructed and their energy storage capabilities are compared with respect to the volumetric considerations. The constructed UC module is shown in Figure 6.1.

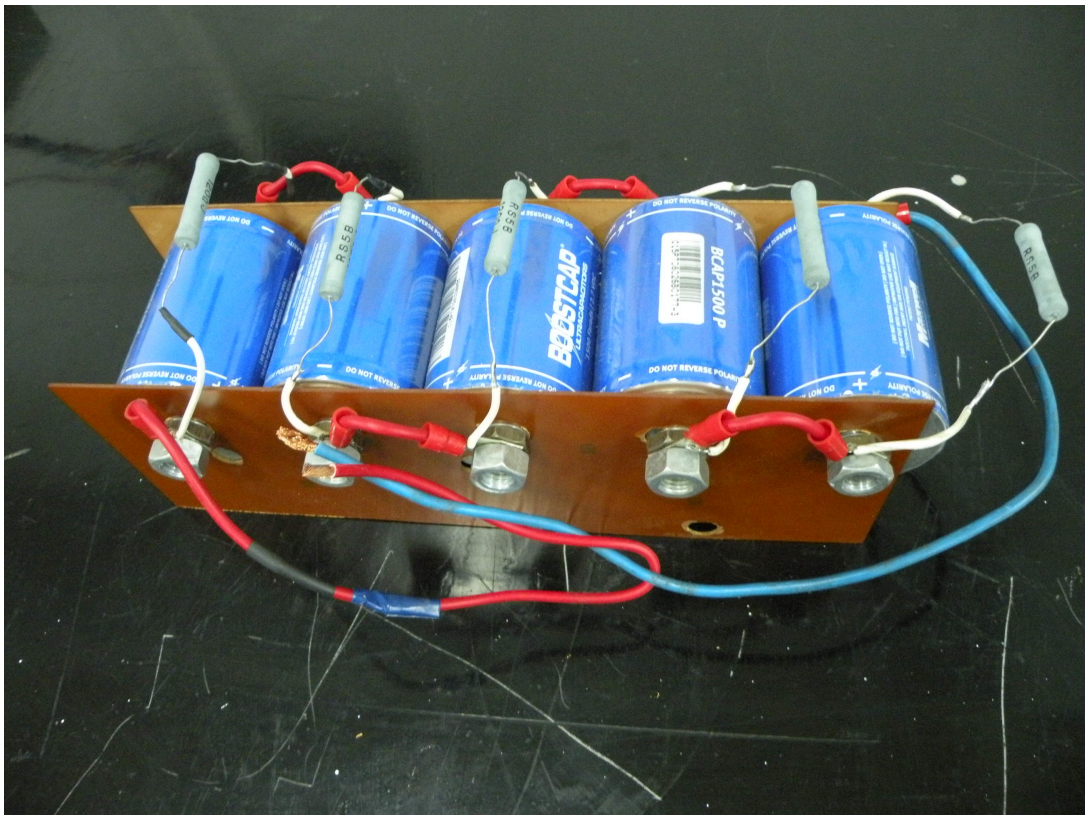


Figure 6.1 The laboratory constructed UC module.

As shown in Figure 6.1, the laboratory constructed UC module is composed of five serially connected UC cells. Voltage balancing resistors are placed in the terminals of the UC cells. The comparison of the UC and electrolytic capacitor modules is shown in Figure 6.2.

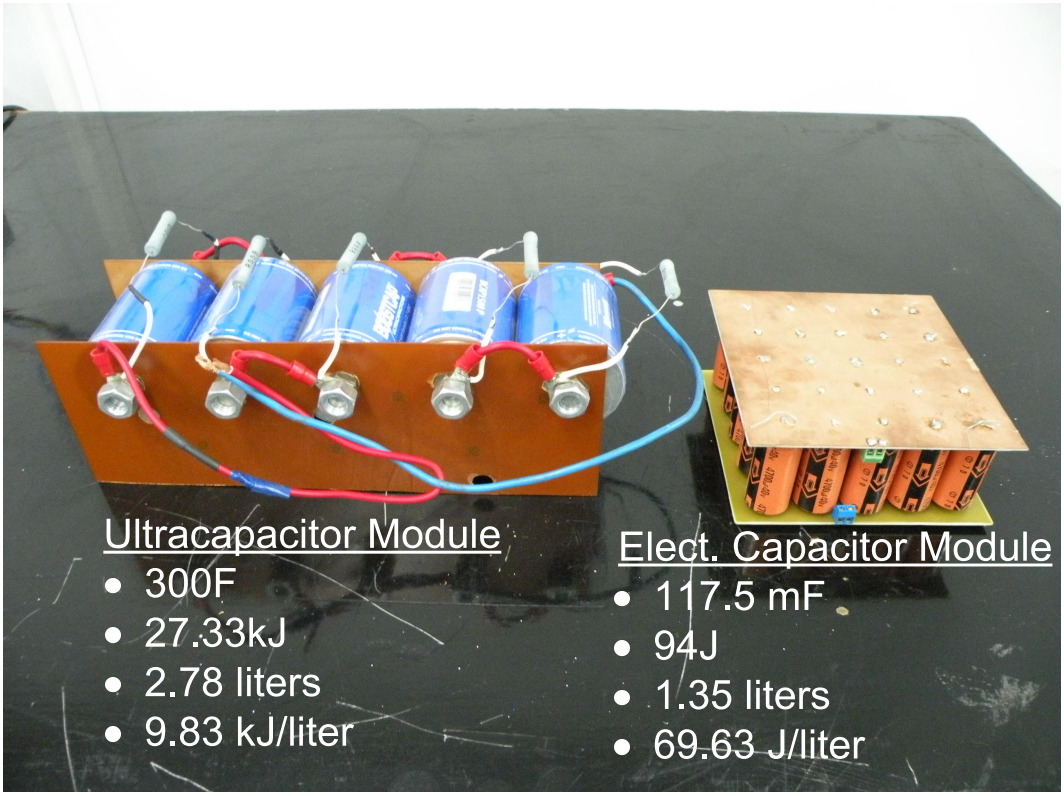


Figure 6.2 Comparison of the laboratory constructed UC and electrolytic capacitor modules.

As shown in Figure 6.2, energy density of the UC module is 140 times higher than the energy density of the electrolytic capacitor module in terms of volumetric considerations. Therefore, it could be concluded that using UCs in energy storage applications instead of electrolytic capacitors will be a rational approach.

The laboratory constructed UC test system is shown in Figure 6.3.

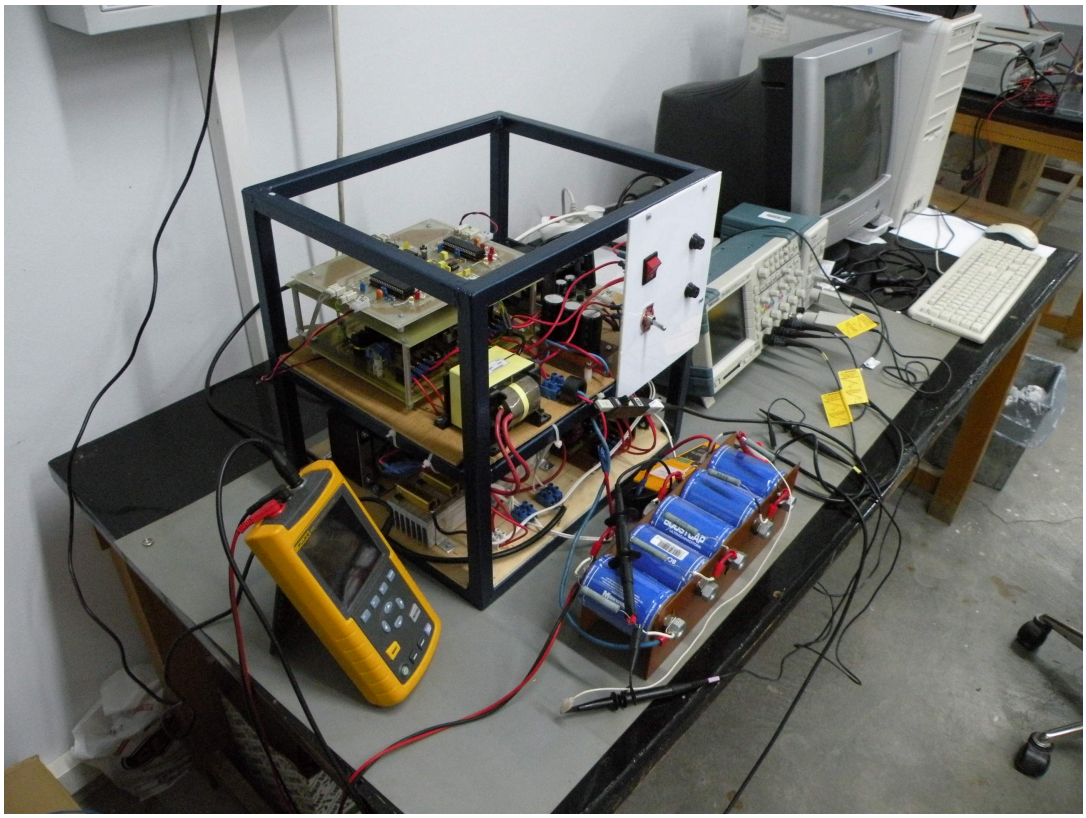


Figure 6.3 The laboratory constructed UC test system.

As shown in Figure 6.3, the laboratory constructed UC test system consists of a two-storey frame structure. Passive and large circuit elements such as transformers, an inductor board, a resistor bank, AC line terminals of the UC test system, an AC fan, and a power supply board with a 12V DC output are placed in the bottom storey, whereas a microcontroller board, a power electronics converter board, a program selection board, a DC power supply board with two 5V DC and two 12V DC outputs, an AC line smoothing inductor, an electrolytic capacitor board, a 12V DC fan, and an operating panel is placed in the upper storey.

There are three transformers in the bottom storey. The largest transformer is used to step down the AC line voltage to 24V RMS level and supply the AC inputs of the power electronics converter board. The medium sized transformer is used to step down the AC line voltage to 15V RMS and 12V RMS levels and bias the AC inputs

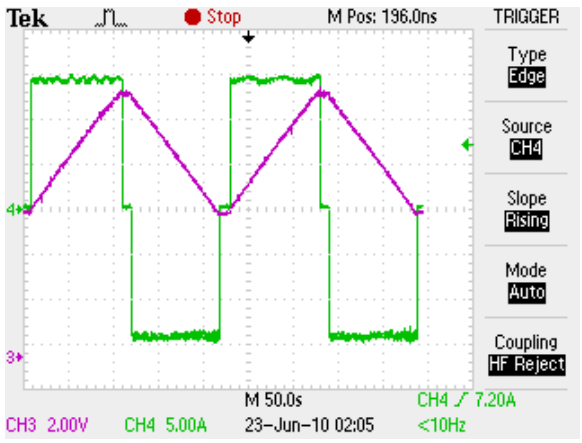
of the power supply board placed in the upper storey. The smallest transformer is used to step down the AC line to 12V RMS level and bias the AC input of the power supply board placed in the bottom storey. The function of the power supply board with a 12V DC output placed in the bottom storey is to supply the 12V DC fan placed in the upper storey. The inductor board placed in the bottom storey consists of two inductors and these inductors are used with the step-down and step-up DC-DC converters of the power electronics converter board. The resistor bank in the bottom storey is used with the DC chopper of the power electronics converter board. The cooling mechanism of the elements placed in the bottom storey is provided by an AC fan.

In the upper storey, the microcontroller board is placed over the power electronics converter board via aluminum spacers in order to utilize the storey area effectively. The schematics, PCB layouts, and photographs of the power electronics converter board and microcontroller board are included in Appendices B-D. The connection between the power electronics converter board, the inductor board, and the resistor bank is realized with direct cabling. On the other hand, the connections of the AC and UC terminals of the power electronics converter board are realized with switch and fuse configurations. The switch and fuse configurations are placed in a panel placed on the front of the upper storey. The function of the inductor placed on the front of the power electronics converter board is to smooth and limit the AC line current that is supplying the diode rectifier inputs of the power electronics converter board in order to protect the diode rectifier of the UC test system. The electrolytic capacitor board is used to reduce the ripple of the DC bus voltage of the UC charging system. The program selection board is used to select the type of the test procedure. The power supply requirements of the microcontroller board, gate drive chips, and current transducers are provided by the power supply board placed in the upper storey. The cooling of the elements in the upper storey is provided by a 12V DC fan. User manual of the UC test system is given in Appendix F.

After introducing the structural details of the constructed UC module and the UC test system, the experimental results of the UC module is given in sections 6.2 and 6.3, respectively.

6.2 Constant Current Test Results

Constant current tests are performed in order to extract the capacitance and ESR parameters of the UC module as mentioned in the introduction section. The magnitude of the applied current signal is selected as 15A. Terminal voltage variation of the UC module and the applied current waveforms for constant current tests are shown in Figure 6.4.



	Green Waveform	*Purple Waveform*
Vertical Axis :	*UC Current: 5 A/div*	*UC Voltage: 2 V/div*
Horizontal Axis :	*time: 50 s/div*	

Figure 6.4 Terminal voltage variation of the UC module and applied current for constant current tests.

As shown in Figure 6.4, the applied current remains constant at 15A level throughout the charging and discharging cycles and the terminal voltage of the UC module increases linearly in the charging cycles, whereas it decreases linearly in the discharging cycles.

This result shows that the capacitance of the UC module remains constant throughout the operation of the UC test system where the applied current is 15A and the maximum voltage of the UC module is selected as 12V which refers to 2.4V maximum voltage per UC cell within the module. In other words, in this experimental procedure the UC cells are not put in a charging and discharging cycle with full stress since the rated voltage of the UC cells are 2.7V. At this point, it will be rational to mention that the capacitance variation of the UC module remains constant with an applied current of 15A and a maximum terminal voltage of 12V.

To evaluate the capacitance value of the UC module, the variation of the UC module terminal voltage and the applied current is recorded for twenty charging and discharging cycles as shown in Figure 6.5. According to the obtained voltage and current profile of the UC module, the capacitance values are calculated by means of multiplying the magnitude of the applied current signal with the length of the time interval where the terminal voltage of the UC module varies linearly and dividing the product with the change of the UC module terminal voltage inside the chosen time interval as defined in (3.1). The calculated capacitance values are listed in Table 6.1 and Table 6.2 for different test cycles.

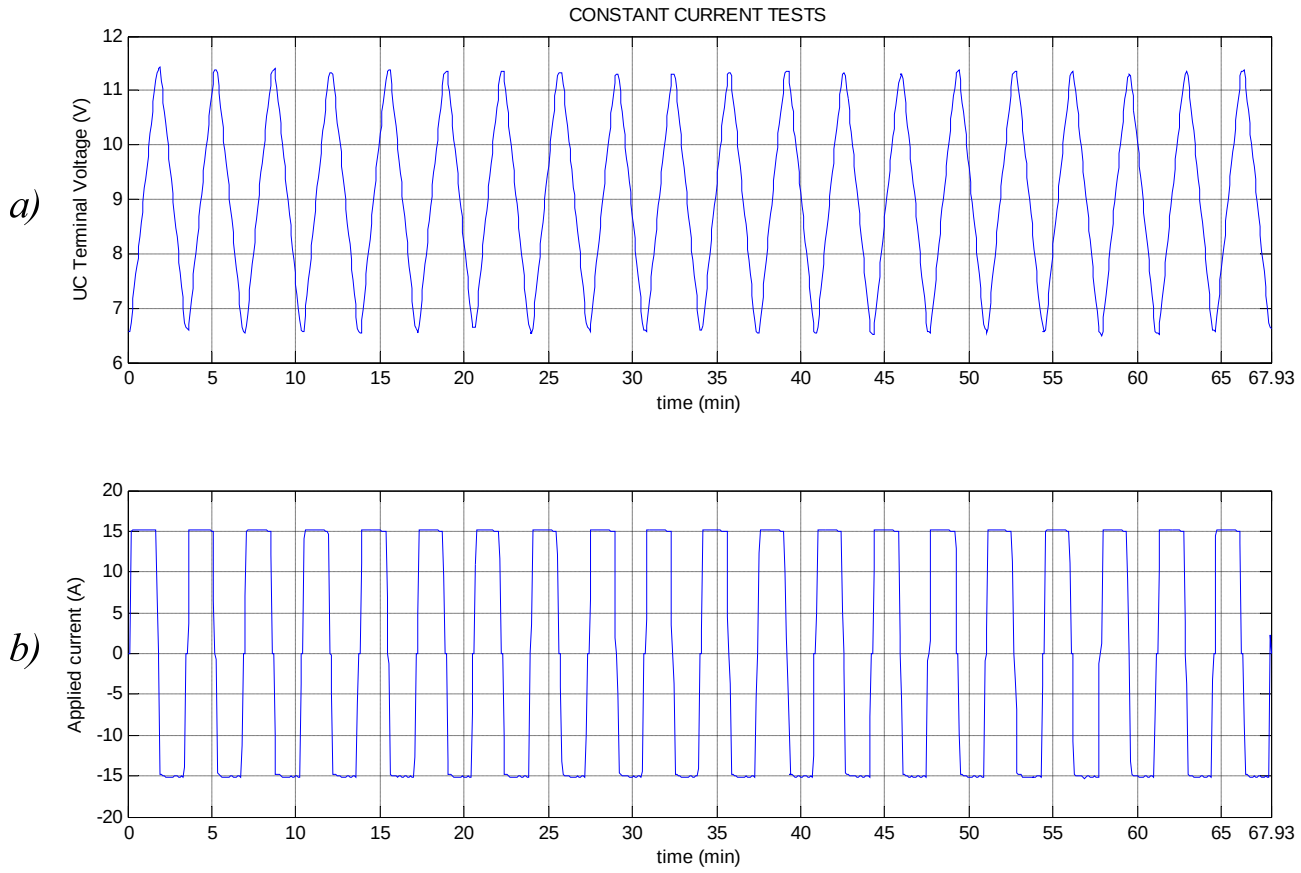


Figure 6.5 Long term variation of the UC module for constant current tests: (a) terminal voltage variation of the UC module, (b) applied current variation.

Table 6.1 Calculated capacitance values for the 1^{st} – 10^{th} charging and discharging cycles

Phase	*Cycle Number*									
	1	2	3	4	5	6	7	8	9	10
$C_{charging}$ *(F)*	300.55	287.46	287.86	288.21	286.58	287.9	285.82	287.17	286.5	287.17
$C_{disharging}$ *(F)*	285.15	284.55	283.72	283.57	283.26	286.1	282.78	285.21	280.98	281.7

Table 6.2 Calculated capacitance values for the 11^{th} – 20^{th} charging and discharging cycles

Phase	*Cycle Number*									
	11	12	13	14	15	16	17	18	19	20
$C_{charging}$ *(F)*	286.48	286.55	287.21	287.16	286.55	285.25	285.85	286.61	285.92	284.67
$C_{disharging}$ *(F)*	282.02	283.83	281.14	281.56	281.97	283.98	281.73	286.76	282.45	281.18

According to Table 6.1 and Table 6.2, it is seen that the capacitance values for different test cycles show small variations. Therefore, it could be concluded that taking the average of the capacitance values of individual test cycles for charging and discharging phases separately can be viewed as a correct approach. A comparison of the average capacitance value of the charging and discharging phases together with the datasheet value for the capacitance value of the UC module is shown in Table 6.3.

Table 6.3 Comparison of the capacitance values of the UC module

Datasheet Value(F)	*Charging Phase*		*Discharging Phase*	
	Average (F)	*Deviation (%)*	*Average (F)*	*Deviation (%)*
300	287.37	- 4.21	283.18	- 5.60

As shown in Table 6.3, the average capacitance values for the charging and discharging phases are lower than the datasheet value. The capacitance deviation value from the rated capacitance is given in Maxwell Boostcap series UCs datasheet as +20 % and -5 % [3]. The calculated capacitance deviations, -4.21 % for the charging phase and -5.60 % for the discharging phase, are very near to the negative deviation limit for the capacitance parameter given in [3].

On the other hand, it is also observed that the capacitance value obtained for the charging phase is higher than the capacitance value obtained for the discharging phase. The difference between the capacitance values for the charging and discharging phases could be explained by considering the equivalent circuit model of the UC module as shown in Figure 6.6.

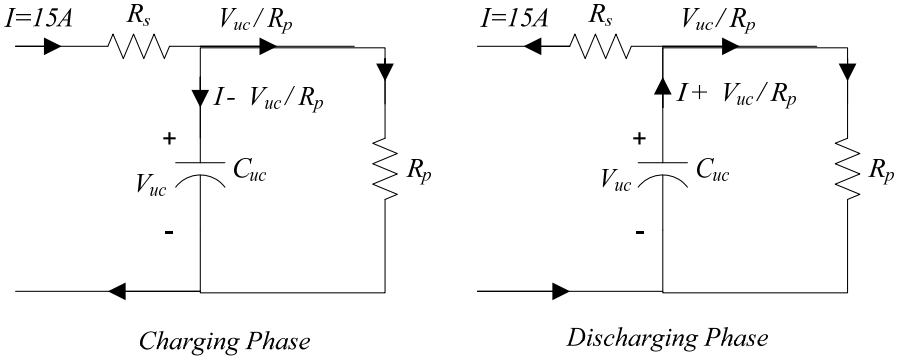
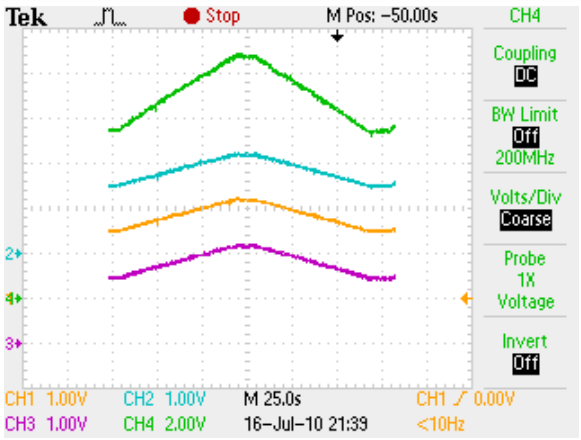


Figure 6.6 Equivalent circuit model of the UC module for the charging and discharging phases.

As shown in Figure 6.6, the UC module is charged with a constant charging current of 15A. It is seen that some of the current is diverted to the parallel resistor branch (R_p). Therefore, the actual charging current on the capacitor branch is lower than 15A. However, during the capacitance calculations, the current on the parallel resistor branch is not taken into consideration. For this reason, the capacitance value obtained by means of averaging the capacitance values of different charging cycles is higher than the actual capacitance value of the UC module. When the discharging phase is considered, it is seen that the actual discharging current is higher than the 15A reference current since the parallel resistor branch diverts current. Therefore, the capacitance value obtained by means of averaging the discharging cycles is lower than the actual capacitance value.

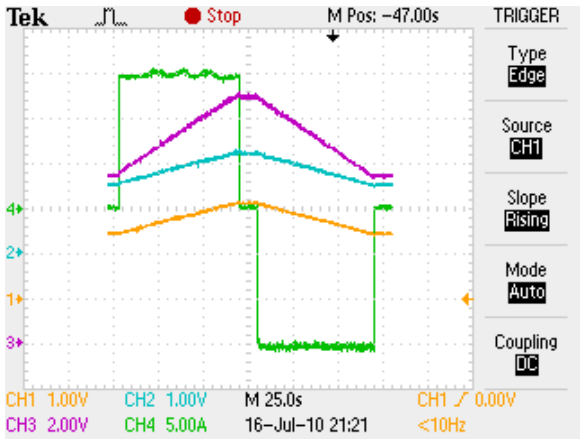
After considering the capacitance variation of the UC module for the charging and discharging phases, the terminal voltage variations of the individual UC cells inside the UC module are also investigated in order to see the distribution of the UC module terminal voltage between the individual UC cells. Experimental results for the terminal voltage variations of the first, second and third UC cells within the UC module are shown in Figure 6.7 and the terminal voltage variations of the fourth and fifth UC cells within the UC module are shown in Figure 6.8.



Vertical Axis:
Greeen Waveform: UC module terminal voltage (2V/div)
Orange Waveform: 1st UC cell terminal voltage (1V/div)
Blue Waveform : 2nd UC cell terminal voltage (1V/div)
Purple Waveform: 3rd UC cell terminal voltage (1V/div)

Horizontal Axis: time (25s/div)

Figure 6.7 Terminal voltage variations of the first, second and third UC cells within the UC module under constant current tests.



Vertical Axis:
Greeen Waveform: applied current (5A/div)
Purple Waveform: UC module terminal voltage (2V/div)
Orange Waveform: 4th UC cell terminal voltage (1V/div)
Blue Waveform: 5th UC cell terminal voltage (1V/div)

Horizontal Axis: time (25s/div)

Figure 6.8 Terminal voltage variations of the fourth and fifth UC cells within the UC module under constant current tests.

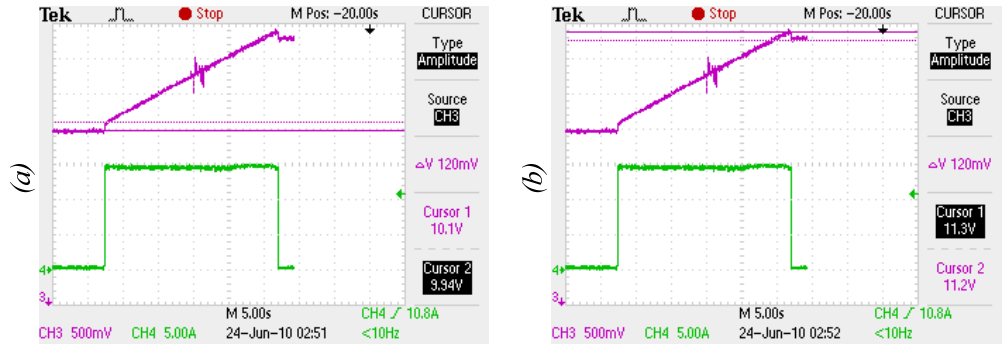
When the terminal voltage variations shown in Figure 6.7 and Figure 6.8 are investigated, a balanced UC module terminal voltage distribution is observed. The terminal voltage measurements of the UC module and individual UC cells at the end of the charging and discharging phases of the UC test system are summarized in Table 6.4.

Table 6.4 Terminal voltage measurements of the UC module and individual UC cells

Terminal Voltage Measurements (V)						
At the end of the	*1st UC cell*	*2nd UC cell*	*3rd UC cell*	*4th UC cell*	*5th UC cell*	*UC module*
Charging phase	2.24	2.24	2.24	2.20	2.28	11.2
Discharging phase	1.44	1.44	1.44	1.40	1.48	7.2

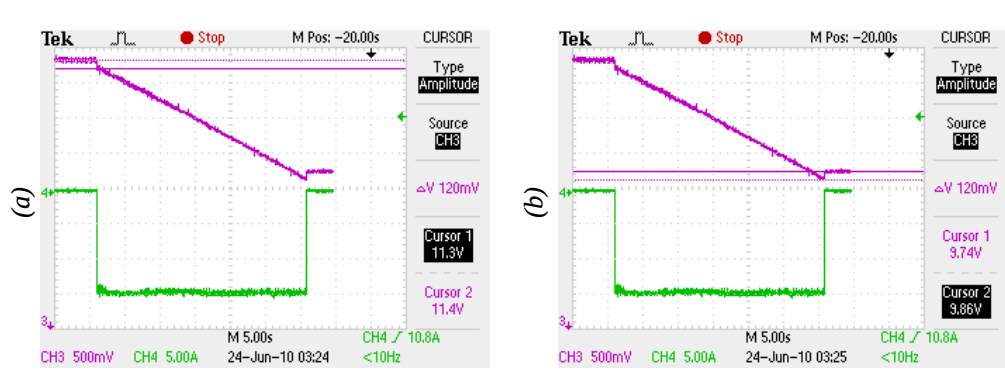
According to the results presented in Table 6.4, it is seen that terminal voltage of the UC module is distributed between the individual UC cells in a balanced manner. Therefore, it could be concluded that the passive resistor balancing structure is sufficient for this application.

After considering the long term variation of the constant current tests, short term variation is also investigated in order to evaluate the ESR parameter of the UC module. For this reason, immediate rise and fall behaviour of the UC module terminal voltage is captured for the charging and discharging phases separately and the captured waveforms are shown in Figure 6.9 and Figure 6.10, respectively.



	Green Waveform	*Purple Waveform*
Vertical Axis :	*UC Current: 5 A/div*	*UC Voltage: 500 mV/div*
Horizontal Axis :	*time: 5 s/div*	

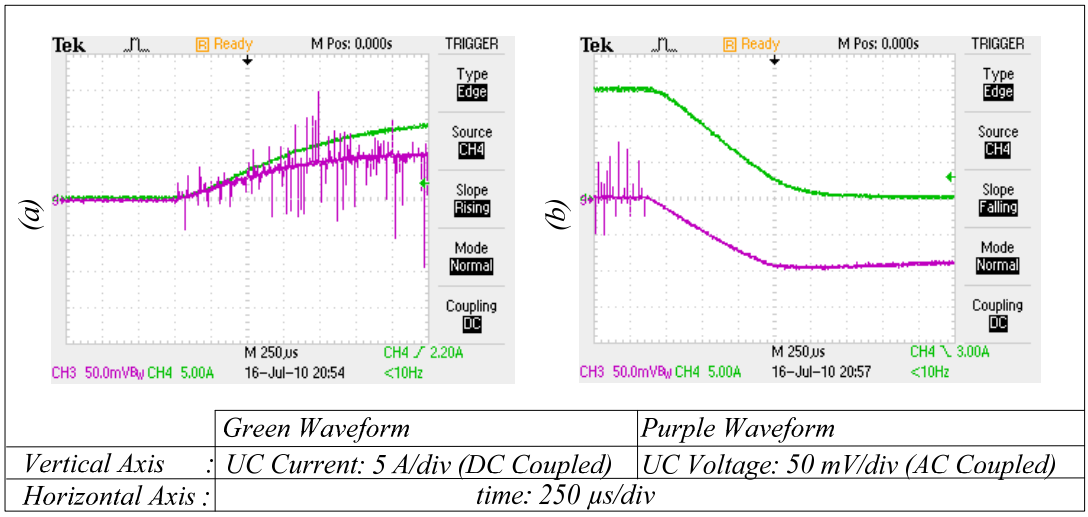
Figure 6.9 Immediate characteristics of the UC module terminal voltage for the charging phase: (a) measurement of the increase of the UC module terminal voltage with purple colored voltage cursors at the beginning of the charging phase, (b) measurement of the decrease of the UC module terminal voltage with purple colored voltage cursors at the end of the charging phase.



	Green Waveform	*Purple Waveform*
Vertical Axis :	*UC Current: 5 A/div*	*UC Voltage: 500 mV/div*
Horizontal Axis :	*time: 5 s/div*	

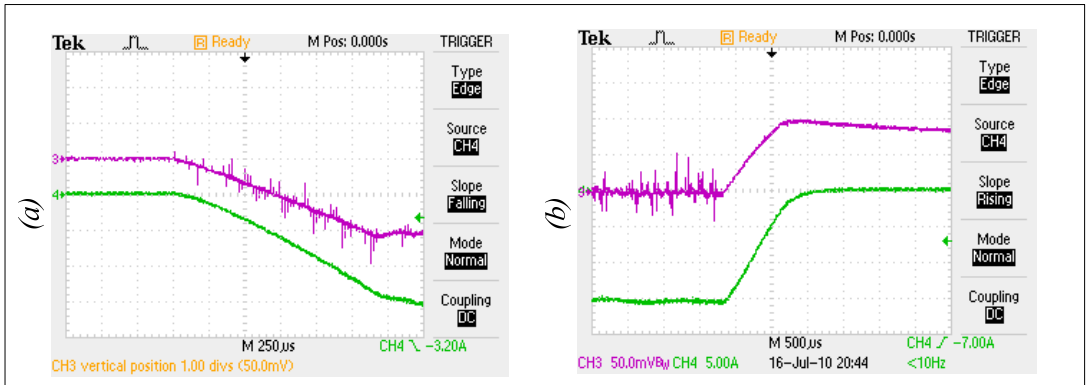
Figure 6.10 Immediate characteristics of the UC module terminal voltage for the discharging phase: (a) measurement of the decrease of the UC module terminal voltage with purple colored voltage cursors at the beginning of the discharging phase, (b) measurement of the increase of the UC module terminal voltage with purple colored voltage cursors at the end of the discharging phase.

To see the dynamics of the UC module terminal voltage in the build-up and fall cases of the applied current, the UC module terminal voltage is measured in AC coupling mode and the variations are shown in Figure 6.11 and Figure 6.12.



	Green Waveform	*Purple Waveform*
Vertical Axis :	*UC Current: 5 A/div (DC Coupled)*	*UC Voltage: 50 mV/div (AC Coupled)*
Horizontal Axis :	*time: 250 µs/div*	

Figure 6.11 Immediate characteristics of the UC module terminal voltage for the charging phase: (a) AC coupled UC module terminal voltage at the beginning of the charging phase, (b) AC coupled UC module terminal voltage at the end of the charging phase.



	Green Waveform	*Purple Waveform*
Vertical Axis :	*UC Current: 5 A/div (DC Coupled)*	*UC Voltage: 50 mV/div (AC Coupled)*
Horizontal Axis :	*time: 250 µs/div*	

Figure 6.12 Immediate characteristics of the UC module terminal voltage for the discharging phase: (a) AC coupled UC module terminal voltage at the beginning of the discharging phase, (b) AC coupled UC module terminal voltage at the end of the discharging phase.

As shown in Figures 6.9-6.12, the terminal voltage of the UC module shows an immediate rise or fall behaviour when the charging or discharging current is applied or terminated. According to (3.2), ESR of the UC module is calculated by means of dividing the voltage difference occurred when the charging and discharging phases are initiated or stopped by the magnitude of the current waveform. The ESR measurements according to Figures 6.9-6.12 are listed in Table 6.5.

Table 6.5 ESR measurements

Measurements		*Charging Phase*		*Discharging Phase*	
		Beginning	*End*	*Beginning*	*End*
UC Module Terminal Voltage (DC coupled)	ΔV *(mV)*	120	120	120	120
	ESR (mΩ)	8	8	8	8
UC Module Terminal Voltage (AC coupled)	ΔV *(mV)*	70	100	100	100
	ESR (mΩ)	7	6.67	6.67	6.67

According to the experimental results shown in Figures 6.9-6.12 and summarized in Table 6.5, it is seen that the UC module terminal voltage shows a build-up or fall characteristics when the current is applied or terminated. The ESR values obtained from the DC coupled and AC coupled measurements are very near to each other and it is seen that the immediate voltage rise and fall events have resistive characteristics.

Datasheet value for the ESR of the UC module is 2.35 mΩ. It is seen that the ESR value obtained from the experimental results are higher than the datasheet value. The reason for this result is due to the extra contact resistance of the constructed UC module since the connections between the individual UC cells inside the module results in extra resistance value.

6.3 Constant Power Test Results

In Chapter 5, digital current regulator mechanisms are described for the charging and discharging operations of UCs and by utilizing the described current regulator mechanisms constant current tests of a UC module are realized. Predetermined current profiles could also be applied to the UC under test with the implemented current regulators. The only requirement is to define the digital current references and their corresponding time interval values. With this approach, the digital current reference of the current regulators is updated after the corresponding time interval is passed. In this sense, the current regulator mechanisms are utilized to implement the constant power tests of the constructed UC module. 100W reference power level is selected for constant power tests and the digital current reference value is updated at each time interval when 0.2V voltage change occurs in the terminal voltage of the UC module.

Digital current profile determination process for constant power tests is described in (6.1)-(6.4). At first, the analog value of the current reference (I_{ref}) is calculated by dividing the reference power (P_{ref}) with the terminal voltage of the UC module (V_{uc}) as given in (6.1).

$$I_{ref} = \frac{P_{ref}}{V_{uc}} \tag{6.1}$$

The digital equivalent of the analog current reference (i_{ref}) value is calculated by considering the current measurement expression shown in Table 5.6 and the calculation is given in (6.2).

$$i_{ref} = \frac{2.5 + I_{ref} \times 0.075}{5} \times 2^{10} \tag{6.2}$$

The time interval value (Δt) of the corresponding analog current reference (I_{ref}) is calculated by considering a 0.2V change in the terminal voltage of the UC module.

Time interval calculation is a modification of (2.7) and 300F datasheet capacitance value is used in this calculation as given in (6.3).

$$\Delta t = C \times \frac{\Delta V}{I} = 300 \times \frac{0.2}{I} = \frac{600}{I} \tag{6.3}$$

The time interval values of the corresponding current references are programmed inside the microcontrollers as timer count values (T_{count}) by considering the interrupt period ($T_{interrupt}$) which is selected as 20 μs for this application. The timer count calculation is given in (6.4).

$$T_{count} = \frac{\Delta t}{T_{interrupt}} = \frac{\Delta t}{20 \times 10^{-6}} = \Delta t \times 50000 \tag{6.4}$$

By utilizing (6.1)-(6.4), the digital current references (i_{ref}) and their corresponding timer count values (T_{count}) are calculated for the charging operation case. The up and down limits of the UC module terminal voltage (v_{uc_up} , v_{uc_down}) are selected as 12V and 6.60V, respectively. The calculated values are listed in Table 6.6. When Table 6.6 is investigated, it is seen that the timer count value is increased by 6000 for each current reference.

The microcontroller implementation of the constant power test procedure for the charging phase of the UC test system is shown in Figure 6.13. By utilizing the current reference values listed in Table 6.6, a look-up table (LUT) is constructed inside the microcontroller and current reference values are selected from the LUT by considering the corresponding timer count values.

Table 6.6 Digital current references and their corresponding timer count values for 100W constant power tests

V_{uc}(V)	I_{ref} (A)	i_{ref}	Δt (s)	T_{count}
6.60	15.00	745	4.00	200000
6.80	14.56	739	4.12	206.000
7.00	14.14	732	4.24	212000
7.20	13.75	725	4.36	218000
7.40	13.38	720	4.48	224000
7.60	13.03	714	4.60	230000
7.80	12.69	709	4.73	236000
8.00	12.38	704	4.85	242000
8.20	12.07	699	4.97	248000
8.40	11.79	694	5.09	254000
8.60	11.51	689	5.21	260000
8.80	11.25	685	5.33	266000
9.00	11.00	681	5.45	272000
9.20	10.76	677	5.58	278000
9.40	10.53	674	5.70	284000
9.60	10.31	670	5.82	290000
9.80	10.10	667	5.94	296000
10.00	9.90	664	6.06	302000
10.20	9.71	661	6.18	308000
10.40	9.52	658	6.30	314000
10.60	9.34	655	6.42	320000
10.80	9.17	653	6.54	326000
11.00	9.00	650	6.67	332000
11.20	8.84	648	6.79	338000
11.40	8.68	645	6.91	344000
11.60	8.53	643	7.03	350000
11.80	8.39	641	7.15	356000
12.00	8.25	639	7.27	362000

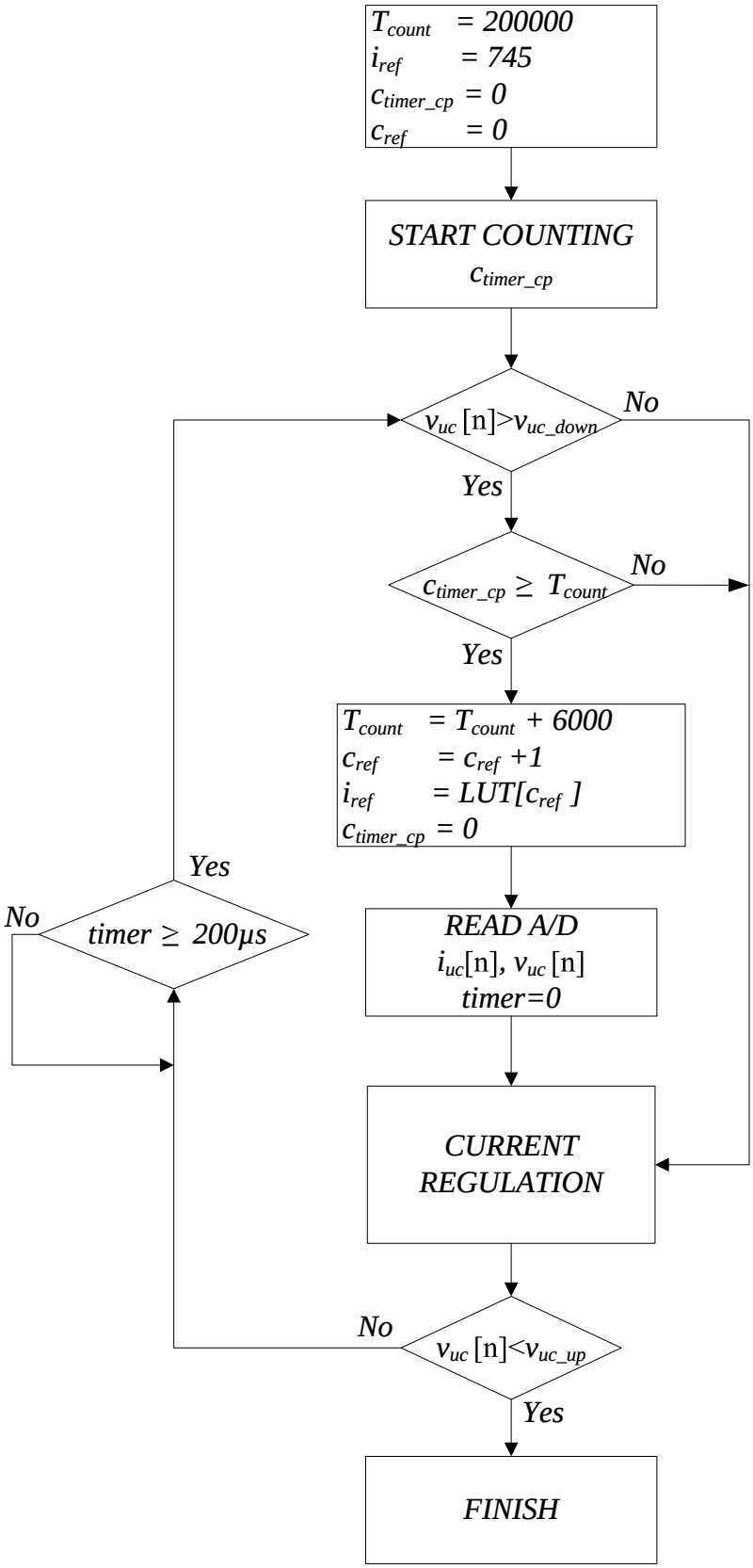
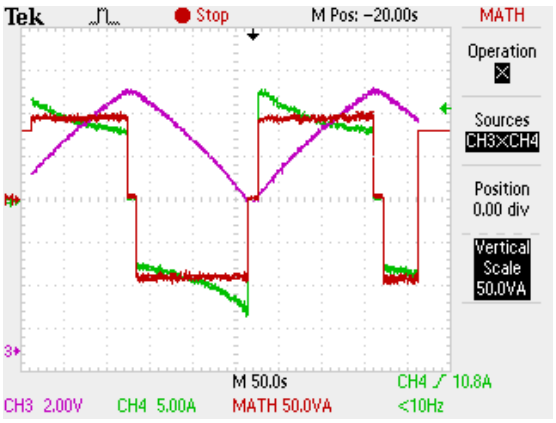


Figure 6.13 Flowchart of the microcontroller implementation of the constant power test procedure for the charging phase of the UC test system.

In the procedure shown in Figure 6.13, the first step is the set of initial values to the timer count (T_{count}), current reference (i_{ref}), current profile timer counter (c_{timer_cp}), and LUT address parameters (c_{ref}). At this point, it is important to express the difference between the T_{count} and c_{timer_cp} parameters. T_{count} refers to the time interval value of the corresponding current reference, whereas c_{timer_cp} refers to the passed time with the selected current reference. After the initial values are set to the constant power test procedure parameters, c_{timer_cp} is activated. In the next step, the terminal voltage of the UC module (V_{uc}) is compared with the down limit (V_{uc_down}) of the test procedure which is selected as 6.60V for this application. Following the comparison, if V_{uc} is lower than V_{uc_down}, then the charging operation will be realized with constant current for the initial current reference value. On the other hand, if V_{uc} is higher than V_{uc_down}, then the constant power test procedure will be applied to the UC module. Current regulation will be performed for the updated current reference values by considering the corresponding T_{count} values.

In this section, microcontroller implementation of constant power test procedure is described by considering the charging phase of the UC test system. The implementation for the discharging phase is very similar to the implementation for the charging phase. The only difference is to consider the V_{uc} values from the up limit ($v_{uc\_up,}$) to the down limit (v_{uc_down}) and calculate i_{ref} and T_{count} values accordingly.

To observe the constant power charging and discharging characteristics of UCs, the constructed UC module is put in a constant power charging and discharging process with the implemented test procedure algorithm. 100W level is selected as the reference power during the constant power tests. The variation of the UC module terminal voltage, applied current, and the power waveforms are shown in Figure 6.14.



	Green Waveform	*Purple Waveform*	*Red Waveform*
Vertical Axis :	*UC Current: 5 A/div*	*UC Voltage : 2 V/div*	*Power : 50 VA/div*
Horizontal Axis :	*time: 50 s/div*		

Figure 6.14 Variation of the UC module terminal voltage, applied current, and power for constant power tests.

As shown in Figure 6.14, the power remains constant at 100W level for both charging and discharging cycles. The variation of the UC module terminal voltage and applied current are also as expected. The long term data of the constant power tests is also recorded and the test results are shown in Figure 6.15. By means of the obtained power profile, round trip cycle efficiency (h_{rt}) of the UC module is calculated for different test cycles. As described in (3.3), round trip cycle efficiency (h_{rt}) is defined as the ratio of the energy expressions in the discharging and charging phases of a constant power test cycle. The calculated round trip cycle efficiency values are listed in Table 6.7 and in Table 6.8.

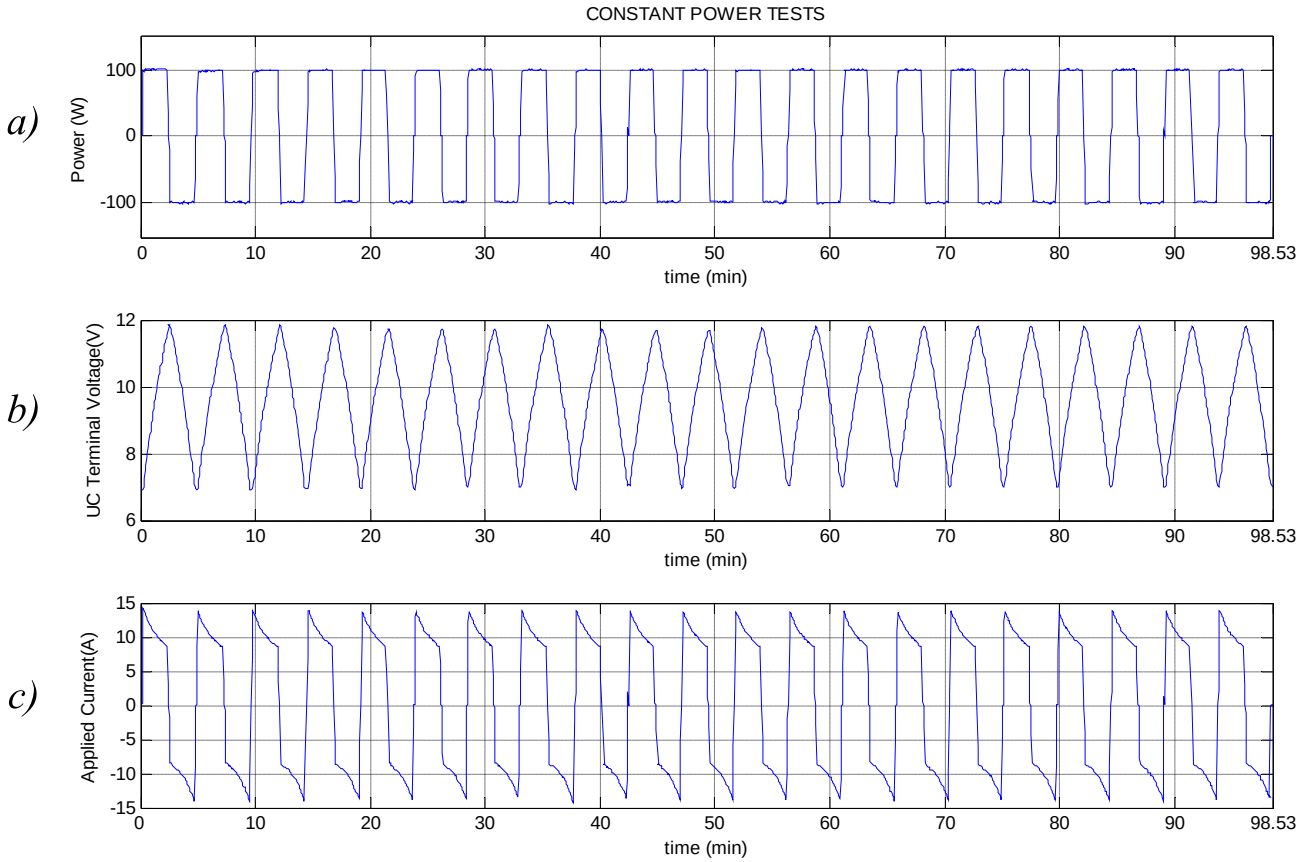


Figure 6.15 Long term variation of the UC module for constant power tests: (a) power variation, (b) terminal voltage variation of the UC module, (c) applied current variation.

Table 6.7 Round trip cycle efficiency calculations for 1st -11th cycles

	Cycle Number										
	1	2	3	4	5	6	7	8	9	10	11
h_{rt}	0,9801	0,9820	0,9785	0,9618	0,9951	0,9770	0,9775	0,9946	0,9749	0,9824	0,9869

Table 6.8 Round trip cycle efficiency calculations for 12th -21st cycles

	Cycle Number									
	12	13	14	15	16	17	18	19	20	21
h_{rt}	0,9942	0,9838	0,9860	0,9867	0,9831	0,9799	0,9870	0,9797	0,9832	0,9879

According to the constant power test results presented in Tables 6.7-6.8, it is seen that the average of the round trip cycle efficiency values is 0.9829 for 100W level. This result is consistent with the efficiency parameter listed in Table 2.5 in Chapter 2 and shows that UCs could be utilized in power cycling applications that require high efficiency. On the other hand, it could also be concluded that the power cycling tests should be repeated for higher reference power levels in order to see the effect of power level on the round trip cycle efficiency value of a UC module.

6.4 Conclusion

In this chapter, constant current and constant power test results of a UC module are presented. It is seen that the experimental results are consistent with the theory of UCs. However, some differences between the datasheet parameters and the calculated values are also observed.

The capacitance and ESR values are the parameters of a UC that determine the energy storage and maximum power capability, respectively. According to the experimental results, it is observed that the datasheet values and experimental results for the capacitance and ESR of a UC module show differences. The calculated capacitance deviations are -4.21 % for the charging phase and -5.60 % for the discharging phase which are very near to the negative deviation limit for the capacitance parameter given in product datasheet [3]. According the ESR measurements, it is seen that the measured ESR values are about three times higher than the datasheet ESR value due to the extra contact resistance inside the UC module. According to these facts, it could be concluded that the UC modules should be evaluated in terms of capacitance and ESR parameters before integrating them to energy storage applications.

According to the constant power test results, it is seen that the average value of the round trip cycle efficiency is 0.9829. This result shows that, UCs could be utilized in power cycling applications that require high efficiency. On the other hand, it could

also be concluded that the power cycling tests should be repeated for higher reference power levels in order to see the effect of power level on the round trip cycle efficiency value of a UC module.

In this study, experimental performance evaluation of a UC module is realized with 15A reference current and 100W reference power level, considering the capability of power electronics converters and the terminal voltage of an individual UC cell within the UC module is put below the rated voltage level during the experiments. The number of test cycles performed during the experiments is above 500 cycles. With the mentioned conditions the terminal electrical characteristics of the UC module show linear behaviour in terms of capacitance and ESR measurements. In addition, round trip cycle efficiency values did not show a decreasing behaviour after certain number of constant power test cycles. However, it is very important to put UCs under full voltage stress and collect data under this condition. In this study, full stress conditions could not be applied since there are no extra UC cells that can be used in the case of a failure condition. Further, thermal and aging behaviour of the UCs could not be investigated due to the lack of extra UC cells in this study.

CHAPTER 7

CONCLUSION

UCs are capacitive energy storage devices with high capacitance, low ESR, and low rated voltage values. For a single UC cell, the capacitance values are above 1000F, the ESR values are below 1mΩ, and the voltage ratings are at 2.5V level [3-6]. The energy density of UCs is lower than batteries. However, the maximum power capability of UCs is higher than batteries. When UCs are compared with conventional capacitors, it is seen that the energy density of these relatively new storage devices are higher than conventional capacitors. However, the maximum power capability of conventional capacitors is higher than UCs. According to the mentioned facts, it is obvious that UCs are energy storage devices that lie between conventional capacitors and batteries [8], [10], [14].

In the scope of the thesis study, it has been aimed to evaluate the characteristics of UCs experimentally. The characteristics of UCs can not be measured with standard measurement devices like LCR meters since the signals applied by an LCR meter will not be adequate to create a measurable change in the terminal voltage of the UC under test that the measurement mechanism of LCR meters could sense. Therefore, a UC test system capable of performing the charging and discharging operations of UCs is implemented in order to apply large DC current signals to the UC under test. The implemented UC test system is based on power electronics converters. To investigate the performance of the UC test system and evaluate the terminal electrical behaviour of UCs, a UC module composed of five serially connected UC cells is constructed. The equivalent capacitance and the ESR value of the constructed UC

module are 300F and 2.35 mΩ, respectively according to the product datasheet information [3].

With the implemented test system the UC under test is charged by a step-down DC-DC converter supplied by the AC utility grid followed by a step-down transformer, a diode bridge, and a large valued filter capacitor configuration. On the other hand, the energy stored in UCs as a result of the charging operation is discharged to a chopper controlled resistor by means of a step-up DC-DC converter. The reason for choosing a step-down DC-DC converter for the charging operation and choosing a step-up DC-DC converter for the discharging operation is to provide continous charging and discharging current profiles to the UC under test. A DC chopper structure is utilized at the output of the step-up DC-DC converter in order to maintain the output voltage of the step-up DC-DC converter constant which simplifies the control process of the UC discharging structure. Current mode control structures are utilized for the control of the step-down and step-up DC-DC converters in order to apply predetermined current profiles to the UC under test. The implemented power electronics converter structure is capable of performing constant current tests of the UC module at 15A and constant power tests of the UC module at 100W level, where the terminal voltage of the UC module is put below 12V.

A PI current regulator mechanism is utilized for the control of the UC charging structure. For a current command of 15A, the rise time, fall time, overshoot, and steady-state ripple value of the applied charging current are observed as 2.5 ms, 1.81 ms, 0 %, and 0.5A, respectively. The observed rise and fall time value of the applied charging current show that the bandwidth of the charging system is at low levels. According to the zero overshoot and low steady-state current ripple value of the applied charging current, it can be concluded that the dynamic and steady-state performance of the PI current regulator structure is sufficient for the UC charging application.

The performance of PI and hysteresis type current regulators is investigated for the control of the step-up DC-DC converter and a hysteresis type voltage regulator is

utilized for the DC chopper of the UC discharging structure. With the PI current regulator structure, the rise time, fall time, overshoot, and steady-state ripple value of the applied discharging current are observed as 1.36 ms, 0.78 ms, 33 %, and 0.4 A, respectively for a current command of 15A. On the other hand, the rise time, fall time, overshoot, and steady-state ripple value of the applied discharging current are observed as 1.18 ms, 0.74 ms, 0 %, and 1.2 A, respectively for a current command of 15A with the hysteresis current regulator structure. The observed rise and fall time value of the applied discharging current show that the bandwidth of the discharging system is at low levels which is also observed for the UC charging structure. When the build-up, fall, and overshoot characteristics of the UC discharging system are considered together, it is seen that the dynamic performance of the hysteresis current regulator is better than the PI current regulator. On the other hand, the steady-state current ripple values observed for the hysteresis current regulator case are higher than the current ripple value observed for the PI current regulator case. Therefore, it could be concluded that the steady-state performance of the PI current regulator is better than the hysteresis current regulator. DC chopper is utilized in parallel with the step-up DC-DC converter during the discharging process. The observed output voltage ripple at the output of the step-up DC-DC converter is 1.5V for both of the current regulator cases. It is seen that, a voltage ripple value of 1.5V is sufficient for the operation of the UC discharging system.

When the performance of PI and hysteresis current regulators is considered together, it is seen that the dynamic performance of the hysteresis regulator is better than the PI regulator, whereas the steady-state performance of the PI regulator is better than the hysteresis regulator. Therefore, a hybrid control mechanism that uses the advantages of both regulator types in terms of dynamic and steady-state considerations is proposed. By utilizing the proposed control mechanism, the overshoot of the discharging current is made zero as in the case of the hysteresis regulator and the steady-state discharging current ripple is reduced to the levels observed for the PI regulator case.

By utilizing the implemented UC test system, constant current and constant power tests of the constructed UC module are performed. According to the constant current

test results, the average capacitance value of the UC module is calculated as 287.37F and 283.18F for the charging and discharging phases, respectively. It is seen that the calculated capacitance values are lower than the datasheet capacitance value which is 300F and the capacitance deviations are calculated as -4.21 % for the charging phase and -5.60% for the discharging phase. The calculated capacitance deviations are near to the negative capacitance deviation value of -5 % given in the product datasheet [3]. On the other hand, the capacitance value obtained for the charging phase is higher than the capacitance value obtained for the discharging phase due to the effect of leakage current inside the UC module.

After the capacitance observations, terminal voltage distribution of the UC module is investigated. It is seen that for a 11.2V UC module terminal voltage level, the individual UC cell terminal voltages are at 2.24V level, whereas for a 7.2V UC module terminal voltage level, the individual UC cell terminal voltages are at 1.44V level. According to this result it is seen that the passive resistor voltage balancing structure is sufficient for this application.

The ESR parameter of the UC module is also investigated during constant current tests. The observed ESR value for the UC module is at 6-8 mΩ level which is higher than the datasheet value of 2.35 mΩ. The increased value for the ESR parameter is resulted from the extra contact resistance due to connections inside the constructed UC module. Since the capacitance and ESR parameters obtained from the experimental results are different from the datasheet values, it could be concluded that testing the capacitance and ESR values of a UC module before using it in an energy storage application could be viewed as a correct approach.

After the constant current test results, constant power test results of the UC module are also presented. It is observed that the average round trip cycle efficiency value of the UC module is at 98 % level for a reference power level of 100W. Therefore, it could be concluded that UCs could be utilized in power cycling applications that require high efficiency.

In this study, 15A reference current and 100W reference power are used for the constant current and constant power tests, respectively considering the capability of power electronics converters. The UC cells are not put into a full voltage stress during the experimental procedures due to the lack of extra UC cells in this study. With these conditions, the measured capacitance and ESR variations show linear characteristic and no second order effects are observed during the study. The experimental procedures should be repeated for increased current and power levels and the devices should be put in full stress in order to observe if the UCs show different terminal electric behaviour at high current and full stress conditions. Furthermore, with this approach thermal and aging characterization of UCs could be performed.

When the future work that could be conducted for improving the implemented UC test system is investigated, it is seen that the current rating of the UC test system should be increased in order to observe the terminal electric behaviour of the UCs for higher current levels and to investigate the thermal and aging behaviour of UCs. Two modifications are necessary in order to improve the current rating of the UC test system. The first modification is paralleling the MOSFETs of the power electronics converter structure. This modification is valid, since the on state resistance of a MOSFET increases as the temperature of the device increases and the current distributes on the paralleled MOSFETs accordingly. The second modification should be performed on the Hall Effect current transducers. In the implemented UC test system, 25A configuration is chosen for the Hall Effect current transducers since the current rating of the UC test system is chosen as 15A. However, 50A or 75A configurations should be selected if it is decided to increase the current rating of the UC test system.

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APPENDIX A

DATASHEET OF THE BOOSTCAP ULTRACAPACITORS

Series: MC Power
Round, Terminal Type

Ultra low internal resistance
Highest power performance available
Lowest RC time constant

> Features:

» 2.7 Volt Operating Voltage
» Ultra low internal resistance
» Over 1 million duty cycles
» Highest power performance available
» Lowest RC time constant
» Threaded terminal or weldable post versions

> Applications:

» Hybrid drive trains
» Automotive subsystems
» Transportation
» Rail system power

> Overview:

The Power-type ultracapacitor product line gives customers in the automotive and transportation sector a much wider range of choices to meet their energy storage and power delivery requirements.

The cells are specifically engineered for hybrid vehicle drive trains, automotive subsystems and other heavy duty applications that require the lowest equivalent series resistance (ESR) and highest efficiency available.

In addition to meeting or exceeding demanding automotive and transportation application requirements for both watt-hours of energy storage and watts of power delivery per kilogram, all of these products will perform reliably for more than one million discharge-recharge cycles.

The proprietary architecture and material science on which BOOSTCAP® products are based enable continued leadership in controlling costs, flexibility in product offerings and allow application specific performance tailoring. The cells operate at 2.7 volts, enabling them to store more energy and deliver more power per unit volume than any other commercially available ultracapacitor products.

> MC Power Series Specifications:

Item	Performance	
Operating Temperature Range	-40 °C to +65 °C	
Storage Temperature Range	-40 °C to +70 °C	
Rated Voltage	2.7 V DC	
Capacitance Tolerance	+20% / -5%	
Resistance Tolerance	Max.	
Temperature Characteristics	Capacitance Change	Within ± 5% of initial measured value at 25 °C (at -40 °C)
	Internal Resistance	Within 150% of initial measured value at 25 °C (at -40 °C)
Endurance	After 1500 hours application of rated voltage at 65 °C	
	Capacitance Change	Within 20% of initial specified value
	Internal Resistance	Within 60% of initial specified value
Shelf Life	After 1500 hours storage at 65 °C without load shall meet specification for endurance	
Life Test	After 10 years at rated voltage and 25 °C	
	Capacitance Change	Within 30% of initial specified value
	Internal Resistance	Within 150% of initial specified value
Cycle Test	Capacitors cycled between specified voltage and half rated voltage under constant current at 25 °C (1 million)	
	Capacitance Change	Within 30% of initial specified value
	Internal Resistance	Within 150% of initial specified value

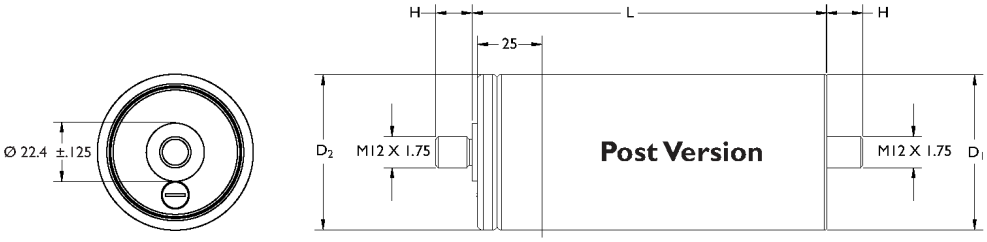
> MC Power Product Specifications:

Part Number	Capacitance (F)	ESR, DC (mohm)	ESR, 1khz (mohm)	Ic (mA)
BCAP0650 P270	650	0.80	0.60	1.5
BCAP1200 P270	1200	0.58	0.44	2.7
BCAP1500 P270	1500	0.47	0.35	3.0
BCAP2000 P270	2000	0.35	0.26	4.2
BCAP3000 P270	3000	0.29	0.24	5.2

> MC Power Product Properties:

Maxwell Part No.	Rth (C/W)	Isc (A)	Emax (Wh/kg)	Pmax (W/kg)	Pd (W/kg)
BCAP0650 P270	6.5	3500	3.29	15,100	5,400
BCAP1200 P270	5.3	3750	4.05	13,800	5,000
BCAP1500 P270	4.5	3900	4.75	16,200	5,800
BCAP2000 P270	3.8	4300	5.06	17,500	6,200
BCAP3000 P270	3.2	4800	5.52	13,800	5,400

> Dimensions:



Part Number	Vol (l)	Mass (kg)	Size (mm)			
			L	H (±0.5mm)	D_1 (±0.2mm)	D_2 (±0.7mm)
BCAP0650 P270 T04	0.211	0.20	51.5 ±0.5	14.0	60.4	60.7
BCAP1200 P270 T04	0.294	0.30	74.0 ±0.3	14.0	60.4	60.7
BCAP1500 P270 T04	0.325	0.32	85.0 ±0.3	14.0	60.4	60.7
BCAP2000 P270 T04	0.373	0.40	102.0 ±0.3	14.0	60.4	60.7
BCAP3000 P270 T04	0.475	0.55	138.0 ±0.3	14.0	60.4	60.7

Product dimensions and specifications may change without notice. Please contact Maxwell Technologies directly for any technical specifications critical to application.

> Mounting Recommendations:

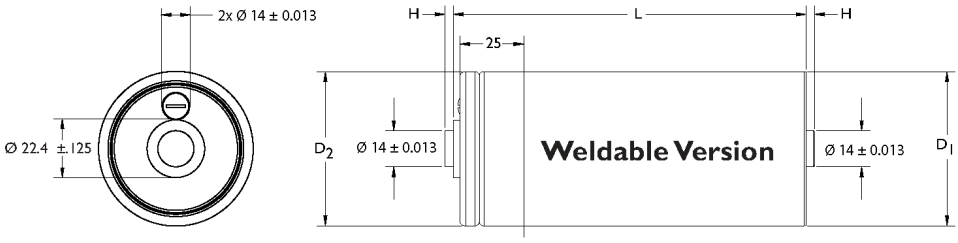
Do not reverse polarity.
Maximum torque for M12 screw terminals are 10Nm.
Cells are designed to be connected into series or parallel strings.
Clean terminals before mounting.

Worldwide Headquarters
MAXWELL TECHNOLOGIES
9244 Balboa Avenue • San Diego, 92123 CA, USA
PHONE: +(1) 858 503 3300
FAX: +(1) 858 503 3301
EMAIL: info@maxwell.com

European Office
MAXWELL TECHNOLOGIES SA
CH-1728 Rossens • Switzerland
PHONE: +41 (0) 26 411 85 00
FAX: +41 (0) 26 411 85 05
EMAIL: info@maxwell.com

www.maxwell.com

> Dimensions:



Part Number	Vol (l)	Mass (kg)	Size (mm)			
			L	H (±0.125mm)	D_1 (±0.2mm)	D_2 (±0.7mm)
BCAP0650 P270 T05	0.150	0.20	51.5 ±0.5	3.18	60.4	60.7
BCAP1200 P270 T05	0.233	0.30	74.0 ±0.3	3.18	60.4	60.7
BCAP1500 P270 T05	0.264	0.32	85.0 ±0.3	3.18	60.4	60.7
BCAP2000 P270 T05	0.312	0.40	102.0 ±0.3	3.18	60.4	60.7
BCAP3000 P270 T05	0.414	0.55	138.0 ±0.3	3.18	60.4	60.7

Product dimensions and specifications may change without notice. Please contact Maxwell Technologies directly for any technical specifications critical to application.

> Markings:

Capacitors are marked with the following information - Rated capacitance and rated voltage as well as energy/power type indication in the product naming. Serial number, name of manufacturer, positive and negative terminal, warning marking.

> Additional Technical Information:

Capacitance and ESR, DC measured per document 1007239

I_c= Leakage current after 72 hours, 25˚C Isc = short circuit current (maximum peak current)

R_{th} = Thermal resistance

$$E_{max} = \frac{\frac{1}{2} CV^2}{3600 \times mass} \qquad P_{max} = \frac{\frac{V^2}{4R\,(1khz)}}{mass} \qquad P_d = \frac{\frac{0.12V^2}{R\,(DC)}}{mass}$$

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Worldwide Headquarters
MAXWELL TECHNOLOGIES
9244 Balboa Avenue • San Diego, 92123 CA, USA
PHONE: +(1) 858 503 3300
FAX: +(1) 858 503 3301
EMAIL: info@maxwell.com

European Office
MAXWELL TECHNOLOGIES SA
CH-1728 Rossens • Switzerland
PHONE: +41 (0) 26 411 85 00
FAX: +41 (0) 26 411 85 05
EMAIL: info@maxwell.com

www.maxwell.com

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Worldwide Headquarters
MAXWELL TECHNOLOGIES
9244 Balboa Avenue • San Diego, 92123 CA, USA
PHONE: +(1) 858 503 3300
FAX: +(1) 858 503 3301
EMAIL: info@maxwell.com

European Office
MAXWELL TECHNOLOGIES SA
CH-1728 Rossens • Switzerland
PHONE: +41 (0) 26 411 85 00
FAX: +41 (0) 26 411 85 05
EMAIL: info@maxwell.com

www.maxwell.com

APPENDIX B

SCHEMATIC DIAGRAMS OF THE ULTRACAPACITOR TEST SYSTEM

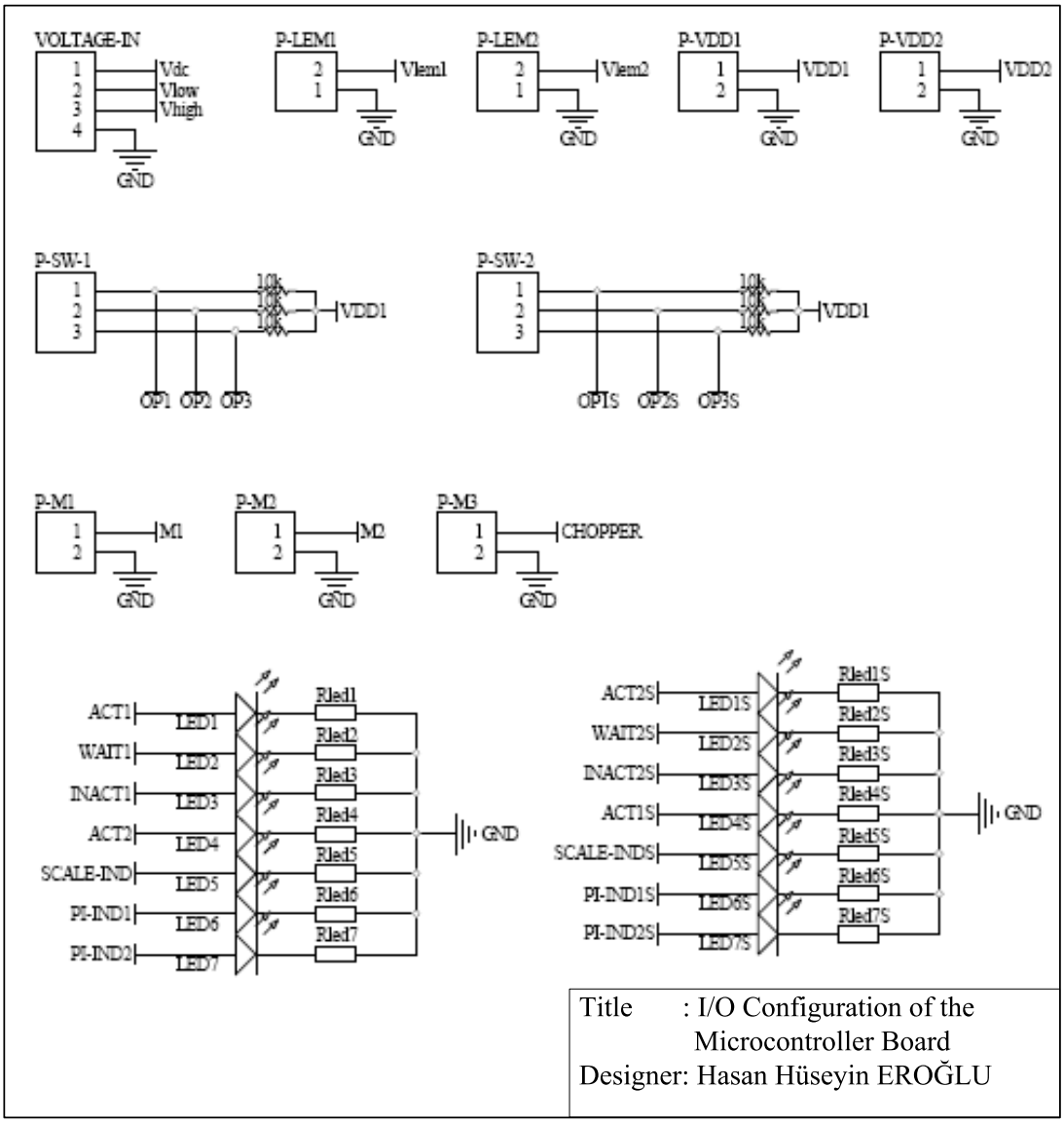

Figure B.1 Schematic diagram of the I/O configuration of the microcontroller board.

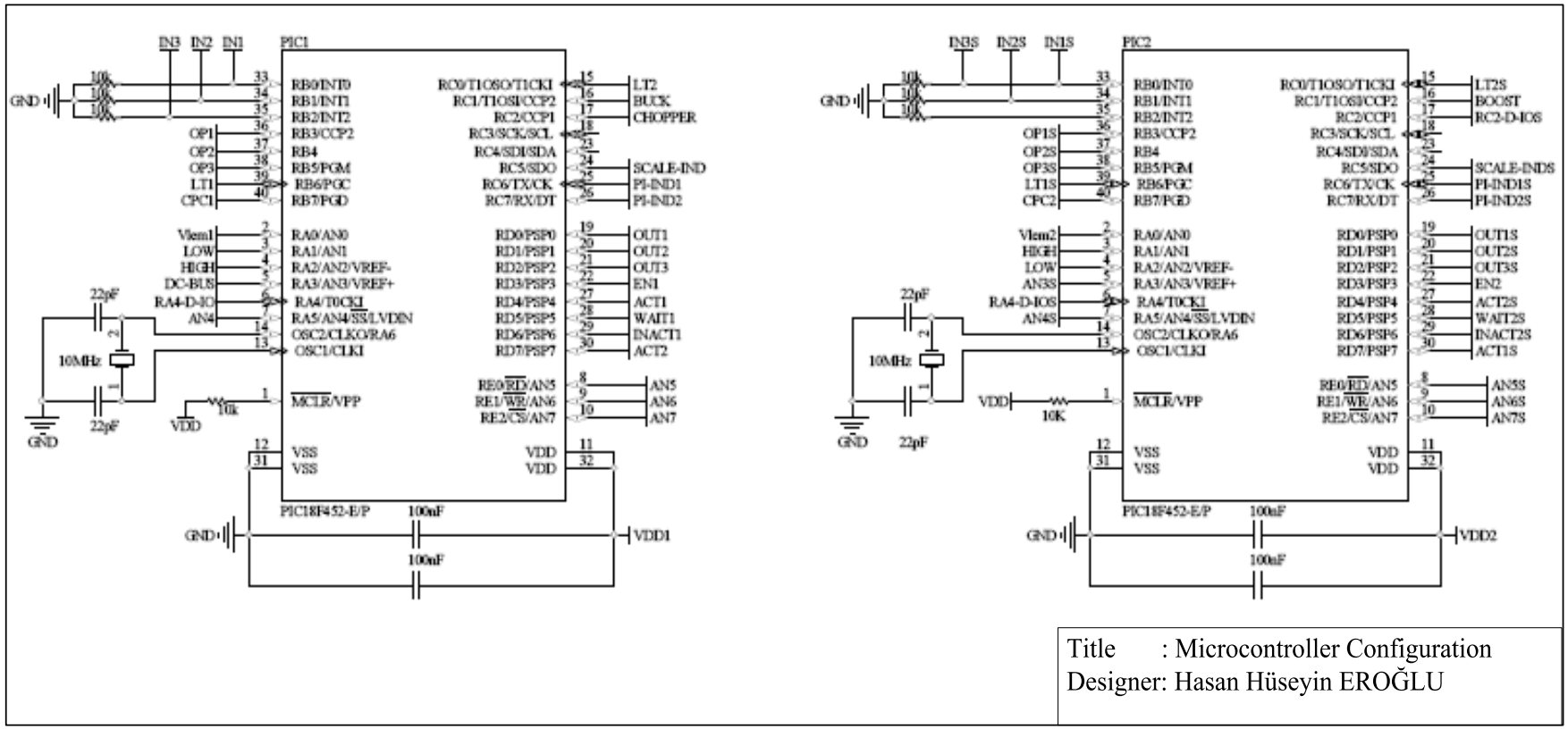

Figure B.2 Schematic diagram of the microcontroller configuration.

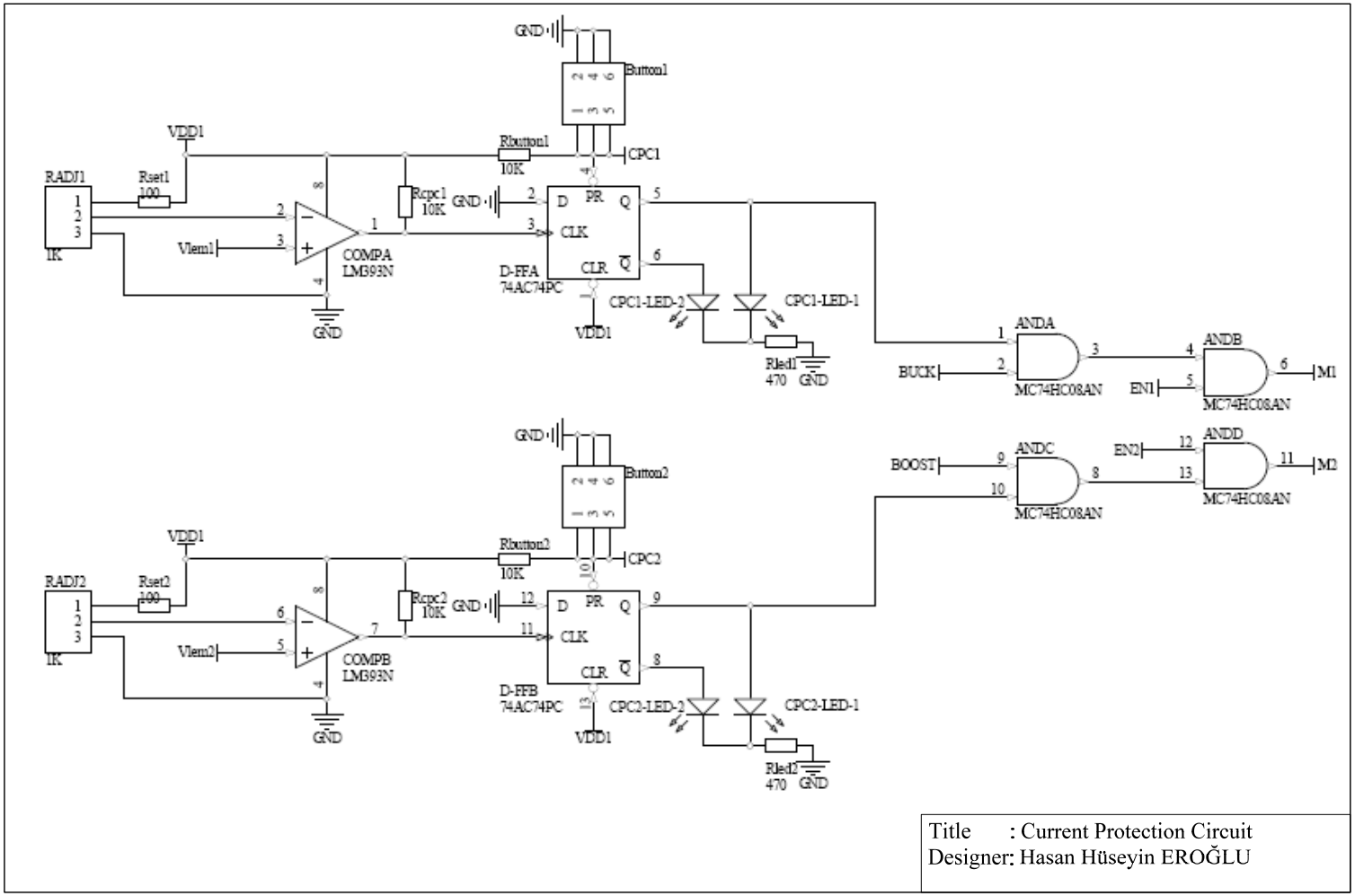

Figure B.3 Schematic diagram of the current protection circuit.

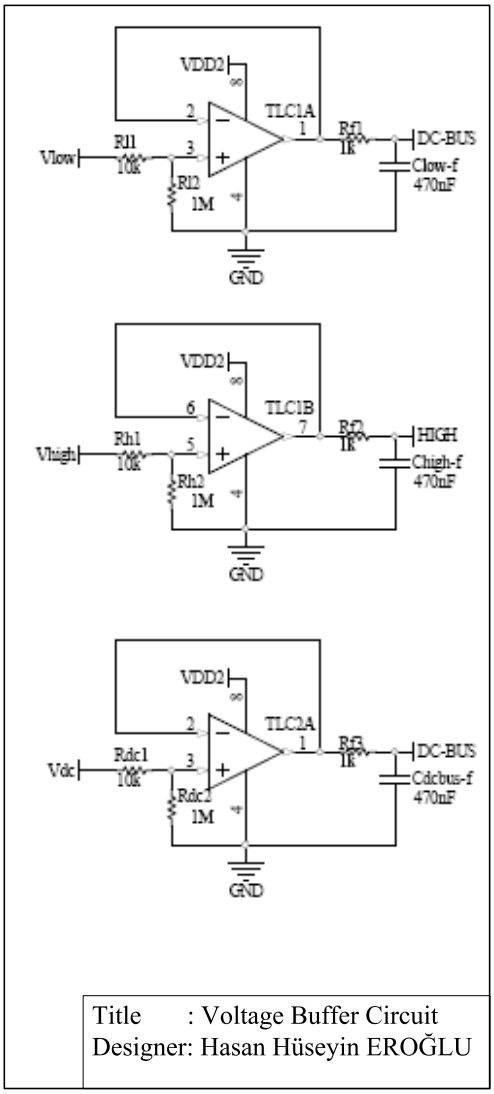

Figure B.4 Schematic diagram of the voltage buffer circuit.

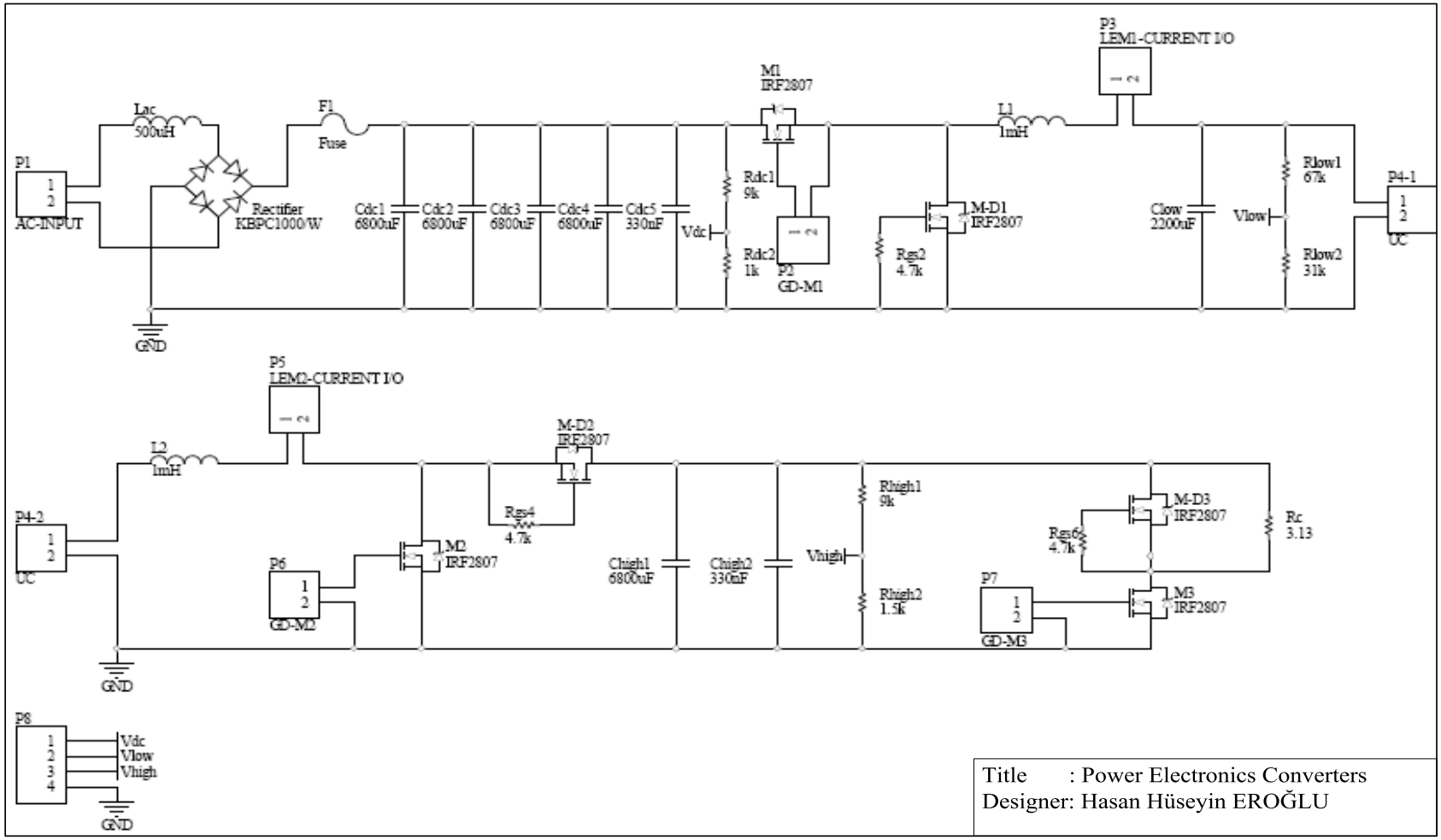

Figure B.5 Schematic diagram of the power electronics converters.

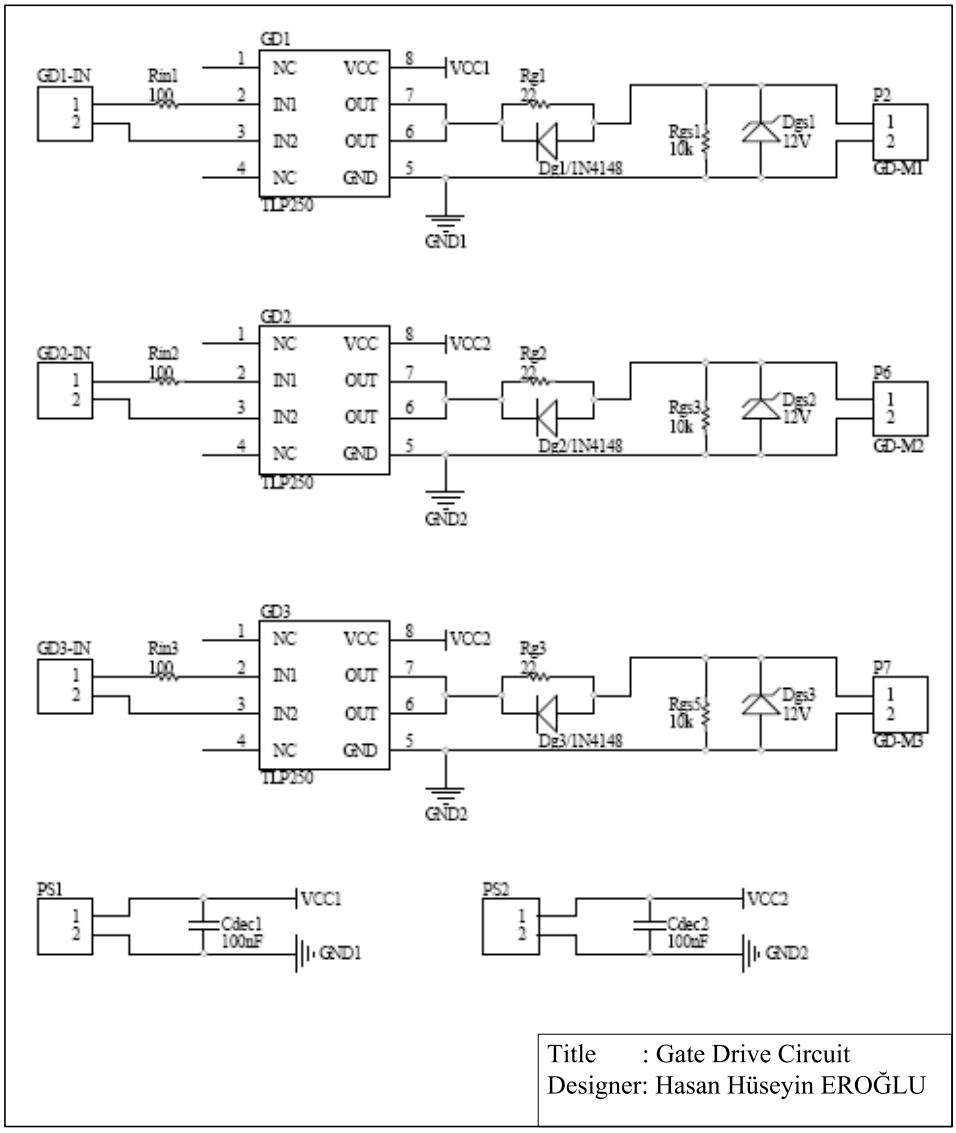

Figure B.6 Schematic diagram of the gate drive circuit.

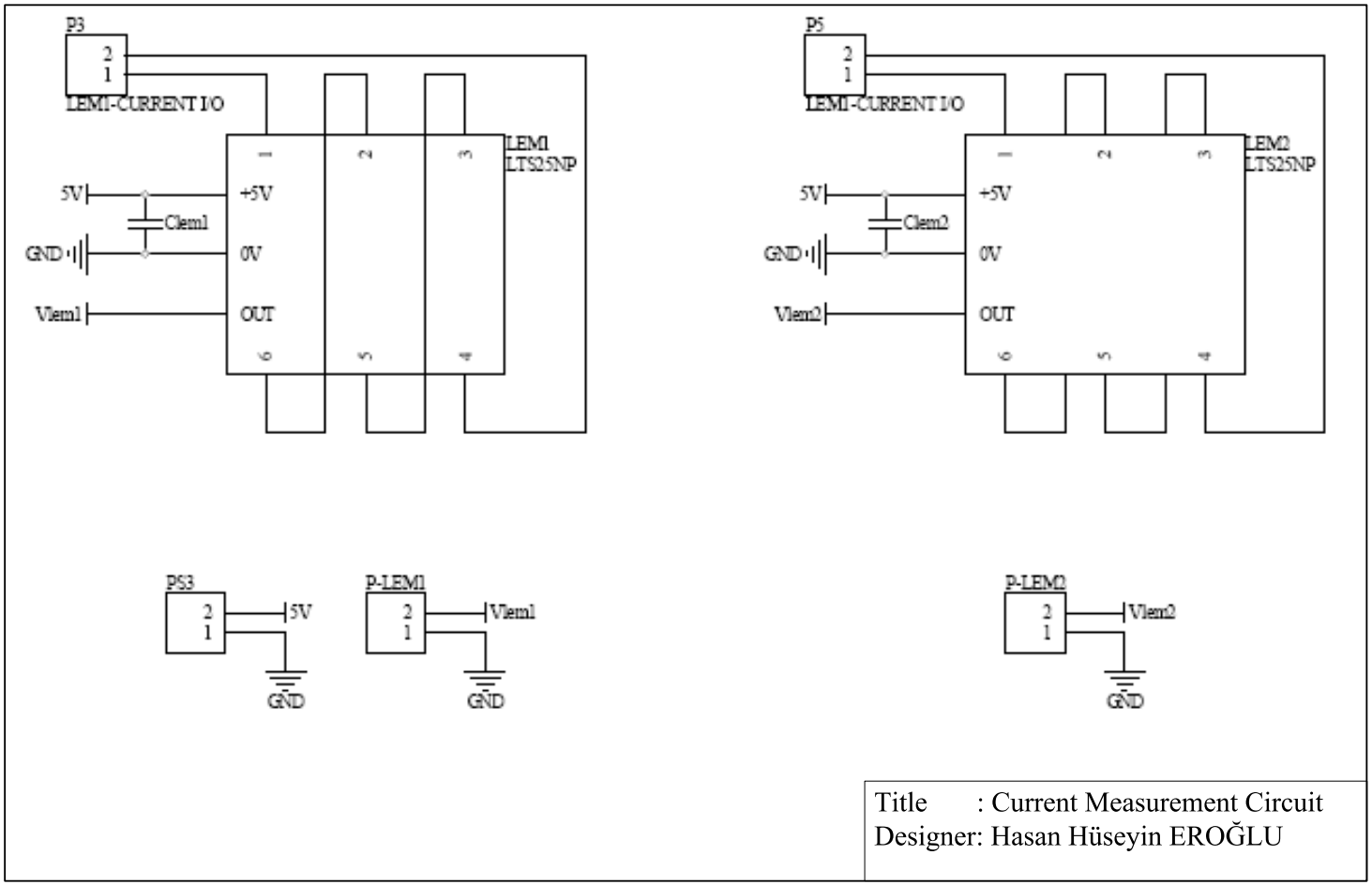

Figure B.7 Schematic diagram of the current measurement circuit.

APPENDIX C

CIRCUIT LAYOUTS OF THE ULTRACAPACITOR TEST SYSTEM

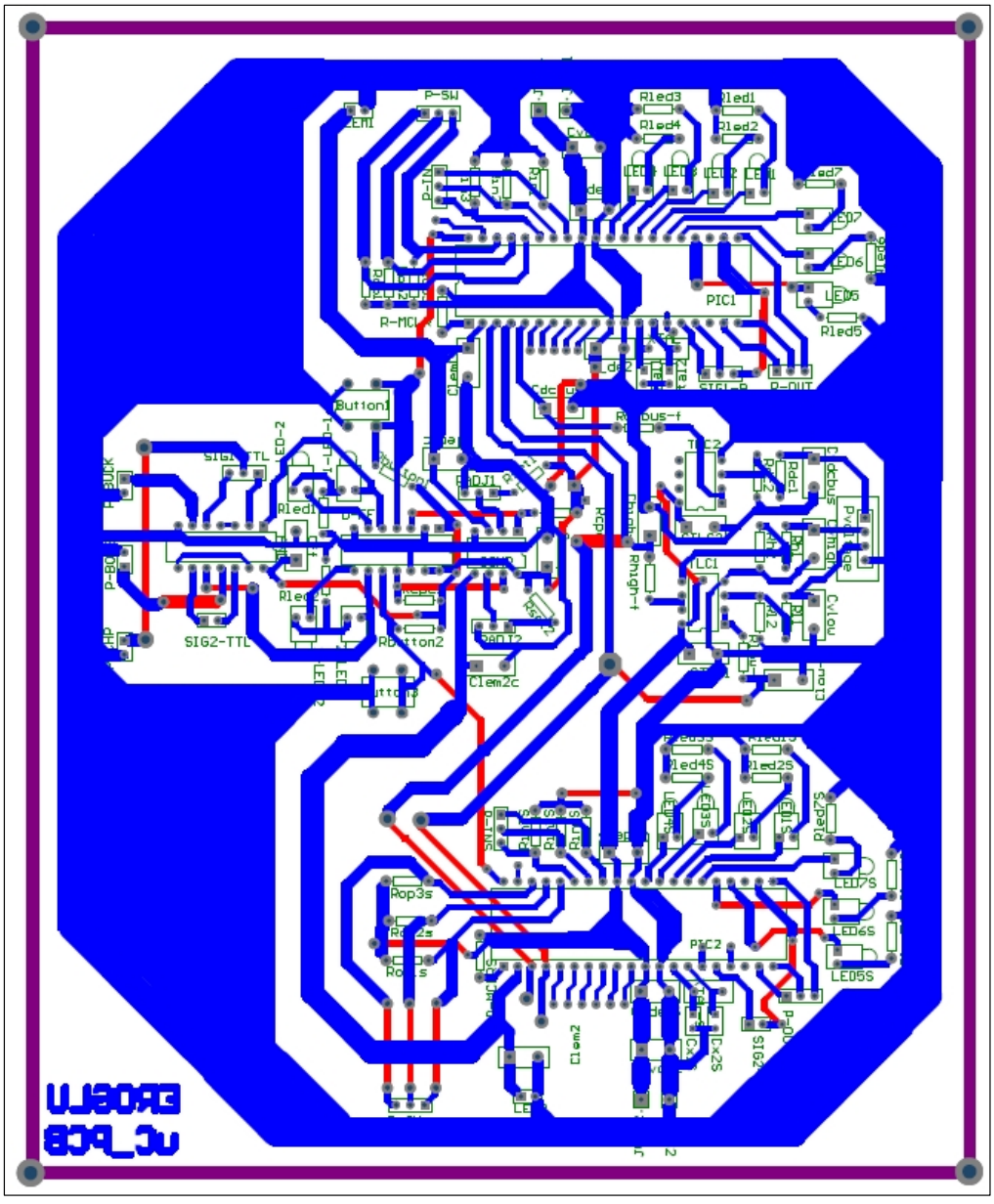

Figure C.1 Circuit layout of the microcontroller board.

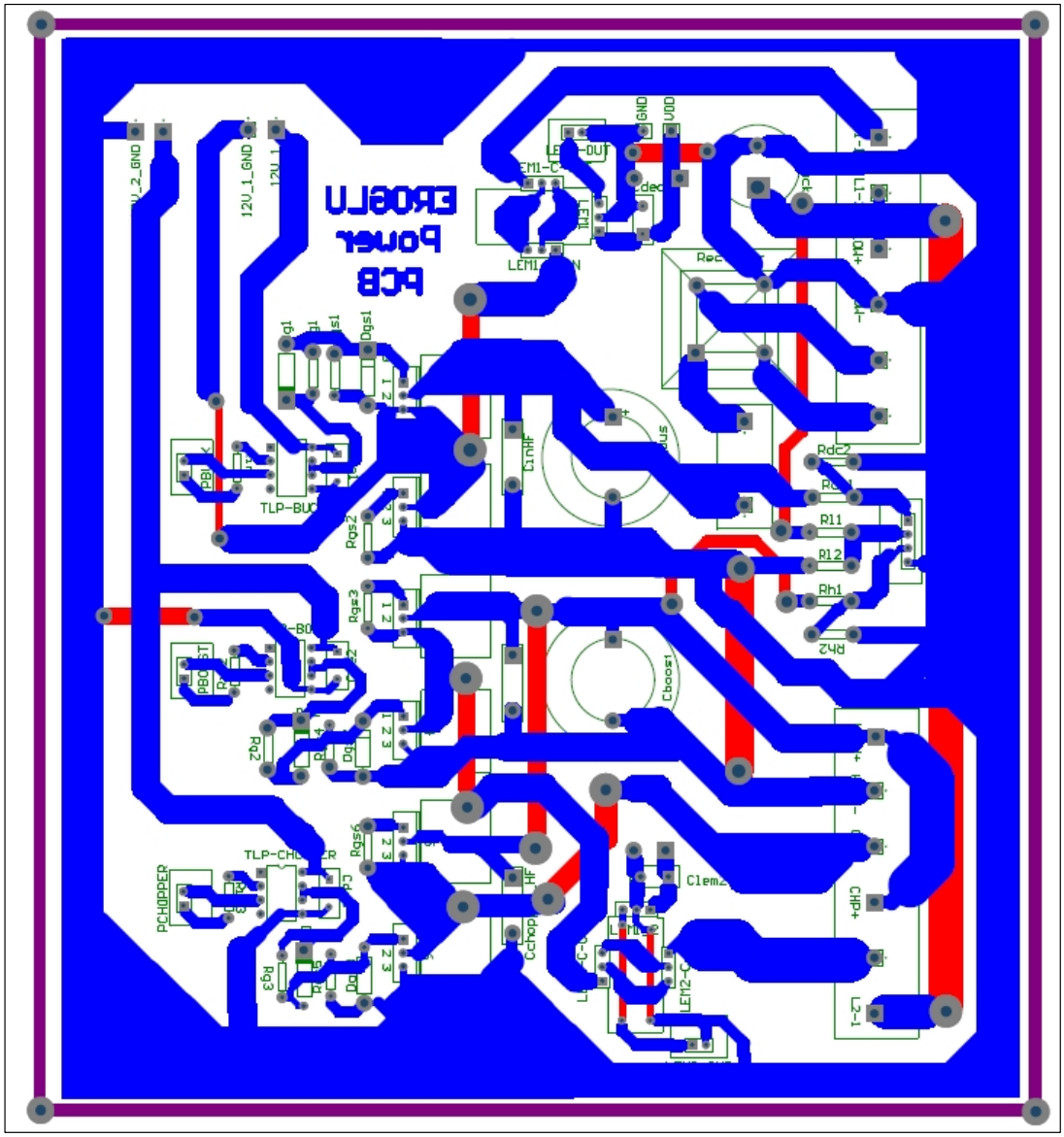

Figure C.2 Circuit layout of the power electronics converter board.

APPENDIX D

PHOTOGRAPHS OF THE PRINTED CIRCUIT BOARDS

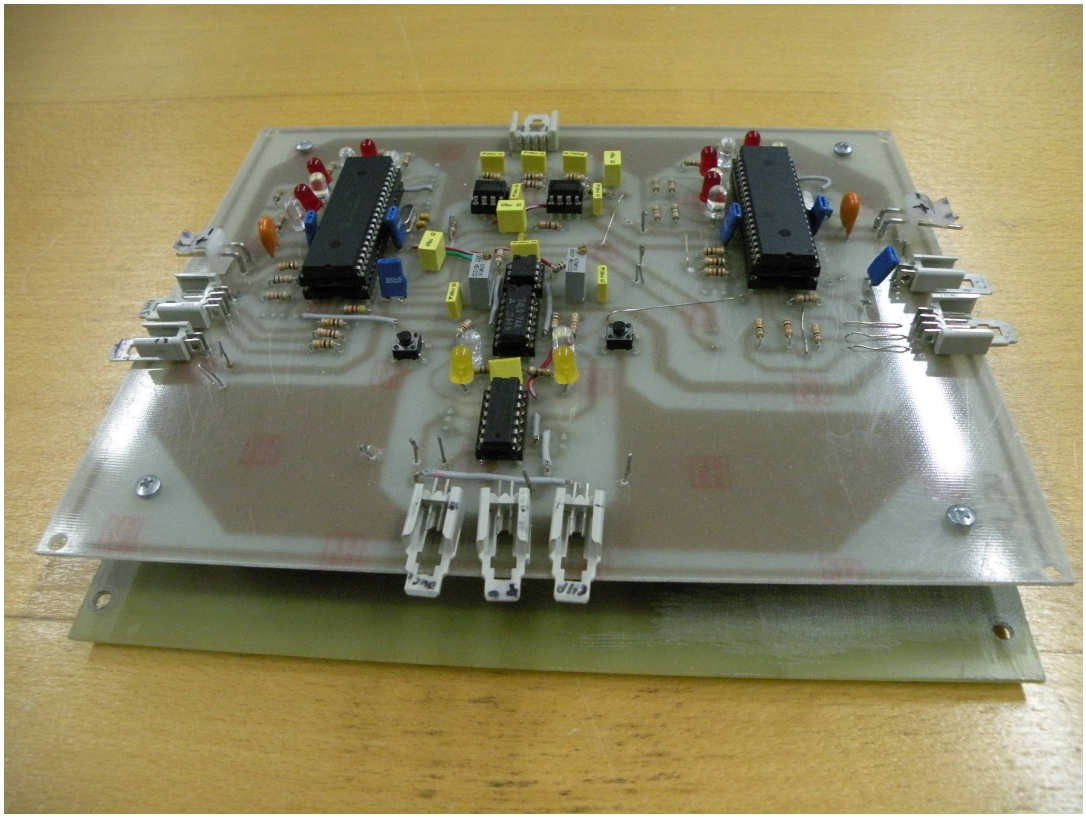

Figure D.1 Photograph of the microcontroller board.

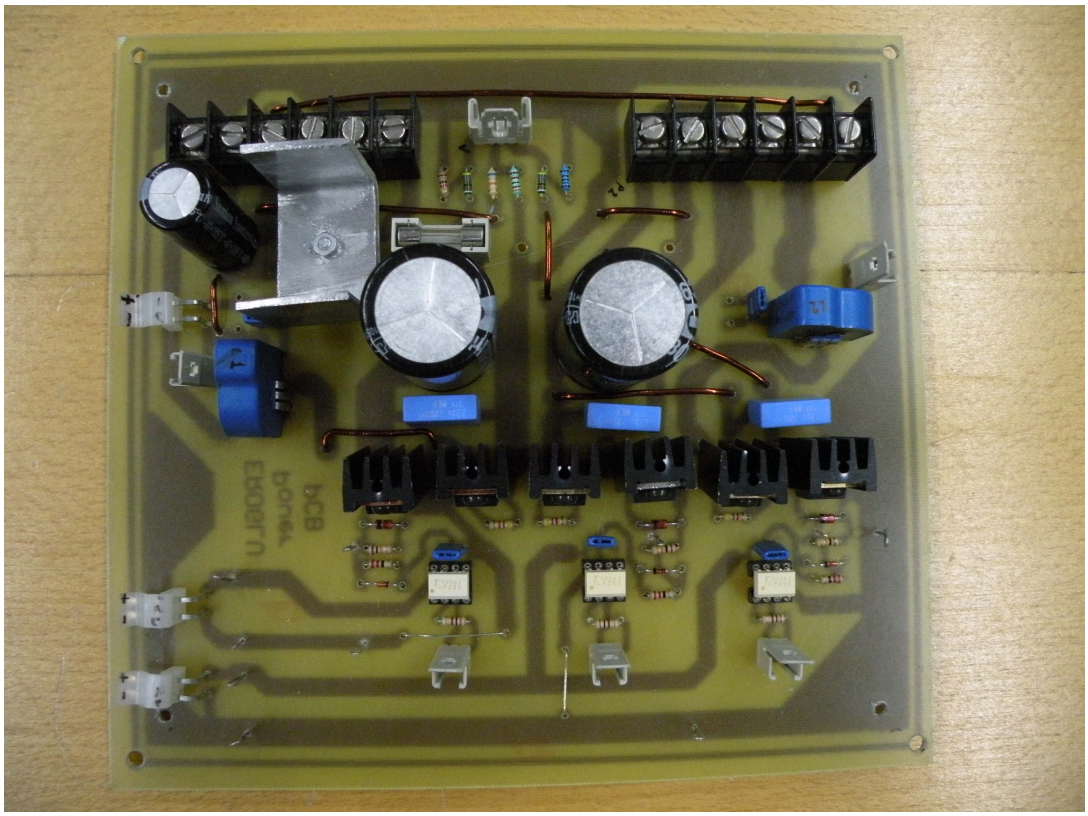

Figure D.2 Photograph of the power electronics converter board.

APPENDIX E

SOFTWARE STRUCTURE OF THE ULTRACAPACITOR TEST SYSTEM

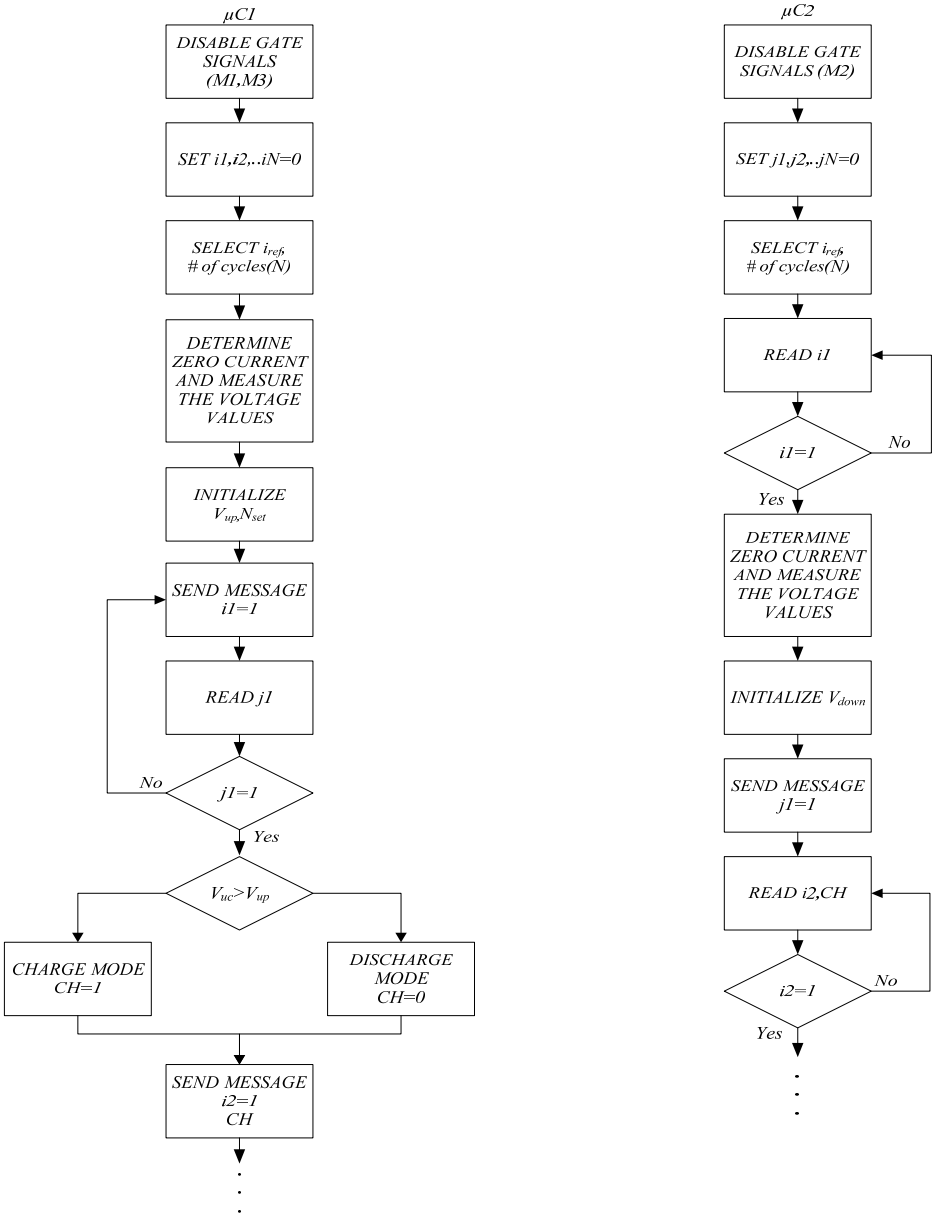

Figure E.1 Software structure of the UC test system (Part 1).

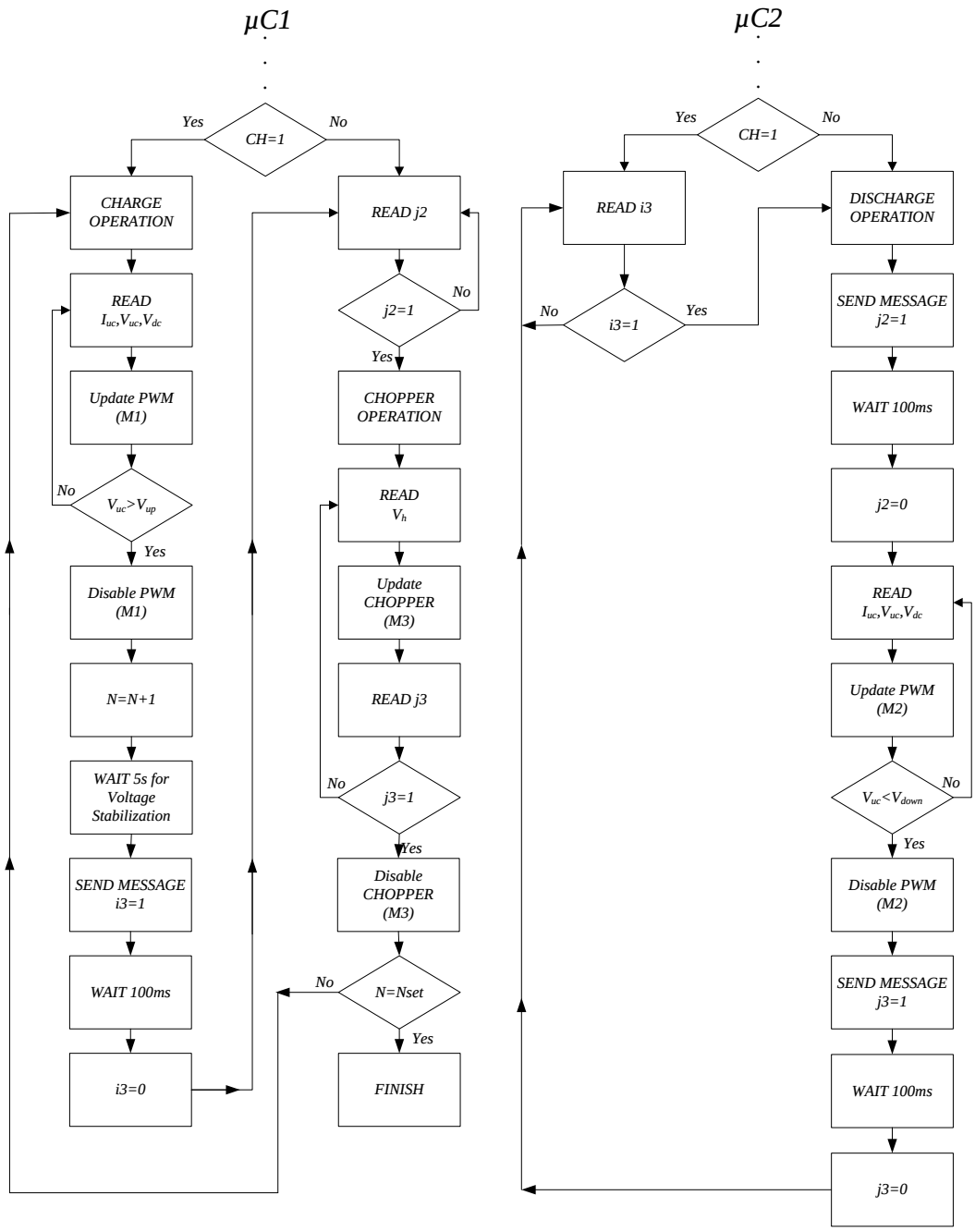

Figure E.2 Software structure of the UC test system (Part 2).

APPENDIX F

USER MANUAL OF THE ULTRACAPACITOR TEST SYSTEM

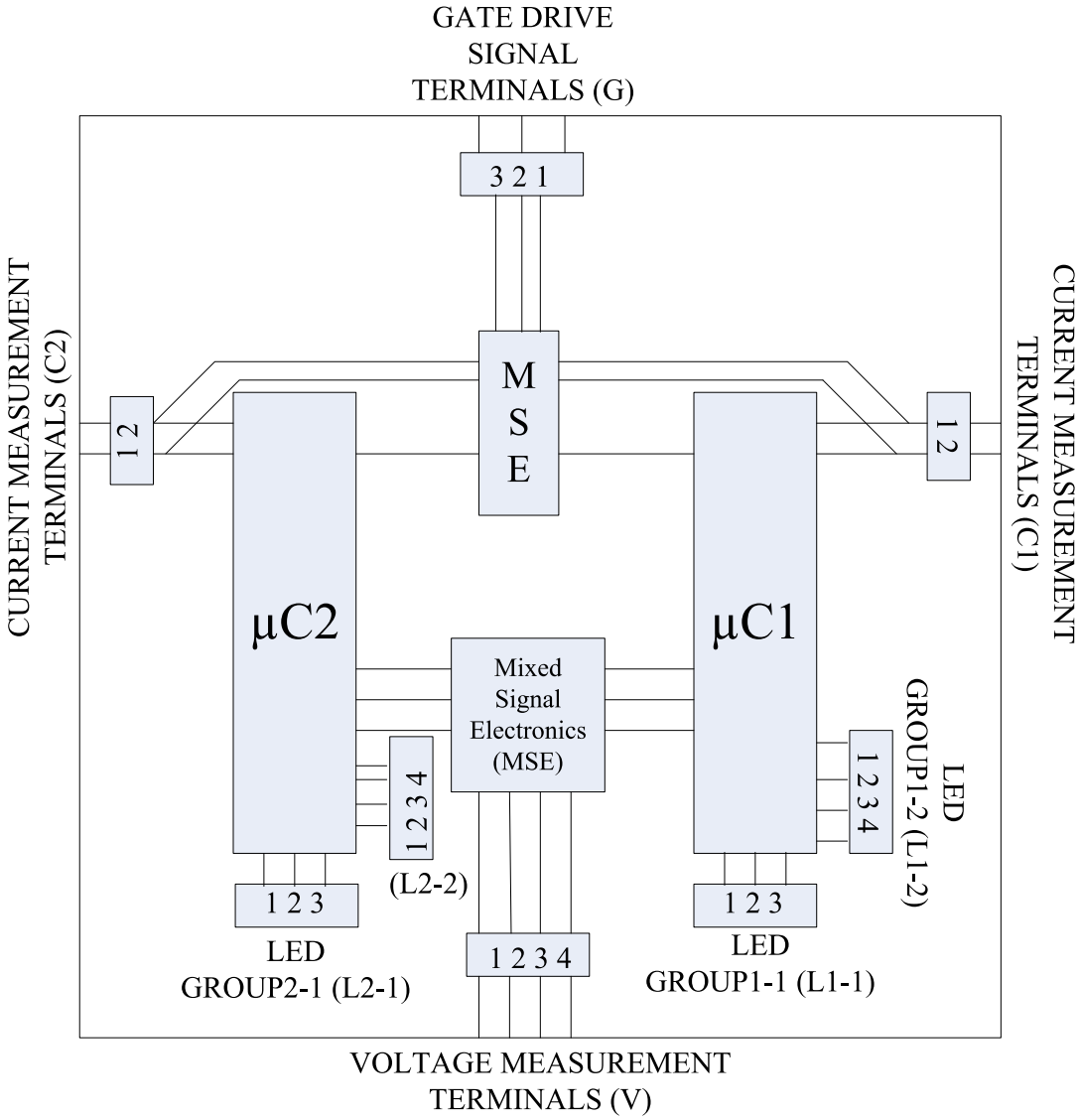

Figure F.1 Block diagram of the microcontroller board.

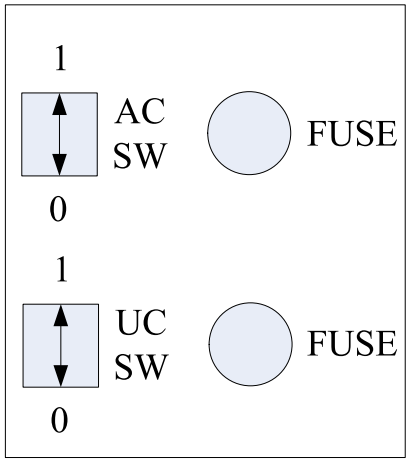

Figure F.2 Front panel structure of the UC test system.

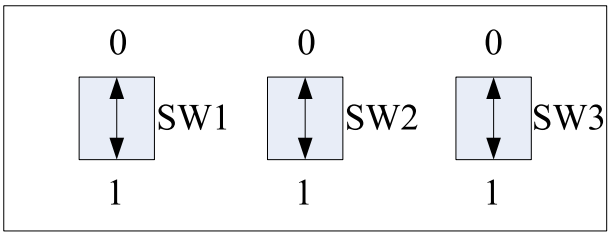

Figure F.3 Structure of the program selection board.

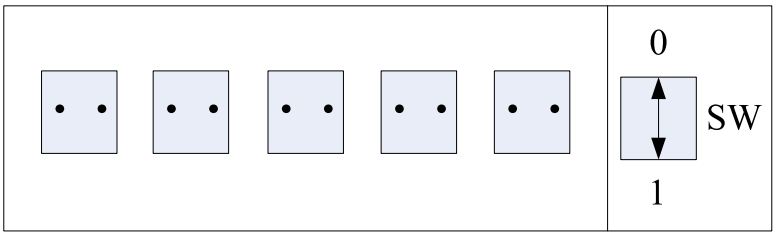

Figure F.4 Structure of the switched multiple sockets.

F.1 Instructions:

1. Make the position of AC SW and UC SW, and SW 0 (OFF).
2. Connect the power cord of the transformers placed on the bottom storey to the switched multiple socket.
3. Select the test program by utilizing the program selection board according to Table F.1.

Table F.1 Program selection

Operation	SW3	SW2	SW1
Discharge the UC module to zero volts level.	0	0	0
15A Constant Current Test	0	0	1
100W Constant Power Test	1	0	1

4. Make the position of AC SW and UC SW 1 (ON).
5. Make the position of SW 1 (ON).
6. L1-2 and L2-2 will illuminate representing the calibration and communication operations between µC1 and µC2.
7. At the end of the calibration and communication process charging process will start and L1-1 will illuminate (For the selection 001 or 101).
   8.1 Illumination of L1-1.1 represents that DC bus voltage is lower than DC bus voltage reference.
   8.2 Illumination of L1-1.2 represents that charging current is higher than the current reference.
   8.3 Illumination of L1-1.3 represents that charging current is lower than the current reference.

Note 8.1: Illumination of L1-1.2 and L1-1.3 together represents that charging current regulation is provided.

8. When the UC module terminal voltage reaches the upper level, charging operation will be stopped. L1-2.4 and L2-2.4 will flash respectively.
9. After the flashing operation of L2-2.4, discharging operation will start and L1-1 and L2-1 will illuminate.

9.1 Illumination of L2-1.1 represents that input voltage (UC voltage) is lower than voltage reference.

9.2 Illumination of L2-1.2 represents that discharging current is lower than current reference.

9.3 Illumination of L2-1.3 represents that discharging current is higher than voltage reference.

9.4 Illumination of L1-1.2 represents that output voltage is lower than the output voltage reference.

9.5 Illumination of L1-1.3 represents that output voltage is higher than the output voltage reference.

Note 9.1: Illumination of L2-1.2 and L2-1.3 together represents that discharging current regulation is provided.

Note 9.2: Illumination of L1-1.2 and L1-1.3 together represents that output voltage regulation is provided.

10. When the UC module terminal voltage reaches the lower level, discharging operation will be stopped. L2-2.4 and L1-2.4 will flash respectively. Charging operation will be provided in the next cycle.
11. If it is needed to finish the charging operation,
    12.1 First, make the position of the AC SW 0 (OFF).
    12.2 Second, make the position of SW 0 (OFF).
12. If it is needed to finish the discharging operation,
    13.1 First, make the position of the UC SW 0 (OFF).
    13.2 Second, make the position of SW 0 (OFF).