PRODUCTION OF HYDROGENATED NANOCRYSTALLINE SILICON BASED THIN FILM TRANSISTOR

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PRODUCTION OF HYDROGENATED NANOCRYSTALLINE SILICON BASED THIN FILM TRANSISTOR

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ABSTRACT

PRODUCTION OF HYDROGENATED NANOCRYSTALLINE SILICON BASED THIN FILM TRANSISTOR

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The instability under bias voltage stress and low mobility of hydrogenated amorphous silicon (a-Si:H) thin film transistor (TFT), produced by plasma enhanced chemical vapor deposition (PECVD) technique, are the main problems impeding the implementation of active matrix arrays for light emitting diode display panels and their peripheral circuitry. Replacing a-Si:H by hydrogenated nanocrystalline silicon film (nc-Si:H) seems a solution due to its higher mobility and better stability. Therefore nc-Si:H TFT was produced and investigated in this thesis.

All TFT layers (doped nc-Si:H, intrinsic nc-Si:H and insulator films) were produced separately, characterized by optical (UV-visible and FTIR spectroscopies, XRD) and electrical (current-voltage, $I-V$) methods, and optimized for TFT application. Afterwards the non self-aligned bottom-gate TFT structure was fabricated by the photolithographic method using 2-mask set.

The n^+ nc-Si:H films, used for TFT drain/source ohmic contacts, were produced at high H_2 dilution and at several RF power densities (P_{RF}). The change of their lateral resistivity (ρ) was measured by reducing the film thickness via reactive ion etching. The ρ values rise

below a critical film thickness, indicating the presence of the disordered and less conductive incubation layer. The optimum P_{RF} for the lowest incubation layer was determined.

Among the deposition parameters only increased NH_3/SiH_4 flow rate ratio improved the insulating properties of the amorphous silicon nitride (a-SiN_x:H) films, chosen as the TFT gate dielectric. The electrical characteristics of two TFTs with a-SiN_x:H having low leakage current, fabricated at different NH_3/SiH_4 ratios (∼19 and ∼28) were compared and discussed.

The properties (such as crystallinity, large area uniformity, etc.) of the nc-Si:H film as TFT channel layer, were found to depend on P_{RF}. For the films deposited at the center of the PECVD electrode the change from an amorphous dominant structure to a nanocrystalline phase took place with increasing P_{RF}, whereas those at the edge had always nanocrystalline nature, independent of P_{RF}. The two different TFTs produced at the center of the electrode with a-Si:H and nc-Si:H grown at low and high P_{RF}, respectively, were compared through their $I-V$ characteristics and electrical stability under the gate bias voltage stress.

Finally, nc-Si:H TFT structure, produced and optimized in this work, was analyzed through gate-insulator-drain/source capacitor by capacitance-voltage ($C-V$) measurements within 10^6-10^{-2} Hz frequency (F) range. The inversion regime was detected at low F without any external charge injection. Besides, ac hopping conductivity in the nc-Si:H bulk was extracted from the fitting results of the $C-F$ curves.

Keywords: Thin film transistor, plasma enhanced chemical vapor deposition technique, hydrogenated nanocrystalline silicon, amorphous silicon nitride

ÖZ

HİDROJENLENMİŞ NANOKRİSTAL SİLİSYUM TABANLI İNCE FİLM TRANSİSTÖR ÜRETİMİ

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Plazma destekli kimyasal buhar biriktirme tekniği (PECVD) ile üretilen alt geçit elektrotlu hidrojenlenmiş amorf silisyum (a-Si:H) ince film transistörün (TFT) voltaj baskısı altındaki kararsızlığı ve düşük hareketliliği, ışıyan diyotlu görüntüleme panellerindeki aktif matris örgüsünün ve çevre devresinin oluşturulmasını zorlaştıran başlıca sorunlardır. a-Si:H yerine, daha yüksek hareketliliği ve kararlılığından dolayı nanokristal silisyum (nc-Si:H) kullanımı çözüm olabileceği sanılmaktadır. Dolayısıyla, bu tezde nc-Si:H TFT üretilmiş ve incelenmiştir.

TFT tabakalarının herbiri (katkılı nc-Si:H, katkısız nc-Si:H ve yalıtkan filmler) ayrı ayrı üretilmiş, optik (Morötesi-görünür ve FTIR spektrometreleri, XRD) ve elektrik (akım-voltaj, $I - V$) metodları ile karakterize edilerek TFT uygulaması için iyileştirilmiştir. Ardından, kendiliğinden düzenlenmemiş alt geçitli TFT yapısı, fotolitografi metodu ile 2-maske takımı kullanarak üretilmiştir.

TFT'nin savak/kaynak ohmik bağlantıda kullanılan n^+ nc-Si:H filmler yüksek H_2 seyreltisi altında birkaç RF güç yoğunluğunda (P_{RF}) üretilmiştir. n^+ nc-Si:H filminin yatay özdirenç (ρ) değişimi, filmin kalınlığı reaktif iyon aşındırmayla kademeli inceltilerek ölçülmüştür. Filmin

kalınlığı bir eşiğin altına düşünce ρ değerlerinin artması düzensiz ve daha dirençli bir geçiş tabakasının varlığına işaret etmektedir. En düşük geçiş tabakası kalınlığını sağlayan P_{RF} belirlenmiştir.

Biriktirme parametrelerinin arasında sadece NH_3/SiH_4 akış hızları oranının yükseltilmesi, TFT'nin geçit yalıtkanı olarak seçilen amorf silisyum nitrür (a-SiN_x:H) filmlerin yalıtkan özelliklerini iyileştirmiştir. Düşük kaçak akımlı, farklı NH_3/SiH_4 oranlarında (~19 and ~28) üretilmiş a-SiN_x:H içeren iki TFT'nin özellikleri karşılaştırılarak tartışılmıştır.

TFT kanal bileşeni olarak, nc-Si:H filminin, kristal derecesi, geniş alan aynı yapılılığı gibi özellikliklerinin P_{RF}'e bağlı oldukları tespit edilmiştir. P_{RF} arttıkça, PECVD'nin elektrot merkezinde büyütülmüş filmler için amorf baskın yapıdan nanokristal faza geçişinin gerçekleşmesine karşın kenar bölgedeki filmler her P_{RF}'de nanokristal yapıda oluşmuştur. Elektrot merkezinde düşük P_{RF}'de büyütülmüş a-Si:H ve yüksek P_{RF}'te büyütülmüş nc-Si:H'yi içeren farklı iki TFT, $I-V$ özellikleri ve geçit voltaj stresinin altındaki elektriksel kararlılıkları bakımından kıyaslanmıştır.

Son olarak, bu çalışmada üretilmiş ve optimize edilmiş nc-Si:H TFT yapısı 10^6-10^{-2} Hz frekans (F) aralığında alınan sığa-gerilim ($C-V$) ölçümleri ile incelenmiştir. Eksi kutuplu geçiş gerilimi altında, karşıt taşıyıcıların yığılması, düşük F'lerde, harici yük enjeksiyonu olmadan gözlemlenebilmiştir. Ayrıca, nc-Si:H bünyesinde, ac hoplama iletkenliği, $C-F$ eğrilerin çözümlenmesinden ortaya çıkartılmıştır.

Anahtar Kelimeler: İnce film transistör, plazma destekli kimyasal buhar biriktirme tekniği, hidrojenlenmiş nanokristal silisyum, amorf silisyum nitrür

Dedicated to my husband, Mustafa

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I would like to express my thanks to my parents, Svetlana and İgor, and my brother İlgar for their love, support and encouragement during my PhD study.

Finally, I dedicate this work to my colleague and husband, Mustafa. I am thankful for his help in the laboratory work and discussions on the optical properties of the thin films. His patience, understanding and moral support are highly appreciated.

TABLE OF CONTENTS

LIST OF TABLES

TABLES

LIST OF FIGURES

FIGURES

CHAPTER 1

INTRODUCTION

1.1 Large Area Electronics

While the aim of today's microelectronics is to decrease the scale of microelectronic devices, macroelectronics deals with the low-cost integration of these devices over large area. Among the common products of the large area electronics are flat-panel displays (FPDs), image sensors, scanners, printers, etc. with substrate sizes larger than the industrial crystalline wafers used for microelectronics. Besides this size limitation of microelectronics for large area applications, conventional crystalline silicon (c-Si) based electronics cannot be integrated with Si optical components due to its poor light emitting/absorbing properties [1]. The solution is found by depositing silicon-based thin films on different substrates (glass, plastics, metal foil, etc.) to form devices equivalent to crystalline counterparts so that the conventional Si technology is implemented on the large scale.

1.2 Need for Thin Film Transistor

Nowadays displaying is modified by gradual replacement of heavy vacuum cathode ray tubes (CRTs) with FPDs, although the latter remain more costly. Modern FPDs are represented by most popular product, liquid crystal displays (LCDs). They are designed by arranging circuits of picture elements, i.e. pixels, in a matrix of m rows and n columns (Figure 1.1). To maintain the state of a pixel usually matrix addressing is preferred, since it requires low number of control signals ($m+n$). When one row is selected by row driver, signals coming from column driver are addressed to the pixels within this row, and then next rows are selected one by one.

In order to increase the response time, which plays important role in fast moving video,

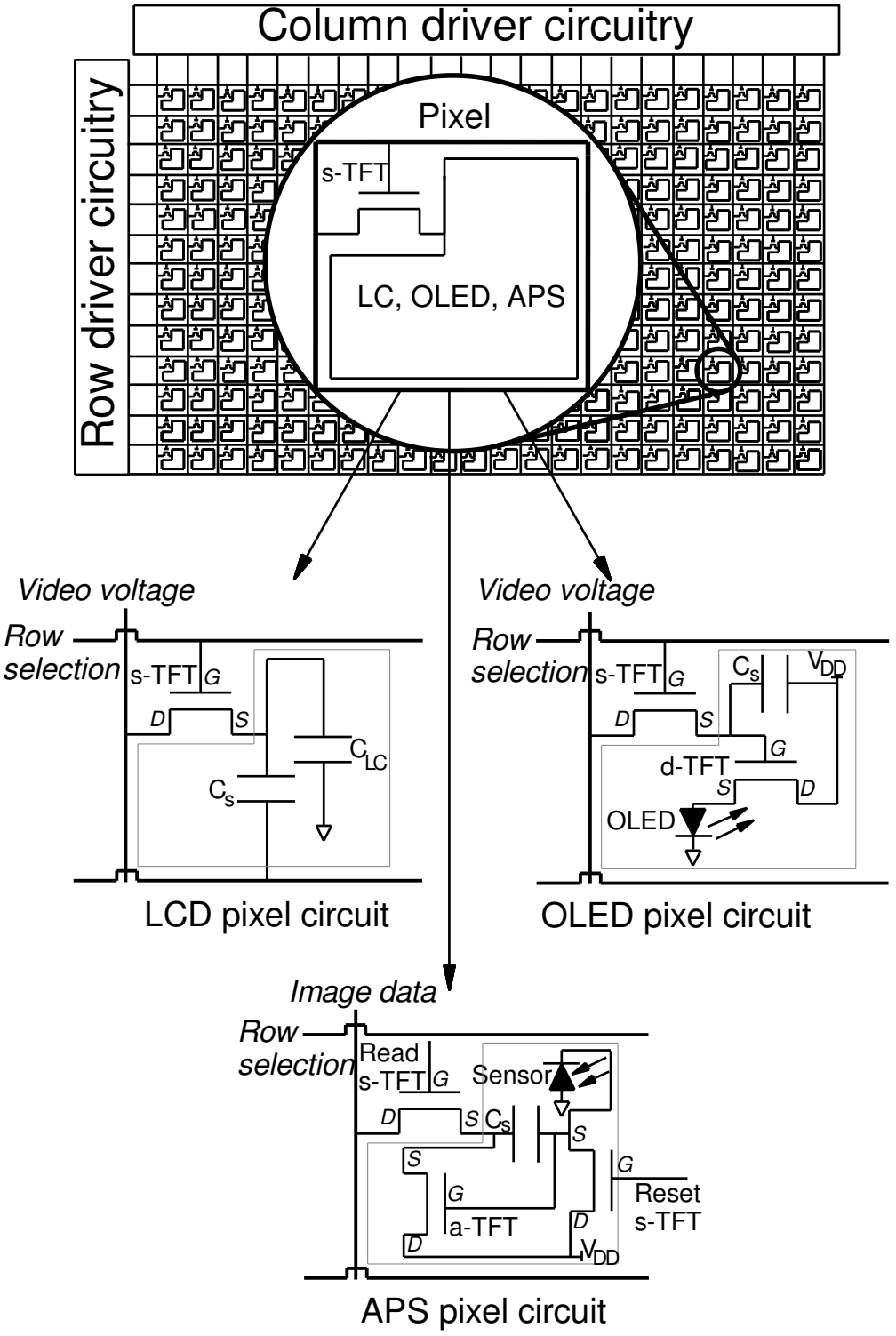


Figure 1.1: Active matrix array with detailed pixel architectures for applications in liquid crystal display (LCD), organic light emitting diode (OLED) display and active pixel sensor (APS) imager.

active-matrix addressing is implemented, providing better performance than passive one. In passive-matrix each pixel is addressed for more than one frame and therefore it receives average signals. This results in poor contrast, low response time and high crosstalks between signal lines. In contrast, active-matrix drives only one pixel in a frame by the use of switching device at each pixel. These switching devices are called thin film transistors (TFT) due to the use of the thin film technology for their easy and low-cost deposition over large area. In addition to this advantage, use of amorphous silicon (a-Si) instead of c-Si wafer inside TFT leads to low leakage currents during "sleep" mode of device operation.

1.3 Applications of TFT

In Figure 1.1 TFTs with switching, driving and amplifying roles are demonstrated for different types of pixels. For example, in LCD pixel [2] switch TFT (s-TFT) is activated by its gate contact (G) to transfer the video voltage through drain/source contacts (D/S, difference comes from voltage value: $V_D > V_S$) to the electrodes of the capacitor containing liquid crystals (LC), which can tune the intensity of the backlight of the LCD panel. Storage capacitor (C_s) acts as stabilizer of voltage between electrodes of LCs for the time until this pixel is driven again (i.e. one frame). In LCDs three subpixels are imbedded in one pixel to produce all colors by 3-colored filter. Therefore, for a given display resolution mn there are $3mn$ as many s-TFTs. Note here how crucial is the role of thin film technology in production of over 2 million TFTs for large scale displays.

Today's FPD market witnesses the birth of the competition between LCDs and organic light emitting diode (OLED) displays. The OLEDs as well as inorganic LEDs (difference lies in the use of organic molecules instead of Si-based *pin* structure) emit light itself, so there is no need for filter and backlight of LCDs, which consumes power even when pixel emit no light or uses light only partly by filtering it. As a result, quick response time, absence of limitation in viewing angle, opportunity to be used on flexible substrates, thinner display are advantages of OLEDs compared to LCDs. However OLEDs' lifetime is lower than that of inorganic LEDs, leading to poor stability. In LED containing pixel (see Figure 1.1) one of the TFTs (s-TFT) again plays switching role to charge C_s [3]. Another TFT (d-TFT) drives to LEDs current, which is determined by its gate voltage value supplied by C_s and $D - S$ voltage supplied by voltage source (V_{DD}). Here d-TFT current is ideally constant throughout the frame period, so that these TFTs must have high electrical stability. Note that small variations in a voltage

across LEDs result in large changes in current and luminance according to current-voltage (I-V) characteristics of LEDs. Consequently, s-TFTs are required to have low leakage current to avoid voltage loss across C_s during "sleep" mode.

As an example for image sensor, active pixel sensor (APS), demonstrated in Figure 1.1, is a promising circuit for medical imaging applications such as fluoroscopy [4]. Here two s-TFTs are used for charging C_s (reset s-TFT) and reading image data (read s-TFT), while the third amplifier TFT (a-TFT) amplifies the small signal coming from generated photocarriers. To obtain gain from a-TFT its stability should be high enough.

It can be concluded that electrical instability in d-TFT and a-TFT is a crucial drawback for their implementation in OLED and APS. Besides, studies to improve switching mobility for s-TFT are conducted to achieve the similar performance of costly CMOS transistors used in row/column driver circuitry.

1.4 Historical Review of TFT

Although field effect concept and devices were attempted before the invention of the first point-contact bipolar transistor in 1947 by J. Bardeen and W. Brattain, history of TFT with nowadays used structure began in 1961 by R.C. Weimer [2, 5]. R.C. Weimer used polycrystalline cadmium sulfide (CdS) for a thin film channel, silicon monoxide for an insulator and gold for gate, D/S electrodes, forming now known as top-gate staggered structured TFT (see Figure 1.2). However until the beginning of 1970s, researches on TFT lagged behind the developments in metal-oxide-semiconductor field-effect transistor (MOSFET), which uses c-Si

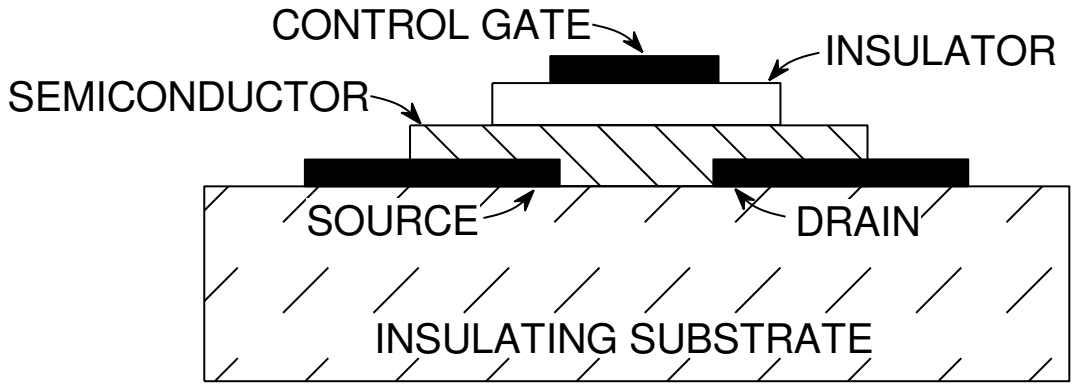


Figure 1.2: The top-gate staggered CdS TFT structure developed by R.C. Weimer [6].

for the active layer and was firstly demonstrated by Kahng and Atalla in 1960 [5, 7]. Main purpose was to obtain denser integrated circuit chips as compared to bipolar transistors with higher performance [8], but such miniaturization did not respond to the needs of low-cost large area electronics. To reduce the crosstalk in liquid crystal displays, Lechner *et al.* [9] proposed incorporation of TFTs in each pixel in 1971. This idea was realized by Brody *et al.* [10] too and as a result they fabricated a first $6'' \times 6''$ sized cadmium selenide (CdSe) based TFT-addressed LCD panel. However, CdSe thin film is a polycrystalline material with grain boundaries and is changed under ambient atmosphere; consequently TFTs have poor DC stability which degrades the drain current under constant gate voltage. While searching for another TFT channel materials, works on solar cells and discovery of *p*- and *n*- doping opportunity for hydrogenated amorphous silicon (a-Si:H) led leComber *et al.* [11] to produce a first a-Si:H TFT with silicon nitride (SiN) as insulator in 1979. Although the mobilities of a-Si:H TFT were less than the ones of CdSe, ON and OFF currents (more than 1 μA and about 1 nA, respectively) suited for their applications in LCDs [5]. In 1983 Suzuki *et al.* [12] deposited n^+ doped D/S semiconductor contacts upon the a-Si:H layer to obtain low contact resistance between channel and D/S electrodes. The advantages of a-Si:H over other TFT channel materials are summarized as follows: its low-cost, i.e. large area and low temperature deposition possibility; its good interface properties with other materials, especially with SiN; it is suitable for photolithographic process; it has high electrical resistivity resulting in low OFF current and at the same time, when doped, its conductivity is enough for charging LC capacitance; it is non-toxic [2]. Further studies on polycrystalline silicon (poly-Si) and CdSe resulted in higher mobilities than in a-Si:H, but more expensive production steps and uncertainty in number of grains in the channel [5] led to dominance of a-Si:H TFTs in today's market.

1.5 Thesis Outline

In chapter 2, the operation principles and physics of TFT were presented in light of ideal square-law model. The deviations of real TFT from this model were also discussed. Besides, the TFT parameter extraction was illustrated on the simulated graphs.

In chapter 3, the components of TFT were reviewed from literature sources. Type and deposition conditions of electrodes, dielectric and semiconductor materials were discussed for their application in TFT.

In chapter 4, production of the test samples and TFT used in this study were presented and summarized by the experimental flowcharts.

Chapter 5 encloses characterization of doped hydrogenated nanocrystalline silicon (nc-Si:H) and hydrogenated amorphous silicon nitride (a-SiN_x:H) thin films deposited in this study, and optimization of their growth conditions for TFT applications. The two TFT sets with different a-SiN_x:H films were fabricated and their device performances were compared.

In chapter 6, the effect of RF power density on the properties of nc-Si:H thin films and their large area uniformity in the deposition system at hand was investigated through opto-electronic characterization. The RF power density of nc-Si:H deposition was optimized for TFT applications and large area uniformity. The performance of the TFT with nc-Si:H layer produced at this optimum condition was compared to that of another TFT with nc-Si:H grown at different power density.

Chapter 7 deals with the capacitance measurements within 10^6-10^{-2} Hz frequency range on the metal-insulator-amorphous silicon (MIAS) structure of the optimized nc-Si:H TFT by mechanically isolating it from the same TFT. The electrical properties of nc-Si:H bulk for both structures were analyzed and the results provide insight into the conduction mechanism within TFT.

Chapter 8 includes the main contributions of this thesis on nc-Si:H TFTs.

CHAPTER 2

PHYSICS OF THIN FILM TRANSISTOR

2.1 Ideal Square-Law Model

TFT operation mechanism and physics behind it will be described considering ideal coplanar bottom-gate TFT structure (see Figure 2.1) and then discussion may be extended to other structures [see section 2.3]. Main components of TFT (Figure 2.1) are n^+ doped drain/source (D/S) semiconductor contacts with the electrodes above them and thin film semiconductor layer between these contacts, which are separated from the gate electrode by the insulator so that semiconductor "sees" only the field of the gate voltage. Applying negative gate voltage depletes electrons from the semiconductor/insulator interface, so that energy bands of the

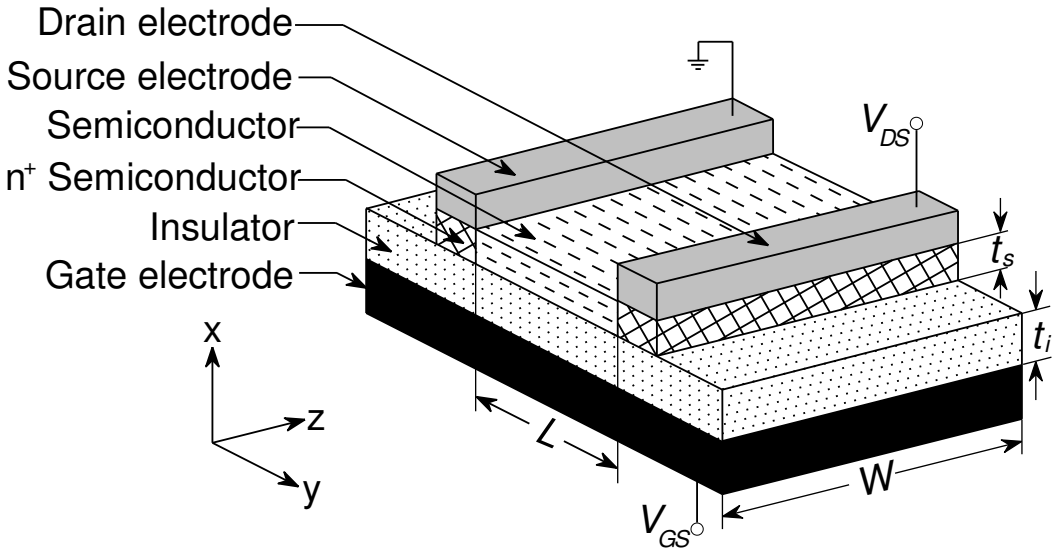


Figure 2.1: The coplanar bottom-gate TFT structure used in the analysis of an ideal TFT.

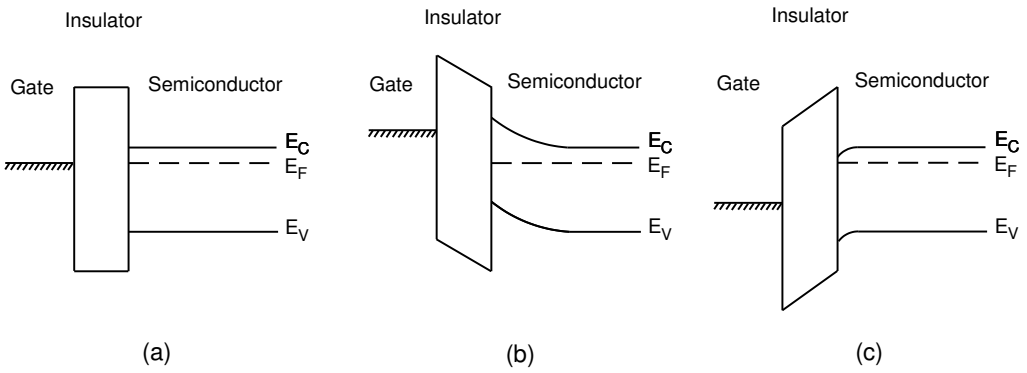


Figure 2.2: Energy band diagrams as viewed from the gate of an ideal n-type TFT under different gate voltage conditions: (a) equilibrium ($V_{GS} = 0$ V), (b) depletion ($V_{GS} < 0$ V), (c) accumulation ($V_{GS} > 0$ V).

semiconductor bend upward forming depletion region as shown in Figure 2.2. In contrary, positive voltage of the gate electrode induces accumulation channel within the active layer near the semiconductor/insulator interface. As a result energy bands of the semiconductor near the interface bend downward. The accumulated electrons begin to flow from the source towards the drain when positive voltage (V_{DS}) is applied to the drain electrode. As V_{DS} is gradually increased the induced channel current (I_{DS}) increases linearly thus forming linear or ohmic region (see Figure 2.3-a), but further V_{DS} increase results in depletion of electrons near the drain region. When this depletion leaves no electrons next to the drain region, called as pinch-off point (P), current saturates at $I_{DS\,sat}$ corresponding to $V_{DS\,sat}$ (onset of saturation, see Figure 2.3-b). For beyond saturation region ($V_{DS} > V_{DS\,sat}$) drain current and voltage at P remains unchanged. However, in the real TFT output curves there might be a very slight increase in the saturation current with increasing V_{DS} instead of such ideal "hard" saturation. This is probably related to the possible decrease in channel length from L to L' (see Figure 2.3-c) if high electron depletion occurs.

The above discussion is based on a typical MOSFET operation [8] with differences in regimes where electrons form channel: it is accumulation in TFT and inversion in MOSFET. In analogy to MOSFETs, depending on type of accumulation layer there are *enhancement*-mode (normally-off) and *depletion*-mode (normally-on) TFTs. In *enhancement*-mode n-type TFTs there is negligible drain current under $V_{GS} = 0$ V. In this case accumulation layer is not formed until a positive voltage $V_{GS} = V_T$ is applied (here V_T is the threshold voltage). For *depletion*-mode TFTs large I_{DS} can flow at $V_{GS} = 0$ V, therefore one needs to apply

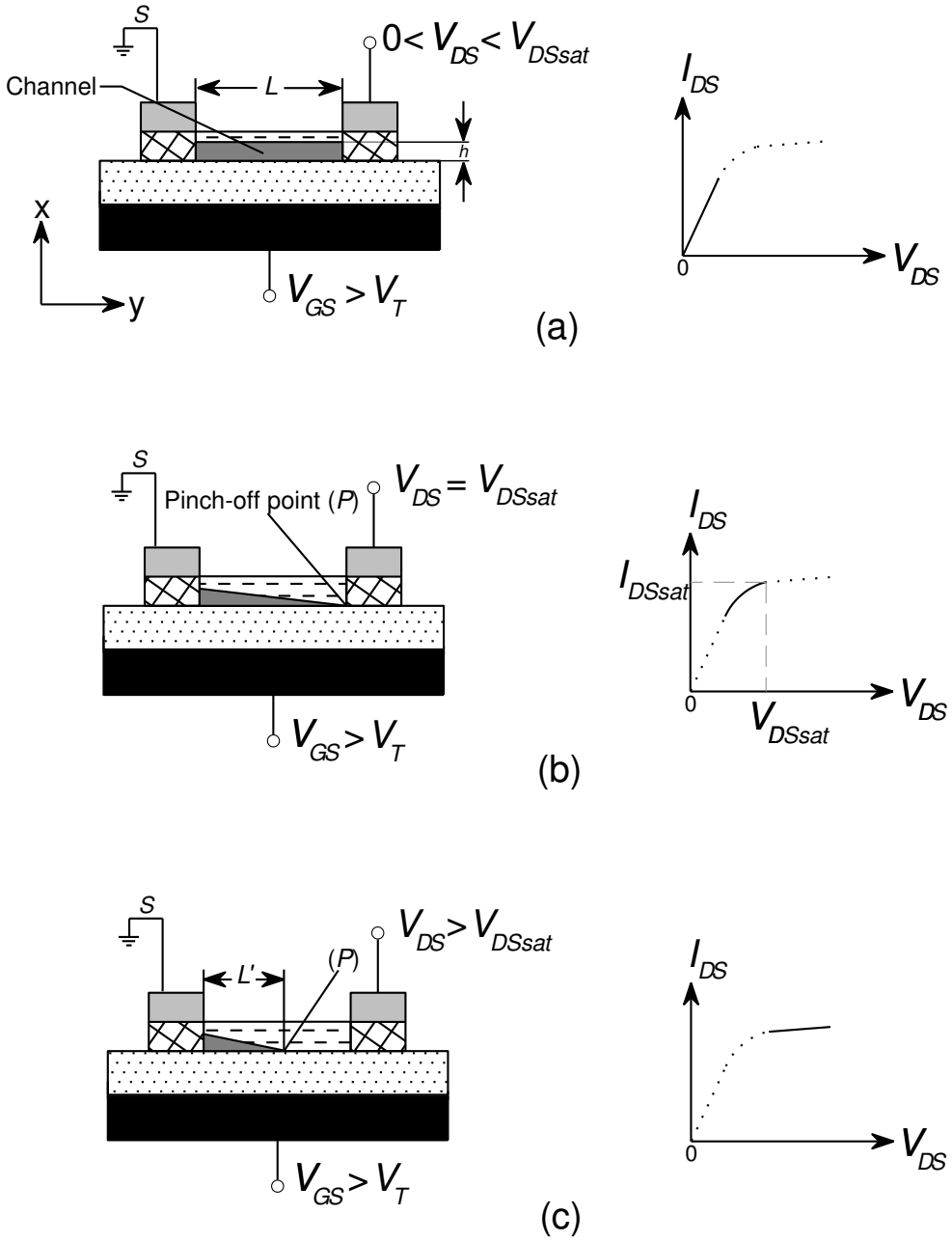


Figure 2.3: Schematic diagram of TFT operation and its output characteristics under different drain voltage conditions: (a) linear region, (b) onset of saturation, (c) beyond saturation.

negative voltage $V_{GS} = V_T = -et_s n_0/C_G$ (where t_s is the semiconductor thickness, n_0 is the initial charge density in the semiconductor, and C_G is the gate capacitance per unit area ($C_G = \epsilon_i/t_i$ with insulator dielectric constant ϵ_i and thickness t_i)) in order to deplete electrons in the channel and achieve negative threshold voltage value to get negligible off-current [8]. Normally-off devices dissipate less power and are more widely used due to easier circuit

design than normally-on ones.

In 1963, Borkan and Weimer [13] reported their theoretical considerations on I-V characteristics, the so-called square-law model. Their essential assumption was gradual channel approximation (GCA), which was developed in 1952 by Shockley to analyze the junction field-effect transistor and then extended to the whole family of FETs [14]. GCA assumes that vertical electric field $\xi(x)$ across the channel is much larger than the horizontal field $\xi(y)$ along the channel. This assumption is valid for FETs with small dielectric thickness and long channel length, but it fails for the modern MOSFETs with very short channel lengths. As for TFT case, GCA is applicable because dielectric thickness is usually about 250-300 nm, while channel length around 5-100 μm is almost thousand times larger.

There are also other main assumptions made in formulation of TFT I-V characteristics: (1) thickness of the semiconductor layer is sufficiently small to regard it as the thickness of the induced channel, i.e. $t_s \simeq h$, (2) electric field is zero at the back interface of the semiconductor layer, (3) carrier mobility, μ, is constant along the channel, (4) D/S contacts are ohmic, (5) gate capacitance, C_G, is constant and independent of the gate voltage, (6) channel current is dominated by the drift current, (7) the initial carrier density in the semiconductor is n_0. As a result of this model (see Appendix A for the complete derivation of the ideal square-law model) channel current depends on both drain and gate voltages in the pre-pinch-off regime:

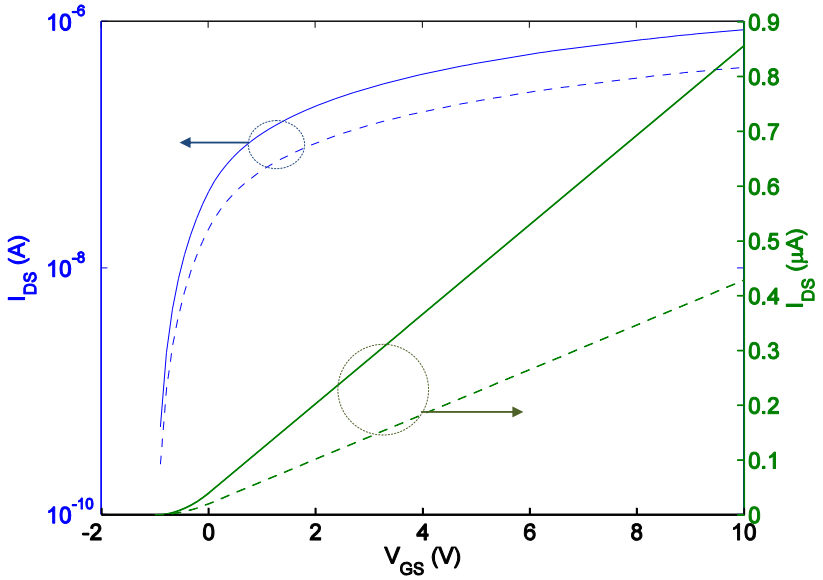
$$I_{DS} = \frac{W\mu C_G}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right], \quad (V_{DS} < V_{Dsat}) \tag{2.1}$$

where W is the channel width (see Figure 2.1-a,b). For the drain voltage equal to $V_{DS\,sat} = V_G - V_T$ channel is pinched off and further increase in V_{DS} (post-pinch-off regime) does not change the voltage at point P, in other words current saturates:

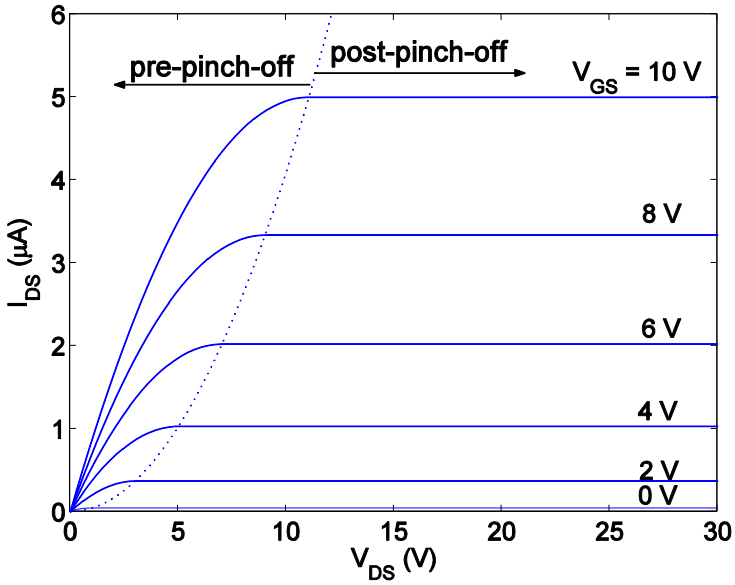
$$I_{DS\,sat} = \frac{W\mu C_G}{2L}(V_{GS} - V_T)^2, \quad (V_{DS} \geq V_{DS\,sat}) \tag{2.2}$$

Here drain current does not depend on drain voltage but has quadratic dependence on gate voltage giving name to the "square-law" model.

The simulated transfer and output $I - V$ characteristics using the ideal square-law model are demonstrated in Figure 2.4. Note that in Figure 2.4-a increasing mobility increases I_{DS} at a given V_{GS} value and changes the slope towards more abrupt I_{DS} turn-on.



(a)



(b)

Figure 2.4: Simulated (a) transfer ($log(I_{DS}) - V_{GS}$: blue, $I_{DS} - V_{GS}$: green curves) and (b) output ($I_{DS} - V_{DS}$) characteristics of n-channel TFT using the ideal square-law model. Here model parameters are taken as: $W/L = 8$ with $L = 50$ μm, $C_G = 20$ nF/cm^2, $V_T = -1$ V, $\mu = 0.5$ cm^2/Vs. In (a) $V_{DS} = 1$ V and dashed curves correspond to $\mu = 0.25$ cm^2/Vs, in (b) V_{GS} is decreased from 10 to 0 V in 2 V steps and dotted curve corresponds to pinch-off values, $V_{DS\,sat}$'s.

2.2 Limitations of Ideal Square-Law Model

In real TFT devices series resistance at the D/S (R_D/R_S) may result in I_D decrease, which in turn gives out mobility value less than the actual one [15]. With inclusion of R_D/R_S into the ideal square-law model the value of $V_{DS\,sat}$ also increases leading to higher pinch-off voltage. Figure 2.5 shows these effects of R_D/R_S on the TFT $I-V$ characteristics.

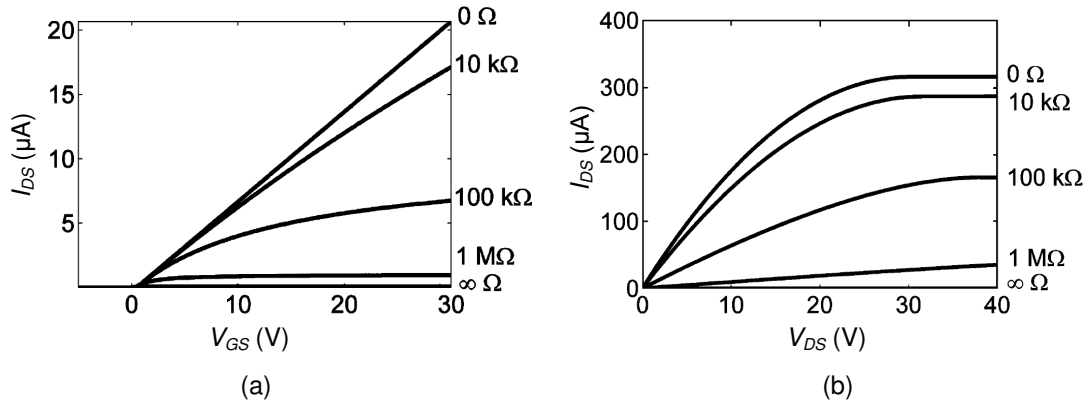


Figure 2.5: Simulation of TFT (a) transfer (at $V_{DS} = 1$ V) and (b) output (at $V_{GS} = 30$ V) characteristics for varying values of series resistance ($R_{SERIES} = R_S + R_D = 0\ \Omega$, 10 kΩ, 100 kΩ, 1 MΩ, ∞ Ω, and $R_S = R_D$). Here model parameters are taken as: $W/L = 10$, $C_G = 700$ nF/cm^2, $\mu = 10$ cm^2/Vs, $t_s = 100$ nm, $n_0 = 10^{14}$ cm^{-3} [15].

When the initial concentration of free carriers in the bulk of the semiconductor channel (N_D) is high, in addition to the induced channel path of square-law model ($I_{DS,IND}$) two conduction paths through the channel bulk ($I_{DS,BULK}$) and back interface ($I_{DS,BACK}$) can be introduced as resistors, thus forming 3-layer model (see Figure 2.6). These two extra paths are not affected by the gate voltage modulation, therefore with increase in N_D, $I_{DS} - V_{DS}$ curves show small variation with respect to V_{GS}. As N_D decreases, the portion of $I_{DS,IND}$ increases and $I_{DS} - V_{DS}$ curves are closer to the ideal ones. As it can be seen from the simulation in Figure 2.6-b, there no "hard" saturation as in the ideal square-law model. The reason is that 3-layer model assumes that channel can not be fully depleted (because of two extra paths) and to recover this the comprehensive depletion-mode model is proposed, which accounts for the depletion region formed near the drain (for details see the work of Hong *et al.* [15]).

As real TFT channel is made of amorphous material and may contain lattice mismatching at the interface with dielectric, there is high density of defects, which should be involved in the TFT electrical modeling. To simplify derivation, instead of distribution of traps over a

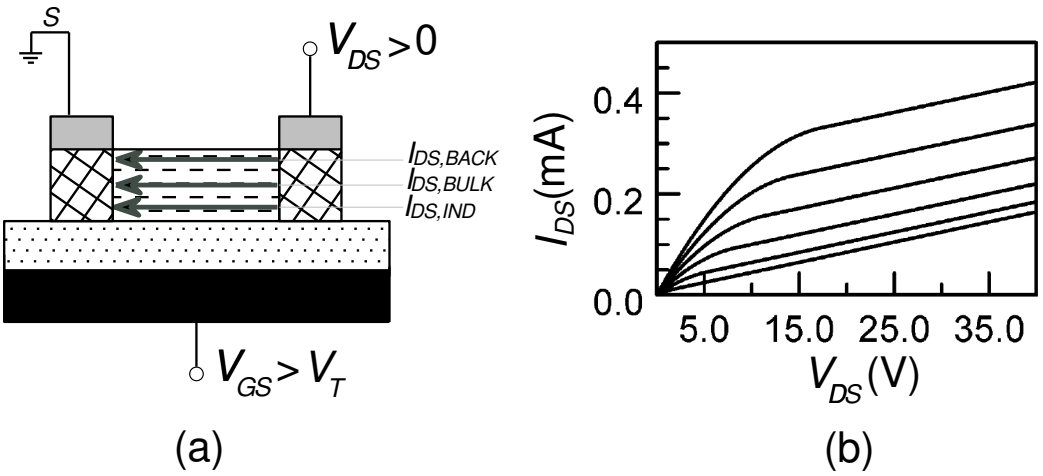


Figure 2.6: (a) Schematic representation of 3-layer model for n-channel TFT. (b) Simulation of TFT output characteristics using 3-layer model. Here model parameters are taken as: $W/L = 5$, $C_G = 700$ nF/cm^2, $\mu = 0.5$ cm^2/Vs, $t_s = 100$ nm, $R_{BACK} = 10^9$ Ω, $N_D = 10^{18}$ cm^{-3} resulting in $V_T = -(qt_sN_D)/C_G = -2.3$ V and $R_{BULK} = L/(q\mu N_D t_s W) = 2.5 \times 10^5$ Ω [15].

specific energy interval discrete trap model is used. The derivation of discrete trap model is provided in Appendix A. The resulted constraint equations and pinch-off equation are similar to the ideal square-law model, but the drain current equations are much more complex due to inclusion of trap effects. The trapping of channel carriers is responsible for subthreshold, above-threshold trends and mobility degradation, which are thoroughly discussed in section 2.4. It was considered in ideal square-law model that leakage current, I_L, i.e. drain current at $V_{GS} < 0$ and $V_{DS} > 0$, is zero. However, in the real case the increase in magnitude of negative V_{GS} enhances I_{OFF}, as shown in Figure 2.7. The reasons for such high conductivity is associated usually with field- and trap-assisted mechanisms that are dominant at the drain-gate overlap region. Poole-Frenkel (PF) emission of carriers from traps inside the semiconductor channel occurs when applied electric field lowers the potential around the trap and drain leakage current is exponentially dependent on the electric field:

$$I_L = I_{L0}\exp(\beta_{PF}\sqrt{\xi}), \tag{2.3}$$

where ξ is the vertical electric field across the drain-gate overlap region, I_{L0} and β_{PF} are coefficients, described in ref. [7]. PF conduction is the typical mechanism for leakage current when ξ is below 2.2 MV/cm (or $V_{DS} < 10$ V) [17]. At higher electric fields the region in drain vicinity is almost fully depleted and trap-assisted band-to-band tunneling becomes the

dominant mechanism:

$$I_L = C\xi\exp(-E_0/\xi), \tag{2.4}$$

where C and E_0 are the constant and tunneling parameter described in [17].

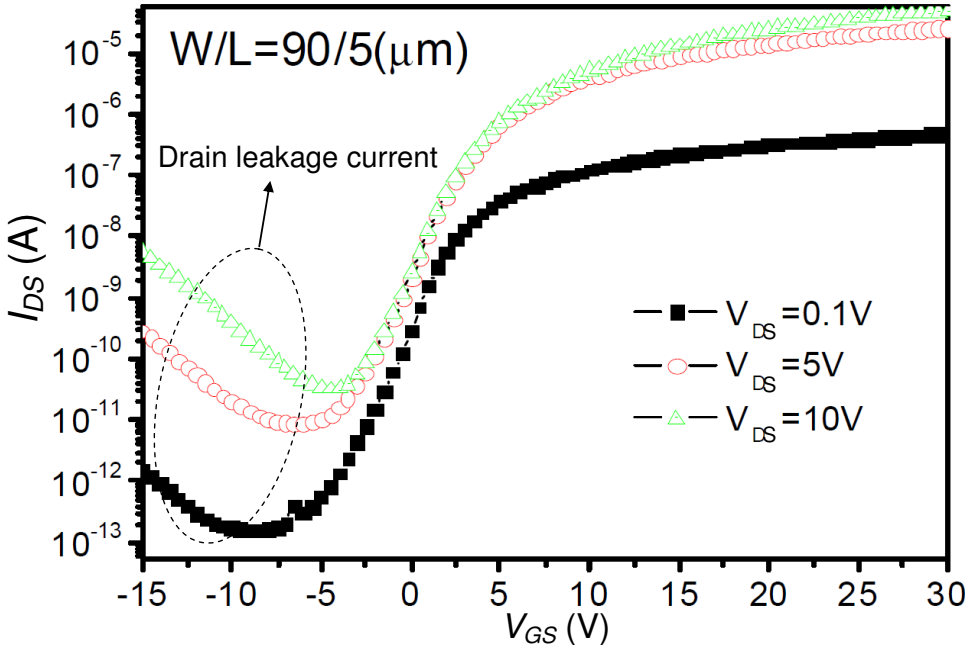


Figure 2.7: Experimental transfer characteristics of bottom-gate nanocrystalline Si TFT with indicated leakage current [16].

2.3 Various TFT Structures

Basic TFT structures are divided into two cases depending on whether D/S contacts and gate dielectric are located w.r.t. the channel on the same (coplanar, Figure 2.8-a, b) or opposite sides (staggered, Figure 2.8-c, d). In the former current flows directly from drain to source remaining in one plane, in the latter there is also a vertical flow from D/S towards the induced channel. Also for different deposition sequences there are top-gate (Figure 2.8-a, c) and bottom-gate or inverted (Figure 2.8-b, d) structures. Other TFT structures, shown in Figure 2.8-e, f, are alternative structures. In dual-gate TFT (Figure 2.8-e) an extra metal gate (meaning extra cost) is deposited over the passivating nitride, thus doubling the current. Interestingly, the current was found to be higher than the arithmetic sum of the separate currents due to low penetration of electric field deeply inside the channel layer resulting in higher effective mobility according to reduced interface roughness scattering [18]. In vertical TFT

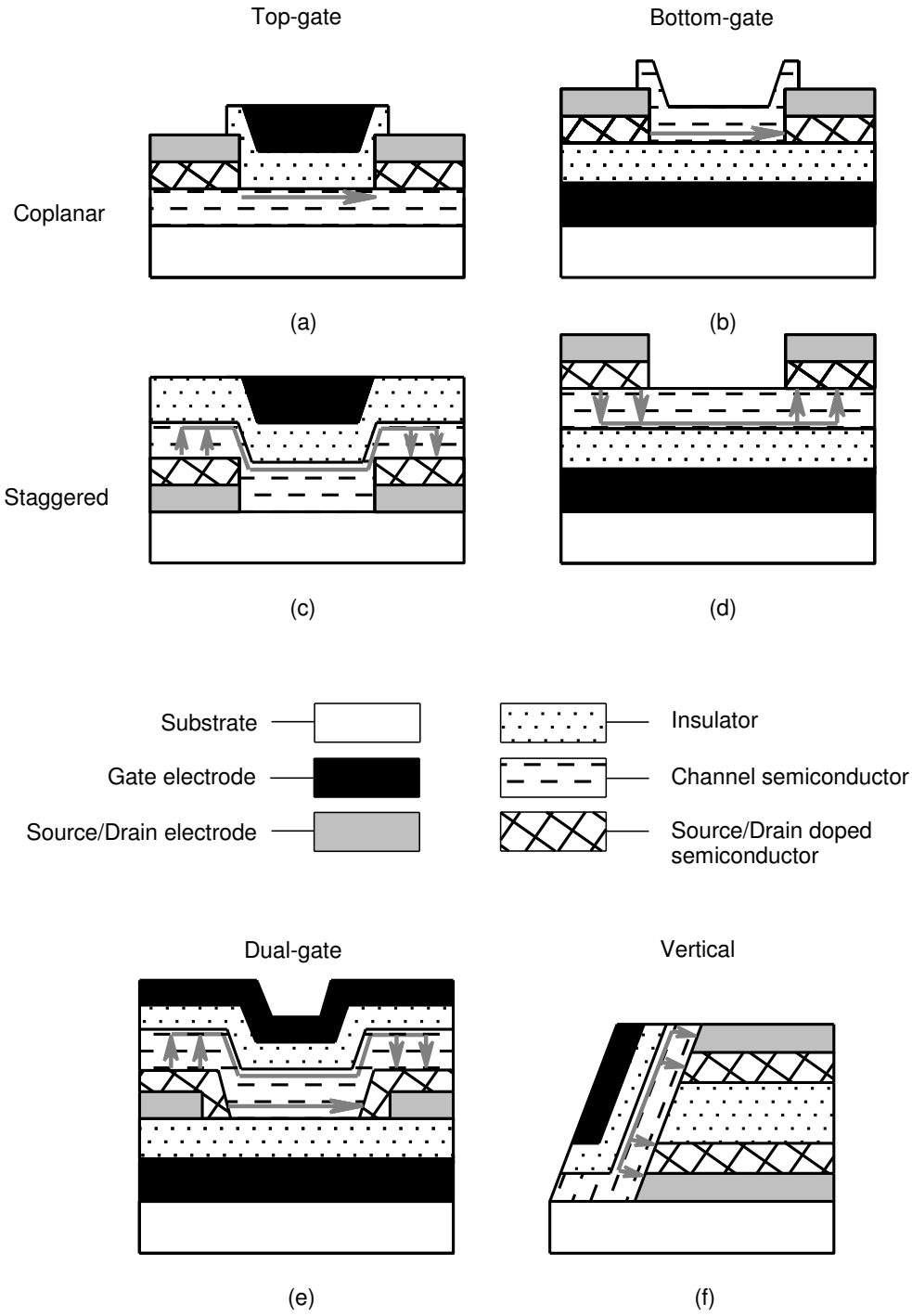


Figure 2.8: Basic TFT structures: (a) coplanar top-gate, (b) coplanar bottom-gate (or inverted), (c) staggered top-gate, (d) staggered bottom-gate. Alternative TFT structures: (e) dual-gate, (f) vertical. Arrows describe the conduction path through the induced channel.

current is increased by reducing channel length now determined rather by insulator thickness than by photolithographic patterning process (lower limit ~10μm) used in the horizontal TFT structure. However, in this vertical structure off-current is very high due to large horizontal area of the D/S contacts relative to the insulator thickness [19].

As can be seen from the Figure 2.8, the induced current path in staggered structure differs from the path used in derivation of the ideal square law (see Figure 2.1) in that it has vertical components towards D/S contacts. However if the channel layer thickness (t_s) is sufficiently small these components can be neglected [2], so that equations 2.1 and 2.2 are still valid.

2.4 TFT Parameter Extraction

The following parameters are extracted from the experimental data of TFTs: threshold voltage (V_T), subthreshold slope (SS), I_{ON}/I_{OFF} ratio, mobility (μ), electrical stability. However, their physical explanations should be clarified further.

2.4.1 Threshold Voltage

There are two parameters describing the onset of drain current depending on their extraction from $I_{DS} - V_{GS}$ curve: V_T is estimated from the linear extrapolation of $I_{DS} - V_{GS}$, while V_{ON} corresponds to the appreciable drain current found from $log(I_{DS}) - V_{GS}$ (see Figure 2.9). Clearly, V_{ON} is the onset of the drain conduction, which can be expressed through the initial density of carriers present in the TFT channel at zero bias ($V_{GS} = 0$). V_T is rather the demarcation point, which separates subthreshold current (when $V_{GS} < V_T$) from more appreciable, above-threshold current (when $V_{GS} > V_T$). Therefore, the previously described V_T in TFT models should be replaced by V_{ON}, but one must keep in mind that usually the reported values of threshold voltage are extracted from the linear extrapolation of $I_{DS} - V_{GS}$ curve. Subthreshold slope (SS) is defined as $SS = \frac{\partial V_{GS}}{\partial log(I_{DS})}|_{\min}$, describing the effectiveness of V_{GS} to reduce I_{DS} to zero or gate leakage value. So, ideally $SS = 0$ and abrupt transition from on-current (I_{ON}, maximum I_{DS}) to off-current (I_{OFF}, gate leakage or minimum I_{DS}) occurs. Besides, in ideal TFT, $V_T = V_{ON}$ due to the lack of trapping and I_{ON}/I_{OFF} ratio (should be as large as possible to reach effective switch) is infinite since the gate leakage is ignored [15].

Considering the discrete trap model the turn-on voltage is given by $V_{ON} = -\frac{qt_s}{C_G}(n_{c0} + n_{T0})$, where n_{c0} and n_{T0} are the initial (at zero V_{GS}) densities of free conduction band (CB) and trapped electrons, respectively. Within the framework of discrete trap model, V_T is the gate

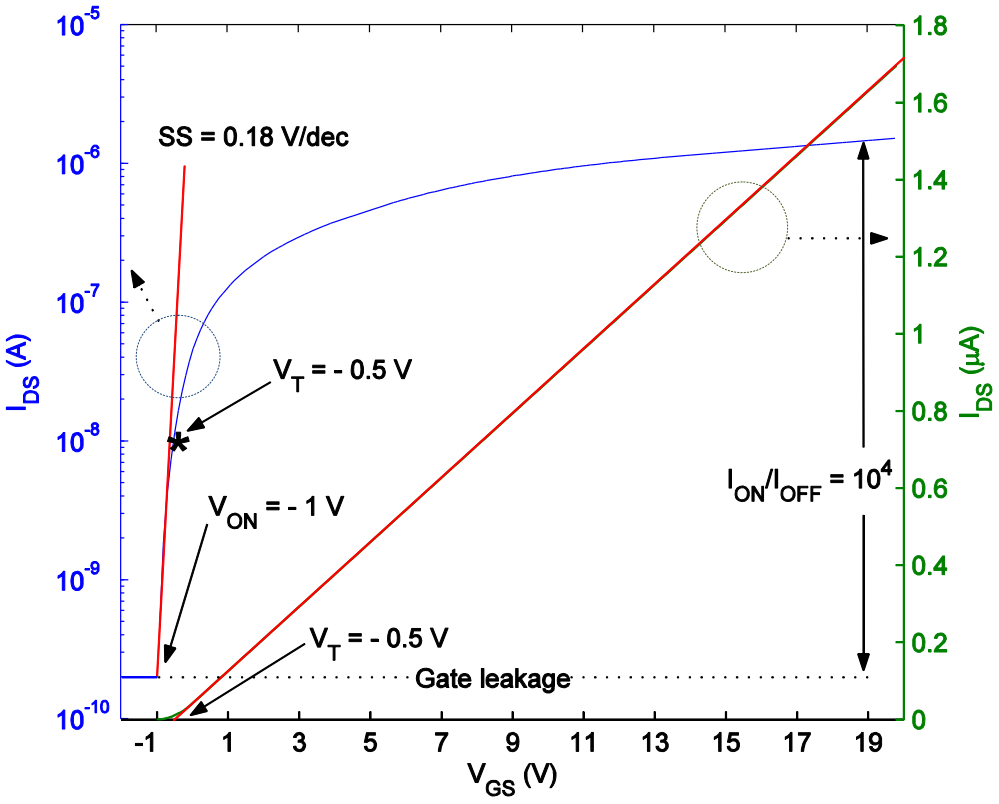


Figure 2.9: Simulated transfer ($log(I_{DS}) - V_{GS}$: blue, $I_{DS} - V_{GS}$: green curves) characteristics of n-channel TFT using the ideal square-law model. The red lines are used to extract V_T, V_{ON} and SS parameters. The "*" indicates the position of V_T on the $log(I_{DS}) - V_{GS}$ curve and obviously does not correspond to the onset of the drain current, as it is in the case of V_{ON}. Here model parameters are the same with those used for the solid curves in Figure 2.4-a.

voltage at which all the traps are filled and consequently the Fermi level (E_F) approaches the trap level:

$$V_T = \frac{qt_s}{C_G}(N_T - n_{T0}) + \frac{qt_s}{C_G}(n_1 - n_{c0}) = V_{TRAP} + V_{CB}, \tag{2.5}$$

where V_{TRAP} is the voltage required to fill the empty traps ($N_T - n_{T0}$), V_{CB} is the voltage required to fill the CB with electron density up to n_1 (the CB electron density when $E_F = E_T$) [15]. As a result, when V_{GS} increases from V_{ON} to V_T, E_F moves closer to E_T and steady-state trap occupancy increases. So, the slope of $log(I_{DS}) - V_{GS}$ curve between V_{ON} and V_T is trap-controlled and non-zero SS results, as shown in Figure 2.10-a. At $V_{GS} > V_T$ E_F moves above E_T and free electrons accumulate only in CB, so that the shape of this portion of $log(I_{DS}) - V_{GS}$ curve is not affected by the trap presence. A kink near V_T, not present

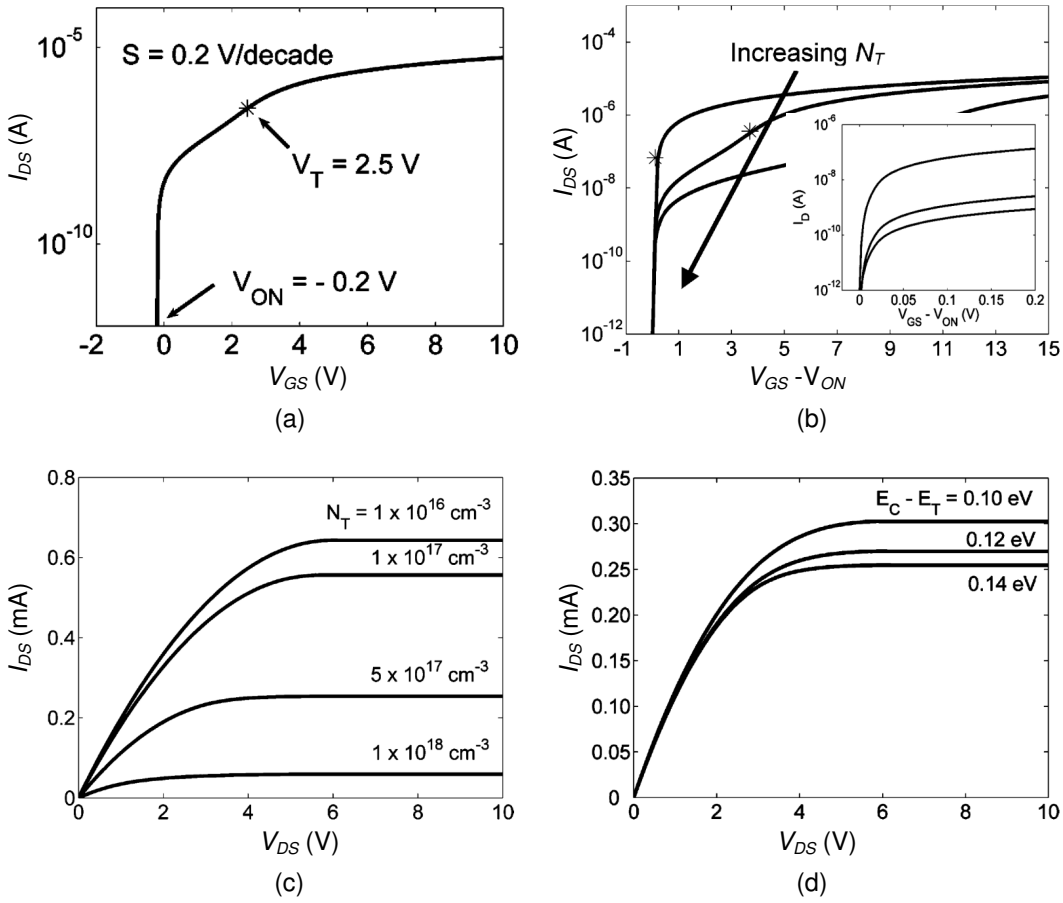


Figure 2.10: Simulated (a-b) transfer ($log(I_{DS}) - V_{GS}$) and (c-d) output ($I_{DS} - V_{DS}$) characteristics of n-channel TFT using the discrete trap model. Simulated $log(I_{DS}) - V_{GS}$ in (a) and (b) deviates from the real curve by the presence of the kink in the current near V_T. The "*" in (b) indicates the position of V_{TRAP} on the $log(I_{DS}) - V_{GS}$ curve and inset shows the increase in SS with increasing N_T. In (c) $E_C - E_F = 0.21$ eV. Other simulation parameters are given in ref. [15].

in real case, may stem from the discrete trap assumption [15]. The effect of trap density on $log(I_{DS}) - (V_{GS} - V_{ON})$ characteristics is provided in Figure 2.10-b. As N_T increases I_{DS} degrades, while V_T and SS increases. Besides, increase in N_T, causing increase in filled trap density (n_T), reduces free electron density available for conduction and consequently affects the above-threshold current by decreasing I_{DS} (see Figure 2.10-c). Also, the deeper energy depth of a trap ($E_C - E_T$) causes larger reduction in I_{DS} when E_F is below E_T (see Figure 2.10-d). This is due to decrease in trap re-emission of more deep traps (remember that $e_n = \sigma_n v_{th} N_c e^{-E_T/k_B T}$). Energy of states with E_T below E_F does not affect much the drain current [15].

2.4.2 Mobility

In the derivation of all TFT models up to now the channel mobility, μ ($\mu = \frac{v_{drift}}{\xi}$), has been taken as a constant. Considering the real case, μ can vary with V_{DS} and V_{GS} due to interface surface roughness, electron trapping, velocity saturation and etc. So, several definitions of mobility due to its dependence on voltage exist. In literature there are usually two parameters, which differentiate by their extraction from the measured data: effective mobility (μ_{EFF}) is found from the drain conductance (g_d) in the linear regime, while field-effect mobility (μ_{FE}) is derived from transconductance (g_m). Since the linear regime of $I_{DS} - V_{DS}$ curve at specific V_{GS} is close to very small V_{DS} values (see Figure 2.11-a), I_{DS} in this regime is approximated from equation 2.1 by dropping the quadratic term of V_{DS}:

$$I_{DS} \approx \frac{W\mu C_G}{L}\left[(V_{GS} - V_T)V_{DS}\right]. \tag{2.6}$$

Then, $g_d = \frac{\partial I_D}{\partial V_D} \approx \frac{W\mu C_G}{L}(V_{GS} - V_T)$ and:

$$\mu_{EFF} = \frac{g_d}{(W/L)C_G(V_{GS} - V_T)}. \tag{2.7}$$

To find μ_{FE}, I_{DS} of equation 2.1 is differentiated with respect to V_{GS} yielding exact expression for transconductance (see Figure 2.11-b) and field-effect mobility:

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{W\mu C_G}{L}V_{DS}, \tag{2.8}$$

$$\mu_{FE,lin} = \frac{g_m}{(W/L)C_G V_{DS}}, \tag{2.9}$$

where $\mu_{FE,lin}$ is the field-effect mobility in the linear region of $I_{DS} - V_{GS}$. When TFT is in the saturation regime, equation 2.2 is valid and one can define $g_{sat} = \frac{\partial\sqrt{I_{DS}}}{\partial V_{GS}}$ corresponding to the slope in Figure 2.11-c, and field-effect mobility in saturation regime is:

$$\mu_{FE,sat} = \frac{2g_{sat}^2}{(W/L)C_G}. \tag{2.10}$$

In addition to the above definitions, there is average mobility, μ_{AVG}, which differs from μ_{EFF} only in V_T replaced by V_{ON}:

$$\mu_{AVG} = \frac{g_d}{(W/L)C_G(V_{GS} - V_{ON})}. \tag{2.11}$$

μ_{AVG} has more physical interpretation, since it corresponds to the average mobility of the *total* carrier concentration in the channel, including carriers localized in traps. As it is seen from Figure 2.11-b, the use of small V_{DS} to find g_m can give more accurate result due to easy determination of the region where I_{DS} changes linearly with V_{GS}. However, it is necessary to

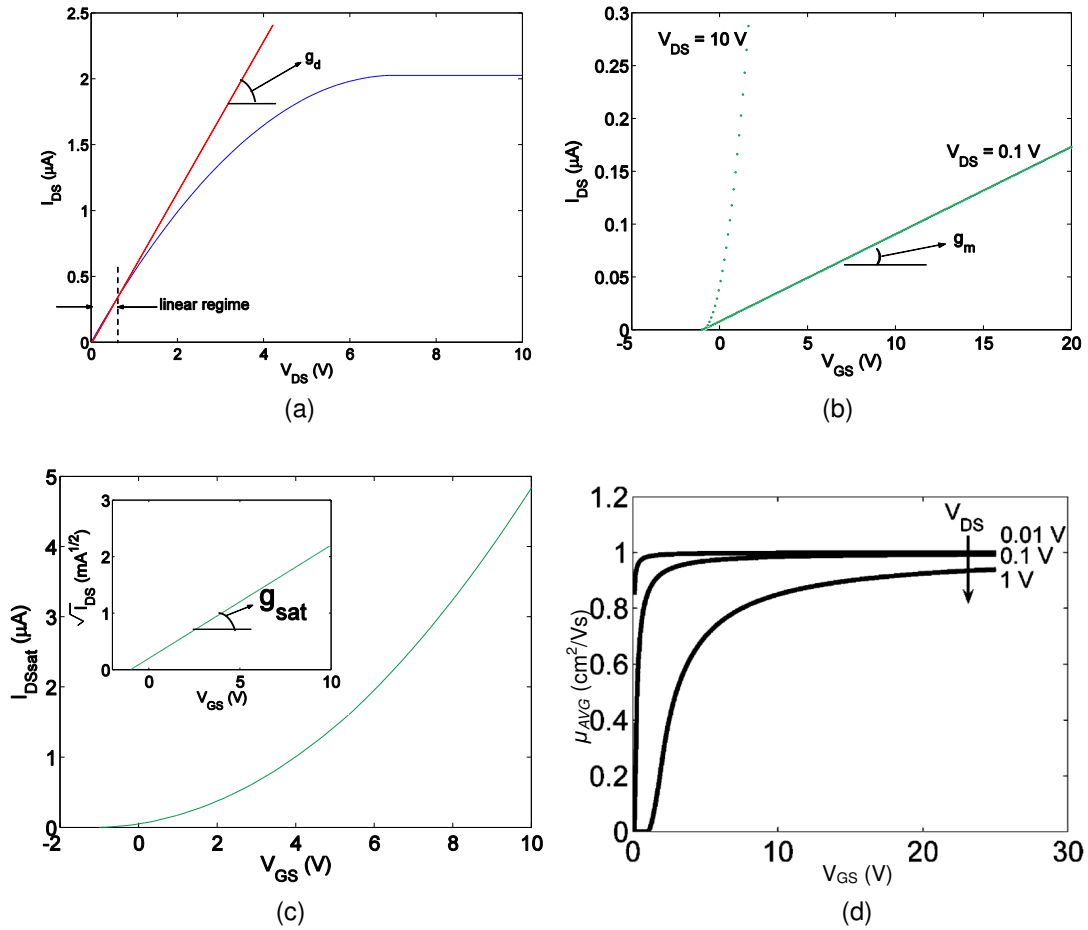


Figure 2.11: (a) Simulated $I_{DS} - V_{DS}$ with $V_{GS} = 6$ V. The red line corresponds to the linear regime with the slope g_d leading to μ_{EFF}. (b) Simulated $I_{DS} - V_{GS}$ on linear scale with $V_{DS} < (V_{GS} - V_T)$. g_m is the slope of linear region, which identifies $\mu_{FE,lin}$. (c) Simulated $I_{DS} - V_{GS}$ on linear scale with $V_{DS} > (V_{GS} - V_T)$. g_{sat} is the slope of saturation region of $\sqrt{I_{DS}} - V_{GS}$ curve shown in the inset, which identifies $\mu_{FE,sat}$. Square-law model parameters are given in Figure 2.4. (d) $\mu_{AVG} - V_{GS}$ extraction from square-law modeled curve depends on V_{DS} value due to approximation made for g_d [15].

use sufficiently small V_{DS}, usually 0.1 V, to get μ_{AVG} value close to the ideal one (see Figure 2.11-d) because of the above approximation in equation 2.6:

$$\mu_{AVG} = \mu_{IDEAL} \frac{(V_{GS} - V_{ON} - V_{DS})}{(V_{GS} - V_{ON})}. \tag{2.12}$$

To measure the mobility of carriers that are incrementally added to the channel as V_{GS} incrementally increases, another definition of such apparent incremental mobility, μ_{INC}, is also adopted:

$$\mu_{INC} = \frac{\frac{\partial g_d}{\partial V_{GS}}}{(W/L)C_G}. \tag{2.13}$$

For example, its degradation due to series resistance can be modeled [15]; but to find actual mobility decrease due to interface roughness scattering under large V_{GS} or mobility measurements after all traps are filled μ_{AVG} must be used. It should be also noted here that the usual report on TFT contain $\mu_{FE,lin}$ and $\mu_{FE,sat}$.

2.4.3 Stability

Electrical stability of TFTs, i.e. the change of I_{DS} with time under prolonged voltage stress, is very important for d-TFTs and not so crucial for s-TFTs, which are subjected to bias for a very short time. The decrease in I_{DS} for TFT working in saturation regime causes the shift of V_T ($\Delta V_T = V_T(t) - V_T(0)$, where $V_T(0)$ is the initial threshold voltage) by equation 2.2. There are two main reasons for instability phenomena in TFTs: (a) defect creation in channel layer and (b) charge trapping in the gate dielectric [20]. For example, it was proposed that metastability in a-Si:H channel is caused by hydrogen atom diffusion leading to the stretched-exponential time dependence of ΔV_T:

$$\Delta V_T = (V_{GS} - V_T(0)) \left\{ 1 - \exp\left[-\left(\frac{t}{\tau} \right)^{\beta} \right] \right\}, \tag{2.14}$$

where τ is temperature dependent time constant, β is fitting exponent and TFT is under usual stressing conditions: $V_{DS} = 0$ V, while $V_{GS} \equiv V_{STRESS} \equiv V_T(\infty)$. Since the usual stressing time is less than $\tau \sim 10^7$ sec, the above equation can be approximated as:

$$\Delta V_T \approx (V_{GS} - V_T(0)) \left[\frac{t}{\tau} \right]^{\beta}. \tag{2.15}$$

This shift in threshold voltage is a reversible process, i.e. TFT can be annealed under 423 K for several hours (but at RT it may take a year [20]) and generated defects are passivated by hydrogen again retrieving the old TFT characteristics.

It was found that subthreshold slope SS is not affected by the charge trapping in dielectric, i.e. gate dielectric affects TFT characteristics under large V_{GS} values. As it is shown in Figure 2.12, several mechanisms are responsible for carrier trapping in dielectric. However, since TFT operates at relatively low electric field, 1-3 mechanisms in Figure 2.12 are believed to be dismissed because they are limited to higher fields [21]. The dependence of ΔV_T on time in this case is considered to be logarithmic [21], although other researches make use of equation 2.14 to explain charge trapping phenomena in dielectric [20]. Experimentally it is found that defect creation is dominant at voltages less than 15−20 V (depending on the bandgap of the dielectric) and at shorter stress time, while at higher bias values and longer stress time only

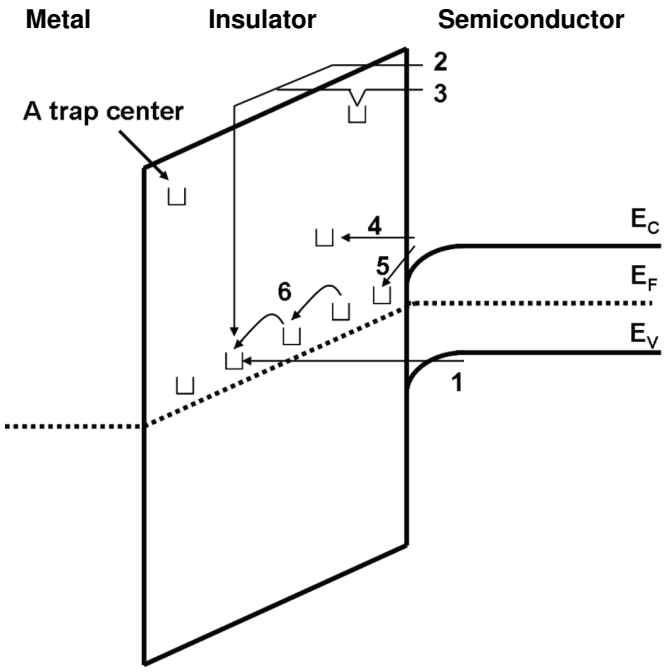


Figure 2.12: Charge trapping mechanisms in metal-insulator-semiconductor (MIS) structure of TFT: 1 - direct tunneling from valence band, 2 - Fowler-Nordheim injection, 3 - trap-assisted injection, 4 - constant-energy tunneling from silicon conduction band, 5 - tunneling from conduction band into traps close to E_F, and 6 - hopping at the Fermi level [21].

charge trapping in the gate dielectric causes the shift of V_T. The two reasons for ΔV_T can be compared by their dependence on RT reversibility and temperature: charge trapping is reversible under relaxation at RT and is weakly temperature-dependent, while defect state creation does not recover $I_{DS} - V_{GS}$ curve at RT and is highly temperature-dependent.

To summarize the above discussion on TFT parameters, a "good quality" s-TFT should exhibit at least the following performance parameters: μ_{FE} of ~0.5 cm^2/Vs, I_{ON}/I_{OFF} ratio of $10^5 - 10^6$, SS of <2 V/dec, V_T of ±(1-5) V. Besides these values, the high electrical stability is crucial for d-TFT, exhibiting, for example, $\Delta V_T \sim 0.1$ V for 3×10^4 sec under $V_{GS} = 10$ V [16].

CHAPTER 3

TFT COMPONENTS

3.1 Electrode Material

Conductor requirements for TFTs are summarized as follows: low resistivity, especially important for gate electrodes to prevent gate delay; thickness of the gate electrode for bottom-gate TFT must be less than 300 nm to prevent short-circuit between gate and data lines; low mechanical stress to prevent cracking or delamination; low sensitivity to wet and dry etching of other TFT materials; thermally stable under deposition of subsequent TFT thin films; good ohmic contacts with n^+ doped drain/source (D/S) [22]. Metals such as aluminium (Al), molybdenum (Mo), chromium (Cr), copper (Cu), tantalum (Ta), indium tin oxide (ITO), indium zinc oxide (IZO) are commonly used as gate and D/S materials because of their high temperature stability. However, there are some practical problems. Al and Mo has poor chemical durability, high diffusion into n^+ doped nc-Si:H layer. Cr has low resistivity and is widely used in TFT LCDs, but when sputter-deposited its high tensile stress should be reduced by deposition parameters. Cu has poor adhesion to glass surface, hillocks on its surface and is chemically unusable. Ta has large resistivity and to reduce its value it requires underlayer, such as Mo. Due to its transparency property and low resistivity, ITO can be used for the source electrodes in LCD TFTs, since source electrode is directly connected to the LC pixel electrode, which is required to be transparent for the backlight of LCDs [22]. As a result gate electrodes are generally produced of Cr, Mo, ITO. The thickness of the D/S electrodes for bottom-gate TFT can be increased in order to reduce resistance and it is not as critical as for gate electrode. Here fabrication of good ohmic contacts is critical, therefore usually low-diffusion metals are used, such as Cr, Mo, Ta. But to reduce resistance Al (possessing low resistivity of $\sim 10^{-6}$ Ωcm) is evaporated above these metals forming dual-layered D/S

contacts: Al/Cr, Al/Mo, Al/Ta. Besides, these contacts may be produced of only Mo but with high thickness because of its poor selectivity with nc-Si:H wet etch.

There are different types of metal coating systems: sputtering, electron-beam evaporation, resistive evaporation and etc.

Also different shaped electrodes depending on TFT fabrication masks can be produced: in self-aligned TFT structures there is no overlap between D/S and gate electrodes (see Figure 2.8-a, c), which minimizes parasitic capacitance (especially C_{GS}) present in non self-aligned TFTs (see Figure 2.8-b, d).

3.2 Dielectric Material

Following the MOSFET technology, amorphous silicon oxide (a-SiO_x) thin films were used as TFT gate dielectric material [23, 24]. In order to deposit thin film components of TFTs low-temperature plasma-enhanced chemical vapor deposition (PECVD) method is industrially utilized. Nowadays, reduction in the deposition temperature is inevitable, particularly for the fabrication of TFTs on flexible plastic substrates. Because of such low deposition temperatures (below 623 K), a-SiO_x films (especially those deposited at 423 K) have poor dielectric properties and high trap density leading to the electrical instability in TFT [24, 25]. Amorphous silicon nitride (a-SiN_x), as a counterpart of a-SiO_x, is commonly used for both gate dielectric and passivation material in silicon based TFTs, and it has higher breakdown field, higher deposition rate and lower density of states at the interface between insulator and channel layers. Works on the improvement of a-SiN_x dielectric properties so far agree on the superiority of slightly nitrogen rich films (with N/Si ratio above the stoichiometric one of 1.33) [26–28]. Films with N/Si ratio around 1.5-1.7 have highest weight density and resistivity [27,29]. Since the gases used for deposition of a-SiN_x contain hydrogen (ammonia-NH_3, silane-SiH_4), the resulted films are hydrogenated by 10−40% [30]. Hydrogen content decreases with increasing substrate temperature (T_s) and power density. The role of hydrogen in these films is to passivate dangling bonds (DBs) by forming Si−H and N−H bonds. However its content should be minimized to shorten the etch time during photolithographic process [26] and to increase the film resistivity [27]. Moreover, a-SiN_x:H films with lowest hydrogen content (with hydrogen preferentially bonded to nitrogen) exhibit high TFT mobility and electrical stability [27]. Surface roughness of a-SiN_x:H also affects the interface properties of bottom-gate TFTs: it decreases the TFT mobility [26]. To reduce the surface

roughness, a high hydrogenation and a high plasma power should be avoided. Even so, in TFTs with two sequential gate dielectrics (generally have higher mobilities than those with only one dielectric layer) the preferred dielectric layer that directly contacts with the channel is a-SiN_x:H, since it has both good physical and chemical interface properties (a low interface state density, $\sim 10^{11}$ $eV^{-1}cm^{-2}$). Besides, the deposition conditions of the channel layer above a-SiN_x:H affect the interface and consequently the whole TFT performance. Therefore the deposition power density should be controlled and some surface treatments before starting the channel layer deposition can be done. For example, it was reported that a hydrogen plasma treatment of a-SiN_x:H surface at an RF power density of 90 $mWcm^{-2}$ for 5 minutes resulted in an improved mobility, I_{ON}/I_{OFF} ratio and electrical stability of a-Si:H TFTs [31]. It was also found that the increase in the deposition rate of a-SiN_x:H with increasing power density stops near the critical power ($W_{critical}$) and then the deposition rate decreases with the further increase in power, i.e. the etching mechanism becomes more dominant [26]. Not only the deposition rate but other film properties exhibit changes near the $W_{critical}$: lowest refractive index (n), (N−H)/(Si−H) bond ratio and mechanical stress [26]. Nevertheless, if the large area uniformity of TFTs is considered, the deposition power should be below the $W_{critical}$ [26]. a-SiN_x:H films provide good dielectric and good interface properties with a high (HDR) and low (LDR) deposition rates, respectively. Therefore, some studies on the bottom-gate TFTs used HDR films for the bottom insulator and above them LDR films for a direct connection with the channel layer [32].

Adopted gas sources for a-SiN_x:H thin film deposition are SiH_4, NH_3, N_2 and H_2. Smith *et al.* analyzed the growth kinetics of a-SiN_x during its deposition from NH_3-SiH_4 [33] and from N_2-SiH_4 [34] gas mixtures, respectively. The growth mechanism from N_2-SiH_4 gas mixture was further "corroborated and refined" by Kessels *et al.* [35]. In NH_3-SiH_4 case, disilane (Si_2H_6) is found to be the main product in plasma for a low power density without dependence on the high NH_3/SiH_4 flow ratio (usually taken around 10−20 to get nitrogen rich films). At a high power density (100 $mWcm^{-2}$) and a high chamber pressure Si_2H_6 was not detected, while tetra-aminosilane ($Si(NH_2)_4$) molecules and tri-aminosilane ($Si(NH_2)_3$) radicals were dominant products within the plasma. It was concluded that the presence of aminosilanes results in the films with a more dense structure, with excess N and eliminated Si−H bonding [33]. Therefore, a high power density and NH_3/SiH_4 flow ratio lead to desirable dielectric properties of a-SiN_x:H. Under amino-saturated conditions the two-staged reaction was proposed, i.e. precursor-forming stage within the plasma is followed

by a surface condensation reaction under the effect of the substrate temperature: SiH_4 + $4NH_3 \xrightarrow{plasma} Si(NH_2)_4$+ $4H_2$; $3Si(NH_2)_4 \xrightarrow{heat} Si_3N_4$ + $8NH_3$. However, usually instead of $Si(NH_2)_4$ molecules $Si(NH_2)_3$ radicals are formed or $Si(NH_2)_4$ lose their NH_2 group easily during the absorption process. Besides, the second reaction does not completely occur even at 803 K, meaning that proposed "condensation zone" depicted in Figure 3.1 is almost absent for films deposited at about 473 K. Therefore, at low T_s the formation of the stretched Si−N bonds instead of the volatile NH_3 is less probable, giving out zero mechanical stress and excess of H in the film bulk [33]. In contrast to NH_3−SiH_4, N_2−SiH_4 gas mixture forms no Si−N precursors within the plasma. Surface reaction of SiH_3 radicals (forming a-Si:H-like outermost surface layer) with N radicals contributes to the film growth and it has nearly

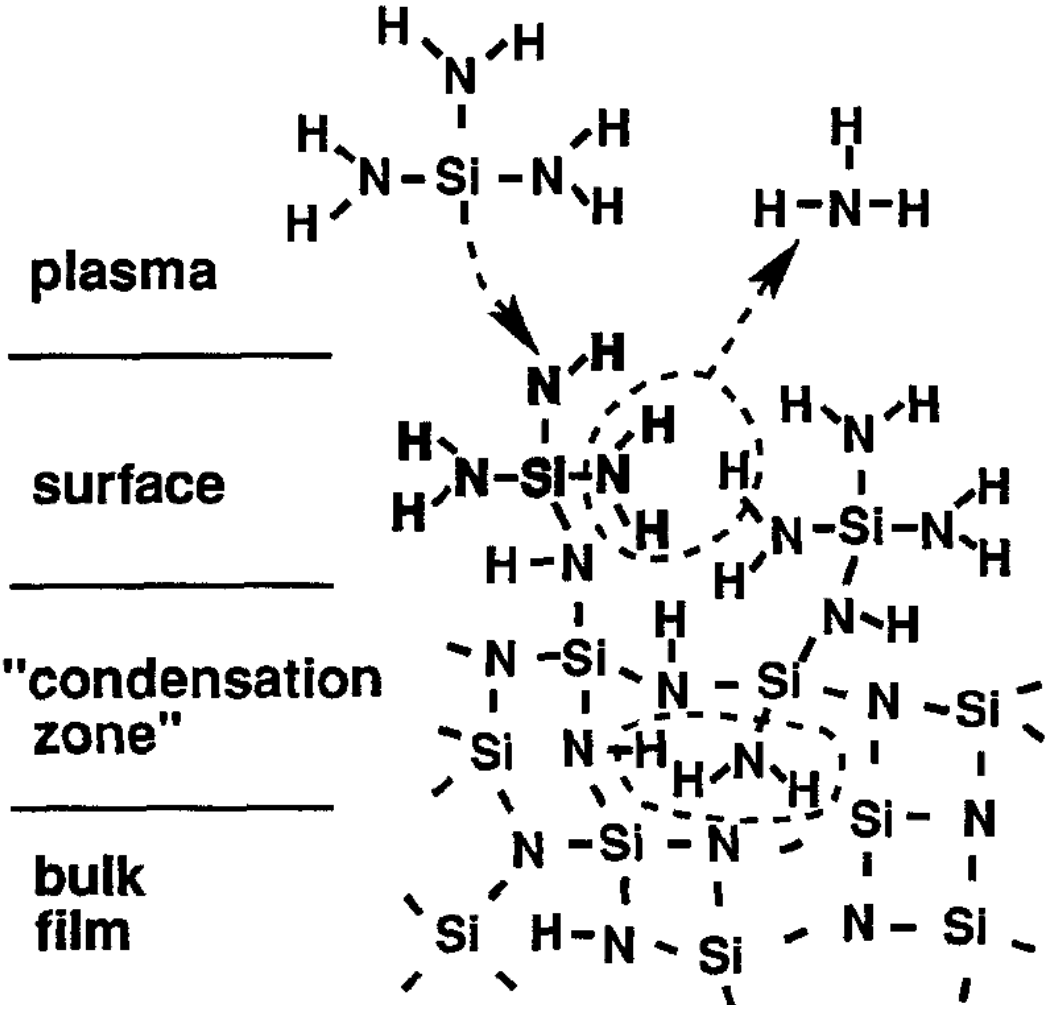


Figure 3.1: Growth model of the a-SiN_x:H from NH_3−SiH_4 reactant mixture with the condensation of adsorbed $Si(NH_2)_3$ radicals toward Si−N network with the evolution of NH_3 [33].

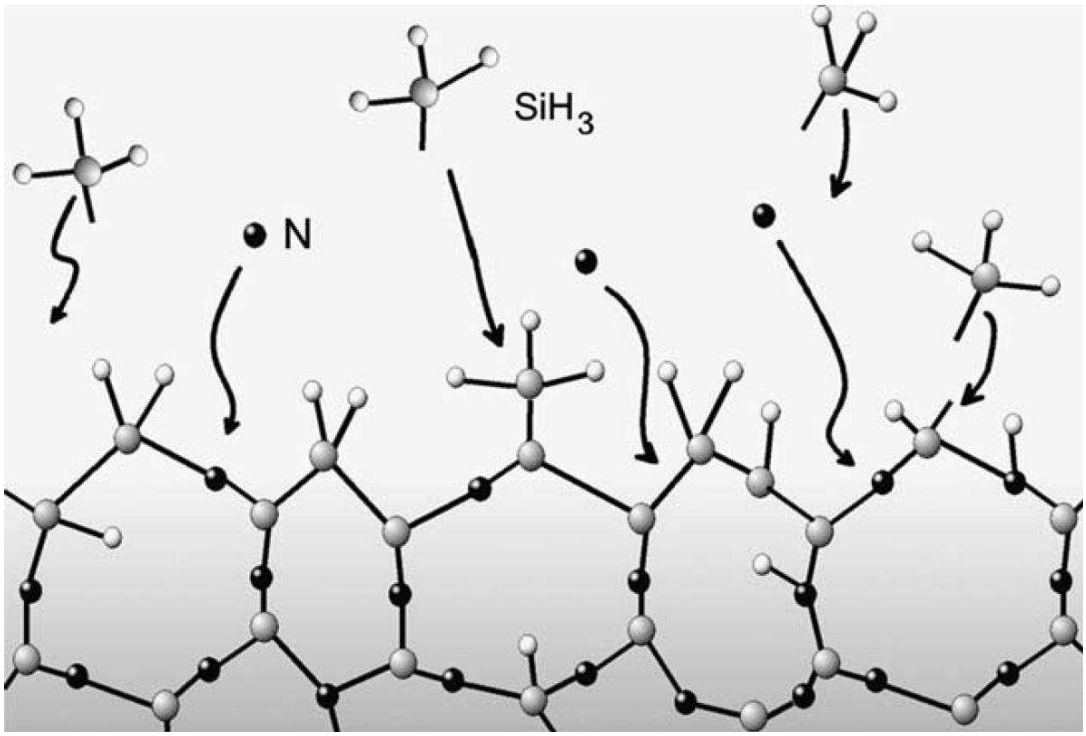


Figure 3.2: Growth model of the a-SiN_x:H from N_2-SiH_4 reactant mixture [35].

no substrate temperature dependence [34, 35]. This growth model is shown in Figure 3.2 where the contribution of Si−H and Si−H_2 radicals to the deposition is concluded to be very small [35]. Films obtained from N_2 source, when compared to those from NH_3 source, contain less hydrogen, more nitrogen, much less stress but have a poor step coverage and generally a low etch rate [34]. Addition of H_2 to the gas mixture is believed to reduce DBs, enhance the surface mobility of growth precursors and promote the deposition of a compact thin films [32].

At low T_s, required for TFT depositions on plastic substrates (<423 K), a-SiN_x:H is highly hydrogenated resulting in an increased TFT leakage current through the gate insulator. The experimental works on this issue indicate that He, Ar and/or H_2 should be added to the plasma at high RF power to achieve denser films with higher n [30]. This gas dilution increases the etch rate of weak Si−Si and Si−N bonds, so that deposition rate is reduced. Also, a-SiN_x:H are used as gas-barrier films for plastic substrates deposited on both sides of the plastic. The mechanical stress-induced bending problems, emerging because of difference in thermal expansion coefficients between a-SiN_x:H and plastic substrates, can be avoided by controlling (with different power density) the tensile-compressive stress values of bottom, top

gas-barrier and dielectric layers.

The infrared (IR) peaks reported for a-SiN_x:H thin films usually are attributed as: Si−N symmetric stretching (ν_s) peak at 470-490 cm^{-1}, Si−N in-plane asymmetric stretching (ν_{as}) peak at about 850 cm^{-1}, Si_2N−H rocking (r) peak at 1175 cm^{-1}, $SiN-H_2$ bending (δ) peak at 1530-1540 cm^{-1}, $Si-H_3$ stretching (ν) peak at 2150-2180 cm^{-1}, Si_2N−H stretching (ν) peak at 3340-3350 cm^{-1} [29, 31, 36]. IR calibration constants can be found elsewhere [36]. With the increase in nitrogen content, IR peak positions of Si−N and Si−H bonds shift towards higher frequencies (blue shift), which is attributed to the fact that Si atoms are bonded to more N ones, which have larger electronegativity than H [37]. Besides, N−H peaks become stronger and Si−H peak decreases in intensity.

Based on the literature reports, the following are the values for "good dielectric" properties of a-SiN_x:H thin films resulting in a better TFT performance: n of 1.8-2.0, dielectric constant (ε_{CV} from capacitance-voltage ($C-V$) measurements at 1 MHz) of 5.7-7.5, breakdown field (E_B) of (1-5)×10^6 Vcm^{-1}, resistivity (ρ) of (1-5)×10^{16} Ωcm, optical band-gap from Tauc's plot (E_{Tauc}) of 4.9-5.0 eV or optical band-gap E_{04} (energy at which the absorption coefficient is equal to $10^4 cm^{-1}$) of 4.5-5.0 eV [26, 27, 32, 38].

3.3 Semiconductor Material

As discussed above in the section 1.4, the use of the silicon technology has many advantages, therefore recent researches on the channel semiconductor are concentrated around silicon derivatives. Depending on the grain size, silicon materials can be divided into: hydrogenated amorphous silicon (a-Si:H), hydrogenated nanocrystalline silicon (nc-Si:H), hydrogenated microcrystalline silicon (μc-Si:H), polycrystalline silicon (poly-Si), and single crystal silicon (c-Si), as shown in Figure 3.3. Usually nc-Si:H and μc-Si:H notations are interchangeably used in the literature because of the lack of a sharp boundary between them. In this work nc-Si:H notation is adopted for films containing crystalline grains of less than 50 nm in diameter embedded in an amorphous tissue. Poly-Si are of single phase with grain boundaries and of grain sizes from ~ 200 nm to several μm. Evidently, the grain size and consequently notations are varied by the deposition conditions.

a-Si:H films are deposited under low H_2/SiH_4 (<10) gas flow ratio in PECVD system at T_s around 493−623 K, and are of single amorphous phase having only a short-range order. a-Si:H has DBs, partly saturated by hydrogen, and slight variations in bond length and/or angle,

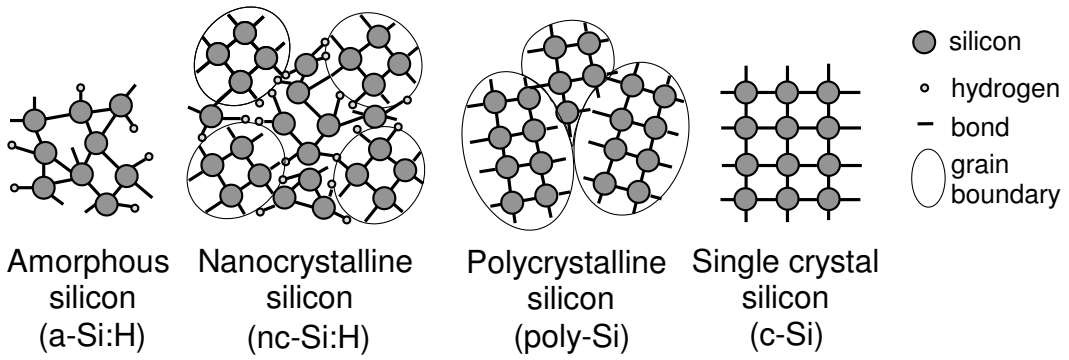


Figure 3.3: Schematic structures of silicon materials: a-Si:H, nc-Si:H, poly-Si and c-Si.

which correspond to localized deep defect states and band tail states within the energy gap, respectively (see Figure 3.4). Passivation of DBs around midgap by hydrogen atoms (H content is 10−30%) reduces the amount of deep states from $\sim 10^{20}$ $cm^{-3}eV^{-1}$ to 10^{15}-10^{16} $cm^{-3}eV^{-1}$ and also reduces tail state density by decreasing the network disorder [30]. As-grown a-Si:H films are slightly n-type. The proposed growth model for a-Si:H is schematically shown in Figure 3.5. During film-growing surface diffusion, dominant SiH_3 radical (1) attracts surface-bonded hydrogen, forming SiH_4 (2) and leaving dangling bond on the surface (growth site formation). Then another SiH_3 (3) diffuses toward the dangling-bond site on the surface and find the site to make Si−Si bond (film growth).

Poly-Si can be produced by: a) direct thermal decomposition of SiH_4 at 873 K by low-

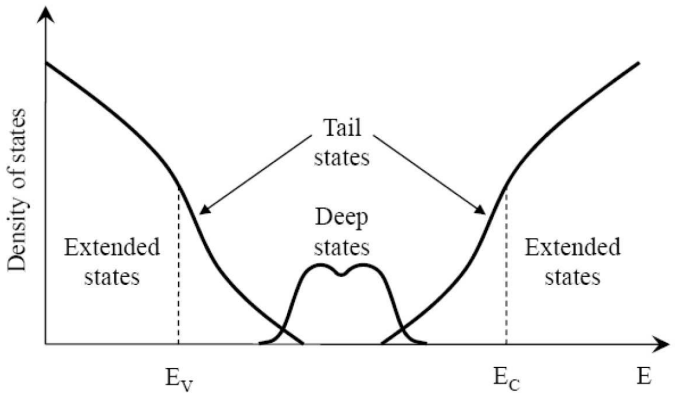


Figure 3.4: Schematic density of states (DOS) distribution in a-Si:H, nc-Si:H. Deep states have Gaussian distribution, while tail states decrease exponentially toward the midgap. Dashed lines indicate the edges of the mobility gap (pseudogap).

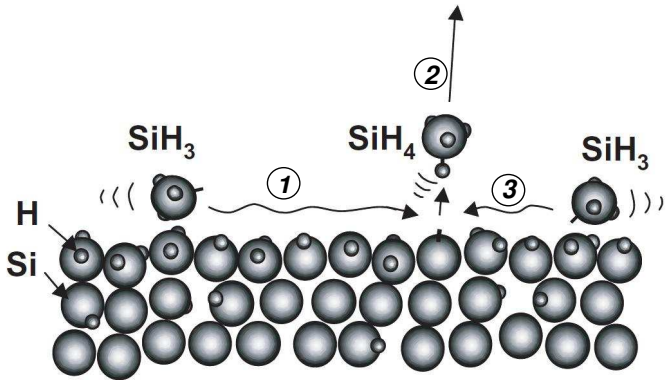


Figure 3.5: Growth model of the a-Si:H from SiH_4-H_2 reactant mixture [39].

pressure chemical vapor deposition (LPCVD), or metal-induced crystallization at temperatures lower than 873−973 K, b) crystallization from precursor a-Si:H film by its thermal annealing in the furnace at temperatures around 873−973 K or by laser annealing. Poly-Si contain much less hydrogen, which incorporates at grain boundaries during the post-fabrication hydrogenation. Larger grain sizes in poly-Si result in very high TFT mobility (> 500 cm^2/Vs for electron μ_{FE} [40]) and electrical stability. However, there are also some disadvantages. Grain boundaries of poly-Si are positioned randomly along the transistor channel leading to device performance non-uniformity over the large area [20]. Poly-Si technology is much more expensive than a-Si:H and nc-Si:H one.

Compared to a-Si:H and poly-Si, nc-Si:H TFT is an emerging low-cost technology and it was proposed to enhance the mobility and especially the stability of a-Si:H TFT required for d-TFTs in OLEDs and peripheral circuits. The nc-Si:H phase can be obtained by similar deposition conditions of a-Si:H but with an increased hydrogen dilution ratio (R_H=H_2/SiH_4). When R_H is at least 20, the formation of nanocrystallites embedded in the amorphous silicon matrix begins, forming thus a quasiordered material. It was then concluded that while SiH_3 radical is the main precursor for both a-Si:H and nc-Si:H deposition, amount of H radical is the crucial issue for nc-Si:H deposition [39]. The decision on which growth mechanisms of nc-Si:H (summarized in Figure 3.6) is dominant, depends on the deposition conditions and growth stage. In the surface-diffusion model the high hydrogen surface coverage increases the surface mobility of SiH_3 radical, which can now easily find the energetically favorable sites. Actually, hydrogen surface coverage and substrate temperature heat the radicals, but solely increased T_s (>773 K) results in a decrease of hydrogen surface coverage leading to amorphous

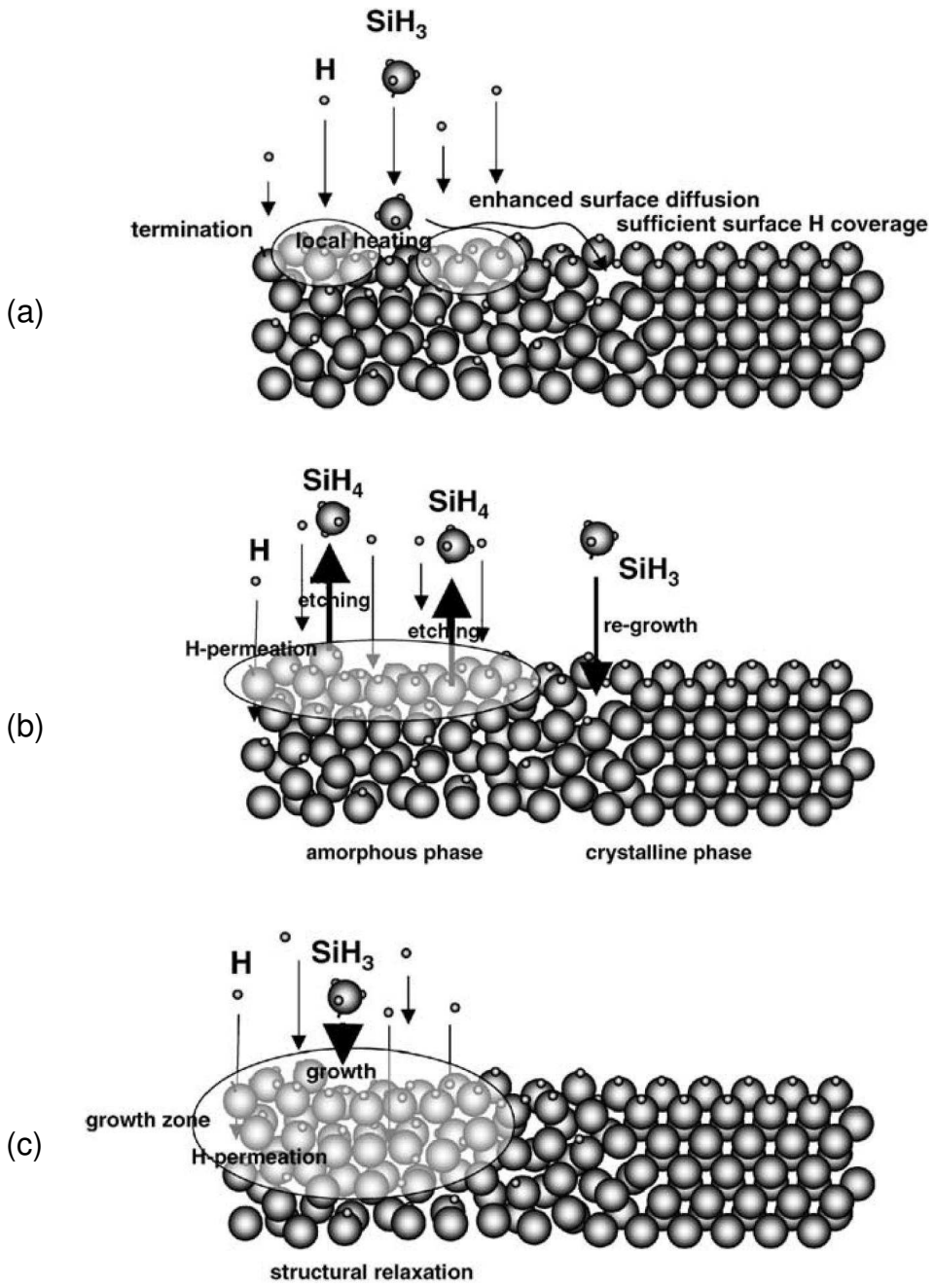


Figure 3.6: Growth models of the nc-Si:H from SiH_4-H_2 reactant mixture: (a) surface-diffusion, (b) etching, (c) chemical-annealing [39].

films. The etching model explains the decrease in deposition rate with increasing R_H: here hydrogen etches Si species from the weak Si−Si bonds, then film growth occurs when empty site is replaced by a new SiH_3 radical forming strong Si−Si bond. The chemical-annealing model was suggested to explain the absence of the remarkable decrease in the growth rate for layer-by-layer growth method. In layer-by-layer growth method H_2 is periodically introduced

when SiH_4 plasma is off and this process is repeated several times, while in a convenient continuous growth method both H_2 and SiH_4 are present within the plasma. If hydrogen is introduced for long period in layer-by-layer method etching mechanism results in almost "no-deposition", which is believed to remove the amorphous incubation layer (that may result in columnar structure, see Figure 3.7) present at the initial stage of the continuous growth. In the chemical-annealing model, hydrogen atoms permeate into the sub-surface (growth zone), induce chemical reactions that break Si−H bonds and form H_2, relaxing the silicon network without removal of Si atoms. This subsurface restructuring enhances Si network relaxation, and the subsurface transformation of a-Si:H into nc-Si:H is promoted [41].

The TFT performance becomes structure-dependent by the presence of the amorphous incubation layer at the initial stage of nc-Si:H film growth, as it is depicted in Figure 3.8. TFT mobility, for example, is now extremely different: up to 150 cm^2/Vs for top-gate TFT [23] and up to 2.8 cm^2/Vs for bottom-gate TFT [43]. The latter one is of the same order with the a-Si:H TFT mobility, which is around 0.5−1 cm^2/Vs. The use of other gases in addition to H_2, such as silicon tetrafluoride (SiF_4) and dichlorsilane ($SiCl_2H_2$), increases etchant efficiency, which produce faster and higher crystallization and decreases thickness of the incubation layer. If the thickness of the incubation layer is around 10 nm, then the nc-Si:H TFT behaves like a-Si:H TFT since the induced channel thickness is ∼10 nm [20]. The grain sizes and incubation layer depend strongly on the surface roughness of the underlying material. For example, crystallinity (X_c) of nc-Si:H deposited on the Conning 7059 is less than on the a-SiN_x:H substrate [44]. It was concluded that a 'hill-like' surface of a-SiN_x:H induces nucleation centers for nanocrystallites more than the smooth surface of the glass, which is favorable for

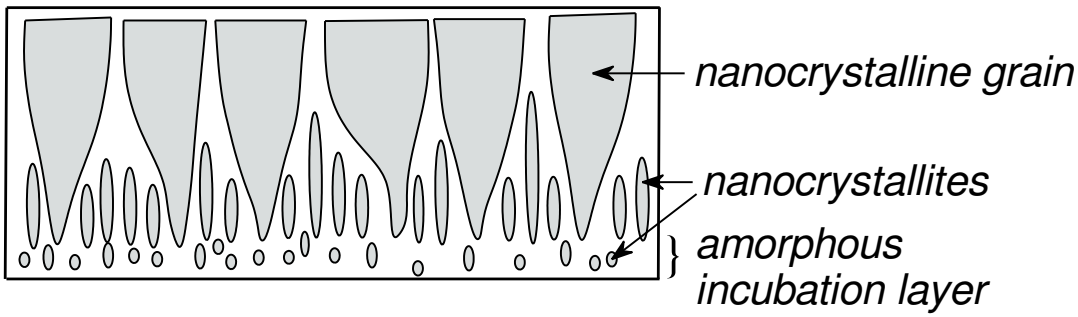


Figure 3.7: One of the possible schematic cross views of nc-Si:H film: amorphous incubation layer gradually evolves into crystallites forming columnar structure. The mobility is higher in the vertical direction (perpendicular to the substrate) than in the lateral direction (parallel to the substrate) [41, 42].

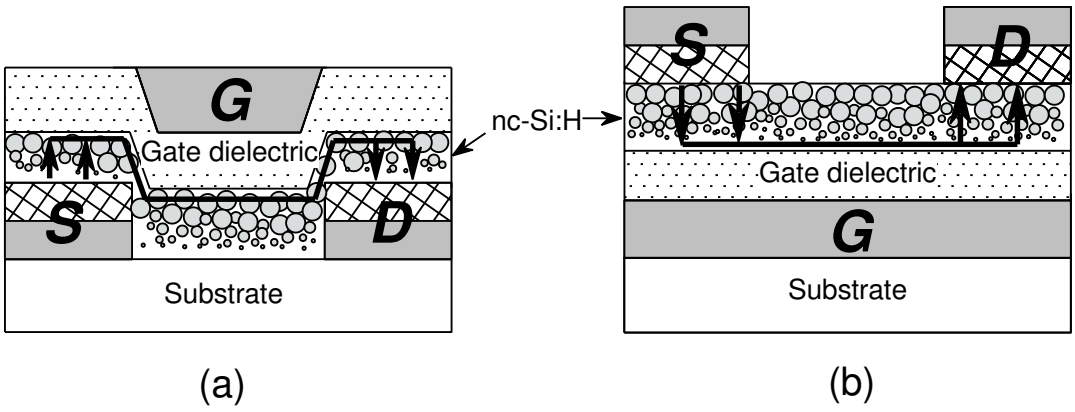


Figure 3.8: Presence of the amorphous incubation layer in nc-Si:H makes (a) top-gate TFT superior over (b) bottom-gate TFT. Arrows describe the conduction path through the induced channel.

the bottom-gate TFTs. However, the density of nucleation sites should be moderate, when it is high, the grain size of the film is small and a lot of grain boundaries along the TFT channel reduces mobility [45]. Besides, it was reported that a nitrogen and hydrogen plasma treatment of a-SiN$_x$:H increases TFT mobility [45]. Many reports agree that a high R_H value, around 100, is required to obtain X_c about 60−80%. However, a high crystallinity inside the TFT channel leads to a high dark conductivity. The high off-current in nc-Si:H TFTs (50 pA−10 nA) as compared to a-Si:H TFTs (≤0.1 pA) is one of major issues [20]. Therefore, X_c should be about 50−60% for a low dark conductivity and at the same time, a high TFT stability [44]. Also, the off-current was reduced in bottom-gate TFTs by the use of a bi-layer channel, i.e. nc-Si:H capped with a-Si:H, which diminishes band-to-band tunneling between silicon nitride passivation layer (and/or n$^+$ nc-Si:H drain) and the channel layer due to larger band gap of a-Si:H (1.78 eV) than that of nc-Si:H (1.52 eV) [20, 46]. To increase the deposition rate of nc-Si:H, while keeping a high crystallinity and low defect density, the conditions of high power density (700 mW/cm^2) and high pressure (130−250 Pa) should be satisfied [47]. But nc-Si:H deposited at such a high power density over the dielectric, can damage a-SiN$_x$:H surface and deteriorate bottom-gate TFT performance. X_c can be followed by Raman spectrum, while relative IR spectra can also give a trend of crystallinity behavior in nc-Si:H. With increased R_H value increase in crystallinity can be followed by a decrease in intensity of Si−H$_x$ stretching modes at 2000-2100 cm^{-1}, scissor-wagging modes at 890 cm^{-1} (corresponding to a-Si:H bonds) and Si-H$_x$ wagging-rocking ($w-r$) modes at 630 cm^{-1} (probably present at the grain boundaries) [47]. Overall hydrogen content in nc-Si:H is lower

than in a-Si:H contributing to a higher TFT stability.

At $T_s < 473$ K the crystallinity of nc-Si:H decreases and becomes a challenge for TFTs with plastic substrates. Recent work on nc-Si:H TFTs at T_s~423 K, used argon (Ar) gas dilution together with H_2-SiH_4 mixture to obtain highly crystalline channel with top-gate TFT mobility of 8 cm^2/Vs [48]. Other high performance top-gate TFTs at such low T_s were reported also, but instead of RF PECVD high frequency PECVD or inductively coupled plasma chemical vapor deposition (ICP-CVD) was implemented. Oxygen contamination by diffusion through the column boundaries becomes dominant at low T_s and resulted nc-Si:H is strongly n-type causing high off-current [41]. To reduce the oxygen content and increase the crystallinity of the film small amount of $SiCl_2H_2$ is added to the gas mixture.

Doping of nc-Si:H was found to be higher by 3-4 orders than in a-Si:H: crystalline phase constrains the impurities of four-fold coordination required for the substitutional doping, while in amorphous phase impurity bonds in the lowest energy configuration, with three-fold coordination, do not lead to donor states. Usually 1% of phosphine (PH_3) dopant gas in a silane mixture together with high dilution in hydrogen is used to obtain n^+ nc-Si:H [30]. To reach high quality TFT contacts both bulk and contact resistivities of n^+ nc-Si:H should be as low as possible. In this sense, n^+ nc-Si:H has low bulk resistivity of 0.1 Ωcm, but may have a high contact resistance due to a possible incubation layer of n^+ nc-Si:H. To improve contact properties post-deposition annealing of TFT at temperatures below T_s can be done.

CHAPTER 4

TFT FABRICATION

4.1 Test Samples and Other Preliminary Work

In this work bottom-gate staggered structured TFT, commonly adopted by industrial production line, was fabricated and characterized. For this purpose before TFT fabrication, sets of test samples for each of the TFT materials were produced to optimize their properties. Test films were deposited on microscope slides, quartz and silicon wafers, which were cleaned by the procedure described in Appendix B.

Firstly, ~200 nm Cr, chosen as a gate electrode, was grown on the glass substrates by the electron-beam evaporation method (see Appendix C.1). Cr coated glasses were checked for their resistance to water, because the TFT layers deposited above Cr are subjected to photolithographic steps involving water solutions.

Afterwards, test samples of gate dielectric, selected as a-SiN_x:H, were obtained by PECVD deposition (see Appendix C.2) of NH_3 and SiH_4 gases on Cr coated glasses, quartz and silicon wafers of 3500 Ωcm resistivity. The characterization methods for each test sample are depicted in the diagram of Figure 4.1. Using dot electrode mask (Figure 4.2), Al dots were evaporated above the a-SiN_x:H/Cr/glass structure by resistive evaporation technique (see Appendix C.3) to measure the electrical properties of the dielectric. Small pieces of silicon wafers were cleaned and placed on the corners of Cr coated glasses prior to the film deposition. They were removed after the film growth process was over, and revealed Cr space, which was used to measure the step from Cr to dielectric, i.e. film thickness, and to take the contact for the electrical measurements, as shown in Figure 4.1. Other optical measurements of a-SiN_x:H film and their corresponding test samples are indicated in Figure 4.1.

The test samples of intrinsic and doped layers, i.e. nc-Si:H and n^+ nc-Si:H, were deposited

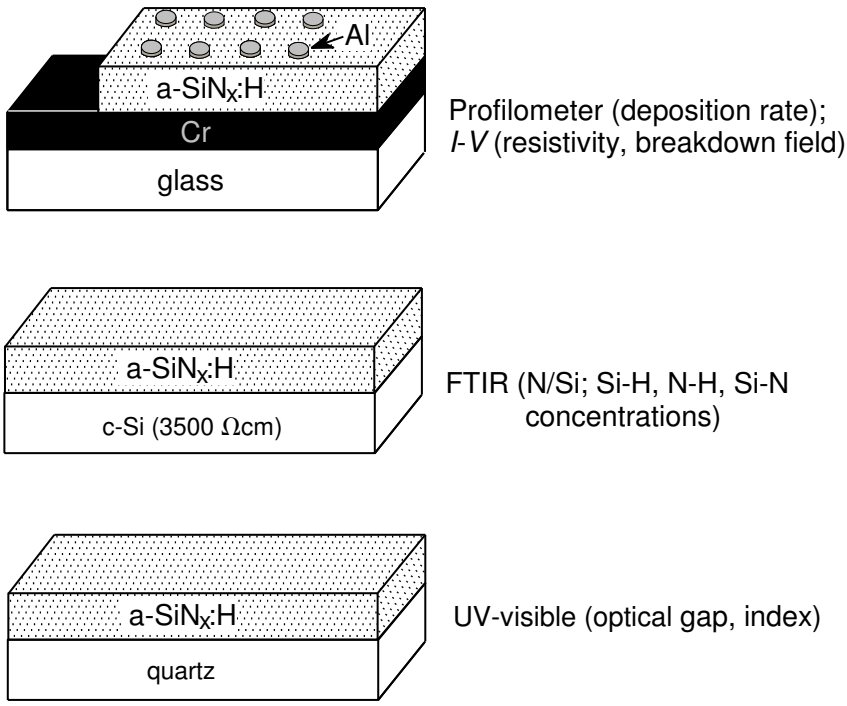


Figure 4.1: Test samples of a-SiN$_x$:H thin films and corresponding characterization techniques.

in the PECVD system on glass and silicon wafers (3500 Ωcm). For lateral resistivity measurements Al planar electrodes were evaporated above nc-Si:H/glass structures using planar electrode mask. This mask together with the dot electrode mask, shown in Figure 4.2, was fabricated from Cu foil by photolithographic method using photoresist (PR) spray, known as POSITIVE-20. The flowchart of characterization steps for nc-Si:H and n$^+$ nc-Si:H test

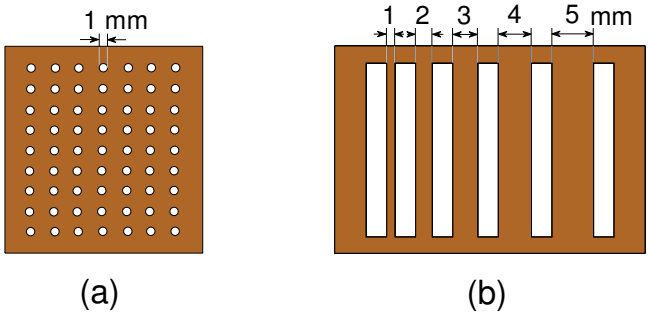


Figure 4.2: (a) Dot and (b) planar electrode mask utilized in this study for the vertical and lateral resistivity measurements of a-SiN$_x$:H and intrinsic/doped nc-Si:H thin films, respectively.

samples is provided in Figure 4.3.

Before TFT fabrication at the optimized conditions deduced from the test sample characterization results (described in chapter 5,6), TFT mask duplication was conducted. This step is done to avoid any damages to the original mask during photolithographic steps. For this, the Cr coated glass was coated by conventional PR and then exposed to UV-visible light through the original mask. The details of the photolithography method used in the mask duplication and fabrication of TFT are described in Appendix D.

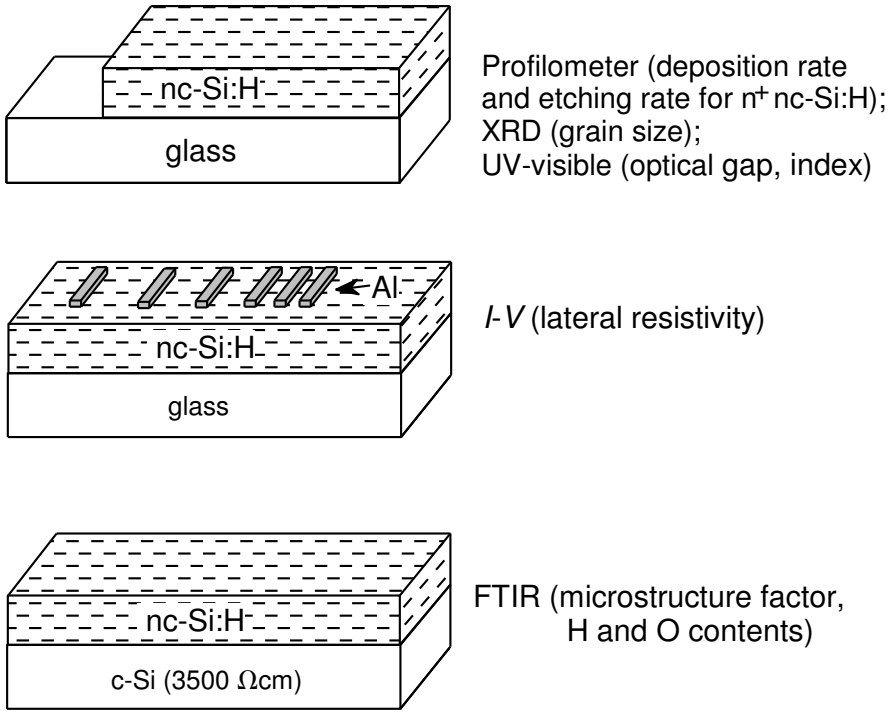


Figure 4.3: Test samples of nc-Si:H thin films and corresponding characterization techniques.

4.2 TFT Production Steps

The TFT production was performed basing on the steps depicted in Figure 4.4 using two masks: one for the drain/source (D/S) patterning and another for the TFT separation from the neighbor TFTs. Since the mask set at hand was designed for non self-aligned TFT structure, there was no gate area patterning. Therefore, the above described Cr coated glass substrates were placed into the PECVD system and then, three thin films, i.e. a-SiN_x:H, nc-Si:H and n^+ doped nc-Si:H were sequentially deposited (Figure 4.4, step 2) using the conditions described

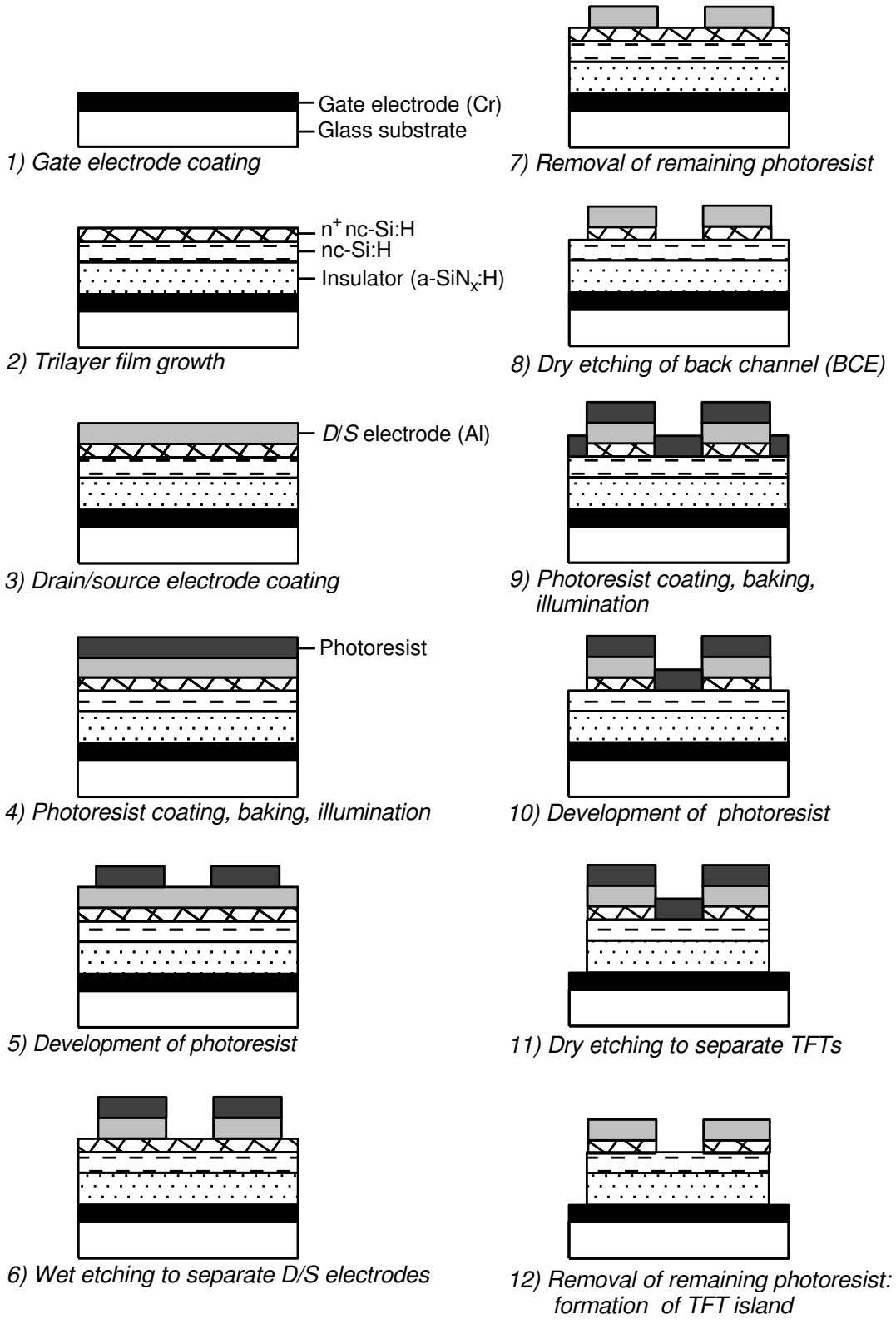


Figure 4.4: Fabrication steps of non self-aligned bottom-gate TFT structure used in this study.

in Table 4.1. In the frame of this thesis three different types of TFTs were fabricated. TFT1 and TFT2 differed only in RF power density used during deposition process of nc-Si:H layers. The dielectric growth conditions of TFT2 and TFT3 distinguished in the NH_3/SiH_4 gas flow ratio, while doped layers were deposited under different RF power density. a-SiN_x:H was grown under 0.5 Torr, and for nc-Si:H layers the chamber pressure was increased up to 1 Torr. Besides, the deposition temperature was decreased for all TFTs from 523 K to 473 K during the deposition of nc-Si:H layers.

Table 4.1: Deposition parameters of the TFTs with three layers (a-SiN_x:H, nc-Si:H and n^+ nc-Si:H) grown in one PECVD cycle.

TFT#	Film	Gases (sccm)					Chamber pressure (Torr)	RF Power density (mW/cm^2)	Substrate temperature (K)
		SiH_4	H_2	NH_3	PH_3	Total			
	a-SiN_x:H	3.9	0	75	0	78.9	0.5	100	523
TFT1	nc-Si:H	3.1	200	0	0	203.1	1	100	473
	n^+ nc-Si:H	3.1	180	0	20	203.1	1	100	473
	a-SiN_x:H	3.9	0	75	0	78.9	0.5	100	523
TFT2	nc-Si:H	3.1	200	0	0	203.1	1	300	473
	n^+ nc-Si:H	3.1	180	0	20	203.1	1	300	473
	a-SiN_x:H	3.9	0	110	0	113.9	0.5	100	523
TFT3	nc-Si:H	3.1	200	0	0	203.1	1	300	473
	n^+ nc-Si:H	3.1	180	0	20	203.1	1	160	473

Formed three layers were then coated by D/S metal, Al, in resistive evaporation system. To obtain the D/S contacts firstly Al layer was patterned (steps 4−7 of Figure 4.4) by wet etching described in Appendix D. Then dry etching by plasma (see Appendix D) was done to remove the n^+ doped nc-Si:H on the back side of the channel layer, giving name to this structure as back-channel etched (BCE). Last steps (9−12 of Figure 4.4) were performed to pattern the active area of the TFTs in order to separate TFTs from each other.

TFT mask layout used for D/S definition is presented in Figure 4.5. The length of the TFT channel was kept constant (L=50 μm), while its width, W, varied depending on the configuration and dimension of the resulted TFTs (see Figure 4.5). In this study, the configuration in Figure 4.5-a with the lowest W/L ratio was the usually measured one.

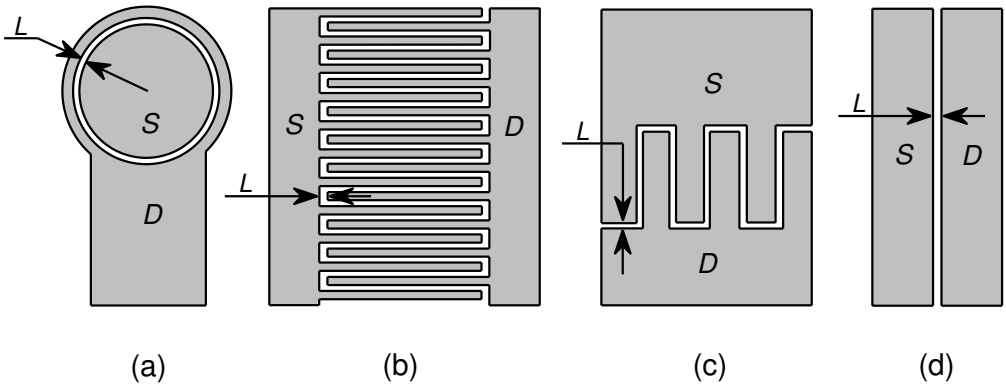


Figure 4.5: TFT mask layout utilized in the present work to define D/S electrodes. Channel length is the same (L=50 μm) for all configurations and W/L ratio varies as: (a) 130, 40, 13; (b) 1735, 160; (c) 55; (d) 9 (here L=150 μm), 8.

4.3 TFT Characterization

TFT $I-V$ testing was done using computer controllable voltage source (Keithley 230), electrometer (Keithley 617) and quasistatic $C-V$ meter (Keithley 595), which were connected to the TFT structure (island) as shown in Figure 4.6. The current function of Keithley 595 and

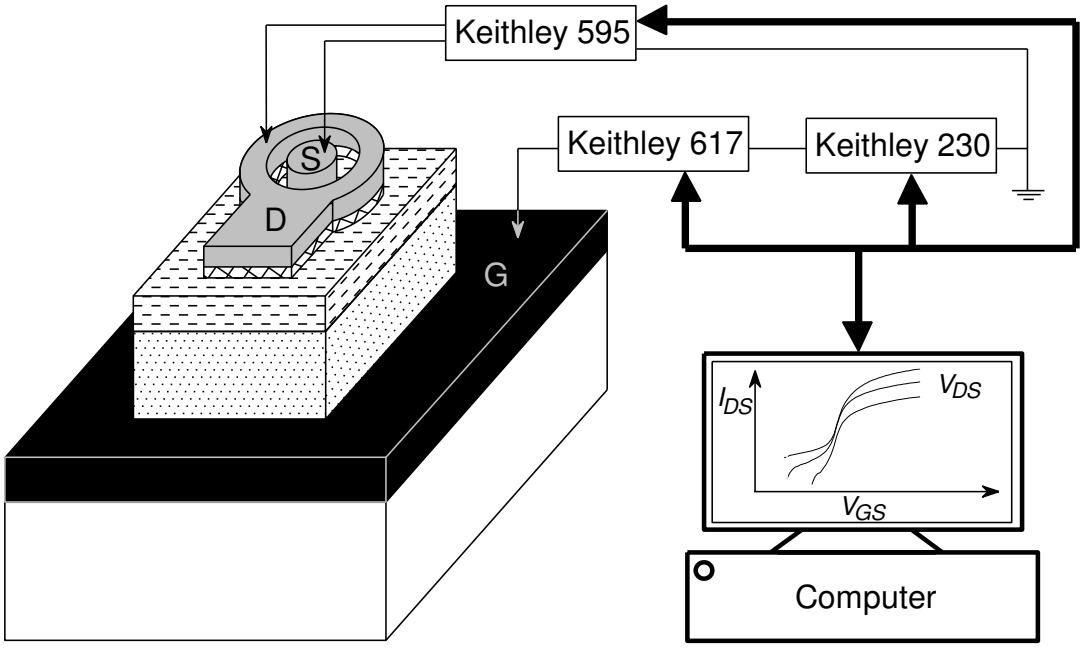


Figure 4.6: Computer controllable $I-V$ system designed for the TFT characterization in this thesis.

its voltage source were used for the $D-S$ current (I_{DS}) measurements for a given $D-S$ voltage (V_{DS}), respectively. Keithley 230 supplied voltage between G and S contacts, while $G-S$ current (I_{GS}) was measured by Keithley 617 to check the gate leakage current of TFT.

During the TFT fabrication, it was found that the TFT isolation from other TFTs on the same sample to form TFT islands (steps 9−12 of Figure 4.4) dramatically decrease the measured gate leakage current I_{GS} (Figure 4.7). The real gate leakage current is obtained after complete etching of trilayered structure until the gate metal. Before TFT separation, the application of gate voltage accumulates electrons in the nc-Si:H layer toward the interface over the whole TFT sample. Therefore at somewhat high positive gate voltage the electrons can flow through the whole sample towards the open Cr space, where the piece of Si wafer was placed during the deposition of the films and so the nc-Si:H layer is possibly weakly electrically connected to Cr. Such connection by conductive nc-Si:H layer over the whole sample is not the case after the trilayer dry etching is conducted to reveal TFT islands, separated from each other.

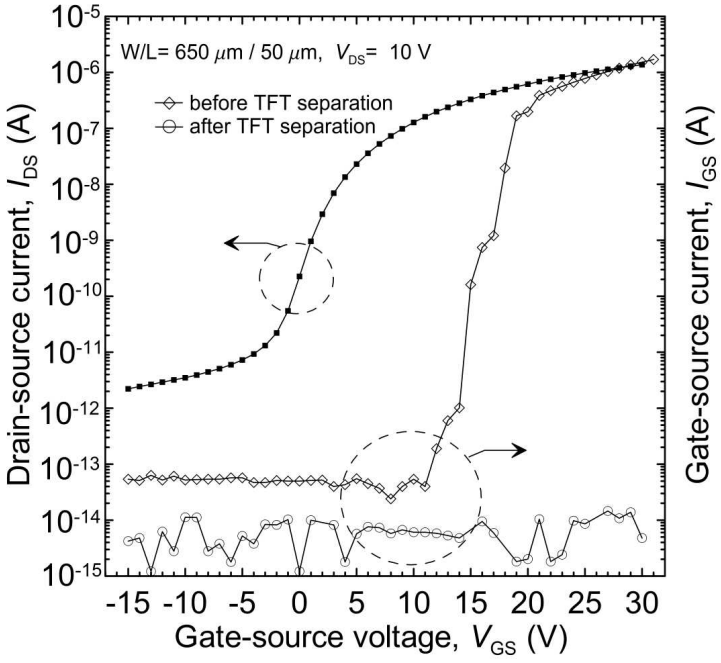


Figure 4.7: The effect of TFT isolation from other TFTs of the sample on the gate leakage current measurements.

At the end of the TFT fabrication, TFT sample was annealed at 423 K under N_2 atmosphere for 30 min in a heater system (see Appendix D). This was conducted to improve the TFT performance, as found in [49]. The change in TFT characteristics after post-deposition annealing was found as shown in Figure 4.8.

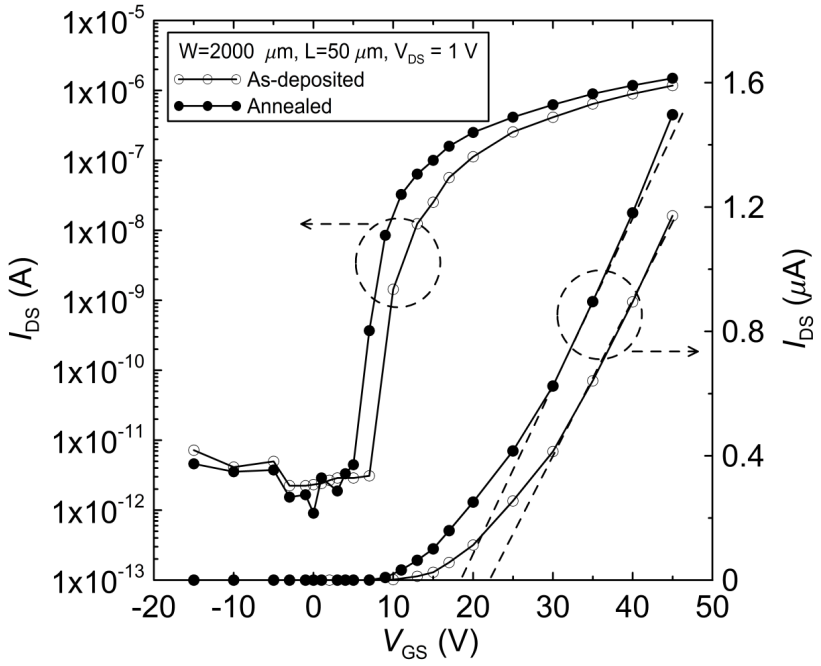


Figure 4.8: The effect of post-deposition annealing on the TFT parameters: the threshold voltage is shifted to lower value, the mobility is increased and the subthreshold slope is decreased.

CHAPTER 5

OPTIMIZATION OF n^+ nc-Si:H AND a-SiN_x:H LAYERS FOR THEIR APPLICATION IN nc-Si:H TFT

5.1 Introduction

Nanocrystalline silicon thin film transistors (nc-Si:H TFTs) are well known to have higher device mobilities compared to amorphous silicon (a-Si:H) TFTs, as it was discussed in section 3.3. However, the TFT mobility of nc-Si:H or microcrystalline silicon (μc-Si:H) TFTs is not always determined to have high values despite high conductivity of the channel layer. The TFT mobility under-estimation may be the case, which is a result of the drain/source (D/S) contact resistance coming from poor quality of doped layer. Several authors found that the crystallinity within the doped layer and the interface between the intrinsic and doped films can affect the TFT performance and should be taken into account [50, 51]. For example, K. Kandoussi *et al.* reported that the single run deposition of doped layer immediately after the intrinsic layer growth (only by opening the dopant gas without plasma stop) improves doped layer and interface, which in turn increases the TFT mobility by several orders [50]. C.-H. Lee *et al.* showed that the application of highly conductive n^+ μc-Si:H films in a-Si:H TFTs leads to higher ON current (by a factor ∼5) when compared to TFTs with n^+ a-Si:H ohmic contacts [51]. Therefore, the reduction of amorphous incubation layer, usually present in nc-Si:H films, and crystallinity improvement of n^+ nc-Si:H films are of high concern for their TFT applications.

Other concerns in low temperature depositions of nc-Si:H TFTs are the electrical properties of dielectric, and the dielectric/channel layer interface. The amorphous silicon nitride (a-SiN_x:H) film is the usual dielectric applied in TFTs because of its higher interface property [26]. However there are still issues on the PECVD grown a-SiN_x:H films. Even when

the leakage problems of a-SiN_x:H films are overcome, their compositional properties dramatically affect TFT performance [27,52]. It seems that there is an optimized N−H/Si−H IR peak area ratio in a-SiN_x:H films that results in the best TFT characteristics [26].

This chapter deals with the production and characterization of PECVD grown n^+ nc-Si:H and a-SiN_x:H films for nc-Si:H TFTs. Both films are applied to the TFT structures and their influences on the TFT performance are discussed.

5.2 Experimental details

Doped silicon thin films were deposited on glass microscope slides and crystalline silicon wafers (3500 Ωcm) by capacitively coupled PECVD reactor (Plasma Lab μP 80) at 13.56 MHz, supplying SiH_4, H_2 and PH_3 (1000 ppm in hydrogen) gases. Two sets of doped silicon thin films had only different R_H=H_2/SiH_4 flow ratios, while one set of the samples was deposited at the same conditions with the n^+ nc-Si:H film in TFT3. The rest of the doped layers were grown within three TFT structures and had deposition conditions provided in Table 4.1. They differed only in the applied RF power density (P_{RF}). All doped films were deposited at the pressure of 1 Torr, maintaining the substrate temperature at 473 K. The etching of doped nc-Si:H films was conducted via the reactive ion etching (RIE) in the etching system, described in Appendix C.2. The details of the etching process and utilized gases are given below in section 5.3.2. The p^+ nc-Si:H film was used only to compare its etching rate with that of the n^+ nc-Si:H film.

The lateral resistivity (ρ) of n^+ nc-Si:H films was measured by the Al planar electrodes grown on both n^+ nc-Si:H/glass and TFT structures. The hydrogen bonding configuration was determined through Si−H stretching mode using the microstructure factor (R), defined as [53]:

$$R = \frac{A_{2090}}{A_{2000} + A_{2090}} \tag{5.1}$$

where A_{2000} and A_{2090} are the deconvoluted integrated area of the infrared absorption for monohydride (Si−H) and dihydride (Si−H_2) silicon bonding, respectively. The bonded hydrogen (C_H) content was calculated from Si−H wagging mode around 635 cm^{-1} using the method described in section 6.2.

The dielectric films, a-SiN_x:H, were grown in the same PECVD system on Cr coated glass, quartz and silicon wafers using NH_3 and SiH_4 as source gases. The deposition conditions of all a-SiN_x:H films grown in this study are provided in Table 5.1. To get above stoichiometrical

Table 5.1: Deposition parameters of a-SiN_x:H thin films grown in this work.

Film#	Gases (sccm)					Chamber pressure (Torr)	RF Power density (mW/cm^2)	Substrate temperature (K)
	SiH_4	H_2	NH_3	NH_3/SiH_4	Total			
SiN1	3.9	0	31.5	~8	35.4	0.5	100	523
SiN2	5.9	0	75	~12	80.9	0.5	100	523
SiN3	3.9	0	75	~19	78.9	0.5	100	523
SiN4	3.9	0	110	~28	113.9	0.5	100	523
SiN5	5.9	0	75	~12	80.9	1	100	523
SiN6	3.9	0	110	~28	113.9	1	100	523
SiN7	3.9	200	75	~19	278.9	0.5	100	523
SiN8	3.9	200	45	~12	248.9	0.5	100	523
SiN9	3.9	200	45	~12	248.9	1	100	523
SiN10	3.9	200	45	~12	248.9	0.5	200	523

N/Si ratio within the films, the NH_3/SiH_4 gas flow ratio was varied as ~8, ~12, ~19, ~28. The a-SiN_x:H films with NH_3/SiH_4 gas flow ratio of ~19 and ~28 (SiN3 and SiN4) was applied to TFT1-TFT2 and TFT3 structures, respectively (see Table 4.1). The effects of H_2 inclusion to the source gases, the increase in the chamber pressure and P_{RF} on the dielectric properties of a-SiN_x:H film were also tested.

The vertical ρ and breakdown field of a-SiN_x:H films were measured from several Al dots (of ~1 mm in diameter) evaporated on a-SiN_x:H/Cr/glass structures and the average $I-V$ behavior for each sample was reported. The film deposition rate (DR) was determined from the profilometer measurements. Fourier transform infrared (FTIR) spectrometer (Nicolet 520) with 2 cm^{-1} resolution was used to determine bond concentrations and configurations of a-SiN_x:H films. The optical gap value (E_{04}, i.e. energy corresponding to absorption coefficient of 10^4 cm^{-1}) and refractive index (n) of a-SiN_x:H films were determined by the computer program OPTICHAR [70] from the UV−visible transmission spectra measured by Perkin Elmer Lambda 2S spectrometer in 200−1100 nm region.

5.3 Results and Discussions

5.3.1 Effect of H_2 Dilution on the Properties of Doped Layer

Two doped silicon thin films deposited at the same conditions, except R_H=H_2/SiH_4 flow ratio, show more than two order difference in the lateral resistivity. The one deposited at R_H=20 flow ratio has ρ of 900 Ωcm, usual for the doped amorphous films [30]. The other grown at

R_H=100 is highly conductive, 0.7 Ωcm, which is an indication of nanocrystalline nature of the film [51]. The FTIR spectra of these films (see Figure 5.1) differs in Si−H bending (around 635 cm^{-1}) and stretching (around 2000-2100 cm^{-1}) bonds. The rise in R for n^+ nc-Si:H film indicates higher porosity due to the crystallite formation [54]. Higher R value is generally well correlated with the film crystallinity and it was confirmed by the study of this thesis, provided in chapter 6, on the intrinsic nc-Si:H films. Lower Si−H bending bond concentration in the doped nc-Si:H, i.e. lower C_H, also supports the reduction of the amorphous tissue volume, since H atoms are located mostly at the grain boundaries in the form of $Si-H_2$ bonds. Low ρ value of n^+ nc-Si:H films can improve TFT properties since the doped layer in TFT reduces the contact resistance between D/S metal and channel semiconductor layer, and increases on-current [51]. As a result, more conductive n^+ nc-Si:H films were applied in TFT structures in this study. They were compared below for their ρ value dependence on the P_{RF} and film thickness.

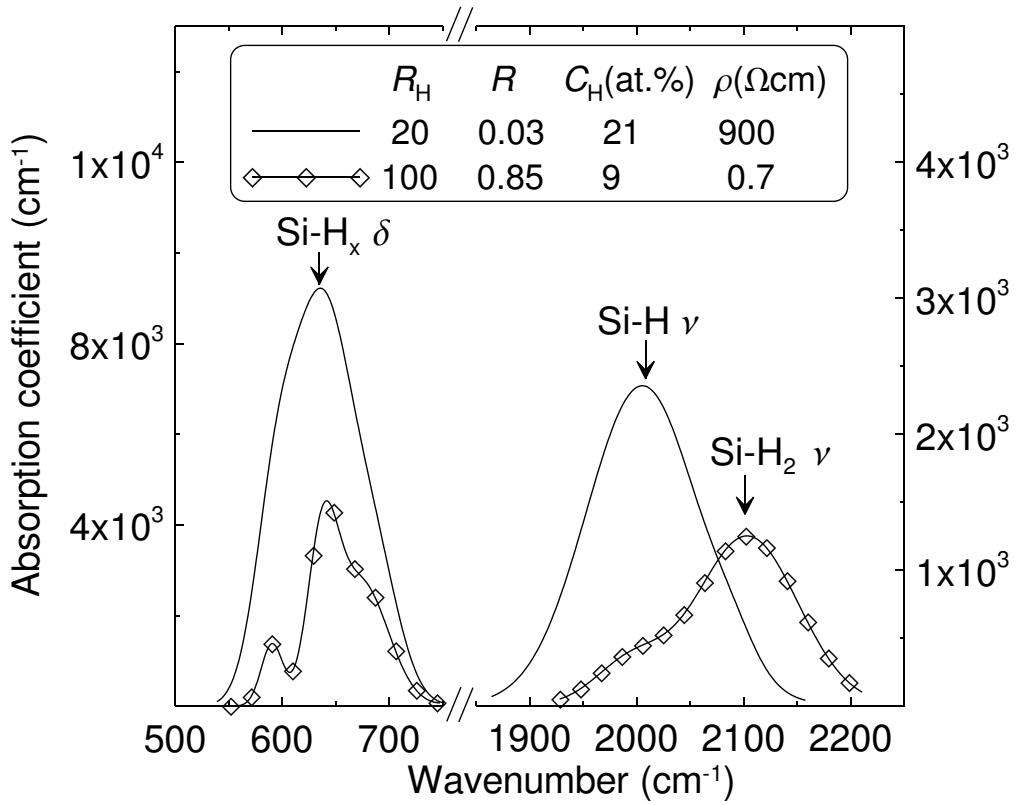


Figure 5.1: FTIR spectra of doped a-Si:H and nc-Si:H thin films deposited under the low (20) and high (100) R_H=H_2/SiH_4 flow ratios, respectively. Other deposition conditions are kept the same. R, C_H and ρ values are indicated in the inset.

5.3.2 Etching of Doped Layer

In this work, three etchant gases were employed for RIE of TFT doped layer: sulphur hexafluoride (SF_6), dichlorodifluoromethane or R-12 (CCl_2F_2), monochlorodifluoromethane or R-22 ($CHClF_2$). Use of R-12 and R-22 is not recommended due to their chlorine atoms, which cause depletion of ozone layer in atmosphere resulting in greenhouse effect. On the other hand, SF_6 does not contain chlorine, so it causes no ozone depletion and is used in recent years as an etchant gas. However, in the present study etching of doped nc-Si:H films could not be obtained by SF_6/O_2 gas mixture. Therefore, R-12 was used instead of SF_6 in both TFT fabrication and PECVD master unit cleaning. During the experimental work of this research, R-12 was run out due to the reactor cleaning, which was done before each thin film deposition process. Then, R-12 was replaced by R-22 gas. As a result, the etching rate of doped nc-Si:H films was determined for both R-12 and R-22 gases. For this, n^+ nc-Si:H/glass substrate sample was divided into a few small samples, one part of which was coated by PR. Each of these samples was etched in the etching unit for different time intervals at 0.1 Torr under P_{RF} of 450 mW/cm^2. After that PR was removed, and a step created between etched and non-etched film region was measured by mechanical stylus profilometer (AMBIOS XP-2), so that etched thickness for a given time interval was determined. The etching results of n^+ nc-Si:H films using R-12 and R-22 gases are provided in Figure 5.2-a and 5.2-b, respectively. The etching rate is found to be higher for R-12 gas, probably due to its higher content of chlorine atoms compared with R-22. It was found that the etch rate is highly dependent on the gas flow rate (Figure 5.2-a). With the decrease of flow rate (variable flow rate) the etching effect increased, therefore the pressure regulator was then mounted to the gas exit valve of the gas tube to provide constant flow rate into the etching unit. As it is seen in Figure 5.2-b, etch rate is almost the same for p-type and n-type nc-Si:H films. Besides, higher P_{RF} of 675 mW/cm^2 resulted in higher etching rate. However it was not used due to the possible increase in damage of the TFT channel layer lying below the doped layer and the decrease in the controllability of the etching time.

5.3.3 Thickness and RF power dependence of n^+ nc-Si:H film

Using the above described etching results for R-22 gas (see section 5.3.2), the resistivity as a function of the film thickness was found by etching highly conductive n^+ nc-Si:H/glass structure at hand (Figure 5.3). Data for the films grown at the edge of the PECVD electrode is

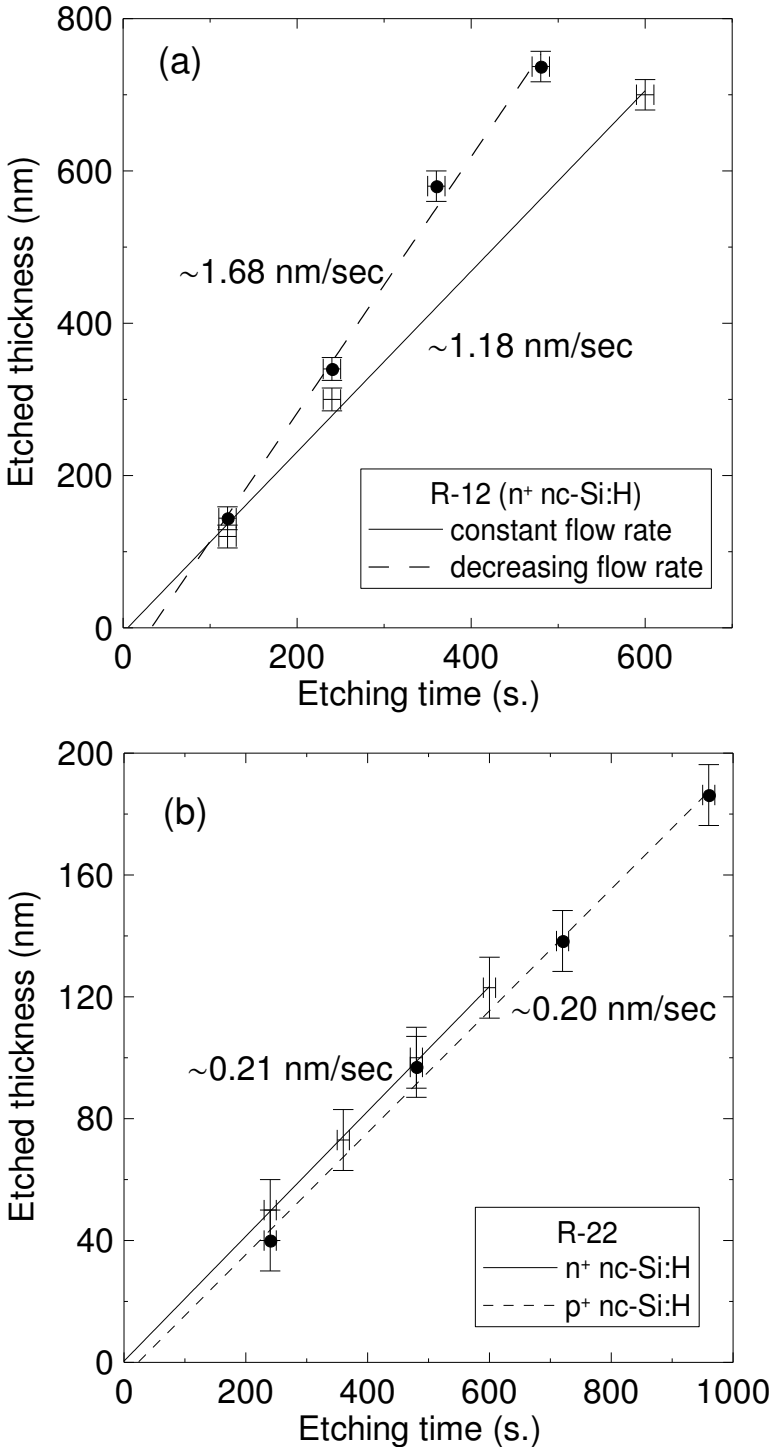


Figure 5.2: Etched thickness of n^+ nc-Si:H film as a function of etching duration time using (a) R-12 and (b) R-22 etchant gases. The determined etching rate is indicated for both cases. Note that: (a) decreasing flow rate enhances the etching rate, (b) etching rate of p^+ nc-Si:H film is similar to that of n^+ nc-Si:H.

almost similar to that for the films at the center. The film thickness dependence of resistivity was found earlier for intrinsic nc-Si:H [23] and n^+ μc-Si:H films [51]. However, the ρ values of n^+ nc-Si:H layer in the present study are highly scattered showing more than 7 orders of magnitude difference within 50 nm thickness. It can be concluded from Figure 5.3 that the ρ values below a critical film thickness (45 nm) are close to the intrinsic nc-Si:H ones, while one can expect them to be below 1000 Ωcm as in the case of doped a-Si:H. This may happen due to the highly defective amorphous incubation layer, where no doping effect is

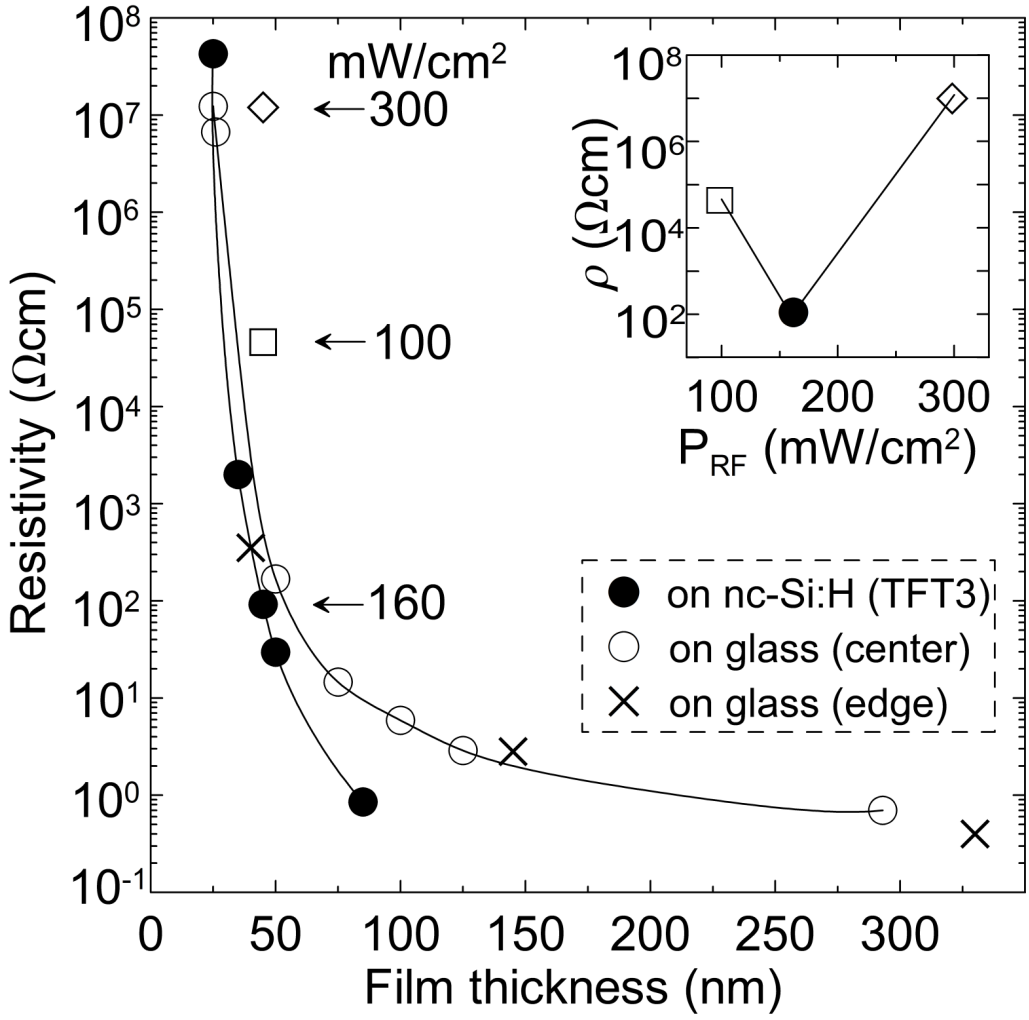


Figure 5.3: Lateral resistivities as a function of the film thickness of n^+ nc-Si:H films deposited at the center of the PECVD electrode at 160 mW/cm^2 on the glass substrate and on nc-Si:H layer in TFT3. The inset shows the RF power density dependence of the resistivity of 45 nm n^+ nc-Si:H films deposited in TFT structures. Here all the films were grown at the center of PECVD electrode, and data for films at the edge of the electrode is provided only for n^+ nc-Si:H/glass structure.

achieved [30]; and/or it can be the consequence of nc-Si:H anisotropy: the lateral current transport is impeded by the columnar structure of the incubation layer [42]. Deposited under the similar conditions to n^+ nc-Si:H/glass structure, n^+ nc-Si:H layer in the TFT3 structure was also gradually etched to retrieve its thickness dependence of resistivity (see Figure 5.3). The film in TFT3 has lower ρ when compared to that of the film on the glass. Consequently, the incubation layer of n^+ nc-Si:H film seems to be thinner when deposited above nc-Si:H layer, i.e. in TFT3 structure. It is expected from the previous studies on various buffer layers [44, 55], where the nc-Si:H films acted as a best seed layer for rapid crystallite nucleation of the nc-Si:H films grown above it and is usually applied to the TFT structures [56]. In our case intrinsic nc-Si:H film seems to promote the higher crystallization at the initial stage of the n^+ nc-Si:H layer, which in turn decreases its resistivity. Figure 5.3 also contains the resistivity data of 45 nm n^+ nc-Si:H films deposited at different P_{RF}, found directly from $I-V$ measurements on TFT1 and TFT2 structures before back-channel etching process. The similar dependence on RF power was reported by C.-H. Lee *et al.* for n^+ μc-Si:H films [51]. The hydrogen decomposition enhances with P_{RF} increasing from 100 to 160 mW/cm^2 and results in more crystalline films, which improves doping and decreases ρ. But with further increase in P_{RF} ion bombardment damages the film surface during the growth process, which leads to high film resistivity. Therefore, the deposition of n^+ nc-Si:H films in TFTs should be performed at the optimum P_{RF} around 160 mW/cm^2.

5.3.4 Effect of deposition conditions on the electrical properties a-SiN$_x$:H films

Figure 5.4 demonstrates the vertical $I-V$ measurements of the a-SiN$_x$:H thin films deposited at the center of the PECVD electrode. To compare all $I-V$ curves the current density (J) vs. electric field (E) were reported using Al dot area and the film thickness. The film resistivity and breakdown field are strongly dependent on the deposition parameters. As discussed above in section 3.2, the high power density, very high gas flow ratio and high pressure values are believed to induce desirable aminosilane radicals instead of disilane. But the results of Figure 5.4 show that such deposition conditions do not always result in the enhanced insulator properties and should be reconsidered carefully. As expected, vertical ρ and breakdown field increases with increasing NH_3/SiH_4 gas flow ratio (see Table 5.1 and Figure 5.4 for SiN1-SiN4). Comparing SiN2 and SiN4 with SiN5 and SiN6, respectively, one can deduce that higher deposition pressure for ~12 and ~28 gas flow ratios deteriorates the insulating property of the dielectric. However it was anticipated that the twice higher pressure would increase the

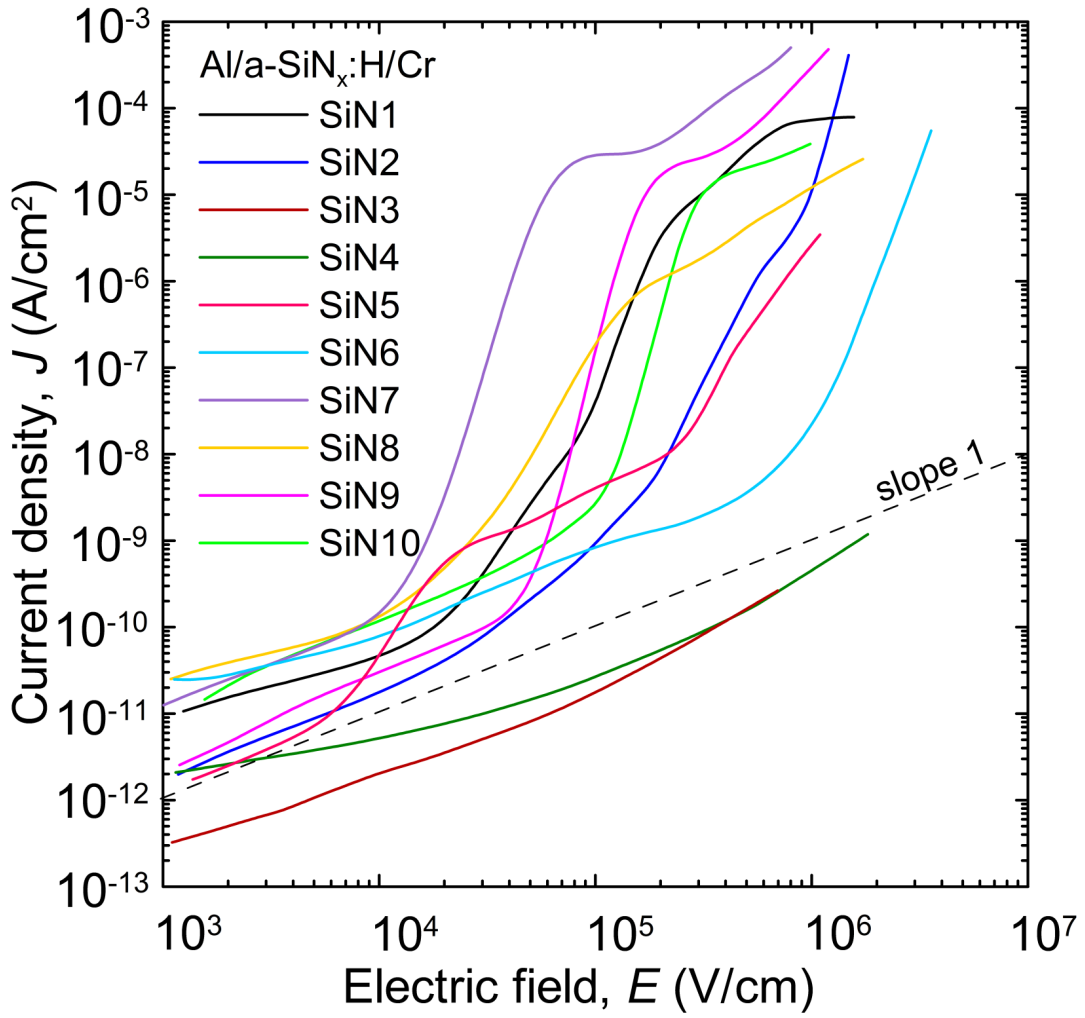


Figure 5.4: The current density vs. electric field of a-SiN_x:H thin films deposited at the center of the PECVD electrode. Refer to Table 5.1 for the deposition parameters of the corresponding films.

residence time of radicals in the plasma, which enhances the amination reaction (see section 3.2) and so improves the film quality. This deterioration may happened due to the high flow rate of SiH_4, since above some critical flow rate there was not enough ammonia to consume all silane and amino-saturated conditions could not be achieved even for 3.9 sccm of SiH_4 [33]. Besides, the addition of H_2 gas during the film growth also increased the current density (compare SiN3 with SiN7 and SiN2 with SiN8). Therefore, in the frame of this work the very high H_2 dilution could not play the constructive role to deposit more compact film [30, 32], instead H_2 decreased the deposition rate and N content within the film. In the case of SiN8 film, increasing its deposition pressure (SiN9) and P_{RF} (SiN10) very slightly improves the

insulator properties, but still both of these films are far away from the TFT requirements for the insulator layer. The lowest J and highest ρ (around 2-3×10^{15} Ωcm) values are found for SiN3 and SiN4 samples, so that their application to TFT structures seems to be plausible. Their expected gate leakage currents, estimated for the S area of the TFT structure given in Figure 4.5-a with W/L=13, are provided in Figure 5.5. The estimated gate leakage current at maximum (in this study) applied V_{GS} of 60 V is $\leq 10^{-13}$ A, which is acceptable for TFT application. To conclude on the effect of the deposition conditions of a-SiN_x:H utilized in this study, only the addition of extra NH_3 gas to the lowest (for the present deposition system) SiH_4 flow rate led to the improvement in the insulator properties. The following section concerns with the possible explanations for this improvement with increasing NH_3/SiH_4 gas flow ratio and the application of SiN3 and SiN4 in TFTs.

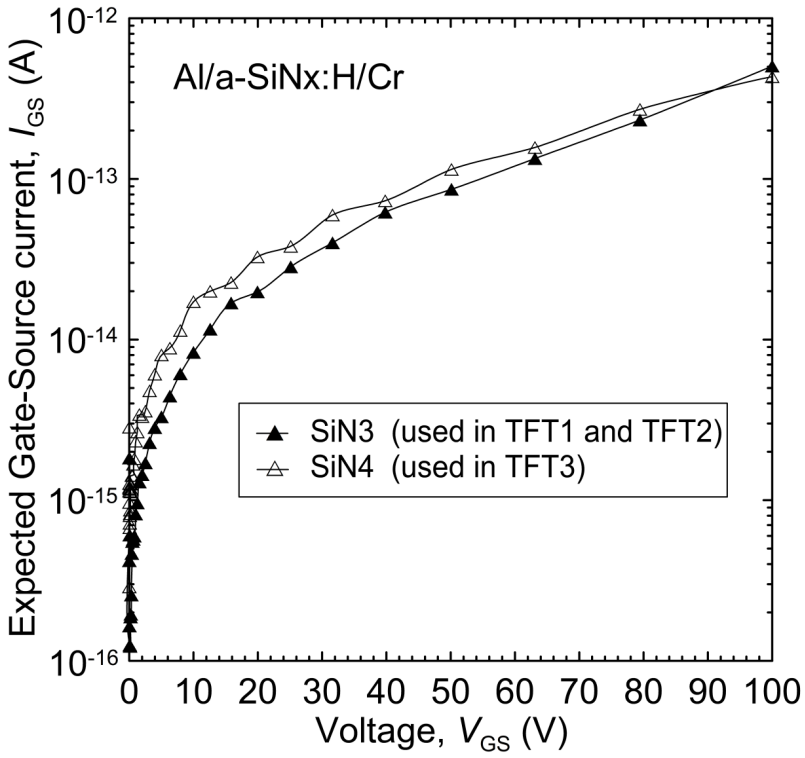


Figure 5.5: Expected gate-source current vs. voltage of SiN3 and SiN4 estimated for the source area of TFTs.

5.3.5 Effect of NH_3 gas flow rate on the properties of a-SiN_x:H films and their application in nc-Si:H TFTs

In SiN1, SiN3 and SiN4 set of a-SiN_x:H films grown in this study the flow rate of SiH_4 was held constant, while NH_3 flow rate was increased from 31.5 to 110 sccm. So, it is quite different from some previous studies, where NH_3/SiH_4 ratio was varied by changing SiH_4 flow rate [27,57], and similar to the reports by M.R. Esmaeili-Rad *et al.* [52] and Y-B. Park *et al.* [37]. The silane flow rate is important for the formation of the amination reaction: above its critical value the ammonia amount is deficient to consume all of the silane, consequently undesirable disilane amount in plasma rises and desirable aminosilanes fall [33]. For example, in this study it was found that the use of SiH_4 flow rate of 5.9 sccm in SiN2 results in higher Si−H (by factor of ∼2), lower N−H bond concentrations and much higher deposition rate (*DR*) of 29.3 nm/min compared with those of SiN1, SiN3 and SiN4 films grown under 3.9 sccm of SiH_4 (see Table 5.1). These results may suggest increased disilane amount during SiN2 film deposition. Si−H bonds are weaker than N−H bonds, so they are more intend to form dangling bonds (DB) [37] leading to charge trapping and electrical instability. As a result, Si−H bond amount should be minimized to obtain high quality insulator [30]. Therefore, the lowest applicable SiH_4 flow rate of 3.9 sccm was preferred in this study. From this point of view, the above film set (SiN1, SiN3 and SiN4) eliminates any discrepancies that may come from the silane flow rate and can be analyzed only by the effect of NH_3 flow rate on the film growth.

As mentioned before, SiN1 with low NH_3/SiH_4 flow ratio of ∼8 has higher *J* than SiN3 and SiN4 with ∼19 and ∼28 flow ratios. To get insight into these three a-SiN_x:H films, the FTIR spectra were measured and normalized to the film thicknesses, as shown in Figure 5.6. All the films contain a small concentration of Si−H bonds when compared to N−H ones, so they are N-rich and can be considered to be over-stoichiometric [27]. The Si−H and SiN−H_2 bond concentration decreases, while N−H one remains the same with increasing NH_3 flow. Hence disilane amount within the plasma is reduced and NH_2 groups react with each other to evolve NH_3. These can imply the enhanced formation of amination reaction during the deposition process and more N-rich films with increasing NH_3. However, Si−N bond concentration is higher for ∼19 flow ratio and lower for ∼28 when compared to that of ∼8 one. This may stem from the lowered residence time for the highest NH_3 flow rate, deduced from *DR* of SiN1, SiN3 and SiN4, which are 18.4 nm/min, 20 nm/min and 18.2

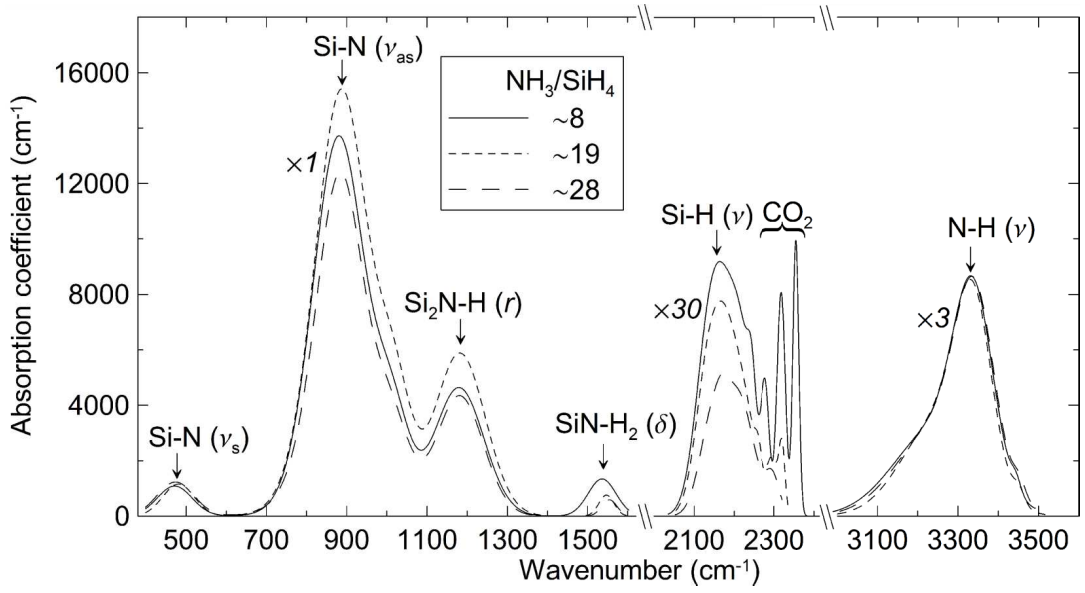


Figure 5.6: FTIR spectra of SiN1, SiN3 and SiN4 films grown with NH_3/SiH_4 gas flow ratio of ~8, ~19, ~28, respectively. CO_2 peaks are the measurement artifacts that come from the changes of the environment surrounding the instrument.

nm/min, respectively. The highest NH_3 flow may deteriorate the films by producing lower Si−N bond amount and so lower N content than in SiN3. It is clearly seen in Figure 5.7 that the E_{04} values roughly follow the Si−N bond concentration and n has a trend just opposite to that of the optical gap. It is known that E_{04} increases when Si−Si bonds decrease and are replaced by Si−N ones [32]. So, in this work the highest reduction of Si−Si bonds seems to be attained at ~19 flow ratio (see Figure 5.7). Similarly, n decreases with increasing Si−N bond concentration. Therefore, in SiN4 the Si−Si bond formation seems to be enhanced than in SiN3. However, the differences in the optical and structural properties of SiN3 and SiN4 are not reflected in their $J - E$ characteristics. SiN3 and SiN4 films can be distinguished by their applications in TFT2 and TFT3, respectively, where the channel layer (nc-Si:H) is grown under the same conditions, while the doped layer has different P_{RF} (see Table 4.1). It is known that the doped layer does not affect the a-SiN$_x$:H/nc-Si:H interface and can only increase the I_{ON} [51]. Consequently, other parameters of these TFTs are determined by their insulator properties. The TFTs show quite different transfer characteristics in Figure 5.8. Note here that the gate leakage current is found around 10^{-14} A and is even less than the estimated ones for SiN3 and SiN4 films shown in Figure 5.5. The TFT3 has much higher threshold voltage (V_T), lower mobility (μ_{FE}, despite its highest conductive doped layer) and larger subthreshold

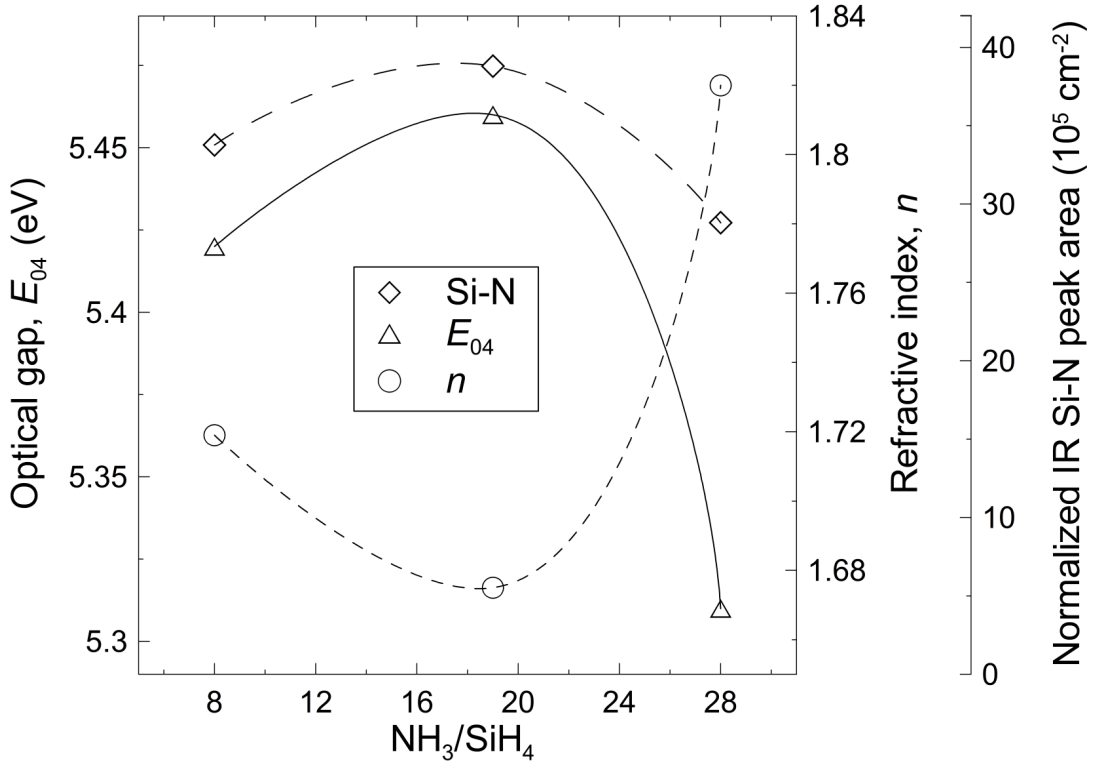


Figure 5.7: Optical gap, refractive index and normalized IR Si−N peak area of SiN1, SiN3 and SiN4 films as function of NH_3/SiH_4 gas flow ratio.

slope (SS) than TFT2. These findings can be interpreted through the charge distribution inside the insulators using the above results for SiN3 and SiN4. As it was reported earlier, N−H and Si−H centers are considered as the negative and positive charge-trapping centers, respectively [26, 57]. Therefore, insulating property (J) is expected to be related with charge screening effects due to negative centers (almost same amount for SiN1, SiN3 and SiN4) and with the reduction of the leakage current through the film bulk (decreasing Si−H bond amount with increasing NH_3/SiH_4 gas flow ratio) [57]. In SiN4 there are less positive centers, i.e. Si−H bonds, than in SiN3, but this increases the insulating property not too much as in the SiN1-SiN3 case. Instead, the positive centers affect the V_T in TFT structures: they may act as the built-in gate voltage in SiN3 and reduce V_T, whereas their deficiency may decrease the field lines across the SiN4 film bulk and raise V_T. On the other hand, since SS value is higher in TFT3, the SiN4/nc-Si:H interface is also deteriorated compared with the SiN3/nc-Si:H one. This might be associated with the possibly increased positive centers at the SiN4/nc-Si:H interface due to its higher N−H/Si−H ratio [57], which act as the electron trapping centers and reduce TFT mobility. So, in addition to the insulating property of a-SiN_x:H films the

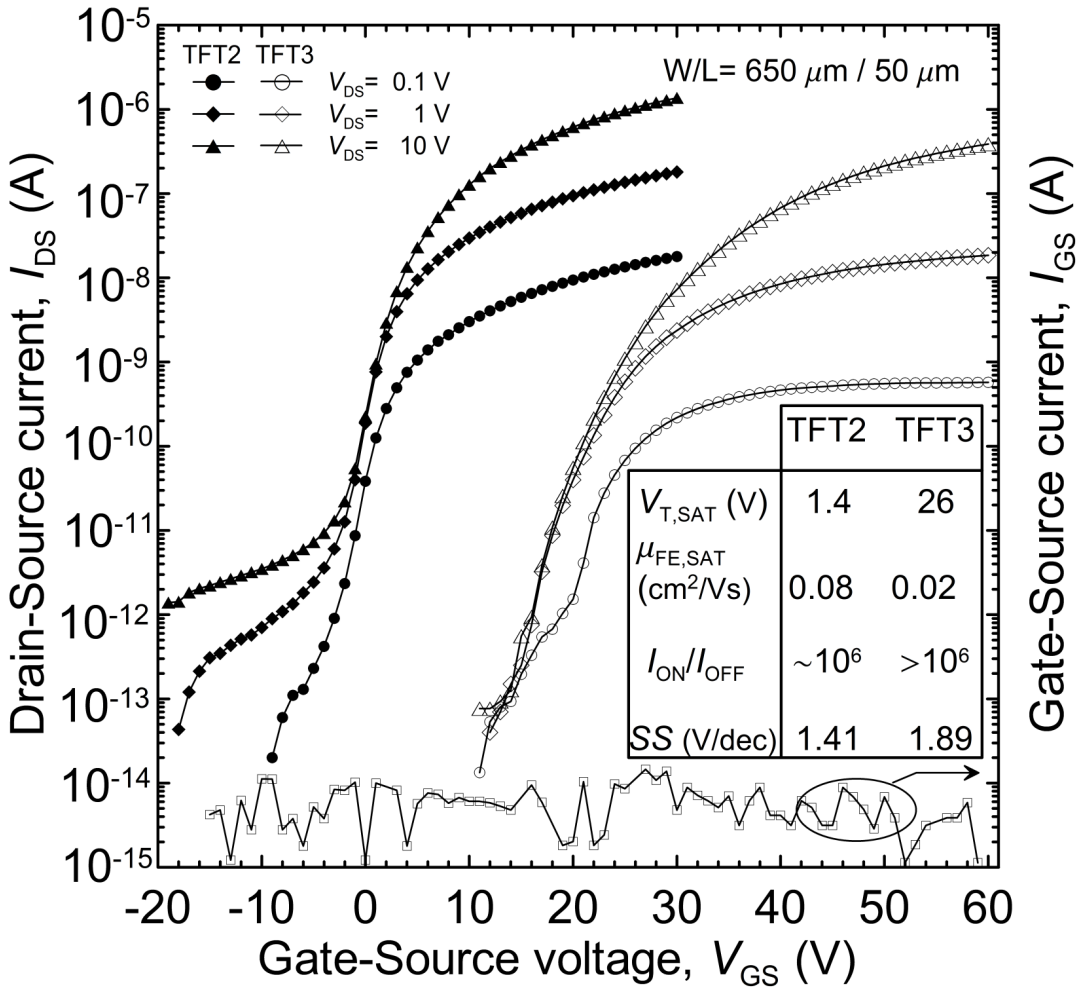


Figure 5.8: TFT transfer characteristics of TFT2 and TFT3 deposited using SiN3 and SiN4 films as a gate dielectric, respectively.

optimum charge distribution inside the film bulk can affect the TFT characteristics.

5.4 Conclusion

The doping of the hydrogenated silicon thin films grown by PECVD technique at 473 K under high H_2 dilution, i.e. nc-Si:H, resulted in more conductive films than under low H_2 dilution, i.e. a-Si:H. However the lateral ρ of n^+ nc-Si:H films was found to be highly dependent on the film thickness due to the disordered incubation layer. This layer was decreased when deposited above nc-Si:H film in BG TFT. The P_{RF}, used in n^+ nc-Si:H deposition, was optimized for the minimum thickness of the incubation layer and was determined to be ~160 mW/cm^2. The etching of n^+ nc-Si:H films, applied during the back-channel etch to form TFT,

was found to have lower etching rate for R-22 gas than for R-12 one.

Several deposition conditions of a-SiN_x:H films were used to examine their effects on the $J - E$ characteristics. The increase in the PECVD chamber pressure from 0.5 Torr to 1 Torr or the dilution of source gases by H_2 deteriorated the insulating properties of a-SiN_x:H. On the other hand, the increase in NH_3 flow decreased Si−H bonds and therefore leakage current through a-SiN_x:H bulk. However, the film grown with the highest NH_3/SiH_4 flow ratio (∼28) probably contained more Si−Si bonds (due to its lower E_{04} and higher n) than the film grown with ∼19 ratio. When applied to TFT, the former film decreased the device performance compared to the latter film. This was associated with the optimum N−H/Si−H bond concentration ratio attained for the a-SiN_x:H film grown with NH_3/SiH_4∼19.

CHAPTER 6

LARGE AREA UNIFORMITY OF PLASMA GROWN HYDROGENATED NANOCRYSTALLINE SILICON AND ITS APPLICATION IN TFT

6.1 Introduction

As mentioned above in section 3.3, nc-Si:H can be easily grown by the standard industrial technique, i.e. plasma enhanced chemical vapor deposition (PECVD) at RF frequency (13.56 MHz), using high dilution of silane (SiH_4) by H_2 and/or inert gases as He, Ar, etc. [58–60]. However, lowering relative silane flow rate decreases the growth rate leading to high-cost devices [61]. As a solution, high RF power density (P_{RF}) together with high pressure (to decrease ion bombardment) was found to increase the deposition rate of nc-Si:H [61, 62]. Therefore, influences of high P_{RF} on the nc-Si:H film quality are one of the critical issues. The effect of P_{RF} on the growth of nc-Si:H films was studied by several authors [58, 61–64]. They usually report that the crystallinity and optical gap of the films are maximized at an optimum P_{RF} value. However, P_{RF} dependence is strongly affected by other deposition conditions such as pressure and use of inert gases. The study of this chapter extends the effect of P_{RF} on the large area uniformity of the structural, optical and electrical properties of nc-Si:H films. Moreover, the nc-Si:H films have been used as a channel material in bottom-gate (BG) TFTs to reveal the influences of P_{RF} on TFT performance. The results are also presented in [65].

6.2 Experimental details

Intrinsic nc-Si:H thin films were deposited on glass microscope slides and crystalline silicon wafers (3500 Ωcm) by capacitively coupled PECVD reactor (Plasma Lab μP 80) at

13.56 MHz, supplying SiH_4 and H_2 gases through the showerhead located at the center of the top electrode (see inset of Figure 6.1-b). Cleaned by the standard procedure, substrates were placed on the grounded bottom electrode of area ~450 cm^2. Hydrogen dilution ratio (H_2/(H_2+SiH_4)) was settled to 99%, deposition pressure to 1 Torr, substrate temperature to 473 K, while RF power densities were varied as 100, 162, 300, 444 mW/cm^2.

After each deposition cycle, the film characterization was performed for two differently positioned film sets: at the center and near the edge of the electrode. The deposition rate (*DR*) of the films was found from the total deposition time and the film thickness (*d*), measured by the mechanical stylus profilometer (AMBIOS XP-2) with error ≤10%. The film thicknesses used in this study are in the range of 230−470 nm. The phase (amorphous or nanocrystalline) of the films and orientations of crystallites were determined by Rigaku Miniflex X-ray diffractometer (XRD) with Cu Kα X-ray radiation source (λ = 1.54 Å) from the films deposited on the glass substrates. The grain size (*L*) of the crystallites was calculated using the Scherrer's formula $L = 0.89\lambda/(\beta\cos\theta)$, where θ is the Bragg angle and β is the full width at half maximum (FWHM) of the XRD peak, fitted with the Gaussian curve. To compare crystalline volume fractions in different films, the intensity of the largest XRD peak (111) was normalized (I_{norm}) by the thickness of the film using the simplified formula [66] due to the low X-ray linear absorption coefficient α=152.19 cm^{-1} of Cu Kα radiation [67] in silicon (i.e. $\alpha d \ll 1$):

$$I = \int_0^d \frac{I_0 abS}{sin\theta} e^{-2\alpha x/sin\theta} dx \approx I_0 abS\, d \tag{6.1}$$

where I_0 is the incident X-ray intensity with cross-section area *S*, *I* is the diffracted intensity, *a* and *b* are the volume fractions of crystals and reflected incident energy, respectively. The hydrogen bonding configuration, bonded hydrogen (C_H) and oxygen (C_O) contents were followed by Fourier transform infrared (FTIR) spectrometer (Nicolet 520) using 2 cm^{-1} resolution. The hydrogen bonding configuration was easily followed by Si−H stretching mode using the microstructure factor (*R*), defined previously in section 5.2. The densities of hydrogen and oxygen (N_H and N_O) were calculated from Si−H wagging and Si−O stretching modes around 635 cm^{-1} and 1030 cm^{-1}, using the proportionality constants 1.6×10^{19} cm^{-2} and 7.8×10^{18} cm^{-2}, respectively [68]. C_O was calculated from $C_O = N_O/(N_O+N_{Si})$ and C_H from the corrected formula (due to the small film thickness) $C_H = (N_H/(N_H+N_{Si}))/(1.72-0.7\times d)$ [69], where the Si atom density (N_{Si}) was taken as 5×10^{22} cm^{-3} and *d* is the film thickness in μm [68]. Refractive index (*n*) and absorption coefficient (α) were determined by the computer program OPTICHAR [70] from the UV−visible transmission spectra, which

were measured between 200 and 1100 nm by Perkin Elmer Lambda 2S spectrometer. The Tauc and cubic gaps were estimated through the extrapolation of the linear fits in the strong absorption region. The refractive indices have been reported at infinite wavelength. Aluminum planar electrodes of 2.5 mm width and five different interelectrode distances from 1 to 5 mm with 1 mm increment were evaporated on the films grown on the glass substrates under a high vacuum of 10^{-6} Torr. The dark resistivity (ρ), obtained from the ohmic region of the current-voltage ($I-V$) dependence, was measured by Keithley 6517 electrometer for the five different distances between the lateral contacts and their average value has been reported for each sample.

Two sets of BG TFTs (TFT1 and TFT2) were fabricated at the center of the reactor electrode on the chrome coated glass substrates by trilayer deposition using a-SiN_x:H as the gate insulator and nc-Si:H films of the present study as the channel material and n^+ layer as the ohmic contact. In TFT1 and TFT2 the channel is 140 nm nc-Si:H film deposited at 100 mW/cm^2 and 300 mW/cm^2, respectively. Aluminum was evaporated above the n^+ nc-Si:H layer and then patterned to obtain the drain (D) and source (S) contacts. After performing post-deposition annealing at 423 K for 0.5 h to improve the performance of the device [49], the TFTs were characterized at room temperature by Keithley 230 voltage source and Keithley 617 electrometer. Since the thicknesses of the nc-Si:H films used in the TFTs are lower than that of the test films for optical-electrical investigation, the $I-V$ measurements were also performed from $D-S$ contacts to find the channel layer resistivities. The bias stress measurements were done under the gate voltages (V_{GS}) with the same voltage drop above the threshold voltage (V_T) for each TFT and without $D-S$ bias (V_{DS}). The TFT transfer characteristics were retrieved at V_{DS} = 5 V at certain time intervals.

6.3 Results

The *DR* dependence on the RF power density is depicted in Figure 6.1-a. The *DR* of the films deposited at the center of the electrode rises from 2.3 to 4.8 nm/min when P_{RF} is increased from 100 to 444 mW/cm^2, while near the edge it remains almost constant around 3.8 nm/min. The highest *DR* uniformity is expected to be around 200 mW/cm^2, whereas at 100 mW/cm^2 and 444 mW/cm^2 the non-uniformity in *DR* is worthy of attention (see Figure 6.1-b).

Other film properties and their non-uniformity are also affected by P_{RF}. Among the interesting findings is that at P_{RF} of 100−162 mW/cm^2 the films at the center of the electrode

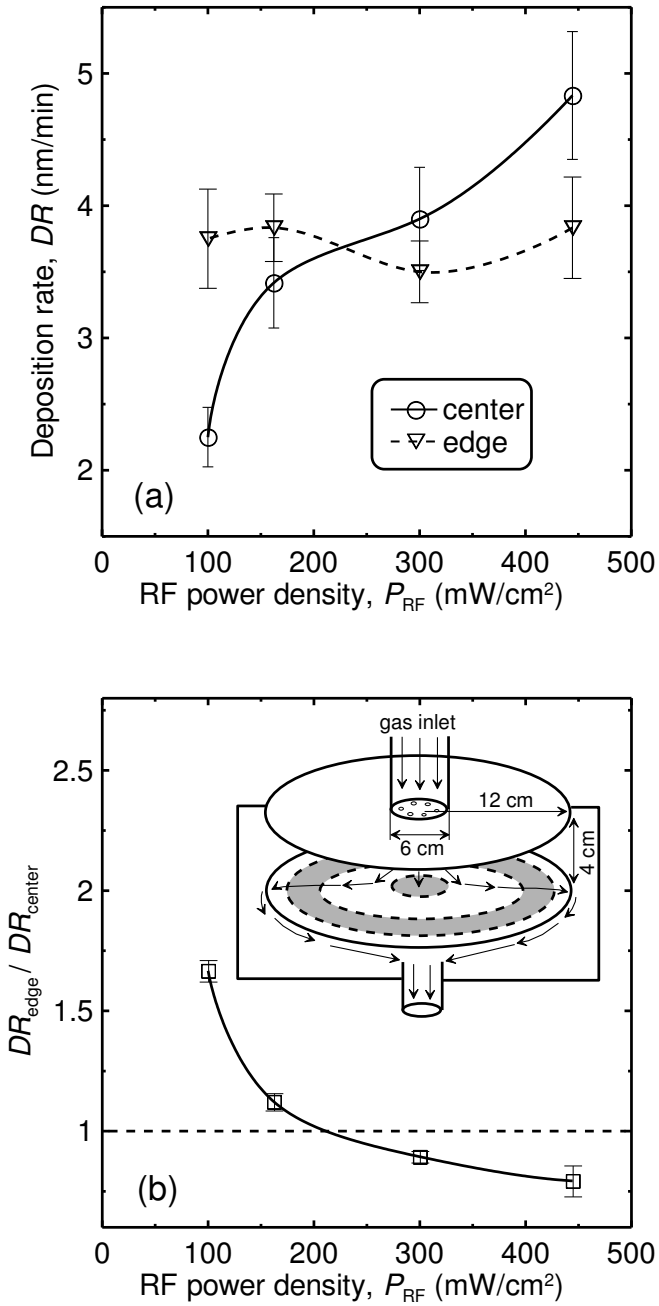


Figure 6.1: (a) Variation of the *DR* of nc-Si:H films at the center and near the edge of the PECVD electrode with P_{RF}. (b) The ratio of the *DR* near the edge of the electrode to the *DR* at the center as a function of P_{RF}. The uniform deposition is indicated by the dashed line at DR_{edge}/DR_{center}=1. The inset shows schematically the gas flow through the center of the top electrode towards the edge of the bottom electrode, from where the gas is pumped down. The painted regions correspond to the center and region near the edge of the bottom electrode, where the samples of this work were placed.

reveal no X-ray diffraction peaks, whereas those near the edge exhibit the presence of the crystallinity, as it is displayed in Figure 6.2. The grain size deduced from (111) XRD peak is about 4−5 nm for all nc-Si:H films. Besides, XRD measurements are used to follow the relative behavior of intensity of (111) peak normalized by the film thickness, which is taken as a measure of the crystalline volume fraction (F_C) variation. As shown in Figure 6.3-a, F_C of the films deposited near the edge of the electrode does not change remarkably with P_{RF} and is always higher than that of the films at the center. This result is similar to the P_{RF} dependence of the microstructure factor (R). Figure 6.3-b shows a rise in R with increasing P_{RF} for the films grown at the center of the electrode, whereas R values at all P_{RF} for the films near the edge are greater and above 0.8 with the maximum of 0.91 at 300 mW/cm^2. On the

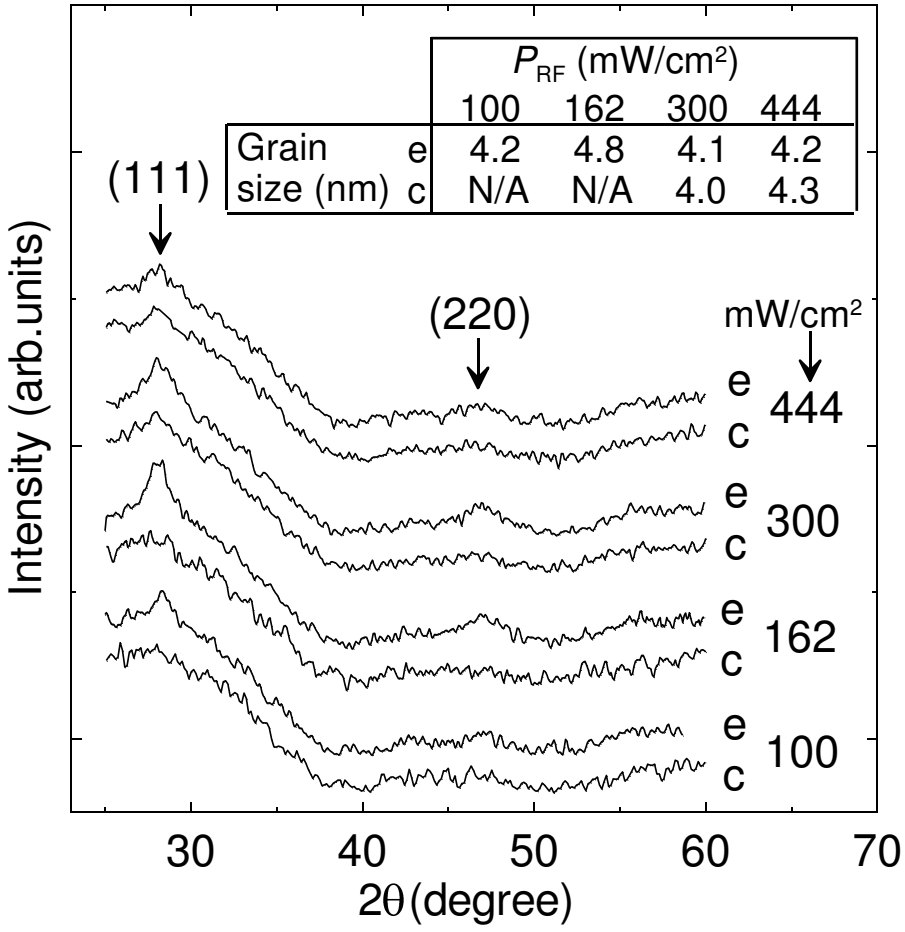


Figure 6.2: X-ray diffraction spectra of nc-Si:H films at the center (c) and near the edge (e) of the PECVD electrode deposited under different P_{RF}. The inset provides the crystallite grain size, which is not available (N/A) for the films of amorphous structure or with the crystallinity below the detection limit.

same graph, the normalized area of 2000 cm^{-1} FTIR peak exhibit the variation with P_{RF} just opposite to that of R.

As it is seen in Figure 6.3-a, the behavior of dark resistivity roughly follows the trends of F_C, R and normalized IR deconvoluted area A_{2000} with increasing P_{RF}. The resistivity of the films grown at the center of the electrode is around (6−9)×10^7 Ωcm at P_{RF} of 100−162 mW/cm^2, then sharply decreases to its minimum value of 2×10^5 Ωcm at 300 mW/cm^2 and

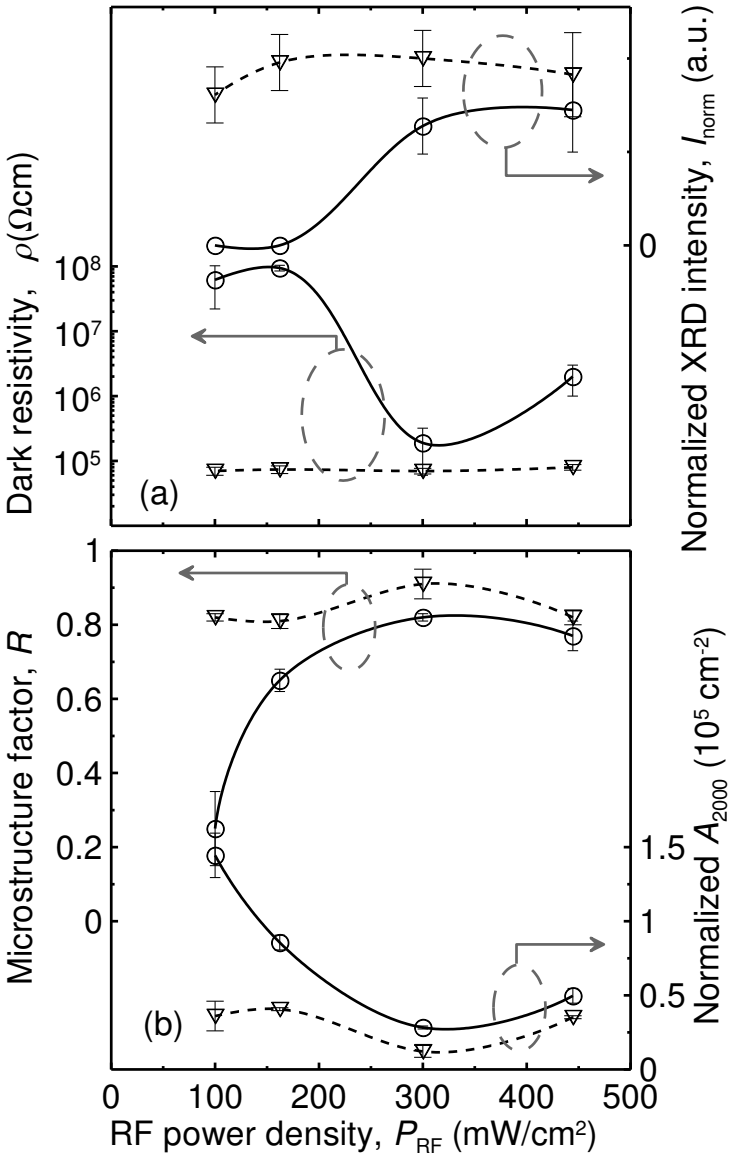


Figure 6.3: (a) Variation of the dark resistivity and the normalized XRD intensity of (111) peak of nc-Si:H films, grown at the center (◯) and near the edge (▽) of the PECVD electrode, with applied P_{RF}. (b) P_{RF} dependence of the microstructure factor and the normalized FTIR area of 2000 cm^{-1} peak.

slightly increases about an order of magnitude at 444 mW/cm^2. The films near the edge of the electrode have ρ around 7×10^4 Ωcm and show almost no change with P_{RF}.

The hydrogen content (Figure 6.4-a) is also lower for the films near the edge than for those grown at the center of the electrode. For both films at the center and near the edge of the electrode, the minimum C_H is attained at 300 mW/cm^2, while the maximum C_H, above 15%, is found in the films grown at the center at 100−162 mW/cm^2. The subgap absorption tail (Urbach tail, E_0) for the films grown at the center at 100−162 mW/cm^2 is 43−65 meV, whereas it increases up to 200 meV for the rest of the films, as shown in Figure 6.4-b. This

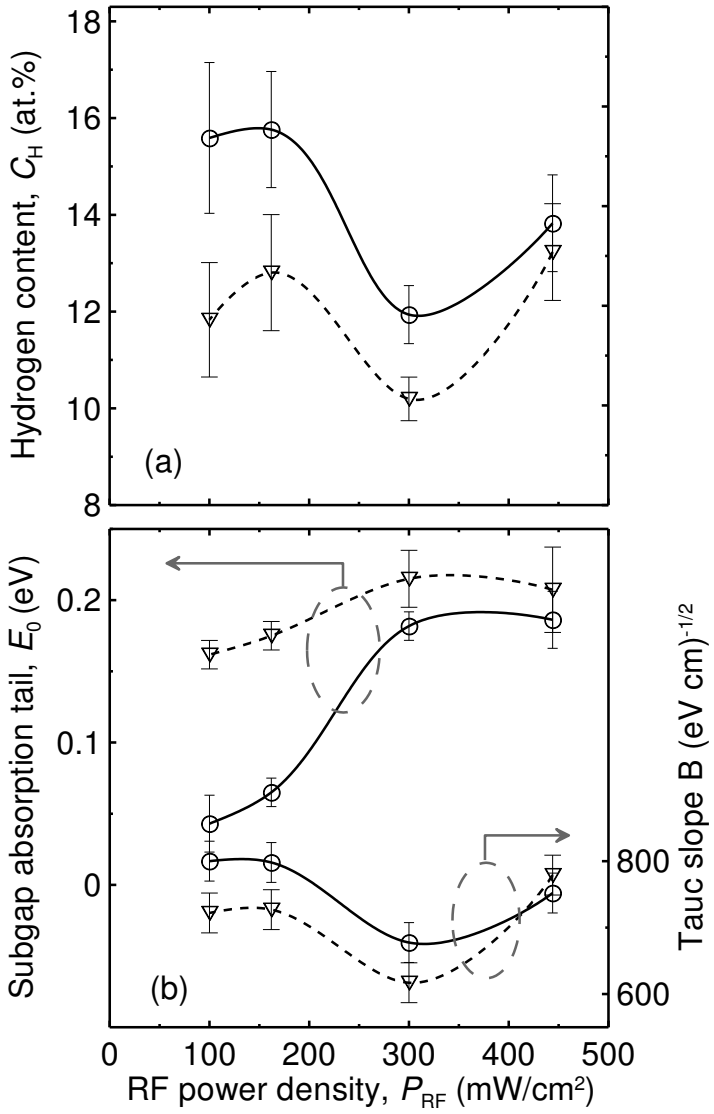


Figure 6.4: (a) The bonded hydrogen content of nc-Si:H films, grown at the center (◯) and near the edge (▽) of the PECVD electrode, as a function of P_{RF}. (b) Variation of the subgap absorption tail and the Tauc slope with P_{RF}.

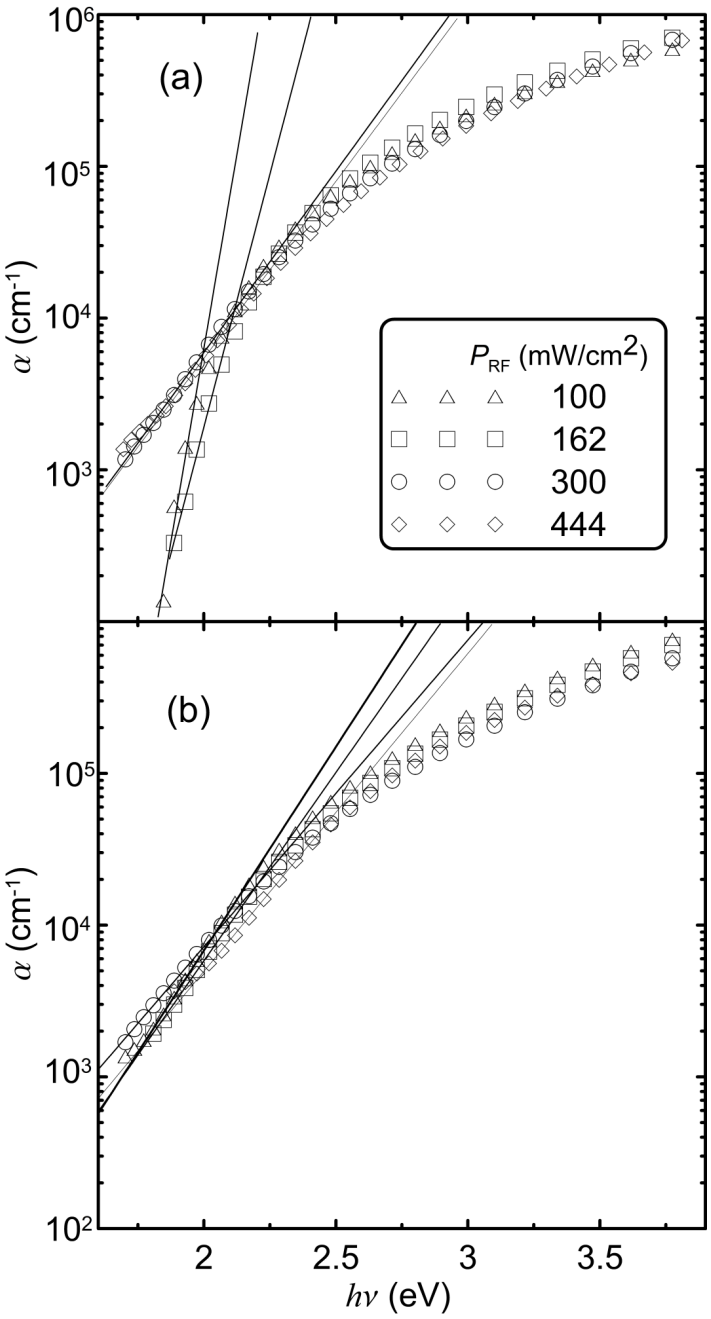


Figure 6.5: Absorption coefficient of nc-Si:H films deposited (a) at the center and (b) at the edge of the PECVD electrode for various P_{RF}.

is the result of the high difference in the slopes of the absorption coefficient (see Figure 6.5). The tendency of E_0 with P_{RF} is similar to that of R and F_C, while Tauc slope (B) has an opposite behavior. The optical gap values obtained from Tauc and cubic plots together with E_{04} (energy corresponding to α=10^4 cm^{-1}) exhibit nearly no variation with P_{RF} (see Figure

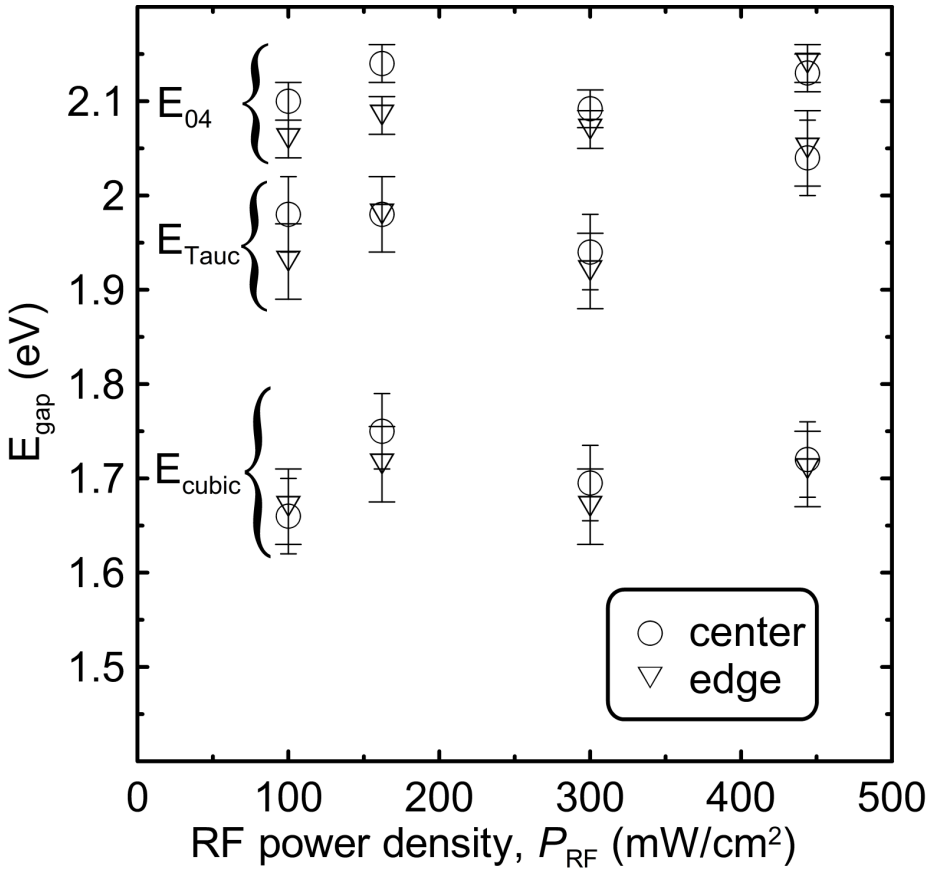


Figure 6.6: Fluctuation of the optical energy gaps of nc-Si:H films, grown at the center and near the edge of the PECVD electrode, with applied P_{RF}.

6.6).

From Figure 6.7 it is seen that the change of the refractive index with P_{RF} is opposite to that of the oxygen content, and it is not correlated with R or F_C unlike some reports [71, 72]. The maximum n value is around 3.1 and is lower than the refractive index of a-Si:H films and c-Si (≥3.5). C_O is relatively low for all films (with the minimum value below 0.2% at 162 mW/cm^2) and it remains the same after the films are exposed to the air for a few months.

The ρ values of nc-Si:H films measured in TFT structures are found as 1.1×10^8 Ωcm and 2.3×10^7 Ωcm for TFT1 and TFT2, respectively. In other words, channel layer of 140 nm deposited at 100 mW/cm^2 has similar ρ values with the corresponding test film, while the one deposited at 300 mW/cm^2 has 2 orders higher ρ values, compared to the corresponding films of higher thicknesses (Figure 6.3-a). The transfer characteristics of TFT1 and TFT2 are depicted in Figure 6.8. In the saturation region, TFT2 has lower $V_{T,SAT}$ of 4 V and slightly higher field-effect mobility ($\mu_{FE,SAT}$) of 0.06 cm^2/Vs when compared to those of TFT1. For

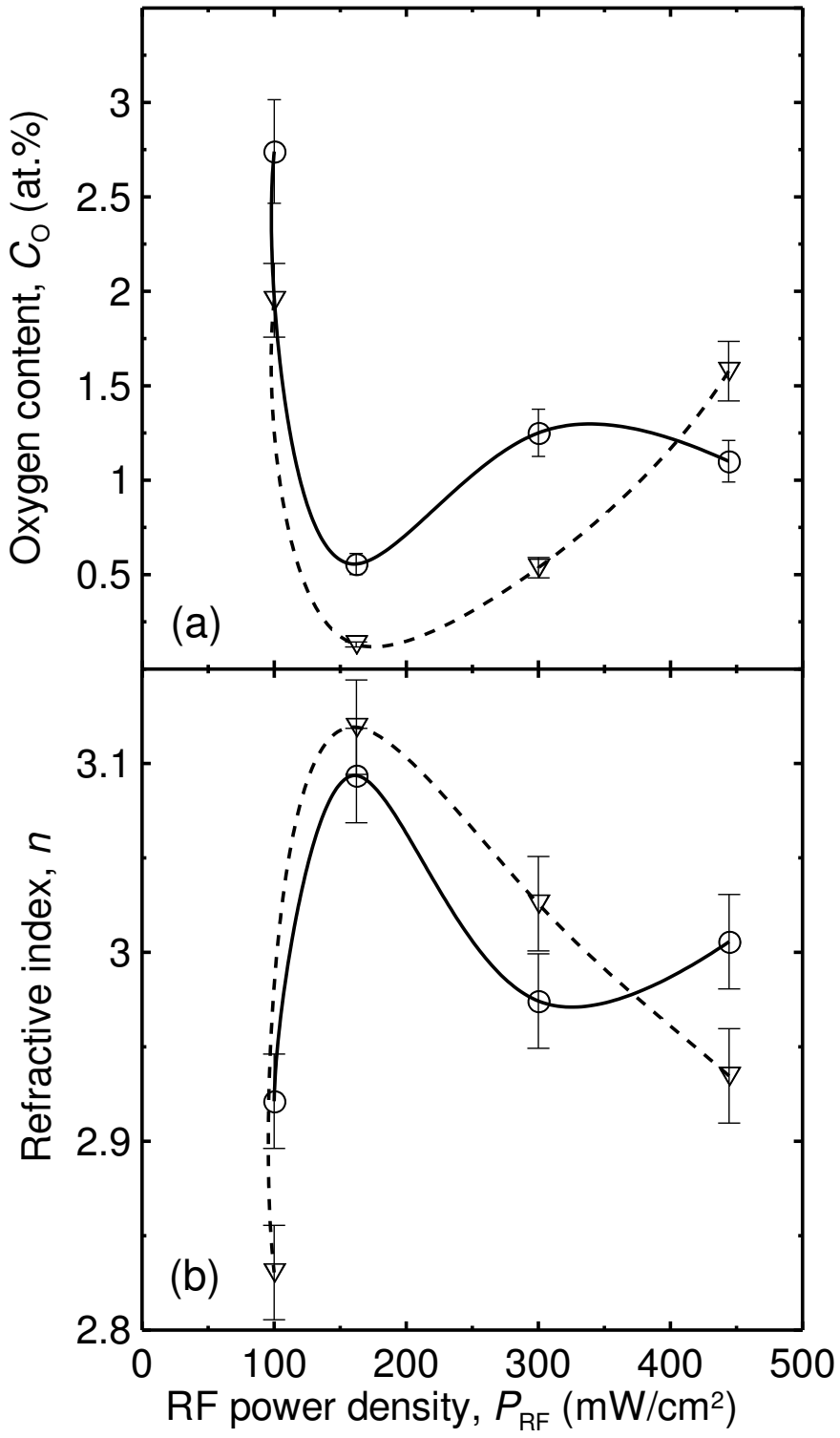


Figure 6.7: Change of (a) bonded oxygen content and (b) refractive index of nc-Si:H films, grown at the center (◯) and near the edge (▽) of the PECVD electrode, with applied P_{RF}.

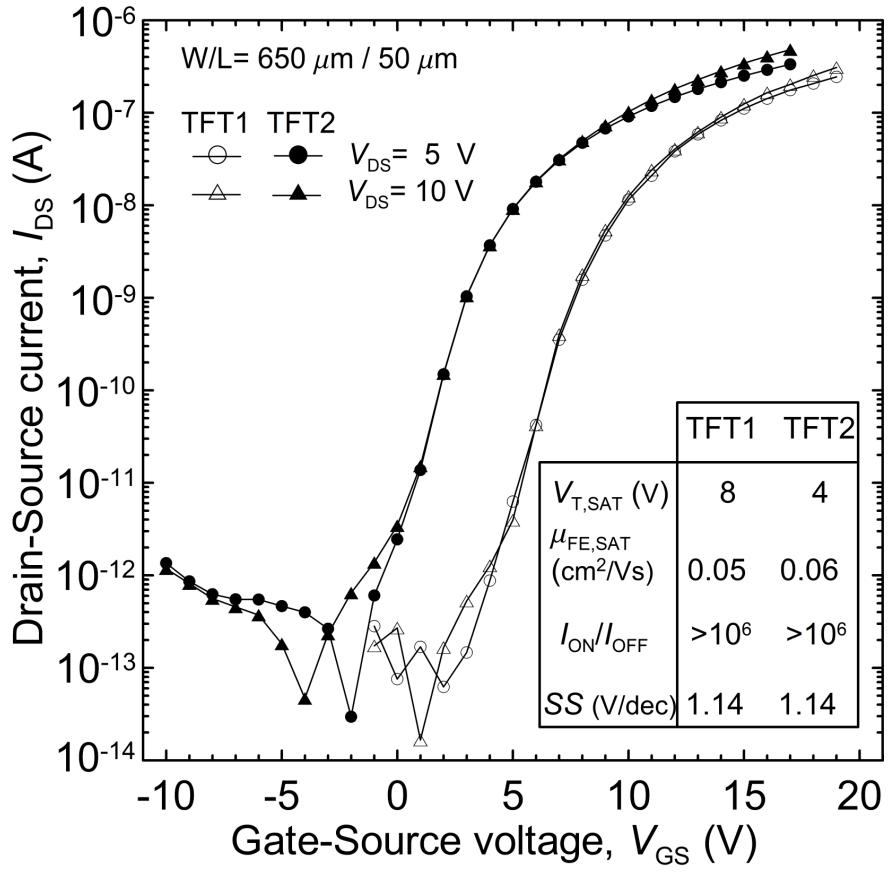


Figure 6.8: Transfer characteristics of TFT1 and TFT2 with extracted TFT parameters indicated in the inset.

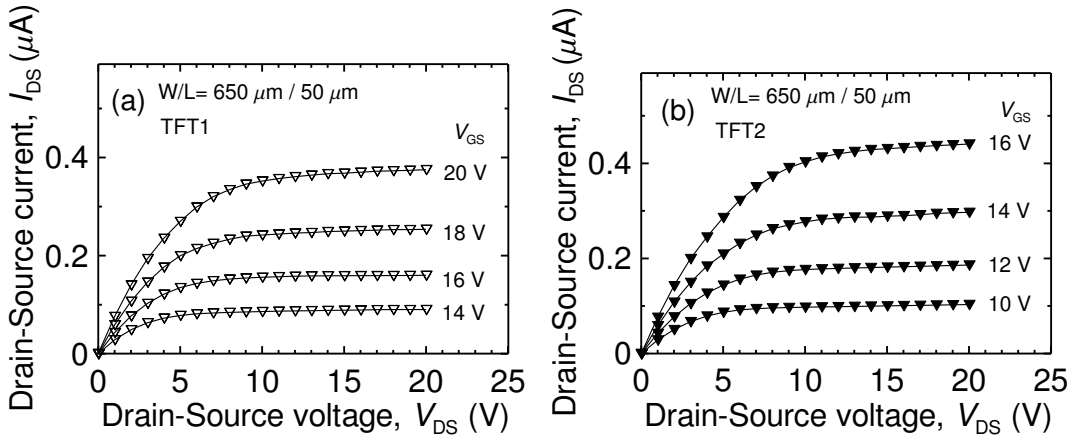


Figure 6.9: Output characteristics of (a) TFT1 and (b) TFT2.

both TFTs, I_{ON}/I_{OFF} ratio is >10^6 and subthreshold slope (SS) is 1.14 V/dec. The output $D-S$ current (I_{DS}) of TFT2 is slightly higher than that of TFT1 at the corresponding V_{GS} values giving the same $V_{GS}-V_{T,SAT}$, as it is shown in Figure 6.9.

For both TFT1 and TFT2, the initial transfer characteristics are parallelly shifted (Figure 6.10) when bias-stressed for 1.2×10^3 s under V_{DS} = 0 V at V_{GS} of 18 V and 14 V, respectively (keeping the same $V_{GS}-V_{T,SAT}$ = 10 V). The dynamics of the shifts, provided in the inset of Figure 6.10, show that the transfer characteristics of TFT2 is shifted for ~0.6 V after the first stress application for 3×10^2 s with no shift under further stressing, while that of TFT1 is continuously shifted with increasing stress time.

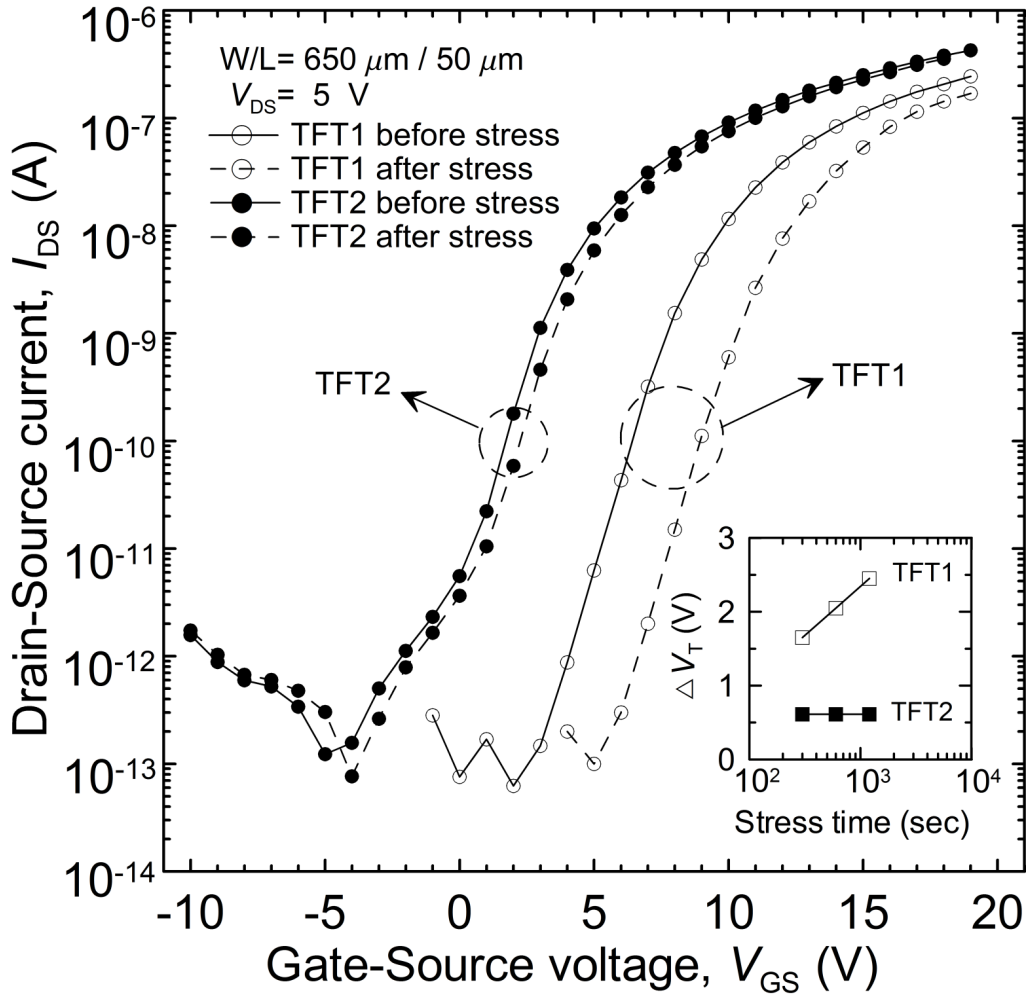


Figure 6.10: TFT transfer characteristics before and after stress for 1.2×10^3 s under V_{DS} = 0 V at V_{GS} = 18 V and 14 V for TFT1 and TFT2, respectively. The inset indicates the dynamics of the threshold voltage (V_T) shift. Here $I_{DS}-V_{GS}$ curve of TFT2 shifts for ~0.6 V after the first application of the stress and does not change with further stressing.

6.4 Discussions

6.4.1 Physical properties and their correlations

The XRD spectra and ρ values in Figure 6.2 and Figure 6.3-a, respectively imply that the films deposited at the center of the electrode are transformed from amorphous to nanocrystalline phase with increasing RF power. This is also supported by the gradual decrease in A_{2000} with increasing P_{RF} (Figure 6.3-b). In other words, the amount of Si−H bonds, attributed to isolated monohydrides in relaxed a-Si:H [54], decreases with increasing P_{RF}, which may be taken as a reduction in the volume fraction of amorphous tissue surrounding the nanocrystallites. Meanwhile, the emergence of A_{2090} accompanies the formation of crystallites covered by Si−H_2 bonds [54]. Also, Si−H_2 bonds might fill the internal surface of the possible voids, that are usually created parallel to the crystallite growth [54]. At 100 mW/cm^2, low R value is consistent with the higher A_{2000} and lower A_{2090}. In this frame, further increase in R with P_{RF} is confirmed by the gradual decrease and increase in A_{2000} and A_{2090}, respectively. This is interpreted as a rise in the crystalline volume fraction and larger grain and void surfaces are surrounded by Si−H_2 bonds. Therefore, here high R values indicate high fraction of the crystallinity, which was also noticed in earlier studies [58,59,68]. In the present work, this has been confirmed by the Raman scattering data for the films with high R (around 0.73−0.80), which resulted in 70−79% crystalline volume fraction. At 162 mW/cm^2 the amorphous part seems to be still dominant, as indicated by both the absence of XRD peaks and high ρ (Figure 6.2 and Figure 6.3-a). At 300 mW/cm^2, the crystallinity is determined by the detection of the XRD signals and supported by the reduction of A_{2000} and ρ. Amorphous structure of the films at P_{RF} of 100−162 mW/cm^2 is also supported by high C_H and E_0 value of 50 meV (Figure 6.4). E_0 increases up to 200 meV for more crystalline films, which rather should be a convolution of several subgap absorption tails probably related to the size and quality distributions of the crystallites. The slight decrease in Tauc slope B also suggests the increase in the overall disorder in the network caused by the nanocrystallization process (Figure 6.4-b) [58].

To discuss the band gap values it is useful to remember that the structure of nc-Si:H is usually defined as the nanocrystallites dispersed throughout the amorphous tissue. The confinement of the Si nanocrystallites within the a-Si:H medium is expected to increase the band gap energy from ∼1.1 eV (gap of c-Si) up to ∼1.8 eV (gap of a-Si:H) depending on the average crystallite size. Hence, the band gap energy of nc-Si:H should be less than 1.8 eV [63]. In this work, the optical gap values of the amorphous rich (P_{RF} of 100−162 mW/cm^2)

and nanocrystalline rich (P_{RF} of 300−444 mW/cm^2) films are similar independent of the used method, but their E_{04} and E_{Tauc} are higher than the usual gap of a-Si:H (Figure 6.6). It is, therefore, difficult to relate these larger gaps to the quantum confinement effect (QCE) of Si nanocrystallites only within the amorphous Si phase. The QCE seems to be enhanced by the high potential barrier at the eventual void interfaces. This explanation is consistent with the refractive indices of Figure 6.7-b, which are lower than that of both c-Si and a-Si:H. The refractive index might be reduced due to the possible voids in the structure [71, 73]. Besides, existence of the voids and correlation of C_O with n imply that oxygen diffuses into the films after breaking the vacuum.

As for the films grown near the edge of the electrode, the structure is nanocrystalline and has almost no variation with P_{RF}. For these films F_C, R, E_0 are higher and ρ, C_H, C_O are lower than for those grown at the center (Figure 6.3 and 6.4). The gap values are also slightly lower possibly due to higher crystalline volume fraction (Figure 6.3-a and Figure 6.6).

6.4.2 Film uniformity along the electrode

The large area non-uniformity is discussed in terms of nc-Si:H growth mechanism and correlated with the physical properties of the films discussed in the previous subsection. SiH_3 radical is the main precursor for both a-Si:H and nc-Si:H deposition [74] due to its higher density and longer lifetime within the plasma as compared to other radicals $SiH_{x<3}$. Two growth models have been proposed for nc-Si:H under the continuous growth conditions, where SiH_4 and H_2 gases are introduced simultaneously into the plasma. In the surface-diffusion model, the high hydrogen surface coverage increases the surface mobility of SiH_3 radical, which can then easily find the energetically favorable sites [39]. The etching model, explains the decrease in deposition rate with increasing hydrogen dilution ratio: here H etches Si species from the weak Si−Si bonds, then film growth occurs when empty site is replaced by a new SiH_3 radical leading to strong Si−Si bond [39].

In the present study taking into account the gas mixture entrance through the center of the top electrode, at P_{RF} of 100 mW/cm^2, SiH_3 and H radical densities are low at the center of the reactor resulting in low DR, while SiH_4 concentration should be high due to its low dissociation. Therefore, the easy reaction of H with SiH_4 probably occurs at the center of the electrode, which further decreases the H atom density in the plasma through the following

reaction [39]:

$$H + SiH_4 \rightarrow SiH_3 + H_2 \tag{6.2}$$

Consequently, H surface coverage is reduced, producing amorphous or less crystalline film structure consistent with the surface-diffusion growth model. Meanwhile, H atom and SiH_3 generation probability might increase towards the edge of the reactor due to the increased residence time of H_2 and SiH_4. Besides, accumulation of SiH_3 radicals toward the edges is likely owing to their long lifetime [39]. So, high H surface coverage with high SiH_3 concentration near the edges of the reactor seems to produce nanocrystalline films with higher *DR* near the edge of the electrode; while the lack of enough H and SiH_3 density at the center result in amorphous films with lower *DR*.

With increasing P_{RF} (162 mW/cm^2), more SiH_4 and H_2 are dissociated to generate more SiH_3 and H radicals which contribute to higher *DR* and higher *R* at the center of the electrode (Figure 6.1-a and 6.3-b). In parallel, *DR* of the films should have also increased near the edge of the electrode in response to higher P_{RF}. Hence, their almost constant *DR* might be regarded as an unexpected result (Figure 6.1-a). However, with increasing P_{RF}, the probability of reactions of the radicals with the molecules (mainly equation 6.2) is reduced at the center of the reactor due to the decreased density of SiH_4 and H_2. As a consequence of this interpretation, the density of SiH_3 produced by these reactions decreases and the density of H atoms increases towards the edge. Therefore, the expected increase of the *DR* near the edge may be hindered by lowered supply of SiH_3 from the center and enhanced etching effect of H. With further increase in P_{RF} (300−444 mW/cm^2), almost constant *DR* near the edges of the electrode and its lower values than at the center, can be related to the etching effect of high atomic hydrogen concentration near the edges, supplied mainly from the center of the reactor where it is not fully consumed. The excess H atom density at the center of the reactor is likely due to the depletion of SiH_4 molecules at such high P_{RF} and pressure, which in return decreases the annihilation of atomic H (equation 6.2). The higher crystallinity and lower C_H in the films near the edge of the electrode than those at the center may be other evidences for the high H atom etching effect at the edges (Figure 6.3-a and 6.4-a). Thus, the films near the edge seem to be highly influenced by the chemical species supplied from the center of the reactor, i.e. from their production domain.

At 300 mW/cm^2, the *DR* of the films grown at the center of the electrode increases, while resistivity decreases down to the values of the films near the edge (Figure 6.1 and 6.3-a). In

this power regime, the XRD peaks of nanocrystallites are detectable also in the spectrum of the films at the center (Figure 6.2). The increased P_{RF} probably results in higher H atom density due to both enhanced dissociation of H_2 and decreasing annihilation of H via equation 6.2 by the fewer SiH_4 molecules. Then, the amount of H should be enough for the surface coverage which promotes the nanocrystallite formation according to the surface-diffusion growth model [39].

At the highest P_{RF} (444 mW/cm^2) higher ρ, A_{2000} and C_H as compared to those obtained at 300 mW/cm^2 can be regarded as a slight degradation of the film properties (Figure 6.3 and 6.4-a). This further increase in P_{RF} probably leads to almost complete dissociation of the SiH_4 molecules. This depletion of SiH_4 reduces its reaction probability with the short life-time radicals ($SiH_{x<3}$) [39]. Therefore, the contribution of these radicals to the film growth increases, which is undesirable for the film quality due to their lower surface-diffusion coefficients in contrast to SiH_3 [75]. This contribution is likely to dominate at the center of the electrode, where DR and ρ is much higher than those near the edges (Figure 6.1-a and 6.3-a). Another possible reason for the film deterioration at 444 mW/cm^2 is that the further increase in the plasma potential raises the ion bombardment during the deposition process. To investigate this possibility, nc-Si:H films were deposited at the same P_{RF} (444 mW/cm^2) but under higher pressure (2 Torr), which should decrease the ion energy and thus decrease its negative effect on the film properties [39]. Raising the pressure twice prolonged the residence time of the molecules and consequently increased the deposition rate by 3 times (14.5 and 11.8 nm/min for the films at the center and near the edge, respectively), leaving the DR_{edge}/DR_{center} ratio unchanged. On the other hand, both high and low pressure deposited films exhibit very similar physical properties. Therefore, the slight deterioration in the film properties at 444 mW/cm^2 is not likely to arise from the enhanced ion bombardment.

6.4.3 TFT application

High ρ values of TFT1 channel suggest the formation of a-Si:H film at 100 mW/cm^2 (see Figure 6.3 and 6.4). As compared to the thicker film of 470 nm deposited at 300 mW/cm^2, the increased ρ of 140 nm TFT2 channel suggests the presence of the less crystalline incubation layer, above which more crystalline film is formed [16, 23]. Despite the fact that main part of the TFT channel is formed by this incubation layer, the nc-Si:H channel of TFT2 lowers the V_T and enhances the TFT stability compared to TFT1 of a-Si:H channel. Decrease in V_T can be attributed to the possibly higher initial free carrier concentration inside the channel of

TFT2 than that of TFT1 [15]. Besides, use of three times higher power during the deposition of TFT2 channel layer would increase the etching effect on the top of the silicon nitride and thus would decrease the number of positive charge-trapping centers, probably created from the weak N_3Si-H and N_3Si-dangling bonds [57, 76]. This decrease in density of positive charge-trapping centers can be taken as another factor lowering V_T [76]. On the other hand, higher power did not result in any deterioration of the a-SiN_x:H/nc-Si:H interface in TFT2 as it is concluded from the similar *SS* values. The enhanced electrical stability of TFT2 can be correlated with the increased volume of nanocrystallites in the channel, which reduces the probability of defect state creation [20, 25, 77]. A slightly higher μ_{FE} and off-current in TFT2 are other consequences of the higher nanocrystalline fraction in TFT2 channel.

6.5 Conclusion

The physical properties and large area uniformity of PECVD grown nc-Si:H films are affected by the behavior of the plasma species at different RF power regimes. With increasing power, the phase of the films deposited at the center of the PECVD electrode is transformed from amorphous to nanocrystalline. On the other hand, films near the edge of the electrode are of nanocrystalline phase and have almost the same properties at all P_{RF}. All the films are considered to contain voids and their oxygen content is correlated with the refractive index. The large gaps are interpreted via the quantum confinement within the Si nanocrystallites surrounded by amorphous tissue and voids.

The large area uniformity in the film properties is attained under conditions of increased silane and hydrogen dissociation, and decreased probability of the reaction of silane with atomic hydrogen. From the aspect of the large area uniformity and nc-Si:H film quality, the optimum P_{RF} lies around 300 mW/cm^2 in the present geometry of the reactor.

BG TFT with the nanocrystalline channel layer deposited at an optimum P_{RF} exhibited lower V_T and improved electrical stability when compared to the TFT with the amorphous channel layer grown at a lower P_{RF}. Also, the use of higher P_{RF} slightly increased μ_{FE} and seems not to alter the a-SiN_x:H/nc-Si:H interface.

CHAPTER 7

CAPACITANCE ANALYSES OF HYDROGENATED NANOCRYSTALLINE SILICON BASED TFT

7.1 Introduction

It has been presented previously in section 3.3 and chapter 6 that the hydrogenated nanocrystalline silicon thin film transistor (nc-Si:H TFT) has been extensively studied due to its better electrical stability and higher mobility as compared with the hydrogenated amorphous silicon (a-Si:H) counterpart. Besides, the low-cost deposition conditions for nc-Si:H film do not much differ from those of a-Si:H film. However, during the deposition of the former, an a-Si:H rich incubation layer formation of thickness within 30−70 nm prior to the nanocrystalline-rich bulk, reduces the quality of the insulator/nc-Si:H interface resulting in low device performance for the bottom-gate (BG) TFT [78, 79]. Also, the two-phase structure of nc-Si:H material, where nanocrystallites are embedded in the a-Si:H matrix, and its columnar growth affect the electrical transport mechanism within the TFT channel [42, 80, 81]. One of the tools to investigate the interface and the bulk properties of the TFT channel in detail is the admittance spectroscopy. So far, the admittance measurements have been applied to a-Si:H TFT and metal-insulator-a-Si:H (MIAS) structures [82–85]. These studies consisted of electron accumulation capacitance within 10^7-10^3 Hz frequency range [82, 83] and quasi-static measurements of "hole capacitance" at large reverse bias [84, 85]. The analysis in the low frequency regime, between quasi-static and 1 kHz seems to be important for investigating deep trap and/or inversion carrier contributions. This work examines the capacitance measurements, within 10^6-10^{-2} Hz, of both gate-drain/source ($G-D/S$) terminals in the nc-Si:H BG TFT and the MIAS structure, mechanically isolated from the same TFT.

7.2 Experimental details

In this chapter the TFT2 structure was investigated. Its deposition conditions are described in Table 4.1 and outlined below. For the gate electrode of the BG TFT, 200 nm Cr thin film was grown on the glass substrates by e-beam deposition technique. First, the gate insulator, a-SiN_x:H (~600 nm), was deposited on these Cr coated glass substrates in the PECVD system at 13.56 MHz from NH_3+SiH_4 gas mixture (NH_3/SiH_4~19) at 0.5 Torr, under RF power density (P_{RF}) of 100 mW/cm^2 and at substrate temperature of 523 K. Then, for the deposition of the intrinsic (~140 nm) and n^+ doped (~45 nm) nc-Si:H layers, the substrate temperature (473 K), the H_2 dilution ratio ($H_2/(H_2+SiH_4)$=99%), the deposition pressure (1 Torr) and the P_{RF} (300 mW/cm^2) were adjusted. Also, during the n^+ layer deposition PH_3 was added to H_2-SiH_4 gas mixture with the PH_3/SiH_4 ratio ~0.6%. Al film (~130 nm) was thermally evaporated on the last n^+ nc-Si:H layer. The D and S contacts were formed by patterning Al layer using standard photolithographic method and then n^+ nc-Si:H layer beyond D and S contacts was removed by the reactive ion etching (RIE) technique in R-12 atmosphere at 0.1 Torr under P_{RF} of 450 mW/cm^2. For separating TFTs from each other, a second photolithographic step was applied. Then, nc-Si:H and a-SiN_x:H layers between the TFTs were removed by RIE until gate metal is reached as depicted in Figure 7.1-a. Finally, a post-deposition annealing at 423 K for 0.5 h was performed to improve the performance of the device. The TFT structure in Figure 7.1-a was used in both current-voltage ($I-V$) and capacitance-voltage ($C-V$) measurements for characterizing the TFT by Keithley voltage source/electrometer (K230/K617) and Novocontrol Alpha-A High Performance Frequency Analyzer, respectively. During $C-V$ measurements of the TFT structure shown in Figure 7.1-a, the voltage bias was applied between the G and the short-circuited D/S ($G-DS$). The MIAS structure (Figure 7.1-b) was obtained by RIE of nc-Si:H and a-SiN_x:H layers using D and S electrodes as Al mask. Therefore, a true MIAS structure with the G as one electrode and the S (or D) as opposite electrode was formed to exclude lateral current flows across the silicon film during the electrical measurements. In this work, $C-V$ measurements performed on the MIAS structure ($G-S$ contacts) were studied in details and compared with those of the TFT structure.

For measuring the insulator capacitance alone, a-SiN_x:H was deposited on the Cr coated glass under the same conditions used in the growth of the TFT gate insulator. Then, Al dots were evaporated above the insulator film, thus forming Cr/a-SiN_x:H/Al sandwich-like metal-insulator-metal (MIM) structure.

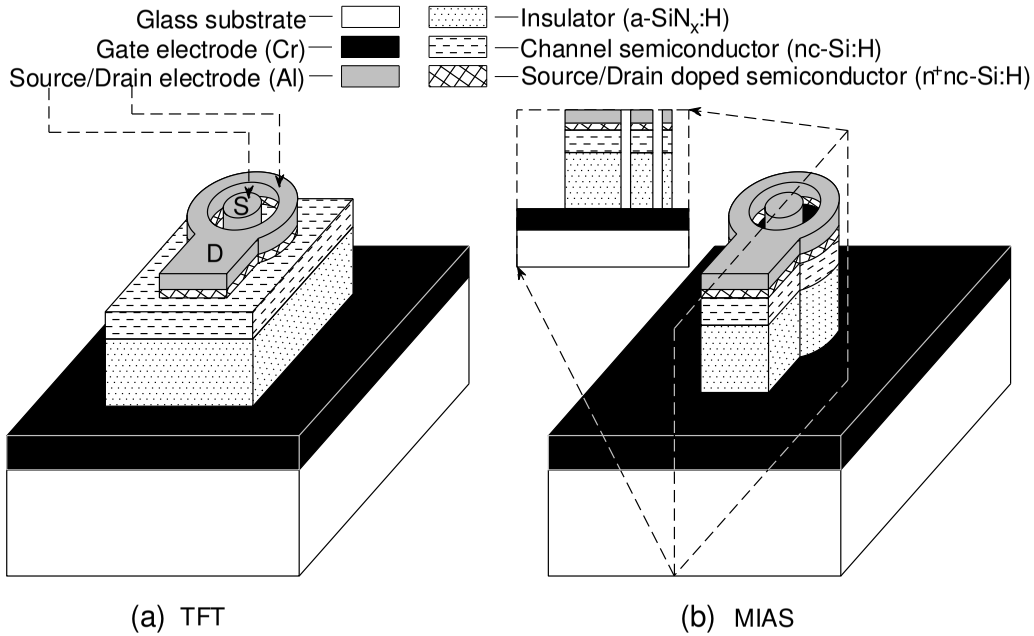


Figure 7.1: (a) One of the TFT islands obtained using photolithographic method followed by the dry etching of nc-Si:H and a-SiN_x:H layers to separate TFTs. (b) The MIAS structure derived from some TFT islands by reactive ion etching of nc-Si:H and a-SiN_x:H layers using Al contacts as mask.

The lateral dc electrical conductivity σ (and its activation energy) of the nc-Si:H film between 300 and 420 K was obtained through $I-V$ curves on both the channel layer (~140 nm) of the TFT at hand and the planar structure of Al/nc-Si:H (~470 nm)/glass substrate.

7.3 Results

7.3.1 TFT and MIAS structures

The TFT output and transfer characteristics measured on the TFT structure are presented in Figure 7.2. In Figure 7.2-a, absence of the "current crowding" at low $D-S$ voltages (V_{DS}) implies good $D-S$ contact properties [30]. Low gate-source current (I_{GS}) in Figure 7.2-b indicates good insulating property of a-SiN$_x$:H. The TFT parameters are reported in the inset of Figure 7.2-b for the linear and saturation regions. Although the mobility values (μ_{FE}) are still quite low, the threshold voltage (V_T), I_{ON}/I_{OFF} ratio and the subthreshold slope (SS) are comparable to the previously reported ones for nc-Si:H BG TFTs [16]. The off-current at $V_{GS} < -3$ V in the reverse subthreshold region (see Figure 7.2-b) has a drain-bias dependence and corresponds to the weak electron conduction mostly at the back channel [86], i.e. upper part of the nc-Si:H film. The high reverse SS value is associated with the higher density of states (DOS) at the back surface of the channel layer compared to that at the front interface [86]. Also, the off-current has low values relatively to the usually reported ones for nc-Si:H BG TFTs [25] and therefore results in high I_{ON}/I_{OFF} ratio. Besides, compared to a-Si:H TFTs, this TFT has higher electrical stability and lower V_T, which were optimized through the deposition conditions of the nc-Si:H film in a previous chapter.

Capacitance−voltage ($C-V$) characteristics of the same TFT structure are shown in Figure 7.3-a within 10^6-10^{-2} Hz frequency range. The insulator capacitance (C_{SiN}) measured as 10.5 nF/cm^2 from the MIM structure is found to be bias and frequency (F) independent. The C_{SiN} values for the actual effective areas are reported on Figure 7.3 as the dashed lines. In Figure 7.3-a, the frequency and voltage independent value of 57 pF for accumulating positive V_{G-DS} values at low frequencies ($F<10^2$ Hz) is substantially larger than the value of C_{SiN}, expected for the actual gate area defined by the short-circuited D/S Al electrode. This value corresponds to C_{SiN} with effective area enlarged over the whole TFT island of the conducting nc-Si:H layer as depicted in Figure 7.1-a. The C_{SiN} value of about 28 pF, corresponding to the actual D/S Al gate area is attained for high frequencies ($F\geq10^6$ Hz). Consequently, an eventual formation of the thin accumulated electron layer over the TFT island interface

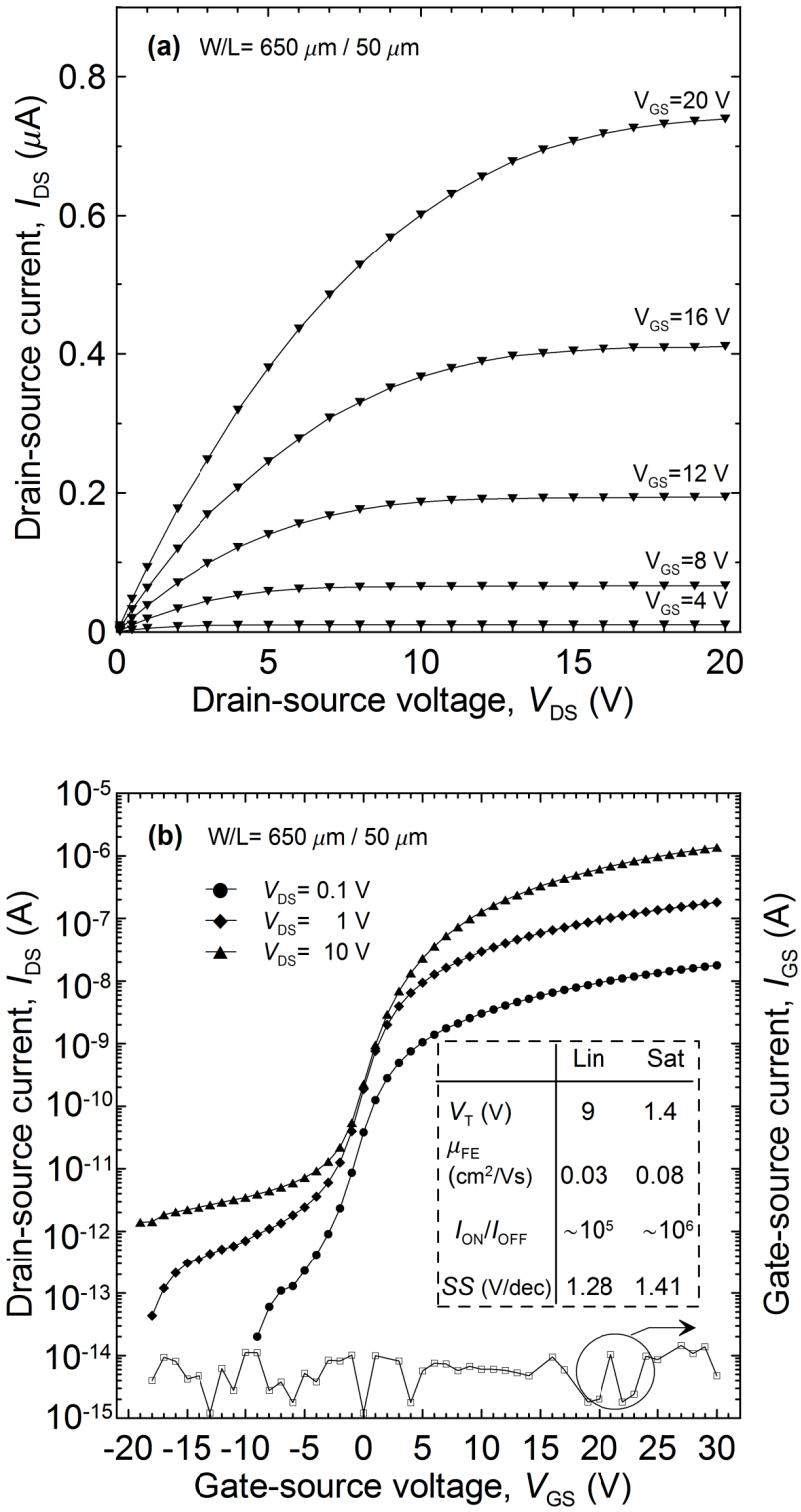


Figure 7.2: (a) Output and (b) transfer characteristics of nc-Si:H TFT. (b) Extracted parameters are shown in the inset for the linear (V_{DS}=0.1 V) and saturation (V_{DS}=10 V) regions.

in the accumulation regime complicates the results and may lead to misinterpretations. The above interpretation was tested as follows: one of the TFT structures was subjected to dry etching in order to reduce the laterally extended nc-Si:H/a-SiN$_x$:H bulk beyond the D and S electrodes to the same area as these electrodes as shown in Figure 7.1-b. After this etching process, the resulted $C-V$ curves (Figure 7.3-b) are now as expected, since the accumulation capacitance is in agreement with the measured C_{SiN} from the MIM structure of area equal to Al source electrode area. At high frequencies (HF), the accumulation capacitance shows frequency dependence roughly similar to earlier findings in a-Si:H TFT, MIAS structures and

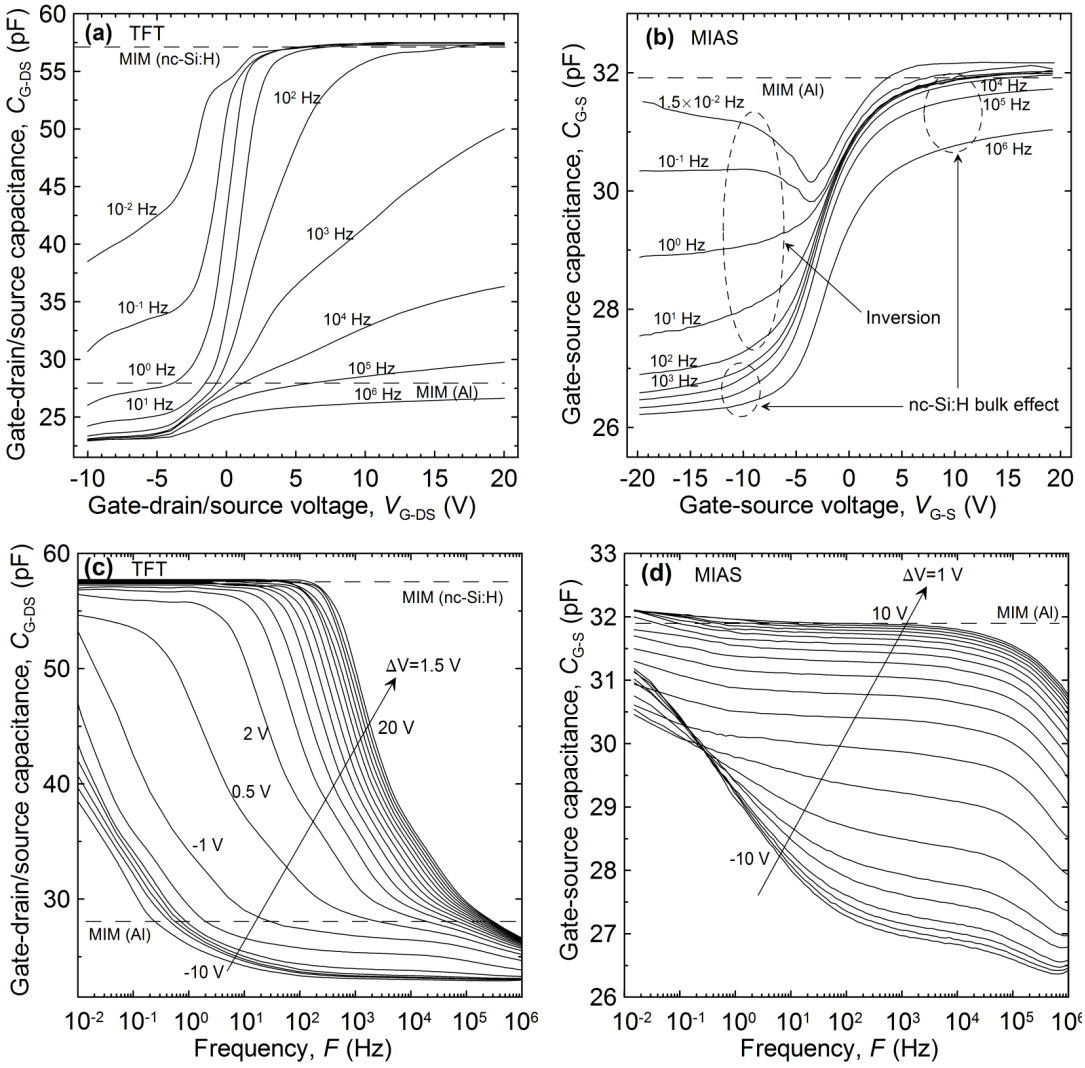


Figure 7.3: $C-V$ characteristics of (a) TFT and (b) MIAS structures given at various frequencies. $C-F$ curves of (c) TFT and (d) MIAS structures at bias varying by steps of 1.5 V and 1 V for (c) and (d), respectively. The dashed lines indicate the a-SiN$_x$:H insulator capacitance obtained from the MIM structure for the given Al electrode and nc-Si:H film areas.

is attributed to the nc-Si:H neutral bulk effect [76, 82]. Moreover, in Figure 7.3-b there is similar frequency dependence at the reverse bias for HF regime and the hole accumulation (or inversion) for low frequencies (LF). The $C-F$ curves are given in Figure 7.3-c,d for both TFT and MIAS structures. In Figure 7.3-c the main change in the capacitance in the TFT structure from 28 pF to 57 pF is mostly attributed to the extension of the effective gate area beyond the D/S electrodes. In the case of the MIAS structure (Figure 7.3-d) capacitance increase at HF comes from the nc-Si:H bulk, while at LF for the reverse bias it stems from the hole accumulation.

7.3.2 Capacitance fitting results for the MIAS structure

The method of fitting $C-F$ curves [82] was applied to the capacitance measurements of the present MIAS structure to deduce its electrical properties. The energy band diagrams with corresponding equivalent circuit models (ECM) used in fitting $C_{G-S}-F$ curves for the inversion-depletion (from -10 V to -2 V) and accumulation (from -1 V to 10 V) regimes are depicted in Figure 7.4-a and 7.4-b, respectively [82, 84]. C_{SiN} was previously determined

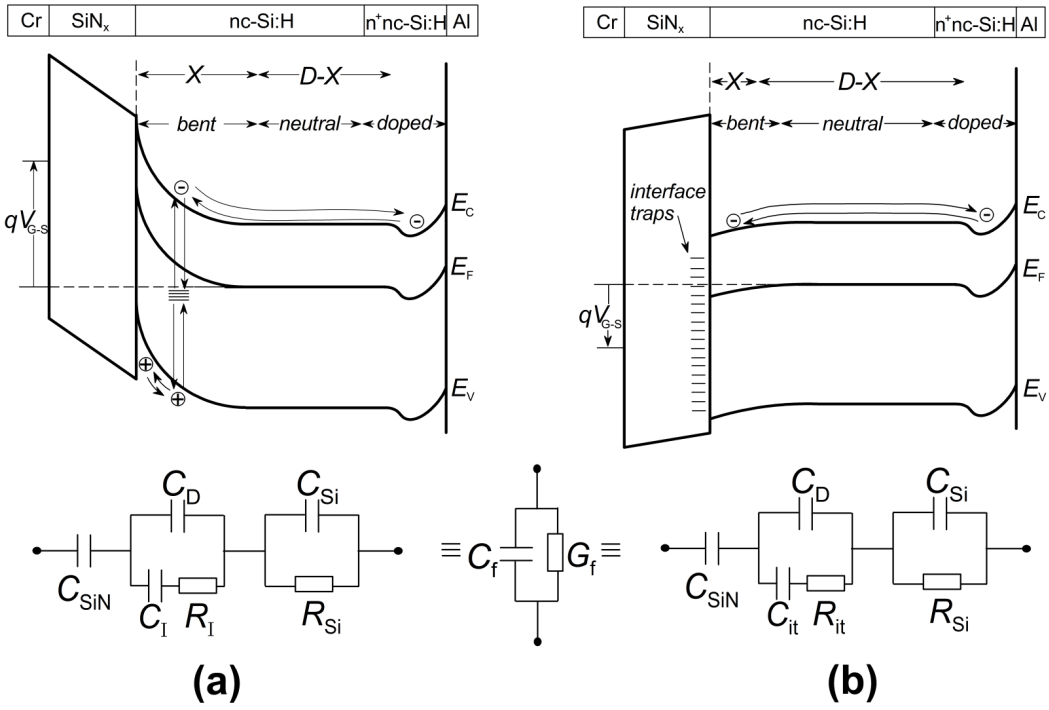


Figure 7.4: The energy band diagram and equivalent circuit model of the MIAS structure for the (a) inversion-depletion and (b) accumulation regimes.

from the $C-V$ measurements of the MIM structure by adapting its electrode area to the MIAS one. C_{Si} and R_{Si} stand for the nc-Si:H bulk capacitance and resistance, respectively. C_D is the depletion capacitance in the depletion and the Debye capacitance in the accumulation regimes. The capacitance of the inversion C_I (or interface states C_{it}) is in parallel to C_D. R_I is the resistance due to the generation-recombination process in the inversion regime. R_{it} is the resistance due to the capture (or emission) of electrons by the interface traps and can be determined in the inversion-free depletion regime. As a result of the ECM, the frequency (or ω=2πF) dependence of the total capacitance is expected to come from both the nc-Si:H bulk at HF and the inversion at LF. Since both circuits of Figure 7.4 have the same nature, the expressions for the fitted capacitance (C_f) are the same but with the substitution of R_{it} for R_I:

$$C_f(\omega) = \frac{C'_{SiN}}{1 + \omega^2 R'^2 C'^2_{SiN}} \tag{7.1}$$

where

$$C'_{SiN} = \frac{C_{SiN}\left[\frac{C'_p C'_{Si}}{C'_p + C'_{Si}}\right]}{C_{SiN} + \left[\frac{C'_p C'_{Si}}{C'_p + C'_{Si}}\right]}, \qquad R' = R''_I + R'_{Si} \tag{7.2}$$

$$C'_{Si} = \frac{1 + \omega^2 R_{Si}^2 C_{Si}^2}{\omega^2 R_{Si}^2 C_{Si}}, \qquad R'_{Si} = \frac{R_{Si}}{1 + \omega^2 R_{Si}^2 C_{Si}^2} \tag{7.3}$$

$$C'_p = \frac{1 + \omega^2 R'^2_I C_p^2}{\omega^2 R'^2_I C_p}, \qquad R''_I = \frac{R'_I}{1 + \omega^2 R'^2_I C_p^2} \tag{7.4}$$

$$C_p = C_D + \frac{C_I}{1 + \omega^2 R_I^2 C_I^2}, \qquad R'_I = \frac{1 + \omega^2 R_I^2 C_I^2}{\omega^2 R_I C_I^2} \tag{7.5}$$

$$C_{Si} = \frac{\varepsilon_r \varepsilon_0 A}{D - X}, \qquad C_D = \frac{\varepsilon_r \varepsilon_0 A}{X} \tag{7.6}$$

Here, ε_r and ε_0 are the dielectric constant of nc-Si:H film and free space, A is the area of the MIAS structure, D is the thickness of the intrinsic nc-Si:H layer, X is the depletion width in depletion and Debye length (L_D) in accumulation regimes. The fitting was done in MATLAB environment by the program written for the above equations with the use of fitminsearch optimization function.

Some of the resulted fitted C_f-F curves are represented in Figure 7.5. The very low frequency part ($10^{-1}-10^{-2}$ Hz) of the curves was not covered by the fit (here a slight increase

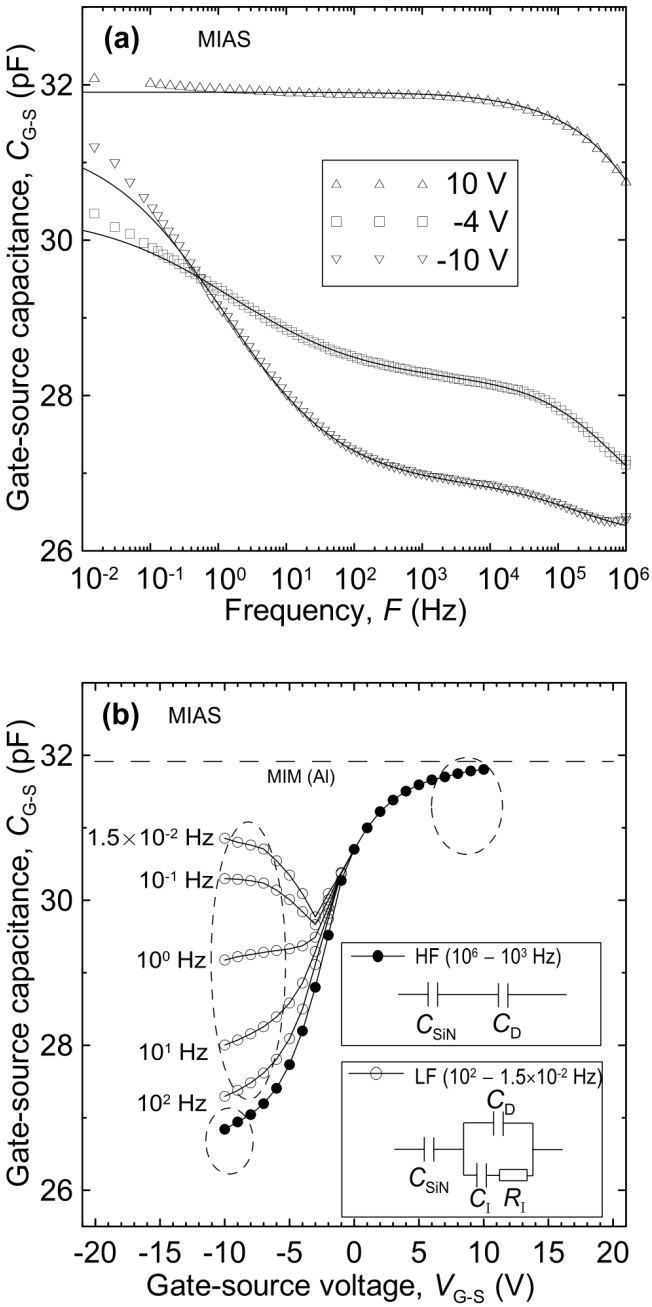


Figure 7.5: (a) Measured (symbols) and fitted (lines) $C-F$ curves of the MIAS structure shown for several bias voltages. Artifact at $10^{-1}-10^{-2}$ Hz is not covered by the fit. (b) Capacitance data constructed from the HF and LF circuits in which the bulk effect is removed as shown in the insets. Here C_D, C_I and R_I are the values obtained from the fitting of MIAS $C-F$ curves. The frequency dependence of the indicated regions due to the nc-Si:H bulk at HF is removed in both accumulation and depletion regions leaving inversion at LF for negative bias (compare with Figure 7.3-b).

in the capacitance may come from the moisture induced current flow at the edges of the channel layer [87]). One of the main results deduced from the fitting is that the resistances of the present work (R_{Si}, R_I and R_{it}) are frequency dependent. The resistances were expressed in the form Kω^{-s}, where K is a constant and s is found around 0.64−0.75 (depending on the type of the carriers and bias voltage), which is consistent with the ac hopping conductivity [88].

The frequency dependence of the capacitance in the inversion region is due to both the nc-Si:H bulk at HF and the inversion at LF (see −10, −4 V curves in Figure 7.5-a). In accumulation region the frequency dependence is only at HF and is due to nc-Si:H bulk (see 10 V curve in Figure 7.5-a). This can be easily distinguished in Figure 7.3-b and Figure 7.5-b, where in the former both effects are present in $C-V$ curves, while in the latter only the inversion effect remains after the removal of the bulk effect. Here, the contribution of the interface state density is omitted for a rough estimation of the total capacitance at HF, C_{HF}.

Interface state density, D_{it}, may be evaluated by using fitting results from the relevant conductance peaks given by equation 7.5 at various depletion voltages [87]:

$$D_{it} = \frac{(G'_{it}/\omega)_{max}}{(0.402q^2A)}. \tag{7.7}$$

In order to find the distribution of D_{it} in the energy gap of nc-Si:H, the estimation of the Fermi level, E_F, and the relation of the band bending, Ψ_s, to V_{G-S} should be found. For this purpose, the activation energy, E_A, of the dc conductivities, σ, of nc-Si:H films was obtained by measuring $I-V$ curves at different temperatures (T) within 300−420 K. However, E_A was found dependent on the thickness of nc-Si:H film (Figure 7.6-a). For the thinner film in the TFT structure E_A=0.68 eV is found, while a thicker nc-Si:H film grown at the same conditions has higher conductivity and lower E_A of 0.33 eV. As discussed later, the lower value of E_A is attributed to higher nanocrystalline fraction [89] in the top region of the film, while higher E_A for the TFT channel layer indicates that a-Si:H rich film is formed in the incubation layer (see Figure 7.6-b). So, the resulted 0.68 eV is considered as the Fermi energy measured from the conduction band as shown in Figure 7.6-b. Besides, due to the amorphous rich nature of the nc-Si:H TFT channel the well-known analysis of the space charge (η) formation in a-Si:H can be applied to the MIAS structure. Figure 7.7-a shows the energy band diagram of the MIAS structure together with the variation of η under the depletion condition. The shaded region about E_F contains the localized gap states of density N and is depleted of electrons [90]. By neglecting contributions of curved parts in I and III regions in Figure 7.7-a, the space charge is considered constant, $\eta = qN$, and then the slope of $1/C^2{}_{HF}-V_{G-S}$ supplies N (Figure 7.7-

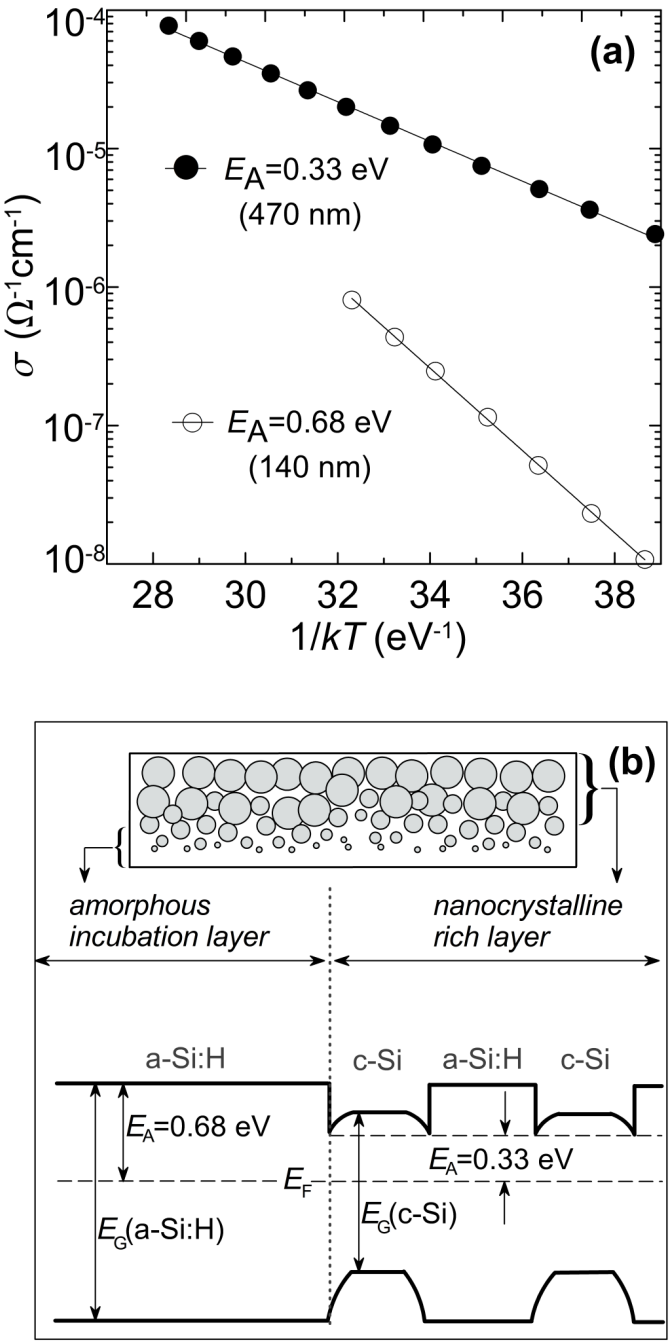


Figure 7.6: (a) Conductivity found from the ohmic region as a function of reciprocal temperature for the TFT with 140 nm nc-Si:H active layer and for the Al/nc-Si:H/glass structure with 470 nm nc-Si:H film. The resulted dc activation energy, E_A, is indicated for both cases. (b) Schematic cross view of nc-Si:H film: initially formed amorphous incubation layer gradually evolves into nanocrystalline-rich bulk. The E_A, found in part (a), is illustrated on the energy band diagrams (adapted from [89]) corresponding to these layers.

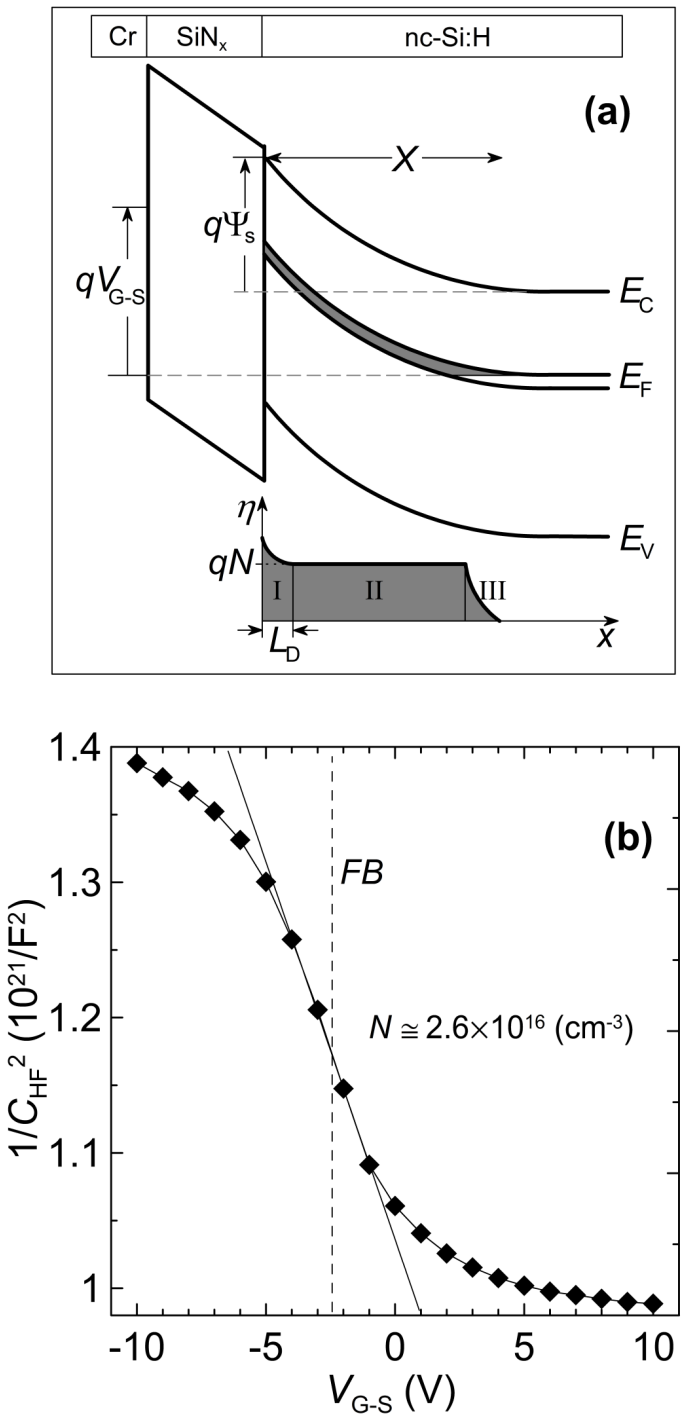


Figure 7.7: (a) Energy band diagram of MIAS in the depletion regime and corresponding space charge distribution. The shaded region about E_F represents the empty localized states of density *N*. (b) $1/C^2_{HF}$ vs. V_{G-S} with the slope equal to *N*. *FB* corresponds to the flatband voltage.

b). Here the flatband voltage, V_{FB}, around −2.4 V is determined from the Debye length of nc-Si:H (region I in Figure 7.7-a), $L_D=(\varepsilon_r\varepsilon_0/(q^2N_T))^{1/2}$ [91]. For this, the density of the localized gap states around E_F, N_T, is calculated from the above found *SS* of the TFT using the relation $SS=qkT(N_Tt_s+D_{it})/(C_{SiN}Log_{10}(e))$ [92], where k is the Boltzmann constant, t_s is the channel layer thickness and D_{it} is taken 0. From the resulted N_T (~9.4×10^{16} $cm^{-3}eV^{-1}$) L_D is around 77 nm and the Debye capacitance ($C_D\varepsilon_r\varepsilon_0A/L_D$) in series combination with C_{SiN} gives the *FB* capacitance of ~29.2 pF on C_{HF} curve. The interface state conductance peaks determined from the fitting results and D_{it} at various gate voltages are depicted in Figure 7.8-a,b. Now, the band bending can be estimated as $\Psi_s=qNX^2/(2\varepsilon_r\varepsilon_0)$ [93] (Figure 7.8-c) and

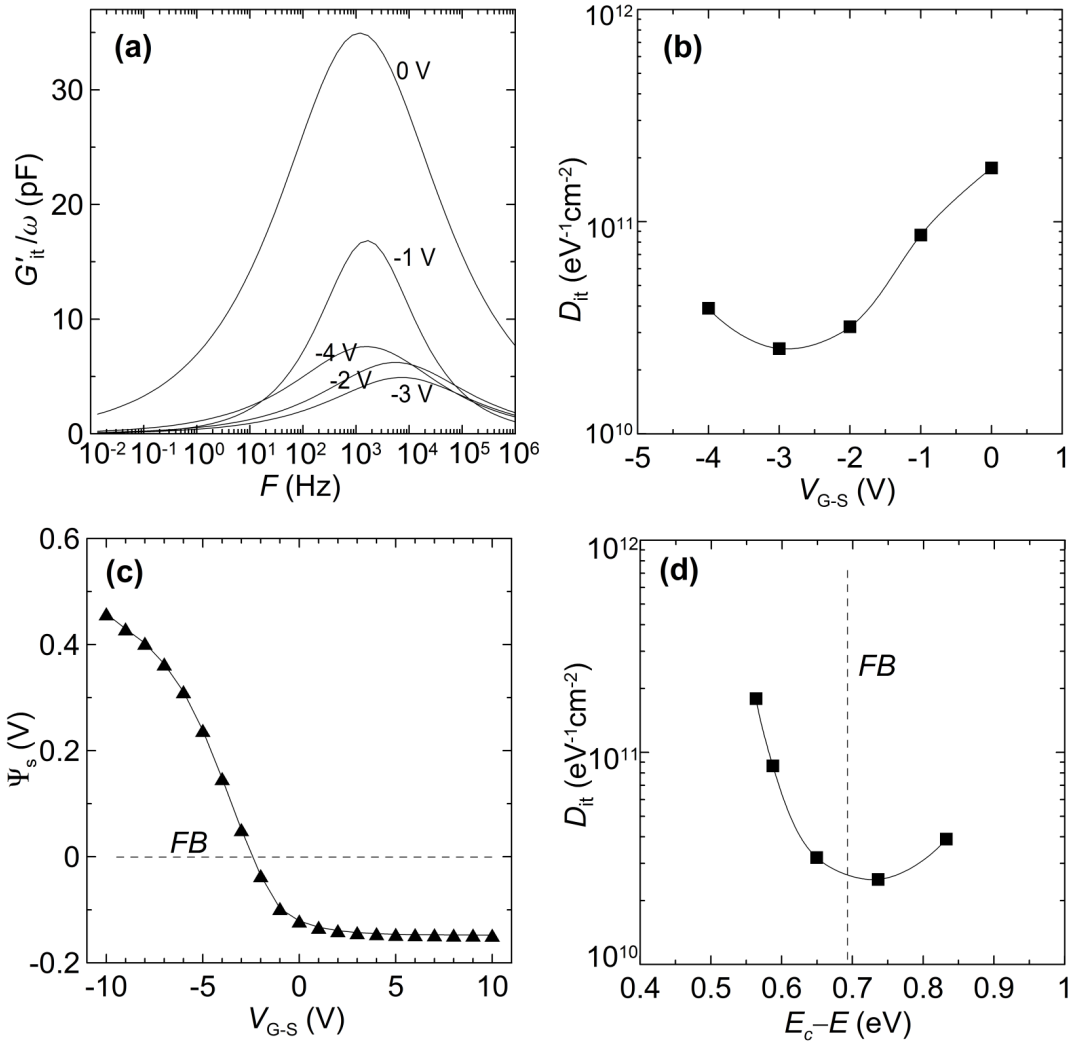


Figure 7.8: (a) Plot of the interface state conductance vs. frequency using the fitting results at various gate voltages. (b) The interface state density (D_{it}) as a function of gate voltages. (c) Band bending (Ψ_s) vs. V_{G-S}. (d) Distribution of D_{it} in the energy gap of nc-Si:H.

taking into account the above results of E_F and FB, the energy dependence of D_{it} is obtained by $E_C - E = E_F + q\Psi_s$ (Figure 7.8-d).

7.4 Discussion

7.4.1 Effective area expansion in the TFT structure

It can be concluded from Figure 7.3 that in the accumulation regime the conducting electron layer is formed at the a-SiN_x:H/nc-Si:H interface with the effective area enlarged over the whole TFT island. The formation of this layer is revealed in Figure 7.3-a by the large step in the capacitance for $V_{G-DS} > -1$ V at $10^5 - 10^2$ Hz. Here the low capacitance step from -5 V to -1 V corresponds to the step in the MIAS structure (Figure 7.3-b), i.e. electron accumulation increases due to the band bending near the TFT interface. At positive V_{G-DS}, the electron layer increases its effective area up to the TFT island area when frequency decreases from 10^5 to 10^{-2} Hz (see Figure 7.3-a). In other words, it requires time to get an ac response from the electrons that are more distant from D/S electrode, therefore the whole TFT island area acts as a capacitor plate only at $10^1 - 10^{-2}$ Hz for $V_{G-DS} > 3$ V. In the case of the negative bias application, the increase of the effective area by the hole layer is also expected. In fact, at $10^0 - 10^{-2}$ Hz the hole capacitance increases due to the increase in the effective area (compare Figure 7.3-a and b). However, this expansion of the area is not as much as in the electron case: even at 10^{-2} Hz the hole capacitance values do not approach accumulation value (Figure 7.3-a) as it is expected from the MIAS structure (Figure 7.3-b). This may happen owing to the lower hole conductivity compared with the electron one. The situation when the hole accumulation could not electrically connect D and S contacts was observed previously [84], and in the present study the effective area increase in the hole capacitance is possible only at low frequencies ($10^0 - 10^{-2}$ Hz).

As mentioned above, the effective area expansion of the TFT structure has frequency dependence easily followed by Figure 7.3-c. Here, $C_{G-DS} - F$ has three steps in the accumulation regime: the small step at $10^5 - 10^6$ Hz up to 28 pF, having the same origin with that of the MIAS structure at HF in Figure 7.3-d; and mainly two large steps between MIM (Al) and MIM (nc-Si:H) capacitances (one at 28−37 pF and the other at 37−57 pF), coming from the increase in the effective area and shifting to the higher frequencies as V_{G-DS} increases. The small step of $C_{G-DS} - F$ is shadowed and therefore it is analyzed in the MIAS structure. The origin of the formation of the two large $C_{G-DS} - F$ steps can be explained by the equiv-

alent network of the TFT structure provided in Figure 7.9 (adapted from [94] and modified for the TFT case). Here the *D*/*S* electrode is shown as the one electrode since the area beyond it, which is actually responsible for the large capacitance increase, is much larger than that between *D* and *S*. At low frequencies, the conduction beyond this *D*/*S* electrode occurs in the lateral and vertical directions through the nc-Si:H bulk until reaching the accumulated electron channel. The bulk capacitance-resistance branches (dC_{Si}–dR_{Si}) have a distributed nature in that dR_{Si} increases gradually when moving away from the electrode as it is illustrated in Figure 7.9. So, beyond the effective region (ΔL) there is only lateral conduction through the channel and bulk effect can be omitted. As a result, the bulk branches (dC_{Si}–dR_{Si}) together with the channel resistances of the accumulated conducting electron layer (dR_{CH}) within the effective region near the electrode edges (ΔL) may be responsible for the $C_{G-DS}-F$ step at 28–37 pF. The further increase in C_{G-DS} from 37 pF to 57 pF occurring at lower frequencies might come from the contribution only of dR_{CH} resistances, that are located at the region more distant from the electrode, i.e. beyond ΔL. With decreasing frequency the whole dR_{CH}–chain acts as a capacitor plate with the area equal to that of nc-Si:H film (or TFT island) and thus C_{G-DS} saturates at 57 pF. It should be noted that as the gate voltage increases more electrons are accumulated and dR_{CH} decreases. Consequently, the same capacitance value is now obtained at higher frequencies [84]. This explains the shift of the two large $C_{G-DS}-F$ steps toward the higher frequencies with increasing V_{G-DS} (see Figure 7.3-c).

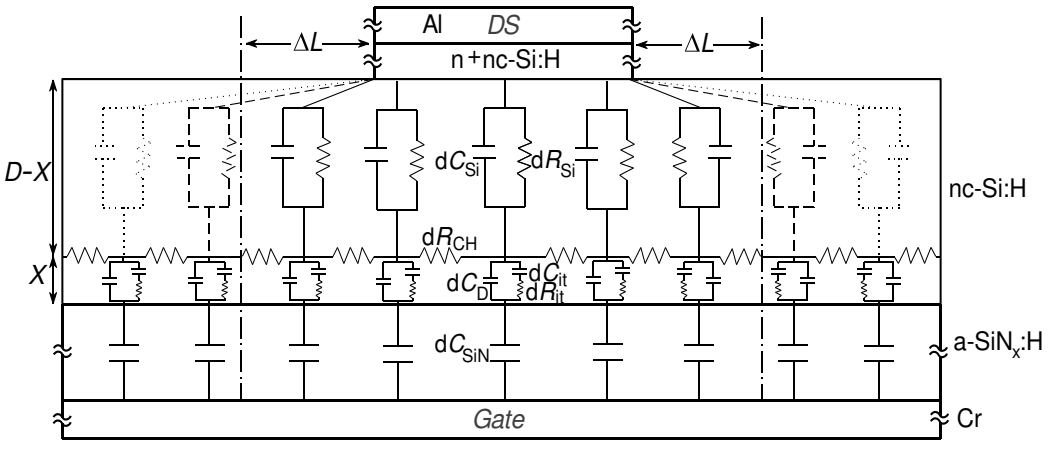


Figure 7.9: The equivalent network of the TFT structure. The gradual increase of the bulk resistances in the region beyond the *D*/*S* electrode is shown by the dashed lines of the corresponding branches.

7.4.2 Electrical properties of the MIAS and TFT

In contrast to the previous reports on the hole capacitance in a-Si:H TFTs [84, 85], the MIAS of this work does not require high reverse bias, high measurement temperature and light illumination to detect the hole accumulation. The use of LF at low negative bias seems to be enough for observing inversion (Figure 7.3-b). Here it should be noted that the bulk effect at HF, similar to the one at positive bias, is separated from the hole accumulation (Figure 7.5-b). The mechanism of the hole accumulation is assumed to be due to the generation-recombination of electron-hole pairs through the trap states in the depletion region [84]. Besides, the hopping conductivity is incorporated in this process, since from MIAS $C{-}F$ fitting R_I is found to be proportional to $\omega^{-0.75}$. This hopping process was also proposed by H.R. Park *et al.* [84] to explain the measured activation energy to be somewhat smaller than half of the mobility gap of a-Si:H.

The use of the Debye capacitance in the accumulation regime is required to fit $C_{G-S}{-}F$ curves of the MIAS (Figure 7.3-d). As it is found above, the Debye length in nc-Si:H is high, which can explain why the full accumulation is not achieved even at high V_{G-S} (Figure 7.3-b). Similarly to the inversion, accumulation process also occurs through the ac hopping conductivity as R_{Si} is found to be proportional to $\omega^{-0.68}$. The phases of different conductivity in any solid is the underlying reason for the ac hopping conductivity [88], so it is also expected for the amorphous rich nanocrystalline structure at hand to have F dependent conductivity. In "hopping" model, the carriers jump across the potential barriers of different heights, which brings up the time (or F) dependence. At high F the carrier transport is within the conducting nanocrystallites (low barrier heights), while at low F it is extended over longer distances and therefore decreases due to poorly conducting amorphous tissue (high barrier heights) [88].

Since the TFT performance is strongly dependent on the interface properties, the poor quality of the nc-Si:H film at the initial stage of its growth may be the reason for the resulted low TFT mobility. Indeed, the presence of the amorphous incubation layer in nc-Si:H film was confirmed by conductivity measurements (Figure 7.6). The possible columnar growth of nanocrystallites, resulting in anisotropic conductivity [42], may also impede the current flow parallel to the substrate and consequently decrease the TFT drain current resulting in low μ_{FE}. The off-current behavior of the TFT in Figure 7.2-b implies relatively low conductivity of the upper part of nc-Si:H bulk, although the lateral conductivity is found to be highly thickness dependent (Figure 7.6-a). This may be explained by the "percolation threshold"

of the nanocrystalline volume fraction, below which σ is low and above which there is an abrupt increase in σ [81]. In the present nc-Si:H film σ increased by more than two orders of magnitude for 470 nm film when compared with that for 140 nm one. Therefore, the thickness dependent σ is affected by the nanocrystalline volume fraction, which is below and above the "percolation threshold" (~30% [81]) for the thinner and thicker film, respectively. Subsequently, the heteroquantum-dots (HQD) model by G. Y. Hu *et al.* [89] can account for the difference in E_A for the thicker and thinner films. The high nanocrystalline volume fraction of the thicker film allows electrons to tunnel through the a-Si:H interface barriers after being activated from E_F to the interface energy level of the band offsets, thus resulting in E_A=0.33 eV (see Figure 7.6-b). The low nanocrystalline volume fraction of the thinner film does not allow the conduction through the HQDs and the convenient case of the electron activation from E_F to E_C (E_A=0.68 eV) as in a-Si:H film is valid.

The interface trap density can be correlated with the TFT subthreshold slope value, and both *SS* obtained from $I_{DS}-V_{GS}$ of the TFT and its corresponding D_{it} from $C_{G-S}-V_{G-S}$ measurements of this study are higher when compared with those found by M. T. Hsieh *et al.* [82]. Since the resulted energy distribution of D_{it} is far away from the band tails, the obtained U-like shape of the D_{it} (Figure 7.8-d) might be attributed to the region of the DOS inside the bandgap between two Gaussian distributions of dangling-bond states (neutral, D^0 and doubly occupied, D^-, see Figure 3.4) [95]. This is supported by the *FB* position, i.e. E_F, which is at the minimum of the D_{it}, so that possible D^0 peak is below and D^- is above the E_F.

7.5 Conclusion

The $C-V$ measurements on the nc-Si:H BG TFT and its MIAS structure show that the channel layer acts as the capacitor plate in the TFT structure with the area expanded over the whole nc-Si:H film. This expansion of the effective area can be associated with both bulk capacitance-resistance branches and channel resistances, where the former is dominant at higher frequencies and the latter is responsible for the further increase in the effective area at lower frequencies. It was also concluded that the hole conductivity along the TFT interface is less than the electron one.

The frequency dispersion of the MIAS capacitance due to the nc-Si:H neutral bulk is found in both accumulation and depletion regimes at high frequencies. The inversion regime is attained at room temperature for relatively low negative gate voltages within 10^2-10^{-2} Hz.

The ac hopping conductivity, found in all regimes, may be related to the phases with different conductivity in the nc-Si:H film. The formation of the amorphous rich incubation layer in nc-Si:H film, which might decrease the TFT mobility, is confirmed by the conductivity and activation energy measurements. The energy distribution of the interface trap density indicates the existence of two-Gaussian shaped DOS inside the bandgap of nc-Si:H.

CHAPTER 8

CONCLUSIONS

In recent years the PECVD grown hydrogenated nanocrystalline silicon thin film transistor (nc-Si:H TFT) has attracted attention due to its better electrical stability and higher mobility in contrast to the hydrogenated amorphous silicon (a-Si:H) TFT. The mobility values are much higher in the case of the top-gate (TG) TFT than that of the bottom-gate (BG) one. This is due to the formation of the incubation layer with low crystalline volume fraction at the initial stage of the nc-Si:H film growth. In this thesis the nc-Si:H BG TFT structure was fabricated and investigated for eventual improvement.

The 2-mask set was used in order to obtain drain/source (D/S) contacts and to separate non self-aligned TFTs from each other. It was deduced that the TFT isolation reduced the apparent leakage current and it should be done before $I-V$ characterization of TFT. Besides, the post-deposition annealing of TFT at 423 K under N_2 atmosphere for 30 min improved the device performance. The reactive ion etching (RIE) was used to etch n^+ nc-Si:H film between D/S contacts. The etching rate of R-22 gas was found to be lower by 5-6 times than that of R-12 gas.

One of the important issues in this study was the doping of nc-Si:H films which were used for improving the nc-Si:H TFT D/S ohmic contacts. The lateral resistivity (ρ) values of n^+ nc-Si:H films of thickness 100-150 nm were measured as ~1 Ωcm. But when the film thickness was reduced below the critical film thickness by RIE, ρ values were increased by several orders, related to the highly defective incubation layer impeding the doping process and/or crystallite columnar structure reducing the lateral current transport. The thickness of this incubation layer was reduced by the optimized power density (P_{RF}) around 160 mW/cm^2. ρ of 45 nm thick n^+ nc-Si:H film, deposited at this P_{RF}, attained ~92 Ωcm.

Ten different depositions of a-SiN_x:H films were performed in this thesis to optimize the

TFT gate dielectric film. The vertical $J-E$ characteristics of these a-SiN_x:H films were used as a testing tool for the insulating property. It was determined that the increasing PECVD chamber pressure or diluting NH_3+SiH_4 gas mixture with H_2 deteriorated the insulating properties. On the other hand, increasing NH_3 flow rate was found to decrease J and so it improved the dielectric. For NH_3/SiH_4 flow rate ratios of ~19 and ~28, the gate leakage current through the a-SiN_x:H films in TFT structure was estimated to be below 10^{-13} A and found to be even less when these two a-SiN_x:H films were applied to nc-Si:H BG TFTs. The TFT deposited with the NH_3/SiH_4~19 ratio showed lower threshold voltage and subthreshold slope, higher mobility than the TFT containing a-SiN_x:H with the NH_3/SiH_4~28 ratio. It was associated with the N−H/Si−H bond concentration ratio, which is responsible for the amount and sign of the local charges within the film bulk. So, not only the leakage current through a-SiN_x:H film but also its compositional structure affecting charge distribution can alter the TFT performance.

The crystallinity, large area uniformity and other properties of intrinsic nc-Si:H films were found to depend on P_{RF}. The structure of the films at the center of the PECVD electrode changed from amorphous dominant to nanocrystalline with P_{RF} increasing from 100 to 444 mW/cm^2. The nc-Si:H films grown at the edge of the electrode had nanocrystalline phase at all P_{RF}. The most uniform properties along the PECVD electrode were obtained at 300 mW/cm^2. The two BG TFTs were grown at the center of the electrode and were different only in P_{RF} used for the channel layer (100 and 300 mW/cm^2). The TFT with the channel layer having nanocrystalline structure (i.e. deposited at 300 mW/cm^2) showed lower V_T, higher μ_{FE}, similar SS and improved stability under gate-bias stress when compared with the TFT having amorphous dominant phase (i.e. deposited at 100 mW/cm^2). Therefore, it was concluded that the use of 3 times higher P_{RF} did not damage the a-SiN_x:H/nc-Si:H interface, but rather enhanced the TFT performance by forming more conductive nanocrystalline intrinsic channel layer.

The TFT island, fabricated from the optimized a-SiN_x:H (grown at NH_3/SiH_4~19) and nc-Si:H (grown at 300 mW/cm^2) films, was analyzed by the capacitance measurements. It was deduced from the frequency dependent $C-V$ measurements that the nc-Si:H bulk beyond D/S contacts was responsible for the effective area expansion of the capacitor plate. The model was proposed for the frequency dependence of this expansion. Subsequently, the parts beyond D/S Al contacts were etched by RIE and the $C-V$ measurements of the remaining MIAS structure were performed and investigated further. The usually obtained nc-Si:H bulk effect on the frequency dispersion in the accumulation regime was also detected in the de-

pletion. It was possible to attain the inversion within 10^2-10^{-2} Hz and without any external charge injection like light illumination, high reverse bias or high measurement temperature, which were applied in the earlier studies in literature. In addition, the ac hopping conductivity was found for all gate voltage regimes. The conductivity and activation energy measurements of nc-Si:H bulk at different thicknesses confirmed the validity of the incubation layer, which seriously reduced the TFT mobility. The a-SiN_x:H/nc-Si:H interface trap density was determined to be around 3×10^{10} $eV^{-1}cm^{-2}$.

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APPENDIX A

TFT SQUARE-LAW MODEL

A.1 Ideal Square-Law Model

Using gradual channel approximation (GCA), i.e. solving 1-D problem instead of 2-D one, electrical modeling of the ideal TFT structure shown in Figure 2.1 is started by the application

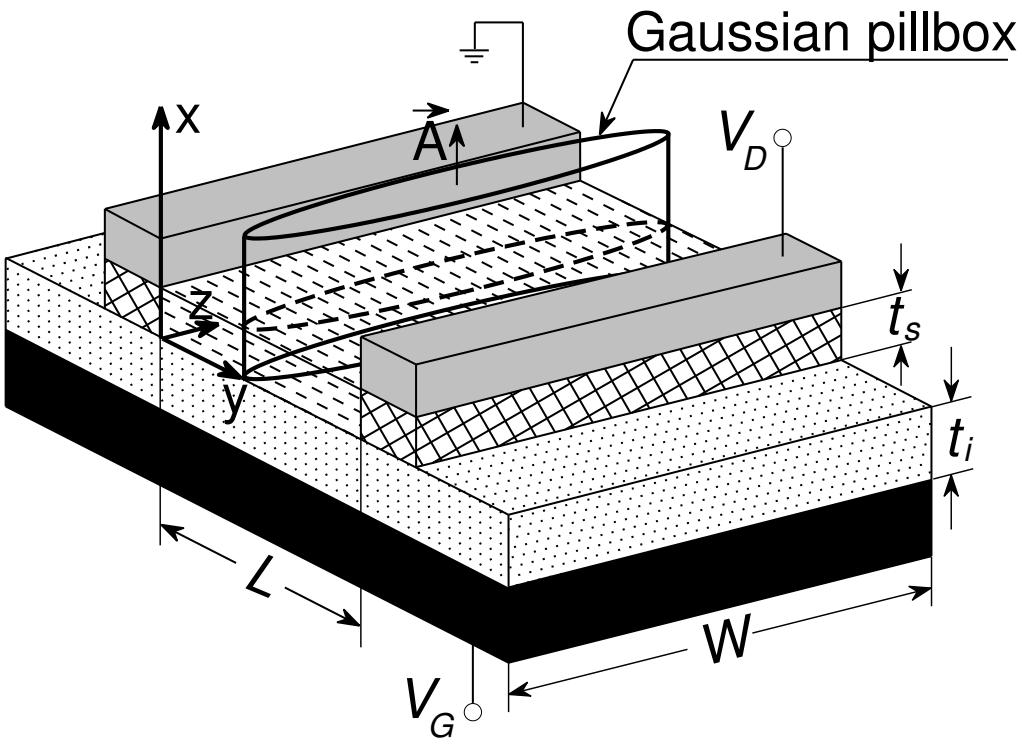

Figure A.1: Application of Gaussian pillbox with total surface S and cross-section area A at a distance y along the TFT channel.

of the integral form of Gauss's law (see Figure A.1):

$$\frac{-q\Delta n(y)At_s}{\epsilon_s} = \oint_S \overrightarrow{\xi_s}(x) \cdot \overrightarrow{dA}, \tag{A.1}$$

where $\Delta n(y)$ is the gate-induced carrier density at a distance y from the source, t_s is the semiconductor thickness, ϵ_s is the semiconductor dielectric constant, A is the cross-section area of the Gaussian pillbox with total surface S, $\xi_s(x)$ is the electric field inside the semiconductor. Here it is assumed that thickness of the semiconductor layer is sufficiently small to regard it as the thickness of the induced channel, i.e. $t_s \simeq h$ (see Figure 2.3). Since gate-induced electric field is perpendicular to the TFT channel, surface integral in the equation A.1 survives only for the top and bottom surfaces of the Gaussian pillbox. Taking into account that the semiconductor channel has low free carrier density and its physical thickness is about 50-250 nm, the boundary condition at the back interface of the channel usually used for MOSFETs ($\psi = 0$ and $d\psi/dx = 0$ at $x = t_s$, where ψ is the electrostatic potential) is not always applicable to the case of TFTs [96]. However, for high distribution of localized states in the energy gap the electric field at the back interface of the semiconductor layer can be ignored [97]:

$$\begin{aligned} \frac{-q\Delta n(y)At_s}{\epsilon_s} &= \xi_s(x = t_s)A - \xi_s(x = 0)A \\ \frac{q\Delta n(y)t_s}{\epsilon_s} &\simeq \xi_s(x = 0) \end{aligned} \tag{A.2}$$

This is also supported by the estimated thickness of the channel region, ~10 nm [20, 98]. Assuming absence of the surface (interface) states, σ_{ss}, at the semiconductor channel/insulator interface, displacement vector of the insulator at this boundary is equivalent to that of the semiconductor: $\epsilon_i\xi_i(x = 0) = \epsilon_s\xi_s(x = 0)$. Note that $\xi_i(x = 0) = [V_G - V(y)]/t_i$, where $V(y)$ is the drain voltage at a distance y from the source and t_i is the insulator thickness. Then, defining gate capacitance per unit area as $C_G = \epsilon_i/t_i$, the expression A.2 is given by:

$$q\Delta n(y) = \frac{C_G}{t_s}\left[V_G - V(y)\right] \tag{A.3}$$

The above discussion is about gate-induced charge inside the channel. But if the *depletion*-mode TFT is considered the initial carrier density of the semiconductor at zero gate bias, n_0, should be also added: $n_0 + \Delta n(y)$. Now, after establishing the total carrier density at a distance y in the channel, its transport under drain electric field, $\xi(y)$, can be expressed assuming only drift current presence and constant mobility, μ, along the channel:

$$J_D = \left[\sigma_0 + \Delta\sigma(y)\right]\xi(y), \tag{A.4}$$

where J_D is the drain current density, σ_0 is the channel conductivity at zero gate bias, $\Delta\sigma(y)$ is the gate-induced channel conductivity. Noting again that the channel is assumed to have the same dimensions as the semiconductor layer itself and remembering that $\sigma = q\mu n$, drain current, I_D, is given by:

$$I_D = t_s W q\mu \left[n_0 + \Delta n(y)\right] \xi(y). \tag{A.5}$$

Using equation A.3 and expressing electric field in terms of $V(y)$ results in:

$$I_D = W\mu C_G \left[\frac{qt_s n_0}{C_G} + V_G - V(y)\right] \frac{dV(y)}{dy}. \tag{A.6}$$

Multiplying both sides by dy and integrating over the length of the channel, L, leads to:

$$\begin{aligned} I_D \int_0^L dy &= W\mu C_G \int_0^{V_D} \left[\frac{qt_s n_0}{C_G} + V_G - V(y)\right] dV(y), \\ I_D &= \frac{W\mu C_G}{L} \left[(V_G - V_T)V_D - \frac{(V_D)^2}{2}\right], \end{aligned} \tag{A.7}$$

where V_T is the threshold voltage depending on the initial carrier density, n_0:

$$V_T = \frac{-qt_s n_0}{C_G}. \tag{A.8}$$

The equation A.7 is valid only for the linear region (pre-pinch-off regime), i.e. when $V_G \geq V_T$ and $V_D \leq V_G - V_T$. For $V_G < V_T$ TFT operation is in the cut-off regime with $I_D = 0$. At pinch-off condition ($V_{Dsat} = V_G - V_T$) and for $V_D > V_{Dsat}$ post-pinch-off regime works with the constant drain current:

$$I_{Dsat} = \frac{W\mu C_G}{2L}(V_G - V_T)^2. \tag{A.9}$$

A.2 Discrete Trap Model

It is known that localized state can be defined by its ionization energy, E_T, concentration, N_T, electron capture coefficient, c_n (or electron capture cross-section, $\sigma_n = \frac{c_n}{v_{th,n}}$, where v_{th} is the thermal velocity of free carriers) and hole capture coefficient, c_p (or hole capture cross-section, $\sigma_p = \frac{c_p}{v_{th,p}}$). Using Shockley-Hall-Read (SHR) statistics and assuming that the average free carriers velocity ($\overline{v_{th}}$) and cross-section are constant, the rate of change in the trap occupancy under various excitations is given as:

$$\frac{\partial n_T}{\partial t} = c_n n_c (N_T - n_T) - e_n n_T + e_p (N_T - n_T) - c_p p_v n_T, \tag{A.10}$$

where n_T is the density of filled traps, $(N_T - n_T)$ is the density of empty traps, n_c is the density of electrons in conduction band (CB), p_v is the density of holes in valence band (VB), e_n and e_p are the emission rates of electron and hole, respectively. In n-typed semiconductor, assuming that hole and electron cross-sections are equal, $n_c \gg p_v$ and $e_p \ll e_n$ leading to drop of two last right terms in equation A.10, i.e. there is trap interaction only with CB. Besides, since the SHR statistics is valid also at thermal equilibrium, where occupancy is expressed as $1/[\exp(E_T - E_F/k_BT) + 1]$ (with E_F-Fermi level and k_B-Boltzmann constant) and electron capture rate is equal to electron emission rate, e_n can be given through c_n:

$$e_n = c_n N_c e^{\left(-\frac{E_T}{k_B T}\right)}, \tag{A.11}$$

where N_c is the effective density of states in CB and $N_c e^{\left(-\frac{E_T}{k_B T}\right)}$ is usually defined as n_1-CB electron density when $E_F = E_T$ [15]. Therefore, the net rate of change in trap occupancy is:

$$\frac{\partial n_T}{\partial t} = \overline{v_{th}}\sigma_n n_c (N_T - n_T) - \overline{v_{th}}\sigma_n n_1 n_T. \tag{A.12}$$

When dynamical equilibrium (steady-state) is reached, $\frac{\partial n_T}{\partial t} = 0$, in other words rate of trap emission is equal to capture and density of filled traps can be found as:

$$n_T = \frac{n_c N_T}{n_c + n_1}. \tag{A.13}$$

Now the square-law model equations should be modified, because total charge induced by gate voltage in the TFT channel is distributed between CB $(n_c - n_{c0})$ and trap states $(n_T - n_{T0})$:

$$q\left[(n_c - n_{c0}) + (n_T - n_{T0})\right] = \frac{C_G}{t_s}\left[V_G - V(y)\right], \tag{A.14}$$

where n_{c0} and n_{T0} are the initial zero-bias densities of free CB and trapped electrons, respectively. Similarly to ideal square-law model, these initial carrier densities are responsible for threshold voltage, $V_T = -\frac{qt_s}{C_G}(n_{c0} + n_{T0})$:

$$q\left(n_c + n_T\right) = \frac{C_G}{t_s}\left[V_G - V(y) - V_T\right]. \tag{A.15}$$

Defining voltages as $V_c(y) \equiv \frac{qn_c(y)t_s}{C_G}$, $V_{N_T} \equiv \frac{qN_T t_s}{C_G}$, $V_1 \equiv \frac{qn_1 t_s}{C_G}$ and substituting Eq. A.13 into Eq. A.15 results in quadratic equation with the following solution:

$$V_c(y) = \frac{1}{2}\left[a - V(y)\right] + \frac{1}{2}\left[a - V(y)\right]^2 + c\left[b - V(y)\right]^{1/2}, \tag{A.16}$$

where $a = V_G - V_{N_T} - V_T - V_1$, $b = V_G - V_T$ and $c = 4V_1$. Since only CB electrons $(n_c(y))$ contribute to drift current, equation A.5 is modified as:

$$I_D = t_s W q \mu n_c(y)\frac{dV(y)}{dy} = \frac{W}{L}\mu C_G \int_0^{V_D} V_c(y) dV(y). \tag{A.17}$$

Substituting Eq. A.16 for $V_c(y)$ and performing integration leads to the drain current for pre-pinch-off regime:

$$I_D = \frac{W}{L}\mu C_G\left[\frac{1}{2}aV_D - \frac{1}{4}V_D^2 + \frac{1}{4}\left(V_D - a - \frac{c}{2}\right)C_1 \right.$$
$$\left. + ln\left(\frac{C_2}{C_3}\right)(V_{N_T}V_1) + \frac{1}{4}\left(a^2 + bc\right)^{1/2}\left(a + \frac{c}{2}\right)\right], \tag{A.18}$$

where $C_1 = [(a - V_D)^2 + c(b - V_D)]^{1/2}$, $C_2 = (-2a - c + 2V_D + 2C_1)$ and $C_3 = [-2a - c + 2(a^2 + bc)^{1/2}]$. For post-pinch-off regime V_D in the above equation is simply replaced by $V_{Dsat} = V_G - V_T$.

APPENDIX B

SUBSTRATE CLEANING

Standard substrate cleaning procedure was used before thin film deposition process to guarantee the high yield and reliability in the TFT production. If not cleaned properly the grown film may peel off from the substrate when exposed to the atmosphere or rinsed in the water solutions. This becomes especially vital for the TFT production, in which photolithographic steps involve water diluted developer and other solutions for wet etching. The cleaning in this study involved organic and ionic cleaning for the glass and quartz substrates, and RCA steps for the silicon substrates.

B.1 Glass and Quartz

The main steps followed in the glass and quartz cleaning are:

1. Boiling in detergent for 5 minutes.
2. Boiling in trichloroethylene (C_2HCl_3) for 3 minutes.
3. Boiling in H_2O_2:H_2O (1:1) solution for 3 minutes.
4. Drying with N_2 gun.

After each step, except the last one, the substrates were rinsed in deionized water (DIW) and then in ultrasonically agitated DIW bath for 3 minutes.

B.2 Silicon Wafer

The main steps followed in the silicon wafer cleaning are:

1. Boiling in H_2O : H_2SO_4 : H_2O_2 (6:1:1) mixture for 5 minutes.
2. Boiling in H_2O : HCl : H_2O_2 (6:1:1) mixture for 10 minutes.
3. Dipping in H_2O : HF (30:1) mixture for 30 seconds.

4. Drying with N_2 gun.

After the first and second steps, silicon wafers were rinsed in DIW and then in ultrasonically agitated DIW bath for 3 minutes. After the third step, wafers were rinsed in running DIW for a few seconds to check whether the silicon surface repels water.

After drying with N_2 gun was over, all the substrates were placed in the film deposition chamber immediately. The Cr coated glasses for the TFT fabrication and a-SiN_x:H test sample production were placed into the PECVD system after being treated by isopropyl alcohol, rinsed in DIW and dried by N_2 gun. Before starting the film deposition process in the PECVD system, the substrates were cleaned (etched) under H_2 plasma for 5 minutes.

APPENDIX C

THIN FILM DEPOSITION AND ETCHING SYSTEMS

C.1 Electron-Beam Deposition System

For the physical vapor deposition of the TFT gate metal (Cr) on the glass substrates, the electron-beam evaporation division of Univex450 system, shown in Figure C.1 , was utilized. The cleaned glass substrates were loaded on the sample holder and thickness monitor crys-

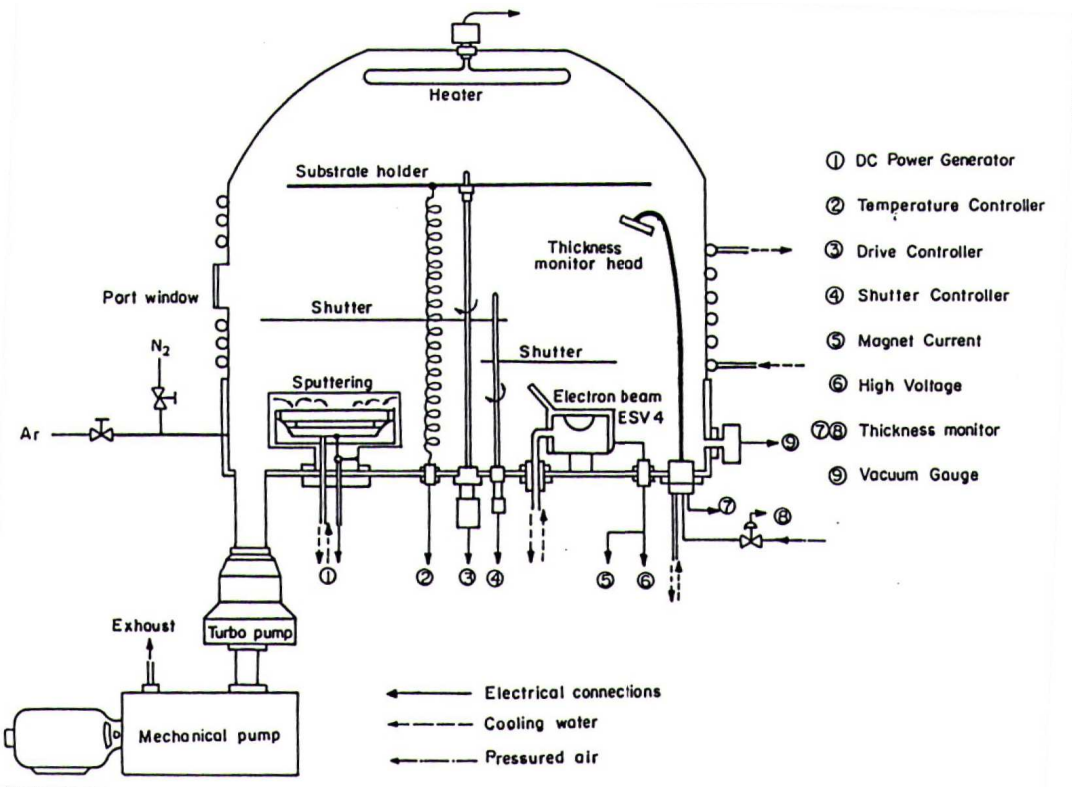

Figure C.1: Sputtering and electron-beam deposition system [99]. The electron-beam division was used for TFT gate metal (Cr) coating.

tal head was adjusted close to the substrate positions to measure the film thickness by the resonant frequency of the piezoelectric crystal. Two pumps, mechanical and turbo molecular, were started together and when the vacuum level reached 0.1 Torr (within two minutes) the mechanical pump was closed. The base pressure of the chamber was then decreased to $\sim 3\times10^{-6}$ Torr in 3-4 hours. A stream of electrons was accelerated up to ~9 kV and directed to the Cr target in the crucible. Thus the highly energetic electrons transform their kinetic energies to the thermal one, which melts and evaporates Cr. Since the outer surface of Cr target particles is oxidized or contaminated the evaporation was done for a few minutes with the shutter closed. This also provided the further decrease in the chamber pressure due to reaction of evaporated Cr with the small amount of the oxygen left in the chamber. Then the shutter was opened and deposition began until the desired thickness, controlled by the programmable XTC thickness monitor. Cr thickness was confirmed by the profilometer measurements and deposition rate was found as ~17 nm/min.

C.2 Plasma Enhanced Chemical Vapor Deposition System

The PECVD master unit of the Plasma Lab μP 80 system used in this work for the film depositions (see Figure C.2) has a source of RF (13.56 MHz) power for the discharge, a gas inlet arrangement, a deposition single-chamber that holds the pair of electrodes and a substrate heating assembly, a pumping system [99]. It is a capacitively coupled reactor, in which the bottom electrode is grounded, while the RF power is applied to the top electrode. Bottom electrode has radius of 12 cm, resulting in ~450 cm^2 electrode area and it was heated to 473-523 K in this study. The cleaned substrates were placed on the bottom electrode, afterwards the chamber was pumped down to 3 mTorr by the roots blower type pump backed with the rotary vane pump and heated. Then the gas mixture was introduced through the top showerhead in the top electrode by adjusting the desired flow rates and deposition pressure. The RF power was applied for the particular deposition time. The combustion furnace (between chamber and pump system) was heated up to 1073 K before the deposition process in order to decompose poisonous and flammable silane gas. In addition the continuous purging of the exhaust line with N_2 during the deposition process was assured.

For the dry etching processes the etching unit (slave unit) of the Plasma Lab μP 80 system was utilized [99]. It has a bottom electrode of ~222 cm^2 area, on which the samples to be etched were placed and RF power was applied. The etching system was pumped down to

3 mTorr by turbo molecular pump backed with the rotary vane pump and the etchant gas was introduced through the top electrode. The chamber pressure was set to 0.1 Torr and RF power of 100 W was applied for the desired period of time determined from the etching rate

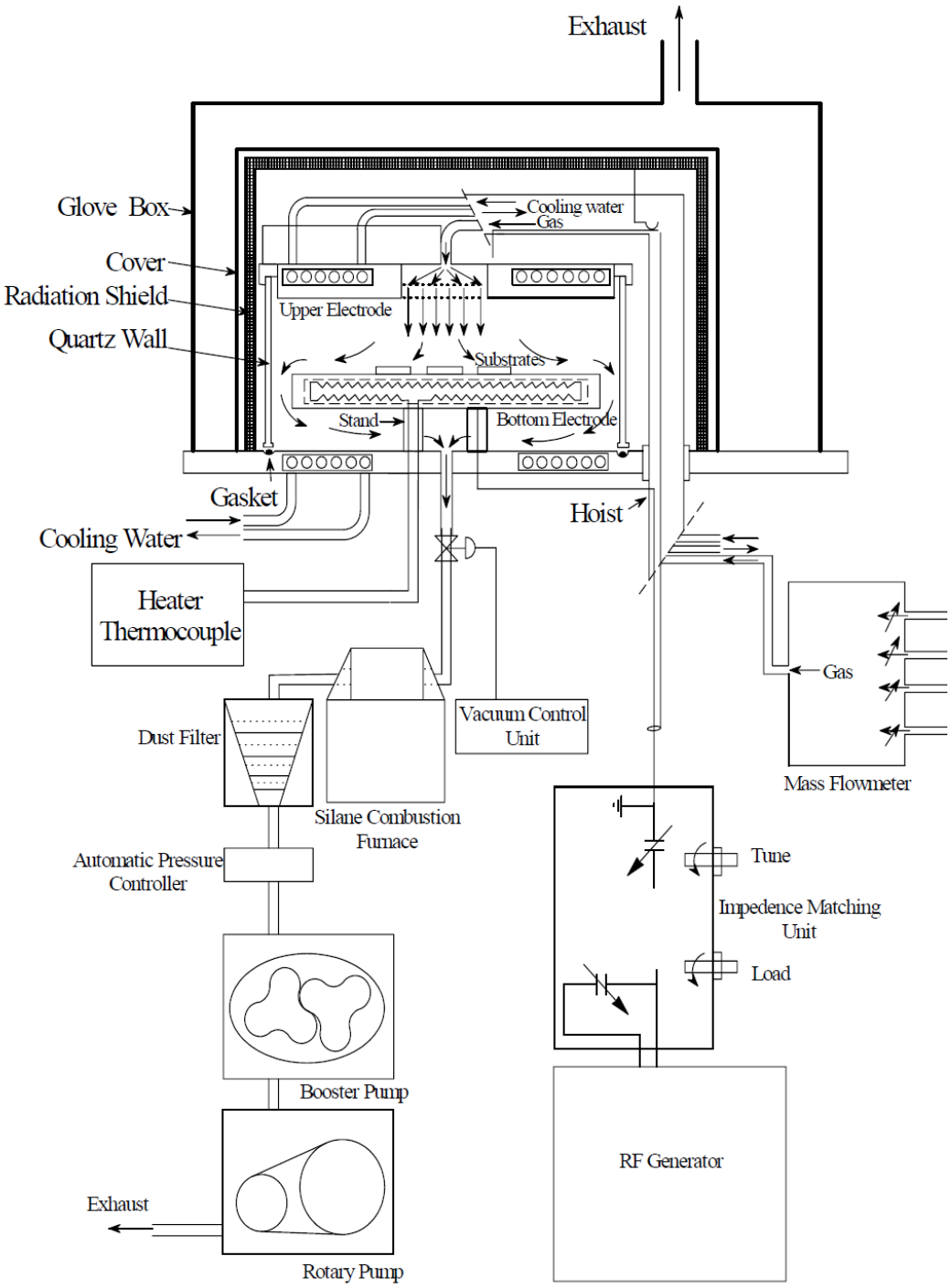

Figure C.2: Plasma enhanced chemical vapor deposition system [99] used in the deposition of TFT thin films (a-SiN$_x$:H, nc-Si:H and doped nc-Si:H).

(found by the preliminary work, see section 5.3.2). Thus the reactive ion etching (RIE) was achieved, where positively charged energetic ions approach the film surface, react with it and by transforming their kinetic energy sputter the film material.

C.3 Resistive Evaporation System

To deposit the TFT drain/source metal contacts and dot/planar shaped electrodes on the test samples, the tungsten (W) filament with Al bar was heated and evaporated in the high vacuum system shown in Figure C.3. Immediately after taken out from the PECVD master unit, the TFT and test samples were loaded on the sample holder with the proper masks (Figure 4.2) on it or without masks for the TFT case (step 3 in Figure 4.4). The sample holder was designed and fabricated from duralumin. It contains window places for the TFT samples and test samples designated for the planar electrodes, while smaller window places were used for the test samples with dot shaped electrodes (see Figure C.4). The Al bar was cleaned by

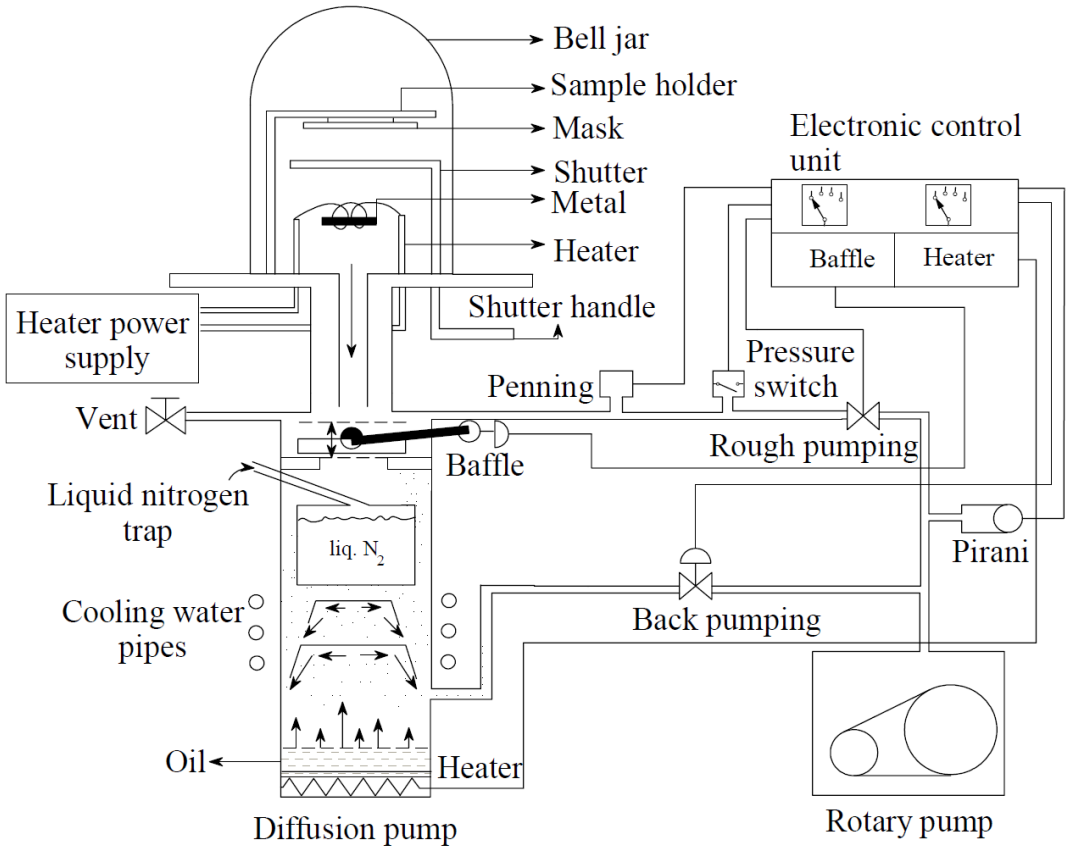

Figure C.3: Resistive evaporation system [100] used for TFT drain/source metal (Al) coating.

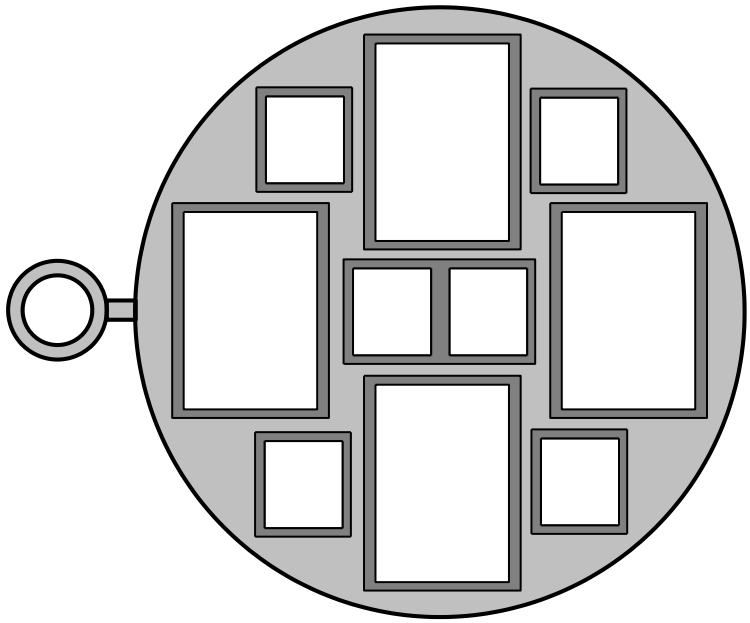

Figure C.4: The top view of the sample holder fabricated for the Al coating of TFT and test samples in the resistive evaporation system.

isopropyl alcohol, rinsed in DIW, dried by N_2 gun and placed on the filament. The glass bell jar was pumped down to $< 2\times10^{-6}$ Torr by diffusion pump cooled with the periodically added liquid N_2 to prevent backstreaming of the vaporized oil [99]. Then, to evaporate the Al bar, W filament was heated up by the electric current controlled by a Variac. When the evaporation started the shutter was kept closed for a few seconds to avoid approach of any Al bar surface contaminants on the samples. Afterwards the shutter was opened and evaporation was continued until the bell jar became opaque due to the Al coating.

All the systems described above were cleaned before the film deposition, and cooled by the running water during the deposition/etching processes. After the deposition process was over, each of the deposition systems was left to cool down under vacuum.

APPENDIX D

PHOTOLITHOGRAPHIC METHOD

The photolithographic method was used for the TFT fabrication in the lithography room, also known as yellow room due to its yellow filters and lights. In this work, the positive photoresist (PR), 1350 Shipley CO, was used to perform patterning. It is a light sensitive material in liquid form, which leaves behind an image that matches the image of the mask, i.e. parts of the PR being exposed to UV-light source are soluble during developing (dipping into the suitable solution-developer). The Al coated TFT trilayered structures were coated by this PR using the spin coating technique. The samples were loaded on the vacuumed holder to retain them during the rotation, then the PR was dropped on the Al surface through the nozzle and the spinner (model EC101 of Headway Research CO) was rotated with the speed of 3000 rpm for 40 s (see Figure D.1). The spinner application resulted in a uniform PR coating of ~1 μm over the desired side of the sample. It was then hardened (evaporation of solvent) by baking at 343 K for 30 min in the temperature controlled heating system, shown in Figure D.2.

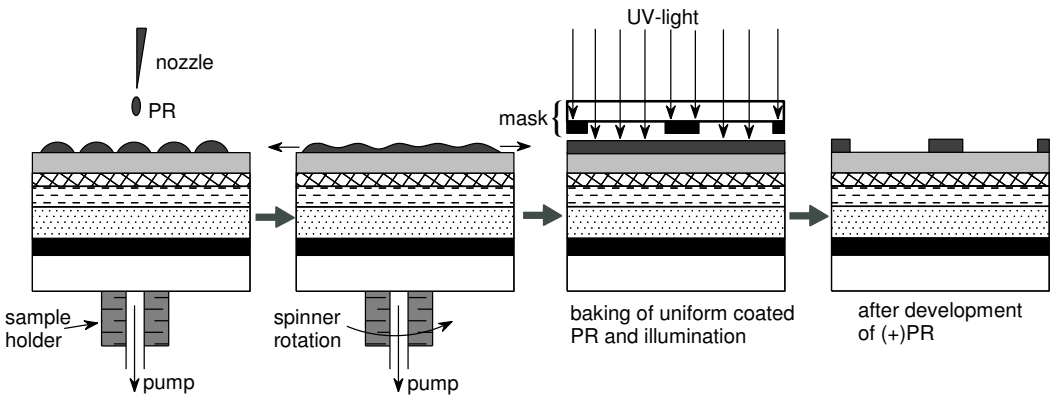

Figure D.1: PR coating, baking and illumination processes utilized in this work for the TFT fabrication.

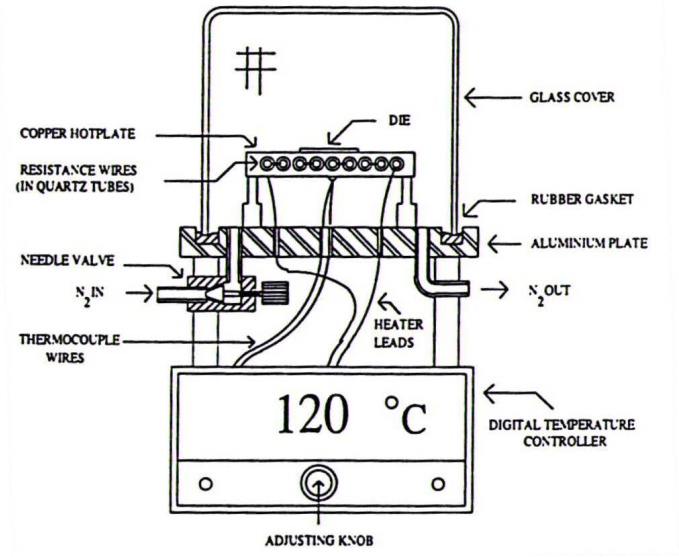

Figure D.2: The heating system used for PR baking and post-deposition annealing of TFT. N_2 gas was introduced continuously during the latter process.

Afterwards the UV-light exposure of PR through the first TFT mask (steps 4-5 in Figure 4.4) was performed in the mask aligner system (model 17A-A2 of Kasper Instruments), diagram of which is provided in Figure D.3. The mask was aligned to the Al part of the sample, then sample was pressed on the mask (contact mode) and 200 W UV-light of mercury-arc lamp was exposed for 12-13 s. Then PR was immediately developed in the prepared NaOH solution (7 g of NaOH stirred in 1 liter of DIW) for ~40 s (checked on the control samples) and the TFT

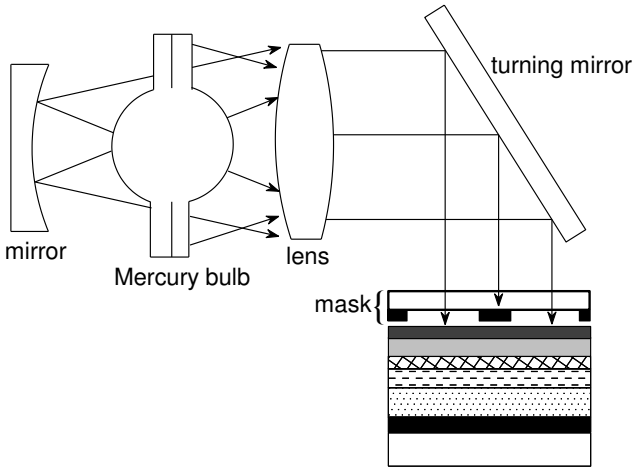

Figure D.3: Optical diagram of the mask aligner used in this work.

sample was quickly washed under running DIW to prevent the further attack of the remained developer solution. After that, following the steps in Figure 4.4 drain/source metal (Al) was etched by wet etching process: the sample was dipped into H_3PO_4 solution with a few drops of HNO_3 for a few minutes until nc-Si:H film appeared on the patterned parts instead of shiny Al. The sample was immediately washed under running DIW, then remaining PR was removed by acetone solution, again the sample was rinsed in running DIW, dried with N_2 gun and then checked through the microscope. Thus, Al acted as a mask for plasma etching of n^+ nc-Si:H layer until the back of the channel layer (see 7-8 steps in Figure 4.4). To pattern the TFT islands, i.e. conduct TFT isolation, second TFT mask was utilized. Firstly PR was coated once more, baked and then sample was accurately aligned to this second mask through the microscope of the mask aligner. After PR development, reactive ion etching (RIE) of nc-Si:H and a-SiN_x:H thin films was performed until Cr gate metal is reached. Finally, the PR was removed by acetone, sample was washed in running DIW and dried with N_2 gun. Before the TFT characterization, the sample was annealed (post-deposition annealing) in the heater system (Figure D.2) at 423 K under N_2 atmosphere for 30 min.

VITA

Tamila Aliyeva was born in Magdeburg, Germany, on April 20, 1984. In 2001 she graduated from Baku European Lyceum, Azerbaijan. In 2001-2002 she received Turkish language education in TÖMER of Gazi University, Ankara, Turkey. During 2002-2006 she conducted her B.S./M.S. degree studies (5-year integrated program) at Middle East Technical University (METU), Ankara, Turkey, and received non-thesis M.S. degree in Physics Education in 2006. Since 2006 she has been undertaking her Ph.D. studies in Experimental Solid State Physics at METU. Her areas of research interest mainly include: production and optoelectronic characterization of amorphous/nanocrystalline thin films, thin film transistors and *pin* diodes.

Her publications are listed below:

related to this thesis

1. T. Aliyeva Anutgan, M. Anutgan, I. Atilgan, B. Katircioglu, *Capacitance analyses of hydrogenated nanocrystalline silicon based TFT*. (2010) Submitted to Thin Solid Films.

2. T. Aliyeva Anutgan, M. Anutgan, I. Atilgan, B. Katircioglu, *Large area uniformity of plasma grown hydrogenated nanocrystalline silicon and its application in TFTs*. J. Non-Cryst. Solids 356 (2010) pp. 1102-1108.

3. T. Aliyeva Anutgan, M. Anutgan, I. Atilgan, B. Katircioglu, *Optimization of n^+ nc-Si:H and a-SiN_x:H layers for their application in nc-Si:H TFT*. (2010) Submitted to Solid-State Electronics.

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4. T. Aliyeva Anutgan, M. Anutgan, I. Atilgan, B. Katircioglu, *Stability and degradation of plasma deposited boron nitride thin films in ambient atmosphere*. Thin Solid Films 518 (1) (2009) pp. 419-425.

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