DESIGN AND IMPLEMENTATION OF A CURRENT SOURCE CONVERTER BASED ACTIVE POWER FILTER FOR MEDIUM VOLTAGE APPLICATIONS

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ABSTRACT

DESIGN AND IMPLEMENTATION OF A CURRENT SOURCE CONVERTER BASED ACTIVE POWER FILTER FOR MEDIUM VOLTAGE APPLICATIONS

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This research work is devoted to the design, development and implementation of a Current Source Converter (CSC) based Active Power Filter (APF) for Medium Voltage (MV) applications. A new approach has been proposed to the design of the CSC based APF for reducing the converter kVA rating considerably. This design approach is called the Selective Harmonic Amplification Method (SHAM), and is based on the amplification of some selected harmonic current components of the CSC by the input filter, and the CSC control system, which is specifically designed for this purpose.

The proposed SHAM has been implemented on the first industrial CSC based APF for the elimination of 11^{th} and 13^{th} current harmonics of 12-pulse rectifiers fed from Medium Voltage (MV) underground cables in order to comply with IEEE Std. 519-1992. 450 kVA rated APF with only 205 kVA CSC rating has been connected to the MV bus via a coupling transformer of 1600kVA, 34.5/1.1 kV. The power stage of the CSC based APF is composed of water-cooled high voltage IGBT and diode modules.

Reference currents to be generated by the CSC are obtained by the use of a selective harmonic extraction method, by employing synchronously rotating reference frames for each selected

harmonic component. An Active damping method is also used to suppress the oscillations around the natural frequency of the input filter, excluding the harmonic components to be eliminated by APF.

Simulation and field test results have shown that SHAM can successfully be applied to a CSC based APF for reduction of converter kVA rating, thus making it a cost-competitive alternative to voltage source converter based APFs traditionally used in industry applications.

Keywords: Active filters, pulse width modulated power converters, harmonic distortion, power quality, current source converter

ÖZ

ORTA GERİLİM UYGULAMALAR İÇİN AKIM KAYNAKLI ÇEVİRGECE DAYALI AKTİF GÜÇ FİLTRESİ TASARIMI VE UYGULAMASI

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Bu çalışma, Orta Gerilim (OG) uygulamaları için Akım Kaynaklı Çevirgece (AKÇ) dayalı Aktif Güç Filtresi (AGF) sisteminin tasarımına, geliştirilmesine ve tesis edilmesine hasredilmektedir. AKÇ dayalı AGF sisteminin tasarımında, çevirgeç anma gücünü dikkate değer biçimde azaltacak yeni bir yaklaşım sunulmaktadır. Bu yaklaşım Seçili Harmonik Yükseltme Metodu (SHYM) olarak anılmakta, ve çevirgecin ürettiği bazı seçilmiş harmonik bileşenlerin giriş filtresi ve bu işe özel tasarlanmış kontrol sistemi tarafından yükseltilmesine dayanmaktadır.

Öne sürülen SHYM, OG yer altı kablolarından beslenen 12-darbeli doğrultucuların 11. ve 13. akım harmoniklerinin IEEE Std. 519-1992 standardına uyum sağlayabilmek amacıyla yok edilmesi için ilk endüstriyel AKÇ dayalı AGF sistemine uygulanmıştır. 450 kVA gücündeki AGF sisteminin 205 kVA gücünde AKÇ anma gücü olup, OG baraya 1600 kVA, 34.5/1.1 kV bir kuplaj transformatörü üzerinden bağlanmaktadır. AGF sisteminin güç katı su soğutmalı yüksek gerilim IGBT ve diyot modüllerinden oluşmaktadır.

AKÇ tarafından oluşturulan referans akımlar, önceden seçilmiş her bir harmonik bileşen için senkron dönen referans düzlemler kullanan bir seçili harmonik ayrıştırma metodu kullanılarak

elde edilmektedir. Giriş filtresinin akord frekansı etrafında ve AGF sisteminin yok edeceği harmonik bileşenler haricindeki salınımları bastırmak amacıyla da bir aktif sönümlendirme metodu kullanılmıştır.

Benzetim ve saha test sonuçları göstermiştir ki SHYM, çevirgecin kVA değerinin düşürülmesi için AKÇ dayalı AGF sistemine başarılı bir biçimde uygulanabilmekte, böylece onu endüstriyel uygulamalarda geleneksel olarak kullanılan gerilim kaynaklı çevirgece dayalı AGF sistemlerine karşı fiyat açısından rekabetçi bir alternatif yapmaktadır.

Anahtar Kelimeler: Aktif filtreler, darbe genişliği kiplenimli çevirgeçler, harmonik bozulum, güç kalitesi, akım kaynaklı çevirgeç

To my family

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The prototype system, developed within the scope of this research work, is a part of the National Power Quality Project (Project No: 105G129). I would like to express my special thanks to TÜBİTAK Public Researchs Group (KAMAG), and Bursa Public Transportation Company (BURULAŞ) for their full financial support.

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NOMENCLATURE

ABBREVIATIONS

AC	Alternating Current
APF	Active Power Filter
CSC	Current Source Converter
DC	Direct Current
DSPWM	Dead-band Sinusoidal Pulse Width Modulation
HPF	High Pass Filter
LPF	Low Pass Filter
MDSPWM	Modified Dead-band Sinusoidal Pulse Width Modulation
MV	Medium Voltage
PLL	Phase Locked Loop
SHAM	Selective Harmonic Amplification Method
SPWM	Sinusoidal Pulse Width Modulation
STATCOM	Synchronous Static Compensator
SVPWM	Space Vector Pulse Width Modulation
TDD	Total Demand Distortion
THD	Total Harmonic Distortion
VA	Volt-Ampere
VAr	Volt-Ampere-reactive
VSC	Voltage Source Converter

SYMBOLS

ω_h	Angular frequency of h^{th} harmonic component
C_{dc}	Dc-link capacitor
C_f	Capacitance of input filter capacitor
f_s	Supply frequency
f_0	Natural frequency of input filter
f_{cr}	Carrier frequency
f_{sw}	Effective switching frequency
G_d	Damping gain
i_d	Damping current
I_{csc}	True rms value of CSC current
i_{csc}	Line current of CSC
I_{dc}	Dc-link current value
I_f	True rms value of APF current
i_f	Line current of APF
I_L	Maximum load current
I_{SC}	Short circuit current of the bus at PCC
K_{11}	Amplification factor of input filter for 11^{th} harmonic component
K_{13}	Amplification factor of input filter for 13^{th} harmonic component
L_{dc}	Inductance value of dc-link reactor
L_f	Inductance of input filter reactor
Q_0	Quality factor of input filter
R_d	Virtual damping resistor
v_c	Line-to-neutral voltage of filter capacitor
v_l	Line-to-neutral voltage of filter reactor

CHAPTER 1

INTRODUCTION

1.1 General

In recent years, utilization of electrical energy has changed with the improvements in power electronic systems and their widespread usage in all kinds of equipment. Conventional type loads have been replaced by those having sophisticated power electronics systems. As an example, AC motors being widely used in all types of industrial processes have been equipped with AC motor drives for ease of control, and energy saving. Adjustable Speed Drives (ASDs), Uninterruptible Power Supplies (UPSs), computers and their peripherals, consumer electronics appliances, etc. are the most common applications incorporating power electronic systems [1]. Although these systems provide many conveniences to improve the efficiency in electrical energy utilization, they also yield inevitable problems like degradation of power quality in both distribution and transmission systems.

The main power quality problem arising from the power electronics systems is the non sinusoidal currents injected to the network as a nature of their non-linear load characteristics. These non-sinusoidal currents, or harmonics, distort the voltage waveform of the supply, and affect all other loads connected to the same bus. Many undesirable effects of the harmonic currents/voltages on the distribution and transmission systems have been reported [3, 4]. Among them, the increase in rms currents and losses, excessive heating of transformers and motors, malfunctioning of relays and circuit breakers, and failure of capacitors due to resonance problems are the most well-known effects of the harmonics.

In order to minimize the harmonic related problems, and to improve the quality of the electrical energy supplied, various national and international agencies have published standards,

recommendations and regulations that specify limits on the magnitudes of harmonic currents and voltages. Standards IEC 61000-3-2 [5], and IEC 61000-3-4 [6] specify the limits of harmonic current components of the equipments, which are being connected to the Low Voltage (LV) distribution systems, and having input current ratings up to 16 A (included), and exceeding 16 A, respectively. In contrast to this *equipment based* approach, IEEE has released the guide, IEEE Std.519-1992 [7] which contains recommended practices and requirements for harmonic control in electric power systems specified both for customers and utilities.

In IEEE Std.519-1992, individual and total distortion indices have been introduced both for current and voltage harmonics. As a common representation, Total Harmonic Distortion (THD), as given in 1.1, is used to define the total distortion level of a waveform including harmonic components. Since, THD is defined with respect to the fundamental components of the voltage and current waveforms; it may be nonsense under some circumstances for evaluating the distortion level of current waveforms. As an example, during the energization instants of transformers, high amounts of second, third and fourth harmonic current components, as well as DC, can be seen. Hence, THD value can be measured very high (> 25.0 %), exceeding the limit values. However, these harmonic components are very small compared to the rated fundamental current of the transformer, and have very limited effect on the network.

$$\begin{aligned} THD_i &= \frac{\sqrt{\sum_n I_n^2}}{I_1} x100 \\ THD_v &= \frac{\sqrt{\sum_n V_n^2}}{V_1} x100 \end{aligned} \tag{1.1}$$

where $n = 2, 3, ...$

Another approach is proposed in IEEE Std.519-1992 to evaluate the distortion level of current harmonics. In this approach, limit values are defined with respect to both rated or maximum current of the load/system under evaluation, and the short-circuit MVA of the bus, to which the load/system is connected. Table 1.1 shows the individual and total current harmonic distortion limits both for customers, and utilities.

In Table 1.1, I_{SC} denotes the short-circuit current of the bus at the Point of Common Coupling (PCC), and I_L is the maximum rms value of the fundamental current component, which is calculated by using the 15-30 min. averaged data for the whole measurement interval, which is

Table 1.1: Current Distortion Limits for Distribution and Transmission Systems (up to 36 kV*) according to IEEE Std.519-1992

Maximum Harmonic Current Distortion in Percent of I_L						
Individual Harmonic Order (Odd Harmonics)						
I_{SC}/I_L	<11	11≤h<17	17≤h<23	23≤h<35	35≤h	TDD
20<	4	2	1.5	0.6	0.3	5
20<50	7	3.5	2.5	1	0.5	8
50<100	10	4.5	4	1.5	0.7	12
100<1000	12	5.5	5	2	1	15
>1000	15	7	6	2.5	1.4	20

Even harmonics are limited to 25% of the odd harmonic limits above.
* Above 36 kV, for transmission system, limit values are half of the values given in this table.

where
I_{SC} = maximum short-circuit current at PCC.
I_L = maximum demand load current (fundamental frequency component) at PCC.

defined as at least one week continuously in IEC 61000-4-30 [8]. If there is no sufficient information, or the system is not existing, I_L can be taken as the rated current of the load/system under consideration, for design purposes. As an alternative to THD, Total Demand Distortion (TDD) is defined with respect to I_L as given in (1.2) to evaluate the current harmonic distortion.

$$TDD = \frac{\sqrt{\sum_n I_n^2}}{I_L} x100\cdot \tag{1.2}$$

Until January 2003, neither distribution companies nor customers have had restrictions on voltage and current harmonics in Turkey. However, Electricity Market Regulatory Authority (EMRA) has published the harmonic limits firstly for distribution companies, and customers connected to the transmission system directly; and then published the corresponding limits for all customers connected to the distribution system. Therefore, as of September 2006, all the customers and distribution companies shall comply with the current and voltage distortion limits specified in these regulations [9]-[11]. Limit values on the current harmonics specified in the regulations are almost identical to those in IEEE Std.519-1992, and the limit values on voltage harmonics are almost the same with those in EN 50160 [12].

Besides, EMRA has published the new and very tight regulations [10, 13] on reactive energy consumptions as of January, 1st 2008. According to these regulations, all customers and distribution companies should have average power factors on monthly basis as 0.98, and 0.99 for inductive and capacitive regions, respectively.

1.2 Solutions for Harmonic Filtering

A traditional solution for filtering of harmonics generated by non-linear loads is using either series or shunt connected passive harmonic filters. Vast majority of the passive filters applied to industrial systems are shunt harmonic filters. Series connected passive filters are usually used to bring the harmonics to a certain level, at which the size and the cost of the passive filter are kept at an optimum point. On the other hand, shunt passive filters provide a low impedance path to the currents at one or more harmonic frequencies, and they have different topologies such as single tuned filters, de-tuned filters, high pass filters, and higher order filters, depending the type of application as shown in Figure 1.1. In general, a number of second order single tuned filters connected in parallel and/or high pass damped filters are sufficient to filter out the harmonics of many loads in industry. At first sight, passive filters seem to be attractive owing to their ease of application, and costs. However, they have many significant drawbacks [4, 14]. First of all, the filtering performance of the passive filters completely depends on the network parameters. Since the idea is simply the Kirchoff's current law, as the impedance of the network increases, the filtering performance of the passive filters also increases. Hence, filtering performance degrades significantly for stiff (with high short circuit MVA) networks. Besides, passive filters result in resonance circuits with the source and/or load impedances. This may yield to high amounts of harmonic currents and dangerous overvoltages in the resonant circuit.

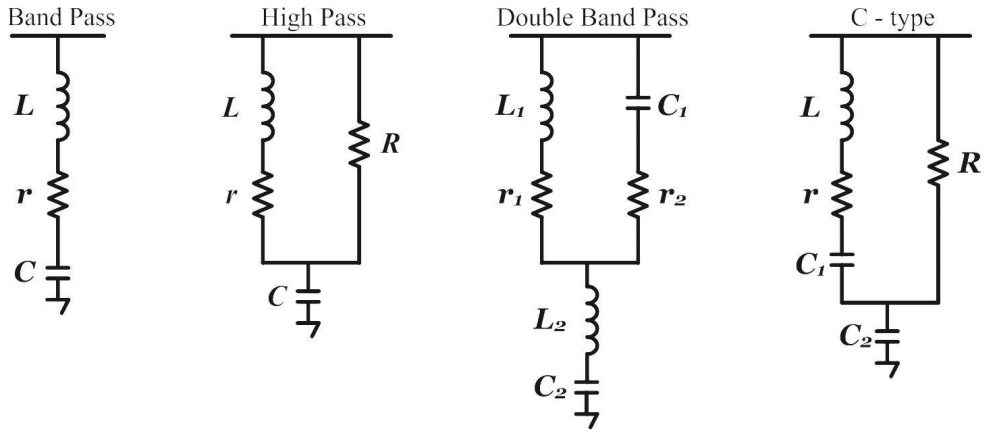


Figure 1.1: Various passive filter topologies

Since most of the customers in Turkey pay their attention to the power factor correction due to very tight regulations on reactive energy, and monetary penalties, harmonic filtering issue is usually under emphasized. In addition to this, the incorrect usage of shunt plain capacitors also increases the level of harmonic current/voltage components. Thereby, distribution companies take measures against harmonics to comply with limit values specified in the associated standards. However, in LV distribution systems, it is not easy to measure the harmonic emissions of thousands of customers, and forcing them to decrease their harmonic emissions. For that reason, distribution companies are trying to force medium and high power customers for taking counter-measures against harmonics, as well as making investment at the interface of distribution and transmission systems.

The increased severity of harmonic related problems has attracted the attention to develop dynamic and adjustable solutions to the power quality problems. With the development of power semiconductor devices, modern solutions such as Active Power Filters (APF) have become a valuable alternative to solve the power quality problems of both customers and utilities. Although basic operating principles of APFs were introduced in early 1970's, deeper interest has been shown by the advent of self-commutating power semiconductor devices, and the progress of the digital technology, such as microprocessors, micro-controllers, digital signal processors (DSP), and analog-to-digital (A/D) converters.

1.3 Active Power Filter Topologies

Thanks to the self-commutating power semiconductor devices, and new digital control systems, APFs are superior in filtering performance of harmonics compared to the conventional passive filter solutions. APFs can be used not only for filtering of harmonics, but also for reactive power compensation, load balancing, harmonic isolation, voltage regulation, and neutral current and flicker compensation issues. For these purposes, APFs having different circuit topologies, and various connection schemes are being used [15, 16]. Fundamentally, like passive filters, APFs can also be classified as shunt filters, series filters, and as a combination of these as shown in Figures 1.2 and 1.3. Shunt APFs are connected in parallel with the load, and act as a controlled current source. Shunt APFs are mostly suitable for compensating of harmonic currents generated by a load acting as a harmonic current source, such as controlled or uncontrolled rectifiers with inductive load on dc side, or with capacitive load on dc side and

a series passive filter on ac side. Shunt APFs, which are acting as a current source, can also be used for the compensation of negative-sequence, zero-sequence and reactive components of the disturbing loads. On the other hand, series APFs act as a controlled voltage source, which makes them suitable for compensating harmonic voltage sources, such as a rectifier with a capacitive dc load, thus providing isolation between the disturbing load and the supply [17]. The combination of shunt and series connected APFs is referred to as Unified Power Quality Conditioner (UPQC), which provides a complete solution almost for all type of power quality problems. However, UPQC systems are not so common in industry due to their complex power and control circuits, and higher costs as compared to shunt APFs, and conventional solutions.

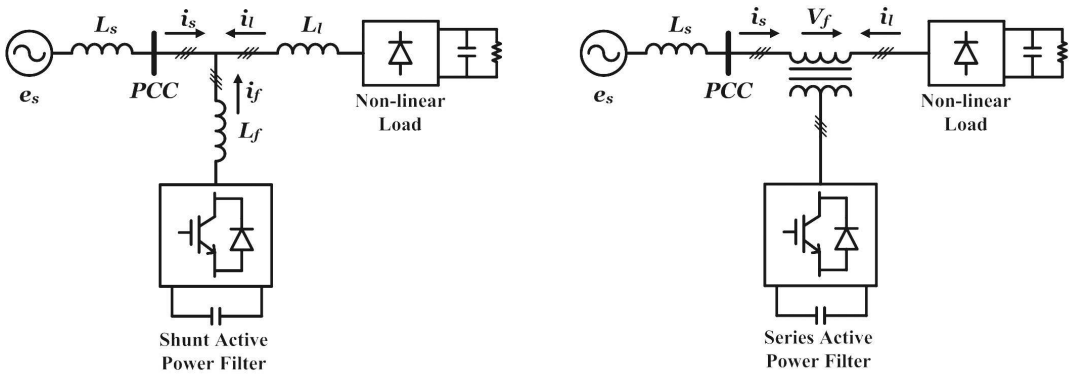


Figure 1.2: Shunt and series connected APFs

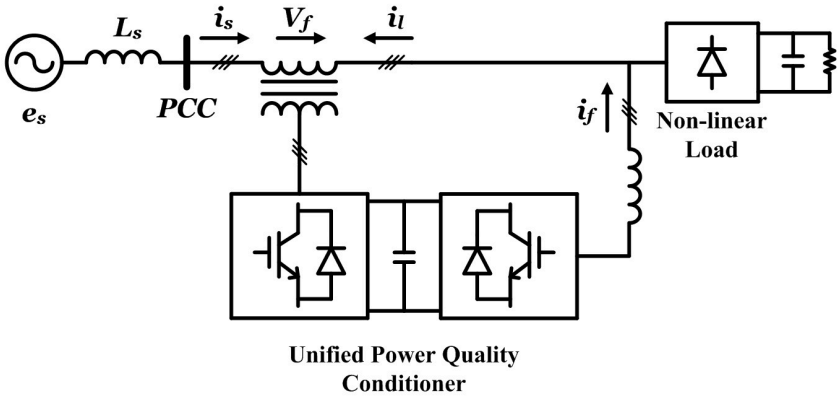


Figure 1.3: UPQC-Combination of shunt and series connected APFs

In some cases, APFs are being used together with passive harmonic filters to reduce the rating of APF. One topology is shown in Figure 1.4, and is referred to as a hybrid filter [16]. The combination of APF with one or more passive harmonic filters makes it possible to reduce the rating of APF significantly both for harmonic filtering, and reactive power compensation. Although, hybrid filters are very attractive for high power applications, special care should be taken in the design, especially for the parallel operation of APFs with passive harmonic filters [18]. In most cases, other existing passive harmonic filters or shunt plain capacitors change the system impedance seen from the load and/or APF side, thus this may deteriorate the performance of APF.

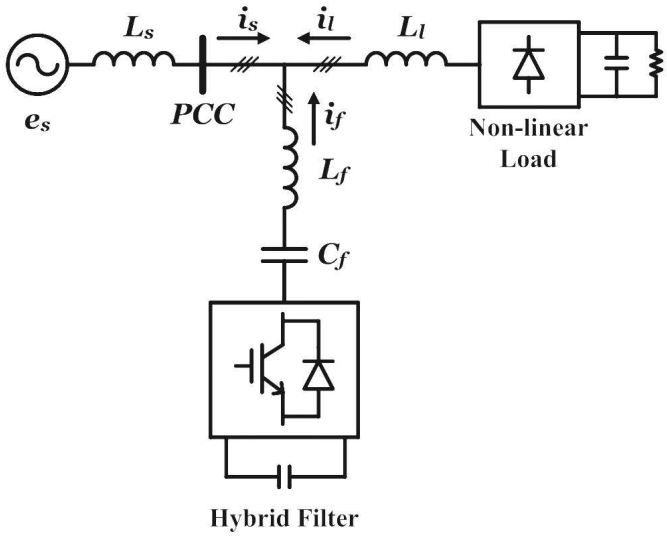


Figure 1.4: Hybrid filter topology

APFs can also be classified as Voltage Source Converter (VSC) based, and Current Source Converter (CSC) based according to their power circuit topologies [19], as shown in Figure 1.5. Vast majority of shunt connected APFs are based on VSC with capacitors in the dc-link, and are considered for connection to low voltage buses. Besides, almost all of the commercially available shunt APFs are being of VSC types [20]-[22]. The VSC based APF consists of a voltage source inverter, a dc link capacitor, and an input filter as shown in Figure 1.5. The dc-link capacitor/s, C_{dc} are used as energy storage elements supplying the energy needed for harmonic or reactive power compensation. VSC based APF is connected to the supply via an input filter. Voltage source inverter is controlled to generate the ac voltages by utilizing the dc-link voltage, thus injecting the required current to network through this input

filter. Besides, input filter also eliminates the undesirable current harmonics generated by the voltage source inverter as a result of Pulse Width Modulation (PWM) at considerably high frequencies. However, in practice, a first order L-type input filter can not provide sufficient attenuation for the current harmonics at modulation frequency. Hence, second or third order, LC- or LCL-type input filters are employed with VSC based APFs [23].

As shown in Figure 1.5, CSC based APF consists of a current source inverter, a dc link reactor, and a second order LC-type input filter [24]-[26]. The energy needed to generate the desired current reference is being stored in the reactor at the dc side. The operation principle of the shunt connected CSC based APF is similar to that of VSC based APF. However, in CSC based APF, reference current is generated directly by modulating the current flowing through the dc-link inductor. Undesired harmonic components due to the high frequency modulation are also filtered out by the second order LC-type input filter. In the literature, VSC based APFs have been considered to be more favorable than CSC based APFs in terms of cost, circuit complexity, and efficiency. On the other hand, fast and superior performance in ac current control, and inherent short circuit protection are the main advantages of the CSC based topology. Comparison of the fundamental characteristics and performances of VSC and CSC based APFs are given in [27]-[29].

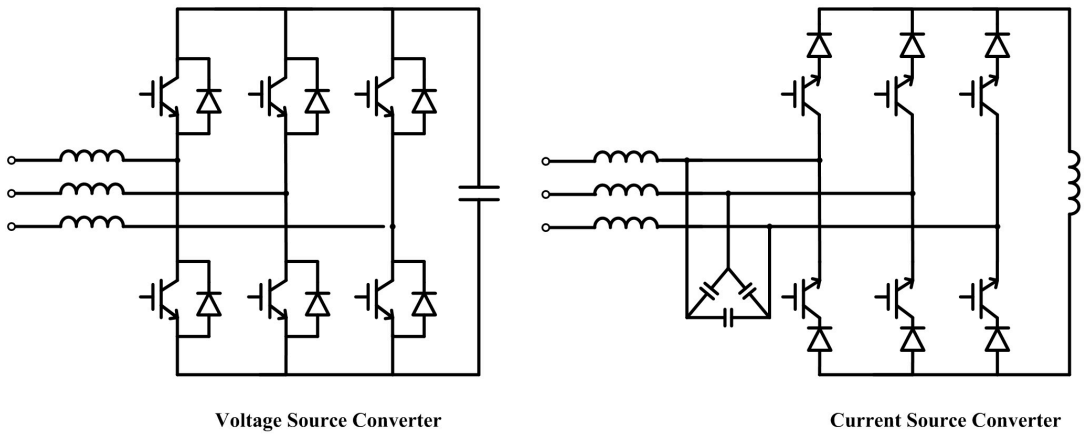


Figure 1.5: Current and voltage source converter based APFs

1.4 Current Source Converter Based Active Power Filters

Although, the CSC based APFs have been reported in the literature, the research work on CSCs are generally based on its use as a rectifier or inverter, especially in ac and dc motor drives [30]-[34]. Hence, the control strategies and waveform modulation techniques have been proposed mostly according to these applications. Unlike VSC based APFs, the number of research works on CSC based ones are limited [35]-[47], although the CSC based APF has been proposed first by Gyugyi in 1976. These research works have been mostly based on the adaptation of the control and modulation techniques, which were proposed for VSC based APFs, to the CSC based ones, and limited to the simulation works and/or laboratory prototypes.

In [26], a CSC based APF with a shunt connected high pass filter has been introduced, where APF suppresses low order harmonics, while high-pass filter does the higher order ones. Hence, an excellent performance over a wide frequency range is obtained with a low switching frequency. Besides, a modified on-line SPWM method has been presented with an effective switching frequency of $2/3^{rd}$ of the carrier frequency. As the complementary of this work, in [36], the oscillations arising from the high pass filter has been suppressed by a feedback controller employing source currents and phase voltages. Besides, it is shown that the time delay arising from the digital controller is also corrected by the use of the proposed feedback controller.

The research in [37] has proposed a CSC based APF with an active damping method employing the voltage across the series filter inductance by the derivatives of the input line currents, to suppress the transient oscillations caused by LC-type input filter without inserting filter resistors. In addition to this, an analysis showing the bandwidth of the APF, that is $1/7^{th}$ of the carrier frequency, has also been presented.

In [38], a simple reference current generation based on lossless resonant elements has been introduced. The lossless element has an infinite gain at the resonant frequency, which is tuned the frequency of the harmonic components to be eliminated. By this way, not only the reference current is obtained, but also the magnitude and phase effect of the LC-type input filter is corrected. However, it suffers from longer response (settling) time, and unstable operation due to the variations in the system parameters and frequency, especially for the

cases, in which inter-harmonics are available.

A decoupled control of the CSC based APF in synchronous reference frame has been introduced in [39] and [40]. Using the proposed strategy, ac and dc control loops, become decoupled and linear, therefore conventional feedback design can be applied. In [39], the proposed method is applied to a case where the ac current control is done via feedback signals from source current, thus reducing the number of the sensor elements.

An artificial intelligent controller for single phase CSC based APFs has been proposed in [41]. The two adaptive linear neurons have been employed to extract the harmonic components of the load current, and to obtain the fundamental component of the phase voltages. Parallel operated units, each tuned to different frequencies, are set to be ON and OFF according to the decisions, based on IEEE Std. 519-1992. The losses of each converter are kept at a minimum by adjusting the dc-link current level according to the magnitude of the current reference. However, due to the complexity of the proposed control system, it was verified only by theoretical simulations.

An on-line carrier based pattern generator for CSCs has been proposed in [42] with unity ac gain and halved switching frequency, and compared with the SVPWM applied to CSCs, as given in [43]. In the method, a dead-band technique is employed with a sawtooth carrier to reduce the number of switchings, where the effective switching frequency becomes half of the carrier frequency at the expense of increased low order harmonics as compared to the triangular carrier case. It also presents the relation between the cycle frequency in SVPWM and the parasitic low order harmonics, which are minimum for a cycle frequency of multiple of 6. Besides, a simple analog implementation of the proposed method was introduced.

In [44], an open-loop control of a CSC based APF has been proposed with minimum number of voltage/current sensors. The reference current to be injected by APF is obtained from line currents of the load, and used in a feedforward control. The oscillations arising from the LC-type input filter are damped without any measurements but by using the dynamic equations of the input filter. However, system is highly sensitive to the deviations of the system parameters, especially the inductance value of the input filter.

In order to reduce the size of the dc-link inductor, a hybrid energy storage in the dc-link of the CSC based APF has been presented in [45]. In this method, hybrid energy storage consists

of a reactor and a capacitor, which is connected to the dc-link of the CSC via two controlled switches (IGBTs) and two diodes. Although the efficiency of the overall system increases and the size of the dc-link reactor decreases, it introduces complex power circuit with complicated control algorithm as well as the reduced filtering performance as compared to the conventional case.

In [46], a four-wire four-leg CSC based APF has been presented, and verified by both theoretical and experimental results with minimum number of current sensors, and a SVPWM method has been adopted to the four-leg CSC as in [44]. However, as discussed above, the size of the dc-link reactor and losses become more significant in four-wire topology, because of the higher dc-link current, which is needed to compensate zero sequence current vector, and increased number of semiconductor devices.

A hybrid filter, which is a CSC based APF with a series capacitor on the ac side, has been proposed in [47]. By this way, the fundamental component of the voltage at the input side of the converter is mostly blocked by the series capacitor, and hence, the voltage stresses on the semiconductor devices are reduced. However, in transient states, or in the case of unbalanced line currents, the voltages on the series capacitors become unbalanced, which may result in high overvoltages on the devices. Hence, the benefit, which comes from the reduced switching losses, disappears due to the extra control of voltage balancing with increased number of switchings.

In summary, few researchers have focused on the analysis and design of CSC based APFs [36]-[47]. Besides, almost all of these research works are limited to theoretical simulations and laboratory work, and any application of the CSC based APF to the industry has not been reported in the literature so far, due to relatively higher converter losses and cost of the conventional CSC based APF configuration as compared to VSC based APF.

1.5 Scope of the Thesis

In this research work, a CSC based APF has been proposed for use in medium voltage, medium power industry applications. A new approach, which is based on the use of the amplification property of the input filter, and called the Selective Harmonic Amplification Method (SHAM) in this thesis, has been proposed in the design of both the control system

and the power stage of the APF. This reduces the kVA rating of the converter considerably, thus eliminating the main disadvantage of the CSCs caused by higher losses of the power stage and storage element as compared to VSCs. In order to make the circuit topology as simple as possible, and to damp out the oscillations due the parallel resonance occurring around the natural frequency of the input filter, passive and active damping solutions have been investigated. A new active damping method based on selective harmonic extraction has been proposed as the damping method to make SHAM applicable. In order to construct the required current waveforms at the output of the APF, different modulation techniques have been investigated, and among them, Dead-band Sinusoidal Pulse Width Modulation (DSPWM) method, which provides minimum low order harmonics, was chosen as the modulator in the proposed APF.

The design procedure has been presented by a systematic approach, and verified by the corresponding computer simulations. An application prototype has been designed and implemented to solve the harmonic current problems of a non-linear load characterized by 12-pulse uncontrolled rectifiers in a Light Rail Transportation system, which are injecting excessive 11^{th} and 13^{th} current harmonics to the network. Theoretical results obtained in EMTDC/PSCAD have been verified by the corresponding laboratory and field test results.

The application prototype of the CSC based APF is composed of 205 kVA CSC, and 95 kVAr input filter capacitor, and is connected to the MV bus via a delta-wye connected coupling transformer of 34.5/1.1 kV, 1600 kVA. The coupling transformer is already available for the connection of a Thyristor Switched Shunt Reactor (TSSR) of 1250 kVAr to compensate for the capacitive reactive power of the long MV underground cables. Although the rating of the CSC is chosen to be only 205 kVA, thanks to the proposed SHAM, the overall APF rating becomes 450 kVA. The leakage inductance of the transformer acts as the series inductance of the input filter, thus eliminating the need for an extra series inductance, and making the circuit topology simple. The input filter is tuned to 780 Hz to provide sufficient elimination of carrier harmonics as well as required amplification of the 11^{th} and 13^{th} harmonic components. As the switching elements, HV Insulated Gate Bipolar Transistor (IGBT), and HV fast-recovery diode modules with isolated cases have been used. Effective switching frequency of the semiconductor devices are reduced by the application of DSPWM method for a carrier frequency of 3.0 kHz. Cooling of the semiconductor devices has been achieved by use of a water cooling system employing a water-to-air heat exchanger. Dc-link reactor was chosen as to be an iron-core reactor for reducing losses, and saving from space.

This research work makes the following original contributions to the area of CSC based APF systems:

- A new approach to the design of the control system and power stage of CSC based APF, which brings a significant reduction in the converter kVA rating by use of the amplification property of the input filter, which is called the Selective Harmonic Amplification Method (SHAM) in the thesis.
- Proposal of a new active damping method based on selective harmonic extraction technique, to make SHAM applicable.
- First design and implementation work of medium voltage, medium power CSC based APF system by making it a cost competitive alternative to conventional VSC based APFs.
- First application of CSC based APF to an industrial load, characterized by 12-pulse uncontrolled rectifiers, supplying the catenary lines of a Light Rail Transportation system.
- Presentation of the design procedure using a systematic approach based on theoretical analyses, and simulation works for the proposed CSC based APF.
- Verification of the proposed design approach to CSC based APF system by field test results.

The outline of the thesis is given below:

In Chapter 2, operation principles of the CSC based APF is described. After presenting the simplified circuit configuration, reference current generation techniques in APF applications are discussed, and the selective harmonic extraction method based on synchronous reference frame, which is used in this work, is described in detail. As the part of the reference current generation, the proposed active damping method, reactive power and dc-link control issues are explained with the necessary analyses and simulation works. Comparing the applicable on-line pattern generation (modulation) techniques to CSCs, DSPWM method is explained with its application both in analog and digital control systems.

In Chapter 3, the proposed SHAM is explained on a specific example, and the key points in the design of the input filter to reduce the kVA rating of the CSC are presented. Suppression

of the carrier harmonics, and hence the selection of the carrier frequency are also given in conjunction with the input filter design.

In Chapter 4, design principles and implementation of a medium voltage, medium power CSC based APF are presented. After characterization of the non-linear load, technical specifications of the prototype system are given. Next, sizing of the input filter elements is described. Besides, determination of the active damping gain is presented for the corresponding filter elements. Then, the dc-link reactor design and the selection of semiconductor devices are described. Optimization of the turn-on/turn-off resistances of the gate drive circuits are also given for the chosen IGBTs and diodes as well as the design of power stage layout including the details of laminated busbars. Design criteria of the heatsinks of semiconductor devices, and the cooling system are described with the theoretical loss calculations based on simulated voltage and current waveforms. Design and implementation of protection and control systems applied to the implemented CSC based APF are also presented.

In Chapter 5, theoretical results obtained by simulation works, and experimental results obtained by field tests on the application prototype of the CSC based APF are presented. Field test results include technical performance indices such as current/voltage waveforms on ac and dc sides, and their harmonic spectra. The results of field tests have shown that the prototype CSC based APF successfully eliminates the 11^{th} and 13^{th} harmonic components of the 12-pulse uncontrolled rectifiers supplying the catenary lines of a LRT system, and thus complying with the associated limits specified in the IEEE Std. 519-1992.

General conclusions are given in Chapter 6 with proposals of a further study.

In Appendix A, equivalent analog circuit representation of the DSPWM based on-line pattern generator is given.

The Fortran code of the gate pattern generator constructed in EMTDC/PSCAD is given in Appendix B.

CHAPTER 2

OPERATION PRINCIPLES OF CURRENT SOURCE CONVERTER BASED ACTIVE POWER FILTER

2.1 Introduction

A CSC based APF, which is assumed to act as an ideal current source is capable of generating any kind of reference current waveform depending on the application purposes, such as harmonic filtering, reactive power compensation, load balancing, and neutral current compensation. For each of these applications, appropriate circuit topologies and control schemes should be employed. As discussed in the previous chapter, shunt connected APFs are well suited for filtering of current harmonics.

When the harmonic filtering is under discussion, correct identification of the load harmonics, and determination of the topology and installed power of the APF are important design issues. In most cases, there are usually a few harmonic current components that should be filtered out to comply with the limit values specified in IEEE Std.519-1992. Hence, elimination of one or a few harmonic current components would be sufficient to meet the objectives. For that reason, first defining the harmonic current components exceeding the limit values, and then, designing the circuit topology and the control system of proposed APF according to these selected components would be a proper engineering approach in the view of technical and economical aspects. 6-pulse and 12-pulse power converters are very common in several industry applications, such as power supplies and ac/dc motor drives. Harmonic current components of the orders of $6n \pm 1$ and/or $12n \pm 1$ are mostly seen in distribution systems. However, it is usually sufficient to comply with the standards/regulations by filtering one of these harmonic groups, e.g. elimination of 11^{th} and 13^{th} harmonics of 12-pulse converters as

described in this thesis.

The best practice for the elimination of harmonics, or for the compensation of reactive power, is to solve the problem as close as possible to its source, thus avoiding the other loads at the same busbar from being disturbed . However, in some applications, it is not possible to solve the problem using this approach, due to the limitations arising from power system design. Besides, there might be many non-linear loads generating harmonics or demanding reactive power, and in that case, it would not be feasible to solve the problems individually rather than bringing a group solution. Therefore, it may be required to solve the problem at an upper (voltage) level, which is usually the MV bus.

Since the cost of a coupling transformer is seen as the main drawback in MV, medium/high power applications, many research works have been presented to achieve a transformerless operation, in particular series capacitor based hybrid filters for VSC based APFs [48]-[51]. However, due to the limitations in the voltage ratings of the available semiconductor devices, and the reliability issues, no such work has been reported yet for the transformerless operation of APFs at MV level. Most of the systems connected to the MV bus without coupling transformers are based on series operation of semiconductor devices and multi-level topologies [52, 53].

Almost in all medium power applications, coupling transformers are being used for either reducing the voltage and/or current rating of the APFs, or providing an isolation between the supply and the converter. The CSC based APF described in this thesis has a coupling transformer for the connection of APF to the MV bus. Besides, the coupling transformer serves also as a part of input filter as described in the following sections.

In this chapter, the system description and operation principles of a shunt connected CSC based APF, which is used for eliminating some pre-selected current harmonics generated by a non-linear load, will be presented. After describing the basic circuit topology of the CSC based APF, reference current generation, and waveform modulation methods will be described in detail. At the end of the chapter, brief conclusions will be posted.

2.2 System Description

2.2.1 Basic Circuit Configuration

Single line diagram of the CSC based APF connected to a MV bus is given in Figure 2.1. It is composed of a CSC, a MV/LV coupling transformer, an optional series reactor with an optional parallel resistor, and a shunt connected capacitor. CSC is consisting of six fully controllable power semiconductor devices, each having a unidirectional current carrying, and bipolar voltage blocking capability, and a dc-link reactor being used as the energy storage element as shown in Figure 2.2.

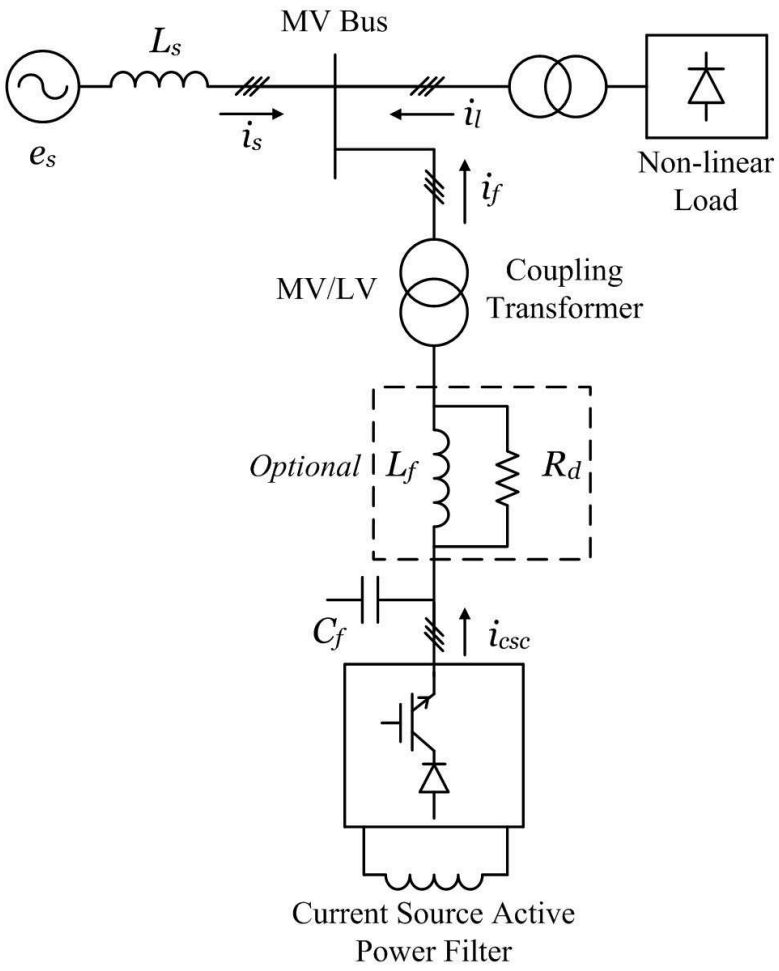


Figure 2.1: Single line diagram of CSC based APF

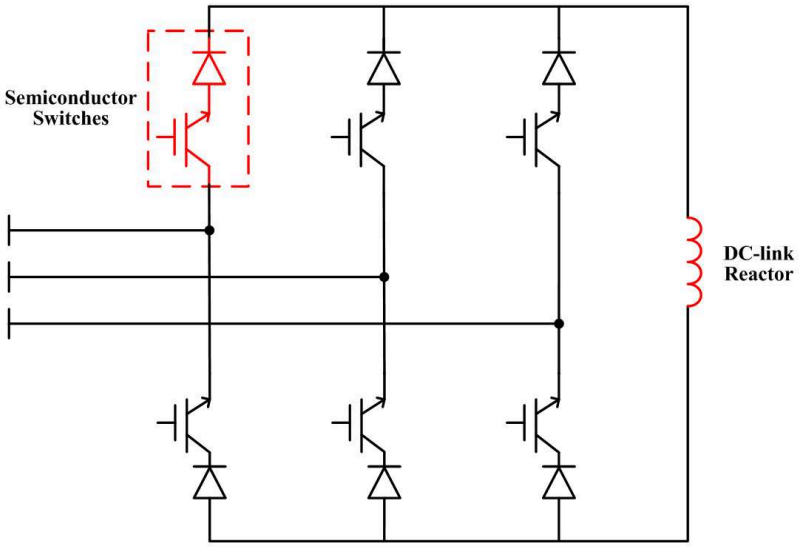


Figure 2.2: Current Source Converter

The output current of the CSC, i_{csc}, is generated by modulating the current flowing through the dc-link reactor, which is almost constant during a switching period. Hence, output current waveform of the CSC has high frequency harmonic current components as well as the harmonic components to be eliminated by APF, and a fundamental component at the supply frequency. In order to filter out the undesired high frequency harmonic components, referred to as switching ripples, an LC-type input filter is employed as shown in Figure 2.1. Unlike CSC based STATCOM applications [30], the output current of the CSC contains both switching ripples, and harmonic current components, which are being eliminated by the CSC based APF. Hence, LC-type input filter may also amplify or attenuate the harmonic current components to be filtered out. For that reason, the design of LC-type input filter requires a more detailed work as described in the next chapter.

The shunt connected capacitor, C_f in Figure 2.1, is providing a low impedance path both for the switching ripples of the CSC, and the recovery currents during commutation periods [30]. The series connected external inductance, L_f, which is optional, and the leakage inductance of the coupling transformer makes the total inductance for LC-type input filter. L_f is optional because, in most cases, the leakage inductance of the transformer would be sufficient to provide the required input filter inductance. However, in some applications, L_f provides an extra flexibility for the tuning of the corner frequency of the LC-type input filter.

The LC-type input filter, having a natural frequency to be selected according to the application type, is seen as a parallel resonant circuit from the CSC side. Hence, harmonic current components, generated by CSC, around the natural frequency of the input filter would be amplified, and high amounts of oscillations would be seen at the supply side. In order to damp out these oscillations, either an external damping resistor, R_d as in Figure 2.1, or an active damping method should be employed.

2.2.2 Basic Operation Principles

The operation principle of the CSC based APF simply requires the generation of the reference current vectors, and then modulation the current flowing through the dc-link inductor according to these reference current vectors. In order to accomplish this work, CSC based APF has a control system whose block diagram is as illustrated in Figure 2.3. The control system has two main parts: (i) reference current generation, (ii) waveform modulation. Reference current generation block in Figure 2.3 is responsible from extracting the harmonic current components to be filtered out from the line currents of the load, and generating the resultant current vectors to be modulated. On the other hand, waveform modulation block is responsible from generating the switching commands to power semiconductor devices according to the corresponding reference current vectors. By this way, CSC injects the required currents through the LC-type input filter to the supply.

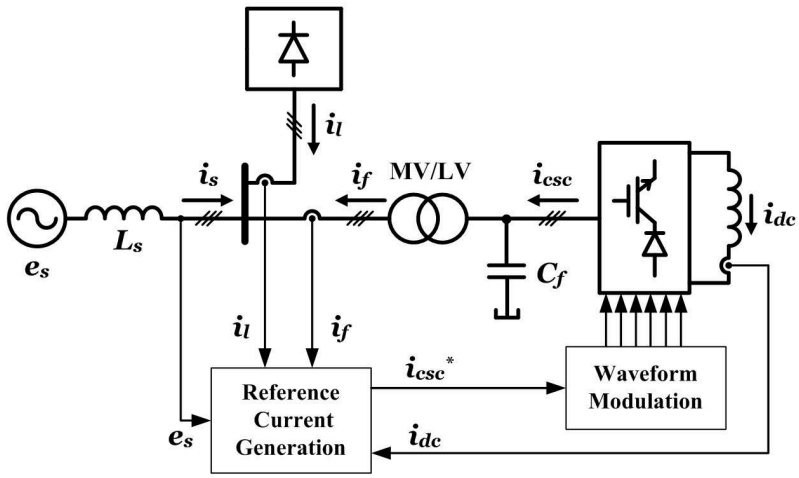


Figure 2.3: Simple block diagram of the control system

Output current of CSC, i_{csc}, in Figure 2.4, is being modulated by the current flowing through the dc-link reactor, and has a chopped waveform. Thus, it is rich in harmonics, including the harmonic components at the frequencies to be selected for filtering, and at the sidebands of the carrier frequency. This chopped current waveform is smoothed while passing through the LC-type input filter, and is transformed to a sinusoidal waveform. Owing to the proposed control system, the output currents of the CSC are being generated in a way that, output currents of the APF are equal in magnitude, but in anti-phase with the pre-selected harmonic current components of the load current. By this way, at those pre-selected frequencies, the harmonic components at PCC will be ideally zero.

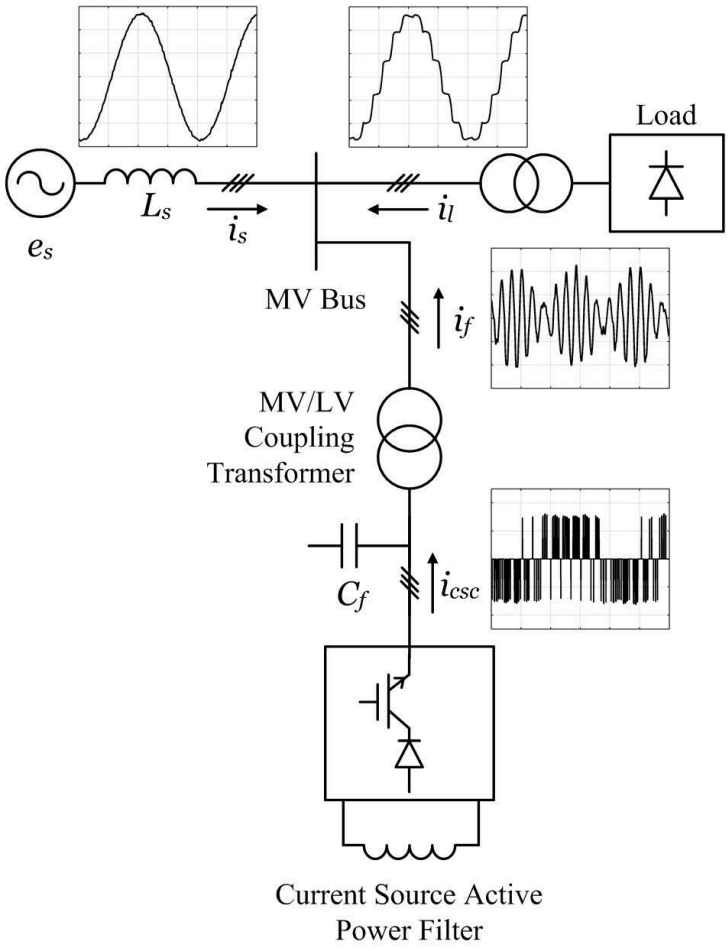


Figure 2.4: Illustration of CSC and APF currents

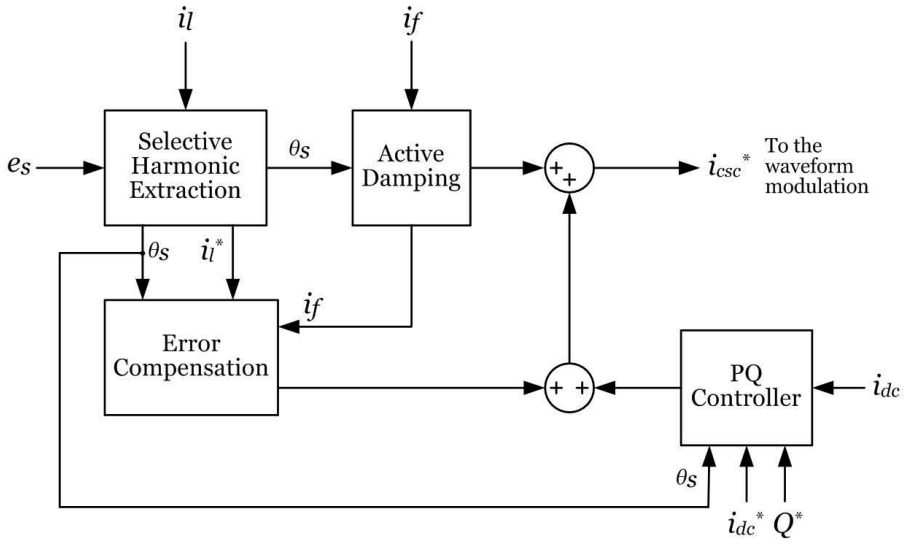


Figure 2.5: Block diagram of the reference current generation

2.3 Reference Current Generation

A closer form of the Reference Current Generation block is given in Figure 2.5. The harmonic components of the load current, at pre-selected frequencies, are extracted by employing the Selective Harmonic Extraction sub-circuit. Active Damping sub-circuit generates the reference current vectors to suppress the undesired oscillations around the natural frequency of the input filter. Besides, Error Compensation sub-circuit is used as a feedback controller to compensate for the error at the output current of APF. Finally, the fundamental current controller, or simply the PQ Controller, generates the reference current vectors at fundamental frequency to provide the required active power flow keeping the dc-link current at its desired value, and reactive power flow, if it is desired. The sum of the outputs of all these sub-circuits is being used as the final reference current vector to be modulated.

2.3.1 Harmonic Current Extraction Method

In order for the CSC based APF to operate effectively, generation of correct reference current vectors is a critical point. First of all, the harmonic components of the load current should be extracted without any gain or phase error. Many techniques, both in time and frequency domains, have been reported and evaluated for extracting the harmonic current/voltage com-

ponents in APF applications [54]-[56]. The frequency-domain methods are mainly identified rearranged forms of Fourier analysis. The main purpose is to provide the result as fast as possible with a reduced number of calculations, to allow a real time implementation using Digital Signal Processors (DSPs). The main drawbacks of the Fourier-based harmonic extraction techniques are: large memory requirements for storage, large computational power required for the DSPs, and unsatisfactory performance during transients.

On the other hand, time domain methods for the extraction of harmonics offer increased speed, and fewer calculations with precise results. The most common methods employed in time domain are: Instantaneous Power Theory (IPT), and Synchronous Reference Frame Method (SRFM) [15, 54, 59].

2.3.1.1 Instantaneous Power Theory (IPT)

The IPT, which is also referred to as *"p-q theory"*, determines the harmonic distortion by calculating the instantaneous power in a three-phase system, which is the multiplication of the instantaneous values of the currents and voltages [57]. The IPT uses $\alpha\beta 0$ transformation, also known as the Clarke transformation, which transforms the three phase quantities in *abc* reference frame into the $\alpha\beta 0$ reference frame. The Clarke transformation, and its inverse transformation for three phase voltages are given by (2.1) and (2.2), respectively.

$$\begin{bmatrix} v_\alpha \\ v_\beta \\ v_0 \end{bmatrix} = C_1 \cdot \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{2.1}$$

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = C_1^{-1} \cdot \begin{bmatrix} v_\alpha \\ v_\beta \\ v_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 & \frac{1}{\sqrt{2}} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \\ v_0 \end{bmatrix}. \tag{2.2}$$

Similarly, transformations can be written for current vectors as given in (2.3), and (2.4).

$$\begin{bmatrix} i_\alpha \\ i_\beta \\ i_0 \end{bmatrix} = C_1 \cdot \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{2.3}$$

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = C_1^{-1} \cdot \begin{bmatrix} i_\alpha \\ i_\beta \\ i_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 & \frac{1}{\sqrt{2}} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \\ i_0 \end{bmatrix} \tag{2.4}$$

Since, the terms corresponding to the zero sequence currents and voltages will disappear for three-phase three-wire systems, such as MV distribution systems, instantaneous current and voltage vectors can be expressed by

(2.5) and (2.6), respectively.

$$\boldsymbol{i} = i_\alpha + j\, i_\beta \tag{2.5}$$

$$\boldsymbol{v} = v_\alpha + j\, v_\beta \tag{2.6}$$

The instantaneous power, ***s*** can be expressed by using the current and voltage vectors as given in

(2.7), and (2.8).

$$\boldsymbol{s} = \boldsymbol{v} \cdot \boldsymbol{i}^* = (v_\alpha + j\, v_\beta) \cdot (i_\alpha - j\, i_\beta) = \underbrace{(v_\alpha i_\alpha + v_\beta i_\beta)}_{\boldsymbol{p}} + j\ \underbrace{(v_\beta i_\alpha - v_\alpha i_\beta)}_{\boldsymbol{q}} \tag{2.7}$$

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{2.8}$$

The real and imaginary powers expressed in (2.7) have both dc and ac components. The dc terms correspond to the conventional active and reactive powers at fundamental frequency, whereas ac terms correspond to the harmonic powers arising from the harmonic components of the load current provided that, supply voltage do not contain harmonics. Hence, if it is wanted to extract the harmonic components of the load current, high frequency components

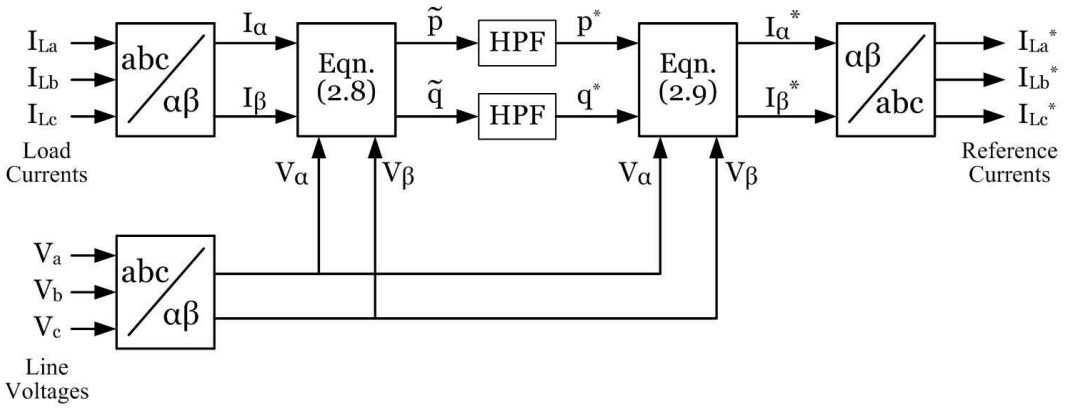


Figure 2.6: Harmonic extraction by *"Instantaneous Power Theory"*

of p, and q in (2.7) should be filtered out as illustrated in Figure 2.6. In practice, High Pass Filter (HPF) in Figure 2.6 is implemented by employing a Low Pass Filter as **(1-LPF)** in order to avoid the phase shift coming from HPF. Since LPF does not introduce a phase shift to the dc signal, there will be no phase error. If reactive power compensation is also desired as well as harmonic filtering, both ac and dc terms of q should be used as reference imaginary power.

After extracting the AC components of p, and q in (2.8), the reference current vectors can be obtained by applying the transformations in (2.9), and (2.10) as follows:

$$\begin{bmatrix} i_\alpha^* \\ i_\beta^* \end{bmatrix} = -\frac{1}{v_\alpha^2 + v_\beta^2} \cdot \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \begin{bmatrix} \tilde{p} \\ \tilde{q} \end{bmatrix} \tag{2.9}$$

$$\begin{bmatrix} i_a^* \\ i_b^* \\ i_c^* \end{bmatrix} = \sqrt{\frac{2}{3}} \cdot \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_\alpha^* \\ i_\beta^* \end{bmatrix} \tag{2.10}$$

The expression in (2.9) is not adequate if the system has a zero sequence component due to an existing unbalance. Thus, a zero sequence power must be added to provide a complete analysis [58]. In addition to this, if the supply voltages are distorted, the reference vectors will be affected, and the result will not be satisfactory. Hence, supply voltages should be filtered before using in the IPT.

As illustrated in Figure 2.6, all the harmonic components, and the reactive power component at fundamental frequency can be extracted by employing IPT. If it is required to filter out some of the harmonic components of the load current at pre-selected frequencies rather than all of them, a notch filtering approach should be employed, which could be already done in *abc* reference frame. Therefore, IPT is not a very suitable method for a selective harmonic extraction/elimination approach.

2.3.1.2 Synchronous Reference Frame Method (SRFM)

SRFM is based on the space vector representation of the current and voltage signals. The load currents at stationary ($\alpha\beta$) reference frame are transformed into a rotating frame, referred to as *dq* reference frame, by means of the Park transformation matrix, C_2 as follows:

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = C_2 \cdot \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} cos\,\theta_h & sin\,\theta_h \\ -sin\,\theta_h & cos\,\theta_h \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{2.11}$$

where θ_h is the phase angle information of the corresponding reference frame. In Figure 2.7, this transformation is illustrated by means of space vectors.

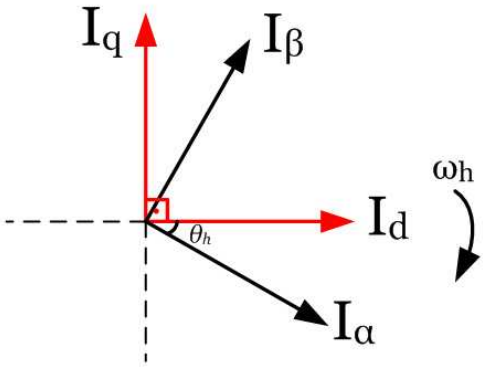


Figure 2.7: Space vectors in $\alpha\beta$ and *dq* coordinates

The *dq* reference frame is rotating at an angular speed, ω_h at a selected frequency, which makes the harmonic components at that frequency dc, and all other harmonics, ac values. Thus, if the angular speed of the reference frame is equal to that of fundamental frequency,

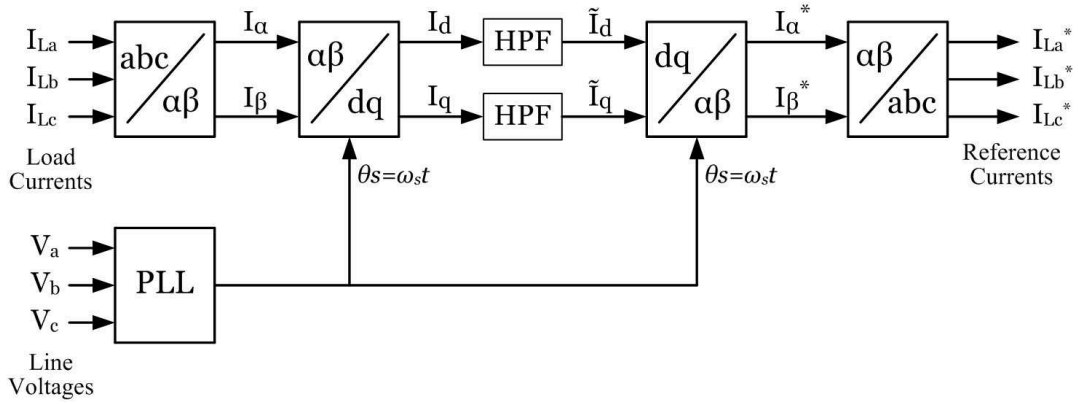


Figure 2.8: Harmonic extraction by Synchronous Reference Frame Method

positive sequence of the fundamental component will appear as dc component, and all other harmonics, as well as the negative sequence of the fundamental one, will be appear as ac components [59, 60]. Hence, harmonic components of the load current to be eliminated by the APF can be easily obtained by filtering out the dc components of the current vectors in *dq* reference frame, as illustrated in Figure 2.8. If the load current has a negative sequence component, and there is no load balancing issue under consideration; another synchronously rotating frame should be employed to eliminate the negative sequence component from the final reference current vectors, which is seen as 100 Hz component for the positive rotating frame [2, 59].

The reference vectors, obtained by filtering out the dc components of current vectors in *dq* reference frame, are then transformed back into the $\alpha\beta$ reference frame by means of inverse Park transformation matrix, ${C_2}^{-1}$ as in (2.12). Then, final reference current vectors can be obtained by applying the inverse Clarke transformation matrix, ${C_1}^{-1}$, as in the IPT.

$$\begin{bmatrix} i_\alpha^* \\ i_\beta^* \end{bmatrix} = C_2^{-1} \cdot \begin{bmatrix} i_d^* \\ i_q^* \end{bmatrix} = \begin{bmatrix} cos\ \theta_h & -sin\ \theta_h \\ sin\ \theta_h & cos\ \theta_h \end{bmatrix} \begin{bmatrix} i_d^* \\ i_q^* \end{bmatrix} \tag{2.12}$$

Let the load current, I_L in Figure 2.8 be expressed by (2.13).

$$
\begin{aligned}
I_a &= \hat{I}_1 cos(\omega_s t + \varphi_1) + \hat{I}_{11} cos(11\omega_s t + \varphi_{11}) + \hat{I}_{13} cos(13\omega_s t + \varphi_{13}) \\
I_b &= \hat{I}_1 cos(\omega_s t - \tfrac{2\pi}{3} + \varphi_1) + \hat{I}_{11} cos(11\omega_s t + \tfrac{2\pi}{3} + \varphi_{11}) + \hat{I}_{13} cos(13\omega_s t - \tfrac{2\pi}{3} + \varphi_{13}) \\
I_c &= \hat{I}_1 cos(\omega_s t + \tfrac{2\pi}{3} + \varphi_1) + \hat{I}_{11} cos(11\omega_s t - \tfrac{2\pi}{3} + \varphi_{11}) + \hat{I}_{13} cos(13\omega_s t + \tfrac{2\pi}{3} + \varphi_{13})
\end{aligned}
\tag{2.13}
$$

where $\hat{I}_1$, $\hat{I}_{11}$ and $\hat{I}_{13}$ are magnitudes of the fundamental, 11th, and 13th harmonic components of the load current with phase angles of φ_1, φ_{11}, and φ_{13}, respectively.

By applying the Clarke transformation matrix, C_1 as given in (2.14), line currents in *abc* reference frame can be transformed into the $\alpha\beta$ reference frame,

$$
\begin{aligned}
I_\alpha &= \sqrt{\tfrac{3}{2}} \{\hat{I}_1 cos(\omega_s t + \varphi_1) + \hat{I}_{11} cos(11\omega_s t + \varphi_{11}) + \hat{I}_{13} cos(13\omega_s t + \varphi_{13})\} \\
I_\beta &= \sqrt{\tfrac{3}{2}} \{\hat{I}_1 sin(\omega_s t + \varphi_1) - \hat{I}_{11} sin(11\omega_s t + \varphi_{11}) + \hat{I}_{13} sin(13\omega_s t + \varphi_{13})\}.
\end{aligned}
\tag{2.14}
$$

The current vectors in $\alpha\beta$ reference frame are then transformed into the *dq* reference frame, which is rotating at a frequency identical to that of supply, ω_s, as in (2.15).

$$
\begin{aligned}
I_d &= \sqrt{\tfrac{3}{2}} \{\hat{I}_1 cos(\omega_s t - \theta_h + \varphi_1) + \hat{I}_{11} cos(11\omega_s t + \theta_h + \varphi_{11}) + \hat{I}_{13} cos(13\omega_s t - \theta_h + \varphi_{13})\} \\
I_q &= \sqrt{\tfrac{3}{2}} \{\hat{I}_1 sin(\omega_s t - \theta_h + \varphi_1) - \hat{I}_{11} sin(11\omega_s t + \theta_h + \varphi_{11}) + \hat{I}_{13} sin(13\omega_s t - \theta_h + \varphi_{13})\}
\end{aligned}
\tag{2.15}
$$

Fundamental components in (2.15) become dc values, whereas 11th and 13th harmonics remain as ac components with a frequency shift of ω_s, provided that $\theta_h = \omega_s t$, as given in (2.16). Hence, if the dc components of the current vectors are filtered out by a HPF (or 1-LPF), resultant vectors will be the reference current vectors for APF. Since, 11th component is a negative sequence, and 13th is a positive sequence component regarding the fundamental (positive sequence), both will have an angular frequency of $12\omega_s$ as in (2.16).

$$I_d = \sqrt{\frac{3}{2}} \{\hat{I}_1 cos(\varphi_1) + \hat{I}_{11} cos(12\omega_s t + \varphi_{11}) + \hat{I}_{13} cos(12\omega_s t + \varphi_{13})\}$$
$$I_q = \sqrt{\frac{3}{2}} \{\hat{I}_1 sin(\varphi_1) - \hat{I}_{11} sin(12\omega_s t + \varphi_{11}) + \hat{I}_{13} sin(12\omega_s t + \varphi_{13})\} \quad (2.16)$$

After extracting the dc values from the current vectors in (2.16), final reference current vectors in *dq* frame are given by (2.17).

$$I_d{}^* = \sqrt{\frac{3}{2}} \{\hat{I}_{11} cos(12\omega_s t + \varphi_{11}) + \hat{I}_{13} cos(12\omega_s t + \varphi_{13})\}$$
$$I_q{}^* = \sqrt{\frac{3}{2}} \{-\hat{I}_{11} sin(12\omega_s t + \varphi_{11}) + \hat{I}_{13} sin(12\omega_s t + \varphi_{13})\}\cdot \quad (2.17)$$

Reference vectors, $I_d{}^*$ and $I_q{}^*$, are then back transformed into the *abc* frame by applying inverse Clarke, and Park transformation matrices, ${C_2}^{-1}$ and ${C_1}^{-1}$, respectively.

In opposition to the IPT, the advantage of the SRFM is that supply voltage waveforms do not have any effect on the reference current generation process, provided that the angular speed of the rotating frame is correctly determined. Hence, in SRFM, determination of the phase angle (or angular speed) of the rotating frame is a critical process, which is done by employing a Phase Locked Loop (PLL), as described in the following subsection.

Another important fact about SRFM is that any harmonic component can be extracted individually by applying an associated synchronously rotating frame for each harmonic component. For that reason, SRFM was chosen as the harmonic extraction method in this work.

2.3.1.3 Phase Locked Loop

Phase Locked Loop (PLL) algorithm is very critical for harmonic extraction techniques employing synchronously rotating frames. The phase angle information obtained by PLL determines the performance of the APF. There have been many methods reported to find the phase angle information, especially under distorted supply conditions as reviewed in [61]. Among them, Synchronous Reference Frame PLL (SRF-PLL) is simple, and used in almost all PLL techniques for three-phase systems [62]. The basic block diagram of the SRF-PLL is as given in Figure 2.9.

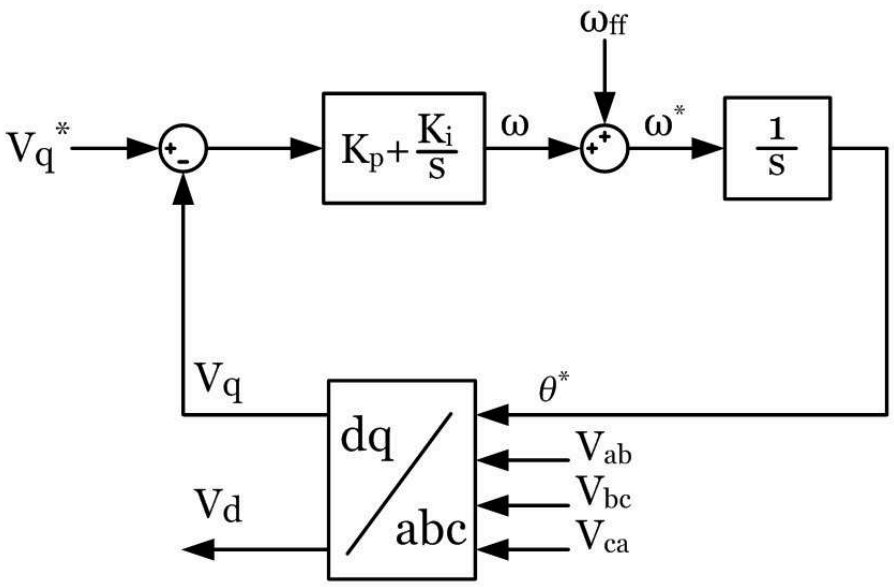


Figure 2.9: Block diagram of the PLL circuit

The line-to-line voltages in stationary (*abc*) reference frame are transformed into the synchronously rotating (*dq*) reference frame by using the phase angle information θ^*, which is synchronized to the utility frequency, and associated Clarke and Park transformation matrices, C_1, and C_2 in (2.1), and (2.11), respectively. θ^* is obtained by integrating a frequency command ω^*. If the frequency command ω^* is identical (locked) to the utility frequency, the voltages, V_d and V_q will appear as dc quantities, where V_q will be zero.

The PI regulator used to obtain the value of θ^* drives the feedback voltage V_q to the commanded value $V_q{}^*$, which is simply zero. Hence, PI regulator results in a rotating reference frame making the V_q zero, and thus necessitates the frequency of this reference frame to be chosen equal to the frequency of the utility voltage.

The main consideration evaluating the performance of the SRF-PLL is its behavior under distorted utility conditions. Since, SRF-PLL has two integrators in the control loop, an inherent filtering is employed against these distortions. Besides, adjusting the gains of the integrators (or reducing the bandwidth of the controller), problems arising from the distorted utility conditions can also be minimized. However, reducing the SRF-PLL bandwidth results in the increase of response time, and the system can not track the angle θ^* quickly [61].

2.3.1.4 Selective Harmonic Extraction via SRFM

In MV applications, only a few harmonic components are usually exceeding the limit values, and in most cases, it is sufficient to eliminate those components for complying with IEEE Std. 519-1992. Furthermore, the need for the elimination of each harmonic component exceeding the limit values would not be identical for a given application. For instance, at least a 70 % filtering performance might be required for the 11^{th} harmonic component, on the other hand, 40 % filtering performance might be sufficient for 13^{th} harmonic component in order to comply with IEEE Std. 519-1992. Hence, by the use of the elective harmonic extraction approach, any harmonic component at pre-selected frequencies can be extracted as the reference for APF, and independent control loops can be employed for each harmonic component to achieve different filtering performances, which also obviously reduce the required installation capacity [63, 64].

SRFM is chosen as the harmonic extraction method in the CSC based APF, because of two main advantages: if the phase angle information is correct, current vectors are not affected by distorted supply voltages; and any harmonic component, at pre-selected frequencies, can be extracted by employing the associated synchronously rotating reference frames. In order to apply SRFM to different harmonic components, a number of synchronous reference frames having different frequencies should be used [65]. A block diagram showing the selective harmonic extraction process for 11^{th} and 13^{th} harmonic components as an example is given in Figure 2.10.

As seen from Figure 2.10, two independent loops, one for each harmonic component, are used. In each loop, synchronous reference frames with the frequencies identical to those of harmonic components are employed. For 11^{th} harmonic component, the synchronously rotating reference frame has an angular frequency of $-11\omega_s$, thus making the 11^{th} harmonic components dc in dq reference frame. Similar case is also valid for 13^{th} harmonic component, provided that associated reference frame has an angular frequency of $13\omega_s$. After making the harmonic components dc values in dq reference frame, LPFs are used to extract these components without any gain or phase error. Then, these extracted dc components are transformed back into the $\alpha\beta$ reference frame by employing back transformations.

The currents injected by the CSC are subject to change, both in magnitude and phase angle

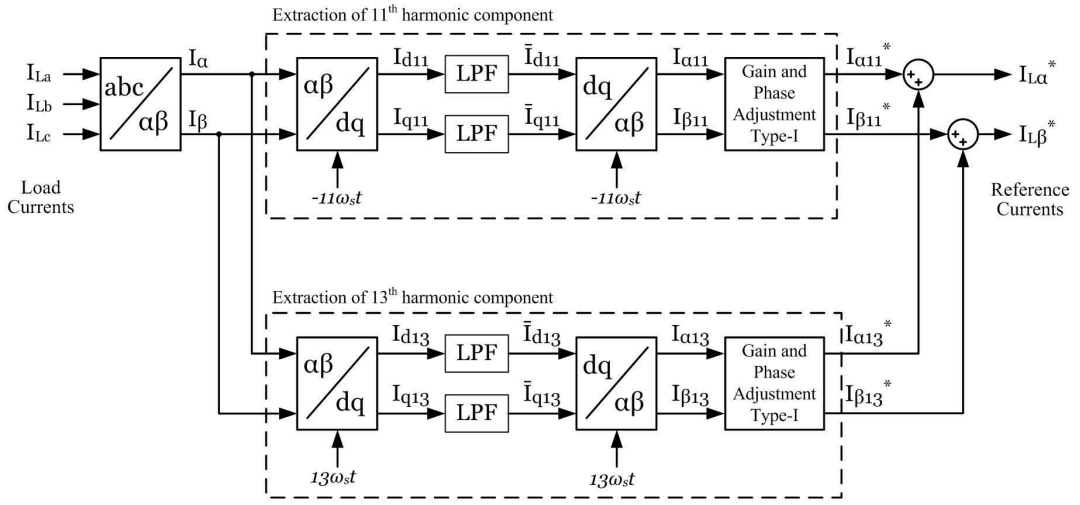


Figure 2.10: Extraction of 11th and 13th harmonic components

while passing through the LC-type input filter owing to the gain and frequency response of the input filter at that frequency. Hence, the reference current vectors, to be generated and injected by CSC, should be adjusted to obtain a resultant output current (of APF), which is equal in magnitude, but in anti-phase with the reference current extracted from the line currents of the load, thus making those harmonic components zero at PCC. Gain and Phase Adjustment blocks of Type-I in Figure 2.10 are used to modify the references in each loop in this manner. In addition to the input filter, coupling transformer also necessitates a further requirement for the gain and phase adjustment. Since, the load currents are measured from MV bus, they should be transferred to the LV side according to the turns ratio, *n* of the transformer. Besides, a delta-wye connected transformer, which is very common in distribution systems, results in a need of phase correction of 30 *degrees* depending on the connection group of the transformer. For instance, if the connection group is Dyn11, secondary currents/voltages lead the primary ones by an angle of 30 *degrees*. As a result, these adjustments arising from the coupling transformer are also achieved with the Gain and Phase Adjustment blocks of Type-I. Besides, the control delay owing to the digital control system can also be compensated by the use of Gain and Phase Adjustment blocks. Although the control delay corresponds to different phase delays in 11th and 13th harmonic components, they can be corrected easily by the help of independent reference current generation loops.

Let again the load currents in *abc* reference frame be as in (2.13). In this case, the 11th and 13th harmonic components of the load current will be extracted separately by using the selective harmonic extraction via SRFM. The load currents in (2.13) are first transformed into the *dq* reference frames by using phase angle information of $\theta_{11} = -11\omega_s t$, and $\theta_{13} = 13\omega_s t$ in two independent loops, as shown in Figure 2.10. Current vectors in the synchronous reference frame, which is rotating at $-11\omega_s$ are given by (2.18).

$$\begin{aligned} I_{d11} &= \sqrt{\tfrac{3}{2}}\,\{\hat{I}_1 cos(12\omega_s t + \varphi_1) + \hat{I}_{11} cos(\varphi_{11}) + \hat{I}_{13} cos(24\omega_s t + \varphi_{13})\} \\ I_{q11} &= \sqrt{\tfrac{3}{2}}\,\{\hat{I}_1 sin(12\omega_s t + \varphi_1) - \hat{I}_{11} sin(\varphi_{11}) + \hat{I}_{13} sin(24\omega_s t + \varphi_{13})\}. \end{aligned} \tag{2.18}$$

Thus, the 11th harmonic component becomes dc, whereas fundamental and 13th harmonic components remain as ac values, but with a frequency shift of $-11\omega_s$. The dc components, $\bar{I}_{d11}$ and $\bar{I}_{q11}$ as in (2.19) are extracted by LPFs, and then transformed back to the $\alpha\beta$ reference frame.

$$\begin{aligned} \bar{I}_{d11} &= \sqrt{\tfrac{3}{2}}\,\{\hat{I}_{11} cos(\varphi_{11})\} \\ \bar{I}_{q11} &= -\sqrt{\tfrac{3}{2}}\,\{\hat{I}_{11} sin(\varphi_{11})\} \end{aligned} \tag{2.19}$$

The vectors transformed back into the $\alpha\beta$ reference frame should be corrected according to the changes in the phase and magnitude of the 11th harmonic component owing to the input filter, coupling transformer and control delay. Let the gain and the phase responses of the input filter at 11th and 13th harmonic components given by

$$\begin{aligned} \boldsymbol{G}_i(j\omega_{11}) &= \boldsymbol{G}_i(j11\omega_s) = K_{11}\angle{-\delta_{11}} \\ \boldsymbol{G}_i(j\omega_{13}) &= \boldsymbol{G}_i(j13\omega_s) = K_{13}\angle{-\delta_{13}} \end{aligned} \tag{2.20}$$

where, K_{11} and K_{13} are the amplification/attenuation factors of the input filter at 11th and 13th harmonic components with phase delays of δ_{11} and δ_{13}, respectively. The gains, K_{11} and K_{13}, may be either higher or smaller than 1.0, which depends on the design of the input filter as

described in the next chapter. The phase delays, δ_{11} and δ_{13}, also depend on the design of the input filter, but especially on the quality factor of input filter, which is determined by the input filter reactor, or the coupling transformer. Besides, let the phase delay for the 11th harmonic component due to the control delay be α_{11}, and for the 13th harmonic component, α_{13} . Also let the coupling transformer has a connection group of Dyn11, with a turns ratio of *n*.

Hence, in order to obtain correct references to be modulated, and injected by CSC, the phase delays and changes in the magnitudes should be corrected. Since the current injected by CSC is delayed while passing through the input filter, the reference current calculated from the load current should be made leading. Besides, the load current measured at the MV side should also be leading by $(\pi/6)$ in order to refer it to the secondary (LV) side. In result, the load current references for 11th harmonic component in stationary reference frame should be leading by an angle of:

$$\beta_{11} = \delta_{11} + \alpha_{11} + \frac{\pi}{6}. \tag{2.21}$$

This can easily be achieved in the $\alpha\beta$ reference frame by

$$\begin{bmatrix} I_\alpha{}' \\ I_\beta{}' \end{bmatrix} = \begin{bmatrix} cos\,\beta_{11} & sin\,\beta_{11} \\ -sin\,\beta_{11} & cos\,\beta_{11} \end{bmatrix} \begin{bmatrix} I_\alpha \\ I_\beta \end{bmatrix} \tag{2.22}$$

where $I_\alpha{}'$ and $I_\beta{}'$ are the shifted vectors by $-\beta_{11}$ with respect to the vectors, I_α and I_β. Hence, the final reference vectors in $\alpha\beta$ frame for the 11th harmonic component of the load current will be as follows:

$$\begin{bmatrix} I_{\alpha 11}{}^* \\ I_{\beta 11}{}^* \end{bmatrix} = \underbrace{\frac{n}{K_{11}} \begin{bmatrix} cos\,\beta_{11} & sin\,\beta_{11} \\ -sin\,\beta_{11} & cos\,\beta_{11} \end{bmatrix}}_{\substack{Gain\ and\ Phase\ Adjustment \\ Type\text{-}I}} \begin{bmatrix} I_{\alpha 11} \\ I_{\beta 11} \end{bmatrix} \tag{2.23}$$

where *n* is the turns ratio of the coupling transformer, and K_{11} is the amplification (or attenuation) factor of the input filter. $I^*_{\alpha 11}$ and $I^*_{\beta 11}$, in (2.23), are final reference vectors for the 11th

harmonic component. Similar equations can also be written for the 13^{th} harmonic component, provided that the employed synchronously rotating reference frame has an angular frequency of $13\omega_s$.

There is another point to note in (2.23), if K_{11} is higher than unity, the reference current to be generated by CSC will be decreased by a factor of K_{11}. This will clearly reduce the installed rating of the CSC for the same APF. K_{11} and K_{13} can be adjusted to be as higher than unity by designing the input filter using this approach, which is referred to as Selective Harmonic Amplification Method (SHAM) in this thesis.

2.3.2 Suppression of Oscillations

The LC-type input filter shown in Figure 2.1 may cause oscillations both in steady- and transient-states, especially at the frequencies around the natural frequency of the input filter. In order to damp out these oscillations caused by resonance, the quality factor, Q_0 of the filter should be low. This can be achieved by introducing a damping resistor to the LC-type input filter [30]. However, the fundamental current passing through the damping resistor results in excessive power losses. Hence, conventional damping resistor, especially for high power applications, is not a suitable method.

Many investigations have been reported to solve this problem without additional power losses, by utilizing virtual resistors [66]-[71]. The main idea of all these methods is based on the fact that the CSC is controlled in a way to inject a current component which would pass through the input filter, the same as there was a passive damping resistor in the circuit. Most of these methods are based on a closed-loop control. The advantages of the closed-loop control are good tracking of the reference, and insensitivity to the disturbances, at the expense of additional current and/or voltage measurements.

One of the main advantages of the CSC based APF is the fast and accurate ac current control in an open-loop manner without any feedback loops. This makes the control system simpler and the system stable. In [68], the active damping of the oscillations at the supply side is achieved by altering the switching pulses without any feedback loops. The main drawback of this method is that it is able to only damp the oscillations due to the converter itself, but not those originated from the power system. In [44], and [69], another active damping method

without feedback loops is proposed, in which the dynamic equations of the input filter are used. However, it is very sensitive to the parameters of the filter elements. Hence, any change in the impedance of the supply will deteriorate the performance of the active filter.

In this work, an active damping method employing a feedback loop is used to damp out these oscillations, by measuring the distorted filter currents, to construct the distorted filter inductor/capacitor voltages [37, 67].

A simple equivalent circuit representing the CSC, as an ideal current source, and the input filter at harmonic frequencies is given in Figure 2.11, by assuming that the supply voltage does not have any harmonic components. In Figure 2.11, L_f represents all the inductances in the system including transformers' leakage, and line inductances, and r_f denotes the series resistances of these inductances.

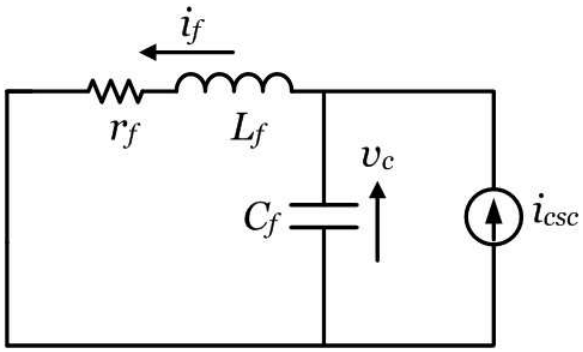


Figure 2.11: Single phase harmonic equivalent circuit of CSC and input filter

When the rms value of the CSC current, i_{csc} is denoted by I_{csc}, then the rms value of the APF current, I_f can be given by

$$I_f = I_{csc} \frac{|1/(r_s + j\omega_h L_s)|}{|1/(r_s + j\omega_h L_s) + j\omega_h C_s|} \tag{2.24}$$

where ω_h is the angular frequency of the harmonic component, that is $2\pi f_h$ rad/sec. Here, the amplification (attenuation) factor, K_h is defined as follows:

$$K_h = \frac{I_f}{Icsc}. \tag{2.25}$$

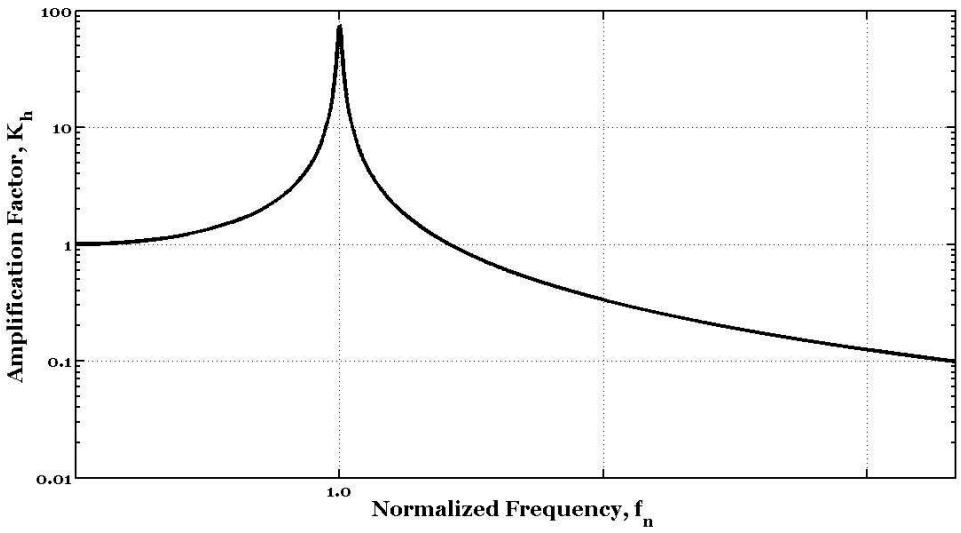


Figure 2.12: Frequency characteristics of the amplification factor, K_h for a sample system

From (2.24), K_h is given by

$$K_h = \sqrt{\frac{1}{(1 - {f_n}^2)^2 + (f_n/Q_0)^2}} \tag{2.26}$$

where,

$$f_0 = \frac{1}{2\pi\sqrt{L_f C_f}} \tag{2.27}$$

$$Q_0 = \frac{1}{R_f}\sqrt{\frac{L_f}{C_f}} \tag{2.28}$$

$$f_n = \frac{f_h}{f_0}. \tag{2.29}$$

In these expressions, f_0 is the natural or resonance frequency and, Q_0 is the quality factor of the input filter. f_n denotes the normalized frequency with respect to the natural frequency, f_0. Although it changes with the quality factor of the input filter, a sample waveform for the amplification factor, K_h with respect to f_n is as given in Figure 2.12. As it can be seen from Figure 2.12, a significant amplification is observed due to the resonance of the input filter, which occurs around the resonance frequency, that is $f_n = 1$.

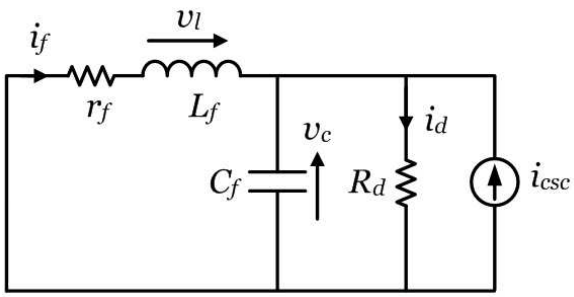


Figure 2.13: Circuit diagram showing fictitious damping resistor

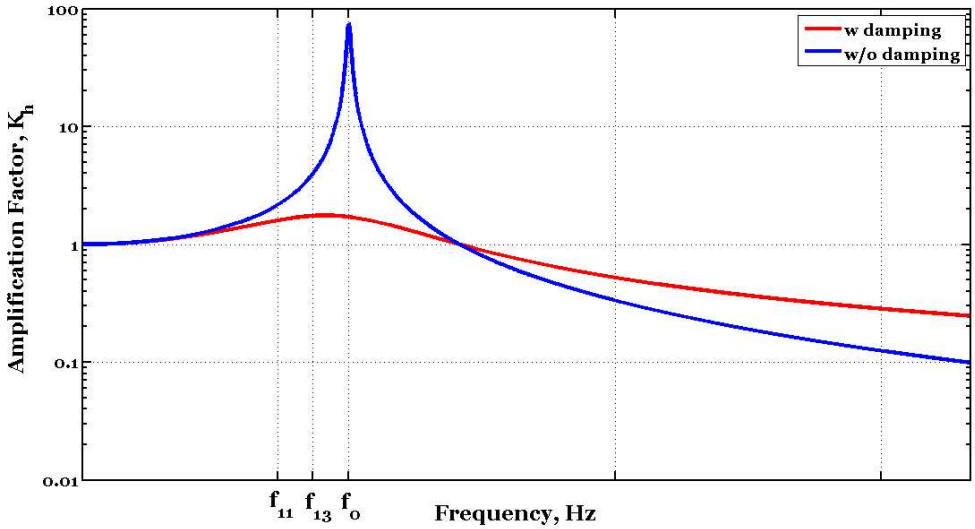


Figure 2.14: Frequency characteristics of the amplification factor, K_h for a sample system with damping resistor, R_d

A damping resistor can be connected to the circuit as shown in Figure 2.13. The damping resistor, R_d reduces the quality factor, Q_0 of the input filter, and effectively suppresses the oscillations caused by the parallel resonance of the input filter as illustrated in Figure 2.14 . The damping current, i_d can be expressed by

$$i_d = \frac{v_c}{R_d}. \tag{2.30}$$

The reference damping current can be simply obtained by detecting the harmonic voltage of the filter capacitor. Since, supply side voltage harmonics are assumed to be zero, capacitor

voltage can also be expressed by (2.31).

$$v_c = v_l = -(L_f \frac{di_f}{dt} + r_f i_f) \cdot \tag{2.31}$$

Hence, v_c or v_l can be obtained by either measuring the voltages across the capacitor/reactor, or measuring the line current of the filter reactor. However, there are some limitations on measuring the capacitor/reactor voltages. First of all, if the system has no neutral connection, which is common for three-phase, three-wire applications, line-to-neutral voltages would be unbalanced, and hence, they could not be used directly to find the reference damping current. Secondly, if the capacitor voltages are measured as line-to-line, triplen harmonics would not appear in the measured line-to-line voltages, thus oscillations occurring at triplen harmonics could not be suppressed. When there is no such an external filter inductance used in the system, leakage inductance of the coupling transformer acts as the filter inductance, L_f, as in Figure 2.11. However, it is not a physical inductance, and there is no way to measure the voltage across it. As a result, if there is no practical way to measure the voltage across either the filter capacitor, or filter reactor, line currents of the filter reactor should be used to construct the voltage across them as given in (2.31).

In this thesis, a coupling transformer is employed to connect the CSC based APF to the MV bus. For that reason, line currents of APF at the secondary side are used to construct the voltage across the filter reactor, and then, corresponding damping current reference is computed using (2.31), but ignoring the series resistor, r_f. Thus, v_l is computed by using (2.32).

$$v_l = -L_f \frac{di_f}{dt} \cdot \tag{2.32}$$

2.3.2.1 Proposed Active Damping Method for Non-selected Harmonics

In order to make the proposed SHAM applicable, the active damping method explained above should be modified. In Figure 2.14, it is seen that all of the harmonic components around the f_0 of the input filter are damped out. However, in this frequency band, there would be some harmonic components, e.g. 11^{th} and 13^{th} harmonics, to be generated by the CSC to filter out

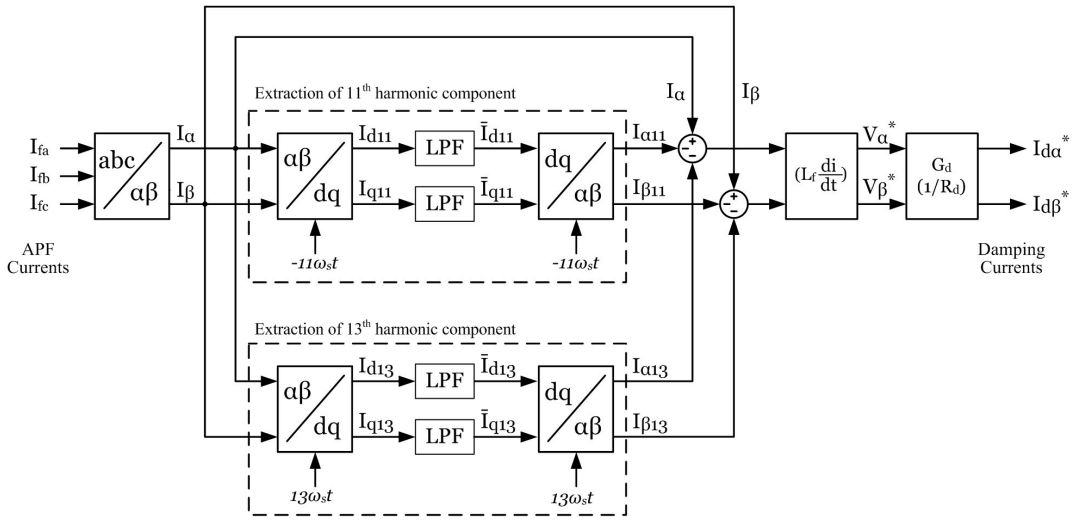


Figure 2.15: Block diagram of the proposed active damping method

the harmonic components of the non-linear load. Hence, these components would also be damped out. This would obviously result in an undesirable operation, since any attenuation at those harmonic components due to the active damping would reduce the kVA rating of APF. In order to avoid the active damping, hence attenuation, for the frequencies at which harmonic components of the load current will be eliminated, a selective harmonic extraction approach is employed as explained in this section. A block diagram illustrating the proposed active damping method for non-selected harmonics is given in Figure 2.15.

It is seen from Figure 2.15 that, 11th and 13th harmonic components of the line current of APF are extracted via SRFM. Then, the selected harmonic components are extracted from the line current in $\alpha\beta$ frame to obtain the non-selected harmonic current components to be used in active damping. Hence, there will be no 11th and 13th harmonic components in the reference current for active damping. After extracting these components, voltage vectors, V_α^* and V_β^*, are calculated by using (2.32). The reference currents for active damping are then obtained by multiplying these voltage vectors with a damping gain, G_d, which is simply equal to $1/R_d$.

2.3.3 Error Compensation

In the proposed control system, effects of the input filter and coupling transformer, in terms of magnitude and phase error, are pre-calculated, and then corrected in addition to the active

damping [37]. However, a further correction might be needed to compensate the errors arising from either the tolerances of the equipment, or the supply side impedance. For this purpose, a simple proportional controller employing the line currents of the APF, which are already measured for active damping, is used as shown in Figure 2.5.

Detailed block diagram of the error compensation is given in Figure 2.16. It is seen that error vectors, ΔI_α and ΔI_β, are calculated by using the reference currents, which are computed directly from the load current, and the line currents of the APF in $\alpha\beta$ reference frame. The fundamental component of the APF current is extracted via SRFM, because the APF current may have a significant fundamental component due to the filter capacitors, and this may result in unnecessary current reference at fundamental frequency for CSC, thus reducing the harmonic filtering capacity. The error vectors are then multiplied with a feedback gain, G_{fb}, and added to the final reference current.

The gain and phase adjustment blocks (Type-II) in Figure 2.16 are different from those (Type-I) in selective harmonic extraction circuit in Figure 2.10. The gain and phase adjustment blocks in Figure 2.16 are used only to refer the load currents to the secondary side. Since line currents of the APF are used in error compensation, phase and magnitude adjustment due to neither the input filter nor the control delay is required. Hence, ${I_{\alpha 11}}^*$ and ${I_{\beta 11}}^*$ can be expressed in terms of $I_{\alpha 11}$ and $I_{\beta 11}$ as given in (2.33).

$$\begin{bmatrix} {I_{\alpha 11}}^* \\ {I_{\beta 11}}^* \end{bmatrix} = \underbrace{n \cdot \begin{bmatrix} cos\,(\frac{\pi}{6}) & sin\,(\frac{\pi}{6}) \\ -sin\,(\frac{\pi}{6}) & cos\,(\frac{\pi}{6}) \end{bmatrix}}_{\substack{\textit{Gain and Phase Adjustment} \\ \textit{Type-II}}} \begin{bmatrix} I_{\alpha 11} \\ I_{\beta 11} \end{bmatrix}. \tag{2.33}$$

2.3.4 PQ Control

The PQ controller shown in Figure 2.5 is mainly responsible for controlling the fundamental current drawn by the APF. Direct and quadrature components of the fundamental current of the APF correspond to active and reactive powers, respectively. Active power is controlled to compensate the losses of the semiconductor devices, and the dc-link reactor for keeping the dc-link current at its design value. On the other hand, reactive power is controlled in order to

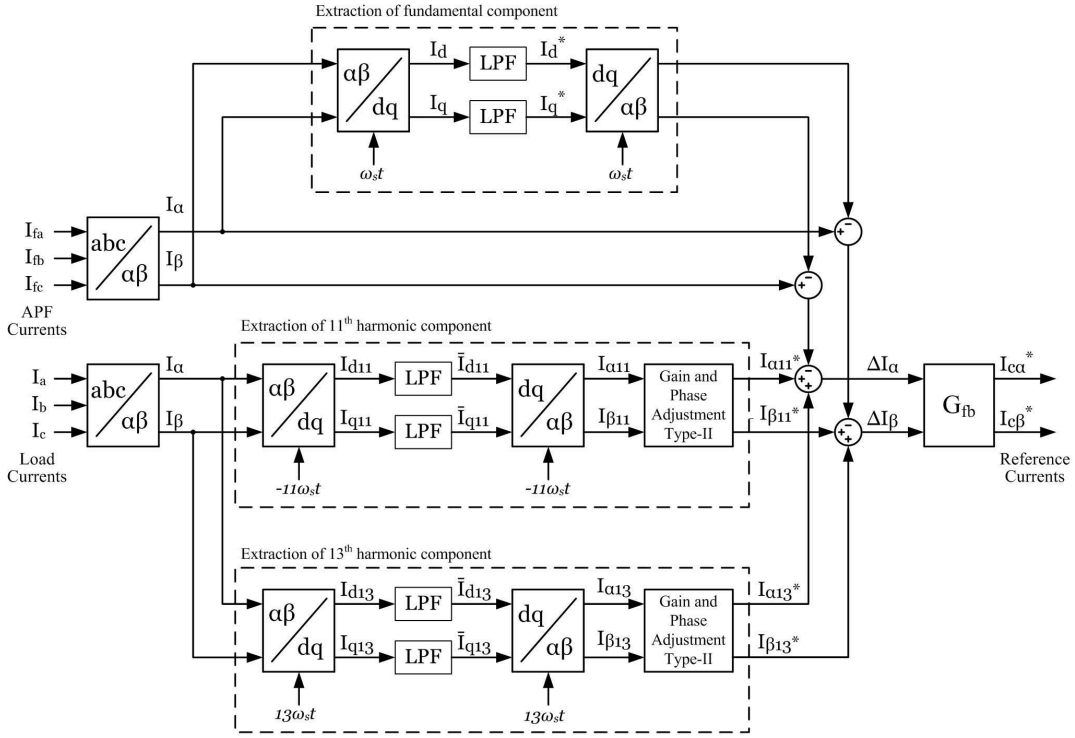


Figure 2.16: Block diagram of the error compensation circuit

avoid the APF from injecting reactive power into the network; or to compensate the reactive power of the non-linear load.

2.3.4.1 Reactive Power Control

The reactive power at the output of the APF is controlled via the quadrature component of the line current of APF in the *dq* reference frame, which is rotating at an angular frequency of ω_s. There are two reasons for controlling the reactive power : (i) compensating the reactive power of the input filter capacitor for unity power factor operation ii) or compensating the reactive power of the non-linear load.

The direct, and quadrature components of the filter capacitor current vector in the synchronous reference frame are given by (2.34), and (2.35), respectively [23].

$$i_{Cf_d} = C_f \frac{dv_d}{dt} - \omega_s C_f v_q \tag{2.34}$$

$$i_{Cf_q} = C_f \frac{dv_q}{dt} + \omega_s C_f v_d. \tag{2.35}$$

Since the quadrature voltage vector, v_q is zero, and direct voltage vector, v_d is almost constant for balanced, symmetrical and sinusoidal supply voltages, the capacitive current can be expressed by the last term in (2.35). Hence, the reference current to compensate for the capacitive reactive power of the input filter capacitor is given by (2.36).

$$i_q{}^* = -\omega_s C_f v_d. \tag{2.36}$$

It is worth to note that v_d is the voltage vector referred to the secondary side of the coupling transformer. Hence, there is no need for an extra measurement of the capacitor, or bus voltage at secondary side.

In order to compensate for the reactive current of the load, the quadrature component of the load current in dq reference frame rotating at ω_s should be obtained by SRFM. For this purpose, one more SRFM loop should be employed in addition to those in Figure 2.10 for current components at fundamental frequency. The block diagram showing the reference vector generation for the PQ control is given in Figure 2.17. The gain and phase adjustment block in Figure 2.17 is used to transform the load currents to the secondary of the coupling transformer. Since references are at fundamental frequency, phase and magnitude adjustment due to the input filter is not required.

2.3.4.2 DC-link Current Control

In CSC based APF, the dc-link current is kept at its design value by controlling the active power drawn by APF with the direct component of the compensating current vector [23]. A block diagram of the dc-link current control is given in Figure 2.18. The dc-link control is implemented in a closed-loop manner with a PI type controller. The error value, ΔI_{dc} for PI controller is calculated by subtracting the dc-link current, I_{dc} from its reference value, $I_{dc}{}^*$. A first-order is filter is used to reduce the ripple of the current feedback signal as shown in Figure 2.18. The output of the PI controller, $v_{dc}{}^*$ is the reference voltage for the converter. The reference value for the direct component of the compensating current is given in [44] as follows:

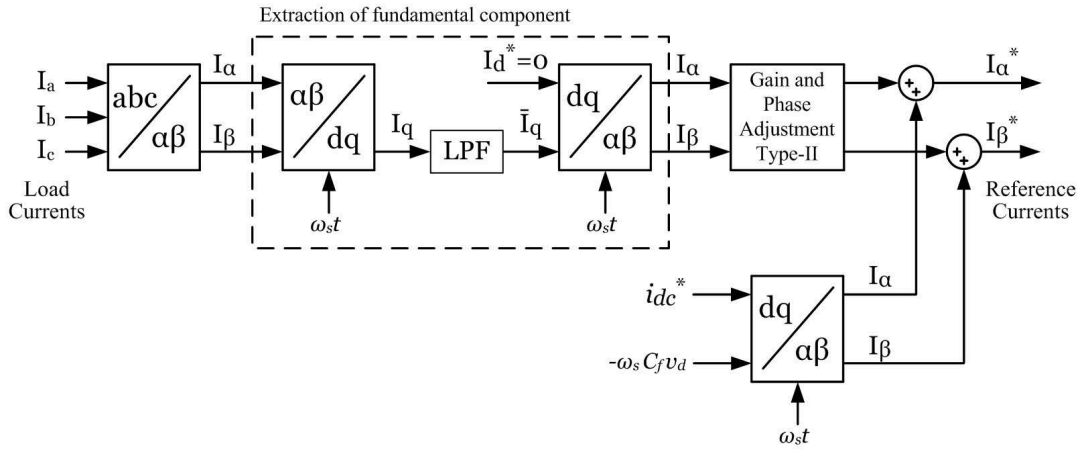


Figure 2.17: Block diagram of the PQ control

$$i_d{}^* = \frac{v_{dc}{}^* i_{dc}}{v_d} \tag{2.37}$$

where v_d is the direct component of the supply voltage referred to the secondary side of the coupling transformer. The reference current, $i_d{}^*$ is then transformed back to the stationary reference frame, and added to the final reference vectors.

Since the response of the system is slower than that of the ac control loop, dc control loop can be analyzed separately, assuming that ac control loop is ideal [24, 37, 70]. From Figure 2.18, the transfer function of the dc side current control is obtained as follows [39]:

$$\frac{i_{dc}}{i_{dc}^*} = \frac{s^2 T_f K_p + s(T_f K_i + K_p) + K_i}{s^3 L_{dc} T_f + s^2(L_{dc} + T_f r_{dc}) + s(K_p r_{dc}) + K_i} \tag{2.38}$$

where K_p and K_i are gains of the proportional and integral parts of the PI type controller, respectively; and T_f is the time constant of the first-order filter. The values, L_{dc}, and r_{dc} are the inductance and resistance of the dc-side circuit, respectively.

In order to reduce the order of the transfer function, the parameters of the PI controller should satisfy the relationship in (2.39).

$$\frac{K_p}{K_i} = \frac{L_{dc}}{r_{dc}}. \tag{2.39}$$

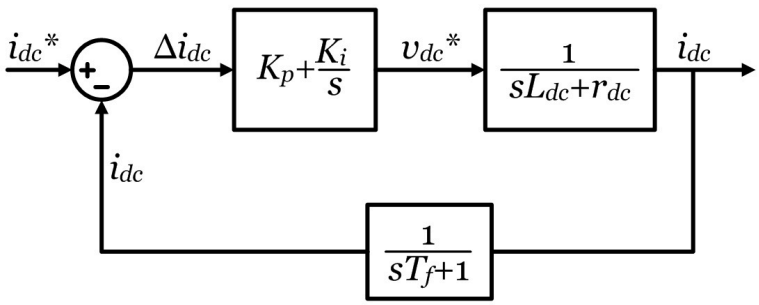


Figure 2.18: Block diagram of the dc-link current control

Then, the transfer function in (2.38) reduces to one in (2.40).

$$\frac{i_{dc}}{i_{dc}^*} = \frac{sT_f + 1}{s^2\frac{T_f r_{dc}}{K_i} + s\frac{r_{dc}}{K_i} + 1}. \tag{2.40}$$

The ITAE (the integral of time multiplied by the absolute value of error) optimum transfer function for a second-order system with zero response is given in [39] as follows:

$$G_{opt}(s) = \frac{1}{s^2\frac{1}{\omega_{ndc}^2} + s\frac{1.4}{\omega_{ndc}} + 1} \tag{2.41}$$

where ω_{ndc} is the cut-off frequency of the closed-loop response in rad/sec. Hence, the parameters of the PI controller and the first-order filter can be found as follows:

$$K_p = \frac{L_{dc}\omega_{ndc}}{1.4} \tag{2.42}$$

$$K_i = \frac{r_{dc}\omega_{ndc}}{1.4} \tag{2.43}$$

$$T_f = \frac{1}{1.4\omega_{ndc}} \tag{2.44}$$

2.3.5 Overall System

After presenting its sub-blocks, block diagram of the overall reference current generation circuit is as given in Figure 2.19. It is seen that all the reference currents for each specific job

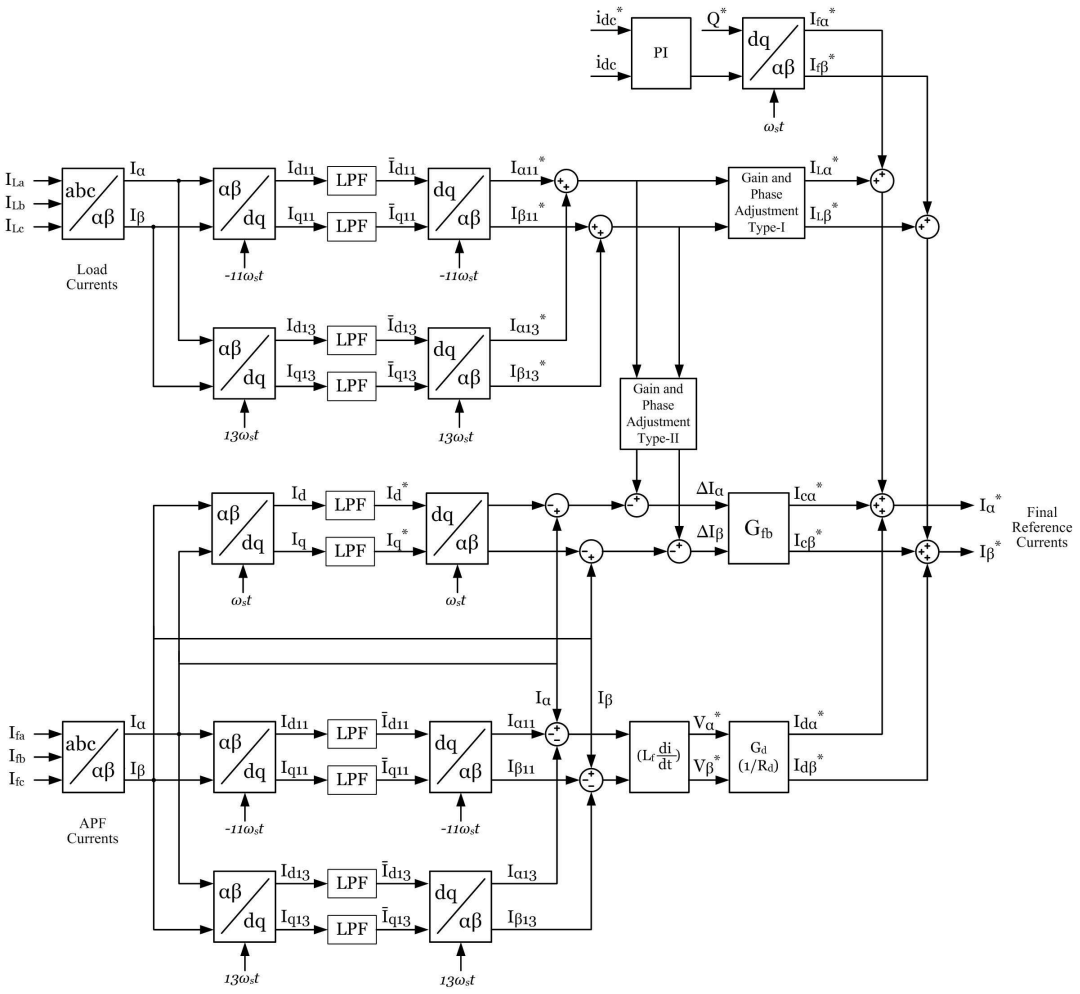


Figure 2.19: Block diagram of the overall reference current generation circuit

are summed in the $\alpha\beta$ reference frame to obtain the final reference current, which are going to be modulated after the transformation back into the *abc* frame.

2.4 Waveform Modulation

VSCs are being widely used in industry for various applications. Therefore, many Pulse Width Modulation (PWM) methods for VSCs have been developed, and evaluated to satisfy the requirements in terms of harmonic reduction, switching frequency, and controllability [72]-[75].

Different PWM techniques, either introduced specially for CSCs, or derived from those ini-

tially proposed for VSCs, have been studied for CSCs [31],[37],[77]-[81]. These methods can be simply analyzed in two groups: (i) off-line pattern generation methods, (ii) on-line pattern generation methods. Off-line pattern generation methods [30], [77]-[81] simplify the generation of the gate patterns, and the application of the special requirements arising from the forced-commutated, uni-directional switches in CSCs. On the other hand, on-line pattern generation methods offer a number of advantages compared to the off-line methods such as faster dynamic response, continuous and precise control of the ac current, but usually at the expense of higher switching losses [34, 36]. The most common on-line pattern generation methods are the Sinusoidal PWM (SPWM), with its variants [34, 36, 42, 83, 84], and Space Vector PWM (SVPWM) [42, 43, 82, 85].

CSC is the dual of VSC [76], hence the following requirements should be met at any time:

- The dc bus is of current source type, and therefore, it can not be opened. Thus, at least one top and one bottom switch should be necessarily conducting at any time.

- The ac side current is a chopped waveform, hence there should be a capacitor at the ac side, and it should not be short-circuited. Therefore, it also imposes that just one top switch, and one bottom switch should be conducting.

In order to meet the requirements above, switching signals of the power semiconductors in Figure 2.20 should be as given in (2.45).

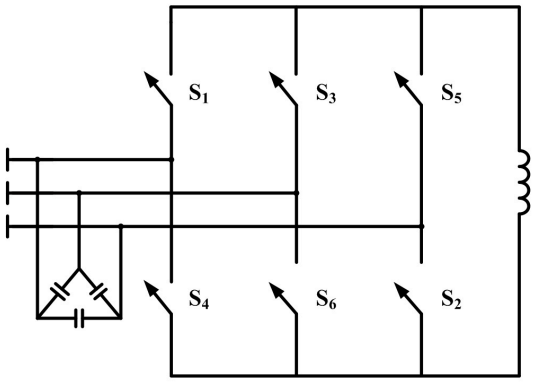


Figure 2.20: CSC with six uni-directional current carrying switches

$$\begin{aligned} m_{S_1} + m_{S_3} + m_{S_5} &= 1 \\ m_{S_2} + m_{S_4} + m_{S_6} &= 1 \end{aligned} \tag{2.45}$$

where ($m_{S_i} = 1$) and ($m_{S_i} = 0$) denote that the switch S_i is ON, and OFF, respectively.

Carrier-based PWM methods, or SPWM with its variants, provide a simple control algorithm as compared to SVPWM methods with nearly the same performances. As in VSCs, many methods have been applied to SPWM for CSCs in order to increase the ac gain of the converter, and to decrease the switching frequency with reduced line harmonics. To decrease the effective switching frequency of the semiconductor devices for the same carrier frequency, dead-band PWM techniques, which were commonly used in VSCs [86], have been adapted to CSCs [42], [84]. With these methods, the ac gain of the converter is made unity with an effective switching frequency, which is half of the carrier frequency. In [84], a Dead-Band SPWM (DSPWM) technique is applied to CSCs, which result in an effective switching frequency, f_{sw} equal to the 2/3 of the carrier frequency, f_{cr}. In [42], a Modified DSPWM (MDSPWM), with a sawtooth carrier, has been introduced, which decreases the f_{sw} down to almost half of the f_{cr}.

In digital control systems employed for VSCs, SVPWM is the most attractive method for generating the gate patterns. Because, it provides the direct application of the enhanced control systems (both in stationary and synchronous reference frames) with straightforward implementation in digital systems. The SVPWM methods used for CSCs are adapted from those originated for VSCs [42, 43, 85]. Unlike VSC, CSC has nine valid conduction states as shown in Table 2.1 and Figure 2.21, thus introduces the advantage of the extra zero vector.

The SPWM [36], DSPWM [84], MDSPWM [42], and SVPWM [85, 42] techniques are compared in Table 2.2. Figures 2.22-2.24 show the corresponding modulating waveforms, carrier waveforms, switching signals, and the harmonic spectra for DSPWM, MDSPWM and SVPWM techniques.

It is seen from Table 2.2 and Figures 2.22-2.24 that MDSPWM has a similar performance with the SVPWM in view of effective switching frequency, and harmonic spectra. However, in these two techniques, the magnitudes of the lower order harmonics are higher than those of DSPWM, and tend to increase with low modulation indices [88, 42]. In order to keep the

Table 2.1: Switching states of the CSC with corresponding normalized line currents

State	ON Switches	i_a/i_{dc}	i_b/i_{dc}	i_c/i_{dc}
1	1, 2	1	0	-1
2	2, 3	0	1	-1
3	3, 4	-1	1	0
4	4, 5	-1	0	1
5	5, 6	0	-1	1
6	6, 1	1	-1	0
7	1, 4	0	0	0
8	3, 5	0	0	0
9	5, 2	0	0	0

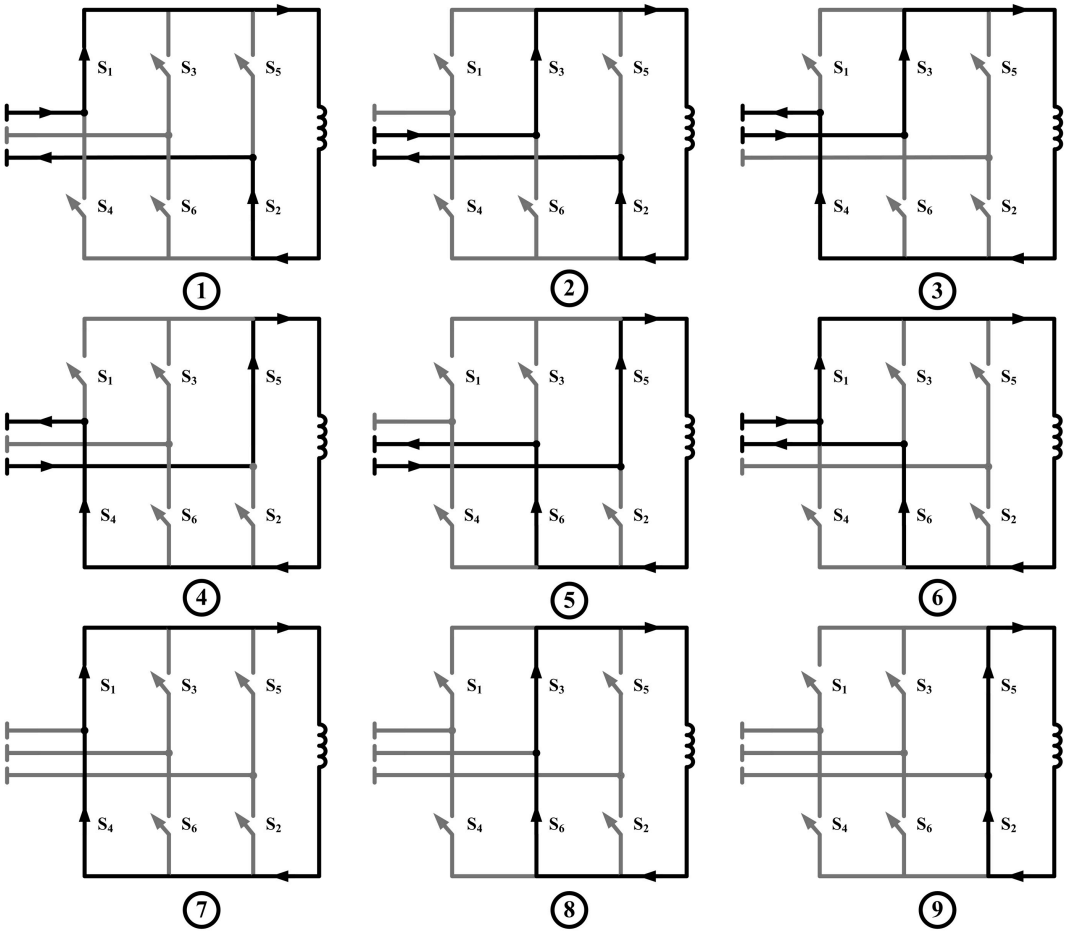


Figure 2.21: Nine conduction states of the CSC

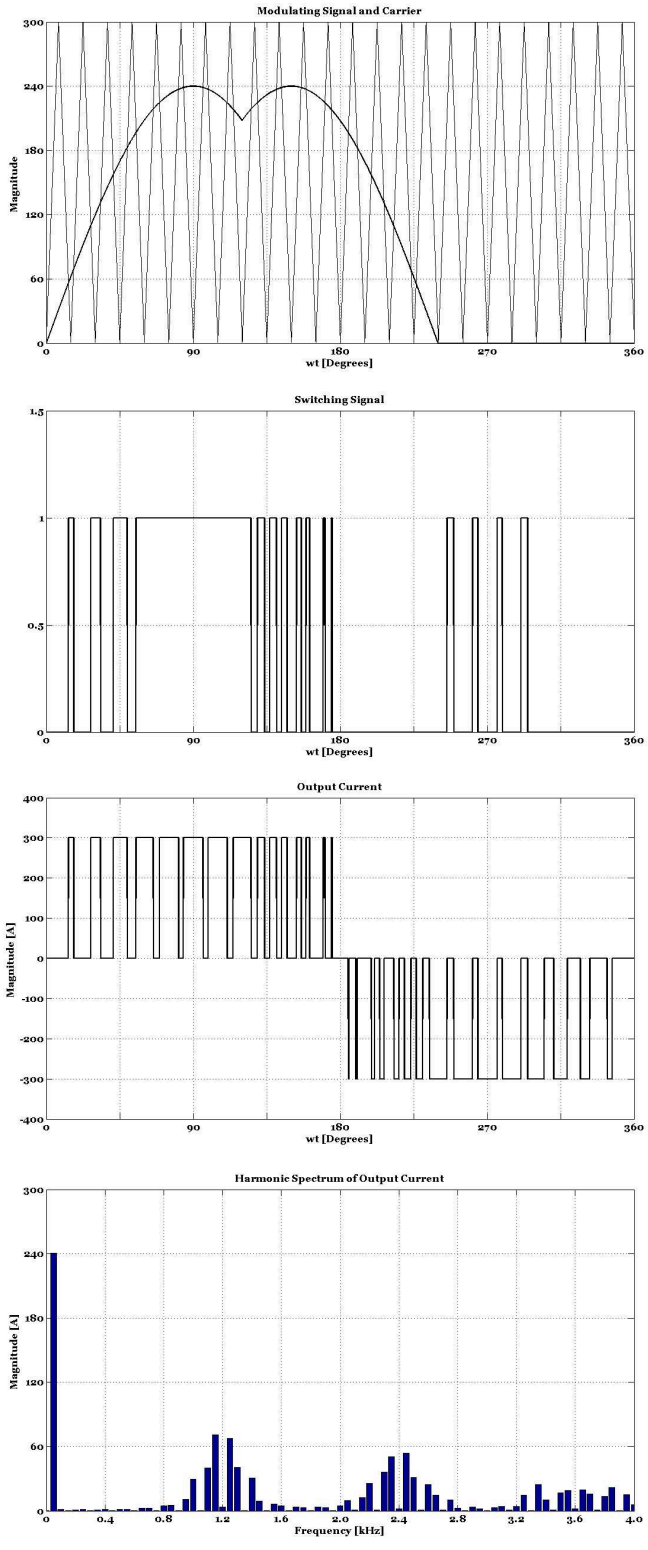


Figure 2.22: Modulating waveform, switching signal of S1, output current waveform and its harmonic spectrum for DSPWM (f_{cr} = 1.2kHz, modulation index, M=0.8)

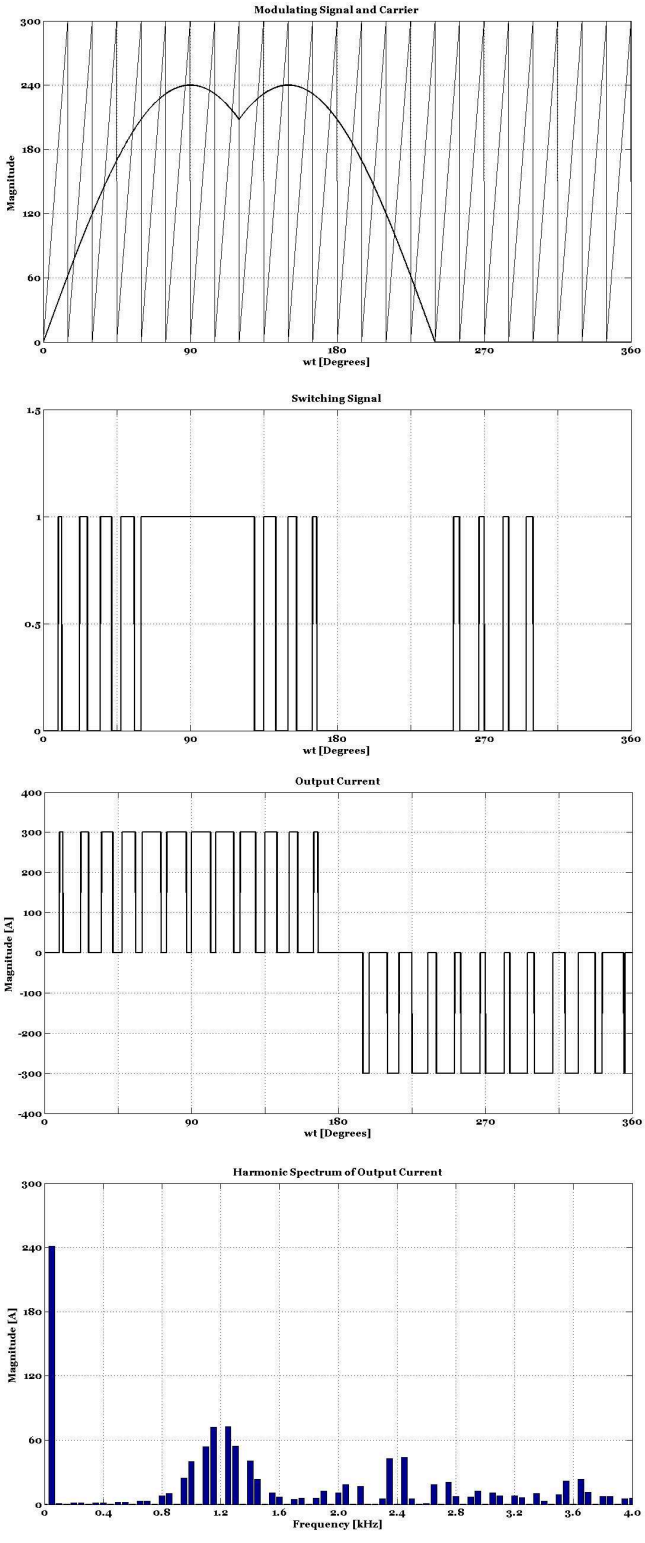


Figure 2.23: Modulating waveform, switching signal of S1, output current waveform and its harmonic spectrum for MDSPWM (f_{cr} = 1.2kHz, modulation index, M=0.8)

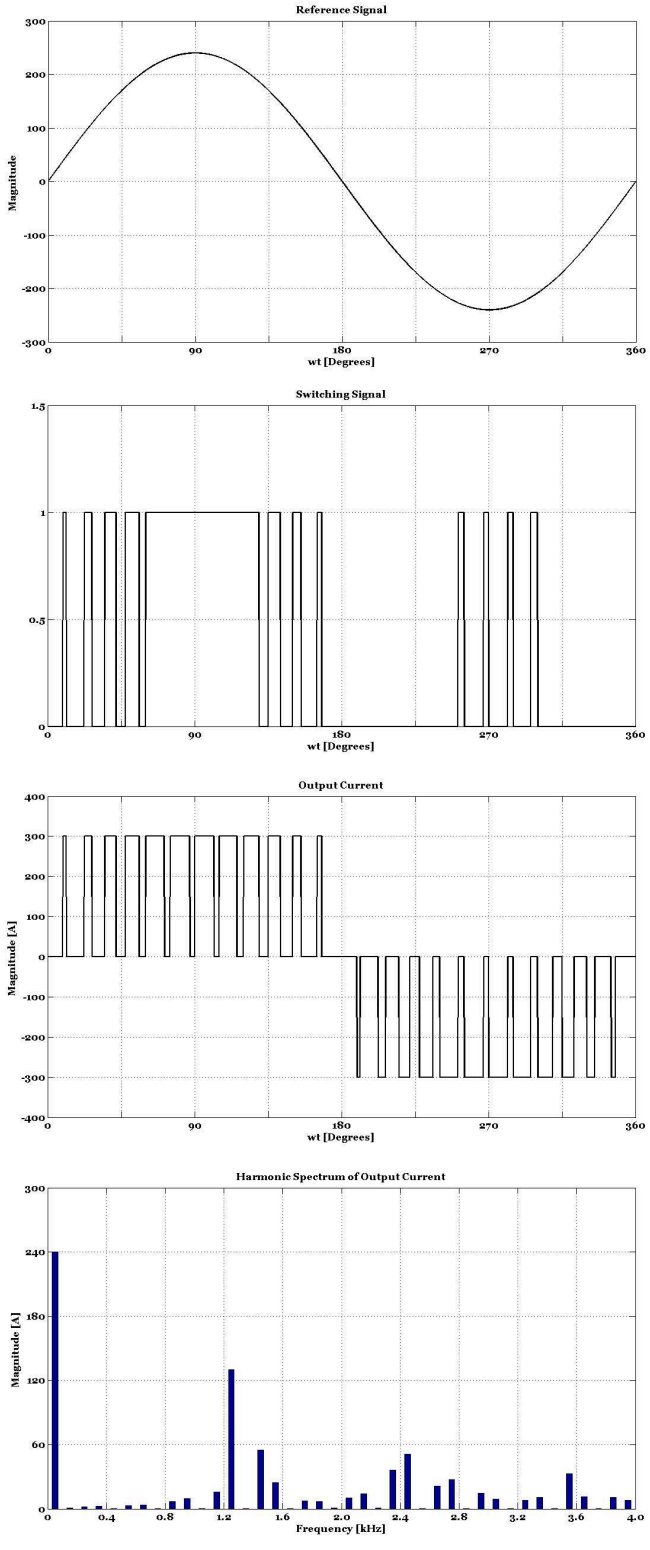


Figure 2.24: Reference current waveform, switching signal of S1, output current waveform and its harmonic spectrum for SVPWM (f_{cycle} = 1.2kHz, modulation index, M=0.8)

Table 2.2: Comparison of on-line PWM methods applicable to CSCs

Technique	Category	Switc. Freq.	Ac gain
SPWM	Analog	$\frac{2}{3} f_{cr}$	0.866
DSPWM	Analog	$\frac{2}{3} f_{cr}$	1.000
MDSPWM	Analog	$\frac{1}{2} f_{cr}$	1.000
SVPWM	Digital	$\frac{1}{2} f_{cyc}$	1.000

lower order harmonics at minimum, and avoid the oscillations due to the input filter at those frequencies, DSPWM was chosen as the waveform modulator. Two sample cases showing the modulation of a reference current consisting of 11^{th} and 13^{th} harmonic components for DSPWM (triangular carrier) and MDSPWM (sawtooth carrier) are given in Figure 2.25. As it is seen that, lower order harmonics are reduced significantly for DSPWM case, but at the expense of slightly increased switching losses. Although, DSPWM is well suited for analog applications with a free-running carrier signal, it is chosen as the waveform modulation, or pattern generation, method in this thesis due to its ease of application even in a digital control system, which consists of only addition and multiplication operands.

2.4.1 Dead-Band Sinusoidal PWM (DSPWM)

The basic block diagram of the Dead-Band SPWM (DSPWM) is given in Figure 2.26 [42, 84]. It has four fundamental blocks: Decoupling block, dead-band or modulating waveform generation block, tri-logic gating signals generator block, and shorting pulse generator block.

The main purpose of the PWM is to produce gating signals of the semiconductor switches (S1,S2,...,S6), which applied to CSC currents that track the given reference vectors. If the purpose of the pattern generator is attained, CSC acts as a current amplifier, and characterized by:

$$[i_{csc}]_{abc} = G_{ac}\,[i_n]_{abc}\,i_{dc} \tag{2.46}$$

where G_{ac} is the ac gain of the converter, $[i_{csc}]_{abc}$ is the actual line currents in *abc* reference

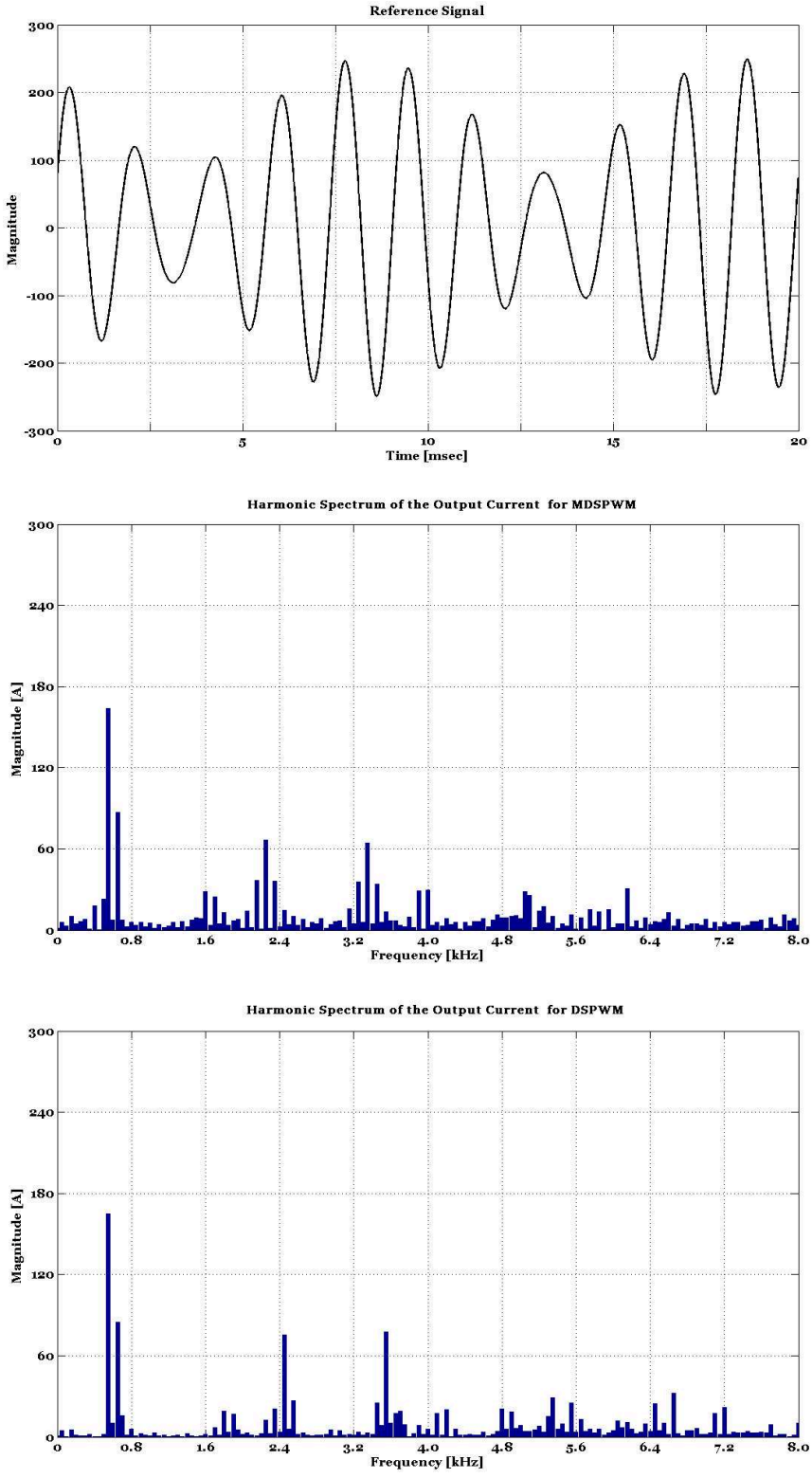


Figure 2.25: Reference current waveform, and harmonic spectra of the output currents for MDSPWM and DSPWM (f_{cr} = 3.0kHz)

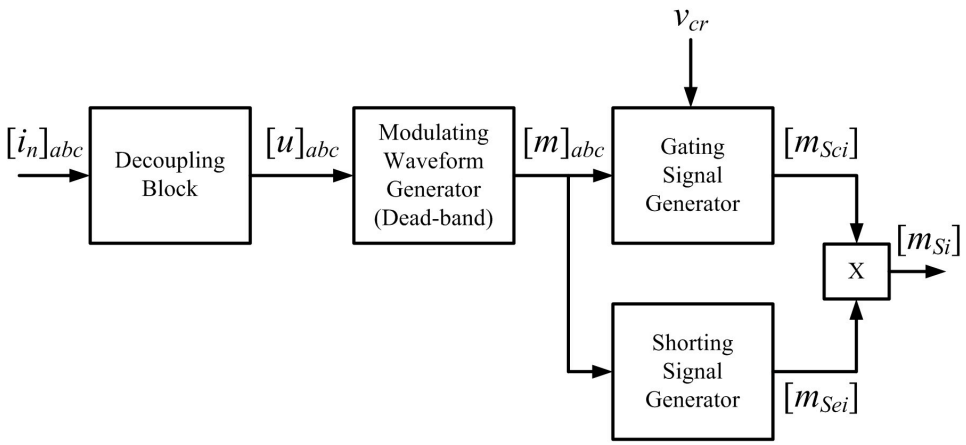


Figure 2.26: Block diagram of the DSPWM method

frame, $[i_n]_{abc}$ is the normalized reference current vectors, and i_{dc} is the dc-link current.

As seen from Figure 2.26 that modulating waveforms, $[m_i]^T$ are compared with a carrier signal, v_c, which is a triangular carrier, to generate the gating signals ($m_{S_1}, m_{S_2}, ..., m_{S_6}$). Hence, the bilogic gating signals should be converted to trilogic signals for applying them to the CSC [83]. The bilogic gate signals for $[m_i]^T$ and v_c are given by

$$X_i = \begin{cases} 1, & \text{if } m_i > v_c \\ -1, & \text{otherwise} \end{cases} \qquad i = 1, 2, 3 \tag{2.47}$$

where $X_i = 1$, and $X_i = -1$ are given for that the upper switch is ON, and the lower switch is OFF, and vice versa, respectively. However, CSC has nine switching states, three for each leg as given in Table 2.1. The line current of the converter can be expressed in terms of the dc-link current for each phase as follows:

$$[i]_{abc} = [Y]_{abc} \cdot i_{dc} \tag{2.48}$$

where Y_{abc} has three possible values: +1, 0, -1. In the first 6 states, dc-link current flows through one ac line, and returns through another. However, in last three states, ac lines do not carry the dc-link current, and it circulates through one of the legs.

Table 2.3: Truth table of the bilogic to trilogic translation for (+1,-1) bilogic signals

Bilogic Signals			Trilogic Signals			State
X1	X2	X3	Y1	Y2	Y3	
-1	-1	-1	0	0	0	7,8,9
-1	-1	+1	0	-1	+1	5
-1	+1	-1	-1	+1	0	3
-1	+1	+1	-1	0	+1	4
+1	-1	-1	+1	0	-1	1
+1	-1	+1	+1	-1	0	6
+1	+1	-1	0	+1	-1	2
+1	+1	+1	0	0	0	7,8,9

The bilogic PWM signals, which have values of +1 or -1, can be translated to trilogic signals with linear mapping by

$$\begin{bmatrix} Y_a \\ Y_b \\ Y_c \end{bmatrix} = \frac{1}{2}\,[C] \begin{bmatrix} X_1 \\ X_2 \\ X_3 \end{bmatrix} \tag{2.49}$$

where

$$[C] = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \tag{2.50}$$

Table 2.3 shows the eight bilogic PWM signals with their corresponding trilogic signals. Trilogic PWM variables meets the requirements for the operation of CSC, which is that one upper and one lower switch can conduct simultaneously at any time.

If the bilogic signals defined as (1 or 0) rather than (+1, -1), Table 2.3 then can be revised as in Table 2.4. Hence, the intermediate gating signals, ($m_{S_{c1}}, m_{S_{c2}}, ..., m_{S_{c6}}$) can be expressed by bilogic signals using the Table 2.4 as in (2.51).

$$\begin{aligned} ms_1 &= x_1\bar{x_2}, \quad ms_3 = x_2\bar{x_3}, \quad ms_5 = x_3\bar{x_1} \\ ms_2 &= x_1\bar{x_3}, \quad ms_4 = x_2\bar{x_1}, \quad ms_6 = x_3\bar{x_2} \end{aligned} \tag{2.51}$$

Table 2.4: Truth table of the bilogic to trilogic translation for (1,0) bilogic signals

Bilogic Signals			Trilogic Signals			State
X1	X2	X3	Y1	Y2	Y3	
0	0	0	0	0	0	7,8,9
0	0	1	0	-1	+1	5
0	1	0	-1	+1	0	3
0	1	1	-1	0	+1	4
1	0	0	+1	0	-1	1
1	0	1	+1	-1	0	6
1	1	0	0	+1	-1	2
1	1	1	0	0	0	7,8,9

where x_i denotes "1", and $\overline{x_i}$ denotes "0" for bilogic signals.

Generation of the bilogic signals from $[m_i]^T$, and v_c, and the translation from bilogic to trilogic signals can easily be achieved by using analog circuits, which correspond to (2.51), as given in Figure A.1.

In order to apply these intermediate gating signals to the CSC, shorting pulses should be generated to make sure that the dc-link current is never discontinued. For this purpose, shorting pulse generator with a distributor for equal loading between phases is employed by using the modulating waveform and trilogic signals. According to the modulating waveforms, the leg, which will carry the current in that zero state, is determined as in the SPWM adapted to the CSCs [36] as. The instants, at which the shorting pulses will be applied, is determined by the trilogic intermediate signals ($m_{S_{c1}}, m_{S_{c2}}, ..., m_{S_{c6}}$). If all of the trilogic intermediate signals are zero, a shorting pulse is generated to keep the dc-link current continuous. An equivalent analog circuit of the shorting pulse generator is given in Figure A.2.

Since the converter is connected as delta, a decoupling block is required to control converter currents by line-to-neutral signals. The expression in (2.52) can be re-written as follows:

$$[i_{csc}]_{abc} = \frac{G_{ac}}{\sqrt{3}v_c} \mathrm{T}\,[u]_{abc}\, i_{dc} \tag{2.52}$$

where

$$[T] = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \tag{2.53}$$

The decoupling block is modeled as a linear transformation by

$$[u]_{abc} = \mathrm{D}\,[i_n]_{abc} \tag{2.54}$$

which yields to

$$[i_{csc}]_{abc} = \frac{G_{ac}}{\sqrt{3}v_c}\mathrm{TD}\,[i_n]_{abc}\, i_{dc} \tag{2.55}$$

Since the determinant of the T is zero, D is chosen to be equal to $[\mathrm{T}]^T$, thus resulting in

$$[i_{csc}]_{abc} = \frac{G_{ac}}{v_c}\,[i_n]_{abc}\, i_{dc} \tag{2.56}$$

Equation (2.56) shows that, line currents of the converter is controlled by normalized reference currents in a linear and decoupled fashion.

The last stage is the modulating waveform generator, or dead-band block. In order to reduce the effective switching frequency of the semiconductor devices, a dead-band is introduced in the modulating waveform. In this band, since the modulating waveform is zero, the top or bottom switch associated with the corresponding modulating waveform will be kept at its previous state, thus there will be no switching. There are many ways to generate dead-bands in the modulating waveforms [86]. In this work, a simple way is chosen as given in Figure A.3, which is represented by the equivalent analog implementation.

If the bilogic signals are given as (1,0), then the overall pattern generation circuit can be shown as in Figure A.4. This process, which is represented as an analog circuit, can easily be implemented in a digital control system as given in Appendix B.

2.5 Summary

In this chapter, the system description and operation principles of a shunt connected CSC based APF have been presented in order to satisfy the following three main objectives:

- filtering of the some pre-selected harmonic components of a non-linear load
- generating corresponding reference current vectors, and injecting them to the network via a coupling transformer
- damping the oscillations due to the parallel resonance of the input filter

It has been demonstrated that there are two major parts in the control system of the CSC based APF: reference current generation, and waveform modulation. Reference current generation consists of not only the generation of the reference current vectors in order to filter out the load current harmonics, but also the generation of the reference current vectors, which are being used to suppress the oscillations due to the input filter, and to control the active/reactive power flow. Waveform modulation is used to generate the gating signals of the semiconductor devices, so that the CSC currents can track the reference current vectors.

It has been noticed that, in most of the cases, it is sufficient to filter out some dominant harmonic components in order to comply with the IEEE Std. 519-1992. For this purpose, a selective harmonic extraction technique via SRFM has been demonstrated to extract these harmonic components of the load current. It has been shown that any one of the harmonic components can be extracted from the line currents of the load via SRFM, in which a synchronously rotating reference frame is employed for each harmonic component. For each harmonic component, synchronously rotating fame has an angular frequency which is identical to the frequency of the corresponding harmonic component. By this way, the harmonic current component at that frequency become dc, and it can be filtered out by a LPF without any phase delay. However, for this operation, a correct phase angle information of the supply is required. For this purpose, a simple but robust PLL has been demonstrated. In addition to this, necessary corrections arising from the input filter and the coupling transformer have been emphasized; and the required calculations have been demonstrated to adjust the reference current obtained from the line current of the load, which is measured from MV level.

Since the LC-type input filter introduces unavoidable oscillations around its natural frequency, suppression of these oscillations has been discussed, and a modified active damping method has been proposed. APF has harmonic components injected by the CSC to filter out the load harmonics, in addition to the undesired harmonic components arising from the input filter, and PWM. Hence, these harmonic components are also subject to be attenuated by the active damping method proposed. For this purpose, a selective harmonic extraction based active damping method has been demonstrated. By this method, the harmonic components very close to the natural frequency of the input filter, are extracted from the reference current being used for the active damping. The attenuation of these harmonic components is therefore avoided, and the rating of the CSC is not reduced.

Although the CSC based APF is operated in an open-loop manner to eliminate the load current harmonics, a feedback loop for compensating the error at the output current of the APF has been also presented. This feedback loop compensates the errors arising from the tolerances of the equipment, uncertain system impedance, and the control system delays. Since the CSC based APF can also be used as a reactive power compensation unit, again a selective harmonic extraction method has been employed to extract the fundamental component of the APF current from the reference current vector used in the error compensation control loop.

A PQ controller, which is used to control the active and reactive power flow, has also been demonstrated. Since the dc-link current of the CSC is usually kept constant in APF applications, the losses in the converter and the dc-link reactor should be supplied from the network to achieve this task. For this purpose, a control loop has been presented to keep the dc-link current at its design value by controlling the active component of the current at fundamental frequency. Besides, if the APF is used also to compensate the reactive power of the load, or that of the input filter capacitors, reactive current components should be added to the reference current vector of the CSC. To achieve this, a simple reactive power controller has been given in synchronously rotating reference frame.

Another important part of the control system employed in the CSC based APF is the waveform modulation because, with an effective waveform modulation technique, CSC current can track its reference precisely with lower switching frequencies, and lower harmonic distortions. Various waveform modulation, or simply pattern generation, methods have been discussed, and among these, appropriate ones for CSCs have been compared. Since APF ap-

plications require fast transient response, on-line pattern generation methods are well suited rather than the off-line methods such as Selective Harmonic Elimination Method (SHEM), which is very common in CSC based rectifiers, and STATCOMs. On-line pattern generators, which are applicable to CSCs, have been examined, and compared in view of effective switching frequency, and harmonic spectra. Among them, Dead-band Sinusoidal PWM (DSPWM), which is used in this work, has been demonstrated in detail. It has been shown that DSPWM provides a good performance with the ease of application both in analog and digital control systems.

CHAPTER 3

PROPOSED SELECTIVE HARMONIC AMPLIFICATION METHOD (SHAM)

3.1 Introduction

As described in Chapter 2, the reference current vectors for the CSC are obtained by employing the selective harmonic extraction method. By this way, any pre-selected harmonic component of the load current can be extracted. This provides two main advantages:

- Any gain and phase adjustment, arising from the input filter characteristics, transformer connection or control delay, can be done easily for each harmonic component in a decoupled manner.
- Different filtering gains for each harmonic component can be employed to comply with the IEEE Std.519-1992.

The first item is the main idea behind SHAM. If the input filter has an amplification property, or gains higher than unity at some selected harmonic frequencies, the APF currents at those frequencies will be obviously higher than CSC currents. In order to make the SHAM applicable, a new active damping method has also been proposed, in which the attenuation of the selected harmonic components due to the active damping is avoided by employing the selective harmonic extraction method, as explained in Chapter 2. By this way, the harmonic current components at selected frequencies are extracted from the reference current to be used in active damping, and the amplification property of the input filter at those frequencies is kept unchanged.

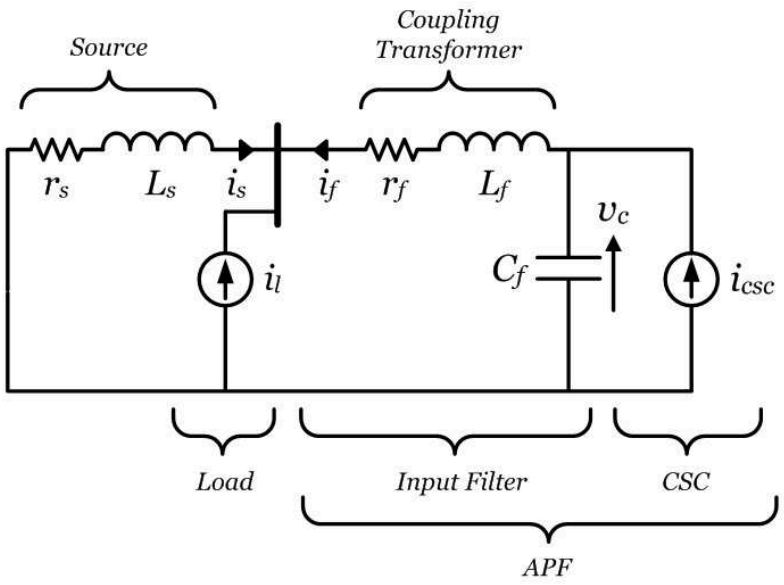


Figure 3.1: Single phase harmonic equivalent of overall system

In this chapter, the proposed SHAM will be explained on an example to eliminate the 11th and 13th current harmonics of a non-linear load. Harmonic equivalent circuit of the overall system is as given in Figure 3.1 on per-phase-wye basis. For the sake of simplicity in the design, supply voltage is assumed to be purely sinusoidal at fundamental frequency. The non-linear load injects 11th and 13th current harmonics into the supply, thereby an ideal APF should generate 11th and 13th harmonics of the same magnitude, and in anti-phase with the load harmonics. This is achieved firstly by generating 11th and 13th harmonics in CSC current, i_{csc}, with magnitudes lower than those needed for ideal harmonic cancelation, and then rising them to the required levels by using the inherent amplification property of the input filter. In other words, selected harmonic currents of APF are higher in magnitude than those produced by CSC. This approach, in the design of control system and input filter, thus reduces the installed kVA rating of the CSC, significantly.

The transfer function of the input filter is as given in (2.26) under the assumption that $L_s \ll L_f$, and $r_s \ll r_f$. Figure 3.2 shows the gain response of a sample input filter where K_{11} and K_{13} are the amplification factors of the input filter at f_{11} = 550 Hz and f_{13} = 650 Hz, respectively. K_{cr} is the gain of the input filter at the carrier frequency, f_{cr}. Besides, Figure 3.3 shows the phase response of the input filter where δ_{11} and δ_{13} are the phase shifts introduced by the input filter to the 11th and 13th harmonic currents of the CSC. In the design of the input filter,

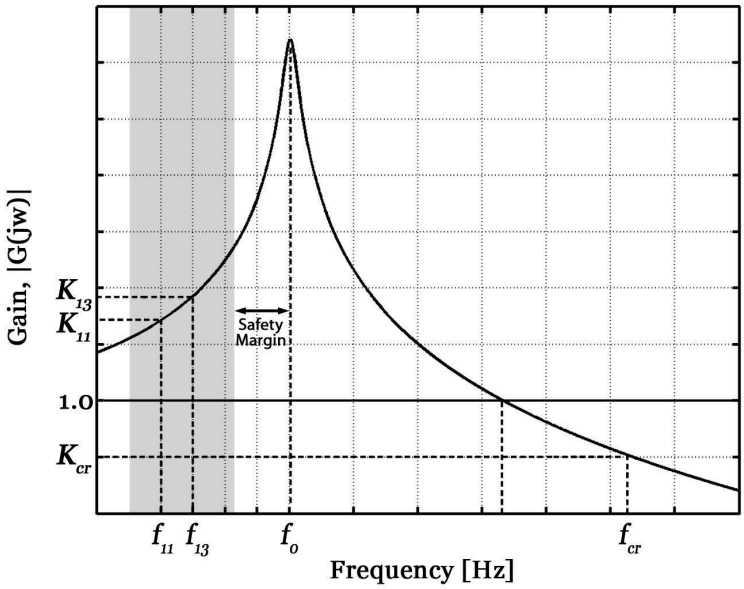


Figure 3.2: Gain response of a sample input filter

f_0 and f_{cr} are under the control of designer, whereas Q_0 is partly controllable. Therefore, a compromise is needed in view of satisfactory filtering of carrier harmonics, kVA reduction and sizes of input filter elements.

3.2 Input Filter Design

3.2.1 Selection of f_0

The choice of the natural frequency, f_0 of the input filter is certainly based on the selection of which harmonic components of the load current are to be eliminated. In the example, since the 11^{th} and 13^{th} harmonics will be filtered out, 550 Hz and 650 Hz are the base frequencies in the design work. The first option for the selection of f_0 is choosing it far above 650 Hz, that is $f_0 \gg 650$ Hz, thus input filter will slightly affect the 11^{th} and 13^{th} harmonic components, as illustrated in Figure 3.4. Although this will make the input filter and the control system simpler, it is not practical because of the fact that higher natural frequency introduces higher carrier frequencies in PWM for the sufficient elimination of the carrier harmonics. Besides, in medium power applications, a switching frequency of maximum a few kHz is applicable due the power semiconductor devices available in the market.

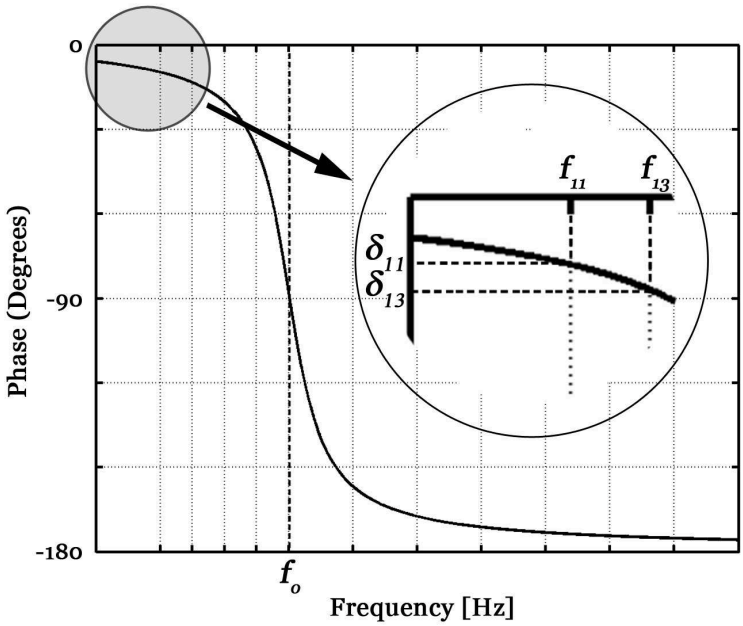


Figure 3.3: Phase response of a sample input filter

The second option is choosing $f_0 \ll 550$ Hz, in this case input filter will affect the 11th and 13th harmonic components, as illustrated in Figure 3.5. This approach may decrease the switching frequency at the expense of the attenuations at 550 Hz and 650 Hz components, thus introduces a reduction in the APF rating, which is an undesired operation. Besides, as in (2.27), the lower f_0 necessitates higher filter capacitances and/or inductances. In the application prototype of the CSC based APF, since there is a coupling transformer, which acts as the filter inductance, it is possible to increase the filter inductance only by introducing a series external inductance, which requires more space, and increases the cost. On the other hand, increasing the filter capacitance will also increase the installed rating of the CSC. As a result, another approach rather than $f_0 \gg 650$ Hz or $f_0 \ll 550$ Hz should be accomplished by compromising the size of the filter equipment, and switching frequency and losses.

In view of the considerations given above, the natural frequency of the input filter should be chosen in such a way that it can be slightly lower than 550 Hz, or slightly higher than 650 Hz. In Figure 3.6, an illustration is given to show the gain responses of the input filters having natural frequencies of $f_0 < 550$ Hz, and $f_0 > 650$ Hz. In both cases, the 11th and 13th harmonics injected by the CSC will be amplified while passing through the input filter. Thanks to the control system employed in the CSC based APF, this amplification is used

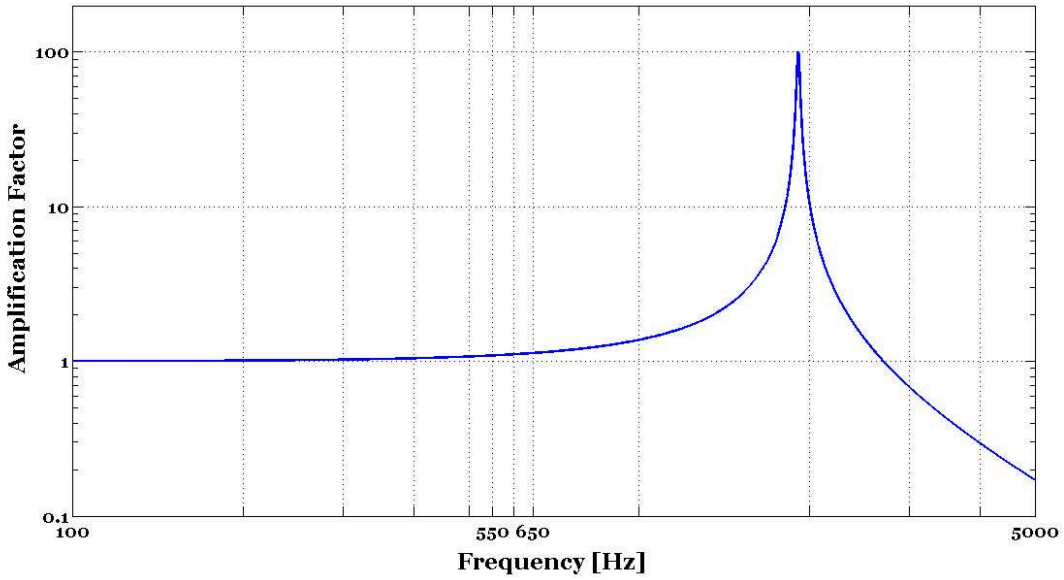


Figure 3.4: Gain response of a sample input filter for $f_0 \gg 650$ Hz

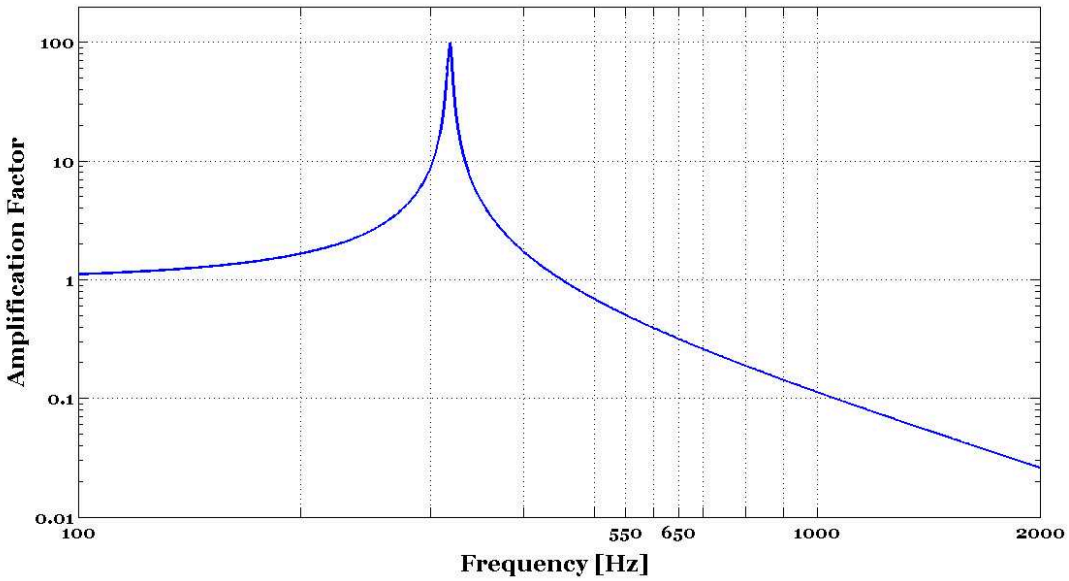


Figure 3.5: Gain response of a sample input filter for $f_0 \ll 550$ Hz

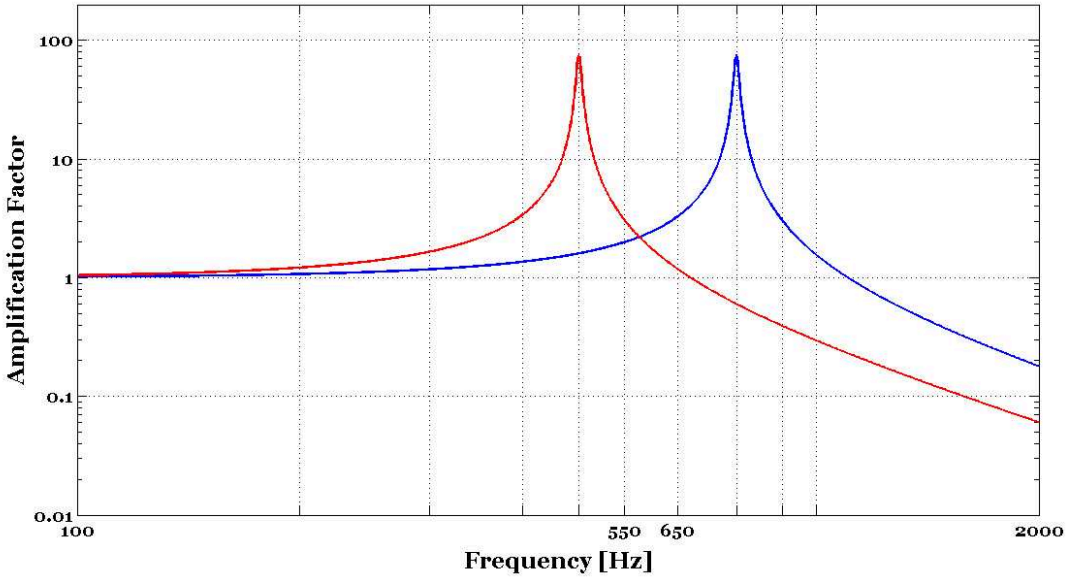


Figure 3.6: Gain responses of sample input filters for $f_0 < 550$ Hz and $f_0 > 650$ Hz

beneficially to reduce the rating of the CSC. Since the 11th and 13th harmonic components in the line current of the APF are not affected by the proposed selective harmonic extraction based active damping method, any gain higher than unity at these frequencies will introduce a reduction in the rating of the CSC for the same APF rating.

For the input filter having $f_0 < 550$ Hz, phase and gain responses at 550 Hz and 650 Hz are given by (3.1).

$$\boldsymbol{G}_i(j\omega_{11}) = \boldsymbol{G}_i(j11\omega_s) = K_{11}\angle(\theta_{11}) = K_{11}\angle\delta_{11}$$
$$\boldsymbol{G}_i(j\omega_{13}) = \boldsymbol{G}_i(j13\omega_s) = K_{13}\angle(\theta_{13}) = K_{13}\angle\delta_{13} \tag{3.1}$$

where K_{11} and K_{13} are higher than **unity**, and

$$\delta_{11} = \arctan\left|\frac{\omega_0\omega_{11}/Q_0}{\omega_0^2-\omega_{11}^2}\right| \tag{3.2}$$

$$\delta_{13} = \arctan\left|\frac{\omega_0\omega_{13}/Q_0}{\omega_0^2-\omega_{13}^2}\right| \tag{3.3}$$

For the input filter having $f_0 > 650$ Hz, phase and gain responses at 550 Hz and 650 Hz are also given by (3.4).

$$\boldsymbol{G}_i(j\omega_{11}) = \boldsymbol{G}_i(j11\omega_s) = K_{11}\angle(\theta_{11}) = K_{11}\angle{-\delta_{11}}$$
$$\boldsymbol{G}_i(j\omega_{13}) = \boldsymbol{G}_i(j13\omega_s) = K_{13}\angle(\theta_{13}) = K_{13}\angle{-\delta_{13}} \tag{3.4}$$

where K_{11} and K_{13} are again higher than **unity**.

Therefore, in order to accomplish SHAM, f_0 can be chosen as either < 550 Hz or > 650 Hz to obtain gains (K_{11} and K_{13}) at these frequencies higher than unity. However, f_0 is chosen as > 650 Hz in this work by taking into consideration the following issues:

- If $f_0 > 650$ Hz, then not only 11^{th} and 13^{th} harmonics, but also the 5^{th} and 7^{th} harmonics can be generated, and injected by the CSC in the same manner, but with reduced amplification gains. On the other hand, there is a wide safety margin between the 350 Hz and f_0, the operation will be stable, and is not affected by the changes in the system parameters as described below. However, for the case of $f_0 < 550$ Hz, there would not be a sufficient safety margin between the 350 Hz and f_0, which may result in an unstable operation with high dependence on system parameters.

- Capacitance of the filter capacitor may decrease in the long term owing to aging. This increases the f_0, as can be understood from (2.27), and if f_0 is chosen as to be < 550 Hz, then f_0 may coincide with 550 Hz (or 650 Hz). Therefore, it is not recommended to choose $f_0 < 550$ Hz.

It can be concluded from the considerations given above that f_0 should be > 650 Hz, K_{11} and K_{13} should be higher than unity, and δ_{11} ad δ_{13} should be as small as possible. In order to meet all these requirements with a stable operation, a safety margin, Δf, as given in Figure 3.2, should be left between f_0 and 650 Hz in view of the following considerations:

- Normally, supply frequency, f_s varies in a limited range, say 50 ± 0.2 Hz. However, during severe faults or in time periods (of the order of seconds) prior to brown outs, larger fluctuations in supply frequency may occur. Obviously, these frequency deviations affect f_{11} and f_{13} proportionately with f_s, while f_0 remains the same as can be understood from (2.27). Such events may push f_{13} towards f_0, resulting in undesirable

operating conditions for APF, although, in fact, its protection mechanism should react before these conditions occur.

- As the frequency of harmonic component, f_{13} approaches to f_0, gain and phase response characteristics become sharper. Since f_{13} is directly proportional to supply frequency variations, the choice of a relatively small safety margin between f_{13} and f_0 gives rise to significant changes in K_{11}, and K_{13}. Hence, selecting f_0 very close to highest order harmonic to be eliminated (f_{13}) violates our assumption of constant K_{13} and δ_{13}. These conclusions can be drawn not only for single-line harmonics f_{11} and f_{13}, but also for their sub-group harmonics defined in [91].

3.2.2 Reduction in kVA Rating of CSC

The kVA rating of the APF can be expressed by (3.5) for the case of eliminating 11^{th} and 13^{th} harmonic components of the load current.

$$kVA_{APF} = \sqrt{3} V_{LV} \sqrt{{I_{f_1}}^2 + {I_{f_{11}}}^2 + {I_{f_{13}}}^2}, \tag{3.5}$$

where, V_{LV} is the true rms value of the line-to-line voltage referred to the secondary side of the transformer, I_{f_1} is the rms value of the fundamental current component corresponding to transformer and CSC losses, and $I_{f_{11}}$ and $I_{f_{13}}$ are the rms values of the 11^{th} and 13^{th} harmonic components of the APF current, respectively. If the system is partly dedicated to reactive power compensation in D-STATCOM mode in addition to major action of active power filtering, the reactive current generated by the circuit should be included in I_{f_1}.

Similarly, the kVA rating of the CSC can be expressed by

$$kVA_{CSC} = \sqrt{3} V_{LV} \sqrt{{I_{csc_1}}^2 + {I_{csc_{11}}}^2 + {I_{csc_{13}}}^2}, \tag{3.6}$$

where, I_{csc_1} is the rms value of the fundamental current component corresponding to transformer and CSC losses, and $I_{csc_{11}}$ and $I_{csc_{13}}$ are the rms values of the 11^{th} and 13^{th} harmonic components of the CSC current, respectively.

11^{th} and 13^{th} harmonic components of the CSC current for the corresponding harmonic components of the APF current are given by (3.7) and (3.8) owing to the proposed SHAM.

$$I_{csc_{11}} = \frac{I_{f_{11}}}{K_{11}} \tag{3.7}$$

$$I_{csc_{13}} = \frac{I_{f_{13}}}{K_{13}} \tag{3.8}$$

where, K_{11} and K_{13} are amplification factors higher than unity as a result of the amplification property of input filter. The kVA rating of the CSC is then expressed with respect to the APF currents as follows:

$$kVA_{CSC} = \sqrt{3}V_{LV}\sqrt{{I_{csc_1}}^2 + \frac{{I_{f_{11}}}^2}{{K_{11}}^2} + \frac{{I_{f_{13}}}^2}{{K_{13}}^2}}. \tag{3.9}$$

In the comparison of the kVA ratings of the APF and CSC, the fundamental components should be excluded because of the fact that kVA ratings of the CSC and APF change not only due to the rms values of the fundamental currents, but also due to the direction of the reactive power flow. In case of a leading power factor at the output of the APF, there will be a further increase in the kVA rating of the APF without any fundamental component in the CSC current. On the other hand, there will be a significant increase in the kVA rating of the CSC for a lagging power factor. Therefore, (3.9) is reduced to (3.10) under the assumption of zero fundamental current component of CSC.

$$kVA_{CSC} = \sqrt{3}V_{LV}\sqrt{\frac{{I_{f_{11}}}^2}{{K_{11}}^2} + \frac{{I_{f_{13}}}^2}{{K_{13}}^2}}. \tag{3.10}$$

It is clearly seen from (3.10) that the kVA rating of the CSC is reduced with respect to the kVA rating of the APF, according to the rms values of the 11^{th} and 13^{th} harmonic currents, and associated amplification factors K_{11} and K_{13}. The variation of the ratio kVA_{APF}/kVA_{CSC} is given in Figure 3.7 for sample values of $K_{11} = 2.0$ and $K_{13} = 3.4$ against the p.u. values of the 11^{th} and 13^{th} harmonic currents injected by the APF.

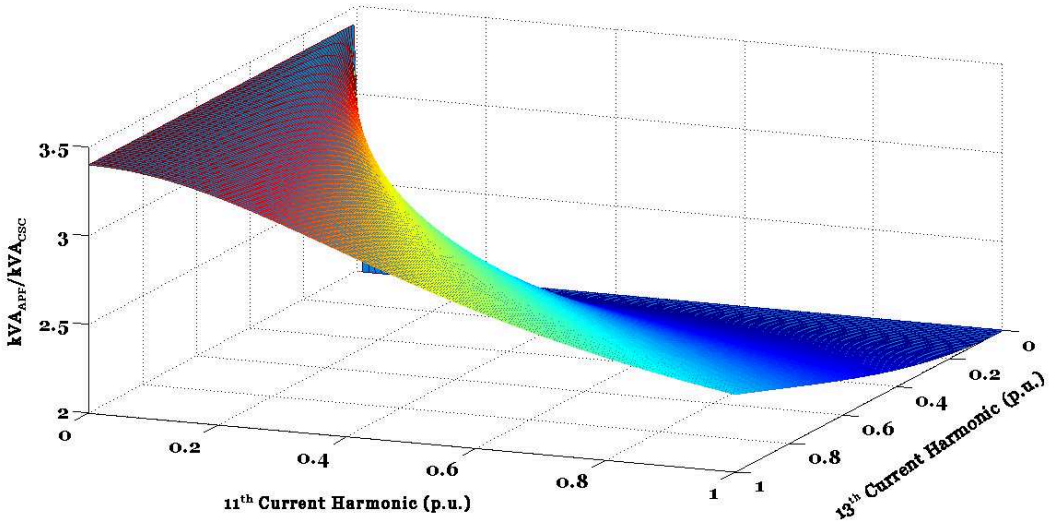


Figure 3.7: Variation of the kVA_{APF}/kVA_{CSC} against the p.u. values of the 11th and 13th harmonic currents for $K_{11} = 2.0$ and $K_{13} = 3.4$

3.2.3 Selection of Q_0

In the design of the input filter, Q_0 in (2.28) is not entirely under the control of the designer. This is because, for small and medium size coupling transformers, total leakage reactance, and internal winding resistances can be realized in a range bounded by practical conditions, e.g. total leakage reactance from 5 to 8 %, and Q_0 from 50 to 100, in practice. Selection of high Q_0 values such as hundred is advantageous in order to make the phase shift angles, δ_{11} and δ_{13} nearly zero. Furthermore, this choice will increase the amplification factors, K_{11} and K_{13}, for the pre-specified f_0, resulting in a further reduction in kVA rating of CSC. However, selection of high Q_0 has some disadvantages, e.g. K_{11} and K_{13} become more sensitive to supply frequency fluctuations, thus may necessitate adaptive control. High K_{11} and K_{13} values would cause large amounts of amplified harmonic currents through the filter capacitor, so that such a power electronic capacitor may not be implementable. Q_0 should be chosen in view of these considerations.

3.2.4 Suppression of Carrier Harmonics

Theoretically, carrier frequency, f_{cr} should be chosen as high as possible in order to minimize the magnitudes of side-band harmonics of carrier significantly. However, in practice, this is

not possible. f_{cr} is largely dictated by switching capability of semiconductor devices available in the market. Switching the power semiconductors at frequencies higher than usual figures (a few kHz) causes an increase in switching losses, which are directly proportional to frequency, and hence results in a de-rated CSC.

According to (2.26) and (2.29), the gain of the input filter at carrier frequency, as shown in Figure 3.2, is given by

$$K_{cr} \simeq \frac{1}{{f_n}^2} = \frac{{f_0}^2}{{f_{cr}}^2} \tag{3.11}$$

for $f_n \gg 1$ and, Q_0 is a large positive number (in the range from 50 to 100).

K_{cr} should be sufficiently small, so that corresponding carrier harmonics should comply with associated harmonic current limits specified in IEEE Std. 519-1992. The limit is specified to be less than 0.3 % for harmonic orders greater than or equal to 35 for the weakest supply, and defined with respect to maximum of 15 min. averages of the load current, I_L. In practice, K_{cr} should be less than 10 % for the weakest supply conditions, and most of the distorted loads. Hence, from (3.11), f_{cr} should be higher than 3.16 times f_0.

3.3 Conclusions

In this chapter, the proposed SHAM for the kVA reduction of the CSC has been explained on the specific example of eliminating the 11^{th} and 13^{th} harmonic components of a non-linear load. It has been shown that SHAM is mainly based on the amplification property of the input filter at some selected frequencies. Hence, the design of input filter is major concern in the application of the proposed SHAM. The second main part in the SHAM is the proposed active damping method for non-selected harmonic components. Since the natural frequency of the input filter has been chosen close to the frequencies of the harmonic components to be eliminated, the active damping method may also affect those harmonic current components. In order to avoid this, the active damping method, which is based on selective harmonic extraction, has been proposed to avoid any attenuation in the harmonic current components to be injected by the CSC. By this way, amplification property of the input filter at those frequencies is kept unchanged.

In the design procedure, it has been shown that the f_0 should be chosen close to the highest frequency of the harmonic current components, which is 650 Hz in the given example, with a safety margin, Δf. Also, f_0 should be lower than the highest frequency of the harmonic current components in order to provide a reliable operation in case of power system faults, or problems arising from the ageing of the filter capacitors. Besides, such a selection of f_0 also provides the capability of filtering the lower dominant current harmonics, 5^{th} and 7^{th} for the given example, in the same manner but, with reduced amplification gains.

In the proposed SHAM, if the gains of the input filter at those pre-selected harmonic frequencies are chosen as higher than unity, the harmonic currents injected by the CSC will be obviously smaller than the corresponding APF currents. It has been shown that the kVA rating of the CSC is reduced considerably as compared to the kVA rating of the APF depending on the rms values of the injected harmonic components.

Finally, the approach to the selection of the f_{cr} for the designed input filter has been presented in order to suppress the sideband harmonics of the carrier. It has been shown that the f_{cr} should be higher than 3.16 times f_0, for sufficient filtering performance, which is higher than 90 %, at the carrier frequency.

CHAPTER 4

DESIGN AND IMPLEMENTATION OF THE CURRENT SOURCE CONVERTER BASED ACTIVE POWER FILTER

4.1 Introduction

The system description and operation principles of the Current Source Converter (CSC) based Active Power Filter (APF) have been presented in Chapter 2. It has been shown that the CSC based APF should meet the following objectives:

- filtering of some pre-selected harmonic components of a non-linear load,
- damping out the oscillations due to the parallel resonance of the input filter.

In this chapter, design and implementation principles of an application prototype for the CSC based APF will be presented. Design of the prototype system will be accomplished according to the needs of an industrial system, which is a Light Rail Transportation (LRT) system characterized by 12-pulse uncontrolled rectifiers fed from a MV bus.

The model of the overall system including supply, load and the APF is constructed in PSCAD v4.2 [89]. The load is modeled by a 12-pulse rectifier supplying power to an RL load. Load parameters are adjusted so that, 11^{th} and 13^{th} harmonics measured in the field are produced. The performance of the APF has been tested by comparing 11^{th} and 13^{th} harmonics injected by APF with load harmonics in view of the IEEE Std.519-1992. The proposed SHAM and DSPWM have been exercised by this model. The specifications of the CSC including power semiconductors, heatsinks, busbars, filter capacitors and the dc-link reactor have been determined according to the results of simulation work.

The first step in the design is the determination of load characteristics by PQ measurements in the field. System sizing study will then be carried out. The size and the specifications of the input filter elements are determined in the next step. The dc-link inductance, L_{dc}, is then determined by considering peak-to-peak current ripple in the dc-link and TDD of the harmonics injected by the APF to the supply excluding the selected 11^{th} and 13^{th} harmonics. Specifications of power switches are roughly determined in view of the semiconductor current and voltage waveforms obtained from the simulations. Among the commercially available semiconductor devices, candidate IGBTs and reverse blocking fast-recovery diodes, the choice of power semiconductors is verified by carrying out switching tests in the laboratory. The performance of the control system is first tested by simulation work, and then after implementation improved by laboratory tests. Implementation work of the CSC based APF is also described in this chapter.

4.2 Load Characterization and Design Specifications

Within the scope of this thesis, an application prototype of CSC based APF has been designed and implemented in order to eliminate the 11^{th} and 13^{th} current harmonics of the 12-pulse uncontrolled rectifiers, which are supplying the catenary lines of the Bursa Light Rail Transportation System (Bursaray).

A simplified single-line diagram of the sample LRT system is given in Figure 4.1. Catenary lines at 1500 Vdc are fed from 12-pulse uncontrolled rectifiers located in different substations. 1500 Vdc is then converted to the variable frequency ac by traction converters. The 12-pulse uncontrolled rectifiers, located in different substations, are fed from MV bus via long underground cables. The major power quality problems encountered in interfacing LRT systems to the grid are as follows:

- Twelve-pulse rectifiers generate 11^{th}, 13^{th}, 23^{rd}, 25^{th},...., $(12n \pm 1)^{th}$ harmonic current components. Among these, usually the 11^{th} and 13^{th} harmonics exceed the limits specified in IEEE Std. 519-1992. For the LRT system in Bursaray, the daily variations of 11^{th} and 13^{th} current harmonics (3 sec. averaged data) are as given in Figure 4.2.
- After midnight, when the transportation system is out of service, long medium voltage underground cables produce large amounts of capacitive reactive power to the grid.

This may cause reactive energy penalties according to the tight regulations [11]. Active and reactive power variations (3 min. averaged data) are given in Figure 4.3.

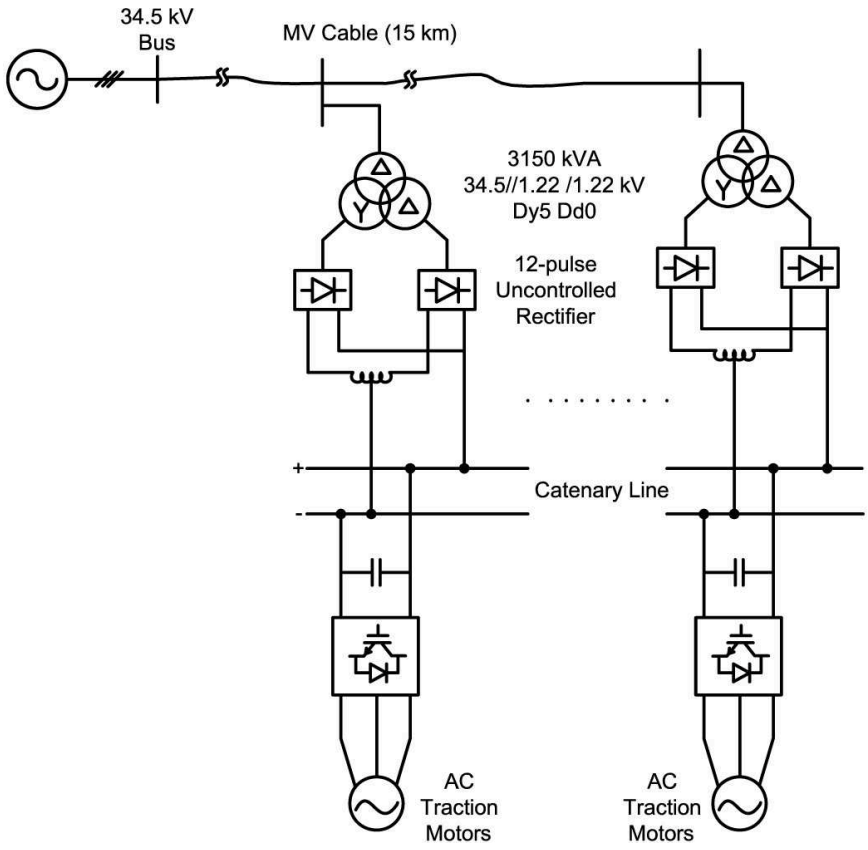
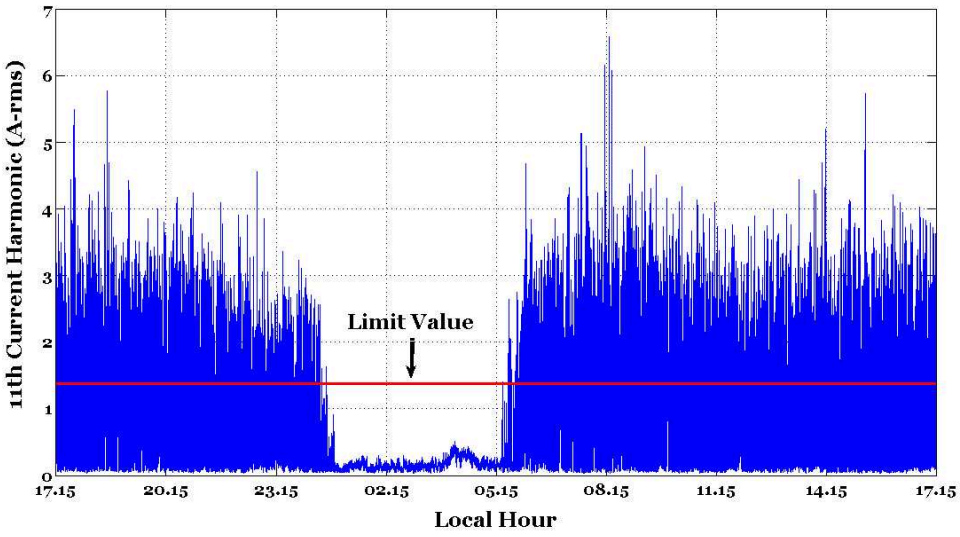


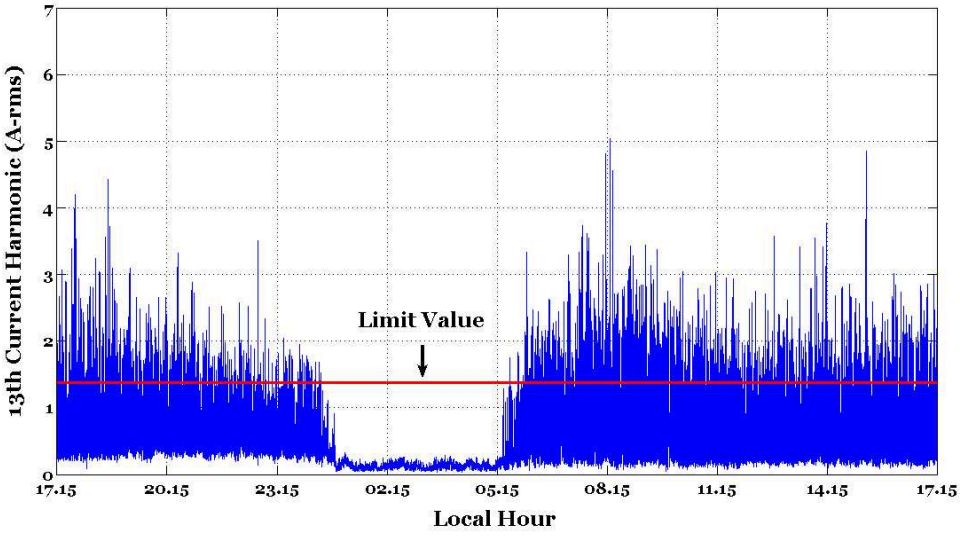
Figure 4.1: Simplified single-line diagram of the LRT system

It is seen from Figure 4.2 that 11^{th} and 13^{th} current harmonics of the sample LRT system are exceeding the specified limits almost all of the times during the operation period. Hence, the application prototype, which is being described in this thesis, has been designed and implemented to eliminate these harmonic components of the Bursaray LRT system.

Since the 12-pulse uncontrolled rectifiers are connected to the MV bus, the CSC based APF should also be connected to the MV bus, which is the PCC of the LRT system. The APF can not be connected to the secondary side of the rectifier transformers because 5^{th} and 7^{th} current harmonic components are eliminated by transformer connection (two secondary windings with delta-wye connection). As described in the previous chapter, the CSC based APF has been designed for connection to the MV bus via a coupling transformer, which has been

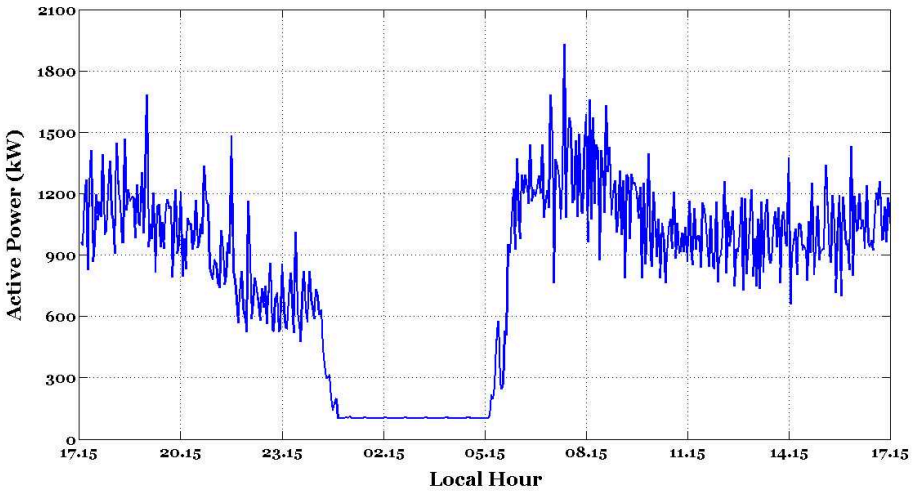


(a)

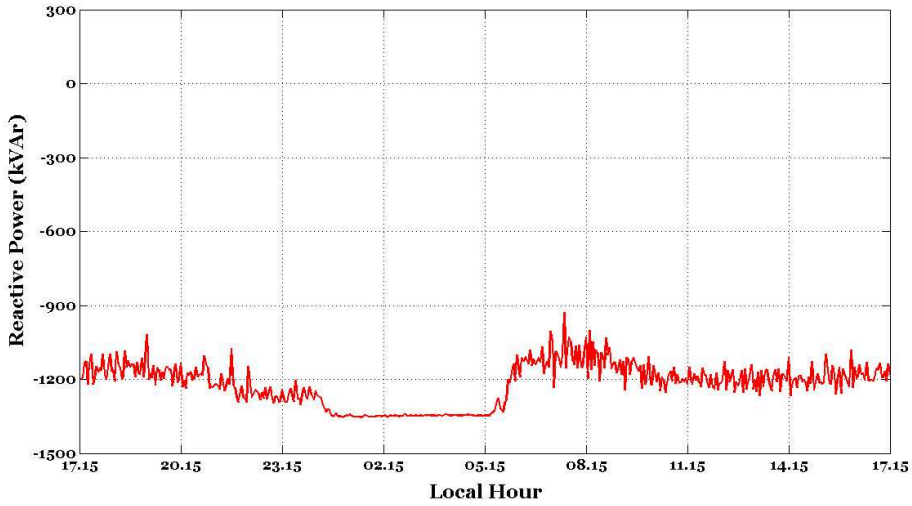


(b)

Figure 4.2: Daily variations of the (a) 11th and (b) 13th current harmonics of the LRT system (3 sec. averaged data recorded in the field)



(a)



(b)

Figure 4.3: Daily variations of the (a) active and (b) reactive power demand of the LRT system (3 min. averaged data recorded in the field)

already established in the LRT system for reactive power compensation of the long MV underground cables as illustrated in Figure 4.4.

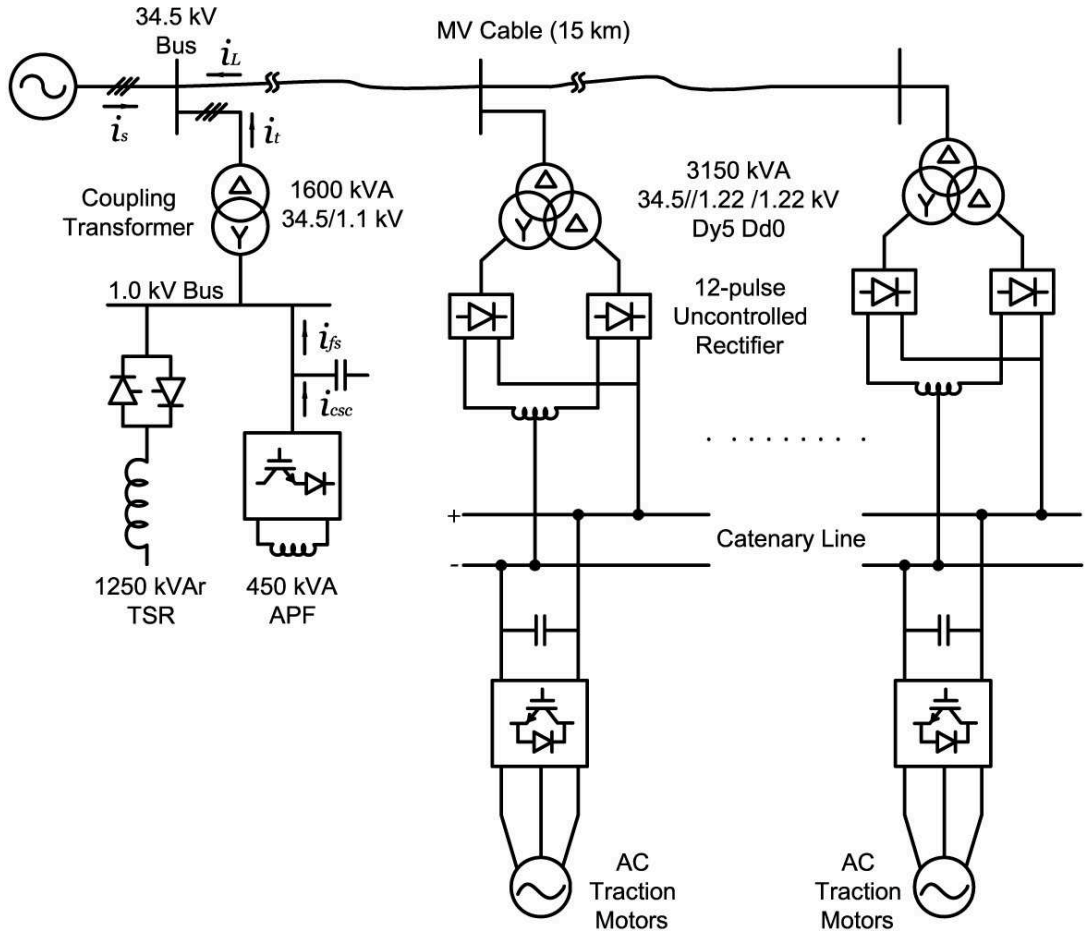


Figure 4.4: Simplified single-line diagram of the LRT system and CSC based APF

The reactive power compensation system, established in year 2004, has a coupling transformer (34.5/1.1 kV, 1600 kVA) to connect the Thyristor Switched Reactor (TSR) of 1250 kVAr to the MV bus. Since a suitable coupling transformer is already available, the CSC based APF has been designed for connection to the secondary side of this coupling transformer, thus necessitating a voltage rating of 1.0 kV, which is the highest voltage for LV systems [90].

Since the coupling transformer and the nominal voltage at the secondary side are determined by the existing system, the power circuit design of the prototype CSC based APF has been accomplished in view of these constraints. Another issue in the design work is the reactive

power generation capability of the CSC based APF required for the application. Since the long MV underground cables generate large amounts of capacitive reactive power, the CSC based APF should either have unity power factor at its output, or be capable of generating further inductive reactive power. This constraint makes necessary the input filter capacitors to be kept at a minimum possible value, or a higher converter rating is required to eliminate the excessive capacitive reactive power.

According to the constraints given above, technical specifications of the application prototype are as listed in Table 4.1. The design of the system will be carried out according to these technical specifications.

Table 4.1: Technical specifications for the prototype CSC based APF

Technical Specification	Rating
Nominal bus voltage	1.0 kVrms line-to-line
Coupling transformer	1600 kVA, 34.5 / 1.1 kV, U_k 5.77 %
11^{th} harmonic current	$\geq$ 6.0 Arms at 34.5 kV
13^{th} harmonic current	$\geq$ 4.0 Arms at 34.5 kV
Net reactive power output	$\geq$ 0 (inductive)
Physical dimensions	as small as possible

4.3 Sizing of Input Filter Elements

As mentioned in the previous chapter, design of the input filter is the most critical task in the overall design procedure of the CSC based APF with SHAM. Three main specifications, which should be taken into consideration in the design procedure, are listed as follows:

- APF is going to inject 11^{th} and 13^{th} harmonic components to the network.
- There is a coupling transformer which is rated at 1600 kVA, 34.5 / 1.1 kV, 5.77 % U_k.
- The net output reactive power of the APF should be either zero, or inductive.

The specifications given above dictate the natural frequency of the input filter, the size of the filter equipment, and the carrier frequency.

In view of the discussions given in Section 3.2.1 and the constraints given above, the safety margin, Δf, is chosen as 130 Hz for $f_s = 50$ Hz. Thus, the natural frequency of the input filter becomes 780 Hz for the highest frequency of the harmonic currents to be filtered out, which is 650 Hz.

4.3.1 Calculation of L_f and C_f

For the chosen $f_0 = 780$ Hz, filter inductance and capacitance values can be found. The leakage reactance X_{tr} of the coupling transformer is given by

$$X_{tr} = \frac{V_{kV}^2}{S_{MVA}} U_k \tag{4.1}$$

where V_{kV} is the nominal line-to-line bus voltage (referred to either primary or secondary side) in kV rms, S_{MVA} is the rated power of the transformer in MVA, and U_k is the short circuit impedance of the coupling transformer. X_{tr} is calculated for the given coupling transformer referred to the LV side is calculated from (4.2).

$$X_{tr} = \frac{1.1^2}{1.6} 0.0577 = 43.79\ m\Omega \tag{4.2}$$

where

$$X_{tr} = 2\pi f_s L_{tr}. \tag{4.3}$$

Thus, L_{tr} is found to be 139 μH. Filter capacitance can then be calculated from (4.4).

$$C_f = \frac{1}{(2\pi f_0)^2 L_{tr}} = \frac{1}{(2\pi \cdot 780)^2 139\mu} \simeq 300\ \mu F. \tag{4.4}$$

The corresponding reactive power generation at rated voltage (1.0 kV) is given by (4.5).

$$Q = V_{l-l}^2 (2\pi f_s C_f) = (1.0k)^2 (2\pi \cdot 50 \cdot 300\mu) = 94.25\ kVAr. \tag{4.5}$$

Hence, an inductive reactive power equal to 94.25 kVAr should be generated by the CSC to cancel out the capacitive reactive power produced by the input filter capacitors.

In view of the considerations given in Section 3.2.3, Q_0 is chosen as 75 in the design work, and it is corrected in the implemented system according to the measured of amplification factors of 11^{th} and 13^{th} harmonics. Thus, series resistance, r_f of the input filter is found as 9.1 $m\Omega$ by using (2.28) for $L_f = 139\ \mu H$, and $C_f = 300\ \mu F$.

4.3.2 Characteristics of the Designed Input Filter

The transfer function of the LC-type input filter is given in (4.6) for the calculated inductance, capacitance and resistance values; and its gain and phase responses are presented in Figures 4.5 and 4.6.

$$\mathbf{G}_i(s) = \frac{\omega_0^2}{s^2 + (\omega_0/Q_0)s + \omega_0^2} = \frac{24.02 \cdot 10^{-6}}{s^2 + 65.35s + 24.02 \cdot 10^{-6}} \tag{4.6}$$

where $\omega_0 = 2\pi f_0$.

The gains and phase angles of the 11^{th} and 13^{th} harmonic components in (4.7) are then deduced from Figures 4.5 and 4.6.

$$\begin{aligned} \mathbf{G}_i(j\omega_{11}) &= \mathbf{G}_i(j11\omega_s) = 2.05\angle(-1.1)^o \\ \mathbf{G}_i(j\omega_{13}) &= \mathbf{G}_i(j13\omega_s) = 3.35\angle(-2.1)^o \end{aligned} \tag{4.7}$$

4.3.3 Filter Capacitor Ratings

The final stage in the input filter design process is the determination of the voltage and current ratings of the input filter capacitor. Since the amplification property of the input filter for the 11^{th} and 13^{th} harmonic components is used, harmonic currents at these frequencies are also circulating through the filter capacitor as illustrated in Figure 4.7, which shows the p.u. values of 11^{th} and 13^{th} current harmonics flowing through the shunt input filter capacitor. Current loading of filter capacitors are determined by calculating actual values of I_{c11} and I_{c13} at rated operating conditions, that is

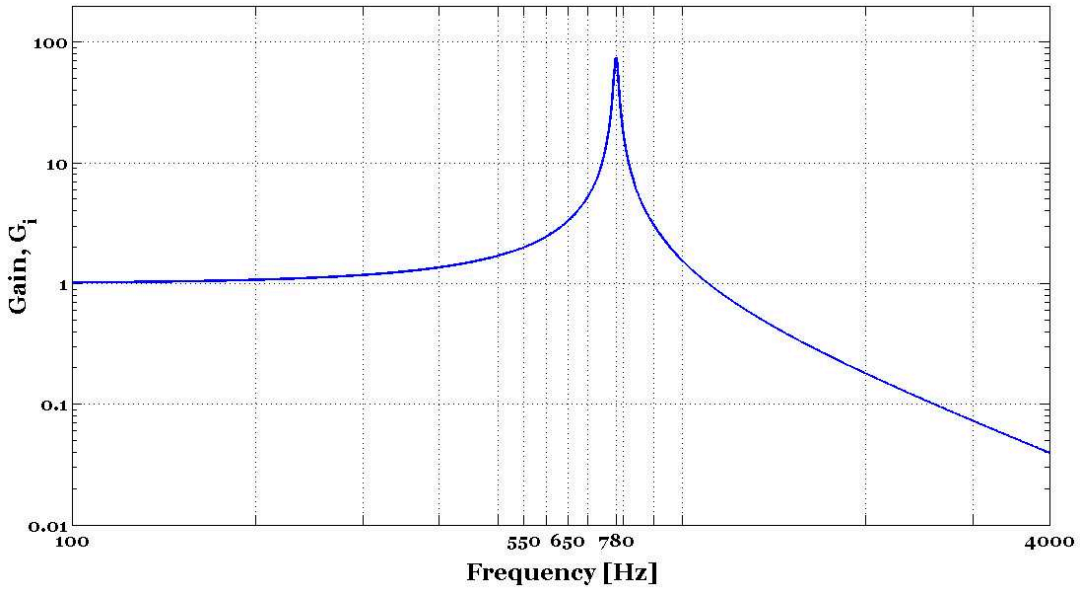


Figure 4.5: Gain response of the designed input filter

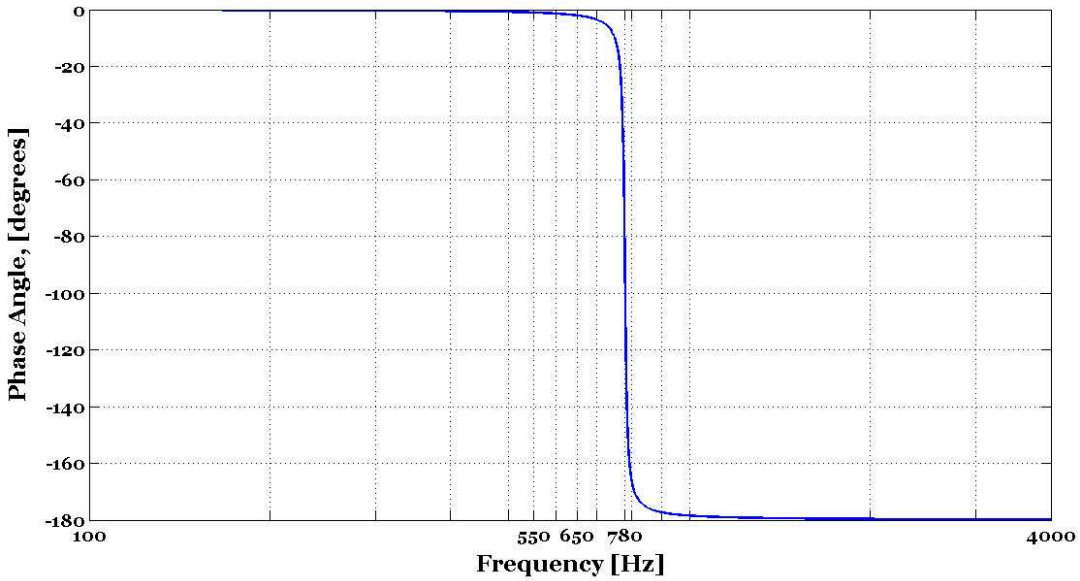


Figure 4.6: Phase response of the designed input filter

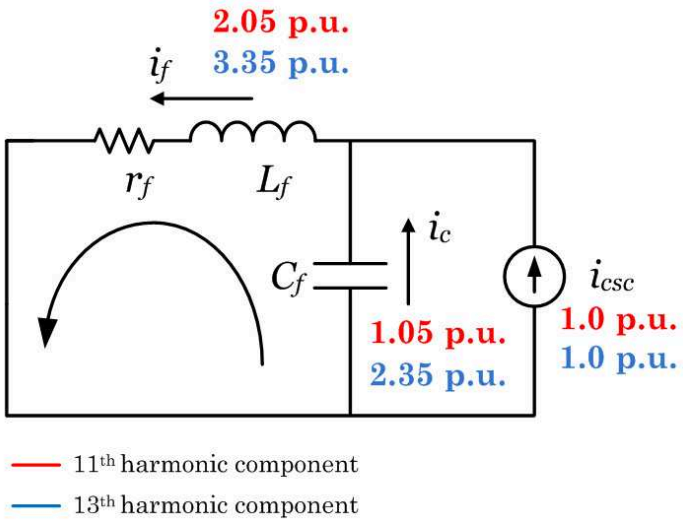


Figure 4.7: Illustration of the flow of 11th and 13th harmonics

$$I_{crated} > \sqrt{I_{c1}^2 + I_{c11}^2 + I_{c13}^2 + \sum_{h\neq 1,11,13} I_{ch}^2} \tag{4.8}$$

where I_{ch} is rms value of the h^{th} harmonic component of the filter capacitor current. It is worth to note that if the amplification gains for the 11th and 13th harmonics were kept at very high values than the design values given above, very high currents would circulate through the filter capacitor, thus making the filter capacitor bulky, and costly.

In order to find the maximum current circulating through the filter capacitor, simulations have been carried out in EMTDC/PSCAD for the design values of the 11th and 13th harmonic components, which are 6.0 Arms and 4.0 Arms at MV level, respectively. In Figure 4.8, current waveform of the line current of the filter capacitor is shown, and its harmonic spectrum is given in Figure 4.9. The true rms value of the line current of the filter capacitor is found as 207 Arms for rated power of the APF with these simulations.

The maximum line-to-neutral rms voltage of the capacitor, V_c can be calculated by

$$V_c = \sum_h \left(\frac{I_{ch}}{2\pi h f_s C_f}\right) \tag{4.9}$$

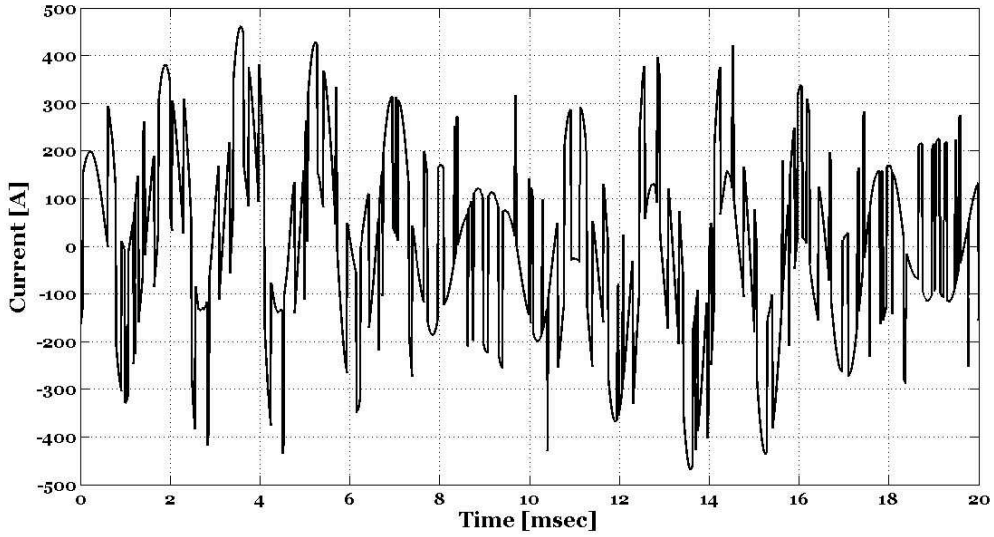


Figure 4.8: Line current waveform of the filter capacitor for the design values of 11th and 13th harmonics (Theoretical)

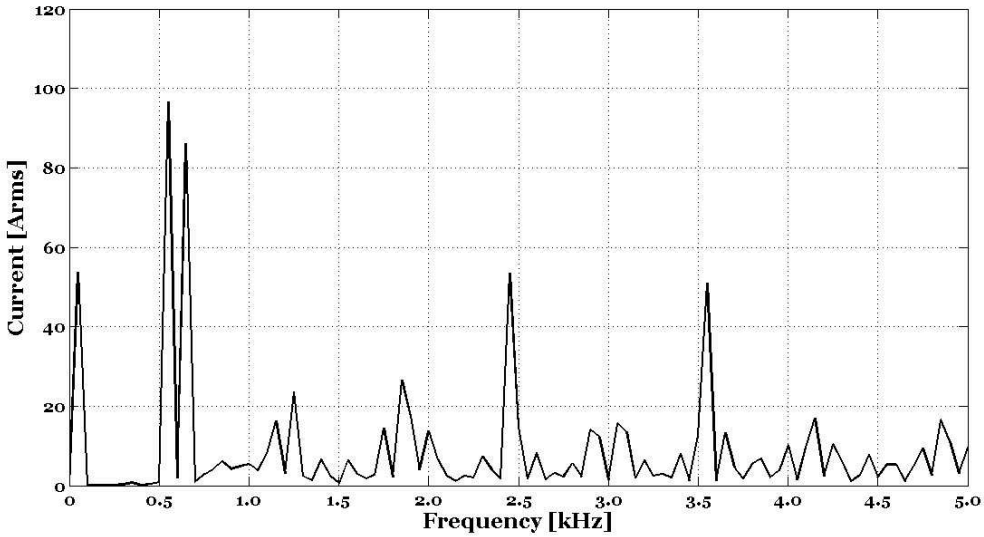


Figure 4.9: Harmonic spectrum of line current of the filter capacitor for the design values of 11th and 13th harmonics (Theoretical)

where I_{ch} is the rms value of the h^{th} harmonic component of the line current of the filter capacitor. V_c is found as 781 Vrms by using Figure 4.9 and taking into account only the dominant harmonic components.

As a result, the filter capacitor should have a minimum current rating of 207 Arms, and a minimum voltage rating of 781 Vrms. Since there is no neutral conductor in the system, filter capacitors have to be connected in delta. This results in ratings of 119.5 Arms and 1352.7 Vrms. In order to meet these requirements, 33 μF capacitors from ELECTRONICON [93] have been chosen as the filter capacitors in the application prototype, in which there are nine capacitors of 33 μF connected in delta as three groups. Therefore, each capacitor, rated at 100 A true-rms current rating, will carry a current of only 39.8 A rms. The chosen capacitor has a voltage rating of 1700 V rms, and 4000 Vdc, which is far above the calculated maximum voltage of 1352.7 V rms. Technical specifications of the chosen capacitor is given in Table 4.2.

Table 4.2: Technical specifications of the filter capacitor

Technical Specification	Rating
Rated capacitance	33 μF ±10%
Rated ac voltage	2400 V ac
Rated dc voltage	4000 V dc
Max. rms voltage	1700 V rms
Surge voltage	6000 V
Rated energy	264Ws
Max. rms current	100 A rms
Series resistance	0.6 mΩ
Self inductance	160 nH

4.4 Selection of f_{cr}

The gain of the input filter at carrier frequency, K_{cr} should be sufficiently small as discussed in 3.2.4, so that corresponding carrier harmonics should comply with IEEE Std. 519-1992. f_{cr} is found to be > 2467 Hz by using the (3.11) for the chosen f_0 = 780 Hz. It is seen from Figure 4.5 that the gain is smaller than 10 % for the frequency values > 2.5 kHz. In view

of these considerations, f_{cr} is, therefore, chosen as 3.0 kHz in the designed and implemented CSC based APF, which provides 93 % filtering of the carrier harmonics.

4.5 Design of DC-link Reactor

Since it is always pursued as the main disadvantage of the CSCs, determination of the dc-link reactor is a critical step in the design procedure. In order to determine the dc-link inductance value, first of all, the design value of the dc-link current should be fixed. The maximum peak value of the reference current vector, i_{max} (excluding the active damping and error compensation) is given by

$$i_{max} = \sqrt{2}(I_{csc_1} + I_{csc_{11}} + I_{csc_{13}}) \tag{4.10}$$

where I_{csc_1} is the rms value of the fundamental current drawn by CSC and, $I_{csc_{11}}$ and $I_{csc_{13}}$ are the rms values of the 11^{th} and 13^{th} current harmonics injected by the CSC, respectively. i_{max} is found for the worst case, in which the peak values of the harmonic components are added.

In the application prototype, design value for the 11^{th} harmonic component at 34.5 kV level is 6.0 Arms, and 4.0 Arms for the 13^{th} harmonic component as in Table 4.1; and the amplification gains (K_{11} and K_{13}) of the input filter for the 11^{th} and 13^{th} harmonic components are 2.05 and 3.35, respectively as given in (4.6). The fundamental current of the CSC, I_{csc_1} is calculated by (4.5) and (4.11) for the unity power factor operation at the output current of the APF.

$$I_{csc_1} = \frac{Q}{\sqrt{3}V_{l-l}} = \frac{94.25kVAr}{\sqrt{3}\ 1.0kV} = 54.4\ Arms \tag{4.11}$$

Therefore, i_{max} is found by

$$I_{csc_{11}} = (I_{11})_{MV}\frac{n}{K_{11}} = 6.0\frac{31.36}{2.05} = 91.8\ Arms, \tag{4.12}$$

$$I_{csc_{11}} = (I_{13})_{MV}\frac{n}{K_{13}} = 4.0\frac{31.36}{3.35} = 37.5\ Arms, \tag{4.13}$$

and

$$i_{max} = \sqrt{2}\,(54.4 + 91.8 + 37.5) = 259.8\ A \tag{4.14}$$

where n=31.36 is the turns ratio of the transformer. From (4.14), the reference dc-link current, $I_{dc}{}^{*}$ is chosen to be 300 A in order to make sure the converter being operated in a linear region. It is worth to note that if the proposed amplification property of the input filter, or simply $SHAM$, was not used, from (4.10), the dc-link current should be minimum 550 A.

Now, the value of the dc-link inductance can be found in view of the $I_{dc}{}^{*}$ and the harmonic currents to be generated by the CSC. Since there is a circulating instantaneous power between the load and APF, the stored energy in the inductor should be capable of supplying the total half-cycle energy of the harmonic components. The maximum half cycle energy required for h^{th} harmonic component is given by [24]

$$E_h = \frac{\sqrt{2}\,V_{l-l}\,I_h}{2\,h\,f_s} \tag{4.15}$$

where I_h is the rms value of the h^{th} harmonic component referred to the LV side.

For the application prototype, total maximum-half cycle energy, $E_{\sum}$ can be found by

$$\begin{aligned} E_{\sum} &= \frac{\sqrt{2}V_{l-l}}{2f_s}\left(\frac{I_{11}}{11} + \frac{I_{13}}{13}\right) \\ &= \frac{\sqrt{2}\,10^3}{100}\left(\frac{91.8}{11} + \frac{37.5}{13}\right) = 158.8\ Joules \end{aligned} \tag{4.16}$$

As a result, the required dc-link inductance for $E_{\sum}$=158.8 J , and $I_{dc}{}^{*}$=300 A is given by

$$\begin{aligned} L_{dc} &\geq \frac{2E_{\sum}}{I_{dc}{}^{2}} \\ &\geq \frac{2\cdot 158.8}{300^2} = 3.53\ mH \end{aligned} \tag{4.17}$$

In order to find the optimum L_{dc} value, the maximum peak value of the dc-link current and the TDD value at the PCC has been analyzed. The peak value of the dc-link current determines

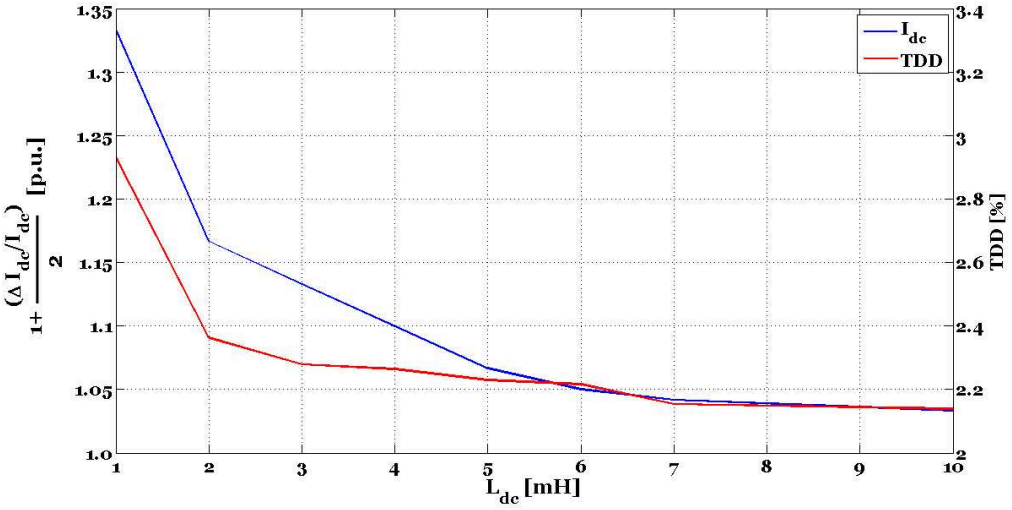


Figure 4.10: Variation of the maximum peak dc-link current and TDD against L_{dc} *(Theoretical)*

the maximum turn-off current of the semiconductor devices. TDD value has been calculated by taking into account all the undesired harmonic components generated by the APF at the PCC, excluding the selected 11^{th} and 13^{th} harmonic components. In Figure 4.10, the variation of the dc-link current in p.u., and the TDD at the PCC are given against the variation of the L_{dc} value. It is seen that the ripple on the dc-link current and the TDD value remain almost same for the L_{dc} values higher than 5.0 mH. In the design procedure, a peak-to-peak ripple of 10.0 % was chosen as the criteria for the selection of L_{dc} value. In view of these considerations, the dc-link reactor value for the application prototype was chosen as 4.0 mH.

The dc-link reactor is implemented as iron-core reactor owing to the lower losses compared to air-core one, in which higher number of turns due to the low permeability (μ_0) result in higher losses. The dc winding resistance of the dc-link reactor is given as 7.4 $m\Omega$ by the manufacturer, H. V. Mangoldt, for 4.0 mH. As described in the previous chapter, gains of the dc control loop can be found by using these values.

The cut-off frequency of the dc-control loop, ω_{ndc} is chosen as 471 rad/sec. For this value, proportional and integral gains are found by using (2.42) and (2.44) as 1.35 and 2.49, respectively. The cut-off frequency of the LPF (2.44), which is used for smoothing the dc-link current, then becomes 667 rad/sec.

4.6 Determination of Damping Gain

After fixing the values of the input filter circuit elements and dc-link current, the next stage in the design procedure is the determination of the damping gain. As seen from Figure 4.5 that the harmonic components around the natural frequency of the input filter are significantly amplified. In order to damp these oscillations, the proposed active damping method will be employed, in which all the undesired harmonic components will be damped without any effect on 11^{th} and 13^{th} ones. By this way, the benefit comes from the amplification property of the input filter at 550 Hz and 650 Hz will not be lost, and the rating of the CSC will be reduced significantly for the same APF rating.

In order to find the optimum damping gain value, which practically equals to the fictitious $1/R_d$, simulations have been carried out both in Matlab [92] and EMTDC/PSCAD. In Figure 4.16, the amplification factor versus frequency characteristics of the input filter are given for various fictitious damping resistor values. It is seen that oscillations are damped effectively for all values of R_d between 1.0 Ω to 5.0 Ω. Since the damping gain, G_d is equal to $1/R_d$, the smaller R_d yields to higher G_d, and higher reference current vectors for active damping. Hence, in order to keep the dc-link current value as low as possible with the linear operation of the converter, G_d should be chosen by compromising the resultant harmonic components and the peak value of the reference current vector.

Another constraint for the selection of damping gain is the stability of the ac control loop. Higher damping gains provide better attenuation of the non-selected harmonic current components. However, there is a limitation on the selection of damping gain in view of the system stability. Simplified block diagram of the ac current control loop, which is used to damp out the non-selected harmonic current components, is as given in Figure 4.11. APF current, i_f is given by (4.18) with respect to i_{csc} as follows [67]:

$$i_f = i_{csc} \cdot \frac{1}{1 + (j\omega L_f + r_f)e^{-j\omega T_d} G_d - \omega^2 L_f C_f + j\omega C_f r_f} \tag{4.18}$$

where $\omega = 2\pi f$ and T_d is the control delay time, which is simply equal to the half of PWM period. From (4.18), loop transfer function, H_{loop}, is obtained by

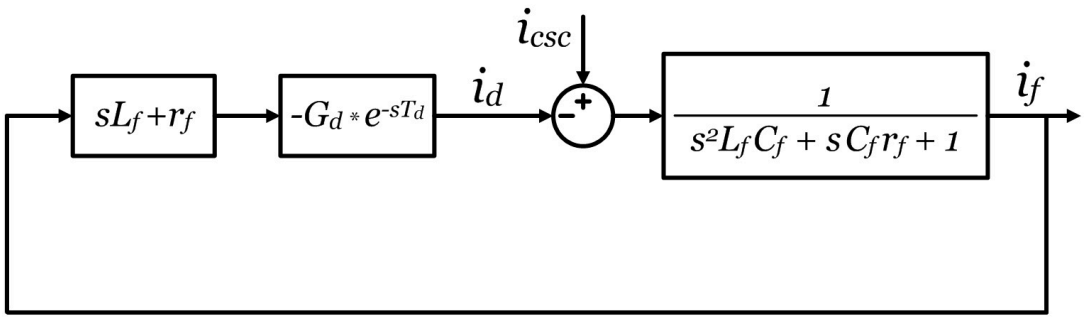


Figure 4.11: Simplified block diagram of the ac current control loop

$$H_{loop} = \frac{(sL_f + r_f)e^{-sT_d}G_d + 1}{s^2L_fC_f + sC_fr_f}. \tag{4.19}$$

In Figures 4.12-4.15, nyquist plots of the loop transfer function are given for different G_d values. It is seen from Figure 4.12 that for $G_d = 0$, phase margin is very small, and response of the system is oscillatory. For $G_d \geq 2.0$, Figures 4.14 and 4.15, the intersection of the nyquist plot and the real axis is on the left of (-1,0), and system becomes unstable. Hence, it can be concluded that G_d should be smaller than 2.0 for a stable operation.

In the view of the considerations given above, $G_d = 0.4$ has been chosen as the optimum value for active damping. Final modulating waveform used in DSPWM is as shown in Figure 4.17 for $G_d = 0.4$ and, design current values of 6.0 Arms, and 4.0 Arms at MV level for 11^{th} and 13^{th} harmonics, respectively. It is seen from Figure 4.17 that peak value of the final reference current is smaller than 300 A for the chosen G_d. Besides, system is stable for the chosen G_d as shown in Figure 4.13.

4.7 Selection of Power Semiconductor Devices

After determination of the dc-link current as to be 300 A, there are no other unknown parameters for the selection of the power semiconductors. The maximum peak voltage, excluding the over voltages during commutations, to which the power semiconductors will withstand, should be calculated to determine the voltage ratings of the power semiconductor devices.

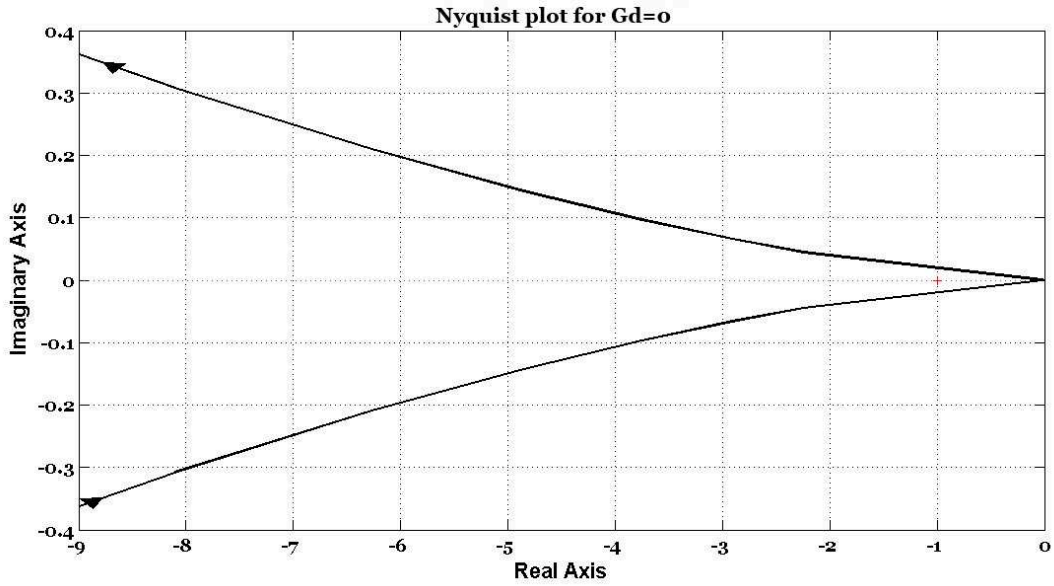


Figure 4.12: Nyquist plot of the loop transfer function for $G_d = 0$

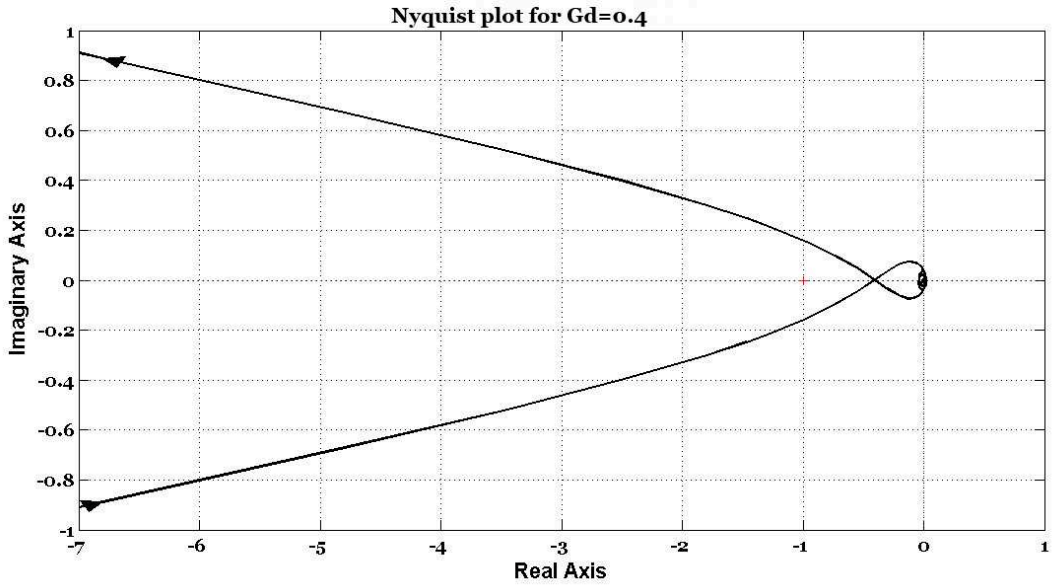


Figure 4.13: Nyquist plot of the loop transfer function for $G_d = 0.4$

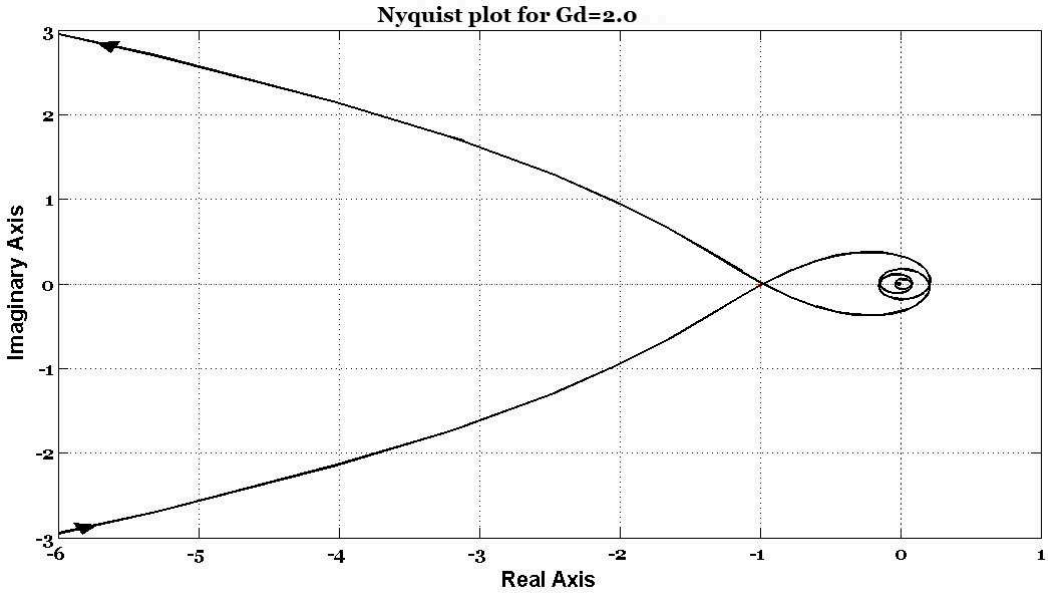


Figure 4.14: Nyquist plot of the loop transfer function for $G_d = 2.0$

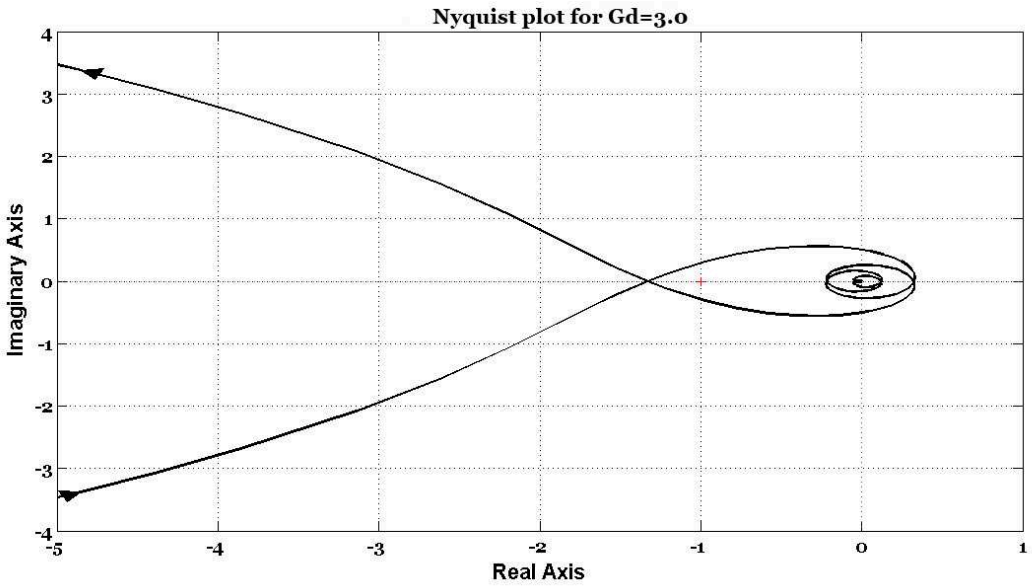


Figure 4.15: Nyquist plot of the loop transfer function for $G_d = 3.0$

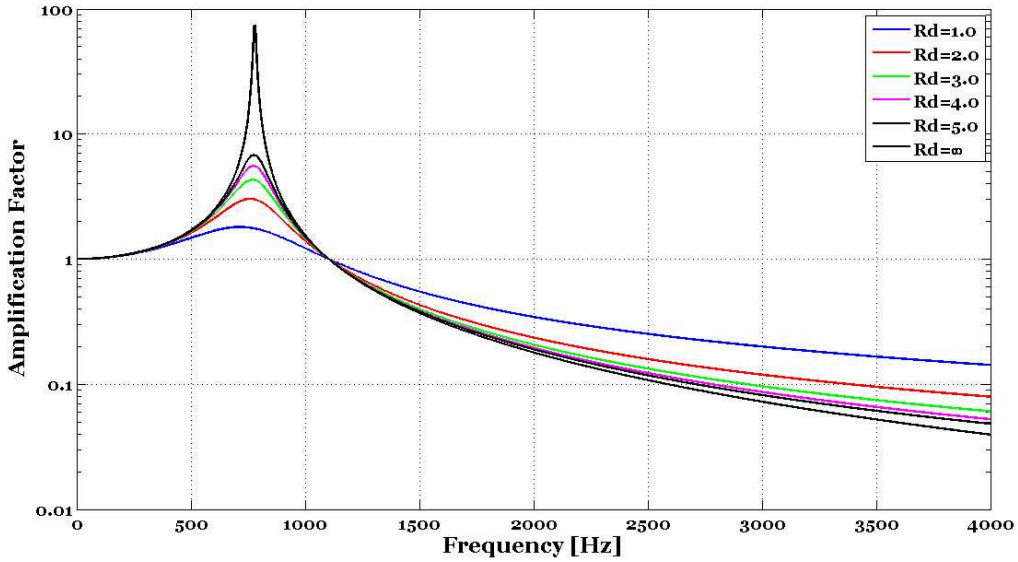


Figure 4.16: Amplification factors for various damping resistors

The maximum peak line-to-line voltage, V_{max} at the secondary side of the coupling transformer is given by (4.20) using (4.12), and (4.13). V_{max} is calculated for the worst case, in which the peak values of the harmonic voltages as well as fundamental one are summed algebraically. The harmonic voltages are calculated for the corresponding currents, which are the design values of the 11^{th} and 13^{th} harmonic components.

$$\begin{aligned} V_{max} &= \sqrt{2}\{1.1V_{l-l} + \sqrt{3}L_f(\omega_{11}K_{11}I_{11} + \omega_{13}K_{13}I_{13})\} \\ &= \sqrt{2}\{1100 + \sqrt{3}\cdot 139\cdot 10^{-6}(3455.8\cdot 2.05\cdot 91.8 + 4084\cdot 3.35\cdot 37.5)\} \\ &= 1951.7\ V \end{aligned} \tag{4.20}$$

It is seen from (4.20) that V_{max} will be higher than 2.0 kV with the transient over voltages during the commutation periods of the semiconductor devices. For that reason, power semiconductor devices should have at least 3300 V voltage rating, which is a standard voltage level for the High Voltage (HV) semiconductor devices available in the market. The candidate power semiconductor devices are GTO (Gate Turn-Off Thyristor), IGBT (Insulated Gate

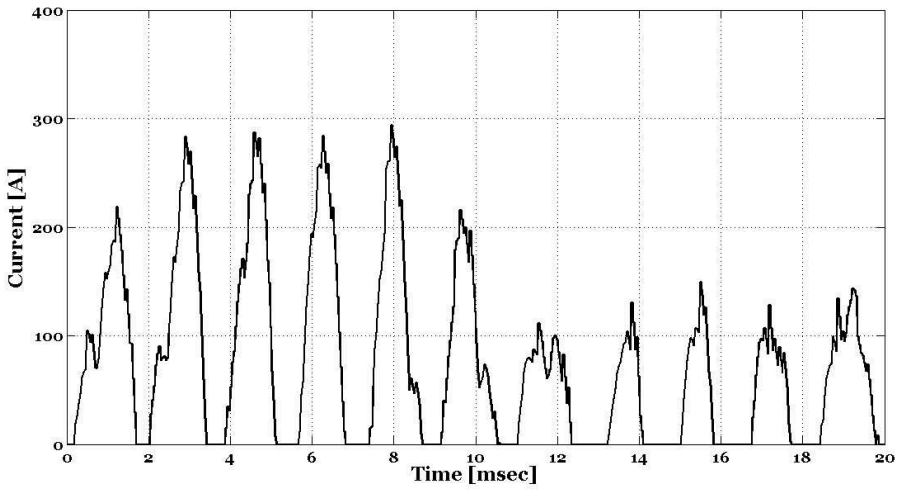


Figure 4.17: Final modulating waveform used in DSPWM for the design values of 11^{th} and 13^{th} harmonics

Bipolar Transistor) and IGCT (Integrated Gate Commutated Thyristor). Owing to the its old technology, which requires a complex drive circuit, and shows poor switching performance, GTO is eliminated. Although there are also other novel power semiconductor switches such as IEGT (Injection Enhanced Gate Transistor) from Toshiba [30, 94] and ETO (Emitter Turn-Off Thyristor), they have not been commercialized yet.

Aforementioned in the previous chapter, there are six power semiconductor switches in the CSC, which have unidirectional current carrying, and bipolar voltage blocking capability, thus being characterized as symmetrical. Although symmetrical IGCT has been known and commercially available, symmetrical HV IGBT has not been produced yet [30], [95]-[97]. HV IGBTs are generally produced with their antiparallel freewheeling diodes in the same housing [98]-[102]. But, there are also some HV IGBTs, which are still asymmetric but do not have antiparallel freewheeling diodes, and can not block reverse voltages [103]. In the view of the chosen switching frequency of 3.0 kHz, although they are well-suited to VSC applications, the most suitable devices are the HV IGBT modules among the candidate devices due to the following advantages:

- HV IGBTs (especially the modules) can be found in the market easily from many manufacturers at different voltage and current ratings.
- Since HV IGBTs are being used in many VSC applications such as traction, isolated

gate drive circuits for these devices are available in the market.

- Since the case of the HV IGBT modules are isolated, it provides flexibility in the design, and reliability in the operation. Besides, isolated case also provide the application of either the conventional forced-air cooling, or water cooling without the need of de-ionized coolant.

From the considerations given above, HV IGBT modules are chosen for use in the CSC based APF application prototype. Although, there is no need to use the antiparallel freewheeling diode of the IGBT in CSC applications, almost all the IGBT modules do have these diodes, which are not harmful in the normal operation of the CSC. In order to achieve the reverse voltage blocking capability, an appropriate diode should be connected in series with the HV IGBT module. For asymmetrical and reverse conducting IGBTs, series diodes are chosen as fast recovery type and compatible with the housing of the corresponding IGBT.

The key technical specifications of the candidate HV IGBT modules are given in the Table 4.3. Although the dc-link current is chosen to be 300 A, IGBT modules having a collector current rating of 1200 A have been chosen due to the possible increase of the LRT system in the near future, and better cooling capacity of these modules compared to the that of having smaller current ratings such as 400 A, and 800 A.

It is seen from Table 4.3 that HV IGBT module of Mitsubishi brand with the part number of **CM1200HC-66H** is showing a better performance in view of the conduction and switching losses as compared to the other ones. For that reason, CM1200HC-66H is chosen as the HV IGBT module to be used in the application prototype.

As mentioned above, a fast-recovery diode should be use in series with the chosen IGBT module to achieve the reverse blocking capability. However, fast-recovery diodes have high reverse-recovery (RR) currents with high *di/dt*. This results in high over voltages during the commutation periods of the diodes, which have been analyzed in detail in [30]. On the other hand, not only the peak value of the RR current, but also the *di/dt* during RR is determined by the total inductance in the commutation circuit, and the switching characteristics of the HV IGBT module. Hence, the fast-recovery diode should be chosen by considering both the maximum safe *di/dt* defined with the RRSOA (Reverse Recovery Safe Operating Area), and the reverse recovery current, I_{rr}.

Table 4.3: Technical specifications of the candidate HV IGBT modules

Part Number	Manufacturer	V_{CES} (V)	I_C (A)	$V_{CE(SAT)}$ (V)	$E_{(ON)}$ (J/P)	$E_{(OFF)}$ (J/P)
FZ1200R33KF2C	Infineon	3300	1200	4.3	2.2	1.55
FZ1200R33KL2C-B5		3300	1200	3.7	3.15	1.9
CM1200HA-66H	Mitsubishi	3300	1200	4.8	1.75	1.0
CM1200HB-66H		3300	1200	4.0	1.80	1.50
CM1200HC-66H		**3300**	**1200**	**3.6**	**1.6**	**1.55**
DIM1200ESM33-F	Dynex	3300	1200	3.6	2.6	1.8
MBN1200D33C	Hitachi	3300	1200	4.8	2.1	1.6
MBN1200E33D		3300	1200	4.2	1.60	1.30
5SNA 1200E330100	ABB	3300	1200	3.8	1.89	1.95
5SNA 1200G330100		3300	1200	3.85	1.73	1.90
MIO1200-33E10	IXYS	3300	1200	3.8	1.89	1.95
MIO1200-33E11		3300	1200	3.8	1.75	2.0

For that reason, a 1200 A, 3300 V diode, **RM1200HA-66S** from Mitsubishi company has been chosen by taking into consideration the compatibility in housing, delivery times (availability in the market) and unit prices, as well as the technical considerations given above. Sample pictures of the chosen semiconductor devices are given in Figure 4.18.

In order to turn the HV IGBT modules on and off, a proper gate drive circuit has to be used with the selected modules. Since, the chosen IGBTs are being widely used in traction applications, suitable and custom-designed gate drivers are available in the market [104, 105]. A driver, which is specifically designed for the CM1200HC-66H, has been chosen from CONCEPT as the gate drive unit to be used in the application prototype. By the use of CONCEPT driver (1SD536F2-CM1200HC-66H) the need of an isolated supply for each IGBT with 3300 V isolation has disappeared. It is seen from the technical specifications of the gate drive unit given in Table 4.4 that the driver can be used upto 9.0 kHz, which is far above the design value of 3.0 kHz. Besides, the fiber optic interface of the driver provides a further isolation between the power and control circuits.

Table 4.4: Technical specifications of the gate drive unit

	Minimum	Typical	Maximum	Unit
General				
Supply voltage	14,5	15	16	V
Supply current		120		mA
Gate peak current	-36		36	A
Switching frequency			9	kHz
DC-link voltage			2200	V
Operating voltage			3300	V
Test voltage (50Hz/1min)			6000	$Vrms$
Short circuit protection				
Vce voltage threshold	50		60	V
Response time		9.5	10	μs
Blocking time		1		s
Gate output				
Turn-on resistor (Rg_{on})		1.8		Ω
Turn-off resistor (Rg_{off})		3.8		Ω
Aux. gate capacitor		220		nF
Timing characteristics				
Turn-on delay time		350		ns
Turn-off delay time		450		ns
Acknowledge time		380		ns
Acknowledge pulse width	0.6		1.8	μs

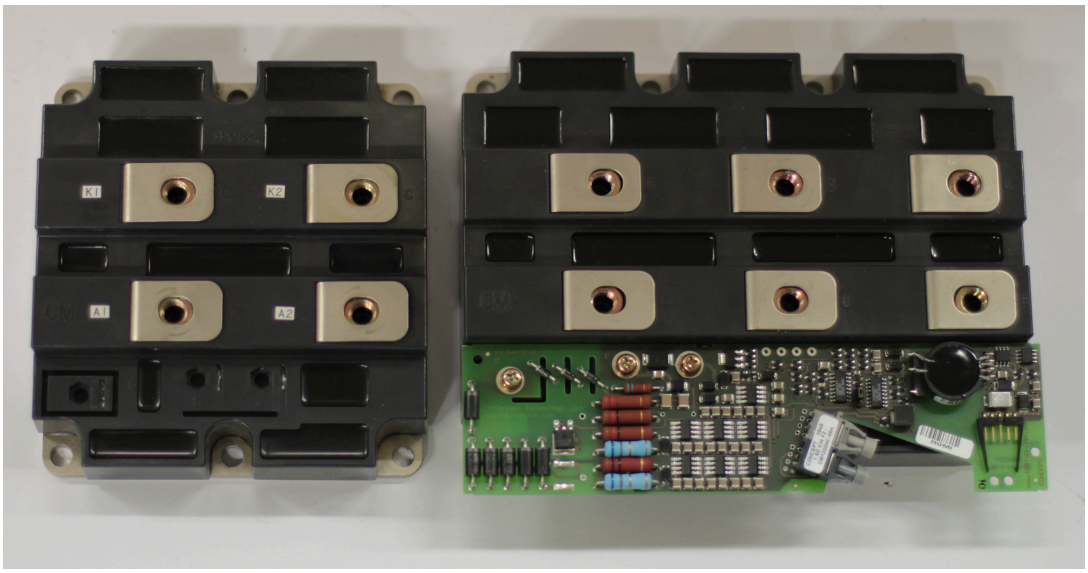


Figure 4.18: Sample picture of the chosen HV IGBT (right) and fast-recovery diode (left) modules

4.8 Design of Cooling System

In order to decide on the type, or rating of the cooling system, total losses expected at the rated power should be calculated theoretically. For this purpose, simulations have been carried out in EMTDC/PSCAD, and theoretical current and voltage waveforms of one IGBT and one diode have been recorded for a duration of 20 ms as given in Figure 4.19 for $I_{11(MV)}$ = 6.0 $Arms$ and $I_{13(MV)}$ = 4.0 $Arms$ harmonic currents at 34.5 kV, and f_{cr} = 3.0 kHz.

For the waveforms given in Figure 4.19, all conduction and switching losses have been calculated for each pulse according to the technical characteristics of the IGBT and diode modules. Before the loss calculation, following calculations and scalings have been made:

- The collector-emitter saturation voltage, $V_{CE(SAT)}$ of the IGBT module was calculated for the collector current, I_C of 300 A, and the gate-emitter voltage, V_{GE} of 15 V from the data sheet of the CM1200HC-66H. For these conditions, $V_{CE(SAT)}$ is taken as 2.3 V.
- The forward voltage drop, V_F of the diode was scaled according to the forward current, I_F of 300 A, and junction temperature, T_j of 25 $°C$, hence V_F is taken as 2.0 V.
- Turn on energy per pulse, E_{on} of the IGBT module is calculated for I_C=300 A, and gate resistances, Rg_{on} and Rg_{off} of 3.8 Ω, and taken as 0.86 J/pulse. However, this value is

valid for V_{CE}=1650 V, for that reason, it is scaled for the corresponding voltage value for each pulse in Figure 4.19, e.g. it is 0.43 J/pulse for V_{CE}=825 V.

- Like E_{on}, turn off energy per pulse, E_{off} is calculated as 0.91 J/pulse, and scaled according to the voltage value of the IGBT for each pulse.
- The reverse recovery energy per pulse, E_{rec} of the diode is also calculated for I_F=300 A as 0.38 J/pulse for reverse recovery voltage, V_{rr} of 1650 V, and scaled according to the voltage value of the diode for each pulse.

By using the Figure 4.19, and the calculations given above, conduction and switching losses of the IGBT and diode are found as in Table 4.5.

As it can be seen from Table 4.5 that total loss, for only one IGBT and one diode module, is 1912 W. Therefore, total loss of the converter (six IGBTs and six diodes) will be nearly 12.0kW. For that reason, the cooling system, to be used in the application prototype, should have a cooling capacity of minimum 12.0kW, and heat sinks to be used for cooling of the IGBT and diode modules should also be capable of transferring this amount of heat.

In the application prototype of the CSC based APF, in order to save from space, and to transfer the generated heat to outside of the building, in which APF will be established, a water cooled system has been chosen as the cooling system of the CSC based APF. The first step in the design procedure of the cooling system is the selection of the heatsinks to be used in the system. The most important design criterion in this work is the maximum allowable junction temperatures of the semiconductor devices. Since the 75 % of the total loss is generated by the IGBTs, this criterion is mostly dictated by the heat transfer characteristics of the IGBTs. The junction temperature of the IGBT module is given by

Table 4.5: Conduction and switching losses of the IGBT and diode modules

	Loss, W
IGBT Conduction	332
Diode Conduction	289
IGBT Turn-on	475
IGBT Turn-off	580
Diode Reverse Recovery	236
Total	**1912**

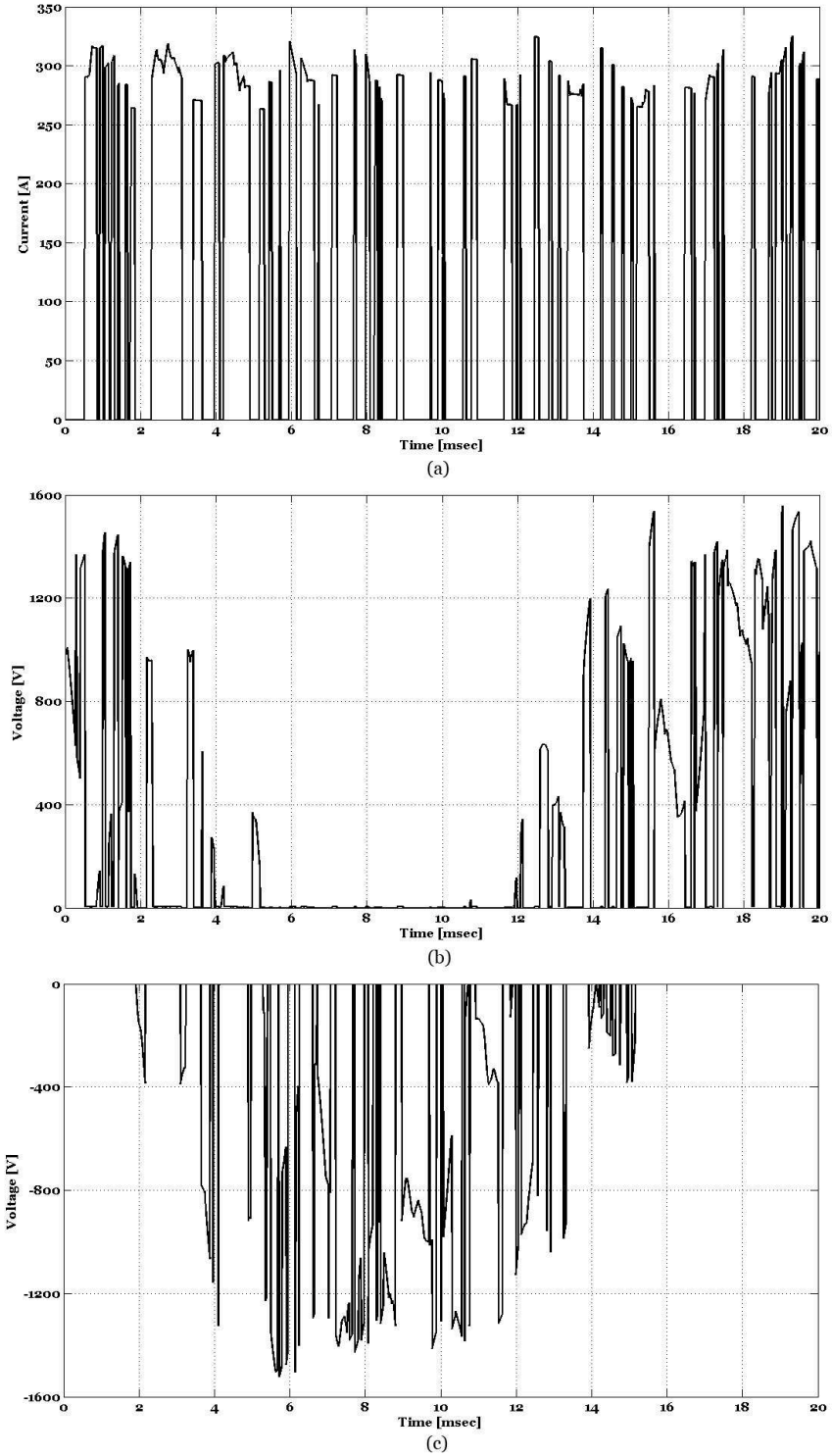


Figure 4.19: Voltage and current waveforms of IGBT and diode for $I_{11(MV)} = 6.0\ Arms$ and $I_{11(MV)} = 4.0\ Arms$ (a) IGBT current (b) IGBT voltage (c) Diode voltage *(Theoretical)*

$$T_j = P_{IGBT}\,(R_{j-c} + R_{c-h}) + T_h \tag{4.21}$$

where P_{IGBT} is the total loss of the one IGBT module, R_{j-c} is the junction-to-case, and R_{c-h} is the case-to-heatsink thermal resistance of the IGBT module, and T_h is the temperature of the heatsink. If T_j of the IGBT module is designed as to be maximum 90 °C for R_{j-c} = 8.5 K/kW, R_{c-h} = 6.0 K/kW and P_{IGBT}=1387 W, T_h will be maximum 70 °C. In order to keep the water flow and the size of the heatsink at minimum, the temperature rise on the heatsink is chosen as 15 K. This results in that the temperature of the outlet water will be maximum 55 °C in worst case.

In order to make the power stage as simple as possible, two IGBTs and two diodes have been mounted on a single heatsink. Hence, there will be three heatsinks in the system, and the power loss on each heatsink will be 4.0 kW. This yields to that each heatsink has a thermal resistance of maximum 3.75 K/kW for a temperature rise of maximum 15 K. In result, the two constraints in the selection of the heatsinks will be as follows:

- The dimensions of the heatsink will be suitable (>320mm x >280mm) for mounting of two IGBT and two diode modules.
- It should have a thermal resistance < 3.75 K/kW.

To meet these objectives, an aluminium made heatsink from DAU [106] has been chosen as the heatsink to be used in the application prototype of the CSC based APF. The chosen heatsink, AKW-300-385 has thermal resistivity and pressure drop versus flow rate curves as given in Figure 4.20. It has a thermal resistance of 3.30 K/kW, and 0.62 bar pressure drop for a coolant flow of 20 l/min. Therefore, the cooling system, which will transfer the heat from heatsinks to the air, should have a total flow of minimum 60 l/min to obtain the required thermal characteristics. A sample photo, and an engineering drawing of the chosen heatsink are given in Figure 4.21.

Since there is no raw water to be used for transferring the heat in the LRT system, the cooling system has been designed as to have a water-to-air heat exchanger. As given above, the heat exchanger of the cooling system should have a capacity of minimum 12.0 kW, and the pumps

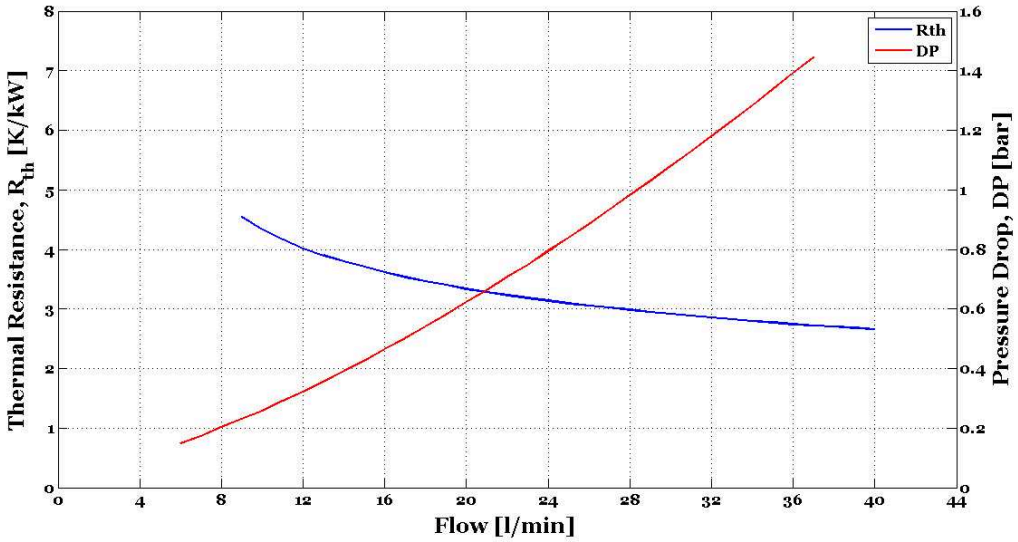
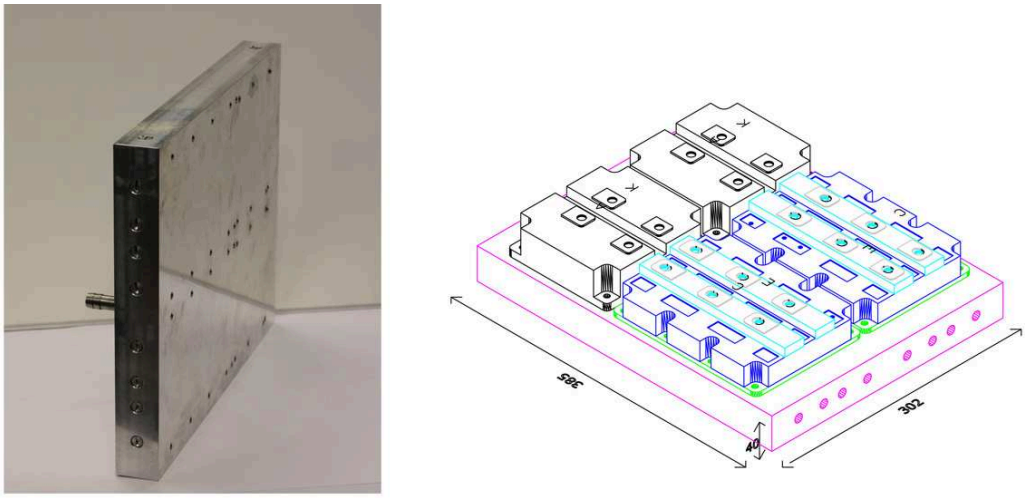


Figure 4.20: Thermal resistance and pressure drop of the heatsink versus flow rate



(a) (b)

Figure 4.21: Chosen heatsink (AKW-300-385) (a) Sample picture (b) Engineering drawing showing the mounting of IGBTs and diodes

Table 4.6: Technical specifications of the cooling system

Technical Specification	Rating/Type
Cooling type	Water-to-air heat exchager
Max. ambient temperature	45 ° C
Min. ambient temperature	-10 ° C
Coolant	Water and glycol
Max. pressure drop	2.0 bar
Min. water flow	60 l/min
De-ionization	NA
Particle filter	80 μ
Pumps	2 (one redundant)

of the cooling system should have a flow of minimum 60 l/min with a total pressure drop of 2.0 bar in the system, which is chosen higher than it would be for providing a flexibility in the system during operation. If the total pressure drop is <2.0 bar, then flow can be adjusted by using of valves. From the considerations given above, a cooling system, having the technical specifications as in Table 4.6, has been chosen for the application prototype.

The temperature rise in the coolant (water) for a dissipation of 12.0 kW , and a flow of 60.0 l/min is given by

$$\Delta T = \frac{Q_{cal}}{m_w \cdot c_w} = \frac{10309}{3600} = 2.86\ K \tag{4.22}$$

where ΔT is temperature rise in the water, Q_{cal} is the total energy in kcal, m_w is the mass of the water in kg, and c_w is specific heat constant of the water in kcal/(kg-K). Therefore, in order to meet the design criterion of maximum 55 °C outlet water temperature, inlet water should be 55-2.86=52.14 °C. For that reason, the capacity of the water-to-air heat exchanger was chosen as to have a temperature difference of < 7.14°C between the temperatures of outgoing water and the ambient, which is specified as 45 °C maximum.

The cooling system has been designed as to be fully outdoor unit in order to save from space. Hence, all the fans, pumps and the heat exchanger has been installed on the roof of the building, in which the APF has been established. The process diagram and the sample drawings of the outdoor cooling system are given in Figures 4.22 and 4.23.

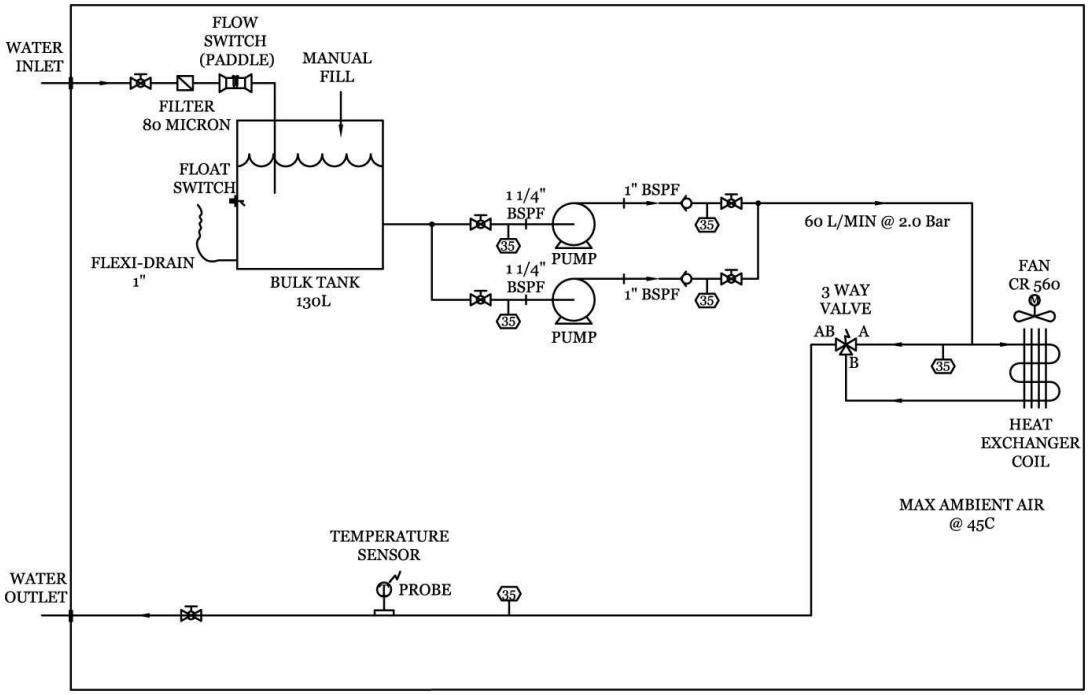


Figure 4.22: Process diagram of the outdoor cooling system

4.9 Design of Power Stage

As the fact that CSC is dual of the VSC, the commutation between the devices occurs in a path at the ac side of the converter [30, 76]. For that reason, the inductance in this commutation path should be as low as possible to avoid the stress on the semiconductor devices due to the transient over voltages during switching instants. However, unlike VSC, the rate of rise of the current during commutation period has to be below some certain values, which are mainly dictated by the series diodes used in the circuit. For a reliable operation, di/dt of the current in the commutation path should be below than that of the diode, which is defined in the RRSOA (Reverse Recovery Safe Operating Area) characteristics. There are three main actors defining this di/dt: diode characteristics, inductance in the commutation path, and the switching behavior of the IGBT. In order to keep di/dt value at a safe value, either the inductance of the commutation path will be increased, or the IGBT will be switched-on slowly, as given in (4.23).

$$\frac{di}{dt} \propto \frac{1}{L_c \; t_{on}} \tag{4.23}$$

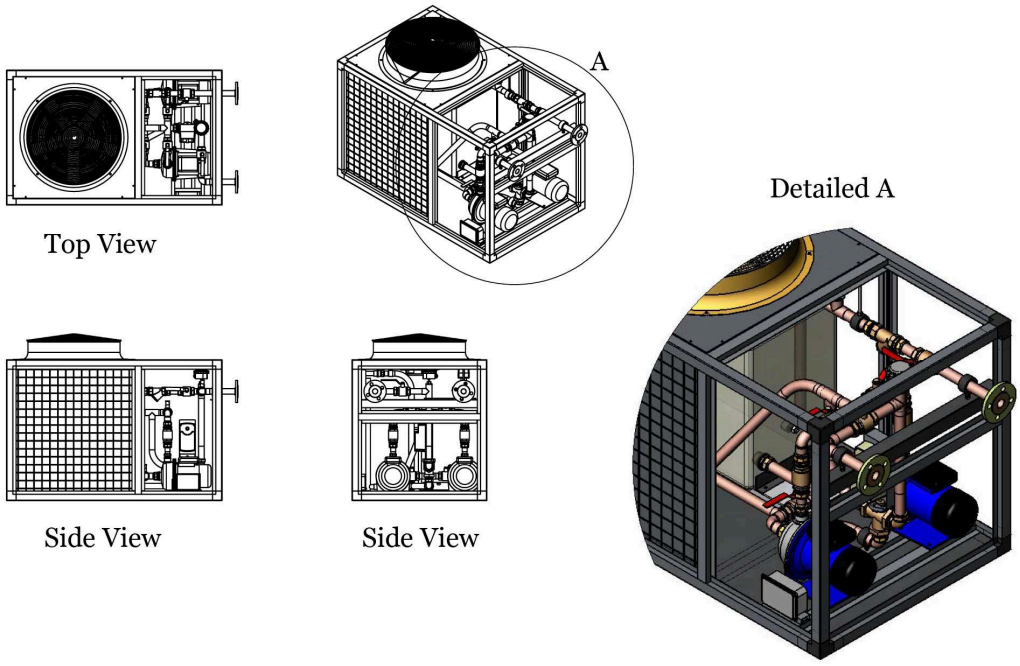


Figure 4.23: Sample drawings of the outdoor cooling system

where L_c is the total stray inductance in the commutation path, and t_{on} is the turn-on time of the IGBT, which can be adjusted by the gate drive circuit. Since each switch consists of two semiconductors, one IGBT and one diode, the stray inductance in the commutation path reaches to some certain values (in practice > 300 nH) unavoidably. Hence, further increase in this inductance would result in higher over voltages. To avoid this and keep the ac side inductance as low as possible, the procedure given below should be followed in the power stage design of the CSC based APF.

- Use special power electronic capacitors having low self-inductances.
- Keep the overall layout of the power stage as compact as possible.
- Keep the commutation path as short as possible by mounting the upper and lower switches as grouped.
- Keep the ac side conductors as close as possible by using laminated busbars.

A diagram showing the layout of the semiconductor devices and the filter capacitors in the application prototype of the CSC based APF is given in Figure 4.24, in which the anti-parallel

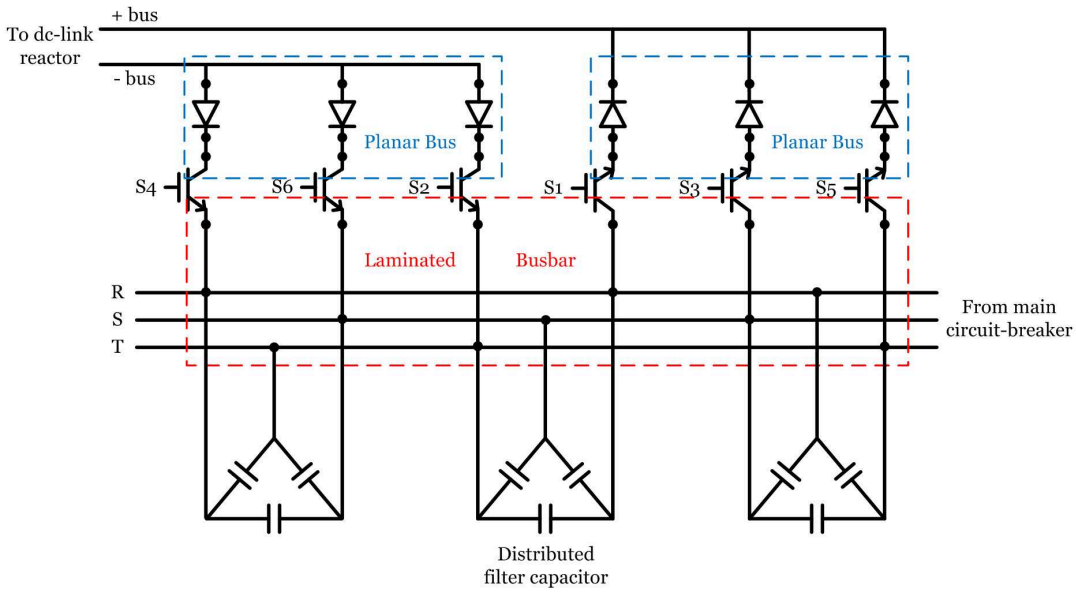


Figure 4.24: Layout of the semiconductor devices and filter capacitors

freewheeling diodes of the IGBTs are not shown for simplicity. Besides, in Figure 4.25, a sample photo showing the power stage of the implemented CSC based APF is given.

As it is seen from Figure 4.24 that all the steps given above have been followed during the design stage of the CSC based APF, and tried to keep the inductances in the commutation path as low as possible. Since the layout is fixed, thus the stray inductances in the commutation paths are fixed, the final step is measuring the stray inductances and di/dt values for different commutation paths at rated voltage and current. For this purpose, the switching tests have been performed on the test circuits as given in Figure 4.26. Since the busbar is not symmetric with respect to the IGBTs grouped as upper and lower ones, switching tests have been performed for different commutation paths, especially for the largest loops, e.g S1 and S5 in the upper group, S4 and S2 in the lower group. Hence, DUT1 and DUT2 vary according to the test carried out. During these tests, the Rg_{on} has been changed in order to see its effect on the di/dt and I_{rr}. Figures 4.27-4.36 show the turn-on and -off characteristics of the devices under tests for different commutation paths. A summary of these tests with the measured values of L_c, di/dt and I_{rr} are given in Table 4.7.

As shown in Figure 4.27 that the stray inductance of the commutation path, L_c is calculated by using the slope of the IGBT current, which corresponds to di/dt of the diode current, and the

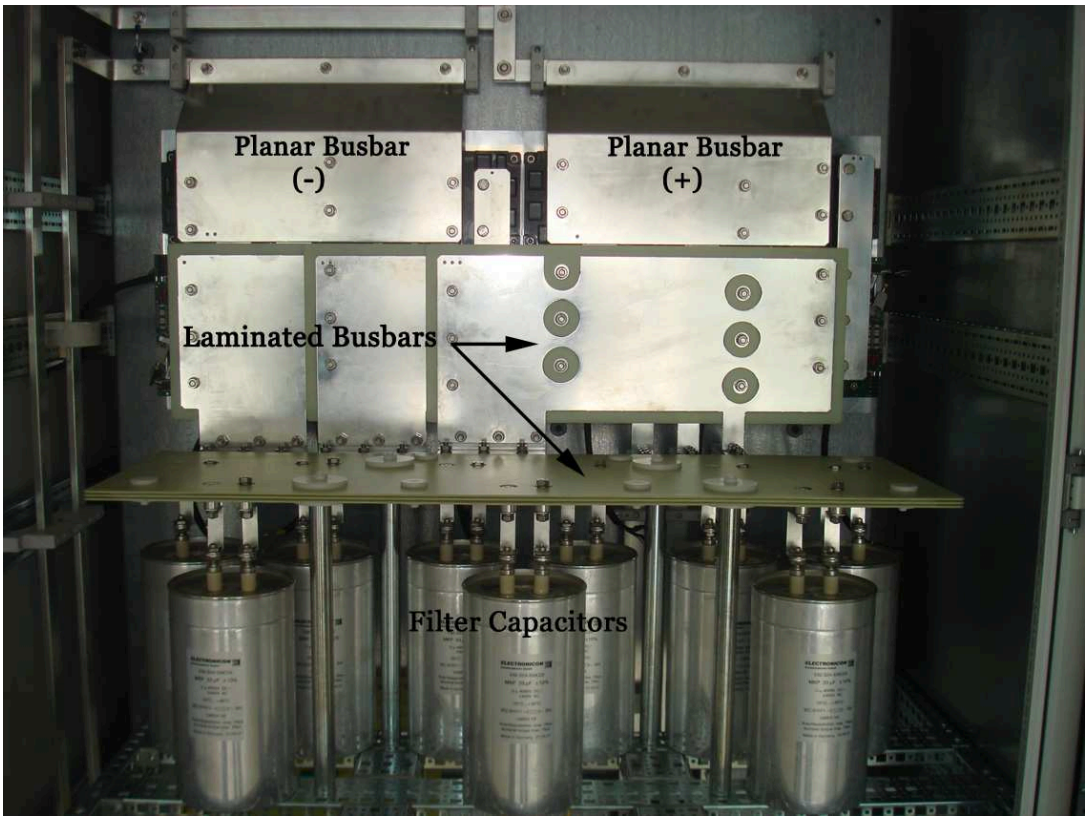


Figure 4.25: A sample photo showing the power stage of the implemented APF

Table 4.7: A summary of the switching tests

Test Conditions					Measured Variables		
DUT1	DUT2	Rgon Ω	Rgoff Ω	Figure	Lc (nH)	di/dt (A/us)	Irr (A)
S1	S5	1.8	3.8	(4.27)	470	2125	570
S2	S4	1.8	3.8	(4.29)	489	2083	550
S3	S5	1.8	3.8	(4.30)	340	3300	800
S1	S5	2.4	3.8	(4.31)	425	2000	545
S2	S4	2.4	3.8	(4.32)	440	1875	500
S3	S5	2.4	3.8	(4.33)	336	3000	720
S2	S6	2.4	3.8	(4.34)	376	2500	580
S1	S5	3.0	3.8	(4.35)	480	1665	480
S3	S5	3.0	3.8	(4.36)	375	2800	650

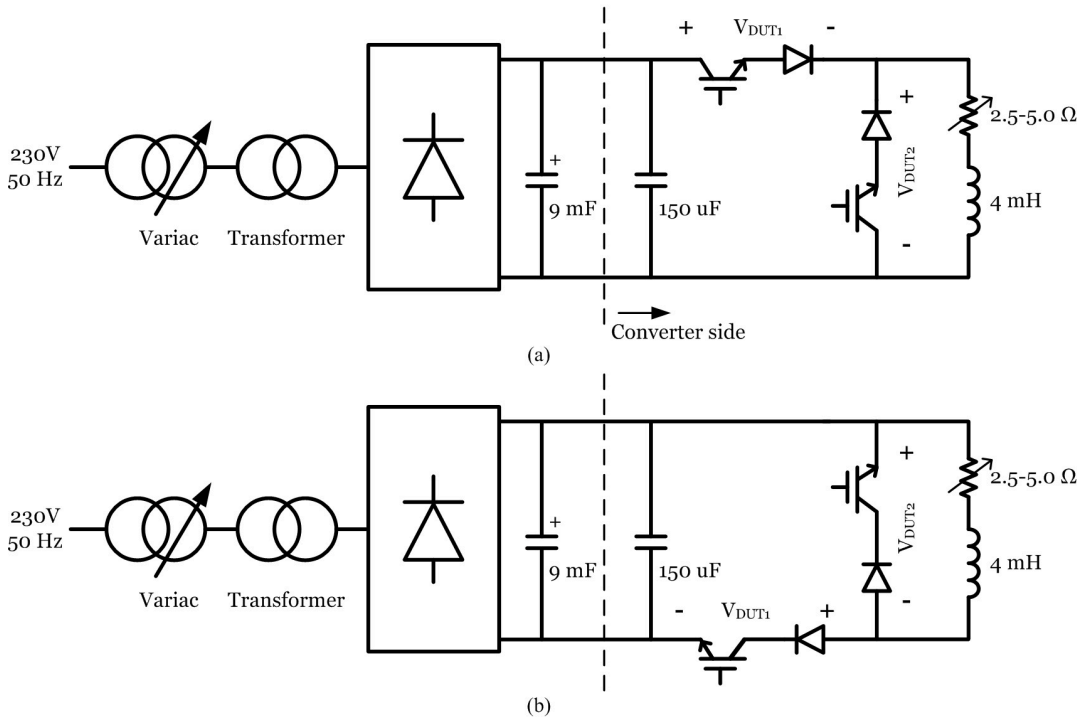


Figure 4.26: Simplified diagram of the switching test circuits (a) Test circuit for upper IGBTs (b) Test circuit for lower IGBTs

voltage drop, ΔV up to the instant at which the IGBT voltage is broken, or remains constant. Besides, I_{rr} is shown as the current, which is from the test/nominal current to the peak current of the IGBT. All the tests have been carried out for 1400-1500 V dc voltage, and 400 A dc current. It is seen from Table 4.7 that, as the Rg_{on} increases, both the di/dt and the I_{rr} of the diode decrease at expense of turn-on losses as expected. Because, as the Rg_{on} increases, the turn-on time of the IGBT also increases. In the technical specifications of the diode di/dt is given as <3000 $A/\mu s$ in the figure of RRSOA. Hence, in order to keep the diode in a safe region during normal operation at rated voltage and current, Rg_{on} is chosen as to be 2.4 Ω in view of the switching test results.

Another issue about the switching behavior of the IGBTs is the transient over voltages during turn-off. As described in [30], there are two commutation types for the turn-off process of the IGBT: forced turn-off, and load turn-off. In the forced turn-off, the current carrying IGBT can be successfully turned-off by applying an OFF signal to its gate driver. In the load turn-off, the current carrying IGBT, which is still receiving turn-on signal, can be successfully turned-off due to the another IGBT turned-on in the same circuit. Hence, outgoing IGBT is turned-off

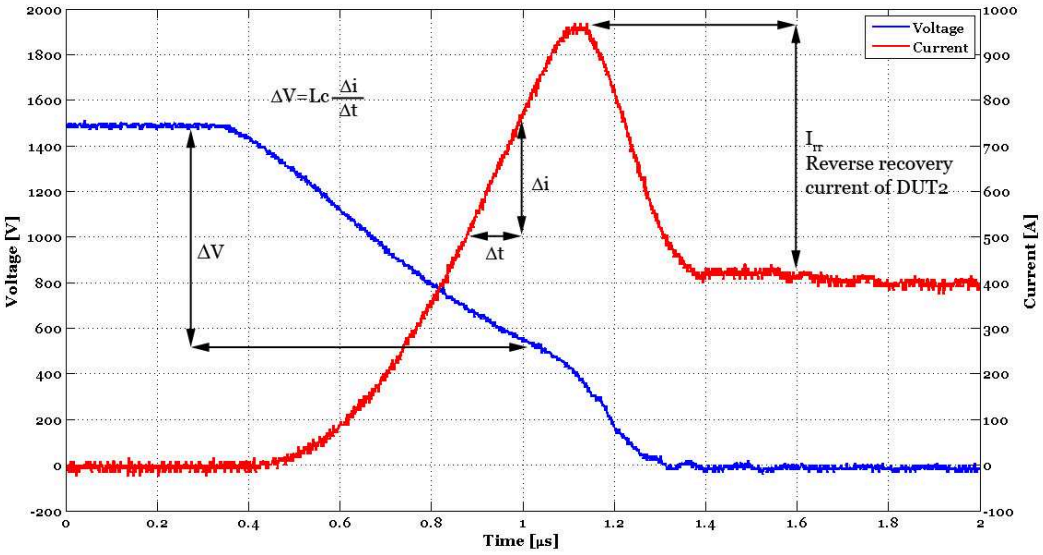


Figure 4.27: Turn on characteristics for DUT1=S1, DUT2=S5 and Rg_{on}=1.8 Ω (*Laboratory data*)

as a result of the turn-on of the incoming IGBT. For a complete analysis, the voltage stress on the IGBTs during these commutations should also be considered. In the load turn-off, the outgoing IGBT is turned-off according to the turn-on behavior of the incoming device, and the diode RR characteristics, and at that instant, the reverse voltage is blocked by the diode. Thus, the IGBT voltage is zero during this turn-off. In the forced turn-off, all the process is dictated by the behavior of the IGBT, and the stray inductance of the circuit. For that reason, the IGBT voltage during the forced turn-off should be kept at a value, which is safe for IGBT. Forced turn-off process for DUT1=S1 and DUT2=S5 is given in Figure 4.28. It is seen that there is only an overshoot of 285 V, and total peak voltage seen on the IGBT is 1800 V, which is far below the nominal voltage (3300V) of the IGBT. Hence, there is no need to adjust the Rg_{off} of the driver.

4.10 Design of Protection Circuits

In CSC applications, some special protection circuits, which are characteristic only to CSCs, should be used as well as the usual protection circuits or devices for protection of the CSC against overcurrents, and overvoltages. In order to achieve these tasks, the common approach is using the standard protection relays both in MV ad LV applications. Since the operating

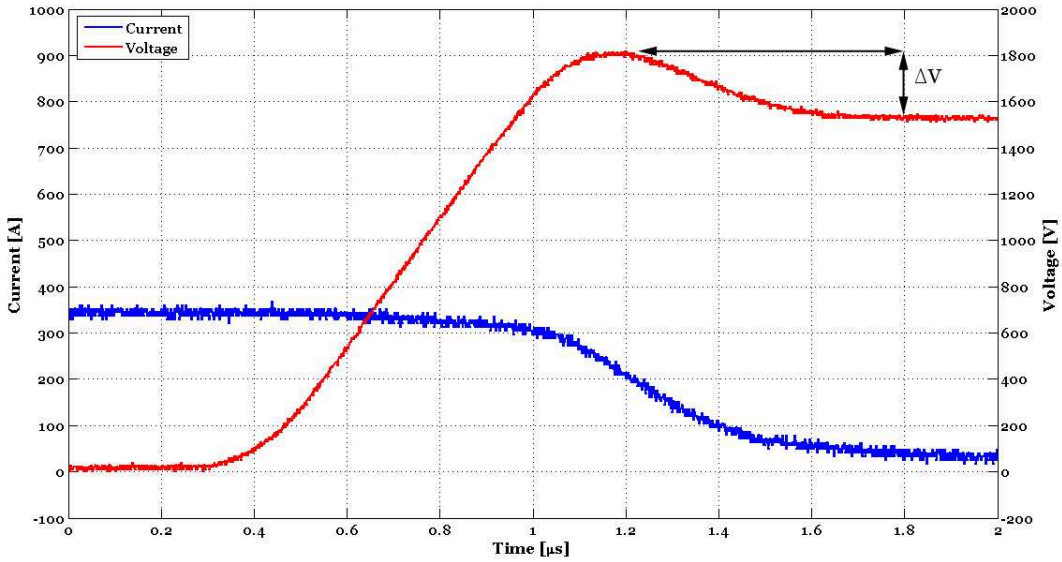


Figure 4.28: Turn off characteristics for DUT1=S1, DUT2=S5 and Rg_{on}=1.8 Ω (*Laboratory data*)

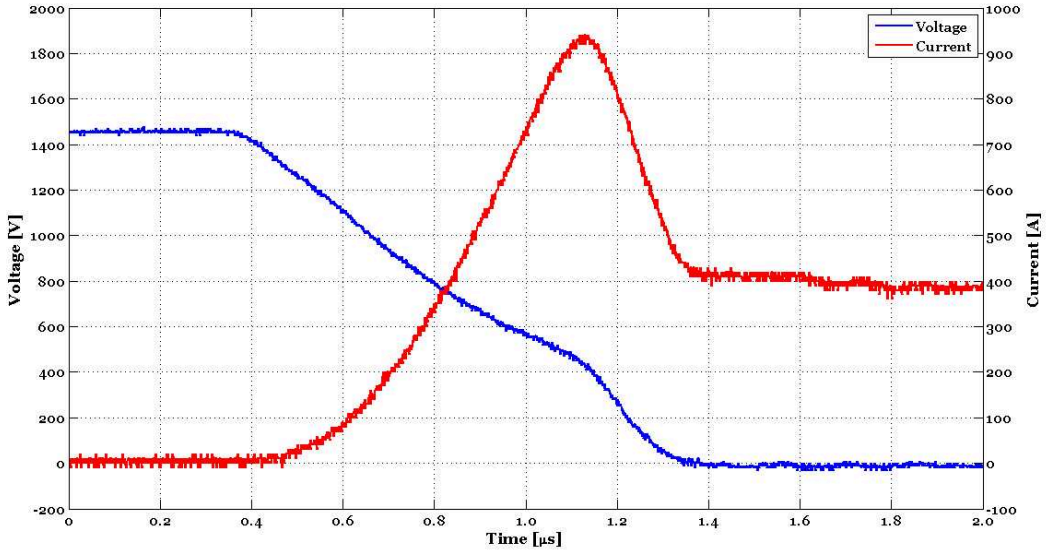


Figure 4.29: Turn on characteristics for DUT1=S2, DUT2=S4 and Rg_{on}=1.8 Ω (*Laboratory data*)

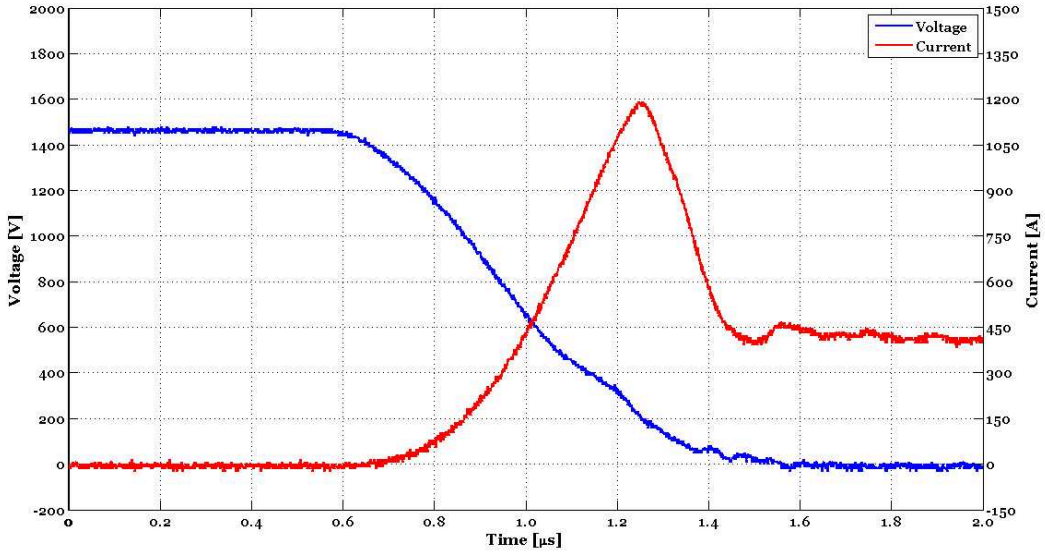


Figure 4.30: Turn on characteristics for DUT1=S3, DUT2=S5 and Rg_{on}=1.8 Ω (*Laboratory data*)

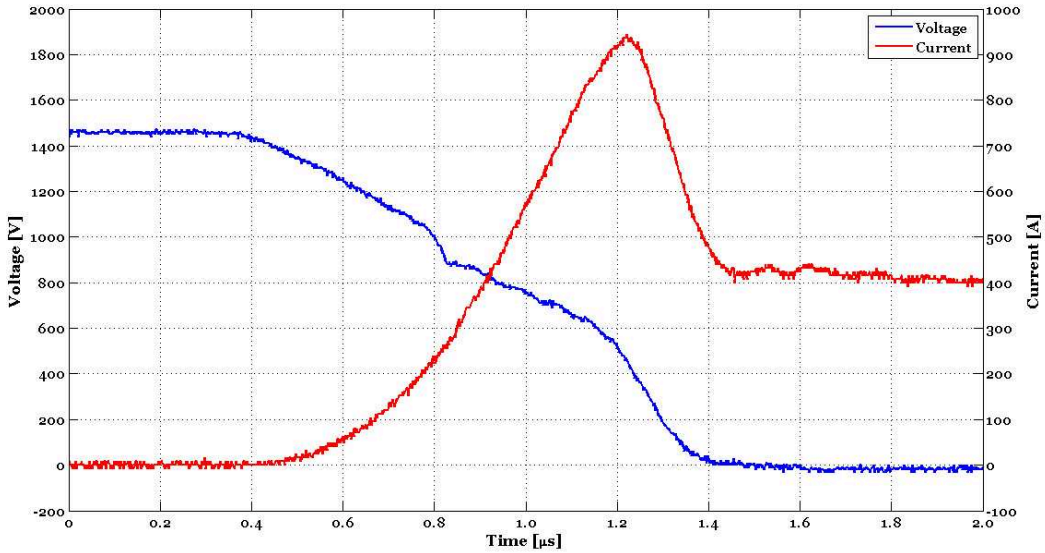


Figure 4.31: Turn on characteristics for DUT1=S1, DUT2=S5 and Rg_{on}=2.4 Ω (*Laboratory data*)

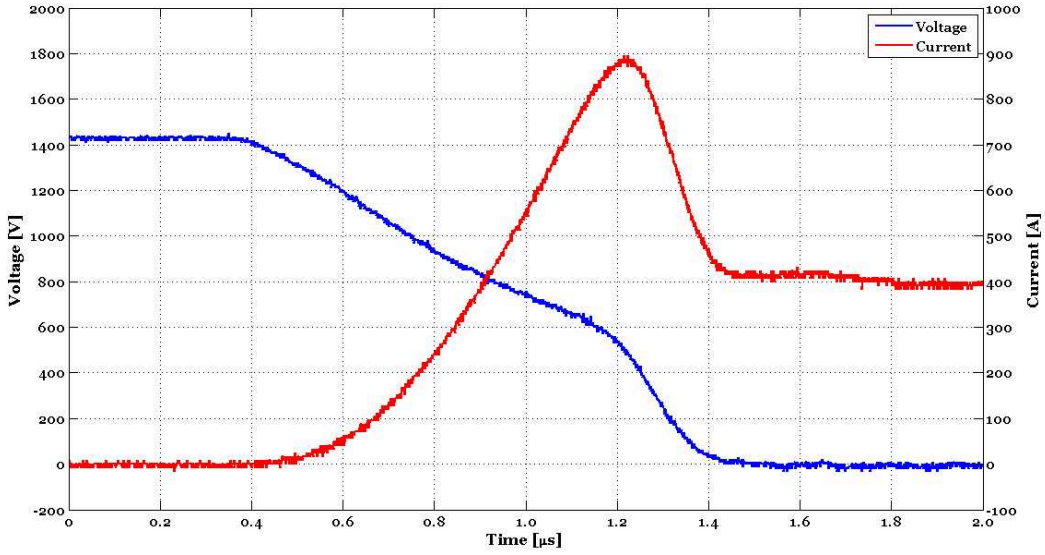


Figure 4.32: Turn on characteristics for DUT1=S2, DUT2=S4 and Rg_{on}=2.4 Ω (*Laboratory data*)

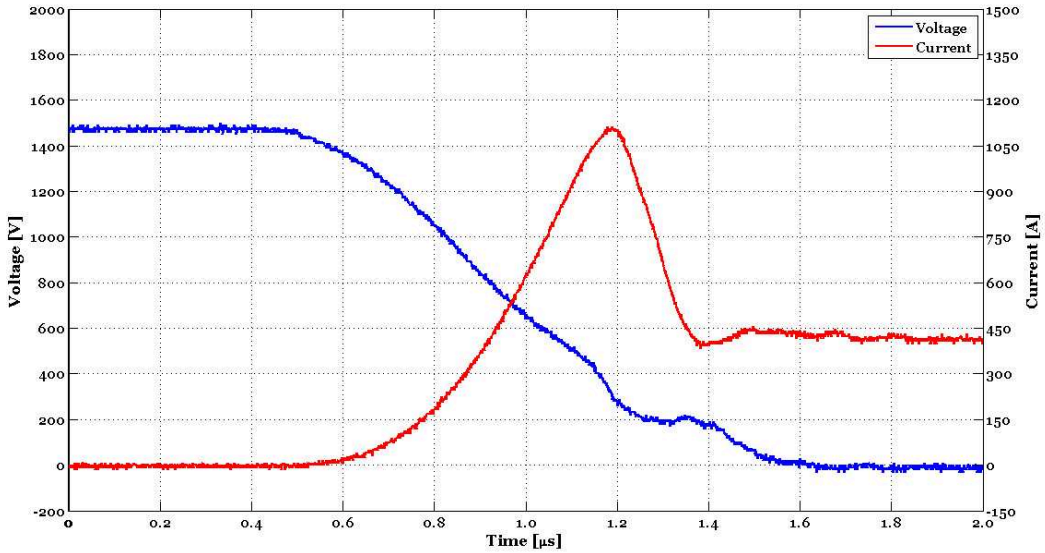


Figure 4.33: Turn on characteristics for DUT1=S3, DUT2=S5 and Rg_{on}=2.4 Ω (*Laboratory data*)

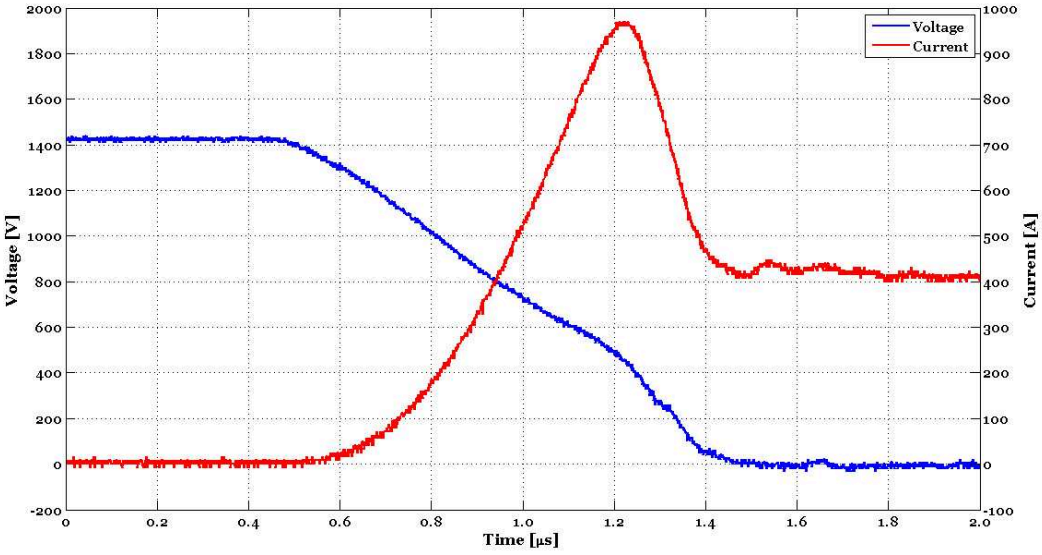


Figure 4.34: Turn on characteristics for DUT1=S2, DUT2=S6 and Rg_{on}=2.4 Ω (*Laboratory data*)

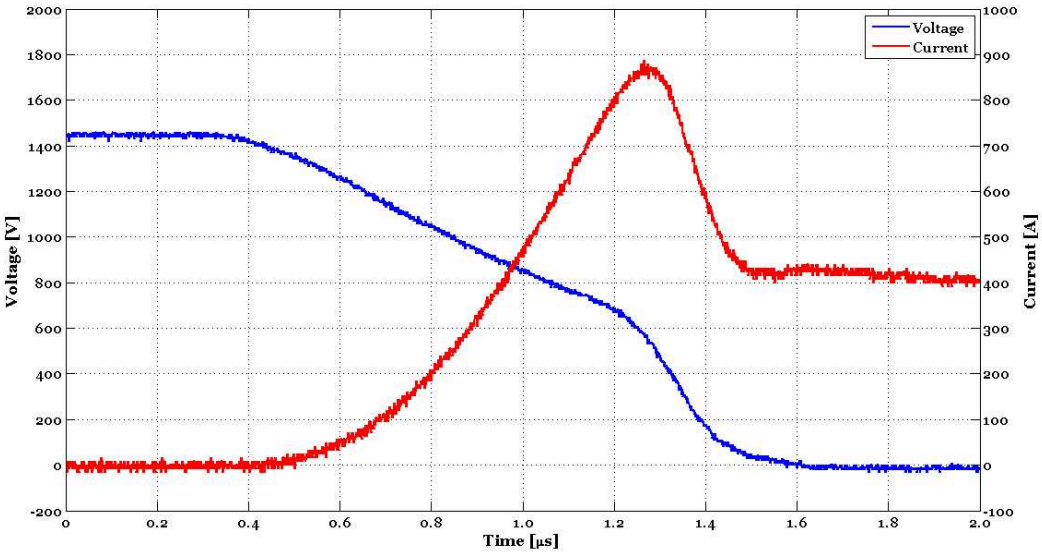


Figure 4.35: Turn on characteristics for DUT1=S1, DUT2=S5 and Rg_{on}=3.0 Ω (*Laboratory data*)

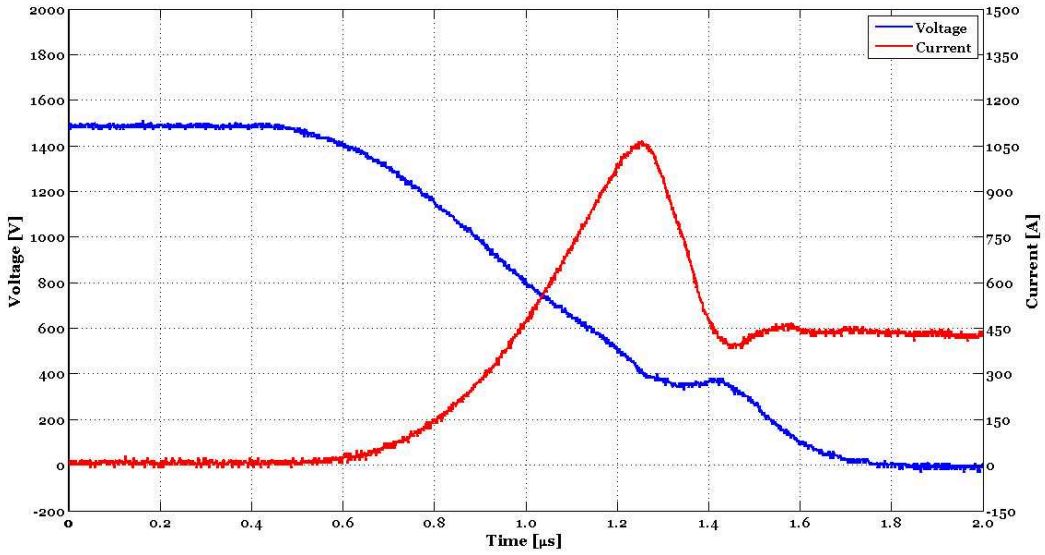


Figure 4.36: Turn on characteristics for DUT1=S3, DUT2=S5 and Rg_{on}=3.0 Ω (*Laboratory data*)

voltage of the APF was specified as 1.0 kV, semiconductor devices have been chosen according to this design value. Hence, in case of an overvoltage at the MV bus, the CSC based APF should not be operated, or disconnected from the 1.0 kV bus. For this purpose, an ”Over/under voltage relay” has been used, and MV and LV circuit breakers are switched off by use of a trip signal coming from this relay as shown in Figure 4.37. In addition to the this relay, LV bus voltage is also monitored by the control system of the APF, and in the cases of under and over voltage, CSC is stopped, and LV circuit breaker is switched off.

In order to protect the overall system from excessive currents in case of a severe fault, the CSC based APF has been equipped with an ”Over current relay”. Any short circuit either at MV or LV side is sensed by this relay, and a trip signal is generated to switch off all circuit breakers in the system. Not only for the over current, but also a protection for the over loading of the CSC due to possible faults in the system should be employed. The overload protection of the APF have been mainly achieved by two mechanisms: (i) the control system of the APF, which occupies both analog and digital protections for this purpose, (ii) the LV circuit breaker, which has been also equipped with both over current and over load protection properties [107].

As an inherent property of the CSC, there is no risk of a short circuit at the dc side of the converter and, if there were no loss of control (in view of switching of semiconductor devices), all the current should circulate through the dc-link reactor. Hence, dc-link current should be

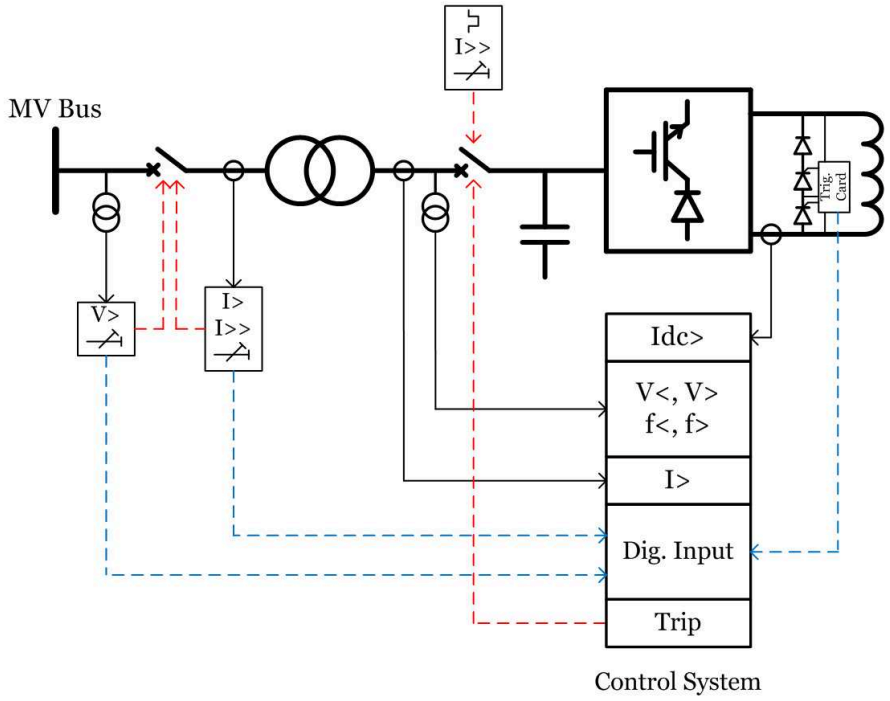


Figure 4.37: Protection circuits in the CSC based APF

monitored, and the system should be protected against any possible over current at the dc-link, which is also flowing through the semiconductor devices. For this reason, Hall Effect Current Transducers [108] have been used in order to sense the dc-link current accurately, and without any delay. The dc-link over current protection has been achieved by the control system by employing both analog and protection circuits.

A special protection, which is characteristic to CSCs, is the over voltage protection at the dc-side of the converter. If the dc-link current is interrupted suddenly, the dc-link voltage goes to a negative very high voltage as a result of the stored energy in the dc-link reactor. This over voltage may yield to failures in the semiconductor devices, and unrecoverable faults in the system. In order to avoid this overvoltage and protect the CSC, an overvoltage protection circuit, also referred to as crowbar circuit, has been used in the application prototype as shown in Figures 4.38 and 4.39. It is composed of two pieces of 3300V asymmetric fast-turn on thyristor (WESTCODE A1080LC330), for making sure of a reliable operation with high dv/dt values, and a 4500V fast recovery diode (WESTCODE M0659LC450). The thyristors are triggered by a self-triggering mechanism without need of an external power supply.

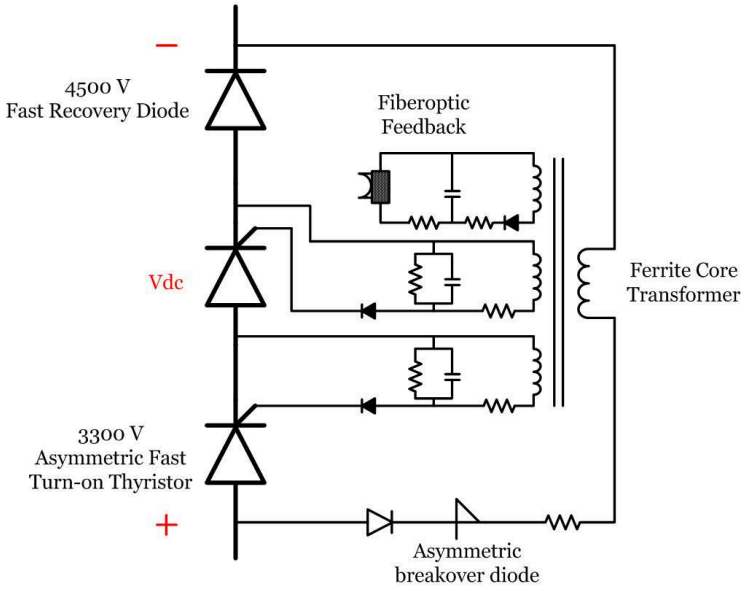


Figure 4.38: Circuit diagram of the implemented crowbar

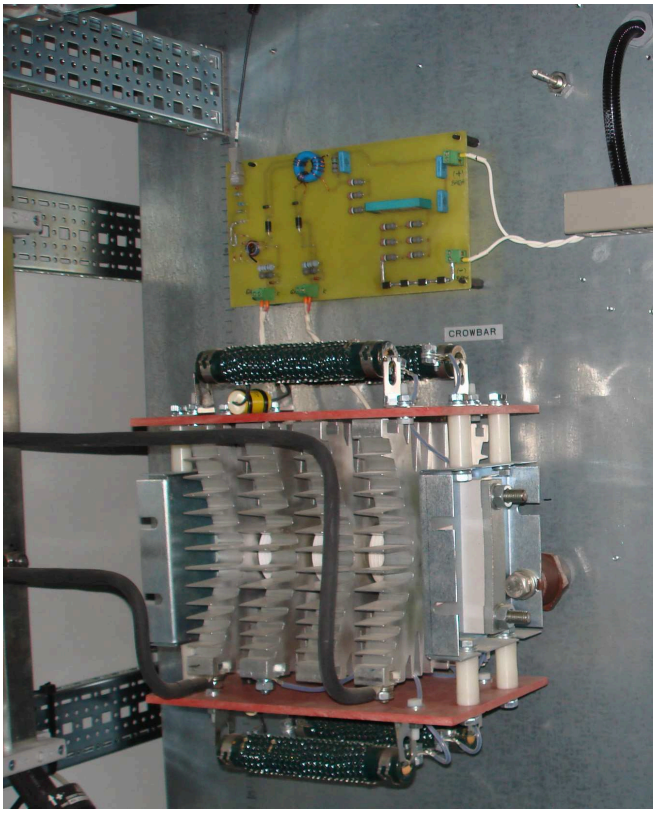


Figure 4.39: A sample picture of the implemented crowbar

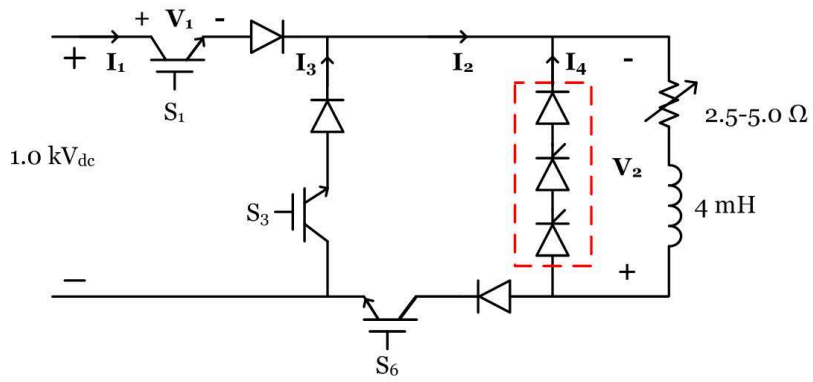


Figure 4.40: Circuit diagram of the crowbar test setup

When the dc-link voltage exceed the design value of 2500 V, the break-over diode shown in Figure 4.38 turns on, and triggering circuit sends a firing pulse to each thyristor with sufficient magnitude. Besides, a feedback signal is sent to the control system via fiber optic interface, which is integrated into the triggering circuit. The control system blocks the gate signals of the IGBTs, and sends a trip signal to the LV circuit breaker upon the receipt of the feedback signal. For any fault signal, the firing circuit in the control system blocks the gate signals of the switches S1, S3, S4, and S6; and sends a turn-on signal to the switches S5 and S2 for freewheeling operation.

Before the implementation of the CSC based APF in the LRT system, crowbar circuit was tested by a setup as shown in Figure 4.40. In this test, the dc-link current is built-up first by turning on the switches S1 and S6, thus applying 1000 Vdc to the dc-link. As the current reaches to 200 A, S3 is turned on, and with a delay, S1 is turned off. When the converter is in freewheel operation, S3 is also turned off, and the dc-link current is interrupted. At this instant, dc-link voltage with a sign as shown in Figure 4.40 starts to rise up until the protection mechanisms operate.

In Figures 4.41-4.43, voltage and current waveforms of the corresponding devices are shown as signed in Figure 4.40. It is seen that until the crowbar circuit operates, the voltage across the device S1 exceeds 2400 V, the active-clamp feature of the driver acts, and turns the IGBT (S1) on to protect the device from this overvoltage. After the operation of the break-over diode, with a delay of about 1 μsec, dc-link current is transferred from S1 to the crowbar, and decays to zero in this path.

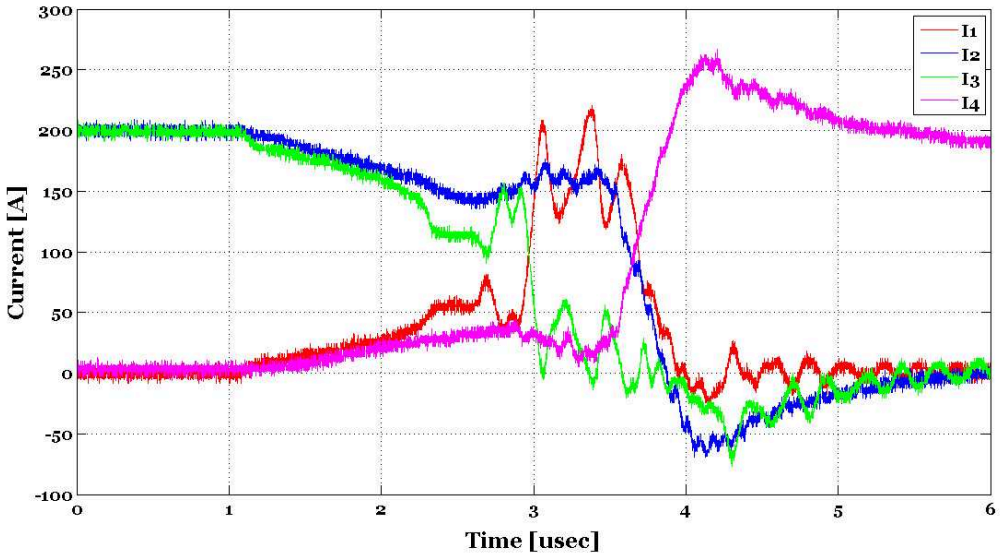


Figure 4.41: Recorded waveforms during crowbar operation (*Laboratory data*)

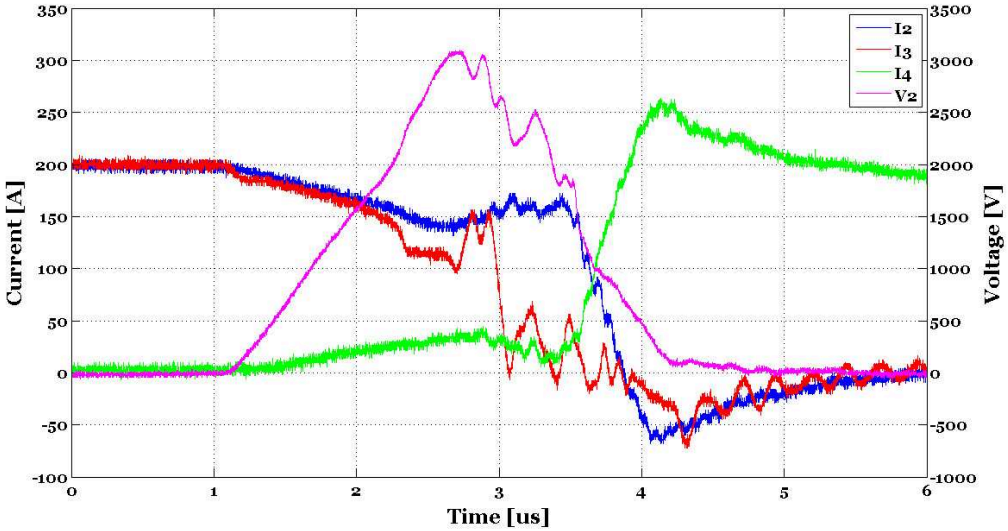


Figure 4.42: Recorded waveforms during crowbar operation (*Laboratory data*)

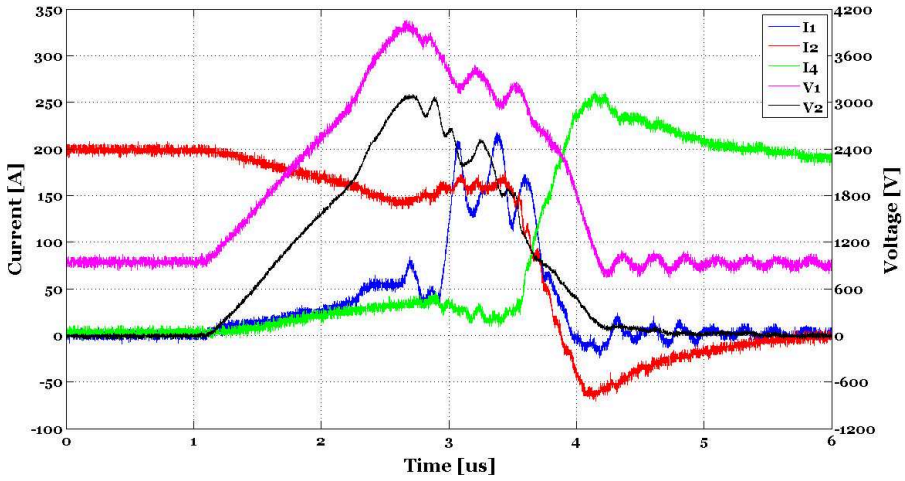


Figure 4.43: Recorded waveforms during crowbar operation (*Laboratory data*)

4.11 Design of the Control System

The control system of the CSC based APF includes the reference current generation, waveform modulation, monitoring and protection circuits, which are being performed by four fundamental units: (i) Digital Signal Processor (DSP) Board, (ii) Firing Board, (iii) Protection Board, and (iv) Programmable Logic Controller (PLC).

DSP Board performs almost all critical jobs such as reference current generation, waveform modulation, dc-link control/protection, and over load protections. As described in the previous chapter, the control of the CSC based APF is based on two main tasks, which are the reference current generation and the waveform modulation. These are implemented on a 150 MHz floating point micro-controller, F28335 which is a member of the C2000 family of the Texas Instruments [109]. A development board [110] of the F28335 has been mounted on the DSP Board, which also provides necessary signal conditioning and analog protection facilities as shown in Figure 4.44. All the current and voltage signals, either coming from conventional transformers or hall effect sensors, are firstly transferred to an appropriate voltage level (±10V), and then sent to the DSP Board, in which signals are filtered (if necessary), scaled, and shifted to fit into the input voltage range of the DSP, that is 0-3V. Each analog signal is sampled at every 40 μsec, and all calculations are made in this time period. At each end of the 40 μsec, reference current vectors, and hence corresponding switching signals are updated. The switching signals calculated by DSP are then forwarded to the Firing Board.

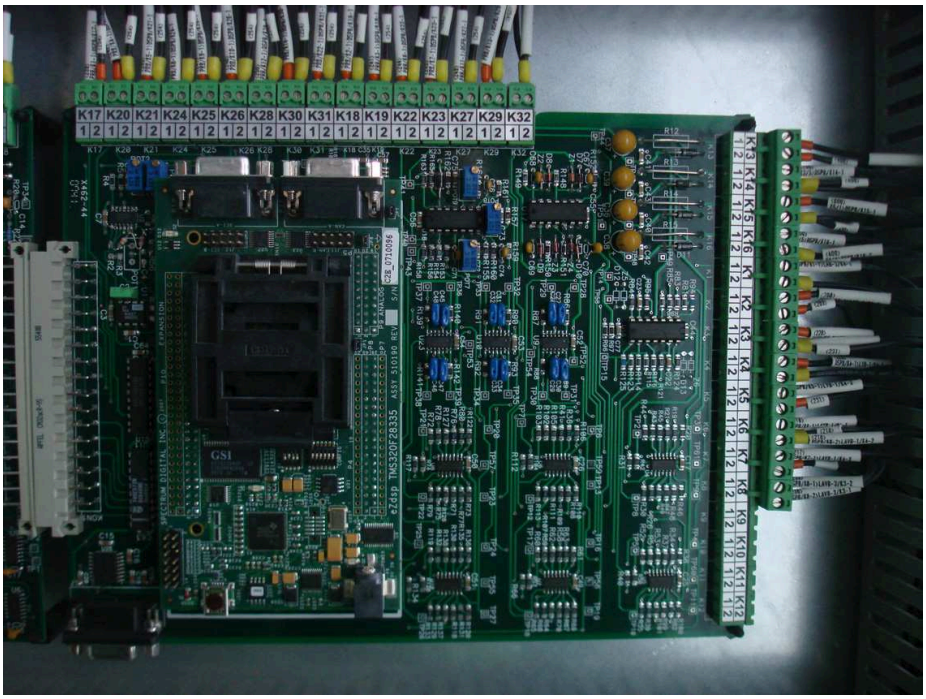


Figure 4.44: DSP Circuit Board

Firing Board is employed to achieve the signal conditioning of the gate signals of the IGBTs coming from DSP, and to implement an extra analog protection for blocking of switching signals and establishing freewheeling path in case of any fault. The global fault signal, and status signals of the gate drivers, which are transmitted at each ON and OFF pulse with a duration of $< 2\mu sec$, are used in the Firing Board to establish a further analog protection. In case of a fault, a device failure, or the loss of control due to DSP, analog circuit operates, and makes sure the continuous operation of the dc-link current with a suitable freewheeling path. Hence, in any case, one IGBT from upper group, and one IGBT from lower group receive ON signals from Firing Board. Besides, another important task, turn-off delay, is also done by the Firing Board. Each signal coming from DSP is delayed about $4\mu sec$ at its falling edge to wait the turn-on process of the incoming device. Firing Board transmits the gate signals, and receives the status signals of the IGBTs via fiber optic link as shown in Figure 4.45.

Protection Board is responsible from taking all fault signals, which are either internal or external, and generating a global fault signal in case of a fault, thus making sure of the proper shut-down of the system. Global fault signal is also forwarded to DSP Board, Firing Board, and PLC. Another important task of the Protection Board is latching the fault signals even

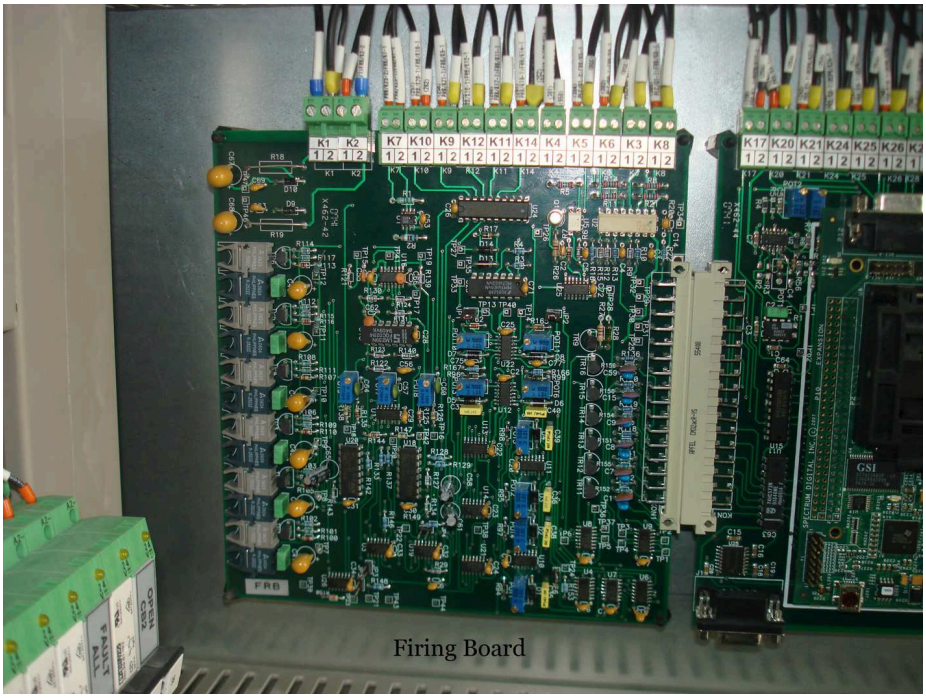


Figure 4.45: Firing Circuit Board

they have a very short pulse duration. By this way, as the global fault signal is HIGH, Firing Board generates switching signals required for freewheeling by analog circuits despite of the DSP PWM outputs. This latching time is adjusted as 2 seconds. All the inputs and the outputs of the Protection Board have opto-couplers for isolation, and noise immunity as shown in Figure 4.46.

In addition the control boards described above, a PLC, which is a member of the S7-200 family of Siemens, is used mainly to implement a Human Machine Interface (HMI) with an Liquid Crystal Display (LCD) based Control Panel from MP77 family of Siemens. PLC also controls the auxiliary equipments such as circuit breaker/s, and cooling system. All the operations, and faults in the system are stored in the internal memory of the Control Panel.

4.12 Summary

In this chapter, design principles of an application prototype of the CSC based APF have been presented. Design of the prototype APF has been accomplished according to the needs of an actual system, which is a Light Rail Transportation (LRT) system characterized by 12-

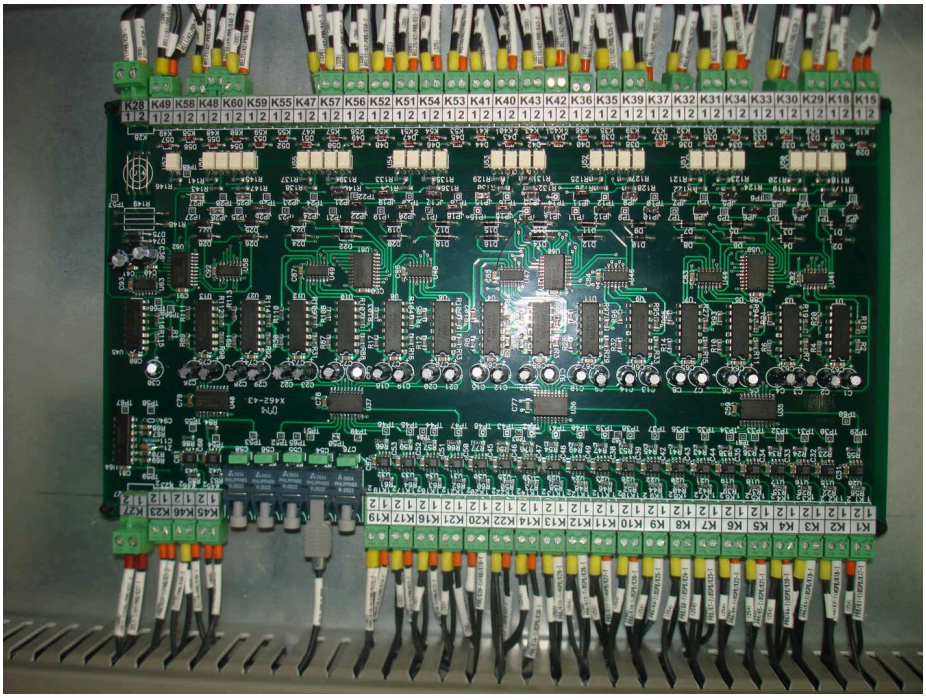


Figure 4.46: Protection Circuit Board

pulse uncontrolled rectifiers fed from MV bus. First of all, load has been identified by the PQ measurements performed in the field, and then, technical specifications of the CSC based APF have been stated by taking into account the constraints arising from the needs of the LRT system as follows:

- suppressing the 11^{th} and 13^{th} current harmonics of the load, which are exceeding the limit values specified in IEEE Std.519-1992
- connecting the APF to the MV bus via an existing coupling transformer of 34.5/1.1 kV
- avoiding the injection of any capacitive reactive power to the network

In view of these specifications, firstly, input filter design, which is an important part of the proposed SHAM, has been explained. It has been shown that the amplification property of the input filter at some pre-selected frequencies can be used in a useful manner, and the rating of the CSC can be reduced significantly for the same APF rating. In this manner, selection of f_o has been discussed, and the requirements for the amplification of 11^{th} and 13^{th} harmonic components have been stated. The necessity of choosing f_o as >650 Hz with a sufficient

safety margin has been also explained. After choosing the f_o as to be 780 Hz, calculations for the determination of the filter inductance and capacitance values have been presented. It has been also shown that there is no need for an extra series filter inductance, and hence, the leakage inductance of the coupling transformer is sufficient for this purpose because of the moderate reactive power demand of the filter capacitors, that is only 94.25 kVAr. Besides, design criterion for the selection of the carrier frequency has been given in view of harmonic standards, and it was chosen as to be 3.0 kHz according to the gain response of the designed input filter.

Since it is always stated as the main disadvantage of the CSCs, keeping the dc-link reactor and the current as low as possible is an important design issue. For this purpose, dc-link current has been determined firstly by the help of simulation results according to the specified 11^{th} and 13^{th} harmonic components of the load current. In result, dc-link current was chosen as to be 300 A. In order to determine the value of the dc-link reactor, an analysis work has been accomplished to calculate the total energy, which has to be stored in the dc-link reactor for the circulation of instantaneous power at harmonic frequencies. By this analysis work, the value of the dc-link reactor was found as to be 4.0 mH.

Another important point in the SHAM is the active damping method, which is proposed to use the amplification property of the input filter as suppressing the undesired harmonic components around f_o effectively. Since active damping method is also based on selective harmonic extraction method, any attenuation of the 11^{th} and 13^{th} harmonic components are avoided. In order to optimize the virtual damping resistor, or damping gain, simulations have been carried out both in Matlab and EMTD/PSCAD. By this way, the optimum damping gain has been determined in view of the chosen dc-link current and satisfactory suppression of the oscillations around f_o.

Since the application prototype of the CSC based APF is connected to the MV bus via an existing coupling transformer, the operating voltage of the APF is dictated by this transformer. Hence, the semiconductor devices to be used in the CSC based APF should be selected according to this voltage, that is 1.0 kV, and the value of dc-link current, that is 300 A. For this purpose, candidate semiconductor devices have been compared, and among them, a 3300 V, 1200 A HV IGBT module from Mitsubishi has been chosen with a suitable fast-recovery HV diode module. After that, the conduction and switching losses in the converter have been

calculated according to the technical specifications of the chosen semiconductors and theoretical current and voltage waveforms for the rated operation of APF. Total loss in the converter has been found as 12.0 kW, and the cooling system has been chosen as to be a water cooling system in order to save from space, and transfer the generated heat outside of the building, in which the APF has been installed. The aluminium made heatsinks have been chosen as to have a thermal impedance of <3.5 K/kw, which provides a junction temperature of 90 °C for IGBTs at maximum 55 °C coolant temperature.

Since the CSC is dual of VSC, inductance in the commutation path on the ac side should be kept as minimum as possible. For this reason, some key points in the power circuit (and layout) design have been introduced. It was shown that although these key points have been taken into account, the inductance in the commutation path can be decreased down to a certain value, because of the circuit topology of the CSC in nature. Besides, it was also shown that, very low inductance in the commutation path would be not desirable in some cases due to the di/dt limitation of the fast-recovery series diodes. In order to show the effect of the stray inductances in the commutation path, and also effect of the turn-on behavior of the IGBTs on the reverse-recovery current of the diode, switching tests have been performed, and a proper turn-on gate resistance, 2.4 Ω, in the drive circuit was determined for a reliable operation of the diode, which is dictated by the RRSOA of it.

Like in all industrial products, some protection mechanisms have been accomplished for the protection of CSC based APF against over voltages and currents. For this purpose, as well as the conventional protection mechanisms such as over/under voltage and over current relays, some special measures have been taken for the protection of CSC based APF. One of them is the over current protection in the dc-link. This protection has been accomplished by the use of Hall effect current transducers, and analog and digital protection circuits. Besides, another important protection issue is the overvoltage protection of the converter on the dc-side, which is arising from the sudden interruption of the dc-link current. In order to provide this protection mechanism, a crowbar circuit has been designed and implemented. It was also shown that inherent active-clamping feature of the gate drivers act as an overvoltage protection mechanism until the thyristors in the crowbar circuit are triggered.

Finally, control system of the implemented CSC based APF has been introduced with the necessary explanations of the main parts such as control boards, and PLC.

CHAPTER 5

RESULTS

In this chapter, the performance of the proposed control system for the CSC based APF will be verified by experimental work. In the first section, simulation results of the CSC based APF, which is designed in Chapter 4, to solve the harmonic problems of a Light Rail Transportation (LRT) system, will be presented. The simulation work has been performed by using the model, which is constructed in EMTDC/PSCAD as given in Appendix B.

In the second section, theoretical results will be verified by experiments conducted in the field. These field tests have been carried out on the prototype of the CSC based APF, which is applied to Bursaray LRT system. During the field tests, not only the proposed Selective Harmonic Amplification Method (SHAM) has been verified, but also the highlights of the CSC based APF have been presented. The records have been obtained by using of the apparatus as listed in Table 5.1.

Table 5.1: List of measurement apparatus used in field tests

- Tektronix TDS5054 Digital Phosphore Oscilloscope
- Tektronix P5210 High Voltage Differential Probe
- Tektronix P5050 Voltage Probe
- Powertek, Rogowski Current Transducers
CWT 15B (2mV/A), CWT 6B (5mV/A)
- Data Acquisition System
National Instruments DAQCard 6962E Data Acquisition Card
National Instruments SC2040 Sample and Hod Card
Fluke 80i-110s AC/DC Current Clamp

Table 5.2: Circuit parameters of the CSC based APF

APF		
Operating voltage		1.0 kVrms 1-to-1
Supply frequency	f_s	50 Hz
Harmonics to be suppressed		11^{th} and 13^{th}
CSC		
DC link current	i_{dc}	300 A
DC inductance	L_{dc}	4 mH
DC resistance	R_{dc}	7.4 mΩ
Carrier frequency	f_{cr}	3.0 kHz
Input filter (on LV side)		
Inductance	L_f	139 μH
Capacitance	C_f	300 μF
Resistance	R_f	9.1 mΩ
Quality factor	Q_0	75
Gain at 550 Hz	K_{11}	2.05
Gain at 650 Hz	K_{13}	3.35
Load (on MV side)		
11^{th} Harmonic	$I_{11(MV)}$	6.0 Arms
13^{th} Harmonic	$I_{13(MV)}$	4.0 Arms

5.1 Theoretical Results

The results of the simulation work for the proposed CSC based APF will be presented in this section. The circuit parameters of the simulated system in Figure 4.4, are as given in Table 5.2.

Simulation results showing the effectiveness of the proposed SHAM are given in Figures 5.1 - 5.4. As can be seen from the harmonic spectra of the CSC and APF currents that 11^{th} and 13^{th} harmonic components are amplified by factors of 2.04 and 3.38, respectively. Therefore, the kVA rating of the CSC is reduced significantly for the pre-specified APF rating as discussed in previous chapters. The carrier harmonics for a switching frequency of 3.0 kHz are also successfully filtered out by the input filter as seen from Figure 5.4. Besides, the reactive power of the filter capacitors are compensated by the CSC, Figure 5.4, thus yielding almost unity power factor operation as aimed in the design work.

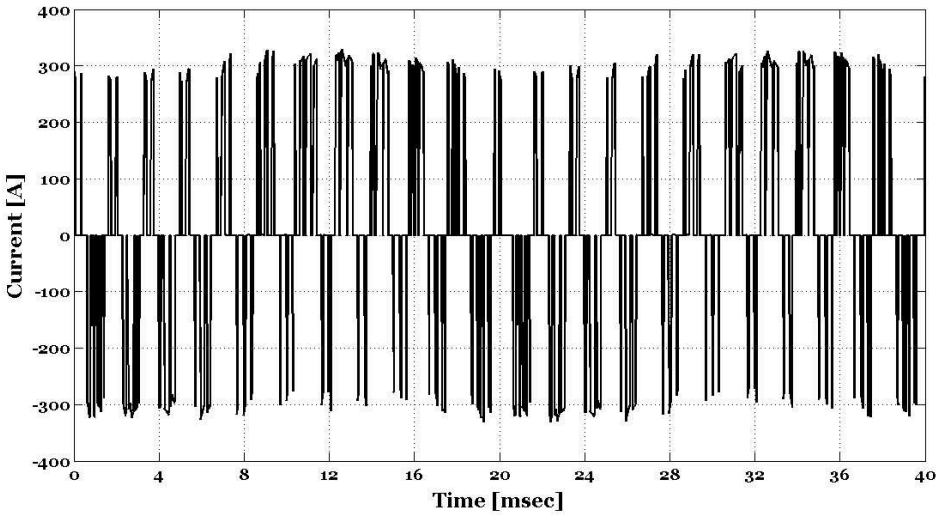


Figure 5.1: CSC current waveform *(Theoretical)*

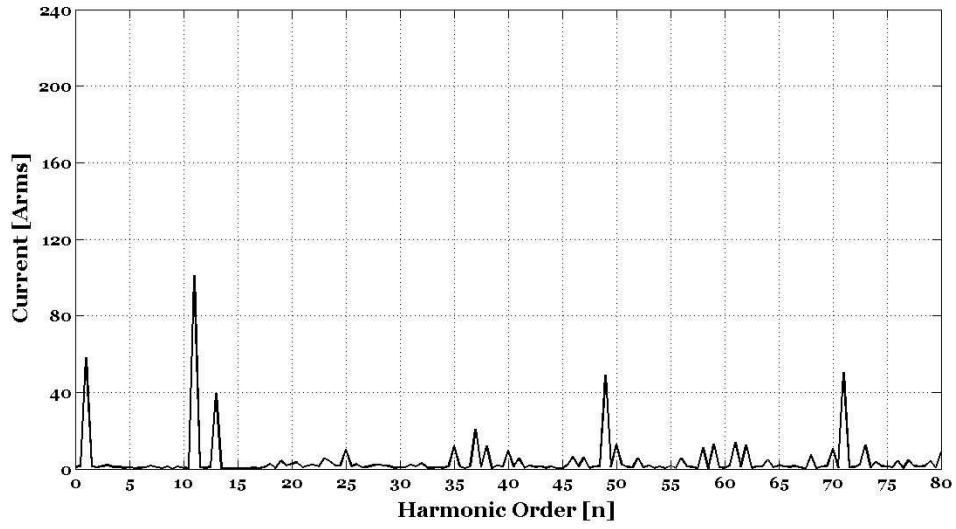


Figure 5.2: Harmonic spectrum of the CSC current *(Theoretical)*

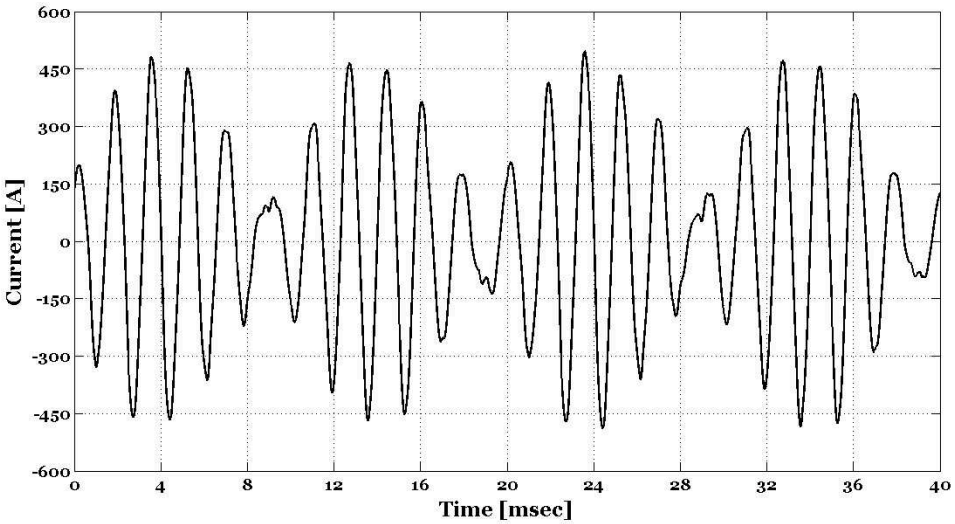


Figure 5.3: APF current waveform on LV side *(Theoretical)*

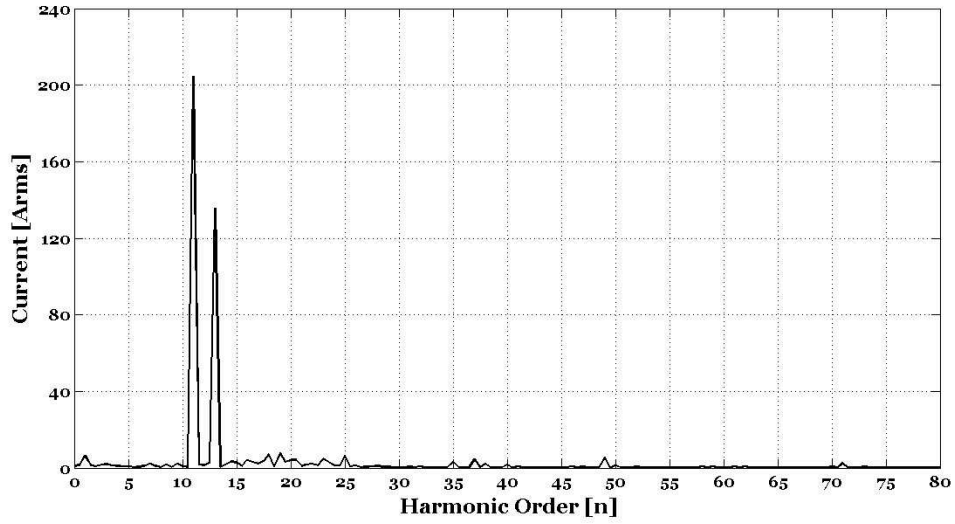


Figure 5.4: Harmonic spectrum of the APF current *(Theoretical)*

In addition to these, another important observation from these figures is that the harmonic components around the natural frequency of the input filter are damped out successfully, as expected, by the help of proposed active damping method for non-selected harmonics.

The increase in the kVA rating of the APF by SHAM can be expressed as (5.1) by using (3.10) for the load conditions given in Table 5.2. It is seen from (5.1) that, for the given load conditions, 1.0 p.u CSC is employed in a 2.275 p.u APF by the use of the proposed SHAM. This ratio can be increased to maximum 3.38 according to the load conditions, e.g. all the capacity is used for eliminating of 13^{th} harmonic.

$$\text{Increase in kVA rating} = \frac{\sqrt{6.0^2 + 4.0^2}}{\sqrt{\frac{6.0^2}{2.04^2} + \frac{4.0^2}{3.38^2}}} = 2.275 \tag{5.1}$$

Load and source current waveforms and, their harmonic spectra on the MV side are given in Figures 5.5 - 5.8. As can be understood from these figures that the 11^{th} and 13^{th} harmonic components of the load current are successfully filtered out by the APF. The 6.0 A rms 11^{th} current harmonic, which is 25 % of the I_L, is reduced to 0.4 A rms. Similarly, the 13^{th} current harmonic is also reduced from 16 % to 1.6 % with respect to I_L.

The waveforms of the APF current and its reference, which is calculated from the load current and, then referred to LV side, are given in Figure 5.9. The reference current is composed only of the 11^{th} and 13^{th} harmonic components of the load current, which are extracted by the selective harmonic extraction method, and does not include any other references such as active damping or error compensation. Since the fundamental current of the input filter capacitors are compensated by the CSC, the input current of the APF tracks its reference successfully as can be seen from Figure 5.9. In the design work, the magnitude of the dc-link current is chosen as 300 A for the pre-specified technical specifications. Figures 5.10 and 5.11 show that the reference current vector in *abc* frame, and hence, the final modulating waveform, u_a in DSPWM are not exceeding the 300 A for the given load conditions even the reference current vectors for reactive power compensation, active damping, and error compensation are added to the final reference.

The dc-link current and voltage waveforms for the rated operation of the APF are shown in Figures 5.12 and 5.13. The harmonic spectrum of the dc-link voltage is as given in Figure

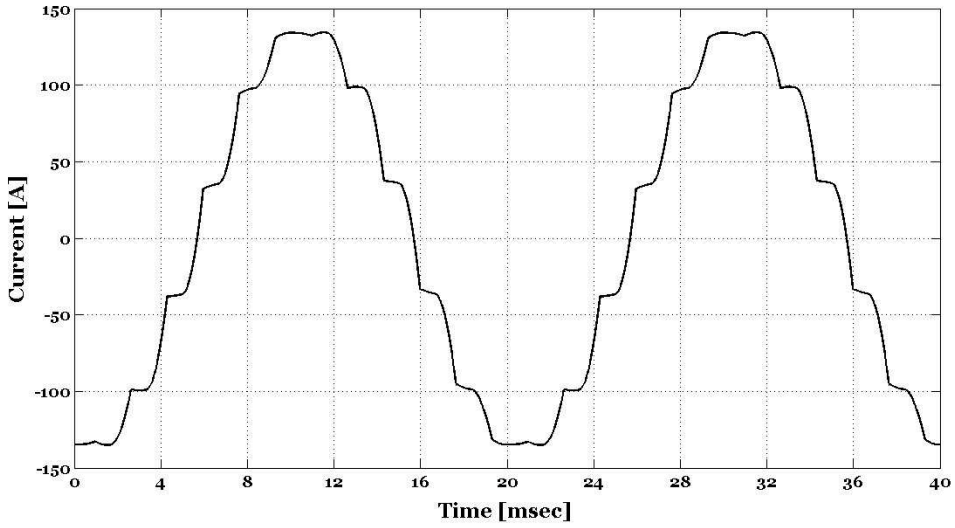


Figure 5.5: Load current waveform on MV side *(Theoretical)*

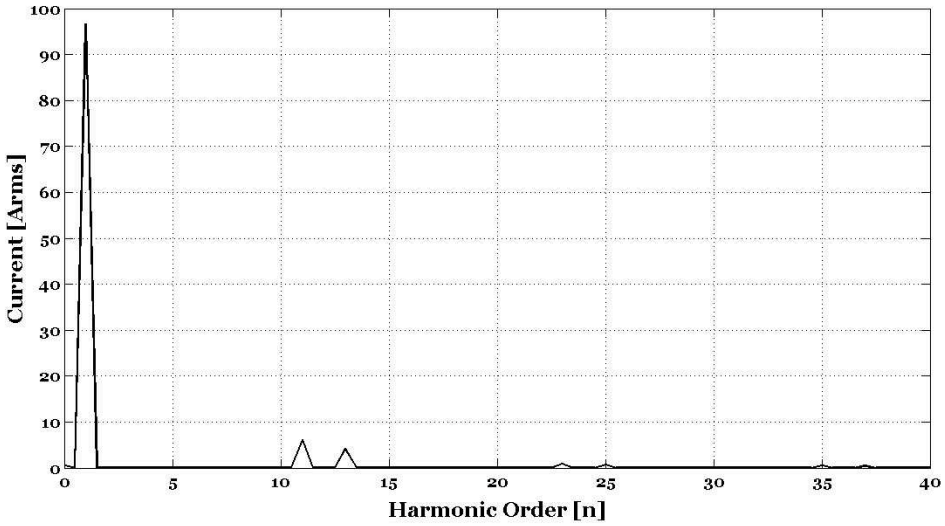


Figure 5.6: Harmonic spectrum of the load current *(Theoretical)*

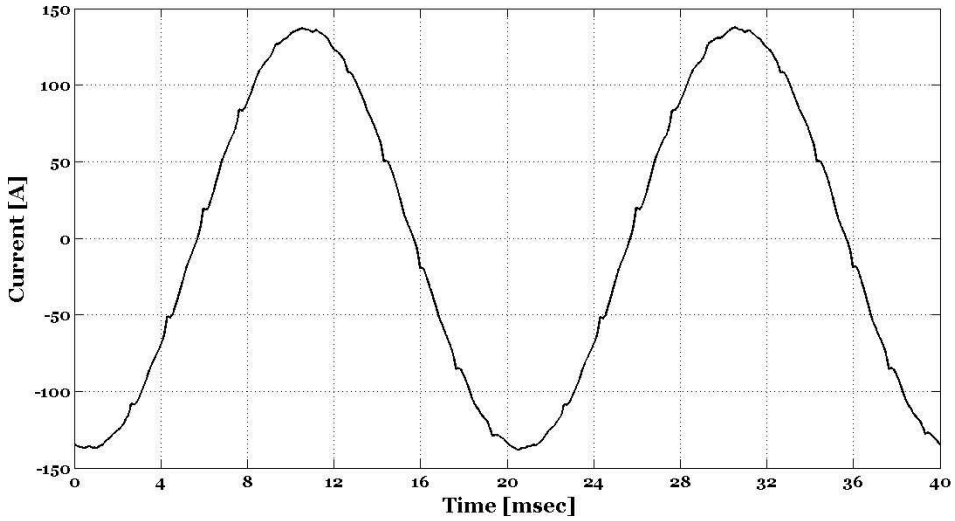


Figure 5.7: Source current waveform *(Theoretical)*

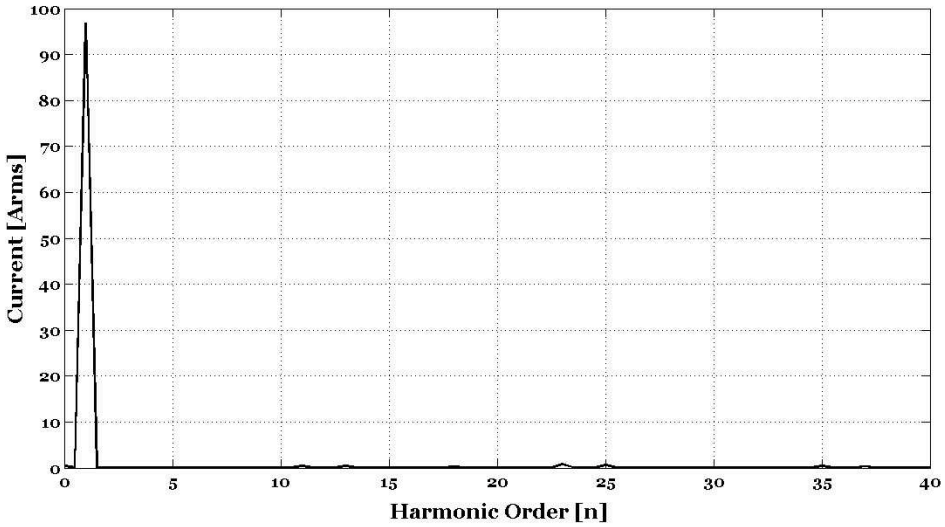


Figure 5.8: Harmonic spectrum of the source current *(Theoretical)*

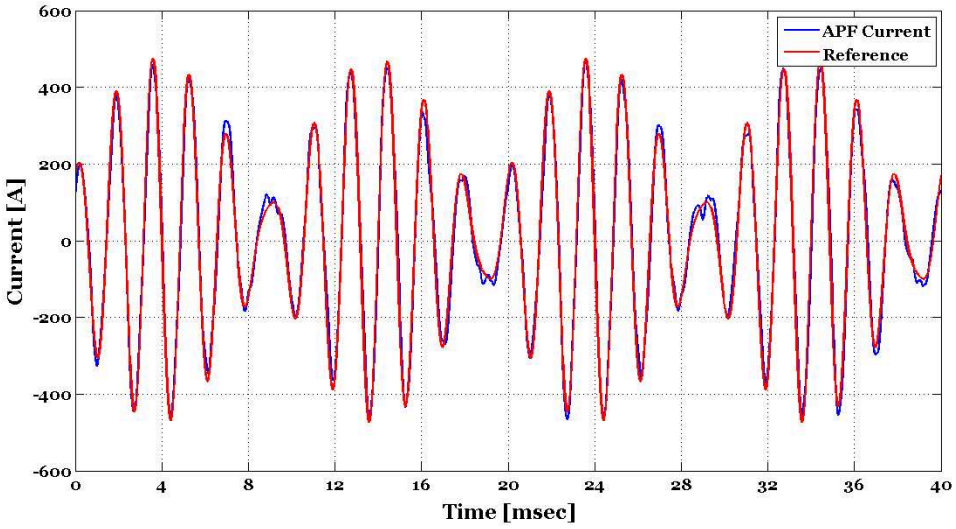


Figure 5.9: APF current waveform with reference signal on LV side *(Theoretical)*

5.14. The main harmonic component of the dc-link current and voltage is 12^{th} one, as expected. Higher frequency harmonics arise from the the DSPWM as described in Chapter 2.

Another issue, which should be considered in the implemented system, is the effective switching frequency of the semiconductor devices. The IGBT current waveform, in Figure 5.15, shows the switching pulses of the S1, is presented. According to the implemented DSPWM method, there should be 40 switchings in a time period of 20 msec for a carrier frequency of 3.0 kHz. However, since the modulating waveform, u_a also has reference current vectors for error compensation and active damping in addition to the 11^{th} and 13^{th} harmonic references, effective switching frequency of the semiconductor devices may exceed the theoretical switching frequency of 2.0 kHz. For the given load conditions, as can be seen from Figure 5.15, the effective switching frequency is about 2.5 kHz, indeed.

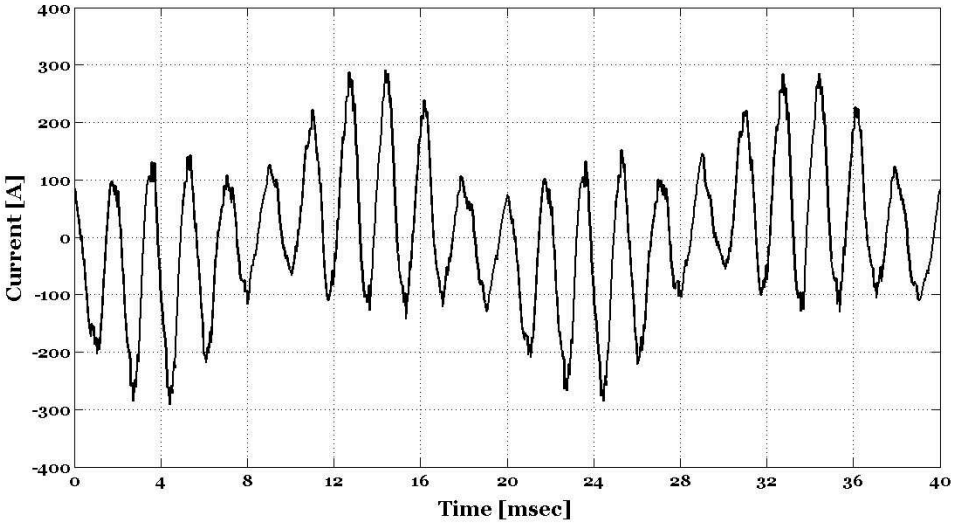


Figure 5.10: Final reference current waveform in *abc* frame *(Theoretical)*

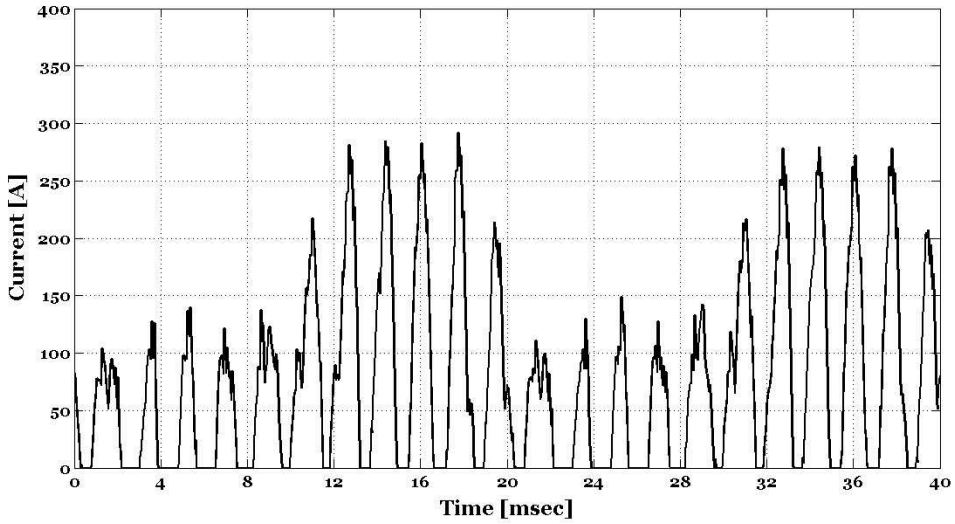


Figure 5.11: Final modulating waveform, u_a in DSPWM *(Theoretical)*

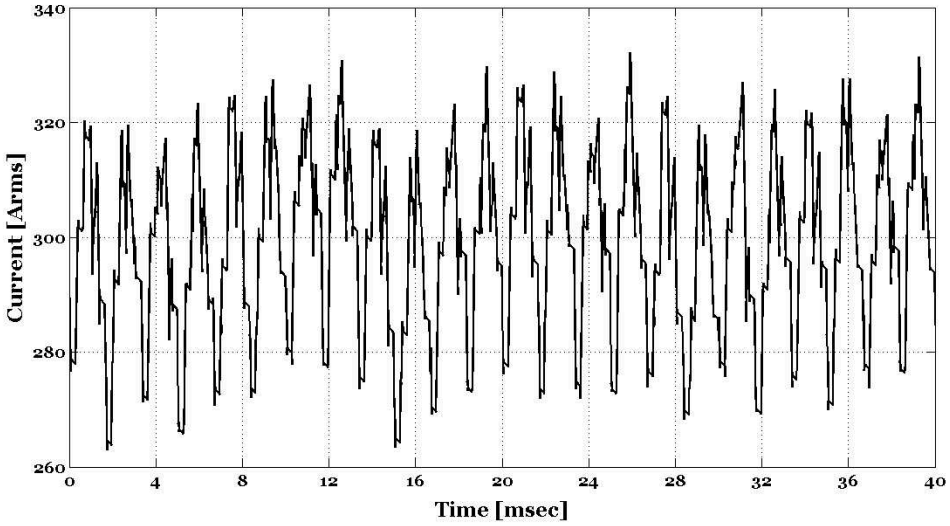


Figure 5.12: Dc-link current waveform for rated operation *(Theoretical)*

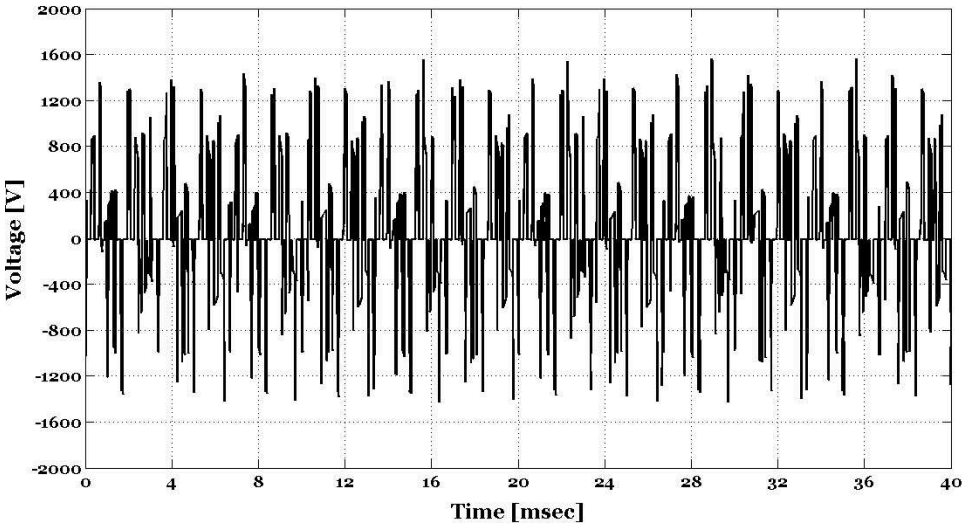


Figure 5.13: Dc-link voltage waveform for rated operation *(Theoretical)*

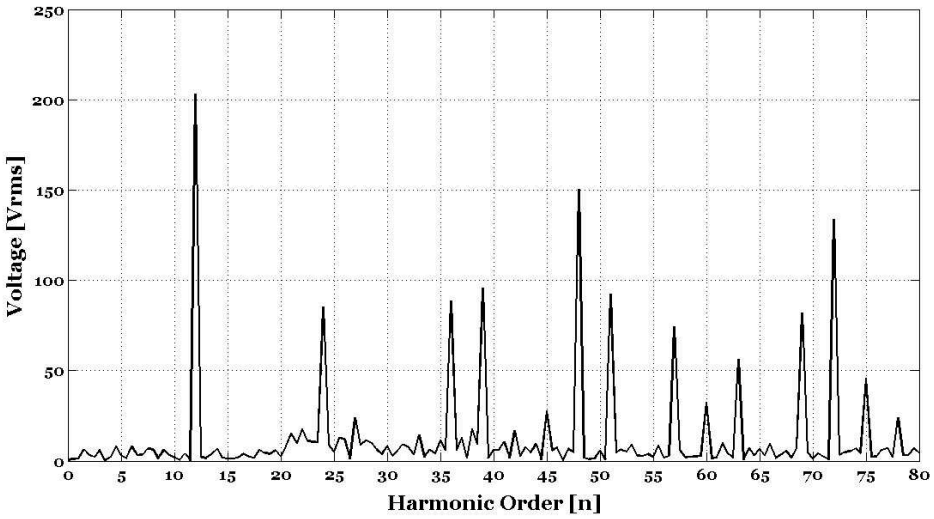


Figure 5.14: Harmonic spectrum of the dc-link voltage for rated operation *(Theoretical)*

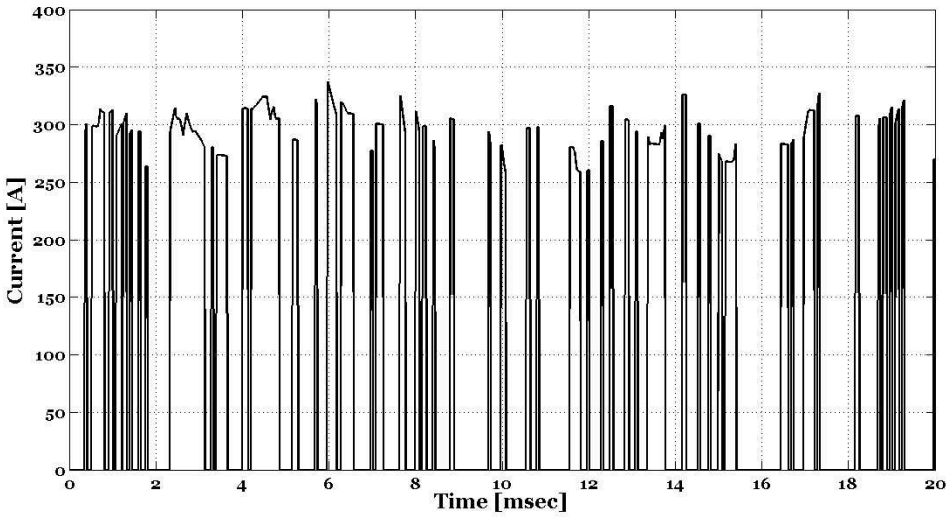


Figure 5.15: Current waveform of S1 *(Theoretical)*

5.2 Experimental Results

The proposed CSC based APF has been implemented to eliminate the 11^{th} and 13^{th} current harmonics of 12-pulse rectifiers supplying the catenary lines of the LRT system in Bursa, Bursaray. Some sample views from the implemented system are as given in Figures 5.16 - 5.19

Figure 5.16: IGBT and control panels after installation

Figure 5.17: Sample view from IGBT panel

Figure 5.18: Sample view from control panel

Figure 5.19: Sample view of dc-link reactor after installation

5.2.1 Verification of SHAM

The proposed SHAM, and the reduction in the kVA rating of the CSC have been verified by the field test results. In Figure 5.20, the line current waveform of the CSC is shown for the condition of rated operation. Reverse Recovery (RR) currents of the diode, which do not appear in theoretical waveforms as a result of ideal switch assumption, are marked on Figure 5.20. The peak value of the CSC line current may exceed 900 A when RR currents of the diodes are super-imposed on it. The harmonic spectrum of the CSC current is given in Figure 5.21. It is seen that CSC current is rich in harmonics, and consisting not only of the harmonic components to be injected by the APF to the supply, but also of the sideband harmonics of the carrier. A significant fundamental current component is apparent in the harmonic spectrum of the CSC current, which corresponds to mainly the reactive current to be injected by the CSC for compensation of reactive current of the input filter capacitors.

For the same operating conditions, the line current of the APF and its harmonic spectrum are shown respectively in Figures 5.22 and 5.23. The line current of APF is mainly composed of 11^{th} and 13^{th} harmonic components, and higher harmonics are much smaller as expected. A small fundamental component corresponds to the active losses of the converter and the dc-link reactor. Another fact is that the carrier, and its sideband harmonics are eliminated successfully by the input filter and the proposed active damping method for non-selected harmonics. In addition to these, harmonic current components around the natural frequency of the input filter are also damped out satisfactorily.

The pre-determined amplification of the 11^{th} and 13^{th} harmonic components of the load are apparent from Figure 5.21 and 5.23, thus reducing the installed kVA rating of the CSC for the pre-specified APF rating. The rms values of the 11^{th} and 13^{th} harmonic components of the associated APF and CSC currents are presented in Table 5.3. The theoretical and experimental amplification factors of the input filter are respectively 2.05 and 1.99 for the 11^{th} harmonic component. The amplification factor for the 13^{th} harmonic component is estimated as 3.35 in the design phase. However, in practice, it is realized to be 3.50, which is only 4.48 % higher than the pre-specified value. If the exact value of the transformer's quality factor were known, experimental amplification factors would be more close to the design values.

The kVA ratings of the APF and the CSC are calculated by using (3.5) and (3.6) for the

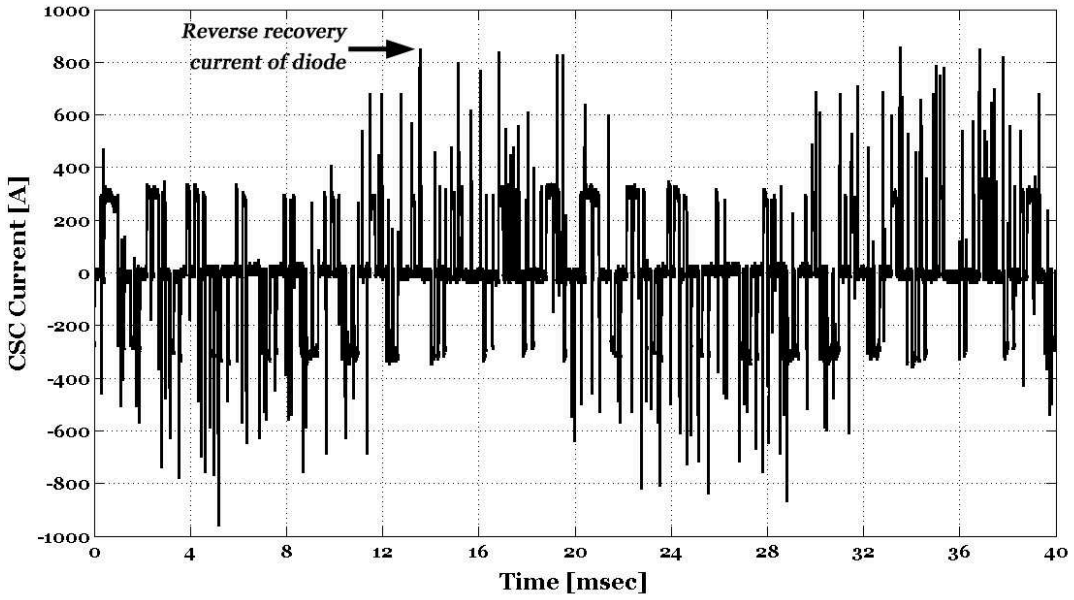


Figure 5.20: CSC current waveform for rated operation *(Field data)*

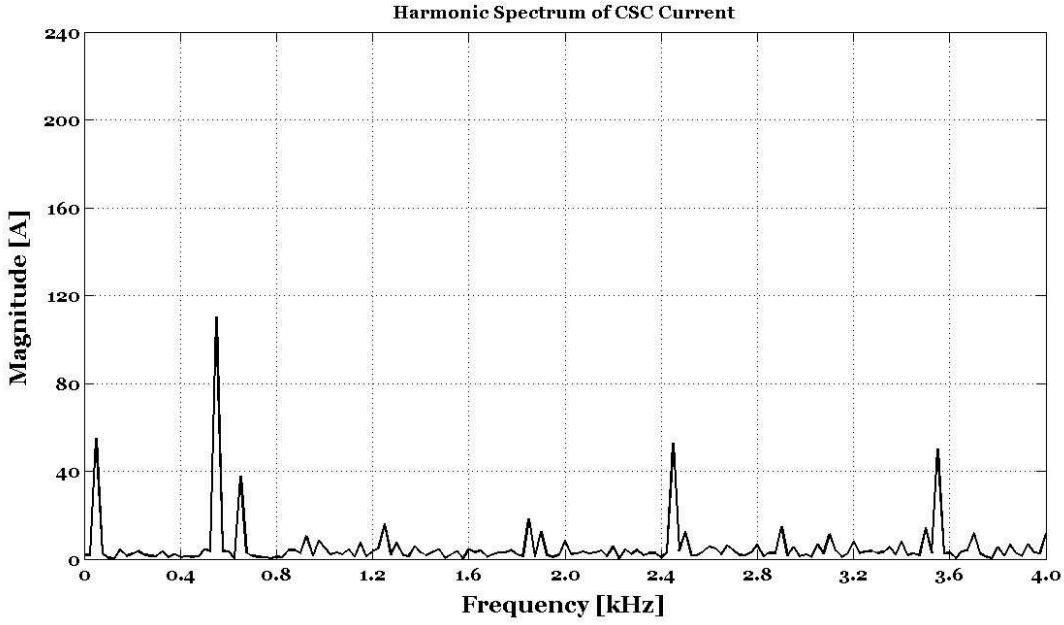


Figure 5.21: Harmonic spectrum of the CSC current for rated operation *(Field data)*

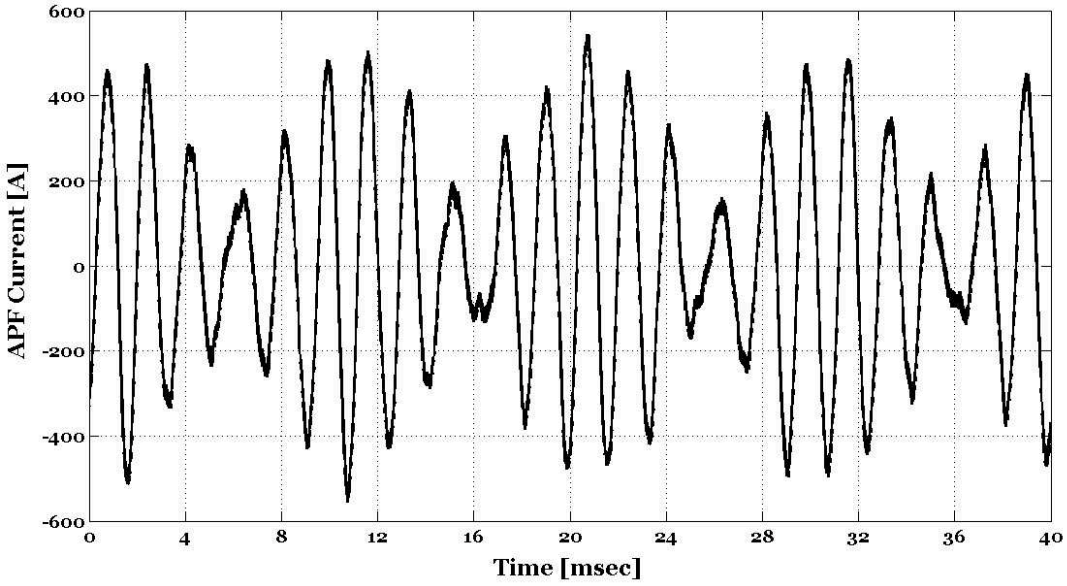


Figure 5.22: APF current waveform for rated operation *(Field data)*

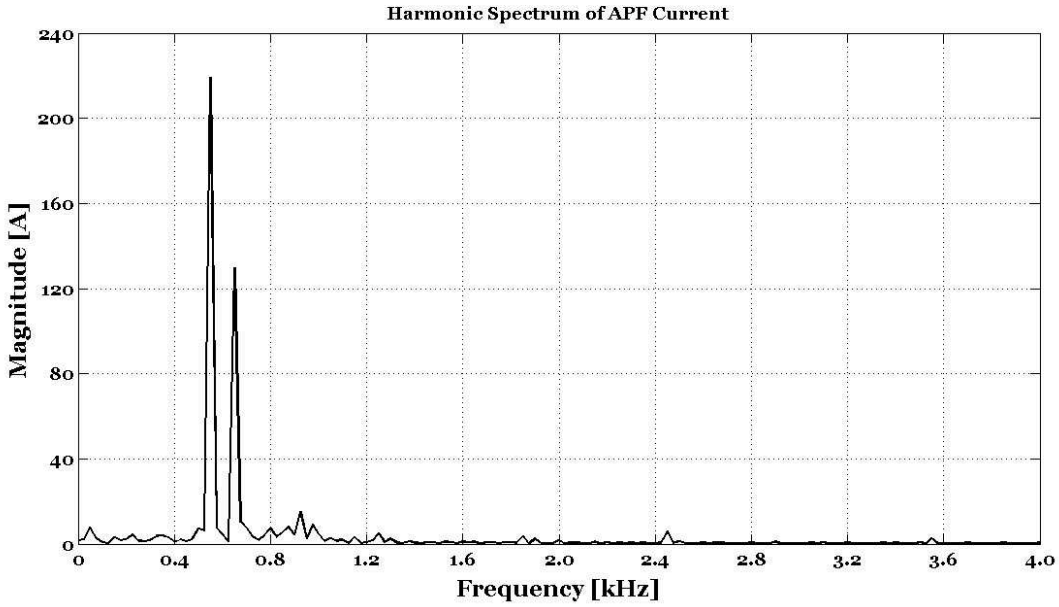


Figure 5.23: Harmonic spectrum of the APF current for rated operation *(Field data)*

harmonic currents given in Table 5.3 as given (5.2) and (5.3).

$$kVA_{APF} = \sqrt{3} \cdot 1032 \cdot \sqrt{216.5^2 + 126^2} = 448 \text{ kVA} \tag{5.2}$$

$$kVA_{CSC} = \sqrt{3} \cdot 1032 \cdot \sqrt{109^2 + 36^2} = 205 \text{ kVA} \tag{5.3}$$

The calculation of kVA_{CSC} in (5.3) does not take into account the reactive current of 57 A rms, which fully compensates the reactive current produced by the input filter capacitors. If it is included in the kVA calculation, kVA_{CSC} increases to 229 kVA as given in (5.4). It is worth to note that in applications for inductive loads, capacitive VAr generation of the input filter capacitor can be used for reactive power compensation of the load. For this case, kVA produced by the CSC varies in the range form 205 to 229 kVA. In summary, the proposed SHAM reduces kVA_{CSC} from 448 to 229 kVA in the worst case.

$$kVA_{CSC} = \sqrt{3} \cdot 1032 \cdot \sqrt{57^2 + 109^2 + 36^2} = 229 \text{ kVA} \tag{5.4}$$

Table 5.3: Rms values of the 11^{th} and 13^{th} harmonic components of APF and CSC currents

Harmonic Component	CSC Current *Arms*	APF Current *Arms*	Amplification Factor
11^{th}	109.0	216.5	1.99
13^{th}	36.0	126.0	3.5

In order to compare the kVA ratings of the CSC and APF, not only for selected harmonics, but also for all harmonic components, non-selected harmonic current components have been also taken into account in the calculation of rms values of the CSC and APF currents. In Table 5.3, the rms current values and the corresponding kVA ratings are given for two different rms current calculation approaches. As expected, if all of the non-selected harmonic components are included into the rms current calculation, the kVA rating of the CSC increased due to the carrier and its sideband harmonics.

Table 5.4: kVA ratings for two different rms current calculation approaches *(Field Data)*

	Only Selected Components ($I_{rms} = \sqrt{I_1^2 + I_{11}^2 + I_{13}^2}$)	True-rms ($I_{rms} = \sqrt{I_1^2 + I_2^2 + \cdots + I_n^2}$)
APF Current (rms)	251	254
CSC Current (rms)	128	178
APF rating (kVA)	448	454
CSC rating (kVA)	229	318
kVA_{APF}/kVA_{CSC}	1.96	1.43

The line-to-line voltage on the LV side for rated operation is as given in Figure 5.24, and its harmonic spectrum in Figure 5.25. The line-to-line voltage waveform is highly distorted, and has mainly the 11^{th} and 13^{th} harmonic components as expected. Since the CSC based APF has been connected to the same LV bus with the Thyristor Switched Shunt Reactor (TSSR) based compensation system, the control system of the TSSR has been adopted to operate with this highly distorted voltage waveform.

In order to show the effectiveness of the proposed CSC based APF, sample measurements have been done on MV side by recording the supply and load current waveforms. A sample waveform set is as shown in Figure 5.26. It is seen that the CSC based APF filters out successfully the 11^{th} and 13^{th} harmonic components of the load current, and the resulting supply current waveform complies with the IEEE Std.519-1992.

5.2.2 DC Side Voltage and Current Waveforms

The dc-link current and voltage waveforms for rated operation are given in Figures 5.27 and 5.28, respectively. The major main harmonic component in the dc-link current (and voltage) is the 12^{th} harmonic component as found by simulations. However, experimental dc-link current waveform differs from the theoretical one regarding the higher order harmonic components.

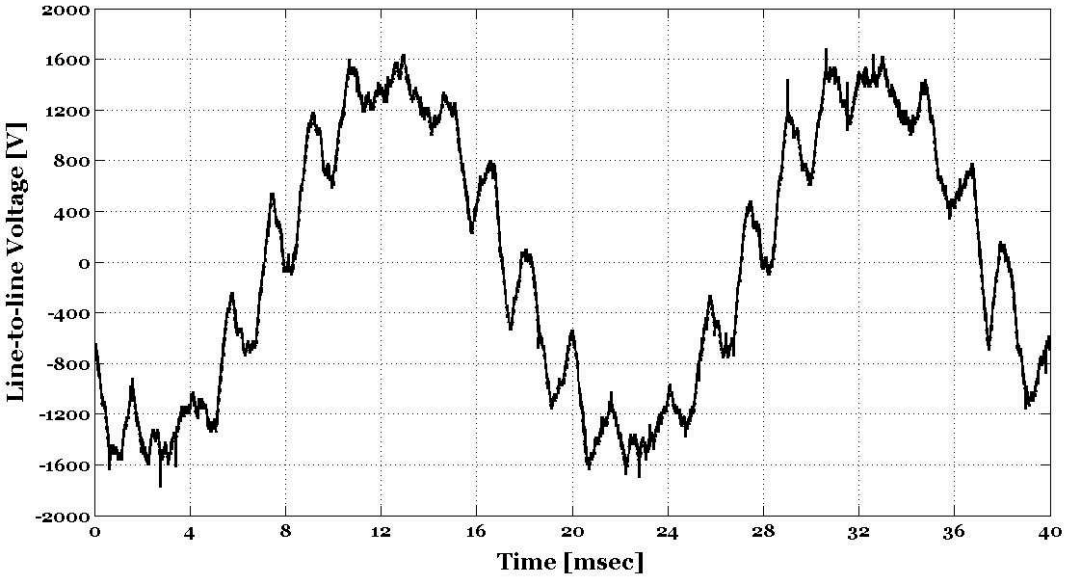


Figure 5.24: Line-to-line voltage waveform on LV side *(Field data)*

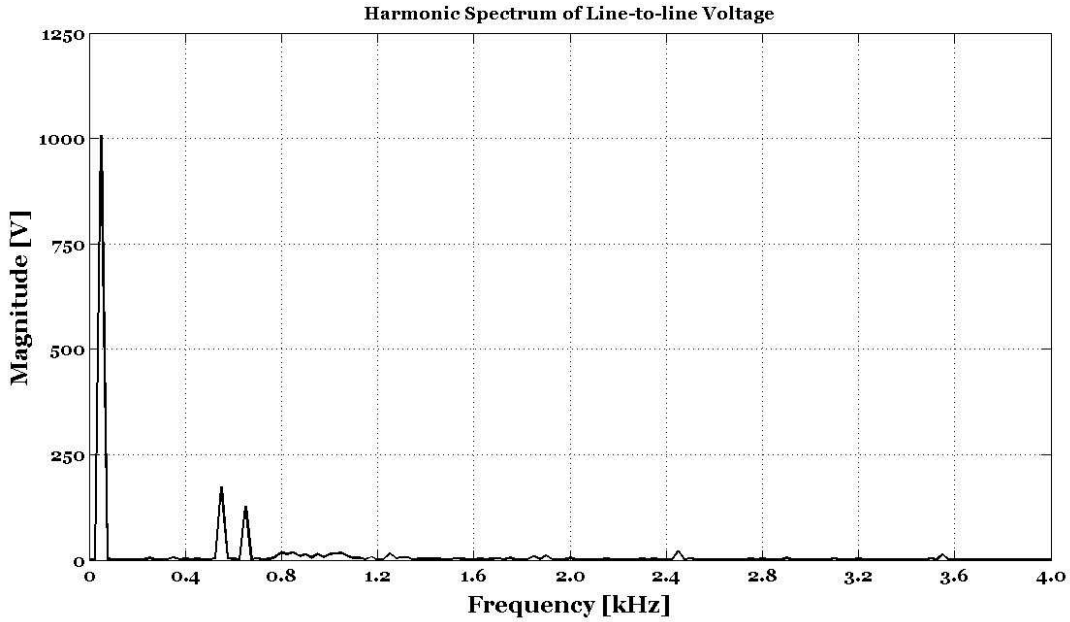


Figure 5.25: Harmonic spectrum of the line-to-line voltage on LV side *(Field data)*

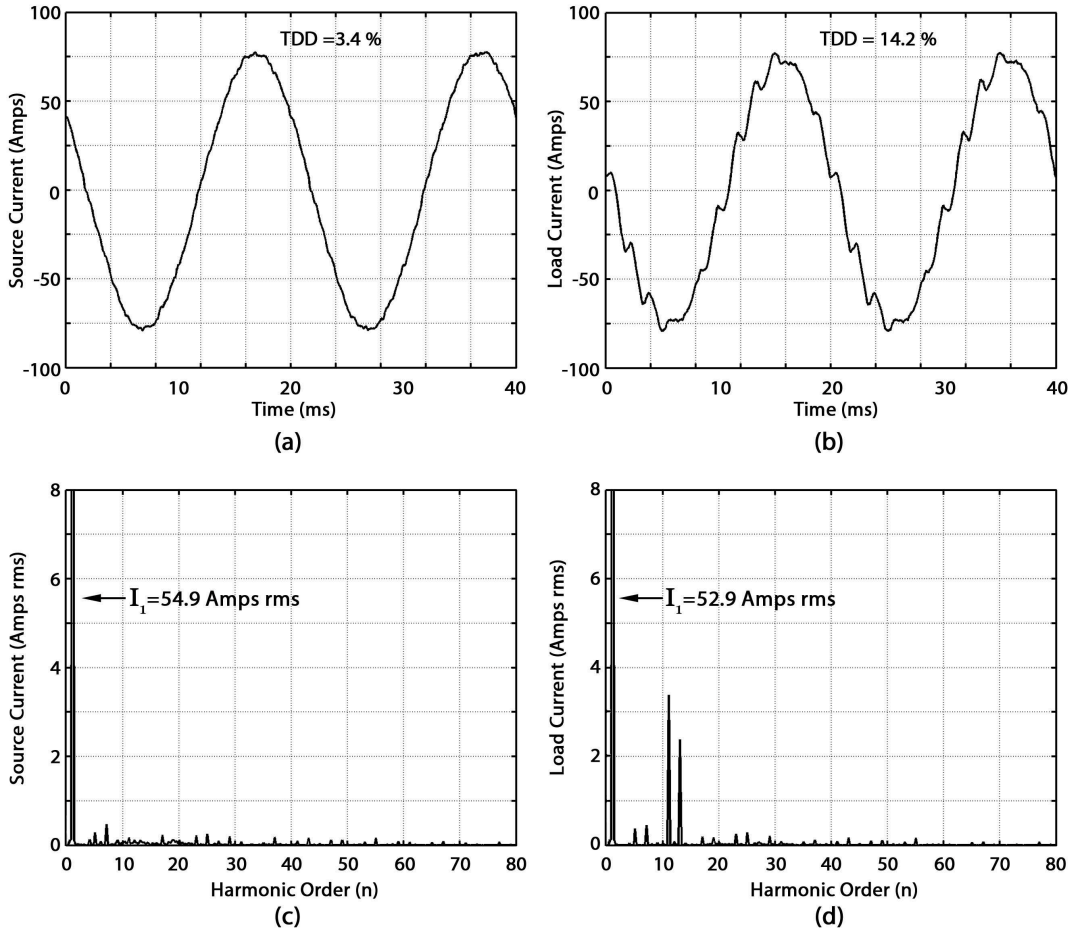


Figure 5.26: Waveforms of the (a) Source current, and (b) Load current with the harmonic spectra of (c) Source current, (d) Load current based on MV measurements *(Field data)*

This can be seen also from the harmonic spectrum of the dc-link voltage given in Figure 5.29. Residual harmonics around the natural frequency of the input filter distorts not only the output current of the APF, but also the dc-link current.

5.2.3 Voltage and Current Waveforms of Power Switches

In Figure 5.30, the voltage and current waveforms of the top switch in one phase are presented. As the characteristics of the CSC topology, each switch should have unidirectional current carrying, ad bipolar voltage blocking capability. As it is seen from Figure 5.30 that, negative voltage pulses are blocked by the diode, whereas positive voltage pulses are blocked by the IGBT, thus having bipolar voltage blocking capability.

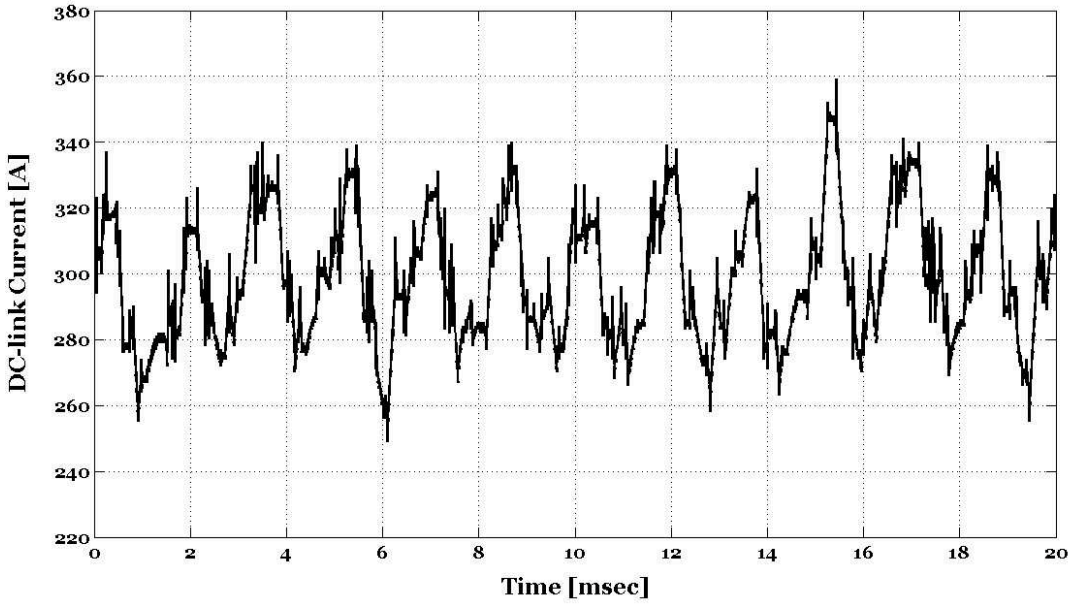


Figure 5.27: Dc-link current waveform for rated operation *(Field data)*

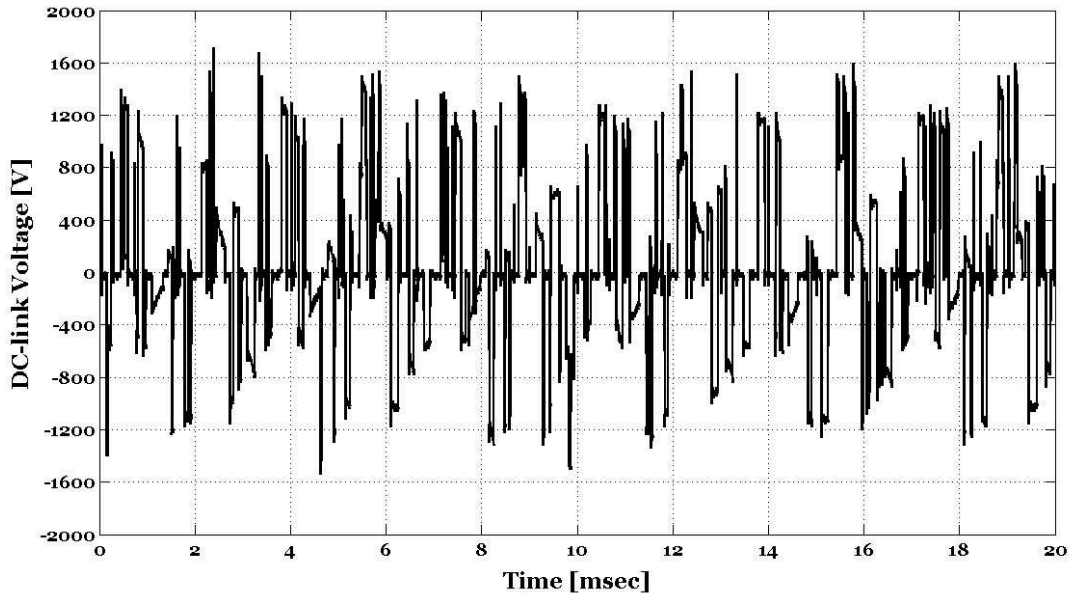


Figure 5.28: Dc-link voltage waveform for rated operation *(Field data)*

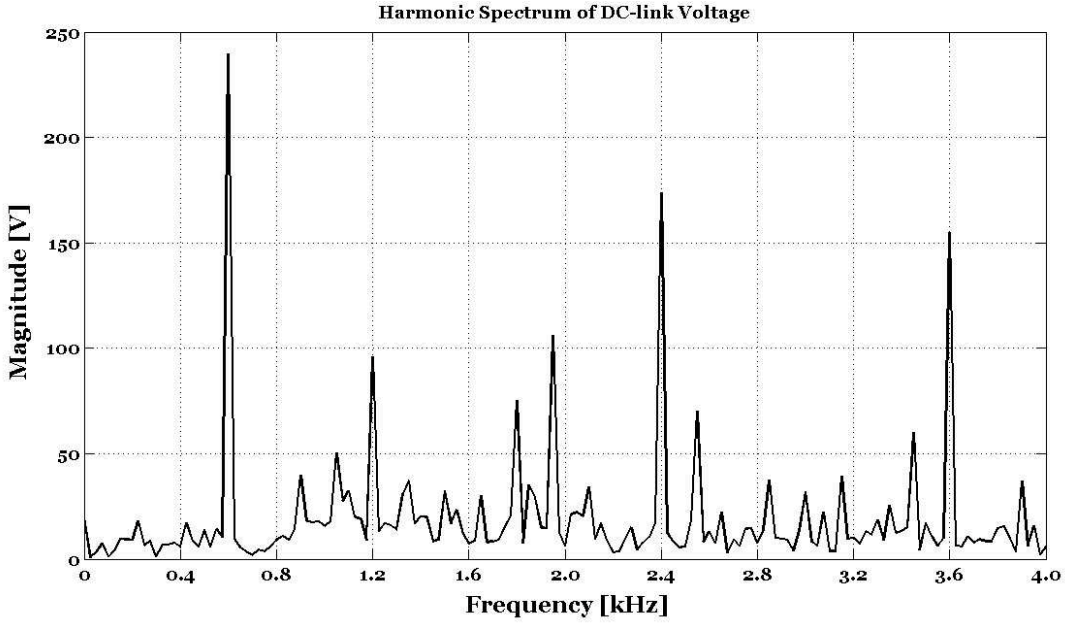
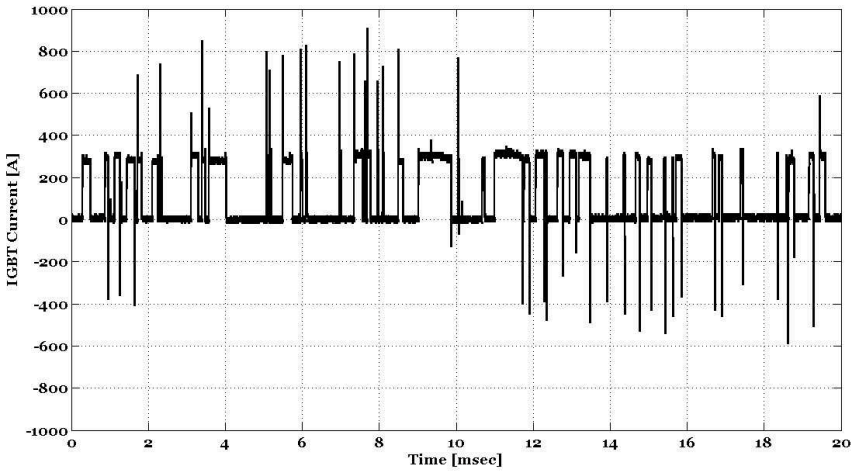


Figure 5.29: Harmonic spectrum of the dc-link voltage waveform for rated operation *(Field data)*

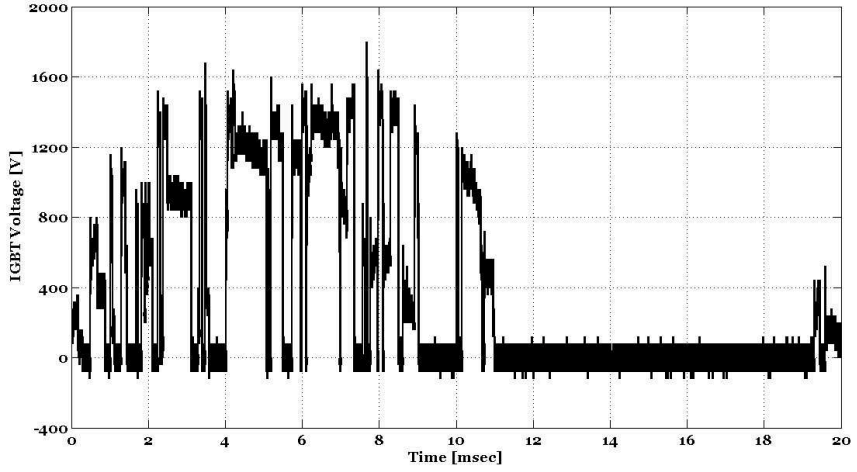
The effective switching frequency of the IGBT is also derived from Figure 5.30. It is seen that there are 47 switching pulses in a period of 20 msec, which corresponds to an effective switching frequency of 2.35 kHz for 3.0 kHz carrier frequency.

The voltage and current waveforms of the phase A switch, S1 in upper half of the bridge circuit are given in Figure 5.30. Unidirectional current carrying, and bi-polar voltage blocking capabilities of each power switch are apparent form Figure 5.30. As can be seen from Figure 5.30.(c), negative voltage pulses are blocked by the first-recovery diode while positive voltage pulses are blocked by the IGBT, thus having bi-polar voltage blocking capability. Reverse recovery current of reverse blocking diode of each power switch is carried by the mated IGBT module, which are marked on Figure 5.30.

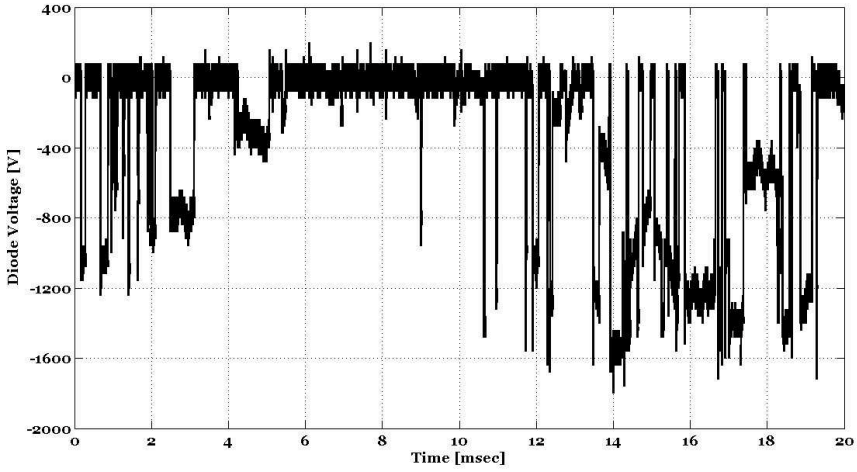
The effective switching frequency of the power switches is also calculated form Figure 5.30. There are 47 switching pulses in one complete cycle of the supply voltage waveform (20 msec) for the associated operating conditions. This corresponds to an effective switching frequency of 2.3 kHz when the f_{cr} is 3.0 kHz. On the other hand, the number of switching pulses is not constant but varies with the operating condition as will be discussed in the next subsection.



(a)



(b)



(c)

Figure 5.30: Device voltage and current waveforms (a) IGBT (S3) current (b) IGBT voltage (c) Diode voltage for I_{F11} = 115 Arms, I_{F13} = 63 Arms *(Field data)*

5.2.4 Characterization of Power Losses

In order to find the total power dissipation of the CSC, and to figure out the variation of these losses with the operation condition, field tests have been carried out for different load conditions. Total loss of the converter has been calculated by the use of the two-watt meter method, in which the two line-to-line voltages, and the two line currents have been measured on the LV side. For the dc-link losses, dc-link voltage and current waveforms have been used. Variation of the dc-link and total losses of the CSC are as given in Table 5.5.

Table 5.5: Variation of the dc-link and total losses of the CSC for different load conditions

Test	Harmonic Components of the APF Current	APF Current A true-rms	APF Rating kVA	Dc-link Loss kW	Total Loss kW
1	I_{F11}=115 Arms I_{F13}=63 Arms	131	227	2.35	12.24
2	I_{F11}=143 Arms I_{F13}=87 Arms	167	289	2.34	11.63
3	I_{F11}=179 Arms I_{F13}=108 Arms	209	362	2.55	11.43
4	I_{F11}=206 Arms I_{F13}=124 Arms	240	416	2.28	11.37
5	I_{F11}=216 Arms I_{F13}=142 Arms	259	448	2.44	11.08

First of all, the most interesting observation made on these results is the variation of the total CSC loss against the current injected by the APF on the LV side. Although the rms value of the APF current increases, total power dissipation decreases. This is because as the modulation index increases, the number of switchings, hence the effective switching frequency, decreases. Figure 5.31 shows the corresponding IGBT current waveform for Test 1 in Table 5.5, and Figure 5.32 that of Test 5. For the lower kVA generation (Test 1), total number of switching is 47, however, for the rated operation (Test 5) it is 41. Thus, the effective switching frequency is reduced from 2.35 kHz to 2.05 kHz as the kVA is increased to its rated value.

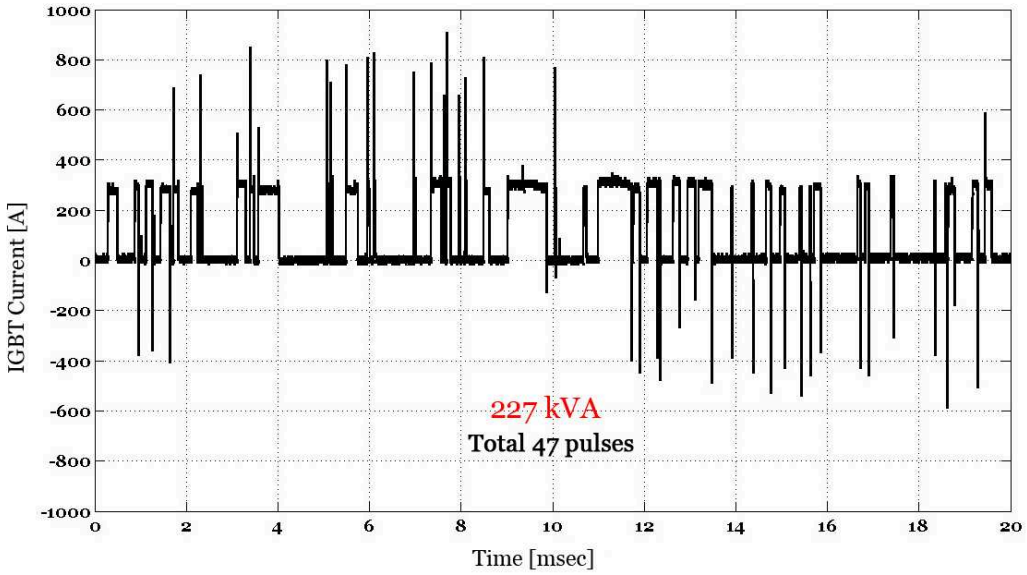


Figure 5.31: IGBT current waveform for I_{F11} = 115 Arms, I_{F13} = 63 Arms *(Field data)*

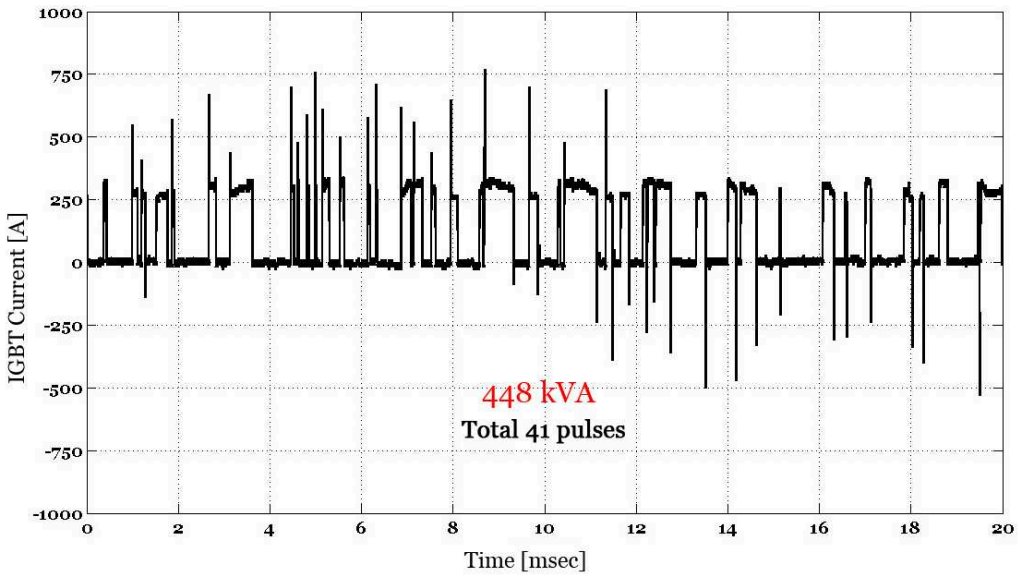


Figure 5.32: IGBT current waveform for I_{F11} = 216 Arms, I_{F13} = 142 Arms *(Field data)*

The switching losses are characterized as the 67.5 % of the total CSC loss from Table 4.5. Although, the conduction loss of the CSC is proportional to the kVA produced, the total power dissipation of the CSC reduces as the kVA production is increased, since the dominant power loss component is the switching losses of power switches.

It is also seen from Table 5.5 that the dc-link losses are around 2.3-2.5 kW, and changing slightly with respect to output current of the APF. It should be noted that 1.0 V offset in the voltage measurement apparatus results in 300 W error in the dc-link loss calculation. For that reason, there may be a considerable error in dc-link loss calculation, and hence, a proportional relationship between the dc-link losses and the kVA production can not be justified.

5.2.5 LV and MV Measurements via Data Acquisition System

The filtering performance of the CSC based APF has been tested by the use of measurements based on a Data Acquisition (DAQ)system. Its technical specifications are given in Table 5.1. Firstly, a one day measurement has been carried out at PCC, i.e., MV current and voltage signals have been taken via conventional voltage transformers, and Rogowski current transducers. Since the supply currents have been measured directly on the MV cable, no gain and/or phase error has been introduced to the current measurements. Figures 5.33 and 5.34 show the daily variations of the 11^{th} and 13^{th} harmonic current components of the supply current during the operation of the APF, respectively. These records should be compared with supply current waveform in Figure 4.2, which is recorded when the APF is out of service. It is seen that APF eliminates the 11^{th} and 13^{th} harmonics successfully, thus making them to comply with IEEE Std.519-1992.

In addition to the MV measurements, measurements on the LV side have been also performed for monitoring the performance of the APF. During the measurements, the LRT system has been operated as it was planned, and APF has been commanded to inject inductive reactive power to the network as well as filtering the 11^{th} and 13^{th} harmonic components. In Figure 5.35, the active power variation of the APF is shown for this measurement period. It is seen that the active power demand of the APF varies from 6.0 to 10.0 kW according to the load variation. Furthermore, the reactive power production of the APF, which was set to 80 kVAr inductive, is as given in Figure 5.36.

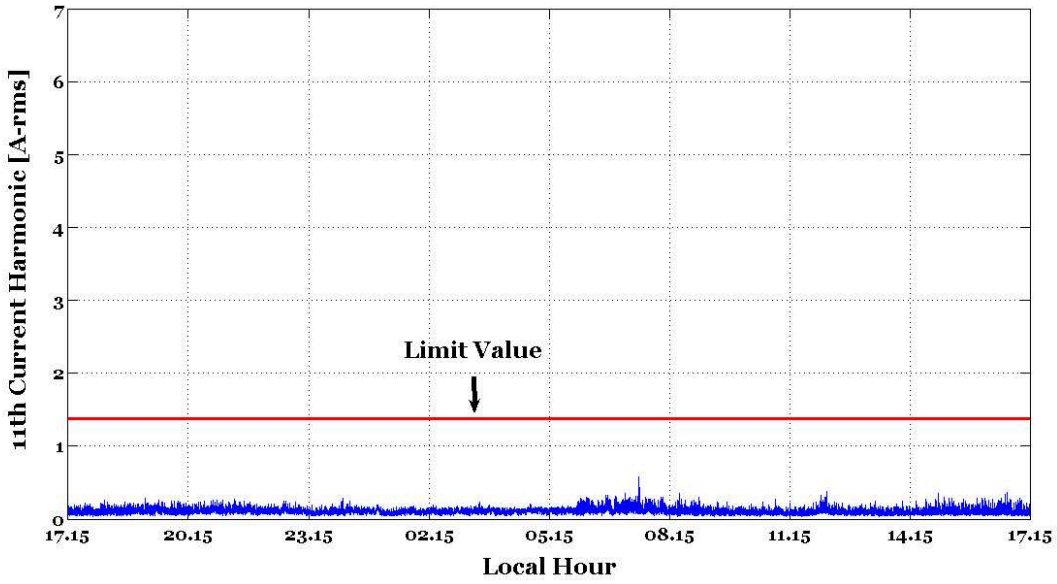


Figure 5.33: Daily variation of the 11th harmonic component of the supply current *(One second averaged field data)*

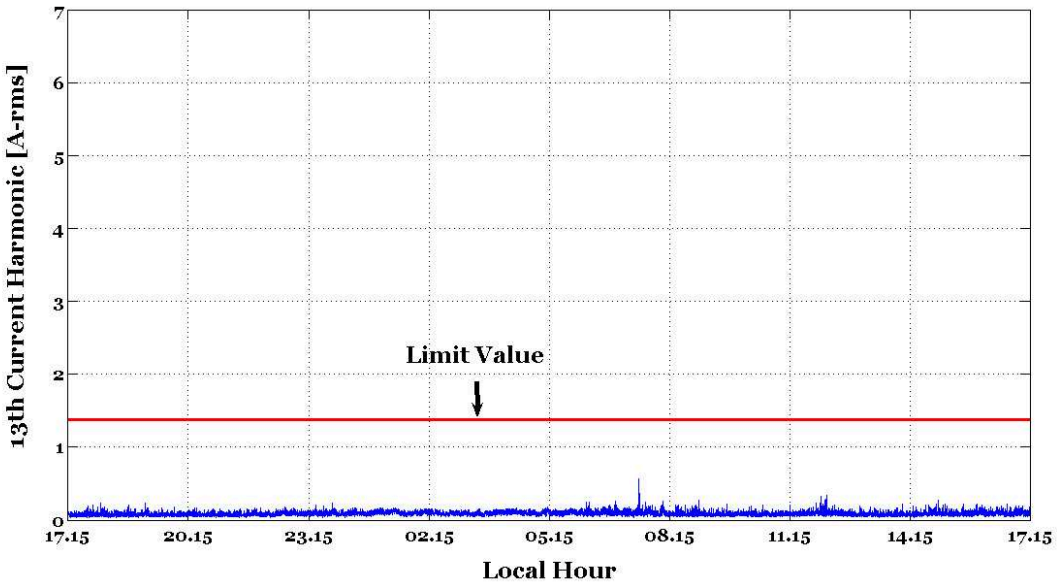


Figure 5.34: Daily variation of the 13th harmonic component of the supply current *(One second averaged field data)*

The rms values of the 11^{th} and 13^{th} harmonic current components are shown in Figures 5.37 and 5.38, respectively. Also, the variation of the true rms value of the APF current is given in Figure 5.39. It can be concluded from these figures that; in order to comply with the very tight limits on reactive energy, some portion of the installed capacity of the APF may be allocated for the compensation of the capacitive reactive power of the long MV cables, thus allowing to operate the APF in D-STATCOM mode.

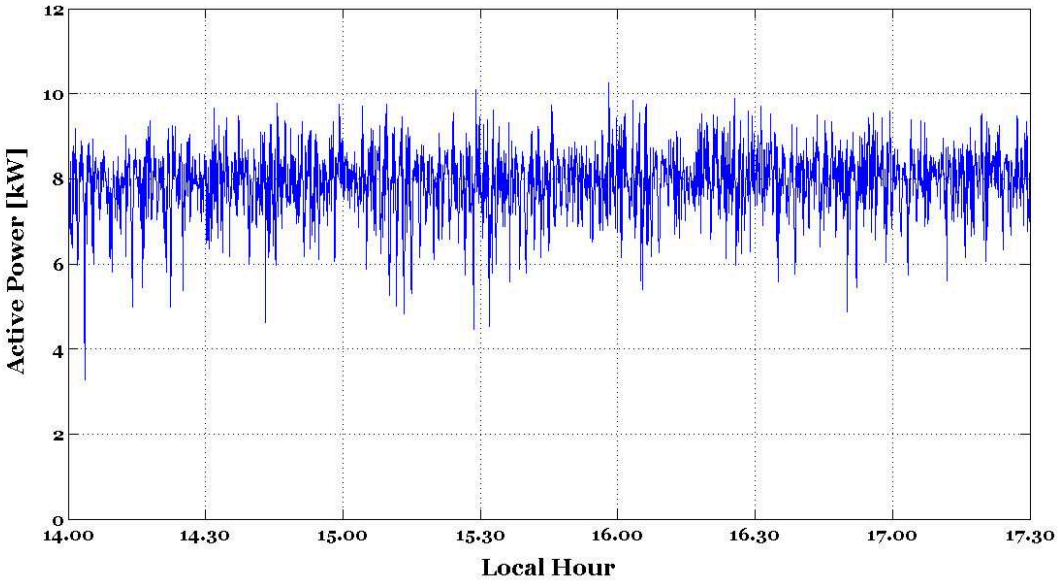


Figure 5.35: Active power variation of the APF *(One second averaged field data)*

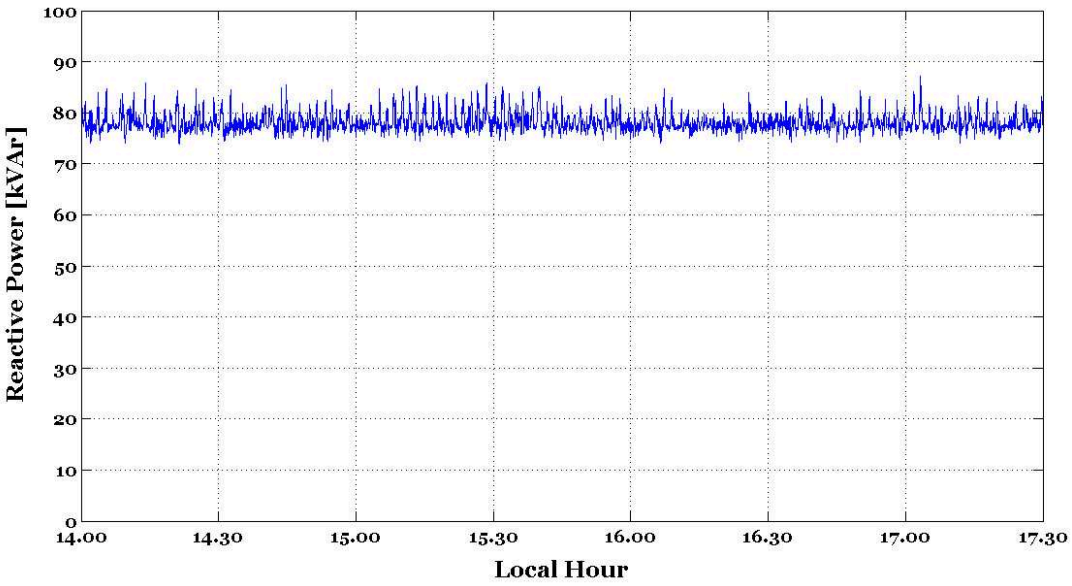


Figure 5.36: Reactive power variation of the APF (One second averaged field data)

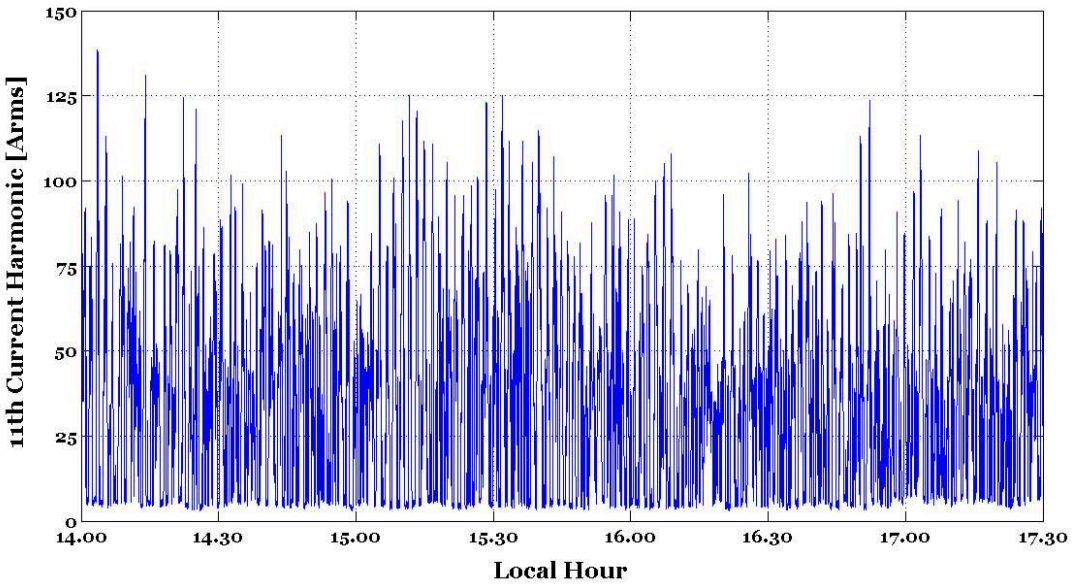


Figure 5.37: Variation of the 11^{th} harmonic component of the APF current (One second averaged field data)

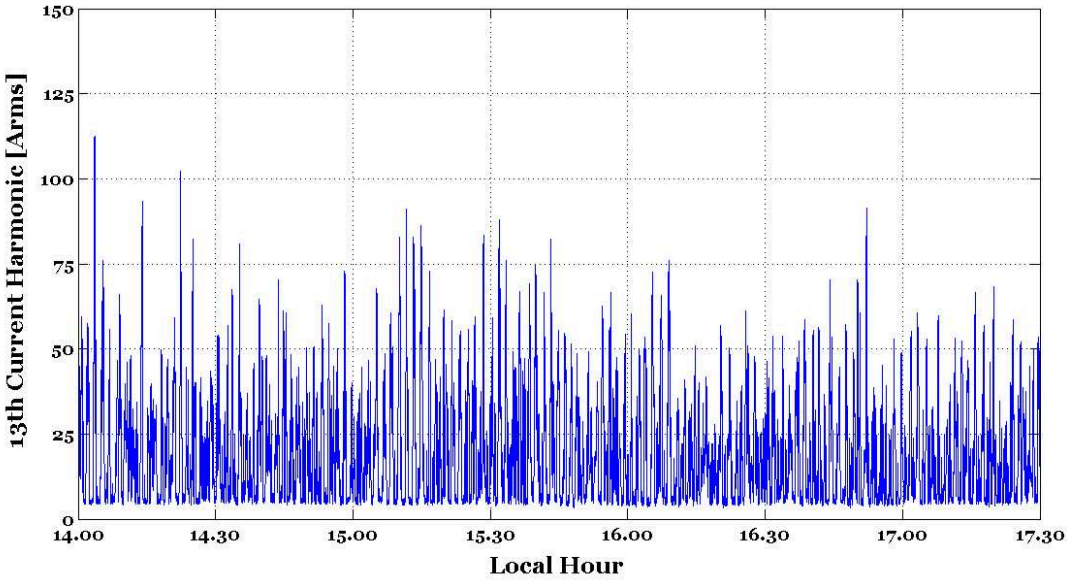


Figure 5.38: Variation of the 13th harmonic component of the APF current (One second averaged field data)

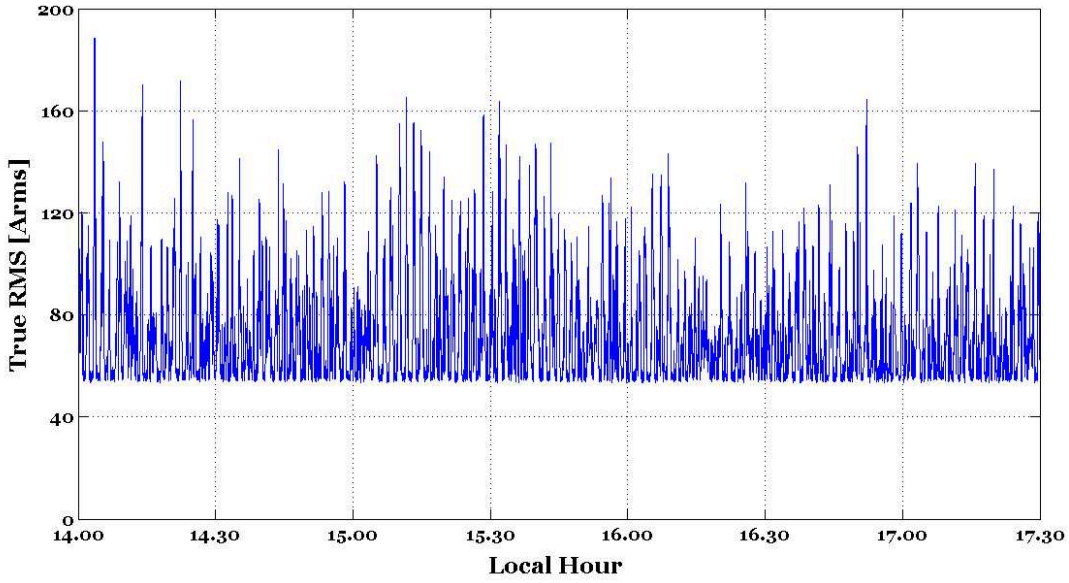


Figure 5.39: True rms variation of the APF current (One second averaged field data)

CHAPTER 6

CONCLUSIONS

Nowadays, Electric Power Quality (PQ) is being an important research, development and application issue in the transmission, distribution, and utilization of electrical energy. Improvements in PQ cause a considerable reduction in electrical power and production losses, and a significant improvement in the quality of final industrial products. On this occasion, utilities and the operators have published grid codes, regulations, and recommendations in order to ensure quality of the electrical power in transmission and distribution systems. As an example in the country, voltage and current harmonics at High Voltage (HV) and Medium Voltage (MV) systems should comply with the values, which are nearly the same as those of IEEE Std. 519-1992 and EN 50160. Although, reactive power or energy is not a direct PQ parameter, it indirectly affects the quality of electrical power, and causes extra transmission and distribution losses. Therefore, the flow of reactive power in O/H lines and feeders should be kept under control. As an example, very tight regulations have been imposed on customers and distribution companies in the country. If these limits are exceeded, the operator penalizes its customer for the total amount of reactive energy consumed (the unit price of reactive energy is nearly half of the unit price of active energy). However, this is not the case for harmonics and other PQ parameters. The penalty for these PQ parameters is to interrupt the electricity service to the customer, which is usually being inapplicable owing to economical and political reasons. Therefore, the industrial and commercial customers pay their attention primarily to the power factor correction by installing usually shunt plain capacitors to their facilities. On the other hand, the customers installing tuned shunt Harmonic Filters (HF) are usually faced with either an overcompensation problem or harmonic overloading problems, owing to the flow of harmonic currents generated by neighboring industrial plants to their HF installations. However, the use of APFs eliminates entirely the mentioned problems of passive filters, and

provides a complete solution to the harmonic problems arising from non-linear loads.

In this research work, a CSC based shunt APF has been investigated for connection to MV buses. In order to minimize the kVA rating of CSC, for the pre-specified kVA rating of APF unit in a given application, a new technique has been proposed, which is called the Selective Harmonic Amplification Method (SHAM) in the thesis. Furthermore, in order to reduce the dissipation in APF systems with passive damping, a modified active damping method for non-selected harmonics has been proposed. The design approach and theoretical findings have been verified by laboratory and field tests. For this purpose, a prototype CSC based APF has been designed and implemented to filter out the 11^{th} and 13^{th} current harmonic components produced by the 12-pulse uncontrolled rectifiers supplying the catenary lines of a LRT system in Bursa.

In the thesis, a new approach has been proposed to the design of the CSC based APF, and to make the CSC based APF a loss and cost competitive alternative to the VSC based APF. This new approach is based on the use of the amplification property of the input filter at some selected frequencies by employing the selective harmonic extraction technique via synchronous reference frames, and is called as SHAM. It reduces the kVA rating of the converter, thus eliminating the main disadvantage of the CSC. In order to make the SHAM applicable, design of the power stage and the control system have been considered together. Since the idea behind the SHAM is using the amplification property of the input filter at some pre-selected frequencies, the design of input filter is of major concern. A systematic input filter design approach has been presented, which takes into consideration the amplification factors, carrier frequency and suppression of carrier harmonics. Then, validity of this approach has been demonstrated on the application prototype of the CSC based APF by taking into account the ratings of the filter equipment. In order to reduce the kVA rating of the CSC for a given application, the gain of the input filter at each pre-selected frequency should be higher than unity. In this manner, the natural frequency of the input filter of the application prototype was chosen as 780 Hz, and hence, the amplification factors 1.99 and 3.50 have been achieved for the 11^{th} and 13^{th} harmonic components, respectively. Hence, the assumption made for the quality factor of the input filter during the design phase, that is 75, and the theoretical amplification factors of 2.05 and 3.35, respectively for the 11^{th} and 13^{th} harmonic components, have been verified. As a result, a 2.19 p.u. APF rating has been achieved by using a 1.0 p.u. CSC rating.

Since the CSC based APFs have an LC-type input filter on the ac side to eliminate the switching ripples, oscillations around the natural frequency of this filter are unavoidable. To suppress these oscillations, a new, modified active damping method, which is based on SRFM, has been proposed. By use of this method, the selected harmonic components such as 11^{th} and 13^{th} are not attenuated, and the amplification factors of the input filter at those frequencies are kept the same, while the undesired oscillations around the natural frequency of the input filter are damped out satisfactorily. Hence, the proposed active damping method makes the SHAM applicable by keeping the amplification factors of the selected harmonics, higher than unity.

As a part of the input filter design issue, suppression of the carrier harmonics has been also discussed, and a carrier frequency of 3.0 kHz was chosen for the corresponding designed input filter, for which the natural frequency of 780 Hz provides more than 90 % filtering of the carrier harmonics. Then, sizing of the filter elements, filter capacitor in particular, has been analyzed for the required amplification factors, and the chosen carrier frequency. Since the amplified CSC harmonic currents are circulating through the input filter capacitors, their rms current and voltage ratings have been selected according to the actual APF rating.

In order to keep the effective switching frequency of the semiconductor devices at an optimum value, some high performance PWM methods have been analyzed, and among them, DSPWM was chosen as the modulator to be used in the application prototype, because of its better performance as compared to SVPWM method in view of the magnitudes of the low order harmonics. Owing to the DSPWM, the effective switching frequency of the semiconductor devices has been reduced almost to the 2/3 of the carrier frequency, and an ac gain of 1.0 has been achieved.

Total power dissipation of the CSC for rated operation of APF, including all losses of the snubber and discharge resistors, has been found as 11.0 kW, 21.2 % of which account for the dc-link losses, and the rest is for the converter losses. The power dissipation of the converter has been found as 12.0 kW theoretically, for the rated operation of APF. The difference between the theoretical (12 kW) and the actual (8.6 kW) one is because of the design approach, which takes into account always the worst cases. However, this high capacity of the cooling system provides to operate the APF at higher kVA values.

The application prototype of the 450 kVA CSC based APF is composed of a three phase full-bridge 205 kVA CSC and a 95 kVAr input filter capacitor with a nominal voltage of 2.7

kV rms taking into account the harmonic loading. It is connected to MV bus via a coupling transformer, which is 1600 kVA, 34.5 /1.1 kV with 5.77% U_k. The leakage inductance of the coupling transformer has been used as the series filter inductance, thus eliminating the need for an extra series inductance, and making the circuit topology simple and cheap. As the switching elements, HV IGBT modules in series with HV fast-recovery diode modules have been used. In order to make sure a reliable operation, the layout of the power stage has been designed carefully to minimize the stray inductances, and the turn-on characteristics of the IGBTs have been adopted by changing the gate turn-on resistances for reducing the high di/dt during reverse recovery period of the diodes. Besides, the control system has been designed and implemented with some special features to protect the CSC from overvoltages and overcurrents, especially on the dc side.

Following major conclusions can be drawn from the results of theoretical and experimental work carried out within the scope of this research work:

- It is possible to reduce the kVA rating of the CSC by the proposed SHAM, and to make the CSC based APF a loss and cost competitive alternative to the VSC based APF.
- The proposed method can be used not only for single harmonic group such as 11^{th} and 13^{th}, but also for more than one harmonic groups, such as all of 5^{th}, 7^{th}, 11^{th} and 13^{th}.
- The use of active damping method to suppress the non-selected harmonics of APF, which also eliminates the need of an extra series filter inductance for damping purpose, thus making the system simple and cheap.
- The design approach makes simple the connection of the CSC based APF to any MV level busbar via a coupling transformer.
- Using HV IGBT and diode modules with isolated cases makes the system reliable, and provides the use of either forced-air or water cooling.
- The flexibility of changing the gate turn-on and -off resistances of the gate drive units provide the opportunity to compensate for the undesired switching characteristics of the semiconductor device arising from power circuit layout, or device characteristics.

An important consequence of this study is that the application of CSC based APF becomes practical and viable in view of efficiency and cost, owing to the application of the proposed

SHAM. By this way, the advantageous features of CSC over VSC, such as the inherent short-circuit protection, direct current control, and low switching ripples in input current have become implementable in APF applications.

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APPENDIX A

ANALOG CIRCUIT REPRESENTATION OF THE DSPWM BASED PATTERN GENERATOR

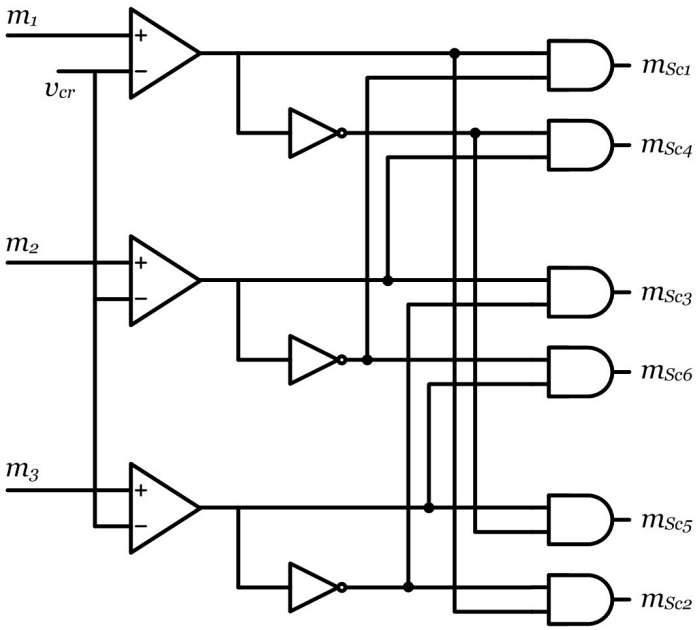

Figure A.1: Analog circuit representation of bilogic to trilogic translation

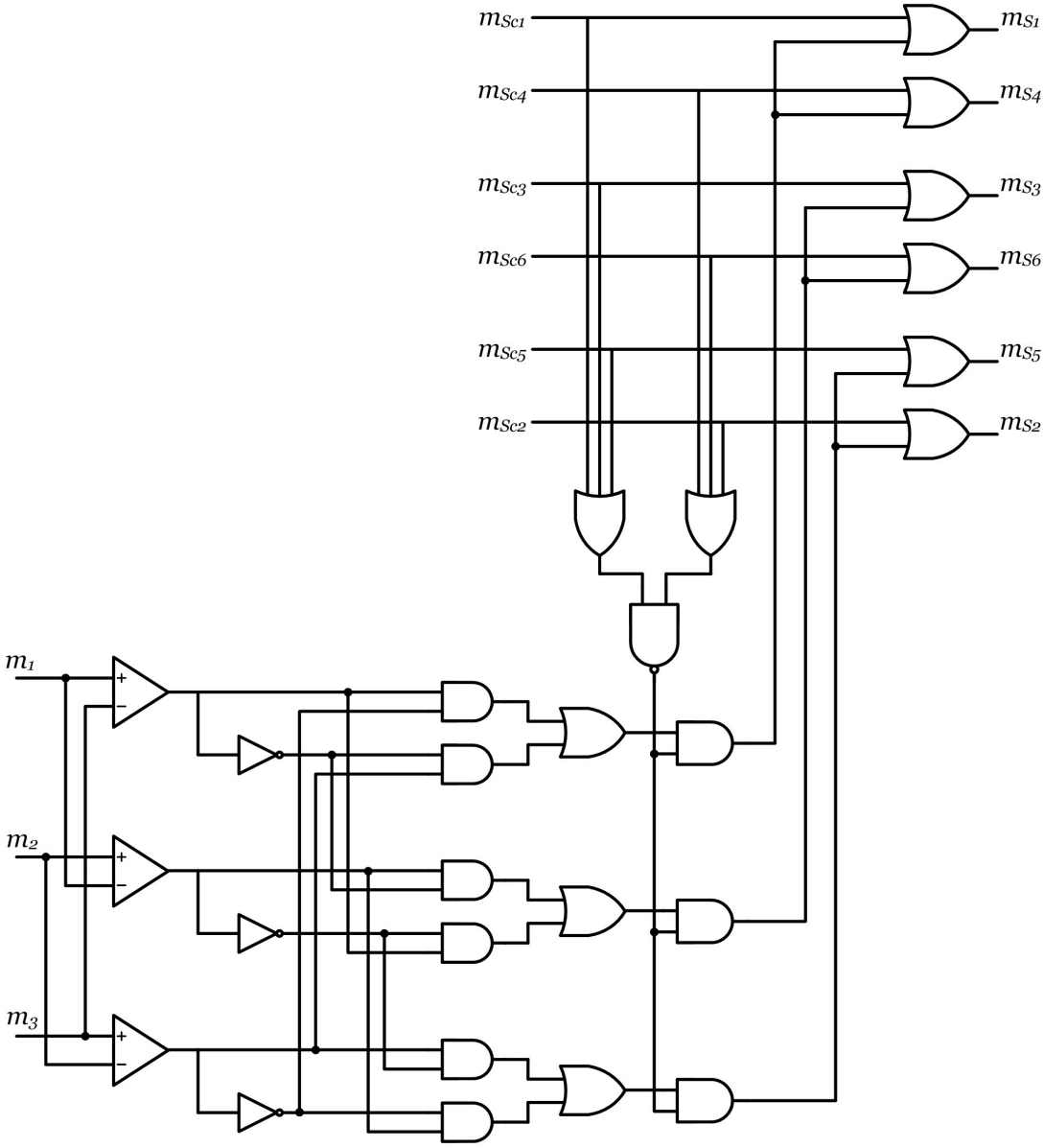

Figure A.2: Analog circuit representation of the shorting pulse generator and distributor

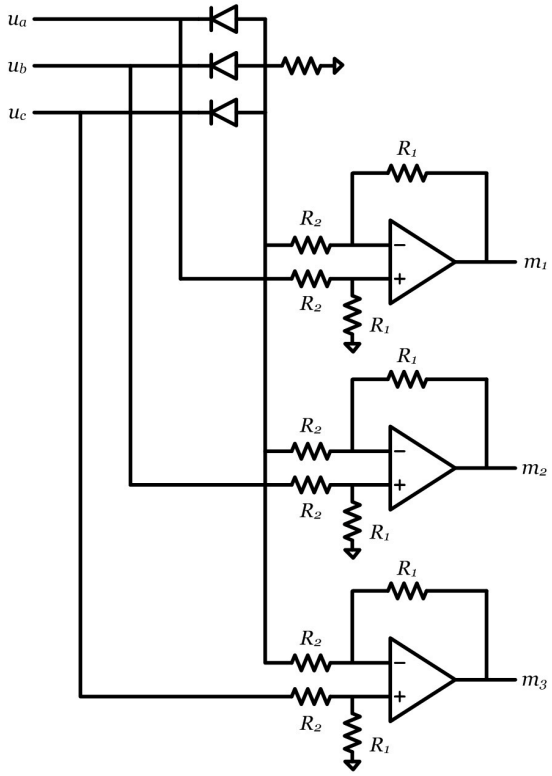

Figure A.3: Analog circuit representation of the modulating waveform generation

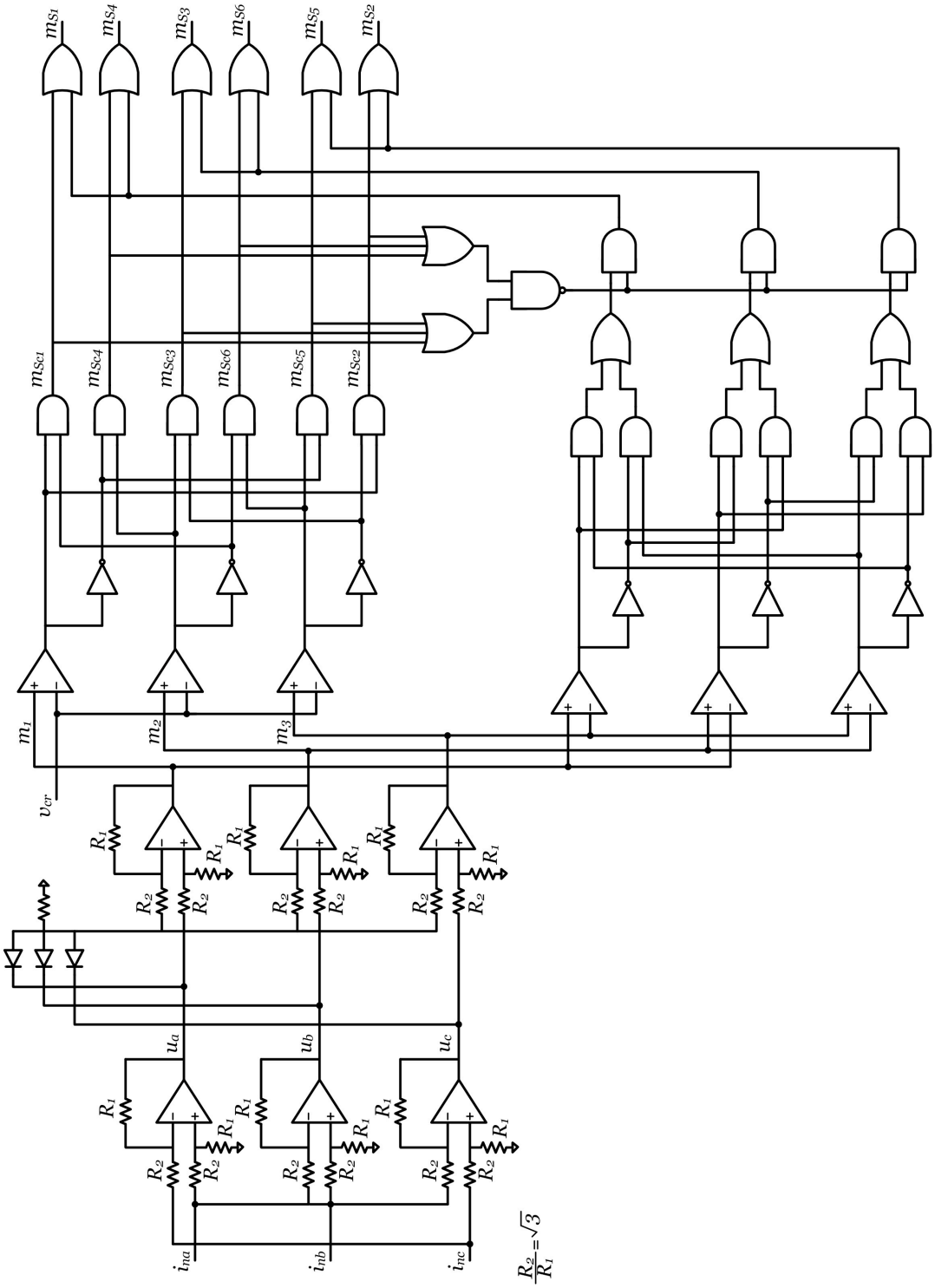

Figure A.4: Analog circuit representation of the overall pattern generation

APPENDIX B

FORTRAN CODE OF THE ON-LINE PATTERN GENERATOR CONSTRUCTED IN EMTDC/PSCAD

Decoupling Part

```
uax=(aref-cref)/SQRT(3)
ubx=(bref-aref)/SQRT(3)
ucx=(cref-bref)/SQRT(3)
```

Dead-band Generation

```
IF ((uax<=ubx) .AND. (uax<=ucx)) THEN
vmin=uax
ELSEIF ((ubx<= uax) .AND. (ubx<=ucx)) THEN
vmin=ubx
ELSE
vmin=ucx
ENDIF
ua=(uax-vmin)/SQRT(3)
ub=(ubx-vmin)/SQRT(3)
uc=(ucx-vmin)/SQRT(3)
```

Bi-logic Signal Generation

```
IF (ua>=car) THEN
Sa1=1
```

```
ELSE
Sa1=0
ENDIF
IF (ub>=car) THEN
Sa2=1
ELSE
Sa2=0
ENDIF
IF (uc>=car) THEN
Sa3=1
ELSE
Sa3=0
ENDIF
```

Bi-logic to Tri-logic Mapping

```
Sa1N=1-Sa1
Sa2N=1-Sa2
Sa3N=1-Sa3
Sc1=Sa2*Sa1N
Sc2=Sa3*Sa2N
Sc3=Sa1*Sa3N
Sc4=Sa1*Sa2N
Sc5=Sa2*Sa3N
Sc6=Sa3*Sa1N
```

Shorting Pulse Generation

```
IF (ua>=uc) THEN
Sb1=1
ELSE
Sb1=0
ENDIF
```

IF (ub>=ua) THEN

Sb2=1

ELSE

Sb2=0

ENDIF

IF (uc>=ub) THEN

Sb3=1

ELSE

Sb3=0

ENDIF

Sb1N=1-Sb1

Sb2N=1-Sb2

Sb3N=1-Sb3

Se1=Sb1*Sb3+Sb1N*Sb3N

Se2=Sb2*Sb1+Sb2N*Sb1N

Se3=Sb3*Sb2+Sb3N*Sb2N

Sd=1-((Sc1+Sc2+Sc3)*(Sc4+Sc5+Sc6))

Shorting Pulse Distribution

S1=(Sc1+Sd*Se1)

S2=(Sc2+Sd*Se2)

S3=(Sc3+Sd*Se3)

S4=(Sc4+Sd*Se1)

S5=(Sc5+Sd*Se2)

S6=(Sc6+Sd*Se3)

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