INVESTIGATION OF ELECTRICAL AND OPTICAL PROPERTIES OF Ag-In-Se BASED DEVICES

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ABSTRACT

INVESTIGATION OF ELECTRICAL AND OPTICAL PROPERTIES OF AG-IN-SE BASED DEVICES

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Ternary chalcopyrite compound semiconductors have received much attention as the absorbing layers in the polycrystalline thin film solar cell structures. Most widely used one is $CuInSe_2$ and $CuInGaSe_2$ structures, but there are some diffusion problems with copper atoms in the structure. On the other hand, $AgInSe_2$ is promising material with several advantages over the $CuInSe_2$. The aim of this study was to investigate and optimize the production and post-production methods of the Ag-In-Se thin film based heterostructure devices. In this study Ag-In-Se thin films were deposited on glass, ITO coated glass and Si wafer substrates by thermal evaporation and RF/DC sputtering methods. The structural, electrical and optical properties of the devices were investigated.

The XRD measurements of the thermally evaporated films showed that as-grown films in amorphous nature. By annealing the films under nitrogen atmosphere, the AIS films turn to polycrystalline structure which including $AgIn_5Se_8$ and $\delta - In_2Se_3$ multi-phases with n-type conductivity. p-Si/n-AIS heterojunctions showed very good diode behavior with 4 order rectification factor. Anneal-

ing under nitrogen atmosphere decreased the series resistance of the devices and calculated solar cell conversion efficiency and fill factor of devices increased up to n=2.6% and $FF = 63$, respectively.

The XRD measurements of layer-by-layer sputtered AIS films were showed that as-grown films amorphous in nature. The AIS thin films were annealed at 300^{o}C temperature under selenium ambient and mono-phase $AgInSe_2$ with desired p-type conductivity were obtained. n-Si/p-AIS heterojunctions showed very good diode behaviors with 6 order rectification factor.

The results of the study showed that AIS thin film has a photoresponce maximum which is exactly matching with solar photon energy maxima. High series resistance of the devices increases the recombination in the junction and this results in the lower solar conversion efficiency. The adequate electrical, optical and structural properties of the AIS thin films reveals that p-AIS thin films could be used as a solar cell absorber layer with an appropriate window layer, such as CdS.

Keywords: Ag-In-Se, solar cell, heterostructure, efficiency, semiconductor

ÖZ

AG-IN-SE TABANLI AYGITLARIN ELEKTİRİKSEL VE OPTİK OZELLİKLERİNİN TESPİT EDİLMESİ

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Üçlü kalkopirit bileşik yarıiletkenler, polikristal ince film güneş pili yapılarında büyük ilgi sahibidirler. En yaygın olarak kullanılanları $CuInSe_2$ ve $CuInGaSe_2$ yapılarıdır, ancak yapıdaki bakır atomlarının difüzyon problemleri vardır. Diğer taraftan, $AgInSe_2$, $CuInSe_2$ göre çeşitli avantajlarıyla, umut verici bir malzeme olarak görünmektedir. Bu çalışmanın amacı Ag-In-Se ince film tabanlı farklı-yapı aygıtlarının üretimi ve üretim sonrası yöntemlerini araştırmak ve optimize etmektir. Bu çalışmada Ag-In-Se ince filmler cam, ITO kaplı cam ve Si yonga alttaşlar üzerine ısıl buharlaştırma ve RF/DC saçtırma yöntemleriyle biriktirildi. Aygıtların yapısal, elektiriksel ve optik özellikleri araştırıldı.

Isıl buharlaştırılmış filmlerin XRD ölçümleri, büyütme sonrası filmlerin düzensiz yapıda olduklarını gösterdi. AIS filmler, azot altında tavlamayla, n tipi iletkenlikle birlikte, $AgIn_5Se_8$ ve $\delta - In_2Se_3$ çoklu fazlarını içeren polikristal yapıya dönüştü. p-Si/n-AIS farklı-eklemler üstel 4 derece doğrultma faktörü ile oldukça iyi diyot davranışı gösterdi. Azot atmosferi altında tavlama, aygıtların seri direncini düşürdü ve güneş pili çevirim verimi ve doldurma çarpanını sırasıyla

n=2.6% ve $FF = 63$'e kadar yükseltti.

Katman-katman saçtırılmış AIS filmlerin XRD ölçümleri, büyütme sonrası filmlerin düzensiz yapıda olduklarını gösterdi. AIS filmler selenyum ortamında 300^{o}C sıcaklıkta tavlandı ve istenilen p tipi iletkenlikte tek-faz $AgInSe_2$ elde edildi. n-Si/p-AIS farklı-eklemler üstel 6 derece doğrultma faktörü ile çok güzel diyot davranışı gösterdi.

Çalışmanın sonuçları gösterdiki; AIS ince filmler güneş foton enerji maksimumu ile eşleşen fototepki maksimumuna sahiptir. Aygıtların yüksek seri direnci, eklemdeki yeniden birleşimi artırır ve bu düşük güneş çevirim verimi ile sonuçlanır. AIS ince filmlerin yeterli elektiriksel, optik ve yapısal özellikleri ortaya çıkarır ki p-AIS ince filmler CdS gibi uygun bir pencere katmanıyla güneş pili soğurucu katmanı olarak kullanılabilir.

Anahtar Kelimeler: Ag-In-Se, güneş pili, hetero yapı, verimlilik, yarıiletken

To my parents

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CHAPTER 1

INTRODUCTION

In the last century, world energy consumption has been increased dramatically and most of the energy production has been supplied by fossil fuels and nuclear energy. These "old energy sources" may be sufficient to cover for an extra century, but limited availability of the fossil fuels and environmental problems such as air pollution, storing problem of the nuclear waste and the increase of the 0.6 ^{0}C of the global temperature over the last century (global warming) concerned the mankind to search for long-term renewable energy solutions [1].

The renewable energy sources, their applicability and efficiencies of these sources are most discussed matter in these days. There are several renewable energy sources such as; solar energy, wind energy, rain, geothermal energy, tides and etc. Among these sources, the longevity, cost-effectivity and clean properties make the solar energy best alternative. Beside these properties, all life on earth is depend on solar energy in someway. The solar energy conversion consist of two main step; absorption of solar photon radiation and yield of chemical energy which takes place in every materials and the creating electrical energy by generating current and voltage [2]. The solar energy conversion to electrical energy made by solar cell devices (photovoltaics) which consist of semiconductor materials. By absorption of light within semiconductor, electron and hole carriers are generated by photovoltaic effect, first recognized in 1839 by Becquerel. First solar cell invented by Charles Fritts in 1883 but Chapin et. al accidently found the first 6% efficient silicon solar cell at Bell labs in the 1950's and this event started the modern age of solar power [3]. Today, photovoltaic cells are made of

bulk (wafer-based / first generation) or thin film form (inorganic layers, organic polymers / second generation) of materials. A thin film is a two dimensional material deposited on a substrate by means of the random nucleation and growth processes of separately condensing and reacting of atomic, ionic and molecular species. Many currently available solar cells are made by crystalline silicon because it is stable and it has highest efficiency (%25.0 $\pm$0.5) which is close to theoretical limit (%30) [4, 5]. Silicon has many advanced properties but crystalline Si cell production needs more material (typical thickness $\sim 300\mu m$) and has high cost production method, it is fragile and it also has indirect band-gap.

$$\begin{pmatrix} Cu \\ Ag \\ Au \end{pmatrix} \begin{pmatrix} Al \\ Ga \\ In \end{pmatrix} \begin{pmatrix} S_2 \\ Se_2 \\ Te_2 \end{pmatrix}$$

Thin film form of solar cells devices are promising approach for photovoltaics by economical processing, a variety of depositing methods, flexibility properties, doping and passivating properties, allowance of wide range band gap engineering and etc. In last decades, there are many research group worked on thin film growth methods and characterization (Fig.1.1) [6, 7]. Especially ternary and quaternary chalcopyrite based materials (Potential combinations of (I, III, VI) elements in the periodic table) has great attraction because of their high optical absorption coefficients, skilled optical and electrical characteristics which can be handeled and calibrated a specific need by changing constituent elements ratio and can be used as detectors, solar cells, light emitting diodes, modulators, nonlinear optics and etc. [8–11]

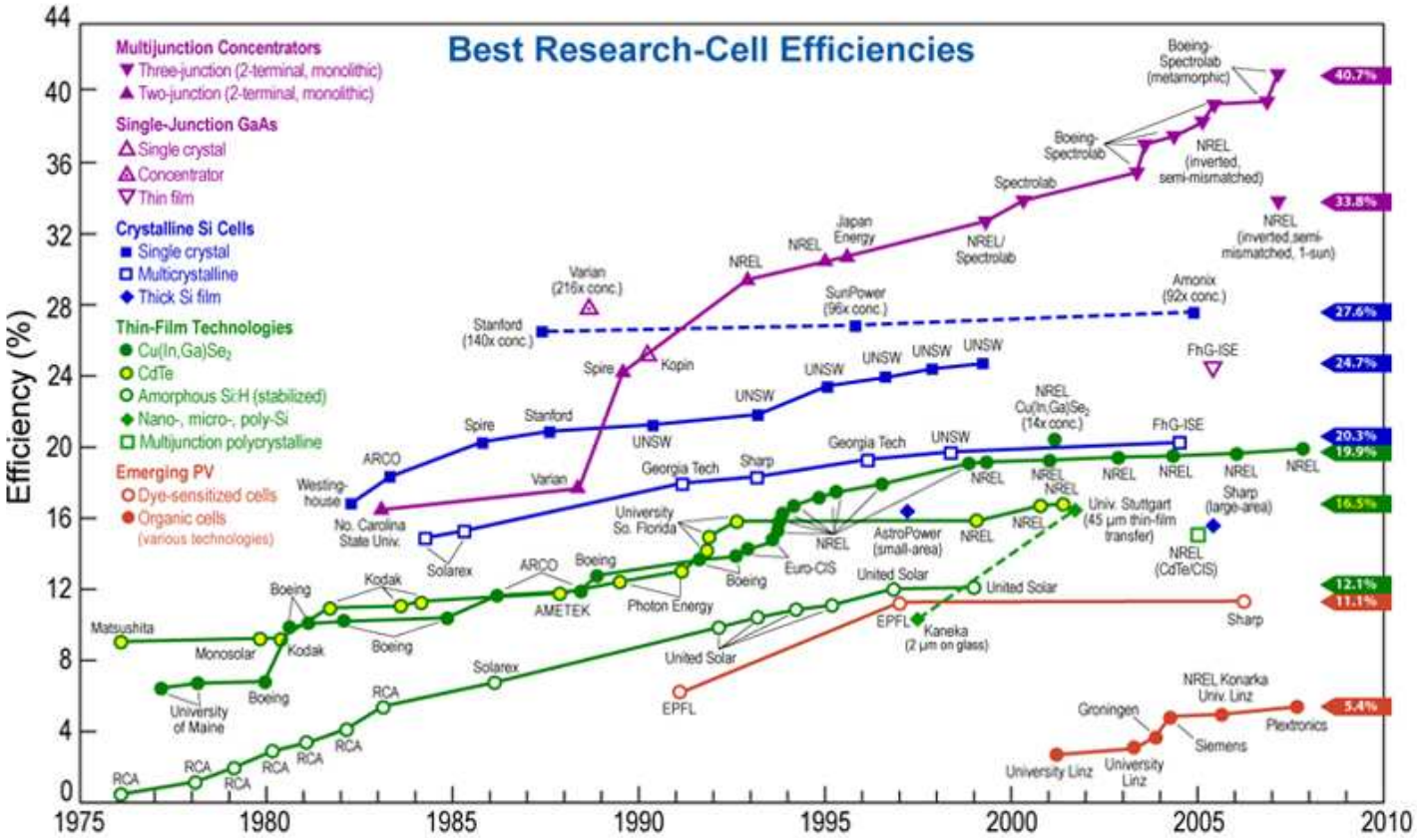

Figure 1.1: Best research cell efficiencies in 2008.

Among this chalcopyrite semiconductor compounds, the first heterojunction solar cell was produced by Kazmerski et al. in the form of $CuInSe_2/CdS$ structure with an 5.7% efficiency in 1976 [12]. Today, the copper indium gallium diselenide (CIGS) thin film solar cell recently reached 19.9%, setting a new world record for this type of cell in the National Renewable Energy Laboratory (NREL). This efficiency is matching to multicrystalline silicon-based solar cells efficiencies as high as 20.3% [7]. In addition to this high efficiency, CIGS thin films semiconductor have wide range band gap values, they have optimum opto-electronic properties and good outdoor stability [13]. Today mono-Si and multi-Si crystalline solar cells are leading the photovoltaics market but CIGS type solar cells are increasing continuously their portion especially in the printed solar cell devices market (Fig. 1.2) [6].

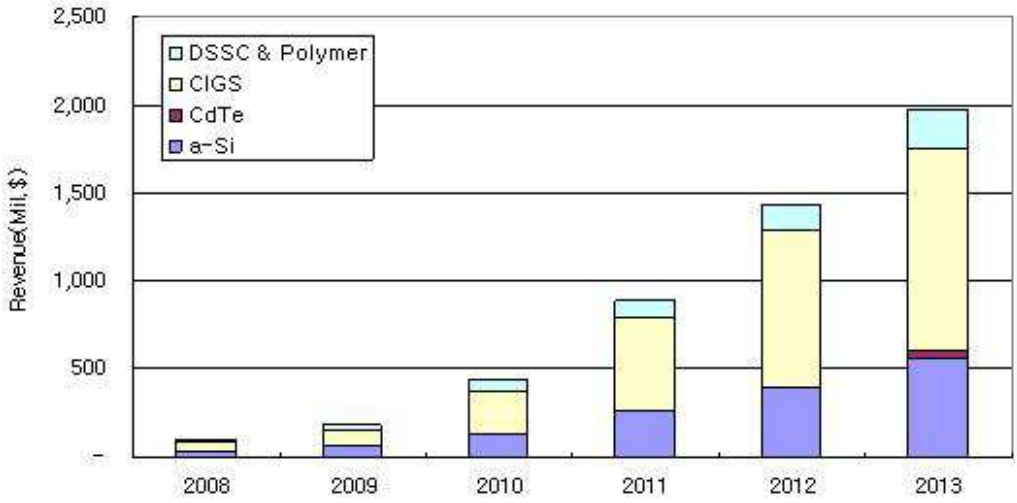

Figure 1.2: Printed solar cell market forecast in 2009.

On the other hand, there are several problems about CIS and CIGS noncrystalline thin films because of the poor material utilization and obtaining uniform thin films over large area substrates. Because of the high diffusion coefficient, Cu atoms in the structure cause shorting effect and this effect increases recom-

bination of generated charge pairs and decreases conversion efficiency [14]. The band gap of CIS is 1.04 eV and it is smaller than the ideal value of 1.35 eV for absorbtion of the average energy of solar photons [15]. Recently, alternative chalcopyrite materials have been worked out to solve this problem [16–18]. Among these materials, silver based ternary chalcopyrite semiconductors (silver indium diselenide (AIS)) differs from the others with wider band gap (1.24 eV), higher optical absorption coefficient and lower melting point [19]. AIS films are used as an absorber layer by using different deposition methods. Recently 9% efficient p-$AgInSe_2$/n-Si solar cells have been produced by laser deposition technique [20]. Wide-band-gap $Ag(In_{1-x}Ga_x)Se_2$ thin films have been deposited on Mo-coated soda-lime glass substrates by using a molecular beam epitaxy (MBE) system with an efficiency of 10.2% [21]. However, studies on silver based ternary and quaternary chalcopyrite semiconductors as solar cell absorber is not enough. The deposition methods, electrical and optical characterization of AIS materials are need to worked out.

In a nutshell, there are four generation of solar cells with paralleling the historical inventions of solar cell materials. First generation photovoltaic cells are the single crystalline and multi crystalline silicon solar cells which have the dominant part in the commercial production of solar cell market. The second generation photovoltaic cells are based on the use of thin-film semiconductors such as amorphous silicon, CdTe, CIGS and etc which has promising increase in efficiency and lowering production cost properties. Third generation photovoltaic cells are more advanced version of the thin-film cells such as tandem-multi junction cells, non-semiconductor technologies, quantum dots and etc. which has the best efficiency result by using sophisticated material and band gap designing. Fourth and newer generation photovoltaic cells are composite photovoltaic technology which is combining elements of the solid state and organic cells (hybrid - nanocrystal/polymer cells).

Today many scientific groups are working on solar cells and these works can be grouped into three main subjects;

-finding newer material and characterization of this materials,

-lowering the production cost by using different growth methods,

-inventing new device mechanism (band gap engineering and contact perfection).

Accordingly, the aim of this study to investigate electrical, optical and device properties of silver based ternary chalcopyrite semiconductor (AIS) thin films deposited by thermal evaporation, electron beam evaporation and (RF-DC) sputtering methods. The main goal is to optimize the opto-electronic properties of AIS thin films and making a solar cell in the form of a heterostructure device by depositing the AIS films on p and n type Si and indium thin oxide (ITO) substrates using different evaporation method under high vacuum. The structural properties of AIS films on glass substrate were studied by X-ray Diffraction (XRD) analysis. Al back and In transparent front contacts were deposited on Si substrates and on AIS films by thermal evaporation method to construct Al/Si/AIS/In heterostructure. The effect of thermal annealing process at different temperatures were studied under the nitrogen atmosphere to enhance the physical properties of the devices. The electrical properties of the heterojunction devices have been investigated by means of current-voltage (I-V), temperature dependent current-voltage measurements in the range of 160-360 K and frequency dependent capacitance-voltage measurements (C-V-f). Optical properties and solar conversion efficiency of AIS devices were studied by spectral response measurement in the wavelength range of 500-1260 nm and under AM1 conditions.

In the second chapter of the thesis, basic theoretical fundamentals about the structural and opto-electrical properties of thin films, metal semiconductor junction (Schottky Diode), heterojunction and solar cell energy conversion are given. In the third chapter, the experimental procedures on the deposition of AIS thin films for the fabrication of heterostructure devices, the measurement techniques and setups are summarized. In the chapter four the structural, electrical and optical properties of the fabricated Al/Si/AIS/In devices are discussed over the results presented. Finally, the key results of this work are summarized and conclusions are drawn.

CHAPTER 2

THEORETICAL CONSIDERATIONS

2.1 Introduction

This chapter is intended as a brief presentation of fundamental information about chalcopyrite based thin film semiconductors, metal semiconductor junction, n-p heterojunction and solar cell device mechanism to explain experimental results obtained by structural characterization and opto-electrical measurements.

2.2 General Properties of Chalcopyrite Thin Films

Thin films are thin material layers of a substance deposited on substrate ranging from fractions of a nanometer to several micrometers in thickness and they have great potential in the photovoltaic industry. Thin films solar cells have many advantages according to wafer based photovoltaic modules because of the cost reduction potential using small amount of material and energy consumption, smaller dimension, fragility and flexibility properties. In recent years, many groups work on chalcopyrite semiconductors with wide band gaps to increase solar cell conversion efficiency by using as an absorber closer to optimum solar spectrum [22]. Today, copper based chalcopyrite absorbers (CIGS) show the best performance among thin film solar cells but there are also some problems [23]. Some important points of the Cu(In,Ga)(S,Se) thin film solar cells are listed below:

- The chalcopyrite absorbers are polycrystalline film with wider grain size so electronic activity of grain boundaries and extended defects inordinately low. Also, these wide gap semiconductors absorbers have better temperature coefficient and they are stable under radiation so suitable for space applications [24].

- The heterojunction contact between two non-lattice matched materials potentially decreases solar conversion efficiency because of the interface recombination via a high density of interface states. Special feature of a Cu poor layer on the surface of CIGS thin film suppress interface recombination.

- Molybdenum back contact enables excellent ohmic properties with CIS cells by forming $MoSe_2$ film on top of the Mo layer during absorber growth [25].

- CIGS films have different chemical elements and this complicate the structure and electronic properties by different intrinsic defects. The occurrence of several Cu poor phases such as $CuIn_3Se_5$ and $CuIn_5Se_8$ can be explained by this complexes and this results as wider band gap energies [26, 27].

- Some works showed that, $CuInSe_2$ tends to be p-type under Se excess or Cu excess conditions and n-type under Se deficient conditions [28, 29].

- CIGS films are direct gap semiconductors and this gap can be controlled by changing constituent elements in between 1.05 eV ($CuInSe_2$) and 2.5 eV ($CuGaS_2$) and therefore these materials suitable for tandem solar cell applications.

There are a lots of work about Cu based chalcopyrite semiconductors absorbers for solar cell applications. Still, there are some problems of CIS semiconductor absorbers which cause decrease solar cell efficiency. CIS band gap value is around 1.1 eV which is higher than previous thin films materials but still low for optimum solar spectrum at 1.35 eV. Additionally, Cu leaks out of Cu based chalcopyrite and this leakage causes defects and also causes shorting effects [23, 30, 31].

2.2.1 The Chalcopyrite Structure

The chalcopyrite is a chemical composition $CuFeS_2$ which crystallizes in the tetragonal system and it is a prototype of $A^I B^{III} C_2^{VI}$ ($A \equiv \mathrm{Cu, Ag}$, $B \equiv \mathrm{Al, Ga, In, Tl}$, and $C \equiv \mathrm{S, Se, Te}$) crystal structure [23]. In this structure, each cation atoms, A and B, is tetrahedrally coordinated to four anion atoms, C, while each C atom is tetrahedrally interconnected to two A atoms and two B atoms in an orderly fashion by dominantly covalent (sp^3 hybrid) bonds [19]. The tetragonal unit cell structure can be seen in Fig. 2.1.

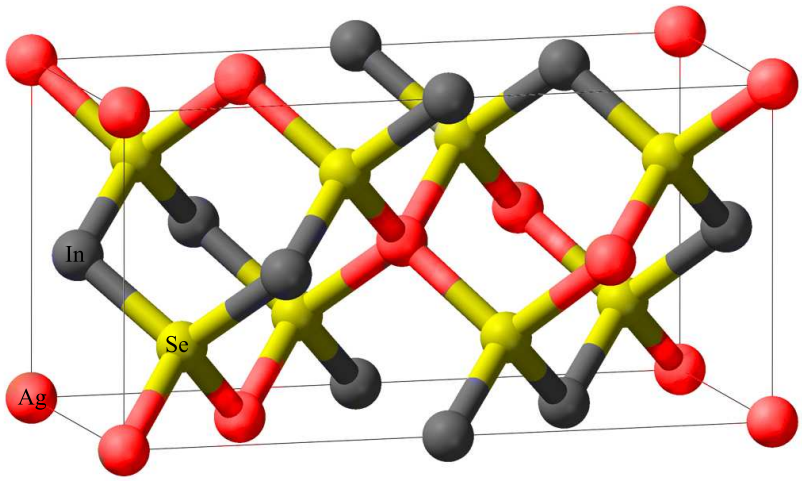

Figure 2.1: The tetragonal unit cell structure for the $AgInSe_2$ chalcopyrite crystal.

The ideal c/a ratio of a chalcopyrite slightly equal to 2 and chalcopyrite compounds can be described as the ternary analogs of the $D^{II}C^{VI}$ binary compounds ($D \equiv \mathrm{Zn, Cd}$). Table 2.1 lists some structural and electronic parameters for Cu and Ag based chalcopyrite semiconductor [19].

2.2.2 Ag Based Chalcopyrite Thin Films

Chalcopyrite type $AgInSe_2$ (AIS) is a direct band gap semiconductor with a band gap of 1.24 eV. There are also three distinct transitions in electronic band

Table 2.1: The experimentally determined structural and electronic parameters of some chalcopyrite semiconductors

Ternary Phase	a (Å)	c/a	E_g (eV)	Reference
$CuInSe_2$	5.782	2.009	1.04	[32]
$AgInSe_2$	6.090	1.916	1.24	[33]
$AgGaSe_2$	5.985	1.793	1.83	[32]
$AgGaTe_2$	6.283	1.897	1.20	[33]
$AgGaS_2$	5.755	1.786	2.70	[23]
$AgInS_2$	5.816	1.920	1.86	[23]

structure at 1.24, 1.32 and 1.60 eV calculated energy values [34]. By introducing Ga in AIS structure results AIGS quaternary semiconductors and band gap value can be altered similar to Cu based chalcopyrite (CIGS) by this way. AIGS has several advantages over CIGS such as;

- The band gap energy of AIGS films is wider than CIGS by 0.2 eV and closer to optimum solar spectrum value (1.35 eV) [35].

- The melting point of AIGS film is lower than CIGS by 200 ^{0}C and commercially more preferable [16].

$AgIn_5Se_8$ and $Ag_3In_5Se_9$ are two different tetragonal phase of AIS films and they are crystallized in space group $P\bar{4}2m$ and P4 or P4mm. $AgIn_5Se_8$ and $Ag_3In_5Se_9$ semiconductor compounds having 4.57 and 4.24 electrons per atom respectively are the isostructural derivatives of binary compounds of In_2Se_3, CdSe and Ag_2Se with 4.80 electrons per atom [36–38]. Band gap value of polyphase AIS films which including $AgIn_5Se_8$ and $Ag_3In_5Se_9$ phases is 1.57 eV and also three distinct transitions in electronic band structure at 1.57, 1.80 and 2.01 eV [39].

2.3 Semiconductor Device Physics

The basic physical process underlying the operation of a semiconductor device include various carriers transport mechanism, generation/recombination and electro-optical interactions. In this section, brief theoretical descriptions of some of these processes are given.

A material whose resistivity is lying in the range of $10^{-2} - 10^{9}\ \Omega - cm$ (metal-insulator) is called a semiconductor. It can be classified as intrinsic or extrinsic according to the purity. They can also be classified as n-type or p-type, depending on their majority carriers either electrons or holes. In addition to these, they can also be classified as single crystal, amorphous or polycrystalline based on their structure properties. Adding impurity atoms to a semiconductor to change the charge concentration is called doping. Defect levels and doping changes the semiconductor conductivity and shift the balance of electron and holes in the structure by changing their concentrations.

Each semiconductor has unique band structure due to the configuration of the energy level. The band gap E_g of a semiconductor is defined as separation between the top of valance band energy (E_v) and the bottom of conduction band energy (E_c). Band diagram of a semiconductor can be seen in Fig. 2.2. Here, the work function (ϕ) of a material is defined as the minimum energy that required removing an electron from the fermi level (E_f) to vacuum level. The electron affinity (χ) of a semiconductor is defined as the minimum energy required removing an electron from the conduction band level to vacuum level.

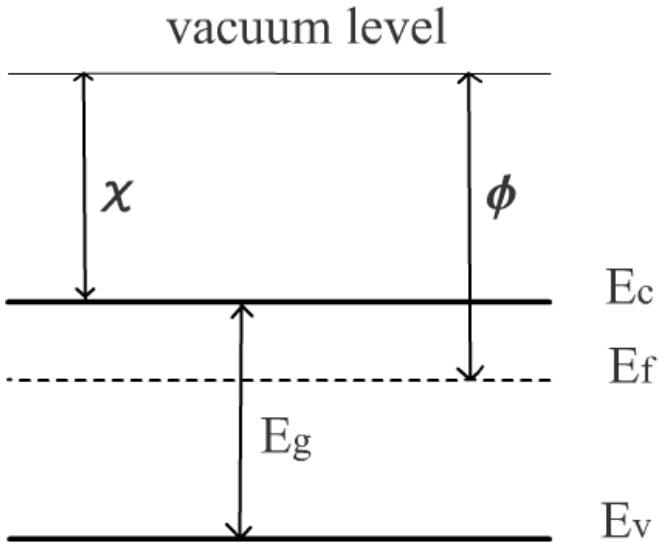

Figure 2.2: Energy band diagram of a n-type semiconductor.

The occupied states of conduction band and valance band states is governed by Fermi-Dirac statistics,

$$F(E) = \frac{1}{1 + exp(\frac{E-E_f}{kT})} \tag{2.1}$$

where k is Boltzmann constant and T is absolute temperature. This equation give the probability of charge occupation in a given energy state and if the Fermi level (E_f) is not close the band edges (kT$\ll$ Ec-E_f or kT$\ll$ E_f-Ev) this equation reduce to Boltzmann factor,

$$exp(-\frac{E - E_f}{kT}) \tag{2.2}$$

The free carrier density in a semiconductor valance and conduction band edge given as,

$$n = N_c exp(-\frac{Ec - E_f}{kT}) \tag{2.3}$$

$$p = N_v exp(-\frac{E_f - Ev}{kT}) \tag{2.4}$$

where N_c and N_v are effective densities of states at band edges.

$$N_{c,v} = 2\Big(\frac{2\pi m^*_{n,p} kT}{h^2}\Big)^{\frac{3}{2}} \tag{2.5}$$

where $m^*_{n,p}$ is electron and hole effective masses. In equilibrium case, the n and p product is constant and change only by temperature, m^* and E_g.

$$np = n_i^2 = Nc.Nv.exp(-\frac{E_g}{kT}) \tag{2.6}$$

Under illumination or external applied bias (V) uniformity of Fermi level disturbed and Eqn.2.6 becomes;

$$np = n_i^2.exp(\frac{qV}{kT}) \tag{2.7}$$

Further information on properties of semiconductor and junctions can be found in many semiconductor textbooks [40].

2.3.1 Semiconductor Junctions

2.3.1.1 Schottky and p-n Junctions

When a metal and a semiconductor brought in contact with each other charge transfer occurs until the Fermi levels of two materials align to achieve equilibrium. If majority carriers are injected from semiconductor to metal a band bending occurs and give rise to a potential difference called contact potential (build in potential V_{bi}). This type metal-semiconductor junction is called Schottky junctions. This band bending results a barrier for majority carriers flow from the semiconductor to the metal and this barrier height is given by

$$q\phi_{barrier} = q(\phi_{metal} - \chi) \tag{2.8}$$

Similarly, n and p type semiconductors brought in contact with each other p-n junction is formed and electrons diffuse into the p-type material, leaving behind ionized donor levels, and holes diffuse into n-type material leaving behind ionized acceptor. This diffusion process counterbalanced by an internal electric field which is opposes diffusion process for electron and holes at p-n interfaces up to equilibrium state reached. At interface both semiconductors deplete of free carriers and a space charge region (depletion region) is created. If p-type and n-type semiconductors are the same materials this junction called as homojunction, other wise heterojunction.

The carrier transport mechanisms for polycrystalline semiconductors can be defined as thermionic emission, tunneling between the grain boundaries or interface states, recombination in space charge and hopping between localized states. The ideal current-voltage characteristic of a p-n junction (diode) in the dark can be approximated by using Shockley diffusion model and given by

$$J = J_0\Big[exp\Big(\frac{qV}{nkT}\Big) - 1\Big] \tag{2.9}$$

where n is the diode ideality factor and J_0 is the saturation current density which is given by equation

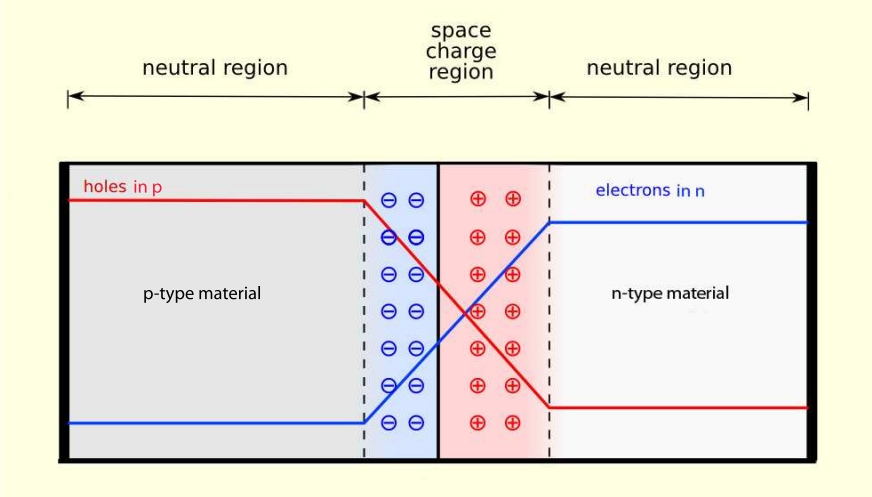

Figure 2.3: A p-n junction at thermal equilibrium under zero bias voltage.

$$J_0 = \frac{qD_p p_n}{L_p} + \frac{qD_n n_p}{L_n} \tag{2.10}$$

where n_p is the electron concentration in p region, p_n is hole concentration in n region, $D_{p,n}$ and $L_{p,n}$ are minority carrier diffusion coefficients and diffusion lengths in p and n regions respectively. By using Einstein relationship and equilibrium condition saturation current can be described as

$$J_0 = \left(\frac{qD_p n_i^2}{L_p N_a} + \frac{D_n n_i^2}{L_n N_d}\right) \tag{2.11}$$

2.3.1.2 Heterojunctions

A heterojunction is a p-n junction formed between two different semiconductors. Heterojunction devices are more complicated than homojunctions because of the different band gaps and electron affinities. This complexness causes discontinues (spike) in the band bending called band offset. If these spikes are large enough, they act as a barrier and directly affects the current flow. There are three types of heterojunction which are shown in Fig.2.4.

The current transport models for heterojunctions are development of customary models for homojunctions. As seen in Fig.2.5 spikes in the band edges arise

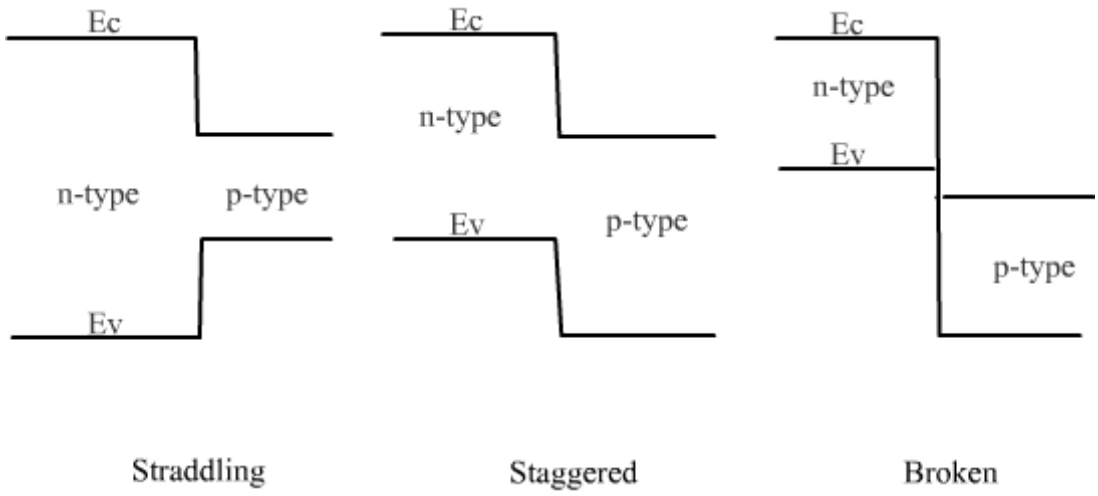

Figure 2.4: The there types of heterojunctions according to band gap alignment. Type 1 (Straddling), Type 2 (Staggered) and Type 3 (Broken)

as a result of different band gaps ($E_{g1,2}$), electron affinities ($\chi_{1,2}$) and work function ($\phi_{1,2}$) of two different semiconductors. The conduction band discontinuity and valance band discontinuity can be calculated by Anderson's Rule [40]. As can be seen in Fig.2.5 electron affinities difference of two semiconductors gives conduction band offset,

$$\Delta E_c = \chi_2 - \chi_1 \tag{2.12}$$

similarly, the valance band discontinuity is given by

$$\Delta E_v = (E_{g2} - E_{g1} - \Delta E_c) = (\Delta E_g - \Delta E_c) \tag{2.13}$$

Band offsets of the heterojunction creates extra barrier in the junction and this barrier increase recombination of the photogenerated charges. So to minimize the band offset effect on current flow in a heterojunction, ΔE_c has to be minimize by choosing closer electron affinity and band gap.

In literature, electron affinity and band gap of the $AgInSe_2$ is given as 4.15V and 1.35eV, respectively [41]. The electron affinity and band gap of the Si is given as 4.01V and 1.11eV, respectively [40, 42]. According to this information, calculated valance band and conduction band offset of n-Si/p-AIS is represented

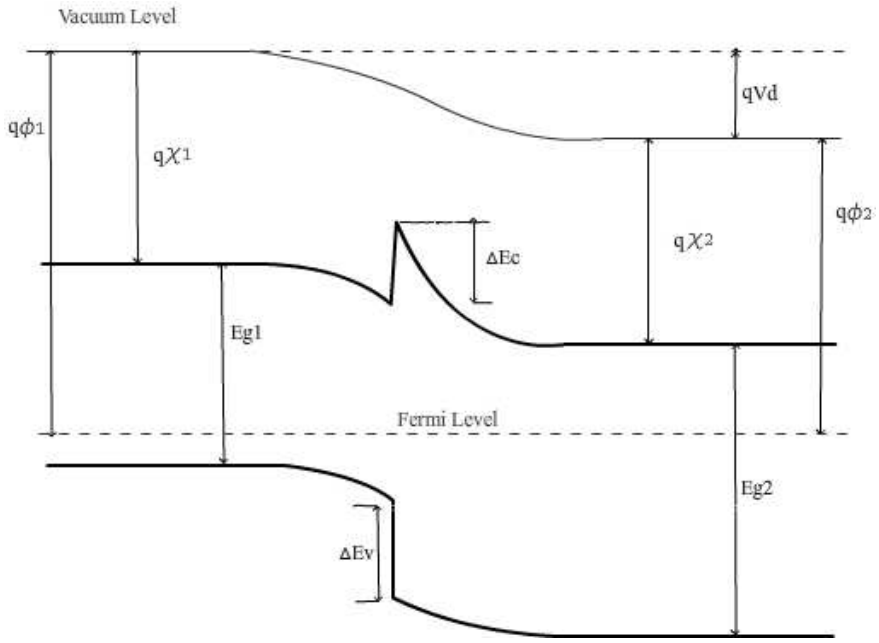

Figure 2.5: Energy band diagram of a heterojunction in thermal equilibrium.

in Fig. 2.6.

Behind the complex transport mechanism of heterojunction, there is also lattice mismatch problem in between two different semiconductors which resulting interface states in junction and acts as recombination centers and also enhance the tunneling current. This is a big problem especially solar cell application. However the advantages of heterojunction overcome these problems. Flexible band gap arrangement allows using high band gap optically transparent window layer. This reduce the recombination at the front contact by most of the carriers are generated in the absorber layer. Also this enhances the short wavelength spectral response and increase photogenerated current.

2.3.2 Solar Cells

2.3.2.1 Theory of Photovoltaic Process

The main process for photovoltaic is the generation of electron-hole pairs by the excitation of electron from valance band to conduction band when the energy of the incident photon greater than the band gap energy. In the p-n junction,

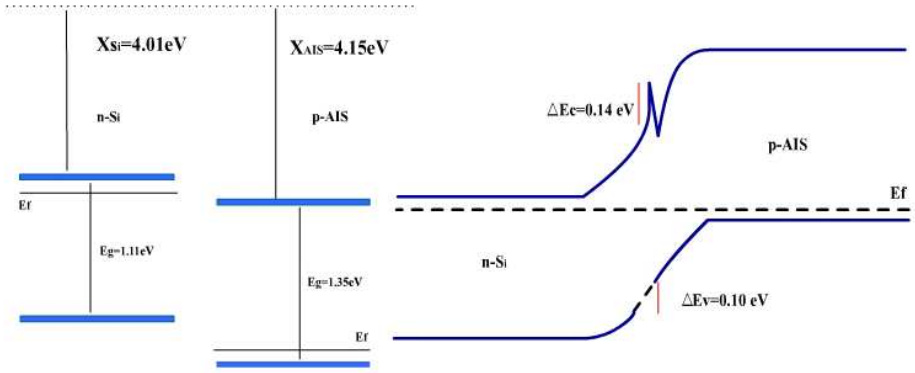

Figure 2.6: The valance band and conduction band offsets of Si/AIS heterojunction.

the photogenerated carriers diffuse the edge of the depletion region and internal electric field in junction separates the carriers before recombining. This results in the collection of the carriers at the contact and gives rise to photocurrent, photovoltage and power.

For the occurrence of photovoltaic effect firstly incoming photon energy has to be grater the band gap ($E_p = hc/\lambda > E_g$). Also, the life time of the carriers in structure must be large enough to reach electrical contacts. In order to get higher carrier lifetimes, the material has moderate doping and low defect densities. When a semiconductor illuminated only a fraction of light penetrates into material and passing light intensity decreases through the semiconductor by [40]

$$I(x) = I(x_0)e^{-\alpha x} \tag{2.14}$$

where I_0 is the intensity of light incident, x is the penetration depth and α is the absorption coefficient of absorbing material. α is important for solar cell design which gives the traveling length of light before it is absorbed and depends on the density of state and directness or indirectness of band gap. The optical absorbtion coefficient for direct gap semiconductors can be given by

$$\alpha = A^*(h\nu - E_g)^{1/2} \tag{2.15}$$

here A^* is a wavelength independent constant.

For a specific wavelength λ the generation of electron-hole pair at a distance x from the surface given by [40]

$$G(\lambda, x) = \alpha(\lambda)F(\lambda)[1 - R(\lambda)]e^{-\alpha(\lambda)x} \tag{2.16}$$

where $F(\lambda)$ is the number of incident photon per cm^2 per second per unit bandwidth, $\alpha(\lambda)$ is the absorbtion coefficient and $R(\lambda)$ is the number of reflected photon from surface. Spectral response photocurrent under low level injection conditions can be found by minority carrier continuity equations as,

$$(\frac{1}{q})(\frac{dJ_{n,p}}{dx}) + G_{n,p} - \frac{(n_p, p_n - n_{p0}, p_{n0})}{\tau_{n,p}} = 0 \tag{2.17}$$

for electrons in p type material and holes for n type materials respectively. The electron current density J_n and hole current density J_p given by

$$J_{n,p} = q\mu_{n,p}(n_p, p_n)E + qD_{n,p}(\frac{dn_p, dp_n}{dx}) \tag{2.18}$$

where E is electric field, p_n and n_p are photogenerated minority carrier densities and n_{p0} and p_{n0} are the equilibrium minority carrier densities in the dark. In depletion region internal electric field is high enough and the generated carriers should be accelerated out before they recombine. So photocurrent generated in depletion region is normally unaffected by recombination. Photocurrent per bandwidth is equal simply to the number of photon absorbed and given as [40]

$$J_{dr} = qF(\lambda)[1 - R(\lambda)]e^{-\alpha(\lambda)x_j}[1 - e^{-\alpha(\lambda)W}] \tag{2.19}$$

where x_j is the junction depth and W is the depletion layer width. The total photocurrent at a specific wavelength is the sum of the minority carrier currents and depletion region current

$$J(\lambda) = J_p(\lambda) + J_n(\lambda) + J_{dr}(\lambda) \tag{2.20}$$

The spectral response is the equal to Eqn.2.20 divided by the quantum efficiency for externally observed response for qF(1-R) for internally observed response.

$$SR(\lambda) = \frac{J_p(\lambda) + J_n(\lambda) + J_{dr}(\lambda)}{qF[1 - R(\lambda)]} \tag{2.21}$$

and photocurrent density is

$$J_L = q \int_0^{\lambda m} F(\lambda)[1 - R(\lambda)]SR(\lambda)d\lambda \tag{2.22}$$

where λ_m is the longest wavelength for the absorber band gap [40].

2.3.2.2 Current-Voltage Characteristics

Solar cells are p-n junction devices so their current-voltage behavior are similar to standard diode equation under dark and at ideal conditions (series resistance $R_s \to 0$ and shunt resistance $R_{sh} \to \infty$).

$$J = J_0\left(e^{\frac{qV}{nkT}} - 1\right) \tag{2.23}$$

total current density will be change under illumination by the amount of light generated current J_L

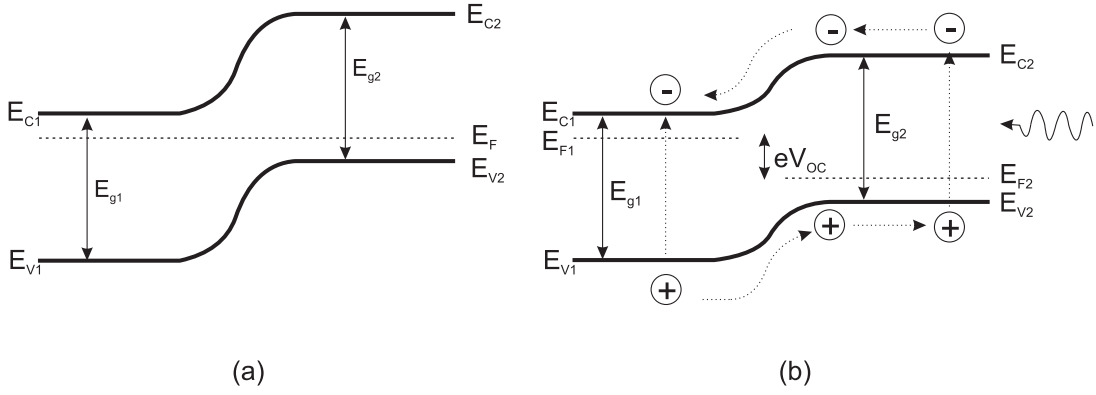

Figure 2.7: Energy band diagram of a typical p-n heterojunction solar cell (a) at thermal equilibrium in dark and (b) under illumination.

$$J = J_0\left(e^{\frac{qV}{nkT}} - 1\right) - J_L \tag{2.24}$$

here n is diode ideality factor which is a fitting parameters shows the diode behavior matching by theory. $n = 1$ corresponds the diode behavior exactly matching the theory and transport process is pure thermionic diffusion, $n = 2$ corresponds transports process is recombination in the space-charge region dominate other recombination. Greater value of ideality factor from 1 indicates different transport mechanism occurring in junction. It can be obtained by using the equation [43],

$$n = \frac{q}{kT}\frac{dV}{d(lnJ)} \tag{2.25}$$

from the slope and the intercept of the straight line region of the forward bias lnJ-V, the ideality factor n and saturation current density J_0 can be calculated by Eqn.2.25 and Eqn.2.23, respectively. Forward bias of a ideal diode and the deviation from theory can be seen in Fig.2.8. For high applied voltage regions, slope of the lnJ-V deviates from linearity because of the series resistance effect (R_s) and series resistance of junction can be calculated by this deviation.

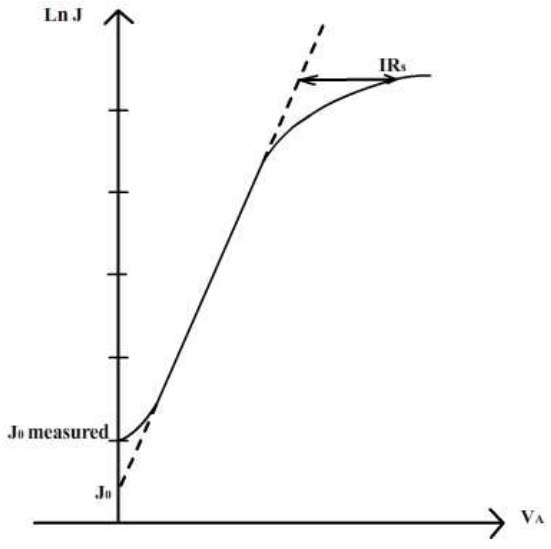

Figure 2.8: Forward bias and deviation from the ideal curve of lnJ-V plot.

2.3.2.3 Capacitance-Voltage Characteristics

When two semiconductors brought together, according the charge distribution, charges diffuse each side of the junction and a space charge region is created. The depletion width of a p-n junction can be described in terms of doping concentration and contact potential as;

$$W = \Big[(\frac{2\varepsilon V_0}{q})\Big(\frac{1}{N_a} + \frac{1}{N_d}\Big)\Big]^{1/2} \tag{2.26}$$

here q is the electron charge, N_a is the acceptor concentration in p type material and N_d is the donor concentration in n type semiconductor, $\varepsilon = \varepsilon_r \varepsilon_0$ where ε_r is the dielectric constant of semiconductor, ε_0 is the permittivity of free space. In the case of charge density in depletion region for uniformly distributed ionized acceptor, the depletion width can be expressed as [44];

$$W = \Big[(\frac{2\varepsilon}{qN_a})|V_{bi} - V_A|\Big]^{1/2} \tag{2.27}$$

where V_{bi} is the built in potential at zero bias and V_A is the applied voltage. According to Eqn.2.27 the width of the depletion region decreases with increasing forward bias voltage and increases with reverse bias voltage. For an abrupt junction depletion layer acts as insulating layer which is similar to parallel plate capacitor. The capacitance can be given as;

$$C = \frac{\varepsilon A}{x_n + x_p} = \frac{\varepsilon A}{W} \tag{2.28}$$

or in terms of total charge stored in junction

$$C = \frac{dQ}{dV} = \frac{d(qN_{ax})}{d(V_0 - V)} \tag{2.29}$$

and the depletion region charge per unit area can be given as

$$Q = \Big[2q\varepsilon_s N_a (V_{bi} - \frac{kT}{q})\Big]^{1/2} \tag{2.30}$$

than the capacitance is given by [45]

$$C = A\Big(\frac{q\varepsilon N_a}{2(V_{bi} + V_A - \frac{kT}{q})}\Big)^{1/2} \tag{2.31}$$

where A is the diode area, $\varepsilon = \varepsilon_r \varepsilon_0$ is the permittivity of the semiconductor and V_A is the applied voltage. In generally the plot of C^{-2} *vs* V_A should be a straight line. Then, the slope of this line gives the doping density ($N_{a,d}$) and the intercept gives the built in voltage ($V_0 = (V_{bi} - kT/q)$) in junction. The capacitance voltage analysis of a device has a resolution equal to Debye length (L_D) which is given by

$$L_D = (\frac{\varepsilon \varepsilon_0 kT}{q^2 N})^{1/2} \tag{2.32}$$

The capacitance voltage behavior in heterostructure devices similar to p-n junction with the modification of abrupt junction approximation. In a hetero-junction electron per unit area in p type semiconductor side must be equal to holes per unit area in n type semiconductor side with the relation,

$$N_d X_n = N_a X_p \tag{2.33}$$

Applying Poisson's equation with the assumption of abrupt junction and doping is uniform in both materials the capacitance-voltage function given by

$$\frac{C}{A} = \Big[\frac{qN_{d1}N_{a2}\varepsilon_1\varepsilon_2}{2(\varepsilon_1 N_{d1} + \varepsilon_2 N_{a2})(V_{bi} - V_A)}\Big]^{1/2} \tag{2.34}$$

This equation shows that C^{-2} is linear as a function of applied voltage V_A. From the slope of $C^{-2} - V_A$ plot, one can obtain carrier concentration (N_d) and from the intercept value, built in potential (V_{bi}) can be calculated. So if one of the material carrier concentration is known, the other material carrier concentration can be calculated.

$$dC^{-2}/dV_A = 2(\varepsilon_1 N_{d1} + \varepsilon_2 N_{a2})/(a^2 q N_{d1} N_{a2} \varepsilon_1 \varepsilon_2) \tag{2.35}$$

Frequency dependent capacitance voltage measurement also useful method for obtaining interface properties of junctions. At sufficiently high frequencies interface states can not follow the a.c. signal, surface states capacitance (C_{ss}) becomes inactive and only space charge capacitance (C_{sc}) play main role which results in decrease in the junction capacitance value. Total capacitance is the

sum of the space charge capacitance and surface states capacitance. At low frequencies C_{ss} becomes dominant and interface states density can be given by [46]

$$N_{ss} = C_{ss}/qA \tag{2.36}$$

where A is the diode area and C_{ss} surface states capacitance value which can be determined from vertical axis intercept of capacitance-frequency plots.

A p-n junction or Schottky diode consist of junction capacitance, conductance and series resistance (R_s) which depends on bulk resistivity and contact resistance [43]. The series resistance R_s of the device structure can also be determined by capacitance (C_m) and conductance (G_m) measurements at high frequencies and strong accumulation region [47]. The series resistance can be determined by [43]

$$R_s = \frac{G_m}{G_m^2 + \omega^2 C_m^2} \tag{2.37}$$

2.3.2.4 Solar Cell Parameters

There are three major electrical parameters for solar cell devices; the open circuit voltage (V_{oc}), short circuit current density (J_{sc}) and the fill factor (FF). The power output (P_{out}) and the efficiency (η) of the solar cell can be derived by this parameters. An ideal current-voltage characteristic of a solar cell under dark and illumination is given in Fig.2.9. As can be seen the dark J-V curve is shifted by the amount of the photocurrent density J_L

When the junction is connected to a zero resistance external circuit under illumination, the current flows through the junction is called short circuit current. Ideally short circuit current is equal to the light generated current at zero bias and can be altered by spectral properties of light, the absorbtion properties of material and the diffusion length of the minority carriers.

The potential difference between front and back contact is defined as open circuit voltage (V_{oc}) under illumination and is given by [48]

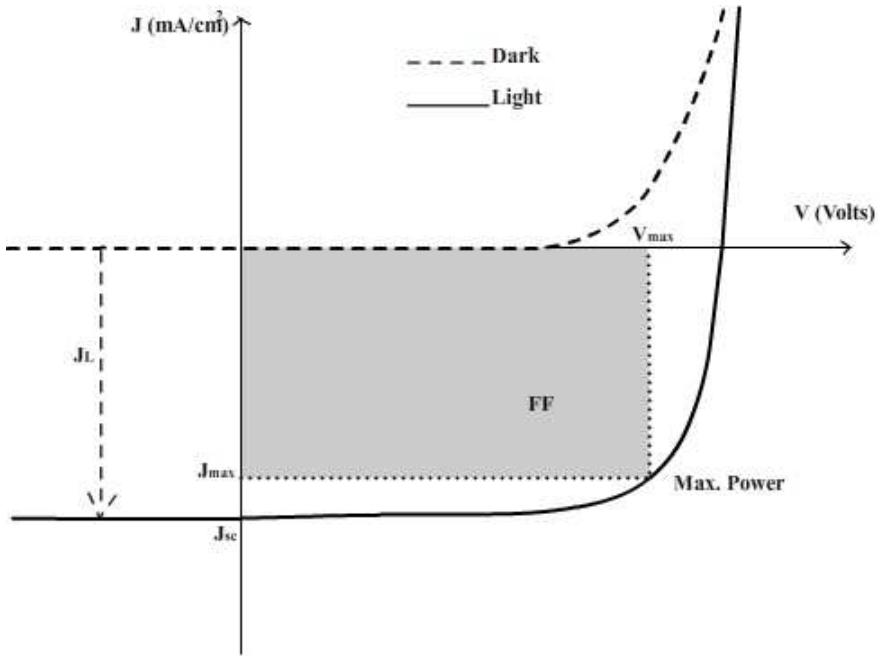

Figure 2.9: Current-Voltage characteristics of an ideal solar cell under dark and illumination.

$$V_{oc} = \frac{nkT}{q} Ln\Big(\frac{J_{sc}}{J_0} + 1\Big) \tag{2.38}$$

The maximum power point of a solar cell is the point that maximizes JV and can be found by the condition $\frac{\partial P}{\partial V} = 0$. As can be seen in Fig.2.9 the maximum power output of an ideal solar cell is found by the product of maximum voltage and maximum current density $P_m = J_m V_m$.

The fill factor (FF) is a squareness of the current density-voltage curve under illumination and shows the quality of the solar cell. FF can be found by

$$FF = \frac{P_{max}}{V_{oc} J_{sc}} = \frac{V_m J_m}{V_{oc} J_{sc}} \tag{2.39}$$

The efficiency η or the energy conversion ability of a solar cell is the ratio of the maximum power output of solar cell to the power incident due to solar irradiation and given by

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_m J_m}{P_{in}} = \frac{V_{oc} J_{sc} FF}{P_{in}} \tag{2.40}$$

Table 2.2: Ideal solar cell performance parameters.

Parameters	Symbol	Unit	Determination
Open circuit voltage	V_{oc}	V	J=0
Short circuit current density	J_{sc}	$mA\ cm^{-2}$	V=0
max-power voltage	V_m	V	V at $(P = JV)_{max}$
max-power current density	J_m	$mA\ cm^{-2}$	J at $(P = JV)_{max}$
Fill factor	FF	%	$(JV)_{max}/(V_{oc}J_{sc})$
Efficiency	η	%	$(JV)_{max}/P_{in}$

The above parameters are defined for an ideal solar cell ($J_L \simeq J_{sc}$) and ideally the current voltage curve of a solar cell is given by

$$J(V) = J_0\Big(e^{(\frac{qV}{kT})} - 1\Big) - J_L \tag{2.41}$$

However in real application this equation has to be modified for parasitic losses as,

$$J(V) = J_0\Big(e^{(\frac{q(V-RsJ)}{nkT})} - 1\Big) + \frac{V - R_sJ}{R_{sh}} - J_L \tag{2.42}$$

As can be seen in Eqn.2.42 series resistance R_s, shunt resistance R_{sh} and diode ideality factor n define these parasitic effects. Some parasitic effects on current-voltage plot of solar cell under illumination can be seen in Fig.2.10 [49,50]. Ideal solar cell parameters are given in Table 2.2 [51].

2.3.2.5 Efficiency Losses in Solar Cells

In real solar cells, deviation from the ideal case can be the result of various loss mechanisms. The main reason for the low efficiency is that the incoming light has various energetic photons. If they have lower energy than the band gap of material, electron hole pair couldn't be created. The higher energetic photons than band gap also lost in the form of heat. Reflection or transmission of light without generating any electron hole pair has 70% of energy loss in solar cell operation. The small band gap material absorbs more photons according to higher band gap material and generates higher current but in the same time

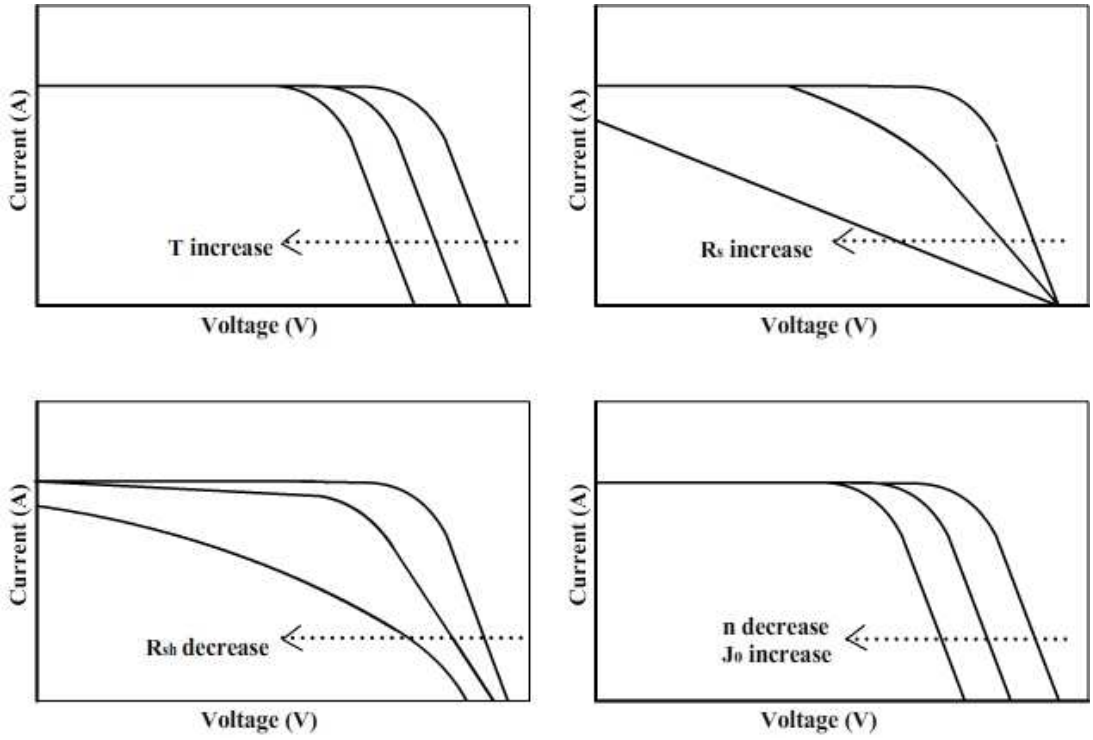

Figure 2.10: Effect of temperature, series resistance, shunt resistance, saturation current and ideality factor parameters on solar cell current-voltage curve under illumination.

half of the band gap value of materials determines the open circuit voltage (V_{oc}) parameters for solar cells.

Series resistance which arises from the bulk resistance and the contact resistance is another cause of energy loss by increasing recombination process. Shunt resistance represent the leakage across the junction and around the cell edge and for lower shunt resistance created electron hole pairs easily recombine by leakage and could not reach the contact by resulting reduction in efficiency.

Therefore, to increase the solar cell efficiency the band gap of absorbing material must be optimum value to absorbe the wide range of incoming photons and at the same time the band gap must be small to minimize saturation current. Also diffusion length of the minority carriers must be as large as possible to reach contact without recombining.

CHAPTER 3

EXPERIMENTAL TECHNIQUES

3.1 Introduction

In this chapter, experimental techniques used for the deposition procedure, post-depositional heat treatment and the characterization techniques of Ag-In-Se (AIS) thin films and devices are presented. It gives short information about the physical nature of the methods and techniques which were utilized during the production, physical improvement and characterization of the thin films and devices.

3.2 The Preparation of Ag-In-Se Thin Films and Devices

In order to study the film and device properties, Ag-In-Se thin films were deposited by thermal evaporation and three magnetron RF and DC Sputtering techniques onto soda lime glass, Indium-tin-oxide coated glass substrates and p and n-type Silicon wafers using the copper masks as shown in Fig.3.1a.

The masks used for the metallic contact deposition for the point contact geometries are shown in Fig.3.1b. Before the deposition process, glass, ITO coated glass and Si wafers substrates should be cleaned in order to get rid of dirtiness between the film and the substrate.

Cleaning of the soda lime glass substrates is an important step before thin film deposition process. The contaminants on the substrates would possibly

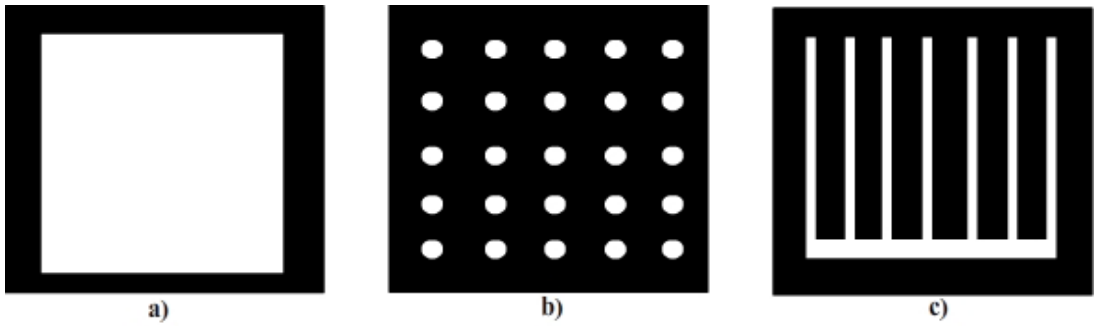

Figure 3.1: Shadow mask shapes for (a) thin film production $2 \times 2cm^2$ square geometry, (b) metal contacts in 1mm diameter and (c) Metallic fringes.

interfere with thin film growth mechanism which results in undesirable thin film properties and instabilities in the structure [52].

The cleaning process of the glass, ITO coated glass and Si wafer substrates include the steps as follows;

- The glass pieces are first sinked in a dilute solution of chemical detergent prepared from highly pure water to dissolve the unwanted contaminants like organic molecules from the surface at a temperature of about 100^oC.
- Then, the solution containing substrate pieces is put into ultrasonic cleaner to increase the effectiveness of solvent cleaning.
- The glass pieces are rinsed in hot pure deionized water in order to remove the layer of residue on the surface due to detergent solution.
- The glass pieces are immersed in a boiling diluted H_2O_2 solution to remove organic contaminants from glass surface by dissolving them.
- Then, H_2O_2 solution containing the glass pieces is put into ultrasonic cleaner to increase the effectiveness of the process.
- Same procedure repeated for Acetone solution.

After completing the cleaning process, the clean glass substrates and ITO coated glass substrates are placed in pure methanol and kept in it till thin film

deposition process starts. The glass substrates are removed from methanol and dried by blowing nitrogen gas upon them before placing them into holder before thin film deposition. Prior to thin film deposition, back surface of p-Si wafer was coated with aluminum (Al) by thermal evaporation and DC sputtering techniques, which serves as the back ohmic contact and front surface was subjected to the cleaning procedure with $HF : H_2O = 1 : 10$ solution in order to remove the native oxide layer and then rinsed in deionized water consecutively blown dry in N_2. To check the cleanliness of the substrates, wettability test was applied to substrates to observe the surfaces were free of any dirty spots.

3.3 The Evaporation Cycle

The determination of appropriate deposition technique is directly assigned by the aimed deposited thin film properties, the application of the film, the temperature optimization of both source and substrate materials, the issues of compositional and thickness uniformity, the deposition rate and the commercial costs. Therefore, the desired composition and microstructure of thin films can be achieved by choosing a suitable deposition technique [19].

Today, most of the practical thin film deposition processes requires a vacuum environment and the physical vapor deposition (PVD) technique is one of the oldest and widely used thin film deposition process in a vacuum chamber. The essence of thin film deposition mechanism for PVD encloses the making a source material evaporate or sublime through heating under vacuum, then the condensation of the evaporated molecules onto a substrate surface to produce a film. According to types of evaporation mechanisms used to evaporate source material in PVD systems. Some of the PVD techniques are

- Thermal evaporation, in which source material in a quartz tube is heated by wounded heating coil around the quartz source tube in low vacuum.
- Electron beam evaporation, in which source material is heated by means of an electron bombardment in high vacuum,

- Sputtering, in which source material which located near a magnet is evaporated by glow plasma discharge bombards the material sputtering away as a vapor.

- Pulsed laser deposition, in which a high power laser remove material through evaporation from the target into a vapor.

In this thesis thermal evaporation and three magnetron RF+DC sputtering method were used and explanations of these methods are given in following sections briefly.

3.3.1 Thermal Evaporation System

The deposition of Ag-In-Se thin films by using thermal evaporation method carried out in a Leybold Univex 300 vacuum system which has the lowest pressure value around $10^{-6} Torr$. The lowest vacuum was reached by a complete turbomolecular pumping system and the vacuum value is read by pirani and penning vacuum gauges. The schematic diagram of the evaporation system is given in Fig.3.2.

Source unit is a quartz ampoule in which the source material was heated, wrap with molybdenum wire all of which was placed into a ceramic shielder in order to stabilize the source temperature. The source was heated by controlling the current passing through the molybdenum wire with the source power unit of the Leybold Univex 300 system. The source temperature during the growth process was measured with Pt/Pt-13 % Rh thermocouple placed within the quartz ampoule and holder, and controlled by Elimko-4000 temperature controller.

The substrate heater was made of an aluminum block with chrome-nickel heating wires which was insulated by quartz tubes. The substrates with masks were placed in the substrate holder which was mounted about 15 cm above the source. The substrate temperature was measured with a copper-constantan thermocouple which is in contact with the holder. Fluke temperature controller was used to monitor the temperature of the substrates. The shutter was placed just

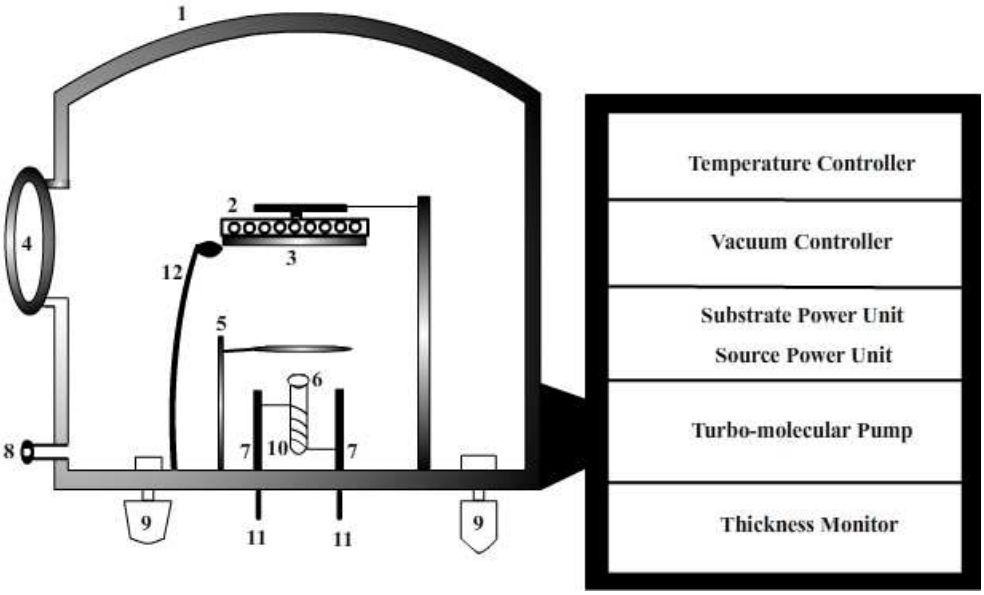

Figure 3.2: The vacuum evaporation system for Ag-In-Se thin film deposition. 1. Bell-jar, 2. Substrate heater, 3. Substrate holder, 4. Window, 5. Shutter, 6. Source boat, 7. Feedthroughs, 8. Air valve, 9. Pirani and Penning gauges, 10. Source heater, 11. Filament current wires, 12. Thickness monitor probe.

above the source for controlling the start and the stop of the thermal deposition process.

$AgIn_5Se_8$ thin films were deposited by thermal evaporation method using $AgIn_5Se_8$ single crystal powder, which were grown by Bridgman-Stockbarger technique as the evaporation source material onto p-type Si(111) wafers with resistivity value of 10.5-19.5 $(\Omega - cm)$ and glass substrates under high vacuum of about $1.33x10^{-4}Pa$ at the substrate temperature of around $T_s = 423K$. The deposition time controlled by the shutter and the growth rate of the sample was measured as 30nm/minute by Inficon XTM/2 thickness monitor during growth process.

3.3.2 Three Magnetron RF/DC Sputtering System

Sputtering is a growth method whereby atoms are ejected from a target material by bombardment with energetic particles or ions which can be supplied from plasma, an ion source, an accelerator etc. [53]. It is generally used for thin-

film deposition or etching. The processing plasma is a pair of sheaths and a uniform plasma between these sheaths. In sputtering systems generally Direct current (DC) or Radio frequency (RF) plasmas are used for metals and insulating materials respectively. DC plasma consists of anode and cathode sheaths and require secondary electron emission with enough energy to reach other sheath. In magnetron sputtering, the magnetic field improves the plasma by generating an electron trajectory in the form of a helix which allowing shorter target-substrate distance and provide the required collision in short distances [54, 55]. In RF sputtering, a radio frequency alternating current is applied to a metal backing electrode and induced on the surface of a target. Because of the electric field between the target and substrate a plasma is created on the target surface. In the positive cycle negative particles and in the negative cycle positive particles are attracted to target and energetic particles bombard the target and sputtering occurs [56].

To create a plasma around target an inert gas generally Argon (Ar) is flown through vacuum chamber. The chamber pressure is kept in the mili-Torr range so plasma can start and also sputtered atoms can reach the substrate with a large mean free path. When an ion impact on a target surface, according to it's energy, four possible outcome occurs; ion bounce back from surface, sputter off an atom, adsorb to the surface or implanted in deeper side of target material.

In this thesis Vaksis three magnetron DC/RF sputtering method was used. The Vaksis Sputtering system's component can be seen in Fig. 3.3. The system has one RF and two DC magnetron heads which are cooling by water circulation. Chamber pressure can be reach up to 10^{-8} Torr and plasma vacuum kept at $3 \times 10^{-5} Torr$ when growth process by adjusting Ar flow and vacuum valve. Substrate can be heated by halogen lamps where under and on the substrate holder up to 600^{o}C. For generating RF plasma Fokus 600W RF Generator and a Dressler VM100A Match-box was used. For DC plasma An Advanced Energy MDX500 power supply was used.

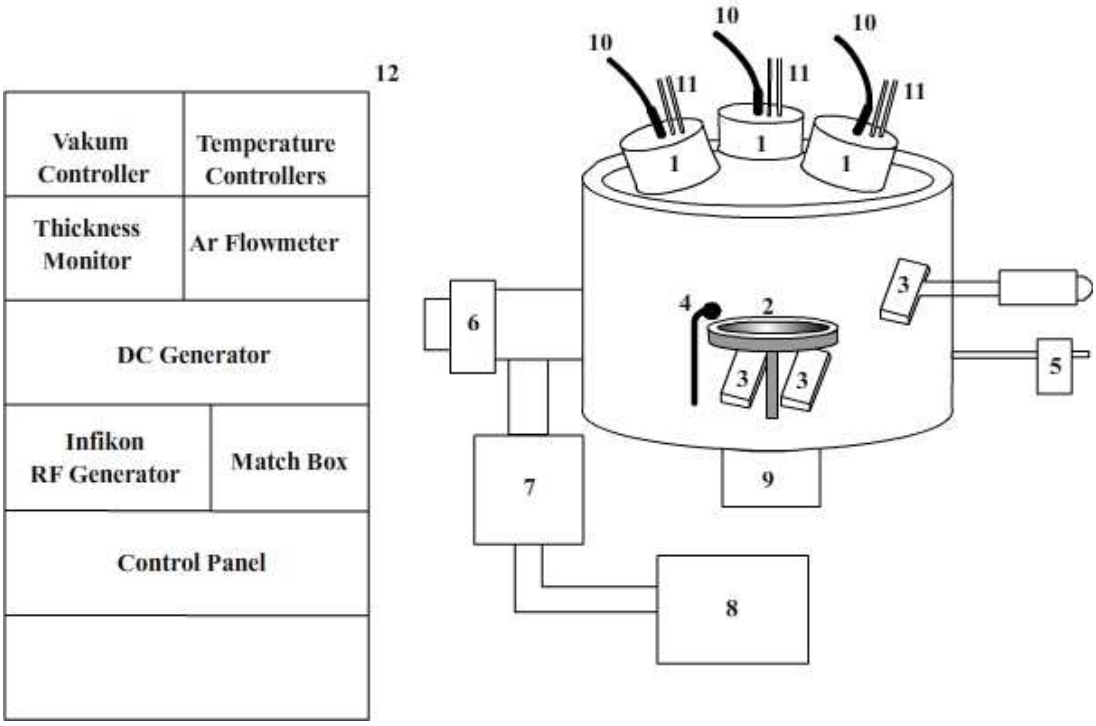

Figure 3.3: Schematic view of three magnetron sputtering system. 1. Magnetron Heads, 2. Substrate Holder, 3. Halogen Lamp Heaters , 4. Thickness Monitor Probe, 5. Ar Flow Controller 6. Vacuum Valve 7. Turbo-molecular Pomp 8. Rough Pomp 9. Adjustable Substrate Rotator 10. RF/DC-Magnetron Wires 11. Water Cooling Pipes 12. System Control Unit.

3.3.3 The Metallic Evaporation System

The metallic evaporation system was used for electrical ohmic contacts. Indium ohmic contacts were evaporated on to Ag-In-Se thin films with dot and strip shape as can be seen in Fig.3.1 to carry out the electrical and optical measurements. For the solar cells, In and Al metals were achieved onto the back of Si wafers and front of Ag-In-Se contact, in order to investigate the device properties of the Si/Ag-In-Se junctions. The metallic evaporations were carried out by using a Nanotech evaporator system, schematic view of the system is shown in Fig.3.4. The lowest attainable pressure with this system is 10^{-6} Torr through a diffusion pump. For the metallic evaporation, the source metal was placed in a molybdenum boat which was heated by a manually controlled variac. The substrates and the appropriate masks were placed in a copper holder that was

mounted around 12 cm above the source boat.

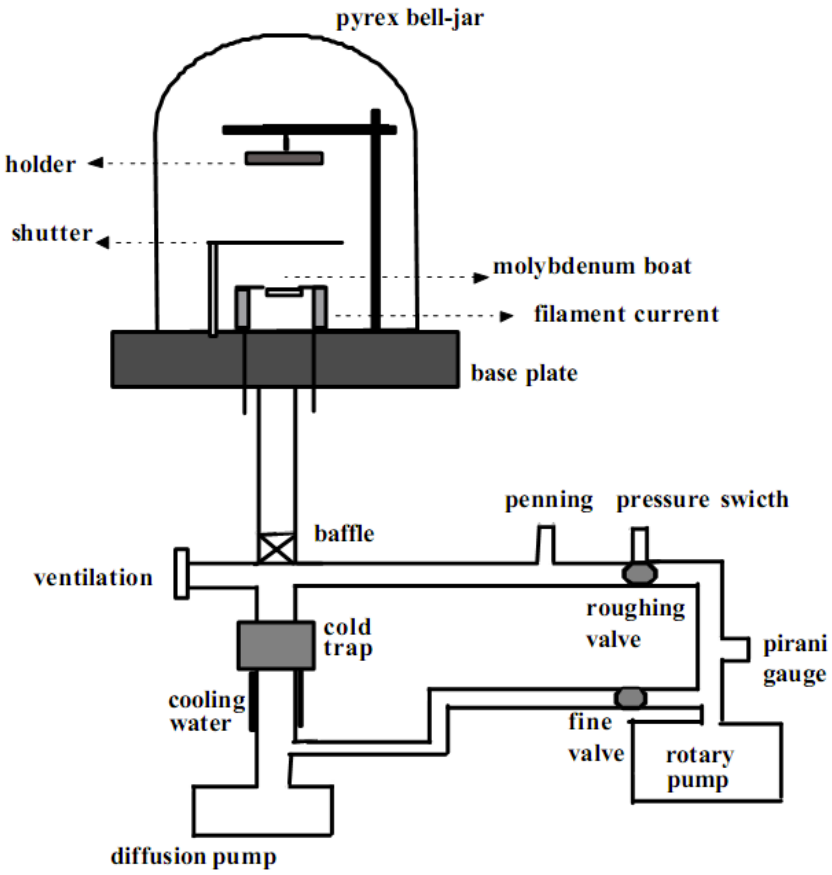

Figure 3.4: The schematic view of metallic evaporation system.

3.4 Post-Annealing Process

Post-annealing process is used technique to revise the physical and/or chemical properties of deposited thin films and eliminate the surface contact adhesion problems . Deposited thin films and metallic contacted films are placed in an isolated furnace in which an inert gas environment is maintained, and heated gradually up to a desirable temperature by a variac as the schematic illustration of such an annealing system is shown in Fig.3.5. The desired temperature value

is maintained for thirty minutes time period and then the system is allowed to cool down to the room temperature slowly.

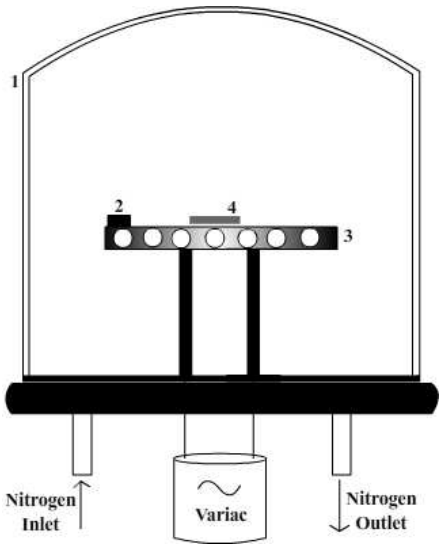

Figure 3.5: Schematic view of post annealing process for AIS thin films and metallic contacts. 1. pyrex glass jar, 2. thermocouple, 3. hot plate and 4. sample.

In this work, after thermal deposition of AIS thin films, annealing process in an inert nitrogen gas ambient was applied at different fixed temperature values changing from 160 to 280°C for a limited time interval of 30 minutes. Also metallic dot contact and metallic strip contact evaporated AIS films were annealed at 100 °C for 30 minutes to increase the ohmicity of the contacts. During the process, a continuous flow of nitrogen gas was maintained to the system to prevent the contamination caused by atmosphere.

The AIS thin films which were deposited by RF/DC sputtering method also annealed in Leybold Univex 300 vacuum system which is shown in Fig. 3.2. InSe target was sputtered by RF method and Ag target was sputtered by DC method layer by layer alternately. After deposition of as grown, AIS films were annealed at 300 °C under Selenium atmosphere for 30 minutes time interval. This process called selenization or two stage process.

3.5 Structural Characterization of Thin Films

3.5.1 Thickness Measurements

Thickness value of thin films has a critical effect on the characteristics of the films and is used in many characterization methods. So, exact determination of thin film thickness is an important and essential task for many optical and electrical measurements and data analysis. There exists a variety of thickness measurement techniques but in this thesis in-contact measuring technique was used by Veeco DEKTAK 6M profilometer. In the contact measuring technique, step height of deposited thin films, which is defined between substrate and thin film surface, is measured by the movement of a stylus over substrate and thin film surface as can be seen in Fig. 3.6. The force applied (1-50 mg) by the stylus on surfaces can be manipulated to obtain optimum thickness measurements which depend critically on hardness and the surface properties of thin film [19].

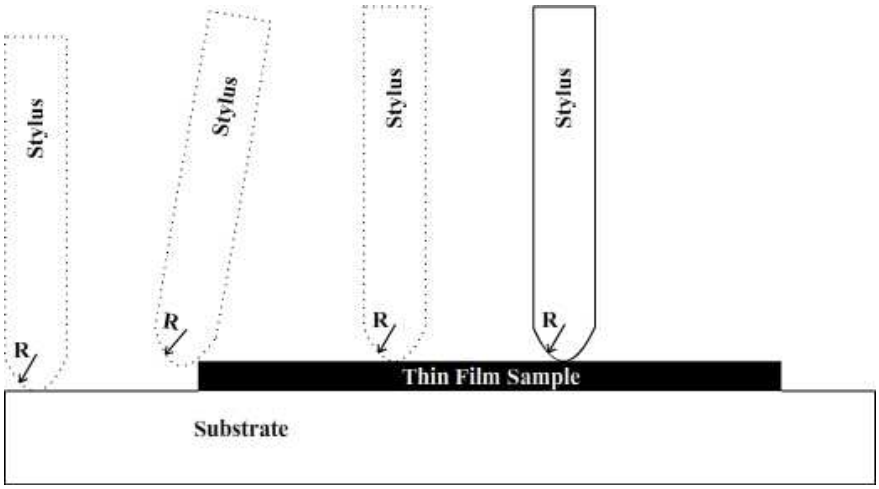

Figure 3.6: Thin film thickness measurement by means of a diamond stylus of Veeco DEKTAK 6M profilometer. R is the radius of curvature of the stylus head, which is 12.5 μm in our measurements, dotted plots show the motion of the stylus during measurement.

3.5.2 X-ray Diffraction (XRD)

X-ray diffraction (XRD) method is one of the main tools for the structural characterization of materials. The structural properties and crystallinity of the AIS films were determined by XRD analysis. Each crystalline solid material has its unique characteristic X-ray pattern which can be used as a distinguishing property of material. The diffraction pattern is used to determine structure, phase composition and purity properties of the material. The diffraction data is compared with the known diffraction patterns recorded in the International Centre for Diffraction Data (ICDD) database in order to match the measured data to get information about analyzed material.

In this work the XRD measurements for AIS thin films were carried out by using a Rigaku Miniflex XRD system equipped with Cu Kα radiation of average wavelength of 1.54059 Å. All XRD measurements were performed by using same parameters which are 2θ values were between 5 and 90^o and scan speed=2^o/minute. The XRD patterns were analyzed with a computer software and the ICDD database. The peak search and matching analysis were carried out based on the diffraction angle (2θ) values and relative intensities of the diffraction peaks [19].

3.6 Electrical Measurements

3.6.1 Current-Voltage Measurements

Al/Si/AIS/In heterostructures were fabricated by growth of AIS films with thermal evaporation and RF/DC sputtering techniques as explained in evaporation cycle section. After deposition of the AIS films annealing (or annealing+selenization) process was applied on the films. Al back and In front contacts were grown by metallic thermal evaporation or DC sputtering techniques. The contact area of metal contact is $7.85 \times 10^{-3} cm^2$. The metallic grid shape In contacts were also deposited on the front side of the junctions as thin as possible to prevent the shadow effect on solar cell characteristic of devices. Metallic contacts

following to the deposition were annealed at 100 °C for 30 minutes to provide good ohmicity. For connecting the metallic front dot contacts, front fringe contacts and back contacts to measurement devices, Cu wires were attached to In contacts with Ag paste.

In order to understand the rectifying behaviors of the devices dark current-voltage (I-V) characteristic was measured at room temperature and in the temperature range of 160-360K. A constant current was applied between front and back contact of the devices and voltage drop was measured with Keithley 2400 source-meter which is controlled by a Labview PC program in the current range of 1×10^{-9}-1×10^{-1}A. Dark current-voltage measurements were carried out in a shielded dark four probe-box to avoid undesired external field and illumination effects on the sample. Type of the AIS films were investigated by hot probe method.

In order to get temperature dependencies of all temperature dependent current-voltage and optical measurements, the deposited AIS thin film samples were mounted onto a cold head part of a Janis Liquid Nitrogen VPF series cryostat as can be seen in Fig. 3.7 and all measurements were performed under a vacuum condition at about 1.33 x 10^{-1} Pa was attained inside the cryostat system in order to prevent the effect of environment. Temperature dependent measurements were carried out between temperature values of 160 and 360 K with 20 K increments. The vacuum environment within cryostat system was maintained by an Ulvac Rotary pump and the cold head temperature could be cold down around 77 K by liquid nitrogen. The temperature of the thin film samples were measured by a GaAlAs diode sensor attached to the cold head and monitored by a LakeShore 331 temperature controller having computer control to manipulate the temperature of the samples inside the cryostat. All electrical connections were made by an electrical feedthrough mounted on the sample holder.

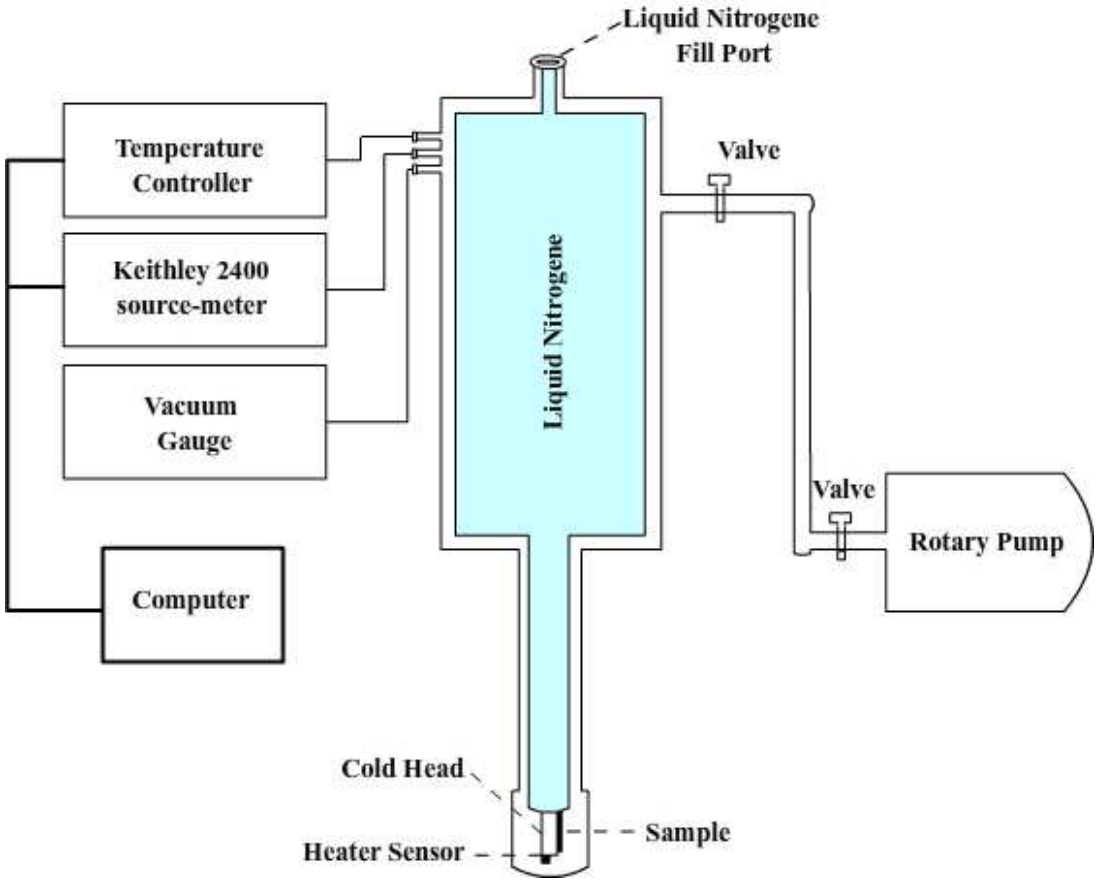

Figure 3.7: The schematic diagram of the Janis liquid nitrogen, sample-in-vacuum type cryostat.

3.6.2 Capacitance-Voltage Measurements

The frequency dependent capacitance-voltage (C-V) measurement has been used as a useful tool to define the junction region structure, some effects due to interface states or deep trap levels. The reverse bias side of the capacitance-voltage measurements gives information about built in potential (V_{bi}) of the junction and effective carrier concentration of the materials. The capacitance-voltage measurements (C-V) with conductance-voltage (G-V) measurements at high frequencies and high forward bias region give the series resistance of the structure. In this study, frequency dependent C-V and G-V measurements were carried out by using HP 4192A LF Impedance Analyzer controlled by a computer with a Labview program. The diagram of the experimental set up for C-V/G-V measurements

is shown in Fig. 3.8.

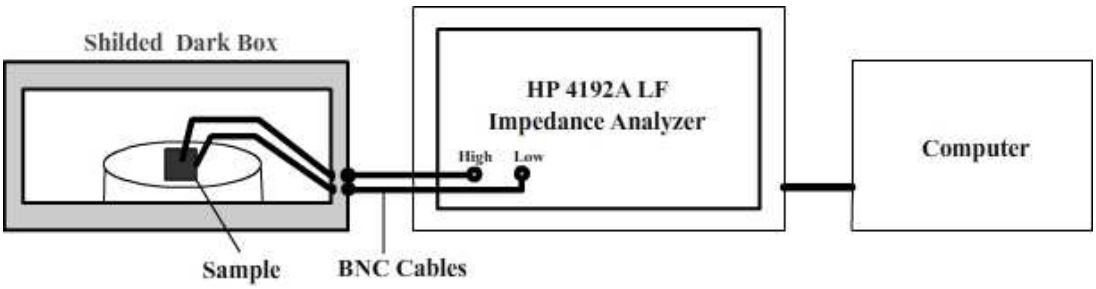

Figure 3.8: The experimental setup of the frequency dependent capacitance-voltage/conductance-voltage measurement system.

The C-V measurement device uses a linear voltage ramp to sweep the voltage over the bias range from accumulation to inversion or vice versa at a described bias ramp rate. A small ac voltage is combined on the ramp voltage to measure the differential capacitance change in the depletion region. The sweep capability of the built-in frequency synthesizer and dc bias source allows quick and precise measurements. The built-in frequency synthesizer can be set to measuring frequency within the range from 5Hz-13 MHz. Oscillation level of the ac voltage can be altered from 5 mV to 1.1 Vrms and it can be swept in 1mV increments. The internal dc bias voltage source can provide 35 V in 10 mV increments. The measuring frequency or dc bias voltage can be adjustable in either direction [57]. The C-V/G-V measurements Si/AIS heterojunction devices were carried out within the frequency range of 1 kHz -10 MHz. The amplitude of the dc ramp was changed from -2 to 1.5 V with 0.05 V increments and the oscillation level of the ac voltage was set to 0.05 V.

3.6.3 Spectral Photoresponse Measurements

The spectral photoresponse measurements are based on measuring the photocurrent as a function of the illumination wavelength. Spectral response measurement is the most direct method for determining the band gaps of the semiconductors

in a junction.

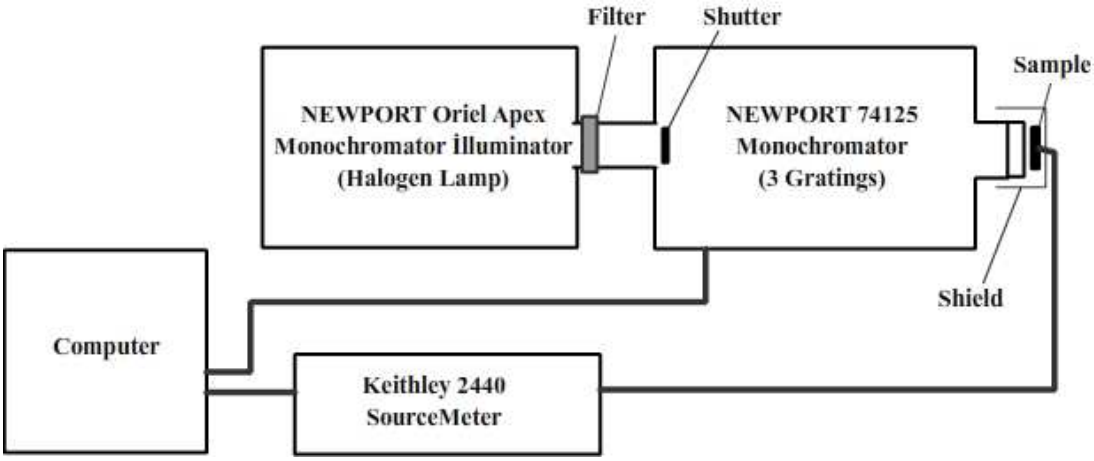

Figure 3.9: The schematic diagram of the experimental setup for the spectral photoresponse measurements of AIS thin films. SourceMeter and monochromator are controlled by a Labview computer program.

The photoresponse measurements of the Si/AIS heterojunctions were carried out at room temperature and in the temperature range of 100 and 450 K. For temperature dependent spectral response measurements, the Janis cryostat was inserted the output of the monochromator. The radiated light generated by Newport Oriel Apex Monochromator Illuminator with a halogen lamp light source and 4 optional filter. The beam of light was directed into a Newport Oriel 74125 Monochromator equipped with 3 diffraction gratings with 600 lines/mm whose ranges are 250-1300nm/600-2500nm/900-2500nm, respectively. The resulting monochromatic light having a wavelength between the range of 400 and 1300nm was projected on the Si/AIS heterojunctions through the quartz optical window of the cryostat.

The schematic diagram for the measurement setup is given in Fig. 3.9. The application of bias voltage and the measurement of photocurrent were performed by a HP 4140 picoammeter/DC voltage source or Keithley 2440 SourceMeter. The illumination time, appropriate grating, wavelength were adjusted by means of a computer software written in Labview language. The obtained photoresponse

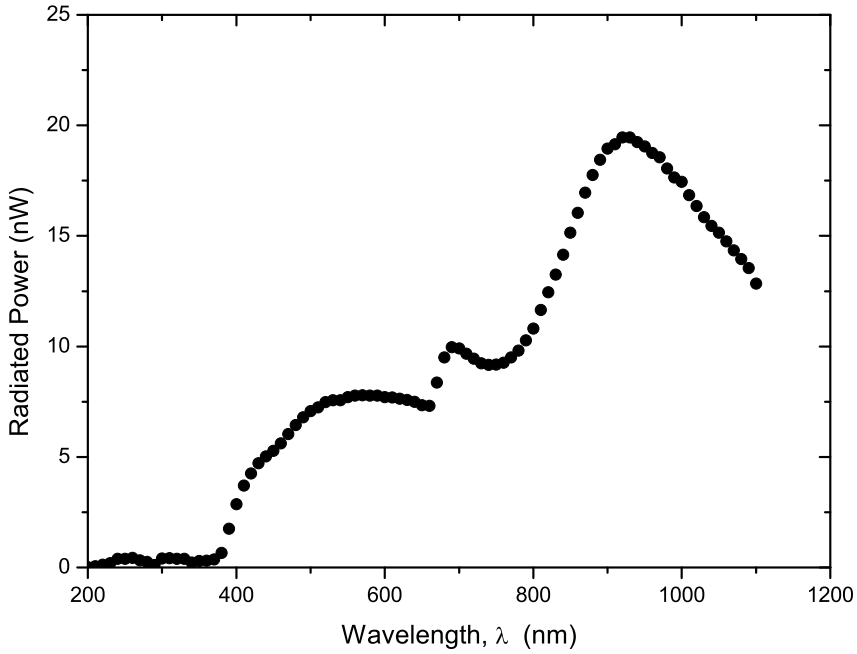

Figure 3.10: The power spectrum of the light outgoing through monochromator output.

spectra was corrected for the spectral distribution of the illumination light. The power spectrum of the light radiated by the Newport Oriel Apex Monochromator Illuminator halogen lamp was obtained by means of a Newport powermeter as given in Fig. 3.10 [19].

3.6.4 Solar Cell Measurements

Current-voltage measurement of the heterojunction devices under solar simulated illumination were measured by using an Oriel 1000W Solar Simulator which has very high intensity Xenon Arc Lamp shown in Fig. 3.11. The simulator has 4×4 inches highly collimated beam area whose spectrum is close to Air Mass 1 (AM1) condition with an AM1 filter.

Air mass (AM) is the optical path length through Earth's atmosphere for light from sun and shown in Fig. 3.12. The power distribution per wavelength

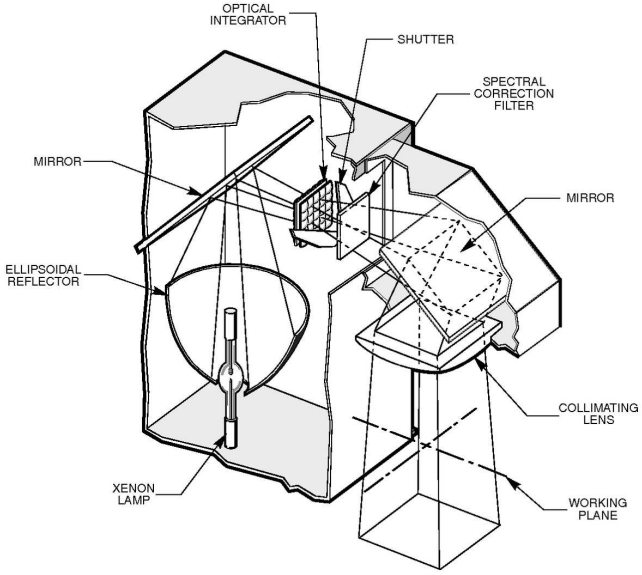

Figure 3.11: The schematic diagram of the solar simulator.

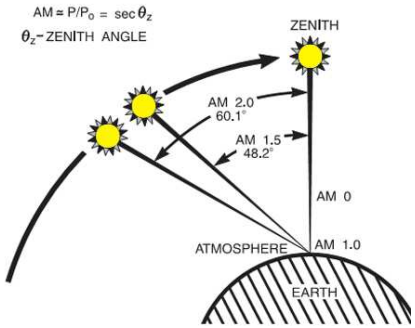

Figure 3.12: The path length of light (Air Mass).

and the spectrum of incident light is changed by the O_3, O_2 and H_2O molecules in the atmosphere, and this changed spectrum is shown in Fig.3.13. In order to reach the AM1 illumination conditions, an AM1 filter is inserted to output of the solar simulator and the output power of filtered light was measured by an 2×2 inches Newport PVIV201 Reference Cell before all solar simulator measurements.

Solar simulated current-voltage measurement workstation is shown in Fig. 3.14. The solar simulator shutter and current-voltage source-meter is controlled by a computer with Newport I-V Test Situation software. All the data i.e.current-

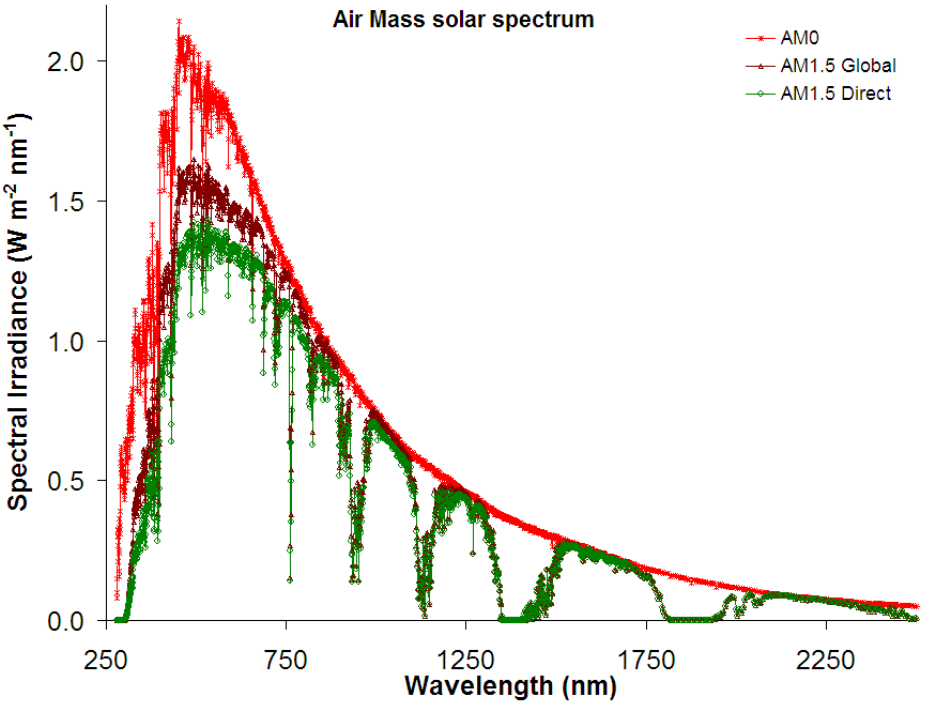

Figure 3.13: The air mass solar spectrum.

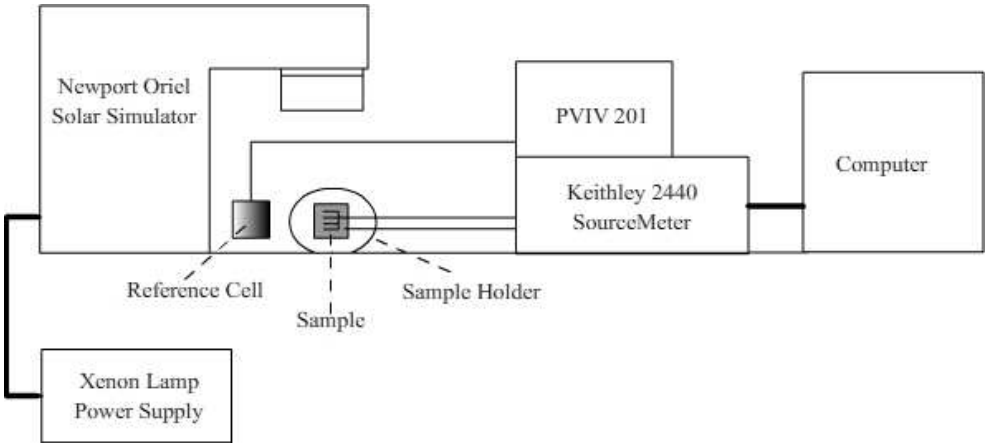

Figure 3.14: The schematic diagram of the solar simulator workstation.

voltage measurement, efficiency, fill factor, open circuit voltage, short circuit current and series resistance can be stored by this software.

CHAPTER 4

RESULTS AND DISCUSSIONS

4.1 Introduction

This chapter introduces the analyzes of the physical properties of Ag-In-Se (AIS) ternary semiconductor thin films and Si/AIS heterojunction devices deposited by thermal evaporation and RF/DC sputtering methods. This chapter is divided into two sub sections according to the deposition methods of thermal and sputtering. It demonstrates the experimental data obtained as a result of structural, electrical and optical analyzes through various experimental techniques, such as X-ray diffraction, conductivity, current voltage, temperature dependent current-voltage, frequency dependent capacitance/conductance-voltage, current-voltage measurements under solar simulated illumination and spectral response measurements. Additionally, annealing effects at different temperature on the AIS films and Si/AIS heterojunction devices are presented.

4.2 Thermally Evaporated Ag-In-Se Thin Films

Ag-In-Se(AIS) thin films were thermally deposited by using $Ag_3In_5Se_9$ and $AgInSe_2$ single crystal powders grown by Bridgman-Stockbarger technique as the evaporation source material onto low resistive Si wafers with resistivity value of 1-10 $(\Omega - cm)$, glass substrates and ITO coated glass substrates under high vacuum of about 1×10^{-6} Torr at the different substrate temperature between $150 - 250^{o}$C . Prior to thin film deposition, back surface of p-Si wafer was coated with aluminum (Al), which serves as the back ohmic contact and annealed at

500^{o}C to diffuse Al atoms into the structure and to increase the ohmicity of the contacts. The front surface was subjected to a cleaning procedure with HF:H_2O=1:10 solution in order to remove the native oxide layer and then rinsed in deionized water consecutively blown dry by N_2 as explained in chapter 3. During the deposition, the growth rate and thickness of the films were checked by Inficon XTM/2 thickness monitor. The thickness of the thin films was also measured electromechanically by a Dektak 6M thickness profilometer as in the range of 800-1500 nm for different samples. Following to the deposition of the films, the samples were annealed at different temperatures under nitrogen atmosphere in order to obtain polycrystalline thin films. Then, the front ohmic contact to the AIS thin films, with indium in 99.995% purity was deposited by metallic evaporation system as described in chapter 3 using copper masks in circular shape with 1mm diameter and grid shape under high vacuum of about 1×10^{-6} Torr. All contacts were annealed at 100^{o}C for 30 minutes to remove the interface problem between the ohmic metallic contact and thin film surface.

Deposition method and parameters such as substrate material, substrate temperature, growth rate etc. are determined for the characterization of the films. The electrical properties of the vacuum deposited films are strictly affecting the extrinsic properties rather than intrinsic properties. The stored composition on the substrate surface mainly depends on the starting compound and could be change during deposition process according to the vapor pressure of evaporating source material component. The growth parameters to control and eliminate the external effects such as impurities and stresses are very hard in thermal evaporation method. Therefore these growth problems in thin film deposition directly affecting the device behavior of the AIS films.

In literature, $AgInSe_2$ films were represented as p-type material [58]. In order to understand the conductivity type of the films, hot probe method was used and it was seen that thermally deposited AIS films have n-type conductivity. Different phases in the films and Ag deficiency could be the reason for this different conductivity mechanism as explained in Chapter 1 for $CuInSe_2$ thin films.

4.2.1 Structural Characterization of Thermally Evaporated Ag-In-Se Thin Films

X-ray diffraction (XRD) measurements were carried out for AIS thin films deposited by thermal evaporation to determine the structural properties of the samples. XRD results of the AIS thin films deposited by thermal evaporation method at 150^{o}C substrate temperature with a 1μm thickness are shown in Fig.4.1.

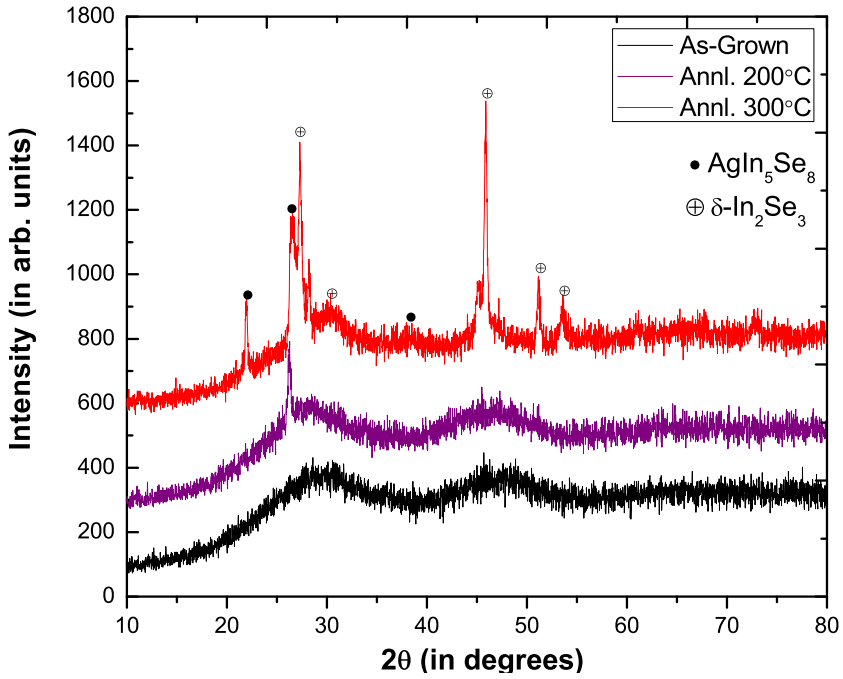

Figure 4.1: XRD pattern of the thermally evaporated as-grown and annealed AIS thin films at 200 and 300^{o}C.

There is no diffraction peak in the XRD scan that could be the result of unconstructed long-range crystallinity in the structure. In other words, AIS thin films deposited at the substrate temperature of 150^{o}C have amorphous structure in the as-grown form.

AIS films were annealed at 200 and 300^{o}C temperatures following to the growth under nitrogen atmosphere for 30 minutes. As can be seen in Fig.4.1, annealing at 200^{o}C resulted in extra $AgIn_5Se_8$ peak in the plane of (112). This

preferred orientation behind the other broaden peaks show the AIS thin films started to change from amorphous structure to the polycrystalline structure. Annealing process at 300^{o}C turns the films into polycrystalline phase with $AgIn_5Se_8$ and $\delta - In_2Se_3$ ternary and binary mixture of the constituent elements of source powder.

These modification in the structure directly affect the device behaviors of the junctions. Annealing effects on the device properties will be explained in following sections.

4.2.2 Electrical Characterization of Ag-In-Se Devices

4.2.2.1 Current-Voltage Measurements of Metal/AIS Schottky Devices

The Schottky junctions gives many information about the device properties, such as conductivity type, series resistance, barrier height, ideality factor, etc. as explained in chapter 2. To reveal these properties, following the AIS thin film deposition on ITO coated glass substrates, various metal contacts such as In, Ag, Au, Al and Pt with area of $7.5 \times 10^{-3} cm^{-2}$ were deposited in circular shape and to eliminate the contact problem, samples were annealed at 100^{o}C for 30 minutes under nitrogen atmosphere. The dark current-voltage measurements carried out at room temperature. In theory, n-type semiconductor makes rectifying junction with metals whose work functions greater than that of the semiconductor depending on the characteristics of the interface. Some metal work functions are given in Table 4.1 [59].

Table 4.1: Work functions of some metals

Metal	In	Al	Ag	Au	Pt
Work Function(eV)	4.09	4.06-4.26	4.52-4.74	5.1-5.47	5.12-5.93

However, because of the different phases in the AIS thin film structure and complex interface states in junction, all metals showed ohmic behavior ordered series resistance values in $k\Omega$ as can be seen in Fig. 4.2 except Au metal contacts.

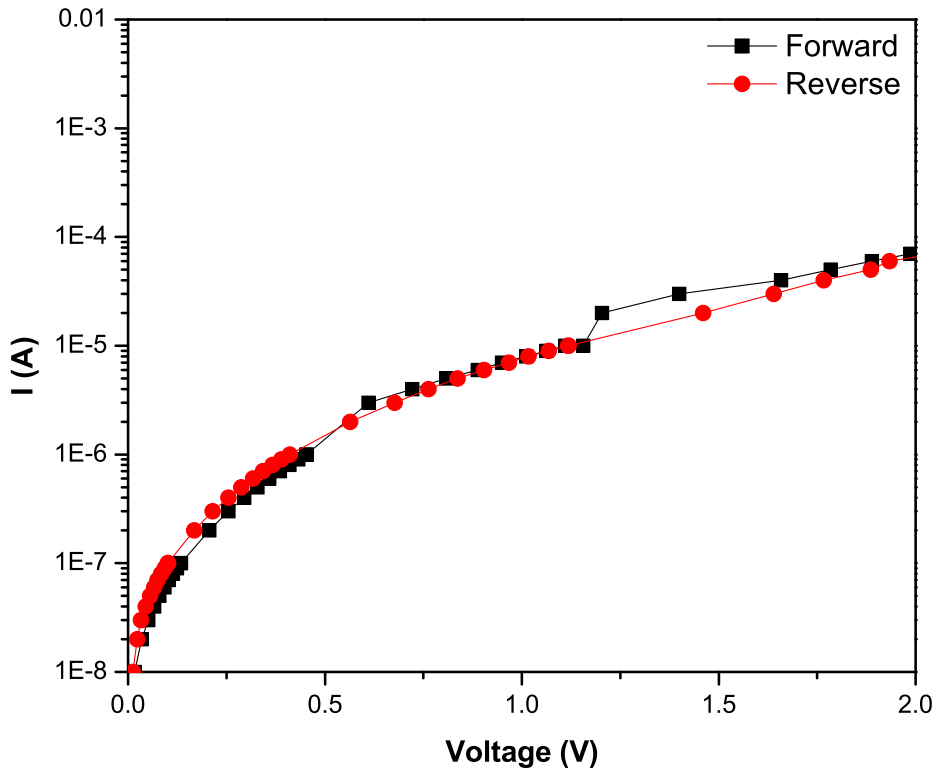

Figure 4.2: The semi-logarithmic plot of I-V for ITO/n-AIS/Al structure.

Au contacts over whole surface of the ITO/n-AIS/Au structure shows rectifying junction with a rectification factor in the order of 10^5 around 1V as shown in Fig.4.3. Still, all ITO/n-AIS/Au rectifying junctions showed different behavior after each current-voltage measurements because of the disordered interface states changing with applied current.

The ideality factor n is extracted from the slope of the lnI-V plots and the value of saturation current I_0 from the intercept of the slope as mentioned in chapter 2. This is not true for low voltages where the lnI-V characteristics deviate from linearity due to the non-exponential behavior of the junction near the origin [60]. For an ideal diode, n is constant and I_0 depends on temperature. If

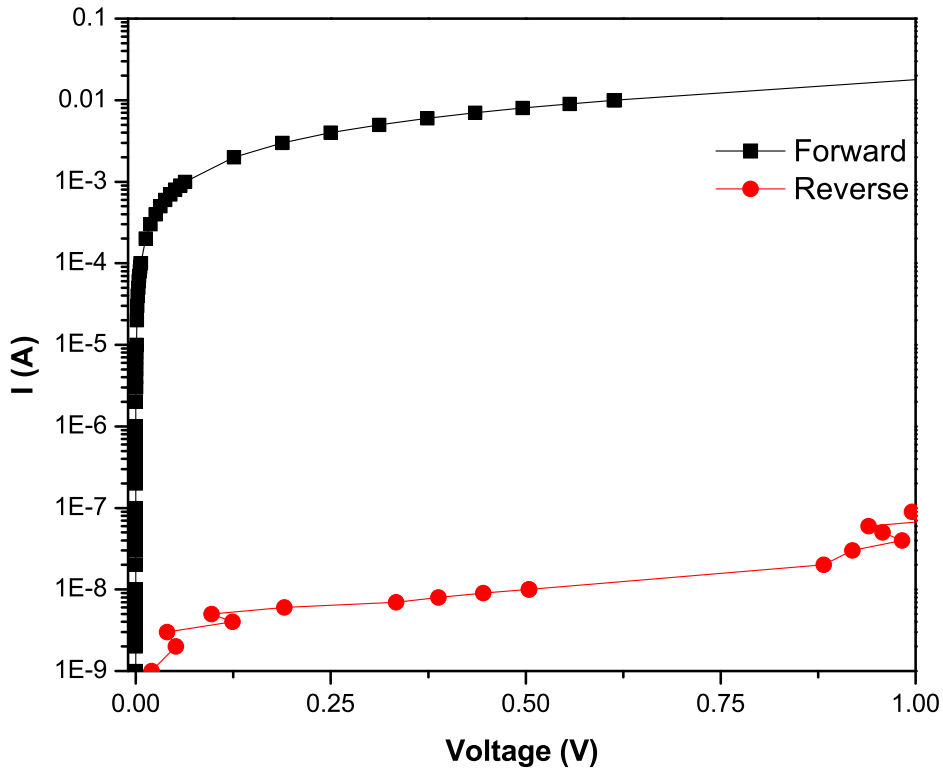

Figure 4.3: The semi-logarithmic plot of I-V for ITO/n-AIS/Au structure.

there is no recombination in the space charge region, n=1 and if the current is dominated by recombination in the space charge region, n=2. Usually, n has a value between 1 and 2, but values greater than 2 are also possible for different transport mechanism involved in junction. n less than 1 in a junction under high-level injection case with saturation current determined by Auger recombination could be the another possible mechanism in the junction [61]. From the calculation of the forward current lnI-V plot, saturation current and ideality factor were found to be around $10^{-11}A$, n lower than 1, and barrier height was around 0.66 eV. The ideality factor value and saturation current obtained from I-V measurements are clues for transport mechanism and interface states in the junction region.

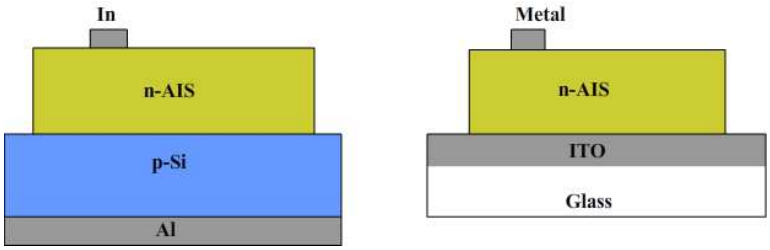

Figure 4.4: Schematic view of In/n-AIS/p-Si/Al and Metal/n-AIS/ITO device structures.

4.2.2.2 Current-Voltage Measurements of p-Si/n-AIS Heterostructure Devices

From the current-voltage measurements of the ITO/AIS/In structure it was seen that In metal makes very good ohmic contact with AIS films. Al metal also makes very good ohmic contact with Si semiconductor. By using Al metal as back contact and In metal for front contact Al/p-Si/n-AIS/In heterostructures was produced with the methods which was explained in previous chapter. To eliminate the contact problem samples were annealed at 100^{o}C for 30 minutes under nitrogen atmosphere.

In order to investigate rectifying behavior of the Al/p-Si/n-AIS/In heterojunction, the dark current-voltage characteristics were studied at room temperature. The data were analyzed by the standard diode equation (Eqn.2.9) and semi-logarithmic plot of current-voltage measurement is given in Fig.4.5.

As seen from Fig. 4.5, the current-voltage behavior of the Al/p-Si/n-AIS/In heterostructure is similar to ideal diode behavior with series resistance plot which is shown in Fig. 2.8. Calculated ideality factor and saturation current from logarithmic plots of current-voltage measurement are 2.5 and $2.9 \times 10^{-7} A$, respectively.

On the other hand, device parameters such as series resistance, barrier height and ideality factor have been determined from forward I-V characteristics by using the method developed by Sato and Yasumura [62]; and improved procedure by Cheung and Cheung [63], such that;

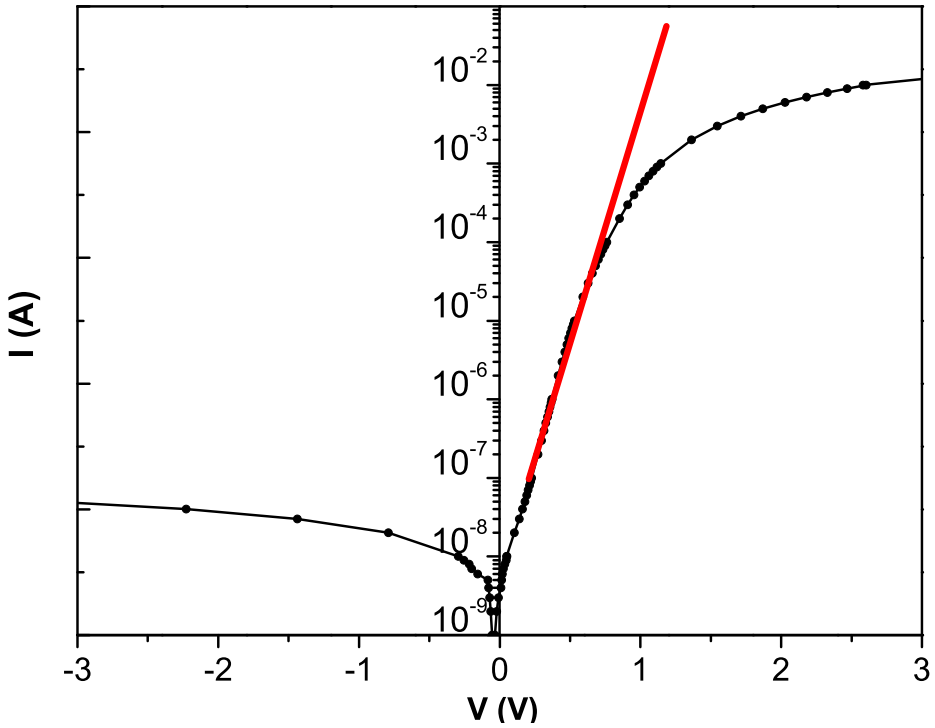

Figure 4.5: The semi-logarithmic plot of I-V for Al/p-Si/n-AIS/In heterostructure at room temperature.

$$\frac{d(V)}{d(LnJ)} = R_s AJ + \frac{n}{\beta} \tag{4.1}$$

where A is diode area and β=q/kT. The slope of the d(V)/d(ln J) vs. J plot gives R_sA and y-axis intercept equals to n/β [63]. The series resistance and ideality factor values as a result of calculation using Eqn. 4.1 for the low and high voltage region were found to be as n=2.4 and $R_s \simeq 167\Omega$ which are consistent with the values obtained from the dark I-V analysis.

The ideality factor of device is greater than ideal value. It implies that the other transport mechanism such as interface recombination, recombination-generation, tunneling, etc. are valid in the junction region. In order to investigate the transport mechanism of the Al/p-Si/n-AIS/In heterojunction, the dark I-V characteristics were studied in the temperature range of 160-360 K and shown in Fig.4.6.

The data were analyzed by the standard diode equation (Eqn.2.9); where V is

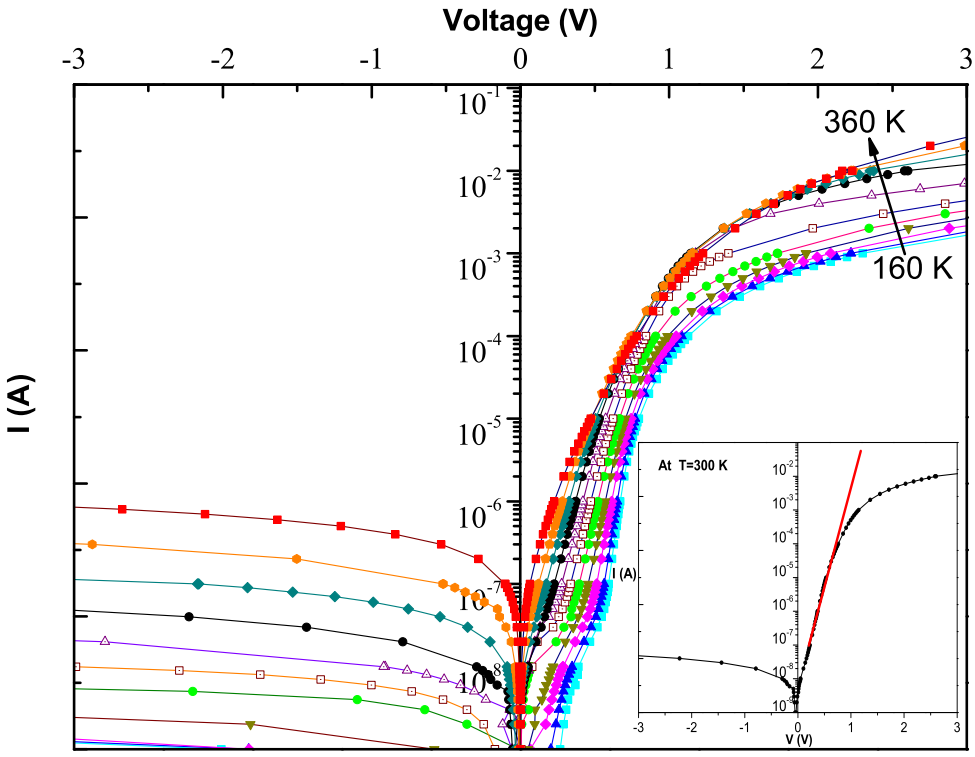

Figure 4.6: Dark forward and reverse I-V characteristics for a typical Al/p-Si/n-AIS/In sandwich structure in the temperature range of 160-360 K.

the applied voltage, R_s is the series resistance which is effective at high forward bias region and I_0 is the reverse saturation current which is given also by,

$$I_0 = I_{00}\Big(exp(-\frac{\triangle E}{kT})\Big) \tag{4.2}$$

where $\triangle E$ is the activation energy and I_{00} is a weak function of temperature. Both the ideality factor n and reverse saturation current I_0 values at different temperatures give the information about the dominating transport properties of the junction. If the current transport mechanism through the junction is dominated by a thermally activated process, the n is independent of the temperature with the values lying in between 1 and 2 and the reverse saturation current I_0 changes with temperature so that $ln(I_0) - T^{-1}$ variation is linear [64, 65].

It is seen from Fig.4.6 that Al/p-Si/n-AIS/In sandwich structure shows very good diode behavior with the rectification factor of about 10^4 for the reverse

Table 4.2: Device parameters evaluated from the temperature dependent current-voltage plots of p-Si/n-(AIS) heterojunction.

T(K)	$J_0(Acm^{-2})$	$\alpha(V^{-1})$	n	$R_s(\Omega)$
160	1.27×10^{-10}	27.21	2.67	1004
180	1.27×10^{-9}	24.71	2.61	933
200	1.15×10^{-8}	22.62	2.57	754
220	1.02×10^{-7}	20.50	2.57	568
240	7.64×10^{-7}	18.59	2.60	469
260	3.82×10^{-6}	17.20	2.60	369
280	1.27×10^{-5}	16.31	2.54	278
300	3.82×10^{-5}	15.68	2.47	177
320	8.91×10^{-5}	14.99	2.42	91
340	2.55×10^{-4}	14.35	2.38	63
360	5.09×10^{-4}	14.03	2.30	41

and forward voltage of 0.6V at all temperatures. The inset of Fig.4.6 illustrates the dark ln(I)-V variations at room temperature. The variations are linear for almost four orders of magnitude of the current, then deviation from the straight line is observed after around 1 V due to the series resistance of the device. Then, series resistance was calculated from the deviation of the I-V curve from linearity at high voltage as $R_s \simeq 177\Omega$ which is high for solar cell applications.

From the slope and intercept of the linear region of the semi-logarithmic plot of current-voltage measurement plots n and I_0 values were obtained. The calculated ideality factor value varies from 2.67 to 2.30 as the temperature increases from 160 to 360 K. Thus, n values decrease with increasing temperature and are all greater than 2, and the temperature dependence of the voltage factor ($\alpha = q/nkT$, slope of ln(I)-V plot) is in the same manner. In general, n=1 corresponds pure thermionic emission mechanism and greater than one indicates the contribution of the other conduction mechanisms to the carrier transport in the junction region, such as tunneling and recombination. Although, the values of n imply that recombination could be dominant transport mechanism, the variation of voltage factor (α) with temperature implies that thermally assisted tunneling might also contribute to the conduction mechanisms in these devices [17, 65, 66].

The activation energy ($\triangle E$) was calculated by using Eqn. 4.2 from the slope of the $ln(J_o) - 1/T$ plot (see Fig. 4.7) as about 0.39 eV and the built-in voltage V_b calculated by using the relation; $V_b = (n(\triangle E)/q$ to be around 0.96 eV at 300K [44].

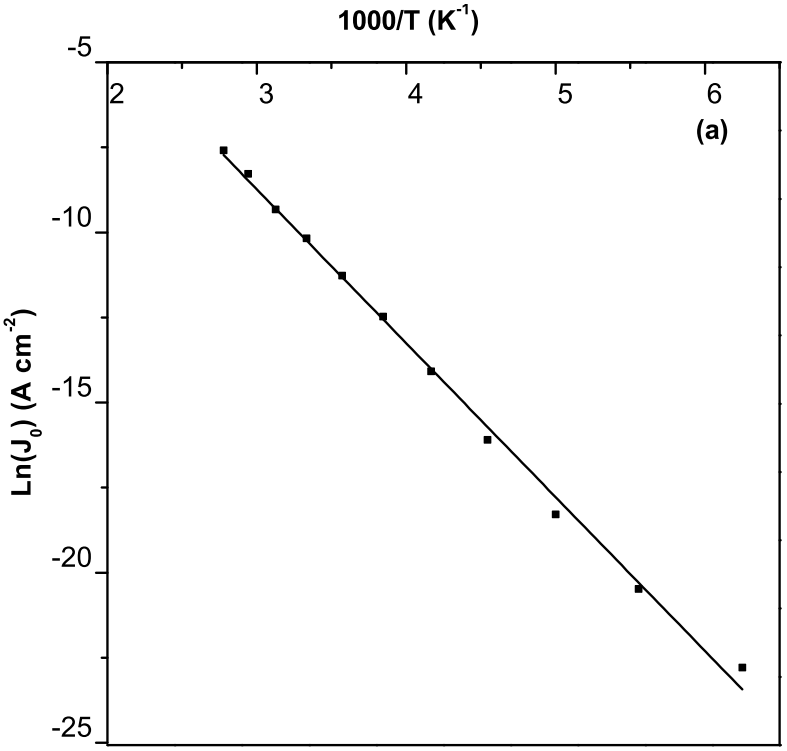

Figure 4.7: The variations of ln(J_o) vs. 1000/T for Al/p-Si/n-AIS/In devices.

In order to identify whether the interface recombination is the dominant carrier conduction mechanism or not, the activation energies obtained from the $ln(J_o) - 1000/T$ and the $ln(J_oT^{-1/2}) - 1000/T$ plots found to be as 0.39 and 0.38 eV, respectively were compared with band gap of absorbing layer. Therefore, the temperature dependence of n with the values greater than 2 and the low activation energy values show that the interface recombination is not the possible transport mechanisms in this structure [65, 66].

To check the possibility of other conduction models such as the recombination-generation in the depletion region, the semi logarithmic plot of $ln(J_oT^{-5/2}) - 1/T$

was plotted as in Fig.4.8. The activation energy calculated from $ln(J_oT^{-5/2}) - 1/T$ plot is around 0.34 eV which is smaller than the half band gap value of AIS layer, so the current transport in this structure is not dominated by the recombination-generation mechanisms in the depletion layer [66].

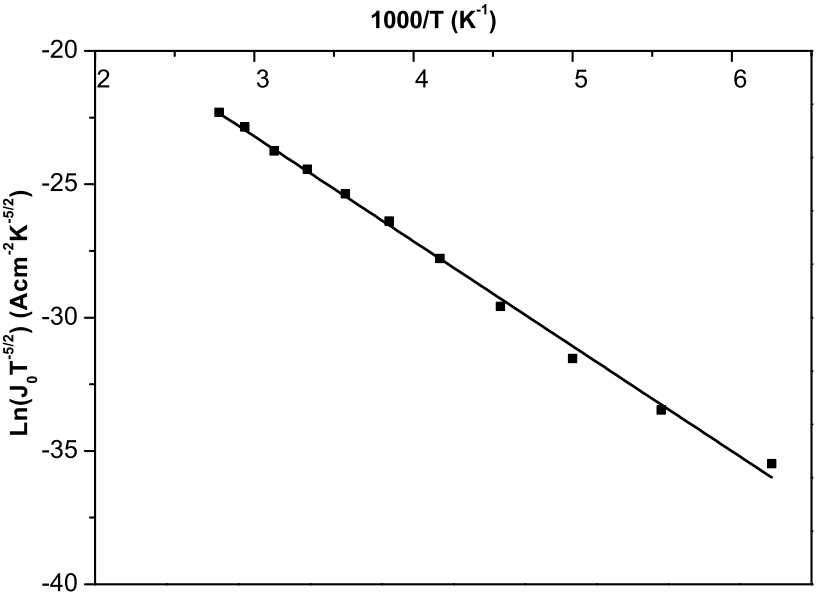

Figure 4.8: Ln ($J_0T^{-2.5}$) vs. 1000/T plot of Al/p-Si/n-AIS/In devices.

After discarding the possibility of interface recombination or recombination-generation transport mechanisms, the combination of tunneling and interface recombination mechanisms is investigated as the dominating conduction mechanism by the model introduced by Miller and Olsen [64]. According to this model, the voltage factor (α) can be expressed as,

$$\alpha = (1 - f)B + \frac{qf}{\partial kT} \tag{4.3}$$

where k is the Boltzmann constant, ∂ is the voltage division between both sides of the junction, and B is the temperature independent tunneling parameter. The f value indicates the degree of tunneling process. In its limiting case, f takes the value of "1" which implies the simple interface recombination with a requirement

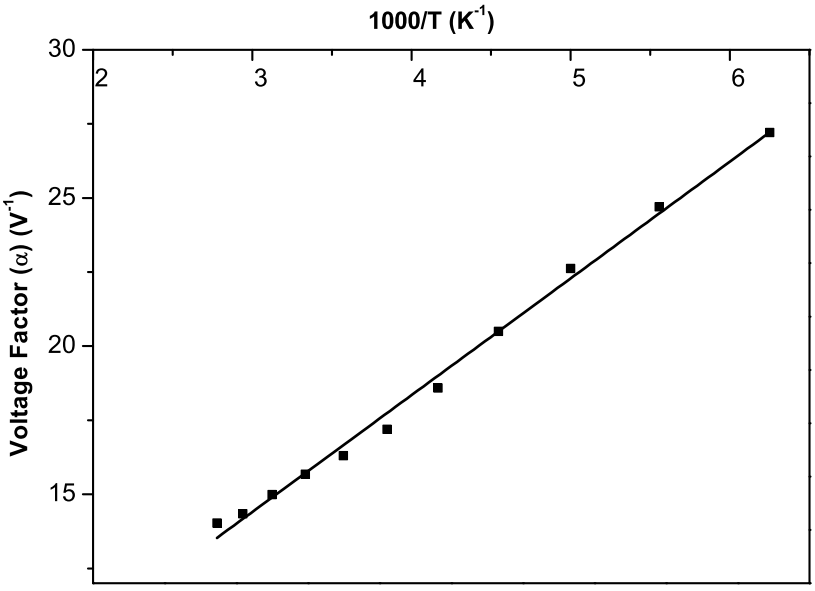

Figure 4.9: Voltage factor (α) vs. inverse temperature plot.

of B=0 and f takes the value of "0" for tunneling [64]. Therefore, the voltage factor (α) as a function of inverse temperature was plotted as in Fig.4.9. The regression of plotted data gives the values of *f/∂* as 0.34 and *(1-f)B* as 2.58 V^{-1}. It can be concluded from these calculated parameters that the current conduction is dominated by both interface recombination and thermally-assisted tunneling in these devices. The same behavior was observed in CdS/CdTe [65, 67] and ZnO/CdS/CuInSe2 [66] heterojunctions.

4.2.2.3 Capacitance-Voltage Characteristics of p-Si/n-AIS Heterostructure Devices

As mentioned in Chapter 2, the frequency dependent capacitance-voltage measurements gives information about built-in potential, carrier concentration, series resistance, surface states, etc. of the heterostructure. Forward and reverse biased junctions was measured at different frequencies by a small ac voltage with the assumptions that there is no interfacial layer between the semiconductor and uniform carrier concentrations. With these assumptions, the width of the depletion region can be obtained from Eqn.2.26 by using the abrupt junction

approximation.

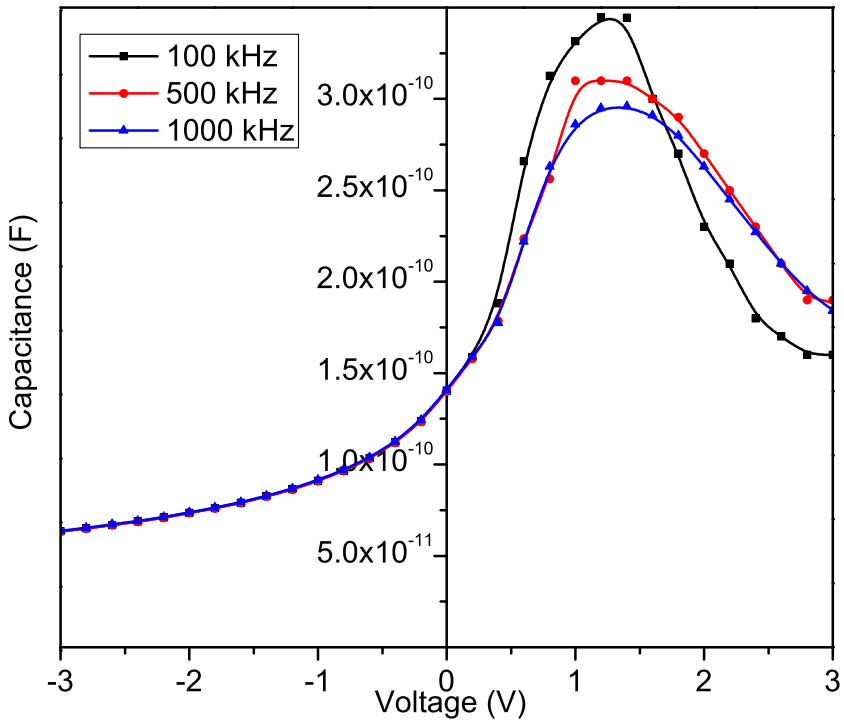

Figure 4.10: Capacitance vs. voltage plots of p-Si/n-AIS heterojunction at room temperature for different frequencies.

The dark capacitance and conductance-voltage measurements at different frequencies were carried out to obtain the further information about the junction at room temperature and the results are shown in Fig.4.10 and Fig.4.11. As seen from figure, the C-V variations show the same behavior at different frequencies.

For finding the built in potential V_b and carrier concentration N_d, $C^{-2}vs.V$ plots given in Fig.4.12 for different frequencies were used. Their variations are linear with the intercept on voltage axis which gives built-in potential and from the slope of this plot; ionized impurity concentration (N_d) can be calculated by using,

$$C = A\Big(\frac{q\varepsilon N_d}{2(V_{bi} + V_A - \frac{kT}{q})}\Big)^{1/2} \tag{4.4}$$

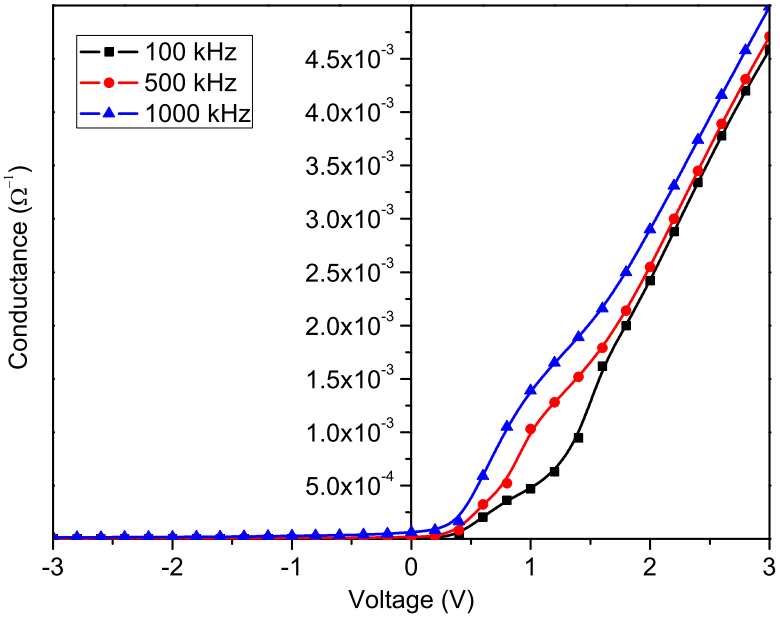

Figure 4.11: Conductance vs. voltage plots of p-Si/n-AIS heterojunction at room temperature for different frequencies.

here A is the diode area, ε_s =12.8ε_0 is the permittivity of AIS thin films [68]. So, the built-in potential and carrier concentration were calculated as $V_b = 0.91V$ and $N_d = 2.9x10^{15}cm^{-3}$, respectively. These obtained V_b and N_d values are in good agreement with the ones obtained from I-V analysis and given in the literature, respectively [16, 41].

Capacitance-voltage measurements as a function of frequency have been carried out in the range of 10-1000 kHz at room temperature and plotted as in Fig.4.13. C-V variations of the device at different frequencies are weak but capacitance changes with frequency. The frequency dependence of capacitance at zero bias is relatively strong at low frequencies and this shows the presence of high interface states responding to the ac signal and as a result of generating higher capacitance. The number of interface states (N_{ss}) is found by using the Eqn.2.36 as $9.93 \times 10^{10}cm^{-2}V^{-1}$.

From capacitance-voltage (C-V) and conductance-voltage (G-V) measurements at sufficiently high frequencies regions, series resistance (R_s) can be evaluated by using the relation;

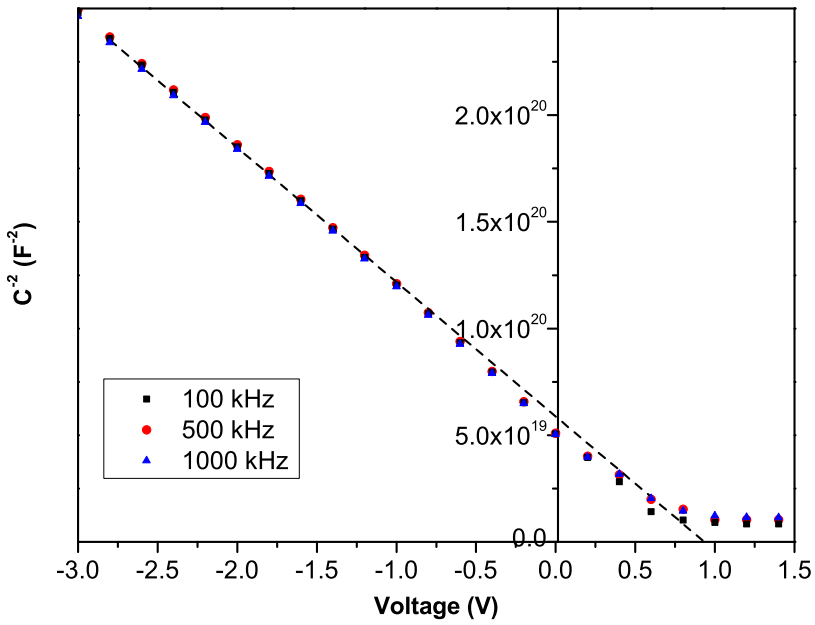

Figure 4.12: $C^{-2} vs. V$ plot of p-Si/n-AIS heterojunction at room temperature for different frequencies.

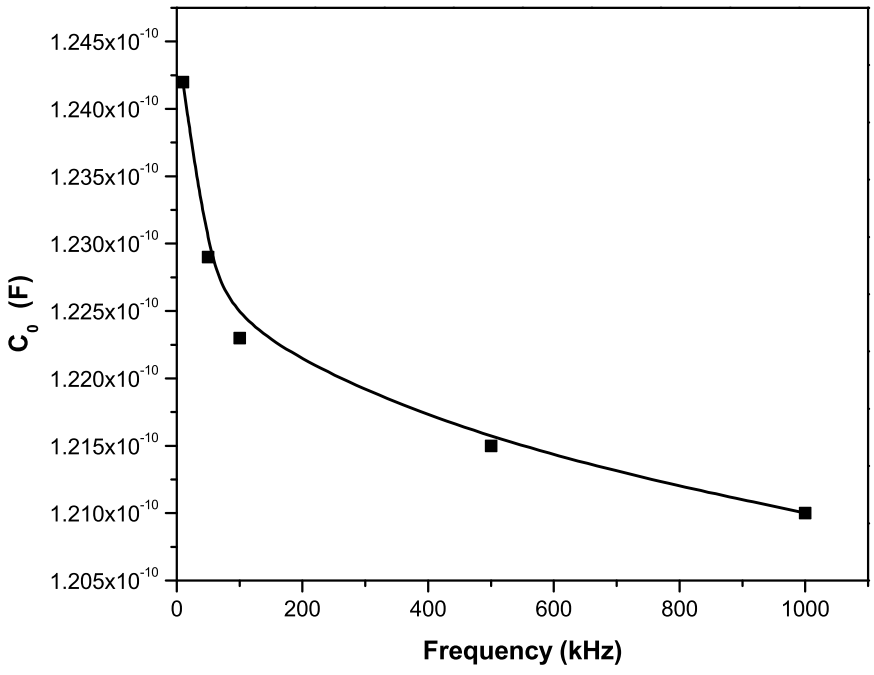

Figure 4.13: The variation of capacitance as a function of frequency at zero bias.

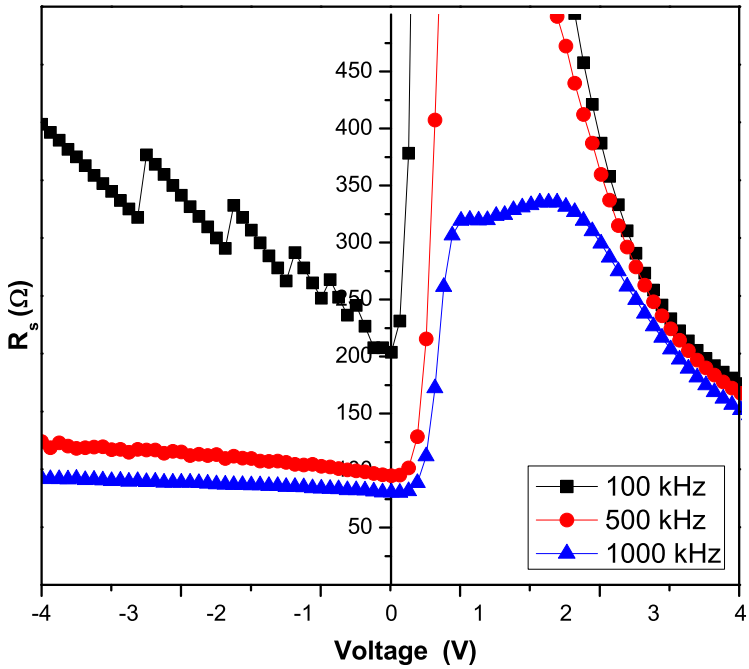

Figure 4.14: Series resistance-voltage plot of p-Si/n-AIS heterojunction at room temperature for different frequencies.

$$R_s = \frac{G_m}{G_m^2 + \omega^2 C_m^2} \tag{4.5}$$

where C_{ma} is the measured capacitance and G_{ma} is the measured conductance in strong accumulation region which was explained in Chapter 2. As a result of the calculation, the series resistance at zero bias is found to be around $\simeq 170\Omega$ which is almost the same value extracted from I-V plot. The R_s-Voltage plot of junction is given in Fig. 4.14. This series resistance value of the device is quite high for solar cell applications.

4.2.3 Spectral Response of p-Si/n-AIS Heterostructure Devices

In order to determine the device behavior under the photon incidence, spectral photo-response measurements were carried out for the light incident through the AIS layer in the wavelength range of 500-1260 nm by changing the temperature of the sample in between 80 and 360 K. As seen from Fig.4.15, the photocurrent

(I_{pc}) values at each wavelength are increasing with increasing temperature, which is the result of the decreasing series resistance with absolute temperature of the device. Moreover, one can also see from Fig.4.15 that the photocurrent spectra of these devices lie in the range of 620-1170 nm.

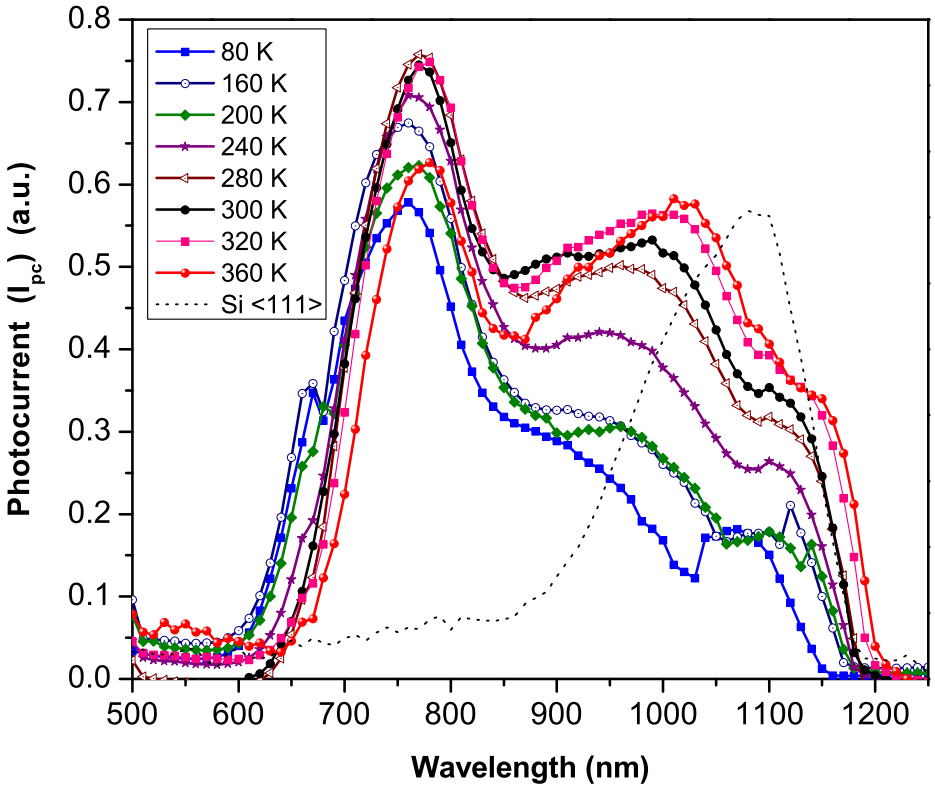

Figure 4.15: Photocurrent vs. wavelength graph of n-AIS/p-Si heterojunction at different temperatures.

In our case, the band edges were found to be at 630 nm and 1180nm, and there is a shifting of the band edge with increasing temperature. This could be related with the trap levels localized at interface and in the bulk of heterostructure. The main photocurrent peak corresponds to 1.61 eV ($\sim 770nm$) but there are two other shoulders at 1.25 eV($\sim 990nm$) and 1.10 eV($\sim 1100nm$). The energy level lying at 1.57 eV was also observed on the spectral distribution of the photoconductivity measurements carried out for AIS thin films deposited on the glass substrates. The spectral responsivity curve for the as-grown AIS

thin films deposited on glass substrates exhibited three peaks located at energies 1.57, 1.77 and 2.01 eV, whereas the corresponding curve for the 200^oC annealed films has two peaks at 1.68 and 1.89 eV energy values at room temperature. Experimentally determined energy values, which are 1.72 and 1.71 eV, from the optical absorption analysis were very close to the observed values for the amorphous as-grown thin films [19, 39]. The other two photocurrent maxima seen in Fig.4.15 are most probably related with the localized trap levels of the interface state, and the band gap of Si substrate which is around 1.1 eV.

The barrier height (Φ_b) p-Si/n-AIS heterostructure was evaluated from the spectral response measurements of the photo-current. Hence, the photocurrent (I_{pc}) generated by incident photon with an energy $h\nu > \Phi_b$, can be expressed by the Fowler relation as [43, 69];

$$I_{pc} = B(h\nu - \Phi_b)^2 \tag{4.6}$$

where B is a constant. Calculated barrier height from the intercept of the $(I_{pc})^{1/2} - h\nu$ plot decreases from 1.05 to 0.99 eV with increasing temperature from 80 to 360 K. The calculated barrier height with the value of 1.01 eV at room temperature is different from the values obtained from I-V measurements, but slightly different from the value of 0.96 eV obtained from C-V measurements. This could be the reasons of defects and acting transport mechanism at the junction region and that could raise n values and lowers Φ_b. The I-V is the most sensitive to these localized traps. Although, C-V measurements are less liable to such defects, they can vary the space-charge region width and the intercept value. Photocurrent measurements are less delicate to such defects and this method is taken as the most assuring [43].

In order to see the effects and contributions of p-Si on this device structure, the photocurrent spectra of the same p-Si(111) wafer used in this study were measured under the same conditions after metallic evaporation of indium circular dots and to check diode behavior of In/p-Si(111)/Al structures. As seen in Fig.4.15, the photocurrent spectra of n-AIS/p-Si heterostructure are completely related with the AIS films. Furthermore, the photocurrent values of the short

wavelength side is higher than the long wavelength side, this implies that the most of the contact potential drop occurred in AIS thin film because of the high resistivity [70].

For the lower value of the incident wavelength, photocurrent starts to decrease sharply, because of the high energetic photons are absorbed at or near the surface where the recombination process occurs. Spectral response range of the thermally deposited AIS thin films are wide enough and also includes the main photocurrent energy maxima at 1.35 eV ($\sim 920nm$).

4.2.4 Current-Voltage Characteristics of the p-Si/n-AIS Heterostructure Devices Under Illumination

The photovoltaic behavior of the p-Si/n-AIS heterojunction were studied as explained in Chapter 3 under simulated AM1 conditions ($\sim 925Wm^{-2}$) at room temperature. Illuminated current-voltage characteristics of the p-Si/n-AIS structure were given in Fig.4.16.

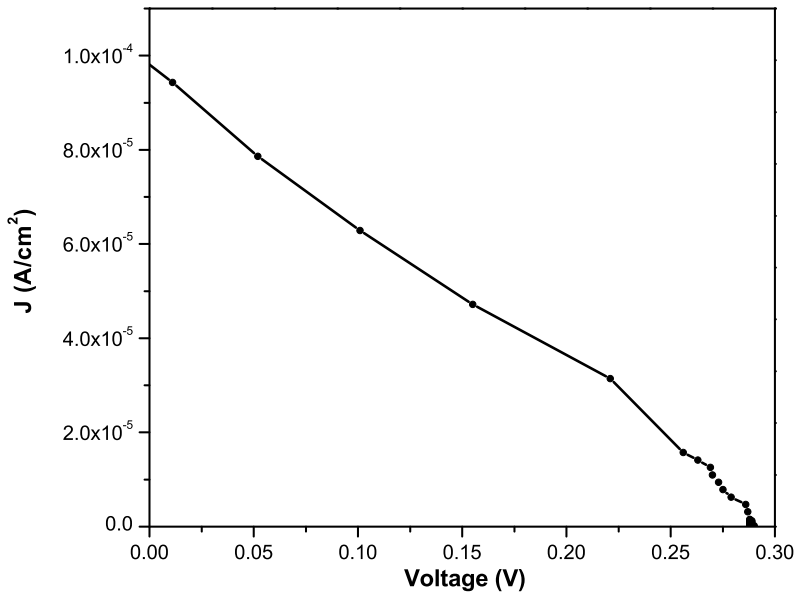

Figure 4.16: Current-Voltage characteristic under AM1 illumination for p-Si/n-AIS structure.

Solar cell conversion efficiency is depend on many parameters such as ideality value of the junction, band gap, series resistance, shunt resistance etc. As can be seen from Fig.4.16, the fill factor of this structure is low and calculated using the Eqn. 2.39 as FF=32%. The open circuit voltage V_{oc} and short circuit current I_{sc} values were calculated as $0.29V$ and $9\times10^{-5}Acm^{-2}$ respectively. Eventhough the band gap of the AIS films close the ideal value, solar cell efficiency was calculated by using Eqn.2.40 as $\eta = 0.10\%$ which is very low because of the high series resistance value of the structure($R_s \sim 170\Omega$). Such a high series resistance increase the probability of recombination of the photogenerated electron-hole pairs before reaching the contacts and decreasing the efficiency of the devices dramatically.

4.2.5 Annealing Effect on Device behavior of the p-Si/n-AIS Heterostructure

To understand the effects of annealing processes on the device behavior, the samples were annealed at 180, 200, 240 and 280^oC under nitrogen atmosphere and then ohmic indium contacts were deposited on the AIS films. Following to these processes, dark current-voltage (I-V) measurements were carried out as shown in Fig. 4.17.

As seen from the figure, the current is increasing at constant bias that can be the indication of the decreasing series resistance with annealing. Such that the annealing provides enough thermal energy to the constituent atoms in the AIS film to decorate the structure of the films and the device behavior by reducing the effect of interface state.

Capacitance-voltage and conductance-voltage measurements were also carried out as given in Fig.4.18 and Fig.4.19, respectively. As observed from these figures, annealing increases the zero bias capacitance value which corresponds the decreasing the width of the depletion region. Also conductance of the structure was increased by annealing as a clue for decreasing series resistance as observed from the current-voltage measurements.

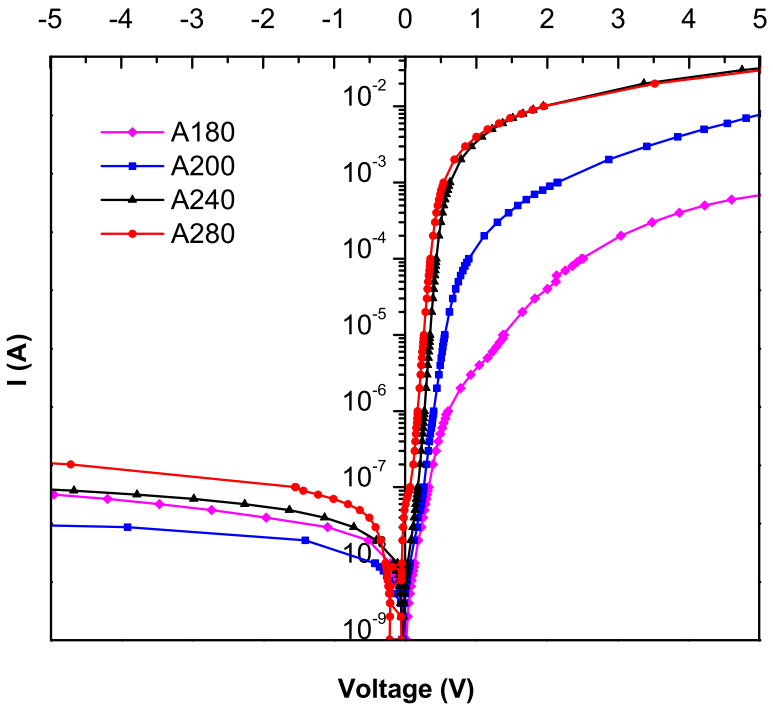

Figure 4.17: Annealing effect on dark current-voltage characteristic of In/n-AIS/p-Si/Al structure.

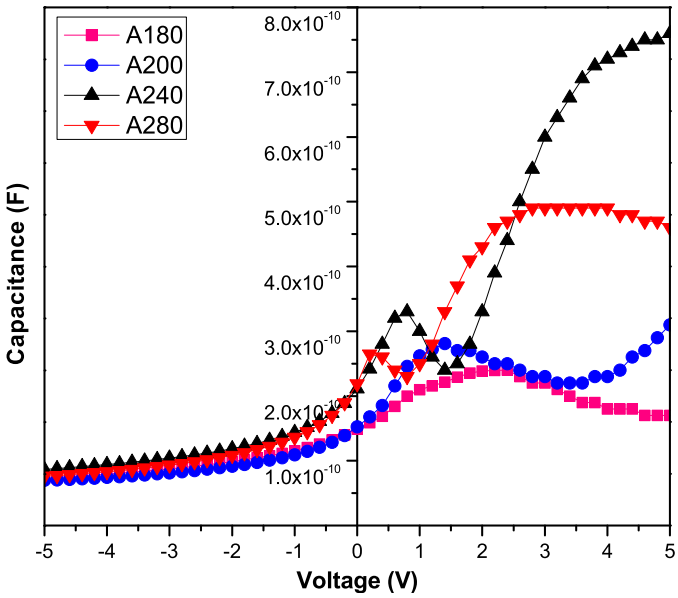

Figure 4.18: Annealing effect on dark capacitance-voltage characteristic of In/n-AIS/p-Si/Al structure at 500kHz frequency.

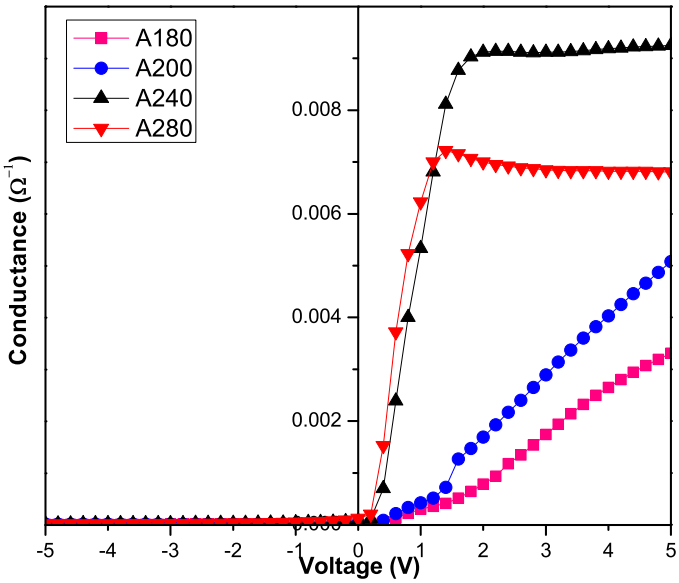

Figure 4.19: Annealing effect on dark conductance-voltage characteristic of In/n-AIS/p-Si/Al structure at 500kHz frequency.

In order to get the information related to the effect of annealing on the device behavior, photoresponse measurements were also carried out in the wavelength range of 500-1280 nm for each annealing temperature. As observed from Fig.4.20, the short-wavelength cut-off and long-wavelength fall-off correspond (2.0eV, 1.05eV) to the band gap values of the AIS thin film and p-Si substrate, respectively. Increasing the annealing temperature shifted the main peak from AIS side to Si side. That can also be taken as the further indication of the decreasing series resistance and the effect of interface states between AIS film and Si layer.

On the other hand, photovoltaic behavior of n-AIS/p-Si structure has been worked out under simulated AM1 conditions (100 $mWcm^{-2}$) at 300 K for different annealing temperatures and shown in Fig.4.21. Short circuit current (I_{sc}) and open circuit voltage (V_{oc}) were measured and listed in Table 4.3. The efficiency value was less than 1% for the samples annealed at 180 and 200 ^{0}C, which was quite small because of the high series resistance. The high value of the series resistance increases recombination of photo-generated carriers that reduces the

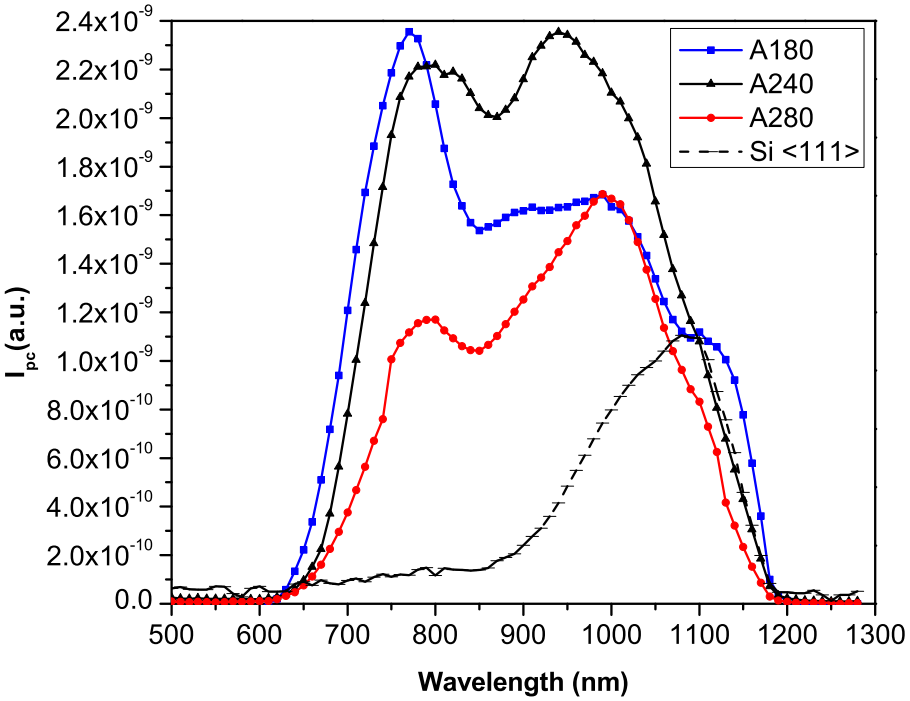

Figure 4.20: Photocurrent vs. wavelength plots of n-AIS/p-Si structure for different annealing temperatures together with In/p-Si structure.

carrier collection by the contacts and results in the small values of the efficiency and fill factor. However, further increasing of the annealing temperature to 240 ^{0}C produced the improved device characteristics as seen from Table 4.3.

Table 4.3: Device parameters of In/n-AIS/p-Si/Al structure calculated from dark and illuminated I-V data as a function of annealing temperature.

Annealing Temperature (^{0}C)	R_s (Ω)	n	J_{sc} (A-cm^{-2})	V_{oc} (V)	η	FF
180	170	2.89	0.00009	0.293	0.10%	32
200	130	2.47	0.00616	0.418	0.50%	21
240	91	1.48	0.01306	0.312	2.60%	63
280	105	1.47	0.01160	0.265	1.50%	47

Higher annealing temperatures resulted in the changes in the structure of the films as depicted in Fig.4.1, these changes directly affected the device behaviors

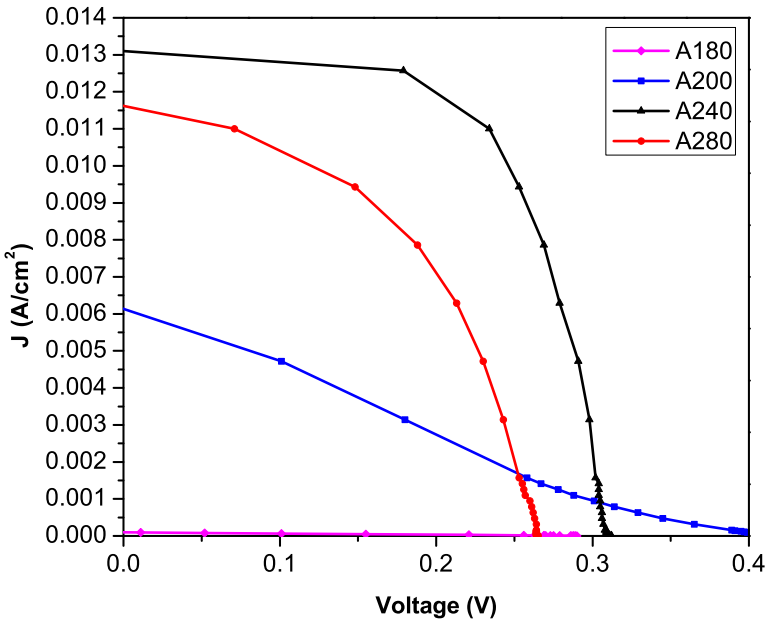

Figure 4.21: Illuminated J-V plot of Al/p-Si/n-AIS/In device under simulated AM1 conditions for different annealing temperatures, at 300K.

of the junction and the solar energy conversion parameters as listed in Table4.3.

4.3 RF/DC Sputtered Ag-In-Se Thin Films

Ag-In-Se(AIS) thin films were deposited by using InSe and Ag targets as the sputtering sources onto the low resistive Si wafers with the resistivity value of 1-10 $(\Omega - cm)$, glass and ITO coated glass substrates of the 150, 200^{o}C and room temperatures.

InSe and Ag bulk targets were sputtered by RF and DC sputtering techniques, under argon (Ar (99.99%)) gas pressure around 5×10^{-3} Torr by Fokus RF generator and MDX500 DC power supply at 40W plasma powers respectively. Before the deposition, back surface of p-Si wafer was coated with aluminum (Al), which serves as the back ohmic contact and annealed at 500^{o}C to improve ohmic behavior of the contacts. The front surface was subjected to a cleaning procedure with HF:H_2O=1:10 solution in order to remove the native oxide layer and then rinsed in deionized water consecutively blown dry in N_2 which is similar procedures as applied before thermal evaporation process. During the deposition, the

growth rate and thickness of the films were checked by Inficon XTM /2 thickness monitor. The thickness of the thin films was determined electromechanically by a Dektak 6M thickness profilometer in between 600 and 1200 nm for different samples.

To deposit $AgInSe_2$ thin films, InSe and Ag targets were sputtered by layer-by-layer respectively according to molar ratio of the constituent elements up to desired thickness of the AIS film. After thin film deposition, all samples were annealed at different temperature in inert nitrogen gas or selenium ambient which is called "two stage process".

Then, the front ohmic contact to the AIS thin films, indium with 99.995 % purity was deposited by metallic evaporation system in circular shape and grid with $1cm^2$ area under high vacuum of about 1×10^{-6} Torr. All contacts were annealed at 100^oC for 30 minutes to decrease the interface problem between the ohmic metallic contact and thin film surface.

In literature, $AgInSe_2$ films were represented as p-type material. In order to understand the conductivity type of the films, hot probe method was used. It was observed that RF/DC sputtered AIS thin films after selenization have p-type conductivity. Eliminating the Ag deficiency by using layer-by-layer sputtering process and increasing the selenium portion in the structure by selenization canceled out the different phases in the structure and resulted in p-type conductivity mechanism.

4.3.1 Structural Characterization of RF/DC Sputtered Ag-In-Se Thin Films

X-ray diffraction (XRD) measurements were carried out for AIS thin films deposited by RF/DC sputtering to determine the structural properties of the films. XRD measurements of the AIS thin films deposited by sputtering technique at room temperature was shown in Fig.4.22.

The diffraction peak seen at 38^o for as-grown sample is related with Ag phase. The other peaks with low intensities and Ag peak show that long-range crys-

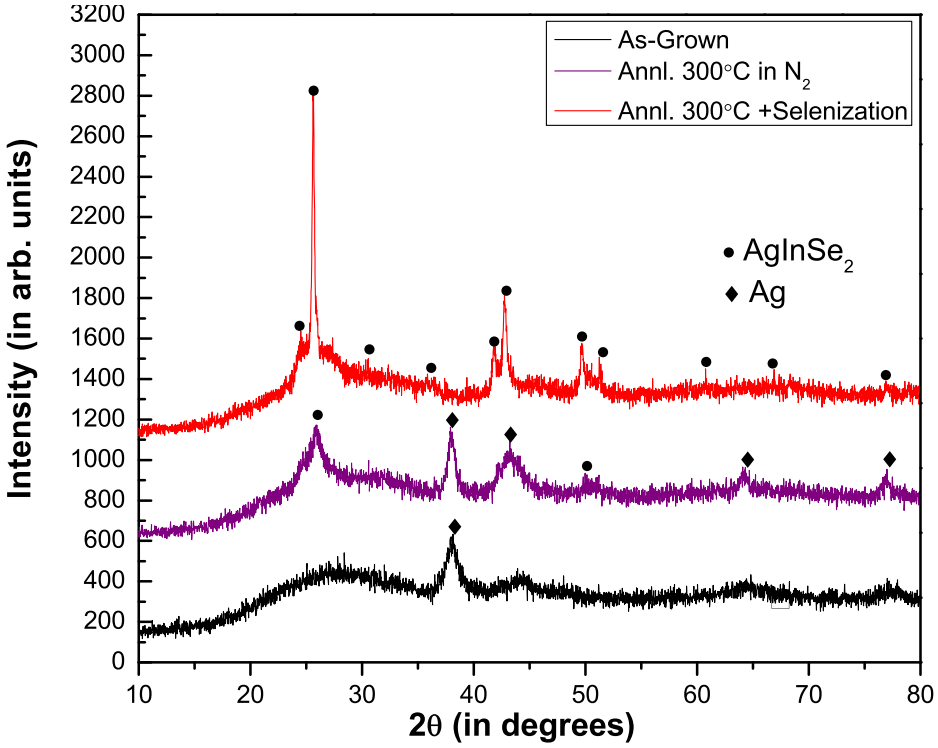

Figure 4.22: XRD pattern of the RF/DC sputtered AIS thin films as-grown, annealed at 300^{o}C in N_2 ambient and at 300^{o}C with selenization.

tallinity was not formed and Ag couldn't react with InSe compound. AIS thin films deposited at room temperature haven't shown single (AIS) phase in the as-grown form.

AIS films were annealed at 300^{o}C under nitrogen atmosphere for 30 minutes. As seen from Fig.4.22, annealing the samples in nitrogen ambient resulted in other diffraction peaks of Ag, InSe and $AgInSe_2$ phases. The increasing intensities of diffraction peaks and growing the new phases show that AIS thin films are started to change their structural behavior and form single phase.

AIS films were also annealed at 300^{o}C under vacuum with Se evaporation for 30 minutes. AIS substrate temperature was slowly increased up to 300^{o}C with steady Se evaporation and after 30 minutes annealing, samples were cooled down slowly. The Se evaporation was stopped when substrate temperature decreased to 150^{o}C. As shown in Fig.4.22, two stage process (selenization) changes the film structure from polyphase to monophase $AgInSe_2$ thin film. There are no extra

peaks except tetragonal $AgInSe_2$ phase with preferred (112) orientation. After selenization $AgInSe_2$ thin film thickness was measured by Dektak 6M thickness profilometer and it was observed that, thin film thickness was increased from $0.5\mu m$ to $1\mu m$ by selenization proofing the Se reacting with amorphous AIS thin film. Similar behavior was reported for CIS thin films deposited by two stage selenization [71]. Finally XRD pattern shows that, after applying selenization and annealing process, monophase $AgInSe_2$ thin films were obtained.

4.3.2 Electrical Characterization of Ag-In-Se Devices

4.3.2.1 Current-Voltage Measurements of n-p-Si/p-AIS Heterostructure Devices

Similar to previous heterostructure production procedure used for thermally evaporated films, Al metal was used as back contact and In metal was used for front contact. The $Al/p-Si/p-AgInSe_2/In$ and $Al/n-Si/p-AgInSe_2/In$ heterostructures were produced by applying the sputtering methods and two stage procedure (selenization) which were explained in previous sections. To eliminate the contact problem samples were annealed at 100^oC for 30 minutes under nitrogen atmosphere.

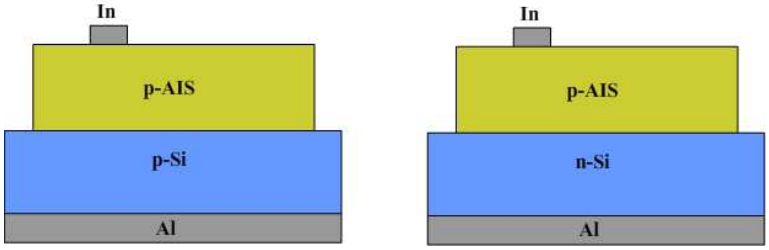

Figure 4.23: Schematic view of In/p-AIS/p-Si/Al and In/p-AIS/n-Si/Al device structures.

In order to investigate rectifying behavior of the $Al/p-Si/p-AgInSe_2/In$ and $Al/n-Si/p-AgInSe_2/In$ heterojunctions, the dark current-voltage characteristics were studied at room temperature. The data were analyzed by the

standard diode equation (Eqn.2.9) and I-V dependence plots are given in Fig. 4.24 and Fig. 4.25 for Al/p-Si/p-AIS/In and Al/p-Si/p-AIS/In heterojunctions, respectively.

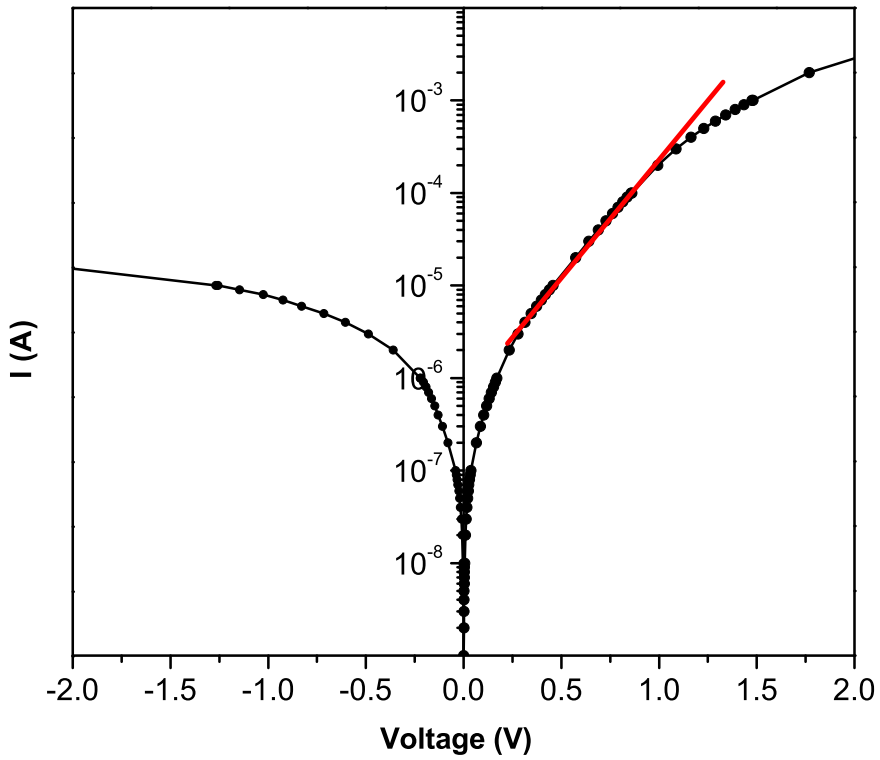

Figure 4.24: The semi-logarithmic plot of I-V for Al/p-Si/p-AIS/In heterostructure at room temperature.

As seen from Fig. 4.24, the current-voltage behavior of the Al/p-Si/p-AIS/In heterostructure differs from ideal diode behavior because of the $p^+ - p$ type of the heterojunction and series resistance. Rectifying factors of this junction was one order of magnitude around 1V forward-reverse bias. Calculated ideality factor, saturation current and series resistance from semilogarithmic I-V plots are $n = 2.35$, $I_0 = 6 \times 10^{-8} A$ and $Rs = 90\Omega$, respectively.

The current-voltage behavior of the Al/n-Si/p-AIS/In heterostructure is similar to ideal diode which is shown in Fig.4.25. The Al/n-Si/p-AIS/In structure shows very good diode properties with the rectification factor of about 6 orders

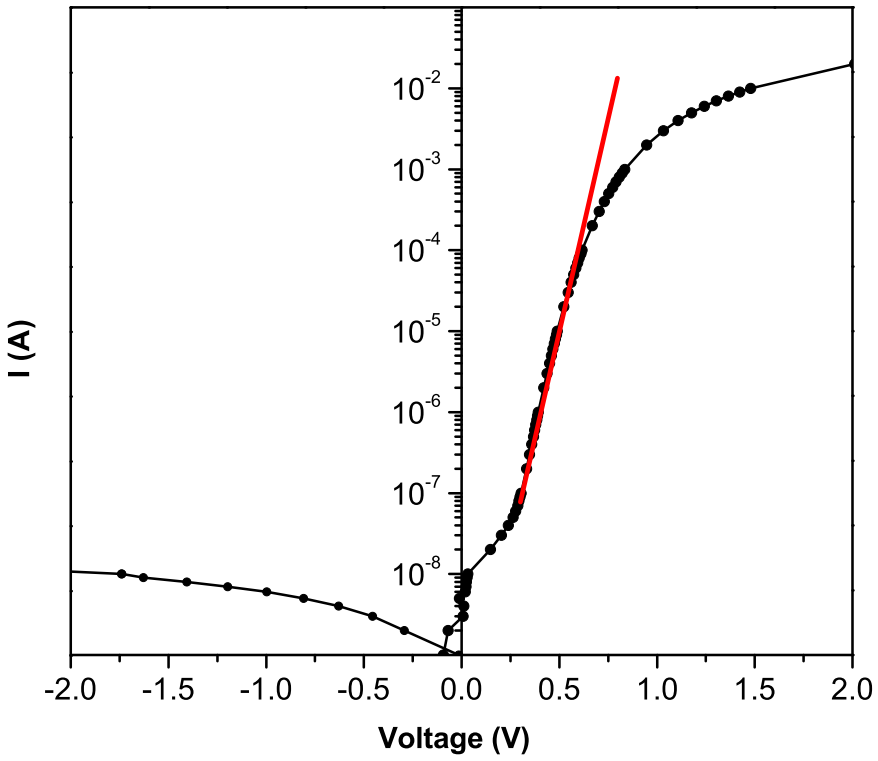

Figure 4.25: The semi-logarithmic plot of I-V for Al/n-Si/p-AIS/In heterostructure at room temperature.

of magnitude as defined by the ratio (I_F/I_R) of the reverse and forward currents at the constant voltage of about 1V and room temperature. Calculated ideality factor, saturation current and series resistance from logarithmic plots of current-voltage measurement are $n = 1.5$, $I_0 = 4 \times 10^{-11} A$ and $Rs = 80\Omega$, respectively.

When there is no recombination in the space charge region, n has a value of 1. However, if the current is dominated by recombination in the space charge region, n is equal to 2. Usually, n has a value between 1 and 2 and this is indicating particularly diffusion current rather than generation/recombination current in the depletion region [72]. In order to clarify the transport mechanism of the Al/n-Si/p-AIS/In heterojunction, the dark I-V characteristics were studied in the temperature range of 160-360 K and shown in Fig.4.26.

As a result of analyzes of I-V behavior by the standard diode equation (Eqn.2.9) and diode ideality factor (n), reverse saturation current (I_0), voltage

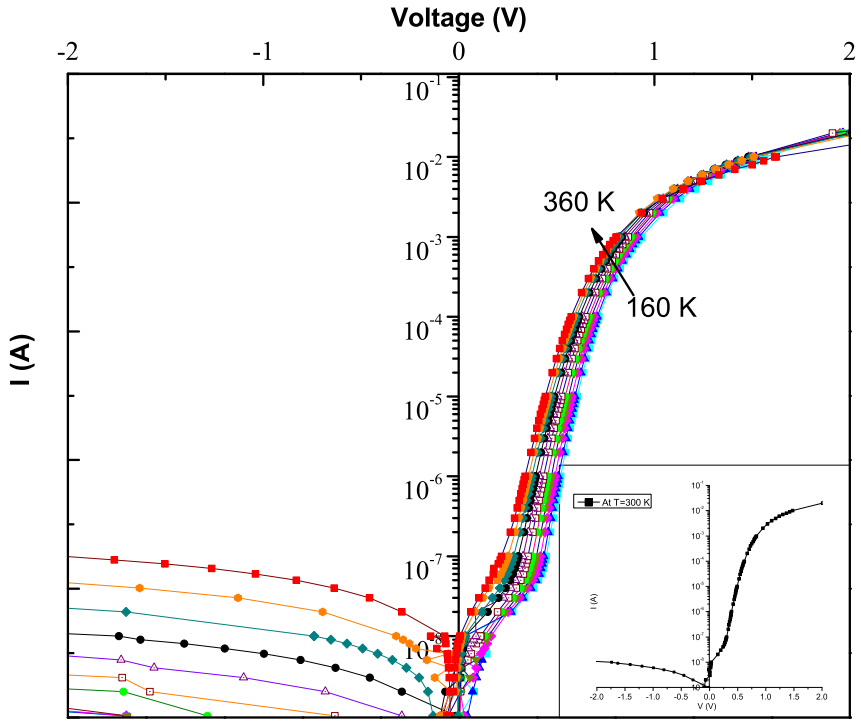

Figure 4.26: Dark forward and reverse I-V characteristics for a typical Al/n-Si/p-AIS/In sandwich structure in the temperature range of 160-360 K.

factor (α) are represented in Table 4.4 . It is seen from Fig.4.4 that Al/n-Si/p-AIS/In sandwich structure shows very good diode behavior with the rectification factor of about 10^6 for the reverse and forward voltage of 1V at all temperatures. The variations are linear for almost six orders of magnitude of the current, then deviation from the straight line is observed after around 1 V due to the series resistance of the device. Then, series resistance was calculated from the deviation of the I-V slope at high voltage as $R_s \simeq 80\Omega$ which is high for solar cell applications.

The activation energy ($\triangle E$) was calculated by using Eqn. 4.2 from the slope of the $ln(J_o) - 1/T$ plot (see Fig. 4.27) as about 0.20 eV and the built-in voltage V_b calculated by using the relation; $V_b = (n(\triangle E)/q$ to be around 0.30V at 300K [44].

Table 4.4: Device parameters evaluated from the temperature dependent current-voltage plots of n-Si/p-(AIS) heterojunction.

T(K)	$J_0(Acm^{-2})$	$\alpha(V^{-1})$	n
160	2.55×10^{-11}	29.81	2.4
180	3.82×10^{-11}	29.52	2.2
200	1.15×10^{-10}	28.24	2.1
220	2.55×10^{-10}	27.85	1.9
240	5.09×10^{-10}	27.24	1.8
260	8.91×10^{-10}	27.36	1.6
280	2.55×10^{-9}	26.43	1.6
300	5.09×10^{-9}	25.60	1.5
320	1.27×10^{-8}	24.59	1.5
340	2.55×10^{-8}	23.65	1.4
360	6.37×10^{-8}	22.62	1.4

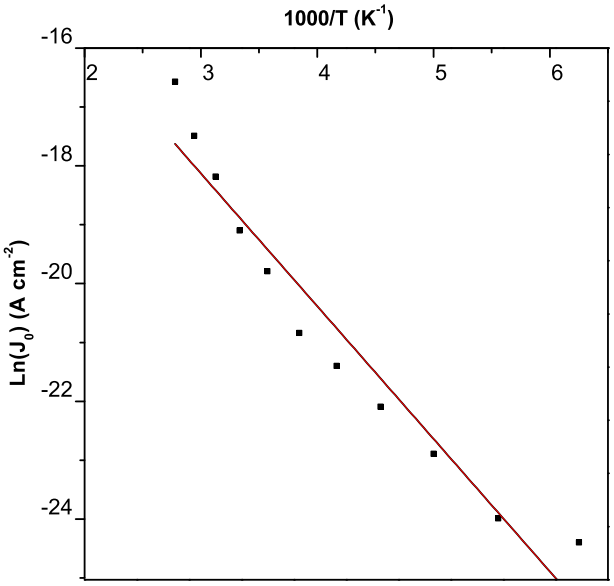

Figure 4.27: The variations of $\ln(J_o)$ vs. 1000/T for Al/n-Si/p-AIS/In devices.

4.3.2.2 Capacitance-Voltage Characteristics of n-Si/p-AIS Heterostructure Devices

To conclude the frequency dependent capacitance-voltage measurements, forward and reverse biased junctions was measured at different frequencies by a small ac

voltage is applied with the assumptions that there is no interfacial layer between the semiconductor and uniform carrier concentrations. With these assumptions, the width of the depletion region can be obtained from Eqn.2.26 by using the abrupt junction approximation.

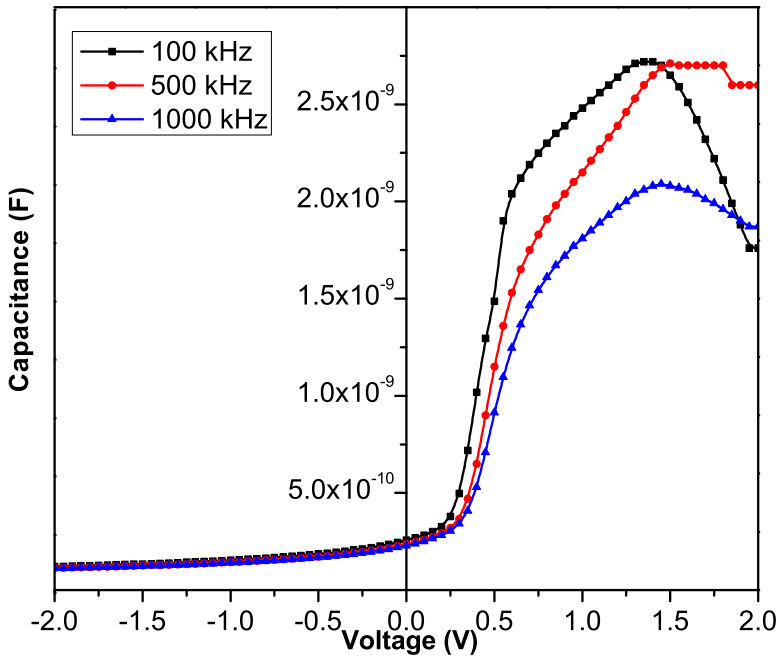

Figure 4.28: Capacitance vs. voltage plots of n-Si/p-AIS heterojunction at room temperature for different frequencies.

The dark capacitance and conductance-voltage measurements at different frequencies were carried out to obtain the further information about the junction at room temperature and the results are shown in Fig.4.28 and Fig.4.29. As seen from figure, the C-V variations show the same behavior at different frequencies.

To find the built in potential V_b and carrier concentration N_d, $C^{-2} vs. V$ plots given in Fig.4.30 for different frequencies were used. Their variations are linear with the intercept on voltage axis which gives built-in potential and from the slope of this plot; ionized impurity concentration (N_d) calculated as $V_b = 0.65V$ and $N_d = 8.79x10^{15} cm^{-3}$, respectively.

Capacitance-voltage measurements as a function of frequency have been car-

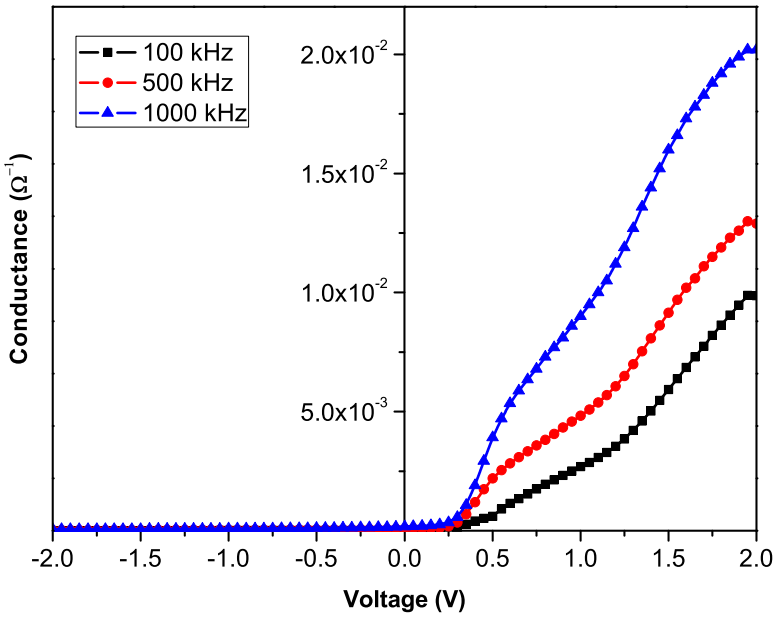

Figure 4.29: Conductance vs. voltage plots of n-Si/p-AIS heterojunction at room temperature for different frequencies.

ried out in the range of 10-1000 kHz at room temperature and it is shown in Fig.4.31. The frequency dependence of capacitance at zero bias is relatively strong at low frequencies. This implies the presence of high interface states responding to the ac signal and generating higher capacitance. The number of interface states (N_{ss}) is found by using the Eqn. 2.36 as $2.1 \times 10^{12} cm^{-2} V^{-1}$ which is grater than the thermally evaporated devices.

As mentioned in previous section, the series resistance of device can be obtained from measured capacitance and conductance in strong accumulation region at high frequencies (i.e. 1MHz) [43, 47]. To calculate series resistance (R_s) from capacitance-voltage (C-V) and conductance-voltage (G-V) measurements at sufficiently high frequency regions, Eqn.4.5 was used. The calculated series resistance at zero bias is found to be around $\simeq 79\Omega$ which is almost the same value extracted from I-V plot. The R_s-Voltage plot of junction is given in Fig. 4.32.

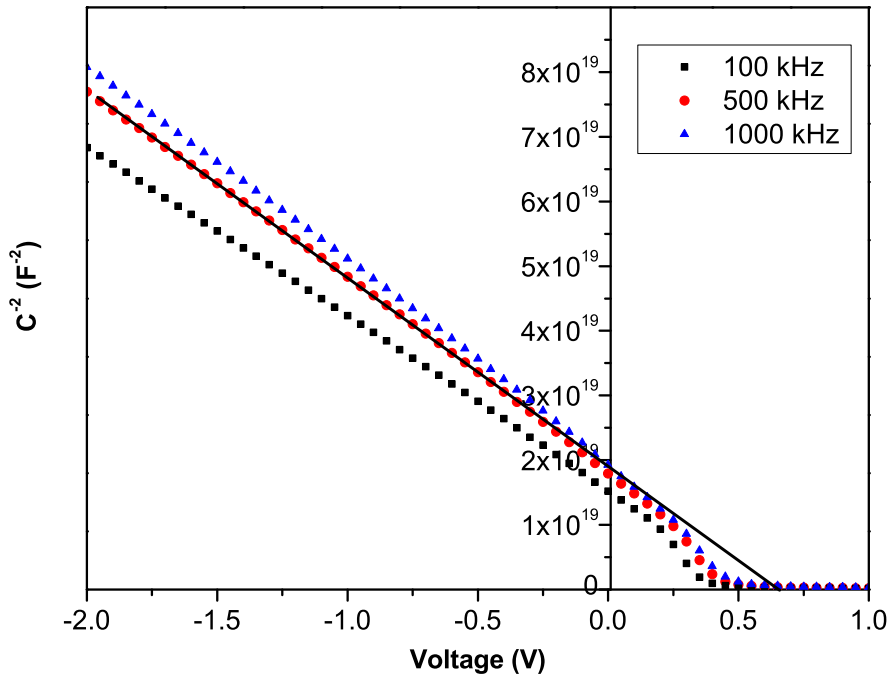

Figure 4.30: $C^{-2} vs. V$ plot of n-Si/p-AIS heterojunction at room temperature for different frequencies.

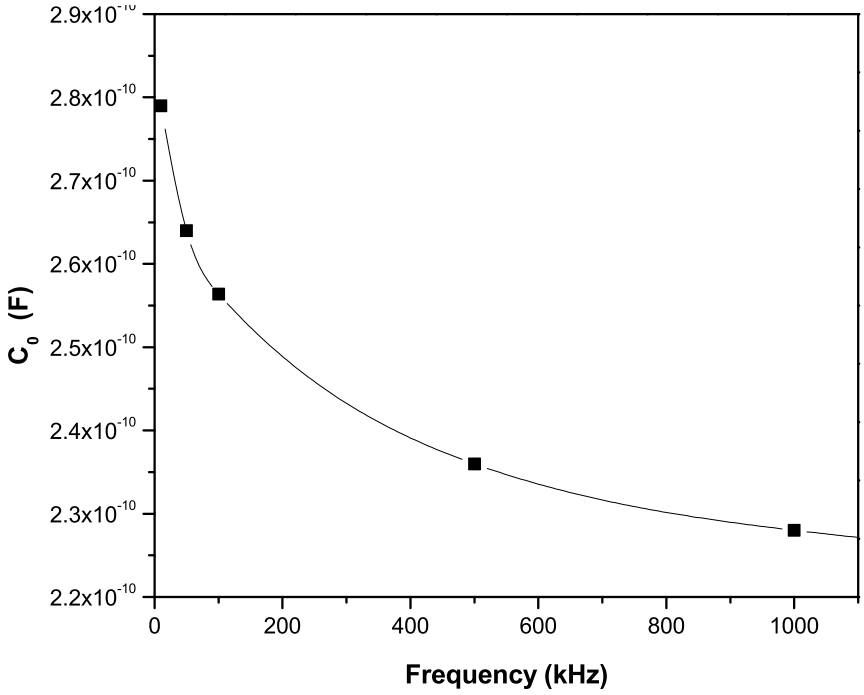

Figure 4.31: The variation of capacitance as a function of frequency at zero bias.

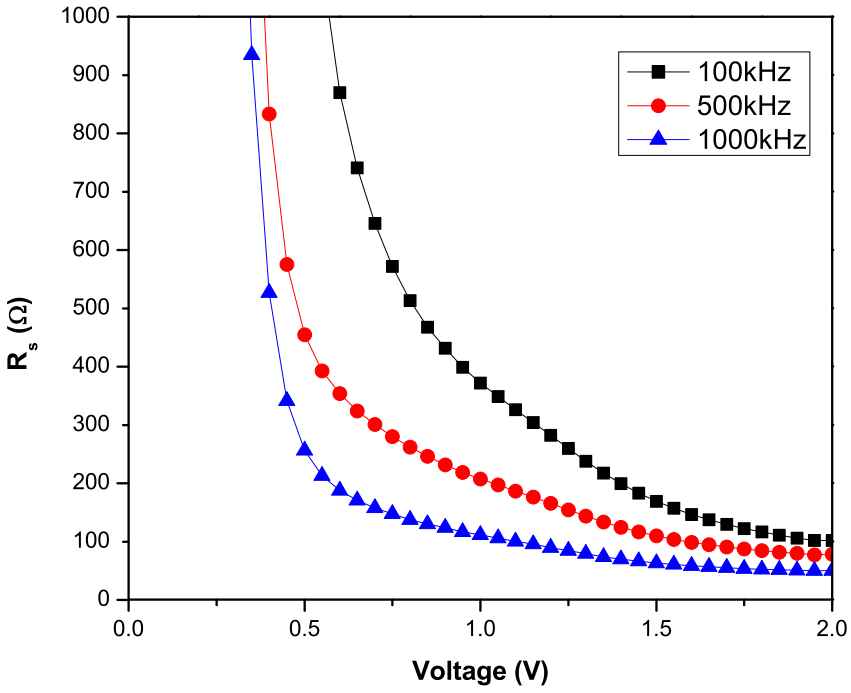

Figure 4.32: Series resistance-Voltage plot of n-Si/p-AIS heterojunction at room temperature for different frequencies.

4.3.3 Spectral Response Characteristics of n-Si/p-AIS Heterostructure Devices

Spectral photo-response measurements were carried out for the light incident through the AIS layer in the wavelength range of 400-1300 nm at room temperature. As can be seen from Fig.4.33, the photocurrent spectra of these devices lie in the range of 480-1170 nm.

As can be seen in Fig.4.33, the band edges were found to be around ≃680nm and ≃1100nm. Higher wavelength side of the photoresponse spectra gives nearly the silicon band gap ($1100nm \simeq 1.13eV$) and the main photoresponse peak (920nm) corresponds to p-AIS thin films band gap value as 1.35 eV as similar to literature [73]. This band gap value exactly match with the incoming solar photon maxima.

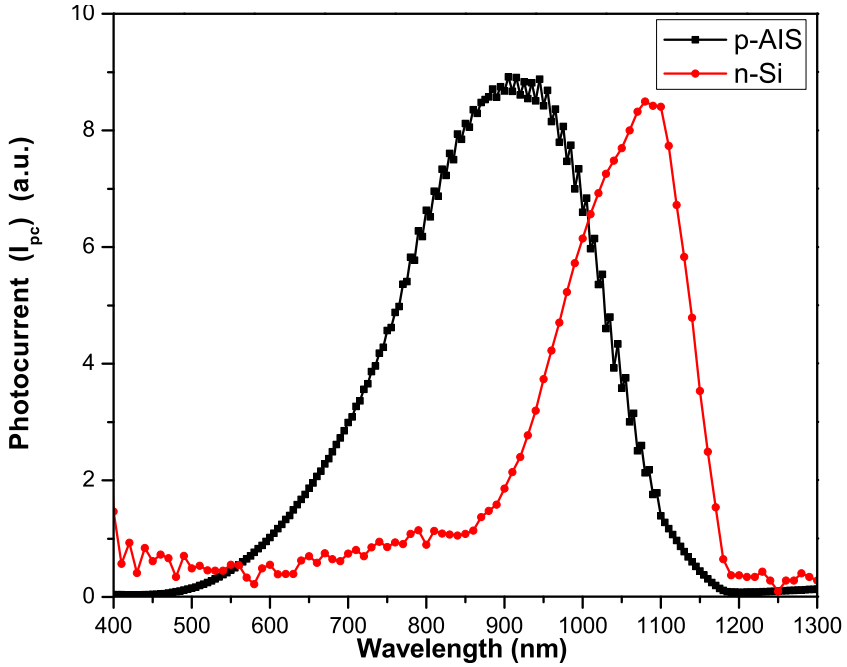

Figure 4.33: Photocurrent vs. wavelength graph of n-Si/p-AIS heterojunction at room temperature.

4.3.4 Current-Voltage Characteristics of the n-Si/p-AIS Heterostructure Devices Under Illumination

The photovoltaic behavior of the n-Si/p-AIS heterojunction were studied as explained in chapter 3 under simulated AM1 conditions ($\sim 100\ mWcm^{-2}$) at room temperature. Illuminated current-voltage characteristic of the n-Si/p-AIS structure is given in Fig.4.34.

As seen from the current-voltage plot under illumination, series resistance decreases the fill factor of the device. Short circuit current and open circuit voltage were obtained from illuminated I-V measurement as $I_{sc} = 2.67 \times 10^{-3}\ Acm^{-2}$ and $V_{oc} = 0.24\ V$, respectively. Calculated maximum current, maximum voltage and fill factor of device were $I_m = 1.23 \times 10^{-3}\ Acm^{-2}$, $V_m = 0.11\ V$ and $FF = 0.21$, respectively. I_m and V_m values of the device obtained by sputtering method were higher than I_m and V_m value of thermally evaporated devices. However, the calculated efficiency of the devices obtained by sputtering method was still $n = 0.13\%$ which is very low for solar cell application. High series resis-

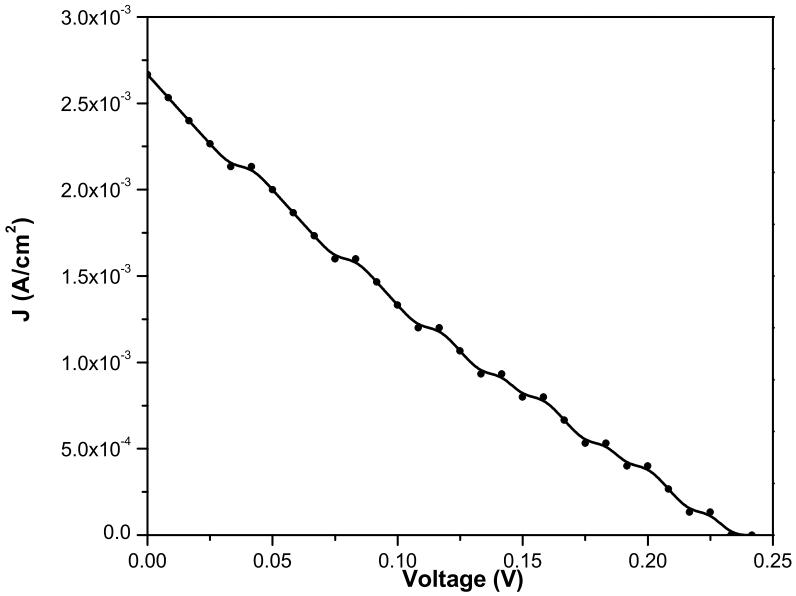

Figure 4.34: Current-Voltage characteristic under AM1 illumination for n-Si/p-AIS structure.

tance of the device and interface states density could be the reasons of this lower efficiency. Also, similar band gap value of the Si and AIS thin films lower the barrier height of the Si/AIS heterojunction and this results lower open circuit voltage.

CHAPTER 5

CONCLUSIONS

The aim of this work was to produce and characterize the device behaviors of the heterostructure made by Ag-In-Se (AIS) thin films.To deposit AIS films, thermal evaporation and RF/DC sputtering method were used. The structural properties of the films were examined by XRD analysis. After production of the devices; electrical and optical properties of the heterostructure were investigated by dark current-voltage, illuminated current-voltage, capacitance-voltage and spectral photo-response measurements.

Thermal Evaporation Method:

AIS thin films were deposited by thermal evaporation method on the Si wafers, glass and ITO coated glass substrate under high vacuum at the substrate temperature of 150^{o}C. XRD measurements showed that the as-grown films were amorphous in nature and after annealing with 200 and 300^{o}C under nitrogen atmosphere, the AIS films turn to the polycrystalline structure including $AgIn_5Se_8$ and $\delta - In_2Se_3$ multi-phases. The films have n-type conduction which was determined by hot probe technique.

In order to obtain device behavior, ITO/AIS/metal structures were produced by different metal contacts in circular shape and because of the different phases in structure and complex interface states of the junction, all metal made ohmic contact with AIS films except Au contacts. ITO/n-AIS/Au structure shows very good rectification factor of about 5 order in magnitude around 1V, but ideality factor of devices smaller than one which can be explain by Auger recombination in junction under high-level injection.

To produce p-n structure device, n-AIS films were deposited on p-Si wafers with Al back and In front contacts and Al/p-Si/n-AIS/In sandwich structure were obtained. In order to investigate rectifying behavior of the Al/p-Si/n-AIS/In devices, dark current-voltage measurements were carried out. The Al/p-Si/n-AIS/In devices shows very good device behavior with the rectification factor of about 4 orders of magnitude and n=2.47. The series resistance was calculated from the deviation of I-V slope from linearity as $R_s = 177\ \Omega$ that quite high for the solar cell applications. The high ideality factor of the diode corresponds to complicated transport mechanism at junction. To identify the transport mechanism of the junction, temperature dependent current-voltage measurement were carried out in the temperature range of 160-360 K. The analysis of the temperature dependent I-V characteristics suggested that the junction current was dominated by the combination of thermally assisted tunneling and interface recombination mechanisms. From the analysis of the frequency dependent C-V measurements, the built-in potential, effective carrier density and series resistance were found to be 0.91V, $2.9 \times 10^{15}\ cm^{-3}$ and 170 Ω, respectively and they were in good agreement with the values obtained from I-V analysis. In addition to C-V measurement, from the frequency dependence of the junction capacitance, interface states was calculate as $9.93 \times 10^{10} cm^{-2} V^{-1}$.

For optical characterization of the junction spectral photoresponse measurement carried out in the wavelength range of 500-1260 nm by changing the temperature of the sample in between 80 and 360 K. Photocurrent spectra of these devices lie in the range of 620-1170 nm and showed a maxima around 770nm (1.61 eV). The photoresponce maxima and general tendency of the photoresponce-wavelength plots showed that photocurrent spectra of the p-Si/n-AIS heterostructure are completely related with the AIS films. Also the band gap values obtained from transmission analysis and photocurrent peaks exactly match with literature. The wide spectral response wavelength range of the device which including the optimum photon energy value shows that the AIS films has good photoresponse performance for solar cell applications.

In order to see the solar cell conversion efficiency of the devices, illuminated

I-V measurements were carried out under AM1 conditions (100 $mWcm^{-2}$). Measured open circuit voltage and short circuit current of the device were 0.29 V and 9×10^{-5} Acm^{-2}, respectively. Calculated fill factor and the efficiency of the device were $FF = 32$ and $\eta = 0.1\%$. Because of the high series resistance of the devices (170 Ω) which calculated both I-V and C-V measurements increased the recombination of photogenerated charge pairs and decreased the fill factor and the conversion efficiency of the device.

To investigate annealing effect on the p-Si/n-AIS device behavior, heterostructure were annealed at 200, 240 and 280^{o}C under nitrogen atmosphere for 30 minutes. Similar to the structural changes by annealing, device properties also changed and resulted in decreases of the series resistance and interface states. Increasing the annealing temperature shifted the photoresponse main peak from AIS side to Si side. This shifting of main peak can be taken as the indication of decreasing the series resistance. Higher series resistance value of the AIS thin film causes the fully depletion of AIS side in the heterostructure. By decreasing the series resistance of the AIS films, Si side of the junction also contribute to the photoresponse and the depletion region is shifting to Si side. The series resistance was decreased from 170 Ω to 91 Ω and the solar cell conversion efficiency and fill factor of the devices increased up to $\eta = 2.6\%$ and $FF = 63$, respectively for 240^{o}C annealing of the sample.

RF/DC Sputtering Method:

AIS thin films were deposited on the Si wafers, glass and ITO coated glass substrate under high vacuum by RF/DC sputtering method. InSe and Ag targets were used for layer-by-layer sputtering. To get desired $AgInSe_2$ structure as-grown films were annealed under nitrogen atmosphere and selenium ambient at 300^{o}C for 30 minutes.

XRD measurements shown that the as-grown films were amorphous in structure and after annealing at 300^{o}C under nitrogen atmosphere, the AIS films turns to polycrystalline structure which including Ag and $AgInSe_2$ multi-phases. XRD measurements of the selenized structure at 300^{o}C showed that AIS thin films turned to mono-phase polycrystalline $AgInSe_2$ thin films with sharp XRD

peaks along (112) direction. The thickness of the films increased from $0.5\mu m$ to $1\mu m$ with the Se penetration resulted in $AgInSe_2$ single phase which has lower density value. The selenized AIS films have p-type conduction which was determined by hot probe technique. Thermal evaporated AIS films has n-type conduction because of the silver and selenium deficiency in the structure. This conduction type was changed to p type in sputtered AIS thin films by introducing the enough silver anion with layer-by layer deposition and selenization (two stage process) which is similar to $CuInSe_2$ production process in literature.

To make heterostructure device, p-AIS films deposited on n-Si and p-Si wafers with Al back and In front contacts and Al/n-Si/p-AIS/In ($p-n$ junction) and Al/p-Si/p-AIS/In ($p-p^+$ junction) heterostructures were produced. In order to investigate rectifying behavior of the Al/p-Si/p-AIS/In devices dark current-voltage measurement were studied. The Al/p-Si/p-AIS/In devices has the rectification factor of about 2 orders of magnitude and n=2.35 diode ideality factor. The series resistance was also calculated from deviating from I-V curve slope as $R_s = 90\ \Omega$ that quite high for the solar cell device applications. Because of the lower diode properties of the junction solar cell efficiency of the devices was below 1%.

To understand the diode properties of the Al/n-Si/p-AIS/In heterostructure, dark current-voltage measurements were carried out and ideality factor saturation current and series resistance value calculated as $n = 1.5$, $I_0 = 4 \times 10^{-11} A$ and $Rs = 80\Omega$, respectively. The ideality factor lying between one and two indicates that in the junction primarily diffusion current rather than generation/recombination current in the depletion region. The Al/n-Si/p-AIS/In structure shows very good diode properties with the rectification factor of about 6 orders of magnitude about 1V at room temperature.

The capacitance-voltage measurements also carried out for Al/n-Si/p-AIS/In heterostructure for different frequencies at room temperature. From analysis of the frequency dependent C-V measurements built-in potential and carrier concentration calculated as $V_b = 0.65\ V$ and $N_d = 8.79x10^{15}\ cm^{-3}$, respectively. Interface states density was calculated by frequency dependence of the zero bias

capacitance values as $N_{ss} = 2.1 \times 10^{12} cm^{-2} V^{-1}$ which is higher then thermal evaporated AIS heterostructures. The series resistance of device was obtained from measured capacitance and conductance in strong accumulation region at high frequencies as $\simeq 79\Omega$ which was almost the same value extracted from I-V plot.

Spectral photo-response measurements were also carried out for Al/n-Si/p-AIS/In heterostructure in the wavelength range of 400-1300 nm at room temperature. The photocurrent spectra of these devices lie in the range of 480-1170 nm which is wide enough for solar cell application. The device photoresponse started at 1100nm which is around Si band gap and the main photoresponse peak was at 920nm corresponds to p-AIS thin films band gap value as similar to literature. This main peaks exactly match with solar photon maxima with high absorbtion coefficient imply that p-AIS films are good candidate material for solar cell applications.

The photovoltaic behavior of the n-Si/p-AIS heterojunction were studied under simulated AM1 conditions ($\sim 100\ mWcm^{-2}$) at room temperature. Short circuit current and open circuit voltage was obtained from illuminated I-V measurement is $I_{sc} = 2.67 \times 10^{-3}\ Acm^{-2}$ and $V_{oc} = 0.24\ V$, respectively. Calculated maximum current, voltage and fill factor of device is $I_m = 1.23 \times 10^{-3}\ Acm^{-2}$, $V_m = 0.11\ V$ and $FF = 0.21$, respectively. Although the n-Si/p-AIS heterojunction had good photoresponse behavior, fill factor and efficiency values were low. High series resistance and interface states density could be the reason of this lower efficiency of the devices.

In this work, different deposition method and post deposition techniques were investigated for Ag-In-Se thin films. The problems have been encountered in device production eliminated by changing production method and annealing techniques. The AIS films showed very good diode properties and rectifying values. Also photoresponse measurements showed that AIS films has acceptable photoresponse properties and the band gap of the samples is lying in the maximum solar radiation region. Layer-by-layer sputtering deposition eliminates the silver deficiency of the films. Also, two stage process (selenization) overcome

the selenium degradation in the structure and desired p-type $AgInSe_2$ thin films were produced. With optical, electrical and structural properties of the p-type $AgInSe_2$ thin films could be used as solar cell absorber layer with an appropriate window layer, such as CdS. The $p-AgInSe_2/n-CdS$ heterostructure for solar cell application is going to be the future work of this study.

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