DESIGN AND IMPLEMENTATION OF LOW PHASE NOISE PHASE LOCKED LOOP BASED LOCAL OSCILLATOR

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ABSTRACT

DESIGN AND IMPLEMENTATION OF LOW PHASE NOISE PHASE LOCKED LOOP BASED LOCAL OSCILLATOR

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In this thesis, a low phase noise local oscillator operating at 2210 MHz is designed and implemented to be used in X-Band transmitter of a LEO satellite. Designed local oscillator is a PLL (Phase Locked Loop) based frequency synthesizer which is implemented using discrete commercial components including ultra low noise voltage controlled oscillator and high resolution, low noise fractional-N synthesizer. Operational settings of the synthesizer are done using three wire serial interface of a microcontroller. Although there are some imperfections in the implementation, phase noise of the prototype system is pretty good which is measured as -123.2 dBc/Hz at 100 kHz offset and less than -141.3 dBc/Hz at 1 MHz offset.

Made up of discrete components, the VCO used in the designed local oscillator is not integrable to frequency synthesizer which is implemented in CMOS technology. Considering technological progress, integrabilitiy of system components becomes important for designing single chip complete systems like transmitters, receivers or transceivers. Therefore considering a potential single chip transceiver production, also a CMOS voltage controlled oscillator is designed using standard TSMC 0.18um technology operating in between 2.05 GHz and 2.35 GHz . Since low phase noise is the main concern, phase noise models and phase noise reduction techniques that are derived from the models are studied. These techniques are applied to the VCO core to see the effects. Design is finalized by applying

some of those techniques which are found to be noticeably effective to the core design. Finalized core operates from 2.15 GHz to 2.25 GHz and phase noise is simulated as -107.265 dBc/Hz at 100 kHz offset and -131.167 dBc/Hz at 1 MHz offset. Also oscillator has figure of merit of -185.4 at 100 kHz offset. These values show that designed core is considerably good when compared to similar designs.

Keywords: PLL, Low Phase Noise, VCO, CMOS, Frequency Synthesizer

ÖZ

DÜŞÜK FAZ GÜRÜLTÜLÜ FAZ KİLİTLEMELİ DÖNGÜ TABANLI YEREL OSİLATÖR TASARIMI VE GERÇEKLEŞTİRİMİ

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Bu tezde, alçak yörünge uydusunun X-Bant vericisinde kullanılmak üzere düşük faz gürültülü yerel osilatör tasarımı ve gerçekleştirimi anlatılmıştır. Tasarlanan yerel osilatör PLL (faz kilitlemeli döngü) tabanlı frekans bireştirici yapısındadır. Bu yapıda çok düşük faz gürültülü gerilim kontrollü osilatör ve yine düşük gürültülü yüksek çözünürlüklü fraksiyonel N bireştiriciyi de içeren ayrık elemanlar kullanılmıştır. Yapının çalışma ayarları mikroişlemcinin seri kanalı kullanılarak yapılmıştır. Gerçekleştirmede bazı eksikler olmasına rağmen ön ürünün faz gürültü performansı oldukça iyi ölçülmüştür. Ölçülen değerler 100 kHz ofsette -123.2 dBc/Hz'dir. 1 MHz ofsette ise -141.3 dBc/Hz'den daha düşük bir seviyededir.

Tasarlanan yerel osilatörde kullanılan gerilim kontrollü osilatör çok düşük faz gürültüsüne sahip olmasına rağmen ayrık parçalardan oluşan, sentezöre entegre olamayan bir yapıdır. Teknolojik gelişim göz önünde bulundurulacak olursa, sistem bileşenlerinin kolaylıkla entegre olabilmesi alıcı, verici ya da alıcı-verici yongalarının tasarlanabilmesi açısından önemlidir. Bu durum düşünülerek bu tezde, yapılması muhtemel tek yonga alıcı-verici için TSMC 0.18 um CMOS teknolojisi kullanılarak 2.05 GHz – 2.35 GHz arasında çalışabilen CMOS sentezör yapılarına entegre olabilecek bir VCO tasarımı da yapılmıştır. Yapının düşük faz gürültülü olması amaçlandığı için faz gürültüsü modelleri ve bu modellerden çıkarılan faz gürültüsü azaltma teknikleri çalışılmış, bu teknikler tasarlanan VCO yapısına uygulanmış ve etkileri gözlenmiştir. Tasarım, bu tekniklerin belirgin etkisi olan birkaçının

ana yapıya uygulanmasıyla bitirilmiştir. Sonlandırılan ana yapı 2.15 GHz'ten 2.25 GHz'e kadar çalışmakla beraber faz gürültüsü 100 kHz ofsette -107.265 dBc/Hz ve 1MHz ofsette -131.167 dBc/Hz olarak simüle edilmiştir. Bunun yanında 100 kHz offsette başarım ölçüsü -185.4 olarak hesaplanmıştır. Bu değerler tasarlanan ana yapının benzer tasarımlara göre oldukça iyi olduğunu göstermektedir.

Anahtar Kelimeler: Faz Kilitlemeli Döngü, Düşük Faz Gürültüsü, Gerilim Kontrollü Osilatör, CMOS, Frekans Bireştirici

To my family

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LIST OF ABBREVIATIONS

CAD	:	Computer Aided Design
CP	:	Charge Pump
DRO	:	Dielectric Resonator Oscillator
FOM	:	Figure Of Merit
LFCSP	:	Lead Frame Chip Scale Package
LTV	:	Linear Time Variant
MIM	:	Metal-Insulator-Metal
NTI	:	Nonlinear Time Invariant
PCB	:	Printed Circuit Board
PFD	:	Phase Frequency Detector
PLL	:	Phase Locked Loop
SSCR	:	Single Sideband to Carrier Ratio
TCXO	:	Temperature Compensated Crystal Oscillator
VCO	:	Voltage Controlled Oscillator
VPD	:	Voltage Phase Detector

CHAPTER 1

INTRODUCTION

Local oscillators are used in communication systems for frequency up conversion or down conversion purposes. For a stable communication system, performance dependence of local oscillators to the environmental conditions should be minimized. Known stable oscillator structures, i.e. crystal oscillators cannot exceed MHz levels and are not sufficiently high for today's frequency limits. Therefore local oscillators are generally implemented as frequency synthesizers that are electronic structures which can generate oscillations at different ranges of frequencies using a reference stable oscillator. This reference is usually a crystal oscillator. Frequency synthesizer operation may include frequency division, multiplication and mixing to obtain desired frequency output.

There are different types of frequency synthesizers like direct analog synthesis (DAS), direct digital synthesis (DDS), delay-locked loop (DDL) and phase-locked loop (PLL). Among these structures PLLs are widely used in RF applications due to their satisfactory performance, easy integration and reasonable power consumption [1]. The first PLL which is a vacuum tube circuit was proposed by Henri de Bellescize in 1932. Then improved versions are used in TV line and frame synchronization, local oscillators in FM receivers, data synchronization in PC applications, i.e. hard disks, modems and tape drivers. Today largest application area of PLLs is mobile phones in which they serve as frequency synthesizers [10].

When using PLL as local oscillator in communication systems, phase noise becomes critical. Phase noise can be simply expressed as noise power in 1 Hz band at $\Delta\omega$ offset from the carrier divided by the carrier power and gives a measure of short term stability of the oscillator. If phase noise is at a significant level, i.e above the standards of the application adjacent channel distortion becomes an issue. In modern wireless communication systems, channel spacing can be as narrow as few hundred kHz while the carrier frequencies may go

up to GHz levels. Under these circumstances phase noise may have destructive effects. Above a certain frequency, phase noise of PLL follows voltage controlled oscillator which is the most critical component giving the system output. Therefore, for a low noise system also a low noise VCO is needed.

In this thesis work, low noise PLL based local oscillator is designed, simulated and implemented. Also a low phase noise CMOS voltage controlled oscillator is designed and simulated.

Thesis is organized as seven chapters. Firstly, in Chapter 2, phase locked loop theory is discussed in detail. At the beginning of this chapter PLL overview, operation principle and building blocks of the charge pump PLL which is most widely used structure is explained. Following these, principles and usage of fractional- N synthesizers which allow division rates to be fractional values and Σ-Δ modulators that eliminate fractional spurs with increasing order are explained. After detailing spurious types in PLLs, chapter is finished with phase noise modeling and loop filter design subjects.

Chapter 3 is allocated to work covering design, simulation and implementation of PLL based local oscillator that is to be used in an X-band transmitter. CAD based design and simulations are done using Applied Radio Labs' ADISim v3.1 software. In the design discrete commercial components are used therefore specifications and characteristics of these components are defined in the simulation environment and designed loop filter is optimized to get best phase noise performance without deteriorating lock time performance much. Then system is realized on the PCB using commercial off the shelf components. In this chapter simulation and measurement results are illustrated.

In Chapter 4, theory of oscillators including basic concepts, oscillator types, oscillator models, voltage controlled oscillator and CMOS differential VCO design are discussed. Since differential LC oscillators are superior to others in terms of phase noise performance, the chapter is finished by giving building blocks of cross coupled differential VCO design.

Chapter 5 is devoted to phase noise in voltage controlled oscillators. In this chapter first noise sources in electronic systems and phase noise phenomenon are discussed. Second, commonly used phase noise models which are Leeson's model, linear time variant model and nonlinear time invariant model are explained. At the end of the chapter phase noise reduction techniques are reported.

Making use of background information on VCO design, in Chapter 6, a CMOS cross coupled VCO operating in between 2.15 GHz and 2.25 GHz is designed using CAD tool Agilent's ADS 2008. Then phase noise reduction techniques which are detailed in Chapter 5 are applied to designed structure to see the effects. After the evaluation of the performance of these techniques design is finalized by reducing VCO gain and using resistor tail biasing. Simulation results for all VCOs with different phase noise reduction techniques and also finalized core are reported in this chapter.

Presentation of the thesis is completed by the conclusion chapter in which summary of work done together with remarks on important points especially on phase noise is given.

CHAPTER 2

PHASE LOCKED LOOP THEORY

In this chapter, PLL structure is discussed in detail. Discussions include technological development, operation principles, theoretical analysis, building blocks and parameters of PLL's. First a general overview of PLL with generic building block is given. Then the theory of operation of charge pump PLL is summarized. After that, the building blocks of charge pump PLLs are investigated in detail. Following that, the principals of most popular PLL type, fractional-N PLL are examined. Then spurs of PLL with the reduction mechanisms are given, phase noise of PLLs are explained and finally loop filter design is summarized. After these discussions, PLL design and implementation using Analog Devices' ADF4157 will be explained in detail including the phase noise measurements.

2.1 PLL Overview

Phase locked loop is simply a feedback system that synthesis and stabilizes the desired frequency output using stable reference oscillator. Simple block diagram is shown in Fig. 2.1.

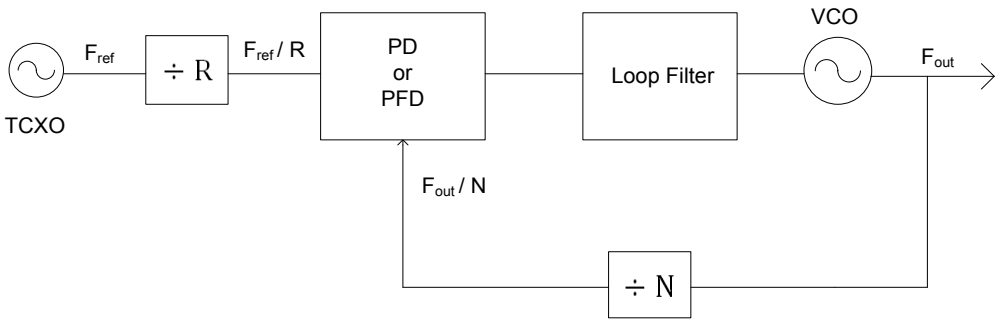


Figure 2.1 : Simple block diagram of a PLL

PLL operation is technology dependent but basically R counter divides the reference frequency by R and N counter divides the output frequency by N. These divided signals are compared at the phase-frequency detector. PFD outputs a DC value which is proportional to the phase-frequency difference of the compared signals and high frequency components. Loop filter which has low-pass characteristics, eliminates the high frequency components and DC value is fed to the control voltage input of the voltage controlled oscillator. According to the control voltage, VCO frequency changes and system is stabilized when no phase-frequency difference remains between compared signals. When the system is stabilized output frequency can be expressed as in (2.1). If a different operation frequency is required N counter should be programmed accordingly.

$$F_{out} = \frac{N}{R} F_{ref} \tag{2.1}$$

If N and R values are assumed to be integers channel spacing (frequency resolution) is equal to the PFD frequency which is F_{ref}/R. This type of PLL is named as integer-N PLL. For a fractional-N PLL, N value can be fractional so we have channel spacing less than PFD frequency. Generally N is selected to be as low as possible for optimum noise performance and in this case PFD frequency is considerably high.

In earlier analog and digital PLLs, mixers [2] and simple XOR gates [3] are used as phase detector respectively. These devices are generally known as voltage phase detectors (VPDs) and have voltage output which is proportional to phase-frequency difference. Main problems of those structures are that they cannot sense and track whole phase-frequency differences so, they have limited lock-in and hold-in ranges. To improve the ranges, active loop filters are necessary to use with VPDs. Active filters also help matching VPD output voltage range to the VCO control voltage range but they add extra noise, cost and complexity to the structure. Note that there are still some studies which use these types of phase detector.

In today's technology, state machines consisting of D or JK type flip-flops and charge pumps are used as phase-frequency detectors [1]. These structures have current output proportional to phase-frequency difference and main advantage is that they can sense all phase-frequency differences. Since charge pumps do not have lock-in or hold-in range problems passive loop filters, which can be modeled as impedance converting current to the voltage, are generally

sufficient for satisfactory performance. In the following sections, charge pump PLLs will be analyzed in detail.

2.2 Charge pump PLL operation

Charge pump PLL operation principle is directly related with PFD operation. Basic block diagram is shown in Fig. 2.2. Implementation details of the components will be given later but in this part only operation is shown.

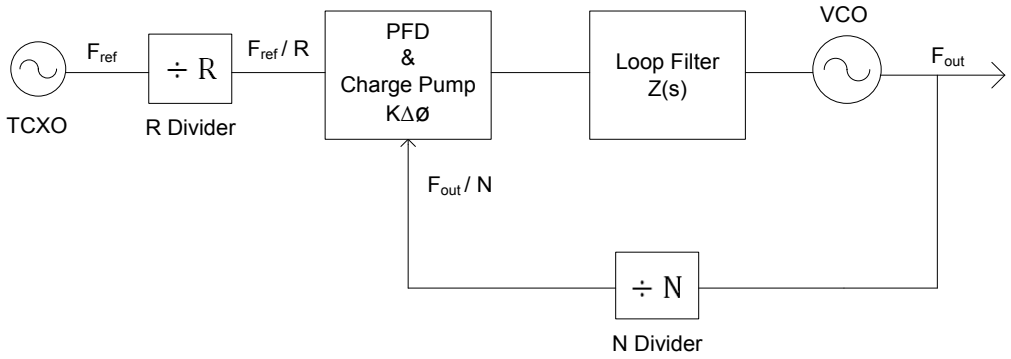


Figure 2.2 : Charge pump PLL block diagram

In the figure, PFD and charge pump are shown as one block since their operations are interrelated. CP-PLL generally starts with temperature-compensated crystal oscillator (TCXO). As is the case in all PLLs, TCXO frequency divided by R and output frequency divided by N are compared in the PFD. As stated in the previous part, PFD is a type of state machine and generally sensitive to the rising edges of the compared signals. As shown in the generic state diagram in Fig. 2.3, PFD has three states namely high-Z, current source and current sink. At the beginning the device is in high-Z. When rising edge of Φ_R is encountered, PFD jumps to the current source state. While sourcing current if rising edge of Φ_N is encountered device returns back to the high-Z otherwise current sourcing operation continues. In the high-Z mode if rising edge of Φ_N is encountered PFD starts sinking current and operation is similar to the current sourcing case. Note that in all these acts, positive polarity is assumed for the VCO which means that VCO frequency increases with control voltage. If polarity is changed operation should be reversed. When compared signals' phases are matched, PFD is in stability. Therefore it is in high-Z mode in which it is neither sourcing nor sinking current.

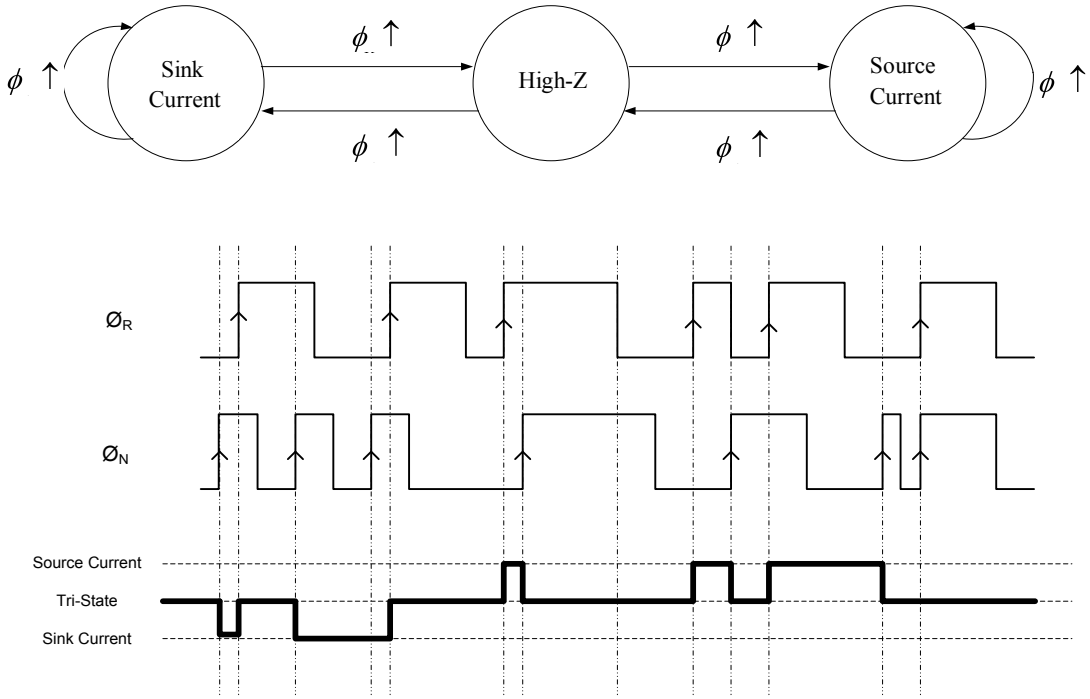


Figure 2.3 : Generic state diagram and operation of PFD

In practice, PFD has spurious output at integer multiples of its comparison frequency for integer-N PLLs and also at fractions in fractional-N PLLs. Details of these spurs will be discussed in later sections. Loop filter, which has low pass characteristic, is used to eliminate these spurs output, especially integer spurs, so that they do not cause spurious frequencies or AM-PM distortion at VCO output. At the output of the filter a clean DC value, corresponding to a frequency increase or decrease, is fed into the VCO control voltage. In stability filter output is the required DC voltage and finally desired frequency output is got from the structure. In the following section, building blocks of the PLL will be discussed in detail.

2.3 Building Blocks of PLL

2.3.1 Phase / Frequency Detector

As mentioned previously, PFD is generally implemented as state machines consisting of D flip-flops combined with the two-transistor charge pump structure as shown in Fig. 2.4. D inputs of flip-flops are connected to “high” and clock inputs are coming from compared signals. When Φ_R rising edge is encountered, upper flip-flop turns on the PMOS transistor, so current sourcing begins. While sourcing current if rising edge of Φ_N is seen, flip flops are

cleared, both transistors turn off and output becomes high-Z otherwise current sourcing operation continues. Reverse situation is the same but this time NMOS transistor is active and there is current sinking instead of current sourcing.

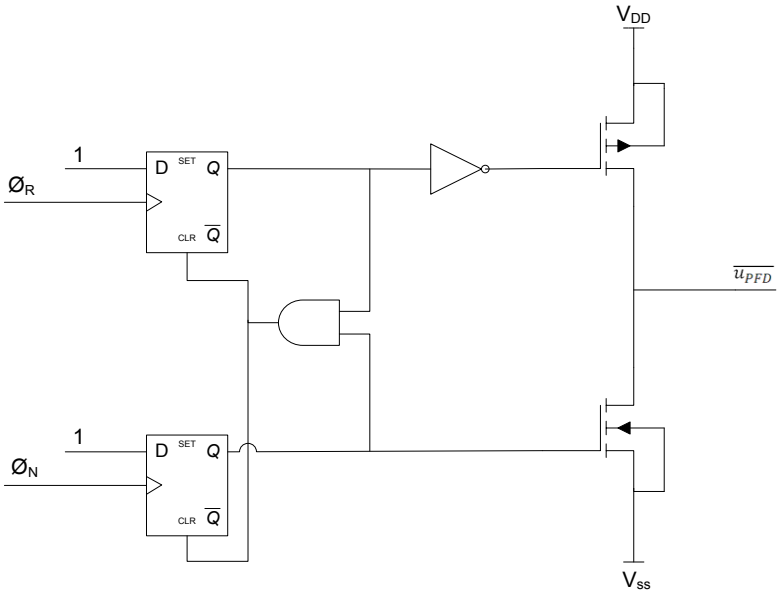


Figure 2.4 : Schematic diagram of PFD

In PFD, there are three modes of operation. When $\Delta\Phi$ is greater than $\pm 2\pi$, device is in frequency detect mode and it is continuously sourcing or sinking current depending on which singal's frequency is higher. When $\Delta\Phi$ is less than $\pm 2\pi$, device is in phase detect mode. In this mode charge, pump is active only for a portion of the cycle which is determined by the phase difference. At the stable point, $\Delta\Phi$ is zero and PFD is in phase-frequency locked mode. In this mode, output is at high-Z. PFD output waveform for a certain phase error is shown in Fig. 2.5[4].

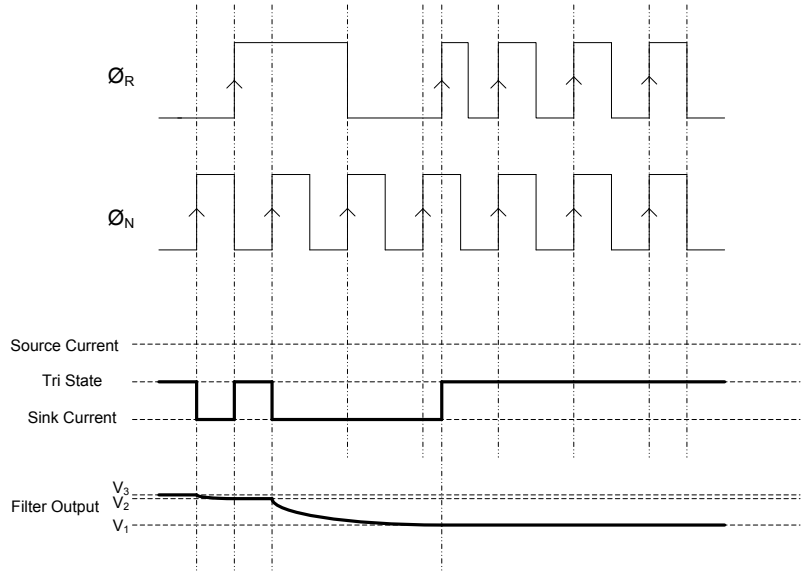


Figure 2.5 : PFD output waveform

If we plot average output signal $\overline{u_{PFD}}$ from PFD versus phase error ΔΦ, we obtain a sawtooth waveform shown in Fig. 2.6. When phase error is in between -2π and 2π, output is a linear function of phase error.

$$\overline{u_{PFD}} = K\Delta\Phi \tag{2.2}$$

K is the PFD gain. When phase error is greater than 2π or smaller than -2π, PFD operates as phase error is recycled to zero so, characteristic curve of PFD is periodic with 2π [5].

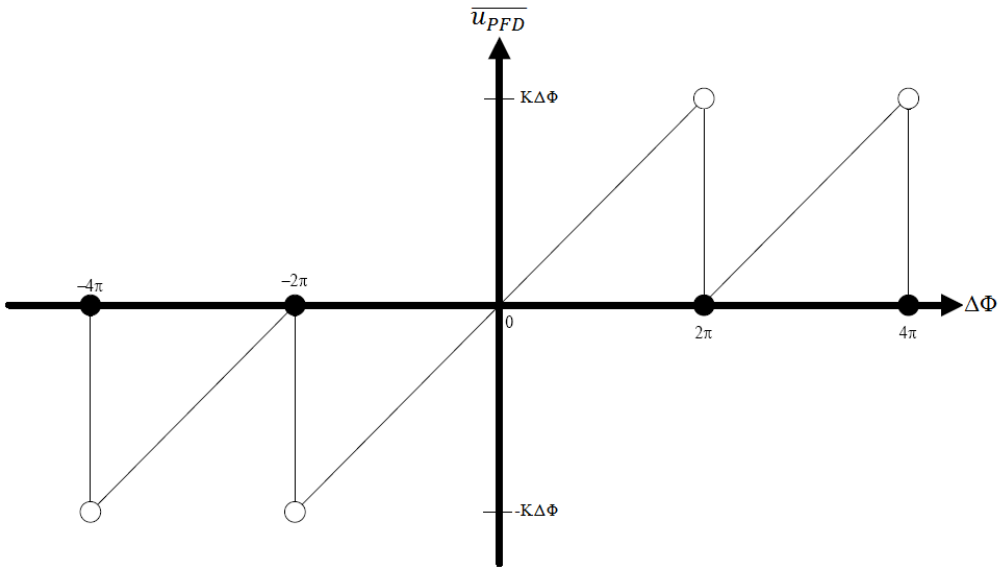


Figure 2.6 : Characteristic curve of PFD

2.3.2 Loop Filter

Output of the phase detector consists of a dc term which is proportional to the phase error and some high frequency components. Since the higher frequency terms create disturbance they are filtered out by the low pass loop filter. Active or passive filters can be used as loop filter. Main topologies of these filters are given in Fig. 2.7. In old fashioned PLLs active filters are mainly used for the improvement of lock-in and hold-in ranges [6]. They also help matching the voltage swings of phase detector and VCO. In charge pump PLLs, since there are no lock-in or hold-in range problems, passive filters are generally satisfactory assuming that there are no mismatches in the voltage swings. In today's technology especially in low noise applications, designs are made such that there is no need for active filters since active devices increase cost, complexity and noise. Details of loop filter design will be discussed at the end of this chapter.

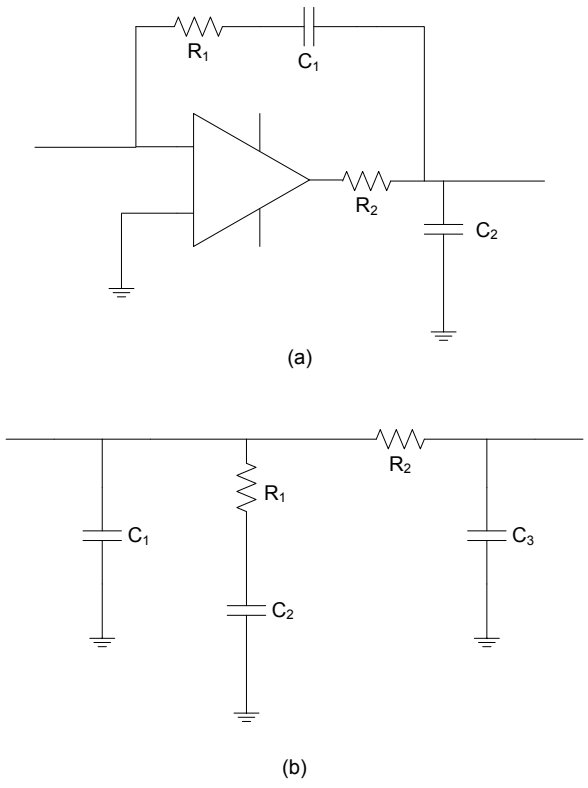


Figure 2.7: (a) Active loop filter (b) passive loop filter

2.3.3 Frequency Divider

For low frequencies i.e. less than 200 MHz, digital counters are used as frequency divider but CMOS counters have difficulties in handling high VCO frequencies so, prescalers are generally employed in front of the counter to reduce the frequency to the levels that the counters can easily work with [6]. Dividers are classified according to prescaler modulus. Common types are single modulus, dual modulus and quadruple modulus prescalers.

2.3.3.1 Single Modulus Prescaler

As shown in Fig. 2.8 single modulus prescaler consists of a fixed value prescaler and a counter. Counter is programmed to "*c"* and prescaler value is *P*. Division rate is calculated as $N = c.P$ and can be changed by changing counter value *c*. Disadvantage of this structure is that only integer multiples of *P* can be obtained as division rate.

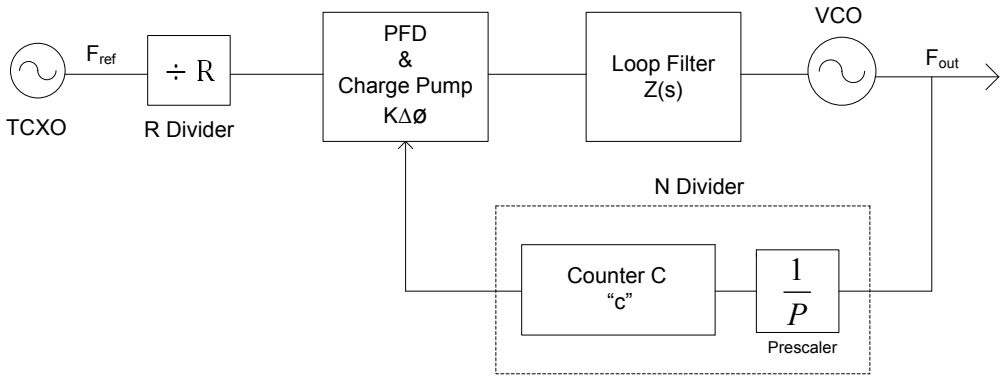


Figure 2.8 : Single modulus prescaler

2.3.3.2 Dual Modulus Prescaler

In order to increase division resolution, dual modulus prescalers as shown in Fig. 2.9 are employed. Actually, in the structure there is one prescaler *P,* and *P+1* is obtained by adding pulse swallowing function in front of it [6]. A and B counters start at the same time and firstly *P+1* prescaler is active for *a* cycles. After *a* cycles, *P* prescaler sets in for the remaining *b-a* cycles. Finally we get a division ratio in (2.3) which shows that division resolution increases.

$$N = a.(P + 1) + (b - a).P = P.b + a \tag{2.3}$$

One restriction for the operation is that *b* value should be greater than or equal to *a* value. This restriction reflects as a minimum division ratio. For example in a $P/P+1 = 8/9$ prescaler, maximum value of *a* is *seven (P-1)*. In consequence minimum *b* is *seven* which gives a minimum division ratio of 56.

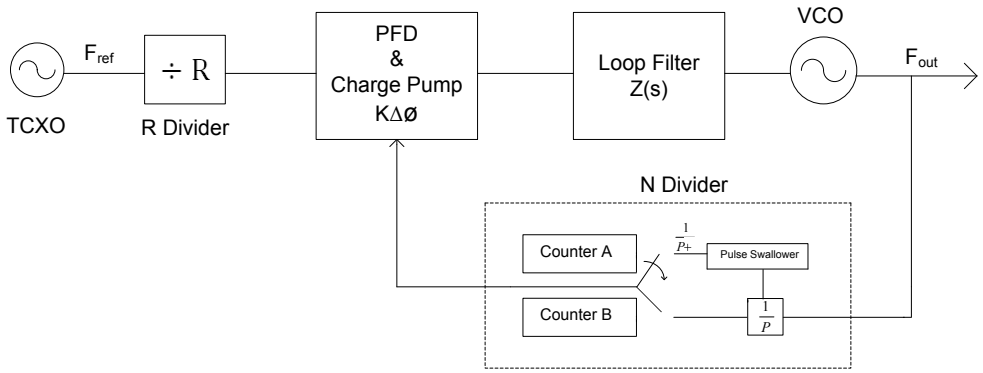


Figure 2.9 : Dual modulus prescaler

2.3.3.3 Quadruple Modulus Prescaler

Minimum division rate is an important concept for the divider. Especially in fractional-N structures from the noise point of view N value is selected as low as possible for minimum phase noise. Importance of minimum division rate will be discussed in detail later in phase noise modeling part. Therefore, for the improvement of minimum division rate and also for increasing range of N, quadruple or higher modulus prescalers are used. Quadruple structure is shown in Fig. 2.10. Working principle is very similar to dual modulus case. This time there are three counters associated with three prescaling operators. *P+4* and *P+5* are implemented using pulse swallowing function *P+1* as in the dual modulus case. All counters start at the same time. *P+5* prescaler is active for *a* cycles, *P+4* is active for *b-a* cycles and *P* is active for *c-b* cycles. Finally we obtain N as given in (2.4).

$$N = a.(P+5) + (b-a).(P+4) + (c-b).P = P.c + 4b + a \qquad (2.4)$$

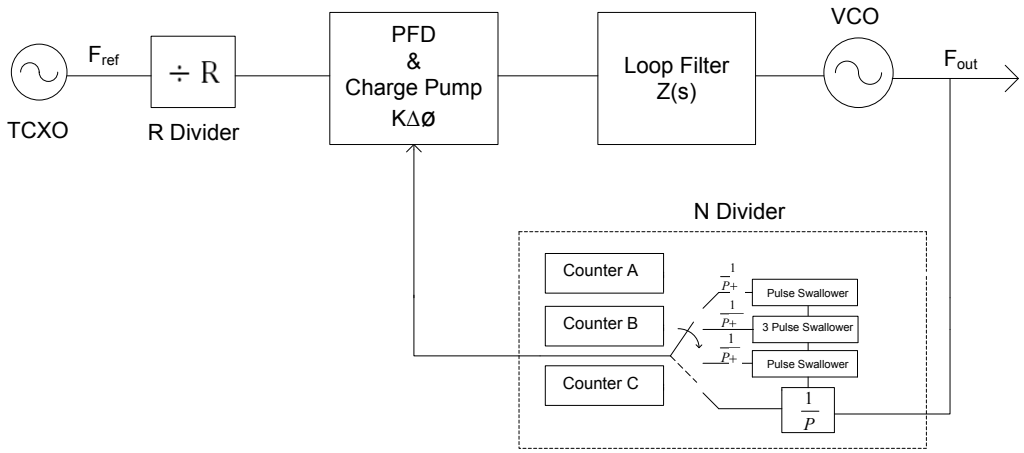


Figure 2.10 : Quadruple modulus prescaler

For legal division ratios *c* should be greater than *max{a,b}*. In this case there is no restriction on *a* or *b*. Depending on which one is smaller, counters associated with *P+5* and *P+4* prescalers can be interchanged. Doing some simple calculations, for a *P/(P+1)/(P+4)/(P+5)* prescaler minimum division rate is calculated as $(P \cdot max\{P/4-1, 3\})$ [1]. In order to compare this with dual modulus one, consider *8/9/12/13* prescaler which has minimum division rate of 24. As we can see minimum division rate is decreased. At the same time maximum division rate is also increased.

2.3.4 Voltage Controlled Oscillator

In a PLL structure, voltage controlled oscillator is the key component which provides the desired frequency output. There are different types of oscillators but in RF applications resonator based oscillators are widely used. A typical VCO is shown in Fig. 2.11. Oscillation frequency is changed by changing voltage on the voltage variable capacitor that tunes the resonance frequency. Main working principle is that active device supplies the negative resistance that compensates resonator loss and provides stable oscillation.

Overall phase noise of the PLL strongly depends on the phase noise of the VCO which is very important for RF applications. Most important parameter for a low noise oscillator is Q factor of the resonator which is a measure of quality. For low phase noise, high Q resonators are desired. Another important parameter for low phase noise is tuning gain K_v (MHz/V) of the oscillator. Lower K_v means output frequency is less sensitive to changes in the control voltage and also the noise on it. By decreasing K_v, phase noise can be decreased but at the

same time operation band is made narrower. Depending on the application, an optimization is necessary. VCOs are analyzed in detail in the Chapter 4.

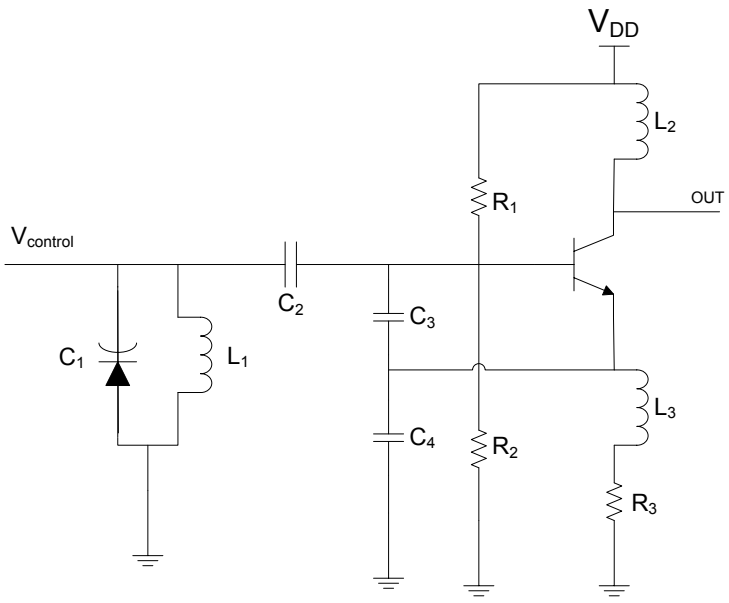


Figure 2.11 : A simple VCO

2.4 Fractional-N PLL

Earlier PLLs were integer N synthesizers in which division rate is an integer value. In such a structure channel spacing is determined by PFD frequency. Therefore if channel spacing is desired to be narrower, reference oscillator value is decreased and N divider value is increased. However increasing division rate degrades phase noise by $20\log(N)$. This will be discussed later in phase noise analysis section of this chapter. The way of keeping N small while decreasing channel spacing is using Fractional N synthesizers. In this type of structures N value can be adjusted to a fractional value which can be written as

$$N = N_{int} + \frac{F_{NUM}}{F_{DEN}} \tag{2.5}$$

where F_{DEN} is the fractional modulus which sets the channel spacing as F_{PFD}/F_{DEN}. All the calculations and theory of fractional structures are the same with integer N PLLs. Difference is in the implementation of division mechanism. Since there are no devices dividing by fractional values, fractional division is obtained by dynamically switching between at least

two integer values. In the simplest case divider is set to divide by *N+1* in F_{NUM} cycles and *N* in $F_{DEN} - F_{NUM}$ cycles. Therefore average division is obtained as given in (2.6).

$$N_T = \frac{(N+1)F_{NUM} + N(F_{DEN} - F_{NUM})}{F_{DEN}} = N + \frac{F_{NUM}}{F_{DEN}} \tag{2.6}$$

Remember from frequency dividers section that *P+1* prescaler is active for *a* counter cycles. After *a* cycles, *P* prescaler sets in for the remaining *b-a* cycles giving a total division of $P.b + a$. All we need to do is to increase a by 1 for F_{NUM} cycles. This is done with an accumulator as simply shown in Fig. 2.12. Accumulator counts F_{NUM} by F_{NUM} in F_{DEN} cycles. In one period of count a total of F_{NUM} carry outs occur. These carry outs command "*a counter"* value to increment by one. Therefore in F_{NUM} cycles, divider is set to N+1. Note that this example is given for dual modulus divider. Due to its improved range of division rate generally quadruple dividers are used in fractional structures [6].

In average desired N value is obtained however instantaneous divider value is incorrect. This instant phase error, which is illustrated in Fig. 2.13 for 1/5 fractional rate, creates fractional spurs at frequencies of channel spacing which can be troublesome if not eliminated. Since frequencies of these spurs are low, they generally fall into the loop bandwidth. Fractional spurs are the main disadvantage of fractional N synthesizers.

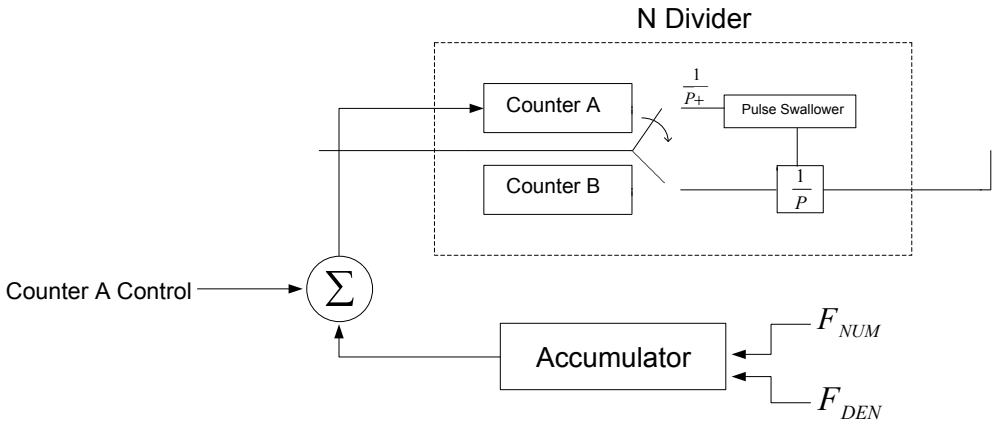


Figure 2.12 : Accumulator operation

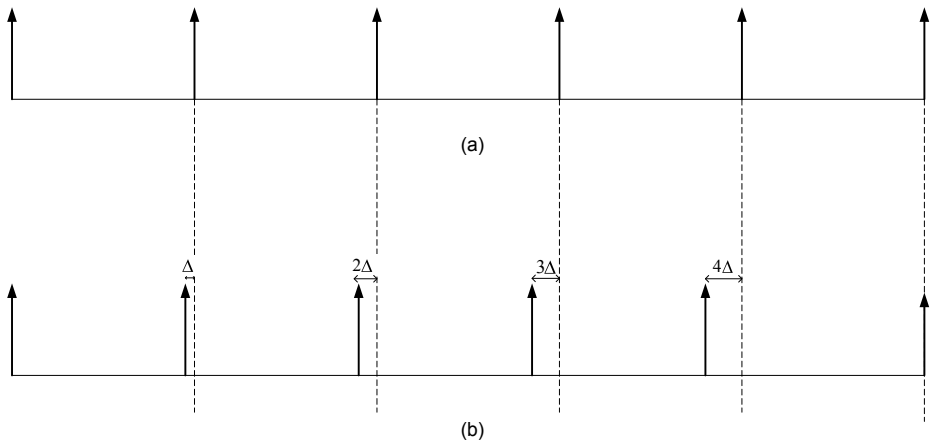


Figure 2.13 : (a) Desired divider output (b) phase error due to fractional divider operation for fraction of 1/5

For reduction of fractional spurs, there are several phase compensation techniques such as current injection, delay line control and DAC compensation. These techniques are known as analog techniques each having problems with process, temperature, voltage variations, extra phase noise and analog mismatch [6],[8]. More elegant way is using Σ-Δ Fractional-N PLL which makes compensation in digital domain.

2.4.1 Σ-Δ Fractional-N PLL

As stated before, alternating between two integers to obtain a fractional value in average is the basic logic behind fractional N synthesizers. This is actually first order Σ-Δ modulator which is a trivial one. Effective Σ-Δ modulators start with 2^{nd} order which alternates in between four integer values. An n^{th} order Σ-Δ modulator switches in between 2^n integers. Advantage of such a structure is that it eliminates the periodicity which creates fractional spurs by increasing possible number of instantaneous division rates. Therefore fractional spurs decrease with increasing modulator order. Another advantage is its noise shaping characteristic which pushes divider noise from low frequencies to higher frequencies so that it can be more easily eliminated by the loop filter [8].

Simplest Σ-Δ Modulator can be modeled with quantization error (instantaneous phase error) added to an ideal divider as shown in Fig. 2.14 where $E(z)$ represents quantization error and Z^{-1} in the feedback path models one clock cycle delay.

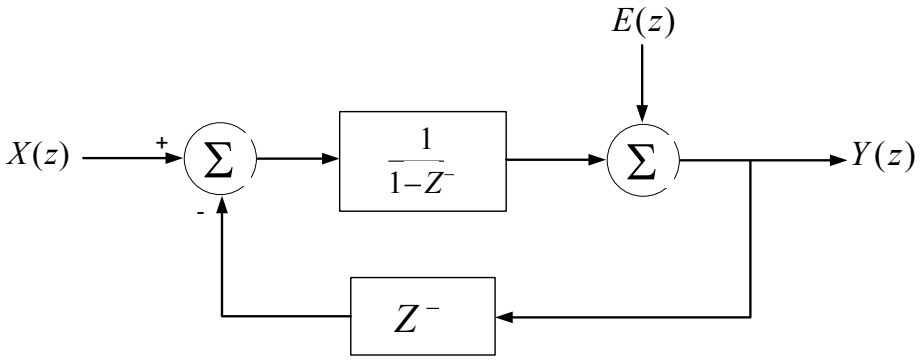


Figure 2.14 First order Σ-Δ modulator

Output function of this model can be easily calculated as:

$$Y(z) = X(z) + E(z)(1 - Z^{-1}) \tag{2.7}$$

This equation shows that previous value of phase error is subtracted from the present value and then reflected to the output which is actually a digital high pass filtering operation [6]. Similarly for an n^{th} order modulator general form of output can be written as given in (2.8).

$$Y(z) = X(z) + E(z)(1 - Z^{-1})^n \tag{2.8}$$

This equation implies that if modulator order is increased, quantization noise is pushed to higher frequencies to be filtered by the loop filter more easily. On the other hand Σ-Δ modulators may create spurs at fractions of channel spacing [1]. To eliminate these spurs a method using sequence randomizer can be used. This method is known as "dithering" which randomizes division rate sequence in a limited extend. Effect is reducing periodicity which reduces strong sub-fractional and fractional spurs in exchange for complexity and noise coming from the extra elements. This technique may be useful in some cases but may not in some other [8].

2.5 PLL Spurs

In PLL's spurious response is an important issue. Considering the causes of spurs there are several types.

2.5.1 Reference Spurs

First spur type is the reference spur which is observed at harmonics of the PFD frequency. Main causes of these spurs are leakage current and charge pump mismatch [6]. In locked operation charge pump is in tri-state. In this state there will be small parasitic leakage through charge pump which cause modulation on tuning line. In modern PLL's leakage currents are in the order of nano amps. Therefore it is not the dominant source of reference spurs. More problematic situation is charge pump mismatch. If current source and sink mechanisms have differences, there is a mismatch in the charge pump. Due to speed differences of PMOS and NMOS transistors current spikes occur at the frequency of PFD. If these spikes are not filtered, they develop ripple on the control voltage which has potential to cause FM modulation in VCO. These current spikes are illustrated in Fig. 2.15.

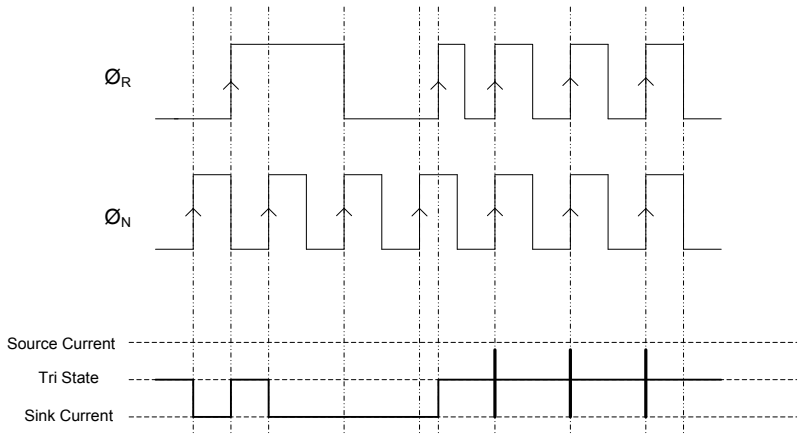


Figure 2.15 : Current spikes

In fractional-N PLL's reference spurs are not troublesome because they are easily filtered out by the loop filter. Advantage of fractional-N synthesizer is that PFD frequencies are fairly high. Therefore reference spurs are far outside the loop bandwidth which enables easy filtering. However these spurs have potential to bypass the filter therefore layout of the circuit should be carefully drawn to prevent any feed through mechanism.

2.5.2 Integer-N Boundary Spurs

Harmonics of the PFD frequency and VCO output frequency can interact in a PLL which lead integer-N boundary spurs. This interaction can be thought as crosstalk. These spurs are observed at offset frequencies which correspond to the difference of integer multiples of PFD frequency and VCO output frequency.

Integer-N boundary spurs are troublesome when output frequency is adjusted to be close to an integer multiple of PFD frequency [7]. Therefore they are problematic in integer-N synthesizers. In fractional-N case generally output frequency is away enough from an integer multiple of PFD frequency. So, they are generally eliminated by the loop filter.

2.5.3 Fractional Spurs

As mentioned in fractional-N synthesizers, fractional spurs show up at an offset of channel spacing from the carrier and they are the most problematic type of spur. The cause of these spurs is the accumulator or Σ-Δ modulator operation. As stated before, since there are no devices which divide by fractional values, fractional N values are obtained by alternating between two or more integer N values such that average is the desired fractional value. Obviously this is done in a discrete manner. This abrupt adjustments cause fractional spurs corresponding to channel spacing or fractions of it (dithering case). When channel spacing is narrow these spurs fall into loop bandwidth and the spurs appear at the output.

Effective way of eliminating them is increasing the order of Σ-Δ modulator. The discussion was done in Σ-Δ fractional-N PLL section in detail.

2.6 Phase Noise Modeling of PLL

In traditional PLLs, VCO is separated from the digital circuitry with isolated external usage. In this type of structures, digital noise is isolated from the VCO which is the dominant component determining the phase noise beyond cut off frequency of the loop bandwidth. Therefore a carefully designed VCO is generally sufficient for matching low phase noise requirements. This is not the case for fully integrated PLLs. Digital noise coupling to VCO may have destructive effects on phase noise performance. So, digital noise becomes very important in such structures [9]. In the following analysis, design is assumed to be done with discrete components and noise coupling is not taken into account to not to make analysis very complex. In a case where noise coupling has significant effect, using simulation tools is

more logical. PLL phase noise is modeled by considering the noise sources in the system one by one and calculating the transfer of these individual noise sources to the output. Model is shown in Fig. 2.16. Noise contributions of individual blocks are shown in the model in angle, current and voltage forms where θ_{REF}, θ_{PFD}, θ_{DIV}, I_{NCP}, V_{NCONT}, θ_{VCO} denote reference noise appearing at the reference input of the PFD, PFD noise including reference oscillator and reference divider noise, N divider noise, charge pump noise, control voltage noise, VCO noise respectively. Note that K_{VCO} is tuning gain of the oscillator.

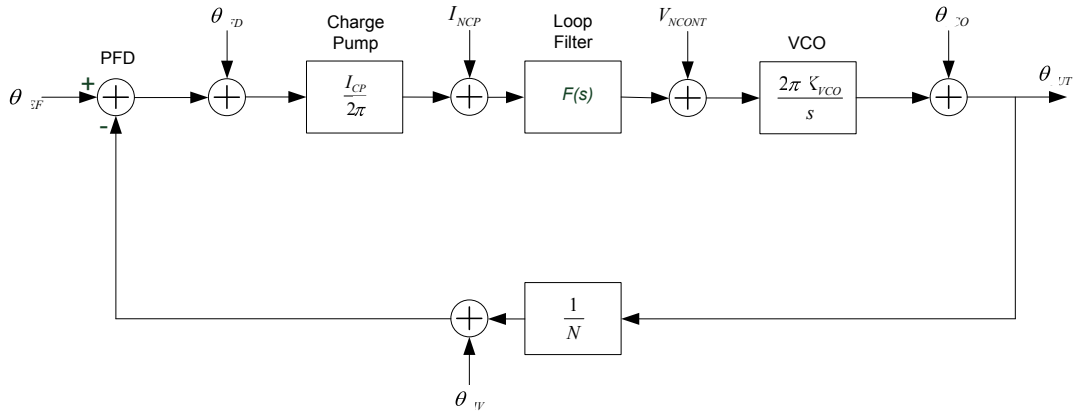


Figure 2.16 : Linear phase domain model of PLL

Combined forward transfer function of the system is the product of charge pump, loop filter and VCO transfer functions which is expressed as (2.9). Considering the feedback transfer function $H(s) = 1/N$, reflections of each noise source to the output can be written as expressed from (2.10) to (2.15).

$$G(s) = \frac{I_{CP}}{2\pi} F(s) \frac{2\pi K_{VCO}}{s} \tag{2.9}$$

$$\frac{\theta_{OUT}(s)}{\theta_{REF}(s)} = T_{REF}(s) = \frac{G(s)}{1 + G(s)H(s)} \tag{2.10}$$

$$\frac{\theta_{OUT}(s)}{\theta_{DIV}(s)} = T_{DIV}(s) = \frac{G(s)}{1 + G(s)H(s)} \tag{2.11}$$

$$\frac{\theta_{OUT}(s)}{\theta_{PFD}(s)} = T_{PFD}(s) = \frac{G(s)}{1 + G(s)H(s)} \tag{2.12}$$

$$\frac{\theta_{OUT}(s)}{i_{NCP}(s)} = T_{NCP}(s) = \frac{2\pi}{I_{CP}} \frac{G(s)}{1 + G(s)H(s)} \tag{2.13}$$

$$\frac{\theta_{OUT}(s)}{\theta_{VCO}(s)} = T_{VCO}(s) = \frac{1}{1 + G(s)H(s)} \tag{2.14}$$

$$\frac{\theta_{OUT}(s)}{V_{NCONT}(s)} = T_{NCONT}(s) = \frac{2\pi K_{VCO}}{s} \frac{1}{1 + G(s)H(s)} \tag{2.15}$$

These equations show individual noise contributions of each block to the output noise. Since these are noise terms total noise is calculated as RMS sum of these terms as given in (2.16).

$$\begin{aligned} \theta_{out}^2 \quad &= (\theta_{REF}T_{REF})^2 + (\theta_{DIV}T_{DIV})^2 + (\theta_{PFD}T_{PFD})^2 + (I_{NCP}T_{NCP})^2 + (\theta_{VCO}T_{VCO})^2 \\ &\quad + (V_{NCONT}T_{NCONT})^2 \\ &= \left(\frac{G(s)}{1 + G(s)H(s)}\right)^2 \cdot \left[\theta_{REF}^2 + \theta_{DIV}^2 + \theta_{PFD}^2 + \left(I_{NCP}\frac{2\pi}{I_{CP}}\right)^2\right] \\ &\quad + \left(\frac{1}{1 + G(s)H(s)}\right)^2 \cdot \left[\theta_{VCO}^2 + \left(V_{NCONT}\frac{2\pi K_{VCO}}{s}\right)^2\right] \end{aligned} \tag{2.16}$$

Examining the common factors, it can be seen that reference, R divider, PFD and charge pump noises are dominant at low offset frequencies; control voltage and VCO noises are dominant at large offset frequencies. This can be better seen looking at common factor transfer functions plotted in Fig. 2.17. Note that f_c, f_p and f_z denote cut-off frequency, pole location and zero location respectively.

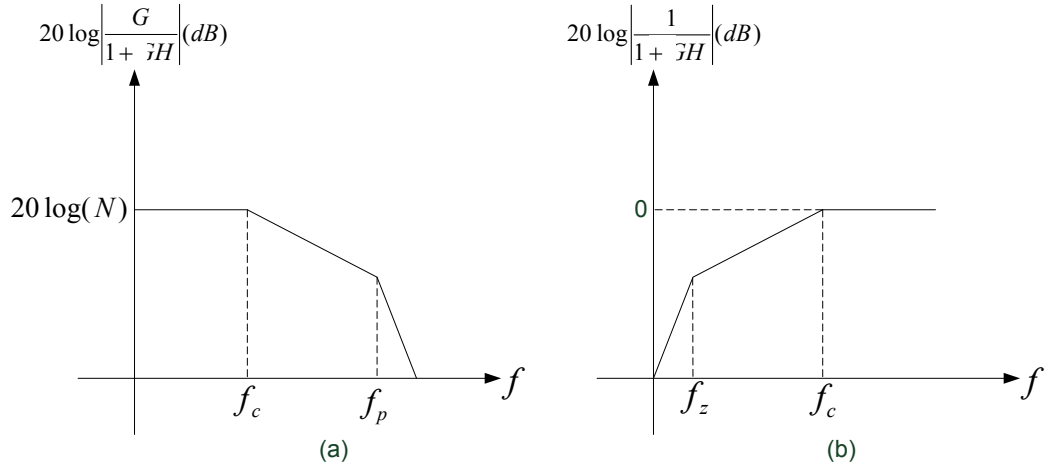


Figure 2.17 : Frequency characteristics of the common terms multiplying (a) reference, PFD, R divider and charge pump noise (b) VCO and control voltage noise

$G(s)$ approaches to infinity when frequency goes to zero. In such a case expression simplifies to *20 log N* in dB scale as illustrated in 2.17.

$$\lim_{G\to\infty}\left(\frac{NG}{N+G}\right)=N \tag{2.17}$$

This means close-in phase noise increases by *20 log N* with increasing *N*. To reduce close-in phase noise, *N* should be kept as small as possible. In integer N synthesizers, N is an integer multiple of the frequency resolution so there is not much choice on the value but this is not the case for fractional N synthesizers. Since fractional division rates are accepted, N value can be made smaller while frequency resolution is kept constant.

Loop bandwidth is also an important design parameter. It shapes the phase noise characteristic of the PLL. Noise on VCO and control voltage is suppressed inside the bandwidth and up to the corner frequency other noise sources are dominant. Beyond f_c characteristic mostly follows VCO noise. Optimum f_c is found as intersection of the noise floor of close-in noise and VCO noise curve which is shown in Fig. 2.18 (a). When f_c is chosen smaller or larger, performance loss occur which are shown in Fig. 2.18 (b) and (c).

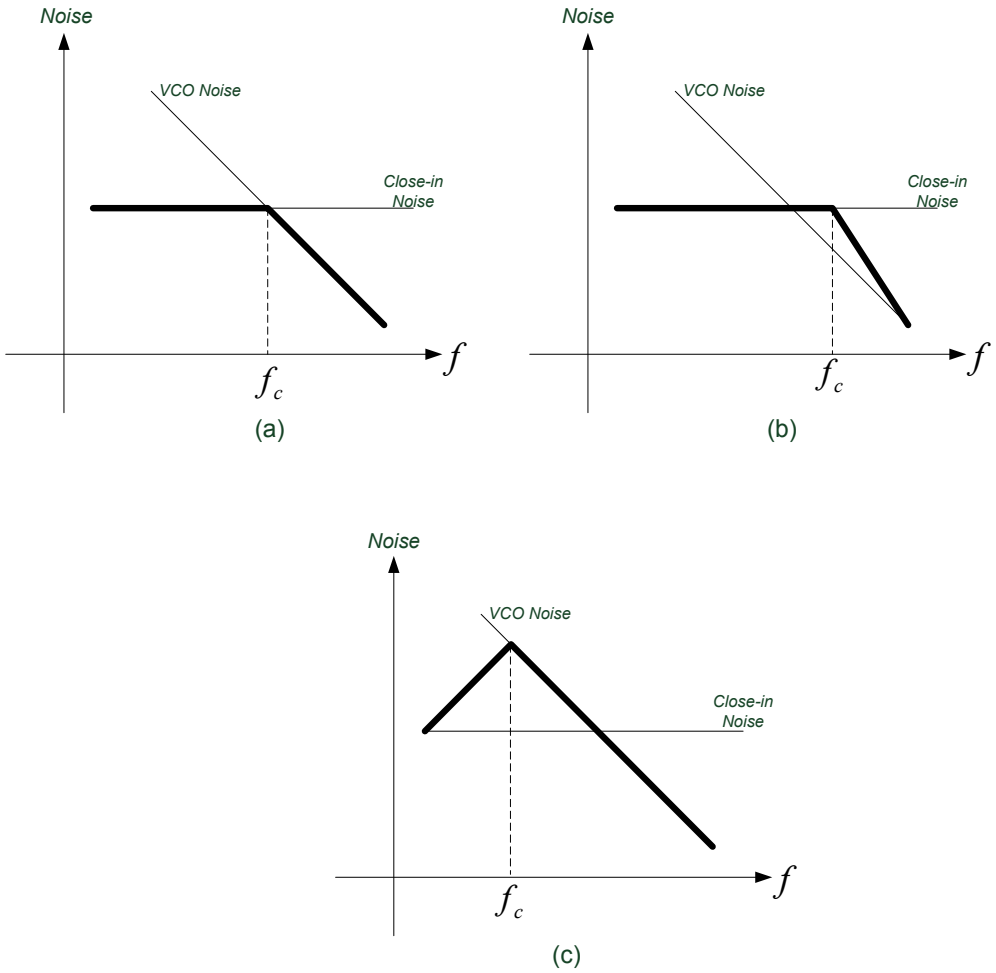


Figure 2.18 : (a) PLL optimum cut-off frequency selection (b) larger than optimum (c) smaller than optimum

In practical PLLs, reference oscillator noise is dominant up to nearly 1 kHz. In between this frequency and filter cut-off frequency, noise of PLL circuitries namely PFD, charge pump and dividers are effective. Beyond cut-off noise of VCO is observed. This characteristic is roughly shown in Fig. 2.19. L_o is the noise floor calculated as given in

$$L_o = 10\log(f_{REF}) + L_{PLL} + 20\log(N) \tag{2.18}$$

where L_{PLL} denotes PLL circuitry noise and f_{REF} is the reference oscillator frequency. The reference frequency term comes from the dead zone characteristics of the charge pump. When the phase error is zero, charge pump is neither sourcing nor sinking current. In such a case due to finite rise time small-loop phase deviations occur which is the dead zone operation. During dead zone both current source and current sink transistors are on.

Therefore some certain noise is injected due to these currents although average is zero. Noise due to this situation is calculated in (2.19) where factor 2 accounts for sink and source currents. T_d is the dead zone period and T_{REF} is the period of reference signal.

$$I_{NCP}^2 = 2\left(\frac{T_d}{T_{REF}}\right) I_{CP,noise}^2 \tag{2.19}$$

According to this equation, close-in noise increases with increasing reference frequency. To avoid this dead zone characteristic, certain artificial phase offset is used so that during locked operation charge pump either sources or sinks current [9].

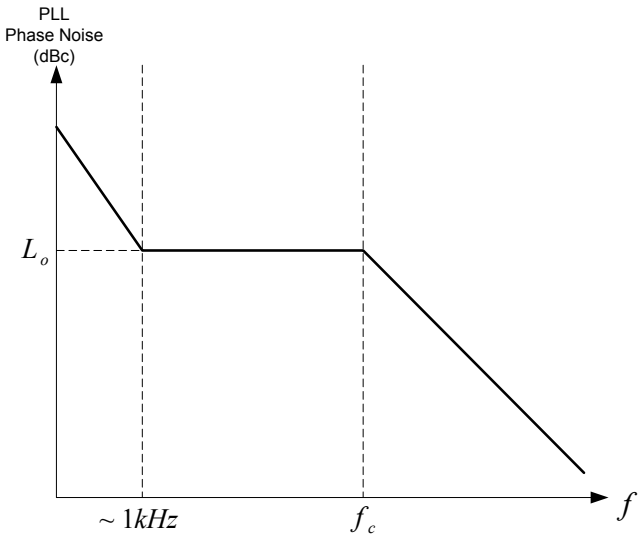


Figure 2.19 : Typical PLL phase noise characteristic

The analysis gives some insight about reduction of the phase noise in PLLs. First, to minimize close-in phase noise PLL circuitry should be carefully designed and digital noise should be kept as low as possible. Second, two inflicting parameters namely reference frequency and division rate *N* should be optimized. Analysis shows that N divider value should be adjusted as small as possible also considering the channel spacing requirement. While doing that naturally reference frequency is increased and we also know that due to dead zone operation noise increases with increasing f_{REF}. Therefore, these parameters should be carefully optimized. Third, charge pump current should be adjusted to maximum. This will increase SNR since noise will be kept at same level. Fourth, to decrease phase

noise beyond cut-off frequency phase noise of VCO and noise on control voltage should be decreased.

These techniques are both technology and operation related. Today, most of the PLLs are made using synthesizer chips including reference divider, PFD, N divider and charge pump. Although it is not possible to intermeddle inside the chip, considering the analysis given in this section, designer should select the chip which has lowest noise specifications among the available ones. Rest is the adjustment of operational settings according to the guidelines mentioned here. It is also seen in phase noise analysis that the most critical component is VCO. Beyond a certain frequency PLL noise follows the VCO. Therefore reduction of VCO phase noise directly reduces the PLL phase noise.

2.7 Loop Filter Design

In this section, basically principles of designing proper loop filter are discussed. As stated before in PLL components section, loop filter is used to filter high frequency components in the control voltage line to maintain pure DC input to the VCO. Loop filter is important for phase noise and spurious responses of the PLL therefore it should be carefully designed. Loop filter design involves selection of proper filter topology, filter order, loop bandwidth, phase margin and pole ratios [6].

Referring to the previous noise considerations, active filters are not desired for low noise applications because of their contributions to the phase noise. Hence, in modern PLLs if there is not a mismatch of VCO control voltage and charge pump output voltage, passive filters are used.

Order of the loop filter is determined by the number of poles and the most basic passive filter is second order filter as shown in Fig. 2.20. Due to the pole coming from VCO, PLL order is one greater than the order of the loop filter. For the proper design of the loop filter, capacitance of the control voltage port should also be taken into account.

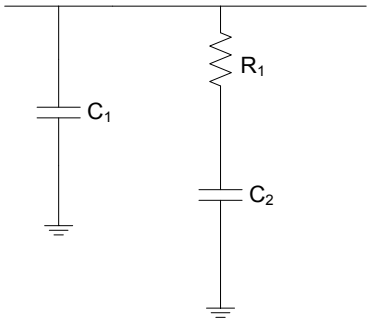


Figure 2.20 : Second order passive loop filter

Filter order is the number of its poles and can be increased by additional poles. If the order of the filter is increased, filter attenuation response in the stop-band is improved. This means better filtering of the spurs. On the other hand additional components come with their thermal noise which contributes to the phase noise. In practice generally third order filter which was shown in Figure 2.7 (b) is used for an additional 10 or 20 dB spur attenuation [10]. In cases where spur frequencies are much higher than loop bandwidth this additional attenuation is important. Although second order filter is less noisy, it cannot attenuate spurs as much as higher order filters. On the other hand using higher order loops may cause instability by reducing phase margin at unity gain.

Easiest way of looking at system stability is to analyze its bode plot. A sample bode plot is shown in Fig. 2.21. Phase margin is the distance to 180^0 at unity gain frequency. Phase margin relates the stability of the system and generally chosen between 40^0 and 55^0 [6]. As the phase margin decreases quality factor of the filter increases however this can cause instabilities and ringing in the system. On the other hand if the phase margin is made too high this will increase the lock time. Stable operation of a second order filter has no problems since its open loop transfer function has two poles and one zero. A pole and a zero create -90^0 and 90^0 phase shifts respectively at far away frequencies. Therefore when they are properly placed, phase margin never becomes zero and loop is stable. With increasing order, new poles are added to filter which have potential to cause a phase shift greater than -180^0 at unity gain which will start unwanted oscillations. For this reason poles and zeros of the higher order filters should be carefully placed not to cause instability.

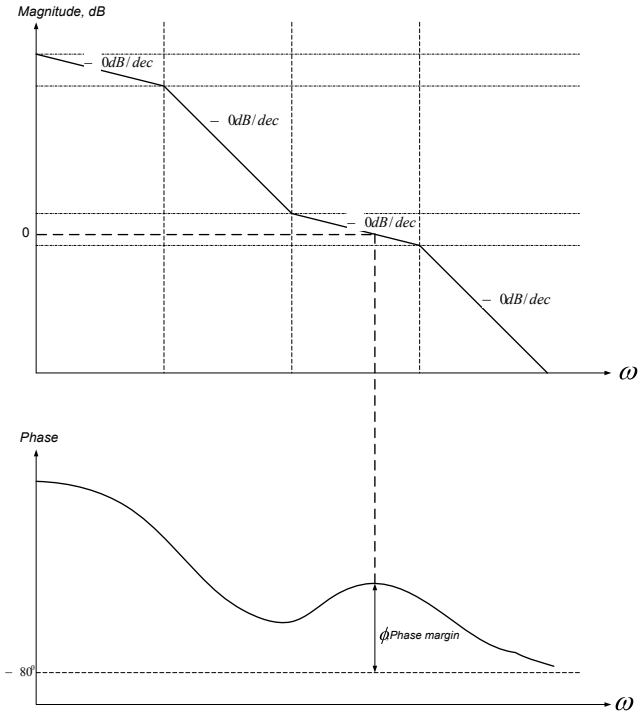


Figure 2.21 : Stability analysis by Bode plot

Bandwidth of the loop filter is also important for the performance of the PLL. Bandwidth effects can be summarized as follows. Since bandwidth and switching speed are related as given in (2.20) where ω_n denotes the bandwidth and ξ is the damping factor, decrease in the bandwidth causes system to lock in a longer period. On the other hand obviously spurs are attenuated better with decreasing bandwidth. Apart from these considerations, in PLL phase noise analysis part it was shown that optimum cut off frequency is the intersection of noise floor and close in phase noise lines. Smaller or larger bandwidths cause performance loss. Therefore decreasing close in noise enables the designer to select smaller bandwidths. This is especially important in the applications where lock time is not critical.

$$T_{sw} \propto \frac{1}{\omega_n \xi} \tag{2.20}$$

After deciding filter topology, filter order, bandwidth and phase margin, component values can be calculated from the time constants which determines poles and zeros of the system. For a third order filter, component values can be calculated from given loop bandwidth f_c , phase margin ϕ , charge pump gain K_{cp}, VCO gain K_{VCO}, output frequency f_{out}, PFD frequency f_{PFD} and pole ratio T_{31}. First time constants and filter coefficients should be calculated. Then filter component values can easily be found. Detailed calculations and MATLAB script of the loop filter design is given in Appendix A.

CHAPTER 3

PLL BASED LOCAL OCILLATOR DESIGN

A low noise PLL based local oscillator working at 2.21 GHz is designed to be used in X-Band transmitter system block diagram of which is given in Fig. 3.1.

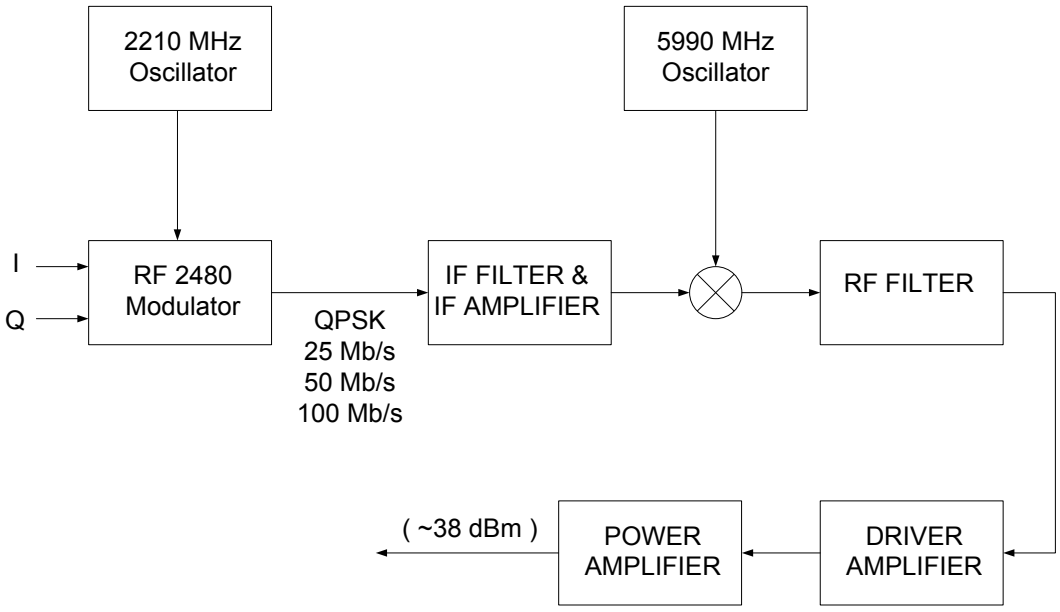


Figure 3.1 : Block diagram of X-Band transmitter system

Structure is implemented using Analog Devices' high resolution Fractional-N frequency synthesizer ADF4157 that is implemented using third order Δ-Σ fractional modulator. Functional block diagram is given in Figure 3.2. Main advantage of this synthesizer is its improved noise performance and frequency resolution. Including 12 bit integer divider, channel spacing can be as low as $f_{PFD}/2^{25}$ as it involves 25 bit fixed modulus for fractional division. This high modulus makes Δ-Σ modulator quantization error spectrum look like

broadband noise spreading the fractional spurs into noise. Other spurious generating mechanisms namely integer boundary spurs and reference spurs will be eliminated by the loop filter.

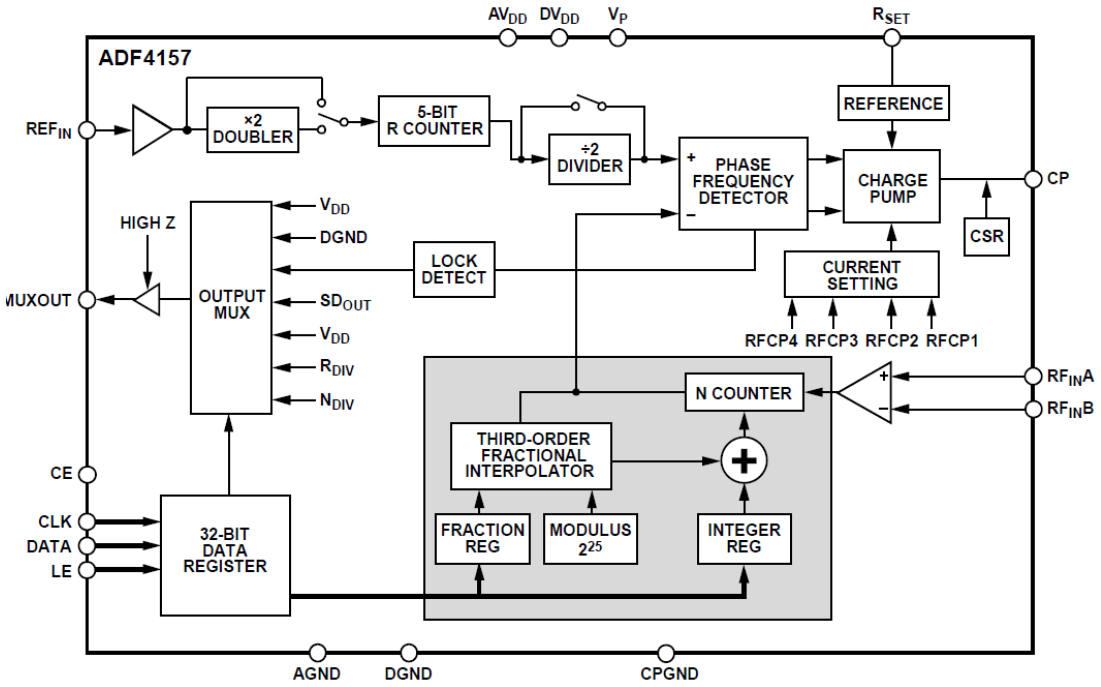


Figure 3.2 : Functional block diagram of ADF 4157 [11]

Synthesizer also includes reference frequency doubler part to improve phase noise performance and cycle slip reduction circuitry which provides faster lock times in exchange for lower noise performance. These functionalities can be enabled or disabled according to preference. Charge pump section works with a separate charge pump voltage and programmable current. Its dividers and other functionalities can be programmed via three wire serial interface.

In the following section, first simulations including loop filter design, system simulations, phase noise simulations and spurs are given. Then implementation details including the measurements are summarized and the difference between design goals and implementation results are examined including the possible causes of the problem.

3.1 Simulations

For the design and analysis, Applied Radio Labs' ADISim v3.1 software is used. As the reference MTI's 10 MHz electrically tuned temperature compensated crystal oscillator which has spacecraft flight heritage is used. Specifications of this TCXO are given in Table 3.1. For simulation purpose this reference TCXO is modeled as a custom reference. Phase noise plot of the modeled custom reference is shown in Fig. 3.3.

Table 3.1 : Specifications of MTI's TCXO

Frequency Stability vs Supply Voltage	±0.4 ppm
Frequency Stability vs Load	±0.4 ppm
Power Consumption	30 mW
Electrically Tuning	±3 ppm
Phase Noise	
1 Hz	-55 dBc/Hz
10 Hz	-85 dBc/Hz
100 Hz	-115 dBc/Hz
1 kHz	-130 dBc/Hz
10 kHz	-145 dBc/Hz
100 kHz +	-150 dBc/Hz

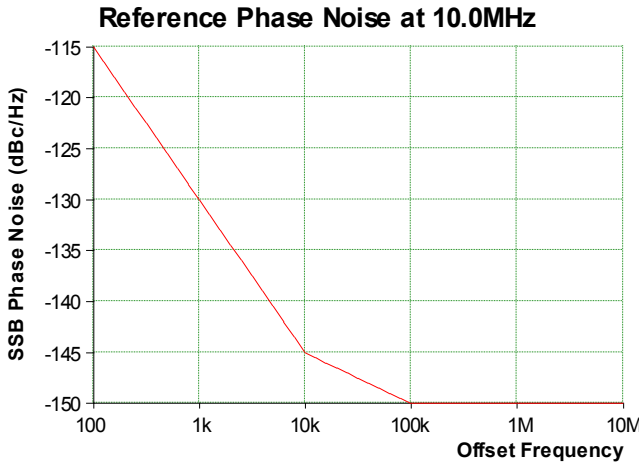


Figure 3.3 : Individual phase noise plot of simulated TCXO

As voltage controlled oscillator UMC's UMX-269-D16 covering 2070 MHz to 2270 MHz band is used. Selected ultra low noise VCO has phase noise about -127 dBc/Hz at 100 kHz offset and about -147 dBc/Hz at 1 MHz offset with the tuning gain K_v of 60 MHz/V. It has a tuning range between 0.5 V to 4.5 V with 47 pF tuning port capacitance and 120 mW power consumption. For simulation ADISim model of this VCO is used after some modifications, which are done to take tuning port capacitance into account. Some important electrical specifications of the VCO are given in Appendix B and characteristic plots are shown in Fig. 3.4.

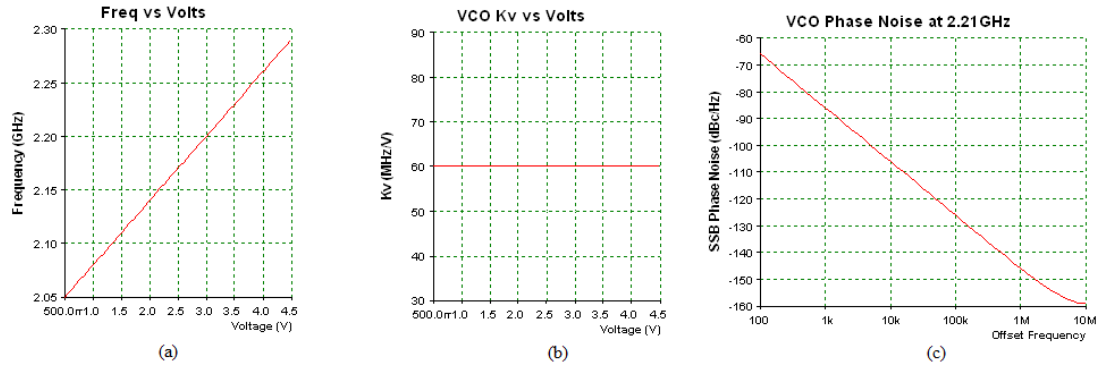


Figure 3.4 : (a) Frequency-Voltage characteristics (b) tuning gain (c) phase noise performance of UMX-269-D16 VCO

3.1.1 Loop Filter Design

Following the theoretical background given in previous chapter, loop filter is designed by using the MATLAB script which is given in Appendix A together with the details of calculations. Different loop bandwidths and phase margins are simulated and results are compared. Phase noise characteristics for different loop bandwidths are shown in Fig. 3.5 and tabulated in Appendix C. As mentioned in phase noise analysis, noise contribution of PLL chip, charge pump and dividers decrease outside the loop bandwidth and noise of VCO gains importance. Therefore as bandwidth is made smaller total phase noise performance approximates ultra-low phase noise VCO performance. On the other hand lock time increases with increasing loop bandwidth. In ADISim, lock times are simulated with certain margin of error. In this design since the output frequency of the transmitter will not change during operation, the lock time is not so critical therefore there is no need for exact values. Simulated and approximated lock times for different bandwidths are tabulated in Table 3.2. Since, the lock time is not so critical, to decrease phase noise lock time is sacrificed. However decreasing bandwidth beyond 10 kHz seems to be impractical since for 5 kHz

bandwidth, lock time increases approximately four times and phase noise is very much approximated to VCO and gain is only ~1 dB at 100 kHz offset. Taking all these into account 10 kHz bandwidth is found to be optimum.

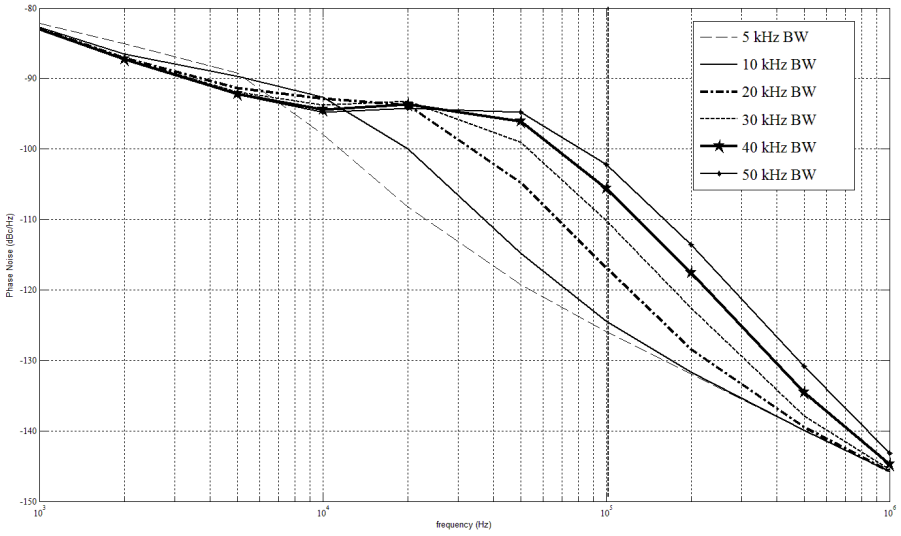


Figure 3.5 : Phase noise simulation for different loop bandwidths at 45^0 phase margin

Table 3.2 : Approximated lock times for simulated loop bandwidths

Loop Bandwidth	Lock Time
50 kHz	150 µsec
40 kHz	220 µsec
30 kHz	360 µsec
20 kHz	760 µsec
10 kHz	2.8 msec
5 kHz	11 msec

To improve phase noise further phase margin is reduced to its proposed lower limit which is 40^0 [6]. This decrement reduces phase noise about 0.5 dB as can be viewed in Table 3.3 and it also improves lock time about 300 μsec.

Table 3.3 : Phase noise improvement due to decrease in phase margin

Phase Margin	Phase Noise at 100 kHz Offset
55^0	123.4 dBc/Hz
50^0	123.8 dBc/Hz
45^0	124.3 dBc/Hz
40^0	124.8 dBc/Hz

In filter calculations, optimization parameters T_{31} and γ are set to 0.23 and 1.10 respectively and calculated filter components are given in Table 3.4. Calculated values are then optimized to improve phase noise performance in simulation environment and improvement is observed as 0.2 dB.

Table 3.4 : Calculated, optimized and realized values of filter components

Filter Component	Calculated Value	Optimized Value	Realization Value
C_1	123.48 nF	136 nF	150 nF
R_2	26.06 Ω	26.6 Ω	27 Ω
C_2	1.44 µF	1.46 µF	1.5 µF
R_3	38.25 Ω	41 Ω	43 Ω
C_3	77.48 nF	77.2 nF	82 nF
Loop BW	10.1 kHz	10.0 kHz	9.9 kHz
Phase Margin	41.2^0	40.2^0	38.5^0

Designed filter is simulated using Murata ceramic capacitor models in ADS environment. Simulated circuit and filter response are shown in Fig. 3.6 and Fig. 3.7 respectively. Note that C_3 value is large enough to ignore tuning port capacitance of the VCO which is 47 pF.

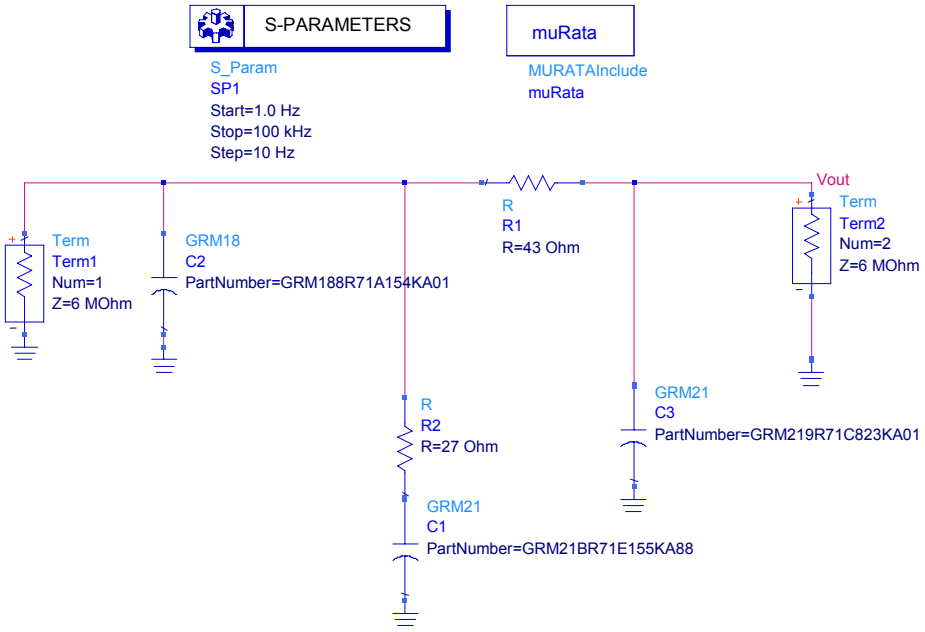


Figure 3.6: Filter circuit

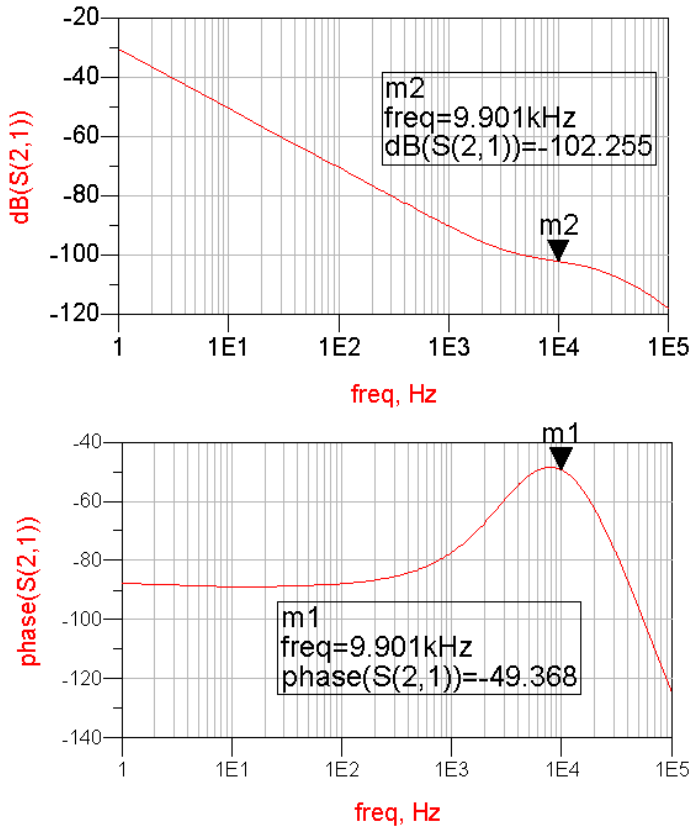


Figure 3.7 : Filter response

Together with charge pump (K_{cp}) and VCO (K_{VCO}/s) , at nearly 10 kHz offset open loop gain will be 0 dB and phase margin will be approximately 40^0.

3.1.2 System Characteristics

Simulated PLL system is shown in Fig 3.8. Bandwidth and phase margin can be viewed in open loop gain plot given in Fig. 3.9(a). In phase noise analysis part in previous chapter, it was shown that phase noise contribution of reference, dividers, PFD and charge pump are multiplied by closed loop transfer function and reflected to the output. Therefore phase noise attenuation of contribution of these components can be followed from closed loop gain plot given in Fig 3.9 (b). Outside the bandwidth phase noise of VCO is effective.

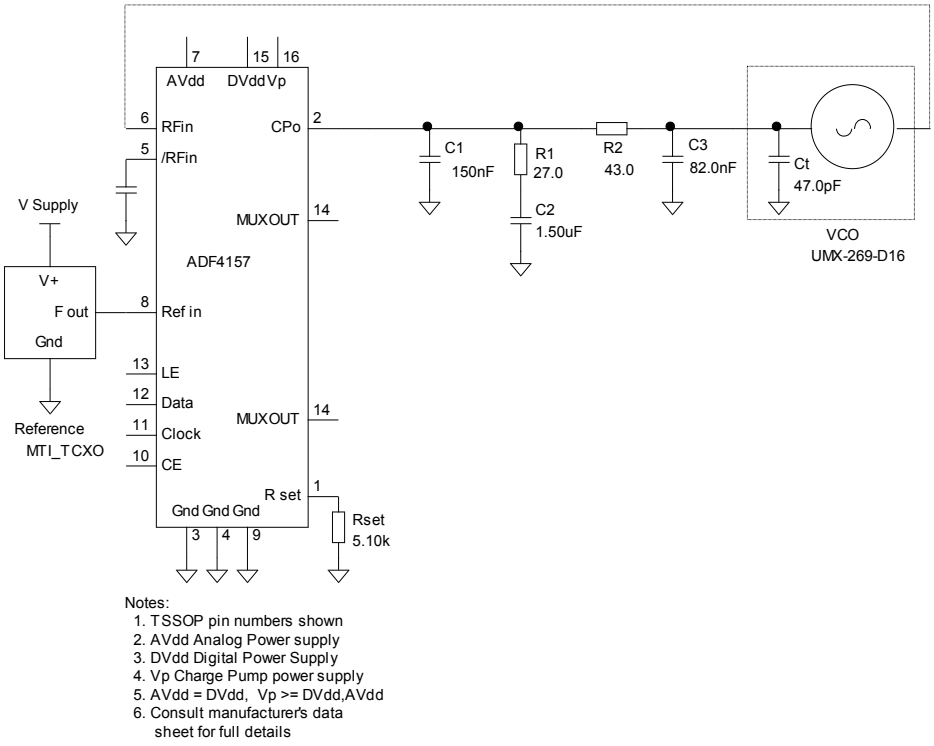
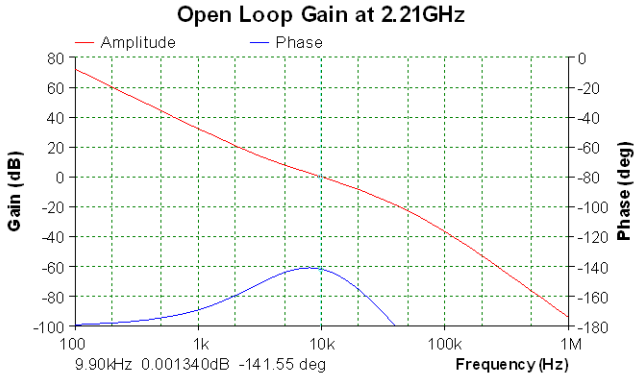
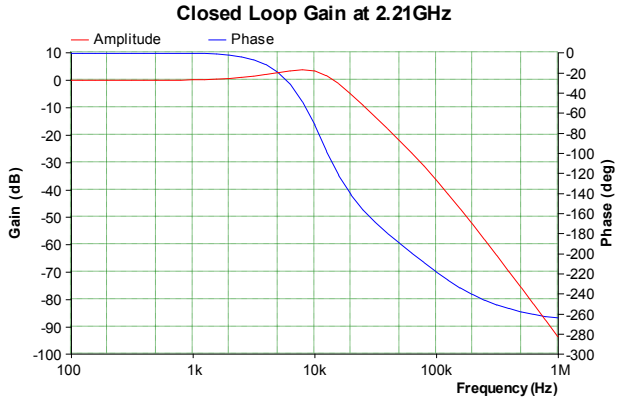


Figure 3.8 : Simulated PLL circuitry



(a)



(b)

Figure 3.9 : (a) Open loop (b) closed loop transfer functions at 2.21 GHz

Simulated transient responses of frequency error, output phase error and frequency stabilization characteristics are given in Fig. 3.10 (a), (b) and (c) respectively. Results show that system needs approximately 2.8 msec to lock to both frequency and phase. Lock time is a critical issue in high speed circuits which require switching frequency of oscillation in a restricted time interval. In this local oscillator design it does not have that much importance and stated lock time seems to be fine.

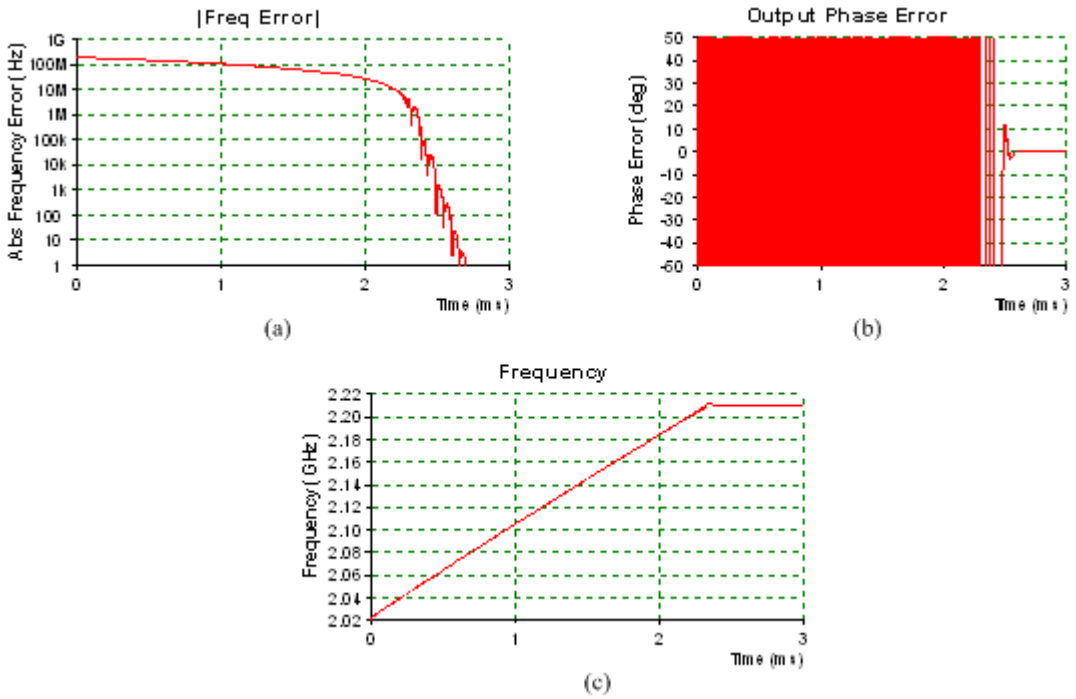


Figure 3.10 : (a) Transient frequency error (b) transient output phase error (c) transient frequency characteristics of simulated PLL.

3.1.3 Phase Noise

Phase noise contribution of each component and total response at different offset frequencies are listed in Table 3.5 and plot is shown in Figure 3.11. As can be seen from results, up to loop bandwidth phase noise of the reference dominates the characteristics. At loop bandwidth contribution reference nearly becomes the same as chip and approximates to filter and VCO. Therefore a decrease in the slope is observed at the loop bandwidth. After that frequency VCO becomes the dominant factor of phase noise as expected and beyond 100 kHz response completely follows the phase noise of the VCO. This is an expected behavior as analyzed in previous chapter.

Table 3.5 : Phase noise simulation results (all results are in dBc/Hz)

Frequency	Reference	Chip	Filter	VCO	**TOTAL**
100 Hz	-68.11	-99.12	-139.7	-138.0	**-68.11**
1 kHz	-82.90	-98.91	-119.7	-118.0	**-82.79**
10 kHz	-94.53	-95.54	-104.7	-102.3	**-91.40**
100 kHz	-139.5	-135.5	-137.6	-125.9	**-125.0**
1 MHz	-196.8	-192.8	-176.0	-145.8	**-145.8**

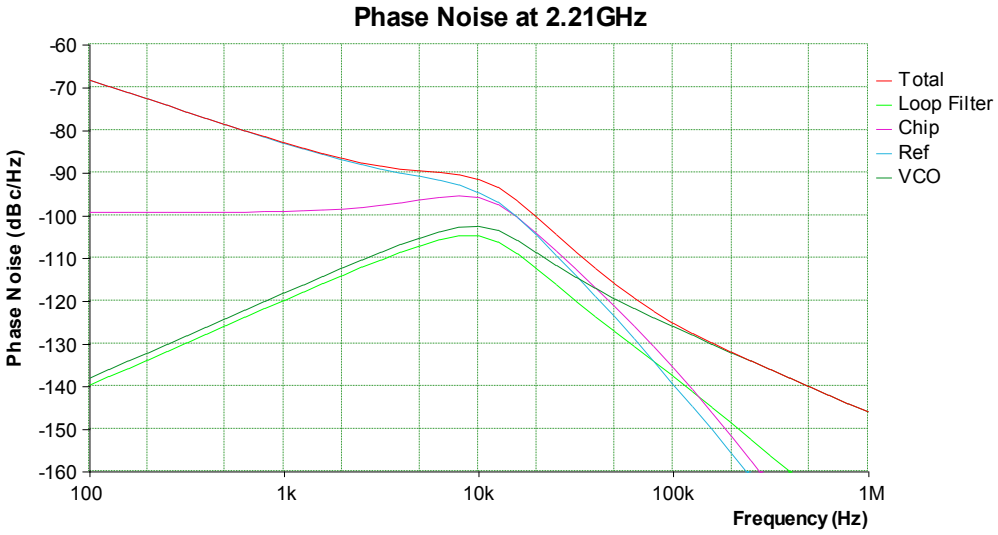


Figure 3.11 : Phase noise contribution of system components and total response

3.1.4 Spurious Response

In simulations there seem to be no reference spurs and no significant fractional spurs. As mentioned in previous chapter reference spurs are not problematic in fractional-N synthesizer. Therefore no significant reference spurs are expected at the output of the system. Nevertheless, theoretically high value of fixed modulus in frequency synthesizer chip makes Δ-Σ quantization error spectrum look like broadband noise. This spreads the fractional spurs into noise and there remains no significant fractional spurs [11].

In practice there will be integer boundary and reference spurs due finite filtering even for a higher order filter and well designed PCB. Spur levels depend on the PCB design. To reduce

them, unexpected feed through of the reference signal to the VCO by passing the loop filter should be avoided. So, output signal should be very-well isolated from reference signal.

3.2 Implementation

Simulated PLL is implemented using LFCPS package of ADF4157. This prototype is designed to be working with a single 5 V supply. Analog and digital 3.3 V supplies needed by the synthesizer is generated using MIC29301 voltage regulator and isolated by TOKO ECM85 DC power filter which also separates analog and digital grounds. In case of a possible failure, prototype circuit also has external supply option. Circuit schematic is drawn in PCAD Schematic tool and shown in Fig.3.12.

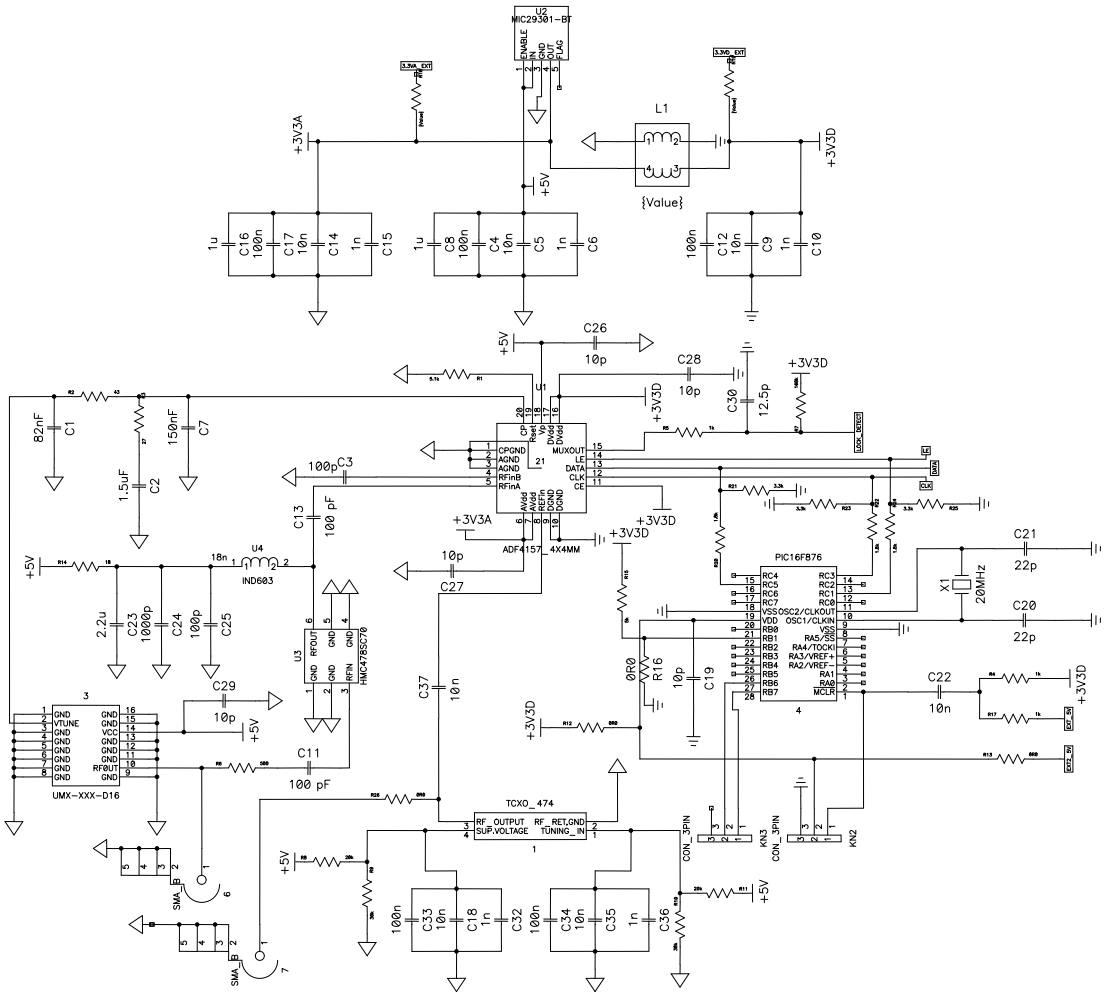


Figure 3.12 : PLL circuit schematic

Reference signal, supplied by MTI Milliren's 10 MHz TCXO having 3 dBm output, is fed to the synthesizer by capacitive coupling. This TCXO can be bypassed and reference can be given externally for testing allowable reference signal level margins.

Charge pump output is fed to the V_{tune} input of UMX-269-D16 via a 3rd order 10 KHz bandwidth passive filter having 40^0 phase margin. In this design, there is no need for an active loop filter since the tuning range of VCO does not exceed charge pump output limit. At the output sampling is done over 500 Ω resistor and this sampled signal level is about -22 dBm. Since the synthesizer requires input between -10 dBm and 0 dBm to the RF prescaler, sampled signal is amplified by 20 dB by Hittite Microwave's HMC478SC70 HBT gain block.

3.2.1 Operational Settings

For setting the registers of the synthesizer, SPI module of Microchip's PIC16F876A is used. This programmable IC works with 5V and resistive voltage division is used to take this voltage down to 3.3V for DATA, CLK and LATCH ENABLE inputs of the synthesizer. Microcontroller code can be changed on the board by using in-circuit debugger. In ADF4157 output- PFD frequency and PFD-reference frequency relations are as given in 3.1 and 3.2 respectively where D, T, R stand for reference doubler, reference divide-by-two and R counter respectively.

$$f_{out} = f_{PFD}\left(INT + \frac{FRAC}{2^{25}}\right) \tag{3.1}$$

$$f_{PFD} = f_{REF}[(1+D)/(R(1+T))] \tag{3.2}$$

In the settings, D is enabled and T is disabled for better phase noise performance. Also R counter is set to 1. According to these adjustments PFD frequency is set to 20 MHz. To have 2.21 GHz output division should be 110.5. This division ratio is adjusted writing appropriate values to the related register using equations 3.3, 3.5 and 3.6[11]. Division to 110.5 is satisfied with writing 110 to the integer division register and 2048 to the 12 bit MSB fraction register.

$$N = int\left(\frac{f_{out}}{f_{PFD}}\right) = 110 \tag{3.3}$$

$$FRAC = F_{MSB}x2^{13} + F_{LSB} \tag{3.4}$$

$$F_{MSB} = int\left[\left(\frac{f_{out}}{f_{PFD}} - N\right) x\ 2^{12}\right] = \ 2048 \tag{3.5}$$

$$F_{LSB} = int\left[\left(\left(\frac{f_{out}}{f_{PFD}} - N\right) x\ 2^{12} - F_{MSB}\right) x\ 2^{13}\right] = \ 0 \tag{3.6}$$

Referring the phase noise analysis in previous chapter for reducing phase noise charge pump current should be set as high as possible to increase SNR. Therefore charge pump current is set to its maximum which is 5 mA and 4/5 prescaler is activated. For frequencies higher than 3 GHz 8/9 prescaler should be turned on. Although it is not needed for this application, lock detect precision is made 40 cycles of 15 nsec. After the locking, at least 600 nsec should pass for lock detect to be set. Since there is no need for a fast lock cycle slip reduction circuitry which will add to the phase noise is not enabled. PLL code for 2.21 GHz output is given in Appendix D.

3.2.2 Measurements

Two layer PCB is implemented with FR4 material having 1 mm thickness and dielectric constant ε_r of 4.70. For this material 50 Ω line width is calculated as 1.95 mm. Produced PCB drawing and photograph are shown in Fig. 3.13 and Fig. 3.14 respectively. Note that in this prototype production hole plating is not done but some critical holes are filled by hand using thin wires. Tests and measurements are done in Agilent E4407B spectrum analyzer. General picture of the output spectrum is shown in Fig. 3.15.

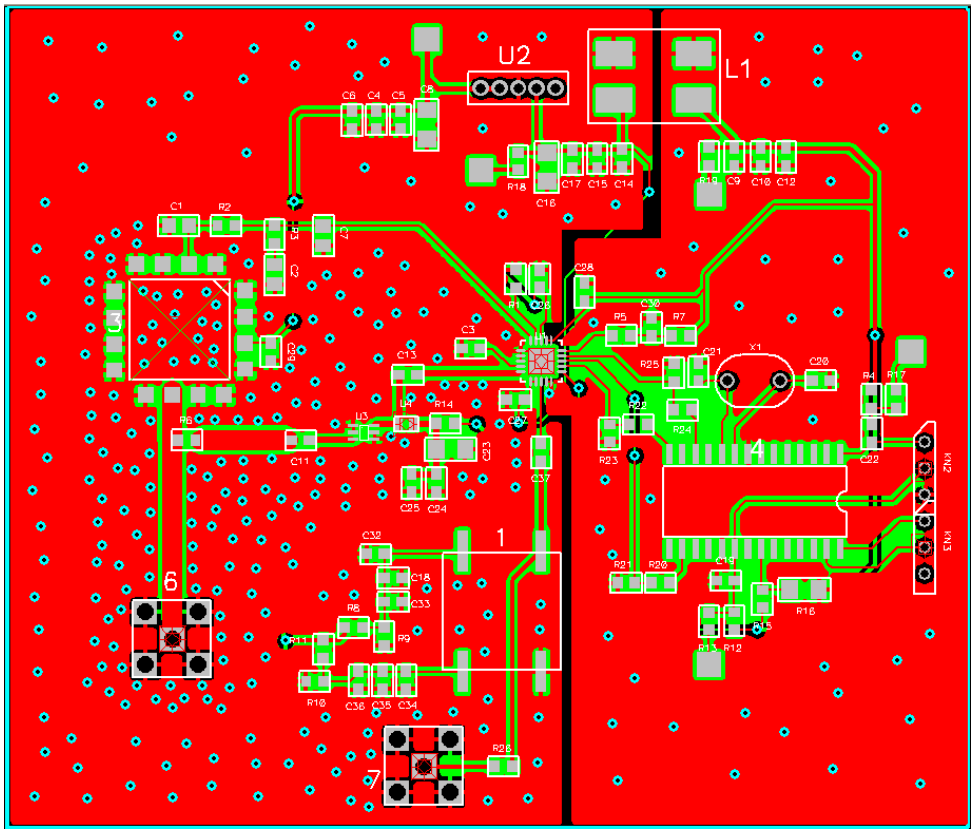


Figure 3.13 : PLL PCB drawing

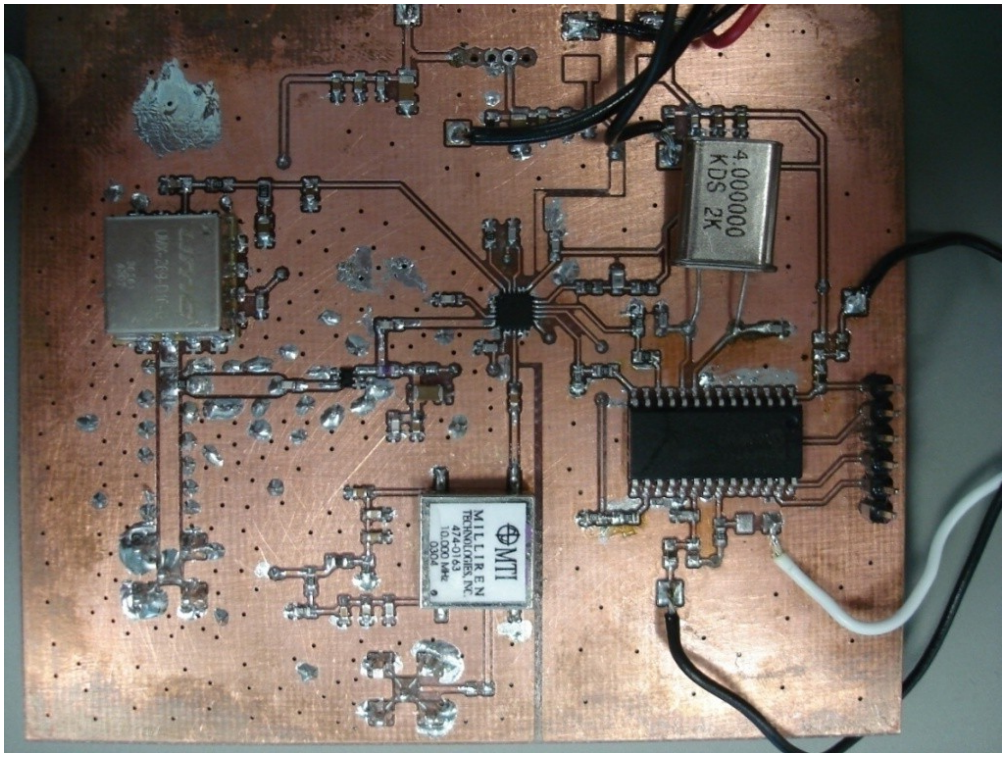


Figure 3.14 : PLL PCB

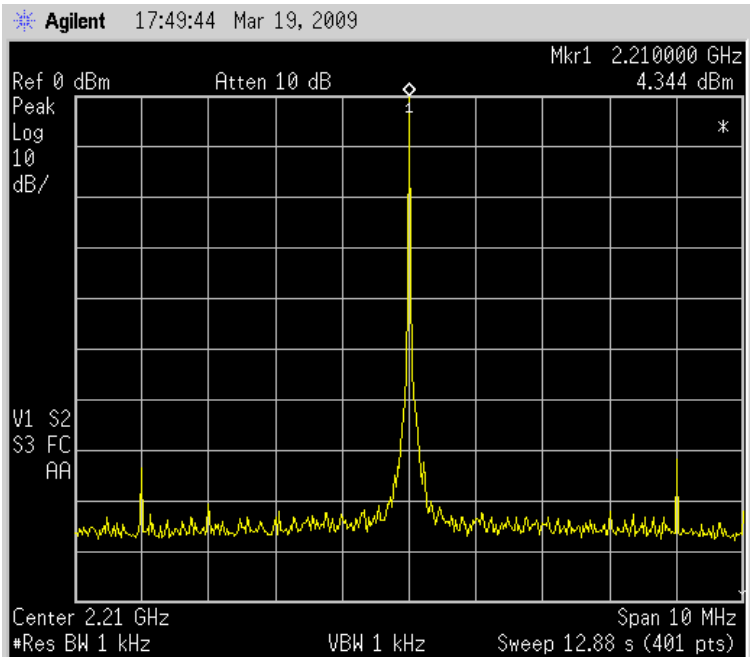


Figure 3.15 : Output spectrum

Harmonic response which shows no discrepancy with the specifications of the UMX VCO is shown in Fig. 3.16 and summarized in Table 3.6.

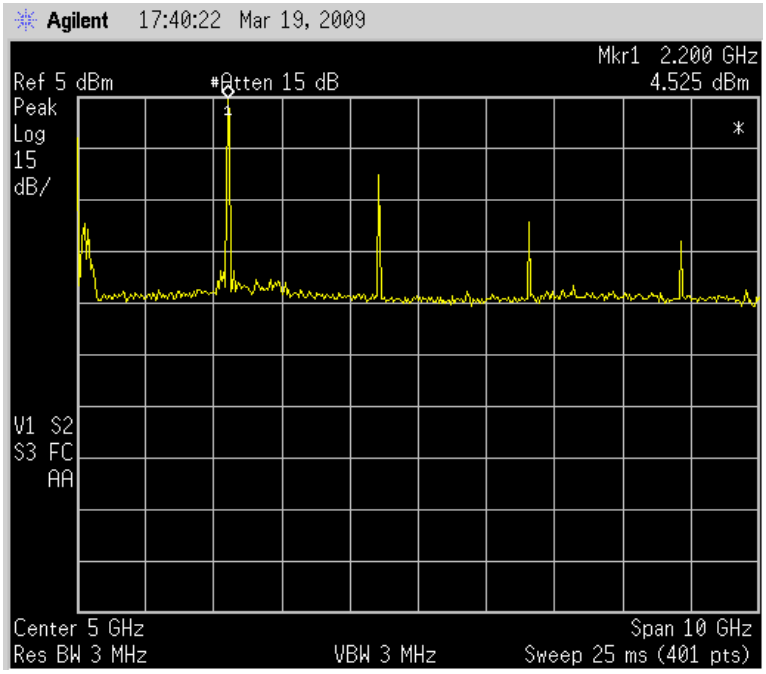


Figure 3.16 : Harmonic response

Table 3.6 : Harmonic response

Frequency (GHz)	Level (dBm)
2.21	4.5
4.42	-17.69
6.63	-30.77
8.84	-37.84

Spurious measurements are shown in Fig. 3.17 and listed in Table 3.7. Results show that system has some problems with the spurious response due to the feed-through of the oscillations to the VCO by passing the loop filter. This problem is mostly originated from bad grounding of the PCB. Spurs will mostly disappear when reference oscillator and crystal oscillator of microcontroller are well isolated from RF routing and hole plating is done.

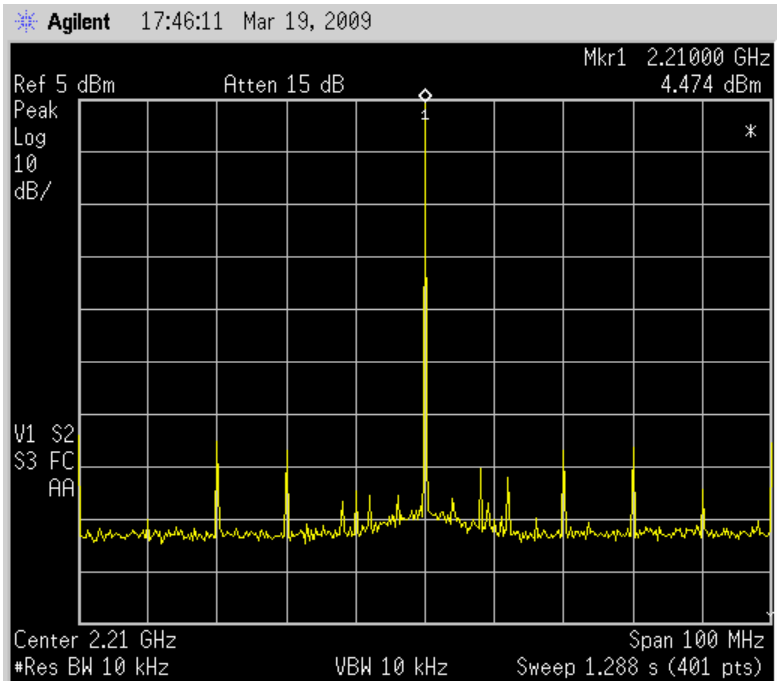
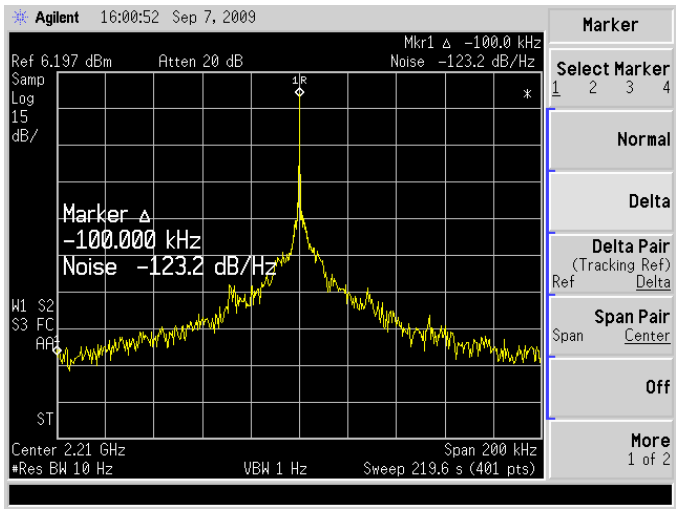


Figure 3.17 : Spurious characteristics

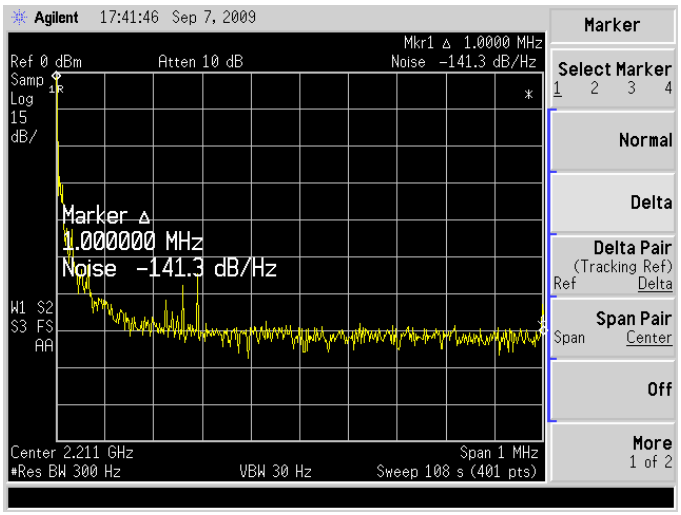
Table 3.7 : Spur levels

Frequency Offset (MHz)	Level (dBc)
4 MHz	-85
8 MHz	-77
10 MHz	-80
12 MHz	-78
20 MHz	-72
30 MHz	-70
40 MHz	-80
50-100 MHz	(-70)-(-80)

Phase noise measurements are done using marker noise functionality and resolution bandwidth is decreased as much as possible to eliminate noise of the spectrum analyzer. Measured phase noise is shown in Fig. 3.18 and summarized in Table 3.8. Note that at 1 MHz offset, measured value is close to the noise floor of spectrum analyzer for those measurement adjustments. Therefore at this offset value actual phase noise is expected to be less than measured phase noise.



(a)



(b)

Figure 3.18 : Phase noise measurement taken at (a) 100 kHz and (b) 1MHz

Table 3.8 : Phase noise measurements

Frequency Offset	**Level (dBc/Hz)**
10 kHz	-84.6
100 kHz	-123.2
1 MHz	< -141.3

As expected, measured phase noise values are somewhat above the simulation results. These differences may be originated from several factors. First, in system implementation an amplifier is added to feedback path to match sampled output signal level to desired level of synthesizer. This amplifier has certain contribution to the phase noise and this effect is not

included in simulation. Second, prototype system is implemented on FR4 material having a high dielectric constant which adds to the phase noise. This effect is expected to be 1-2 dB and can be lowered by using a less noisy material for the PCB. Moreover hole plating is not done in PCB. This may cause bad grounding and adds to the noise. Third, although loop filter is placed near to the VCO, it has potential to be modulated by any noise source due to long tuning voltage path and poor screening which may cause undesired noise coupling. This path should be made shorter. Fourth ground distance to 50 Ω output path is very short which distorts this impedance and cause impedance mismatch. This mismatch may cause additional noise [12]. To eliminate this effect ground distance to this path should be increased or this 50 Ω line should be designed as coplanar which will take ground distance into account. Fifth in such a sensitive measurement marker noise functionality may show 1-2 dB measurement error. This adds an uncertainty to the measured phase noise.

Electrical properties of designed oscillator are summarized in Table 3.9. 4.5 dBm output power is within the limits of modulator and no attenuation or amplification is needed. Therefore output of the module can directly be fed to the modulator. Also note that phase noise at 10 MHz could not be measured due to noise floor restriction of the spectrum analyzer. -160 dBc is the expected value from the phase noise data of VCO.

Table 3.9 : Electrical properties of designed oscillator

Frequency of Oscillation	2210 MHz
Power Output(dBm)	4.5 dBm
Harmonics(dBc)	-22 (Max)
Spurious (dBc)	-70(Max)
Supply Voltage (V)	5
Supply Current(mA)	110
Phase Noise (dBc/Hz)	
1 kHz	*-76*
10 kHz	*-84.6*
100 kHz	*-123.2*
1 MHz	*<-141.3*
10 MHz	*~(-160)*

CHAPTER 4

VOLTAGE CONTROLLED OSCILLATOR

In the previous chapter, a PLL is implemented using UMC's voltage controlled oscillator which is a DRO replacement discrete component. In today's technology, trend is to implement complete transceiver structure in a single chip therefore integrability is an important parameter for all of the components constituting PLL. For the purpose of easy integration a low phase noise CMOS voltage controlled oscillator is designed using TSMC 0.18μ technology. In this chapter, general oscillator overview including oscillator types, oscillator models, LC oscillator types are given, then basics of voltage controlled oscillators are explained, after that CMOS cross coupled differential VCO design which is the suitable topology for low phase noise requirements is explained in detail with implementation methods of each element in standard CMOS process. In chapter 5, phase noise models are analyzed and some common phase noise reduction techniques which are derived using phase noise models are introduced. Finally in chapter 6, oscillator is designed and noise reduction techniques are applied to see the effects in ADS simulation environment.

4.1 Oscillator Basics

4.1.1 Oscillator Overview

Electronic oscillator is a circuit that uses DC input to create periodic waveform which is generally a sine or a square wave. Oscillators are used in almost all of the electronic systems. Depending on the application types may differ. Oscillators that work in a certain frequency band with a voltage controlling the operation frequency are called voltage controlled oscillators and they are used in frequency synthesizers. Note that, although crystal oscillators may satisfy single frequency oscillation in MHz levels, at high frequencies, i.e. GHz levels, it is nearly impossible to implement an oscillator at single frequency in high resolution precisely due to imperfections in fabrication. For example it is impossible to

implement 2.0000 GHz oscillator in 1 kHz resolution. So, even though single frequency operation is required, tunable devices, i.e. VCO's are generally preferred and used with PLL circuitry.

In the following sections, first types of oscillators are summarized, then oscillator models are given, after that LC oscillators that are the most popular oscillator type for RF systems are explained in detail and finally common LC oscillator types are examined including realization method and performance comparison.

4.1.2 Types of Oscillators

Different categorizations of oscillators are possible but generally they are mainly classified according to the oscillation method as tuned (resonator) and nonlinear (waveform) oscillators as shown in Fig. 4.1[13]. As the name implies, resonators are the key structures in tuned oscillators which have sinusoidal output. Depending on the resonator type they are further divided into RC, switched-capacitor, LC and crystal oscillator. Among all LC oscillators are commonly used. On the other hand nonlinear feedback with active devices is used to generate certain waveforms like square or triangular shape in nonlinear oscillators.

Nonlinear oscillators, especially ring oscillators, are widely used in digital world. They are compact devices which have easy integration and implementation but they have unsatisfactory phase noise performance. Therefore they are not suitable for RF applications. Although LC oscillators have large chip area and problematic implementation they are widely used in RF due to their satisfactory phase noise performance. In this work CMOS LC oscillators are mainly focused.

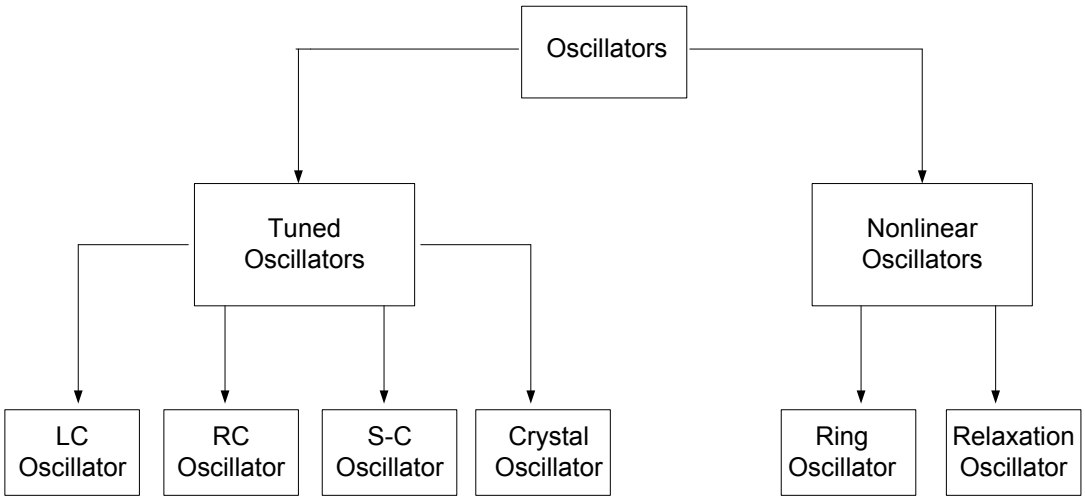


Figure 4.1 : Classification of oscillators

4.1.3 Oscillator Models

4.1.3.1 Feedback Model

An Oscillator can be modeled as linear feedback system as shown in Fig. 4.2. This model is also known as two port model. Transfer function of this system is given as:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{H(s)}{1 + H(s)} \tag{4.1}$$

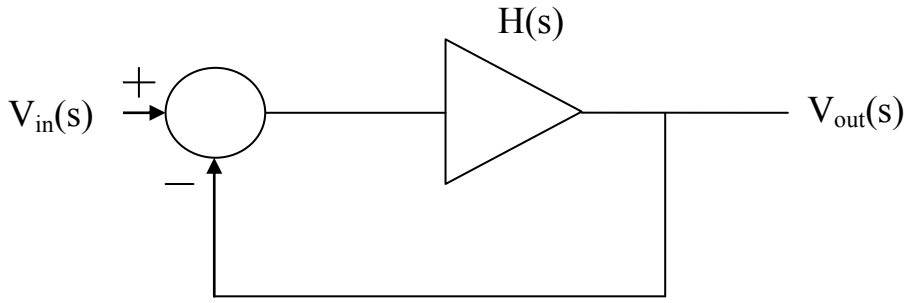


Figure 4.2 : Feedback model

Actually there are no intentional input signals in oscillators. Main source is incident noise which is modeled as V_{in}. For the oscillation to begin input noise should be amplified and added to the input by the loop. Note that loop transfer function H(s) also contains frequency

selection network so that oscillation occurs at desired frequency. To maintain oscillation there are mainly two conditions as shown in (4.2) and (4.3) which should be satisfied at the same time. These conditions are known as “Barkhausen Criteria” [14].

$$|H(jw_0)| \geq 1 \tag{4.2}$$

$$\angle H(jw_0) = 180^o \tag{4.3}$$

Second criteria should not be confusing. Since we model the structure as a negative feedback system, phase shift of the loop transfer function should be 180^0 for the total effect to be additive. If positive feedback were used phase shift would be zero (or 360^0). Note that in practical oscillators, in order to ensure oscillation in different environmental conditions and also taking into account probability of process variations loop gain is chosen to be three or four [14].

4.1.3.2 Negative Resistance Model

Another common oscillator model is negative resistance model which is also known as one port model as shown in Fig 4.3. The idea behind is that negative resistance of the active device cancels the loss of the resonator satisfying continuous oscillation at resonance frequency [15].

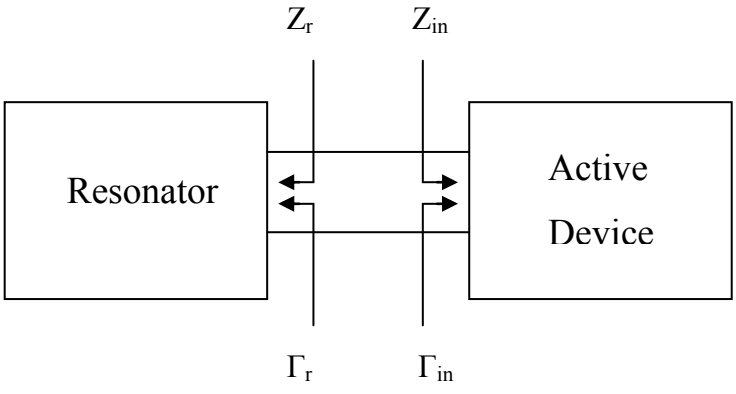


Figure 4.3 : Negative resistance model block diagram

Consider a small noise power P_N incident on the resonator. Reflected power from the resonator is $|\Gamma_r|^2 . P_N$. Then this power is incident on the active device which totally provides

$|\Gamma_r|^2 . |\Gamma_{in}|^2 . P_N$. In order oscillations to build up, the noise power should be amplified so we get the oscillation build up condition as given in 4.4.

$$|\Gamma_r \Gamma_{in}| > 1 \tag{4.4}$$

$$\Gamma_r = \frac{Z_r - Z_0}{Z_r + Z_0} \tag{4.5}$$

$$\Gamma_{in} = \frac{Z_{in} - Z_0}{Z_{in} + Z_0} \tag{4.6}$$

Solving 4.4, we find that in order oscillation to start , R_r + R_{in} should be negative which implies that R_{in} should be negative. After oscillations grow, active device is affected by the nonlinearity and the oscillations are stabilized. In stable oscillation case which is $|\Gamma_r \Gamma_{in}| = 1$, we obtain that R_r should be equal to -R_{in} and X_r should be equal to X_{in}. Reactive part determines frequency of oscillation and real parts cancel which means active device compensates the resonator loss.

For example in an NMOS cross coupled LC oscillator which is a common CMOS oscillator type, active part contains cross coupled NMOS transistors as shown in Fig 4.4. Input resistance R_{in} that will compensate resonator loss and maintain stable oscillation is calculated from small signal view as $-2/g_m$.

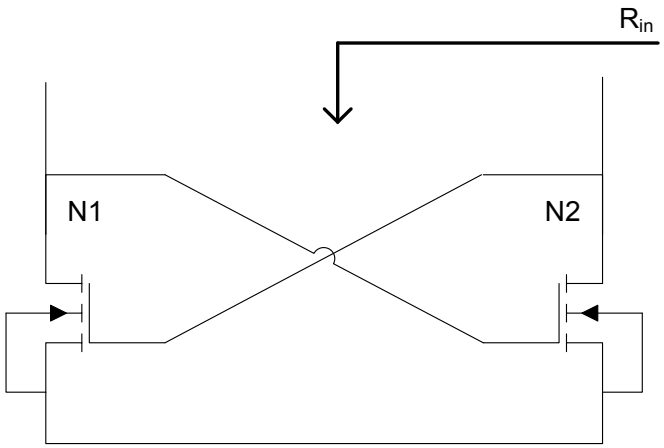


Figure 4.4 : NMOS cross coupled pair

4.1.4 LC Oscillators

LC oscillators are superior to other oscillator types in terms of phase noise performance. Since the phase noise is one of the most critical parameters of RF oscillators, in this work LC oscillators are focused. As the name implies, LC oscillators have LC resonators. Basically LC resonator consists of parallel or series connected inductor and capacitor. Parallel connected version is shown in Fig. 4.5(a). This ideal system resonates at frequency $w_c = 1/\sqrt{LC}$ and has an infinite quality factor since there are no losses. In practice passive components have certain losses which can be modeled as resistors. These losses limit the Q factor of the tank circuit. In comparison loss of the inductor is dominant so practically circuit can be modeled as given in Fig. 4.5(b) or in Fig 4.5(c). In transforming series resistance configuration to parallel one R_p is calculated as $Q^2 R_s$ [14].

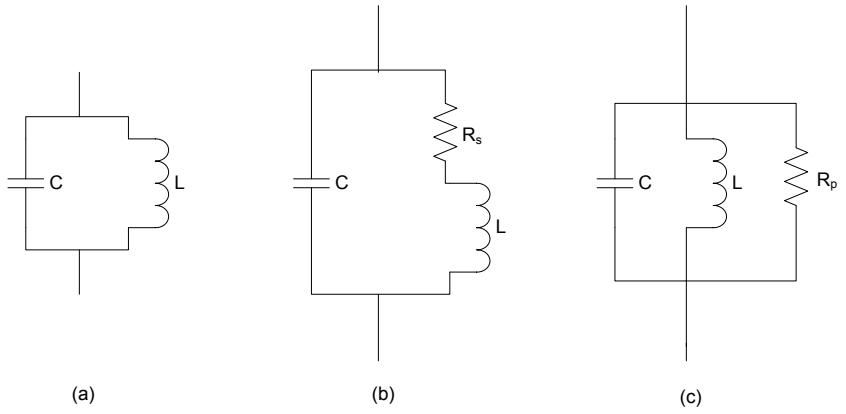


Figure 4.5 : (a) Ideal LC resonator (b) Practical LC resonator
(c) equivalent practical LC resonator (parallel configuration)

At $w_c = 1/\sqrt{LC}$ tank reduces to simple resistance. When $w < w_c$ inductive behavior and $w > w_c$ capacitive behavior is obtained as can be viewed in Fig. 4.6. At w_c, 90^0 phase shift is obtained from the resonator. We need two more poles and negative feedback to satisfy Barkhausen Criteria given in (4.2) and (4.3). There are several ways to implement these poles and the feedback which appear to be different LC oscillator topologies. In the next part some common topologies will be explained.

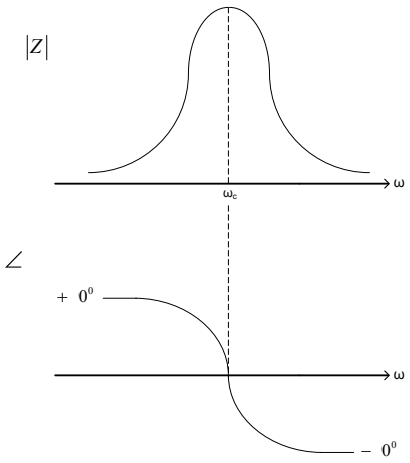


Figure 4.6 : Magnitude and phase of the impedance of an LC tank circuit

4.1.5 Common LC Oscillator Types

4.1.5.1 Cross- Coupled Differential LC Oscillator

When active device and resonator are connected together as shown in Fig 4.7 (a), at the resonance frequency voltage gain equals $-g_m R$ which means total phase shift around the loop is 180^0. As stated before in section 4.1.3, we need a total of 360^0 phase shift around the loop to maintain oscillation so we need one more stage as shown in Fig. 4.7(b). Total response is shown in Fig. 4.9. We can see that at resonance frequency magnitude response become sharper .This two stage configuration is also known as cross coupled differential topology as the signals at the drains of two transistors are 180^0 phase shifted versions of each other. This structure can also be drawn as in Fig. 4.8.

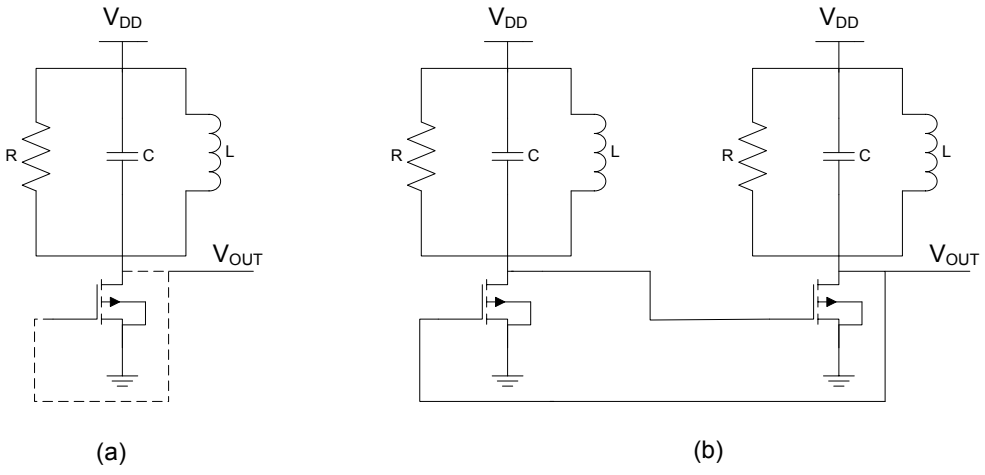


Figure 4.7 : (a) Single tuned stage (b) cascaded two tuned stages

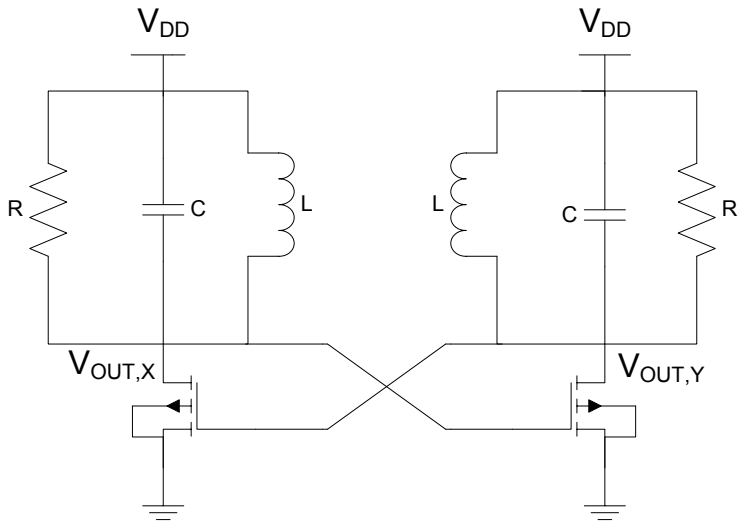


Figure 4.8 : Another drawing of cross coupled differential LC oscillator

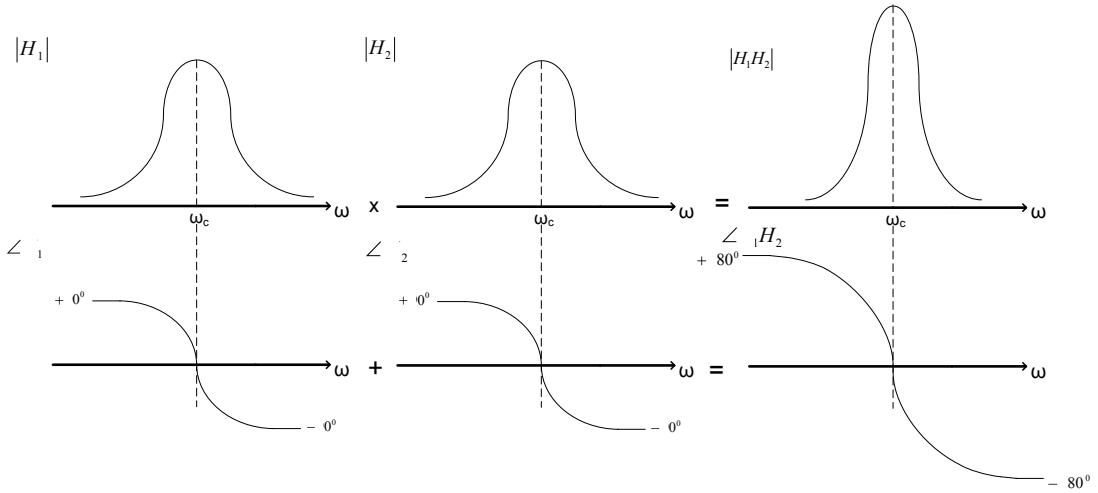


Figure 4.9 : Two stage total frequency response

If negative resistance model of differential oscillator is considered, from small signal point of view cross coupled NMOS part can be drawn as shown in Fig. 4.10 (b). Input resistance is calculated in (4.8) as $-2/g_m$ assuming that the transistors are identical. This negative resistance should compensate the resonator loss which can be denoted as a resistor R_p. Parallel combination of these impedances should be negative to build oscillation up. So $|R_{in}|$ should be less than or equal to R_p. This condition puts a restriction on g_m of the transistors as given in (4.10).

$$V_x = V_2 - V_1 = -I_x\left(\frac{1}{g_m} + \frac{1}{g_m}\right) \tag{4.7}$$

$$\frac{V_x}{I_x} = -\frac{2}{g_m} \tag{4.8}$$

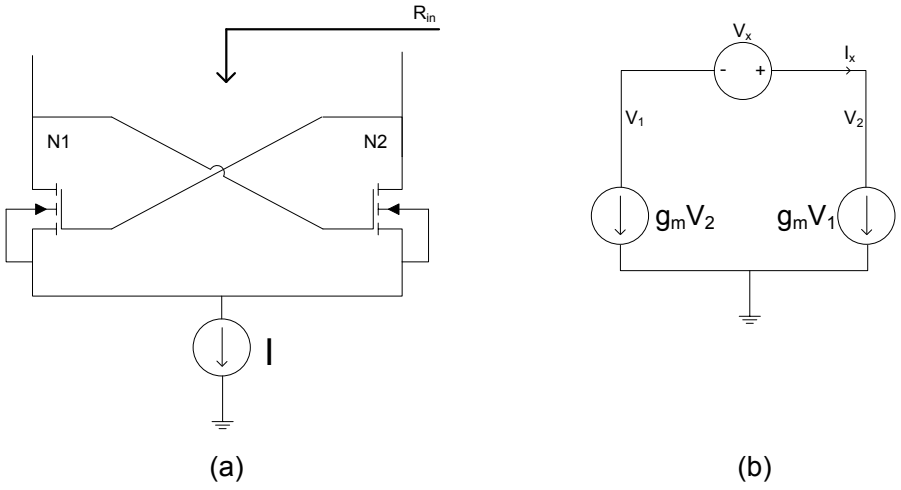


Figure 4.10 : (a) Differential NMOS part (b) small signal model

$$\frac{2}{g_m} \leq R_p \tag{4.9}$$

$$g_m \geq \frac{2}{R_p} \tag{4.10}$$

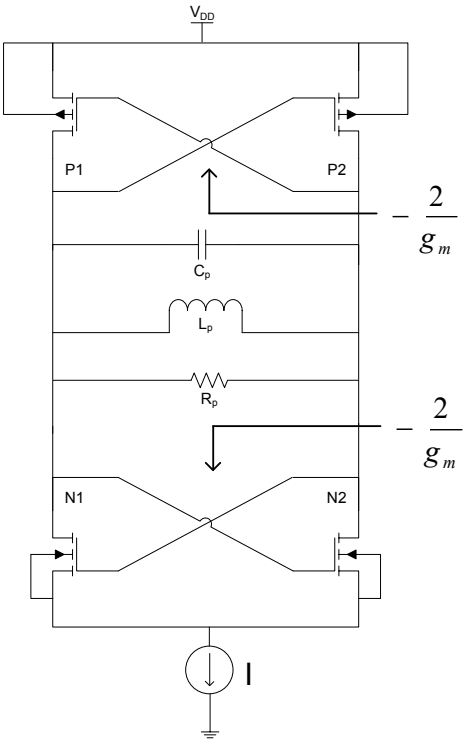


Figure 4.11 : Differential NMOS-PMOS topology

Another alternative is using both NMOS and PMOS pairs together as active part as shown in Fig. 4.11. Both differential pairs provide $-2/g_m$ assuming that transconductances of the all transistors are equal and have value g_m. Since the mobility of holes are less than the mobility of electrons, size of PMOS transistor should be larger than the size of NMOS counterpart to get same transconductance value [16] . So, basically same g_m can be achieved by selecting width of PMOS transistors two or three times the width of the NMOS counterparts and using the same technology in the fabrication. In this case equivalent input resistance is parallel combination of impedances shown by differential pairs which is $(-2/g_m)\,//\,(-2/g_m) = -1/g_m$. When oscillation build up condition is applied, it can be seen that new restriction on the transconductance is as given in (4.11). From here it can be deduced that in NMOS-PMOS cross coupled topology, g_m can be selected two times smaller than the one in NMOS only or PMOS only topologies. This implication means current consumption can be reduced by using both NMOS and PMOS differential pairs.

$$g_m \geq \frac{1}{R_p} \tag{4.11}$$

4.1.5.2 Single Transistor Oscillators

Single transistor configurations are commonly in Colpitts or Hartley oscillator forms as shown in Fig. (4.12). These oscillators have minor differences but mostly the same working principle. Colpitts oscillator employs capacitive feedback while Hartley uses inductive one. Since less number of inductors are used, Colpitts oscillator has less phase noise and smaller chip area. In previously mentioned single stage topology feedback was from drain to gate. This configuration was not satisfactory to start oscillation since total phase shift around the loop was 180^0. Idea behind the Colpitts oscillator is making feedback between drain and source which provides a total 360^0 phase shift. In the feedback path capacitor is employed to not to disturb DC operating point of the transistor.

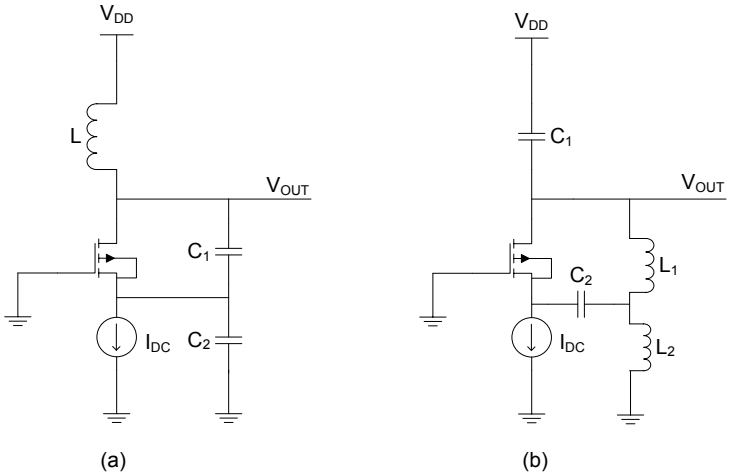


Figure 4.12 : (a) Colpitts oscillator (b) Hartley oscillator

Assuming a disturbing noise current incident on the source of the transistor and taking into account the parasitic resistance of the inductor, small signal equivalent circuit of the Fig. 4.12 (a) is drawn in Fig. 4.13. Closed loop transfer function is calculated in (4.12)[14].

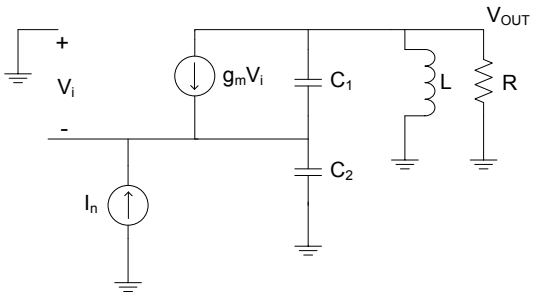


Figure 4.13 : Small signal equivalent circuit of Colpitts oscillator

$$\frac{V_{OUT}}{V_i} = \frac{RLs(g_m + C_1 s)}{RC_1C_2Ls^3 + (C_1 + C_2)Ls^2 + [g_mL + R(C_1 + C_2)]s + g_mR} \quad (4.12)$$

If closed loop transfer function goes to infinity at $s = jw_c$, circuit oscillates. Requirement is that at w_c both real and imaginary parts of the denominator must drop to zero as shown in 4.12 and 4.14.

$$-RC_1C_2Lw_c^3 + [g_mL + R(C_1 + C_2)]w_c = 0 \quad (4.13)$$

$$-(C_1 + C_2)Lw_c^2 + g_mR = 0 \quad (4.14)$$

Since g_m is very small when compared to typical values of L and C, $g_mL \ll R(C_1 + C_2)$ assumption is done to obtain 4.15 and 4.16.

$$w_c^2 = \frac{1}{L\frac{C_1C_2}{C_1 + C_2}} \quad (4.15)$$

$$g_mR = \frac{C_2}{C_1}(1 + \frac{C_1}{C_2})^2 \quad (4.16)$$

Minimum voltage gain g_mR is obtained as four when $C_1/C_2 = 1$. So we get a restriction as $g_mR \geq 4$ to maintain oscillation.

In CMOS technology, inductors generally suffer from low Q which means a low R_p value. Required minimum voltage gain of Colpitts oscillator puts a strict condition on g_m. This fact reveals a disadvantage of Colpitts oscillator compared to cross coupled differential LC oscillator. In that case minimum voltage gain was unity which means g_m can be selected four times less for NMOS only or PMOS only case and eight times less for NMOS-PMOS cross coupled case. Note that the previously assumed loss resistance R_p in differential topology was equivalent to $2R$.

4.1.5.3 Quadrature- Phase Balanced Oscillator

Quadrature phase generating oscillators are widely used for modulation, detection and image rejection in modern RF systems. In integrated circuit designs old technology for quadrature phase generation was passing signal from RC networks or RC poly-phase filters [17]. Today

technology is employing the cross coupled oscillators for the direct generation of multiphase signals. Considering recent works, it can be seen that there are small differences in implementations but logic behind them are almost the same. Basic topology in which the two differential oscillators are coupled together to generate quadrature output is given in Fig. 4.14.

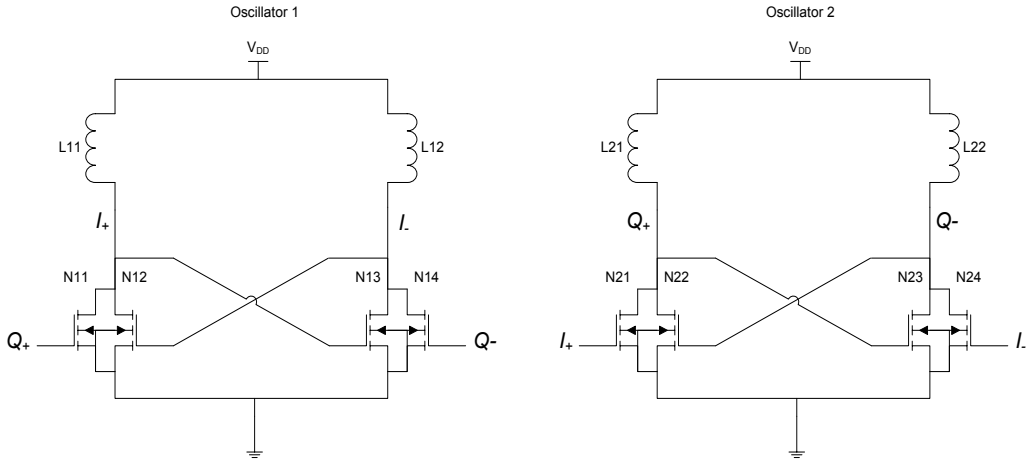


Figure 4.14 : Differential oscillators coupled for quadrature phase generation

In the structure, drains of the transistors in first oscillator are directly connected to the gates of the transistors in second oscillator while drains of the transistors in second oscillator are crossed connected to the gates of the transistors in first oscillator. If the oscillators are supposed to be in-phase, then the cross-coupled path from second oscillator to first absorbs the negative resistance current produced by N12 and N13 so first oscillator stops working. As a result drains of the transistors in the first oscillator are pulled up to V_{DD} which shuts off the second oscillator. Situation is similar when out of phase operation is assumed. So, oscillations can only occur when oscillators are synchronized in quadrature [18]. To mathematically prove this fact, consider the equivalent model of Fig. 4.14 which is given in Fig.4.15 [19]. Note that in the system G denotes transfer function of the each pair. This oscillatory system can be described by a set of linear homogenous equations in frequency domain given as:

$$\begin{bmatrix} -1 & mG & G & 0 \\ 0 & -1 & mG & G \\ G & 0 & -1 & mG \\ mG & G & 0 & -1 \end{bmatrix} \begin{bmatrix} X_1 \\ X_2 \\ X_3 \\ X_4 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{4.17}$$

Solving this system we can obtain the expressions in terms of X_1 as given in (4.18) and nontrivial solution of the system exists if determinant of the system matrix is zero which gives the roots in (4.20) and (4.21).

$$X_2 = \frac{2mG^2 + m^3G^3}{1 - G^2 - m^2G^3} X_1$$

$$X_3 = \frac{G + m^2G^2 - G^3}{1 - G^2 - m^2G^3} X_1 \tag{4.18}$$

$$X_2 = \frac{mG + mG^3}{1 - G^2 - m^2G^3} X_1$$

$$1 - 2G^2 - 4m^2G^3 + (1 - m^4)G^4 = 0 \tag{4.19}$$

$$G_{1,2} = \frac{1}{1 \pm m} \quad , \quad G_{3,4} = \frac{-1}{1 \pm jm} , \qquad for \;\; m^2 \neq 1 \tag{4.20}$$

$$G_1 = \frac{1}{2} \quad , \quad G_{2,3} = \frac{-1 \pm j}{2} , \qquad for \;\; m^2 = 1 \tag{4.21}$$

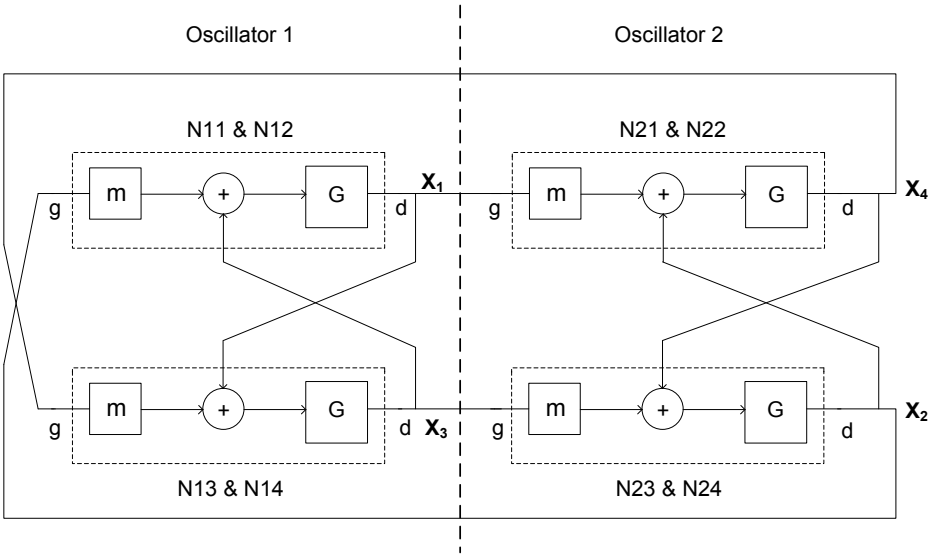


Figure 4.15 : Equivalent model of quadrature phase generator system

Substituting the *G* values in (4.18), expressions take the form (4.22) which proves the quadrature phase generation.

$$X_k = X_1 e^{(k-1)j\frac{\pi}{2}} \qquad k = 1,2,3 \tag{4.22}$$

Latest works present new quadrature oscillator topologies. From the phase noise point of view injection-locked oscillator gives good results [20]. Quadrature phase generator employing coupled tail injection locked oscillators is shown in Fig. 4.16.

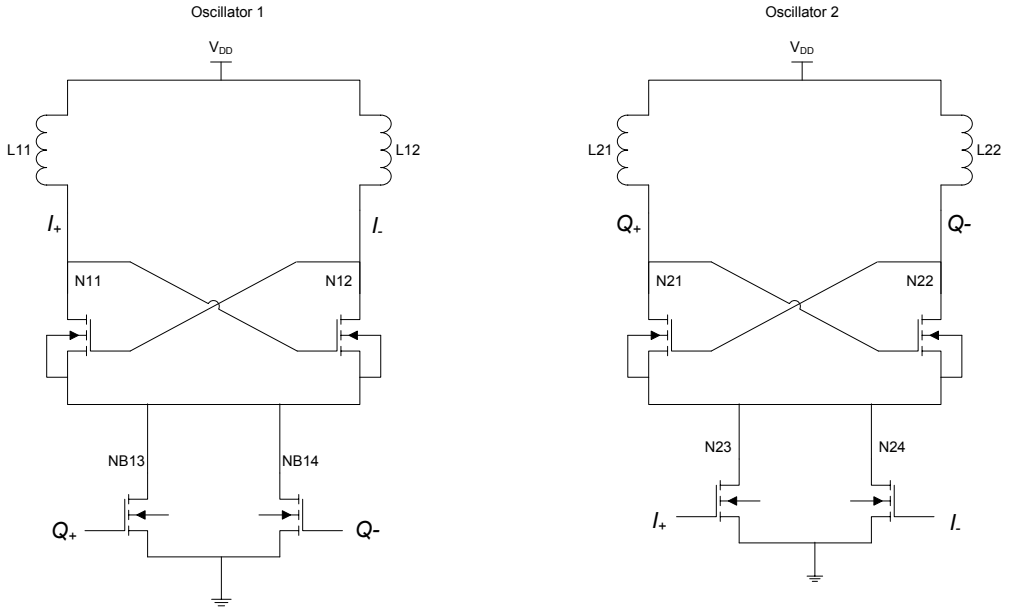


Figure 4.16 : Differential tail injection quadrature oscillator

Operation principle depends on injection locked frequency divider theory [20]. Differential injection signals oscillating at w_0 are fed to the tail biasing transistors of the dual structures. This creates oscillation at $2w_0$ at common source terminals which in turn generates output signal oscillating at w_0. Injection locking also provides 90^0 phase shift among all output signals.

4.1.5.4 Comparison and Evaluation of LC Oscillator Topologies

In 4.1.5, some common LC oscillator topologies are explained. Each topology has advantages and disadvantages considering the evaluation criteria. Generally choices depend on the application. Also several versions within selected topology must be considered for finest performance.

Actually any LC oscillator, containing large on chip inductor, cannot be as compact as ring oscillators which are not preferred in RF applications due to their noisy nature. In some studies in order to make oscillator compact, instead of passive inductors active inductors

originating from gyrators are used but while minimizing the structure active inductors bring important problems including power consumption and noise [21].

Although single transistor structures are easier to implement, they have some important drawbacks. First, they can only provide single ended output which fails to operate with modern mixers having double balanced structures requiring differential signals. Second, common mode noise cannot be eliminated by the structure and contributes to the phase noise of the oscillator. Lastly as analyzed there is a strict condition on g_m of the transistor for the satisfaction of oscillation start-up.

Specified problems associated with single transistor topology are mostly solved in the differential one. Differential oscillators can provide differential output to be used in modern double balanced mixers. Also by its nature subtracting differential signals from each other common mode noise can be eliminated which means an improvement on the phase noise performance. Another improvement is the elimination of the even harmonics. Remember that in any balanced circuit, even harmonics flow in the common path and odd harmonics flow in the differential path. Since in the common mode symmetry plane is a virtual open circuit, ideally even harmonics cannot find a path to flow which intrinsically provides elimination of even harmonics. As mentioned in the analysis, condition on the g_m of the transistors are also relaxed in the differential topologies compared to the single one. Today, popular oscillators are mostly in the differential form.

In single transistor oscillator or in single pair differential oscillator cases, LC resonators are used as loads connecting transistors to V_{DD} or ground according to their configuration. In these cases oscillation peak to peak voltage swing can exceed V_{DD} [14]. For example consider a single NMOS transistor case. DC bias is around V_{DD} if the parasitic resistance of the inductor is small. Output voltage is expected to be inverted and amplified version of the noise signal at the resonance frequency. If the average value of oscillation significantly varies from V_{DD}, parasitic resistance of the inductor should carry an average current higher than bias value. So voltage swing can exceed supply voltage.

Differential oscillators can be in NMOS only, PMOS only or in CMOS form. PMOS transistor has lower flicker noise than the NMOS counterpart so for low phase noise applications PMOS transistors are generally preferred but as mentioned in differential oscillator part, size of the PMOS transistor should be nearly three times the size of the NMOS transistor to achieve same transconductance. Differential oscillators show better

phase noise performance when compared to single ended ones by providing better power supply and substrate noise rejection [35]. These noise sources can be accepted as common mode noise sources. Employing both NMOS and PMOS transistors CMOS oscillators show full symmetry which eliminates the common mode noise more effectively. Also for the same power consumption, active circuit shows a negative resistance twice as large as single differential pair versions which makes it indispensible for low power applications. Despite these advantages there are some disadvantages with CMOS core. One of these is about phase noise. Adding one more pair to the oscillator causes extra flicker noise which consequently contributes to the phase noise. Considering the improvement coming from the fully symmetric topology, a careful optimization is required for the effective advancement of the phase noise performance. Notwithstanding, since voltage swing is limited to the operation ranges of the transistors up to the cut-off regions, it cannot exceed supply voltage which can be achievable in single pair topologies.

Classical quadrature balanced oscillators have no significant phase noise improvement over single stage differential oscillators but injection locked quadrature structures have some advantages. Although they use more elements which contribute to noise, injection locked quadrature oscillators reduce the low frequency noise due to tail transistors by modulating the bias voltage of the tail which in turn provides reduced phase contribution of the tail biasing transistors [22]. Also using two LC resonators filters sideband noise more powerfully and more symmetrically compared to the single resonator. As a result signal-to-noise ratio is increased [23].

Although there exist oscillators that biasing circuitry is not used, in most of the practical oscillators current mirrors composed of NMOS or PMOS transistors are used as biasing network. Main reason to use a biasing network is easy control on the operation point and power consumption. By this way oscillator can be operated in current limited region that reduces harmonics. Although NMOS current mirrors provide better characteristics due to their property that they are better approximate to ideal current source, PMOS current mirrors are claimed to be achieving lower phase noise due to their low flicker noise contribution compared to the NMOS counterpart [24],[25]. Totally eliminating the biasing circuit may sometimes be advantageous but actually control on the current consumption and operating point is lost because oscillator works in voltage limited region.

4.2 Voltage Controlled Oscillator

As stated in the overview section, in most of the applications tunable oscillators are required. Straightforward and effective way of making oscillator tunable is varying the capacitance of the resonator by changing the voltage on it so that resonance frequency is adjusted. This type of capacitances are generally called varactors and implemented by using reverse biased p-n junctions. All types of oscillators given in the previous part can be made voltage controlled by using varactor diodes or transistors as capacitors. Frequency characteristics of a VCO can be modeled and shown as given in (4.23) and Fig 4.17. K_{VCO}(rad/V) denotes the frequency sensitivity of the system.

$$\omega = \omega_0 + K_{VCO}V_{control} \tag{4.23}$$

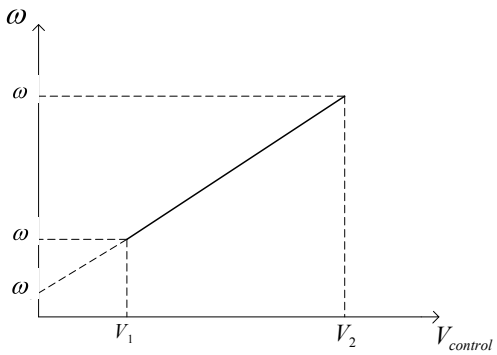


Figure 4.17 : Typical VCO frequency characteristics

Mathematical modeling of VCO characteristics [14] starts with the fact that if the phase of the signal varies faster, frequency increases which suggests writing frequency as the derivative of the phase with respect to time or expressing phase as the integral of the frequency as given in (4.24) and (4.25).

$$\omega = \frac{d\emptyset}{dt} \tag{4.24}$$

$$\emptyset = \int \omega dt + \emptyset_0 \tag{4.25}$$

Substituting (4.23) in (4.25) and defining the output waveform as $V_{out} = V\cos\emptyset(t)$, $V_{control}$ and output waveform relation is obtained as given in (4.26). Unimportant initial phase component $\emptyset_0$ may be dropped in the calculations.

$$V_{out}(t) = \mathrm{V}\cos\left(\omega_0 t + K_{VCO}\int V_{control}dt + \emptyset_0\right) \tag{4.26}$$

$V_{control}$ is assumed to be very stable DC value in the ideal operation and when variations in this voltage occur undesired frequency components appear in the output spectrum. In order to avoid these components, control voltage must experience very little variations.

Actually oscillator outputs have significant harmonics and in some applications these harmonics are used as desired frequency output by filtering other harmonics. In VCO modeling these harmonics can be taken into account by using Fourier series expansion and by modifying (4.26) as [14]:

$$\begin{aligned} V_{out}(t) = {} & \mathrm{V}_1\cos\left(\omega_0 t + K_{VCO}\int V_{control}dt\right) + \mathrm{V}_2\cos\left(2\omega_0 t + 2K_{VCO}\int V_{control}dt\right) \\ & + \mathrm{V}_3\cos\left(3\omega_0 t + 3K_{VCO}\int V_{control}dt\right) \\ & + \cdots \end{aligned} \tag{4.27}$$

In the assessment of VCO there are some important performance criteria that determine its specifications. First one is the tuning range. Tuning range is mostly determined by the frequency sensitivity related with the used varactor and generally set by the frequency range necessary for the application. MOSFET varactors are able to yield higher tuning sensitivity and in turn wider tuning range when compared to the diode varactors.

Second important characteristic is the phase noise. Basically phase noise is a measure of short term frequency instabilities of the system and very important for RF applications. It is also called as "jitter" in the time domain. There are various concepts about phase noise but basically lowering the frequency sensitivity makes system less sensitive to noise at the same time which yields less phase noise. In that sense tuning range and phase noise are struggling parameters which need to be optimized depending on the application. Also increasing output voltage swing lowers noise sensitivity improving the phase noise characteristics. Phase noise concept will be discussed later in detail.

Another parameter is tuning linearity. Different from the ideal characteristics given in Fig. 4.17, in practice tuning characteristics of the VCO exhibits nonlinearity, i.e slope of $\omega - V_{control}$ curve is not constant in the whole tuning range. Since this nonlinearity degrades the settling behavior of PLLs, slope variations should be minimized and VCO should be as linear as possible.

Last critical parameter is the power dissipation. As usual there exists a trade-off between the power dissipation and noise characteristics. Increasing power dissipation increases voltage swing which improves the phase noise. In recent applications power dissipation is as important as phase noise so people work on smarter ways of decreasing phase noise while keeping power dissipation low.

4.3 CMOS Cross-Coupled Differential VCO Design

This work mainly focuses on the low phase noise and low power consumption oscillator design. From the discussions made in oscillator topologies section most suitable is selected as the differential cross coupled one. The design phase is split into three main parts namely active circuit, resonator and biasing circuit. In a systematic design all parts should be handled separately and then combined together for the final tests and optimization. Performance and quality of the oscillator are mostly determined by the resonator which consists of the inductor and the varactor. Active circuit is designed to compensate the resonator loss and operating points of its transistors are adjusted by the biasing circuit. As mentioned before biasing circuit also provides flexibility on the working regime of the oscillator by enabling current limited operation. In the next sections design and implementation details of each part in CMOS technology will be discussed.

4.3.1 Resonator (Tank Circuit)

Resonators are generally in series or parallel LC form determining the oscillation frequency as $\omega_0 = 1/\sqrt{LC}$. As the name implies it consists of an inductor generally implemented as on chip spiral inductor and a varactor made by using p-n junctions. The most important parameter of a resonator is its quality factor. Q factor is simply defined as the ratio between stored energy in inductor-capacitor pair and the dissipated energy in parasitic resistance of the tank. Q factors of each component can be calculated separately and then combined to get total Q factor. Using the energy storage values of capacitor $X_C = 1/\omega C$ and inductor $X_L = \omega L$, Q factors can be calculated as given in (4.28) and (4.29).

$$Q_C = \omega_0 R_{pr} C \tag{4.28}$$

$$Q_C = \frac{\omega_0 L}{R_{sr}} \tag{4.29}$$

where ω_0 is the center frequency, R_{pr} is the parallel modeled resistance of the capacitor and R_{sr} is the series modeled resistance of inductor. The total Q factor Q_R is calculated using the equation given as:

$$\frac{1}{Q_R} = \frac{1}{Q_L} + \frac{1}{Q_C} \tag{4.30}$$

Although Q factor of bondwire inductors are quite high (~50) , in most of today's applications on chip spiral inductors are widely used due to their ease of packaging . In recent technology their Q factors can be as high as 15 [26] while that of capacitors can reach 300 [27]. In that sense determinative component of Q factor of a resonator is its inductor.

4.3.1.1 Inductor

Inductor is the key component of an oscillator determining its performance. Although different designs using off-chip or bondwire inductors are tried to improve performance by increasing quality factor, still fully integrated topologies are preferred to achieve compact design. Two main options are active and on chip spiral inductor topologies. Active inductors, shown in Fig. 4.18, employ gyrators working together with a capacitor adjusting the inductance as $L = C/g_{m1}g_{m2}$ [28].

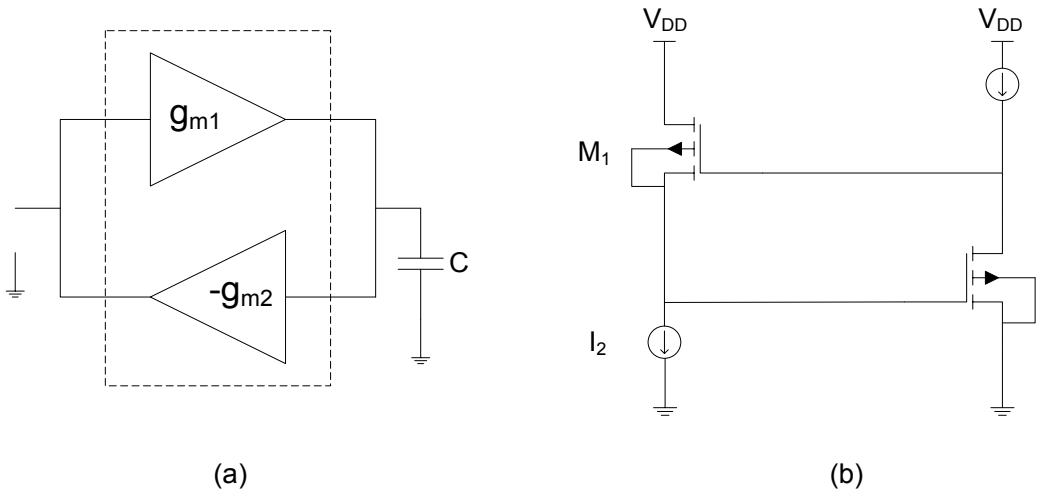


Figure 4.18 : (a) Active inductor employing gyrators (b) simplest gyrator topology

Another alternative is on chip spiral inductor implemented by a spirally aligned transmission line. It can be in rectangular, circular or polygonal shape. Widely used one is the rectangular spiral inductor that is shown in Fig. 4.19. Various equivalent circuit models for this spiral inductor [29] and enhanced ones [30] exist in the literature. These models include ideal

resistors, inductors and capacitors expressed by the layout design parameters of the inductor namely width of the metal w, space between metal lines s, number of turns N, internal spacing d_{in} and external spacing d_{out}.

In some of the studies differential active inductors are claimed to have very high quality factors , i.e around 70 [31]. However in practice, adding extra transistors to the structure increases noise, distortion and power consumption. Thus passive on chip spiral inductors are generally used in oscillator designs and its value is selected as low as possible to not to degrade phase noise performance.

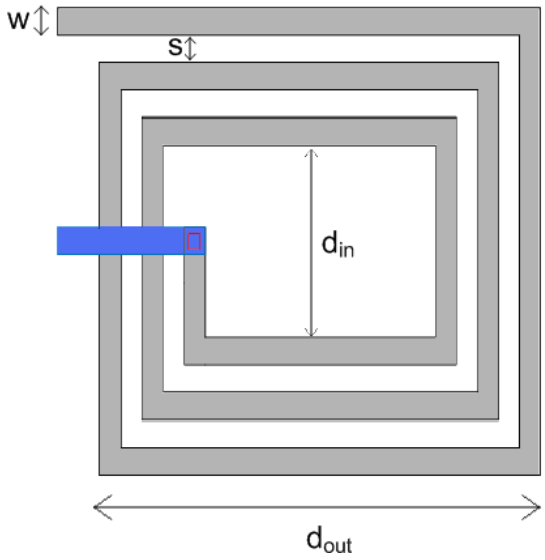


Figure 4.19 : Rectangular spiral inductor

Spiral inductor faces two main loss mechanisms. First one is resistive loss due to the finite conductivity of metal wire. Finite conductivity causes resistive effect that is directly proportional to length and inversely proportional to conductivity, width and effective thickness. At high frequencies this effect is even stronger due to skin effect and "current crowding" seen at the corners [32]. Second mechanism is substrate loss which is caused by the parasitic current flows in the substrate. Coupling between metal and Si substrate via insulating SiO_2 layer creates displacement current which flows through the substrate. Also Eddy currents flow in the substrate resulting from time varying magnetic field. Remembering that the resistivity of Si substrate can be as high as 20 Ω-cm which is much higher that that of GaAs counterpart so, these currents create significant losses.

Inner turns of a spiral inductor have negligible contribution to the inductance but increase the loss by adding extra metal wires and strengthening the parasitic current flow through substrate. Thus, easiest and widely used way to decrease losses and increase quality factor is using hollow spiral inductors that omit innermost turns. Another option to decrease loss is etching the substrate present below the inductor so that parasitic current flow through substrate is avoided. Although etching is very effective this method is not widely used since it is a nonstandard CMOS process.

4.3.1.2 Varactor (Voltage Variable Capacitor)

Varactor is the tuning element in the oscillator. Basically a reversed biased diode (p-n junction), illustrated in Fig. 4.20, can serve as varactor. Junction capacitance is inversely proportional to width of depletion region width W. Increase in the reverse bias voltage also increases W resulting a certain decrease in the junction capacitance. Capacitance- voltage relation of this structure is as given in (4.31) and typical characteristic is plotted in Fig. 4.21 [14]. In the equation C_0 stands for zero bias capacitance, V_r is reverse bias voltage and $\emptyset_B$ denotes the built in potential of the junction. For CMOS technology "m" is between 0.3 and 0.4.

$$C_{var} = \frac{C_0}{\left(1 + \frac{V_r}{\emptyset_B}\right)^m} \tag{4.31}$$

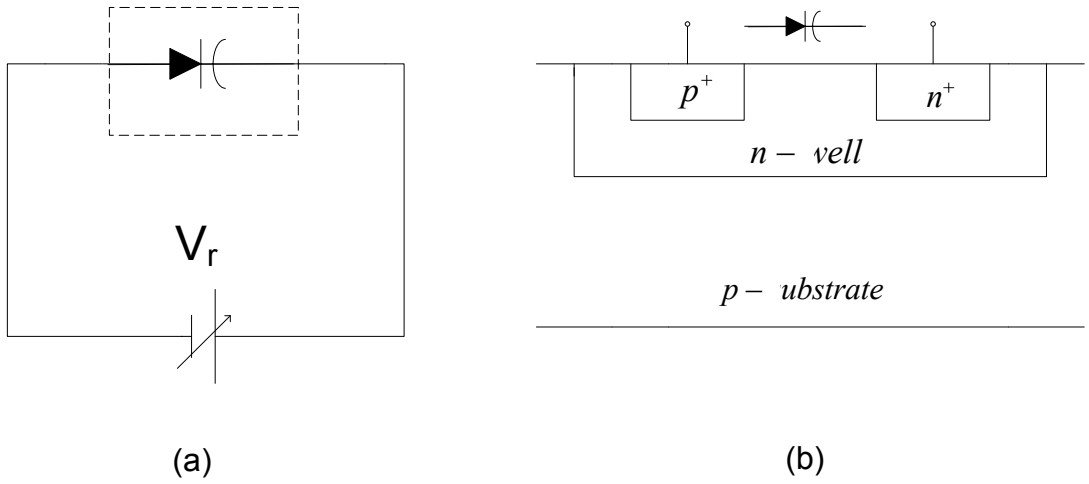


Figure 4.20 : (a) Reverse biased diode based varactor (b) CMOS realization of varactor diode

Diode based varactor has an important trade-off problem between tuning range and voltage swing. As the voltage swing increases, allowable range of applied voltage decreases to avoid diode from forward bias. This in turn limits the tuning range.

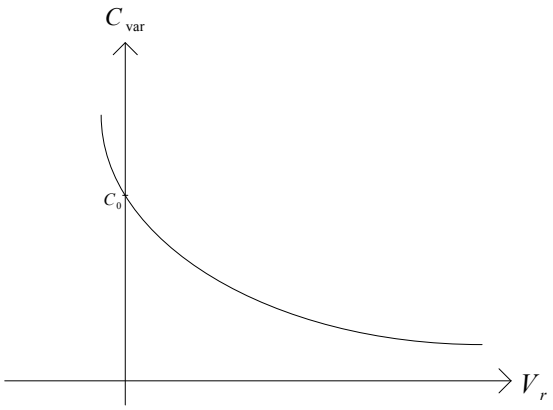


Figure 4.21 : Capacitance-voltage characteristic of the diode based varactor

An alternative varactor device is obtained by varying the gate capacitance of MOS transistor. MOS varactor is obtained by forming a capacitor between drain, source and bulk connected together and gate of the transistor. Realization is as shown in Fig. 4.22. Capacitance of this structure shows non-linear dependence on bulk-to-gate voltage V_{BG} as illustrated in Fig. 4.23. Detailed analysis and information about the operation can be found in text book [33]. MOS varactors are generally operated in weak and moderate inversion regions where V_{BG} is greater than the threshold voltage of the transistor V_T because of the linearity and tuning range issues but there also exist some works in which depletion region is used.

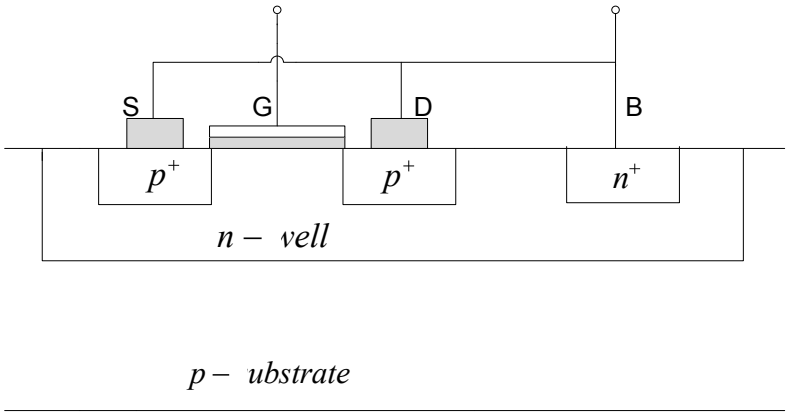


Figure 4.22 : Realization of the MOS varactor

MOS varactor is advantageous over diode varactor in the following respects [34]. First, capacitance curve of a MOS varactor has steeper and more linear characteristics than that of a diode varactor. Also MOS varactor has wider tuning range because of the reversed biased operation restriction of diode varactor. Second, when approaching to forward bias boundary Q-factor of a diode varactor drops very quickly which increases phase noise. Third, MOS varactor has larger maximum capacitance per unit area when compared to zero biased diode varactor. Therefore, MOS varactor is more popular in recent oscillator projects. From phase noise point of view, one disadvantage of MOS varactor is that it brings larger tuning gain K_{VCO} to the oscillator which makes it more sensitive to noise sources.

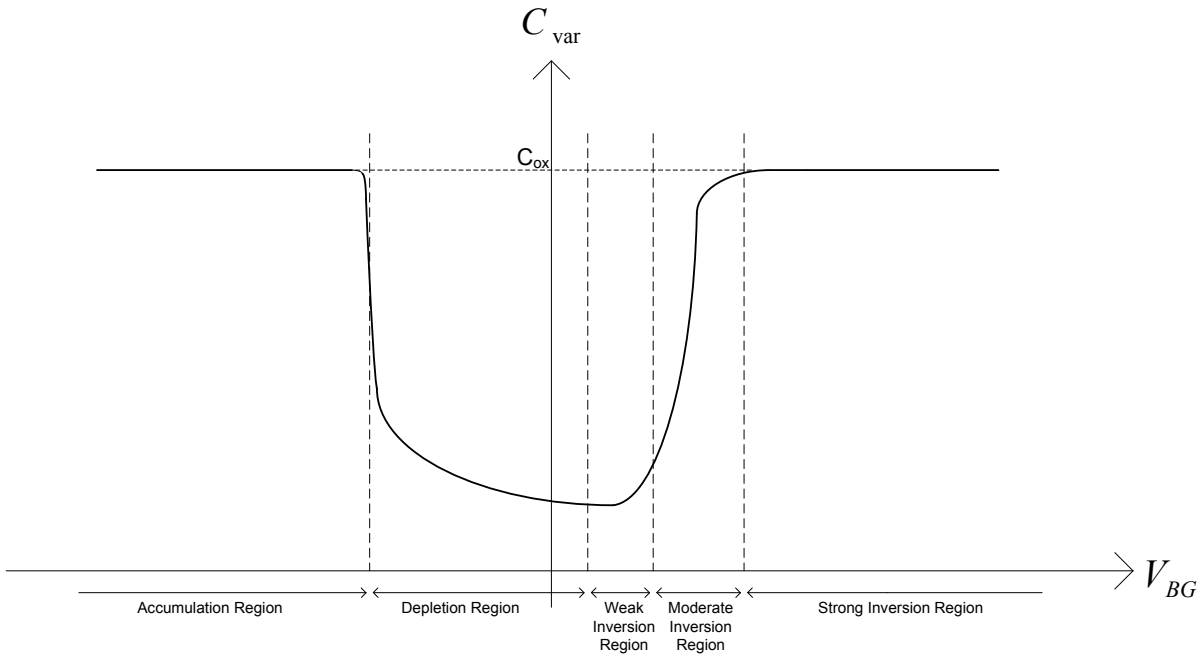


Figure 4.23 : Capacitance-Voltage characteristic of the MOS varactor

4.3.2 Active Circuit

Active circuit is composed of transistors. In RF circuits transistors are generally serve amplifiers, in oscillators they are used to compensate loss to maintain stable oscillation. Simple oscillators have single transistor as the active part but differential structures consist of at least two transistors. An example circuit composed of NMOS transistors is shown in Fig. 4.24. Detailed analysis of the circuit in this figure was done in cross coupled LC oscillator section.

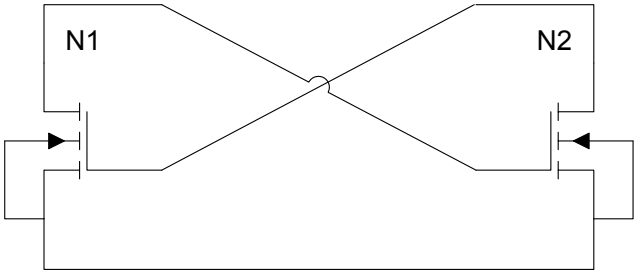


Figure 4.24 : Differential cross coupled active circuit topology

Mainly there are two transistor types FET (Field Effect Transistor) and BJT (Bipolar Junction Transistor) both of which exist in standard CMOS technology. Negative resistance shown by the active part is mainly adjusted by the transconductance g_m of the transistors. Typical I-V characteristics of an NMOS FET and a NPN BJT are shown in Fig. 4.25. In the ideal operation, FET is biased at saturation region and BJT is biased in the linear region but in practice transistors experience all the regions in a single oscillation period because of the periodic voltage change at the drain port of FET and collector port of BJT. This situation causes some problems which will be discussed later in the phase noise part.

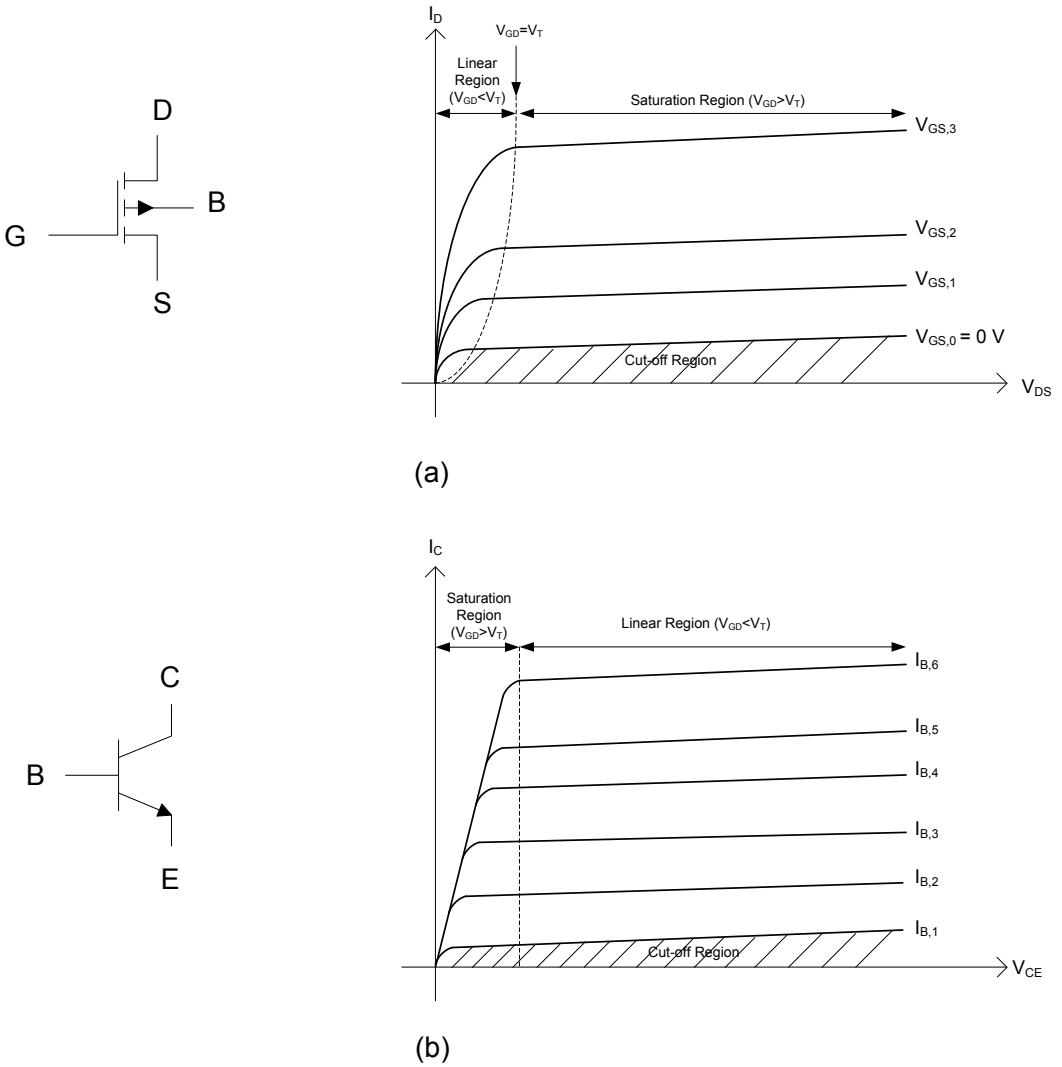


Figure 4.25 : I-V characteristics of (a) an NMOS FET and (b) an NPN BJT

BJT has less flicker noise than FET and also it can operate at higher frequencies but when power dissipation and production cost is considered FET is preferable. Today majority of ICs are fabricated using CMOS (Complementary Metal-Oxide Semiconductor) technology which consists of both n-type and p-type MOSFETs. Most important characteristic of CMOS transistor is its low power consumption.

4.3.3 Bias Circuit

Standard bias circuits used in oscillators are current mirrors composed of NMOS or PMOS FETs. A typical single stage NMOS current mirror is shown in Fig. 4.26. Transistors in current mirrors are generally operated at the saturation region where the drain current can be

written in terms of gate-to-source voltage V_{GS}, technology related parameter K_p, width W and length L of the transistor as:

$$I_d = \frac{1}{2} K_p \left(\frac{W}{L}\right) (V_{GS} - V_{th})^2 \tag{4.32}$$

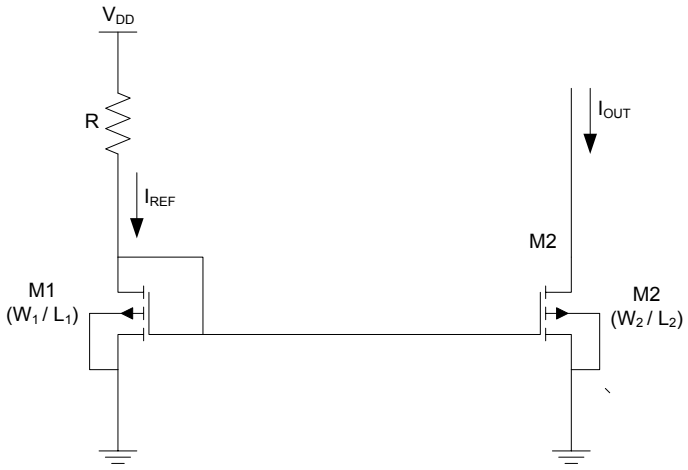


Figure 4.26 : Single stage NMOS current mirror

Basically I_{REF} is adjusted by V_{DD} and R. By the nature of the structure both transistors are biased with the same V_{GS} and copying ratio is adjusted by W and L of the transistors as:

$$I_{OUT} = \frac{W_2/L_2}{W_1/L_1} I_{REF} \tag{4.33}$$

Output resistance of the single stage NMOS current mirror is calculated as given in (4.34). In this equation λ stands for channel length modulation parameter of the transistor. For the oscillator design output resistance of the biasing circuit is very critical so that it should be as high as possible approximating to ideal case for better phase noise performance.

$$r_0 = \frac{1/\lambda + V_{DS}}{I_{DS}} \tag{4.34}$$

In practice generally tail biasing with NMOS current mirror is used as biasing circuit since it is a better approximate to ideal current source than PMOS counterpart however as stated before there are also some studies claiming that top biasing with PMOS current mirror gives better performance because PMOS transistor has lower flicker noise than NMOS transistor.

CHAPTER 5

PHASE NOISE IN VOLTAGE CONTROLLED OSCILLATORS

5.1 Noise Sources in Electronic Systems

5.1.1 Thermal Noise

Thermal noise, also known as Johnson-Nyquist noise [35],[36], is the electronic noise generated by thermal motion of the charge carriers in a conducting medium regardless of the presence of any DC source. This noise shows a white noise behavior that is constant in the whole spectrum. In any conducting medium thermal noise can be modeled as a voltage source in series with ideal resistive component presenting a power spectral density given in 1.1 where k is the Boltzmann's constant in joules per Kelvin; T is the absolute temperature in Kelvin; R is the resistance value and Δf represents the system bandwidth.

$$\frac{\overline{v^2}}{\Delta f} = 4kTR \tag{5.1}$$

Active devices also have thermal noise. Dominant thermal noise component in BJT's is base spreading resistor R_b and in MOSFET's channel resistance. Spectral density modelings are given in (5.2) and (5.3) respectively.

$$\frac{\overline{v^2}}{\Delta f} = 4kTR_b \tag{5.2}$$

$$\frac{\overline{v^2}}{\Delta f} = \frac{2}{3}\frac{1}{g_m}4kT \tag{5.3}$$

Note that g_m is the transconductance of the MOSFET and $^2/_3$ term is only valid for long channel devices. For smaller MOSFETs this term should be larger [37].

A capacitor, if the parasitic resistance is taken into account, behaves like an RC filter which has a bandwidth $1/4R_pC$ [37]. When we substitute this into (5.1) we get the thermal noise of a capacitor as given in (5.4) .

$$\overline{v^2} = \frac{kT}{C} \tag{5.4}$$

Since R eliminated in this expression thermal noise of a capacitor is generally referred as kTC noise.

5.1.2 Shot Noise

Shot noise is the electronic noise caused by the current carrying discrete charges namely electrons. When electrons give rise to random fluctuations in a conducting medium, shot noise effect can be observed. Main reason is that individual electrons arrive at a junction at random times [38]. The magnitude of this noise increases with the intensity of the DC current and spectral density is modeled as given in (5.5). Note that similar to thermal noise, shot noise also shows white noise characteristics.

$$\frac{\overline{I^2}}{\Delta f} = 2qI_{DC} \tag{5.5}$$

In MOSFETs current flowing through channel; in BJTs collector current are the dominant sources of shot noise and spectral densities can be modeled by replacing I_{DC} with I_D and I_C respectively.

5.1.3 Flicker Noise

In electronics, flicker noise is the low frequency noise which exists in all active devices as well as some passive components. This noise is also known as $1/f$ noise since its spectrum varies as $1/f^{\alpha}$ where α is very close to unity. Physics of this noise is not exactly known today and it is still a research topic. Up to now, studies show that origins of flicker noise in various media can be quite different. In electronic systems, flicker noise spectral density can be modeled as given in (5.6) where i_k stands for flicker noise strength.

$$\frac{\overline{I^2}}{\Delta f} = i_k \frac{1}{f} \tag{5.6}$$

As expected, flicker noise is effective in low frequencies as shown in Fig. 5.1 in logarithmic scale. In practice impact of this noise can be seen up to a certain frequency where noise floor is reached.

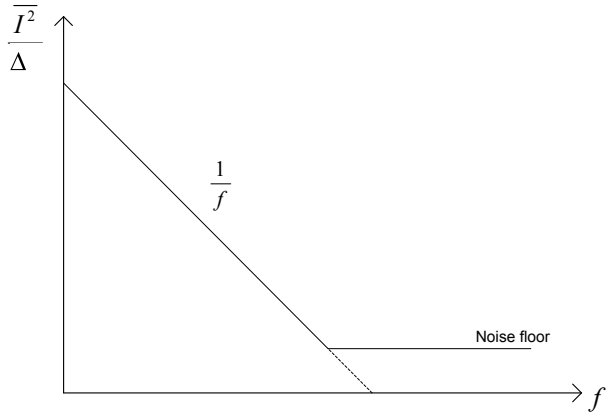


Figure 5.1 : Flicker noise spectrum

From the phase noise point of view, most troublesome noise is flicker noise. Different techniques that are developed to suppress this noise will be studied later. Note that in between active devices, MOSFETs generate more flicker noise than JFETs and for lowest flicker noise BJTs are preferred compromising low power dissipation [39].

5.2 Phase Noise

An oscillator is expected to have impulsive frequency characteristics in the ideal case but in practice, due to the inherent noise sources in the system, sidebands appear close to the center frequency as shown in Fig. 5.2. These sidebands are generally referred as phase noise.

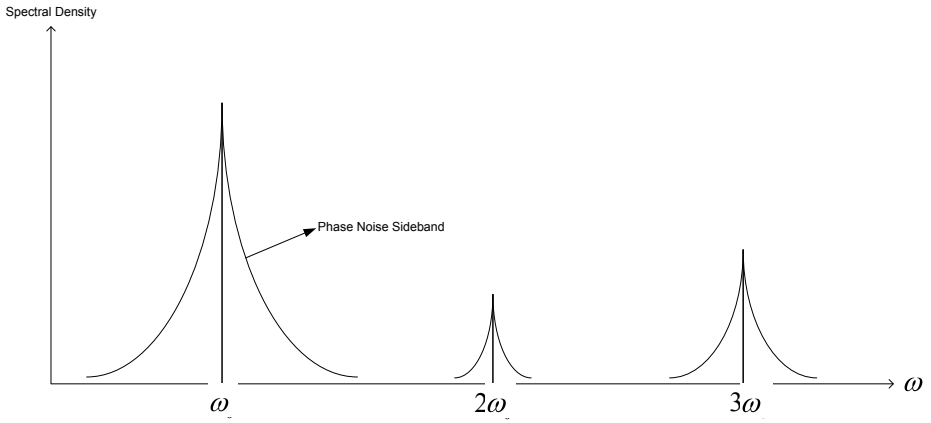


Figure 5.2 : Output spectrum of a practical oscillator

This phenomenon is best explained using phasor notation. In the oscillator, noise can be considered as random FM or AM modulation imposed on the main oscillation signal which is an ideal sine wave. Since the imposed noise have random phase and amplitude, phasor diagram is used to visualize the effect as shown in Fig. 5.3(a). In the figure, few noise vector samples are shown. In the actual case, many of these vectors exist corresponding to random phase and random amplitude noise at many frequencies. So, total effect can be defined as an uncertain area as shown in Fig 5.3(b).

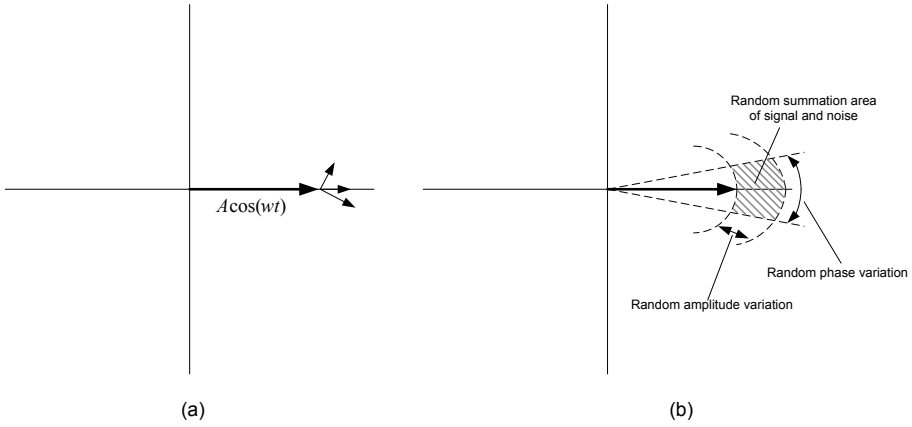


Figure 5.3 : (a)Random noise vectors imposed on the carrier (b) uncertain region corresponding to many random noise vectors imposed on the carrier

In most of the circuits, noise is generally represented as voltage source and due to the randomness it is characterized in statistical terms in RMS voltage which obeys Gaussian

probability distribution with mean μ and variance σ^2 as given in (5.7) and shown in Fig. 5.4. This distribution also shapes the spectrum of the oscillator.

$$f_X(x) = \frac{1}{\sqrt{2\pi}\sigma} exp\left[-\frac{(x-\mu)^2}{2\sigma^2}\right], \qquad -\infty < x < \infty \tag{5.7}$$

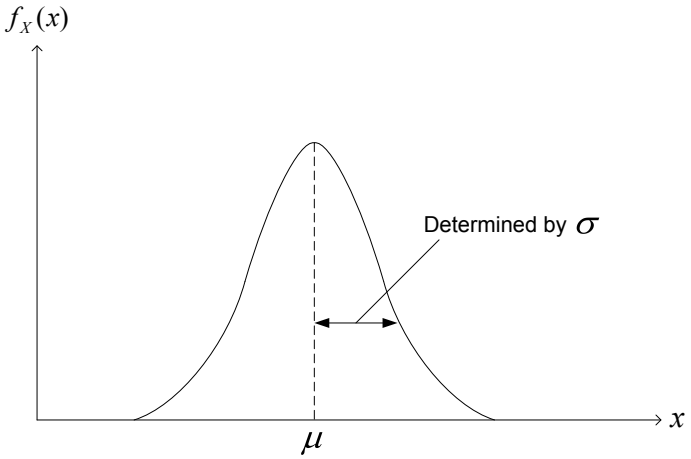


Figure 5.4 : Gaussian probability distribution function

Phase noise is generally measured as single sideband noise spectral density with unit dBc/Hz and it is defined as noise power in 1 Hz band at $\Delta\omega$ offset from the carrier divided by the carrier power as given in (5.8) and illustrated in Fig. 5.5.

$$L(\Delta\omega) = 10\ log\left[\frac{P_{sideband}(\omega_0 + \Delta\omega, 1\ Hz)}{P_{carrier}}\right] \tag{5.8}$$

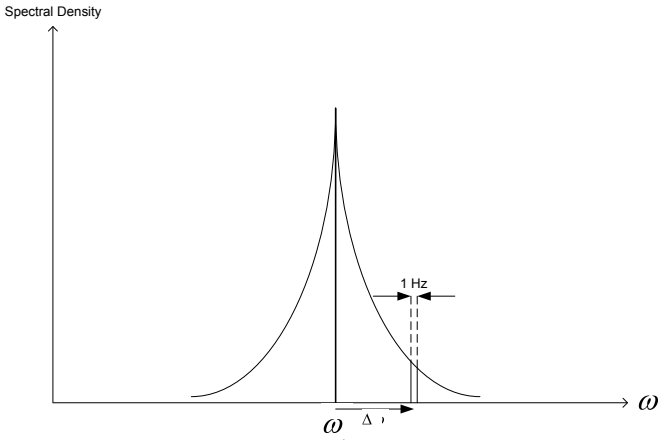


Figure 5.5 : Phase noise measurement illustration

In modern wireless communication systems, channel spacing can be as narrow as few hundred kHz while the carrier frequencies may go up to GHz levels. Under these circumstances phase noise may have destructive effects as illustrated in Fig. 5.6. Both in transmitter and receiver sides, unwanted signals may fall into the desired signal's band and mask even completely absorb it due to the spreading of the local oscillator's output spectrum. It is apparent from these discussions that local oscillator should have extremely sharp frequency characteristics considering that phase noise of this oscillator is directly effective on the modulation or demodulation quality.

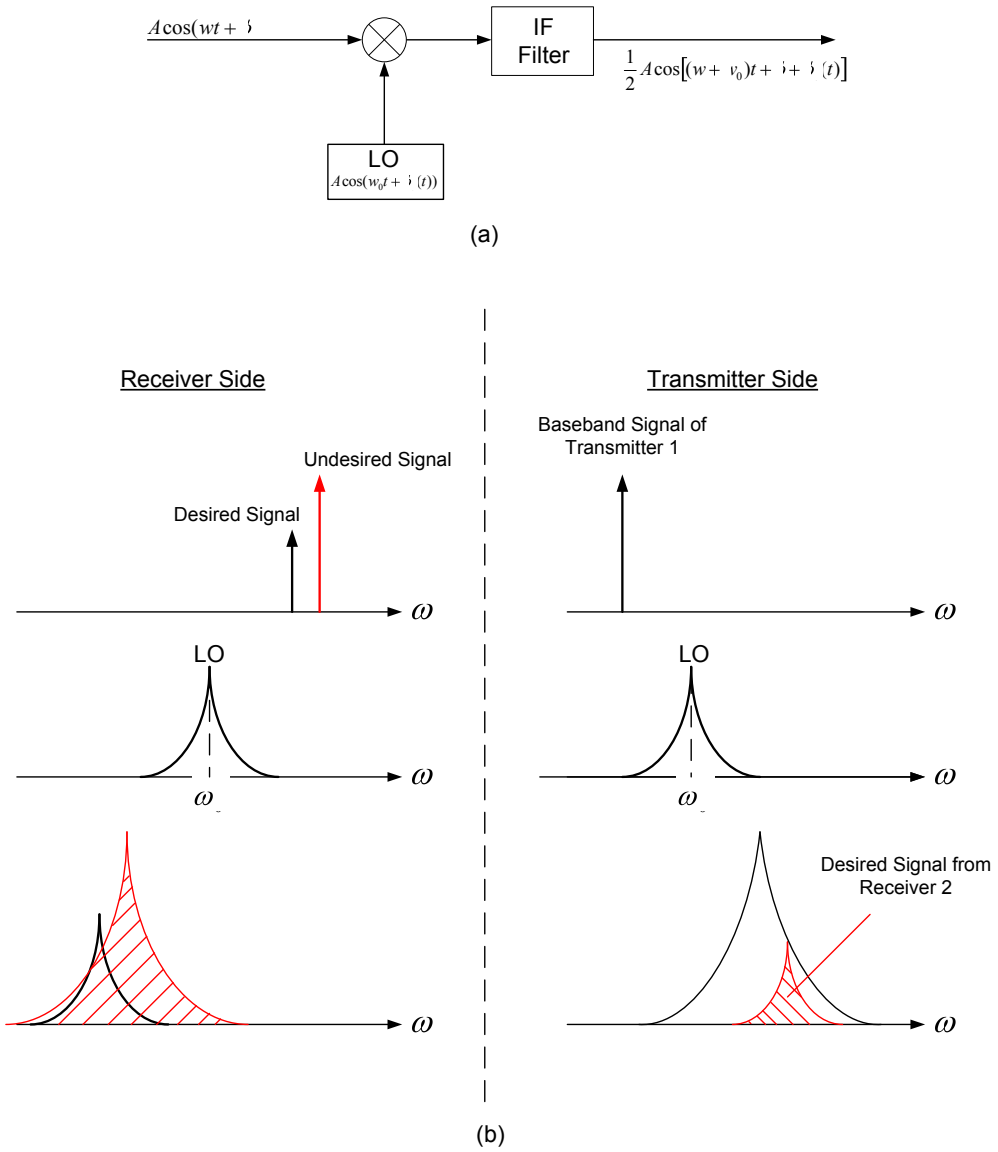


Figure 5.6 : (a) Use of local oscillator in a communication system with phase noise reflection to the output (b) destructive effects of phase noise in a transceiver

5.3 Common Phase Noise Models

5.3.1 Leeson's Phase Noise Model

A commonly used phase noise model is the empirical model proposed by D. B. Leeson in 1966 [40]. Although the model includes empirical parameters, it still has a mathematical background. In this model, oscillator is considered as a feedback system shown in Fig. 5.7 in which active part is modeled as noise free amplifier [41]. In the figure, $S_{\emptyset}(\omega)$ and $S_{\theta}(\omega)$ represent input and output power spectral densities. H(w) is the transfer function of the resonator which is calculated in (5.9) where Q_L is the loaded Q factor which is calculated as $\omega_0/2\omega_h$ and $\Delta\omega$ is the carrier offset. Obviously this transfer function has band pass characteristics around center frequency ω_0. Closed loop response of the whole system is as given in (5.10). Note that G is taken as unity in the rest of the calculations.

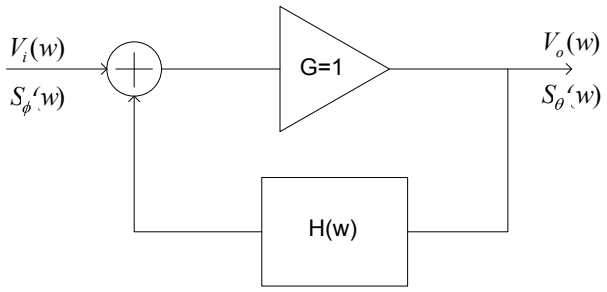


Figure 5.7 : Oscillator model block diagram

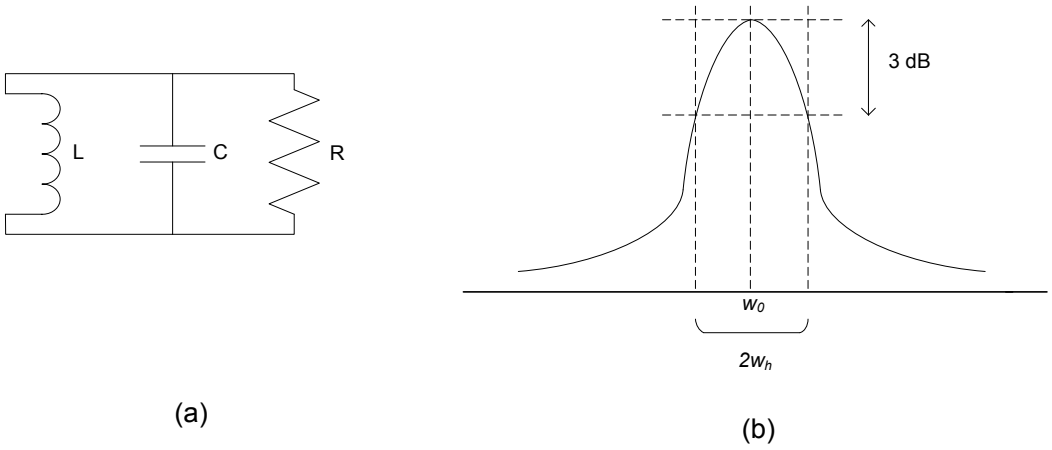


Figure 5.8 : (a) Sample resonator structure (b) frequency response

$$H(\omega) = \frac{V_{out}(\omega)}{V_{in}(\omega)} = \frac{1}{1 + j2\frac{\Delta\omega}{\omega_0}Q_L} \tag{5.9}$$

$$V_o(\omega) = \frac{G}{1 - GH(\omega)}V_i(\omega) \tag{5.10}$$

$S_\theta(\omega)$ is calculated by multiplying $S_\emptyset(\omega)$ with square of closed loop gain in frequency domain as :

$$S_\theta(\omega) = \left|\frac{1}{1 - H(\omega)}\right|^2 S_\emptyset(\omega) = \left(1 + \frac{\omega_0^2}{4\Delta\omega^2 {Q_L}^2}\right)S_\emptyset(\omega) \tag{5.11}$$

Input noise spectral density $S_\emptyset(w)$ is modeled by using phase deviation expression resulting from thermal noise incident on active devices. Since amplifier is modeled as noise free, its noise factor F and flicker noise effect are also included in the input noise expression. This expression is as written in (5.12) and illustrated in Fig. 5.9(a). In the equation, k stands for Boltzmann constant, F denotes the noise factor, ω_c corresponds to the flicker noise corner of the active device and P_{avg} is the average power in the resonator bandwidth. Substituting (5.12) into (5.11) and making some simplifications $S_\theta(w)$ is obtained as in (5.13). Obtained characteristic is plotted in Fig. 5.9 (b). Note that noise floor is calculated as kTF/P_{avg}.

$$S_\emptyset(\omega) = \frac{kTF}{P_{avg}}\left(1 + \frac{\omega_c}{\Delta\omega}\right) \tag{5.12}$$

$$S_\theta(\omega) = \frac{kTF}{2P_{avg}}\left[1 + \frac{\omega_c}{\Delta\omega} + \frac{{\omega_0}^2}{4\Delta\omega^2 {Q_L}^2} + \frac{{\omega_0}^2\omega_c}{4\Delta\omega^3 {Q_L}^2}\right] \tag{5.13}$$

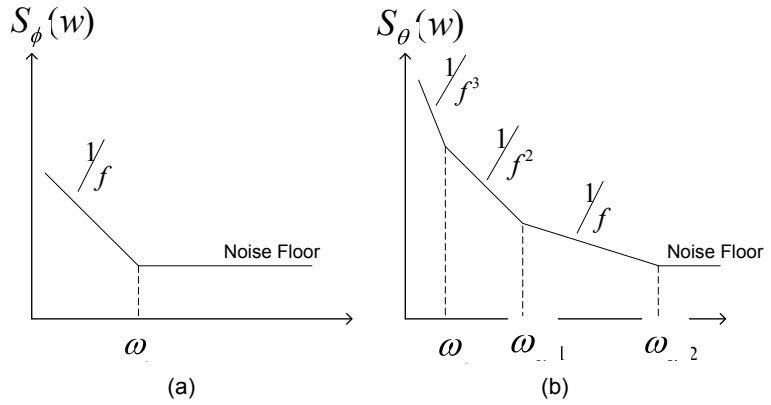


Figure 5.9 : (a)Spectrum of $S_\emptyset$ (b) Spectrum of S_θ

Leeson's model is generally written with logarithmic expression in a more compact form as given in 5.14. Looking at this final expression, a general idea about the ways of reducing the phase noise can be adopted. These ways can be listed as maximizing Q factor and power; reducing flicker noise and lowering the noise figure by using low noise active devices and limiting compression.

$$S_\theta(\omega) = 10log\left\{\frac{kTF}{2P_{avg}}\left[1+\frac{\omega_c}{\Delta\omega}+\left(\frac{\omega_0}{2\Delta\omega Q_L}\right)^2\left(1+\frac{\omega_c}{\Delta\omega}\right)\right]\right\} \quad (5.14)$$

Although Leeson's model gives a general insight about reducing phase noise, it cannot explain the phase noise generation mechanisms [48]. So, by using this model only, it is difficult to derive circuitwise phase noise reduction techniques which can only be done by using a more accurate phase noise model also explaining the physics of the phenomenon.

Besides Leeson's model, in the literature, there are various models looking at the same problem from different views, making distinct assumptions and taking different factors into account. First of them is the linear time invariant model [42]. In this model, oscillator is approximated as a linear system which enables handling noise contributions of each part separately and adding them together at the end to get overall noise. Resembling the Leeson's one, this model also includes fitting parameters and cannot explain nonlinear effects however it has some useful suggestions like decreasing effective resistance and increasing oscillation amplitude.

5.3.2 Linear Time Variant Model

In the previous model, oscillator was assumed to have time invariant nature but in reality it has time variant characteristic that should be taken into account especially for low phase noise designs. Hajimiri and Lee introduced a general phase noise model [43] by taking into account periodically time-varying nature of oscillators. Some small errors in this model is corrected in [44]. Although different results are obtained in frequency domain analysis done by Jannesari and Kamarei, later they are found to be incorrect and it is realized that original analysis is correct [45]. The analysis is important since it proposes some useful phase noise suppression techniques.

An oscillatory system can be characterized with noise currents as inputs and amplitude $A(t)$ and phase $\phi(t)$ responses as outputs. As shown in Fig. 5.10 output responses strongly depend on the time varying function of noise current. If the noise impulse is incident at the peak of the oscillation it only changes the amplitude while the phase is not distorted. On the other hand if it is incident at zero crossing it only changes the phase while the amplitude stays constant. In both cases instantaneous voltage change can be written as $\Delta V = \Delta q / C_{n,t}$ where Δq is injected charge and $C_{n,t}$ is the total capacitance of the node. As another case noise is injected between these time instants which cause both amplitude and phase distortion.

Assuming a very small noise charge injection into each node, whole system may be treated as linear. Linearity assumption is valid when the injected charge Δq does not exceed 10% of maximum charge swing q_{max} across the node capacitance. This linearity combined with the time varying nature characterizes the system with amplitude and phase impulse responses shown in Figure 5.11. In any oscillator there is an amplitude limiting mechanism which stabilizes oscillation. Caused by nonlinear nature of the active devices, this mechanism eliminates the amplitude distortion and we left with the phase distortion only. From the given impulse response this distortion can be expressed as step function given in (5.15).

$$h_{\phi}(t,\tau) = \frac{\Gamma(\omega_0 \tau)}{q_{max}} u(t-\tau) \tag{5.15}$$

$\Gamma(x)$ in (5.15) is the "impulse sensitivity function (ISF)" which gives a measure of the phase shift due to the applied impulse at time τ. ISF which is a dimensionless quantity actually describes the behavior illustrated in Figure 5.10. Therefore it is periodic with 2π and its value is maximum at zero crossings and minimum at oscillation peaks.

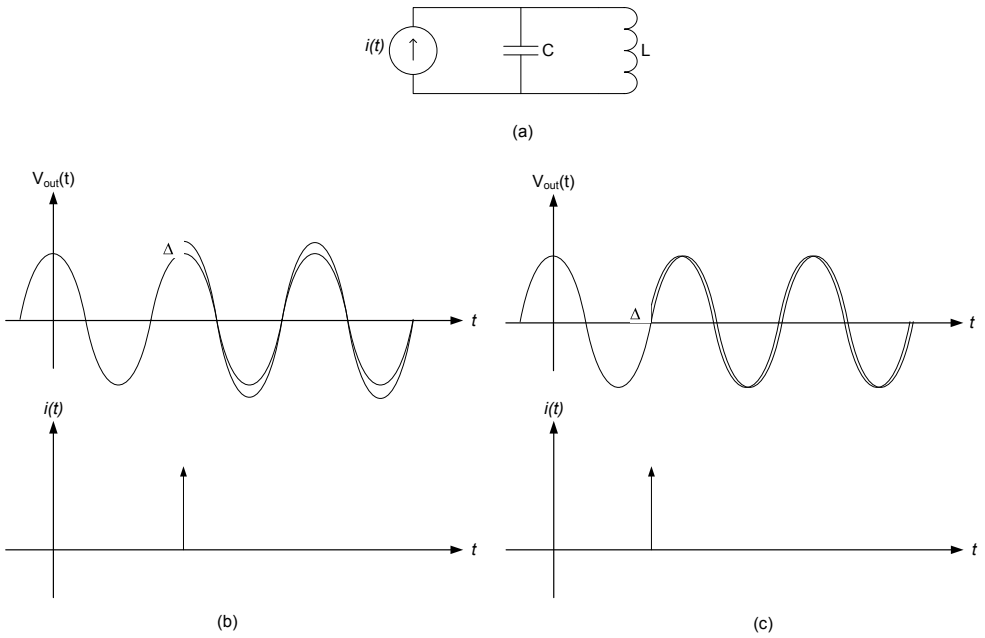


Figure 5.10 : (a) Noise injected at a circuit node (b) noise injected at the peak (c) noise injected at zero crossing

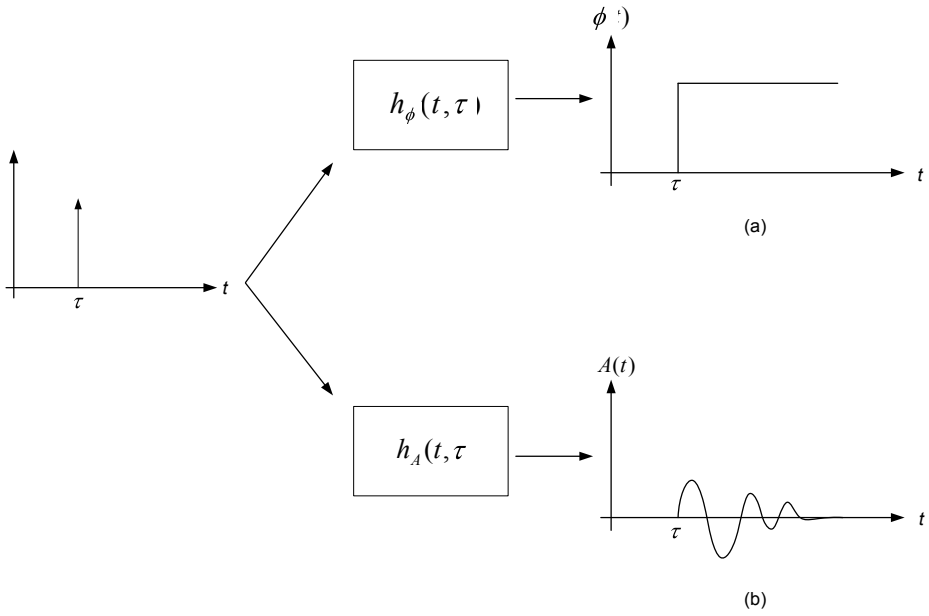


Figure 5.11 : (a) Phase response (b) amplitude response models

Knowing the impulse response, phase fluctuation can be calculated as :

$$\phi(t) = \int_{-\infty}^{\infty} h_\phi(t,\tau) i(\tau) d\tau = \frac{1}{q_{max}} \int_{-\infty}^{\infty} \Gamma(\omega_0 \tau) i(\tau) d\tau \qquad (5.16)$$

where $i(t)$ is noise current. Periodicity of the ISF enables us to expand it into Fourier series and using this form excess phase can be written as:

$$\phi(t) = \frac{1}{q_{max}}\left[\frac{c_0}{2}\int_{-\infty}^{t} i(\tau)d\tau + \sum_{1}^{\infty} c_n \int_{-\infty}^{t} i(\tau)\cos(n\omega_0\tau)\,d\tau\right] \tag{5.17}$$

To calculate excess phase exactly, first Fourier series coefficients (c_n's) of the ISF should be found which is generally not easy but nonetheless the expression in (5.17) gives good insight about the phenomenon. Considering the low pass characteristics of the integration, each noise current tone close ($\Delta\omega$) to the integer multiples of the oscillation frequency is multiplied with the corresponding Fourier series coefficient of ISF and reflected to excess phase formulated as:

$$\phi(t) \approx \frac{I_n c_n \sin(\Delta\omega t)}{2q_{max}\Delta\omega} \tag{5.18}$$

Substituting this $\phi(t)$ into generic oscillator output expression which is $V_{out}(t) = A(t).f[\omega_0 t + \phi(t)]$, single tone phase modulations for output voltage is obtained. As a general expression, noise currents at $n\omega_0 + \Delta\omega$ injected to a node of an oscillator results in equal sidebands at $\omega_0 \pm \Delta\omega$ with power given in (5.19) relative to the carrier.

$$P_{SBC}(\Delta\omega) = 10\,log\left(\frac{I_n c_n}{4q_{max}\Delta\omega}\right)^2 \tag{5.19}$$

Up to now, analysis was done considering single noise tones. To predict actual phase noise characteristics, practical case should be considered. In a practical case an arbitrary noise current has $1/f$ region at low frequencies and a flat region as shown in Figure 5.12 (a). Considering the previous discussions, conversion of this noise to the phase noise is illustrated in Figure 5.12 (b) and (c).

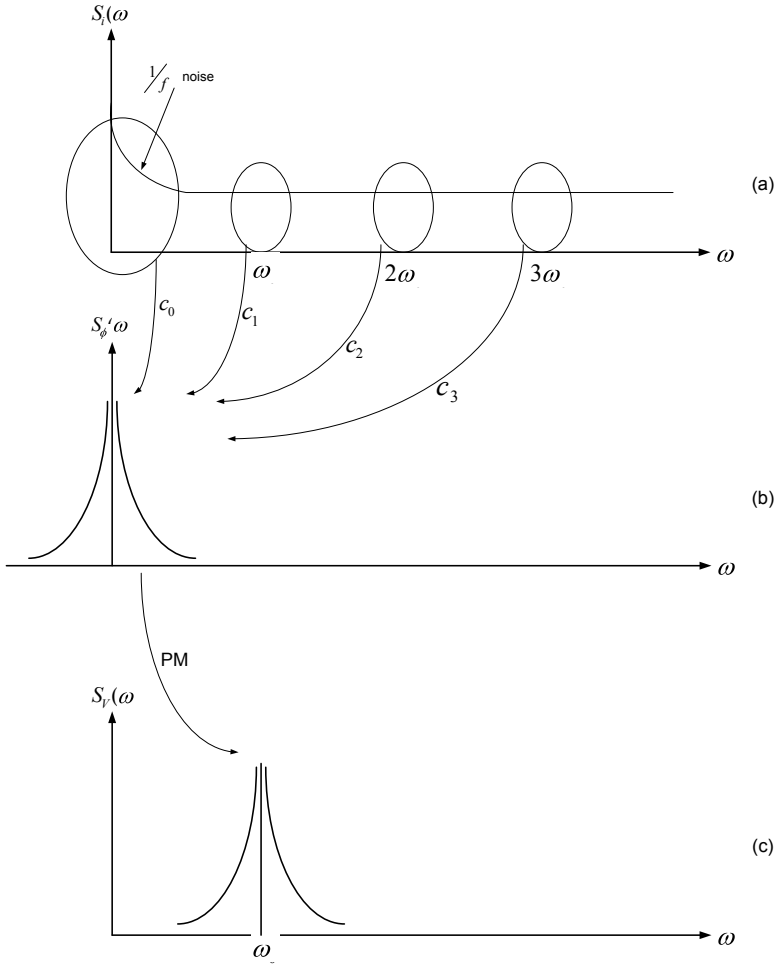


Figure 5.12 : (a) Spectral density of the noise current and (b),(c) its conversion to phase noise

The low frequency noise sources are weighted by c_0 and constitute $1/f^3$ region while the flat regions are weighted by c_n's and form the $1/f^2$ region of phase noise spectrum. To formulate this characteristic, calculation of single tone case will be used.

Considering a noise current with noise spectral density $\overline{i_n^2}/\Delta f$ is injected into oscillator. (5.20) is the resulted single sideband noise spectral density which is calculated using (5.19) where I_n is the peak amplitude which means $I_n^2/2 = \overline{i_n^2}/\Delta f$ [44].

$$\mathcal{L}\{\Delta\omega\} = 10\log\left(\frac{\frac{\overline{i_n^2}}{\Delta f}\sum_{n=0}^{\infty} c_n^2}{4q_{max}^2\Delta\omega^2}\right) \tag{5.20}$$

Using Parseval's relation given in (5.21), this expression can be written in the form (5.22) which represents $1/f^2$ region of phase noise spectrum.

$$\sum_{n=0}^{\infty} c_n^2 = \frac{1}{\pi}\int_0^{2\pi} |\Gamma(x)|^2 dx = 2\Gamma_{rms}^2 \tag{5.21}$$

$$\mathcal{L}\{\Delta\omega\} = 10\log\left(\frac{\Gamma_{rms}^2}{q_{max}^2}\frac{\overline{i_n^2}/\Delta f}{2\,\Delta\omega^2}\right) \tag{5.22}$$

$1/f^3$ corner of the output phase noise spectrum is not the same as $1/f$ corner of the device noise. To find the relation, phase noise expression in $1/f^3$ region should also be found. The device noise in the flicker noise portion ($\Delta\omega < \omega_{1/f}$) can be expressed as:

$$\overline{i_{n,1/f}^2} = \overline{i_n^2}\,\frac{\omega_{1/f}}{\Delta\omega} \tag{5.23}$$

Substituting this expression in (5.19), phase noise expression for $1/f^3$ region is found as (5.24).

$$\mathcal{L}\{\Delta\omega\} = 10\log\left(\frac{c_0^2}{q_{max}^2}\frac{\overline{i_n^2}/\Delta f}{8\,\Delta\omega^2}\frac{\omega_{1/f}}{\Delta\omega}\right) \tag{5.24}$$

Writing the equality between $1/f^2$ and $1/f^3$ regions ω_{1/f^3} is found in terms of $\omega_{1/f}$ as:

$$\omega_{1/f^3} = \omega_{1/f}\frac{c_0^2}{4\Gamma_{rms}^2} \approx \omega_{1/f}.\frac{1}{2}\left(\frac{c_0}{c_1}\right)^2 \tag{5.25}$$

Note that c_0 strongly depends on the symmetry properties of the waveform and can be significantly reduced by achieving good symmetry.

5.3.2.1 Cyclostationary Noise Sources

If statistical properties of a process change periodically with time it is called cyclostationary process. One example for our case is the channel noise of MOS device caused by gate-source overdrive voltage which changes periodically with time. A cyclostationary noise current can be decomposed as:

$$i_n(t) = i_{n0}(t).\alpha(\omega_0 t) \tag{5.26}$$

where $i_{n0}(t)$ is stationary and $\alpha(t)$ is a periodic function of noise amplitude modulation. Writing the phase fluctuation with this decomposed form (5.27) is obtained.

$$\phi(t) = \int_{-\infty}^{t} i_{n0}(\tau) \frac{\alpha(\omega_0\tau)\Gamma(\omega_0\tau)}{q_{max}} d\tau \tag{5.27}$$

As can be seen from the expression cyclostationary noises can be treated as stationary noise with an effective ISF given as:

$$\Gamma_{eff}(x) = \Gamma(x)\alpha(x) \tag{5.28}$$

Significance of effective ISF depends on circuit topology and voltage waveform. In LC oscillators it is especially critical because effective ISF function may be very different from the ISF which means time dependent characteristics change significantly. In such a case, cyclostationary properties of the noise gain importance.

Linear time variant model gives useful insights by explaining the physics of the phenomenon. Advantage of the model is that it can be applied to any oscillator. On the other hand there is a considerable difficulty in calculating the ISF function which is necessarily needed for the model. Despite this difficulty model gives very useful design implications for the reduction of phase noise which will be discussed in phase noise reduction techniques section in detail.

5.3.3 Nonlinear Time Invariant Model

Previously mentioned models were derived assuming linear operation of the transistors. In practice, this is not a valid assumption since transistors face both linear and nonlinear operation regions in an oscillation period. Considering this fact, a new phase noise model is derived by Samori based on differential pair LC oscillators [46]. The model accounts for the nonlinearity of the transconductor characteristic and shows that this characteristic causes folding of the wideband noise basically originating from the thermal and shot noise sources. Findings of this model provide very useful insights, enabling beneficial circuit optimizations and phase noise reduction techniques.

In the linear analysis of the oscillator noise, analyzed as the preliminary work, phase noise expression is derived using sideband to carrier ratio as given in (5.29). In this expression, A_0 is the oscillation amplitude, Q is the quality factor of the tank and F is the noise factor which is estimated considering the circuit operating in the linear region.

$$SSCR(\Delta\omega) = \frac{2}{A_0^2}\frac{kT}{C}\frac{\omega_0}{Q}\frac{1}{(\Delta\omega)^2}(1+F) \tag{5.29}$$

Q factor of the tank can be given by the well known expression $Q = C\omega_0/g_{ot}$ where g_{ot} is the loss conductance calculated as given in (5.30) in which g_{pC} and g_{pL} denote parallel parasitic conductances ; g_{sC} and g_{sL} denote series parasitic conductances of capacitor and inductor.

$$g_{ot} \cong g_{pC} + g_{pL} + \frac{(\omega_0 C)^2}{g_{sC}} + \frac{1}{(\omega_0 L)^2 g_{sL}} \tag{5.30}$$

According to this linear approach, to decrease phase noise, capacitance C, quality factor of the tank Q and oscillation amplitude A_0 should be maximized. On the other hand, maximizing A_0 leads to drive the transconductor in highly nonlinear regime and this nonlinearity creates discrepancy with linear analysis. Therefore, a model accounting for the nonlinearity is needed.

5.3.3.1 Harmonic Transfer in Nonlinear Systems

Oscillator's transconductance, denoted by *I= I(V)*, can be written as given in 5.31 assuming a relatively very weak harmonic tone $V_l(t)$ at $\omega_0 - \Delta\omega$ superimposed on the carrier $V_0(t)$ with amplitude A_0.

$$I\big(V_0(t) + V_l(t)\big) \cong I\big(V_0(t)\big) + \left.\frac{dI}{dV}\right|_{V_0(t)} V_l(t) \tag{5.31}$$

In the expression, first term is the fundamental component and the second term gives the intermodulation tones. The derivative dI/dV is the transconductance $g(V_0(t))$ of the differential pair and considering voltage and current waveform characteristics of LC

oscillators it is an even function of time with the fundamental component at $2\omega_0$ [48]. Therefore, it can be written as Fourier expansion given by :

$$g\big(V_0(t)\big) = \sum_{n=-\infty}^{+\infty} g^{(2n)} e^{j2n\omega_0 t} \tag{5.32}$$

where the coefficients $g^{(2n)}$ are real and assuming fundamental signal $V_0(t) = A_0 \cos(\omega_0 t)$, they also alternate in sign.

In order to express fundamental current component with transconductance terms, dI/dt is mathematically differentiated as (5.33). This differentiation allows writing $I\big(V_0(t)\big)$ as an integral of the transconductance as given in (5.34).

$$\frac{dI}{dt} = \frac{dI}{dV}\frac{dV}{dt} = g(V)\frac{dV}{dt} \tag{5.33}$$

$$I\big(V_0(t)\big) = I_0(t) = \int g(V_0(t))\frac{dV_0(t)}{dt}dt \tag{5.34}$$

Replacing (5.32) into (5.34), fundamental current component at ω_0 is founded and expressed in phasor as (5.35). Note that effective transconductance g_{meff} is equal to $\overline{I_0}/\overline{V_0}$.

$$\overline{I_0} = \big(g^{(0)} - g^{(2)}\big)\overline{V_0} = g_{meff}\overline{V_0} \tag{5.35}$$

After finding the fundamental component, next job is to analyze intermodulation components. Intermodulation tones at $n\omega_0 \pm \Delta\omega$, given by the second term of (5.31), can be calculated from [47]:

$$\left(\frac{\overline{V_l}}{2}e^{j(\omega_0-\Delta\omega)t} + \frac{\overline{V_l}^*}{2}e^{-j(\omega_0-\Delta\omega)t}\right) x \sum_{n=-\infty}^{+\infty} g^{(2n)} e^{jn\omega_0 t} \tag{5.36}$$

Expanding the series in this equation, input harmonic tone $\overline{V_l}$ at $\omega_0 - \Delta\omega$ generates two intermodulation terms $\bar{I}_l$ at $\omega_0 - \Delta\omega$ given by $g^{(0)}\overline{V_l}$ and $\bar{I}_u$ at $\omega_0 + \Delta\omega$ given by $g^{(2)}\overline{V_l}^*$. Similar terms are generated by an input harmonic tone $\overline{V_u}$ at $\omega_0 + \Delta\omega$. The situation is illustrated in Fig. 5.13 and written in a compact form as:

$$2\begin{bmatrix}\bar{I}_l^{\,*}/2\\ \bar{I}_u/2\end{bmatrix}=\begin{bmatrix}g^{(0)} & g^{(2)}\\ g^{(2)} & g^{(0)}\end{bmatrix}\begin{bmatrix}\bar{V}_l^{\,*}/2\\ \bar{V}_u/2\end{bmatrix} \tag{5.37}$$

In the introduction of this chapter it was shown that when a small signal tone is superimposed on the carrier, it causes both amplitude and phase modulations. Considering this fact, writing AM and PM expressions due to $\overline{V}_l$ and $\overline{V}_u$ will help clarifying the problem. In the presence of a single tone $\overline{V}_l$, resulting signal can be written as:

$$V(t) = A_0\cos(\omega_0 t) + |\bar{V}_l| cos[(\omega_0 - \Delta\omega)t + \emptyset_l] \tag{5.38}$$

Decomposing $\overline{V}_l$ into AM and PM terms (5.38) can also be written using modulation indexes as:

$$V(t) = A_0[1 + m_v(t)]cos(\omega_0 t + \beta_v(t)) \tag{5.39}$$

where $A_0 m_v(t) = Re\{\bar{V}_l^* e^{j\Delta\omega t}\}$ and $A_0\beta_v(t) = Im\{-\bar{V}_l^* e^{j\Delta\omega t}\}$. Accounting for the similar calculations for $\overline{V}_u$ and using phasor representations of $m_v(t) = Re\{\bar{m}_v e^{j\Delta\omega t}\}$ and $\beta_v(t) = Im\{\bar{\beta}_v e^{j\Delta\omega t}\}$, modulation indexes can be expressed as:

$$\begin{bmatrix}\bar{m}_v\\ \bar{\beta}_v\end{bmatrix}=\frac{1}{A_0}\begin{bmatrix}1 & 1\\ -1 & 1\end{bmatrix}\begin{bmatrix}\bar{V}_l^{\,*}\\ \bar{V}_u\end{bmatrix} \tag{5.40}$$

Taking the inverse, intermodulation voltages are found as:

$$\begin{bmatrix}\bar{V}_l^{\,*}\\ \bar{V}_u\end{bmatrix}=\frac{A_0}{2}\begin{bmatrix}1 & -1\\ 1 & 1\end{bmatrix}\begin{bmatrix}\bar{m}_v\\ \bar{\beta}_v\end{bmatrix} \tag{5.41}$$

Similarly, intermodulation currents can be expressed in terms of current modulation indexes as:

$$\begin{bmatrix}\bar{I}_l^{\,*}\\ \bar{I}_u\end{bmatrix}=\frac{|\bar{I}_0|}{2}\begin{bmatrix}1 & -1\\ 1 & 1\end{bmatrix}\begin{bmatrix}\bar{m}_I\\ \bar{\beta}_I\end{bmatrix} \tag{5.42}$$

Also using (5.37), modulation terms are expressed in terms of transconductance terms as:

$$|\bar{I}_0|\begin{bmatrix}\bar{m}_I\\ \bar{\beta}_I\end{bmatrix}=\begin{bmatrix}g^{(0)}+g^{(2)} & 0\\ 0 & g^{(0)}-g^{(2)}\end{bmatrix}\begin{bmatrix}\bar{m}_v\\ \bar{\beta}_v\end{bmatrix}|\bar{V}_0| \tag{5.43}$$

Transconductances $g^{(0)} + g^{(2)}$ and $g^{(0)} - g^{(2)}$ can be written as AM (g_{am}) and PM (g_{pm}) terms respectively. Typical characteristics are plotted as functions of oscillation amplitude for an NMOS pair in Fig. 5.14 [48].

Looking at this figure it can be seen that when the oscillation amplitude increases, g_{am} decreases more rapidly than g_{pm} and becomes zero after a certain value. After this value, oscillator is in highly nonlinear region and oscillation starts resembling square wave. Therefore, if the oscillation amplitude is high enough, change of the amplitude of a superimposed signal has no effect on the clamped output. On the other hand, transitions of output waveform occur when the input signal crosses zero level. So, g_{pm} is directly effective on the output causing time shifts. That's why $g_{pm} = g_{meff}$.

According to the discussions above if the hard limiter approximation is valid, half of the noise power, which is PM noise power, is effective on the output. This result should be included in SSCR expression by dividing (5.29) by 2 giving the result in (5.44). Furthermore, intermodulations between the carrier and wideband noise sources cause an increase in noise factor F which should also be reflected to (5.44).

$$SSCR(\Delta\omega) = \frac{1}{A_0^2}\frac{kT}{C}\frac{\omega_0}{Q}\frac{1}{(\Delta\omega)^2}\left(1 + F_{eff}\right) \tag{5.44}$$

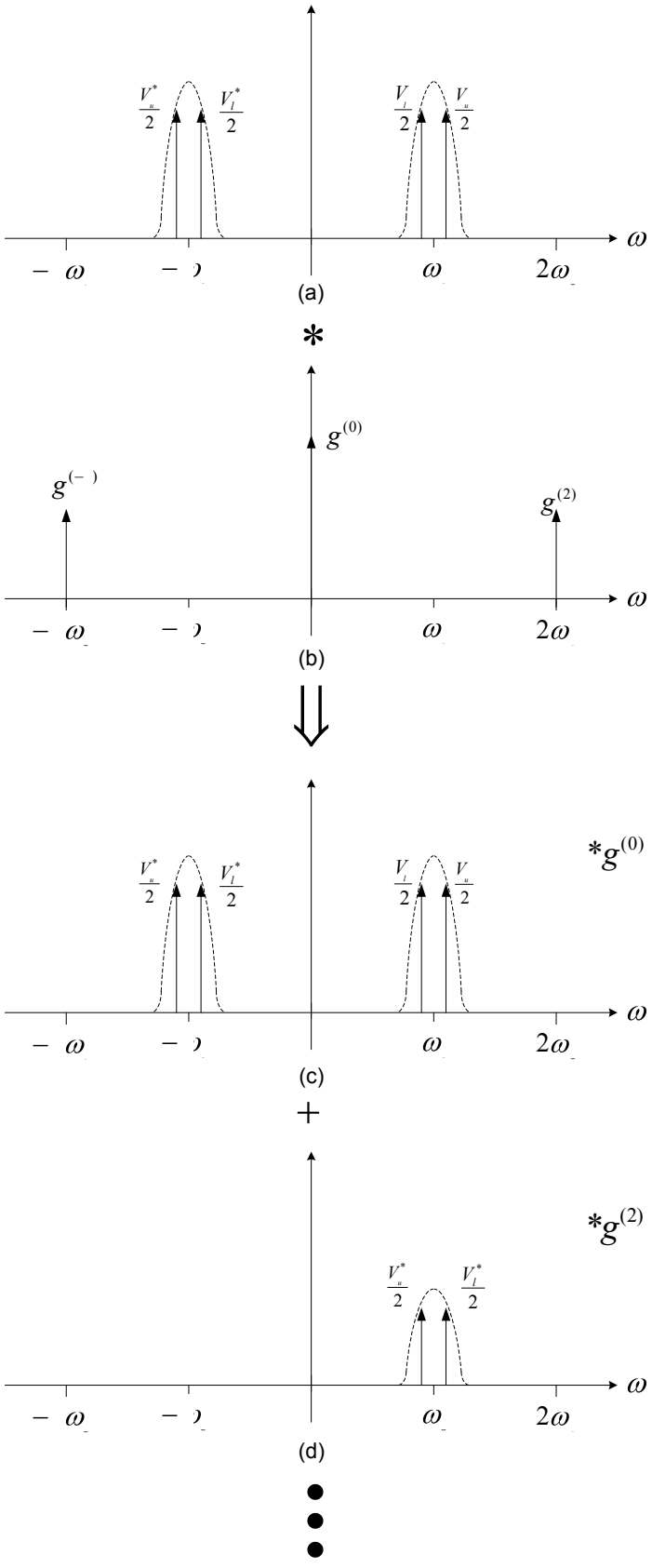


Figure 5.13 : Illustration of harmonic transfer: (a) noise spectrum (b) transconductance terms (c) convolution with $g^{(0)}$ (d) convolution with $g^{(2)}$

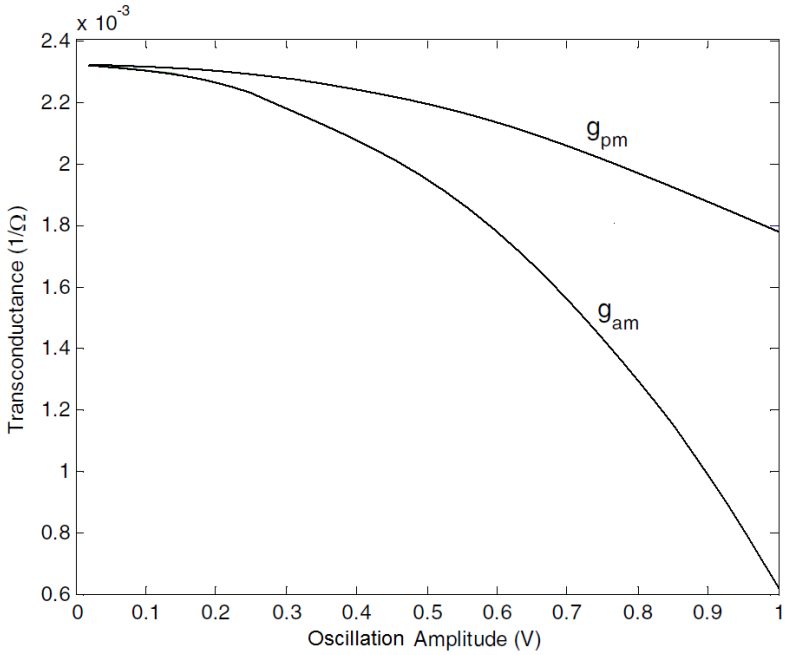


Figure 5.14 : $\mathbf{g_{am}}$ and $\mathbf{g_{pm}}$ of a typical NMOS pair

5.3.3.2 Phase Noise Due to Active Part

Wideband white noise sources of the transistors forming the active circuit contribute to phase noise according to the mentioned harmonic transfer theory. These noise sources are mainly shot noise of collector current, thermal noise of base spreading resistor for BJTs ; shot noise of drain current and channel thermal noise for MOSFETs. These sources can be modeled as an equivalent noise voltage at the input of the active part that can be written as $2kTR_{eff}$ where R_{eff} is the effective noise resistance. This noise voltage can also be transformed to the noise current which is parallel to the device.

If the oscillation amplitude is high enough to operate the device as a hard limiter, the transconductor $g(V_0(t))$ is a train of δ functions at a frequency $2\omega_0$. In this case spectrum of the transconductor includes infinite number of terms given by $(-1)^n\delta(\omega - 2n\omega_0)\, g_{ot}/2$. Since multiplication in the time domain is convolution in frequency domain, these terms are convolved with wideband noise to be reflected to the output spectrum as illustrated for a bandwidth of $N\omega_0$ in Fig. 5.15 where vertical dashed line identifies the bandwidth of the loop filter.

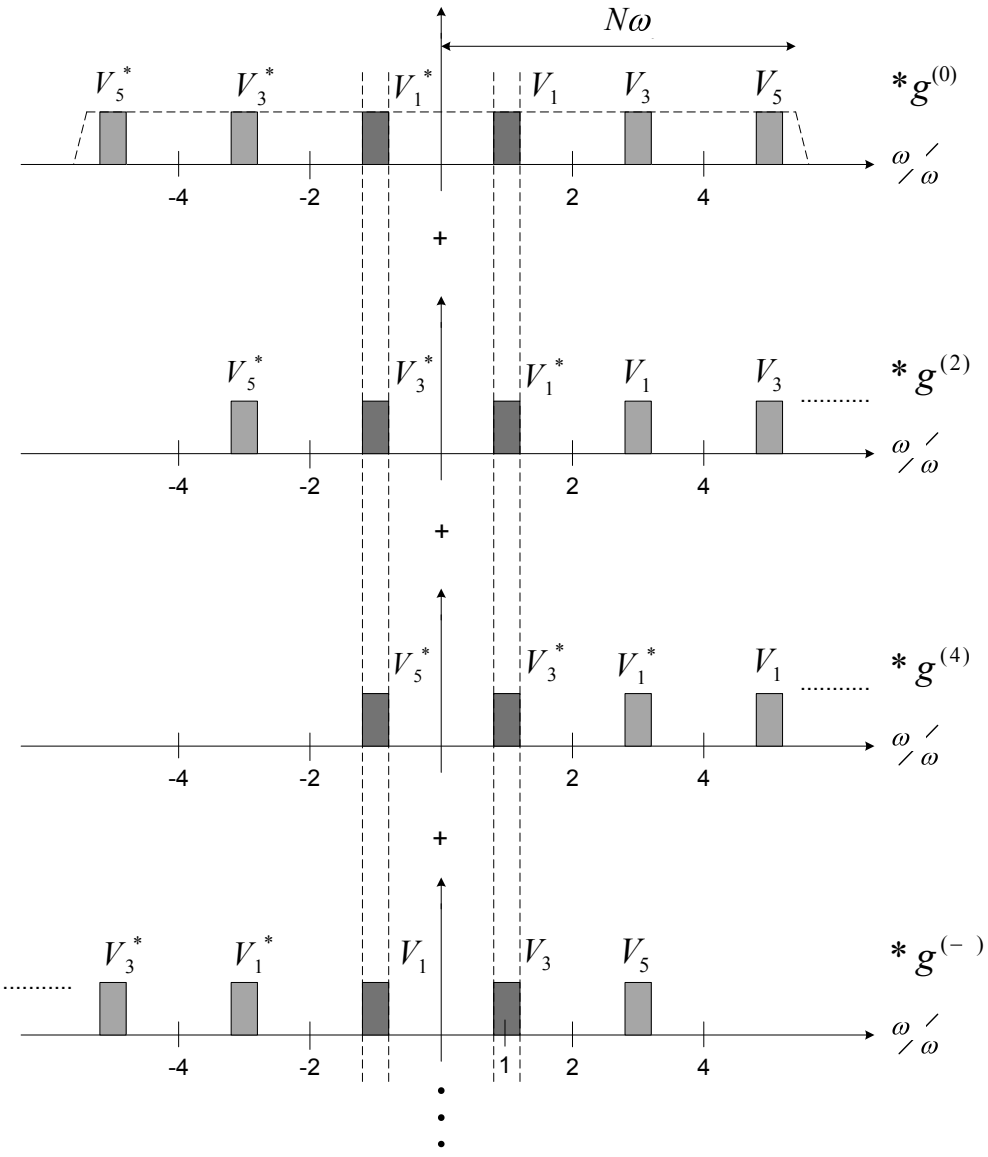


Figure 5.15 : Folding of the wideband noise spectrum.

As can be seen from Fig. 5.15, noise components close to the frequencies $\pm(2n+1)\omega_0$, emphasized as hatched areas, fall into the filter bandwidth and contribute to the phase noise by being weighted by $g^{(2n)}$ terms. Situation can be summarized by the equation:

$$\begin{bmatrix} \bar{I}_l^{\,*}/2 \\ \bar{I}_u/2 \end{bmatrix} = \begin{bmatrix} g^{(-2n)} & g^{(2n+2)} \\ g^{(2n+2)} & g^{(-2n)} \end{bmatrix} \begin{bmatrix} \bar{V}_{(2n+1)l}^{\,*}/2 \\ \bar{V}_{(2n+1)u}/2 \end{bmatrix} \tag{5.45}$$

Using this hard limiter assumption resulting contributions from V_l components to the phase noise at $\omega_0 - \Delta\omega$ can be found as:

$$\left(\frac{g_{ot}}{2}\right)^2 \left|\frac{\bar{V}_{l(2n+1)}}{2}\right|^2 = \left(\frac{g_{ot}}{2}\right)^2 2kTR_{eff} \tag{5.46}$$

Also taking into account V_u terms, overall noise power spectrum is obtained as $2 * 2kTR_{eff}\frac{g_{ot}^2}{2}\frac{N}{2}$, assuming $N\omega_0$ bandwidth causing $N/2$ folded replicas. Note that first factor 2 is due to the double transistor structure. Dividing this expression by the reference phase noise caused by the loss conductance g_{ot} , F factor is found as :

$$F = 2R_{eff}\, g_{ot}\, \frac{N}{2} \tag{5.47}$$

5.3.3.3 Noise Due to Biasing Circuit

During the discussions in the previous parts, noise of the biasing circuit was not taken into account since it is a common mode noise. However, when oscillation amplitude is high enough to drive transconductor in nonlinear regime, during most of the period transistors are completely switched which means generated current flows through only one of the transistors. In this case relative importance of the noise sources changes. Noise of the biasing circuit which is neglected in the small signal regime becomes important while contribution of other noise sources decrease.

In the mathematical analysis, transconductor is assumed to be working as a hard limiter. This transconductor characteristics, modeled by a square wave $T(t)$ with frequency ω_0, is multiplied with the noise currents generated by the biasing circuit and transferred to the tank circuit to see the effects. Using (5.36) the expression in (5.48) is obtained as the result of the multiplication with a generic noise tone $\bar{I}_n$. Note that in the equation $T^{(2n+1)}$ are the Fourier coefficients obtained as $e^{jn\pi}/\pi(2n+1)$.

$$\left(\frac{\bar{I}_n}{2}e^{j\omega t} + \frac{\bar{I}_n^*}{2}e^{-j\omega t}\right)\sum_{n=-\infty}^{n=\infty} T^{(2n+1)}e^{j(2n+1)\omega_0 t} \tag{5.48}$$

Similar to the calculated spectrum for active circuit case, this multiplication means convolution in frequency domain. Convolving the terms, it turns out that noise around even

harmonics, i.e. $2n\omega_0 \pm \Delta\omega$ contribute to the noise around ω_0. This characteristic is obviously seen in (5.49) where the noise current tones $\bar{I}_l$ and $\bar{I}_u$ at $\omega_0 \pm \Delta\omega$ are calculated.

$$\begin{bmatrix} \bar{I}_l^*/2 \\ \bar{I}_u/2 \end{bmatrix} = \begin{bmatrix} T^{(-1)} & T^{(1)} & T^{(-3)} & \dots \\ T^{(1)} & T^{(3)} & T^{(-1)} & \dots \end{bmatrix} \begin{bmatrix} \bar{I}_n(\Delta\omega)/2 \\ \bar{I}_n^*(2\omega_0 - \Delta\omega)/2 \\ \bar{I}_n(2\omega_0 + \Delta\omega)/2 \\ \bar{I}_n^*(4\omega_0 - \Delta\omega)/2 \\ \dots \end{bmatrix} \tag{5.49}$$

To see the effects of these noise tones at $2n\omega_0 \pm \Delta\omega$ AM and PM modulation indexes should be calculated. For this purpose calculations using (5.40) are carried out and modulation indexes are calculated as (5.50) and (5.51) for $2n\omega_0 - \Delta\omega$ terms. Similar results can be obtained for the tones at $2n\omega_0 + \Delta\omega$.

$$\bar{m}_{2n} = \frac{1}{|\bar{I}_0|} \frac{2e^{j(n-1)\pi}}{\pi(4n^2-1)} \bar{I}_n^*(2n\omega_0 - \Delta\omega) \tag{5.50}$$

$$\bar{\beta}_{2n} = \frac{1}{|\bar{I}_0|} \frac{4ne^{jn\pi}}{\pi(4n^2-1)} \bar{I}_n^*(2n\omega_0 - \Delta\omega) \tag{5.51}$$

Using these modulation indexes, AM noise component $\bar{I}_{l,am}$ and PM noise component $\bar{I}_{l,pm}$ of $\bar{I}_l$ are obtained as in (5.52) and (5.53) respectively.

$$\begin{aligned} \bar{I}_{l,am}(\omega_0 - \Delta\omega) &= \frac{|\bar{I}_0|}{2} \sum_{n=0}^{n=+\infty} \bar{m}_{2n} = \frac{1}{\pi} \bar{I}_n(\Delta\omega) \\ &+ \frac{1}{\pi} \sum_{n=1}^{n=+\infty} \frac{\bar{I}_n^*(2n\omega_0 - \Delta\omega) + \bar{I}_n(2n\omega_0 + \Delta\omega)}{(4n^2-1)} e^{j(n-1)\pi} \end{aligned} \tag{5.52}$$

$$\begin{aligned} \bar{I}_{l,pm}(\omega_0 - \Delta\omega) &= \frac{|\bar{I}_0|}{2} \sum_{n=0}^{n=+\infty} \bar{\beta}_n \\ &= \frac{1}{\pi} \sum_{n=1}^{n=+\infty} (2n) \frac{\bar{I}_n^*(2n\omega_0 - \Delta\omega) + \bar{I}_n(2n\omega_0 + \Delta\omega)}{(4n^2-1)} e^{jn\pi} \end{aligned} \tag{5.53}$$

Examining the calculated components, it is concluded that main contribution to the phase noise comes from the noise at $2n\omega_0 \pm \Delta\omega$. Besides, noise at $\Delta\omega$ contributes to the AM noise

together with the noise at $2n\omega_0 \pm \Delta\omega$ which have the risk of transfer to the phase noise by special AM-PM conversion mechanisms.

For the calculation of the noise factor F, total phase noise spectral density $S_{pm}(\omega_0 - \Delta\omega)$ is calculated assuming the noise of the biasing circuit is white as in (5.54). Note that S_{nt} is the double sided power spectral density.

$$S_{pm}(\omega_0 - \Delta\omega) = \frac{S_{nt}}{\pi^2} \sum_{n=1}^{n=+\infty} (2n)^2 \frac{2}{(4n^2-1)^2} = \frac{S_{nt}}{8} \tag{5.54}$$

Resulting contribution to F factor is again obtained by dividing this expression to the reference phase noise as given in (5.55).

$$F = \frac{S_{nt}}{8kTg_{ot}} \tag{5.55}$$

Combining the calculated noise factors for active and biasing circuits total F is calculated as:

$$F = 2R_{eff}g_{ot}\frac{N}{2} + \frac{S_{nt}}{8kTg_{ot}} \tag{5.56}$$

In the calculations of the noise terms and phase noise spectral density ideal hard limiter approximation is used giving the upper values for the multiplicative terms as $N/2$ and $1/8$. In practical cases ideal hard limiter operation is not valid but since the logic behind noise folding is the same and hard limiter operation is generally approximated, formulation of F is still valid for a rough estimation. To obtain more accurate results, what should be done is to replace these upper limit values by the suitable ones which match the case of the oscillator.

At all, the nonlinear time invariant phase noise model gives useful results for developing efficient phase noise reduction techniques by taking into account the nonlinearity of transconductance and identifying fractions of the noise spectrum of active and biasing circuit which contributes to the phase noise.

5.4 Phase Noise Reduction

For low phase noise oscillator designs first thing is the selection of the circuit topology. As mentioned several times in the previous sections LC tuned oscillators are superior to the other oscillator types in terms of phase noise performance. Therefore in this part reduction techniques will be explained over LC tuned oscillators.

In the models section, simple formulations of different phase noise models are done which give useful information about phase noise generation and evident ways of its reduction. Using those models, effective reduction techniques which are mostly based on noise filtering are developed. Also there are some operational tricks that help steaming up endurance against noise sources. In this section those techniques and operational tricks will be explained.
Techniques are divided into two groups namely technology and operation related techniques and circuit techniques. First group is related with the basic requirements of low noise oscillators and second group includes circuitwise phase noise reduction techniques.

Before going into details, firstly in the following section, phase noise generation mechanisms will be summarized.

5.4.1 Phase Noise Generation

In the discussions up until now, general considerations were on the white noise sources. Although the flicker noise is a low frequency noise source which mostly contributes to the AM, it is also effective on PM by special AM-PM conversion mechanisms which will be explained in following parts. Therefore flicker noise of active devices should be taken into account for phase noise issue. Considering this fact, phase noise sources can be classified as follows: thermal noise generated by the parasitic resistances in the circuit especially parasitic resistance of the inductor in the tank circuit; white noise of active circuit; flicker noise of the transistors in active circuit; white noise of biasing circuit and flicker noise of the transistors in biasing circuit.

In all of the phase noise models it is pointed out that parasitic resistances cause thermal noise which has white characteristics. In the Leeson's approach and nonlinear model, looking at the same problem from different points of view and with different assumptions, this noise

found out to be causing phase noise. Obviously to reduce its effect parasitic resistances should be minimized.

In nonlinear time invariant phase noise model, white noise generated by the active circuit was found out to be contributing to phase noise. According to this model, noise components close to the frequencies $\pm(2n+1)\omega_0$ fall into the bandwidth of the tank and cause boosting of phase noise by explained folding mechanism. This model also explained contribution of the white noise in biasing circuit to the phase noise by showing that noise at $2n\omega_0 \pm \Delta\omega$ directly generates phase noise. Note that according to the model, near DC noise generates AM noise which has the risk of conversion to the phase noise. In addition, in the LTV model it is shown that noise power around integer multiples of ω_0 scaled by Fourier series coefficients c_n's contribute to the close-in phase noise.

Together with the mentioned white noise sources, flicker noise of the active devices also contributes to the phase noise. Flicker noise of transistors in biasing circuit which is more powerful than near DC white noise, generates AM noise which is converted to phase noise by AM-PM conversion mechanism. On the other hand flicker noise of transistors in active circuit cause modulation of the tail voltage waveform at every half period injecting noise at frequency $2\omega_0$ to the biasing circuit [48]. It follows that this noise generates phase noise by the mechanism explained for biasing circuit in nonlinear time invariant model. Also flicker noise, being a strong near DC noise, effects the voltage waveform on the varactors therefore causing phase noise.

To eliminate or reduce the effects of the mechanisms expressed in this part, some phase noise reduction techniques are developed. In the following sections, these techniques will be explained.

5.4.2 Technology and Operation Related Techniques

For achieving lowest phase noise performance first thing is to match most basic conditions. These include technological restrictions, setting and being well aware of operational characteristic of the circuit. Therefore to reduce phase noise preferential things that can be applied are the basic ones given in the following subsections.

5.4.2.1 Selecting Fully Differential Topology

Differential oscillators consist of NMOS and/or PMOS pair of transistors. As mentioned previously, in this type of structures common mode noise is mostly eliminated due to differential configuration resulting in reduced phase noise.

In LTV phase noise model, symmetry properties of oscillator and waveform was founded to be important for reduction of phase noise. Remembering that c_0 which has multiplicative effect in $1/f^3$ region is twice the DC value of ISF namely

$$c_0 = \frac{1}{\pi}\int_0^{2\pi} \Gamma_{eff}(x)dx \tag{5.57}$$

it is obvious that DC value of ISF should be minimized in order to improve phase noise performance. This condition is satisfied when waveform is symmetric [43]. In this model, importance of duty cycle which is symmetry related parameter is also highlighted. It is told that non-50% duty cycles result in larger c_n for even n and increase in these terms also increases the phase noise contributions of noise around integer multiples of oscillation frequency.

In fully symmetric oscillators both NMOS and PMOS pairs are used. This configuration has better common mode rejection, improved waveform symmetry and less flicker noise up conversion which lead further reduction of phase noise [49],[50],[51]. Along with improved phase noise performance, in fully symmetric structures drawn current can be reduced keeping oscillation amplitude same as only NMOS or PMOS topologies.

Despite these benefits there is an obvious disadvantage of additional NMOS or PMOS pair. Extra transistors come along with flicker noise which may have destructive effect on phase noise. Considering this fact fully symmetric oscillator should be carefully designed and optimized. Especially layout should be perfectly symmetric for the effective enhancement of the performance.

5.4.2.2 Optimizing Size of Transistors

As stated in phase noise generation part, one of the sources of the phase noise is AM-PM conversion. Basically changes in the oscillation amplitude cause distortion in the frequency response due to nonlinear nature of the cross coupled transistors. Result is the modulation of the phase shift [52]. To reduce this effect, W/L ratio of the transistors may be lowered to

increase gate overdrive voltage for the same bias current. This increases linear range of cross coupled pair and reduces AM-PM conversion. On the other hand, since flicker noise is related to the device size as given in (5.58), decreasing W and L increases the flicker noise contribution of the transistors [52]. Therefore an optimization in size of transistors may help lowering phase noise.

$$\overline{i_{1/f}^2} = \frac{k_f}{fC_{ox}WL}\Delta f \tag{5.58}$$

5.4.2.3 Improving Q-Factor

It is well known from phase noise models that improving Q factor of the resonator makes frequency response narrower which directly improves phase noise performance. Since Q factor is a technology related parameter, designer has limited effect on it. Therefore it generally determines the minimum phase noise that can be achieved.

In a standard CMOS process, Q factor of capacitors are generally much higher than that of on chip inductors. So, inductors are the key components that determine the quality. Although in some applications off-chip inductors are used to improve performance, in general on chip spiral inductors are used taking into account the integrability issues.

In order to increase Q factor of CMOS on-chip inductors, designers and manufacturers make use of some certain tricks. Most basic one is to increase coil width to decrease metal loss but this is effective for low frequencies. When frequency increases, due to skin effect current is forced to flow through certain region so that wideness of the coil is no more effective. Moreover coil parasitic capacitance also increases with increasing coil width. Therefore width of the coil should be carefully optimized. Another effective way is making inductor hollow. Due to eddy current generation, resistance of the innermost turns increase while they have little effect on inductance. This deteriorates Q factor so, there is no need to fill the all area. Together with these considerations coil area should also be limited in order to decrease resistive loss originating from current generation in the substrate due to magnetic field of the inductor. In addition, to decrease this loss, substrate etching can also be used. This process is basically corroding underneath the area occupied by the inductor [32].

5.4.2.4 Increasing Amplitude of Oscillation

One of the most basic suggestions of phase noise models is keeping oscillation amplitude as high as possible. Fundamental logic behind this fact is that as the signal level increases, noise component nearly remains the same which increases signal to noise ratio. This was also mathematically explained in the phase noise models part. Also increasing oscillation amplitude increases signal charge displacement q_{max} across the oscillation node capacitance which will reduce phase noise degradation as proved in LTV model [43]

One drawback of increasing oscillation amplitude is the need for increasing drawn current from the source which in turn increases power consumption. From this point of view fully differential topology seems to be best way of optimizing between phase noise and power consumption.

5.4.2.5 Reducing Tuning Sensitivity

As it is obvious varactor determines the tuning sensitivity of the oscillator. As it is an element of the resonator and determines the frequency of oscillation by the voltage on it, oscillation frequency is sensitive to noise on this voltage. Remembering that resonator is directly connected to the active device all low frequency noise is imposed on the varactor and it converts this low frequency noise to the phase noise (AM-to-PM conversion), strength of which is determined by the tuning sensitivity of the varactor. So, reducing tuning sensitivity also reduces phase noise in that manner. On the other hand tuning sensitivity directly affects oscillation bandwidth so, reducing it will narrows the frequency band of operation. According to the application circuit should be optimized between phase noise and frequency bandwidth.

5.4.3 Circuit Related Techniques

5.4.3.1 Noise Filtering

In nonlinear time invariant phase noise model, it was found that white noise in biasing circuit at $2n\omega_0 \pm \Delta\omega$ directly generates phase noise. To eliminate this noise a large capacitance C_f can be added in parallel with the current source as shown in Fig. 5.16. Practically, this capacitance shorts the noise at $2n\omega_0 \pm \Delta\omega$ to the ground.

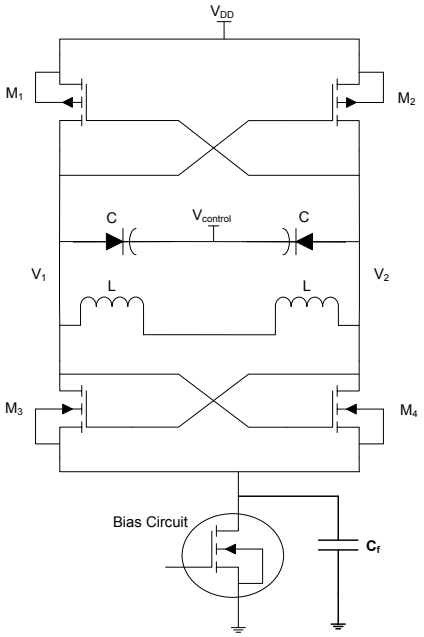


Figure 5.16 : Noise filtering capacitance added in parallel with current source

Another advantage of this capacitance is that it compensates the voltage fluctuations mostly caused by flicker noise of differential pair at common impedance point [53]. As a result less AM-to-PM conversion occurs and phase noise is reduced. However, this capacitor decreases the impedance at common mode point causing degradation of loaded Q factor.

Remember that transistors in an oscillator experience all operation regions in an oscillation period. In triode region output resistance of the transistors decrease effectively which loads the resonator with the impedance at common node point. Therefore low impedance at common node is undesired. In order to compensate decrease in impedance, an inductor can be added between current source and common impedance point as shown in Figure 5.17 [48]. This inductor forms an LC filter with the capacitance of the common source node and also with capacitance of bias circuit. As result impedance of common mode point raised and Q factor is preserved. In addition this LC filter also helps eliminating noise around $2\omega_0$. Note that to preserve symmetry same filtering is also needed at the top section of the circuit, hence another inductor L_2 which forms the same filter along with the node capacitance C_2 is added in between V_{DD} and common mode node at the top.

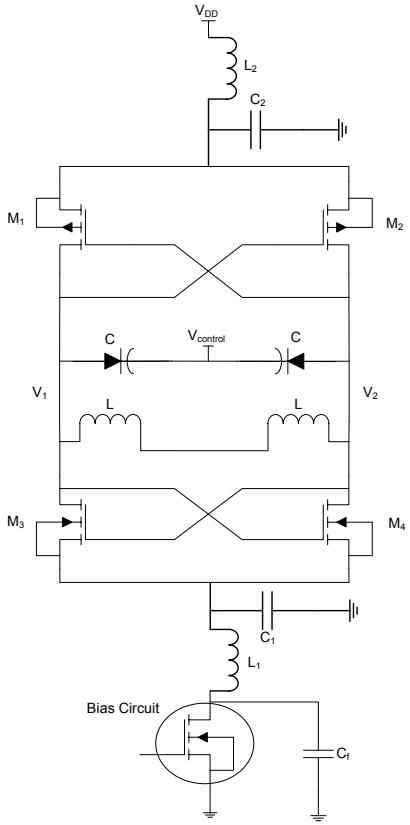


Figure 5.17 : LC filtering by added inductor in between current source and common impedance point

In conclusion, although additional components enlarge the structure and add some extra noise, noise filtering seems to be a very effective way of reducing phase noise.

5.4.3.2 Eliminating Bias Circuit and Resistor Tail Biasing

As discussed in phase noise models section, at large signal operation noise of tail transistors becomes important. If the oscillation amplitude gets larger it even becomes dominant noise source in some operation regions. In practice, to decrease power consumption generally high mirroring ratios (high W/L) are used. This also helps reducing flicker noise contribution in a limited extend. If current biasing circuit is completely eliminated as shown in 5.18 (a), we get rid of the noise of its transistors but while doing that we may give rise to other problems.

By eliminating current bias we lost the control over current consumption and oscillator works in voltage limited region in which the oscillator draws current as much as it can. This situation increases phase noise. This problem may be solved by decreasing transconductance

value by adjusting *W/L* of differential pair transistors smaller but in this case their flicker noise increases [48].

Another problem with this method is degradation of impedance at common mode point. As discussed in the noise filtering part this will lower the Q factor of resonator which will give rise to increase in phase noise.

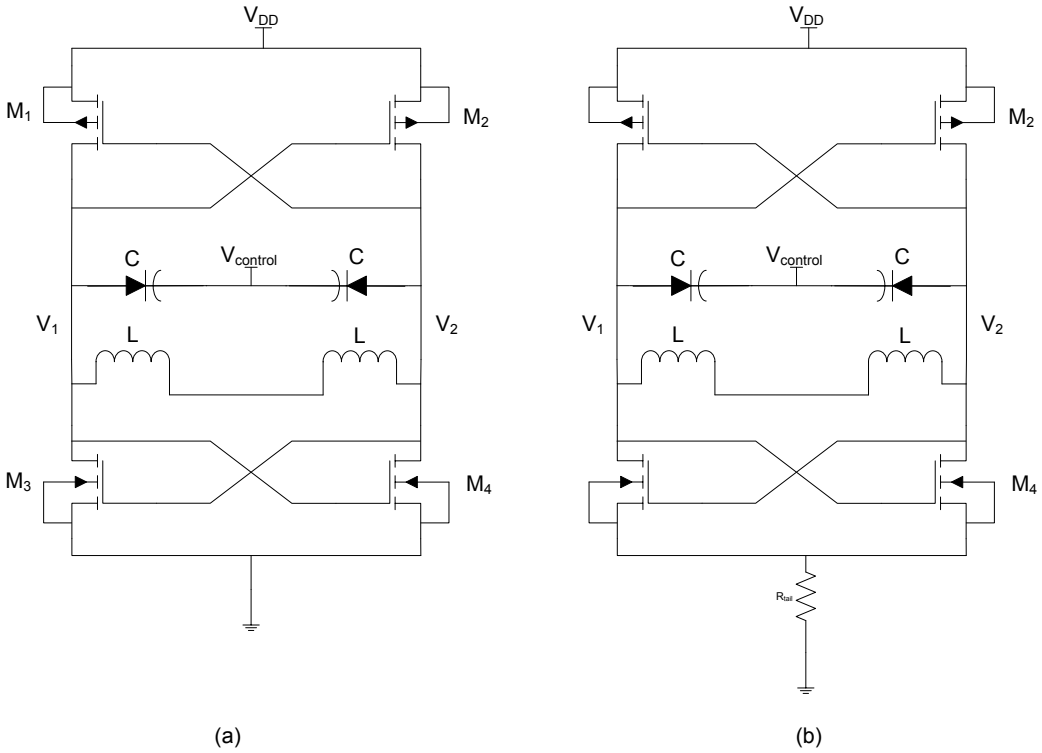


Figure 5.18 : Differential oscillator with (a) no tail biasing (b) resistor tail biasing

A solution to this low impedance problem is resistor tail biasing as shown in Fig. 5.18(b). With a resistor added to common node will raise the common mode impedance and preserve the Q factor [54]. Moreover by adjusting this resistor current consumption can tolerably be controlled. Another advantage of the bias resistor is it can serve as source damping device which can suppress excess 1/f noise of differential pair transistors if cautiously selected [55]. However adding a resistor means adding extra thermal noise. Also oscillator can still be working in the voltage limited regime. Therefore systems with tail resistor bias must be carefully designed and designer should also check the improvement over the version with bias circuit.

5.4.3.3 Discrete Frequency Tuning

Reducing tuning sensitivity of the varactor was said to be a phase reduction technique by reducing AM-to-PM conversion in previous sections. It was also mentioned that while reducing tuning sensitivity frequency band of oscillation also become narrower. This disadvantage can be eliminated by using a capacitor bank and switching between them to cover desired frequency band [48],[53],[56]. An example of bank with three capacitors and frequency tuning characteristics is shown in Fig. 5.19.

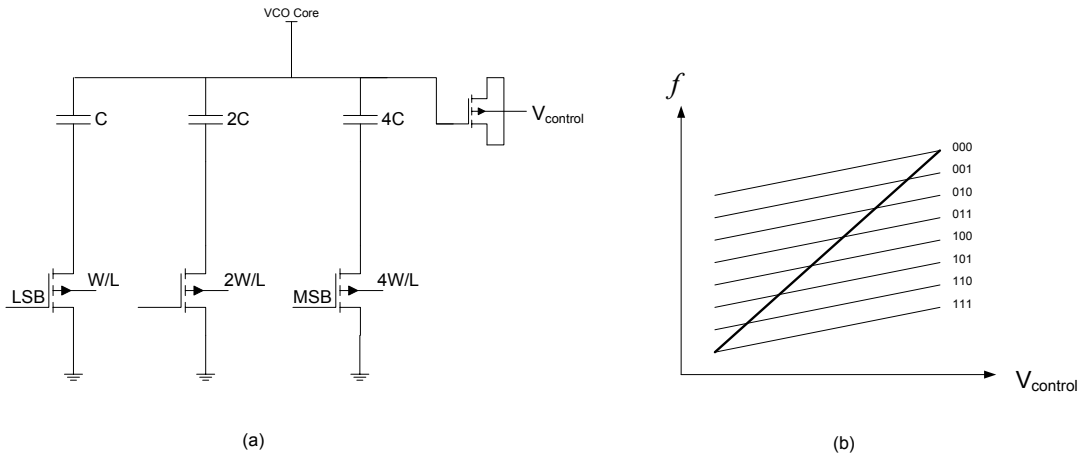


Figure 5.19 : (a) Discrete frequency tuning (b) resultant frequency characteristic

Overlaps between individual configurations enable continuous tuning. Obviously by using switched capacitor array tuning gain is made smaller while the frequency band stands the same in the exchange of extra elements and extra control mechanism. In CMOS technology, generally high quality metal insulator metal (MIM) capacitors are used as constant capacitors.

Drawback of this frequency tuning scheme is that due to finite on resistance R_{on}, MOS switches add extra noise to the system which degrades Q factor. To decrease this resistance W/L ratio of switches should be increased however they cannot be made arbitrarily wide because of their off-state drain to bulk parasitic capacitances. These capacitances limit the achievable tuning range [56]. Therefore a careful optimization is needed for this scheme to be effective.

5.4.3.4 Inductive Degeneration

As discussed in the NLTI phase noise model, flicker noise of tail current source contributes to phase noise by AM-to-PM conversion mechanism. To reduce this effect an inductor is placed in between the current source transistor and ground as shown in Figure 5.20 [48]. Degenerating the current source transistor and shorting the flicker noise to ground, inductor reduces the power of noise current by a factor of $|1 + jg_m\omega L|^2$ which is effective in a frequency band bounded by parasitic capacitance of the inductor and inductance value [57].

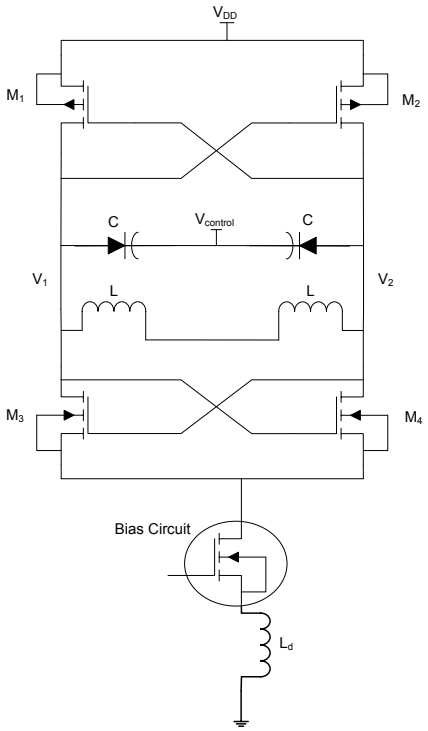


Figure 5.20: Inductive degeneration of current source transistor

For an effective degeneration inductance value should be high. It is difficult and problematic to implement this inductor on the chip, therefore an off-chip inductor which is generally in μH level is used for this purpose.

5.4.3.5 Differential Tuning

In single varactor circuits common mode noise is directly multiplied by the tuning gain and contributes to the phase noise as illustrated in (5.58) where C_0 denotes zero bias capacitance and v_{cm} is the common mode noise.

$$C = C_0 + K_v(V_{cont} - v_{cm}) \tag{5.58}$$

Rejection of this common mode noise can be achieved by differential tuning [58]. The topology consists of two pairs of varactors as shown in Figure 5.21 (a). One pair is excited in cathode (C_1) while the other pair is excited in anode (C_2). Capacitance characteristic is shown in Figure 5.21 (b).

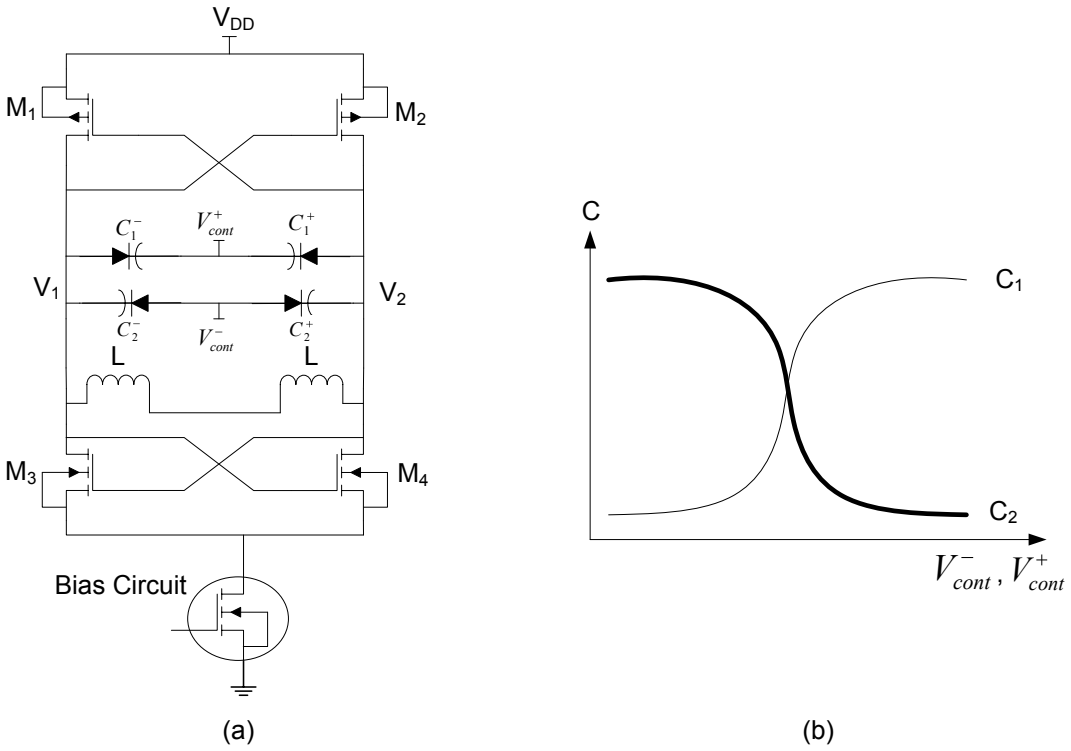


Figure 5.21 : (a) Differential tuning (b)capacitance curve

Assuming that the varactors are perfectly symmetrical, i.e $K_{v,1} = K_{v,2} = K_v$, opposite excitation enables the system to eliminate common mode noise by the simple mathematics explained in the following part. Capacitances of each branch can be written as:

$$C_1^+ = C_0 + K_{v,1}(V_{cont}^+ - v_{cm}) \tag{5.59}$$

$$C_2^+ = C_0 + K_{v,2}(v_{cm} - V_{cont}^-) \tag{5.60}$$

Since $C = C_1^+ + C_2^+$ and varactors are symmetric resultant capacitance is:

$$C = 2C_0 + K_v(V_{cont}^+ - V_{cont}^-) = 2C_0 + K_v(V_{cont}) \tag{5.61}$$

The calculations show that common mode noise is rejected. Therefore up-conversion of low frequency noise, i.e. flicker and shot noise is reduced by differential tuning.

Another problem with the varactors is instantaneous imbalance in the circuit. Instantaneous voltage of V_1 and V_2 is different in most of the oscillation period. As a result instantaneously capacitance values become different which creates imbalance in the circuit. This imbalance creates even harmonics of oscillation to flow through V_{cont}. This situation degrades Q factor. If a destructive effect of this situation is observed, a noise filter may be used to eliminate parasitic even harmonics as shown in Fig. 5.22 [48]. Note that L_c and C_c should be adjusted to filter $2\omega_0$.

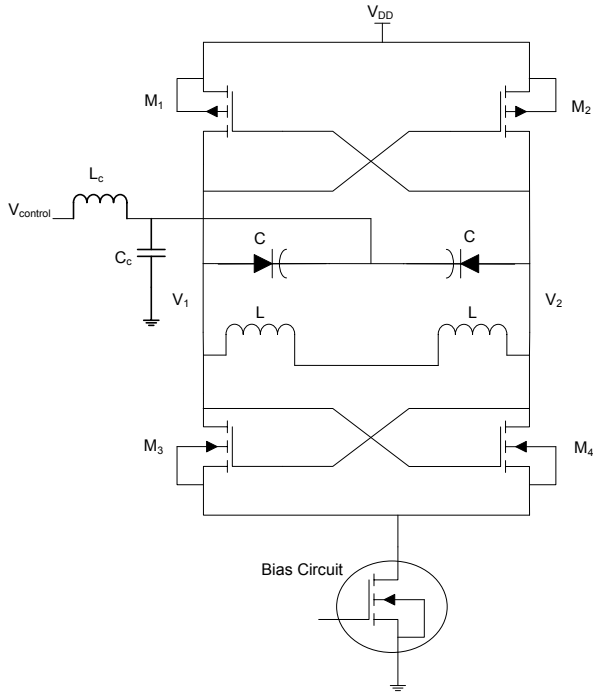


Figure 5.22 : Harmonic filter on control voltage

CHAPTER 6

LOW PHASE NOISE VCO DESIGN

In light of the background information about voltage controlled oscillators and research on phase noise reduction techniques, a low phase noise CMOS VCO is designed. Following the core design, different phase noise reduction techniques are applied and effects are simulated. In all phases of the design ADS 2008 CAD tool is used together with the TSMC 0.18 μm technology library. In this chapter, first, CAD based voltage controlled oscillator design will be explained. Then, effects of phase noise reduction techniques will be discussed. Design will be finalized with applying the practical and most effective reduction techniques to the VCO core.

6.1 VCO Design

As mentioned before VCO is composed of three main parts namely active circuit, resonator and bias circuit. Although design of each part can be done separately, because of the strong interactions in between the parts, it is more logical to think the system as a whole and make design accordingly. Then responses of individual sections can be checked if any ridiculous conditions exist. In this work, active circuit and resonator are designed separately but they are optimized in the system simulations. Then, individual parts are re-checked to see the effects of tuning. In the following parts, main building blocks of VCO will be discussed.

6.1.1 Varactor

In the core design MOS varactor is used. For the applications which need wide tuning range accumulation mode MOS varactors are used. Accumulation mode varactors are implemented by removing D-S diffusions from MOS device and implementing n^+ bulk contacts instead. By doing so, formation of inversion regions is inhibited [59]. In this work, since there is no need for wide tuning range, MOS varactor is used in depletion region. Therefore there is no need for an extra process that is needed for accumulation mode MOS varactor. Simulation

circuit and capacitance curve of varactor is shown in Fig. 6.1 and Fig. 6.2 (a) respectively. Actually width and length of the MOS varactor are chosen with an optimization of the complete system which will be seen later in this chapter. Bias voltage is changed between -1 V and 0.5 V which corresponds to depletion region of the complete capacitance curve which is also shown in Fig. 6.2(b).

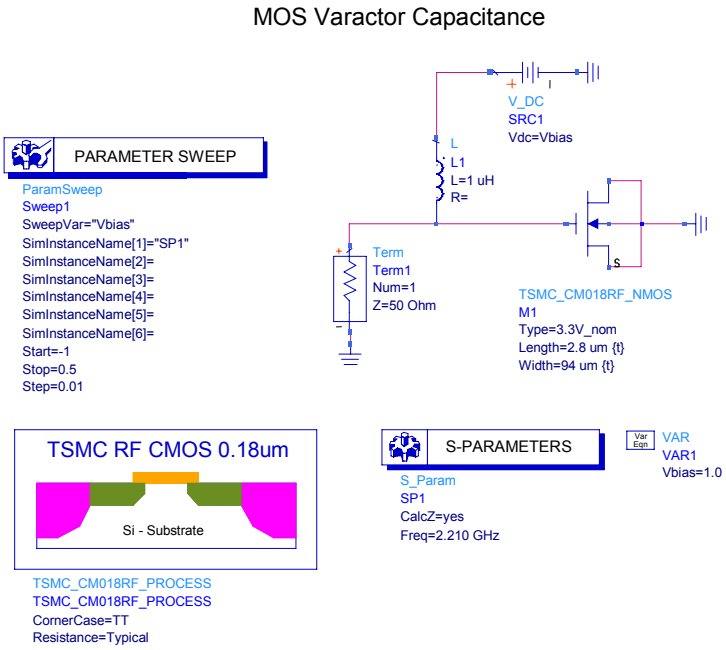


Figure 6.1 : Capacitance simulation circuit of MOS varactor

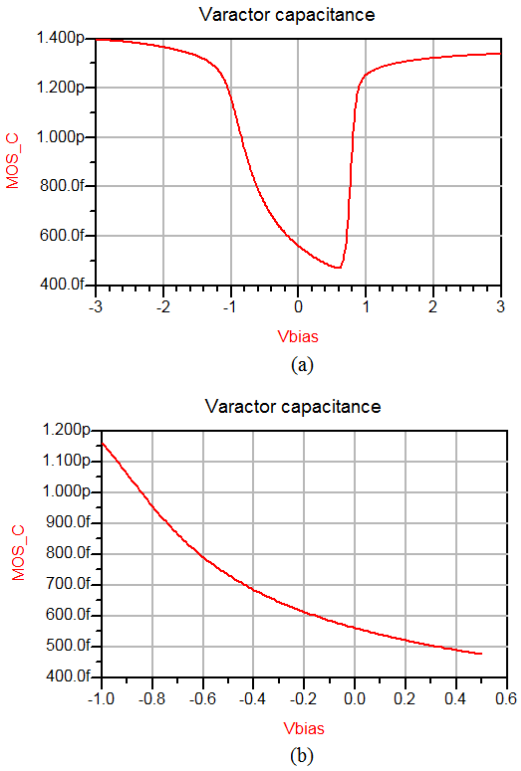


Figure 6.2 : (a) Complete capacitance curve (b) capacitance in depletion region of MOS varactor

In the differential oscillator design, to preserve symmetry two back to back connected varactors are used as shown in Fig. 6.3 and linear section of the capacitance curve given in Fig. 6.4 is used which corresponds to tuning voltage in between 0 V and 1 V.

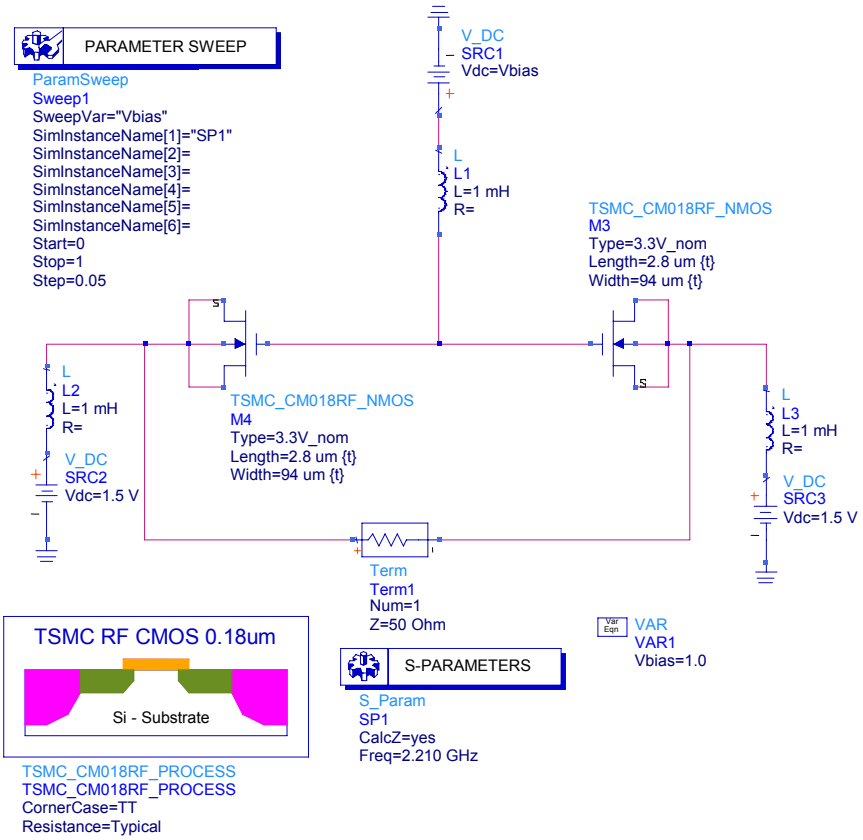


Figure 6.3 : Used varactor structure in VCO design

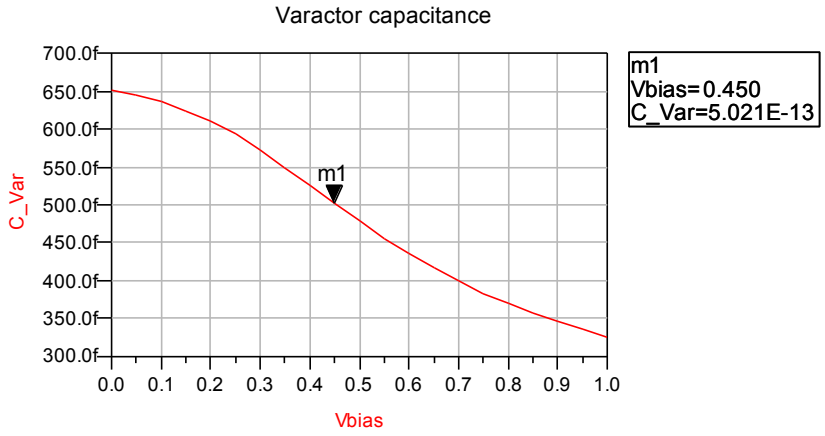


Figure 6.4 : Used portion of the capacitance curve of varactor structure

6.1.2 Active Circuit

As stated before in this work, fully differential topology is used. Also widths of the PMOS transistors are adjusted as three times those of NMOS counterpart to match their transconductances. As bias circuit, cascaded NMOS current mirror is preferred to decrease the effect of channel length modulation parameter and increase the output resistance [60]. Copying ratio is adjusted as nearly five with an optimization between power consumption and phase noise. Simulated copying ratio is approximately 4.6, i.e. 600 μA is boosted to 2.76 mA. Total current drawn is nearly 3.36 mA from 3 V supply.

Simulation circuit of negative resistance presented to resonator is given in Fig. 6.5 and result is shown in Fig. 6.6. In the calculation, voltage over the current source is divided by current generated to find resistance presented to resonator. Simulated negative resistance values can be used to check if oscillation condition is satisfied. In this work oscillation test is done in simulation of whole system.

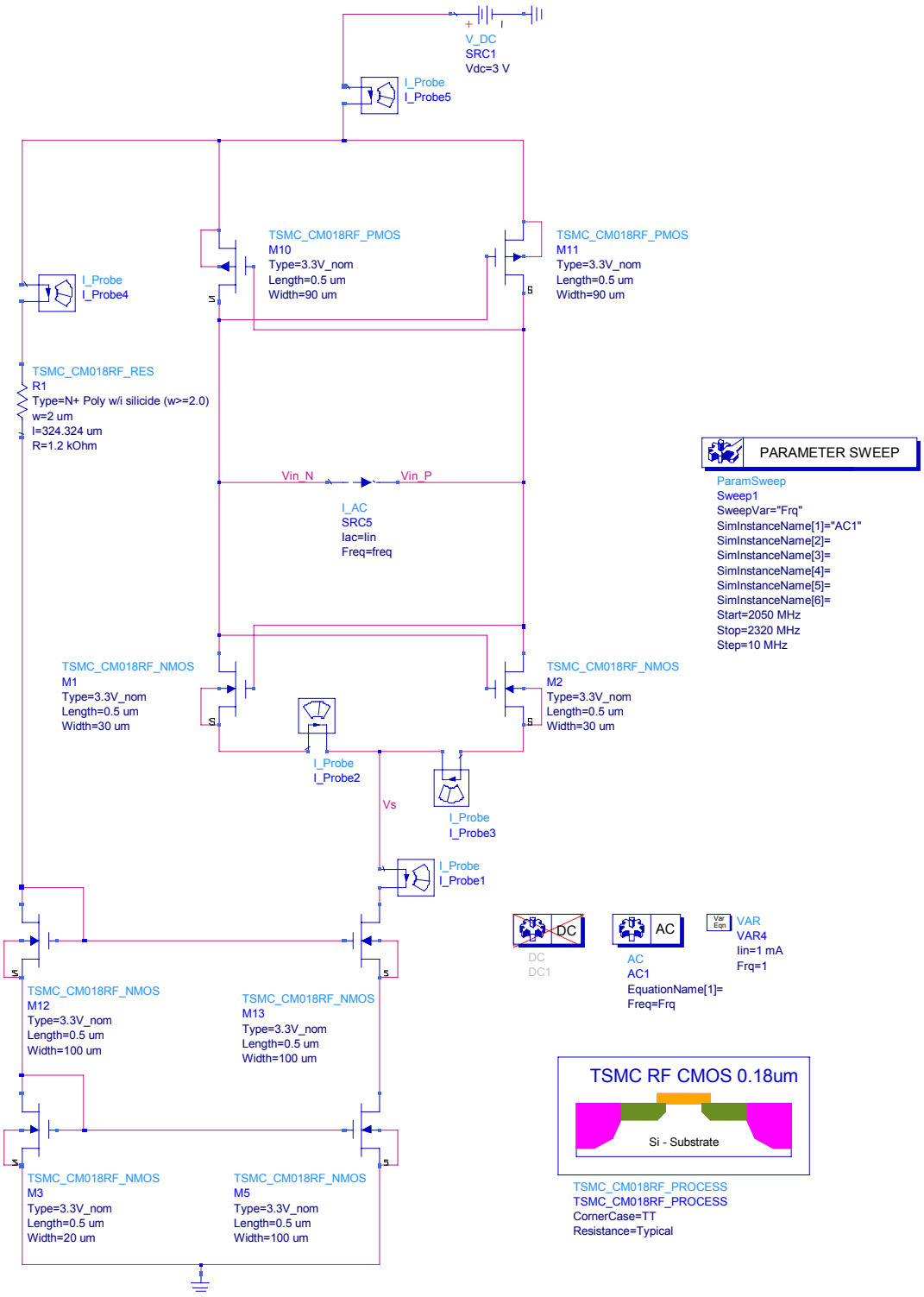


Figure 6.5 : Negative resistance simulation circuit

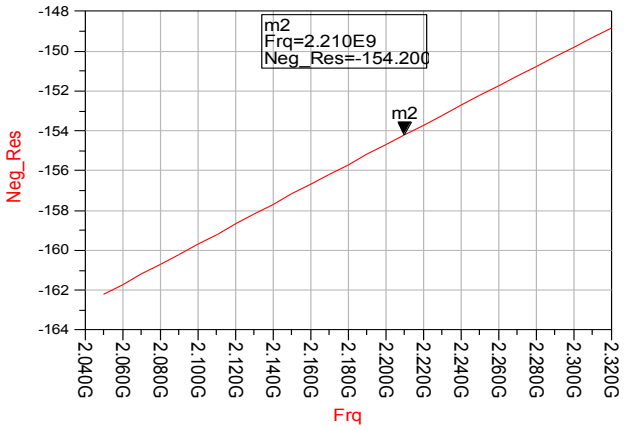


Figure 6.6 : Negative resistance of the active part

6.1.3 Resonator

Resonator is designed using the varactor structure which is described above and a 4.5 turn approximately 6 nH spiral inductor which is shown in the simulation circuit given in Fig. 6.7. Magnitude and phase responses are shown in Fig. 6.8.

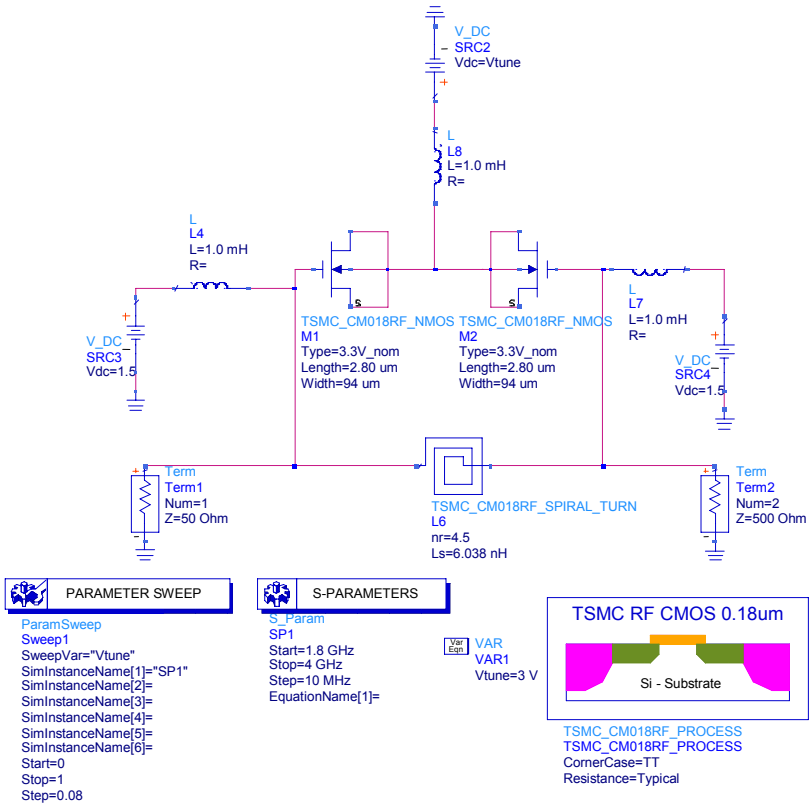


Figure 6.7 : Frequency response simulation circuit of resonator

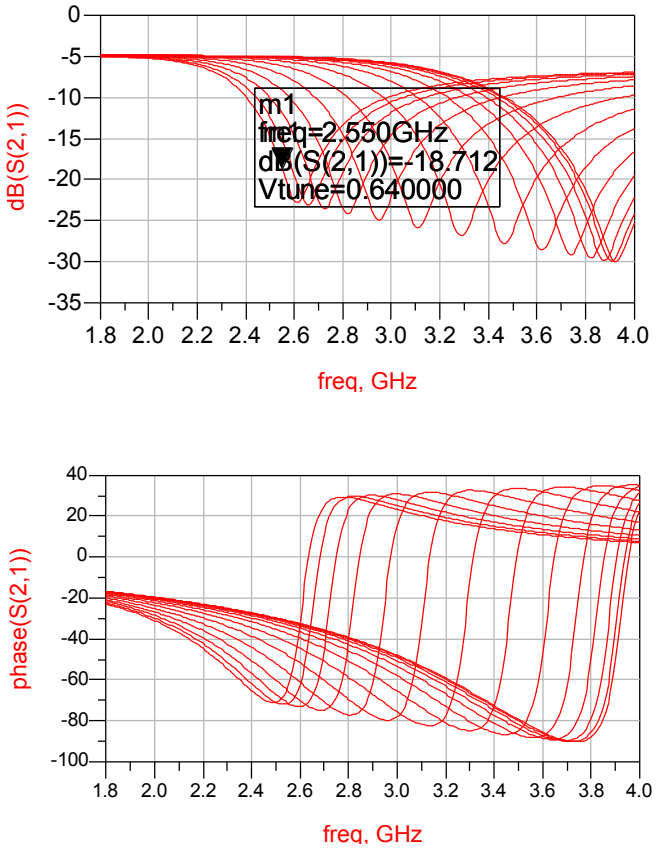


Figure 6.8 : Frequency response of the resonator

As seen in the frequency response of the resonator, resonance frequency band is above the desired band. With the addition of capacitances of the transistors in active circuit, resonance frequency will decrease. Therefore it is better to see frequency response in the simulations of the whole system.

As stated in oscillator models section, to maintain oscillation resonator loss should be compensated by the active circuit. To see if this is satisfied, resonator impedance and impedance of active circuit can be simulated to see if negative resistance supplied by the active part cancels resonator loss. In the simulation of resonator impedance, both frequency and tuning voltage are swept. Impedance corresponding to correct tuning voltage and frequency pair should be matched to impedance of the active circuit. In this work a more efficient and easier test method is used. In this method, basically S-parameter simulation is done in whole system to see if magnitude of S_{11} is greater than one where its phase is zero. Details of this test are explained in the following section.

6.1.4 Oscillation Test

Actually in ADS “OscPort2” component that is used to simulate differential VCO checks if oscillation condition is satisfied or not. However in that simulation oscillation margins can not be seen. Therefore to control the margins of oscillation a separate oscillation test should be done.

Effective way of testing if oscillation condition is satisfied for the desired frequency band is using “OscTest” component. This component simply performs an S parameter simulation in desired frequency band, and evaluates closed loop gain of the system. From S-parameters, frequencies where magnitude of closed loop gain is greater than one and phase is zero can be observed. For those frequencies it can be said that oscillation condition is satisfied. The circuit for “OscTest” simulation is shown in Fig. 6.9.

Examining the magnitude and phase plots given in Fig. 6.10 and Fig. 6.11, it can be seen that oscillation condition is satisfied in between 2.05 GHz and 2.35 GHz which define bandwidth of oscillation in complete system simulations. Approximate level of magnitude is four which is satisfactory for safety of oscillation start-up.

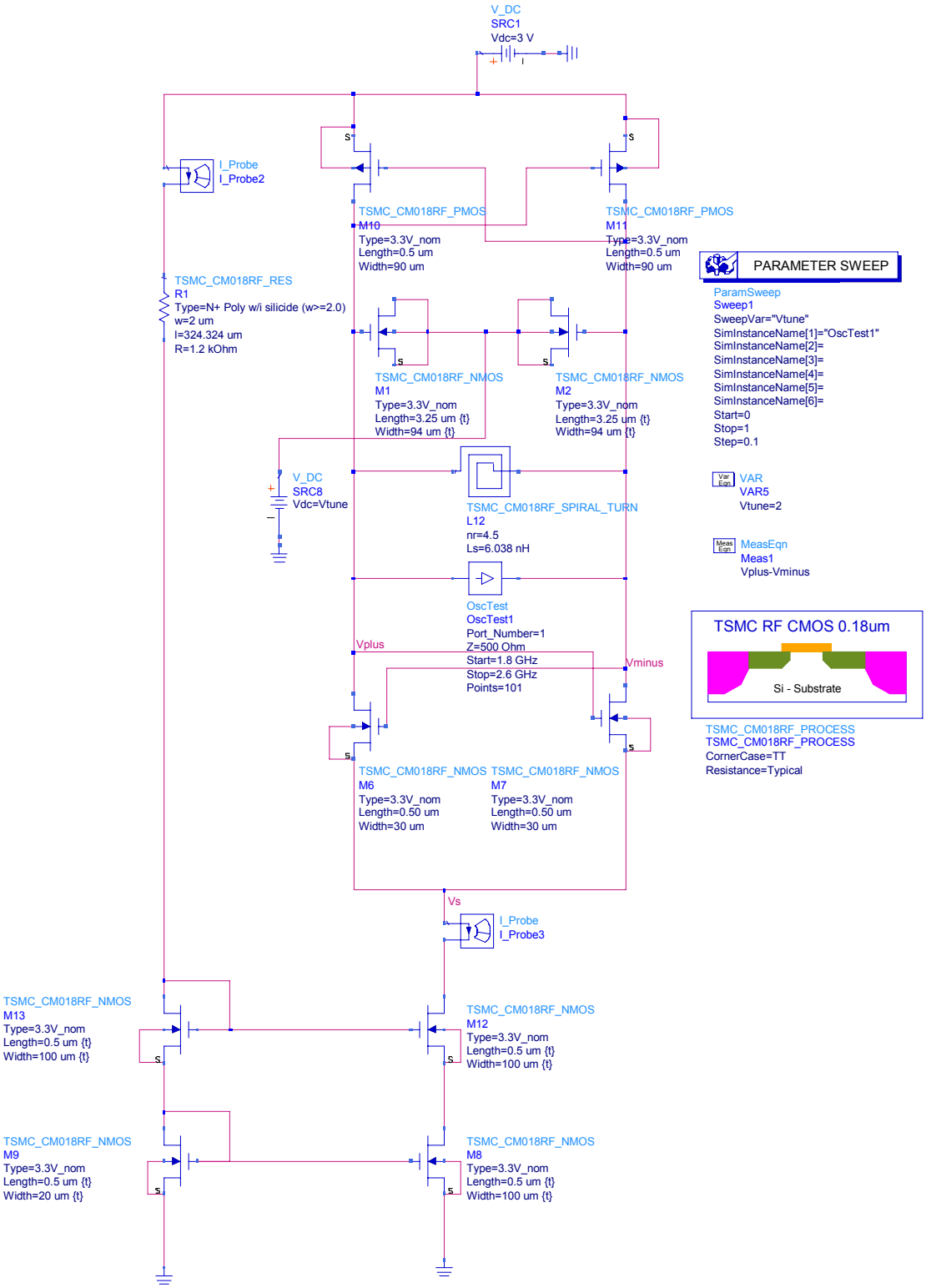


Figure 6.9 : Oscillation test setup

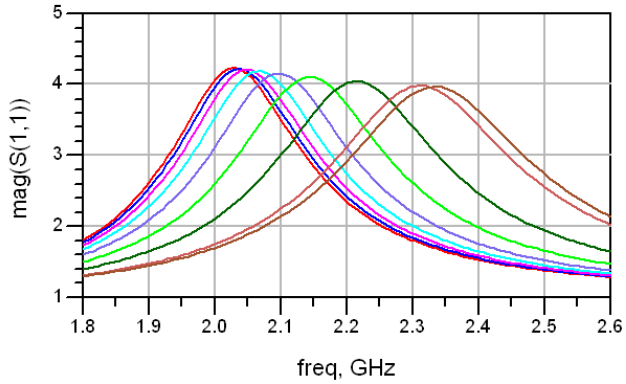


Figure 6.10 : Magnitude of S_{11} for testing oscillation start-up

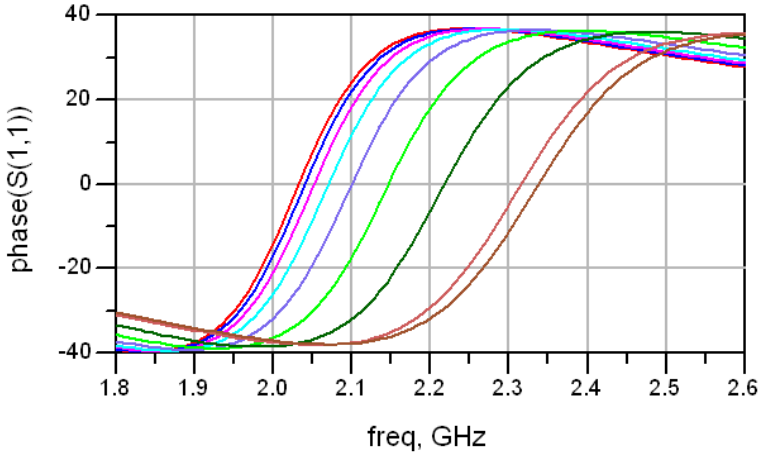


Figure 6.11 : Phase of S_{11} for testing oscillation start-up

6.1.5 Complete VCO

VCO design is completed by combining resonator and active part as shown in Fig 6.12. Using "OscPort2" component, a harmonic balance simulation is done to get oscillator spectrum, tuning characteristics, time domain signal and phase noise characteristic. Circuit is optimized by tuning varactor FET, and width and length of transistors in the active circuit. Responses of the finalized core design are given from Fig. 6.13 to Fig. 6.16.

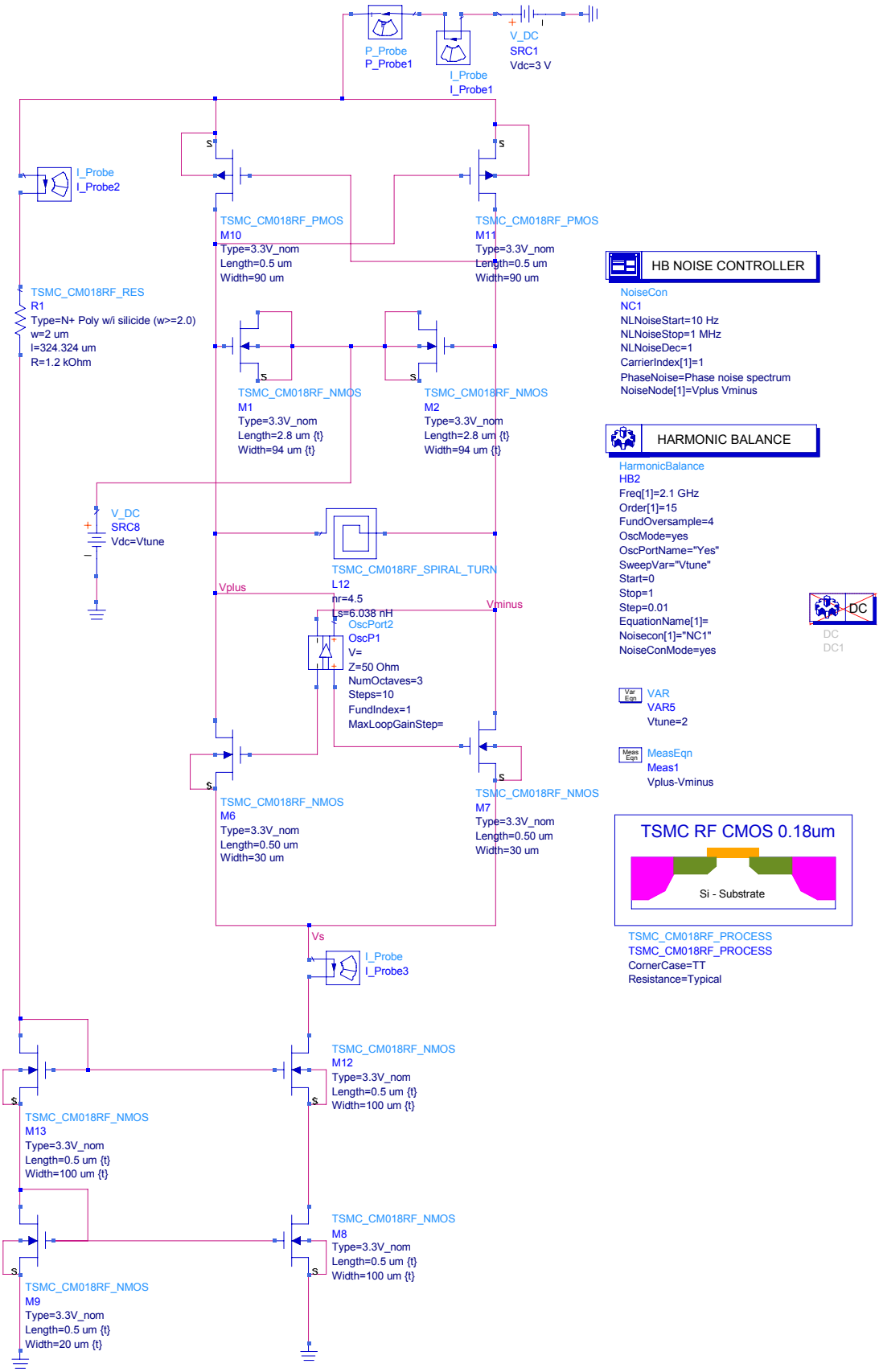


Figure 6.12 : Designed VCO core

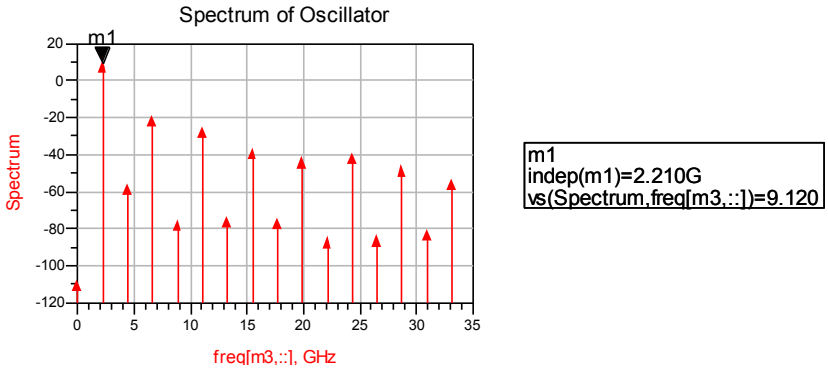


Figure 6.13 : Spectrum of the VCO tuned at 2.21 GHz

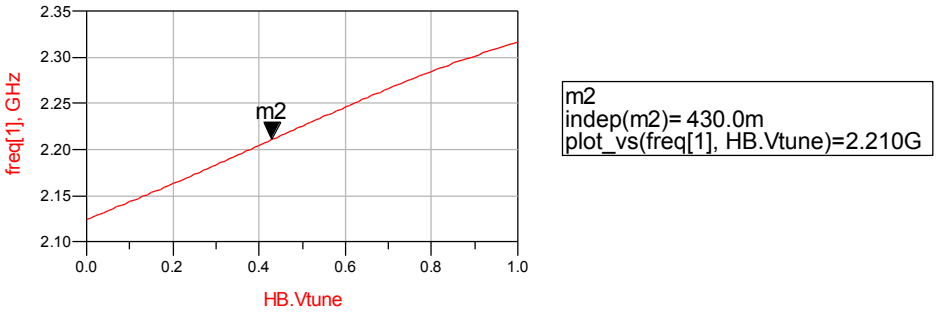


Figure 6.14 : Tuning characteristics of the VCO

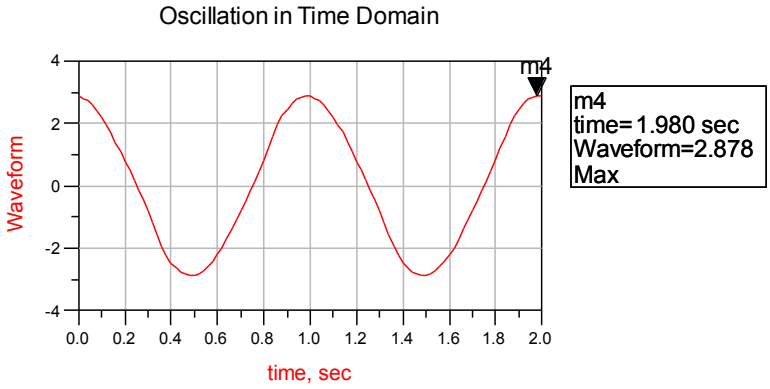


Figure 6.15 : VCO Output view in time domain

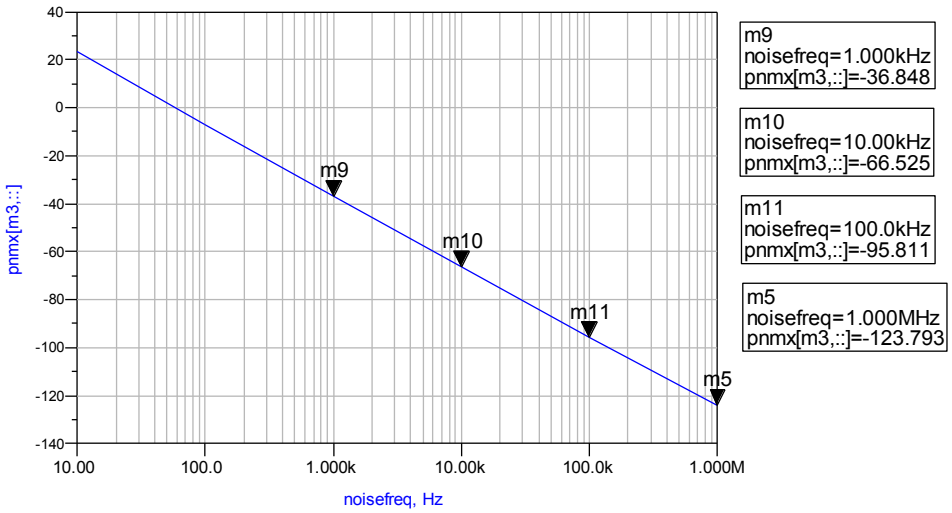


Figure 6.16 : Phase noise response of the VCO

Designed VCO is calculated to have approximately 10 mW power consumption with approximately 9 dBm fundamental frequency output. Strengths of the first ten harmonics for oscillator tuned at 2210 MHz are summarized in Table 6.1.

Table 6.1 : Spectrum of the designed VCO tuned at 2210 MHz

Frequency (GHz)	**Power (dBm)**
2.21	9.12
4.42	-57.27
6.63	-20.19
8.84	-76.54
11.05	-26.10
13.26	-74.98
15.47	-37.78
17.68	-75.45
19.89	-42.67
22.10	-85.72

As can be viewed in the table differential structure nearly eliminates even harmonics. This effect will also be the same for common mode noise. As seen in Fig. 6.14 oscillator can be tuned form 2.126 GHz to 2.315 GHz by changing bias voltage from 0 V to 1 V. This corresponds to 8 % bandwidth. Tuning characteristic is not perfectly but approximately

linear with an average tuning sensitivity of 191 MHz. As expected voltage swing is approximately between +V_{DD} and -V_{DD} which corresponds to 6 V.

As can be read in Fig. 6.16, phase noise is measured as -36.848 dBc/Hz at 1 kHz, -66.52 dBc/Hz at 10 kHz ; -95.811 dBc/Hz at 100kHz and -123.793 dBc/Hz at 1 MHz offset from the carrier. In the following parts previously studied phase noise reduction techniques will be applied to the core design to see the effects.

6.2 Phase Noise Reduction

6.2.1 Reducing VCO gain

VCO gain can simply be reduced by decreasing width and length of MOS varactor. To compensate increase in the resonance frequency resulting from the decrease in capacitance of the varactor, either extra constant capacitance can be inserted to the circuit or inductance value can be increased.

In the first method, without changing value of inductance, a constant MIM capacitance of 0.23 pF is inserted to circuit as shown in Fig. 6.17 and width and length of the varactor capacitances are tuned to 94 µm and 1.6 µm to make tuning bandwidth approximately 100 MHz in average and make tuning bandwidth 4.7% (2.145 GHz - 2.248 GHz) as shown in Fig. 6.18. New phase noise plot is illustrated in Fig. 6.18. Improvement is about 8 dB at 100 kHz offset and 5.5 dB at 1 MHz offset.

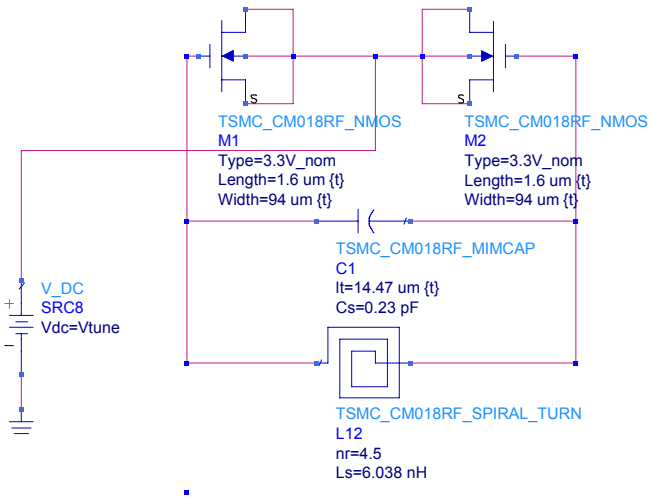


Figure 6.17 : Reducing VCO gain by constant capacitance insertion

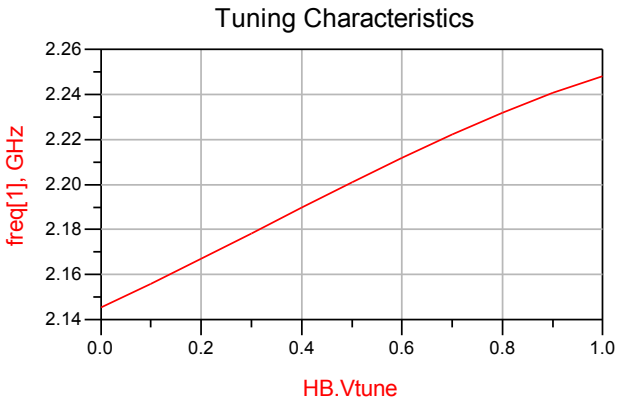


Figure 6.18 : Tuning characteristics with constant capacitance insertion

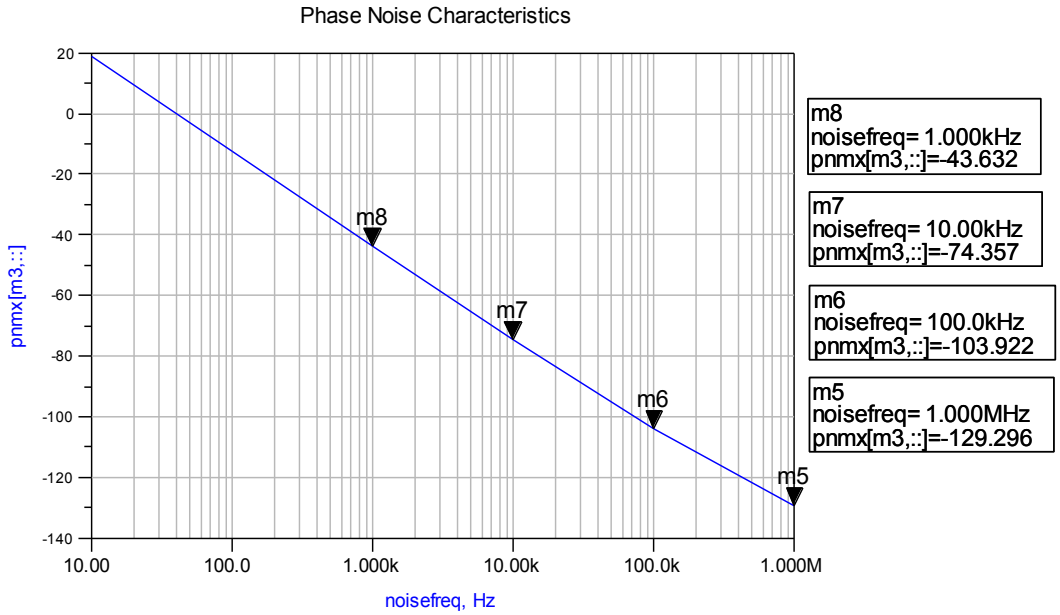


Figure 6.19 : Phase noise characteristics with constant capacitance insertion and reduced VCO gain

In second method, shown in Fig. 6.20, width and length of the varactor are decreased to 84 µm and 1.3 µm respectively. Also inductor is made 5.5 turn which corresponds to 9 nH. These changes decrease tuning gain to 100 MHz in average and make tuning bandwidth 4.7% (2.145 GHz -2.248 GHz) as illustrated in Fig 6.21.

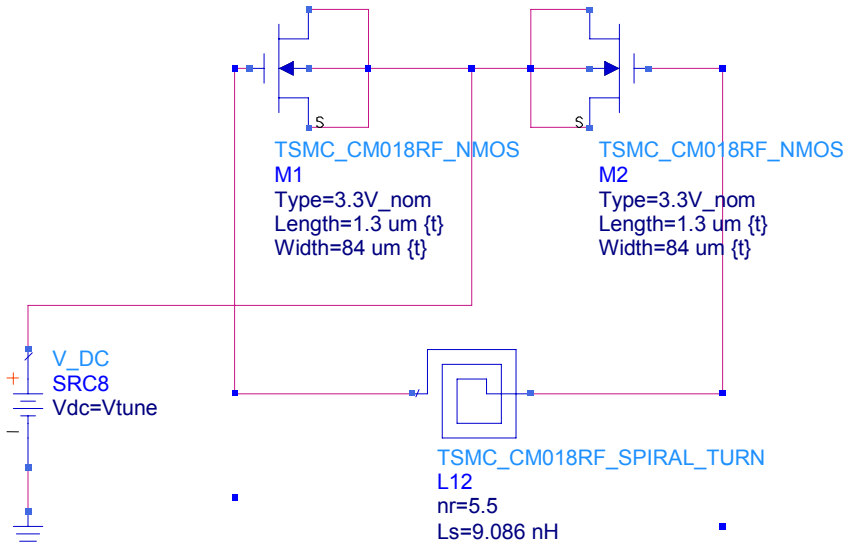


Figure 6.20 : Reducing VCO gain by increasing inductance

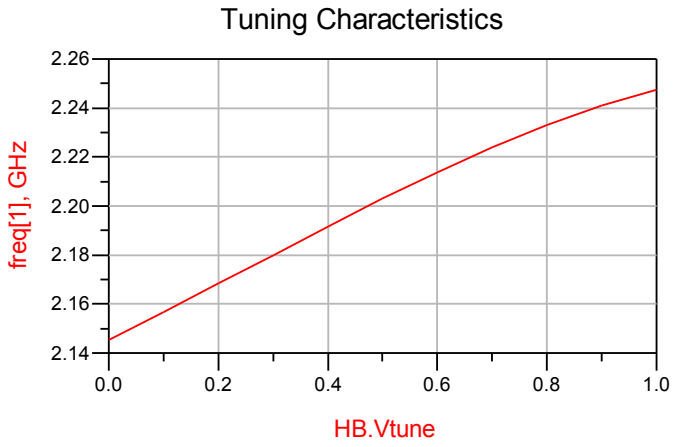


Figure 6.21 : Tuning characteristics with increased inductance value

Resultant phase noise characteristic is shown in Fig. 6.22. As can be viewed from the results improvement is about 6.3 dB at 100 kHz offset and 3 dB at 1 MHz offset. As stated before increasing value of inductor means adding extra turns which will increase the loss and phase noise. Therefore inserting constant capacitance is more reasonable and more effective way of reducing VCO gain.

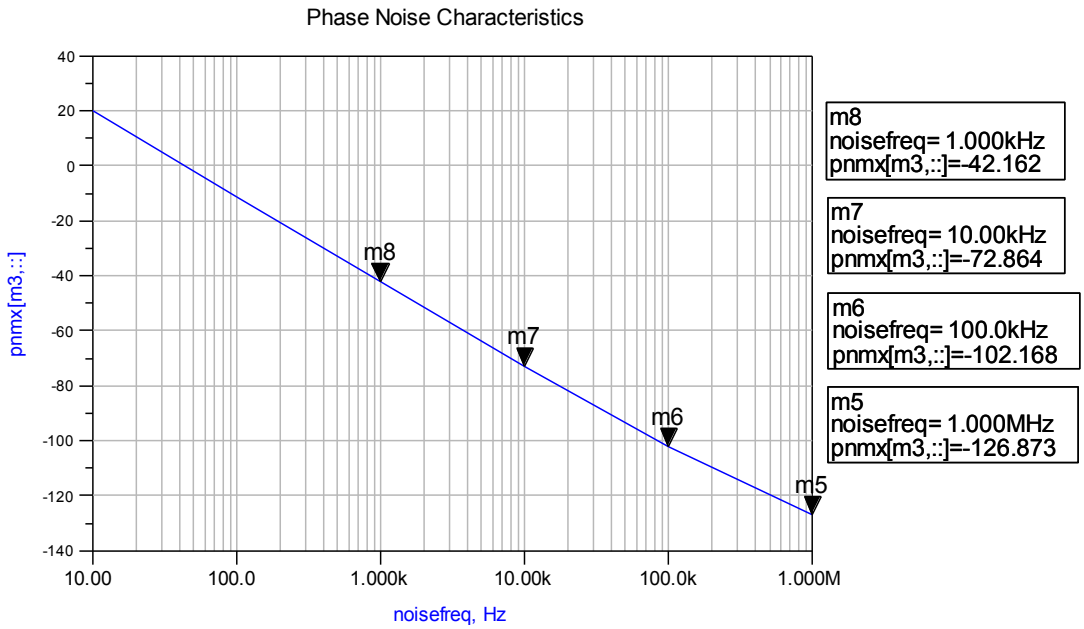


Figure 6.22 : Phase noise characteristics for reduced VCO gain with increased inductance

6.2.2 Noise Filtering

To eliminate white noise generated by biasing circuit and to compensate voltage fluctuations at common source node, a capacitance is added to the circuit as shown in Fig. 6.23. It is obtained from the simulations that to get a significant improvement on the phase noise the capacitance value is found to be at least 100 nF. In this case voltage fluctuation at common source point is completely eliminated. Phase noise plot for 100 nF capacitive filtering is shown in Fig. 6.23.

In this simulation added capacitance is an ideal one. Certainly, an integrated one will have some restrictions on the value of capacitance. For the used technology to get a 100 nF capacitance an edge length of 9.5 mm is required which is not realistic to implement. Phase noise plot for this case is given in Fig. 6.24. Although improvement is about 6.4 dB at 100 kHz and 4 dB at 1 MHz offset, capacitive noise filtering is not seem to be useful because of the technology restrictions.

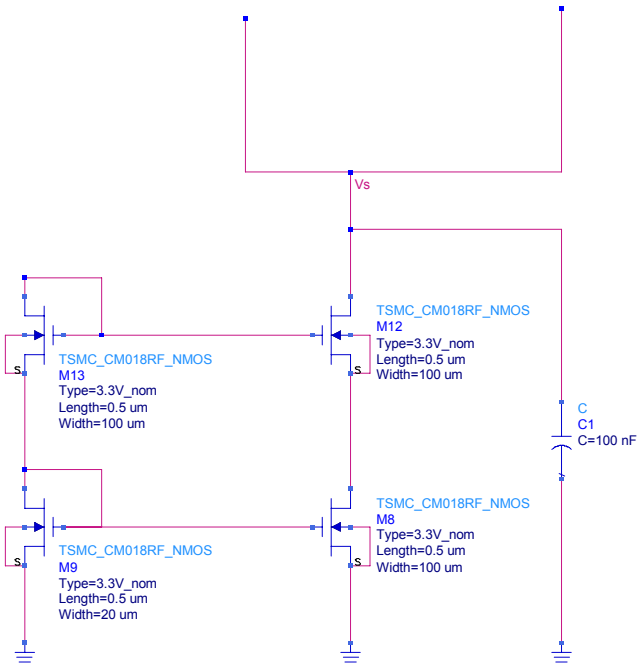


Figure 6.23 : An ideal noise filtering capacitance in parallel with biasing circuit

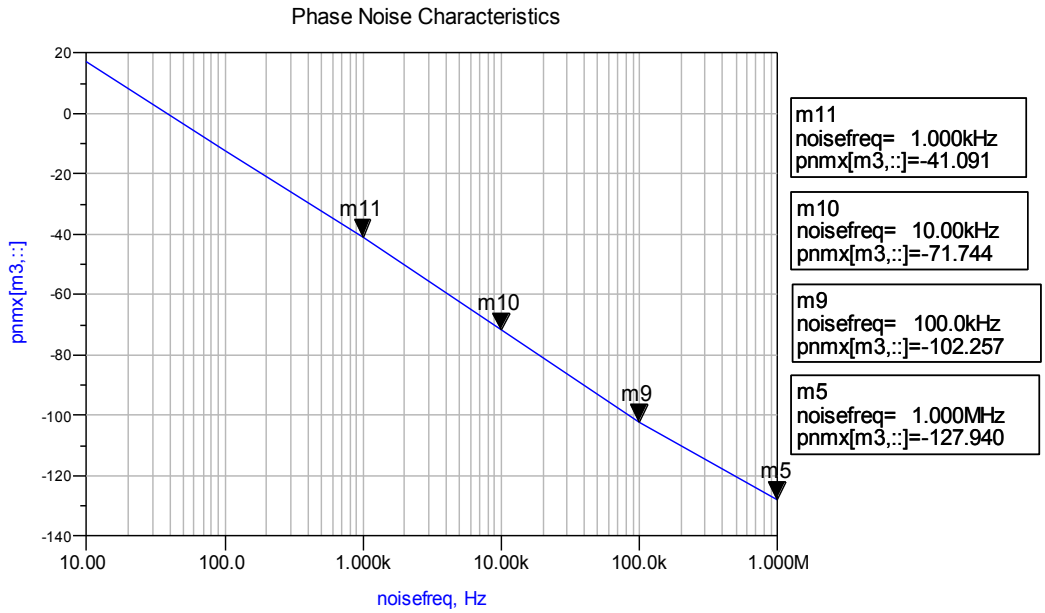


Figure 6.24 : Phase noise plot with 100 nF capacitive filtering

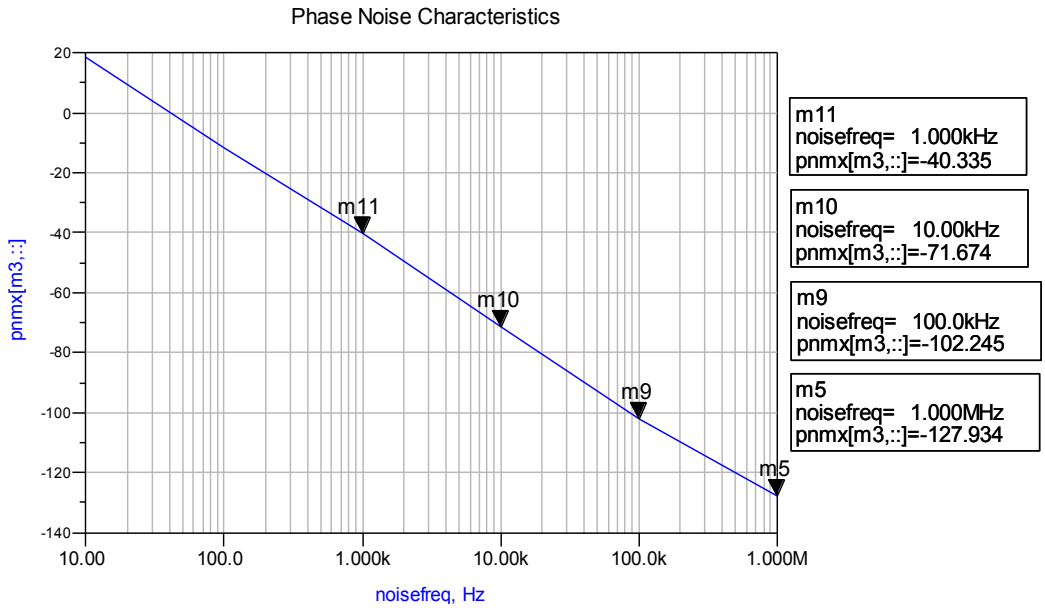


Figure 6.25 : Phase noise plot for 100 nF MIM capacitance

As mentioned previously, another filtering method is forming an LC filter by inserting inductor in between bias circuit and common source point. Although adding extra spiral inductor increases chip area and adds extra noise this method is more realistic to implement on chip then capacitive filtering. An optimized inductor is of 5.5 turn approximately 9 nH as shown in Fig. 6.25. An improvement about 3.7 dB at 100 kHz and 3 dB at 1 MHz offset is observed with this method as illustrated in the phase noise plot in Fig. 6.26.

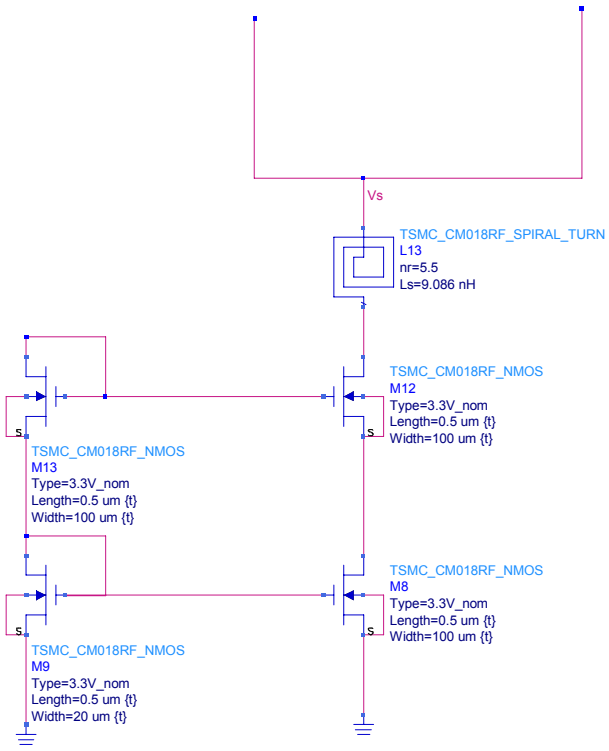


Figure 6.26 : LC noise filtering by inductor insertion

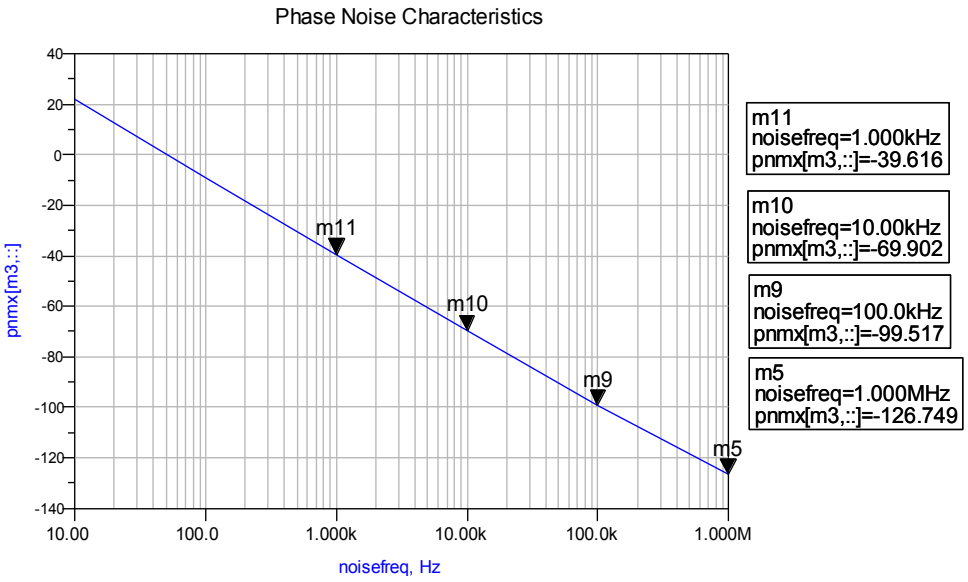


Figure 6.27 : Phase noise plot for LC noise filter

6.2.3 Eliminating Bias Circuit and Resistor Tail Biasing

By eliminating bias circuit, noise coming from the transistors of biasing circuit is completely eliminated. Although impedance at common source point decreases with connecting it to ground, the total effect on the phase noise is an improvement about 6 dB as can be viewed in Fig. 6.27.

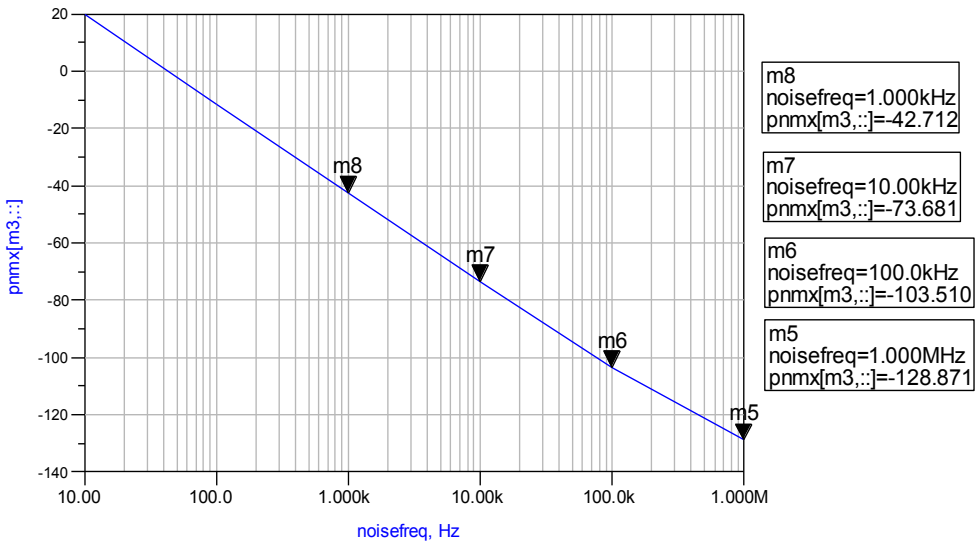


Figure 6.28 : Phase noise plot with no biasing circuit.

As stated before without biasing circuit, system works in the voltage limited region and control over power consumption is lost. However in biasing circuit case to increase amplitude of oscillation circuit was optimized to work in the limits of voltage and current limited regions. Therefore power consumption only increases by approximately 1 mW in no biasing case. Also amplitude of oscillation increases from 2.88 V to 3 V. One significant disadvantage of working in the voltage limited region is that level of the harmonics increase as summarized in Table 6.2.

Table 6.2 : Table of harmonics in no bias case

Harmonics	Level (dBm)
1st	9.622
3rd	-17.25
5th	-24.75
7th	-34.31
9th	-41.98

To increase impedance at common source point and also to get control over power consumption back, a resistor is inserted to common source point. This technique has great effect on the general performance of the system. First, transistors of the biasing circuit are removed which means noise and extra power consumption of them is completely eliminated. Second, circuit can still be worked in current limited region by resistive control on the power consumption so that increase in level of harmonics, which was observed in no bias case, is not seen. Third, impedance at common source node can be controlled by the added resistor.

In the simulations, biasing resistor is optimized to 200 Ω as shown in Fig. 6.29. Power consumption is decreased to 7 mW while preserving oscillation amplitude at approximately 2.83 V. Phase noise improvement is about 7.4 dB at 100 kHz and 5.5 dB at 1 MHz offset as illustrated in Fig. 6.30. Reducing both power consumption and phase noise, resistor biasing effectively improves Figure of Merit (FOM) which is a generalized measure of oscillator performance and formulated as given in (6.1) where $\mathcal{L}(\Delta\omega)$ is phase noise at $\Delta\omega$ offset from center frequency, ω_0 is center frequency and P_{diss} is the power dissipation.

$$FOM(dBc) = \mathcal{L}(\Delta\omega) - 20\,log\left(\frac{\omega_0}{\Delta\omega}\right) + 10\log(P_{diss}(mW)) \quad (6.1)$$

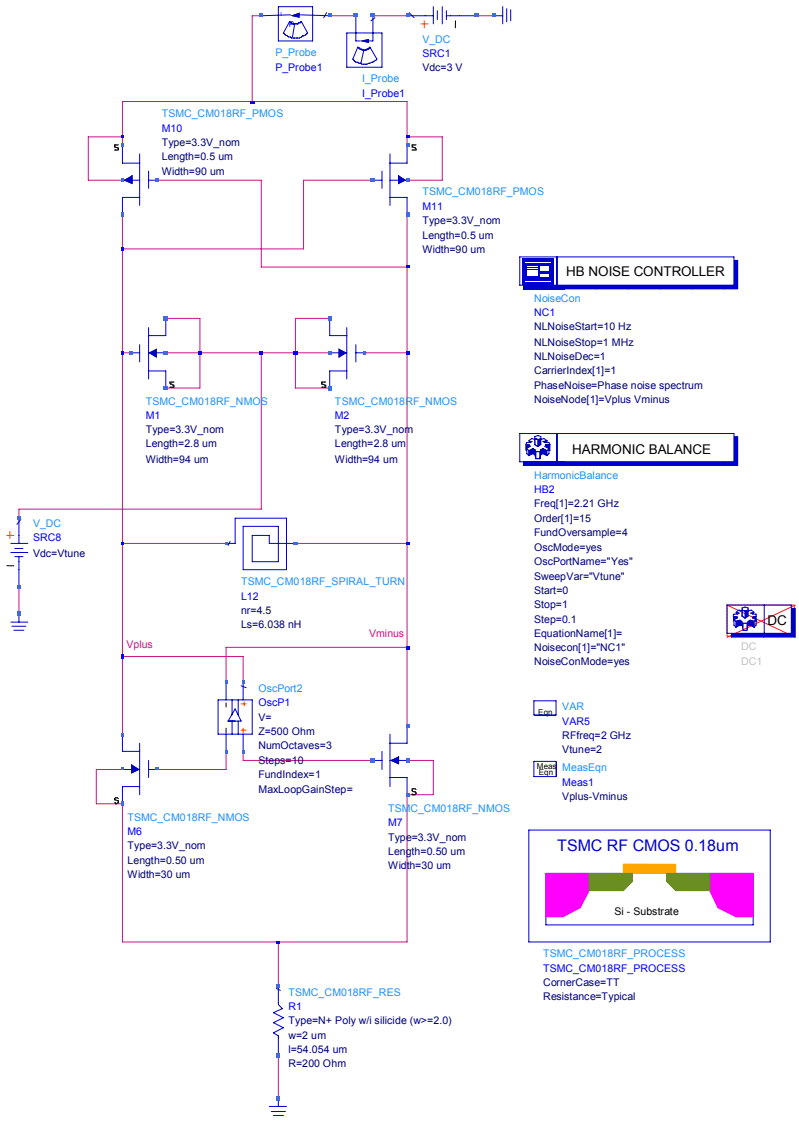


Figure 6.29 : VCO with resistor tail biasing

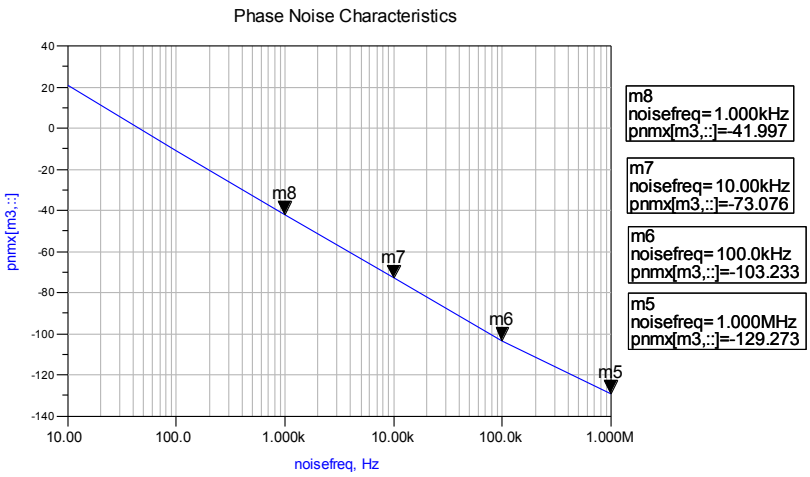


Figure 6.30 : Phase noise plot with resistor tail biasing

6.2.4 Inductive Degeneration

To reduce the effect of flicker noise of tail current source an off-chip inductor is used as shown in Fig. 6.30. Since the inductor is off-chip its value is not restricted with the used technology. In the simulations it is found that 1 µH has quite effective to reduce phase noise as illustrated in Fig. 6.31.

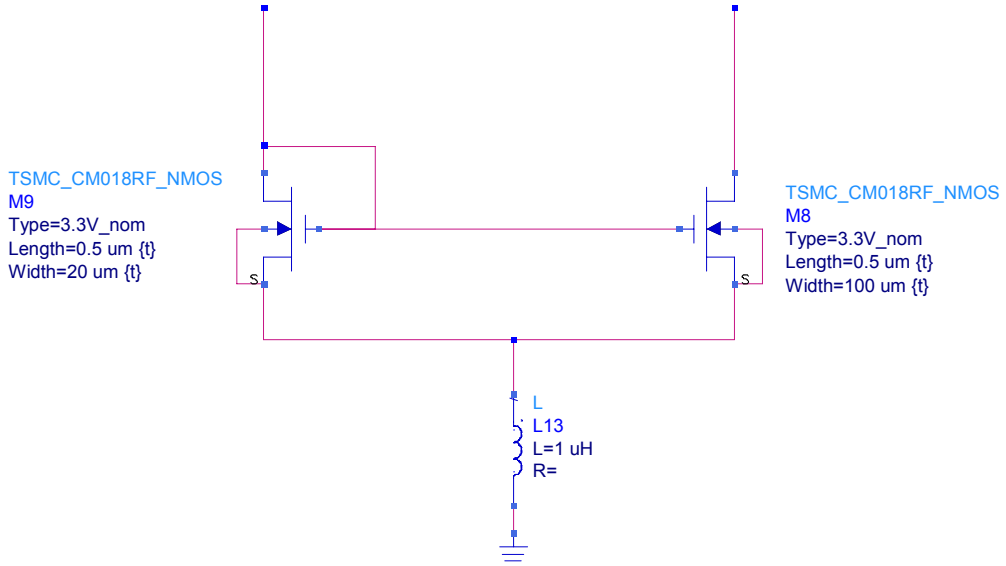


Figure 6.31 : Inductive degeneration

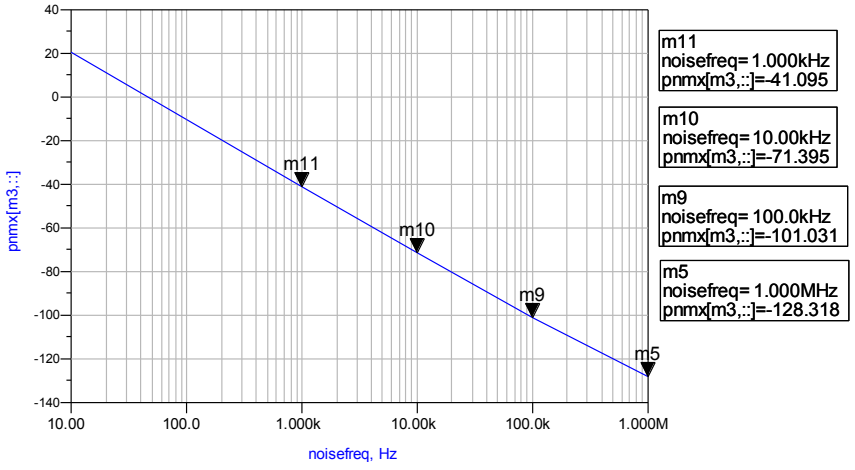


Figure 6.32 : Phase noise plot with inductive degeneration

While applying this method, impedance at common source node also increases and copying ratio of the biasing circuit approaches to ideal case which increases current drawn by the VCO core. This causes approximately 1 mW increase in power consumption. However, approximately 5 dB reduction in phase noise still improves FOM.

6.2.5 Differential Tuning

To decrease common mode noise further, differential tuning can be used. Calculations for differential tuning were done in phase noise reduction section. Width and length of all varactor transistors are tuned to 1.6 µm and 80 µm to adjust frequency band correctly. Differential voltage is adjusted in between -0.2 V and 0.8 V. Simulated differential varactor structure is shown in Fig. 6.32. In the simulations there seem to be no significant difference between standard and differential tuning cases. VCO gain stays nearly the same while phase noise is improved by 0.2 dB as illustrated in Fig. 6.33 and Fig. 6.34.

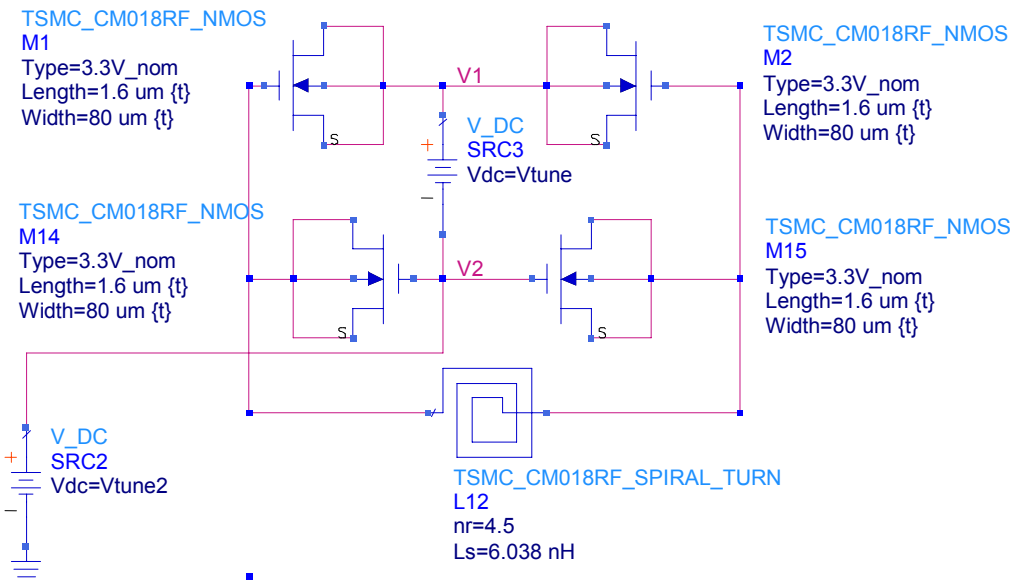


Figure 6.33: Resonator structure for differential tuning

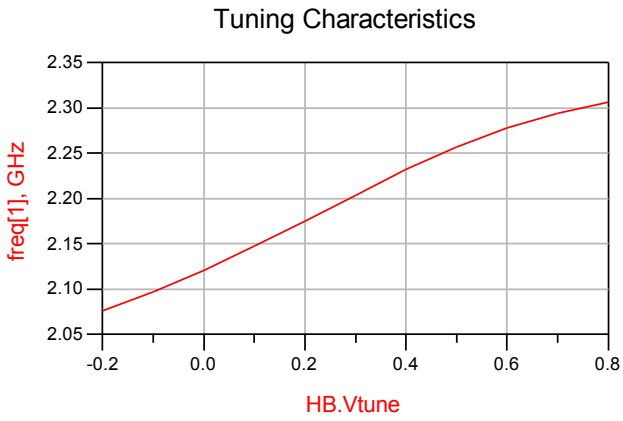


Figure 6.34 : Tuning characteristics with differential tuning

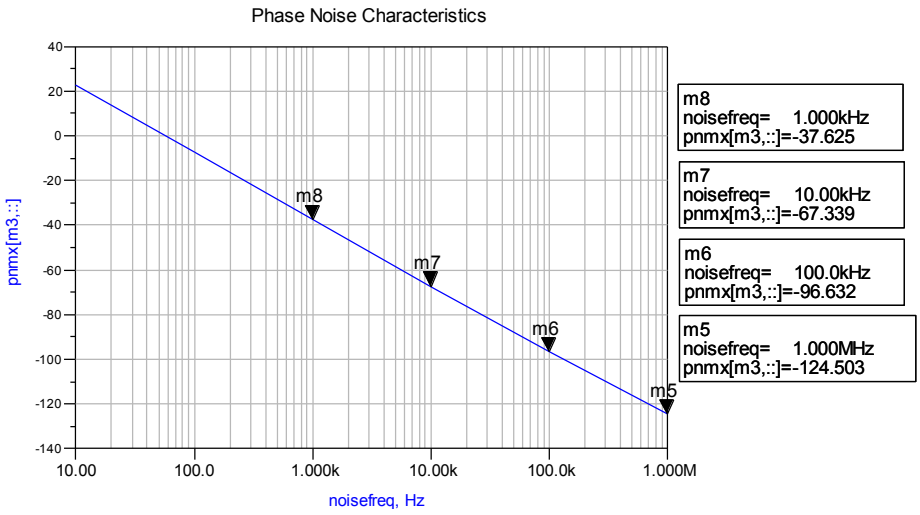


Figure 6.35 : Phase noise plot with differential tuning

6.2.6 Control Voltage Line Filtering

To filter the parasitic even harmonics created by the instantaneous imbalance in the circuit, an LC filter is inserted into circuit as shown in Fig. 6.35 and optimized for best phase noise performance. Even for the best case phase noise cannot be improved significantly. Results, shown in Fig. 6.36, show that there is no need for filtering control voltage line.

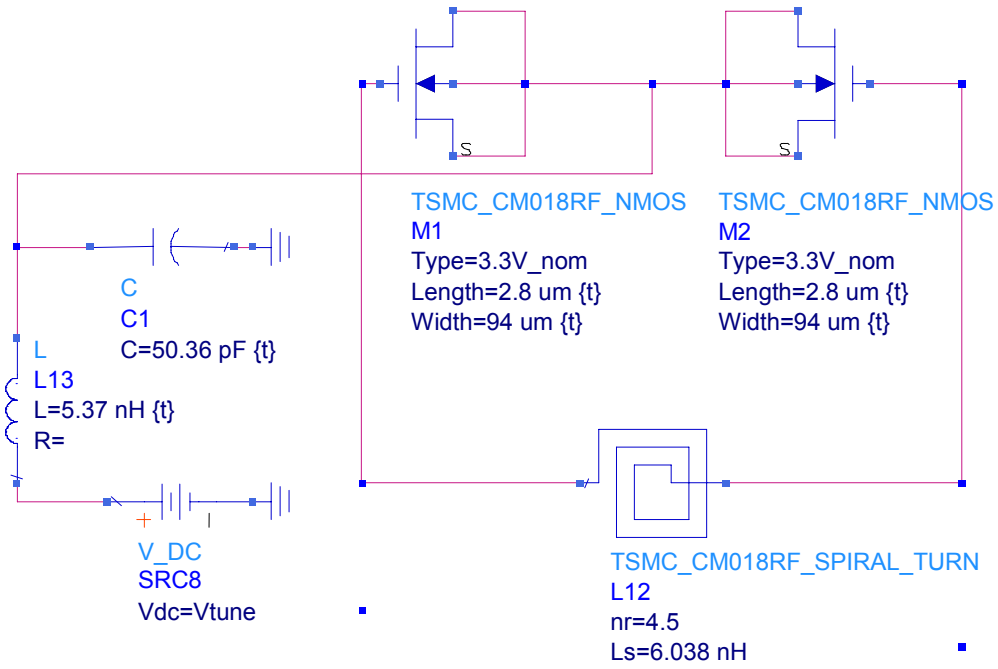


Figure 6.36 : Filtering control voltage line

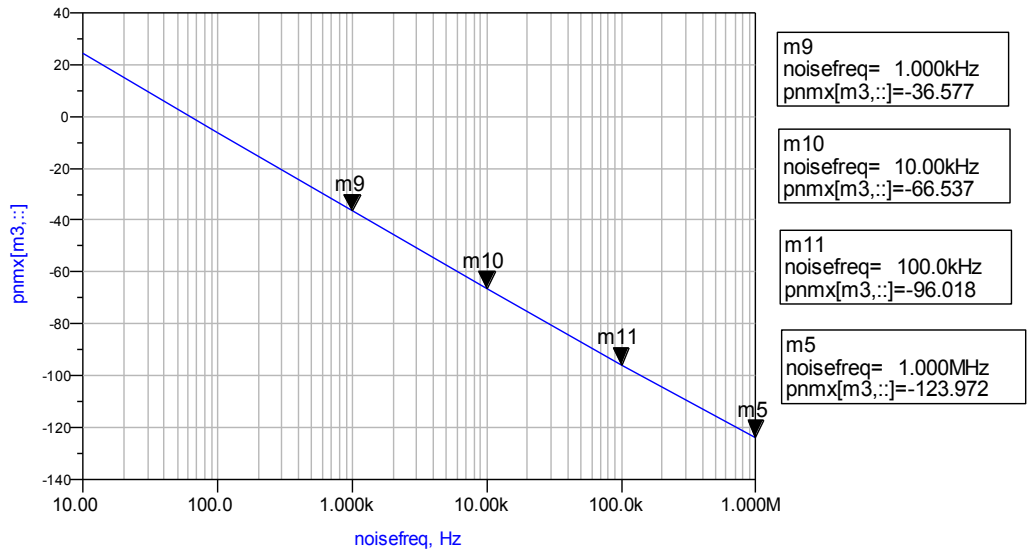


Figure 6.37 : Phase noise plot with control voltage line filtering

6.2.7 Summary and Design Finalization

Phase noise values at different offset frequencies for applied phase noise reduction techniques are summarized in Table 6.3 and Table 6.4. Among all methods, especially Reducing K_{VCO} and Resistor Tail Biasing provide best improvement. If tail biasing is used inductive degeneration and LC Filter can be used for better phase noise performance.

Table 6.3 : Simulated phase noise with applied methods

Method	**PN @ 1 kHz (dBc/Hz)**	**PN @ 10 kHz (dBc/Hz)**	**PN @ 100 kHz (dBc/Hz)**	**PN @ 1 MHz (dBc/Hz)**
No Method	-36.848	-66.525	-95.811	-123.793
Reducing K_{VCO}	-43.632	-74.357	-103.922	-129.296
Noise Filtering with Capacitance	-40.335	-71.674	-102.245	-127.934
LC Filter	-39.616	-69.902	-99.517	-126.749
No bias Circuit	-42.712	-73.681	-103.510	-128.871
Resistor Tail Biasing	-41.997	-73.076	-103.233	-129.273
Inductive Degeneration	-41.095	-71.395	-101.031	-128.318
Differential Tuning	-37.625	-67.339	-96.632	-124.503
Filtering Control Voltage	-36.575	-66.537	-96.018	-123.972

Table 6.4 : Phase noise improvement of applied methods

Method	**Imp. @ 1 kHz (dB)**	**Imp. @ 10 kHz (dB)**	**Imp. @ 100 kHz (dB)**	**Imp. @ 1 MHz (dB)**
Reducing K_{VCO}	6.784	7.832	8.111	5.503
Noise Filtering with Capacitance	3.487	5.149	6.434	4.141
LC Filter	2.768	3.377	3.706	2.956
No bias Circuit	5.864	7.156	7.699	5.078
Resistor Tail Biasing	5.149	6.551	7.422	5.48
Inductive Degeneration	4.247	4.87	5.22	4.525
Differential Tuning	0.777	0.814	0.821	0.71
Filtering Control Voltage	-0.273	0.012	0.207	0.179

After evaluation of the performance of phase noise reduction methods, VCO design is finalized with reducing VCO gain by using extra MIM capacitor. Also bias circuit is eliminated and resistor tail biasing is used. Finalized core design is shown in Fig. 6.38.

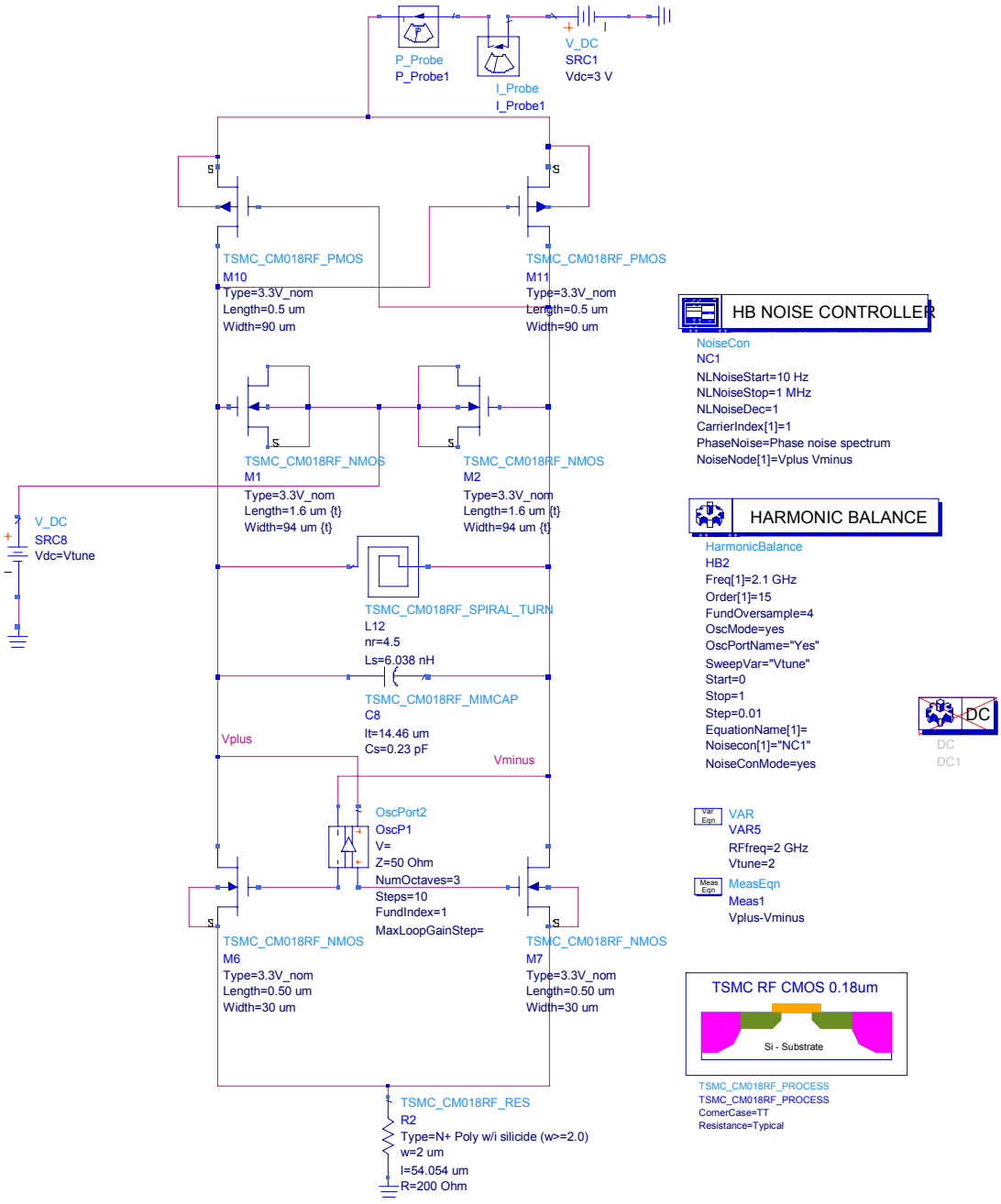


Figure 6.38 : Finalized VCO core design

Oscillator spectrum is shown in Fig. 6.39. As it was before even harmonics are suppressed due to differential topology. List of the harmonics is given in Table 6.5.

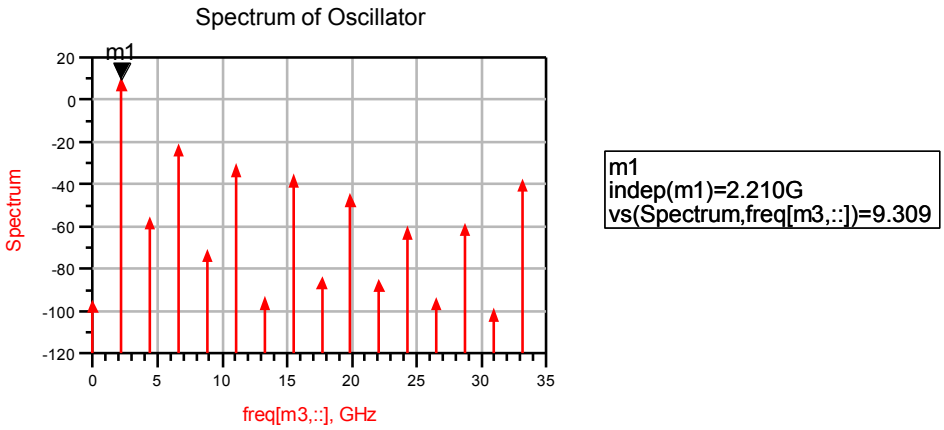


Figure 6.39 Spectrum of the finalized core

Table 6.5 : Spectrum of the finalized VCO tuned at 2210 MHz

Frequency (GHz)	**Power (dBm)**
2.21	9.309
4.42	-56.36
6.63	-21.89
8.84	-71.73
11.05	-31.41
13.26	-94.12
15.47	-36.30
17.68	-84.46
19.89	-45.47
22.10	-85.75

Finalized oscillator can be tuned from 2.15 GHz to 2.25 GHz corresponding to 100 MHz/V tuning gain as illustrated in Fig. 6.40. Oscillation in time domain is shown in Fig. 6.41.

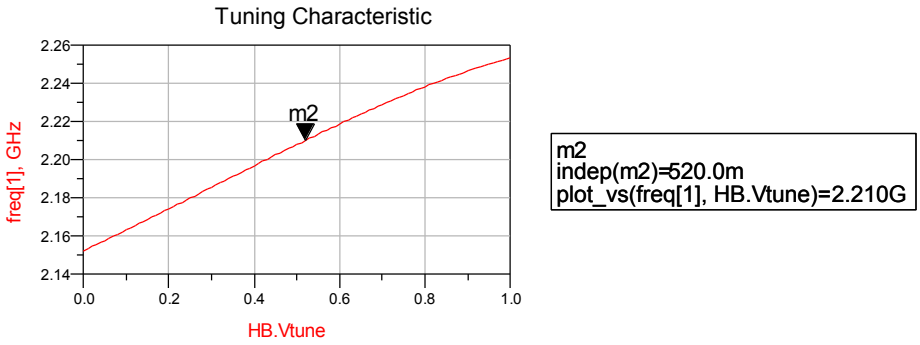


Figure 6.40 : Tuning characteristic of finalized core

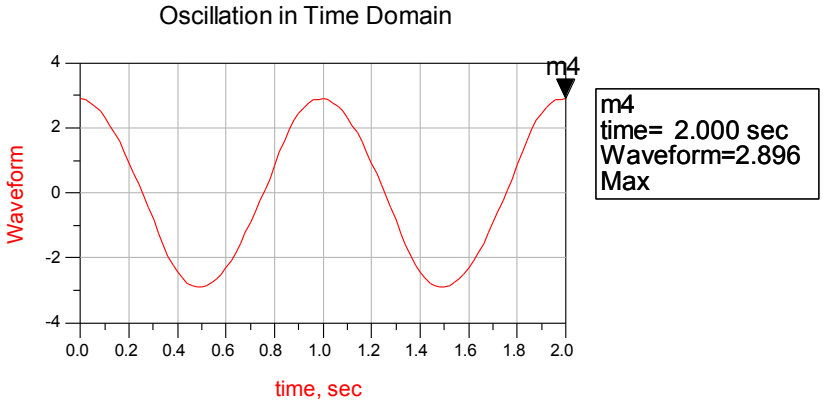


Figure 6.41 : Time domain output signal of finalized core

Phase noise plot for tuning voltage adjusted to 520 mV which corresponds to 2.21 GHz oscillation is given in Fig. 6.42.

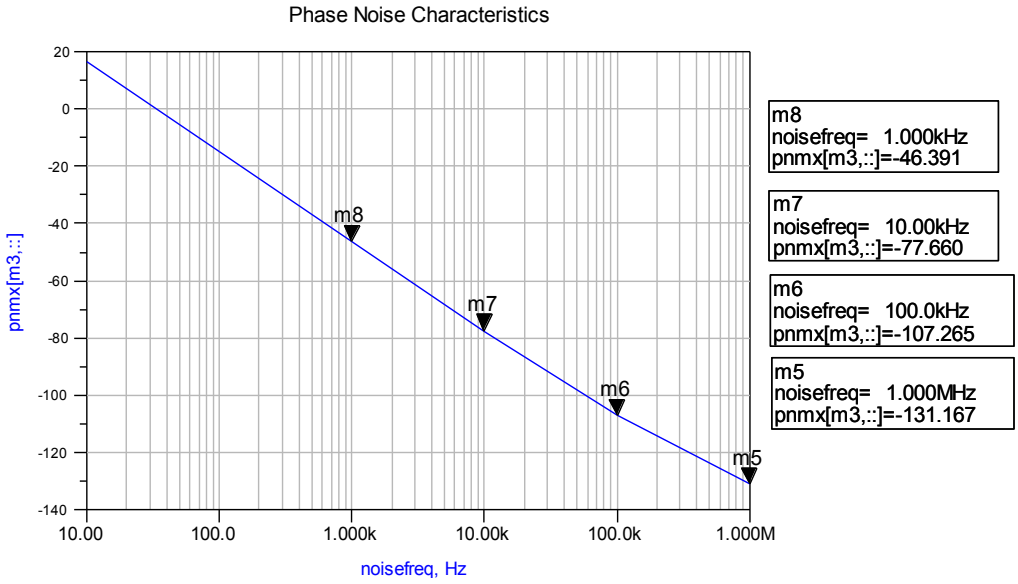


Figure 6.42 : Phase noise plot of finalized core

With 7.5 mW power consumption, at 100 kHz offset FOM is calculated as -185.4 and at 1 MHz offset -189.3. Measured FOM shows that performance of the designed VCO is better than other similar designs as illustrated in Table 6.6. Note that tuning ranges of the VCOs are not taken into account in FOM calculation, therefore they are not included in this comparison table.

Table 6.6 : VCO performance comparison

Reference	[61]	[25]	[62]	This work
	0.18 µm CMOS	0.18 µm CMOS	0.18µm CMOS	0.18µm CMOS
Implementation Status	Not Implemented	Not Implemented	Not Implemented	Not Implemented
f_0	2 GHz	2.03 GHz	2.4 GHz	2.21 GHz
Δf	100 kHz	100 kHz	100 kHz	100 kHz
$P(mW)$	10 mW	5.4 mW	1.8 mW	7.5 mW
$PN(\Delta f)$	-95.2	-102.6	-100.2	-107.265
FOM	-171.22	-180.8	-185.2	-185.4

CHAPTER 7

CONCLUSION

Phase noise is the most important parameter of oscillators used in communication systems. Phase noise may have destructive effects especially in modern wireless communication systems where channel spacings are very narrow. In these systems, generally, to make oscillator independent of environmental conditions and to prevent phase and frequency shifting as much as possible PLL based local oscillators are used. For low phase noise PLL based local oscillator design, there are different techniques. First, since phase noise increases by $20 \log (N)$ with increasing division rate, value of N divider should be decreased. For this purpose fractional-N structures, in which fractional division rates are allowed, are used. Thus value of N can be decreased and PFD frequency can be selected higher without changing channel spacing. Second, if there is no mismatch in between voltage range of VCO and charge pump output, using active loop filters should be avoided to not to add noise of active devices to the system. Also keeping in mind that loop filter shapes the phase noise characteristic of the PLL, bandwidth and order should be selected carefully. Note that since bandwidth and switching speed are inversely proportional, although spurs are attenuated better decrease in the bandwidth causes system to lock in a longer period. Thirdly to increase SNR, charge pump current should be selected as high as possible. Fourth, since phase noise of the system follows phase noise of VCO above certain frequency, using low noise VCO is important.

In this thesis work, first a PLL based local oscillator is designed and prototype is implemented to operate at 2.21 GHz. This oscillator is planned to be used as IF oscillator in an X-Band communication system. In the design, discrete commercial components are used. Operational settings are done taking low noise techniques into consideration and filter is optimized in the simulation in terms of phase noise, spurious response and lock time. Since lock time is not so critical for this application, it is allowed to be approximately 2.8 msec. Measured phase noise values are -84.6 dBc/Hz at 10 kHz, -123.2 dBc/Hz at 100 kHz and less than -141.3 dBc/Hz at 1 MHz offsets.

Although measured values are considerably good when compared to commercial products, potential problems, caused by the implementation, that deteriorate phase noise performance are also considered. Considering the fact that prototype system is implemented on FR4 material having a high dielectric constant which adds to the phase noise, using a less lossy material will improve phase noise. Moreover hole plating is not performed in prototype PCB. This may cause bad grounding and contributes to the noise. Another potential problem is long tuning voltage path and poor screening. Although loop filter is placed near to the VCO, this long path causes undesired couplings that modulate VCO. This path should be made shorter.

Second work in this thesis is the design of a low phase noise CMOS VCO which is to be used in integrated communication systems. In RF systems, LC oscillators, especially differential ones are widely used due to their satisfactory phase noise performance. By its nature in differential oscillators common mode noise is eliminated which means an improvement on the phase noise performance. Another improvement in differential structures is the elimination of even harmonics. If fully differential topology is preferred improvement is more drastic. Apart from topology selection, phase noise generation mechanisms and some common phase noise reduction techniques derived so far depending on common phase noise models namely Leeson's model, LTV model and NTI model are investigated. Increasing amplitude of oscillation, improving Q-factor of resonator and reducing VCO gain are basic methods of improving phase noise. There are also some circuit techniques which can be listed as noise filtering, elimination of bias circuit, resistor biasing, discrete frequency tuning, inductive degeneration, voltage line filtering and differential tuning. Together with advantages, these techniques have some certain disadvantages. Therefore effects may not always be positive. For this reason methods should carefully be applied and effects should be observed in simulations.

Forming the background information, using CAD tool ADS 2008, a low phase noise CMOS cross-coupled differential VCO operating in between 2.15 GHz and 2.25 GHz is designed with TSMC 0.18 μm technology to be used in single chip transmitters, receivers and transceivers which are planned to be parts of future work. In oscillator design, since there is a strong interaction between design components it is more logical to make design considering the system as a whole. In this work, although active circuit and resonator are designed and simulated separately, they are finalized in the system simulations. In this core design, in order to reduce phase noise VCO gain is reduced, transistor sizes are optimized and oscillation amplitude is increased as much as possible. Although obtained phase noise

values are quite good, it is attempted to reduce these values further by applying known circuit techniques. These techniques are simulated and the design is finalized by eliminating bias circuit and applying resistor biasing. Since bias circuit is eliminated there is no need for tail noise filtering. Also VCO gain is reduced further by inserting constant capacitor to the structure. Having -107.265 dBc/Hz and -131.167 dBc/Hz phase noise at 100 kHz and 1 MHz offset from carrier at 2.21 GHz and FOM of -185.4 at 100 kHz offset, resultant VCO core is quite good when compared to similar works. As stated before this structure is planned to be used in an integrated communication system which is to be our future work.

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APPENDIX A

THIRD ORDER LOOP FILTER DESIGN [6]

Impedance of a third order loop filter given in Fig. 2.7(b) can be written as

$$Z(s) = \frac{1 + sT_2}{s(C_1 + C_2 + C_3)(1 + sT_1)(1 + sT_3)} \tag{A.1}$$

where time constants are approximated as :

$$T_2 = R_2 C_2 \tag{A.2}$$

$$T_1 \approx \frac{C_1 C_2 R_2}{(C_1 + C_2 + C_3)} \tag{A.3}$$

$$T_3 \approx R_3 C_3 \tag{A.4}$$

This expression can be written in a more compact form as:

$$Z(s) = \frac{1 + sC_2 R_2}{s(A_2 s^2 + A_1 s + A_0)} \tag{A.5}$$

where the coefficients can be written in terms of component values as:

$$A_2 = A_0 T_1 T_3 = C_1 C_2 R_2 C_3 R_3 \tag{A.6}$$

$$A_1 = A_0(T_1 + T_3) = C_2 C_3 R_2 + C_1 C_2 R_2 + C_1 C_3 R_3 + C_2 C_3 R_3 \tag{A.7}$$

$$A_0 = C_1 + C_2 + C_3 \tag{A.8}$$

Writing the expression of phase margin and equating the derivative of it to zero at the loop bandwidth, T_2 is written in terms of other time constants as given in (A.11) where T_{31} is the ratio of pole 3 to pole 1 which can be chosen from zero to one and γ is the optimization parameter.

$$\phi = 180^0 + tan^{-1}(\omega_c T_2) - tan^{-1}(\omega_c T_1) - tan^{-1}(\omega_c T_3) \tag{A.9}$$

$$T_3 = T_1 T_{31} \tag{A.10}$$

$$T_2 = \frac{\gamma}{\omega_c^2 T_1 (1 + T_{31})} \qquad (A.11)$$

Substituting (A.11) into (A.10), T_1 is approximately calculated as (A.12).

$$T_1 \approx \frac{\sec(\phi) - \tan(\phi)}{\omega_c (1 + T_{31})} \qquad (A.12)$$

Knowing T_1 , T_2 and T_3 can easily be calculated from (A.10) and (A.12). Next is to calculate loop filter coefficients. Total capacitance A_0 is calculated as in (A.13). The other coefficients A_1 and A_2 can be calculated from (A.14) and (A.15).

$$A_0 = \frac{K_{cp} K_{VCO}}{\omega_c^2 N} \sqrt{\frac{1 + \omega_c^2 T_2^2}{(1 + \omega_c^2 T_1^2)(1 + \omega_c^2 T_3^3)}} \qquad (A.13)$$

Loop filter coefficients enable us to find component values. From the possible set of solutions optimum one should be selected. In practice control voltage inputs of the VCOs have certain capacitances. For a healthy design this capacitance should also be considered in the filter design. To make filter independent from this capacitance as much as possible C_3 value should be set to maximum. Therefore firstly C_1 value that maximizes C_3 should be found. Maximizing C_3 also means minimum R_3. Therefore thermal noise contribution of this resistor is also minimized which helps reduction of the phase noise.

Filter coefficient A_1 can be expressed in terms of C_1 and C_3 as:

$$A_1 = T_2 C_1 - \frac{A_2 A_0}{T_2 C_1} - \frac{A_2 C_3}{T_2 C_1} \qquad (A.14)$$

From the expression of A_1, C_3 can be expressed in terms of C_1 as:

$$C_3 = \frac{-T_2^2 C_1^2 + T_2 A_1 C_1 - A_2 A_0}{T_2^2 C_1 - A_2} \qquad (A.15)$$

Taking the derivative of C_3 with respect to C_1 and equating it zero we can find the critical points. These critical points may belong to local minimums or local maximums. To understand whether the solution is a maximum or a minimum second derivative is found. C_1 value that makes second derivative negative indicates local maximum. Therefore this value is selected to be optimum value for C_1 expression of which is given as:

$$C_1 = \frac{A_2}{T_2^2}\left(1 + \sqrt{1 + \frac{T_2}{A_2}(T_2 A_0 - A_1)}\right) \qquad (A.16)$$

After finding optimum C_1, other filter components can easily be written as:

$$C_3 = \frac{-T_2^2 C_1^2 + T_2 A_1 C_1 - A_2 A_0}{T_2^2 C_1 - A_2} \qquad (A.17)$$

$$C_2 = A_0 - C_1 - C_3 \qquad (A.18)$$

$$R_2 = \frac{T_2}{C_2} \qquad (A.19)$$

$$R_3 = \frac{A_2}{C_1 C_3 T_2} \qquad (A.20)$$

Filter Optimization

In filter design, there are two optimization parameters namely pole ratio T_{31} and γ. Effects of these parameters are analyzed by considering spur gain. Spur gain is defined as the noise induced at the VCO resulted from single frequency noise injection to loop filter. Spur gain is inversely proportional to ***r*** which is defined as f_{spur}/f_c [6].

To maximize ***r***, T_{31} should be selected close to one. On the other hand value of the capacitor next to VCO decreases with increasing T_{31}. As stated before to reduce the effect of capacitance of control voltage input of VCO , capacitor next to it is desired to be maximized. Therefore pole ratio should not exceed a certain value. This parameter should be optimized by considering capacitance of the VCO.

Other parameter γ is related with phase margin at loop bandwidth and maximized when it is equal to unity and in most designs it is selected to be unity. Together with the phase margin this parameter controls lock time. Lock time decreases with increasing phase margin and decreasing γ. In applications where lock time is not critical phase margin can be reduced and γ can be increased.

MATLAB Script

```
%%%%%%% PLL Parameters %%%%%%%

Kvco=60e6;
Kpd=5e-3;
Fref=20e6;
RFout=2210e6;

fc=50e3; %loop BW
phasemargin=pi/(180/45);
gamma=1.2; %optimization parameter
T31=0.5;

N=RFout/Fref;

%%%%%% Time Constants %%%%%%

wc=2*pi*fc;
T1= (sec(phasemargin)-tan(phasemargin))/(wc*(1+T31));
T3=T1*T31;
T2=gamma/((wc^2)*(T1+T3));

%%%%%% Filter Coefficients %%%%%%
A0=((Kpd*Kvco)/(N*wc^2))*sqrt((1+wc^2*T2^2)/((1+wc^2*T1^2)*(1+wc^2*T
3^2)));
A1=A0*(T1+T3);
A2=A0*T1*T3;

%%%%%% Component Values %%%%%%
C1=(A2/(T2^2))*(1+sqrt(1+(T2/A2)*T2*A0-A1))
C3=(-T2^2*C1^2+T2*A1*C1-A2*A0)/((T2^2)*C1-A2)
C2=A0-C1-C3
R2=T2/C2
R3=A2/(C1*C3*T2)
```

APPENDIX B

TYPICAL ELECTRICAL SPECIFICATIONS OF VOLTAGE CONTROLLED OSCILLATOR UMX-269-D16

Frequency Tuning Range (MHz)	2070 - 2270
Power Output(dBm)	5
Harmonics(dBc)	-12 (Max)
Frequency Pushing(MHz/V)	1.5
Frequency Pulling(MHz p-p at 12 dBr)	0.6
Tuning Port Capacitance(pF)	47
Supply Voltage (V)	5
Supply Current(mA)	26
3 dB Modulation Bandwidth (MHz)	1
Frequency Sensitivity (MHz/V)	60
Phase Noise (dBc/Hz)	
1 kHz	*-80*
10 kHz	*-106*
100 kHz	*-127*
1 MHz	*-147*
10 MHz	*-160*

APPENDIX C

PHASE NOISE SIMULATON RESULTS FOR DIFFERENT LOOP BANDWIDTHS

5 kHz at 45^0phase margin

Freq	Total	VCO	Ref	Chip	Filter
100	-68.10	-125.1	-68.10	-99.11	-129.0
200	-72.58	-119.0	-72.59	-99.08	-123.0
500	-78.33	-111.2	-78.37	-98.89	-115.1
1.00k	-82.17	-105.4	-82.31	-98.32	-109.4
2.00k	-85.04	-100.4	-85.52	-97.02	-104.4
5.00k	-89.25	-97.66	-91.27	-96.80	-102.0
10.0k	-97.91	-102.8	-102.8	-103.8	-108.3
20.0k	-108.2	-110.8	-115.8	-115.3	-118.7
50.0k	-119.3	-119.8	-135.8	-133.3	-132.6
100k	-125.9	-126.0	-153.2	-149.2	-143.5
200k	-132.0	-132.0	-170.5	-166.5	-155.1
500k	-139.9	-139.9	-194.2	-190.2	-170.9
1.00M	-145.8	-145.8	-212.2	-208.2	-182.9

10 kHz at 45^0phase margin

Freq	Total	VCO	Ref	Chip	Filter
100	-68.11	-137.1	-68.11	-99.12	-138.0
200	-72.61	-131.1	-72.62	-99.11	-132.0
500	-78.50	-123.1	-78.54	-99.06	-124.1
1.00k	-82.77	-117.2	-82.88	-98.89	-118.1
2.00k	-86.50	-111.4	-86.83	-98.32	-112.4
5.00k	-89.72	-105.1	-91.02	-96.55	-106.2
10.0k	-92.62	-103.7	-95.79	-96.80	-105.1
20.0k	-100.0	-108.9	-104.3	-103.8	-111.3
50.0k	-114.8	-119.2	-121.9	-119.4	-125.1
100k	-124.5	-125.9	-137.3	-133.3	-135.6
200k	-131.7	-132.0	-153.2	-149.2	-146.5
500k	-139.9	-139.9	-176.2	-172.3	-161.9
1.00M	-145.8	-145.8	-194.2	-190.2	-173.9

20 kHz at 45^{0}phase margin

Freq	Total	VCO	Ref	Chip	Filter
100	-68.11	-149.1	-68.11	-99.12	-147.1
200	-72.62	-143.1	-72.63	-99.12	-141.0
500	-78.54	-135.2	-78.58	-99.11	-133.1
1.00k	-82.94	-129.2	-83.05	-99.06	-127.1
2.00k	-87.10	-123.2	-87.40	-98.89	-121.1
5.00k	-91.34	-115.7	-92.45	-97.98	-113.7
10.0k	-92.83	-111.1	-95.54	-96.55	-109.2
20.0k	-93.75	-109.7	-97.29	-96.80	-108.1
50.0k	-104.8	-117.4	-109.7	-107.2	-117.5
100k	-116.9	-125.2	-123.4	-119.4	-128.1
200k	-128.4	-131.9	-137.3	-133.3	-138.6
500k	-139.5	-139.9	-158.7	-154.7	-153.2
1.00M	-145.8	-145.8	-176.2	-172.3	-164.9

30 kHz at 45^{0}phase margin

Phase Noise Table

Freq	Total	VCO	Ref	Chip	Filter
100	-68.11	-156.2	-68.11	-99.12	-152.3
200	-72.62	-150.2	-72.63	-99.12	-146.3
500	-78.55	-142.2	-78.59	-99.12	-138.4
1.00k	-82.98	-136.2	-83.09	-99.10	-132.3
2.00k	-87.22	-130.2	-87.52	-99.02	-126.4
5.00k	-91.92	-122.5	-93.01	-98.53	-118.6
10.0k	-93.80	-117.1	-96.41	-97.42	-113.3
20.0k	-93.25	-113.5	-96.65	-96.16	-109.8
50.0k	-99.07	-116.5	-103.7	-101.3	-113.8
100k	-110.2	-124.3	-116.1	-112.1	-123.7
200k	-122.6	-131.6	-128.9	-125.0	-134.3
500k	-137.9	-139.9	-148.9	-144.9	-148.4
1.00M	-145.5	-145.8	-165.9	-161.9	-159.8

40 kHz at 45^{0}phase margin

Freq	Total	VCO	Ref	Chip	Filter
100	-68.11	-161.2	-68.11	-99.12	-156.1
200	-72.62	-155.2	-72.63	-99.12	-150.1
500	-78.55	-147.2	-78.59	-99.12	-142.1
1.00k	-82.99	-141.2	-83.10	-99.11	-136.1
2.00k	-87.27	-135.2	-87.57	-99.06	-130.1
5.00k	-92.17	-127.3	-93.25	-98.77	-122.3
10.0k	-94.40	-121.7	-96.97	-97.98	-116.7
20.0k	-93.70	-117.2	-97.04	-96.55	-112.2
50.0k	-96.11	-116.6	-100.7	-98.20	-112.2
100k	-105.6	-123.5	-111.2	-107.2	-120.5
200k	-117.6	-131.2	-123.4	-119.4	-131.1
500k	-134.6	-139.9	-142.2	-138.2	-145.1
1.00M	-144.8	-145.8	-158.7	-154.7	-156.2

50 kHz at 45^0phase margin

Freq	Total	VCO	Ref	Chip	Filter
100	-68.11	-165.1	-68.11	-99.12	-159.0
200	-72.62	-159.0	-72.63	-99.12	-153.0
500	-78.56	-151.1	-78.59	-99.12	-145.0
1.00k	-82.99	-145.1	-83.10	-99.11	-139.0
2.00k	-87.29	-139.0	-87.59	-99.08	-133.0
5.00k	-92.29	-131.2	-93.37	-98.89	-125.1
10.0k	-94.76	-125.4	-97.31	-98.32	-119.4
20.0k	-94.20	-120.4	-97.51	-97.02	-114.4
50.0k	-94.75	-117.7	-99.28	-96.80	-112.0
100k	-102.2	-122.8	-107.8	-103.8	-118.3
200k	-113.6	-130.8	-119.3	-115.3	-128.7
500k	-130.9	-139.8	-137.3	-133.3	-142.6
1.00M	-143.2	-145.8	-153.2	-149.2	-153.5

APPENDIX D

MICROCONTROLLER CODE FOR PROGRAMMING FREQUENCY SYNTHESIZER ADF4157

```
/*
-----------------
Digital PLL ADF4157
------------------
*/
#include   <pic.h>
#include   <stdio.h>
#include   <math.h>
#include   <stdlib.h>

long int i,j;
int x,a;

/********** SPI Write Function *********/
void SPII(a)
{
  SSPBUF = a;
  for(j=0;j<10;j++);
}

/********* Load Enable Function ********/
void LE() {

PORTC = 0x02;
for(j=0;j<10;j++);
PORTC = 0x00;


}

void main()      {
#define FOSC (2000000L)

TRISC=0b00000000;
TRISB=0b00000010;
ADCON1=0x0F;
SSPSTAT=0b00000000;
SSPCON=0b00110000;

//for(j=0;j<10;j++)
PORTC = 0x00;
```

```
while(1)
{
        if( (PORTB&0x02)==0 )
        {
                /*******REG4********/

                x=0b00000001;
                SPII(x);
                x=0b10000000;
                SPII(x);
                x=0b00000000;
                SPII(x);
                x=0b00000100;
                SPII(x);
                LE();

PORTC=0b00000001;
PORTC=0b00000000;

                //REG 3

x=0b00000000;
                SPII(x);
                SPII(x);
                SPII(x);
                x=0b11000011;
                SPII(x);
                LE();

                PORTC=0b00000100;
PORTC=0b00000000;

                //REG2
                 x=0b00000111;
                 SPII(x);
                 x=0b10010000;
                 SPII(x);
                 x=0b10000000;
                 SPII(x);
                 x=0b00000010;
                 SPII(x);
                 LE();

                PORTC=0b00010000;
PORTC=0b00000000;

//REG1
                x=0b00000000;
                SPII(x);
                SPII(x);
                SPII(x);
                x=0b00000001;
                SPII(x);
```

```
                    LE();

                    PORTC=0b01000000;
PORTC=0b00000000;

                    //REG0
                     x=0b00011000;
                     SPII(x);
                     x=0b00110111;
                     SPII(x);
                     x=0b01000000;
                     SPII(x);
                     x=0b00000000;
                     SPII(x);
                     LE();


                    for(i=0;i<250;i++);
                    for(i=0;i<250;i++);
                    for(i=0;i<250;i++);
                    for(i=0;i<250;i++);
                    for(i=0;i<250;i++);
                    for(i=0;i<250;i++);
                    for(i=0;i<250;i++);
          }


}
```