DESIGN, IMPLEMENTATION, AND CONTROL OF A TWO–STAGE AC/DC ISOLATED POWER SUPPLY WITH HIGH INPUT POWER FACTOR AND HIGH EFFICIENCY

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
MIDDLE EAST TECHNICAL UNIVERSITY

BY

MEHMET CAN KAYA

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF MASTER OF SCIENCE
IN
ELECTRICAL AND ELECTRONICS ENGINEERING

SEPTEMBER 2008

Approval of the thesis:

DESIGN, IMPLEMENTATION, AND CONTROL OF A TWO–STAGE AC/DC ISOLATED POWER SUPPLY WITH HIGH INPUT POWER FACTOR AND HIGH EFFICIENCY

submitted by **MEHMET CAN KAYA** in partial fulfillment of the requirements for the degree of **Master of Science in Electrical and Electronics Engineering Department, Middle East Technical University** by,

Prof. Dr. Canan Özgen _____
Dean, Graduate School of **Natural and Applied Sciences**

Prof. Dr. İsmet Erkmen _____
Head of Department, **Electrical and Electronics Engineering**

Assist. Prof. Dr. Ahmet M. Hava _____
Supervisor, **Electrical and Electronics Engineering Dept., METU**

Examining Committee Members:

Prof. Dr. Aydın Ersak _____
Electrical and Electronics Engineering Dept., METU

Assist. Prof. Dr. Ahmet M. Hava _____
Electrical and Electronics Engineering Dept., METU

Prof. Dr. Kemal Leblebicioğlu _____
Electrical and Electronics Engineering Dept., METU

Prof. Dr. Nevzat Özay _____
Electrical and Electronics Engineering Dept., METU

Dr. Erbil Nalçacı _____
EPDK

Date: 02/09/2008

I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

Name, Last name : Mehmet Can Kaya

Signature :

DESIGN, IMPLEMENTATION, AND CONTROL OF A TWO–STAGE AC/DC ISOLATED POWER SUPPLY WITH HIGH INPUT POWER FACTOR AND HIGH EFFICIENCY

Kaya, Mehmet Can
M.S., Department of Electrical and Electronics Engineering
Supervisor: Assist. Prof. Dr. Ahmet M. Hava

September 2008, 154 pages

In this thesis a two-stage AC/DC/DC power converter is designed and implemented. The AC/DC input stage of the converter consists of the two–phase interleaved boost topology employing the average current mode control principle. The output stage consists of a zero voltage switching phase shifted full bridge (ZVS–PS–FB) DC/DC converter. For the input stage, main design goals are obtaining high input power factor, low input current distortion, and well regulated output dc voltage, and obtaining these attributes in a power converter with high power density. For the input stage, the interleaved structure has been chosen in order to obtain reduced line current ripple and EMI, reduced power component stresses, and improved power density. The control of the pre–regulator is provided by utilizing a new commercial monolithic integrated circuit, which provides interleaved continuous conduction mode power factor correction (PFC). The output stage is formed by utilizing the available prototype hardware of a ZVS–PS–FB DC/DC converter and mainly the system integration and controller design and implementation studies have been conducted. The converter small signal model is derived and utilizing its transfer function and employing voltage loop control, the output voltage regulator has been designed. The output voltage controller is implemented utilizing a digital signal

processor (DSP). Integrating the AC/DC preregulator and DC/DC converter, a laboratory AC/DC/DC converter system with high overall performance has been obtained. The overall system performance has been verified via computer simulations and experimental results obtained from laboratory prototype.

Keywords: Power factor correction, interleaving, average current mode control, full bridge DC/DC converter, phase shifted PWM, zero voltage switching, transformer saturation.

YÜKSEK VERİMLİLİKTE ÇALIŞAN YÜKSEK GİRİŞ GÜÇ ÇARPANLI, İKİ KATLI, İZOLASYONLU AA/DA GÜÇ KAYNAĞININ TASARIM, DENETİM VE İMALATI

Kaya, Mehmet Can
Yüksek Lisans, Elektrik ve Elektronik Mühendisliği Bölümü
Tez Yöneticisi: Yrd. Doç. Dr. Ahmet M. Hava

Eylül 2008, 154 sayfa

Bu tezde iki aşamalı bir AA/DA/DA güç çeviricisi tasarlanmış ve üretilmiştir. Güç çeviricisinin AA/DA giriş katı iki fazlı sarmaşık yapılı yükseltici topolojisi ile inşa edilmiş ve ortalama akım denetleme yöntemi uygulanmıştır. Çıkış katı ise sıfır gerilimde anahtarlama yapan faz kaymalı tam köprü DA/DA güç çeviricisinden oluşmaktadır. Giriş katının tasarım hedefleri yüksek güç yoğunluğunda yüksek giriş güç çarpanı, düşük giriş akımı bozunumu ve yüksek çıkış gerilimi kararlılığı sağlamaktır. Giriş katı tasarımında, düşük giriş akım dalgacıklanması ve elektromanyetik girişim elde etmek, güç devresi bileşenleri üzerindeki zorlamaları azaltmak ve daha yüksek güç yoğunluğu elde etmek için sarmaşık yapısı kullanılmıştır. Giriş katının denetimi, sürekli akım iletim kipinde sarmaşık yapıda güç çarpanı doğrultucusu denetimi yapabilen ve piyasaya yeni sürülmüş ticari bir tümleşik devre ile sağlanmaktadır. Çıkış katı, kullanıma hazır bulunan sıfır gerilimde anahtarlama yapan faz kaymalı tam köprü DA/DA çeviricinin ilkörnek donanımı kullanılarak oluşturulmuştur. Sistem birleştirimi, denetleyici tasarımı ve uygulaması bu donanım üzerinden yürütülmüştür. Çıkış geriliminin denetlenmesi amacıyla çeviricinin küçük işaret modeli türetilmiş ve model, gerilim döngüsü denetiminin tasarımında kullanılmıştır. Çıkış gerilim denetimi, denetleme algoritmasının içine

gömüldüğü bir sayısal işaret işleyicisi üzerinden sağlanmaktadır. AA/DA/DA laboratuvar ilkörneğinin yüksek çalışma başarımı, AA/DA çevirici giriş katı ve DA/DA çevirici çıkış katının birleştirilip beraber çalıştırılmasıyla gözlemlenmiştir. Tüm sistemin başarımı bilgisayar bemzetim ve laboratuvar deney sonuçlarıyla doğrulanmıştır.

Anahtar Kelimeler: Güç çarpanı düzeltimi, sarmaşık yapı, ortalama akım denetimi, tam köprü DA/DA çevirici, faz kaydırmalı DGM, sıfır gerilimde anahtarlama, trafo doyumu.

To my family,

Gülhan Ersoy,

Aydan Kaya,

Ali Vehbi Kaya,

and

to my love,

Gizem Çorakbaş

for their support and kindness

ACKNOWLEDGMENTS

I express my sincerest thanks to my supervisor, Dr. Ahmet M. Hava, for his guidance, support, encouragement, and valuable contributions throughout my graduate education, and his advices about the life.

I would like to express my deepest gratitude to my family for their support and love.

I am grateful to my research groupmates Ömer Göksu, Eyyüp Demirkutlu, Emre Ün, Osman Selçuk Şentürk, Hasan Özkaya, Süleyman Çetinkaya, and Kerem Baykent for their help, support, and mainly friendship. I specially thank to Mutlu Uslu for his excellent thesis study which has enlightened my way. I would also like to thank Erdal Bizkevelci for his friendship in long laboratory nights.

I would like to express my gratitude to my colleagues and managers at ASELSAN Inc. for their understanding, help, and support.

I would like to extend my special appreciation to my love Gizem Çorakbaş for her support, patience, and kindness throughout my graduate study.

I wish to thank the Department of Electrical and Electronics Engineering faculty and staff and Graduate School of Natural and Applied Sciences for their help throughout my graduate study.

TABLE OF CONTENTS

LIST OF FIGURES

FIGURES

LIST OF TABLES

CHAPTER 1

INTRODUCTION

1.1 General

The electrical energy available in the utility grid is not suitable for direct use in many applications. In particular, applications requiring DC voltage/current source must involve an interface device between the AC power line and the load requiring the DC voltage. For such applications, AC/DC switch–mode power converters are the modern choice.

Conventional AC/DC conversion involves diode or thyristor rectifiers. In both rectifiers the line current is highly distorted. The thyristor rectifier also draws fundamental component reactive power. Harmonic components injected to the power line result in many unfavorable effects for electricity consumers. They overheat transformer windings and cause malfuncting in the electrical devices connected to the grid. Another drawback of these old technology AC/DC conversion devices and methods is that the output DC voltage is less than the AC line voltage peak (determined by the rectifier average output voltage equation). Therefore, the output voltage significantly decreases with increased loading and the DC bus voltage cannot be kept regulated. With the main advantages being low cost, these topologies are no more favorable as the power line pollution due to harmonics has reached a critical level where the power line utility imposes rules on the customers. Therefore, the input power quality of the AC/DC first stage is critical in most power converters, in particular for converters involving power ratings surpassing kilowatts. Further, the DC load power quality requirements have also become stringent. In many

applications constant DC bus voltage is favorable as the load performance can be easier maintained with the fixed bus rather than load dependent and decreasing DC bus voltage cases.

Modern AC/DC switch–mode converters involve at least two cascaded stages. The first stage is the AC/DC conversion stage that interfaces the utility grid voltage with a compatible level DC voltage. The second stage is a DC/DC converter stage that conditions the first DC voltage stage such that the performance requirements of the load are satisfied. For example in a telecom power supply, the load requires DC voltage at 48 V level and the power rating is in the range of kilowatts. Supplying the telecom equipment from the 50 Hz, 220 Vrms single phase AC line through an AC/DC power converter involves the following switch–mode power converter technology. The first stage, which is called the input stage, utilizes a power factor correcting AC/DC boost rectifier. With this topology the input current becomes sinusoidal and the AC line voltage is converted to an intermediate DC voltage such that it has a DC value compatible with the line voltage. For the 220 Vrms case, this value is typically 400 V. The 400 V DC voltage output must be converted to well regulated 48 V DC voltage with the second stage. The second stage at this power rating is typically a DC/AC/DC converter consisting of an inverter, a transformer, and a rectifier connected in cascade form. This structure is illustrated in Figure 1.1.

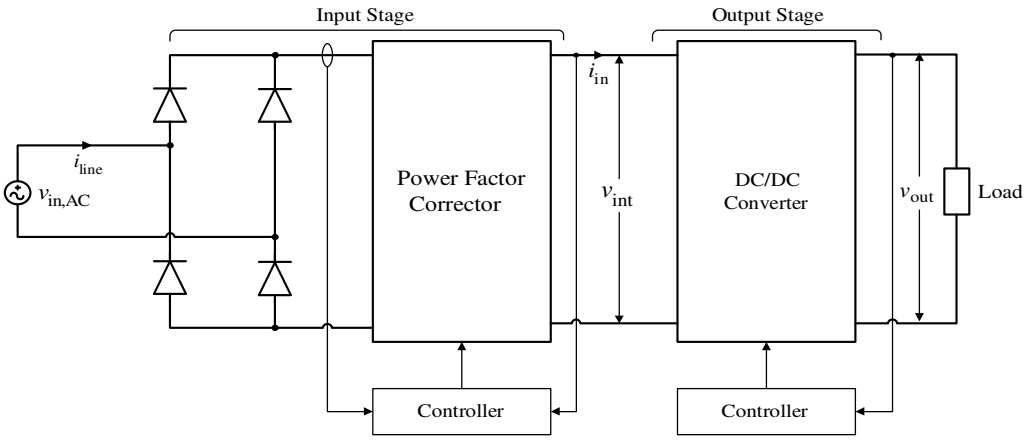

Figure 1.1 A two stage AC/DC converter employing input power factor correction.

The focus of this thesis is the design and implementation of such a high performance switch–mode power supply. The work involves design and implementation of an interleaved PFC for high performance and small size, the controller design and implementation of the full bridge phase shifted zero voltage switching DC/DC converter, and the integration of the two stages to form a high performance power supply.

1.2 Power Factor Correction

The average apparent power driven from the utility grid is expressed by (1.1).

$$S = \left(v_{in,AC}\right)_{rms}\left(i_{line}\right)_{rms} \tag{1.1}$$

The real power drawn by the load is defined as the product of the first harmonic component of the line voltage and the first harmonic component line current which is in phase with the line voltage (1.2).

$$P = \left(v_{in,AC}\right)_{1,rms}\left(i_{line}\right)_{1,rms}\cos\varphi \tag{1.2}$$

Where, φ is the angle between the phasor vectors of the real power and the apparent power. Power factor is the quantity defined for measuring the ratio of the real power driven by the load to the apparent power as in (1.3) [1].

$$PF = \frac{P}{S} = \frac{\left(v_{in,AC}\right)_{1,rms}\left(i_{line}\right)_{1,rms}}{\left(v_{in,AC}\right)_{rms}\left(i_{line}\right)_{rms}}\cos\varphi \tag{1.3}$$

With the assumption of ideal grid, the only harmonic component of the line voltage is the first harmonic component. Therefore (1.3) takes the form (1.4).

$$PF = \frac{(i_{line})_{1,rms}}{(i_{line})_{rms}} \cos\varphi = k_{dist} k_{disp} \tag{1.4}$$

From (1.4) it is seen that there are two components of the power factor, distortion factor (k_{dist}), and displacement factor (k_{disp}). The distortion factor is the ratio of the line current first harmonic rms value to the line current rms value. The displacement factor is the ratio of the phasor magnitudes of real power to the apparent power. The index called total harmonic distortion can be defined to quantify the amount of the distortion in the line current and expressed by (1.5) [1].

$$\%THD = \frac{\sqrt{(i_{line})^2_{rms} - (i_{line})^2_{1,rms}}}{(i_{line})_{1,rms}} \tag{1.5}$$

Power factor can be described in terms of THD and displacement factor.

$$PF = \frac{1}{\sqrt{1+THD^2}} k_{disp} \tag{1.6}$$

The AC voltage present on the utility is converted to a DC voltage by diode or thyristor rectifiers due to the simplicity of the structure. The output voltage waveform is smoothened by the utilization of a big output capacitor as shown in Figure 1.2. There are several disadvantages involving this easy approach. Mainly the output capacitor voltage cannot be controlled and therefore the output voltage changes when the load current changes.

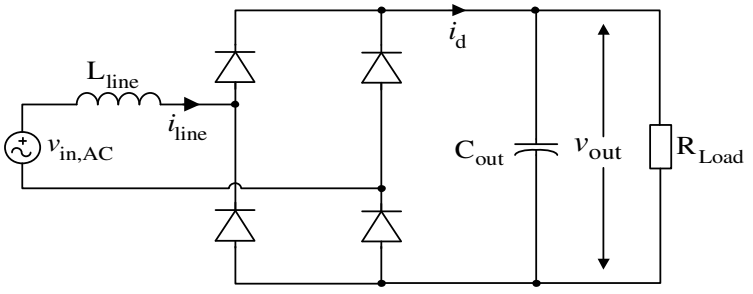

Figure 1.2 Practical diode bridge rectifier with a filter capacitor.

The output current of the diode rectifier, which is denoted by i_d in the figure, becomes discontinuous due to the output filter capacitor [1]. Such a discontinuous current contains large number of harmonics which contribute to the line current distortion; therefore the THD becomes very large.

Obtained by a simulation, the waveforms of the current driven from the line and output voltage of a full bridge diode rectifier are given in Figure 1.3. The system parameters of this rectifier are given in Table 1.1.

Table 1.1 System parameters of the full bridge diode rectifier

Output Filter Capacitor (C_{out})	4	mF
Line Inductor (L_{line})	1	mH
Load Resistance (R_{Load})	35	Ω

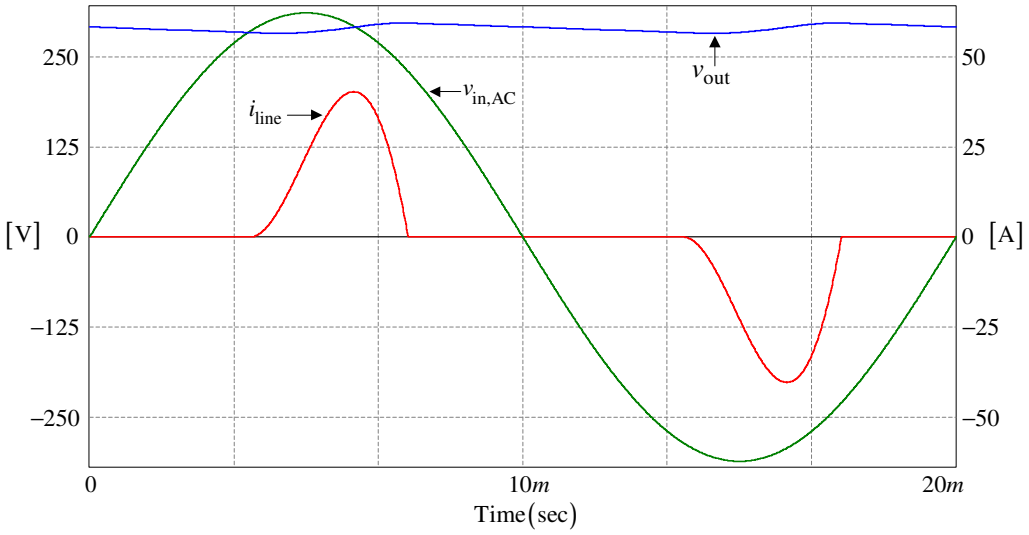

Figure 1.3 The waveforms of a full bridge diode rectifier with output filter capacitor: the line voltage (green), line current (red), and output voltage (blue).

The harmonic components of the line current are shown in Figure 1.4. The odd harmonics are spread over a wide frequency range and the magnitudes of them are comparable with the first harmonic. This results in high THD and low power factor. The THD of the line current is calculated as 99.5% and power factor is calculated as 0.68. In modern power supplies the THD requirement is reduced down to 3% and power factor requirement is increased to unity.

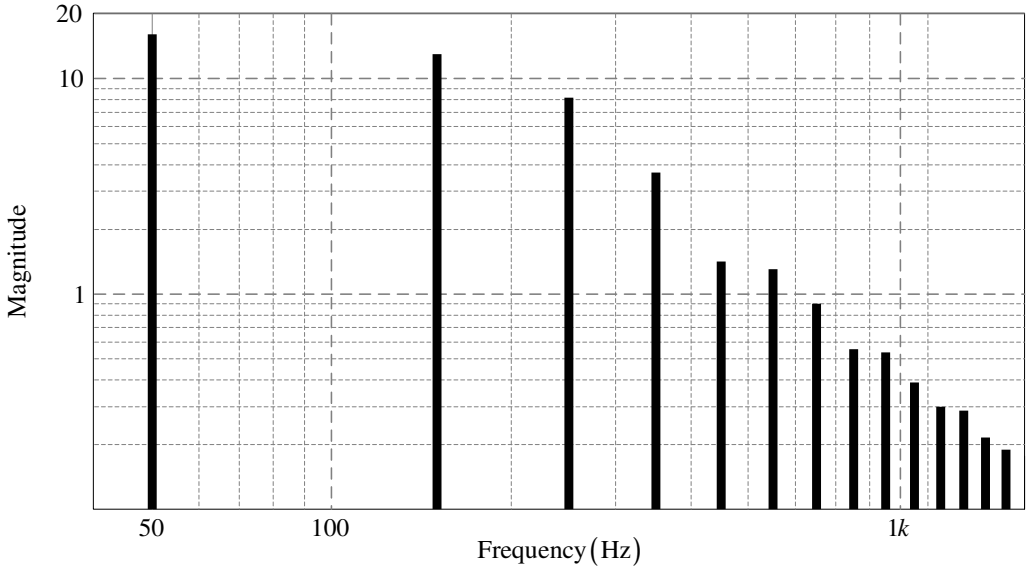

Figure 1.4 Harmonic components of the line current.

The following hazardous problems may occur due to harmonics:

- The voltage in the utility grid is distorted.
- Core losses of the magnetic equipment such as transformers and electric motors increase.
- The electrical equipment connected to the grid can be damaged.
- Heating problems on capacitive load banks may occur.
- Electromagnetic propagation may occur on transmission lines and this may result in electromagnetic interference (EMI) with sensitive equipments.

In order to avoid harmonic contributions to the line, some international standards were published. The last edition of the standard IEC 61000–3–2, “Limits for harmonic current emissions,” was published by International Electrotechnical Commission (IEC) in 2005. This standard regulates the harmonic contribution for equipment input current up to and including 16 A per phase [IEC 61000–3–2]. Power factor correction methods are applied for adopting the electrical equipments to such standards and reducing the harmonic contribution. There are two main approaches for power factor correction: passive and active approaches. In the passive approach passive components such as inductors and capacitors are utilized. Switch mode power supply topologies are adapted to power factor correction applications in the active approaches. The content of the harmonic regulation standards and passive power factor correction methods are out of the scope of this thesis but some information about these topics can be found in [2].

The waveform input current is forced to track the waveform of the input voltage in active power factor correction methods to provide unity input power factor and low current THD. Active PFC methods are preferred in modern power supplies because of their high performance and high efficiency. In this thesis, for the design of the PFC stage, the active PFC interleaved boost topology is chosen. The boost topology is the most popular topology for power factor correction applications. The main reason is the continuous inductor current provided at the input. Interleaving is a known and applied technology in power electronics for years [3]. The previous interleaving technologies involved self design of the phase shift and controllers while in this thesis the new control chip is utilized.

Interleaving is beneficial in particular for high power converters, surpassing several hundred watts. As the power rating increases, one PFC circuit can not meet the thermal and electrical performance requirements. Increasing the power rating by paralleling elements is not a good idea for the transistors in particular. Paralleling PFC units is thermally favorable, but electrically the stresses remain relatively high. Paralleling units and providing phase shift between their PWM signals, which are the basic principle of interleaving results in better electrical and thermal performance of

the converter. The PWM signal interleaving technique is a fairly old concept, which has been applied to various power converter systems. While its application to PFC systems has been reported, this has been mainly for small power rating units and mainly by designing the phase shift mechanism with hardware. This thesis involves the implementation of the technique using a recently developed monolithic chip. Also, a relatively high power rating system has been built, manufactured, and tested to illustrate the performance of such a system.

1.3 Output DC/DC Converter Stage

The regulated DC voltage of the PFC stage is usually converted into different power forms considering the specifications of the applications. The provided DC voltage can be converted into different DC voltage levels or can be converted to varying frequency AC voltage for AC motors. The modern and energy efficient method of converting a DC level power to another form is by means of switch mode power supplies. The full bridge DC/DC converter topology has some superior features compared to other topologies in multi–kilowatt applications. The isolation of input and output stages is the main feature provided by the topology. The load connected to the output is protected against malfunctions that may occur at the input stage. Another important feature provided by the topology is its suitable structure for applying soft switching methods. In conventional hard switching converters semiconductor losses are generated during switching transients. These losses are originated from the voltage–current characteristics of switches. At turn–on transients switch current is developed while there is still a potential difference between the switch terminals and at turn–off switch voltage is developed before the switch current is ceased to zero. The switching frequency is limited and electromagnetic propagation occurs because of switching losses. In the full bridge DC/DC converter topology with the implementation of the phase shifted PWM method and properly designed isolation transformer, the switches are turned on at zero voltage [4]. Zero voltage switching (ZVS) is provided by the resonant transfer of the energy stored in the leakage inductor of isolation transformer to the parasitic output capacitors of the

switches. With the reduction of switching losses, the switching frequency can be increased and the volume of the magnetic components can be reduced.
In this thesis, the output voltage of the full bridge phase shifted zero voltage switching (FB–PS–ZVS) DC/DC converter is controlled digitally. The gate signals of the semiconductor switches are generated by a digital signal processor (DSP). The flexibility of the converter control can be improved by the digital control.

1.4 Scope of the Thesis

The motivation point of this thesis involves investigating the performance of the converter by theory, simulation and experimental study of a prototyped two stage power converter. The input stage consists of an interleaved boost PFC and the output stage consists of an FB – PS – ZVS DC/DC converter. The utilization areas of such a converter may be wide in the market due to distinct features provided by both the input and output stages.

The input stage is studied in Chapter two in detail. First, the theory is reviewed and then the circuit average model of the boost PFC has been derived for the purpose of controller design. Then, the controller design is followed by detailed interleaved PFC converter simulations. Finally the simulation results are verified by the experimental investigation of the manufactured 2.5kW PFC converter.

Chapter three involves the second stage of the conversion, the DC/DC converter. Here, the DC/DC converter is ZVS–PS–FB type and a hardware manufactured by a former graduate student, Mr. M. Uslu has been utilized [5]. Interfaces and signal conditioning devices have been built and the output voltage regulator for the ZVS has been established in this thesis. The converter small signal state-space modeling has been provided to derive the system small signal transfer functions. Then, utilizing the transfer functions, the controller has been designed. Utilizing the design parameters, a simulation has been built to verify the control method. Finally, the laboratory performance of the system has been proven.

Chapter four integrates the AC/DC and DC/DC converter stages. Here the hardware system is described and the experimental results of the AC/DC conversion system regarding power quality, energy efficiency, and output voltage regulation are illustrated.

This thesis overall studies the AC/DC converter operating principle, design, control, and detailed performance. In particular the interleaving technology as applied to the input PFC stage has been the main focus and its practical realization which involves technical challenges, has been considered. A 2.5kW converter system has been manufactured and its laboratory tests conducted to verify the overall high power quality and control performance.

CHAPTER 2

DESIGN AND IMPLEMENTATION OF A TWO PHASE INTERLEAVED BOOST POWER FACTOR CORRECTION PRE-REGULATOR CIRCUIT

2.1 Introduction

Active power factor correction (PFC) techniques are widely utilized in the power electronic products for their low cost and high performance. Several converter topologies may be utilized for active power factor correction applications. Among these topologies, the boost converter topology (boost PFC topology) is utilized most frequently due to its advantages over other topologies. The main advantage of the boost PFC topology is its continuous input current which can be forced to track the diode bridge rectifier output voltage. Non–pulsating input current eases current waveform shaping while reducing EMI in the power line. Also the ground referenced power switch eases and reduces the cost of the gate driving circuitry. In boost PFC applications, the average current mode control method is widely utilized for its suitability to the topology. For high power applications, decreasing stresses on the power semiconductor switches, decreasing the input and output current ripples, and increasing the power density of the converter become the main issues. The interleaving technique is utilized in order to provide such requirements in multi–kilowatt PFC applications. In this thesis study, the two–phase interleaved boost power factor corrector which is controlled by the average current mode control method is investigated, its mathematical model is analyzed, computer simulations are performed, and a 2.5 kW prototype is designed and manufactured. The interleaving continuous conduction mode PFC converter controller integrated circuit (IC) manufactured by Texas Instruments, UCC28070 is utilized as the control IC in the

design. In this chapter, the steady–state analysis of a two–phase interleaved boost PFC circuit is performed, a small signal model for average current mode control is derived, all derived expressions are verified via computer simulations, and the experimental results of the prototype pre–regulator are presented.

2.2 Review Of The Basic DC/DC Boost Converter Topology

The classical boost converter topology is one of the basic non–isolated converter topologies that is utilized for generating an output voltage greater than the input voltage. The boost topology schematic diagram is given in Figure 2.1.

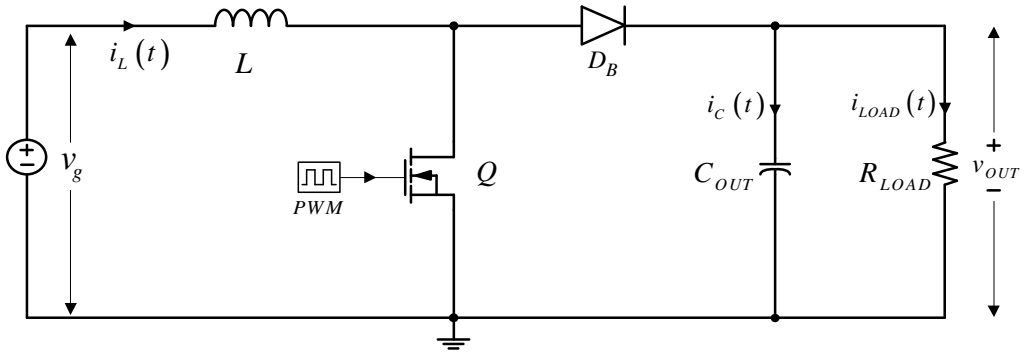

Figure 2.1 The basic boost converter schematic diagram (using a MOSFET switch).

The operation principle of the converter is based on transferring the stored energy in the boost inductor (L) to the output capacitor (C_{OUT}) and load by controlling the switch (Q). When the switch is on, as shown in Figure 2.2(a), the inductor output terminal is connected to the ground and energy is stored depending on its inductance value and the on time duration of the switch. The stored energy is transferred to the output when the switch is in off state (Figure 2.2(b)).

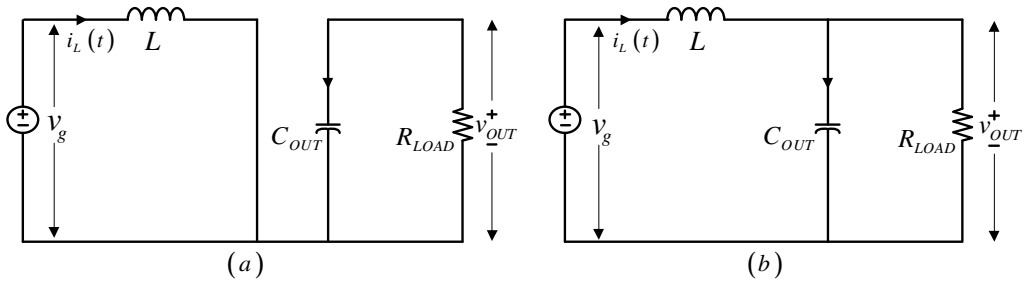

Figure 2.2 Boost converter circuit modes; (a) switch Q is on, (b) switch Q is off.

Let s be the switching function of the switch Q as expressed in (2.1) and s' be the complementary of s.

$$\begin{aligned} &s = 1, \text{ when the switch is on} \\ &s = 0, \text{ when the switch is off} \\ &s' = 1 - s \end{aligned} \tag{2.1}$$

The inductor voltage can be expressed by equation (2.2)

$$L\frac{di_L}{dt} = v_g - s'v_{OUT} \tag{2.2}$$

In order to prevent energy build-up in the inductor, the total volt–seconds applied to the inductor over one switching period should be zero. Therefore, the integral of (2.2) over one switching period should be equal to zero.

$$\int_0^{T_S} \left(v_g - s'v_{OUT}\right)dt = \int_0^{DT_S} v_g\,dt + \int_{DT_S}^{T_S} \left(v_g - v_{OUT}\right)dt = 0 \tag{2.3}$$

The relationship of input and output voltages, which is given in (2.4), can be derived by solving (2.3).

$$\frac{v_{OUT}}{v_g} = \frac{1}{D'} \tag{2.4}$$

D'=1-D is the complementary of D. The output voltage of the converter is inversely proportional to the complementary of the duty cycle (D'), and directly proportional to input voltage (v_g). In PFC applications, the input voltage is not constant DC; it is a rectified AC voltage which has the shape of absolute value of a sine function. Therefore, the duty cycle is continuously alternating with alternating input voltage to provide nearly constant dc output voltage.

2.3 Advancing Power Ratings of PFC Converters

The power level of a power electronic converter is limited due to several factors. Increasing current increases stresses on switching devices, diode reverse recovery current and parasitic resonance currents become greater than the main switch can handle, and the size of the boost inductor should be increased to avoid saturation and overheating problems. The component stresses can be reduced by controlling the turn off rate of the boost diode current by implementing passive or active snubber circuits [6] and the power level can be slightly advanced, but in order to advance the power level significantly the methods including device paralleling, module paralleling, power stage paralleling, and interleaving are widely utilized.

2.3.1 Device Paralleling

Paralleling two or more switching devices is a widely utilized approach to increase the current handling capability of switches. The same PWM signal is applied to devices and switch currents are shared. This method can be utilized to positive temperature constant (PTC) devices such as MOSFETs easily. When the temperature of a PTC device increases, its internal resistance also increases, therefore current flowing through it decreases and excess current flows through other paralleled

devices. Current is shared equally without forcing with these devices. Paralleling operation is not easy with negative temperature constant (NTC) devices like IGBTs. When the temperature of an NTC device increases, its internal resistance decreases, therefore more current flows through the device and the temperature further rises, the internal resistance further decreases, and so on, until the device fails. Therefore, the current cannot be shared equally without forcing with utilization of NTC devices. The device paralleling method is not practical for all applications.

2.3.2 Converter Paralleling

For some applications, boost stages are designed modularly such that the converter stages can be connected in parallel to meet the increasing power requirement. This method is preferable as it is easy to increase the power rating by simply stacking converters, and increased redundancy. The drawbacks of the method are; its relatively high cost, large volume covered, and cooling difficulties. Furthermore, to provide equal sharing of input current among the converters, additional circuitry should be utilized and the switched currents of individual converters do not return properly, switched current of one module can circulate through other module and some unexpected failures may occur [7].

2.3.3 Power Stage Paralleling

The power stage of the converter consists of semiconductor switches and magnetic components. The drawbacks such as unbalanced current sharing between semiconductor switches and magnetic saturation is partially overcame by the power stage paralleling method. A boost rectifier which has N–phase paralleled power stage is shown in Figure 2.3. The same PWM signal is applied to switches Q_1 to Q_N and the input current, i_g, is shared equally among N power branches. In this configuration, transistors are not paralleled directly; therefore current sharing problems mentioned previously are not an issue. Besides, energy storage requirement

of the inductors is decreased, so the total magnetic component volume can be reduced significantly. This method is better than the previously mentioned two methods in the safe operation and power density aspects. Furthermore, hot swapping and increasing the power rating by simply stacking modules is possible.

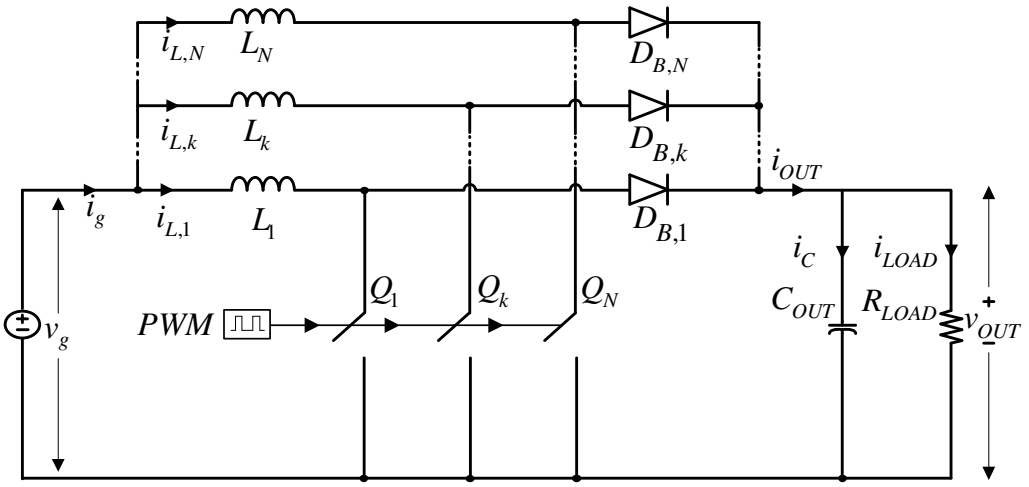

Figure 2.3 Boost rectifier with N–phase paralleled power stage.

2.3.4 Interleaving

The method explained in the previous section is very practical but not the optimal solution in terms of converter performance and size considerations. The same paralleling method can be utilized with a different switching pattern than the identical switching patterns of the previous section in order to reduce input current and output voltage ripples. The separate power branches are controlled by interleaved switching signals but they have a phase shift. In Figure 2.4 a general structure for an N–phase interleaved boost converter is given. Mathematically there is no limit for the number of interleaved power branches. But, in practice as the phase number increases, the system complexity increases and maintenance becomes difficult. The main advantage of interleaving is the reduction of input current and output voltage ripples with smaller magnetic material volume than other methods.

The input EMI filter size and output capacitor size are reduced in proportion with the ripple reduction. The disadvantage of the interleaving method is increase in the gate driving logic complexity, but necessarily the size and cost of the gate drive. Logic signals to all the gates are equally phase shifted by the amount defined in (2.5).

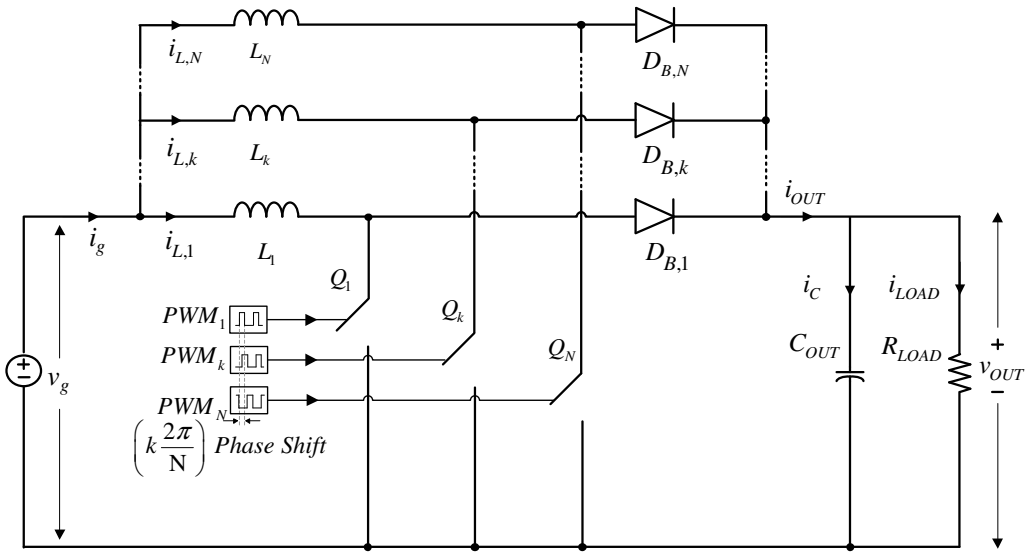

Figure 2.4 N–Phase interleaved boost converter.

$$PS = k\frac{2\pi}{N} \tag{2.5}$$

In (2.5), N denotes the number of interleaved branches and k denotes the order of discrete interleaved branches ($k = 1,\ldots, N$). In Figure 2.5, PWM signals applied to a four–phase interleaved boost converter are given. In this case, a four phase interleaved boost converter has gate drive logic signals that are sequentially gated with 90º phase delays with respect to each other.

The input current and output voltage ripple reduction for an N–phase interleaved converter is analyzed in the following sections. In the analysis, each power branch is assumed to be identical, the inductors are totally decoupled, and inductor copper losses are zero. A more detailed analysis can be found in [8].

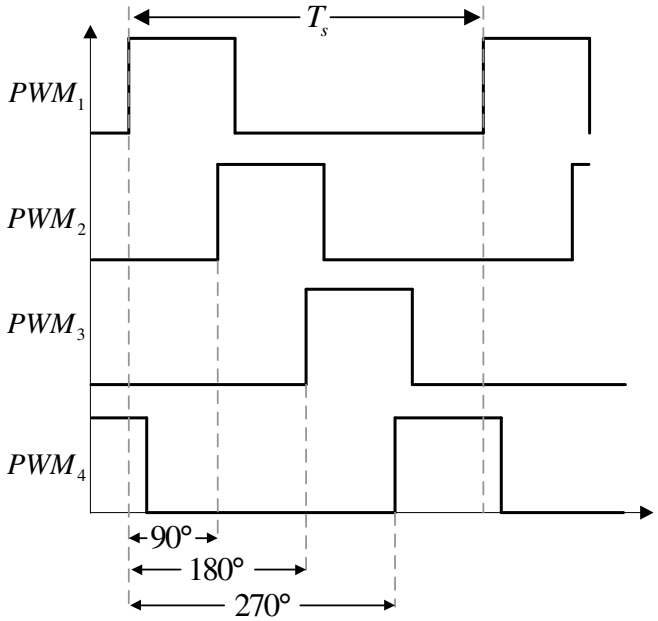

Figure 2.5 PWM signals applied to discrete legs of a four–phase interleaved boost converter.

2.3.4.1 Input Current Ripple Reduction

The input current, i_g, is the sum of distinct inductor currents. Inductor currents in separate branches can be assumed to have the same magnitude as the power branches are identical. In Figure 2.6(a) the inductor current waveforms and in Figure 2.6(b) the input current waveform of a four–phase interleaved boost rectifier are given. From Figure 2.6, it is seen that the amplitude of the input ripple and ripple period are decreased due to the interleaved switching of transistors. The period, τ, of the input current ripple can be expressed by (2.6). In the equation, T_s denotes the switching period.

$$\tau = \frac{T_S}{N} \tag{2.6}$$

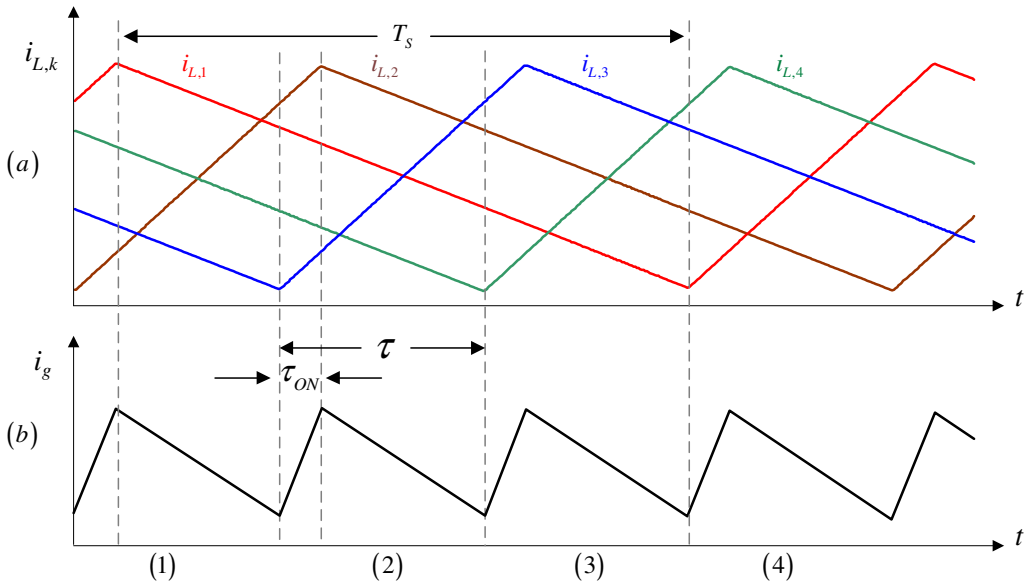

Figure 2.6 Current waveforms of a four–phase interleaved boost converter, (a) inductor current ripple waveforms, (b) input current ripple waveform.

During a ripple period, τ, only one transistor is switched and other switches are in their on or off states depending on duty cycle. For example, in Figure 2.6, during sub–period (2), Q_2 is switched while Q_1 and Q_4 are in their off state and Q_3 is in its on state. Equation (2.7) is valid for N–phase interleaved boost converters.

$$N = N_{ON} + N_{OFF} + 1 \tag{2.7}$$

In (2.7), N_{ON} and N_{OFF} denote the number of transistors which are in their on and off states during a input current ripple period. N_{ON} and N_{OFF} depend on the duty cycle. The rising time of input current can be denoted by τ_{ON}, and duty cycle of input current ripple, q, can be expressed by using this term (2.8).

$$q = \frac{\tau_{ON}}{\tau} \tag{2.8}$$

By investigating Figure 2.6, it is seen that the rising time of input current is dependent on the rising time of inductor current, period of input ripple current, and number of on state transistors. This relationship can be expressed by (2.9).

$$\tau_{ON} = T_{ON} - N_{ON}\tau \tag{2.9}$$

A generalized expression (2.10) for q can be derived by substituting (2.6) and (2.8) into (2.9).

$$q = ND - N_{ON} \tag{2.10}$$

The input current, i_g, is the sum of all inductor currents and is expressed by (2.11).

$$i_g = \sum_{k=1}^{N} i_{L,k} \tag{2.11}$$

Equation (2.12) is valid due to the linearity of (2.11).

$$\frac{di_g}{dt} = \sum_{k=1}^{N} \frac{di_{L,k}}{dt} \tag{2.12}$$

The expression for the inductor current of a boost converter is given by (2.2). Thus, the change of input current by time can be expressed by (2.13) with substituting (2.2) in (2.12).

$$\frac{di_g}{dt} = N\frac{V_g}{L}\left(1 - \frac{1}{ND'}\sum_{k=1}^{N} s_k'\right) \tag{2.13}$$

The expression for input current ripple for an N–phase interleaved boost converter, (2.14), can be derived from (2.13).

$$\Delta i_g = N \frac{V_g}{L} \left(1 - \frac{1}{ND'} \sum_{k=1}^{N} s'_k \right) q\tau \tag{2.14}$$

From (2.14), it can be seen that the input current ripple depends on the duty cycle and number of interleaved phases. The ratio of the input current ripple to any inductor current ripple is calculated for two and four phases and their change depending on duty cycle change is shown in Figure 2.7.

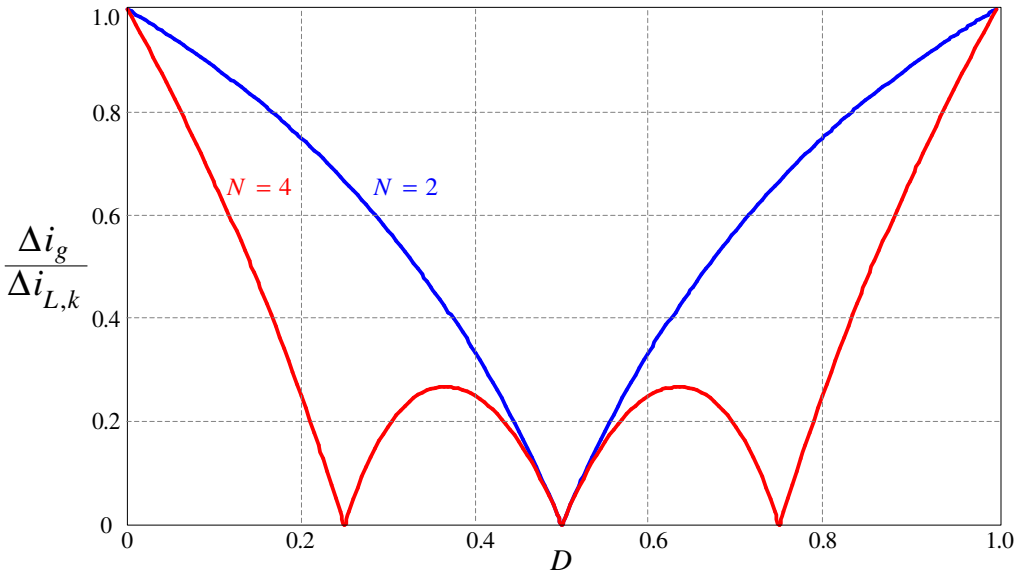

Figure 2.7 Input current ripple variation of an interleaved converter according to duty cycle and number of phases.

Several comments can be made by investigating the figure:

- The relative input current ripple is equal to one, when the duty cycle is zero or unity.

- Zero input current ripple can be obtained theoretically at some special duty cycles, expressed by (2.15).

$$D_{zero} = \frac{k}{N} \tag{2.15}$$

- The input current ripple decreases with increasing number of interleaved phases.

2.3.4.2 Output Voltage Ripple Reduction

The output current of the converter is the sum of capacitor current and load current. The output current has a periodical AC component and a DC component. It is assumed that the output capacitor is large enough to suppress all AC ripple current therefore AC component flows through the capacitor and the average value of the current flows through the load. The waveforms of inductor currents and output current of a four–phase interleaved boost converter are given in Figure 2.8.

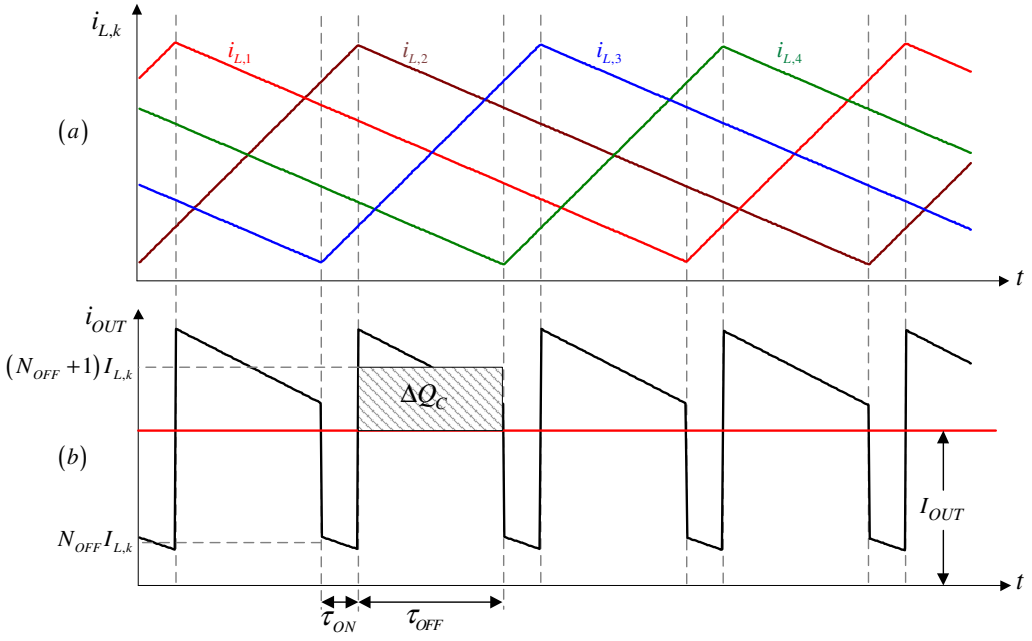

Figure 2.8 For a four-phase interleaved boost converter, (a) the inductor currents, (b) the output current.

In Figure 2.8, $I_{L,k}$ denotes the average value of the inductor current of branch k and I_{OUT} denotes the average value of the output current. During τ_{ON}, the switched transistor is in its on state and during τ_{OFF}, the switched transistor is in its off state. Therefore during τ_{ON}, N_{OFF} diode currents are transferred to the output and during τ_{OFF}, $(N_{OFF}+1)$ diode currents are transferred to output. The shaded area, ΔQ_C, in Figure 2.8 denotes the charge accumulated in the capacitor to provide constant output current. ΔQ_C can be expressed by (2.16).

$$\Delta Q = \left\{ \left(N_{OFF} + 1 \right) I_{L,k} - I_{OUT} \right\} q' \tau \tag{2.16}$$

Where q'=1-q, denotes the complementary of q. The average input current, I_g, is shared among N inductors according to identical power branches assumption. Therefore equation (2.17) is valid.

$$I_{L,k} = \frac{I_g}{N} = \frac{I_{OUT}}{ND'} = \frac{V_{OUT}}{R_{LOAD} ND'} \tag{2.17}$$

The expression for q given in (2.10) can be expanded to express q' as in (2.18).

$$q' = ND' - N_{OFF} \tag{2.18}$$

Substituting (2.17) and (2.18) in (2.16) yield a more generalized expression for ΔQ (2.19).

$$\Delta Q = \frac{T_S}{N^2} \frac{V_{OUT}}{R_{LOAD}} \frac{qq'}{D'} \tag{2.19}$$

The relationship between the charge and the voltage of a capacitor is given in (2.20).

$$\Delta V = \frac{\Delta Q}{C} \tag{2.20}$$

Substituting (2.19) in (2.20) yields the expression for the output voltage ripple (2.21).

$$\Delta V_{OUT} = \frac{T_S}{N^2} \frac{V_{OUT}}{R_{LOAD} C_{OUT}} \frac{qq'}{D'} \tag{2.21}$$

The output voltage ripple depends on the switching period, output voltage, load resistance, output capacitor, and the duty cycle as in conventional single phase boost converter. Additional parameters for interleaving method are the number of interleaved branches and duty cycle of sub–periods. In order to show the effect of interleaving on output voltage ripple, the ratio of output voltage ripple to output voltage is divided to common parameters for single and multi–phase converters, (2.22).

$$\left(\frac{\Delta V_{OUT}}{V_{OUT}} \right)_{NORM} = \frac{\Delta V_{OUT}}{V_{OUT}} \frac{R_{LOAD} C_{OUT}}{T_S} = \frac{qq'}{N^2 D'} \tag{2.22}$$

The normalized output voltage ripple ratio according to duty cycle for different number of phases is shown in Figure 2.9.

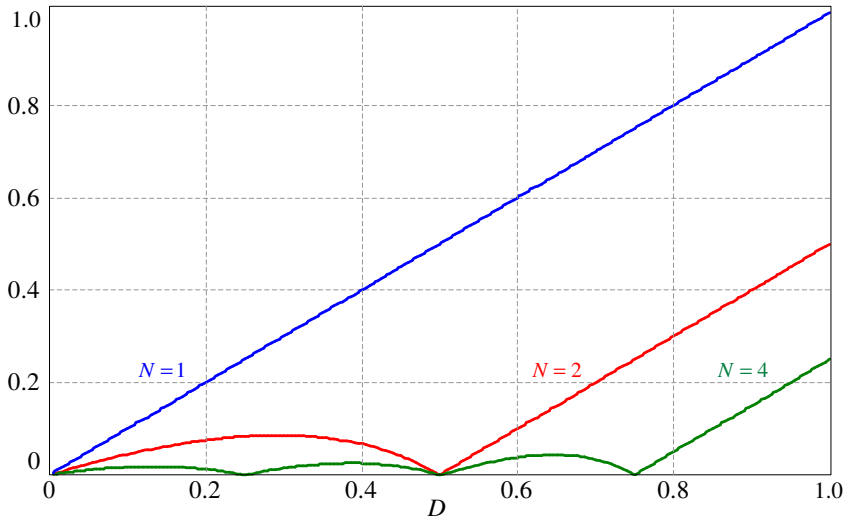

Figure 2.9 The normalized output voltage ripple ratio according to duty cycle for different number of phases.

The output voltage ripple is minimized at the points where the input current ripple is minimized. The output current ripple can be decreased by increasing the number of interleaved phases.

In the previous two sections, the effect of interleaving on the input current and the output voltage ripples were investigated. It has been illustrated that, these ripples are significantly reduced by the interleaving method, allowing the manufacture more EMI compliant converters and utilization of smaller EMI filters and output capacitors.

The total energy storage requirement in boost inductors is reduced with utilization of interleaving method. Therefore the total boost inductor volume can also be reduced. The energy storage requirement for a single phase and multi–phase converters are given in (2.23) and (2.24).

$$E_{Single} = \frac{1}{2} \times L \times \left(i_{L,Single} \right)^2 \tag{2.23}$$

$$E_{Interleaved} = N \left(\frac{1}{2} \times L \times \left(i_{L,k} \right)^2 \right) \tag{2.24}$$

With the assumption of identical power branches, the input current is shared equally among the phase inductors, therefore the current flows through the inductor in single phase case is N times larger than N–phase interleaved case (2.25).

$$i_{L,Single} = N i_{L,k} \tag{2.25}$$

Substituting (2.25) into (2.24) yields,

$$E_{Interleaved} = N \left(\frac{1}{2} \times L \times \left(\frac{i_{L,Single}}{N} \right)^2 \right) = \frac{E_{Single}}{N} \tag{2.26}$$

The energy storage requirement in the boost inductor for a single phase converter is N times larger than total energy storage requirement of N–phase interleaved converter. A simple inductor with air gap is illustrated in Figure 2.10.

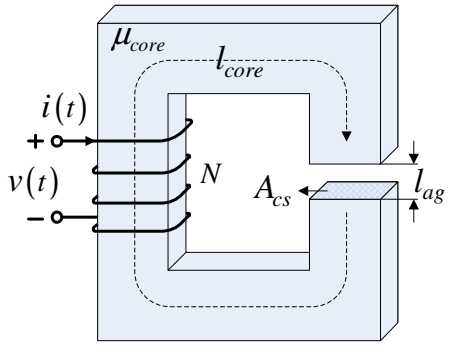

Figure 2.10 Simple inductor with air gap.

The magnetic flux can be assumed continuous throughout the magnetic circuit since air gap length (l_{ag}) is much smaller than the core length (l_{core}) [9]. Therefore magnetic flux is continuous and the same in the core and air gap. The relation between flux density and inductor voltage is given in (2.27).

$$v(t) = NA_{cs}\frac{dB}{dt} \tag{2.27}$$

In (2.27) N denotes the number of the turns, A_{cs} denotes cross sectional area of the core and B denotes the flux density. The magnetic field intensities in the air gap ad in the core are given in (2.28) and (2.29).

$$H_{core} = \frac{B}{\mu_{core}} = \frac{B}{\mu_0\mu_r} \tag{2.28}$$

$$H_{ag} = \frac{B}{\mu_0} \tag{2.29}$$

H_{core} and H_{ag} are the magnetic field intensity in the core and in the air gap. μ_{core} and μ_0 are permeability of core and air gap and μ_r is the relative permeability. Applying Ampere's Law to the magnetic circuit given in Figure 2.10 yields,

$$i(t) = \frac{1}{N}\left(H_{core}l_{core} + H_{ag}l_{ag}\right) = \frac{1}{N}\frac{B}{\mu_0}\left(\frac{l_{core}}{\mu_r} + l_{ag}\right) \tag{2.30}$$

The stored energy in the inductor can be expressed by (2.31).

$$E = \int v(t)\, i(t) dt \tag{2.31}$$

An expression for the stored energy in the inductor can be obtained by substituting (2.27) and (2.30) into (2.31),

$$E = \frac{A_{cs}}{\mu_0}\left(\frac{l_{core}}{\mu_r} + l_{ag}\right)\int B dB \tag{2.32}$$

The stored energy in the inductor is directly related to the size of the inductor as can be seen from (2.32). It is seen that total inductor size smaller in interleaved converter than single phase inverter when (2.32) is compared with (2.26). In other words, the volume of the interleaved inductor is one N^{th} of the volume of the single inductor. A further reduction in the magnetic volume can be achieved by utilizing a single core and integrating all inductors [10] but the analysis of the circuit is changed due to the coupled magnetics among the phases [8].

The benefits of the interleaving technique by means of size and input ripple current reductions are mathematically expressed. In order to design a multi–kilowatt rated PFC, the two-phase interleaved topology has been chosen in this thesis study.

2.4 Average Current Mode Control

The main purpose of active power factor correction control strategies is providing the converter to behave like a resistor to obtain unity power factor. To obtain resistor characteristics, the input current should track the input voltage variations. Average current mode control (ACM) is one of the methods widely utilized to control the inductor current. In the method, the inductor current is averaged, and this averaged value is manipulated by switching the main switch [11]. The ACM control method has some superiority over peak current mode control, which is one of the most popular current mode control methods due to its simplicity. At first, high degree of accuracy can be obtained in input voltage wave shape tracking. Secondly, in the ACM control method slope compensation is not required while it is required in peak current mode control when duty cycles greater than 0.5 are obtained. Lastly, it has excellent noise immunity [12]. The general block diagram of a single phase ACM controlled boost PFC is shown in Figure 2.11.

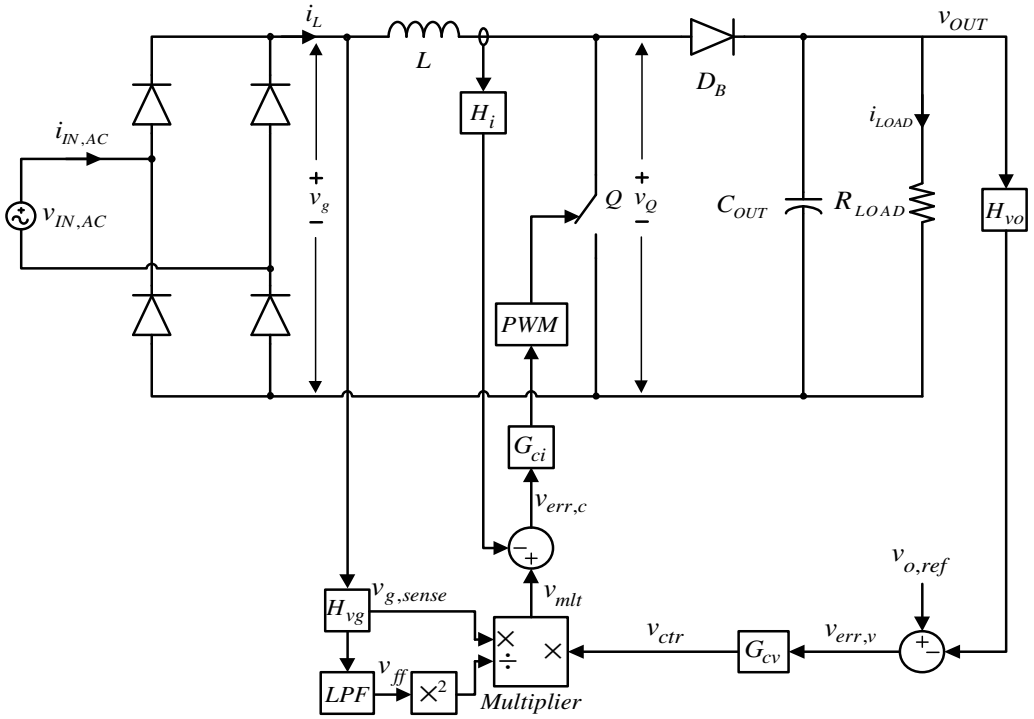

Figure 2.11 Block diagram of a single phase ACM controlled boost PFC.

Descriptions of terms in Figure 2.11 are given below.

H_{vo} : Output voltage sensor attenuation factor.
H_{vg} : Input voltage sensor attenuation factor.
G_{cv} : Output voltage loop compensator.
G_{ci} : Input current loop compensator.
H_i : Inductor current sensor attenuation factor.
$v_{o,ref}$: Output voltage reference.
$v_{err,v}$: Output voltage error.
$v_{err,c}$: Inductor current error.
v_{ctr} : Control voltage.
$v_{g,sense}$: Sensed diode rectifier output voltage.
v_{ff} : Input feedforward voltage
LPF : Low pass filter.

There are two control loops in ACM to the control output voltage and inductor current. The output voltage is sensed with a resistor voltage divider network and compared with a reference input ($v_{o,ref}$) to generate output voltage error. This error is compensated with a compensator (G_{cv}). Voltage loop compensator output voltage (v_{ctr}) is amplitude reference of inductor current. The diode rectifier output voltage (v_g) is sensed with a resistor voltage divider network. This signal is shape reference of the inductor current. The amplitude and shape references are multiplied with a multiplier to generate inductor current reference. The multiplier output is compared with the sensed inductor current and the current error is generated. This error is compensated with the current loop compensator (G_{ci}) and PWM signals for the transistor are generated.

Apart from voltage and current feedback loops, there is a feedforward loop for the purpose of keeping the load power constant. In general, PFC converters are pre–regulator stages for power converters as used in this thesis work. The output stage power converter can be thought as constant power load; therefore the power supplied to the load should be constant, even though the RMS value of input line voltage may

vary in time. An increase in the RMS value of the input line voltage should lead to a decrease in the input line current in order to keep the power constant. Since ACM control involves a multiplier structure [13], this increase results in an increase in the inductor current reference. Therefore, the power supplied to the output stage increases, because the output voltage feedback loop is not fast enough to compensate for sudden changes in the input voltage. The sensed diode rectifier output voltage is passed through a low pass filter (LPF) to gain information about the RMS value of the line voltage. The inductor current reference signal is divided by the square of the LPF output to adjust the current reference for supplying constant power. The effect of the feedforward can be clarified with an example. Assume that the RMS value of the line voltage is doubled. Therefore, to obtain constant power, the inductor current should be halved, but since the magnitude of the current shape reference is doubled, the inductor current is doubled also. Therefore, the resulting power is four times bigger than the initial condition. With the addition of the feedforward loop, the current reference is divided to four and the inductor current is halved, so the power provided to output stage is kept constant [2], [14].

The general operation principle of ACM control for a single phase boost rectifier has been explained. The basic control structure is not different for multi–phase interleaved converters. The only difference is number of current feedback loops. For an N–phase interleaved PFC, there should be N current feedback loops. Furthermore, there should be an additional phase shift circuitry for the switching PWM signals to ensure interleaving operation.

2.4.1 Small Signal Modeling of ACM Control

To understand the small signal perturbation behavior of the PFC system at steady-state operating points and designing stable inner and outer loop controllers, linear time invariant (LTI) small signal model (SSM) of the system should be derived. System SSM can be separated into two parts, power stage SSM and multiplier SSM. The model of the power stage is different for the outer voltage loop and the inner

current loop, because frequency bandwidth of these two loops is significantly different. All details of model derivation will not be given in this thesis. More comprehensive analyses are provided in [14] and [15].

2.4.1.1 Modeling The Power Stage

The operation of the boost converter has been explained in section 2.2. Recalling the basic operational principles, large signal average model of the power stage can be derived. The instantaneous transistor voltage and diode current can be expressed by (2.33) and (2.34).

$$v_Q(t) = s' v_{OUT}(t) \tag{2.33}$$

$$i_{DB}(t) = s' i_L(t) \tag{2.34}$$

$v_Q(t)$ and $i_{DB}(t)$ denote the transistor voltage and the diode current. To obtain an averaged model, the expressions for the transistor voltage and diode current should be averaged over a switching period. The averaged expressions are given in (2.35) and (2.36).

$$\langle v_Q(t) \rangle_{T_S} = d'(t) \langle v_{OUT}(t) \rangle_{T_S} \tag{2.35}$$

$$\langle i_{DB}(t) \rangle_{T_S} = d'(t) \langle i_L(t) \rangle_{T_S} \tag{2.36}$$

$d'(t)$ denotes the complementary duty cycle ($1–d(t)$). The large signal average model of the boost converter is given in Figure 2.12.

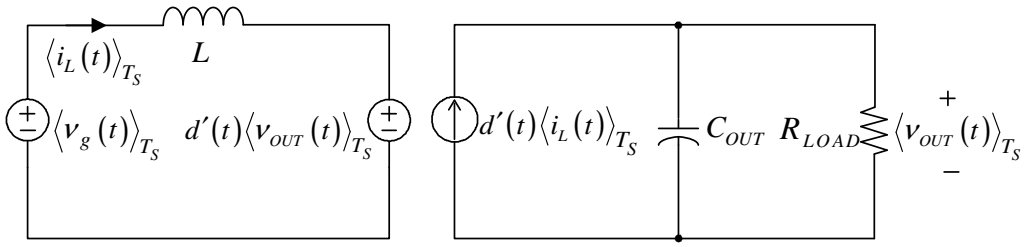

Figure 2.12 Large signal average model of a boost converter.

For a steady-state operating point, large signal averaged values of a boost PFC can be separated into two parts, DC steady-state component and AC ripple component. DC steady-state components are represented by uppercase letters and AC ripple components are represented by subscript "r". Equations (2.37), (2.38), (2.39), and (2.40) express the basic averaged variables with their AC and DC components.

$$\langle v_{OUT}(t)\rangle_{T_S} = V_{OUT} + v_{OUT,r}(t) \tag{2.37}$$

$$\langle i_L(t)\rangle_{T_S} = I_L + i_{L,r}(t) \tag{2.38}$$

$$d'(t) = D' + d'_r(t) \tag{2.39}$$

$$\langle v_g(t)\rangle_{T_S} = V_{RMS} + v_{g,r}(t) \tag{2.40}$$

In (2.40) the DC component of the average value of v_g over one switching period is denoted with V_{RMS} due to the linear relation between the RMS value and the average value of a sine wave. Substituting equations (2.37), (2.38), (2.39), and (2.40) into (2.35) and (2.36) yields,

$$\langle v_Q(t)\rangle_{T_S} = D' v_{OUT,r}(t) + d'_r(t) V_{OUT} \tag{2.41}$$

$$\left\langle i_{DB}(t)\right\rangle_{T_S} = D' i_{L,r}(t) + d'_r(t) I_L + d'_r(t) i_{L,r}(t) \tag{2.42}$$

The expressions in (2.41) and (2.42) are derived under the assumption that V_{OUT} >> $v_{OUT,r}$ due to the large output capacitor. The last term, $d'_r(t)i_{L,r}(t)$ can be approximated to a DC value, because it has a dominant DC components and small second and fourth harmonic contributions [15]. Under the assumption of large output capacitor, harmonic contributions can be ignored; therefore (2.42) can be approximated to an LTI equation (2.43).

$$\left\langle i_{DB}(t)\right\rangle_{T_S} = D' i_{L,r}(t) + d'_r(t) I_L + I_{DC} \tag{2.43}$$

An LTI steady-state model of the converter can be expressed by (2.41) and (2.43).

It is proven that the system can be approximated to an LTI model. Therefore, a small signal perturbation analysis can be performed to derive the SSM of the power stage. A small signal perturbation is added to averaged variables which are expressed by (2.37), (2.38), (2.39), and (2.40). Small signal perturbation contributions are represented by subscript "p".

$$\left\{\left\langle v_{OUT}(t)\right\rangle_{T_S}\right\}_{perturbed} = V_{OUT} + v_{OUT,r}(t) + v_{OUT,p}(t) \tag{2.44}$$

$$\left\{\left\langle i_L(t)\right\rangle_{T_S}\right\}_{perturbed} = I_L + i_{L,r}(t) + i_{L,p}(t) \tag{2.45}$$

$$\left\{d'(t)\right\}_{perturbed} = D' + d'_r(t) + d'_p(t) \tag{2.46}$$

$$\left\{\left\langle v_g(t)\right\rangle_{T_S}\right\}_{perturbed} = V_{RMS} + v_{g,r}(t) + v_{g,p}(t) \tag{2.47}$$

Substituting (2.44), (2.45), (2.46), and (2. 47) into (2.37) and (2.38) yields,

$$\left\{\left\langle v_Q(t)\right\rangle_{T_S}\right\}_{perturbed} = \left\langle v_Q(t)\right\rangle_{T_S} + D'v_{OUT,p}(t) + d'_p(t)V_{OUT} = \left\langle v_Q(t)\right\rangle_{T_S} + v_{Q,p}(t) \quad (2.48)$$

$$\left\{\left\langle i_{DB}(t)\right\rangle_{T_S}\right\}_{perturbed} = \left\langle i_{DB}(t)\right\rangle_{T_S} + D'i_{L,p}(t) + d'_p(t)I_L = \left\langle i_{DB}(t)\right\rangle_{T_S} + i_{DB,p} \quad (2.49)$$

The expressions in (2.48) and (2.49) are derived under the assumption that perturbation contributions are significantly smaller than the DC steady-state and AC ripple components. It is seen from (2.48) and (2.49) that the perturbed transistor voltage and diode current expressions have two components; steady-state average component and small signal perturbation component. Since the steady-state average components are LTI, equations (2.48) and (2.49) are also LTI. Therefore, the small signal perturbation components represent the SSM of the power stage. The SSM of the power stage is given in Figure 2.13.

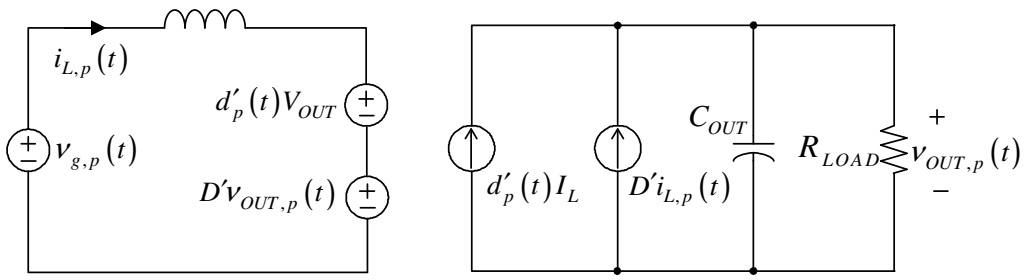

Figure 2.13 The small signal model of the power stage of the boost PFC pre-regulator.

2.4.1.2 The Multiplier Modeling

The multiplier stage has very important role in ACM control. Even though it is the primary source of non–linearity of the control block [15], it can be linearized around the steady-state operation point, due to the fact that variations on the output and input voltages are very small.

The large signal average value of multiplier output can be expressed by (2.50) with considering Figure 2.11.

$$\left\langle i_{mlt}(t)\right\rangle_{T_S} = \frac{\left\langle v_{g,sense}(t)\right\rangle_{T_S}\left\langle v_{ctr}(t)\right\rangle_{T_S}}{\left\langle v_{ff}{}^{2}(t)\right\rangle_{T_S}} \tag{2.50}$$

In practical PFC controller ICs output of the multiplier is current and multiplier output voltage range is adjusted with a resistor, therefore in (2.50) output of the multiplier is denoted by i_{mlt}. The equation set (2.51), (2.52), and (2.53) represent the large signal averaged values of multiplier terms by means of DC steady-state and AC ripple contributions. $v_{g,sense}$ is sensed value of diode rectifier output voltage, therefore it can be expressed by the diode rectifier output voltage times the attenuation factor, H_{vg}.

$$\left\langle v_{ctr}(t)\right\rangle_{T_S} = V_{ctr} + v_{ctr,r}(t) \tag{2.51}$$

$$\left\langle i_{mlt}(t)\right\rangle_{T_S} = I_{mlt} + i_{mlt,r}(t) \tag{2.52}$$

$$\left\langle v_{ff}(t)\right\rangle_{T_S} = V_{ff} + v_{ff,r}(t) \tag{2.53}$$

Attenuation factor H_{vg} is multiplied with (2.40) to obtain $v_{g,sense}$ term in (2.50). Later this term and (2.51), (2.52), (2.53) are substituted to (2.50) and the expression for the average multiplier output current (2.54) is obtained under the assumption that AC ripple contributions are too small compared to their DC contributions

$$\left\langle i_{mlt}(t)\right\rangle_{T_S} = \frac{H_{vg}V_{RMS}V_{ctr}}{V_{ff}^{2}} + \frac{H_{vg}V_{RMS}v_{ctr,r}(t)}{V_{ff}^{2}} + \frac{H_{vg}V_{ctr}v_{g,r}(t)}{V_{ff}^{2}} - \frac{2I_{mlt}v_{g,r}(t)v_{ff,r}(t)}{V_{ff}} \tag{2.54}$$

Equation (2.54) is the large signal LTI expression of the multiplier output (current reference). Adding small signal perturbations to the large signal average values of the multiplier terms given in (2.51), (2.52), and (2.53), results in a new equation set consisting of (2.55), (2.56), and (2.57).

$$\left\{\left\langle v_{ctr}(t)\right\rangle_{T_S}\right\}_{perturbed} = V_{ctr} + v_{ctr,r}(t) + v_{ctr,p}(t) \tag{2.55}$$

$$\left\{\left\langle i_{mlt}(t)\right\rangle_{T_S}\right\}_{perturbed} = I_{mlt} + i_{mlt,r}(t) + i_{mlt,p}(t) \tag{2.56}$$

$$\left\{\left\langle v_{ff}(t)\right\rangle_{T_S}\right\}_{perturbed} = V_{ff} + v_{ff,r}(t) + v_{ff,p}(t) \tag{2.57}$$

Substituting equations (2.47), (2.55), (2.56), and (2.57) into (2.50) yields,

$$\left\{\left\langle i_{mlt}(t)\right\rangle_{T_S}\right\}_{perturbed} = \left\langle i_{mlt}(t)\right\rangle_{T_S} + \frac{H_{vg}V_{RMS}v_{ctr,p}}{V^2_{ff}} + \frac{H_{vg}V_{ctr}v_{g,r}(t)}{V^2_{ff}} - \frac{2I_{mlt}v_{ff,r}(t)}{V_{ff}} \tag{2.58}$$

$$\begin{aligned} i_{mlt,r}(t) &= \frac{H_{vg}V_{RMS}v_{ctr,p}}{V^2_{ff}} + \frac{H_{vg}V_{ctr}v_{g,r}(t)}{V^2_{ff}} - \frac{2I_{mlt}v_{ff,r}(t)}{V_{ff}} \\ &= g_{ctr}v_{ctr,p} + g_g v_{g,r}(t) + g_{mlt}v_{ff,r}(t) \end{aligned} \tag{2.59}$$

The calculation above is conducted under the assumption that perturbation contributions are significantly smaller than the AC ripple and DC steady-state contributions. Equation (2.58) shows that the multiplier model is LTI around the steady-state operation point. Equation (2.59) represents the small signal perturbation contribution of the multiplier output (current reference). In Figure 2.14 the SSM of the multiplier stage is given.

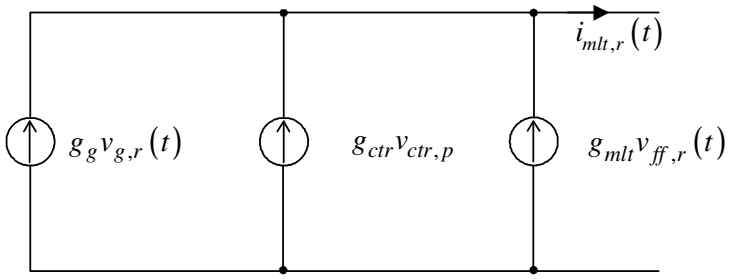

Figure 2.14 The SSM of the multiplier stage.

2.4.2 Controller Design

The SSM of the power and multiplier stages have been derived in previous sections. The general structure of the ACM controlled boost PFC converter, given in Figure 2.15, can be constituted by using those models.

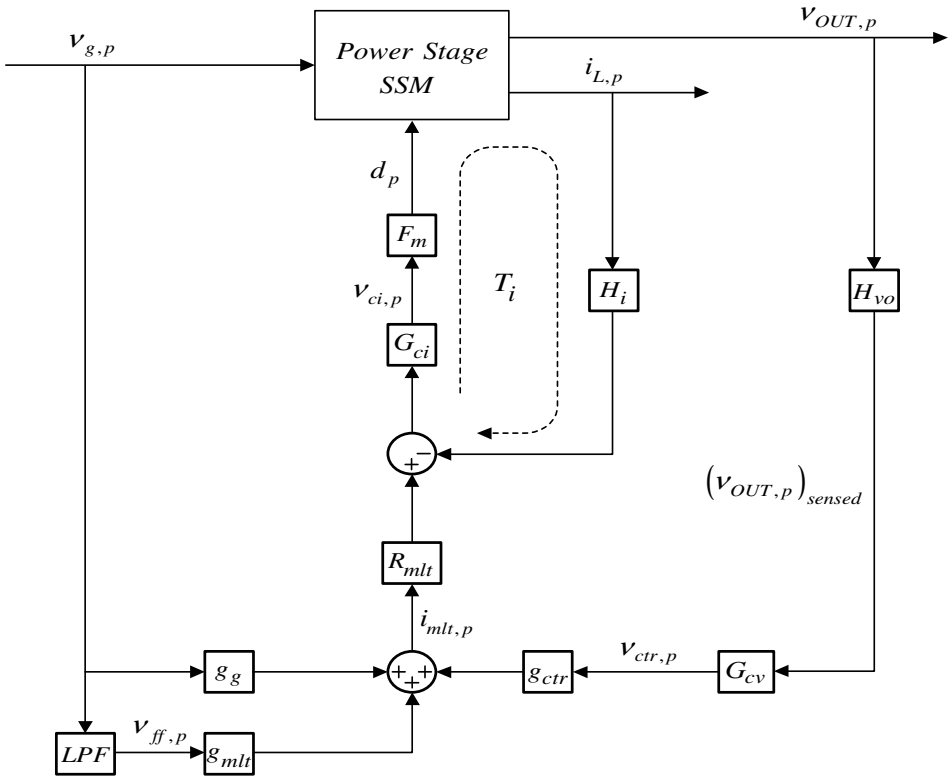

Figure 2.15 Small signal block diagram of the ACM controlled boost PFC converter.

In Figure 2.15, R_{mlt} denotes the multiplier resistance and F_m denotes the PWM unit gain. To generate PWM signals, the output of the current loop compensator, v_{ci}, is compared with a repetitive sawtooth signal, called the PWM carrier signal. The current compensator output should be in the range of between zero and peak voltage value of the carrier signal. Let the peak value of the carrier signal be V_M, then the PWM unit gain, F_m, can be expressed by (2.60).

$$F_m = \frac{1}{V_M} \tag{2.60}$$

The duty cycle becomes unity when v_{ci} is equal to V_M. This means that current error is at its maximum. The duty cycle become zero when v_{ci} is zero, and this means no error.

The duty cycle–to–inductor current and output voltage–to–control voltage transfer functions of the PFC converter system are derived for the design parameters given in Table 2.1. The current and voltage loop compensators are designed by considering these transfer functions.

Table 2.1 Design parameters of the prototype PFC pre-regulator

Parameter	Value	Unit
Target Output Power Rating	5000	W
Output Voltage	400	V
Switching Frequency	40	kHz
Line Frequency	50	Hz
Minimum Input Line Voltage (rms)	180	V
Boost Inductor	1	mH
Output Capacitor	3,30	mF
Current Transformer Turns Ratio	200	A/A
Current Sense Resistor	30	Ω

2.4.2.1 Current Loop Compensator Design

The average inductor current is controlled by a current loop compensation network. The sensed inductor current is compared with the reference current (the multiplier output) and the error is compensated with a second order lead-lag compensator to generate PWM signals for the switches of the interleaved converter. The current loop, shown in Figure 2.15, consists of a current feedback gain, loop compensator, PWM gain, and the small signal transfer function of the power stage. The current loop consists of the current feedback attenuation factor, H_i; current compensator, G_{ci}; PWM modulator gain, F_m, and power stage duty cycle–to–inductor current transfer function. In Figure 2.15, the current loop is denoted by T_i. By considering the figure, current loop can be expressed by (2.61).

$$T_i(s) = H_i(s) G_{ci}(s) F_M(s) G_{id}(s) \tag{2.61}$$

$G_{id}(s)$ is the duty cycle–to–inductor current transfer function. Assuming the output voltage perturbations are negligible due to large output capacitor, the voltage supply $D'v_{OUT,p}$ term of the model given in Figure 2.13 can be omitted. The expression for $G_{id}(s)$ given in (2.62) can be derived by performing a circuit analysis to the reduced model given in Figure 2.13

$$G_{id}(s) = \frac{V_{OUT}}{sL} \tag{2.62}$$

In the prototype converter, the inductor current is sensed by a current transformer with turn ratio, N_{CT}, with the value of 200. Therefore, the current loop feedback attenuation factor is as in (2.63).

$$H_i = \frac{R_{sense}}{N_{CT}} \tag{2.63}$$

R_{sense} is the current sense resistor. In order to obtain high steady-state accuracy and good dynamic response, the current loop should have high gain in low frequencies and reasonable phase margin. A second order compensator with two poles and one zero is utilized to compensate the loop. The transfer function of the compensator is given in (2.64).

$$G_{ci}(s) = \frac{\omega_{ic}}{s} \times \frac{1 + s/\omega_{zc}}{1 + s/\omega_{pc}} \tag{2.64}$$

The gain at the frequencies lower than the corner frequency of the loop is determined by the pole located at ω_{ic} and the pole is located at ω_{zc}. The crossover frequency and the phase margin of the loop are determined by the zero located at ω_{zc} and the pole located at ω_{pc}. The high frequency ripples are attenuated by the pole located at ω_{pc}. As stated, high gain at low frequencies is desirable for minimizing the steady-state error but the gain should be reduced to frequencies up to switching frequency [20]. This is because, in ACM control, the average value of the inductor current is controlled; therefore the switching frequency ripples of the inductor current should be averaged in the compensator. The sensed inductor current ripple can be considered as negligibly low by attenuating the sensed inductor current ripple to one tenth of PWM modulator amplitude. Therefore the zero and low frequency poles of the compensator should be located to provide (2.65).

$$\frac{\omega_{ic}}{\omega_{zc}} \times \frac{\Delta I_L R_{sense}}{N_{CT}} \leq \frac{1}{10} V_M \tag{2.65}$$

The maximum inductor current ripple is denoted by ΔI_L. Loop crossover frequency is determined by equating the open loop gain to unity (2.66).

$$f_{cxo} = \frac{V_{OUT}}{2\pi L} \times \frac{R_{sense}}{N_{CT}} \frac{1}{\Delta V_M} \times \frac{\omega_{ic}}{\omega_{zc}} \tag{2.66}$$

In order to obtain good dynamic response and ensuring stability of the loop the crossover frequency should be suitably high and the phase margin should be around 45°. If the zero of the compensator is located at the crossover frequency, 45° of phase margin is provided. At last a high frequency pole is added to the compensator to attenuate the noises at PWM frequency and higher frequencies. Its value is usually chosen by equating s/ω_p value to 1 at PWM frequency. By applying the procedure explained above, low frequency pole (ω_{ic}) is located to 2.86 kHz, high frequency pole (ω_{pc}) is located to 40 kHz and zero (ω_{zc}) is located to 2.38 kHz. Compensator transfer function is given in (2.67)

$$G_{ci}(s) = \frac{1.2s + 1.799\times10^{4}}{3.979\times10^{-6}s^{2} + s} \tag{2.67}$$

Bode plots of the loop compensator and open loop transfer functions are given in Figure 2.16. From the figure it is seen that the low frequency gain of the current loop is increased to 140dB. The crossover frequency of the loop is obtained at around 2.8 kHz and the phase margin is around 40°.

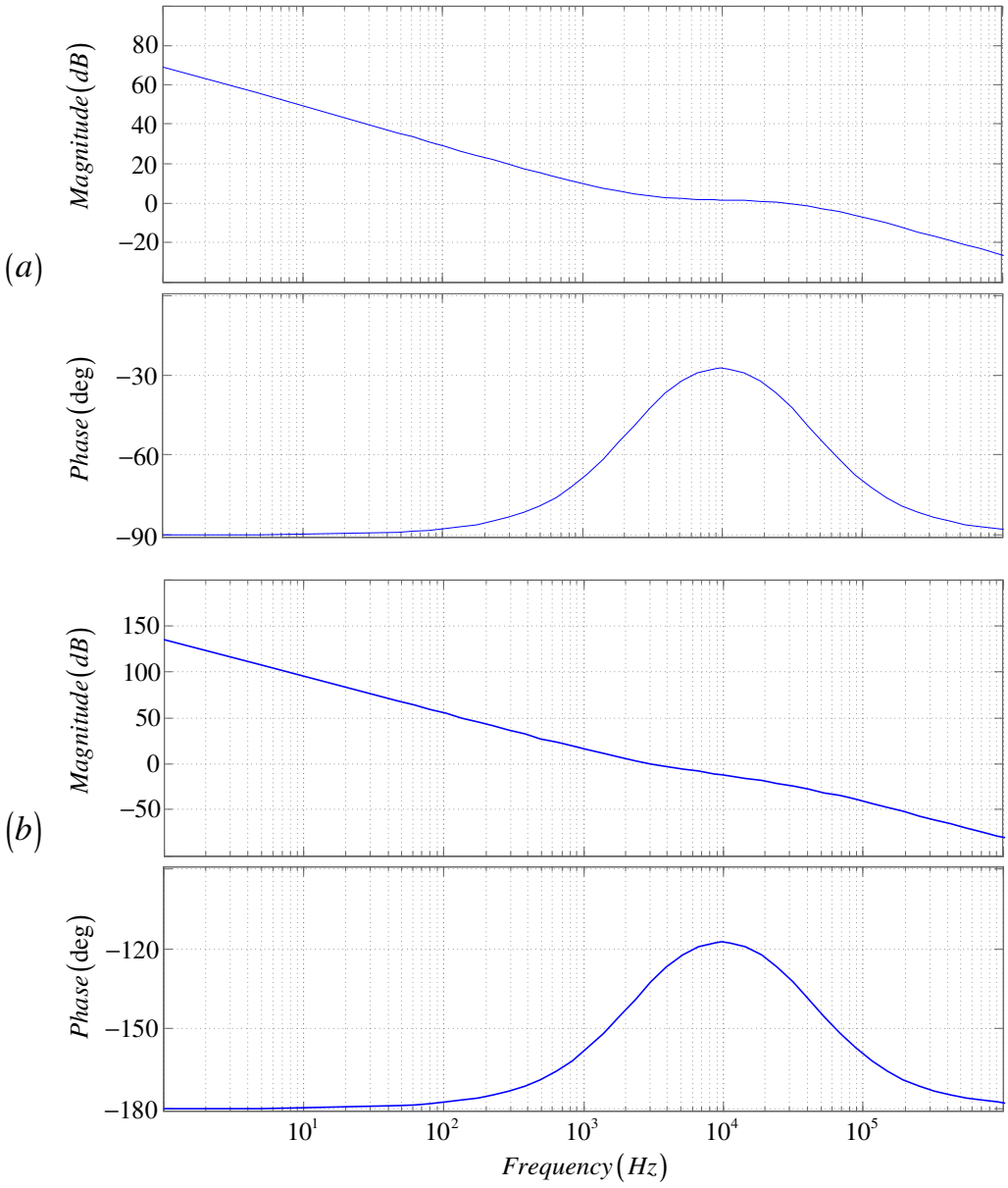

Figure 2.16 Current loop Bode plots, (a) loop compensator, (b) open loop response.

2.4.2.2 Voltage Loop Compensator Design

Output voltage loop compensator design is one of the key design aspects in converter performance because the voltage compensator output signal is amplitude reference of the inductor current. Therefore, to obtain low THD and high power factor, the outer voltage loop should be designed carefully. The control voltage–to–output voltage transfer function of the converter with closed current loop can be found as in (2.68) by analyzing Figure 2.15.

$$\frac{\left(v_{OUT,p}\right)_{sensed}}{v_{ctr,p}} = \frac{H_{vo} g_{ctr} R_{mlt} G_{ci} F_m G_{vd}}{1 + T_i} \tag{2.68}$$

G_{vd} is the duty cycle–to–output voltage transfer function. The expression for G_{vd} given in (2.69) can be derived by applying a circuit analysis to the model given in Figure 2.13 and assuming unity input power factor [14], [15], [16].

$$G_{vd} = \frac{v_{OUT,p}}{d'_p} = \frac{V_{RMS}}{D'^2} \frac{1 - s\dfrac{L}{R_{LOAD} D'^2}}{s^2 \dfrac{LC_{OUT}}{D'^2} + s\dfrac{R_{LOAD}}{L} + 1} \tag{2.69}$$

The reduced expression for the control voltage–to–output voltage transfer function given in (2.70) is derived after substituting (2.69) into (2.68) under the assumption of constant power load and for the frequencies below the current loop crossover frequency [15], [16].

$$\frac{\left(v_{OUT,p}\right)_{sensed}}{v_{ctr,p}} = H_{vo} g_{ctr} \frac{R_{mlt}}{H_i} \frac{V_{RMS}}{V_{OUT}} \frac{1}{sC_{OUT}} \tag{2.70}$$

Characteristics of the voltage loop are determined by the flow of the input power to output power. Proper design of output voltage and multiplier can be conducted with understanding of these characteristics. A detailed study on this topic is accomplished

in [14]. In this chapter only the major points of the analysis are introduced. At steady–state, the pre–regulator stage behaves like an emulated resistance because of the unity power factor behavior and non–energy storage structure of the converter. The instantaneous input power and output power of the converter can be expressed by (2.71) and (2.72). It is seen from the equations that, while the instantaneous output power is constant, the instantaneous input power is not constant.

$$p_g(t) = v_g(t) \times i_L(t) \tag{2.71}$$

$$p_{LOAD}(t) = v_{OUT}(t) \times i_{LOAD}(t) \tag{2.72}$$

Assuming a lossless system, the input power is equal to the load power. The alternation of diode rectifier output voltage, v_g, can be expressed by (2.73).

$$v_g(t) = \sqrt{2} V_{RMS} \left| \sin(\omega t) \right| \tag{2.73}$$

The converter behaves like an emulated resistance as stated previously, due to the unity input power factor characteristics of the converter. Therefore, the inductor current can be expressed by equation (2.74).

$$i_L(t) = \frac{v_g(t)}{R_e} \tag{2.74}$$

R_e, in (2.74) denotes the emulated resistance characteristics of the converter. Substituting (2.73) and (2.74) into (2.71) and averaging it over one switching period yields the behavior of load power.

$$\left\langle p_{LOAD}(t) \right\rangle_{T_S} = \frac{V^2_{RMS}}{R_e} \times \left(1 - \cos(2\omega t)\right) \tag{2.75}$$

It can be seen from (2.75) that, the instantaneous input power of the converter has an AC contribution alternating at twice line frequency and a DC contribution. Since no energy storage element is contained in the internal structure of the converter and providing a constant output power, the difference between input and output power is handled by the output storage element, which is the output capacitor. The second line harmonic ripple content of the capacitor voltage is originated from this difference. In Figure 2.17, the low frequency large signal model of the converter, which is averaged over switching frequency, is given.

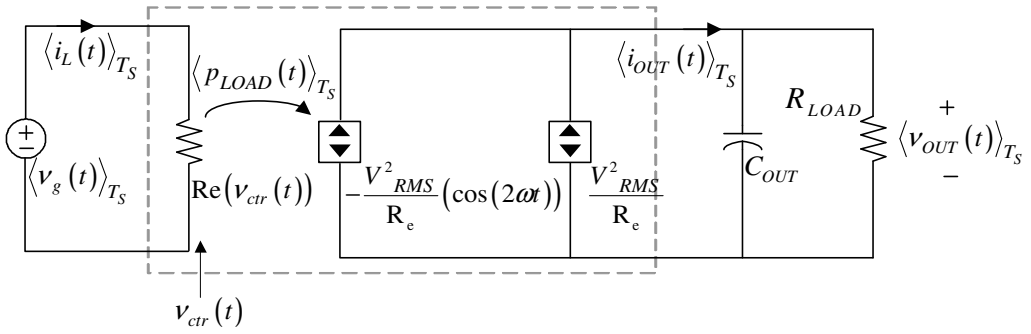

Figure 2.17 Large signal model of the converter averaged one switching period.

Second order line harmonics flow through the output stage of the converter and affect v_{ctr}, which is the amplitude reference of the inductor current. The shape of the current reference is deteriorated due to this harmonic contribution. The control bandwidth of the outer loop should be narrower than twice of the line frequency in order to avoid this unfavorable situation. The second line harmonic contribution can be removed and the model can be made LTI by averaging the derived large signal model of the converter over one half of the line period. After applying the perturbation analysis to LTI and averaging over one half of the line period model, the control voltage–to–output voltage transfer function given in (2.76) for constant power load can be obtained [14].

$$G_{vv_C} = \frac{\left(v_{OUT,p}\right)_{sensed}}{v_{ctr,p}} = \frac{P_{LOAD}}{sC_{OUT}V_{ctr}V_{OUT}} \tag{2.76}$$

The design of the multiplier output resistance and current feedback attenuation factor can be done by comparing equations (2.70) and (2.76) under the assumption that the average input power is equal to the average output power. The multiplier resistance is selected according to (2.77). $I_{L,peak}$ is the peak value of the inductor current where the instantaneous input power is at its peak magnitude.

$$R_{mlt} = \frac{H_i I_{L,peak} V^2{}_{ff}}{V_{RMS}V_{ctr}} \tag{2.77}$$

The output voltage loop is compensated by a second order compensator with two poles and a zero (2.78) to obtain good steady-state behavior. Target bandwidth for the voltage loop is one fifth of the line frequency in order to suitably suppress the second harmonic contribution. Some methods for improving the dynamic response of the outer loop are proposed in [17], [18], and [19] but this subject is out of the scope of the thesis.

$$G_{cv}(s) = \frac{\omega_{iv}}{s} \times \frac{1 + s/\omega_{zv}}{1 + s/\omega_{pv}} \tag{2.78}$$

The second line harmonic contribution present on output voltage and feedforward voltage causes a third harmonic contribution on the input line voltage and current. The voltage loop gain at the second line frequency should not be more than 2% for every 1% of third harmonic distortion allowed on the input current [20]. This means that the second harmonic ripple on the sensed output voltage should be attenuated by factor 0.02 for every 1% of third harmonic distortion allowed. Therefore at twice line frequency, voltage loop compensator should satisfy equation (2.79).

$$H_{vo}G_{vv_c}G_{cv} = 0.02k_{3rd} \tag{2.79}$$

In (2.79), k_{3rd} is the percent harmonic distortion allowed on the input line current. G_{cv} is reduced to (2.80) at twice line frequency.

$$G_{cv} = \frac{\omega_{iv}\omega_{pv}}{s\omega_{zv}} \tag{2.80}$$

The voltage loop compensator gain at twice the line frequency can be determined by substituting (2.76) and (2.80) into (2.79).

$$\frac{\omega_{iv}\omega_{pv}}{\omega_{zv}} = \frac{0.02k_{3rd}}{H_{vo}} \frac{V_{ctr}V_{OUT}2\pi f_{2LF}C_{OUT}}{P_{LOAD}} \tag{2.81}$$

The voltage loop crossover frequency is determined by equating the open loop gain to unity. This value should be suitably low in order to eliminate the effects of the second harmonic contribution.

$$f_{vxo} = \sqrt{H_{vo}\frac{P_{LOAD}}{(2\pi)^2 C_{OUT}V_{ctr}V_{OUT}}\frac{\omega_{iv}\omega_{pv}}{\omega_{zv}}} \tag{2.82}$$

The ω_{iv}/ω_{zv} term of the compensator is equated to $2\pi/\omega_{pv}$ term at crossover frequency in order to obtain 45° phase margin. The dc gain of the loop is increased by locating a zero at one tenth of the crossover frequency. The compensator transfer function which is utilized in the prototype is given in (2.83).

$$G_{vi} = \frac{10.5s + 131.9}{6.332\times10^{-3}s^2 + s} \tag{2.83}$$

Bode diagrams of compensator and open loop transfer functions are given in Figure 2.18. The loop crossover frequency is 15 Hz and the phase margin is 50° as can be

seen from Figure 2.18(b). The dynamical response of the outer loop is very poor but stability is ensured with the suitable phase margin. The performance of the controller is verified by means of computer simulations is further sections.

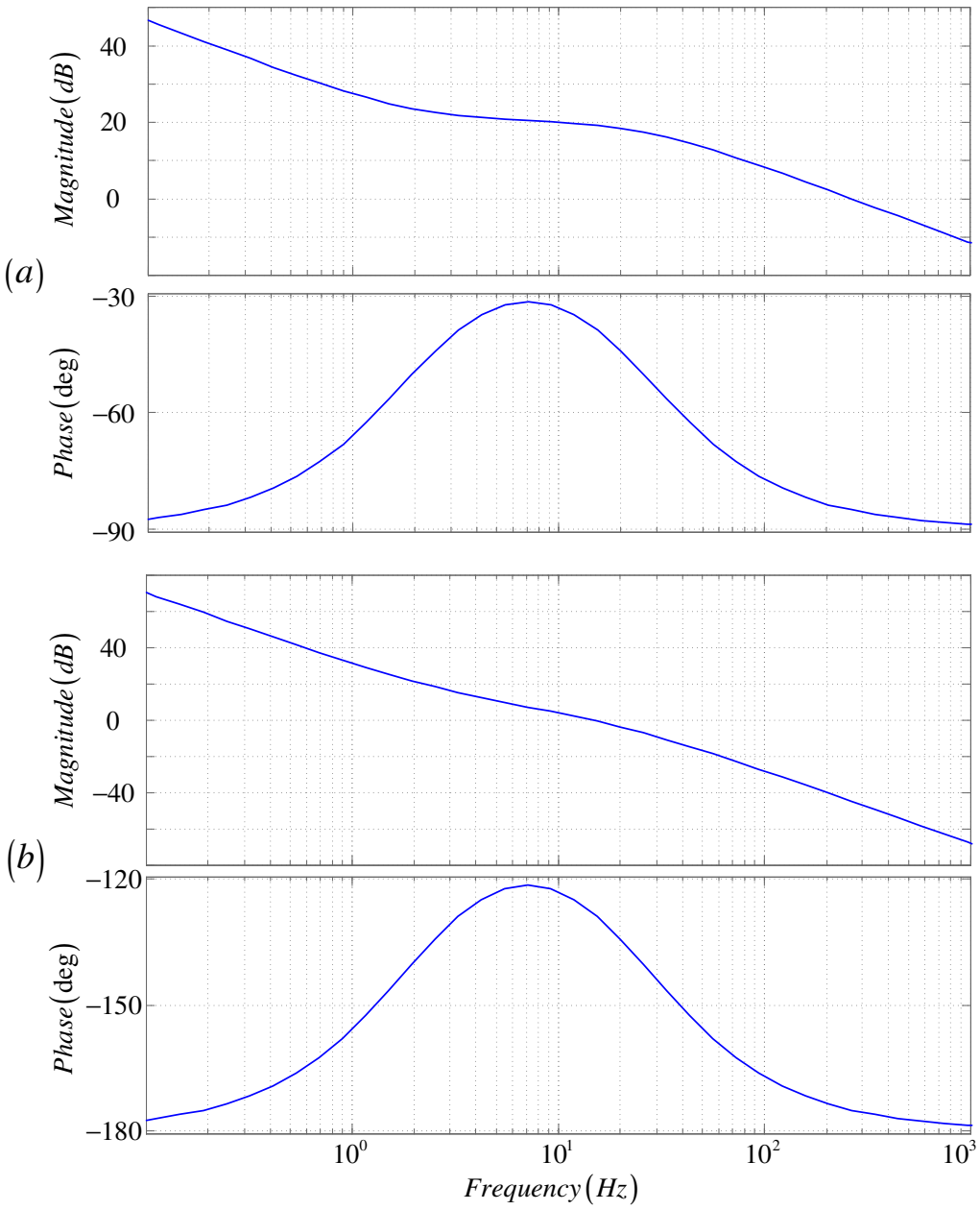

Figure 2.18 Voltage loop Bode plots, (a) loop compensator, (b) open loop response.

2.5 Design Of the Two–Phase Interleaved ACM Controlled PFC

A laboratory prototype of the two–phase interleaved ACM controlled PFC is manufactured for the purpose of investigating characteristics of the converter in a real system, verifying the model, and examining the controller performance. The design of the system is separated into two parts: power stage design and controller design. To establish modularity and to ease the maintenance, the controller and power stages are built on separate printed circuit boards (PCB). In this section, design of the system will be explained.

2.5.1 Design Of The Power Stage

The power stage consists of a diode bridge rectifier, input and output capacitors, inductors, power switching semiconductors, current and voltage sensing components and soft starting circuitry. The design is based on 5kW output power rating with 90% efficiency. The experiments are performed at maximum 3 kW output power because of some problems related to EMI compliance of the prototype system. Experiments are conducted up to 3 kW load and the experimental data is taken under 1.25kW and 2.5kW loading. Basic design specifications are given in Table 2.2. The power stage components are chosen by considering these design specifications. The rated output power is desired to be 5kW because this prototype will be the pre–regulator of the 5kW FB–PS–ZVS DC/DC converter. The output voltage is specified as 400V for the same manner, as it is the required input voltage level for the output power stage. The switching frequency is 40 kHz, because the IGBTs utilized in the system allow maximum 50 kHz switching frequency. To decrease switching losses a 10 kHz safety margin is added. In the future, this value may be reduced to 30 kHz to reach 5kW output power. The maximum inductor ripple current is desired to be 10% of the peak current at rated power in order to minimize conducted and radiated EMI while keeping the size of the inductors feasible. The output voltage second harmonic fluctuation is specified to be kept lower than 2.5% of the average output voltage.

Table 2.2 Basic design specifications of the two–phase interleaved ACM controlled PFC prototype

Output Power	5000	W
Minimum Input Line Voltage	180	V_{rms}
Line Frequency	50	Hz
Average Output Voltage	390	V
Switching Frequency	40	kHz
Efficiency	90	%
Maximum Inductor Ripple Current	10	%
Maximum Output Voltage 2^{nd} Harmonic Fluctuation	2.5	%

In order to reach design specifications for the inductor current ripple at rated load, (2.84) can be used for determining the inductance value of the boost inductors.

$$L = \frac{\Delta V_L \times \Delta t}{\Delta i_L} = \frac{\Delta V_L \times D}{\Delta i_L \times f_{sw}} \tag{2.84}$$

In (2.84), ΔV_L denotes the maximum inductor voltage, f_{sw} denotes the switching frequency, and Δi_L denotes the maximum inductor current ripple specified. The maximum inductor current occurs when the voltage difference between the inductor terminals are maximum at the rated inductor current, therefore the inductor voltage is the peak value of minimum input line voltage specified. Peak input current is calculated from (2.85) and the peak inductor current is half of this value with the assumption of equally shared current between to power stages.

$$\left(I_{IN,AC}\right)_{peak} = \sqrt{2} \times \frac{P_g}{\eta \times V_{RMS}} = 48A \tag{2.85}$$

The specified maximum input current ripple is 10% of this value, 2.5A, as stated in Table 2.2. The duty cycle at the peak input voltage is calculated by (2.86).

$$D = \frac{V_{OUT} - \sqrt{2}V_{RMS}}{V_{OUT}} = 0.36 \tag{2.86}$$

The inductor value is calculated by substituting the values calculated by (2.85) and (2.86) into (2.84). The inductor value satisfying the target maximum current ripple is calculated as 1mH this value is utilized in the system.

In the voltage loop compensator design section, the second line harmonic contribution to the output voltage is explained. The output capacitor should be designed in order to keep that contribution in a reasonable range. For the design this range is specified as 2.5% of average value of the output voltage at full load. The magnitude of the maximum second harmonic component can be calculated by solving (2.76) for twice the line frequency. Then the output capacitor value can be found by solving (2.87) for the given design specifications.

$$C_{OUT} = \frac{P_{LOAD}}{V_{OUT} \times 2\pi f_{LINE2} \times V_{OUT2,peak}} = 2.5mF \tag{2.87}$$

In (2.87), $V_{OUT2,peak}$ denotes the maximum peak–to–peak amplitude of the second harmonic AC content of output voltage and f_{LINE2} is the second line harmonic frequency.

The switching components are chosen by considering their breakdown voltage and peak current ratings, turn–on and turn–off times, package type, and of course availability. IGBT is utilized for the controlled switching device, because as power level reaches kW levels, IGBT becomes superior to MOSFET because of its high

voltage and current handling capabilities. The maximum current flow through the IGBT is approximately 25A as calculated previously and maximum collector–to–emitter voltage applied is the output voltage of 390V. For the design there should be some additional safety regions for current and voltage ratings of the device. The reverse recovery current of the boost diode increases the current flown through the IGBT during the turn–on transients. Therefore, an IGBT with a current rating greater than 30A should be selected. The leakage inductance on the current trace caused by the PCB non–idealities and current transformer causes ringing on collector–to–emitter voltage of the IGBT. The collector–to–emitter breakdown voltage of the IGBT should be greater than the output voltage of the converter. Also the turn–on and turn off times should be as fast as possible to decrease switching losses. In the design, the IGBT manufactured by Fairchild Semiconductors, with the part number HGTG30N60B3D is utilized. The major electrical characteristics of the device are given in Table 2.3. More detailed information can be obtained from [21].

Table 2.3 The electrical characteristics of HGTG30N60B3D

Collector–To–Emitter Breakdown Voltage	BV_{CES}	600	V
Continuous Collector Current (@ 25℃)	I_C	60	A
Continuous Gate–To–Emitter Voltage	V_{GE}	±20	V
Turn–On Energy	E_{ON}	1300	μJ
Turn–Of Energy	E_{OFF}	1600	μJ
Operating Frequency (@ I_C = 20A, V_{GE} = 15V And T_C = 75℃)	F_{OPR}	40	kHz

The reverse recovery time of the diode is the key design parameter for selecting the boost diode, because the reverse recovery current is directly proportional to reverse recovery time. The diode reverse recovery current, and with it the switching losses decrease with decreasing reverse recovery time. The diode with manufacturer part

number, FFH30S60S, which is manufactured by Fairchild Semiconductors with "Stealth 2", is chosen and utilized. The major electrical characteristics of the device are given in Table 2.4 More detailed information can be obtained from [22].

Table 2.4 Electrical characteristics of FFH30S60S

Peak Repetitive Reverse Voltage	V_{RRM}	600	V
Average Rectified Forward Current	$I_{F(AV)}$	30	A
Typical Forward Voltage	V_F	2.1	V
Reverse Recovery Time ($I_{F(AV)}$ = 30A, V_R = 390V, T_C = 125ºC)	t_{rr}	75	ns

A film capacitor is placed at the output of the diode bridge rectifier in order to bypass the high frequency components of the input current. The capacitance of the filter capacitor should be high enough to bypass switching ripples and low enough to keep the sinusoidal shape of the input current ripple. In the design the capacitance is chosen as 2μF. Metallized polypropylene film (MKP) capacitors are utilized for their high ripple current handling capacity.

The two inductor currents, diode rectifier output voltage and output voltage should be sensed for the feedback control purpose. Voltages are sensed by simple resistor dividers. Sensing the inductor current is an involved task. For low power systems, a simple sense resistor with low resistance value can be utilized, but for high power applications this method is not applicable due to high power consumption on the sense resistor. In conventional power converters, the inductor current is sensed directly by utilizing Hall Effect sensors, but this method is not preferable due to its complexity and high cost. A low cost and less complicated solution is utilizing current transformers (CT). Two CTs should be connected serially to boost diode and IGBT because CTs cannot measure dc current. The CT on the IGBT leg senses upslope of the inductor current and the CT on the diode leg of the converter senses

the down slope of the inductor current. The sensed inductor current is summation of these two signals. For a two–phase interleaved system, there are two IGBTs and two boost diodes in the power circuitry therefore; there should be four CTs in the system, resulting in increased cost and complexity. The control chip utilized in the circuit has a superior feature: current synthesizing. Only IGBT currents are sensed by CTs and current synthesizer circuitry predicts the downslope to generate the inductor current. Comprehensive information about current synthesizing concept is applicable in [20], [23]. the CTs should handle the IGBT current and should not saturate at the switching frequency. For the design, a CT with 50 kHz bandwidth is chosen and a flux resetting circuitry consisting of a resistor and a capacitor is connected to output of the secondary windings in order to prevent transformer saturation. The primary side inductance of the CT should be as small as possible because it is connected serially to IGBT, and high inductance in this trace causes excessive stress on the IGBT. The inductance is mainly determined by the winding turn number of the primary side. The power losses caused by sense resistor would be high and the magnetizing inductance can be inadequate when the primary side turn number is low while, high turns number results in high leakage inductance. In the design the current sense transformer manufactured by Coilcraft Company with part number CS4200V–01L is utilized. Characteristics of the current transformer are given in Table 2.5. The current sense circuit is given in Figure 2.19. The switch current is attenuated with a factor equal to turns ratio of the converter and converted to voltage by sense resistor.

Table 2.5 Characteristics of the current sense transformer (CT)

Turns Ratio (N_{SEC}/N_{PRI})	200
Frequency Range	1 – 50 (kHz)
Current Range	5mA – 35A

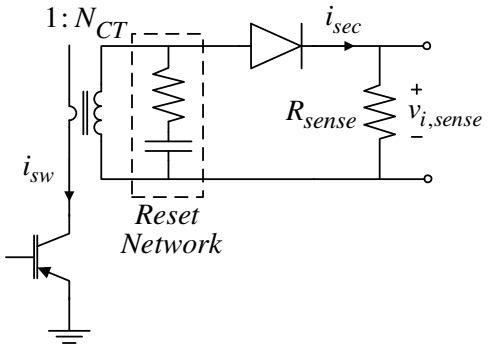

Figure 2.19 Switch current measuring circuitry.

The circuit is built up on a two–sided PCB. The IGBTs and boost diodes are located on the bottom side of the PCB. This is because; the heatsink is located under the board for the sake of optimizing the volume of the converter. The metallic heat transfer surfaces of switching devices are pressed on this heatsink. Heat transfer from the heatsink to ambient is forced by an AC fan which blows air directly on to heatsink. Related board PCB layouts are provided in Appedix A, circuit schematics are provided in Appendix B, and photographs of input and output stage are provided in Appendix C.

2.5.2 Design Of The Control Stage

System control and protection is provided with the control board. This board is attached to the power board with mated connectors. PFC controller IC, IGBT drivers and over current protection circuitry are included in the board.

2.5.2.1 PFC Controller

A newly released product of Texas Instruments, UCC28070, is utilized as the PFC controller. UCC28070 is continuous conduction mode PFC controller IC. It has some

distinct features over conventional commercial PFC controller ICs. The main distinct feature of the chip is there are two pulse width modulators integrated into the chip which operate 180° out of phase, therefore; interleaving action can be performed. There are two separate current error amplifiers for separate interleaving legs of the converter. The chip also has some other innovative features including quantized voltage feedforward and inductor current synthesizer. Comprehensive information about the monolithic chip is available in [20].

The control strategy of the controller is average current mode control. The voltage error amplifier and the multiplier are common for two legs. The multiplier output is the current reference of both current error amplifiers. Currents of both inductors are measured separately and both voltage error amplifier and current error amplifiers are transconductance type operational amplifiers. Compensator transfer functions are achieved by external capacitor and resistor networks connected to error amplifiers. The general structure of the error amplifiers are shown in Figure 2.20.

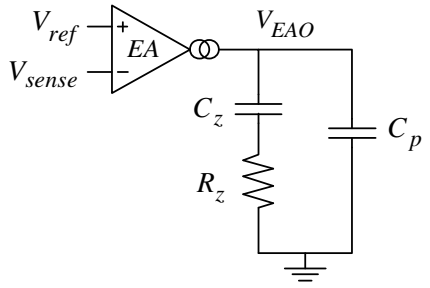

Figure 2.20 Transconductance type error amplifier structure.

The input to output relationship of a transconductance type operational amplifier is given in (2.88). In the equation, g_{mv} denotes transconductance constant of the amplifier and Z_{EAO} denotes output impedance. Signals at plus and minus inputs of the amplifier are subtracted to generate an error signal. This error signal is amplified with transconductance constant and output impedance.

$$V_{EAO} = g_{mv} \times \left(V_{ref} - V_{sense} \right) \times Z_{EAO} \tag{2.88}$$

The output impedance is determined by capacitors and resistors connected to the outside of the amplifier. The gain of the amplifier is given in (2.89).

$$g_{mv} Z_{EAO} = \frac{1 + sR_z C_z}{s^2 R_z C_z C_p + s(C_z + C_p)} \simeq \frac{1}{sC_z} \frac{1 + sR_z C_z}{1 + sR_z C_p} = \frac{\omega_i}{s} \frac{\left(1 + \frac{\omega_z}{s} \right)}{\left(1 + \frac{\omega_p}{s} \right)} \tag{2.89}$$

Therefore the low frequency pole of the compensator is determined by C_z, the high frequency pole is determined by R_z and C_p, and zero is determined by R_z and C_z .

The output voltage is sensed by a simple resistor divider network with an attenuation factor of 0.0075. This voltage is compared with a 3V reference voltage and the voltage error is amplified with voltage error amplifier. Switch currents are sensed with sensed circuitry given in Figure 2.19 and compared with multiplier output. Current errors are amplified with current error amplifiers. The capacitor and resistor values of the impedance networks connected at error amplifier outputs are given in Table 2.6. The subscript "c" is used for the parameters involved current loop and the subscript "v" is used for the parameters involved voltage loop. Same circuit components are utilized for both current error amplifiers.

Table 2.6 Gain resistors and capacitors of voltage and current error amplifiers.

R_{zv}	180	kΩ
C_{zv}	470	nF
C_{pv}	47	nF
R_{zc}	12	kΩ
C_{zc}	6.8	nF
C_{pc}	330	pF

2.5.2.2 Gate Drivers

The switches utilized in high power applications have large gate charge requirement, therefore the gate drive output of the control IC is inadequate to charge and discharge the gate capacitor of the semiconductor switches. In the design, two gate driver ICs are utilized for providing proper driving to IGBTs in order to provide safe, efficient, and fast switching. The gate driver ICs are produced by Avago Technologies with part number HCPL–316J. The input PWM control signal and output gate drive signals are optically isolated and the IC can provide gate current up to 2.5A. The IC also has a desaturation protection feature. The collector voltage of the IGBT is measured and when this voltage become greater than 7V, the gate driver outputs are turned off.

There is an over current protection circuitry on the control board. The sensed switch current is compared with a reference signal. If the current is above the reference, gate driver outputs are turned off to protect switches. Schematics, PCB layout and the photographs of the controller board are applicable in Appendix A.

2.6 Simulation Results of The Two-phase Interleaved ACM Controlled PFC

In this section, the power stage and controller performance of the PFC, which utilizes the design parameters applied to the prototype converter, is investigated by means of computer simulations. The computer simulations are conducted utilizing the SIMPLORER software package developed by Ansoft Cooperation. Power stage components such as IGBT switches, diodes, magnetic components etc. are modeled in the program and control stage is constructed by programming equation blocks and joint utilization of continuous time blocks such as transfer functions, signal generators etc. Simulation results can be displayed on graphic view and can be mathematically evaluated by analysis tools. For the simulations of the two–phase interleaved power factor corrector, device level modeled semiconductors are utilized for semiconductor power components and standard modeled passive components are

utilized for inductors, capacitors and resistors. Error amplifiers and multiplier of the control block are coded in equation editors, which perform basic mathematical and logical operations. Controller transfer functions are coded into s–domain transfer function blocks. All continuous blocks conduct their computations with simulation step size 100ns to simulate analog characteristics of the controller realistically. Component and controller parameters are the same that utilized laboratory prototype. The simulation parameters are given in Table 2.7 and the simulation diagram is shown in Figure 2.21.

Table 2.7 Interleaved PFC simulation parameters

Simulation Parameters			
Parameter Description	Abbreviation	Value	Unit
Simulation Step Size	h	100	nsec
Simulation Run Time	T_{END}	100	msec
Integration Formula		Trapezoidal	
Power Circuit Parameters			
Input line voltage	$V_{IN,RMS}$	220	V
Leading Leg Boost Inductor	L_{BOOST1}	1	mH
Lagging Leg Boost Inductor	L_{BOOST2}	1	mH
Input Capacitor	C_{IN}	2	μF
Output Capacitor 1	$C_{OUT,1}$	1	μF
Output Capacitor 2	C_{OUT2}	2.4	mF
Capacitor equivalent serial resistance	R_{ESR}	0.1	Ω
Control Circuit Parameters			
Input Voltage Scaling Resistor 1	$R_{AC,SENSE1}$	3000	kΩ
Input Voltage Scaling Resistor 2	$R_{AC,SENSE2}$	23	kΩ
Output Voltage Scaling Resistor 1	$R_{OUT,SENSE1}$	3000	kΩ
Output Voltage Scaling Resistor 2	$R_{OUT,SENSE2}$	23	kΩ
Output Voltage Reference	$V_{OUT,REF}$	3	kΩ

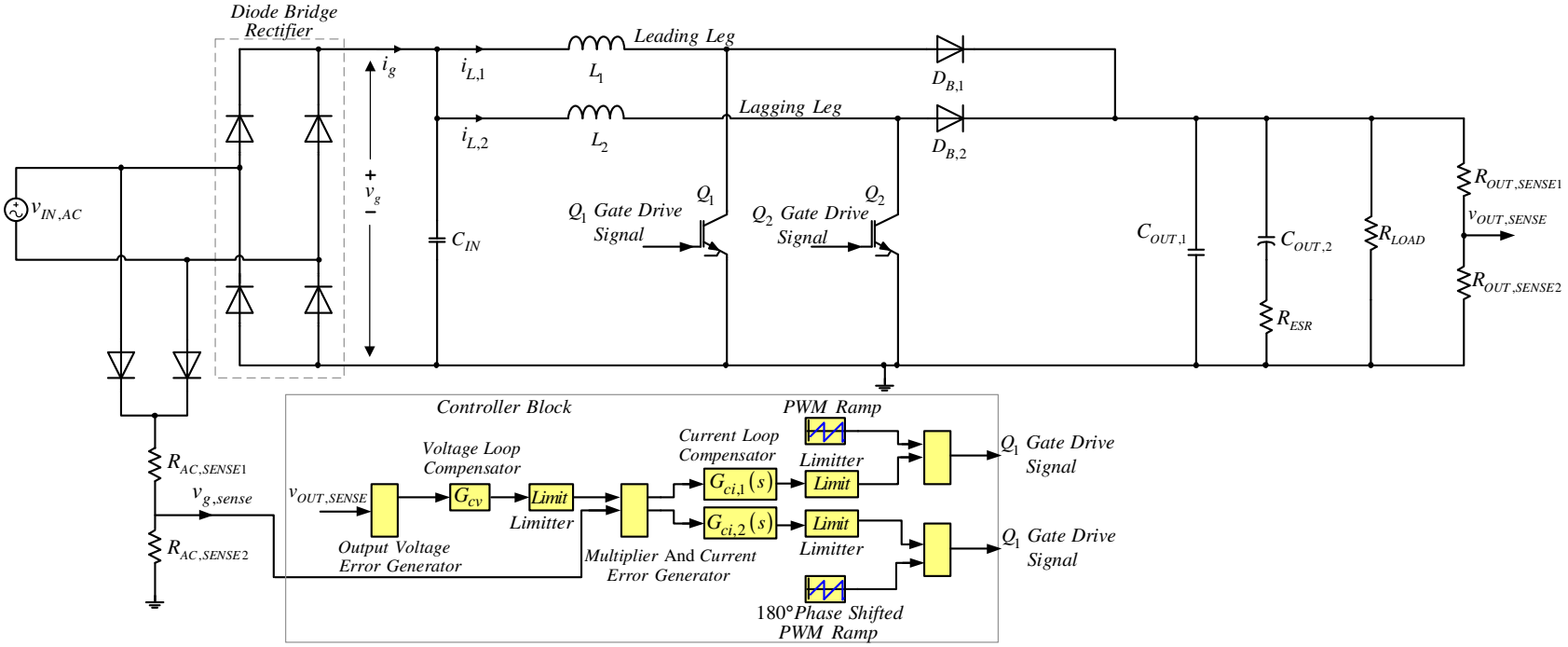

Figure 2.21 Simplorer simulation diagram of the two–phase interleaved ACM controlled PFC.

Voltage and current loop compensator transfer functions are the values which were derived in the compensator design section. G_{ci} is given by (2.67) and G_{vi} is given by (2.83).

2.6.1 Simulation Results Of The Two–Phase Interleaved ACM Controlled PFC

In this section, the circuit operation and performance is investigated by means of computer simulations based on the model derived in the previous section. Simulations are conducted under half and full load conditions to demonstrate the converter performance under various load conditions. Simulation results are classified in three groups: external characteristics, internal characteristics and control characteristics. External characteristics consist of the line voltage, line current and output voltage while internal characteristics consist of the inductor and switching semiconductor currents. The controller performance is evaluated by investigating the dynamic response and reference following capability of the system.

2.6.1.1 Simulation Results at 1.25 kW Output Power

For the present physical power limitation of the circuit being 3kW, the experiments performed for the purpose of passing beyond this power limit resulted in IGBT failure in several trials. Therefore, in the thesis power rating of the circuit is determined as 2.5kW. The basic waveforms determining the characteristics and behavior of the circuit are given in this section at the half output power. In Figure 2.22, the input line voltage, input line current waveform, and output voltage waveforms are given. From Figure 2.22(a) it can be observed that, the input current tracks the input voltage despite some deviation at zero transitions. Since at zero transitions the duty cycle has tendency of converging to unity, this area is out of controllable range. The output voltage is regulated at 390V and it fluctuates at twice of the line frequency with amplitude of 5 volts. The reason of this fluctuation is

explained in detail in voltage control loop section. This fluctuation cannot be totally eliminated, but its amount can be reduced by utilization of big hold up capacitor at the output. The unfavorable effect of this fluctuation on current reference signal can be eliminated by reducing the bandwidth of the output voltage loop down to one fifth of the line frequency as is done in this design. The drawback of reducing the bandwidth is the deteriorated dynamic response of the output voltage.

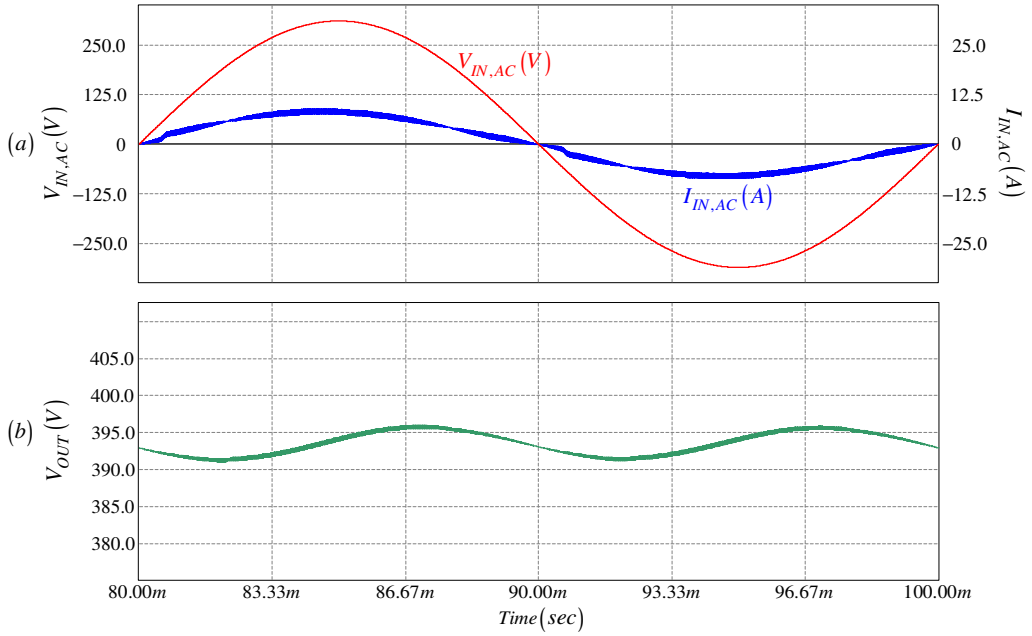

Figure 2.22 The two–phase interleaved ACM controlled PFC external characteristic waveforms at 1.25kW output power: (a) Line voltage (red) and line current (blue), (b) output voltage.

In Figure 2.23, the internal characteristics of the converter are shown. As it is seen in Figure 2.23(a), (b) and (c), the diode rectifier current is equally shared between two legs of the converter. The maximum inductor ripple current is approximately 1.7 A. The maximum input current ripple is reduced approximately to 1.3 A. Investigating Figure 2.23(c), it is seen that the input ripple current varies with the phase angle. This is because, as the input voltage increases from zero to its peak value, the duty

cycle decreases. The ripple is theoretically zero when the duty cycle is 0.5 and it increases when duty cycle deviates from 0.5 as explained in section 2.2.1. The duty cycle is 0.5 when the input voltage is 200V and it is 0.22 at the voltage peak. Therefore, ripple decreases as input voltage increases towards 200V and decreases as it increases towards its peak value.

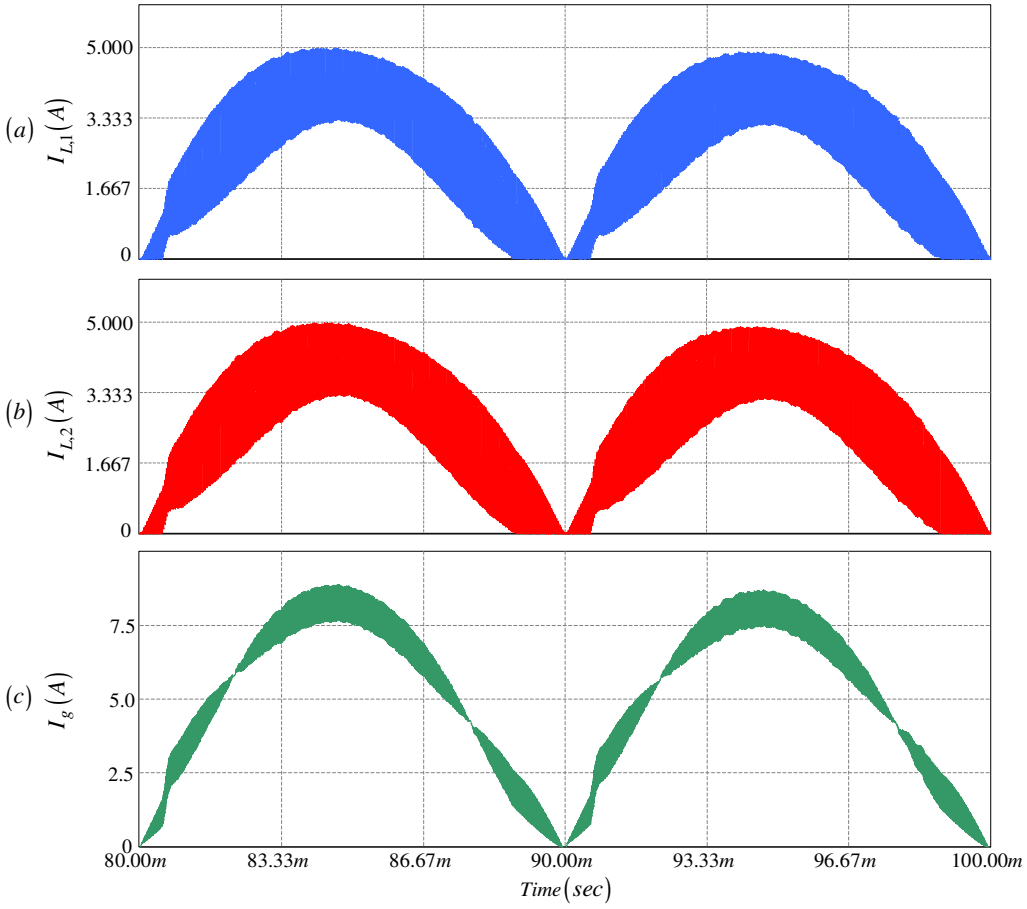

Figure 2.23 The two–phase interleaved ACM controlled PFC internal characteristic waveforms at 1.25kW output power: (a) Leading leg boost inductor current, (b) lagging leg boost inductor current, (c) diode rectifier output current.

The detailed inductor current ripples at the peak inductor currents are shown in Figure 2.24(a) and (b). Ripples are out of phase with half of the switching period. From Figure 2.24(c) it is seen that overall ripple amplitude is reduced and ripple frequency is doubled. Illustrating the benefit of interleaving, these two results give opportunity to utilization of smaller input EMI filter and lower harmonic distortion on the input current.

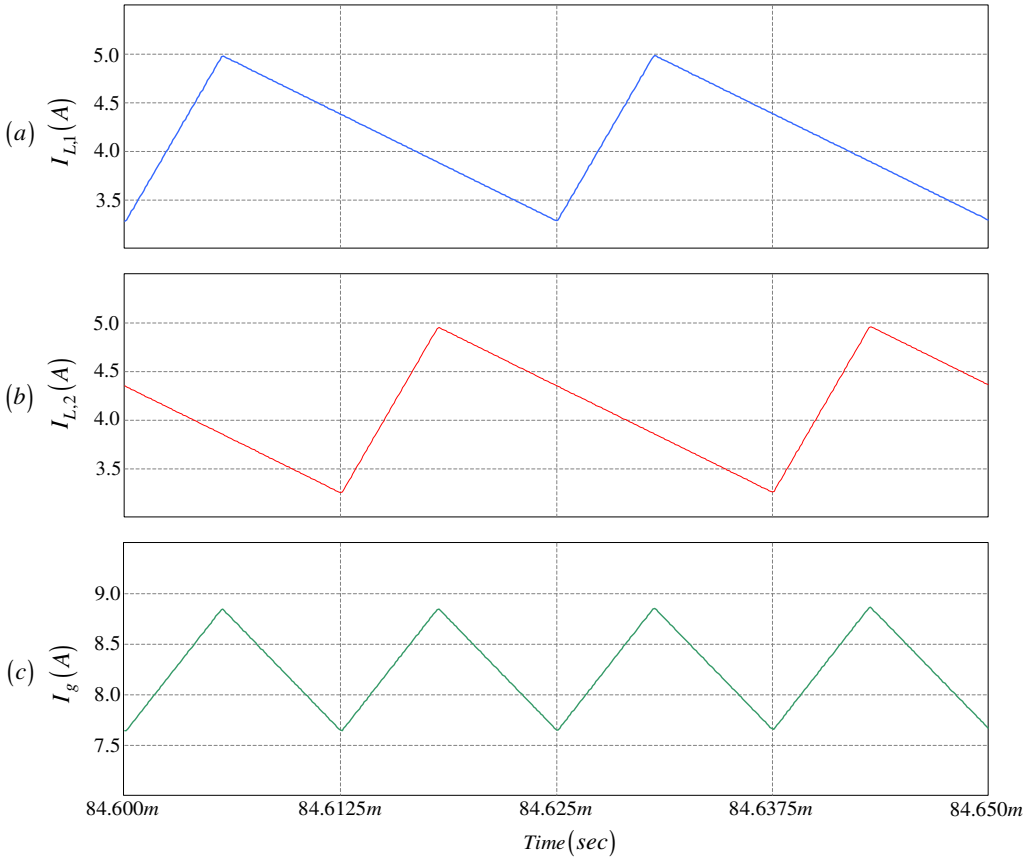

Figure 2.24(a) Leading leg inductor current ripple at the peak inductor current, (b) lagging leg inductor current ripple at the peak inductor current, (c) diode rectifier output current ripple at the peak current.

The peak switching semiconductor device currents are shown in Figure 2.25(a) and (b). The current transferred from the input to the output is shared with the devices in two legs, therefore current stress on the devices are reduced. This results in reduced switching and conduction losses on the devices and gives opportunity to utilization of smaller package semiconductor devices and smaller heatsink.

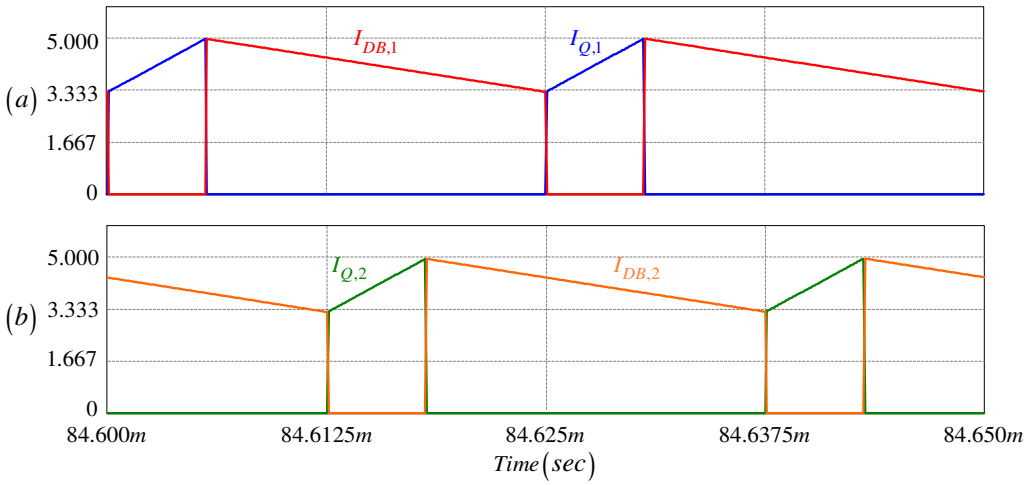

Figure 2.25 The two–phase interleaved ACM controlled PFC switching component current waveforms at 1.25kW output power: (a) Leading leg IGBT peak current (blue) and diode current (red), (b) lagging leg IGBT peak current (green) and diode current (orange).

In Figure 2.26, reference tracking ability of the inductor current controller is investigated. The waveform indicated with red curve is the output voltage of multiplier, which is the inductor current reference. The green waveform is the inductor current of one of the legs. Since the inductor current is sensed via a current transformer and sense resistor, the reference signal is proportional to the attenuation ratio of the inductor current. This ratio is 30/200 for the design. Since the operation principle of ACM control is to provide average value of the inductor current to track current reference, the inductor current is averaged in the current loop with the bandwidth of the current loop at one tenth of the switching frequency. From the

figure, it seen that inductor current tracks the reference voltage with high accuracy and also it is seen that reference signal takes the shape of the diode rectifier output voltage very well. This indicates that the output voltage loop compensator is designed with sufficient accuracy and bandwidth. The performance of the controller can be evaluated by these waveforms.

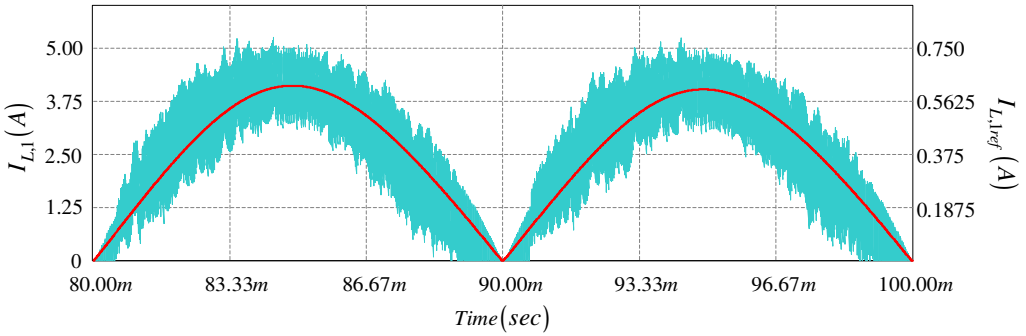

Figure 2.26 Reference tracking ability of the inductor current regulator: the leading leg inductor current (green) and the multiplier output reference voltage (red).

The quality of the input power can be obtained by investigating harmonic contents of the input current, input power factor, and total harmonic distortion (THD). These computations are performed by the "day post processor" tool of the simulation program. The harmonic contents of the input current can be investigated from Figure 2.27. There exist harmonic contents up to seventh harmonic of the line frequency. The significant content is the fundamental frequency content. Note that the switching frequency ripple current is absorbed by the high frequency capacitor placed at the rectifier output terminals and the line current harmonic spectrum is practically free of switching ripple and mainly consists of low frequency harmonics which have been discussed in here.

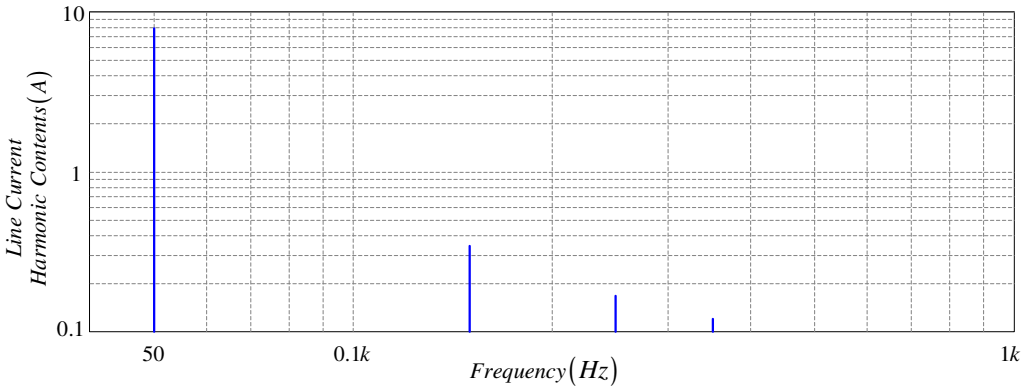

Figure 2.27 Harmonic contents of the input line current.

The real power, active power, and reactive power supplied from input is computed by Day Post Processor, and by using these parameters input power factor is calculated. Results of these computations are given in Table 2.8. The input power factor is near unity as can be observed from the table. The THD of the input current is calculated by performing Fourier transform by Day Post Processor. The design goal THD is smaller than 5%, but for rated power (5kW). Since these simulations are conducted under 1.25kW load conditions, results are deviated from the design goals.

Table 2.8 Power quality performance indicators of the two–phase interleaved ACM controlled PFC for 1.25kW.

Real Power	1240.4	VAR
Active Power	1231.5	W
Reactive Power	147.6	VA
Cos(θ)	0.993	
THD	7.454	%

2.6.1.2 Simulation Results at 2.5 kW Output Power

To investigate the circuit performance on various power levels, same simulations are performed under 2.5kW output power. The power quality parameters are expected to be improved, because signal–to–noise ratio of sensed inductor currents is improved and all compensators are designed for full load power. In Figure 2.28, waveforms of the input line voltage, line current, and output voltage are given. From Figure 2.28 (a) it is observed that line current tracks line voltage in more accurate way than former simulation result. The average output voltage is regulated at 390V and the fluctuation on output voltage has amplitude of 10 V peak–to–peak. The magnitude of the fluctuation increases as power increases, as expected.

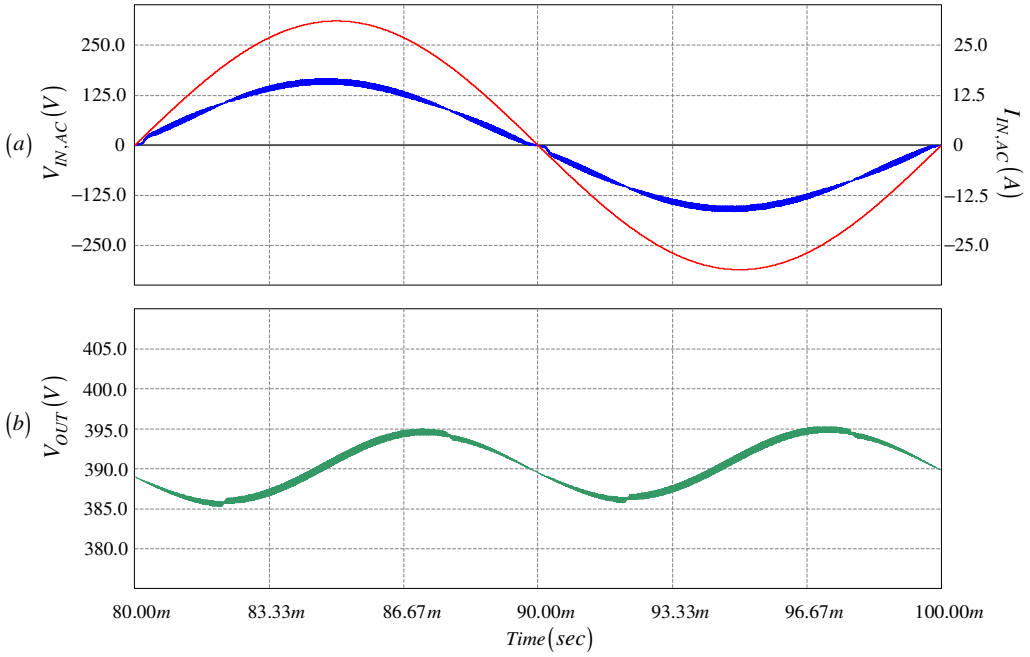

Figure 2.28 The two–phase interleaved ACM controlled PFC external characteristic waveforms at 2.5kW output power: (a) Line voltage (red) and line current (blue), (b) output voltage.

The inductor currents and diode rectifier output current are given in Figure 2.29. The diode rectifier output current is shared equally between two legs of the converter due to the symmetry of the circuit. The detailed inductor current ripples at the peak inductor currents are shown in Figure 2.30(a) and (b). The peak inductor current ripple amplitudes are approximately 1.8A and peak input current ripple is reduced to approximately 1.2A. It is observed that the amount of inductor current ripple and input current ripple do not change dramatically with increased power when the former and latter simulation waveforms of the inductor peak current ripples are compared. In Figure 2.31, the peak currents of semiconductor switching devices of both legs under 2.5kW loading are given. The amplitude of currents flown these devices are increased with increasing power. In Figure 2.32, the reference tracking ability of the inductor current is investigated. From the figure, it is seen that the reference voltage is tracked by the inductor current with high accuracy. The satisfactory performance of the ACM current controller has been proven by these waveforms. The harmonic contents of the input current can be investigated from Figure 2.33. There exist only fundamental and third harmonic contents on the line current. The significant content is the fundamental frequency content. It is seen that quality of input line current is significantly improved as the power increases by comparing Figure 2.27 and Figure 2.33.

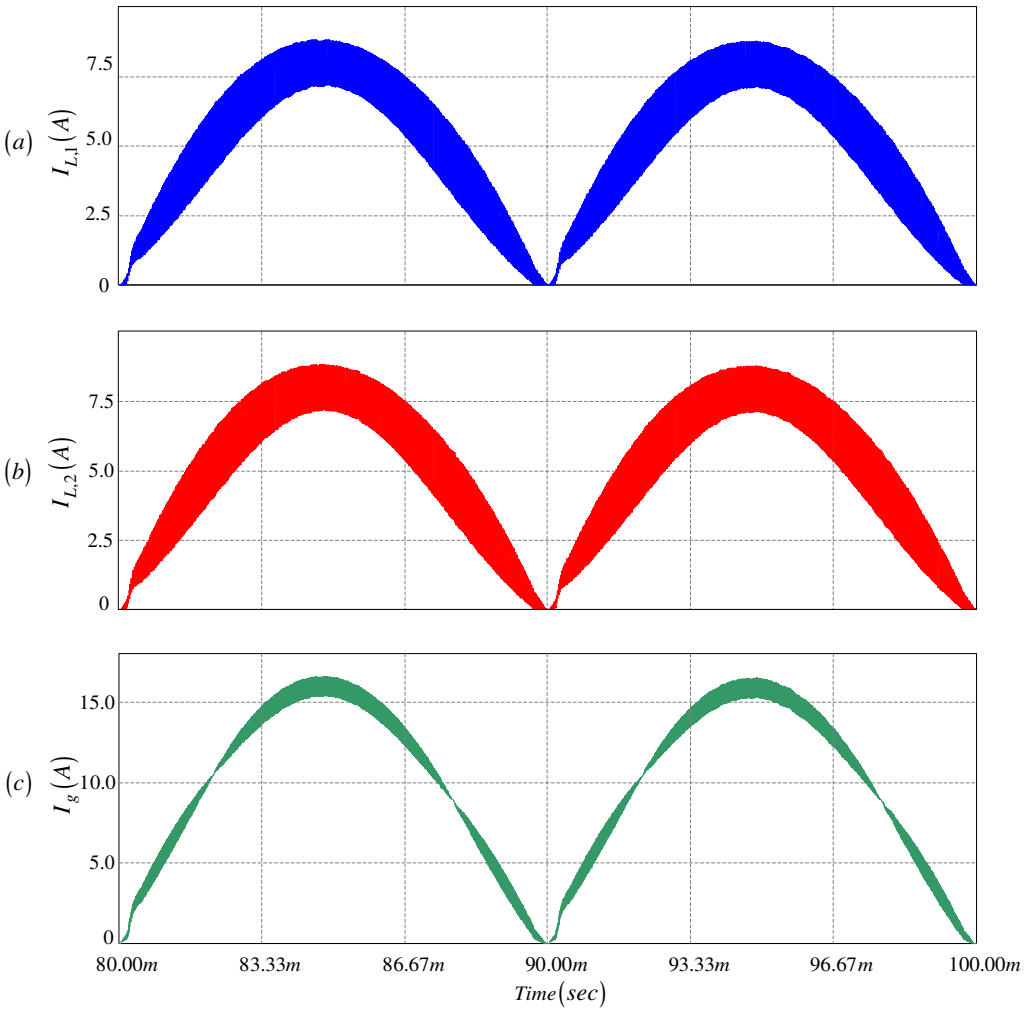

Figure 2.29 The two–phase interleaved ACM controlled PFC internal characteristic waveforms at 2.5kW output power: (a) Leading leg inductor current, (b) lagging leg inductor current, (c) diode rectifier output current.

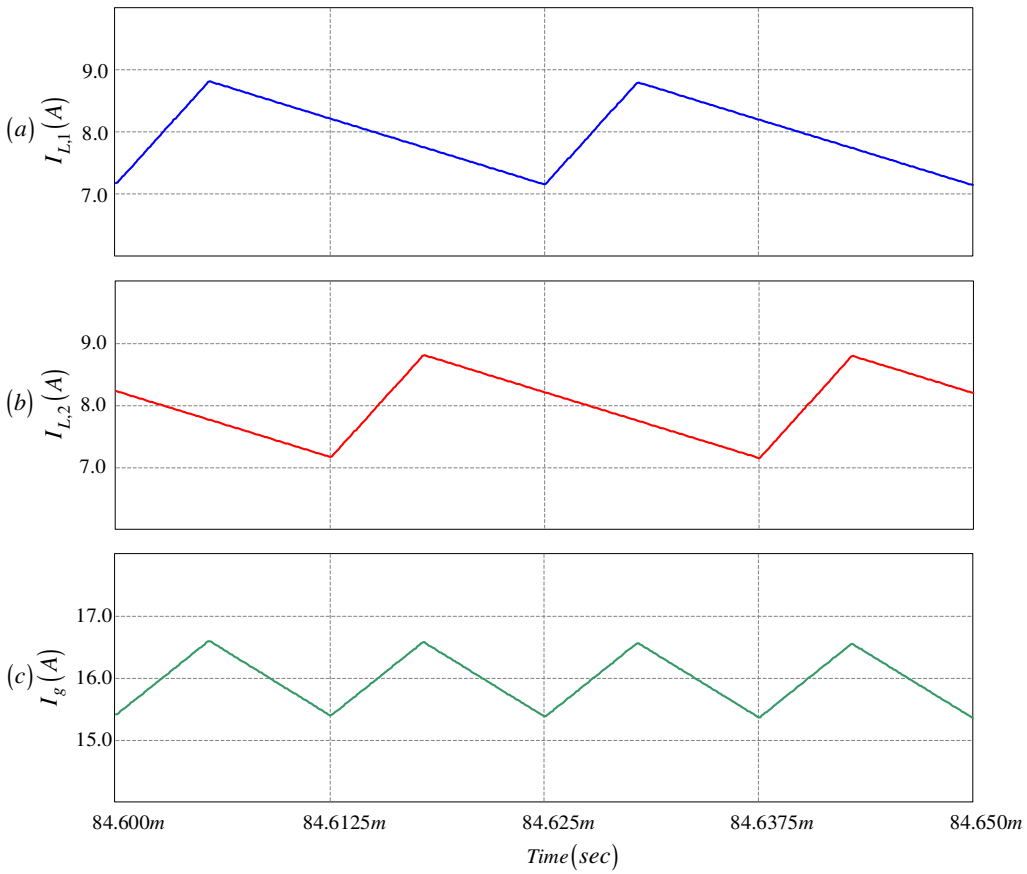

Figure 2.30(a) Leading leg inductor current ripple at the peak inductor current, (b) lagging leg inductor current ripple at the peak inductor current, (c) diode rectifier output current ripple at the peak current at 2.5kW output power.

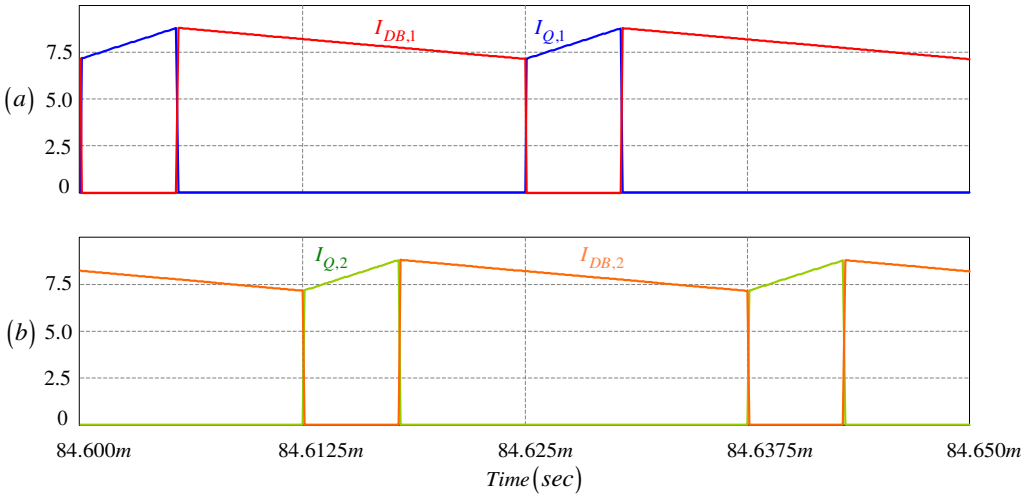

Figure 2.31 The two–phase interleaved ACM controlled PFC switching component current waveforms at 2.5kW output power: (a) Leading leg IGBT peak current (blue) and diode current (red), (b) lagging leg IGBT peak current (green) and diode current (orange).

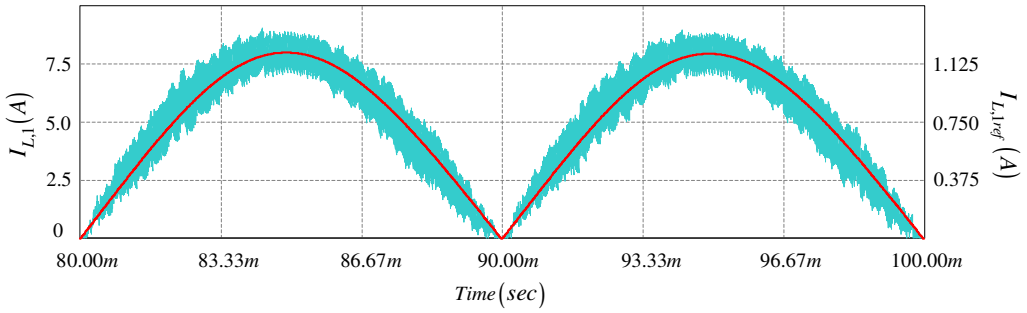

Figure 2.32 Reference tracking ability of the inductor current controller. Leading leg inductor current (green) and the multiplier output reference voltage (red).

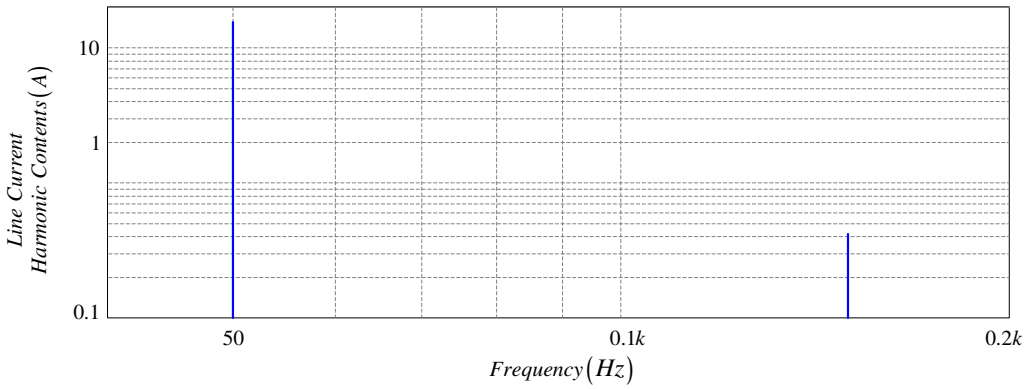

Figure 2.33 Harmonic contents of the input line current.

The indicating parameters of input power quality are given in Table 2.9. The input power factor is near unity as can be observed from the table. The THD of the input current is calculated by performing Fourier transform by Day Post Processor. It is observed that the THD reduced significantly with increasing power by comparing Table 2.8 and Table 2.9.

Table 2.9 Power quality parameters of the two–phase interleaved ACM controlled PFC at 2.5kW

Real Power	2427.7	VAR
Active Power	2421.7	W
Reactive Power	171.7	VA
Cos(θ)	0.997	
THD	3.997	%

2.6.1.3 The Dynamic Response of the Converter

To observe the dynamic response of the controller, the response of the controlled system variables to step varying load power is investigated. At steady-state, the output load is 1.25kW for t<100msec. At t=100msec the output load power is increased to 2.5kW rapidly. There exists a sag on the output voltage due to this loading. The output voltage reaches its regulated average steady-state value in several fundamental cycles because of the low bandwidth of the output voltage control loop. The inductor current stabilizes faster than the output voltage. At t=200msec, the output load is again reduced to 1.25kW rapidly. In this case, the output voltage increases and overshoots temporarily until it stabilizes to its new steady-state value in several fundamental cycles. In Figure 2.34, the dynamic response of the controller by means of responses to rapid loading of output voltage and inductor current is illustrated.

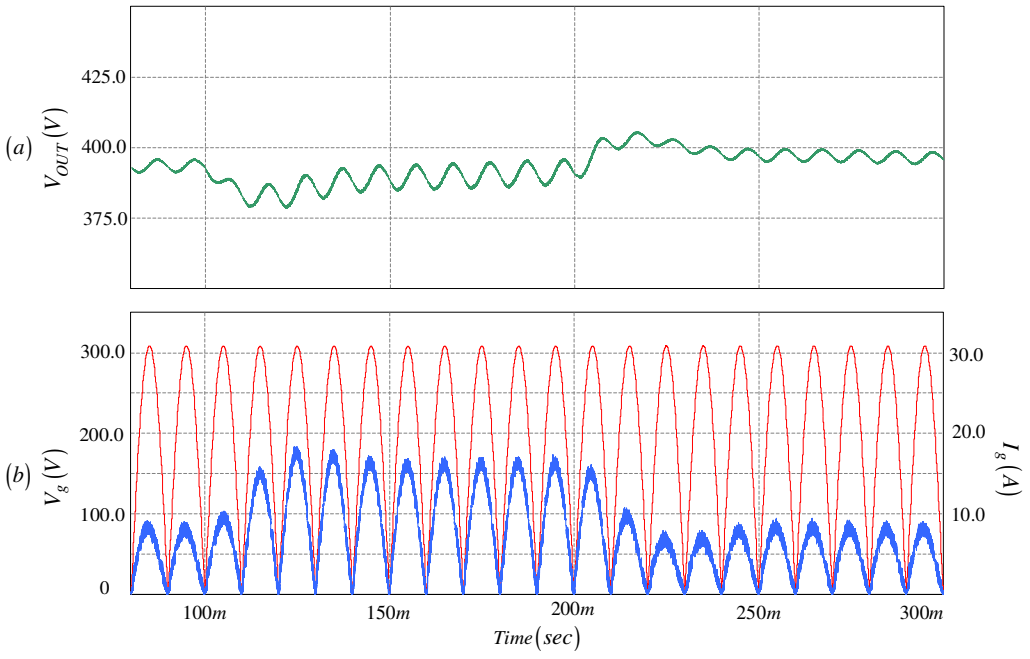

Figure 2.34 The dynamic response of the converter to loading and load removal conditions, (a) the output voltage regulation and (b) the inductor current regulation.

2.7 Experimental Results of The Two–Phase Interleaved ACM Controlled PFC

In this section the experimental performance of the prototype two–phase ACM controlled PFC is investigated. The experiments are conducted on the prototype PFC which is explained in design section. The waveforms are measured with LeCroy Wave Runner 6050A oscilloscope. The current probes of the oscillator have 10MHz bandwidth and 150 A current rating. The voltage waveforms have 100MHz bandwidth and 1400 V voltage rating. Variable resistor load bank is utilized as load and results are taken at two different output power levels: 1.25 kW and 2.50 kW. These results are compared with simulation results and correlation between them is investigated.

2.7.1 Experimental Results At 1.25kW Output Power

In this part, results taken at 1.25 kW output power load condition are presented. The measured quantities are the line current, line voltage, output load voltage, inductor currents, inductor current and input current ripples, collector–to–emitter voltages of IGBTs, input power quality, and line current THD. In Figure 2.35 and Figure 2.36, the input and output characteristics of the PFC are given. In Figure 2.35, the line voltage and line current waveforms are shown. The line current tracks the line voltage and its wave shape is nearly sinusoidal. At light loading, signal–to–noise ratio (SNR) of the sensed switch currents is low and the compensator is not fully suitable therefore input current is not a pure sine. Also at zero transition points the current is not controllable due to the situation explained in the simulation section. The output voltage ripple is shown in Figure 2.35. The target output voltage is 390V as specified in Table 2.2 and measured mean output voltage is 391.2V (numerical value seen on the oscilloscope screen). The amplitude of 100Hz AC contribution on output voltage is nearly 5V peak–to–peak. These results are consistent with the simulation results.

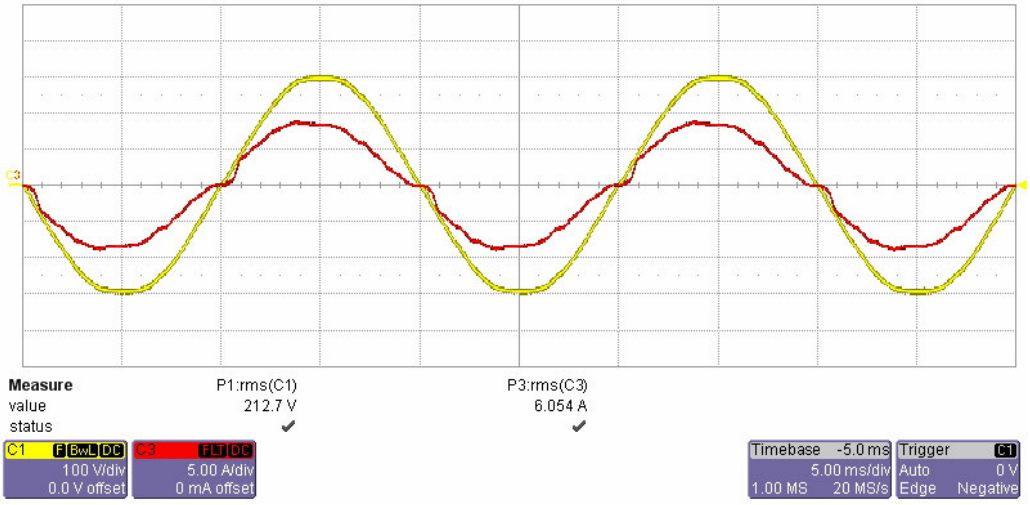

Figure 2.35 The input line voltage (yellow) and line current (red) at 1.25kW.

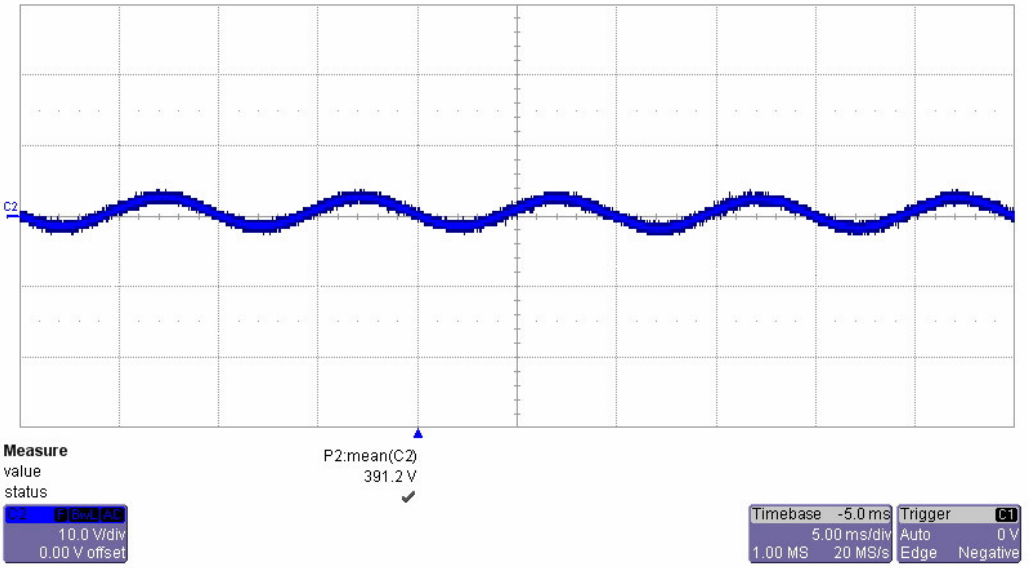

Figure 2.36 The output voltage waveform of the PFC converter at 1.25 kW load (the oscilloscope is in the AC coupling mode where only the AC ripple component of the output voltage is seen on the screen).

From Figure 2.37 to Figure 2.40 the internal characteristics of the PFC converter are given. In Figure 2.37 inductor currents of interleaved legs are given. From the figure it is seen that main design goal is achieved: the input current is shared equally between leading and lagging legs. The detailed views of the peak inductor currents and the peak input current are given in Figure 2.38. Inductor current ripples are approximately 2A and input current ripple is approximately 1.5A. The input current ripple is reduced and its frequency is doubled as explained by theory and simulation. The current ripple magnitudes are consistent with simulation results. In Figure 2.39 collector–to–emitter voltages of leading and lagging leg IGBTs at peak input voltage are given. From the figure it is seen that duty cycle is about 0.25 at peak voltage and 180° phase shift is present between two legs. In Figure 2.40, the detailed view of collector–to–emitter voltage of lagging leg IGBT at turn off is given. The voltage is ringed due to PCB non–idealities and current transformer primary side leakage inductance. The peak value of the oscillation is about 445V. The breakdown voltage of the IGBT is 600V; therefore this situation is not hazardous for circuit operation.

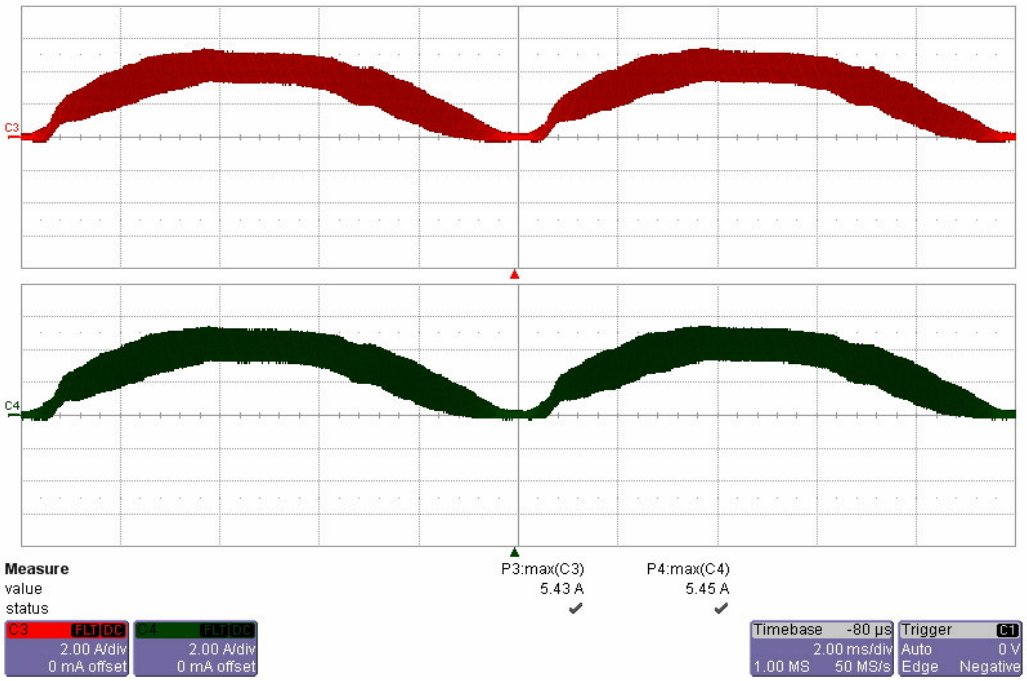

Figure 2.37 Inductor currents of leading (red) and lagging leg (green) for 1.25 kW output power.

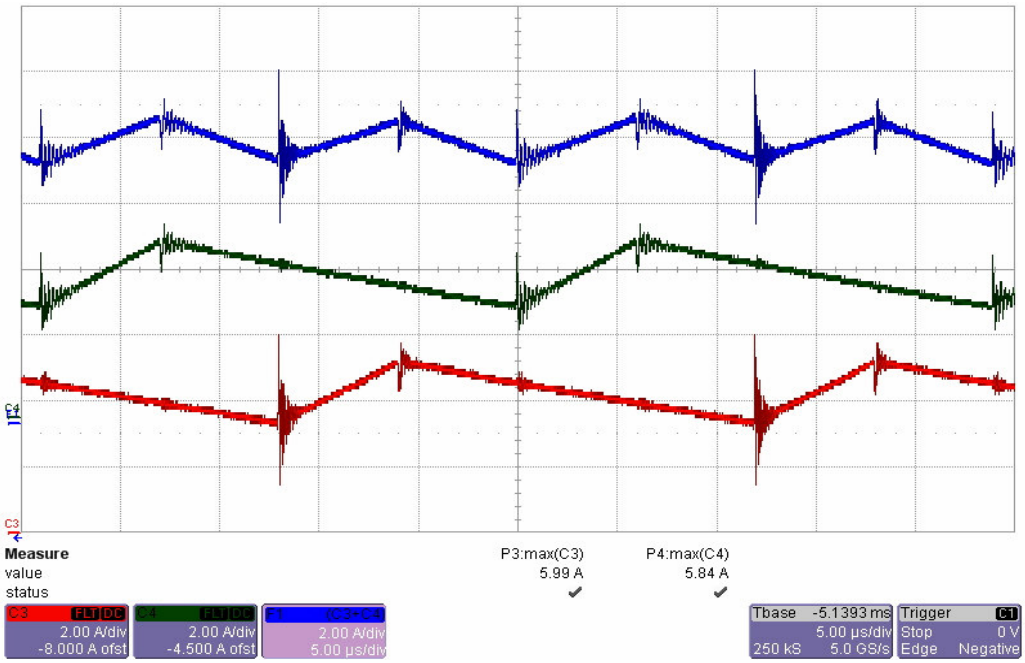

Figure 2.38 Detailed views of peak inductor current ripples of leading leg (red), lagging leg (red), and input current (blue) for 1.25 kW output power.

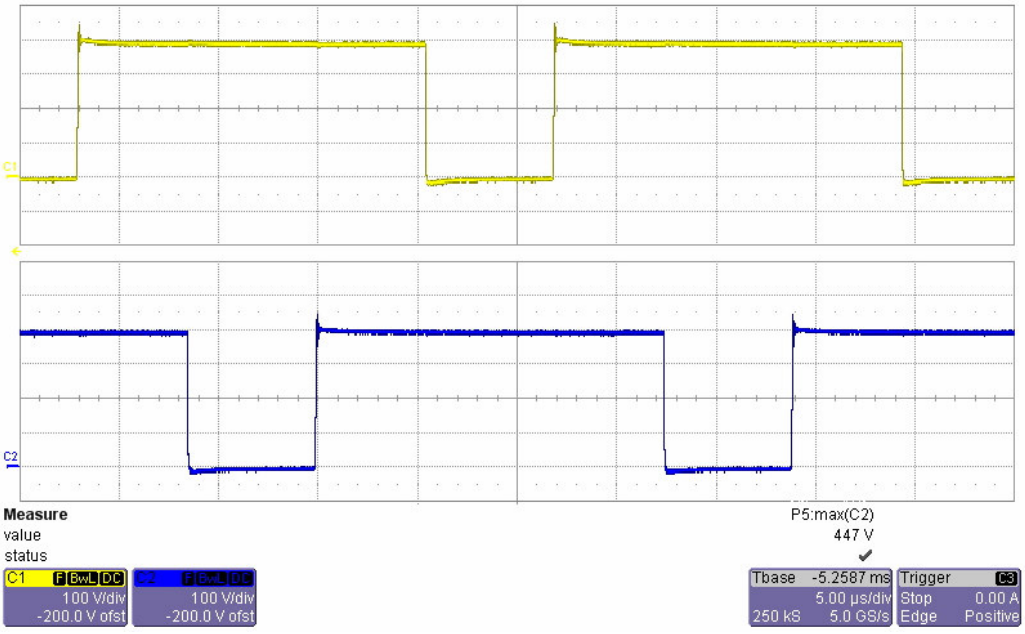

Figure 2.39 Collector–to–emitter voltages of leading (yellow) and lagging (blue) leg IGBTs for 1.25 kW output power.

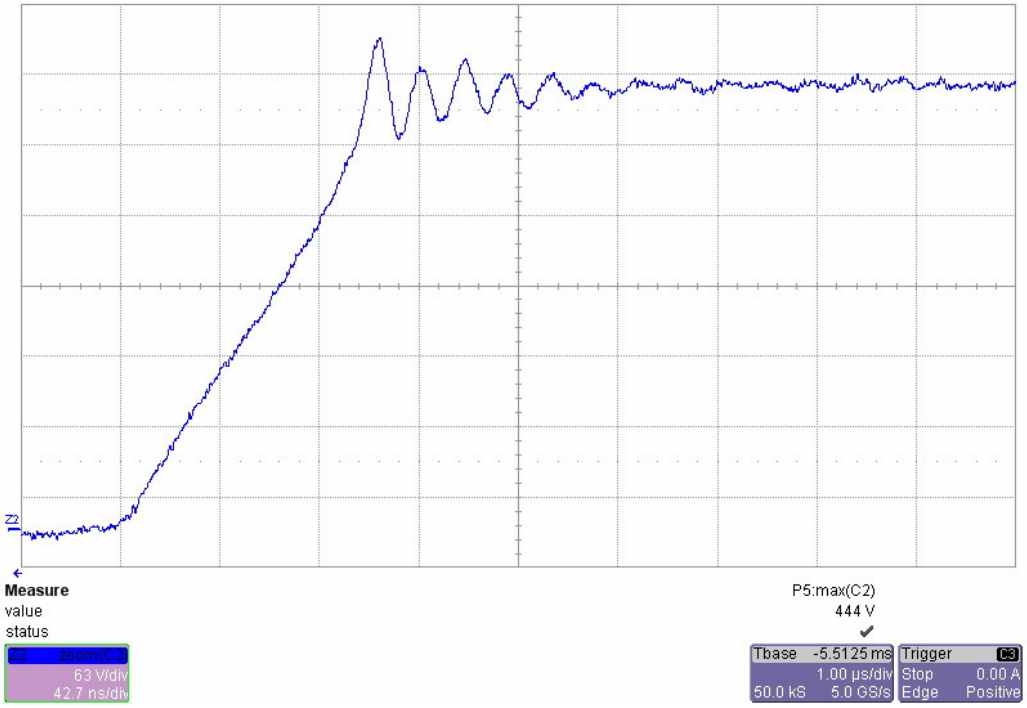

Figure 2.40 Detailed view of lagging leg IGBT collector–to–emitter voltage at turn off for 1.25 kW output power.

In Figure 2.41 and Figure 2.42 the power quality measurements are given. The measurements are taken by Fluke 43B power quality analyzer. In Figure 2.41 input power factor, displacement factor (cosφ) and, input voltage and current waveforms are shown. Both power factor and displacement factor are measured 0.99. These values are better than reasonable levels. In Figure 2.42 harmonic spectrum of the input current is given. Even though the input current has harmonic components up to 15^{th} harmonic, fundamental harmonic is the most dominant while third and fifth harmonics are other significant components. THD of the input current is 8.1%. The experimental results are very close to simulation results given in Figure 2.27 and Table 2.8.

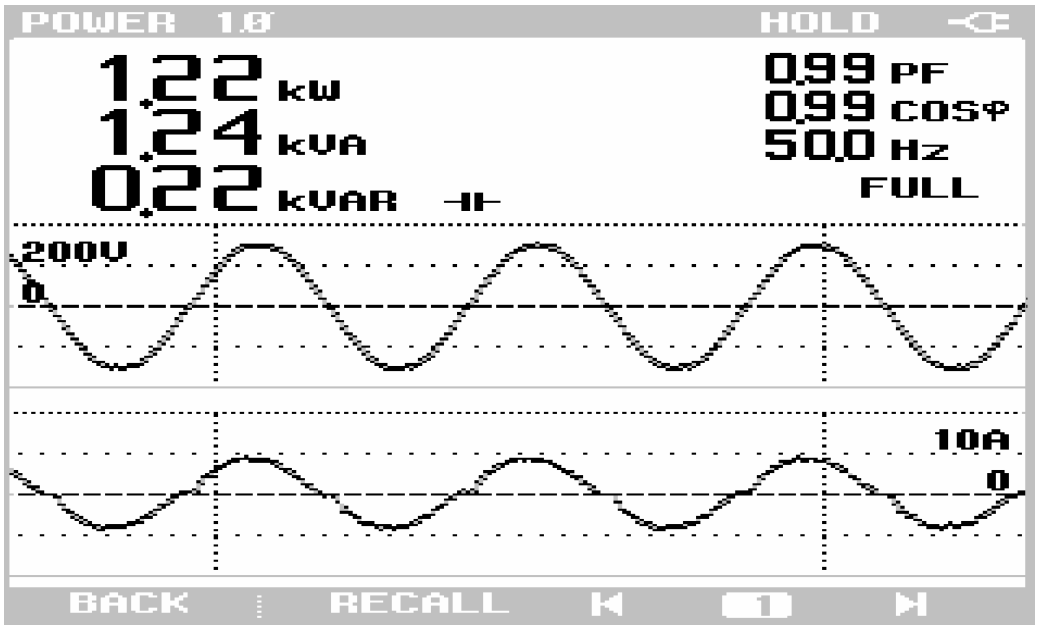

Figure 2.41 Input power factor information obtained by Fluke power quality analyzer for 1.25 kW output power.

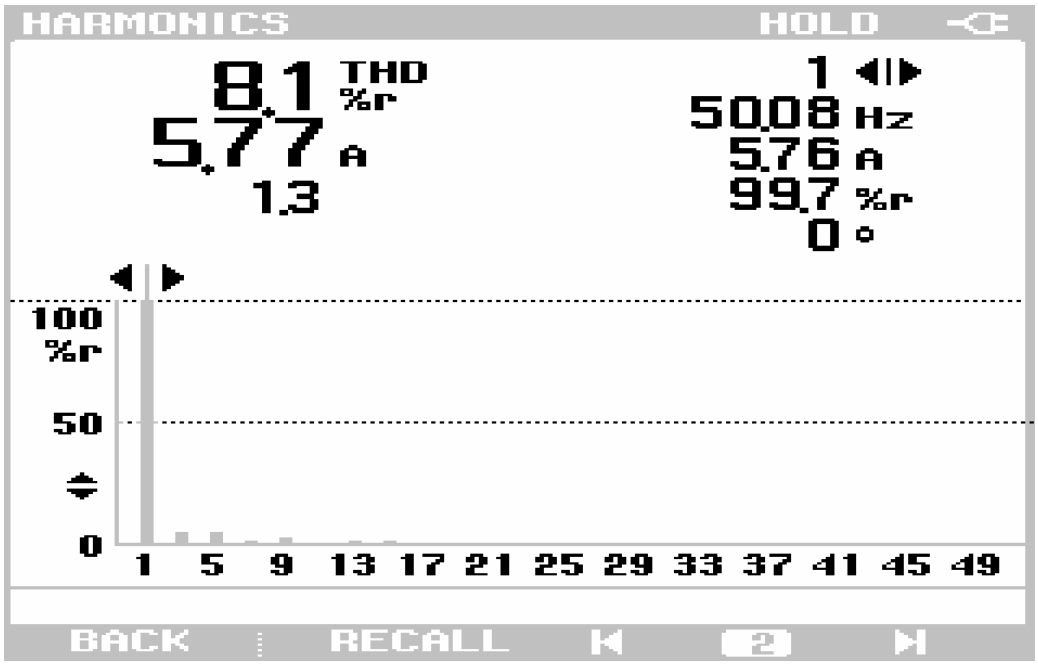

Figure 2.42 Input current harmonics and THD information obtained by Fluke power quality analyzer for 1.25 kW output power.

2.7.2 Experimental Results at 2.5 kW Output Power

Same experiments are conducted under 2.5 kW output load condition to compare the system performance with previous experiment set. It is seen from the experiment results that overall performance of the system is improved with increasing power. The reason for this situation is SNR of switch current measurements are improved and compensators act better. In Figure 2.43 input line voltage and line current waveforms are given. The current waveform is more sinusoidal than the previous experiment result. Output voltage is shown in Figure 2.44. Mean value of the output voltage is 390.7V and the amplitude of the second harmonic contributions are increased as stated by (2.87). Inductor currents are shown in Figure 2.45 and Figure 2.46. The input current is shared equally between two legs as can be observed from Figure 2.45. In Figure 2.46, detailed views of inductor currents and input current at peak current are given. The ripple reduction can be observed from this figure.

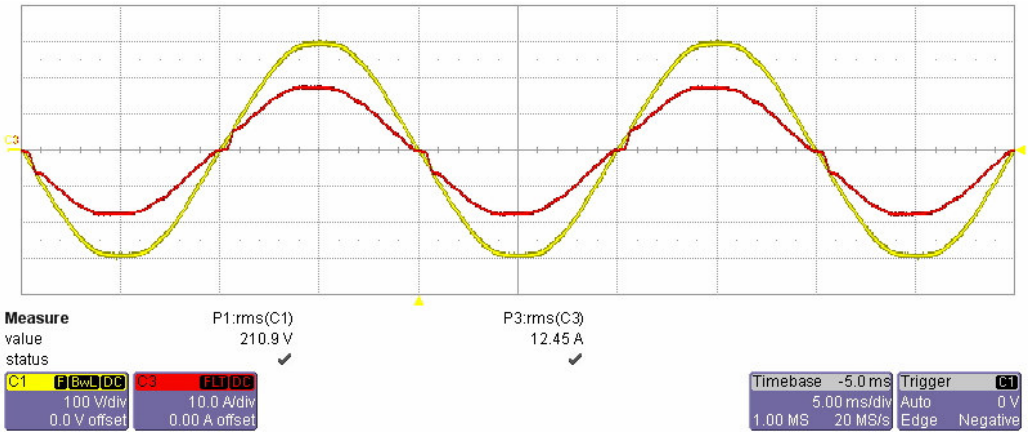

Figure 2.43 The input line voltage (yellow) and line current (red) for 2.5 kW output power.

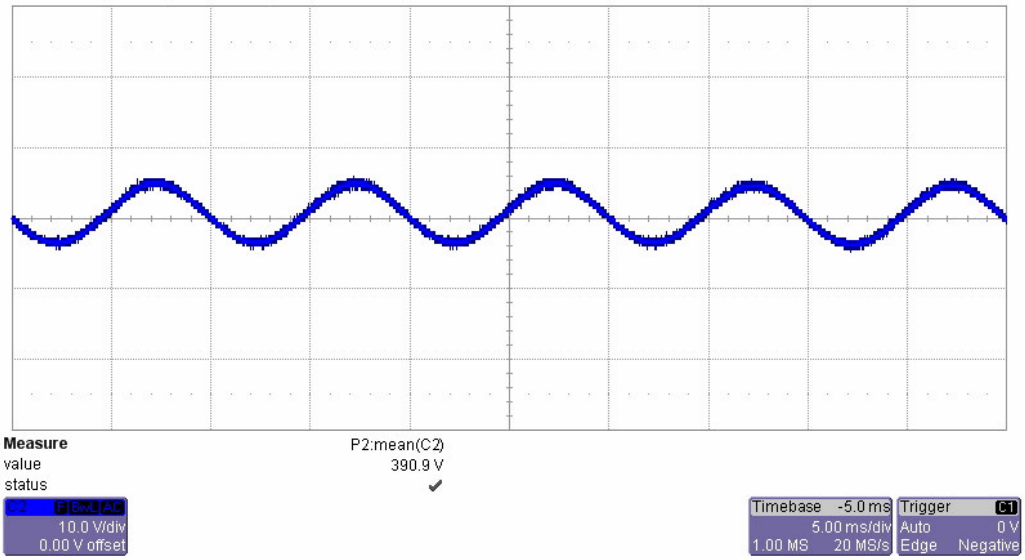

Figure 2.44 The output voltage of the PFC at 2.5 kW loading (the oscilloscope is in the AC coupling mode where only the AC ripple component of the output voltage is seen on the screen).

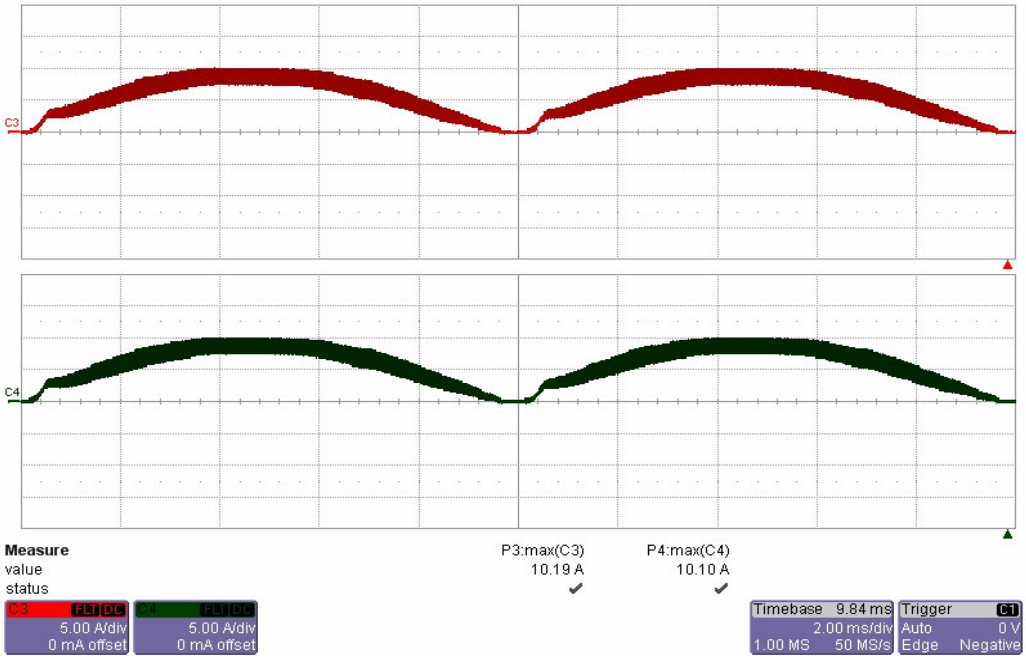

Figure 2.45 Inductor currents of leading (red) and lagging leg (green) for 2.5 kW output power.

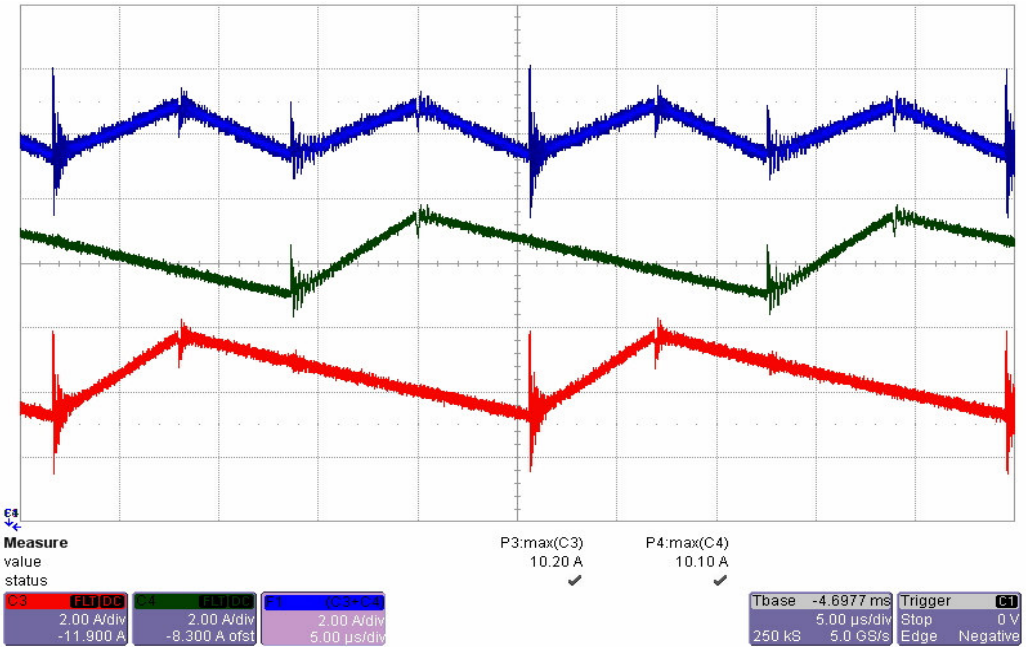

Figure 2.46 Detailed views of peak inductor current ripples of leading (red), lagging leg (red), and diode rectifier output current (blue) for 2.5 kW output power.

In Figure 2.47 and Figure 2.48 collector–to–emitter voltages of two IGBTs are shown. In Figure 2.48, it is seen that the ringing amplitude of the collector–to–emitter voltage at turn off increases with increasing power. Further increasing of this ringing voltage may be hazardous for an 600V breakdown voltage rated IGBT.

The power quality measurements for 2.5 kW output power are given in Figure 2.49 and Figure 2.50. It is seen from Figure 2.49 that input power factor and displacement factor are unity. In Figure 2.50, harmonic spectrum of the line current is given. It is seen from the figure that even though the line current has harmonic components up to 15^{th} harmonic they not significant with compared to fundamental harmonic content. THD of the line current is reduced to 4.2%. Evaluating power quality results of 1.25 kW output load experiments and 2.5 kW output load experiments together indicates that the power quality is improved with increasing power.

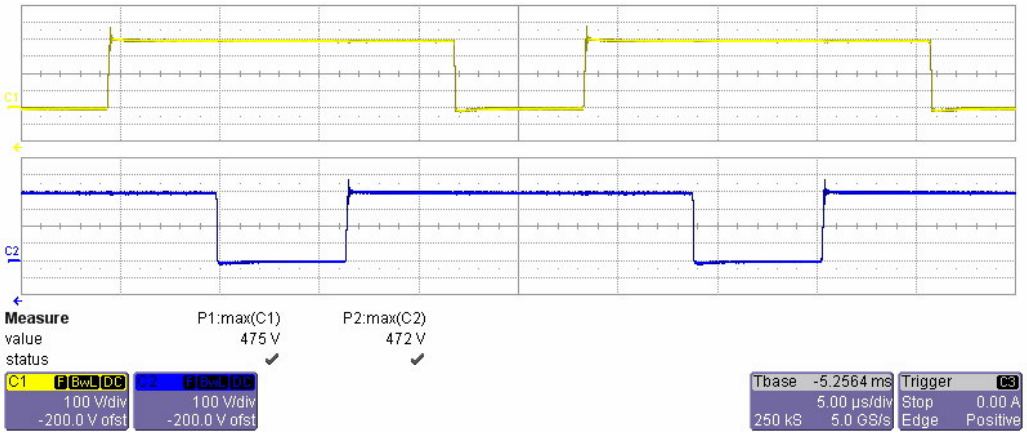

Figure 2.47 Collector–to–emitter voltages of leading (yellow) and lagging (blue) leg IGBTs for 2.5 kW output power.

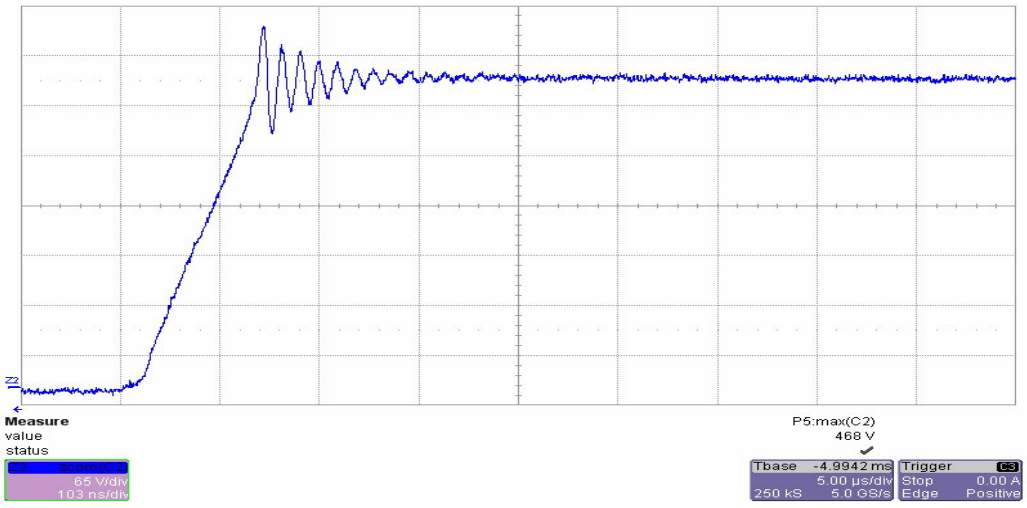

Figure 2.48 Detailed view of lagging leg IGBT collector–to–emitter voltage at turn off for 2.5 kW output power.

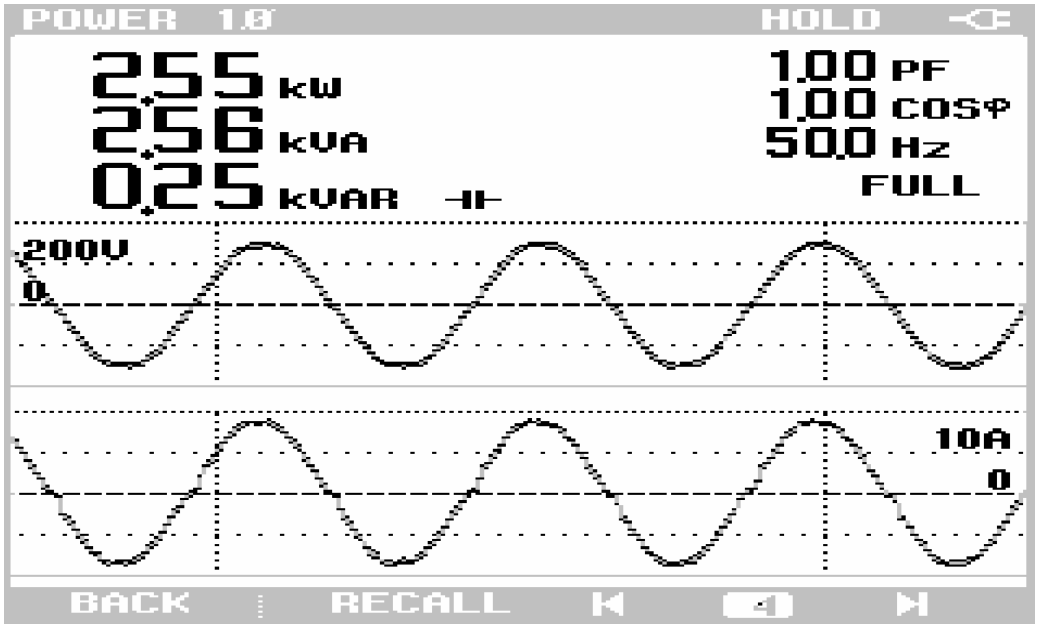

Figure 2.49 The input power factor information obtained by the Fluke power quality analyzer for 2.5 kW output power.

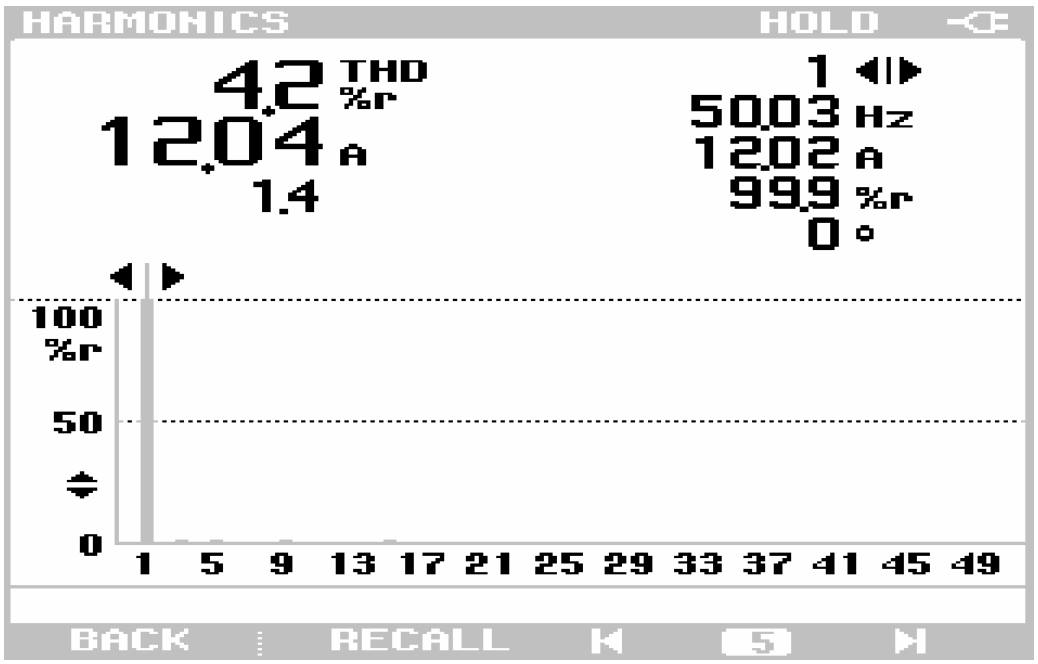

Figure 2.50 The input current harmonics and THD information obtained by the Fluke power quality analyzer for 2.5 kW output power.

2.8 Chapter Conclusion

In this chapter an interleaved ACM controlled boost PFC is introduced and investigated. At first, some methods including device paralleling, module paralleling, and power stage paralleling are mentioned and their advantages and disadvantages are discussed. Later interleaving method and its features are introduced. Reductions in the input current and output voltage ripples due to interleaving are mathematically expressed. The ACM control method is explained and small signal model of the ACM controlled boost PFC is derived. Voltage and current loop compensators of the PFC is designed. Design of the two–phase interleaved PFC prototype is explained. The design is verified via computer simulations. At last, results of the experiments conducted on prototype are presented, and the theory and simulation results are verified. The next chapter involves the next stage of power conversion involved in the AC/DC regulated supply, the DC/DC full bridge converter.

CHAPTER 3

OUTPUT VOLTAGE REGULATION OF AN FB – PS – ZVS – DC/DC CONVERTER

3.1 Introduction

3.1.1 The Full Bridge DC/DC Converter Topology And The Phase Shifted PWM Method

The full bridge DC/DC converter topology is one of the isolated converter topologies with four controllable switches. The topology has a suitable structure to be utilized for various applications including DC motor driving, DC/AC conversion for single phase uninterruptible power supplies and DC/DC conversion [1]. In this thesis study, the converter is utilized for DC/DC conversion. The general structure of the converter is given in Figure 3.1. It is seen from the figure that the converter has three stages: the DC/AC inverter stage, the isolation stage, and the AC/DC converter stage. The input DC voltage is converted to high frequency AC voltage and transferred to the secondary side of the transformer with a gain factor determined by the winding ratio of the transformer. The transformer secondary AC voltage is rectified with the output diode rectifier and the high frequency components of the output voltage are filtered by the output LC filter. The galvanically isolated input and output stages provide safe operation in high power applications; therefore this topology is widely utilized in multi–kilowatt DC/DC conversion applications. The topology allows all switching devices operate under zero voltage switching (ZVS) condition with the utilization of the phase shifted (PS) PWM method [24]. A comprehensive

explanation of the PS PWM method is given in [5]. In the PS PWM method, all switches of the inverter operate at nearly 0.5 duty cycle. There should be a dead time between the switching of two switches in one leg of the inverter stage to avoid shoot-through failure. The switches in different legs of the AC/DC inverter are switched with a variable phase shift. The gate signals are applied earlier to the switches in the "leading leg" of the inverter and applied with a phase shift (lag) to the switches in the "lagging leg" of the inverter. The output voltage of the converter is determined by this phase shift. The input voltage–to–output voltage relation of the full bridge DC/DC converter is similar to that of the conventional buck converter. This relation is given in (3.1).

$$\frac{v_{out}}{v_g} = \frac{N_S}{N_P} d_{oeff} \tag{3.1}$$

Where d_{oeff} is the effective duty cycle and defines the width of the secondary voltage of the transformer.

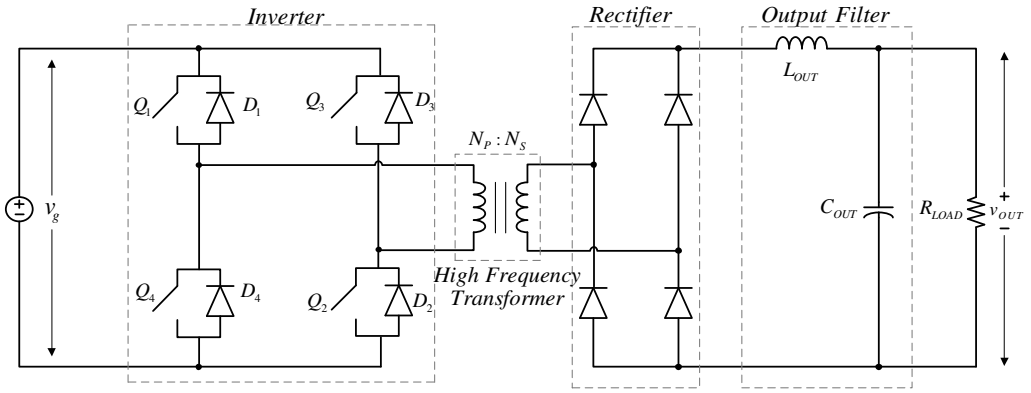

Figure 3.1 The general structure of a full bridge DC/DC converter.

3.1.2 Zero Voltage Switching

In the switch mode power converters, the power consumed on the switches has two components: the conduction losses and the switching losses. The conduction losses are caused by the junction potential and the on-state resistance voltage drop of the switch and the switching losses are caused by the current flown through the switch while there is voltage on it at the switching moment. The switching losses become dominant at high switching frequency operation. Zero switching losses can be provided by switching the transistor when there is no voltage drop on it. The PS PWM method applied on a full bridge converter permits resonant charging and discharging of the parasitic output capacitances of the transistors with the energy stored in the leakage inductance of the high frequency transformer. Therefore, with proper switching of the transistors, switching at zero voltage can be achieved. The FB DC/DC converter circuit configuration with parasitic components included is given in Figure 3.2.

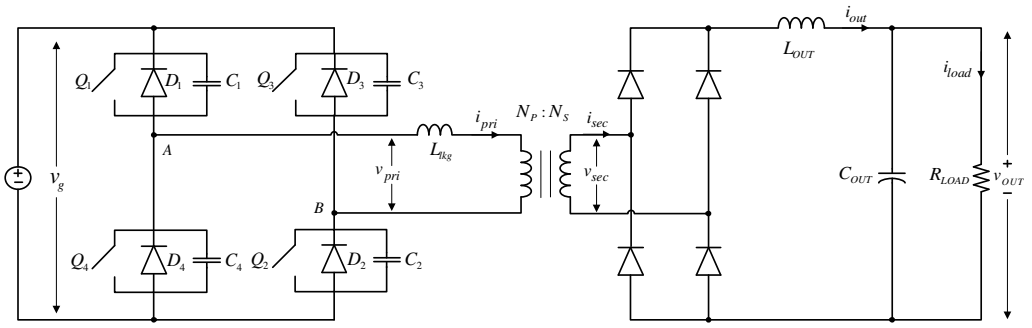

Figure 3.2 The full bridge DC/DC converter circuit topology with parasitic components included in the circuit.

The main waveforms of the converter including the primary voltage, the primary current, and the secondary voltage waveforms of the transformer are given in Figure 3.3. The zero voltage switching operation is briefly explained referring to that figure. The circuit operation can be divided into six operation modes in a half switching

period. These modes are identical for the other half of the switching period. In mode0, the diagonal switches Q_1 and Q_2 are conducting the primary current and power is transferred from the primary side to the secondary side. Currents flown through the leakage and the output inductors are built up and energy is stored in these inductors. In mode1, transistor Q_1 is turned off and C_1 is charged while C_4 is discharged by the resonance between these capacitors, the leakage, and the output inductors. The energy stored in the output inductor is much bigger than the energy required for charging and discharging the capacitors, therefore zero voltage switching condition is guaranteed for the switches of leading leg. At the end of mode1, the voltage across Q_4 is totally removed. Therefore, this transistor can be turned on at zero voltage. In mode3 Q_2 is turned off and capacitors C_2 and C_3 start resonating. Referring to Figure 3.3 all diodes of the output diode rectifier start conducting therefore secondary side of the isolation transformer is shorted. Therefore the energy required to discharge C_3 and charge C_2 cannot be supplied from the output inductor, only supplied from the leakage inductor. If the energy stored in the leakage inductor is big enough, at the end of this mode the voltage on transistor Q_3 is totally removed. In mode4 transistors Q_3 and Q_4 are turned on at zero voltage and the primary voltage is reversed. All rectifier diodes are still conducting in this mode, therefore secondary voltage is zero. At the end of this mode the current flowing through two diagonal rectifier diodes become zero and secondary voltage is developed again.

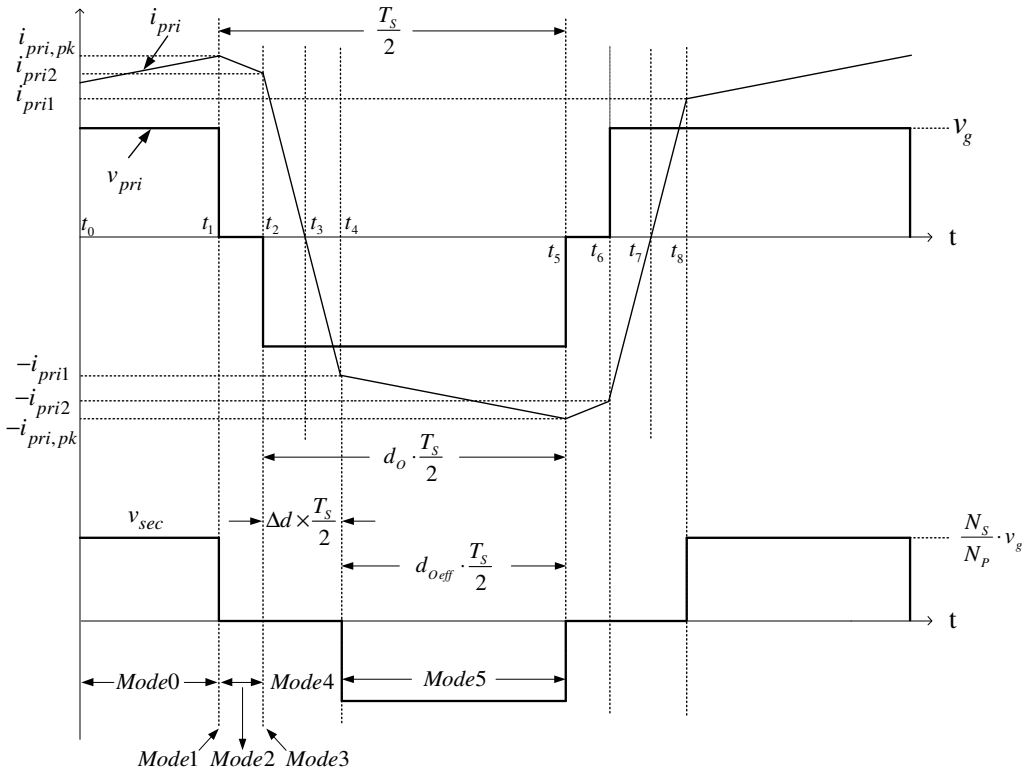

Figure 3.3 The primary voltage, primary current, and secondary voltage waveforms of the isolation transformer.

As stated previously, zero voltage switching conditions are not the same for the leading and the lagging legs because the energy required to totally charge and discharge the output capacitors of the switches in the leading leg can be supplied from the large output inductor. But the same energy for the lagging leg can only be supplied from the small leakage inductor of the transformer and this energy may be insufficient for some loading conditions. In order to provide ZVS condition for the lagging leg switches, the dead time applied between two consecutive switching actions should be at least one fourth of the resonance period (3.2).

$$\delta_R = \frac{T_R}{4} = \frac{\pi}{2}\sqrt{L_{lkg}C_t} \tag{3.2}$$

C_t is the equivalent parasitic capacitance of lagging leg switches and can be expressed by (3.3).

$$C_t = C_2 + C_3 \tag{3.3}$$

The zero voltage switching range of the lagging leg switches can be improved by increasing the value of leakage inductance. However, it follows from equation (3.1) and Figure 3.3 that increasing the leakage inductance increases the required dead time and decreases the slope of primary current. These two results negatively effect the efficiency and the dynamic behavior of the converter. Therefore, an optimum value for the leakage inductance should be utilized. The minimum load current satisfying the adequate energy for ZVS can be expressed by (3.4) [24]. Δi_{OUT} is the output inductor current ripple.

$$i_{OUT,critical} = v_g \frac{N_P}{N_S}\sqrt{\frac{C_t}{L_{lkg}}} - \frac{\Delta i_{OUT}}{2} + \frac{v_{OUT}}{L_{OUT}}(1-d_o)\frac{T_S}{2} \tag{3.4}$$

3.1.3 Design Parameters of Prototype FB – PS – ZVS DC/DC Converter

In this thesis, the investigations and experiments are conducted on a prototype converter which was manufactured by Mr. Mutlu USLU for his thesis study [5]. This converter was designed as a current source for arc welding machines. In this thesis study, this power converter has been converted to a voltage regulator by adding an output filter capacitor in parallel to the load and output voltage sensing circuitry.

Controlling the output voltage of the PS-FB DC/DC converter with a digital controller is the scope of this chapter. In order to design a proper controller, the small signal model of the converter is derived. The designed controller is verified by means of computer simulations and it is implemented on the prototype converter with a digital signal processor (DSP). The electrical design specifications of the prototype FB–PS–ZVS DC/DC converter are given in Table 3.1.

Table 3.1 Electrical specifications of the prototype FB–PS–ZVS DC/DC converter

Input voltage (v_g)	400 V
Output voltage (v_{OUT})	55 V
Maximum output current (i_{OUT})	100 A
Switching frequency (f_S)	50 kHz
Dead-time (t_d)	0.9 μsec
Critical output current ($i_{OUT,critical}$)	35 A

The resonance capacitance and the leakage inductance value cannot be provided by the parasitic components of the transistors and the isolation transformer for given electrical specifications. Therefore, two external capacitors are connected to the lagging leg transistors and an external inductor is connected in series with the high frequency isolation transformer. The design parameters including external resonance components are given in Table 3.2.

Table 3.2 The design parameters of prototype FB–PS–ZVS DC/DC converter

External resonance capacitor (C_{ext})	4.7	nF
External resonance inductor (L_{ext})	23	μH
Output inductor (L_{out})	125	μH
Output capacitor (C_{out})	720	μF
Primary to secondary winding turns ratio (n)	4	
Leakage inductance of transformer (L_{lkg})	0.28	μH

The fast switching IGBT modules produced by Semikron are utilized in the inverter stage of the converter due to their high performance under high current, high voltage and high frequency operation conditions. Comprehensive information about these IGBT modules is applicable in [25] and has been summarized in [5]. In this thesis study, the small signal analysis of the FB–PS–ZVS DC/DC converter is performed

and a controller is designed based on the small signal model of the converter. The controller is implemented on the prototype power converter by a digital signal processor manufactured by Texas Instruments with the part number TMS320F2808.

3.2 Small Signal Analysis of the FB–PS–ZVS DC/DC Converter

The FB–PS–ZVS DC/DC converter is operationally similar to the conventional buck converter. Therefore, their small signal models are also similar except some significant differences originated from the phase shifted PWM operation and the large leakage inductance of the isolation transformer [26]. The effects of these differences are investigated and the small signal model (SSM) of the FB–PS–ZVS DC/DC converter is developed by modifying the model of the conventional buck converter which is given in Figure 3.4 [14].

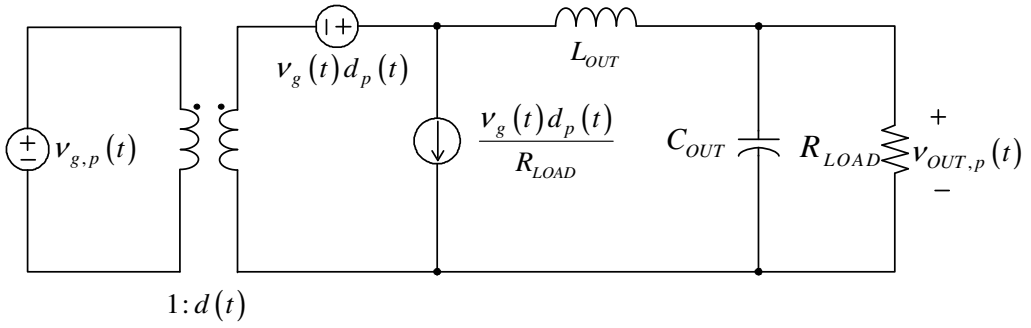

Figure 3.4 The small signal circuit model of the conventional buck converter.

The effective duty cycle can be expressed by (3.5) by investigating Figure 3.3.

$$d_{oeff} = d_o - \Delta d \tag{3.5}$$

Where Δd is the loss of the duty cycle due to the rising and falling slopes of the primary current and can be expressed by (3.6) by examining Figure 3.3.

$$\Delta d = \frac{n}{\frac{v_g}{L_{lkg}}\frac{T_S}{2}}\left(2i_{OUT} - \frac{v_{OUT}}{L_{OUT}}(1-d_o)\frac{T_S}{2}\right) \tag{3.6}$$

It is obvious from (3.6) that the effective duty cycle is dependent to the input voltage, switching period, the output current, the leakage inductor, the output inductor, and the primary duty cycle. The contributions of these terms to the small signal model should be analyzed [26]. The analysis is performed by investigating the effective duty cycle modulation due to the output current and the input voltage perturbations.

The peak value of the primary current is changed due to the small signal variations of the output current. The slope of the primary current is not affected due to this change but the width of the secondary voltage is affected. The situation is illustrated in Figure 3.5. Assume that the primary duty cycle is kept constant and a small signal perturbation increasing the output current is added. Therefore, the peak value of the primary current is increased as illustrated in Figure 3.5. The width of the secondary voltage is decreased with an amount of Δt due to this variation. Thus, the effective duty cycle decreases. The change of duty cycle due to the output current variation can be expressed by (3.7) by examining Figure 3.3.

$$d_{i,p} = -\frac{\Delta t}{T_S/2} = -4\frac{nL_{lkg}f_s}{v_g}i_{OUT,p} = -\frac{R_d}{nv_g}i_{OUT,p} \tag{3.7}$$

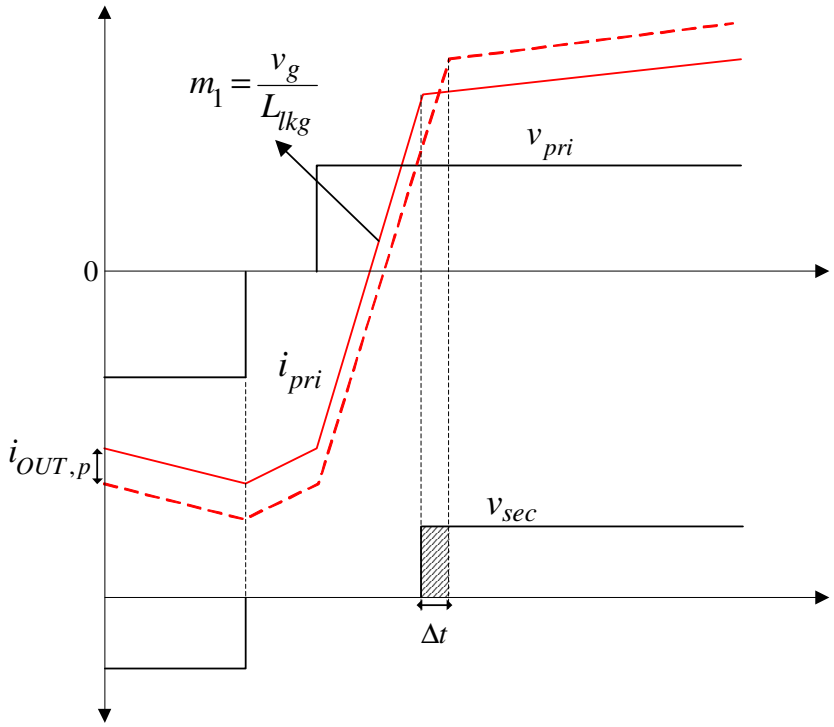

Figure 3.5 The effect of output current variations on the effective duty cycle.

The negative sign in (3.7) points out the natural feedback behavior of the system. An increase in inductor current causes reduction in the effective duty cycle and vice versa [26].

The slope of the primary current in mode4 is proportional to the input voltage and the leakage inductance. Therefore, this slope is changed by variation of the input voltage. Assume that a small signal perturbation is added to increase the input voltage while the primary duty cycle is kept constant. Then the primary current slope is increased and it reaches to its peak value sooner; therefore the effective duty cycle is increased. This situation is illustrated in Figure 3.6. Change of the effective duty cycle can be derived by examining Figure 3.6 under the assumption that the perturbation value is much smaller than the input voltage (3.8) [26].

$$d_{v,p} = \frac{\Delta t}{T_S/2} = \left(i_{OUT} - \frac{v_{OUT}}{L_{OUT}}(1-d_o)\frac{T_S}{4} \right) \frac{4nL_{lkg}f_s}{v^2{}_g} v_{g,p} \tag{3.8}$$

The $(1–d_o)$ term in (3.8) should be kept as small as possible to minimize the conduction losses caused by the circulating currents at the primary side [24], therefore this term can be neglected. Then (3.8) can be simplified to (3.9).

$$d_{v,p} = \frac{4nL_{lkg}f_s i_{OUT}}{v^2{}_g} v_{g,p} = \frac{R_d i_{OUT}}{nv^2{}_g} v_{g,p} \tag{3.9}$$

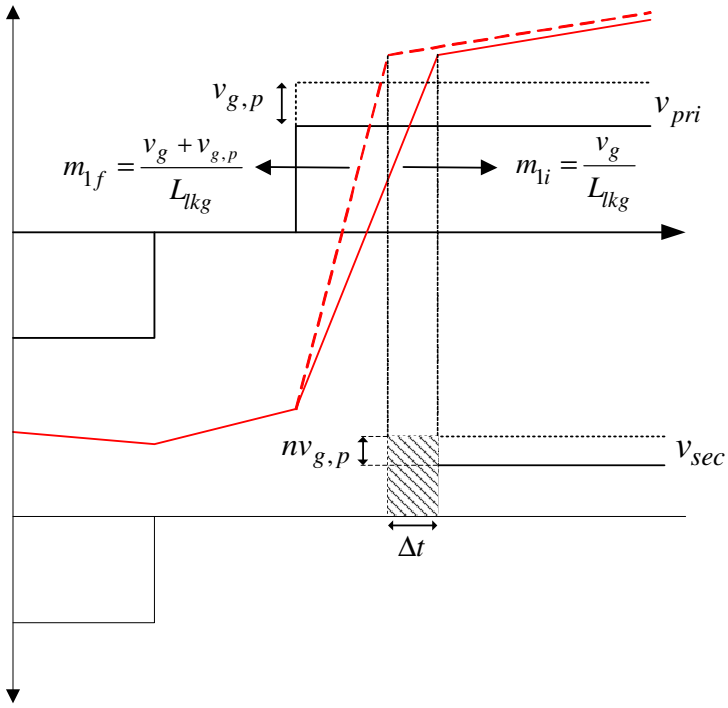

Figure 3.6 The effect of input voltage variations on the effective duty cycle.

The SSM of the FB–PS–ZVS DC/DC converter, which is given in Figure 3.7, can be derived from the SSM of the buck converter by replacing the d_p term of Figure 3.4 with the $d_{eff,p}$ term which is the result of the previous analysis (3.10).

$$d_{eff,p} = d_p + d_{i,p} + d_{v,p} \tag{3.10}$$

The small signal contributions caused from $d_{v,p}$ and $d_{i,p}$ are depicted as dependent voltage and current sources in Figure 3.7, because their values are controlled by the input voltage and output current variations.

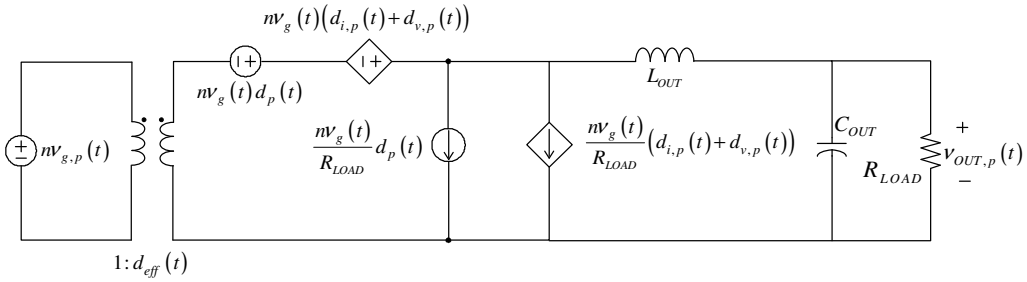

Figure 3.7 The small signal model of the FB–PS–ZVS DC/DC converter derived from the buck converter.

In this thesis work, the output voltage is controlled by a voltage mode controller. Therefore, the duty cycle–to–output voltage transfer function of the converter is derived from the SSM of the converter. The duty cycle–to–output voltage transfer function expresses impression of control parameter disturbance on the output while the input voltage disturbance is zero. It can be expressed by (3.11).

$$G_{vd} = \left.\frac{v_{OUT,p}(s)}{d_p(s)}\right|_{v_{g,p}=0} \tag{3.11}$$

The SSM given in Figure 3.7 can be reduced to one in Figure 3.8 after removing the small signal perturbations of the input voltage.

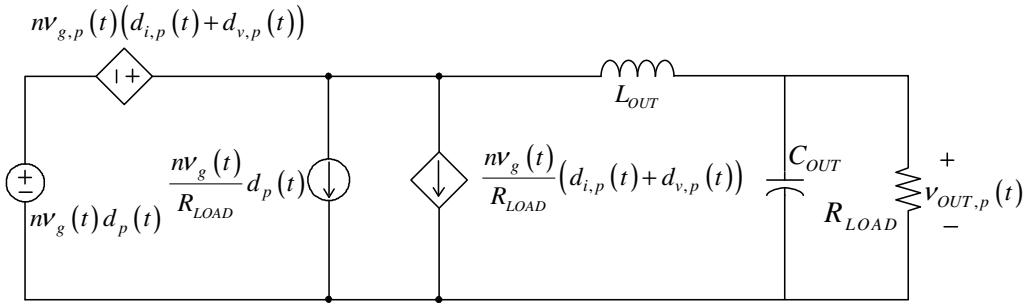

Figure 3.8 The reduced model of the FB-PS DC/DC converter with zero input voltage disturbances.

In order to analyze the circuit given in Figure 3.8, the superposition rule is applied. The independent voltage and current sources are killed independently and the expression for the output voltage is computed for two cases. At last, these two results are summed and the expression for the output voltage given in (3.12) is found.

$$v_{out,p}=\frac{nv_g}{s^2L_{OUT}C_{OUT}+s\left(R_d+\frac{L_{OUT}}{R_{LOAD}}\right)+\frac{R_d}{R_{LOAD}}+1}d_p \tag{3.12}$$

As stated previously, the leakage inductance value should be kept as low as possible to minimize duty cycle loss. Therefore, the R_d value can be assumed to be much smaller than the load resistance and the R_d/R_{LOAD} term can be neglected. Substituting (3.12) into (3.11) yields,

$$G_{vd}=\left.\frac{v_{OUT,p}(s)}{d_p(s)}\right|_{v_{g,p}=0}=\frac{nv_g\omega_o^{\,2}}{s^2+s2\omega_o\xi+\omega_o^{\,2}} \tag{3.13}$$

The damping factor and critical frequency are expressed in (3.14) and (3.15).

$$\xi=\frac{1}{2\times R_{LOAD}}\sqrt{\frac{L_{OUT}}{C_{OUT}}}+\frac{R_d}{2}\sqrt{\frac{C_{OUT}}{L_{OUT}}} \tag{3.14}$$

$$\omega_o = \frac{1}{\sqrt{L_{OUT} C_{OUT}}} \tag{3.15}$$

The system behavior can be understood by investigating the duty cycle–to–output voltage transfer function of the system. Substituting the design parameters given in Table 3.1 and Table 3.2 into the transfer function (3.13) yields,

$$G_{vd} = \frac{1.111 \times 10^9}{s^2 + 5028s + 1.111 \times 10^7} \tag{3.16}$$

The voltage control loop is given in Figure 3.9. In the figure, G_{vc} is the loop compensator and $T_v(s)$ is the open loop voltage loop gain.

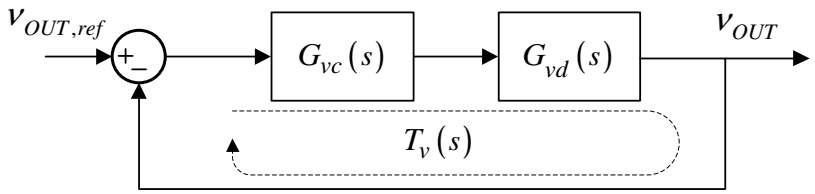

Figure 3.9 The voltage control loop of the FB–PS–ZVS converter.

The Bode diagram of duty cycle–to–output voltage transfer function of (3.16) is given in Figure 3.10(a). From the figure it is observed that crossover frequency of the system is 5.3 kHz and the phase margin is 9°. In order to compensate the phase margin and improve the low frequency gain, a PI compensator is implemented. The parameters of the PI controller are designed to obtain 45° of phase margin and a reasonable low frequency gain. PI compensator transfer function is given in (3.17). Bode diagram of voltage loop gain is given in Figure 3.10(b).

$$G_{vc}(s) = \frac{0.0205s + 50}{s} \tag{3.15}$$

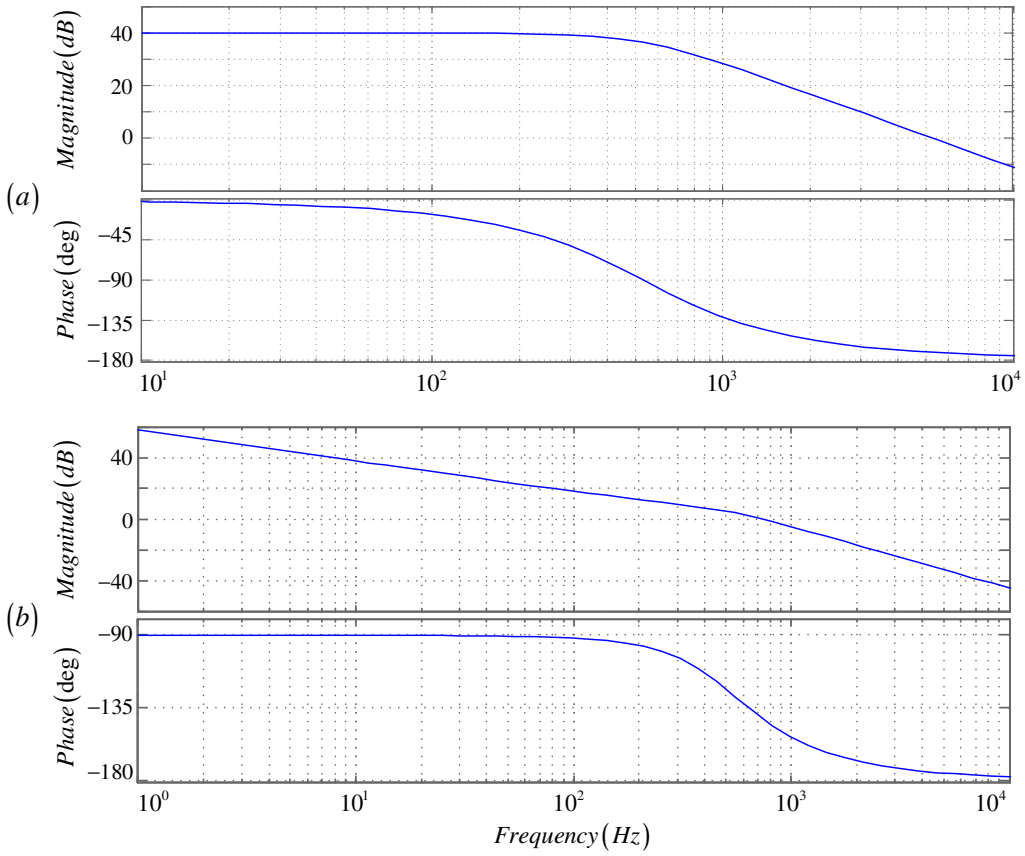

Figure 3.10 Bode diagrams of (a) the duty cycle–to–output voltage transfer function of power stage and (b) the voltage loop gain.

The control algorithm is embedded into a digital signal processor. The reason for utilization of the digital controller is improving the flexibility and enabling the implementation of different control algorithms. The controller transfer function given in (3.17) is discretized by the bilinear approximation method for the purpose of preserving the gain and phase properties of the controller at low frequencies [27]. Designing the controller in continuous domain and later discretizing it is called as digital redesign approach [27]. The output voltage is sensed with Hall effect type voltage transducers and the measured voltage is conditioned for analog–to–digital conversion. TMS320F2808 has 16 analog–to–digital converters (ADC) with 12 bits resolution [28]. The discretized output voltage is compared with the reference signal and the output voltage error is compensated with the digital compensator. The output

of the compensator is the duty cycle information. Therefore it is converted to the phase information with the expression given in (3.18) [5] The control block diagram of the system is given in Figure 3.11.

$$d_o = 1 - \frac{\varphi}{180} - \frac{2t_d}{T_s} \tag{3.18}$$

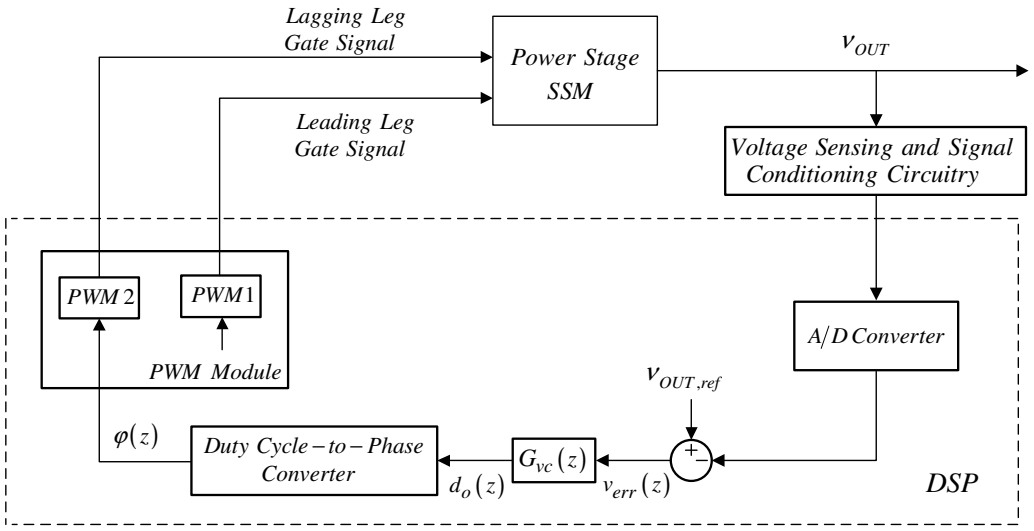

Figure 3.11 The controller block diagram of the FB–PS–ZVS DC/DC converter.

3.3 Transient Flux Unbalancing on The Primary Windings of The Isolation Transformer

In previous sections, the small signal model of the FB–PS–ZVS DC/DC converter was derived. The magnetic characteristics of the isolation transformer do not take part in this model, unsaturable transformer utilization is assumed. Therefore, in the practical real system some unpredicted problems related to the transformer saturation can be encountered. The magnetic flux developed on the primary turns of transformer is expressed by (3.19). In order to prevent magnetic saturation of the

primary windings of the transformer, the flux over one switching cycle should be set to zero. This condition is satisfied in the steady–state.

$$\int_{t_o}^{t_o+T} d\Phi = \frac{1}{N_P}\int_{t_o}^{t_o+T} v_{pri}\,dt \tag{3.19}$$

Therefore, the flux over one period can be expressed by (3.20). T is the half of one switching cycle.

$$\Delta\Phi = \frac{v_{pri}T}{N_P}d \tag{3.20}$$

Assume that while the converter is operated at steady–state, a sudden increase in the duty cycle is demanded and the phase shift between the PWM gate signals of two legs is changed in one switching period. Let the peak flux at the first half of the switching period be Φ_{P1}, the peak flux at the second half be Φ_{P2}, the duty cycle demand at the first half d_1 and at the second half be d_2. This situation is illustrated in Figure 3.12. Expressions for the fluxes at the first and second halves of the duty cycle are given in (3.21) and (3.22).

$$\Phi_{P1} = -\frac{v_g}{N_P}\frac{T}{2}d_1 \tag{3.21}$$

$$\Phi_{P2} = -\frac{v_g}{N_P}\frac{T}{2}d_1 + \frac{v_g}{N_P}T_S d_2 = \frac{v_g}{N_P}T\left(d_2 - \frac{d_1}{2}\right) \tag{3.22}$$

The offset flux generated on the transformer core is the average of the peak flux values (3.23).

$$\Phi_{Offset} = \frac{\Phi_{P1}+\Phi_{P2}}{2} = \frac{v_g}{N_P}\frac{T}{2}\left(d_2 - d_1\right) \tag{3.23}$$

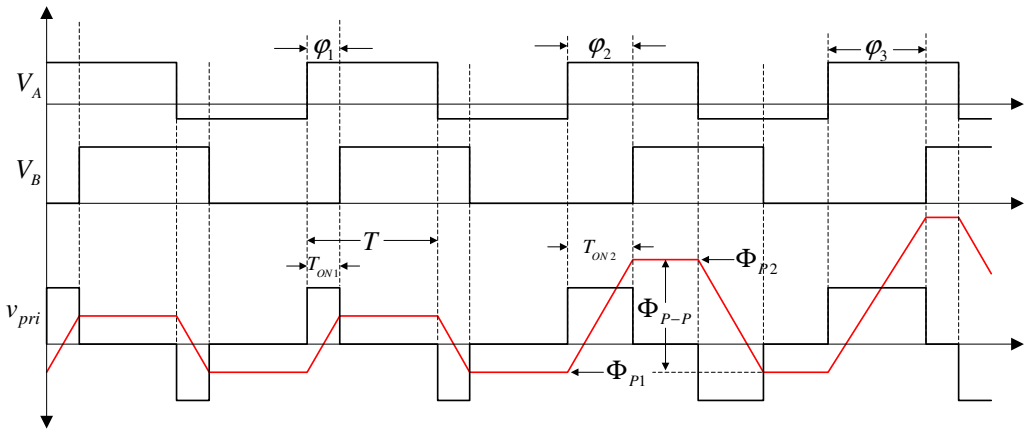

Figure 3.12 Flux unbalancing on the primary windings of the transformer during transients. Node A (top), node B (middle) and primary winding (bottom) voltages and the primary winding flux (red) are shown.

If the flux offset is sufficiently large, the transformer core may saturate and excessive currents can be developed. Excessive primary current may cause catastrophic system failures like blowing up IGBTs and melting the isolation plating of transformer windings. The excessive primary current due to core saturation is shown in Figure 3.13. This data was recorded while the experiments on the prototype converter were conducted. When the current exceeds the predetermined safety value, the over current protection circuitry is operated and gate signals are stopped to protect the system. The dynamical response is negatively affected from this phenomenon. The bandwidth of the voltage loop should be suitably low because fast dynamical response cause sudden changes in the phase shift. The bandwidth of the voltage loop with the proposed controller given in (3.17) is set around 700 Hz for the purpose of preventing the core saturation. Note that this bandwidth is quite low for a system with 50 kHz switching frequency.

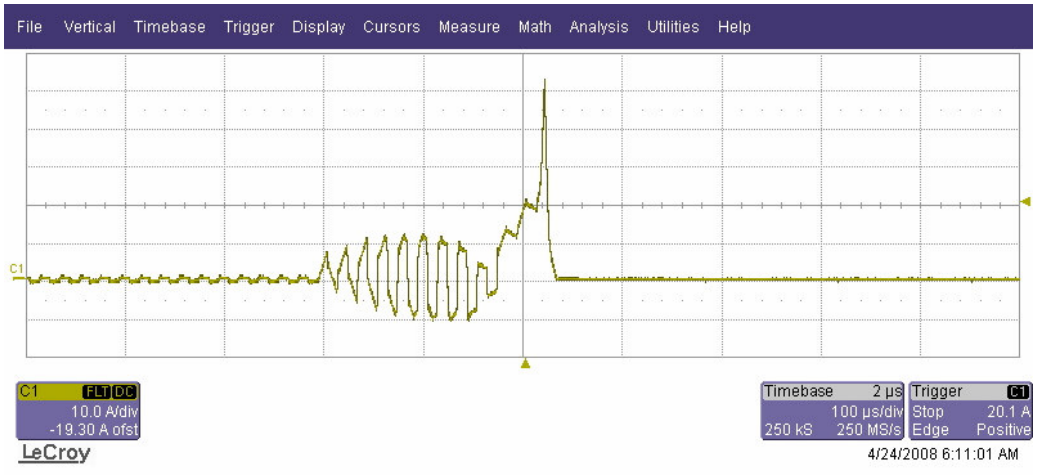

Figure 3.13 Excessive development of the DC/DC converter transformer primary current due to core saturation under transient conditions.

There are some solutions proposed to solve this problem in the literature. The simplest solution is to overdesign the transformer, but then the cost and the size significantly increase. Connecting a DC component isolation capacitor in series to the primary side of the transformer is a suggested method in some application notes but this method is impracticable for high power and high frequency applications. A flux balancing algorithm suggested in [29] is very easy to implement and cost free, therefore it is implemented in the control algorithm in this thesis and some minimal benefits are observed. In this method, when a step change in the duty cycle is demanded, before the utilization of the final duty cycle intermediate duty cycle utilization is suggested to limit the rate of change. Substituting this intermediate duty cycle into (3.23) yields

$$\Phi_{Offset} = \frac{v_g}{N_P} T \left(\frac{d_2}{2} - d_{int} + \frac{d_1}{2} \right) \tag{3.24}$$

The value of the intermediate duty cycle is determined by setting (3.24) to zero. Therefore, d_{int} becomes,

$$d_{int} = \frac{d_2 + d_1}{2} \tag{3.25}$$

To remove the flux offset the average value of consecutive duty cycles should be applied. This method responded well for small changes of consecutive duty cycles but was not successful for large step changes in the experiments. Therefore, the dynamical response of the system cannot be improved significantly. It is seen after a literature survey that an effective remedy of the problem is the current mode control. The peak value of transformer primary winding current is controlled in this control method. Small signal model of the FB–PS–ZVS DC/DC converter is derived for current mode control in [30]. This method is considered as future work in this thesis.

3.4 Performance Investigation of The FB–PS–ZVS DC/DC Converter by Means of Computer Simulations

In this section, the power stage and controller performance of FB–PS–ZVS DC/DC converter are investigated by means of computer simulations. The computer simulations are conducted utilizing the SIMPLORER software package as in the previous chapter. Circuit parameters utilized in the simulation model are the same as the laboratory prototype parameters. Since ZVS operation is verified in [Mutlu], only results involving the controller performance are given. The digital control algorithm is coded into equation blocks. The analog controller given in (3.17) is digitized with the Tustin approximation and its transfer function in z–domain is given in (3.26).

$$G_{vc}(z) = \frac{0.021z - 0.02}{z - 1} \tag{3.23}$$

The output of the equation block is the phase information and it is sent to the lagging leg PWM block. The PWM block consists of sawtooth carrier signal and state transition model block to generate gate signals of transistors in one leg. Sampling rate of digital control blocks is chosen same width as the switching period, 20μs. The simulation circuit diagram is given in Figure 3.14.

The parasitic components of IGBTs are very critical in the operation of the FB–PS–ZVS DC/DC converter; therefore the simulation model of IGBT should meet the electrical characteristics of the one utilized in the real system. In the simulation the model of Semikron SKM 100GB125DN IGBT is utilized and the electrical characteristics of the model are very similar to the IGBT utilized in the system.

Unless otherwise stated, the parameters given in Table 3.3 are utilized in the simulations. All other parameters not given in Table 3.3 are the same with the ones in Table 3.1 and Table 3.2.

Table 3.3 FB–PS–ZVS DC/DC converter simulation parameters

Parameter Description	Abbreviation	Value	Unit
Output Power	P_{OUT}	2500	W
Output Voltage	V_{OUT}	50	V
Input Voltage	V_g	400	V
Load Resistor	R_{LOAD}	1	Ω
Simulation Step Size	h	10	nsec
Sample Time for Digital Components	t_s	20	μsec

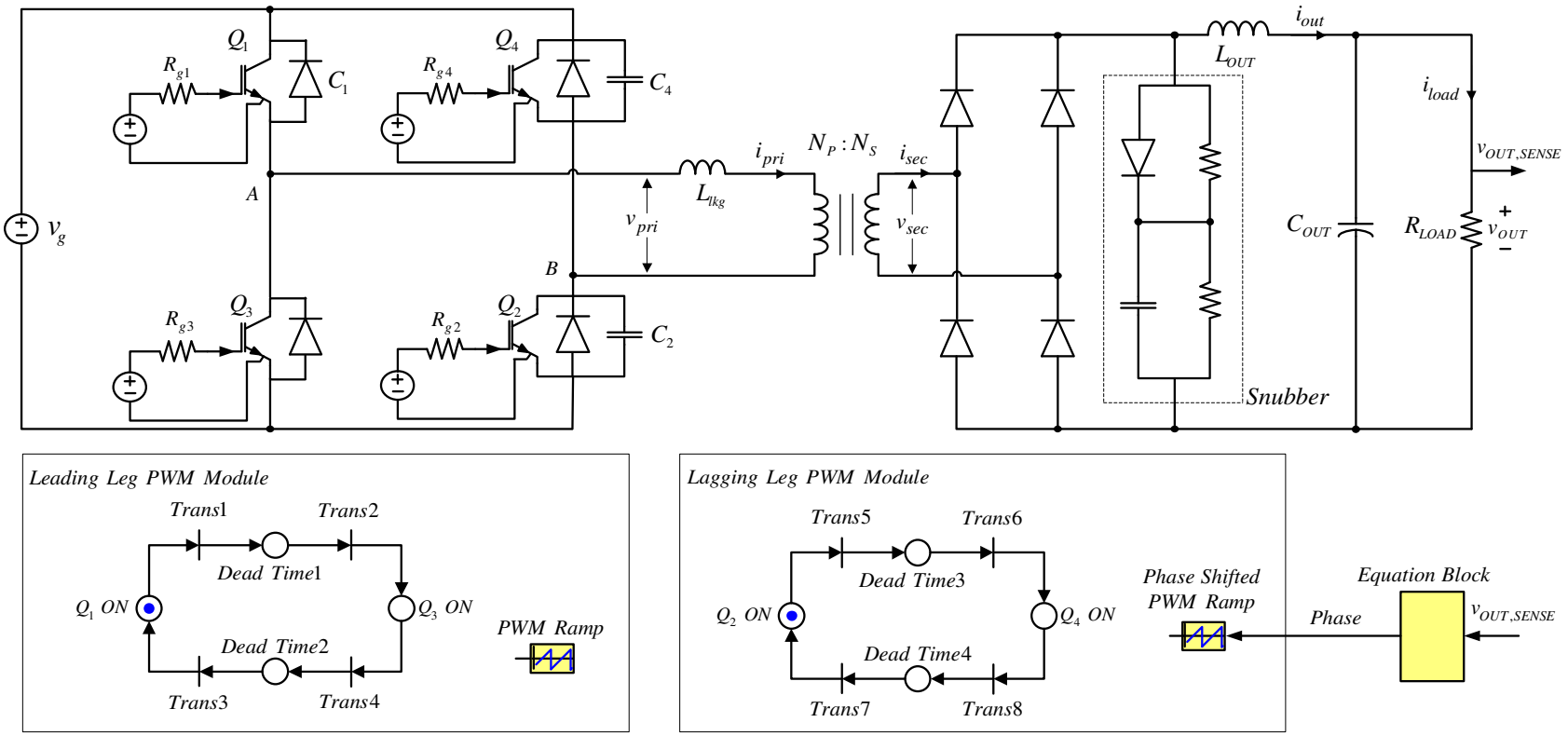

Figure 3.14 Simulation diagram of the FB–PS–ZVS DC/DC converter.

3.4.1 Simulation Results of FB–PS–ZVS DC/DC Converter

In this section, the waveforms illustrating the input, the output, and the controller performance of the converter are given. In Figure 3.15 the output voltage and the output current waveforms are given. The output voltage is set to 50V and it settles down to this value in about 7.5 milliseconds as shown in Figure 3.15(a). From Figure 3.15(b) it is given that the peak–to–peak ripple on the output current is about 2A.

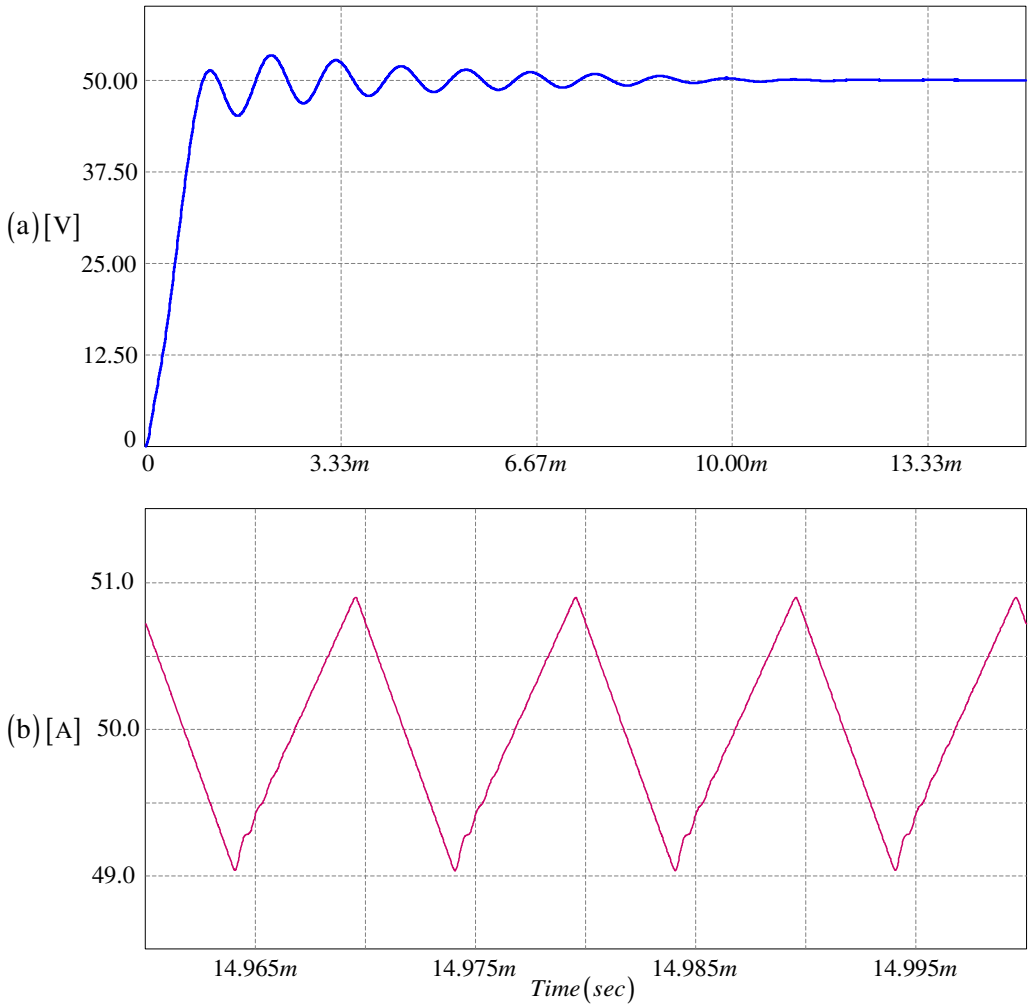

Figure 3.15 Output parameters of the FB–PS–ZVS DC/DC converter; (a) output voltage, (b) output current.

The primary voltage, the primary current and the secondary voltage waveforms of the isolation transformer are given in Figure 3.16. These waveforms are consistent with Figure 3.3. The effective duty cycle obtained from this figure is 0.5, which verifies (3.1). The high frequency oscillations that appear on the secondary side voltage are caused from the parasitic components of IGBTs and diodes, which are included in their simulation models.

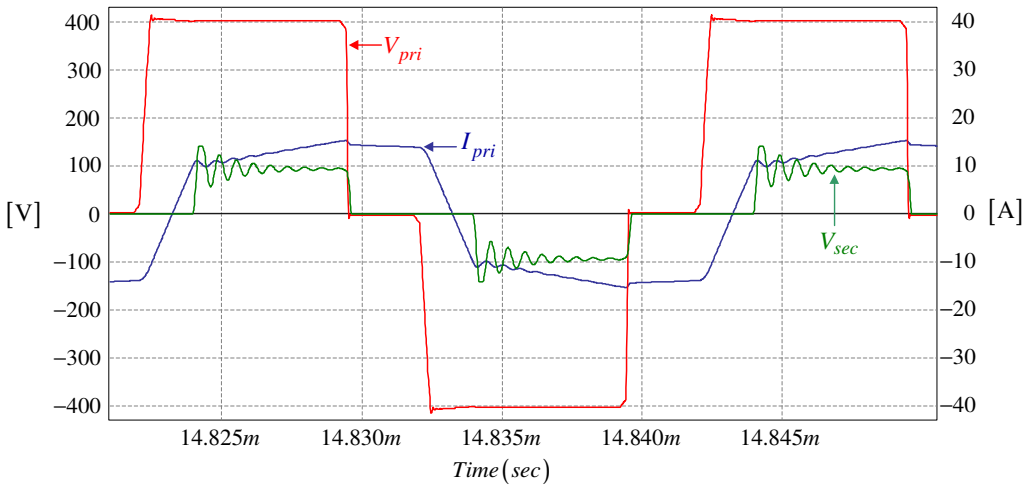

Figure 3.16 Isolation transformer waveforms, primary voltage (red), secondary voltage (green), and primary current (blue).

Simulation results involving investigating the performance of the controller are given in Figure 3.17. In order to investigate the dynamical performance of the controller, the output power is rapidly increased to 5 kW by connecting a 1 Ω resistor in parallel to the load resistor. The output voltage is suddenly decreased down to 20 volts due to this loading but settles back to 50 volts again in 3.5 milliseconds as can be seen from Figure 3.17. The dynamic performance could be improved by tuning the controller parameters but the transformer core flux imbalancing behavior imposes limitations on the controller design. Another simulation is performed to investigate the reference following capability of the controller. A step change is applied to the output voltage

reference and it is decreased from 50V to 30V rapidly. The reference command change is indicated with red waveform in Figure 3.17(b). The controller immediately responds this change and the output voltage tracks the reference. Digital control provides to the user the flexibility for changing output voltage. Changing the reference command is sufficient to obtain any value of output voltage within the design range.

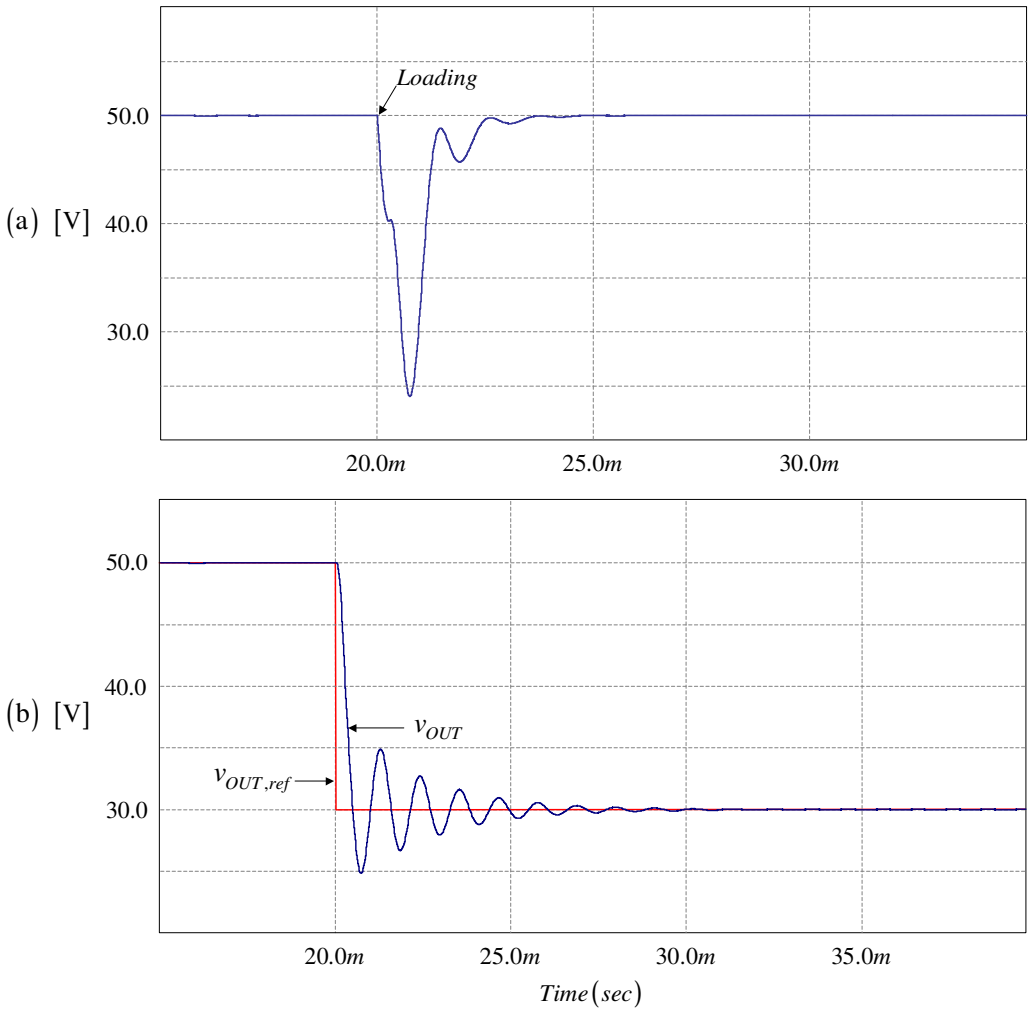

Figure 3.17 Controller performance of the FB–PS–ZVS DC/DC converter: (a) output voltage under 100% loading condition, (b) reference tracking capability of the output voltage.

The effect of the flux balancing algorithm, which is explained in section 3.3, is investigated with computer simulations. Same simulations are performed with and without applying this algorithm and the results are given in Figure 3.18. In Figure 3.18(a) the primary current waveform of the isolation transformer without application of the algorithm is given. An offset on the primary current is developed temporarily but removed later because of the selection of the suitable controller parameters. The effect of the algorithm is indicated in Figure 3.18(b). In this figure primary current waveform without application of the algorithm is given. The flux offset is insignificant when compared to the former situation.

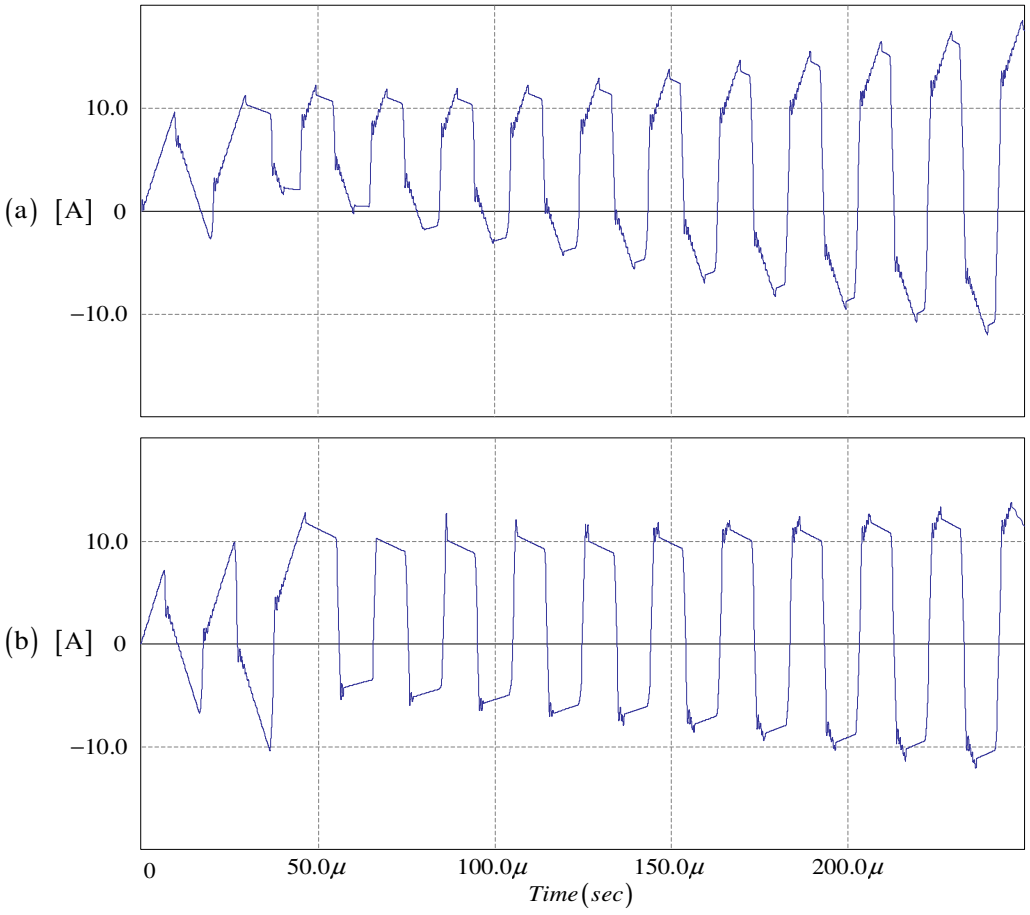

Figure 3.18 Performance improvement of the flux balancing algorithm during transients, (a) primary current development without the algorithm and (b) with the algorithm.

3.5 Experimental Results of the FB–PS–ZVS DC/DC Converter

The performance of the FB–PS–ZVS DC/DC converter is experimentally investigated in this section. The experiments are conducted on the laboratory prototype of the converter. The photographs of the prototype are given in Appendix C.

The input 400V DC voltage is supplied by rectifying the output of a three phase variable transformer with a three–phase diode rectifier. A three–phase 20A automatic fuse and a 25A circuit breaker are connected to the output of the variable transformer for safety purpose. In order to obtain a smooth DC voltage at the output of the three–phase diode rectifier, a capacitor bank with 1100μF total capacitance is connected in parallel to the diode rectifier. A 20A fast fuse is inserted between the positive terminal of the diode rectifier and the capacitor bank in order to protecting the system from hazardous short circuit situations. The DC bus is constructed by utilizing a planar structure to minimize the parasitic inductances. Two aluminum plates are connected to positive and negative terminals of the capacitor bank and the inverter and an insulation material is inserted between them. The IGBT modules of inverter are mounted on a 99AS model heatsink which is cooled by an AC fan. The high frequency transformer and the external inductor are directly connected to the inverter output. The design of the high frequency transformer is explained in detail in [Mutlu]. An RCD type snubber is employed at the output of the high frequency diode rectifier at the secondary side to suppress oscillations on the secondary voltage of the transformer. An LC filter is connected to the output of the diode rectifier for smoothing the output DC voltage. The structure of the experimental setup is illustrated by block diagrams in Figure 3.19.

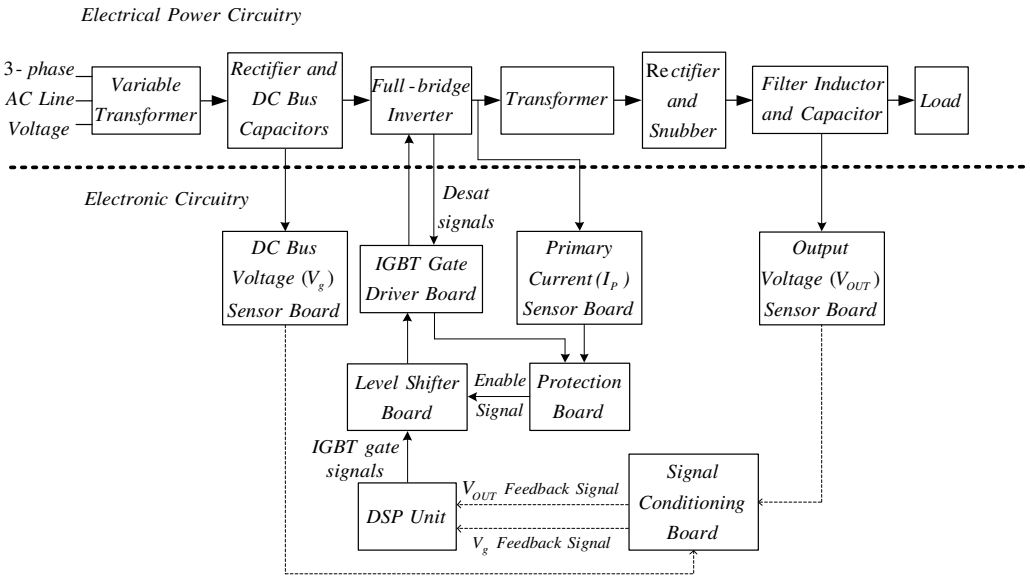

Figure 3.19 The structure of experimental prototype.

The waveforms verifying the ZVS operation of the converter are given in [Mutlu]. Therefore, these results are not covered in this study and only the waveforms illustrating the circuit and controller performances are included. The same experiments are performed at two different output power levels: 2.5 kW and 1.25 kW. In the experiments, the output voltage is set to 48V in order to show that the DC/DC full bridge converter can be utilized as a telecom power supply.

3.5.1 Experimental Results at 2.5 kW Load Power

In this section results of experiments at 2.5 kW load power are given. The output voltage of the inverter stage, the primary current and the secondary voltage waveforms of the transformer are shown in Figure 3.20. The load voltage and the load current waveforms are shown in Figure 3.21.

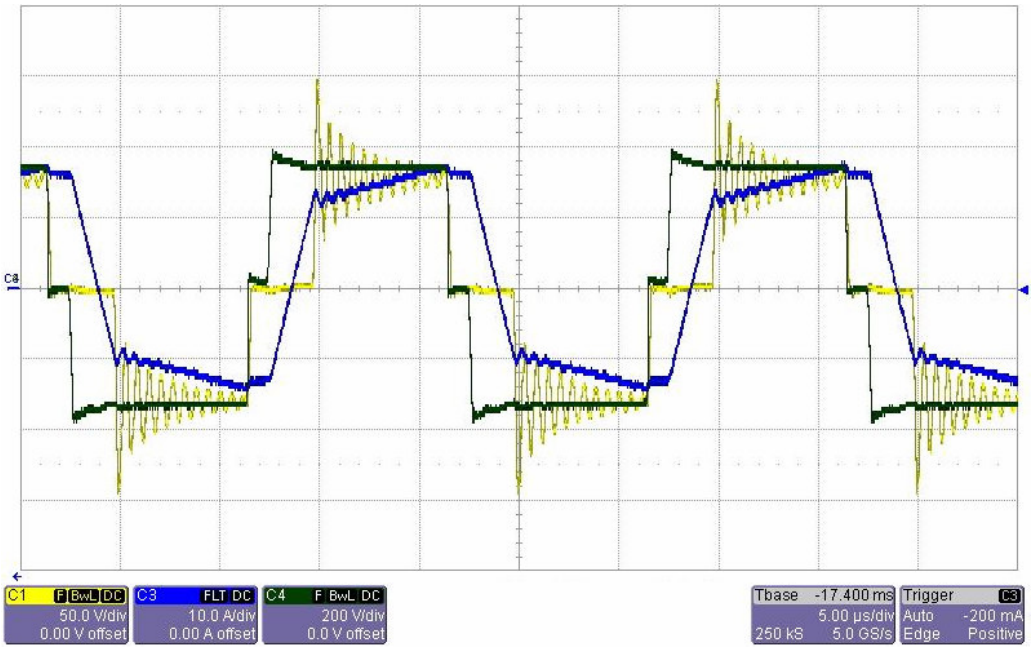

Figure 3.20 The inverter output voltage (green), transformer primary current (blue), and transformer secondary voltage (yellow) at 2.5 kW output power. (Scales: 200V/div, 10A/div, 50V/div).

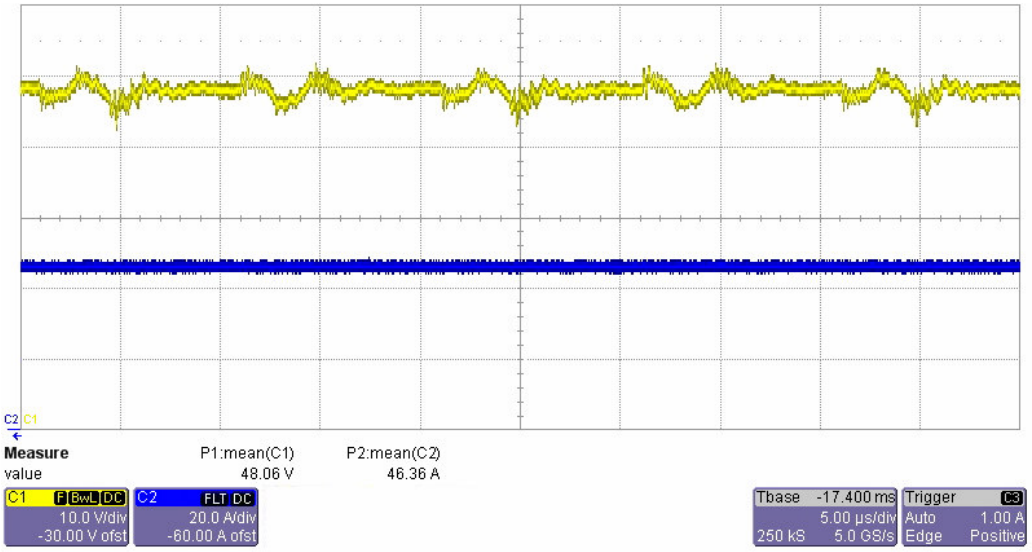

Figure 3.21 The load voltage (yellow) and the load current waveforms at 2.5 kW. (Scales: 10V/div, 20A/div).

The waveforms given in Figure 3.20 are consistent with the simulation results. The secondary voltage of the transformer oscillates due to the resonance between the secondary referred transformer leakage inductance, the additional external inductance, the high frequency rectifier junction capacitances, and transformer winding capacitance. The mean value of the load voltage is 48.06 V as can be observed from Figure 3.21. This value is very close to the target output voltage value, 48 V. There is a high frequency oscillation on output the voltage with peak–to–peak amplitude of 5 V. The main reason of this oscillation is the loss of duty cycle in secondary part of the circuit and the resonance between the secondary windings of the transformer and parasitic components of secondary diode bridge rectifier. Since the secondary diode rectifier terminals are shorted in mode3 and mode4, power cannot be transferred from input to output and therefore the output voltage is decreased. The amplitude of the oscillation can be reduced by utilizing a higher value output filter capacitor.

3.5.2 Experimental Results at 1.25 kW Load Power

The same experiments are performed at 1.25kW load power to observe the performance of the converter at different power levels. In Figure 3.22 the inverter output voltage, the transformer primary current, and the transformer secondary voltage waveforms are given. The frequency and peak–to–peak magnitude of the secondary voltage are almost same with the previous experiment results. The primary duty cycle is reduced due to the reduced primary current, but the secondary duty cycle is kept constant because of the unchanged load voltage. The load voltage and the load current waveforms are given in Figure 3.23. The mean load voltage accuracy is high as in the previous experiment.

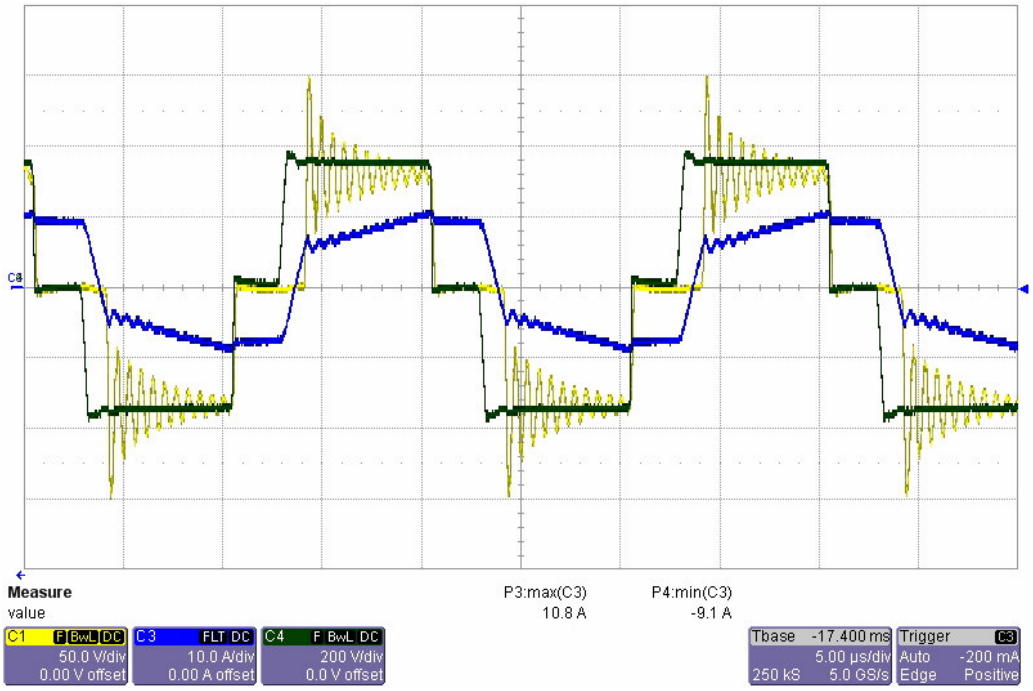

Figure 3.22 The inverter output voltage (green), transformer primary current (blue), and transformer secondary voltage (yellow) at 1.25kW output power. (Scales: 200V/div, 10A/div, 50V/div).

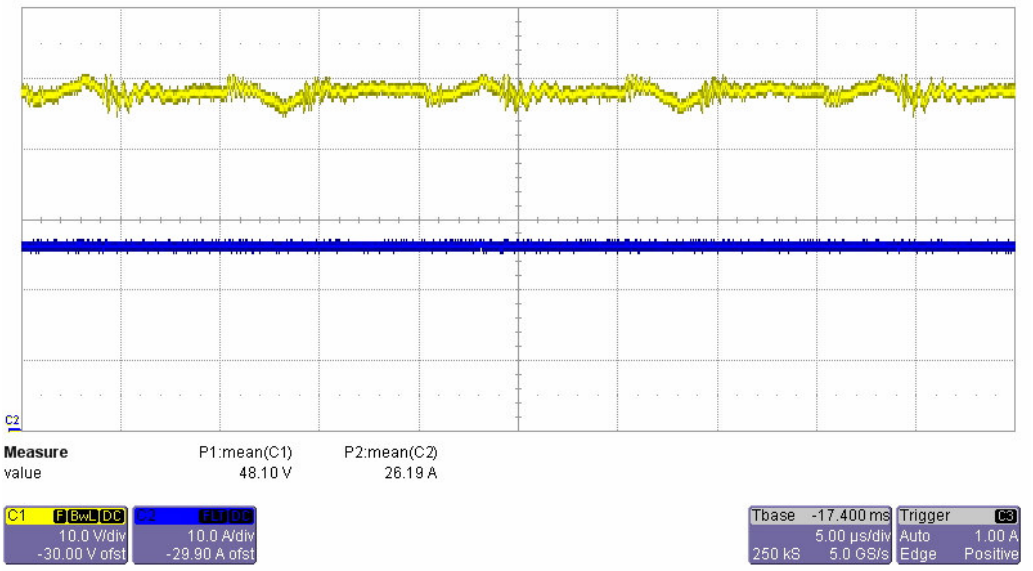

Figure 3.23 The load voltage (yellow) and the load current waveforms at 1.25 kW load. (Scales: 10V/div, 10A/div).

3.5.3 Controller Performance

In order to observe the performance of the designed controller, some experiments for investigating the dynamical response regarding the load disturbance rejection and reference tracking ability have been performed. In Figure 3.24 the controller performance under load removal condition is investigated. The output current is reduced from 60 A to 40 A rapidly. A small fluctuation occurs on output voltage and then it settles to its steady–state value in about 1 millisecond.

In Figure 3.25 the dynamical response of the controller under the loading condition is investigated. The output current is rapidly increased from 30A to 60A. The output voltage oscillates with the maximum amplitude of 8 V and settles to its steady–state value in about 2.5 milliseconds. These two experiments show that controller performance is satisfactory at the loading and the load removal conditions. Therefore, the load disturbances are well rejected by the controller.

In Figure 3.26, the reference tracking ability of the output voltage is illustrated. The voltage reference signal (shown with red line in the figure) is rapidly changed from 30 V to 48 V when a 1 Ω resistive load is connected to the output terminals. The output voltage oscillates with maximum peak–to–peak amplitude of about 8V and settles to 48V in about 4 ms. One important feature of the digital control is shown with this experiment: flexibility. The controlled variable of the system (in this case the output voltage) can easily be adjusted according to operational requirements by simply modifying the reference signal. The output voltage of the prototype converter is adjustable within the range from 10 V to 55 V.

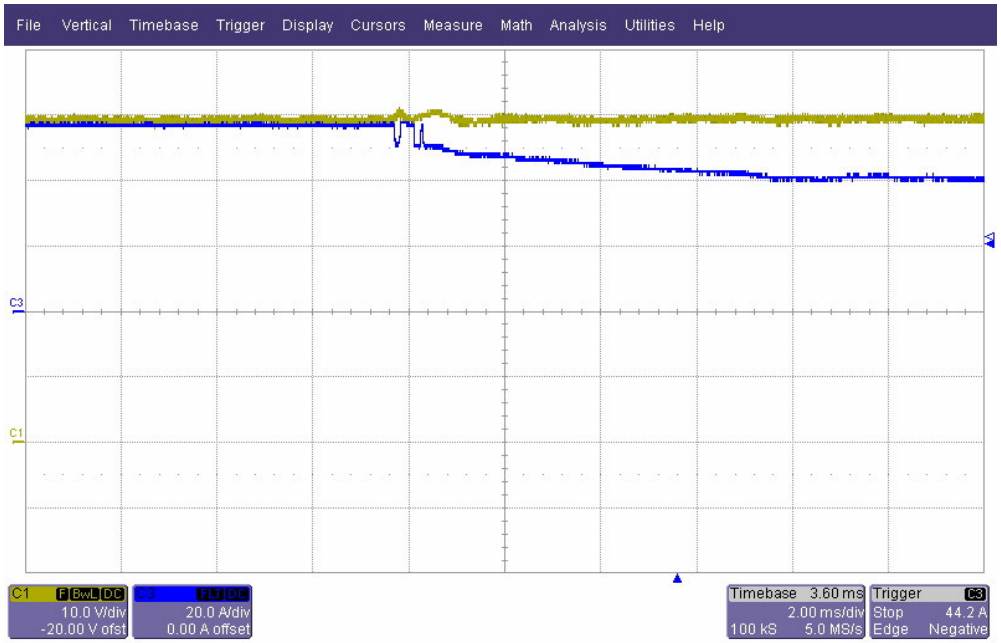

Figure 3.24 The dynamical response of the controller under load removal condition, output voltage (yellow), load current (blue). (Scales : 10 V/div, 20 A/div, 2 ms/div).

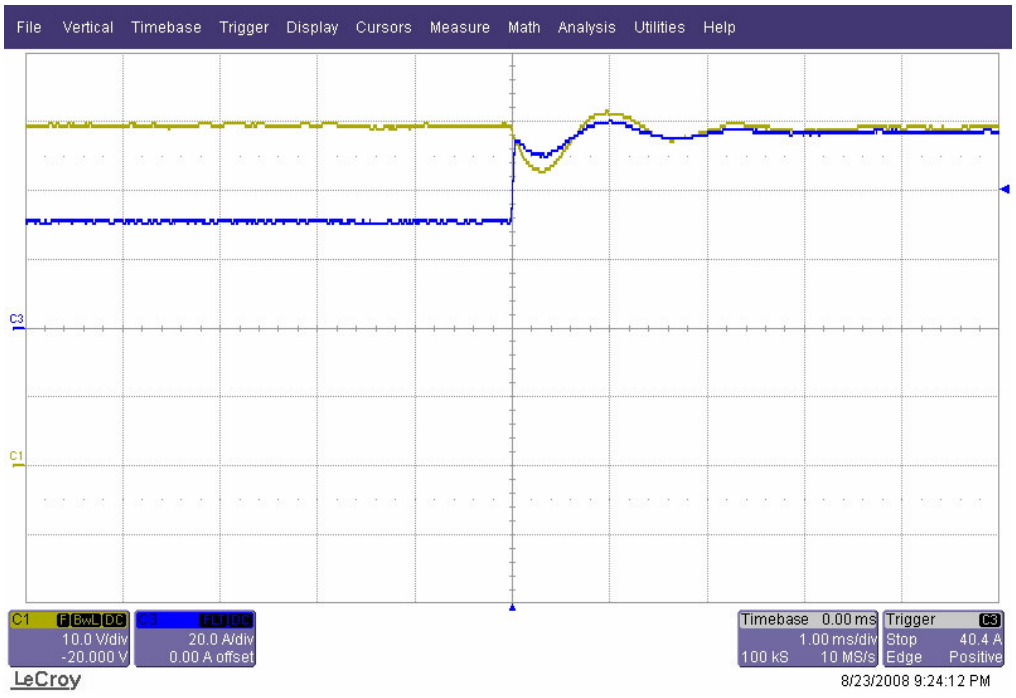

Figure 3.25 The dynamical response of the controller under loading condition, output voltage (yellow), load current (blue). (Scales : 10V/div, 20A/div, 1ms/div).

Figure 3.26 Reference tracking capability of the output voltage, output voltage (yellow), load current (blue), reference signal (red). (Scales : 10V/div, 20A/div, 2ms/div).

3.6 Chapter Conclusion

In this chapter the isolated full bridge topology was briefly explained, the phase shifted PWM and the zero voltage switching concepts were introduced. The small signal model and duty cycle–to–output voltage transfer function of the converter were derived. The parameters of the voltage controller were calculated according to the SSM of the converter. The controller and system performance have verified by means of computer simulations and laboratory experiments. Experiments were performed on the laboratory setup and the design parameters of this prototype were given. The flux imbalancing phenomenon of the high frequency isolation transformer was mathematically analyzed and some methods to overcome this problem were introduced. A flux balancing algorithm explained in [29] was utilized and the positive effect of the method is shown by computer simulations.

CHAPTER 4

THE MANUFACTURING AND EXPERIMENTAL PERFORMANCE VERIFICATION OF THE TWO STAGE ISOLATED AC/DC POWER SUPPLY WITH HIGH INPUT POWER FACTOR

4.1 Introduction

In the previous two chapters the interleaved boost PFC and the FB–PS–ZVS DC/DC converters were introduced and their designs were explained. The PFC converter is not functional when it is utilized alone; because the output voltage is higher than the input line voltage due to the boost topology characteristic, there is a significant second harmonic ripple on it, and the control bandwidth of the output voltage is very low (the output voltage is prone to load and line disturbances). Similarly the FB–PS–ZVS DC/DC converter is not very practical when it is utilized alone; because the input voltage of the converter that is manufactured in this study is 400V and this voltage cannot be supplied by a single phase AC grid via passive rectifiers. As done in [5], with a three-phase passive rectifier solution, the three–phase AC line is adjusted with a three–phase variable transformer and converted to 400V DC voltage with a three–phase uncontrolled rectifier. This makes the system bulky and unpractical. Also harmonic components are contributed to the line from the converter due to the non–linear characteristics of the converter. Therefore, a better choice involves active PFC at the input stage. For this purpose, these two separate converters are connected back–to–back in order to obtain adjustable DC voltage with good dynamic performance while supplying the input voltage from a single phase AC grid and providing high power factor and low THD on the power line side. Also the output DC voltage is provided to be isolated from input AC line voltage with the

utilization of high frequency transformer. In this chapter overall system is introduced, integration of the input and the output stages are explained and experimental results are presented.

4.2 The Structure of The AC/DC Converter

The integration process of two different systems is a somewhat complicated task. The electronics noise that is generated by one system may interfere with the other system. Also a malfunction occurred in one system may cause hazardous failures in the other system. In the experimental verification stage of this thesis, during the integration process of the two individual converters, some additional units were connected to the circuit in order to minimize the noise interference between two systems and to isolate the two systems from each other when an operational failure occurs in one system. The electrical circuit schematic of the overall two stage isolated AC/DC converter prototype is illustrated in Figure 4.1. The two converters are linked together with an EMI filter consisting of two high frequency bypass capacitors and a common mode choke. The common mode noise of each system is prevented from interfering with the other system by the common mode choke. The common mode choke forms a high impedance path for high frequency common mode noise. Also there is a differential filter between two systems consisting of the serial leakage inductance of the common mode choke and the bypass capacitors. The differential mode noise generated by the individual converters is damped with this filter. It is seen from Figure 4.1 that there are also some protection components in order to protect the circuit when a malfunction occurs. An automatic fuse and a circuit breaker are connected in the input AC mains side. The input connection can be disconnected manually or automatically with these components. Since the automatic fuse cannot react fast, two fast fuses are connected in series to the line and in front of the DC bus capacitors of the output stage. When an excessive current flows in the PFC stage, the fast fuse interrupts the line and the input power is disconnected.

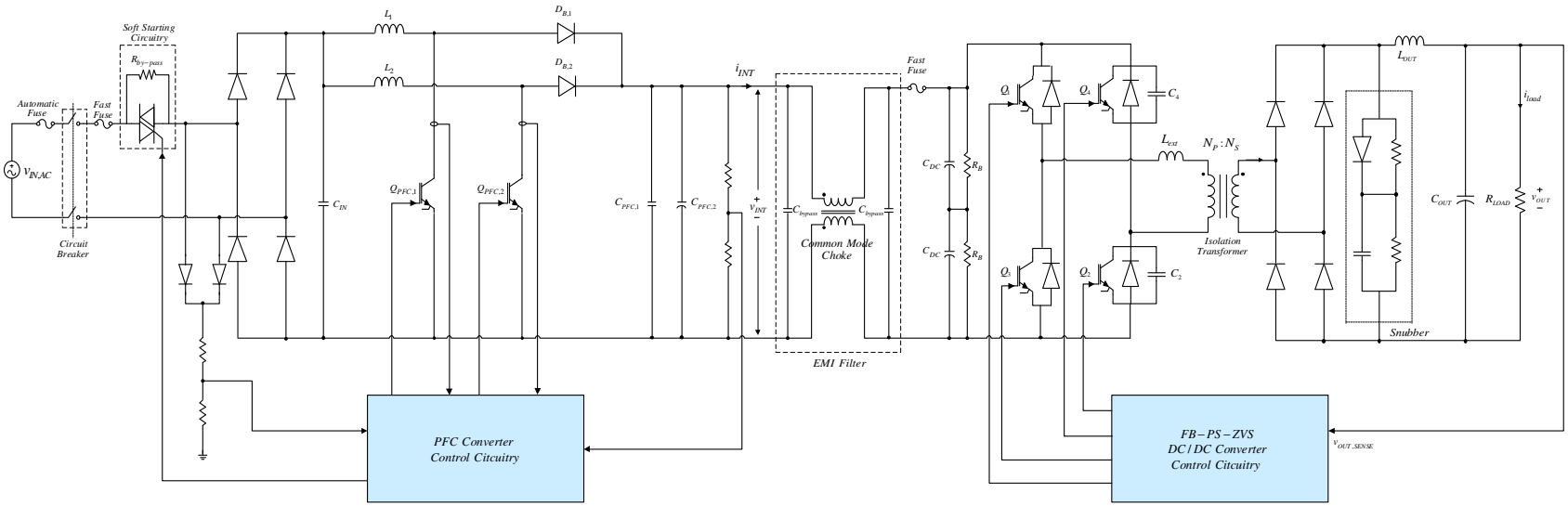

Figure 4.1 The electrical power circuitry of the overall two stage isolated AC/DC converter with high input power factor.

In the start up stage, the output capacitor of the input stage and the input DC bus capacitors of the output stage are fully discharged. Therefore, application of the line voltage to the input causes excessive inrush current that flows through the power circuit components. Therefore, the start up transient should be slowed down to limit the start up (inrush) current. A triac is connected in series with the line and a bypass resistor is connected in parallel to the triac to slow down the start up [31]. The output capacitor voltage of the input stage is measured. The triac is in the off state provided that the output capacitor voltage is below the predetermined voltage level; therefore the input current is forced to flow through the bypass resistor. The input current is limited with this resistor. The photographs of the laboratory prototype of two stage isolated AC/DC converter with high input power factor are presented in Figure 4.2 and Figure 4.3.

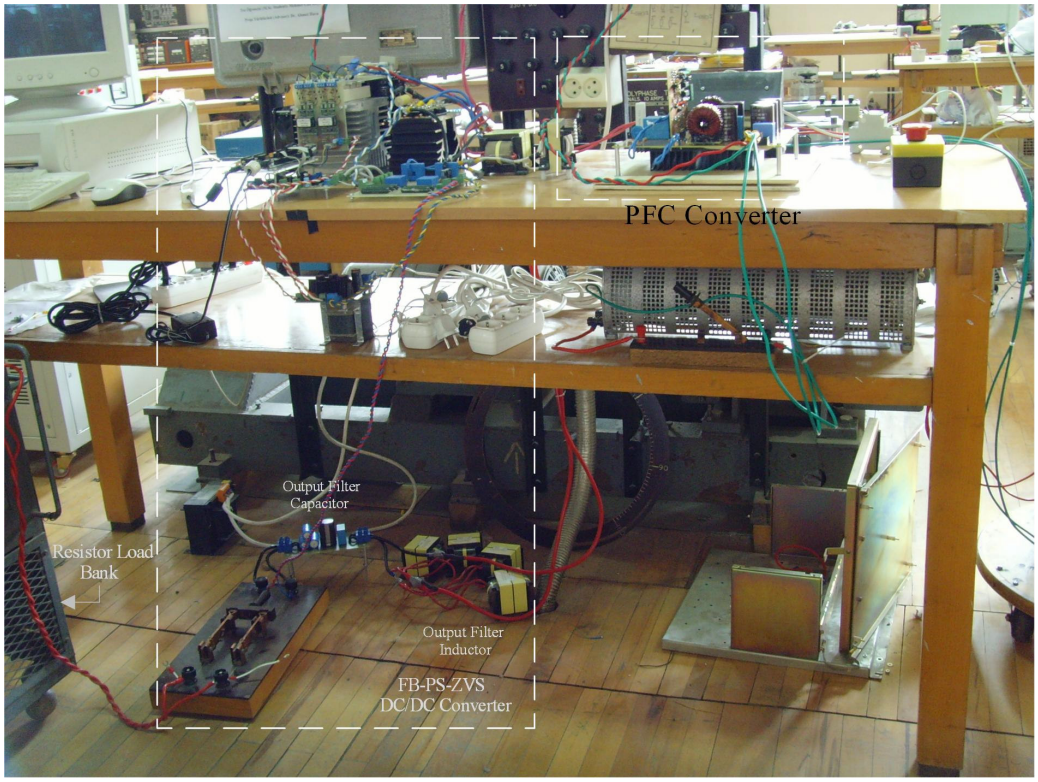

Figure 4.2 Laboratory prototype system set–up photograph of the two stage isolated AC/DC converter with high input power factor.

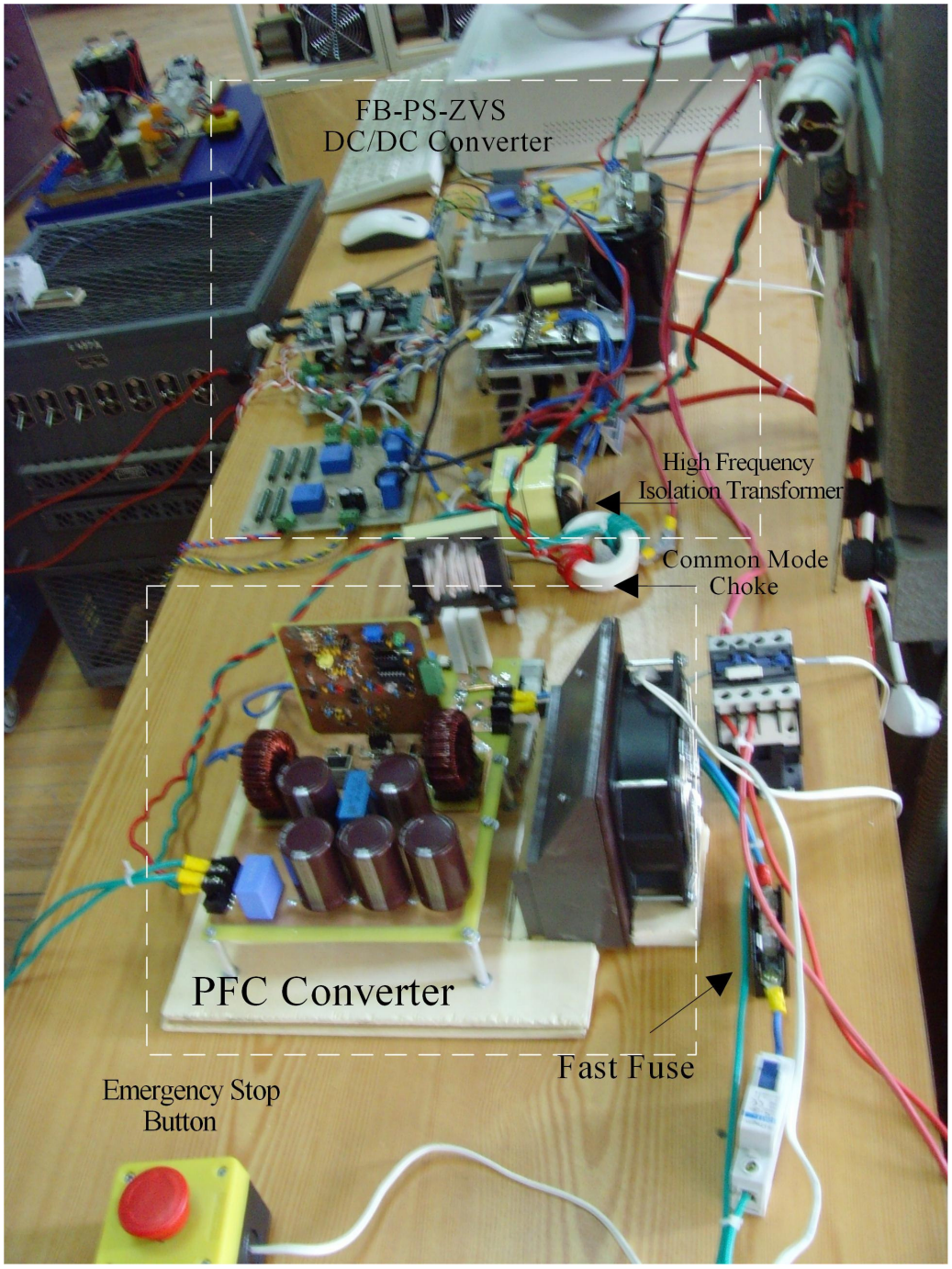

Figure 4.3 Laboratory prototype of two stage isolated AC/DC converter with high input power factor (converter system top view).

4.3 Experimental Results of The Two Stage Isolated AC/DC Power Supply With High Input Power Factor

Several experiments are conducted on the laboratory setup explained in previous sections in order to investigate the overall system performance. Two sets of experiments are performed with two different output power levels: 2.5 kW and 1.25 kW. In this section the results of these experiments are presented.

4.3.1 Experimental Results at 2.5 kW Output Power

The waveforms of the voltages and currents at the input, output, and intermediate levels, and the input power quality data at 2.5 kW output power are given in this section. In Figure 4.4, the waveforms illustrating the input and output performances of the overall system are given. As it can be seen from the figure, the input current tracks the input voltage, therefore high input power factor is provided. The output voltage of the overall system is 48 V DC voltage but it can be adjusted to any value between 10 V and 55 V simply by changing the output voltage reference signal. The average input power of the system is measured as 2964 W and average the output power is measured as 2570 W. Then the overall efficiency is calculated as 86.7%.

In Figure 4.5, detailed views of the AC component output voltage and the current waveforms are shown in order to observe the ripple magnitudes. The peak–to–peak amplitude of the output voltage ripple is about 10V. This amplitude can be reduced by the utilization of bigger output filter capacitors.

The output voltage and output current of the PFC converter are defined as the intermediate voltage and the intermediate current, and their waveforms are given in Figure 4.6. The detailed views of these waveforms are shown in Figure 4.7. It is observed from this figure that the intermediate voltage and the current have second harmonics contribution.

In Figure 4.8, the input power factor measured by the Fluke 43B power quality analyzer is given. The input power factor is unity as can be seen from the figure. The harmonic contribution into the input current is illustrated in Figure 4.9. There are third and fifth harmonics on the fundamental, but their magnitude are very low when compared with the fundamental. The line current THD is measured as 3.5% which is in the range of design goals.

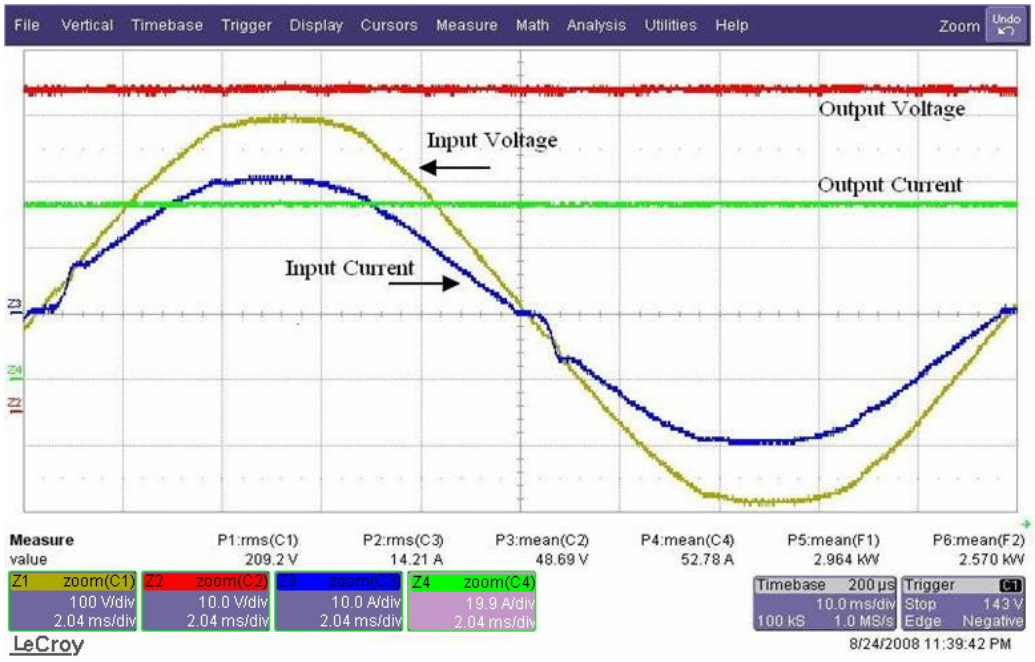

Figure 4.4 The input voltage (yellow), input current (blue), output voltage (red), and output current (green) waveforms of the two stage AC/DC converter at 2.5 kW output power (Scales: 100 V/div, 10 A/div, 10 V/div, 19.9 A/div).

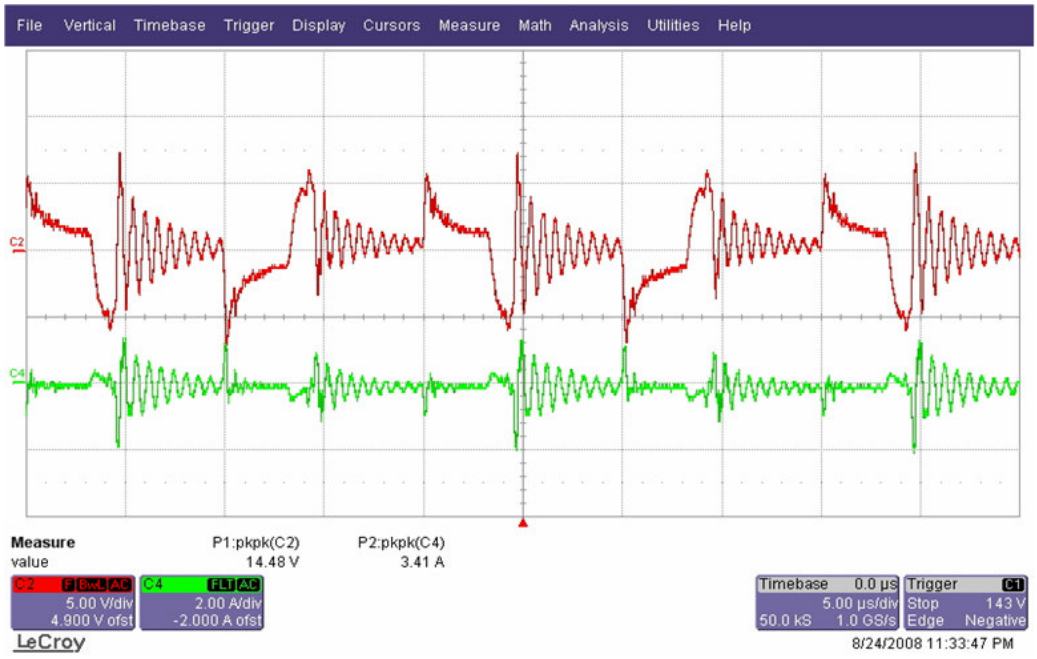

Figure 4.5 Detailed views of the output voltage (red), and output current (green) AC component waveforms at 2.5 kW output power (Scales: 5 V/div, 2 A/div).

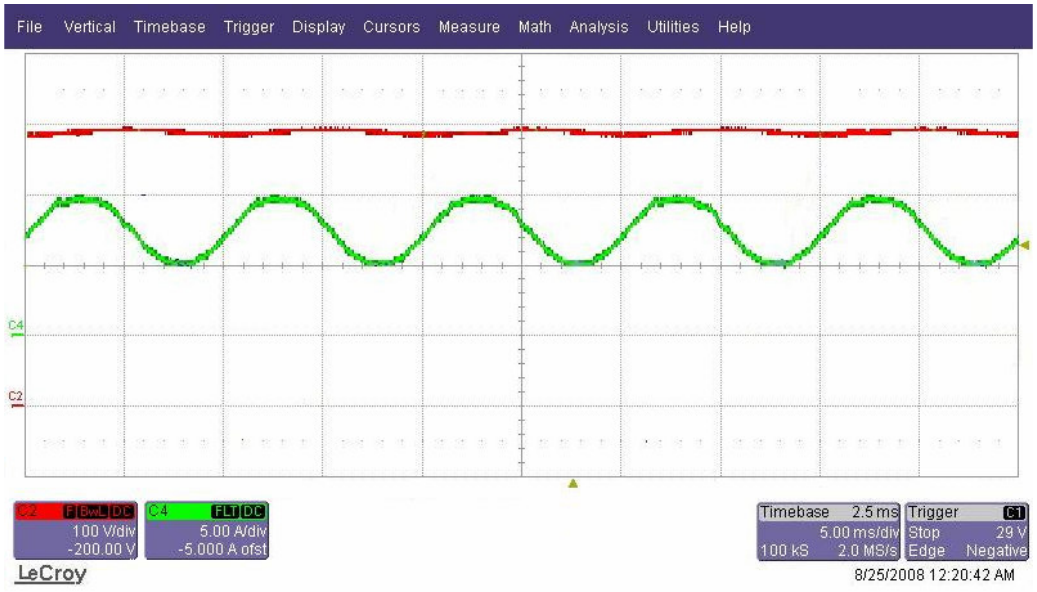

Figure 4.6 The intermediate voltage (red) and current (green) waveforms at 2.5 kW output power (Scales: 100 V/div, 5 A/div, Time: 5 ms/div)

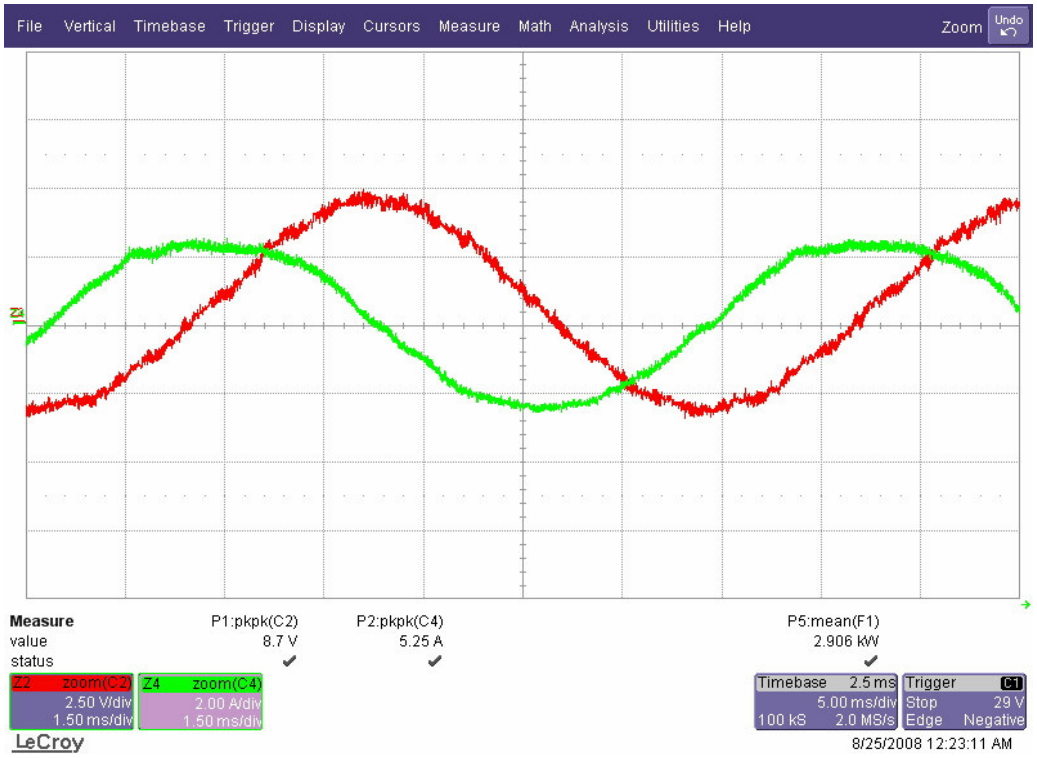

Figure 4.7 Detailed views of the intermediate voltage (red) and intermediate current (green) waveforms at 2.5 kW output power (Scales: 2.5 V/div, 2 A/div, Time: 5 ms/div).

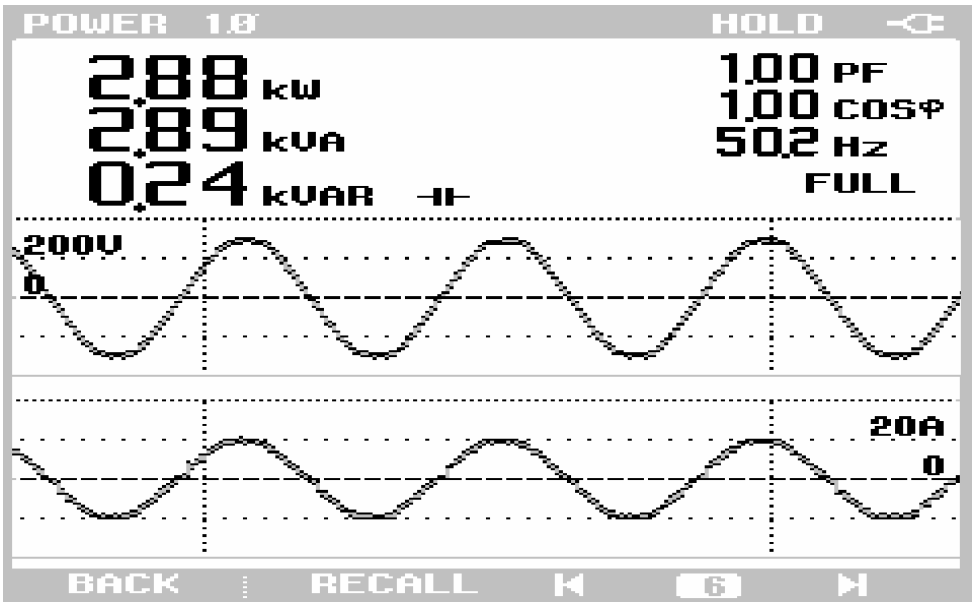

Figure 4.8 The input power factor information obtained at 2.5 kW output power.

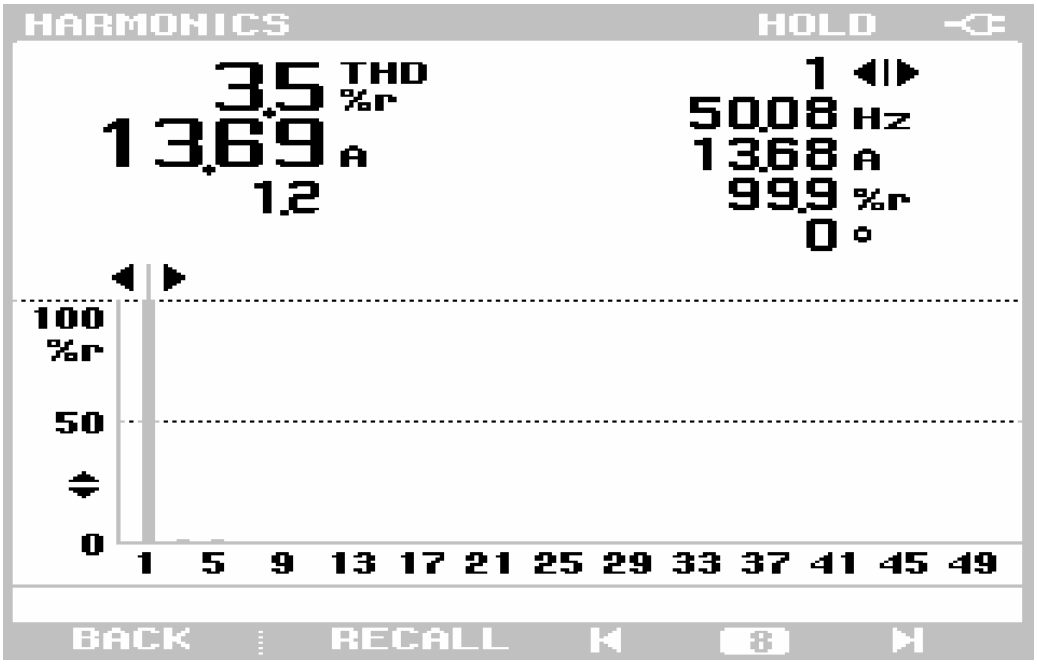

Figure 4.9 The input current harmonics and THD information obtained at 2.5 kW output power.

4.3.2 Experimental Results at 1.25 kW Output Power

The same experiments with the previous section are performed under 1.25 kW output power condition. In Figure 4.10 the input and the output voltage and current waveforms are given. The input current tracks the input voltage so high input power factor is obtained. The output voltage of the overall system is kept constant after the load is changed. The average input power of the system is measured as 1452 W and the average output power is measured as 1248.6 W. Then the overall efficiency is calculated as 86%, system efficiency does not change drastically with the change of the output power.

In Figure 4.11, detailed views of the output voltage and the current waveforms are shown in order to observe the ripple magnitudes. The peak–to–peak amplitude of the output voltage ripple is about 10V and is not affected by the output power level.

The intermediate voltage and current waveforms are given in Figure 4.12. The detailed views of these waveforms are shown in Figure 4.13. The second harmonic contribution and the phase shift can be observed as in the previous experiment results.

In Figure 4.14, the input current and voltage waveforms measured by the power quality analyzer are given. The input power factor is measured as 0.99 with the analyzer. This value is only slightly smaller than that of the previous experiment. The harmonic contribution into the input current is illustrated in Figure 4.15. The spectrum of the harmonic contribution is extended as can be seen from the figure. Again their magnitudes are very low with compared to the fundamental component. THD is calculated as 6.6% in this case, which is worse than the previous. In second and third chapters experimental results of individual converters were given. When the results given in these chapters are compared with the ones given in this chapter, it is seen that the results are consistent.

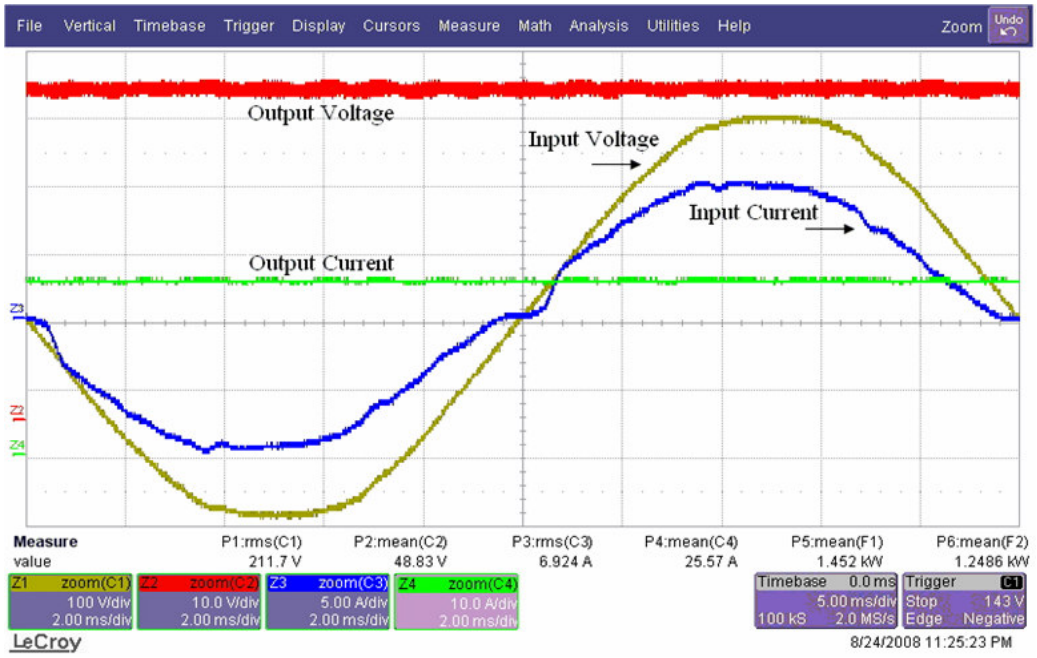

Figure 4.10 The input voltage (yellow), input current (blue), output voltage (red), and output current (green) waveforms of the two stage AC/DC converter at 1.25 kW output power (Scales: 100 V/div, 5 A/div, 10 V/div, 10 A/div).

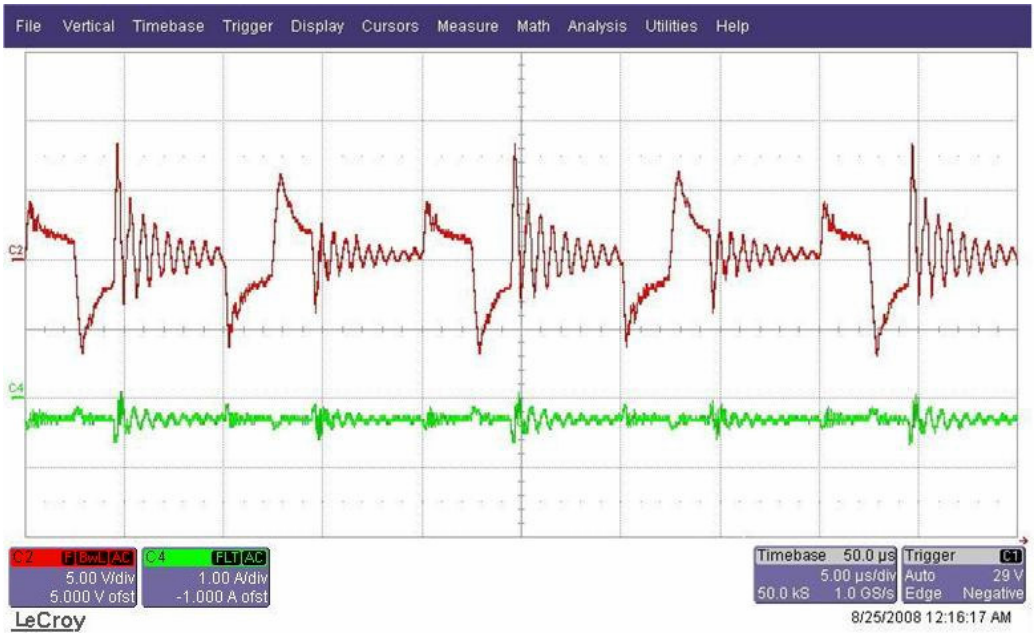

Figure 4.11 Detailed views of the output voltage (red), and output current (green) AC component waveforms 1.25 kW output power (Scales: 5 V/div, 1 A/div).

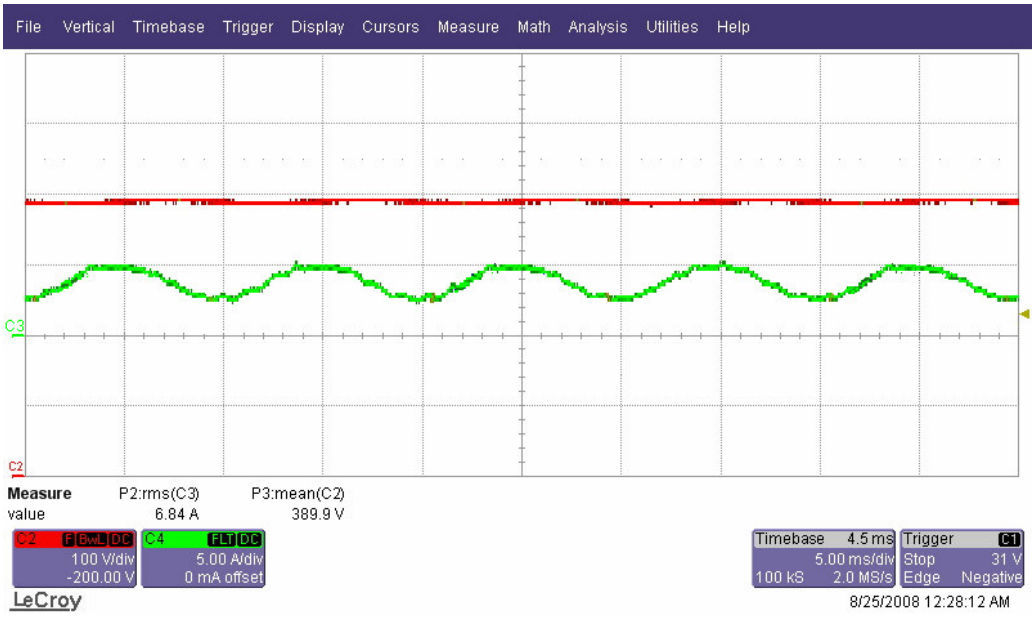

Figure 4.12 The intermediate voltage (red) and current (green) waveforms at 1.25 kW output power (Scales: 100 V/div, 5 A/div, Time: 5 ms/div).

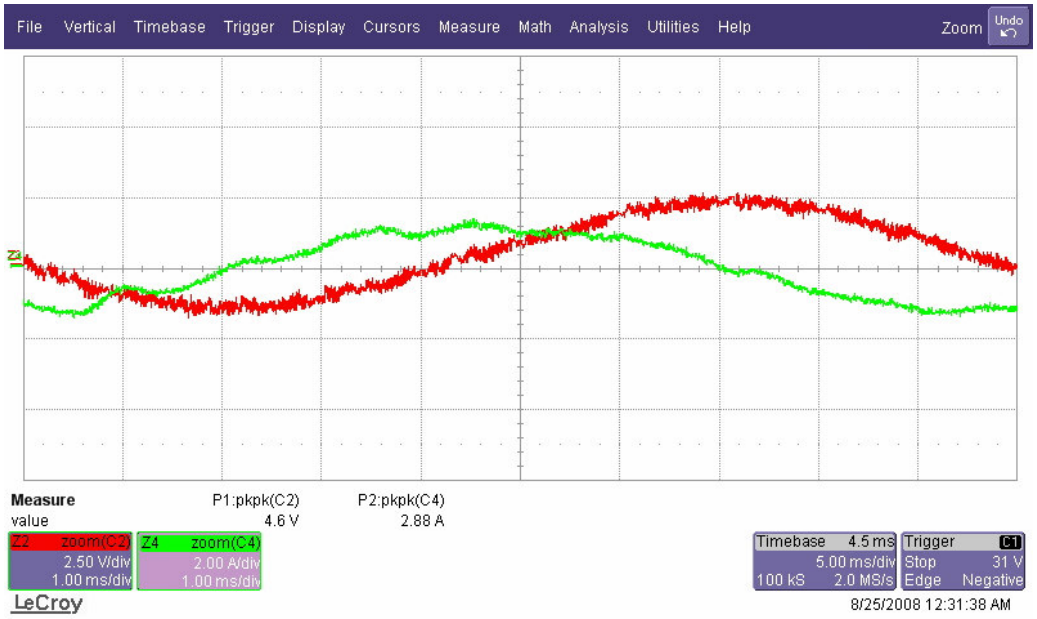

Figure 4.13 Detailed views of the intermediate voltage (red) and intermediate current (green) waveforms at 1.25 kW output power (Scales: 2.5 V/div, 2 A/div, Time: 5 ms/div).

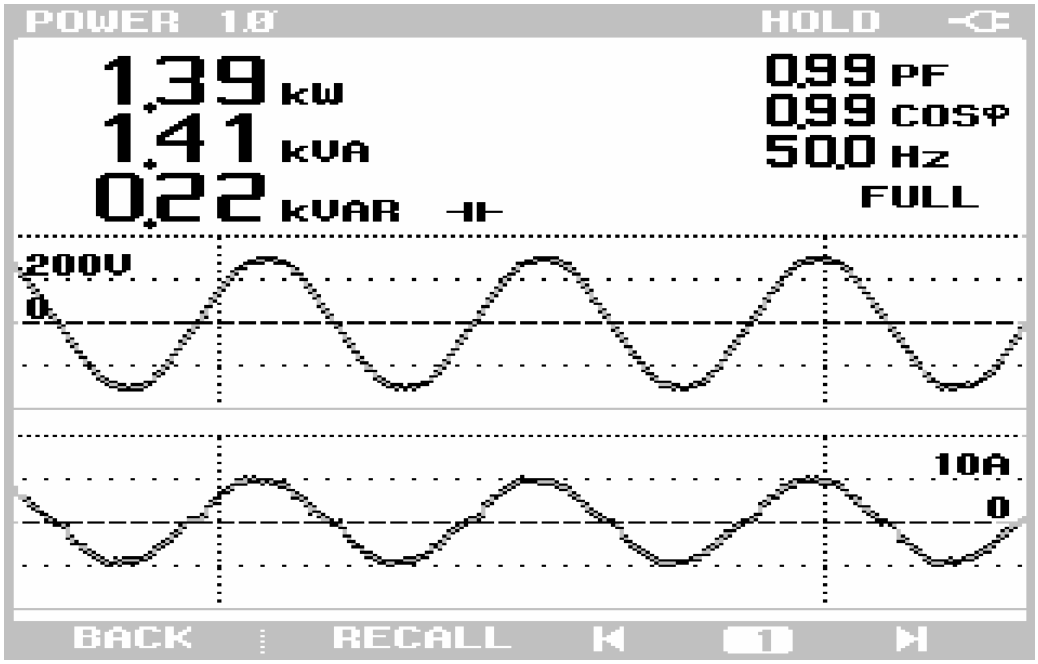

Figure 4.14 The input power factor information obtained at 1.25 kW output power.

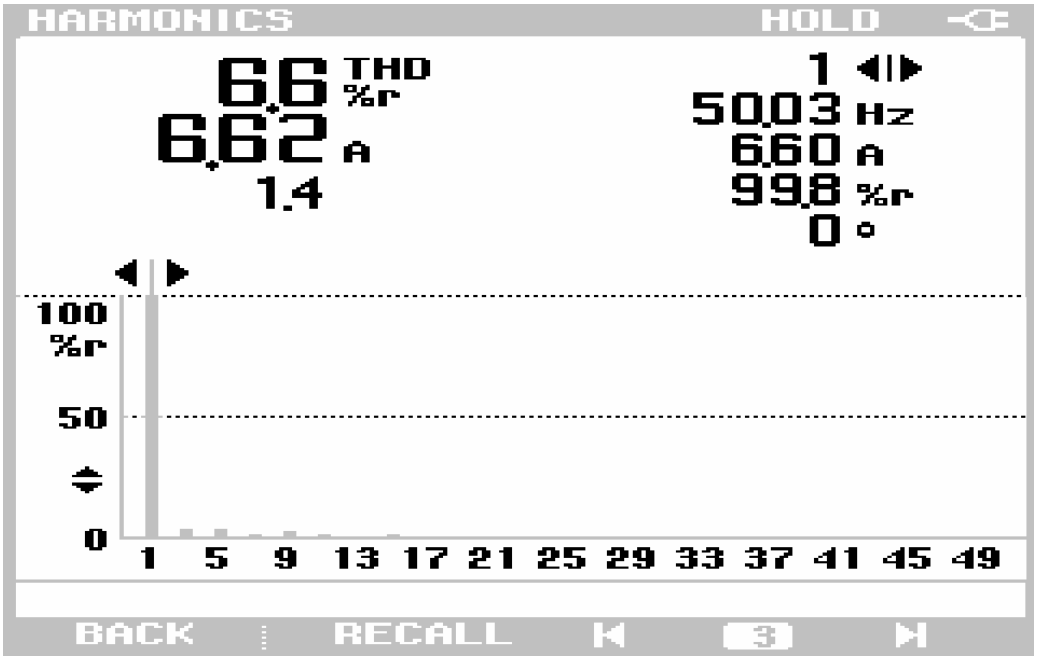

Figure 4.15 The input current harmonics and THD information obtained at 1.25 kW output power.

4.4 Chapter Conclusion

In the second and third chapters the operation and the design of the two–phase interleaved PFC converter and the FB–PS ZVS DC/DC converter were explained. The results of the experiments conducted on laboratory prototypes of these converters are given in this chapter. In order to manufacture an isolated AC/DC converter with high input power factor and digitally controllable output voltage, these two prototype converters were integrated. In this chapter, the integration process was summarized; potential problems caused by the integration and solution methods were discussed. Several experiments were conducted on the AC/DC converter and the results were presented. Strong correlation between theory, simulations, and experiments has been obtained. Thus, the feasibility of the given converter system has been proven.

CHAPTER 5

CONCLUSION

Energy conversion is the main issue of the power electronics and widely applied in today's world. The AC energy present in the utility grid is usually required to be converted to DC form for a variety of applications. For this purpose, modern power electronic converters provide high efficiency and low harmonic distortion contribution to the line. The structure of an AC/DC power electronic converter generally consists of two stages: an input stage providing AC/DC conversion with high input power factor and low harmonic distortion contribution, and an output stage performing DC/DC conversion with high efficiency and low EMI. In this thesis study, analysis, design and practical implementation of such a converter are performed. The input stage is a two-phase interleaved boost converter based power factor corrector converting the AC line voltage to DC voltage with unity input power factor and low THD on the line. The output stage is an isolated full bridge DC/DC converter employing zero voltage switching to improve efficiency and increase the switching frequency.

The first chapter of the thesis provided a literature summary and the goal of this thesis which is to analyze the performance of such a converter, to design a 2.5 kW converter, and finally manufacture and test its performance to verify the theory by experiments.

In the second chapter, the input/output PWM ripple reduction and magnetic component size reduction attributes of the interleaved PFC converter were analytically investigated and it was shown that the converter provides significant

ripple and size reduction. The conclusion arrived in this chapter was that the interleaved PFC converter solution is favorable for kW power rating converters as the ripple reduction is significant and the magnetic component size reduction is quite significant when the power rating is high. It has become obvious for the given 2.5 kW power rating the two-phase interleaved converter structure is satisfactory and increasing the phase number does not yield additional benefits for typical applications.

Also in Chapter 2, the controller design was approached systematically and using the small signal converter model, the system transfer functions have been derived and utilizing these models, the controller design for the closed loop control of the system has become an easy task. Thus, at this step, design guidelines have been provided for the controller design. The controller involved a cascade control structure using an output voltage control loop with a bandwidth approximately equal to one third of the line frequency and an inner current loop (based on average mode current control principle) with a bandwidth of 2.8 kHz for the PWM frequency of 40 kHz. The design was verified by detailed computer simulations.

In Chapter 2, the final stage involved the monolithic chip based control implementation of the two-phase interleaved PFC converter. This is one of the novel features of the thesis, as this chip has recently become available on the market and it provides advantageous features compared to the conventional implementation which involves the development of such a controller (involving the phase shift between the phases and the parallel operation of the current loops) by the design engineers. Having completed the design and system hardware manufacturing, the converter performance was verified by detailed laboratory experiments. It has been illustrated that the 2.5 kW PFC converter provides unity input power factor and low input current THD of 4% which is less than the typical modern benchmark value of 5% for such equipment.

In chapter 3, the DC/DC converter was taken into consideration. The main focus of this chapter being the controller design and practical implementation, analytical approach to voltage mode control design has been followed and the controller design guideline was established. The theoretical design has been found inapplicable in practice due to the transformer core saturation during dynamic transients (as the magnetization flux builds up a DC offset). And flux offset canceling methods have been considered and applying such methods has yielded minor performance improvement when the control bandwidth is high. Based on this fact, the controller bandwidth was reduced to a much narrower range than the switching frequency of the converter allows. This issue has been investigated by simulations and experiments. This important result indicates that the voltage mode control approach has limited performance and more secure approach that yields high bandwidth is the current mode control where it is easier to track the transformer primary current DC offsets and manipulate them. As this approach has been left as a future work, in the present system the voltage loop was designed to have 780 Hz bandwidth for the 50kHz PWM frequency of the system, which is a quite low bandwidth, perhaps one tenth of the theoretically feasible when the core saturation is not considered.

In Chapter 3 in addition to the control performance related contributions discussed above, the converter hardware implementation and its input/ouput performance results have been reported and background provided for the integrated AC/DC converter system study and implementation.

In Chapter 4, the input PFC stage and the output FB DC/DC converters stage are integrated in order to manufacture a high performance isolated AC/DC converter with high input power factor. In this, chapter the integration process is explained in detail and the results of the experiments at 2.5 kW and 1.25 kW output power are given. It has been shown that the input and output electrical performance of the AC/DC converter is high and at full load, the input current THD and power factor were found as 3.5% and unity. Due to the duty cycle loss and the circuit parasitic components, with small output capacitor size the output ripple voltage becomes large (10 V peak to peak for the 48 V DC output voltage rating). The capacitor size has to

be increased compared to the implemented value or the transformer and circuit design has to be modified in order to reduce the ripple to acceptable values for typical telecom power supplies and other sensitive applications (which require voltage ripple in the range of 1-5%). The input to output converter efficiency under full load has been measured as 86.7% which is an acceptable level for modern converters. The controller dynamic performance for both the PFC controller and the DC/DC converter controllers have been experimentally verified and the targeted reference tracking and load disturbance performance characteristics were obtained.

During the thesis study, some limitations of the given hardware and the designed controllers have been found and methods to overcome these limitations are described as future work. The power level of the output stage is verified as 5 kW in [5], therefore the input PFC stage is designed for supplying 5 kW output power to the output stage. But due to the some problems caused by the EMI propagation and circuit non–idealities, the boost switch of the PFC stage failed for output power ratings above 3 kW. The gate driver circuit of the PFC converter has been found the problematic unit and its enhancement is left as future work for the purpose of extending the power rating to the full 5 kW where the AC/DC converter will be tested at.

The control bandwidth of the outer voltage loop of the input PFC stage for the current design very low, which is approximately one fifth of the twice line frequency. Therefore, the dynamic performance of the PFC is very poor. There are some methods, such as the load current disturbance decoupling and feedforward compensation methods proposed for improving the control bandwidth in the literature. The investigation and implementation of these methods are left as future work.

The stress on the semiconductor devices of the PFC stage can further be reduced by implementing the passive and active snubber structures as proposed in the literature. These methods are planned to be investigated and implemented with interleaving to further improve the converter performance in the future.

In the third chapter, the magnetic core saturation problem of the isolation transformer of the output FB DC/DC converter stage was discussed. An attempt to solve this problem by the implementation of the flux resetting algorithm has provided a limited improvement. The main solution of the problem involves implementing a current mode controller rather than the voltage mode controller. This subject is also left as future work.

In summary, this thesis provides a comprehensive analysis, design, and implementation of an isolated two stage AC/DC converter with high input power factor and high efficiency. The theory, analysis and design methods involved in this thesis are verified by means of computer simulations and experimental studies. This thesis helps the design engineer understand and design such a converter using a rigorous mathematical approach and provides experimental data for performance evaluation such power converter systems.

REFERENCES

[1] N. Mohan, T. M. Undeland, W. P. Robbins, "Power electronics: converters, applications, and design" *John Wiley & Sons*, Second Edition, 1995.

[2] T. Ünal , "Design of a single phase full bridge diode rectifier power factor corrector educational test system", *Msc. Thesis*, METU, 2006.

[3] D. J. Perreault, J.G. Kassakian, "Distributed interleaving of paralleled power converters", *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 44, Issue 8, pp.728–734, 1997.

[4] R. L. Steigerwald, "Power Electronic Converter Technology," *Proceedings of the IEEE*, vol. 89, Issue 6, pp. 890-897, 2001.

[5] M. Uslu, "Analysis, Design and Implementation of a 5 KW Zero Voltage Switching Phase–Shifted Full–Bridge DC/DC Converter Based Power Supply for Arc Welding Machines", *MSc Thesis*, METU, 2006.

[6] M. M. Jovanović, J Yungtaek, "State-of-the-art, single-phase, active power-factor-correction techniques for high-power applications – an overview", *IEEE Transactions on Industrial Electronics*, vol. 52, Issue 3, pp. 704-708, 2005.

[7] K. C. Wu, "Switch-Mode Power Converters: Design and Analysis", *Academic Press*, 2005.

[8] H. B. Shin, J.G. Park, S.K. Chung, H.W. Lee, T.A. Lipo, "Generalised steady-state analysis of multiphase interleaved boost converter with coupled inductors", *IEEE Proceedings on Electric Power Applications*, vol. 152, Issue 3, pp. 584 – 594, May 2005.

[9] A. E. Fitzgerald, C. Kingsley, S. D. Umans, "Electric Machinery", *McGraw–Hill*, 1983.

[10] S. Chandrasekaran, L. U. Gökdere, "Integrated magnetics for interleaved DC-DC boost converter for fuel cell powered vehicles", *Power Electronics Specialists Conference*, vol. 1, pp. 356–361, 2004.

[11] W. Tang, F.C. Lee, R. B. Ridley "Small signal modeling of average current mode control", *IEEE Transactions on Power Electronics*, vol. 8, Issue 2, pp. 112-119, April 1993.

[12] L. Dixon, "Average current mode control of switching power supplies", *Unitrode Power Supply Design Seminar Manual SEM700*, 1990.

[13] J. Sebastian, M. Jaureguizar, J. Uceda, "An overview of power factor correction in single-phase off-line power supply systems", In *20th International Conference on Industrial Electronics, Control and Instrumentation,* vol. 3, pp. 1688-1693, 1994.

[14] R. W. Erickson, D. Maksimović, "Fundamentals of power electronics", *Springer*, 2nd Edition, 1999.

[15] F. A. Huliehel, F. C. Lee, B. H. Cho, "Small-signal modeling of the single-phase boost high power factor converter with constant frequency control", In *IEEE Power Electronics Specialists Conference Records*, vol.1, pp. 475–482, 1992.

[16] W. Tang, F. C. Lee, R. B. Ridley, "Small–signal modeling of average current mode control", *IEEE Transactions on Industrial Electronics*, vol. 8, Issue 2, pp. 112–119, 1993.

[17] G. Spiazzi, P. Mattavelli, and L. Rossetto, "Methods to improve dynamic response of power factor preregulators: An overview," *Proc. IEE European Power Electronics (EPE) Conf.*, vol. 3, pp.754–759, 1995.

[18] G. Spiazzi, P. Mattavelli, and L. Rossetto, "Power factor preregulators with improved dynamic response," *IEEE Transactions on Power Electronics*, vol. 12, pp. 343–349, 1997.

[19] A. Prodic, "Compensator design and stability assessment for fast voltage loops of power factor correction rectifiers", *IEEE Transactions on Power Electronics*, vol. 22, pp. 1719–1730, 2007.

[20] "UCC28070, Interleaving continuous current mode PFC controller datasheet" *Texas Instruments document: SLUS794A*, pp. 26–27, March 2008.

[21] "HGTG30N60B3D Datasheet" *Fairchild semiconductors*, April 2004.

[22] "FFH30S60S Datasheet" *Fairchild semiconductors*, September 2007.

[23] S. V. Oknaian, S. J. Brown, "Inductor current synthesizer for switching power supplies", *United States Patent 6381159*, April 2002.

[24] J. A. Sabate, V. Vlatkovic, R. B. Ridley, F.C. Lee, B. H. Cho, "Design considerations for high-voltage high-power full-bridge zero-voltage-switched PWM converter", *Applied Power Electronics Conference and Exposition Proceedings*, pp. 275 – 284, March 1990.

[25] "SKM 100GB125DN Datasheet", *Semikron*.

[26] V. Vlatkovic, J. A. Sabate, R. B. Ridley, F.C. Lee, B. H. Cho, "Small-signal analysis of the phase-shifted PWM converter", *IEEE Transactions on Power Electronics*, vol. 7, Issue 1, pp. 128–135, 1992.

[27] Y. Duan, H. Jin, "Digital controller design for switch mode power converters", *Applied Power Electronics Conference and Exposition*, vol. 2, pp. 967–973, 1999.

[28] TMS320F280X Data Manual, pp. 60–64, 2006.

[29] J. A. Claassens, I. W. Hofsajer, "A flux balancer for phase shift ZVS DC-DC converters under transient conditions", *Applied Power Electronics Conference and Exposition*, pp. 523–527, 2006.

[30] X. Xiaofeng "Small-signal model for current mode control full-bridge phase-shifted ZVS converter", *Power Electronics and Motion Control Conference Proceedings*, vol.1, pp.514–518, 2000.

[31] K. Dierberger, D. Grafham, "Optimizing the design of 3.5kW single MOSFET power factor correctors", *Application Note*, Advanced Power Technologies.

APPENDIX A

CIRCUIT LAYOUTS OF THE POWER AND CONTROL BOARDS OF THE PFC CONVERTER

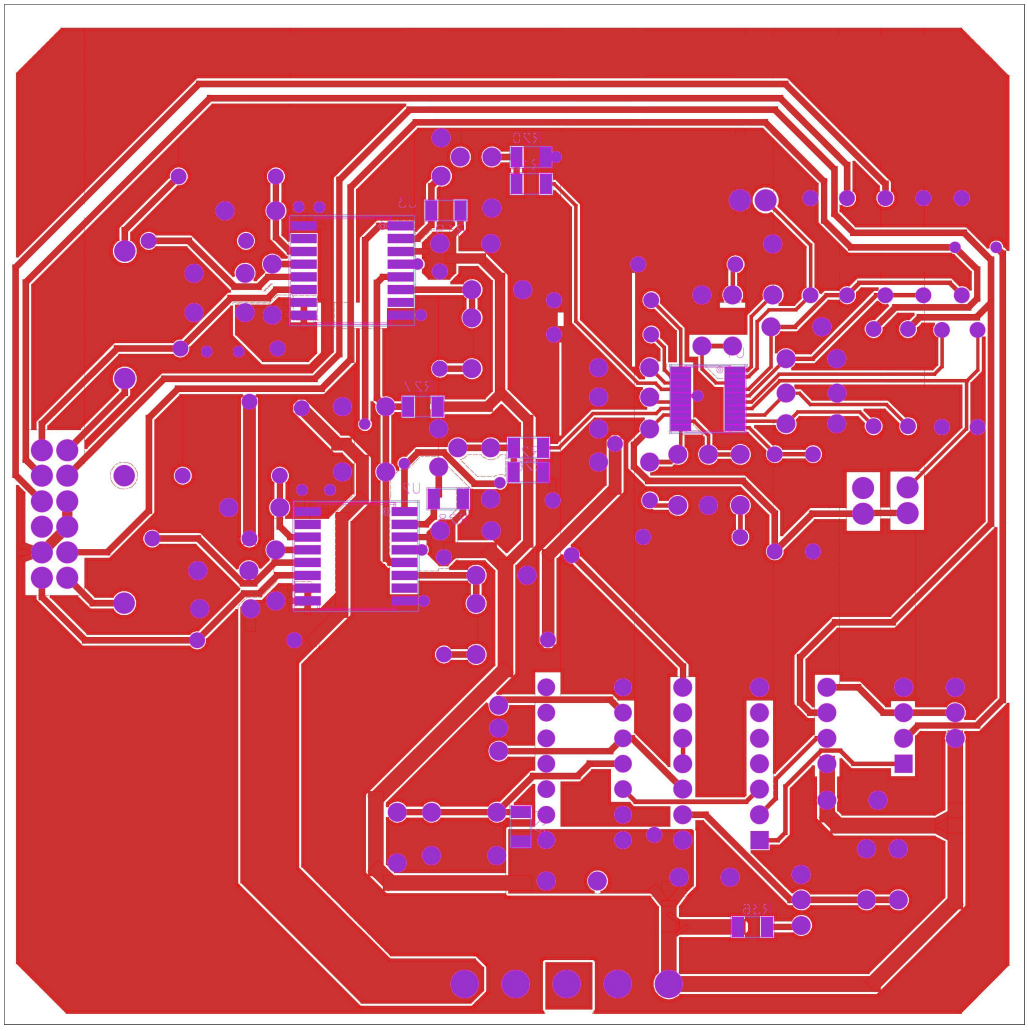

Figure A.1 PFC converter control board bottom side circuit layout.

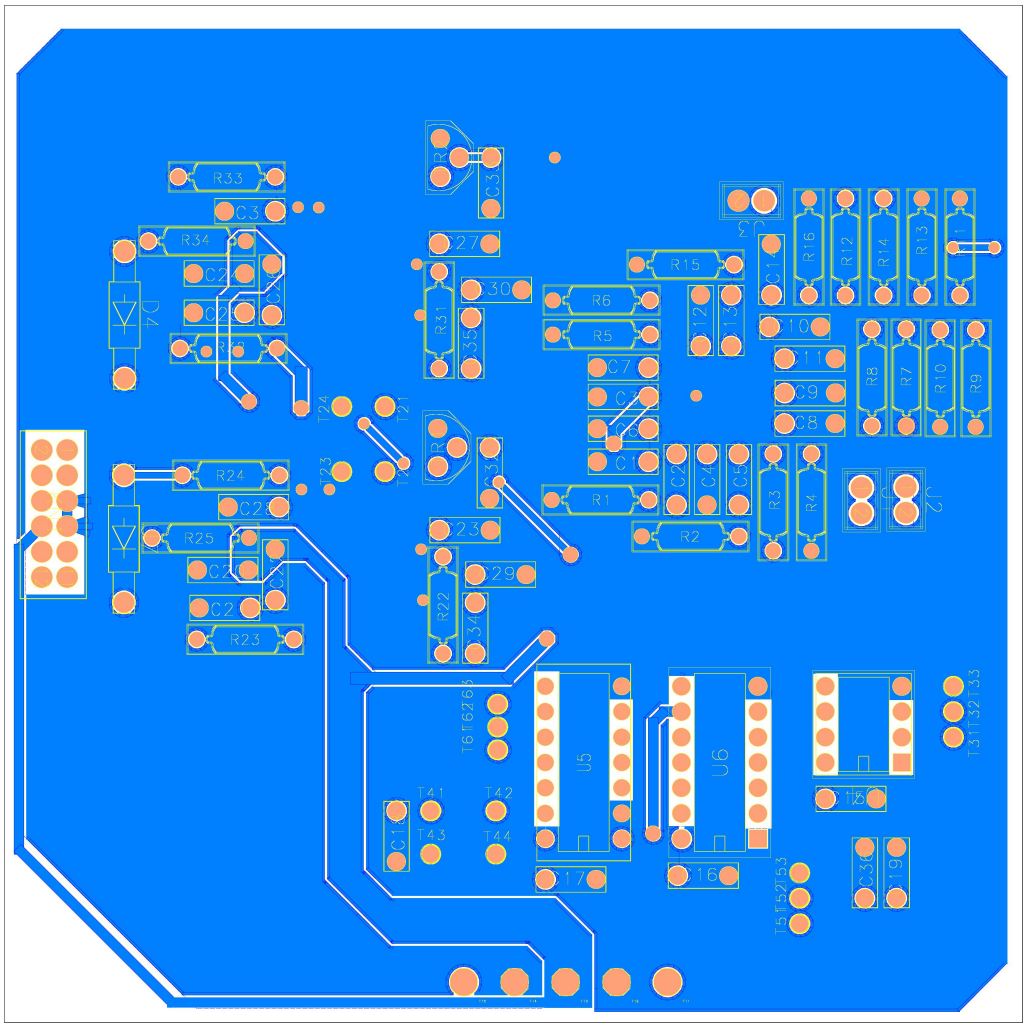

Figure A.2 PFC converter control board top side circuit layout.

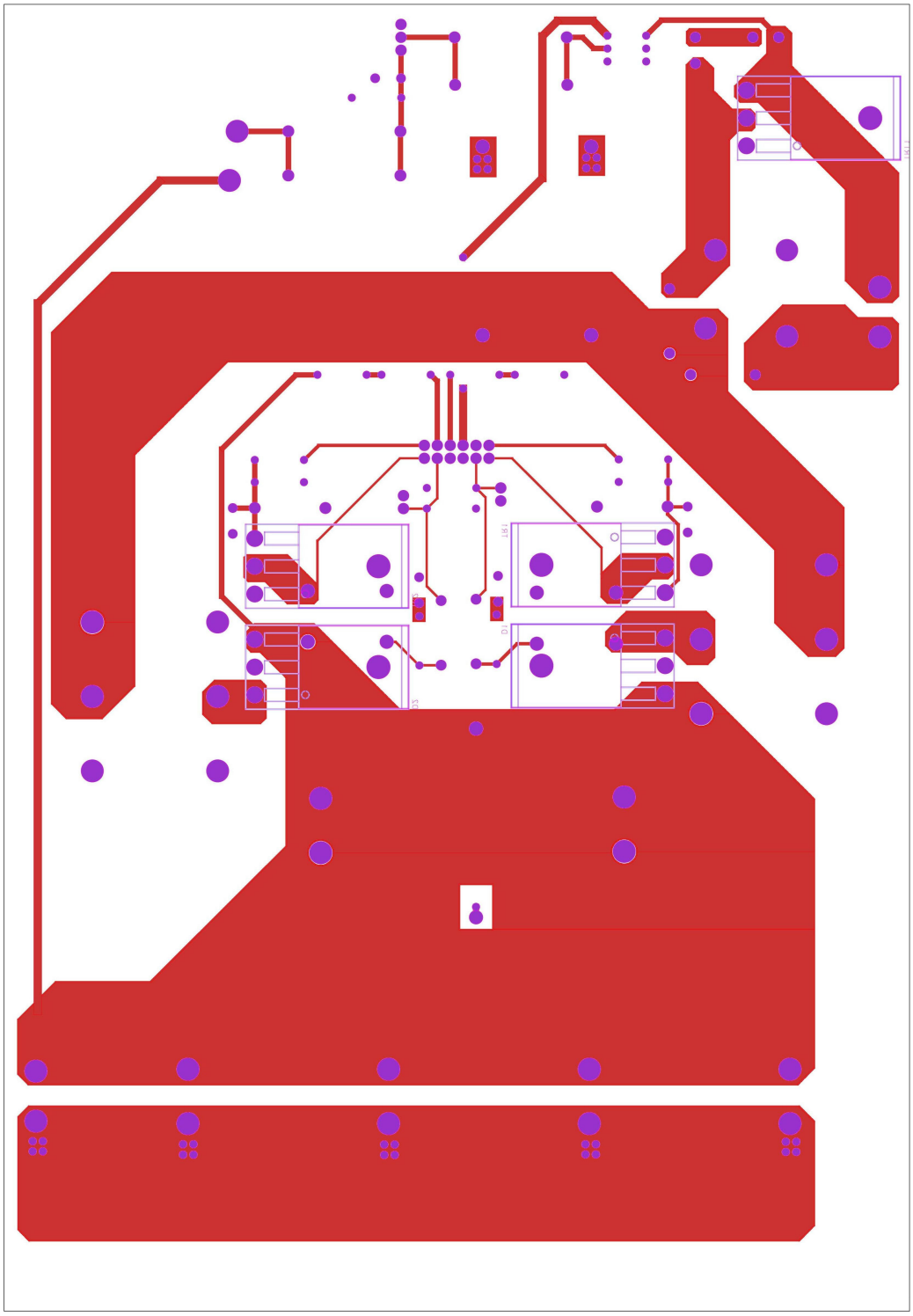

Figure A.3 PFC converter power board bottom side circuit layout.

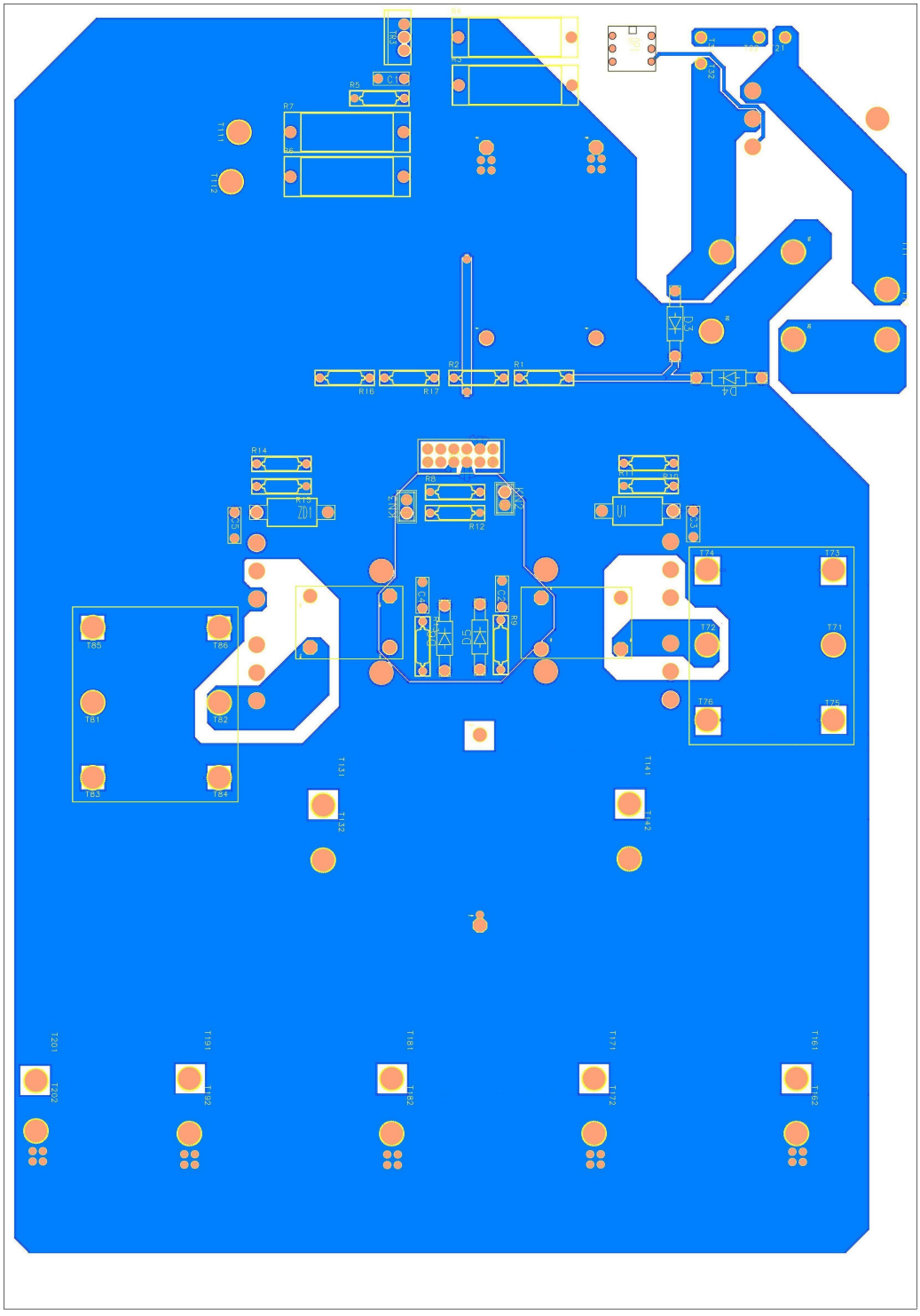

Figure A.4 PFC converter power board top side circuit layout.

APPENDIX B

CIRCUIT SCHEMATICS OF THE POWER AND CONTROL BOARDS OF THE PFC CONVERTER

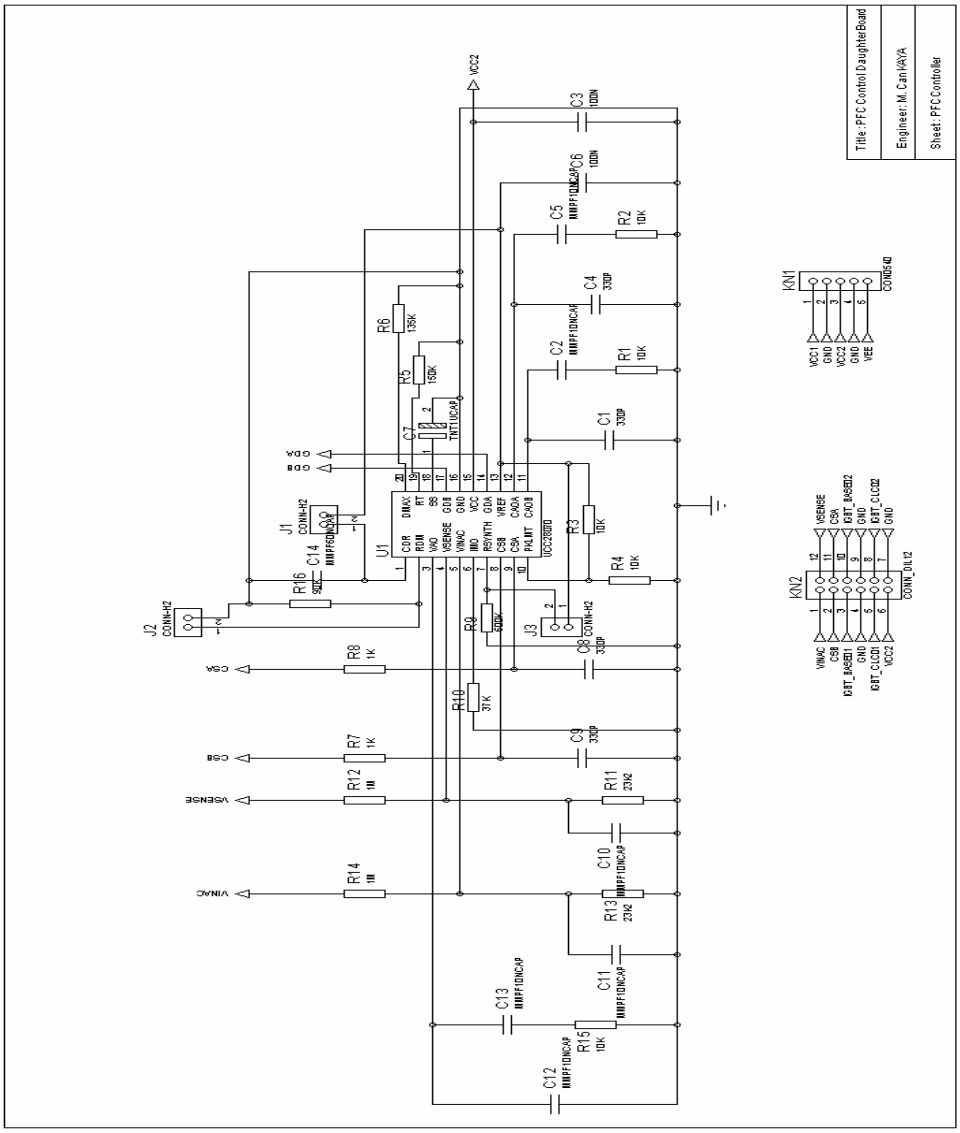

Figure B.1 The PFC control board circuit schematic (sheet 1).

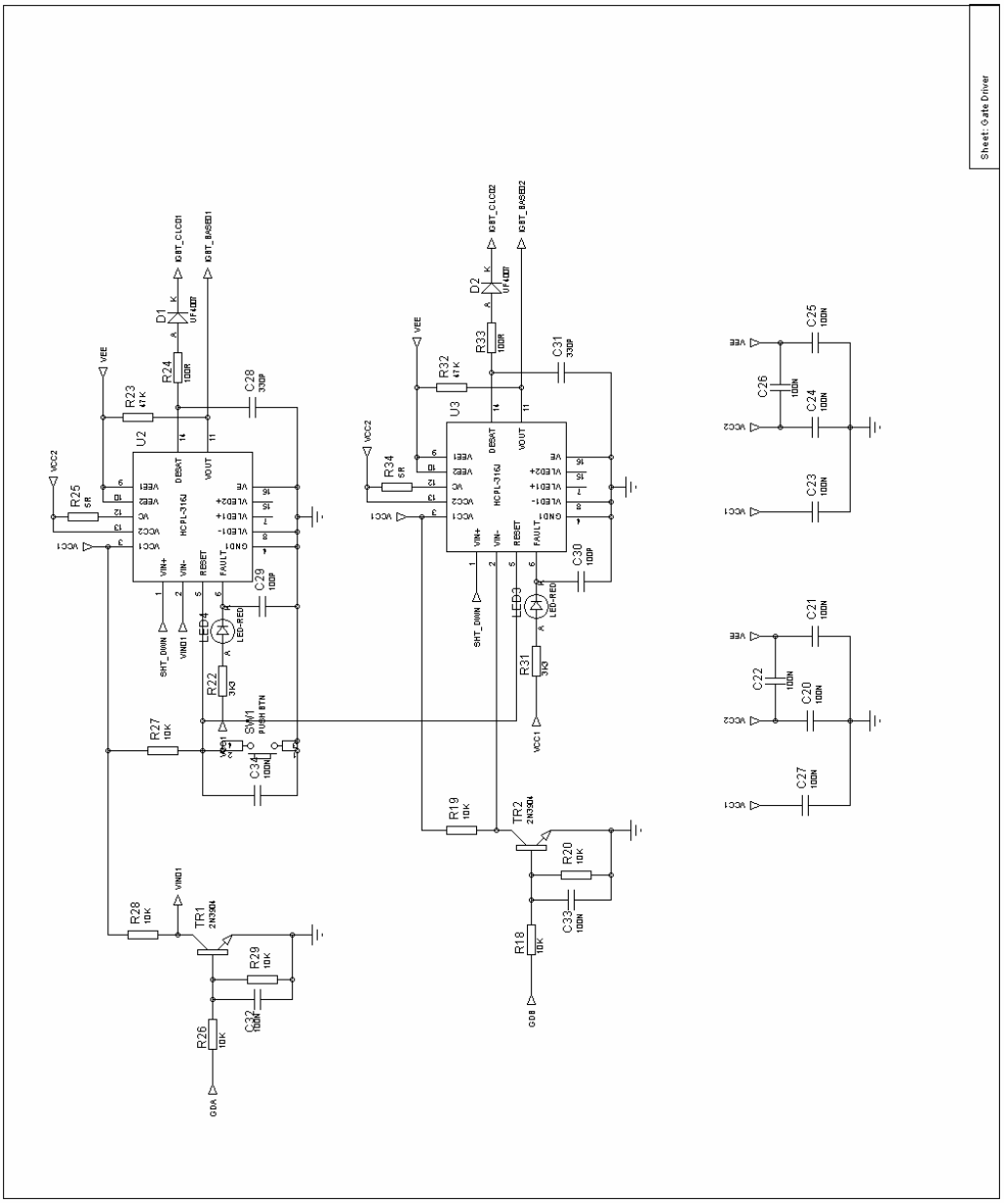

Figure B.2 The PFC control board circuit schematic (sheet2).

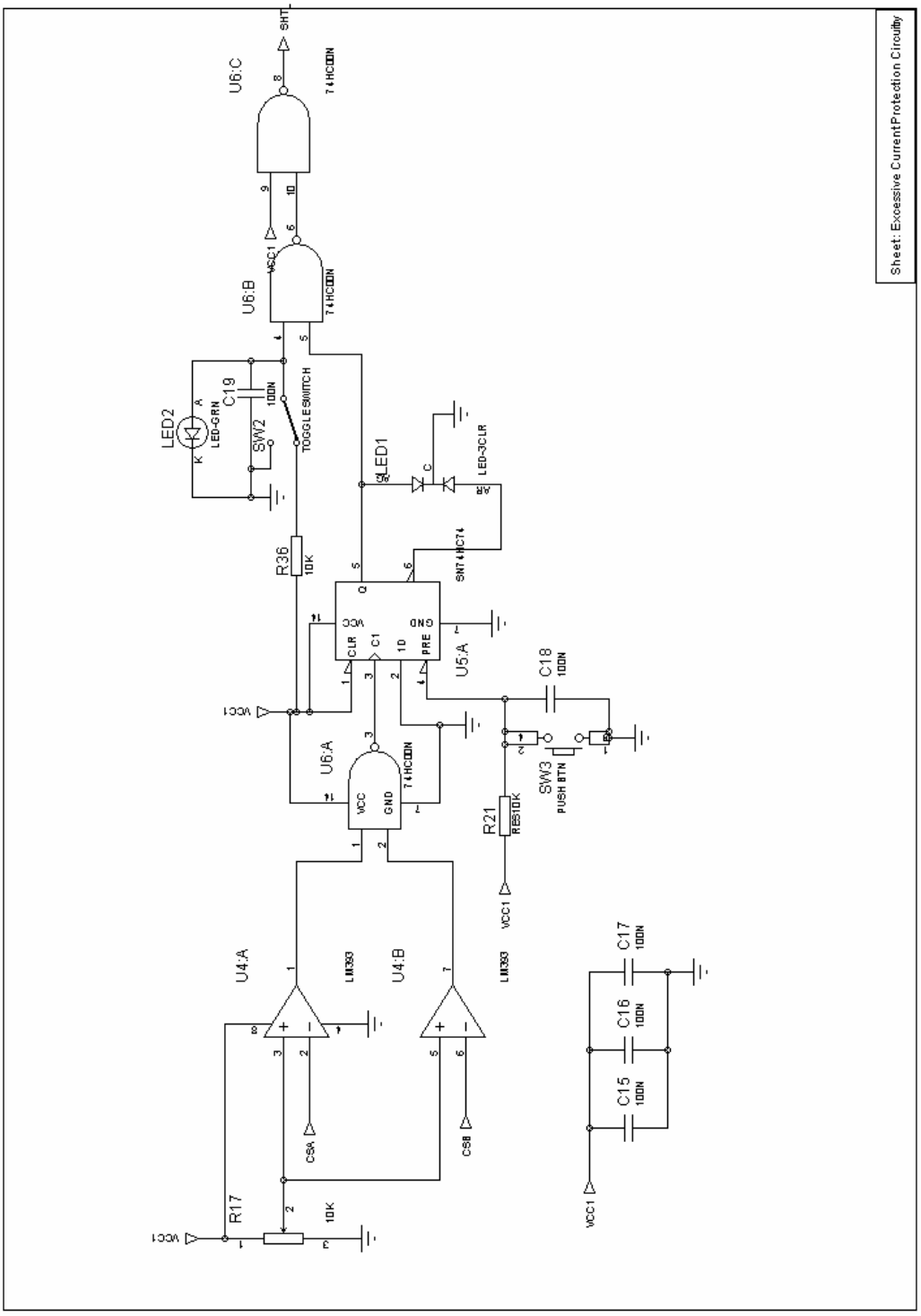

Figure B.3 The PFC control board circuit schematic (sheet 3).

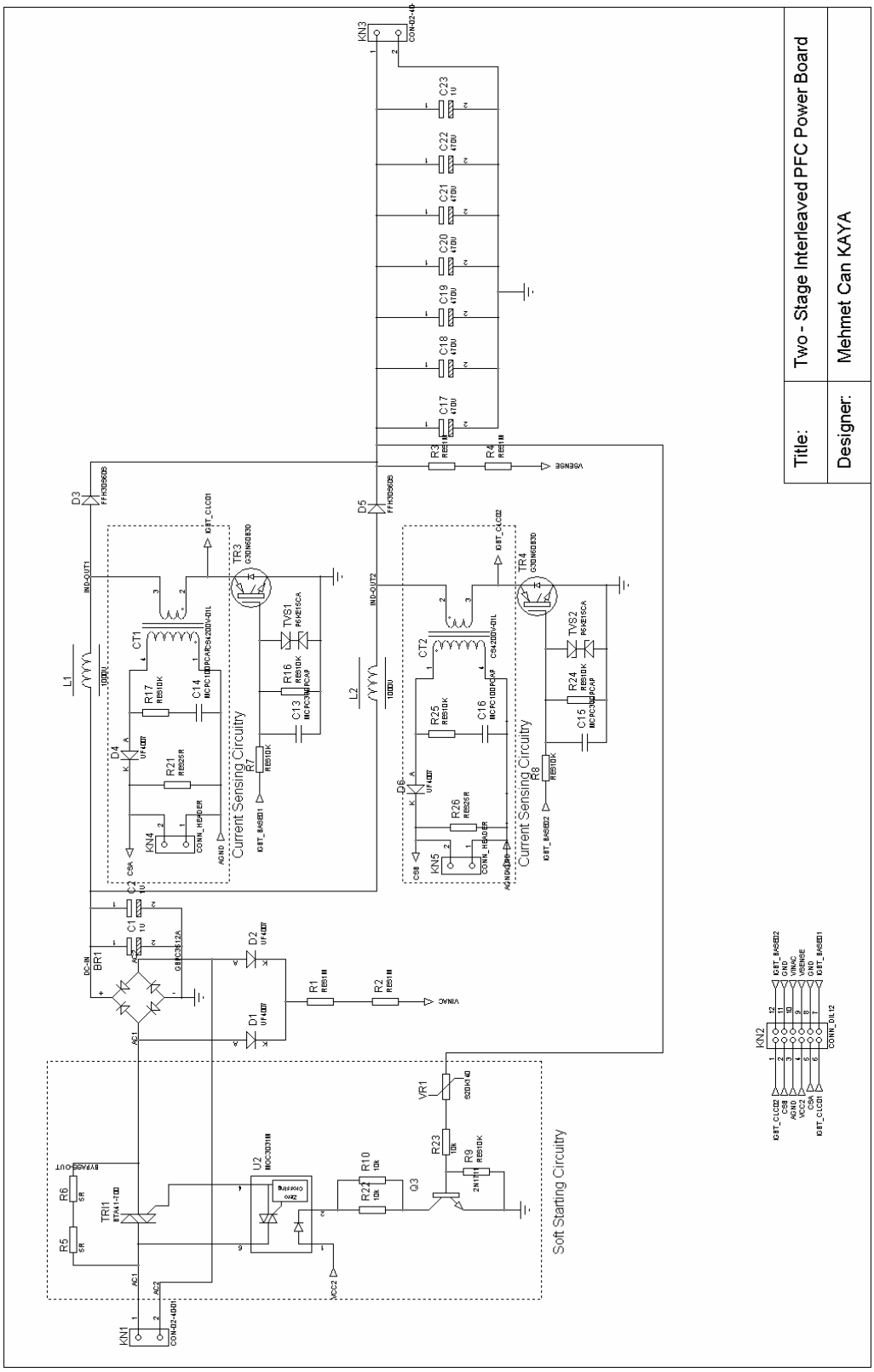

Figure B.4 The PFC power board circuit schematic.

APPENDIX C

PHOTOGRAPHS OF THE CONVERTERS

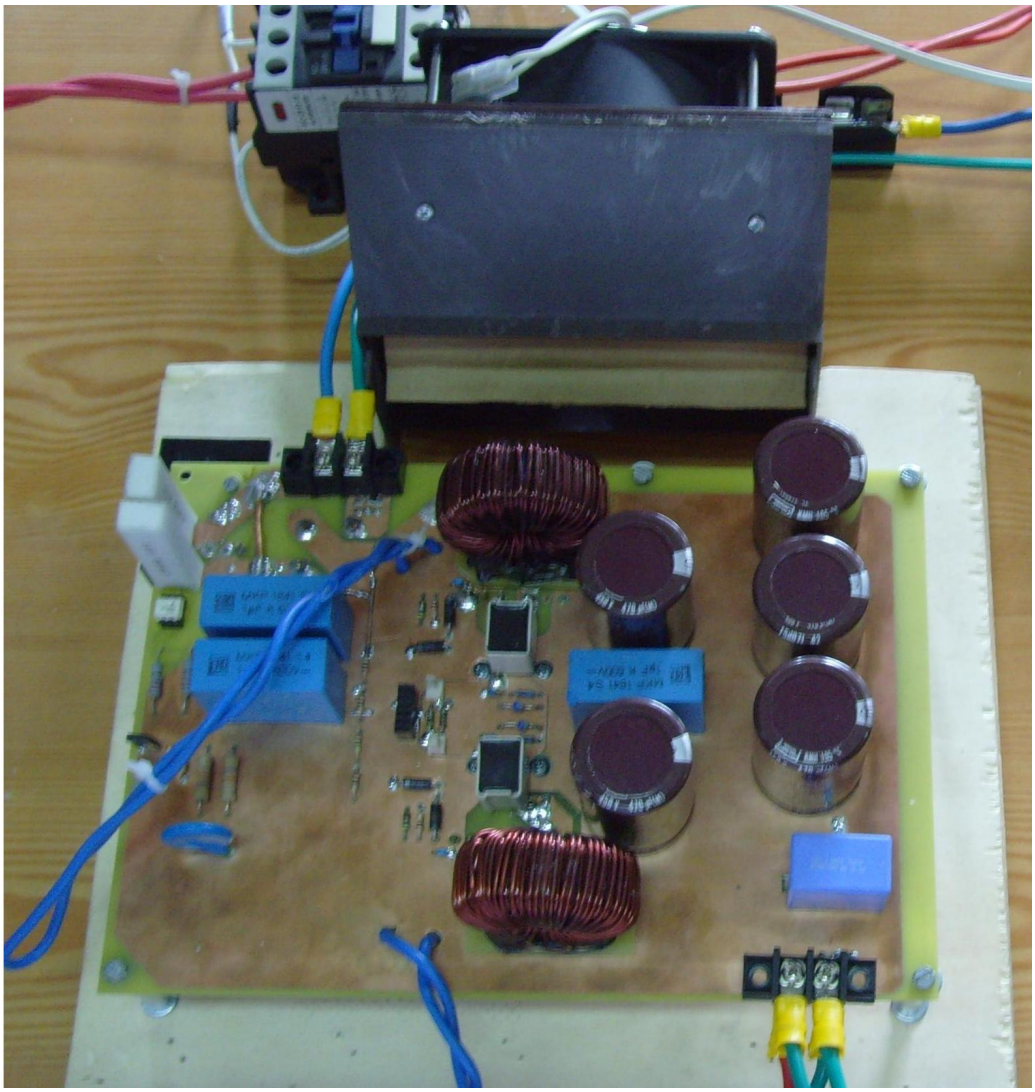

Figure C.1 The input PFC stage power board.

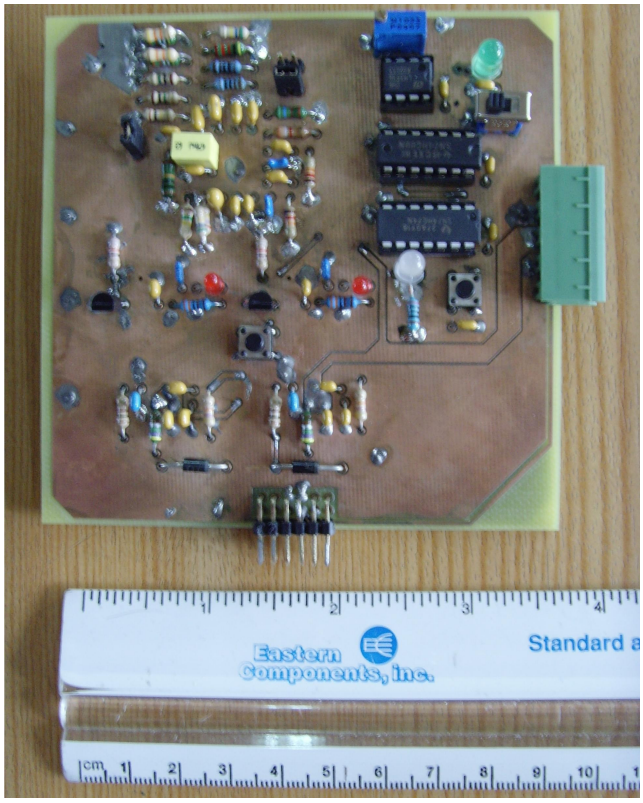

Figure C.2 The input PFC stage control board (front side).

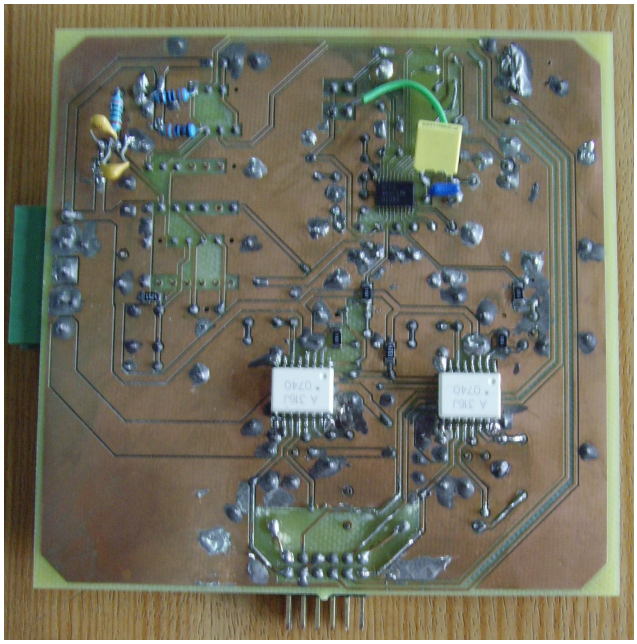

Figure C.3 The input PFC stage control board (back side).

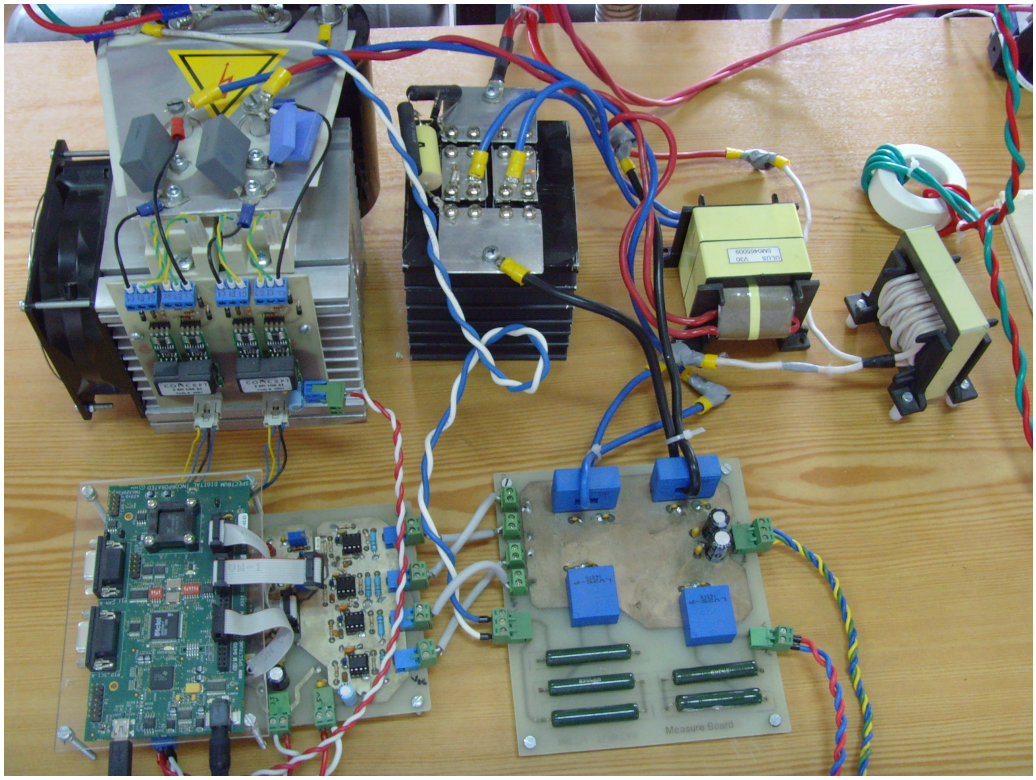

Figure C.4 The output FB–PS–ZVS DC/DC converter stage.